SIEMENS

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Data Book 1980/81

ICs for Entertainment Electronics

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SIEMENS AKTIENGESELLSCHAFT

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▼ New type
■ Not for new design

1. New type nomenclature for ICs[1])

The code consists of: **Three letters** followed by a **serial number**

First two letters

A. Individual circuits

The **first letter** identifies the circuit as:
S: Individual digital circuit
T: Analog circuit
U: Mixed analog/digital circuit
The **second letter** has no special significance, except the letter H which stands for hybrid circuits.

B. Family circuits

These are digital circuits related in their specifications and primarily designed to be mutually connected.

The first two letters identify the family.

The **third letter:** indicates the operational temperature range or, exceptionally, another significant characteristic.

A — No temperature range specified
B — 0 to 70 °C
C — −55 to 125 °C
D — −25 to 70 °C
E — −25 to 85 °C
F — −40 to 85 °C

If a circuit is designed for a wider temperature range, but does not qualify for a higher classification, the code letter for the narrower temperature range is used.

The **serial number** may either be a 4-digit number (stated by PRO ELECTRON) or a serial number (combining figures and perhaps numbers) of an existing company number. Company numbers consisting of less than four digits are extended to a fourdigit number by adding zeroes (0) in front.

A version letter may be added to indicate a variation of the basic type. Thus, slight changes of the basic type or the case may be designated. Version letters have no fixed significance, except letter Z: connection as specified by customer ("customized wiring").

The following letters are used for the different package outlines:

C — Cylindrical package
D — Dual in-line ceramic
F — Flat pack
P — Dual in-line plastic
Q — Quadruple in-line
U — Chips, not encased

1) Applied since 1973.

Former type nomenclature:

First two letters: same as new code.
The third letter: indicates the function

H — Combinatorial circuit
J — Bistable or multistable sequential circuit (static)
K — Monostable sequential circuit
L — Level converter (dynamic)
N — Bi-metastable or multi-metastable sequential circuit
Q — Read-write memory
R — Read-only memory
S — Sense amplifier with digital output
Y — Miscellaneous

The third figure (of the serial number comprising three figures) indicates the operating temperature range.

0 — No temperature range specified
1 — 0 to 70 °C
2 — −55 to 125 °C
3 — −10 to 85 °C
4 — 15 to 55 °C
5 — −25 to 70 °C
6 — −40 to 85 °C

2. Mounting instructions

2.1 General

With MOS components, it must be observed that no currents will flow between substrate and solder bath or soldering iron respectively. It is therefore recommended, to ground the connections to be soldered as well as the solder bath and/or the solder iron.

During preparation and assembly on the PCB, the MOS circuits need protection against static overvoltages and electrical spikes. On no account, MOS circuits are allowed to be taken from or inserted into the circuit while the operating voltage is applied.

2.2 **Plastic plug-in packages**

Plastic plug-in packages are soldered on the reverse side of the printed circuit board, opposite the package. The package pins are bent down by 90° and fit into holes 2.54 mm apart, with hole diameters of 0.7 to 0.9 mm. Dimension X should be taken from the appropriate dimensional drawing of the package.
The bottom of the package does not touch the printed circuit board surface after its insertion, as the pins widen at a proper distance from the package (see figure).
After inserting the package into the printed circuit board it is advantageous to bend two pins at an angle of approximately 30° towards the board. This way the pakage does not need to be held down during the soldering process.

Dimensions in mm

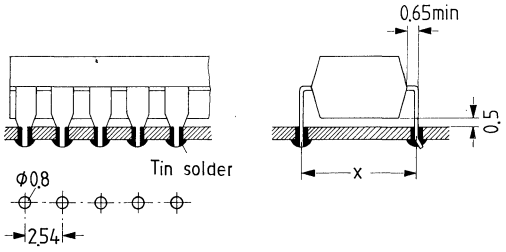


Fig. 1

2.3 **Package 5 H8 DIN 41873 and similar packages with 8, 10, and 12 pins**

The case may be mounted in any position. The pins may be bent sideways at a minimum distance of 1.5 mm from the case according to the hole distance (fig. 2). Pins that are too long should be clipped before soldering. Iron or dip soldering may be employed.

Dimensions in mm

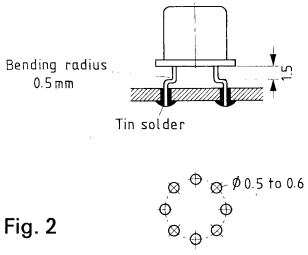


Fig. 2

2.4 **Hints for soldering**

Solder temperature: max. 260 °C

Soldering duration: dip soldering max. 5 sec
iron soldering max. 10 sec

3. Glossary of terms

3.1. Bipolar circuits

Main terms

a	Suppression, rejection
a	Intermodulation ratio
a	Attenuation
AC	Alternating current
AF	Audio frequency
AM	Amplitude modulation
B	Bandwidth
C	Capacitance
CMRR	Common mode rejection ratio
DC	Direct current
f	Frequency
Δf	Frequency deviation
FM	Frequency modulation
G	Giga (10^9)
G	Gain
Hz	Cycles per second (Hertz)
I	Current
IF	Intermediate frequency
THD	Total harmonic distortion
K	Kelvin
k	Kilo (10^3)
L	Inductance
m	Milli (10^{-3})
M	Mega (10^6)
m	Linearity
m	Modulation factor
MW	Medium wave
NF	Noise figure
P	Power dissipation
Q, Q_B	Q-factor
R	Resistance
RF	Radio frequency
S/N	Signal to noise
SVR	Supply voltage rejection
T	Temperature
t	time
V, V	Voltage
W	Watt
Z	Impedance
Z	Zener

Index terms

AF	Audio frequency
AM	Amplitude modulated
amb	Ambient
B	Base
C	Capacitance
C	Collector
cont	Control
c	Cross talk
cr	Cross talk rejection
D	Differential
d	Disturbance
E	Emitter
fb	Feedback
fly	flyback
FM	Frequency modulated
G	Generator
hum	Hum
i	Input
IF	Intermediate frequency
j	Junction
lim	Limiting
lk	Leakage
mod	Modulated
n	Noise
o	Offset
OD	Overdrive
osc	Oscillator
pot	Potentiometer
pp	Peak to peak
q	Output
RF	Radio frequency
rms	Route mean square
S	Supply
stg	Storage
switch	Switching
sy	System
S/N	Signal to noise
thSA	Thermal (system-air)
thSC	Thermal (system-case)
tot	Total
tun	Tuning
o	Open loop
V, v	Voltage

3.2 MOS circuits

Voltages

V	Voltage, general
V_S	Supply voltage
V_{SS}	Substrate supply voltage
V_{DD}	Drain supply voltage
V_{GG}	Gate supply voltage
V_{iH}	High level at a signal input
V_{iL}	Low level at a signal input
V_{qH}	High level at an output
V_{qL}	Low level at an output
$V_{\Phi H}$	High level at a clock input
$V_{\Phi L}$	Low level at a clock input
V_i	Voltage at a signal input
V_R	Reset voltage

Currents

I_{DD}	Drain supply current
I_{GG}	Gate supply current
I_q	Output current, general

Resistances

R_{qH}	High level output resistance
R_{qL}	Low level output resistance
R_q	Load resistance at an output
R_i	Input resistance at a signal input
R_Φ	Input resistance at a clock input
R	Resistance

Capacitances

C	Capacitance
C_i	Input capacitance
C_Φ	Input capacitance at a clock input
C_q	Output load capacitance

Frequencies

f_i	Input frequency
f_Φ	Clock frequency

Power

P	Power dissipation (power consumption)
P_{tot}	Total power dissipation

Temperatures

T_{amb}	Ambient temperature
T_{stg}	Storage temperature

Timing

t_d	Delay time
t_{pd}	Propagation delay
t_r	Rise time
t_f	Fall time
t_t	Transition time
t_w	Pulse width
t_{tHLq}	Transition time HL of the output signal
t_{tLHq}	Transition time LH of the output signal
t_{dHLq}	Delay of the HL transition of the output signal
t_{dLHq}	Delay of the LH transition of the output signal
$t_{wH\Phi}$	Pulse width at the H-level of the clock signal
$t_{wL\Phi}$	Pulse width at the L-level of the clock signal
$t_{tHL\Phi}$	HL transition time of the clock signal
$t_{tLH\Phi}$	LH transition time of the clock signal
$t_{dHL\Phi}$	Delay of the HL transition of the clock signal
$t_{dLH\Phi}$	Delay of the LH transition of the clock signal
t_{wHi}	Pulse width at the high level of the input signal
t_{wLi}	Pulse width at the low level of the input signal
t_{tHLi}	HL transition of the input signal
t_{tLHi}	LH transition of the input signal
t_{dLH}	Delay of the LH transition
t_{wHq}	Pulse width at the high level of the output signal

Miscellaneous

t_{cy}	Cycle time
Φ	Clock input
I	Input
I_1	Input 1
I_2	Input 2
$\underline{Q}$	Data output
$\overline{Q}$	Data output inverted

4. Quality specifications

The quality of delivery is specified as follows:

4.1. Maximum and minimum values of characteristics

4.2. Random sample agreement, AQL values (Acceptable Quality Level)

A delivery batch whose defect percentage for a certain value is equal to or less than the specified AQL value will be accepted with high probability (above 90%) during the appropriate random sample inspection with respect to this characteristic value. The average defect percentage of delivered goods generally lies below the AQL value.

4.3. Classification of defects

A defect exists if a characteristic of a component does not comply with the specifications in the data sheet. The defects are divided into major and minor defects with respect to their seriousness, and into mechanical and electrical defects with respect to the type of defect. Unless otherwise specified, the AQL values summarized in section 4 apply to the various groups of defects. The identical random sample plans DIN 40080 (or) ABC-Std 105 are used as a base for attribute inspection.
For each defect group for which an AQL value is specified, only the number of defective units (each with one or more defective characteristics) is evaluated within that defect group.

4.3.1 Division into groups of defects

Depending on the probable effect of the defect on the application circuit, defects are divided into

Group of **major defects**

If such a defect exists, the usefulness for the intended purpose is probably substantially reduced.

Group of **minor defects**

If such a defect exists, the usefulness for the intended application is probably only slightly reduced.

4.3.2 Division according to defect type

A distinction is made between:

Defects in **mechanical characteristics**
(Package and leads)

Defects in **electrical characteristics**

Examples:

Major defects, mechanical characteristics

Broken connections or package, missing identification, wrong packages, bad cracks and cavities in the package, major surface defects, leads which cannot be soldered.

Minor defects, mechanical characteristics

Minor damage to the body surface, identification difficult to read, bent pins, incorrect dimensions.

Major defects, electrical characteristics

Malfunction, open circuit, short circuit, deviation from characteristic values by more than 50%.

Minor defects, electrical characteristics

Minor deviations of voltages and currents, deviations from the dynamic characteristics, provided that they have no major effect on the application.

4.4. **AQL table** for ICs in entertainment electronics

Defect type and defect group	AQL values for	
	bipolar circuits	MOS circuits
Defects at packages and supply lines		
Major defects	0.4	0.4
Minor defects	0.65	0.65
Sum of major and minor defects	0.65	0.65
Electrical defects		
Major defects	0.4	0.4
Minor defects	0.65 [1])	1.0
Sum of major and minor defects	0.65	1.0

Annotation

The higher AQL values for MOS circuits in comparison with bipolar circuits result from the substantially larger functional range.

Incoming inspection

The inspections carried out at the manufacturer's plant are intended to make incoming inspections unnecessary. If the buyer still wishes to carry out incoming inspection, the use of a random sample plan as shown in section 5 is recommended. The testing technology to be used must be agreed upon between the customer and the supplier.

The following details are necessary for assessment of any complaints:

Test circuit, random sample size, number of defective elements found, sample of evidence, number of the packing slip.

1) 2.5 applies to the noise voltage in accordance with DIN 45405.

4.5. **Random sampling test plan for normal inspection**

in accordance with DIN 40080 or ABC-Std 105 D, test level II

Lot size	Sample size	AQL-value										
		0.065	0.10	0.15	0.25	0.40	0.65	1.0	1.5	2.5	4.0	6.5
		A R	A R	A R	A R	A R	A R	A R	A R	A R	A R	A R
2 to 8	2	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	0 1
9 to 15	3	↓	↓	↓	↓	↓	↓	↓	↓	↓	0 1	↕
16 to 25	5	↓	↓	↓	↓	↓	↓	↓	↓	0 1	↑	↓
26 to 50	8	↓	↓	↓	↓	↓	↓	↓	0 1	↑	↓	1 2
51 to 90	13	↓	↓	↓	↓	↓	↓	0 1	↑	↓	1 2	2 3
91 to 150	20	↓	↓	↓	↓	↓	0 1	↑	↓	1 2	2 3	3 4
151 to 280	32	↓	↓	↓	↓	0 1	↑	↓	1 2	2 3	3 4	5 6
281 to 500	50	↓	↓	↓	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8
501 to 1200	80	↓	↓	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11
1201 to 3200	125	↓	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15
3201 to 10000	200	0 1	↑	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22
10001 to 35000	315	↑	↕	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	↑
35001 – 150000	500	↓	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	↑	↑
150001 – 500000	800	1 2	2 3	3 4	5 6	7 8	10 11	14 15	21 22	↑	↑	↑
600001 and more	1250	2 3	3 4	5 6	7 8	10 11	14 15	21 22	↑	↑	↑	↑

A = Number of acceptances; i.e. the maximum number of defective sample elements up to which the lot is accepted,

R = Number or rejections; i.e. the number of defective sample elements, at least achieved when the lot has been rejected.

Additional requirement

As the combination "Acceptance 0 and Rejection 1" has a low degree of significance, the next larger sample-size is to be used.

ICs for Special TV Applications

Video IF/AFC
Quasi-parallel sound
Sound-stage IF amplifier
System for color signal handling in TV receivers in acc. with the PAL standard
ICs for driving purposes
Dividers
Siemens digital tuning system SDA 100 (frequency synthesis)
Siemens digital tuning system SDA 200 (frequency synthesis)

Video IF IC for Black/White and Color TV Sets

TBA 1440 G
TBA 1441

Bipolar circuit

Highly amplifying controlled video IF amplifier including controlled demodulator, low-ohmic video outputs for positive- and negative-going signal, gated control, and delayed tuner control.

TBA 1440 G for pnp tuners
TBA 1441 for npn tuners

- High integration
- Large control range
- High input sensitivity
- Few 1.07 MHz disturbances
- Positive- and negative-going signal
- White and black levels separately adjustable
- Excellent tuning behavior

Type	Ordering code	Package outline
TBA 1440 G	Q67000-A1022	DIP 16
TBA 1441	Q67000-A1224	

Maximum ratings

Supply voltage	V_S	15 [1])	V
Voltages	V_4	5	V
	V_5	20	V
	V_{14}	5	V
Ohmic resistance between pin 8 and 9	$R_{8\text{-}9}$	$\leqq 20$	Ω
Thermal resistance (system-air)	$R_{th\ SA}$	90	K/W
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C

Range of operation

Supply voltage range	V_S	10.5 to 15	V
Ambient temperature range	T_{amb}	−25 to 60	°C

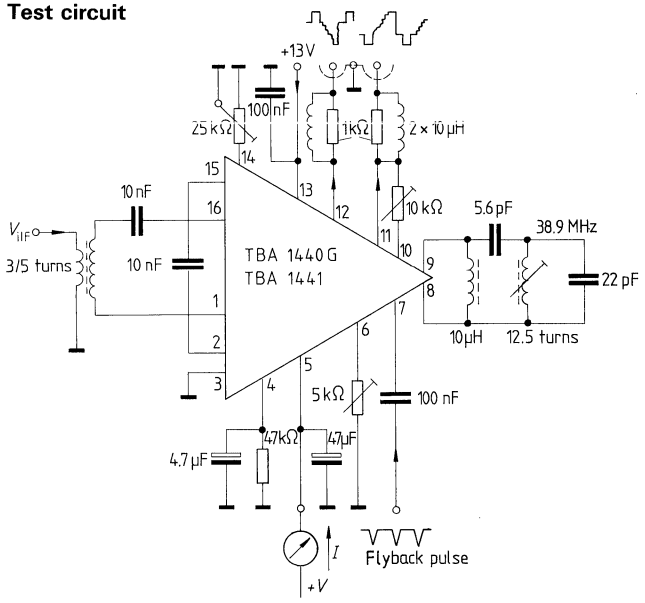
[1]) intermittently 16.5 V

Characteristics (V_{13} = 13 V; f_{IIF} = 38.9 MHz; T_{amb} = 25 °C; all data measured with respect to ground, unless otherwise stated)

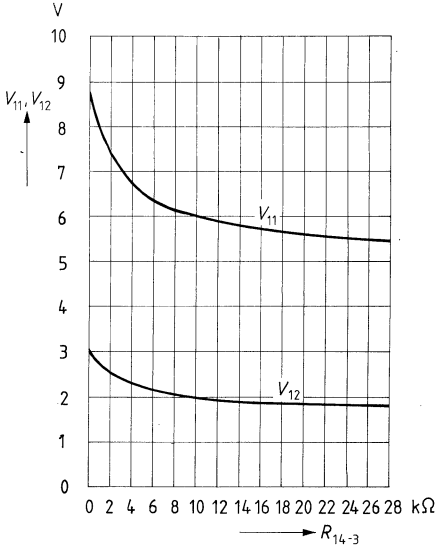
		min	typ	max	
Current consumption	I_{13}	33	42	61	mA
DC voltage at output 11 (V_{13} = 15 V; V_i = 0)					
$R_{14\text{-}3} = \infty$	V_{11}		5.5		V
$R_{14\text{-}3} = 0$	V_{11}		9.6		V
DC voltage at output 12 (V_{13} = 15 V; V_i = 0)					
$R_{14\text{-}3} = \infty$	V_{12}		1.9		V
$R_{14\text{-}3} = 0$	V_{12}		3.5		V
White level deviation	$\Delta V_{11}/\Delta V_{13}$		100		mV/V
	$\Delta V_{12}/\Delta V_{13}$		20		mV/V
Resistance for ΔV_{11} = 1 V	$R_{14\text{-}3}$		8.5		kΩ
AGC threshold V_{10} = sync pulse level for $R_{10\text{-}11} = 0$	$V_{10} = V_{11}$		1.9		V
Resistance for sync pulse level deviation of 1 V	$R_{10\text{-}11}$		2.4		kΩ
Sync pulse level with async or without gating pulses (peak level control)	$V_{11\ sync}$		0.5		V
Video output voltage	V_{video}		3		V
Control current for tuner prestage ($V_5 > 2$ V)	I_5	10	15		mA
(TBA 1440 G: 10 dB after AGC TBA 1441 :10 dB prior to AGC)					
IF control voltage for max gain	V_4	0		0.5	V
for min gain	V_4	2.5		5	V
Gating pulse voltage	$-V_7$	2		5	V
Residual IF (basic frequency)	V_{11}; V_{12}		10		mV
Output current to ground	I_{11}-I_{12}			5	mA
to plus	I_{11}; I_{12}			−1	mA
Input impedance at max gain	$Z_{1\text{-}16}$		1.8/2		kΩ/pF
at min gain	$Z_{1\text{-}16}$		1.9/0		kΩ/pF
Input voltage [1]) for V_{11} = 3 V_{pp}	V_i	70	100	200	µV
Video bandwidth (−3 dB)	B_{video}	6	7		MHz
AGC range	ΔG		55		dB
Intermodulation ratio (1.07 MHz) with reference to color carrier [2])	a		45		dB
Output impedance	$Z_{q\ 8\text{-}9}$		2/2.5		kΩ/pF

[1]) According to test circuit: V_i = rms sync pulse level at 60 Ω
[2]) Test level a_{cc} = − 3 dB
a_{sc} = −20 dB referred to picture carrier

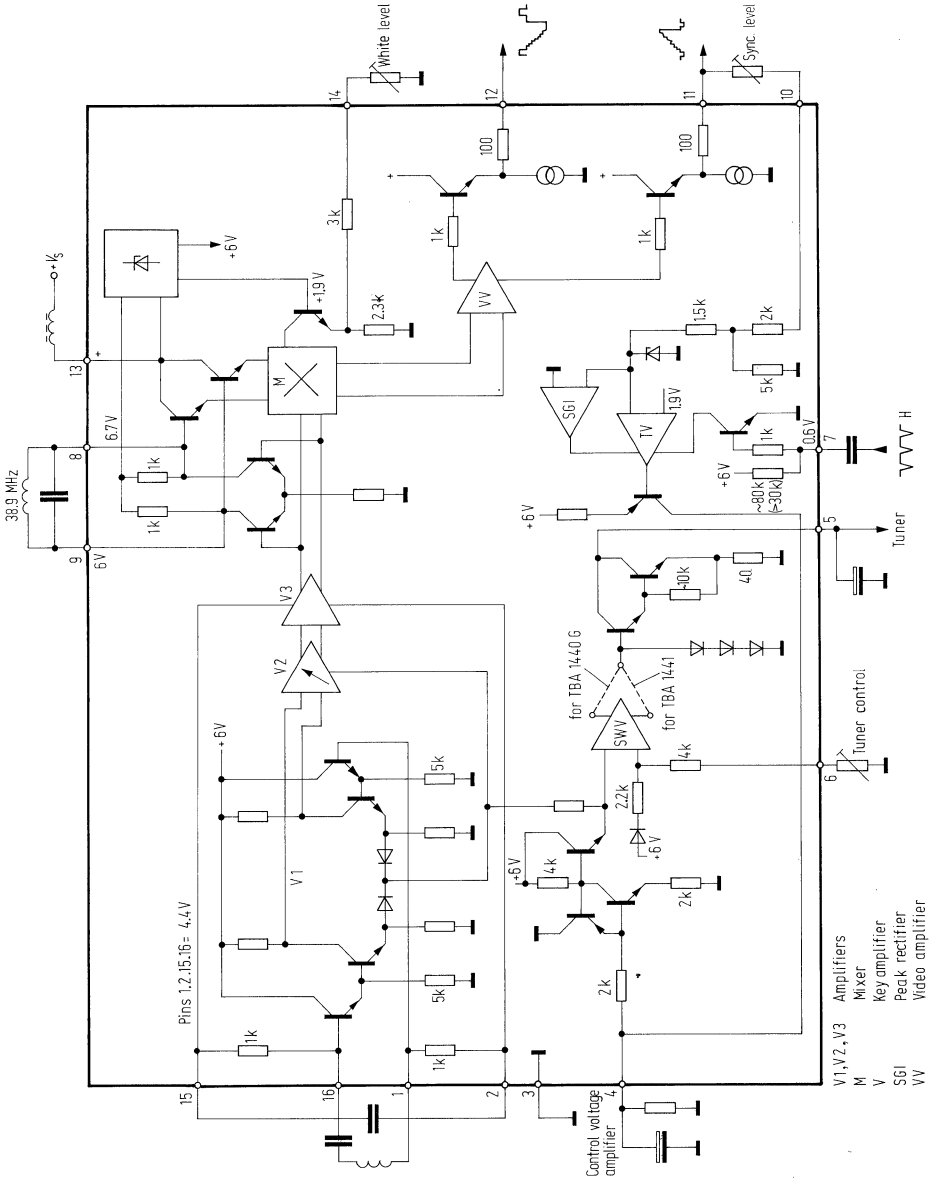
Test circuit



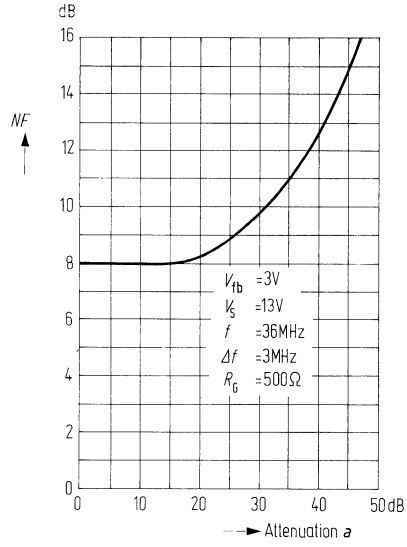
DC output voltage versus white level resistance
V_S = 13 V; $R_{10\text{-}11}$ = ∞



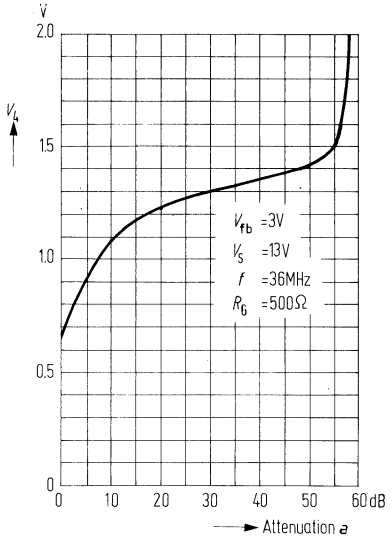
Block diagram



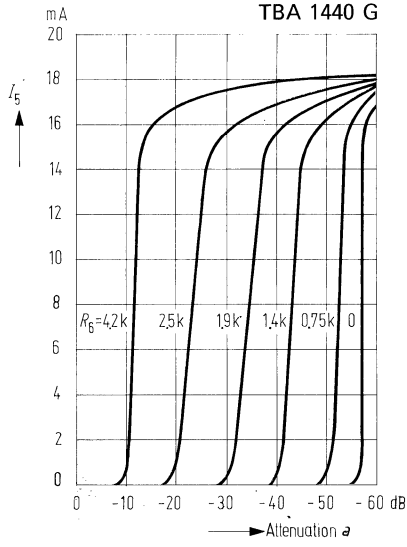
Noise figure versus attenuation
(measured at video frequency)
V_S = 13 V, f = 36 MHz, Δf = 3 MHz,
R_G = 500 Ω, $-V_{fb}$ = 3 V



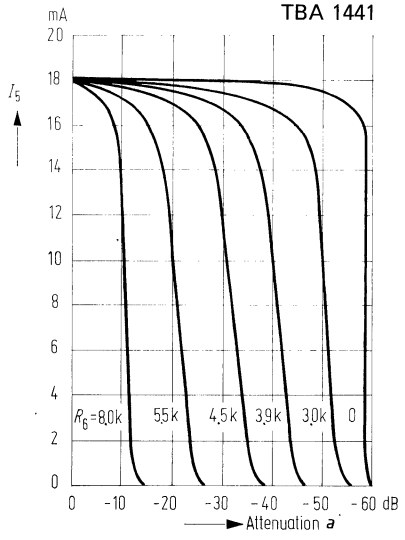
Control voltage versus attenuation
$-V_{fb}$ = 3 V, V_S = 13 V, f = 36 MHz,
R_G = 500 Ω



Tuner control current versus attenuation
R_6 = parameter

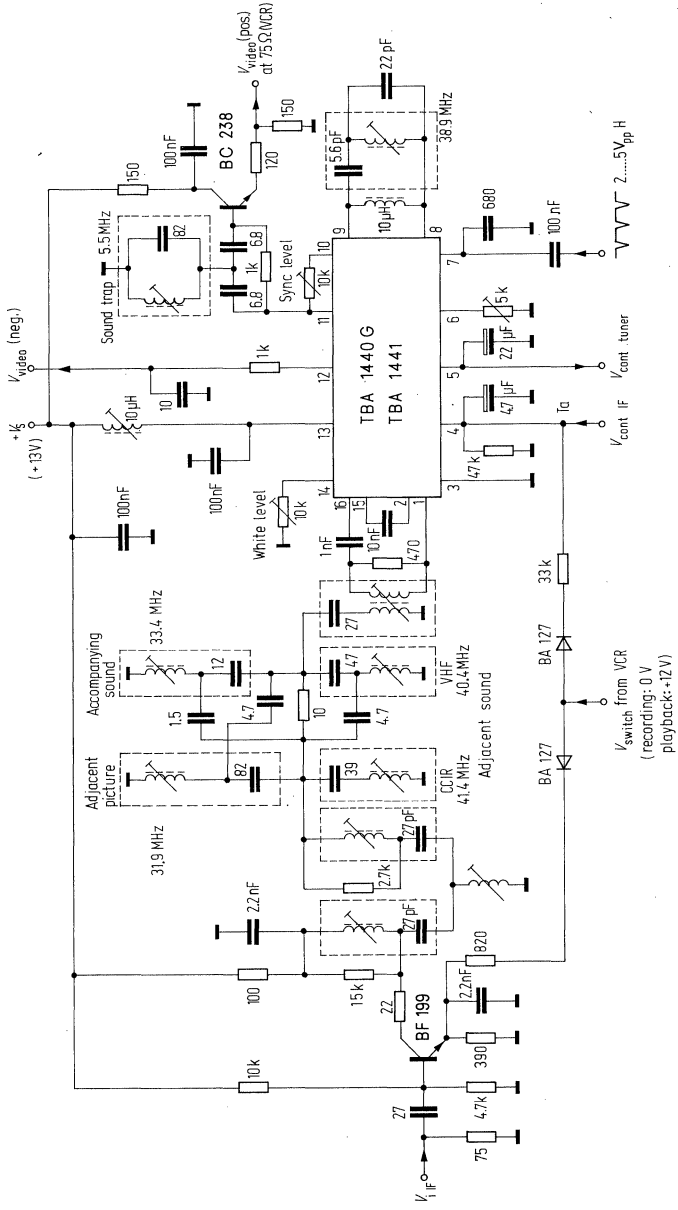


Tuner control current versus attenuation
R_6 = parameter



Application circuit

suitable for connection of video recorders (75 Ω)



Bipolar circuit

The TDA 5500 represents a variant of the TBA 1440 G. It contains — like the TBA 1440 G — a highly amplifying video IF amplifier, a controlled demodulator and two low-ohmic video outputs with positive- and negative-going signals as well as the complete, gated control, and delayed tuner control.
Connection of pin 10 is unlike the TBA 1440 G. Whereas pin 10 of the TBA 1440 G is provided for adjusting the sync pulse level, that of the TDA 5500 is used as standard VCR connection.
Switchover from VCR recording to playback is done via pin 4.

- Standard VCR connection
- Internal VCR switchover
- Gated control
- Positive and negative video output

Type	Ordering code	Package outline
TDA 5500	Q67000-A1377	DIP 16

Maximum ratings

Supply voltage	V_{13}	15[1])	V
Voltages	V_4	7	V
	V_5	15	V
Ohmic resistance between pin 8 and 9	$R_{8\text{-}9}$	≤ 20	Ω
Thermal resistance (system-air)	$R_{\text{th SA}}$	90	K/W
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C

Range of operation

Supply voltage range	V_{13}	10.5 to 15	V
Ambient temperature range	T_{amb}	−25 to 60	°C

[1]) intermittently 16.5 V

Characteristics (V_{13} = 13 V; T_{amb} = 25 °C; all data measured with respect to ground, unless otherwise stated)

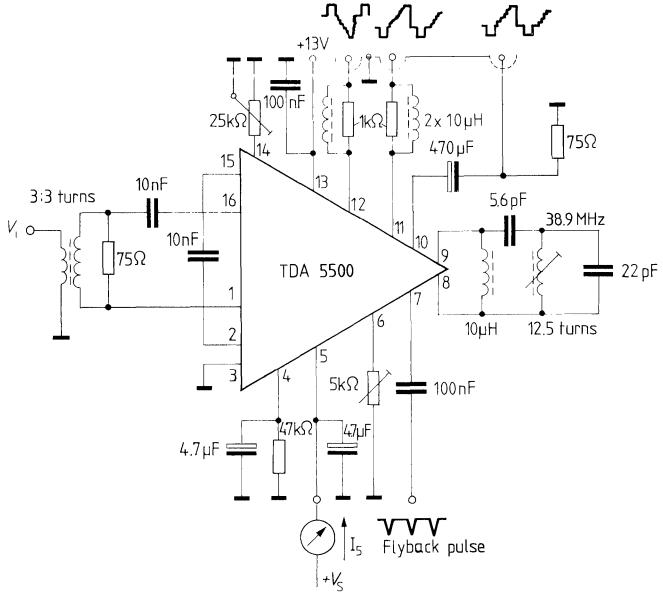
		min	typ	max	
Current consumption	I_{13}		55		mA
DC voltage at output 11 ($V_i = 0$)					
$R_{14\text{-}3} = \infty$	V_{11}		4.5		V
$R_{14\text{-}3} = 0$	V_{11}		7.5		V
DC voltage at output 12 ($V_i = 0$)					
$R_{14\text{-}3} = \infty$	V_{12}		1.5		V
$R_{14\text{-}3} = 0$	V_{12}		3		V
DC voltage at output 10 ($V_i = 0$)					
$R_{14\text{-}3} = \infty$	V_{10}		5.5		V
$R_{14\text{-}3} = 0$	V_{10}		8		V
Video amplification	$\frac{V_{11}}{V_{10}} = \frac{V_{12}}{V_{10}}$		3		
White level deviation	$\Delta V_{11}/V_{13}$		100		mV/V
	$\Delta V_{12}/V_{13}$		25		mV/V
AGC threshold = sync level	$V_{11\ sync}$		1.9		V
Sync pulse level with async or without gating pulses (peak level control)	$V_{11\ sync}$		1.5		V
Control current for tuner prestage ($V_5 \geqq 2$ V)	I_5	10	15		mA
Gating pulse voltage	$-V_7$	2		5	V
IF control voltage max. gain	V_4	0		0.5	V
min. gain	V_4	2		4	V
Voltage range VCR recording	V_4	0		4	V
VCR playback	V_4	4		6.5	V
Output current to ground	I_{11}; I_{12}			5	mA
to plus	I_{11}; I_{12}			−1	mA
Input impedance at max gain	$Z_{i\ 1\text{-}16}$		1.8/2		kΩ/pF
at min gain	$Z_{i\ 1\text{-}16}$		1.9/0		kΩ/pF
Output impedance	$Z_{q\ 8;9}$		2/2.5		kΩ/pF
Output resistance VCR recording	$R_{q\ 10}$		75		Ω
Input resistance VCR playback	$R_{i\ 10}$		75		Ω
Input voltage[1]) for $V_{11} = 3\ V_{pp}$ (at $G_{V\ max}$)	V_i		180	250	μV
AGC range	ΔG		55		dB
Intermodulation ratio (1.07 MHz) with reference to color carrier[2])	a		45		dB

[1]) According to test circuit: V_1 = rms sync pulse level at 60 Ω

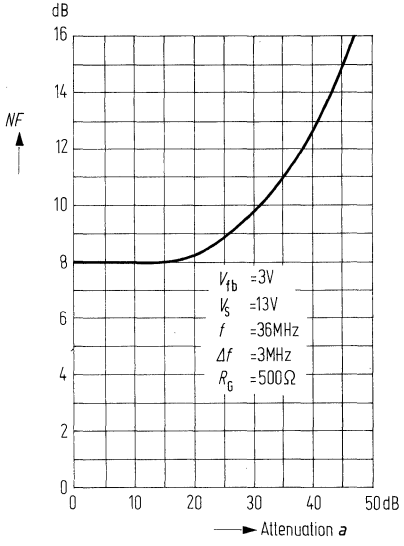
[2]) Test level a_{cc} = − 3 dB

a_{sc} = −20 dB referred to picture carrier

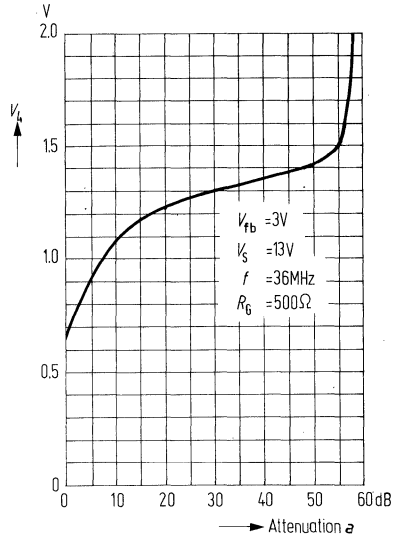
Test circuit



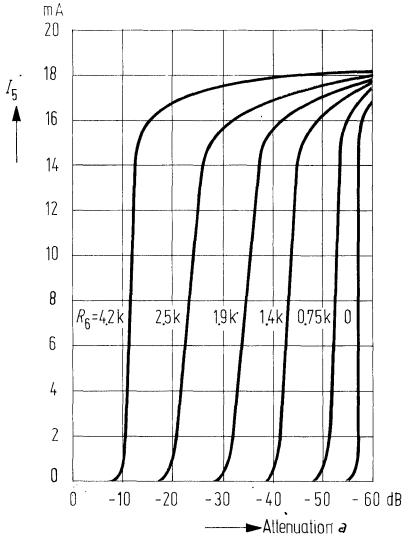
Noise figure versus attenuation
(measured at video frequency)
V_S = 13 V, f = 36 MHz, Δf = 3 MHz,
R_G = 500 Ω, $-V_{fb}$ = 3 V



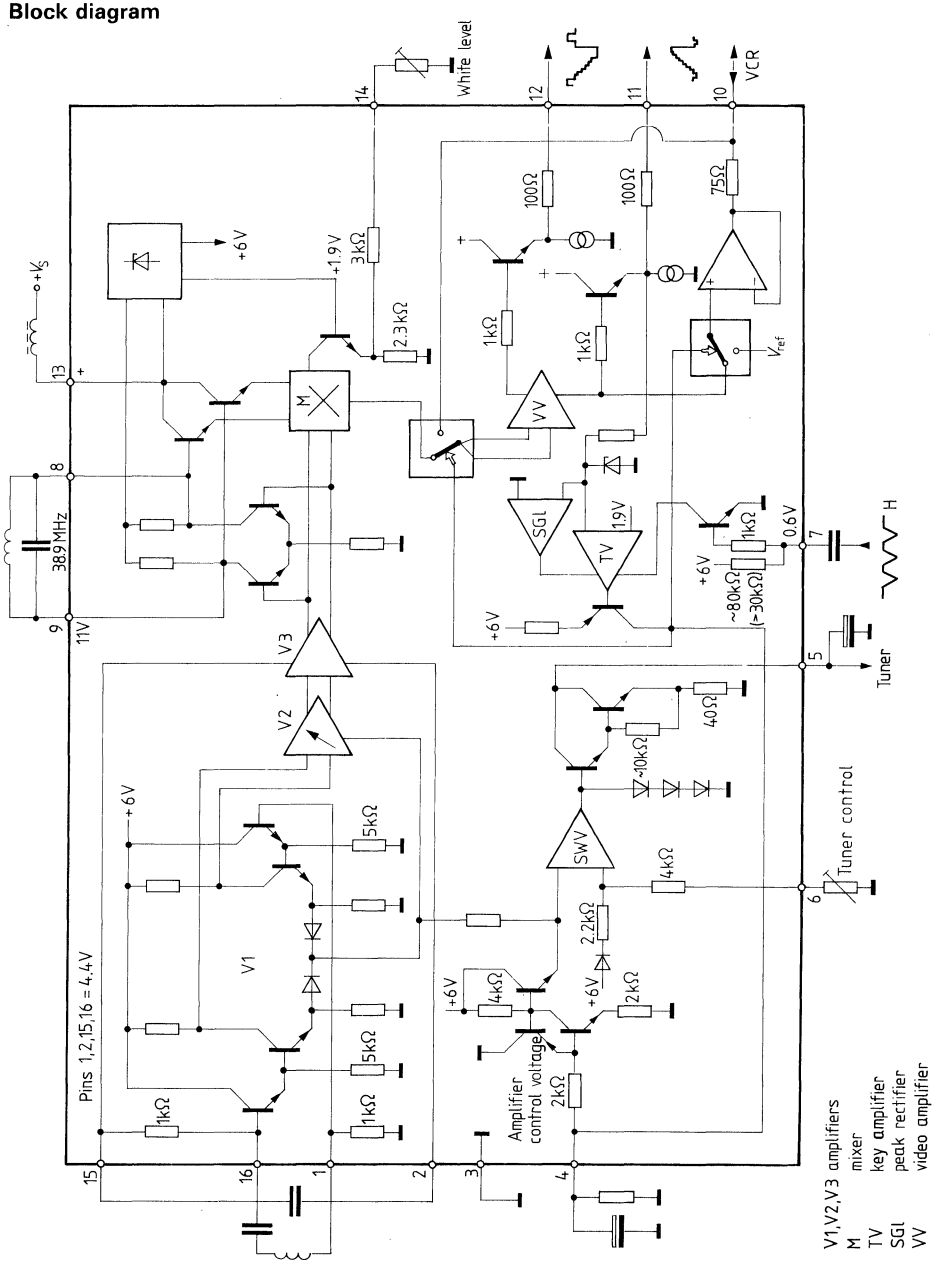
Control voltage versus attenuation
$-V_{fb}$ = 3 V, V_S = 13 V, f = 36 MHz,
R_G = 500 Ω



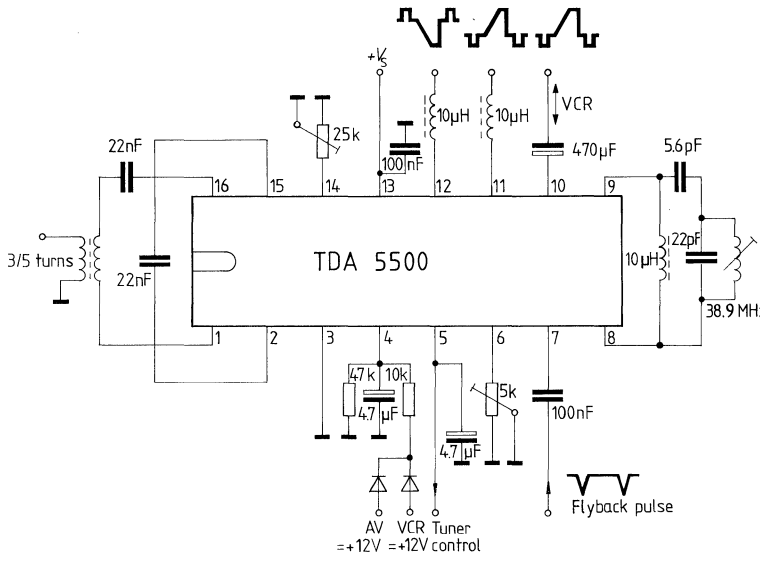
Tuner control current versus attenuation
R_6 = parameter



Block diagram



Application circuit



Video IF IC with AFC

TDA 5600
TDA 5610
TDA 5611

Bipolar circuit

Highly amplifying controlled video IF amplifier including demodulator, low-ohmic video outputs for positive- and negative-going signal, gated control, AFC output, and delayed tuner control.
Both types — TDA 5600 and TDA 5610 — only differ by the direction of their AFC voltage and are provided for pnp tuners. If npn tuners are used, the TDA 5611 is suitable.
TDA 5600: AFC zero crossing after positive direction
TDA 5610: AFC zero crossing after negative direction
TDA 5611: like TDA 5610; however, for npn tuners

- High integration
- Large control range
- High input sensitivity
- PC board layout TDA 5600/5610 or 5611, respectively, also intended for TBA 1440 G or 1441, respectively.

Type	Ordering code	Package outline
TDA 5600	Q67000-A1519	DIP 18
TDA 5610	Q67000-A1526	
TDA 5611	Q67000-A1625	

Maximum ratings

Supply voltage	V_S	15 [1]	V
Voltages	V_4	5	V
	V_5	20	V
	V_{16}	5	V
Ohmic resistance between			
pin 9 and 10	$R_{9\text{-}10}$	20	Ω
pin 8 and 11	$R_{8\text{-}11}$	20	Ω
Thermal resistance (system-air)	$R_{th\ SA}$	70	K/W
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C

Range of operation

Supply voltage range	V_S	10.5 to 15	V
Ambient temperature range	T_{amb}	−25 to 70	°C

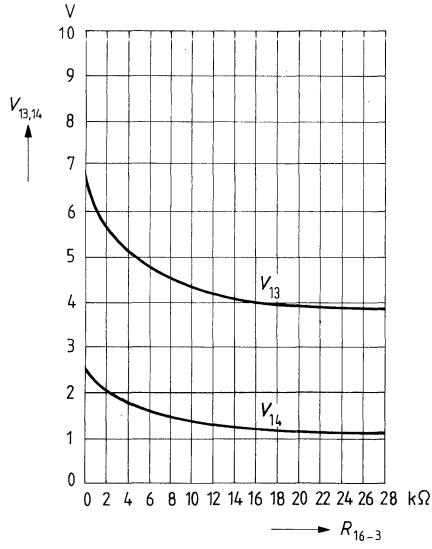
1) maximal 16.5 V for 1 minute

Characteristics (V_S = 13 V, $f_{i\,IF}$ = 38.9 MHz, T_{amb} = 25 °C)

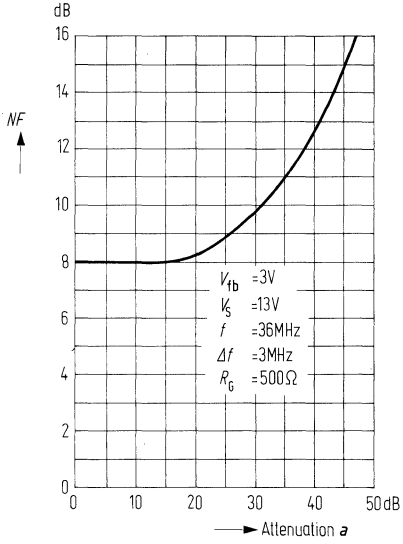
		min	typ	max	
Current consumption	I_{15}		60		mA
DC voltage at output 13 (V_{15} = 15 V, V_i = 0)					
$R_{16\text{-}3} = \infty$	V_{13}		3.5		V
$R_{16\text{-}3} = 0$	V_{13}		7		V
DC voltage at output 14 (V_{15} = 15 V, V_i = 0)					
$R_{16\text{-}3} = \infty$	V_{14}		1.1		V
$R_{16\text{-}3} = 0$	V_{14}		2.5		V
White level deviation	$\Delta V_{13}/\Delta V_{15}$		100		mV/V
	$\Delta V_{14}/\Delta V_{15}$		20		mV/V
Resistance for ΔV_{13} = 1 V	$R_{16\text{-}3}$		8.5		kΩ
Sync pulse level	V_{13}		1.9		V
Sync pulse level with async or without gating pulses (peak level control)	$V_{13\,sync.}$		0.5		V
Control current for tuner prestage ($V_5 > 2$ V)	I_5	10	15		mA
IF control voltage for max. gain	V_4	0		0.9	V
for min. gain	V_4	2.8		5	V
Gating pulse voltage	$-V_7$	2		7	V
Residual IF (basic frequency)	V_{13}, V_{14}		10		mV
Output current to ground	I_{13}, I_{14}			6	mA
to plus	I_{13}, I_{14}			−1	mA
Input impedance at max. gain	$Z_{1\text{-}18}$		1.8/2		kΩ/pF
at min. gain	$Z_{1\text{-}18}$		1.9/0		kΩ/pF
Input voltage for V_{13} = 3 V_{pp}[1])	$V_{i\,1\text{-}18}$		160	300	μV
Video bandwidth (−3 dB)	B_{video}	6	7		MHz
AGC range	ΔG		55		dB
Intermodulation ratio (1.07 MHz) with reference to color carrier[2])	a		45		dB
Output impedance	$Z_{q\,8\text{-}11}$		2/2.5		kΩ/pF
AFC input impedance	$Z_{i\,9\text{-}10}$		20		kΩ
AFC output current	$\pm I_{12}$		2.5		mA

[1]) According to test circuit: V_1 = rms sync pulse level at 60 Ω
[2]) Test level a_{cc} = − 3 dB, referred to picture carrier
a_{sc} = −20 dB, referred to picture carrier

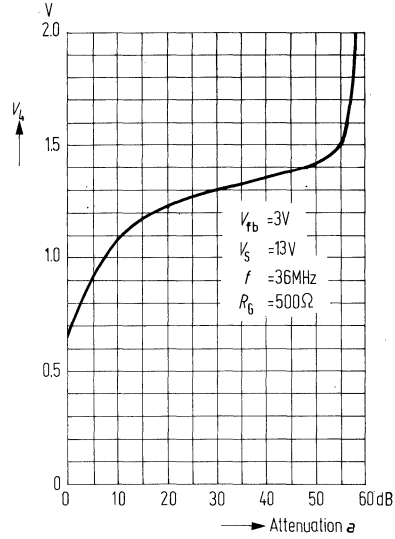
DC output voltage
versus white level resistance
V_S = 13 V; $R_{12\text{-}13}$ = ∞



Noise figure versus attenuation
(measured at video frequency)
V_S = 13 V, f = 36 MHz, Δf = 3 MHz,
R_G = 500 Ω, $-V_{fb}$ = 3 V

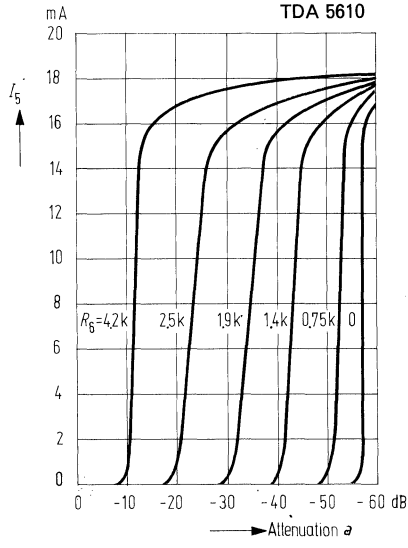


Control voltage versus attenuation
$-V_{fb}$ = 3 V, V_S = 13 V, f = 36 MHz,
R_G = 500 Ω



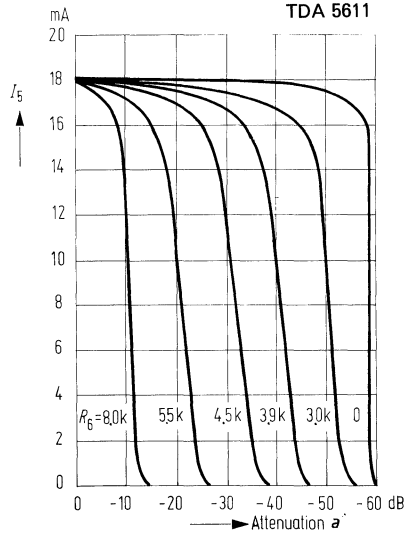
Tuner control current versus attenuation
R_6 = parameter

TDA 5600
TDA 5610

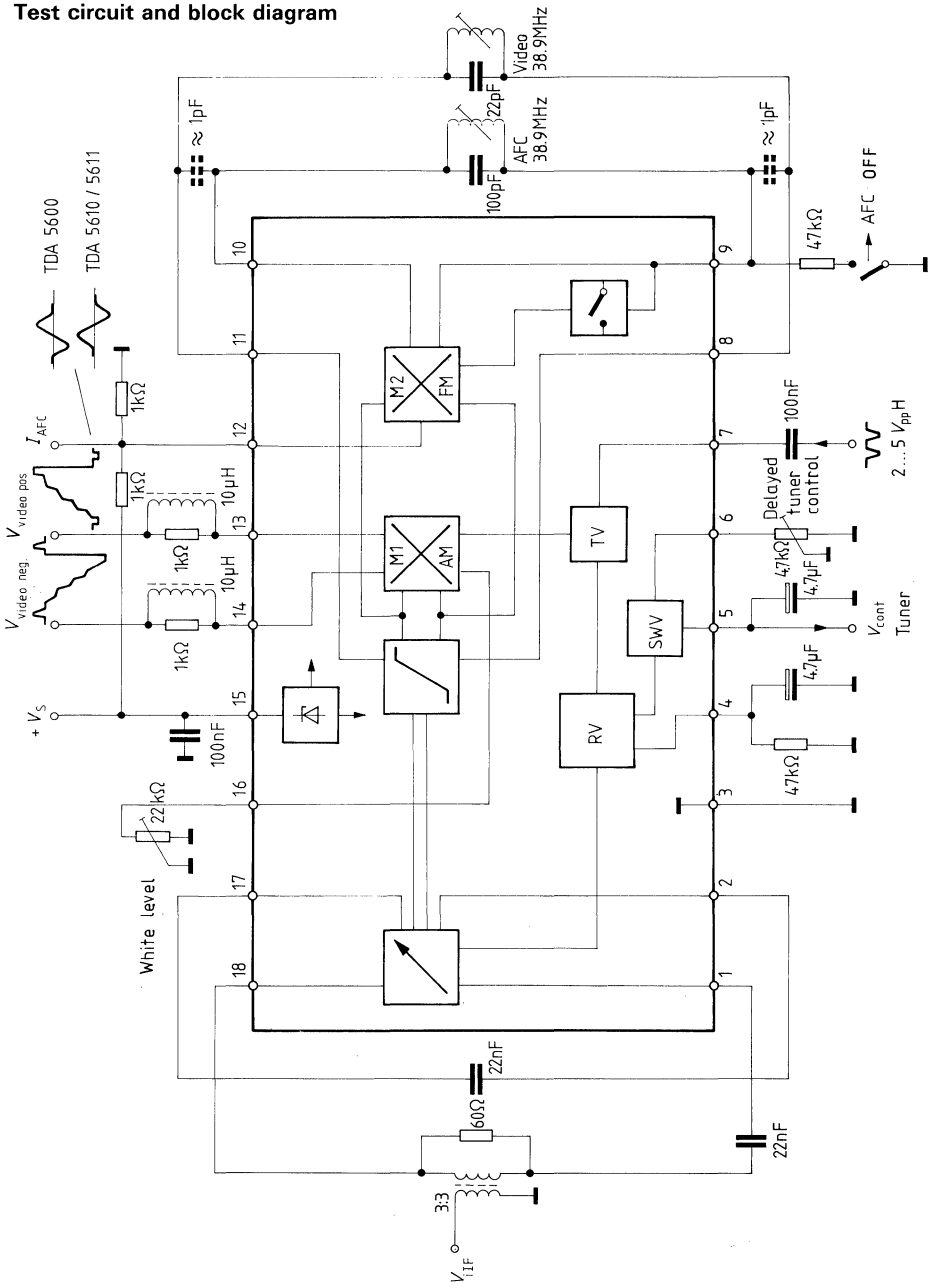


Tuner control current versus attenuation
R_6 = parameter

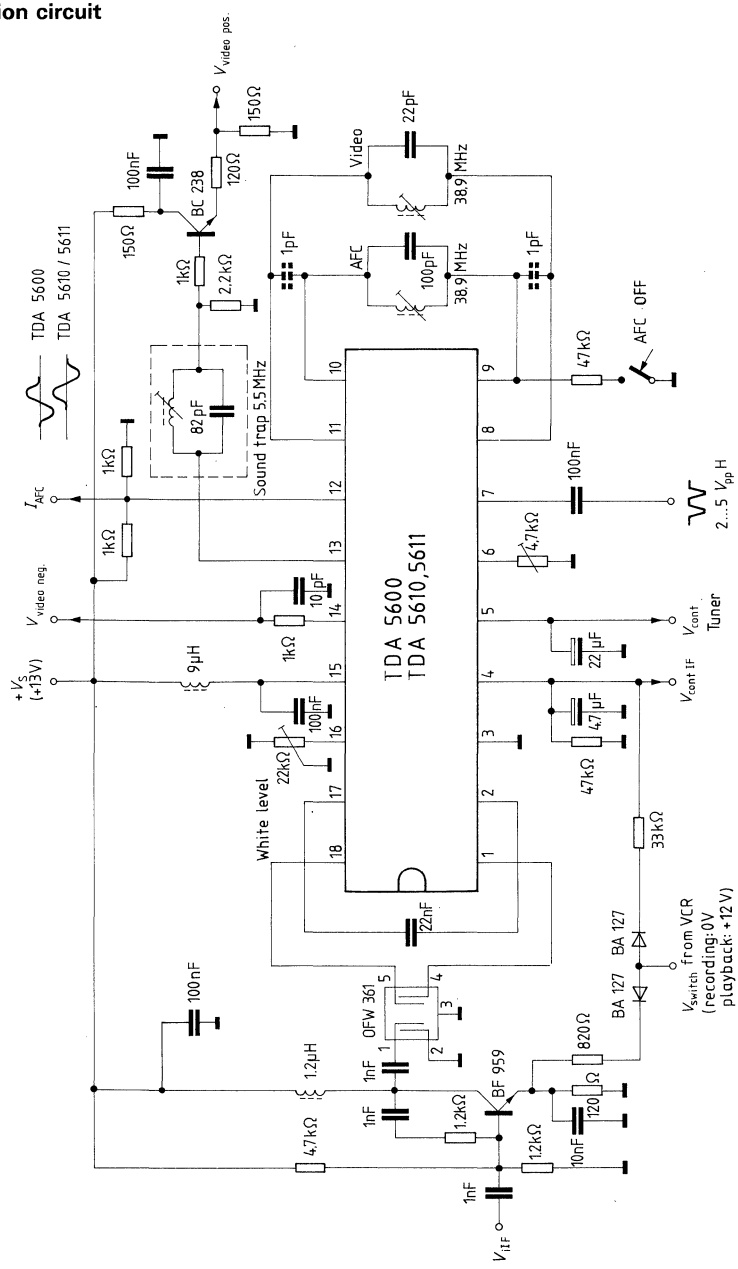
TDA 5611



Test circuit and block diagram



Application circuit



Bipolar circuit

Symmetrical, single-stage limiter amplifier with symmetrical coincidence demodulator and symmetrical AFC amplifier including a push-pull current output. Particularly suitable for automatic tuning in TV sets.

- Good limiting characteristics
- Excellent frequency stability of the converter characteristic
- Few external components
- Programmable current deviation

Type	Ordering code	Package outline
TDA 4260	Q67000-A1300	DIP 8

Maximum ratings

Supply voltage	V_S	15[1])	V
Thermal resistance (system-air)	$R_{th\ SA}$	100	K/W
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C

Range of operation

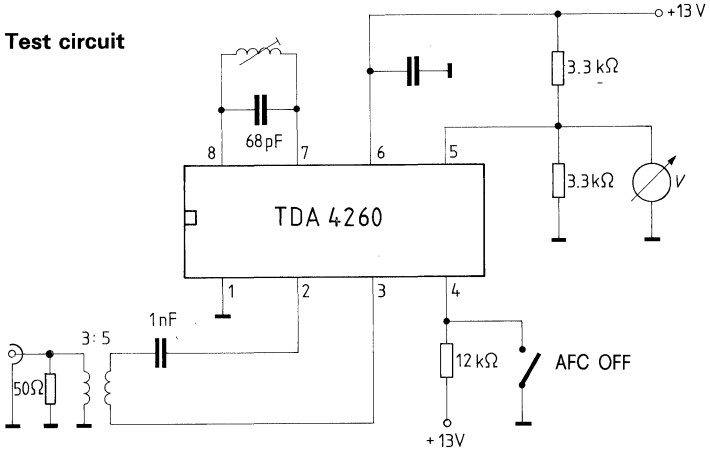
Supply voltage range	V_S	10.5 to 15	V
Ambient temperature range	T_{amb}	−25 to 60	°C

Characteristics (V_S = 13 V; T_{amb} = 25 °C)

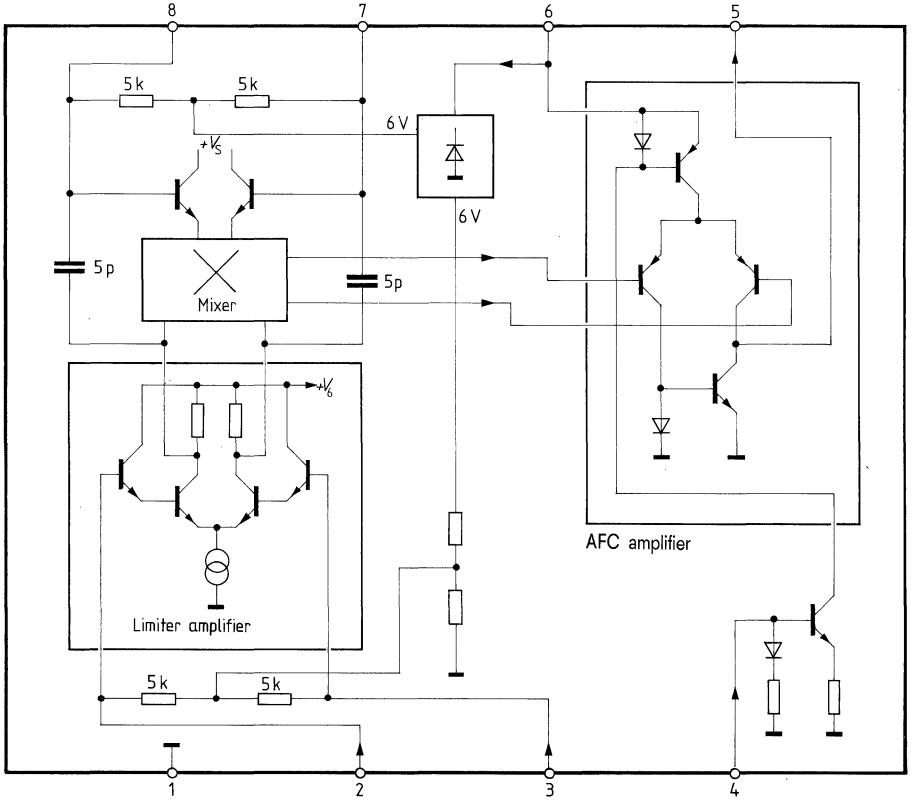
		min	typ	max	
Current consumption	I_6	13	18	23	mA
Limiting use	$V_{2/3\ lim}$		60	80	mV_{rms}
Input resistance	$R_{i\ 2/3}$		10		kΩ
Programming current	I_4			1	mA
Output current (at I_4 = 1 mA)	$I_{q\ 5}$	±600	±750	±900	µA
Output current: without signal	$I_{q\ 5}$		0	±10% · I_4	µA
Output current for AFC off (I_4 = 0)	$I_{q\ 5}$		0	±10	µA

1) intermittently 16.5 V

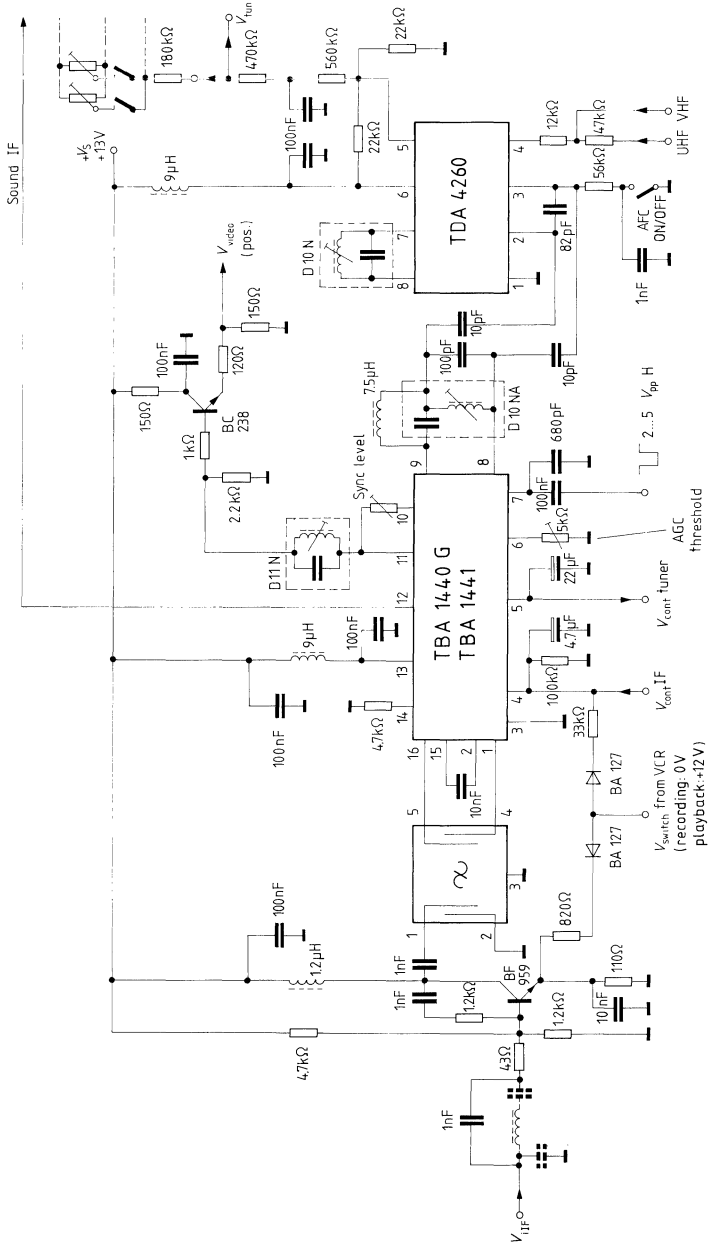
Test circuit



Block diagram



Application circuit



Bipolar circuit

With the TDA 2840 a new concept is offered to eliminate from the sound carrier interference that arises in the video IF amplifier and demodulator. For this purpose the video IF signal is tapped before the sound trap of the compact filter and fed to the TDA 2840. This IC includes the following stages: 3-stage, controlled IF amplifier with subsequent coincidence demodulator and peak value control. The sound carrier is obtained at the output of the demodulator via a low-pass configuration and an impedance converter.

- Good control characteristics
- Good AM rejection in the demodulator

Type	Ordering code	Package outline
TDA 2840	Q67000-A1268	DIP 14

Maximum ratings

Supply voltage	V_S	15[1])	V
Voltage	V_2	5	V
Thermal resistance (system-air)	$R_{th\ SA}$	90	K/W
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C

Range of operation

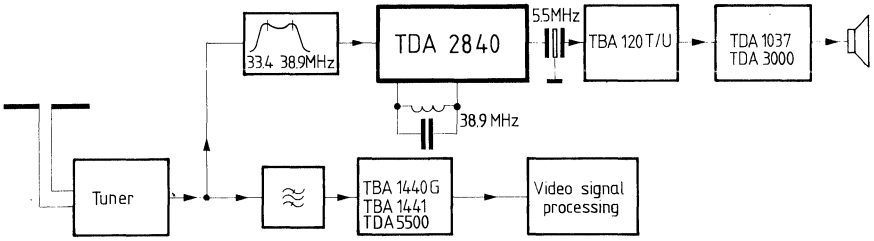
Supply voltage range	V_S	10.5 to 15	V
Ambient temperature range	T_{amb}	0 to 60	°C

Characteristics (V_S = 12 V; T_{amb} = 25 °C) according to application circuit

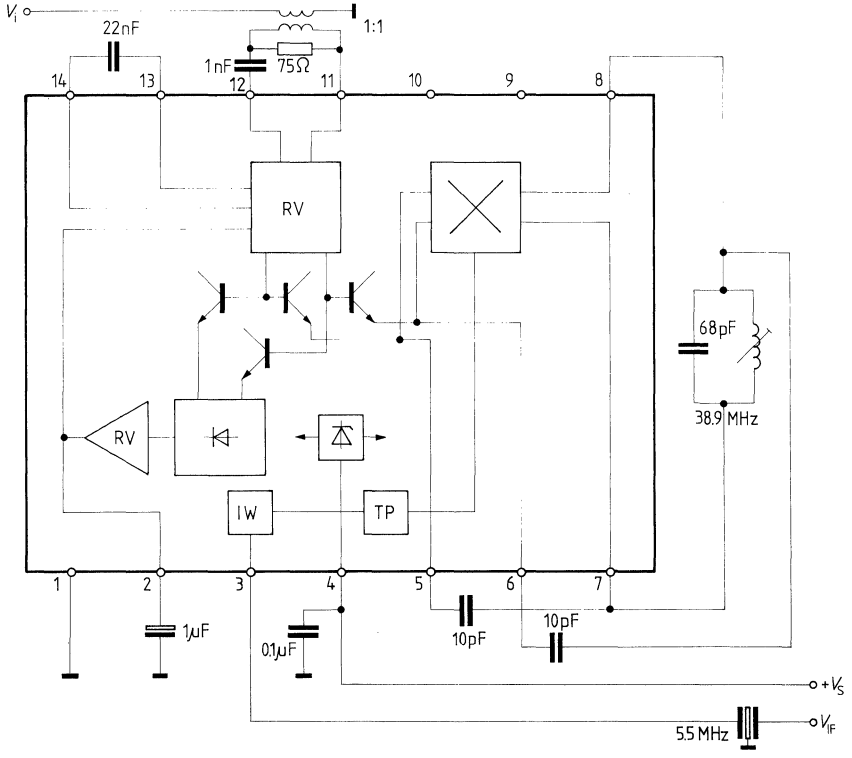
		min	typ	max	
Current consumption	I_S	25	36	47	mA
Input voltage for AGC threshold	$V_{i\ 11/12}$	100		300	µV
AGC range	ΔG	50			dB
Input impedance	$Z_{i\ 11/12}$	1.3/2	1.8/3	2.3/4	kΩ/pF
Sound carrier output voltage ($V_{i\ cc}$ = 1 mV; $V_{i\ sc}$ = 100 µV)	V_3	10			mV
Input impedance	$Z_{i\ 7/8}$	8.5		14	kΩ
Output impedance	Z_3	400	470	600	Ω

[1]) intermittently 16.5 V

Block diagram for application of the quasi-parallel sound IC



Test and application circuit



Bipolar circuit

Equivalent to the TDA 2840, the TDA 2841 taps the video IF signal before the sound trap of the compact filter. Interference in the sound carrier arising in the video IF amplifier and in the demodulator, are thus eliminated.
Compared to the TDA 2840, the TDA 2841 is additionally equipped with an AFC unit having two push-pull outputs. The control direction of both the outputs is inverse to each other.

- Good limiting qualities
- Good AM rejection in the demodulator
- Programmable current deviation

Type	Ordering code	Package outline
TDA 2841	Q 67000-A1473	DIP 16

Maximum ratings

Supply voltage	V_S	15	V
Voltage	V_2	5	V
Programming current	I_{10}	500	μA
Thermal resistance (system-air)	$R_{th\ SA}$	90	K/W
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C

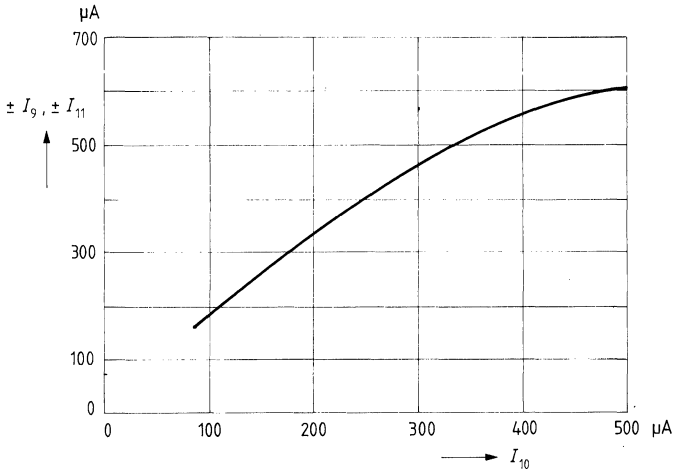
Range of operation

Supply voltage range	V_S	10.5 to 15	V
Ambient temperature range	T_{amb}	0 to 70	°C

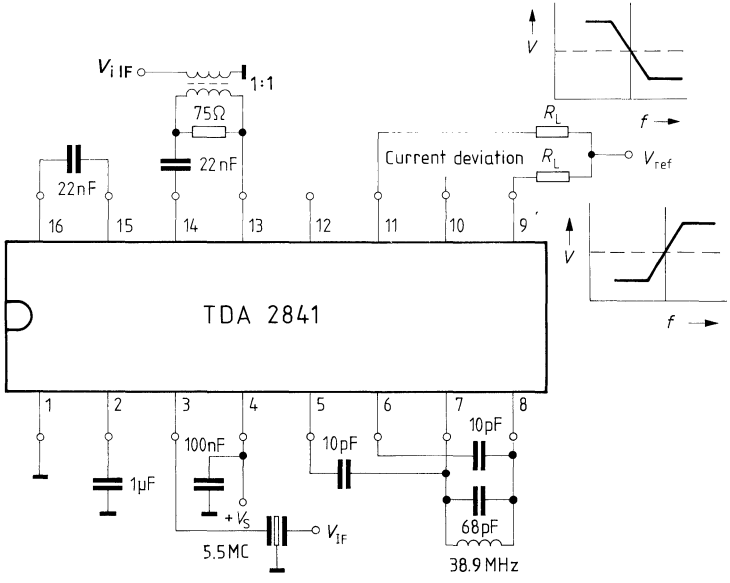
Characteristics (V_S = 12 V; T_{amb} = 25 °C)

		min	typ	max	
Current consumption	I_4	26	37	50	mA
Input voltage for AGC threshold	$V_{i\ 13/14}$	100		300	μV
AGC range	ΔG	50			dB
Input impedance	$Z_{i\ 13/14}$	1.3/2	1.8/3	2.3/4	kΩ/pF
Input impedance	$Z_{i\ 7/8}$	8.5		14	kΩ
Output impedance	$Z_{q\ 3}$	400	470	600	Ω
Sound carrier output voltage ($V_{i\ cc}$ = 1 mV; $V_{i\ sc}$ = 100 μV)	$V_{q\ 3}$	10			mV
Programming current	I_{10}	0		300	μA
Push-pull output currents (I_{10} = 300 μA)	$I_9 = -I_{11}$	±300		±600	μA

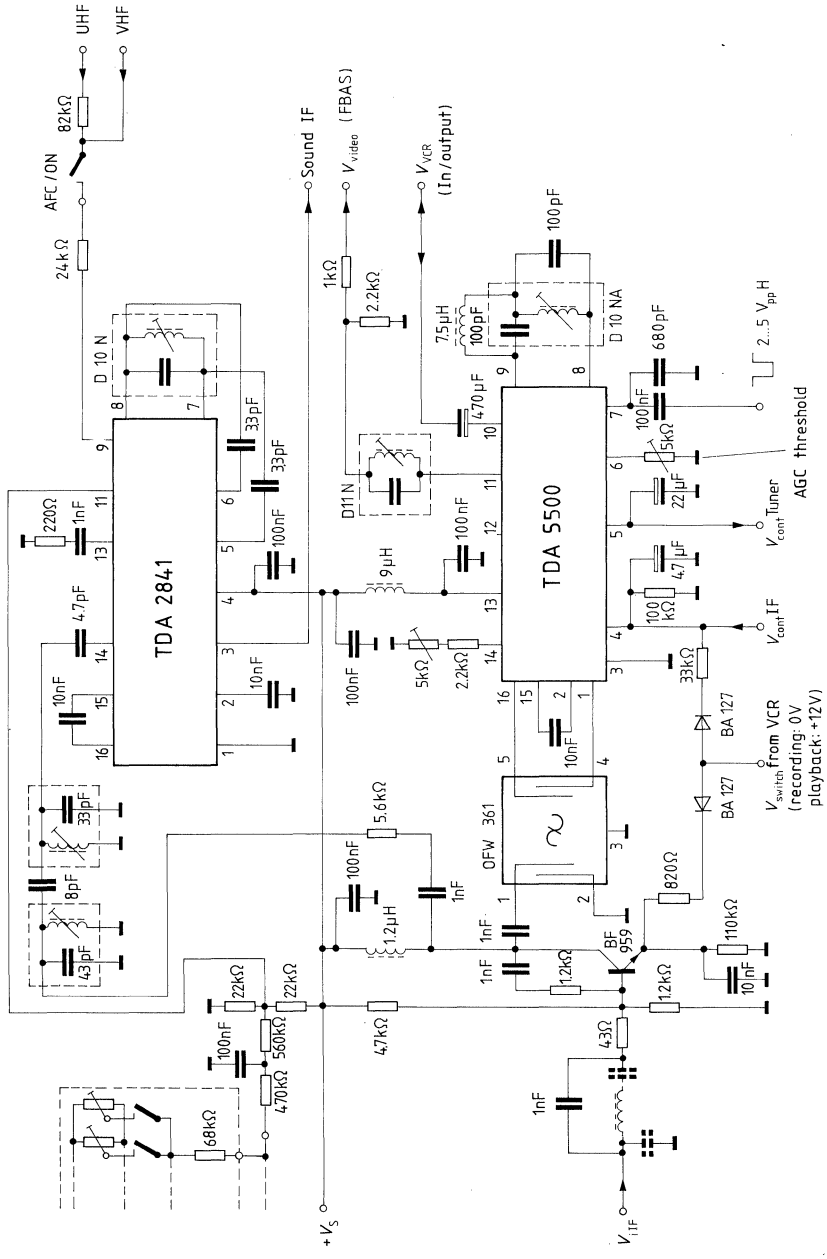
Push-pull output currents



Test circuit



Application circuit



Bipolar circuit

TDA 4280 T and TDA 4280 U include the combination of a quasi-parallel sound circuit with subsequent FM IF amplifier.
A controlled AM wideband amplifier with subsequent FM demodulator is used for gaining the intercarrier frequency. The AF signal is obtained after a sound IF limiter amplifier with coincidence demodulator. A standard VCR terminal is available.

TDA 4280 T: Demodulator matched to ceramic resonators

TDA 4280 U: Demodulator matched to LC networks

- Excellent limiting characteristics
- Terminal for video recorder
- Few external components

Type	Ordering code	Package outline
TDA 4280 T	Q 67000-A1439	DIP 18
TDA 4280 U	Q 67000-A1378	

Maximum ratings

Supply voltage	V_S	15	V
$t \leq 1$ min	V_S	16.5	V
Thermal resistance (system-air)	$R_{th\ SA}$	90	K/W
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C

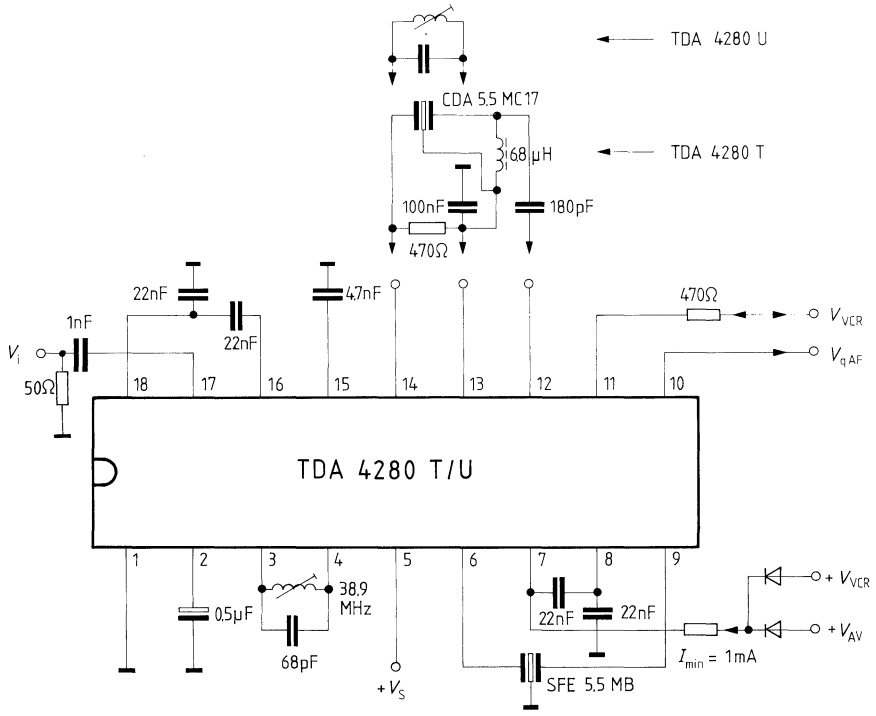
Range of operation

Supply voltage range		V_S	10.5 to 15	V
Frequency range	AM part	f_{AM}	10 to 60	MHz
	FM part	f_{FM}	0.01 to 12	MHz
Control voltage range	AM part	V_2	0 to 5	V
Switching current range	FM part	I_7	1 to 3	mA
Ambient temperature range		T_{amb}	0 to 60	°C

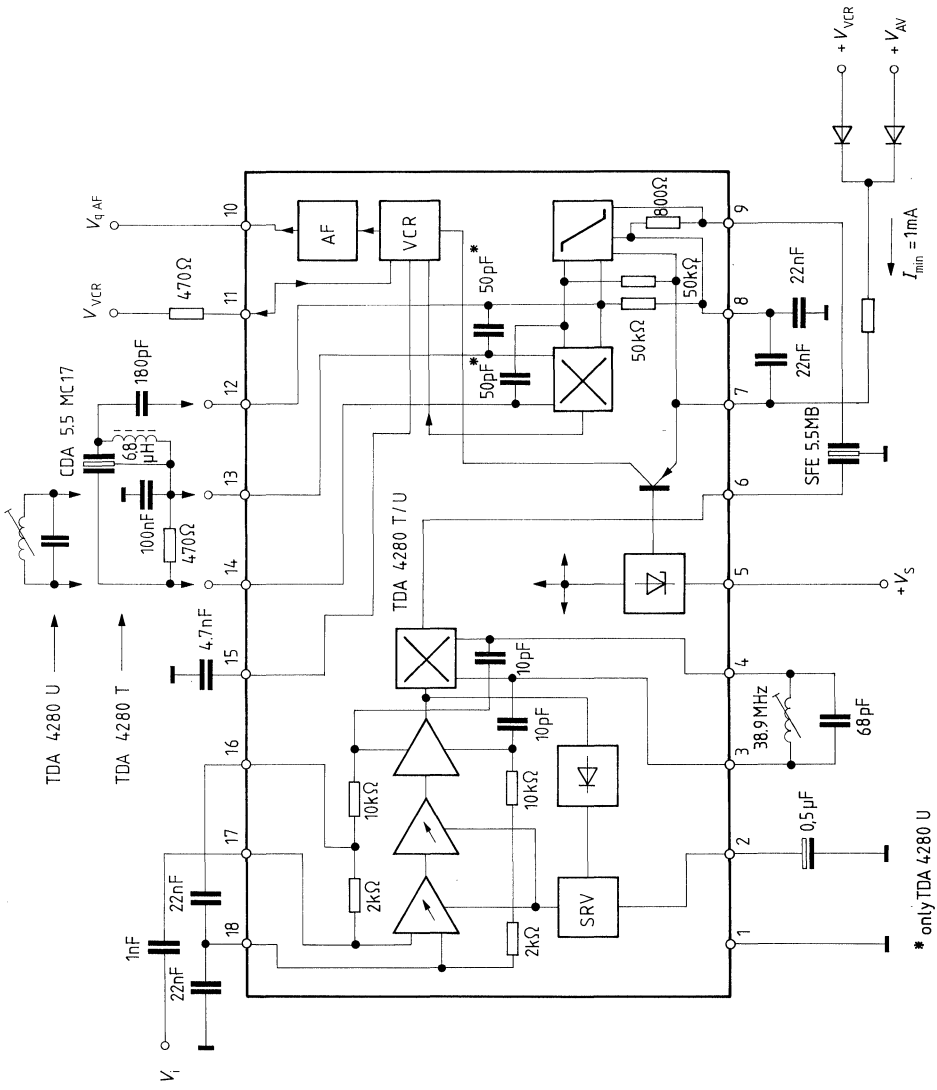
Characteristics (V_S = 12 V, T_{amb} = 25 °C)

		min	typ	max	
Current consumption	I_S		55	70	mA
AM part:					
AGC range	ΔG		55		dB
AGC voltage	V_2	0		5	V
Input resistance	$R_{i\,3\text{-}4}$		10		kΩ
Input impedance for max. gain	$Z_{i\,17}$		1.8/2		kΩ/pF
for min. gain	$Z_{i\,17}$		1.9/0		kΩ/pF
Output resistance	$R_{q\,6}$		500		Ω
FM part: ($f_{i\,8\text{-}9}$ = 5.5 MHz; f_{mod} = 1 kHz)					
Input impedance	$Z_{i\,8\text{-}9}$		800		Ω
AM suppression ($V_{i\,8\text{-}9}$ = 1 mV; Δf = ± 12.5 kHz; m = 30%)	a_{AM}		42		dB
Signal-to-noise ratio ($V_{i\,8\text{-}9}$ = 10 mV)	$a_{S/N}$		85		dB
Input voltage for limiting use (Δf = ± 30 kHz)	$V_{i\,lim.}$		60		µV
Output resistance for VCR recording	$R_{q\,11}$			500	Ω
Input resistance for VCR playback	$R_{i\,11}$	10			kΩ
De-emphasis resistance	R_{15}		11		kΩ
AF-output voltages	$V_{q\,11}$		600		mV_{rms}
	$V_{q\,10}$		300		mV_{rms}
AF amplification in case of VCR playback	$\frac{V_{10}}{V_{11}}$		0.5		
Total harmonic distortion (Δf = ± 30 kHz)	THD		1		%
Demodulator input resistance	$R_{i\,13\text{-}14}$		5.4		kΩ

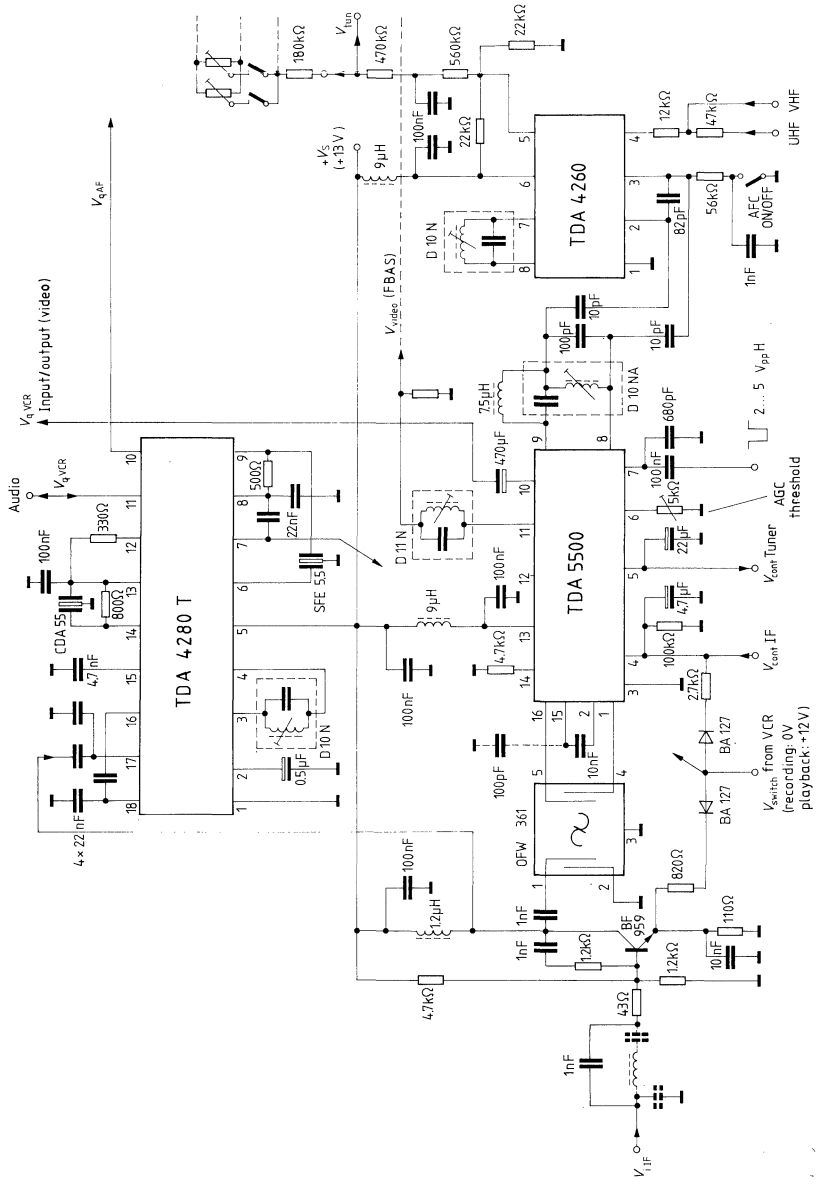
Test circuit



Block diagram



Application circuit



Quasi-Parallel Sound IC with FM IF with sym. Input

TDA 4281 T

Bipolar circuit

TDA 4281 T is a controlled AM wideband amplifier including FM demodulator (for obtaining the intercarrier frequency) and subsequent sound IF limiter amplifier with coincidence demodulator as well as standard VCR terminal and separated AF output.

- Excellent limiting characteristics
- Terminal for video recorders
- Few external components

Type	Ordering code	Package outline
TDA 4281 T	Q67000-A1589	DIP 22

Maximum ratings

Supply voltage	V_S	15	V
$t \leq 1$ min	V_S	16.5	V
Thermal resistance (system-air)	$R_{th\ SA}$	65	K/W
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C

Range of operation

Supply voltage range		V_S	11 to 15	V
Frequency range	AM part	f_{AM}	10 to 60	MHz
	FM part	f_{FM}	0.01 to 12	MHz
Control voltage range	AM part	V_2	0 to 5	V
Switching current range	FM part	I_8	0.3 to 1	mA
Ambient temperature range		T_{amb}	0 to 60	°C

Characteristics (V_S = 12 V, T_{amb} = 25 °C)

		min	typ	max	
Current consumption	I_S		60	80	mA
AM part:					
AGC range	ΔG		55		dB
AGC voltage	V_2	0		5	V
Input resistance	$R_{3\text{-}4}$		10		kΩ
Input impedance for max. gain	$Z_{20\text{-}21}$		1.8/2		kΩ/pF
for min. gain	$Z_{20\text{-}21}$		1.9/0		kΩ/pF
Output resistance	$R_{q\,6}$		500		Ω
	$R_{q\,7}$		500		Ω
FM part: (f_i = 5.5 MHz; f_{mod} = 1 kHz)					
Input impedance	$Z_{i\,9\text{-}10}$		800		Ω
AM suppression ($V_{i\,9\text{-}10}$ = 1 mV; Δf = 12.5 MHz; m = 30%)	a_{AM}		42		dB
Signal-to-noise ratio ($V_{i\,9\text{-}10}$ = 10 mV)	$a_{S/N}$		85		dB
Input voltage for limiting use (Δf = 30 kHz)	$V_{i\,lim}$		60		µV
Demodulator output resistance	$R_{q\,15\text{-}16}$		5.4		kΩ
Output resistance for VCR recording	$R_{q\,12}$			500	Ω
Input resistance for VCR playback	$R_{i\,12}$	10			kΩ
De-emphasis resistance	R_{17}		10		kΩ
AF output voltages	$V_{q\,12}$		600		mV_{rms}
(V_i = 10 mV; with CDA 5.5 MC 10) (Δf = 12.5 kHz)	$V_{q\,11}$	260	300		mV_{rms}
AF amplification in case of VCR playback	$V_{12\text{-}11}$		0.6		
Total harmonic distortion	THD_{12}		1		%
Cross talk (V_i = 1 mV)					
V_{12} = 2 V_{rms}	$c_{12\text{-}11}$	50	52		dB
V_{12} = 0.3 V_{rms}	$c_{12\text{-}11}$	60	65		dB

Circuit description

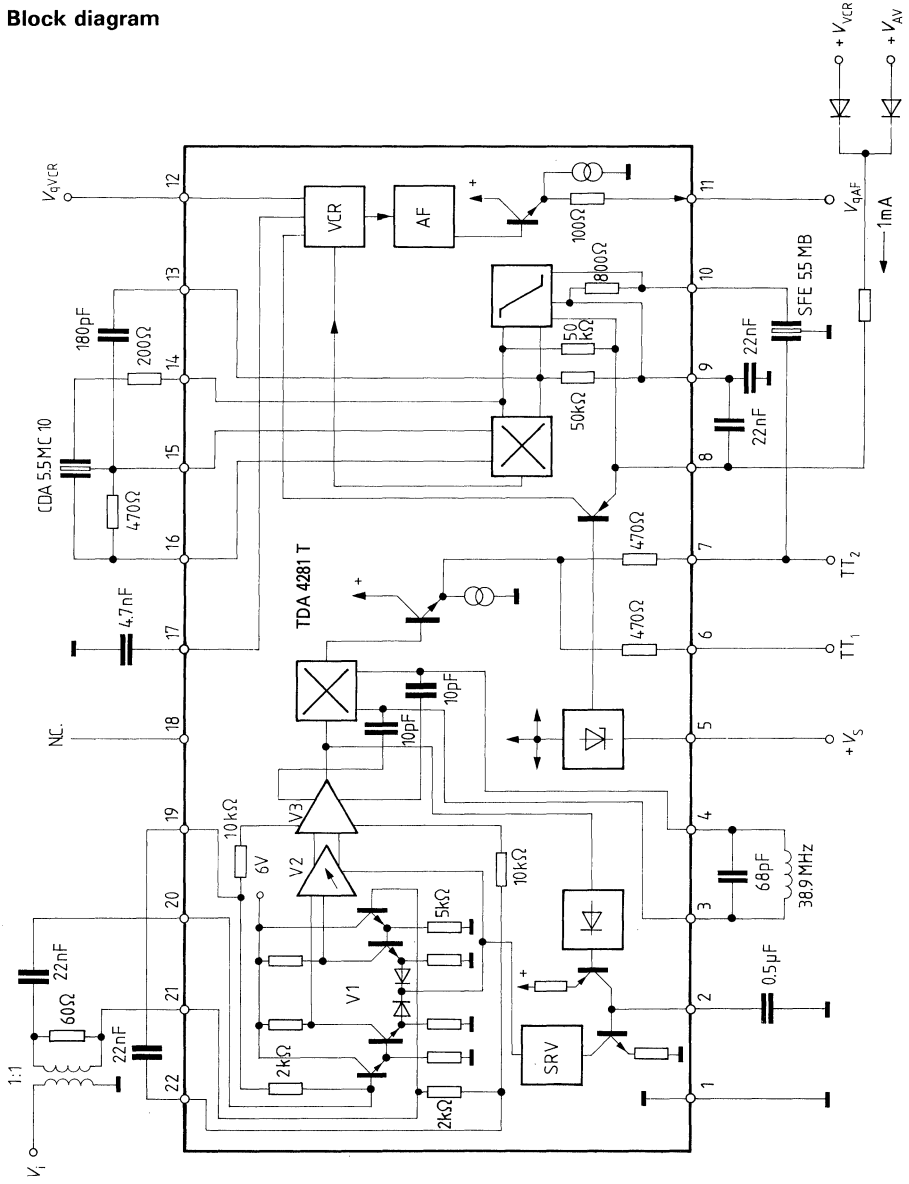
The TDA 4281 T mainly contains two functional blocks:

1. a controlled AM amplifier including point contact rectifier for control voltage generation. The AM amplifier drives an FM demodulator at the output of which the differential sound carrier (38.9 MHz — 33.4 MHz = 5.5 MHz) is available. The carrier-near double sideband parts are thereby suppressed. This 5.5 MHz carrier is externally filtered and has excellent side-band suppression.
2. an FM limiter amplifier with coincidence demodulator, a standard VCR terminal, and a separated AF output.

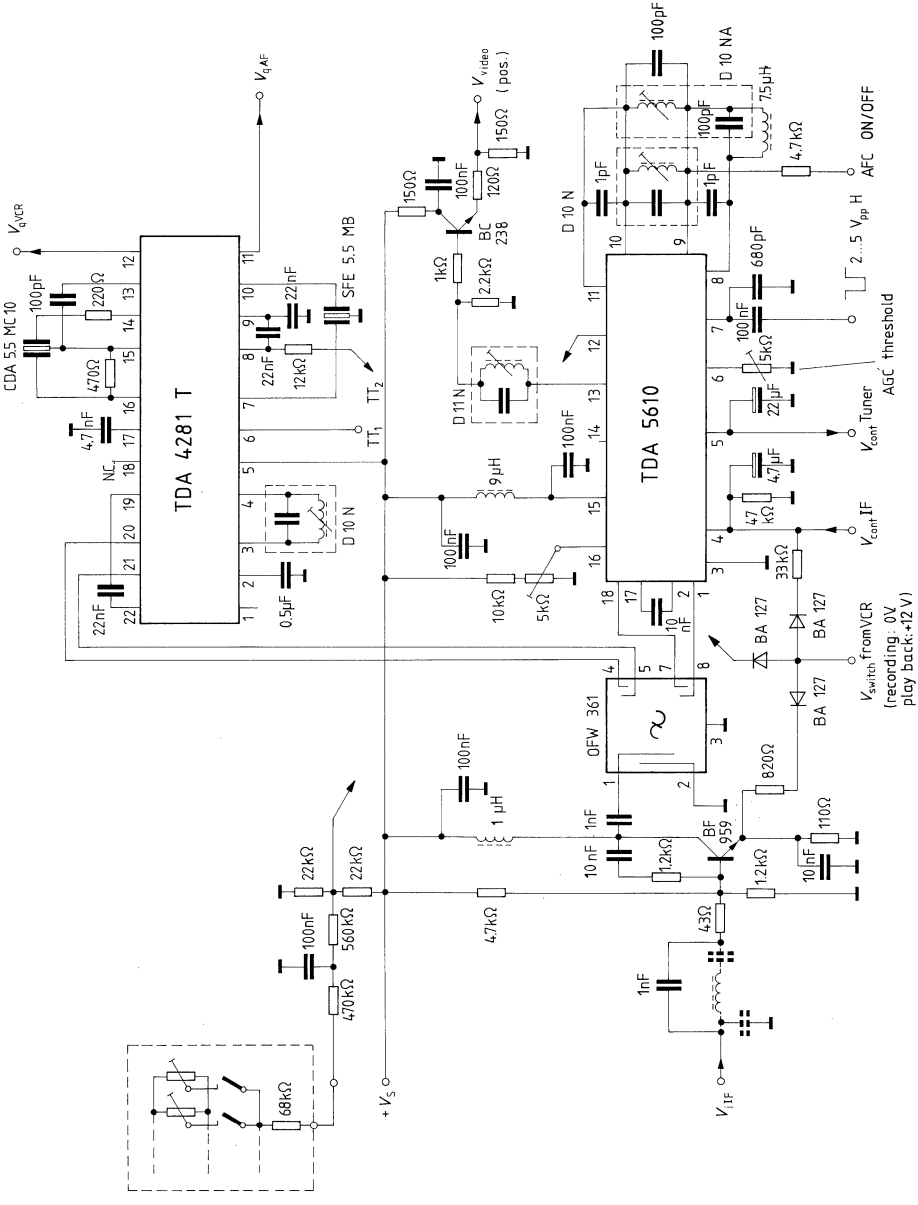
Pin designation

Pin No.	Description
1	Ground
2	AM IF control
3	AM amplifier demodulator
4	AM amplifier demodulator
5	Battery voltage (plus)
6	AM amplifier sound carrier output TT_1
7	AM amplifier sound carrier output TT_2
8	Negative feedback of FM IF amp. for working point
9	Negative feedback of FM IF amp. for working point
10	FM IF amplifier IF input
11	AF output
12	VCR terminal
13	Emitter follower output of the FM IF amplifier
14	Emitter follower output of the FM IF amplifier
15	FM amplifier demodulator
16	FM amplifier demodulator
17	Connection for de-emphasis capacitor
18	N.C.
19	Negative feedback of AM IF amp. for working point
20	AM IF amplifier IF input
21	AM IF amplifier IF input
22	Negative feedback of AM IF amp. for working point

Block diagram



Application circuit



FM IF Amplifier with Demodulator

TBA 120
TBA 120 A

Bipolar circuit

Symmetrical six-stage amplifier with symmetrical coincidence demodulator for the amplification, limiting and demodulation of frequency-modulated signals. Especially suited for radio receivers and sound-IF units in TV sets. These circuits are applicable as limiter amplifiers, as controlled demodulators or modulators or as mixers with excellent suppression of input frequencies.

- Good limiting characteristics
- Wide range of operation (5 to 15 V)
- Very few external components (i.e. for hum suppression)

Type	Ordering code	Package outline
TBA 120	Q67000-A151	DIP 14
TBA 120 A	Q67000-A175	DIP 14

Maximum ratings

Supply voltage	V_S	15	V
Thermal resistance (system-air)	$R_{th\ SA}$	90	K/W
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C

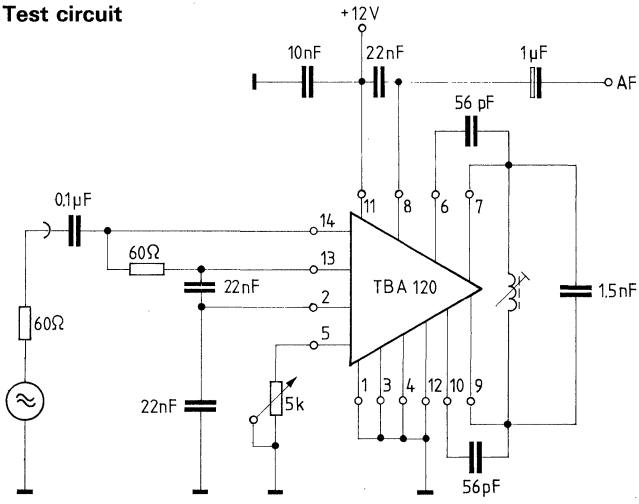
Range of operation

Supply voltage range	V_S	5 to 15	V
Ambient temperature range	T_{amb}	−15 to 70	°C
Frequency range	f	0 to 35	MHz

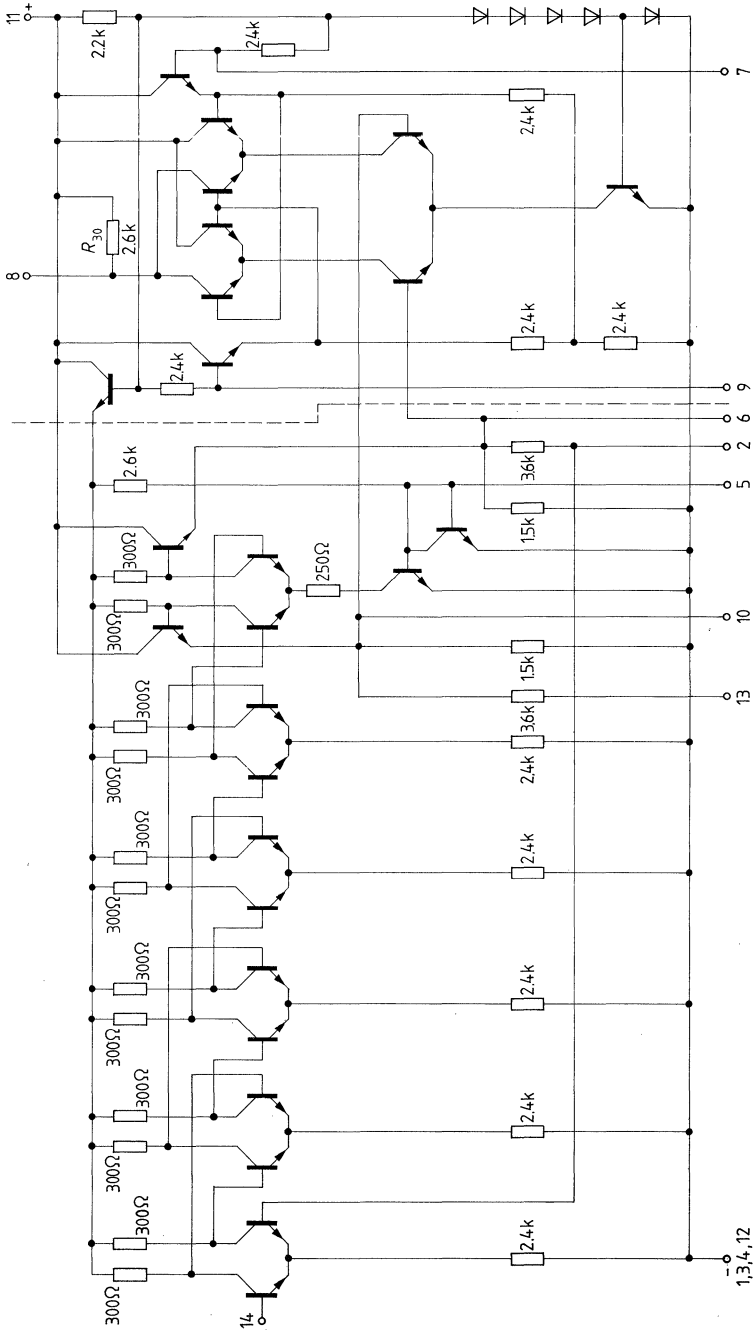
Characteristics (T_{amb} = 25 °C, V_S = 12 V, Q_B approx. 45, f_{mod} = 1 kHz)

		min	typ	max	
Current consumption	$-I_S$	12.5	16.5	20.5	mA
IF voltage gain (f_I = 5.5 MHz)	G_v		60		dB
IF output voltage at limiting each output	$V_{6\,pp}$; $V_{10\,pp}$		240		mV
AF output voltage (f_I = 5.5 MHz, Δf = ±25 kHz, V_i = 10 mV)	$V_{q8\,rms}$	0.6	0.85		V
AF output voltage (f_I = 5.5 MHz, Δf = ±50 kHz, V_i = 10 mV)	$V_{q\,8\,rms}$	1.2	1.7		V
Total harmonic distortion (f_I = 5.5 MHz, Δf = ±25 kHz, V_i = 10 mV)	THD		1.8	3	%
Input voltage for limiting (f_I = 5.5 MHz, Δf = ±50 kHz)	$V_{i\,lim}$		50	100	µV
Input impedance f_I = 5.5 MHz	$Z_{i\,5.5}$		15/7.8		kΩ/pF
f_I = 10.7 MHz	$Z_{i\,10.7}$		7.2/6.2		kΩ/pF
Output resistance	$R_{q\,7\text{-}9}$		4.8		kΩ
Output resistance	$R_{q\,8}$	1.9	2.6	3.3	kΩ
Range of volume control	$\frac{V_{AF\,max}}{V_{AF\,min}}$		60		dB
DC level of output signal (V_i = 0)	V_8	6.1	7.3	8.6	V
AM suppression (f_I = 5.5 MHz, V_i = 10 mV, m = 30%, Δf = ±50 kHz)	a_{AM}		55		dB

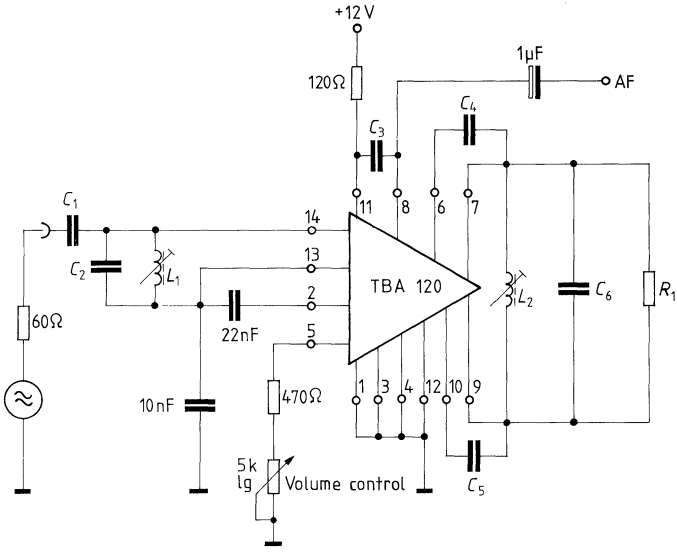
Test circuit



Circuit diagram



Application circuit



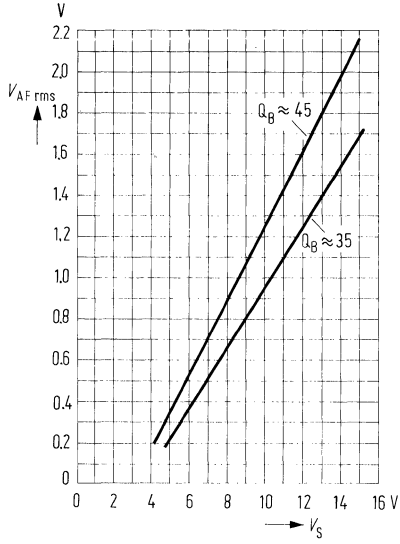
Component data for various applications

	Sound IF in TV sets	FM IF in radio sets	
	5.5 MHz	10.7 MHz Mono	10.7 MHz Stereo
C_1	47 pF	27 pF	47 pF
C_2	220 pF	120 pF	150 pF
C_3	22 nF	22 nF	470 pF
C_4	56 pF	27 pF	30 pF
C_5	56 pF	27 pF	30 pF
C_6	1.5 nF	470 pF	330 pF
L_1	20 turns	20 turns	15 turns
L_2	8 turns	8 turns	12 turns
R_1	∞	∞	1 kΩ

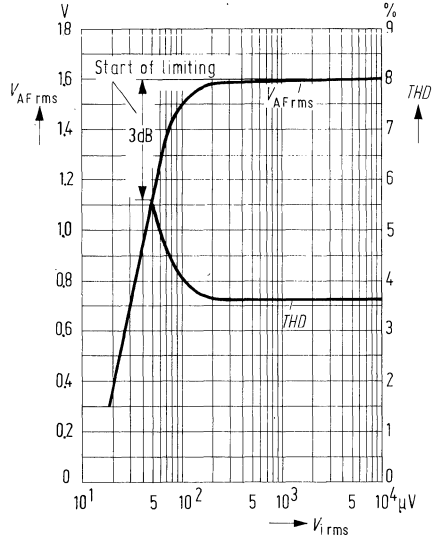
A capacitive decoupling of supply voltage input 11 is not necessary. The 22 nF capacitor between pins 8 and 11, together with the integrated resistor R_{30}, constitutes the de-emphasis and may be reduced if required.

The distance of the peaks on the S-curve can be adjusted with the Q_B of the phase-shifting circuit. Zero crossing corresponds to resonant frequency. The two coupling capacitors of equal size connected between pins 6/7 or 9/10, respectively should be dimensioned to produce approx. 250 mV_{pp} at the tank circuit at resonance.

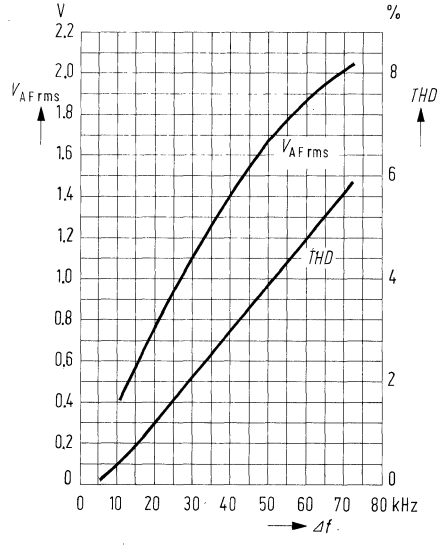
AF output voltage versus supply voltage
f_I = 5.5 MHz, Δf = ±50 kHz, f_{mod} = 1 kHz,
$V_{i\,rms}$ = 10 mV



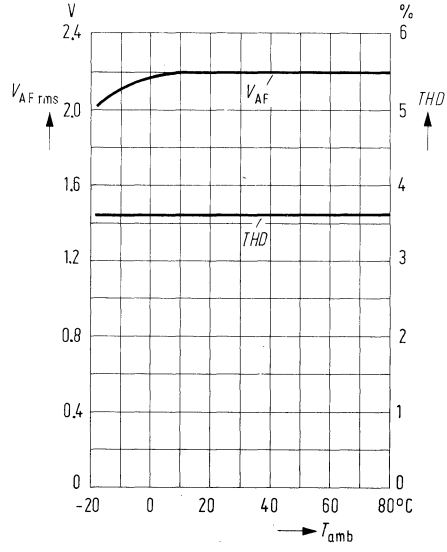
AF output voltage and total harmonic distortion versus input voltage
V_S = 12 V, f_I = 5.5 MHz, Δf = ±50 kHz,
f_{mod} = 1 kHz, Q_B approx. 45



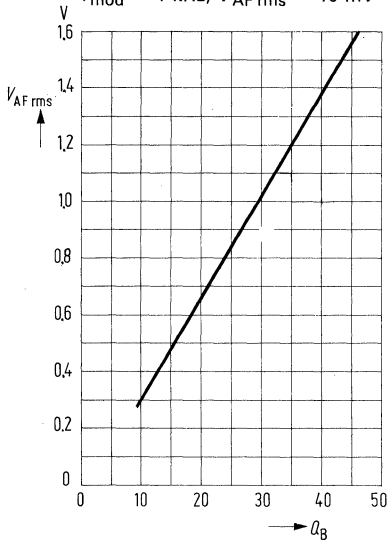
AF output voltage and total harmonic distortion versus frequency deviation
V_S = 12 V, f_I = 5.5 MHz, f_{mod} = 1 MHz,
$V_{i\,rms}$ = 10 mV, Q_B approx. 45



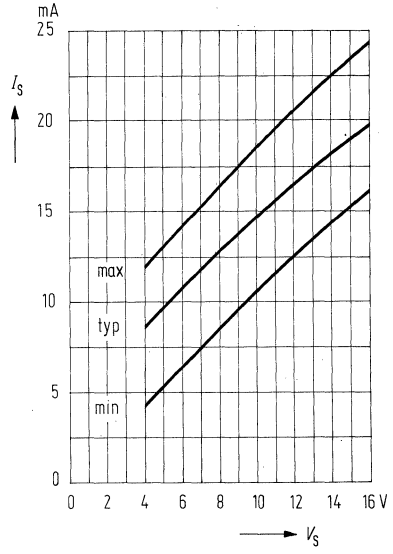
AF output voltage and total harmonic distortion versus ambient temperature
V_S = 15 V, f_I = 5.5 MHz, Δf = ±50 kHz,
f_{mod} = 1 kHz, $V_{i\,rms}$ = 10 mV, Q_B approx. 45



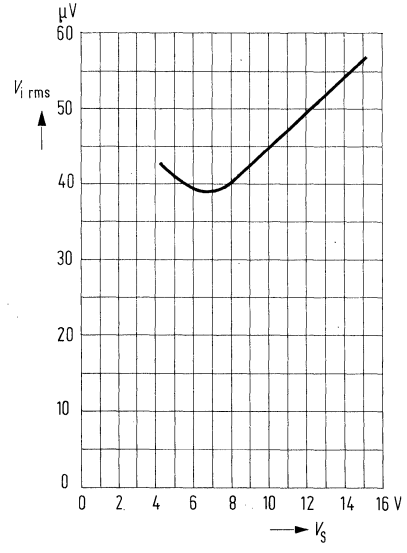
AF output voltage versus Q_B factor
V_S = 12 V, f_I = 5.5 MHz, Δf = ±50 kHz,
f_{mod} = 1 kHz, $V_{AF\,rms}$ = 10 mV



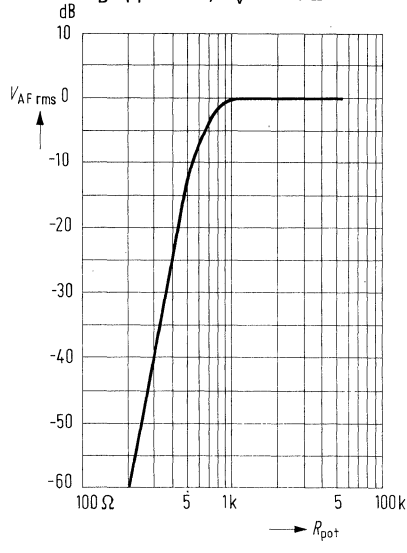
Current consumption versus supply voltage



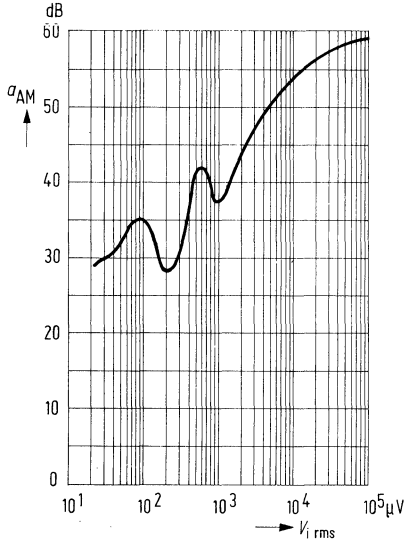
Input voltage for limiting versus supply voltage
f_I = 5.5 MHz, Δf = ±50 kHz,
f_{mod} = 1 kHz, Q_B approx. 45



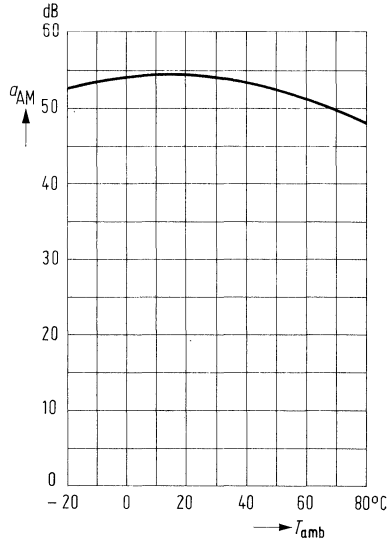
Volume control versus potentiometer resistance
V_S = 12 V, f_I = 5.5 MHz, Δf = ±50 kHz,
f_{mod} = 1 kHz, $V_{i\,rms}$ = 10 mV,
Q_B approx. 45, R_V = 470 Ω



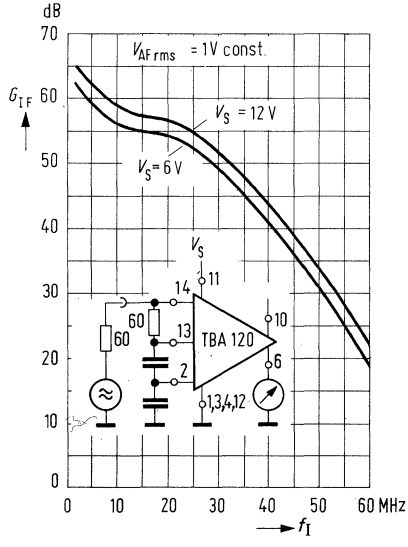
AM suppression
versus input voltage
V_S = 12 V, f_I = 5.5 MHz, Δf = ±50 kHz,
f_{mod} = 1 kHz, m = 30%, Q_B approx. 45



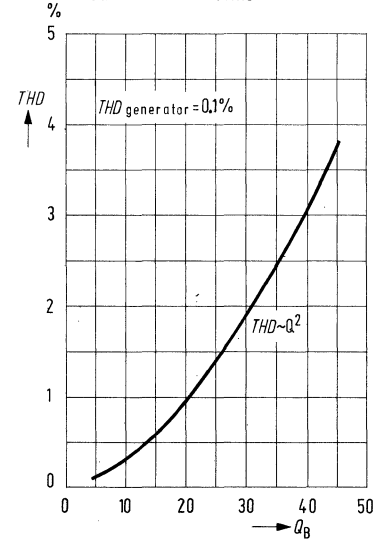
AM suppression
versus temperature of case
V_S = 12 V, f_I = 5.5 MHz, f_{mod} = 1 kHz,
m = 30%, $V_{i\ rms}$ = 10 mV, Q_B approx. 45



IF amplification versus IF frequency



Total harmonic distortion
versus Q_B factor
V_S = 12 V, f_I = 5.5 MHz, Δf = ±50 kHz,
f_{mod} = 1 kHz, $V_{i\ rms}$ = 10 mV



FM IF Amplifier with Demodulator

TBA 120 S
TBA 120 AS

Bipolar circuit

Symmetrical 8-stage amplifier with symmetrical coincidence demodulator for amplification, limiting and demodulation of frequency-modulated signals, especially suited for the sound IF parts in TV sets and FM IF amplifiers in radio sets. The circuit is directly interchangeable with TBA 120 (pin-compatible).

- Outstanding limiting characteristics
- Wide range of operation (6 to 18 V)
- Few external components
- Voltage for AFC

Type	Ordering code	Package outline
TBA 120 S	Q67000-A490	DIP 14
TBA 120 AS	Q67000-A525	QIP 14

Maximum ratings

Supply voltage [1])	V_S	18	V
Z current	I_{12}	15	mA
$t \leqq 1$ min	I_{12}	20	mA
Voltage	V	4	V
Current	I_3	5	mA
	I_4	2	mA
Thermal resistance (system-air)	$R_{th\ SA}$	90	K/W
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C

Range of operation

Supply voltage range	V_S	6 to 18	V
Ambient temperature range	T_{amb}	−15 to 70	°C
Frequency range	f	0 to 12	MHz

1) The IC must not be plugged in or out when supply voltage is switched on.

Characteristics (T_{amb} = 25 °C, V_S = 12 V; f_I = 5.5 MHz or 10.7 MHz, respectively)

		min	typ	max	
Current consumption	$R_5 = \infty$	I_S	10	14	18	mA
	$R_5 = 0$	I_S	11	15.2	20	mA
IF voltage gain		G_v		68		dB
IF output voltage at limiting (each output)		V_{qpp}	170	250		mV
Output resistance (pin 8)		$R_{q\,8}$	1.9	2.6	3.3	kΩ
Shunt resistance		$R_{13\text{-}14}$			1	kΩ
AGC range of volume control		$\frac{V_{AF\,max}}{V_{AF\,min}}$	70	75		dB
DC level of output signal		V_8	6.2	7.4	8.5	V
Potentiometer resistance						
	− 1 dB down	R_5		3.7	4.7	kΩ
	−70 dB down	R_5	1	1.4		kΩ
Voltage						
	− 1 dB down	V_5		2.4		V
	−70 dB down	V_5		1.3		V
Signal-to-noise ratio (V_i = 10 mV, Δf = ±50 kHz)		$a_{S/N}$	75	85		dB
Total harmonic distortion (V_i = 10 mV, Δf = ±25 kHz)		THD		1.3	2.5	%
Noise voltage (according to DIN 45405)		V_n		80	140	μV_s
Output resistance		$R_{q\,7\text{-}9}$		5.4		kΩ

Characteristics for f_I = 5.5 MHz (T_{amb} = 25 °C, V_S = 12 V, f_I = 5.5 MHz, Δf = ±50 kHz, f_{mod} = 1 kHz, Q_B approx. 45)

AF output voltage (V_i = 10 mV)	$V_{AF\,rms}$	0.7	1		V
Input voltage for limiting	$V_{i\,lim}$		30	60	µV
AM suppression V_i = 500 µV, m = 30%	a_{AM}	45	55		dB
V_i = 10 mV, m = 30%	a_{AM}	60	68		dB
Input impedance	Z_i		40/4.5		kΩ/pF

Characteristics for 10.7 MHz (T_{amb} = 25 °C, V_S = 12 V, f = 10.7 MHz, Δf = ±75 kHz, f_{mod} = 1 kHz, Q_B approx. 45)

AF output voltage (V_i = 10 mV)	$V_{AF\,rms}$	0.4	0.7		V
Input voltage for limiting	$V_{i\,lim}$		50	100	µV
AM suppression V_i = 500 µV, m = 30%	a_{AM}	40	50		dB
V_i = 10 mV, m = 30%	a_{AM}	60	68		dB
Input impedance	Z_i		20/4		kΩ/pF

Characteristics of the additive circuit

		min	typ	max	
Z voltage (I_{12} = 5 mA)	V_{12}	11.2	12	13.2	V
Z resistance	R_Z		30	55	Ω
Breakdown voltage	V_{CBO}	26	40		V
Breakdown voltage (I_3 = 500 µA)	V_{CEO}	13			V
Current gain (V_{CE} = 5 V, I_C = 1 mA)	G_I	25	80		

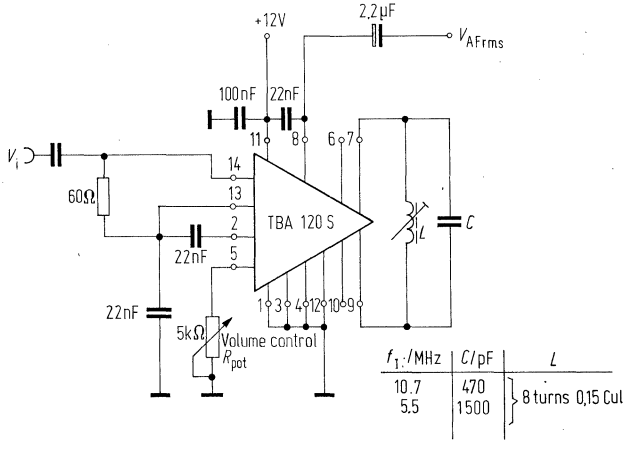
Pins 3 and 4 are connected to collector or base of a transistor, respectively, which may be used as an AF preamplifier ($I_C < 5$ mA) or as a bass/treble switch (dc on- or off-switching of an *RC* circuit).

At pin 12, a Z diode (12 V) is accessible which can be used to stabilize the supply voltage of this IC or the voltage of other circuit elements in the set ($I_Z \leqq 15$ mA).

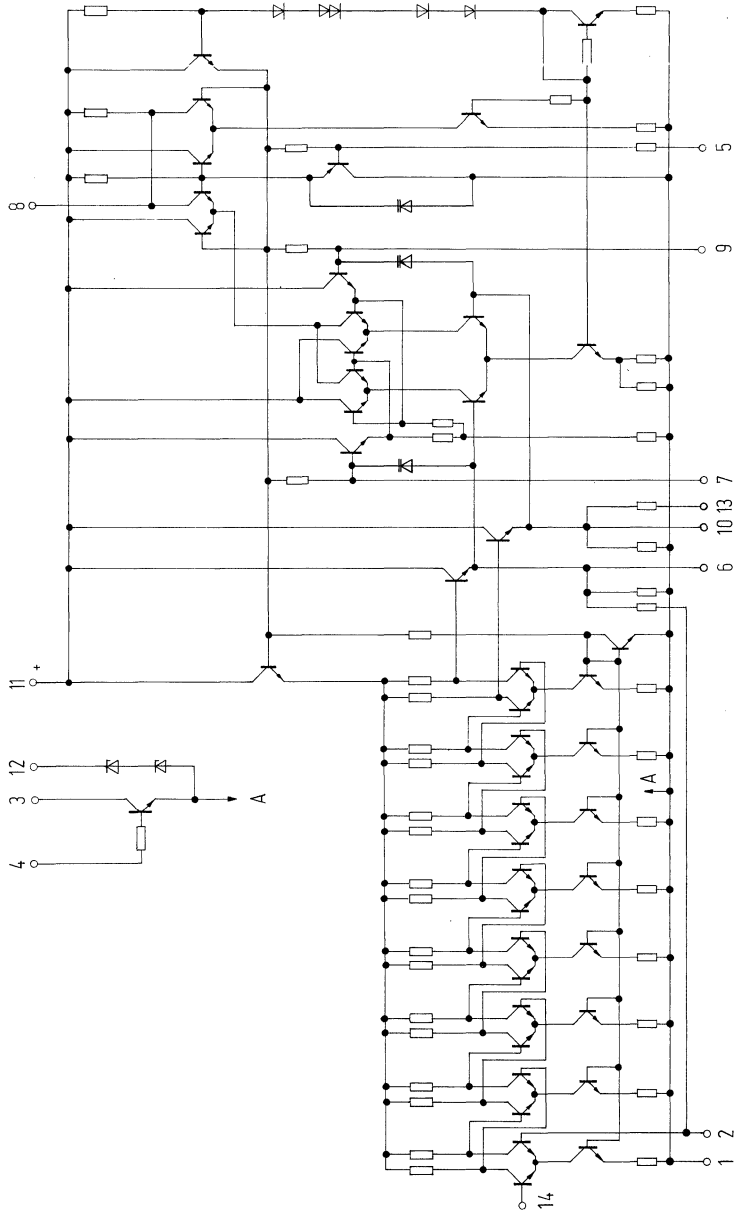
The IC TBA 120 S is supplied in different groups. Parameter is the volume. An attenuation of 30 dB requires a resistor between pin 5 and ground with a resistance value according to the group number tabulated below. The group number is imprinted on the plastic package.

Group	II	III	IV	V
R_{pot}	1.9 to 2.2	2.1 to 2.5	2.4 to 2.9	2.8 to 3.3

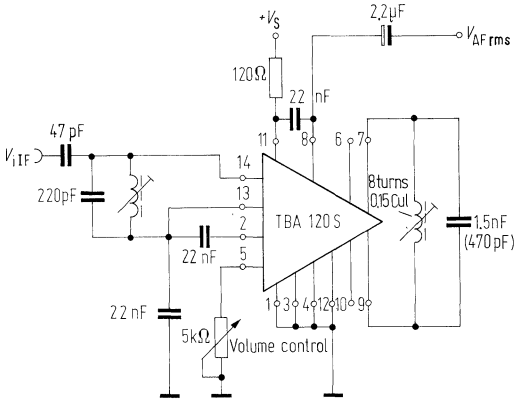
Test circuit



Circuit diagram



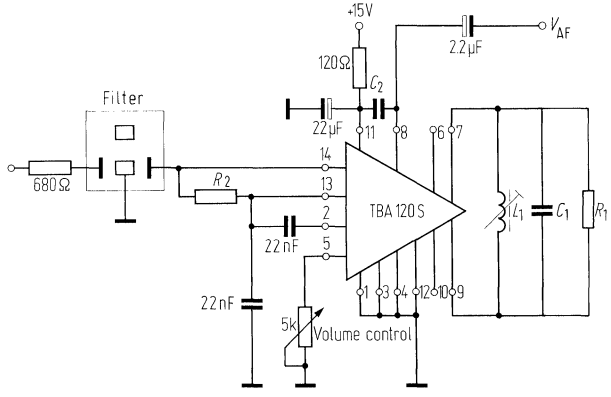
Application circuit 5.5 MHz (10.7 MHz)



Values in parentheses apply to 10.7 MHz

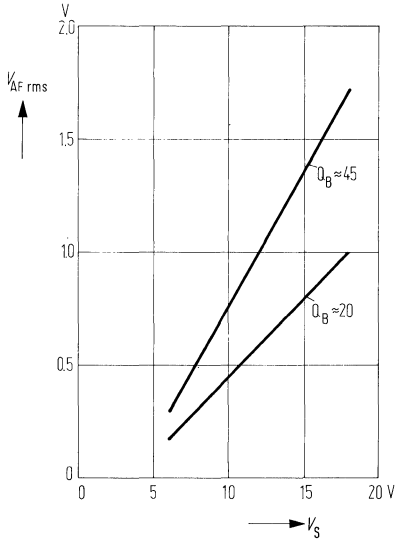
Application circuit with ceramic filter (Murata)

For a good adjacent channel suppression the ceramic filter should be combined with an *LC* network

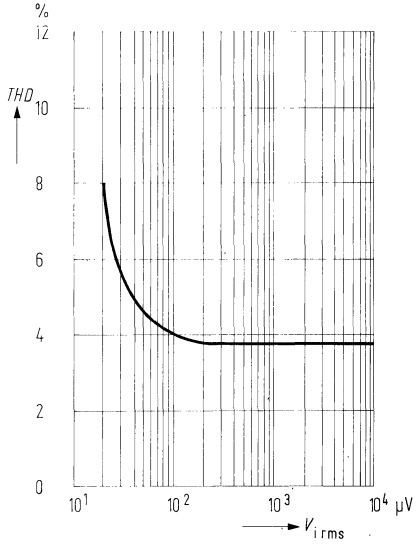


	Sound IF in TV sets	Sound IF in TV sets of American Std.	FM IF in radio mono sets	FM IF in radio stereo sets
C_1	1.5 nF	2.2 nF	470 pF	330 pF
C_2	22 nF	22 nF	22 nF	470 pF
L_1	8 turns, 0.15 CuL	8 turns, 0.15 CuL	8 turns, 0.15 CuL	12 turns, 0.15 CuL
R_1	∞	∞	∞	1 kΩ
R_2	680 Ω	1 kΩ	330 Ω	330 Ω
Filter (Murata)	SFE 5.5 MA	SFE 4.5 MA	SFE 10.7	SFE 10.7

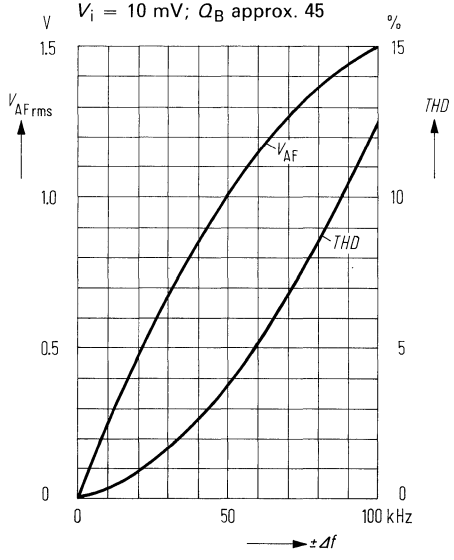
AF output voltage versus supply voltage
f_I = 5.5 MHz; Δf = ±50 kHz,
f_{mod} = 1 kHz; V_i = 10 mV



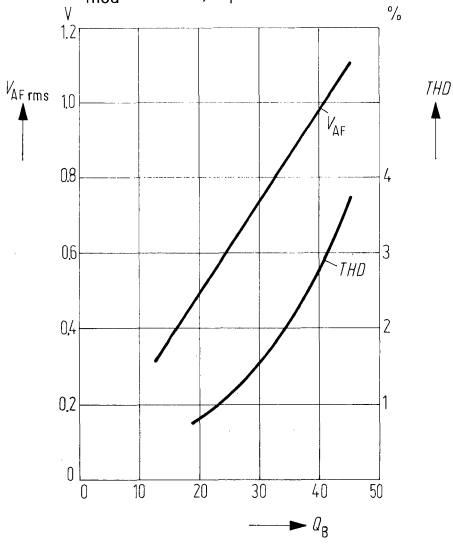
Total harmonic distortion versus input voltage
V_S = 12 V; f_I = 5.5 MHz; Δf = ±50 kHz;
f_{mod} = 1 kHz; Q_B approx. 45



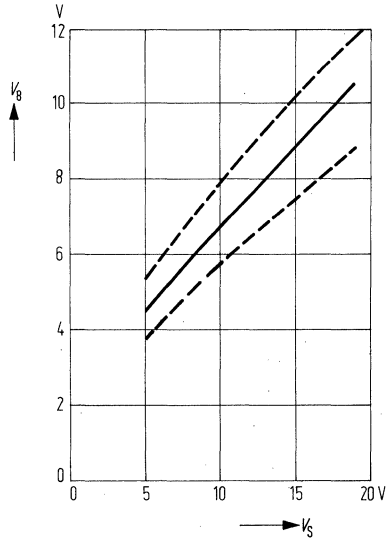
AF output voltage and total harmonic distortion v. frequency deviation
V_S = 12 V; f_I = 5.5 MHz; f_{mod} = 1 kHz
V_i = 10 mV; Q_B approx. 45



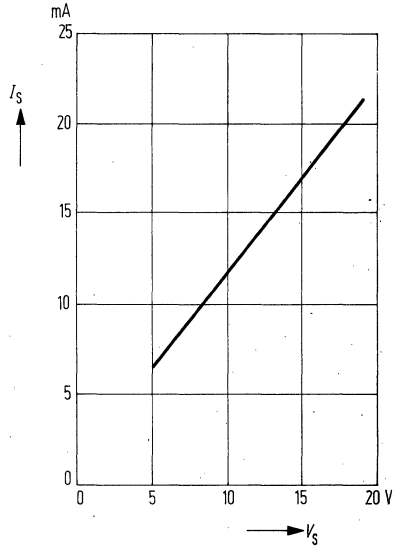
AF output voltage and total harmonic distortion versus Q_B factor
V_S = 12 V; Δf = ±50 kHz;
f_{mod} = 1 kHz; V_i = 10 mV



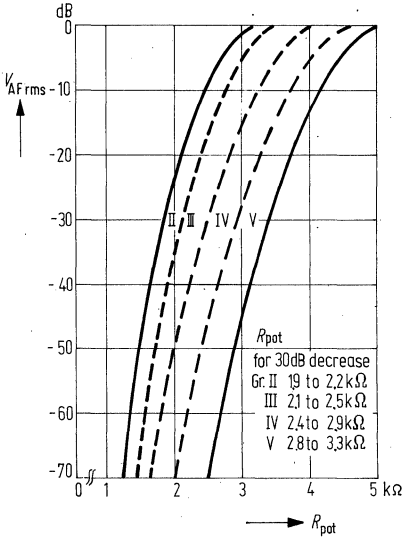
DC output voltage versus supply voltage



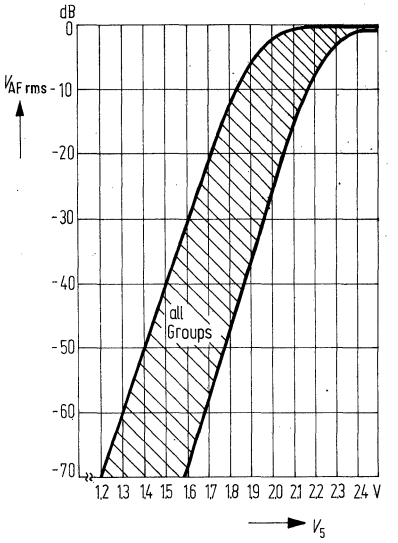
Current consumption versus supply voltage



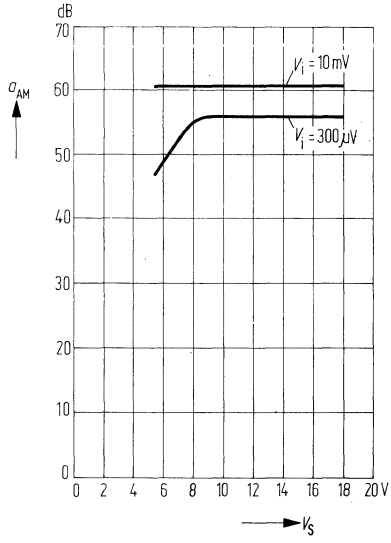
Volume control versus potentiometer resistance
V_S = 12 V; f_I = 5.5 MHz; Δf = ±50 kHz
f_{mod} = 1 kHz; V_i = 10 mV



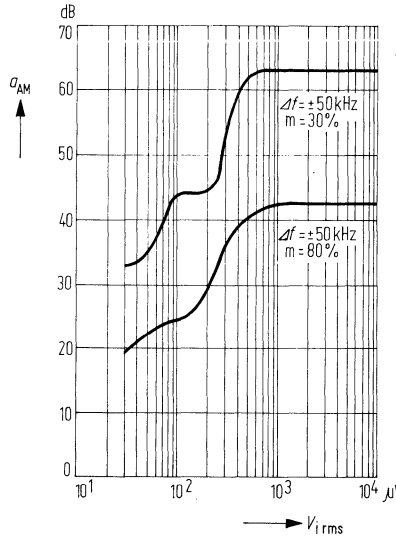
Volume control versus voltage to pin 5
V_S = 12 V; f_I = 5.5 MHz; Δf = ±50 kHz
f_{mod} = 1 kHz; Q_B approx. 45



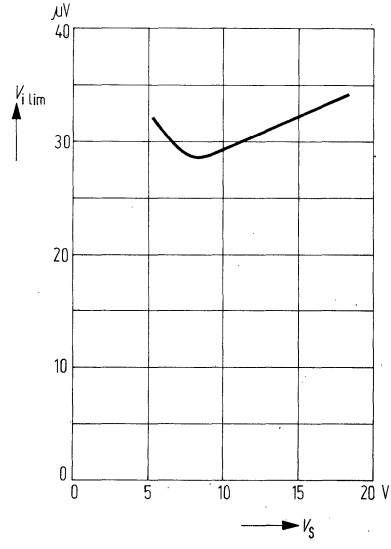
AM suppression versus supply voltage
f_I = 5.5 MHz; Δf = ±50 kHz; f_{mod} = 1 kHz
m = 30%; Q_B approx. 45



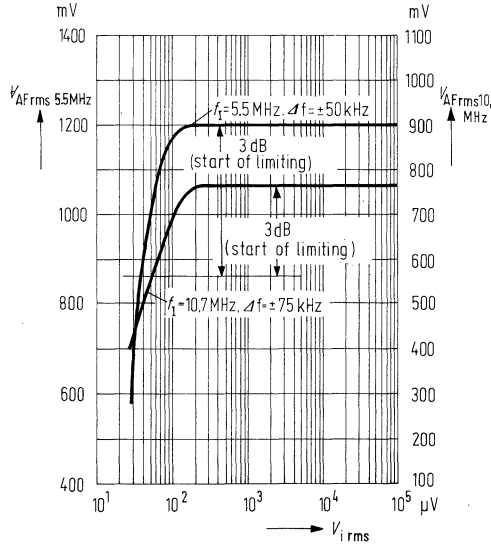
AM suppression versus input voltage
V_S = 12 V; f_I = 5.5 MHz; f_{mod} = 1 kHz
Q_B approx. 45



Input voltage for limiting versus supply voltage
f_I = 5.5 MHz; Δf = ±50 kHz;
f_{mod} = 1 kHz; Q_B approx. 45



AF output voltage versus input voltage
V_S = 12 V; f_{mod} = 1 kHz; Q_B approx. 45



FM IF Amplifier and Demodulator

TBA 120 T
TBA 120 U

Bipolar circuit

Symmetrical 8-stage amplifier with symmetrical coincidence demodulator for amplification, limiting, and demodulation of frequency-modulated signals, especially suited for the sound IF units in TV sets. In addition to the controlled AF output, an uncontrolled AF output and an AF input for the connection of video recorders is available.

- Outstanding limiting qualities
- Few external components
- Terminal for video recorder
- AF output voltage independent of supply voltage
- Insensitive to hum
- Very little residual IF

TBA 120 T: Input and demodulator matched to ceramic resonators
TBA 120 U: Input and demodulator matched to *LC* networks

Type	Ordering code	Package outline
TBA 120 T	Q67000-A919	DIP 14
TBA 120 U	Q67000-A920	

Maximum ratings

Supply voltage	V_S	18	V
Voltage	V_5	6	V
Current	I_4	5	mA
Thermal resistance (system-air)	$R_{th\ SA}$	90	K/W
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C

Range of operation

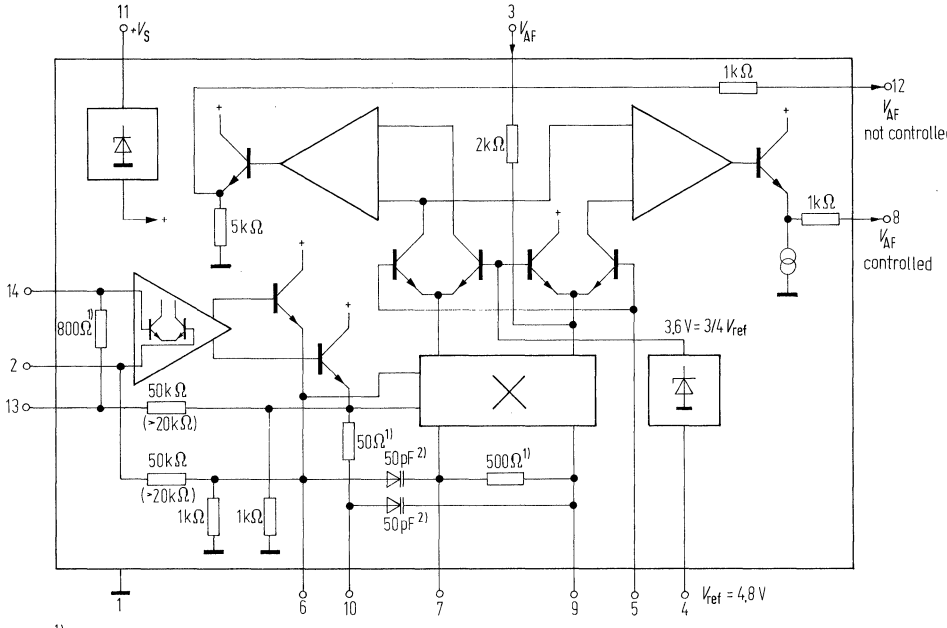
Supply voltage range	V_S	10 to 18	V
Ambient temperature range	T_{amb}	−15 to 70	°C
Frequency range	f	0 to 12	MHz

Characteristics (V_S = 12 V; T_{amb} = 25 °C, Q_B approx. 45, f_{IF} = 5,5 MHz)

		min	typ	max	
Current consumption	I_S	9.5	13.5	17.5	mA
IF voltage gain V_6/V_{14}	G_v		68		dB
IF output voltage with limiting at each output	V_{qpp}	175	250	325	mV
Output resistance	$R_{q\,8}$	0.8	1.1	1.4	kΩ
	$R_{q\,12}$	0.8	1.1	1.4	kΩ
Shunt resistance	$R_{13\text{-}14}$			1	kΩ
Input resistance	$R_{i\,3}$	1.4	2	2.6	kΩ
Internal resistance	$R_{i\,4}$		12	16	Ω
DC level of output signal	V_8	3.4	4	4.7	V
(V_i = O)	V_{12}	4.4	4.9	6.3	V
Stabilized voltage	V_4	4.2	4.8	5.3	V
Residual IF voltage without deemphasis	V_8		20		mV
	V_{12}		30		mV
AF gain (AF not attenuated)	V_8/V_3	6	7.5	8.5	
Attenuation ($R_{4\text{-}5}$ = 5 kΩ; $R_{5\text{-}1}$ = 13 kΩ)	V_{AF8}	20	30	40	dB
Range of volume control	$\frac{V_{AF8\,max}}{V_{AF8\,min}}$	70	85		dB
Resistance	$R_{4\text{-}5}$[1])	1		10	kΩ
Input voltage for limiting (Δf = ± 50 kHz; f_{mod} = 1 kHz)	$V_{i\,lim}$		30	60	μV
Hum suppression	V_8/V_{11}		35		dB
	V_{12}/V_{11}		30		dB
Signal-to-noise ratio (V_i = 10 mV)	$a_{S/N}$	80	85		dB
Noise voltage (according to DIN 45405) P_{pot} = 0	V_n		50	100	μV_{os}
Input impedance	$R_{q\,7\text{-}9}$		5.4		kΩ
TBA 120 T only:					
AF output voltage	$V_{8\,rms}$	650	900		mV
(Δf = ± 50 kHz; f_{mod} = 1 kHz)	$V_{12\,rms}$	400	650		mV
Input impedance	Z_i		800/5		Ω/pF
AM suppression (V_i = 500 μV; Δf = ± 50 kHz; m = 30%; f_{mod} = 1 kHz)	a_{AM}	50	60		dB
TBA 120 U only:					
AF output voltage	$V_{8\,rms}$	850	1200		mV
(Δf = ± 50 kHz; V_i = 10 mV; f_{mod} = 1 kHz; THD = 4%)	$V_{12\,rms}$	600	1000		mV
Input impedance (f_I = 5.5 MHz)	Z_i	15/6	40/4.5		kΩ/pF
AM suppression (Δf = ± 50 kHz; V_i = 500 μV; f_{mod} = 1 kHz; m = 30%)	a_{AM}	50	60		dB
Total harmonic distortion (Δf = ± 25 kHz; V_i = 10 mV; f_{mod} = 1 kHz)	THD		1.3	2.5	%

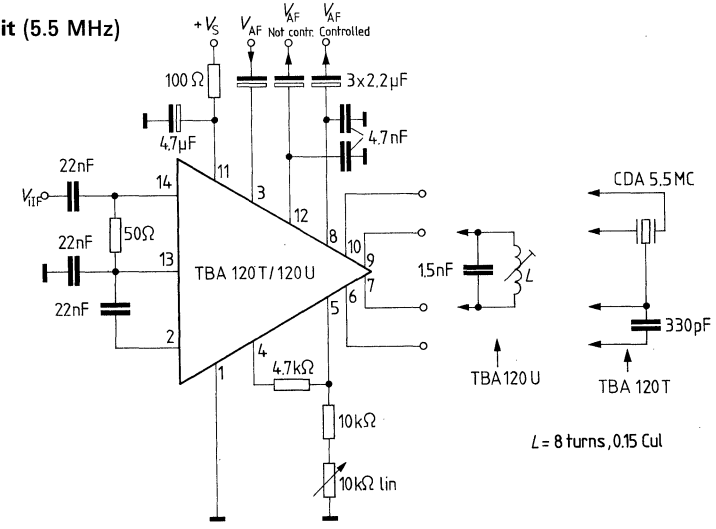
1) If DC volume control is not used, pin 4 has to be connected directly to pin 5.

Block diagram

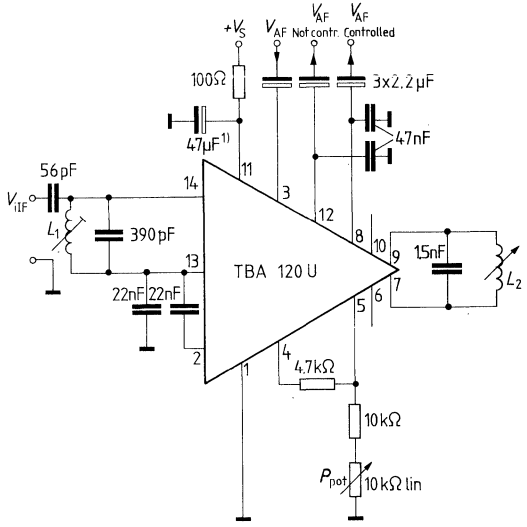


1) only TBA 120 T
2) only TBA 120 U

Test circuit (5.5 MHz)

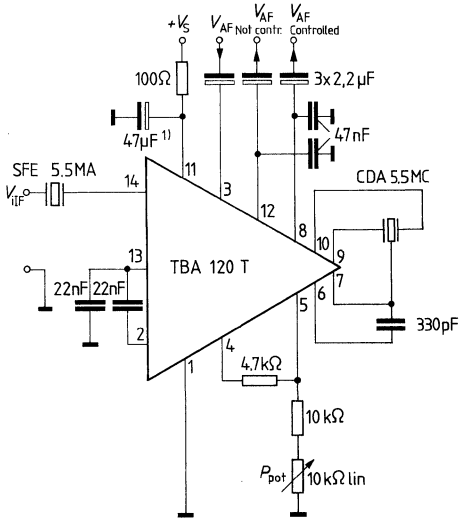


Application circuit TBA 120 U for 5.5 MHz



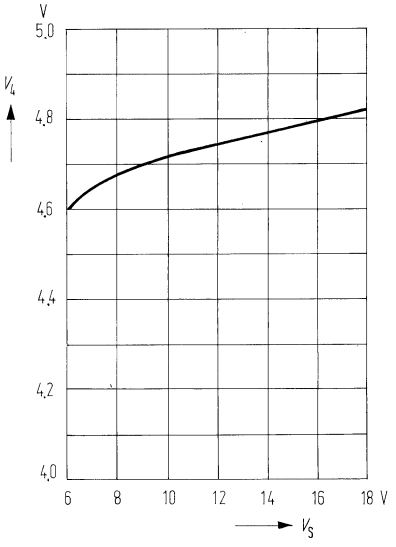
L_1: 20 turns 15 × 0.05 CuLS; $Q_0 \approx 73$
L_2: 9 turns 0.25 CuLS; $Q_0 \approx 40$
Coil Assembly Vogt D41 – 2165 (2438)
without gaussion core

Application circuit TBA 120 T for 5.5 MHz

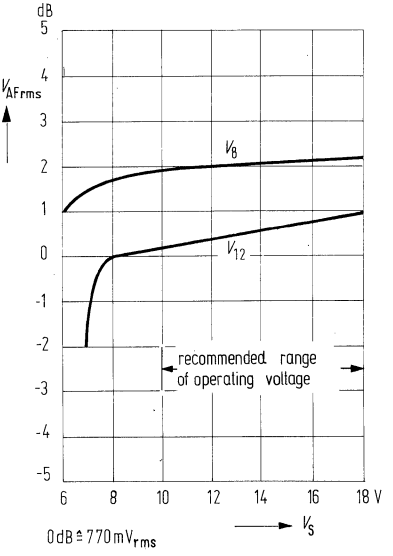


[1]) Omitting the electrolytic capacitor 47 µF on pin 11 changes volume-control range.

Z voltage versus supply voltage

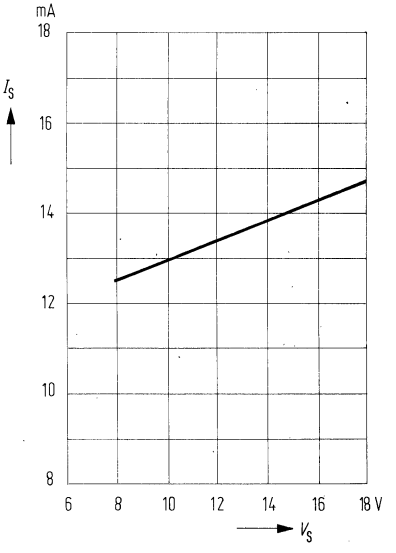


AF output voltage versus supply voltage

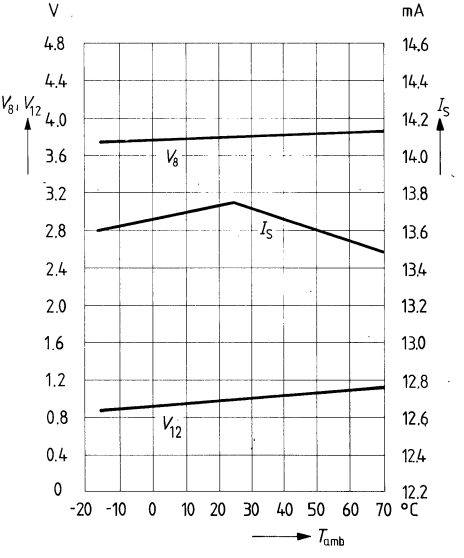


• 0dB ≙ 770 mV_{rms}

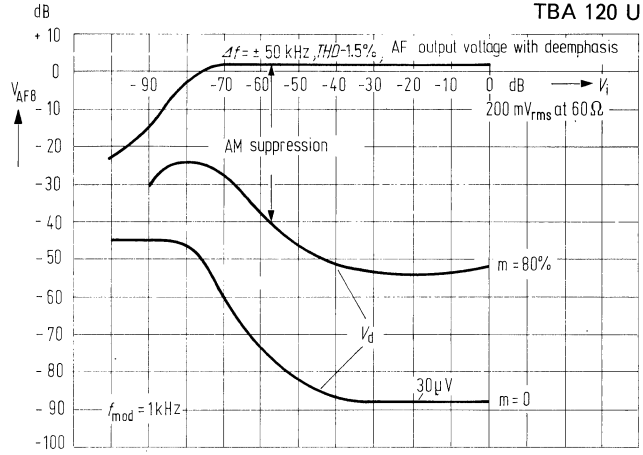
Current consumption versus supply voltage



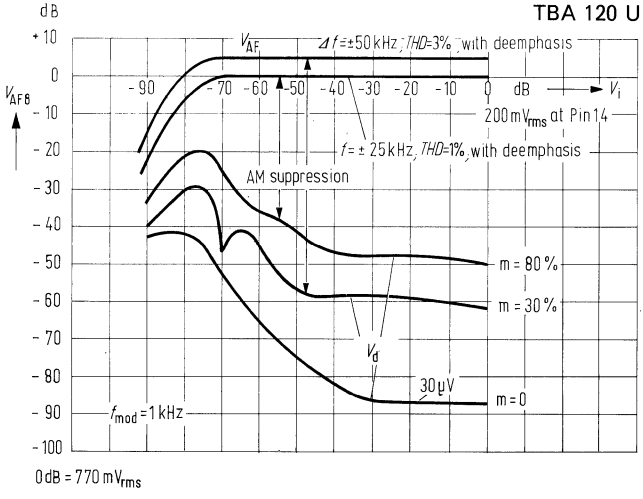
AF output voltage and current consumption versus ambient temperature



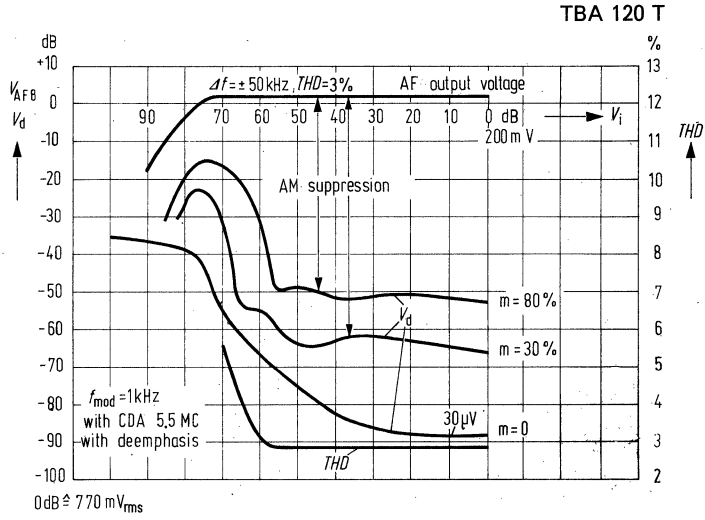
AF output voltage and disturbance voltage versus input voltage
(Input wired with SFE 5.5 MA/Murata)



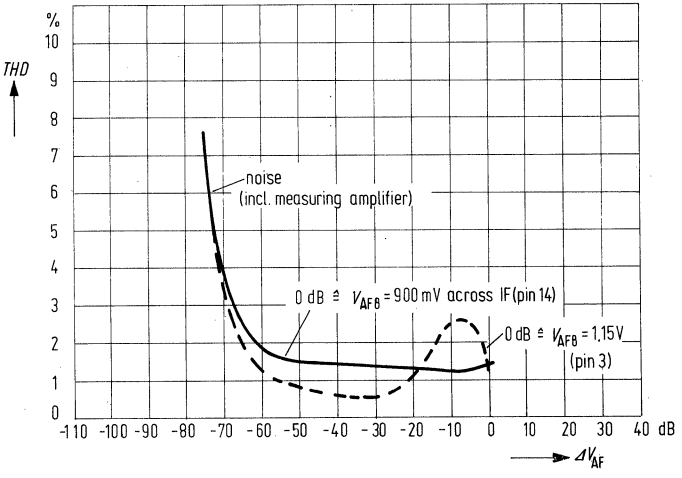
AF output voltage and disturbance voltage versus input voltage
(Input 60 Ω impedance broadband)



AF output voltage (pin 8), disturbance voltage, and total harmonic distortion versus input voltage

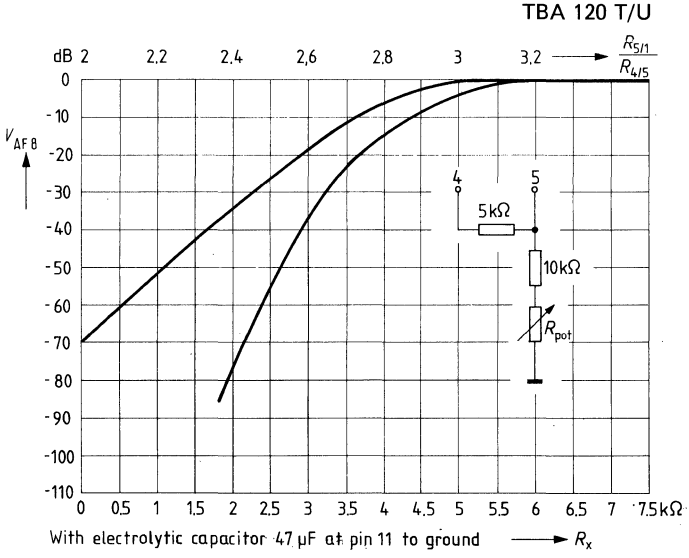


Total harmonic distortion versus volume control

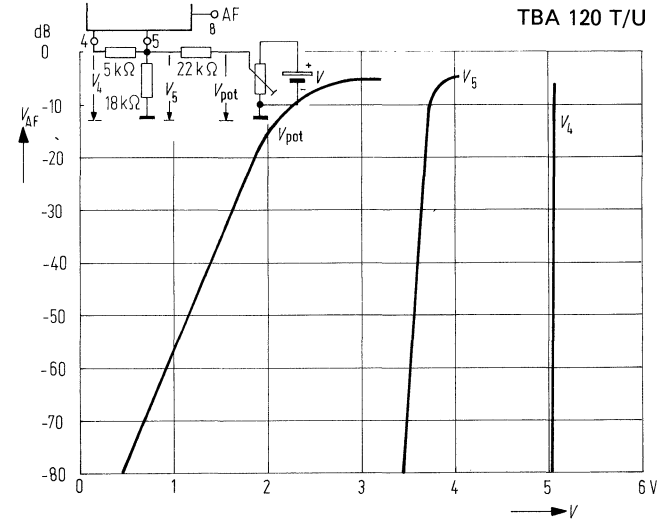


Spread

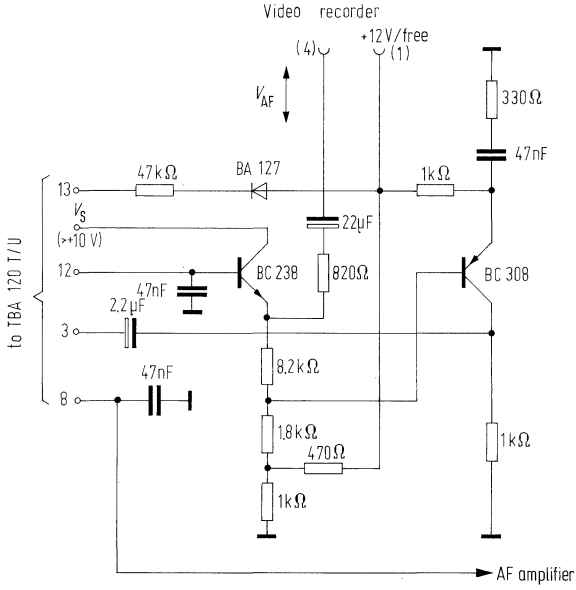
AF output voltage (pin 8) versus potentiometer resistance and versus ratio of resistance



AF output voltage (pin 8) versus voltage fed into pin 5



Circuit for direct connection to video recorders



Socket (1): Switching voltage: at playback: + 12 V
at recording: free
Socket (4): Simultaneous input and output for AF

Function

When the switching voltage is applied, the emitter follower, BC 238, is blocked on the output and the buffer stage, BC 308, is switched on. It includes a pre-emphasis to balance the de-emphasis at the AF output. The IF amplifier is put out of operation by the diode, BA 127, and the 47 kΩ resistor. The remotely controllable volume regulator in the TBA 120 T/U is used for recording and playback.

Controlled AM Amplifier with Demodulator and AF Volume Control

TDA 1048

Bipolar circuit

The integrated circuit TDA 1048 contains a gain-controlled push-pull amplifier, a demodulator, and a DC volume control. The AF outputs are referred to ground and stabilized against hum of the supply voltage.

The IC TDA 1048 is particularly suited for the use in the sound section of TV sets of French Standard (amplitude modulation).

- High input sensitivity
- Distortion-low control
- Distortion-low demodulation
- Volume control by means of DC voltage
- Internally stabilized supply voltage

Type	Ordering code	Package outline
TDA 1048	Q67000-A1090	DIP 16

Maximum ratings

Supply voltage	V_S	16.5	V
Output current	I_{11}	5	mA
Thermal resistance (system-air)	$R_{th\ SA}$	90	K/W
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C

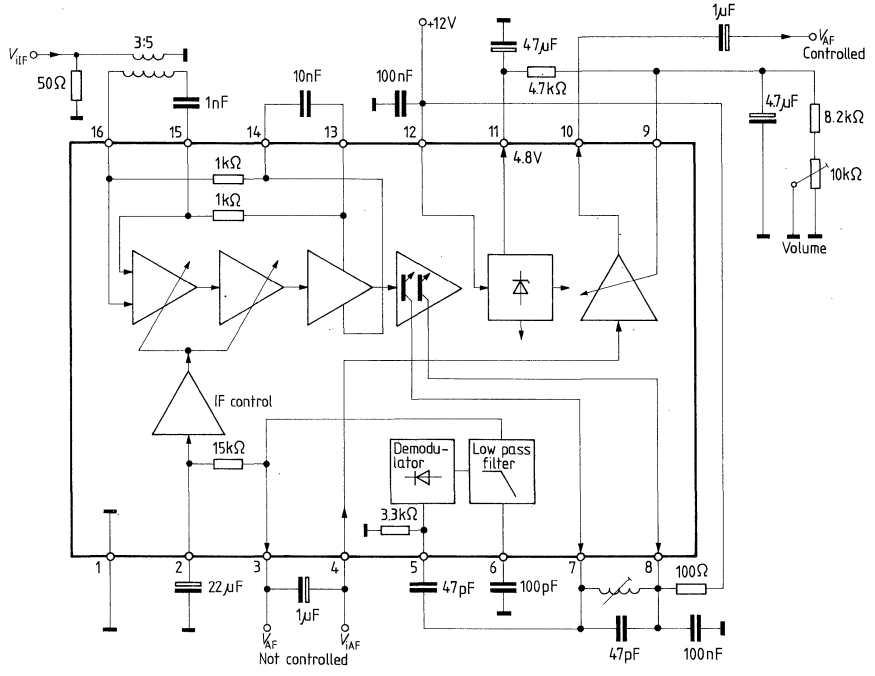
Range of operation

Supply voltage range	V_S	10 to 15	V
Ambient temperature range	T_{amb}	0 to 60	°C

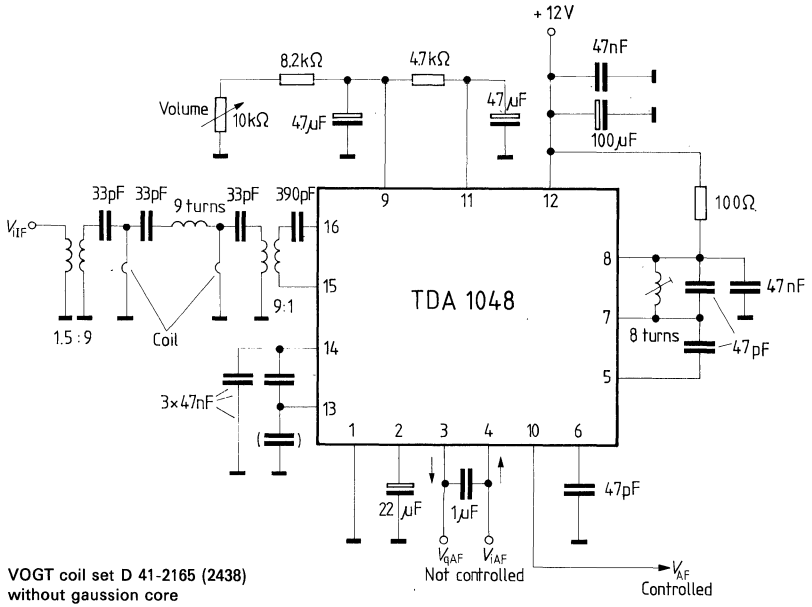
Characteristics (V_S = 12 V; f_i = 40 MHz; f_{mod} = 1 kHz; T_{amb} = 25 °C)

		min	typ	max	
Total current consumption	$I_{12}+I_7+I_8$	29	37	45	mA
Output DC currents of amplifier	$I_7 = I_8$		4		mA
Input voltage for AGC threshold	V_i	100			µV
Control range	ΔG	50	60		dB
AF output voltage (m = 80%)	$V_{q\,10}$	0.9	1.2	1.5	V_{rms}
Total harmonic distortion (m = 80%)	THD		1.3	2.0	%
Output resistance	$R_{q\,3}$		200	300	Ω
	R_{q10}		50	100	Ω
Load resistance	R_{L3}	3.3			kΩ
	$R_{L\,10}$	3.3			kΩ
Stabilized voltage	V_{11}	4.4		5.8	V
Range of volume control	$\Delta G_{10\text{-}4}$	70	80		dB
Gain of the AF part	ΔG	6	7		dB
Input resistance	$R_{i\,4}$	6.5			kΩ
Potentiometer resistance for −30 dB attenuation	R_{pot}	3.4		4	kΩ

Test circuit and block diagram

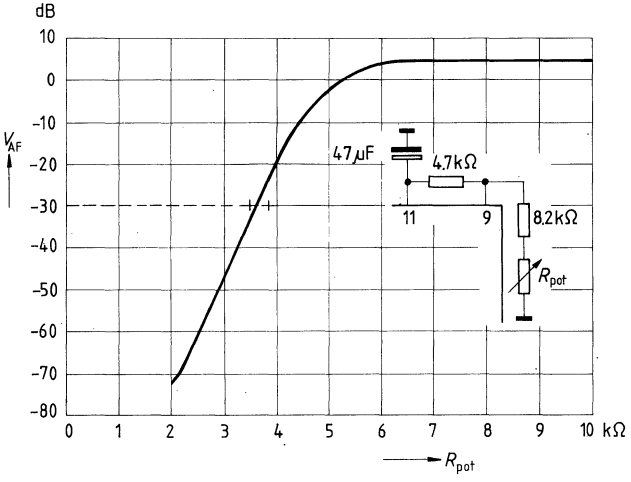


Application circuit for $f_{i\,IF}$ = 39.2 MHz



VOGT coil set D 41-2165 (2438)
without gaussion core
wire: 0.25 CuLS

AF output voltage versus potentiometer resistance
V_S = 15 V



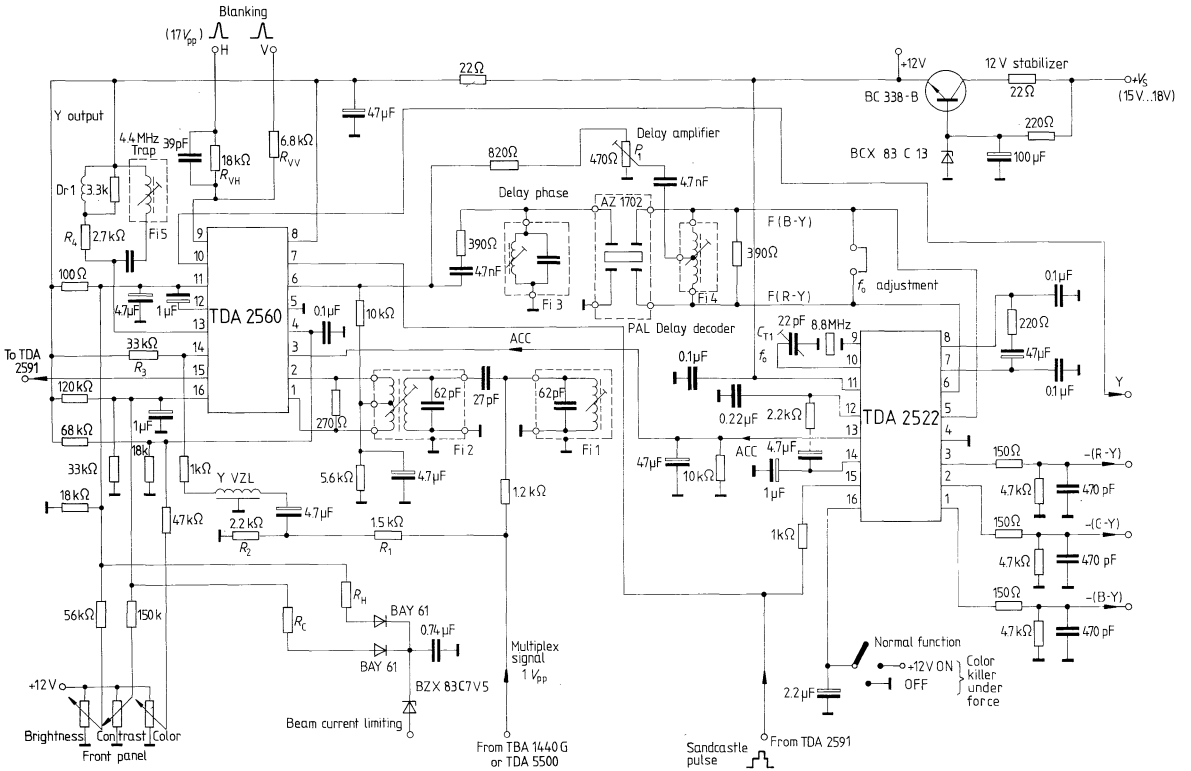
After demodulation of the IF signal in the video IF amplifier (e.g. TBA 1440 G) in color TV sets, the color TV signal is divided into the individual color components red, green, and blue in a color preparation circuit. These color signals drive the individual cathodes of the color picture tube via one video final stage each.

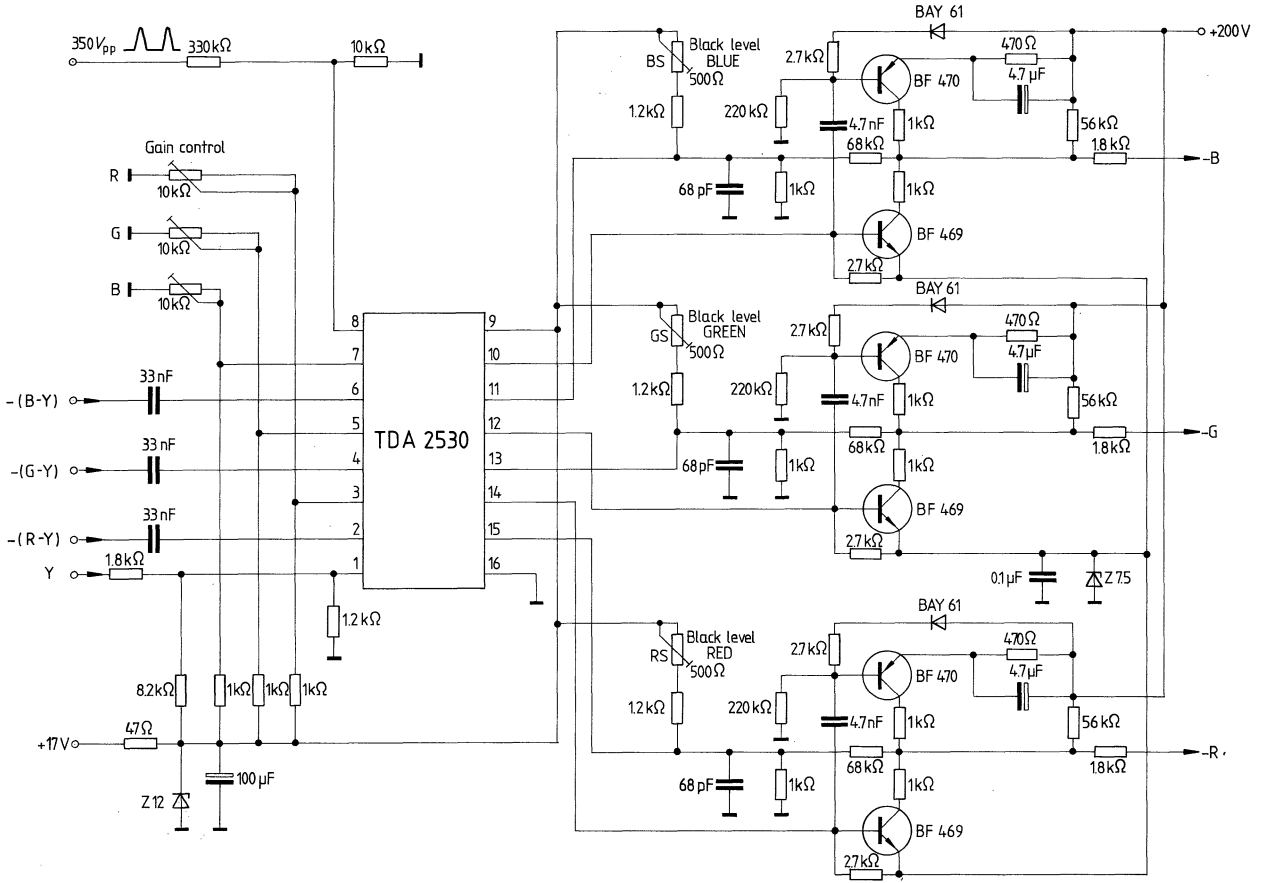
The ICs TDA 2522, TDA 2530, and TDA 2560 are available for color preparation. After separating the video signal in a luminance portion and a chrominance portion, the TDA 2560 serves in this connexion as a combined luminance and chrominance amplifier. Control of contrast, brightness, and color saturation are additionally included in the TDA 2560.

The chrominance signal is separated into a blue and a red portion in an external delay line decoder. The TDA 2522 finally demodulates both the chrominance signals and delivers at the output color difference signals of the three basic colors. Preparation of the reference carrier frequency in the TDA 2522 is based upon twice the color subcarrier frequency. The color subcarrier components necessary for demodulation and offset by 90° can, thus, be provided by means of a 2 : 1 divider without requiring any adjustment.

It is the TDA 2530 where the color signals red, green, and blue, necessary for driving the color tube, are generated in a matrix circuitry by adding the luminance portion to the color difference signals.

Apart from the color ICs TDA 2522 and TDA 2560, use of the horizontal combination TDA 2591 is also recommended. Thus, the sandcastle pulse — important for color decoding — may very easily be made available.


Blanking
(17 V_{pp})
H
V
22Ω
+12V
12 V stabilizer
BC 338-B
22Ω
+V_S
(15 V...18V)
220Ω
BCX 83 C 13
100 µF
Y output
4.4MHz Trap
39pF
18kΩ
R_{VH}
6.8kΩ
R_{VV}
47µF
820Ω
Delay amplifier
470Ω
P_1
4.7nF
Delay phase
AZ 1702
Dr1
3.3k
R_4
2.7kΩ
Fi 5
390Ω
4.7nF
Fi 3
Fi 4
390Ω
F(B-Y)
F(R-Y)
f_0 adjustment
0.1µF
100Ω
47µF
1µF
TDA 2560
0.1µF
10kΩ
220Ω
47µF
0.1µF
ACC
PAL Delay decoder
22pF
8.8MHz
C_{T1}
f_0
To TDA 2591
33kΩ
R_3
0.1µF
Y
120kΩ
62pF
27pF
62pF
0.22µF
2.2kΩ
TDA 2522
68kΩ
1µF
270Ω
Fi 2
Fi 1
150Ω
-(R-Y)
33kΩ
18kΩ
1kΩ
Y VZL
5.6kΩ
4.7µF
47µF
10kΩ
ACC
4.7µF
4.7kΩ
470 pF
18kΩ
47kΩ
2.2kΩ
R_2
4.7µF
1.2kΩ
1.5kΩ
R_1
1µF
150Ω
-(C-Y)
1kΩ
4.7kΩ
470 pF
150Ω
-(B-Y)
56kΩ
150k
R_H
R_C
BAY 61
0.74µF
4.7kΩ
470 pF
Normal function
+12V ON
OFF
Color killer under force
Multiplex signal
1 V_{pp}
BAY 61
2.2µF
+12V
BZX 83C7V5
Brightness
Contrast
Color
Front panel
Beam current limiting
From TBA 1440G or TDA 5500
Sandcastle pulse
From TDA 2591


350 Vpp
330 kΩ
10 kΩ
Gain control
R
G
B
10 kΩ
33 nF
-(B-Y)
-(G-Y)
-(R-Y)
Y
1.8 kΩ
TDA 2530
1.2 kΩ
8.2 kΩ
1 kΩ
47 Ω
+17 V
100 µF
Z 12
BAY 61
Black level BLUE
BS
500 Ω
2.7 kΩ
1.2 kΩ
220 kΩ
4.7 nF
68 kΩ
68 pF
BF 470
BF 469
470 Ω
4.7 µF
56 kΩ
+200 V
-B
Black level GREEN
GS
-G
Black level RED
RS
-R
0.1 µF
Z 7.5

Synchronous Demodulator Combination for PAL Color TV Receivers

TDA 2522

Bipolar circuit

The IC TDA 2522 comprises the following circuit portions

- 8.8-MHz color subcarrier oscillator with divider stage for the production of both 4.4-MHz reference signals.
- Production of the chrominance signal control voltage and a reference voltage
- Production of the color killer and identification signal
- Color killer delay
- Two synchronous demodulators for (B-Y) and (R-Y) signals
- Matrix for (G-Y)-signal
- PAL flipflop and PAL switch
- Blanking in the synchronous demodulators

Type	Ordering code	Package outline
TDA 2522	Q67000-A1230	DIP 16

Maximum ratings

Supply voltage	V_{11}	14	V
Thermal resistance (system-air)	$R_{th\ SA}$	90	K/W
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C

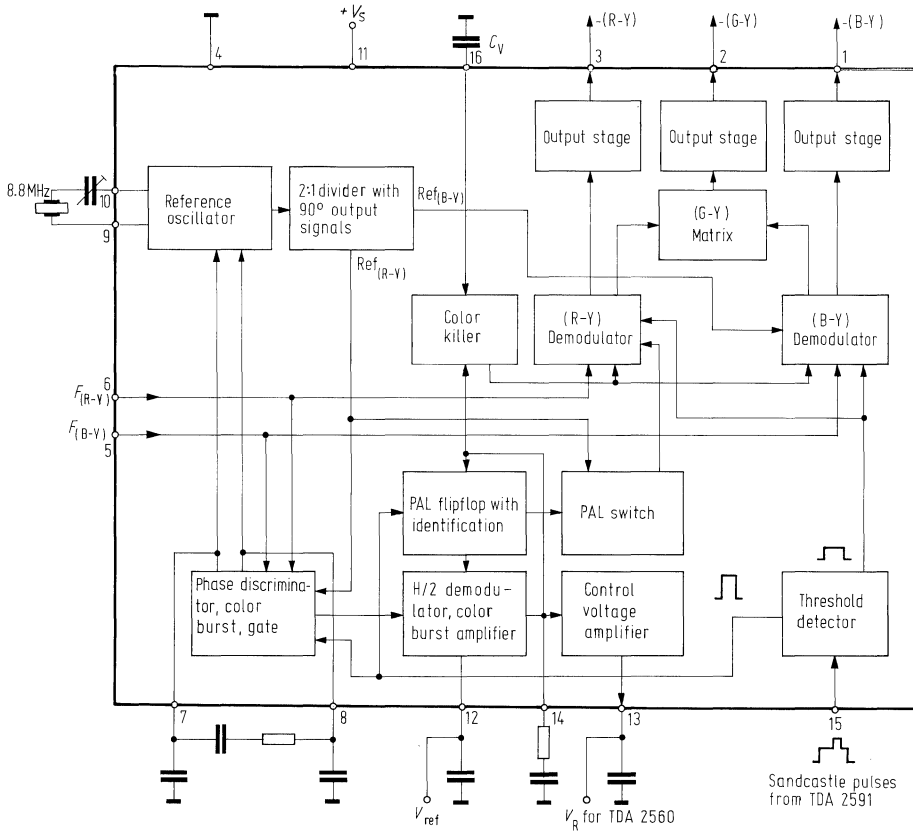
Range of operation

Supply voltage range	V_{11}	10.8 to 13.2	V
Ambient temperature range	T_{amb}	−20 to 60	°C

Characteristics (V_{11} = 12 V; T_{amb} = 25 °C)

		min	typ	max	
Current consumption	I_{11}		48		mA
Ratio of demodulated signals at $V_{F(B-Y)} = V_{F(R-Y)}$	$V_{(B-Y)}$		1.78 $V_{(R-Y)}$		V
Matrix for (G-Y)-signal	(G-Y)		−0.51 (R-Y) −0.19 (B-Y)		
Input resistance of the chrominance signal inputs	$R_{i\ F(R-Y)}$	800			Ω
	$R_{i\ F(B-Y)}$	800			Ω
Input capacitance of the chrominance signal inputs	$C_{i\ F(R-Y)}$			10	pF
	$C_{i\ F(B-Y)}$			10	pF
Output voltages of color difference	$V_{q\ (R-Y)}$	2.4			V_{pp}
	$V_{q\ (G-Y)}$	1.35			V_{pp}
	$V_{q\ (B-Y)}$	3			V_{pp}
DC voltage at the color difference signal outputs	$V_3; V_2; V_1$		5.6		V
Output resistance of the color difference signal outputs	$R_{q\ (R-Y)}$		250		Ω
	$R_{q\ (G-Y)}$		250		Ω
	$R_{q\ (B-Y)}$		250		Ω
H/2 ripple voltage at (R-Y) output	$V_{H/2}$			10	mV_{pp}
Input resistance of the 8.8 MHz oscillator	$R_{i\ 9}$		270		Ω
Output resistance of the 8.8 MHz oscillator	$R_{q\ 10}$		200		Ω
Total holding range	Δf		±500		Hz
Key pulses (at pin 15) coming from horizontal combination TDA 2591					
Color sync. signal gating ON	V_{15}	7.5			V
OFF	V_{15}			6.5	V
Blanking ON	V_{15}	2			V
OFF	V_{15}			1	V
Voltage at pin 14 without color sync signal	V_{14}		7		V
with color sync signal (peak-to-peak value) of 0.25 V at pins 5 and 6	V_{14}		5.5		V
Reference output voltage	V_{12}		7		V
Chrominance signal control voltage (depending on V_{14})					
at $\pm I_{13} < 200\ \mu A$	V_{13}		0.5 to 5		V
at $V_{14} < 5.5$ V	V_{13}			1	V
Phase difference between reference signal and color sync signal at ±400 Hz frequency deviation	φ		±5		degree
Color killing at	V_{14}	6			V
or at	V_{16}		12		V
Color setting at	V_{14}			5.6	V
or at	V_{16}		0		V
Color setting delay (by C_v at pin 16)	t_v		24		ms/μF

Block diagram with application hint



Bipolar circuit

The IC TDA 2530 is intended for driving RGB final stage transistors.
The following stages are integrated:

- Clamping control circuit
- Matricing facility
- Electronic potentiometer for gain adjustment
- Facing-coupled driver amplifier

Type	Ordering code	Package outline
TDA 2530	Q67000-A1295	DIP 16

Maximum ratings

Supply voltage	V_9	15	V
Voltages	V_1	V_9	V
	V_3; V_5; V_7	V_9	V
	V_2; V_4; V_6	V_9	V
	V_8	V_9	V
	V_{10}; V_{12}; V_{14}	$> V_{11}$; V_{13}; V_{15}	V
	V_{10}; V_{12}; V_{14}	$< V_9$	V
	V_{11}; V_{13}; V_{15}	$> 0.3 \cdot V_9 / < V_9$	V
Current	$-I_8$	1	mA
Thermal resistance (system-air)	$R_{th\ SA}$	90	K/W
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C

Range of operation

Supply voltage range	V_9	10.8 to 13.2	V
Ambient temperature range	T_{amb}	−20 to 60	°C

Characteristics (V_9 = 12 V; V_1 = 1.5 V; T_{amb} = 25 °C) according to application circuit

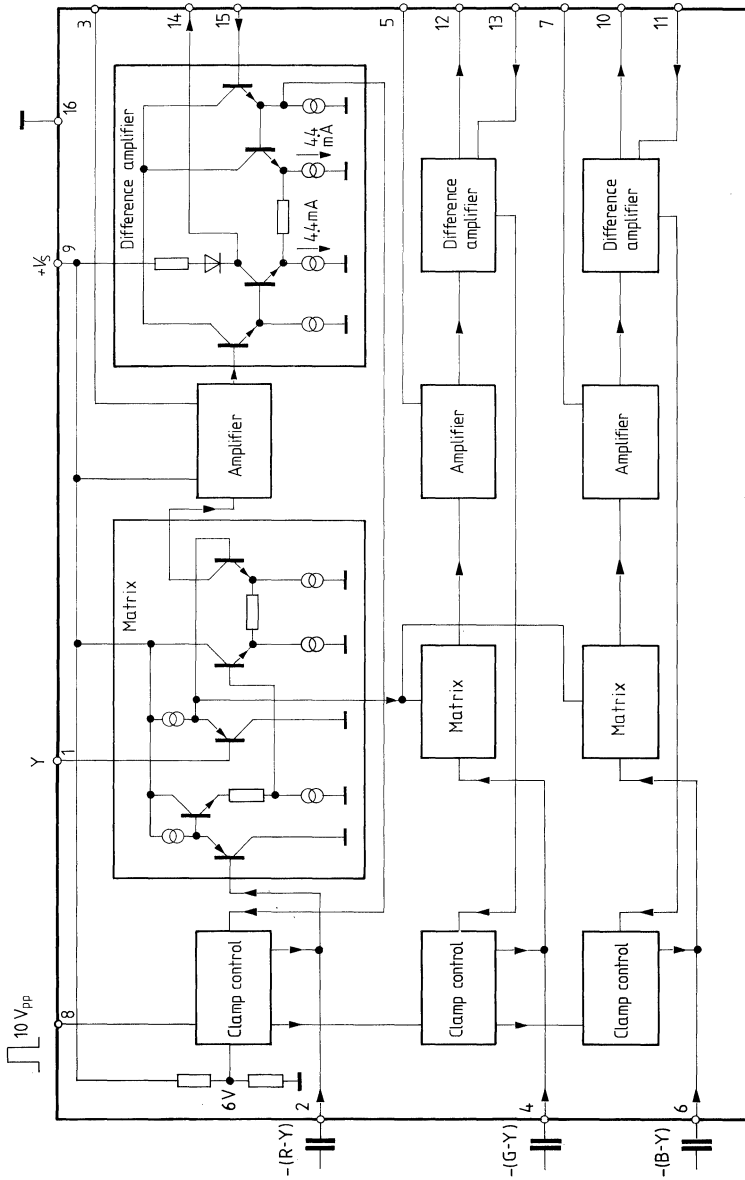
		min	typ	max	
Luminance signal input					
Black level	V_1		1.5		V
BA signal voltage	V_1		1.0		V_{pp}
Input resistance	$R_{i\,1}$	100			kΩ
Color difference signal inputs					
Input voltages	V_2		1.4		V_{pp}
	V_4		0.82		V_{pp}
	V_6		1.78		V_{pp}
Input currents	I_2; I_4; I_6		2	4	µA
Feedback inputs					
DC voltage level during clamping	V_{11}; V_{13}; V_{15}		6		V
Adjustment of ac voltage gain					
Adjusting voltage range	V_3; V_5; V_7		0 to 10		V
Adjusting voltage for nominal gain	V_3; V_5; V_7		5		V
Nominal gain between color difference signal inputs or Y input, resp., and feedback inputs 11, 13, 15	G[1])		0		dB
Adjusting range of this gain at $\Delta V_{3,5,7}$ = ± 5 V	ΔG	± 3			dB
Output difference amplifier					
Transconductance of the difference amplifier	S_d		20		mA/V
Integr. load resistors[2])	$R_{10/9}$		680		Ω
	$R_{12/9}$		680		Ω
	$R_{14/9}$		680		Ω
Clamping pulse input for dc voltage feedback					
Input voltage for clamping IN	V_8[3])		6.5 to 12		V
OUT	V_8		0 to 5.5		V
Input current for clamping IN	I_8			1	µA
OUT	$-I_8$			20	µA

[1]) If inputs 11, 13, 15 are not connected, nominal gain will appear.

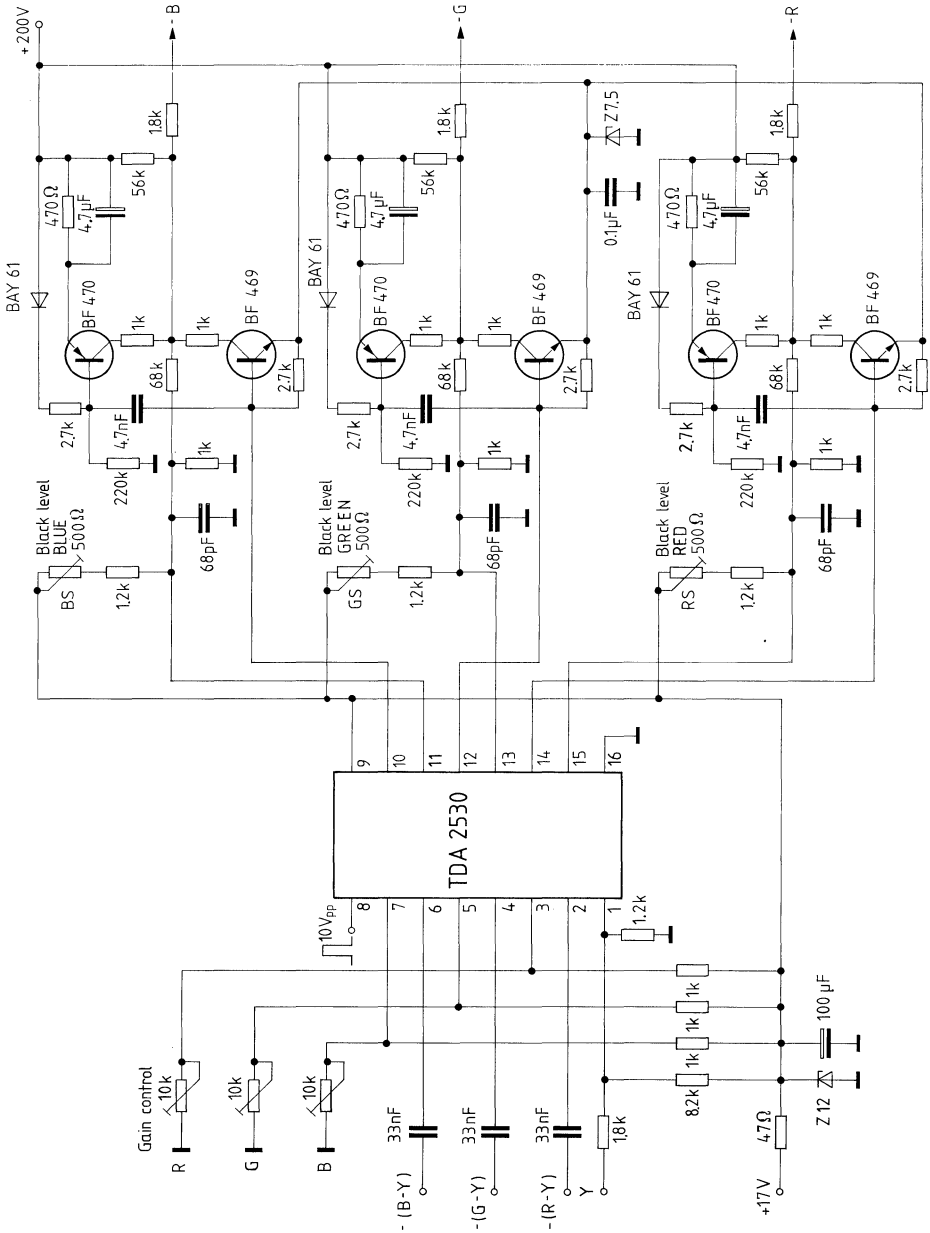
[2]) The integrated load resistors are each in series with one diode, which causes the resistors to become ineffective at V_{10}, V_{12}, $V_{14} > V_9$.
The external load resistors, needed in this case, have to be designed for a current of 4.4 mA nom.

[3]) The changeover clamping IN to clamping OUT is performed at V_8 approx. 6 V.

Block diagram



Application circuit



Luminance and Chrominance Combination for PAL TV Receivers

TDA 2560

Bipolar circuit

The integrated circuit TDA 2560 contains:

Luminance amplifier

with adaptation circuit for Y-delay line
contrast and brightness control
blanking and gating
additional video output with positive-going synchronous level

Chrominance amplifier

with controlled chrominance signal amplifier
saturation and contrast control
direct driving of the PAL delay line
common output for chrominance and color sync signal (without influencing the color sync signal amplitude by contrast and saturation control)

Type	Ordering code	Package outline
TDA 2560	Q67000-A1231	DIP 16

Maximum ratings

Supply voltage	V_8	14	V
Thermal resistance (system-air)	$R_{th\ SA}$	90	K/W
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C

Range of operation

Supply voltage range	V_8	9 to 14	V
Ambient temperature range	T_{amb}	−20 to 60	°C

Characteristics (V_8 = 12 V; T_{amb} = 25 °C) according to application circuit[1])

		min	typ	max	
Current consumption	I_8		46		mA
Luminance amplifier[2])					
Input current	I_{14}		0.2		mA_{pp}
Input resistance	$R_{i\,14}$		150		Ω
Contrast control range	E_K	20			dB
Brightness control range (black level)	V_{10}		1 to 3		V
Brightness control voltage	V_{11}		1 to 3		V
Black level shifting by contrast control, picture contents and temperature	ΔV			±20	mV
3 dB bandwidth	B		5		MHz
BAS output voltage with positively directed sync level	V_{15}		3.4		V_{pp}
Black level clamping pulse[3])	V_7		6		V
Blanking pulses[4])					
for 0 V at output (pin 10)	V_9		2		V
for 1.5 V at output (pin 10)	V_9		5		V
Chrominance amplifier					
Input voltage	$V_{2/1}$		4 to 80		mV_{pp}
Obtainable output signal[5])	V_6		2		V_{pp}
Control range of the chrominance signal amplifier	ΔG_{chro}	30			dB
Starting of the chrominance signal control[6])	V_3		1.1		V
Contrast synchronism (at 10-dB contrast variation)	K		±1		dB
Saturation control range[7])	E_S		+6 to −50		dB
Color sync signal gating[3])	V_7		2		V
Signal-to-noise ratio at nominal input voltage	$a_{S/N}$	50	1.5		dB
Phase shifting of the color sync signal to the chrominance signal				±5	degree

For remarks see next page

Remarks to the previous page

[1]) Supply voltage range V_8 = 9 to 14 V,
admissible hum voltage V_{8pp} = 100 mV

[2]) The gain of the luminance amplifier can be influenced by the load resistance R_g at pin 13. The scattering of the gain is reduced to a minimum, since it only depends on the scattering of the relationship between Y delay line terminating resistance and the resistor R_g.

[3]) Key pulses (from TDA 2591) for color sync signal keying and for black level clamping are sent to pin 7.
The black level clamping becomes effective at + 6 V, the key pulses must be in that time that clamping only becomes effective at the black slope of the black shoulder. The color sync signal gate circuit, which switches the gain of the chrominance signal amplifier during its return to maximum, becomes effective at + 1.5 V.

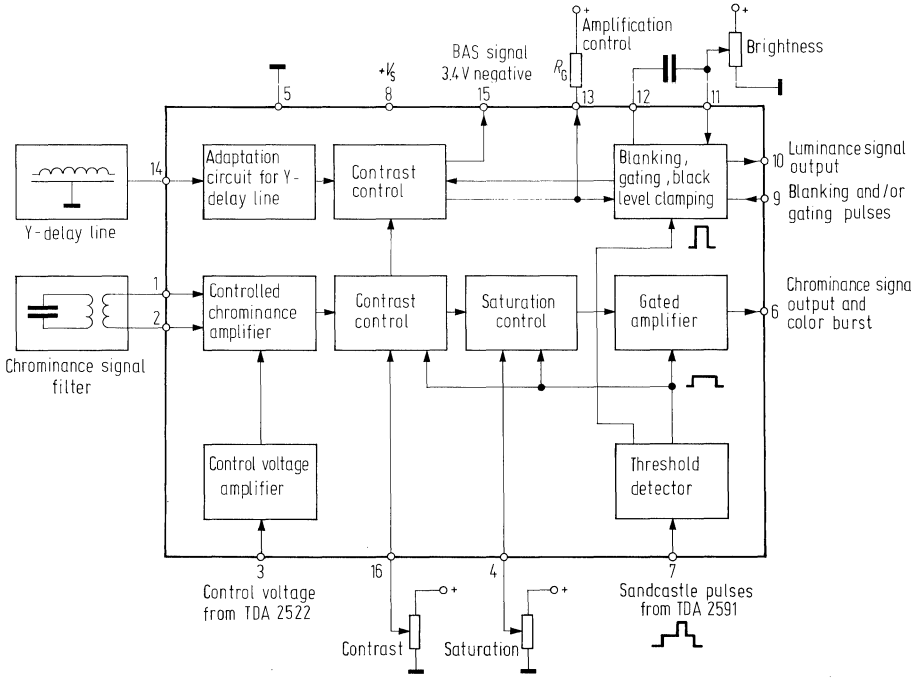
[4]) The luminance signal is keyed via pin 9:
when the key pulse reaches + 2 V, the luminance signal output (10) is blanked;
at + 5 V, a standard level of approx. 1.5 V is keyed which can be used for clamping.

[5]) Chrominance signal and color sync signal are both available at pin 6. The color sync signal is not influenced by contrast and saturation control; it remains stable by means of the control voltage of TDA 2522.
The ratio of the chrominance signal to the color sync signal is at nominal contrast (3 dB below maximum) and at nominal saturation (6 dB below maximum) the same at the output and at the input.

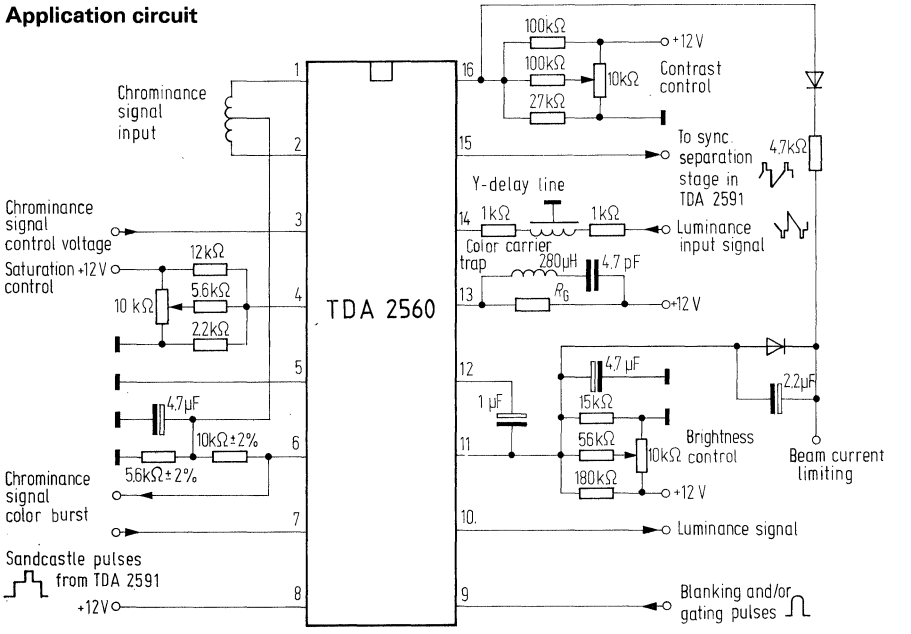
[6]) When the voltage becomes more negative, the gain is reduced.

[7]) Linear range down to −40 dB.

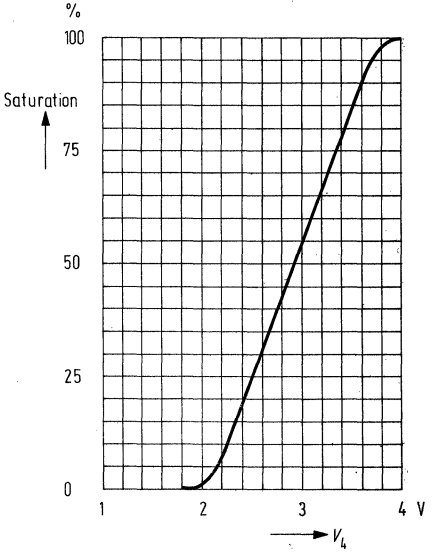
Block diagram



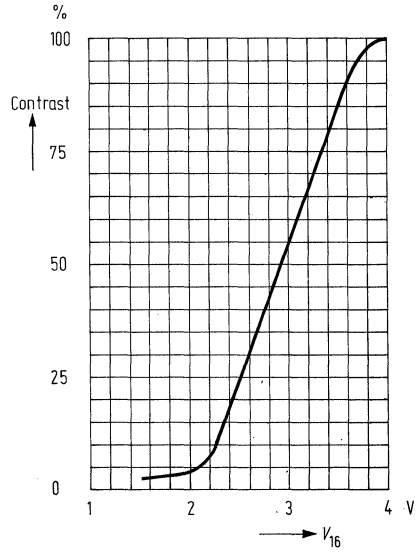
Application circuit



Saturation control



Contrast control



Bipolar circuit

The integrated circuit TDA 2591 is adapted to the integrated color circuits TDA 2522 and TDA 2560. It includes the following stages:

- Line oscillator according to the threshold switch principle
- Phase comparsion between sync pulse and oscillator (φ_1)
- Internal gating pulse for phase discriminator φ_i
- Phase comparison between line flyback pulse and oscillator (φ_2)
- Catching range extension by coincidence detector φ_3 (coincidence between sync and gating pulse)
- Time constant and gate switching (VCR operation)
- Sync pulse separation stage
- Blanking circuit for interference signal
- Vertical sync pulse separation stage and output stage
- Production of gating pulses for color sync signal and for line flyback blanking pulses
- Phase shifter for control pulse
- Switching of control pulse width and switch-off
- Output stage with separate supply voltage for direct triggering of thyristor deflection circuits
- Control pulse switch-off in case of too low supply voltage

Type	Ordering code	Package outline
TDA 2591	Q67000-A1365	DIP 16

Maximum ratings

Supply voltage	V_1	13.2	V
Voltages	V_2	18	V
	V_4	13.2	V
	V_9	−6/7	V
	V_{10}	−6/7	V
	V_{11}	13.2	V
Currents	I_2	650	mA
	I_3	−650	mA
	I_4	1	mA
	I_6	±10	mA
	I_7	−10	mA
	I_{11}	2	mA
Thermal resistance (system-air)	$R_{th\ SA}$	90	K/W
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C

Range of operation

Supply voltage range	V_1	9 to 13	V
Ambient temperature range	T_{amb}	−20 to 60	°C

Characteristics (V_S = 12 V; t_{fly} = 12 µs; T_{amb} = 25 °C)

		min	typ	max	
Current consumption	I_1		30		mA
Control pulses, positive (pin 3)					
Output voltage	V_3	10	11		V_{pp}
Output resistance front slope (high)	$R_{q\,3}$		2.5		Ω
back slope (low)	$R_{q\,3}$		20		Ω
Duration of control pulses at thyristor operation (V_4 = 9.4 V to V_1)	t_{Th}	5.5		8.5	µs
Duration of control pulses at transistor operation (V_4 = 0 to 3.5 V)	t_{Tr}		14 + t_d		µs
Control pulse switch-off	V_1			4	V
Switching of control pulse width and switch-off (pin 4)					
for t = 6 µs (thyristor operation)					
Input voltage	V_4	9.4		V_1	V
Input current (V_4 = V_1)	I_4	200			µA
for t = 14 µs + t_d (transistor operation)					
Input voltage	V_4	0		3.5	V
Input current (V_4 = 0 V)	I_4			−200	µA
for t = 0 (V_3 = 0 V)					
Input voltage	V_4	5.4		6.6	V[1]
Input current (V_4 = $V_{1/2}$)	I_4	−10		10	µA
Phase comparison φ_2 and phase shifter (pin 5)					
Control voltage range	V_5	5.4		7.6	V
Control current	± I_5		1		mA_{pp}
Reverse current (V_5 = 6.5 V)	$I_{5\,o}$			5	µA
Output resistance V_5 = 5.4 to 7.6 V	$R_{q\,5}$		high ohmic		[2]
V_5 < 5.4 V/> 7.6 V	$R_{q\,5}$		8		kΩ
Admissible delay between front slope of control pulse and line flyback pulse	t_d			15	µs
Static control error	$\Delta t/\Delta t_d$			0.2	%
Total phase position					
Phase position between mid sync pulses and line flyback pulses	Δt	1.9	2.6	3.3	µs
Total phase position and phase position of front slope of control pulses is set automatically by phase comparison φ_2.					
If additional setting is required, current can be supplied via pin 5. It then applies	$\Delta I/\Delta t$		30		µA/µs
Line flyback pulse input (pin 6)					
Input switching voltage	$V_{6\,switch}$		1.4		V
Input voltage limitation	$V_{6\,lim}$	−0.7		+1.4	V
Input current	I_6	0.01		1	mA

[1]) or input 4 open
[2]) Current source circuit configuration

Characteristics (cont'd)

		min	typ	max	
Color sync signal gating pulses, positive (pin 7)					
Output voltage	$V_{q\,7}$	10	11		V_{pp}
Output resistance	$R_{q\,7}$		70		Ω
Output current during back slope	I_7		2		mA
Width of color sync signal gating pulses at $V_7 = 7$ V	t	3.7		4.3	µs
Phase position between mid sync pulses at input and front slope of color sync signal gating pulses at $V_7 = 7$ V	t_{SB}	2.45		3.15	µs
Line flyback blanking pulses, positive (pin 7)					
Output voltage	V_7	2.5		3.5	V_{pp}
Output resistance	$R_{q\,7}$		70		Ω
Output current during back slope	I_7		2		mA
Vertical sync pulses, positive (pin 8)					
Output voltage	$V_{q\,8}$	10	11		V_{pp}
Output resistance	$R_{q\,8}$		2		kΩ
Delay between front slopes of input signal and output signal	$t_{V\,an}$		15		µs
Delay between back slopes of input signal and output signal	$t_{V\,ab}$		$t_{V\,an}$		
Sync pulse separation stage (pin 9)					
Input switching voltage	$V_{i\,9\,S}$		0.8		V
Input switching current	$I_{i\,9\,S}$	5		100	µA
Input modulation current	$I_{i\,9\,T}$			100	µA
Input switch-off current	$I_{i\,9\,A}$	100	150		µA
Input leakage current ($V_9 = -5$ V)	$I_{i\,9\,O}$			1	µA
Input signal (-BAS)	$V_{i\,9}$	3		4	V_{pp}[1])
Interference signal blanking circuit (pin 10)					
Input switching voltage	$V_{i\,10}$		1.4		V
Input switching current	$I_{i\,10\,S}$	100	150		µA
Input modulation current	$I_{i\,10\,T}$	5		100	µA
Input leakage current ($V_{10} = -5$ V)	$I_{10\,O}$			1	µA
Input signal (-BAS)	$V_{i\,10}$	3		4	V_{pp}[1])
Admissible superposed interference signal	V_{10}			7	V

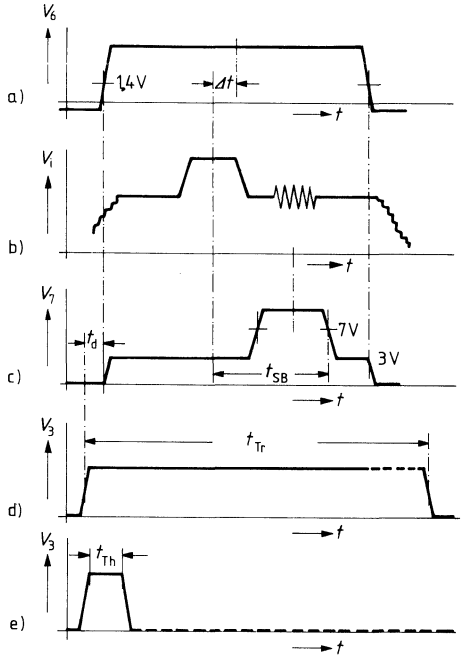
[1]) Admissible range: 1 to 7 V

Characteristics (cont'd)

		min	typ	max	
Coincidence detector φ_3 (pin 11)					
Output voltage, no coincidence	$V_{q\,11}$			0.5	V
Output voltage, with coincidence	$V_{q\,11}$	5			V
Output current, no coincidence	$I_{q\,11}$		0.1		mA
Output current, with coincidence	$I_{q\,11}$		−0.5		mA
Switching to VCR operation (pin 11)					
Input voltage	$V_{i\,11}$	0		1.5	V
Input current (V_{11} = 0 V)	$I_{i\,11}$	−200			µA
or					
Input voltage	$V_{i\,11}$	9		V_1	V
Input current ($V_{11} = V_1$)	$I_{i\,11}$			2	mA
Time constant switch (pin 12)					
Output voltage	$V_{q\,12}$		6		V
Output current, limited to	$\pm I_{12}$		1		mA
output resistance V_{11} = 2.5 to 7 V	$R_{q\,12}$		100		Ω
Output resistance V_{11} <1.5 V/>9 V	$R_{q\,12}$		60		kΩ
Phase comparison φ_1 (pin 13)					
Control voltage range	V_{13}	3.8		8.2	V
Control current	$\pm I_{13}$		2		mA
Leakage current at V_{13} = 4 to 8 V	$I_{13\,O}$			1	µA
Output resistance V_{13} = 4 to 8 V	$R_{q\,13}$		high ohmig		[2]
Output resistance V_{13} <3.8 V/>8.2 V	$R_{q\,13}$		low ohmic		[4]
Control sensitivity	S_φ		2		kHz/µs
Catching and holding range	Δf		±780		Hz
Scattering of catching and holding range	$\Delta(\Delta f)$		±10		%[5]
Oscillator (pins 14 and 15)					
Lower threshold voltage	$V_{14\,S}$		4.4		V
Upper threshold voltage	$V_{14\,S}$		7.6		V
Reverse current	$\pm I_{14\,V}$		0.47		mA
Oscillator frequency (unsynchronized)					
at C_{osc} = 4.7 nF; R_{osc} = 12 kΩ	f_o		15,625		Hz
Scattering of oscillator frequency	Δf_o		±5		%[5]
Frequency-adjusting level	$\Delta f_o/\Delta I_{15}$		31		Hz/µA
Adjusting range for the indicated external circuitry	Δf_o		±10		%
Dependence of oscillator frequency on supply voltage	$\frac{\Delta f_o/f_o}{\Delta V_1/V_1}$		±0.05		[5]
Frequency modification with supply voltage lowered to V_S = 5 V	Δf_o		±10		%[5]
Temperature coefficient of oscillator frequency	TC_f		$\pm 10^{-4}$		Hz/K[5]

[1]) or input 4 open
[2]) Current source switching
[3]) Admissible range 1 to 7 V
[4]) Emitter follower
[5]) Scattering of external components is not considered.

Phase relations



a) Line flyback pulse

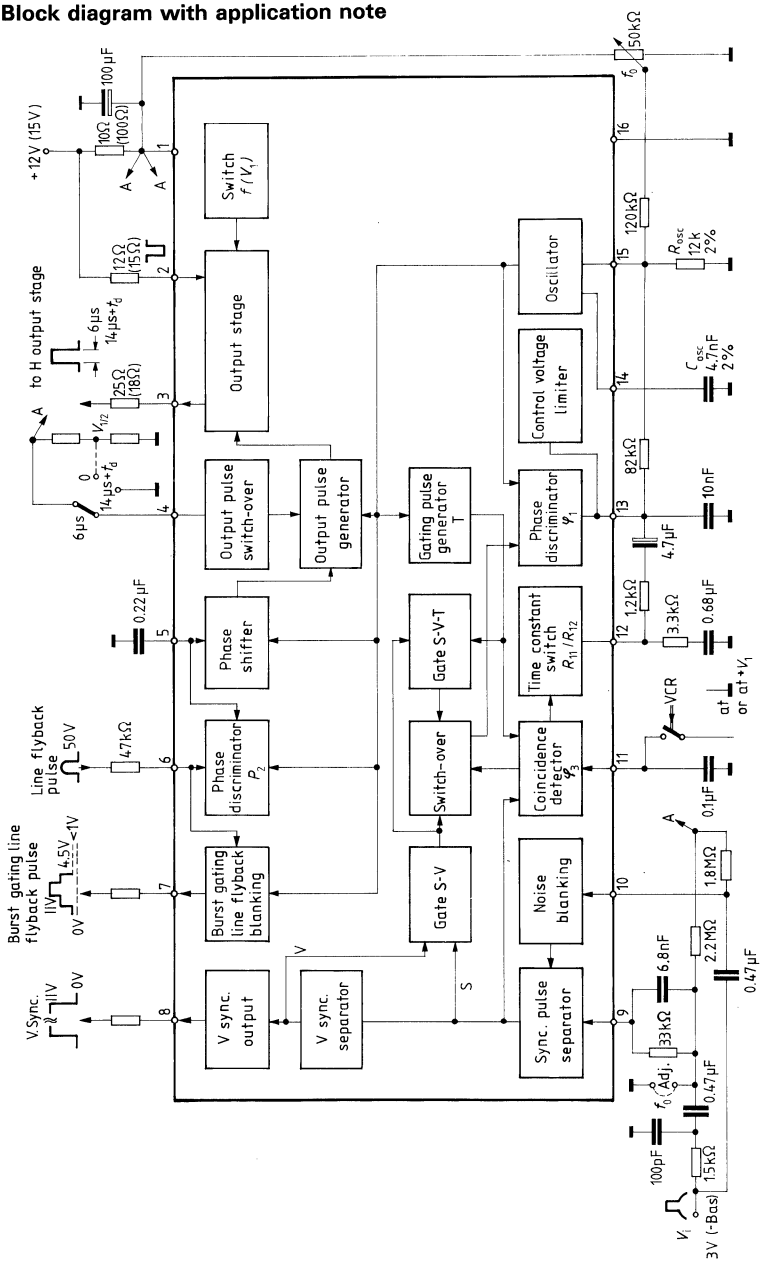
b) FBAS input signal

c) Color sync gating pulse and line flyback blanking pulse

d) Transistor output pulse ($V_4 < 3.5$ V)

e) Thyristor output pulse ($V_4 > 9.4$ V)

Block diagram with application note



Horizontal Combination with Improved Sandcastle Pulse for TV Receivers

TDA 2593

Bipolar circuit

The IC TDA 2593 is matched to the color ICs TDA 2522 and TDA 2560. It includes an improved sandcastle pulse with a new H flyback blanking threshold as well as the following stages:

- Line oscillator according to the threshold switch principle
- Phase comparsion between sync pulse and oscillator (φ_1)
- Internal gating pulse for phase discriminator φ_1
- Phase comparison between line flyback pulse and oscillator (φ_2)
- Catching range extension by coincidence detector φ_3 (coincidence between sync and gating pulse)
- Time constant and gate switching (VCR operation)
- Sync pulse separation stage
- Blanking circuit for interference signal
- Vertical sync pulse separation stage and output stage
- Production of gating pulses for color sync signal and of line flyback blanking pulses
- Phase shifter for control pulse
- Switching of control pulse width and switch-off
- Output stage with separate supply voltage application for direct triggering of thyristor deflection circuits
- Switching off of control pulse in case of too low supply voltage

Type	Ordering code	Package outline
TDA 2593	Q67000-A1524	DIP 16

Maximum ratings

Supply voltage	V_1	13.2	V
Voltages	V_2	18	V
	V_4	13.2	V
	V_9	−6/7	V
	V_{10}	−6/7	V
	V_{11}	13.2	V
Currents	I_2	650	mA
	I_3	−650	mA
	I_4	1	mA
	I_6	±10	mA
	I_7	−10	mA
	I_{11}	2	mA
Thermal resistance (system-air)	$R_{\text{th SA}}$	90	K/W
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C

Range of operation

Supply voltage range	V_1	9 to 13	V
Ambient temperature range	T_{amb}	−20 to 60	°C

Characteristics (V_S = 12 V; t_{fly} = 12 µs; T_{amb} = 25 °C)

		min	typ	max	
Current consumption	I_1		30		mA
Control pulses, positive (pin 3)					
Output voltage	V_3	10	11		V_{pp}
Output resistance front slope (high)	$R_{q\,3}$		2.5		Ω
back slope (low)	$R_{q\,3}$		20		Ω
Duration of control pulses at thyristor operation (V_4 = 9.4 V to V_1)	t_{Th}	5.5		8.5	µs
Duration of control pulses at transistor operation (V_4 = 0 to 3.5 V)	t_{Tr}		$14+t_d$		µs
Control pulse switch-off at	V_1			4	V
Switching of control pulse width and switch-off (pin 4)					
for t = 6 µs (thyristor operation)					
Input voltage	V_4	9.4		V_1	V
Input current ($V_4 = V_1$)	I_4	200			µA
for t = 14 µs + t_d (transistor operation)					
Input voltage	V_4	0		3.5	V
Input current (V_4 = 0 V)	I_4			−200	µA
for t = 0 (V_3 = 0 V)					
Input voltage	V_4	5.4		6.6	V [1]
Input current ($V_4 = V_{1/2}$)	I_4	−10		10	µA
Phase comparison φ_2 and phase shifter (pin 5)					
Control voltage range	V_5	5.4		7.6	V
Control current	$\pm I_5$		1		mA_{pp}
Leakage current (V_5 = 6.5 V)	$I_{5\,0}$			5	µA
Output resistance V_5 = 5.4 to 7.6 V	$R_{q\,5}$		high ohmic		[2]
V_5 <5.4 V/>7.6 V	$R_{q\,5}$		8		kΩ
Admissible delay between front slope of control pulse and line flyback pulse	t_d			15	µs
Static control error	$\Delta t/\Delta t_d$			0.2	%
Total phase position					
Phase position between mid sync pulse and line flyback pulse	Δt	1.9	2.6	3.3	µs
Total phase position and phase position of front slope of control pulses is set automatically by phase comparison φ_2.					
If additional positioning is required, current can be supplied via pin 5. It then applies	$\Delta I/\Delta t$		30		µA/µs
Line flyback pulse input (pin 6)					
Input switching voltage	$V_{6\,S}$		1.4		V
Input voltage limitation	$V_{6\,B}$	−0.7		1.4	V
Input current	I_6	0.01		1	mA

For notes refer to page 110.

Characteristics (cont'd)

		min	typ	max	
Color sync signal gating pulses, positive (pin 7)					
Output voltage	$V_{q\,7}$	10	11		V_{pp}
Output resistance	$R_{q\,7}$		70		Ω
Output current during back slope	I_7		2		mA
Width of color sync signal gating pulses at $V_7 = 7$ V	t	3.7		4.3	µs
Phase position between mid sync pulses at input and front slope of color sync signal gating pulses at $V_7 = 7$ V	t_{SB}	2.45		3.15	µs
Line flyback blanking pulses, positive (pin 7)					
Output voltage	V_7	4		5	V_{pp}
Output resistance	$R_{q\,7}$		70		Ω
Output current during back slope	I_7		2		mA
Vertical sync pulses, positive (pin 8)					
Output voltage	$V_{q\,8}$	10	11		V_{pp}
Output resistance	$R_{q\,8}$		2		kΩ
Delay between front slopes of input signal and output signal	$t_{V\,an}$		15		µs
Delay between back slopes of input signal and output signal	$t_{V\,ab}$		$t_{V\,an}$		
Sync pulse separation stage (pin 9)					
Input switching voltage	$V_{i\,9S}$		0.8		V
Input switching current	$I_{i\,9S}$	5		100	µA
Input modulation current	$I_{i\,9T}$			100	µA
Input switch-off current	$I_{i\,9A}$	100	150		µA
Input leakage current $V_9 = -5$ V)	$I_{i\,9O}$			1	µA
Input signal (−BAS)	$V_{i\,9}$	3		4	V_{pp} [3])
Interference signal blanking circuit (pin 10)					
Input switching voltage	$V_{i\,10}$		1.4		V
Input switching current	$I_{i\,10S}$	100	150		µA
Input modulation current	$I_{i\,10T}$	5		100	µA
Input leakage current ($V_{10} = -5$ V)	$I_{10\,O}$			1	µA
Input signal (−BAS)	$V_{i\,10}$	3		4	V_{pp} [3])
Admissible superposed interference signal	V_{10}			7	V
Coincidence detector φ_3 (pin 11)					
Output voltage, no coincidence	$V_{q\,11}$			0.5	V
Output voltage, with coincidence	$V_{q\,11}$	5			V
Output current, no coincidence	$I_{q\,11}$		0.1		mA
Output current, with coincidence	$I_{q\,11}$		−0.5		mA

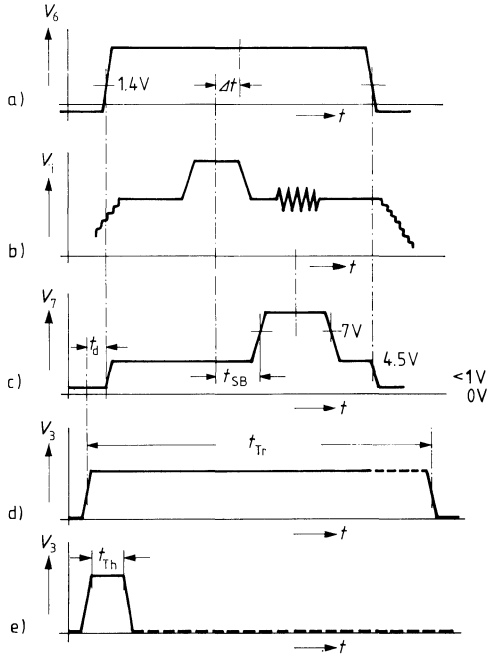
For notes refer to page 110.

Characteristics (cont'd)

		min	typ	max	
Switching to VCR operation (pin 11)					
Input voltage	$V_{i\,11}$	0		1.5	V
Input current (V_{11} = 0 V)	$I_{i\,11}$	−200			µA
or					
Input voltage	$V_{i\,11}$	9		V_1	V
Input current (V_{11} = V_1)	$I_{i\,11}$			2	mA
Time constant switching (pin 12)					
Output voltage	$V_{q\,12}$		6		V
Output current, limited to	$\pm I_{12}$		1		mA
output resistance V_{11} = 2.5 to 7 V	$R_{q\,12}$		100		Ω
Output resistance V_{11} <1.5 V/>9 V	$R_{q\,12}$		60		kΩ
Phase comparison φ_1 (pin 13)					
Control voltage range	V_{13}	3.8		8.2	V
Control current	$\pm I_{13}$		2		mA
Leakage current at V_{13} = 4 to 8 V	$I_{13\,O}$			1	µA
Output resistance V_{13} = 4 to 8 V	$R_{q\,13}$		high ohmic		[2]
Output resistance V_{13} <3.8 V/>8.2 V	$R_{q\,13}$		low ohmic		[4]
Control sensitivity	S_φ		2		kHz/µs
Catching and holding range	Δf		±780		Hz
Scattering of catching and holding range	$\Delta(\Delta f)$		±10		% [5]
Oscillator (pins 14 and 15)					
Lower threshold voltage	$V_{14\,S}$		4.4		V
Upper threshold voltage	$V_{14\,S}$		7.6		V
Reverse current	$\pm I_{14\,V}$		0.47		mA
Oscillator frequency (unsynchronized) with C_{osc} = 4.7 nF; R_{osc} = 12 kΩ	f_O		15625		Hz
Scattering of oscillator frequency	Δf_O		±5		% [5]
Frequency-adjusting level	$\Delta f_O/\Delta I_{15}$		31		Hz/µA
Adjusting range for the indicated external circuitry	Δf_O		±10		%
Dependence of the oscillator frequency on the supply voltage	$\frac{\Delta f_O/f_O}{\Delta V_1/V_1}$		±0.05		[5]
Frequency modification with supply voltage lowered to V_S = 5 V	Δf_O		±10		% [5]
Temperature coefficient of oscillator frequency	TC_f		$\pm 10^{-4}$		Hz/K [5]

[1]) Or input 4 open
[2]) Current source switching
[3]) Admissible range 1 to 7 V
[4]) Emitter follower
[5]) Scattering of external components is not considered.

Phase relations



a) Line flyback pulse

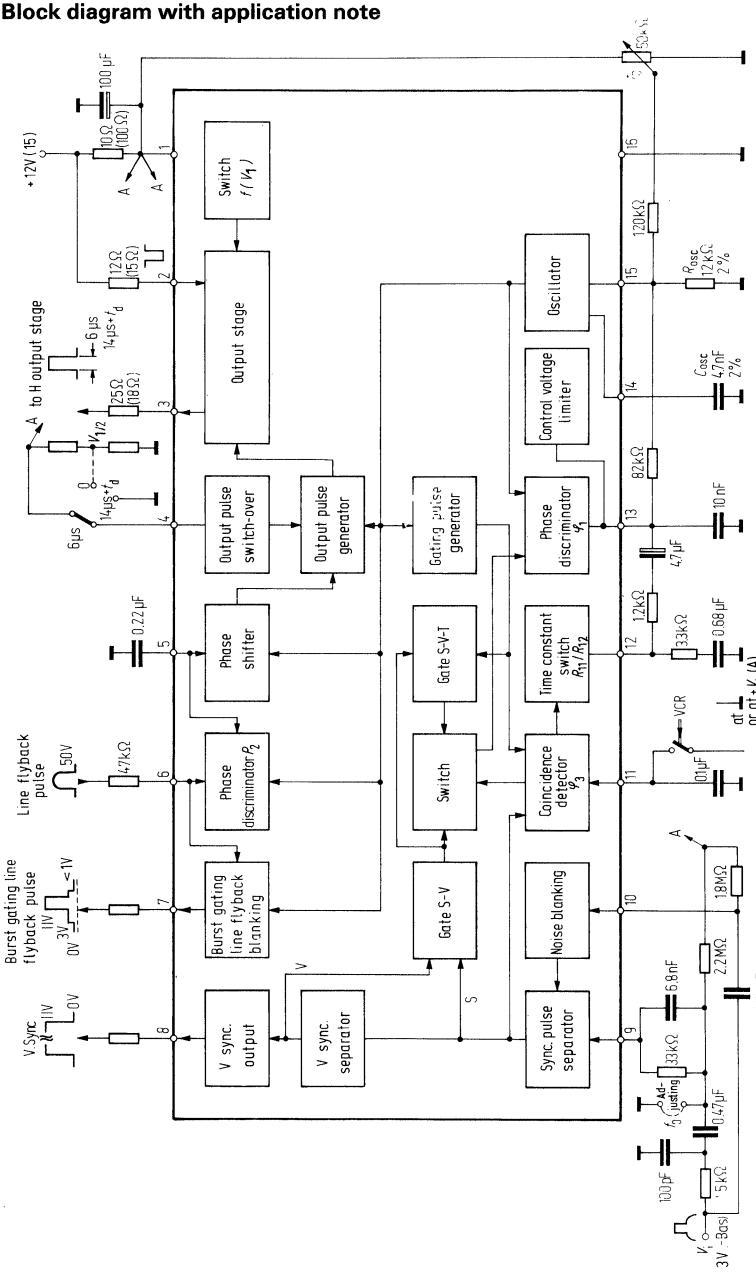
b) FBAS input signal

c) Color sync gating pulse and line flyback blanking pulse

d) Transistor output pulse ($V_4 < 3.5$ V)

e) Thyristor output pulse ($V_4 > 9.4$ V)

Block diagram with application note



Bipolar circuit

TDA 4600 has to regulate and control the switching transistor of switching power supplies. Because of its wide operational range and high voltage stability even at high load changes; this IC is used not only in TV receivers and video recorders but also in power supplies of Hifi sets and active speakers.

- Direct control of switch transistor
- Low start-up current
- Reverse-going linear overload characteristic curve
- Collector current — proportional to base-current input

Type	Ordering code	Package outline
TDA 4600	Q67000-A1451	SIP 9

Maximum ratings

Supply voltage	V_9	20	V
Voltages			
reference output	V_1	6	V
identification input	V_2	±0.6	V
controlled amplifier	V_3	3	V
collector current simulation	V_4	3	V
trigger input	V_5	3	V
base current cut-off point	V_7	6	V
base current amplifier output	V_8	6	V
Currents			
feedback, zero passage	$I_{i\,2}$	−3 to 3	mA
controlled amplifier	$I_{i\,3}$	−3	mA
collector current simulation	$I_{i\,4}$	5	mA
base current cut-off point	$I_{q\,7}$	1.5	A
base current amplifier output	$I_{q\,8}$	−1.5	A
Thermal resistance (junction-case)	$R_{th\,JC}$	15	K/W
Thermal resistance (system-air)	$R_{th\,SA}$	70	K/W
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C

Range of operation

Supply voltage range	V_9	7.6 to 15	V
Ambient temperature range	T_{amb}	0 to 70	°C

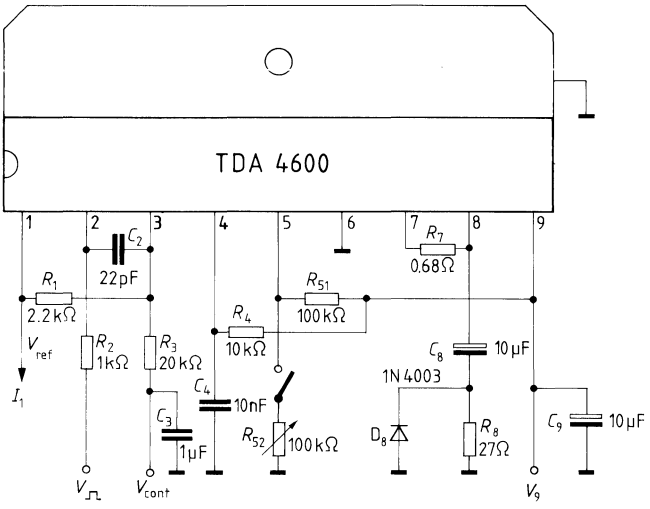
Characteristics (T_{amb} = 25 °C) according to test circuit 1 and diagram

		min	typ	max	
Start operation					
Current consumption (V_1 not yet switched on)					
V_9 = 3 V	I_9			0.5	mA
V_9 = 5 V	I_9		1.5	2	mA
V_9 = 10 V	I_9		2.4	3.2	mA
Switching point for V_1	V_9	11.3	11.8	12.3	V
Normal operation (V_9 = 10 V; V_{cont} = −10 V; V_{clock} = ±0.5 V; f = 20 kHz; duty cycle 1:1) after switch on					
Current consumption V_{cont} = −10 V	I_9	110	135	160	mA
V_{cont} = 0 V	I_9	60	85	110	mA
Reference voltage I_1 < 0.1 mA	V_1	4	4.2	4.5	V
I_1 = 5 mA	V_1	4	4.2	4.4	V
Temperature coefficient of reference voltage	TC_1		10^{-3}		1/K
Feedback voltage	V_2*		0.2		V
Control voltage	V_3	2.3	2.6	2.9	V
Collector current simulation voltage					
V_{cont} = 0 V	V_4*	1.8	2.2	2.5	V
V_{cont} = 0 V/−10V	ΔV_4*	0.3	0.4	0.5	V
Trigger input voltage	V_5	5.5	6.3	7	V
Output voltage V_{cont} = 0 V	$V_{q\,7}$*	2.8	3.3	4	V
V_{cont} = 0 V	$V_{q\,8}$*	2.8	3.4	4	V
V_{cont} = 0 V/−10 V	$\Delta V_{q\,8}$*	1.4	1.8	2.2	V
Safety operation (V_9 = 10 V; V_{cont} = −10 V; V_{clock} = ±0.5 V; f = 20 kHz; duty cycle 1:1)					
Current consumption (V_5 < 1.8 V)	I_9	14	20	26	mA
Switch-off voltage (V_5 < 1.8 V)	$V_{q\,7}$	1.3	1.5	1.8	V
	V_4	1.8	2.1	2.5	V
Ext. trigger input					
enable voltage	V_5		2.4	2.7	V
disable voltage	V_5	1.8	2.2		V
Supply voltage for V_8 blocked	V_9	6.5	7	7.6	V
Characteristics (T_{amb} = 25 °C) according to test circuit 2					
Switching time (secondary voltages)	t_{on}		350	450	ms
Voltage change					
S_3 = closed (ΔN_3 = 20 W)	ΔV_2		100	500	mV
Sound output power					
S_2 = closed (ΔN_2 = 15 W)	ΔV_2		500	1000	mV
Standby operation					
(secondary useful load = 3 W)					
S_1 = open	ΔV_2		20	30	V
	f	70	75		kHz
	$N_{primary\sim}$		10	12	VA

The cooling area has to be optimized according to the limit values (T_j, $R_{th\,SA}$, $R_{th\,JC}$, T_{amb}).

* only dc part

Test circuit 1



Circuit description

The TDA 4600 regulates, controls, and protects the switching transistor in reverse converter power supplies at starting, normal, and overload operation.

A. Starting behavior

During the start-up three consecutive operation states are passed.

1. An internal reference voltage is built up which supplies the voltage regulator and enables the supply to the coupling electrolytic capacitor and the switching transistor. Up to a supply voltage of $V_9 \approx 12$ V, the current I_9 is less than 3.2 mA.
2. Release of the internal reference voltage $V_1 = 4$ V. This voltage is abruptly available when $V_9 \approx 12$ V and enables all parts of the IC to be supplied from the control logic with a thermally stable and overload protected current supply.
3. Release of control logic. As soon as the reference voltage is available, the control logic is switched on through an additional stabilization circuit. Thus, the IC is ready for operation.

This start-up sequence is necessary to guarantee the supply through the coupling electrolytic eapacitor to the switching transistor. Correct switching of the transistor is only in this way guaranteed.

B. Normal operation

Zero crossing of the feedback coil is registered at pin 2 and passed to the control logic.

At pin 3 (regulation of input, overload, and standby recognition) the rectified amplitude variations of the feedback coil are applied. The regulating amplifier works with an input voltage of about 2 V and a current of about 1.4 mA. Together with the collector current simulation pin 4, the overload recognition defines the operating region of the regulating amplifier depending on the internal reference voltage. The simulation of the collector current is generated by an external RC network at pin 4 and an internally set voltage level. By increasing the capacitance (10 nF) the max. collector current of the switching transistor rises, thus setting the required operating range. The extent of the regulation lies between a 2 V clamped dc voltage and an ac voltage rising in a sawtooth waveform, which may vary up to a maximum amplitude of 4 V (reference voltage).

A reduction of the secondary load down to 20 watts causes the switching frequency to rise to about 50 kHz at an almost constant pulse duty factor (period to on-time approx. 3). A further reduction of the secondary load down to about 1 watt results in changing the switching frequency to approx 70 kHz, and additionally the pulse duty factor rises to approx. 11. At the same time the collector peak current falls below 1 A.

In the trigger the output level of the regulating amplifier, the overload recognition, and the collector current simulation are compared and instructions are given to the control logic. There is an additional triggering and blocking possibility by means of pin 5. The output at pin 8 is blocked at a voltage of less than 2.2 V at pin 5.

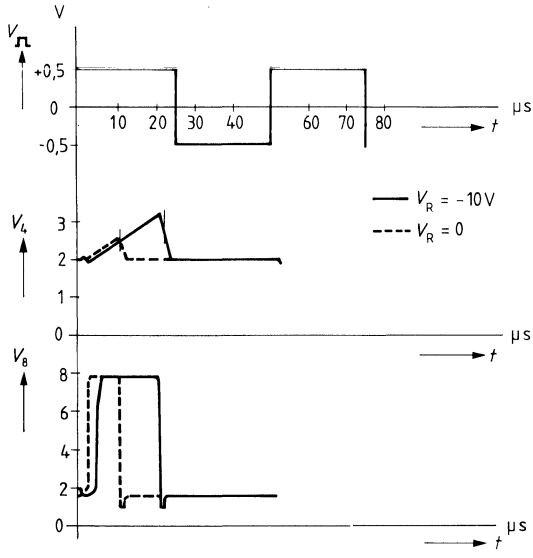
Depending on the start-up circuit, the zero crossing identification, and the release with the aid of the trigger, the control logic flip flops are set which control the base current amplifier and the base current shut-down. The base current amplifier moves the sawtooth voltage V_4 to pin 8. A current feedback having an external resistance of $R \approx 0.68\,\Omega$ is inserted between pin 8 and pin 7. The resistance value determines the maximum amplitude of the base driving current for the switching transistor.

C. Protective measures

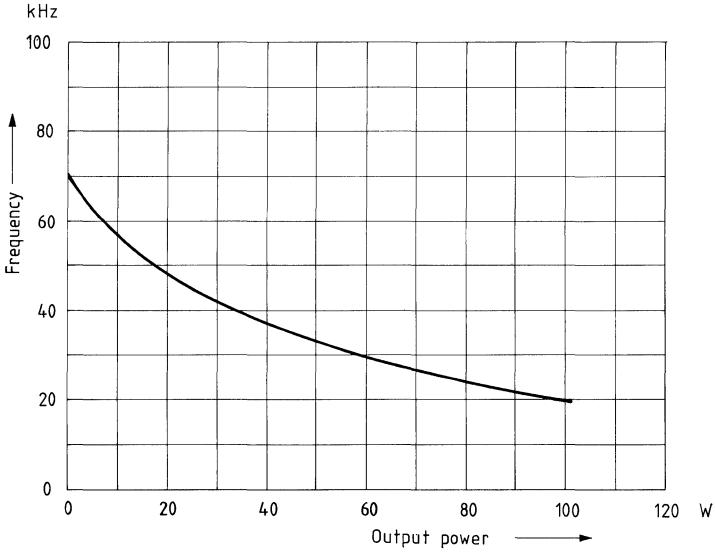
The base current shut-down, released by the control logic, clamps the output of pin 7 at 1.6 V and thus blocks driving of the switching transistor. This protective measure will be released if the voltage at pin 9 reaches a value of less than 7 V or if voltages of less than 2.2 V occur at pin 5. In the case of a short circuit of the secondary windings of the P.S.U., the IC continuously monitors the fault condition.

With the load completely removed from the secondary winding of the P.S.U., the IC is set to a large pulse duty factor. The total power consumption of the P.S.U. is held below $n =$ 6 to 10 watts in both operating conditions. After having blocked the output, caused at a supply voltage V_9 of 7 V, a further voltage reduction to 6 V results in switching off the reference voltage (4 V).

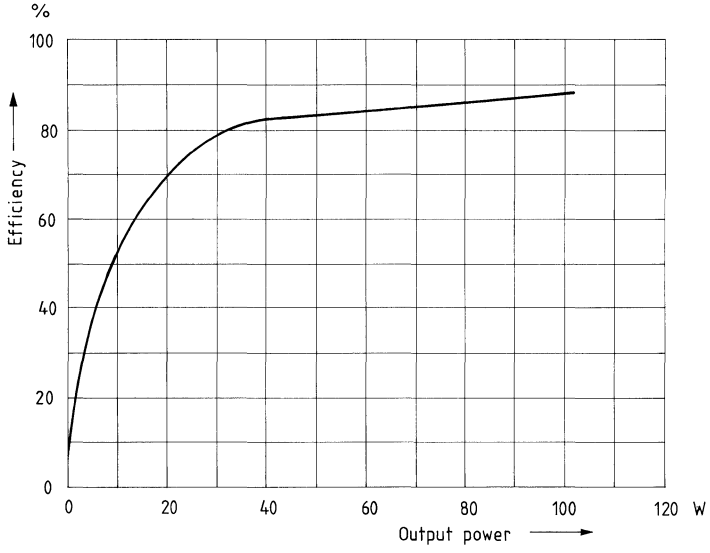
Test diagram: Normal operation



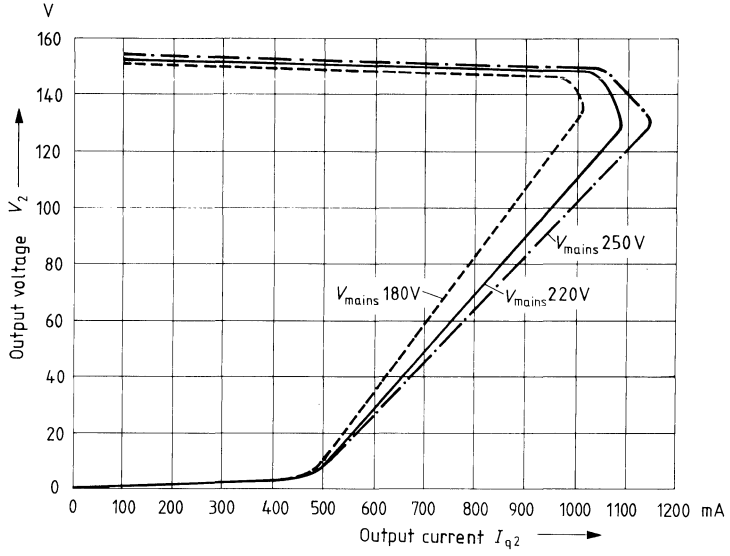
Frequency versus output power



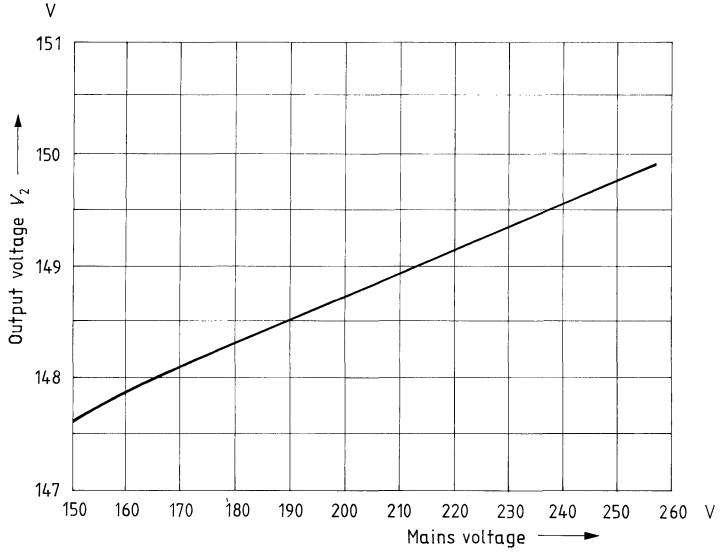
Efficiency versus output power



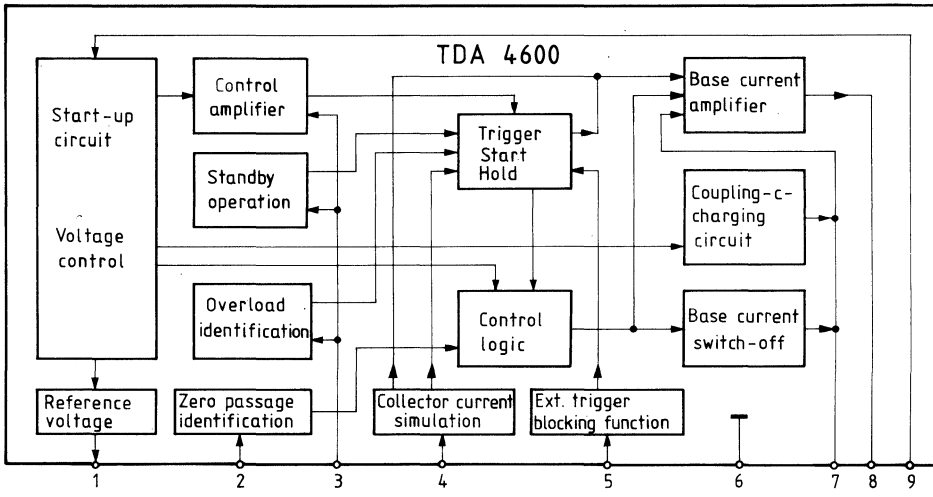
Load characteristics $V_2 = f(I_{q2})$



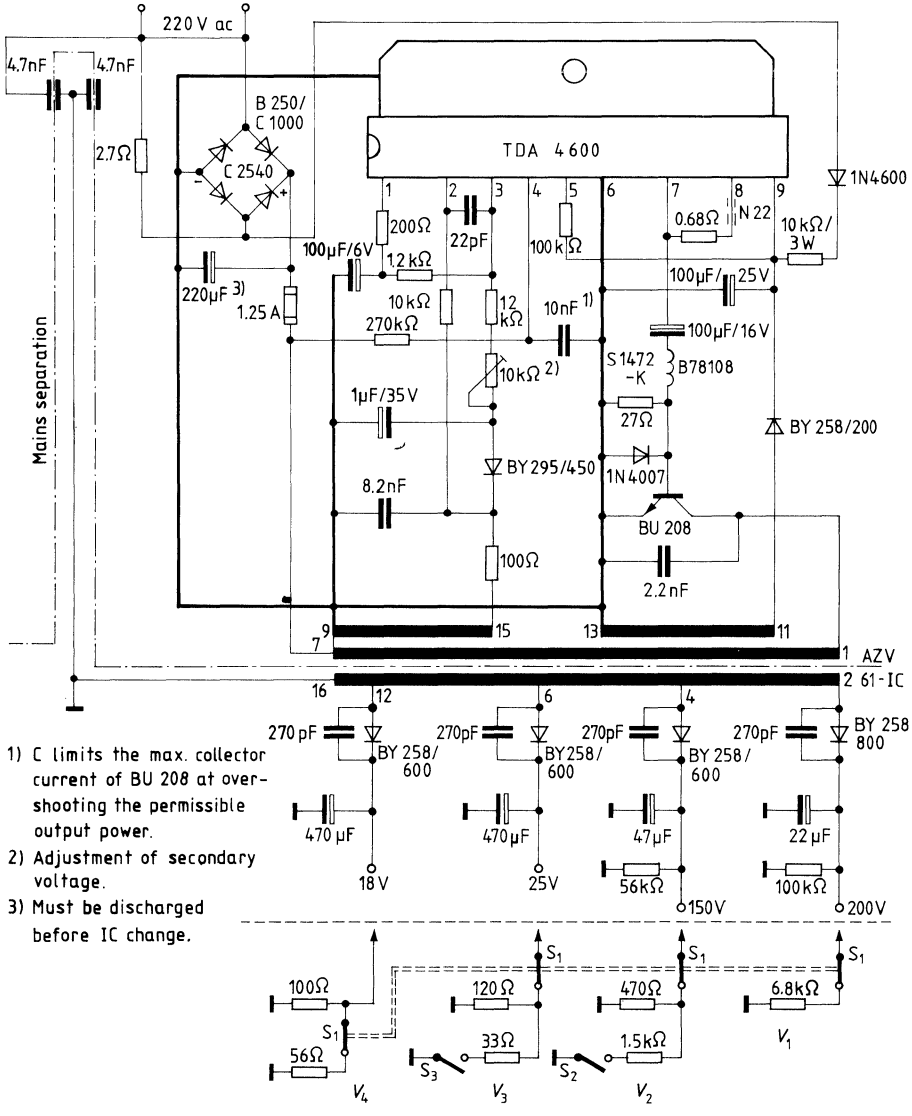
Output voltage V_2 (mains change)



Block diagram



Test circuit 2 and application circuit



1) C limits the max. collector current of BU 208 at overshooting the permissible output power.
2) Adjustment of secondary voltage.
3) Must be discharged before IC change.

Bipolar circuit

The TDA 4610 is used for pin cushion correction in color TV sets. Moreover, the circuit offers the possibility of performing trapezoidal corrections as well as setting the picture width and the degree of the pin cushion correction. By making use of the switching operation, the diode modulation is controlled directly, thus resulting in very low power dissipation.

- Low power dissipation
- Wide regulating range
- Simple tuning
- Few external components

Type	Ordering code	Package outline
TDA 4610	Q67000-A1523	SIP 9

Maximum ratings

Operating voltage	V_{S1}	36	V
Voltages			
Vertical input	V_7	V_{S1}	V
Parabola position	V_6	V_{S1}	V
Correction of parabola error	V_8	5	V
Correction onset	V_9	5	V
Flyback	V_4	42	V
Horizontal picture width	V_3	V_{S1}	V
Final stage output	V_{K2}	42	V
Current			
Final stage output	I_2	1.5	A
Thermal resistance (junction-case)	$R_{th\,JC}$	12	K/W
Thermal resistance (system-air)	$R_{th\,SA}$	70	K/W
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C

Range of operation

Supply voltage range	V_{S1}	12 to 36	V
Ambient temperature range	T_{amb}	0 to 70	°C

1. Characteristics (V_{S1} = 24 V; T_{amb} = 25 °C)

		min	typ	max	
Current consumption	I_5		10	12	mA
input current verticai	$-I_7$		100		µA
Input current parabola position	$-I_6$		100		µA
No load voltage parabola position	V_8		0.7		V
Input current	$-I_8$		0.4		mA
No load voltage correction onset	V_9		3.6		V
Input current correction onset	$-I_9$		0.4		mA
Input current picture width	I_3		0.2		mA
Saturation voltage final stage (I_2 = 1 A)	V_2		2	2.5	V

2. Characteristics (V_{K2} = 40 V; T_{amb} = 25 °C)

Parabola position with R_6 (diagram 1)		±10			%
Parabola correction					
Onset point with R_9 (diagram 2)		75			%
Permissible deviation referred to onset point (diagram 2)				10	%
Intensity of parabola correction with R_8					
Increase of the parabola when adjustable to 0					
Parabola amplitude with R_4	V_{PA}	5		20	V_{pp}
Useful voltage range of the parabola (parabola amplitude V_{PA} = 5 V_{pp})	V_P	2		40	V

Circuit description

The vertical sawtooth voltage (2 V_{pp} increasing from 0, flyback time <0.1 msec) is applied to two differential amplifiers.

Antiphase signals are available at the outputs of the differential amplifiers. Differential amplifier 1 controls the multiplexer which converts the sawtooth signal into a symmetrical parabola.

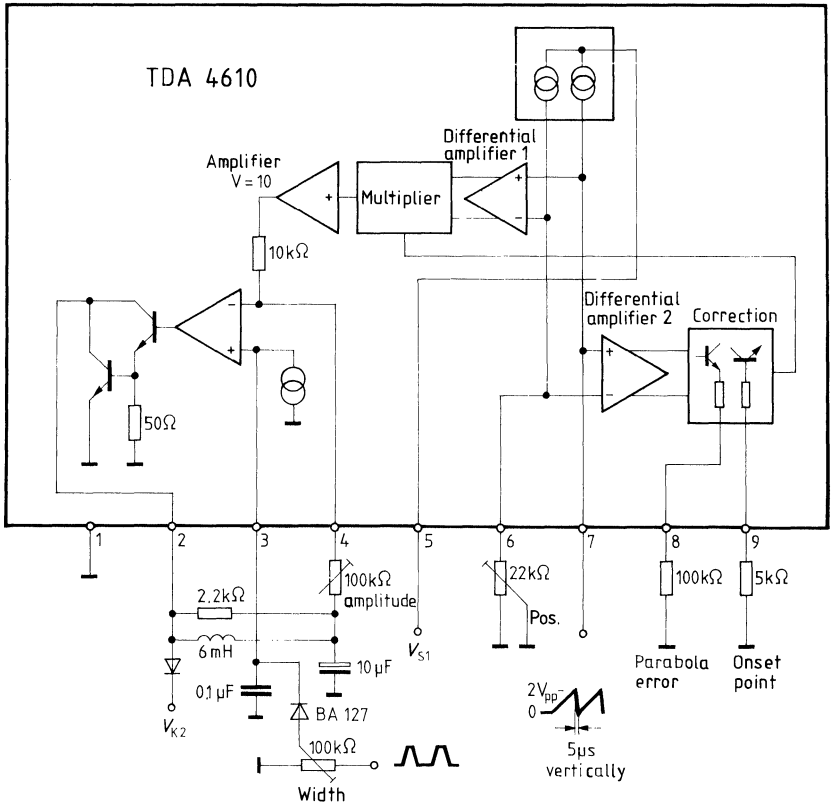
The differential amplifier 2 controls a correction voltage circuit by which the shape of the parabola can be suited to the characteristics of the tube.

The parabola signal is amplified and fed to the pulse width modulator. The modulator controls the final output transistor.

Pin designation

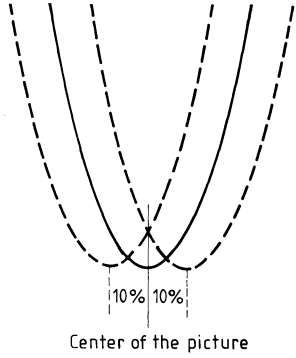
Pin No.	Description
1	Ground
2	Final stage output
3	Horizontal picture width
4	Flyback
5	Supply voltage
6	Parabola position adjustment
7	Vertical input
8	Correction of parabola error
9	Adjustment of onset point

Block diagram and test circuit

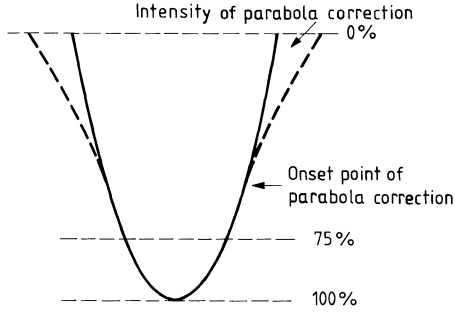


Pulse diagram 1 and 2

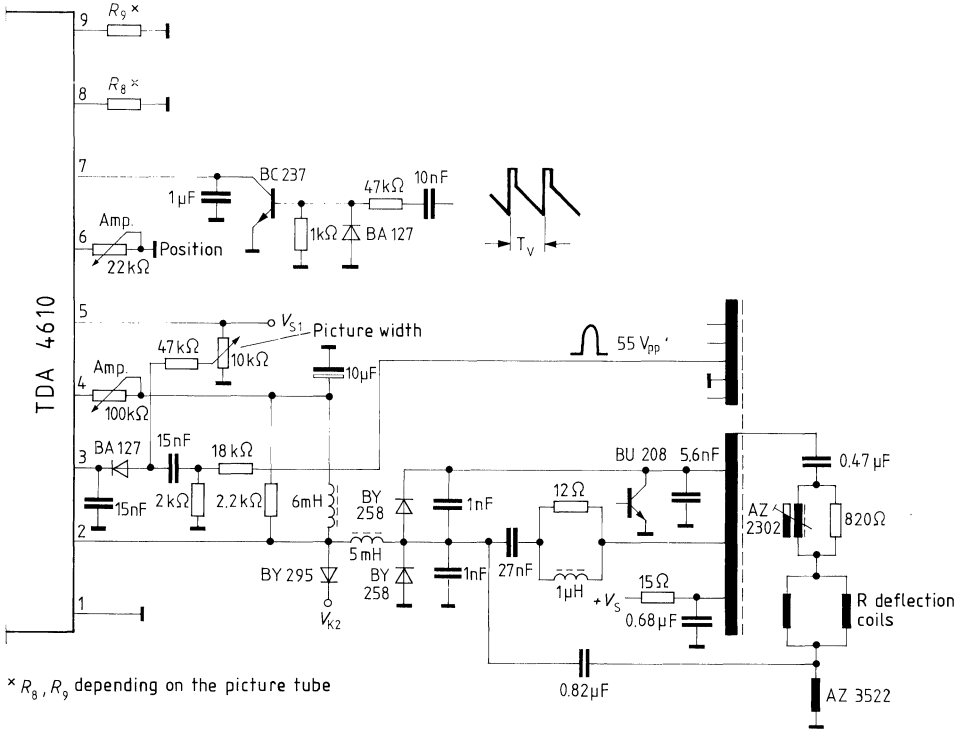
Parabola position



Parabola correction



Application circuit



× R_8, R_9 depending on the picture tube

IC for Onscreening of the Bargraph in the Television Picture

UAA 190

Bipolar circuit

The IC UAA 190 generates a bar which corresponds to the tuning frequency and can be displayed in the TV picture during tuning.

- Few external components
- Low power consumption
- Straightforward driving of the RGB stage

Type	Ordering code	Package outline
UAA 190	Q67000-A1282	DIP 8

Maximum ratings

Supply voltage	V_6	18	V
Output current	I_4	35	mA
Thermal resistance (system-air)	$R_{th\ SA}$	120	K/W
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C

Range of operation

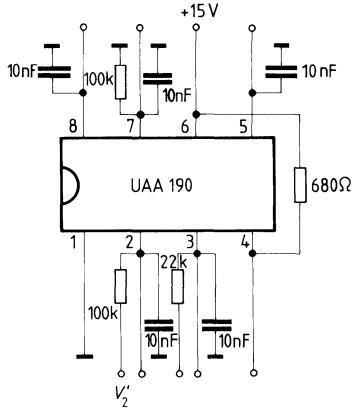
Supply voltage range	V_6	12 to 18	V
Ambient temperature range	T_{amb}	0 to 70	°C

Characteristics (V_6 = 15 V; T_{amb} = 25 °C)

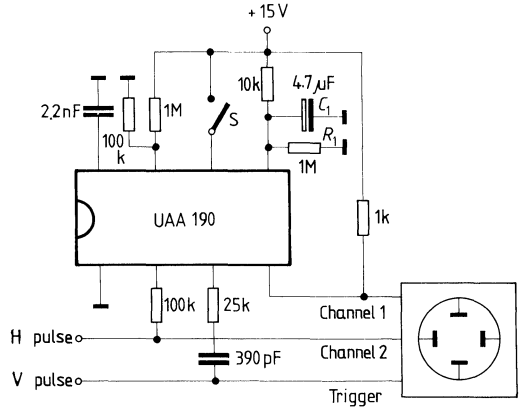
		min	typ	max	
Current consumption					
$V_5 \leqq 1$ V	I_6	1		4	mA
$V_5 \geqq 2.5$ V	I_6	8		35	mA
Line input current (V_2 = 0)	$-I_2$	50		400	µA
Line pulse current (R_v = 100 kΩ)					
V_2 = 0 V	$-I_2$		10		µA
V_2 = −55 V	$-I_2$		500		µA
Line pulse width	T_2	4			µA
Picture input current (V_3 = 0 V)	$-I_3$	75		250	µA
Picture pulse current	$-I_3$	250			µA
(V_3 = −10 V; R_v = 22 kΩ)					
Output voltage (I_4 = 20 mA)	V_{4L}[1])		0.4	1.5	V
	V_{4H}			V_6	V
Output current	I_{4L}[1])		15	20	mA
(V_{4H} = V_6)	I_{4H}			10	µA
Switching threshold search pulse	V_5	1		2.5	V
Input current V_5 = 8 V	I_5		1		mA
V_5 = 6 V	I_5			5	µA
V_5 = 0 V	$-I_5$			0.5	µA
Input resistance ($V_5 \leqq 6$ V)	R_{i5}	1	2		MΩ
Perm. comp. input voltage	V_7	0		V_6-2	V
Comparator input voltage	V_7			0.3	V
(on R_v = 100 kΩ)					
Comparator input voltage					
I_8 = 10 mA; $-I_2 \geqq 400$ µA	V_8			1	V
I_8 = 2 mA; $-I_2 \geqq 400$ µA	V_8			0.2	V
$-I_2 \leqq 50$ µA	V_8	V_6-2			V
Comparator current					
$-I_2 \geqq 400$ µA	I_8			15	mA
$-I_2 \leqq 50$ µA; V_8 = 0 V	I_8	115	145	175	µA
Internal comparator bias	V_v	0.3		0.6	V

[1]) V_{4L} and I_{4L} may only be measured during lines 88 to 95
Index L = Low
Index H = High

Measuring circuit for static measurements



Measuring circuit for dynamic measurements



1. S off: no onscreening
2. S on : onscreening line 88 to 95
3. S off: onscreening time according to C_1 and R_1 (for 4.7 µF and 1 MΩ approx. 5 sec)

Description of functions and circuit

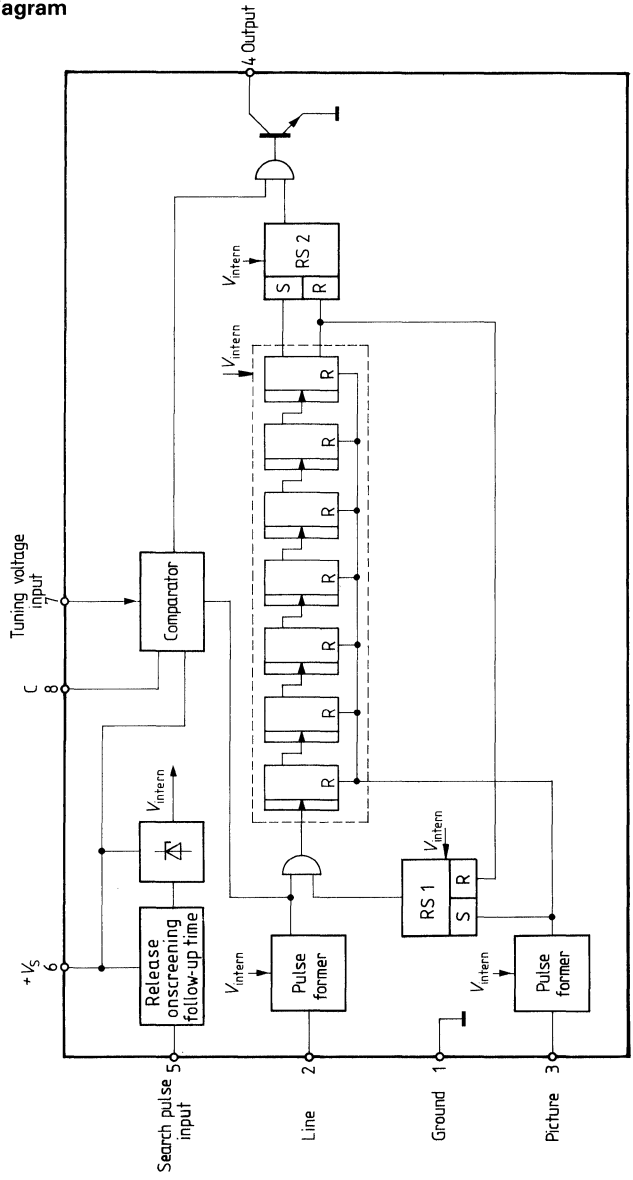
With the aid of the UAA 190 the tuning voltage can be displayed in form of a bar into the TV picture during channel selection. For that purpose 8 pulses are delivered during each picture sweep whereby the duration of the pulses depends on the tuning voltage. These pulses can be used for bright and dark blanking for control of the color picture cathodes.

It is the transmitter station search signal V_5 2.5 V which makes the circuit ready for operation since the internal voltage regulator only then provides the supply voltage regulated to 6 V.

Position and width of the bar onscreening is determined by a 7-bit counter, the length, however, by a voltage comparator. The counter is reset by the vertical pulse to the initial position at line 0. For the first picture sweep after switching on, the counter position is undefined. The output for lines 88 to 95 is enabled by the counter. The output is driven by the comparator as soon as the capacitor voltage V_8 (see application circuit) is lower than the voltage V_7. The indication for $V_7 = 0$ V is made possible by an internal bias which is added to the externally applied voltages. During the line pulse the capacitor is discharged and subsequently loaded with a constant current of typically 145 µA (see Fig. 1).

The length of the bar onscreening is determined by the following magnitudes: tuning voltage, shunt resistor and dividing ratio of the input divider, input current of the tuning voltage input, internal bias, capacitance of the load capacitor and load current.

Block diagram



Pulse diagram

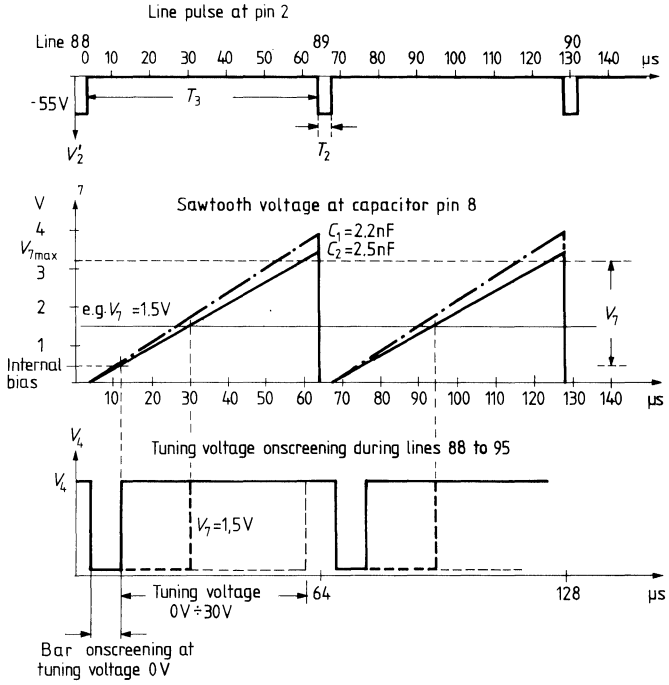


Figure 1

Pulse diagram

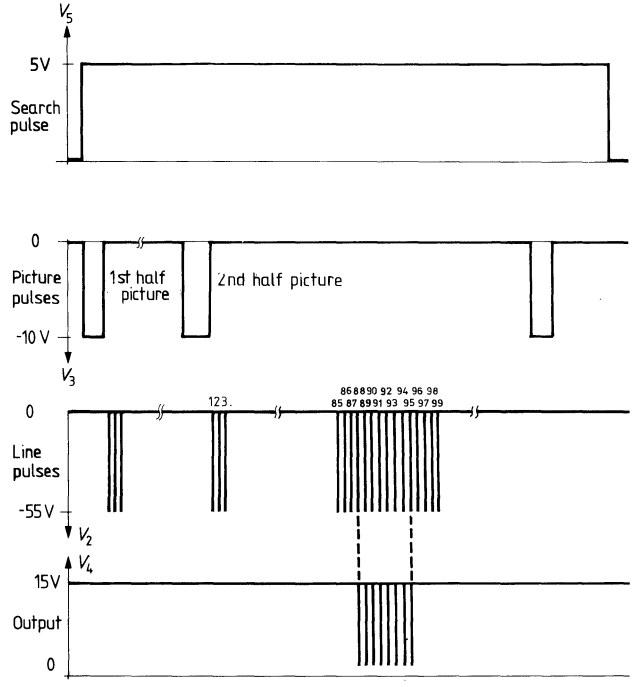
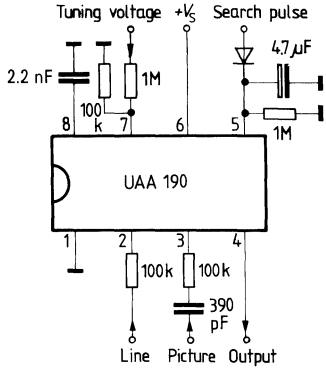


Figure 2

Application circuit



Bipolar circuit

Fast ECL prescaler with a divider ratio 1:256 for input frequencies of 80 MHz up to 1 GHz. Particularly suitable for use in TV sets with frequency synthesis.

- Input frequency up to 1 GHz
- Few external components
- Separate inputs for UHF and VHF

Type	Ordering code	Package outline
SDA 4040	Q67000-A1462	DIP 14

Maximum ratings

Supply voltage	V_1, V_2	10	V
Input voltages	V_8	2.5	V_{pp}
	V_{10}	2.5	V_{pp}
Switching voltage	V_{14}	−0.5 to 7.2	V
Switching current	I_{14}	−10	mA
Output current	I_{q4}	−30 to 30	mA
Thermal resistance (system-air)	$R_{th\ SA}$	80	K/W
Storage temperature range	T_{stg}	−40 to 125	°C
Junction temperature	T_j	125	°C

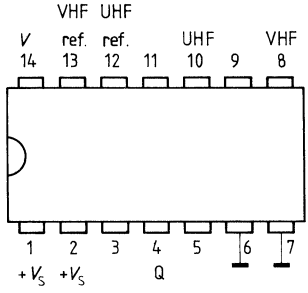
Range of operation

Supply voltage range	V_1, V_2	6.45 to 7.15	V
Input frequency range VHF	$f_{i\,8}$	80 to 300	MHz
UHF	$f_{i\,10}$	80 to 950	MHz
Ambient temperature range	T_{amb}	0 to 65	°C

Characteristics (V_S = 6.8 V; T_{amb} = 25 °C)

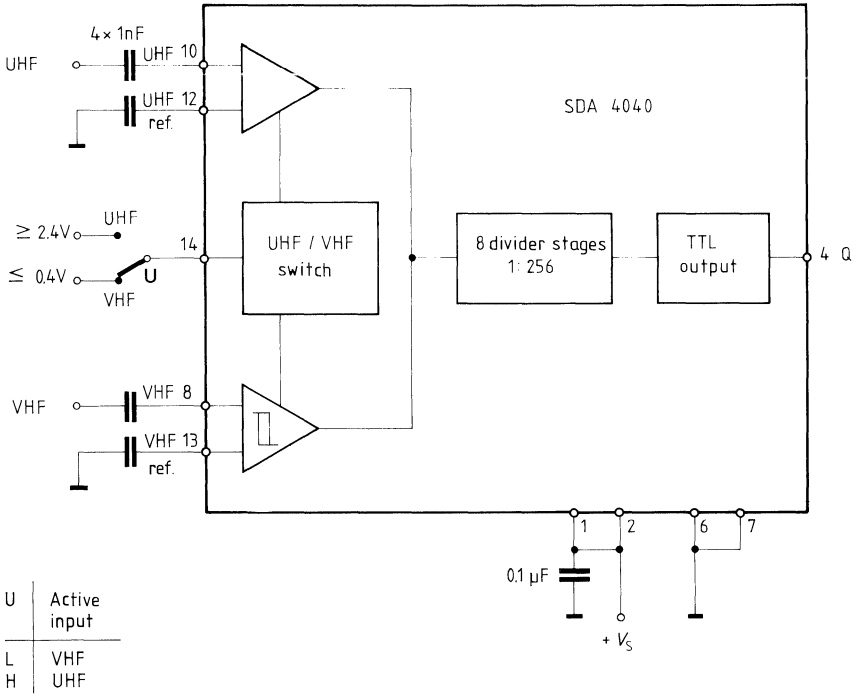
		min	typ	max	
Current consumption (V_S = 7.15 V)	I_1, I_2		70	95	mA
Input voltages VHF (sine) [1])					
f_i = 80 MHz	V_8	200		700	mV_{rms}
f_i = 100 MHz	V_8	100		700	mV_{rms}
f_i = 300 MHz	V_8	100		700	mV_{rms}
Input voltages UHF (sine) [1])					
f_i = 80 MHz	V_{10}	300		700	mV_{rms}
f_i = 100 MHz	V_{10}	250		700	mV_{rms}
f_i = 200 MHz	V_{10}	150		700	mV_{rms}
f_i = 450 MHz	V_{10}	100		700	mV_{rms}
f_i = 900 MHz	V_{10}	200		700	mV_{rms}
L switching voltage	$V_{14\,L}$			0.4	V
H switching voltage	$V_{14\,H}$	2.4			V
Switching current (V_{14} = 0.4 V)	$-I_{14}$			0.8	mA
L output voltage ($I_{q\,L}$ = 5 mA)	$V_{q\,L4}$			0.4	V
H output voltage ($I_{q\,H}$ = −1 mA)	$V_{q\,H4}$	2.4	3.5		V

Pin configuration (top view)



1) For deviating ambient temperatures the input sensitivity may decrease down to 20%.

Block diagram and application circuit

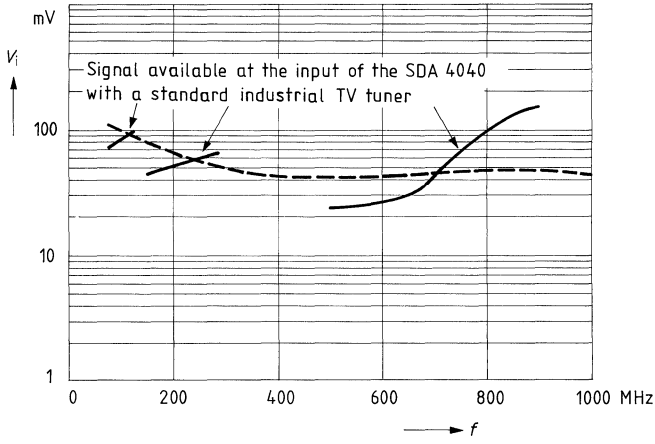


If needed hysteresis can be achieved at the UHF input by connecting a resistor (e. g. 33 kΩ) between UHF_{ref} (pin 12) and ground (pins 6, 7). At the VHF input the hysteresis can be increased in the same way.

Circuit description

The IC SDA 4040 has a VHF and a UHF input. The VHF input is activated by applying a "Low" to the switching input U. The UHF input is activated by applying a "High" to pin U. The VHF input has a hysteresis of approx. 50 mV which improves the switching behavior at sine wave input signals of low frequencies. If necessary a hysteresis can be applied to the UHF input by means of an external resistor matrix.
The connection of the input signal to the VHF or UHF input is done capacitively. The inputs are internally terminated with approx. 400 Ω. The pins VHF_{ref} and UHF_{ref} have to be grounded via capacitors (see application diagram).

Input sensitivity versus frequency



Bipolar circuit

The SDA 4041 is derived from the SDA 4040. It comprises two input amplifiers independent from each other as well as an 8-stage divider. This IC is particularly suitable for use in TV sets with frequency synthesis.

- Input frequency up to 1 GHZ
- Few external components
- Separated inputs for UHF and VHF
- ECL outputs

Type	Ordering code	Package outline
SDA 4041	Q67000-A1463	DIP 18

Maximum ratings

Supply voltage	V_S	6	V
Input voltages	V_4	2.5	V_{pp}
	V_5	2.5	V_{pp}
Switching voltage	V_2	−0.5 to 20	V
Switching current	$-I_2$	10	mA
Thermal resistance (system-air)	$R_{th\,SA}$	65	K/W
(system-case)	$R_{th\,SC}$	20	K/W
Storage temperature range	T_{stg}	−40 to 125	°C
Junction temperature	T_j	125	°C

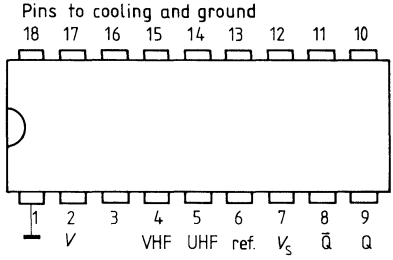
Range of operation

Supply voltage range	V_S	4.7 to 5.5	V
Input frequency range VHF	$f_{i\,4}$	80 to 300	MHz
UHF	$f_{i\,5}$	80 to 950	MHz
Ambient temperature range	T_{amb}	0 to 70	°C

Characteristics (V_S = 5 V; T_{amb} = 25 °C)

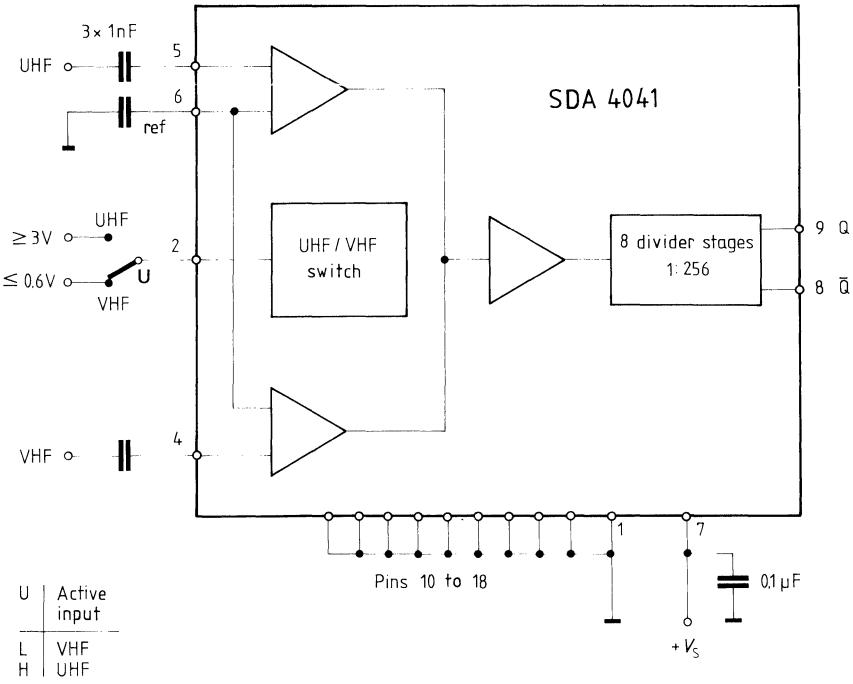
		min	typ	max	
Current consumption	I_7		95	130	mA
Input voltages VHF (sine)[1]					
f_i = 80 MHz	V_4	40		500	mV_{rms}
f_i = 100 MHz	V_4	30		500	mV_{rms}
f_i = 300 MHz	V_4	20		500	mV_{rms}
Input voltages UHF (sine)[1]					
f_i = 80 MHz	V_5	40		500	mV_{rms}
f_i = 100 MHz	V_5	30		500	mV_{rms}
f_i = 300 MHz	V_5	20		500	mV_{rms}
f_i = 450 MHz	V_5	20		500	mV_{rms}
f_i = 900 MHz	V_5	40		300	mV_{rms}
L switching voltage	V_{2L}			0.6	V
H switching voltage	V_{2H}	3			V
Switching current (V_2 = 12 V)	$-I_2$		1.5		mA
Output voltages	V_{q8}, V_{q9}	0.75	1		V_{pp}
Output resistance	R_{q8}, R_{q9}		250		Ω

Pin configuration (top view)



1) For deviating ambient temperatures the input sensitivity may decrease down to 20%.

Block diagram and application circuit



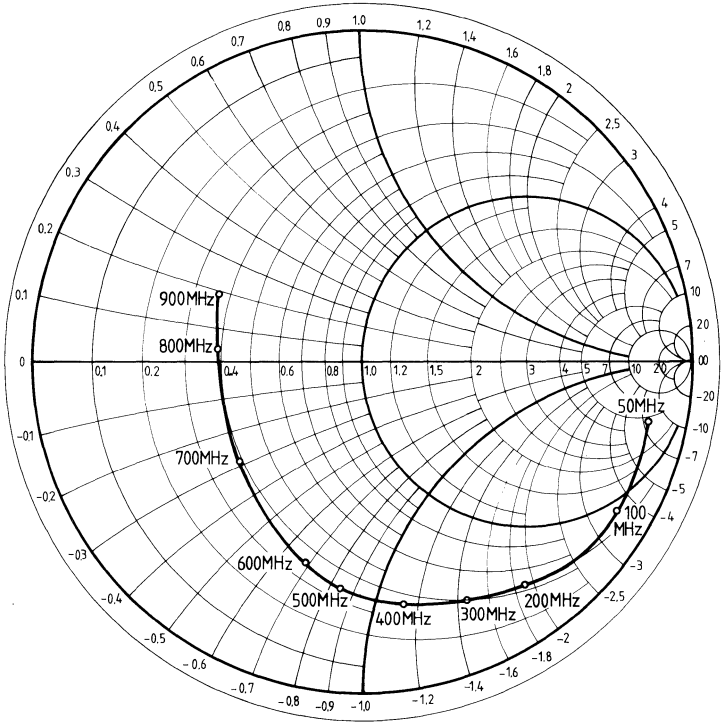
Pins 10 to 18 are internally interconnected by means of a metal web, they are also connected to the chip body. They are intended for cooling and ground connection.

Circuit description

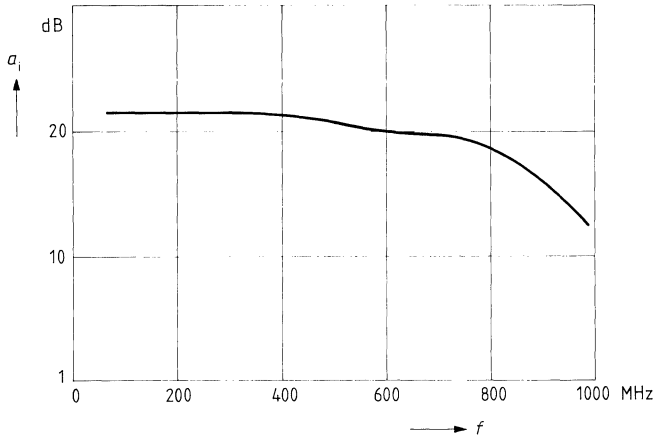
The IC SDA 4041 has a VHF and a UHF input. The VHF input is activated by applying a "Low" to the switching input U. The UHF input is activated by applying a "High" to pin U.

The connection of the input signal to the VHF or UHF input is done capacitively.
The connection ref has to be grounded. Preamplifiers at the inputs provide for a high input sensitivity.
The outputs are in phase opposition and deliver ECL level.

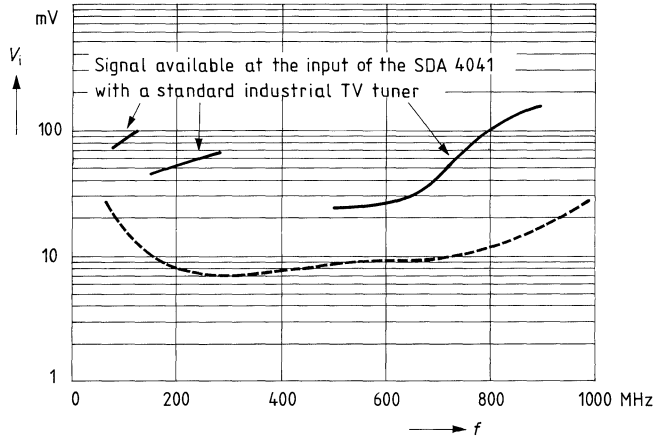
Input reflection factor
for determining the input impedance for the VHF as well as UHF input
$Z_0 = 75\ \Omega$



Decoupling of the VHF and UHF input versus input frequency $\alpha_i = f(f)$



Input sensitivity versus input frequency $V_i = f(f)$



Design ideas

As a result of technological advance: High speed dividers in ECL technology allow digital handling of the oscillator frequency of TV tuners up to one GHz. Together with a programmable divider and a phase locked loop (PLL) the oscillator can be connected digitally and in a phase locked way to a quartz stabilized reference frequency, thus providing the prerequisite for a tuning system that is able to store an initially programmed channel unvaried with a precision so far reserved to professional devices, only.

Whereas TV sets, which are voltage tuned, need time and temperature stability of reference voltage, tuning potentiometer and/or D/A converter, varicap diode, oscillator transistor, oscillating inductance and some other components, tuning by frequency synthesis is only determined by the quartz oscillator and a programmed digital divider stage.

It is the inital start-up procedure of the TV set, at which the station buttons are set with the appropriate channels, e.g. channel 10 (first program) assigned to sensor 1, channel 35 (second program) to sensor 2, channel 56 (third program) to sensor 3, channel 8 (Austria 1) to sensor 4, etc.

Performance of this assignment shall be safe and simple since it is done only once for a period of several years.

It is, therefore, of great interest not only for TV set owners but also for merchants to keep programming of these station buttons unchanged for years. It is the Siemens channel program system, which optimally meets this requirement.

With the aid of two keys or by means of channel selection the channels Nos. 00 to 99 can be set within a few seconds, only. For the CCIR channels 02 to 12 and 21 to 68, these are identical with the numbers indicated unless converted in a GA system. With the indication 81 to 00, the cable channels S1 to S20 may be called provided that tuner facilities are available. 13 to 20 are reserved to the Italian channels A to H and the remaining gaps are occupied with some OIR channels as well as other expected to be important in the near future. Selection of station button and desired channel provides in most cases optimal setting of the station and can be stored.

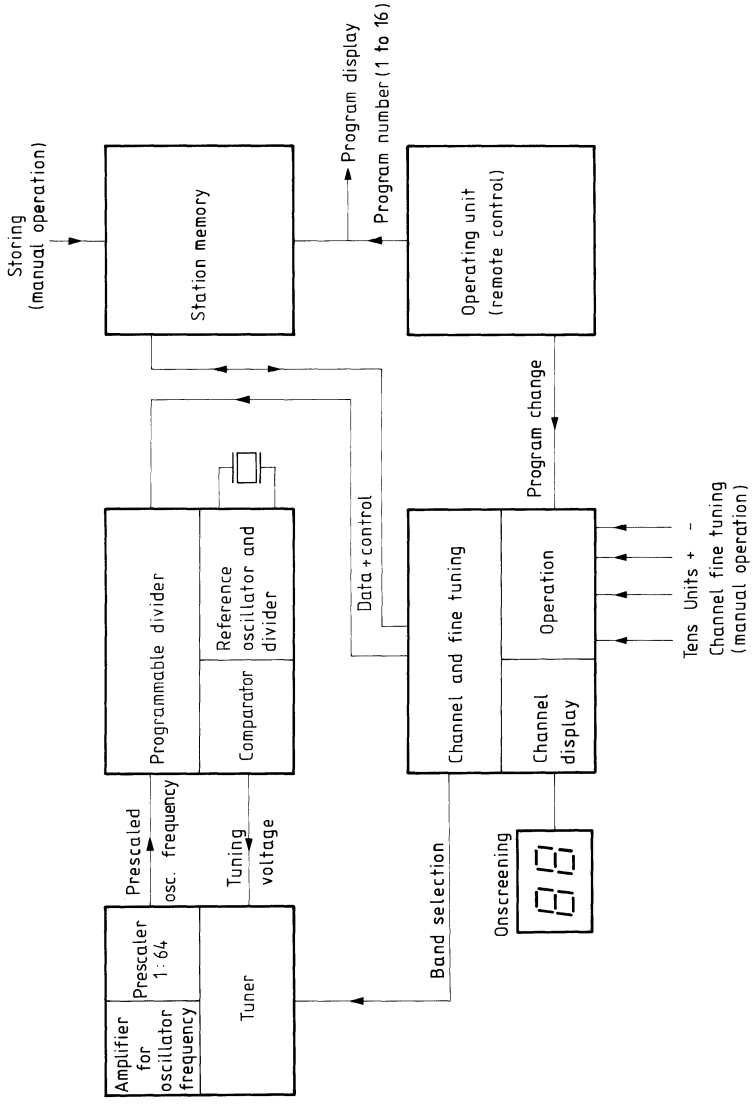
Programming can also be done when no transmission takes place or when reception is not yet possible due to a missing antenna.

Direct channel selection is particularly useful when many transmitters can be received. The correct channel and the nearest transmitter can be identified unambiguously.

In case of inadequate receiving conditions or unfavorable frequency responses, the visual impression can be improved by fine detuning. In foreign countries, such as Belgium, the Netherlands, Luxembourg and Switzerland, some TV cable networks are admitted to have slight deviations from the standardized channel raster in order to avoid interference. Subsequent fine tuning is also necessary, performed in steps of 125 kHz, and stored, too. The remaining deviation of ± 62.5 kHz from the theoretically ideal tuning is not noticeable even in case of critical observation and is lower than those tolerances caused by the IF amplifier.

An AFC could be coupled — if required — to the fine tuning unit which would automatically provide at offset channel raster for fine tuning in antenna installations. Visual correction at unfavorable receiving conditions, however, cannot be performed by the AFC. Moreover, it is well-known that an AFC tends to mismatching in case of noisy signals and at certain picture contents. Expensive peripheral circuitry is necessary if trapping of incorrect carrier signals shall to some degree be reliably eliminated. In accordance with the present state of the art, the teletext reception is only to be obtained with tuning systems of high precesion, this is however, scarcely possible by means of AFC.

Frequency synthesis for TV sets



Description of the system

A digital tuning system essentially consists of 3 blocks.

Frequency synthesis
Controller and display
Station memory

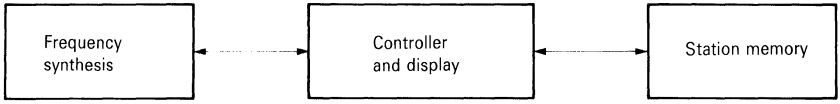


Fig. 1

Frequency synthesis

The desired frequencies are generated according to the PLL principle (Fig. 2). The PLL comprises a VCO (the equivalent tuner oscillator), a prescaler with fixed divider factor P, a divider with digitally selectable divider factor N, a phase detector, and an integrator. The reference frequency for the phase detector can be obtained from a crystal oscillator with following divider (divider factor Q).

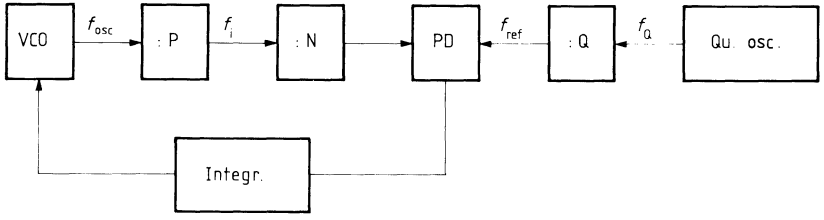


Fig. 2

The selection of the parameter is as follows:

1. VCO frequency range $f_{osc.\ min}$, $f_{osc.\ max}$
2. Necessary frequency raster Δf
3. Max. permissible tuning time and noise phase shift

In TV applications a frequency raster of $\Delta f = 125$ kHz is sufficient. Therefore it follows that

$N_{min} = \frac{f_{osc.\ min}}{\Delta f}$ and $N_{max} = \frac{f_{osc.\ max}}{\Delta f}$.

Hence a 13 bit programmable divider N = 2.....8191 is required. The reference frequency f_{ref} decisively determines the tuning time and the noise phase shift of the oscillator. It results from the frequency raster Δf and the prescaler factor P: $f_{ref} = \frac{\Delta f}{P}$.

On the other hand, the prescaler factor P determines the max. input frequency for the programmable divider $f_{imax} = \frac{f_{osc.\ max}}{P}$.

The reference frequency f_{ref} is obtained from oscillator $f_{ref} = \frac{f_Q}{Q}$.

Hence, it follows: $f_{osc} = \frac{PN}{Q} \cdot f_Q$

In the given system P = 64, Q = 2048, and $f_Q = 4.0$ MHz have been determined. The reference frequency thus results in: $f_{ref} = \frac{\Delta f}{P} = \frac{f_Q}{Q} = 1.953125$ kHz.

1. The **prescaler S 0436** is an ECL divider with a fixed divider factor P = 64. The max. input frequency is 1 GHz. In order to ensure reliable operation, the sinusiodal input voltage covering the frequency range between 60 and 1000 MHz should be greater than 200 mV_{rms}. In order to avoid reactions on the tuning oscillator, a broadband preamplifier of approx. 20 dB voltage amplification becomes necessary. The push-pull outputs result in a good noise immunity against cross talking. The output levels of 1 V_{pp} only cause slight noise radiation.
2. The **PLL IC S 0437** includes a 13-bit binary programmable synchronous divider (max. input frequency $f_{imax} = 15$ MHz), a digital phase detector with push-pull current output, a quartz oscillator ($f_{osc} = 4$ MHz) with subsequent divider (divider factor Q = 2048). Input of dividing factor N is done serially by means of a 13-bit shift register. The shift clock is derived from the crystal divider and is available at a collector output. The repetition time of the clock CL is 16 µsec, the H pulse duration is 4 µsec. Acceptance of the information takes place at the leading edge of the pulse. Moreover, a synchronous pulse SYC with 512 µsec repetition time and 8 µsec H pulse duration is delivered. The enable input PLE is only allowed to be high during the phase of the synchronous pulse. At too high input frequency the push-pull current output acts as **current source** and supplies current pulses of 100 μA_{pp}, at too low input frequency as **current lowering.** At correct input frequency the push-pull current output becomes **high-ohmic.**
   In the case of tuning voltages $V_{tun} \leq 12.5$ V, the output can be directly connected to an integrating network. At higher tuning voltages an external operational amplifier is necessary. The sign of the phase pulses can be switched over with the aid of the PD

REF terminal. In the latching state of the PLL, L-level appears at the LOCK indication, in the non-latching case the output pulses.

3. The TBB 1331 integrator is needed for tuning voltages $V_{tun} > 12.5$ V. With the aid of an integrating circuit the tuning voltage can be varied between 0.5 V and 30 V. The PD REF terminal supplies the reference voltage for the non-inverted input of the op amp.

Flow of control and display

1. **The SM 564 controller**
   The integrated MOS circuit, part of the frequency synthesis tuning system, is located between the programmable divider of the PLL circuit and the tuning memory which electrically programmably memorize the allocation of the tuning information (fine tuning) and the program number. The controller converts the tuning information into frequency information (divider ratio). The frequency information is a binary number, representing the divider factor for the PLL divider; it is serially transferred into the PLL. Under usual operation, only the station selection buttons of the TV set are actuated.

   A fixed program address in the tuning memory is assigned to every station button. This program address is intended to store the actual tuning information. After having actuated a station button, a program change instruction PC is issued from the remote control receiver to the controller. This instruction causes the controller to read the tuning information (fine tuning) out of the tuning memory and to assign it to the corresponding channel; hence the TV set is precisely tuned to the requested frequency by means of the PLL.

   Setting of a not yet stored TV transmitter is done by means of the actuating buttons:
   "setting of channel units digits" (SKE) and
   "setting of channel tens digits" (SKZ).

   By means of the button SKE the channel number units digits 0 to 9 without carry and by means of the button SKZ the channel number tens digits can be set. After every button operation, the concerned channel number is incremented by 1. For every adjustment of the channel number, the controller converts this information into frequency information (the PLL divider factor) and provides serial output to the PLL circuit. The success of every tuning step can be watched on the screen.

   In addition to that, the controller is outfitted for station search, which can also be used for setting a TV channel. The station search is started via the setting button: "Search Start" (SST).

   Thereupon the controller sequentially issues every frequency information contained in the internal ROM individually to the PLL circuit. This process is automatically stopped as soon as an operating TV broadcast station is found. This is indicated to the controller by a pulse at the input "Search STOP" (SST) which can be derived from line synchronization.

   Via the setting buttons "fine tuning plus (SEP) +" and "fine tuning minus (SFM) —" frequency deviations from the rated frequency of the individual channel can be set in steps of 125 kHz up to 3.875 MHz and down to — 4 MHz. Frequency tuning, moreover, readjusts automatically every 250 ms, as soon as the proper button is pressed. Within the tuning limits mentioned above, fine tuning runs against a stop (overflow inhibit). After having attained it, the channel number display lights up as long as the setting button is kept pressed.

The tuning information of a once tuned TV broadcast station can be stored in the tuning memory by actuating the store button (L). Upon the L instruction, the controller serially outputs the tuning data on the output DM. The tuning data comprises the fine tuning information and the channel number information.

From the tuning information read into or set in the MOS IC the channel number is used for addressing the mask-programmable ROM table. Frequency information of 100 TV channels is stored in the ROM table.

There are some frequencies to which several TV channels are allocated (stored in the ROM refer to fig. 3), hence no unambiguous channel designation can be gathered from the frequency. This is the reason why the channel number is used as tuning information, since only in this way unambiguous channel designation and frequency information can be gained, simultaneously.

The frequency information is obtained by adding up the ROM divider factor and the center position of fine tuning. At every process of setting a new channel number, fine tuning is adjusted to center position. The PLL divider factor then complies with the nominal divider factor. The nominal divider factor results in an oscillator frequency lying only by $f = 25$ kHz below the nominal value. It represents the frequency information of the exact channel frequency, except the deviation of 25 kHz which is needed to attain a 125 kHz raster frequency at a given IF of 38.9 MHz. For every frequency information the band selection information is programmed in the internal ROM and is serially output from the controller. Band selection differentiates between VHF range I/III and UHF. The internal ROM table is made up such that between the CCIR channels — designated with corresponding channel numbers — other channels are allocated. Thus, the Italian TV channels A-H are stored between channel 12 and channel 21 under channel Nos. 13 to 20 (refer to fig. 4).

Data communication between the MOS IC and the tuning memory is done via a data bus that comprises shift clock "PHI", the actual data, and an enable signal (PCM). The data word contains information on channel number and fine tuning. The channel number is output in BCD coded form (4 bit per digit) and fine tuning as 6 bit dual number.

Figure 5 shows how data is output from (I) or input into (II) the memory by means of the controller SM 564.

The sequence of reading data in and out is fine tuning, channel tens, and channel units digits.

2. Display

The channel number is displayed at the outputs A_1 to A_4, AM_1 and AM_2. The channel digits ($AM_{1.....}$) are output at A_1 to A_4 in BCD coded form in parallel as 4-bit word. The outputs AM_1 and AM_2 determine allocation of the data to units or tens digits. The frequency of these multiplex signals amounts to approx. 60 Hz.

The channel No. can either be indicated via the SAB 3211 on a 2-digit LED display or on-screened.

Station memory

The nonvolatile memory SDA 5650 F can be used as station memory. It includes a 224 bit (16 × 14) or 256 bit (16 × 16) EAROM. Its memory arrangement permits storing of data which is output from the SM 564 (16 words of 14 bits, each). A circuit proposal with the SDA 5650 F as station memory for the SDA 100 system is shown in figure 6.

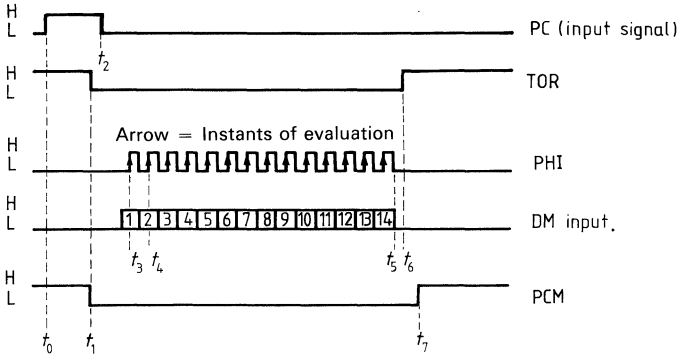
Figure 3
Example of a ROM occupation

Displayed No.	Channel designation	Band selection output UHF VHF BD3	Vision carrier/MHz	Oscillator frequency theoretical/MHz	Oscillator frequency actual/MHz	Deviation f/kHz	Divider factor decimal	Divider factor binary	Divider factor ROM
04	K4	H L H	62.25	101.15	101.125	−25	809	0 0 0 I I 0 0 I 0 I 0 0 I	0 0 0 I I 0 0 0 0 I 0 0 I
05	K5	L L H	175.25	214.15	214.125	−25	1713	0 0 I I 0 I 0 I I 0 0 0 I	0 0 I I 0 I 0 0 I 0 0 0 I
								MSB LSB	MSB LSB

Figure 4
Allocation of channel indication to frequency information contained in the ROM

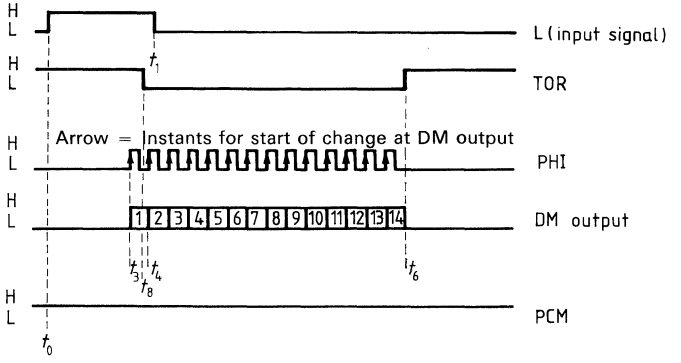
Channel indication	Designation	Channel indication	Designation
01	Australia	81	channel S 1
02	CCIR channel 2	82	channel S 2
•	•	83	channel S 4
12	CCIR channel 12	84	channel S 5
13	Ital. channel A	85	channel S 6
14	Ital. channel B	87	channel S 7
15	Ital. channel C	88	channel S 8
16	Ital. channel D	89	channel S 9
17	Ital. channel E	90	channel S 10
18	Ital. channel F	91	channel S 11
19	Ital. channel G	92	channel S 12
20	Ital. channel H	93	channel S 13
21	CCIR channel 21	94	channel S 14
•	•	95	channel S 15
69	CCIR channel 69	96	channel S 16
73	Standby UHF	97	channel S 17
74	S 21	98	channel S 18
78	S 25	99	channel S 19
79	channel 2 OIR	00	channel S 20
80	channel 5 OIR		

Figure 5
a) Timing diagram - program change



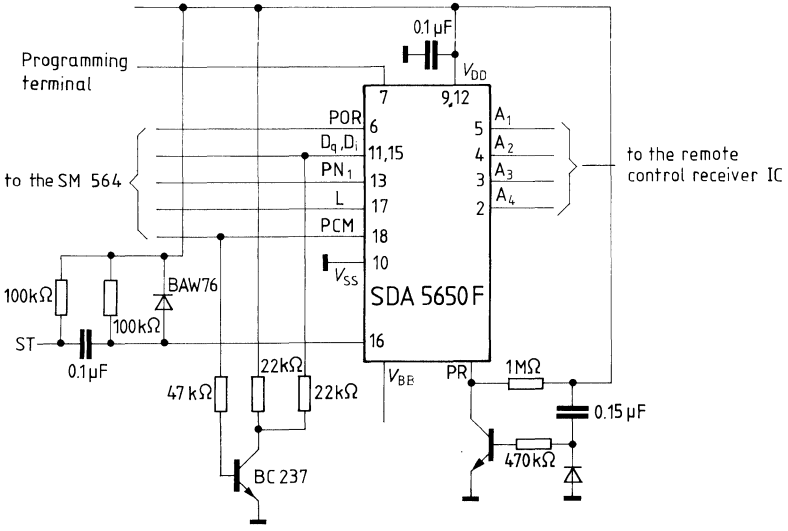
$0 \leqq t_2 - t_0 \cong 32$ ms
$0 \leqq t_1 - t_0 \leqq 32$ ms
$t_3 - t_1 = 956\,\mu s$
$t_4 - t_3 = 512\,\mu s$
$t_6 - t_1 = 8.19$ ms
$t_5 - t_1 = 7.16$ ms
$t_7 - t_1 = 8.91$ ms

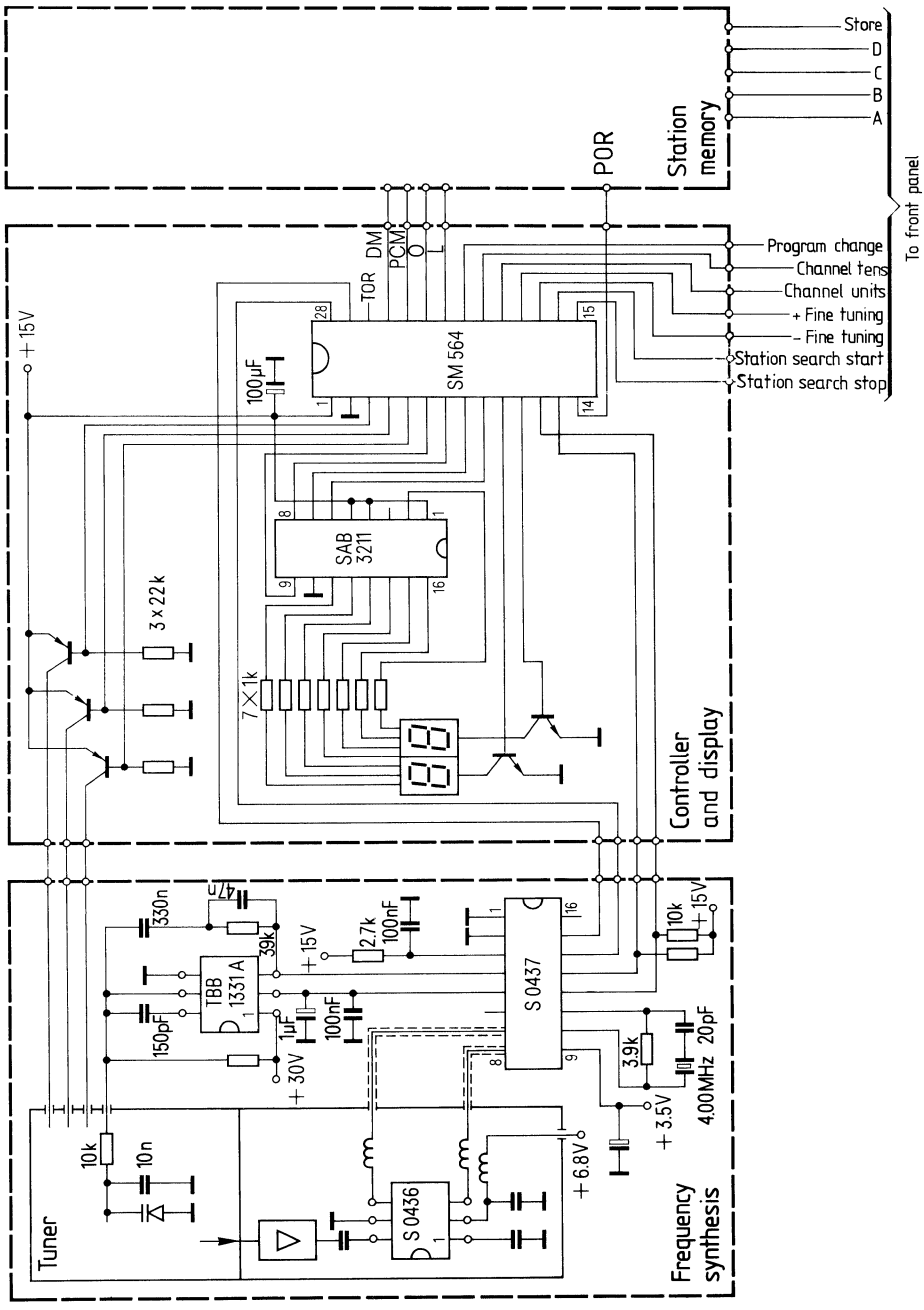
b) Timing diagram - storage of a tuning information



$0 \leqq t_1 - t_0 \cong 32$ ms
$0 \leqq t_8 - t_0 \leqq 32$ ms
$t_8 - t_3 = 256\,\mu s$
$t_4 - t_3 = 512\,\mu s$
$t_6 - t_8 = 7.16$ ms

Figure 6
Possible application of a nonvolatile SDA 5650 F memory as station memory




Station memory
POR
Store
D
C
B
A
To front panel
Program change
Channel tens
Channel units
+ Fine tuning
- Fine tuning
Station search start
Station search stop
Controller and display
SM 564
SAB 3211
TOR
DM
PCM
CL
+15V
100µF
3 x 22k
7 x 1k
Frequency synthesis
Tuner
TBB 1331A
S 0437
S 0436
330n
47
39k
150pF
1µF
100nF
2.7k
10k
3.9k
20pF
4.00MHz
+30V
+3.5V
+6.8V
10n

High Frequency Divider 1:64

S 0436

Bipolar circuit

Fast ECL divider with constant dividing ratio 1:64 covering the frequency range between 80 MHz and 1 GHz. Together with the types S 0437, TBB 1331 A, and a voltage controlled oscillator, a frequency and phase comparison circuit can be designed, intended for channel selection in TV sets.

- Input frequency up to 1 GHz
- Few external components
- Sinusoidal input signal possible
- 2 balanced ECL antiphase outputs

Type	Ordering code	Package outline
S 0436	Q67000-A1339	DIP 6

Maximum ratings

Supply voltage	V_2	8	V
Input voltage	$V_{6\,pp}$	2.5	V
Output current	$-I_3; -I_4$	3	mA
Thermal resistance (system-air)	$R_{th\,SA}$	140	K/W
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C

Range of operation

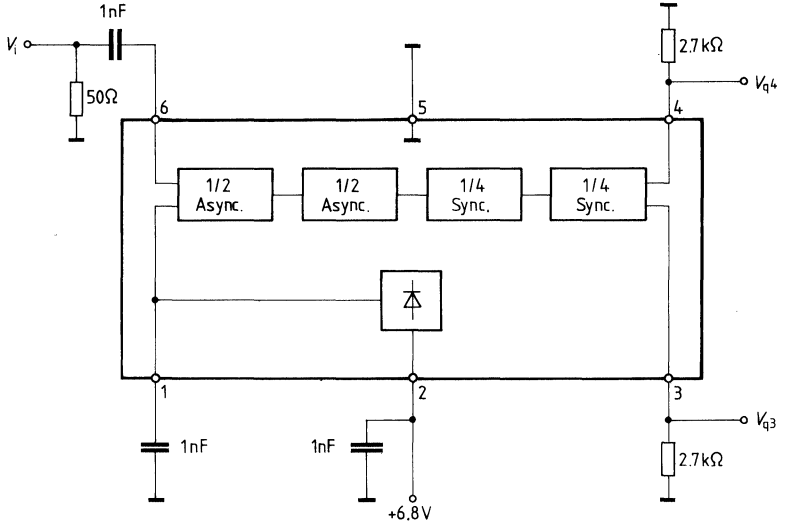
Supply voltage range	V_2	6.45 to 7.15	V
Ambient temperature range	T_{amb}	0 to 70	°C
Input frequency range	f_i	80 to 1000	MHz

Characteristics (V_2 = 6.8 V; T_{amb} = 25 °C; input signal) according to test circuit

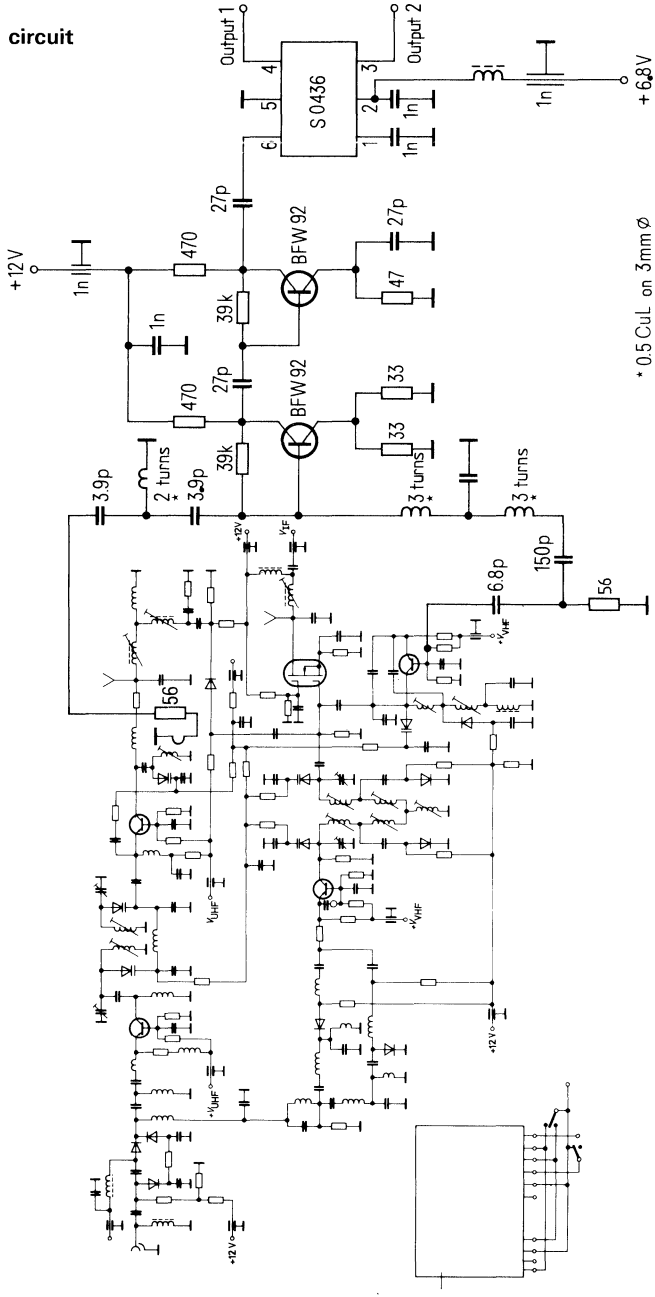
		min	typ	max	
Current consumption	I_2		55	75	mA
Input voltage range					
f_i = 100 MHz	V_6	200		1000	mV
f_i = 300 MHz	V_6	150		1000	mV
f_i = 470 MHz	V_6	100		1000	mV
f_i = 800 MHz	V_6	150		1000	mV
f_i = 900 MHz	V_6	200		1000	mV
Output low level	V_3; V_4		5.4	5.6	V
Output high level	V_3; V_4	6	6.2		V
Output voltage deviation	V_3; V_4	600	800	1000	mV

Input voltage ratings are measured according to the test circuit with HP 3406 A at the divider input.

Test circuit



Application circuit



Bipolar circuit

PLL divider with programmable dividing ratio 1:2 to 1:8191
Together with the types S 0436, TBB 1331 A, and a voltage-controlled oscillator a frequency and phase comparison circuit can be designed, intended for the channel selection in TV sets.
Programming allows quartz-controlled setting of the oscillator frequency for the television bands I/III/IV/V) in 125 kHz raster.

- Few external components
- Internal time base
- High noise immunity

Type	Ordering code	Package outline
S 0437	Q67000-A1347	DIP 16

Maximum ratings

Supply voltage	V_9	6.5	V
	V_3	13.5	V
Input voltage IFO	V_{15}	16	V
Input voltage PLE	V_{14}	16	V
Input voltage divider F, $\overline{F}$	V_7; V_8	7.5	V
Output voltage clock CL	V_{12}	16	V
Sync. output voltage SYC	V_{13}	16	V
Thermal resistance (system-air)	$R_{th\ SA}$	90	K/W
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C

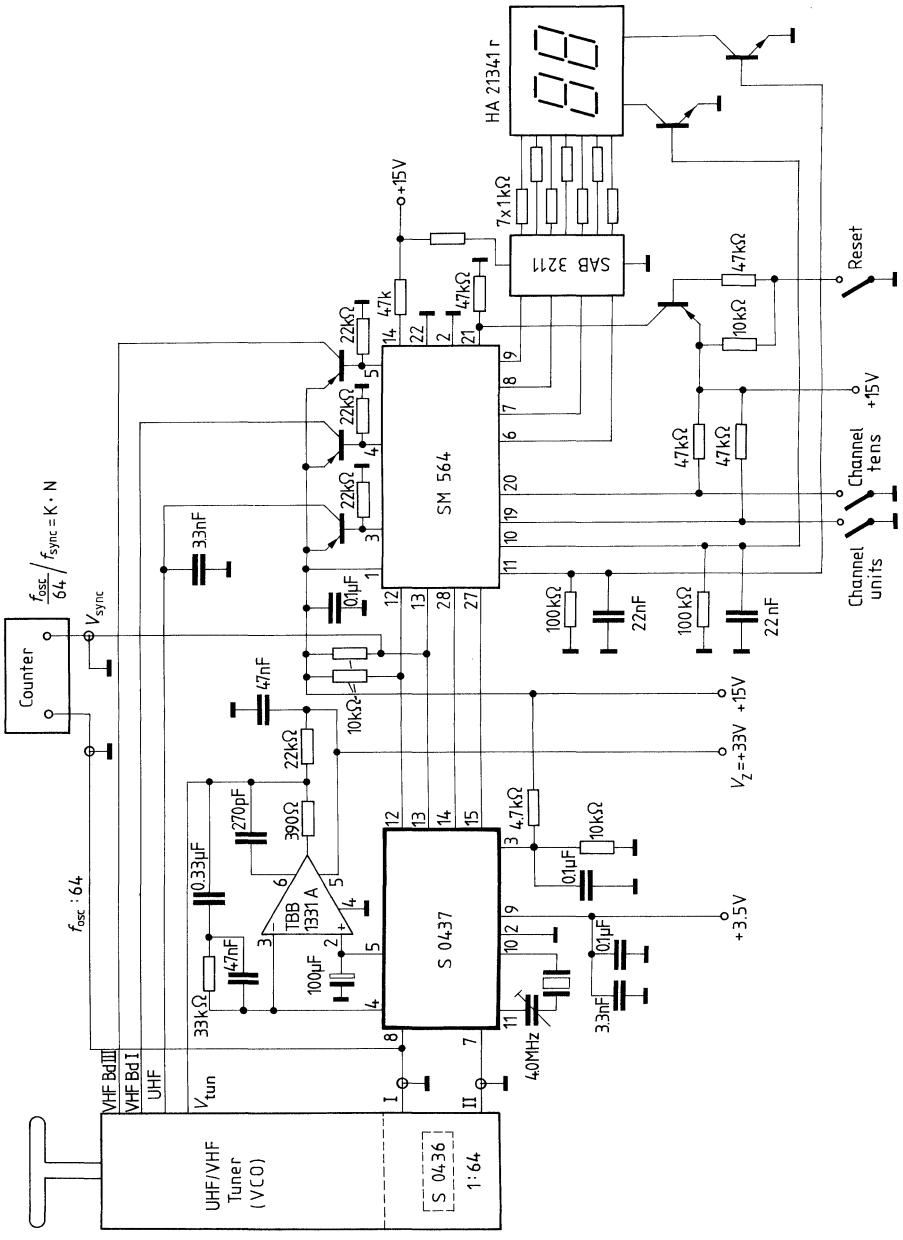
Range of operation

Supply voltage range	V_9	3.25 to 3.75	V
	V_3	3.5 to 12.5	V
Input frequency	f_i	≦15	MHz
Ambient temperature range	T_{amb}	0 to 60	°C

Characteristics (V_9 = 3.5 V; T_{amb} = 25 °C) according to test circuit

		min	typ	max	
Current consumption	I_9	100	150	200	mA
	I_3			1	mA
Input level					
$I_{7/8\,H}$ = 2.4 mA	$V_{7/8\,H}$		6.2		V
$I_{7/8\,L}$ = 2,2 mA	$U_{7/8\,L}$		5.3		V
Inputs IFO, PLE					
(V_{pp} = 15 V; τ = 500 µs; T/τ = 250)	$V_{14/15\,H}$	14	14.5	15	V
	$I_{14/15\,H}$			1.5	mA
	$I_{14/15\,L}$			50	µA
Set-up time	t_S		1.5		µs
Hold time	t_H		3.0		µs
Clock output CL					
(V_{pp} = 15 V; $R_L \geqq$ 6.8 kΩ)	$V_{12\,H}$	14	14.5	15	V
	$V_{12\,L}$			1.5	V
Switching times					
High pulse width	t_{WH}		4		µs
Low pulse width	t_{WL}		12		µs
High-low transition time (R_L = 9.5 kΩ)	t_{THL}			0.5	µs
Low-high transition time (C_L = 50 pF)	t_{TLH}			1.5	µs
Synchronous output SYC					
(V_{pp} = 15 V; $R_L \geqq$ 6.8 kΩ)	$V_{13\,H}$	14	14.5	15	V
	$V_{13\,L}$			1.5	V
Switching times					
High pulse width	t_{WH}		8		µs
Low pulse width	t_{WL}		504		µs
High-low transition time (R_L = 9.5 kΩ)	t_{THL}			0.5	µs
Low-high transition time (C_L = 50 pF)	t_{TLH}			1.5	µs
Delay time	t_p		4		µs
Phase detector output PD	$I_{4\,Load}$		+100		µA
	$I_{4\,Sink}$		−100		µA
PD reference PD REF	V_3	$\frac{V_3}{2}+0.2$		$\frac{V_3}{2}+0.7$	V
Divider input sensitivity (f_i = 15 MHz)	$V_{7/8_{pp}}$	600	800	1000	mV
Lock indication output LOCK IND	$V_{6\,L}$		0		V
(R_L = 10 kΩ)	$V_{6\,H}$	2.5			V

Test circuit



Functional description

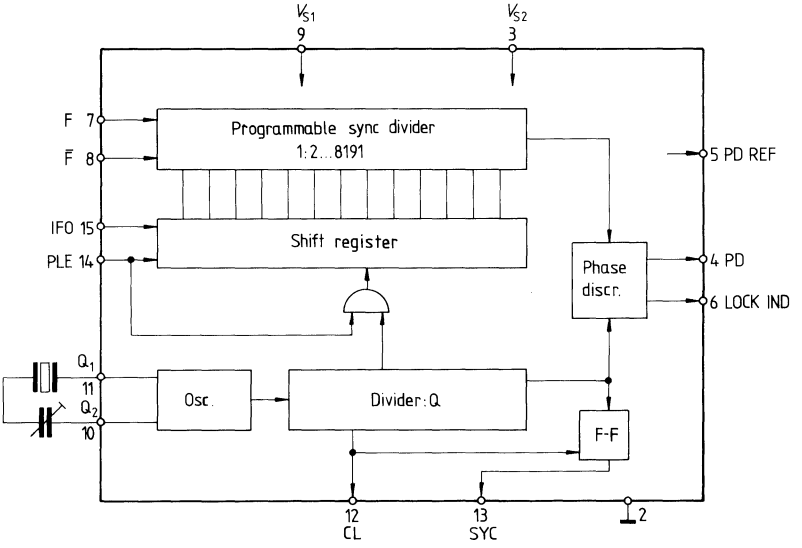
S 0437 includes a 13 bit parallel-programmable synchronous divider (divider factor N = 2 to 8191), a 13 bit shift register, a quartz oscillator (f_{osc} = 4.0 MHz) with subsequent divider (divider factor Q = 2048) and a frequency and phase sensitive digital phase detector. The dividing factor N in 13 digit dual code — is serially input into a 13 bit shift register with parallel output. As first bit the LSB (least significant bit) is pushed in, and the MSB (most significant bit) as last one. Acceptance at the information input (IFO) only takes place when the enable input is at high level (PLE). The shifting clock (f = 62.5 kHz) is available at the open collector output (CL). Shifting is done by the low — high transition of the shifting cycle.

Referred to the high — low transition of the enable input, only the last 13 cycles are utilized. Possible preceding dummy bits remain without importance. H level of the enable input is only allowed to exist when the synchronous output (SYC) is at L level. The synchronous divider has balanced pushpull clock inputs (F, $\overline{F}$) for ECL level.

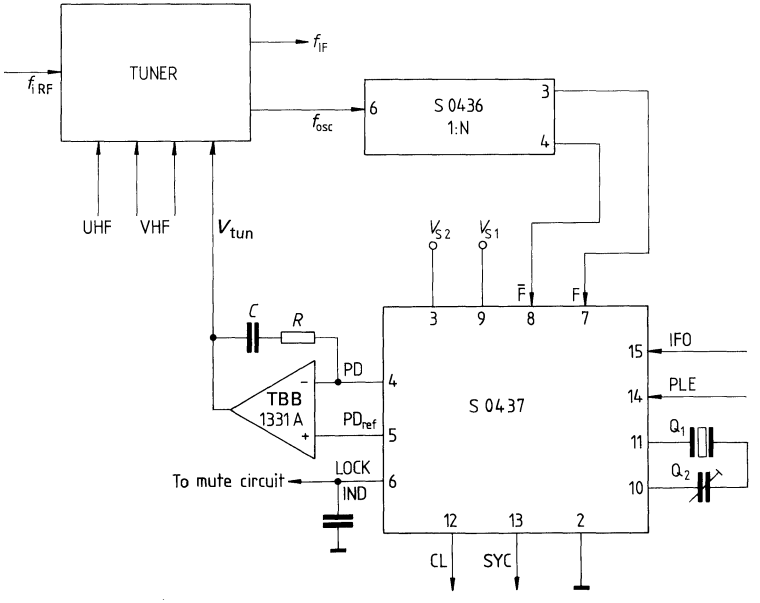
L signal is obtained at the output LOCK IND in case of frequency and phase synchronization.

The phase detector may be operated with a separated voltage supply (V_{S2}). From the output phase detector (PD), the fine tuning voltage for the VCO (tuner) is gained by means of an active PI network (OP AMP). The output PD REF can be used as reference potential for the operational amplifier.

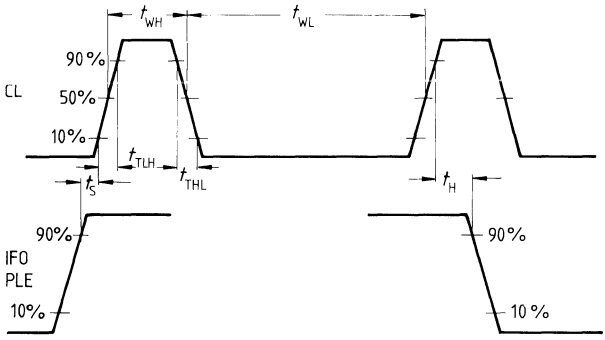
Block diagram

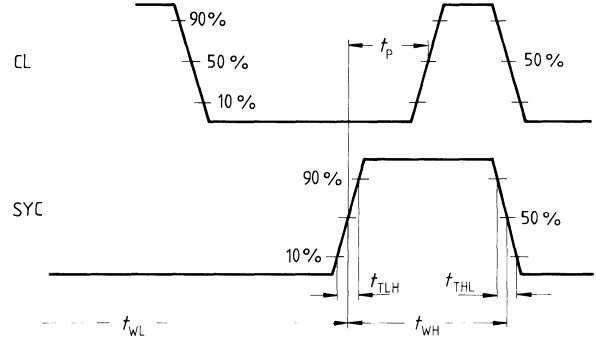


Application circuit (schematic)

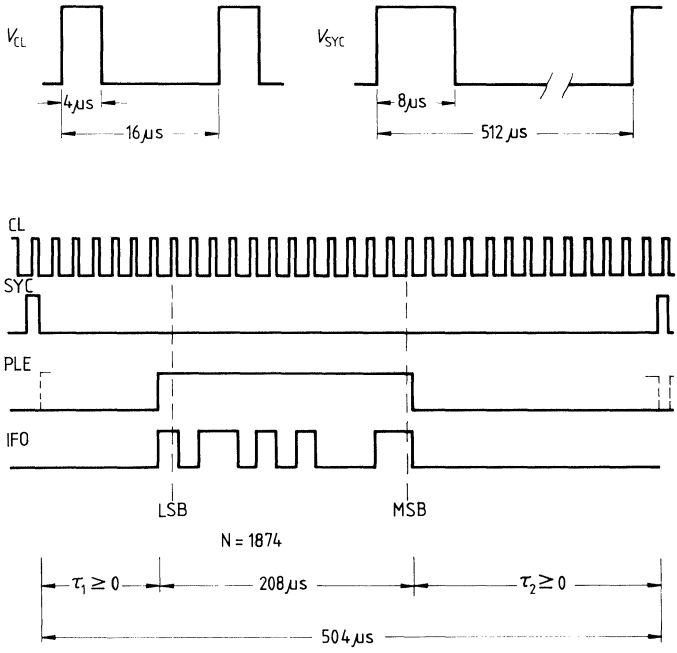


Pulse diagram





Timing diagram



Operational Amplifier with Darlington Input — TBB 1331 A

Bipolar circuit

Operational amplifier which is due to its features particularly suited for use as integrator. Together with the S 0436, S 0347, and a voltage controlled oscillator a frequency and phase comparison circuit can be designed, intended for channel selection in TV sets.

- High input resistance
- Large supply voltage range
- Large control range
- Simple frequency compensation

Type	Ordering code	Package outline
TBB 1331 A	Q67000-A1348	DIP 6

Maximum ratings

Supply voltage	V_S	± 17	V
Output current	I_q	10	mA
Differential input voltage			
V_S = 2 to 13 V	V_{Di}	± V_S	
V_S = 13 to 17 V	V_{Di}	± 13	V
Thermal resistance (system-air)	$R_{th\ SA}$	140	K/W
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C

Range of operation

Supply voltage range	V_S	± 2 to ± 17	V
Ambient temperature range	T_{amb}	0 to 70	°C

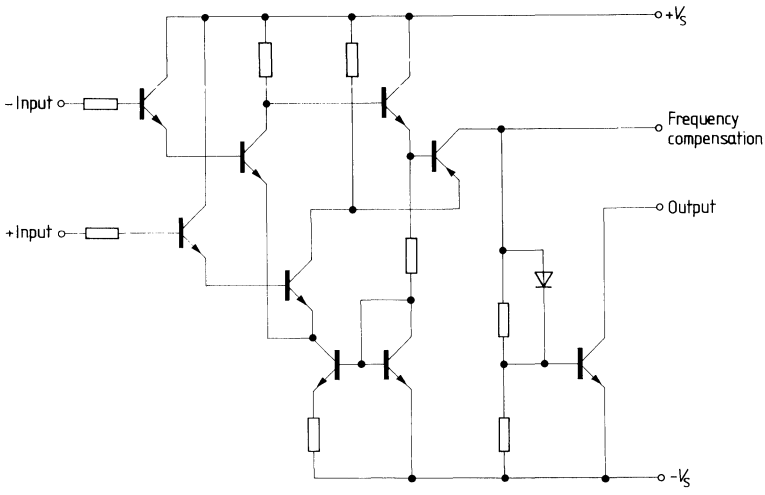
Characteristics ($V_S = \pm 15$ V; $T_{amb} = 25$ °C)

		min	typ	max	
No-load current	I_1		1.5	2.5	mA
Input offset voltage ($R_G = 50\ \Omega$)	V_{ios}	−20		+20	mV
Input offset current	I_{ios}	−25	±10	+25	nA
Input current	I_i		30	50	nA
$V_{Di} = \pm 13$ V	I_i			200	nA
Output voltage ($R_L = 18$ kΩ)	V_{qpp}	+14.8		−14.5	V
Input resistance ($f_i = 1$ kHz)	R_i		3		MΩ
Open-loop voltage gain ($R_L = 18$ kΩ; $f_i = 1$ kHz)	G_v	55	68		dB
Input common mode range ($R_L = 18$ kΩ)	V_{icM}	+13		−13	V
Common mode rejection ratio ($R_L = 18$ kΩ)	$CMRR$	60	74		dB
Supply voltage rejection ($G_v = 100$)	$\frac{\Delta V_{ios}}{\Delta V_S}$		100	400	µV/V
Temp. coeff. of V_{ios} ($R_G = 50\ \Omega$)	α_i		12		µV/K
Temp. coeff. of I_{ios}	α_i		50		pA/K
Rise time of V_q for non-inverting operation (see TAA 761, test circuit1)	$\frac{dV_q}{dt_r}$			4.5	V/µs
Rise time of V_q for inverting operation (see TAA 761, test circuit 2)	$\frac{dV_q}{dt_r}$		9		V/µs
Output saturation voltage ($I_q = 2$ mA)	V_{qo}			0.5	V
Output leakage current	I_{qlk}		1	10	V/µs

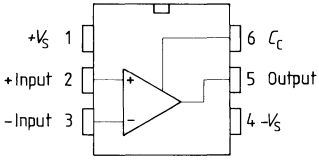
Characteristics ($V_S = \pm 5$ V; $T_{amb} = 25$ °C)

Input offset voltage ($R_G = 50\ \Omega$)	V_{ios}	−20		+20	mV
Input offset current	I_{ios}	−25	±10	+25	nA
Input current	I_i		30	50	nA
Open loop voltage gain ($R_L = 18$ kΩ; $f = 1$ kHz)	G_v	53			dB

Internal circuit

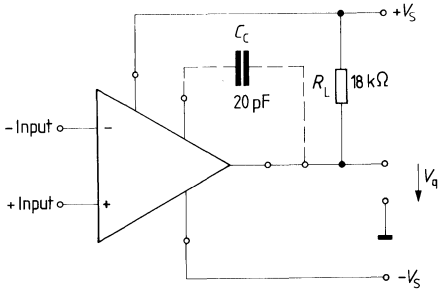


Pin configuration

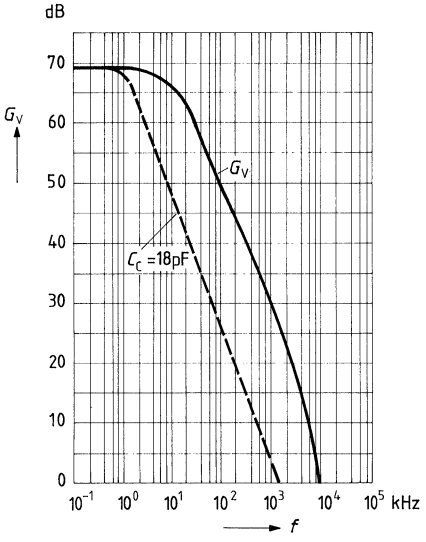


Connection diagram

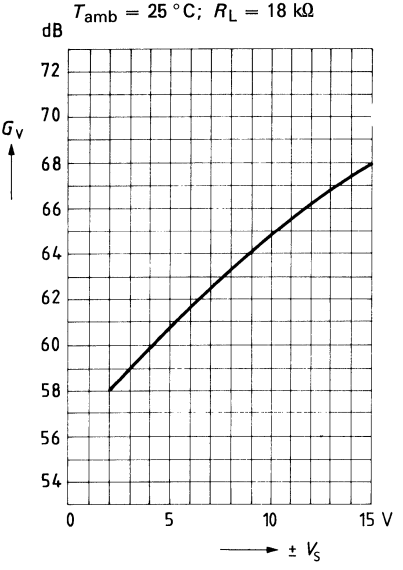
C_C = Output frequency compensation
R_L = Load resistance



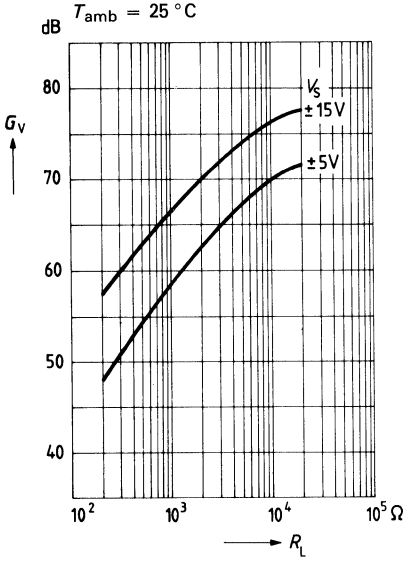
Open-loop voltage gain versus frequency
R_L = 18 kΩ; T_{amb} = 25 °C



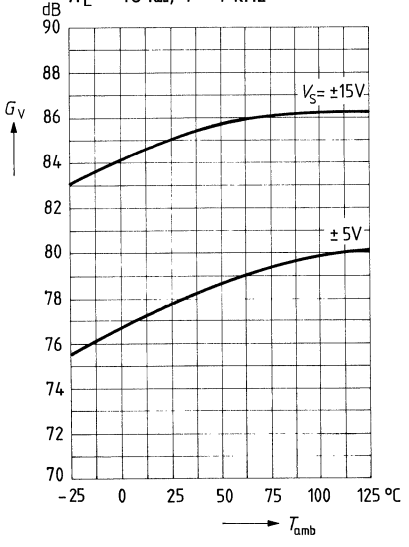
Open-loop voltage gain versus supply voltage
T_{amb} = 25 °C; R_L = 18 kΩ



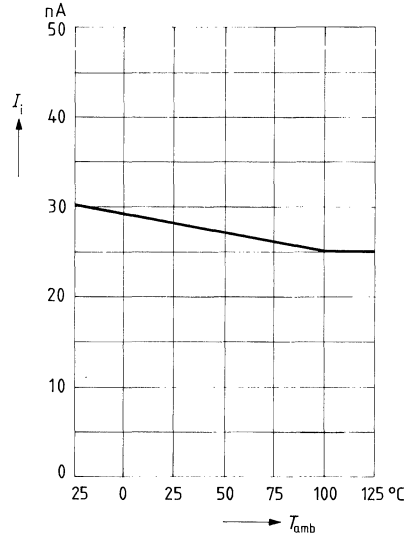
Open-loop voltage gain versus load resistance
T_{amb} = 25 °C



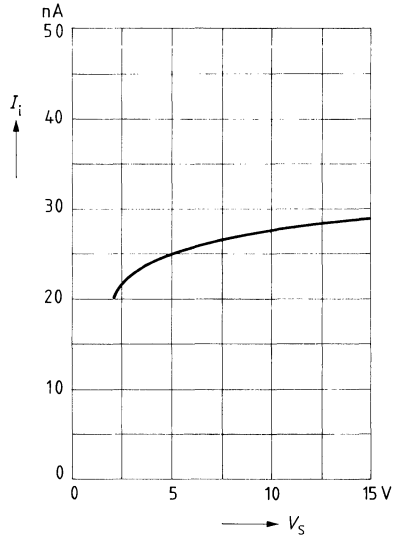
Open-loop voltage gain versus ambient temperature
R_L = 18 kΩ; f = 1 kHz



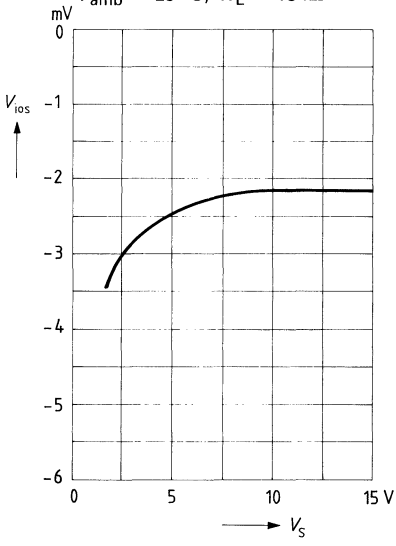
Input current
versus ambient temperature
R_L = 18 kΩ



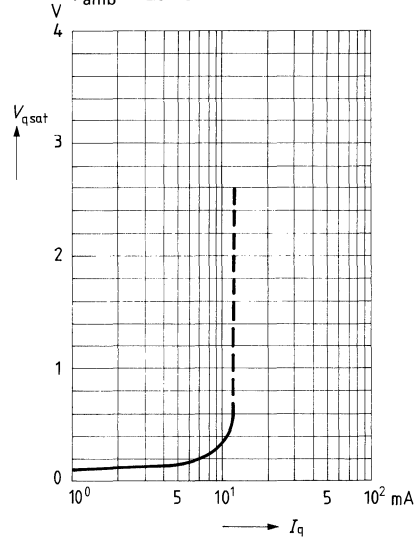
Input current
versus supply voltage
T_{amb} = 25 °C; R_L = 18 kΩ



Input offset voltage
versus supply voltage
T_{amb} = 25 °C; R_L = 18 kΩ



Saturation voltage
versus output current
T_{amb} = 25 °C



MOS circuit

The integrated MOS IC SM 564 is part of the frequency synthesis tuning system for TV sets. The IC is intended for converting the tuning information in a frequency information. It is located between the programmable divider of the PLL module and the tuning memory which electrically programmably stores the assignment of tuning information and storage number. In an ROM the IC SM 564 includes the exact frequency information (in the 125 kHz raster) mask programmable for 100 channel numbers and takes control of the tuning memory and the programmable divider over.

The programmable divider in the PLL module and the tuning memory receive different information: the programmable divider is informed with a frequency information in form of a dividing factor. On the other hand, the channel number and fine detuning (here called tuning information) are stored in the tuning memory. The IC SM 564 is used to convert the tuning information into a frequency information.

The outputs PHI, A_1 to A_4, AM_1, AM_2, PCM, and TOR are short-circuit proof against V_{DD} and V_{SS}.

Type	Ordering code	Package outline
SM 564	Q67100-Z123	DIP 28

Maximum ratings (all voltages referred to V_{DD})

		min	max	
Supply voltage	V_{SS}	−0.3	18	V
Input voltage	V_i	0	V_{SS} +0.3 V	
Power dissipation per output	P_q		100	mW
Total power dissipation	P_{tot}		500	mW
Storage temperature range	T_{stg}	−55	125	°C

Range of operation (referred to V_{DD})

Supply voltage range	V_{SS}	13.5 to 16	V
Ambient temperature range	T_{amb}	0 to 70	°C

Characteristics (all voltages referred to V_{DD})

		min	typ	max	
Current consumption V_{SS} = 16 V output without load	I_{SS}	3	6	30	mA
CL Clock signal from S 0437					
H-input voltage	V_{iH}	$V_{SS}-1$ V		V_{SS}	
L-input voltage	V_{iL}	0		1.5	V
H-pulse width	$t_{WH\ CL}$	3.5	4	4.5	µs
Period	t_{CL}		16		µs
H-L transition time	$t_{THL\ CL}$	0		0.5	µs
L-H transition time	$t_{TLH\ CL}$	0		1.5	µs
Input capacitance	C_i	0		10	pF
Input resistance	R_i	1			MΩ
SYC synchronous signal from S 0437					
H-input voltage	V_{iH}	$V_{SS}-2.5$V		V_{SS}	
L-input voltage	V_{iL}	0		1.5	V
H-pulse width	$t_{WH\ SYC}$		8		µs
Overlap angle 1	$t_{R\ 1}$	0			µs
Overlap angle 2	$t_{R\ 2}$	0			µs
Input capacitance	C_i	0		10	pF
Input resistance	R_i	1			MΩ
L-pulse width	$t_{WL\ SYC}$		504		µs
Input signals SKE, SKZ, SFP, SFM, SST, SSP					
Schmitt-trigger inputs with incorporated "Pull High" resistors					
H-input voltage	V_{iH}	$V_{SS}-1$ V		V_{SS}	
L-input voltage	V_{iL}	0	V_{SS}	$V_{SS}-7$ V	
Necessary L-input current	I_{iL}	0.03		1	mA

Characteristics (cont'd)

		min	typ	max	
Input signals: POR, PC Schmitt-trigger inputs					
H-input voltage	V_{iH}	$V_{SS}-1$ V		V_{SS}	
L-input voltage	V_{iL}	0		$V_{SS}-7$ V	
Input capacitance	C_i	0		10	pF
Input resistance	R_i	1			MΩ
Input signals: DM, L					
H-input voltage	V_{iH}	$V_{SS}-1$ V		V_{SS}	
L-input voltage	V_{iL}	0		$V_{SS}-7$ V	
Output signals: Tuner band selection outputs UHF, VHF, BD3					
Open drain stages turning to V_{SS} with internal high-ohmic pull-low resistors for measuring purposes					
H-output voltage (I_{load} = 1 mA)	V_{qH}	$V_{SS}-0.35$ V		V_{SS}	
L-reverse current ($V_q = V_{DD}$)	I_{qL}			15	µA
Output signals: IFO, PLE					
Open-drain stages (load resistor incorporated in S 0437)					
H-output voltage (I_{load} = 1.5 mA)	V_{qH}	$V_{SS}-1.4$ V		V_{SS}	
L-reverse current	I_{qL}			50	µA
Delay time (C_{load} = 50 pF)	$t_{Dq}+t_{Tq}$			9	µs
Ext. load current	I_{load}			2	mA

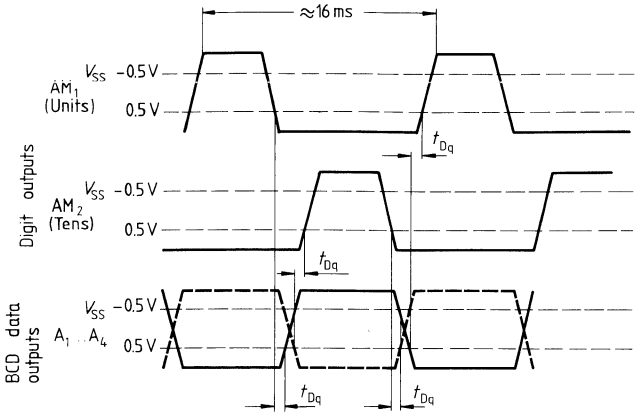
Characteristics (cont'd)

		min	typ	max	
Output signals: PHI, A_1, A_2, A_3, A_4, AM_1, AM_2, PCM, TOR					
Open-drain stage with incorporated load resistor					
H-output voltage (at I_{load} = 2 mA)	V_{qH}	$V_{SS}-6$ V		V_{SS}	
H-output voltage (at I_{load} = 100 µA)	V_{qH}	$V_{SS}-0.5$ V	V_{SS}		
L-output voltage (at I_{load} = 1 µA)	V_{qL}	0		0.4	V
Short circuit current against V_{SS} ($V_q = V_{SS}$ = 16 V)	I_{qLKH}	50			µA
PHI period (at t_{CL} = 16 µs)	t_{PHI}		512		µs
PHI transition times (at C_{load} = 30 pF)	$t_{THL\ PHI}$			10	µs
Multiplex period (at t_{CL} = 16 µs)	T_M		16		ms
Delay of BCD outputs $A_1 \ldots A_4$ against digit output AM_1 or AM_2, resp. (at t_{CL} = 16 µs) Delay of digit outputs against BCD outputs	t_{Dq}	0.5	2		ms
Output signals: DM					
Open-drain output					
H-output voltage (I_{load} = 2 mA)	V_{qH}	$V_{SS}-6$ V	V_{SS}		
H-output voltage (I_{load} = 100 µA)	V_{qH}	$V_{SS}-0.5$ V	V_{SS}		
DM-overlap angle 1 (at t_{CL} = 16 µs)	$t_{D1\ DM}$	100	256		µs
DM-overlap angle 2	$t_{D2\ DM}$	100	256		µs
L-reverse current (V_{qL} = 0 V)	I_{qL}		50		µA

Pin designation

Pin No.	Description
1	V_{SS} supply voltage
2	V_{DD} supply voltage
3	UHF band selection
4	VHF band selection
5	BD3 band selection
6	A_1 } BCD display
7	A_2 } BCD display
8	A_3 } BCD display
9	A_4 } BCD display
10	AM_2 } display, multiplex control
11	AM_1 } display, multiplex control
12	CL clock
13	SYC synchronization
14	POR power reset
15	SSP station search stop
16	SST station search start
17	SFM fine tuning −
18	SFP fine tuning +
19	SKE control channel units
20	SKZ control channel tens
21	PC program change
22	L load, from memory
23	PHI clock for memory
24	PCM program change, memory
25	DM data memory
26	TOR
27	IFO data line PLL
28	PLE PLL enable

Timing diagram

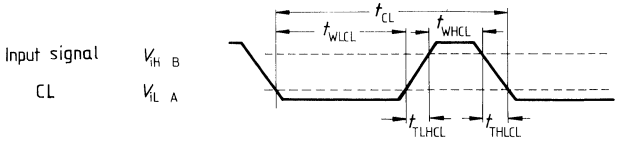


BCD code

A_4	A_3	A_2	A_1	Display
L	L	L	L	0
L	L	L	H	1
L	L	H	L	2
L	L	H	H	3
L	H	L	L	4
L	H	L	H	5
L	H	H	L	6
L	H	H	H	7
H	L	L	L	8
H	L	L	H	9

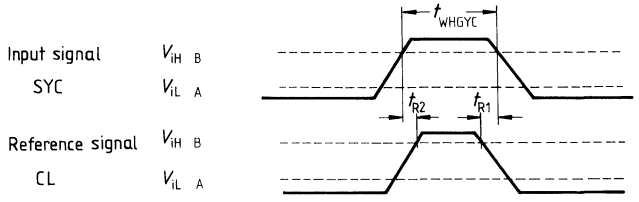
CL clock signal from S 0437

Timing diagram



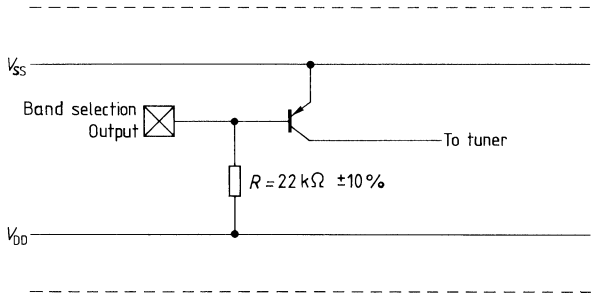
SYC sync signal from S 0437

Timing diagram



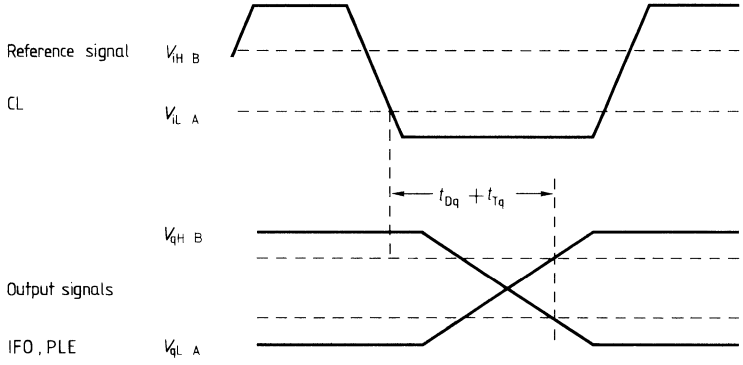
Tuner band selection outputs UHF, VHF BD 3

Operating circuit provided

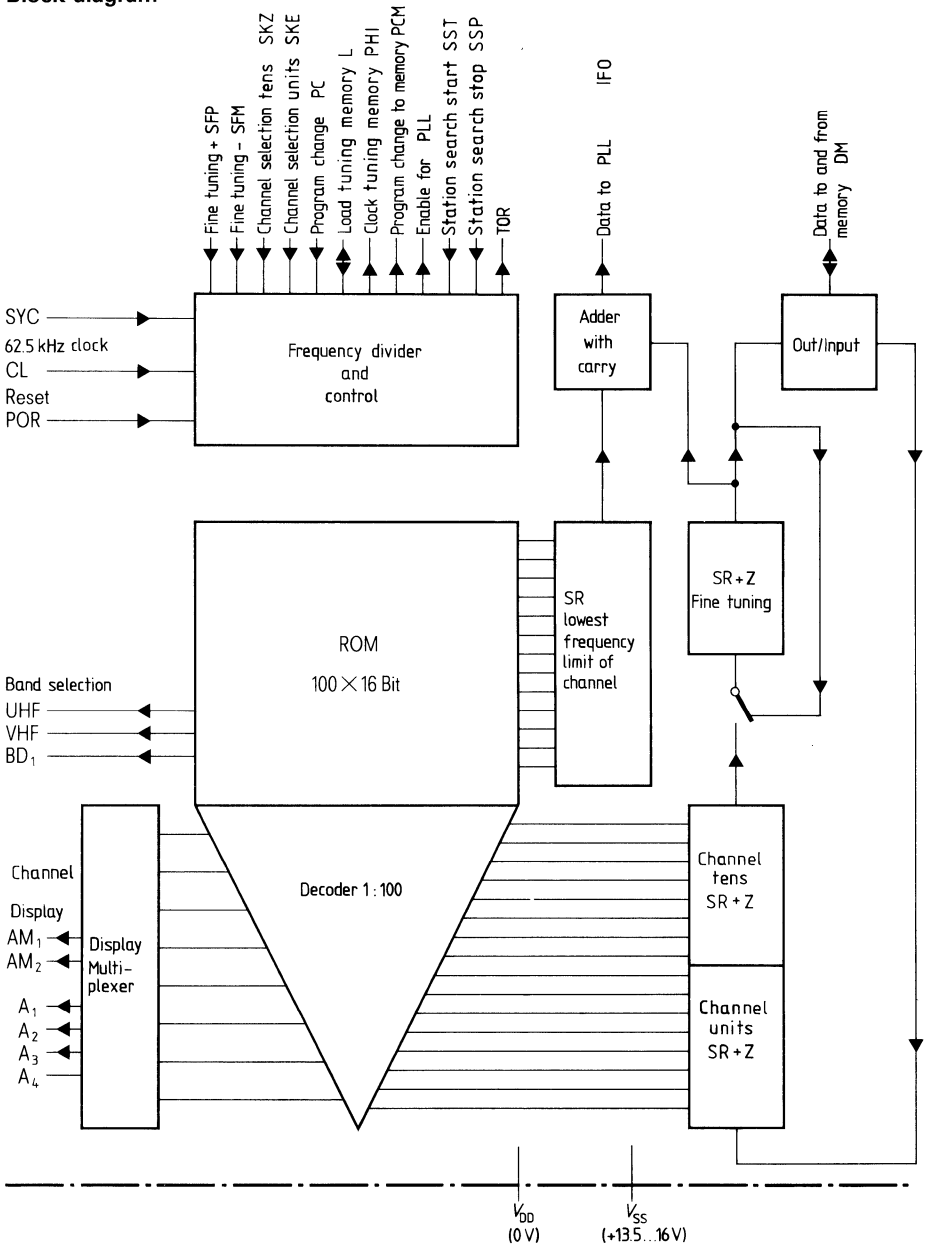


Output signals IFO, PLE

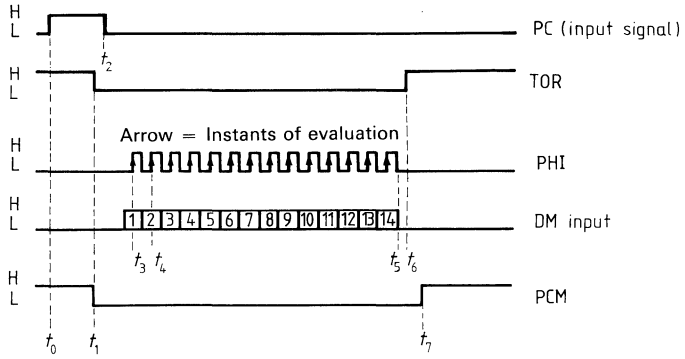
Timing diagram



Block diagram

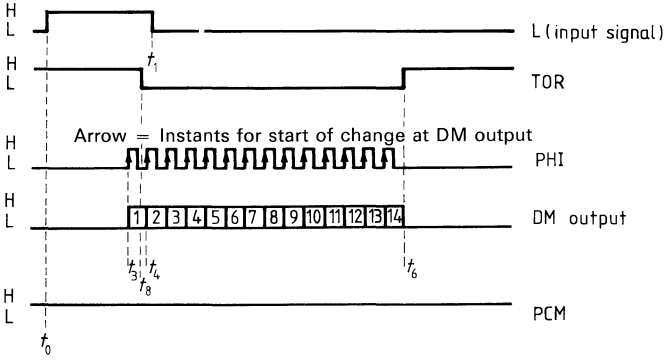


a) Timing diagram — program change



$0 \leqq t_2 - t_0 \cong 32$ ms
$0 \leqq t_1 - t_0 \leqq 32$ ms
$t_3 - t_1 = 956$ µs
$t_4 - t_3 = 512$ µs
$t_6 - t_1 = 8.19$ ms
$t_5 - t_1 = 7.16$ ms
$t_7 - t_1 = 8.91$ ms

b) Timing diagram — storage of a tuning information



$0 \leqq t_1 - t_0 \cong 32$ ms
$0 \leqq t_8 - t_0 \leqq 32$ ms
$t_8 - t_3 = 256$ µs
$t_4 - t_3 = 512$ µs
$t_6 - t_8 = 7.16$ ms

Coverage of functional processes (see block diagram)

The most frequent process is a **program change** indicated by the operating unit via line PC. Switching-on the TV set starts the same process which is caused by a slope at the POR input.

The process runs as follows:
a) Reading-in of the information from the memory
The input/output stage is switched as input and PCM is set on LOW level. After a period $t_3 - t_1 \geqq 512$ µsec, the clock PHI moves to H and clocks 14 times at a period of 512 µsec.

The tuning information appears at input DM emating from the memory. At the LH edges of PHI, the information is evaluated and read into the channel and the fine detuning counters. PCM again moves to HIGH and the output/input stage is switched through, whereas, outwards, it is set to neutral.

b) Shifting the divider factor to PLL.
The ROM resident frequencies of the channels are read out using the channel number (8 bit address), in parallel to that the read-out shift register is loaded.

Now the frequency information is moved to the programmable divider of the PLL circuit: The line PLE is set on high level, and 13 clocks reach the read-out shift register at a period of 16 µsec. While the first 6 bits are shifted out, an adder adds the contents of the fine tuning counter to the contents of the ROM. After the 13th clock the PLE output returns to low.

The process (b) is repeated every 250 msec thus ensuring that tuning of the TV set is always synchronous to the indication.

During runs (a) and (b), all the inputs for fine detuning, channel setting, program change (PC), and load (L memory signal) are not weighted.

c) Alteration of the tuning information

The channel number can be altered either by calling the inputs: channel, unit digits, (SKE), and channel, tens digits, (SKZ), or by the station search start (SST) which is stopped by an own input.

Via the inputs fine detuning "plus" (SFP) and "minus" (SFM), the tuning information can be varied upwards by 31 × 125 kHz and downwards by 32 × 125 kHz. With the alteration of the channel number the fine detuning counter is repositioned to its mean position.

Press on button	Alteration	Clock for automatic counting
SFP	Fine detuning increments by 1	0.25 sec
SFM	Fine detuning decrements by 1	0.25 sec
SKZ	Tens digit of channel counter increments by 1	–
SKE	Unit digit of channel counter increments by 1 without carry to tens digit	–
SST	Unit digit of channel counter increments by 1 with carry to tens digit until input SPP is acknowledged	0.25 sec

d) Storage of the tuning information
The IC is provided for the connection of nonvolatile and CMOS memories (information material can be obtained upon request).

Detailed run
Via the L input it is indicated with high level that the tuning information shall be moved to the memory. After a period $(t_8 - t_7) \geqq 512$ µsec, the clock PHI goes to high and clocks 14 times at a period of 512 µsec. At every LH slope of the PHI cycle, information changes to the next bit.

After storage has taken place and when the L input is on low level a process will run like that of the program change (see (a) and (b)) in order to control the new memory contents. During the run of (d), inputs PC, SFP, SFM, SKZ, and SKE are blocked.

Display

The display information is output in BCD code for 2 digits in multiplex operation. The channel counter is designed as a decimal counter. The 2 digits are output via a multiplexer. When in case of fine detuning the stop of the internal counter is reached the display unit signals as long as the fine detuning input has been actuated.

Tuner range selection outputs

3 independent outputs — UHF, VHF, BD 3 — are available (see table ROM occupation). The outputs only change with or after the LH slope of PLE during the run according to (b).

ROM occupation

Indicated number	Channel designation	Band selection output UHF	Band selection output VHF BD 3	Vision - carrier / MHz	Oscillator frequency theoretical/MHz	Oscillator frequency actual/MHz	Deviation Δf/kHz	Divider factor decimal	Divider factor binary 2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	Divider factor ROM 13	12	11	10	9	8	7	6	5	4	3	2	1
									13	12	11	10	9	8	7	6	5	4	3	2	1	13	12	11	10	9	8	7	6	5	4	3	2	1
01	AU0	H	L H	46.25	85.15	85.125	−25	681	0	0	0	1	0	1	0	1	0	1	0	0	1	0	0	0	1	0	1	0	0	0	1	0	0	1
02	K2	H	L H	48.25	87.15	87.125	−25	697	0	0	0	1	0	1	0	1	1	1	0	0	1	0	0	0	1	0	1	0	0	1	1	0	0	1
03	K3	H	L H	55.25	94.15	94.125	−25	753	0	0	0	1	0	1	1	1	1	1	0	0	0	1	0	0	0	1	0	1	1	1	0	1	0	0	0	1
04	K4	H	L H	62.25	101.15	101.125	−25	809	0	0	0	1	1	0	0	1	0	1	0	0	1	0	0	0	1	1	0	0	0	0	1	0	0	0	1
05	K5	L	L H	175.25	214.15	214.125	−25	1713	0	0	1	1	0	1	0	1	1	0	0	0	1	0	0	1	1	0	1	0	1	0	0	1	0	0	0	1
06	K6	L	L H	182.25	221.15	221.125	−25	1769	0	0	1	1	0	1	1	1	0	1	0	0	1	0	0	1	1	0	1	1	1	0	0	1	0	0	0	1
07	K7	L	L H	189.25	228.15	228.125	−25	1825	0	0	1	1	1	0	0	1	0	0	0	0	1	0	0	1	1	1	0	0	0	0	0	0	0	0	0	1
08	K8	L	L H	196.25	235.15	235.125	−25	1881	0	0	1	1	1	0	1	0	1	1	0	0	1	0	0	1	1	1	0	0	1	1	1	0	0	1	0	1
09	K9	L	L H	203.25	242.15	242.125	−25	1937	0	0	1	1	1	1	0	0	1	0	0	0	1	0	0	1	1	1	0	1	1	1	0	0	0	1	0	1
10	K10	L	L H	210.25	249.15	249.125	−25	1993	0	0	1	1	1	1	1	0	0	1	0	0	1	0	0	1	1	1	1	1	0	1	0	1	0	0	0	1
11	K11	L	L H	217.25	256.15	256.125	−25	2049	0	1	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	1	1	1	1	1	1	0	0	0	0	1
12	K12	L	L H	224.25	263.15	263.125	−25	2105	0	1	0	0	0	0	0	1	1	1	0	0	1	0	1	0	0	0	0	0	0	1	1	0	0	1	0	1
13	A	H	L H	53.75	92.65	92.625	−25	741	0	0	0	1	0	1	1	1	0	0	1	0	1	0	0	0	1	0	1	1	1	0	0	0	1	0	1	0
14	B	H	L H	62.25	101.15	101.125	−25	809	0	0	0	1	1	0	0	1	0	1	0	0	1	0	0	0	1	1	0	0	0	0	1	0	0	1	0	1
15	C	H	L H	82.25	121.15	121.125	−25	969	0	0	0	1	1	1	1	0	0	1	0	0	1	0	0	0	1	1	1	0	1	0	1	0	0	1	0	1
16	D	L	L H	175.25	214.15	214.125	−25	1713	0	0	1	1	0	1	0	1	1	0	0	0	1	0	0	1	1	0	1	0	0	1	0	0	0	1	0	1
17	E	L	L H	183.75	222.65	222.625	−25	1781	0	0	1	1	0	1	1	1	1	1	0	1	0	1	0	0	1	1	0	1	1	1	0	1	0	1	0	1
18	F	L	L H	192.25	231.15	231.125	−25	1849	0	0	1	1	1	0	0	1	1	1	0	0	1	0	0	1	1	1	0	0	0	1	1	0	0	1	0	1
19	G	L	L H	201.25	240.15	240.125	−25	1921	0	0	1	1	1	1	0	0	0	0	0	0	1	0	0	1	1	1	0	1	1	0	0	0	0	1	0	1
20	H	L	L H	210.25	249.15	249.125	−25	1993	0	0	1	1	1	1	1	0	0	1	0	0	1	0	0	1	1	1	1	1	0	1	0	1	0	0	0	1
21	K21	H	H L	471.25	510.15	510.125	−25	4081	0	1	1	1	1	1	1	1	1	1	0	0	0	1	0	1	1	1	1	1	1	1	0	1	0	0	0	1
22	K22	H	H L	479.25	518.15	518.125	−25	4145	1	0	0	0	0	0	0	1	1	0	0	0	1	1	0	0	0	0	0	0	0	0	1	0	0	0	1	1
23	K23	H	H L	487.25	526.15	526.125	−25	4209	1	0	0	0	0	0	1	1	1	0	0	0	1	1	0	0	0	0	0	1	0	1	0	0	0	0	1	1
24	K24	H	H L	495.25	534.15	534.125	−25	4273	1	0	0	0	0	1	0	1	1	0	0	0	1	1	0	0	0	0	1	0	0	1	0	0	0	0	1	1
25	K25	H	H L	503.25	542.15	542.125	−25	4337	1	0	0	0	0	1	1	1	1	0	0	0	1	1	0	0	0	0	1	1	0	1	0	0	0	0	1	1

ROM occupation

Indicated number	Channel designation	Band selection output UHF	Band selection output VHF	Band selection output BD 3	Vision - carrier / MHz	Oscillator frequency theoretical/MHz	Oscillator frequency actual/MHz	Deviation Δf/kHz	Divider factor decimal	Divider factor binary 2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	Divider factor ROM 13	12	11	10	9	8	7	6	5	4	3	2	1
										13	12	11	10	9	8	7	6	5	4	3	2	1												
26	K26	H	H	L	511.25	550.15	550.125	−25	4401	1	0	0	0	1	0	0	1	1	0	0	0	1	1	0	0	0	1	0	0	0	1	0	0	0	1
27	K27	H	H	L	519.25	558.15	558.125	−25	4465	1	0	0	0	1	0	1	1	1	0	0	0	1	1	0	0	0	1	0	1	0	1	0	0	0	1
28	K28	H	H	L	527.25	566.15	566.125	−25	4529	1	0	0	0	1	1	0	1	1	0	0	0	1	1	0	0	0	1	1	0	0	1	0	0	0	1
29	K29	H	H	L	535.25	574.15	574.125	−25	4593	1	0	0	0	1	1	1	1	1	0	0	0	1	1	0	0	0	1	1	1	0	1	0	0	0	1
30	K30	H	H	L	543.25	582.15	582.125	−25	4657	1	0	0	1	0	0	0	1	1	0	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	1
31	K31	H	H	L	551.25	590.12	590.125	−25	4721	1	0	0	1	0	0	1	1	1	0	0	0	1	1	0	0	1	0	0	1	0	1	0	0	0	1
32	K32	H	H	L	559.25	598.15	598.125	−25	4785	1	0	0	1	0	1	0	1	1	0	0	0	1	1	0	0	1	0	1	0	0	1	0	0	0	1
33	K33	H	H	L	567.25	606.15	606.125	−25	4849	1	0	0	1	0	1	1	1	1	0	0	0	1	1	0	0	1	0	1	1	0	1	0	0	0	1
34	K34	H	H	L	575.25	614.15	614.125	−25	4913	1	0	0	1	1	0	0	1	1	0	0	0	1	1	0	0	1	1	0	0	0	1	0	0	0	1
35	K35	H	H	L	583.25	622.15	622.125	−25	4977	1	0	0	1	1	0	1	1	1	0	0	0	1	1	0	0	1	1	0	1	0	1	0	0	0	1
36	K36	H	H	L	591.25	630.15	630.125	−25	5041	1	0	0	1	1	1	1	0	1	0	0	0	1	1	0	0	1	1	1	0	0	1	0	0	0	1
37	K37	H	H	L	599.25	638.15	638.125	−25	5105	1	0	0	1	1	1	1	1	1	0	0	0	1	1	0	0	1	1	1	1	0	1	0	0	0	1
38	K38	H	H	L	607.25	646.15	646.125	−25	5169	1	0	1	0	0	0	0	1	1	0	0	0	1	1	0	1	0	0	0	0	0	1	0	0	0	1
39	K39	H	H	L	615.25	654.15	654.125	−25	5233	1	0	1	0	0	0	1	1	1	0	0	0	1	1	0	1	0	0	0	1	0	1	0	0	0	1
40	K40	H	H	L	623.25	662.15	662.125	−25	5297	1	0	1	0	0	1	0	1	1	0	0	0	1	1	0	1	0	0	1	0	0	1	0	0	0	1
41	K41	H	H	L	631.25	670.15	670.125	−25	5361	1	0	1	0	0	1	1	1	1	0	0	0	1	1	0	1	0	0	1	1	0	1	0	0	0	1
42	K42	H	H	L	639.25	678.15	678.125	−25	5425	1	0	1	0	1	0	0	1	1	0	0	0	1	1	0	1	0	1	0	0	0	1	0	0	0	1
43	K43	H	H	L	647.25	686.15	686.125	−25	5489	1	0	1	0	1	0	1	1	1	0	0	0	1	1	0	1	0	1	0	1	0	1	0	0	0	1
44	K44	H	H	L	655.25	694.15	694.125	−25	5553	1	0	1	0	1	1	0	1	1	0	0	0	1	1	0	1	0	1	1	0	0	1	0	0	0	1
45	K45	H	H	L	663.25	702.15	702.125	−25	5617	1	0	1	0	1	1	1	1	1	0	0	0	1	1	0	1	0	1	1	1	0	1	0	0	0	1
46	K46	H	H	L	671.25	710.15	710.125	−25	5681	1	0	1	1	0	0	0	1	1	0	0	0	1	1	0	1	1	0	0	0	0	1	0	0	0	1
47	K47	H	H	L	679.25	718.15	718.125	−25	5745	1	0	1	1	0	0	1	1	1	0	0	0	1	1	0	1	1	0	0	1	0	1	0	0	0	1
48	K48	H	H	L	687.25	726.15	726.125	−25	5809	1	0	1	1	0	1	0	1	1	0	0	0	1	1	0	1	1	0	1	0	0	1	0	0	0	1
49	K49	H	H	L	695.25	734.15	734.125	−25	5873	1	0	1	1	0	1	1	1	1	0	0	0	1	1	0	1	1	0	1	1	0	1	0	0	0	1
50	K50	H	H	L	703.25	742.15	742.125	−25	5937	1	0	1	1	1	0	0	1	1	0	0	0	1	1	0	1	1	1	0	0	0	1	0	0	0	1

ROM occupation

Indicated number	Channel designation	Band selection output UHF	Band selection output VHF	Band selection output BD 3	Vision - carrier / MHz	Oscillator frequency theoretical/MHz	Oscillator frequency actual/MHz	Deviation ⊥f/kHz	Divider factor decimal	Divider factor binary 2^{12} 2^{11} 2^{10} 2^{9} 2^{8} 2^{7} 2^{6} 2^{5} 2^{4} 2^{3} 2^{2} 2^{1} 2^{0}	13 12 11 10 9 8 7 6 5 4 3 2 1	Divider factor ROM 13 12 11 10 9 8 7 6 5 4 3 2 1
51	K51	H	H	L	711.25	750.15	750.125	−25	6001	1 0 1 1 1 0 1 1 1 0 0 0 1	1 0 1 1 1 0 1 0 1 0 0 0 1
52	K52	H	H	L	719.25	758.15	758.125	−25	6065	1 0 1 1 1 1 1 0 1 1 0 0 1	1 0 1 1 1 1 1 0 0 1 0 0 1
53	K53	H	H	L	727.25	766.15	766.125	−25	6129	1 0 1 1 1 1 1 1 1 1 0 0 1	1 0 1 1 1 1 1 1 0 1 0 0 1
54	K54	H	H	L	735.25	774.15	774.125	−25	6193	1 1 0 0 0 0 0 0 1 1 0 0 1	1 1 0 0 0 0 0 0 0 1 0 0 1
55	K55	H	H	L	734.25	782.15	782.125	−25	6257	1 1 0 0 0 0 1 1 1 1 0 0 1	1 1 0 0 0 0 1 0 1 1 0 0 1
56	K56	H	H	L	751.25	790.15	790.125	−25	6321	1 1 0 0 0 1 0 1 1 1 0 0 1	1 1 0 0 0 1 0 0 1 1 0 0 1
57	K57	H	H	L	759.25	798.15	798.125	−25	6385	1 1 0 0 0 1 1 1 1 1 0 0 1	1 1 0 0 0 1 1 0 1 1 0 0 1
58	K58	H	H	L	767.25	806.15	806.125	−25	6449	1 1 0 0 1 0 0 1 1 1 0 0 1	1 1 0 0 1 0 0 0 1 1 0 0 1
59	K59	H	H	L	775.25	814.15	814.125	−25	6513	1 1 0 0 1 0 1 1 1 1 0 0 1	1 1 0 0 1 0 1 0 1 1 0 0 1
60	K60	H	H	L	783.25	822.15	822.125	−25	6577	1 1 0 0 1 1 0 1 1 1 0 0 1	1 1 0 0 1 1 0 0 1 1 0 0 1
61	K61	H	H	L	791.25	830.15	830.125	−25	6641	1 1 0 0 1 1 1 1 1 1 0 0 1	1 1 0 0 1 1 1 0 1 1 0 0 1
62	K62	H	H	L	799.25	838.15	838.125	−25	6705	1 1 0 1 0 0 0 1 1 1 0 0 1	1 1 0 1 0 0 0 0 1 1 0 0 1
63	K63	H	H	L	807.25	846.15	846.125	−25	6769	1 1 0 1 0 0 1 1 1 1 0 0 1	1 1 0 1 0 0 1 0 1 1 0 0 1
64	K64	H	H	L	815.25	854.15	854.125	−25	6833	1 1 0 1 0 1 0 1 1 1 0 0 1	1 1 0 1 0 1 0 0 1 1 0 0 1
65	K65	H	H	L	823.25	862.15	862.125	−25	6897	1 1 0 1 0 1 1 1 1 1 0 0 1	1 1 0 1 0 1 1 0 1 1 0 0 1
66	K66	H	H	L	831.25	870.15	870.125	−25	6961	1 1 0 1 1 0 0 1 1 1 0 0 1	1 1 0 1 1 0 0 0 1 1 0 0 1
67	K67	H	H	L	839.25	878.15	878.125	−25	7025	1 1 0 1 1 0 1 1 1 1 0 0 1	1 1 0 1 1 0 1 0 1 1 0 0 1
68	K68	H	H	L	847.25	886.15	886.125	−25	7089	1 1 0 1 1 1 0 1 1 1 0 0 1	1 1 0 1 1 1 0 0 1 1 0 0 1
69	K69	H	H	L	885.25	894.15	894.125	−25	7153	1 1 0 1 1 1 1 1 1 1 0 0 1	1 1 0 1 1 1 1 0 1 1 0 0 1
70	ex.	H	H	L	863.25	902.15	902.125	−25	7217	1 1 1 0 0 0 0 0 1 1 0 0 1	1 1 1 0 0 0 0 0 0 1 0 0 1
71	ex.	H	H	L	871.25	910.15	910.125	−25	7281	1 1 1 0 0 0 1 1 1 1 0 0 1	1 1 1 0 0 0 1 0 1 1 0 0 1
72	ex.	H	H	L	879.25	918.15	918.125	−25	7345	1 1 1 0 0 1 0 1 1 1 0 0 1	1 1 1 0 0 1 0 0 1 1 0 0 1
73	ex.	H	H	L	887.25	926.15	926.125	−25	7409	1 1 1 0 0 1 1 1 1 1 0 0 1	1 1 1 0 0 1 1 0 1 1 0 0 1
74	ex.	H	L	H	69.25	108.15	108.125	−25	865	0 0 0 1 1 0 1 1 0 0 0 0 1	0 0 0 1 1 0 1 0 0 0 0 0 1
75	ex.	H	L	H	76.25	115.15	115.125	−25	921	0 0 0 1 1 1 0 0 1 1 0 0 1	0 0 0 1 1 0 1 1 1 1 0 0 1

ROM occupation

Indicated number	Channel designation	Band selection output UHF	Band selection output VHF BD 3	Vision - carrier / MHz	Oscillator frequency theoretical/MHz	Oscillator frequency actual/MHz	Deviation Δf/kHz	Divider factor decimal	Divider factor binary 2^{12} 2^{11} 2^{10} 2^{9} 2^{8} 2^{7} 2^{6} 2^{5} 2^{4} 2^{3} 2^{2} 2^{1} 2^{0}	13 12 11 10 9 8 7 6 5 4 3 2 1	Divider factor ROM 13 12 11 10 9 8 7 6 5 4 3 2 1
76	ex.	H	L H	83.25	122.15	122.125	−25	977	0 0 0 1 1 1 1 0 1 0 0 0 1	0 0 0 1 1 1 1 0 1 1 0 0 1	0 0 0 1 1 1 0 1 1 0 0 0 1
77	ex.	H	L H	90.25	129.15	129.125	−25	1033	0 0 1 0 0 0 0 0 0 1 0 0 1	0 0 0 1 1 1 1 1 1 0 1 0 0 1	0 0 0 1 1 1 1 1 1 0 1 0 0 1
78	ex.	H	L H	97.25	136.15	136.125	−25	1089	0 0 1 0 0 0 1 0 0 0 0 0 1	0 0 1 0 0 0 0 1 0 0 0 0 1	0 0 1 0 0 0 0 1 0 0 0 0 1
79	20IR	H	L H	59.25	98.15	98.125	−25	785	0 0 0 1 1 0 0 0 1 0 0 0 1	0 0 0 1 0 1 1 1 1 1 0 0 1	0 0 0 1 0 1 1 1 1 1 0 0 1
80	50IR	H	L H	93.25	132.15	132.125	−25	1057	0 0 1 0 0 0 0 0 1 0 0 0 1	0 0 1 0 0 0 0 0 0 0 0 0 1	0 0 1 0 0 0 0 0 0 0 0 0 1
81	S1	L	L H	105.25	144.15	144.125	−25	1153	0 0 1 0 0 1 0 0 0 0 0 0 1	0 0 1 0 0 0 1 1 0 0 0 0 1	0 0 1 0 0 0 1 1 0 0 0 0 1
82	S2	L	L H	112.25	151.15	151.125	−25	1209	0 0 1 0 0 1 0 1 1 1 0 0 1	0 0 1 0 0 1 0 0 1 1 0 0 1	0 0 1 0 0 1 0 0 1 1 0 0 1
83	S3	L	L H	119.25	158.15	158.125	−25	1265	0 0 1 0 0 1 1 1 1 0 0 0 1	0 0 1 0 0 1 1 0 1 0 0 0 1	0 0 1 0 0 1 1 0 1 0 0 0 1
84	S4	L	L H	126.25	165.15	165.125	−25	1321	0 0 1 0 1 0 0 1 0 1 0 0 1	0 0 1 0 1 0 0 0 0 1 0 0 1	0 0 1 0 1 0 0 0 0 1 0 0 1
85	S5	L	L H	133.25	172.15	172.125	−25	1377	0 0 1 0 1 0 1 1 0 0 0 0 1	0 0 1 0 1 0 1 0 0 0 0 0 1	0 0 1 0 1 0 1 0 0 0 0 0 1
86	S6	L	L H	140.25	179.15	179.125	−25	1433	0 0 1 0 1 1 0 0 1 1 0 0 1	0 0 1 0 1 0 1 1 1 1 0 0 1	0 0 1 0 1 0 1 1 1 1 0 0 1
87	S7	L	L H	147.25	186.15	186.125	−25	1489	0 0 1 0 1 1 1 0 1 0 0 0 1	0 0 1 0 1 1 0 1 1 0 0 0 1	0 0 1 0 1 1 0 1 1 0 0 0 1
88	S8	L	L H	154.25	193.15	193.125	−25	1545	0 0 1 1 0 0 0 0 0 1 0 0 1	0 0 1 0 1 1 1 1 0 1 0 0 1	0 0 1 0 1 1 1 1 0 1 0 0 1
89	S9	L	L H	161.25	200.15	200.125	−25	1601	0 0 1 1 0 0 1 0 0 0 0 0 1	0 0 1 1 0 0 0 1 0 0 0 0 1	0 0 1 1 0 0 0 1 0 0 0 0 1
90	S10	L	L H	168.25	207.15	207.125	−25	1657	0 0 1 1 0 0 1 1 1 1 0 0 1	0 0 1 1 0 0 1 0 1 1 0 0 1	0 0 1 1 0 0 1 0 1 1 0 0 1
91	S11	L	L H	231.25	270.15	270.125	−25	2161	0 1 0 0 0 0 1 1 1 0 0 0 1	0 1 0 0 0 0 1 0 1 0 0 0 1	0 1 0 0 0 0 1 0 1 0 0 0 1
92	S12	L	L H	238.25	277.15	277.125	−25	2217	0 1 0 0 0 1 0 1 0 1 0 0 1	0 1 0 0 0 1 0 0 0 1 0 0 1	0 1 0 0 0 1 0 0 0 1 0 0 1
93	S13	L	L H	245.25	284.15	284.125	−25	2273	0 1 0 0 0 1 1 1 0 0 0 0 1	0 1 0 0 0 1 1 0 0 0 0 0 1	0 1 0 0 0 1 1 0 0 0 0 0 1
94	S14	L	L H	252.25	291.15	291.125	−25	2329	0 1 0 0 1 0 0 0 1 1 0 0 1	0 1 0 0 0 1 1 1 1 1 1 0 0 1	0 1 0 0 0 1 1 1 1 1 1 0 0 1
95	S15	L	L H	259.25	298.15	298.125	−25	2385	0 1 0 0 1 0 1 0 1 0 0 0 1	0 1 0 0 1 0 0 1 1 0 0 0 1	0 1 0 0 1 0 0 1 1 0 0 0 1
96	S16	L	L H	266.25	305.15	305.125	−25	2441	0 1 0 0 1 1 0 0 0 1 0 0 1	0 1 0 0 1 0 1 1 0 1 0 0 1	0 1 0 0 1 0 1 1 0 1 0 0 1
97	S17	L	L H	273.25	312.15	312.125	−25	2497	0 1 0 0 1 1 1 0 0 0 0 0 1	0 1 0 0 1 1 0 1 0 0 0 0 1	0 1 0 0 1 1 0 1 0 0 0 0 1
98	S18	L	L H	280.25	319.15	319.125	−25	2553	0 1 0 0 1 1 1 1 1 1 0 0 1	0 1 0 0 1 1 1 0 1 1 0 0 1	0 1 0 0 1 1 1 0 1 1 0 0 1
99	S19	L	L H	287.25	326.15	326.125	−25	2609	0 1 0 1 0 0 0 1 1 0 0 0 1	0 1 0 1 0 0 0 0 1 0 0 0 1	0 1 0 1 0 0 0 0 1 0 0 0 1
00	S20	L	L H	294.25	333.15	333.125	−25	2665	0 1 0 1 0 0 1 1 0 1 0 0 1	0 1 0 1 0 0 1 0 0 1 0 0 1	0 1 0 1 0 0 1 0 0 1 0 0 1

MOS circuit

General features

- Electrically wordwise reprogrammable, nonvolatile memory in floating-gate technology
- Memory capacity 16 words of 14 or 16 bits each (224 or 256 bit EAROM) pin-programmable
- Data input and output serially via separated inputs and outputs
- Address input in parallel via 4 inputs
- No determination of erase and write duration with external RC networks
- N-channel silicon gate technology
- Nonvolatile data storage for more than 10 years
- Unlimited number of read cycles without refresh, number of reprogrammings $> 10^3$
- Programming within 1 second
- Typical application: tuning memory

Type	Ordering code	Package outline
SDA 5650 F	Q67100-Q247 F	DIP 18

Maximum ratings (all voltages referred to V_{SS})

Supply voltage	$V_{DD\,12\text{-}1}$	21	V
Supply voltage	$V_{PH\,7\text{-}1}$	40	V
Supply voltage	$V_{PI\,9\text{-}1}$	21	V
Input voltage	V_i	16	V
Total power dissipation	P_{tot}	400	mW
Thermal resistance (system-air)	$R_{th\,SA}$	80	K/W
Storage temperature range	T_{stg}	−40 to 125	°C

Range of operation (referred to V_{SS})

Supply voltage range	$V_{DD\,12}$	14 to 16	V
Ambient temperature range	T_{amb}	0 to 70	°C

Static characteristics (all voltages referred to V_{SS} = 0 V)

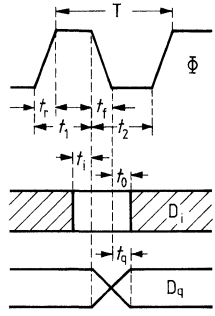
		min	typ	max	
Supply current	$I_{DD\,12}$		10	20	mA
Substrate bias	$-V_{BB\,1}$	4		5	V
Substrate current[1])	$-I_{BB\,1}$			100	µA
Substrate current[2])					
average current	$I_{BB\,1a}$		0.5	2	mA
peak pulse current	$I_{BB\,1p}$			10	mA
Programming voltage	$V_{PP\,7}$		33	35	V
Programming current[1]) (switchable)	$I_{PP\,7}$			300	µA
Programming current[2])					
average current	$I_{PP\,7a}$		1	2	mA
peak pulse current	$I_{PP\,7p}$		5	10	mA
Write voltage (> 13 V by the read process)	$V_{PI\,9}$		15	16	V
Write current[1]) (V_{PI} > 13 V)	$I_{PI\,9}$			100	µA
Write current[2])					
average current	$I_{PI\,9a}$		5	20	mA
peak pulse current	$I_{PI\,9p}$		15	50	mA
Inputs A_1, A_2, A_3, A_4, D_E, Φ, B, ST, PCM, PR	V_L	0		0.5	V
(Pins 5, 4, 3, 2, 15, 13, 14, 16, 18, 8)	V_H	4		V_{DD}	V
	I_H			10	µA
B (pin 14) (V_L = 0 V)	$-I_L$			300	µA
PR (pin 8) (V_L = 0 V)	$-I_L$			200	µA
($V_H = V_{DD}$)	$+I_H$			200	µA
Outputs (open drain) L, POR, D_A (pins 17, 6, 11)					
V_0 = 0.5 V	I_L			0.5	mA
$V_0 = V_{DD}$	I_H			10	µA

[1]) Quiescent condition, read process
[2]) During a reprogramming operation

Dynamic characteristics

		min	typ	max	
Switching times					
Clock signal Φ	$T = t_1 + t_2$	100			µs
	t_1, t_2	20			µs
	t_r, t_f			10	µs
D_i (data input)	t_i	10			µs
D_i (data input)	t_0	70			µs
D_q (data output)	t_q			70	µs
Total erase — write time[1]) (V_{PI} = 15 V; V_{PP} = 33 V)	t_{prog}			1	s
Programming frequency	f_{prog}			1	Hz

[1]) without the part for the data input



Circuit description

Read operation (fig. 1)

The read operation is initialized with the transition of the external signal PCM from high to low at the time $t = t_0$. The address information has to be stable for at least 10 seconds prior to and after t_0. After $t_0 + 10$ seconds, all address inputs as well as the control input are blocked as long as the PCM signal is low. The data output D_q is low-ohmic as long as PCM remains low. At a time $t_1 > 50$ µsec, the first written data bit of the selected 14 (16) bit word is available at the output. The further data bits are clocked each by the falling edge of 14 (16) positive clock pulses.

After having finished the read operation — with the transition of the external signal PCM from low to high — the address lines and control lines are again enabled.

Rewrite operation (fig. 2)

The write operation is initialized with the transition of the external signal ST from high to low (at least for 50 µsec) at the time $t = t_0$. The address information has to be stable for at least 10 seconds prior to and after t_0. At the time t_0 the memory outputs a signal L from low to high as long as the rewrite operation lasts. This signal blocks the address, the PCM, and the control (ST) input.

After a time $t_1 > 50$ µsec the data information can be written into the data shift register with 14 (16) clock pulses. Data carry takes place at the negative edges of the positive clock pulses.

With the aid of internal control inside the memory, the reprogramming begins, as soon as data transfer after the 14^{th} (16^{th}) clock pulse has been finished. The end of write operation is also determined with internal control. It is indicated at the control output L by the transition from high to low.

After programming, the ST input remains blocked, it is only again released by a leading edge at the PCM input (repetitive blocking for programming at too long pressing of the store button).

Reset

The memory remains in the reset condition as long as the input PR is low. During reset also the output POR is low.

Word length

A connection between input B and ground V_{SS} results in an extended word length from 14 to 16 bits. In the open state the shorter word length is set through an integrated pull-up resistor.

Pin designation

Pin No.	Symbol	Function
1	V_{BB}	Substrate bias
2	A_4	Address 4 (input)
3	A_3	Address 3 (input)
4	A_2	Address 2 (input)
5	A_1	Address 1 (input)
6	POR	Reset output
7	V_{PP}	Programming voltage
8	PR	Reset input
9	V_{PI}	Write current
10	V_{SS}	Ground
11	D_q	Data output
12	V_{DD}	Operating voltage
13	Φ	Clock signal (input)
14	B	Switching between 16 and 14 bits
15	D_i	Data input
16	ST	Reprogramming signal (input, active low)
17	L	Programming — condition signal (output)
18	PCM	Read signal (input, active low)

Fig. 1 Read operation

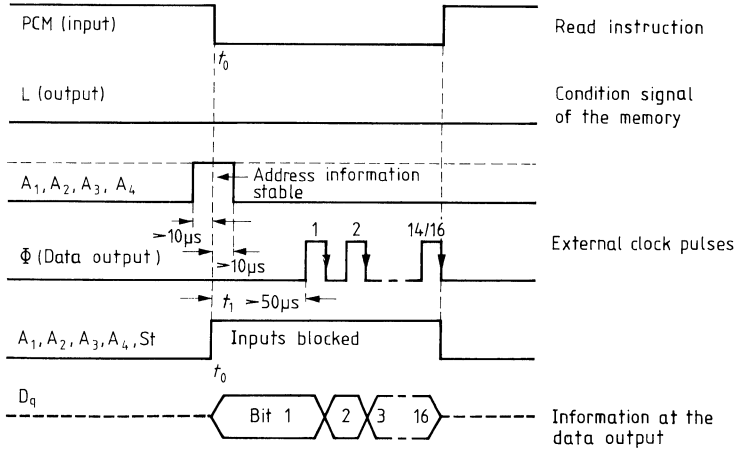
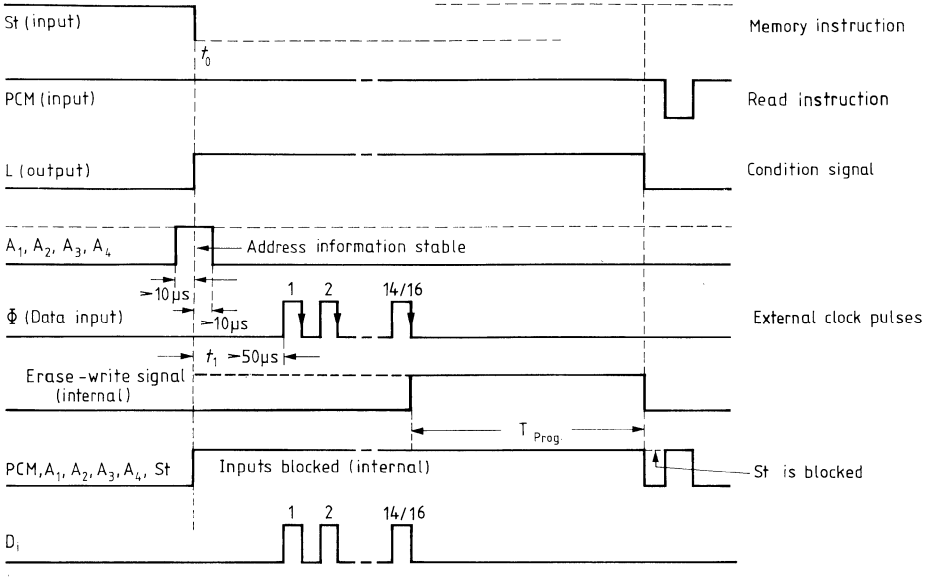
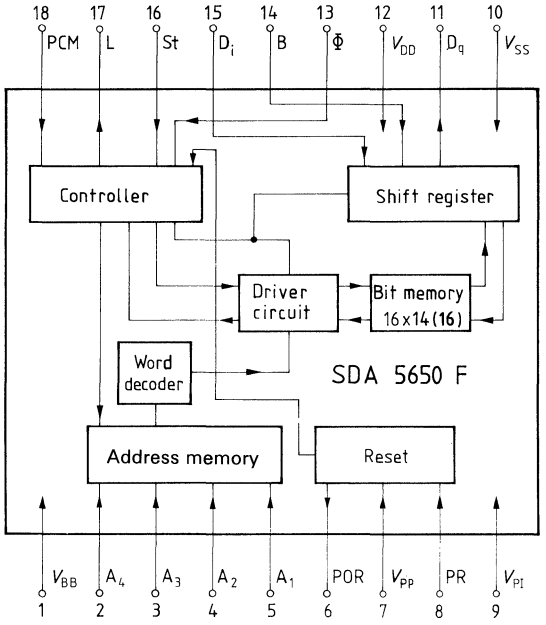


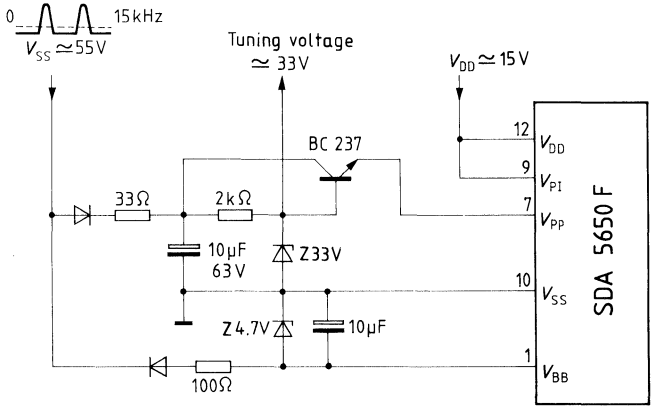
Fig. 2 Erase-write operation



Block diagram



Supply voltage for tuning memory in TV sets



Description of the system

A digital tuning system essentially consists of 3 blocks.

Frequency synthesis
Controller and display
Station memory

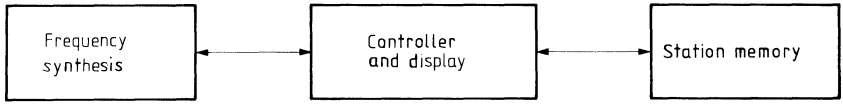


Fig. 1

Frequency synthesis

The desired frequencies are generated according to the PLL principle (Fig. 2). The PLL comprises a VCO (the equivalent tuner oscillator), a prescaler with fixed divider factor P, a divider with digitally selectable divider factor N, a phase detector, and an integrator. The reference frequency for the phase detector can be obtained from a crystal oscillator with following divider (divider factor Q).

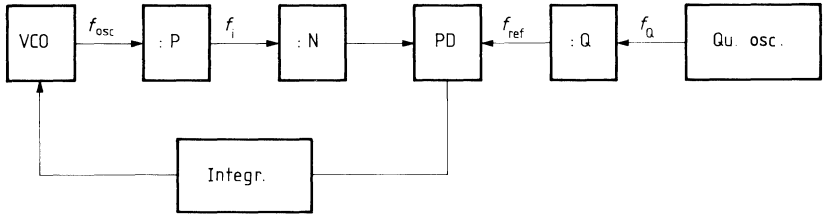


Fig. 2

The selection of the parameter is as follows:

1. VCO frequency range $f_{osc.\,min}$, $f_{osc.\,max}$,
2. Necessary frequency raster Δf
3. Max. permissible tuning time and noise phase shift.

In TV applications a frequency raster of $\Delta f = 125$ kHz is sufficient. Therefore it follows that

$N_{min} = \frac{f_{osc.\,min}}{\Delta f}$ and $N_{max} = \frac{f_{osc.\,max}}{\Delta f}$.

Hence a 13 bit programmable divider N = 2 . . . . . 8191 is required. The reference frequency f_{ref} decisively determines the tuning time and the noise phase shift of the oscillator. It results from the frequency raster Δf and the prescaler factor P: $f_{ref} = \frac{\Delta f}{P}$.

On the other hand, the prescaler factor P determines the max. input frequency for the programmable divider $f_{imax} = \frac{f_{osc.\,max}}{P}$.

The reference frequency f_{ref} is obtained from an oscillator $f_{ref} = \frac{f_Q}{Q}$.

Hence, it follows: $f_{osc} = \frac{PN}{Q} \cdot f_Q$.

In the given system P = 64, Q = 2048, and $f_Q = 4$ MHz have been determined.

The reference frequency thus results in: $f_{ref} = \frac{\Delta f}{P} = \frac{f_Q}{Q} = 1.953125$ kHz.

1. The prescaler SDA 2001

is an ECL divider with a fixed divider factor P = 64. The max. input frequency is 1 GHz.

A broadband preamplifier with 20 dB gain and separated switchover inputs for VHF and UHF is integrated in the SDA 2001.

To ensure reliable operation, the sinusoidal input voltage covering a frequency range between 80 and 1000 MHz should be $V_i = 20$ mV.

The push-pull outputs result in good noise immunity against cross talking. The output levels of 1 V_{pp} only cause low noise radiation.

2. The PLL IC SDA 2002

The IC contains a 13 bit binary programmable synchronous divider (divider factor N = 256 . . . . . 8191), a 16 bit shift register, a quartz oscillator ($f_{osc} = 4$ MHz) with following divider stage (divider factor Q = 2048), and a frequency and phase sensitive digital phase detector. Together with the 3-bit information "VHF Bd I", "VHF Bd III" and "UHF" the divider factor N is serially mored in the 16 bit dual code into the 16 bit shift register with parallel output. First the LSB (least significant bit) is put in, at least the MSB (most s.b.) as last bit. The transition at information input (IFO) is done only during the H state of the enable input (PLE).

The infeeding is done with the L-H slope of the clock (CPL). A 16-bit buffer memory follows the 16-bit shift register. The information transition into the buffer is done with the L-level of the enable input (PLE). Referred to the H-L trailing edge of the enable input only the last 16 clocks are interpreted. Possibly preceding dummy bits will not be interpreted.

A clock with the frequency $f = 62.5$ kHz. Appears at the open collector output C_L. The outputs VHF Bd I, VHF Bd III, and UHF are active low current sources (open collector).

The sync divider has symmetrical push-pull inputs (F, $\overline{F}$) for ECL level.

In the case of frequency and phase synchronization, an L-signal is obtained at the output LOCK IND.

The phase detector can be driven with a separated supply voltage (V_{S2}). The outputs PD and V_D are connected with an RC network. V_D delivers the tuning voltage for the VCO (tuner).

3. The SDA 2003 controller

The integrated MOS circuit, part of the frequenc synthesis tuning system, is located between the programmable divider of the PLL circuit and both the tuning memories which electrically memorize the allocation of the tuning information (fine tuning) and the program number. The controller converts the tuning information into frequency information (divider ratio). The frequency information is a binary number, representing the divider factor for the PLL divider; it is serially transferred into the PLL. Under usual operation, only the station selection buttons of the TV set are actuated.

A fixed program address in the tuning memory is assigned to every static on button. This program address is intended to store the actual tuning information as well as the pertinent channel. After actuating a station button, a program change instruction PC is issued from the remote control receiver or from the front-end keyboard to the controller. This instruction causes the controller to read the tuning information (fine tuning) out of the tuning memory and to assign it to the corresponding channel; hence the TV set is precisely tuned to the requested frequency by means of the PLL.

Setting of a not yet stored TV transmitter is done by means of the actuating buttons:
K 1 for setting of channel units digits and
K 10 for setting of channel tens digits.

By means of the button K 1 the channel number units digits 0 to 9 without carry and by means of the button K 10 the channel number tens digits can be set. After every button operation, the concerned channel number is incremented by 1. For every adjustment of the channel number, the controller converts this information into frequency information (the PLL divider factor) and provides serial output to the PLL circuit. The success of every tuning step can be watched on the screen.

In addition to that, the SDA 2003 is designed for station search, which can also be used for setting a TV channel. The station search is started via the setting button: Search Start SL.

Thereupon the controller sequentially issues every frequency information contained in the internal ROM individually to the PLL circuit. This process is automatically stopped as soon as an operating TV broadcast station is found. This is indicated to the controller by a pulse (active low) at the input "Search STOP", which can be derived from line synchronization and the video signal.

Via the setting buttons "fine tuning plus FT+" and "fine tuning minus FT−" frequency deviations from the rated frequency of the individual channel can be set in steps of 125 kHz up to 3,875 MHz and down to − 4 MHz. Frequency tuning, moreover, readjusts automatically every 250 ms, as soon as the proper button is pressed. Within the tuning limits mentioned above, fine tuning runs against a stop (owerflow inhibit). After having attained it, the channel number display lights up as long as the setting button is kept pressed.

The tuning information of a tuned TV broadcast station can be stored in the tuning memory by actuating the store button. The SDA 2003 then serially outputs the tuning data on the output IFO. The tuning data comprises the fine tuning information and the channel number information.

From the tuning information serially read into the MOS memories, it is the channel number which is used for addressing the internal ROM table. Frequency information from 100 TV channels as well as band selection (2 bytes) are stored in the ROM table.

There are some frequencies to which several TV channels are allocated (stored in the ROM), hence no unambiguous channel designition can be gathered from the frequency. This is the reason why the channel number is used as tuning information, since only in this way unambiguous channel designation and frequency information can be gained, simultaneously.

The frequency information is obtained by adding up the ROM divider factor and the center position of fine tuning. At every process of setting a new channel number, fine tuning is adjusted to center position. The PLL divider factor then complies with the nominal divider factor. The nominal divider factor results in an oscillator frequency lying only by $f = 25$ kHz below the nominal value. It represents the frequency information of the exact channel frequency, except the deviation of 25 kHz which is needed to attain a 125 kHz raster frequency at a given IF of 38.9 MHz. The band selection information is programmed in the internal ROM for every frequency information and is serially output from the controller. Band selection differentiates between VHF range I/III and UHF.

The internal ROM table is made up such that between the CCIR channels — designated with corresponding channel numbers — other channels are allocated. Thus, the Italian TV channels A-H are stored between channel 12 and channel 21 under channel Nos. 13 to 20.

Data communication between the SDA 2003 and the memory is done via a data bus that comprises shift clock $\overline{\text{CNVM}}$, actual information (IFO), and an enable signal (EX/$\overline{\text{REC}}$). The data word contains information on channel number and fine tuning.

4. Display driver SDA 2004

The LED display driver decodes in the remote-controlled tuning system of TV sets the channel and program numbers from a serially offered BCD code and drives in multiplex operation 2 or 4 digits, as required.

The information D (active H) for the four digits is coded in 16 bits and is serially input in two shift registers of 8 bits, each. The input for the digits D_1 and D_2 and/or D_3 and D_4 is provided by 8 falling edges of the driving clock pulses T_{12} or T_{34}, respectively, if Enable EN is on high level. The contents of both the shift registers is stored in an eight bit broad memory, if EN is on low level. The 16 memory outputs operate on a multiplexer. The multiplexer and the digit selection outputs $\overline{\text{DI}_1}$, $\overline{\text{DI}_2}$, $\overline{\text{DI}_3}$ and $\overline{\text{DI}_4}$ (digit driver for the LED displays, active low) are serviced by an internal clock generator. The 7 outputs of the de-

coder, series-connected to the multiplexer, are used for driving the segments (active high) in the LEDs.

If input $\overline{DI}_4$ is grounded, the multiplexer only works for the digits 1 and 2. Thereby the duty cycle for the clock pulse of the multiplexer is changed over.

5. On-screen IC SDA 2105

The SDA 2105 IC is intended to display channel and program numbers on the screen of the TV set and is adapted to the SDA 2003 Siemens channel processor.

The on-screen device provides 2 display panels of 2 digits, each, and 1 display panel of 5 digits. The information for the display panels is serially transferred via the DATA line. The display panels are activated via the pertinent ENABLE line.

6. Nonvolatile memory SDA 2006

This IC allows the nonvolatile, wordoriented reprogrammable storage of 32×16 bit words. Thus, up to 32 programs or channels as well as their possible allocations can be stored.

The SDA 2006 is fabricated in the n-channel floating gate technology in order to provide extremely long storage times and as many read-out operations as required refresh.

Addressing and instruction input is done serially and may comprise 8 or 12 bits as required. The entailing erase and write cycles are determined by a complex, chip-internal control.

7. IR remote control receiver SDA 2007

The device is a further development of the types SAB 3209 and SAB 4209. Like those, it utilizes the proven biphase code for IR transmission and, therefore, it can be applied with the SAB 3210 or SDA 2008 as IR instruction generator. It is, in particular, designed for operation in connection with the tuning system SDA 200. The program memory has, therefore, been relocated from the remote control receiver to the channel processor SDA 2003.

Particulars:

2 combined series interfaces with common DATA line for information transfer (leading bit LB = H and 6 information bits A, B, C, D, E, and F). Distinction is made by the enable signals DLE and TE (7 pulses, each, i.e. 1 pulse/bit). Modification is possible through the outputs of the TUS 1/2 flip-flops, thus different groups of equipment such as teletext decoder and the VCR device can be addressed precisely. H level at one of the TUS outputs drops the DLE pulses (DLE = L) out and switches the TE output over to single mode operation. For a better adaptation to a microprocessor the output is now executed by means of $4\ T_{osc}$/bit (64 µs/bit at 62.5 kHz).

During the "standby" status (ON/OFF = H), all outputs of the 4 analog memories VOLU, BRIG, COLO and CONT are kept on L level. Corrective instructions (instruction Nos. 8 to 15) will then not be executed, i.e. the last set status of the analog memories is retained.

The connection VPM, included in the volume memory VOLU, is provided for front end controlling, which acts like the instructions "volume+" and "volume−", respectively.

2 spare outputs, controlled by 2 alternating flip-flops with different quiescent levels open up additional individual applications (e.g. clock time display).

There is, moreover, the possibility to switch over the start bit for IR reception. Thus, two receiver units can be operated in the same room at the same clock frequency independently of each other.

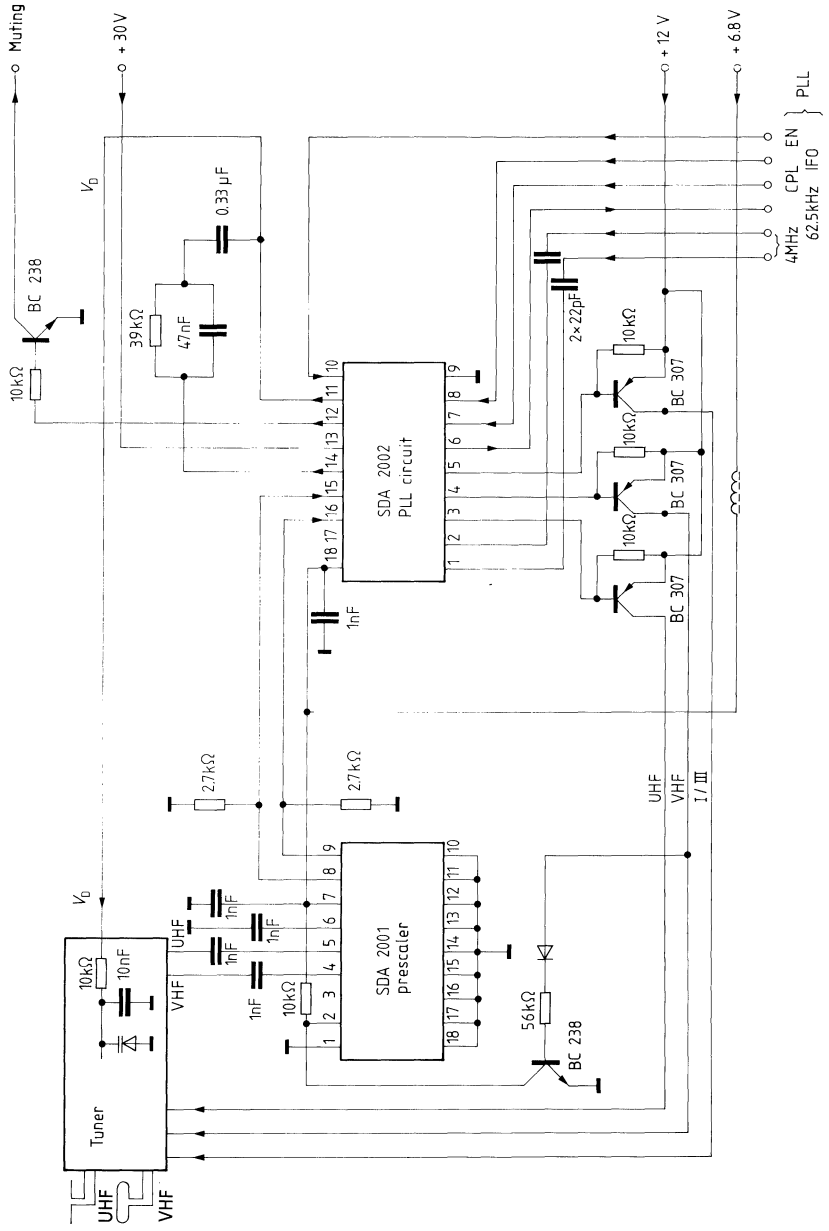
8. Remote control transmitter SDA 2008

The transmitter module SDA 2008 is an advanced product of the SAB 3210 IC within the frame of the IR 60 Siemens infrared remote control system. In detail,the IC includes the following:

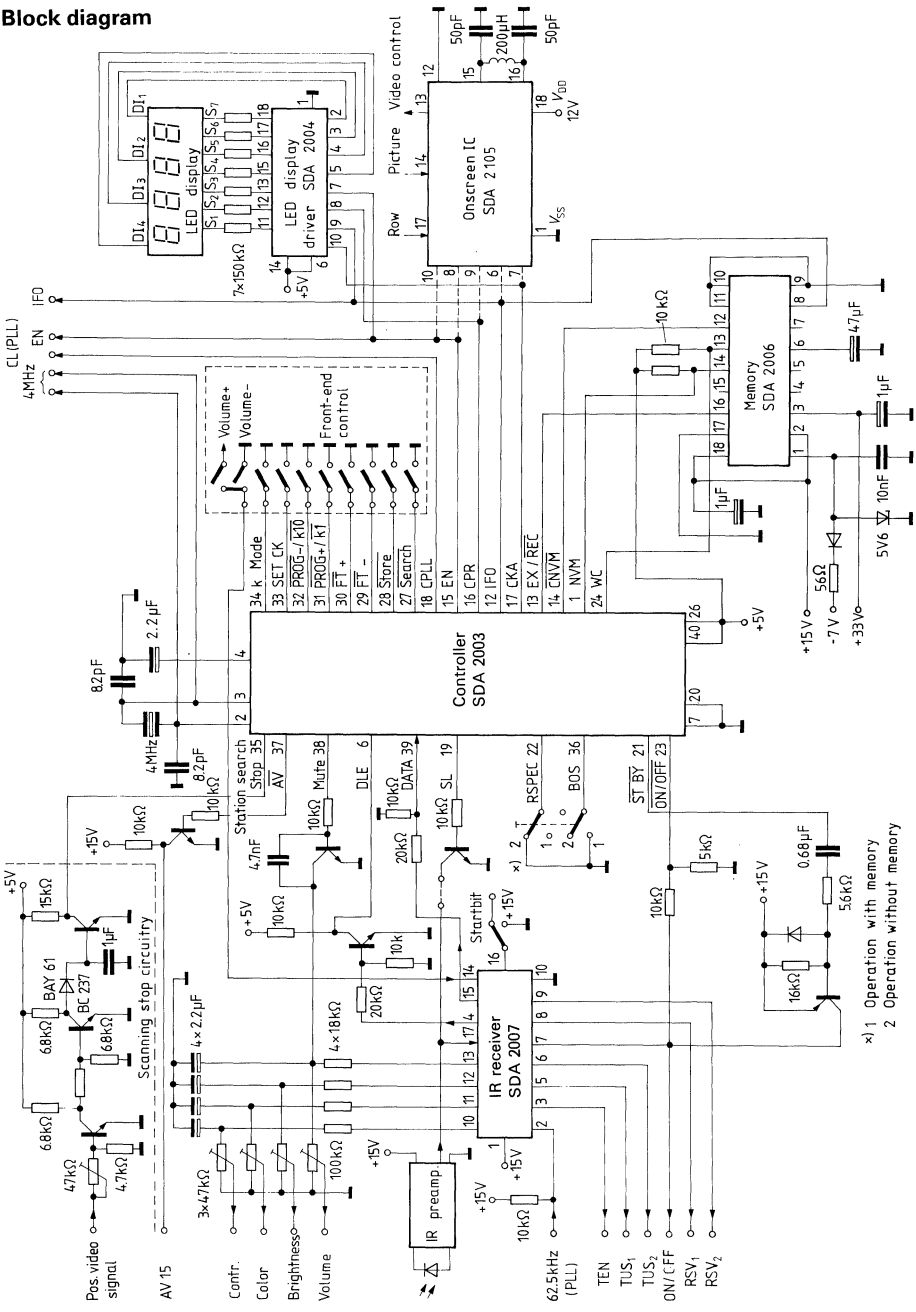
1. The keyboard is completely latched against incorrect operation. Even in case of double operation as provided for instruction input within one column with one of the lines 1 to 7 incl. line 8, practically no misinstruction can be generated by pressing two buttons, since for that both the buttons had to be pressed absolutely simultaneously.
2. After outputting the first information instruction, the instruction can only be changed by switching off the transmitter (releasing all buttons). This avoids further incorrect servicing because no unwanted instruction change can be effected by premature releasing the "shift button" (keyboard changeover) or pressing a further button.
3. Instruction expansion to more than 32 instructions can be done as previously by diode wiring, and recently additionally via a "shift button" (connects PPIN to SA). Moreover, the instructions 40 to 47 can be issued by connecting the line inputs to $-V_S$ without requiring any additional component.
4. The start bit in infrared transmission can be changed over from outside (connecting PPIN to SC). Thus, selective addressing of 2 different receivers by one transmitter is possible. A TV transmitter and a broadcasting set with one transmitter can, therefore, be serviced independently of each other in one room.
5. The oscillator was converted to 8 times the frequency in order to permit operation with a ceramic resonator. Hence, also lowcost AM IF resonators (appr. 500 kHz or 455 kHz) can be used instead of the oscillator.
6. In addition to the hitherto existing final instruction, an "initial instruction" is transmitted. The initial instruction exactly complies with the final instruction, except that it is issued by information instructions.

   Thus separation between 2 button operations can be recognized even more precisely, and more time is provided for the gain control of the preamplifiers on the receiver side.
7. No external column resistors are required.

SDA 200 prescaler and PLL circuit



Block diagram



Bipolar circuit

Fast ECL divider with constant dividing ratio 1 : 64 covering the frequency range from 80 MHz to 1 GHz. The SDA 2001 includes a broadband preamplifier with approx. 20 dB voltage gain and two seperate inputs for UHF and VHF, which can be selected by external dc voltage.

- Input frequency up to 1 GHz
- Integrated preamplifier
- Balanced output in phase opposition

Type	Ordering code	Package outline
SDA 2001	Q67000-A1464	DIP 18

Maximum ratings

Supply voltage	V_S	10	V
Input voltage	$V_{i\,4}$, $V_{i\,5}$	1	V
Output current	$I_{q\,8}$, $I_{q\,9}$	−2.1	mA
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\,SA}$	70	K/W

Range of operation

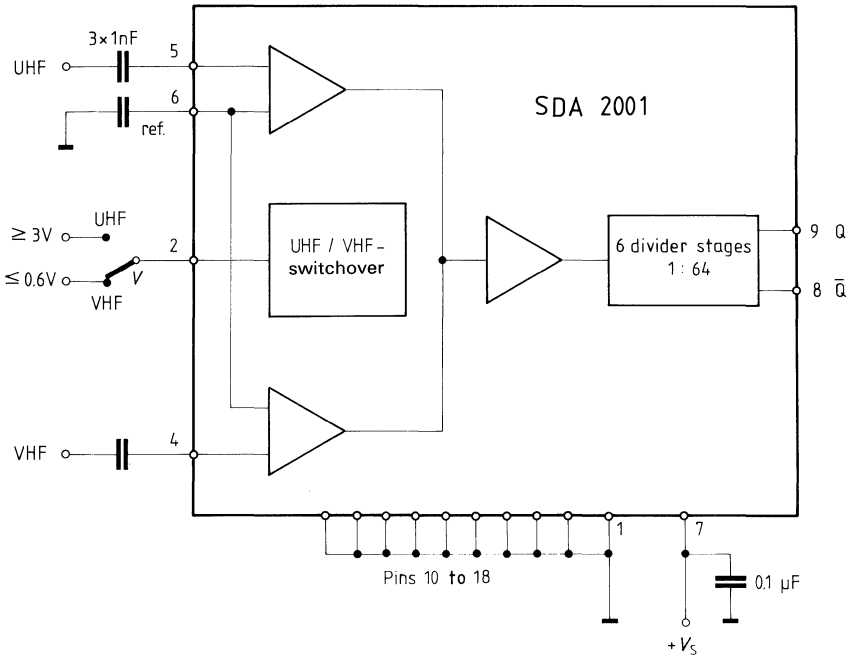
Supply voltage range	V_S	6.45 to 7.15	V
Ambient temperature range	T_{amb}	0 to 70	°C

Characteristics (V_S = 6.8 V; T_{amb} = 25 °C)

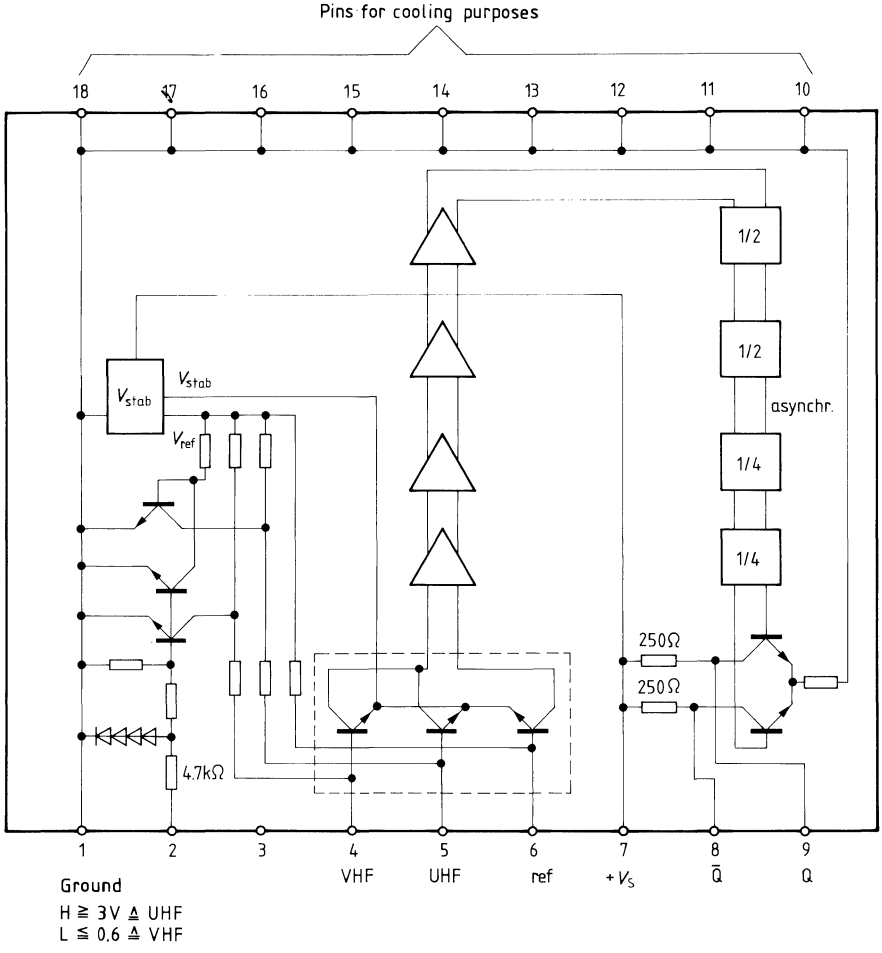
			min	typ	max	
Current consumption		I_7	75	105	140	mA
Input voltage range						
	f_i = 100 MHz	$V_{i\,4}$	35		500	mV
	f_i = 200 MHz	$V_{i\,4}$	20		500	mV
	f_i = 470 MHz	$V_{i\,5}$	20		300	mV
	f_i = 900 MHz	$V_{i\,5}$	35		100	mV
Input frequency	Maximum $f_{i\,max}$	$f_{i\,5}$	950	1100		MHz
	Minimum $f_{i\,min}$	$f_{i\,4}$		60	80	MHz
Output voltage		$V_{q\,8}$, $V_{q\,9}$	600	800	1000	mV_{pp}
L-changeover voltage		$V_{2\,L}$			0.6	V
H-changeover voltage		$V_{2\,H}$	3			V
Changeover current (V_2 = 12 V)		$-I_2$		1.5		mA
Output resistance		R_q		250		Ω

Input voltage ratings are measured with Vector-voltmeter 8405 A at amplifier input.

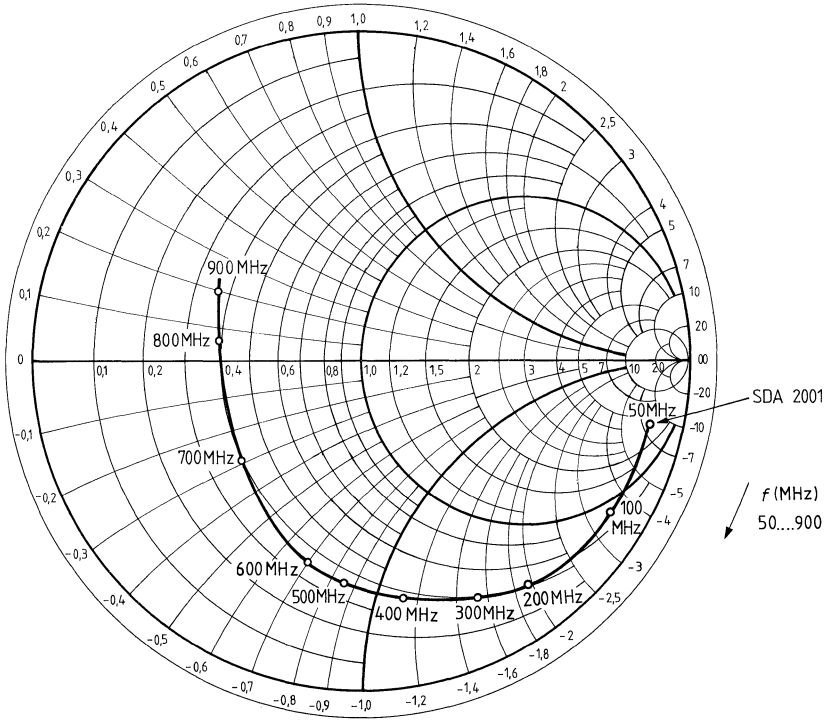
Test circuit



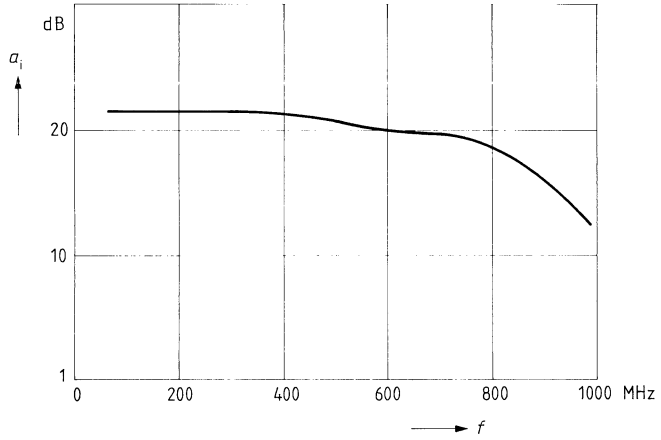
Block diagram incl. internal pin configuration



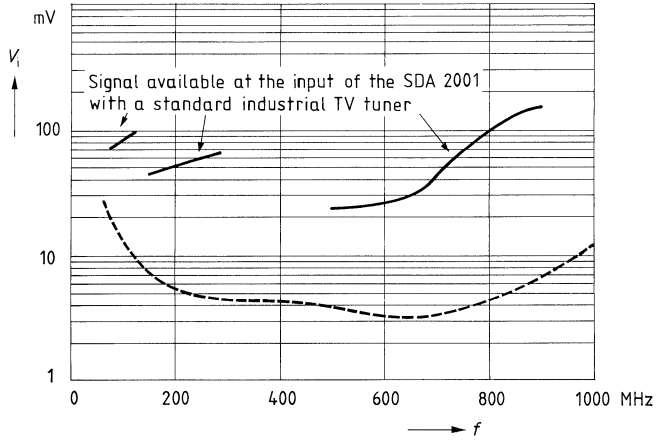
Input impedance behavior versus frequency
Z_0 = 75 Ω, measured asymmetrically



Decoupling of the VHF and UHF input versus input frequency



Input sensitivity versus input frequency



Bipolar circuit

The PLL IC SDA 2002 is part of the frequency synthesis tuning system SDA 200. Together with the frequency divider SDA 2001 and a voltage-controlled oscillator in the tuner, a frequency and phase comparison circuit can be designed. It is intended for channel selection in TV sets.
Programming allows quartz-controlled setting of the oscillator frequency for the television bands I/III/IV/V in 125 kHz raster. The SDA 2002 includes a 13 bit programmable synchronous divider, a 16 bit shift register, a quartz oscillator with subsequent divider, and a frequency and phase sensitive digital phase detector.

- No external integrator necessary
- Internal buffer memory
- Microprocessor compatible

Type	Ordering code	Package outline
SDA 2002	Q67000-A1465	DIP 18

Maximum ratings

Supply voltage 1		$V_{S\,18}$	7.5	V
Supply voltage 2		$V_{S\,13}$	32	V
Input voltage	IFO	$V_{i\,8}$	5.5	V
	PLE	$V_{i\,10}$	5.5	V
	CPL	$V_{i\,7}$	5.5	V
	$\overline{F}$, F	$V_{i\,15}$, $V_{i\,16}$	7.5	V
Output voltage	CL	$V_{q\,6}$	16	V
	Band selection	$V_{q\,3}$, $V_{q\,4}$, $V_{q\,5}$	16	V
Thermal resistance (system-air)		$R_{th\,SA}$	70	K/W
Junction temperature		T_j	140	°C
Storage temperature range		T_{stg}	−40 to 125	°C

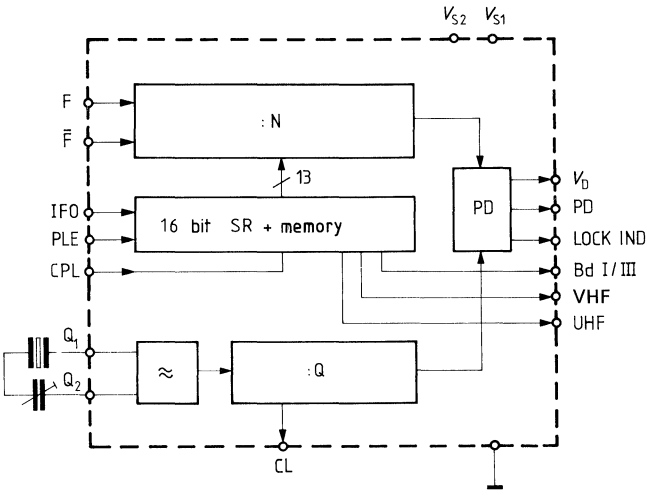
Range of operation

Supply voltage 1 range	$V_{S\,18}$	6.45 to 7.15	V
Supply voltage 2 range	$V_{S\,13}$	3.5 to 31.5	V
Tuning voltage range	$V_{D\,11}$	0.5 to 30	V
Input frequency	$f_{i\,15}$, $f_{i\,16}$	≤ 15	MHz
Ambient temperature range	T_{amb}	0 to 70	°C

Characteristics ($V_{S\,18}$ = 6.8 V; T_{amb} = 25 ° C)

		min	typ	max	
Current consumption	I_{18}		30	40	mA
	I_{13}		1.4	2	mA
Input level	$V_{15\,H}$, $V_{16\,H}$		6.8		V
	$V_{15\,L}$, $V_{16\,L}$		5.8		V
Sensitivity of divider inputs ($f_{i\,15,\,16}$ = 15 MHz)	$V_{i\,15}$, $V_{i\,16}$	600	800	1000	mV_{pp}
Inputs CPL, IFO, PLE					
Upper threshold voltage	$V_{i\,7/8/10\,u}$	1	1.3	1.6	V
Lower threshold voltage	$V_{i\,7/8/10\,l}$	0.5	0.7	1	V
Hysteresis	$V_{i\,7/8/10}$		0.6		V
H-input current ($V_{i\,7/8/10\,H}$ = 5 V; $V_{S\,18}$ = 7.15 V)	$I_{i\,7/8/10\,H}$			8	µA
L-input current ($V_{i\,7/8/10\,L}$ = 0.4 V; $V_{S\,18}$ = 7.15 V)	$I_{i\,7/8/10\,L}$			−50	µA
Inputs IFO, PLE					
Set-up time	t_S	2	1.5		µs
Hold time	t_H	2	1.5		µs
Clock input CPL					
H-pulse width	t_{CH}	2	1.5		µs
L-pulse width	t_{CL}	2	1.5		µs
Clock output CL					
(V_{pp} = 15 V; $R_L \geq$ 6.8 kΩ)					
H-output voltage	$V_{q\,6H}$	14	14.5	15	V
L-output voltage	$V_{q\,6L}$			1.5	V
H-pulse width	t_{TH}		8		µs
L-pulse width	t_{TL}		8		µs
H-L transition time (R_L = 9.5 kΩ)	t_{THL}	0		0.5	µs
L-H transition time (C_L = 50 pF)	t_{TLH}	0		1.5	µs
Phasen detector output PD					
Load current	$I_{14\,LOAD}$		+100		µA
Sink current	$I_{14\,SINK}$		−100		µA
Voltage in case of synchronization	V_{14}		2		V
Band selection output					
H-output voltage (V_{pp} = 15 V)	$I_{q\,3,\,4,\,5\,H}$			10	µA
L-output voltage (2 V ≤ V_{pp} ≤ 15 V)	$I_{q\,3,\,4,\,5\,L}$	0.5	1.2	1.7	mA

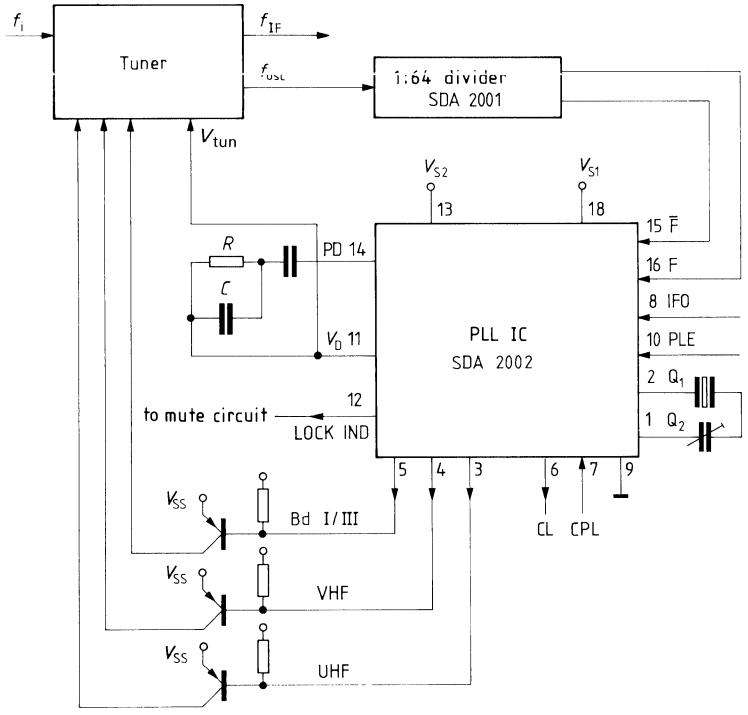
Block diagram



Pin designation

Pin No.	Symbol	Description
1	Q_2	Quartz
2	Q_1	Quartz
3	UHF	} Band selection outputs
4	VHF	
5	Bd I/III	
6	CL	Clock output
7	CPL	Clock input
8	IFO	Data input
9	⊥	Ground
10	PLE	Shift register enable input
11	V_D	Tuning voltage
12	LOCK IND	Lock indication output
13	V_{S2}	Supply voltage phase detector
14	PD	Phase detector voltage
15	$\bar{F}$	Inverted input
16	F	Input
17	open	
18	V_{S1}	Supply voltage

Application circuit (schematic)

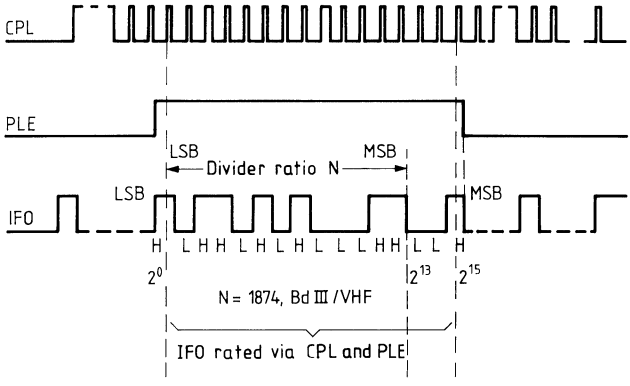


Truth table

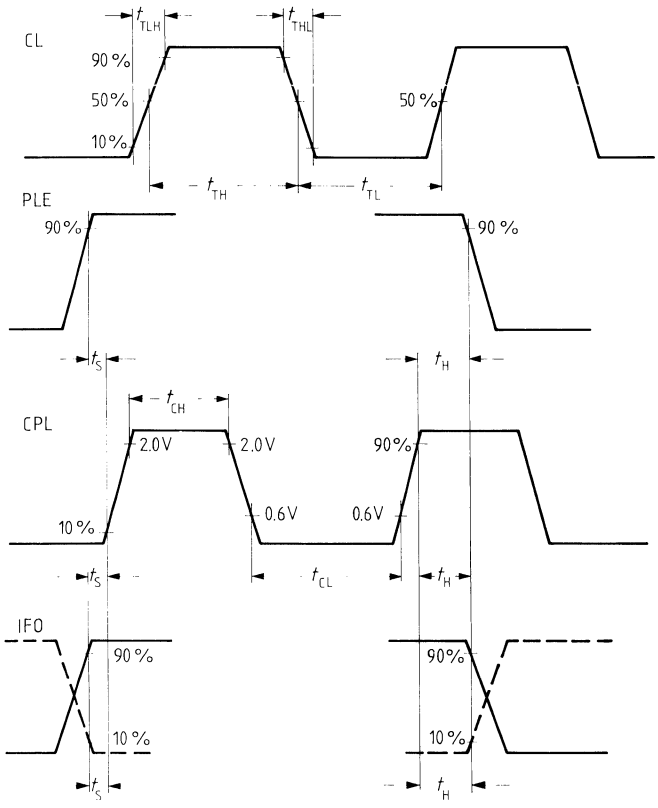
	Input "IFO" Bit			Output			Meaning
	2^{13}	2^{14}	2^{15}	Bd I/III	VHF	UHF	
	H	H	L	H	H	L	"UHF"
	H	L	H	H	L	H	"Bd I/VHF"
	L	L	H	L	L	H	"Bd III/VHF"
or	L	H	H	L	H	H	"Bd III/VHF"

In the case of positive logic, the "IFO"-bits $2^0 \ldots 2^{12}$ are the complement of the dual code from divider ratio N.

Pulse diagram



Pulse diagram



MOS circuit

In the frame of the frequency synthesis tuning system SDA 200, the SDA 2003 8-bit microcomputer takes over the control functions necessary for operation. In case of program or channel selection, the microcomputer has the job to route the relevant frequency information to the programmable divider, or to control the tuning memory, respectively. Precise frequency information for 100 channel numbers of standard B or standard G, CCIR specification, as well as for several channels not included in these specifications, is stored in the ROM of the SDA 2003.

- Program and channel indication on LEDs or onscreened
- Operation with program selection or channel selection as required
- Clock generation by means of a quartz or external clock from PLL
- +5 V supply voltage

Type	Ordering code	Package outline
SDA 2003	Q67120-C32	DIP 40

Maximum ratings (all voltages referred to V_{SS} = 0 V)

Voltage at every pin referred to ground	V	−0.5 to 7	V
Total power dissipation	P_{tot}	1.5	W
Thermal resistance (system-air)	$R_{th\ SA}$	50	K/W
Storage temperature range	T_{stg}	−65 to 150	°C
Operating temperature	T_{amb}	0 to 70	°C

Range of operation (referred to V_{SS} = 0 V)

Supply voltage range	$V_{CC\ 40}$, $V_{DD\ 26}$	4.75 to 5.25	V
Ambient temperature range	T_{amb}	0 to 70	°C

Characteristics (referred to V_{SS} = 0 V)

		min	typ	max	
Current consumption	I_{DD}		65	135	mA
L-input voltage (except pin 2, 3)	V_{iL}	−0.5		0.8	V
H-input voltage (except pin 2, 3, 4)	V_{iH}	2		V_{CC}	V
H-input voltage (except pin 2, 4)	V_{iH}	3		V_{CC}	V
L-output voltage (except pin 12 to 19) I_L = 2.0 mA	V_{qL}			0.45	V
L-output voltage (pin 3, 8, 9, 10, 21, 37, 38) I_L = 1.6 mA	V_{qL}			0.45	V
H-output voltage (pin 12 to 19) I_H = 100 µA	V_{qH}	2.4			V
H-output voltage (pin 3, 8, 9, 10, 21, 37, 38) I_H = 50 µA	V_{qH}	2.4			V
Input leakage current (pin 6, 7, 39) $V_{SS} \leq V_{IN} \leq V_{CC}$	I_R			±10	µA
Input leakage current (pin 1) $V_{CC} \geq V_{IN} \geq V_{SS} + 0.45V$	I_R			−10	µA
Clock frequency	f_{CL}	3.4	4	4.6	MHz
Input signal duration (pin 27 to 32) f_{CL} = 4 MHz	t_{BED}	40			ms
Input signal duration for $\overline{\text{STOP}}$ (35) f_{CL} = 4 MHz	t_{STOP}	270			ms
Delay between $\overline{\text{ONOFF}}$ (23) and $\overline{\text{DLE}}$ (6) f_{CL} = 4 MHz	t_d	−30		+30	ms
Permissible delay of the STOP signal referred to the end of the output to the PLL for correct breaking-off the station search.	$t_{STOP\,SL}$			180	ms
Muting at station search	$t_{MUTE\,1}$		90		ms
	$t_{MUTE\,2}$		180		ms
Muting at program changing	$t_{MUTE\,1}$		90		ms
	$t_{MUTE\,2}$		30		ms

Description of functions

1. Servicing functions in case of front-end control for universal programming (ESPEC)

The specification (ESPEC) makes servicing by IR remote control of every function pertinent to TV set operation feasible. This means that in addition to the so far provided instructions for program selection, analog functions, quick tone, normal positioning, and standby, now also direct channel selection, fine tuning, memorizing, and station search start can be remote controlled.

1.1 Front-end control

The input KMODE differentiates between both the modes of operation: "program selection" and "channel selection" in case of externally interfaced program memory.

1.2 Program selection (30 programs 0 to 29)

The input KMODE has to be on high level (open). Provided an H→L edge at the "Prg +" or "Prg −" inputs, the program number is incremented or decremented by 1, respectively.

1.3 Channel selection

Apply low level to input KMODE, the channel number is then permanently displayed. With the inputs "Prg +" and "Prg −" (which now mean "channel tens" and "channel units") the channel counter can be readjusted in tens or units steps (ring counter in forward direction). This does not include carry from the units to the tens digit.

1.4 Station search

After having applied the low level to the KMODE input, the channel No. is displayed. The station search starts with the input "SLS". On the instruction "station search start" the IC keeps switching the channel No. in an interval of approximately 250 ms; after the channel No. 99, the SDA 2003 restarts with the No. ØØ
The station search is either discontinued by the leading edge of the stop signal, generated by the TV set after a transmitter suitable for reception has been found, or when KMODE of the front-end control has been switched on to program, or when the channel tens or units button has been actuated.
If station search has been stopped by a stop signal it doesn't run any longer even if the stop signal redisappears
Stop = Low
During station search a "High" signal which can be used to block the remote control is provided at the output 19 (SL).

1.5 Fine tuning

As compared to mask-programmed tuning, the tuning range can be changed via the fine tuning buttons "FT +" and "FT −" by +3.875 to −4 MHz. The tuning runs automatically with about 4 steps/sec. into the selected direction up to the stop as long as one of the buttons has been pressed. When the upper or lower "channel limits" are reached the channel indication starts to blink in intervals of 0.5 sec. During tuning, channel indication remains unaffected.

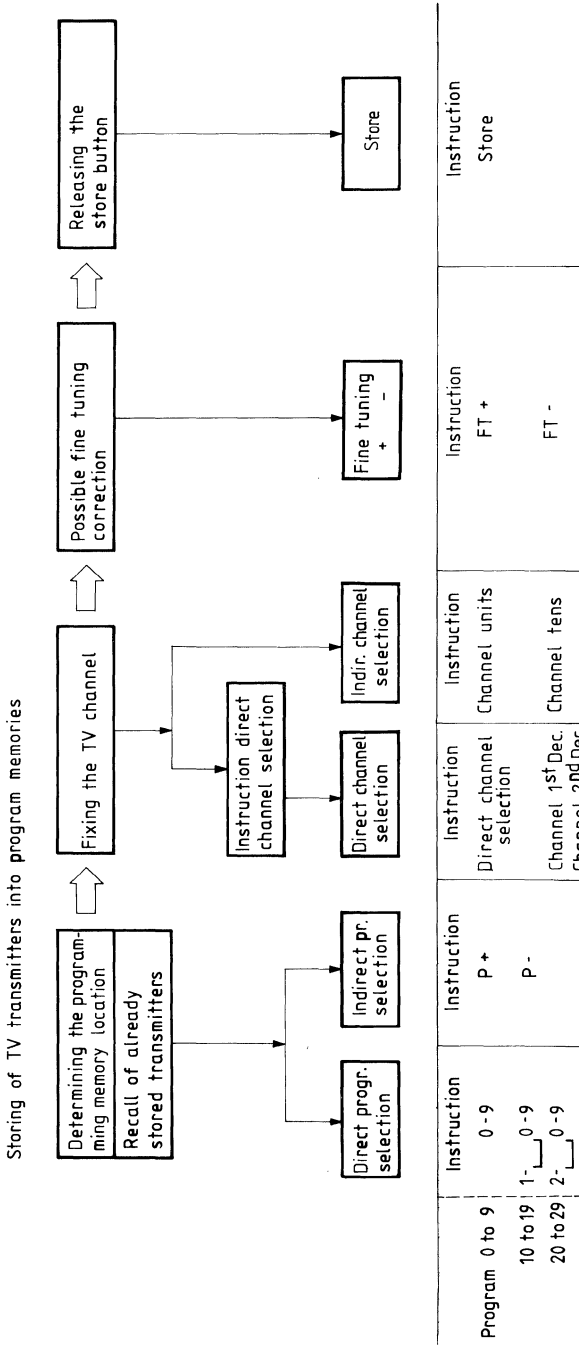
1.6 Storing of a tuning information

A found tuning can be stored on the indicated program number. The store button has to be pressed once, the display remains unaffected.

1.7 Muting circuit

The output "mute" is switched on "high" approximately 100 ms prior to an output of the tuning information up to approximately 20 ms after that.
During station search or when the stop signal is not available, the output "mute" is also switched on "high".

Operating sequence for the SDA 2003



2. Remote control

2.1 Direct channel selection

If the button KAN on the remote control unit is pressed, the device is switched over from program to channel selection mode. Thereby, the actual channel No. is on-screened or indicated on the display, independent of the position of the front-end control mode switch.

If there is no further operation, the SDA 2003 switches back to program selection after 8 sec., whereby channel indication also disappears (front-end control mode switch on program). If program selection is again wanted prior to the course of 8 sec. only an external instruction e.g. analog instruction, quick tone etc., or command "IN" has to be issued.

The same effect is obtained by actuating the front-end control mode switch. In channel mode the first digit instruction is interpreted as tens digit input and indicated on the display. At the units digit the symbol "—" (segment g) lights up, designating a still incomplete input. The input stand-by position available for 8 sec. for the units digit restarts with every instruction; hence the 8 sec. counter only starts after releasing the button. If again the operation is not continued within the 8 sec. time, the device switched back to the standard mode of operation (P-selection, channel indication dependent on the front-end control mode switch). After input of the second digit instruction,an according information is output to the PLL. The changeover P-selection, channel indication is again performed after 8 sec. (henceforth called 8 sec-mode).

With the aid of the store button (remote and front-end control), switching back to P selection is possible. This way, programming via remote control is easily to be done. After switching-on the device is in P-selection mode.

Example

Program setting via remote control

Function	Button
Input program number	1-, 2- 0 9
Changeover to channel mode	"channel selection"
Input tens digit	0 9
Input units digit	0 9
(possibly channel correction)	
(possibly fine tuning)	
Storage	"STORE"
Next program number etc.	1-, 2- 0 9

2.2 Fine tuning

Fine tuning via remote control operates as via front-end control. By means of shortly pressing (τ < appr. 250 msec.) a step is performed into the appropriate direction. In case of continuous actuation, fine-tuning steps are performed in intervals of appr. 250 ms.

Overflow in both directions is signalled in case of on-screened channel indication by blinking. If there was no channel indication prior to the overflow, no blinking takes place during the overflow.

2.3 End-of instruction processing

At every program selection and channel selection instructions, at station search start and fine tuning, the "end instruction" is made up 8 sec. after the last repeat instruction, i.e. the pertinent flag is activated.

All external instructions also activate the end-of-instruction flag.

The end instruction signals unambiguously releasing and repressing of a remote-control button, which has to be reliably recognized for digit instructions, station search, quick tone, etc.

2.4 STORE

By means of the instruction "STORE" (as in case of front-end control), the actual channel number and fine tuning information is filed under the actual program number in the non volatile memory. The program selection initializing goes out, the valid program number is indicated. Channel indication depends on the mode switch of the front-end control; if this one is on program, the previously on-screened channel number is blanked. There is a simultaneous changeover to P-selection mode. During station search, STORE is blocked.

2.5 Program plus/minus

If the device is in P-selection mode, the program number will be incremented or decremented with the aid of the instructions P+/P−.

2.6 Channel tens/units plus

If the device is switched over with the instruction KMODE or if the mode switch of the front-end control is on channel, the instructions P+/P− will act on channel selection. With Z+(P−) the channel number modulo 100 is incremented by 10 (tens digit +1). With E+(P+) the channel number modulo 10 is incremented by 1 (units digit +1) whereby no overflow takes place.

2.7 Station search

Compared to front-end control, station search is also possible if the mode switch of the front-end control is in position "standard". During station search the channel number is indicated (8 sec. mode).

Station search start is edge triggered, i.e. station search stops after a transmitter has been found, even if the station search button is still pressed. Station search can only be restarted when the button was released in the meantime. Station search start by remote control additionally provides a changeover to channel selection mode (8 sec. mode) as well as display of the channel number. Station search can be stopped with all instructions except STORE (and station search). In case of digit instructions, the stop begins with channel selection (8 sec.). External instructions, e.g. volume or ON cause back spacing to P channel mode.

3. **Reduced operation (RESPEC)**

At front-end control, reduced operation provides the same functions as described under SPEC. In case of remote control the possibilities such as STORE, channel selection (CHAN), fine tuning (FT±), and program stepping P+/− are renounced. The hence no longer needed program parts can be made inoperative by external pin programming (RESPEC pin 22 = "H").

Table 1

RESPEC (22)	BOS (36)	Function	Remote control
L	H	Extended spec. operation without program storage	Only channel selection SL, FT+/−, KZ, KE
L	L	Extended spec. operation with program storage	Direct channel selection and program selection KMODE, SL, FT+/−, Store, P+/−
H	H	Reduced spec. operation without program storage	Channel selection (only digits)
H	L	Reduced spec. operation with progr. storage	Only program selection (1-, 2-, digits)

In the case of BOS = H, channel selection is dropped.

4. **Operation without storage** (channel selection, only)

The device is operated without the external non-volatile program memory (BOS, pin 36 = "H"). The selection of the transmitter is done via direct channel input with digit instructions. If it is switched on with the instruction "ON" PLL will be loaded with the previous channel. In the power-on-reset, standby mode is set. If a digit instruction is used for switching-on, the tens digit and a horizontal bar appear (segment "g") on the units digit, whereas the PLL is loaded with the previous word (= channel number at which there was the changeover to stand-by). Further operation is again subject to 8 sec-mode.

If the mains switch is used for switching on, channel 01 is read in.

5. Status-dependent functions

5.1 Applying the supply voltage

The device is brought into the standby state by means of applying the supply voltage.

The input ONOFF is ignored up to the end of this procedure, the status "Standby" is assumed.

5.2. Status Standby

The status Standby is controlled through the remote control receiver IC via the ONOFF input.

Level High = Standby
Level Low = ON

Indication: Retrace blanking is provided for channel indication at the transition into standby mode. Only the right-hand digit of program indication shows a dash (central segment of the 7 segment display). The remote control instructions are only performed if prior to the start the input ONOFF was on low level for at least 30 msec or goes to low within 30 msec after the end of the instruction. The program tens digit instructions 1- or 2- are also accepted during the Standby status. The display then shows 1- or 2-. If an external instruction arrives or if the program selection is not finished within about 8 sec. whereby the ONOFF input changes to low, the display goes back to Standby and program preparation is erased. The front end operating inputs are blocked during the Standby status.

If the device is operated without received transmitter (Stop, pin 35 = "H") and no operate instruction is input, Standby is switched automatically after 5 minutes.

6. Organization of output information

The SDA 2003 IC serially outputs the information to the PLL circuit SDA 2002 and the display decoder SDA 2004 for indication of the program. No. and channel No. The data is shifted via the IFO line which is in common to all external devices. Assignment of the information to the connected circuits is done via 3 clock channels (clock channel: CKA, clock-PLL: CPLL; clock program: CPR). Thus, it is possible to distribute the indications to any location without changing the display device SDA 2004 or the on-screen device SDA 2105; see table 2. The channel No. is on-screened on the screen and the program No. on an LED display, or in a VCR device program No. and channel No. on one LED display.

The order of the IFO blocks is arbitrary. Intervals between any bits are permitted. Data transfer should preferably be done with the HL edge of the clock.

Table 2

Display combinations with the SDA 2004 display decoder driver and the SDA 2105 onscreen device.

SDA 2004		SDA 2105	
CHANNEL	PROGRAM	CHANNEL	PROGRAM
X	–	–	X
–	X	X	–
X	X	–	–
–	–	X	X

7. **Program AV**

Program 0 is indicated as AV (AU) and pin 37 is thereby switched to "H".

Pin designation

Pin No.	Mnemonic	Function
1	NVM [3])	Serial data input for the connection of the nonvolatile memory (NVM)
2	OSC IN	Input for external clock generation (4 MHz)
3	OSC OUT	Oscillator output, if the internal oscillator is used
4	$\overline{\text{RESET}}$	Reset input: active "low"
5	$\overline{\text{SS}}$	Not connected
6	$\overline{\text{DLE}}$ [4])	Clock input for remote control inquiring
7	EA	Connected to ground
8	$\overline{\text{RD}}$	Not connected
9	$\overline{\text{PSEN}}$	Not connected
10	$\overline{\text{WR}}$	Not connected
11	ALE	Not connected
12	IFO [3])	Common serial data output for PLL IC, LED display device, onscreen device, and nonvolatile memory
13	EX/$\overline{\text{REC}}$ [2])	Control output (inverted) for the nonvolatile memory (SDA 2006)
14	$\overline{\text{CNVM}}$ [3])	Clock output (inverted) for the nonvolatile memory
15	ENB	Common enable output for PLL, LED display, and onscreen device
16	CPR [3])	Clock output for program indication (LED display device SDA 2004)
17	CKA [3])	Clock output for channel indication (onscreen device SDA 2105)
18	CPLL [3])	Clock output for PLL IC SDA 2002
19	SL	Active "High" status output being active during station search
20	V_{SS}	Operating ground (OV)
21	$\overline{\text{STBY}}$	Active "Low" pulse output An appr. 4 msec long pulse appears if during the ON state the stop input is non active (high) for about 5 minutes and no operation is performed during this period. The signal is used for initializing the transition from ON to Standby.
22	RESPEC	Wiring according to table 2
23	$\overline{\text{ONOFF}}$ [4])	Active "Low" message input for initializing the transition Standby — ON and ON — Standby
24	$\overline{\text{WC}}$ [2])	Message input from the nonvolatile memory (write complete). As long as $\overline{\text{WC}}$ is on "H", data handling with the memory is blocked.

For notes refer to page 224.

Pin designation (cont'd)

Pin No.	Mnemonic	Function
25	PROG	Not connected
26	V_{DD}	Must be connected to V_{CC}
27	$\overline{\text{SEARCH}}$	A negative pulse at this input starts station search. Every 25 msec (appr.) the channel No. is incremented (ØØ follows after 99) Station search is finished either by a negative pulse at the $\overline{\text{STOP}}$ input, at the $\overline{\text{PROG}+/K_1}$ input, at the $\overline{\text{PROG}-/K_{10}}$ input or by a positive pulse at the $\overline{\text{KMODE}}$ input as well as by a remote control instruction.
28	$\overline{\text{STORE}}$	A negative pulse at this input initializes the storage process. The actual adjustment (channel No. + fine tuning) is filed under the indicated program No. in the nonvolatile memory.
29	$\overline{\text{FT}-}$	Via the active "low" inputs, fine tuning is performed. The tuning process runs automatically with about 4 steps/sec (step 125 kHz) in the selected direction up to the stop, as long as one of the selected signals is active. Starting from the pre-programmed value, the tuning can be adjusted throughout the range between +3.875 and −4 MHz.
30	$\overline{\text{FT}+}$	
31	$\overline{\text{PROG}+/K_1}$ [5]	Setting inputs sensitive to negative pulses.
32	$\overline{\text{PROG}-/K_{10}}$	The function depends on the statuts of the inputs $\overline{\text{KMODE}}$ and $\overline{\text{SET CK}}$

	$\overline{\text{PROG}+/K_1}$	$\overline{\text{PROG}-/K_{10}}$
$\overline{\text{KMODE}}$ "H" $\overline{\text{SET CK}}$ "H" (Program)	Set program No. is incremented by 1 (29+1→Ø!)	Set program No. is decremented by 1 (Ø−1→29!)
$\overline{\text{KMODE}}$ "L" $\overline{\text{SET CK}}$ "H"	Set channel No. is incremented by 1. No carry to the tens digit results. (39+1→30)	Set channel No. is incremented by 10. No influence on the units digit of the channel No. (96+10→06)
	Station search is stopped	
$\overline{\text{SET CK}}$ "L"	no effect	no effect

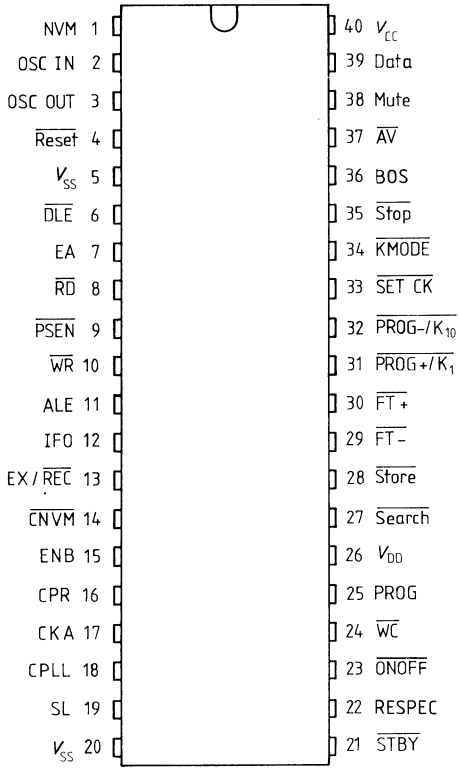
Pin designation (cont'd)

Pin No.	Mnemonic	Function
33	$\overline{\text{SET CK}}$	Input is active "low". The inputs $\overline{\text{PROG}-/\text{K}_{10}}$ and $\overline{\text{PROG}+/\text{K}_1}$ are blocked such that the connected buttons can be used for setting the clock. Channel indication is blanked. Station search is blocked.
34	$\overline{\text{K MODE}}$ [1])	Channel mode input is active "low". The channel indication appears, the function of the inputs $\overline{\text{PROG}-/\text{K}_{10}}$ and $\overline{\text{PROG}+/\text{K}_1}$ is changed and station search enabled.
35	$\overline{\text{STOP}}$	Active "low" message input to stop the station search and to reset the internal 5-min-timer.
36	BOS	Wiring according to table 1
37	$\overline{\text{AV}}$	Active "low" status output, which is active at the set program ØØ. (time constant changeover for VCR)
38	MUTE	Active "high" status output. Appr. 90 msec prior to the output of a tuning information and up to appr. 30 msec thereafter as well as during station search the output is active.
39	DATA [4])[5])	Serial data input for remote control of SDA 2007 IR receiver.
40	V_{CC}	+5 V power supply

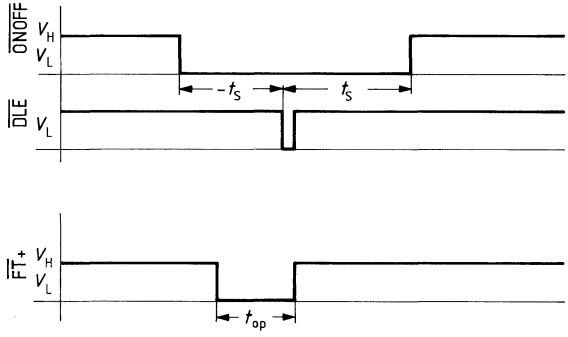
Notes

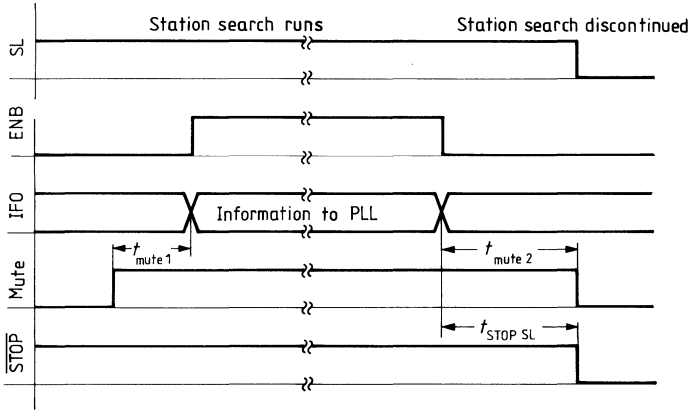
1) 30 msec debouncing
2) For details refer to description of the nonvolatile memory
3) For data format refer to description of the individual peripherals
4) Remote control instructions are only processed if the input ONOFF was on "low" for at least 30 msec prior to the start or goes to "low" within 30 msec after the end of the instruction.
5) Program ØØ is indicated as AU.

Pin configuration, top view



Pulse diagrams





ROM occupation

$f_{video\ carrier}$/MHz		Band selection UHF VHF BD I IFO output	Channel designation	Indicated number
46.25	Australia	H L H	AU_0	01
48.25	BD I	H L H	K_2	02
55.25		H L H	K_3	03
62.25		H L H	K_4	04
175.25	BD III	L L H	K_5	05
182.25		L L H	K_6	06
189.25		L L H	K_7	07
196.25		L L H	K_8	08
203.25		L L H	K_9	09
210.25		L L H	K_{10}	10
217.25		L L H	K_{11}	11
224.25		L L H	K_{12}	12
53.75	Ital. channels	H L H	A	13
62.25		H L H	B	14
82.25		H L H	C	15
175.25		L L H	D	16
183.75		L L H	E	17
192.25		L L H	F	18
201.25		L L H	G	19
210.25		L L H	H	20
471.25	BD IV/V	H H L	K_{21}	21
479.25		H H L	K_{22}	22
487.25		H H L	K_{23}	23
495.25		H H L	K_{24}	24
503.25		H H L	K_{25}	25
511.25		H H L	K_{26}	26
519.25		H H L	K_{27}	27
527.25		H H L	K_{28}	28
535.25		H H L	K_{29}	29
543.25		H H L	K_{30}	30
551.25		H H L	K_{31}	31
559.25		H H L	K_{32}	32
567.25		H H L	K_{33}	33
575.25		H H L	K_{34}	34
583.25		H H L	K_{35}	35
591.25		H H L	K_{36}	36
599.25		H H L	K_{37}	37
607.25		H H L	K_{38}	38
615.25		H H L	K_{39}	39
623.25		H H L	K_{40}	40
631.25		H H L	K_{41}	41
639.25		H H L	K_{42}	42
647.25		H H L	K_{43}	43
655.25		H H L	K_{44}	44
663.25		H H L	K_{45}	45
671.25		H H L	K_{46}	46
679.25		H H L	K_{47}	47
687.25		H H L	K_{48}	48
695.25		H H L	K_{49}	49
703.25		H H L	K_{50}	50

ROM occupation (cont'd)

$f_{video\ carrier}$/MHz	Band selection IFO output	UHF VHF BD I	Channel designation	Indicated number
711.25		H H L	K_{51}	51
719.25		H H L	K_{52}	52
727.25		H H L	K_{53}	53
735.25		H H L	K_{54}	54
743.25		H H L	K_{55}	55
751.25		H H L	K_{56}	56
759.25		H H L	K_{57}	57
767.25		H H L	K_{58}	58
775.25		H H L	K_{59}	59
783.25	BD IV/V	H H L	K_{60}	60
791.25		H H L	K_{61}	61
799.25		H H L	K_{62}	62
807.25		H H L	K_{63}	63
815.25		H H L	K_{64}	64
823.25		H H L	K_{65}	65
831.25		H H L	K_{66}	66
839.25		H H L	K_{67}	67
847.25		H H L	K_{68}	68
855.25		H H L	K_{69}	69
863.25		H H L	ex	70
871.25		H H L	ex	71
879.25		H H L	ex	72
887.25		H H L	ex	73
69.25		H L H	S_{21}	74
76.25		H L H	S_{22}	75
83.25		H L H	S_{23}	76
90.25		H L H	S_{24}	77
97.25		H L H	S_{25}	78
59.25		H L H	OIR channel 2	79
93.25		H L H	OIR channel 5	80
105.25		H L H	S_1	81
112.25		H L H	S_2	82
119.25		L L H	S_3	83
126.25		L L H	S_4	84
133.25	Cable channels	L L H	S_5	85
140.25		L L H	S_6	86
147.25		L L H	S_7	87
154.25		L L H	S_8	88
161.25		L L H	S_9	89
168.25		L L H	S_{10}	90
231.25		L L H	S_{11}	91
238.25		L L H	S_{12}	92
245.25		L L H	S_{13}	93
252.25		L L H	S_{14}	94
259.25		L L H	S_{15}	95
266.25		L L H	S_{16}	96
273.25		L L H	S_{17}	97
280.25		L L H	S_{18}	98
287.25		L L H	S_{19}	99
294.25		L L H	S_{20}	00

Bipolar circuit

In the frequency synthesis system SDA 200, the SDA 2004 provides decoding of the serially offered BCD code and drives in multiplex operation a 4 digit LED 7-segment display for program and channel number indication.

- Serially read-in BCD code
- Enable input
- 2- or 4-digit operation, as required

Type	Ordering code	Package outline
SDA 2004	Q67000-Y501	DIP 18

Maximum ratings

Supply voltage	V_S	8.5	V
Supply current	I_S	400	mA
Input voltage (pins 7, 8, 9, 10)	V_i	5.5	V
H-output current (pins 11, 12, 13, 15, 16, 17, 18)	$I_{q\,H}$	−60	mA
L-output current (pins 2, 3, 4, 5)	$I_{q\,L}$	380	mA
Thermal resistance (system-air)	$R_{th\,SA}$	80	K/W
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C

Range of operation

Supply voltage range	V_S	4.5 to 8.0	V
Ambient temperature range	T_{amb}	0 to 70	°C

Characteristics (V_S = 6.8 V, T_{amb} = 25 °C, unless otherwise specified)

		min	typ	max	
Internal current consumption (without load) (V_S = 7.15 V)	I_S		20	31	mA
Load resistance (LED: V_F = 1.6 V)	R	95			Ω
Current consumption (V_S = 7.15 V)	I_S			380	mA
Upper threshold voltage (pins 7, 8, 9, 10)	$V_{S\,u}$	1	1.3	1.6	V
Lower threshold voltage (pins 7, 8, 9, 10)	$V_{S\,l}$	0.5	0.7	1	V
Hysteresis (pins 7, 8, 9, 10)	V_H		0.6		V
H-output voltage (pins 11, 12, 13, 15, 16, 17, 18) (V_S = 7.15 V, $I_{q\,H}$ = −40 mA)	$V_{q\,H}$			6.5	V
H-output voltage (pins 11, 12, 13, 15, 16, 17, 18) (V_S = 6.45 V, $I_{q\,H}$ = −40 mA)	$V_{q\,H}$	5.1			V
L-output voltage (pins 2, 3, 4, 5) (V_S = 6.45 V, $I_{q\,L}$ = 280 mA)	$V_{q\,L}$		0.6	0.8	V
H-input current (pins 7, 8, 9, 10) (V_{iH} = 5.0 V)	$I_{i\,H}$			8	µA
L-input current (pins 6, 7, 8, 9, 10) (V_S = 7.15 V, $V_{i\,L}$ = 0.4 V)	$I_{i\,L}$			−40	µA
H-output current (pins 11, 12, 13, 15, 16, 17, 18) (V_S = 7.15 V)	$I_{q\,H}$			−48 *	mA
H-output current (pins 2, 3, 4, 5) (V_S = 7.15 V)	$I_{q\,H}$			50	µA
L-output current (pins 2, 3, 4, 5) (V_S = 7.15 V)	$I_{q\,L}$			336	mA

Switching times

H-pulse width (level = 2 V)	$t_{WH\,8,\,10}$	0.5	0.1		µs
L-pulse width (level = 0.6 V)	$t_{WL\,8,\,10}$	3	1.5		µs
Set-up time	$t_{S\,9}$	0	−0.4		µs
Hold time	$t_{H\,9}$	3	1.5		µs
Set-up time	$t_{S\,7}$	0	−0.3		µs
Hold time	$t_{H\,7}$	3			µs
H-pulse width (level = 2 V)	$t_{WH\,7}$	70	50		µs
L-pulse width (level = 0.6 V)	$t_{WL\,7}$	3	1.6		µs
H-pulse width (pins 2, 3, 4, 5) **4-digit operation**	t_{WH}		4.5		ms
L-pulse width (pins 2, 3, 4, 5) **4-digit operation**	t_{WL}		1.5		ms
Set-up time (pins 2, 3, 4, 5)	t_S	0		2	µs
H-pulse width **2-digit operation**	$t_{WH\,2,\,3}$		3		ms
L-pulse width **2-digit operation**	$t_{WL\,2,\,3}$		3		ms
Set-up time	$t_{S\,2,\,3}$	0		2	µs

*) 48 mA ≙ 12 mA integral value at 4 digit operation or 24 mA at 2 digit operation, respectively

Truth table

Data D LSB . . . MSB*				Display	Segment driver (active H) a	b	c	d	e	f	g
L	L	L	L	0	H	H	H	H	H	H	L
H	L	L	L	1	L	H	H	L	L	L	L
L	H	L	L	2	H	H	L	H	H	L	H
H	H	L	L	3	H	H	H	H	L	L	H
L	L	H	L	4	L	H	H	L	L	H	H
H	L	H	L	5	H	L	H	H	L	H	H
L	H	H	L	6	H	L	H	H	H	H	H
H	H	H	L	7	H	H	H	L	L	L	L
L	L	L	H	8	H	H	H	H	H	H	H
H	L	L	H	9	H	H	H	H	L	H	H
L	H	L	H	dark	L	L	L	L	L	L	L
H	H	L	H	dark	L	L	L	L	L	L	L
L	L	H	H	U	L	H	H	H	H	H	L
H	L	H	H	A	H	H	H	L	H	H	H
L	H	H	H	—	L	L	L	L	L	L	H
H	H	H	H	dark —	L	L	L	L	L	L	L

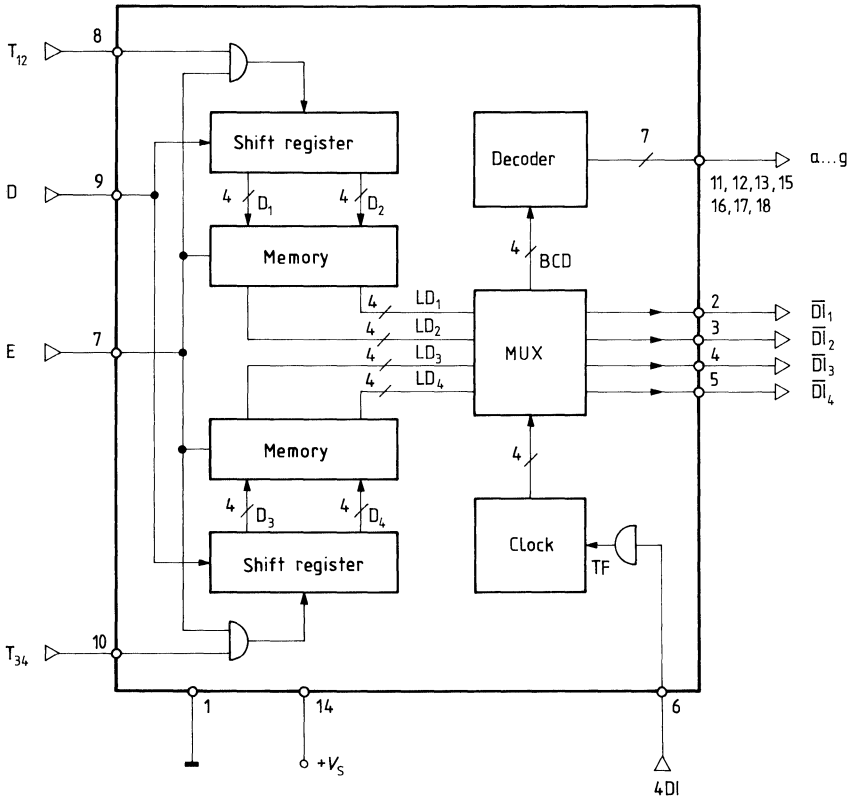
* LSB = least significant bit
MSB = most significant bit

Segment designation

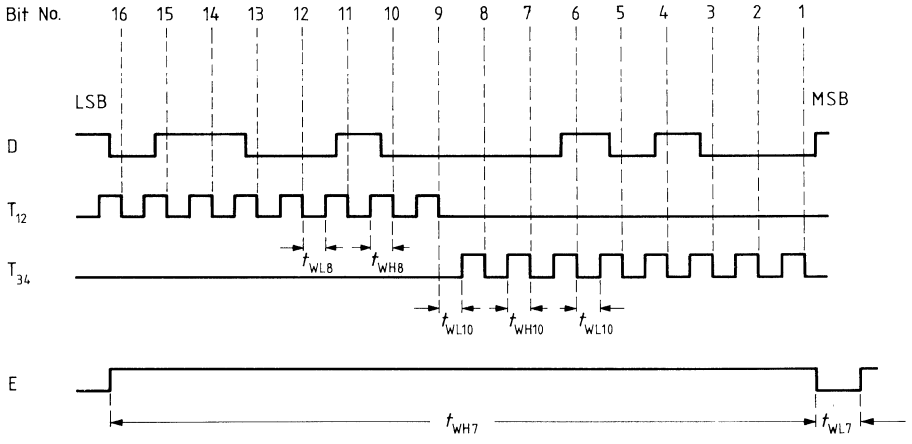
Pin designation

Pin No.	Symbol	Description
1	$\perp$	Ground
2	$\overline{DI_1}$	Output for digit 1
3	$\overline{DI_2}$	Output for digit 2
4	$\overline{DI_3}$	Output for digit 3
5	$\overline{DI_4}$	Output for digit 4
6	4DI	Input for digit switching operation (4- or 2-digit operation, respectively)
7	E	Input for enable
8	T_{12}	Input for clock (digit 1 and 2)
9	D	Input for data
10	T_{34}	Input for clock (digit 3 and 4)
11	g	Output for segment g
12	f	Output for segment f
13	e	Output for segment e
14	V_S	Supply voltage
15	d	Output for segment d
16	c	Output for segment c
17	b	Output for segment b
18	a	Output for segment a

Block diagram



Pulse diagram

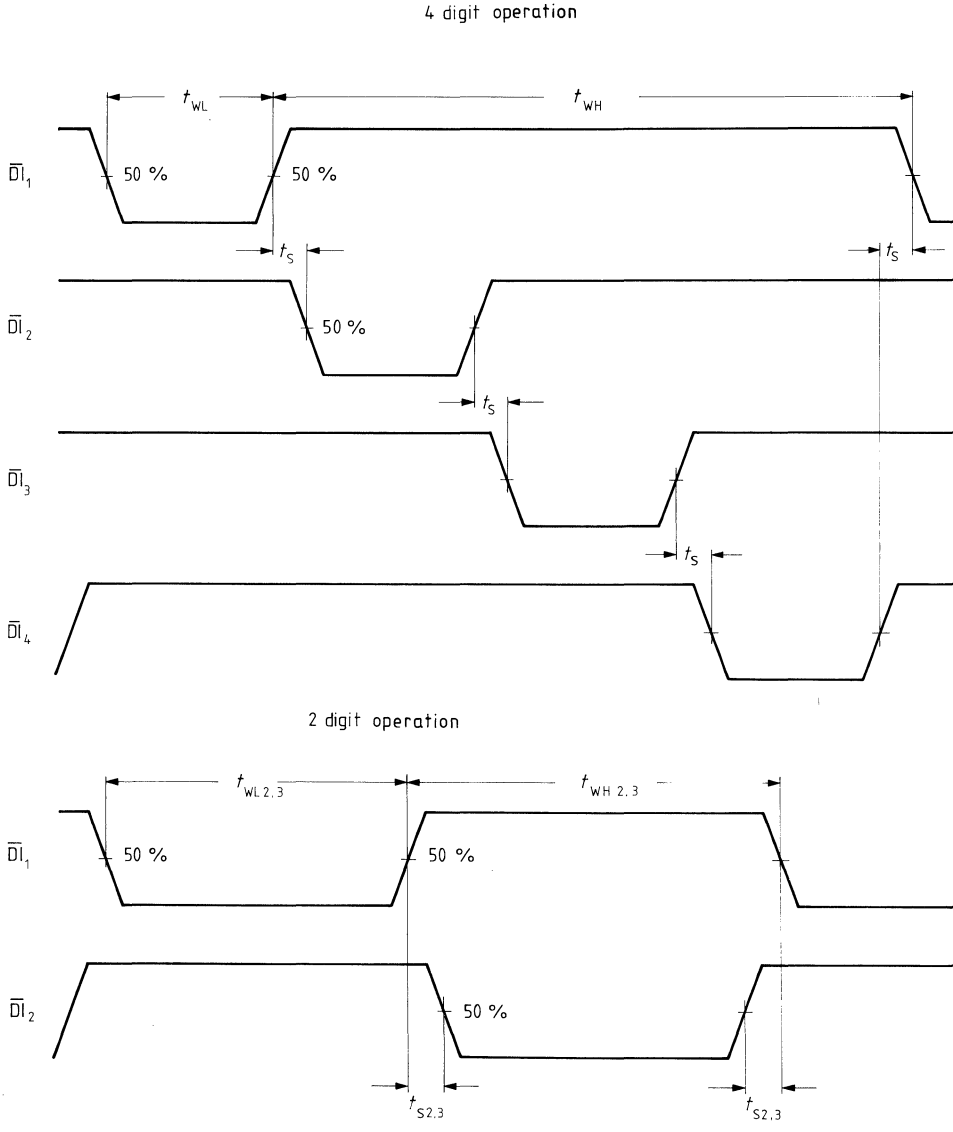


Memory contents after the trailing edge of E

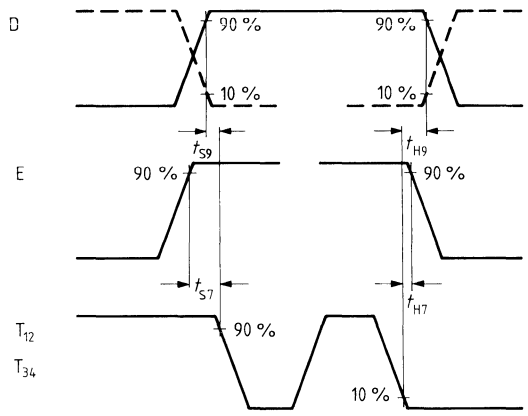
	L	H	H	L	L	H	L	L	L	L	H	L	H	L	L	L
Display		6				2				4				1		
		Digit 2				Digit 1				Digit 4				Digit 3		

Remark: The information at first shifted to D is displayed at digit 2; digit 1, digit 4, and digit 3 follow. At every digit, LSB has to be shifted first.

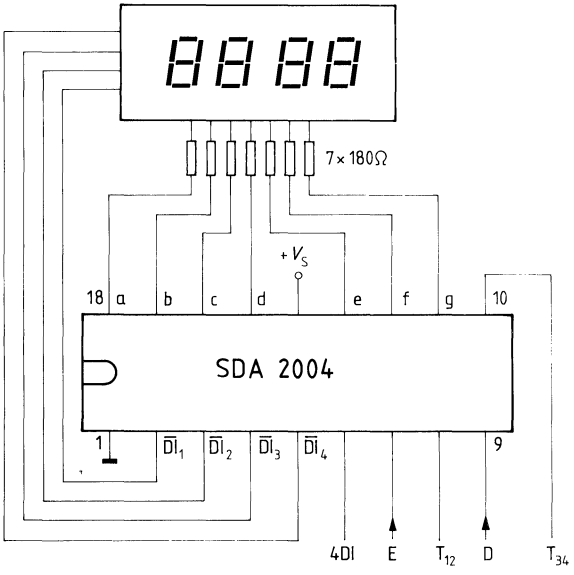
Timing diagram



Timing diagram: Set-up and hold times



Application circuit 4-digit operation



At 2-digit operation ($\overline{DI}_1$ and $\overline{DI}_2$), 4 DI is grounded

Bipolar circuit

The SDA 2014 LED display driver that permits cascade connection decodes a serially offered BCD code and drives in multiplex operation 2 or 4 digits, as required. An output with serial data output permits cascade connection of the display drivers for more than 4 digits (6, 8, 10, etc.).

- Serially read-in BCD code
- Enable input
- Any number of ICs permitted for cascade connection
- 2- or 4-digit operation, as required

Type	Ordering code	Package outline
SDA 2014	Q67000-Y538	DIP 18

Maximum ratings

Supply voltage	V_S	8.5	V
Supply current	I_S	400	mA
Input voltage (pins 7, 8, 9)	V_i	5.5	V
Output voltage (pin 10)	$V_{q\,H}$	8.5	V
H-output current (pins 11, 12, 13, 15, 16, 17, 18)	$I_{q\,H}$	−60	mA
L-output current (pins 2, 3, 4, 5)	$I_{q\,L}$	380	mA
Thermal resistance (system-air)	$R_{th\,SA}$	80	K/W
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−65 to 150	°C

Range of operation

Supply voltage range	V_S	4.5 to 8	V
Ambient temperature range	T_{amb}	0 to 70	°C

Characteristics (V_S = 5.0 V, T_{amb} = 25 °C, unless otherwise specified)

		min	typ	max	
Internal current consumption (without load) (V_S = 8 V)	I_S		20	31	mA
Current consumption (V_S = 8 V)	I_S			380	mA
Upper threshold voltage (pins 7, 8, 9)	$V_{S\,u}$		1.3		V
Lower threshold voltage (pins 7, 8, 9)	$V_{S\,l}$		0.7		V
Hysteresis (pins 7, 8, 9)			0.6		V
H-output voltage (pins 11, 12, 13, 15, 16, 17, 18) (V_S = 8 V, $I_{q\,H}$ = −40 mA)	$V_{q\,H}$			7.35	V
H-output voltage (pins 11, 12, 13, 15, 16, 17, 18) (V_S = 4.5 V, $I_{q\,H}$ = −40 mA)	$V_{q\,H}$	3.2			V
L-output voltage (pins 2, 3, 4, 5) (V_S = 4.5 V, $I_{q\,L}$ = 280 mA)	$V_{q\,L}$		0.6	0.8	V
H-input current (pins 7, 8, 9) (V_i = 5 V)	$I_{i\,H}$			8	µA
L-input current (pins 6, 7, 8, 9) (V_S = 8 V, $V_{i\,L}$ = 0.4 V)	$I_{i\,L}$			−50	µA
H-output current (pins 11, 12, 13, 15, 16, 17, 18) (V_S = 8 V)	$I_{q\,H}$			−48*	mA
H-output current (pins 2, 3, 4, 5) (V_S = 8 V)	$I_{q\,H}$			50	µA
L-output current (pins 2, 3, 4, 5) (V_S = 8 V)	$I_{q\,L}$			336	mA
H-output voltage (pin 10) (−$I_{q\,H}$ = 200 µA)	$V_{q\,H}$	V_S−2	V_S−1.5	V_S−1	V
L-output voltage (pin 10) ($I_{q\,L}$ = 3 mA, V_S = 4.5 V)	$V_{q\,L}$			0.4	V
Short-circuit output current (pin 10) (V_S = 8 V, max. duration: 1 sec)	I_q	−20		−50	mA

* 48 mA ≙ 12 mA integral value at 4 digit operation or 24 mA at 2 digit operation, respectively

Switching times

		min	typ	max	
H-pulse width (level = 2 V)	$t_{WH\,8}$	0.5	0.1		µs
L-pulse width (level = 0.6 V)	$t_{WL\,8}$	3	1.5		µs
Hold time	$t_{H\,8}$	0.3	0		µs
Set-up time	$t_{S\,9}$	0	−0.4		µs
Hold time	$t_{H\,9}$	3	1.5		µs
Set-up time	$t_{S\,7}$	0	−0.3		µs
Hold time	$t_{H\,7}$	3			µs
H-pulse width (level = 2 V)	$t_{WH\,7}$	70	50		µs
L-pulse width (level = 0.6 V)	$t_{WL\,7}$	3	1.6		µs
H-pulse width (pins 2, 3, 4, 5)	t_{WH}		4.5		ms
4-digit operation					
L-pulse width (pins 2, 3, 4, 5)	t_{WL}		1. 5		ms
4-digit operation					
Set-up time (pins 2, 3, 4, 5)	t_S	0		2	µs
H-pulse width	$t_{WH\,2.3}$		3		ms
2 digit operation					
L-pulse width	$t_{WL\,2.3}$		3		ms
2 digit operation					
Set-up time	$t_{S\,2.3}$	0		2	µs

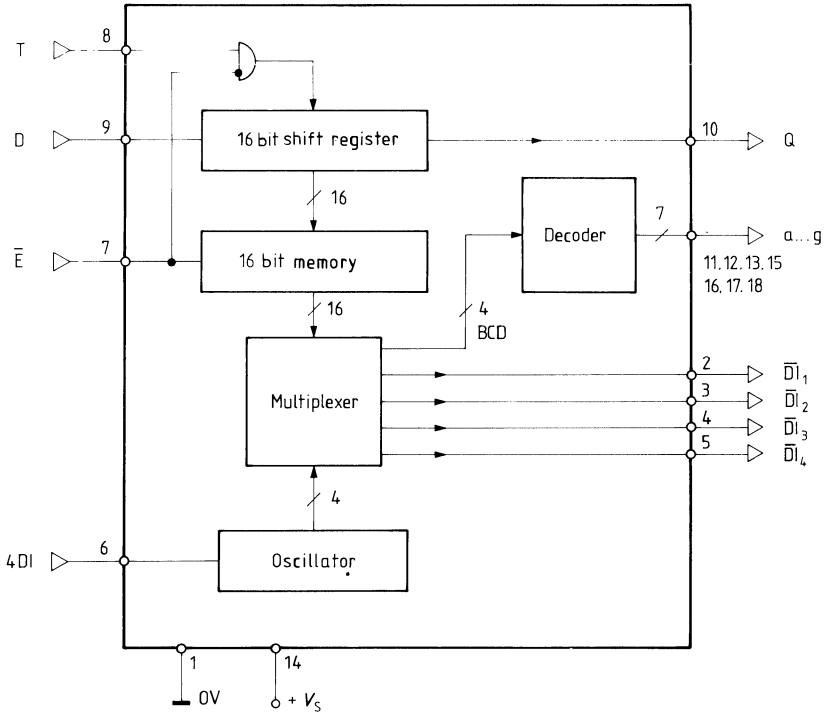
Truth table

Data D LSB . . . MSB*	Display	Segment driver (active H) a	b	c	d	e	f	g
L L L L	0	H	H	H	H	H	H	L
H L L L	1	L	H	H	L	L	L	L
L H L L	2	H	H	L	H	H	L	H
H H L L	3	H	H	H	H	L	L	H
L L H L	4	L	H	H	L	L	H	H
H L H L	5	H	L	H	H	L	H	H
L H H L	6	H	L	H	H	H	H	H
H H H L	7	H	H	H	L	L	L	L
L L L H	8	H	H	H	H	H	H	H
H L L H	9	H	H	H	H	L	H	H
L H L H	dark	L	L	L	L	L	L	L
H H L H	dark	L	L	L	L	L	L	L
L L H H	dark	L	L	L	L	L	L	L
H L H H	dark	L	L	L	L	L	L	L
L H H H	dark	L	L	L	L	L	L	L
H H H H	dark	L	L	L	L	L	L	L

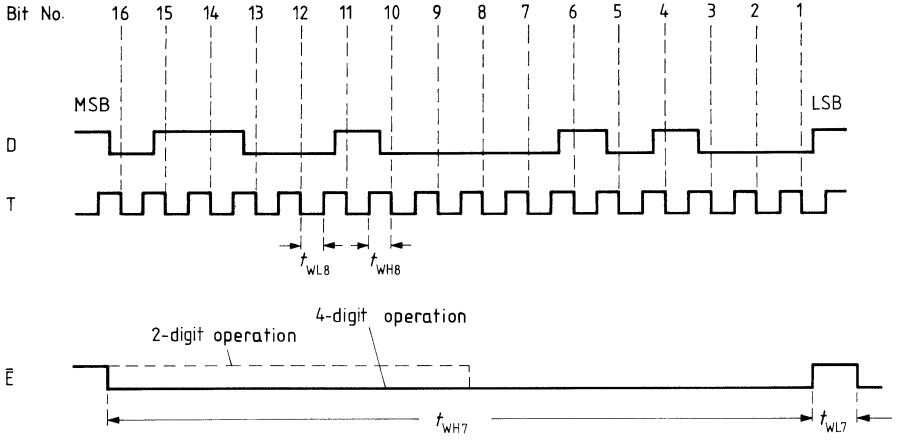
Segment designation

* LSB = least significant bit
MSB = most significant bit

Block diagram



Pulse diagram



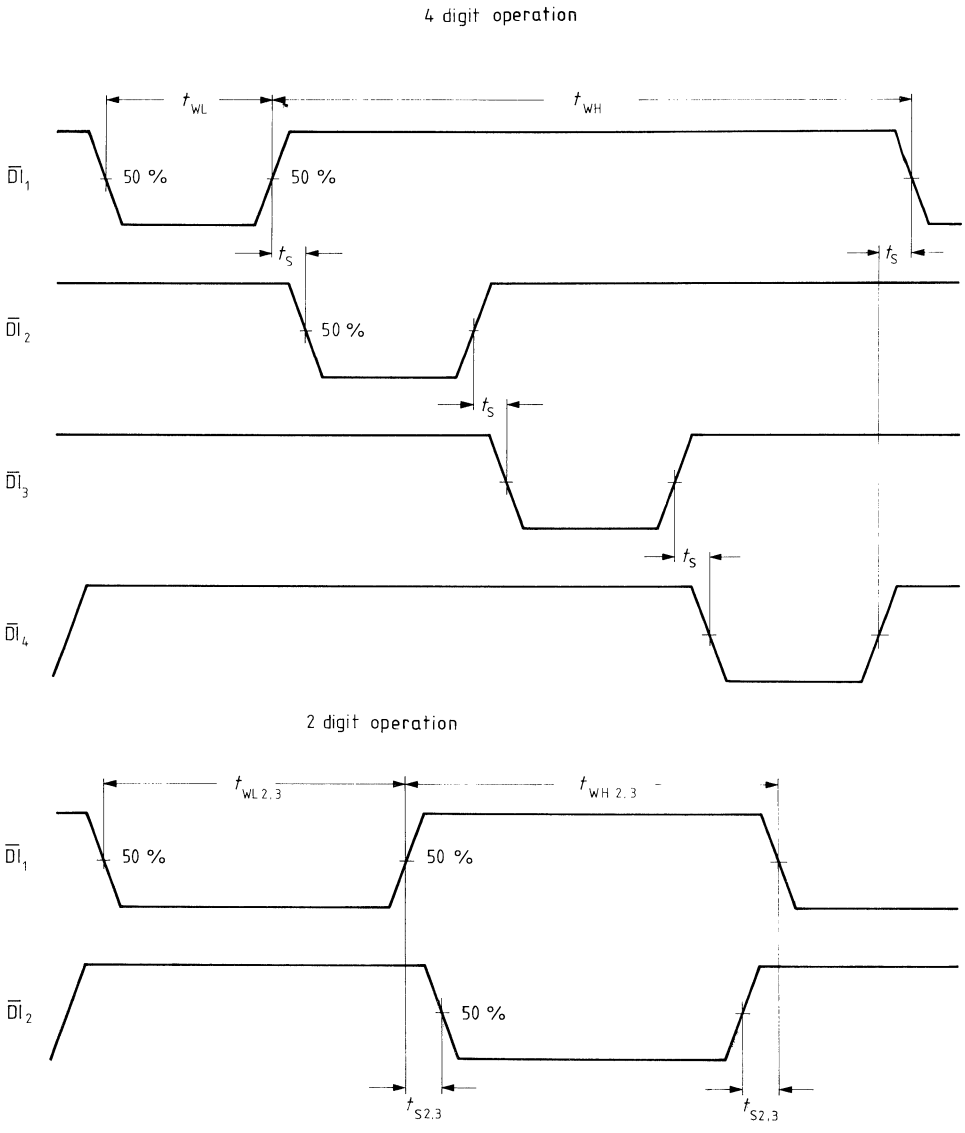
Memory contents after the rising edge of E: (4-digit operation)

	L	H	H	L	L	H	L	L	L	L	H	L	H	L	L	L
Display		6				4				2				8		
		Digit 4				Digit 3				Digit 2				Digit 1		

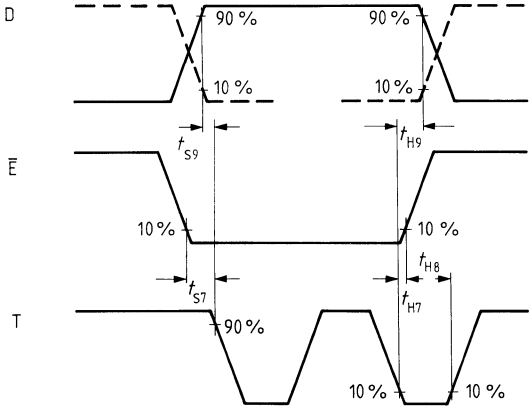
Memory contents and display at 2-digit operation

Remark: The information at first shifted to D is displayed at digit 4; digit 3, digit 2, and digit 1 follow. At every digit, MSB has to be shifted first.

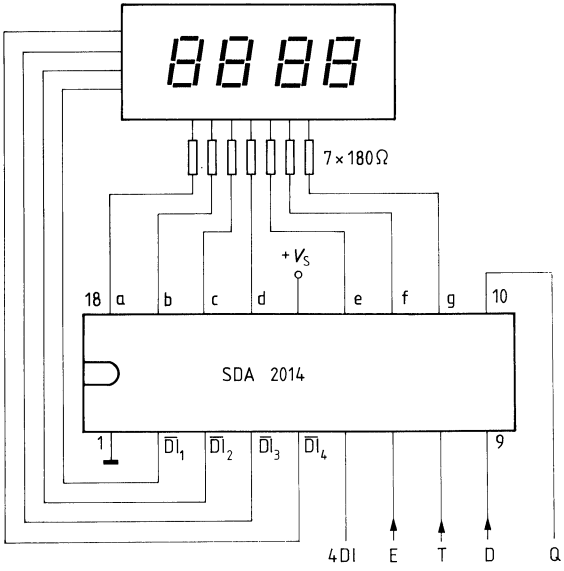
Timing diagram



Timing diagram: Set-up and hold times



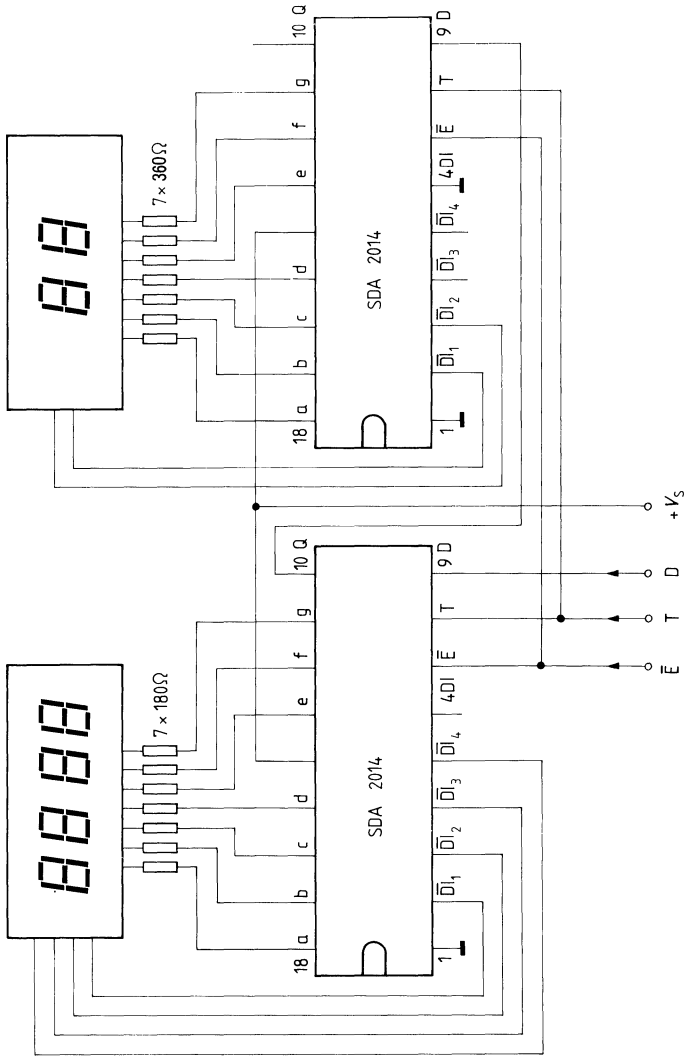
Application circuit: 4-digit operation



At 2-digit operation ($\overline{DI}_1$ and $\overline{DI}_2$), 4 DI is grounded

Application circuit

Example: Cascade connection to 6 digits



MOS circuit

The SDA 2105 IC is intended to display the channel number and the program number on the screen of TV receivers. The digits can be displayed at the top right, at the bottom right, and at the bottom left; the digits are 21 frame lines in height.

- 4-bit character set
- 3 fixed onscreen locations
- Onscreen locations can be driven and selected separately
- 5-digit onscreen location permits display of time or frequency

Type	Ordering code	Package outline
SDA 2105	Q 67000-Y 645	DIP 18

Maximum ratings (all voltages referred to V_{SS} = 0 V)

Supply voltage	V_{DD}	−0.3 to 12	V
Input voltages	V_i	−0.3 to 12	V
Total power dissipation	P_{tot}	850	mW
Thermal resistance (sytem — air)	$R_{th\ SA}$	70	K/W
Storage temperature range	T_{stg}	−25 to 125	°C

Range of operation (referred to V_{SS} = 0 V)

Supply voltage range	V_{DD}	9 to 11	V
Ambient temperature range	T_{amb}	0 to 70	°C

Characteristics (all voltages referred to V_{SS} = 0 V)

		min	typ	max	
Supply current at V_{DD} = 11 V	I_{18}			70	mA
Schmitt Trigger inputs LIM, FIM					
H-input voltage	$V_{i\,H\,14,\,17}$	5		11	V
L-input voltage	$V_{i\,L\,14,\,17}$	0		0.8	V
Input capacitance	$C_{i\,14,\,17}$			10	pF
Input resistance	$R_{i\,14,\,17}$	1			MΩ
Line frequency	$f_{LIM\,17}$	15.5	15.625	15.7	kHz
Field frequency	$f_{FIM\,14}$	45	50	52	Hz
LH/HL transition time	t_T			5	µs
Inputs DATA, CL_1, ENA_1, CL_2, ENA_2, CL_3, ENA_3					
H-input voltage	$V_{i\,H\,4\ldots10}$	2.4		11	V
L-input voltage	$V_{i\,L\,4\ldots10}$	0		0.8	V
Input capacitance	$C_{i\,4\ldots10}$			10	pF
Input resistance	$R_{i\,4\ldots10}$	1			MΩ
Overlap time	$t_{D\,1}$	2			µs
Follow-up time	$t_{D\,2}$	2			µs
LH/HL transition time	t_T	0		5	µs
H pulse width	t_{WH}	5			µs
L pulse width	t_{WL}	5			µs
Onscreen output EB_1 (open drain output)					
L-output voltage at $I_{L\,13}$ = 3 mA	$V_{q\,L\,13}$	0		3	V
H-leakage current at $V_{q\,H}$ = 11 V	$I_{H\,13}$			10	µA

Circuit description

The IC is used to display the channel number, the program number, and the reception frequency on the screen of a TV set. Two display locations of two digits each and one display location of five digits are available (refer to figure "Allocation").

The character set (4 bits/character) comprises the digits 0 to 9, A, V, —, :,. (refer to figure "Outline of the signs").

The information for a display location is transferred via three lines:

DATA (common to all three display locations)
ENA (Enable, a special line for every display location)
CL (Clock = read-in clock, a special line for every display location)

During switching of the supply voltage, the ENA line must be on low lewel in order to ensure a correct reset of the input registers. As long as a display location is not used, the pertinent ENA terminal must directly be connected to the pin V_{SS}.

The sequence of the information input is from LSB of the right sign to MSB of the left sign (refer to figure "Data input"). The information in the read-in register does not alter provided that either the ENA line or the CL line remains on low level.

During the read-in of new data (ENA = high) the previous data is displayed and as soon as ENA moves to low again, the new data is displayed.

The IC includes an internal oscillator for the dot frequency. The oscillator frequency is automatically regulated according to the line frequency conditions such that independent of production deviations a fixed display raster is obtained. A capacitor should be connected to the terminals I_{OUT} (pin 16) and I_{IN} (pin 15) in order to provide functioning of the regulation.

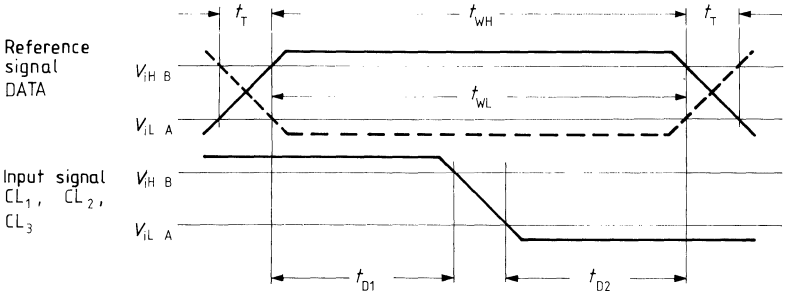
An N channel open-drain transistor is used as onscreen output EBA. In the case of onscreening, the transistor is switched on and moves the level towards low.

Pin designation

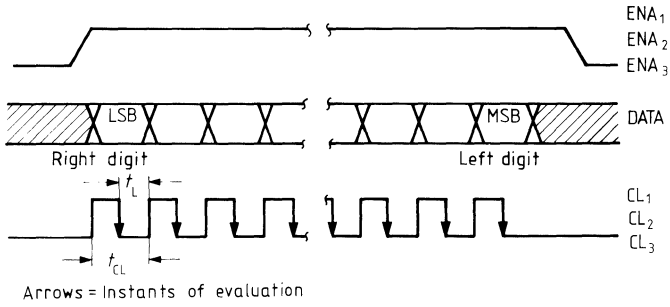
Pin No.	Symbol	Function	Pin No.	Symbol	Function
1	V_{SS}		18	V_{DD}	
2	PRIO	(f. test, not connected)	17	LIM	Line synch. pulse
3	PRS	(f. test, apply to V_{SS})	16	I_{OUT}	Integrator
4	ENA_3	Enable bottom left	15	I_{IN}	Integrator
5	CL_3	Clock bottom left	14	FIM	Field synch pulse
6	DATA	Data	13	EBA	Onscreen output
7	CL_1	Clock bottom right	12	n.c.	
8	ENA_1	Enable bottom right	11	n.c.	
9	ENA_2	Enable top right	10	CL_2	Clock top right

Input signals ENA_1, ENA_2, ENA_3, CL_1, CL_2, CL_3, DATA

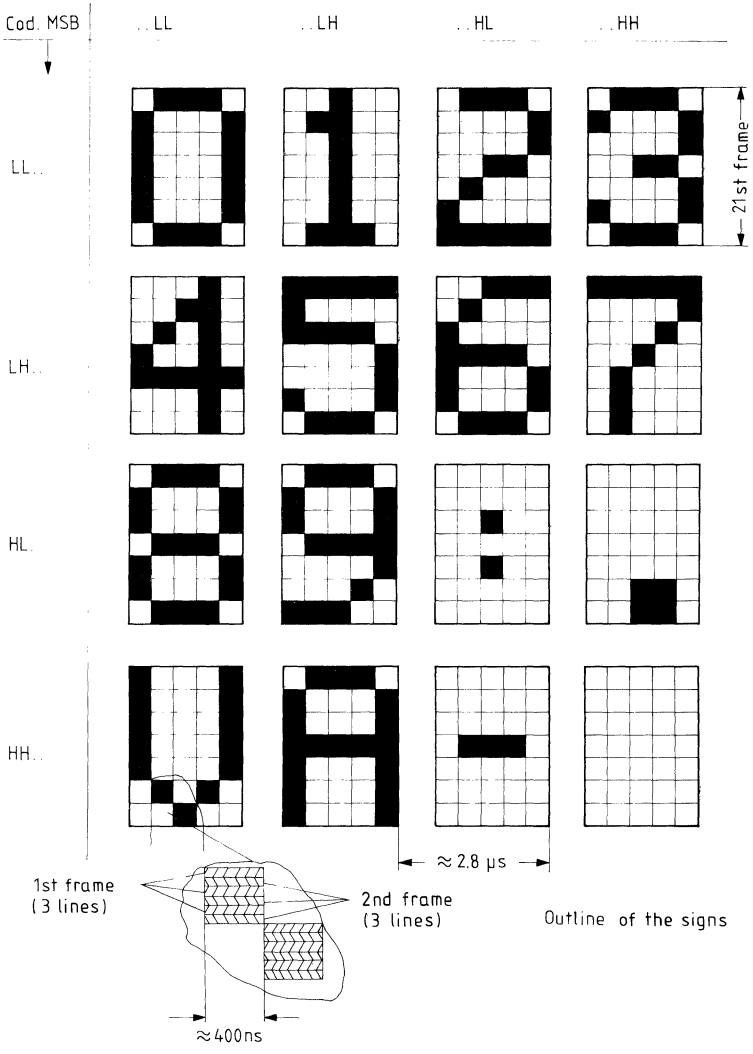
Timing diagram

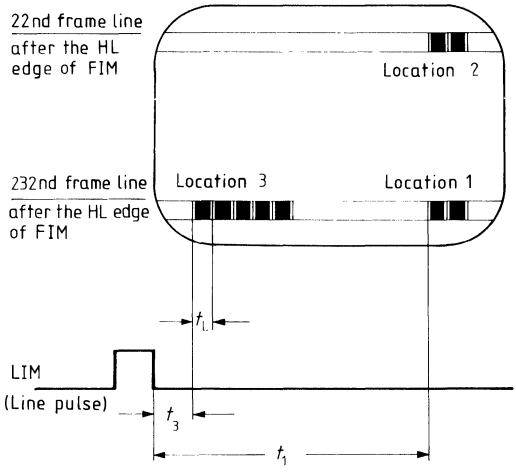


Data transfer with DATA



Data channel proc.				Display
MSB			LSB	
L	L	L	L	0
L	L	L	H	1
L	L	H	L	2
L	L	H	H	3
L	H	L	L	4
L	H	L	H	5
L	H	H	L	6
L	H	H	H	7
H	L	L	L	8
H	L	L	H	9
H	L	H	L	:
H	L	H	H	.
H	H	L	L	V
H	H	L	H	A
H	H	H	L	—
H	H	H	H	blank


Cod. MSB
..LL
..LH
..HL
..HH
LL..
LH..
HL..
HH..
21st frame
≈2.8 µs
1st frame
(3 lines)
2nd frame
(3 lines)
Outline of the signs
≈400ns

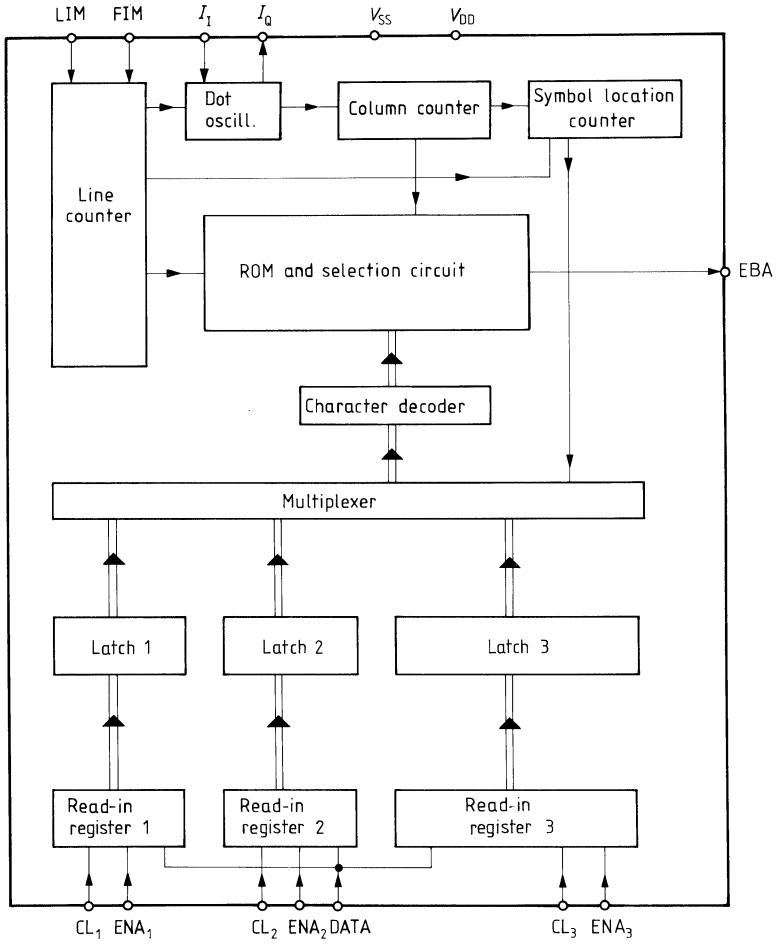


t_3 = approx. 5.7 µs

t_1 = approx. 40 µs

t_L = approx. 2.8 µs

Block diagram



MOS circuit

General features

- Nonvolatile memory of electrical, word-organized reprogrammability, in n channel floating gate technology
- 512-bit storage capacity (32 words of 16 bits, each)
- Serial word address, chip select, and instruction input via an 8-bit or 12-bit control word (switchable by means of external components)
- Erase and write duration determined with the aid of chip-internal control
- Signal outputs with open-drain stages
  active signal inputs and outputs can be inverted by terminal wiring
- Number of reprogrammings $> 10^4$
- Unlimited number of read-out procedures without refresh
- Min. 10 years storage time

Type	Ordering code	Package outline
SDA 2006	Q67100-Q264	DIP 18

Maximum ratings

Supply voltage	$V_{DD\ 2\text{-}1}$	22	V
Supply voltage	$V_{PI\ 18\text{-}1}$	22	V
Supply voltage	$V_{PP\ 3\text{-}1}$	41	V
Input voltage	$V_{i\text{-}17}$	16	V
Total power dissipation	P_{tot}	400	mW
Thermal resistance (system — air)	$R_{th\ SA}$	90	K/W
Storage temperatur range	T_{stg}	−40 to 125	°C

Range of operation (referred to $V_{SS} = 0$ V)

Supply voltage range	$V_{DD\ 2}$	11 to 16	V
Ambient temperature range	T_{amb}	0 to 70	°C

Static characteristics (all voltages referred to V_{SS} = 0 V)

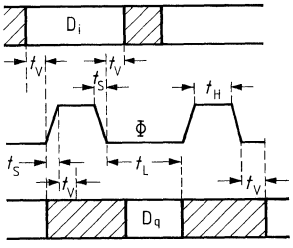
		min	typ	max	
Supply current	$I_{DD\,2}$		10	20	mA
Substrate bias	$-V_{BB\,1}$	4		6	V
Substrate current					
Substrate current, average current	$-I_{BB\,1\,a}$*		0.5	2	mA
Substrate current, peak pulse current	$-I_{BB\,1\,p}$*			10	mA
Programming voltage	$V_{PP\,3}$*		33	35	V
Programming current, quiescent current	$I_{PP\,3}$		0.1		mA
Programming current, average current	$I_{PP\,3a}$		2	5	mA
Programming current, peak pulse current	$I_{PP\,3p}$		5	10	mA
Write voltage	$V_{PI\,18}$*		15	16	V
Write current, quiescent current	$I_{PI\,18}$		0.1		mA
Write current, average current	$I_{PI\,18a}$		5	20	mA
Write current, peak pulse current	$I_{PI\,18p}$		15	50	mA
Inputs					
D_i	$V_{L\,8,12,16}$	0		0.5	V
$\Phi/\overline{\Phi}$	$V_{H\,8,12,16}$	4		V_{DD}	V
REC/$\overline{\text{REC}}$	$I_{H\,8,12,16}$			10	µA
($V_H = V_{DD}$)					
STWL					
($-I_L$ = 100 µA, pull-up resistors)	$V_{L\,4,15,9,11,10}$	0		0.5	V
INV	$V_{H\,4,15,9,11,10}$	4		V_{DD}	V
CS_3	$I_{H\,4,15,9,11,10}$			10	µA
CS_1, CS_2					
(with a control word of 12 bits only; $V_H = V_{DD}$)	$I_{H\,4,15,9,11,10}$			10	µA
(V_L = 0 V; $V_H = V_{DD}$)	$I_{L\,4,15,9,11,10}$			300	µA
$\overline{\text{RES}}$	$V_{L\,6}$	0		0.5	V
	$V_{H\,6}$	4		V_{DD}	V
(V_L = 0 V)	$-I_L$			200	µA
($V_H = V_{DD}$)	I_H			200	µA
Outputs					
$D_q/\overline{D_A}$, $\overline{L}/L$	$V_{L\,14,13}$			0.5	V
(I_L = 1 mA; open-drain stages)					
($V_H = V_{DD}$)	$I_{H\,14,13}$			10	µA

* only necessary during programming

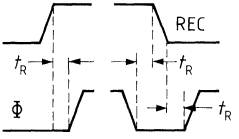
Dynamic characteristics

		min	typ	max	
Data bus					
Φ—Clock	t_H	5			µs
INV on low	t_L	10			µs
Φ—Clock	t_H	10			µs
INV on high	t_L	5			µs
	t_V	5			µs
	t_S			2	µs
Signal edge distance INV on low or high	t_R	5			µs
Programming duration (V_{PH} = 33 V, V_{PI} = 15 V)	t_{prog}		0.1	1	s
Programming frequency	f_{prog}			1	Hz

INV on low



Signal edge distance



Circuit description

Data transfer

Data transfer with the SDA 2006 is performed serially via a 5-line bus, consisting of:

Data input D_i
Data output $D_q/\overline{D_q}$
Data input signal REC/$\overline{\text{REC}}$ (receive data)
Clock input $\Phi/\overline{\Phi}$
Programming output signal $\overline{L}$/L (load)

The active input or output levels, respectively, may be inverted via the input INV. They are switchable, as a group, in order to facilitate adaptation to different external circuits.

Terminal	Potential		Remark
INV	low (V_{SS})	high (V_{DD})	
$D_i/\overline{D_q}$	$D_i = D_q$	$D_i = \overline{D_q}$	
REC/$\overline{\text{REC}}$	high	low	During data input
$\Phi/\overline{\Phi}$	high	low	Active shift pulse
$\overline{L}$/L	low	high	In the case of reprogramming

Chip control

The control information is input via data input D_i in the form of a control word, the length of which may be set via input STWL:

Terminal STWL	low	high (open or V_{DD})
Control word length	8 bits	12 bits

The control words contain information on word address, chip address, and instruction, and have the following formats (A_0 as LSB at first):

8-bit control word	$A_0\ A_1\ A_2\ A_3\ A_4\ B_1\ B_2\ C_3$
12-bit control word	$A_0\ A_1\ A_2\ A_3\ B_0\ B_1\ B_2\ B_3\ A_4\ C_1\ C_2\ C_3$

with $A_0 \ldots\ldots A_4$ Word address bits
$B_0 \ldots\ldots B_3$ Instruction bits
$C_1 \ldots\ldots C_3$ Chip select bits

Instruction coding

12-bit control word				
B_0	B_1	B_2	B_3	Instruction
low	high	high	high	Read out, D_9 as LSB
low	low	high	high	Read out, D_1 as LSB
low	low	low	high	Programming
	8-bit control word			

Chip select

An instruction is only decoded in a memory, if the information of the chip select bits matches that of the chip select inputs.

Chip select — Terminal		Chip select — Bit
	$CS_1 \leftrightarrow C_1$ $CS_2 \leftrightarrow C_2$	12-bit control word
8-bit control word	$CS_3 \leftrightarrow C_3$	

CS_1 and CS_2 remain unconnected in the case of the 8-bit control word.

Read-out (figure 1a and 1b)

Prior to the read operation of the memory the 8-bit or 12-bit control word must be serially clocked into the data input D. 8 or 12 clock pulses, respectively, at the input $\Phi/\overline{\Phi}$ are necessary for the input of the control word. During the input, the REC/$\overline{\text{REC}}$ input is active (active high for low at INV, active low for high at INV).

The information input is closed by means of the trailing edge of the REC/$\overline{\text{REC}}$ signal and at chip select the read-out instruction is decoded. In this way, also the data output $D_i/\overline{D}_9$ becomes low-ohmic.
With the aid of a further clock pulse S, the read-out operation is initialized. The data is shifted with the trailing edge of further clock pulses. The LSB arrives at the data output with the first of these pulses. During the read-out operation via the control word either the first data bit D_1 or the ninth data bit D_9 can be chosen as LSB. The read-out operation can be discontinued after any number of shift pulses. Thus,every stored 16-bit data word can also be read split into two 8-bit data words.

Reprogramming (figure 2a and 2b)

Prior to programming, the 16-bit data word (D_1 as LSB, first), then the 8-bit or 12-bit control word at the data input D_i must be clocked in by means of the active REC/$\overline{\text{REC}}$ signal. It is the trailing edge of the REC/$\overline{\text{REC}}$ signal which decodes the programming instruction at chip select. The reprogramming operation, however, only starts with the trailing edge of a further clock pulse and is recorded to the memory controller via the $\overline{\text{L}}$/L signal.

The duration t_{prog} of reprogramming is determined by chip-internal control. Independent of the external operating voltages V_{PH} and V_{PI} the erase and the write operation are only finished after every memory has reached the desired state. During rewriting, the memory cannot be influenced externally, because the input REC/$\overline{\text{REC}}$, $\Phi/\overline{\Phi}$ and D_i remain blocked. Premature termination of the operation can only be caused by zero level at the input $\overline{\text{RES}}$.

Reset function

A low level voltage at the input $\overline{\text{RES}}$ moves the memory into the reset status. A voltage divider is internally connected to the input. It reliably finishes the reset status for $V_{DD} > 11$ V.

Voltage supply

The SDA 2006 includes four brought out voltage inputs V_{PP}, V_{PI}, V_{DD}, V_{BB} with respect to V_{SS} (ground). Normally, V_{DD} and V_{PI} are externally interconnected. The voltages V_{PH} and V_{PI} are only required during the programming operation. During read out or in the quiescent state, they may also be open or grounded. The values of these voltages are only of influence on the duration, but not on the reliability of the nonvolatile storage operation. Figure 3 shows an appropriate circuit configuration as tuning memory in TV sets.

Inverted level (input INV on high or open)

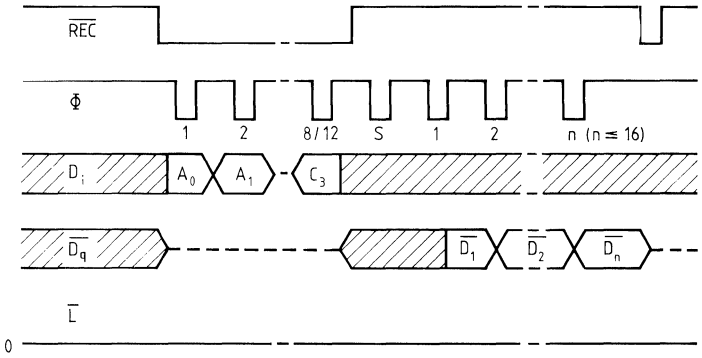


Figure 1a

Non-inverted level (input INV on low)

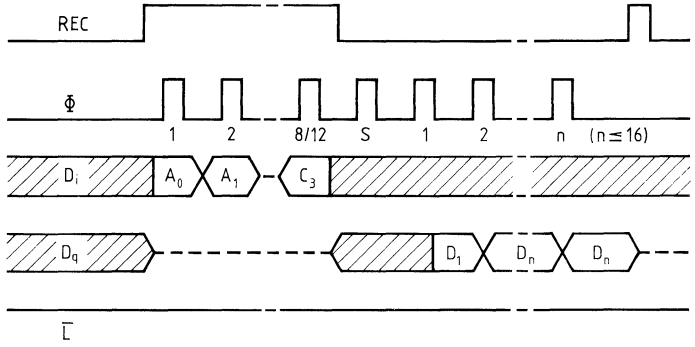


Figure 1b

Figures 1a and 1b Read operation (only the pertinent active levels are indicated)

Inverted level (input INV on high or open)

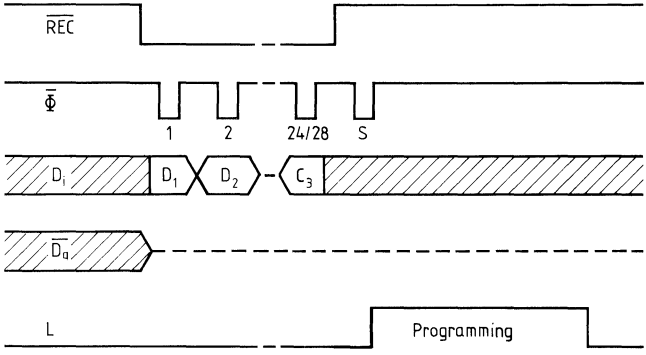


Figure 2a

Non-inverted level (input INV on low)

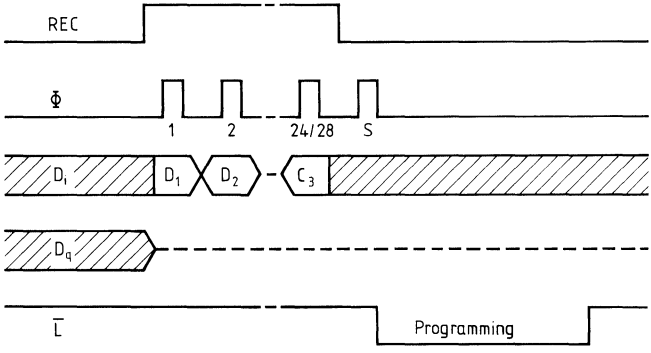


Figure 2b

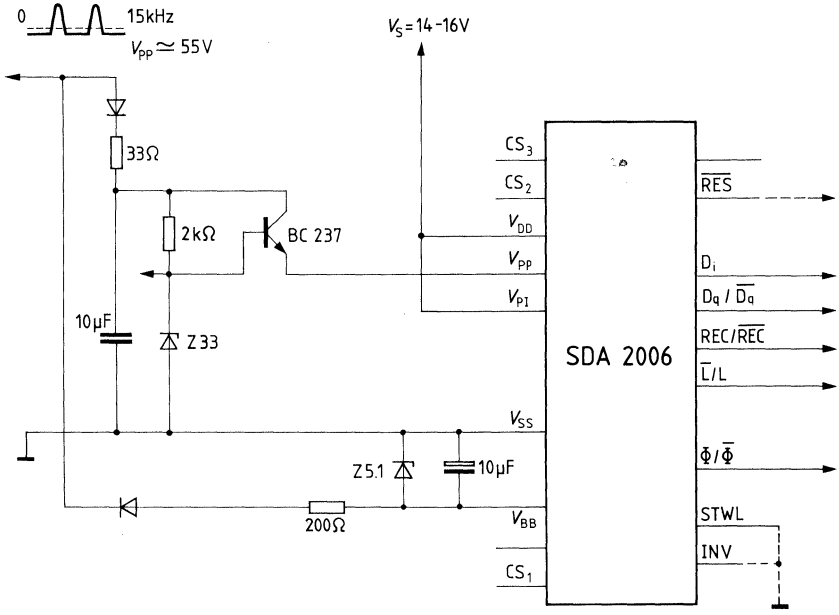
Figures 2a and 2b Programming operation (only the pertinent active levels are indicated)

Pin designation

Pin No.	Symbol	Function
1	V_{BB}	Substrate bias
2	V_{DD}	Supply voltage
3	V_{PP}	Programming voltage
4	STWL	Control word length 12 or 8 bits (input) (12 bits for high or open)
5		Remains open
6	$\overline{RES}$	Reset input
7		Remains open
8	D_i	Data input
9	CS_3	Chip select input (8-bit or 12-bit control word)
10	CS_2	Chip select input (12-bit control word)
11	CS_1	Chip select input (12-bit control word)
12	$\Phi/\overline{\Phi}$	Clock input *
13	$\overline{L}/L$	Programming signal output (load) *
14	$D_q/\overline{D}_q$	Data output*
15	INV	Signal inverting (input)
16	REC/$\overline{REC}$	Data input control input (receive) *
17	V_{SS}	Ground
18	V_{PI}	Write voltage

*) First polarity for INV on low; second polarity for INV on high.

Figure 3: SDA 2006 as tuning memory in TV sets



MOS circuit

The SDA 2007 IC is a further development of the SAB 3209 and SAB 4209 ICs. Like these it utilizes the proven biphase code for IR transmission. The SDA 2007 can be applied with the SAB 3210 as well as with the SDA 2008 as IR instruction generator. This IC is particularly intended for operation with the tuning system SDA 200. It does not contain a program memory which is now included in the channel processor SDA 2003.

- 2 combined serial interfaces with common data line for information transfer
- Microprocessor suitable serial interface
- Front-end control for volume storage, standby and keyboard changeover
- 2 T F-F spare outputs
- Switchable startbit

Type	Ordering code	Package outline
SDA 2007	Q 67100-Y504	DIP 18

Maximum ratings (all voltages referred to $V_{DD} = 0$ V)

Supply voltage range	V_{SS}	0 to 18	V
Input voltage	V_i	0 to V_{SS}	V
Power dissipation, each output	P_q	100	mW
Total power dissipation	P_{tot}	500	mW
Storage temperature range	T_{stg}	−55 to 125	°C

Range of operation (referred to $V_{DD} = 0$ V)

Supply voltage range	V_{SS}	11 to 16	V
Ambient temperature range	T_{amb}	0 to 70	°C

Characteristics (all voltages referred to V_{DD} = 0 V)

		min	typ	max	
Supply current (V_{SS1} = 16 V)	I_1		10	20	mA
Input CLCK					
Clock frequency	f_{CL2}	20	62.5	70	kHz
Coupling capacitor	C_C	10			nF
Inputs VPM, STBT					
H input voltage	$V_{iH14,16}$	$V_{SS}-1$		V_{SS}	V
L input voltage	$V_{iL14,16}$	0		$V_{SS}-7$	V
Input RSIG					
H input voltage	V_{iH17}	$V_{SS}-1$		V_{SS}	V
L input voltage	V_{iL17}	0		$V_{SS}-3.5$	V
L pulse width	t_{WL}	2			µs
Input resistance	R_{i17}	0.2			MΩ
Input ONOFF					
H input voltage ($\lvert I_{iH7} \rvert$ <1 mA)	V_{iH7}	$V_{SS}-1$		V_{SS}	V
Outputs TUS_1, TUS_2, ONOFF, RSV_1, RSV_2					
H output voltage (Test circuit 1)	$V_{qH5,6,7,8,9}$	$V_{SS}-1.5$		V_{SS}	V
L output voltage (Test circuit 2)	$V_{qL5,6,7,8,9}$	0		0.35	V
Outputs TE, DLE, DATA					
H output voltage (Test circuit 3)	$V_{qH3,4,15}$	$V_{SS}-2$		V_{SS}	V
L output voltage (Test circuit 4)	$V_{qL3,4,15}$	0		0.35	V
Outputs CONT, COLO, BRIG, VOLU					
H output voltage (Test circuit 3)	$V_{qH10,11,12,13}$	$V_{SS}-1.5$		V_{SS}	V
L output voltage (Test circuit 2)	$V_{qL10,11,12,13}$	0		0.35	V

Circuit description

The circuit is used as receiver for IR remote control of TV sets. It includes two combined serial interfaces for universal extensions and is especially suitable for use in connection with the tuning system SDA 200.

1. **IR receiver**

Pin RSIG

It accepts the IR signal and outputs the received instructions at the serial interface.

The IR signal consists of ac pulses at a frequency of approx. 30 kHz and a duration of approx. 0.5 msec. per pulse group. The instructions are transferred as 7-bit words (1 start bit and 6 information bits) in the biphase code (see timing diagram 1).

Pin STBT

Via the input STBT, the receiver can be changed to a negated start bit (e.g. for separation between TV and broadcasting remote control).

In this context, there is:

STBT = H → start bit = 1
STBT = L → start bit = 0

2. **Serial interface (I bus)**

Pins DATA, DLE, TE

Both the combined serial interfaces utilize the pin DATA via which the actual information (leading bit LB and 6 information bits) is serially processed. They differ by their different enable signals DLE and TE which may appear at the TUS_1 or TUS_2 output depending on their level and instruction (see also timing diagram of the I bus output):

	TUS_1	TUS_2	DLE output	TE output
TV level	L	L	all instructions in the repeat mode	all instructions in the repeat mode
Text level	H	L	DLE = L	except the instructions 2 and 62, all instructions in single mode (without end instruction)
Spare level	L	H		

The output stages are open-drain stages with included load resistances.

3. **Analog value memory**

Pins VOLU, BRIG, COLO, CONT

The circuit includes 4 memories for the setting of volume, brightness, color saturation, and contrast.
There are approx. 60 stages of analog output voltage adjustment. The adjustment speed corresponds to the repetition frequency of the repeat instructions (approx. 8 Hz). The voltages are output as square-wave voltage at a frequency of approx. 1 kHz, with the duty cycle corresponding to the analog value. The analog voltage is provided in an external lowpass by forming the mean time value.
It is the instruction "normal position" which moves the analog value memory into a mask-programmable normal position; here these are: $\nu_{VOLU} = 1/3$, $\nu_{BRIG} = \nu_{COLO} = \nu_{CONT} = 1/2$ with $\nu = t_{high}/T$; the same normal position is achieved when the supply voltage rises starting from zero.

The standby status keeps all analog memory outputs on low level — the last set analog values remain stored.

Quicktone

The volume output is kept on low level as long as the quicktone flipflop is set. The instruction "quicktone" moves the flipflop into the complementary status.

The flipflop is reset
- by the instruction "volume+"
- by the status "standby"
- by the instruction "normal"
- by the instructions 16 to 25 (digits 0 to 9), however not, if TUS_1 or TUS_2 is set to high level.
- by the instruction "TUS_1" or "TUS_2".

Pin VPM

The input VPM provides front-end operation for the volume storage VOLU. If this pin is applied to high (low) it corresponds to the input of the instruction "volume+(−)".

The adjustment speed of the memory is the same as for operation via the transmitter (approx. 8 Hz).

4. **Standby input/output ONOFF**

This pin controls the mains via a transistor. The output can be set into both positions from outside.

Low ≙ on, high ≙ standby

The preferred position is high. It is set

— when the operating voltage is switched on
— when the instruction 2/"Standby" is given.

With the instructions 5 to 7 and 16 to 25 the status "low/on" is set.

5. **Keyboard changeovers**

Pin TUS_1 and TUS_2

The outputs are controlled by an alternating flipflop, each. Every pressure on the appropriate button of the transmitter causes a change of the pertinent output into the complementary status. Both outputs can be set from outside into both positions.

The preferred position is low (TV set operation).
It is set

— when the supply voltage is switched on,
— when the standby mode exists

If TUS_1 or TUS_2 are on high level, DLE remains on low level. The instructions are then only issued via the serial interface TE/DATA as single instructions[1]). Not every instruction is encoded in the receiver (see instruction set).

The status TUS_2 = H (TUS_1 = H) resets TUS_1 (TUS_2) to low.

6. **Spare functions**

Pins RSV_1 and RSV_2

The outputs are controlled by a T flipflop, each. With every pressure on the relevant button of the transmitter, the output changes to the complementary status. It can also be set from outside into both states.

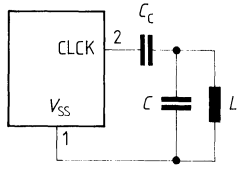
The preferred position of RSV_1 is high, that of RSV_2 low.

It is set:

— when the operating voltage is switched on
— when the status "Standby" exists
— when the instruction "normal" is output.

1) The instruction 2/"Standby" results in ONOFF = H; thus, also TUS_1 and TUS_2 are reset to low and single mode is abolished. If TUS_1 or TUS_2 is on high, the first instruction No. 62 "end instruction" is suppressed. All other end instructions following immediately, are, however, output. (In single mode, the further output of an instruction at pin TE is blocked until an end instruction releases the blocking. Further immediately following end instructions are, therefore, again issued).

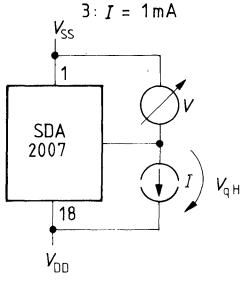
Oscillator connection



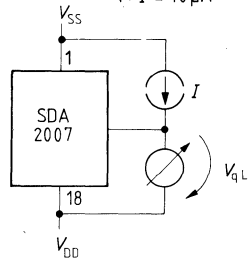
$$f_{CLCK} \approx \frac{1}{2\pi\sqrt{LC}}$$

Test circuits

Test circuit 1: I = 0.3mA
3: I = 1mA



Test circuit 2: I = 1µA
4: I = 10µA



Code table, LB (leading bit) = H

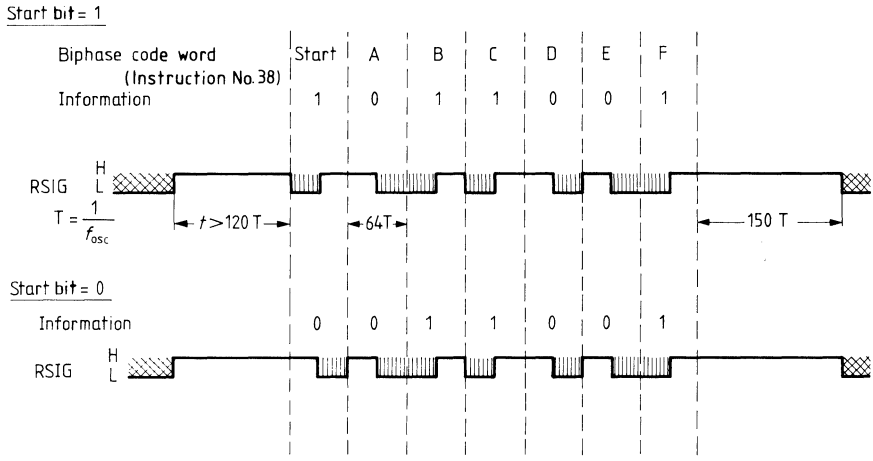
Instruction No.	F E D	C B A	Function at TUS_1 = L, TUS_2 = L	Function at TUS_1 = H, TUS_2 = L	Function at TUS_1 = L, TUS_2 = H
0	L L L	L L L	Normal	Normal	—
1		L L H	Quicktone	Quicktone	—
2		L H L	Standby	Standby	Standby
3		L H H	Spare 1	—	—
4		H L L	—	—	—
5		H L H	TUS_1/On	TUS_1	TUS_1
6		H H L	A previous prog.	—	—
7		H H H	TUS_2/On	TUS_2	TUS_2
8	L L H	L L L	Volume +	Volume +	—
9		L L H	Volume −	Volume −	—
10		L H L	Brightness +	Brightness +	—
11		L H H	Brightness −	Brightness −	—
12		H L L	Color +	Color +	—
13		H L H	Color −	Color −	—
14		H H L	Contrast +	Contrast +	—
15		H H H	Contrast −	Contrast −	—
16	L H L	L L L	On	—	—
17		L L H	On	—	—
18		L H L	On	—	—
19		L H H	On	—	—
20		H L L	On	—	—
21		H L H	On	—	—
22		H H L	On	—	—
23		H H H	On	—	—
24	L H H	L L L	On	—	—
25		L L H	On	—	—
26		L H L	—	—	—
27		L H H	—	—	—
28		H L L	—	—	—
29		H L H	—	—	—
30		H H L	—	—	—
31		H H H	—	—	—
32	H L L	L L L	Spare 2	—	—
33		L L H	—	—	—
34		L H L	—	—	—
35		L H H	—	—	—
36		H L L	—	—	—
37		H L H	—	—	—
38		H H L	—	—	—
39		H H H	—	—	—
40	H L H	L L L	—	—	—
41		L L H	—	—	—
42		L H L	—	—	—
43		L H H	—	—	—
44		H L L	—	—	—
45		H L H	—	—	—
46		H H L	—	—	—
47		H H H	—	—	—

Code table (cont'd), LB (leading bit) = H

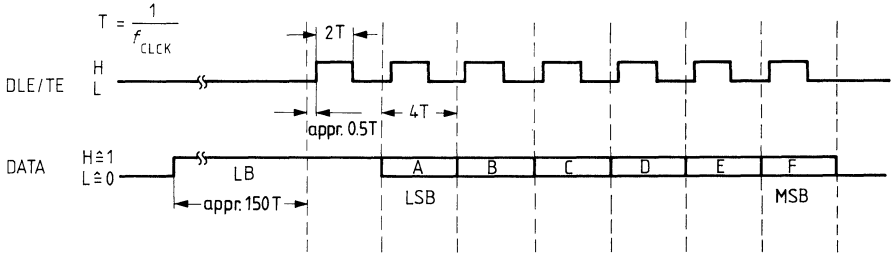
Instruction No.	F E D	C B A	Function at TUS_1 = L, TUS_2 = L	Function at TUS_1 = H, TUS_2 = L	Function at TUS_1 = L, TUS_2 = H
48	H H L	L L L	—	—	—
49		L L H	—	—	—
50		L H L	—	—	—
51		L H H	—	—	—
52		H L L	—	—	—
53		H L H	—	—	—
54		H H L	—	—	—
55		H H H	—	—	—
56	H H H	L L L	—	—	—
57		L L H	—	—	—
58		L H L	—	—	—
59		L H H	—	—	—
60		H L L	—	—	—
61		H L H	—	—	—
62		H H L	End-instruction	End-instruction	End-instruction
63		H H H	not permitted	not permitted	not permitted

Timing diagrams

IR biphase coding



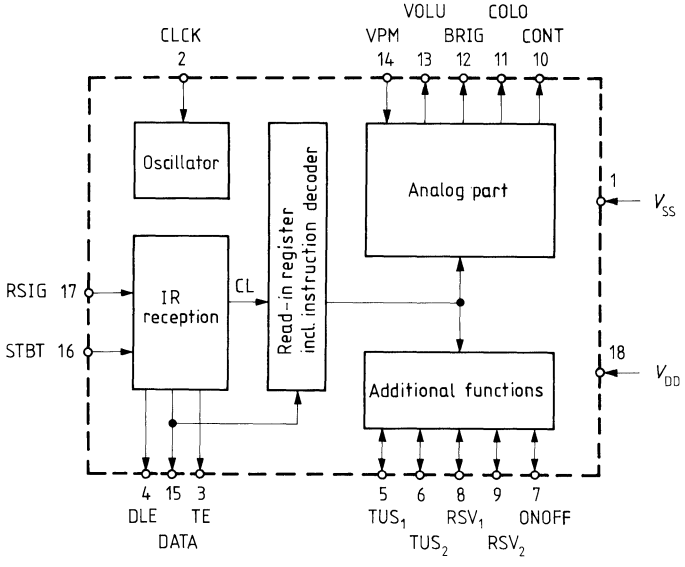
I bus output



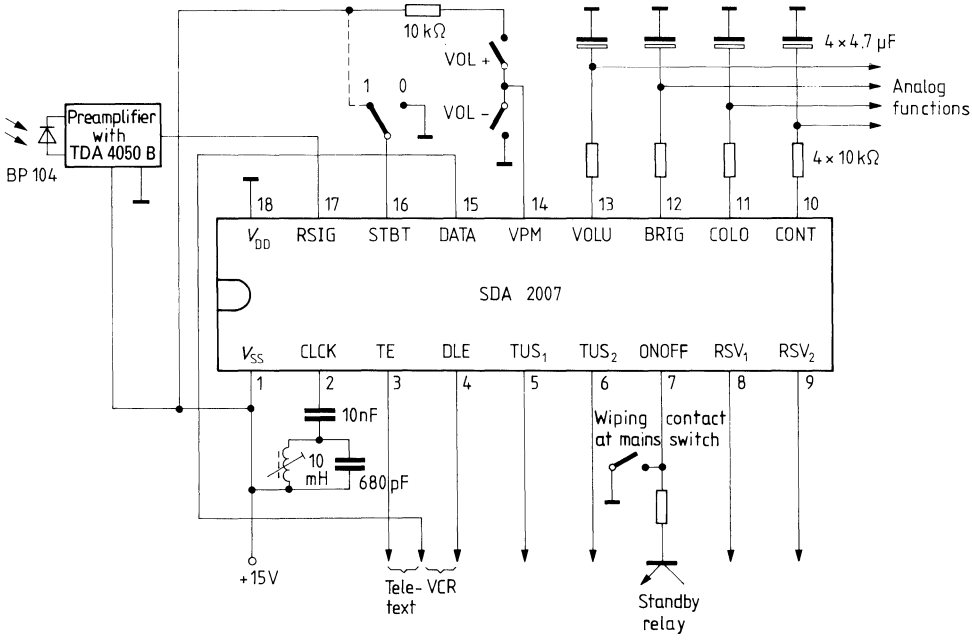
Pin designation

Pin No.	Symbol	Function
1	V_{SS}	Supply voltage + pole
2	CLCK	osc. input
3	TE	Text enable + clock
4	DLE	TV enable + clock
5	TUS_1	Keyboard changeover 1
6	TUS_2	Keyboard changeover 2
7	ONOFF	Standby output
8	RSV_1	Spare 1
9	RSV_2	Spare 2
10	CONT	Analog memory
11	COLO	Analog memory
12	BRIG	Analog memory
13	VOLU	Analog memory
14	VPM	Front-end control for VOLU
15	DATA	Serial interface
16	STBT	Start bit changeover
17	RSIG	IR input
18	V_{DD}	Supply voltage -pole

Block diagram



Application circuit



MOS circuit

The SDA 2008 IC is a further development of the infrared transmitter IC SAB 3210. It includes a disconnectable 8-stage divider, thus enabling the oscillator to operate up to 500 kHz with a ceramic oscillator instead of an LC circuit.

- Complete security of the keyboard against operating errors
- Instruction expandability up to 60 instructions is possible by using diodes and additionally by means of a shift button (keyboard changeover)
- Programmable start bit by external voltage
- Wide supply voltage range between 5 V and 16 V
- Low current consumption, typically 3 mA. The battery can be switched off by an external transistor
- With the aid of special contacts, ASC II transmission with 64 instructions is possible
- No external column resistors necessary

Type	Ordering code	Package outline
SDA 2008	Q67100-Y503	DIP 18

Maximum ratings (all voltages referred to $V_{DD} = 0$ V)

Supply voltage	V_{SS}	18	V
Input voltage	V_i	18	V
Power dissipation per output	P_q	100	mW
Total power dissipation	P_{tot}	500	mW
Storage temperature range	T_{stg}	−55 to 125	°C

Range of operation (referred to $V_{DD} = 0$ V)

Supply voltage range	$V_{SS\,1}$	5 to 16	V
Supply voltage range [1])	$V_{SS\,1}$	5.5 to 16	V
Ambient temperature range	T_{amb}	0 to 70	°C

[1]) Instruction extension with diodes

Characteristics (all voltages referred to V_{DD})

		min	typ	max	
Supply current (outputs not connected)	I_6		3	7	mA
Leakage current, total current (outputs $V_{q2, 3, 4, 5, 7, 8}$)	$I_{2, 3, 4, 5, 7, 8}$			1	µA
Inputs					
Oscillator input CLCK I					
Operating frequency with prescaler	f_{17}	160		560	kHz
Operating frequency for external clock with disconnected prescaler	f_{17}	20		70	kHz
IRA remote control signal output					
H-output voltage (refer to test circuit) $I_{qH} = 4$ mA; $V_{SS} = 6$ V	$V_{q\,H8}$	$V_{SS}-5$			V
H-resistor with respect to V_{SS}	$R_{q\,H8}$	200			Ω
ETA switch-on transistor output					
H-output current $V_{q7} = V_{SS} - 4$ V	$I_{q\,H7}$	100		10.000	µA

Row input 1 to 8 (internal pull-high resistor)

The row inputs are connected to the column outputs when a command shall be sent.

The maximum resistance of the connection is that of a silicon diode junction in forward direction and in series to that a resistance of 100 Ω. The minimum resistance is zero.

For command extension 2 rows can be connected with one column output.

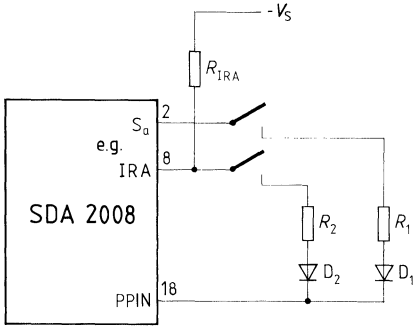
ETA input

The ETA input is connected to the battery voltage via the base-emitter diode of the NPN switching transistor.

PPIN program input

The PPIN input is joined with the corresponding column output or with the IRA output — in this case, the resistance IRA to $-V_S$ should be between 33 kΩ and 47 kΩ — via a diode if a special function is required. Combinations are possible.

In this connection the maximum resistance is that of a silicon diode in forward direction and in series to that a resistance of 100 Ω. The minimum resistance is zero.



Description of function

The SDA 2008 IC works as a transmitter for the infrared remote control system IR 60.

The PMOS circuit contains a control output for an NPN transistor which switches off the supply voltage when no button is pressed (i.e. no row is in "LOW" state).

Input, keyboard

The transmitter contains an input matrix of 8 rows and 4 columns. In order to input an instruction, a row must be connected to a column. Thus, the transmitter is switched on and the appropriate instruction is sent. Without further measures it is possible to issue up to 32 instructions. The instruction set can be extended up to 60 either with the aid of additional diodes (for this purpose 2 diodes are required for each 4 additional instructions) or up to 62 instructions with a shift button. In both cases the additional connection (diodes to row 8 or shift button) is necessary prior to the emission of the first instruction — after that the originally allocated instruction is sent independent of the additional connection.

As a fifth matrix column, $-V_S$ can be used to input the instructions 40 to 47 (without external diode connection using only one button, each).

Operating error

The circuit includes a security lock against multi-operation (depression of several buttons simultaneously). An exception is the double operation inside a column with one of the rows 1 to 7 and row 8, since this combination is used in order to extend the instruction set with the aid of diodes. After transmission of the first infrared instruction after the startbit, there is however also security against this double operation.

Start instruction, end instruction

After the switch-on, the instruction No. 62 is issued as start instruction thus indicating to the receiver the start of the instruction transmission.

In case of an operating error, this instruction is given as a consequence of the security lock. If the button or buttons are released then the chosen instruction is maximally sent once more (depending upon the exact instant of release) and then the instruction No. 62 is sent once as stop before the supply voltage is switched off. There is security against changing one instruction to another than the instruction No. 62.

Output

The transmitter encodes the input in bi-phase code (refer to timing diagram). Prior to the 6 information bits, a presignal and a startbit which can be selected via PPIN, are sent. The presignal enables proper control of the preamplifier on the receiver side, whereas the startbit is used for receiver discrimination. Thus it is possible to control a TV set and a radio in one room independently of each other with the same remote control system.

The output signal is carried at 1/16 of the clock frequency ($f_{CLCKI}/16$) and a pulse duty factor of 1 : 4. With the help of corresponding wiring of the program input PPIN, the carrier can be switched off. Thus any other external carrier can be used.

Instruction interval

The interval between two given instructions (except the start instruction) is approximately 12 times the instruction length (incl. presignal) or 35,536 CLCKI clocks, respectively. This interval can be reduced to 30,976 CLCKI clocks in order to obtain diminished instruction intervals at lower clock frequencies.

Operation at low clock frequency

The prescaler (divide by 8) can be switched off. Thus, operation is possible at a clock frequency of approx. 500 kHz or 62.5 kHz, as required. The prescaler can only be switched off if — at low resistance — the IRA output is not forced to LOW (by means of a base-emitter space), e.g. in the case of wiring for front-end control.

Operation without switching transistor

At operation with a fixed supply voltage (ETA = LOW), the columns a to d are periodically interrogated (H-pulse) in the normal sequence (as if an instruction is emitted) in order to permit an external synchronization.

After the supply voltage has risen from 0 V on, the flow of control is brought into a definite state and starts column addressing. After having recognized a row in the "LOW" state, the flow of control is reset — then the flow corresponds until disconnection to that at battery voltage operation. After the end of the transmission the flow of control continues column addressing, however, without any further output to IRA.

Multi-transmitter operation:

Without great increase in external circuitry it is possible to cascade two SDA 2008 ICs such that these can be multiplexed to give out the instructions. For this purpose it is utilized that the flow of control and the instruction register are reset if the columns a and b are simultaneously on high level.

PPIN connections:

Connect with:	Function
Column a	Shift into second instruction group (bit F = "1"
Column b Column c	Shortened instruction interval Startbit = "0"
Column d	No carrier of the IRA signal
IRA	Bridging the prescaler

(In the case of combinations of these functions, decoupling with diodes according to figure PPIN circuitry is necessary).

ETA circuit:

ETA = V_{DD}	Operation at constant supply voltage. If no row is set to "LOW", IRA is without output, however permanent column addressing.
ETA to base of the voltage commutation transistor	Normal battery operation including disconnection of the supply voltage after the end instruction at open row combination.

Instruction set

No diodes at Z_8
unshifted

Instr. No.	Code FED CBA	Key
0	000 000	1a
1	000 001	1b
2	000 010	1c
3	000 011	1d
4	000 100	2a
5	000 101	2b
6	000 110	2c
7	000 111	2d
8	001 000	3a
9	001 001	3b
10	001 010	3c
11	001 011	3d
12	001 100	4a
13	001 101	4b
14	001 110	4c
15	001 111	4d
16	010 000	5a
17	010 001	5b
18	010 010	5c
19	010 011	5d
20	010 100	6a
21	010 101	6b
22	010 110	6c
23	010 111	6d
24	011 000	7a
25	011 001	7b
26	011 010	7c
27	011 011	7d
28	011 100	8a
29	011 101	8b
30	011 110	8c
31	011 111	8d

shifted

Instr. No.	Code FED CBA	
32	100 000	
33	100 001	
34	100 010	
35	100 011	
36	100 100	
37	100 101	
38	100 110	
39	100 111	
40	101 000	
41	101 001	
42	101 010	
43	101 011	
44	101 100	
45	101 101	
46	101 110	
47	101 111	
48	110 000	
49	110 001	
50	110 010	
51	110 011	
52	110 100	
53	110 101	
54	110 110	
55	110 111	
56	111 000	
57	111 001	
58	111 010	
59	111 011	
60	111 100	
61	111 101	
62	111 110	} end instructions
62	111 110	}

With diodes at Z_8
unshifted and ←shifted

Instr. No.	Code FED BCA	Key
32	100 000	81a
33	100 001	81b
34	100 010	81c
35	100 011	81d
36	100 100	82a
37	100 101	82b
38	100 110	82c
39	100 111	82d
40	101 000	83a
41	101 001	83b
42	101 010	83c
43	101 011	83d
44	101 100	84a
45	101 101	84b
46	101 110	84c
47	101 111	84d
48	110 000	85a
49	110 001	85b
50	110 010	85c
51	110 011	85d
52	110 100	86a
53	110 101	86b
54	110 110	86c
55	110 111	86d
56	111 000	87a
57	111 001	87b
58	111 010	87c
59	111 011	87d

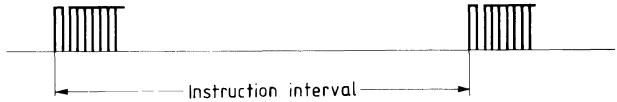
Special group
unshifted and ← shifted

Instr. No.	Code FED CBA	Key
40	101 000	1L
41	101 001	2L
42	101 010	3L
43	101 011	4L
44	101 100	5L
45	101 101	6L
46	101 110	7L
47	101 111	8L

Instruction interval (prescaler switched on)

Interval	Interval in CLCKI clocks	Interval in msec f_{CLCKI} = 500 kHz	PPIN connected to column b
Normal	65536	approx. 131	———
Reduced	30976	approx. 62	X

Definition of the instruction interval



Hints for special functions

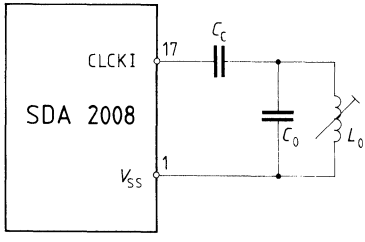
	IR remote control TV/radio sets	Front-end operation TV/radio sets	Transmission via AF cable	Remote control for model rail way	Typewriter keyboard	Time programmable remote control	TV games	Light switch remote control
Start bit changeover	X	X	X	X	X	X	X	
Shift into second group	X	X	X	X		X	X	
Diode matrix	X	X	X	X	X	X	X	
Special instruction group	X	X	X	X	X	X	X	
No carrier		X	X		X			
Bridged prescaler		X						
Shortened instruction interval			X	X				
Cascade connection				X			X	
No debounce delay								X
Special connection			X		X	X		

Pin designation

Pin No.	Description
1	V_{SS}, +supply voltage
2	Column a
3	Column b
4	Column c
5	Column d
6	V_{DD}, -supply voltage
7	ETA (switch-on transistor output)
8	IRA (infrared output)
9	Row 1
10	Row 2
11	Row 3
12	Row 4
13	Row 5
14	Row 6
15	Row 7
16	Row 8
17	CLCKI (oscillator input)
18	PPIN (programming input)

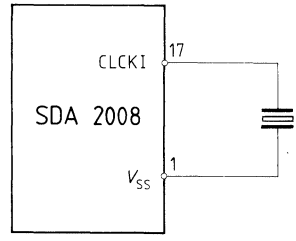
Oscillator connection

1)

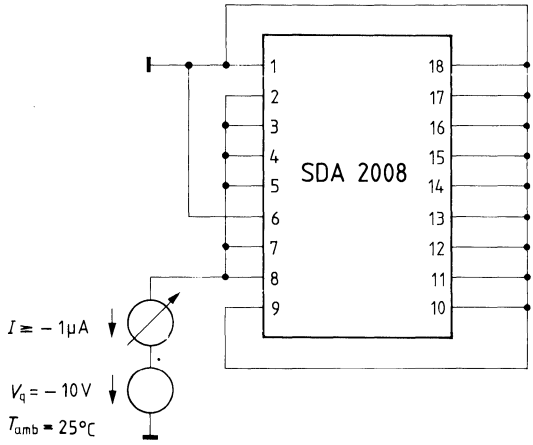


$C_C \geq 10\,nF \quad f_{CLCKI} \approx \frac{1}{2\pi\sqrt{L_0\,C_0}}$

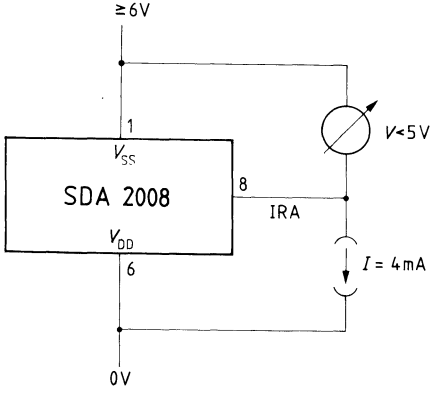
2)



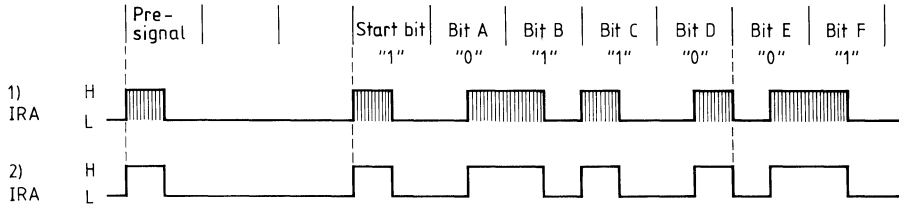
Leakage current, total current (test current)



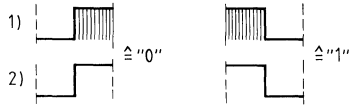
IRA remote control signal output (test circuit)



Biphase coding from instruction 011001

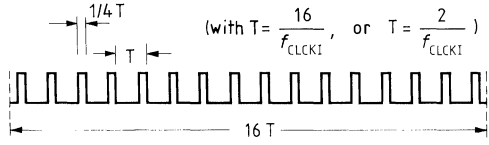


Def: for "0" and "1"

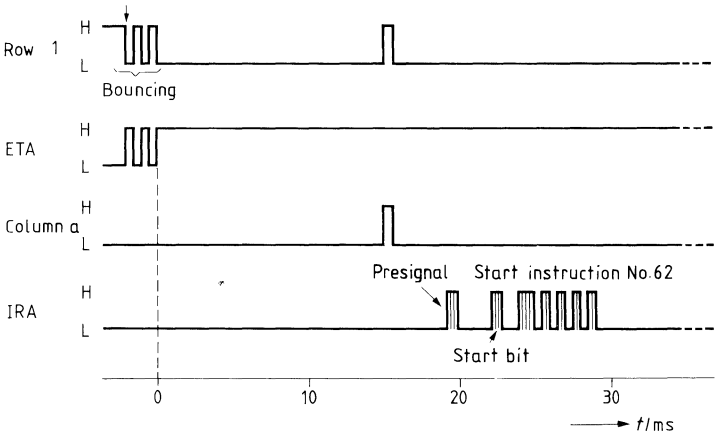


1) with carrier
2) without carrier

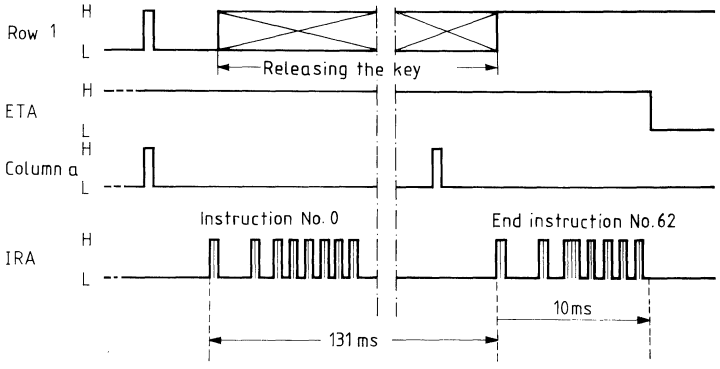
Exact pulse train of a burst for 1):



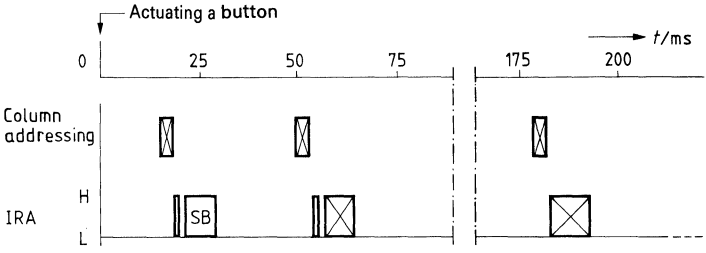
Actuating a button (e.g. 1a), f_{CLCKI} = 500 kHz



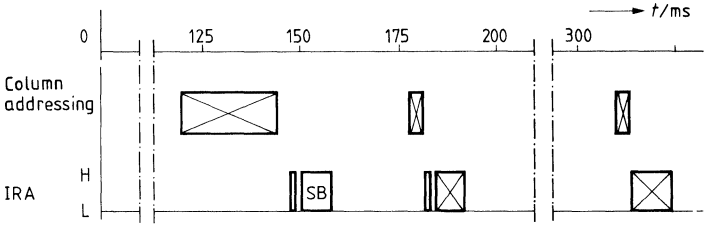
Releasing a button (1a), f_{CLCKI} = 500 kHz



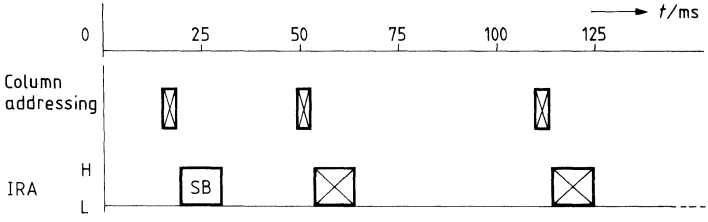
Instruction interval, f_{CLCKI} = 500 kHz



PPIN at IRA (bridged prescaler) f_{CLCKI} = 62.5 kHz

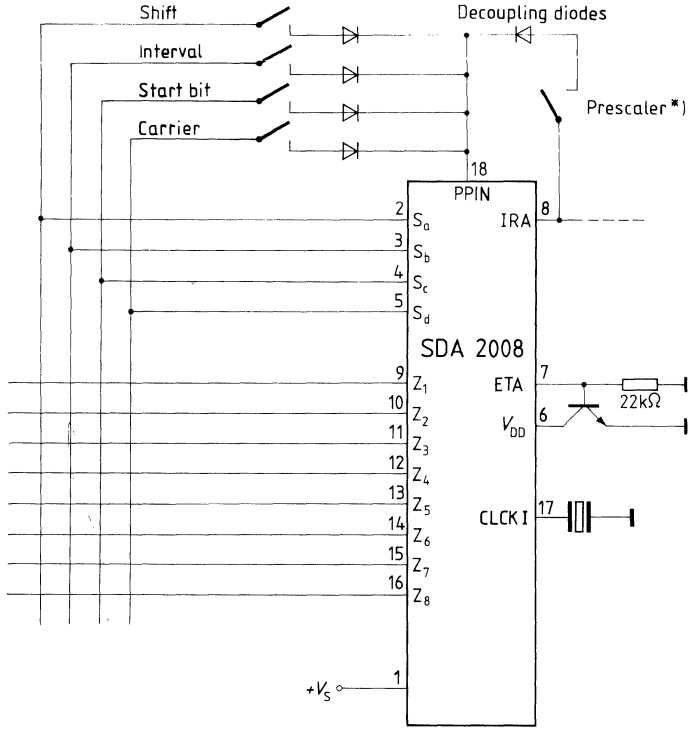


PPIN at column b (shortened instruction interval) f_{CLCKI} = 500 kHz



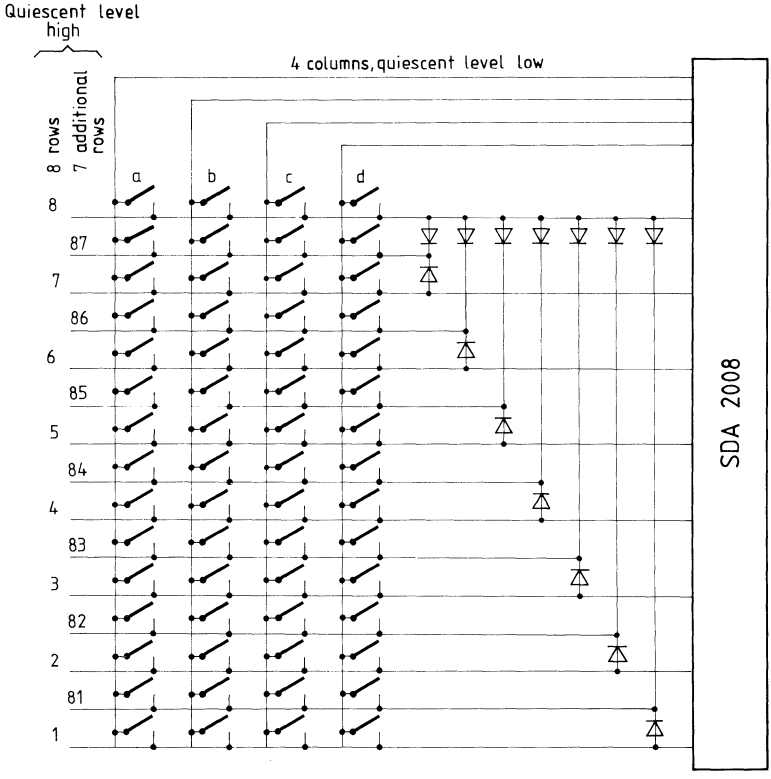
SB:= Instruction No. 62

PPIN connection

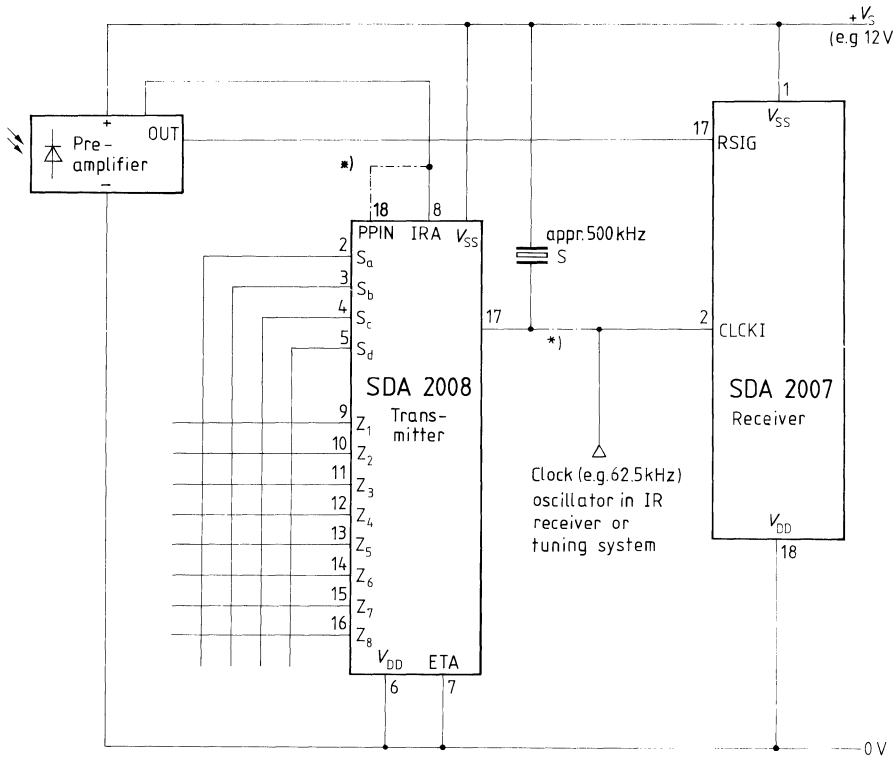


*) Disconnection only possible, if IRA is not set to $-V_S$ at low impedance.

Extension for 60 instructions with additional diodes

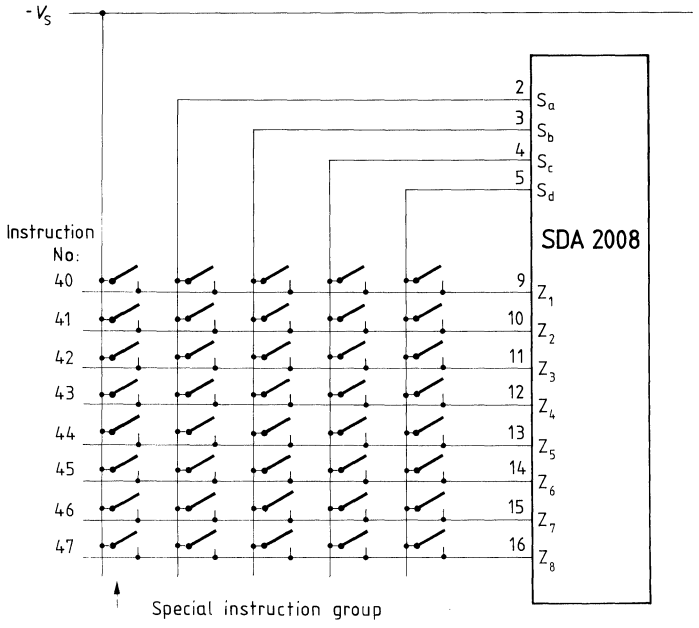


Application circuit for front-end control

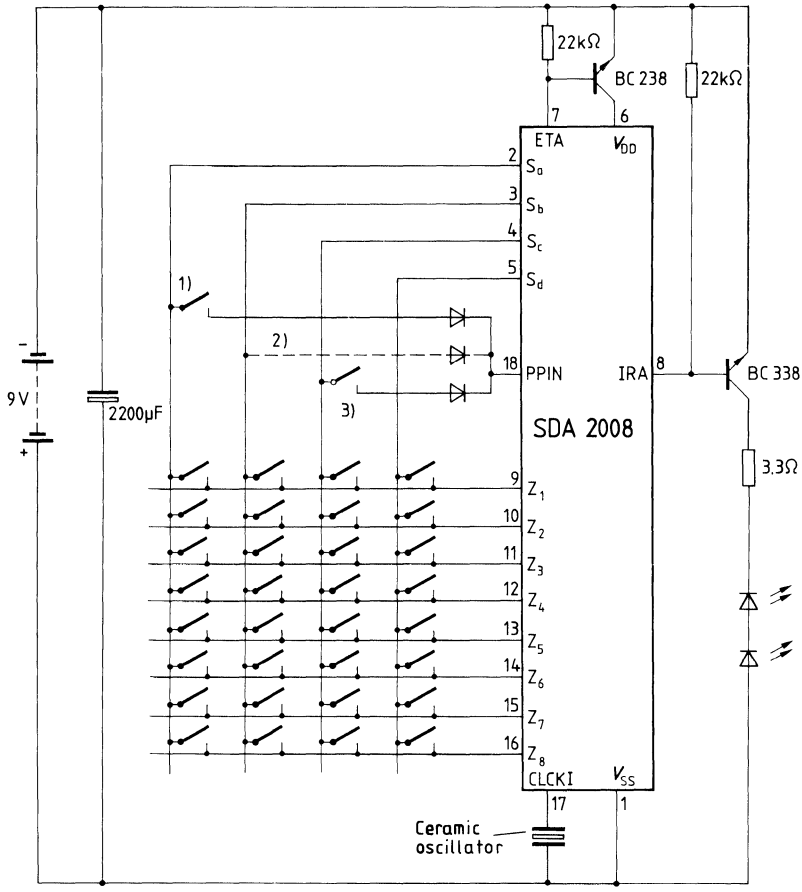


*) alternative to ceramic oscillator S

— V_S as fifth matrix column

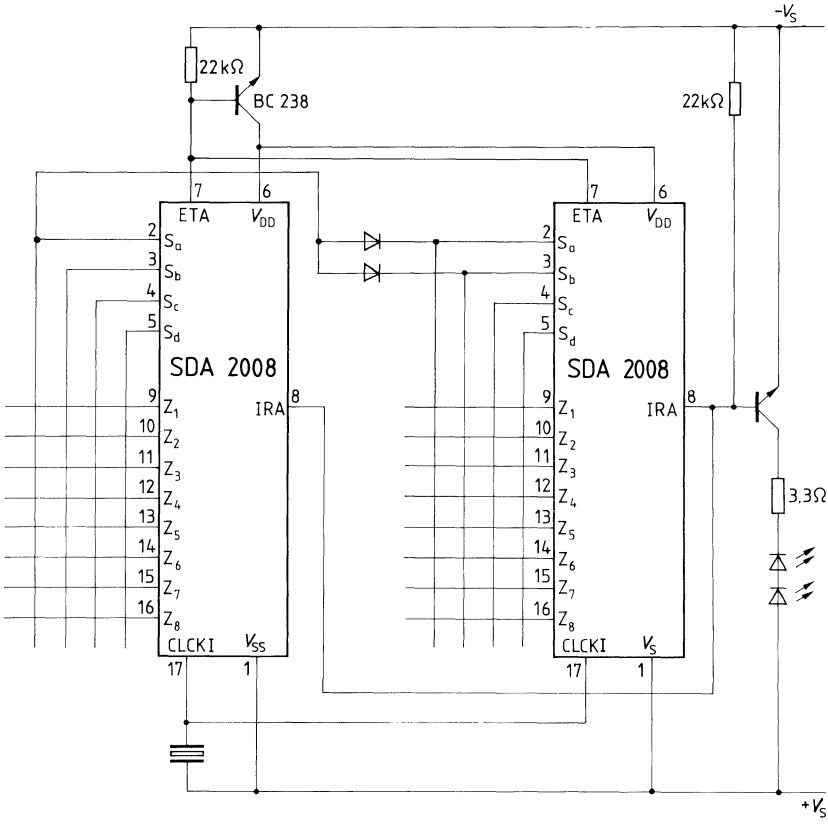


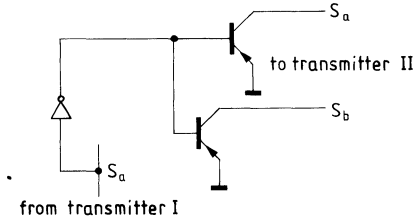
Application circuit



1) Shift button
2) Connection for shortened instruction interval
3) Start bit changeover

External connection for cascading of two SDA 2008





ICs for Special Broadcasting Applications

Tuners
IF stage
System for the reception of road traffic transmitters (ARI)
Voltage synthesis
Frequency counters
Stereo decoders
ICs for cassette and tape recorders

Bipolar circuit

Symmetrical mixer for frequencies up to 200 MHz. It can be driven from an external source or from the built-in oscillator. The input signals are suppressed at the outputs. In addition to the usual mixer applications in receivers, converters, and demodulators for AM and FM, the S 042 can also be used as an electronic polarity switch, multiplier etc.

- Versatile application
- Wide range of supply voltage
- Few external components
- High conversion transconductance
- Low noise figure

Type	Ordering code	Package outline
S 042 P	Q67000-A335	DIP 14
S 042 E	Q67000-A627	5 J 10 DIN 41873/sim. to TO 100

Maximum ratings

Supply voltage		V_S	15	V
Storage temperature range		T_{stg}	−40 to 125	°C
Junction temperature		T_j	150	°C
Thermal resistance (system-air)	S 042 P:	$R_{th\ SA}$	90	K/W
	S 042 E:	$R_{th\ SA}$	190	K/W

Range of operation

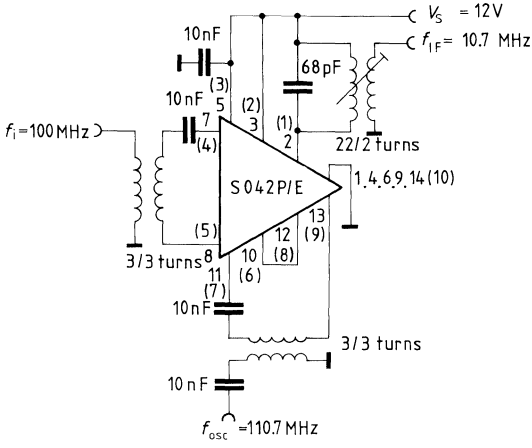
Supply voltage range	V_S	4 to 15	V
Ambient temperature range	T_{amb}	−15 to 70	°C

Characteristics (V_S = 12 V, T_{amb} = 25° C)

		min	typ	max	
Current consumption	$I_S = I_2 + I_3 + I_5$	1.4	2.15	2.9	mA
Output current	$I_2 = I_3$	0.36	0.52	0.68	mA
Output current difference	$I_3 - I_2$	−60		60	mA
Supply current	I_5	0.7	1.1	1.6	mA
Power gain (f_i = 100 MHz, f_{osc} = 110.7 MHz)	G_p	14	16.5		dB
Breakdown voltage ($I_{2,3}$ = 10 mA; $V_{7,8}$ = 0 V)	V_2, V_3	25			V
Output capacitance	$C_{2\text{-}M}$, $C_{3\text{-}M}$		6		pF
Conversion transconductance (f = 455 kHz)	$S = \frac{I_2}{V_7 - V_8} = \frac{I_3}{V_7 - V_8}$		5		mS
Noise figure	NF		7		dB

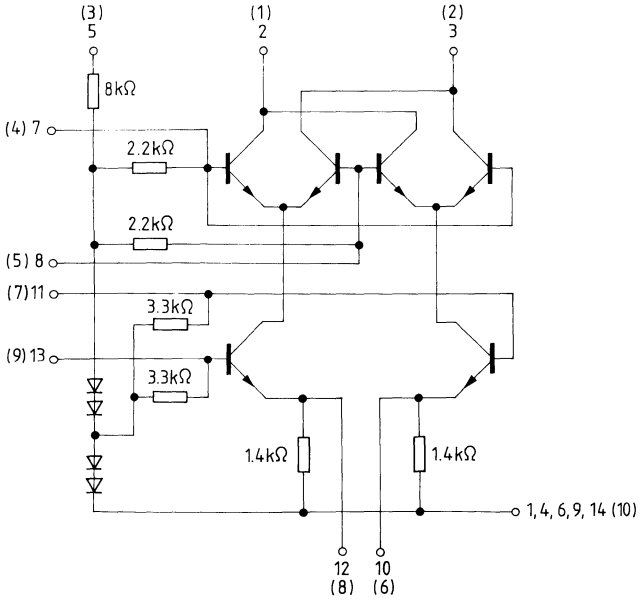
All connections mentioned in the index are referred to S 042 P (e.g. I_2)

Test circuit



Connections in parentheses apply to S 042 E

Circuit diagram

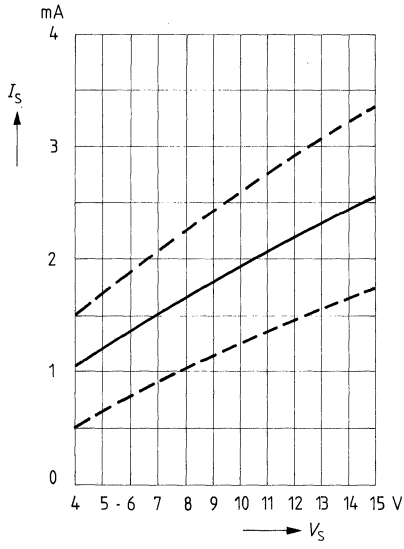


Connections in parentheses apply to S 042 E

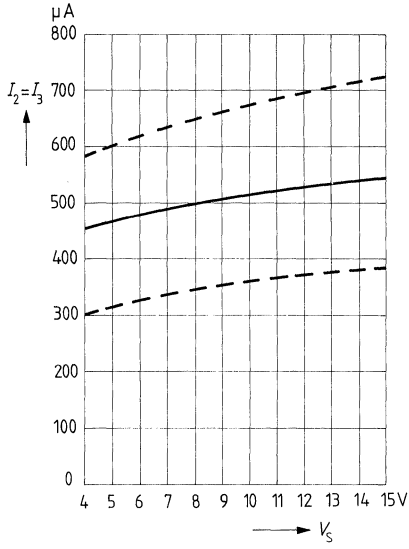
A galvanic connection between pins 7 and 8 and pins 11 and 13 through coupling windings is recommended.

Between pins 10 and 14 (ground) and between pins 12 and 14, one resistance each of at least 200 Ω may be connected to increase the currents and thus the conversion transconductance. Pins 10 and 12 may be connected through any impedance. In case of a direct connection between pins 10 and 12, the resistance from this pin to 14 may be at least 100 Ω. Depending on the layout, a capacitor (10 to 50 pF) may be required between pins 7 and 8 to prevent oscillations in the VHF band.

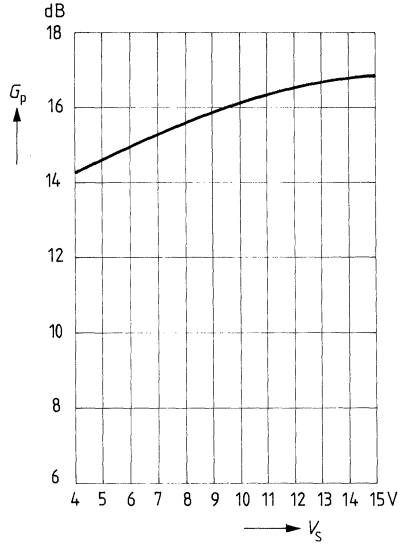
Total current consumption versus supply voltage



Output voltages versus supply voltage

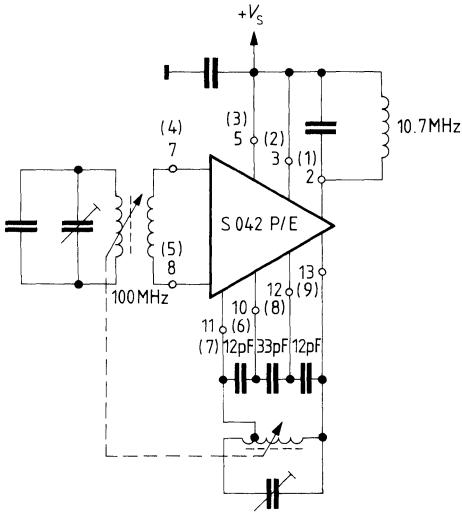


Power gain versus supply voltage



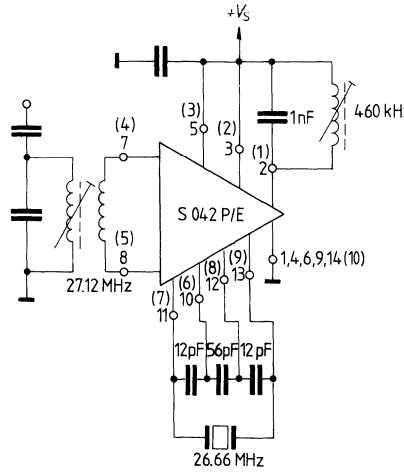
Application circuits

VHF mixer with inductive tuning



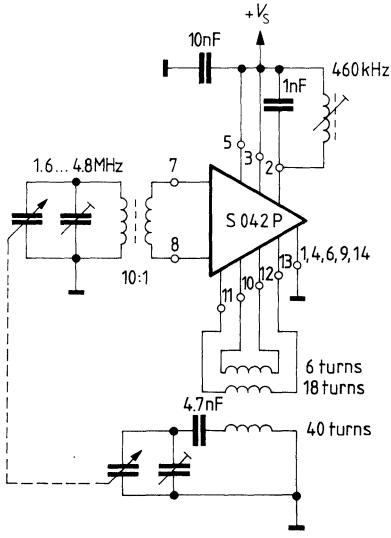
Connections in parentheses apply to S 042 E

Mixer for remote control receivers without oscillator



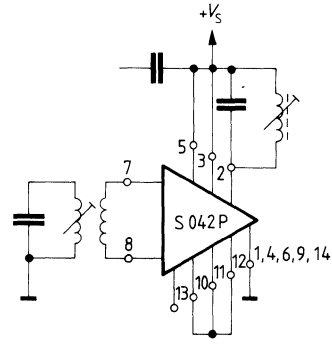
Connections in parentheses apply to S 042 E

Mixer for short wave application in self-oscillating operation



For overtone crystals an adequate inductance is recommended between pins 10 and 12 to avoid oscillations to the fundamental tone.

Differential amplifier with internal neutralization, also suited for use as limiter for frequencies up to 50 MHz, at higher currents up to 100 MHz



FM IF Amplifiers with Demodulator

S 041 P
S 041 E

Bipolar circuit

S 041 is a symmetrical, six-stage amplifier with symmetrical coincidence demodulator for the amplification, limiting and demodulation of frequency-modulated signals. S 041 is particularly suited for sets where low current consumption is of importance, or where major supply voltage fluctuations occur.
The pin configuration corresponds to the well-known TBA 120. Pin 5 of S 041 P, however, is not connected internally. The S 041 is especially suited for applications in narrow-band FM systems (455 kHz) and in usual FM IF systems (10.7 MHz).

- Good limiting properties
- Wide voltage range
- Low current consumption
- Few external components

Type	Ordering code	Package outline
S 041 P	Q67000-A529	DIP 14
S 041 E	Q67000-A694	5 J10 DIN 41873/T 0-100

Maximum ratings

Supply voltage		V_S	15	V
Storage temperature range		T_{stg}	−40 to 125	°C
Junction temperature		T_j	150	°C
Thermal resistance (system-air)	S 041 P	$R_{th\ SA}$	90	K/W
	S 041 E	$R_{th\ SA}$	190	K/W

Range of operation

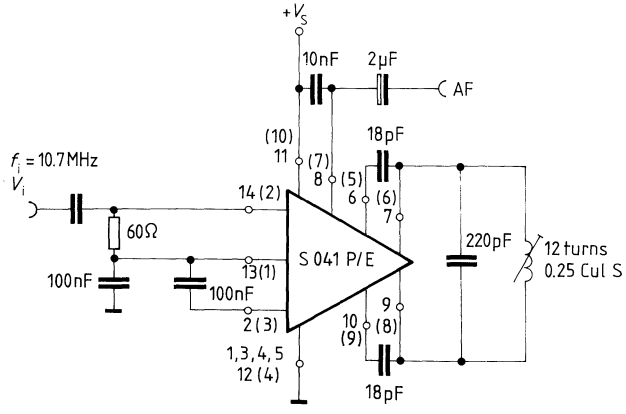
Supply voltage range	V_S	4 to 15	V
Frequency range	f_i	0 to 35	MHz
Ambient temperature range	T_{amb}	−25 to 85	°C

Characteristics (V_S = 12 V, Q approx. 35, f_{mod} = 1 kHz, T_{amb} = 25 °C)

		min	typ	max	
Current cunsumption	I_S	4	5.4	6.8	mA
AF output voltage (f_i = 10.7 MHz, Δf = ± 50 kHz, V_i = 10 mV)	$V_{q\ rms}$	100	170		mV
Total harmonic distortion (f_i = 10.7 MHz, Δf = ± 50 kHz, V_i = 10 mV)	THD		0.55	1	%
Deviation of AF output voltage (V_S = 15 V → 4 V, f_i = 10.7 MHz, Δf = ± 50 kHz)	ΔV_q		1.5		dB
Input voltage for limiting (f_i = 10.7 MHz, Δf = ± 50 kHz)	$V_{i\ lim}$		30	60	µV
IF voltage gain (f_i = 10.7 MHz)	G_v		68		dB
IF output voltage for limiting (each output)	V_{qpp}		130		mV
Input impedance f_i = 10.7 MHz	Z_i		20/2		kΩ/pF
f_i = 455 kHz	Z_i		50/4		kΩ/pF
Output resistance (pin 8)	R_q	3.5	5	8.5	kΩ
Voltage drop at AF ballast resistance	V_{11-8}		1.5		V
AM suppression (V_i = 10 mV, Δf = ± 50 kHz, m = 30%)	a_{AM}		60		dB

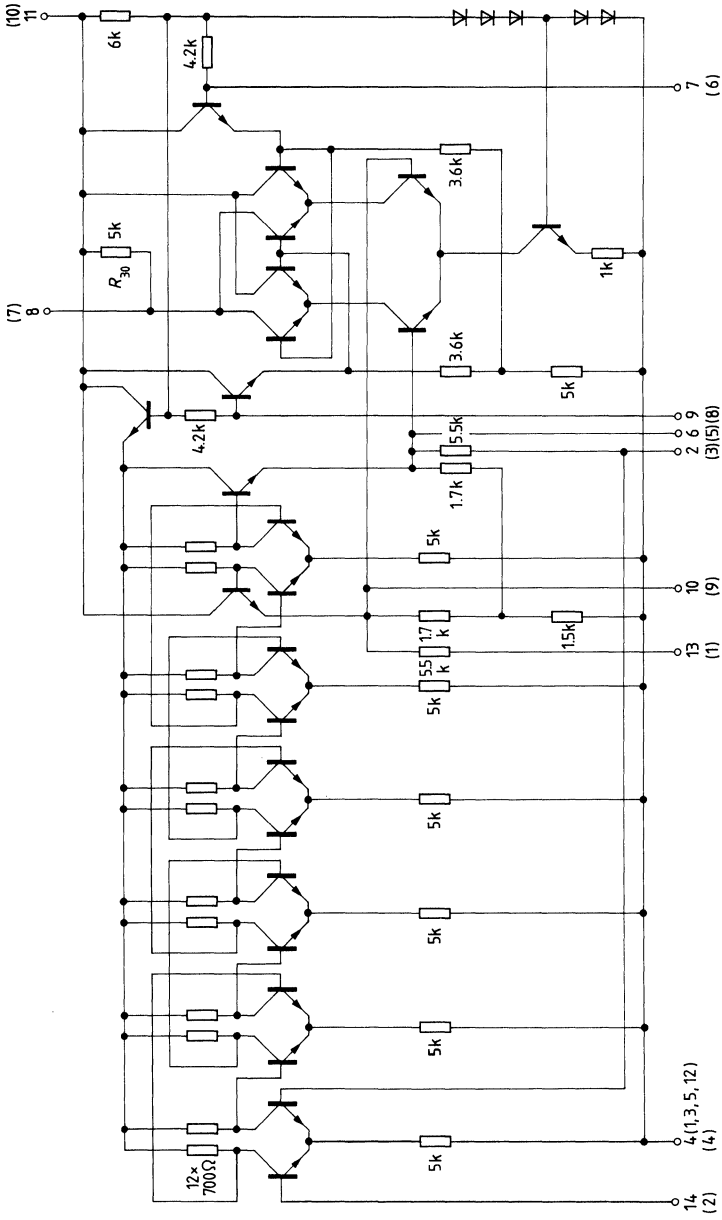
All connections mentioned in the index are referred to S 041 P (e.g. V_{11})

Test circuit



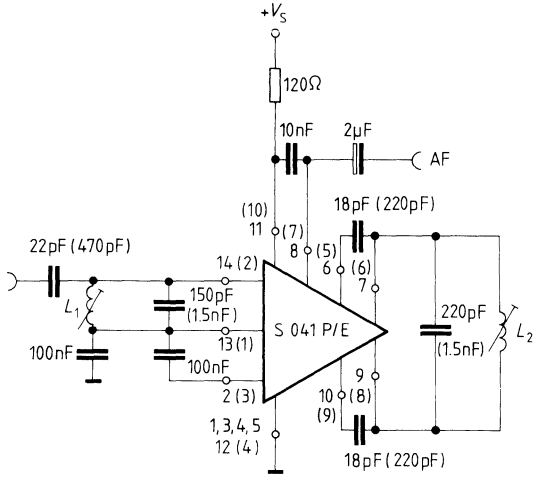
Connections in parentheses apply to S 041 E

Circuit diagram



Connections in parentheses apply to S 041 E

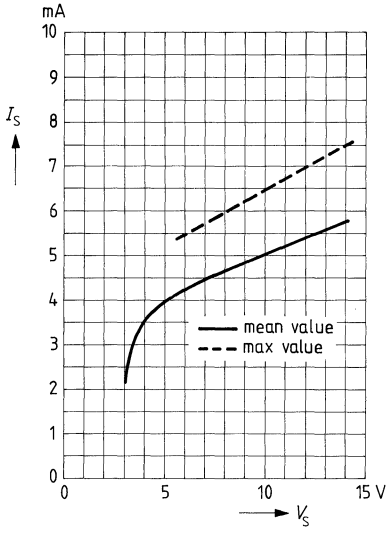
Application circuit for 10.7 MHz (FM-IF)
and 455 kHz (narrow-band-FM)



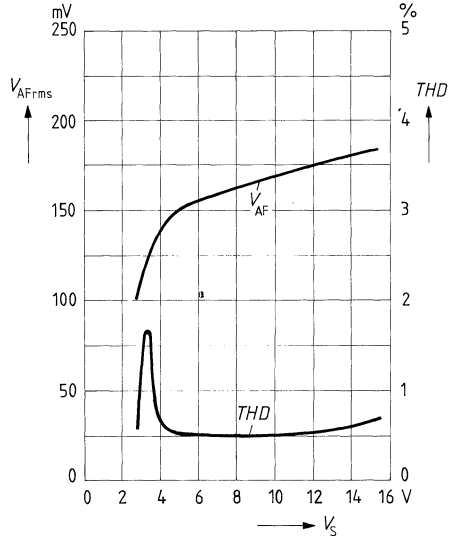
Data in parentheses for 455 kHz (narrow-band FM)
Connections in parentheses apply to S 041 E

Coils	10.7 MHz	455 kHz
L_1	15 turns/0.15 CuLS	71.5 turns/12 × 0.04 CuLS
L_2	12 turns/0.25 CuLS	71.5 turns/12 × 0.04 CuLS
Coil set	D 41 – 2165	D 41 – 2393 of Messrs. Vogt

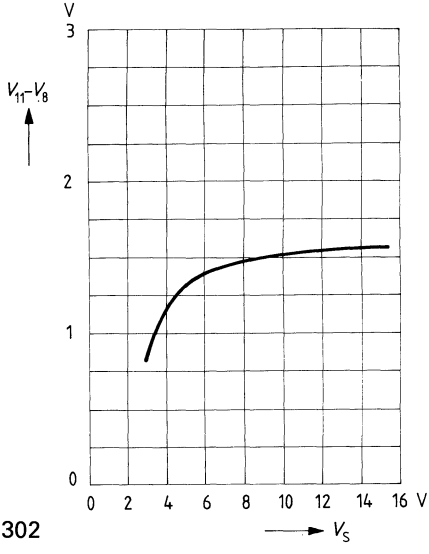
Current consumption versus supply voltage



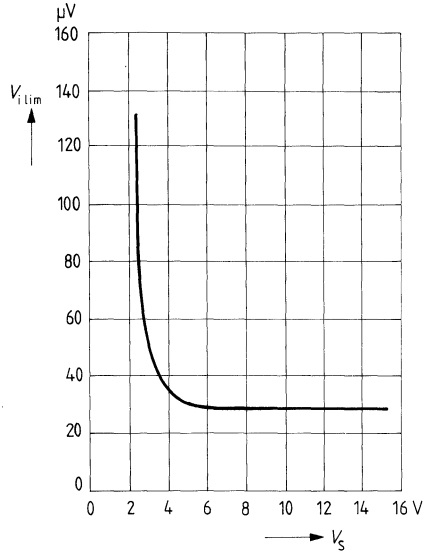
AF output voltage and total harmonic distortion versus supply voltage
f_i = 10.7 MHz; Δf = ± 50 kHz;
f_{mod} = 1 kHz; Q approx. 35



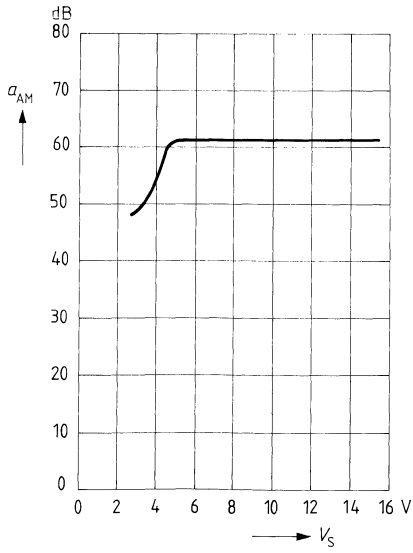
DC output voltage difference versus supply voltage
(without signal)



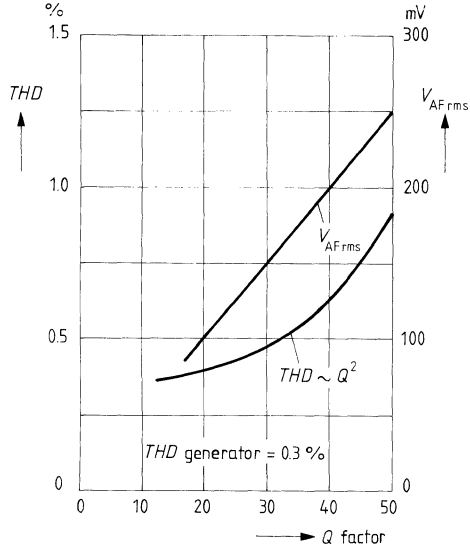
Input voltage for limiting versus supply voltage
f_i = 10.7 MHz; Δf = ± 50 kHz;
f_{mod} = 1 kHz; Q approx. 35



AM suppression versus supply voltage
f_i = 10.7 MHz; Δf = ± 50 kHz;
V_i = 10 mV, f_{mod} = 1 kHz, m = 30%



AF output voltage and total harmonic distortion versus Q-factor
V_S = 12 V, f_i = 10.7 MHz,
Δf = ±50 kHz, f_{mod} = 1 kHz



Bipolar circuit

AM receiver circuit for LW, MW, and SW in battery and mains operated radio receivers. It includes an RF prestage with AGC, a balanced mixer, separated oscillator and an IF amplifier with AGC. Because of its internal stabilization, all characteristics are nearly independent of the supply voltage. For use in high quality radio sets the TDA 1046 should be preferred to the TCA 440.

- Separately controllable prestage
- Multiplicative push-pull mixer with separate oscillator
- High large signal capability from 4.5 V supply voltage on
- 100 dB feedback control range in 5 stages
- Direct connection for tuning meter
- Minimum external components

Type	Ordering code	Package outline
TCA 440	Q67000-A669	DIP 16
TCA 440 I	Q67000-A669-S2	
TCA 440 II	Q67000-A669-S3	

Maximum ratings

Supply voltage	V_S	15	V
Thermal resistance (system-air)	$R_{th\ SA}$	120	K/W
Storage temperature range	T_{stg}	−40 to 125	°C
Junction temperature	T_j	150	°C

Range of operation

Supply voltage range	V_S	4.5 to 15	V
Ambient temperature range	T_{amb}	−15 to 80	°C

Characteristics (V_S = 9 V; T_{amb} = 25 °C; f_{iRF} = 600 kHz; f_{mod} = 1 kHz)

Total current consumption at	V_S = 4.5 V	I_S	7	mA
	V_S = 9 V	I_S	10.5	mA
	V_S = 15 V	I_S	12	mA
RF level deviation for	ΔV_{AF} = 6 dB	ΔG_{RF}	65	dB
(m = 80%)	ΔV_{AF} = 10 dB	ΔG_{RF}	80	dB
AF output voltage for V_{iRF} (symm. measured at 1—2)				
for m = 80%	$V_{i\,RF}$ = 20 µV	$V_{AF\,rms}$	140	mV
	$V_{i\,RF}$ = 1 mV	$V_{AF\,rms}$	260	mV
	$V_{i\,RF}$ = 500 mV	$V_{AF\,rms}$	350	mV
for m = 30%	$V_{i\,RF}$ = 20 µV	$V_{AF\,rms}$	50	mV
	$V_{i\,RF}$ = 1 mV	$V_{AF\,rms}$	100	mV
	$V_{i\,RF}$ = 500 mV	$V_{AF\,rms}$	130	mV
Input sensitivity (measured at 60 Ω, $f_{i\,RF}$ = 1 MHz, m = 30%/0%, R_G = 540 Ω)				
at signal-to-noise ratio (in acc. with DIN 45405)	$\frac{S+N}{N}$ = 6 dB	$V_{i\,RF}$	1	µV
	$\frac{S+N}{N}$ = 26 dB	$V_{i\,RF}$	7	µV
	$\frac{S+N}{N}$ = 58 dB	$V_{i\,RF}$	1	mV

RF stage

Input frequency range	$f_{i\,RF}$	0 to 50	MHz
Output frequency $f_{i\,F} = f_{osc} - f_{i\,RF}$	f_{IF}	460	kHz
Control range	ΔG_V	38	dB
Input voltage (for 600 kHz, m = 80%) for overdrive (THD_{AF} = 10%), symmetrically measured at: pins 1 and 2	$V_{i\,RF\,pp}$	2.6	V_{pp}
(mean carrier value)	$V_{i\,RF\,rms}$	0.5	V
IF suppression between 1—2 and 15	a_{IF}	20	dB
RF input impedance			
a) unsymmetrical coupling			
at $G_{RF\,max}$	Z_i	2/5	kΩ/pF
at $G_{RF\,min}$	Z_i	2.2/1.5	kΩ/pF
b) symmetrical coupling			
at $G_{RF\,max}$	Z_i	4.5	kΩ/pF
at $G_{RF\,min}$	Z_i	4.5/1.5	kΩ/pF
Mixer output impedance (pins 15 or 16)	Z_q	250/4.5	kΩ/pF

IF stage

Input frequency range	$f_{i\,IF}$	0 to 2	MHz
Control range at 460 kHz	ΔG_V	62	dB
Input voltage (mean carrier value) at G_{min} for overdrive (THD_{AF} = 10%), measured at pin 12 (60 Ω to ground, $f_{i\,IF}$ = 460 kHz, m = 80%; f_{mod} = 1 kHz)	$V_{IF\,rms}$	200	mV
AF output voltage for $V_{i\,IF}$ at 60 Ω (pin 12)			
V_{IF} = 30 µV, m = 80%; f_{mod} = 1 kHz	$V_{AF\,rms}$	50	mV
V_{IF} = 3 mV, m = 80%; f_{mod} = 1 kHz	$V_{AF\,rms}$	200	mV
V_{IF} = 3 mV, m = 30%; f_{mod} = 1 kHz	$V_{AF\,rms}$	70	mV
IF input impedance (unsymm. coupling)	Z_i	3/3	kΩ/pF
IF output impedance	$Z_{q\,7}$	200/8	kΩ/pF

Tuning meter

Recommended instruments: 500 µA (R_i = 800 kΩ)
or 300 µA (R_i = 1.5 kΩ)

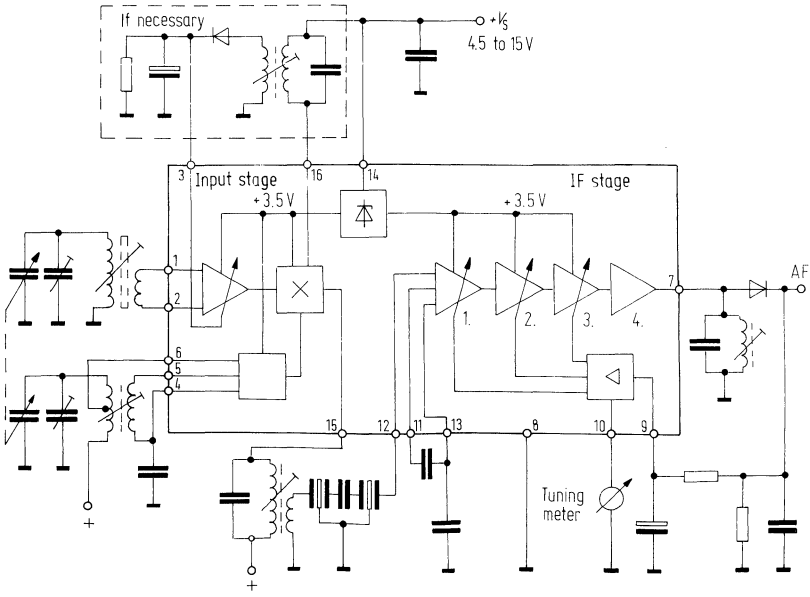
The IC offers a tuning meter voltage of 600 mV_{EMF} max. with a source impedance of approx. 400 Ω.

Selection:

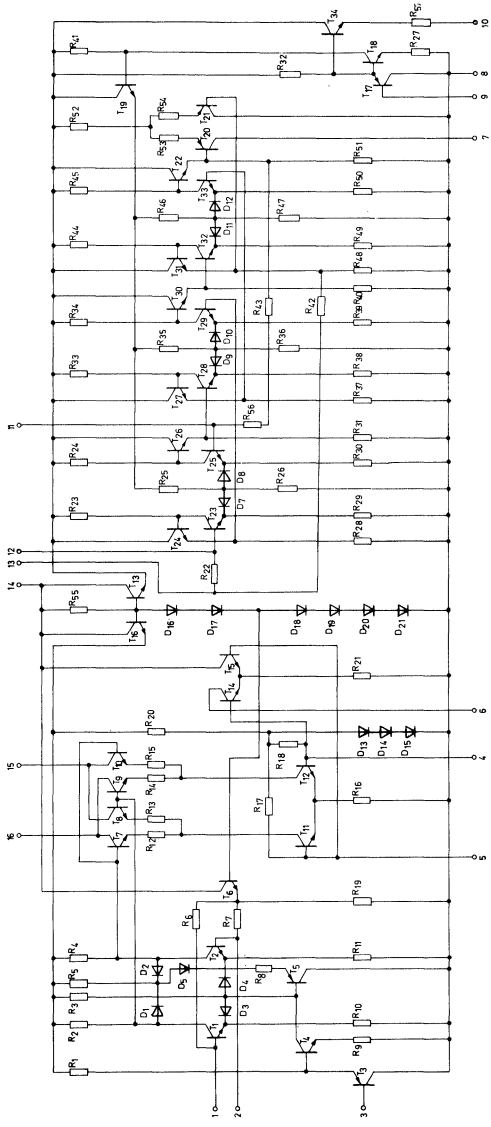
TCA 440 is selected in 2 groups as concerns the output voltage V_7:

Parameter: V_S = 8 V; $V_{i\,IF}$ approx. 4.5 mV_{rms}; m = 30%; f_{IF} = 455 kHz; $f_{q\,AF}$ = 1 kHz
TCA 440 I: V_7 = 40 to 80 mV_{rms}
TCA 440 II: V_7 = 55 to 100 mV_{rms}
TCA 440: V_7 = 40 to 100 mV_{rms}
The number of the group is stamped on the IC.

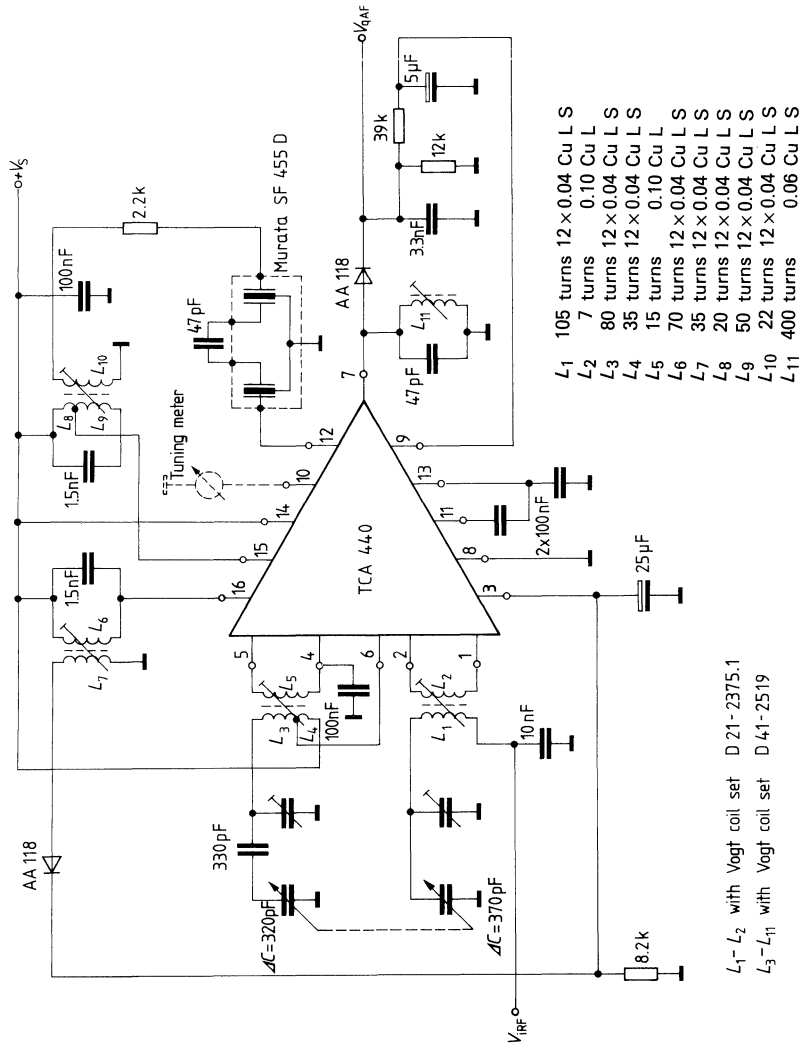
Block diagram



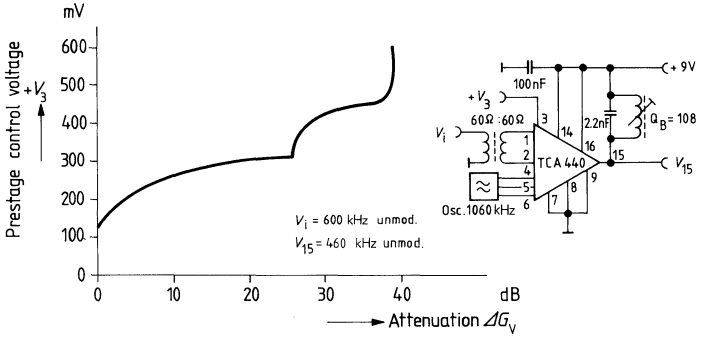
Circuit diagram



Application example for MW with TCA 440

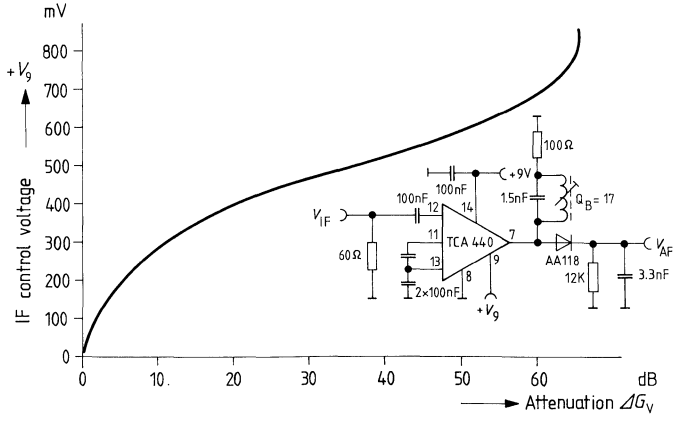


Prestage control TCA 440



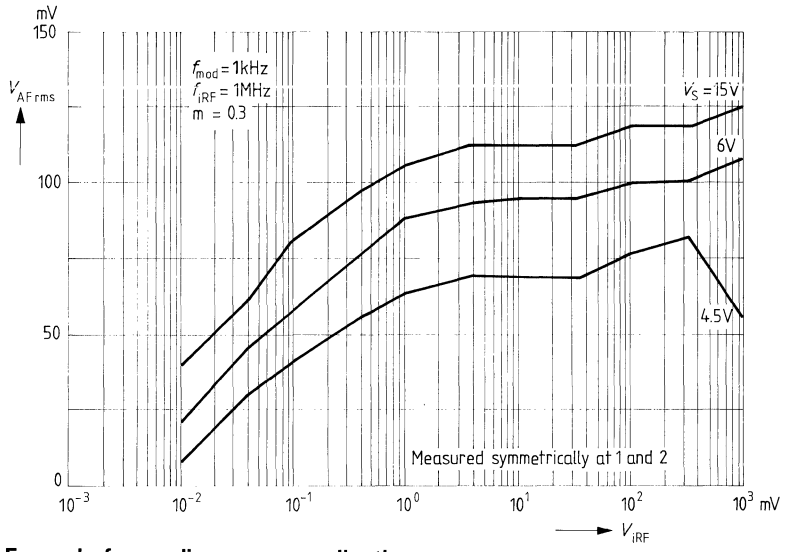
The input is not power matched and can be driven with a higher resistance. V_i is chosen such that a constant V_{15} is obtained (50 mV_{pp}).

IF control



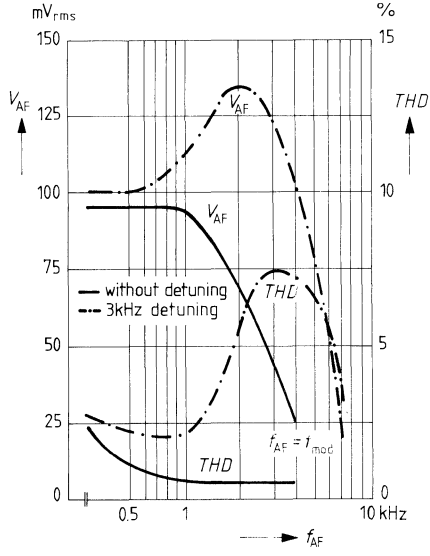
V_{IF} (469 kHz; $m = 80\%$; $f_{mod} = 1$ kHz) is chosen such that always a constant V_{AF} is obtained (200 mV_{rms}).

AF output voltage versus RF input voltage

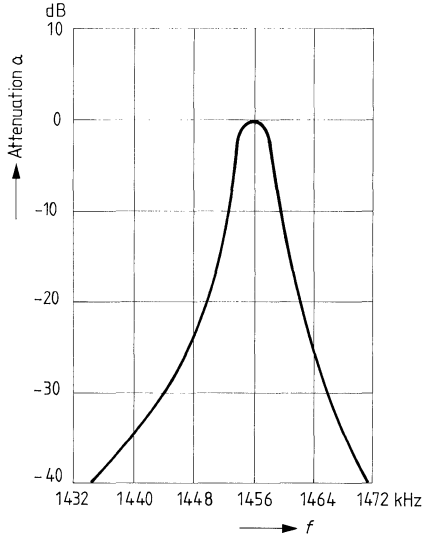


Example for medium wave applications

AF output voltage versus output frequency
Total harmonic distortion versus modulation frequency

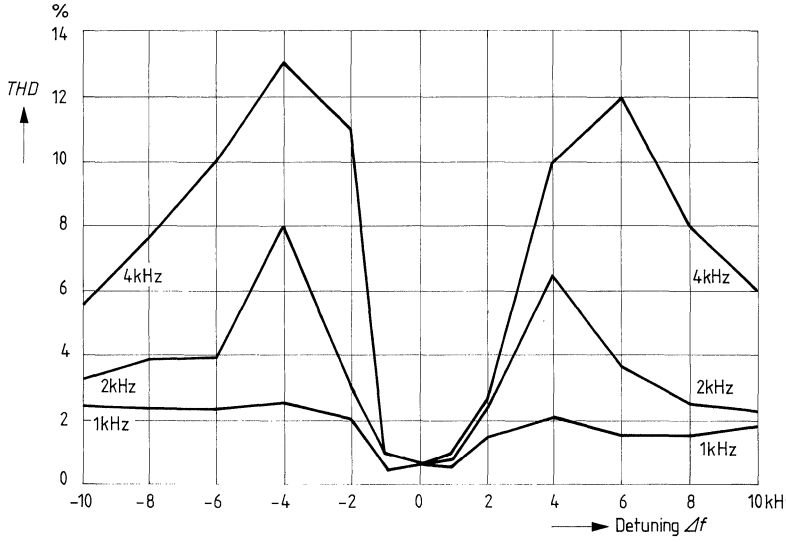


Passband characteristic versus input frequency, measured from input to output of the circuit

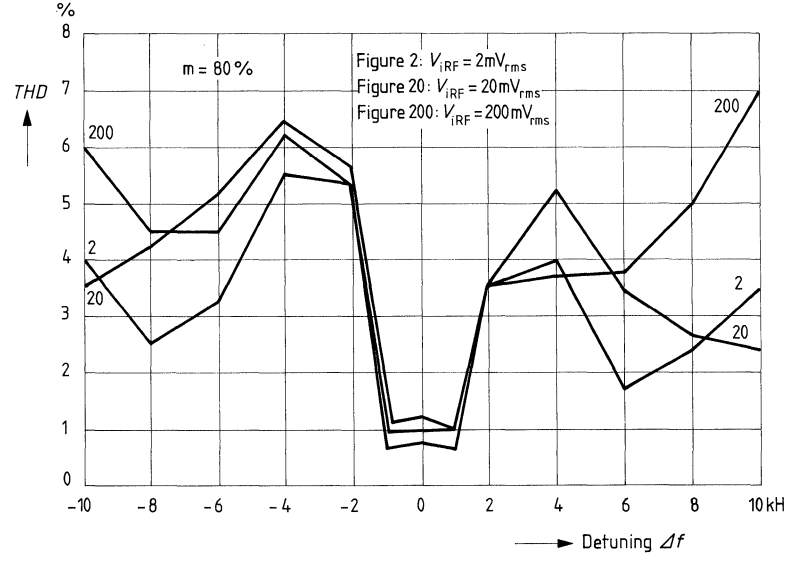


Total harmonic distortion versus detuning (parameter: modulation frequency)

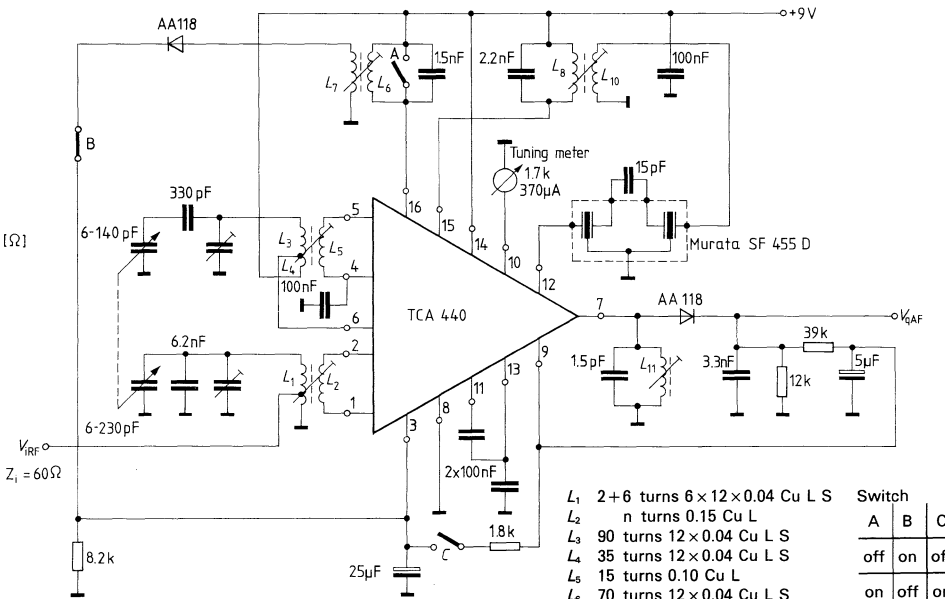
$V_S = 9\,V$ $f_{osc} = 1.455\,MHz \pm \Delta f$ $m = 30\%$
$f_{i\,RF} = 1\,MHz$ $f_{IF} = 455\,kHz$ $V_{i\,RF} = 20\,mV_{rms}$



Total harmonic distortion versus detuning (parameter: RF input voltage)



Test circuit for noise figure



n[turns]	$R_{Generator}$ [Ω]
1	15
2	60
4	240
6	540
9	1.2k
12	2.2k
18	4.8k

L_1 – L_2 M 25 pot core
L_3 – L_{11} with Vogt coil set D41-2519

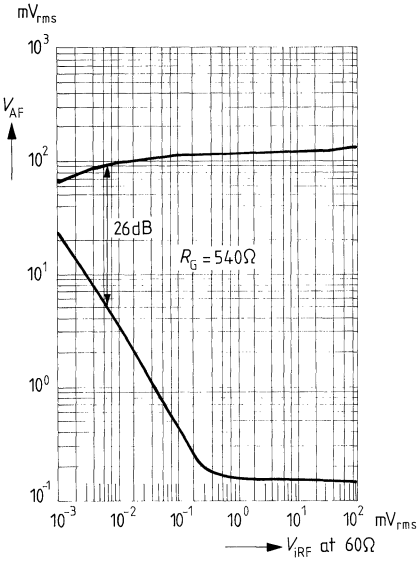
L_1	2+6 turns 6×12×0.04 Cu L S
L_2	n turns 0.15 Cu L
L_3	90 turns 12×0.04 Cu L S
L_4	35 turns 12×0.04 Cu L S
L_5	15 turns 0.10 Cu L
L_6	70 turns 12×0.04 Cu L S
L_7	35 turns 12×0.04 Cu L S
L_8	60 turns 12×0.04 Cu L S
L_{10}	22 turns 12×0.04 Cu L S
L_{11}	68 turns 0.06 Cu L

Switch

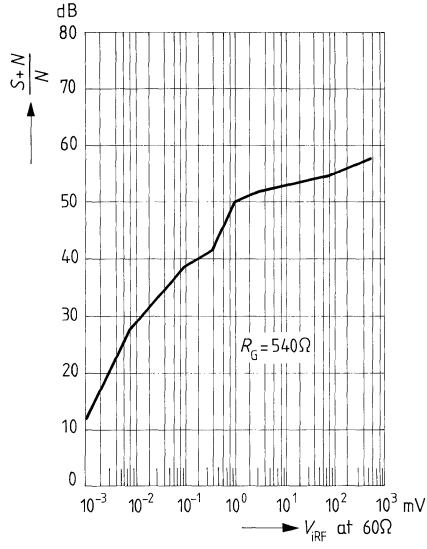
A	B	C		
off	on	off	separate prestage control	(1)
on	off	on	prestage control voltage derived from IF control voltage	(2)

f_i = 1 MHz; m = 30%

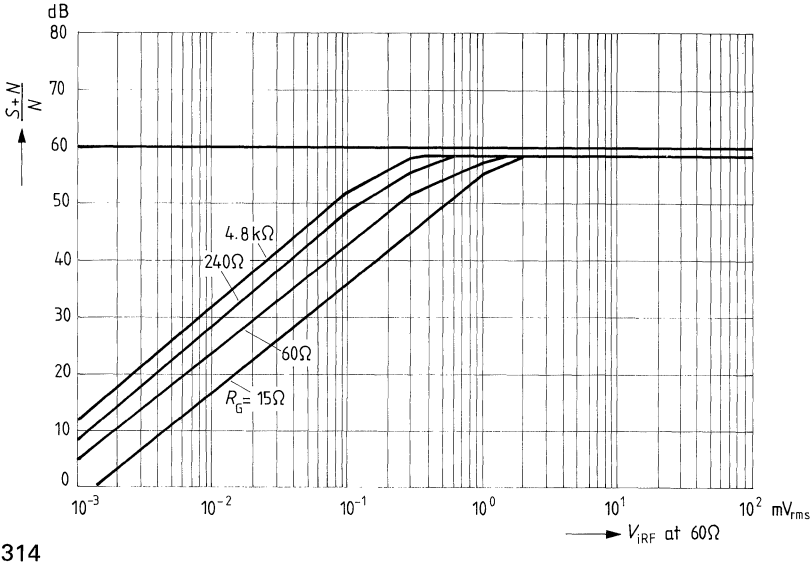
AF output voltage and noise figure versus RF input voltage
switching position (1)



Signal to noise ratio versus RF input voltage
switching position (2)

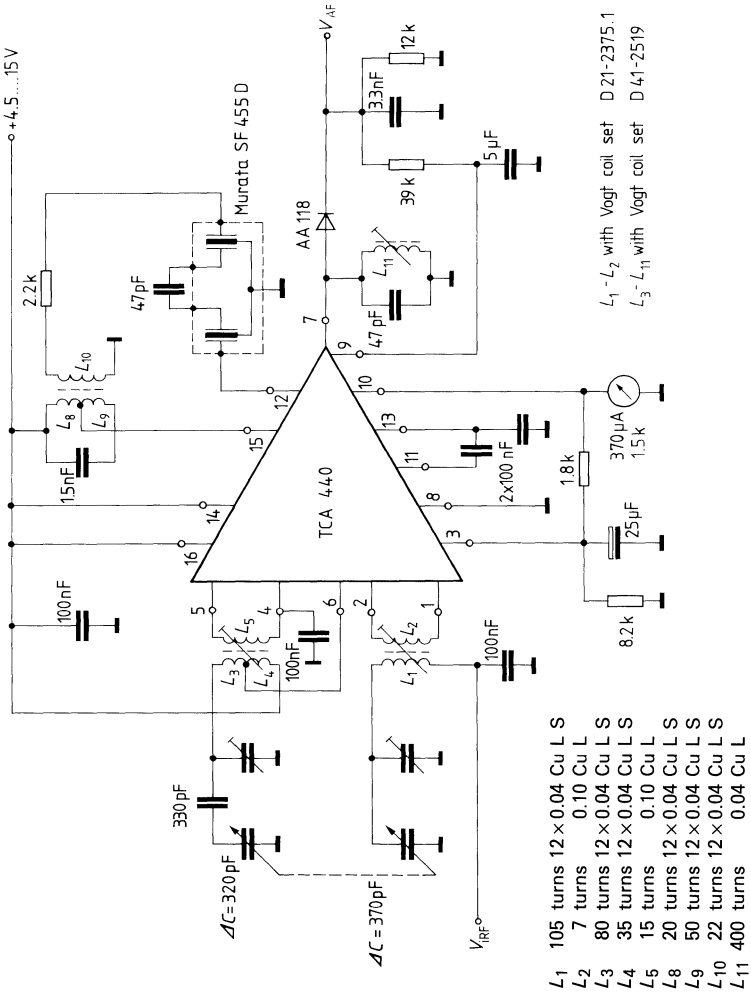


Signal to noise ratio versus RF input voltage
(parameter is generator impedance)
(switching position 1)



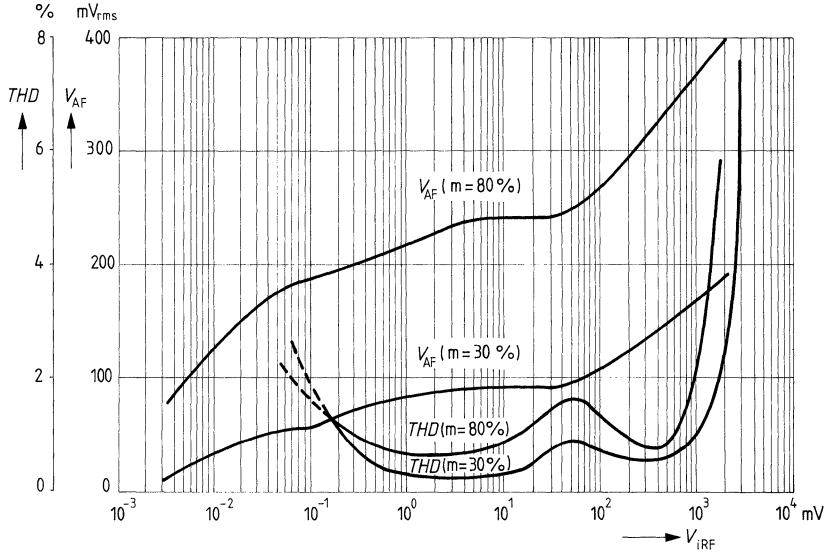
Application example for MW

Prestage control is derived from IF control

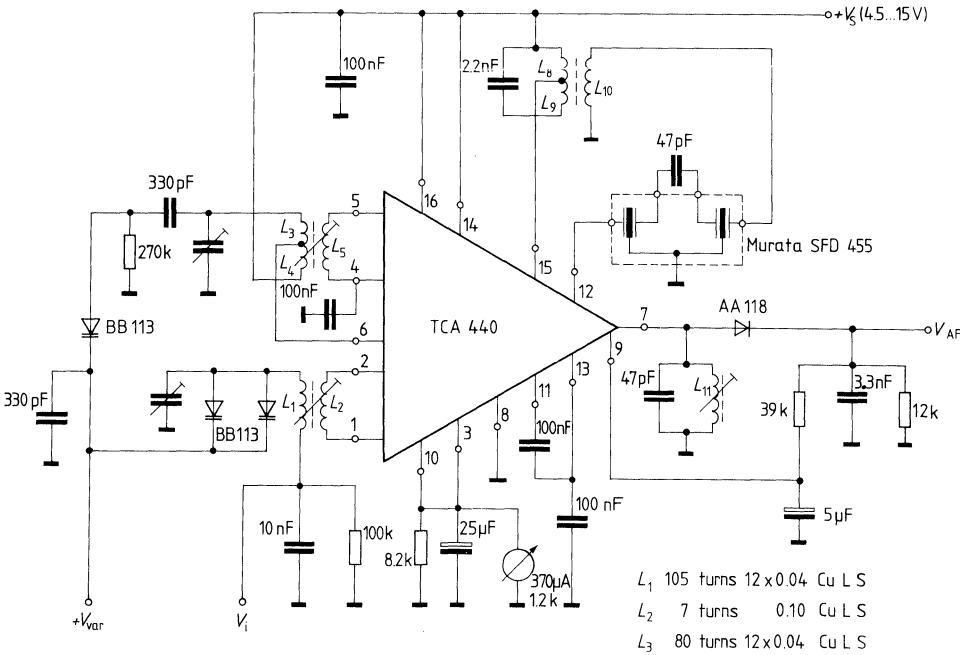


L_1 105 turns 12 × 0.04 Cu L S
L_2 7 turns 0.10 Cu L
L_3 80 turns 12 × 0.04 Cu L S
L_4 35 turns 12 × 0.04 Cu L S
L_5 15 turns 0.10 Cu L
L_8 20 turns 12 × 0.04 Cu L S
L_9 50 turns 12 × 0.04 Cu L S
L_{10} 22 turns 12 × 0.04 Cu L S
L_{11} 400 turns 0.04 Cu L

Test figures for application example for MW
Total harmonic distortion and AF output voltage
versus RF input voltage
measured symmetrically at pins 1 and 2
f_i = 1 MHz, f_{mod} = 1 kHz, f_{IF} = 455 kHz, V_S = 9 V



Application example for MW using BB 113 varicap diodes

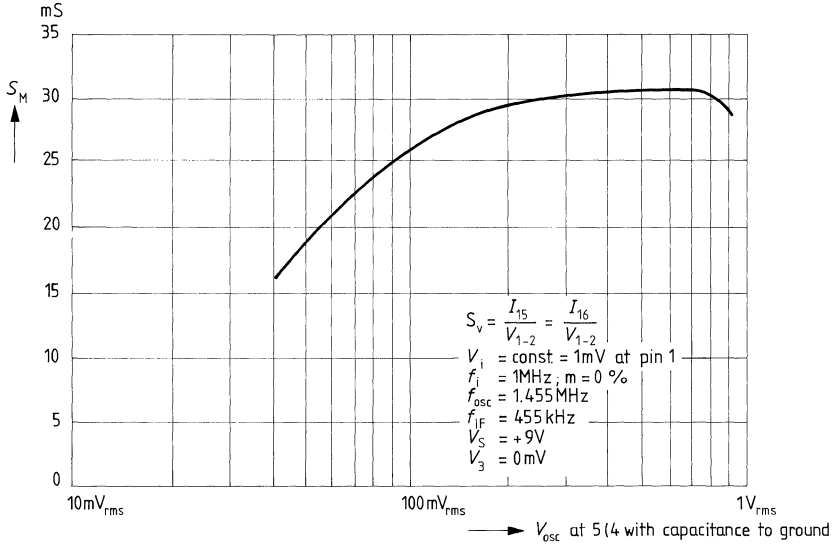


L_1 - L_2 with Vogt coil set D 21-2375 1
L_3 - L_{11} with Vogt coil set D 41-2519

V_D = 8,5 V ⟶ f_t = 800 kHz
V_D = 30 V ⟶ f_t = 1620 kHz

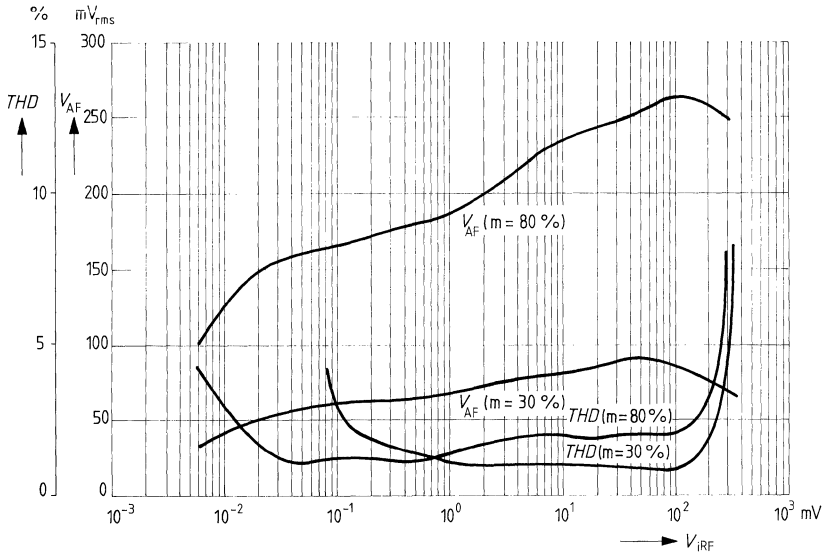
L_1	105	turns	12 x 0.04	Cu L S
L_2	7	turns	0.10	Cu L S
L_3	80	turns	12 x 0.04	Cu L S
L_4	35	turns	12 x 0.04	Cu L S
L_5	15	turns	0.10	Cu L S
L_8	20	turns	12 x 0.04	Cu L S
L_9	50	turns	12 x 0.04	Cu L S
L_{10}	22	turns	12 x 0.04	Cu L S
L_{11}	400	turns	0.06	Cu L

Conversion transconductance versus oscillator voltage

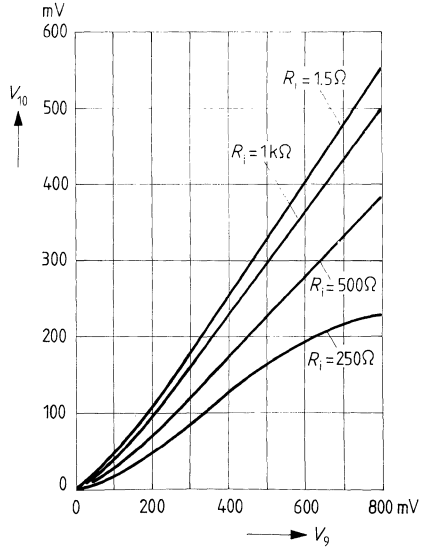


Measured values for application example for MW using BB 113

AF output voltage and total harmonic distortion versus RF input voltage
f_i = 1 MHz; f_{mod} = 1 kHz; f_{IF} = 455 kHz
V_S = 9 V; $V_{i\,RF}$ symetrically measured at pins 1 and 2



Tuning meter voltage versus IF control voltage (parameter: impedance of tuning meter)



Example for moving coil instruments

R_i	Full-scale deflection
1.5 kΩ	100 µA
1.5 kΩ	170 µA
2 kΩ	200 µA
350 Ω	500 µA

Bipolar circuit

AM receiver circuit for LW, MW, and SW in car radios and mains operated radio receivers. TDA 1046 includes controlled RF pre- and intermediate stages, a multiplicative push-pull mixer with separate oscillator, controlled IF amplifier, full-wave demodulator, active low pass, as well as an amplifier to directly feed a field-strength indicator instrument. By means of its amplitude-controlled oscillator, the TDA 1046 is particularly suited for applications with varicap diodes. The circuit is balanced.

- Provision of internal AGC voltage
- High large signal capability
- Internal demodulator
- Internal AF filtering
- Direct feed of a logarithmical field strength indicator (range 90 dB)
- High AF output voltage with low distortion factor
- Minimization of external components
- Provisions for additional RF circuitry

Type	Ordering code	Package outline
TDA 1046	Q67000-A1092	DIP 16

Maximum ratings

Supply voltage	V_S	18	V
Thermal resistance (system-air)	$R_{th\ SA}$	90	K/W
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C

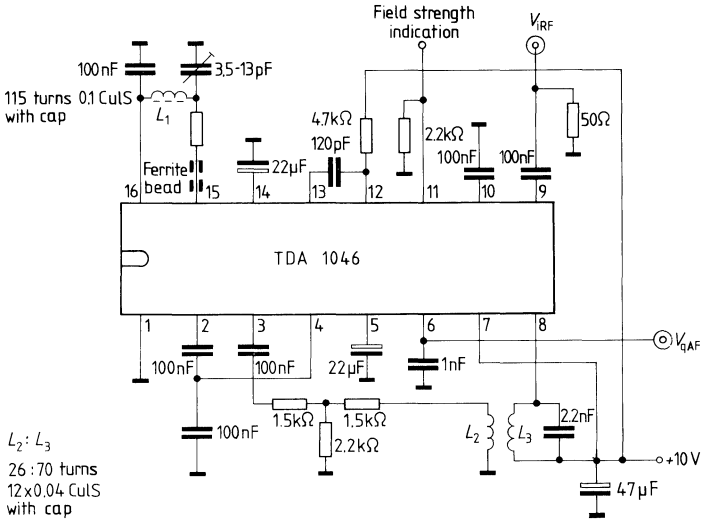
Range of operation

Supply voltage range	V_S	8 to 18	V
Oscillator frequency range	f_{osc}	0.5 to 31	MHz
Input frequency range RF unit	$f_{i\ RF}$	0 to 30	MHz
IF unit	$f_{i\ IF}$	0.2 to 1	MHz
Ambient temperature range	T_{amb}	−15 to 85	°C

Characteristics (V_7 = 10 V, T_{amb} = 25 °C, f_{mod} = 1 kHz, $f_{i\,RF}$ = 1000 kHz) see test circuit

		min	typ	max	
Current consumption	I_S	15	20	25	mA
AF output voltage and total harmonic distortion factor					
m = 80%; $V_{i\,RF}$ = 1 mV_{rms}	V_{AF}	600	800	1000	mV_{rms}
	THD		0.8	1	%
m = 80%; $V_{i\,RF}$ = 25 mV_{rms}	V_{AF}	600	800	1000	mV_{rms}
	THD		1.5	2	%
m = 30%; $V_{i\,RF}$ = 1 mV_{rms}	V_{AF}	200	300	400	mV_{rms}
	THD			0.6	%
m = 30%; $V_{i\,RF}$ = 45 mV_{rms}	V_{AF}	200	300	400	mV_{rms}
	THD			0.9	%
Total range of AGC (variation of AF voltage $\Delta V_6 \leqq$ 6 dB)	ΔG	85			dB
Input voltage for AGC triggering					
with tuned LC circuit	$V_{i\,9-10}$		19		µV
with wide-band circuit	$V_{i\,9-10}$		28		µV
Signal to noise ratio (measured at 50 Ω, m = 30%/0%)					
at $V_{i\,RF}$ = 2.5 µV	$\frac{S+N}{N}$		6		dB
= 14 µV	$\frac{S+N}{N}$		26		dB
= 1 mV	$\frac{S+N}{N}$		53		dB
Instrument current (V_S = 15 V; at G_{min}; $V_{11} \leqq V_7 - 3$ V)	I_{11}	1		1.5	mA
AF output resistance	R_{q6}	2.25	3	3.75	kΩ
Noise voltage in accordance with DIN 45405	V_n		500	700	μV_{os}

Test circuit



Additional characteristics RF stage

(V_S = 10 V, T_{amb} = 25 °C; $f_{i\,RF}$ = 1000 kHz, f_{mod} = 1 kHz, m = 95%, f_{IF} = 450 kHz)

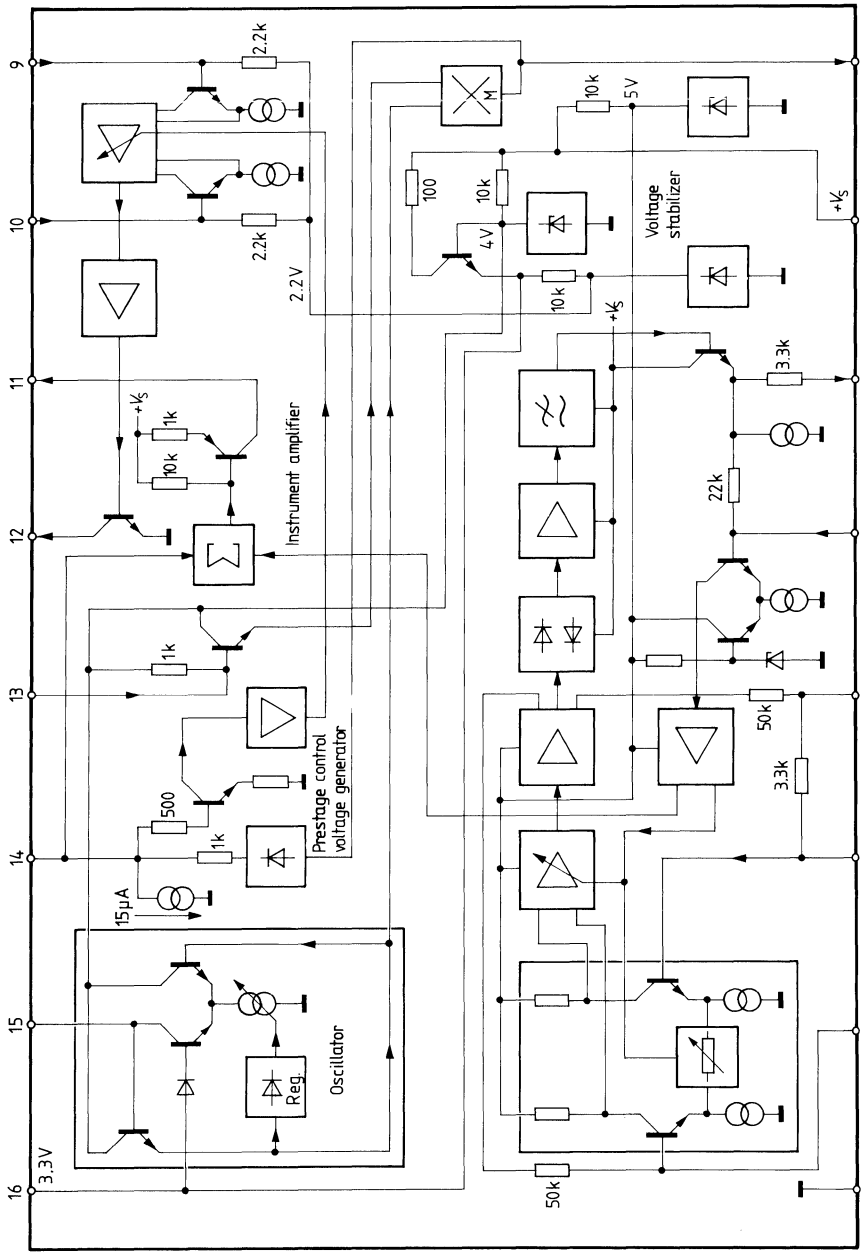
		min	typ	max	
Oscillator voltage (f_{osc} = 1.45 MHz)	V_{15}			350	mV_{rms}
AGC range of RF prestage	ΔG	40			dB
Voltage gain	$G_{V/8\text{-}9/10}$		40		dB
Voltage gain of RF stage	$G_{V\,13\text{-}9/10}$		20		dB
Input impedance	$Z_{i\,9\text{-}1} = Z_{i\,10\text{-}1}$		2/5		kΩ/pF
	$Z_{i\,9\text{-}10}$		4/5		kΩ/pF
Input voltage for overload (THD_{mod} = 10%)	$V_{i\,9\text{-}10}$		2		V_{pp}
Reference voltage ($I_{16} \leqq$ 3 mA)	V_{16}	3	3.3	3.8	V

Additional characteristics IF stage

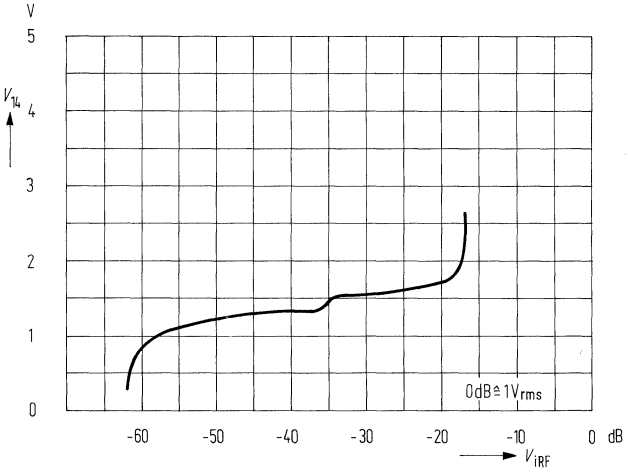
(V_S= 10 V, T_{amb} = 25 °C, f_{IF} = 450 kHz, f_{mod} = 1 kHz, m = 95%)

AGC range at 450 kHz	ΔG	45			dB
Input voltage for overload (THD = 10%)	V_3		120		mV_{rms}
Output impedance	$Z_{q\,8}$		100		kΩ
Input impedance	$Z_{i\,3}$		3.3/3		kΩ/pF
AF output voltage ($V_{3\,rms}$ = 10 mV; m = 30%)	V_{AF}	245			mV_{rms}

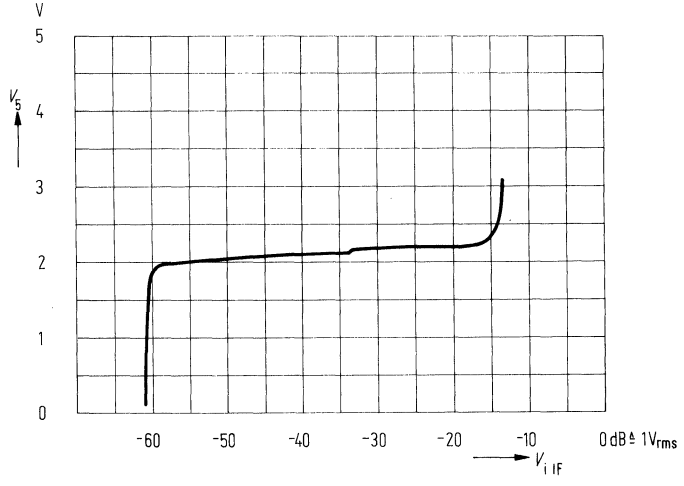
Block diagram



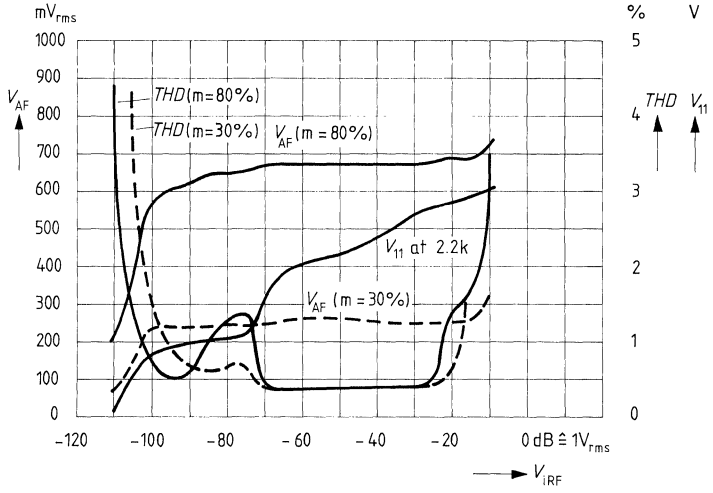
Prestage control
V_S = 10 V; T_{amb} = 25 ° C; $f_{i\,RF}$ = 1000 kHz; f_{mod} = 1 kHz, m = 80%; V_{IF} = V_q = const.



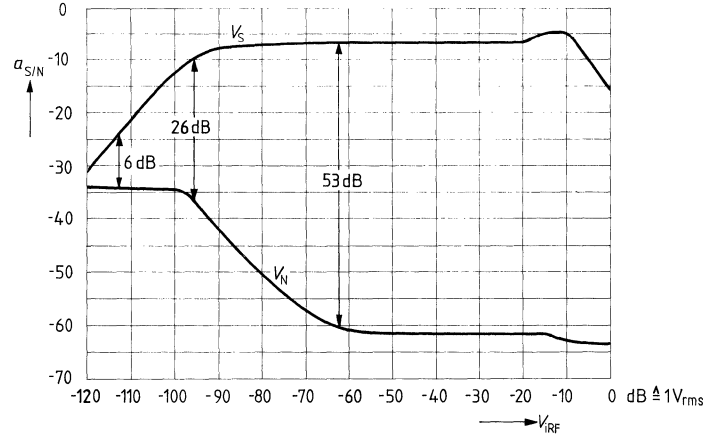
IF stage control
V_S = 10 V; T_{amb} = 25 °C; $f_{i\,IF}$ = 455 kHz; f_{mod} = 1 kHz; m = 80%; V_{AF} = V_6 = const.



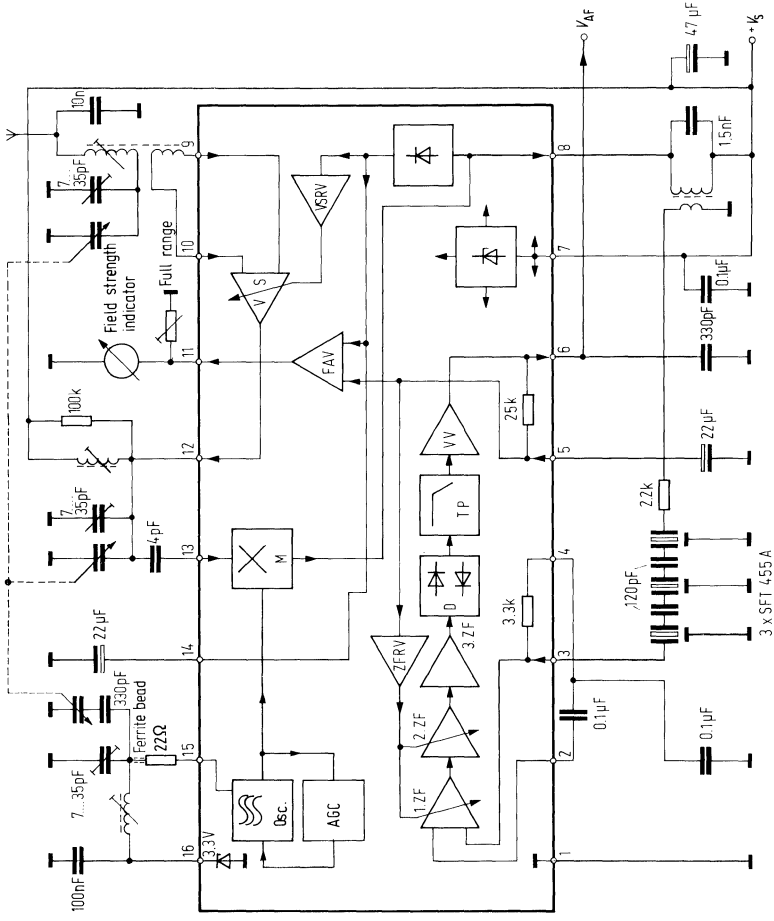
AF output voltage, total harmonic distortion, instrument voltage versus RF input voltage
V_S = 15 V, $f_{i\,RF}$ = 1000 kHz, f_{mod} = 1 kHz Coupling with wide-band circuit

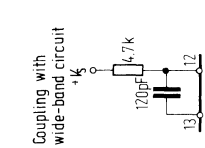


Signal-to-noise ratio versus input voltage
V_S = 15 V; m = 30%; $f_{i\,RF}$ = 1000 kHz; f_{mod} = 1 kHz



Application circuit





Osc. oscillator
M mixer
VS RF prestage
VSRV prestage AGC amplifier
FAV field strength indicator
ZF IF amplifier
ZFRV IF AGC amplifier
D demodulator
TP active low pass
VV preamplifier

Coil data

1. RF prestage		
primary	105 turns	15 × 0.04 CuLS
sec. (pin 9—10)	7 turns	15 × 0.04 CuLS
wound on Vogt D 21-2375.1		
2. RF intermediate circuit		
	105 turns	15 × 0.04 CuLS
wound on Vogt D 21-2375.1		
3. Oscillator circuit		
	115 turns	0.10 CuLS
wound on Vogt D 41-2519 with cap		
4. IF circuit (pin 8)		
primary (LC circuit)	70 turns	12 × 0.04 CuLS
secondary	26 turns	12 × 0.04 CuLS
wound on Vogt D 41-2519 with cap		

Variable capacitor

HOPT triple rotary capacitor set MG 06-05 A

FM IF Amplifier with Demodulator for Radio Receivers

TDA 1047

Bipolar circuit

FM-IF amplifier for radio sets with 8-stage amplifier and symmetrical coincidence demodulator. The TDA 1047 additionally offers provisions for the feeding of an amplitude indicator, either positive or negative going mono-stereo voltage, AFT output (push-pull-current output) with automatic switch-off, is squelch adjustable throughout an input signal range of more than 40 dB and depends on detuning.

- Excellent limiting qualities
- Excellent frequency stability of demodulator characteristic
- Large range of operating voltage between 4 and 18 V
- Low current consumption
- Externally adjustable squelch
- Few peripheric components

Type	Ordering code	Package outline
TDA 1047	Q67000-A1091	DIP 18

Maximum ratings

Supply voltage	V_S	18	V
Thermal resistance (system-air)	$R_{th\ SA}$	90	K/W
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C

Range of operation

Supply voltage range	V_S	4 to 18	V
Frequency range	f	0 to 15	MHz
Ambient temperature range	T_{amb}	−25 to 85	°C

Characteristics (V_S = 12 V; T_{amb} = 25 °C; f_i = 10.7 MHz; f_{mod} = 1 kHz; Δf = ±75 kHz; Q_B approx. 20) see test circuit

		min	typ	max	
Current consumption (I_{14} = 0)	I_{12}	9	12	15	mA
Voltage for field strength indicator (R_{14} = 3.3 kΩ)					
V_i = 160 mV_{rms}	V_{14}	1.6	2		V
V_i = 16 μV_{rms}	V_{14}		10	20	mV
Current	I_{14}			3.6	mA
Voltage for squelch adjustment (approx. log.)					
V_i = 8 mV_{rms}	V_{15}		0		V
V_i = 16 μV_{rms}	V_{15}	2.2	2.5		V
Current	I_{15}			3.6	mA
AF output DC voltage	V_7		2.1		V
AF output voltage (V_i = 10 mV; THD = 0.4%)	V_7	270	300		mV_{rms}
Internal DC voltage of output emitter follower	I_7	180	200		µA
Total harmonic distortion (V_i = 10 mV) [1]	THD		0.4	0.8	%
Input voltage for limiting [2]	V_i		30	50	µV
Input resistance	$R_{i\,18}$	10			kΩ
AF output resistance [3] (emitter follower output)	$R_{q\,7}$		0.3	1	kΩ
Threshold of detuning-depending squelch (referred to f = 10.7 MHz)	Δf		±100	±150	kHz
Switching threshold for AFT off	V_2			20	mV_{os}
Input resistance	$R_{i\,2}$	40	100		kΩ
Voltage for AFT off	V_3	0.8			V
Current deviation of the AFT output	Δ_5		±150		µA
IF output voltage for limiting	$V_{8\text{-}11}$		500		mV_{pp}
Input resistance for demodulator circuit	$R_{9\text{-}10}$		5.4		kΩ
Recommended voltage for demodulator circuit [4]	$V_{9\text{-}10}$		500		mV_{pp}
Threshold for AF off	V_{13}		0.85	0.95	V
AF on	V_{13}	0.5	0.6		V
Hysteresis for switching threshold	ΔV_{13}		120	200	mV
Internal resistance for AF switch-off time constant	$R_{q\,6}$		500		Ω
AM suppression (V_i = 10 mV; m = 30%)	a_{AM}	60			dB
Signal-to-noise-ratio (V_i = 10 mV)	$a_{S/N}$	70			dB
AF suppression at muting circuit (V_i = 10 mV)	a_{AF}		60		dB

[1]) In the case of using a band filter: THD_{max} = 0.3%

[2]) Limiting application for V_{AF} = −3 dB

[3]) The output resistance R_{q7} can be reduced by connecting a resistor of at least 2.7 kΩ between pin 7 and ground.

[4]) The recommended voltage at the demodulator circuit $V_{9\text{-}10}$ can be adjusted by the capacitors $C_{8\text{-}9}$ and $C_{10\text{-}11}$, which are also influencing the voltage V_{14} and V_{15}.

If the slider of potentiometer P is grounded, the field-strength-dependent squelch is switched off.

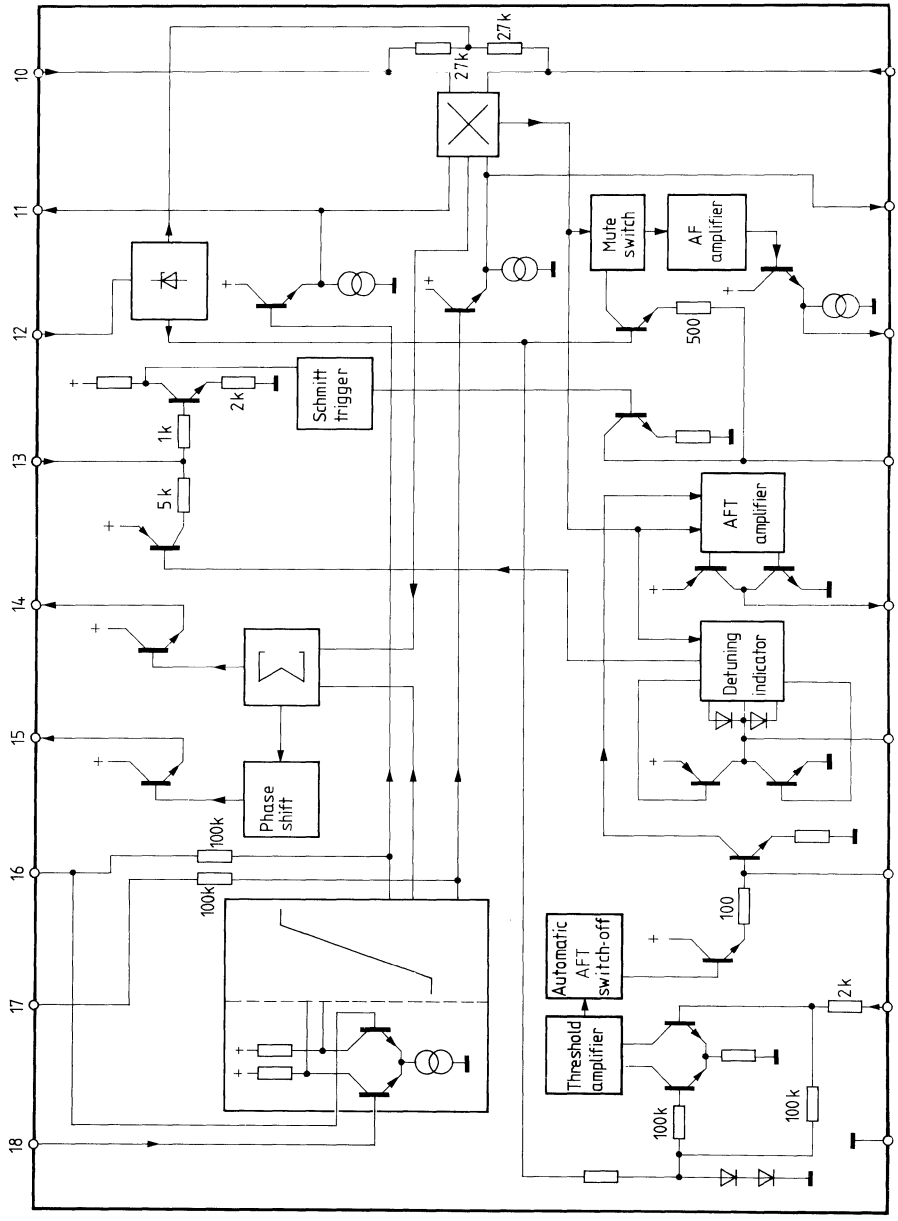
If pin 13 is grounded, both the field-strength- and the detuning-dependent squelch are switched off.

The noise level between the transmitters becomes more or less audible, when pin 6 is loaded with a resistance to +12 V in case of "squelch on". Noise attenuation increases with the size of the resistance ($R \geqq 10\,k\Omega$).

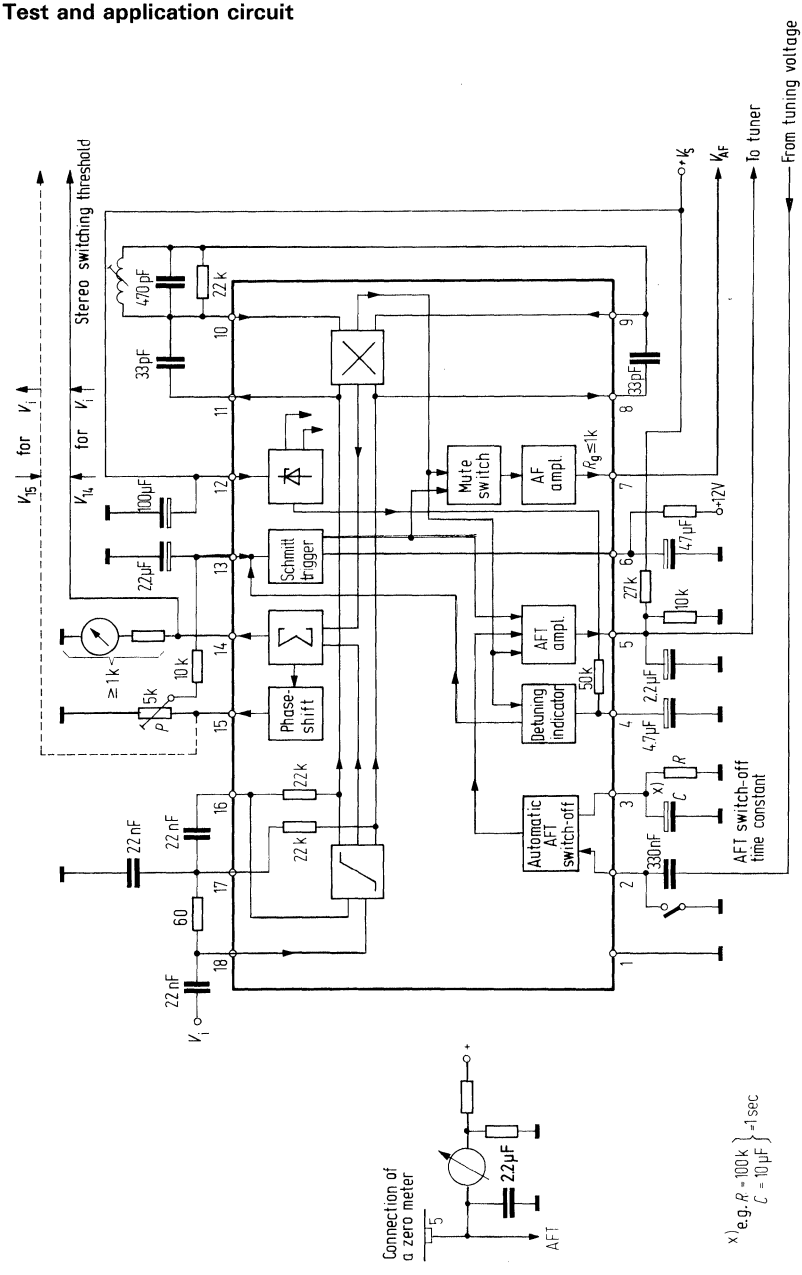
Pin designation

Pin No.	Description
1	Ground
2	Sensor input for AFT switch off
3	AFT switch off time constant
4	Low-pass capacitor for detuning-dependent AF switch off
5	AFT output (push-pull output)
6	Low-pass capacitor for suppression of switch off clicks in case of detuning and insufficient field strength
7	AF output (emitter follower with constant-current source)
8	Output of limiter amplifier
9, 10	Phase shifting circuit
11	Output of limiter amplifier
12	Positive operating voltage
13	Input for amplitude-dependent switch off
14	Instrument connection and stereo switching voltage (positive going)
15	Squelch and stereo switching voltage (negative going)
16, 17	Feedbacks for IF amplifier
18	IF input

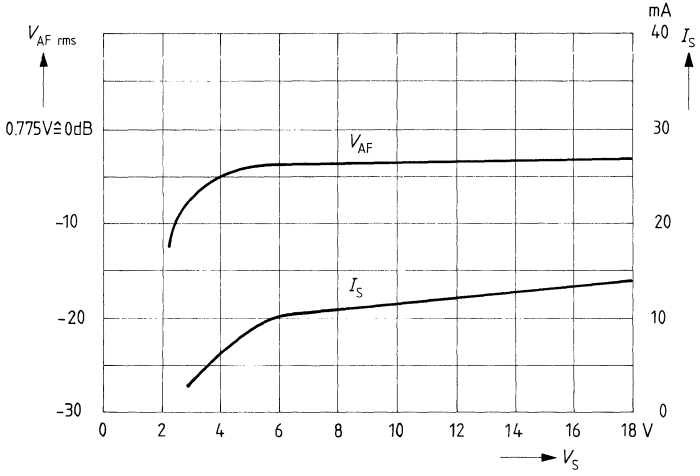
Block diagram



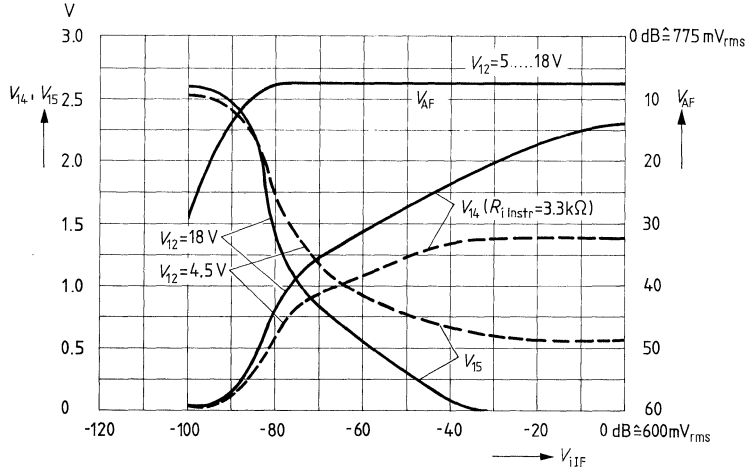
Test and application circuit



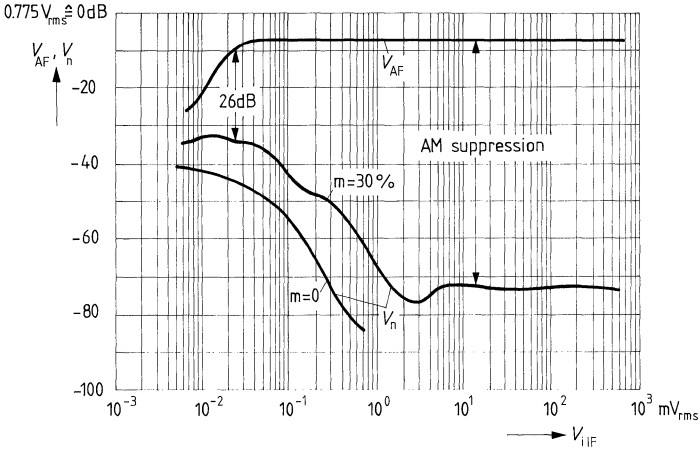
AF output voltage, total current consumption versus supply voltage
$V_{i\,IF}$ = 60 mV_{rms} wide band, pin 13 to ground, $V_{9\text{-}10}$ = 500 mV_{pp}



AF output voltage, indicator voltage, squelch voltage versus input voltage
V_{12} = 15 V; f = 10.7 MHz, Δf = ±75 kHz, f_{mod} = 1 kHz
$V_{9\text{-}10}$ = 500 mV_{pp}, wide band measured by 100 nF, THD = 0.4%



AF output voltage, noise voltage versus input voltage
f = 10.7 MHz, Δf = ±75 kHz, V_{12} = 15 V



AM Short-Wave Tuner IC for Superheterodyne Receivers

S 054 T

Bipolar circuit

The S 054 T is an AM short-wave tuner IC comprising an adjustable prestage at 45 dB gain and internal control voltage generation. Moreover, the S 054 T includes a mixer with a separate, amplitude-controlled oscillator. The oscillator drive signal to the counter is available subsequently to an emitter-follower. The input is resistant to large signals and cross modulation. The oscillator is generally designed for varicap tuning and can additionally be used with a crystal. The IC is mainly suitable for use in double and multiple superhet receivers.

- Resistance to large signals and cross modulation
- Linear mixer
- Wide control range
- Designed for varicap tuning

Type	Ordering code	Package outline
S 054 T	Q 67000-A 1472	DIP 14

Maximum ratings

Supply voltage	V_S	18	V
Junction temperature	T_j	150	°C
Thermal resistance (system-air)	$R_{th\ SA}$	90	K/W
Storage temperature range	T_{stg}	−40 to 125	°C

Range of operation

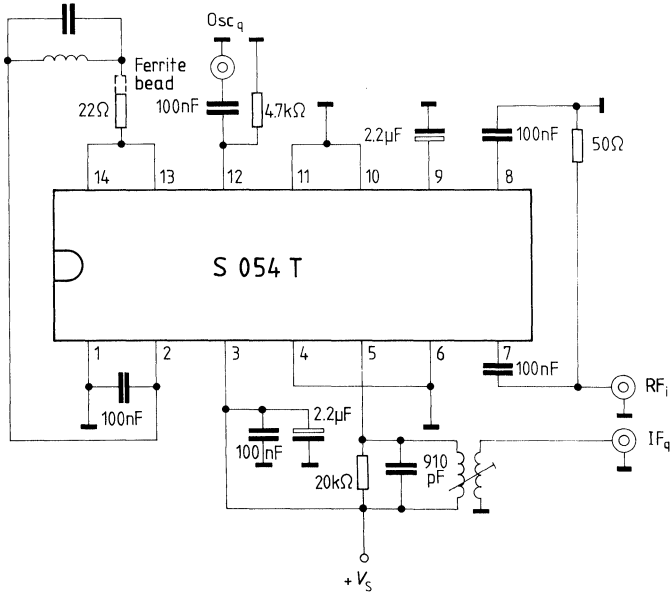
Supply voltage range	V_S	4 to 18	V
Oscillator frequency range	f_{osc}	0.1 to 32	MHz
Input frequency range	f_i	0 to 30	MHz
Output frequency range	f_q	0 to 30	MHz
Ambient temperature range	T_{amb}	−20 to 85	°C

Characteristics (see test circuit) (V_S = 10 V; f_i = 1 MHz; T_{amb} = 25 °C)

		min	typ	max	
Current consumption	I_3		13	15	mA
Output voltage (Q_B approx. 20)	V_5		500		mV_{rms}
Range of AGC	ΔG_v	40	45		dB
Input voltage causing overdrive	V_7		1.8		V_{pp}
Oscillator voltage	V_{12}	150		350	mV_{rms}
Reference voltage	V_2		3.6		V
Counter dc voltage output at $R_{12\text{-}1}$ = 4.7 kΩ	V_{12}		1.4		V
Short circuit output current ($R_{12\text{-}1}$ = 0; t = 10 s)	I_{q12}			20	mA

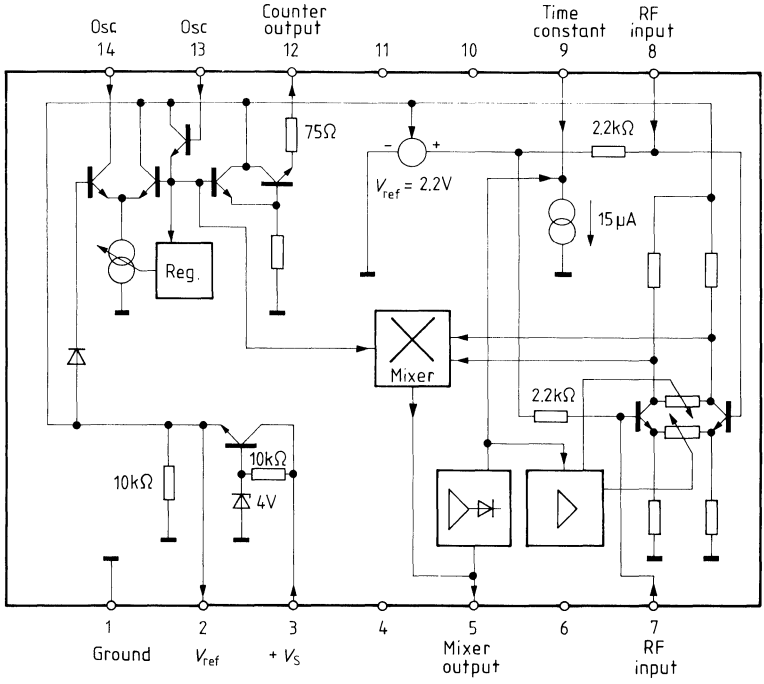
Test circuit

V_S = 10 V, f = 1 MHz
f_{osc} = 1.2 MHz, f_{IF} = 200 kHz
T_{amb} = 25 °C



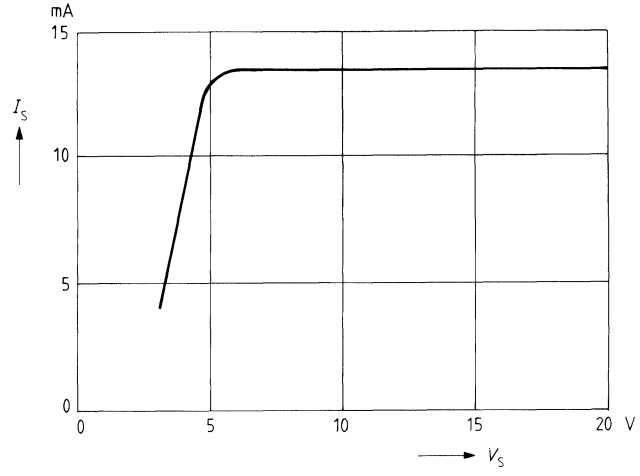
1) Pot core N28 A_L 250
$n_1 : n_2$ = 50 : 5 turns 12 × 0.04 CuLS
Q_O approx. 250, Q_B approx. 20

Block diagram

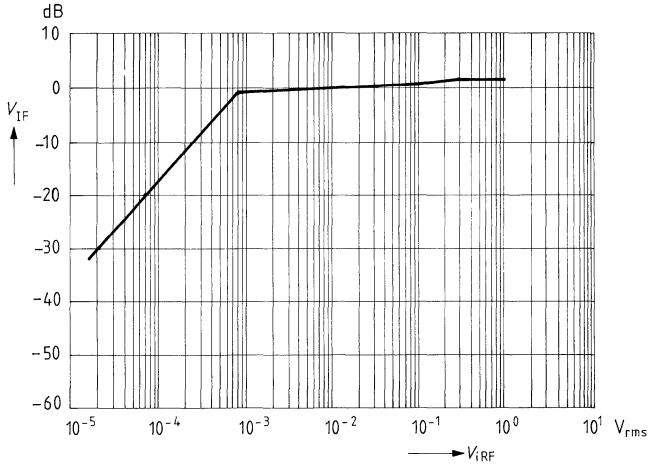


Current consumption on battery voltage

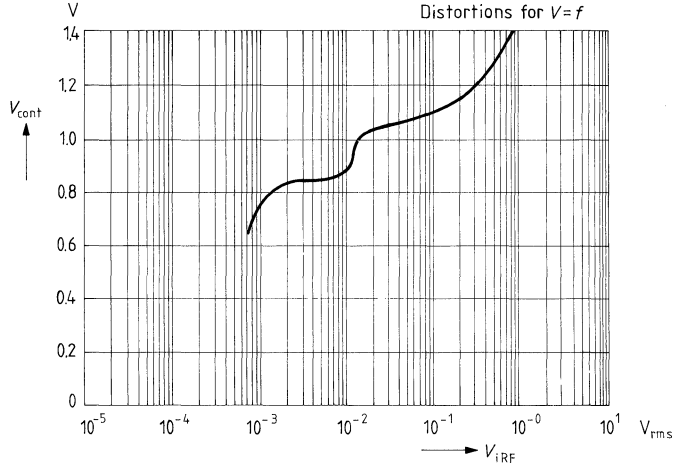
V_{ref} (10 V = V_S) = 3.7 V



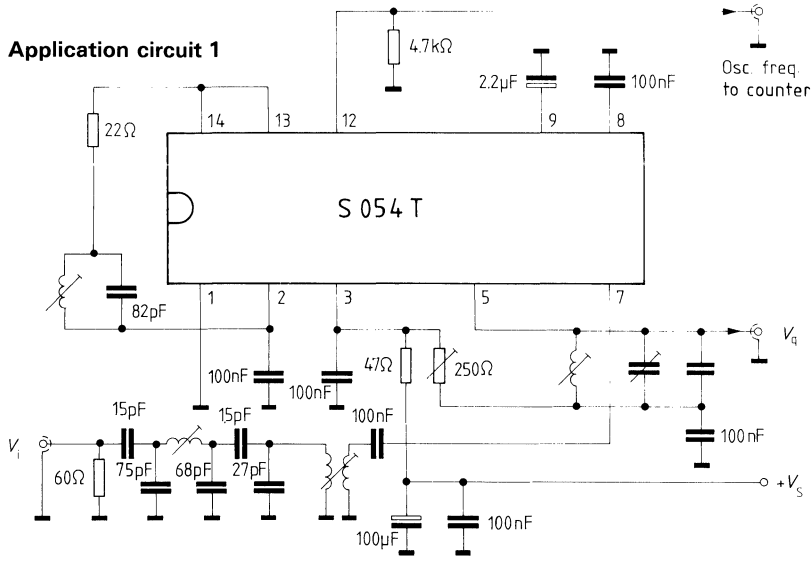
IF output on RF input signal V_S = 10 V; 0 dB ≙ 225 mV_{rms}



Control characteristic curve V_S = 10 V; V_{IF} = 225 mV_{rms}

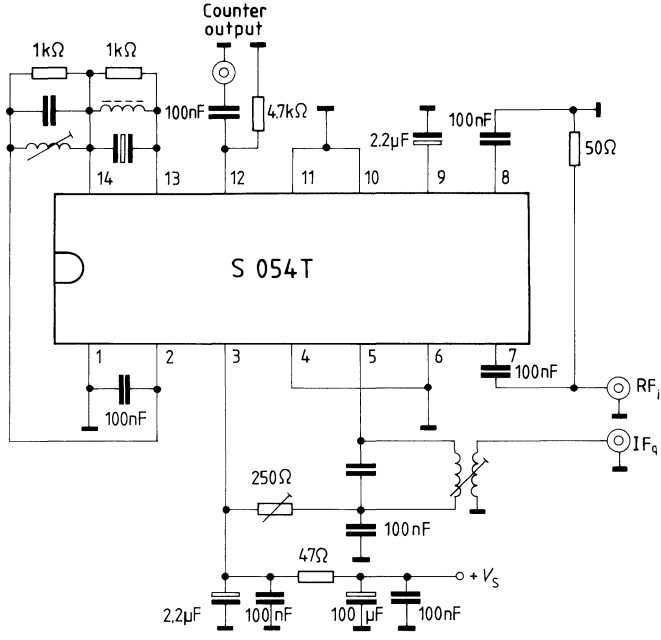


Application circuit 1



Application circuit 2

Crystal-controlled oscillator (series resonance)



Bipolar circuit

The TDA 4200 is an FM IF IC with demodulator, particularly developed for use in car radios. It includes the facility to set the input amplification for automatic search tuning. Moreover, a search tuning stop pulse can be obtained.

- 8-stage limiter amplifier
- Product demodulator
- AFC output
- Field strength-dependent volume control

Type	Ordering code	Package outline
TDA 4200	Q 67000-A1469	DIP 18

Maximum ratings

Supply voltage	V_S	18	V
Thermal resistance (system-air)	$R_{th\ SA}$	70	K/W
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C

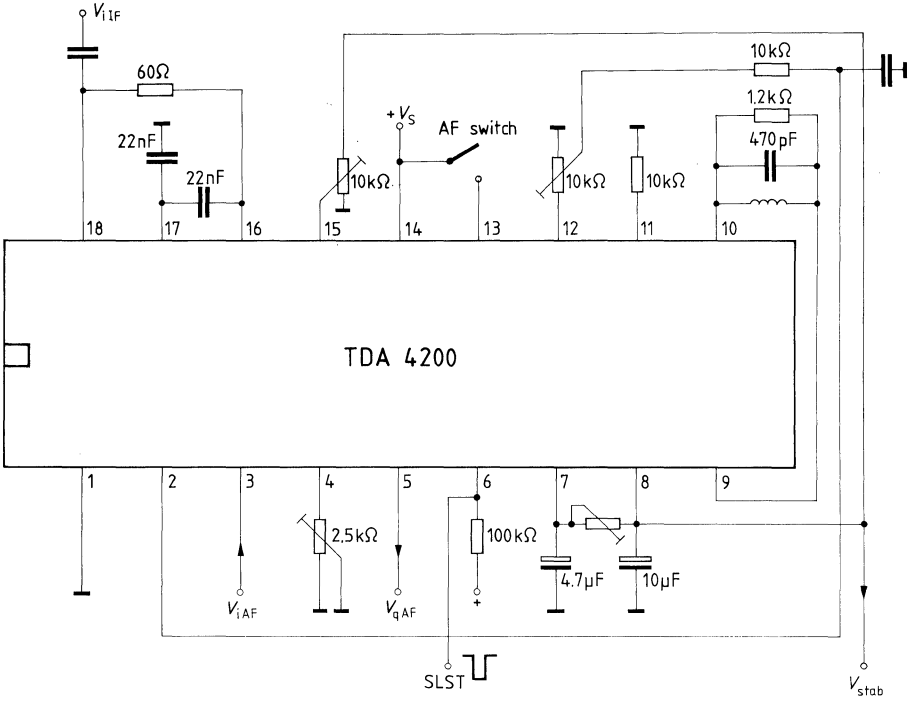
Range of operation

Supply voltage range	V_S	7.5 to 15	V
Frequency range	f	0 to 15	MHz
Ambient temperature range	T_{amb}	−25 to 85	°C

Characteristics (V_S = 8.5 V; $V_{i\,rms}$ = 10 mV; f_i = 10.7 MHz; Δf = ±75 kHz; f_{mod} = 1 kHz; Q_B approx. 25; T_{amb} = 25 °C)

		min	typ	max	
Current consumption	I_{14}	15	20	26	mA
Voltage at field strength output					
$V_{i\,rms}$ = 50 mV	V_{12}	3	3.8		V
$V_{i\,rms}$ = 0	V_{12}		0		V
Current out of field strength output	I_{12}			5	mA
Voltage at the inverse field strength output					
$V_{i\,rms}$ = 5 mV	V_{11}			0.9	V
$V_{i\,rms}$ = 0	V_{11}	3	3.8		V
Current out of inverse field strength output	I_{11}			5	mA
AF output dc voltage	$V_{q\,5}$	2.8	3.8	4.8	V
AF output voltage	$V_{q\,5\,rms}$	270	300		mV
Internal dc current of output emitter follower	I_5	0.75	1		mA
Total harmonic distortion at FM IF operation (V_{13} = ∞)	*THD*		0.5	1	%
Input voltage for limiting action ($V_{q\,5}$ −3 dB)	$V_{i\,IF\,rms}$		30	60	µV
Input resistance for demodulator circuit	R_{9-10}		30		kΩ
AM suppression (m = 30%)	a_{AM}	60			dB
Signal-to-noise ratio	$a_{S/N}$	70			dB
Current deviation of the AFC output	I_7	100	150	250	µA
Output current	I_6			0.5	mA
Stabilized voltage	V_8	3.6	4.1	4.6	V
Adjustment range of the limiting (adjusted by pin 15)	a_i		40		dB
AF mute $V_{2/1}$ = 0; $R_{4/1}$ = ∞	a_{AF}	3	7	11	dB
$V_{2/1}$ = 0; $R_{4/1}$ = 0	a_{AF}	31	40	47	dB
Voltage for AF mute OUT	$V_{2/1}$	0.75			V
Input resistance	$R_{i\,3}$		100		kΩ
AF output voltage for $V_{i\,3\,rms}$ = 200 mV	$V_{q\,5\,rms}$	200	270	330	mV

Test circuit

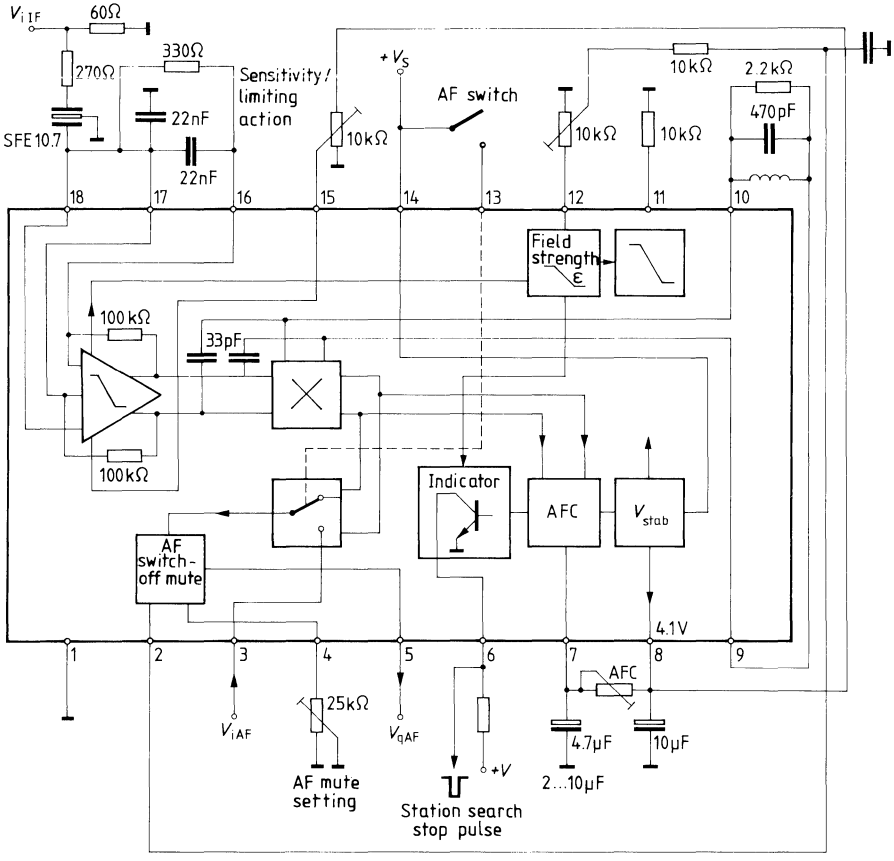


Circuit description

This IC includes an 8-stage limiter amplifier with demodulator and an uncontrolled AF output. The limiting action can be varied by 40 dB with the help of external components. The AF output signal can be attenuated continuously by typically 30 dB in the range close to the limiting action. Thus, the noise generation between the broadcasting stations can be avoided.

A field strength output, an inverted field-strength output, an AFC output and an open collector output (at zero crossing of the S curve, this output becomes conductive) are available. If used in combined AM FM units, it is possible to feed the AM AF signal into pin 3 of the TDA 4200 and to switch over to pin 5 by means of the mute stage.

Block diagram and application circuit



System for the Reception of Road Traffic Transmitters
(Car Driver Broadcasting Information — ARI)

S 0280
S 0281
S 551
S 552

In West Germany the so-called car driver broadcasting information (ARI) was introduced about 5 years ago.

This system is intended to provide the car driver with hints on the actual traffic situation. For this purpose a particular identification frequency was assigned to the transmitters which broadcast messages from time to time. In detail, this transmitter signal includes the following three portions:

1. Station decoding SK

Station decoding is used to locate a road traffic transmitter. For this purpose a 57 kHz pilot tone is superimposed on the normal AF signal.

2. Message decoding DK

In order to enable the car driver of becoming aware of a message even during listening to cassette music or when the loudness level has been lowered, a 125 Hz pilot tone is being transmitted during the message transmission. Thus, the message in the loudspeaker of the receiver increases to loud.

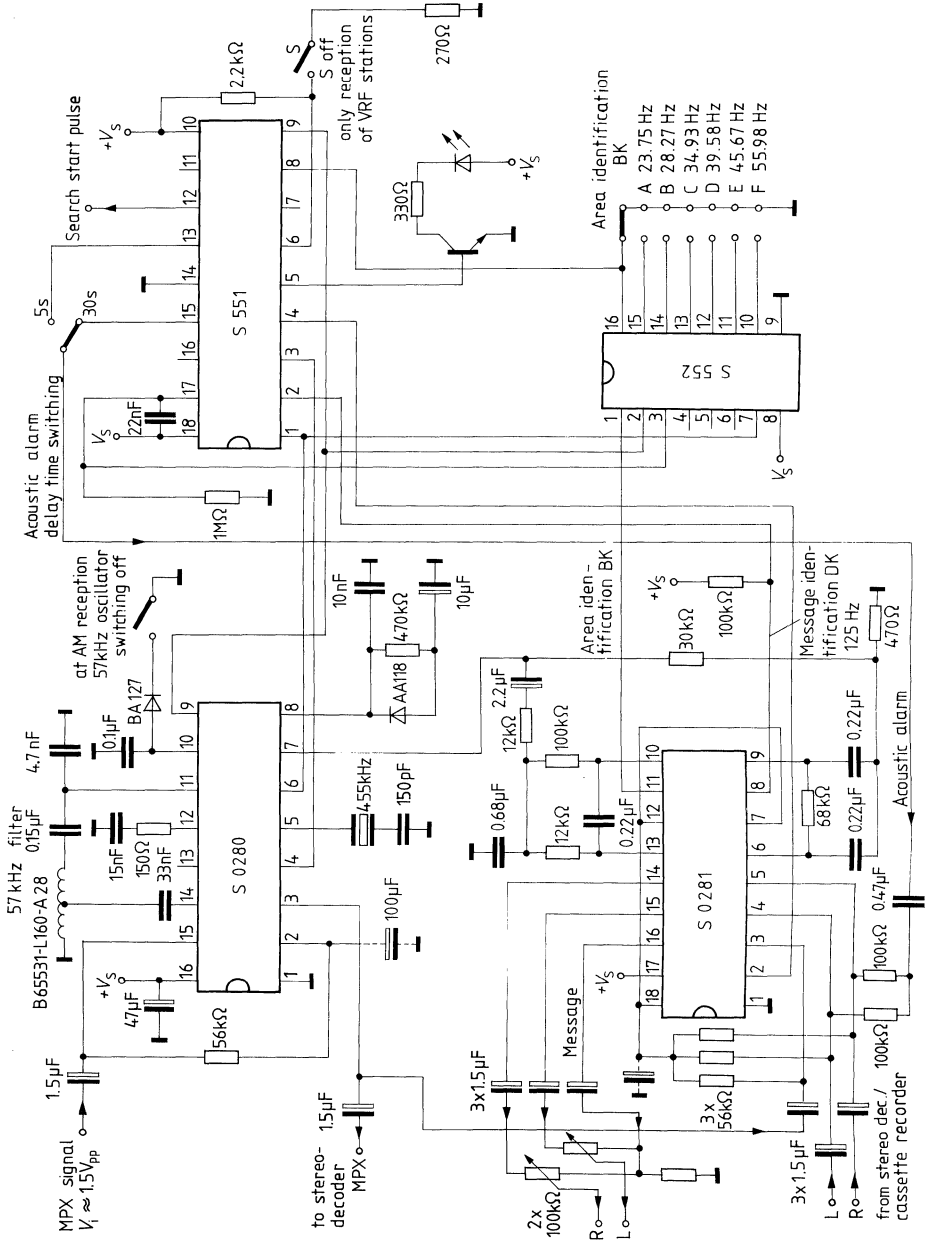
3. Area decoding BK

Since road traffic messages are transmitted regionally, the appropriate transmitter of the area referred to can be located by area decoding. For this purpose special frequencies in the range between 25 and 60 Hz are assigned to certain areas.

To decode road traffic broadcasting signals the ICs S 0280, S 0281, S 551, and S 552 are available.

Application of S 0280, S 0281, and S 551 results in a system which recognizes road traffic transmitters and transmits road traffic messages. If the system has been extended to the IC S 552, the regional frequencies of the VRF transmitters can be decoded and, thus, road traffic messages of preselected regions can be received.

Application circuit for the reception of VRF transmitters with SK + DK + BK



Bipolar circuit

The S 0280 IC includes a PLL circuit, an AM demodulator and an electronic AF switch for switching an MPX signal.

The IC delivers the station identification frequency (57 kHz) as square-wave voltage (pin 6) for subsequent operation in the S 551 and S 552 ICs and the station decoding trigger for the S 551. At pin 7 of the S 0280 the message identification frequency (125 Hz) and the area identification frequency (23.75 to 53.98 Hz) are available. After the message has been decoded in the S 551, the message AF is switched in the S 0280 to pin 5 by means of a logic control signal.

- Little adjustment
- Minimum DC voltage jump at the AF volume switch

Type	Ordering code	Package outline
S 0280	Q 67000-A1264	DIP 16

Maximum ratings

Supply voltage	V_{16}	18	V
Thermal resistance (system-air)	$R_{th\ SA}$	90	K/W
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C

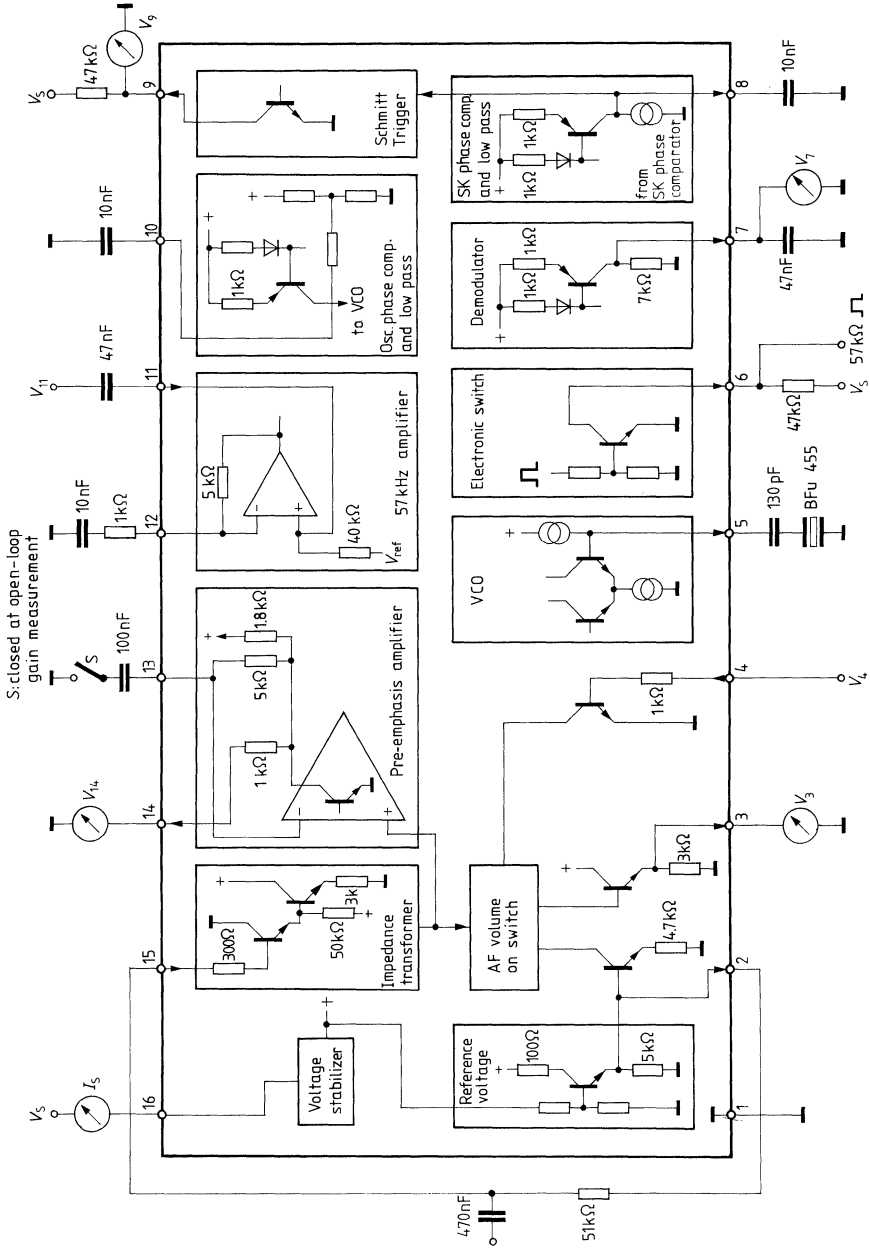
Range of operation

Supply voltage range	V_{16}	10 to 16	V
Ambient temperature range	T_{amb}	−20 to 85	°C

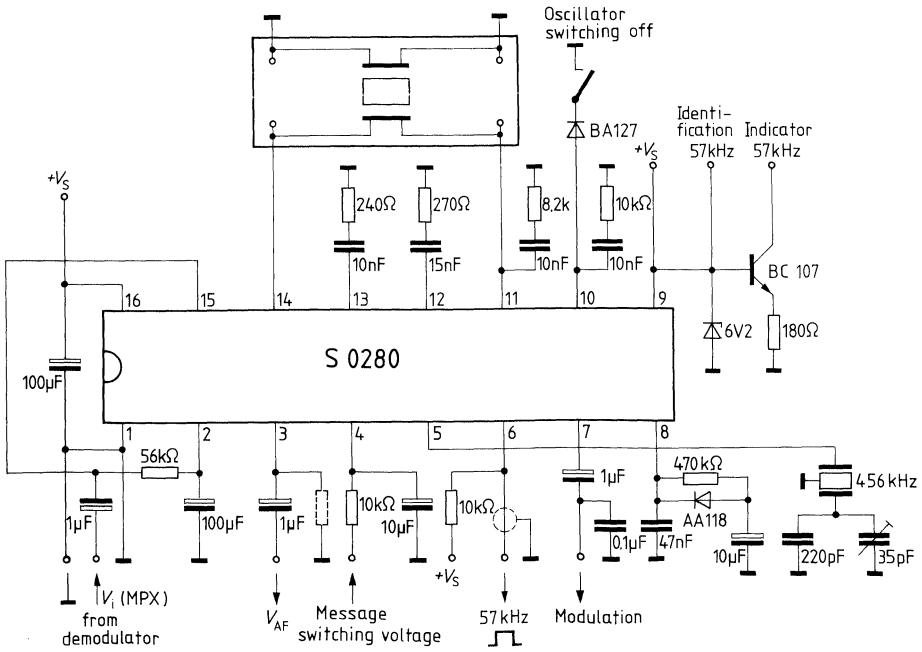
Characteristics (V_{16} = 14 V, T_{amb} = 25 °C, referred to test circuit)

		min	typ	max	
Current consumption	I_{16}		25	35	mA
Input voltage (THD = 10%)	$V_{i\,15}$			2.5	V_{pp}
Input resistance	$R_{i\,15}$	300			kΩ
Pre-emphasis amplifier					
Output resistance	$R_{q\,14}$	1.6	2	2.4	kΩ
Voltage gain (open loop)	G_{vo}	30			dB
Internal GK resistance	R_{13}		5		kΩ
57 kHz amplifier					
Voltage gain (open loop)	G_{vo}		35		dB
Internal GK resistance	R_{12}		5		kΩ
Input resistance	$R_{i\,11}$	20			kΩ
SK information					
SK switching threshold (switching at pin 9) V_{11}, f = 57 kHz	V_{SK}	6		18	mV_{rms}
BK-OK output voltage V_{11} = 50 mV_{rms}, 57 kHz +125 Hz, m = 30%	V_7	24			mV_{rms}
Load voltage SK = H	V_8	3			V
($R_{9/10}$ = 10 kΩ) SK = L	V_8			2	V
Hysteresis voltage	ΔV_8		1		V
Output current	$I_{q\,9}$			5	mA
Output current/frequency divider	$I_{q\,6}$			5	mA
Volume switch					
Bandwidth	B	60			kHz
Transmission loss	a	−1	0	+1	dB
Rejection loss	a_{rej}	50	80		dB
Output resistance	$R_{q\,3}$		380	500	Ω
Switching threshold	V_4		0.65		V
Noise voltage at pin 3 at decrease of 3 dB (f = 100 Hz −10 kHz, short-circuited input)	V_3		15		μV

Block diagram and test circuit



Application circuit



Pin designation

Pin No.	Description
1	Ground
2	Reference voltage
3	MPX output signal
4	Control voltage input for MPX signal
5	Oscillator wiring (LC, RC)
6	57 kHz output
7	57 kHz demodulator output
8	SK phase comparator, integration C
9	SK output
10	PLL phase comparator
11	57 kHz amplifier input +
12	57 kHz amplifier input −
13	Pre-emphasis amplifier input −
14	Pre-emphasis amplifier output
15	Impedance converter input
16	Supply voltage + V_S

Bipolar circuit

The S 0281 IC is used for preparing message and area decoding of VRF transmitters.

The S 0281 contains two double operational amplifiers which are used as filter and limiter amplifier. Moreover, 3 AF switches are intended for switching the message signal.

- High cross talk rejection
- High rejection loss
- Min. dc voltage change when switching the signals

Type	Ordering code	Package outline
S 0281	Q 67000-A1265	DIP 18

Maximum ratings

Supply voltage	V_{17}	18	V
Thermal resistance (system-air)	$R_{th\ SA}$	90	K/W
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C

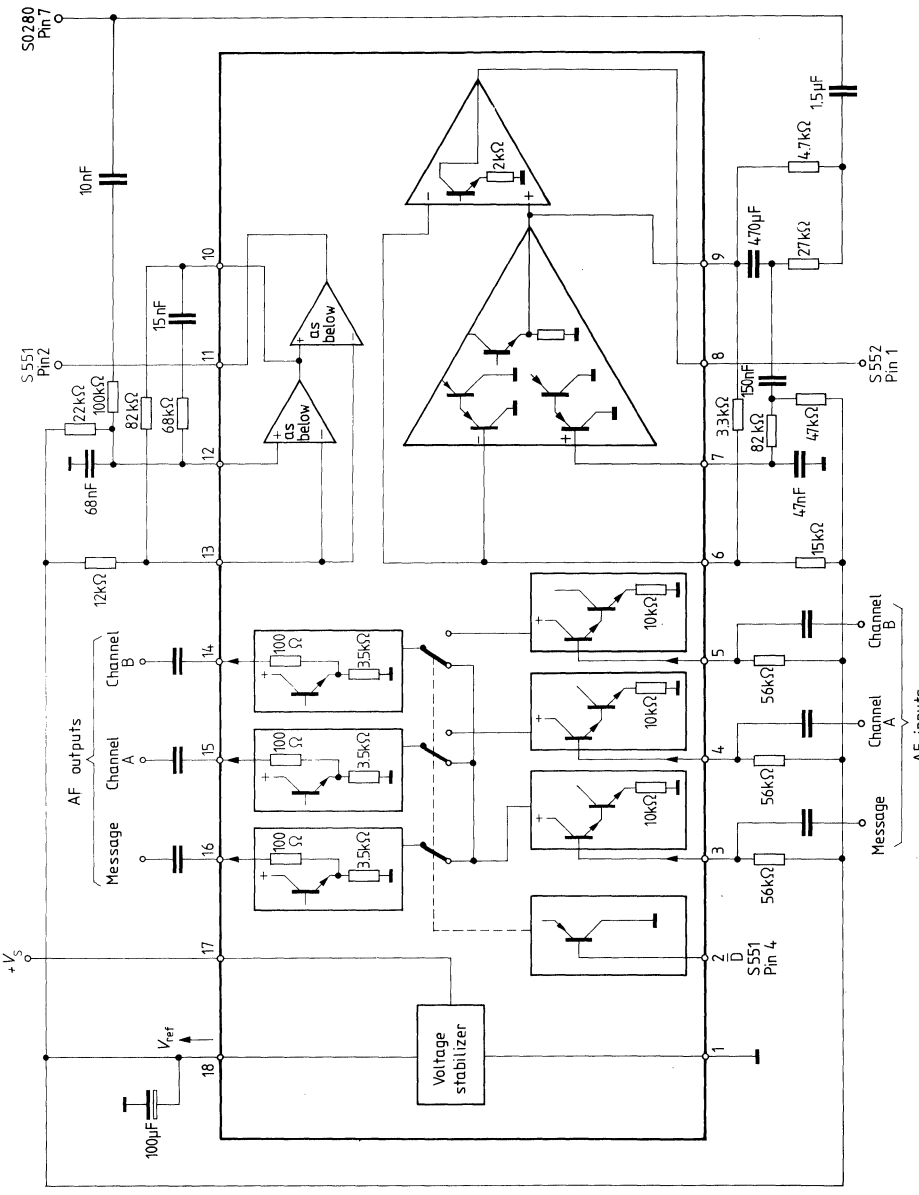
Range of operation

Supply voltage range	V_{17}	10 to 16	V
Ambient temperature range	T_{amb}	−20 to 85	°C

Characteristics (V_{17} = 14 V, T_{amb} = 25 °C)

		min	typ	max	
Current consumption	I_{17}		15	30	mA
Band filter amplifier					
Voltage gain (open loop) (f = 150 Hz)	G_{vo}	50	64		dB
Dynam. output resistance at open loop voltage gain	$R_{9/10}$	1.2			kΩ
Limiter amplifier					
Voltage gain (open loop)	G_{vo}	50			dB
Input voltage	$V_{6/9}$; $V_{10/13}$			4	V_{pp}
H output leakage current	$I_{8/11}$			50	µA
DK switch, control input D					
L-input voltage	V_{i2}			0.8	V
L-input current (V_2 = 0.8 V)	$-I_{i2}$			1	µA
H-input voltage	V_{i2}	2.8			V
H-input current (V_2 = 2.8 V)	$-I_{i2}$			0.5	µA
Switches					
Forward gain	G	2	3	4	dB
Rejection loss	a_{rej}	50	60		dB
Cross talk rejection from channel to channel					
f = 1 kHz	a_{cr}	50			dB
f = 10 kHz	a_{cr}	40			dB
Large signal behavior of the inputs THD = 1%	$V_{3/4/5}$		2	3	V_{pp}
THD = 10%	$V_{3/4/5}$		2.5		V_{pp}
Input resistance	R_{i3}; R_{i4}; R_{i5}	500			kΩ
Input current	I_{i3}, I_{i4}, I_{i5}			0.1	µA
Output resistance	R_{q3}; R_{q4}; R_{q5}		0.3	2	kΩ
	R_{q16}		175		Ω
Interference voltage at the output (f = 10 Hz to 10 kHz, 3 dB down)	V_{14}; V_{15}; V_{16}		12	20	µV
Reference voltage	V_{18}	3.1	3.4	3.7	V

Block diagram



Message Decoder for FM Road Traffic Information Service

S 551

MOS circuit

The MOS circuit S 551, built up in depletion-load-technology, constitutes in connection with the two bipolar circuits S 0280 (Station Decoder) and S 0281 (Message Decoder) and the MOS circuit S 552 (Area Decoder) the main portion of a traffic broadcast decoder used for car radios.

The traffic broadcast decoder (VRF decoder) recognizes a VRF station and the traffic messages (VDS) transmitted by it. An additional unit, the area decoder, ensures to identify the regional identity of a station. The VRF decoder also permits automatic search for a VRF station.

The S 551 is intended to recognize a traffic broadcast message. The technical prerequisites for this are the presence of identification frequencies jointly used by the various broadcasting stations:

VRF frequency: 57 kHz
VDS frequency: 125 Hz

Type	Ordering code	Package outline
S 551	Q 67100-Z109	DIP 18

Maximum ratings (all voltages referred to $V_{DD} = 0$ V)

		min	max	
Supply voltage	V_{SS}	−0.3	18	V
Input voltage	V_i	0	V_{SS} +0.3	V
Power dissipation	P_{tot}		360	mW
Power dissipation per output (one output at a time)	P_q		100	mW
Storage temperature	T_{stg}	−40	125	°C

Range of operation (referred to $V_{DD} = 0$ V)

Supply voltage range	V_{SS}	9 to 16	V
Ambient temperature range	T_{amb}	−25 to 85	°C

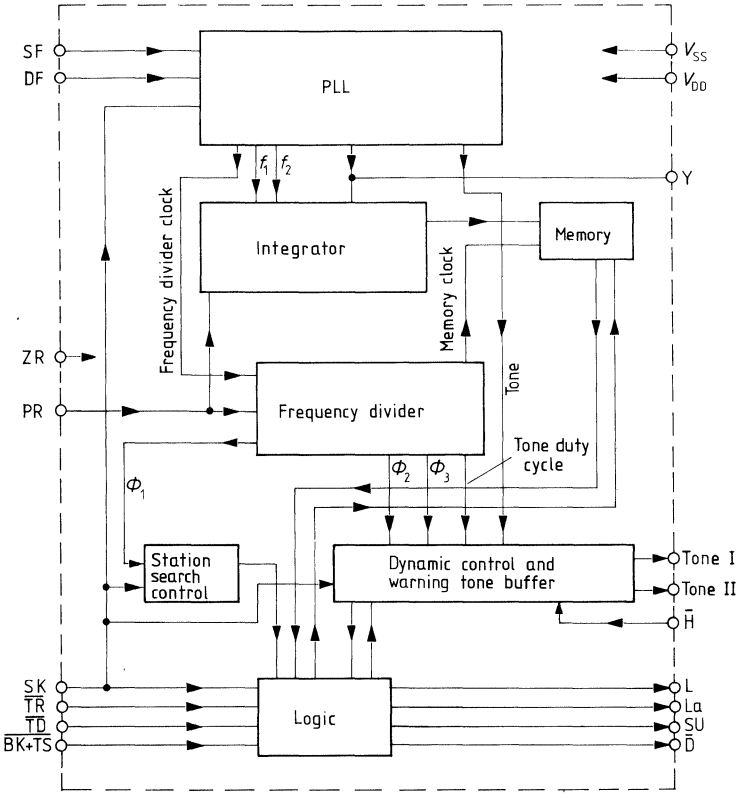
Characteristics (all voltages referred to V_{DD} = 0 V)

		min	typ	max	
Supply current	I_{SS}			15	mA
Inputs					
Transmission frequency SF (57 kHz) (Internal pull-high resistor)					
Message frequency DF (125 Hz) (Internal pull-high resistor)					
H-pulse width (Duty cycle approx. 1:2)	t_{WH}				
L-pulse width (Duty cycle approx. 1:2)	t_{WL}				
H-L-transition time	t_{THL}			3.5	µs
L-H transition time	t_{TLH}			3.5	µs
Harmless H-input current	$\lvert I_{iH} \rvert$			1	µA
L-input source resistance (to V_{DD})	$R_{i\,QL}$			10	kΩ
L-input source resistance (to V_{DD} +1 V)	$R_{i\,QL}$			6	kΩ
Button radio $\overline{TR}$ (see fig. 1) **Button message $\overline{TD}$** (see fig. 2) (Internal pull-high resistor)					
Transmission identification SK (from DK analog circuit) (Internal pull-high resistor)					
Harmless H-input current	$\lvert I_{iH} \rvert$			1	µA
L-input source resistance (to V_{DD})	$R_{i\,QL}$			5	kΩ
L-input source resistance (to V_{DD} +1 V)	$R_{i\,QL}$			3	kΩ
Area identification $\overline{BK+TS}$					
Warning tone suppression $\overline{H}$ (see fig. 3)					
H-input voltage	V_{iH}	V_{SS}−1.5 V		V_{SS}	
L-input voltage	V_{iL}			2	V
Required input current	$\lvert I_i \rvert$			10	µA
Reset input ZR (see fig. 4)					
H-input voltage (Reset)	V_{iH}	V_{SS}−1.3 V		V_{SS}	
L-input voltage (release)	V_{iL}			2	V
H-pulse width	t_{WH}	20			µs
Required input current	$\lvert I_i \rvert$			10	µA

Characteristics (all voltages referred to V_{DD} = 0 V)

Outputs		min	typ	max	
Station search SU Loud-circuit La					
H-output voltage (at/I/ = 0.05 mA)	$V_{q\,H}$	$V_{SS}-5$ V		V_{SS}	
L-output voltage (at/I/ = 1 µA)	$V_{q\,L}$			0.35	V
Short circuit current	$\lvert I_{SC\,max} \rvert$			10	mA
Lamp L					
H-output voltage (at/I/ = 0.5 mA)	$V_{q\,H}$	$V_{SS}-7$ V		V_{SS}	
L-output voltage (at/I/ = 1 µA)	$V_{q\,L}$			0.35	V
Short circuit current	$\lvert I_{SC\,max} \rvert$			10	mA
Message $\overline{D}$					
H-output voltage (at/I/ = 0.2 mA)	$V_{q\,H}$	$V_{SS}-3$ V		V_{SS}	
L-output voltage (at/I/ = 1 µA)	$V_{q\,L}$			0.35	V
Short-circuit current	$\lvert I_{SC\,max} \rvert$			10	mA
Tone I (see fig. 5)					
H-output voltage (loud) (see test circuit 1)	$V_{q\,HI}$	$\frac{6}{10} V_{SS}$	$\frac{9}{10} V_{SS}$	V_{SS}	V
L-output voltage (see test circuit 1)	$V_{q\,L}$			100	mV
H-output voltage (medium) (see test circuit 1)	$V_{q\,H\,m}$		$\frac{3}{10} V_{SS}$		V
H-output voltage (soft)	$V_{q\,H\,s}$		$\frac{1}{10} V_{SS}$		V
Turn-off damping (referred to operating level)	a	60	80		dB
Sequence frequency	$\frac{1}{T}$		appr. 2		Hz
Tone frequency	f_{tone}		appr. 1.7		kHz
Duty cycle	t_1/T		approx.1/4		
Tone II (see fig. 6)					
H-output voltage (see test circuit 2)	$V_{q\,H}$	$\frac{1}{2} V_{SS}$	$\frac{3}{4} V_{SS}$	V_{SS}	V
L-output voltage (see test circuit 2)	$V_{q\,L}$			100	mV
H-output voltage (soft) (see test circuit 2)	$V_{q\,H\,s}$		$\frac{1}{4} V_{SS}$		V
Turn-off damping (referred to operating level)	a	60	80		dB
Sequence frequency	$\frac{1}{T}$		appr. 2		Hz
Tone frequency	f_{tone}		appr. 1.7		kHz
Duty cycle	t_1/T		appr. 1/4		

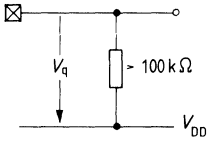
Block diagram



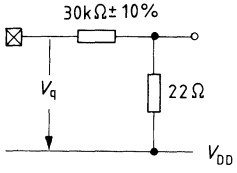
Pin designation

Pin No.	Description	Pin No.	Description
1	Transmission frequency SF	10	V_{SS}
2	Message frequency DF	11	Warning tone suppression $\overline{H}$
3	Loud-circuit La	12	Station search SU
4	Message $\overline{D}$	13	Tone II (undelayed)
5	Lamp L	14	V_{DD}
6	Key radio $\overline{TR}$	15	Tone I (delayed)
7	Key message $\overline{TD}$	16	Y for testing purposes
8	Area identification $\overline{BK+TS}$	17	Reset ZR
9	Transmission identification SK	18	Test pin PR

Test circuit 1
tone I



Test circuit 2
tone II



Measuring the turn-off damping

1. The supply voltage is kept constant during the measurement.
2. The measurement is taken with respect to the V_{DD} pin.
3. The measurement is taken selectively for the basic frequency.

For operation with button "reset" of the function, at reapplication of supply voltage

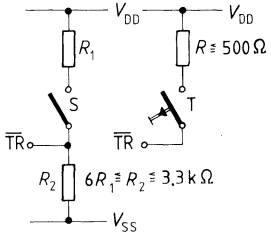


Figure 1

Connection of the $\overline{TD}$-input

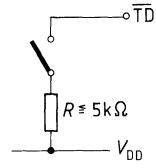


Figure 2

Suggested connection of the $\overline{H}$-Input

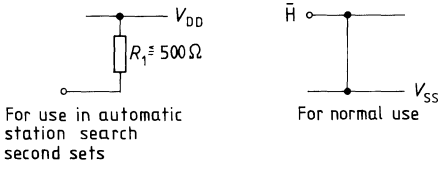


Figure 3

Circuit for automatic reset upon turn-on

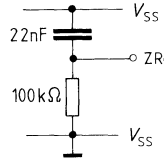


Figure 4

Output signals of the tone I output

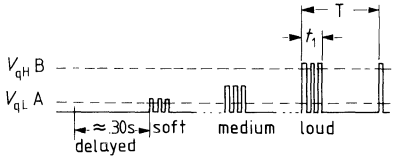


Figure 5

Output signals of the tone II output

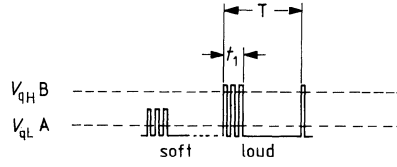


Figure 6

Functional description of the S 551

The S 551 contains 7 function blocks. The 4 blocks used for the recognition of the 125 Hz VDS tone constitute the largest portion of the circuit. They comprise a PLL-circuit (phase locked loop), an integrator, a memory, and a frequency divider. The PLL-circuit is a 2-stage synchronous counter, the first portion of which can be switched between 28 and 29 counting steps. The subsequent divider has a 3-bit and a 4-bit output. A 57 kHz rectangular signal is used as the clock frequency for the block. The two portions of the counter are interconnected in such a way that a 125 Hz signal appears at the 4-bit output as mean value. An incoming DF is applied to an Exclusive-OR-gate by means of this signal; the output of this gate causes the switching of the counting steps of the first PLL-divider stage. The frequency at the 4 bit output is thereby displaced in time, until a stable divider ratio is produced at the output of the Exclusive-OR-gate. However, this is only possible when the DF amounts to approximately 125 Hz.

As an indicator whether the PLL has recognized a DF as correct, the output of a second Exclusive OR-gate (Y) is used which has, as its input signals, the DF and also a reference frequency from the PLL divider for comparison, which has been phase-shifted by 90°. The output Y is consistently at an H-potential as long as the DF is proper. Small deviations of the DF with respect to the reference frequency are indicated by "low"-times within a Y-period. In the case of major frequency deviations, the PLL is continuously trying to fit the reference frequency to the DF, which results in a Y-signal appearing to be irregular as a first impression.

For the evaluation of the Y-signal, the integrator is used. It is an 11-bit synchronous up-down counter, which is defined in its counting direction by "Y". As clock frequencies, two clocks derived from the PLL circuit are available ($f_1 = 57\,\text{kHz}\ 2^{-2}$ and $f_2 = 57\,\text{kHz}\ 2^{-3}$). These clock signals are also selected by the Y-signal. The integrator is constructed in such a way, that due to Y = high — for incrementing slowly — and Y = low — for decrementing fast — the two possible counting combinations are achieved. For this reason a full-counting of the integrator is only possible when the L-portion within a Y-period is smaller than 1/3. An evaluation of the counter contents is done through a hysteresis circuit, with thresholds at the counter contents 1/4 full and 3/4 full. In order to make the DK less sensitive to short-time turn-offs of the VRF-broadcasting frequencies, the integrator is followed by a memory. The memory is a 4-bit synchronous incrementer/decrementer. Its clock frequency is about $57\,\text{kHz}\ 2^{-14}$ and is derived from a central frequency divider. The counting direction of the memory is defined by a hysteresis circuit. When the hysteresis circuit indicates a full integrator, the memory will still be empty, but its output "DK" (internal signal) already indicates a message. From this point on, the counter increments until it is full and remains that way. At this counting position, the memory is able to compensate for a gap in the VDS frequency of approximately 4,6 s. After this time the memory is empty and the DK signal goes high. A 9-bit counter serves as a central frequency divider. It has been constructed for the first 5-bit as a synchronous counter and for the rest as an asynchronous counter. The various input clocks used in the IC are taken from the appropriate divider stages or are decoded. As input clock the reference frequency of 125 Hz from the PLL is used.

An additional block consists of logic circuits which are not directly related to each other. The purpose of this circuit is an improvement in the comfort of handling.

The inputs $\overline{TR}$, $\overline{TD}$, $\overline{BK+TS}$, SK and $\overline{H}$ and the internal signal DK determine the output functions L (lamp), La (loud circuit), $\overline{D}$ (message decoding), SU (station searching).

A low level at input $\overline{TR}$ (key broadcast) indicates that no VRF operation is intended. The input behaves in a bistable way; for switching it requires a low resistance driving. When the supply voltage is turned on again, the input is automatically set to VRF operation.

A low level at input $\overline{TD}$ (key message) indicates that only road traffic information messages are to be reproduced.

A low level at input $\overline{BK+TS}$ (area identification or key "only broadcast recognition") indicates that either the area identification circuit (BK IC) has recognized the wanted area identification signal or that area distinguishing is not wanted.

A high level from the SK analog IC at input SK (transmission identification) indicates that the station received is a VRF station.

Through a low level at input $\overline{H}$, the circuit can be reprogrammed for the use in a station-searching second set. This function acts upon the warning tone.

The lamp output L shows a high level when the wanted kind of operation may be performed. For this purpose the SK (transmission identification) input must receive an H-signal which means that a station with the proper transmission identification is being received. In addition, the $\overline{BK+TS}$ (area identification or transmission identification only) input must receive an L-signal which means that a station of the wanted area is being received or that no area identification is wanted.

This is also true in the case that no VRF function is wanted (key "broadcast") pushed: $\overline{TR} = 0$).

$$L = SK\ \overline{BK+TS}$$

Output La from the loud-switch controls the loudspeaker amplifier. With a high level it sets the loudness to:

$$La = D + TR + L \cdot \overline{TD}$$

The message-identification output $\overline{D}$ indicates with a low level that a message is being recognized and the station received is located in the wanted area. With the key "broadcast" this signal is suppressed.

$$D = DK \cdot L \cdot \overline{TR}$$

Station search output SU controls the automatic VRF station searching motion. (High level: search, low level: stop).

$\overline{SU}$ = TR + L + stop pulse (SK)

The stop pulse lasts about 0.5 s; it is produced every time a VRF station has been found (SK = high) to give the BK IC a chance to check whether or not the area identification is correct. (Own 4-bit asynchronous counter with frequency 57 kHz 2^{-12}). Station search is started with a delay to avoid response to brief noise signals received.

The output tone 1 produces a warning when no VRF station is received from the wanted area.

Tone 1 = $\overline{TR + L}$

However, the tone is turned-on no sooner than about 30 s after this condition has been established. Through a dynamic stage it is produced at first four times soft then four times medium and finally loud.

(The delay and the dynamic control consist of a 5-bit asynchronous counter with a clock frequency of approx. 57 kHz 2^{-17}).

The output tone II is different from tone I by producing a warning tone undelayed and only in two dynamic stages (four times soft and then loud). For this function a resistor to V_{DD} is required.

In connection with station search second sets a warning tone will make no sense if no VRF station can be received at all (poorly covered area). In this case the station search second set is to continue searching to discover a VRF station as soon as possible. Not before a VRF station has been found, which does not belong to the wanted area, however, a warning tone will make sense again indicating the possibility of an improved operation.

Operation:

If no VRF station can be received, the SU signal remains low. As soon as a VRF station has been found during the periodic searches, periodic pulses with SU = high occur. When the $\overline{H}$-input is low, the warning tone is blocked if SU remains low for a period exceeding 20 s.

Note:

Inputs PR and Y are intended for testing. They must not be externally connected for other purposes.

Area Decoder for FM Road Traffic Information Service

S 552

MOS circuit

The MOS circuit S 552, built up in depletion load technology, is an extension of the two bipolar circuits S 0280 (station decoder), S 0281 (message decoder) and the MOS circuit S 551 (message decoder), which together constitute the main portion of a traffic broadcast decoder used in car radios.

The S 552 recognizes the identification frequency of a VRF station of a specific region and switches traffic messages of only this station to the loudspeaker. The S 552 has been designed for 6 different area frequencies, which can be pre-selected at inputs $\overline{A}$ to $\overline{F}$.

Type	Ordering code	Package outline
S 552	Q 67100-Z110	DIP 16

Maximum ratings (all voltages referred to $V_{DD} = 0$ V)

		min.	max.	
Supply voltage	V_{SS}	−0.3	18	V
Input voltage	V_i	0	V_{SS} +0.3	V
Total power dissipation	P_{tot}		400	mW
Power dissipation per output	P_q		100	mW
Storage temperature	T_{stg}	−40	125	°C

Range of operation (referred to $V_{DD} = 0$ V)

Supply voltage range	V_{SS}	9 to 16	V
Ambient temperature range	T_{amb}	−25 bis 85	°C

Characteristics (all voltages referred to V_{DD} = 0 V)

		min.	typ.	max.	
Supply current	I_{SS}			15	mA
Inputs					
Transmission frequency SF (57 kHz) (internal pull-high resistor)					
Area frequency BF (internal pull-high resistor) (A = 23.79 Hz, B = 28.32 Hz, C = 34.98 Hz, D = 39.65 Hz, E = 45.75 Hz, F = 54.04 Hz)					
H-pulse width (Duty cycle approx. 1:2)	t_{WH}				
L-pulse width (Duty cycle approx. 1:2)	t_{WL}				
H-L transition time	t_{THL}			3.5	µs
L-H transition time	t_{TLH}			3.5	µs
Harmless H-input current	I_{iH}			1	µA
L-input source resistance (to V_{DD})	$R_{i\,QL}$			10	kΩ
L-input source resistance (to V_{DD} + 1 V)	$R_{i\,QL}$			6	kΩ
Transmission identification SK (from DK analog circuit) (internal pull-high resistor)					
Harmless H-input current	$\lvert I_{iH} \rvert$			1	µA
L-input source restistance (to V_{DD})	$R_{i\,QL}$			5	kΩ
L-input source resistance (to V_{DD} +1 V)	$R_{i\,QL}$			3	kΩ

Characteristics (all voltages referred to V_{DD} = 0 V)

		min.	typ.	max.	
Programming inputs $\overline{A}$...$\overline{F}$ (see fig. 1) (Internal pull-high resistor)					
Harmless H-input current	$\lvert I_{iH} \rvert$			1	µA
L-input source resistance (to V_{DD})	$R_{i\,QL}$			5	kΩ
L-input source resistance (to V_{DD} +1 V)	$R_{i\,QL}$			3	kΩ
Reset input ZR (see fig. 2)					
H-input voltage (Reset)	V_{iH}	V_{SS} – 1.3 V		V_{SS}	
L-input voltage (released)	V_{iL}			2	V
H-pulse width	t_{WH}	20			µs
Required input current	I_i			10	µA
Area identification $\overline{BK}$					
H-output voltage (at /I/ <10 µA)	$V_{q\,H}$	V_{SS} – 1.3 V		V_{SS}	
L-output voltage (at /I/ <10 µA)	$V_{q\,L}$			1.5	V
Short circuit current (Continuously short circuit proof)	$I_{SC\,max.}$			1	mA

Connection of programming inputs $\overline{A}$...$\overline{F}$

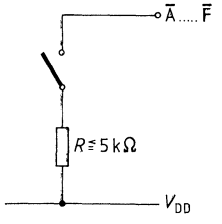


Figure 1

Circuit for automatic reset upon turn-on

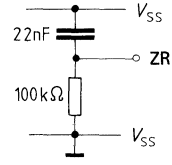
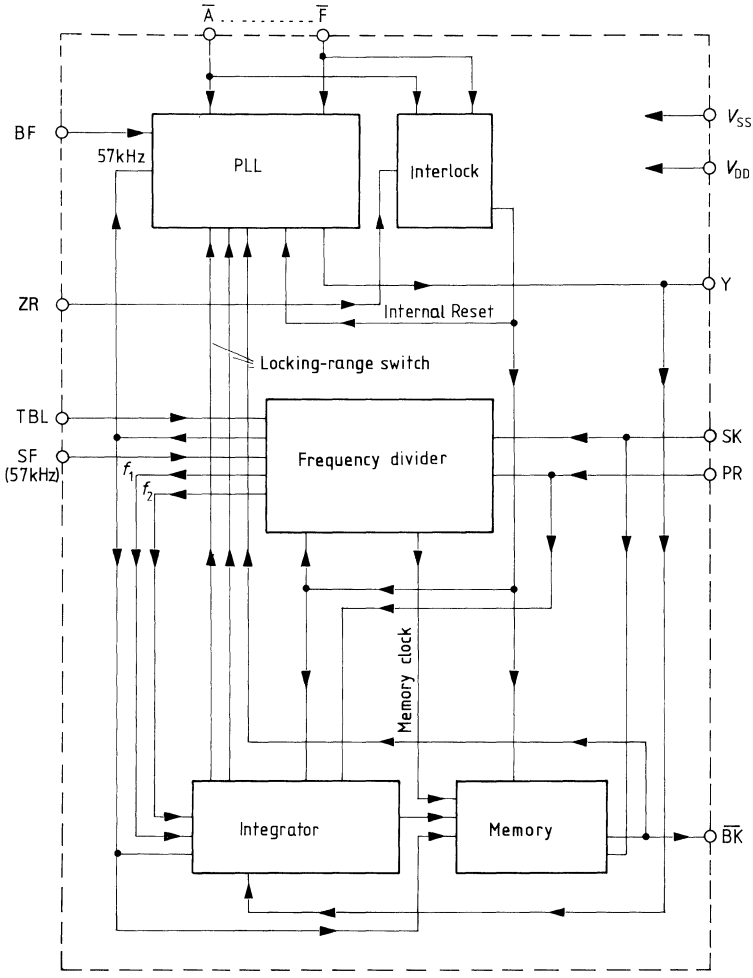


Figure 2

Block diagram



Pin designation

Pin No.	Description	
1	Area frequency BF	
2	Transmission identification SK	
3	Reset ZR	for testing purposes
4	Testing PR	
5	Y-input/output	
6	Clock blocking TBL	
7	Station frequency SF	
8	V_{SS}	
9	V_{DD}	
10	Area selection $\overline{F}$	
11	Area selection $\overline{E}$	
12	Area selection $\overline{D}$	
13	Area selection $\overline{C}$	
14	Area selection $\overline{B}$	
15	Area selection $\overline{A}$	
16	Area identification $\overline{BK}$	

Functional description of the S 552

The area decoder circuit S 552 is an extension of the VRF decoder system. It is used to recognize the area frequency (identification frequency of the VRF station of a region). The S 552 has been designed for 6 different area frequencies (BF), which are preselected by means of an L level at the programming inputs $\overline{A}$-$\overline{F}$. This can be done with a switch, which briefly opens all inputs when turned, as well as with a switch which bridges several inputs simultaneously when operated.

The circuit contains a PLL portion like the S 551. It consists of three synchronous counters in series. The first of these counters can be switched between the two counting positions 23 and 25. In addition, for an extension of the locking range, two additional counter combinations are possible: 21/27 and 19/29. The switching of the locking range is done by an integrator following the PLL. The second divider of the PLL circuit can be switched externally through the $\overline{A}$-$\overline{F}$ inputs. With an L-level at $\overline{A}$ it divides by 25, at $\overline{B}$ by 21, at $\overline{C}$ by 17, at $\overline{D}$ by 15, at $\overline{E}$ by 13 and at $\overline{F}$ by 11. In order to convert, through division, a 57 kHz SF-signal into a BF-signal, the PLL contains an additional 2-bit divider. Corresponding to the programming inputs $\overline{A}$ . . . $\overline{F}$ used, the PLL generates an internal BF signal. An externally applied BF (at the BF input) is applied to an exclusive-OR-gate together with the internal signal. The output of this gate causes switching of the counting steps at the first divider stage (e.g. 23/25). Thereby the internal BF is shifted in phase until a stable switching ratio has been obtained.

As an indication that the PLL has recognized a BF properly, the output of a second exclusive OR (Y-signal) gate is used; the inputs of this gate are the internal reference frequency, shifted by 90°, and the BF.

In case of a stable switching ratio mentioned above, Y has a high level and thereby indicates the recognition of a proper BF. If the BF received is wrong, the Y output shows an irregular signal.

Just as in the case with S 551, the S 552 also contains an integrator and a memory. Both blocks receive their clock frequency from an internal frequency divider. This frequency divider essentially consists of a synchronous counter, which generates the integrator clock, and an asynchronous divider operated in series, which supplies the memory clock.

The integrator is an 8-bit synchronous up-down counter. Its clock frequency depends on the PLL output. For Y = high it amounts to approx. 2370 Hz and at Y = low 4750 Hz. In addition, the direction of counting of the integrator is determined by the level of the Y signal. At the high clock frequency it counts down (at Y = low) and at the low frequency it counts up (Y = high). The minimum duty cycle of the Y signal for upcounting of the integrator is $<1:3$ for Y = Low.

An evaluation of the contents of the counter is done by means of a hysteresis circuit with thresholds at counter contents 1/4 full and 3/4 full. In addition, the integrator stages with the highest significance determine a change of the locking range in the first PLL divider stage.

When the integrator is empty (0 to 1/4), the PLL-divider can be switched between 19 and 29 counting steps, when the integrator has been partially filled (1/4 to 1/2) between 21 and 27 steps and if it is filled more than 1/2 or if $\overline{BK}$ = low between 23 and 25 counting steps.

When the integrator is full or when the memory is not entirely empty, the output $\overline{BK}$ = low. The memory will bridge a brief disappearance of SK or BF. It consists of a 4-bit synchronous up/down counter and the maximum storage time amounts to approx. 6 s. Its clock frequency is approx. 2.3 Hz. When the hysteresis output shows a full integrator the memory counts up and for an empy integrator down. The hysteresis signal, together with the Q_1 outputs of the individual memory bits, forms the $\overline{BK}$-signal through a gate. Therefore the $\overline{BK}$ output remains low for additional 6 s after the integrator has counted down to zero.

Note:

The inputs TBL, PR and Y are intended for testing purposes. They must not be connected externally.

MOS circuit

Digital storing and retrieving of the tuner voltage according to the voltage synthesis concept may be performed by means of the SDA 5690 R IC, designed in MOS depletion technology, in connection with a nonvolatile memory.

The system comprises 3 ICs, a multistage RC low-pass, and several external components. The tuning voltage is digitized into a 10-bit word, thus obtaining a resolution accuracy of approximately ±10 kHz throughout the entire VHF bandwidth.

- Few external components
- Fine-tuning during storage
- Mute signal during progam change or storage
- Frequency monitoring of a stored station

Type	Ordering code	Package outline
SDA 5690 R	Q67100-Z138-R	DIP 28

Maximum ratings (referred to $V_{DD} = 0$ V)

Supply voltage	V_{SS}	0 to 17	V
Input voltage	V_i	0 to 17	V
Power dissipation per output (unless otherwise specified under characteristic data)	P_q	10	mW
Total power dissipation	P_{tot}	500	mW
Thermal resistance (system-air)	$R_{th\ SA}$	60	K/W
Storage temperature range	T_{stg}	−55 to 125	°C

Range of operation (referred to $V_{DD} = 0$ V)

Supply voltage range	V_{SS}	5 to 14	V
Ambient temperature range	T_{amb}	0 to 70	°C

Characteristics (all voltages referred to V_{DD})

		min	typ	max	
Supply current (V_{SS} = 12 V)	I_{DD}		3	10	mA
Inputs					
switch-on reset-POR					
forward-backward K					
(incl. pull-high resistors)					
H-input voltage	V_{iH}	11		12	V
(test circuit 1, V_{SS} = 12 V)					
L-input voltage	V_{iL}	0		7.5	V
(test circuit 1, V_{SS} = 12 V)					
Input short-circuit current (V_{SS} = 12 V)	I_{iL}	−100		−10	µA
Inputs					
Store S					
Progr. selection V_1, V_2, V_3, V_4, V_5, V_6, V_7, V_8, TP, TQ					
(incl. pull-high resistors)					
H-input voltage	V_{iH}	11		12	V
(test circuit 1, V_{SS} = 12 V)					
L-input voltage	V_{iL}	0		7.5	V
(test circuit 1, V_{SS} = 12 V)					
Input short-circuit current (V_{SS} = 12 V)	I_{iL}	−50		−5	µA
Inputs DM, L					
H-input voltage	V_{iH}	11		12	V
(test circuit 1, V_{SS} = 12 V)					
L-input voltage	V_{iL}	0		7.5	V
(test circuit 1, V_{SS} = 12 V)					
Input oscillator CL	f_{osc}		455*		kHz
Output DM					
(open-drain output)					
H-output voltage	V_{qH}	11		12	V
(test circuit 2, I_{qH} = 100 µA, V_{SS} = 12 V)					
Leakage current (test circuit 2, V_{SS} = 12 V)	I_{qlk}			1	µA
Power dissipation	P_q			50	mW
Output Store ST					
(open drain output)					
H-output voltage	V_{qH}	11		12	V
(test circuit 2, I_{qH} = 300 µA, V_{SS} = 12 V)					

* Murata Resonator CSB 455

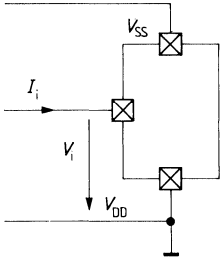
Characteristics (all voltages referred to V_{DD})

		min	typ	max	
Leakage current (V_{SS} = 12 V)	$I_{q\,lk}$			1	µA
Power dissipation	P_q			50	mW
Output Mute—M					
(open-drain output, short-circuit proof)					
(test circuit 2)					
H-output current ($V_{q\,H}$ = 2.6 V; V_{SS} = 5 V)	$I_{q\,H}$	500		1600	µA
Leakage current (V_{SS} = 12 V)	$I_{q\,lk}$			1	µA
Power dissipation	P_q			50	mW
Output DA					
(open drain output)					
(test circuit 2)					
H-output voltage ($I_{q\,H}$ = 400 µA)	$V_{q\,H}$	9.4		12	V
Leakage current (V_{SS} = 12 V)	$I_{q\,lk}$			10	µA
Power dissipation	P_q			80	mW
Outputs					
(Test circuit 2)					
Retrieval W					
memory location Address A, B, C					
H-output voltage ($I_{q\,H}$ = 100 µA)	$V_{q\,H}$	11		12	V
L-output voltage ($I_{q\,L}$ = −10 µA)	$V_{q\,L}$	0		1	V
Output					
memory shift clock I					
(testc circuit 2)					
H-output voltage (V_{SS} = 12 V; $I_{q\,H}$ = 50 µA)	$V_{q\,H}$	11		12	V
L-output voltage (V_{SS} = 12 V; $I_{q\,L}$ = −20 µA)	$V_{q\,L}$	0		1	V
Output					
program change PC*					
(test circuit 2)					
H-output voltage (V_{SS} = 12 V; $I_{q\,H}$ = 100 µA)	$V_{q\,H}$	11		12	V
L-output voltage (V_{SS} = 12 V; $I_{q\,L}$ = −5 µA)	$V_{q\,L}$	0		1	V

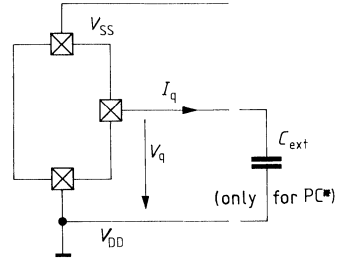
Characteristics (all voltages referred to V_{DD})

		min	typ	max	
H-L transition time (C_{ext} = 20 pF)	t_{HL}			10	µs
Output					
turn-on reset PR					
(test circuit 2)					
H-output voltage	$V_{q\,H}$	11		12	V
($I_{q\,H}$ = 20 µA; V_{SS} = 12 V)					
L-output voltage	$V_{q\,L}$	0		1	V
($I_{q\,L}$ = −2 µA; V_{SS} = 3.3 V)					
Changeover values (V_{SS} − V_{DD})		3.3	3.8	4.5	V
(refer to test diagram)					

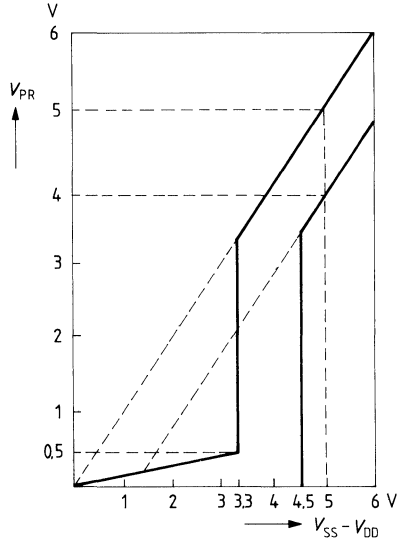
Test circuit 1



Test circuit 2



Test diagram



Circuit description

1. Total system — survey

The total system for digital storage and retrieval of the tuning voltage is based on a voltage synthesis concept which comprises three ICs, a multistage RC low-pass, and several discrete peripherals. The tuning voltage is digitized into a 10 bit word, thus resulting in a resolution accuracy of approximately ±10 kHz at 20 MHz bandwidth. An AFC operates in addition. Maximally 8 programs or 16 programs, respectively, can digitally be processed from the SDA 5690 R to the SDA 5650 R memory for storage.

The P-MOS control circuit SDA 5690 R mainly performs a DA conversion in case of program fetch or an AD conversion for program storage. It operates according to a counting method.

The 10-bit digital value is represented as periodic squarewave signal of constant frequency, with the IFO being of the order of the pulse width. The following low-pass filtering yields in the mean time value thus delivering the analog value. The low pass consists of a switching stage in order to generate the voltage swing of 0 to V_{stab} and the passage characteristic for adaptation to the capacitance diode characteristic curve as well as of several RC networks, to minimize the ripple of the analog voltage (<10 µV).

The comparator TDB 0453 A is necessary for the AD conversion. In case of scale operation (button U_{scale}), the comparator output instructs the control unit to vary the digital value such that the low-pass voltage V_C aims at equality with the scale potentiometer voltage V_{pot}. The converter velocity was designed such that equality can be achieved during transmitter setting and storage. The digital value of V_{pot} can then be stored.

With the aid of the tuning knob and the muting circuit, the frequency of a stored transmitter can be retrieved on the scale.

2. Function of the control IC SDA 5690 R

The converter comprises each a 10-stage cycle counter, a digital comparator, and an IFO register which operates either as incrementer/decrementer or as shift register. The periodically circulating cycle counter is clocked by an oscillator of approximately 455 kHz. The digital value equivalent to the tuning voltage is to be found in the IFO register. The conversion into a corresponding pulse width is done such that an F-F is set at the initial position of the cycle counter, and reset when equalization between cycle and IFO counter is achieved. In accordance with the 2^{10} possible IFO counter positions, there are also 2^{10} different pulse widths. The period of the DA output signal is 4 ms, it is subdivided into 8 individual pulses in order fo facilitate filtering. The program button inputs lead to the input logic which recognizes the button pressure and performs binary encoding. A locking device ensures that simultaneous pressure of two buttons does not lead to the recognition of the binary value of a third button. On principle, the last pressed button becomes active. With the aid of the divider and the control logic all clocks necessary for command recognition and data transfer are generated.

2.1 Program change

- press U_1 to U_8
- load the program storage address A, B, C
- transmit the PC* signal as read instruction for the memory; the data pin DM is switched as input; DE, DA of the memory as output.
- transmit 10 Φ clocks; shift the memory IFO in the IFO register.
- convert the IFO into one pulse width
- the filtered diode voltage V_{LP} is fed to the tuner

2.2 Storage

- press the button U_{scale}
- tune with scale potentiometer

The scale potentiometer voltage V_{pot} is directly fed to the tuner, it is also applied to the analog comparator. The comparator compares the voltage V_C which corresponds to the IFO register level, with V_{pot}. In case of inequality the comparator output determines via pin K in which direction the IFO register, switched as a counter, has to run such that equality will be achieved. The comparator itself does not determine "equality", but only "greater" or "less". For this reason, the digital value cannot be more precise than 1 LSB. At first, the IFO register is provided with a clock frequency of approximately 250 Hz.

Owing to this higher clock frequency as well as to possible incrementing/decrementing, the low-pass voltage will follow after a reasonable period of time at a change of the scale potentiometer voltage, i. e. there is no waiting period between the finished tuning process and pressing the store button. Because of the high response time of the low pass — given by the severe requirement as to ripple — the counter removes too far from the exact value (approx. ± 8 steps) when reaching equality of $V_C = V_{pot}$. Therefore, retuning during storage follows.

- Storage process

At first the store button is pressed and kept down, subsequently the desired program button is actuated. The store button can be released, thereafter. After having actuated the store button retuning takes place by continuously slowing the clock frequency down during 1 second. After the course of this time the digital value reaches an accuracy of 1 LSB. Immediately after that the contents of the IFO register is moved into the memory:

- transmit ST signal
- data pin DM is switched as output; DA is brought into the high-ohmic state by the memory
- transmit 10 Φ-clocks; shift IFO from the control device to the memory and memorize.

After the memory has finished the erasing and writing procedures — indicated with the signal L — then the stored station is read out again for control purposes.

2.3. Further particulars

2.3.1. Muting

During program change or storage, the M output is switched to "H". Thus, the sound can be muted during undefined states of the voltage V_{LP}.

2.3.2. Frequency control of a stored transmitter

At first, the store button is pressed and kept pressing; "H" appears at M; i.e. the sound becomes quiet. Now the scale potentiometer is turned until the sound is audible again within a narrow range of the scale. This means again that equality between V_{pot} and V_c is given at this spot of the scale; the comparator causes the sound to be switched on with M = "L".

The frequency can be read from the scale.

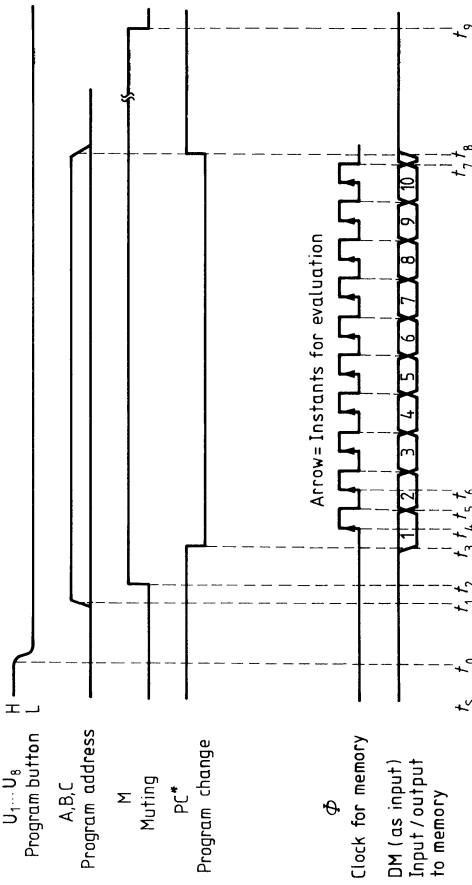
2.3.3. Switch-on reset

If supply voltage is applied to the device, the input POR will get a signal change from "L" to "H" from the memory. This signal change automatically causes a program change, when a program button is pressed.

2.3.4. Program extension

The non-volatile memory SDA 5650 R has a capacity of max. 16 x 10 bit. With an according changeover of the addressing input A4 also up to 16 stations may be stored.

Program change timing diagram

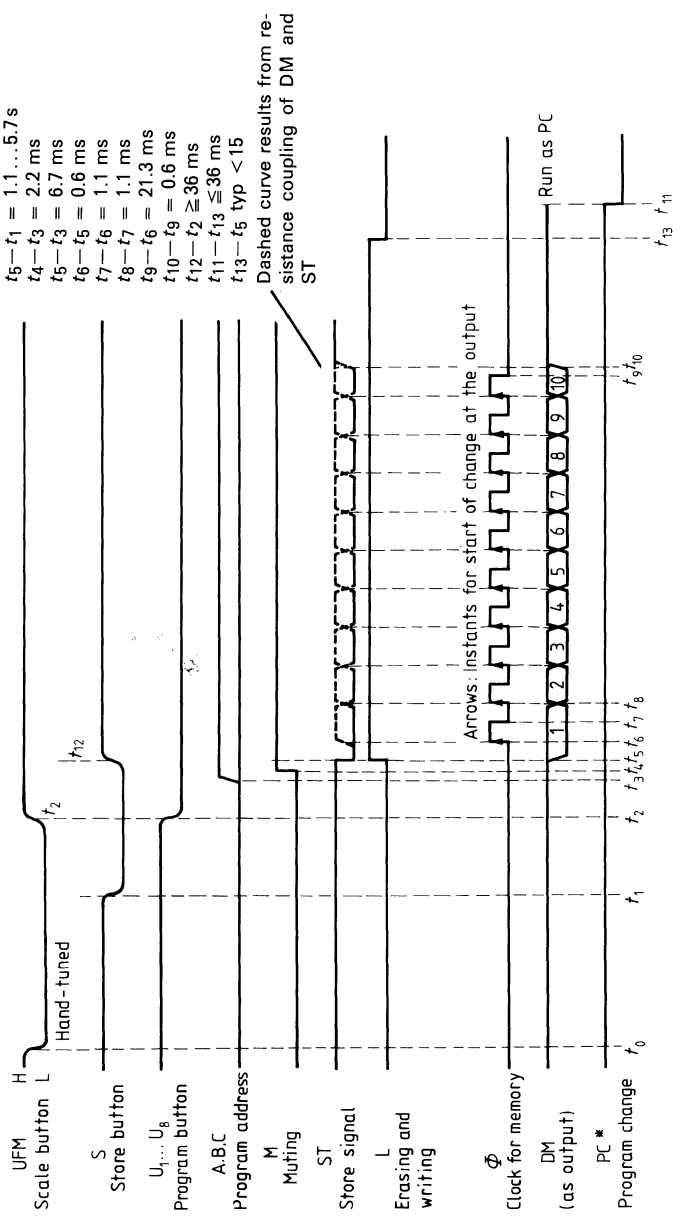


at T_{osc} approx. 455 kHz applies:

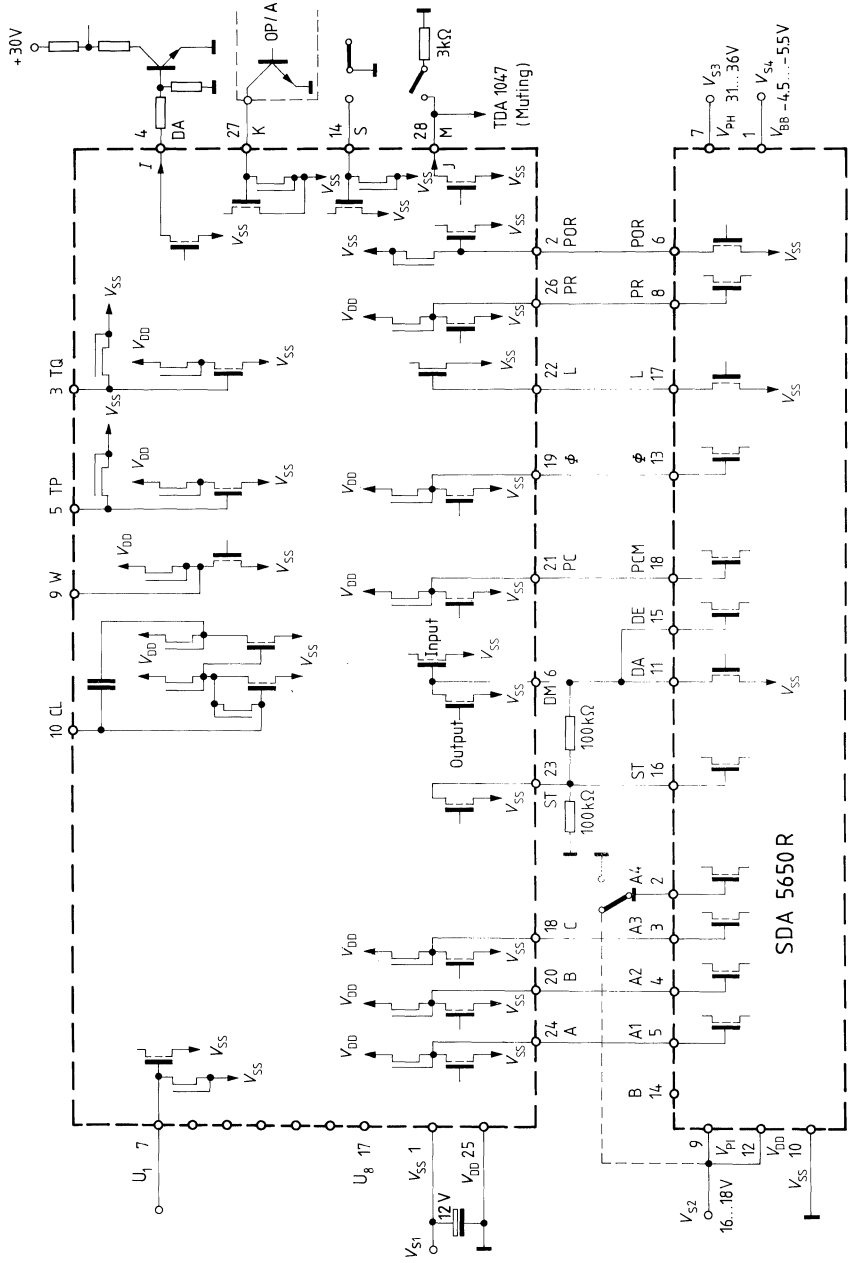
$t_1 - t_0 \equiv$ 2.2...38 ms
$t_2 - t_1 \equiv$ 2.2 ms
$t_3 - t_1 \equiv$ 6.7 ms
$t_4 - t_3 \equiv$ 0.6 ms
$t_5 - t_4 \equiv$ 1.1 ms
$t_6 - t_5 \equiv$ 1.1 ms
$t_7 - t_4 \equiv$ 21.3 ms
$t_8 - t_7 \equiv$ 0.6 ms
$t_9 - t_2 \equiv$ 564.5 ms
$t_0 - t_S \geqq$ 36 ms

Minimum time between opened store button (→H) and pressed program button (→L) after which program change is unambiguously identified. At less than 36 msec, storage or program change can follow.

Storage timing diagram



Graph: Inputs/outputs

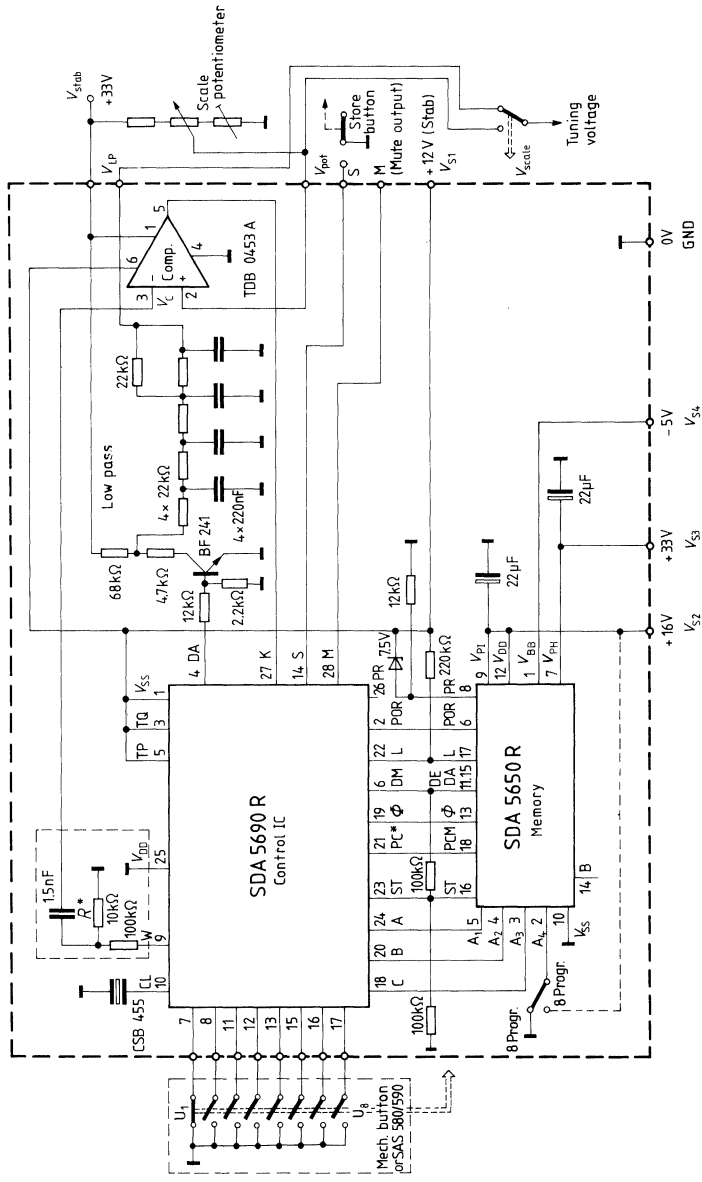


Pin designation

Pin No.	Symbol	Description
1	V_{SS}	Supply voltage
2	POR	Switch-on reset input
3	TQ	Test pin
4	D_q	Information output
5	TP	Test pin
6	DM	Serial data input/output
7	U_1	Program selection signal input
8	U_2	Program selection signal input
9	W	Retrieval signal output
10	CL	Oscillator input/output
11	U_3	Program selection signal input
12	U_4	Program selection signal input
13	U_5	Program selection signal input
14	S	Storage signal input
15	U_6	Program selection signal input
16	U_7	Program selection signal input
17	U_8	Program selection signal input
18	C	Memory location address
19	Φ	Memory shift clock
20	B	Memory location address
21	PC*	Program change signal for memory
22	L	Erase and write blocking signal
23	ST	Store signal for memory
24	A	Memory location address
25	V_{DD}	Supply voltage
26	PR	Switch-on reset signal for memory
27	K	Forward/backward signal (from comp.)/input
28	M	Mute output

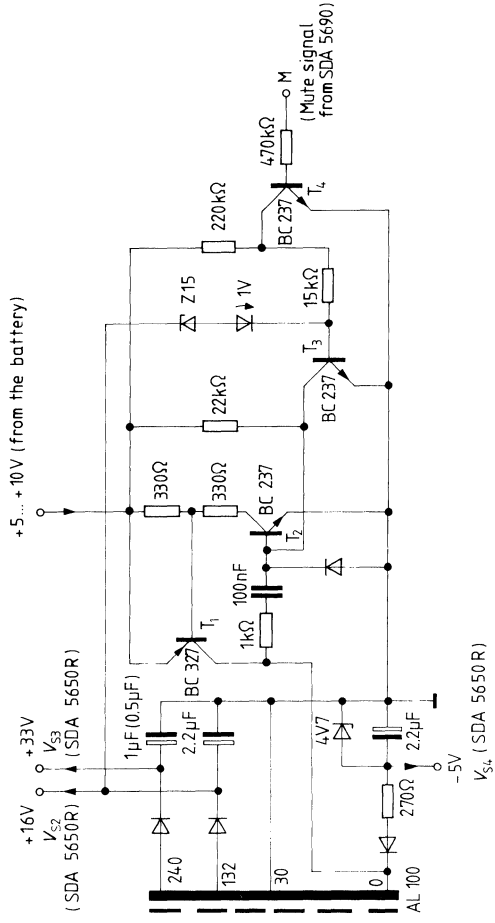
Block diagram

Fully electronic station memory for FM equipment incl. nonvolatile memory



* The width of the window to retrieve the station can be set with the help of *R*.

VHF voltage synthesis for battery equipment
Supply voltage for nonvolatile memory SDA 5650 R



MOS circuit

Digital storing and retrieving of the tuner voltage according to the voltage synthesis concept may be performed by means of the SDA 5690 IC, designed in MOS depletion technology, in connection with a C-MOS memory.
The system comprises 3 ICs, a multistage RC low-pass, and several external components. The tuning voltage is digitized into a 10-bit word, thus obtaining a resolution accuracy of approximately ±10 kHz throughout the entire VHF bandwith.

- Few external components
- Fine-tuning during storage
- Mute signal during program change or storage
- Frequency monitoring of a stored station

Type	Ordering code	Package outline
SDA 5690 C	Q 67100-Z137-C	DIP 28

Maximum ratings (all voltages referred to V_{DD} = 0 V)

Supply voltage	V_{SS}	17	V
Input voltage	V_i	V_{SS}	V
Power dissipation per output (unless otherwise specified under characteristic data)	P_q	10	mV
Total power dissipation	P_{tot}	500	mW
Storage temperature range	T_{stg}	−55 to 125	°C

Range of operation (referred to V_{DD} = 0 V)

Supply voltage range	V_{SS}	5 to 6	V
Ambient temperature range	T_{amb}	0 to 70	°C

Characteristics (all voltages referred to V_{DD}, according to test circuit 1)

		min	typ	max	
Supply current (V_{SS} = 6 V)	I_{DD}		2.5	10	mA
Inputs					
switch-on reset-POR					
forward-backward K					
(incl. pull-high resistors)					
H input voltage (V_{SS} = 5 V)	V_{iH}	4		5	V
L input voltage (V_{SS} = 5 V)	V_{iL}	0		0.5	V
Input short-circuit current (V_{SS} = 6 V)	I_{iL}	−100			µA
Input short-circuit current (V_{SS} = 5 V)	I_{iL}			−10	µA
Inputs					
Store S					
Progr. selection V_1, V_2, V_3,					
V_4, V_5, V_6, V_7, V_8, TP, TQ					
(incl. pull-high resistors)					
H input voltage (V_{SS} = 5 V)	V_{iH}	4		5	V
L input voltage (V_{SS} = 5 V)	V_{iL}	0		0.5	V
Input short-circuit current (V_{SS} = 6 V)	I_{iL}	−50			µA
Input short-circuit current (V_{SS} = 5 V)	I_{iL}			−5	µA
Input DM					
H input voltage (V_{SS} = 5 V)	V_{iH}	4		5	V
L input voltage (V_{SS} = 5 V)	V_{iL}	0		0.5	V
Input oscillator CL	f_{osc}		455*		kHz

* Murata Resonator CSB 455

Characteristics (all voltages referred to V_{DD}, according to test circuit 2)

Outputs		min	typ	max	
Output DM					
(open-drain-output)					
H output voltage ($I_{q\,H} = 100\,\mu A$; $V_{SS} = 5\,V$)	$V_{q\,H}$	4		5	V
Leakage current ($V_{SS} = 6\,V$)	$I_{q\,lk}$			1	µA
Power dissipation	P_q			50	mW
Output Store — ST					
(open-drain-output)					
H-output voltage ($I_{q\,H} = 300\,\mu A$; $V_{SS} = 5\,V$)	$V_{q\,H}$	4		5	V
Leakage current ($V_{SS} = 6\,V$)	$I_{q\,lk}$			1	µA
Power dissipation	P_q			50	mW
Output Mute — M					
(open-drain output, short-circuit proof)					
H output current ($V_{q\,H} = 2.6\,V$; $V_{SS} = 5\,V$)	$I_{q\,H}$	500		1600	µA
Leakage current ($V_{SS} = 6\,V$)	$I_{q\,lk}$			1	µA
Power dissipation	P_q			50	mW
Output DA					
(open-drain output)					
H-output voltage ($I_{q\,H} = 400\,\mu A$; $V_{SS} = 5\,V$)	$V_{q\,H}$	2.4		5	V
Leakage current ($V_{SS} = 6\,V$)	$I_{q\,lk}$			10	µA
Power dissipation	P_q			80	mW
Outputs					
Retrieval W					
memory location address A, B, C					
H-output voltage ($I_{q\,H} = 100\,\mu A$)	$V_{q\,H}$	4		5	V
L-output voltage ($I_{q\,L} = -10\,\mu A$)	$V_{q\,L}$	0		1	V
Output					
Memory shift clock Φ					
H output voltage ($V_{SS} = 5\,V$; $I_{q\,H} = 50\,\mu A$)	$V_{q\,H}$	4		5	V
L output voltage ($I_{q\,L} = -20\,\mu A$)	$V_{q\,L}$	0		1	V
Output					
Program change PC*					
H output voltage ($V_{SS} = 5\,V$; $I_{q\,H} = 100\,\mu A$)	$V_{q\,H}$	4		5	V
L output voltage ($I_{q\,L} = -5\,\mu A$)	$V_{q\,L}$	0		1	V
Transition time ($C_{ext} = 20\,pF$)	t_{HL}			10	µs
Output					
RC time constant for memory					
H output voltage ($V_{SS} = 5\,V$; $I_{q\,H} = 50\,\mu A$)	$V_{q\,H}$	4.5		5	V
L output voltage ($I_{q\,L} = -2.5\,\mu A$)	$V_{q\,L}$	0		0.7	V
Output					
Switch-on reset PR					
H output voltage ($V_{SS} = 5\,V$; $I_{q\,H} = 20\,\mu A$)	$V_{q\,H}$	4		5	V
L output voltage ($I_{q\,L} = -2\,\mu A$; $V_{SS} = 3.3\,V$)	$V_{q\,L}$	0		0.5	V
Changeover values ($V_{SS} - V_{DD}$) (Test diagram)		3.3	3.8	4.5	V

Circuit description

1. Total system — survey

The total system for digital storage and retrieval of the tuning voltage is based on a voltage synthesis concept which comprises three ICs, a multistage *RC* low-pass, and several discrete peripherals. The tuning voltage is digitized into a 10 bit word, thus resulting in a resolution accuracy of approximately ± 10 kHz at 20 MHz bandwidth.

An AFC operates in addition. The reference voltage V_{stab} is generated e.g. by means of a voltage converter.

The SDA 5690 can digitally process max. 8 programs (8×10 bits) to a memory for storing. If a CMOS memory is used, e.g. the MC 144101, 2 mono cells will provide for retaining the information (IFO) after the supply voltage has been switched off.

The PMOS control circuit SDA 5690 C mainly performs a DA conversion in case of program fetch or an AD conversion for program storage. It operates according to a counting method.

The 10-bit digital value is represented as periodic squarewave signal of constant frequency, with the IFO being of the order of the pulse width. The following low-pass filtering yields in the mean time value thus delivering the analog value. The low pass consists of a switching stage in order to generate the voltage swing of 0 to V_{stab} and the passage characteristic for adaptation to the capacitance diode characteristic curve as well as of several RC networks, to minimize the ripple of the analog voltage (< 10 µV).

The comparator TDB 0453 A is necessary for the AD conversion. In case of scale operation (button UFM) the comparator output instructs the control unit to vary the digital value such that the low-pass voltage V_C aims at equality with the scale potentiometer voltage V_{pot}. The converter velocity is designed such that equality can be achieved during transmitter setting and storage. The digital value of V_{pot} can then be stored.

With the aid of the tuning knob and the muting circuit, the frequency of a stored transmitter can be retrieved on the scale.

2. Function of the control IC SDA 5690 C

The converter comprises each a 10-stage cycle counter, a digital comparator and an IFO register which operates either as incrementer/decrementer or as shift register. The periodically circulating cycle counter is clocked by an oscillator of approximately 500 kHz. The digital value equivalent to the tuning voltage is to be found in the IFO register. The conversion into a corresponding pulse width is done such that an F-F is set at the initial position of the cycle counter, and reset when equalization between cycle and incrementer/decrementer is achieved. In accordance with the 2^{10} possible IFO counter positions, there are also 2^{10} different pulse widths. The period of the DA output signal is 4 ms, it is subdivided into 8 individual pulses.

The program button inputs lead to the input logic which recognizes the button pressure and performs binary encoding. A locking device ensures that simultaneous pressure of two buttons does not lead to the recognition of the binary value of a third button. On principle, the last pressed button becomes active. With the aid of the divider and the control logic all clocks necessary for command recognition and data transfer are generated.

2.1. Program change

- press U_1 to U_8
- load the program storage address A, B, C
- transmit the PC* signal and the RC auxiliary signal as read instruction for the memory; the data pin DM is switched as input; DM of the memory as output.
- transmit 10 Φ-clocks; shift the memory IFO in the IFO register.
- convert the IFO into one pulse with
- the filtered diode voltage V_{LP} is fed to the tuner

2.2. Storage

- press the button U_{scale}
- tune with scale potentiometer

  The scale potentiometer voltage V_{pot} is directly fed to the tuner, it is also applied to the analog comparator. The comparator compares the voltage V_C which corresponds to the IFO register level, with V_{pot}. In case of inequality the comparator output determines via pin K in which direction the IFO register, switched as a counter, has to run such that equality will be achieved. The comparator itself does not determine "equality", but only "greater" or "less". For this reason, the digital value cannot be more precise than 1 LSB. At first, the IFO register is provided with a clock frequency of approximately 250 Hz.

  Owing to this higher clock frequency as well as to possible incrementing/decrementing, the low-pass voltage will follow after a reasonable period of time at a change of the scale potentiometer voltage, i.e. there is no waiting period between the finished tuning process and pressing the store button. Because of the high response time of the low pass — given by the severe requirement as to ripple — the counter removes too far from the exact value (approx. $\pm$ 8 steps) when reaching equality of $V_C = V_{pot}$. Therefore, retuning during storage follows.

- Storage process

  At first the store button and subsequently the desired program button are actuated.

  After having actuated the store button, retuning takes place by continuously slowing down the clock frequency during 1 second. After the course of this time, the digital value reaches an accuracy of 1 LSB. Immediately after that, the contents of the IFO register is moved into the memory:
- transmit ST signal and auxiliary RC signal for the memory
- data pin DM is switched as output; by the memory, DM is switched as input
- transmit 10 Φ clocks; shift IFO from the control IC to the memory amd memorize.

  A subsequent program change is performed for control purposes.

2.3. Further particulars

2.3.1. Muting

During program change or storage, the M output is switched to "H". Thus, the sound can be muted during undefined states of the voltages V_{LP}.

2.3.2. Frequency control of a stored transmitter

Ar first, the store button is pressed and kept pressing; "H" appears at M; i.e. the sound becomes quiet. Now the scale potentiometer is turned until the sound is audible again within a narrow range of the scale. This means again that equality between V_{pot} and V_c is given at this spot of the scale; the comparator causes the sound to be switched on with M = "L".

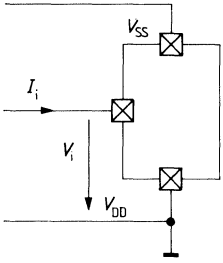
The frequency can be read from the scale.

2.3.3. Switch-on reset

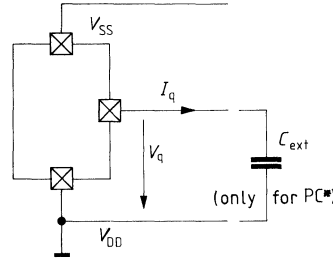
If supply voltage is applied to the device, the input POR will get a signal change from "L" to "H" from the memory. This signal change automatically causes a program change, when a program button is pressed.

Test circuits

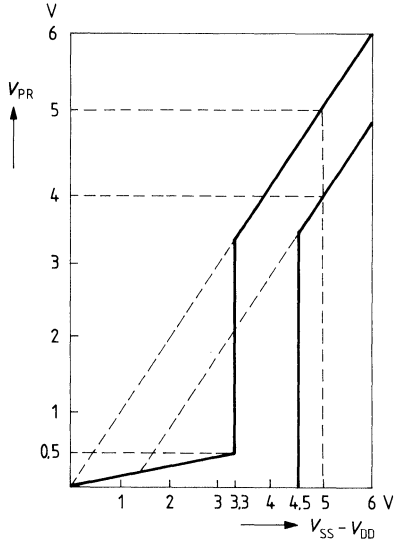
Test circuit 1



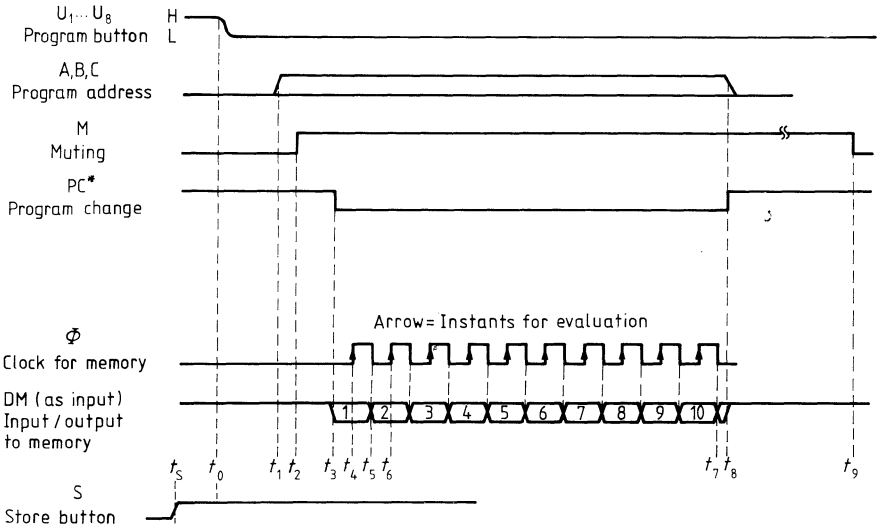
Test circuit 2



Test diagram



Program change timing diagram



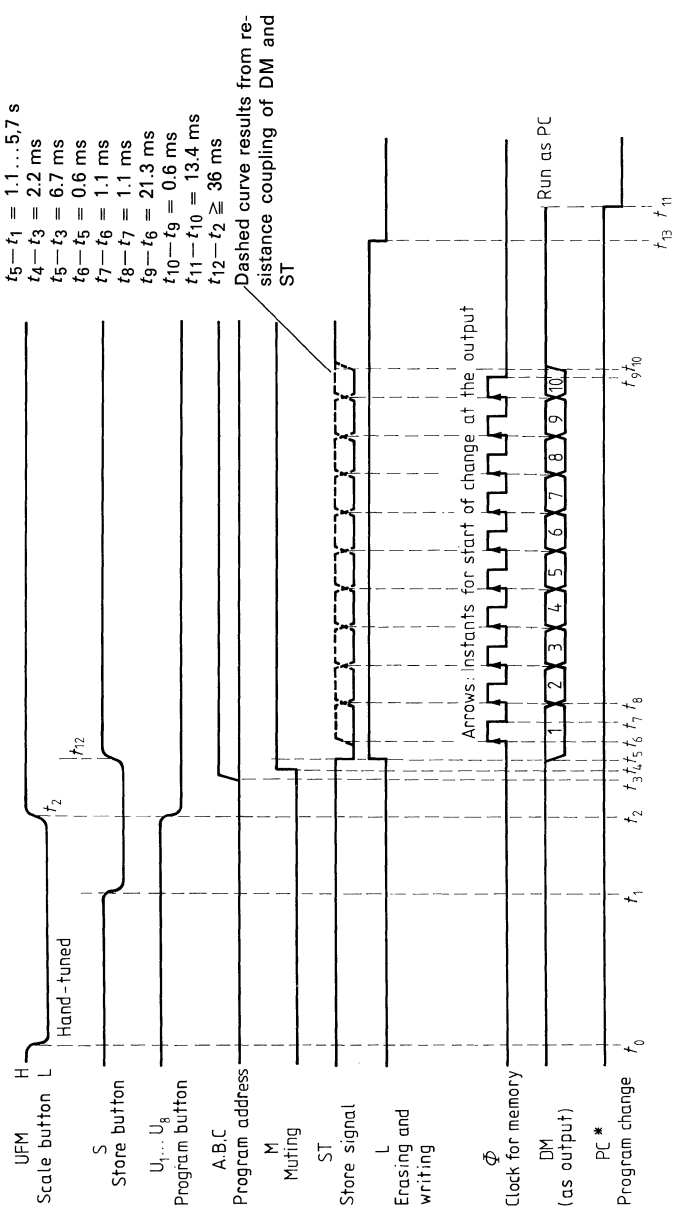
at T_{osc} approx. 455 kHz applies:

$t_1 - t_0$ = 2.2...38 ms
$t_2 - t_1$ = 2.2 ms
$t_3 - t_1$ = 6.7 ms
$t_4 - t_3$ = 0.6 ms
$t_5 - t_4$ = 1.1 ms
$t_6 - t_5$ = 1.1 ms
$t_7 - t_4$ = 21.3 ms
$t_8 - t_7$ = 0.6 ms
$t_9 - t_2$ = 564.5 ms

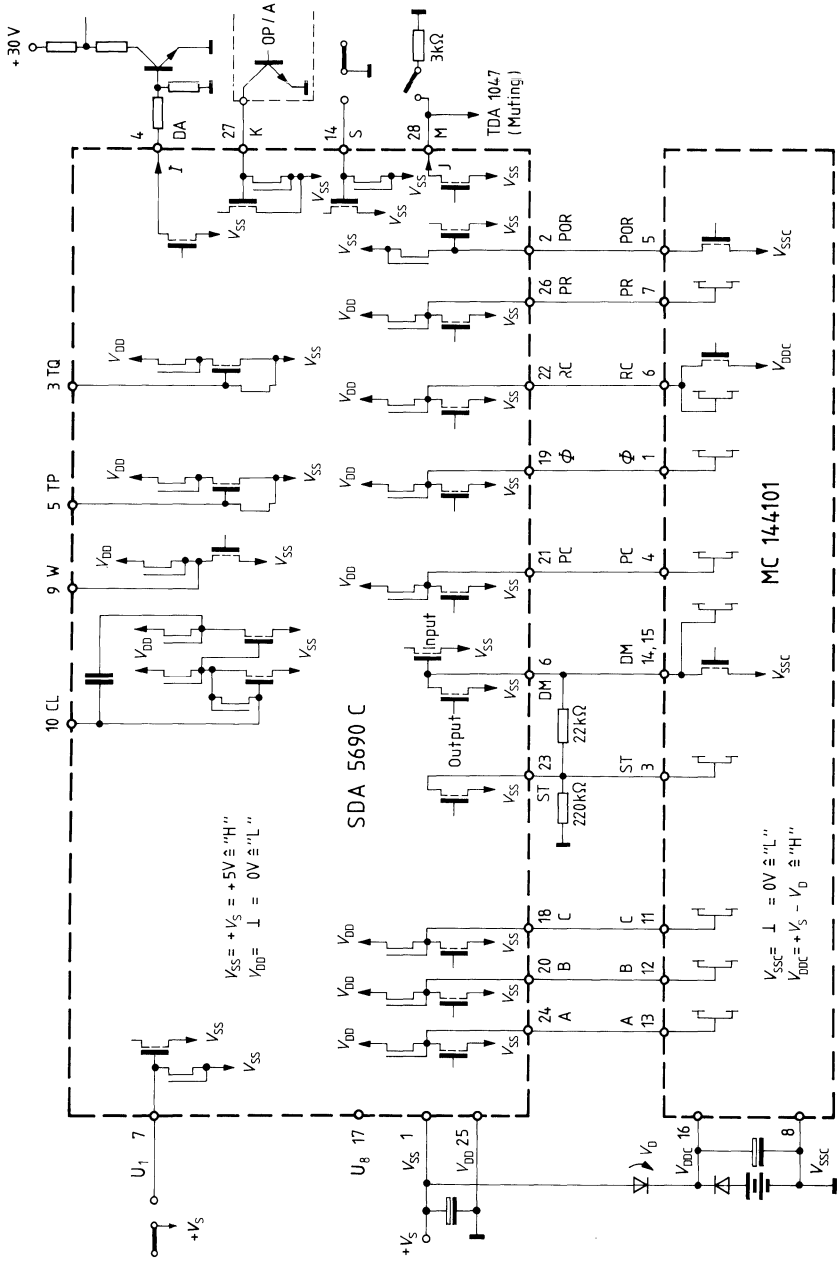
$t_0 - t_s \geqq 36$ ms

Minimum time between opened store button (→H) and pressed program button (→L) after which program change is unambiguously identified. At less than 36 msec, storage or program change can follow.

Storage timing diagram



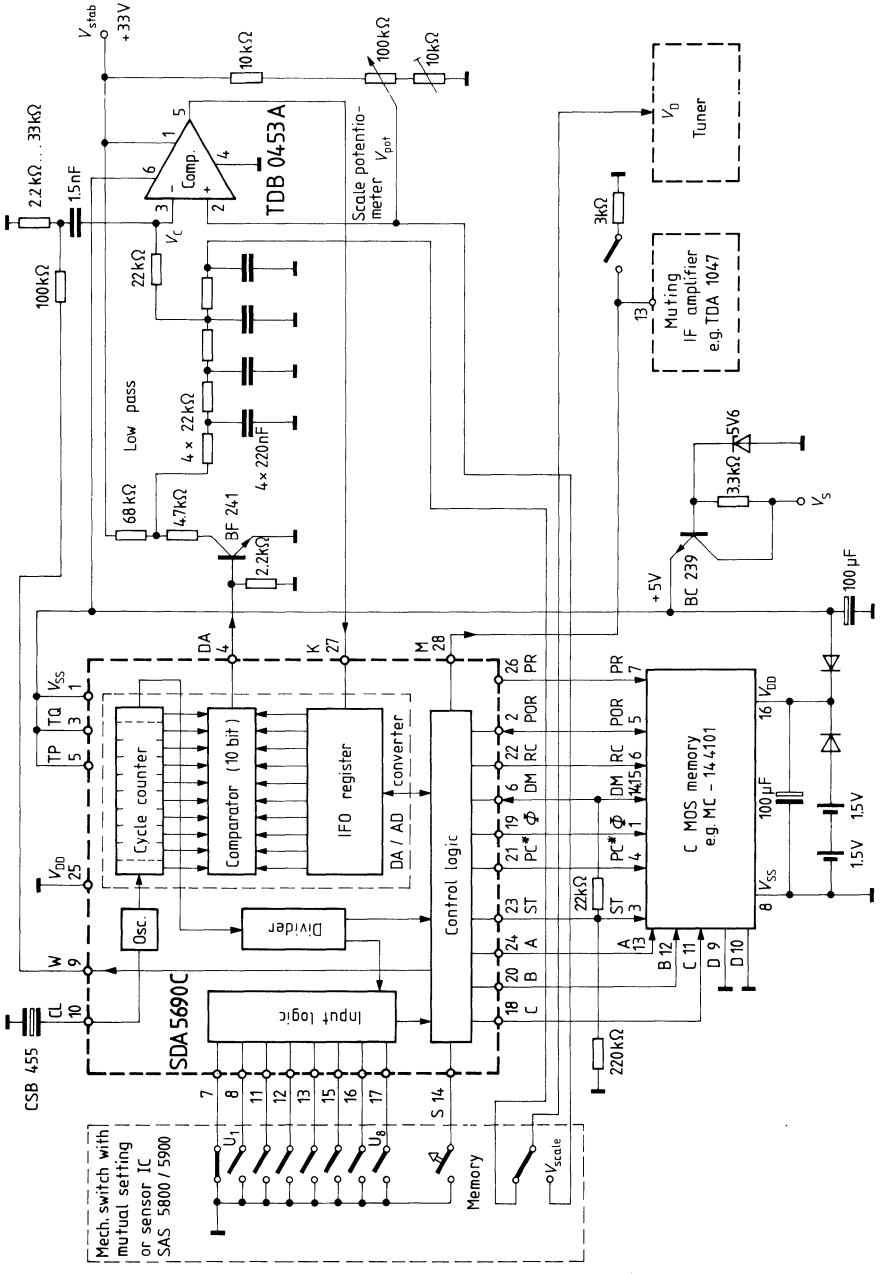
Graph: inputs/outputs



Pin designation

Pin No.	Symbol	Description
1	V_{SS}	Supply voltage
2	POR	Switch-on reset input
3	TQ	Test pin
4	D_q	Information output
5	TP	Test pin
6	DM	Serial data input/output
7	U_1	Program selection signal input
8	U_2	Program selection signal input
9	W	Retrieval signal output
10	CL	Oscillator input/output
11	U_3	Program selection signal input
12	U_4	Program selection signal input
13	U_5	Program selection signal input
14	S	Storage signal input
15	U_6	Program selection signal input
16	U_7	Program selection signal input
17	U_8	Program selection signal input
18	C	Memory location address
19	Φ	Memory shift clock
20	B	Memory location address
21	PC*	Program change signal for memory
22	RC	Time constant simulation signal
23	ST	Store signal for memory
24	A	Memory location address
25	V_{DD}	Supply voltage
26	PR	Switch-on reset signal for memory
27	K	Forward/backward signal (from comp.)/input
28	M	Mute output

Block diagram and application circuit



MOS circuit

16 × 10 (12) bit SDA 5650 R memory for radios.

General features

- Electrically wordwise reprogrammable, nonvolatile memory in floating gate technology
- Memory capacity 16 words of 10 or 12 bits each, pin programmable
- Serial data input and output via separate inputs and outputs
- 4 parallel address input lines
- No determination of erase and write cycles with external RC networks
- N-channel silicon gate technology
- Nonvolatile data storage for more than 10 years
- Unlimited number of read cycles without refresh
  number of rewrite cycles greater than 10^3 per word
- Programmining within 1 second
- Typical application: tuning memory

Type	Ordering code	Package outline
SDA 5650 R	Q67100-Q247-R	DIP 18

Maximum ratings (all voltages referred to V_{SS} = 0 V)

Supply voltage	$V_{DD\ 12\text{-}1}$	21	V
Supply voltage	$V_{PH\ 7\text{-}1}$	40	V
Supply voltage	$V_{PI\ 9\text{-}1}$	21	V
Input voltage	V_i	16	V
Total power dissipation	P_{tot}	400	mW
Thermal resistance (system-air)	$R_{th\ SA}$	80	K/W
Storage temperature range	T_{stg}	−40 to 125	°C

Range of operation (referred to V_{SS} = 0 V)

Supply voltage range	$V_{DD\ 12}$	14 to 16	V
Ambient temperature range	T_{amb}	0 to 70	°C

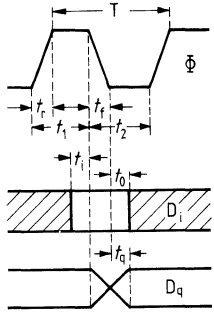
Static characteristics (all voltages referred to V_{SS} = 0 V)

		min	typ	max	
Supply current	$I_{DD\ 12}$		10	20	mA
Substrate bias	$-V_{BB\ 1}$	4		5	V
Substrate current[1])	$-I_{BB\ 1}$			100	µA
Substrate current[2])					
average current	$I_{BB\ 1a}$		0.5	2	mA
peak pulse current	$I_{BB\ 1p}$			10	mA
Programming voltage	$V_{PP\ 7}$		33	35	V
Programming current[1]) (switchable)	$I_{PP\ 7}$			300	µA
Programming current[2])					
average current	$I_{PP\ 7a}$		1	2	mA
peak pulse current	$I_{PP\ 7p}$		5	10	mA
Write voltage	$V_{PI\ 9}$		15	16	V
(> 13 V at the read process)					
Write current[1]) (V_{PI} > 13 V)	$I_{PI\ 9}$			100	µA
Write current[2])					
average current	$I_{PI\ 9a}$		5	20	mA
peak pulse current	$I_{PI\ 9p}$			50	mA
Inputs A_1, A_2, A_3, A_4, D_E, Φ, B, St, PCM, PR	V_L	0		0.5	V
(pin 5, 4, 3, 2, 15, 13, 14, 16, 18, 8)	V_H	4		V_{DD}	V
	I_H			10	µA
B (pin 14) (V_L = 0 V)	$-I_L$			300	µA
PR (pin 8) (V_L = 0 V)	$-I_L$			200	µA
($V_H = V_{DD}$)	$+I_H$			200	µA
Outputs (open drain)					
L, POR, D_A (pin 17, 6, 11)					
(V_0 = 0.5 V)	I_L			0.5	mA
($V_0 = V_{DD}$)	I_H			10	µA

[1]) Quiescent state, read process
[2]) During a reprogramming operation

Dynamic characteristics

		min	typ	max	
Switching times					
Clock signal Φ	$T = t_1 + t_2$	100			µs
	t_1, t_2	20			µs
	t_r, t_f			10	µs
D_i (data input)	t_i	10			µs
D_i (data input)	t_0	70			µs
D_q (data output)	t_q			70	µs
Total erase — write time (V_{PI} = 15 V; V_{PH} = 33 V)*	T_{prog}			1	s
Programming frequency	f_{prog}			1	Hz



[1]) without the portion for data input

Circuit description

Read operation (fig. 1)

The read operation is initialized with the transition of the external signal PCM from high to low at the time $t = t_0$. The address information has to be stable for at least 10 seconds prior to and after t_0. After t_0 + 10 seconds, all address inputs as well as the control input are blocked as long as the PCM signal is low. The data output D_q is low-ohmic as long as PCM remains low. At a time $t_1 > 50$ µsec, the first written data bit of the selected 10 (12) bit word is available at the output. The further data bits are clocked each by the falling edge of 10 (12) positive clock pulses.
After having finished the read operation — with the transition of the external signal PCM from low to high — the address lines and control lines are again enabled.

Rewrite operation (fig. 2)

The write operation is initialized with the transition of the external signal ST from high to low (at least for 50 µsec) at the time $t = t_0$. The address information has to be stable for at least 10 seconds prior to and after t_0. At the time t_0 the memory outputs a signal L from low to high as long as the rewrite operation lasts. This signal blocks the address, the PCM, and the control (ST) input.

After a time $t_1 = t_0 + \Delta t$ with $\Delta t > 50$ µsec the data information can be written into the data shift register with 10 (12) clock pulses. Data carry takes place at the negative edges of the positive clock pulses.

With the aid of internal memory control, the write operation begins as soon as the data transfer after the 10^{th} (12^{th}) clock pulse and the erasure have been finished. The end of the write operation is also determined by means of internal control. It is indicated at the control output L by the transition from high to low.

After programming, the ST input remains blocked, it is not released again before a leading edge at the PCM input (repetitive blocking for programming at too long pressing the store button).

Reset

The memory remains in the reset condition as long as the input PR is low. During reset also the output POR is low.

Word length

A connection between input B and ground V_{SS} results in an extended word length from 10 to 12 bits. In the open state, the shorter word length is set through an integrated pull-up resistor.

Pin designation

Pin No.	Symbol	Description
1	V_{BB}	Substrate bias
2	A_4	Address 4 (input)
3	A_3	Address 3 (input)
4	A_2	Address 2 (input)
5	A_1	Address 1 (input)
6	POR	Reset output
7	V_{PP}	Programming voltage
8	PR	Reset input
9	V_{PI}	Write current
10	V_{SS}	Ground
11	D_q	Data output
12	V_{DD}	Supply voltage
13	Φ	Clock signal (input)
14	B	Changeover between 10 and 12 bit (input)
15	D_i	Data input
16	St	Reprogramming signal (input, active low)
17	L	Programming conditional signal (output)
18	PCM	Read signal (input, active low)

Fig. 1 Read operation

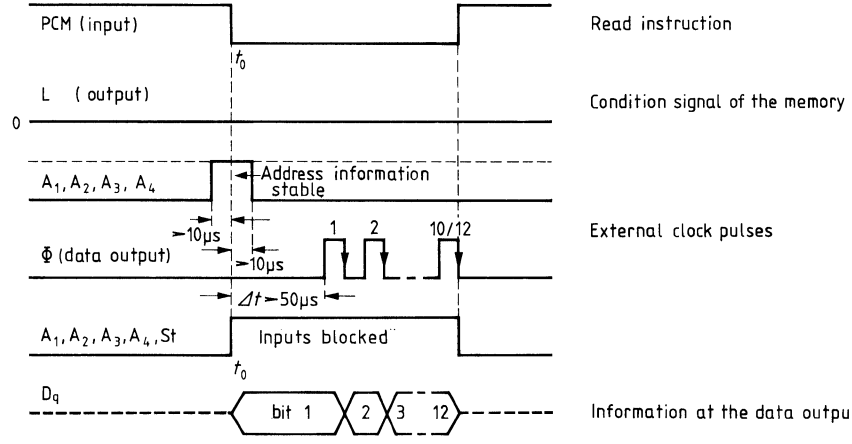
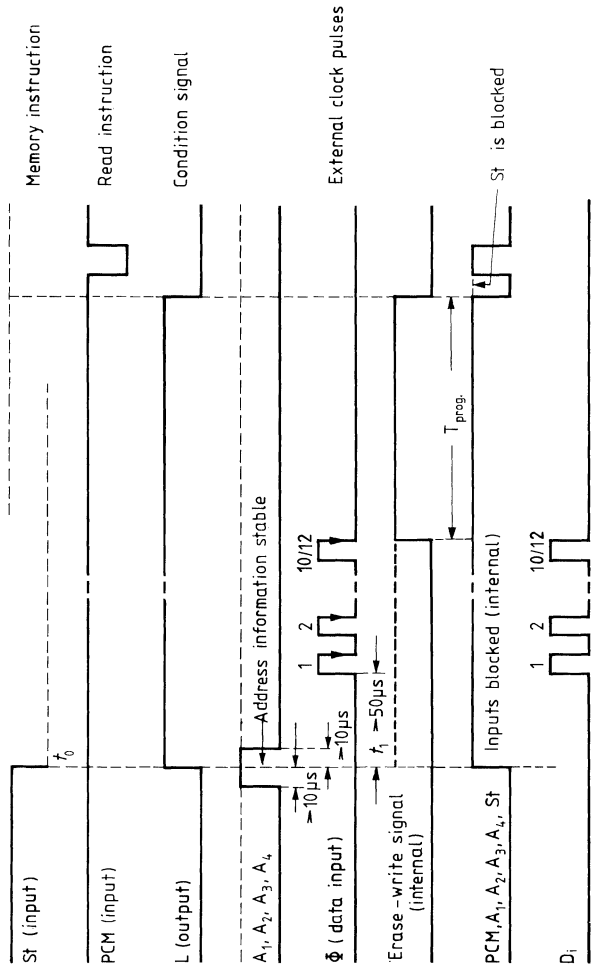
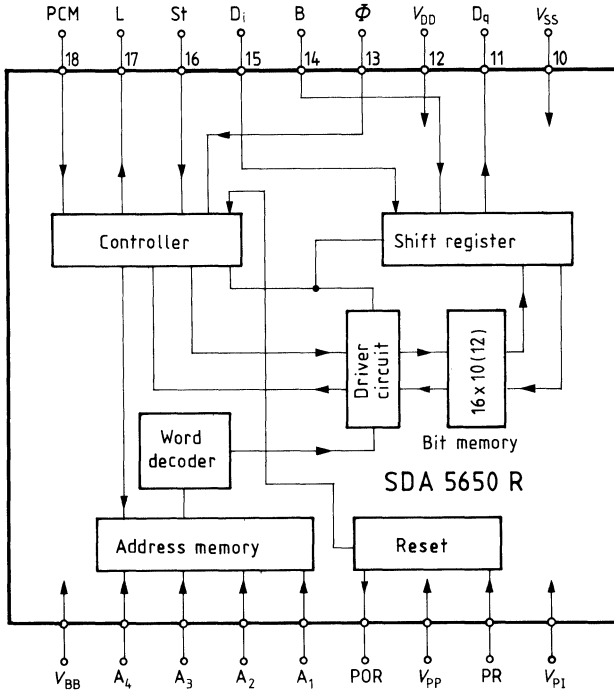


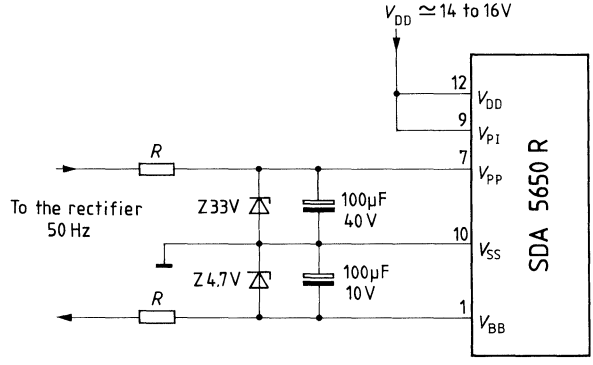
Fig. 2 Erase-write operation



Block diagram



Supply voltage for the tuning memory in radios



Bipolar circuit

The comparator TDB 0453 A is particularly developed for use in the voltage synthesis concept for radios (SDA 5690).
The TDB 0453 A includes a PNP input. The prestages and final stages can be supplied separately. Thus, the advantage results that comparatively low battery voltages are adequate for supplying the final stages and a very low current is needed for supplying the input stages. The supply voltage V_{S1} must be slightly higher than the required common-mode range; moreover, current consumption I_{S1} of the prestage only slightly changes at switching over the final stage. In addition to this advantage as well as high gain, high input impedance, low zero voltage, low temperature and supply voltage dependence, the TDB 0453 A is outstanding for:

- Large supply voltage range
- High output power
- Low current consumption
- Low saturation voltage
- Common mode range up to 0 V

Type	Ordering code	Package outline
TDB 0453 A	Q 67000-A1499	DIP 6

Maximum ratings

Supply voltage	V_{S1}, V_{S2}	32	V
Output current	$I_{q\,5}$	70	mA
Differential input voltage	$\Delta V_{i\,2-3}$	$\pm V_S$	
Thermal resistance (system-air)	$R_{th\,SA}$	140	K/W
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−55 to 125	°C

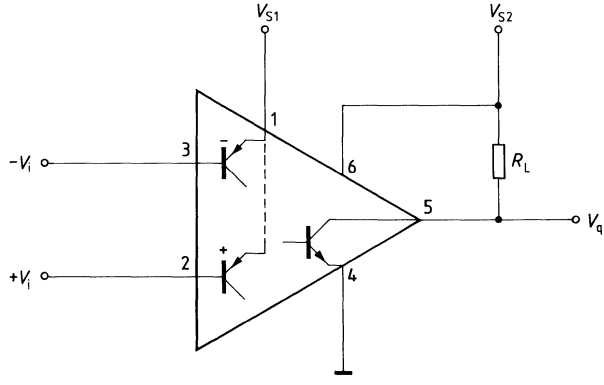
Range of operation

Supply voltage range	V_{S1}, V_{S2}	3 to 32	V
Ambient temperature range	T_{amb}	0 to 70	°C

Characteristics (V_S = 30 V; T_{amb} = 25 °C, R_L = 10 kΩ, unless otherwise specified)

		min	typ	max	
Current consumption Pin 1	I_{S1}		0.25	0.30	mA
V_{S1} = 30 V, V_{S2} = 15 V } Pin 6	I_{S2}		0.7	1	mA
Input offset voltage (R_G = 50 Ω)	ΔV_{ios}	−7.5		+7.5	mV
Input offset current	ΔI_{ios}			80	nA
Input current	I_i		50	150	nA
Output voltage R_L = 2 kΩ	V_q	29.9			V
R_L = 620 Ω	V_q	29.9			V
Output leakage current R_L = 2 kΩ	V_q			0.3	V
R_L = 620 Ω	V_q			0.5	V
Input resistance	R_i		200		kΩ
Open-loop voltage gain	G_{vo}	75	83	95	dB
Output reverse current	I_{qR}		1	10	μA
Input common mode range	$V_{i\,G}$	−0.2		V_S − 2.0	V
Common mode rejection	CMR	65	79		dB
Supply voltage rejection	$\frac{\Delta V_{ios}}{\Delta V_S}$		25	200	μV/V
Temperature coefficient of input offset voltage	TC_V		6		μV/K
Temperature coefficient of input offset current	TC_I		0.3		nA/K
Rate of voltage rise	$\Delta V_q/\Delta t_r$	depending on the mode of operation and wiring (typ. < 9 V/μs)			

Schematic diagram



Frequency Counter for LMS und VHF

SDA 5680 A
SDA 5680 B

Bipolar circuit

SDA 5680 is a single-chip solution of a frequency counter for radio receivers. The display is provided by a 5 digit liquid crystal display in multiplex operation. The SDA 5680 is suitable for use in single as well as in multi-heterodyne receivers. Two versions of the SDA 5680 are available differing by their intermediate frequency.

- Single chip solution
- Direct LCD driving
- For all broadcasting ranges
- Low current consumption

Type	Ordering code	Package outline
SDA 5680 A	Q 67000-Y 505-A	DIP 28
SDA 5680 B	Q 67000-Y 505-B	

Maximum ratings

Supply voltage	V_S	6.5	V
Input voltage	$V_{i\,6}$, $V_{i\,7}$, $V_{i\,9}$	V_S	V
	$V_{i\,2}$, $V_{i\,4}$, $V_{i\,5}$*	1.5	V_{rms}
Thermal resistance (system-air)	$R_{th\ SA}$	60	K/W
Junction temperature	T_j	125	°C
Storage temperature range	T_{stg}	−40 to 125	°C

Range of operation

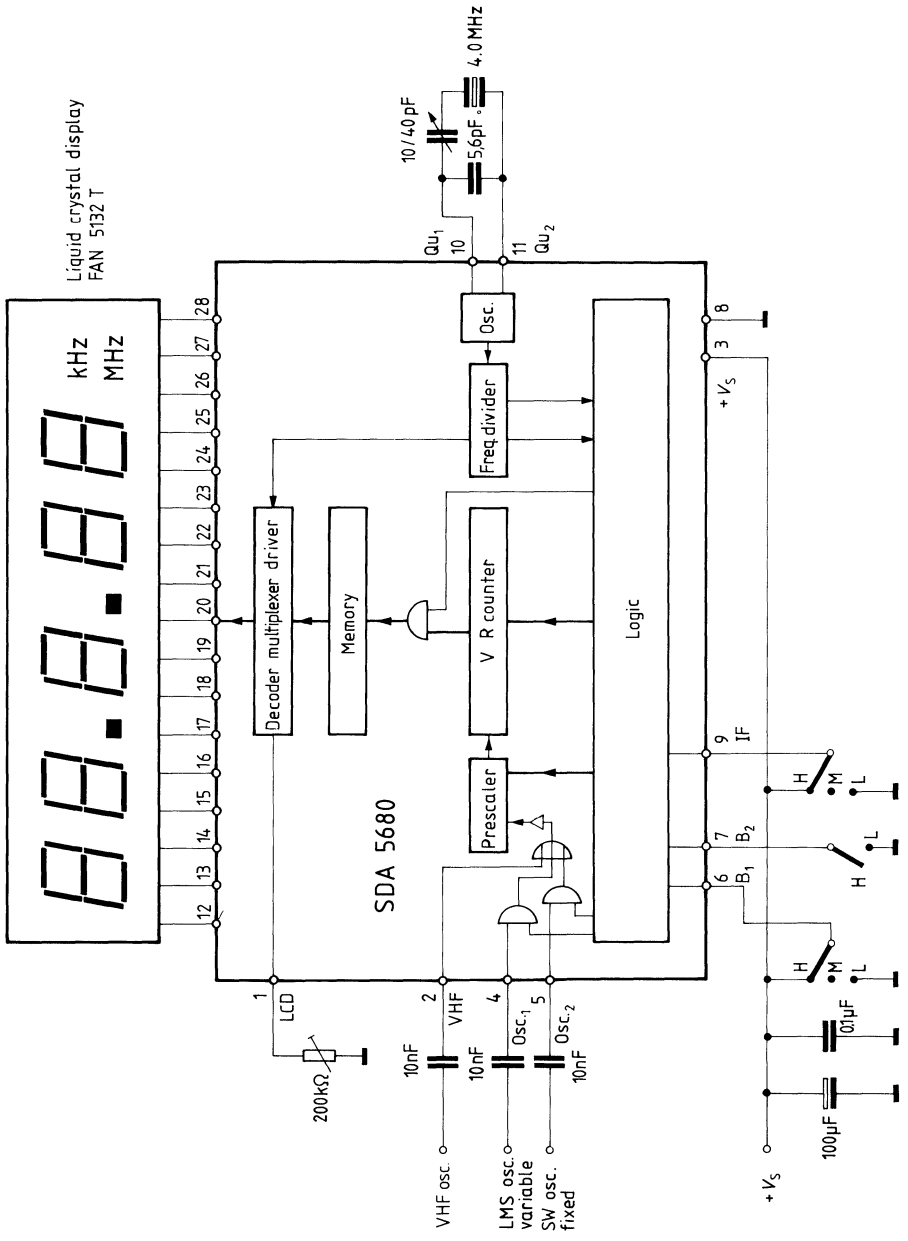
Supply voltage range	V_S	4.7 to 6	V
Ambient temperature range	T_{amb}	0 to 70	°C

* no ext. dc voltage

Characteristics (V_S = 5 V; T_{amb} = 25 °C)

		min	typ	max	
Current consumption	I_3		30		mA
Input voltage 590 kHz ≤ f ≤ 1 MHz	$V_{i\,2}$, $V_{i\,4}$, $V_{i\,5}$	150			mV_{rms}
1 MHz ≤ f ≤ 2 MHz		80			mV_{rms}
f > 2 MHz		40			mV_{rms}
Input resistance	$R_{i\,2}$	250			Ω
	$R_{i\,4}$	1			kΩ
	$R_{i\,5}$	1			kΩ
H-input voltage	$V_{i\,6H}$	2.4			V
	$V_{i\,7H}$	2.4			V
	$V_{i\,9H}$	2.4			V
M-input voltage (tristate inputs)	$V_{i\,6M}$		1		V
	$V_{i\,9M}$		1		V
			or free		
L-input voltage	$V_{i\,6L}$			0.2	V
	$V_{i\,7L}$			0.2	V
	$V_{i\,9L}$			0.2	V
H-input current	$I_{i\,6H}$			100	µA
($V_{i\,6H}$ = $V_{i\,7H}$ = $V_{i\,9H}$ ≤ 2.4 V)	$I_{i\,7H}$			100	µA
	$I_{i\,9H}$			100	µA
L-input current	$I_{i\,6L}$			−300	µA
	$I_{i\,7L}$			−300	µA
	$I_{i\,9L}$			−300	µA
Input frequency	$f_{i\,2}$	0.59		119	MHz
	$f_{i\,4}$	0.59		33	MHz
	$f_{i\,5}$	0.59		33	MHz

Block diagram and application circuit



Circuit description

(refer to block diagram)

The heterodyne principle is used in radio receivers in different variants. Types of different center frequencies are applied as IF filter.

In case of single heterodyning the inputs osc_1 and VHF of the IC are connected; in case of double heterodyning the inputs osc_1, osc_2, and VHF. Two inputs are provided for the logic selection of osc_1, osc_2, or VHF. One input permits the IF frequencies of MS and VHF to be programmed.

The receiver frequency f_{rec} can be derived from the equation

$$f_{rec} = f_{i1} \pm f_{i2} \pm f_{IF}$$

An incrementer/decrementer and a gate circuit (using a crystal as time base) are used for processing the frequencies f_{i1} and f_{i2}.

The frequency f_{i2} can be zero, f_{i1} then corresponds to the oscillator frequency of LMS or VHF. The programmed result of the counter takes the frequency f_{IF} into account when the counting operation starts. The crystal frequency amounts to 4 MHz.

Frequency processing in the IC

LMS/VHF_{single} : $f_{rec} = f_{i1} - f_{IF}$
SW_{double} : $f_{rec} = f_{i1} - f_{i2} + f_{IF}$

Band selection

B_1	B_2	active inputs	Function
L		Osc_1	LM
M	L	Osc_1	SW_{single} heterodyned
M	H	Osc_1, Osc_2	SW_{double} heterodyned
H		VHF	VHF

Input B_1 is not connected M
Input B_2 is not connected H

IF programming:

The SDA 5680 is available in two versions; they differ by their mask programming throughout the intermediate frequency range:

SDA 5680 A : LMS: f_{IF} = 460 kHz
VHF: f_{IF} = 10.7 MHz

SDA 5680 B : LMS: f_{IF} = 452 kHz
VHF: f_{IF} = 10.7 MHz

IF Pin 9	Type A LMS	VHF	Type B LMS	VHF
L	459 kHz	10.675 MHz	451 kHz	10.675 MHz
M	460 kHz	10.7 MHz	452 kHz	10.7 MHz
H	461 kHz	10.725 MHz	453 kHz	10.725 MHz

Display:

Display range:

VHF:	108.00 MHz	(max. of range)
SW:	30.00 MHz	
MF:	1605 kHz	
LF:	285 kHz	

Indicating accuracy: clock accuracy ± 1 digit.
Leading 0 gated.

At the LCD input the voltage can be varied at the outputs D_{12} to D_{28} by means of a resistance to ground and matched to possible specimen deviation of the LCDs.

Pin designation

Pin No.	Symbol	Description
1	LCD	LCD voltage setting
2	VHF	VHF oscillator
3	$+V_S$	Supply voltage
4	$Osc._1$	LMS oscillator, variable
5	$Osc._2$	SW oscillator, fixed
6	B_1	Area selection
7	B_2	Single/double heterodyning
8	GND	Ground
9	IF	IF programming
10	Qu_1	Crystal pin 1
11	Qu_2	Crystol pin 2
12	com_1	LCD connection
13	com_2	LCD connection
14	com_3	LCD connection
15	FED_1	LCD connection
16	AG_1	LCD connection
17	BC_1	LCD connection
18	FED_2	LCD connection
19	AG_2	LCD connection
20	BC_2P_1	LCD connection
21	AFE_3	LCD connection
22	BGD_3	LCD connection
23	$F_4C_3P_2$	LCD connection
24	AGE_4	LCD connection
25	BCD_4	LCD connection
26	FED_5	LCD connection
27	AGC_5	LCD connection
28	B_5, kHz, MHz	LCD connection

Bipolar circuit

The TCA 4500 A is a phase-locked loop stereo decoder which incorporates a variable channel separation control. In this IC, the sensitivity to the third harmonics of both the pilot and subcarrier frequencies has been eliminated thanks to the use of appropriate, digitally generated waveforms in the phase-locked loop and decoder sections.

- Low distortion
- Excellent rejection of ARI subcarrier and pilottone harmonics
- No need for coils

Type	Ordering code	Package outline
TCA 4500 A	Q 67000-A 1471	DIP 16

Maximum ratings

Supply voltage	V_S	16	V
Lamp drive voltage (lamp off)	V_7	30	V
Lamp current	I_7	100	mA
Channel separation control voltage	V_{11}	10	V
Thermal resistance (system-air)	$R_{th\ SA}$	90	K/W
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C

Range of operation

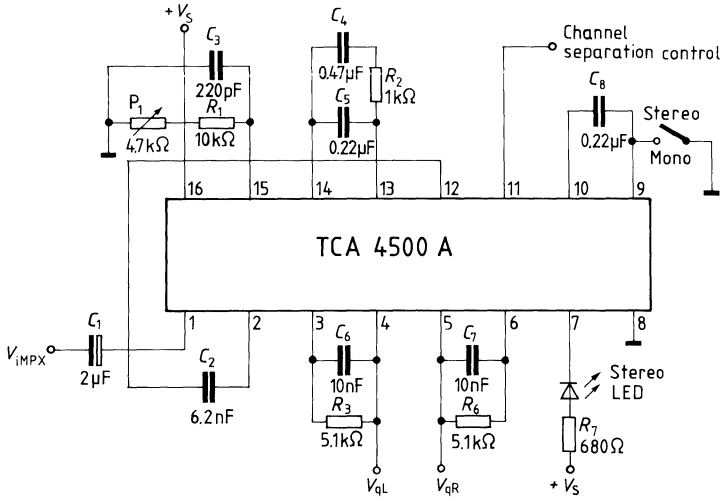
Supply voltage range	V_S	8 to 16	V
Ambient temperature range	T_{amb}	−25 to 85	°C

Characteristics

(V_S = 12 V; T_{amb} = 25 °C; $V_{i\,(MPX)}$ = 2.5 V_{SS}; f_{mod} = 1 kHz; V_{pilot} = 10% V_i)

		min	typ	max	
Current consumption (I_7 = 0)	I_{16}		35		mA
Stereo channel separation					
unadjusted	a	30			dB
optimized on other channel	a_{opt}	40			dB
Monaural voltage gain	G	0.8	1	1.2	
THD at 2.5 V_{pp}	*THD*			0.3	%
THD at 1.5 V_{pp}	*THD*		0.2		%
Signal to noise ratio in acc. with DIN 45405	$a_{S/N}$		85		dB
quasi peak reading RMS 20 Hz — 15 kHz	$a_{S/N}$		90		dB
Frequency rejection 19 kHz	a		31		dB
38 kHz	a		50		dB
Pilot tone harmonic rejection 57 kHz ARI	a		60		dB
Subcarrier harmonic rejection 76 kHz	a		45		dB
114 kHz	a		50		dB
152 kHz	a		50		dB
Input voltage for stereo switching threshold (19 kHz input signal for lamp "on")	$V_{i\,1}$	12	16	20	mV_{rms}
Hysteresis for stereo switching threshold	H		6		dB
Quiescent output voltage change with mono/stereo switching	ΔV_{ql}, ΔV_{qr}		5	20	mV
Channel separation control voltage					
3 dB separation	V_{11}		0.7		V
30 dB separation	V_{11}		1.7		V
Minimum channel separation (V_{11} = 0 V)	a			1	dB
Monaural channel inbalance (pilottone off)	$\Delta V_{ql,r}$			0.3	dB
Hum suppression	a_{hum}		55		dB
Input resistance	$R_{i\,1}$		50		kΩ
Output resistance	$R_{q\,4}$, $R_{q\,5}$		100		Ω
Channel separation control current	I_{11}			−300	µA
Catching range	$\Delta f/f_0$		±5		%

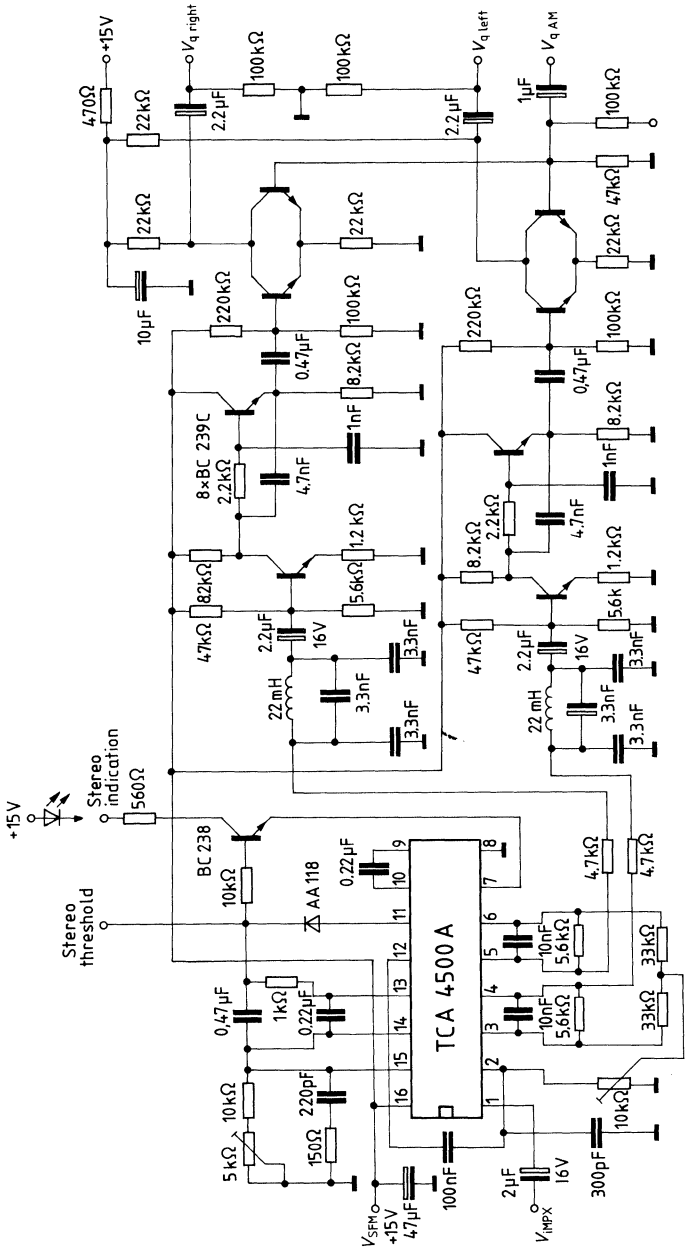
Test circuit



Pin designation

Pin No.	Description
1	Input
2	Preamplifier output
3	Left amplifier input
4	Left channel output
5	Right channel output
6	Right amplifier input
7	Stereo indicator lamp
8	Ground
9	Switching threshold
10	Switching threshold
11	19 kHz output/channel separation control
12	Modulator input
13	Loop filter
14	Loop filter
15	Oscillator RC network
16	Supply voltage + V_S

Application circuit with low-pass filter



Bipolar circuit

The TCA 4510 decodes the transmitter-side stereo information in both L and R channels. Stereo transmission is shown by means of an indicator lamp. Continuous blending of mono and stereo signals is possible. The switching frequencies are controlled by a phase-locked loop.

- Good channel separation
- No need for coils
- Controllable channel separation
- Good rejection of ARI subcarrier and pilottone harmonics

Type	Ordering code	Package outline
TCA 4510	Q 67000-A 1533	DIP 18

Maximum ratings

Supply voltage	V_S	18	V
Lamp voltage	V_{LP}	18	V
Current for stereo indication lamp	I_{LP}	60	mA
Thermal resistance (system-air)	$R_{th\ SA}$	70	K/W
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C

Range of operation

Supply voltage range	V_S	4.5 to 18	V
Ambient temperature range	T_{amb}	−25 to 85	°C

Characteristics (V_S = 8 V; T_{amb} = 25 °C)

		min	typ	max	
Total current without I_{LP} (S_1 closed)	I_S		10	15	mA
Total current without I_{LP} (S_1 open)	I_S		6	8	mA
MPX op amp output voltage	V_{14}	700	900		mV_{pp}
Output voltage 1 kHz (stereo) (for modul. output, V_i = 700 mV_{pp})	V_q	700	900	1100	mV_{pp}
Output voltage 1 kHz (mono) (L or R modul., V_i = 700 mV_{pp})	V_q	350	450	550	mV_{pp}
Input resistance	R_i	90	100		kΩ
Output resistance	R_q		1.5	2	kΩ
Cross-talk attenuation (f_{AF} = 1 kHz; V_H > 0.8 V)	a_{cr}		40		dB
19 kHz reduction V_i = 700 mV_{pp} (test circuit 1)	a_{19}		32		dB
19 kHz reduction V_i = 700 mV_{pp} (test circuit 2)	a_{19}		30		dB
38 kHz reduction V_i = 700 mV_{pp} (test circuit 1)	a_{38}		40		dB
38 kHz reduction V_i = 700 mV_{pp} (test circuit 2)	a_{38}		30		dB
57 kHz reduction V_i = 700 mV_{pp} (test circuit 1)	a_{57}		45		dB
57 kHz reduction V_i = 700 mV_{pp} (test circuit 2)	a_{57}		37		dB
76 kHz reduction V_i = 700 mV_{pp} (test circuit 1)	a_{76}		40		dB
76 kHz reduction V_i = 700 mV_{pp} (test circuit 2)	a_{76}		20		dB
Oscillator switch-off (S_1 open)	V_{LP}			0.4	V
Oscillator functions (S_1 closed)	V_{LP}	0.9			V
Oscillator function (I_{LP} = 10 mA)	V_{LP}	0.9			V
Mono a_{cr} = 6 dB (f_{AF} = 1 kHz)	V_H			0.5	V
Stereo a_{cr} = 40 dB (f_{AF} = 1 kHz)	V_H		0.8	0.9	V
Threshold stereo on (S_1 closed)	$V_{i\,PT}$		30		mV_{pp}
Threshold stereo off (S_1 closed)	$V_{i\,PT}$		15		mV_{pp}
Switch-over to mono	V_S		4.8	5	V
Lamp current	I_{LP}	10	35	50	mA
Oscillator basic frequency	f_{osc}		19		kHz
Catching range	f_C		±1		kHz
Channel balance (S_1 open; V_H = 0 V)	B			0.5	dB
Signal-to-noise ratio (RMS 20 Hz—15 Hz)	S/N	60			dB
Total harmonic distortion					
V_q = 700 mV_{pp}; f_{AF} = 1 kHz (test circuit 1)	THD			0.5	%
V_q = 900 mV_{pp}; f_{AF} = 1 kHz (test circuit 2)	THD			0.5	%

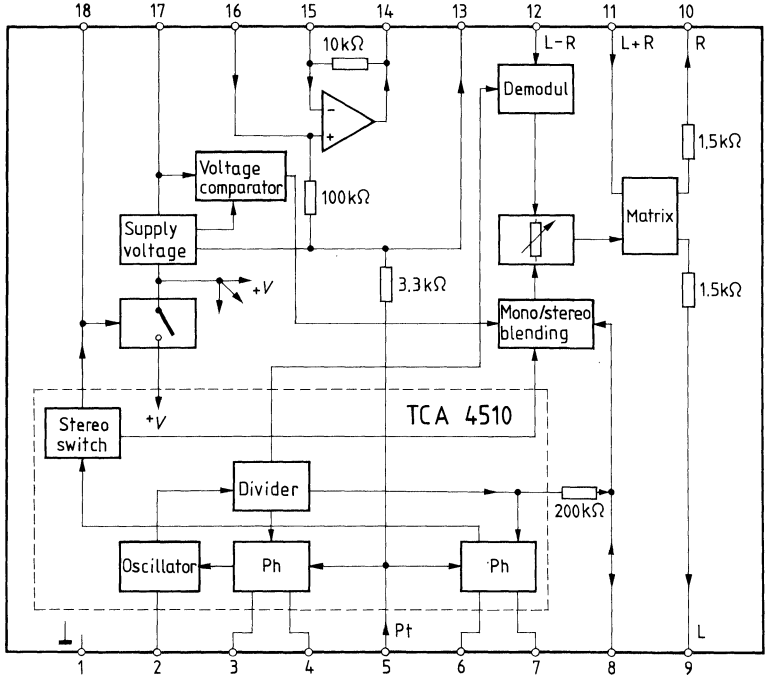
Circuit description

The TCA 4510 is especially intended for battery operation. The IC can be used in time multiplex (switching) or in frequency multiplex (matrix) mode of operation. The necessary signal separation can be achieved by means of de-emphasis, the (L—R) signals are de-emphasized prior to their demodulation.

Amplitude and phase of the MPX input signal can be corrected by an operational amplifier. For this purpose an RC circuit is connected at pin 15. In matrix mode of operation, separation of (L+R) and (L−R) signals is achieved through an attenuated tuning circuit. In case of switching mode of operation, this separation is not required.

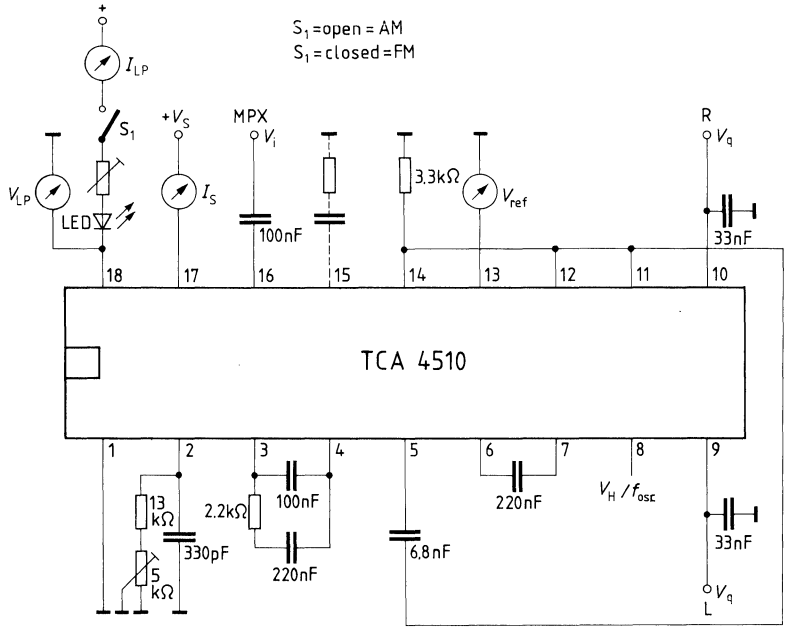
The (L−R) signal is demodulated and can be attenuated by means of an auxiliary voltage V_H or by a lower supply voltage (V_S <5 V).
The matrix generates the output signal by adding the (L+R) signal according to the formula (L+R) ± (L−R) = 2 L or 2 R, respectively. Only in case of switching mode of operation, the necessary de-emphasis is provided by output capacitors. The frequency required for demodulating the (L—R) signal is obtained by a phase-locked loop (PLL) from the divider. The oscillator is synchronized to the pilottone applied to pin 5 by means of phase comparison. A further phase comparison issues the information mono or stereo. Thus, the indicator lamp is switched and indicates as soon as a signal of adequate strength is available at the input. Moreover, the (L—R) attenuation has also been eliminated. If the switch S_1 is open, the IC switches the oscillator off, thus suppressing the (L—R) signal via the stereo switch and the mono/stereo blending. The supply current is thus reduced. If pin 8 is disconnected, the oscillator frequency can be measured

Block diagram



Test circuit 1

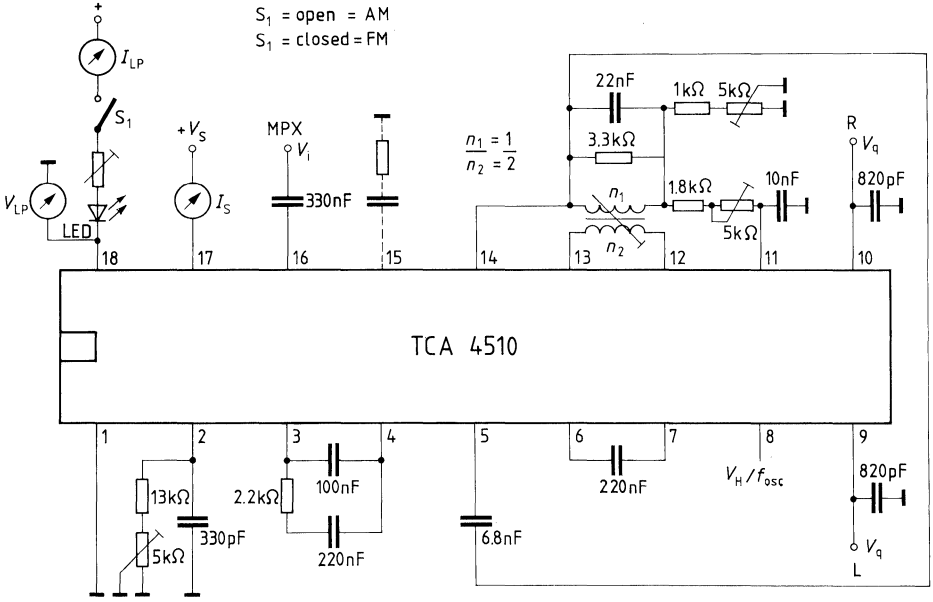
Switching mode of operation



V_i = (L+R) + $(L-R)_{HT}$ + PT
L = 100%; R = 0% or
R = 100%; L = 0%

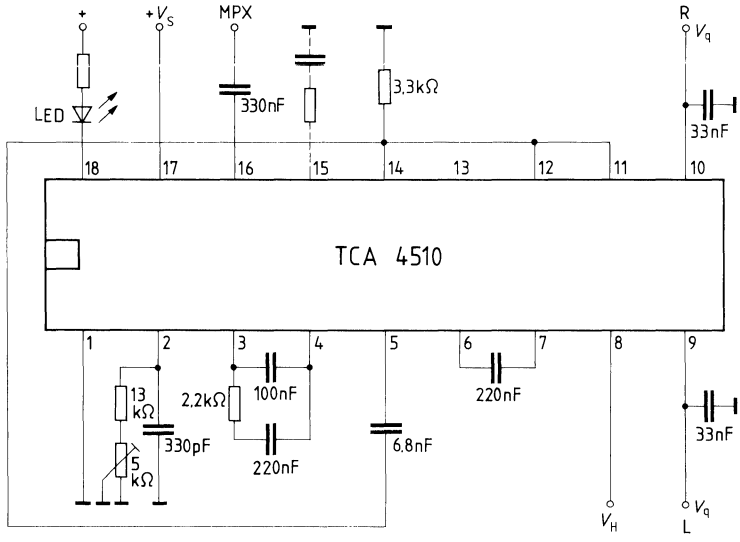
Test circuit 2

Matrix mode of operation



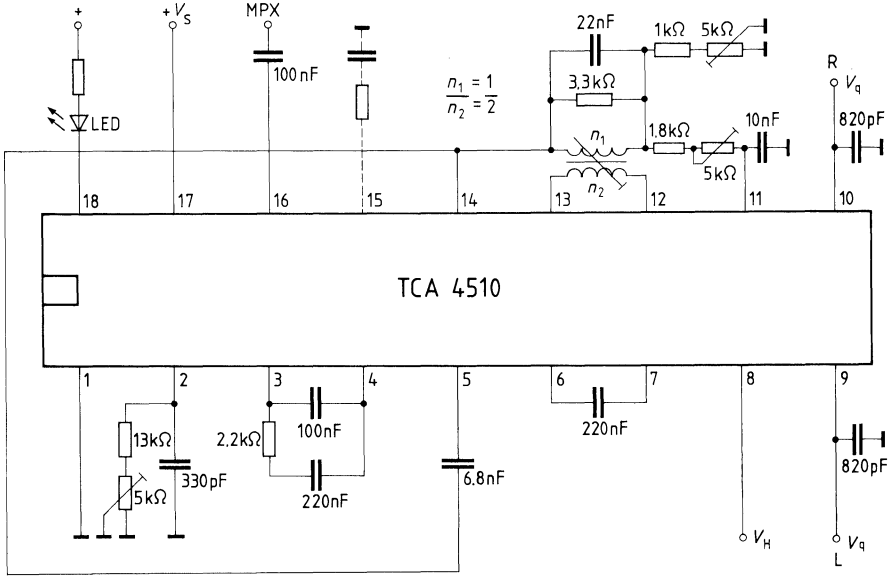
Application circuit 1

Switching mode of operation



Application circuit 2

Matrix mode of operation



Bipolar circuit

The S 0282-2 is intended for automatic control and for indication of the reception level in stereo tape recorders and cassette recorders.

- Wide input voltage range
- Good synchronization
- Covering all signal portions

Type	Ordering code	Package outline
S 0282-2	Q67000-A1115-2	DIP 18

Maximum ratings

Supply voltage	$V_{S\,18}$	36	V
Voltages			
Control reference point	V_2	10	V
Control current output	V_3	10	V
Display output	V_4, V_{15}	10	V
Instrument driver	V_5, V_{14}	10	V
Preamplifier output	$V_{q\,6}$, $V_{q\,13}$	10	V
Feedback input	$V_{i\,7}$, $V_{i\,12}$	10	V
Preamplifier input	$V_{i\,8}$, $V_{i\,11}$	10	V
Control element-filtering	V_9	5	V
	V_{10}	10	V
Pulse rejection	V_{16}	10	V
Switch-on delay	V_{17}	$V_{S\,18}$	V
Currents			
Output current, $t \leq 1$ sec	I_5, I_{14}	15	mA
Output current	$-I_{16}$	1	mA
Input current in operation	$-I_{17}$	0.2	mA
Thermal resistance (system-air)	$R_{th\,SA}$	90	K/W
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C

Range of operation

Supply voltage range	$V_{S\,18}$	16 to 32	V
Ambient temperature range	T_{amb}	0 to 70	°C

Characteristics (V_S = 24 V; T_{amb} = 25 °C)

		min	typ	max	
Current consumption					
V_i = 0 V	I_{18}		27	36	mA
V_i = 1.75 V	I_{18}		24	32	mA
Preamplifier (Switch S_1, S_2, S_3 closed)					
Gain (V_i = 40 mV)	$G_{V\,6}$, $G_{V\,13}$	39	40		dB
Open-loop gain (f = 1 kHz)	$G_{0\,6}$, $G_{0\,13}$	60	75		dB
Upper cut-off frequency (−3 dB, V_i = 40 mV)	$f_{u\,6}$, $f_{u\,13}$	50	70		kHz
Lower cut-off frequency (−3 dB, V_i = 40 mV)	$f_{l\,6}$, $f_{l\,13}$	20	30		Hz
Input resistance	R_i	350	500		kΩ
Input capacitance	C_i		5		pF
Detector amplifier (Switch S_1, S_2, S_3 closed)					
Max. current of detector outputs (short-circuit with reference to ground)	I_4, I_{15}	3.2	4	4.8	mA
Voltage of the instrument drivers (f_i = 1 kHz) V_i = 5 mV	V_5, V_{14}	1.1	1.5	1.9	V
V_i = 10 mV	V_5, V_{14}	2.1	3	3.9	V
V_i = 20 mV	V_5, V_{14}	4.5	6	7.5	V
Pulse rejection (Switch S_1, S_2, S_3 closed)					
Output voltage V_i = 15 mV	V_{16}		V_{17}		V
V_i = 30 mV	V_{16}		4.5	5	V
Control amplifier					
Control current (S_2 closed) (V_i = 1.75 V)	I_3	200	300	400	µA
Current load of the timing element (V_3 = 5 V, V_i = 0 V)	$-I_3$			10	nA
Input voltage for control start (f = 1 kHz)	V_i	15	20	25	mV
Setting range for control threshold		8		50	mV
Control voltage V_i = 50 mV	V_2		3.5		V
V_i = 1.75 V	V_2		10		V
Dynamic behavior					
Control slope ΔV_a (V_i = 40 mV to 1.75 V)	ΔV_8, ΔV_{11}		0.5	1.5	dB
Total harmonic distortion (V_i = 20 mV to 1.75 V, f_i = 40 Hz to 15 kHz)	THD		0.4	1	%
Noise voltage (V_i = 0, V_3 = 0 to 10 V)	$V_{n\,8}/V_{n\,11}$		3	10	µV
Cross talk rejection R⟷L (V_i = 2 V, f_i = 500 Hz)	a_{cr}	30	38		dB
Channel synchronization R⟷L (V_i = 50 mV)	a		0.2	1	dB
Hum suppression ($V_{hum} \leq$ 1 V, f_{hum} = 100 Hz)	a_{hum}		80		dB

Circuit description

The AF input signals V_i of both channels are moved each to an input of the IC via a defined generator resistance R_G. With the aid of the control element R_S the input resistance is controlled such that the output signal V_q, adjusted to the desired level, can be obtained.

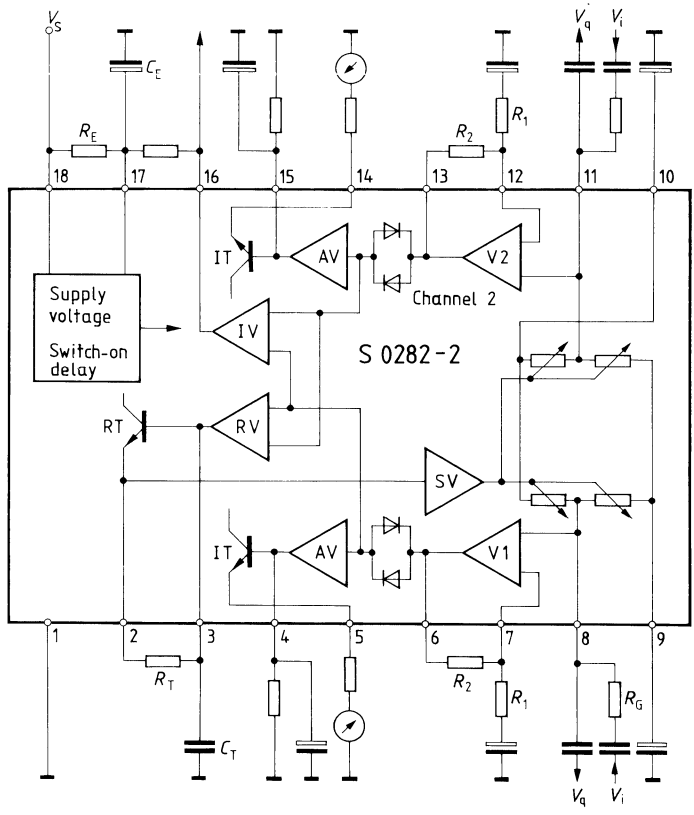
Inside the IC the signal is at first amplified with the aid of the preamplifiers V_1 and V_2. The adjusted output voltage V_q is determined by the amplification, set by the resistors R_1 and R_2, of the preamplifiers. After the amplification both signal half waves are rectified.

The rectified signals of each channel then arrive at the detector amplifier AV. The desired indicating characteristic is set by means of an RC circuit. The series-connected instrument drivers IT supply the current for the indicating instruments. The rectified signals of both channels are summed up and thus processed for the control and pulse gating. The control amplifier RV drives the control element amplifier SV via the control driver RT. The desired time response is determined by R_T, C_t.

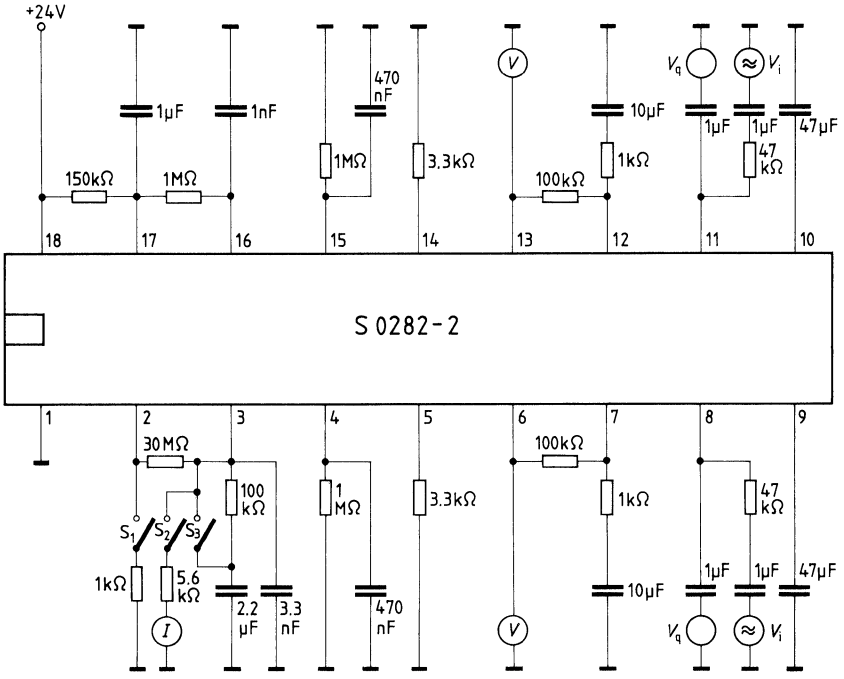
The pulse amplifier IV supplies pulses at its output as soon as one of the half waves exceeds the control threshold.

The internal supply voltage has been stabilized at approximately 14 V. After applying the supply voltage, control and instrument indication can be delayed by means ot the timing elements R_E, C_E.

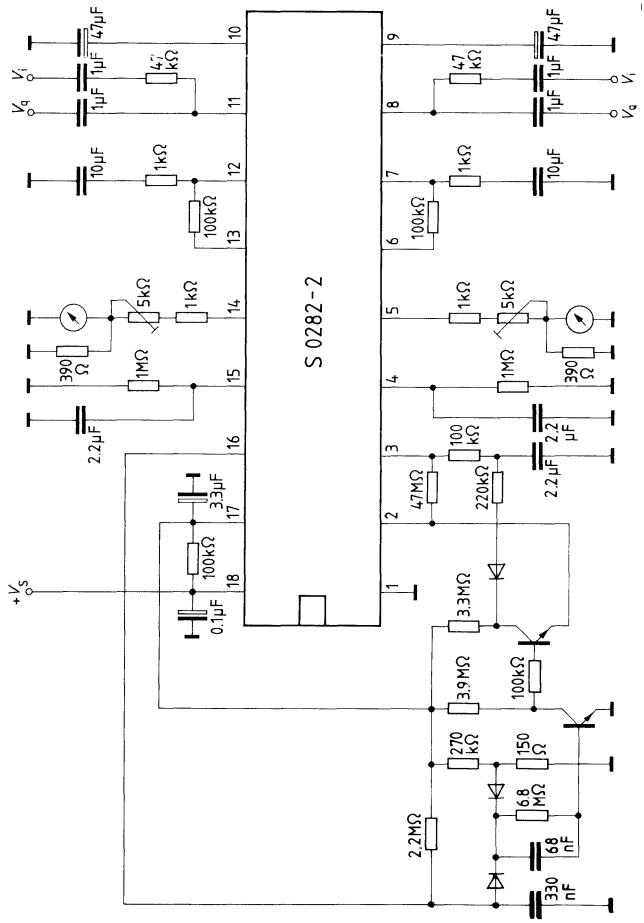
Block diagram



Test circuit



Application circuit



Stereo Equalizing Amplifier, Signal Source Switch and AF Regulator

TDA 2000

Bipolar circuit

The TDA 2000 is a signal processing IC for use in stereo cassette radio sets and is particularly suitable for use in car radios.
For each channel the TDA 2000 includes a preamplifier for playback equalization, a changeover switch for cassette to radio, and an audio control for adjustment of volume.

- Few external components
- Insensitive to hum
- Volume control by DC voltage

Type	Ordering code	Package outline
TDA 2000	Q 67000-A 1509	DIP 18

Maximum ratings

Supply voltage	$V_{S\,18}$	18	V
Voltages			
Amplifier input	$V_{i\,2}$, $V_{i\,17}$	5	V
Feedback input	$V_{i\,3}$, $V_{i\,16}$	5	V
Amplifier output	$V_{q\,4}$, $V_{q\,15}$	5	V
Radio input	$V_{i\,5}$, $V_{i\,13}$	5	V
AF output	$V_{q\,6}$, $V_{q\,7}$, $V_{q\,11}$, $V_{q\,12}$	5	V
Reference output	$V_{q\,9}$	3	V
Control voltage input	$V_{i\,10}$	5	V
Switch-on delay	V_8	5	V
Signal changeover	V_{14}	6	V
Thermal resistance (system-air)	$R_{th\,SA}$	70	K/W
Junction temperature	T_j	+150	°C
Storage temperature range	T_{stg}	−40 to 125	°C

Range of operation

Supply voltage range	$V_{S\,18}$	7 to 16	V
Ambient temperature range	T_{amb}	−25 to 85	°C

Characteristics (V_S = 9 V; T_{amb} = 25 °C according to test circuit 1, unless otherwise specified)

		min	typ	max	
Current consumption	I_S		24	35	mA
Reference voltage ($R \geq 10$ kΩ)	V_{ref}	4	4.4	4.8	V
Hum suppression (f = 100 Hz, $V_{hum} \leq 1$ V)	a_{hum}	55			dB
Cross-talk between channels [1] (f = 1 kHz, $V_q \leq 1$ V, C_{filter} = 220 µF)	a_{cr}	−45			dB
Equalizing amplifier					
Voltage gain (f = 1 kHz, V_{iK} = 1 mV)	G_v	59	60	61	dB
Open loop voltage gain (switch S closed)	G_{vo}	82	90		dB
Max. output voltage (f = 1 kHz, $THD \leq 1$ %)	$V_{q\,max}$	1.4	1.7		V
Signal-to-noise ratio (in acc. with DIN 45405, f = 330 Hz, V_{iK} = 250 µV)	$a_{S/N}$	57	60		dB
Changeover switch					
Switch-over threshold	V_{switch}	2.5	3	3.5	V
Switching voltage cassette	V_{switch}		3.2	3.5	V
Switching voltage radio	V_{switch}	2.5	2.8		V
Input current switching input V_{switch} = 0 V)	V_{switch}		100	150	µA
Blocking attenuation (V_q = 1 V, f = 1 kHz)	a_{block}	65	70		dB
Max. input voltage radio (f = 1 kHz, THD <1.2%, attenution 20 dB)	$V_{i\,max}$	800	900		mV
Volume controller					
Volume gain	G_V	6	8	10	dB
Total harmonic distortion including attenuation (f = 1 kHz, V_{iR} = 400 mV)	THD		0.5	1	%
Max. output voltage ($THD \leq 1$%, $V_{iR} \leq 400$ mV)	V_q	0.5	1		V
Noise voltage at the output (max. attenution)	V_n		5	10	µV
Control					
Range of AGC (f = 1 kHz, $V_{iR} \leq 100$ mV)	$\frac{V_{q\,max}}{V_{q\,min}}$	75	85		dB
Control difference of output V_{q1} = −20 dB	V_{q1}/V_{q2}		−12		dB
V_{q1} = −40 dB	V_{q1}/V_{q2}		−23		dB
V_{q1} = −60 dB	V_{q1}/V_{q2}		−33		dB
Control difference of the channels (V_q = 0 dB to −40 dB)	V_{q1}/V_{q2}		0	2	dB

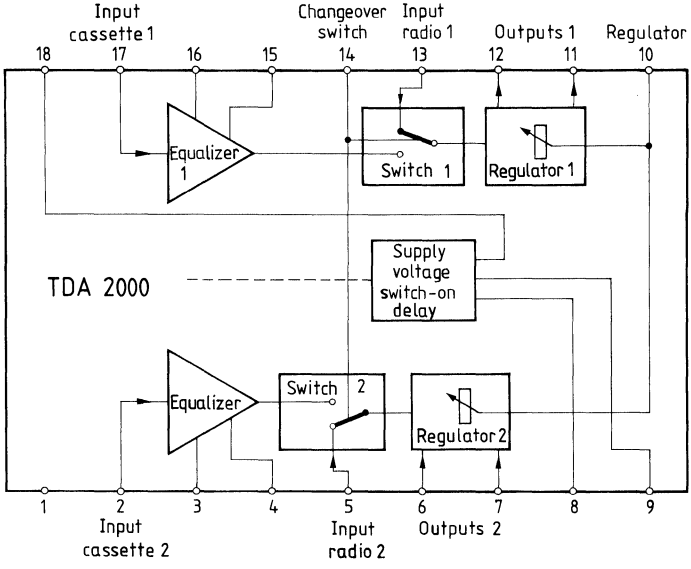
[1]) according to test circuit 2

Circuit description

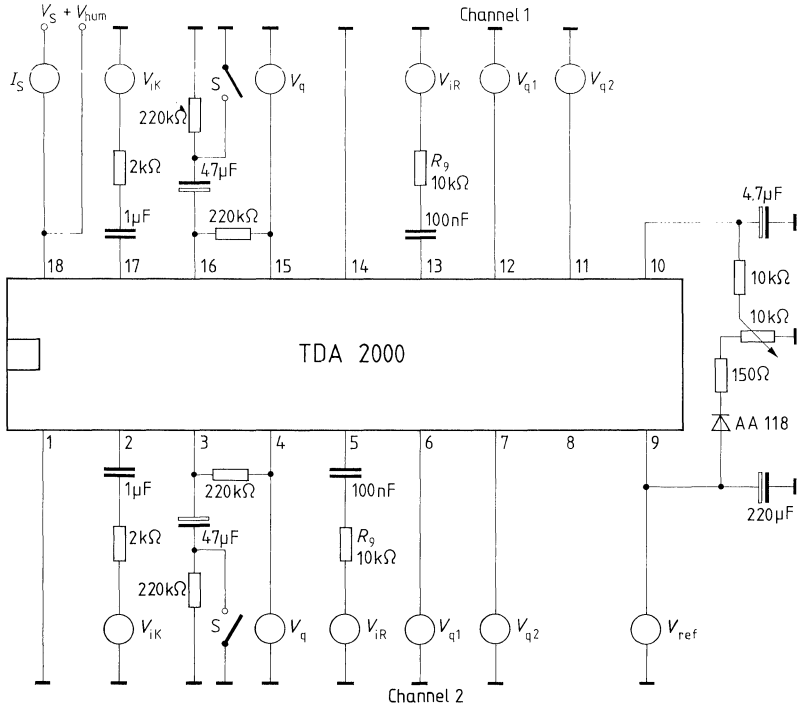
With the two-stage equalizing amplifier low noise is achieved by matching to the reply head. The amplified signal or a radio input signal respectively, is fed to a changeover switch. The changeover results from applying a DC voltage in common to both channels.

The changeover circuit supplies the AF control unit, consisting of two parallel control stages with differing attenuation characteristic. The application of an RC network permits physiologic sound amplification.
During start-up operation, an additional circuit mutes the volume.

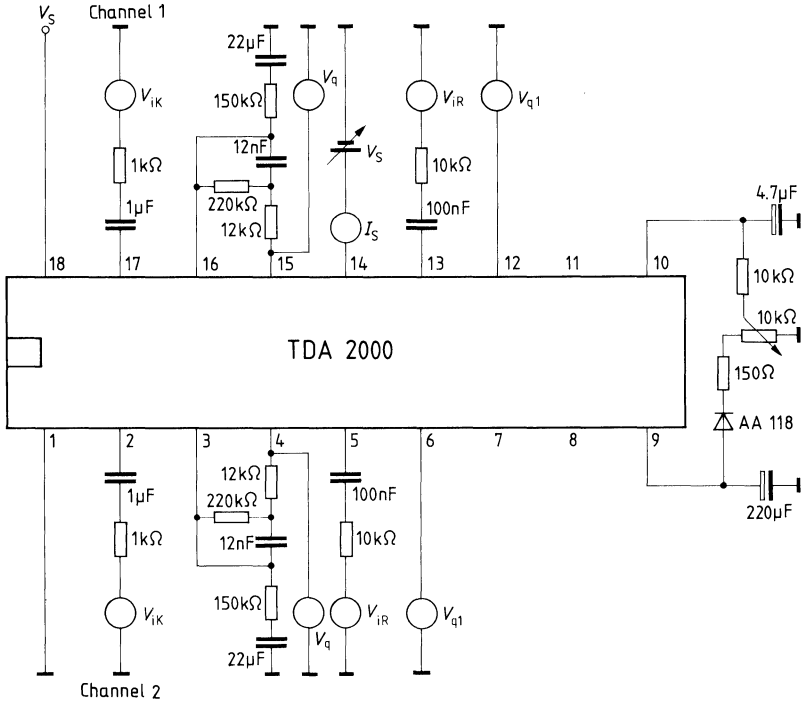
Block diagram



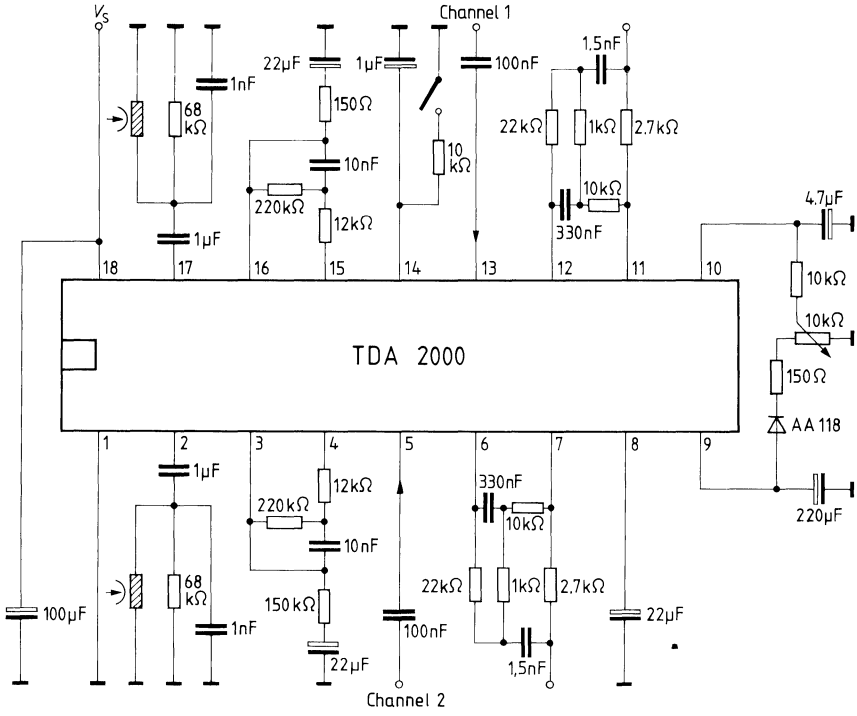
Test circuit 1



Test circuit 2



Application circuit



ICs for general-purpose applications

Remote control systems
Switches
AF power amplifiers
LED array driving
Tone control IC

Infrared Remote Control System IR 60

The MOS circuits SAB 3209, SAB 4209, SAB 3271, or SDA 2007 as receiver and SAB 3210 or SDA 2008 as transmitter permit the construction of a noise-immune IR-remote control system for up to 60 different instructions.

Because of its great variety of possible functions, this remote control system will find applications not only in the entertainment field but in the industrial area, as well.

The system concept contains an essential element of the microprocessor — the serial data bus. Because of this feature the remote control can be universally extended to include all future TV-additions conceivable today, such as digital tuning, teletext, timer, and TV-games.

Whereas three analog functions are processed by the SAB 3209, the SAB 4209 makes handling of four analog functions possible.

The SAB 3271 module exclusively is a receiver without analog functions. It mainly includes one series output and 6 parallel outputs. The display-decoder-driver SAB 3211 has optimally been matched to the receiver ICs SAB 3209 and SAB 4209 and is particularly suitable for driving LED displays.

The SDA 2007 receiver IC and the SDA 2008 transmitter IC are dealt with in the SDA 200 tuning system.

The IR 60 remote control system was completed by the IR preamplifier TDA 4050 the regulation range and regulating speed of which ensure a constant input signal at the receiver IC independent of the distance of the transmitter.

The MOS ICs SDA 3205 (receiver) and the SDA 3206 (transmitter) are available for applications with fewer instructions (up to 5).

MOS circuit

Not for new design

The receiver circuit SAB 3209, developed in MOS depletion technology, evaluates the IR signals coming from the transmitter circuit SAB 3210. Through a serial interface, which is externally accessible, the instructions get to the program memory and the analog memory. The SAB 3209 permits control of 16 programs and three analog functions. The circuit additionally contains two spare outputs and one input or output for the on/off function.

Special features:

- At the serial interface (I-bus) 30 instructions can be applied in addition to those intended for the SAB 3209, i.e. for teletext
- Through the serial interface, instructions can be transferred into the SAB 3209 directly, whereby these instructions have an absolute priority over IR-signals coming from the transmitter.
- The program outputs are short-circuit proof and can be set externally.
- The SAB 3209 can be operated with the built-in oscillator as well as with an external clock.

Type	Ordering code	Package outline
SAB 3209	Q 67100-Y 395	DIP 18

Maximum ratings (referred to V_{DD} = 0 V)

		min	max	
Supply voltage	V_{SS}	−0.3	18	V
Input voltage	V_i	−18	0.3	V
Total power dissipation	P_{tot}		500	mW
Power dissipation per output	P_q		100	mW
Storage temperature range	T_{stg}	−55	125	°C

Range of operation (referred to V_{DD} = 0 V)

Supply voltage range	V_{SS}	11 to 16	V
Ambient temperature range	T_{amb}	0 to 70	°C

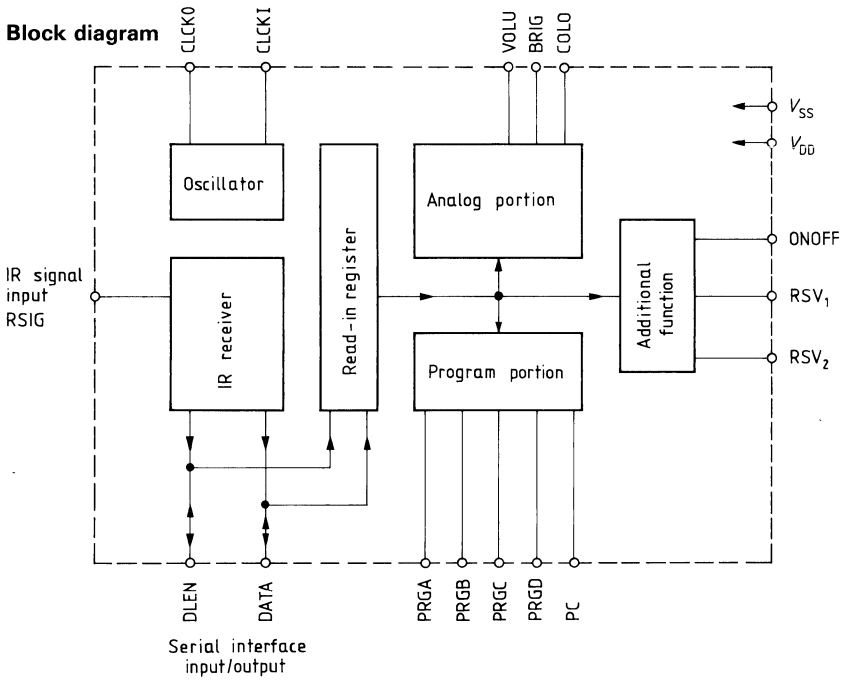
Characteristics (referred to V_{DD} = 0 V)

		min	typ	max	
Current consumption (outputs not connected)	I_{DD}		5	10	mA
Inputs					
Clock input CLCKI					
L-input voltage	V_{iL}	0		$V_{SS}-7$	V
H-input voltage	V_{iH}	$V_{SS}-1$		V_{SS}	V
Input current	I_i			15	µA
Transition times	t_{THL}, t_{TLH}			4	µs
Frequency	f	20	60	70	kHz
Remote control signal input RSIG					
Input alternating voltage	V_{iH}	$V_{SS}-1$		V_{SS}	V
	V_{iL}	0		$V_{SS}-3.5$	V
Input resistance	R_i	0.2			MΩ
Seriel interface inputs DLEN and DATA					
L-input voltage	V_{iL}	0		$V_{SS}-7$	V
H-input voltage	V_{iH}	$V_{SS}-1$		V_{SS}	V
H-input current ($V_i = V_{SS}$) (internal pull-low resistor)	I_{iH}			2	mA
Delay time + transition time	$(t_D+t_T)_{HL}$			1	µs
	$(t_D+t_T)_{LH}$			1	µs
Program stepping input PC					
H-input voltage	V_{iH}	$V_{SS}-1.5$		V_{SS}	V
L-input voltage	V_{iL}	0		$V_{SS}-7$	V
H-input current ($V_i = V_{SS}$) (internal pull-low-resistor)	I_{iH}			10	µA

Characteristics (referred to V_{DD} = 0 V)

		min	typ	max	
Outputs					
Serial interface outputs					
H-output voltage ($I_{load} \leqq 200$ mA)	V_{qH}	$V_{SS}-1.5$		V_{SS}	V
L-output voltage (I_q = 10 µA)	V_{qL}	0		0.35	V
Delay and transition time (C_L = 50 pF referred to CLCKO, V_{iLA})	$t_{DH}+t_{THL}$ and $t_{DL}+t_{TLH}$			5	µs
Program memory outputs PRGA, PRGB, PRGC, PRGD					
H-output voltage (I_q = 0.1 mA)	V_{qH}	$V_{SS}-0.5$		V_{SS}	V
L-output voltage (I_q = 10 µA)	V_{qL}	0		1.0	V
Program stepping output PC					
H-output voltage (I_q = 0.3 mA)	V_{qH}	$V_{SS}-1.5$		V_{SS}	V
L-output voltage (no load)	V_{qL}	0		2	V
Analog function outputs COLO, BRIG, VOLU					
H-output voltage (I_q = 1 mA)	V_{qH}	$V_{SS}-1.5$		V_{SS}	V
L-output voltage (I_q = 1 µA)	V_{qL}	0		0.35	V
Standby and spare outputs ONOFF, RSV_1, RSV_2					
H-output voltage (I_q = 0.3 mA)	V_{qH}	$V_{SS}-1.5$		V_{SS}	V
L-output voltage (I_q = 1 µA)	V_{qL}	0		0.35	V
Clock output CLCKO					
H-output voltage (no load)	V_{qH}	$V_{SS}-1$		V_{SS}	V
L-output voltage (no load)	V_{qL}	0		1	V

Block diagram



Pin designation

Pin No.	Description
1	V_{SS} + supply voltage
2	CLCKO, clock output
3	CLCKI, clock input
4	PRGD, program control output
5	PRGC, program control output
6	PRGB, program control output
7	PRGA, program control output
8	PC, program change strobe input/output
9	RSV_2, spare output
10	RSV_1, spare output
11	VOLU, volume control output
12	ONOFF, standby output
13	BRIG, brightness output
14	COLO, color contrast output
15	RSIG, signal input, remote control
16	DLEN, I-bus input/output
17	V_{DD}, − supply voltage
18	DATA, I-bus input/output

Description of functions

1. Infrared receiver
(pin RSIG)

The infrared receiving portion accepts the IR-signal, processes it and transfers the instructions received to the serial interface. The IR-signal consists of alternating current pulses with a frequency of approx. 30 kHz and a duration of approx. 0.5 ms per cycle. The instructions are transferred as 7-bit words (1 start bit, 6 information bits) in the biphase code. See timing diagram.

Through a change in one mask, the circuit can be converted to operate with an inverted start bit (e.g. for separation of television and radio remote control). Coding of the other 6 bits is done according to the code of table 1.

The infrared signals are repeated approx. every 120 ms. All instructions are issued by the receiving portion as repeat-instructions, with a sequence-frequency equal to that of the incoming IR-signals.

2. Serial interface (I-BUS) as an output and input
(pins DLEN, DATA)

Output at the serial interface (I-BUS) is done according to the timing diagram 2.

The outputs are open-drain stages with built-in load resistors, which may also be used as inputs. All instructions may also be put in through the serial interface, (the infrared instructions will not be processed in the circuit before they have passed the serial interface).

The input is tested to protect the transfer of the instructions against capacitive and inductive noise pulses. Therefore, the leads at the serial interface must be kept close together.

Input through the serial interface has an absolute priority over an infrared input.

It is possible to read-out instructions through the serial interface but at the same time to change them through an external circuit in such a way that they cannot be interpreted any more by the following receiver portions. For example, the pin DLE of the instructions for direct program selection can be kept on high level for two clock pulse periods beyond the output time, whereby the program memory is no longer addressed and the program instructions can be used as digit-instructions for other purposes (e.g. teletext page-selection).

3. Analog-value memory
(outputs VOLU, BRIG, COLO)

The SAB 3209 contains 3 analog-value memories for the setting of volume, brightness and color saturation.

The analog values can be altered in approx. 64 steps. The speed of alteration corresponds to the sequence-frequency of the repeat instructions (approx. 8 Hz). The analog values are put out as square pulses with a frequency of approx. 1 kHz, whereby the duty cycle corresponds to the analog value. The analog voltage value originates in an external low-frequency passing filter through formation of the mean values of timing.

By means of the instruction "normal position", the analog memories are set to a mask-programmed basic position ($\nu_{VOLU} = 1/3$, $\nu_{BRIG} = \nu_{COLO} = 1/2$, whereby $\nu = t_{High}/T$). When the supply voltage rises starting at 0, the analog values are also set to the normal position.

Volume control output VOLU:

The volume output is internally kept on a low level
- when the quicktone-flipflop is set,
- when the circuit is in a "standby" mode,
- when pin PC is on a high level

Quicktone:

An appropriate instruction sets a flipflop.
The flipflop is reset:
- by instruction "Vol+",
- by condition "standby",
- by an instruction from the program memory,
- by the instruction "normal position".

As long as the qickton flipflop is set, the volume output is kept "low".

As long as the circuit remains in the "standby" condition, the alteration-instructions for the analog memory are ineffective.

4. Program memory
(outputs and inputs PRGA, PRGB, PRGC, PRGD)

The program memory consists of a 4-bit ring counter which permits the addressing of 16 programs.

The 16 programs may be addressed through remote control by selecting 1...16 or through up- and downcounting of the ring counter.

When the supply voltages rises starting at zero, the program outputs are set to LLLH. By changing one mask it is possible to set a different program instead. The outputs of the program memory are also effective as inputs, as they may be set or reset externally through a low-resistance control.

Strobe output, stepping sequence input:
(pin PC)

When the program counter receives an instruction via remote control, or the supply voltage rises starting at zero, a positive pulse in produced at output PC. For the duration of a positive potential the volume output is kept "low" (muting).

The output may be connected to a capacitor to extend the muting (up to approx. 0.5 s).

The same capacitor will have the effect that a change at the program memory outputs has been completed when the strobe signal occurs.

Pin connection PC may also be used as an input. If a positive potential is applied externally, the program counter proceeds by one step. Thereby, the external capacitor will have a debouncing effect. During "standby" condition the output "PC" is on a static positive level.

5. Additional control functions

Standby output/input:
(pin ONOFF)

Through a transistor it controls the power supply. When a program is called for — and also in connection with some other instructions specified in table 1 — the set is turned on through this output.

In = low, standby = high

Through the instruction "standby" the set is put into a "standby" mode. When the supply voltage rises starting at zero, the set is also switched to "standby".

Pin connection ONOFF also acts as an input when controlled from a low resistance source, e.g. with a wiping contact at the mains-switch.

Spare outputs

Pin RSV_1

The output is controlled by a toggle-flipflop. With each depression of the corresponding button of the transmitter the output changes to the opposite condition.

The preference position is high.

The position is set:
— when the supply voltage is turned on,
— when condition "standby" exists,
— when the instruction "normal position" is issued.

Pin RSV_2

The output is controlled by a toggle-flipflop. With each depression of the corresponding button of the transmitter the output changes to the opposite condition.

The preference position is low

The position is set:
— when the supply voltage is turned on,
— when condition "standby" exists,
— when the instruction "normal position" is issued.

Table 1
Coding of instructions on the I BUS and for IR transmission

No.	Code						Instruction
	F	E	D	C	B	A	
0	0	0	0	0	0	0	Normal position/switch on
1				0	0	1	Quicktone (muting)
2				0	1	0	Standby
3				0	1	1	Spare 1
4				1	0	0	Program step + /switch on
5				1	0	1	Program step − /switch on
6				1	1	0	Switch on
7				1	1	1	Spare 2/switch on
40	1	0	1	0	0	0	Volume +
41				0	0	1	Volume −
42				0	1	0	Brightness +
43				0	1	1	Brightness −
44				1	0	0	Color +
45				1	0	1	Color −
46				1	1	0	reserved for the 4th analog function
47				1	1	1	

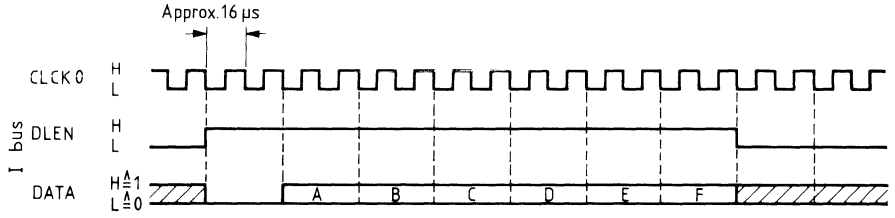
Table 1, continued
Coding of instructions on the I BUS and for IR transmission

No.	Code						Instruction			
	F	E	D	C	B	A	D	C	B	A (PRG output)
16	0	1	0	0	0	0	L	L	L	L / on
17				0	0	1	L	L	L	H / on preferred position
18				0	1	0	L	L	H	L / on
19				0	1	1	L	L	H	H / on
20				1	0	0	L	H	L	L / on
21				1	0	1	L	H	L	H / on
22				1	1	0	L	H	H	L / on
23				1	1	1	L	H	H	H / on
24	0	1	1	0	0	0	H	L	L	L / on
25				0	0	1	H	L	L	H / on
26				0	1	0	H	L	H	L / on
27				0	1	1	H	L	H	H / on
28				1	0	0	H	H	L	L / on
29				1	0	1	H	H	L	H / on
30				1	1	0	H	H	H	L / on
31				1	1	1	H	H	H	H / on

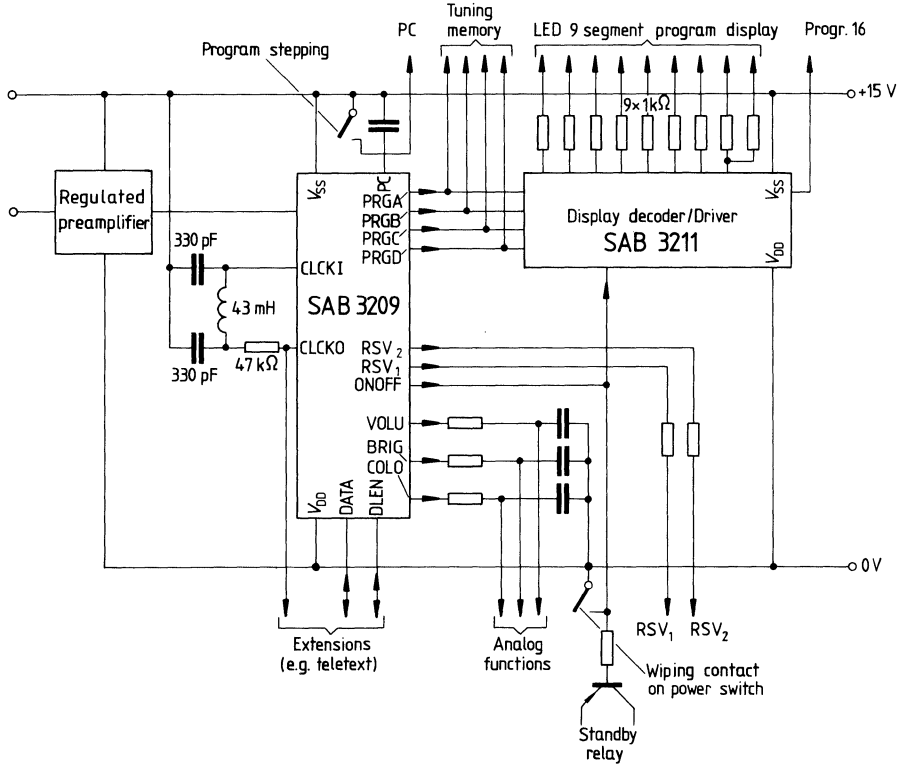
Instructions 8 to 15, 32 to 39, and 48 to 61 are not evaluated by the circuit, but only edited through the serial interface.

Instruction 63 (= 111 111) must be kept free (see timing diagram).
Instruction 62 (= 111 110) is the end-instruction. (see data sheet of SAB 3210)

Timing diagram
Serial interface (I BUS) for the input and output of instructions



External connections



MOS circuit

The receiver circuit SAB 4209, developed in MOS depletion technology, evaluates the IR signals coming from the transmitter circuit SAB 3210. Through a serial interface, which is externally accessible, the instructions get to the program memory and the analog memory. The SAB 4209 permits the control of 16 programs and four analog functions. In addition, the circuit is provided for a keyboard changeover and one input or output for the on/off function.

Special features

- At the serial interface (I-bus) 30 instructions can be applied in addition to those intended for the SAB 4209, i. e. for teletext.
- Through the serial interface, instructions can be transferred into the SAB 4209 directly. whereby these instructions have an absolute priority over IR signals coming from the transmitter.
- The program outputs are short-circuit proof and can be set externally.
- The SAB 4209 can be operated with the built-in oscillator as well as with an external clock.

Type	Ordering code	Package outline
SAB 4209	Q 67100-Y460	DIP 18

Maximum ratings (referred to V_{DD} = 0 V)

Supply voltage range	V_{SS}	−0.3 to 18	V
Input voltage range	V_i	V_{SS} − 18 to V_{SS} + 0.3	V
Total power dissipation	P_{tot}	500	mW
Power dissipation per output	P_q	100	mW
Storage temperature range	T_{stg}	−40 to 125	°C

Range of operation (referred to V_{DD} = 0 V)

Supply voltage range	V_{SS}	11 to 16	V
Ambient temperature range	T_{amb}	0 to 70	°C

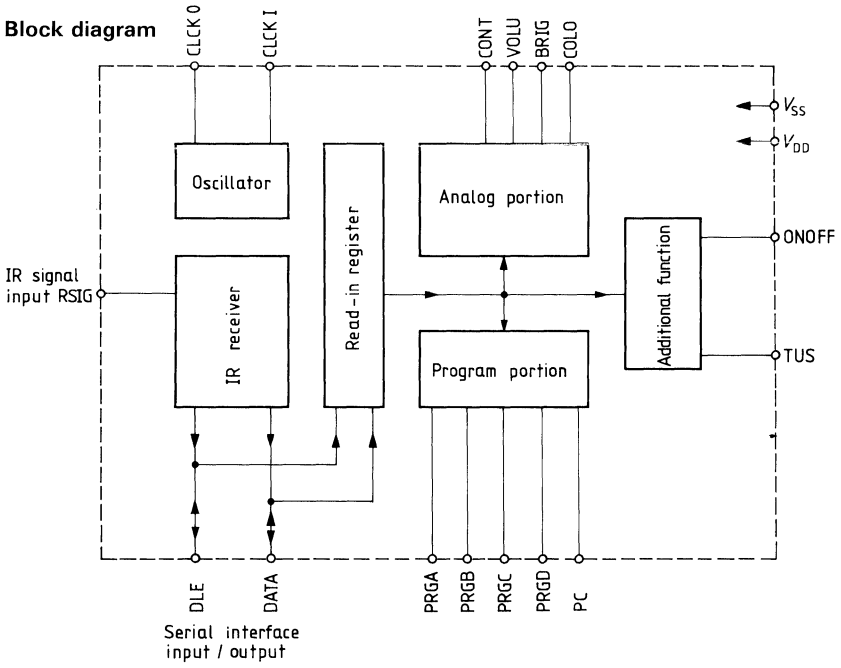
Characteristics (referred to V_{DD} = 0 V, T_{amb} = 0 to 70 °C)

		min	typ	max	
Current consumption (outputs not connected)	I_{DD}		5	10	mA
Inputs					
Clock input CLCKI					
L-input voltage	V_{iL}	0		$V_{SS}-7$	V
H-input voltage	V_{iH}	$V_{SS}-1$			V
Input current	I_i			V_{SS} 15	µA
Transition times	t_{THL}, t_{TLH}			4	µs
Frequency	f	20	60	70	kHz
Remote control signal input RSIG					
Input alternating voltage	V_{iH}	$V_{SS}-1$		V_{SS}	V
	V_{iL}	0		$V_{SS}-3.5$	V
Input resistance	R_i	0.2			MΩ
Serial interface inputs					
DLEN and DATA					
L-input voltage	V_{iL}	0		$V_{SS}-7$	V
H-input voltage	V_{iH}	$V_{SS}-1$		V_{SS}	V
H-input current ($V_i = V_{SS}$) (internal pull-low resistor)	I_{iH}			2	mA
Delay time + transition time	$(t_D+t_T)_{HL}$			} 1	µs
	$(t_D+t_T)_{LH}$			}	
Program stepping input PC					
H-input voltage	V_{iH}	$V_{SS}-1.5$		V_{SS}	V
L-input voltage	V_{iL}	0		$V_{SS}-7$	V
H-input current ($V_i = V_{SS}$) (internal pull-low-resistor)	I_{iH}			10	µA
Outputs					
Standby output ONOFF					
H-input voltage (I_{iH} <1 mA)	V_{iH}	$V_{SS}-1$ V		V_{SS}	V

Characteristics (referred to V_{DD} = 0 V, T_{amb} = 0 to 70 °C)

		min	typ	max	
Outputs					
Serial interface outputs					
H-output voltage ($I_{load} \leqq 200\ \mu A$)	$V_{q\,H}$	$V_{SS}-1.5$		V_{SS}	V
L-output voltage (I_q = 10 µA)	$V_{q\,L}$	0		0.35	V
Delay- and transition time	$t_{DH}+t_{THL}$			5	µs
(CL = 50 pF referred to CLCKI)	$t_{DL}+t_{THL}$				µs
Program memory outputs PRGA, PRGB, PRGC, PRGD					
H-output voltage (I_q = 0.1 mA)	$V_{q\,H}$	$V_{SS}-0.5$		V_{SS}	V
L-output voltage (I_q = 10 µA)	$V_{q\,L}$	0		1	V
Program stepping output PC					
H-output voltage (I_q = 0.3 mA)	$V_{q\,H}$	$V_{SS}-1.5$		V_{SS}	V
L-output voltage (no load)	$V_{q\,L}$	0		2	V
Analog function outputs COLO, BRIG, VOLU, CONT					
H-output voltage (I_q = 1 mA)	$V_{q\,H}$	$V_{SS}-1.5$		V_{SS}	V
L-output voltage (I_q = 1 µA)	$V_{q\,L}$	0		0.35	V
Standby and spare outputs ONOFF, TUS					
H-output voltage (I_q = 0.3 mA)	$V_{q\,H}$	$V_{SS}-1.5$		V_{SS}	V
L-output voltage (I_q = 1 µA)	$V_{q\,L}$	0		0.35	V
Clock output CLCKO					
H-output voltage (no load)	$V_{q\,H}$	$V_{SS}-1$		V_{SS}	V
L-output voltage (no load)	$V_{q\,L}$	0		1	V

Block diagram



Pin designation

Pin No.	Description
1	V_{SS}, supply voltage
2	CLCKO, clock output
3	CLCKI, clock input
4	PRGD, program control output
5	PRGC, program control output
6	PRGB, program control output
7	PRGA, program control output
8	PC, program change, strobe input/output
9	TUS, keyboard changeover
10	VOLU, volume control output
11	ONOFF, standby output
12	CONT, contrast output
13	BRIG, brightness output
14	COLO, color contrast output
15	RSIG, IR input
16	DLE, I-bus input/output
17	V_{DD}, supply voltage
18	DATA, I-bus input/output

Description of functions

1. **Infrared receiver**
(pin RSIG)

The infrared receiving portion accepts the IR signal, processes it and transfers the instructions received to the serial interface. The IR-signal consists of alternating current pulses with a frequency of approx. 30 kHz and a duration of approx. 0.5 ms per cycle. The instructions are transferred as 7-bit words (1 start bit, 6 information bits) in the biphase code. See timing diagram 1.

Through a change in one mask, the circuit can be converted to operate with an inverted start bit (e.g. for separation of television and radio remote control). Coding of the other 6 bits is done according to the code of table 1.

The infrared signals are repeated approx. every 120 ms. All instructions are issued by the receiving portion as repeat-instructions, with a sequence-frequency equal to that of the incoming IR-signals.

2. **Serial interface (I-BUS) as an output and input**
(pins DLEN, DATA)

Output at the serial interface (I-BUS) is done according to the timing diagram 2.

The outputs are open-drain stages with built-in load resistors, which may also be used as inputs. All instructions may also be put in through the serial interface, timing diagram 3 (the infrared instructions will not be processed in the circuit before they have passed the serial interface).

The input is tested to protect the transfer of the instructions against capacitive and inductive noise pulses. Therefore, the leads at the serial interface must be kept close together. Input through the serial interface has absolute priority over an infrared input. It is possible to read-out instructions through the serial interface but at the same time to change them through an external circuit in such a way that they cannot be interpreted any more by the following receiver portions. For example, pin DLE of the instructions for direct program selection can be kept on high level for two clock pulse periods beyond the output time, whereby the program memory is no longer addressed and the program instructions can be used as digit-instructions for other purposes (e.g. teletext page-selection).

3. **Analog-value memory**
(outputs VOLU, BRIG, COLO, CONT)

The SAB 4209 contains 4 analog-value memories for the setting of volume, brightness, color saturation, and contrast.

The analog values can be altered in approx. 60 steps. The speed of alteration corresponds to the sequence-frequency of the repeat instructions (approx. 8 Hz). The analog values are put out as square pulses with a frequency of approx. 1 kHz, whereby the duty cycle corresponds to the analog value. The analog voltage value originates in an external low-frequency passing filter through formation of the mean values of timing.

By means of the command "normal position", the analog memories are set to a mask-programmed basic position ($\nu_{VOLU} = 1/3$, $\nu_{CONT} = \nu_{BRIG} = \nu_{COLO} = 1/2$, whereby $\nu =$

t_{High}/T). When the supply voltage rises starting at 0, the analog values are also set to the normal position.

Volume control output VOLU:

The volume output is internally kept on a low level
- approx. 128 msec prior to appearing of the H pulse at the output after a program change instruction
- when the quicktone-flipflop is set,
- when the circuit is in a "standby" mode,
- when pin PC is on a high level

Quicktone:

An appropriate command sets a flipflop in the actually complementary state.
The flipflop is reset
- by instruction "Volt +",
- by condition "standby",
- by an instruction to the program memory,
- by the instruction "normal position".

As long as the quicktone flipflop is set, the volume output is kept "low".

As long as the circuit remains in the "standby" condition, the alteration instructions for the analog memory are ineffective.

When switching-on again after the "standby" condition, the analog outputs move into the basic position.

4. Program memory
(outputs and inputs PRGA, PRGB, PRGC, PRGD)

The program memory consists of a 4-bit ring counter which permits the addressing of 16 programs.

The 16 programs may be addressed through remote control by selecting 1...16 or, through up- and downcounting of the ring counter.

When the supply voltage rises starting at zero, the program outputs are set to LLLH. By changing one mask it is possible to set a different program instead. The outputs of the program memory are also effective as inputs, as they may be set or reset externally through a low-resistance control.

Strobe output, stepping sequence input:
(pin PC)

When the program counter receives an instruction via remote control, a potitive pulse is produced at output PC after a certain time delay. At the start of the delay time the volume output VOLU is muted. Muting can be reverted with the aid of the trailing edge of the PC pulse (see timing diagram 4). The output PC may additionally be connected to a capacitor to extend the muting (up to approx. 0.5 s).

The same muting hehavior results when the supply voltage rises starting at zero, and pin ONOFF is simultaneously kept on low (see timing diagram 5).

Pin connection PC may also be used as an input. If a positive potential is applied externally, the program counter proceeds by one step. Thereby the external capacitor will have a debouncing effect (see timing diagram 6). During "standby" condition the output "PC" is on a static positive level. The PC pulse occurs only once per pressure on the according transmitter button.

5. Standby-output/input:
(pin ONOFF)

Through a transistor it controls the power supply. When a program is called for — and also in connection with some other instructions specified in table 1 — the set is turned on through this output.

In = low, standby = high

Through the instruction "standby" the set is put into a "standby" mode. When the supply voltage rises starting at zero, the set is also switched to "standby".

Pin ONOFF also acts as an input when controlled from a low resistance source, e.g. with a wiping contact at the mains-switch.

6. Keyboard changeover
(pin TUS)

The output is controlled by a toggle-flipflop. With each depression of the corresponding button of the transmitter the output changes to the opposite condition.

The preference position is low.

The position is set
— when the supply voltage is turned on,
— when condition "standby" exists,
— when the instruction "normal position" is issued.

The output can be set and reset from outside by low-ohmic connections.

When the output is in the high condition, the incoming instructions are no longer evaluated in the receiver module, but only output at the serial interface. Exception: The instruction "Keyboard changeover" (No. 7) and "Standby" (No. 2) are evaluated in any case.

Table 1
Coding of instructions on the I BUS and for IR transmission

No.	Code						Instruction	After instruction TUS
	F	E	D	C	B	A		
0	0	0	0	0	0	0	Normal position	Previous condition is maintained
1				0	0	1	Quicktone (muting)	
2				0	1	0	Standby	Standby + TR (keyboard switching)
3				0	1	1		Previous condition is maintained
4				1	0	0	Program step +/on	"
5				1	0	1	Program step −/on	"
6				1	1	0	On	"
7				1	1	1	TUS/on	TR (keyboard reset)
8	0	0	1	0	0	0	Volume +	Previous condition is maintained
9				0	0	1	Volume −	
10				0	1	0	Brightness +	"
11				0	1	1	Brightness −	"
12				1	0	0	Color +	"
13				1	0	1	Color −	"
14				1	1	0	Contrast +	"
15				1	1	1	Contrast −	"

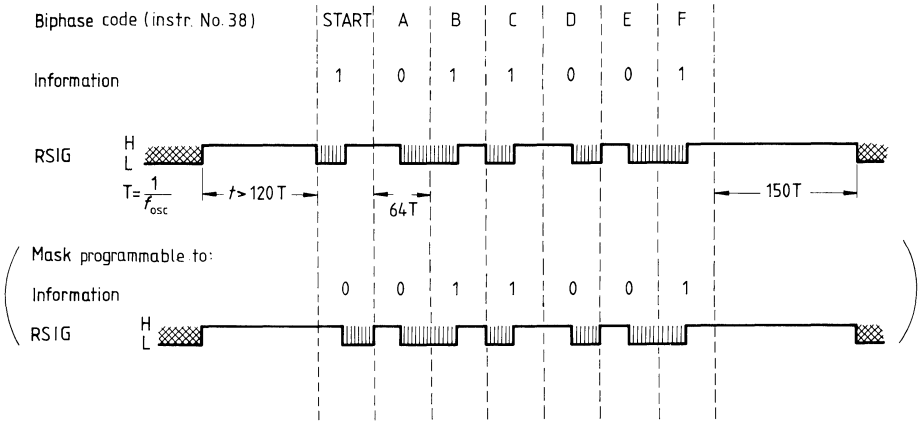
Table 1 continued
Coding of instructions on the I-BUS and for IR-transmission

No.	Code						Instruction				After instruction 7
	F	E	D	C	B	A	D	C	B	A (PRG output)	Keyboard changeover
16	0	1	0	0	0	0	L	L	L	L / on	Previous condition
17				0	0	1	L	L	L	H / on preferred position	is maintained
18				0	1	0	L	L	H	L / on	"
19				0	1	1	L	L	H	H / on	"
20				1	0	0	L	H	L	L / on	"
21				1	0	1	L	H	L	H / on	"
22				1	1	0	L	H	H	L / on	"
23				1	1	1	L	H	H	H / on	"
24	0	1	1	0	0	0	H	L	L	L / on	"
25				0	0	1	H	L	L	H / on	"
26				0	1	0	H	L	H	L / on	"
27				1	0	0	H	L	H	H / on	"
28				1	0	0	H	H	L	L / on	"
29				1	0	1	H	H	L	H / on	"
30				1	1	0	H	H	H	L / on	"
31				1	1	1	H	H	H	H / on	"

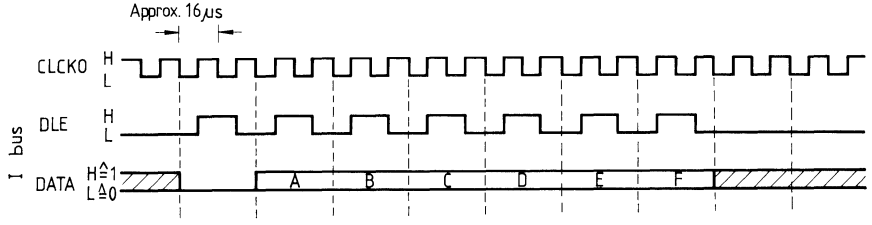
Instructions 32 to 61 are not processed by the circuit but only edited through the serial interface.

Instruction 63 (= 111111) must be kept free (see timing diagram 1).
Instruction 62 (= 111110) is the end-instruction. (See data sheet of SAB 3210)

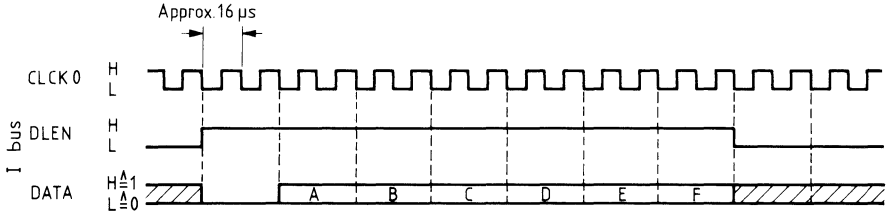
Timing diagram 1
(biphase coding)



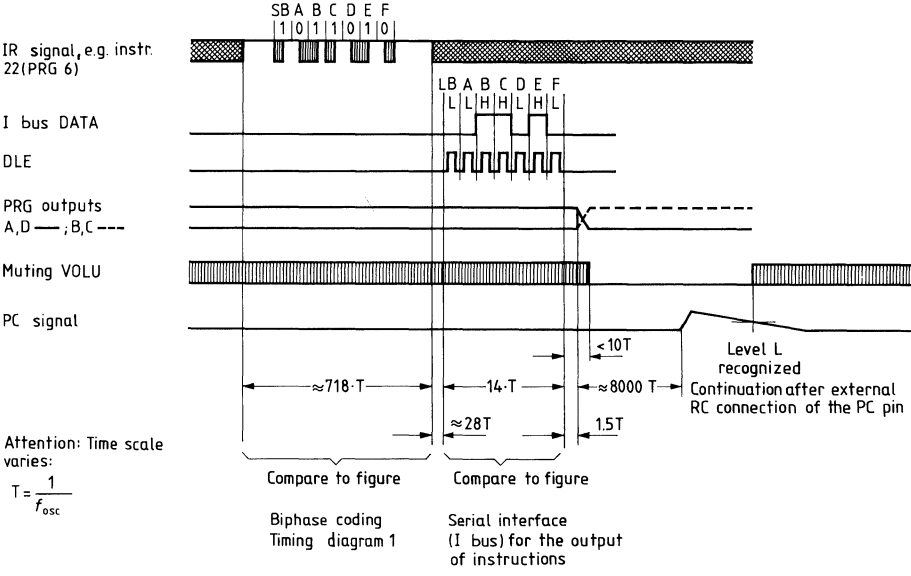
Timing diagram 2
Serial interface (I bus) for the output of instructions



Timing diagram 3
Serial interface (I bus) for the input of instructions

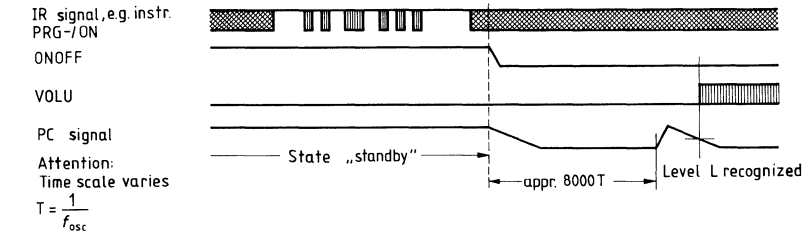


Timing diagram 4

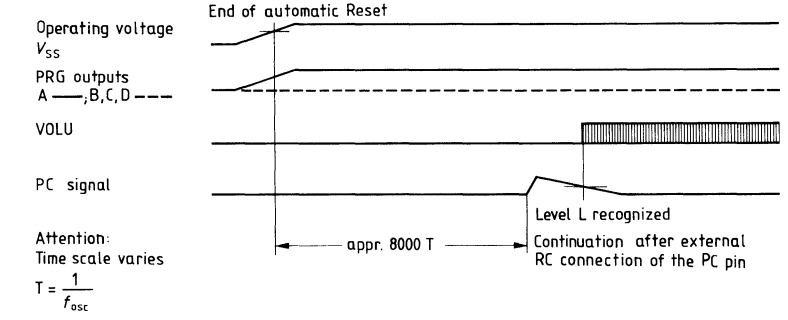


Timing diagram 5

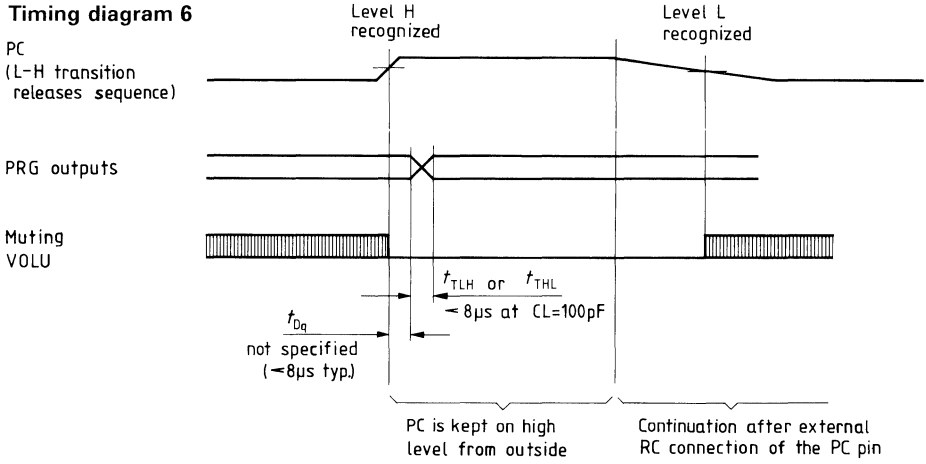
Example a) Switching on by means of an IR instruction



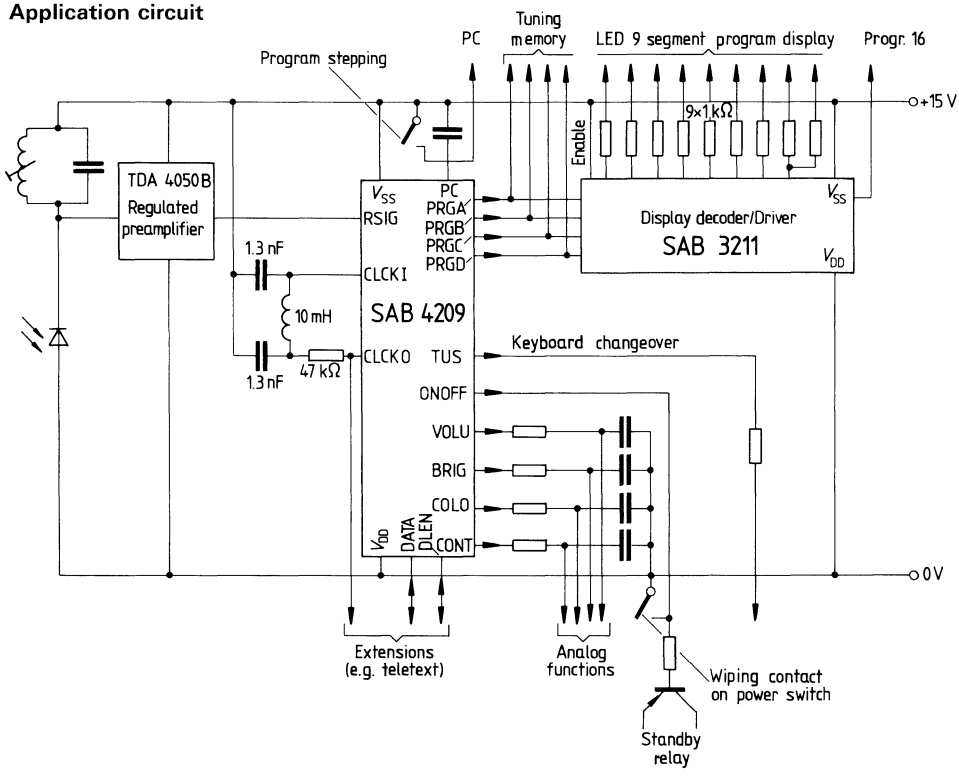
Example b) ONOFF is connected to V_{DD} during the supply voltage rise via wiping contact



Timing diagram 6



Application circuit



MOS circuit

The transmitter circuit SAB 3210, developed in P-MOS depletion technology converts the instructions obtained from a matrix to a 6-bit biphase code. By means of this code up to a maximum of 60 instructions can be transferred via an infrared transmitting stage, to a receiver equipped with the IC SAB 3209.

Special features:

- 32 instructions are possible without special means — an extension to 60 is possible connecting additional diodes.
- Low power consumption of typically 3 mA (5 mA max.)
  An external npn transistor, driven by the transmitter circuit, disconnects the battery during quiescent periods, thereby extending its life period considerably
- Large supply voltage range from 5 V to 16 V
- A mask-programmed starting bit preceding each instruction makes an additional discrimination possible for the receiver. This feature permits using two independent remote control systems in the same room (e.g. for TV and radio sets)

Type	Ordering code	Package outline
SAB 3210	Q 67100-Y 396	DIP 18

Maximum ratings (referred to V_{DD} = 0 V)

Supply voltage	V_{SS}	0.3 to 18	V
Input voltage	V_i	$V_{SS}-18$ to $V_{SS}+0.3$	V
Total power dissipation	P_{tot}	500	mW
Power dissipation per output	P_q	100	mW
Storage temperature range	T_{stg}	−55 to 125	°C

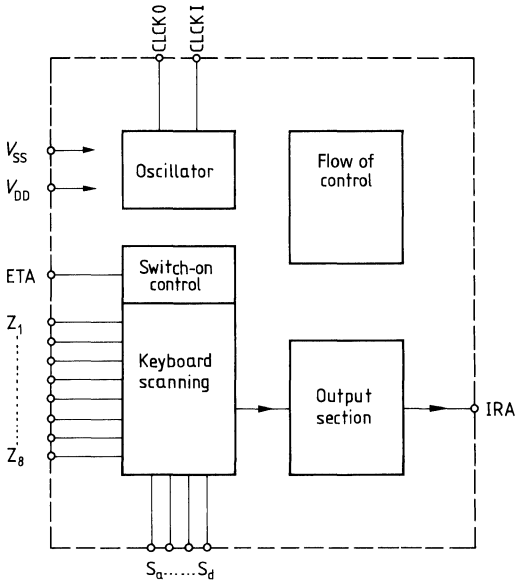
Range of operation (referred to V_{DD} = 0 V)

Supply voltage range	V_{SS}	5 to 16	V
Ambient temperature range	T_{amb}	0 to 70	°C

Characteristics (referred to $V_{DD} = 0$ V)

		min	typ	max	
Current consumption (outputs not connected)	I_{DD}		3	5	mA
Oscillator: Clock input CLCKI					
H-input voltage	V_{iH}	$V_{SS}-1$		V_{SS}	V
L-input voltage	V_{iL}	0		$V_{SS}-4$	V
Clock output CLCKO					
H-output voltage	V_{qH}	$V_{SS}-1$		V_{SS}	V
L-output voltage	V_{qL}	0		$V_{SS}+1$	V
Leakage current, total current of column outputs S_a, S_b, S_c, S_d, ETA, IRA ($V_q = -10$ V; $V_{DD} = 0$ V)					
Column resistors R_a, R_b, R_c, R_d, towards $-V_S$	R_C	33		47	kΩ
Remote control signal — output IRA ($I_{qH} = 4$ mA; $V_{DD} \leqq -6$ V) H-output voltage	V_{qH}	$V_{SS}-5$		V_{SS}	V
Switch-on transistor — output ETA H-output current ($V_q = V_{SS} - 4$ V)	I_{qH}	0.1		0.5	mA

Block diagram



Pin designation

Pin No.	Description
1	V_{SS}
2	Column a
3	Column b
4	Column c
5	Column d
6	V_{DD}
7	ETA (switch-on trans. output)
8	IRA (Infrared output)
9	Row 1
10	Row 2
11	Row 3
12	Row 4
13	Row 5
14	Row 6
15	Row 7
16	Row 8
17	CLCKI (oscillator input)
18	CLCKO (oscillator output)

Description of functions

The SAB 3210 operates in a wide range of supply voltages and with a very low current consumption. It is therefore suited for battery operation and for operation in a television set as a keyboard scanner from a 12 V supply. The circuit contains a control output for an npn transistor which separates the circuit from the battery as long as no button has been pushed.

Input keyboard:

The transmitter contains an input matrix consisting of 4 columns and 8 rows. In order to input an instruction a column output must be connected with a row input. Thereby the transmitter is turned on and a corresponding instruction is issued. Without further steps it is possible to input 32 instructions with simple switching contacts.

With additional diodes, the instruction set can be expanded to 60. For this purpose 2 diodes are required for every additional 4 instructions. As a protection against an unintended double-actuation (pushing 2 buttons simultaneously) the SAB 3210 contains a column interlock. E.g. 1a+1c are recognized as an erroneous operation. Instead of a wrong instruction only the end-command is transmitted. The circuit is not inerlocked against a multiple-button operation within one column (e.g. 8a + 5a = 85a) as this combination is used for the extension of input capabilities from 4×8 instructions to $4 \times (8+7)$ instructions.

End instruction:

After release of a key, the instruction selected is repeated no more than once, depending on the exact timing of the release. After the last transmission of the instruction selected, an end instruction is transmitted which signalizes to the receiver that the button has been released.

Output:

The transmitter converts the instruction received to a biphase code (timing diagram 1). Ahead of the 6 information bits, a startbit is transmitted. This startbit permits an additional discrimination to the receiver.

Through mask-programming the startbit can be changed from 1 to 0 which makes it possible to remote-control, with the same remote control system, a television set and a radio set in the same room independent from each other.

The output signal is keyed with half the clock frequency ($f_{CLCK}/2 \approx 30$ kHz); with this signal an infrared transmitter stage can be controlled. At rest, the output is on a high-resistance low-level.

Ahead of the output of an IR instruction a pre-signal is output which facilitates gain control on the receiver side.

Timing:

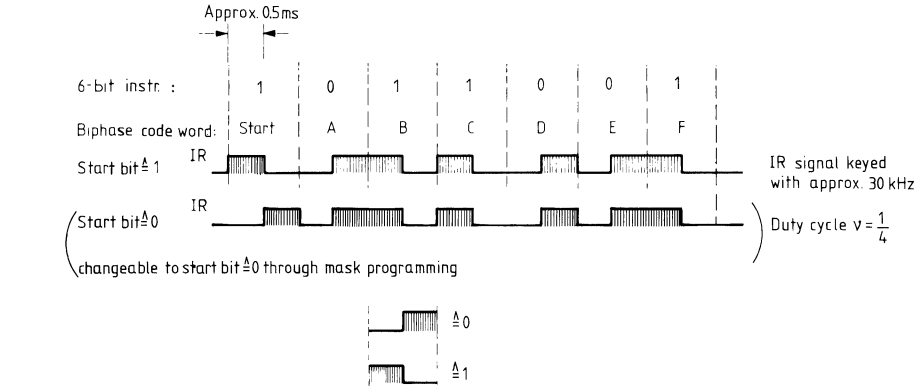
In normal operation the clock frequency is approx. 60 kHz. The instructions are issued in a time interval of approx. 120 ms, the duration of an instruction being approx. 7 ms (see timing diagram 1). Before scanning the matrix there is a debounce-delay of approx. 20 ms.

Instruction set with assignment of the instructions to the buttons

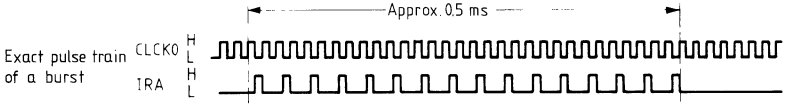
Basic instructions			Extension instructions		
Instr. No.	Code FED CBA	Button	Instr. No.	Code FED CBA	Button
0	000 000	1a	32	100 000	81a
1	000 001	1b	33	100 001	81b
2	000 010	1c	34	100 010	81c
3	000 011	1d	35	100 011	81d
4	000 100	2a	36	100 100	82a
5	000 101	2b	37	100 101	82b
6	000 110	2c	38	100 110	82c
7	000 111	2d	39	100 111	82d
8	001 000	3a	40	101 000	83a
9	001 001	3b	41	101 001	83b
10	001 010	3c	42	101 010	83c
11	001 011	3d	43	101 011	83d
12	001 100	4a	44	101 100	84a
13	001 101	4b	45	101 101	84b
14	001 110	4c	46	101 110	84c
15	001 111	4d	47	101 111	84d
16	010 000	5a	48	110 000	85a
17	010 001	5b	49	110 001	85b
18	010 010	5c	50	110 010	85c
19	010 011	5d	51	110 011	85d
20	010 100	6a	52	110 100	86a
21	010 101	6b	53	110 101	86b
22	010 110	6c	54	110 110	86c
23	010 111	6d	55	110 111	86d
24	011 000	7a	56	111 000	87a
25	011 001	7b	57	111 001	87b
26	011 010	7c	58	111 010	87c
27	011 011	7d	59	111 011	87d
28	011 100	8a	60	111 100	} not used
29	011 101	8b	61	111 101	} not used
30	011 110	8c	62	111 110	end-instruction not permitted[1]
31	011 111	8d	63	111 111	end-instruction not permitted[1]

[1] because of ambiguity of the biphase-code

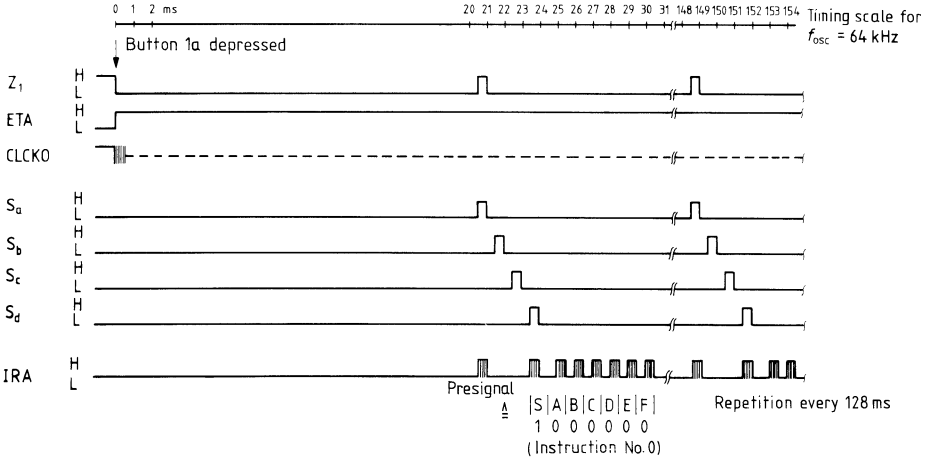
Timing diagram 1 (biphase coding, plotted without presignal)



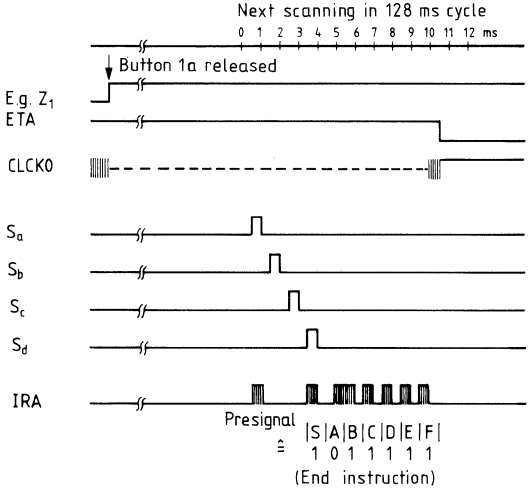
Instruction 111 111 with start bit 1 may not be programmed in order to avoid mixup with the already programmed instruction 000 000 with start bit 0



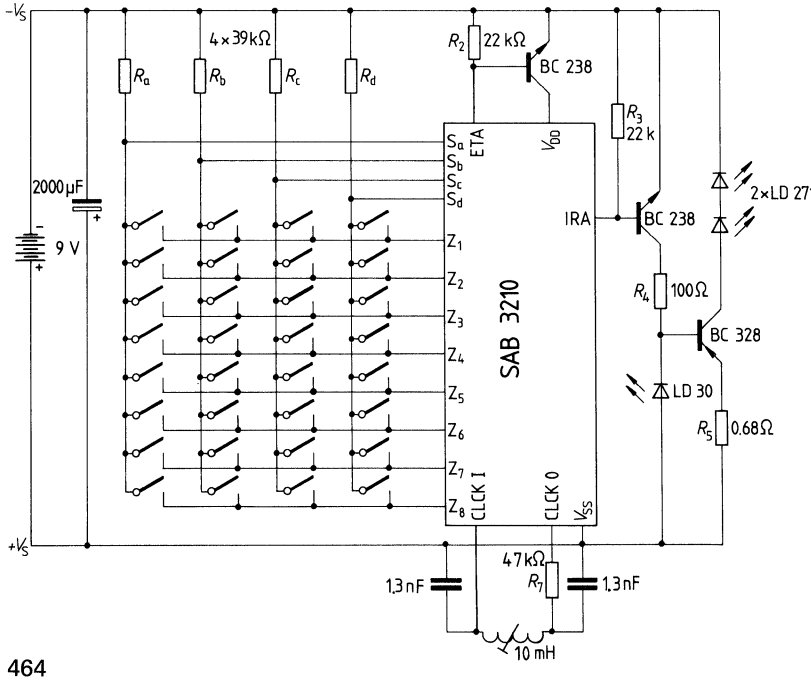
Timing diagram 2 (pushing a button)



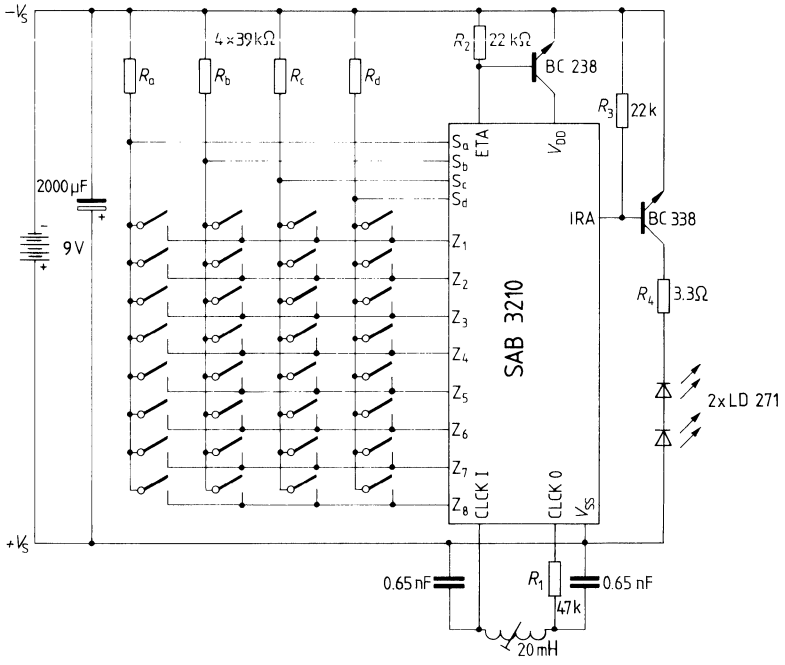
Timing diagram 3 (releasing a button)



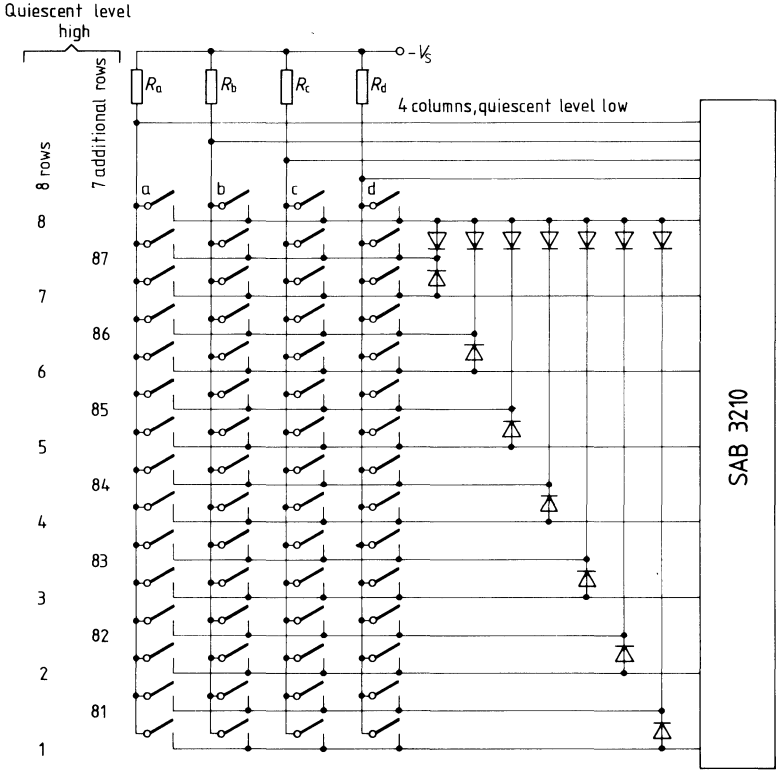
External connection of the SAB 3210 (example)



Another example of external connection of the SAB 3210
(simplified final stage and changed oscillator circuitry)



Expanded external connection of the SAB 3210 for 60 instructions (example)



MOS circuit

The SAB 3211, developed in MOS depletion technology, is especially matched to the SAB 3209.
It is particularly suited to indicate channels 1 to 16 and 1 to 8 at TV sets by means of LED displays.
Reprogramming makes indication from 0 to 15 and in case of multiplexing from 00 to 99 possible.

- Automatic reset
- Reprogrammable 0 to 15 and 1 to 16
- Strict binary decoding
- Input memory (LATCH)

Type	Ordering code	Package outline
SAB 3211	Q 67100—Y440	DIP 16

Maximum ratings (all voltages referred to V_{DD})

Supply voltage	V_{SS}	−0.3 to 18	V
Input voltage	V_i	$V_{SS}-18$ to $V_{SS}+0.3$	V
Power dissipation per output	P_q	100	mW
Total power dissipation	P_{tot}	500	mW
Output voltage	V_q	$V_{SS}-18$ to $V_{SS}+0.3$	V
Storage temperature range	T_{stg}	−55 to 125	°C

Range of operation (referred to V_{DD})

Supply voltage range (final stage not connected)	V_{SS}	11 to 16	V
Ambient temperature range	T_{amb}	0 to 70	°C

Characteristics (all voltages referred to V_{DD})

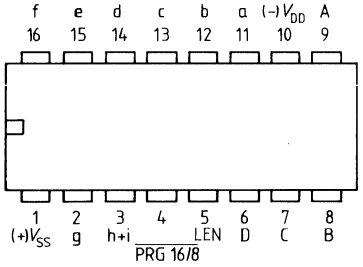
		min	typ	max	
Current input (Final stages not connected)	I_{DD}		0.3	5	mA
Input voltage for					
inputs A, B, C, D, Latch, Enable, LEN	V_{iH}	$V_{SS}-3$		V_{SS}	V
	V_{iL}	0		$V_{SS}-8$	V
Output voltage for					
outputs a, b, c, d, e, f, g (I_{Load} = 10 mA)	V_{qH}	$V_{SS}-3$	$V_{SS}-1.2$	V_{SS}	V
outputs (h + i) (I_{Load} = 20 mA[1])	V_{qH}	$V_{SS}-3$		V_{SS}	V
Leakage current — outputs a...(h + i) ($V_q = V_{DD}$)	I_{qL}		0.05	50	µA
Programming input (Input current required $I_{iH} \leqq 200$ µA)	V_{iH}	$V_{SS}-1$		V_{SS}	V
	V_{iL}	0		$V_{SS}-10$	V
as output for					
decoding channel 16 or 8 ($I_{Load} \leqq 100$ µA)	V_{qH}	$V_{SS}-1$	$V_{SS}-0.25$	V_{SS}	V
($I_{Load} \leqq$ 1 µA)	V_{qL}	0		0.4	V

[1]) IC with I_{Load} = 15 mA or 30 mA, resp., available upon request

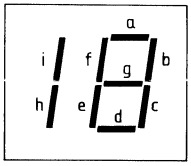
Pin designation

Pin No.	Description
1	V_{SS} positive supply voltage
2	Output to display segment g
3	Output to display segments h + i
4	Channel 16 display/programming input
5	Latch enable LEN
6	Binary input D
7	Binary input C
8	Binary input B
9	Binary input A
10	V_{DD} negative supply voltage
11	Output to display segment a
12	Output to display segment b
13	Output to display segment c
14	Output to display segment d
15	Output to display segment e
16	Output to display segment f

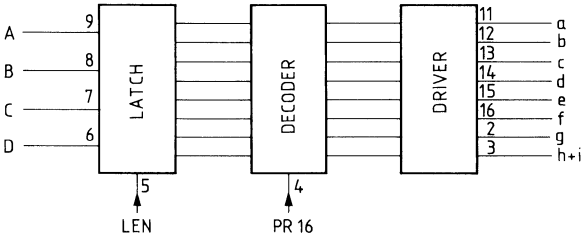
Pin configuration (top view)



Pin arrangement 9 segment display



Block diagram



Description of functions

The circuit is intended, e.g. to control a 9 segment program display at a TV set whereby the channel Nos. 1 to 16 are displayed. At channel No. 16 an additional signal is output which can be used for AV changeover of the TV set (fig. 1). Decoding is based on the straightforward binary code, indicating "16" instead of zero.

By changing the external wiring, the device can also be used for TV sets with 8 channels (fig. 2). In this case "8" is displayed instead of zero and the AV changeover signal appears with the display of channel 8.

It is possible to reprogram the circuit for general applications via the connection that would issue the AV changeover signal. If this connection is wired to the positive pole of the supply voltage, a "0" is indicated at the binary zero. The character set then comprises 0 to 15 in accordance with the simple 4 bit binary code. The BCD code is only to be understood as a subset of this code; the circuit is thus made suitable for application in usual numerical displays (fig. 3 and 4).

As another particularity, the circuit includes input latches which can be made responsive at high level with the aid of an enable input. At low level they keep the information retained.

The inputs are high-ohmic MOS inputs. Supply voltage may vary between 11 and 16 Volts taking into consideration that the inputs are not allowed to become positive against the V_{SS} connection since otherwise safety resistors would become necessary at the inputs.

The brightness of the display can be adjusted via the external current limiting resistors.

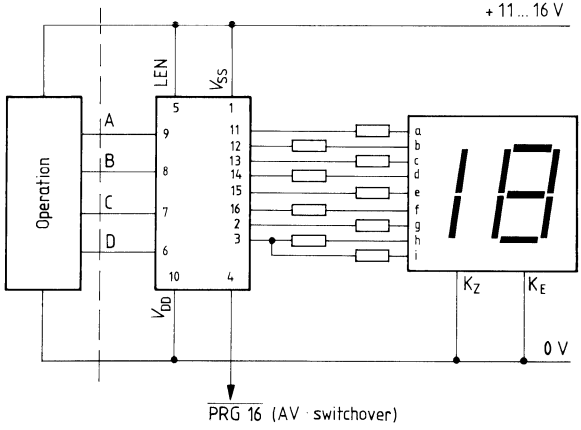
For the purpose of darkening the display, it is recommended to disconnect the cathode line of the display or the negative pole of the supply voltage (V_{DD}).

Truth table

Display	LEN	Inputs				Outputs									
		D	C	B	A	a	b	c	d	e	f	g	h+i	*	**
0	H	L	L	L	L	H	H	H	H	H	H	L	L		H[1])
1	H	L	L	L	H	L	H	H	L	L	L	L	L	H	
2	H	L	L	H	L	H	H	L	H	H	L	H	L	H	
3	H	L	L	H	H	H	H	H	H	L	L	H	L	H	
4	H	L	H	L	L	L	H	H	L	L	H	H	L	H	
5	H	L	H	L	H	H	L	H	H	L	H	H	L	H	
6	H	L	H	H	L	H	L	H	H	H	H	H	L	H	
7	H	L	H	H	H	H	H	H	L	L	L	L	L	H	
8	H	H	L	L	L	H	H	H	H	H	H	H	L	H	
9	H	H	L	L	H	H	H	H	H	L	H	H	L	H	
10	H	H	L	H	L	H	H	H	H	H	H	L	H	H	
11	H	H	L	H	H	L	H	H	L	L	L	L	H	H	
12	H	H	H	L	L	H	H	L	H	H	L	H	H	H	
13	H	H	H	L	H	H	H	H	H	L	L	H	H	H	
14	H	H	H	H	L	L	H	H	L	L	H	H	H	H	
15	H	H	H	H	H	H	L	H	H	L	H	H	H	H	
16	H	L	L	L	L	H	L	H	H	H	H	H	H	L	
	L	X	X	X	X	Display according to the input status A...D ahead of the H/L slope at LEN									
		X: as required													

[1]) forced on H from outside
* PRG 16/8 (as output high-ohmically loaded)
** PRG 16/8 (as input)

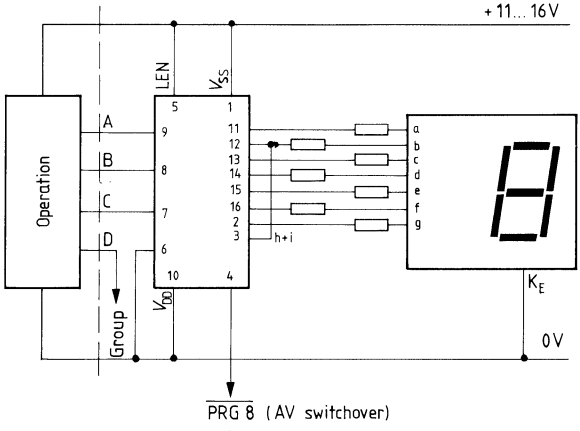
Fig. 1
Program display 16 channels



All resistors approx. 1.2 kΩ

D	C	B	A	Display	AV
L	L	L	L	16	L
L	L	L	H	1	H
L	L	H	L	2	H
L	L	H	H	3	H
L	H	L	L	4	H
L	H	L	H	5	H
L	H	H	L	6	H
L	H	H	H	7	H
H	L	L	L	8	H
H	L	L	H	9	H
H	L	H	L	10	H
H	L	H	H	11	H
H	H	L	L	12	H
H	H	L	H	13	H
H	H	H	L	14	H
H	H	H	H	15	H

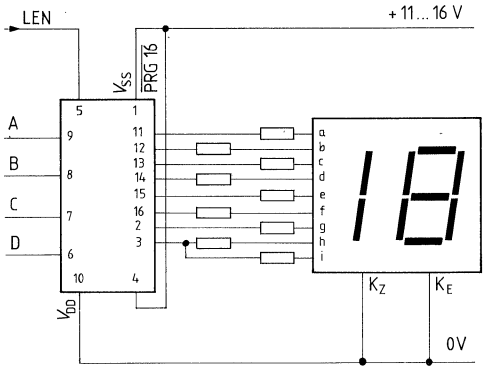
Fig. 2
Program display 8 channels



All resistors approx. 1.2 kΩ

D	C	B	A	Display	AV
L	L	L	L	8	L
L	L	L	H	1	H
L	L	H	L	2	H
L	L	H	H	3	H
L	H	L	L	4	H
L	H	L	H	5	H
L	H	H	L	6	H
L	H	H	H	7	H
L	L	L	L	8	L
L	L	L	H	1	H
L	L	H	L	2	H
L	L	H	H	3	H
L	H	L	L	4	H
L	H	L	H	5	H
L	H	H	L	6	H
L	H	H	H	7	H

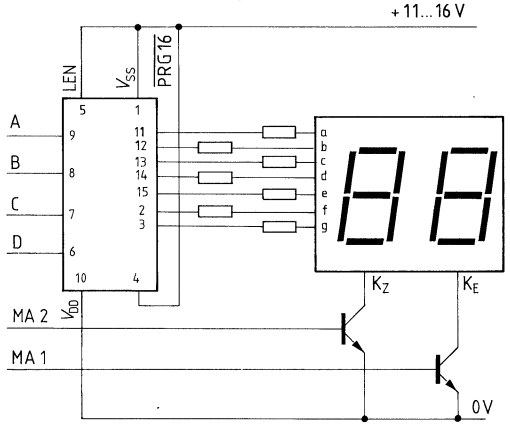
Fig. 3
Binary display 0 to 15 (thus also BCD 0 to 9)



All resistors approx. 1.2 kΩ

D	C	B	A	Display
L	L	L	L	0
L	L	L	H	1
L	L	H	L	2
L	L	H	H	3
L	H	L	L	4
L	H	L	H	5
L	H	H	L	6
L	H	H	H	7
H	L	L	L	8
H	L	L	H	9
H	L	H	L	10
H	L	H	H	11
H	H	L	L	12
H	H	L	H	13
H	H	H	L	14
H	H	H	H	15

Fig. 4
Multiplexer display BCD 00 to 99



All resistors approx. 1.2 kΩ

MOS circuit

The SAB 3211 Z, developed in MOS depletion technology, represents an addition to the SAB 3211.
It is particularly suitable for direct coding binary +1.

- Input memory
- Decoding binary +1
- Additional decoding channel 16

Type	Ordering code	Package outline
SAB 3211 Z	Q 67100-Y 466	DIP 16

Maximum ratings (all voltages referred to V_{DD})

Supply voltage range	V_{SS}	−0.3 to 18	V
Input voltage	V_i	$V_{SS}-18$ to $V_{SS}+0.3$	V
Power dissipation per output	P_q	100	mW
Total power dissipation	P_{tot}	500	mW
Output voltage	V_q	$V_{SS}-18$ to $V_{SS}+0.3$	V
Storage temperature range	T_{stg}	−55 to 125	°C

Range of operation (referred to V_{DD})

Supply voltage range (final stages unconnected)	V_{SS}	11 to 16	V
Ambient temperature range	T_{amb}	0 to 70	°C

Characteristics (all voltages referred to V_{DD})

		min	typ	max	
Current consumption	I_{DD}			1.5	mA
Input voltage for inputs A, B, C, D	V_{iH}	$V_{SS}-3$		V_{SS}	V
Enable, LEN	V_{iL}	0		$V_{SS}-8$	V
Output voltage for outputs a, b, c, d, e, f, g (I_{load} = 15 mA)	V_{qH}	$V_{SS}-3.5$		V_{SS}	V
Output voltage for outputs h, i (I_{load} = 30 mA)	V_{qH}	$V_{SS}-3.5$		V_{SS}	V
Leakage current outputs a ... (h + i) ($V_q = V_{DD}$)	I_{qL}		0.05	20	µA
Output for decoding channel 16 (I_{load} < 100 µA)	V_{qH}	$V_{SS}-1$		V_{SS}	V
(I_{load} < 1 µA)	V_{qL}	0		0.4	V

Circuit description

LED display latch decoder driver for 7- or 9-segment display with common cathode

The circuit is intended, e.g., to control a 9-segment program display at a TV set whereby the channel Nos. 1 to 16 are displayed. At channel No.16 an additional signal is output which can be used for AV changeover of the TV set (fig. 1).

Decoding is done by indicating the number of the direct binary code incremented by 1, each (refer to truth table).

As particularity the circuit includes input latches which can be made responsive at high level with the aid of an enable input (LEN). At low level they keep the information retained.

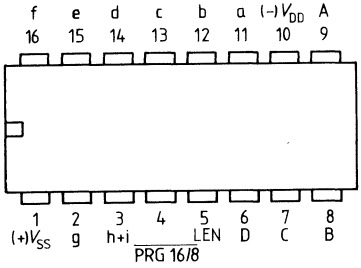
The inputs are high-ohmic MOS inputs. Supply voltage may vary between 11 and 16 Volts taking into consideration that the inputs are not allowed to become positive against the V_{SS} connection since otherwise safety resistors (min 500 kΩ) would become necessary at the inputs.

The brightness of the display can be adjusted via the external current limiting resistors. For the purpose of darkening the display, it is recommended to disconnect the cathode line of the display or the negative pole of the supply voltage (V_{DD}).

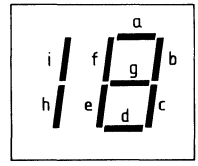
Truth table

Display	LEN	Inputs D	C	B	A	Outputs a	b	c	d	e	f	g	h+i	$\overline{\text{PRG 16}}$ high-ohmically loaded
1	H	L	L	L	L	L	H	H	L	L	L	L	L	H
2	H	L	L	L	H	H	H	L	H	H	L	H	L	H
3	H	L	L	H	L	H	H	H	H	L	L	H	L	H
4	H	L	L	H	H	L	H	H	L	L	H	H	L	H
5	H	L	H	L	L	H	L	H	H	L	H	H	L	H
6	H	L	H	L	H	H	L	H	H	H	H	H	L	H
7	H	L	H	H	L	H	H	H	L	L	L	L	L	H
8	H	L	H	H	H	H	H	H	H	H	H	H	L	H
9	H	H	L	L	L	H	H	H	H	L	H	H	L	H
10	H	H	L	L	H	H	H	H	H	H	H	L	H	H
11	H	H	L	H	L	L	H	H	L	L	L	L	H	H
12	H	H	L	H	H	H	H	L	H	H	L	H	H	H
13	H	H	H	L	L	H	H	H	H	L	L	H	H	H
14	H	H	H	L	H	L	H	H	L	L	H	H	H	H
15	H	H	H	H	L	H	L	H	H	L	H	H	H	H
16	H	H	H	H	H	H	L	H	H	H	H	H	H	L
	L	X	X	X	X	Display according to A... D status prior to the H/L slope of the LEN signal								

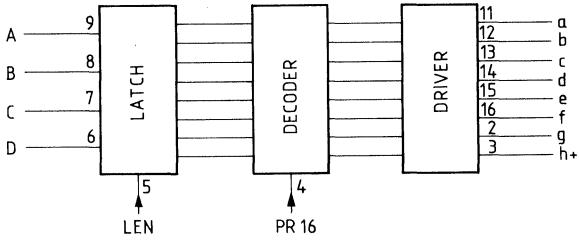
Pin configuration (top view)



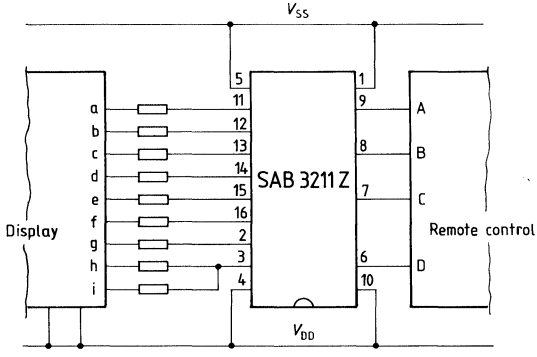
Pin arrangement in 9 segment display



Block diagram



Program display 16 channels



D	C	B	A	Display	$\overline{\text{PRG 16}}$ (AV)
H	H	H	H	16	L
L	L	L	L	1	H
L	L	L	H	2	H
L	L	H	L	3	H
L	L	H	H	4	H
L	H	L	L	5	H
L	H	L	H	6	H
L	H	H	L	7	H
L	H	H	H	8	H
H	L	L	L	9	H
H	L	L	H	10	H
H	L	H	L	11	H
H	L	H	H	12	H
H	H	L	L	13	H
H	H	L	H	14	H
H	H	H	L	15	H

MOS circuit

The IC SAB 3271 is a straightforward infrared receiver for the Siemens IR remote control system. It includes the receiver part, the output shift register with one series output and 6 parallel outputs, 1 start bit output/input, 1 T flip-flop output, 1 RS flip-flop output, a circuit for single and repeat enable signals and a changeover for the parallel outputs (see block diagram).

At first the incoming infrared instruction is checked, then read into the shift register, switched to the parallel outputs and then serially output as I bus.

Type	Ordering code	Package outline
SAB 3271	Q67100-Y461	DIP 16

Maximum ratings (all voltages referred to V_{DD})

Supply voltage range	V_{SS}	−0.3 to 18	V
Input voltage	V_i	$V_{SS}-18$ to $V_{SS}+0.3$	V
Power dissipation per output	P_q	100	mW
Total power dissipation	P_{tot}	500	mW
Storage temperature range	T_{stg}	−55 to 125	°C

Range of operation (referred to V_{DD})

Supply voltage range	V_{SS}	11 to 16	V
Ambient temperature range	T_{amb}	0 to 70	°C

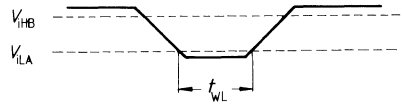
Characteristics (all voltages referred to V_{DD}; T_{amb} = 25 °C)

		min	typ	max	
Supply current (V_{SS} = 16 V, outputs not connected)	I_{DD}		5	10	mA
Oscillator frequency range	f_{osc}	20	62.5	70	kHz
Infrared signal input					
H-input voltage (quiescent level)	V_{iH}	$V_{SS}-1$ V		V_{SS}	
L-input voltage	V_{iL}	0		$V_{SS}-3.5$	V
L-pulse width	t_{wL}	2			µs
Input resistance	R_i	0.2			MΩ
Parallel outputs					
Q_A, Q_B, Q_C, Q_D, Q_E, Q_F; T F-F output Q_1 SU, Q_3; RS F-F outputs Q_2; I bus outputs DATA, DLER, DLES					
H-output voltage (I_D = +1 µA)	V_{qH}	$V_{SS}-0.4$V		V_{SS}	
L-output voltage (I_D = −1 µA)	V_{qL}	0		0.4	V
H-output voltage (I_D = +300 µA)	V_{qH}	$V_{SS}-1$V		V_{SS}	
L-output voltage (I_D = −5 µA)	V_{qL}	0		3	V

RSIG infrared signal input

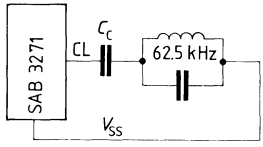
Timing diagram

Input signals



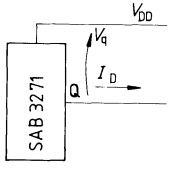
CL oscillator connection

Circuitry:



Coupling capacitor	C_C	$\geq$ 10 nF
Coil	L	= 10 mH
Capacitance	C	= 680 pF

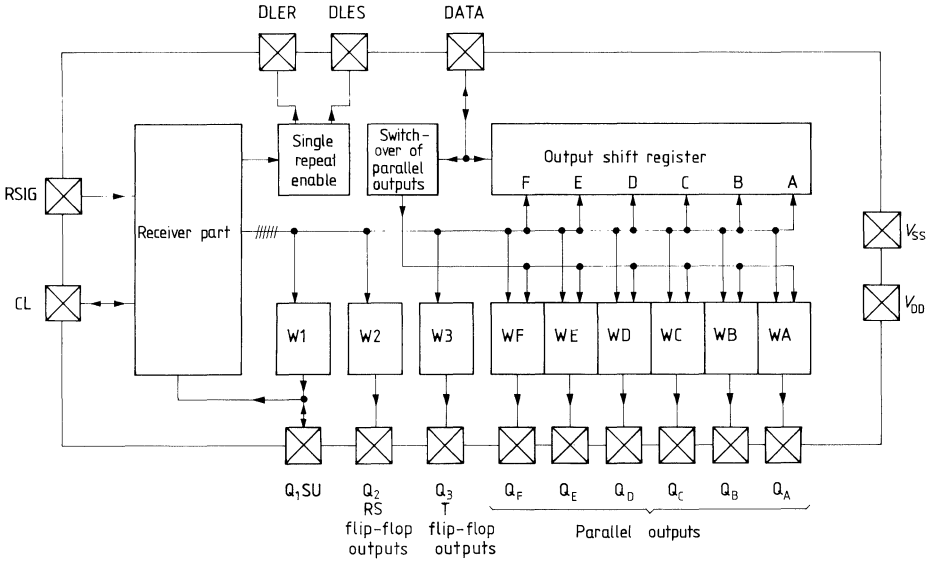
Q_A, Q_B, Q_C, Q_D, Q_E, Q_F parallel outputs
Q_1SU, Q_2 RS flip-flop outputs; Q_3 T flip-flop-output



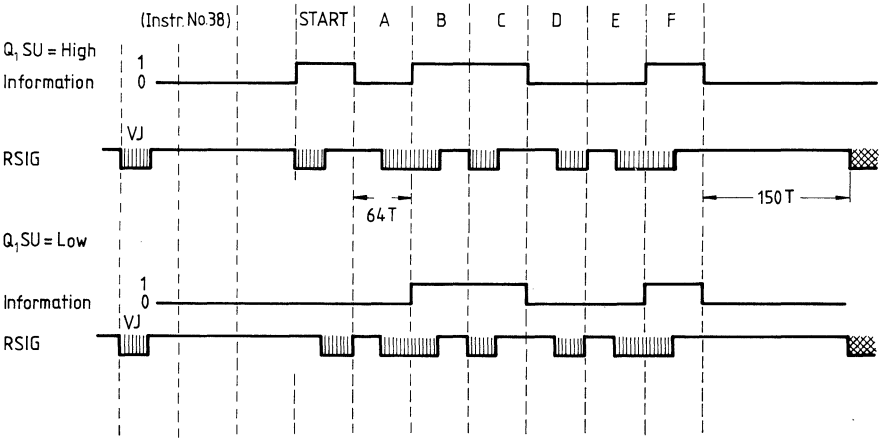
Pin designation

Pin No.	Description
1	V_{SS}
2	CL oscillator
3	Q_1SU start bit changeover
4	Q_2 RS flip-flop output
5	Q_3 T flip-flop output
6	RSIG infrared input
7	DATA series output
8	Q_A } parallel outputs
9	Q_B
10	Q_C
11	Q_D
12	Q_E
13	Q_F
14	V_{DD}
15	DLER repeat } valid signal
16	DLES single

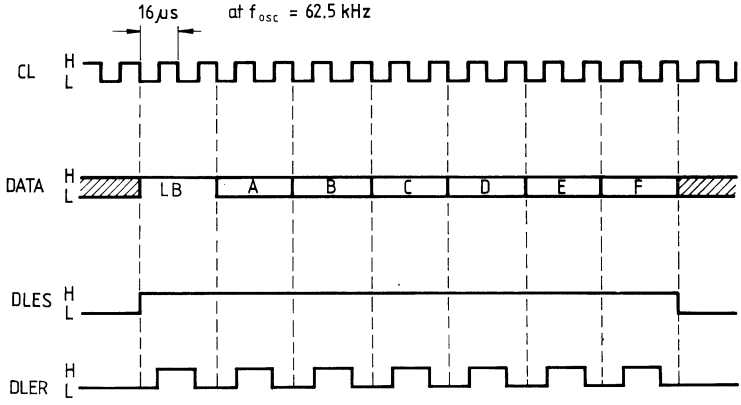
Block diagram



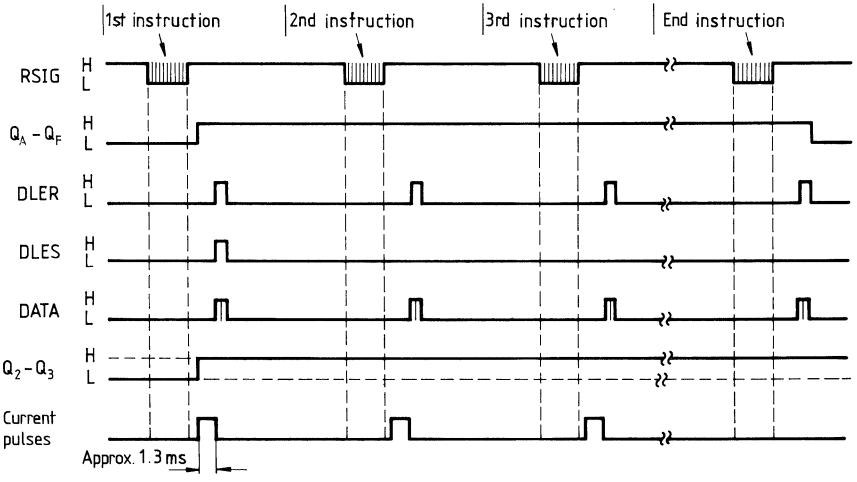
Biphase coding, timing diagram



I Bus timing diagram



Infrared signal and output signals



Instruction table

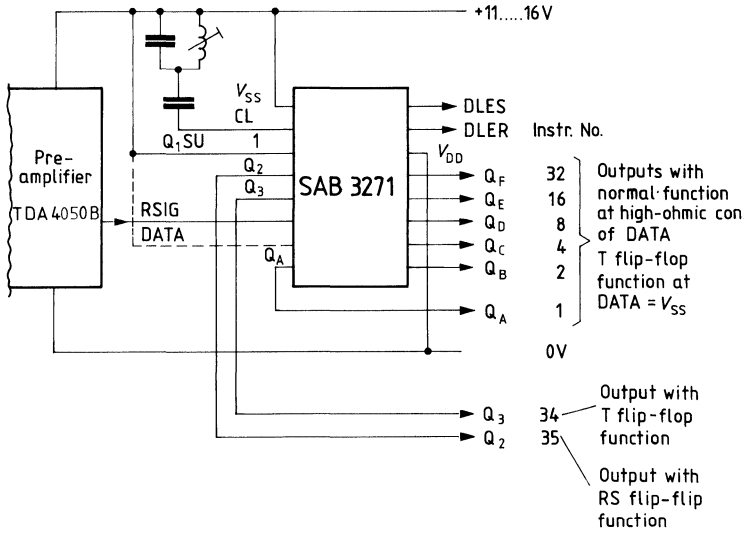
Instr. No.	Code F E D C B A	Instr. No.	Code F E D C B A	Instr. No.	Code F E D C B A	Instr. No.	Code F E D C B A
0	L L L L L L [1]	16	L H L L L L [2]	32	H L L L L L [2]	48	H H L L L L
1	L L H [2]	17	L L H	33	L L H Q_1 SU [3]	49	L L H
2	L H L [2] Q_2 L	18	L H L	34	L H L Q_2 H [3]	50	L H L
3	L H H	19	L H H	35	L H H Q_3 [3]	51	L H H
4	H L L [2]	20	H L L	36	H L L	52	H L L
5	H L H	21	H L H	37	H L H	53	H L H
6	H H L	22	H H L	38	H H L	54	H H L
7	H H H	23	H H H	39	H H H	55	H H H
8	L L H L L L [2]	24	L H H L L L	40	H L H L L L	56	H H H L L L
9	L L H	25	L L H	41	L L H	57	L L H
10	L H L	26	L H L	42	L H L	58	L H L
11	L H H	27	L H H	43	L H H	59	L H H
12	H L L	28	H L L	44	H L L	60	H L L
13	H L H	29	H L H	45	H L H	61	H L H
14	H H L	30	H H L	46	H H L	62	H H H H H L end
15	H H H	31	H H H	47	H H H	63	instruction not allowed

[1]) is simultaneously quiescent position at the parallel outputs, i.e. this instruction can only be used at the parallel outputs in connection with DLER or DLES, respectively, whereby this coding also applies to the instructions 33, 34, 35 (see 3).

[2]) In case of these instructions, only 1 bit is on high level, see section "Operation as Remote Control Receiver".

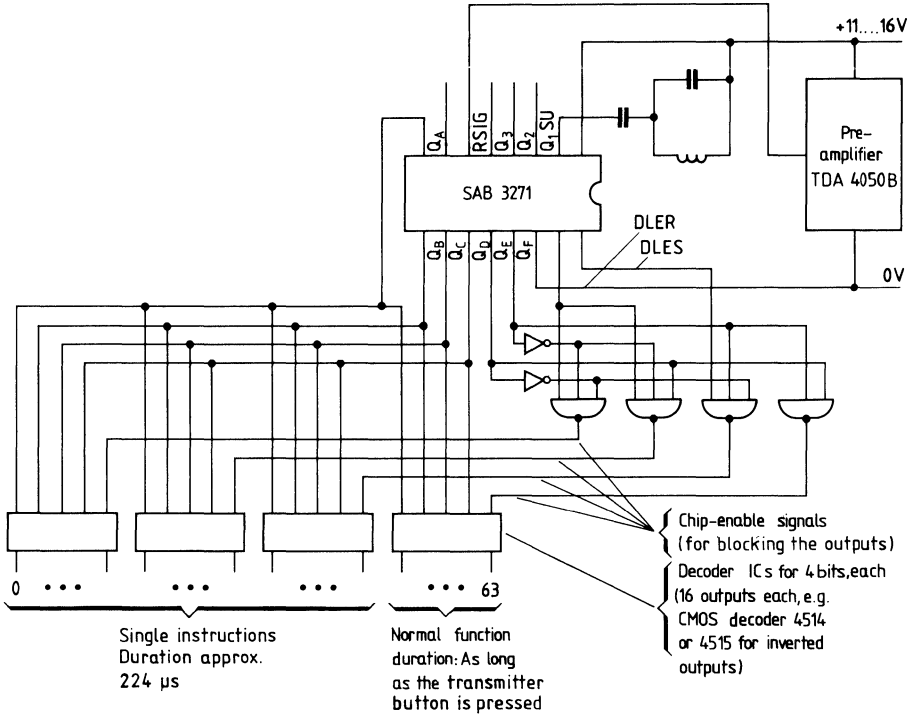
[3]) These instructions are blocked for the parallel output in order to have 9 channels available for remote control without decoder. The parallel outputs remain in quiescent position, whereas the serial interface outputs also these instructions without peculiarities.

Application circuit as receiver for 8 channels



[1])Plotted version: Operation with start bit = 1
For operation with start bit = 0, the terminal Q_1SU must be wired to V_{DD} (= 0 V).

Example for a decoder circuit



With this circuit all instructions of the instruction table but the end instruction (instr. No. 62) and the not allowed instruction (instr. No. 63) can be obtained in decoded form, whereby instructions 33, 34, and 35 are already decoded in the circuit (outputs Q_1SU, Q_2, Q_3). If DLES is used, single instructions or the normal function will be generated.

Description of functions

Receiver (RSIG, Q_1SU)

The receiver checks the infrared signal (1 prepulse + 1 start bit + 6 information bits, refer to fig.) transmitted in biphase code. The receiver can be changed over to both kinds of start bits: in case of an infrared signal with the start bit = 0, the start bit terminal Q_1SU must be connected to low level, with the start bit = 1 to high level. Between the prepulse and the start bit a muting test is performed. Then, reading-in and checking of the code word follow. After a second muting test, the output begins. During this period of time the infrared input is blocked, thus no interfering pulse may interrupt the output procedure.

If an interference is recognized in the infrared signal, only this interfered instruction (within several repeat instructions) will not be interpreted (same behavior as in the case of a missing instruction).

Parallel outputs (Q_A.... Q_F)

At the first repeat instruction the code word is switched to the parallel outputs Q_A to Q_F with 1 = high and 0 = low. The parallel outputs then remain in this state as long as the transmitting button is pressed. Only after receipt of the end instruction (when releasing the button), they are again reset to low (refer to fig. "Infrared signal and output signals"). Also refer to the section "Operation as remote control receiver without external decoder". The end instruction (No. 62) and the instructions 33, 34, 35 are suppressed for the parallel outputs.

RS flip-flop output (Q_2)

The RS flip-flop output Q_2 is set with the instruction 34 and reset with the instruction 2, which also acts upon the parallel output Q_2. The output can also be directly set and reset at the terminal with a low-ohmic connection.
If the output is low-ohmically applied to low level, e.g. via the base-emitter path of an NPN transistor, it issues at transmitting the instruction No. 34 base current pulses of approximately 1.3 msec duration in the interval of the repeat instructions transmitted. If a PNP transistor is applied towards high level, base current pulses can also be obtained during transmitting the instruction No. 2, thus however, also influencing the output Q_B.

T flip-flop output (Q_3)

The T flip-flop output (Q_3) changes its state at every pressure on the corresponding transmitting button (see instruction table) and keeps the new position until the button is pressed anew. This output can also be set and reset directly in the same way as the output Q_2. At the next appropriate instruction of the remote control, the output again changes its state.

When the output is low-ohmically connected, e.g. via the base-emitter path of a transistor to high (PNP transistor) or to low (NPN transistor), current pulses of about 1.3 ms duration are output during pressure of the appropriate transmitting button at an interval of the transmitted repeat instructions (pulse function, refer to fig.).

Pulse output Q_1SU

The output Q_1SU is on the one hand the input for the start bit changeover; on the other hand also current pulses may be coupled at this output via a transistor as also described for the output Q_3. Refer to figure "Pulse function".

Serial interface (DATA, DLER, DLES)

After the received instruction word has been switched to the parallel outputs Q_A to Q_F and the 3 special outputs Q_1SU, Q_2 and Q_3, output at the serial interface takes place via the outputs DATA (information) and DLER (enable and clock for repeat instructions). The end instruction (No. 62) and the instructions 33, 34, and 35 are also output at the serial interface. The output DLS (enable for single instructions) only moves to high during the output of one instruction (No. 62). Refer to figure "I bus timing diagram" and "Infrared signal and output signals".

Operation as remote control receiver without external decoder

The instruction table includes 6 instructions, only one bit of which equals high and the remaining 5 bits equal low. They actually effect only one of the 6 parallel outputs. Together with the RS flip-flop output and the T flip-flop start-bit terminal a remote control, comprising nine independent channels is thus possible. The parallel outputs can thereby be operated in 2 different modes of operation:

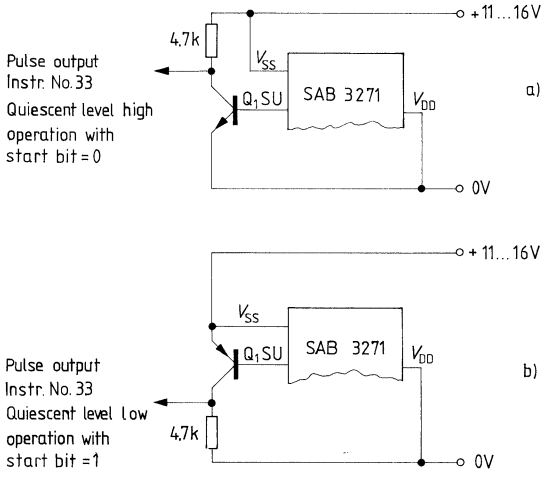
a) When the DATA output is subject to high-ohmic load, only (normal case), each of the 6 parallel outputs alone moves to high as long as the according button is being pressed.

b) The parallel outputs may also be operated as T flip-flops. For that purpose, the DATA terminal must be put to high level (that can also be done via the base-emitter path of a PNP transistor, if the I bus information shall not be lost — refer to fig.). The outputs then work like the described T flip-flops, i. e. they can be individually set and reset from outside or individually changed over to the pulse function by a low-ohmic load.

Switching-on

When the supply voltage rises, the parallel output, the start-bit output Q_1SU, the RS flip-flop output Q_2, and the T flip-flop output Q_3 are put to low level.

Pulse function, with channel Q_1SU taken as an example



The circuit configured to a) can also be applied without restriction at the RS flip-flop output Q_2, the T flip-flop output Q_3 and the parallel outputs Q_A to Q_F in order to change the outputs individually to the pulse function.

The circuit configured according to b) can also be used at the RS flip-flop output Q_2, the T flip-flop output Q_3 and, if DATA is connected to high at the parallel outputs Q_A to Q_F. Also the DATA output can be moved to high level with this circuit in order not to loose the I bus information at this mode of operation.

MOS circuit

The SDA 3205 receiver IC, developed in P-MOS depletion technology, interprets the IR signals of the transmitter IC SDA 3206.

With the SDA 3205, 16 programs and 1 analog function can be selected. Moreover, the IC contains an on/off input or output, respectively.

- The program outputs are short-circuit proof and can be externally set.
- The SDA 3205 can be operated with the on-chip oscillator or with an external clock.

Type	Ordering code	Package outline
SDA 3205	Q 67100-Y578	DIP 18

Maximum ratings (all voltages referred to V_{DD} = 0 V)

Supply voltage range	V_{SS}	−0.3 to 18	V
Input voltage	V_i	V_{SS} − 18 to V_{SS} + 0.3	V
Total power dissipation	P_{tot}	500	mW
Power dissipation per output	P_q	100	mW
Thermal resistance (system-air)	$R_{th\ SA}$	90	K/W
Storage temperature range	T_{stg}	−40 to 125	°C

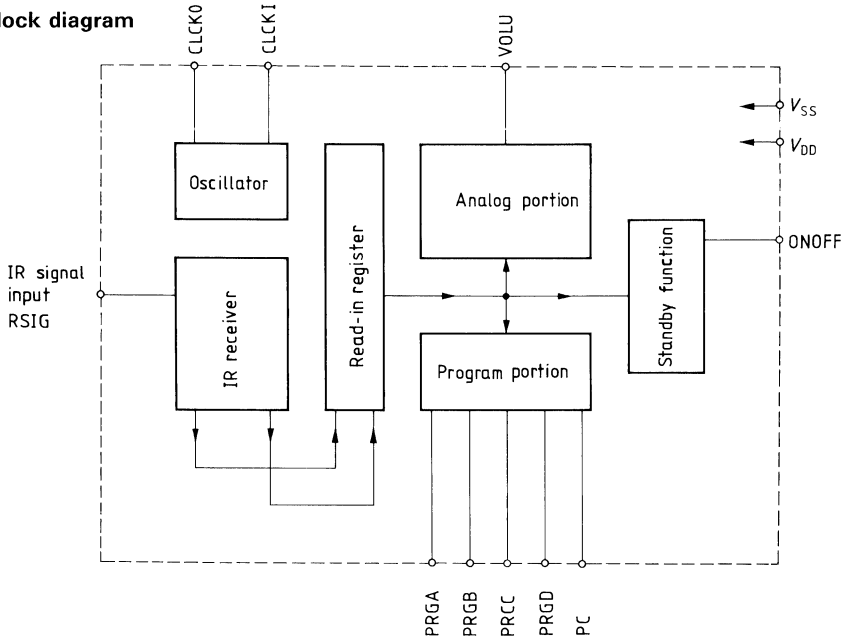
Range of operation (referred to V_{DD} = 0 V)

Supply voltage range	V_{SS}	−16 to −11	V
Ambient temperature range	T_{amb}	0 to 70	°C

Characteristics (referred to V_{DD} = 0 V, T_{amb} = 0 to 70 °C)

		min	typ	max	
Current consumption (outputs open)	I_{DD}		5	10	mA
Inputs Clock input CLCKI					
L-input voltage	V_{iL}	0		$V_{SS}-7$	V
H-input voltage	V_{iH}	$V_{SS}-1$		V_{SS}	V
Input current	I_i			15	µA
Transition times	t_{THL}, t_{TLH}			4	µs
Frequency	f	20	60	70	kHz
Remote control signal input RSIG					
Input alternating voltage	V_{iH}	$V_{SS}-1$		V_{SS}	V
	V_{iL}	0		$V_{SS}-3.5$	V
Input resistance	R_i	0.2			MΩ
Inputs Program stepping input PC					
H-input voltage	V_{iH}	$V_{SS}-1.5$		V_{SS}	V
L-input voltage	V_{iL}	0		$V_{SS}-7$	V
H-input current ($V_i = V_{SS}$) (internal pull low resistor)	I_{iH}			10	µA
Standby output ONOFF					
H-input voltage (I_{iH} <1 mA)	V_{iH}	$V_{SS}-1$ V		V_{SS}	V
Outputs Program memory outputs PRGA, PRGB, PRGC, PRGD					
H-output voltage (I_q = 0.1 mA)	V_{qH}	$V_{SS}-0.5$		V_{SS}	V
L-output voltage (I_q = 10 µA)	V_{qL}	0		1	V
Program stepping output PC					
H-output voltage (I_q = 0.3 mA)	V_{qH}	$V_{SS}-1.5$		V_{SS}	V
L-output voltage (no load)	V_{qL}	0		2	V
Analog functions output VOLU					
H-output voltage (I_q = 1 mA)	V_{qH}	$V_{SS}-1.5$		V_{SS}	V
L-output voltage (I_q = 1 µA)	V_{qL}	0		0.35	V
Standby output ONOFF					
H-output voltage (I_q = 0.3 mA)	V_{qH}	$V_{SS}-1.5$		V_{SS}	V
L-output voltage (I_q = 1 µA)	V_{qL}	0		0.35	V
Clock output CLCKO					
H-output voltage (no load)	V_{qH}	$V_{SS}-1$		V_{SS}	V
L-output voltage (no load)	V_{qL}	0		1	V

Block diagram



Pin designation

Pin No.	Description
1	V_{SS}, supply voltage
2	CLCKO, clock output
3	CLCKI, clock input
4	PRGD, program control output
5	PRGC, program control output
6	PRGB, program control output
7	PRGA, program control output
8	PC, program change strobe output
9	
10	VOLU, volume control output
11	ONOFF, standby output
12	
13	
14	
15	RSIG, IR input
16	
17	V_{DD}, supply voltage
18	

Pins 9, 12, 13, 14, 16, and 18 are not allowed to be connected.

Circuit description

1. IR receiver (pin RSIG)

The IR receiver takes the IR signal, decodes it and moves it to the control logic. The IR signal consists of ac pulses with a frequency of approx. 30 kHz and a duration of 0.5 ms per cycle. The instructions are transmitted as 7 bit words (1 start bit, 6 information bits). The IR signals are repeated approximately every 120 ms.

2. Analog value memory (output VOLU)

The analog value can be varied in approx. 60 steps. The variation speed is according to the repetition frequency of the repeat instruction (approx. 8 Hz). The analog value is output as square-wave voltage with a frequency of approx. 1 kHz, whereby the duty cycle corresponds to the analog value. The analog voltage is generated in an external low pass filter.

If the supply voltage rises from 0 the analog value is set to the start position
($\nu_{VOLU} = 1/3$, with $\nu = t_{high}/T$).

The output is internally kept to low

- if the IC is in standby,
- for approx. 128 ms if a program + or program — instruction has been received, before the high pulse of the PC output will be issued.

As long as the IC is in standby, instructions to the analog memory remain undecoded. After switch-on from standby, the analog output is set to the start position.

3. Program memory (outputs and inputs PRGA, PRGB, PRGC, PRGD)

The programm memory consists of a 4 bit ring counter to call 16 programs. The 16 programs can be called via remote control by incrementing or decrementing with the ring counter.

If the supply voltage rises from 0, the program outputs are set to LLLH. The outputs can be used as inputs. They can be set and reset by low-ohmic external control.

Strobe output, program continuation input PC

When the program memory has received an instruction via remote control, a positive pulse appears at the output PC after a certain delay time. The volume output VOLU is muted as soon as the delay time starts. Muting is reverted with the trailing edge of the PC pulse (refer to timing diagram 1). A capacitor can be additionally connected to the output PC in order to prolong muting (up to approx. 0.5 sec.).

The same muting behavior appears when the supply voltage rises from zero and simultaneously the pin ONOFF is kept on low level (refer to timing diagram 2).

The pin PC can also be used as input. If positive potential is applied from outside, the program counter will increment by 1 step. The external capacitor thereby acts as debouncing (refer to timing diagram 3). In the state "Standby", the output is statically positive. The PC pulse only once appears per pressure on the according transmitter button.

4. Other control functions

Standby output/input:
(pin ONOFF)

The output is controlled by an RS flip-flop. The high level (standby) appears

— when the supply voltage is switched on
— when the instruction "standby" is received

The low level (on) appears, when the instruction program + or program — is received.

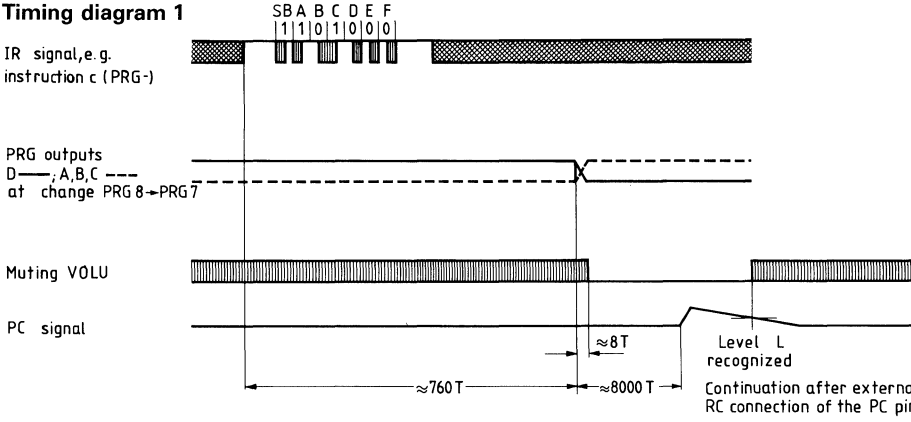
At low-ohmic control the pin ONOFF also acts as input.

Table

Instruction set for IR transmission

Instruction No.	Description
a	Standby
b	Program + / on
c	Program − / on
d	Vol +
e	Vol −
f	End instruction

Timing diagram 1

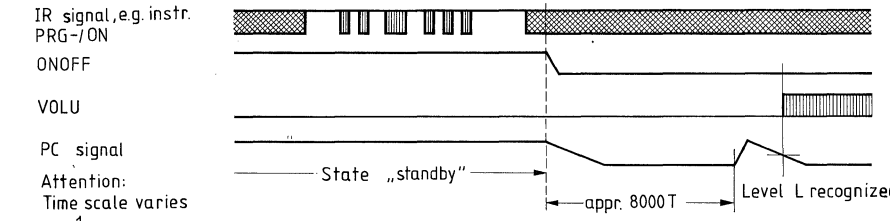


Attention: time scale varied

$T = \frac{1}{f_{osc}}$

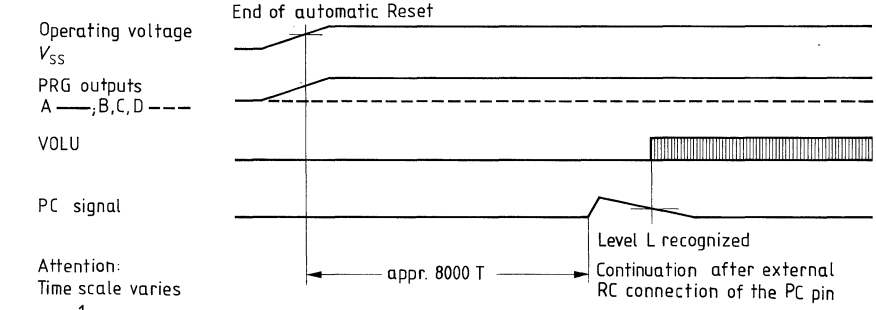
Timing diagram 2

Example a) Switching on by means of an IR instruction



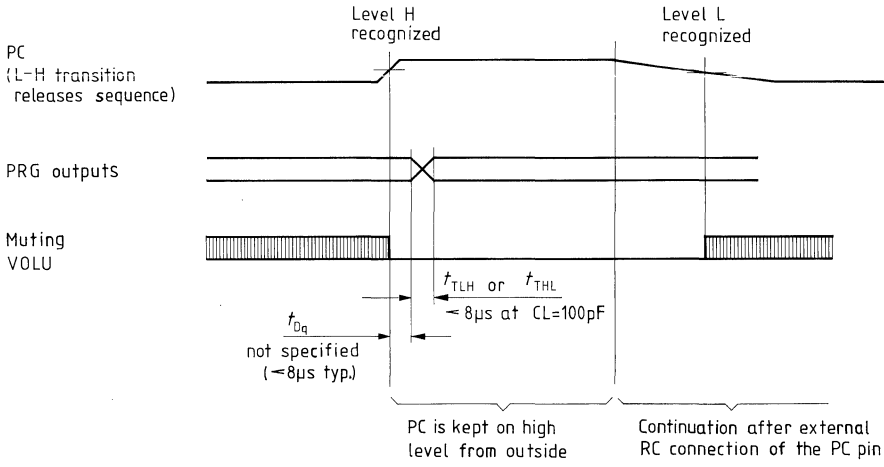
$T = \frac{1}{f_{osc}}$

Example b) ONOFF is connected to V_{DD} during the supply voltage rise via wiping contact

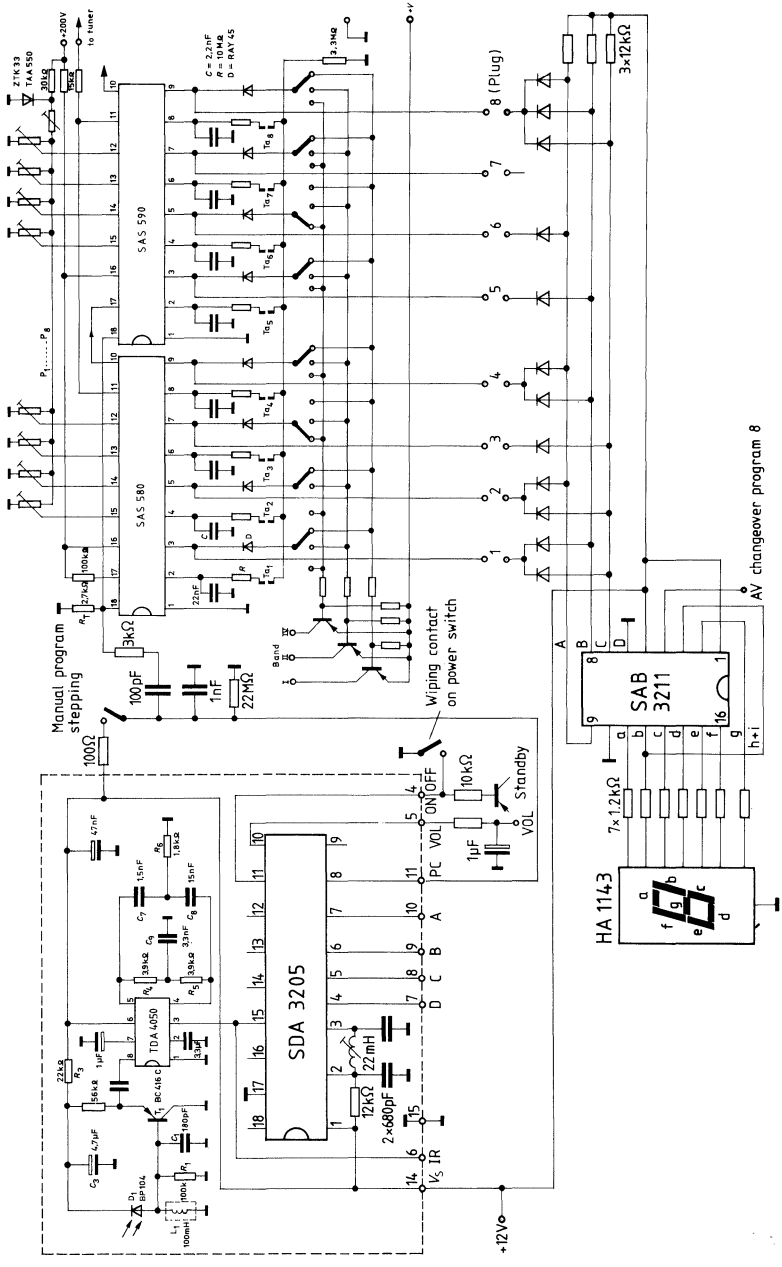


$T = \frac{1}{f_{osc}}$

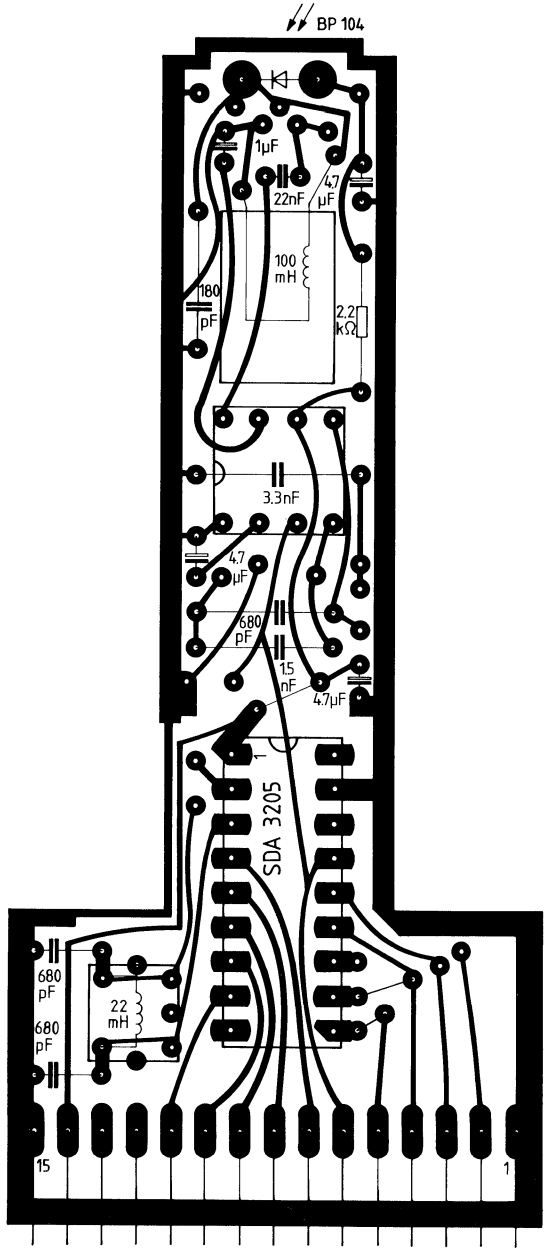
Timing diagram 3



Application circuit IR 60 V with program stepping and display of the program number



Layout


BP 104
1µF
22nF
4.7 µF
100 mH
180 pF
2.2 kΩ
3.3nF
4.7 µF
680 pF
15 nF
4.7µF
SDA 3205
680 pF
22 mH
680 pF
15
1

MOS circuit

The SDA 3206 transmitter IC, developed in P-MOS depletion technology, converts the input instructions into a 6-bit biphase code. The instructions are transmitted via an infrared transmitter stage onto an IR receiver stage of the SDA 3205.

- Low current consumption of typically 3 mA (max. 5 mA). An external NPN transistor, controlled by the transmitter IC, disconnects the battery from the IC, thus substantially increasing the battery life time.
- 5 V to 10 V supply voltage

Type	Ordering code	Package outline
SDA 3206	Q67100-Y577	DIP 18

Maximum ratings (all voltages referred to $V_{DD} = 0$ V)

Supply voltage	V_{SS}	−0.3 to 18	V
Input voltage	V_i	$V_{SS}-18$ to $V_{SS}+0.3$	V
Total power dissipation	P_{tot}	500	mW
Power dissipation per output	P_q	100	mW
Storage temperature range	T_{stg}	−55 to 125	°C
Thermal resistance (system-air)	$R_{th\ SA}$	90	K/W

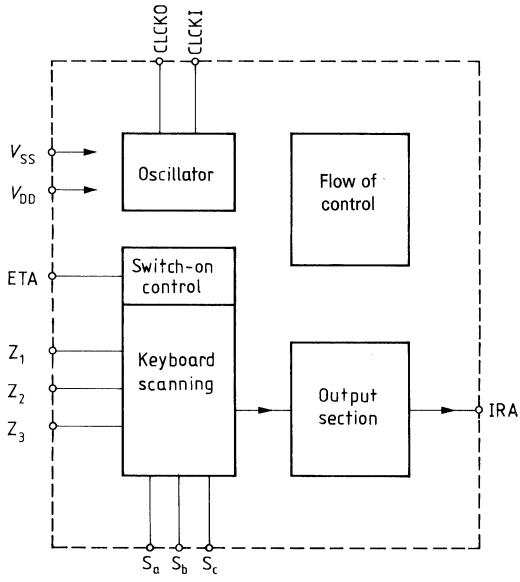
Range of operation (referred to $V_{DD} = 0$ V)

Supply voltage range	V_{SS}	5 to 10	V
Ambient temperature range	T_{amb}	0 to 70	°C

Characteristics (all voltages referred to $V_{DD} = 0$ V)

		min	typ	max	
Current consumption without load	I_{DD}		3	5	mA
Oscillator:					
Clock input CLCKI					
H-input voltage	V_{iH}	$V_{SS}-1$		V_{SS}	V
L-input voltage	V_{iL}	0		$V_{SS}-4$	V
Clock output CLCKO					
H-output voltage	V_{qH}	$V_{SS}-1$		V_{SS}	V
L-output voltage	V_{qL}	0		$+1$	V
Leakage current, total current					
of column output S_a, S_b, S_c, ETA, IRA ($V_q = -10$ V; $V_{SS} = 0$ V; $T_{amb} = 25$ °C)				1	µA
Column resistors					
R_a, R_b, R_c towards $-V_S$	R_C	33		47	kΩ
Remote control signal — output IRA					
H-output voltage ($I_{qH} = 4$ mA; $V_{SS} > 6$ V)	V_{qH}	$V_{SS}-5$		V_{SS}	V
Switch-on transistor — output ETA					
H-output current ($V_q = V_{SS} - 4$ V)	I_{qH}	0.1		0.5	mA

Block diagram



Pin designation

Pin. No.	Description
1	V_{SS}
2	Column a
3	Column b
4	Column c
5	
6	V_{DD}
7	ETA (switch-on transistor output)
8	IRA (infrared output)
9	Row 1
10	Row 2
11	Row 3
12	
13	
14	
15	
16	
17	CLCKI (oscillator input)
18	CLCKO (oscillator output)

Pins 5, 12, 13, 14, 15, 16 are not allowed to be connected.

Description of functions

The SDA 3206 works throughout a wide supply voltage range at low current consumption, it is, therefore, suitable for battery supply. The IC contains a control output for an NPN transistor, which disconnects the IC from the battery if no button is pressed.

Input keyboard:

The transmitter includes an input matrix containing 3 columns and 3 rows. A column output has to be connected to a row input in order to input an instruction. Thus, the transmitter is switched on and a corresponding instruction is transmitted.

End instruction:

After having actuated a button, the selected instruction is transmitted maximally once again, depending on the exact instant of the release. After the last transmission of the desired instruction the end instruction is transmitted which informs the receiver that the button was released.

Output:

The transmitter converts the incoming instruction into a biphase code (timing diagram 1). Prior to the 6 information bits, a start bit is transmitted.

The output signal is keyed with the clock frequency divided by 2 ($f_{CLCK}/2 \approx 30$ kHz); the signal controls an infrared transmitter stage. The idling output is high-ohmic. Prior to an IR instruction, a presignal is released which relieves the amplifier at the receiver side.

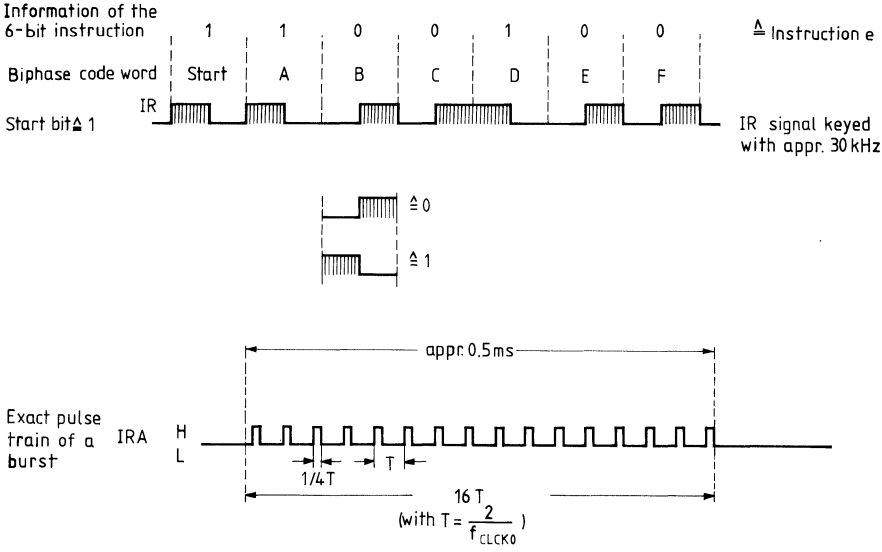
Timing:

The clock frequency is set to 60 kHz. The instructions are transmitted at an interval of approx. 120 msec, an instruction lasts approx. 7 msec (timing diagram 1). The instructions cannot be recognized before a debounce time of 20 msec.

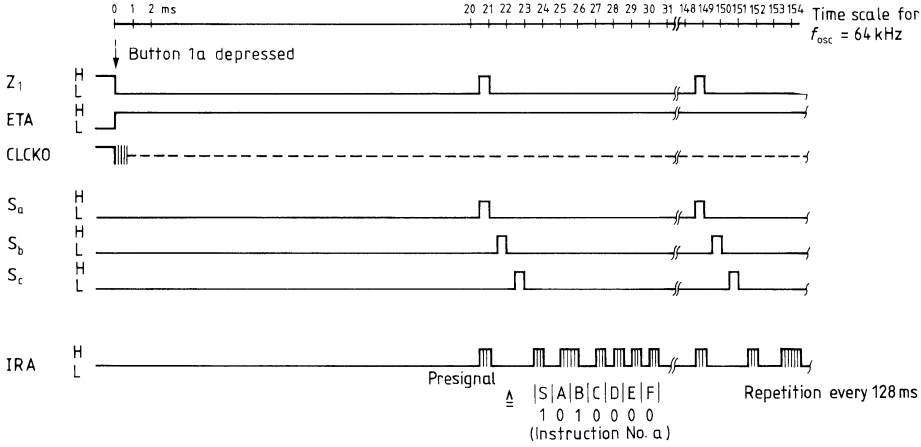
Instruction set with assignment of the instructions to the buttons

Instr. No.	Code F E D C B A	Logic operation
a	0 0 0 0 1 0	1c
b	0 0 0 1 0 0	2a
c	0 0 0 1 0 1	2b
d	0 0 1 0 0 0	3a
e	0 0 1 0 0 1	3b
f	1 1 1 1 1 0	End instruction

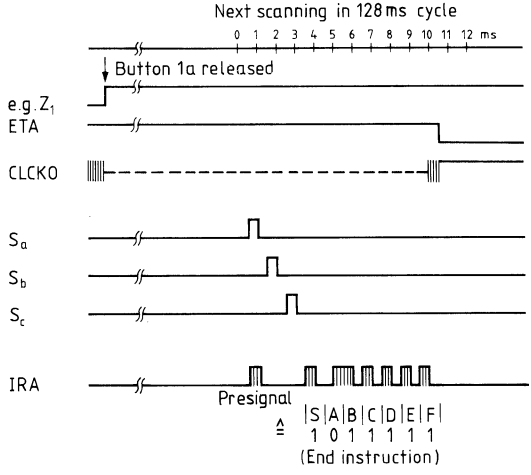
Timing diagram 1
(biphase coding without presignal)



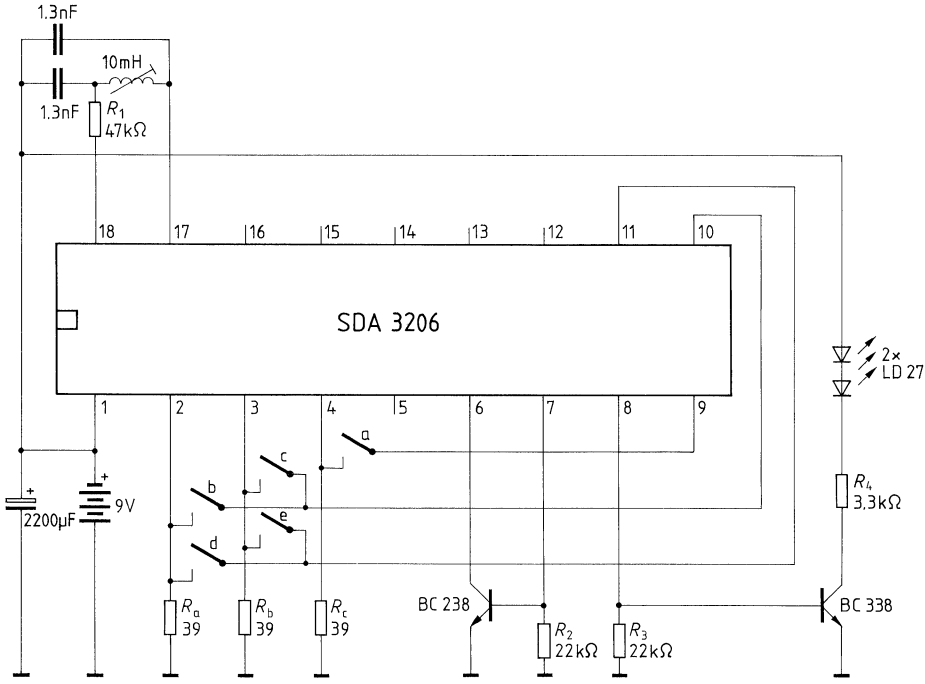
Timing diagram 2
(pressing a button)



Timing diagram 3
(releasing a button)



External connection
(example)



Bipolar circuit

The IC TDA 4050 B is suitable for use as infrared preamplifier in remote control facilities for radio and TV sets.

The IC includes a controlled driver stage with subsequent amplifier stage as well as an amplifier of the threshold value. The circuit is largely balanced.

- Provision of internal AGC voltage
- High capability for large signals
- Short-circuit proof signal output
- Simple connection for an active band filter
- Few external components

Type	Ordering code	Package outline
TDA 4050 B	Q 67000-A 1373	DIP 8

Maximum ratings

Supply voltage	V_S	16 [1])	V
Thermal resistance (system-air)	$R_{th\ SA}$	140	K/W
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C

Range of operation

Supply voltage range	V_S	9 to 16	V
Ambient temperature range	T_{amb}	−15 to 80	°C
Input frequency range	f_i	0 to 100	kHz

[1]) intermittently 17.5 V

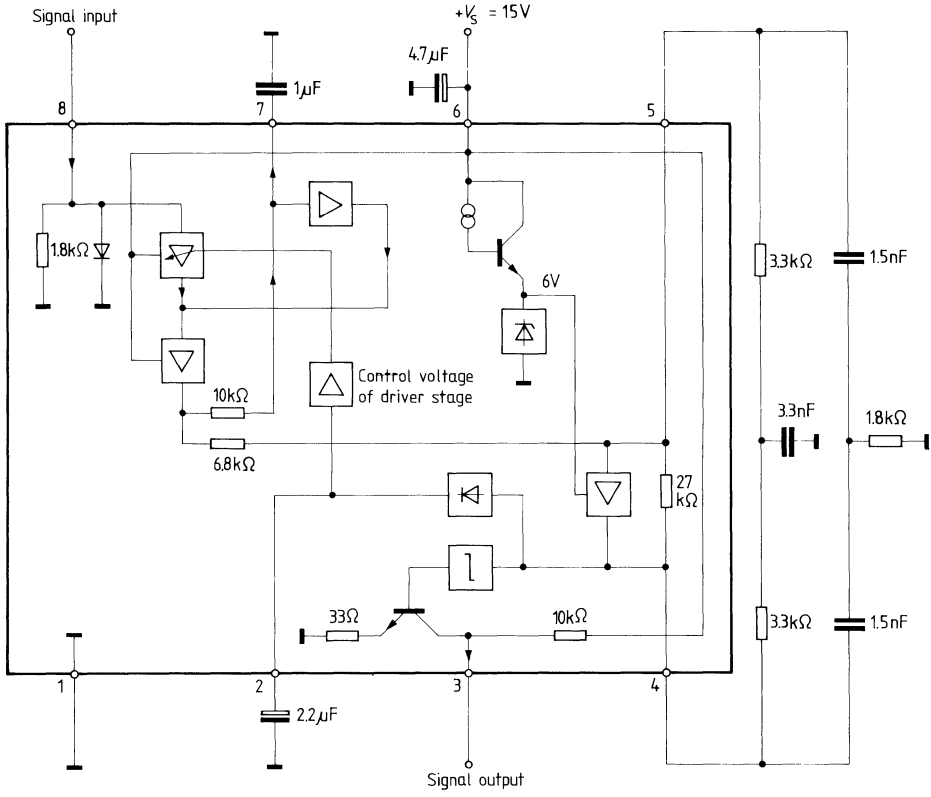
Characteristics (with reference to test circuit, $V_S = 12\,V$; $T_{amb} = 25\,°C$; $f_{IR} = 31.25\,kHz$)

		min	typ	max	
Current consumption ($R_L \geqq 10\,k\Omega$)	I_6		9	13	mA
Input voltage for starting control	$V_{i\,8}$		50		μV_{rms}
Gain	$G_{4/8}$	74	77	85	dB
Gain	$G_{3/4}$		21		dB
Total control range	ΔG	74	77	85	dB
Output current ($R_L = 0\,\Omega$)	$I_{q\,3}$		20		mA
Output DC voltage for L level ($I_{q\,3L} = 2\,mA$)	$V_{q\,3L}$		150	500	mV
Output DC voltage for H level ($I_{q\,3L} = 0\,mA$)	$V_{q\,3H}$	$V_S - 0.4$	V_S		V
Input resistance	$R_{i\,8}$		1.8		kΩ
Output resistance	$R_{q\,3}$		10		kΩ
Rated impedance of the double-T network at pin 4 (unbalanced to ground)	R_4	2			kΩ

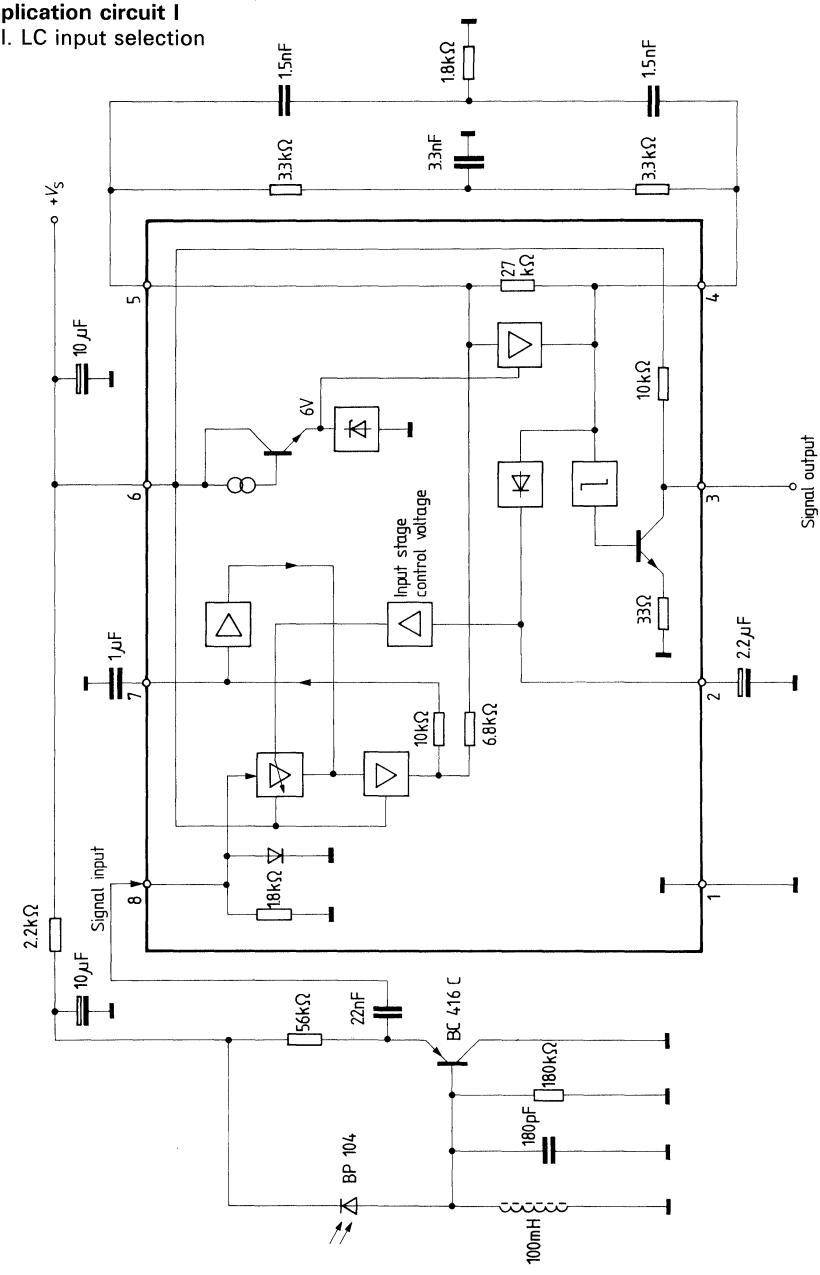
Pin designation

Pin No.	Description
1	Ground
2	Connection for capacitance for prestage control
3	Output threshold amplifier
4	Output active filter
5	Input active filter
6	Supply voltage, positive
7	Unlocking of operation point control
8	Signal input

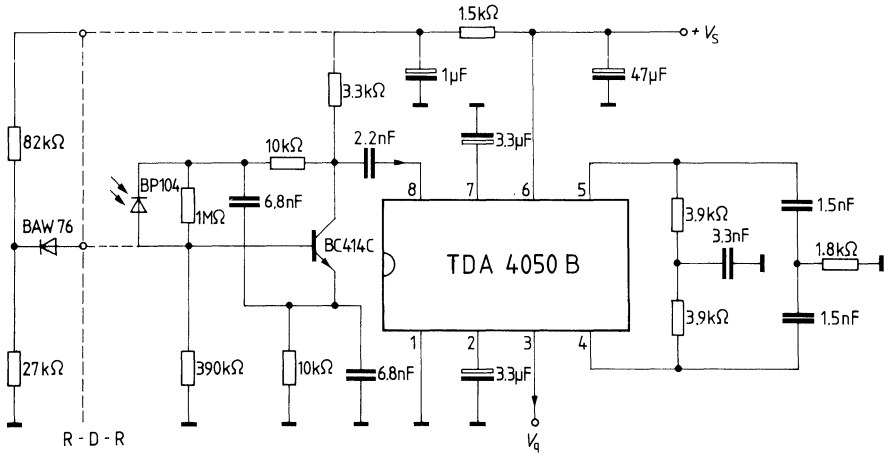
Test circuit and block diagram



Application circuit I
incl. LC input selection



Application circuit II
without coil



Notes

Circuit 1 uses and LC resonant circuit and features higher quality because of its high selectivity (approx. 3 kHz bandwidth at −3 dB).

Circuit 2 offers the lower cost solution without coil incl. wideband input selection. Higher requirements as to steady radiation and large signal capability can be met by means of resistor-diode-resistor connection (RDR).

Switching Amplifier for 4-Channel Touch Tuning

SAS 560 S
SAS 570 S

Bipolar circuit

Channel memory for use in radio and TV sets. The four stages can be switched over by touching the sensor areas with the finger. Each stage is provided with a read-out output and a tuning output.

The high input sensitivity allows application in devices without mains separation. Almost any number of ICs can be interconnected.

SAS 560S: after applying V_7 stage 1 switches on.
SAS 570S: after applying V_7 no stage switches on.

- High input sensitivity
- Low saturation voltage of driver outputs
- Low temperature drift of tuning outputs
- Driver outputs for filament lamps and LEDs

Type	Ordering code	Package outline
SAS 560 S	Q 67000-S30	DIP 16
SAS 570 S	Q 67000-S31	

Maximum ratings

Supply voltage 1	V_7	36	V
Supply voltage 2	V_8	26.5	V
Voltage	V_2	6	V
Driver current	I_9, I_{11}, I_{13}, I_{15}	55	mA
Max. driver current, $t_{max} \leqq 2$ sec	I_9, I_{11}, I_{13}, $I_{15\,max}$	100	mA
Tuning current	I_3, I_4, I_5, I_6	1.5	mA
Max. tuning current, $t_{max} \leqq 2$ sec	I_3, I_4, I_5, $I_{6\,max}$	10	mA
Thermal resistance (system-air)	$R_{th\,SA}$	90	K/W
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C

Range of operation

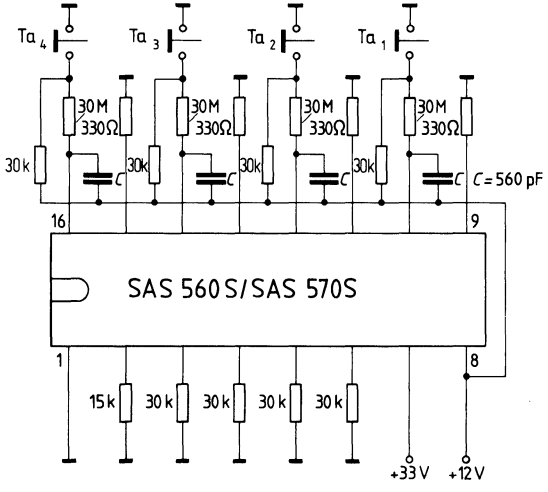
Supply voltage 1 range	V_7	11 to 35	V
Supply voltage 2 range	V_8	5 to 25	V
Ambient temperature range	T_{amb}	0 to 70	°C

Characteristics (with reference to test circuit, V_7 = 33 V, V_8 = 12 V, T_{amb} = 25° C)

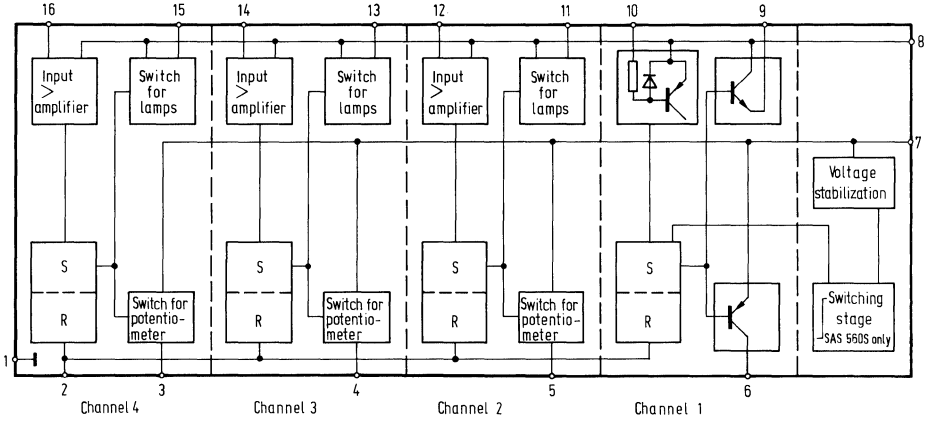
		min	typ	max	
Voltage at pin 2 (R_K = 15 kΩ					
during touching	$V_{2\text{-}1}$	4.2	4.7	5.5	V
after touching	$V_{2\text{-}1}$	2.6	3.2	3.7	V
Saturation voltage of driver outputs	$V_{15\text{-}8}$, $V_{13\text{-}8}$,		0.9	1.5	V
	$V_{11\text{-}8}$, $V_{9\text{-}8}$		0.9	1.5	V
Saturation voltage of tuning voltage outputs	$V_{3\text{-}7}$, $V_{4\text{-}7}$, $V_{5\text{-}7}$, $V_{6\text{-}7}$		0.15	0.5	V
Temperature drift of saturation voltage of tuning outputs (T_{amb} = 25 to 55 °C)	$V_{3\text{-}7}$, $V_{4\text{-}7}$, $V_{5\text{-}7}$, $V_{6\text{-}7}$		0.3	1	mV/deg
Current consumption					
during touching	I_7	3.15	4.3	5.35	mA
after touching	I_7	3.4	4.7	5.75	mA
Current consumption (without load)	I_7	0.5	1.4	2.1	mA
Input current	I_{10}, I_{12}, I_{14}, I_{16}		100	300	nA
Reverse current of driver outputs	I_9, I_{11}, I_{13}, I_{15}			10	µA
Reverse current of tuning voltage outputs	I_3, I_4, I_5, I_6			1	µA

After simultaneous selection of more than one channel, only **one** channel will be selected. This also applies when several ICs are interconnected. After switching of V_8, the last selected channel is stored as long as V_7 supply is maintained.

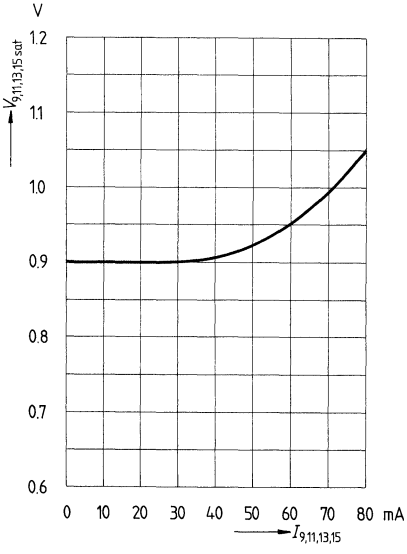
Test circuit



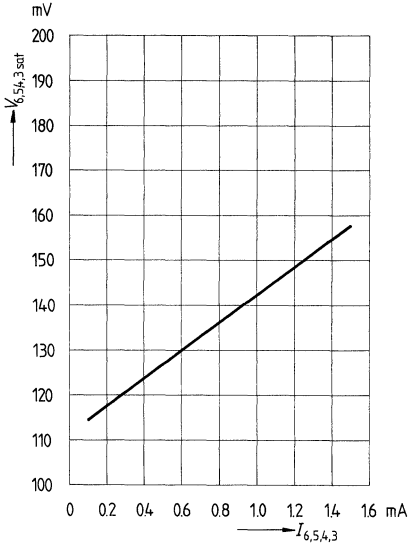
Block diagram



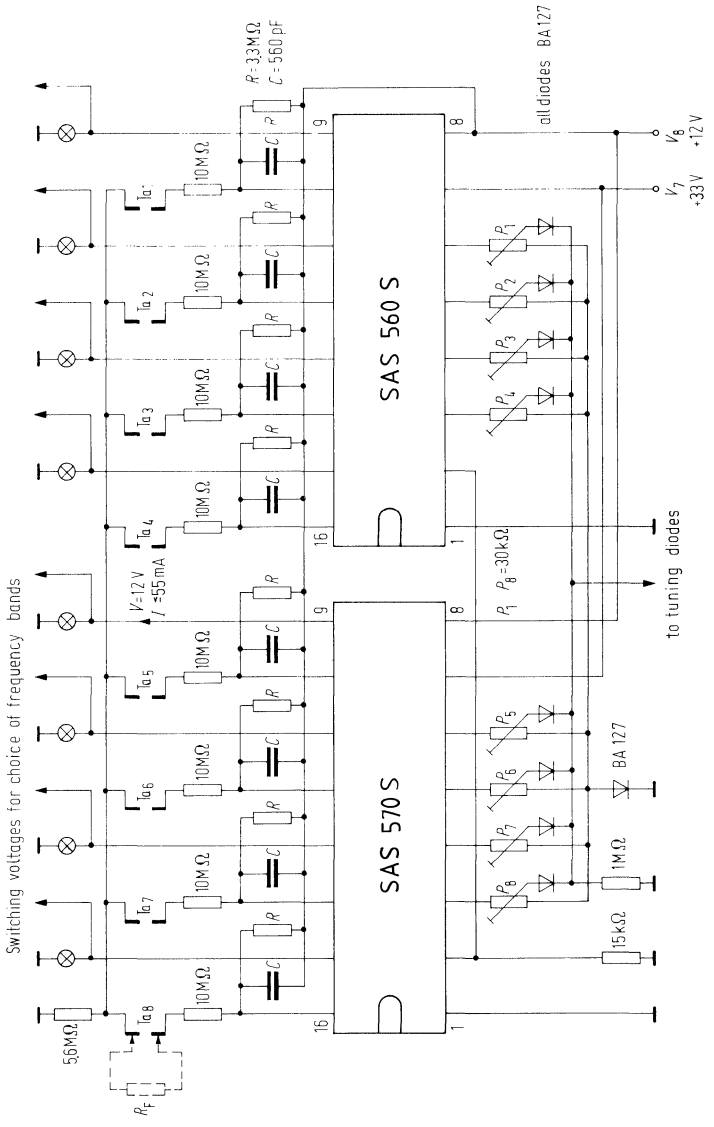
Saturation voltage of driver outputs versus current of these outputs



Saturation voltage of tuning voltage outputs versus current of these outputs



Application circuit



Switching Amplifiers for 4-Channel Touch Tuning

SAS 580
SAS 590

Bipolar circuit

Channel memory for use in radio and TV sets. The four stages can be selected by touching the sensor area with the finger. Each stage is provided with a read-out output. The tuning voltage is switched through to a common output. SAS 580 is the basic component for the first 4 channels. By adding almost any number of SAS 590, the number of channels can be extended by 4 channels, each.

- High input sensitivity
- Low saturation voltage of the driver outputs
- Low temperature drift of the tuning switches
- Driver outputs to control filament lamps, LEDs, neon lamps or nixie tubes
- Standby operation possible
- Ring counter up to 10 kHz
- No external diode matrix
- **Single** power supply

Type	Ordering code	Package outline
SAS 580	Q 67000-S28	DIP 18
SAS 590	Q 67000-S29	

Maximum ratings

Supply voltage (without series resistor)	V_{16}	36	V
Current consumption (for operation with higher voltage, a series resistor is required)	I_{16}	15	mA
Driver current	I_3, I_5, I_7, I_9	55	mA
Max. driver current, $t_{max} \leq 2$ sec	I_3, I_5, I_7, $I_{9\,max}$	100	mA
Junction temperature	T_j	150	°C
Thermal resistance (system-air)	$R_{th\,SA}$	90	K/W
Storage temperature range	T_{stg}	−40 to 125	°C

Range of operation

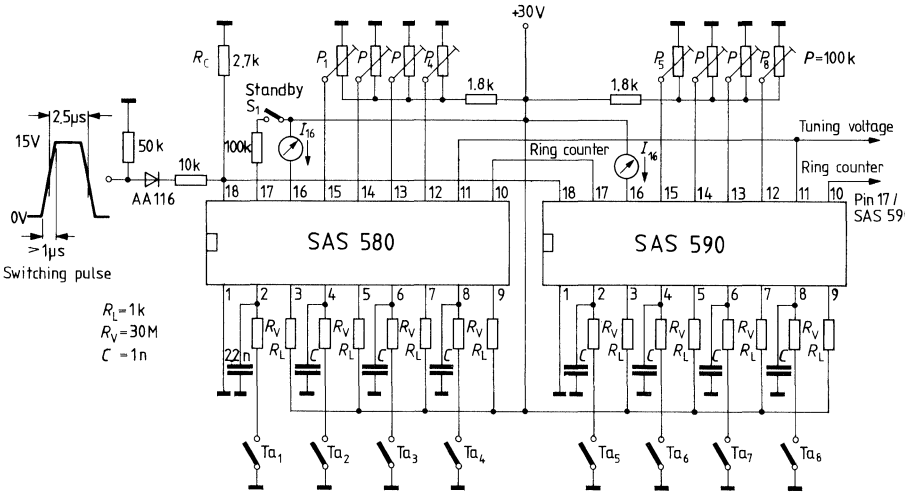
Supply voltage range	V_{16}	10 to 36	V
Ambient temperature range	T_{amb}	0 to 70	°C

Characteristics (with reference to test circuit, $V_{16} = 30$ V, $T_{amb} = 25°C$)

		min	typ	max	
Internal current consumption					
channel switched	I_{16}	4.5	7	9.5	mA
channel not switched	I_{16}	2.9	5	8.5	mA
Voltage at pin 18					
during touching	$V_{18\,s}$	3.25	3.7	4.2	V
after touching	$V_{18\,h}$	2.6	2.9	3.2	V
Saturation voltage of driver outputs					
$R_L = 1$ kΩ	V_3, V_5, V_7, V_9		0.8	1.5	V
$R_L = 30$ kΩ	V_3, V_5, V_7, V_9		30	60	mV
Reverse voltage of driver outputs					
$I_{rev} = 100$ µA	V_3, V_5, V_7, V_9	60			V
$I_{rev} = 5$ µA	V_3, V_5, V_7, V_9	50			V
Tuning voltage	V_{12}, V_{13}, V_{14}, V_{15}	0.3		$V_{16}-2$	V
Input current of tuning voltage inputs	I_{12}, I_{13}, I_{14}, I_{15}		150	300	nA
Offset voltage of tuning switches[1])	$V_{12\text{-}11}$, $V_{13\text{-}11}$			±100	mV
	$V_{14\text{-}11}$, $V_{15\text{-}11}$			±100	mV
Temperature drift of tuning voltage switches ($T_{amb} = 20$ to 50 °C)[1])	V_T			5	mV
Resistance of tuning output ($I_{11} < \pm 30$ µA)	$R_{q\,11}$		3		kΩ
Trigger current for channel switching	I_2, I_4, I_6, I_8	20	80	200	nA
Input threshold voltage of switch amplifiers (I_2, I_4, I_6, $I_8 = 80$ nA)	V_2, V_4, V_6, V_8		5.5		V
Switch frequency of ring counter	f_{rc}		10		kHz
Reset to channel 1					
Switching pulse level	$V_{SI\,18}$		15		V
Switching pulse duration	$T_{SI\,18}$	70			µs
Switching pulse rise time	$t_{SI\,LH\,18}$			1	µs
Switching to the next stage					
Switching pulse level	$V_{SI\,18}$		15		V
Switching pulse duration	$T_{SI\,18}$		2.5		µs
Switching pulse rise time	$t_{SI\,LH\,18}$			1	µs
Characteristics of the Z diode					
Z voltage ($I_{16\,(30\,V)} + 3$ mA)	V_Z	34		39	V

* measured between switched input and pin 11.

Test circuit



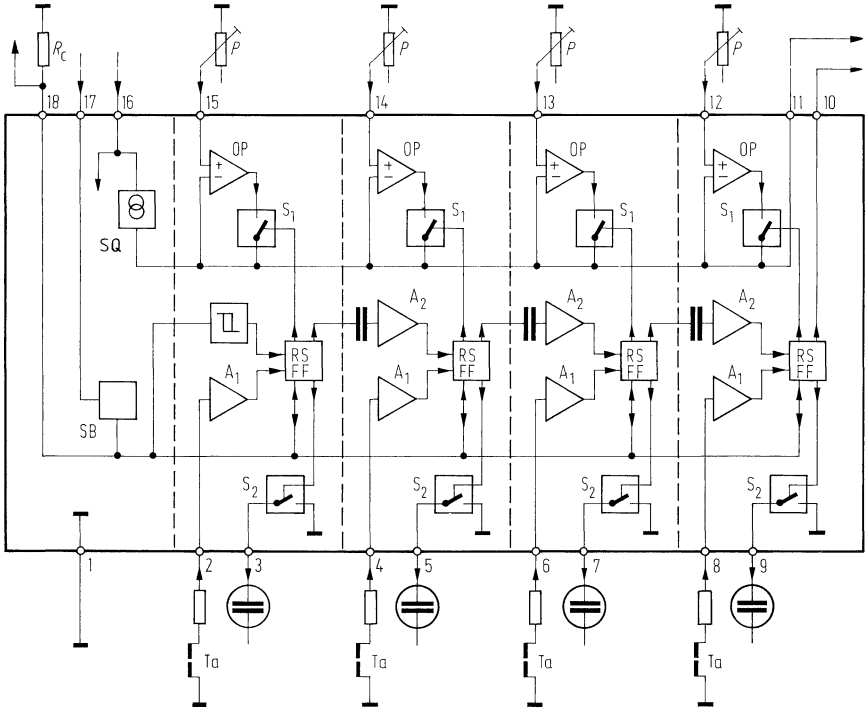
SAS 580 is absolutely necessary for testing SAS 590;
otherwise no function
SAS 580 can be tested individually.

At a channel change, the capacitor which operates as a load on pin 11 is reversely charged with a current of approx. ±50 µA.

SAS 580 only: After applying supply voltage V_{16}, channel 1 is selected, i.e. the tuning voltage is switched from pin 15 to pin 11 and the lamp at pin 3 is switched on.

V_{17} <0.5 V means standby operation, i.e. even when selecting another channel, the channel previously selected remains stored. Selection of a new channel is not possible. A stored channel must come on again after closing S_1.

Block diagram SAS 580



SQ: Current source
SB: Standby

Figure 1

Circuit diagram: one channel

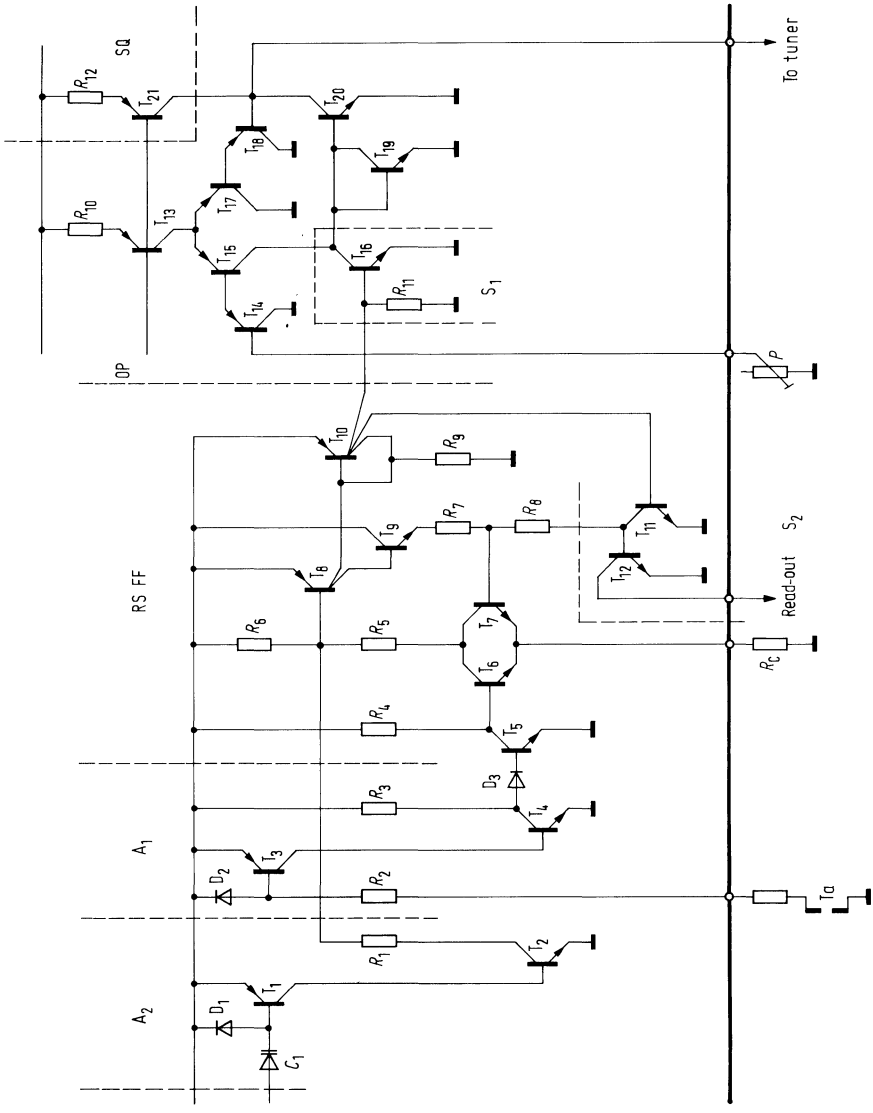


Figure 2

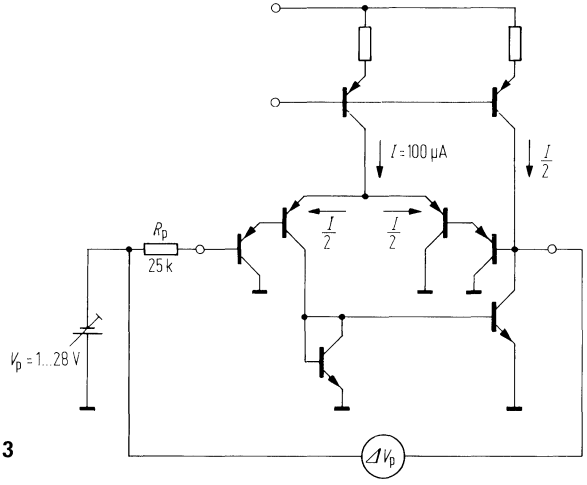


Figure 3

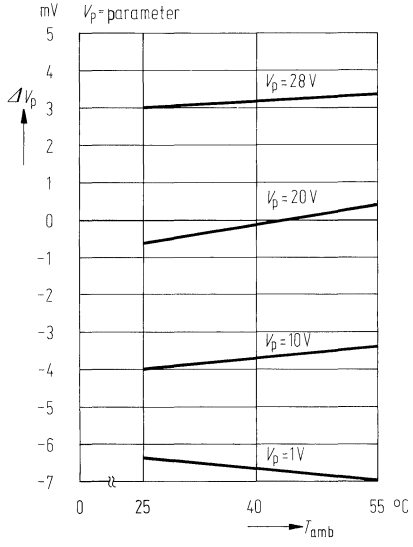


Figure 4

Application circuit 1

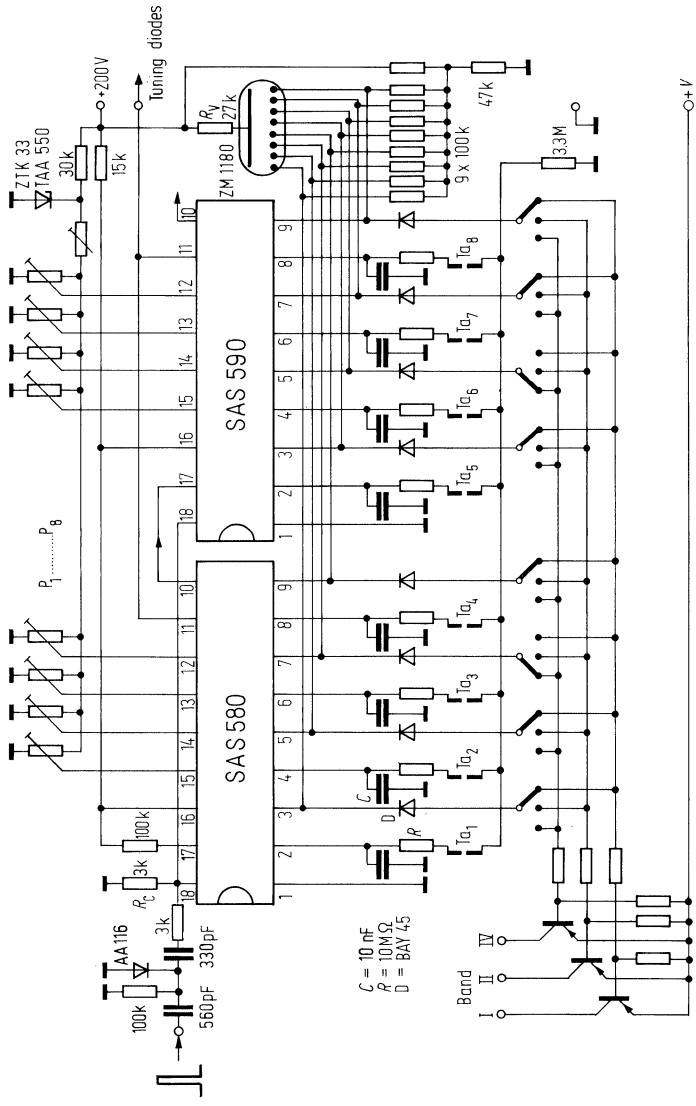


Figure 5

Application circuit 2

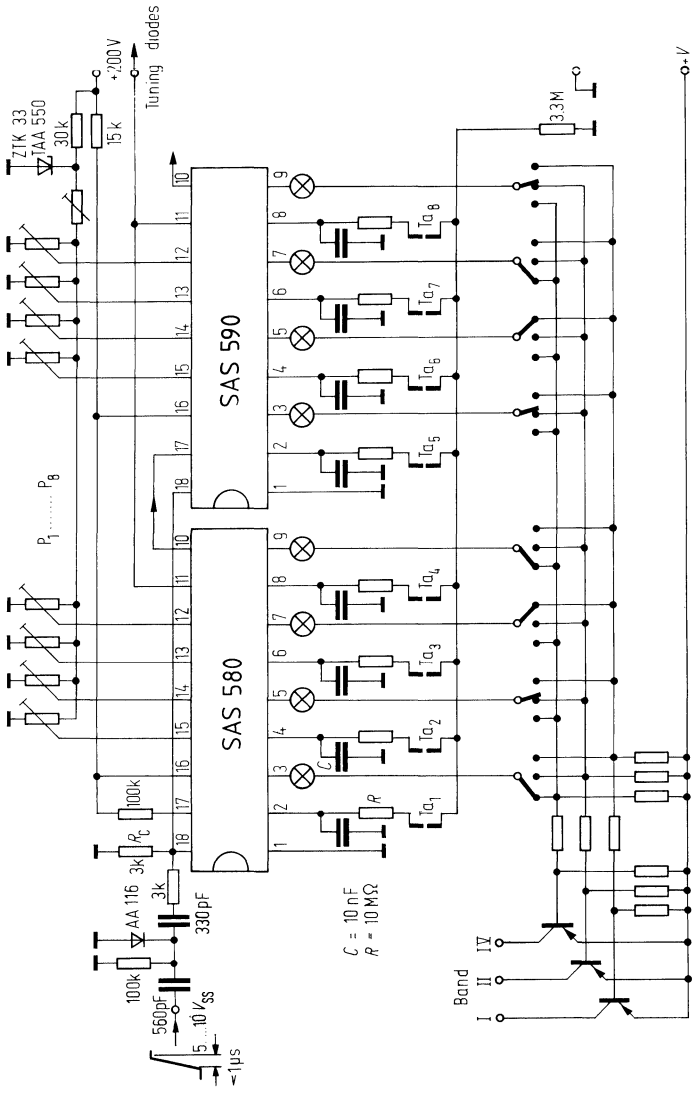


Figure 6

Switching Amplifiers for 4 Channel Touch Tuning with Muting Pulse

SAS 5800
SAS 5900

Bipolar circuit

Not for new design

The ICs SAS 5800/SAS 5900 are provided for channel selection in radio and TV sets. By means of sensitive contact inputs (sensors) four different, previously set tuning voltages may be switched for every module at a programmed delay to the tuner. A positive pulse without delay, released by switching, of longer duration than the switching process, causes a completely noiseless changeover with the aid of driving a muting circuit. When the supply voltage has been applied, the first step in the SAS 5800 is automatically set.

- Adjustable muting
- Standby operation possible
- Direct driving of LED's or lamps

Type	Ordering code	Package outline
SAS 5800	Q67000-S62	DIP 22
SAS 5900	Q67000-S63	DIP 18

Maximum ratings

		SAS 5800	
Supply voltage	V_{13}	36	V
	V_{21}	30	V
Input voltage	$V_{17/18/19/20}$	$V_{21}+5$	V
Input current	$I_{17/18/19/20}$	0.5	mA
Output current	$-I_{3/5/7/9}$	35	mA
$t \leqq 2$ s	$-I_{3/5/7/9\ max}$	100	mA
Reference voltage	$V_{2/4/6/8}$	V_{13}	V
Current consumption (for operation at higher voltage, a series resistor is required)	I_{13}	25	mA
Muting output current	$-I_{10}$	10	mA
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\ SA}$	70	K/W

Range of operation

Supply voltage range	V_{13}	12 to 36	V
	V_{21}	8 to 24	V
Ambient temperature range	T_{amb}	0 to 70	°C

Maximum ratings (cont'd)

		SAS 5900	
Supply voltage	V_{10}	36	V
	V_{17}	30	V
Input voltage	$V_{13/14/15/16}$	$V_{17}+5$	V
Input current	$I_{13/14/15/16}$	0.5	mA
Output current	$-I_{3/5/7/9}$	35	mA
$t \leqq 2$ s	$-I_{3/5/7/9\ max}$	100	mA
Reference voltage	$V_{2/4/6/8}$	V_{10}	V
Current consumption (for operation at higher voltage a series resistor is required)	I_{10}	20	mA
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\ SA}$	90	K/W

Range of operation

Supply voltage range	V_{10}	12 to 36	V
	V_{17}	8 to 24	V
Ambient temperature range	T_{amb}	0 to 70	°C

Characteristics (with reference to test circuit, $V_{13} = 30$ V; $V_{21} = 20$ V; $T_{amb} = 25$ °C)

SAS 5800

		min	typ	max	
Current consumption (without load at pin 10)					
Channel not switched	I_{13}	5	9	13.5	mA
Channel switched	$I_{13\,H}$	7	11.5	16	mA
Switched state	$I_{13\,S}$	12	18	25	mA
Current consumption	I_{21}			100	µA
Switching voltage at touching the buttons Ta_1 to Ta_8 (dynamically measured)	$V_{14\,S}$		3		V
Hold voltage after touching the buttons Ta_1 to Ta_8	$V_{14\,H}$		2.5		V
Saturation voltage of driver outputs					
$R_L = 510\ \Omega$	$V_{3/5/7/9}$		1	2	V
$R_L = 30$ kΩ	$V_{3/5/7/9}$		20	60	mV
Reverse voltage of driver outputs ($I_{rev} = 5$ µA)	$V_{3/5/7/9}$	30			V
Tuning voltage	$V_{2/4/6/8}$	0.5		$V_{13}-2$	V
Offset voltage of tuning switches	$V_{2\text{-}22}$, $V_{4\text{-}22}$	−100		100	mV
	$V_{6\text{-}22}$, $V_{8\text{-}22}$	−100		100	mV
Temperature drift of tuning voltage switches[1]) ($T_{amb} = 20$ to 50 °C)	V_T			5	mV
Tuning charge current with ref. to cap. load at lower voltage	$-I_{22}$	0.7	1		mA
Tuning discharge current with ref. to cap. load at higher voltage	I_{22}	2	4		mA

[1]) measured between switched input and pin 22

Characteristics (with reference to test circuit, $V_{13} = 30$ V; $V_{21} = 20$ V; $T_{amb} = 25$ °C)

SAS 5800, cont'd

		min	typ	max	
Internal resistances of the tuning voltage outputs ($-I_{22} \geqq 300$ µA)	R_{22}		60	90	Ω
Input current of tuning voltage inputs	$-I_{2/4/6/8}$		100	200	nA
Trigger current for channel switching	$-I_{17/18/19/20}$	40	200	400	nA
Saturation voltage muting output	$V_{10\text{-}13}$		1.5	2.5	V
Switching threshold S_1 for switching the tuning voltage[2])	V_{16}	1.2	1.5	1.75	V
Switching threshold S_3 for muting pulse end[2])	V_{16}		3.3		V

Characteristics (with reference to test circuit, $V_{10} = 30$ V; $V_{17} = 20$ V; $T_{amb} = 25$ °C)

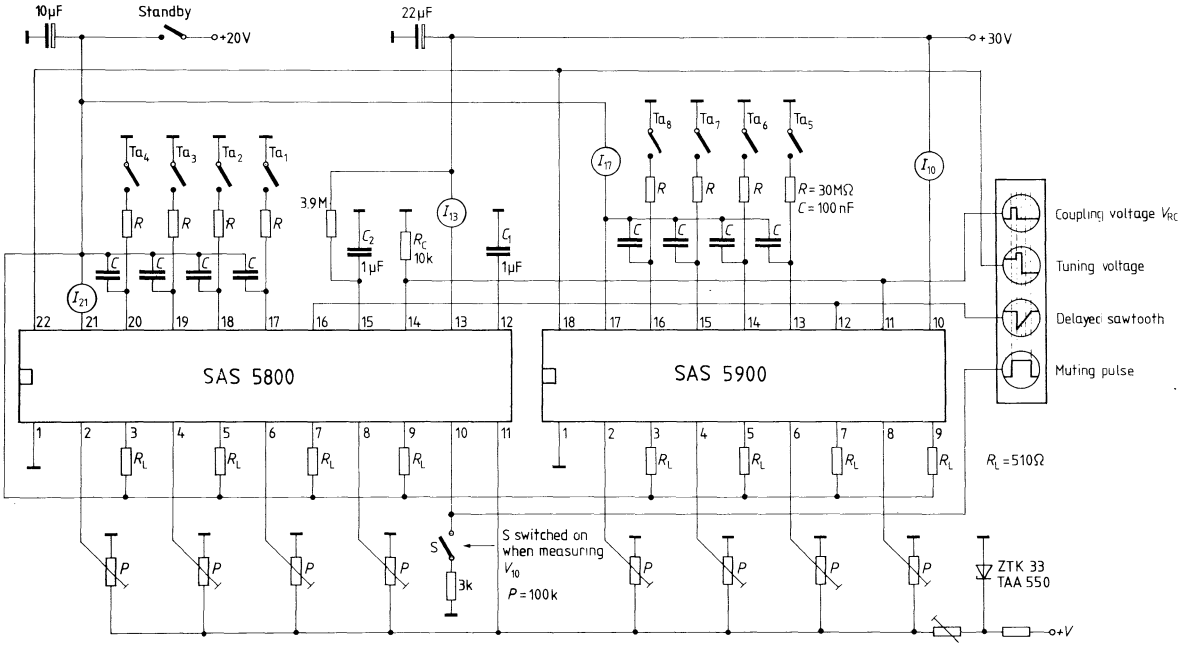
SAS 5900

Current consumption					
Channel not switched	I_{10}	5	8	12	mA
Channel switched	$I_{10\,H}$	7	10	14	mA
Switched state	$I_{10\,S}$	9	13	17	mA
Current consumption	I_{17}			100	µA
Switching voltage at touching the buttons Ta_1 to Ta_8 (dynamically measured)	$V_{11\,S}$		3		V
Hold voltage after actuating the buttons Ta_1 to Ta_8	$V_{11\,H}$		2.5		V
Saturation voltage of driver outputs					
$R_L = 510\,\Omega$	$V_{3/5/7/9}$		1	2	V
$R_L = 30$ kΩ	$V_{3/5/7/9}$		20	60	mV
Reverse voltage of driver outputs ($I_{rev} = 5$ µA)	$V_{3/5/7/9}$	30			V
Tuning voltage	$V_{2/4/6/8}$	0.5		$V_{10}-2$	V
Offset voltage of tuning switches	$V_{2\text{-}18}$, $V_{4\text{-}18}$	−100		100	mV
	$V_{6\text{-}18}$, $V_{8\text{-}18}$	−100		100	mV
Temperature drift of tuning voltage switches[1]) ($T_{amb} = 20$ to 50 °C)	V_T			5	mV
Tuning discharge current with ref. to cap. load at higher voltage	I_{18}	2	4		mA
Input current of tuning voltage inputs	$-I_{2/4/6/8}$		100	200	nA
Trigger current for channel switching	$-I_{13/14/15/16}$	40	200	400	nA
Switching threshold S_1 for switching the tuning voltage[2])	V_{12}	1.2	1.5	1.75	V

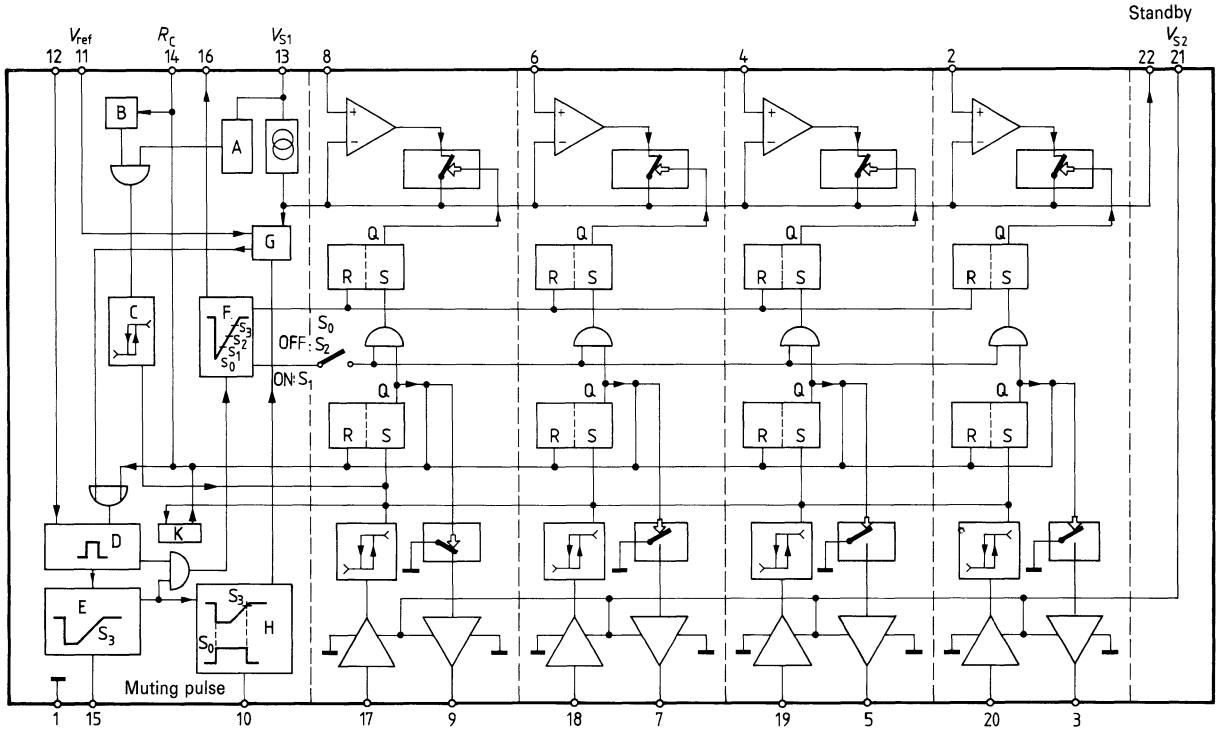
Functional data (applies to SAB 5800 and SAB 5900)

1. After applying the supply voltage V_{S1}, stage 1 of the SAS 5800 ist automatically set.
2. All inputs Ta_1 to Ta_8 are blocked, if the supply voltage V_{S2} is less than 2 V.
3. The supply voltage V_{S2} has no influence on which stage has been switched on. After V_{S2} has been switched off and switched on again (standby operation), the indicator lamp of the previously keyed stage is switched on again. The tuning voltage remains switched on even in standby operation.

[1]) measured between switched input and pin 18
[2]) see pulse diagram

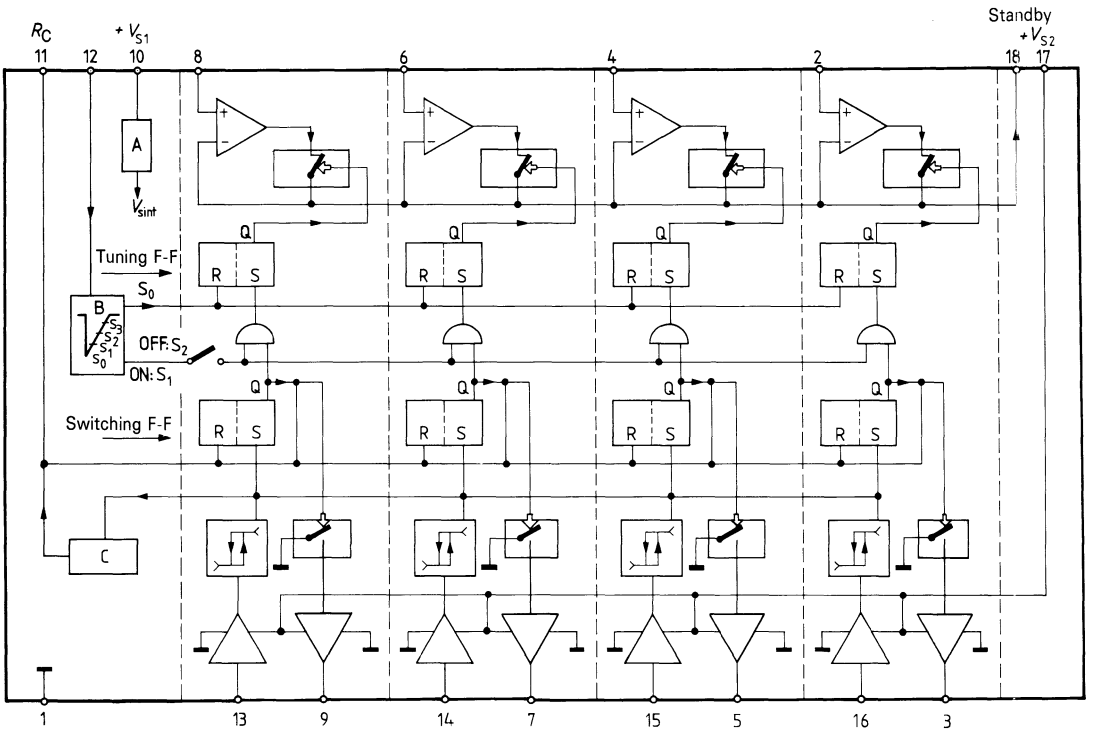


SAS 5800 is absolutely necessary for testing SAS 5900;
otherwise no function
SAS 5800 can be tested individually.



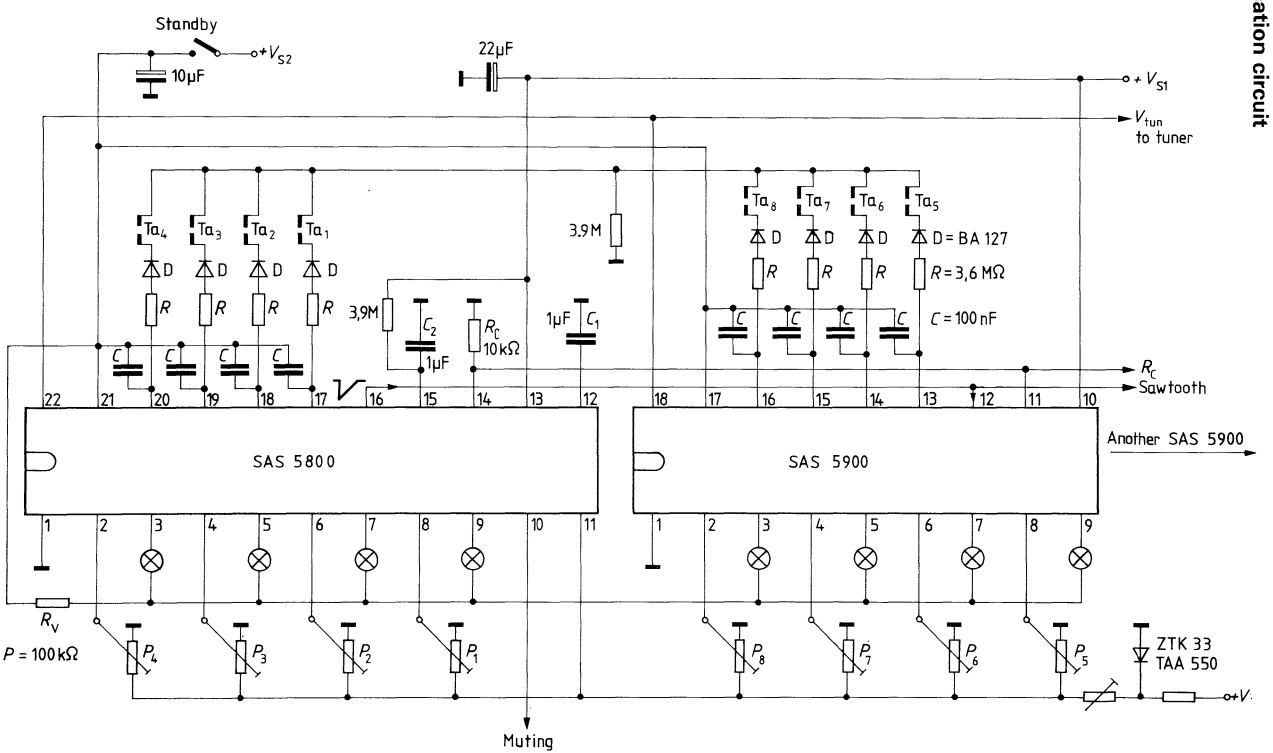
A Stabilizing of internal supply voltage V_{sint}
B V_{RC} = O; voltage at coupling resistor is still zero when applying V_s or V_{sint}
C After having switched on, the first stage is set via the Schmitt trigger as soon as V_{sint} attains its full extent and V_{RC} equals zero.
D Switching stage for switching pulse generation
E Sawtooth generation
F Gating the pulse D and E results in obtaining the delayed sawtooth
G New sawtooth start, in case of incoccrect tuning voltage transfer $V_{tun} = V_{ref} + V_{BE}$
H Muting pulse generation. Duration is determined by start and threshold of sawtooth
K Recognition whether finger still on button

Not for new design



A Stabilizing of the internal supply voltage V_{sint}
B Delayed sawtooth from SAS 5800. S = End of muting pulse from SAS 5800
C Recognition whether finger still presses button

Not for new design



Not for new design

Bipolar circuit

The IC SAS 6800 includes five independent switching stages which can be selected by touch tuning. After every actuation they can change their output state. They are intended for use in radio sets to switch on and off noise filters, AFC, sound control etc. independently from each other.

- High input sensitivity
- Storage of the switching state at standby operation
- Outputs can be loaded with 35 mA

Type	Ordering code	Package outline
SAS 6800	Q 67000-S60	DIP 18

Maximum ratings

Supply voltage	V_7	20	V
	V_8	33	V
Input voltage	$V_{2,3,4,5,6}$	V_8+5	V
Input current	$I_{2,3,4,5,6}$	0.5	mA
Output current	$-I_q$	35	mA
Thermal resistance (system-air)	$R_{th\ SA}$	90	K/W
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C

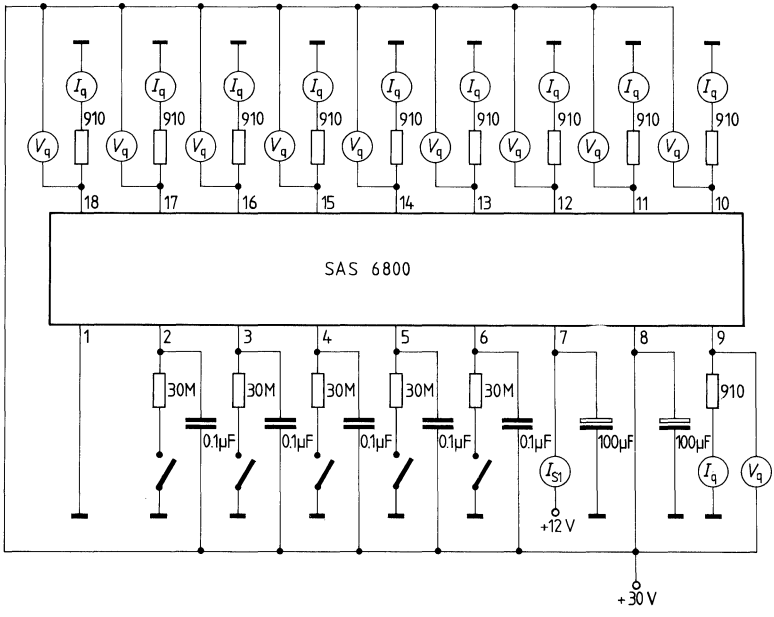
Range of operation

Supply voltage range	V_7	5 to 18	V
	V_8	10 to 30	V
Ambient temperature range	T_{amb}	0 to 70	°C

Characteristics with reference to test circuit, (V_7 = 12 V; V_8 = 30 V; T_{amb} = 25 °C)

		min	typ	max	
Current consumption	I_7		13	18	mA
Current consumption without load current	I_8			6	mA
Saturation voltage of outputs (referred to V_8)	V_q		1.8	2.4	V
Reverse current of outputs	$-I_q$		1	50	µA
Input current of tuning voltage inputs	$-I_{2,3}$		200	400	nA

Test circuit



Description of functions (see block diagram)

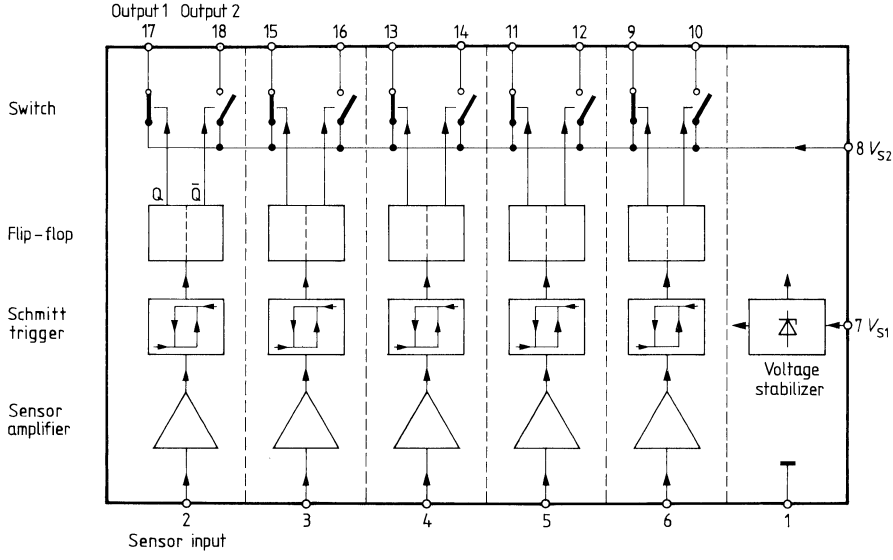
After having applied the supply voltage V_{S1}, the Q driver outputs are activated. All inputs are blocked as soon as the supply voltage V_{S2} is lower than 2 V. The supply voltage V_{S2} has no influence on the position of the outputs. After the supply voltage V_{S2} has been switched off and on again (standby operation) the previously selected position is set again.

Description of the circuit

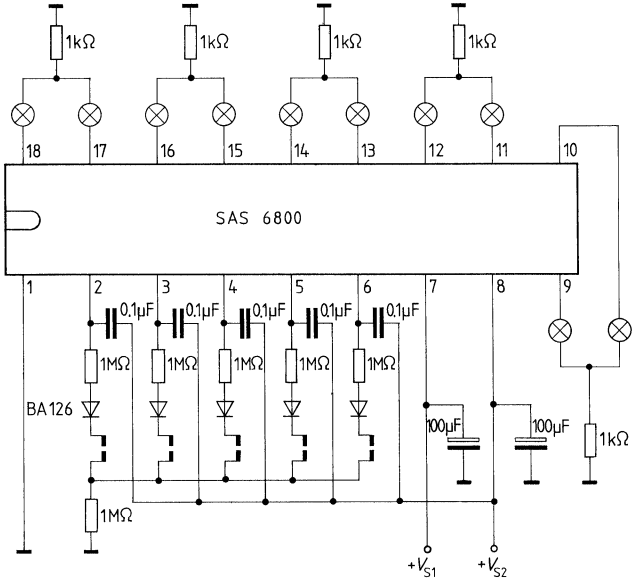
The sensor amplifier of each of the five sequence switches is followed by a Schmitt trigger in order to achieve debouncing. The Schmitt trigger sets a bistable multivibrator. The outputs Q and $\overline{Q}$ of the multivibrators each control two output switching amplifiers which are able to directly drive the LED displays. After having activated the sensor inputs either output Q or $\overline{Q}$ is subsequently activated. An auxiliary circuit provides for a defined output position after applying the supply voltage. Thus, the user can freely select the desired switching sequence by means of external facilities.

The internal supply voltage is stabilized by a control circuit.

Block diagram



Application circuit



Bipolar circuit

The IC SAS 6810 is referred to the SAS 6800. It includes only one switching stage, which is selected by a sensor key and changes its output state after every actuation. Thus, the SAS 6810 is suited for use in radio sets to switch on or off functions such as AFC or noise filter.

- High input sensitivity
- Storage of the switching state at standby operation
- Direct LED driving
- Output load permitted: 35 mA

Type	Ordering code	Package outline
SAS 6810	Q67000-S61	DIP 6

Maximum ratings

Supply voltage	V_4	20	V
	V_5	33	V
Input voltage	V_3	$V_{S2}+5$	V
Input current	I_3	0.5	mA
Output current	$-I_q$	35	mA
Thermal resistance (system-air)	$R_{th\,SA}$	120	K/W
Junction temperature	T_j	150	°C
Storage temperature	T_{stg}	−40 to 125	°C

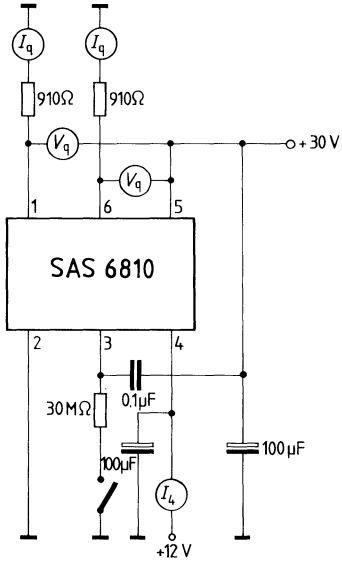
Range of operation

Supply voltage range	V_{S1}	5 to 18	V
	V_{S2}	10 to 30	V
Ambient temperature range	T_{amb}	0 to 70	°C

Characteristics (with reference to test circuit, $V_4 = 12$ V; $V_5 = 30$ V; $T_{amb} = 25$ °C)

		min	typ	max	
Current consumption	I_4		3.5	5	mA
Current consumption without load current	I_5			2	mA
Saturation voltage of outputs (referred to V_5)	V_q		1.8	2.4	V
Reverse current of outputs	$-I_q$		1	50	µA
Trigger current for channel switching	$-I_3$		200	400	nA

Test circuit



Description of functions (see block diagram)

After having applied the supply voltage V_{S1}, the Q driver output 1 is activated. The input is blocked as soon as the supply voltage V_{S2} is lower than 2 V. The supply voltage V_{S2} has no influence on the position of the outputs. After the supply voltage V_{S2} has been switched off and on again (standby operation) the previously selected position is set again.

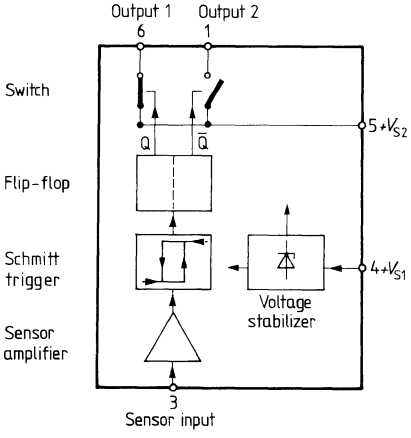
Description of the circuit

The sensor amplifier is followed by a Schmitt trigger in order to achieve debouncing. The Schmitt trigger sets a bistable multivibrator, the outputs Q und $\overline{Q}$ of which each control two output switching amplifiers which are able to directly drive the LED displays. After having activated the sensor inputs, either output Q oder $\overline{Q}$ are subsequently activated.

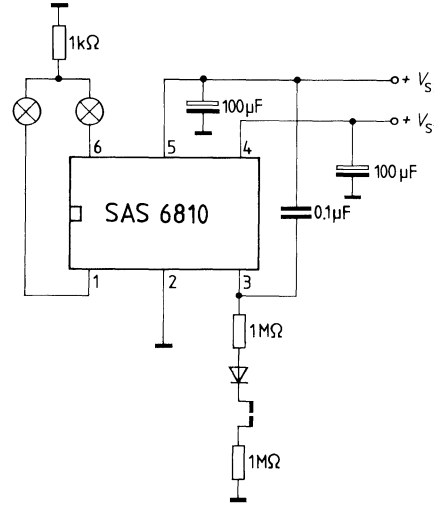
An auxiliary circuit provides for a defined output position after applying the supply voltage. Thus, the user can freely select the desired switching sequence by means of external facilities.

The internal supply voltage is stabilized by a control circuit.

Block diagram



Application circuit



AF Power Amplifier IC with Thermal Shutdown

TDA 1037
TDA 1037 D

Bipolar circuit

AF power amplifier for use in equipment of entertainment electronics. Its wide supply voltage range permits versatile use. The amplifier operates in the push-pull B mode and is available in the SIP 9 package as well as in the DIP 18 package. The integrated shutdown protects the IC from overheating.

- Wide supply voltage range: 4 V to 28 V
- High output power up to 8 W
- Large output current up to 2.5 A
- Simple mounting

Type	Ordering code	Package outline
TDA 1037	Q 67000-A1229	SIP 9
TDA 1037 D	Q 67000-A1387	DIP 18

Maximum ratings

Supply voltage $R_L \geqq 16\,\Omega$	V_S	30	V
$R_L \geqq 8\,\Omega$	V_S	24	V
$R_L \geqq 4\,\Omega$	V_S	20	V
Output peak current (not repetitive)	I_q	3.5	A
Output current (repetitive)	I_q	2.5	A
Junction temperature[1])	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
SIP 9 package			
Thermal resistance (junction-case)	$R_{th\,JC}$	12	K/W
Thermal resistance (system-air)	$R_{th\,SA}$	70	K/W
DIP 18 package			
Thermal resistance (junction-case)	$R_{th\,JC}$	35	K/W
Thermal resistance (system-air)	$R_{th\,SA}$	70	K/W

Range of operation

Supply voltage range	V_S	4 to 28	V
Ambient temperature range	T_{amb}	−25 to 85	°C

*) May not be exceeded even as instantaneous value.

Characteristics

with reference to test circuit

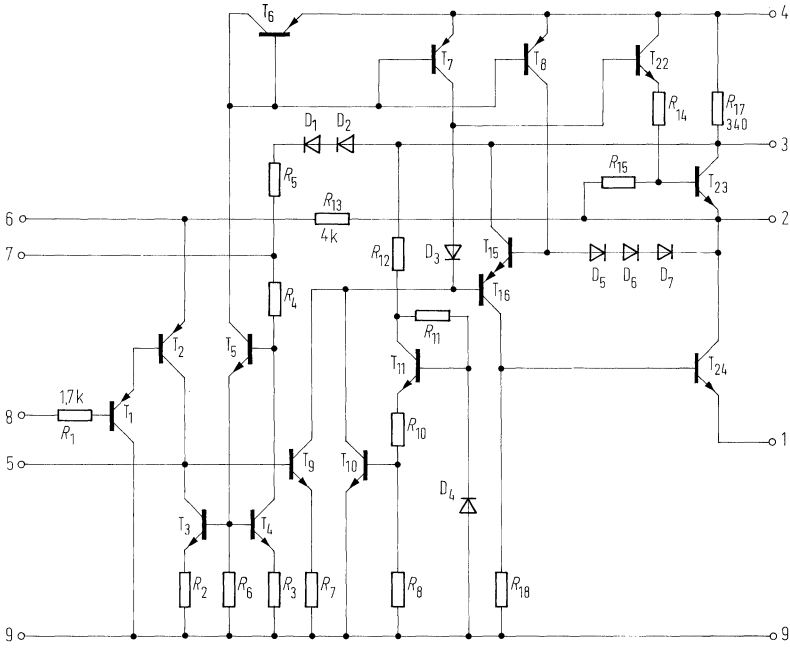
1. V_S = 12 V; R_L = 4 Ω; C_1 = 1000 µF; f_i = 1 kHz; T_{amb} = 25 °C

		min	typ	max	
Quiescent output voltage	V_{2q}	5.4	6.0	6.6	V
Quiescent drain current	I_3+I_4		12	20	mA
Input DC current	I_{8i}		0.4	4	µA
Output power THD = 1%	P_q	2.5	3.5		W
THD = 10%	P_q	3.5	4.5		W
Voltage gain (closed loop)	G_V	37	40	43	dB
Voltage gain (open loop)	G_{V0}		80		dB
Total harmonic distortion P_q = 0.05 to 2.5 W)	THD		0.2		%
Noise voltage with reference to input (f_i = 3 Hz to 20 kHz)	V_n		3.8	10	μV_S
Disturbance voltage in acc. with DIN 45405 referred to input	V_d		2.5		µV
Hum suppression (f_{hum} = 100 Hz)	a_{hum}		48		dB
Frequency range (−3 dB)					
C_4 = 560 pF	f_i	40		20000	Hz
C_4 = 1000 pF	f_i	40		10000	Hz
Input resistance	R_{8i}	1	5		MΩ

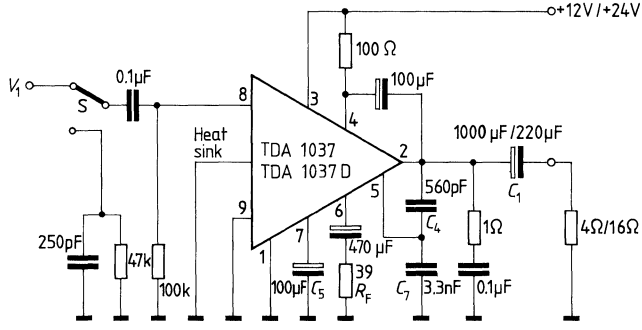
2. V_S = 24 V; R_L = 16 Ω; C_1 = 220 µF; f_i = 1 kHz; T_{amb} = 25 °C

Quiescent output voltage	V_{2q}	11	12	13	V
Quiescent drain current	I_3+I_4		18	30	mA
Input DC current	I_{8i}		0.8	8	µA
Output power THD = 1%	P_q		3.5		W
THD = 10%	P_q	4.5	5		W
Voltage gain (closed loop)	G_V	37	40	43	dB
Voltage gain (open loop)	G_{V0}		80		dB
Total harmonic distortion (P_q = 0.05 to 3 W)	THD		0.2	0.5	%
Noise voltage with reference to input (f_i = 3 Hz to 20 kHz)	V_n		5	15	μV_S
Disturbance voltage in acc. with DIN 45405 referred to input	V_d		3.8		µV
Hum suppression (f_{hum} = 100 Hz)	a_{hum}		40		dB
Frequency range (−3 dB)					
C_4 = 560 pF	f_i	40		20000	Hz
C_4 = 1000 pF	f_i	40		10000	Hz
Input resistance	R_{8i}	1	5		MΩ

Circuit diagram

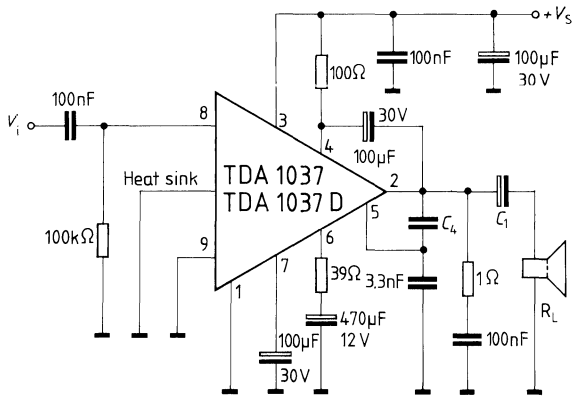


Test circuit



S switched on for noise measurement

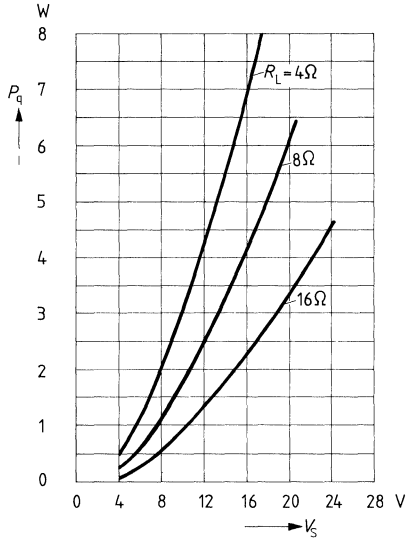
Application circuit



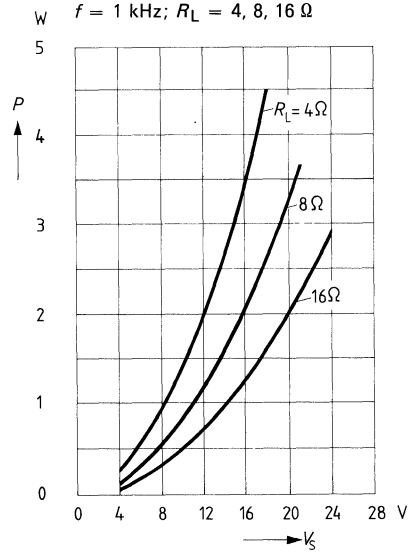
V_S	12 V	18 V	24 V
R_L	4 Ω	8 Ω	16 Ω
C_1	1000 µF	470 µF	220 µF

f_{max}	10 kHz	20 kHz
C_4	1000 pF	560 pF

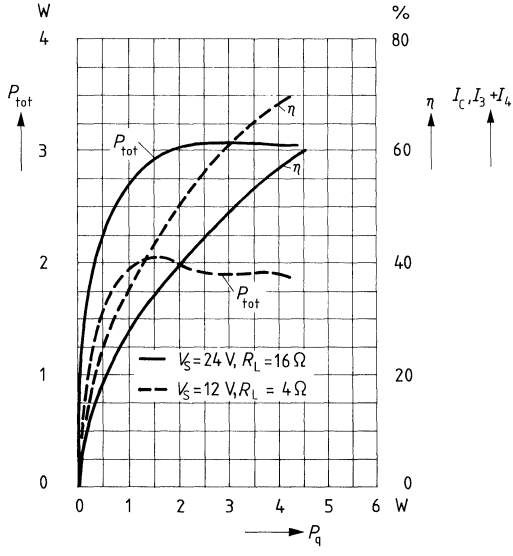
Output power versus supply voltage
THD = 10%; R_L = 4, 8, 16 Ω; *f* = 1 kHz



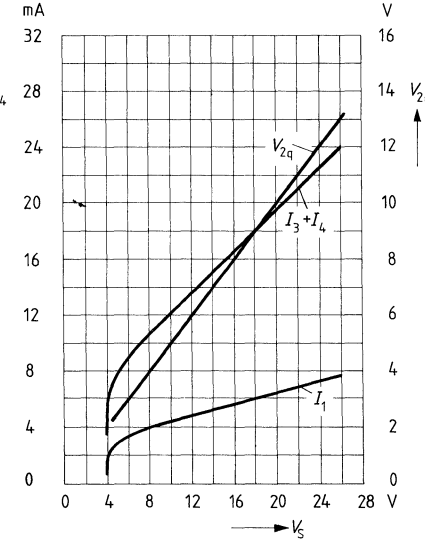
Max. power dissipation versus supply voltage at sine-shaped driving
f = 1 kHz; R_L = 4, 8, 16 Ω



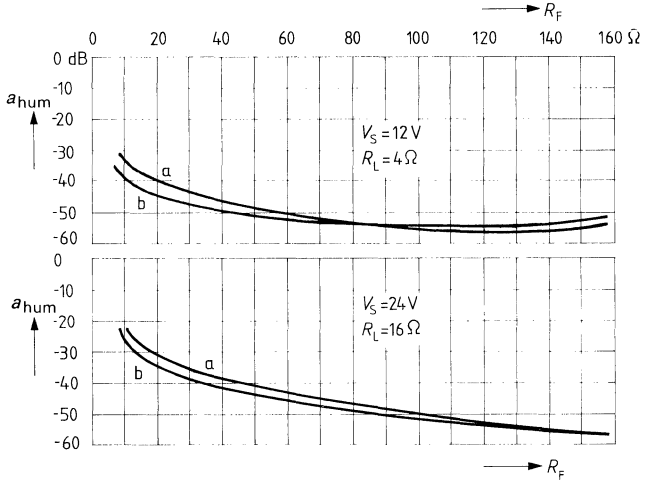
Total power dissipation and efficiency versus output power
THD = 10%; *f* = 1 kHz



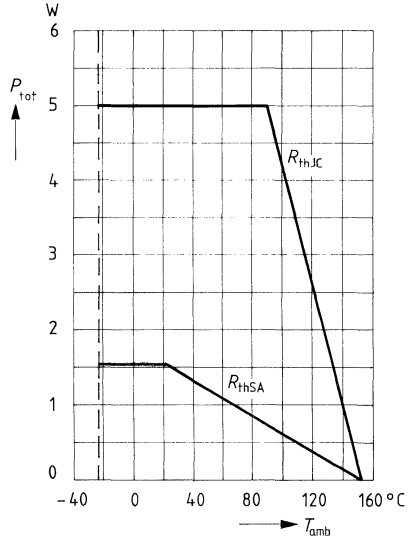
Quiescent drain current, quiescent current of output transistors, quiescent output voltage versus supply voltage



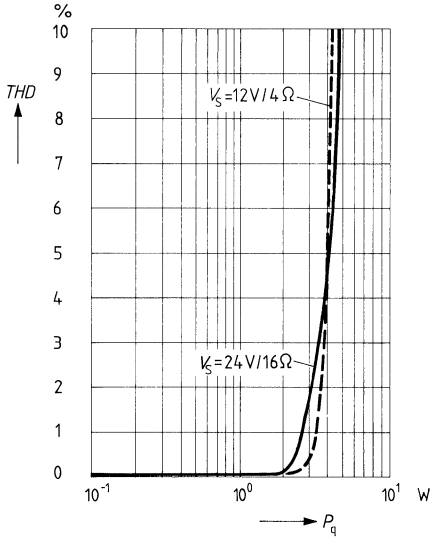
Hum suppression versus feedback resistance
f_{hum} = 100 Hz; C_5 = 100 µF
a: input short-circuited
b: input open



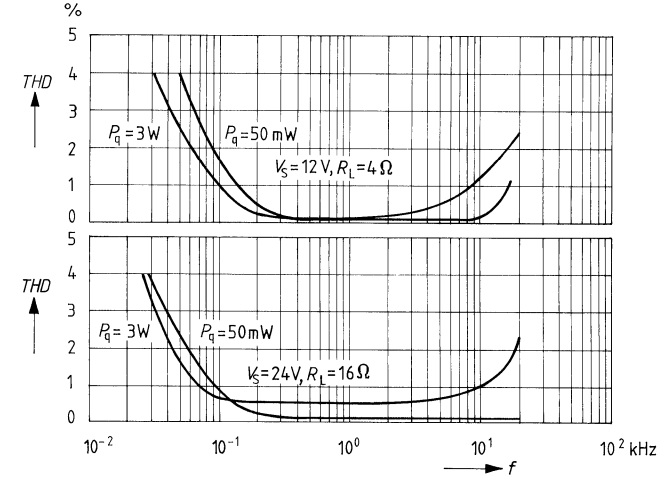
Max. total power dissipation versus ambient temperature



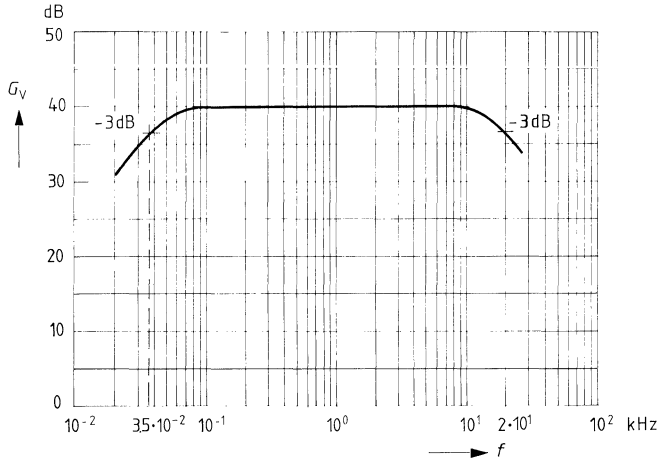
Total harmonic distortion versus output power
$f = 1$ kHz



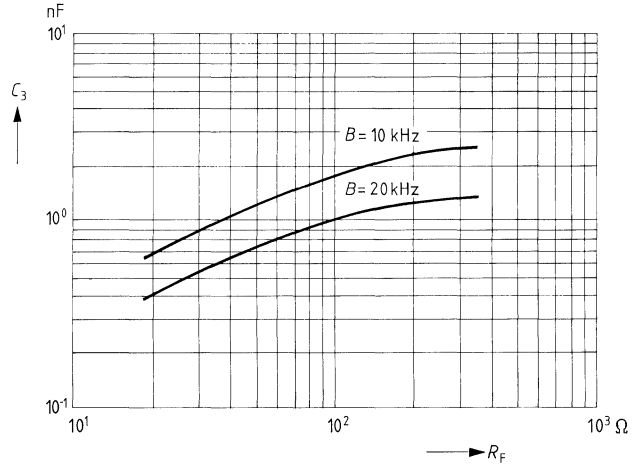
Total harmonic distortion versus frequency



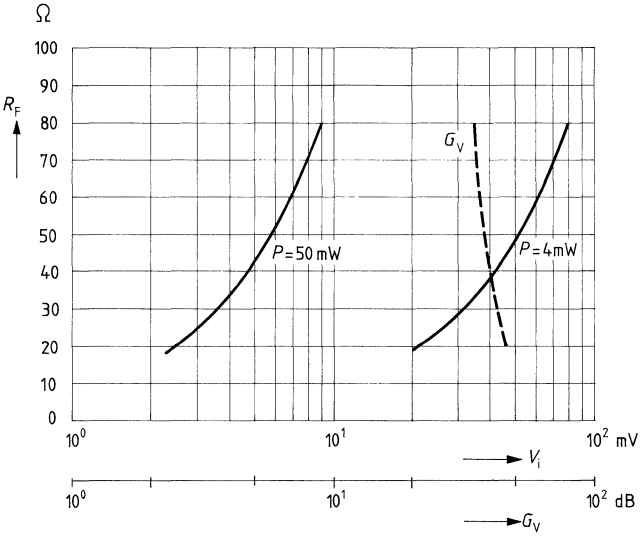
Voltage gain versus frequency
V_S = 12 V; R_L = 4 Ω



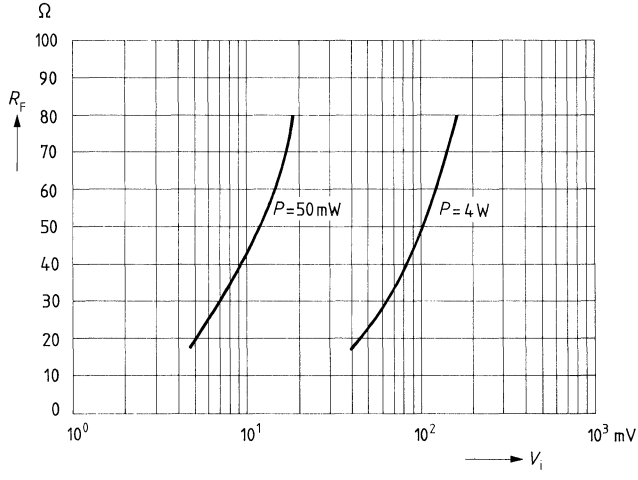
Bandwidth C_3 versus feedback resistance
V_S = 12 V; R_L = 4 Ω, G_V = 40 dB
$C_1 = 5 \cdot C_4$



Output power and voltage gain versus feedback resistance and input voltage
V_S = 12 V; R_L = 4 Ω; f = 1 kHz



Output power versus feedback resistance and input voltage
V_S = 24 V; R_L = 16 Ω; f = 1 kHz



Bipolar circuit

The TDA 2003 is an audio power amplifier in a TO 220 Pentawatt case. This IC is particularly intended for use in car radios, it also meets the requirements of AF amplifiers for supply voltages between 8 and 18 V. At low harmonic distortion, the TDA 2003 produces an output power of 6 W at 4 Ω and V_S = 14.4 V. Operation at 2 Ω enhances the output power to 10 W.

Included thermal shutdown protects the IC against damage from short circuits and thermal overload.

- High output peak current up to 3.5 A
- Low distortion and low *THD*
- Electrical and thermal overload protection
- Few external components
- Easy mounting thanks to TO 220/5 case

Type	Ordering code	Package outline
TDA 2003	Q 67000-A 1606	Plastic power case TO 220/5, or TO 220/5-H

Maximum ratings

Supply voltage	V_S	28	V
Peak supply voltage ($t \leqq 50$ ms)	V_S	40	V
Output current (repetitive)	$I_{q\,4}$	3,5	A
Output peak current (non-repetitive)	$I_{q\,5}$	4,5	A
Thermal resistance (junction-case)	$R_{th\,JC}$	5	K/W
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C

Range of operation

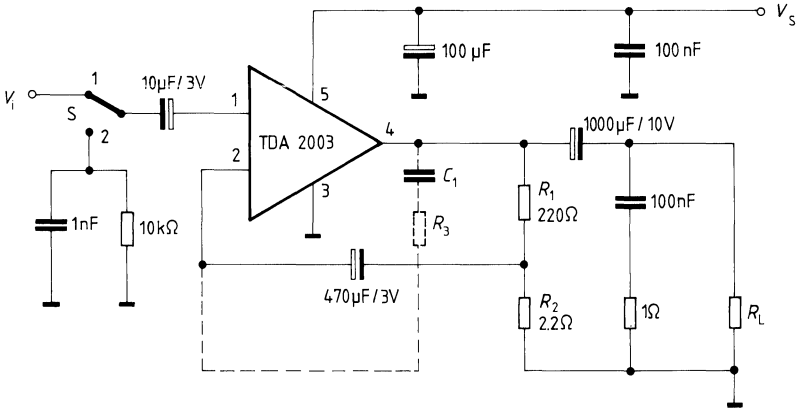
Supply voltage range	V_S	8 to 18	V
Ambient temperature range	T_{amb}	−20 to 85	°C

Characteristics (with reference to test circuit, $V_S = 14.4$ V; $T_{amb} = 25$ °C)

		min	typ	max	
Quiescent output voltage	$V_{q\,4}$	6.3	6.9	7.5	V
Quiescent drain voltage	I_5		45	80	mA
Output power ($THD = 10\%$, $f = 1$ kHz)					
$R_L = 4\,\Omega$	$P_{q\,4}$	5.5	6		W
$R_L = 2\,\Omega$	$P_{q\,4}$	8	10		W
$R_L = 3.2\,\Omega$	$P_{q\,4}$		7.5		W
$R_L = 1.6\,\Omega$	$P_{q\,4}$		12		W
Input voltage	V_i		300		mV
Hum suppression ($R_L = 4\,\Omega$, $f_{hum} = 100$ Hz; $V_{hum} = 0.5$ V)	a_{hum}	34	40		dB
Input resistance	R_i	100	150		kΩ
Input voltage ($G_v = 40$ dB)					
$P_q = 0.5$ W, $R_L = 4\,\Omega$	V_i		15		mV
$P_q = 0.5$ W, $R_L = 2\,\Omega$	V_i		11		mV
$P_q = 6$ W, $R_L = 4\,\Omega$	V_i		60		mV
$P_q = 6$ W, $R_L = 2\,\Omega$	V_i		50		mV
Frequency range (−3 dB) ($C_1 = 39$ nF, $R_3 = 39\,\Omega$)			40 to 50 000		Hz
Total harmonic distortion ($f_i = 1$ kHz)					
$P_q = 0.05$ to 3.5 W, $R_L = 4\,\Omega$	THD		0.2		%
$P_q = 0.05$ to 5 W, $R_L = 2\,\Omega$	THD		0.2		%
Voltage gain					
$R_L = 4\,\Omega$ open loop	G_{vo}		80		dB
closed loop	G_{vc}	39.5	40	40.5	dB
Disturbance voltage (DIN 45405)	V_d		2	5	μV
Noise voltage (DIN 45405)	V_n		3	8	μV
Input noise current	I_{in}		50		pA
B (−3 dB) 40 to 50 000 Hz					
Thermal resistance (junction-case)	$\Delta R_{th\,JC}$[1])			1	K/W

[1]) $\Delta R_{th\,JC}$ is the variation of $R_{th\,JC}$ throughout a period of time at a given power $P_\Delta = \frac{P_{max}}{3}$

Test and application circuit



Switch S in position 2 for noise measurement

Bipolar circuit

The TDA 2030 is an audio power amplifier in a TO 220 Pentawatt case, designed as a B class amplifier. At low harmonic distortion and high output currents, the TDA 2030 produces an output power of 14 W at 4 Ω and $V_S = \pm 14$ V. Included thermal shutdown protects the IC against damage from short circuits and thermal overload.

- High output peak current up to 3.5 V
- High supply voltage up to 36 V
- Low distortion and low *THD*
- Electrical and thermal overload protection
- Few external components

Type	Ordering code	Package outline
TDA 2030	Q 67000-A 1607	Plastic power case TO 220/5, or TO 220/5-H

Maximum ratings

Supply voltage	$\pm V_S$	18	V
Input voltage	V_{i1}, V_{i2}	$\pm V_S$	V
Differential input voltage	$V_{i\,D1\text{-}2}$	± 30	V
Output peak current	I_{q4}	3.5	A
Thermal resistance (system-case)	$R_{th\,JC}$	4	K/W
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C

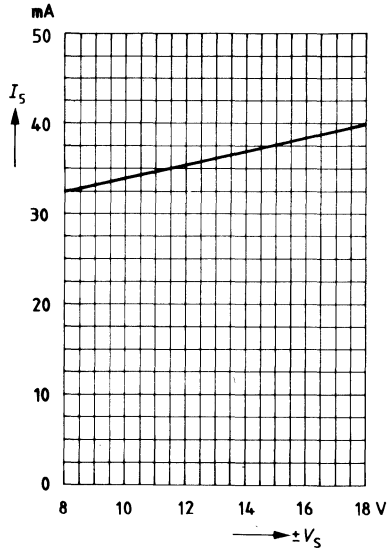
Range of operation

Supply voltage range	$\pm V_S$	6 to 18	V
Ambient temperature range	T_{amb}	0 to 70	°C

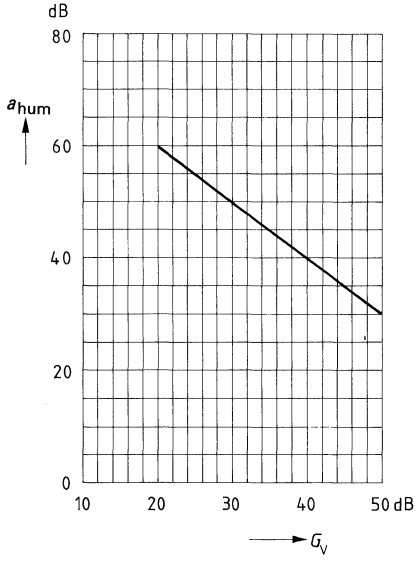
Characteristics ($\pm V_S$ = 14 V; T_{amb} = 25 °C; f = 1 kHz; test circuit 1) unless otherwise specified

		min	typ	max	
Quiescent drain current $\pm V_S$ = 18 V, R_L = 4 Ω	I_5		40	60	mA
Total current consumption					
P_q = 15 W, R_L = 4 Ω	$I_{tot\,5}$		925		mA
P_q = 9 W, R_L = 8 Ω	$I_{tot\,5}$		515		mA
Input voltage					
P_q = 12 W, R_L = 4 Ω	V_i		215		mV
P_q = 8 W, R_L = 8 Ω	V_i		250		mV
Input resistance	R_i	0.5	5		mΩ
Frequency range (−3 dB) $\pm V_S$ = 18 V, R_L = 4 Ω			10 to 140 000		Hz
Total harmonic distortion					
P_q = 0.1 to 12 W, R_L = 4 Ω	THD		0.2	0.5	%
P_q = 0.1 to 8 W, R_L = 8 Ω	THD		0.1	0.5	%
Voltage gain					
open loop	G_{vo}		90		dB
closed loop	G_{vc}		30		dB
Disturbance voltage (in acc. with DIN 45405 referred to input)	V_d		3		μV
Noise voltage (in acc. with DIN 45405 referred to input)	V_n		4.5	15	μV_S
Thermal shutdown P_{tot} = 12 W	T_{case}	110			°C
Hum suppression R_L = 4 Ω, V_{hum} = 0.5 V f_{hum} = 100 Hz, R_G = 22 kΩ	a_{hum}	40	50		dB
Input offset voltage $\pm V_S$ = 18 V	$V_{i\,1\text{-}2}$		±2	±20	mV
Input offset current $\pm V_S$ = 18 V	$I_{i\,1\text{-}2}$		±20	±200	nA
Input current $\pm V_S$ = 18 V	$I_{i\,1,2}$		0.2	1	μA
Output offset voltage $\pm V_S$ = 18 V	$V_{q\,4}$		±2,5	±22	mV
Output power					
THD = 0.5%, R_L = 4 Ω	P_q	12	14		W
THD = 0.5%, R_L = 8 Ω	P_q	8	9		W
THD = 10%, R_L = 4 Ω	P_q		18		W
THD = 10%, R_L = 8 Ω	P_q		11		W

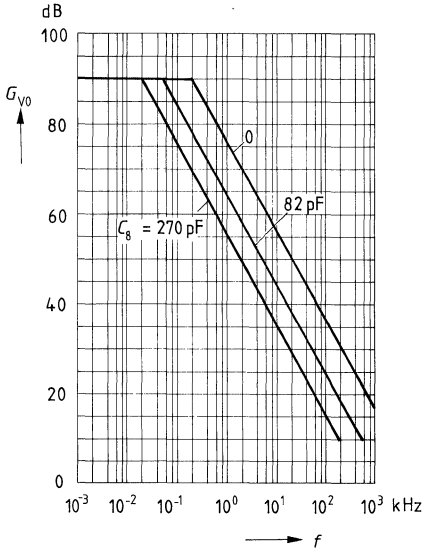
Quiescent drain current versus supply voltage



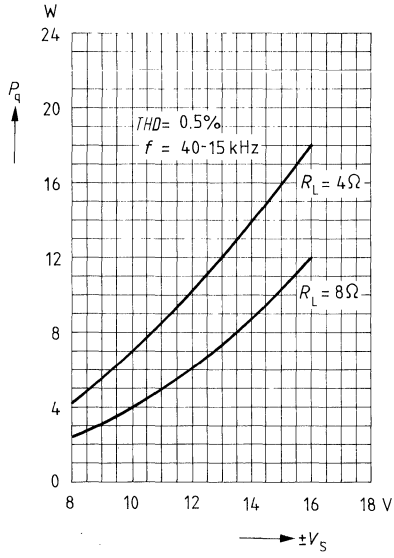
Hum suppression versus voltage gain



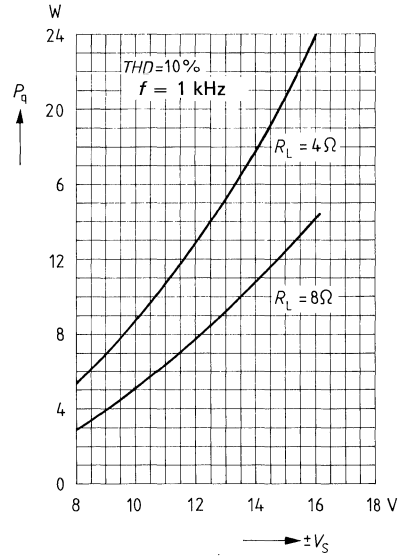
Open loop voltage gain versus frequency



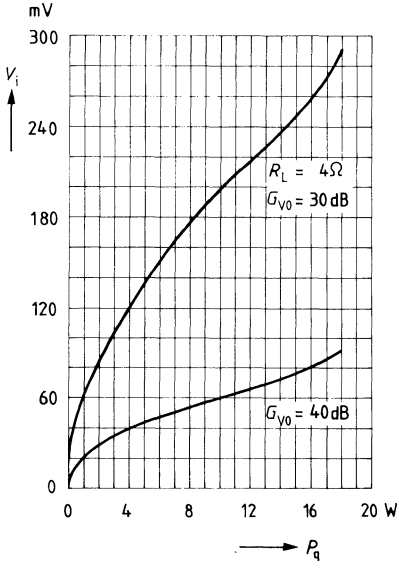
Output power versus supply voltage



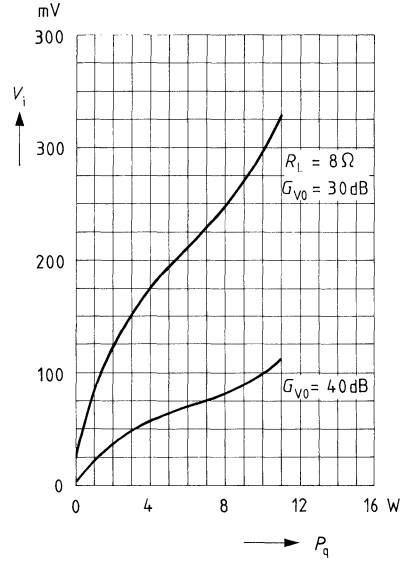
Output power versus supply voltage



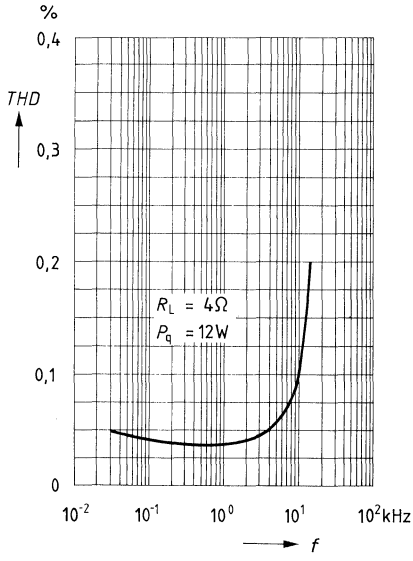
Input voltage versus output power



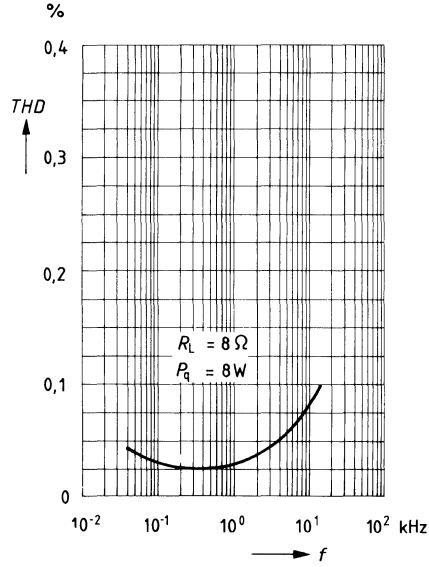
Input voltage versus output power



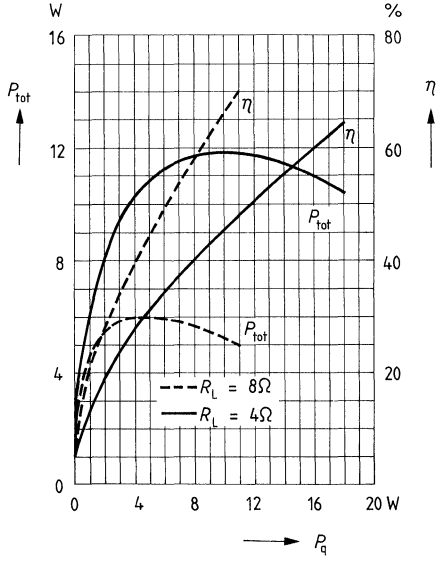
Total harmonic distortion THD versus frequency



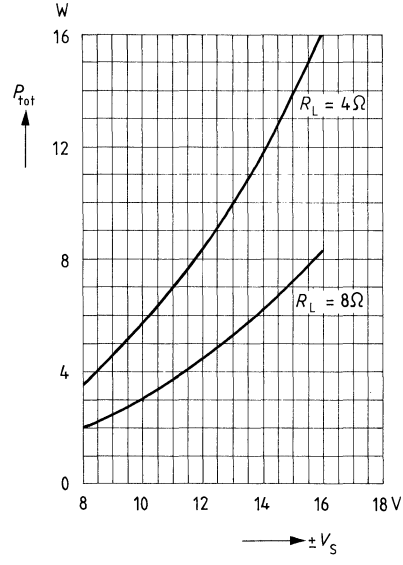
Total harmonic distortion THD versus frequency



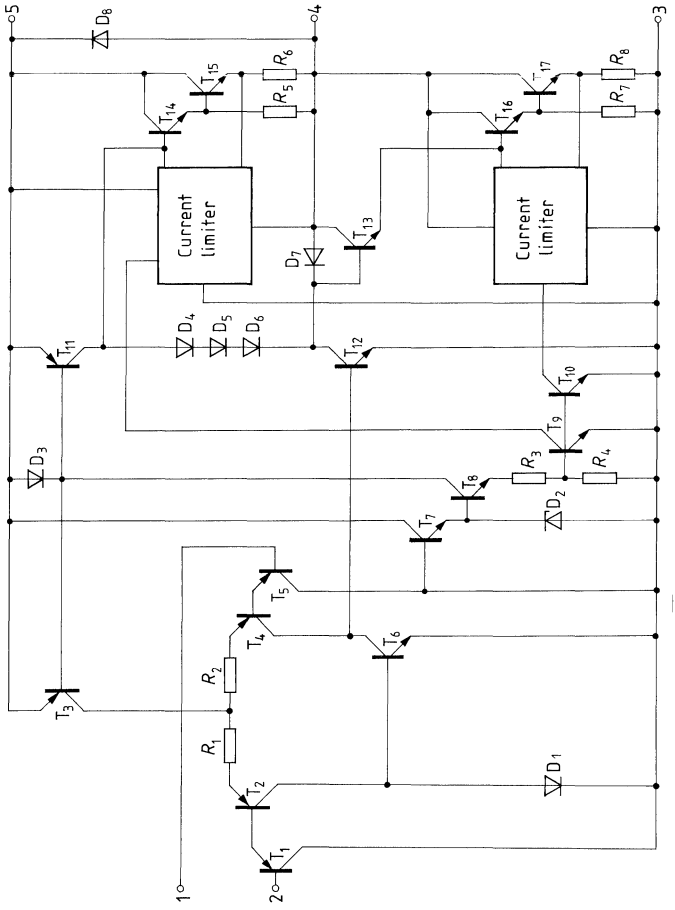
Total power dissipation or efficiency, resp., versus power output



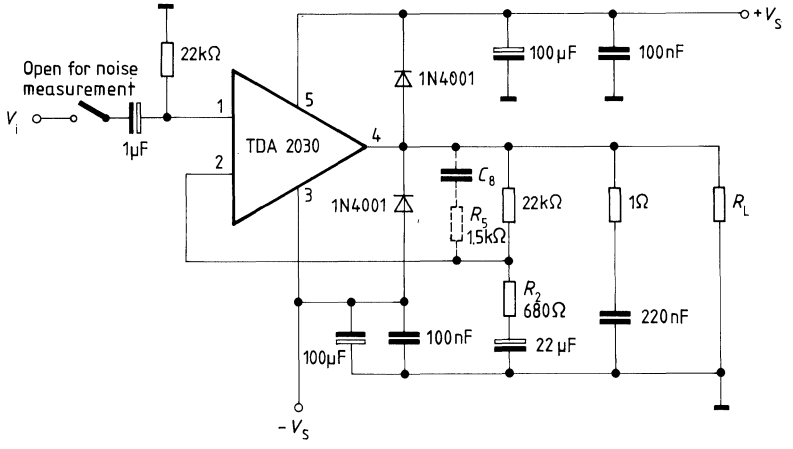
Total power dissipation versus supply voltage



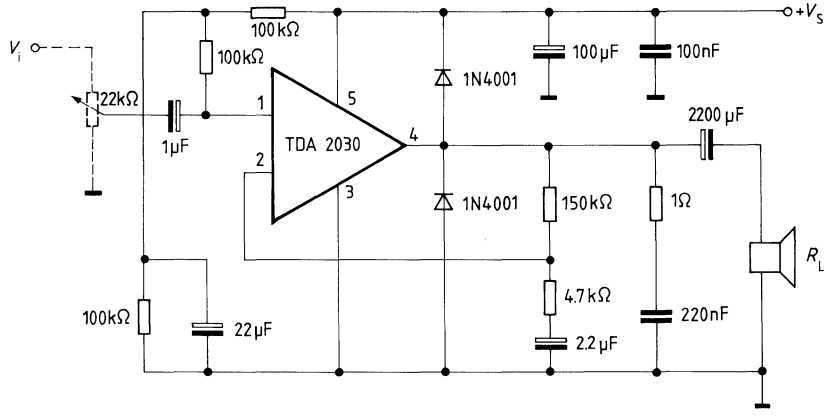
Circuit diagram



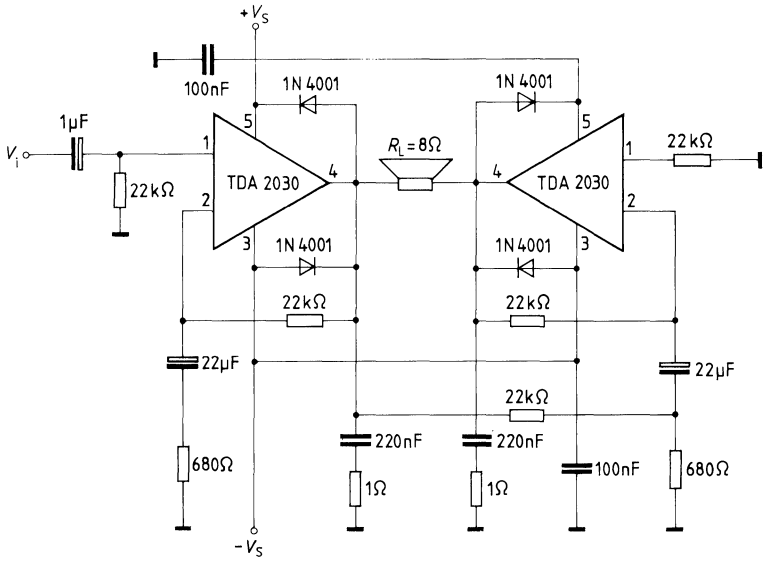
Test and application circuit 1
AF amplifier with split power supply



Application circuit 2
AF amplifier with single power supply



Application circuit 3



Bridge amplifier with split power supply

15 W AF Power Amplifier with Short-Circuit Protection

TDA 3000

Bipolar circuit

AF power amplifier intended for appliances of entertainment electronics. The amplifier operates in push-pull B mode and is available in a TO 220 case with 7 pins. Included thermal shutdown protects the IC against damage from short circuits and thermal overload.

- High output power up to 15 W
- High output current up to 3.5 A
- Easy mounting thanks to TO 220/7 case

Type	Ordering code	Package outline
TDA 3000	Q67000-A1332	Plastic power case TO 220/7

Maximum ratings (restricted data $V_S \leqq 26$ V)

Supply voltage $R_L = 8\,\Omega$	V_6	32	V
Supply voltage $R_L = 4\,\Omega$	V_6	26	V
Boost voltage	V_7	32	V
Input voltage	V_2	5	V
Output current (repetitive)	$I_{q\,5}$	3.5	A
Output peak current (non-repetitive)	$I_{q\,5}$	5	A
Thermal resistance (junction-case)	$R_{th\,JC}$	4	K/W
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C

Range of operation

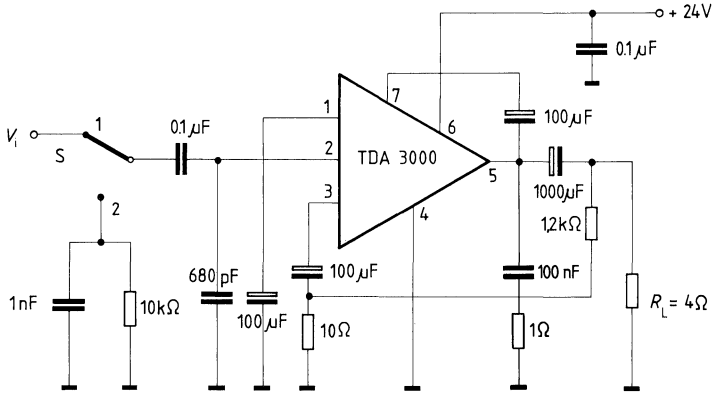
Operating voltage range	V_6	9 to 32	V
Ambient temperature range	T_{amb}	0 to 70	°C

In order to ensure that the maximum permissible voltage of 26 V at pin 7 will in no case be exceeded, a resistance of 100 Ω must be connected in series with the boost capacitor between pin 5 and pin 7 for current and voltage limitation in case of supply voltages of $16\text{ V} < V_S < 26\text{ V}$.

Characteristics (with reference to the test circuit $V_6 = 24\,V$, $T_{amb} = 25\,°C$, $R_L = 4\,\Omega$)

		min	typ	max	
Quiescent drain current	I_6		40	60	mA
Quiescent output voltage	V_5	11.3	12	12.7	V
Output power					
($THD = 10\%$, $f = 1$ kHz)	$P_{q\,5}$	12	15		W
($THD = 1\%$, $f = 1$ kHz)	$P_{q\,5}$	10	12		W
Voltage gain (closed loop)	G_v	39	40	41	dB
Input sensitivity ($P_q = 1$ W)	V_i		20		mV
Total harmonic distortion	THD		0.2	0.5	%
($P = 0.05$ to 8 W, $f = 0.1; 1; 10$ kHz)					
Frequency range (−3 dB)	f_i	0.05		20	kHz
Input saturation voltage ($THD \leqq 1\%$)	$V_{i\,max}$	1			V_{rms}
Input resistance	$R_{i\,2}$	70	120		kΩ
Voltage gain (open loop)	G_{vo}		80		dB
Hum suppression	a_{hum}		45		dB
($f_{hum} = 100$ Hz, $V_{hum} < 2\,V_{pp}$)					
Disturbance voltage	V_d		3		μV
(in acc. with DIN 45405 referred to input)					
Noise voltage	V_n		8	15	μV_S
(in acc. with DIN 45405 referred to input)					

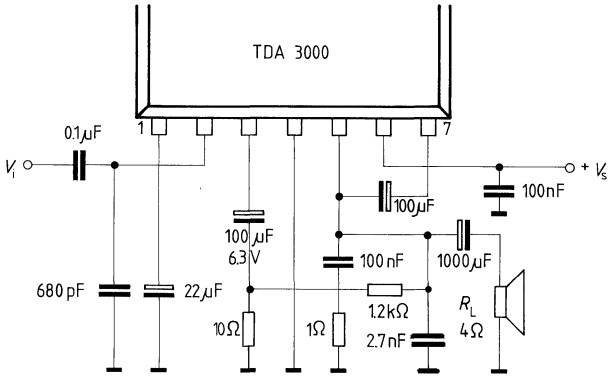
Test circuit



Switch S in position 2 for noise measurement.

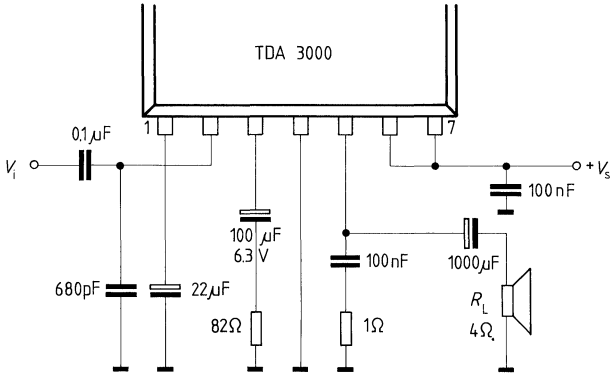
Application circuit 1

This circuit is recommended for supply voltages $\leqq$ 20 V, since a boost voltage is supplied to pin 7 in order to increase the power at pin 6. The push-pull resistance of 1.2 kΩ reduces the leakage range of the voltage gain to limits as given in our data sheets.



Application circuit 2

with minimized external components



LED Driver for Light Spot Displays

UAA 170
■ UAA 170 L

Bipolar circuit

■ Not for new design

IC for driving 16 light emitting diodes. Depending on the input voltage, the individual LEDs are driven within one row in form of a light spot. Whereas the UAA 170 provides a linear relation between control voltage and the driven LED, the UAA 170 L has a nearly logarithmical characteristic. With the aid of suitable circuitry, the brightness of the LEDs can be varied and the crossing over of the light spot can be set between "smooth" and "abrupt". By connecting two ICs in parallel, up to 30 LEDs can be driven.

Type	Ordering code	Package outline
UAA 170	Q 67000-A 940	DIP 16
UAA 170 L	Q 67000-A 1362	

Maximum ratings

Supply voltage	V_S	18	V
Input voltages	V_{11}, V_{12}, V_{13}	6	V
Load current	I_{14}	5	mA
Junction temperature	T_j	150	°C
Thermal resistance (system-air)	$R_{th\ SA}$	90	K/W
Storage temperature range	T_{stg}	−40 to 125	°C

Range of operation

Supply voltage (LED red) [1])	V_S	11 to 18	V
Ambient temperature range	T_{amb}	−25 to 85	°C

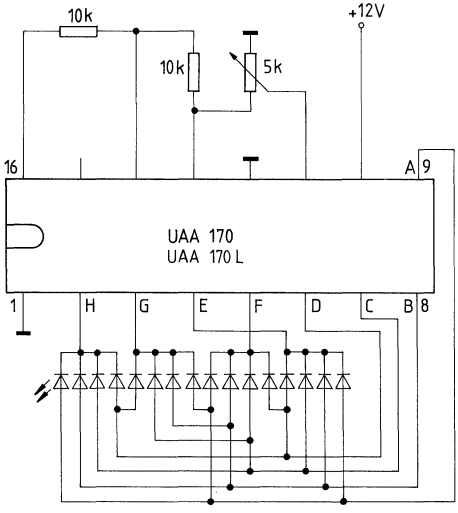
[1]) The lower limit is only valid for a forward voltage of the LED's of approx. 1.5 V (red LED's); the lower limit increases according to higher forward voltage.

■ Not for new design

Characteristics (V_S = 12 V; T_{amb} = 25 °C)

		min	typ	max	
Current consumption (I_{14} = 0; I_{16} = 0)	I_S	2	4	10	mA
Control input current	I_{11}	−2			µA
Reference input current	I_{12}, I_{13}	−2			µA
Voltage difference	$\Delta V_{12/13}$	1.4		6	V
Voltage difference for gliding light transition UAA 170, only	$\Delta V_{12/13}$	1.4			V
Voltage difference for jumping light transition UAA 170, only	$\Delta V_{12/13}$	4			V
Voltage difference	$\Delta V_{12/13}$	4			V
Stabilized voltage I_{14} = 300 µA	V_{14}		5	6	V
I_{14} = 5 mA	V_{14}	4.5			V
Reference input voltage	$V_{ref\ max}$	1.4		6	V
	$U_{ref\ min}$	0		4.6	V
Tolerance of forward voltages of LEDs, mutually	ΔV_D			0.5	V
Output current for LEDs	ΣI_D		25		mA

Test circuit



Scale display with light emitting diodes

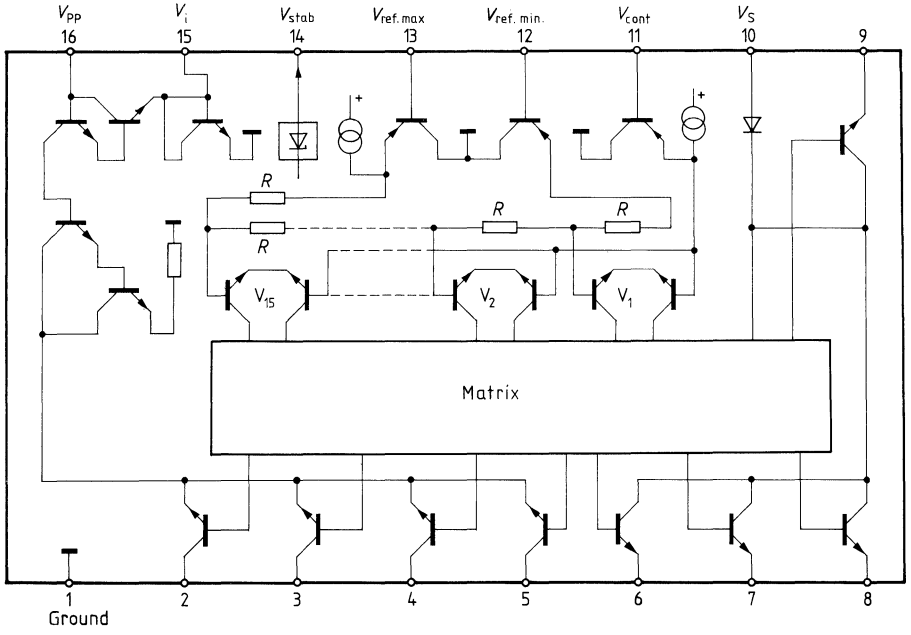
Scale displays by means of a wandering light point are particularly suitable for indicating approximate values. Applications of this kind are level sensors, VU-meters, tachometers, radio scales etc. When applying the displays in measuring equipment, multicolored light emitting diodes can be used as range limitation. Ring scales are obtained by a circular arrangement of the diodes. The IC UAA 170 has especially been developed for driving a scale of 16 LEDs.

The input voltages at pins 11, 12 and 13 are freely selectable in the range between 0 and 6 V. Any kind of adjustment, is enabled by suitable voltage dividers. The DC value V_{cont} is always assigned to a certain spot of the diode chain.

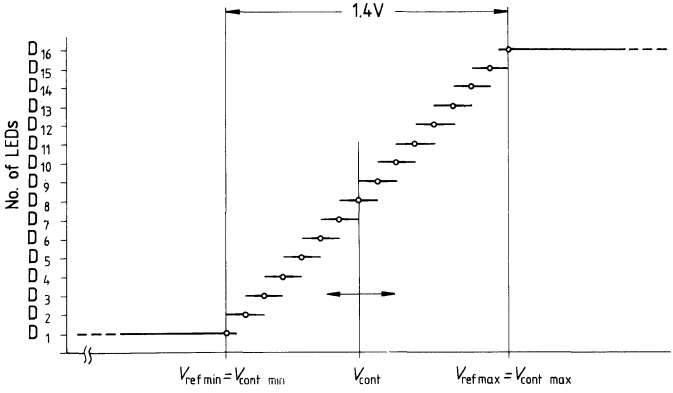
The voltage difference between pins 12 and 13 thereby corresponds to the possible indication range. $\Delta V_{12/13}$ defines at the same time the light transition between two diodes. With $\Delta V_{12/13}$approx. 1.4 V, the light point glides smoothly along the scale. With increasing voltage difference, the passage becomes more abrupt. With $\Delta V_{12/13}$ approx. 4 V, the light point jumps from diode to diode.

Input voltages beyond the selected indication range cause the diodes D_1 or D_{16} respectively, to light up, thereby exceeding of the range can only be recognized.

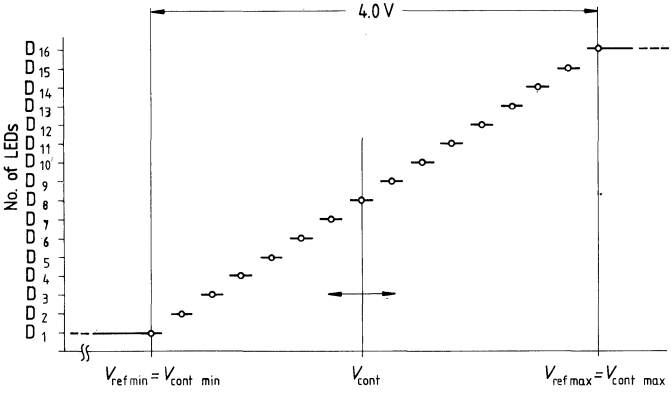
Block diagram



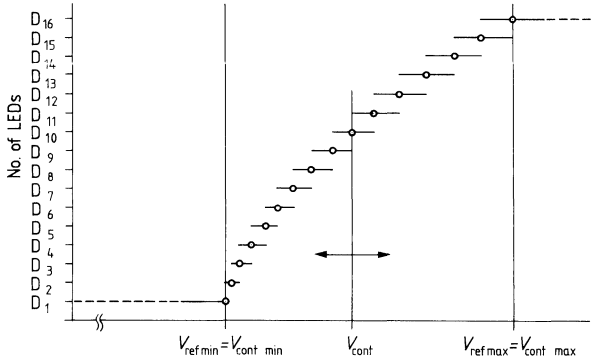
Indication for gliding transition UAA 170



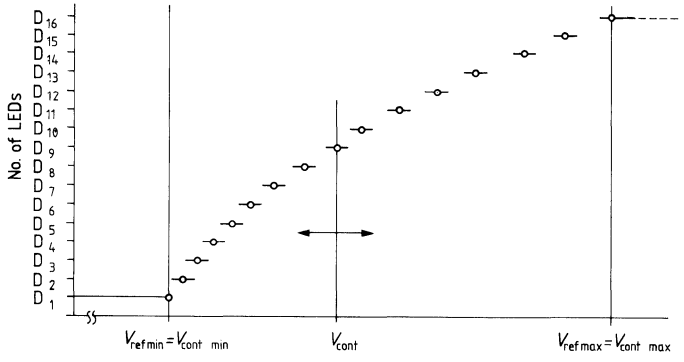
Indication for jumping transition UAA 170



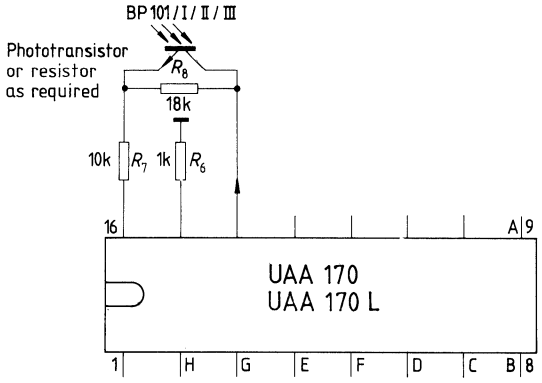
Indication for gliding transition UAA 170 L



Indication for jumping transition UAA 170 L



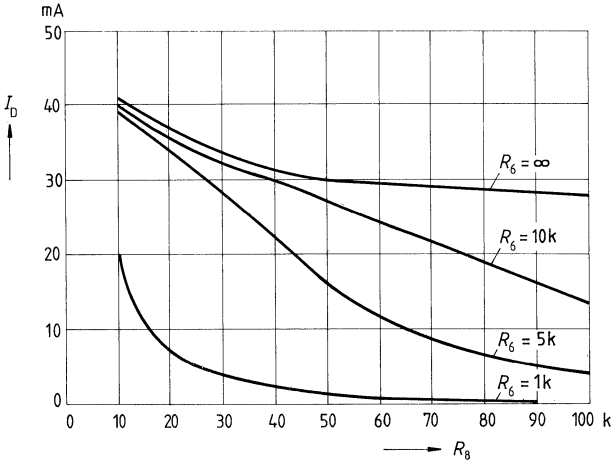
Brightness control



Pins 14, 15, and 16 serve to determine the diode current. Corresponding to the desired light intensity, the forward current of the diodes is linearly variable in the range I_f approx. 0 to 50 mA. The resistance at pin 15 defines the adjusting range. The resistances between pin 14 and 16 determine the current.

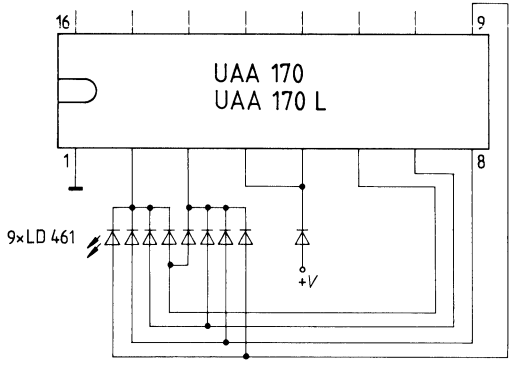
With the aid of a phototransistor, such as BP 101, the light intensity of the LEDs can be matched to a varying brightness of the environment.

Diode current versus base emitter resistor
V_S = 12 V; T_{amb} = 25 °C; V_{14} = 5.4 V; red LEDs

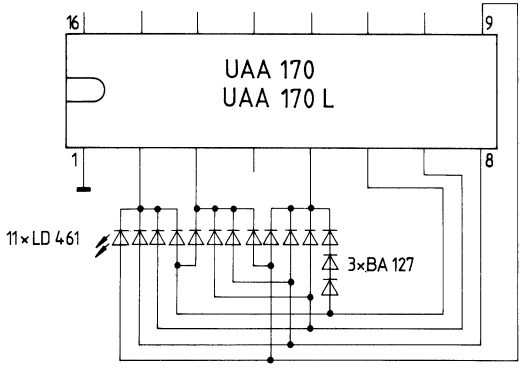


Operation of less than 16 LEDs

Control of 9 LEDs

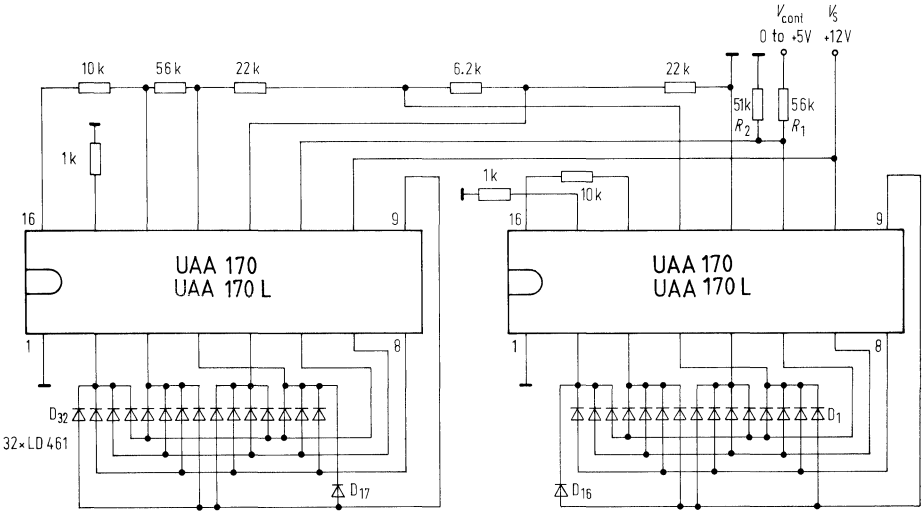


Control of 11 LEDs



Application circuit for the control of 30 LEDs with 2 x UAA 170

Range of control voltage V_{cont} = 0 to 5 V
Voltage difference $V_{12/13}$ = 2 × 1.2 V = 2.4 V.
Since the diodes D_{16} or D_{17} are permanently lighting up when the maximum or minimum voltages V_{13} or V_{12} adjusted by R_3, R_4, R_5, are exceeded or fallen below, the diodes should be covered, if necessary.



The figure shows an extension of the circuit to 30 diodes with 2 UAA 170. The diodes D_{16} or D_{17} light permanently, when the reciprocal absolute ratings are exceeded. They should be covered. The reference voltage $\Delta V_{12/13}$ = 2 × 1.2 = 2.4 V is derived from a stabilized dc voltage of typ. 5 V available at pin 14. A resistance of 6.2 kΩ provides an overlapping of the ranges in order to ensure a smooth transition from D_{15} to D_{18}. The control voltage V_{cont} is fed to pins 11 parallel via a divider $R_1 : R_2$. The voltage divider is to be dimensioned according to the desired input voltage. With a divider current of I = 100 µA and a control voltage of V_{cont} = 10 V, the following are valid:

$$R_2 = \frac{\Delta V_{12/13}}{I} = \frac{2.4}{0.1} = 24\ \text{k}\Omega \text{ and}$$

$$R_1 = \frac{V_{cont} - \Delta V_{12/13}}{I} = \frac{7.6}{0.1} = 76\ \text{k}\Omega$$

The nearest standard value is R_1 = 75 kΩ. The voltage difference for switching one step is then $\Delta V_{cont} = \frac{10\ \text{V}}{30} = 0.16\ \text{V}$.

Bipolar circuit

Integrated circuit for driving 12 light emitting diodes. Corresponding to the input voltage the LEDs forming a light band are controlled similar to a thermometer scale.

By appropriate circuitry the brightness of the LEDs can be varied and the light passage between two adjacent LEDs can be arranged between "smooth" and "jumping".

Type	Ordering code	Package outline
UAA 180	Q67000-A1104	DIP 18

Maximum ratings

Supply voltage	V_S	18	V
Input voltage	V_3	6	V
	V_{16}	6	V
	V_{17}	6	V
Thermal resistance (system air)	$R_{th\ SA}$	120	K/W
Storage temperature range	T_{stg}	−40 to 125	°C
Junction temperature	T_j	150	°C

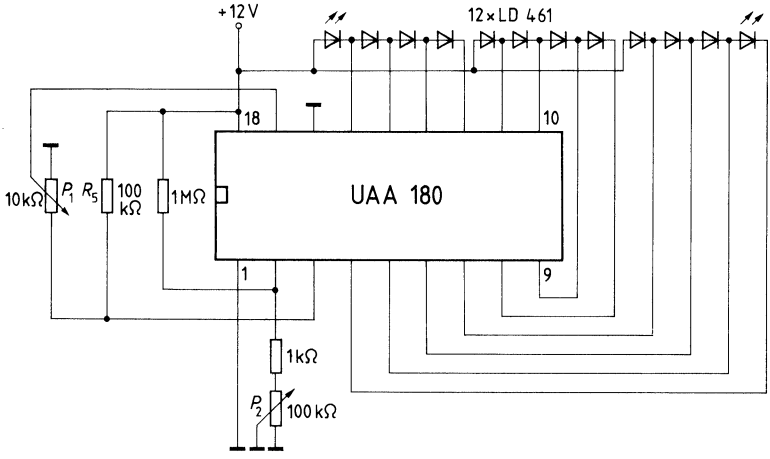
Range of operation

Supply voltage range	V_S	10 to 18	V
Ambient temperature range	T_{amb}	−25 to 85	°C

Characteristics (V_S = 12 V, T_{amb} = 25 °C)

		min	typ	max	
Current consumption (I_2 = 0) (without LED current)	I_{18}		5.5	8.2	mA
Input currents	I_3		0.3	1	µA
($V_3 - V_{16} < 2$ V)	I_{16}		0.3	1	µA
	I_{17}		0.3	1	µA
Voltage difference for smooth light transition	$V_{16/3}$	1			V
Voltage difference for jumping light transition	$V_{16/3}$	4			V
Diode current per diode	I_D		10		mA
Tolerance of LED forward voltages	ΔV_D			1	V

Test circuit



P_1 light band test
P_2 brightness test

Scale display with light emitting diodes

Scale displays by means of a growing light band are particularly suitable for the measuring of approximate values. Applications of this kind are level sensors, VU meters, tachometers, field strength indicators etc. When applying the displays in measuring equipment, multicolored LEDs can be used as range limitation.

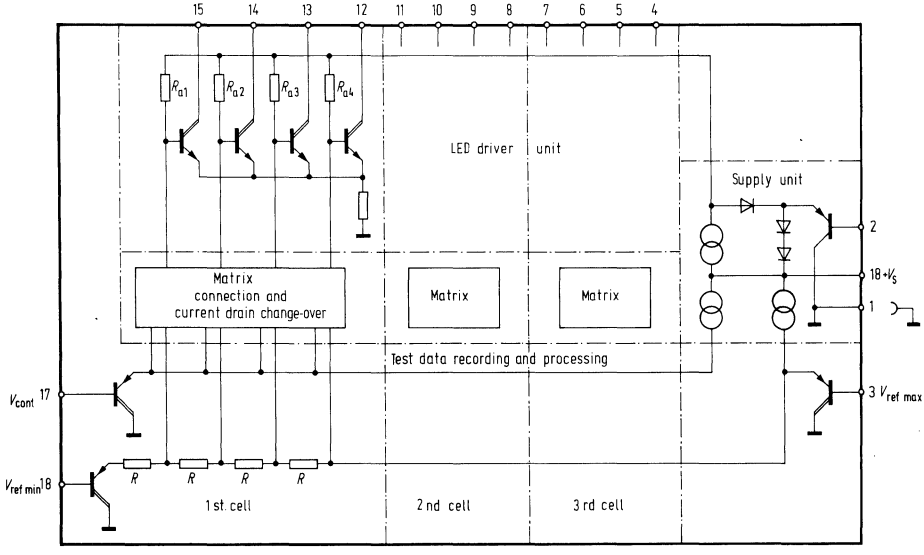
The voltage difference between pins 16 and 3 thereby corresponds to the possible indication range. $\Delta V_{16/3}$ defines at the same time the light passage between two diodes. With $\Delta V_{16/3} \geqq 1$ V, the light band glides smoothly along the scale. With increasing voltage difference, the passage becomes more abrupt. With $\Delta V_{16/3}$ approx. 4 V, the light band jumps from diode to diode.

Each quartet must consist of homogeneous diodes in order to ensure the function. Therefore, it is possible to provide the first and third quartet lighting red and the second quartet green in order to mark a working range.

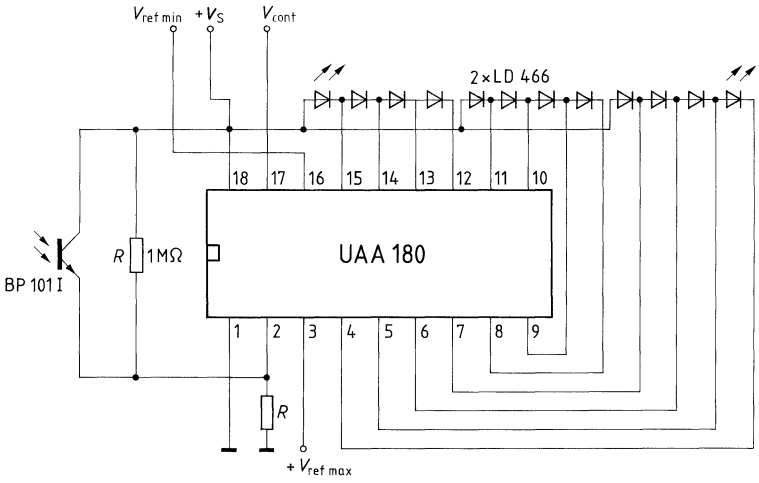
Pin 2 serves to determine the diode current. Corresponding to the desired light intensity, the forward current of the diodes is variably linear in the range I_f approx. 0 to 10 mA.

Application circuit1 shows the possibility of designing this resistance, adjustable by means of a phototransistor BP 101, in order to adapt the light intensity to changing ambient brightness. The adjusting range of the diode current lies between I_f approx. 5 mA (BP 101 not lighted) and I_f approx. 10 mA (BP 101 fully lighted). If pin 2 is open the diode current is 10 mA.

Block diagram

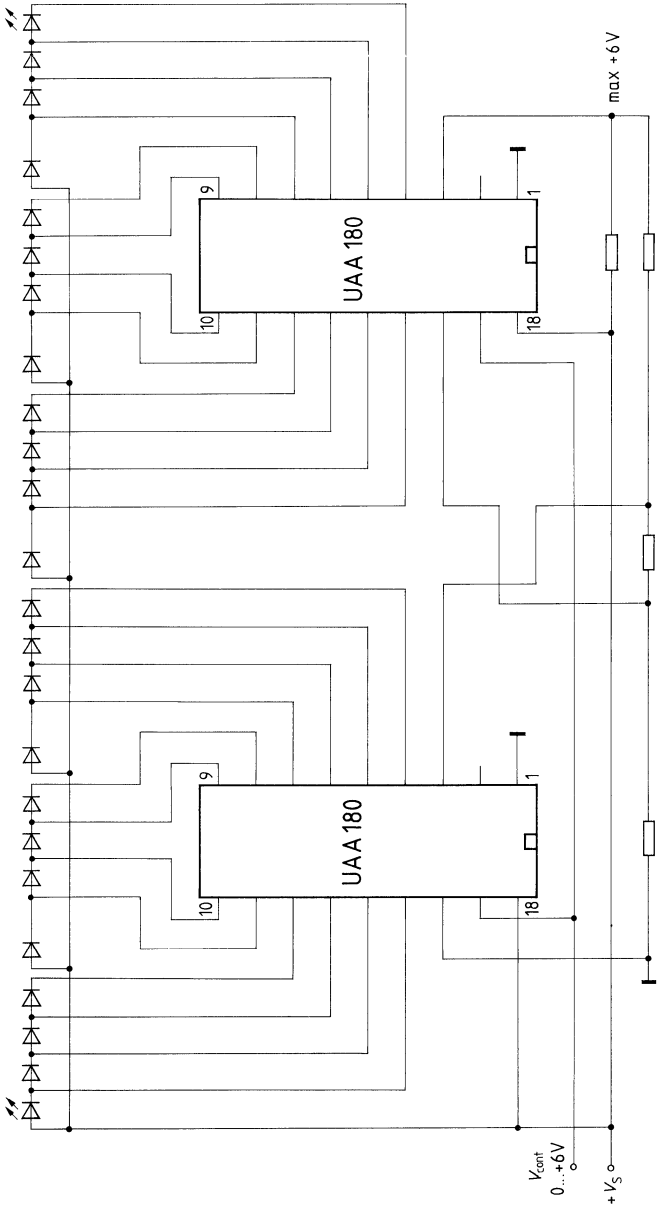


Application circuit 1



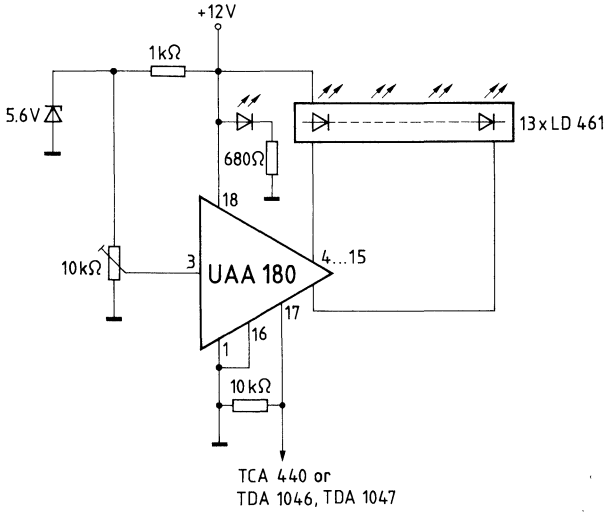
If a quartet does not need the full number of display diodes and if the first wired diodes shall be left luminous at full driving, bridges have to be inserted replacing the missing LEDs. Otherwise the first diodes of the quartet switch off with exceeding their display range.

Application circuit 2
for cascading several UAA 180 ICs (up to 7)



Application circuit 3

for field strength indication



Bipolar circuit

The tone control unit is provided for the DC voltage control of volume, treble, and bass. The volume characteristic can be switched over from linear to physiological.

For stereo applications, the TDA 4290 is also available in groups, selected according to synchronization.

- Few external components
- High signal-to-noise ratio
- Low total harmonic distortion

Type	Ordering code	Package outline
TDA 4290	Q 67000-A 1359	DIP 14

Maximum ratings

Supply voltage	V_S	18	V
Load current	I_2	10	mA
Thermal resistance (system-air)	$R_{th\ SA}$	90	K/W
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C

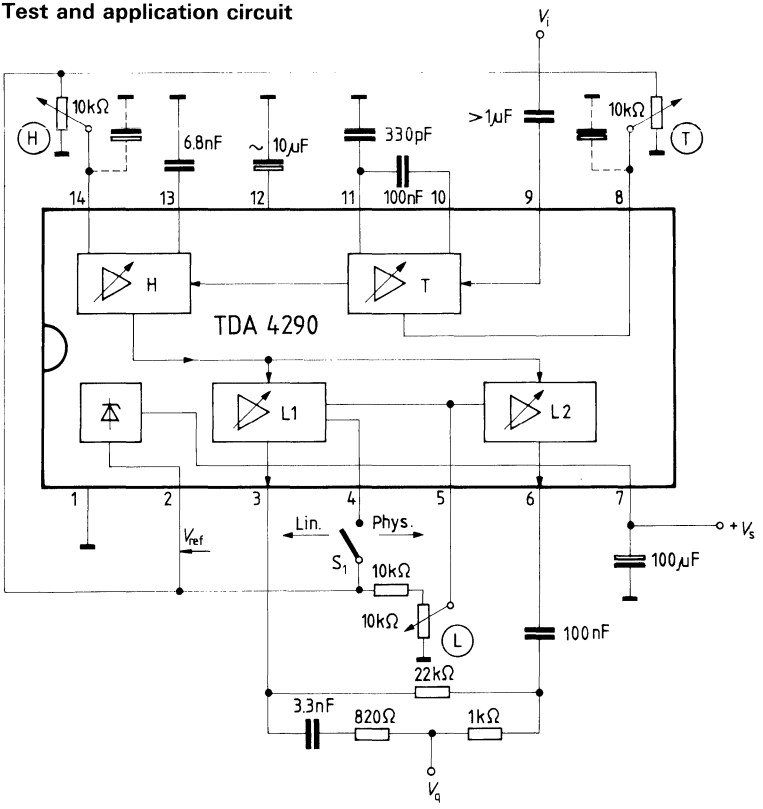
Range of operation

Supply voltage range	V_S	10.5 to 18	V
Frequency range (−1 dB)	f_i	20 to 20.000	Hz
Ambient temperature range	T_{amb}	0 to 70	°C

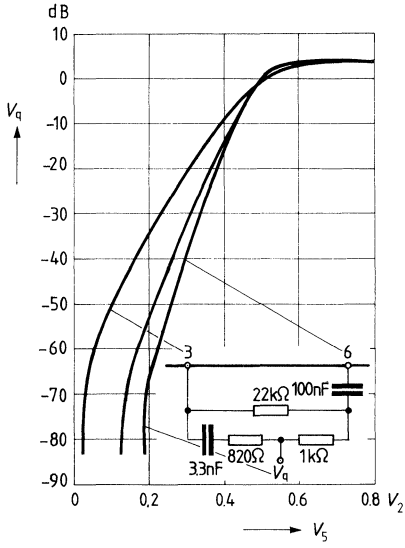
Characteristics (V_S = 14 V; T_{amb} = 25 °C)

		min	typ	max	
Current consumption	I_S		35	50	mA
Reference voltage	V_2	4.5	4.85	5.2	V
Input resistance	$R_{i\,9}$	2.9	3.9		kΩ
Output resistance	$R_{q\,3/6}$		200		Ω
Changeover current	I_4		3.5		mA
Input current for set inputs ($V_{5/8/14} = 0.5 \cdot V_2$)	$-I_{5/8/14}$		4	20	µA
Gain (f_i = 1 kHz; V_i = 300 mV_{rms})					
S_1 lin; V_5 = 0 V	$V_{3.6}/V_9$		−80		dB
S_1 lin; V_5 = 1.0 V	$V_{3.6}/V_9$		−60		dB
S_1 lin; $V_5 = 0.5 \cdot V_2$	$V_{3.6}/V_9$		0		dB
S_1 phys; V_5 = 1.0 V	V_3/V_9		−30		dB
	V_6/V_9		unchanged		
Gain change (f_i = 1 kHz)					
max. bass/treble emphasis	V_q/V_9		+2		dB
max. bass/treble deemphasis	V_q/V_9		−2		dB
Treble emphasis (f_i = 15 kHz; $V_{14} = V_2$)	V_q/V_9	+15	+17		dB
Treble deemphasis (f_i = 15 kHz; V_{14} = 0 V)	V_q/V_9		−17	−15	dB
Bass emphasis (f_i = 40 Hz; $V_8 = V_2$)	V_q/V_9	+15	+17		dB
Bass deemphasis (f_i = 40 Hz; V_8 = 0 V)	V_q/V_9		−17	−15	dB
Frequency range (−1 dB) (all control units in linear position)	f_i	20		20000	Hz
Total harmonic distortion (V_i = 300 mV_{rms}; f_i = 1 kHz; control unit in 0 dB position)	*THD*		0.2	0.7	%
Disturbance voltage (f_i = 20 to 20,000 Hz; tone control unit in 0 dB position, volume −20 dB)	V_d		30	50	μV_{rms}

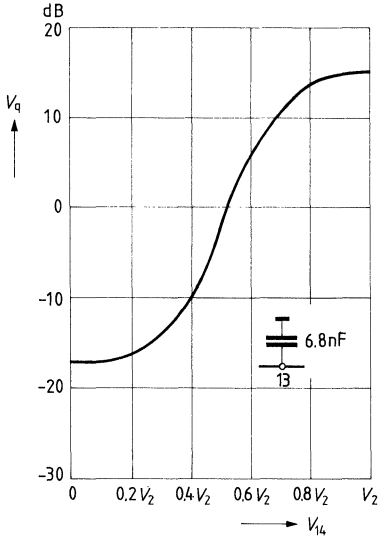
Test and application circuit



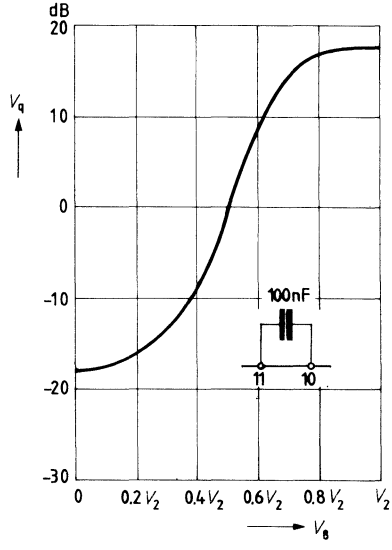
Physiological volume characteristic
(treble and bass control in linear position)
V_i = 300 mV, f_i = 1.6 kHz



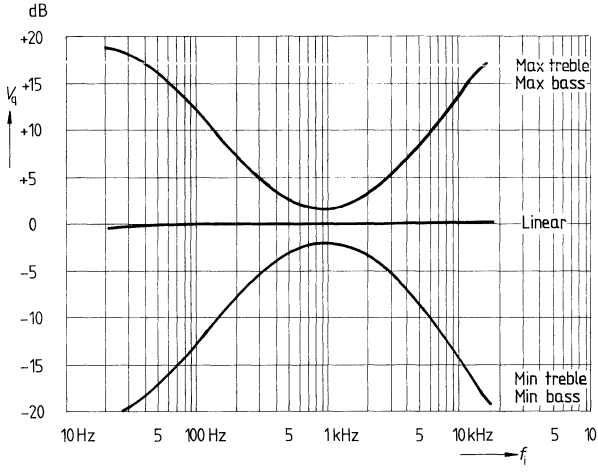
Treble control
S_1 open; V_i = 300 mV_{rms}; volume = 0 dB
V_i = 300 mV, f_i = 20 Hz



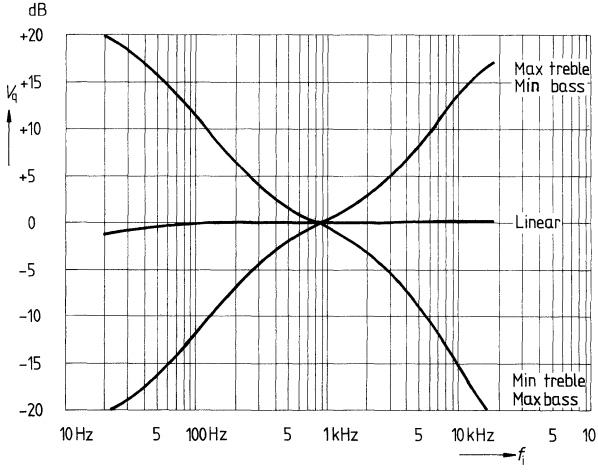
Bass control
S_1 open; V_i = 300 mV_{rms}; volume = 0 dB
V_i = 300 mV, f_i = 20 kHz



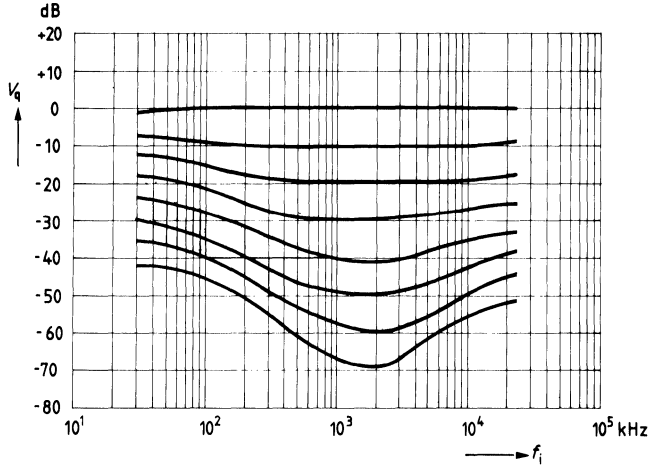
Bass and treble control
V_i = 300 mV ≙ 0 dB; S_1 open



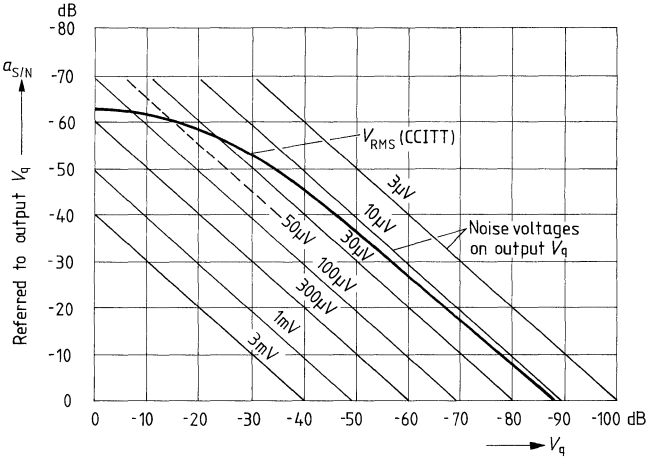
Bass and treble control
V_i = 300 mV ≙ 0 dB; S_1 open



Physiological volume versus input frequency
S_1 closed; V_i = 300 mV_{rms} ≙ 0 dB



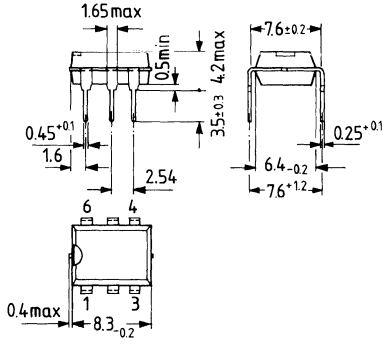
Disturbance voltage spacing
Bandwidth 30 Hz to 20 kHz; V_i = 300 mV_{rms} ≙ 0 dB; f_i = 1 kHz
S_1 open; treble and bass control in linear position



Packaging Information

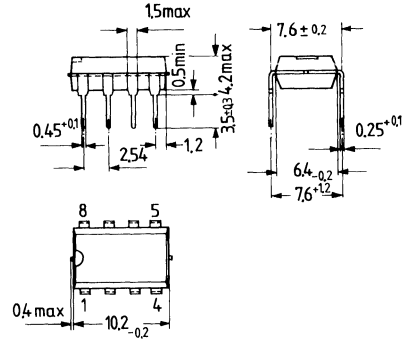
Packaging Information

Plastic plug-in package 20 A 6 DIN 41 866,
6 pins, DIP



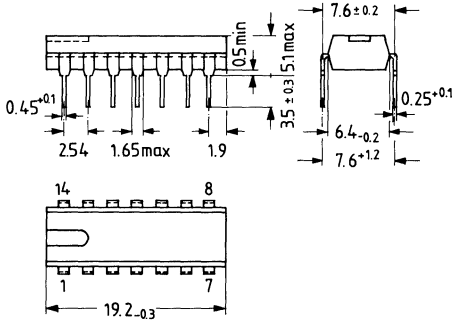
Approx. weight 0.7 g

Plastic plug-in package 20 A 8 DIN 41 866,
8 pins, DIP



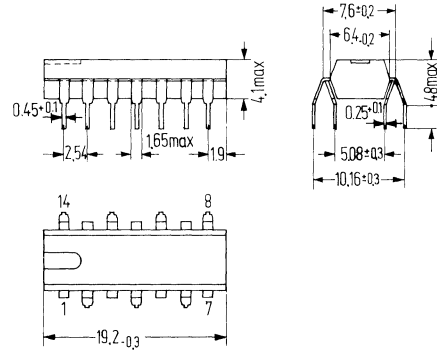
Approx. weight 0.7 g

Plastic plug-in package 20 A 14 DIN 41 866,
14 pins, DIP



Approx. weight 1.1 g

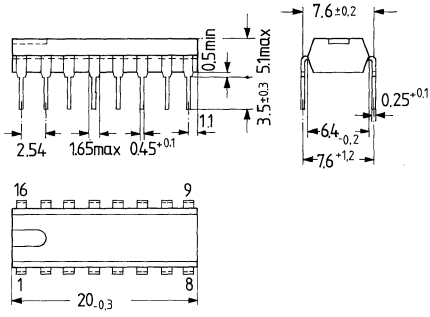
Plastic plug-in package similar to 20 A 14 DIN 41 866,
14 pins, QIP



Approx. weight 1.1 g

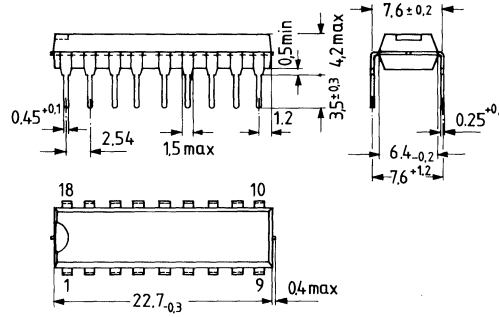
Dimensions in mm

Plastic plug-in package 20 A 16 DIN 41866,
16 pins, DIP



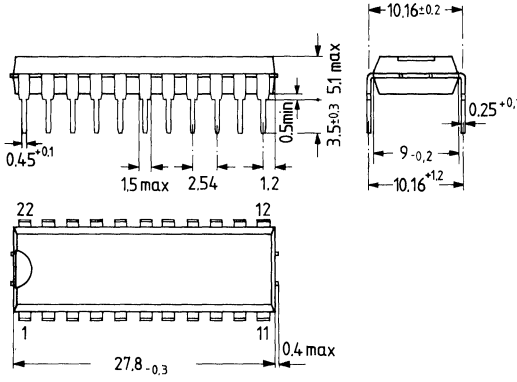
Approx. weight 1.2 g

Plastic plug-in package 20 A 18 DIN 41866,
18 pins, DIP



Approx. weight 1.3 g

Plastic plug-in package 20 D 22 DIN 41866,
22 pins, DIP

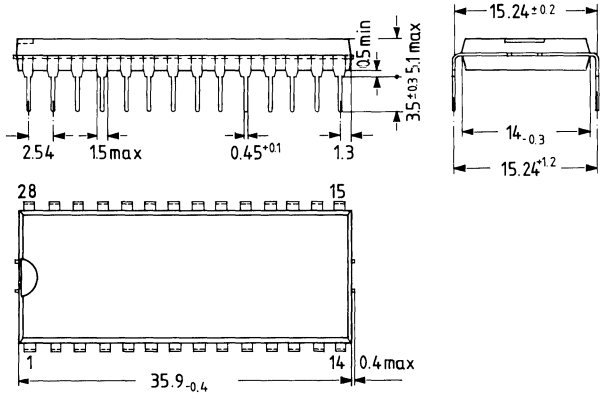


Approx. weight 2.1 g

Dimensions in mm

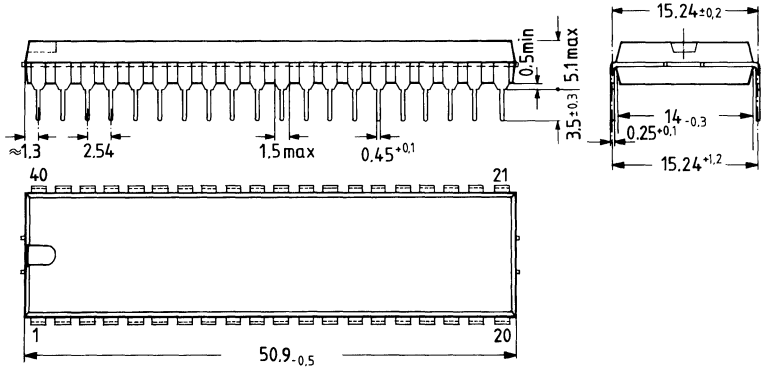
Packaging Information

Plastic plug-in package 20 A 28 DIN 41866,
28 pins, DIP



Approx. weight 3 g

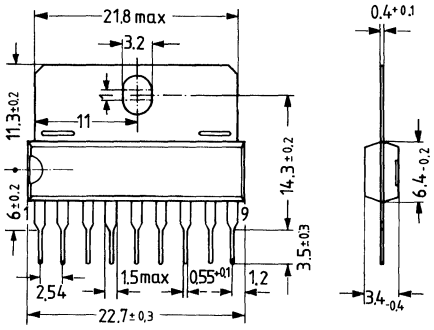
Plastic plug-in package 20 A 40 DIN 41866,
40 pins, DIP



Dimensions in mm

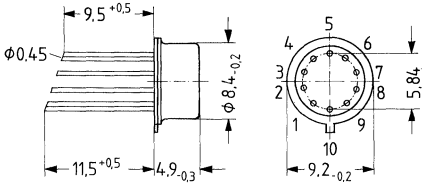
Packaging Information

Plastic power package, SIP 9,
with cooling fin and 9 pins



Approx. weight 1.9 g

Metal case 5 J 10 DIN 41 873 (similar to TO-100)

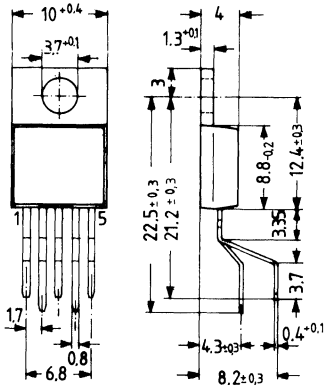


Approx. weight 1.1 g

Dimensions in mm

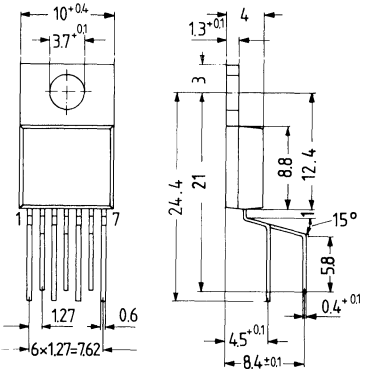
Packaging Information

Plastic power package
TO-220/5 with cooling strip and 5 pins



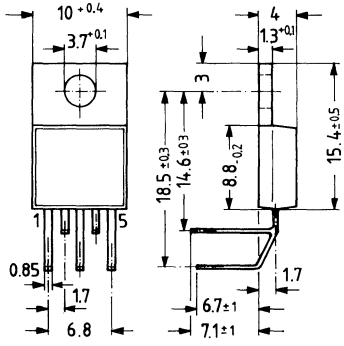
Approx. weight 2.1 g

Plastic power package
TO-220/7 with cooling strip and 7 pins



Approx. weight 2.1 g

Plastic power package
TO-220/5-H with cooling strip and 5 pins



Approx. weight 2.1 g

Dimensions in mm

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