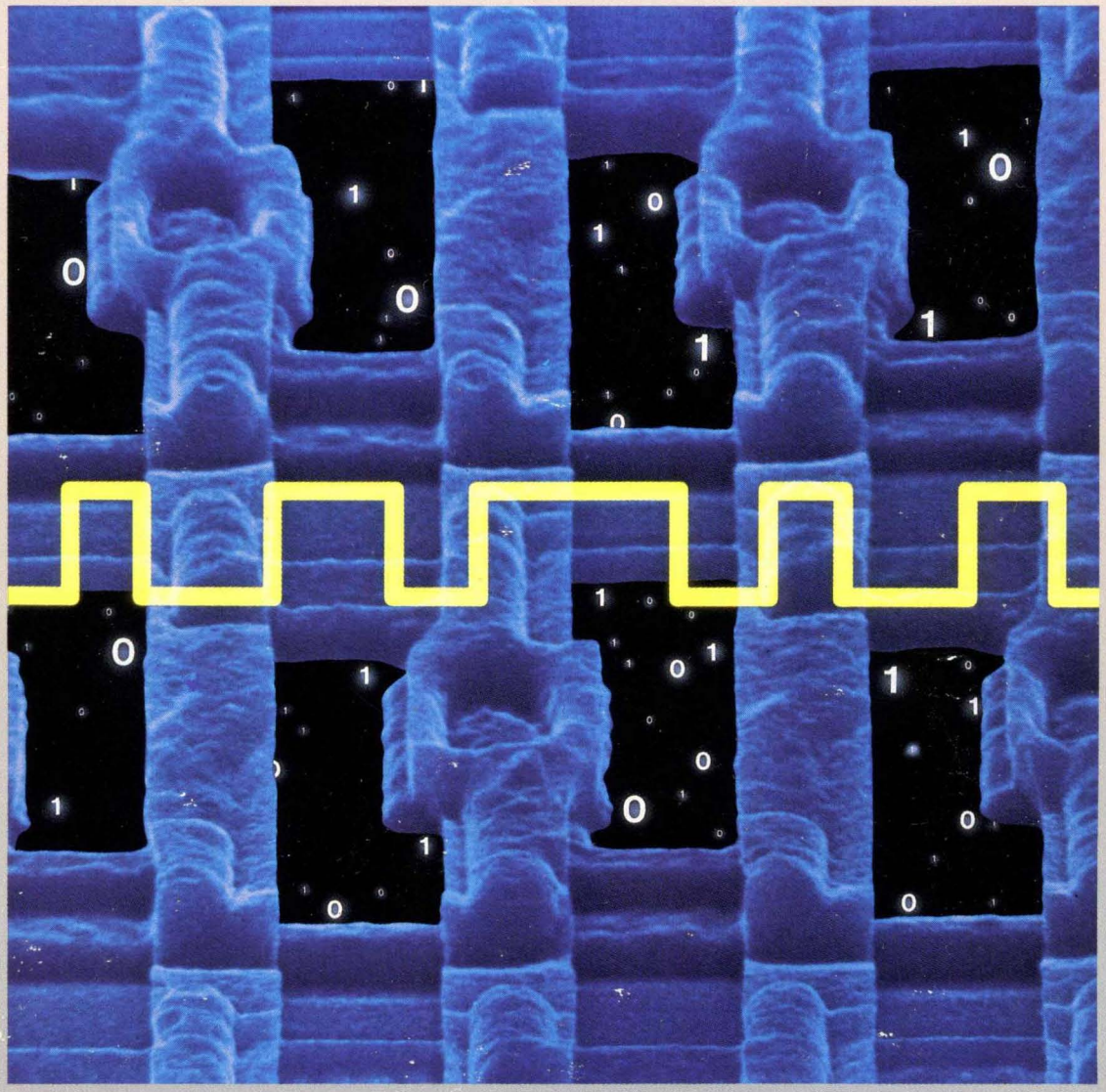
SIEMENS

Linear and Digital Integrated Circuits

Data Book 1988/89



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General Information

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2.1 Type Designation Code for ICs

The IC type designations are based on the European code system of Pro Electron. The code system is explained in the Pro Electron brochure D 15, edition 1982, which can be obtained from:

Pro Electron
Boulevard de Waterloo 103
B-1000 Bruxelles

2.2 Mounting Instructions

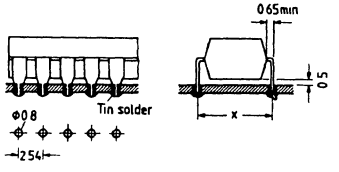
2.2.1 Plastic and Ceramic Plug-In Package

The plug-in packages are soldered to the PCB with the solder joints at the back of the board. The pins are bent down at an angle of 90°. They fit into holes of 0.7 to 0.9 mm diameter, spaced at an equal distance of 2.54 mm. The dimension x is shown in the corresponding package outline drawing.

The bottom of the package does not touch the printed circuit board after insertion, because the pins have shoulders just below the package (see Figure).

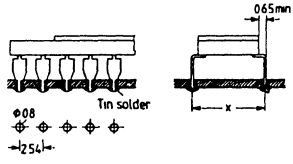
After inserting the package into the printed circuit board, two or more pins should be bent at an angle of approximately 30° relative to the printed circuit board so that the package need not be held down during soldering. The maximum permissible soldering temperature for iron soldering is 265°C (max. 10s) and for dip soldering 240°C (max 4s).

Plastic Plug-In Package



0010-1

Ceramic Plug-In Package



0010-2

Dimensions in mm

2.3 Assembly Instructions for MIKROPACKs

2.3.1 Delivery Package

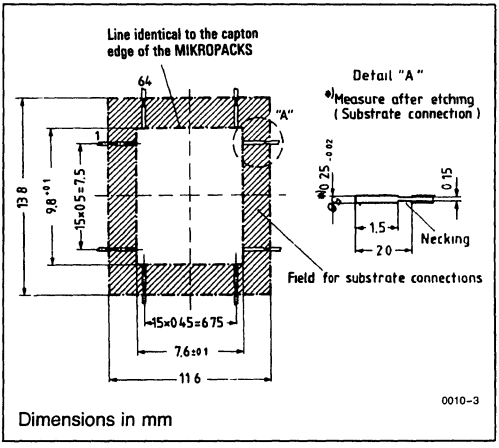
The MIKROPACK PSB 7510 is generally delivered on metal film spools in metal cans. For prototypes, the IC can also be packed individually. MOS handling is necessary.

2.3.2 Substrate Connections

For assembly of the MIKROPACK, the connection points on the substrate must be coated with solder. This can be achieved by:

- Galvanic deposition and melting
- Screen printing and melting
- Dip or wave tinning

Solder tin composition: Sn 60 / Pb 40
Thickness of the layer: approx. 15 µm (after melting)



Dimensions in mm

Note:
Necking of the connection leads is not required in the case of galvanically deposited Sn/Pb and subsequent melting.

2.3.3 Assembly Recommendations

All assembly recommendations are valid for the following substrate materials:

- Epoxy resin
- Hard-paper
- Ceramic (thick-thin-film)
- Flexible materials, as for example polyimide
- Glass

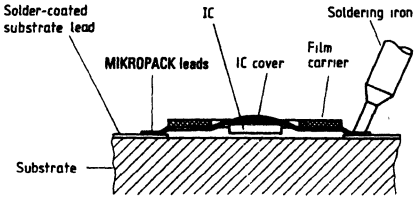
I. Prototypes and Small Quantities

(e.g., up to approx. 1.0/year)

Recommended Processing Method:

Manual Soldering with Mini Soldering Iron

Principle



Required Equipment and Accessories

- Devices for cutting and punching (only when processing from tape)
- Forming tools
- Temperature-regulated miniature soldering iron, certified for the soldering of MOS components
- Stereo microscope (magnification 6...40 x)
- Suction tub or tweezers
- Hair brush
- Sodium-free flux according to DIN 8511 (e.g., pure colophonium dissolved in alcohol)
- Cleaning agents (if required): e.g., Freon T-P 35 and TF
- Bench top suited for the processing of MOS components

Soldering Data

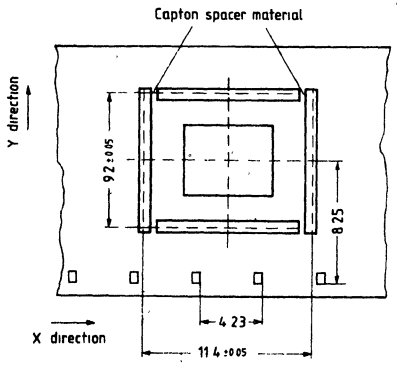
- Soldering temperature at the soldering iron tip: 230°C max.
- Soldering time: approx. 1–2 s

Procedure

Caution! The general rules for the processing of MOS components must be followed during all operations.

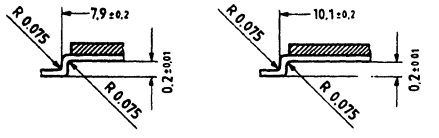
Cut MIKROPACK leads free with hand tool (for components delivered on spools only).

Cutting Dimensions: 9.2 ± 0.05 mm x 11.4 ± 0.05 mm

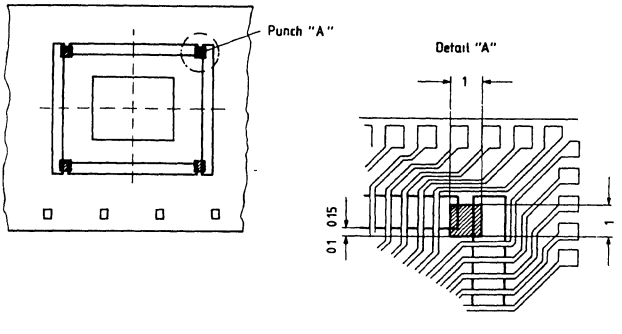


Caution! Only cut free along the dashed lines! Do not cut the 4 capton spacers.
Form MIKROPACK leads with hand tool.
(For the relief of mechanical stress when mounted)

Forming Dimensions



Dimensions in mm



Punch MIKROPACK out of the film tape with hand tool (for components delivered on spools only)

Lay down the punched MIKROPACK onto an electrically conductive surface vacuum pickup.

Coat the mounting points on the substrate with flux (with brush by hand).

Position the MIKROPACK and adjust by hand under stereo microscope (approx. 5 to 10x magnification).

Solder the individual leads by hand with soldering iron under stereo microscope.

Important! First solder two opposite leads. This prevents a shifting of the MIKROPACK during the soldering process.

Cleaning (if required)

Move the substrates one after the other for approx. 1 minute in T-P 35 and TF for example (no ultrasonic cleaning).

Place the cleaning substrates on an electrically conductive surface or in appropriate trays.

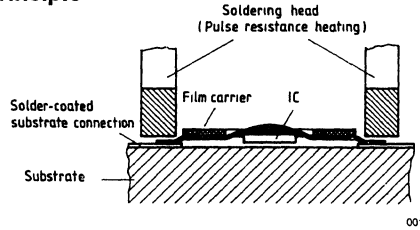
II. Medium Quantities

(e.g., up to approx. 30.0/year)

Recommended Assembling Method:

Pulse Soldering with Manual Device

Principle

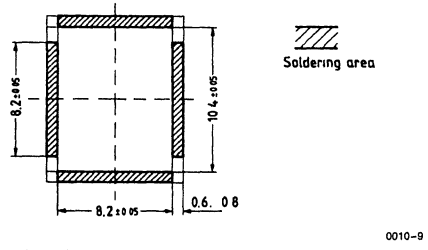


Required Equipment and Accessories

As in I., only instead of the soldering iron:

Pulse Soldering Device

Pulse Soldering Head
(dimensions according to the drawing)



Dimensions in mm

Head holder
Control device (temperature, time)
Substrate holder (with micro-manipulator, if necessary)
Stereo microscope

Soldering Data

Soldering temperature at the pulse soldering head: 230°C max.

Soldering time: approx. 2s plus an additional holding time of 1s until the solder becomes solidified.

Procedure

As described in I. including the positioning of the MIKROPACK onto the substrate and the adjustment.

Further Steps

Position the substrate with the positioned MIKROPACK onto the substrate holder of the pulse soldering device.

Lower, adjust and set down the soldering head onto the MIKROPACK leads manually, then trigger the soldering pulse.

After the Pb/Sn solder becomes solidified (holding time, observation through stereo microscope) raise the soldering head and place the substrate onto an electrically conductive surface or in an appropriate tray.

Caution! Ceramic and glass substrates must be preheated and the stated temperatures must be maintained during the soldering process.

Ceramic: 150°C
Glass: 125°C

Neither preheating nor cooling may be sudden (danger of breakage).

Cleaning (if required): as in I.

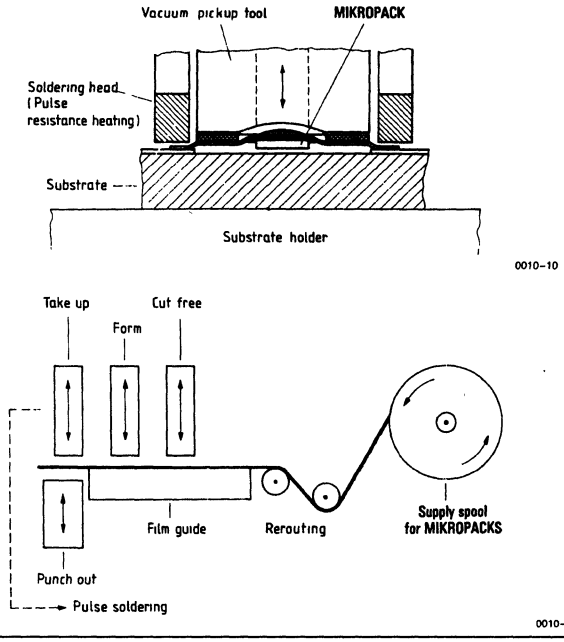
III. Large Quantities

(e.g., approx. 30.0/year)

Recommended Assembling Method:

Semi-Automatic Pulse Soldering

Principle



Required Equipment and Accessories

Semi-automatic pulse soldering device including tools for cutting, forming and punching.

Stero microscope (magnification 6 to 40x).

Flux according to DIN 8511 (e.g., pure colophonium dissolved in alcohol).

Cleaning agents (if necessary): Freon T-P 35 and TF.

Soldering Data

Soldering temperature at the pulse soldering head 230°C max.

Soldering time: approx. 2s plus an additional holding time of 1s until the solder becomes solidified.

Procedure

Position the supply roll in the pulse soldering device.

Coat the mounting positions on the substrate with flux by hand or machine.

Position the substrate onto the substrate holder.

Caution! Ceramic and glass substrates must be preheated and the state temperatures must be maintained during the soldering process.
Ceramic: 150°C
Glass: 125°C

Neither preheating nor cooling may be sudden (danger of breakage).

Machine-cut, form, punch and pre-adjust the MIKROPACK.

Fine-adjust with micro-manipulator (under the stereo microscope or on a monitor).

Pulse-solder by machine.

Place the substrate onto an electrically conductive surface or in an appropriate tray.

Cleaning: (if required): as in I.

IV. Very Large Quantities

(e.g., approx. 500.0/year)

Recommended Assembling Method:

Fully Automatic Pulse Soldering

Processing method as in III. but fully automatic

2.3.4 Final Inspection

It is recommended, that a final visual inspection of the mounted MIKROPACKs be included after soldering, respectively cleaning (under the stereo microscope, magnification 6 to 40x).

Important Criteria

The solder transition between the MIKROPACK leads and the substrate traces should be concave tapered.

The connections to the semiconductor IC must not be damaged.

The solder on all substrate leads must be visibly melted.

MIKROPACK and substrate surface must not show signs of soiling after soldering, respectively cleaning.

2.3.5 Replacment

Experience shows that MIKROPACKs can be replaced as many as five times depending on substrate material and layer construction.

Desolder the MIKROPACK with miniature soldering iron or hot air gun and tweezers. The leads are heated to the melting point of the Pb/Sn solder and bent up with the tweezers.

Plane the mounting spots and recoat with flux.

Solder in a new MIKROPACK using one of the methods described.

2.4 Processing Guidelines for ICs

Integrated circuits (ICs) are electrostatic-sensitive (ESS) devices. The requirement for greater packing density has led to increasingly small structures on semiconductor chips, with the result that today every IC, whether bipolar, MOS, or CMOS, has to be protected against electrostatics.

MOS and CMOS devices generally have integrated protective circuits and it is hardly possible any more for them to be destroyed by purely static electricity. On the other hand, there is acute danger from electrostatic discharges (ESD).

Of the multitude of possible sources of discharge, charged devices should be mentioned in addition to charged persons. With low-resistive discharges it is possible for peak power amounting to kilowatts to be produced.

For the protection of devices the following principles should be observed:

a) Reduction of charging voltage, below 200V if possible.
Means which are effective here are an increase in relative humidity to $\geq$ 60% and the replacement of highly charging plastics by antistatic materials.

b) With every kind of contact with the device pins a charge equalization is to be expected. This should always be highly resistive (ideally R = 10^6 to 10^8 Ω).

All in all this means that ICs call for special handling, because uncontrolled charges, voltages from ungrounded equipment or persons, surge voltage spikes and similar influences can destroy a device. Even if devices have protective circuits (e.g., protective diodes) on their inputs, the following guidelines for their handling should nevertheless be observed.

2.4.1 Identification

The packing of ESS devices is provided with the following label by the manufacturer:

2.4.2 Scope

The guidelines apply to the storage, transport, testing, and processing of all kinds of ICs, equipped and soldered circuit boards that comprise such components.

2.4.3 Handling of Devices

1. ICs must be left in their containers until they are processed.
2. ICs may only be handled at specially equipped work stations. These stations must have work surfaces covered with a conductive material of the order of 10^6 to 10^9 Ω/cm.
3. With humidity of > 50% a coat of pure cotton is sufficient. In the case of chargeable synthetic fibers the clothing should be worn close-fitting. The wrist strap must be worn snugly on the skin and be grounded across a resistor of 50 to 100 kΩ.
4. If conductive floors, R = 5 x 10^4 to 10^7 Ω are provided, further protection can be achieved by using so-called MOS chairs and shoes with a conductive sole (R $\approx$ 10^5 to 10^7 Ω).
5. All transport containers for ESS devices and assembled circuit boards must first be brought to the same potential by being placed on the work surface or touched by the operator before the individual devices may be handled. The potential equalization should be across a resistor of 10^6 to 10^8 Ω.
6. When loading machines and production devices it should be noted that the devices come out of the transport magazine charged and can be damaged if they touch metal, e.g., machine parts.

   Example 1) conductive (black) tubes.

   The devices may be destroyed in the tube by charged persons or come out of the tube charged if this is emptied by a charged person.

   Conductive tubes may only be handled at ESS work stations (high-resistance work-station and person grounding).

   Example 2) anti-static (transparent) tubes.

   The devices cannot be destroyed by charged persons in the tube (there may be a rare exception in the case of custom ICs with unprotected gate pins). The devices can be endangered as in 1) when the tube is emptied if the latter, especially at low humidity, is no longer sufficiently antistatic after a long period of storage (> 1 year).

In both cases damage can be avoided by discharging the devices across a grounded adapter of high-resistance material ($\approx$ 10^6 to 10^8 Ω/cm) between the tube and the machine.

The use of metal tubes—especially of anodized aluminum—is not advisable because of the danger of low-resistance device discharge.

2.4.4 Storage

ESS devices should only be stored in identified locations provided for the purpose. During storage the devices should remain in the packing in which they are supplied. The storage temperature should not exceed 60°C.

2.4.5 Transport

ESS devices in approved packing tubes should only be transported in suitable containers of conductive or longterm anti-static-treated plastic or possibly unvarnished wood. Containers of high-charging plastic or very low-resistance materials are in like manner unsuitable.

Transfer cars and their rollers should exhibit adequate electrical conductivity ($R < 10^6\ \Omega$). Sliding contacts and grounding chains will not reliably eliminate charges.

2.4.6 Incoming Inspection

In incoming inspection the preceding guidelines should be observed. Otherwise any right to refund or replacement if devices fail inspection may be lost.

2.4.7 Material and Mounting

1. The drive belts of machines used for the processing of the devices, in as much as they come into contact with them (e.g., bending and cutting machines, conveyor belts), should be treated with anti-static spray (e.g., anti-static spray 100 from Kontaktchemie). It is better, however, to avoid the contact completely.
2. If ESS devices have to be soldered or desoldered manually, soldering irons with thyristor control may not be used. Siemens EMI-suppression capacitors of the type B 81711-B31. . .-B36 have proven very effective against line transients.
3. Circuit boards fitted and soldered with ESS devices are always to be considered as endangered.

2.4.8 Electrical Tests

1. The devices should be processed with observation of these guidelines. Before assembled and soldered circuit boards are tested, remove any shorting rings.
2. Test receptacles must not be conducting any voltage when individual devices or assembled circuit boards are inserted or withdrawn, unless works specifications state otherwise. Ensure that the test devices do not produce any voltage spikes, either when being turned on and off in normal operation or if the power fuse blows or other fuses respond.
3. Signal voltages may only be applied to the inputs of ICs when or after the supply voltage is turned on. They must be disconnected before or when the supply voltage is turned off.
4. Observe any notes and instructions in the respective data books.

2.4.9 Packing of Assembled PC Boards or Flatpack Units

The packing material should exhibit low volume conductivity:
$10^5\ \Omega/cm < p < 10^{10}\ \Omega/cm$.

In most cases—especially with humidity of > 40%—this requirement is fulfilled by simple corrugated board. Better protection is obtained with bags of conductive polyethylene foam (e.g., RCAS 1200 from Richmond of Redlands, California).

One should always ensure that boards cannot touch.

In special cases it may be necessary to provide protection against strong electric fields, such as can be generated by conveyor belts for example. For this purpose a sheath of aluminum foil is recommended, although direct contact between the film and the PCB must be avoided. Cardboard boxes with an aluminum-foil lining, such as those used for shipping our devices, are available from Laber of Munich.

2.4.10 Ultrasonic Cleaning of ICs

The following recommendation applies to plastic packages. For cavity packages (metal and also ceramic) separate regulations have to be observed.

Freon and isopropyl alcohol (trade name: propanol) can be used as solvents. These solvents can also be used for plastic packages because they do not eat into the plastic material.

An ultrasonic bath in double halfwave operation is advisable because of the low component stress.

The ultrasonic limits are as follows:

sound frequency	$f > 40$ kHz
exposure	$t < 2$ min
alternating sound pressure	$p < 0.29$ bar
sound power	$N < 0.5\ W/cm^2/litre$

ICs for Data Conversion

SIEMENS

Preliminary

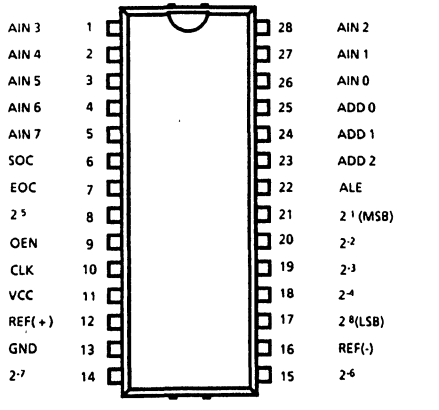
SDA 0808 A, SDA 0808 B, SDA 0808 N
8-Bit CMOS Analog-to-Digital Converters with 8-Channel Multiplexers

- Resolution 8 Bits
- Total Unadjusted Error ±½ LSB
- No Missing Codes
- Fast Conversion Time (15 μs)
- Single Supply 5 V_{DC}
- 8-Channel Multiplexer with Latched Control Logic
- Easy Interface to All Microprocessors, or Stand Alone Operation
- 0V to 5V Analog Input Voltage Range
- No Offset or Gain Adjustments Required
- Latched TRI-STATE Outputs
- Outputs Meet TTL Voltage Level Specifications
- CMOS Low Power Consumption, −15 mW
- 28-Pin P-DIP Standard Package or PLCC
- Extended Temperature Range −40°C to +125°C (SDA 0808B)

3

Pin Configurations

Top View



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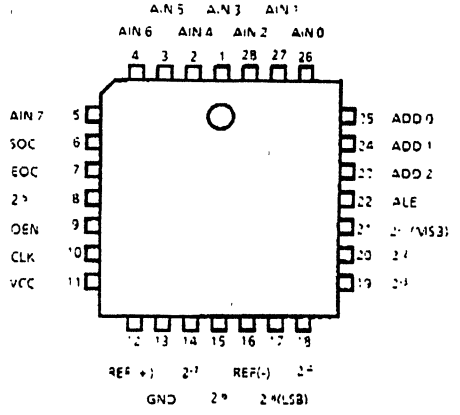
SDA 0808 N



0077-4

The SDA0808 is a monolithic CMOS 8-bit analog to digital converter, with 8-channel analog multiplexer, with a single supply of 5 V_{DC}. The device has a microprocessor compatible control logic and an 8-bit data bus. It is a pin-to-pin compatible device to the data acquisition component ADC 0808/0809.

The SDA0808 uses the method of successive approximation with a capacitor network as conversion technique. The converter features a temperature stabilized differential comparator, 8-channel multiplexer for 8 analog inputs and a sample and hold circuit. The device needs no external offset or gain adjustments. Easy interfacing to microprocessors is provided by 3-bit address latches, 8-bit data-output latches and an 8-bit TRI-STATE® databus.

The temperature range of the SDA 0808A is −40°C to +85°C and for the SDA 0808B −40°C to +125°C.

Pin Definitions

Pin No.	Symbol	Function
1 to 5	AIN3 to AIN7	Analog Inputs
6	SOC	Start of Conversion
7	EOC	End of Conversion
8	2^{-5}	Digital Output Signal
9	OEN	Output Enable
10	CLK	External Clock Input
11	V_{DD}	Pos. Supply Voltage
12	REF(+)	Pos. Reference Voltage
13	GND	Ground
14, 15	$2^{-7}, 2^{-6}$	Digital Output Signals
16	REF(−)	Neg. Reference Voltage
17 to 21	2^{-8} to 2^{-1}	Digital Output Signals
22	ALE	Address Latch Enable
23 to 25	ADD2 to ADD0	Address Inputs
26 to 28	AIN0 to AIN2	Analog Inputs

Technology

Advanced **CMOS** (ACMOS) process.

Functional Description

The Converter

The converter is partitioned into 3 major sections: An approximately 50 pF capacitor network as a sample and hold circuit, the successive approximation register and the comparator. The capacitor network includes a circuit configuration, which provides the first output for a transition when the analog signal has reached + ½ LSB.

The A/D converter's successive approximation register (SAR) is reset on the positive edge of the start of conversion (SOC) pulse. The conversion starts after the falling edge of the start of conversion pulse with the next rising edge of the external clock signal. A conversion in process will be interrupted by a SOC pulse.

The end of conversion output (EOC) will go low after the rising edge of the start of conversion pulse. It is set to logical one with the first rising edge of the external clk after the internal latch pulse. The autozeroed, high resolution, low drift comparator makes the A/D-converter extremely immune to temperature errors.

A/D Converter Timing

After a conversion has been started, the analog voltage at the selected input channel is sampled for 10 external clock cycles which will then be held at the sampled level for the rest of the conversion time. The external analog source must be strong enough to source the current in order to load the sample and hold capacitance, being approximately 50 pF, within those 10 clock cycles.

Conversion of the sampled analog voltage takes place between the 11th and 19th clock cycle after sampling has been completed. In the 19th clock cycle the converted result is moved to the output data latch. With the leading edge of the 20th clock cycle at the end of conversion signal is set.

Multiplexer

The device provides eight multiplexed analog input channels. A particular input channel is selected by programming 3 address lines (AD2, AD1, AD0). Table I shows the input states for the address lines to select a channel. The address is latched on the rising slope of the ALE signal.

Table I

Address Lines			Selected Analog Channel
AD2	AD1	AD0	AIN
L	L	L	AIN 0
L	L	H	AIN 1
L	H	L	AIN 2
L	H	H	AIN 3
H	L	L	AIN 4
H	L	H	AIN 5
H	H	L	AIN 6
H	H	H	AIN 7

Absolute Maximum Ratings*

Supply Voltage[1] (V_{CC}) 6.5V
Input Voltage Range (V_I) ..... −0.3V to V_{CC} + 0.3V
Continuous Total Power Dissipation
(at or below 25°C Free-Air
Temperature Range) ..... 875 mW
Operating Free-Air Temperature Range
SDA 0808A (T_A) ..... −40°C to +85°C
SDA 0808B (T_A) ..... −40°C to +125°C
Storage Temperature
Range (T_{stg}) ..... −65°C to +150°C

Note:
1. All voltage values are with respect to network ground terminal.

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions V_{CC} = 5V; T_A = 25°C

Parameter	Symbol	Conditions	Limits			Units
			Min	Typ	Max	
Supply Voltage	V_{CC}		4.5	5	6	V
Positive Reference Voltage	V_{REF+} [3]			V_{CC}	V_{CC} + 0.1	V
Negative Reference Voltage	V_{REF-}			0	−0.1	V
Differential Reference Voltage	$\Delta V_{REF} = V_{REF+} - V_{REF-}$			5		V
Start Pulse Duration	t_{wiSi}		200			ns
Address Load Control Pulse Width	$t_{w(ALC)}$		200			ns
Address Setup Time	t_{su}		50			ns
Address Hold Time	t_h		50			ns
Clock Frequency	f_{clock}		10	640	1500	kHz

Note:
3. Care must be taken that this rating is observed even during power up.

Electrical Characteristics

over recommended operating free-air temperature range, V_{CC} = 4.75V to 5.25V (unless otherwise noted)

Total Device

Parameter	Symbol	Conditions	Limits			Units
			Min	Typ	Max	
High-Level Input Voltage, Control Inputs	V_{IH}	V_{CC} = 5V	V_{CC} − 1.5			V
Low-Level Input Voltage, Control Inputs	V_{IL}	V_{CC} = 5V			1.5	V
High-Level Output Voltage	V_{OH}	I_O = −360 μA	V_{CC} − 0.4			V
Low-Level Output Voltage						
Data Outputs	V_{OL}	I_O = 1.6 mA			0.45	V
End of Conversion	V_{OL}	I_O = 1.2 mA			0.45	V

Electrical Characteristics over recommended operating free-air temperature range, V_{CC} = 4.75V to 5.25V (unless otherwise noted) (Continued)

Total Device (Continued)

Parameter	Symbol	Conditions	Limits			Units
			Min	Typ	Max	
Off-State (High Impedance-State)	I_{OZ}	V_O = 5V			3	μA
Output Current	I_{OZ}	V_O = 0			−3	μA
Control Input Current at Maximum Input Voltage	I_I	V_I = 5V			1	μA
Low-Level Control Input Current	I_{IL}	V_I = 0V			−1	μA
Supply Current	I_{CC}	f_{clock} = 640 kHz		0.3	3	mA
Input Capacitance, Control Inputs	C_I	T_A = 25°C		10	15	pF
Input Capacitance, Data Outputs	C_O	T_A = 25°C		10	15	pF
Resistance from Pin 12 to Pin 16			1	1000		kΩ

Analog Multiplexer V_{CC} = 5V; T_A = 25°C

Parameter	Symbol	Conditions	Limits			Units
			Min	Typ	Max	
Channel On-State Current[4]	I_{on}	V_I = 5V, f_{clock} = 640 kHz			2	μA
		V_I = 0V, f_{clock} = 640 kHz			−2	μA
Channel Off-State Current	I_{off}	V_{CC} = 5V, T_A = 25°C, V_I = 5V		10	200	nA
		V_{CC} = 5V, T_A = 25°C, V_I = 0V		−10	−200	nA
		V_{CC} = 5V, V_I = 5V			1	μA
		V_{CC} = 0V, V_I = 0V			−1	μA

Note:
4. Channel on-state current is primarily due to the bias current into or out of the threshold detector, and it varies directly with clock frequency.

Operating Characteristics

T_A = 25°C, V_{CC} = V_{REF+} = 5V, V_{REF-} = 0V, f_{clock} = 640 kHz (unless otherwise noted)

Parameter	Symbol	Conditions	SDA 0808A Limits			SDA 0808B Limits			Units
			Min	Typ	Max	Min	Typ	Max	
Supply Voltage Sensitivity	k_{SVS}	V_{CC} = V_{REF+} = 4.75V to 5.25V, T_A = −40°C to +85°C[5]		±0.05			±0.05		%/V
Linearity Error[6]				±0.25			±0.25		LSB
Zero Error[7]				±0.25			±0.25		LSB

Electrical Characteristics over recommended operating free-air temperature range, V_{CC} = 4.75V to 5.25V (unless otherwise noted) (Continued)

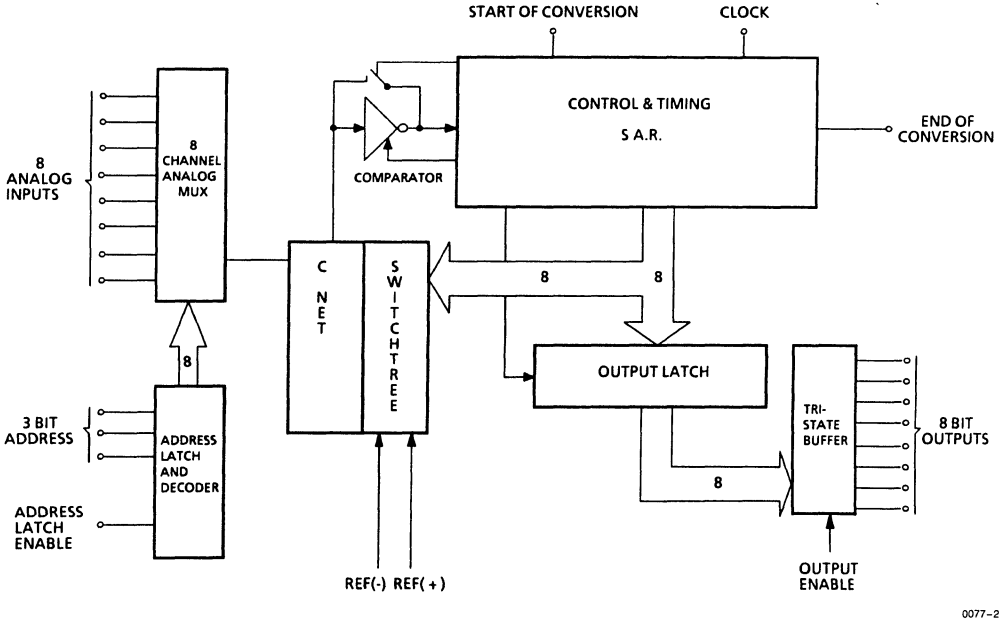
Operating Characteristics (Continued)

T_A = 25°C, V_{CC} = V_{REF+} = 5V, V_{REF-} = 0V, f_{clock} = 640 kHz (unless otherwise noted)

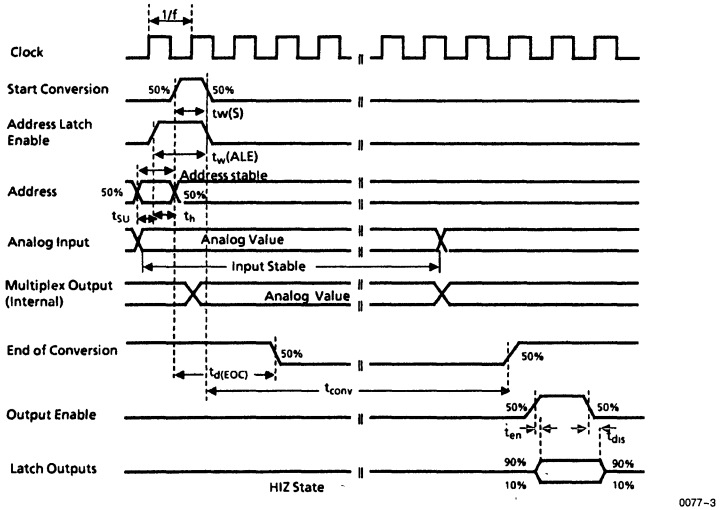
Parameter	Symbol	Conditions	SDA 0808A Limits			SDA 0808B Limits			Units
			Min	Typ	Max	Min	Typ	Max	
Total Adjusted Error(8)		T_A = +25°C		±0.25	±0.5		±0.25	±0.5	LSB
		T_A = −40°C to +85°C			±0.5				LSB
		T_A = −40°C to +125°C						±0.5	LSB
Output Enable Time	t_{en}	C_L = 50 pF, R_L = 10 kΩ		80	250		80	250	ns
Output Disable Time	t_{dis}	C_L = 10 pF, R_L = 10 kΩ		105	250		105	250	ns
Conversion Time	t_{conv}	f_{clock} = 1.5 MHz(10)		15	16		15	16	μs
Delay Time, End of Conversion Output	$t_{d(EOC)}$(9,10)		0		14.5	0		14.5	μs

Notes:
5. Supply voltage sensitivity relates to the ability of an analog to digital converter to maintain accuracy as the supply voltage varies. The supply and V_{REF+} are varied together and the change in accuracy is measured with respect to full-scale.
6. Linearity error is the maximum deviation from a straight line through the end points of the A/D transfer characteristic.
7. Zero error is the difference between the output of an ideal converter and the actual A/D converter for zero input voltage.
8. Total unadjusted error is the maximum sum of linearity error, zero error, and full scale error.
9. For clock frequencies other than 640 kHz, $t_{d(EOC)}$ maximum is 8 clock periods plus 2 μs.
10. Refer to the operating sequence diagram.

Functional Block Diagram



Operation Sequence



Ordering Information

Type	Ordering Code	Package
SDA 0808A	Q67100-A8128	P-DIP28
SDA 0808B	Q67100-A8129	P-DIP28
SDA 0808N	Q67100-A8206	PLCC-28

SIEMENS

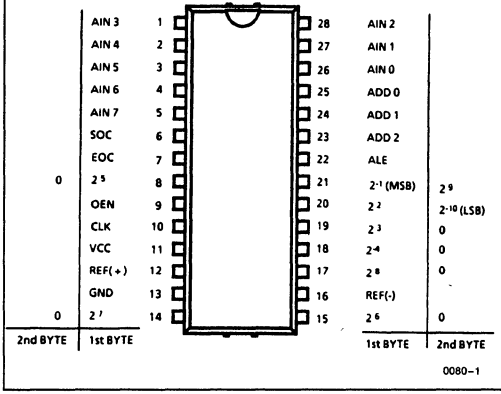
SDA 0810 A, SDA 0810 B, SDA 0810 N
10-Bit CMOS Analog-to-Digital Converters with 8-Channel Multiplexers

- Resolution 10 Bits
- Total Unadjusted Error ±½ LSB
- No Missing Codes
- Fast Conversion Time (15 μs)
- Single Supply 5 V_{DC}
- 8-Channel Multiplexer with Latched Control Logic
- Easy Interface to All Microprocessors, or Stand Alone Operation
- 0V to 5V Analog Input Voltage Range
- No Offset or Gain Adjustments Required
- Latched TRI-STATE Outputs
- Outputs Meet TTL Voltage Level Specifications
- CMOS Low Power Consumption, −15 mW
- 28-Pin P-DIP Standard Package or 28-Pin PLCC
- Extended Temperature Range −40°C to +125°C (SDA 0810 B)

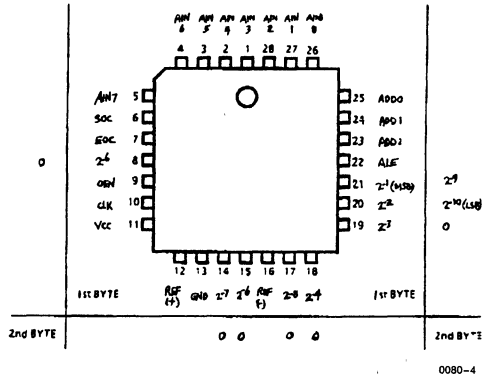
3

Pin Configurations

(Top View)



(Top View)



The SDA 0810 is a monolithic CMOS 10-bit analog to digital converter with 8-channel analog multiplexer, with a single supply of 5 V_{DC}. The device has a microprocessor compatible control logic and an 8-bit data bus. It is a pin-to-pin compatible device to the data acquisition component ADC 0808/0809, with the 10-bit data output in a two-byte format for interface with 8-bit microprocessors.

The SDA 0810 uses the method of successive approximation with a capacitor network as conversion technique. The converter features a temperature stabilized differential comparator, 8-channel multiplexer for 8 analog inputs and a sample and hold circuit. The device needs no external offset or gain adjustments. Easy interfacing to microprocessors is provided by 3-bit address latches, 10-bit data-output latches and a 8-bit TRI-STATE databus. The temperature range of the SDA 0810 A is −40°C to +85°C and for the SDA 0810 B −40°C to +125°C.

Advanced CMOS (ACMOS) process.

Pin Definitions

Pin No.	Function	Symbol 1st Byte	Symbol 2nd Byte
1 to 5	Analog Inputs	AIN3 to AIN7	
6	Start of Conversion	SOC	
7	End of Conversion	EOC	
8	Digital Output Signal	2^{-5}	0
9	Output Enable	OEN	
10	External Clock Input	CLK	
11	Pos. Supply Voltage	V_{DD}	
12	Pos. Reference Voltage	REF(+)	
13	Ground	GND	
14, 15	Digital Output Signals	2^{-7}, 2^{-6}	0
16	Neg. Reference Voltage	REF(−)	
17 to 19	Digital Output Signals	2^{-8} to 2^{-3}	0
20	Digital Output Signal	2^{-2}	2^{-10}
21	Digital Output Signal	2^{-1}	2^{-9} (LSB)
22	Address Latch Enable	ALE	
23 to 25	Address Inputs	ADD2 to ADD0	
26 to 28	Analog Inputs	AIN0 to AIN2	

Functional Description

The Converter

The converter is partitioned into 3 major sections: An approximately 50 pF capacitor network as a sample and hold circuit, the successive approximation register and the comparator. The capacitor network includes a circuit configuration, which provides the first output for a transition when the analog signal has reached + ½ LSB.

The A/D converter's successive approximation register (SAR) is reset on the positive edge of the start of conversion (SOC) pulse. The conversion starts after the falling edge of the start of conversion pulse with the next rising edge of the external clock signal. A conversion process will be interrupted by a SOC pulse.

The end of conversion output (EOC) will go low after the rising edge of the start of conversion pulse. It is set to logical one with the first rising edge of the external clk after the internal latch pulse. The comparator is an autozeroed fully differential comparator for a high power supply rejection ratio.

A/D Converter Timing

After a conversion has been started, the analog voltage at the selected input channel is sampled for 4 external clock cycles which will then be held at the sampled level for the rest of the conversion time. The external analog source must be strong enough to source the current in order to load the sample and hold capacitance, being approximately 50 pF, within those 4 clock cycles.

Conversion of the sampled analog voltage takes place between the 5th and 15th clock cycle after sampling has been completed. In the 15th clock cycle the converted result is moved to the output data latch. With the leading edge of the 16th clock cycle the end of conversion signal is set.

Multiplexer

The device provides eight multiplexed analog input channels. A particular input channel is selected by programming 3 address lines (AD2, AD1, AD0). Table I shows the input states for the address lines to select a channel. The address is latched on the rising slope of the ALE signal.

Table 1

Address Lines			Selected Analog Channel
AD2	AD1	AD0	AIN
L	L	L	AIN 0
L	L	H	AIN 1
L	H	L	AIN 2
L	H	H	AIN 3
H	L	L	AIN 4
H	L	H	AIN 5
H	H	L	AIN 6
H	H	H	AIN 7

Reading the Conversion Results: On the SDA 0810, the data is read as two 8-bit bytes. The converter's digital outputs are positive true. Data is left justified and is presented high byte first. The first OEN high after completing a conversion will enable high byte (2^{-1} to 2^{-8}) on the output buffers, the second OEN pulse will enable the low byte (2^{-9} to 2^{-10}), the unused bits of this byte are fixed to ground. The BYTE CONTROL logic determines which byte is to be read. On each read a flip-flop is toggled so that on successive reads alternative bytes will be output. This flip-flop is always reset to the high byte at the end of a conversion.

Data Bit Locations:

High Byte	2^{-1}	2^{-2}	2^{-3}	2^{-4}	2^{-5}	2^{-6}	2^{-7}	2^{-8}
Low Byte	2^{-9}	2^{-10}	0	0	0	0	0	0

3

Absolute Maximum Ratings*

Supply Voltage(1) (V_{CC}) 6.5V

Input Voltage Range (V_I) ..... −0.3V to V_{CC} + 0.3V

Continuous Total Power Dissipation (at or below 25°C Free-Air Temperature Range) ..... 875 mW

Operating Free-Air Temperature Range
SDA 0810 A (T_A) ..... −40°C to +85°C
SDA 0810 B (T_A) ..... −40°C to +125°C

Storage Temperature Range (T_{stg}) ..... −65°C to +150°C

Note:
1. All voltage values are with respect to network ground terminal.

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions V_{CC} = 5V; T_A = 25°C

Parameter	Symbol	Conditions	Limits			Units
			Min	Typ	Max	
Supply Voltage	V_{CC}		4.5	5	6	V
Positive Reference Voltage	V_{REF+} (3)			V_{CC}	V_{CC} + 0.1	V
Negative Reference Voltage	V_{REF-}			0	−0.1	V
Differential Reference Voltage	$\Delta V_{REF} = V_{REF+} - V_{REF-}$			5		V
Start Pulse Duration	t_{wiSi}		200			ns
Address Load Control Pulse Width	$t_{w(ALC)}$		200			ns
Address Setup Time	t_{su}		50			ns
Address Hold Time	t_h		50			ns
Clock Frequency	f_{clock}		50	640	1000	kHz

Note:
3. Care must be taken that this rating is observed even during power up.

Electrical Characteristics

over recommended operating Free-Air Temperature Range V_{CC} = 4.75V to 5.25V unless otherwise noted

Total Device

Parameter	Symbol	Conditions	Limits			Units
			Min	Typ	Max	
High-Level Input Voltage, Control Inputs	V_{IH}	V_{CC} = 5V	V_{CC} − 1.5			V
Low-Level Input Voltage, Control Inputs	V_{IL}	V_{CC} = 5V			1.5	V
High-Level Output Voltage	V_{OH}	I_O = −360 μA	V_{CC} − 0.4			V
Low-Level Output Voltage Data Outputs End of Conversion	 V_{OL} V_{OL}	 I_O = 1.6 mA I_O = 1.2 mA			 0.45 0.45	 V V
Off-State (High Impedance-State)	I_{OZ}	V_O = 5V			3	μA
Output Current	I_{OZ}	V_O = 0V			−3	μA
Control Input Current at Maximum Input Voltage	I_I	V_I = 5V			1	μA
Low-Level Control Input Current	I_{IL}	V_I = 0V			−1	μA
Supply Current	I_{CC}	f_{clock} = 640 kHz		0.3	3	mA
Input Capacitance, Control Inputs	C_I	T_A = 25°C		10	15	pF
Output Capacitance, Data Outputs	C_O	T_A = 25°C		10	15	pF
Resistance from Pin 12 to Pin 16			1	1000		kΩ

Analog Multiplexer

V_{CC} = 5V; T_A = 25°C

Parameter	Symbol	Conditions	Limits			Units
			Min	Typ	Max	
Channel On-State Current[4]	I_{on}	V_I = 5V, f_{clock} = 640 kHz V_I = 0V, f_{clock} = 640 kHz			2 −2	μA μA
Channel Off-State Current	I_{off}	V_{CC} = 5V, T_A = 25°C, V_I = 5V V_{CC} = 5V, T_A = 25°C, V_I = 0V V_{CC} = 5V, V_I = 5V V_{CC} = 5V, V_I = 0V		10 −10	200 −200 1 −1	nA nA μA μA

Note:

4. Channel on state current is primarily due to the bias current into or out of the threshold detector and it varies directly with clock frequency.

Operating Characteristics

T_A = 25°C, V_{CC} = V_{REF+} = 5V, V_{REF-} = 0V, f_{clock} = 640 kHz, (unless otherwise noted)

Parameter	Symbol	Conditions	Limits						Units
			SDA 0810 A			SDA 0810 B			
			Min	Typ	Max	Min	Typ	Max	
Supply Voltage Sensitivity	k_{SVS}	V_{CC} = V_{REF+} = 4.75V to 5.25V, T_A = −40°C to +85°C(5)		±0.05			±0.05		%/V
Linearity Error(6)					±0.5			±0.5	LSB
Zero Error(7)					±0.5			±0.5	LSB
Total Unadjusted Error(8)		T_A = 25°C T_A = −40°C to +85°C T_A = −40°C to +125°C			±0.5 ±0.5			±0.5 ±0.5	LSB LSB LSB
Output Enable Time	t_{en}	C_L = 50 pF, R_L = 10 kΩ		80	250		80	250	ns
Output Disable Time	t_{dis}	C_L = 10 pF, R_L = 10 kΩ		105	250		105	250	ns
Conversion Time	t_{conv}	f_{clock} = 1.5 MHz(10)		15	16		15	16	µs
Delay Time, End of Conversion Output	$t_{d(EOC)}$	(Notes 9, 10)	0		14.5	0		14.5	µs

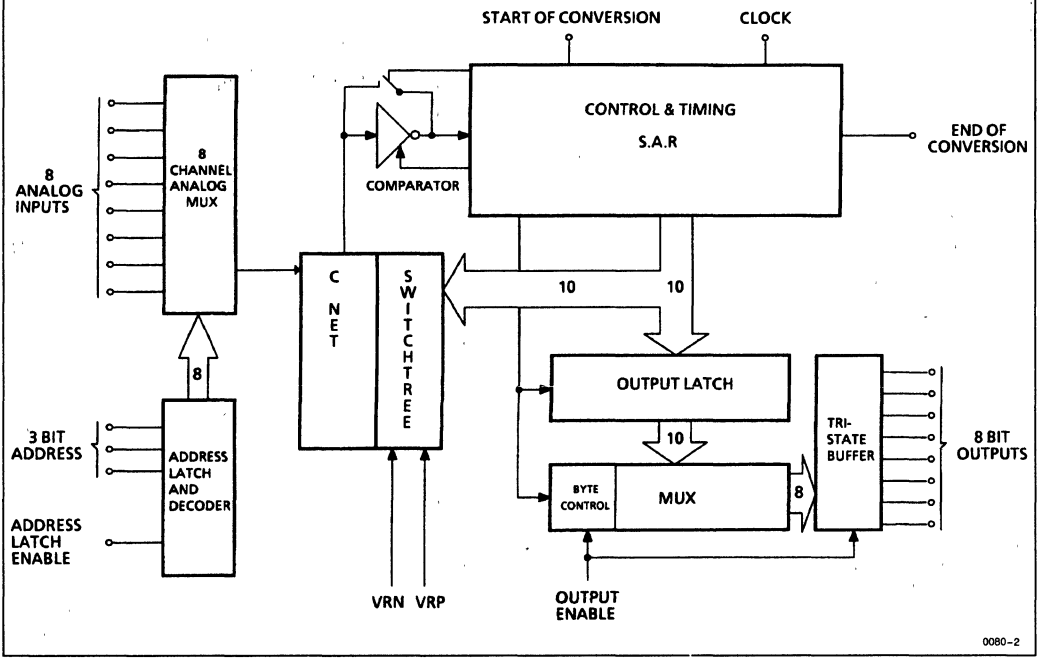
Notes:
5. Supply voltage sensitivity relates to the ability of an analog to digital converter to maintain accuracy as the supply voltage varies. The supply and V_{REF+} are varied together and the change in accuracy is measured with respect to full-scale.
6. Linearity error is the maximum deviation from a straight line through the end points of the A/D transfer characteristic.
7. Zero error is the difference between the output of an ideal converter and the actual A/D converter for zero input voltage.
8. Total unadjusted error is the maximum sum of linearity error, zero error, and full scale error.
9. For clock frequencies other than 640 kHz, $t_{d(EOC)}$ maximum is 8 clock periods plus 2 µs.
10. Refer to the operating sequence diagram.

Ordering Information

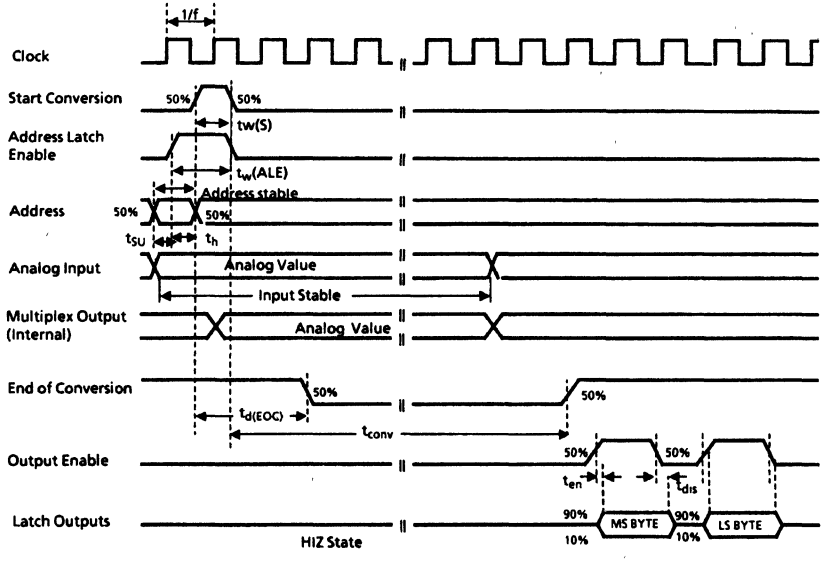
Type	Ordering Code	Package
SDA 0810 A	Q67100-A8130	P-DIP28
SDA 0810 B	Q67100-A8144	P-DIP28
SDA 0810 N	Q67100-A8207	PLCC28

Functional Block Diagram

ADC 10



Operation Sequence



SIEMENS

Advance Information

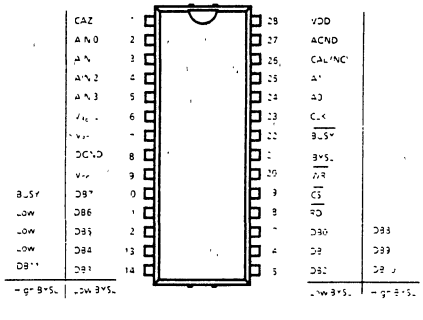
SDA 0812
12-Bit CMOS Analog-to-Digital Converters with 4-Channel Multiplexers

- 12-Bit Monolithic Successive Approximation ADC
- Autocalibration Circuitry
- No Offset or Gain Adjustments Required, Autocalibration
- Total Unadjusted Error ±½ LSB
- No Missing Codes
- Fast Conversion Time (17 µs)
- Single 5V DC Supply
- 4-Channel Multiplexer with Latched Control Logic
- Easy Interface to 8- and 16-Bit Microprocessors
- Data Output in a Two-Byte Format
- 0V to 5V Analog Input Voltage Range
- Digital Inputs and Outputs are TTL Compatible
- CMOS Low Power Consumption
- 28-Pin P-DIP Standard Package
- Temperature Range −40°C to +85°C

3

Pin Configuration

(Top View)



The SDA 0812 is a monolithic CMOS 12-bit analog-to-digital converter with a 4-channel analog multiplexer. It needs only a 5V supply and achieves a conversion time of 17 µs. An autocalibration circuit guarantees a total unadjusted error within ±½ LSB max. Therefore the device needs no external offset or gain adjustments. The converter features a temperature stabilized differential comparator, and a sample and hold circuit. It uses the method of successive approximation based on a capacitor network and a 12-bit data output in a two-byte format. Designed for easy microprocessor interface using standard control signals CS, RD and WR. The 4-channel input multiplexer is controlled via address inputs A9 and A1.

Two converter busy flags are available to facilitate polling of the converter's status. The temperature range of the SDA 0812 is −40°C to +85°C. The SDA 0812 is compatible to AD7582 with few pins having different specifications.

Advanced **CMOS** (ACMOS) process.

Pin Description

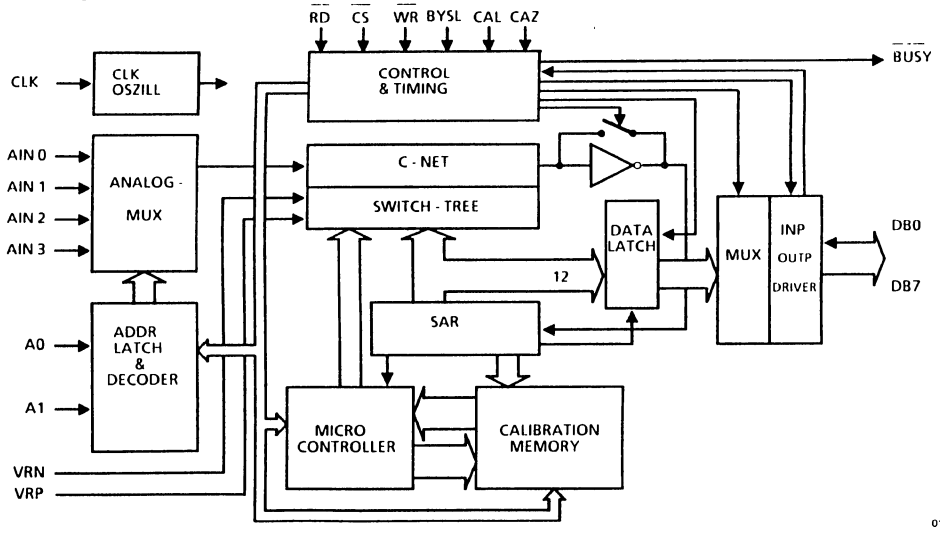
<table>
<tr><th>Pin</th><th>Symbol</th><th>Description</th></tr>
<tr><td>1</td><td>CAZ</td><td>Special function pin (see output modes, and internal clock operation), connect pin to a capacitor (2.2 µF) and the other side of capacitor to AGND, or connect Pin CAZ to AGND.</td></tr>
<tr><td>2–5</td><td>AIN0 to AIN3</td><td>Analog Inputs, channel 0 to channel 3.</td></tr>
<tr><td>6</td><td>V_{REF+}</td><td>Pos. voltage reference input, V_{REF+} = +5V.</td></tr>
<tr><td>7</td><td>V_{REF-}</td><td>Neg. voltage reference input, V_{REF-} = 0V.</td></tr>
<tr><td>8</td><td>DGND</td><td>Digital ground, D_{GND} = 0V.</td></tr>
<tr><td>9</td><td>V_{CC}</td><td>Logic supply voltage, V_{CC} = +5V.</td></tr>
<tr><td>10–17</td><td>DB0 to DB7

Symbol
(BYSL = HIGH)</td><td>Three state data outputs.
DATA BUS OUTPUT ($\overline{CS}$, $\overline{RD}$ = LOW)
Symbol
(BYSL = LOW)</td></tr>
<tr><td>10
11
12
13
14
15
16
17</td><td>BUSY
LOW
LOW
LOW
DB11 (MSB)
DB10
DB9
DB8</td><td>DB7
DB6
DB5
DB4
DB3
DB2
DB1
DB0 (LSB)</td><td>BUSY is an active high converter status flag. It is high during a conversion and during autocalibration.

LOW Pin 11 to Pin 13 are tied to D_{GND} when BYSL = High.

DB11 is the MSB.
DB0 is the LSB.</td></tr>
<tr><td>18</td><td>$\overline{RD}$</td><td>READ INPUT, active low, is used to read the data outputs in combination with $\overline{CS}$ and BYSL.</td></tr>
<tr><td>19</td><td>$\overline{CS}$</td><td>CHIP SELECT INPUT, active low.</td></tr>
<tr><td>20</td><td>$\overline{WR}$</td><td>WRITE INPUT, active low, is used to start a new conversion and to select an analog channel via address inputs A0, A1 in combination with $\overline{CS}$ low. The minimum $\overline{WR}$ pulse width is 100 ns. It is independent of internal/external clock operation.</td></tr>
<tr><td>21</td><td>BYSL</td><td>BYTE SELECT INPUT, is used to select high or low data output byte in combination with $\overline{CS}$ and $\overline{RD}$. See description of Pins 10 to 17.</td></tr>
<tr><td>22</td><td>$\overline{BUSY}$</td><td>Converter Status output. $\overline{BUSY}$ is low during conversion or autocalibration. $\overline{BUSY}$ is high after the converter has finished its operation.</td></tr>
<tr><td>23</td><td>CLK</td><td>CLOCK INPUT for internal/external clock operation. For external clock operation connect PIN 23 to a 74 Hc compatible clock source. For internal clock operation connect PIN 23 to R/C timing components (see clock operation description).</td></tr>
<tr><td>24–25</td><td>A0 to A1</td><td>ADDRESS INPUTS, are used to select one of four analog inputs channels, in combination with $\overline{CS}$ and $\overline{WR}$. The address inputs are latched with the rising edge of $\overline{WR}$.
<table>
<tr><th>A0</th><th>A1</th><th>Selected Channel</th></tr>
<tr><td>Low</td><td>Low</td><td>AIN0</td></tr>
<tr><td>Low</td><td>High</td><td>AIN1</td></tr>
<tr><td>High</td><td>Low</td><td>AIN2</td></tr>
<tr><td>High</td><td>High</td><td>AIN3</td></tr>
</table></td></tr>
<tr><td>26</td><td>CAL (NC)</td><td>CALIBRATION INPUT. An autocalibration cycle is initiated with CAL = high. The CAL input also may remain unconnected like a NC Pin. In this case autocalibration is only initiated by power on. The minimum pulse width of CAL is 100 ns.</td></tr>
<tr><td>27</td><td>AGND</td><td>ANALOG GROUND, AGND = 0V.</td></tr>
<tr><td>28</td><td>V_{DD}</td><td>ANALOG SUPPLY, V_{DD} = +5V.</td></tr>
</table>

Block Diagram



Functional Description

The SDA 0812 is a 4-channel 12-bit CMOS A/D converter. Its successive approximation technique provides 17 μs conversion time. An autocalibration technique guarantees a total unadjusted error within $\pm 1/2$ LSB maximum over the entire temperature range. The major components are shown in the Block Diagram of the converter.

The comparator is a fully differential autozeroed comparator for a high power supply rejection ratio and very low offset voltages. The capacitor network is binary weighted, providing 12-bit resolution. A Sub-C Network is used to correct linearity-errors in the Main-Capacitor Network. The correction terms are calculated by a microcontroller in an autocalibration cycle, started by Power up or an external CAL signal. The correction terms are stored in a calibration memory. The stability of integrated C-Networks guarantees the correction terms to be valid over time and temperature. In the case of a power fail new calibration cycles will be initiated automatically. This guarantees the integrity of the correction terms.

Three state output drivers with multiplexer for two byte data format, an analog multiplexer with address latch and a clock oscillator with external or internal clock operation complete the functional components of the device.

A/D Converter Timing

After a conversion has been started (with the rising edge of $\overline{WR}$) the analog input voltage at the selected input channel is sampled for 5 clock cycles. The external analog source must be capable of sourcing the current to load the 50 pF sample and hold capacitance within those 5 clock cycles. Conversion of the sampled analog voltage takes place between the 6th and 17th clock cycle after sampling has been completed. The CAZ Pin is not used for normal operation, therefore it can directly be connected to AGND or DGND.*

An autocalibration cycle is started with CAL = high, and takes 114 clock cycles. Finally, a normal conversion cycle (17 clock cycles) is added automatically. An external CAL signal is ignored if calibration is already in progress. The external CAL signal is stored if a conversion cycle is in progress, and the calibration starts after finishing this cycle.

During an autocalibration or conversion cycle each power supply voltage and each reference voltage has to be stable. Therefore an internal timer is integrated to provide a waiting period of 58368 clock cycles between power up and autocalibration function. This timer is not activated by external calibration function.

***Note:**
However CAZ serves as an additional programming pin when selecting the output mode or measuring the internal clock frequency.

Internal Clock Operation

The external circuitry for internal clock operation is shown in Figure 1, C_1 may be omitted.

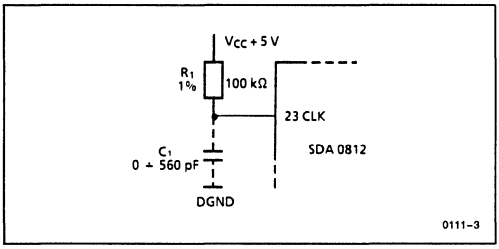


Figure 1

The internal clock frequency only depends on the R_1 value.

$$f_{clock} = \frac{K}{R1} \qquad K = 10^{11}$$

if $R_1 = 100\ k\Omega$ $\quad f_{clock} = 1$ MHz

Note that the specifications are referenced to $f_{clock} = 1$ MHz external.

The actual operating frequency of the internal clock oscillator can vary from device to device by up to 20%. This is due to parameter variations of the CMOS processes. Therefore for precisely defined conversion times usage of an external clock generator is recommended.

The internal clock frequency may be read out on PIN 17 by $\overline{CS}$, $\overline{RD}$ active in combination with CAZ = high and BYSL = high. So it is possible to adjust internal clock frequencies via variations of R_1.

External Clock Operation

The required circuitry for external clock operation is shown in Figure 2.

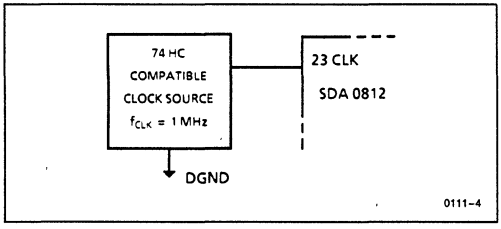


Figure 2

The external clock source has to perform 0.8 V_{max} for low voltage level and 3.0 V_{min} for high voltage level.

The rise and fall times have to be 200 ns maximum.

There is no synchronizing between external clock and any other signal necessary.

Typical Internal Clock Frequency Versus Temperature

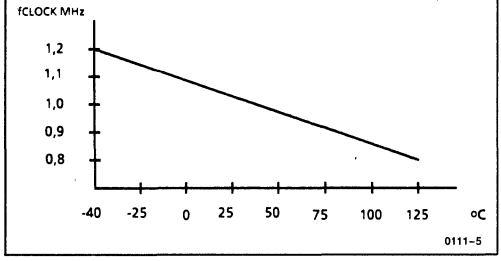


Figure 3

Output Modes

Normal Mode (Transparent)

On the SDA 0812 the data is read as two 8-bit bytes. The converters digital outputs deliver positive true logic signals. Data is presented in right justified format (i.e., the LSB is the most right-hand bit in a 16-bit word). Two READ operations are required, the BYSL input determines which byte is to be read. Because the conversion results are held in a successive approximation register the high byte may be read out before the conversion is finished.

The 4 most significant bits are valid in the 9th clock cycle after starting a conversion. Valid 12-bit data is available for reading after the $\overline{BUSY}$ PIN has gone high, or internal status flag BUSY (available on PIN 10) has gone low.

Latched Output Mode

An additional function in reading the data is available via an integrated data latch, which is transparent in normal function mode.

The latched output may be activated by writing a high on DB0 (into an internal register) with $\overline{WR}$, $\overline{CS}$ active in combination with CAZ and BYSL PIN high.

DB0	$\overline{WR}$	$\overline{CS}$	CAZ	BYSL	Setting Data Latch
High	Low	Low	High	High	Enabled
Low	Low	Low	High	High	Transparent
X	Low	Low	High	Low	Forbidden! Otherwise Unpredictable Behavior

The data latch is set transparent by POWER UP function.

Activating the latch function an internal generated latch enable signal shifts the data from the SAR into a 12-bit latch. This occurs when $\overline{BUSY}$ gets inactive (HIGH). The conversion result is valid during the next conversion cycle until new data is latched. Therefore it may be read out even after starting a new conversion.

Absolute Maximum Ratings*

Supply Voltages[1] (V_{CC}, V_{DD}) 6.5V

Input Voltage Range
All Inputs (V_I) ..... −0.3V to V_{CC} +0.3V

Package Dissipation
(at or below 25°C Free-Air Temperature Range) ..... 875 mW

Operating Free-Air
Temperature Range (T_A) ..... −40°C to +85°C

Storage Temperature Range .... −65°C to +150°C

Note:
1. All voltage values are with respect to network ground terminal.

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3

Specifications

V_{DD} = +5V, V_{REF+} = +5V, V_{REF-} = 0V, DGND = 0V, AGND = 0V, f_{CLK} = 1 MHz external, all specifications T_{min} to T_{max} unless otherwise noted

Parameter	Conditions/Comments	−40°C to +85°C	Units
Accuracy			
Resolution		12	Bits
Total Unadjusted Error[1]	All Channels, AIN0–AIN3	±½	LSB max
Differential Nonlinearity	No Missing Codes Guaranteed	±½	LSB max
Full Scale Error (Gain Error)	All Channels, AIN0–AIN3 Full Scale TC is Typically 5 ppm/°C	±¼	LSB max
Offset Error	All Channels, AIN0–AIN3 Offset Error TC is Typically 5 ppm/°C	±¼	LSB max
Channel to Channel Mismatch		±¼	LSB max
Analog Inputs			
Analog Input Range	V_{REF} = 5.0V	0 to 5	V
C_{AIN}, On Channel Input Capacitance		50	pF Typ
I_{AIN}, Input Leakage Current +25°C T_{min} to T_{max}	AIN0–AIN3; 0V to +5V	 10 100	 nA max nA max
Reference Input			
V_{REF} (for Specified Performance)	±5%	5	V
V_{REF} Range	Degraded Transfer Accuracy	4 to 6	V
V_{REF} Input Reference Current	V_{REF} = 5.0V		mA max

Specifications (Continued)

V_{DD} = +5V, V_{REF+} = +5V, V_{REF-} = 0V, DGND = 0V, AGND = 0V, f_{CLK} = 1 MHz external, all specifications T_{min} to T_{max} unless otherwise noted

Parameter	Conditions/Comments	−40°C to +85°C	Units
Power Supply Rejection			
V_{DD}	V_{DD} = 4.75V to 5.25V	±⅛	LSB Typ
Logic Inputs			
CAZ (Pin 1), $\overline{RD}$ (Pin 18), $\overline{CS}$ (Pin 19), $\overline{WR}$ (Pin 20), BYSL (Pin 21), A0 (Pin 24), A1 (Pin 25)			
V_{IL} Input Low Voltage	V_{CC} = +5V ±5%	0.8	V_{max}
V_{IH} Input High Voltage		2.4	V_{min}
I_{IN} Input Current			
+25°C	V_{IN} = 0 to V_{CC}	±1	μA max
T_{min} to T_{max}		10	μA max
CLK (Pin 23)			
V_{IL}, Input Low Voltage	V_{CC} +5V ±5%	0.8	V_{max}
V_{IH}, Input High Voltage		3.0	V_{min}
V_{IL}, Input Low Current		±10	μA max
I_{IH}, Input High Current		1.5	mA max
Logic Outputs			
DB0–DB7 (Pins 10–17), BUSY (Pin 22)[2]			
V_{OL} Output Low Voltage	V_{CC} = +5V ±5%, I_{SINK} = 1.6 mA[2]	0.4	V_{max}
V_{OH} Output High Voltage	V_{CC} = +5V ±5%, I_{SOURCE} = 200 μA	4.0	V_{min}
Floating State Leakage Current (Pins 10–17)	V_{OUT} = 0V to V_{CC}	15 ±1	μA max
Floating State Output Capacitance		15	pF max
Conversion Time[3]			
with External Clock	f_{CLK} = 1 MHz	17	μs min
with Internal Clock, T_A = 25°C	Using Recommended Clock Components as Shown in Figure 1.	17/20	μs min/max
Power Requirements			
V_{DD}	±5% for Specified Performance	5	VNOM
V_{CC}	±5% for Specified Performance	5	VNOM
I_{DD}	Typically 4 mA with V_{DD} = 5V	7.5	mA max
I_{CC}	V_{IN} = V_{IL} or V_{IH}	100 1.0	μA Typ mA max
Power Dissipation	$\overline{WR}$ = $\overline{RD}$ = $\overline{CS}$ = $\overline{BUSY}$ = Logic HIGH	20	mW Typ

Notes:
1. Includes Full Scale Error, Offset Error and Relative Accuracy.
2. I_{SINK} for $\overline{BUSY}$ (Pin 22) is 1.0 mA.
3. Conversion Time includes autozero cycle time.

SDA 5200 N
6-Bit Analog/Digital Converter

The SDA 5200 N is an ultrafast A/D converter with 6 bit resolution and overflow output. After cascading, it enables straightforward construction of 7 or 8 bit A/D converters, respecitively (refer to application circuit).

Apart from a guaranteed strobe frequency of 100 MHz and an excellent linearity, the SDA 5200 N is outstanding for a broad analog bandwidth which – from the analog side – enables application up to the limit of the Nyquist theorem.

The SDA 5200 N is pin-compatible to the ICs SDA 5010, SDA 6020, and SDA 5200 S (differing output code in the overflow).

Features

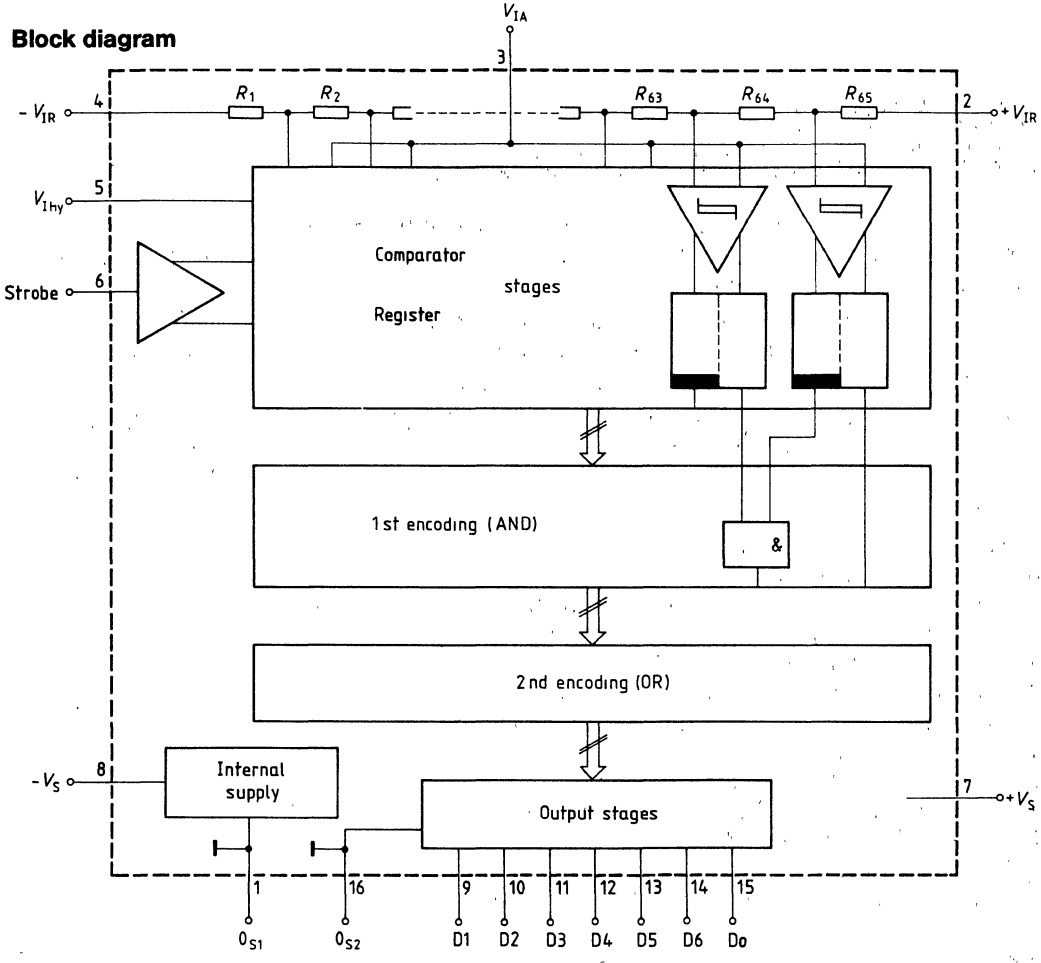
- Strobe frequency 100 MHz
- 6 bit resolution (1.6%)
- Overflow output (7th bit) at simultaneous blocking of the remaining outputs → simple cascading for 7 bit or 8 bit A/D converters
- Broad analog bandwidth (140 MHz)
- High slew rate of the input stages (typ. 0.5 V/ns)
- Processing of analog signals up to the Nyquist limit
- Linearity ± 1/4 LSB
- No sample and hold required
- Dynamic driving of reference inputs for analog addition and multiplication
- Power dissipation 550 mW
- ECL compatible
- Logic-compatible supply voltage +5 V; −5.2 V

The following versions[1] are available upon request:

- IC with a nonlinear conversion characteristic of a given characteristic curve
- IC with any output code (e.g. gray code)

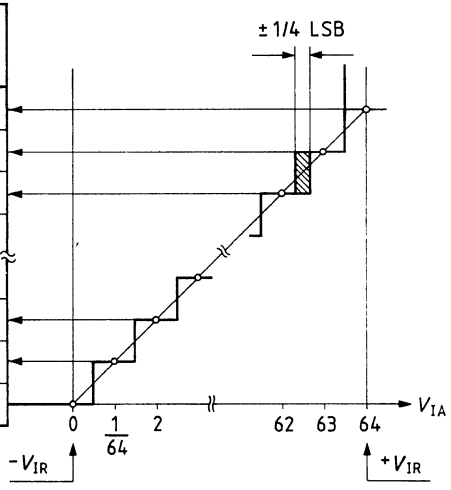
1) Conditions upon request.

Block diagram

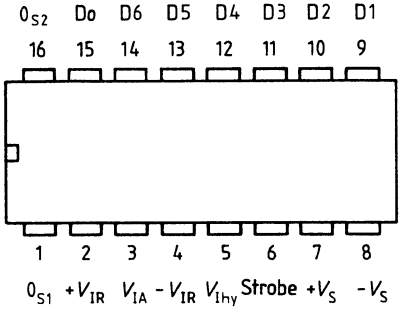


Transfer characteristic and truth table

Do	D6	D5	D4	D3	D2	D1
H	L	L	L	L	L	L
L	H	H	H	H	H	H
L	H	H	H	H	H	L
≈						
L	L	L	L	L	H	L
L	L	L	L	L	L	H
L	L	L	L	L	L	L



Pin configuration
top view



Pin	Symbol	Function
1	0_{S1}	Digital ground 1
2	$+V_{IR}$	Positive reference voltage (+2 V)
3	V_{IA}	Analog signal input (max. +2 V; −3 V)
4	$-V_{IR}$	Negative reference voltage (−3 V)
5	V_{Ihy}	Hysteresis control (9 V to +2.5 V)
6	Strobe	Strobe input (ECL)
7	$+V_S$	Positive supply voltage (+5 V)
8	$-V_S$	Negative supply voltage (−5.2 V)
9 to 14	D1 to D6	Data outputs, bits 1 to 6 (ECL)
15	Do	Overflow output
16	0_{S2}	Digital ground 2

Maximum ratings

		Lower limit B	Upper limit A	
Supply voltage	$+V_S$	−0.3	6.0	V
Supply voltage	$-V_S$	−6.0	0.3	V
Input voltages	$V_{IA}, +V_{IR}, -V_{IR}$	−3.5	2.5	V
Strobe	V_{strobe}	$-V_S$	0	V
Hysteresis control	V_{Ihy}	0	3.0	V
Voltage difference	$0_{S1} - 0_{S2}$	−0.5	0.5	V
Ambient temperature	T_A	0	70	°C
Junction temperature	I_j		125	°C
Storage temperature	T_{stg}	−55	125	°C
Thermal resistance System-air	$R_{th\,SA}$		85	K/W

Characteristics

Power supply

		Lower limit B	typ	Upper limit A	
Pos. supply voltage	$+V_S$	4.5	5.0	5.5	V
Neg. supply voltage	$-V_S$	−5.7	−5.2	−4.7	V
Current consumption					
at $+V_S = +5.0$ V, $V_{IA} \leqq -V_{IR}$	I_{S+}		50	80	mA
at $-V_S = -5.2$ V, $V_{IA} \leqq -V_{IR}$	I_{S-}		55	80	mA

Analog section

Signal input

Max. input voltage	V_{IAmax}	$-V_{IRmin}$		$+V_{IRmax}$	V
$V_{IRmax} = \lvert(+V_{IRmax}) - (-V_{IRmin})\rvert$				5	V
V_{IA} for 6 bit resolution			0.3		V
V_{IA} for 1/2 LSB linearity		1.2	0.6		V
V_{IA} for 1/4 LSB linearity		2.4	1.2		V
Input current					
at $V_{IA} = +V_{IR}$	I_{IA}		150	500	µA
at $V_{IA} < -V_{IR}$	I_{IA}	−500		500	nA
Input capacitance					
at $V_{IA} < -V_{IR}$	C_{IA}		25		pF

Reference inputs

Pos. reference voltage	$+V_{IR}$	−2.5		2	V
Neg. reference voltage	$-V_{IR}$	−3.0		1.5	V
Reference resistance	R_{ref}	96	128	195	Ω

Digital section

Strobe input

H input voltage	V_{IH}	−1.1	−0.9	−0.6	V
L input voltage	V_{IL}	−2.0	−1.7	−1.6	V
H input current	I_{IH}		6	50	µA
L-input current	I_{IL}		6	50	µA

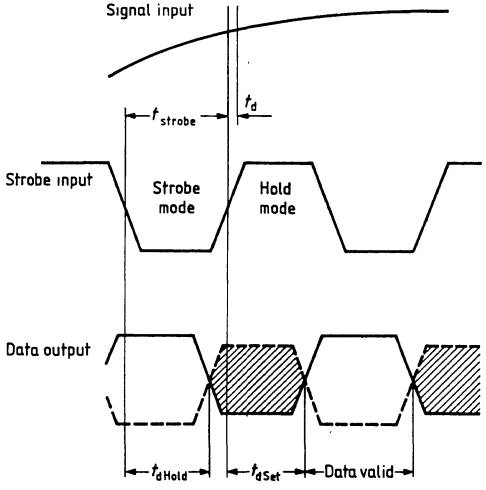
Data outputs (100 Ω to −2 V)

H output voltage	V_{QH}	−1.1	−0.9	−0.7	V
L output voltage	V_{QL}	−2.0	−1.7	−1.5	V

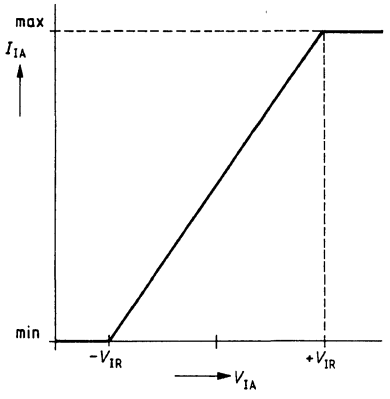
Characteristics (cont'd)

		Lower limit B	typ	Upper limit A	
Dynamic parameters					
Aperture time	t_d		2		ns
Aperture jitter			25		ps
Strobe	t_{strobe}		5		ns
Signal transition time	$t_{d\,Hold}$		12	17	ns
Signal transition time	$t_{d\,Set}$		12	17	ns
Strobe frequency	f_{strobe}	100			MHz
Max. slew rate			0.5		V/ns
bandwidth (−3 dB)	B		140		MHz

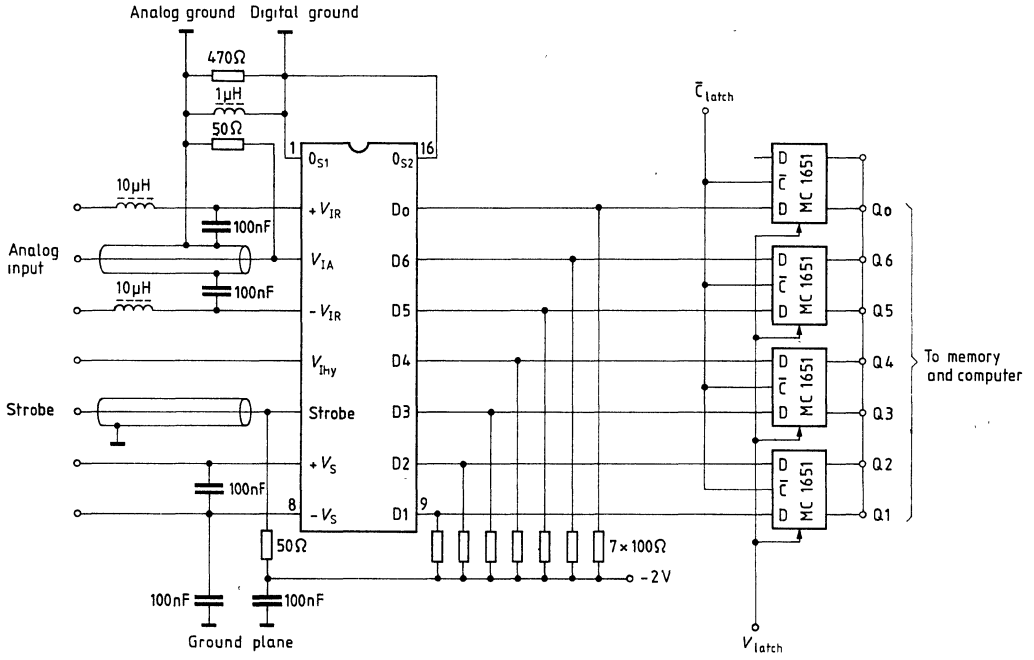
Pulse diagram of strobe input and data outputs



Input current versus input voltage

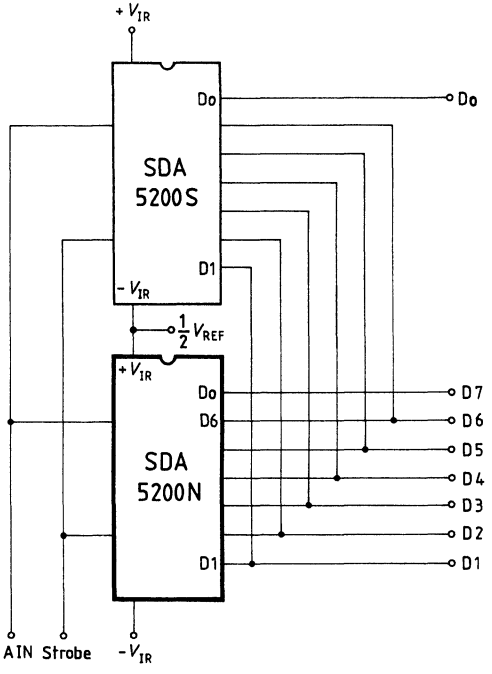


Measurement circuit



Application circuit

7 bit A/D converter with SDA 5200 S and SDA 5200 N



SDA 5200 S
6-Bit Analog/Digital Converter

The SDA 5200 S is an ultrafast 6 bit A/D converter with overflow output. It has been designed as terminating device for a 7 bit or 8 bit A/D converter comprising several cascaded ICs (refer to application circuit), or exclusively for 6 bit operation.

Apart from a guaranteed strobe frequency of 100 MHz and an excellent linearity, the SDA 5200 S is outstanding for a broad analog bandwidth which – from the analog side – enables application up to the limit of the Nyquist theorem.

The SDA 5200 S is pin-compatible to the ICs SDA 5010, SDA 6020, and SDA 5200 N (differing output code in the overflow).

Features

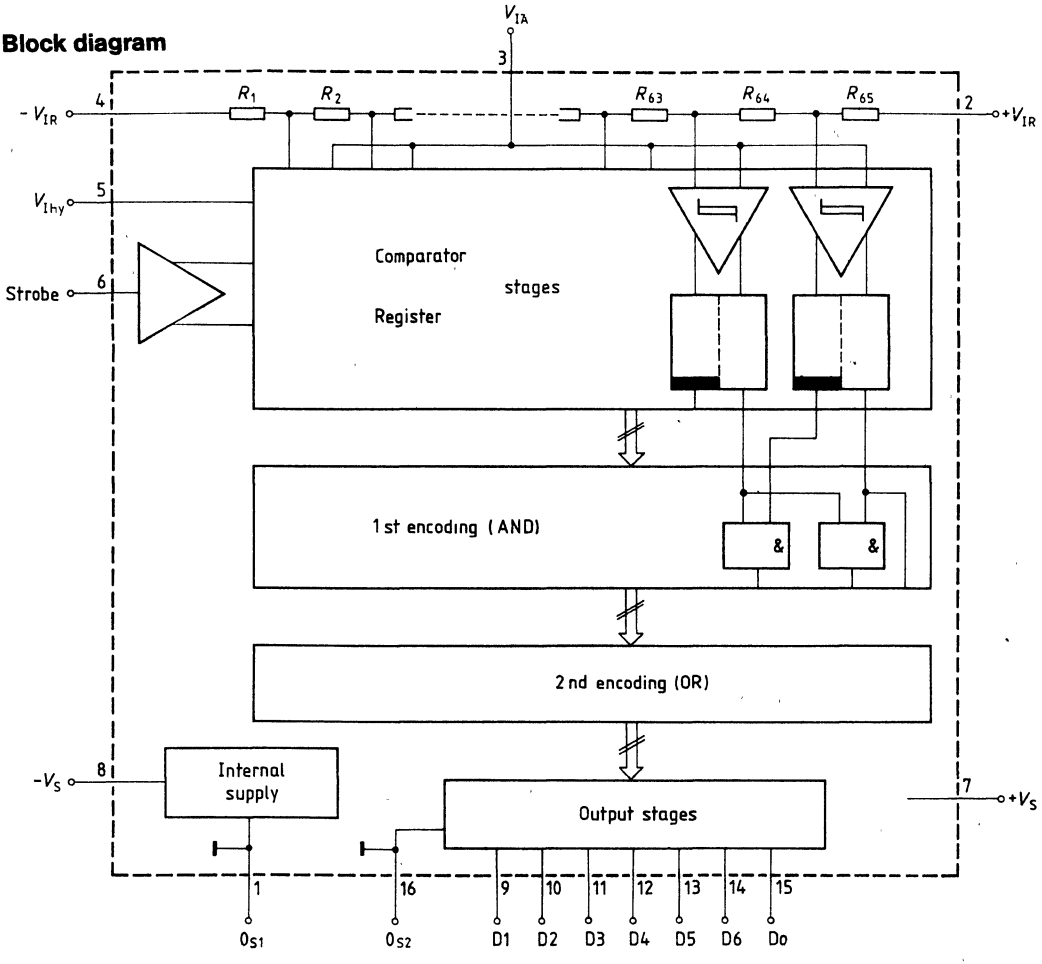
- Strobe frequency 100 MHz
- 6 bit resolution (1.6%)
- Overflow output (7th bit)
- Broad analog bandwidth (140 MHz)
- High slew rate of the input stages (typ. 0.5 V/ns)
- Processing of analog signals up to the Nyquist limit
- Linearity ± 1/4 LSB
- No sample and hold required
- Dynamic driving of reference inputs for analog addition and multiplication
- Power dissipation 550 mW
- ECL compatible
- Logic-compatible supply voltage +5 V; −5.2 V

The following versions[1] are available upon request:

- IC with a nonlinear conversion characteristic of a given characteristic curve
- IC with any output code (e.g. gray code)

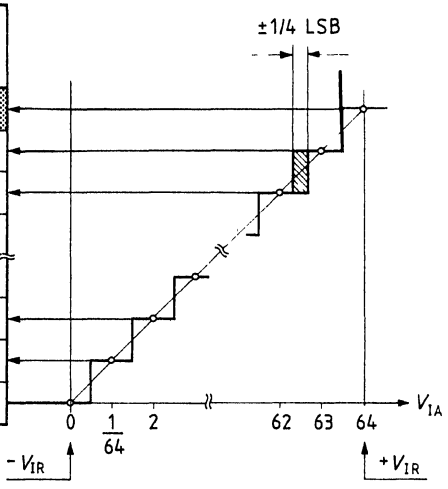
1) Conditions upon request.

Block diagram



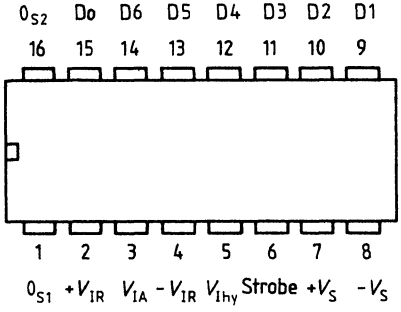
Transfer characteristic and truth table

Do	D6	D5	D4	D3	D2	D1
H	H	H	H	H	H	H
L	H	H	H	H	H	H
L	H	H	H	H	H	L
≈						
L	L	L	L	L	H	L
L	L	L	L	L	L	H
L	L	L	L	L	L	L



Pin configuration

top view



Pin	Symbol	Function
1	0_{S1}	Digital ground 1
2	$+V_{IR}$	Positive reference voltage (+2 V)
3	V_{IA}	Analog signal input (max. +2 V; −3 V)
4	$-V_{IR}$	Negative reference voltage (−3 V)
5	V_{Ihy}	Hysteresis control (9 V to +2.5 V)
6	Strobe	Strobe input (ECL)
7	$+V_S$	Positive supply voltage (+5 V)
8	$-V_S$	Negative supply voltage (−5.2 V)
9 to 14	D1 to D6	Data outputs, bits 1 to 6 (ECL)
15	Do	Overflow output
16	0_{S2}	Digital ground 2

Maximum ratings

		Lower limit B	Upper limit A	
Supply voltage	$+V_S$	−0.3	6.0	V
Supply voltage	$-V_S$	−6.0	0.3	V
Input voltages	$V_{IA}, +V_{IR}, -V_{IR}$	−3.5	2.5	V
Strobe	V_{strobe}	$-V_S$	0	V
Hysteresis control	$V_{I\,hy}$	0	3.0	V
Voltage difference	$0_{S1} - 0_{S2}$	−0.5	0.5	V
Ambient temperature	T_A	0	70	°C
Junction temperature	T_j		125	°C
Storage temperature	T_{stg}	−55	125	°C
Thermal resistance System-air	$R_{th\,SA}$		85	K/W

Characteristics

Power supply

		Lower limit B	typ	Upper limit A	
Pos. supply voltage	$+V_S$	4.5	5.0	5.5	V
Neg. supply voltage	$-V_S$	−5.7	−5.2	−4.7	V
Current consumption					
at $+V_S = +5.0$ V, $V_{IA} \leqq -V_{IR}$	I_{S+}		50	80	mA
at $-V_S = -5.2$ V, $V_{IA} \leqq -V_{IR}$	I_{S-}		55	80	mA

Analog section

Signal input

Max. input voltage	$V_{I\,Amax}$	$-V_{I\,Rmin}$		$+V_{I\,Rmax}$	V
$V_{I\,Rmax} = \lvert(+V_{I\,Rmax}) - (-V_{I\,Rmin})\rvert$				5	V
V_{IA} for 6 bit resolution			0.3		V
V_{IA} for 1/2 LSB linearity		1.2	0.6		V
V_{IA} for 1/4 LSB linearity		2.4	1.2		V
Input current					
at $V_{IA} = +V_{IR}$	I_{IA}		150	500	µA
at $V_{IA} < -V_{IR}$	I_{IA}	−500		500	nA
Input capacitance					
at $V_{IA} < -V_{IR}$	C_{IA}		25		pF

Reference inputs

Pos. reference voltage	$+V_{IR}$	−2.5		2	V
Neg. reference voltage	$-V_{IR}$	−3.0		1.5	V
Reference resistance	R_{ref}	96	128	195	Ω

Digital section

Strobe input

H input voltage	V_{IH}	−1.1	−0.9	−0.6	V
L input voltage	V_{IL}	−2.0	−1.7	−1.6	V
H input current	I_{IH}		6	50	µA
L-input current	I_{IL}		6	50	µA

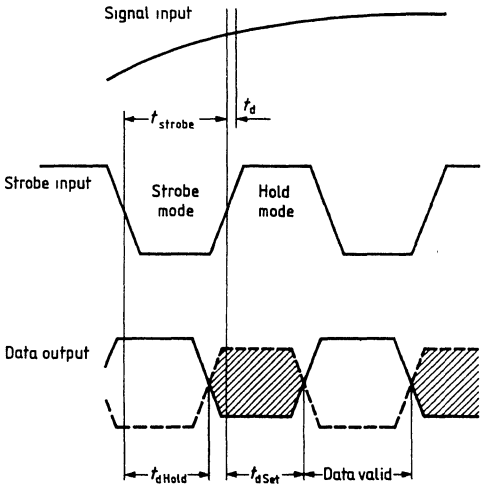
Data outputs (100 Ω to −2 V)

H output voltage	V_{QH}	−1.1	−0.9	−0.7	V
L output voltage	V_{QL}	−2.0	−1.7	−1.5	V

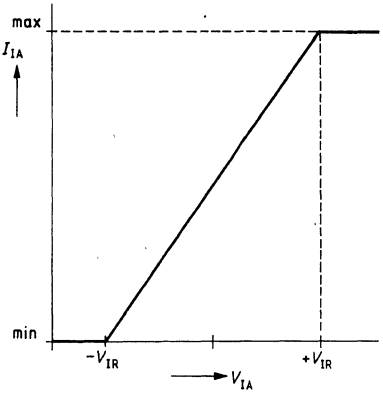
Characteristics (cont'd)

Dynamic parameters		Lower limit B	typ	Upper limit A	
Aperture time	t_d		2		ns
Aperture jitter			25		ps
Strobe	t_{strobe}		5		ns
Signal transition time	$t_{d\,Hold}$		12	17	ns
Signal transition time	$t_{d\,Set}$		12	17	ns
Strobe frequency	f_{strobe}	100			MHz
Max. slew rate			0.5		V/ns
Bandwidth (−3 dB)	B		140		MHz

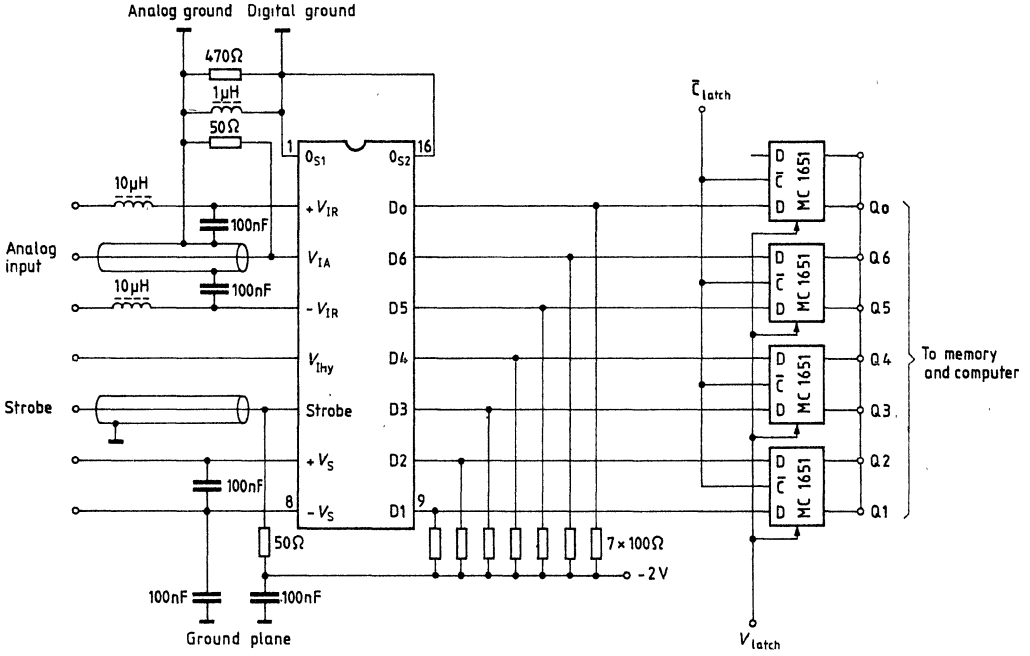
Pulse diagram of strobe input and data outputs



Input current versus input voltage

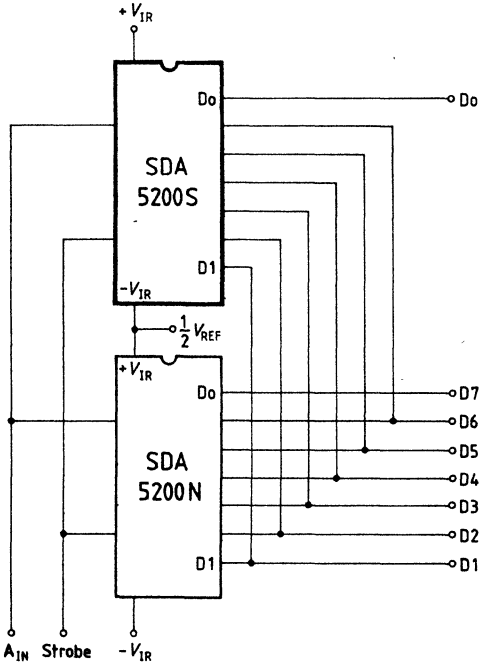


Measurement circuit



Application circuit

7 bit A/D converter with SDA 5200 S and SDA 5200 N



SDA 6020
6-Bit Analog/Digital Converter

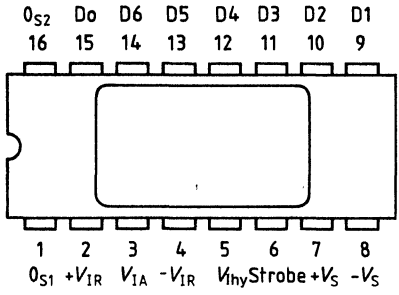
The SDA 6020 is an ultrafast A/D converter with 6 bit resolution. In addition to a scanning frequency of typically 50 MHz and excellent linearity, the SDA 6020 has the following outstanding features:

- 6-bit resolution (1.6%), simple expansion to 8 bits
- ±1/4 LSB linearity
- No sample and hold required
- Dynamic driving of reference inputs for analog addition and multiplication
- ECL compatible (ECL – TTL matching possible, e.g. with SH 100.255)
- Low power dissipation 450 mW
- Logic compatible supply voltage +5 V; –5.2 V

Maximum ratings

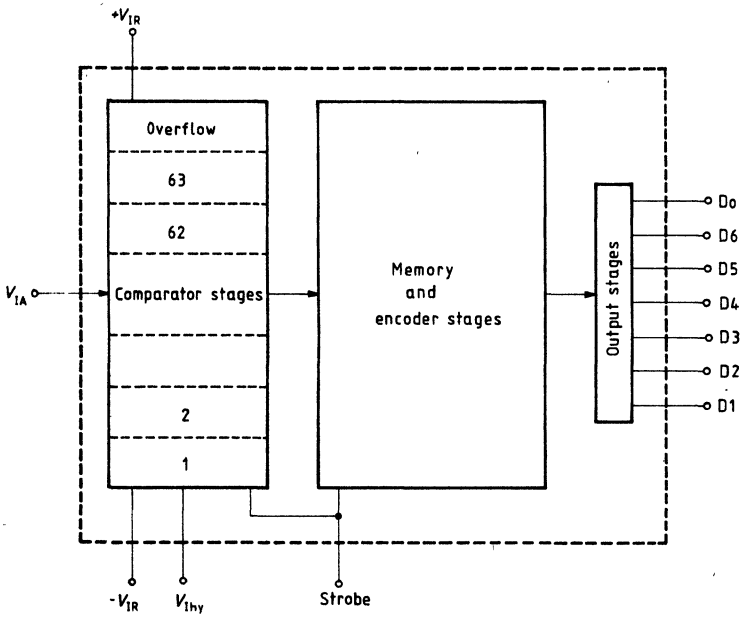
		Lower limit B	Upper limit A	Unit
Supply voltage	$+V_S$	–0.3	6.0	V
Supply voltage	$-V_S$	–6.0	0.3	V
Input voltages	V_{IA}, $+V_{IR}$, $-V_{IR}$	–3.0	3.0	V
Strobe	V_{Strobe}	$-V_S$	0	V
Hysteresis control	V_{IH}	0	3.0	V
Voltage difference	$O_A - O_D$	–0.5	0.5	V
Operating temperature	T_{amb}	0	70	°C
Storage temperature	T_s	–55	125	°C

Pin configuration
top view



Pin	Symbol	Function
1	0_{S1}	Digital ground
2	$+V_{IR}$	Positive reference voltage (<+2.5 V)
3	V_{IA}	Analog signal input (max. ± 2.5 V)
4	$-V_{IR}$	Negative reference voltage (> −2.5 V)
5	V_{Ihy}	Hysteresis control (0 V to +2.5 V)
6	Strobe	Strobe input (ECL)
7	$+V_S$	Positive supply voltage (+5V)
8	$-V_S$	Negative supply voltage (−5.2 V)
9 to 14	D1 to D6	Data outputs, bits 1 to 6 (ECL)
15	Do	Overflow
16	0_{S2}	Digital ground of output stages

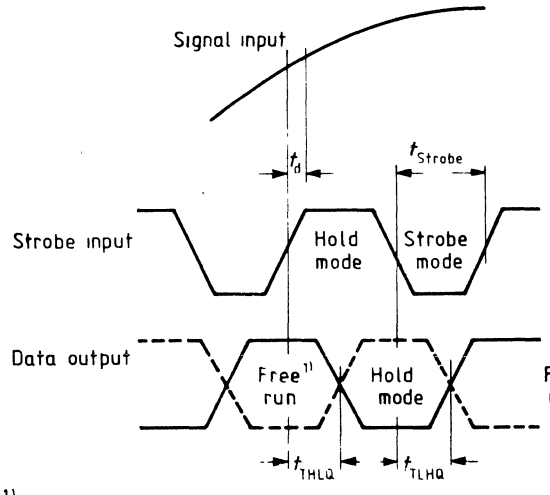
Block diagram



Characteristics		Lower limit B	typ	Upper limit A	
Power supply					
Positive supply voltage	$+V_S$	4.5	5.0	5.5	V
Negative supply voltage	$-V_S$	−5.7	−5.2	−4.7	V
Current consumption					
at $+V_S = +5.0$ V; $V_{IA} \leq -V_{IR}$	I_S		30	60	mA
at $-V_S = -5.2$ V; $V_{IA} \leq -V_{IR}$	I_S		55	80	mA
Analog section					
$T_A = 25$ °C; $+V_S = 5$ V; $-V_S = 5.2$ V					
Signal input					
Maximum input voltage	$V_{IA\,max}$	$-V_{IR\,min}$		$+V_{IR\,max}$	V
$V_{IA\,max} = \lvert (+V_{IR\,max}) - (-V_{IR\,min}) \rvert$				5	V
V_{IA} for 6-bit resolution	V_{IA}		0.3		V
V_{IA} for 1/2 LSB linearity	V_{IA}	1.2	0.6		V
V_{IA} for 1/4 LSB linearity	V_{IA}	2.4	1.2		V
Input current					
at $V_{IA} = +V_{IR}$ in sample mode	I_{IA}		200	800	µA
at $V_{IA} < -V_{IR}$ in sample mode	I_{IA}	−10		10	µA
$-V_{IR} < V_{IA} < +V_{IR}$ in hold mode	I_{IA}	−10		10	µA
Input capacitance					
at $V_{IA} < -V_{IR}$	C_{IA}			35	pF
Reference inputs					
Positive reference voltage	$+V_{IR}$	−2		2.5	V
Negative reference voltage	$-V_{IR}$	−2.5		2	V
Reference resistance	$64\,R$	96	128	256	Ω
Digital section					
Strobe input					
H input voltage	V_{IH}	−1.1	−0.9	−0.6	V
L input voltage	V_{IL}	−2.0	−1.7	−1.5	V
H input current	I_{IH}	5	30	100	µA
L input current	I_{IL}	5	30	100	µA
Data outputs (100 Ω to −2 V)					
H output voltage	V_{QH}	−1.1	−0.9	−0.6	V
L output voltage	V_{QL}	−2.0	−1.7	−1.5	V

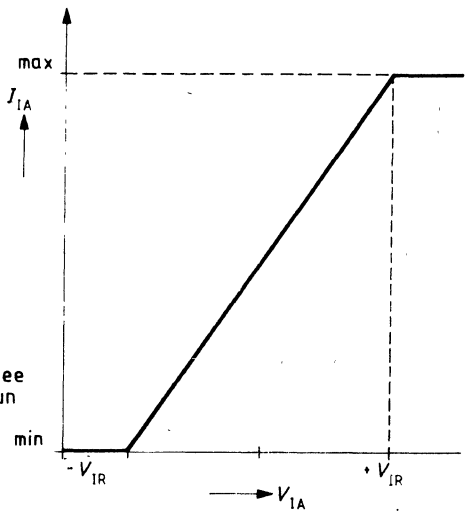
3

Pulse diagram of strobe inputs and data output

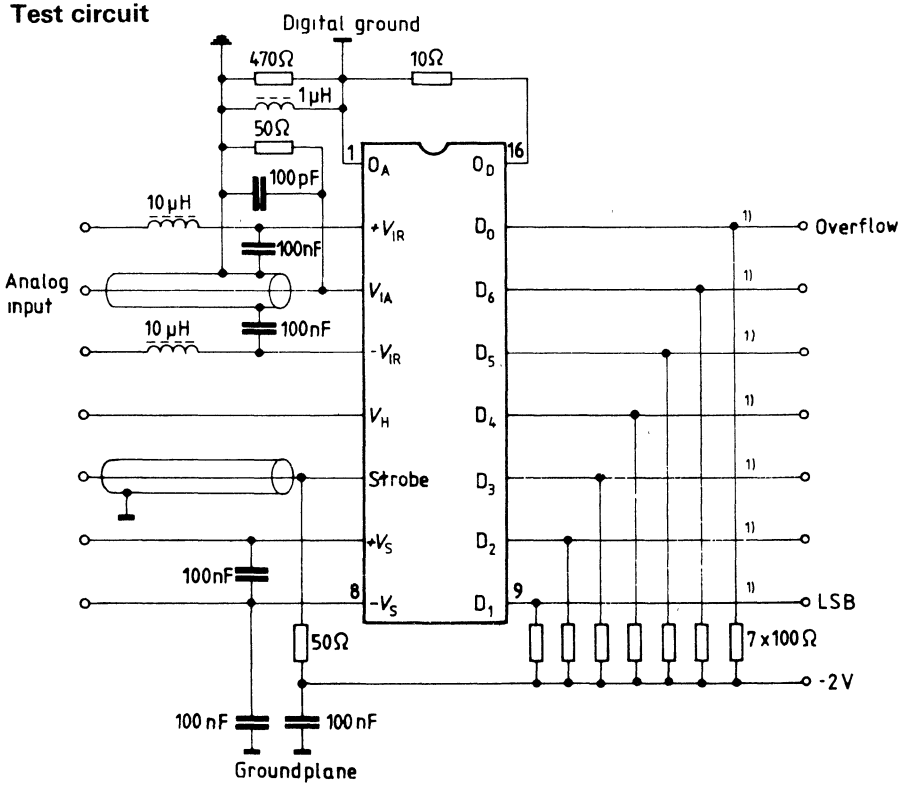


1) undefined output levels

Input current versus input voltage

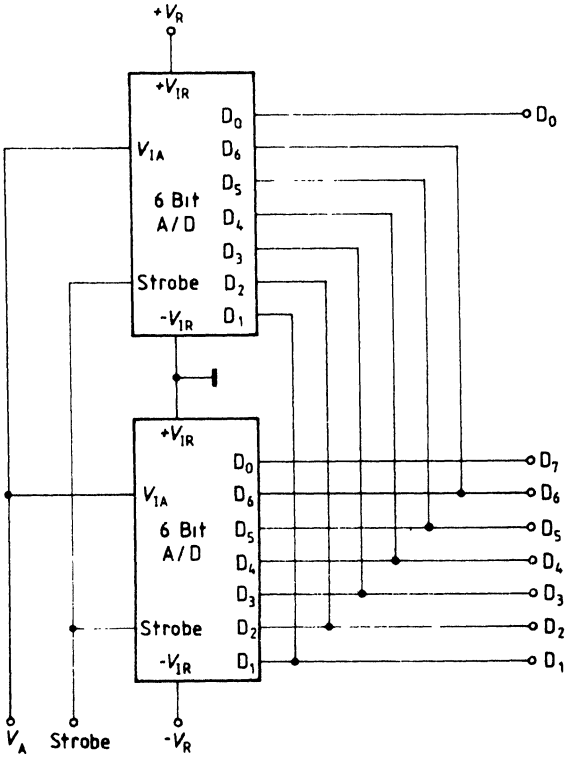


Test circuit

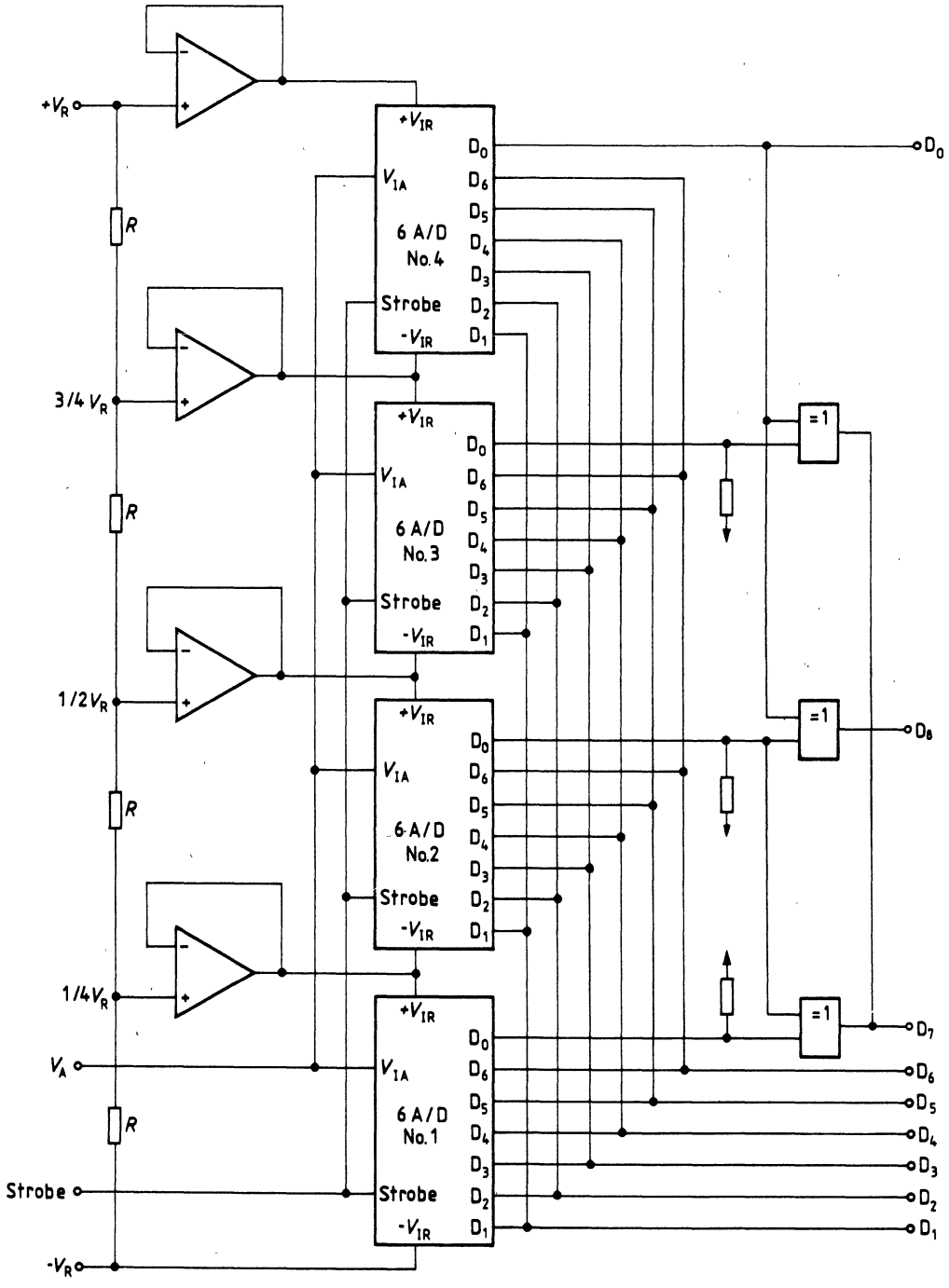


1) Lines effected as Microstrip

Circuit example for expansion to 7 bit



Circuit example for expansion to 8 bit



SIEMENS

SDA 8005
8-Bit/7 ns Digital/Analog Converter

The SDA 8005 is a high-speed D/A converter with splendid dynamic qualities and offers the following features:

- Settling time typ. 7 ns
- Extremely small glitch area
- Digital input register
- Data inputs 10 K and 100 K ECL-compatible
- Single power supply −5.2 V
- Deglitch control input

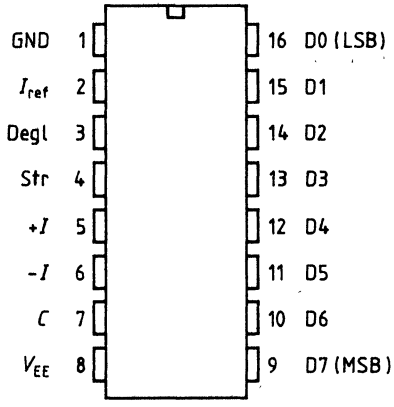
Functional description

The SDA 8005 is a high-speed 8-bit D/A converter with ECL-compatible data and strobe inputs.

The data word is received in the input buffer with the Low active strobe. An external reference voltage source with a reference resistor is needed. At a reference current of 2.5 mA the full-scale output current amounts to 40 mA.

The output glitches can be minimized by adjusting the deglitch input voltage between −2.3 V and −2.9 V. The deglitch input can also be left unwired.

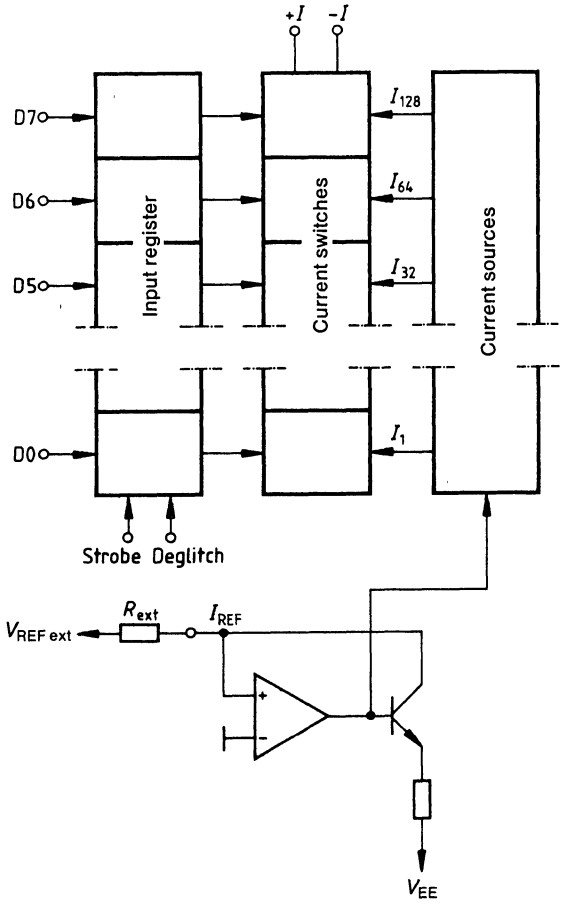
Pin configuration
(top view)



Pin description

Pin	Symbol	Function
1	GND	Ground
2	I_{ref}	Reference current input
3	Degl	Deglitch input
4	Str	Strobe
5, 6	$+I, -I$	Complementary current outputs $+I$: zero current if D0 to D7 are High
7	C	Stabilization
8	V_{EE}	Supply voltage −5.2 V
16 to 9	D0 to D7	Data input 0 (LSB) to 7 (MSB)

Block diagram



Maximum ratings

		Lower limit B	Upper limit A	
Supply voltage	V_{EE}	−6.0	0.3	V
Input voltage	$V_{D0..D7}$	−3.0	0	V
Strobe input voltage	V_{Str}	−4.0	0	V
Deglitch input voltage	V_{Degl}	−5.2	0	V
Output voltages, $+I$, $-I$	V_{QI+}, V_{QI-}	−1.9	5	V
Junction temperature	T_j		125	°C
Ambient temperature	T_A	−25	85	°C
Storage temperature	T_{stg}	−55	125	°C
Thermal resistance	$R_{th\,JA}$		85	K/W

Characteristics

Analog outputs

Static performance

		Lower limit B	typ	Upper limit A	
Ratio of full-scale output current to reference current	I_{QFS}/I_{ref}		16		
Absolute unadjusted error	ERR	−1		+1[2]	%
Integral nonlinearity	*I NL*		0.40[1]	0.55[2]	LSB
Differential nonlinearity	*D NL*		0.6[1]	1[2]	LSB
Full-scale temperature coefficient					
−25 °C to +25 °C	*TC*	80		120	ppm/°C
+25 °C to +85 °C	*TC*	50		80	ppm/°C
Zero-code output current	I_{Q0}		6[1]	30[3]	µA
Full-scale output current	I_{QFS}			40[2]	mA
Output voltage range	V_Q	−1.4		+5	V
Supply voltage sensitivity	S_{VS}		0.03[1]	0.04[2]	%/%

Dynamic performance[1]

Output rise time	t_{rQ}		1.3		ns
Output settling time	t_{sQ}		7		ns
Adjusted worst case glitch area			80		pVs
Digital crosstalk attenuation					
Data	α_{Data}		15[4]		pVs
Strobe	α_{Strobe}		30[4]		pVs

Characteristics			Lower limit B	typ	Upper limit A	
Digital inputs						
DC characteristics						
H input voltage		V_{IH}	−1.105		−0.810	V
L input voltage		V_{IL}	−1.850		−1.505	V
Input capacitance	D7	$C_{I\,D7}$		1.2		pF
	D6	$C_{I\,D6}$		0.8		pF
	D0 to D5	$C_{I\,D0...D5}$		0.5		pF
	Strobe	$C_{I\,Str}$		1.5		pF
H input current	D7	$I_{IH\,D7}$		25		µA
	D6	$I_{IH\,D6}$		12		µA
	D0 to D5	$I_{IH\,D0...D5}$		6		µA
	Strobe	$I_{IH\,Str}$		75		µA
Input coding				binary		
Switching characteristics						
Setup time		t_{setup}	0.5			ns
Hold time		t_{Hold}	2.5			ns
Strobe time (see **Fig. 1**)		t_{Str}	2			ns
Deglitch input						
Deglitch input current						
at $V_{Degl} = 2.3$ V		$I_{I\,Degl}$			200	µA
at $V_{Degl} = 2.9$ V		$I_{I\,Degl}$	−150			µA
Deglitch voltage range		$-V_{Degl}$	+2.9		+2.3	V
Deglitch voltage (not connected)		V_{Dgl}		$0.5 \times V_{EE}$		V
Power supply[1]						
Supply voltage		V_{EE}	−5.46		−4.94	V
Supply current		I_{EE}		98	105	mA
Power consumption		P_D		495		mW

3

Comments

[1]) Measured at: 25 °C
$V_{EE} = -5.2$ V
Full-scale output current $I_Q = 20$ mA
Output load = 50 Ω

[2]) Guaranteed at: −25 °C to +85 °C
−5.46 V to −4.94 V
Full-scale output current $I_Q = 1$ mA to 40 mA

[3]) Measured at 100 °C
Full-scale output current $I_Q = 20$ mA
$V_{Degl} = -2.3$ V
$V_{EE} = -5.2$ V

[4]) $V_{IH} = -0.95$ V
$V_{IL} = -1.6$ V
Input signal rise time $t_r = 3$ ns

Switching all inputs at the same time in the same direction (worst case).

The crosstalk attenuation can be reduced by using other input signals.

Pulse diagram of the inputs

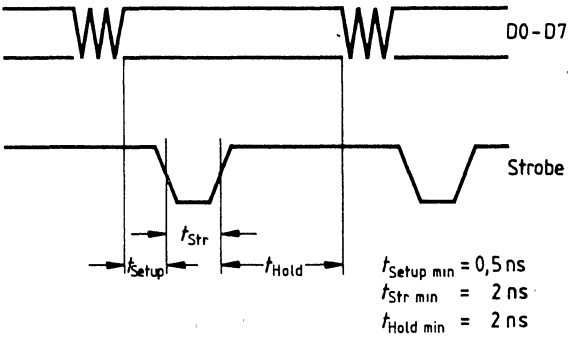


Figure 1

Terminology

Absolute unadjusted error

The full-scale output current with the same reference voltage and reference resistance is different for different chips. The variation results from the deviation of technology parameters. The specification is the maximum deviation from an average value.

Integral nonlinearity

The integral nonlinearity is the maximum deviation of the output of a linear regression from the output values of all possible input codes.

Differential nonlinearity

Differential nonlinearity is the difference between the actual and the ideal deviation between any two adjacent input codes, this being 1 LSB. A specified differential nonlinearity of ± 1 LSB max. over the entire operating temperature range ensures monotonicity.

Supply voltage sensitivity

The supply voltage sensitivity is the dependence of the analog output current on the supply voltage V_{EE} with all other parameters or conditions constant. It is specified in % per %.

Output rise time

The output rise time is the time between the 10% value and the 90% value of V_Q max. at the leading edge.

Output settling time

The output settling time is the time from the 50% point of the trailing strobe edge to the last entry of the analog output signal into an admissible error window of $\pm 1/2$ LSB.

The specified value is measured by using a comparator to detect the entry time point (see **fig. 2**).

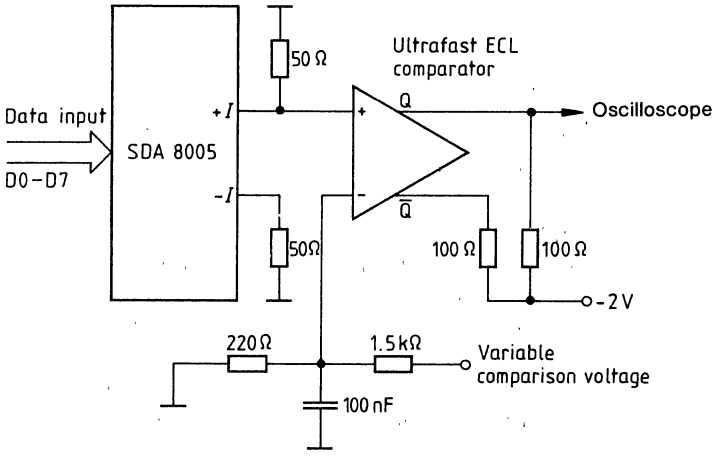
Adjusted worst case glitch area

Glitches which arise from input code switching can be minimized by varying the deglitch input voltage.

The specified value can be measured under the following conditions:

- Input code change from 01111111 to 10000000 and vice versa
- Input data are received with strobe
- Deglitch input voltage is optimized for switching in both directions

Figure 2 shows the test circuit and the timing diagram for the determination of the output settling time.



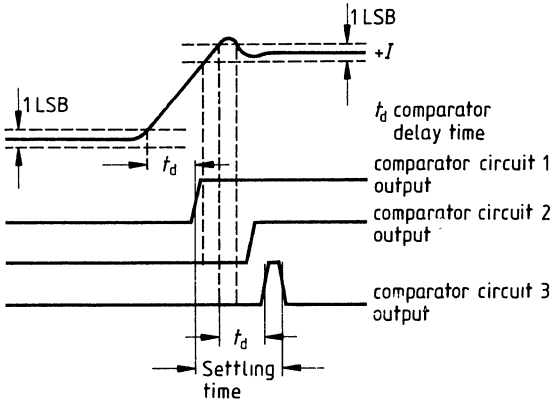


Figure 2

Application instructions

- Board with at least one ground area in its entirety.
- Ground pin should be connected very close to the large ground area by using contact studs or by direct soldering.
- Voltage supply must be blocked directly at the V_{EE} pin by using a 100-nF ceramic capacitor (preferably small chip capacitors).
- The analog outputs should be loaded with 50 Ω as near as possible to the package.
- Each of the DC voltages (V_{EE}, *DEGL*, V_{ref}) has to be checked for its suitability as regards ripple and noise.
- If a D/A output is connected to the 50-Ω input of a scope, an attenuator should be arranged on the D/A converter side of the connecting line to prevent the reflection from the oscilloscope from seeing the practically open line termination (output impedance of D/A converter approx. 20 kΩ); the ground connection between the board and the instrument should have a very low impedance.
- To minimize the crosstalk of used strobe to the output you can place a voltage divider at the strobe input to form an RC filter in combination with the input capacitance (see **figure**).

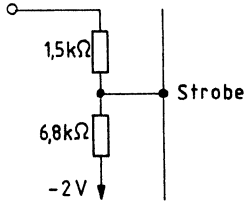


Figure 3 shows an application where the output signal is transmitted over a 50-Ω line to a receiver with a 50-Ω input, possibly a high-speed oscilloscope.

I_{ref} may be adjusted by varying V_{ref} between 0 V and 2.5 V, reference resistor R_{ref} being 1 kΩ.

Alternatively R_{ref} can be changed with V_{ref} constant.

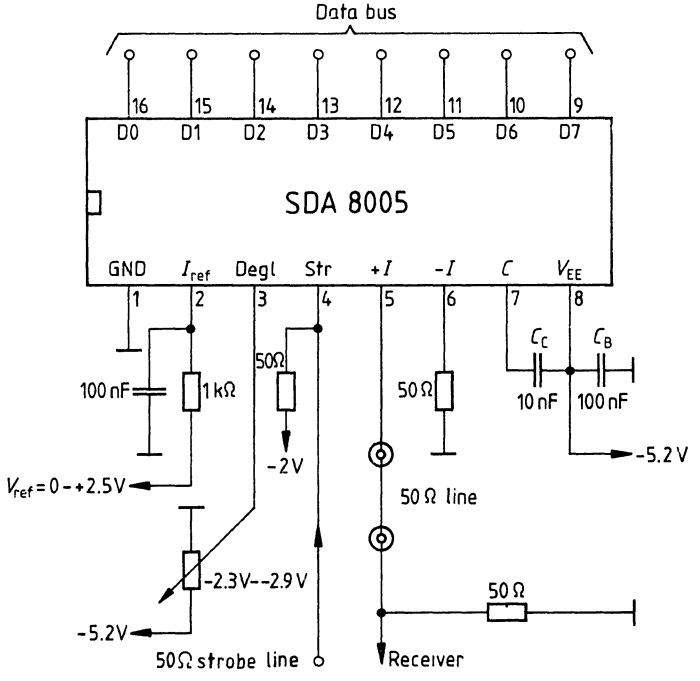


Figure 3

Here the strobe input is connected to a voltage divider, which forms an RC filter together with the input capacitance, and in this way reduces the digital crosstalk from strobe to output. The 100-Ω output line from $+I$ is terminated at both ends.

The high maximum, full-scale output current in this case also allows an acceptable voltage range.

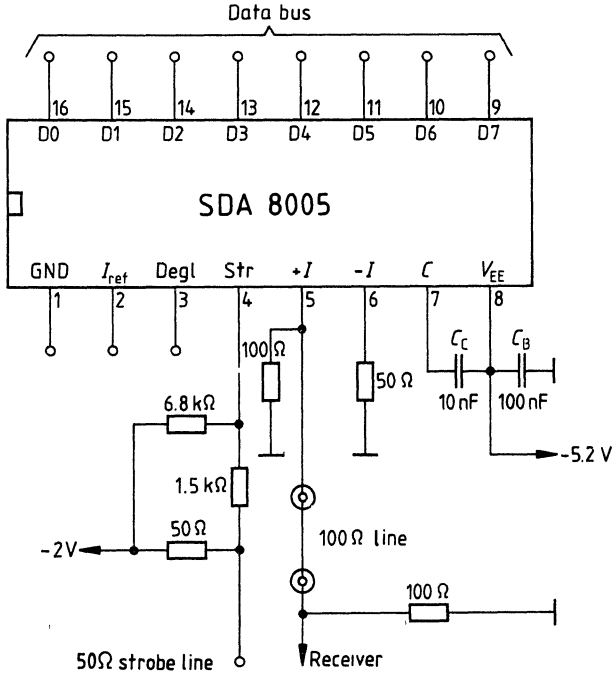


Figure 4

SIEMENS

Preliminary

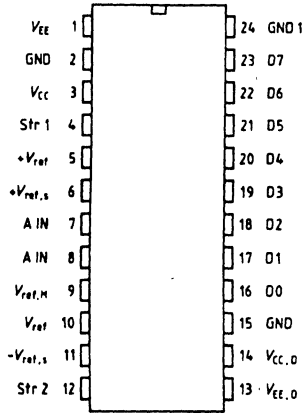
SDA 8010
8-Bit Analog/Digital Converter

- Maximum Conversion Rate >100 MHz
- 8-Bit Resolution
- 6.3 Effective Bits (F_{AN} = 30 MHz)
- Nonlinearity <½ LSB
- Excellent Large-Signal Bandwidth
- Extremely Low Error Rates
- Balanced Input Voltage Range
- ECL 100k Compatible Output Data
- Low Power Dissipation
- Small 24-Pin Ceramic Package

3

Pin Configuration

(Top View)



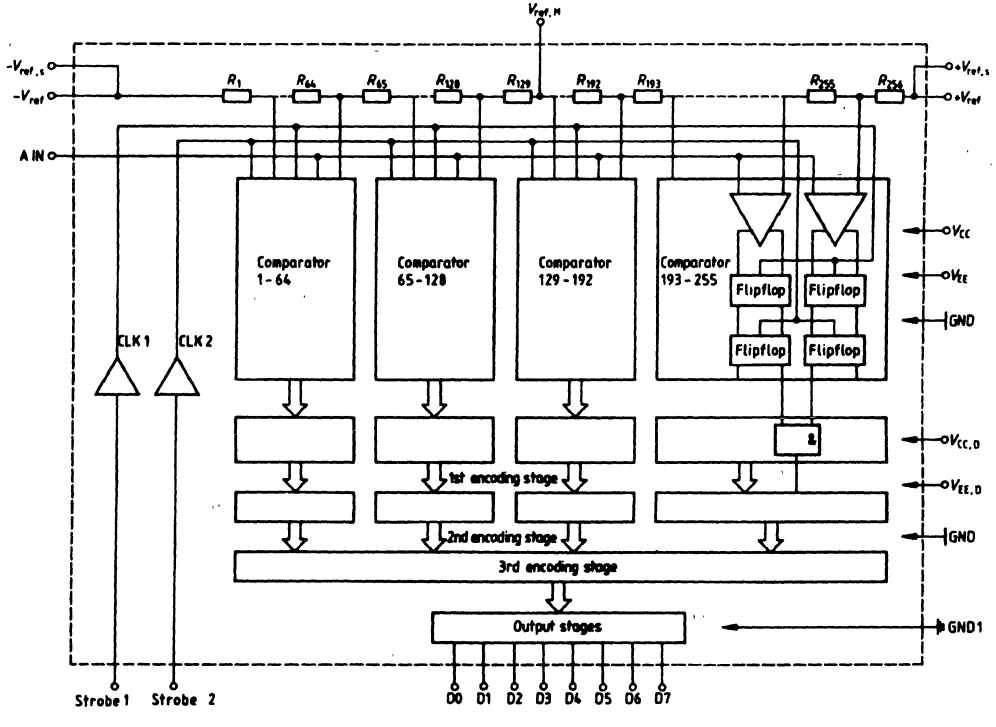
0152-1

Pin Definitions

Pin	Symbol	Function
1	V_{EE}	Negative Supply Voltage, Analog Section
2	GND	Ground
3	V_{CC}	Positive Supply Voltage, Analog Section
4	STR1	Strobe Signal 1
5	$+V_{REF}$	Pos. Reference Voltage
6	$+V_{REF,S}$	Pos. Reference Voltage Sense
7	A IN	Analog Input
8	A IN	Analog Input
9	$V_{REF,M}$	Center Tap of Voltage Divider
10	$-V_{REF}$	Negative Reference Voltage
11	$-V_{REF,S}$	Negative Reference Voltage Sense
12	STR 2	Strobe Signal 2
13	$V_{EE,D}$	Negative Supply Voltage, Digital Section
14	$V_{CC,D}$	Positive Supply Voltage, Digital Section
15	GND	Ground
16 to 23	D0 to D7	Digital Output Signal
24	GND 1	Ground Connection for Output Emitter Follower

The SDA 8010 is an ultrafast A/D converter according to the parallel principle, with a resolution of 8 bits and a guaranteed strobe frequency of 100 MHz. The device is capable of digitizing analog signals with full scale (±1V) frequency components up to 50 MHz at a power consumption of typically 1.3W. Due to the symmetric input voltage range it can be driven directly by a customary 50Ω source.

Block Diagram



Functional Description

The SDA 8010 is an ultrafast A/D converter according to the "flash" or parallel principle: A field of 255 comparators simultaneously compares the analog signal with 255 reference voltages spread linearly over the input voltage range. The result of this comparison, delivered in the so-called thermometer code, is converted into binary representation by three encoding stages and is then available as a digital signal with ECL levels at the outputs (**See Block Diagram**).

An individual comparator consists of a differential amplifier and a master/slave register stage. They are activated alternately by means of two strobe signals STR1 and STR2, thereby sampling the analog signal and holding the corresponding logical state. The sequence of the conversion process is given in the pulse diagram.

During the L phase of STR1, the analog signal is compared with the reference voltages. With the rising edge of STR1 the result of the comparison is passed into the first register stage and held there until the falling edge of STR1. Towards the end of this hold period the signal is accepted into the second flipflop with the L phase of the second strobe STR2 and stored with the rising edge. After a delay $t_{d,Q}$ this data appears at the output and remains valid for the period $t_{v,Q}$.

Driving the converter's analog input is an easy task. Due to the ground-symmetrical input voltage range and the low input capacitance, the converter can be operated in a customary 50Ω system without any preamplifiers or level shifters. Nevertheless, lower impedance driving would be a means for further improving the device's specified dynamic parameters. Two input pins AIN ensure low lead inductance. The internal reference voltages are generated by an

on-chip resistor string. The potentials at its end points, $+V_{REF}$ and $-V_{REF}$, respectively, determine the input voltage range which is resolved with an accuracy of 8 bits. Additional sense pins $+V_{REF,S}$ and $-V_{REF,S}$ allow compensation of voltage drops across parasitic resistances at top and bottom of the string. The assignment of the digital output code to the input voltage is shown in the transfer characteristic. As no overflow function is provided, the output will remain at a value of 255 when the reference voltage range is exceeded.

Connection $V_{REF,M}$ only serves for RF decoupling; no additional adjustment is required for maintaining the specified accuracy of ±0.5 LSB.

The use of two supply systems, V_{CC}, V_{EE} and $V_{CC,D}$, $V_{EE,D}$ and an additional ground line GND1 for the output stages reduces the mutual influence of analog and digital signals. Additionally, the separate return of the analog signal ground line is recommended (**See Test Circuit**).

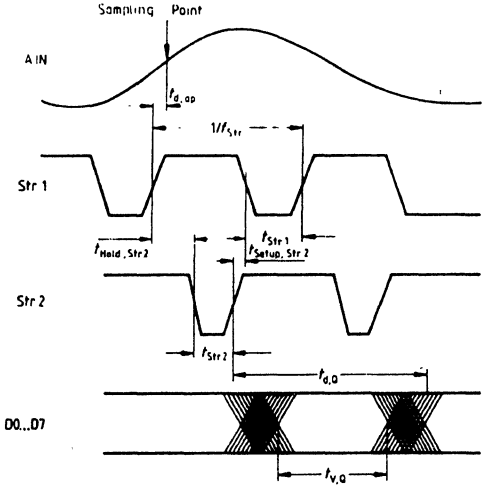
Strobe Timing (Note 1)

Symbol	Min	Typ	Units
t_{STR1}	4	5	ns
t_{STR2}	3	3.5	ns
$t_{Set\ Up,\ STR2}$	−2.0 (Note 2)	−1.5 (Note 2)	ns
$t_{HOLD,\ STR2}$	2		ns

Notes:
1. This is the recommended strobe setting for operation at 100 MHz. At lower strobe frequencies the timing more and more becomes uncritical. Below 75 MHz complementary strobe signals with a duty cycle of 50% may be used.
2. Negative values of $t_{Set\ Up,\ STR2}$ indicate, that the rising edge of STR2 should appear after the falling edge of STR1.

3

Pulse Diagram



0152-3

Absolute Maximum Ratings*

Positive Supply Voltages
(V_{CC}, $V_{CC,D}$) ..... −0.3V to +6.0V
Negative Supply Voltages
(V_{EE}, $V_{EE,D}$) ..... −6.0V to +0.3V
Reference Voltages (Note 1)
($+V_{REF}$, $-V_{REF}$ ..... −2.5V to +1.5V
Analog Input Voltage (V_{AIN}) ..... −2.5V to +1.5V
Digital Input Voltages
(V_{STR1}, V_{STR2}) ..... −3.5V to 0V
Output Current (I_{D0}–I_{D7}) ..... 20 mA
Junction Temperature (T_j) ..... 125°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Ambient Temperature (T_A)
(Without Dissipator) ..... 50°C
Storage Temperature (T_{stg}) ..... 125°C
Thermal Resistance Junction-Air
(Without Dissipator) ..... 50 K/W

Note:
1. $+V_{REF}$ always has to be more positive than $-V_{REF}$.

Electrical Characteristics

V_{CC}, V_{CCO} = 5V ±5%; V_{EE}, $V_{EE,D}$ = −4.5V ±5%; 25°C < T_j ≤ +125°C

Parameter	Symbol	Conditions	Limits			Units
			Min	Typ	Max	
Power Supply						
Pos. Supply Current, Analog	I_{CC}			95		mA
Pos. Supply Current, Digital	$I_{CC,D}$			85		mA
Total Pos. Supply Current	$I_{CC} + I_{CC,D}$			180	200	mA
Neg. Supply Current, Analog	I_{EE}			70		mA
Neg. Supply Current, Digital	$I_{EE,D}$			20		mA
Total Neg. Supply Current	$I_{EE} + I_{EE,D}$			90	100	mA
Power Dissipation	P_D			1.3	1.5	W
Permissible Supply Voltage Difference	ΔV_{CC}, ΔV_{EE}				700	mV
Reference Inputs						
Reference Voltages (Note 1)	$+V_{REF}$, $-V_{REF}$		−2		1	V
Total Reference Resistance	R_{REF}		105	150	190	Ω
Temperature Coefficient of Reference Resistor	T_C			3×10^{-3}		1/K
Analog Input						
Input Current (Note 2)	I_I	$V_{AIN} \geq +V_{REF}$ $V_{AIN} \leq -V_{REF}$	150		700 1	µA µA
Input Capacitance (Note 3)	C_{AIN}	$V_{AIN} \geq +V_{REF}$ $V_{AIN} \leq -V_{REF}$		45 55		pF pF

Electrical Characteristics (Continued)

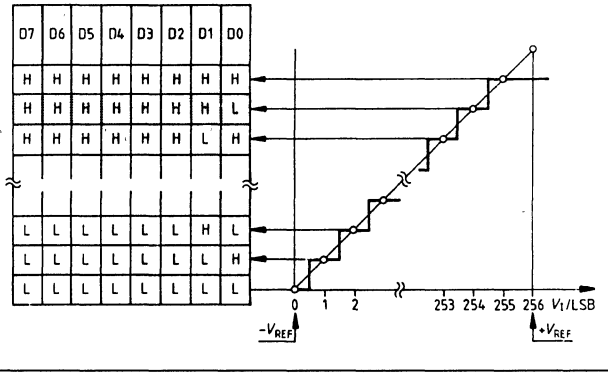
V_{CC}, V_{CCO} = 5V ±5%; V_{EE}, $V_{EE,D}$ = −4.5V ±5%; 25°C < T_j ≤ +125°C

Parameter	Symbol	Conditions	Limits			Units
			Min	Typ	Max	
Strobe Inputs						
Input High Voltage	V_{IH}		−1.165			V
Input Low Voltage	V_{IL}				−1.475	V
Input High Current	I_{IH}	$V_{STR} = V_{IH}$	2		30	µA
Input Low Current	I_{IL}	$V_{STR} = V_{IL}$			40	nA
Max. Strobe Frequency	$f_{Str.\,Max}$		100	125		MHz
Aperture Delay	$t_{d,\,ap}$			1		ns
Aperture Jitter	t_{jit}			15		ps
Data Outputs						
Output High Voltage	V_{QH}	100Ω to −2V	−1.025		−0.880	V
Output Low Voltage	V_{QL}	100Ω to −2V	−1.810		−1.620	V
Signal Transition Time	$t_{d,\,Q1}$ (Note 4) $t_{d,\,Q2}$ (Note 5)				10.5 14	ns ns
Time of Valid Output Data (Note 6)	$t_{v,\,Q}$	f_{STR} = 100 MHz	4	6		ns

Notes:
1. $+V_{REF}$ always has to be more positive then $-V_{REF}$.
2. The input current is linearly dependent on the input voltage.
3. In good approximation the dependency on V_{AIN} is linear (See Figure 2).
4. Delay from the rising edge of STR2 to the begin of validity of the associated output data. The typical temperature dependency is given in Figure 3.
5. Delay falling edge of STR2/Output data.
6. Time interval, during which the conversion of a 30 MHz 2 V_{PP} signal at 100 MHz sampling rate yields an SNR of more than 40 dB. The typical temperature dependency is given in Figure 3. Note the variation of the position of this period with temperature.

Characteristics include the guaranteed distribution boundaries of the values which are maintained by the integrated circuit in the specified operating range. The typical characteristics are mean values which are expected from manufacture. Unless otherwise specified, the typical characteristics are valid at T_A = 25°C.

Transfer Characteristic



Conversion Characteristics

V_{CC}, $V_{CC,\,D}$ = 5V ±5%, V_{EE}, $V_{EE,\,D}$ = −4.5V ±5%; 25°C < T_j < +125°C

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Static Nonlinearity (Note 1)						
Integral Nonlinearity	INL	ΔV_{REF} = 1.8V			0.5	LSB
Differential Nonlinearity	DNL	ΔV_{REF} = 1.8V		0.5	0.6	LSB
Dynamic Performance (Note 2)						
Large Signal Bandwidth	f_{3dB}		80			MHz
Signal-to-Noise Ratio	SNR	f_{AN} = 30 MHz f_{AN} = 45 MHz	40	43 35		dB dB
Total Harmonic Distortion	THD THD	f_{AN} = 30 MHz f_{AN} = 45 MHz		−43 −30		dB dB
Effective Bits	N_{eff}	f_{AN} = 1 MHz f_{AN} = 30 MHz f_{AN} = 45 MHz	 6.0	7.4 6.3 4.5		

Notes:
1. The actual transfer characteristic is measured by means of the well-known servo loop principle at both low sampling rates (100 kHz) and slow strobe edges (>500 ns).
2. Dynamic measurements are performed at 100 MHz sampling rate using the typical strobe timing. All specified parameters are derived from the FFT of the converter's response to a full scale (2 V_{pp}) sine wave input. The analog source impedance is 25Ω (50Ω line with 50Ω termination). The test circuit is shown in Figure 1.

Definition of Terms

Static Nonlinearity

Deviation of the actual transfer characteristic (output code as a function of input voltage) from that of an ideal ADC. It is expressed in terms of the measured transition voltages V_i (input voltage, at which the output code transition (i−1) ⟶ i occurs):

Integral nonlinearity INL—maximum deviation of the mean input voltage associated with any output code from the ideal value (in LSB), so

$$INL = \max \left| \left(\frac{V_i + V_{i+1}}{2} - \left(-V_{REF} \right) \right) \times \frac{256}{+V_{REF} - (-V_{REF})} - i \right|$$

Differential nonlinearity DNL—maximum deviation of the input voltage range associated with any output code from the ideal value (in LSB), so

$$DNL = \max \left| \left(V_{i+1} - V_i \right) \times \frac{256}{+V_{REF} - (-V_{REF})} - 1 \right|$$

Given values of INL and DNL are related to a reference voltage range $\Delta V_{REF} = (+V_{REF} - (-V_{REF}))$ of 1.8V.

Large Signal Bandwidth

That frequency of a sinusoidal 2 V_{PP} input signal, at which the amplitude of the signal derived from digital output data has decreased by 3 dB compared to the low-frequency value. The measurement is carried out at a sampling rate of 100 MHz in a 50Ω system. As this impedance together with the input capacitance forms the main limitation, bandwidth could be further increased by driving the input from a lower-impedance source.

Signal-to-Noise Ratio SNR

Energy ratio (in dB) of the fundamental to the sum of all other spectral components except harmonics in the spectrum of the quantized representation resulting from the conversion of a 2 V_{PP} input sine wave at 100 MHz sampling rate.

Total Harmonic Distortions THD

Energy ratio (in dB) of harmonic distortions (mainly resulting from 2nd and 3rd order harmonics) to the fundamental spectral component (see SNR).

Effective Bits

Resolution of an ideal converter that would give a quantization noise equal to the total noise and distortions produced by the tested device. It is related to the total SNR (including harmonics) by

$$N_{eff} = \frac{SNR_T\,[dB] - 1.8}{6}$$

$$\text{with } SNR_T = -10 \log \left[10^{-\frac{SNR}{10}} + 10^{\frac{THD}{10}} \right]$$

Diagrams

Analog Input Capacitance versus Input Bias Voltage

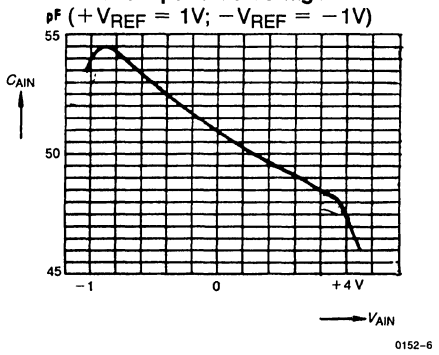


Figure 2

Signal Transition Time t_d, Q_7 and Valid Data Range $t_{V,Q}$ versus Junction Temperature

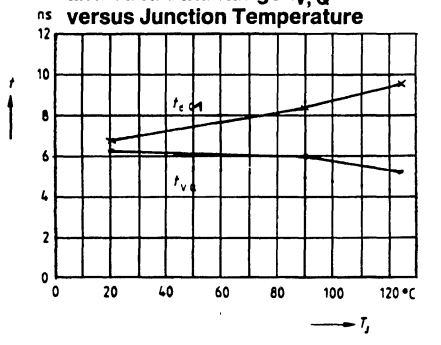
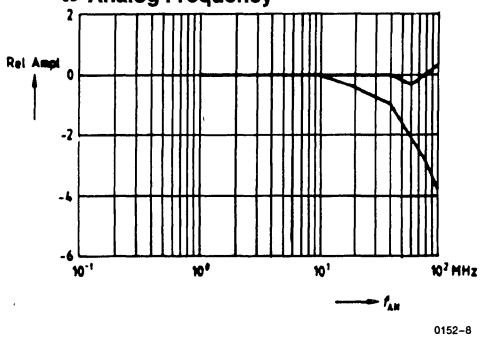


Figure 3

Amplitude Response versus Analog Frequency



a) Including voltage drop across source impedance (25Ω)

b) Without voltage drop across source impedance (25Ω)

Figure 4

Signal-to-Noise Ratio SNR and Harmonic Distortions THD2, 3 versus Analog Frequency

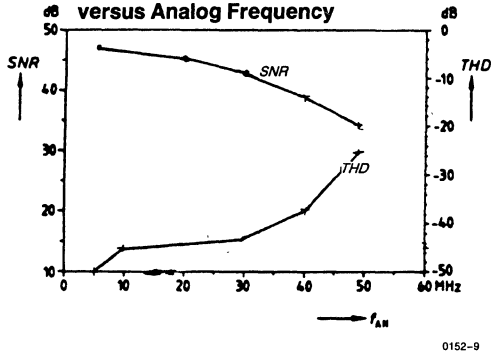


Figure 5

Test Circuit

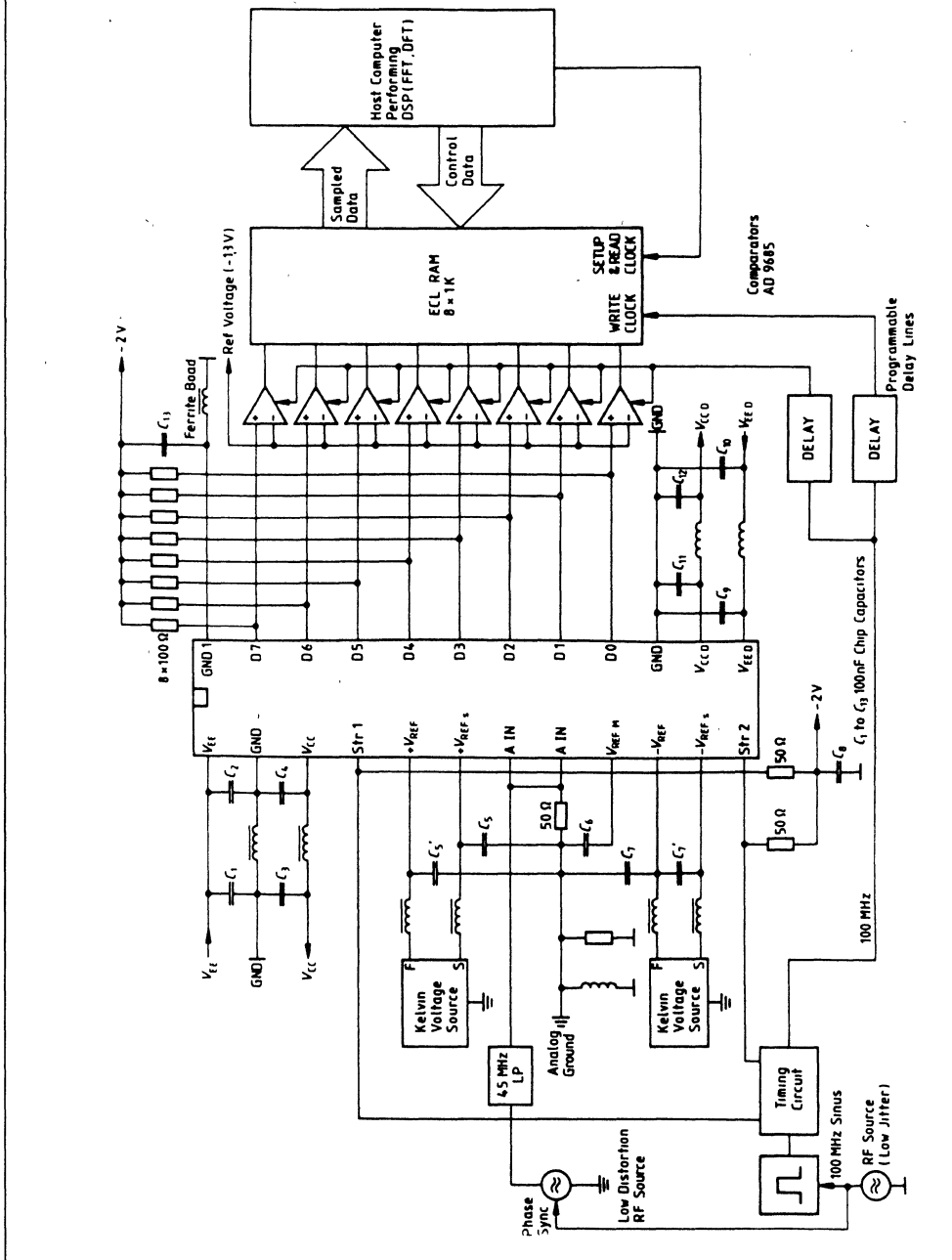


Figure 1

Diagrams (Continued)

Effective Resolution N_{eff} versus Analog Frequency

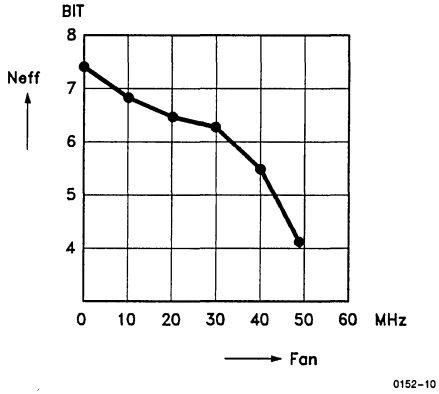


Figure 6

Ordering Information

Type	Ordering Code	Package
SDA 8010	Q67000-A2566	C-DIP 24

SIEMENS

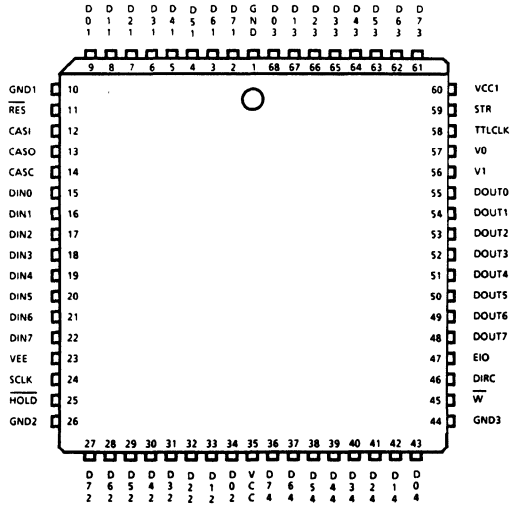
Preliminary

SDA 8020
Data Acquisition Shift Register (DASR)

- 8-Bit x 4 Shift Register
- ECL-Serial or TTL-Parallel Loading
- 125 MHz Shift Clock Frequency Typically
- Latches for Parallel TTL Input/Output Data
- TTL-Compatible Control Pins
- Cascadable, thereby Automatically Decreasing the TTL Clock Frequency
- Two Clock Outputs, TTLCLK and $\overline{W}$, for Easy Handling
- Interface between High Speed ECL and Slower TTL-Circuits
- Power Consumption Typically 1.5W

Pin Configuration

(Top View)



0113-1

The DASR SDA 8020 with ECL signal compatble inputs is capable of **DEMULTIPLEXING** an 8-bit wide data stream with a clock rate of up to 100 MHz into four parallel 8-bit TTL data channels with a clock rate of one fourth of the serial clock. In a second operating mode a **MULTIPLEX** function combining four 8-bit wide TTL data channels into one 8-bit ECL compatible channel with up to 100 MHz clock rate is provided.

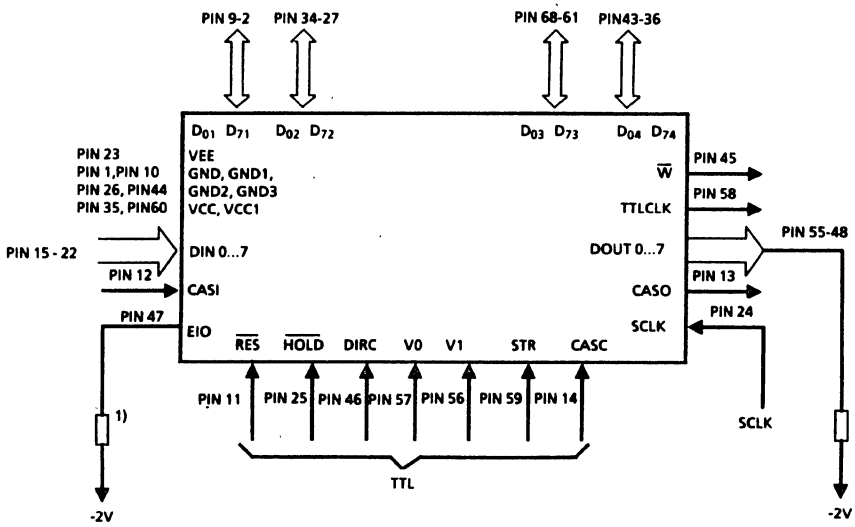
For the circuits, descriptions and tables indicated no responsibility is assumed as far as patents or other rights of third parties are concerned.

The information describes the type of component and shall not be considered as assured characteristics.

Terms of delivery and rights to change design reserved.

Liability for patent rights of third parties for components per se, not for circuitries/applications.

Basic Configuration



Note:
1. Only at multiplexing mode.

Pin Definitions and Functions

Pin	Type	Symbol	I/O	Function
1		GND		TTL Data Ground
9–2 34–27 43–36 68–61	TTL TTL TTL TTL	D_{01}–D_{71} D_{02}–D_{72} D_{04}–D_{74} D_{03}–D_{73}	I,O I,O I,O I,O	These are the 32 parallel TTL inputs or outputs (dependent on the DIRC input) of the single shift register cells. The fanout of these outputs is 2 TTL loads.
10		GND1		ECL Ground
11	TTL	$\overline{RES}$	I	By activating this input (low active) all 32 shift register cells are cleared and the clock generator is reset (DOUT0–DOUT7 = Low, TTLCLK = Low, $\overline{W}$ = High).
12, 13	—	CASI, CASO	I,O	Cascading in, Cascading out (see Figure 2): These two pins control in connection with the Cascading control input the TTL-Clock rate and internal strobe timing. Used only to establish the clock loop. They don't provide ECL compatibility.
14	TTL	CASC	I	Cascading Control: The required logic level at this input depends on the cascading configuration (see chapter "Cascading" and Figure 2). A single chip configuration requires a high level.
15–22	ECL	DIN0–DIN7	I	ECL data input byte
23		VEE		Negative supply voltage; ECL section
24	ECL	SCLK	I	The single shift register cells are clocked by this signal. Data pending at DIN0–DIN7 are transferred with the falling clock edge.
25	TTL	$\overline{HOLD}$	I	A logic low at the $\overline{HOLD}$ input inhibits the shift clock and sets the 32 parallel I/Os into the high impedance state. The register is inactive.
26		GND2		TTL ground; clock and control section

Pin Definitions and Functions (Continued)

Pin	Type	Symbol	I/O	Function
35		VCC		Positive supply voltage; TTL data section
44		GND3		Ground for ECL output emitter followers
58	TTL	TTLCLK	O	The frequency of the TTL-Clock in single chip operation is 1/4 of the shift clock frequency. In a cascaded configuration the TTL-Clock frequency is automatically decreased.
46	TTL	DIRC	I	A logic high on the DIRC configurates the DASR for parallel in/ serial out (multiplexing, parallel loading), and a logic low for serial in/parallel out (demultiplexing, serial loading) operation.
47	ECL	EIO	I,O	Enables the internal data transfer from the latches to the shift registers in multiplexing mode. In this mode the EIOs provide internal timing information to all cascaded DASRs. This pin must be connected to −2V via 1k resistor (see Figure 2). In demultiplexing mode the EIO pin has no influence on internal timing and could be left open.
55–48	ECL	DOUT0–DOUT7	O	ECL data output byte. Data are transferred to the output on the falling SCLK edge.
56, 57	TTL	V1, V0	I	With V0, V1 one of four possible delay times of the $\overline{W}$ signal is selected.
45	TTL	$\overline{W}$	O	The $\overline{W}$ output has the same frequency as the TTLCLK but other duty cycle (1/4 in single chip operation). It could be used as the write or chip select signal for high speed MOS SRAMs which are placed at the parallel inputs/outputs. It can be delayed in multiples of shift clock periods programmable by V0, V1 (see Programming Table for V0, V1 below).
59	TTL	STR	I	The four 8-bit data words are latched in the first input/second output latch by the Strobe. A high strobe level makes these latches transparent.
60		VCC1		Positive supply voltage; TTL clocks and control signal section.

Programming Table for V0, V1

V0	V1	Delay of $\overline{W}$
0	0	0 SCLK-Period
0	1	1 SCLK-Period
1	0	2 SCLK-Periods
1	1	3 SCLK-Periods

Circuit Description

The DASR contains eight parallel 4-bit long shift registers, each of them with two internally cascaded level-operated input/output latches. The device has 8 ECL compatible serial inputs and outputs and 32 parallel TTL compatible common inputs/outputs. Beside the data inputs and outputs the device is equipped with 7 mode control inputs and it provides 2 clock signals which especially support the use of the DASR together with fast static MOS RAMs in a data acquisition system. All these inputs and outputs are TTL compatible.

The clock section comprises a 1-bit x 4 shift register whose output (CASO) is fed back to its input (CASI) via the external clock loop. If the cascade control input (CASC) is set to H a single pulse is written into the first shift register cell. When $\overline{HOLD}$ is released this single clock pulse is moved around the clock loop and all timing signals are derived from this pulse.

The DASR is intended primarily as an interface between a high speed A/D or D/A converter and the memories in a data acquisition or waveform generating system. Further applications are high speed logic analyzers and digital word generators.

Operation Mode

The DASR has two distinct operation modes, selected by the DIRC. For avoiding excessive power dissipation those circuit parts, which are unused in one mode, are switched off.

Serial In/Parallel Out

After activating the DASR by asynchronous $\overline{RES}$ and $\overline{HOLD}$ (see Figure 3 for recommended $\overline{HOLD}$, $\overline{RES}$-timing), the 8-bit wide ECL data words (present at DIN0–DIN7) are loaded synchronously into the register by the falling SCLK edge. Shortly after every fourth trailing SCLK-edge the content of the single shift register cells are strobed into the first output latch by an internally created clock. These four data bytes appear at the outputs (D01–D71, D04–D74) after they are passed to the second output latch by the external STR signal. This latch can be also made transparent by setting STR to H or not connecting this pin. The first acquired data byte appears at D04–D74, the second at D03–D73, the third at D02–D72 and the fourth at D01–D71. Due to the inherent skew of the latches a falling edge of the external STR must not appear during a short interval ($t_{H,STR,D}$) after every fourth SCLK period (because output latch 1 is just made transparent; see Figure 6).

An acquisition cycle is finished by a negative $\overline{HOLD}$ level, which is internally synchronized first with the leading TTLCLK edge and second with the leading $\overline{W}$ edge. This double synchronization eases stopping the acquisition on a well-defined sample (see application example, Figure 10).

There are a few possibilities of the TTLCLK-waveform at the end of an operation cycle depending on the delay of $\overline{W}$ (see Figure 3). $\overline{W}$ remains high after stopping the DASR. When inhibiting SCLK by $\overline{HOLD}$ the TTL data outputs change to the high impedance state.

Parallel In/Serial Out

Synchronous parallel loading is accomplished by applying four 8-bit TTL data words at D01–D74 and taking the STR high.

Every fourth SCLK-period, beginning with the 6th falling edge of SCLK after starting operation with a high $\overline{HOLD}$, the second input latch is transparent for one SCLK-cycle. With the next falling edge of SCLK the data are written into the shift register cells. The first valid data at DOUT appear not before the 8th falling edge of SCLK from the beginning onwards. Those data pending at D04–D74 are shifted out first and those at D01–D71 at last within a TTLCLK cycle. For getting defined starting conditions at DOUT, DIN should be set to logic low. The setup and hold times $t_{S,D,SCLK}$, $t_{H,D,SCLK}$ apply only if the first input latch is made transparent by setting STR to H.

In either operating mode the first rising edge of the TTLCLK appears two falling edges of shift clock after activating the DASR. The first $\overline{W}$ pulse with a duration of one SCLK cycle and a delay programmed by V0 and V1 is provided after the third falling edge of SCLK.

Cascading

The ability to cascade the DASR enables lower TTL data rates in connection with the advantage of a 100 MHz shift clock. By cascading the DASR the CASO of one device must be connected with the CASI of the next. This clock loop is closed by connecting the CASO of the last DASR with the CASI of the first one. Furthermore the Cascading control input (CASC) only of one DASR is set high (see Figure 2). The position of the DASR with a high CASC input determines the moment of the internal strobes for transferring data to the second input latch and to the single shift register cells, in parallel in/serial out mode (see Figure 5). The first internal strobes appear at the same time as in single chip operation and their period depends on the length of the shift register cascade. In a system with cascaded DASRs the first edge of $\overline{W}$ or TTLCLK is offered at that DASR with CASC = H. The $\overline{W}$ and TTLCLK signals of the other SDA 8020s are provided in such a succession as they are interconnected via CASI, CASO.

The time delay between the rising edges of the TTLCLK signals is four SCLK periods. In parallel in/ serial out mode all EIOs must be tied together and connected to −2V via a 1 kΩ resistor. In serial in/ parallel out mode the position of the DASR with a high CASC is unimportant for internal timing. In this mode the period of the internal strobe (for output latch 1) is not increased. So the data of the shift registers are strobed to the output latch 1 every fourth SCLK period. For getting valid TTL output data over the whole TTLCLK period a STR pulse with a duration of maximal 4 SCLK periods must be used, e.g.: $\overline{W}$ (see Figure 4). The signals at the EIOs are for internal use only (see Figure 2).

The TTL-Clock high phase of the DASRs with a low CASC is doubled. When cascading the DASR the $\overline{W}$ signal can be delayed not only in four steps as in the single chip configuration but over the whole TTL clock period by using the $\overline{W}$ output of the appropriate chip.

Functional Block Diagram

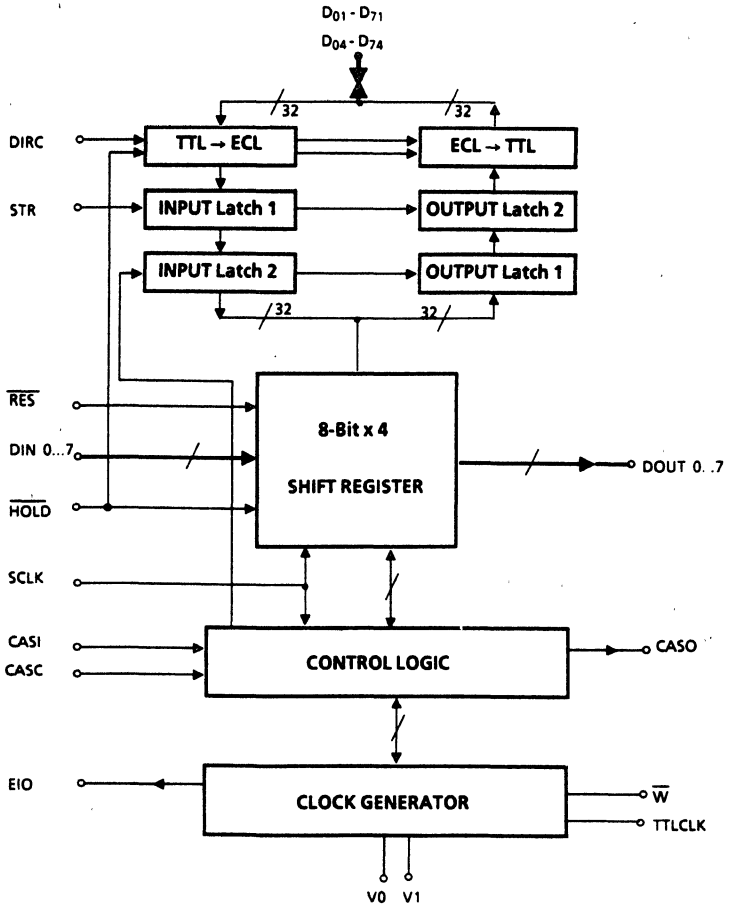


Figure 1

Cascading Block Diagram

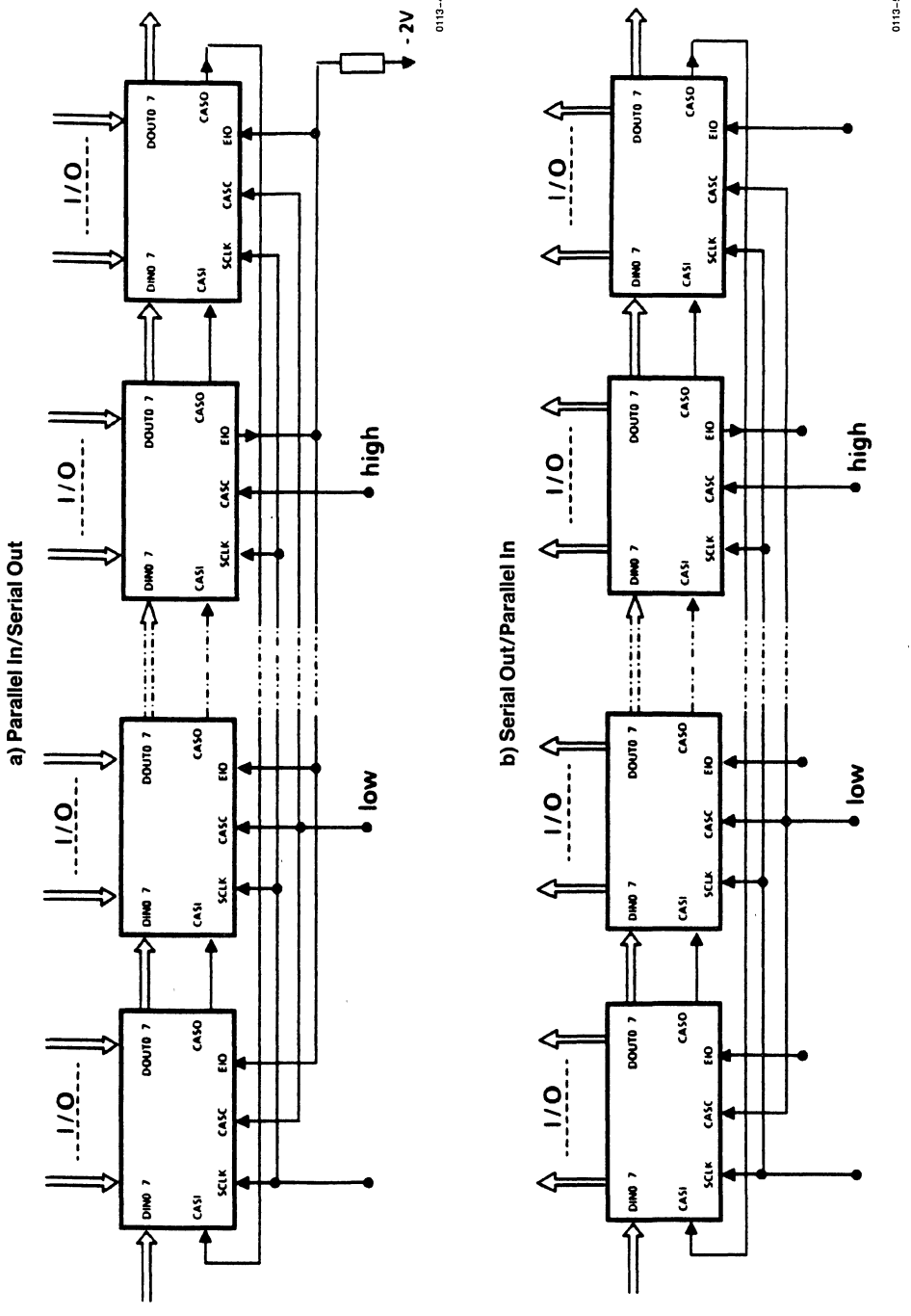
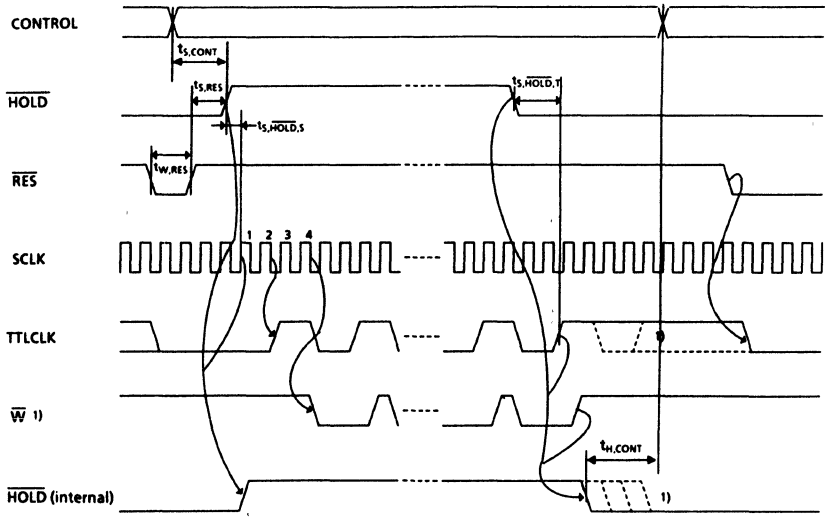


Figure 2

HOLD/RES-Timing



Note:
1. Dependent on the programmed delay of $\overline{W}$; solid line shows conditions for V0 = 0, V1 = 0.

Figure 3

Cascading of Two DASRs—Serial In/Parallel Out

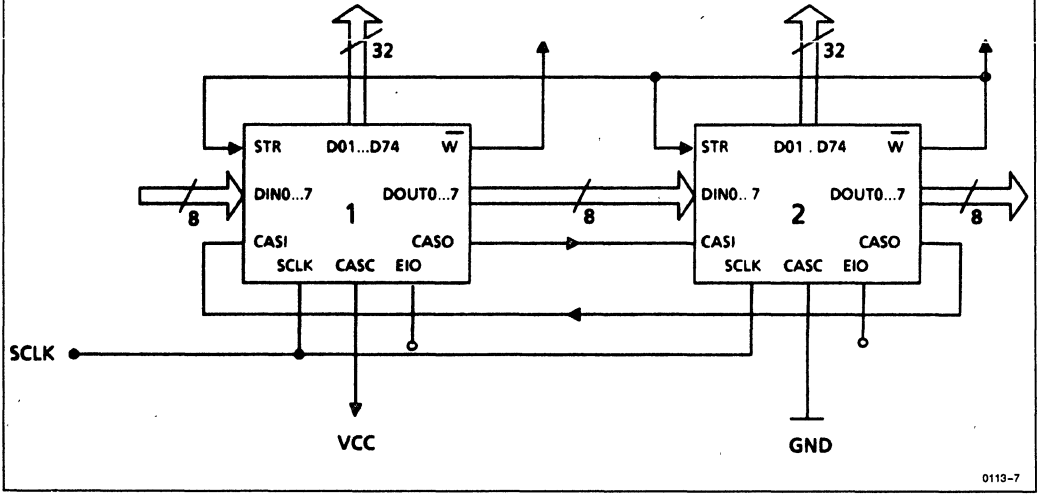
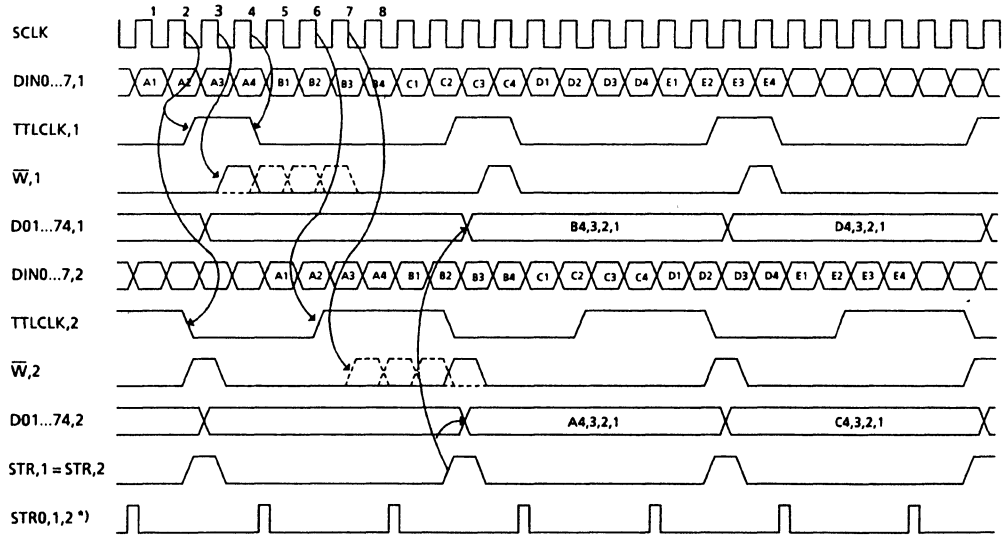


Figure 4a

Cascading of Two DASRs—Serial In/Parallel Out



*Controls output latch 1 of either DASR.

Figure 4b

Cascading of Two DASRs—Parallel In/Serial Out

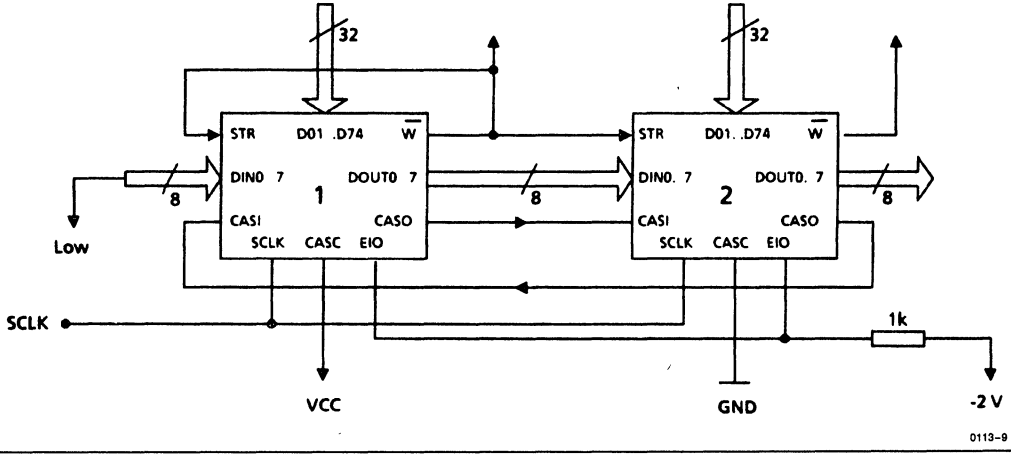
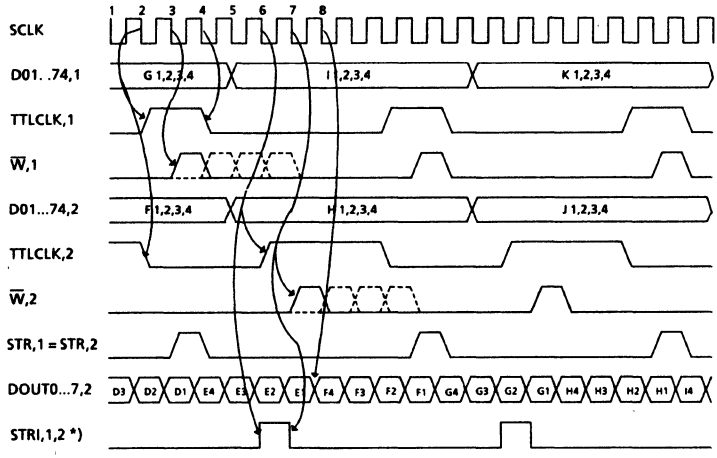


Figure 5a

Cascading of Two DASRs—Parallel In/Serial Out



*Controls Input Latch 2 of either DASR.

Figure 5b

Timing Relations at Serial In/Parallel Out Operation

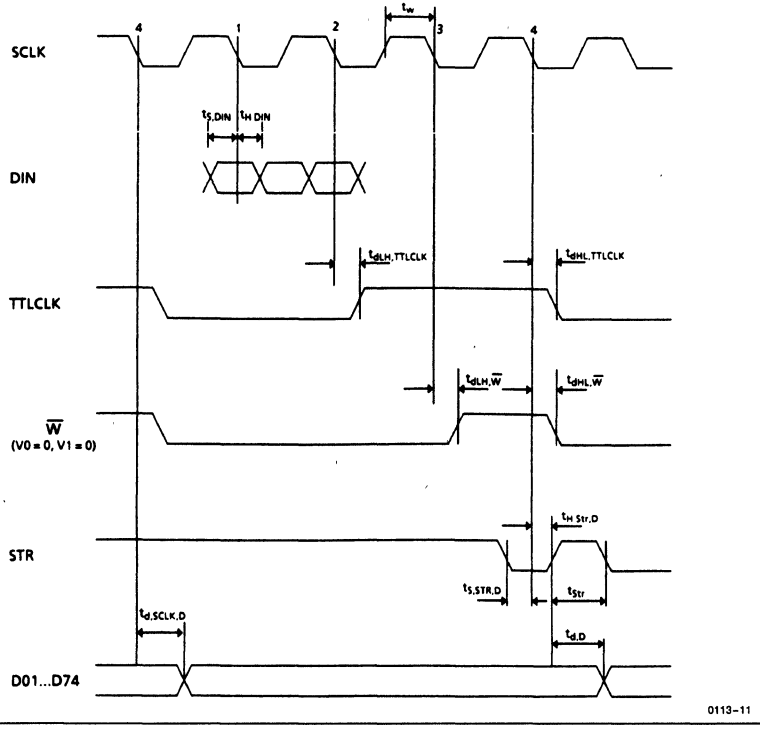


Figure 6

Timing Relations at Parallel In/Serial Out Operation

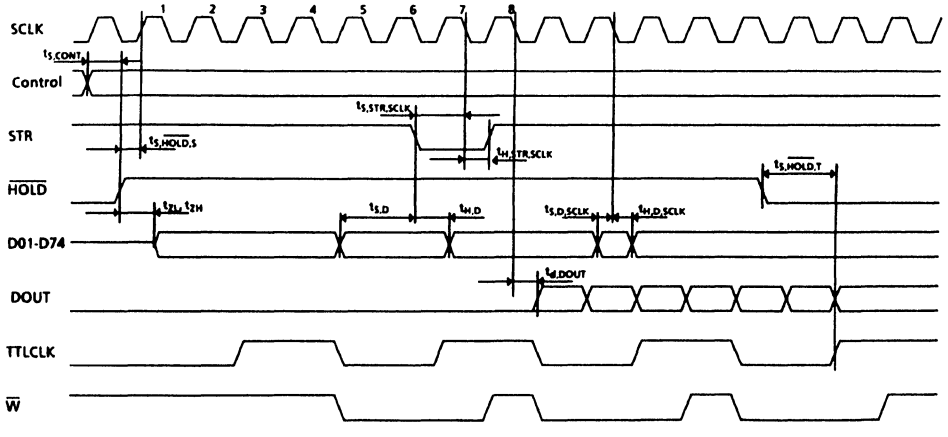


Figure 7

Absolute Maximum Ratings*

Maximum ratings are absolute limits. The integrated circuit may be destroyed if only a single value is exceeded.

Maximum Rating for
Ambient Temperature .... $-25°C < T_A < +70°C$

Positive Supply
Voltages (V_{CC}) ..... $-0.3V$ to $+6.0V$

Negative Supply
Voltages (V_{EE}) ..... $-6.0V$ to $+0.3V$

ECL Input Voltages ..... $-3.5V$ to $0V$

ECL Output Voltages ..... $1V$

TTL Input and Output
Voltages ..... $-0.6V$ to $+5.5V$

Tri-State Currents
into $D_{01}-D_{74}$ ..... 1 mA

Output Current at W ..... $-40^{(1)}$ mA to $+40^{(2)}$ mA

Notes:
1. High-State.
2. Low-State.

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Output Current
at $D_{01}-D_{74}$ ..... $-10^{(1)}$ mA to $+10^{(2)}$ mA

Output Current
at TTLCLK ..... $-20^{(1)}$ mA to $+20^{(20)}$ mA

Output Current
at DOUT0–DOUT7 ..... -20 mA to 0 mA

Output Current at EIO ..... -10 mA to 0 mA

Junction Temperature (T_J) ..... $125°C$

Storage Temperature (T_S) ..... $-55°C$ to $+125°C$

Thermal Resistance:

System-Air (R_{thSA}) ..... 30 K/W

System-Package (R_{thSP}) ..... 15 K/W

Electrical Characteristics

The electrical characteristics include the guaranteed distribution boundaries of the values which are maintained by the integrated circuit in the specified operating range. The typical characteristics are mean values which are expected from fabrication. Unless otherwise specified, the typical characteristics are valid at T_A = 25°C and the specified supply voltage.

Supply Voltages: V_{CC} = 5V ±5%, V_{EE} = −4.5V ±5%, $|V_{CC} - V_{CC1}| < 0.5V$

Ambient Temperature: $-25°C < T_A < 70°C$

Parameter	Symbol	Conditions	Test Circuit	Limits			Units
				Min	Typ	Max	
Power Supply							
Positive Supply Current	I_{CC}				65	80	mA
Negative Supply Current	I_{EE}				240	250	mA
TTL-Pins							
High-Level Input Voltage	V_{IHT}			2			V
Low-Level Input Voltage	V_{ILT}					0.8	V
High-Level Input Current	I_{IHT}	V_{CC} = Max; V_I = 2.4V				30	µA
Low-Level Input Current	I_{ILT}	V_{CC} = Max; V_I = 0.5V				−1.6	mA
High-Level Output Voltage	V_{OHT}	V_{CC} = Min; I_{IOH} = −800 µA	a	2.4			V
Low-Level Output Voltage	V_{OLT}	V_{CC} = Min; I_{OL} = 3.2 mA	a			0.5	V
Off-State Output Current	I_{OZLT}	V_{CC} = Max; V_O = 0.5V				−50	µA
	I_{OZHT}	V_{CC} = Max; V_O = 2.4V				50	µA
ECL-Pins							
High-Level Input Voltage	V_{IHE}			−1.165		−0.88	V
Low-Level Input Voltage	V_{ILE}			−1.81		−1.475	V
High-Level Output Voltage	V_{QHE}		c	−1.025		−0.88	V
Low-Level Output Voltage	V_{QLE}		c	−1.81		−1.62	V
CASI, CASO							
High-Level Input Voltage	V_{IHC}			−1.0		−0.65	V
Low-Level Input Voltage	V_{ILC}			−1.6		−1.35	V
High-Level Output Voltage	V_{OHC}				−0.9		V
Low-Level Output Voltage	V_{OLC}				−1.55		V
Maximum Load Capacity at CASO	C_{CASO}					5	pF

Timing Characteristics

Parameter	Symbol	Conditions	Test Circuit	Limits			Units
				Min	Typ	Max	
Setup Time DIN 0–7 to SLCK	$t_{S,DIN}$			0.5			ns
Hold Time DIN 0–7 to SCLK	$t_{H,DIN}$			2.0			ns
Setup Time D01–D74 to STR	$t_{S,D}$(1)			8.0			ns
Hold Time D01–D74 to STR	$t_{H,D}$(1)			0			ns
Setup Time Control to $\overline{HOLD}$	$t_{S,CONT}$(2)			30	7		ns
Hold Time Control to $\overline{HOLD}$	$t_{H,CONT}$(2, 6)			20	0		ns
Min. Setup Time STR to SCLK	$t_{S,STR,D}$(1, 3)				−4.5		ns
Min. Hold Time STR to SCLK	$t_{H,STR,D}$(1, 3)				6.5		ns
Min. Setup Time $\overline{HOLD}$ to SCLK	$t_{S,\overline{HOLD},S}$				14	20	ns
Setup Time $\overline{HOLD}$ to TTLCLK	$t_{S,\overline{HOLD},T}$			20			ns
Setup Time RES to $\overline{HOLD}$	$t_{S,RES}$			20			ns
Min Setup Time STR to SCLK	$t_{S,STR,SCLK}$(4, 7)				3		ns
Min Hold Time STR to SCLK	$t_{H,STR,SCLK}$(4, 7)				0		ns
Min Setup Time D01–D74 to SCLK	$t_{S,D,SCLK}$(5)				5		ns
Min Hold Time D01–D74 to SCLK	$T_{H,D,SCLK}$(5)				1		ns
Delay SCLK—D01–D74	$t_{d,SCLK,D}$	R_L = 1200, C_L = 15 pF	a		24		ns
Delay STR—D01–D74	$t_{d,D}$	R_L = 1200, C_L = 15 pF	a	16.5	21	23	ns
Delay DIRC, HOLD—D01–D74	t_{ZL}, t_{ZH}	R_{L1} = 1200, C_L = 15 pF	b		40		ns
Delay DIRC, HOLD—D01–D74	t_{HZ}, t_{LZ}(6)	R_{L1} = 1200, C_L = 15 pF	b		25		ns
Delay SCLK—$\overline{W}$	$t_{dHL,\overline{W}}$	R_L = 1200, C_L = 40 pF	a		9.5	13	ns
Delay SCLK—$\overline{W}$	$t_{dLH,\overline{W}}$	R_L = 1200, C_L = 40 pF	a		9	11	ns
Delay SCLK—TTLCLK	$t_{dLH,TTLCLK}$	R_L = 1200, C_L = 15 pF	a		11	13	ns
Delay SCLK—TTLCLK	$t_{dHL,TTLCLK}$	R_L = 1200, C_L = 15 pF	a		12.5	15	ns
Delay SCLK— DOUT 0–7	$t_{d,DOUT}$		c		5	7.5	ns
Delay RES—DOUT 0–7	t_d		c		15		ns
Pulse Width of SCLK	t_W			4			ns
Pulse Width of RES	$t_{W,RES}$			30			ns
Min Pulse Width of STR	t_{STR}				6		ns
Max SCLK Frequency	f_{SCLK}			100	125		MHz

Notes:
1. Only every 4th SCLK-period from the 4th trailing edge on.
2. Control: Signals DIRC, V0, V1, CASC.
3. Doesn't apply if output latch 2 is transparent.
4. Doesn't apply if input latch 1 is transparent.
5. Only every 4th SCLK-period and if input latch 1 is transparent.
6. Refers to HOLD after internal synchronization.
7. Only every 4th SCLK period from the 7th trailing edge on.

Test Circuits

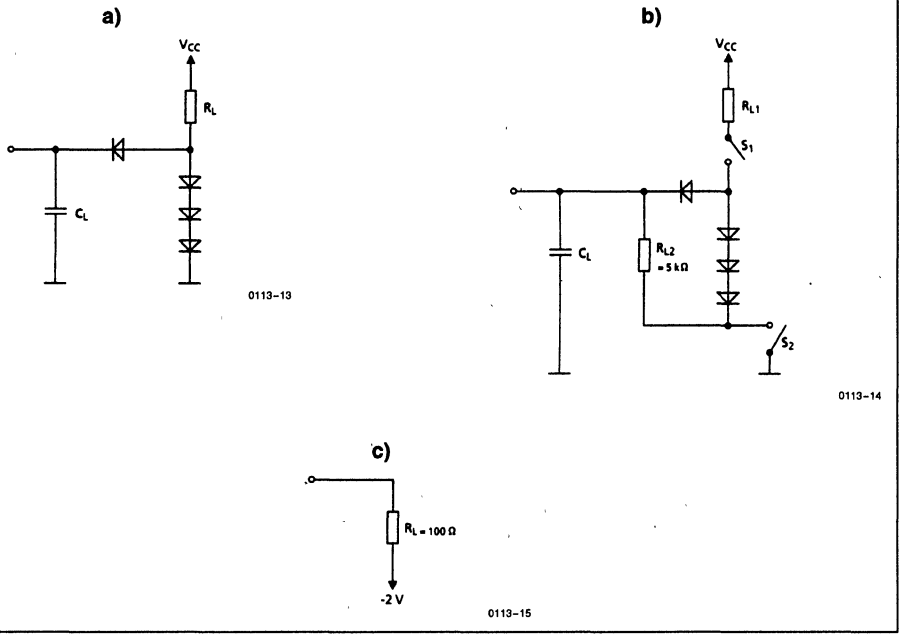


Figure 8

Application Examples

Data Acquisition (Serial In/Parallel Out)
(See Figure 10 and Figure 11)

In the first example a high speed data acquisition system consisting of an 8-bit/100 MHz A/D-converter (SDA 8010), CMOS SRAMs (tacc ≤ 35 ns), a µP-interface (SAB 8286) and a high speed TTL address counter is shown.

The analog input signal with frequency components of up to 50 MHz is sampled and converted to 8-bit digital data by the SDA 8010. These ECL data are demultiplexed into four TTL data streams by the DASR. Writing the TTL data to the fast CMOS SRAMs is supported by DASR signals $\overline{W}$ and TTLCLK. When an acquisition cycle is finished, e.g. after the counter has clocked out the memories' top address, a low $\overline{HOLD}$ disables the DASR and the TTL data outputs change to the high impedance state. Now a microprocessor or -controller access to the acquired data is possible via the single bus transceivers.

The input/output configuration is attained by setting DIRC to low. The best way for starting the system is to reset the DASR before activating it by a rising $\overline{HOLD}$ edge. Now data acquisition can be easily interrupted and restarted (e.g. after the memories are read out via the bus transceivers) only by $\overline{HOLD}$.

The critical time relations in this system are set by the requirement of the CMOS memories. Usually the chip select signal for the memories must be high during address transitions (CS controlled write cycle). This high pulse should be as short as possible for easy memory timing. Additionally, the time of valid data at the parallel TTL outputs (i.e. the memory inputs) is in a tight relation to the chip select signal. These requirements can be met by connecting the $\overline{W}$ with the Strobe (STR) and adjusting the $\overline{W}$ delay time by V0, V1. Sometimes, especially when the memories are operated near their frequency limit, it could become necessary to delay $\overline{W}$ slightly by an external device (T1), but this should not be the normal case. Because the data out valid time of the DASR is correlated with the memories' chip select signal by the Strobe, the timing demands of the memories are fulfilled. The delay of $\overline{W}$ is mainly determined by the memories' address transitions, which have to be during the $\overline{CS}$ high phase. To get a close time relation between the DASR and the address counter the TTLCLK is used as the counter's clock. RCOUNT is a signal of lower frequency than TTLCLK for reading the memories to the µP-data bus ($\overline{HOLD}$ = L, $\overline{CS1}$ = L, $\overline{W1}$ = H).

Data Acquisition System

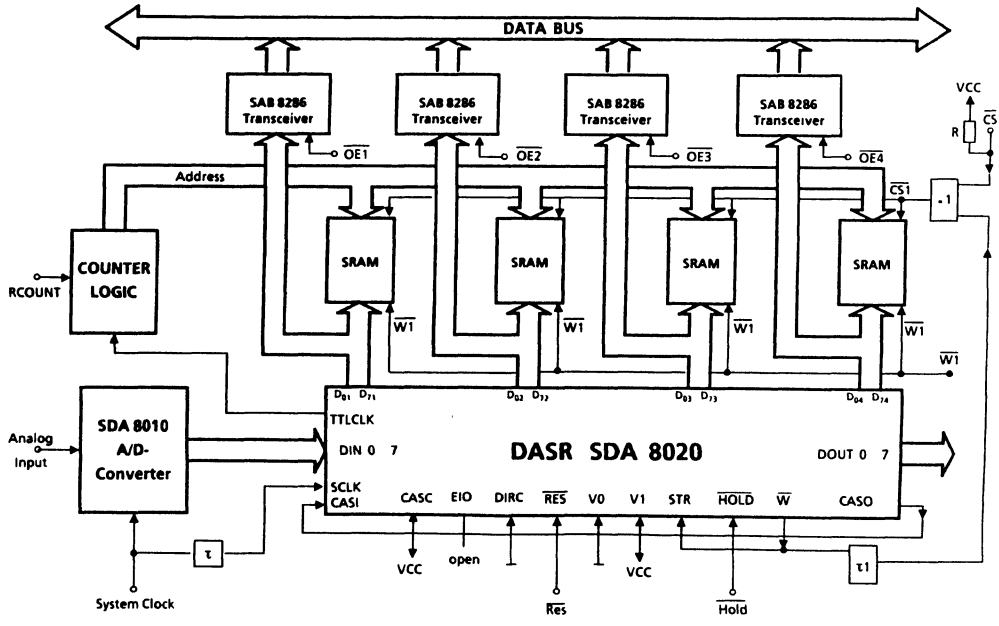
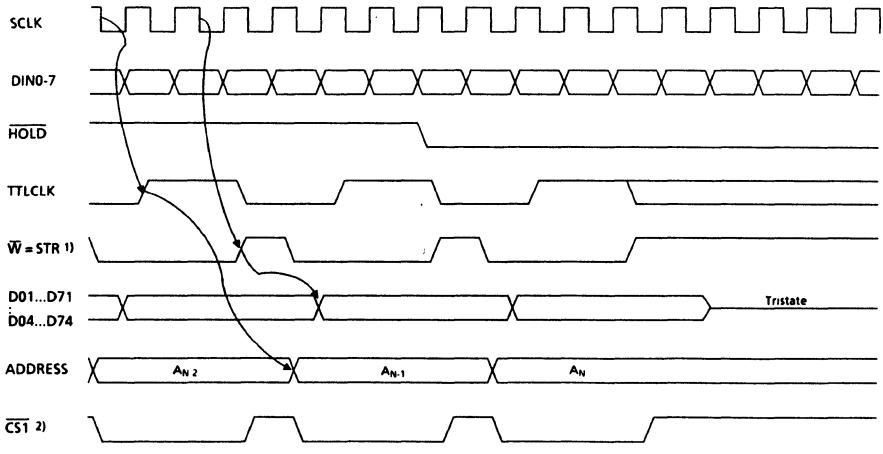


Figure 10

Serial In/Parallel Out (End of Operation)



Notes:
1. Delay programmed by V0, V1.
2. Additional delay by external circuit.

Figure 11

The data acquisition system of Figure 10 is not configured for all SCLK frequencies. If frequency independent operation is required the rising $\overline{W}$ edge and that TTLCLK edge, which clocks the address counter, must have the same reference edge of SCLK. This is attained by the falling TTLCLK edge and the second possible $\overline{W}$ pulse (V0 = 0, V1 = 1; reference edge is the fourth SCLK edge) or by the leading TTLCLK edge and the fourth possible $\overline{W}$ pulse (V0 = 1, V1 = 1; reference edge is the sixth SCLK edge). In the second case the first TTLCLK's leading edge after starting must be suppressed for writing defined data to the whole memory or the counter's start/stop-addresses are manipulated suitably.

Waveform Generation (Parallel In/Serial Out)
(See Figure 12 and Figure 13)

The second example shows a waveform generating system consisting of two cascaded DASRs, an 8-bit/7 ns D/A-converter (SDA 8005), CMOS SRAMs (tacc ≤ 75 ns), the same µP-interface as above and a fast TTL counter, preferably a programmable one.

With these few components a very versatile waveform generating system can be constructed. First the desired waveform must be written into an EPROM. These data are then transferred to the fast SRAMs, e.g. memories with 45 ns access time organized as 8k words of 8 bits each, under control of the SAB 8051. With such memories the available memory space for the digitized waveform is 64k words of 8 bits. The cascaded shift registers represent an 8 to 1 multiplexer with 100 MHz data at the outputs DOUT0–DOUT7 of the second DASR. The digital data are converted to the analog waveform by the SDA 8005.

The following timing mainly depends on the speed of the memories and on the delay time of the counter which provides the memory addresses. After valid memory addresses and the subsequent address access time, data applied at the parallel TTL inputs of the DASR are valid only for a short time t_{valid} (assuming memories with 45 ns read cycle time and a 100 MHz shift clock rate, t_{valid} amounts to about 40 ns).

During this time slot the data must be read into the first latch stages of both DASRs by the strobe high pulse. This could be reached by connecting the $\overline{W}$ output of the second DASR to the strobe inputs and adjusting the required delay time by delaying $\overline{W}$ via V0, V1 (in this case $\overline{W}$ is delayed two shift clock periods). The data are then received into the next latch stage by an internal clock. Afterwards they are shifted out serially with the shift clock rate. To avoid bus contention, when the memories are written by the microcontroller, the outputs of the counter must be set to the high impedance state.

The control inputs of the memories, $\overline{CS}$ and $\overline{W}$, must be provided by the system processor or could be easily derived from DASR signals

Waveform Generation System

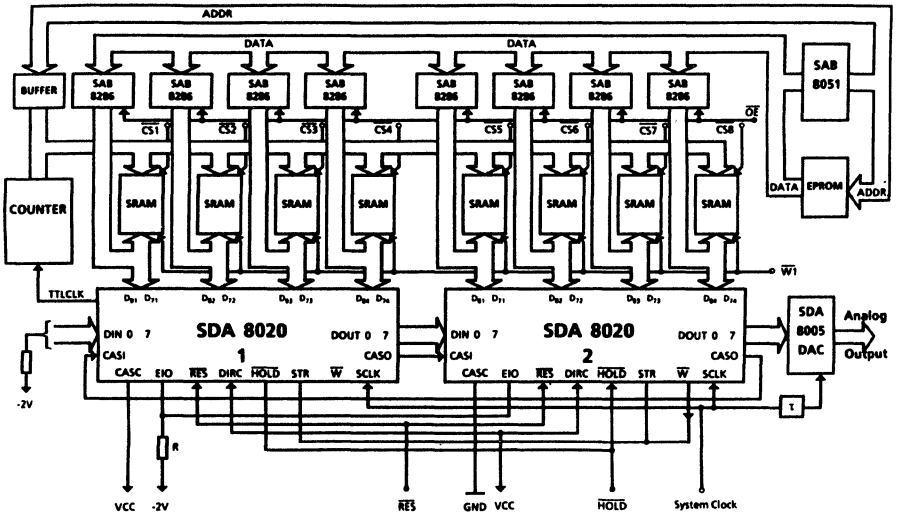


Figure 12

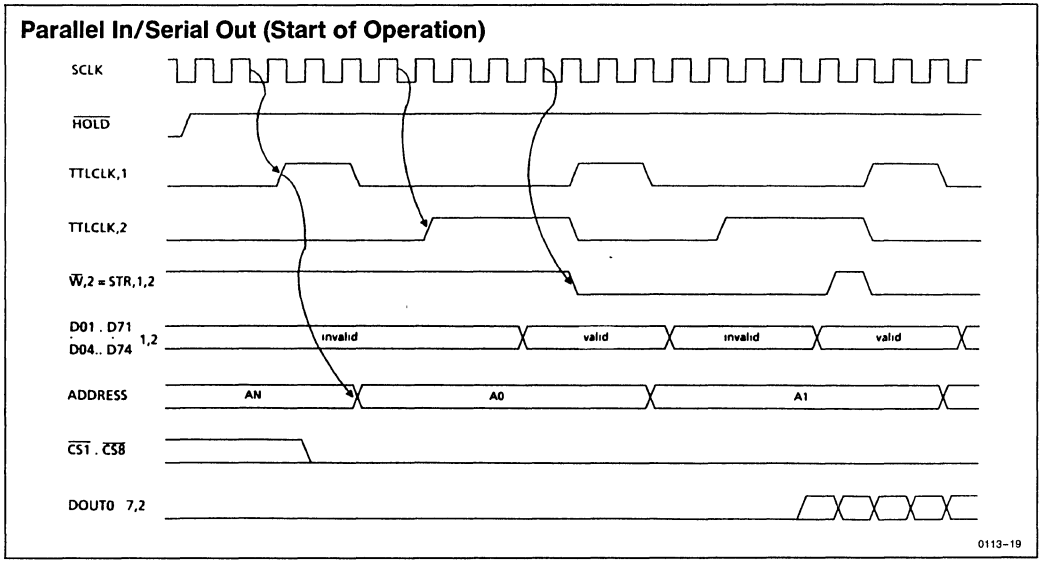

Parallel In/Serial Out (Start of Operation)
SCLK
HOLD
TTLCLK,1
TTLCLK,2
W,2 = STR,1,2
D01 . D71
D04.. D74 1,2
invalid
valid
invalid
valid
ADDRESS
AN
A0
A1
CS1 . CS8
DOUT0 7,2
0113-19

Figure 13

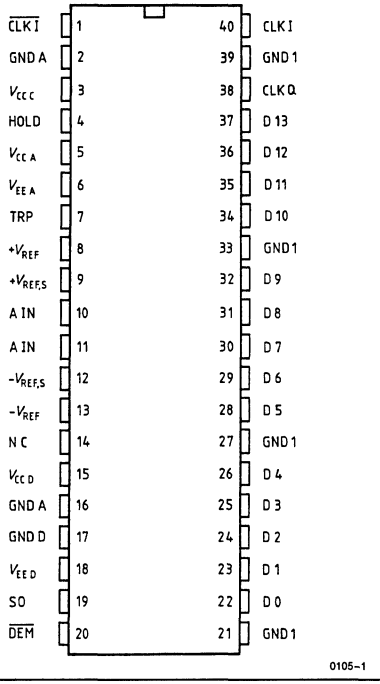
SIEMENS

Preliminary

SDA 8200
6 Bit 300 MHz A/D Converter

- 300 MHz Conversion Rate
- 5.4 Eff. Bits (f_{analog} = 100 MHz)
- ±0.25 LSB Max. Linearity Error
- ±1V Input Voltage Range
- 12 pF Input Capacitance
- Optionally 2:1 Demultiplexed Output Data
- No Pipelining in "Transparent Mode"
- Data Ready Clock Output
- Overflow Output

Pin Configuration



0105–1

The SDA 8200 is an ultrafast A/D converter according to the parallel principle with a resolution of 6 bits, a guaranteed clock frequency of 300 MHz and high performance up to 150 MHz full scale inputs.

Block Diagram

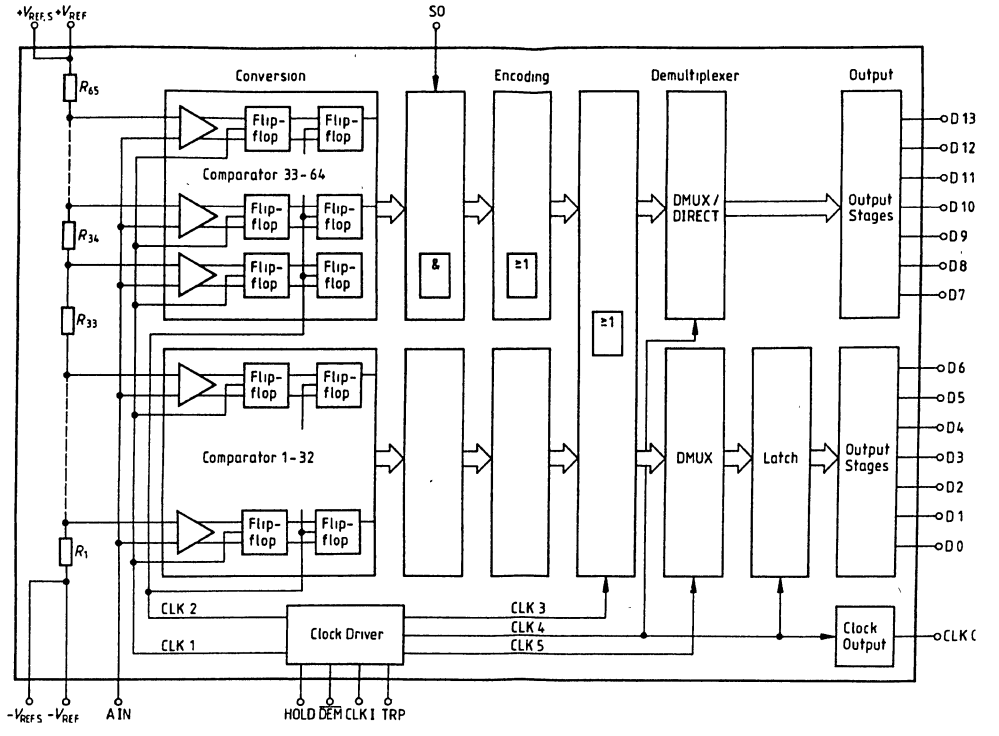


Figure 2

Pin Description

Pin	Name	Symbol	Description
10, 11	Analog Input	AIN	Input for the signal to be digitized. To lower parasitic inductance two pins are used for this input.
13, 12, 8, 9	Reference Inputs	$-V_{REF}$ $-V_{REF,S}$ $+V_{REF}$ $+V_{REF,S}$	Bottom and top of the reference-resistor-string. The inputs may either be used as sense and force for a Kelvin connection or connected in parallel to minimize parasitic resistance.
40, 1	Conversion Clock	CLKI, $\overline{\text{CLKI}}$	Every rising edge of a signal applied to CLKI initiates sampling of the analog signal. Either ECL (differential or single-ended) or sinewave clock inputs may be used.
38	Clock Output	CLKQ	Provides an ECL signal which can be used to control the takeover of the digital outputs into subsequent circuits (not available in the transparent mode). In the demultiplexing mode the frequency of CLKQ is half the sampling frequency (see "Modes of Operation").
22, 23, 24, 25, 26, 28, 29	Output Word 1	D0–D6	ECL outputs including overflow bit (D6) valid only in the demultiplexing mode. In this mode every first digital word of a pair of subsequent samples is delivered with a clock rate of half the sampling frequency. In the direct modes undefined data are shown at these outputs.
30, 31, 32, 34, 35, 36, 37	Output Word 2	D7–D13	ECL outputs (D13 overflow) delivering the second word of a pair in the demultiplexing mode. In the direct modes the digital data at these outputs appear with a clock rate equal to the sampling rate.
19	Set Overflow	SO	A logic H at this ECL input or strapping the pin to GNDD causes the overflow bit to be H and the data bits to be L when the analog signal exceeds the uppermost comparator threshold. If the pin is not connected or L is applied the data bits remain H in case of overflow.
20	Demultiplexing	DEM	Setting this pin to H or strapping it to GNDD sets the device into the direct mode.
7	Set Transparent	TRP	A logic H (or GNDD) at this input sets the device into the transparent mode (no pipelining). In this mode both DEM and HOLD input become ineffective. Besides, no clock output is provided.

Pin Description (Continued)

Pin	Name	Symbol	Description
4	Hold	HOLD	H active ECL input that immediately stops data transfer to the outputs (D0–D13) and inhibits the clock output. The last data word remains at the output and CLKQ is forced to low. In the direct mode the first valid output data together with the output clock appear one clock cycle after HOLD is released. In the demultiplexing mode clock and valid data appear after two conversion clock cycles with the first data word (corresponding to the first sampled value after HOLD is set to L) always shown at D0–D6. HOLD is inactive in the transparent mode.
5, 6, 2, 16, 15, 18, 17, 3	Analog Supply Digital Supply Clock Supply	$V_{CC\,A}$, $V_{EE\,A}$ GND A $V_{CC\,D}$, $V_{EE\,D}$ GND D $V_{CC\,C}$	Supply Voltages
21, 27, 33, 39	Output Ground	GND1	Return path for the current of the emitter followers in the ECL output stages.

3

Circuit Description

The A/D conversion is carried out in an array of 64 comparators connected in parallel to the analog input AIN. The signal is compared simultaneously with 64 equally spaced reference voltages provided by the resistor string R1–R65. With the rising edge of the conversion clock CLKI the result of the comparison is stored in the first comparator latch and afterwards passed to the second latch in a pipelining operation. Then the digital result of the comparison is pending at the comparators' output in a so-called thermometer code. Three subsequent encoding stages form the binary representation of the sampled value and a demultiplexer optionally divides the 300 MHz output data stream into two 150 MHz channels which are converted to ECL levels by two parallel output driver blocks. All clock signals for the pipelining and demultiplexing stages are formed internally by a clock driver circuit connected to the external conversion clock via CLKI. A clock signal for taking over the output data into subsequent circuitry is provided at CLKQ. If, however, the pipelined operation is disadvantageous (e.g. in subranging converter applications), all internal latches following the comparators may be set transparent via the programming input TRP. So any encode command directly causes the appearance of the respective output data after a short delay.

Clock Input (CLKI)

The clock inputs are designed to be driven differentially with ECL levels (Figure 3a). Since $\overline{\text{CLKI}}$ is internally biased to −1.32V, it is possible to use CLKI single-ended, too. With this configuration a bypass capacitor from CLKI to GNDC is recommended.

In this case the clock has to be stable with regard to the internal reference voltage to ensure the specified timing ($t_{WH,CLKI}$, $t_{WL,CLKI}$) over the operating range. For continuously applied input clock the configuration shown in Figure 3b is recommended. A capacitively coupled sinewave clock input (typ. 300 mV_{pp}) can then be employed without degradation in performance (Figure 3c).

Analog and Reference Inputs

The input voltage range is determined by the voltages applied to the top ($+V_{REF}$) and bottom ($-V_{REF}$) of the resistor string. Two pins for each voltage allow a Kelvin connection (sense, force) if highest precision is required. Otherwise the parallel connection of these pins ensures low parasitic resistances. The analog input can be driven from a customary 50Ω source since the input capacitance is a very low 12 pF, independent of input voltage,

and the input voltage range may be set symmetric to ground.

Supply System

The supply system breaks down into three parts. The analog supply $V_{CC\,A}$, $V_{EE\,A}$ is connected to the first comparator stages, the digital supply $V_{CC\,D}$, $V_{EE\,D}$ serves for encoding, demultiplexer and output stages and a special clock supply $V_{CC\,C}$ is provided to separate the high and noisy driver currents from the other supply systems. Additionally a separate return path for the currents of the output emitter followers is established via GND1.

Modes of Operation

The analog signal is sampled with every rising edge of the clock signal CLKI. By programming the TRP and $\overline{DEM}$ inputs three different output modes can be chosen:

a) Direct modes (Figure 4):

The output data appear at the outputs D7–D13 with a word rate equal to the sampling rate.

The logic state of the outputs D0–D6 is not defined.

One of two submodes can be chosen:

(I) Normal Mode (TRP low, $\overline{DEM}$ high)

Due to internal pipelining the output data appear one clock cycle after the rising edge of CLKI (sampling moment). CLKQ delivers a clock signal with the same frequency as CLKI.

(II) Transparent Mode (TRP high)

After a sampling command the associated output data appear directly with a delay of less than 7 ns. No output clock is available.

b) Demultiplexing mode (TRP low, $\overline{DEM}$ low; Figure 5)

The output words corresponding to two subsequent samples appear simultaneously at the outputs D0–D6 and D7–D13, respectively, with half the clockrate of the conversion clock CLKI. After a HOLD pulse the word belonging to the first sample is always shown at D0–D6 and the delay between the first sample and output is two cycles of the conversion clock CLKI. At CLKQ a clock signal with half the frequency of the conversion clock, synchronous to the output data, is provided.

In all modes the output format in the overflow status can be programmed via the SO input. Setting SO to H causes the overflow bits (D6 and D13, respectively) to remain H and the data bits (D0–D5 and D7–D12, respectively) to go to L when the analog signal exceeds the threshold of comparator 64. If SO is set to L or not connected all data and overflow bits remain H in case of overflow (Figure 6). This enables easy cascading of two SDA 8200 to a 7 bit A/D-system by connecting them as shown in Figure 7 and strapping the SO input of the lower one to H.

The HOLD input allows to stop the digital data stream of the output and to restart with defined output conditions. It is disabled in the transparent mode.

Absolute Maximum Ratings*

Positive Supply Voltages
($V_{CC\,A}$), ($V_{CC\,D}$), ($V_{CC\,C}$) ..... −0.3V to +6.0V

Negative Supply Voltages
($V_{EE\,A}$), ($V_{EE\,D}$) ..... −6.0V to +0.3V

Analog Input Voltages
($+V_{REF}$), ($-V_{REF}$), (V_{AIN}) ... −2.5V(1) to +1.5V

Digital Input Voltages
(V_{CLKI}), ($V_{\overline{CLKI}}$), (V_{DEM}),
(V_{SO}), (V_{TRP}) ..... −3.0V to +0.3V

Output Current (I_{D0}–I_{D13}) ..... 20 mA

Junction Temperature (T_j) ..... 125°C

Ambient Temperature
(without Dissipator) (T_A) ..... 50°C

Storage Temperature (T_{stg}) ..... 125°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Resistances

Junction-Air (without Dissipator) ..... 45 K/W

Note:
1. Reference voltages below −2V must not be applied without the negative supply voltage.

Characteristics

$V_{CC\ A}$, $V_{CC\ D}$, $V_{CC\ C}$ = 5V ±5%, $V_{EE\ A}$, $V_{EE\ D}$ = −4.5V ±5%, 25°C < T_j < 125°C

Parameter	Symbol	Conditions	Limits			Units
			Min	Typ	Max	
Supply						
Positive Supply Current	$I_{VCC\ A}$ $I_{VCC\ D}$ $I_{VCC\ C}$			50 65 35		mA mA mA
Negative Supply Current	$I_{VEE\ A}$ $I_{VEE\ D}$			45 125		mA mA
Power Dissipation	P			1.5	1.8	W
Permissible Supply	ΔV_{CC}				100	mV
Voltage Difference	ΔV_{EE}					
Analog Section **Signal Input**						
Voltage Range	V_{AIN}		−2		1	V
Max. Input Current (V_{AIN} = $+V_{REF}$)	I_{AIN}			500	700	µA
Input Capacitance	C_I			12		pF
Reference Inputs						
Reference Voltage(1)	$+V_{REF}$		−2		1	V
Reference Resistance	R_R			120		Ω
Temperature Coefficient of Reference Resistor	TC			1.7		$10^{-3/K}$
Digital Section **Logic Levels**						
Input H Voltage(2)	V_{IH}		−1.165			V
Input L Voltage(2)	V_{IL}				−1.475	V
Output H Voltage(3)	V_{QH}	R_L = 100Ω	−1.025		−0.88	V
Output L Voltage(3)	V_{QL}	R_L = 100Ω	−1.810		−1.620	V
Clock Inputs(4)						
Input Current	I_{CLKI}				20	µA
Maximum Clock Frequency	$f_{c,max}$		300	350		MHz
Aperture Delay	t_A			7		ns
Hold Time	$t_{WH,CLKI}$		1.2			ns
Strobe Time	$t_{WL,CLKI}$		1.2			ns

3

Characteristics (Continued)

$V_{CC\ A}$, $V_{CC\ D}$, $V_{CC\ C}$ = 5V ±5%, $V_{EE\ A}$, $V_{EE\ D}$ = −4.5V ±5%, 25°C < T_j < 125°C

Parameter	Symbol	Conditions	Limits			Units
			Min	Typ	Max	
Digital Section (Continued) **Programming Inputs**(2)						
Input H Current	I_{IH}			80		µA
Input L Current	I_{IL}			60		µA
Hold Input						
Setup Time	$t_{S,HOLD}$		0.5			ns
Release Time	$t_{r,HOLD}$		2			ns
High Pulse Width	$t_{W,HOLD}$		1			ns
Data Outputs(5) **Data Valid Range**						
Normal Mode	$t_{V,N}$	f_c = 250 MHz	3	3.5		ns
Transparent Mode	$t_{V,T}$	f_c = 250 MHz	2.5			ns
Demultiplexing Mode	$t_{V,D}$	f_c = 300 MHz	5	5.8		ns
Output Delay						
Normal Mode	$t_{d,N}$		0.5			ns
Transparent Mode	$t_{d,T}$				8	ns
Demultiplexing Mode	$t_{d,D}$		0			ns
Clock Output						
Maximum Frequency(6)	$f_{a,max}$			250		MHz
Clock Delay LH	t_{dLH}			6		ns
Clock Delay HL	t_{dHL}			5.5		ns

Notes:
1. $+V_{REF}$ has to be more positive than $-V_{REF}$.
2. Applies for DEM, SO, HOLD, TRP
3. Applies for CLKQ, D0–D13
4. See "Circuit Description"
5. Values refer to sinewave clock inputs (duty cycle 50%).
6. Has been chosen lower than maximum sampling frequency because at very high input clock rates the device should preferably be operated in the demultiplexing mode.

Conversion Characteristics

$V_{CC\ A}$, $V_{CC\ D}$, $V_{CC\ C}$ = 5V ±5%, $V_{EE\ A}$, $V_{EE\ D}$ = −4.5V ±5%, T_A = 25°C

Parameter	Symbol	Conditions	Limits			Units
			Min	Typ	Max	
Static Nonlinearity						
Integral Nonlinearity	INL				0.25	LSB
Differential Nonlinearity	DNL				0.25	LSB

Conversion Characteristics (Continued)

$V_{CC\ A}$, $V_{CC\ D}$, $V_{CC\ C}$ = 5V ±5%, $V_{EE\ A}$, $V_{EE\ D}$ = −4.5V ±5%, T_A = 25°C

Parameter	Symbol	Conditions	Limits			Units
			Min	Typ	Max	
Dynamic Performance(1)						
Large Signal Bandwidth	f_{3dB}			250		MHz
Effective Resolution(1)	b_{eff}	f_C = 300 MHz				
f_{AIN} = 10 MHz		V_{AIN} = 2 V_{pp}		5.9		Bit
f_{AIN} = 50 MHz			5.6	5.8		Bit
f_{AIN} = 100 MHz			5.3	5.4		Bit
f_{AIN} = 150 MHz				5.0		Bit
Signal-to-Noise Ratio(2)	SNR	f_C = 300 MHz				
f_{AIN} = 50 MHz		V_{AIN} = 2 V_{pp}	36	37.5		dB
f_{AIN} = 100 MHz			35	36		dB
f_{AIN} = 50 MHz		V_{AIN} = 1 V_{pp}		37		dB
f_{AIN} = 100 MHz				36		dB
Total Harmonic Distortion	THD	V_{AIN} = 2 V_{pp}				
f_{AIN} = 50 MHz				−44		dB
f_{AIN} = 100 MHz				−33		dB

Notes:
1. Measured in a 50Ω analog system at 300 MHz sampling rate (300 mV_{pp} sinewave clock).
2. Includes both noise and harmonic distortions.
3. Without the effect of harmonics; thus b_{eff}, SNR[dB] and THD[dB] are related by
$b_{eff} = (-10 \log (10^{-SNR/10} - 10^{THD/10}) - 1.8)/6$

Clock Input

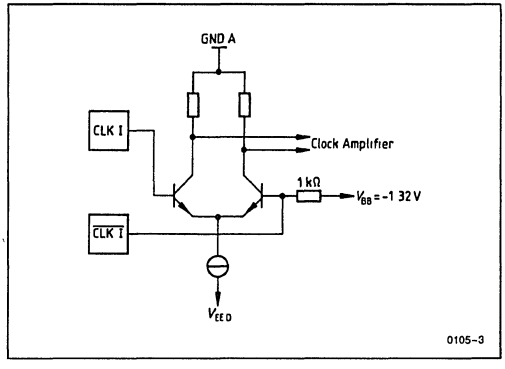


Figure 3a

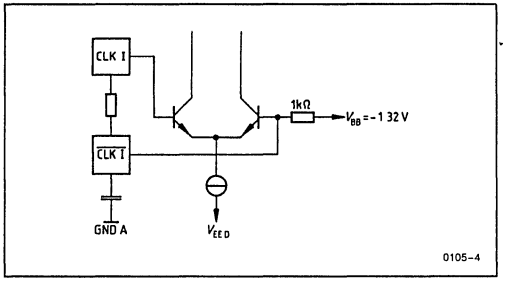


Figure 3b

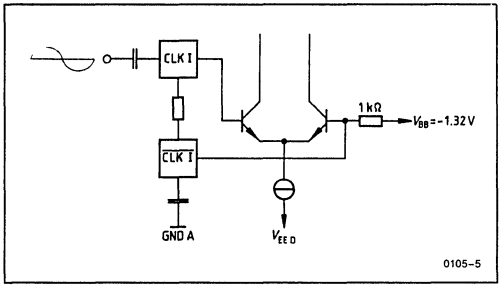
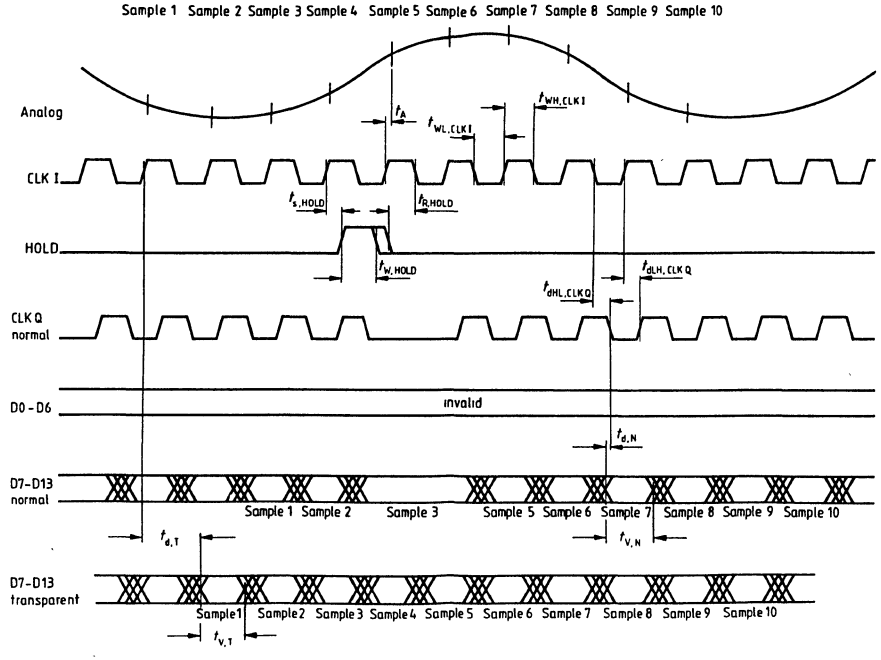


Figure 3c

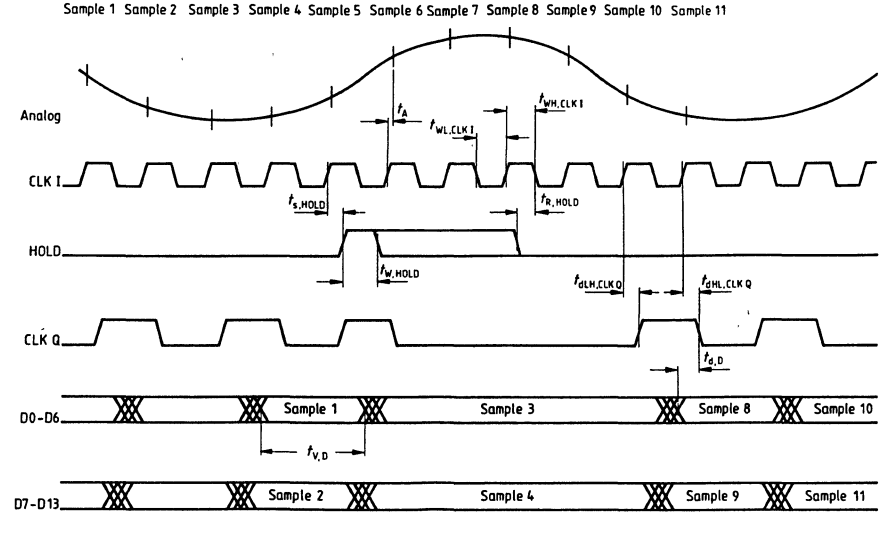
Timing Diagram Direct Modes



0105-6

Figure 4

Demultiplexing Mode

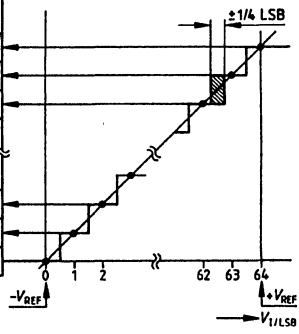


0105-7

Figure 5

Transfer Characteristic and Truth Table

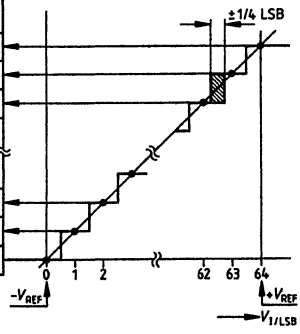
D6	D5	D4	D3	D2	D1	D0
H	H	H	H	H	H	H
L	H	H	H	H	H	H
L	H	H	H	H	H	L
≈						
L	L	L	L	L	H	L
L	L	L	L	L	L	H
L	L	L	L	L	L	L



0105-8

a) SO set to "L" or not connected

D6	D5	D4	D3	D2	D1	D0
H	L	L	L	L	L	L
L	H	H	H	H	H	H
L	H	H	H	H	H	L
≈						
L	L	L	L	L	H	L
L	L	L	L	L	L	H
L	L	L	L	L	L	L



0105-9

b) SO set to "H" or strapped to ground

Figure 6

Block Diagram of a 7 Bit A/D-System with Two SDA 8200

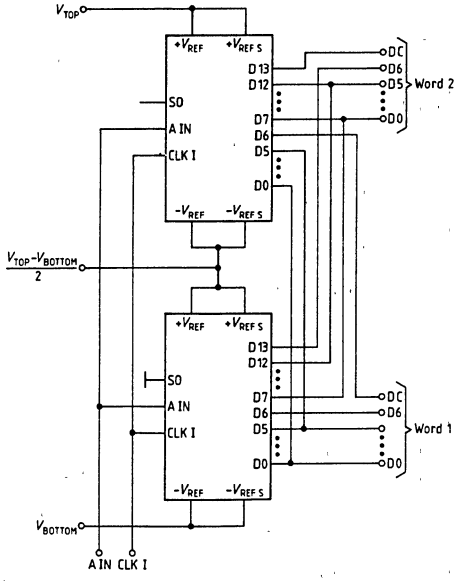
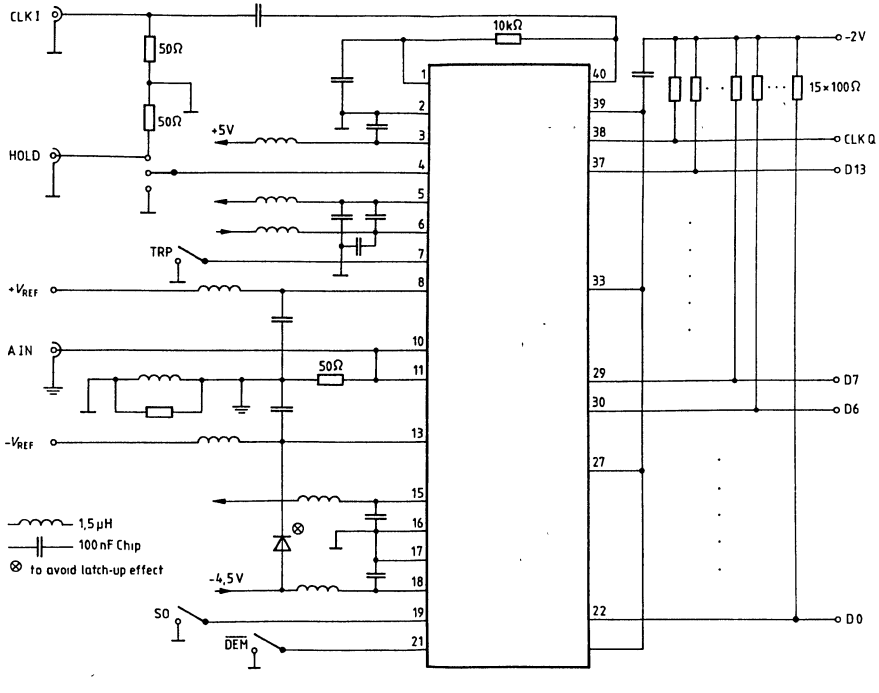


Figure 7

Test Circuit



Ordering Information

Type	Order Code	Package
SDA 8200	Q67100-Hxxxx	DIC 40

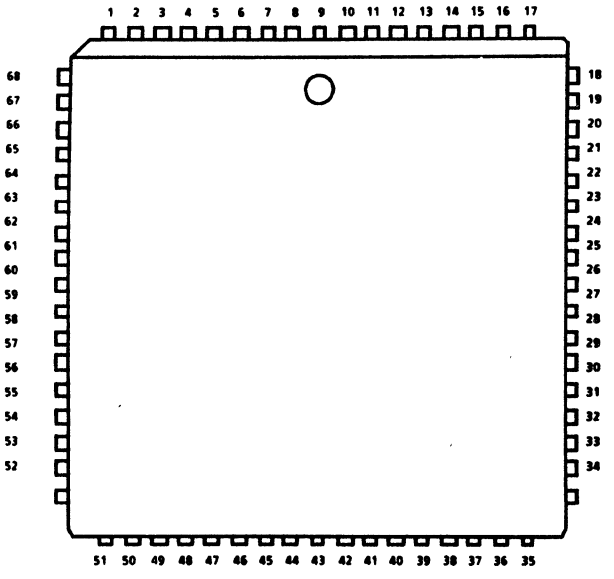
SIEMENS

Preliminary

SDA 8800
Data Acquisition Controller

- Controls HSDA Cache Memories with Sizes from 1 kByte to Several MBytes
- Supports Static CMOS RAMs
- Allows the Design of Data Acquisition and Data Transmission Systems
- Fully Register Programmable
- Compatible with SIEMENS HSDA Components
- Compatible with SIEMENS/INTEL 80xx, 80xxx and MOTOROLA 68xxx Microprocessors
- Supports 8-, 16- and 32-bit Data Bus Widths
- High Speed DMA Data Transfer Capability
- 16 bits Address Range for the Cache, Extendable to 20 bits
- Programmable Pre-/posttrigger Function
- 2 µm ACMOS Technology, PLCC 68 Package

Pin Configuration



The DACO SDA 8800 is the controller for High Speed Data Acquisition (HSDA) cache memories. Together with the Data Acquisition Shift Register (DASR) SDA 8020, fast 100 MHz caches with sizes in the range of 1 kByte up to several MBytes can be designed with static CMOS RAMs. The DACO makes the whole HSDA cache to behave like a microprocessor peripheral device. It handles autonomously the acquisition or transmission of data, and offers a variety of microprocessor access structures, including high speed DMA-based data transfers.

Block Diagram

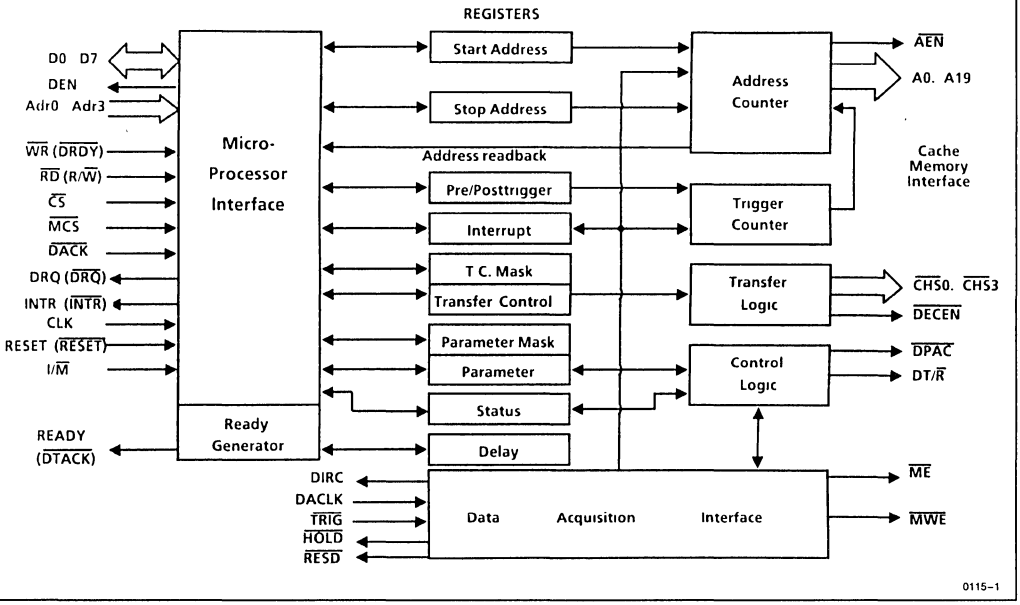


Figure 1

General Description

The Data Acquisition Controller SDA 8800, together with the Data Acquisition Shift Register (DASR) SDA 8020, provides a complete, highly integrated solution for the design of fast cache memories. The range of applications spans from DSO's, logic analyzers and transient recorders over waveform and pattern generators to radar and high resolution image processing systems, whereby the cache forms the front-end of the digital data processing unit.

The high flexibility of the HSDA system stems from its unique architecture. All the fast data handling functions are assigned to the DASR. This device can be arranged in serial, parallel and serial/parallel configurations according to the specific application requirements. With its ECL to TTL level conversion and speed reduction it minimizes the system's power consumption and communicates directly with the DACO.

The DACO SDA 8800 performs all the controlling functions of the HSDA system. It is a register programmable device suited to a large variety of applications and environments. The DACO can be strapped to interface SIEMENS/INTEL and MOTOROLA microprocessor systems. It makes the whole HSDA system to be viewed as a peripheral device to the microprocessor with communication links via interrupt and DMA request lines.

The DACO supports both systems with and without a DMA-controller by providing high DMA transfer rates as well as the memory-saving "Direct Processor Access" mode. The main part of the DACO for controlling the HSDA system are two 16-bit counters for the address generation and the trigger delay, which can be extended to 20-bit by internal prescalers. With these counters the DACO is also prepared to support future SRAM-types like the 1M x 4-bit, and provides a posttrigger delay range of at least 4M samples (with 1 DASR). Both counters can be operated up to 25 MHz, thus 100 MHz data acquisition or transmission systems can be implemented with 1 DASR.

Pin Definitions and Functions

Pin	I/O	Symbol	Function
1–4	I	Adr0–Adr3	Address lines to System Address Bus. These lines are used to select the appropriate registers when the DACO is in programming mode and to select the appropriate data channel in the DPAC mode.
61–68	I/O	D0–D7	8-bit data bus used to read from or write to an internal register of the DACO.
58	O	DEN	Data Enable signal, used as a transmit signal for an external data bus driver at the Di lines. Normally DEN is low.
47	I	I/$\overline{M}$	The I/$\overline{M}$ pin straps the DACO to an INTEL 80xxx or a MOTOROLA 68xxx environment.
57	I	$\overline{RD}$ (R/$\overline{W}$) (1)	Read strobe used to clock out the contents of an internal register or an HSDA-memory location. (The R/$\overline{W}$ line determines the direction of the data transfer).
56	I (O)	$\overline{WR}$ ($\overline{DRDY}$) (1)	Write strobe used to write data to an internal register or an HSDA-memory location. (Ready for single cycle DMA transfers.)
55	I	$\overline{CS}$	Chip select for programming cycles.
54	I	$\overline{MCS}$	Memory chip select line to get access to any memory location in the DPAC mode.
48	I	CLK	Clock input of the DACO. The system clock should be used to drive this input preferably.
51	O	READY ($\overline{DTACK}$) (1)	Output of the internal READY or DTACK generator for all HSDA-memory accesses.
5	O	$\overline{DPAC}$	Direct processor access signal. Serves as an output enable to the address latch in the DPAC-mode.
6	O	DT/$\overline{R}$	Data transmit/receive, used to set the direction of the data flow through the data latches.
8, 11–13	O	$\overline{CHS0}$–$\overline{CHS3}$	Channel select lines for the data latches and the cache memories, applied either directly or via an address decoder depending on the data bus width and the number of DASR's in the HSDA-system.
7	O	$\overline{DECEN}$	Decoder enable line for an address decoder attached to the $\overline{CHSi}$ signals.
25–21, 37–33, 19–15, 31–27	O	A0–A19	Address output bus for the HSDA-memory. In DPAC-mode these lines are in a tristate condition.
39	O	$\overline{ME}$	Memory enable signal providing the selection of the whole HSDA-memory for the DT-mode and DMA-read mode.
14	O	$\overline{AEN}$	Address enable for an external address buffer driver.
38	O	$\overline{MWE}$	Memory write enable signal, is tied low in all cases that require a write access to the HSDA-memory.
41	I	DACLK	Data acquisition clock input, used to clock out consecutive addresses for the HSDA-memory when the DACO is in the DA or DT mode.
45	O	$\overline{HOLD}$	$\overline{HOLD}$ line, brings the DASR's into an inactive condition, i.e. in the DMA- and DPAC-modes.
40	O	DIRC	Direction pin, determines the data transfer direction of the HSDA system (low: DA, high: DT).
46	I	$\overline{TRIG}$	Trigger input. Starts the operation of the trigger counter.

Pin Definitions and Functions (Continued)

Pin	I/O	Symbol	Function
52	O	DRQ ($\overline{DRQ}$)(1)	DMA-request line. It is activated in order to obtain a DMA service. The DRQ pulse width is determined by the EOD-bit of the transfer control register.
53	I	$\overline{DACK}$	DMA-acknowledge, used as a chip select for DMA transfers.
50	O	INTR ($\overline{INTR}$)	Interrupt request line. It is reset at the first CPU access to the DACO's interrupt register.
49	I	RESET ($\overline{RESET}$)	Reset input. Brings the DACO in the idle mode. All counters and registers are cleared.
44	O	$\overline{RESD}$	Reset to DASR, issued prior to the release of the $\overline{HOLD}$ signal at the beginning of a data acquisition or transmission process.
10, 26, 43, 60	I	VDD	Positive power supply (+5V).
9, 20, 32, 42, 59	I	GND	Negative power supply (0V).

Note:
1. Pin definition for MOTOROLA 68xxx systems I/$\overline{M}$ strapped low).

Functional Overview

The DACO can be divided into the data acquisition, the cache memory and the microprocessor interfaces as shown in the block diagram of Figure 1. All transactions are controlled by the register block of the device, which can be read or written via the microprocessor interface according to the address selection summarized in Table 1.

The DACO can be operated in 4 distinctive modes which can be selected by programming cycles:

(1) Data acquisition (DA)/Data transmission (DT)

(2) DMA-transfer/Interrupt

(3) DPAC (Direct processor access)

(4) Idle

All possible mode transitions are depicted on the state diagram of Figure 2.

Modes (1) to (4) are characterized by two bits (S0, S1) of the status register. The data flow direction is set by the DIR bit.

As can be seen from the state diagram, all modes can be entered or left under the control of the microprocessor by setting the status bits appropriately. Additional mode transitions may occur either if a task is finished or if a new task has to be started automatically. The latter cases may be chosen optionally in order to minimize the processor's intervention. The DACO locks internal and external requests for mode transitions mutually in order to avoid time race conditions. However, external mode transitions requests may only be delayed but not suppressed by internal ones.

Microprocessor Interface

The DACO offers interfaces to SIEMENS/INTEL and MOTOROLA microprocessor systems, adjustable by the strap pin I/$\overline{M}$. The interfaces provide an easy to use connection to all important microprocessors of both families. Low cost systems with only few external circuits as well as high performance systems allowing for high data transfer rates can be implemented.

Although the DACO has an asynchronous interface it needs a clock (CLK) in order to generate a lot of correctly timed sequences. The CLK signal needs not necessarily be synchronous to the processors system clock but it is recommended to establish a constant phase relationship between these two clocks in order to avoid a lot of timing uncertainties.

DACO State Diagram

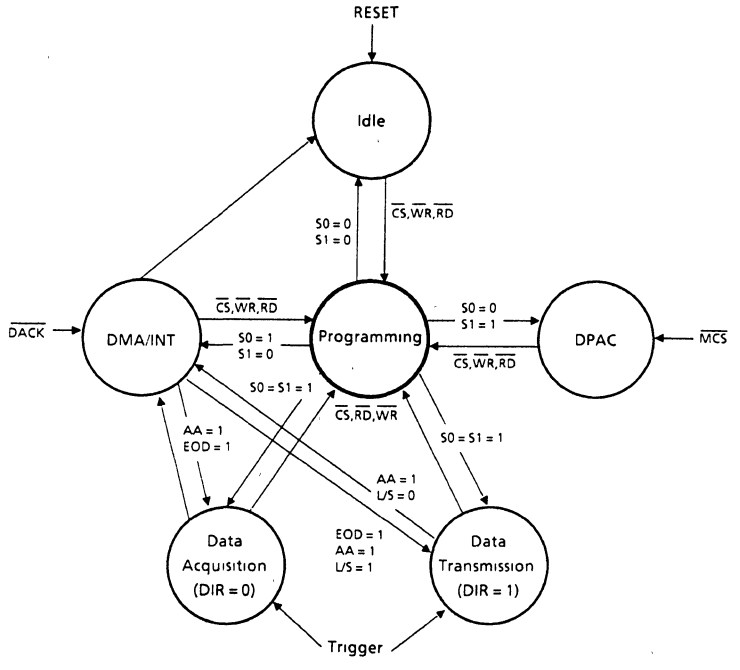


Figure 2

SIEMENS/INTEL Interface

With its I/$\overline{M}$ pin strapped high, the DACO's MP-interface directly fits to 8086 (8088), 80186 (80188) and 80286 systems. Bus transfers should operate without wait states, if the HSDA memory is fast enough. If not, the DACO generates a programmable READY signal.

The chip select signals ($\overline{CS}$, $\overline{MCS}$ and $\overline{DACK}$) serve as enable inputs for the microprocessor interface and have to be asserted throughout a whole bus cycle or throughout a series of bus cycles. The data transfers are controlled by the $\overline{RD}$ and $\overline{WR}$ strobes of the processor system.

READY is an open-drain output. If no wait states are required (programmed value = 0), READY remains in a stable high-impedance state. If it's programmed to 1, 2 or 3 the DACO pulls the READY output low for the corresponding number of CLK periods.

MOTOROLA Interface

The DACO has an asynchronous interface for 68000 systems when I/$\overline{M}$ is strapped low. Bus transfers without wait states should be possible in 68000, 68008, 68010 and 68020 systems, if the HSDA memory is fast enough.

The DACO latches R/$\overline{W}$ and Adri at each falling edge of $\overline{CS}$, $\overline{MCS}$ and $\overline{DACK}$. This requires that R/$\overline{W}$ and Adri are stable just at the beginning of the bus cycle with some setup and hold times to the select signal.

$\overline{DTACK}$ is an open-drain output with an active dynamic pullup which can be programmed to delay its falling edge for 1 to 3 CLK periods.

READY (DTACK) Generation

The DACO provides a programmable READY or DTACK Generator for bus access to the HSDA memory in order to insert a sufficient number of wait states in the processor's bus cycle. This allows to use various types of memories and access structures without the need for additional hardware. The READY ($\overline{DTACK}$) line may be delayed by 1 . . . 3 CLK periods, depending on the delay register value.

Bus access to the internal registers should not require any wait states with all popular microprocessors, thus the DACO provides the READY ($\overline{DTACK}$) signal without any delay in programming cycles.

The DACO provides two insertion mode:

1) Insertion of wait states into every DMA or DPAC bus cycle. The number of the wait states can be programmed via the RDY0 and RDY1 bits of the delay register.

2) Insertion of wait states at address transitions only. This dynamic insertion mode which can be applied in DMA based systems only reduces the number of wait states significantly. When reading the HSDA memory all SRAMs are enabled continuously. As a consequence wait states need only be inserted in the first bus cycles after each address transition until all the memories data become valid (see Figure 3).

On the contrary, when writing the memories, wait states are necessary only in advance of each address transition—provided that data latches form the connection between data bus and memories, so that all memories can be written at once (see Figure 4).

The number of wait states can be programmed via the RDA0 and RDA1 bits of the delay register (See: Application examples: How to use slow SRAMs).

If both, the RDY and RDA delays are set the DACO will apply RDA to each bus cycle at address transitions and RDY to all the remaining bus cycles accessing the HSDA memory. Thus RDA has to be programmed to 0 (then it is ignored) or to a value greater than RDY.

Programming Cycles

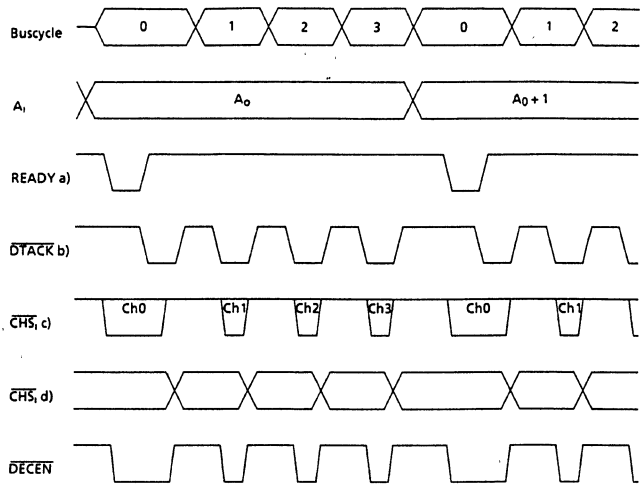
Programming cycles can be initialized from each mode at any time by read or write accesses to the DACO via its microprocessor interface. In general all changes of the register contents will affect the operation of the DACO immediately.

If the DACO is in DA or DT mode, programming cycles may be executed without interrupting the DA/DT process, as far as no relevant parameters are changed.

Note:
Each microprocessor write access to the status register effects immediately a termination of the current operation mode and the DACO enters into the programmed mode via the idle mode. When changes of the status bits occur, e.g. at the end of a DA/DT-process or via programming, the DACO disables further programming of the status bits for 8 CLK periods.

The programming of single bits of the parameter and the transfer control registers can be done very easily by the use of the corresponding mask registers. If a mask bit is set (high) the corresponding bit will not be changed and vice versa. Thus additional read cycles and bit manipulations by the microprocessor can be avoided.

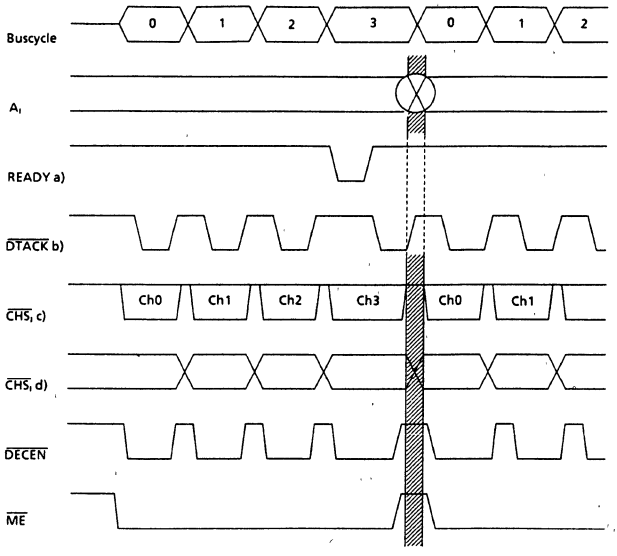
Dynamical Wait State Insertion (Acquisition System—DMA Read from DACO)



a) for IAPX systems
b) for MOTOROLA systems
c) 4 channels systems (1 DASR)
d) more than 4 channels, with address decoder

Figure 3

Dynamical Wait State Insertion (Latched Data Transmission System—DMA Write to DACO)



a) for IAPX systems
b) for MOTOROLA systems
c) 4 channels systems (1 DASR)
d) more than 4 channels, with address decoder

Figure 4

Idle Mode

In the idle mode the DACO is in a "do nothing" condition. It is entered at a hardware reset, a software reset (S0 = S1 = 0) or after finishing a DMA process according to the state diagram of Figure 2. When the idle mode is entered via a hardware reset, all counters and registers of the DACO are set to zero. However, if the idle mode is entered via software, the contents of the counters and registers will not change, the output lines with exception of INTR will be switched to the inactive state and D0 ... D7 will be set to input. It is recommended to program the DACO in the idle mode only and start the next transaction by changing the status bits in the last programming cycle.

The DACO changes from one operation mode to another always via the idle mode.

Data Acquisition/Transmission Mode

In the data acquisition/transmission mode the DACO will activate the HSDA-system. It is characterized by both status bits being set. The DACO can distinguish data acquisition from data transmission by the value of the DIR bit of the status register. Each acquisition/transmission process starts at the start address A_0.

Two operating modes, depending on the L/S bit of the status register, are supported (see Figure 5):

— Loop mode

— Start/stop mode

Depending whether the start/stop or the loop mode is used, the trigger input accommodates for starting or stopping the DA/DT process, respectively. In DA systems, both the pre- and posttrigger function can be provided in the loop mode only. Thus, the loop mode will be preferred for DSO or Logic Analyzer applications. The start/stop mode can be regarded as a "single shot" with potential, but not exclusive applications in the field of arbitrary waveform generation or other DT systems. It provides the posttrigger feature only.

Trigger Counter

The trigger counter is loaded with the trigger register contents when entering the DA/DT mode. The external trigger input is sampled at the positive edge of the DACLK if the DACLK is active or level-triggered asynchronously if not. When $\overline{TRIG}$ is sampled low, the internal 16-bit trigger counter, which was set to the predefined value from the pre-/posttrigger registers up to now, is started. At each DACLK leading edge the trigger counter is decremented by 1. By

reaching 0000H, the DT/DA process is started or stopped and the trigger counter is reloaded. An extended posttrigger range can be chosen by setting the EP-(Extended Posttrigger) bit of the status register. With this extension the DACO provides a posttrigger range of 1 million DACLK periods! In the DA loop mode the trigger recognition circuit is sensitive to the falling $\overline{TRIG}$ edge. The DACO assures that the whole active memory range is filled up with data by gating the trigger input during the first loop (see Figure 5b). The trigger counter is not retriggerable. If a trigger events the DACO is insensitive to further triggering until the current operation cycle is finished.

Address Counter

The address counter generally is loaded with A_o when entering the DA/DT or DMA/INT mode. As an exception the content of the counter is maintained over DA-loop mode to DMA transitions. At each data acquisition or data transmission process, a sequence of consecutive addresses is clocked out of the DACO by each DACLK leading edge. The address range is defined by the current values of the start and stop address A_o and A_n, respectively. With its fully programmable 16-bit address counter, the DACO can process up to 65.536 groups of (parallel) samples. Also, Ao and An may define an address range between any two address locations.

Optionally, a 4-bit prescaler can extend the address range to 20-bit when the Extended Address (EA) bit of the parameter register is set. In this configuration Ao and An can be set to each 16th address location, i.e., the prescaler is always set to 0H and compared to FH. The full 20-bit counter value can be read via the virtual address readback registers (see Table 1).

Note:
If the programmed stop address equals the programmed start address the whole memory range will be passed through. Furthermore, setting the stop address one or two addresses higher than the start address is forbidden.

DMA/INT-Mode

In the DMA/INT-mode the status bits S0, S1 of the DACO have to be set to 1 and 0, respectively. This can be done either by programming the appropriate value, or by entering the DMA/INT-mode automatically after a DA/DT process has been completed. In this case the status bits are set internally.

When entering the DMA/INT-mode, the DACO raises its DRQ line in order to signal the DMA-controller that it requires a DMA service. The EOD bit of the transfer control register controls the activation time of the DRQ line, hence source and destination synchronized and unsynchronized DMA transfers can be implemented. When high, DRQ is activated throughout the complete DMA transfer of all data within the range defined by the start and stop address. In this case the DACO controls the length of the DMA transfer. When low, DRQ is deactivated in the first DMA transfer cycle. The DRQ signal is cleared also when the DMA/INT mode is left.

The INTR line is activated in order to request for programming cycles after some DMA sequences whose length are controlled by the DACO (see Operational Description and Table 4). If the INT bit of the parameter register (see Tables 2, 3) is set, the DACO will assert INTR pulses together with DRQ for all applications where an interrupt to the CPU should be issued after DA/DT in order to obtain any kind of service, for example DPAC. In general, the INT bit will be set in systems without a DMA controller, because the DRQ signal cannot be used there. Additional INTR pulses are issued at some error conditions. At any time when INTR is asserted, DACO sets a bit of the interrupt register characterizing the exact reason of the interrupt (see Table 3c). The INTR signal as well as the INT-register itself will be cleared by the first read cycle accessing the INT-register.

For DMA transfers the cache memory data are accessed by read-or write cycles when $\overline{DACK}$ is asserted. Note, that the DIR bit has to be set in accordance with the direction of the data transfer, otherwise an INT7 will occur. If the SC-(Single cycle) bit is set, the $\overline{RD}$ and $\overline{WR}$ lines are interchanged internally. In 68xxx systems, the R/$\overline{W}$ line is interpreted inversly and no $\overline{DTACK}$ but the $\overline{DRDY}$ signal is issued. The DACO provides all signals needed for the transfer of data between the system data bus and the HSDA memory, regardless of the data bus width. 8-, 16- and 32-bit data buses can be supported by programming the BW0 and BW1 bits of the transfer control register appropriately. In the same way the number of DASR's in the system has to be adjusted correctly. On RESET, the DACO is programmed for 8-bit data buses and 1 DASR.

In a DMA transfer cycle, the DACO will continuously apply addresses and channel select signals to the HSDA memory in order to maintain the correct order of the transferred data. Normally, the DACO will transfer the data in ascending order, starting with channel 0 at the starting address. However, when the DACO changes from the DA loop mode to the DMA mode automatically, it will start transfers at the address that contains the "oldest" data (Ak) as it is shown in Figure 6.

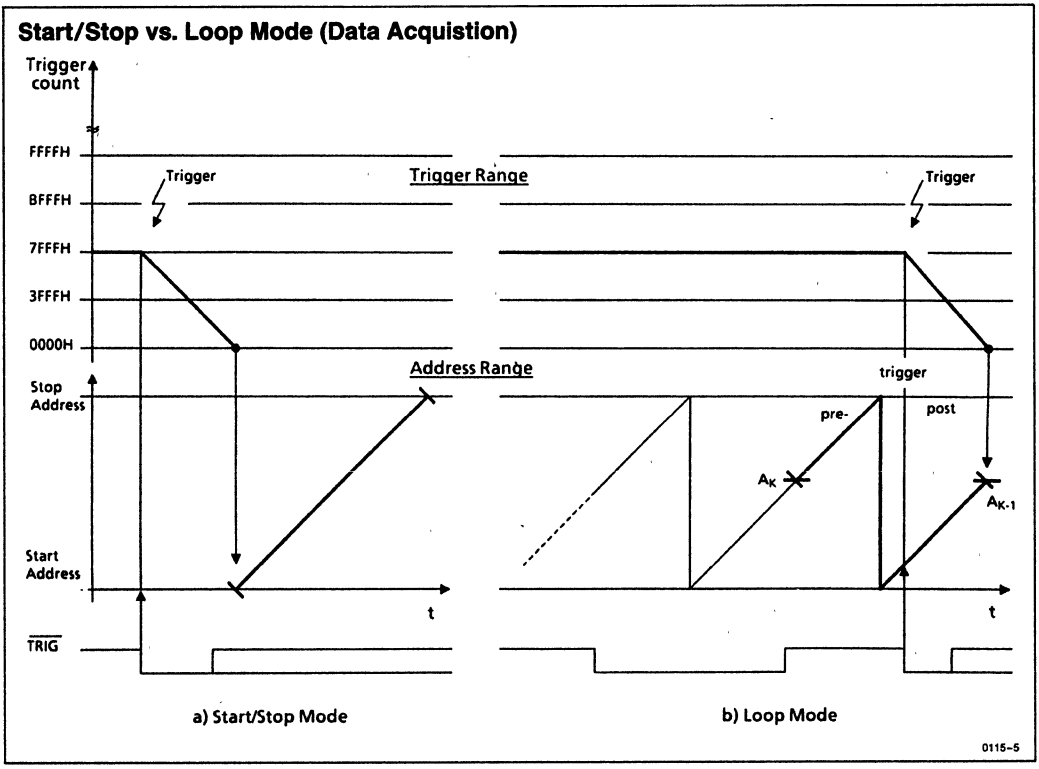


Figure 5

DPAC Mode

The direct processor access mode is mainly important for low end HSDA systems. In this mode the fast HSDA memory can be made part of the system memory temporarily. The DPAC-mode can be entered by programming the DACO status bits S0, S1 to 0, 1. When entered, the DACO will activate its $\overline{\text{DPAC}}$ line and tristates its cache memory address bus in order to allow the processor to access the memory via its own address bus. If an external address buffer is used, its drivers can be tristated by the $\overline{\text{AEN}}$ line of the DACO. DPAC cycles have to be performed via the normal data, address and control buses of the processor and the DACO has to be addressed by its $\overline{\text{MCS}}$ (memory chip select) line.

In DPAC mode, the DACO automatically uses the required address lines and, depending on the system configuration, provides the correct channel select signals at its $\overline{\text{CHSi}}$ and $\overline{\text{DECEN}}$ outputs (see Tables 5, 6, 7). For example, if the system is equipped when an 8-bit wide data bus and 1 DASR, the DACO uses the lowest two address lines (A0, A1) to select 1 of the 4 channels of the HSDA system to be accessed.

By using the DPAC mode, the processor can make any modification of the data in the HSDA memory and, after its completion, return to a DT/DA cycle again. Then the DACO has the complete control of the HSDA system and the processor can perform other tasks with its remaining system memory simultaneously. Note, however, that the DIR bit has to be set in accordance with the direction of the data transfer, otherwise an INT7 will occur.

Operational Description

Bus Operation

The DACO provides an asynchronous interface to 80xxx, 80xx and 68xxx systems strapped by I/$\overline{\text{M}}$. It is addressed via CS for programming, via $\overline{\text{DACK}}$ for DMA transfers and via $\overline{\text{MCS}}$ for DPAC.

DMA Transfer for the Loop Mode

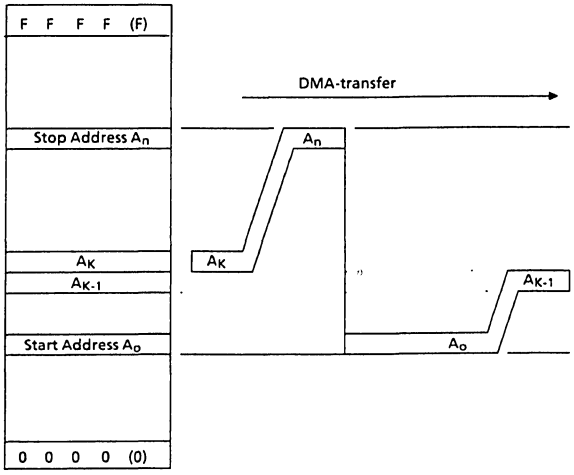


Figure 6

After RESET, the DACO first has to be programmed for its specific task. This requires a number of write operations to its internal registers. It is recommended to perform this programming sequence from the idle mode (S0 = S1 = 0) and alter the status bits by the last write command.

Note:
The DACO will accept programming bus cycles from any operating mode, however, it will accept DMA or DPAC bus cycles in the corresponding mode only.

Data Acquisition

In data acquisition systems, normally the DA mode will be entered after programming. In the start/stop mode (L/S = 0), the DACO will enter a DA waiting state. It continues to activate its $\overline{\text{HOLD}}$ line, thereby keeping the clock system of the DASR disabled and expects to receive a trigger pulse. Upon this event it releases its $\overline{\text{HOLD}}$ line. As a consequence DACLK will become active and start to decrement the trigger counter. By reaching 0000H, it starts the address counter and the data acquisition process will take place by writing data to the HSDA memory in the address range as previously defined by the start and stop addresses. This sequence guarantees a virtually constant time delay from the trigger event to the stored data range. This is important for time critical applications.

In the loop mode (L/S = 1) the trigger pulse is sampled by the positive DACLK edge. Thus an inherent time uncertainty between 4 and 16 samples is introduced into the delay from the trigger event to the stored data range according to the DACLK period. On the other hand, the pretrigger characteristics can be realized in the loop mode only. As a consequence it might be necessary to measure the trigger offset with respect to the DACLK by a fast external hardware and correct it appropriately by the microprocessor system for all these systems that require the pretrigger and cannot tolerate the time uncertainty.

According to Table 4a six different operating sequences may be chosen by setting the AA, EOD and L/S bits for DMA based systems. These operational sequences also can be seen from the state diagram of Figure 2. With low performance systems, the DPAC mode may be the preferrable choice for further data processing. In this case, all sequences have to be performed via programming according to Figure 2.

DMA based systems need some more detailed evaluations.

In all sequences the DACO will activate its DRQ line when entering a DMA cycle. The length of the DRQ pulse is determined by the EOD bit. Additionally the DACO can assert its INTR line together with DRQ for all sequences but sequences 3 and 4 in order to support easy communication with the processor in DPAC based systems if the INT bit is set. In the sequences 3 and 4 (characterized by AA = 0 and EOD = 1) the INTR line is issued when entering the

idle mode after a source synchronized DMA operation in order to signal the processor the end of the sequence.

Data Transmission

In data transmission systems the HSDA memory usually has to be loaded after the initial programming sequence. This can be done in the DPAC mode or in the DMA mode. In systems employing DPAC all mode transitions have to be performed via programming, according to Figure 2. DMA based systems allow for additional mode transitions. All possible operational sequences that can be chosen by the AA, EOD and L/S bits are summarized in Table 4b.

Generally, it is anticipated that the beginning of the data transmission process has to be exactly controlled. For this reason a DT waiting state is provided in all operational sequences. When entering this state the DACO releases the $\overline{\text{HOLD}}$ line but provides the start address at its address port until a trigger has occurred and the trigger counter is decremented to 0000H. Additionally, all operational sequences but sequence 8 (AA = EOD = L/S = 1) enter the idle mode before DT in order to avoid unintended DT processes.

In start/stop mode data transmission the AA bit controls whether repeated DT processes, released by consecutive trigger pulses, but with the same memory content should occur (AA = 0), or whether the HSDA memory content should be updated after each DT process (AA = 1). Loop mode DT processes have to be interrupted by programming in any case. In the DT mode, the DACO will activate its DRQ line upon entering the DMA mode, and it will activate its INTR line in sequences 3, 4 and 7 upon entering the idle mode in order to obtain a programming cycle from the processor. The latter sequences are characterized by EOD = 1 which enables the DACO to detect the end of the DMA cycle. If the INT bit is set, additional INTR pulses are issued in sequences 5 and 7 when entering the DMA mode.

Table 1. Register Selection

Adri				Register Name	R/W
3	2	1	0		
0	0	0	0	Start Address Low Byte	R/W
0	0	0	1	Start Address High Byte	R/W
0	0	1	0	Stop Address Low Byte	R/W
0	0	1	1	Stop Address High Byte	R/W
0	1	0	0	Address Low Byte, $A_0 \ldots A_7$	R
0	1	0	1	Address High Byte, $A_8 \ldots A_{15}$	R
0	1	1	0	Address/Trigger Extension Nibbles, $A_{16} \ldots A_{19}, T_{16} \ldots T_{19}$	R/W(1)
0	1	1	1	Interrupt	RW
1	0	0	0	Pre-/Posttrigger Low Byte	R/W
1	0	0	1	Pre-/Posttrigger High Byte	R/W
1	0	1	0	Delay	R/W
1	0	1	1	Status	R/W
1	1	0	0	Transfer Control	R/W
1	1	0	1	Transfer Control Mask	R/W
1	1	1	0	Parameter	R/W
1	1	1	1	Parameter Mask	R/W

Note:
1. $A_{16} \ldots A_{19}$ read only.

Table 2. Register Bit Map

Bit Mapping	7	6	5	4	3	2	1	0
Transfer Control			SC	EOD	SR1	SR0	BW1	BW0
Parameter			EA	EP	TO	AA	L/S	INT
Delay					RDA1	RDA0	RDY1	RDY0
Interrupt	INT7	INT6	INT5	INT4	INT3	INT2	INT1	INT0
Address/Trigger Ext.	T_{19}	T_{18}	T_{17}	T_{16}	A_{19}	A_{18}	A_{17}	A_{16}
Status						DIR	S1	S0

Table 3a. Transfer Control Register Bit Description

BW0, BW1	**Bus Width:**	BW1	BW0	
		0	0	8-bit
		0	1	16-bit
		1	0	32-bit
		1	1	—
SR0, SR1	Number of DASR's in System	SR1	SR0	
		0	0	1 DASR
		0	1	2 DASR
		1	0	3 DASR
		1	1	4 DASR
EOD	High: DRQ is activated as long as the whole address range defined by the start and stop addresses is transferred. Low: DRQ is activated at the beginning of the DMA-transfer only.			
SC	**Single Cycle:** If set, the DACO interchanges its $\overline{RD}$ and $\overline{WR}$ lines upon DMA access or interprets R/$\overline{W}$ inversly.			

Table 3b. Parameter Register Bit Description

INT	**Interrupt/DMA Mode:** High: INTR is activated together with DRQ. Low: INTR is not activated together with DRQ.
L/S	High: Loop mode Low: Start/stop mode
AA	**Auto-Acquisition:** This bit controls the operational sequences according to Table 5.
TO	The trigger occurred bit is cleared when entering DA/DT mode and set by the first detected trigger pulse.
EP	**Extended Posttrigger:** When set, the trigger counter is extended to 20-bit thereby widening the posttrigger range of the DACO to 1 Msamples.
EA	**Extended Address:** When set, the address bus is extended from 16- to 20-bit.

Table 3c. Wait State Programming

RDY1 RDA1	RDY0 RDA0	Number of Delay CLK Cycles
0	0	0
0	1	1
1	0	2
1	1	3

Table 3d. Interrupt Source Description

INT0	(INT = 1) Data transfer or data modification in HSDA memory required (e.g. after DA if finished).
INT1	All transactions completed, DACO enters the idle mode and expects further instructions from the processor.
INT2	DMA address range overflow (EOD = 0) or DMA-transfer requests unallowed in the current DACO mode.
INT3	Reserved
INT4	Reserved
INT5	Reserved
INT6	Reserved
INT7	Direction error (DIR bit didn't correspond to the direction of microprocessor access), bus cycle terminated without valid data transfer.

Table 3e. Status Register Bit Description

S0, S1	DACO S1 S0 Status: 0 0 Idle 0 1 DMA-Transfer 1 0 Direct Processor Access 1 1 Data Acquisition/Transmission
DIR	**Direction Bit:** Low: Data Acquisition /DPAC read/DMA read High: Data Transmission /DPAC write/DMA write

Table 4. DMA Based Operational Sequences

AA	EOD	L/S	Sequence	No.
a) Data Acquisition Systems				
0	0	0	DA w - T - DA - (!!) DMA d, u. - P	1
0	0	1	DA - T - (!!) DMA d, u - P	2
0	1	0	DA w - T - DA - DMAs - (!) Idle	3
0	1	1	DA - T - DMA s - (!) Idle	4
1	0	0	not permitted	5
1	0	1	not permitted	6
1	1	0	DA w - T - DA - (!!) DMA s - DA w	7
1	1	1	DA - T - (!!) DMA s - DA	8
b) Data Transmission Systems				
0	0	0	DMA s, u - P - DT w - T - DT - DT w - T - DT - . . . - P	1
0	0	1	DMA s, u - P - DT w - T - DT - P	2
0	1	0	DMA d - (!) Idle - P - DT w - T - DT - DT w - T - DT - . . . P	3
0	1	1	DMA d - (!) Idle - P - DT w - T - DT - P	4
1	0	0	DMA s, u - P - DT w - T - DT - (!!) DMA s, u	5
1	0	1	Not Permitted	6
1	1	0	DMA d - (!) Idle - P - DT w - T - DT - (!!) DMA d	7
1	1	1	DMA d - DT w - T - DT - P	8

T = Trigger
P = Programming
d = destination synchronized
u = unsynchronized
s = source synchronized
w = waiting
(!) = INTR to CPU issued
(!!) = INTR to CPU issued, if INT-bit is set

Table 5. Address Decoding Adri → $\overline{CHSi}$ (Direct Processor Access Mode)

8-bit BUS				1 DASR					2 DASR					3 DASR					4 DASR				
Adr-Lines used for decoding				Adr0, Adr1					Adr0–Adr2					—					Adr0–Adr3				
Adri				$\overline{CHSi}$					$\overline{CHSi}$					$\overline{CHSi}$					$\overline{CHSi}$				
3	2	1	0	3	2	1	0	EN	3	2	1	0	EN	3	2	1	0	EN	3	2	1	0	EN
0	0	0	0	1	1	1	0	0	x	0	0	0	0	not applicable for DPAC-mode					0	0	0	0	0
0	0	0	1	1	1	0	1	0	x	0	0	1	0						0	0	0	1	0
0	0	1	0	1	0	1	1	0	x	0	1	0	0						0	0	1	0	0
0	0	1	1	0	1	1	1	0	x	0	1	1	0						0	0	1	1	0
0	1	0	0	1	1	1	0	0	x	1	0	0	0						0	1	0	0	0
0	1	0	1	1	1	0	1	0	x	1	0	1	0						0	1	0	1	0
0	1	1	0	1	0	1	1	0	x	1	1	0	0						0	1	1	0	0
0	1	1	1	0	1	1	1	0	x	1	1	1	0						0	1	1	1	0
1	0	0	0	1	1	1	0	0	x	0	0	0	0						1	0	0	0	0
1	0	0	1	1	1	0	1	0	x	0	0	1	0						1	0	0	1	0
1	0	1	0	1	0	1	1	0	x	0	1	0	0						1	0	1	0	0
1	0	1	1	0	1	1	1	0	x	0	1	1	0						1	0	1	1	0
1	1	0	0	1	1	1	0	0	x	1	0	0	0						1	1	0	0	0
1	1	0	1	1	1	0	1	0	x	1	0	1	0						1	1	0	1	0
1	1	1	0	1	0	1	1	0	x	1	1	0	0						1	1	1	0	0
1	1	1	1	0	1	1	1	0	x	1	1	1	0						1	1	1	1	0

Table 6

16-bit BUS				1 DASR					2 DASR					3 DASR					4 DASR				
Adr-Lines used for decoding				Adr0					Adr0, Adr1					—					Adr0–Adr2				
Adri				$\overline{CHSi}$					$\overline{CHSi}$					$\overline{CHSi}$					$\overline{CHSi}$				
3	2	1	0	3	2	1	0	EN	3	2	1	0	EN	3	2	1	0	EN	3	2	1	0	EN
0	0	0	0	x	x	1	0	0	1	1	1	0	0	not applicable for DPAC-mode					x	0	0	0	0
0	0	0	1	x	x	0	1	0	1	1	0	1	0						x	0	0	1	0
0	0	1	0	x	x	1	0	0	1	0	1	1	0						x	0	1	0	0
0	0	1	1	x	x	0	1	0	0	1	1	1	0						x	0	1	1	0
0	1	0	0	x	x	1	0	0	1	1	1	0	0						x	1	0	0	0
0	1	0	1	x	x	0	1	0	1	1	0	1	0						x	1	0	1	0
0	1	1	0	x	x	1	0	0	1	0	1	1	0						x	1	1	0	0
0	1	1	1	x	x	0	1	0	0	1	1	1	0						x	1	1	1	0
1	0	0	0	x	x	1	0	0	1	1	1	0	0						x	0	0	0	0
1	0	0	1	x	x	0	1	0	1	1	0	1	0						x	0	0	1	0
1	0	1	0	x	x	1	0	0	1	0	1	1	0						x	0	1	0	0
1	0	1	1	x	x	0	1	0	0	1	1	1	0						x	0	1	1	0
1	1	0	0	x	x	1	0	0	1	1	1	0	0						x	1	0	0	0
1	1	0	1	x	x	0	1	0	1	1	0	1	0						x	1	0	1	0
1	1	1	0	x	x	1	0	0	1	0	1	1	0						x	1	1	0	0
1	1	1	1	x	x	0	1	0	0	1	1	1	0						x	1	1	1	0

Table 7

32-bit BUS				1 DASR					2 DASR					3 DASR					4 DASR				
Adr-Lines used for decoding				—					Adr0					—					Adr0, Adr1				
Adri				$\overline{CHSi}$					$\overline{CHSi}$					$\overline{CHSi}$					$\overline{CHSi}$				
3	2	1	0	3	2	1	0	EN	3	2	1	0	EN	3	2	1	0	EN	3	2	1	0	EN
0	0	0	0	x	x	x	0	0	x	x	1	0	0	not applicable for DPAC-mode					1	1	1	0	0
0	0	0	1	x	x	x	0	0	x	x	0	1	0						1	1	0	1	0
0	0	1	0	x	x	x	0	0	x	x	1	0	0						1	0	1	1	0
0	0	1	1	x	x	x	0	0	x	x	0	1	0						0	1	1	1	0
0	1	0	0	x	x	x	0	0	x	x	1	0	0						1	1	1	0	0
0	1	0	1	x	x	x	0	0	x	x	0	1	0						1	1	0	1	0
0	1	1	0	x	x	x	0	0	x	x	1	0	0						1	0	1	1	0
0	1	1	1	x	x	x	0	0	x	x	0	1	0						0	1	1	1	0
1	0	0	0	x	x	x	0	0	x	x	1	0	0						1	1	1	0	0
1	0	0	1	x	x	x	0	0	x	x	0	1	0						1	1	0	1	0
1	0	1	0	x	x	x	0	0	x	x	1	0	0						1	0	1	1	0
1	0	1	1	x	x	x	0	0	x	x	0	1	0						0	1	1	1	0
1	1	0	0	x	x	x	0	0	x	x	1	0	0						1	1	1	0	0
1	1	0	1	x	x	x	0	0	x	x	0	1	0						1	1	0	1	0
1	1	1	0	x	x	x	0	0	x	x	1	0	0						1	0	1	1	0
1	1	1	1	x	x	x	0	0	x	x	0	1	0						0	1	1	1	0

Absolute Maximum Ratings*

Ambient Temperature Under Bias .... 0°C to +70°C
Storage Temperature ..... −65°C to +150°C
Voltage on Any Pin with Respect to Ground ..... −0.3V to V_{DD} +0.3V
DC Power Supply ..... −0.3V to 7.0V
Power Dissipation 1W

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics T_A = 0°C to 70°C, V_{CC} = 5V ±10%

Parameter	Symbol	Conditions	Limits		Units
			Min	Max	
Input Low Voltage	V_{IL}	—	0	0.8	V
Input High Voltage	V_{IH}	—	2.0	V_{DD}	V
Output High Voltage	V_{OH}	I_{OH} = −2.8 mA	3.5	—	V
Output Low Voltage $\overline{ME}$, $\overline{MWE}$, DT/$\overline{R}$, READY, $\overline{HOLD}$	V_{OL}	I_{OL} = 6.4 mA Other Outputs: 3.2 mA	—	0.4	V
Load Capacitance	CL			70	pF

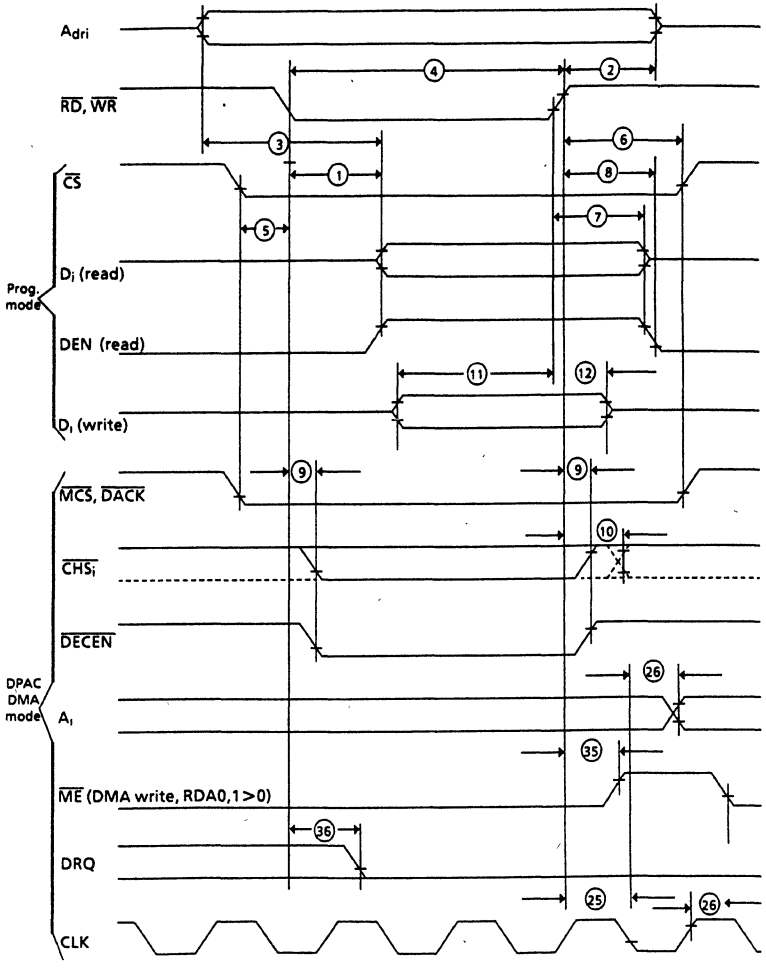
A.C. Characteristics $T_A = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 10\%$

Timing Requirements: all timings measured at 1.5V unless otherwise specified

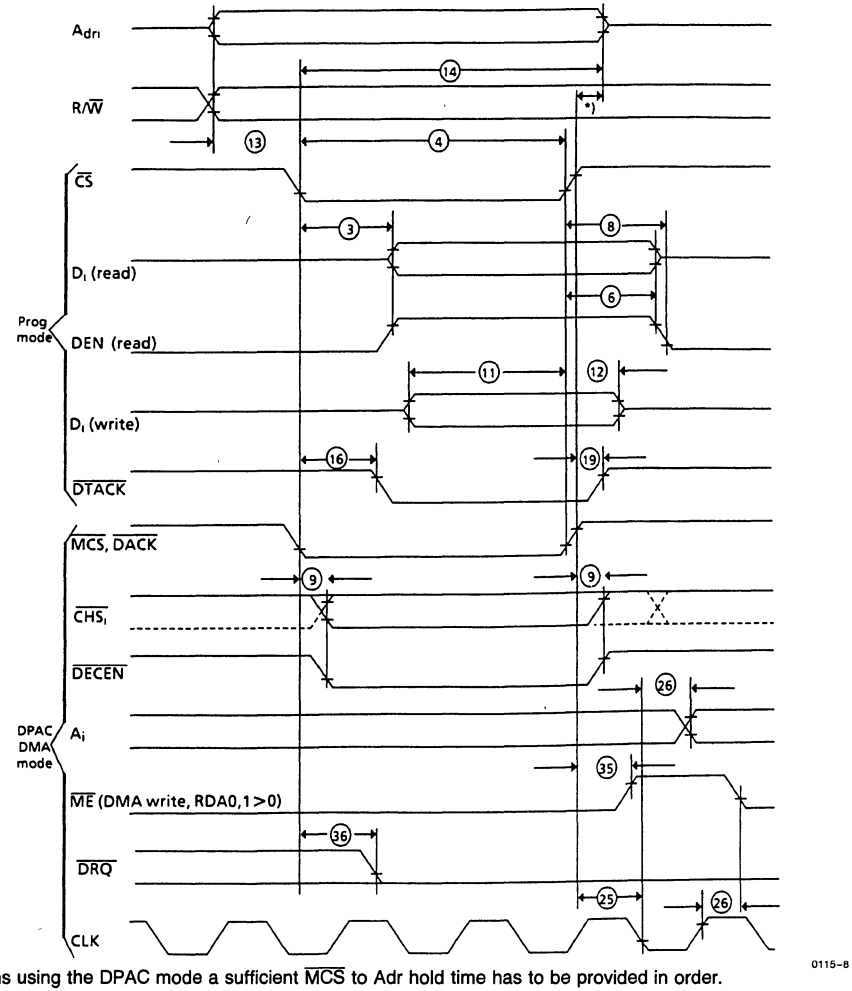
No.	Parameter	Symbol	Limit Values			Units	Test Condition
			Min	Typ	Max		
1	Di Delay			35		ns	
2	Adri Hold			3		ns	
3	Adri to Data Valid Setup			42		ns	
4	Command, Select Pulse Width			150		ns	
5	Select to Command Setup			3		ns	
6	Select Hold			3		ns	
7	Di, DEN Hold			15		ns	
8	$\overline{RD}$ to Di Float, DEN Low Delay			23		ns	
9	$\overline{DECEN}$ Delay			26		ns	
10	$\overline{CHSi}$ Delay			30		ns	
11	Di Setup			15 (5)[a]		ns	
12	Di Hold			15		ns	
13	Adri, R/$\overline{W}$ Setup			5		ns	
14	Adri Hold						
15	$\overline{MCS}$, $\overline{DACK}$ to CLK Setup			15 (10)[a]		ns	
16	$\overline{DTACK}$, READY High Setup			30		ns	
17	$\overline{MCS}$, $\overline{DACK}$ to $\overline{DTACK}$, READY Delay			18		ns	
18	CLK High to $\overline{DTACK}$, READY Delay			18		ns	
19	$\overline{MCS}$, $\overline{DACK}$ to $\overline{DTACK}$ High Delay			25		ns	
20	$\overline{DTACK}$ Active High Pullup				35	ns	
21	CLK Period				$t_4 - 20$	ns	
22	CLK High, Low			40		ns	
23	DACLK Period		40			ns	
24	DACLK High, Low			16		ns	
25	$\overline{WR}$ ($\overline{CS}$, $\overline{DACK}$) Inactive Setup						
26	CLK to Control, Ai Delay			26		ns	
27						ns	
28	DACLK to Ai Delay			20		ns	
29	$\overline{TRIG}$ to $\overline{HOLD}$ Inactive Delay			20		ns	
30	DACLK to $\overline{HOLD}$ Active Delay			28		ns	
31	$\overline{HOLD}$ to CLK Setup						
32	Address Valid						
33	$\overline{TRIG}$ to DACLK Setup			7		ns	
34	$\overline{TRIG}$ Pulse Width		$>t_{23}$				
35	Command, $\overline{CS}$ to $\overline{ME}$, $\overline{HOLD}$ Inactive Delay						
36	DRQ, INTR Inactive Delay			40		ns	
37	$\overline{TRIG}$ Hold			3		ns	

Note:
(a) Timing specifications for Motorola 68 xxx systems (I/$\overline{M}$ strapped low).

SIEMENS/INTEL Interface Bus Cycle Timing

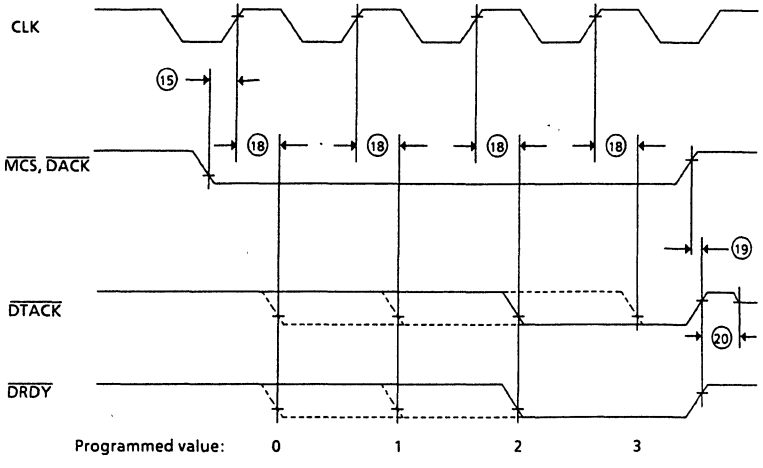


MOTOROLA Interface Bus Cycle Timing

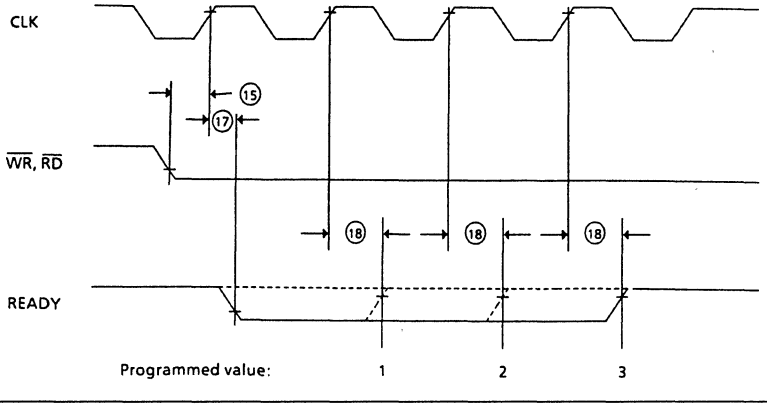


(*) In systems using the DPAC mode a sufficient $\overline{MCS}$ to Adr hold time has to be provided in order.

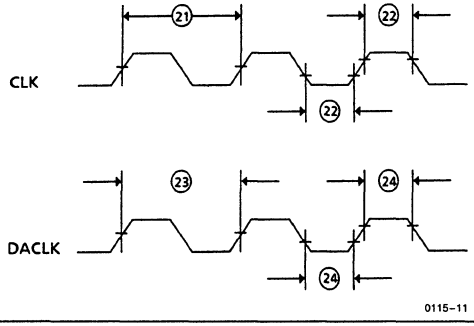
$\overline{\text{DTACK}}$, $\overline{\text{DRDY}}$ Programming



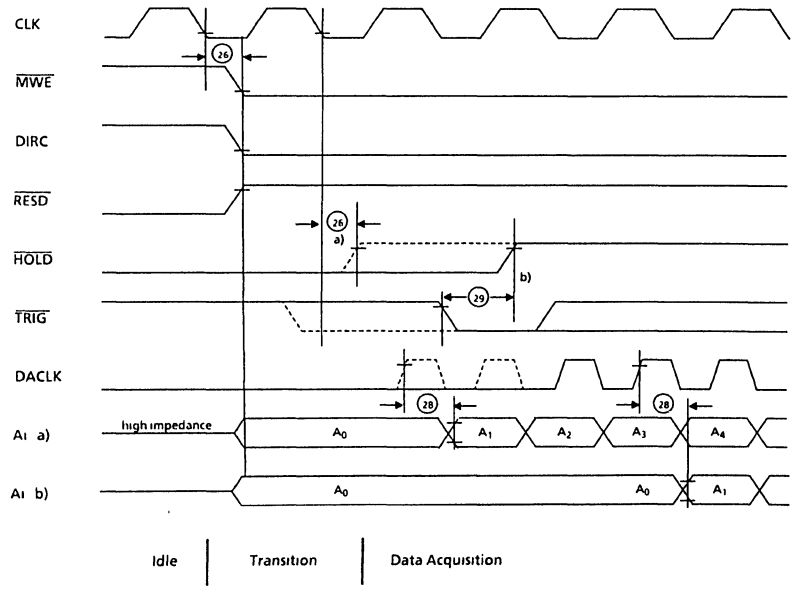
READY Programming



CLK-Inputs

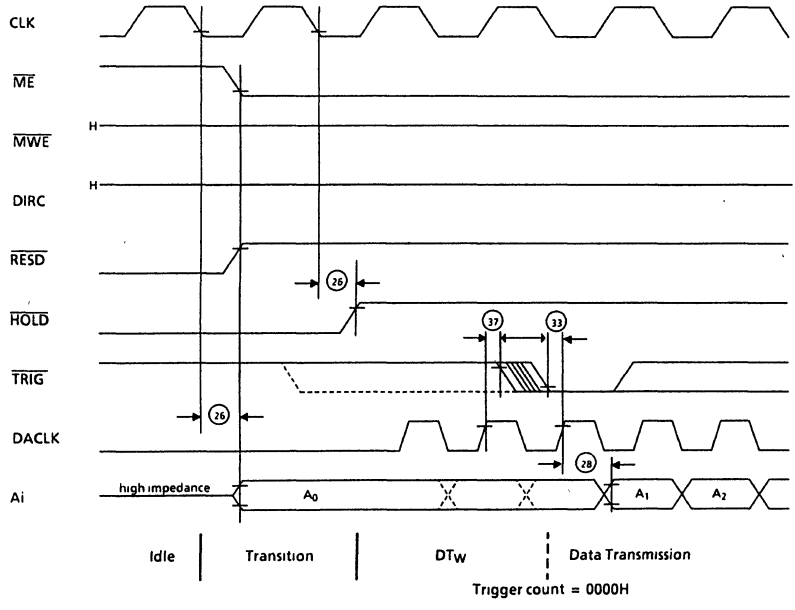


IDLE-DA



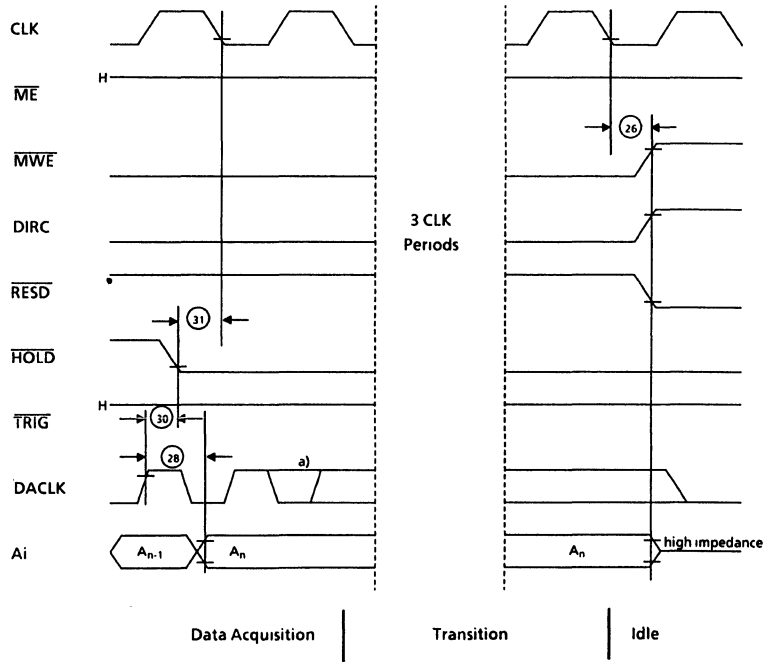
(a) Loop mode
(b) Start/Stop mode

IDLE-DT



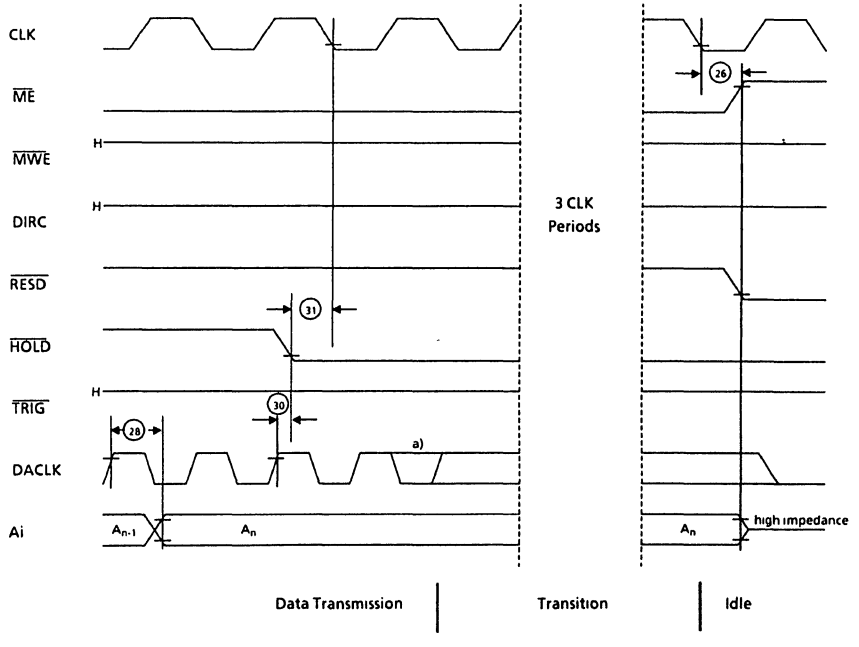
0115-13

DA-IDLE



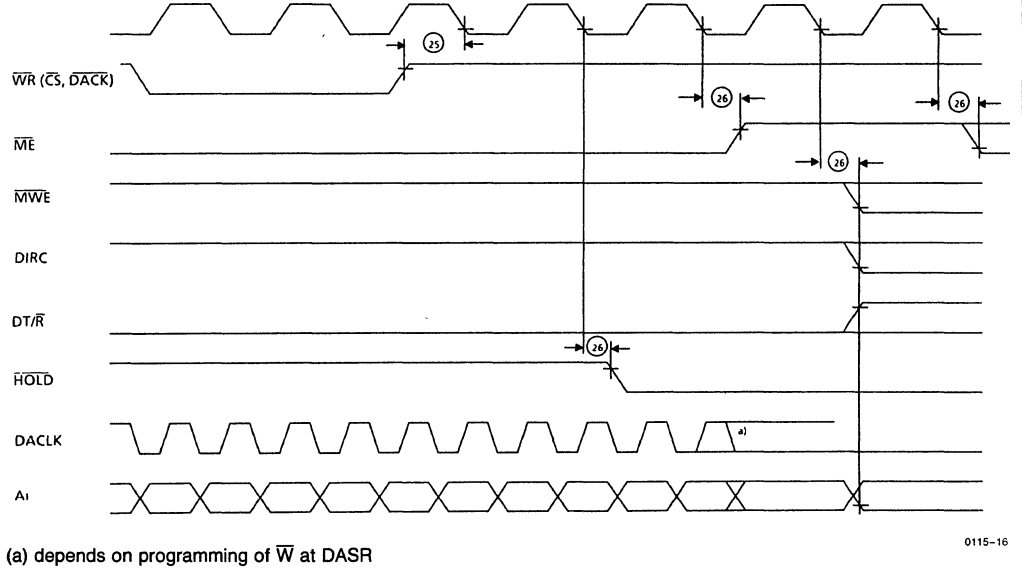
(a) depends on $\overline{W}$ programmed as DAS

DT-IDLE



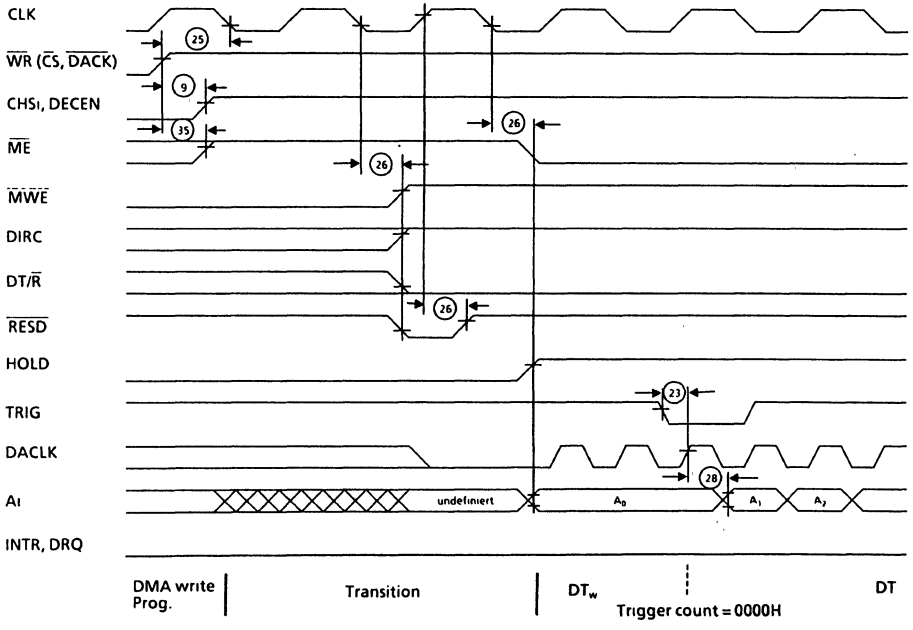
(a) depends on $\overline{W}$ programmed at DAS

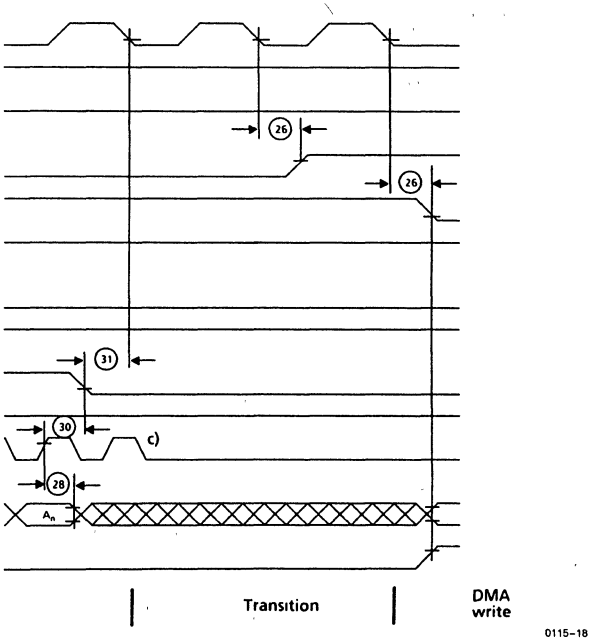
End of DT-mode by Programming



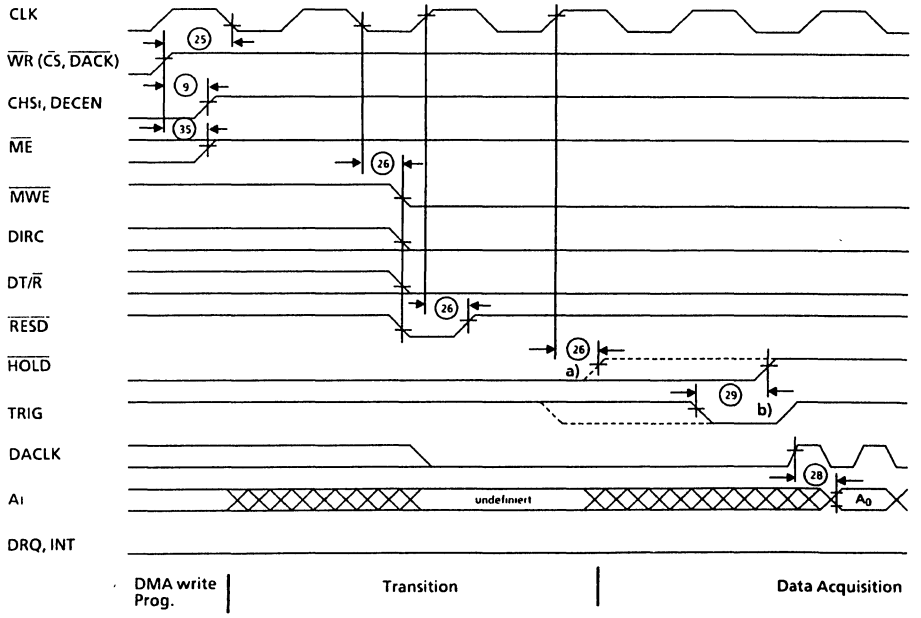
(a) depends on programming of $\overline{W}$ at DASR

DMA/Prog - DT - DMA Cycle

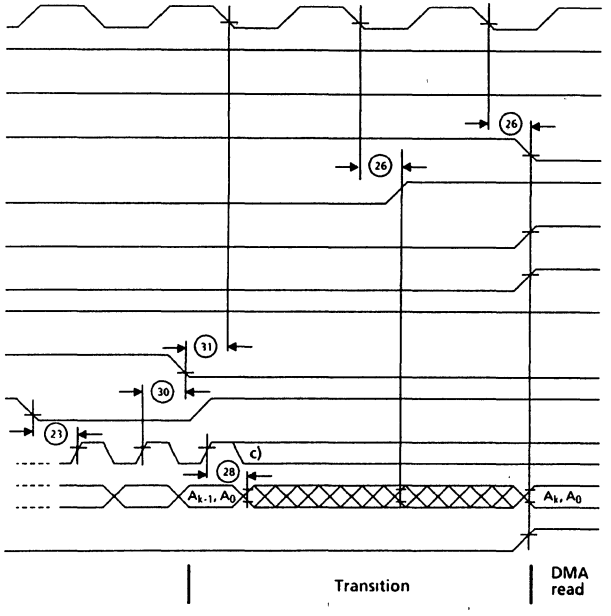




DMA/Prog - DA - DMA



0115-19



0115-20

(a) Loop
(b) Start-Stop
(c) depends on W prog. at DASR

Pin Definitions

Pin	Function	Pin	Function
1	ADR 0	35	A 2
2	ADR 1	36	A 1
3	ADR 2	37	A 0
4	ADR 3	38	$\overline{MWE}$
5	$\overline{DPAC}$	39	$\overline{ME}$
6	DT/$\overline{R}$	40	DIRC
7	$\overline{DECEN}$	41	DACLK
8	$\overline{CHS\,0}$	42	GND
9	GND	43	VDD
10	VDD	44	$\overline{RESD}$
11	$\overline{CHS\,1}$	45	$\overline{HOLD}$
12	$\overline{CHS\,2}$	46	$\overline{TRIG}$
13	$\overline{CHS\,3}$	47	I/$\overline{M}$
14	$\overline{AEN}$	48	CLK
15	A 19	49	RESET
16	A 18	50	INTR
17	A 17	51	READY
18	A 16	52	DRQ
19	A 15	53	$\overline{DACK}$
20	GND	54	$\overline{MCS}$
21	A 14	55	$\overline{CS}$
22	A 13	56	$\overline{WR}$
23	A 12	57	$\overline{RD}$
24	A 11	58	DEN
25	A 10	59	GND
26	VDD	60	VDD
27	A 9	61	D 0
28	A 8	62	D 1
29	A 7	63	D 2
30	A 6	64	D 3
31	A 5	65	D 4
32	GND	66	D 5
33	A 4	67	D 6
34	A 3	68	D 7

Ordering Information

Type	Ordering Code	Package
SDA 8800	Q67000-Axxxx	PLCC68

ICs for Industrial Applications

4

SIEMENS

SAB 0600, SAB 0601, SAB 0602
Three-Tone Chime, Single-Tone Chime, Dual Tone Chime

Three-tone chime SAB 0600

This IC generates the tone sequence of a 3-tone chime. The sound pattern is created by three harmonically tuned frequencies which are switched in succession to a summing point and decay individually in amplitude.

The tone color is adjusted by an external *RC* network (R_1, C_1, and C_2). An 8 Ω loudspeaker can be connected directly via a 100 µF capacitor.

An appropriate design of the loudspeaker housing (shaped as tube or horn) enhances the volume and tone quality and contributes to a pleasant, melodious sound.

4

Features

- Melodious sound
- Few components required
- Integrated output stage for 8 Ω loudspeaker
- Standby current < 1 µA

Single-tone chime SAB 0601 and dual-tone chime SAB 0602

The two variants SAB 0601 and SAB 0602 were derived from type SAB 0600 by suppressing the last two tones or last tone, respectively, of the three-tone sequence. The SAB 0600 data applies correspondingly.

Maximum ratings

		Lower limit B	Upper limit A	
Supply voltage	V_S	−0.5	11	V
Input voltage at E	V_E	−0.5	V_S	V
Neg. input current at E	$-I_E$		2	mA
Load resistance at Q	R_L	7		Ω
Current consumption at start of tone sequence } refer to	I_{SM}		90	mA
Current consumption at end of tone sequence } measurement circuit	I_{SO}		35	mA
Oscillator frequency at C (due to power dissipation)	f_{OSC}	6		kHz
Junction temperature	T_j		150	°C
Storage temperature	T_{stg}	−55	125	°C
Thermal resistance (system-air)	$R_{th\,SA}$		120	K/W

Operating range

Supply voltage	V_S	7	11	V
Ambient temperature	T_{amb}	0	70	°C
Oscillator frequency at C	f_{OSC}	6	100	kHz

Characteristics

$V_S = 7$ V to 10 V; $T_{amb} = 25$ °C

		min	typ	max	
Standby input current	I_0		<1	10	µA
Supply current with open output	I_{SO}		20	35	mA
Max. output power at 8 Ω (tone 3)	P_Q		0.16		W
Max. output voltage at Q (tone 3)	V_{Qpp}		2.8	4.0	V
Deviation of the max. individual amplitudes referred to tone 3	ΔV_{QM}		± 5		%
Frequency variation of basic oscillator with $R_1, C_1 =$ const.	Δf_o		± 5		%
Triggering voltage at E	V_E	1.5		V_S	V
Input current at E ($V_E = 6$ V)	I_E	500	700		µA
Noise voltage immunity at E	$V_{EN\,pp}$		0.3		V
Triggering delay at $f_o = 13.2$ kHz (t_d varies in inverse proportion to f_o)	t_d	2		5	ms
Min. value of external load resistor	R_1		10		kΩ
Max. value of external load resistor	R_1		100		kΩ

Measurement circuit

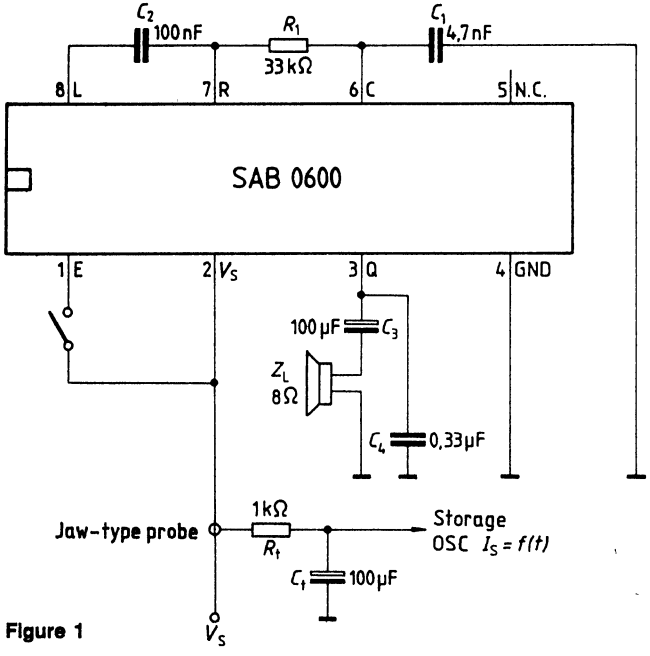


Figure 1

Integral current consumption in the measurement circuit

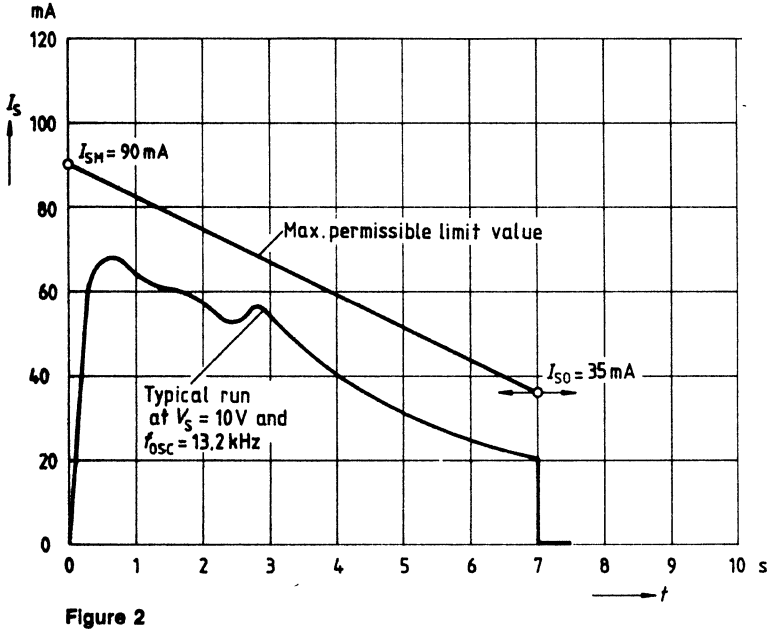


Figure 2

Block diagram

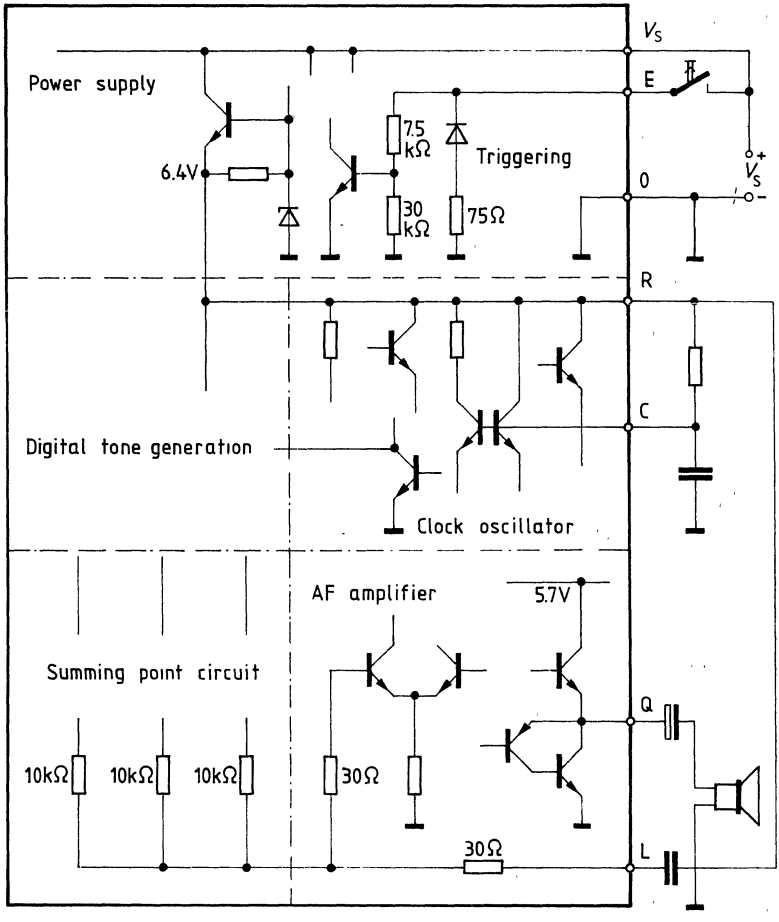


Figure 3

Typical application circuit

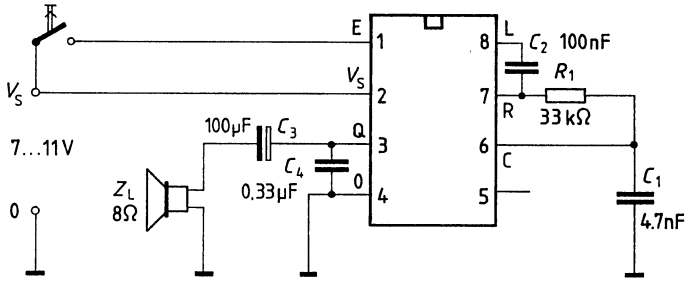


Figure 4

4

Functional description

The three frequencies – 660 Hz, 550 Hz, and 440 Hz – are obtained by dividing the output of a 13.2 kHz oscillator. One of these three frequencies is divided again to obtain the time base for the tone-decay process. From this time base, 4-bit D/A converters (one for each tone) generate the decay voltage with which the three tones are successively activated and, overlapping each other, are attenuated. The basic frequency is determined by an external *RC* network (pins R and C).

The output stage can drive an 8 Ω loudspeaker with approximately 0.16 W via 100 µF. The output voltage is of square shape. To obtain a melodions output tone as required, the higher harmonics may be reduced by shunting pin L through a suitable capacitor to ground. The output volume can be regulated here by means of a potentiometer.

The circuit only draws current in the active state, and automatically switches off after the tones have decayed. The circuit is activated by a short pulse, between 1.5 V and V_S in amplitude, applied to the triggering connection E (pin 1). If the trigger voltage is still, or again, present when the tones have decayed, the three tones are repeated.

The circuit is not activated when a trigger pulse on E is shorter than 2 ms (interference suppression).

To prevent triggering of the circuit by cross-talk voltages, especially in case of long input lines, the noise voltage peaks should be limited to 0.3 V at the IC input. For this purpose the control line (possibly in front of a series resistor) can be shunted to ground through a suitable capacitor.

Application for ac and dc triggering (figure 5)

The input can alternatively be triggered with direct or alternating current. An internal diode circuit hereby short-circuits the input for negative halfwaves.

The peak voltage of the positive halfwave is added to the battery voltage. A series resistor must be connected into the trigger line to limit the voltage at input E (pin 1) to a maximum value equal to V_S.

The minimum input current at pin E of the SAB 0600 (pin 1) is 500 µA at 6 V. If the voltage drop occurring at 500 µA at the series resistor R_3 (figure 5) amounts to at least the ac peak voltage between A and B ($\hat{V}_{AB}$ ~), the IC will be safe.

The formula $$R_{3\,min} = \frac{\hat{V}_{AB\,max.}}{500\ \mu A}$$

determines the lower limit for R_3.

The upper limit for R_3 is determined by the lowest trigger voltage between A and 0 (pin 4). In the application shown in figure 5, this will be the battery voltage if the device is also to be operated independently of the bell system (triggering by short circuit of A and B).

For reliable triggering, the SAB 0600 requires a current of at least 50 µA with approx. 1.5 V at pin E. Assuming this current, the voltage drop at R_3 must, therefore, not exceed $V_S - 1.5$ V.

The formula $$R_{3\,max} = \frac{V_{S\,min.} - 1.5\ V}{50\ \mu A}$$

results in the upper limit for R_3.

Calculation example for the circuit in figure 5

max. $V_{AB\,rms} = 25$ V max. $\hat{V}_{AB} = 25\ V \times \sqrt{2} = 35.4$ V

$$R_{3\,min} = \frac{35.4\ V}{500\ \mu A} = 70.8\ k\Omega$$

min. $V_S = 6$ V

(The operating range of the SAB 0600 may extend to 6 V for individual components).

$$R_{3\,max} = \frac{6\ V - 1.5}{50\ \mu A} = 90\ k\Omega$$

In this example, a value of 82 kΩ ± 10% would be suitable for R_3.

Circuit for SAB 0600 application in home chime installations utilizing ac and dc triggering; adjustable sound and volume

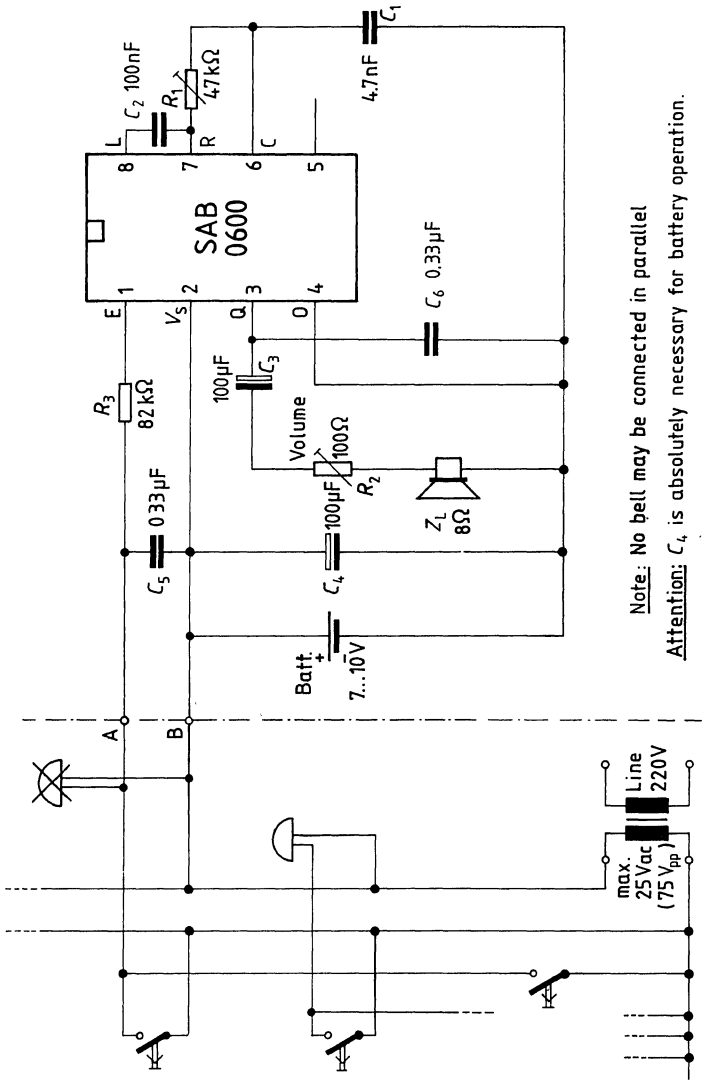


Figure 5

PCB layout information: Because of the high peak currents at V_S, Q, and 0 (ground) and to avoid RF oscillations, the lines should be designed in a flatspread way or as star pattern. Star points are the terminals of capacitor C_4.

Further details regarding the circuit in figure 5

Because an ohmic contact between A and B causes triggering of the chime, no bell may be connected in parallel to the chime. However, paralleling several chimes does not cause any problems.

In older batteries, the higher internal resistance of the battery may cause voltage drops becoming apparent as distortions. C_4 serves as a buffer element expanding the service life of the battery.

The trigger line connected to pin A acts – in open state – as antenna for noise pulses which could trigger the chime unintentionally. Capacitor C_5 will largely suppress such interference.

If there is the risk of incorrect polarity connection when changing the battery, the battery line should be protected by a diode.

For the selection of components, the following recommendations are given:

Capacitors:

C_1: 4.7 nF/≥ 10 V, ± 5%; e.g. MKT
C_2: 100 nF/≥ 10 V, ± 20%; e.g. MKT
C_3: 100 µF/≥6.3 V, ± 100/−10%; e.g. aluminum electrolytic
C_4: 100 µF/≥ 10 V, + 100/−10%; e.g. aluminum electrolytic
C_5, C_6: 330 nF/≥ 50 V, + 100/−20%; e.g. ceramic

Resistors:

R_3: 82 kΩ/0.1 W, ± 10%, carbon film resistor
R_1: When a fixed resistor is used, 0.1 W ± 5% metal film resistor.

SIEMENS

SAE 0700
Audible Signal Device

The audible signal device SAE 0700 generates two tone frequencies in a ratio of approx. 1.4 : 1 that follow one another in a periodic sequence. The tone frequency can be varied throughout a range between 100 Hz and 15 kHz by an external resistor. The switching frequency of 0.5 to 50 Hz is set by an external capacitor. The SAE 0700 can be used to drive either a loudspeaker or a piezo-ceramic transducer. The SAE 0700 can be supplied with voltage in two ways:

1. rms ac voltage from 10 V
2. dc voltage from 9 to 25 V

The SAE 0700 issues the tone sequence for as long as the supply voltage is applied. After application of the supply voltage, the tone sequence commences with the higher of the two tones.

4

Features

- Direct ac-voltage feeding possible through integrated bridge rectifier
- Integrated overvoltage protection through Z diode, approx. 28 V
- Bridge rectifier provides for protection against incorrect polarity in dc operation
- Few external components (one resistor and one capacitor minimum)

Block diagram (with external components for dc supply)

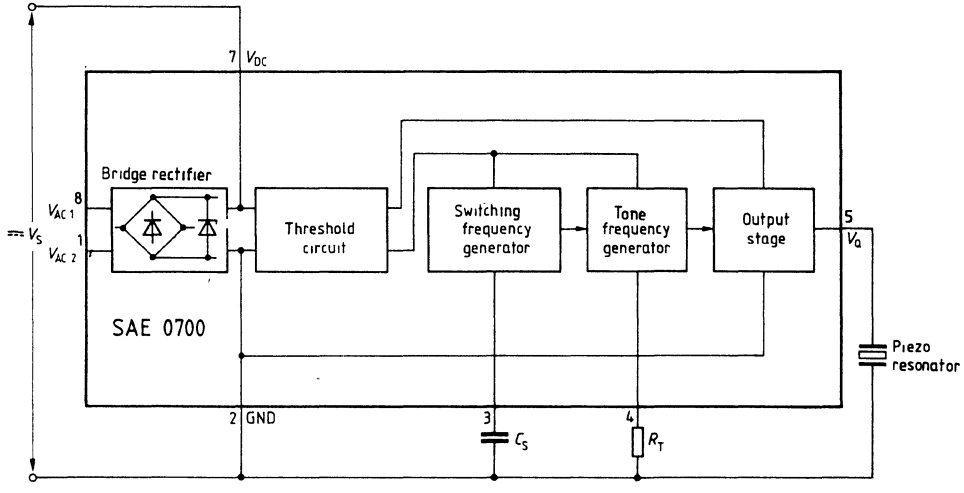


Figure 1

Functional description

The audible signal device SAE 0700 (see blcok diagram, **fig. 1**) includes the following functional blocks:

- bridge (for voltage supply) and overvoltage protection
- threshold circuit
- switching-frequency generator
- tone-frequency generator
- output stage

Bridge rectifier: The bridge rectifier enables direct feeding with ac voltage or dc voltage (independent of polarity). DC-voltage supply without integrated bridge is also possible via pins V_{DC} and GND.

If the voltage is supplied via the bridge, the input voltage V_{81} should be dimensioned such that at least 9 V appear at the pin V_{DC} (also with output loading). It should also be noted that in the case of voltage supply via the bridge, the maximum output current has to be limited to 50 mA.

Response of the SAE 0700 as a result of spikes on the AC line is prevented by a built-in initial resistance R_{INI}. In a voltageless condition R_{INI} provides for discharging the storage capacitor of V_{DC} to ground.

The Z diode following the bridge serves as overvoltage protection. The bridge circuitry shown in **figure 2** efficiently protects the SAE 0700 against damage as a result of the following voltage values:

- overvoltages in acc. with VDE 0433 (2 kV – 10/700 µs)
- ac voltages up to 220 V/50 Hz for a duration of 30 s

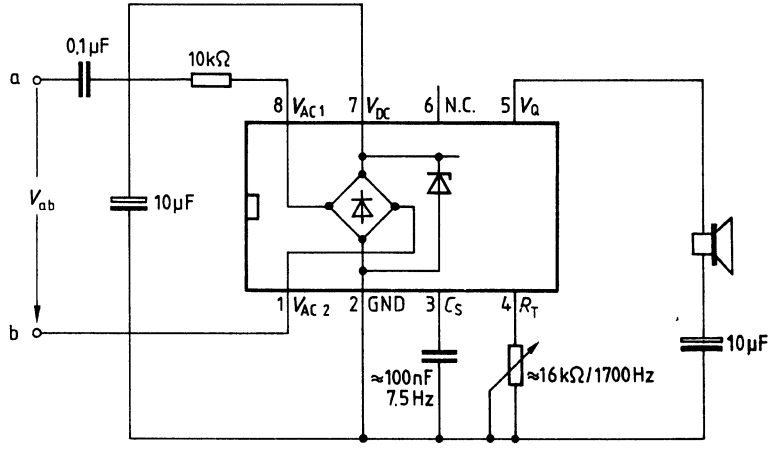


Figure 2

Threshold circuit: With a threshold voltage of typically 8.6 V this ensures that the SAE 0700 is not activated by noise pulses.

Switching-frequency generator: This switches periodically between the two frequencies produced by the tone-frequency generator. Wiring with a capacitor C_S produces a switching frequency f_S according to the following formula:

$$f_S\ [\text{Hz}] = \frac{750}{C\ [\text{nF}]} \pm 25\% \quad \text{(valid from 0.5 to 50 Hz)}$$

Tone-frequency generator: This generates a squarewave voltage with the two tone frequencies f_{T1} and f_{T2}. The basic frequency f_{T1} and the second tone frequency f_{T2} are calculated according to the following formulae:

$$f_{T1}\ [\text{Hz}] = \frac{2.72 \times 10^4}{R\ [\text{k}\Omega]} \pm 25\% \quad \text{(valid from 0.1 to 15 kHz)}$$

$$f_{T2}\ [\text{Hz}] = f_{T1} \times (0.725 \pm 5\%)$$

The tone-frequency generator is temperature-compensated for better stability.

Output stage: This boosts the generated tone voltage for direct driving of a piezo-ceramic transducer or a loudspeaker, possibly across a dropping resistor.

Pin configuration

Pin No.	Symbol	Function
1	V_{AC2}	AC-voltage input
2	GND	Ground
3	C_S	Connection for capacitor C_S
4	R_T	Connection for resistor R_T
5	Q	Output
6	N.C.	Not connected
7	V_{DC}	DC-voltage input
8	V_{AC1}	AC-voltage input

Maximum ratings

		Lower limit	Upper limit	
Voltage at pin 7	V_{DC}	−0.5	26	V
Voltage at pin 3	V_{32}	−0.5	5.5	V
Voltage at pin 4	V_{42}	−0.5	7	V
Output voltage at pin 5	V_Q	−0.5	V_{DC}+0.5	V
AC voltage at pin 8 and 1 (peak value)	V_{AC}		28	V
Input current of bridge	I_{81}	−50	50	mA
AC input current of bridge	$I_{81\,rms}$		25	mA
Output current (50 µs, duty cycle 1 :10)	I_Q	−100	100	mA
Output current	$I_{Q\,rms}$		50	mA
Total power dissipation (T_{amb} = 25 °C)	P_{tot}		0.8	W
Junction temperature	T_j		150	°C
Storage temperature	T_{stg}	−40	125	°C
Thermal resistance (system-air)	$R_{th\,SA}$		120	K/W

Operating range

Supply voltage	V_{DC}	9	25	V
Tone frequency	f_{T1}	0.1	15	kHz
Ambient temperature	T_{amb}	−25	85	°C

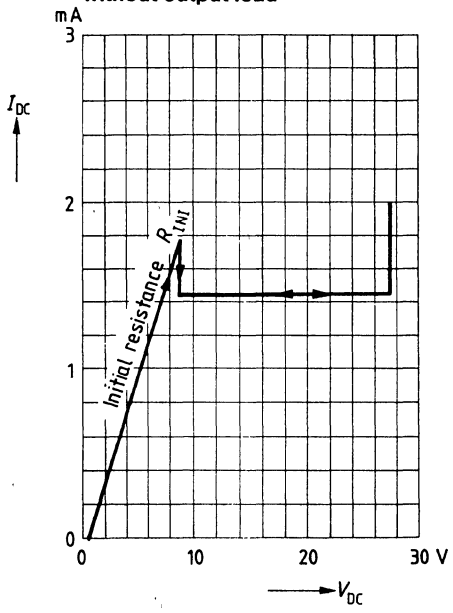
Characteristics

T_{amb} = −25 °C to 85 °C

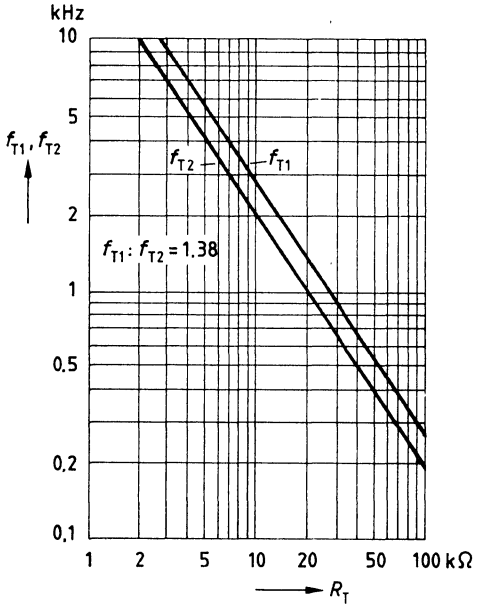
		Test conditions	Lower limit B	typ	Upper limit A	
Current consumption	I_{DC}	V_{DC} = 9 V to 25 V, w/o load		1.5	1.8	mA
Switching threshold	$V_{DC\,ON/OFF}$		8	8.6	9	V
Initial resistance	R_{INI}	see characteristic, figure 3	3.5	4.7	6	kΩ
Output-voltage swing	V_Q	I_Q = ± 10 mA	V_{DC}−3.7	V_{DC}−3		V
Tone frequency	f_{T1}	V_{DC} = 15 V, V_{32} = 0 V, R_T = 16 kΩ	1.275	1.700	2.125	kHz
Switching frequency	f_S	V_{DC} = 15 V, C_S = 100 nF	5.6	7.5	9.4	Hz
Tone frequency ratio	f_{T1}/f_{T2}		1.31	1.38	1.45	
Temperature coefficient of tone frequencies	TC_f			8×10^{-4}		K^{-1}

Characteristic curves

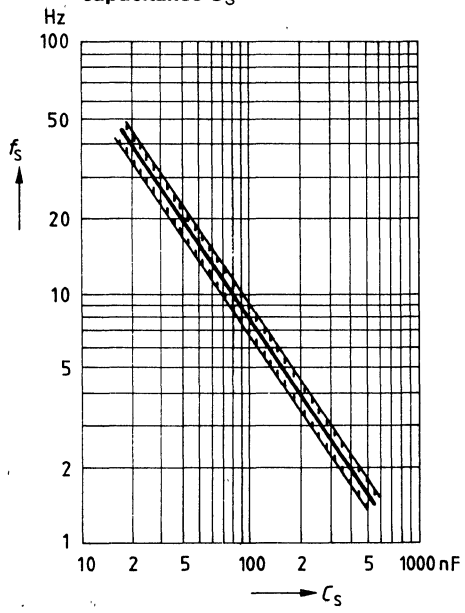
Current consumption versus supply voltage V_{DC} without output load



Tone frequencies f_{T1} and f_{T2} versus resistance R_T



Switching frequency f_S versus capacitance C_S



4

SIEMENS

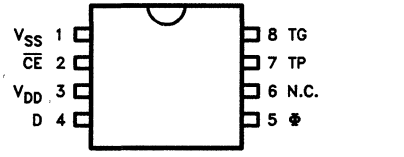
Preliminary

SLB 0586
CMOS Dimmer

- Sensor Operation—No Mechanically Moved Switching Elements
- Operation Is Also Possible from Several Extensions by Means of Sensors or Push Buttons
- Can Replace Electromechanical Wall Switches in Conventional Light Installations
- Brightness Control with a Physiologically Approximated Linear Characteristic
- Very High Interference Immunity, also against Ripple Control Signals
- Very Few Peripheral Components
- Programming Input Permits Selection of Three Different Functions (Type A/B/C)
- "Soft" Turn-On with Types A and C

Pin Configuration

(Top View)



0109-5

Pin Definitions

Pin	Function
1	V_{DD}
2	Programming Input
3	C_1 Integrator
4	Sync Input
5	Sensor Input
6	Extension Input
7	V_{SS}
8	Trigger Pulse Output

The SLB 0586 is an integrated circuit in CMOS technology that permits the design of digital electronic dimmers. A single sensor or an equivalent extension input are used to turn the dimmer on and off and to set the required brightness.

(The SLE 0586 replaces the S 576 A/B/C family).

Block Diagram

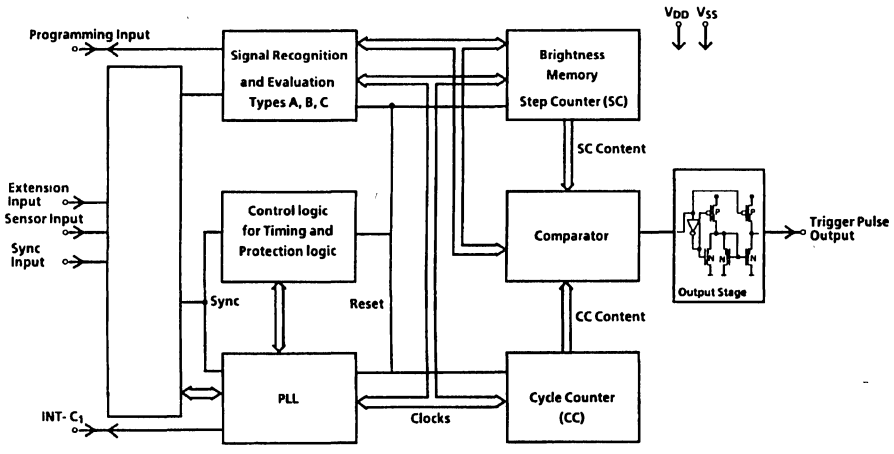


Figure 1

Description of Function

The SLB 0586 permits the design of fully electronic dimmers for light bulbs (resistive loads) which are operated via a single sensor.

The integrated circuit replaces mechanical wall switches in conventional light circuit installations. All functions can be selected from several switching points (extensions).

The brightness is set by phase control. Its digital logic is synchronized with the line frequency (see block diagram, Figure 1).

It is possible to supply the IC via a two-wire connection, as the angle of current flow is limited to a maximum of 152°C of the half wave.

Operation (Refer to Figure 2)

The integrated circuit can distinguish the instruction "ON/OFF" and "Dimming" by the duration for which control input is operated, i.e. the sensor is touched.

Turning On/Off

Short touching (50 to 400 ms) of the sensor area turns the lamp on or off, depending on its preceding state. The switching process is activated as soon as the sensor is released.

Setting of the Brightness (Dimming)

If the sensor is touched for a longer period (>400 ms), the angle of current flow will be varied continuously. It runs across its control loop in approximately 7.6s (e.g. bright-dark-bright) and continues this sequence until the sensor is released.

Easy operation, even in the lower brightness range, is enabled by the following procedure: the phase control angle is controlled such that the lamp brightness varies physiologically-linear with the operating time and rests for a short period when the minimum brightness is reached.

Control Behavior

The three functions A, B, C, differ in their control behavior. The required function is set with the programming input.

Type A With turn-on, the maximum brightness level is set.; with dimming, control starts from the minimum brightness level. With repeated dimming, control is carried out in the same direction (e.g. "brighter").

Type B With turn-off, the selected brightness is stored and set again when the switch is turned on. Dimming starts at this stored value and the control direction is reversed with repeated dimming.

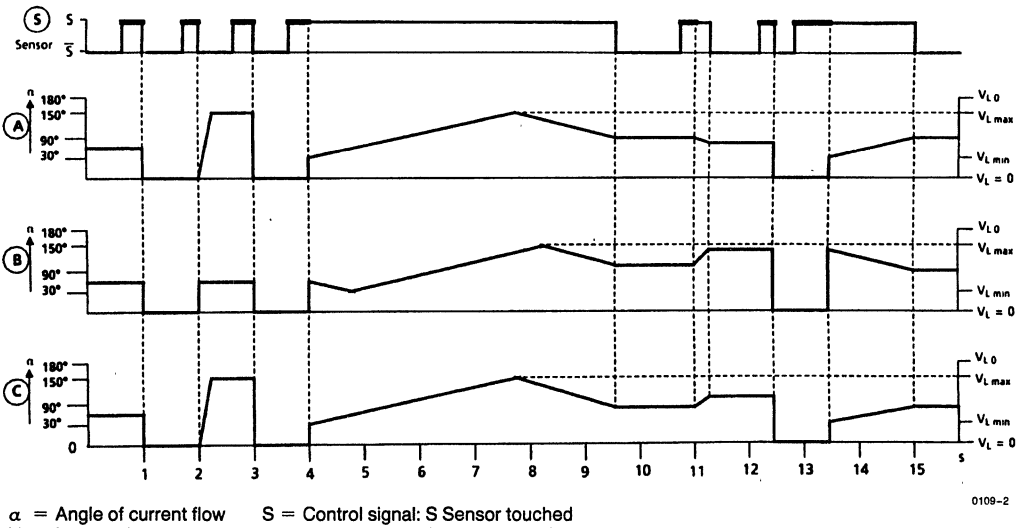
Type C With turn-on, the maximum brightness is set; with dimming, control is started from the minimum brightness. the control direction is reversed with repeated dimming.

Programming of the Various Functions

Type A: V_{12} = V_{SS} (L)
Type B: V_{12} = open (tristate)
Type C: V_{12} = V_{DD} (H)

V_{12} = Level at pin 2

Control Behavior of Function Types A/B/C: (Schematic)



α = Angle of current flow
V_L = Lamp voltage
S = Control signal: S Sensor touched ($\leq$0.4s, $\geq$ 0.4s)
$\overline{S}$ Sensor not touched

Types A and C permit "soft" turn-on, i.e. brightness is increased from 0 to maximum within 380 ms.

Figure 2

Absolute Maximum Ratings*

Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit (V_{DD} = 0V). (without external protective circuitry)

Supply Voltage (V_{SS}) ..... −7.5V to +0.3V
Input Voltage (V_I) ..... V_{SS} −0.3V to +0.3V
Junction Temperature (T_j) ..... 125°C
Storage Temperature (T_{stg}) ..... −55°C to +125°C
Total Power Dissipation
(T_A = 25°C) ..... 10 mW
Thermal Resistance
(System-Air) (R_{thSA}) ..... 135 K/W

Integrated circuits exhibit optimum reliability and service life when the junction temperature does not exceed 125°C during operation. In principle, an IC can tolerate a maximum junction temperature of 150°C. It has to be considered, however, that operation at maximum ratings for prolonged periods may adversely effect component reliability.

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Operating Range

In the operating range the functions given in the circuit description will be fulfilled. Deviations from the characteristics are possible. All voltages are referred to V_{DD} = 0V.

Supply Voltage (V_{SS}) ..... −4.8V to −5.8V
Ambient Temperature (T_A) ..... 0°C to +80°C

4

Characteristics

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics will apply at T_A = 25°C, V_{SS} = 5V (V_{DD} = 0V).

Parameter	Symbol	Conditions	Limits			Units
			Min	Typ	Max	
Supply Current	I_{SS}	f_{sync} = 50/60 Hz		0.45/0.46	0.6	mA
Supply Current with Missing Sync Signal	I_{SS}	f_{sync} = 0			0.45	mA
Input Reverse Current	I_I			0.5		nA
Input Capacitance	C_I	U_I = 0V f = 1 MHz		5		pF
Sensor Input (Pin 5)						
H Input Voltage L Input Voltage Peak Input Current	V_{IH} V_{IL} I_{IH}	with Series Resistor 10 MΩ at 220V Line	½ V_{SS} + 1.1	 33	 ½ V_{SS} − 1.1 37	V V µA
HL Transition Time (Trigger Transition) LH Transition Time Frequency with Active Signal	t_{THL} t_{TLH} f	Synchronized with 50/60 Hz Clock at Sync Input		Line Sine Wave 50/60		 Hz
Extensions (Pin 6)						
H Input Voltage L Input Voltage Input Current	V_{IH} V_{IL} I_{IH}	 V_{SS} − 0.3V (or V_{DD} + 0.3V)	½ V_{SS} + 1.1	 0.5	 ½ V_{SS} − 1.1	V V µA

Characteristics (Continued)

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics will apply at T_A = 25°C, V_{SS} = 5V (V_{DD} = 0V).

Parameter	Symbol	Conditions	Limits			Units
			Min	Typ	Max	
Sync Input (Pin 4)						
H Input Voltage L Input Voltage Input Current	V_{IH} V_{IL} I_{IH}	with Series Resistor 1.5 MΩ from 220V Line	½ V_{SS} + 1.1	 207	 ½ V_{SS} − 1.1 240	V V µA
HL Transition Time (Trigger Transition) LH Transition Time Frequency	t_{THL} t_{TLH} f			Supply Sine Wave 50/60		 Hz
Programming Input (Pin 2)						
Input Capacitance to V_{SS}	C_I			7		pF
Load Capacitance through Board with TRISTATE	C				7	pF
Programming of Function Types (See Figure 2)						
Integrator (Pin 3)						
Application Circuit	C_5 R_{10}	Ref: Figure 3	68 82	100 100	330 120	nF kΩ
Output (Pin 8)						
L Output Current	I_Q	V_{SS} = −5V V_{QL} = −3V	25			mA
L Pulse Width	t_{QL}	50 Hz Supply 60 Hz Supply			39.0 32.6	µs µs
L Output Voltage	V_L			V_{DD} − 0.6		V
HL Transition Time	t_{HLQ}				20	µs
LH Transition Time	t_{LHQ}				20	µs

Description of Application Circuit

(See Figure 3)

The suggested circuit design for the SLB 0586 has the following functions:

- Current supply for the circuit (R_1, C_2, D_1, D_2, C_3).
- Filtered signal for synchronizing the internal time base (PLL circuit) with the line frequency (R_2, C_4). For special applications C_4 may be increased to 15 nF, but only at the expense of the lamp brightness! Brightness wil be reduced (shift of the control range to the left)
- Integrator for internal PLL circuit (C_5, R_{10})
- User protection (R_8, R_9)
- Sensitivity setting of the sensor (R_7)
- Current limitation in case of incorrect polarization of the extension (R_5, R_6). Both resistors can be omitted if no extension is connected. In this case pin 6 must be connected to V_{SS} (pin 7).
- D3: Reduction of positive voltages, which may arise during the triggered state at the gate of some triacs, to values below V_{SS} + 0.3V (compare characteristics). If suitable triacs are used, diode D3 can be omitted. (This feature of the triac depends on the anode current and on the internal resistance between G and A1; it can be measured and specified by the manufacturer.)

Application Circuit

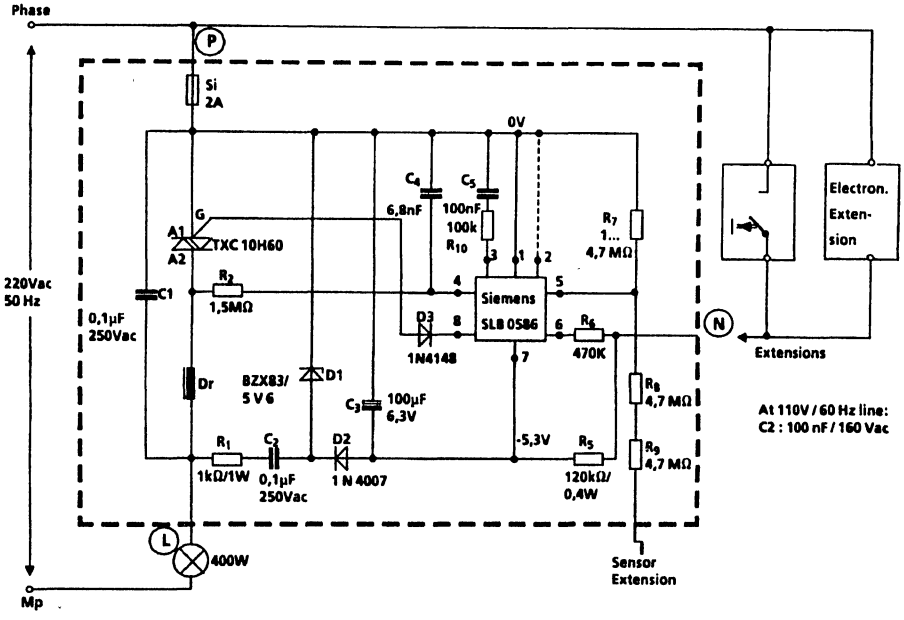


Figure 3

- Dr: The choke and C1 are integrated for EMI suppression. The elements for EMI suppression have to be dimensioned in accordance with
  VDE 0875/Part 2 (general)
  VDE 0550/Part 6 (chokes)
  or in accordance with other relevant regulations, depending on the application intended.

Reference values: 1.4 mH ... 2 mH, Q = 11 ... 24

Extensions

All switching and control functions can also be performed from extensions which are connected to the extension input. The main sensor input and the extension inputs have equal priority. Electronic sensor switches or mechanical pushbutton switches can be connected to the extensions. During operation "H" potential must be applied to the extension input for both half cycles.

An electronic circuit suitable for this purpose is shown in the application example (Figure 4). The circuit operates as return delay and takes over the triggering of the switching transistors during the negative half cycle.

- Response time approx. 2 ms
- Return delay time approx. 30 ms
- Protection against incorrect polarization (R_1, D1, Si)

Note:
The extension input must be connected to V_{SS}, if this input is not required.

Operation of the Control Inputs

Input potential during both half ways of the line phase:

Function	Line Half Wave	Sensor Input	Extension Input		
Operated	Positive	L	H		
	Negative	0	H		
Not Operated	Positive	H	L	or	0
	Negative	0	0		L

Application Circuit-Electronic Extension

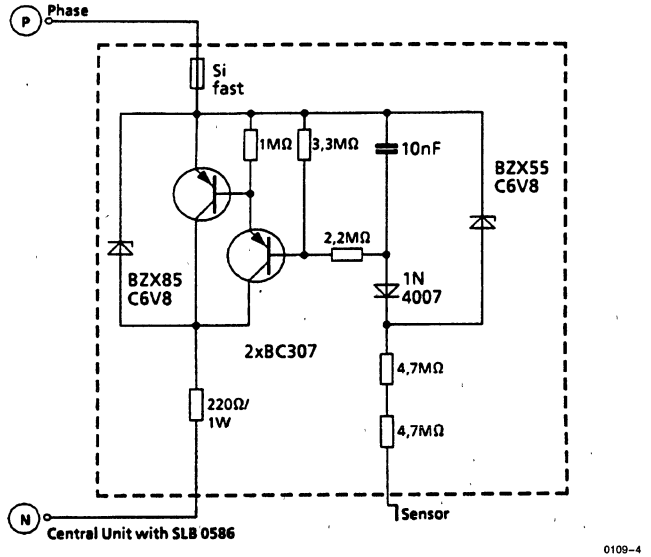


Figure 4

Wireless Remote Control

The connection of a wireless remote control to the extension is very easy. All functions of the SLB 0586 can be performed with the aid of a single transmission channel.

Interference Immunity

A digitally determined immunity period of approximately 50 ms ensures a high interference immunity against electrical variations on the control inputs and additionally allows almost delay-free operation.

Due to the special logic of the extension input, even large ground capacitances of the control line will not lead to interference.

In case of power failure the set switching state with the recommended external circuitry remains stored. After prolonged power failure the circuit turns into off-state.

The control characteristic of the synchronous oscillator (PLL circuit) is designed such that interference due to ripple control signals may cause slight variations in brightness. However, they will not lead to malfunction of the dimmer.

General Information

All time specifications refer to a line frequency of 50 Hz. In case of a line frequency of 60 Hz, the times are reduced accordingly.

Ordering Information

Type	Ordering Code	Package
SLB 0586	Q67100-H8605	DIP 8

SIEMENS

SLE 4501
Nonvolatile Safety Counter

Preliminary Data

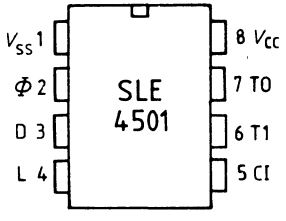
Type	Ordering Code	Package
SLE 4501	Q67100-H8377	P-DIP 8
SLE 4501 K	in preparation	MIKROPACK

Features

- Internal generation of programming voltage
- Counting range 22 bits binary, nonvolatile storage
- Count output in serial binary code
- Counting operation is executed under on-chip control and cannot be influenced externally
- Disconnection of the operating voltage, even during a counting operation, has no effect on the stored count
- The count is protected against manipulation by internal safety logic after blowing a fusible link
- Additional 64x8 bit EEPROM area with serial access (byte organization)
- Extended temperature range: −40...+110 °C

4

Pin Configuration



Pin Description

Pin	Symbol	Funktion
1	V_{SS}	Ground
2	Φ	Clock input
3	D	Data input/output
4	L	Chip select for data input (active high) and indication of storage operation (active low)
5	CI	Counter input (active high)
6	T1	Fusible link
7	TO	Control input test operation and fusible link
8	V_{CC}	Operating voltage

Circuit Description

The nonvolatile counter (NC) has a counting range of 22 binary bits and retains its count even after the operating voltage has been disconnected. The safety logic of the device prevents any alteration other than the intended incrementing of the count from being caused by supply voltage failures, eg. during a counting operation. Before the fusible link is blown, a desired count can be preset in a test operation. After the fusible link is blown, the count can only be altered by a count request. Thus it is only possible to increment the counter.

The count is binary coded and can be sampled serially on a three-wire bus (section 4). A counting operation has priority in any case and will terminate any readout operation that has been started.

The 64x8 bit EEPROM area (NVM) is addressed serially by a 1-byte OP code (see programming and readout operation). Addresses 16 through 63 can no longer be reprogrammed after the fusible link is blown. Before the fusible link is blown, test input T0 should be set low for normal operation.

An on-chip reset circuit ensures operational reliability. Its function is described on page 5.

Counting Operation (fig. 1c)

The integrated circuit consists of a 22-step, asynchronous counter and a nonvolatile, electrically reprogrammable memory (EEPROM) for nonvolatile storage of the counter content.

For reasons of operational reliability, the counting operation is executed entirely under on-chip control. The device includes the necessary sequence control for which it generates an internal clock of approx. 50 kHz. A pulse at input CI causes the asynchronous counter to be incremented by 1.

The new count is stored as nonvolatile information. This storage operation is indicated by low on input/output L. During storage no other count events are registered resulting in a dead time of 10 ms max. in the rated-voltage range. The operating voltage must be maintained in the rated-voltage range for at least another 10 ms after the start of a storage operation, or else the last count event might not be permanently stored (response time). Counts that have already been stored are not at all affected if the operating voltage is switched off during a storage operation and thus cannot be manipulated. If the operating voltage is reduced during the counting operation, the dead time and the response time will become longer, but storage reliability is not affected due to the integrated programming-duration control. The device is inactive outside the operating-voltage window defined by the reset circuit.

The nonvolatile counter includes overflow protection. If all counter bits are 1, any further count pulses are ignored.

Count Readout (fig. 1d)

For sampling the count, input/output L is first set low and then the two instruction bits B0, B1 are clocked in. After this, pin L goes high again. With the trailing edge of each further clock pulse Φ there appears on pin D, starting with the most significant bit, the next least significant bit. The entire count is read out with 22 clock pulses. A low pulse on input/output L switches pin D back to high impedance.

A storage operation (nonvolatile counter or 64x8 bit EEPROM) indicated by a low on pin L always has priority. During this time the device cannot be addressed. A count request will terminate any readout operation that has already been started.

Programming of NVM (fig. 1a)

The input/output L must be set low. Then the 8-bit data word (D0 as the 1st bit) is first clocked in, followed by the 8-bit instruction word (consisting of six address bits A0 through A5 and two instruction bits B0, B1). After pin L has gone high again, the programming operation, indicated by low on the input/output L, begins following a further clock pulse Φ. When the internally controlled storage operation has been completed, L returns to high. In the rated-voltage range, the maximum programming time is 10 ms.

Readout of NVM (fig. 1b)

The input/output L must be set low. Then the 8-bit instruction word (consisting of 6 address bits A0 through A5 and two instruction bits B0, B1) is clocked in. After pin L has gone high again, one bit (beginning with D0) of the respective data word appears on pin D with the trailing edge of each further clock pulse Φ. The entire data word is read out with eight clock pulses. A low pulse on input/output L switches pin D back to high impedance.

Fusible Link (fig. 4)

Blowing the fusible link has the following irreversible effects:

a) The count can now only be altered by count pulses on count input CI.
b) It is no longer possible to program the entire NVM in one operation.
c) Addresses 16 through 63 of the NVM can no longer be reprogrammed.

In order to blow the fusible link, the following conditions have to be produced on the inputs (cf. **fig. 4**):

a) Test input T0 on 17 V
b) Test input T1 on 17 V with max. 1 µs edge rise time.

The fusible link melts within 100 ms. On test input T0 there is a temporary peak current of up to 100 mA which can be taken from a storage capacitor for instance.

For the blowing process, test input T0 must be connected according to **fig. 4b**, otherwise the device might be destroyed.

Test Operation (fig. 2a, 2b, 2c)

Provided the fusible link is not blown, the following modes of test operation are possible (T1 must always be kept low and T0 high):

a) Presetting of count **(fig. 2a)**

The input/output L is set low and then the 22 bits constituting the required count are clocked in starting with the most significant bit. Here it should be noted that the counter bits CB0 through CB3 can only be programmed uniformly as 0 or 1. After the two bits of the instruction code have been clocked in, pin L is set high again.

Differing values for CB0 through CB3 will lead to undefined counts.

A high on count input CI starts the programming operation which is indicated by a low on pin L. In order to activate the safety logic for the present count, T0 must then be set low and the supply voltage briefly switched off.

b) Erasure of entire NVM **(fig. 2b)**
Writing into entire NVM **(fig. 2c)**

Input/output L is set low and the two bits B0, B1 of the instruction code are clocked in. After switching pin L to high, a high on input Φ will start the programming operation which is indicated by a low on input/output L. Input Φ must be kept high for at least 50 ms because the internal timing control for the NVM is off and the programming duration (t_{prog}) is defined for the length of the Φ pulse.

Instruction Codes

a) T0 low or after blowing the fusible link:

Function	B0	B1
Program NVM	1	0
Read out NVM	1	1
Read out counter	0	1

b) T0 high (test operation):

Started by pulse at CI

Function	B0	B1
Preset counter	0	0

Started by clock pulse ϕ

Function	B0	B1
Erase entire NVM Write into entire NVM	1	0

Reset Function

For reasons of operational reliability the device contains an internal reset circuit that limits the active range of a voltage window. The lower limit is a maximum of 4.5V and the upper limit a minimum of 5.5V.

If the supply voltage is outside this window, even if only because of spikes, the device will reset. As soon as the supply voltage is again within the voltage window, an internal reset routine is run which is indicated by a low on input/output L and means a dead time of 100 ms max. in the rated-voltage range.

Maximum Ratings

		min.	typ.	max.	Unit
Supply voltage	V_{CC}	−0.3		6	V
Input voltage	V_I	−0.3		6	V
Power dissipation	P_D		40		mW
Storage temperature	T_{stg}	−55		125	°C
Thermal resistance system-air	$R_{th\ SA}$		100		K/W

Operating Range

Supply voltage	V_{CC}	4.75		5.25	V
Ambient temperature	T_A	−40		110	°C

Maximum Ratings

Maximum ratings are absolute ratings. Exceeding even one of them may result in the destruction of the integrated circuit.

Operating Range

Within the operating range the functions mentioned in the circuit description will be fulfilled. Deviations from the characteristics are possible.

Characteristics

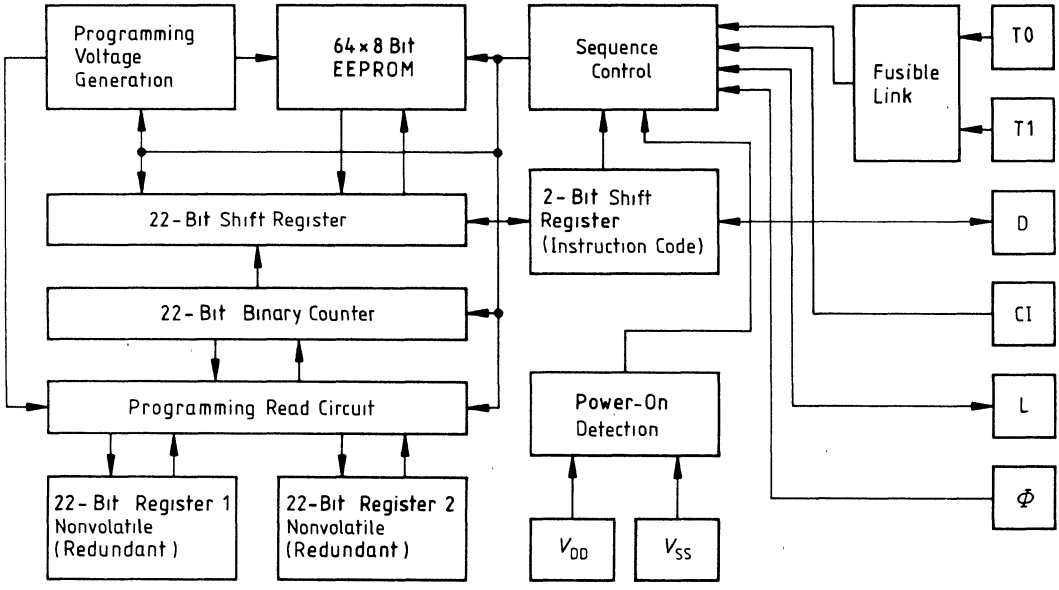
		min.	typ.	max.	Unit
Supply voltage	V_{CC}	4.75		5.25	V
Supply current	I_{CC}		7	10	mA
Inputs	V_I		0.5	0.8	V
(Φ, L, CI, D, T0, T1)	V_H	2.2		V_{CC}	V
(Φ, L, CI, D, T1)	I_H			10	µA
(T0)	I_H			100	µA
Outputs (D, L)		1			mA
(open drain, $V_I = 5$ V)	I_L			10	µA
	I_H				
Counting dead time	t_{dead}			100	ms
Counting response time	t_{resp}			10	ms
Clock Φ	t_H	5		1000	µs
	t_L	5			µs
	t_f	1			µs
Interval start pulse/ trailing edge L	t_{ST}	5			µs
Count input CI	t_{CI}	5			µs
Programming time NVM (per byte)	t_{prog}			10	ms
Programming time NVM (total memory)	t_{prog}	50		100	ms
Blowing of fusible link:					
T0	V_H		17		V
	I_H			100	mA
T1	V_H		17		V
	I_H			10	µA
	t_r			1	µs
	t_s	100			ms

4

DC Characteristics

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics will apply at $T_A = 25$ °C and mean supply voltage.

Block Diagram



a) Programming of NVM

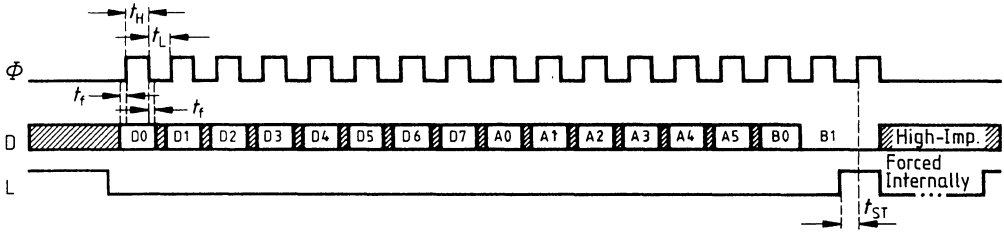


Figure 1a

b) Readout of NVM

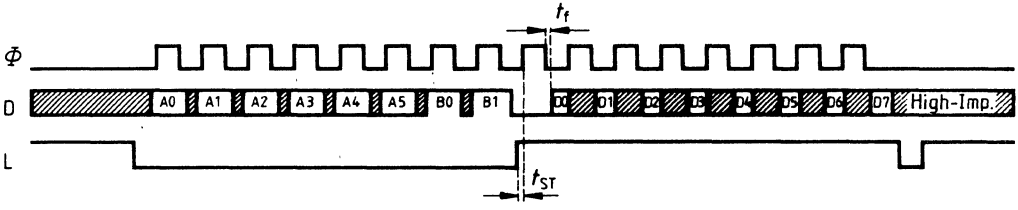


Figure 1b

4

c) Counting Operation

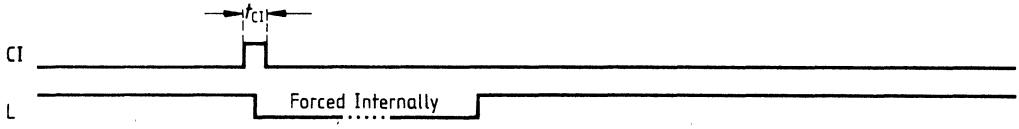


Figure 1c

d) Reading Out Count

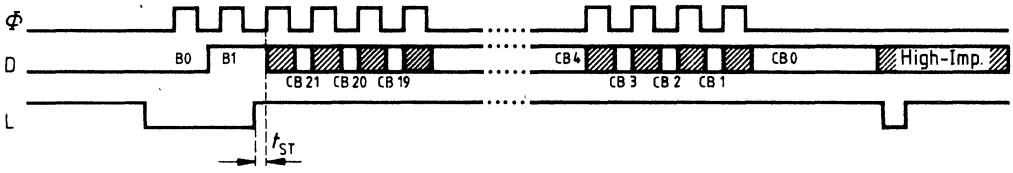


Figure 1d

a) Presetting Count on NC

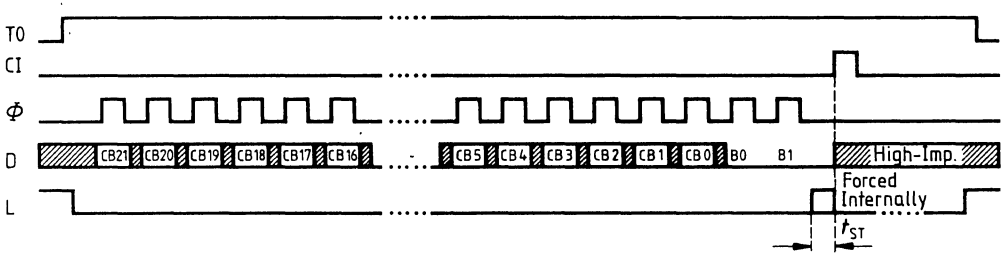


Figure 2a

b) Erasure of Entire NVM

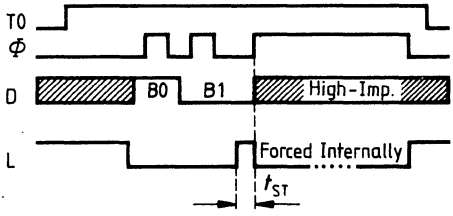


Figure 2b

c) Writing into Entire NVM

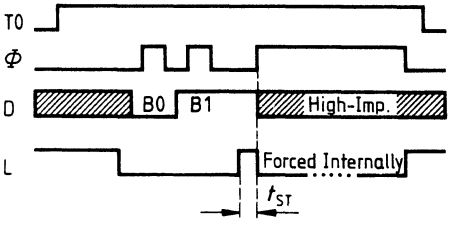


Figure 2c

Application Circuit

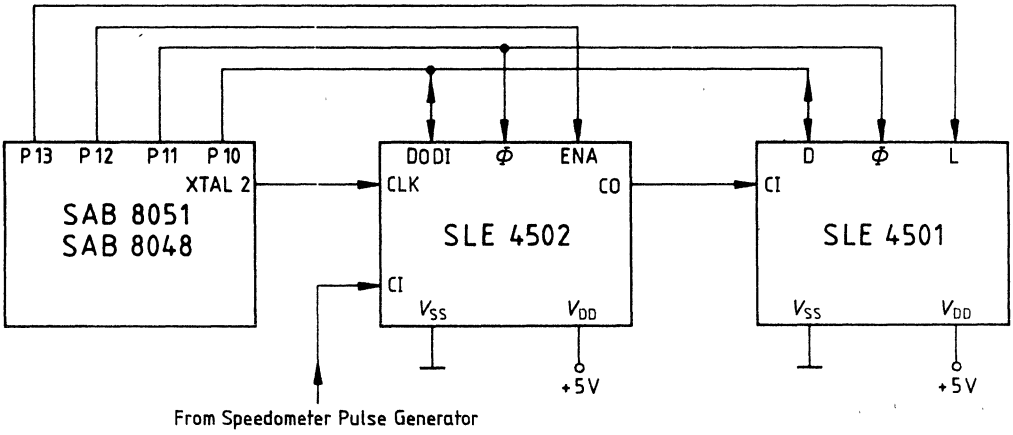


Figure 3

Blowing Fusible Link

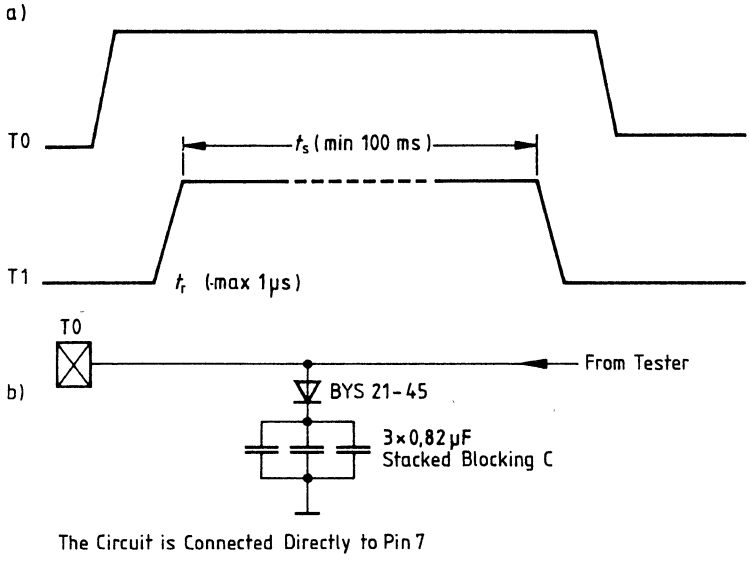


Figure 4

SIEMENS

SLE 4502
Prescaler for Safety Counter

Preliminary Data

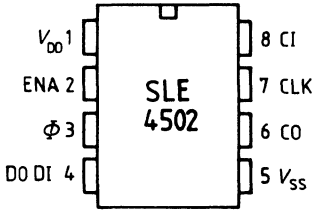
Type	Ordering Code	Package
SLE 4502	Q67100-H8378	P-DIP 8

The SLE 4502 integrated circuit transforms the speed pulses for the SLE 4501 nonvolatile safety counter.

Features

- CMOS technology
- Inputs/outputs protected against latch-up
- NMOS-compatible inputs and outputs
- Standby current (1 µA)
- Schmitt trigger input for counter
- 4-bit miles counter with a programmable prescaler (between 1 and 65000)
- 16-bit register for miles-counter function with external time base
- 16-bit register for trip counter resettable
- Serial three-wire bus
- Power-fail flag
- Extended temperature range: −40...+85 °C

Pin Configuration



Pin Description

Pin	Symbol	Function
1	V_{DD}	Supply voltage +5V
2	ENA	Enable input
3	Φ	Clock input for data input/output
4	DODI	Data output – data input
5	V_{SS}	Supply voltage 0V
6	CO	Counter output
7	CLK	Clock input for IC timing
8	CI	Count pulse input

Edition 3.87

Circuit Description

1. Counter Function

The arriving count pulses are sent to the count output via a programmable 16-bit counter and a fixed 4-bit counter. At a 12-MHz clock frequency, the output pulse width is 10 µs. The contents of the 4-bit counter is readable over the serial interface.

2. Trip Counter

The output pulses of the programmable divider are counted in an additional 16-bit register. This counter is readable and resettable.

3. Speedometer

The clock frequency reaches a 16-bit interval counter, which is programmable in a 16-bit register, over a 5-bit prescaler. The speed pulses are counted during an interval and stored in a latch at the end of the interval. This latch may be read at any time.

4. Power-Fail Flag

Upon an increase in the supply voltage from 0V to 5V a reset is generated. The power-fail flag indicates this condition. The power-fail flag is reset when it is read out.

5. Instruction Code

Function	B3	B2	B1	B0
Program divider factor of miles counter	1	1	0	0
Program divider factor of speedometer	1	0	1	0
Reset trip counter	1	0	0	1
Read out miles counter	0	1	0	0
Read out trip counter	0	0	0	1
Read out speedometer	0	0	1	0
Read out power-fail flag	0	1	1	1

Maximum Ratings

		min.	typ.	max.	Unit
Supply voltage	V_{DD}	−0.3		6	V
Input voltage	V_{IM1}	−0.3		V_{DD} +0.3	V
Power dissipation per output	P_Q			50	mW
Total power dissipation	P_{tot}			150	mW
Storage temperature	T_{stg}	−50		125	°C

Operating Range

Supply voltage	V_{DD}	4.5	5	5.5	V
DC supply currrent	I_{DDS}			1	µA
Supply current (meas. circuit)	I_{DD}			1	mA
Operating frequency	f_{CLK}	1		15	MHz
Ambient temperature	T_A	−40		+85	°C

Maximum Ratings

Maximum ratings are absolute ratings. Exceeding even one of them may result in the destruction of the integrated circuit.

Operating Range

Within the operating range the function mentioned in the circuit description will be fulfilled. Deviations from the characteristics are possible.

Characteristics

$T_A = 25\,°C$

		min.	max.	Unit
All input signals except CI				
H input voltage	V_{IH}	2.2	V_{DD}	V
L input voltage	V_{IL}	0	0.8	V
Input capacitance	C_I		10	pF
L input current	I_{IL}		1	µA
Input signal CI				
H input voltage	V_{IH}	$V_{DD}-1$	V_{DD}	V
L input voltage	V_{IL}	0	1	V
Input capacitance	C_I		10	pF
L input current	I_{IH}		1	µA
Hysteresis	V_H	1	2	V
Output signals				
H output voltage $I_Q = 0.5$ mA	V_{QH}	$V_{DD}-0.4$		V
L output voltage $I_Q = 1.6$ mA	V_{QL}		0.4	V

AC Characteristics

$T_A = 25\,°C$

Clock frequency	f_{CLK}	1	15	MHz
Pulse duration CLK	t_{CLKH}	50	500	ns
Pulse spacing CLK	t_{CLKL}	50	500	ns
Pulse duration Φ	$t_{\Phi H}$	100		ns
Pulse spacing Φ	$t_{\Phi L}$	100		ns
Enable low to Φ	$t_{E\Phi}$	$6/f_{CLK}$		ns
Φ low to enable	$t_{\Phi E}$	50		ns
Data setup	t_S	50		ns
Data hold	t_H	50		ns
Output delay	t_D	50		ns
Enable low to data high-impedance	t_{HZ}	$6/f_{CLK}$		ns
Output pulse width CI	t_{CI}	$128/f_{CLK}$		ns

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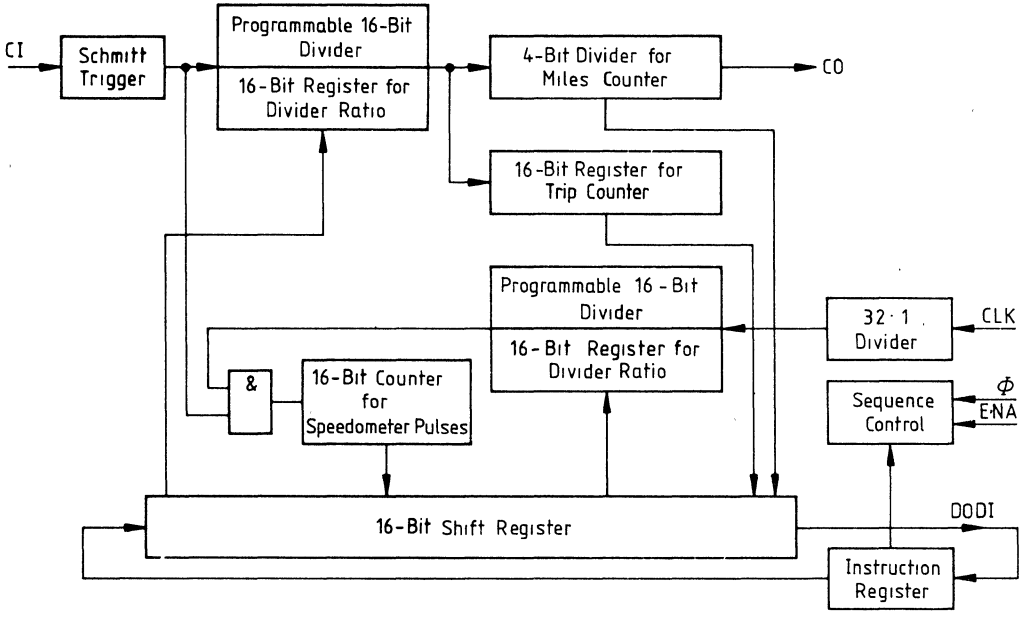
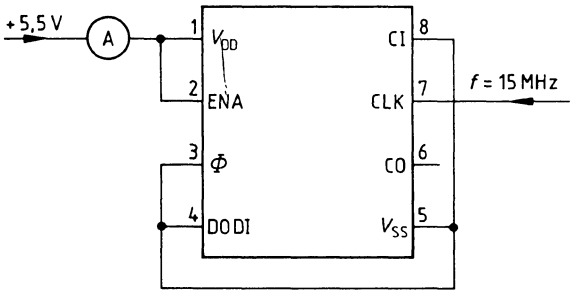
DC Characteristics

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics will apply at $T_A = 25\,°C$ and mean supply voltage.

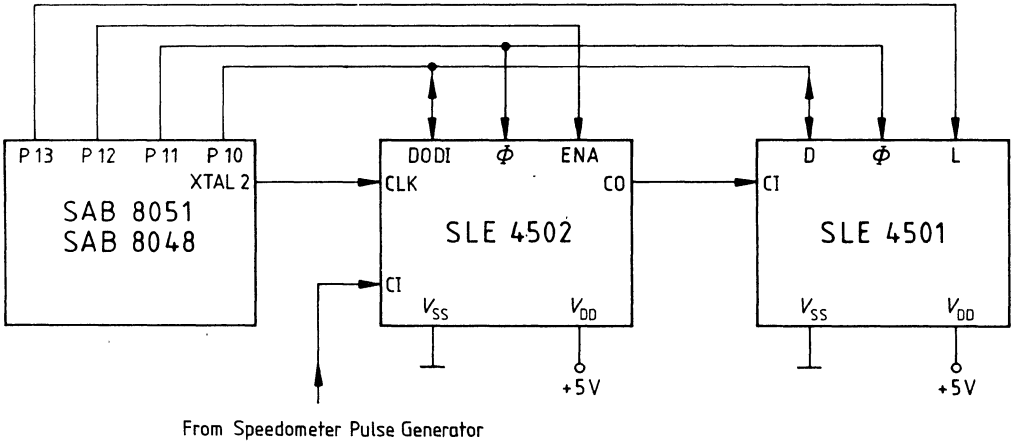
Block Diagram



Measurement Circuit

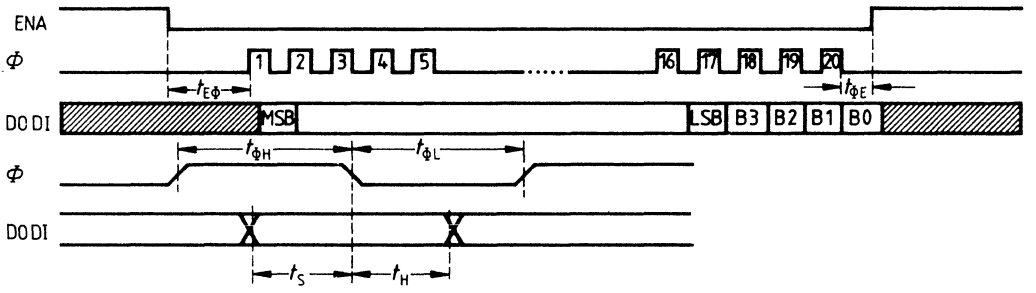


Application Circuit

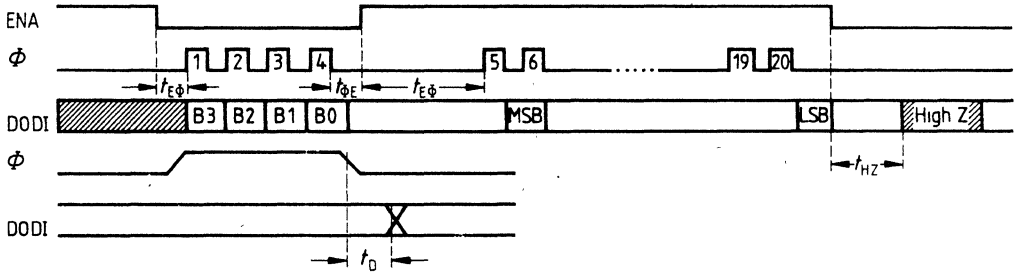


Diagrams

Write



Read



SLE 4520
3 Phase Pulse Width Modulator

- Generation of Three Pairs of Pulse Width Modulated Rectangular Pulses (Phase Angle between One Phase and the Next is, for Example, 120°C) to Drive Six Individual Transistors of an Inverter Power Block
- Programmable Deadtime to Safely Drive Both Power Switches of Half-Bridge from 0 to 15 $\times \frac{6}{f_{crystal}}$ or 15 $\times \frac{4}{f_{crystal}}$ in 15 Steps. The Negative Edge is always Delayed because the Output Signal is Active Low
- Programmable Predivider in the Pulse Width Modulator to Obtain Low Switching Frequencies (for Output Stages with Thyristors, GTOs, and Bipolar Transistors) and at the Same Time to Operate the Microcontroller at Higher Crystal Frequencies
- Direct Drive of an Optocoupler Interface to Isolate Control and Load Circuits (I_{sink} = 20 mA Maximum)
- All Six Outputs of the SLE 4520 are Set to High Level either Dynamically by an Inhibit Signal (INHIBIT) or Statically by an R-S Flipflop (SET STATUS) Thus Blocking of all Six Individual Transistors of the Power Circuit is Possible
- DC Braking by Selecting Different Fixed Duty Cycles in the Three Output Pairs
- Direction of Rotation is Software-Reversed by Changing between Two Phases
- Sine-Wave Frequency Range about 0 Hz to >3,000 Hz
- Switching Frequency Range <1 kHz to >23 kHz
- 8-Bit Resolution of the Desired Sine-Wave Function with a Switching Frequency of $\frac{f_{crystal}}{6 \times 2^8}$ or 7 Bit Resolution with $\frac{f_{crystal}}{6 \times 2^7}$ ($f_{crystal}$ = 12 MHz and Resolution = 7 Bits Result in a 15.6 kHz Switching Frequency)
- Smallest Increment of the Pulse Width is 333 ns with $f_{crystal}$ = 12 MHz and Divider Ratio 1:4
- Changing the Switching Frequency Cycle in 1 µs Steps Allows the Transition from One Sine-Wave Frequency Stage to the Next Quasi Continuously (Virtually Analog)
- Evaluating the Bit Pattern at One Port of the Microcontroller Enables Many (256) Different Speed Control Programs to be Selected
- Low Current Consumption of the Pulse Width Modulator because of ACMOS Technology

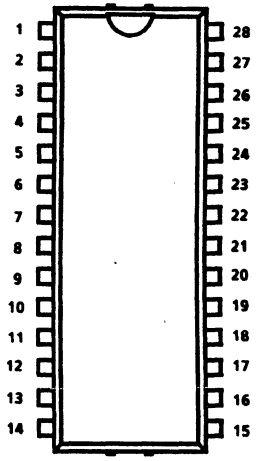
4

- Digital sinus-synthesis for controlling the speed of rotation and the torque of three-phase motors.
- 2-chip solution (e.g. SAB 8051 with SLE 4520) for easy configuration of a powerful frequency converter.
- Motor frequencies from 0 Hz to 3.000 Hz and above with a switching frequency selectable up to 23.4 kHz.
- Adaption to different output stages through a programmable deadtime.
- Functional and performance features determined by dedicated software.

The new pulse width modulator converts an 8-bit data word into a rectangular signal of corresponding width.

Pin Configuration

(Top View)



0151-2

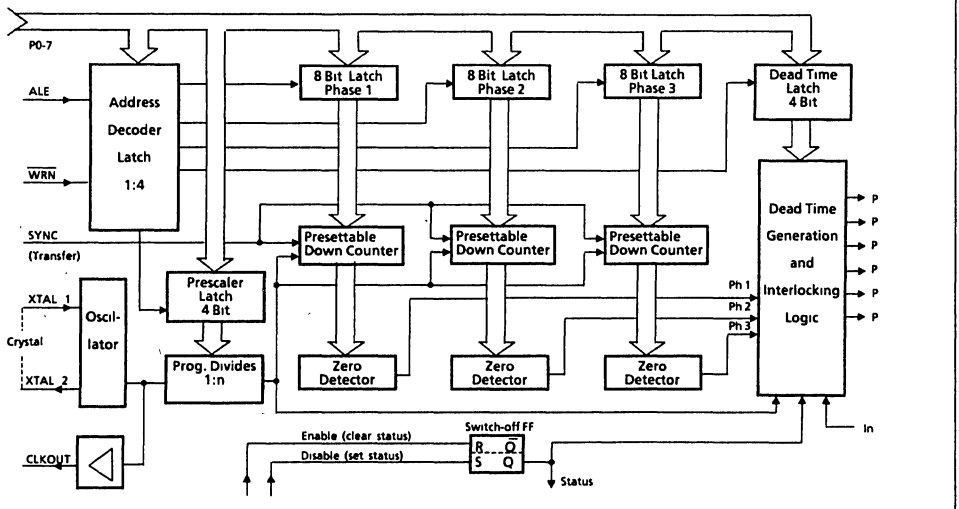
Pin Definitions

Pin	Symbol	Function
1	V_{DD}	+5V Connection
2	XTAL1	Crystal Connection
3	XTAL2	Crystal Connection
4	P7	Data Bus Connections (Inputs)
5	P6	
6	P5	
7	P4	
8	P3	
9	P2	
10	P1	
11	P0	
12	PH3/2	Output Phase 3 Inverted
13	PH3/1	Output Phase 3 Normal (Active Low)
14	PH2/2	Output Phase 2 Inverted
15	V_{SS}	Ground Connecting
16	PH2/1	Output Phase 2 Normal (Active Low)
17	PH1/2	Output Phase 1 Inverted
18	PH1/1	Output Phase 1 Normal (Active Low)
19	INHIBIT	Inhibit (Active High) Sets All Phase Outputs to High
20	STATUS	Output of Status Flipflop
21	CLEAR STATUS	Resets Status Flipflop
22	SET STATUS	Sets Status Flipflop
23	RES	Chip Reset
24	$\overline{WR}$	Input for $\overline{WR}$ Pulse from Microcontroller
25	ALE	Input for ALE Clock from Microcontroller
26	CS	Chip Select
27	SYNC	Input for Trigger Pulse from Microcontroller
28	CLK OUT	Output Crystal Frequency for Microcontroller

Three independently operating channels consisting of a latch, loadable counter and zero detector are used for this purpose. Together with a microcontroller (e.g. SAB 8051) and suitable software, pulses are generated to drive AC converters and inverters (three-phase) with an almost unlimited range of waveforms (sinusoidal, triangular) and phase relationships. An oscillator with clock output, a programmable prescaler to adapt the switching frequency to the requirements of the output stage, an interlocking stage with status flipflop and the ability to program deadtimes are features that recommend the SLE 4520 for use in frequency converters to drive three-phase induction motors.

Speed control of three-phase motors is easily done when such motors are supplied with a three-phase voltage of which the U/f ratio is kept almost constant with variable frequency. To generate this three-phase voltage a frequency converter is required to rectify and filter the AC supply voltage and subsequently reconvert it into an AC voltage of different frequency by a drive circuit and three power half-bridges. To avoid high losses the output stages operate in a switched mode and are driven by rectangular pulses which increase or decrease in width, depending on the waveform of the sinusoidal function. To produce such pulses with a repetition frequency (switching frequency) up to the limit of the audible range, a drive block consisting of the SAB 8051 microcontroller and the SLE 4520 PWM as a minimum configuration proves to be best suited to the job.

Block Diagram



Principle of Function

The combination of the SLE 4520 and the SAB 8051 microcontroller are described here. Other hardware combinations are in general possible.

Oscillator on-chip feeds the programmable prescaler and has a buffered output for the connected microcontroller. Interface to microcontroller has a width of 8 bits.

Data from the SAB 8051 μC to the SLE 4520 PWM are transferred via the data bus P0 using control signals ALE and $\overline{WR}$. Three 8-bit registers for the three phases and two 4-bit registers to preset deadtime and prescaler ratios, as well as an address decoder latch to buffer particular addresses, are connected to the internal data bus of the SLE 4520 (see block diagram).

Addresses are as follows:

Address	Register
00	8-Bit Register for Phase 1
01	8-Bit Register for Phase 2
02	8-Bit Register for Phase 3
03	Deadtime Control Register
04	Divider Control Register

The last two registers have to be written only once when initialized. In the case of a controller output the above mentioned 3-bit address is latched and decoded with the falling edge of the ALE clock. With the rising edge of the $\overline{WR}$ signal data are loaded from the bus into the registers of the pulse width modulator. Divider ratio is selected by divider control register.

To produce low switching frequencies with a simultaneously high microcontroller operating frequency the divider control register is loaded in the initial routine with an appropriate number. Allocation of value and divider ratio is shown in Table 1.

Table 1. Allocation of Value in the Divider Register to the Divider Ratio by Which the SLE 4520 Operating Frequency is Selected

Value	Divider Ratio Counter	Divider Ratio Delay Clock
0	1:4	1:4
1	1:6	1:6
2	1:8	1:4
3	1:12	1:6
4	1:16	1:4
5	1:24	1:6
6	1:32	1:4
7	1:48	1:6

The switching cycle should be selected after the ratio is fixed so as to barely reach the maximum pulse width. This means that with a PWM counter clock of, e.g. 1 MHz (oscillator frequency of 12 MHz, divider ratio 1:12) and a table value of 127 (7 bits) the counter reaches zero after 128 μs (switching frequency cycle 128 μs). Table 2 gives a number of useful allocations of counter and switching frequencies for the SAB 8051 (12 MHz clock).

Table 2. Allocation of Counter Frequency and Switching Frequency of SAB 8051

Divider Ratio	Counter Frequency	Operating Time Timer 0	Switching Frequency	Resolution
1:6	2 MHz	64 µs	15.6 kHz	7-Bit
1:6	2 MHz	128 µs	7.8 kHz	8-Bit
1:12	1 MHz	128 µs	7.8 kHz	7-Bit
1:12	1 MHz	256 µs	3.9 kHz	8-Bit
1:24	500 kHz	256 µs	3.9 kHz	7-Bit
1:24	500 kHz	2 x 256 µs	1.95 kHz	8-Bit
1:48	250 kHz	2 x 256 µs	1.95 kHz	7-Bit
1:48	250 kHz	4 x 256 µs	975 Hz	8-Bit

Converting a Data Word into a Pulse Width

Pulse generation in the three processing channels is done by a presettable 8-bit downcounter and a zero detector (NOR gate) which is connected to the eight counter outputs. With the trigger pulse from the microcontroller (which is one instruction cycle) whose repetition rate determines the switching frequency, the presettable counter is loaded with the contents of the appropriate register and 0 appears at the zero detector's output (provided the register does not contain 00H).

This 0 digit enables the counter and starts it running down. When zero is reached the pulse ends and the counter is stopped until the next transfer pulse arrives. The crystal frequency multiplied by the divider ratio clocks the PWM counter.

Selecting Deadtime by Presetting Control Register to Avoid Overlapping Switching Operations

Deadtime is defined as the period of time between switching on one of the half-bridge transistors while the other switches off, and vice versa, to obviate dangerous overlapping of switching operations ("shoot-through"). In the pulse width modulator the dead time is obtained by linking the pulse width modulated source signal and its delayed signal. The delay is obtained by passing the source signal through a 15-bit shift register with 15 outputs.

The shift pulse is either $\frac{f_{crystal}}{6}$ or $\frac{f_{crystal}}{4}$, depending on the contents of the divider control register.

16 deadtimes are presettable (including zero deadtime) by writing a value between 0 and 0FH into the appropriate control register.

Deadtime depends on the crystal frequency and the preset divider ratio (1:4 or 1:6). For a 12 MHz crystal frequency the programmable deadtimes are given in Table 3.

Table 3. Deadtime Presettable in the Deadtime Register Using Divider Ratios of 1:4 and 1:6

Word in Deadtime Memory	Divider Ratio 1:4 Deadtime (µs)	Divider Ratio 1:6 Deadtime (µs)
0	0	0
1	0.33	0.5
2	0.66	1
3	1.0	1.5
4	1.33	2
5	1.66	2.5
6	2.0	3
7	2.33	3.5
8	2.66	4
9	3.0	4.5
10	3.33	5
11	3.66	5.5
12	4.0	6
13	4.33	6.5
14	4.66	7
15	5.0	7.5

Interface to the Power Circuit Provided by Outputs PH1/1 to PH3/2

Without deadtime PH1/2 is inverted to PH1/1, PH2/2 to PH2/1 and PH3/2 to PH3/1. The active switching state is low.

With a programmed deadtime the negative edges of the output signal are shifted to the right by the deadtime.

The outputs are capable of directly driving TTL devices or optocouplers for voltage isolation of drive blocks and power circuits with currents up to 20 mA.

Static or Dynamic Interlocking of Outputs is Possible

All outputs are set to high level during the inhibit signal (Pin 19). Hence, the light emitting diodes of the connected optocouplers are currentless and all six individual transistors of the power circuit are blocked. This option is particularly needed when switching on the drive block, as proper pulses at the pulse width modulator output are only available after the oscillator output has set up and the initialization routine has been executed.

As the SAB 8051 sets the port outputs to high when switched on, only one port pin of the microcontroller has to be connected to inhibit. At the end of the initialization routine this port pin is set to low. Another way of inhibiting the outputs (hold function) is to apply a high pulse to the Set input (Pin 22) of the status flipflop. This inhibit state is indicated by the "Status" output (Pin 20) and can be used to indicate or inform the microcontroller (active high; used, for example, in the event of power failure, short circuit, excess temperature, etc.).

The status flipflop is cleared by a high pulse at the "Clear Status" input (Pin 21).

Absolute Maximum Ratings*

Maximum ratings are absolute ratings. Exceeding even one of them may result in the destruction of the integrated circuit.

Pos	Parameter	Symbol	Min	Max	Units
1	Storage Temperature	T_S	−50	+125	°C
2	Total Power Dissipation	P_{tot}		500	mW
3	Power Dissipation per Output	P_O		50	mW
4	Input Voltage	V_{IN}	−0.3	V_{DD} + 0.3	V
5	Supply Voltage	V_{DD}	−0.3	6	V

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Operating Range

Within the operating range the functions mentioned in the circuit description will be fulfilled. Deviations from the characteristics are possible.

Pos	Parameter	Symbol	Min	Typ	Max	Units
1	Supply Voltage	V_{CC}	4.5	5	5.5	V
2	Supply Current (Outputs Not Connected)	I_{DD}			15	mA
3	Operating Frequency	f_{CLK}			12	MHz
4	Ambient Temperature	T_A	−40		+85	°C

D.C. Characteristics

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics will apply at T_A = 25°C and mean supply voltage.

Pos	Parameter	Symbol	Conditions	Min	Typ	Max	Units
All Input Signals Except XTAL 2							
1	H-Input Voltage	V_{IH}		2.2		V_{DD}	V
2	L-Input Voltage	V_{IL}		0		0.8	V
3	Input Capacitance	C_I				10	pF
4	Input Current	I_{IL}				1	µA

D.C. Characteristics

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics will apply at T_A = 25°C and mean supply voltage. (Continued)

Pos	Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input Signal XTAL2 for External Clock							
5	H-Input Voltage	V_{IH}		4.0		V_{DD}	V
6	L-Input Voltage	V_{IL}		0		0.3	V
7	Input Capacitance	C_I				10	pF
8	Input Current	I_{IL}				1	µA
Output Signals STATUS, Clockout							
9	H-Output Voltage	V_{OH}	I_O = 0.5 mA	V_{DD} − 0.8			V
10	L-Output Voltage	V_{OL}	I_O = 1.6 mA			0.4	V
Output Signals PH1/1, PH1/2, PH2/1, PH2/2, PH3/1, PH3/2							
11	L-Output Voltage	V_{OL}	I_O = 20 mA			1	V
12	H-Output Voltage	V_{OH}	I_O = 1 mA	V_{DD} − 0.8		V_{DD}	V

A.C. Characteristics

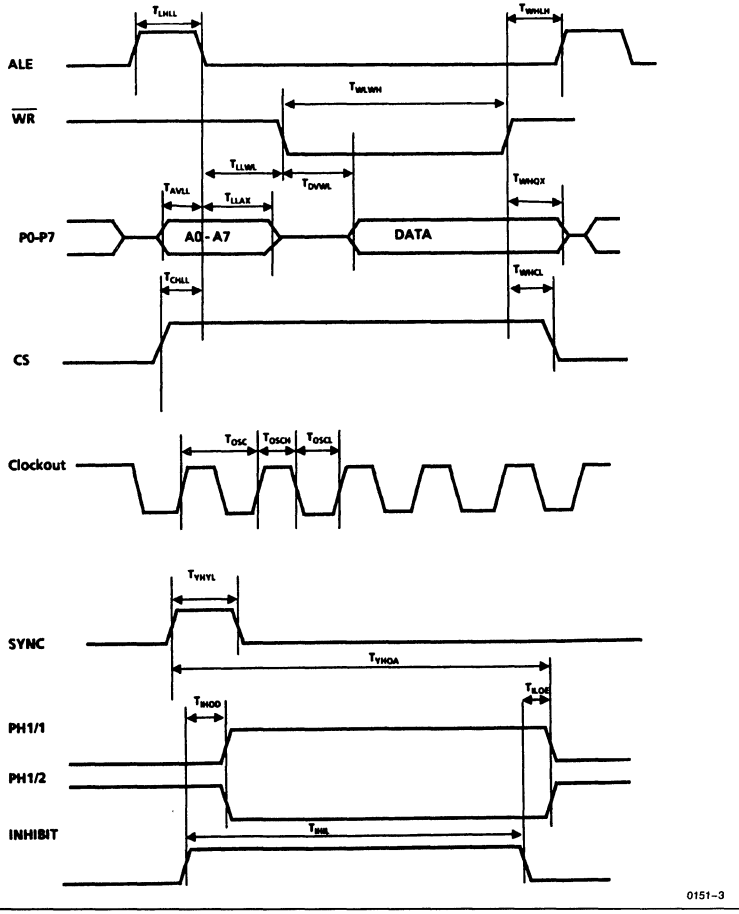
Parameter	Symbol	Min	Max	Units
ALE Pulse Width	T_{LHLL}	100		ns
Address Setup to ALE	T_{AVLL}	30		ns
Address Hold after ALE	T_{LLAX}	30		ns
WRN Pulse Width	T_{WLWH}	200		ns
WRN High to ALE High	T_{WHLH}	50		ns
Data Setup after WRN Low	T_{DVWL}	20		ns
ALE Low to WRN Low	T_{LLWL}	100		ns
Data Hold after WRN*	T_{WHQX}	30		ns
Oscillator Period	T_{OSC}	83		ns
High Time	T_{OSCH}	35		ns
Low Time	T_{OSCL}	35		ns
SYNC Pulse Width	T_{YHYL}	200		ns
INHIBIT Low to Output Enable	T_{ILOE}		100	ns
Delay between SYNC High to Output Active	T_{YHOA}	4 T_{OSC}	97 T_{OSC} + 20	ns
Chip Select Setup to ALE Low	T_{CHLL}	20		ns
Chip Select Hold after WRN High	T_{WHCL}	30		ns
Reset Pulse Width	T_{RHRL}	12 T_{OSC}		ns
Set Status Pulse Width	T_{SHSL}	200		ns
Clear Status Pulse Width	T_{CHCL}	200		ns

A.C. Characteristics (Continued)

Parameter	Symbol	Min	Max	Units
INHIBIT High to Output Disable	T_{IHOD}		100	ns
Set Status High to Output Disable	T_{SHOD}		100	ns
Clear Status High to Output Enable	T_{CHOD}		100	ns
Set Status Pulse Length	T_{SHTH}	100		ns
Clear Status Pulse Length	T_{CHTL}	100		ns
Inhibit Pulse Length	T_{IHIL}	100		ns

*If T_{WLWH} shorter as 2 T_{OSC} + 20 ns, then T_{WHQX} is 50 ns.

Pulse Diagram



Ordering Information

Type	Ordering Code	Package
SLE 4520	Q 67100-H 8271	DIP 28

SIEMENS

TCA 785
Phase Control

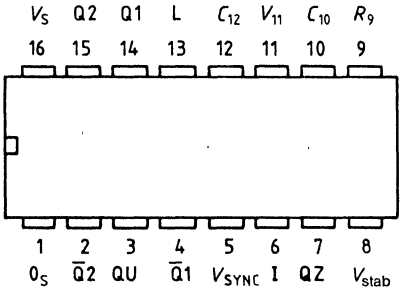
This phase control IC is intended to control thyristors, triacs, and transistors. The trigger pulses can be shifted within a phase angle between 0° and 180°. Typical applications include converter circuits, AC controllers and three-phase current controllers.

This IC replaces the previous types TCA 780 and TCA 780 D

Features

- Reliable recognition of zero passage
- Large application scope
- May be used as zero point switch
- LSL compatible
- Three-phase operation possible (3 ICs)
- Output current 250 mA
- Large ramp current range
- Large temperature range

Pin configuration
top view



Pin No.	Symbol	Function
1	0_S	Ground
2	$\overline{Q}2$	Output 2 inverted
3	QU	Output U
4	$\overline{Q}1$	Output 1 inverted
5	V_{SYNC}	Synchronous voltage
6	I	Inhibit
7	QZ	Output Z
8	V_{stab}	Reference voltage
9	R_9	Ramp resistance
10	C_{10}	Ramp capacitance
11	V_{11}	Control voltage
12	C_{12}	Pulse extension
13	L	Long pulse
14	Q1	Output 1
15	Q2	Output 2
16	V_S	Supply voltage

Functional description

The synchronization signal is obtained via a high-ohmic resistance from the line voltage (voltage V_5). A zero voltage detector evaluates the zero passages and transfers them to the synchronization register.

This synchronization register controls a ramp generator the capacitor C_{10} of which is charged by a constant current (determined by R_9). If the ramp voltage V_{10} exceeds the control voltage V_{11} (triggering angle φ), a signal is processed to the logic. Dependent on the magnitude of the control voltage V_{11}, the triggering angle φ can be shifted within a phase angle of 0° to 180°.

For every half wave, a positive pulse of approx. 30 µs duration appears at the outputs Q1 and Q2. The pulse duration can be prolonged up to 180° via a capacitor C_{12}. If pin 12 is connected to ground, pulses with a duration between φ and 180° will result.

Outputs $\overline{Q}1$ and $\overline{Q}2$ supply the inverse signals of Q1 and Q2.

A signal of $\varphi + 180°$ which can be used for controlling an external logic, is available at pin 3.

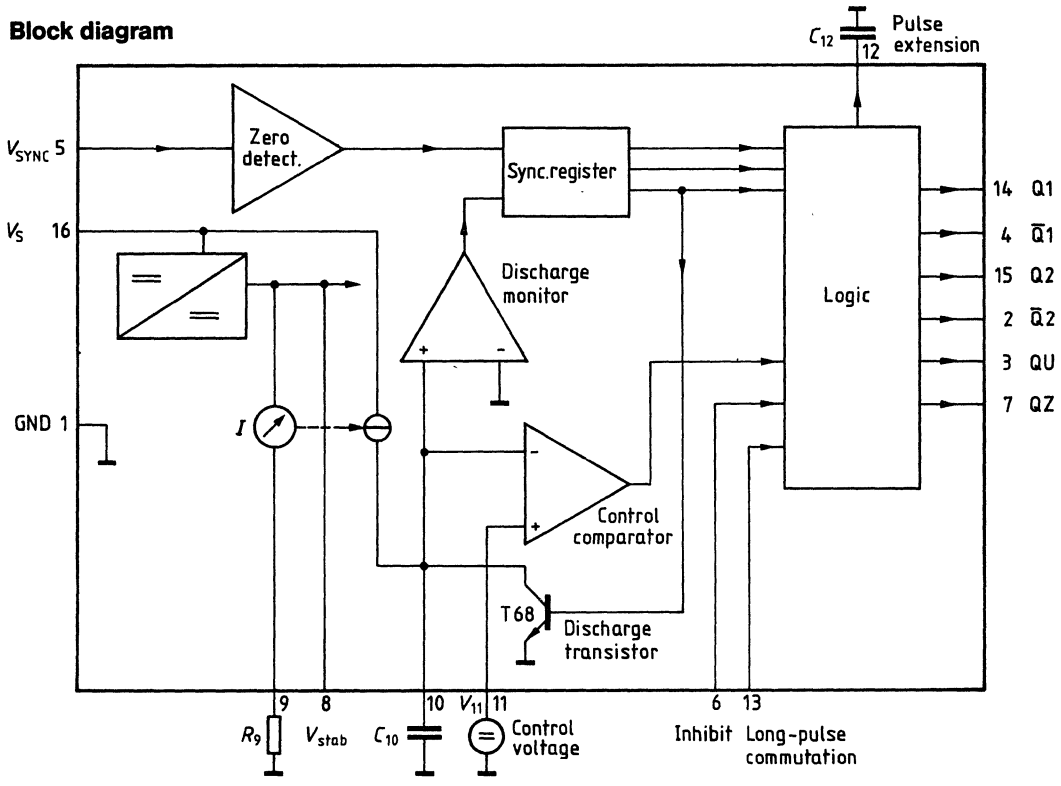
A signal which corresponds to the NOR link of Q1 and Q2 is available at output QZ (pin 7).

The inhibit input can be used to disable outputs Q1, Q2, $\overline{Q}1$, $\overline{Q}2$, QU.

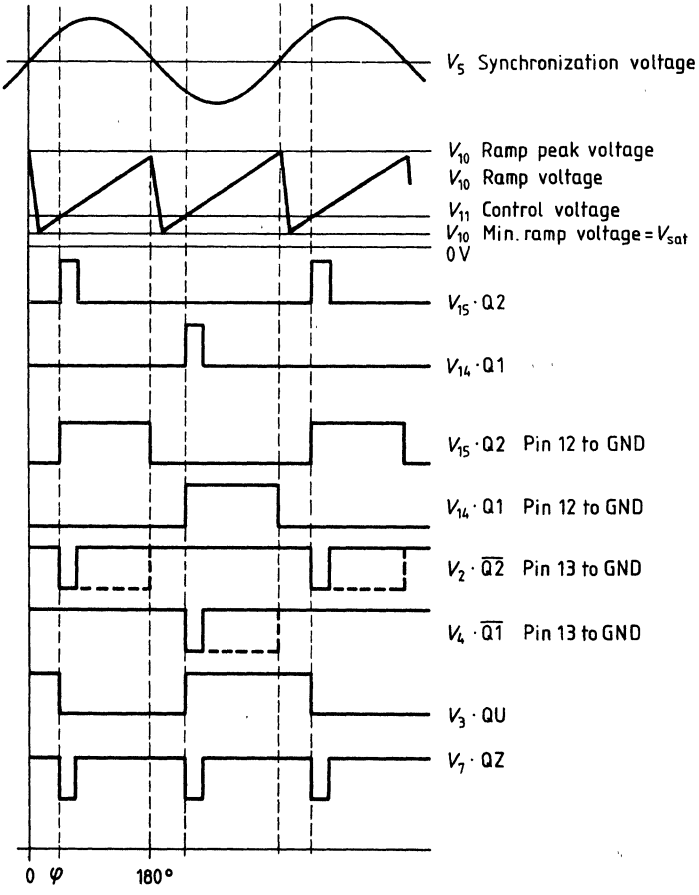
Pin 13 can be used to extend the outputs $\overline{Q}1$ and $\overline{Q}2$ to full pulse length (180° – φ).

4

Block diagram



Pulse diagram



Maximum ratings

		Lower limit B	Upper limit A	
Supply voltage	V_S	−0.5	18	V
Output current at pin 14, 15	I_Q	−10	400	mA
Inhibit voltage	V_6	−0.5	V_S	V
Control voltage	V_{11}	−0.5	V_S	V
Voltage short-pulse circuit	V_{13}	−0.5	V_S	V
Synchronization input current	I_5	−200	± 200	µA
Output voltage at pin 14, 15	V_Q		V_S	V
Output current at pin 2, 3, 4, 7	I_Q		10	mA
Output voltage at pin 2, 3, 4, 7	V_Q		V_S	V
Junction temperature	T_j		125	°C
Storage temperature	T_{stg}	−55	125	°C
Thermal resistance (system-air)	$R_{th\,SA}$		80	K/W

Operating range

Supply voltage	V_S	8	18	V
Operating frequency	f	10	500	Hz
Ambient temperature range	T_{amb}	−25	85	°C

4

Characteristics $8 \leq V_S \leq 18$ V; $-25\,°C \leq T_{amb} \leq 85\,°C$; $f = 50$ Hz		Test circuit No.	Lower limit B	$f = 50$ Hz $V_S = 15$ V typ	Upper limit A	
Supply current consumption S 1...S 6 open $V_{11} = 0$ V $C_{10} = 47$ nF; $R_9 = 100$ kΩ	I_S	1	4.5	6.5	10	mA
Synchronization pin 5						
Input current R_2 varied	$I_{5\,rms}$	1	30		200	µA
Offset voltage	ΔV_5	4		30	75	mV
Control input pin 11						
Control voltage range	V_{11}	1	0.2		$V_{10\,peak}$	V
Input resistance	R_{11}	5		15		kΩ
Ramp generator						
Load current	I_{10}		10		1000	µA
Max. ramp voltage	V_{10}	1			$V_S - 2$	V
Saturation volt. at capacitor	V_{10}	1.6	100	225	350	mV
Ramp resistance	R_9	1	3		300	kΩ
Sawtooth return time	t_f	1		80		µs
Inhibit pin 6 switch-over of pin 7						
Outputs disabled	V_{6L}	1		3.3	2.5	V
Outputs enabled	V_{6H}	1	4	3.3		V
Signal transition time	t_r	1	1		5	µs
Input current $V_6 = 8$ V	I_{6H}	1		500	800	µA
Input current $V_6 = 1.7$ V	$-I_{6L}$	1	80	150	200	µA
Deviation of I_{10} $R_9 = $ const. $V_S = 12$ V; $C_{10} = 47$ nF	I_{10}	1	−5		5	%
Deviation of I_{10} $R_9 = $ const. $V_S = 8$ to 18 V	I_{10}	1	−20		20	%
Deviation of the ramp voltage between 2 following half-waves. $V_S = $ const.	$\Delta V_{10\,max}$			± 1		%

Characteristics $8 \leq V_S \leq 18$ V; $-25\,°C \leq T_{amb} \leq 85\,°C$; $f = 50$ Hz		Test circuit No.	Lower limit B	$f = 50$ Hz $V_S = 15$ V typ	Upper limit A	
Long pulse switch-over pin 13 switch-over of S 8						
Short pulse at output	$V_{13\,H}$	1	3.5	2.5		V
Long pulse at output	$V_{13\,L}$	1		2.5	2	V
Input current $V_{13} = 8$ V	$I_{13\,H}$	1			10	µA
Input current $V_{13} = 1.7$ V	$-I_{13\,L}$	1	45	65	100	µA
Outputs pin 2, 3, 4, 7						
Reverse current $V_Q = V_S$	I_{CE0}	2.6			10	µA
Saturation voltage $I_Q = 2$ mA	V_{sat}	2.6	0.1	0.4	2	V
Outputs pin 14, 15						
H output voltage $-I_Q = 250$ mA	$V_{14/15\,H}$	3.6	V_S–3	V_S–2.5	V_S–1.0	V
L output voltage $I_Q = 2$ mA	$V_{14/15\,L}$	2.6	0.3	0.8	2	V
Pulse width (short pulse) S 9 open	t_p	1	20	30	40	µs
Pulse width (short pulse) with C_{12}	t_p	1	530	620	760	µs/nF
Internal voltage control						
Reference voltage	V_{ref}	1	2.8	3.1	3.4	V
Parallel connection of 10 ICs possible						
TC of reference voltage	α_{ref}	1		2×10^{-4}	5×10^{-4}	1/K

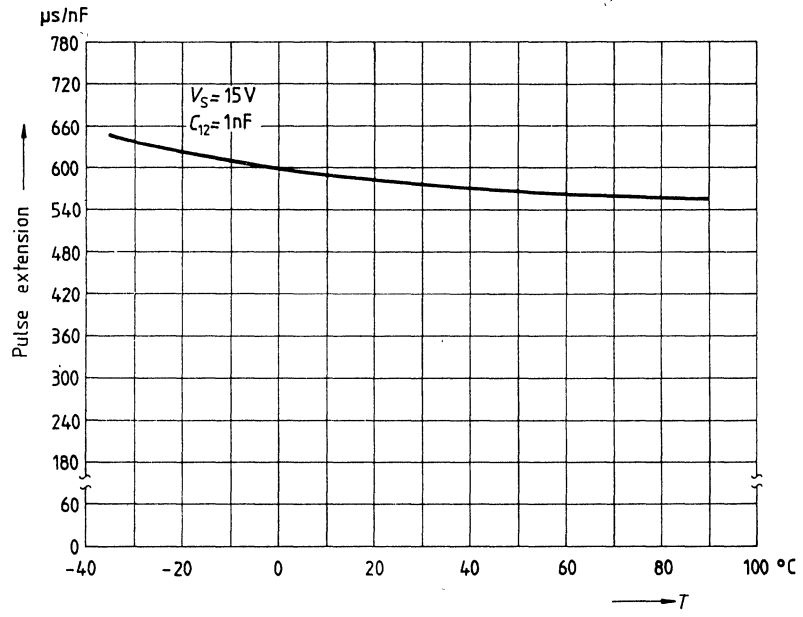
Application hints for external components

		min	max	
Ramp capacitance	C_{10}	500 pF	1 µF[1]	The minimum and maximum values of I_{10} are to be observed
Triggering point	$t_{Tr} = \frac{V_{11} \times R_9 \times C_{10}}{V_{ref} \times K}$		[2]	
Charging current	$I_{10} = \frac{V_{ref} \times K}{R_9}$		[2]	Ramp voltage $V_{10\,max} = V_S - 2$ V $V_{10} = \frac{V_{ref} \times K \times t}{R_9 \times C_{10}}$ [2]

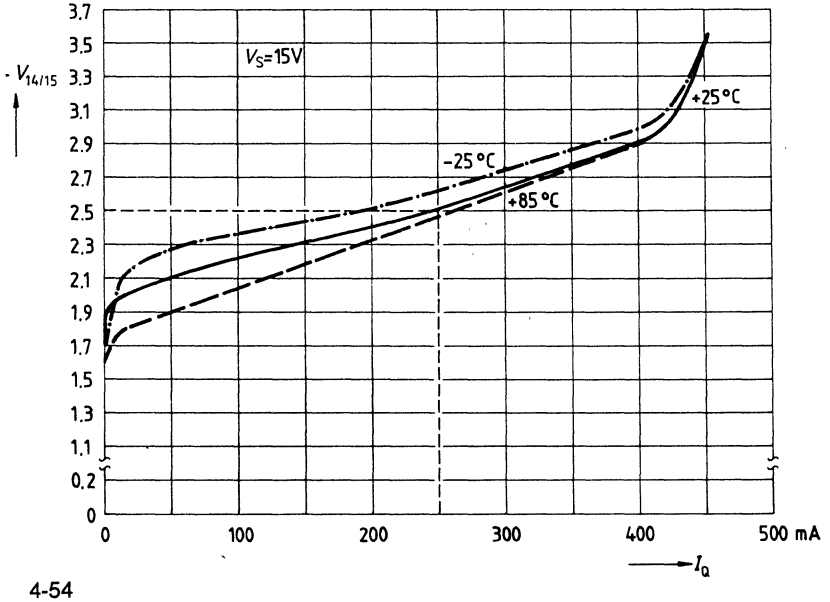
1) Attenuation to flyback times

2) $K = 1.10 \pm 20\%$

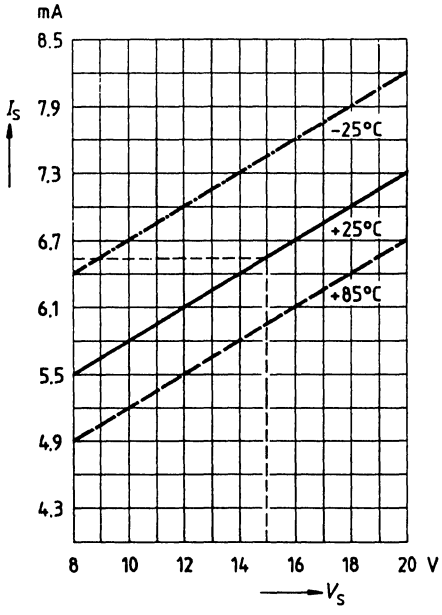
Pulse extension versus temperature



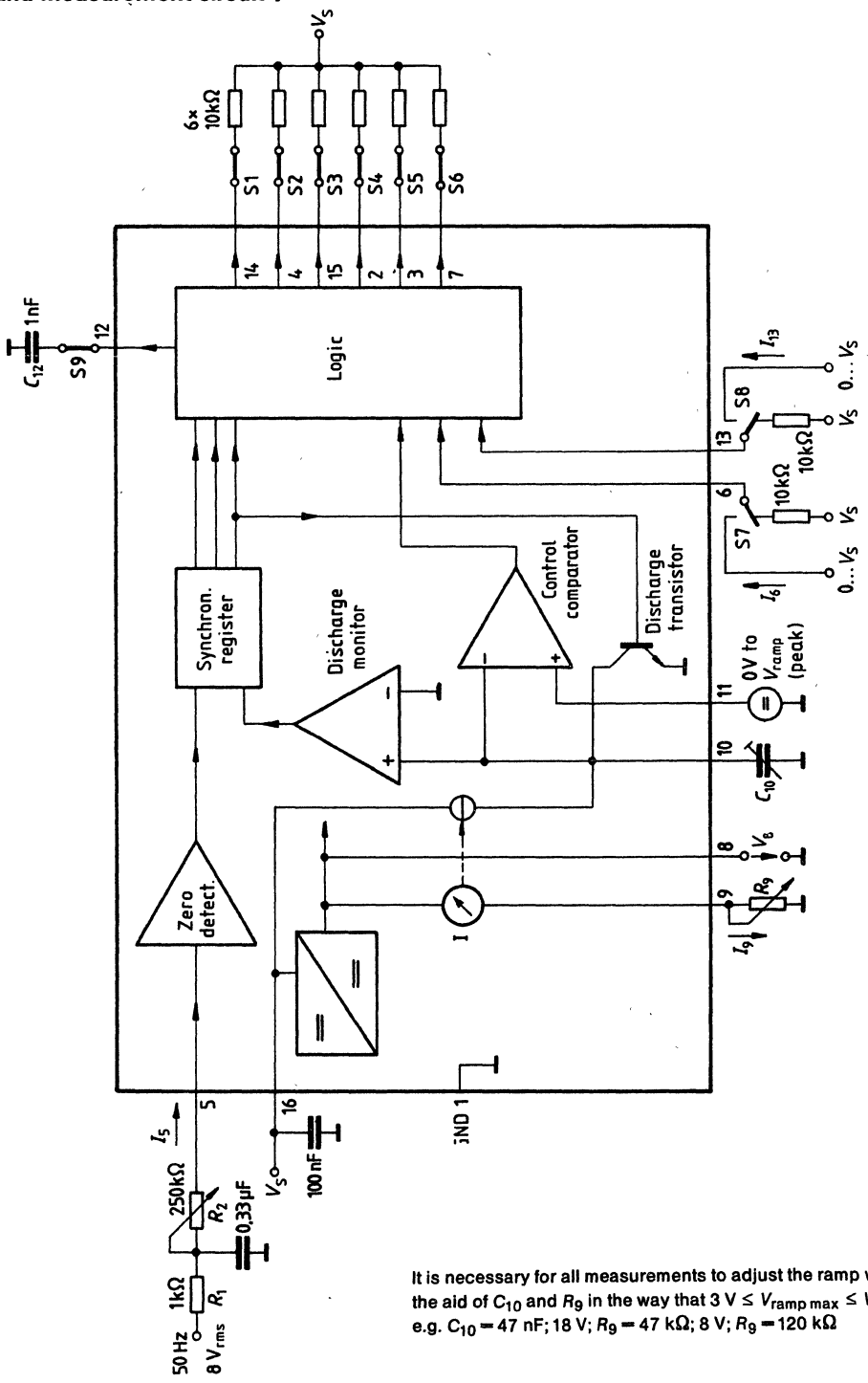
Output voltage measured to $+V_S$



Supply current versus supply voltage



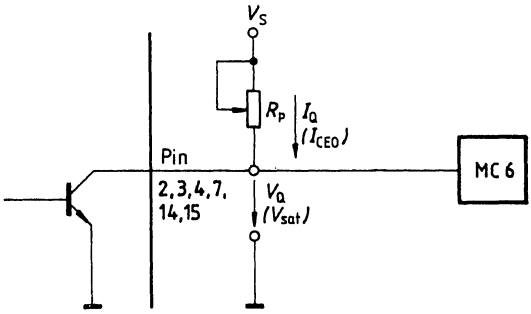
Test and measurement circuit 1



It is necessary for all measurements to adjust the ramp with the aid of C_{10} and R_9 in the way that $3\,V \leq V_{ramp\,max} \leq V_S - 2\,V$
e.g. $C_{10} = 47$ nF; 18 V; $R_9 = 47$ kΩ; 8 V; $R_9 = 120$ kΩ

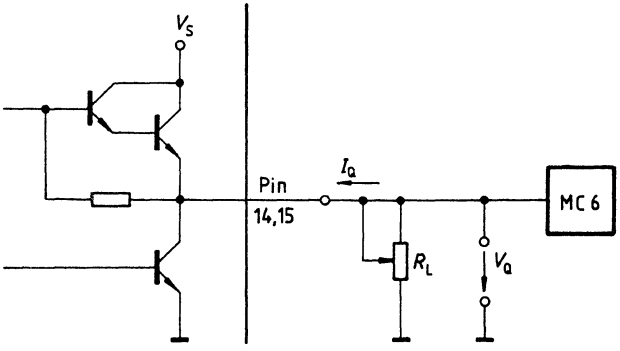
Test and measurement circuits

Measurement circuit 2



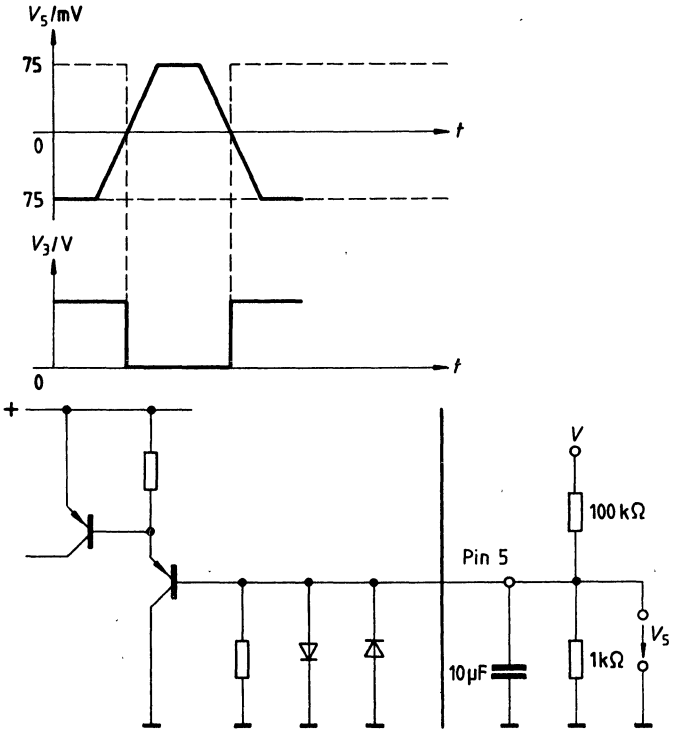
The residual pins are connected as in measurement circuit 1

Measurement circuit 3



The residual pins are connected as in measurement circuit 1

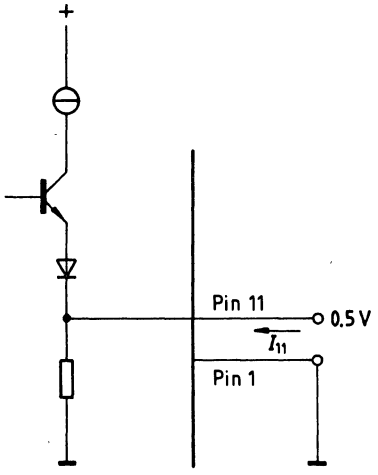
Measurement circuit 4



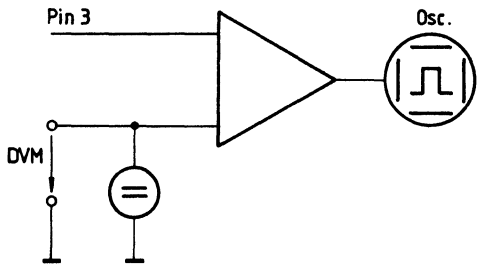
Residual pins are connected as in measurement circuit 1

The 10 µF capacitor at pin 5 serves only for test purposes

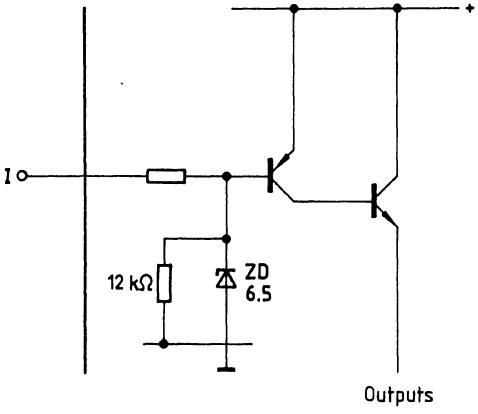
Measurement circuit 5



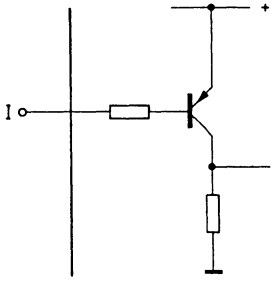
Measurement circuit 6



Inhibit 6



Long pulse 13



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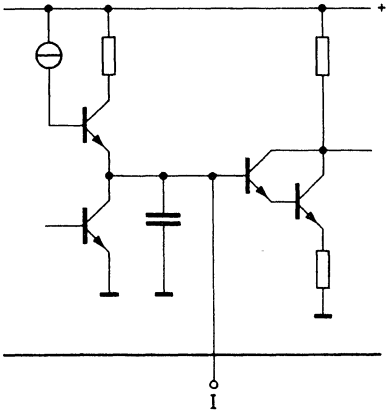
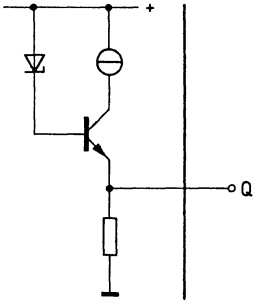
Pulse extension 12



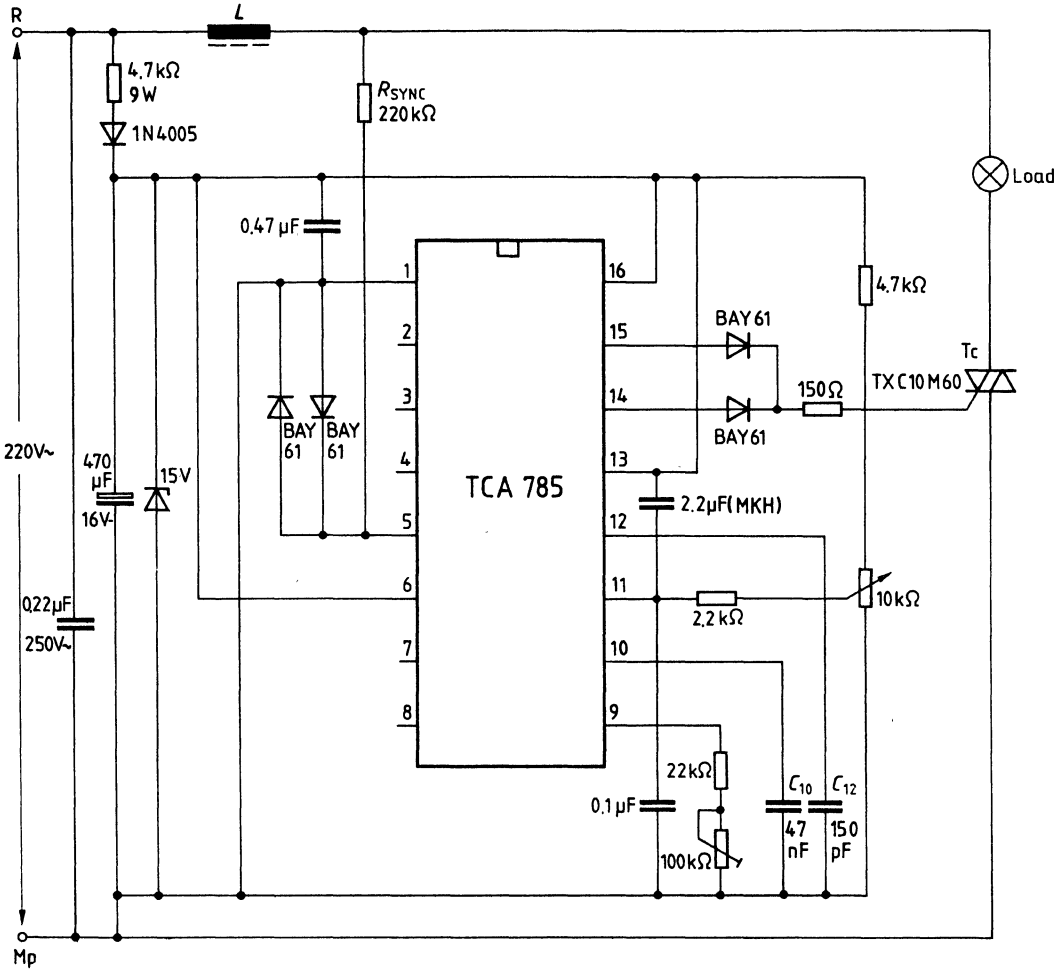
Reference voltage 8



Additional circuit description

Application examples

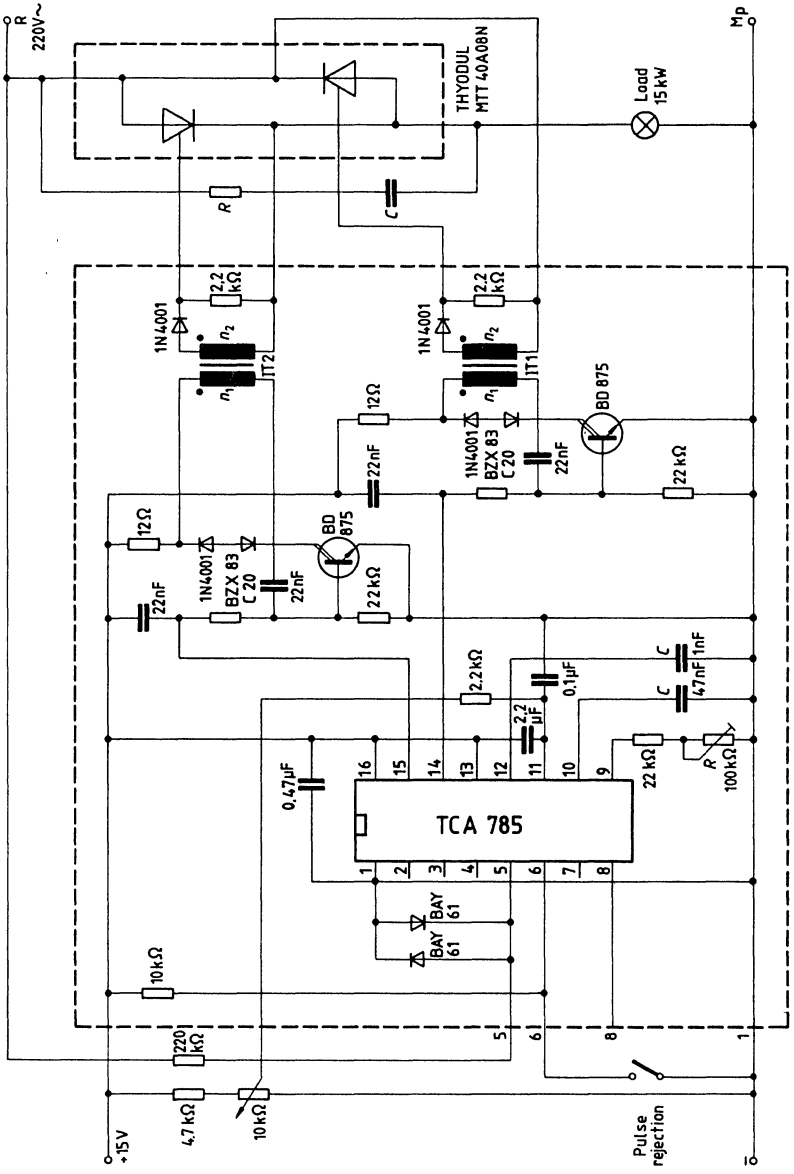
Triac control for up to 50 mA gate trigger current



A phase control with a diretly controlled triac is shown in the figure. The triggering angle of the triac can be adjusted continuously between 0° and 180° with the aid of an external potentiometer. During the positive half wave of the line voltage, the triac receives a positive gate pulse from the IC output pin 15. During the negative half wave, it receives also a positive trigger pulse from pin 14. Trigger pulse width is approx. 100 µs.

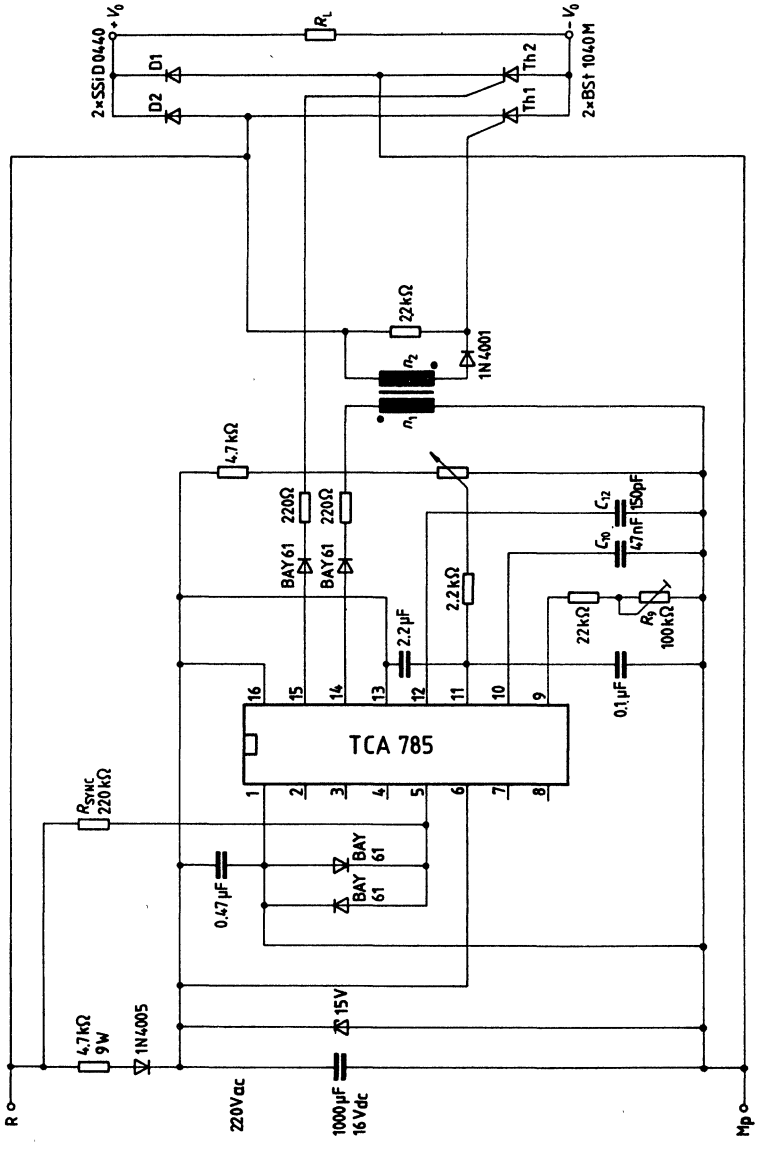
Fully controlled AC power controller

Circuit for two high-power thyristors

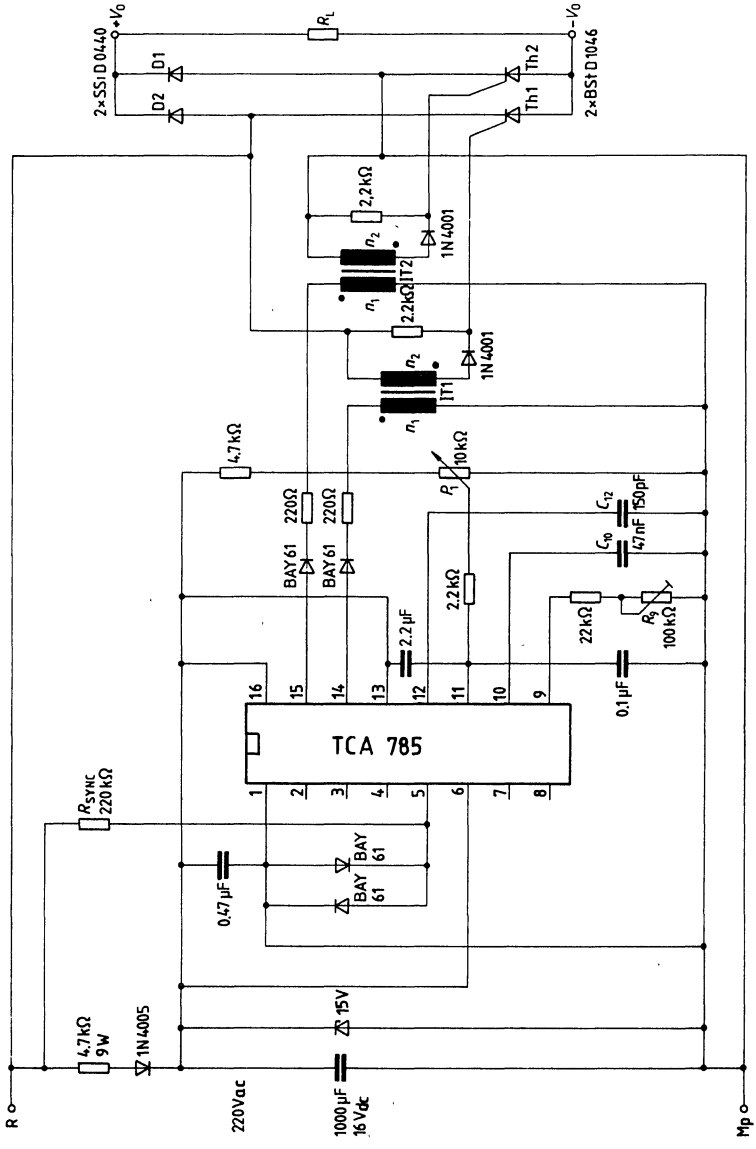


Shown is the possibility to trigger two antiparalleled thyristors with one IC TCA 785. The trigger pulses can be shifted continuously within a phase angle between 0° and 180° by means of a potentiometer. During the negative line half wave the trigger pulse of pin 14 is fed to the relevant thyristor via a trigger pulse transformer. During the positive line half wave, the gate of the second thyristor is triggered by a trigger pulse transformer at pin 15.

Half-controlled single-phase bridge circuit with trigger pulse transformer and direct control for low-power thyristors



Half-controlled single-phase bridge circuit with two trigger pulse transformers for low-power thyristors



SIEMENS

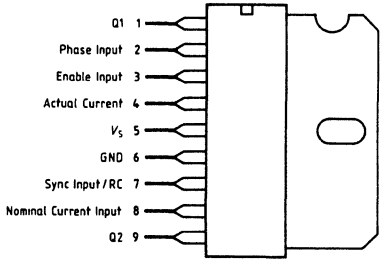
Preliminary

TCA 1561 B, TCA 1560 B
Bipolar IC Stepper Motor Drivers

- 2.5A Peak Current
- High-Speed Integrated Clamp Diodes
- Simple Drive
- Thermal Overload Protection with Hysteresis

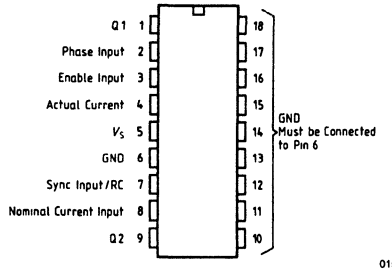
Pin Configurations

TCA 1561 B
(Top View)



0158-1

TCA 1560 B
(Top View)



0158-19

Pin Definitions

TCA 1561 B

Pin	Symbol	Function
1	Q1	Output Q1
2		Phase Input
3		Enable Input
4		Actual Current
5	V_S	Supply Voltage
6	O_S	GND
7	RC	Sync Input/RC
8		Nominal Current Input
9	Q2	Output Q2

The cooling fin is connected internally to pin 6 (ground).

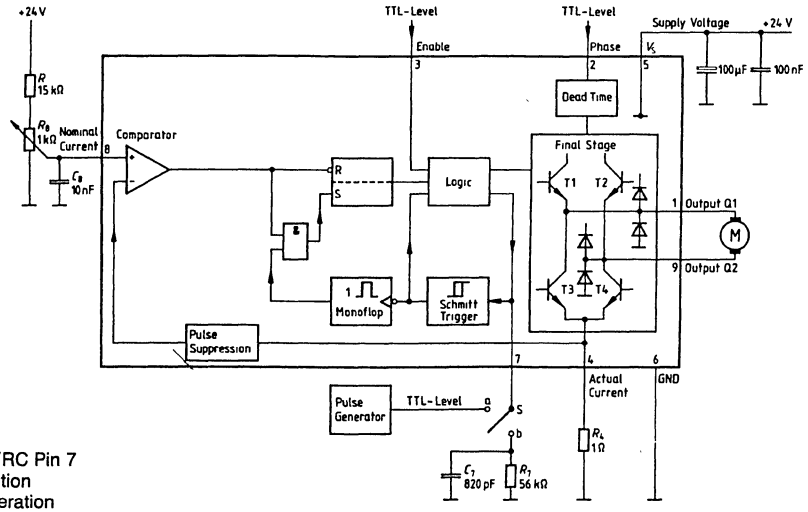
TCA 1560 B

Pin	Symbol	Function
1	Q1	Output Q1
2		Phase Input
3		Enable Input
4		Actual Current
5	V_S	Supply Voltage
6	O_S	GND
7	RC	Sync Input/RC
8		Nominal Current Input
9	Q2	Output Q2
10–18		Ground (Must be Connected to Pin 6)

The TCA 1561 B is a bipolar monolithic IC designed to control the motor current in one phase of a bipolar stepper motor. It can also be used to drive direct-current motors as well as all inductive loads operated by constant current.

The IC has TTL-compatible logic inputs and contains a full-bridge driver with integrated, high-speed clamp diodes and chopper-operated dynamic motor current limiting. The nominal current is infinitely variable with a control voltage. Using minimum external components and a single supply voltage, two TCA 1561 B ICs form a complete and directly MC-drivable system for two-phase bipolar stepper motors with output currents up to 2.5A per phase. The functionally identical TCA 1560 B in the P-DIP-18-L9 package is designed for output currents up to 1.25A.

Block Diagram



Sync Input/RC Pin 7
Switch Position
a. Sync Operation
b. Free-Running Operation

0158-2

4

Circuit Description

Outputs

Outputs Q1, Q2 (Pins 1, 9) are fed by push-pull output stages. The two integrated clamp diodes, referred to ground or supply voltage respectively, protect the IC against flyback voltages from an inductive load.

Enable

Outputs Q1 and Q2 are turned off when voltage $V_{I3} \leq 0.8V$ is applied to pin 3. The supply current then decreases maximally to 1 mA. The same occurs if pin 3 is open. The sink transistors are turned on when $V_{I3} \geq 2V$.

Phase

The voltage at pin 2 determines the phase position of the output current. Output Q1 acts as sink for $V_{I2} \leq 0.8V$ and as source for $V_{I2} \geq 2V$.

Similarly output Q2 acts as

Sink when $V_{I2} \geq 2V$ and
Source when $V_{I2} \leq 0.8V$

The sink transistors are current-chopped. An internal circuit avoids undesired cross-over currents at phase change.

Nominal Current Input

The peak current in the motor winding is determined by the voltage at pin 8. A comparator compares this with the voltage drop at the actual current sensor at pin 4. If the nominal current is exceeded, the output sink transistors are turned off by a logic circuit.

Sync Input/RC

Outputs are turned on by a signal at pin 7. Two operation modes are possible: Synchronizing by a fed-in TTL signal or free-running with the external RC combination.

Free-Running Operation

When the supply voltage is applied, capacitor C_7 at pin 7 charges to a limiting voltage, typically 2.4V. With increasing current in the motor winding, the voltage rises at the actual current sensor R_4 (pin 4). After exceeding the predetermined value at the nominal current input (pin 8) the comparator, in conjunction with pulse suppression, resets an RS flip-flop. The logic turns off sink transistors T3 and T4. C_7 ceases charging and the parallel resistance R_7 then discharges C_7. The sink transistors remain turned off until the lower threshold voltage of the Schmitt trigger is reached. This off period is thus controlled by the time constant $t_s = R_7 \times C_7$. After the lower trigger threshold has been passed, the

monoflop is triggered by the falling edge of the Schmitt trigger output and, provided the voltage at the actual current sensor (pin 4) is lower than the nominal value at pin 8, the RS flipflop is reset. The logic circuit then turns on the sink transistors T3 or T4 and recharges capacitor C_7. If the voltage at pin 4 rises above the comparator value at pin 8, the sink transistors T3 and T4 are turned off again. Turn-on cannot be repeated until capacitor C_7 has discharged to the lower trigger threshold, the discharge time being a function of R_7 and C_7.

Synchronous Operation

If a TTL level sync signal is fed to pin 7, the negative edge sets the RS flipflop, via the Schmitt trigger/monoflop combination, provided that the voltage at pin 4 is below the nominal value at pin 8. As in the free-running operation mode, the relevant output transistors become conducting. Similarly they are cut off by resetting the RS flipflop once the voltage at pin 4 is higher than the nominal value at pin 8.

Pulse Suppression

In all cases the puse suppression circuit eliminates positive pulses, typically of 0.5 μs duration, at pin 4. These can result from cross-over currents in chopper operation through the integrated clamp diodes. As a result, the voltage at pin 4 rises well above the nominal value, and without pulse suppression this would lead to dynamic current limiting. The duration of these basically unavoidable cross-over currents is of the same order of magnitude as the reverse-recovery time of the clamp diodes.

Temperature Safeguard

If the temperature of the IC rises to approximately 150°C, the final stages are turned off. At approximately 130°C they are turned on again.

Logic Table

Enable	L	L	H	H	
Phase	L	H	L	H	
Output Q1	/	/	L	H	
Output Q2	/	/	H	L	
Transistor T1	X	X	X	•	
Transistor T2	X	X	•	X	at:
Transistor T3	X	X	••	X	$V_4 > 10$ mV
Transistor T4	X	X	X	••	$R_4 > 0\Omega$

L = Low voltage level, input open
H = High voltage level
X = Transistor turned off
• = Transistor conducting
•• = Transistor conducting with current limiting turned on
/ = Output high-impedance

Absolute Maximum Ratings*

T_C = −25°C to +85°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Supply Voltage, Pin 5 (V_S) ..... −0.3V to +45V
Supply Current, Pin 5 (I_S) ..... 0A to +2.5A
Peak Current in Output
Transistors, Pins 1, 9 (I_Q) ..... −2.5A to +2.5A

Diode Currents
Diode against +V_S (I_{FH}) 2.5A
Diode against Ground (I_{FL}) 2.5A

Input Voltage, Pins 2, 3, 7, 8 (V_I) ..... −0.3V to +6V
Output Current, Pin 4 (I_4) ..... −2.5A
Voltage, Pin 4 (V_4) ..... −0.3V to +5V
Ground Current, Pin 6 (I_6) 2.5A

Junction Temperature (T_j) ..... 150°C*
Storage Temperature (T_{stg}) ..... −40°C to +125°C
Thermal Resistance
System-Ambient ($R_{th\ SA}$) ..... 70 K/W
System-Package ($R_{th\ SC}$) ..... 8 K/W

Operation Range

Supply Voltage, Pin 5 (V_S) ..... 8V to 40V
Package Temperature (T_C) ..... −25°C to +85°C
Input Voltage, Pins 2, 3, 7 (V_I) 5V
Output Current (I_Q) ..... −2A to +2A

*ICs provide optimal reliability and service life if the junction temperature does not exceed 125°C in operation. Operation up to the maximum permissible limit of the junction temperature at 150°C is possible in principle. It should be noted, however, that exposure to absolute maximum rating conditions for extended periods may effect device reliability.
Within the operating range the functions given in the circuit description will be fulfilled. However, deviations from the characteristics are possible.

Characteristics $T_C = 25°C; V_S = 24V$

The listed characteristics are ensured over the operating rnage of the integrated circuit at the given supply voltage and ambient temperature. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics will apply at $T_C = 25°C$ and $V_S = 24V$.

Parameter	Symbol	Conditions	Limits			Units
			Min	Typ	Max	
Supply Current, Pin 5	I_S	$V_{I3} = V_{IH}$		18	30	mA
Supply Current, Pin 5	I_S	$V_{I3} = V_{IL}$		0.5	1	mA
Output, Pins 1, 9						
Output Voltage: Source	V_{QH}	$\|I_Q\| = 1A$		1.7	1.9	V
Output Voltage: Source	V_{QH}	$\|I_Q\| = 1.5A$		1.9	2.1	V
Output Voltage: Sink	V_{QL}	$\|I_Q\| = 1A$		1.2	1.4	V
Output Voltage: Sink	V_{QL}	$\|I_Q\| = 1.5A$		1.5	1.7	V
Reverse Current	$\|I_{QS}\|$				300	µA
Phase Dead Time	t_T	Figure 1	0.1	0.3	1.0	µs
Forward Voltage of Diodes against $+V_S$	V_{FH}	$I_{FH} = 1A$		1.0	1.2	V
	V_{FH}	$I_{FH} = 1.5A$		1.1	1.3	V
Forward Voltage of Diodes against Ground	V_{FL}	$I_{FL} = 1A$		1.1	1.3	V
	V_{FL}	$I_{FL} = 1.5A$		1.3	1.5	V
Inputs: Enable, Pin 3 and Phase, Pin 2						
H Input Voltage	V_{IH}		2			V
L Input Voltage	V_{IL}				0.8	V
H Input Current	I_{IH}	$V_{IH} = 5V$		50	100	µA
L Input Current	$-I_{IL}$	$V_{IL} = 0V$			100	µA
Rise and Fall Time	t_r, t_f				2	µs
Nominal Current, Pin 8						
Control Range	V_{I8}		0		2	V
Input Current	$-I_{I8}$	$V_{I8} = 0V$			5	µA
Input Offset Voltage	$V_{I(8-4)}$	Figure 5		0		mV
Actual Current, Pin 4						
Control Range	V_{I4}	Figure 5	0		2	V
Turn-Off Delay	t_d	Figure 3		2	3	µs
Sync Input/RC, Pin 7						
Sync Frequency	f	Duty Cycle: 0.5	1		100	kHz
Duty Cycle	υ	f = 40 kHz	0.1		0.9	
Rise and Fall Time	t_r, t_f				2	µs
Output Current, Pin 7	$-I_{Q7}$		1.2	1.6	2.0	mA
Trigger Threshold, Pin 7	V_{L7}	Figure 2		0.6	0.8	V
Charging Limit C_7	V_{G7}		2.2	2.4		V
Off Period	t_S	Figure 4		64		µs
Dynamic Input Resistance, Pin 7	R_{I7}	$V_7 = 1.5V$		1		kΩ

Absolute Maximum Ratings*

T_C = −25°C to +85°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Supply Voltage, Pin 5 (V_S) ..... −0.3V to +45V

Supply Current, Pin 5 (I_S) ..... 0A to +1.25A

Peak Current in Output Transistors, Pins 1, 9 (I_Q) .... −1.25A to +1.25A

Diode Currents, Pins 1, 9

Diode against +V_S (I_{FH}) 1.25A

Diode against Ground (I_{FL}) 1.25A

Input Voltage, Pins 2, 3, 7, 8 (V_I) ..... −0.3V to +6V

Output Current, Pin 4 (I_4) ..... −1.25A

Voltage, Pin 4 (V_4) ..... −0.3V to +5V

Ground Current, Pin 6 (I_6) 1.25A

Junction Temperature (T_j) ..... 150°C*

Storage Temperature (T_{stg}) ..... −40°C to +125°C

Thermal Resistance

System-Ambient ($R_{th\ SA}$) ..... 70 K/W

System-Package Measured at Pin 14 ($R_{th\ SC}$) ..... 15 K/W

Operating Range

Supply Voltage, Pin 5 (V_S) ..... 8V to 40V

Package Temperature Measured at Pin 14 (T_C) ..... −25°C to +85°C

Input Voltage, Pins 2, 3, 7 (V_I) 5V

Output Current, Pins 1, 9 (I_Q) ..... −1A to +1A

*ICs provide optimal reliability and service life if the junction temperature does not exceed 125°C in operation. Operation up to the maximum permissible limit of the junction temperature at 150°C is possible in principle. It should be noted, however, that exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Within the operation range the functions given in the circuit description will be fulfilled. However, deviations from the characteristics are possible.

Characteristics T_C = 25°C; V_S = 24V

The listed characteristics are ensured over the operating range of the integrated circuit at the given supply voltage and ambient temperature. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics will apply at T_C = 25°C and V_S = 24V.

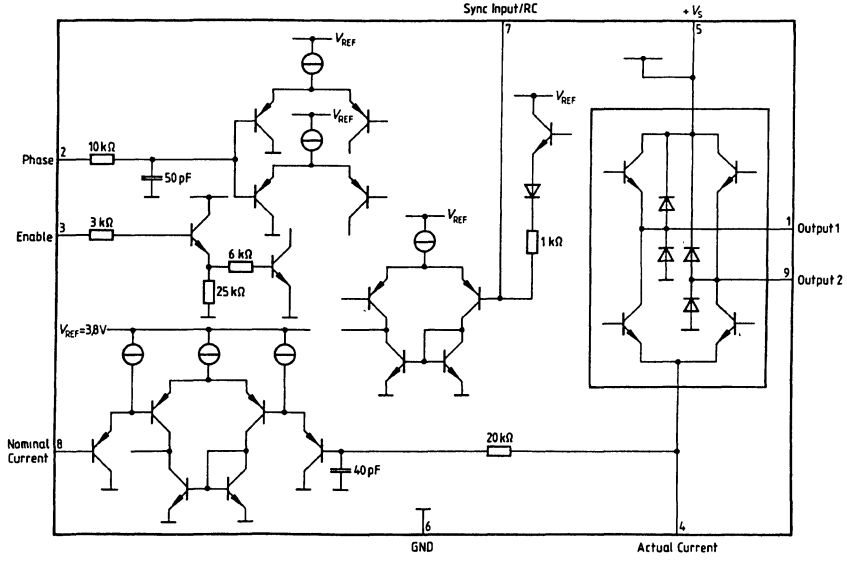
Parameter	Symbol	Conditions	Limits			Units
			Min	Typ	Max	
Supply Current, Pin 5	I_S	$V_{I3} = V_{IH}$		18	30	mA
Supply Current, Pin 5	I_S	$V_{I3} = V_{IL}$		0.5	1	mA
Output, Pins 1, 9						
Output Voltage: Source	V_{QH}	$\|I_Q\|$ = 0.5A		1.6	1.8	V
Output Voltage: Source	V_{QH}	$\|I_Q\|$ = 0.75A		1.65	1.90	V
Output Voltage: Sink	V_{QL}	$\|I_Q\|$ = 0.5A		1.0	1.2	V
Output Voltage: Sink	V_{QL}	$\|I_Q\|$ = 0.75A		1.1	1.4	V
Reverse Current	$\|I_{QS}\|$				300	µA
Phase Dead Time	t_T	Figure 1	0.1	0.3	1.0	µs
Forward Voltage of Diodes against +V_S	V_{FH}	I_{FH} = 0.5A		0.9	1.1	V
	V_{FH}	I_{FH} = 0.75A		0.95	1.15	V
Forward Voltage of Diodes against Ground	V_{FL}	I_{FL} = 0.5A		0.95	1.15	V
	V_{FL}	I_{FL} = 0.75A		1.0	1.2	V
Inputs: Enable, Pin 3 and Phase, Pin 2						
H Input Voltage	V_{IH}		2			V
L Input Voltage	V_{IL}				0.8	V
H Input Current	I_{IH}	V_{IH} = 5V		50	100	µA
L Input Current	$-I_{IL}$	V_{IL} = 0V			100	µA
Rise and Fall Time	t_r, t_f				2	µs

Characteristics T_C = 25°C; V_S = 24V (Continued)

The listed characteristics are ensured over the operating range of the integrated circuit at the given supply voltage and ambient temperature. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics will apply at T_C = 25°C and V_S = 24V.

Parameter	Symbol	Conditions	Limits			Units
			Min	Typ	Max	
Nominal Current, Pin 8						
Control Range	V_{I8}		0		2	V
Input Current	$-I_{I8}$	V_{I8} = 0V			5	µA
Input Offset Voltage	$V_{I(8-4)}$	Figure 5		0		mV
Actual Current, Pin 4						
Regulating Range	V_{I4}	Figure 5	0		2	V
Turn-Off Delay	t_d	Figure 3		2	3	µs
Sync Input/RC, Pin 7						
Sync Frequency	f	Duty Cycle: 0.5	1		100	kHz
Duty Cycle	υ	f = 40 kHz	0.1		0.9	
Rise and Fall Time	t_r, t_f				2	µs
Output Current, Pin 7	$-I_{Q7}$		1.2	1.6	2.0	mA
Trigger Threshold, Pin 7	V_{L7}	Figure 2		0.6	0.8	V
Charging Limit C_7	V_{G7}		2.2	2.4		V
Off Period	t_S	Figure 4		64		µs
Dynamic Input Resistance, Pin 7	R_{I7}	V_7 = 1.5V		1		kΩ

Internal Wiring of Pins



Phase Dead Time

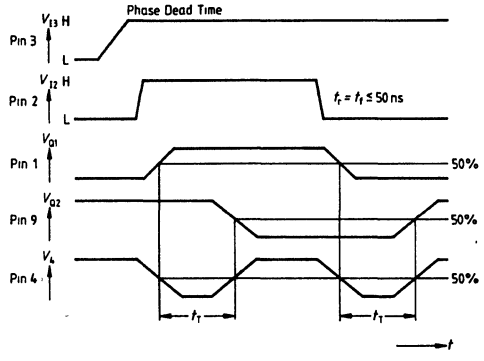


Figure 1

Trigger Threshold

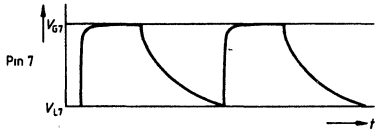


Figure 2

Turn-Off Delay

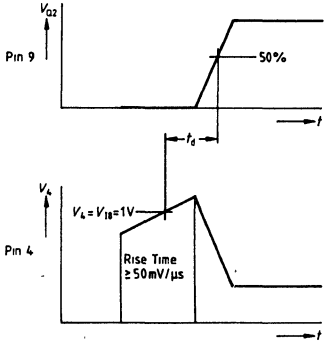


Figure 3

Off Period $T_S = f(C_7)$

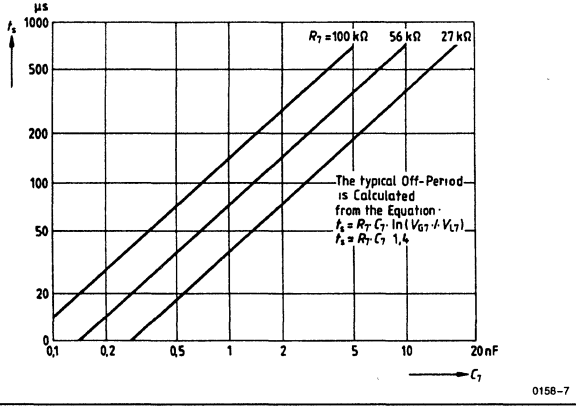


Figure 4

Control Range, Input Offset Voltage

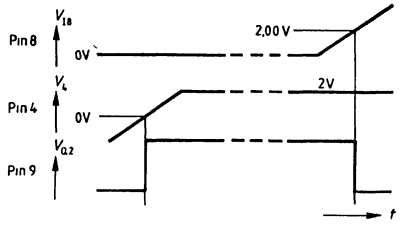
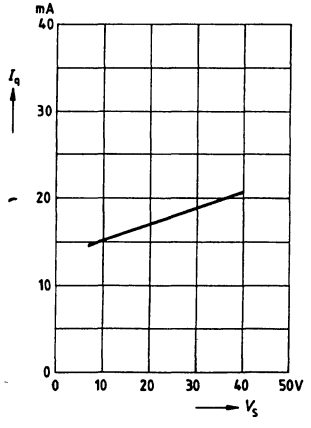
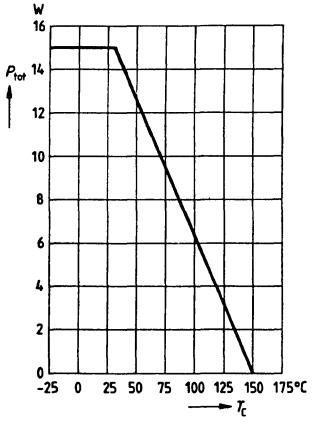


Figure 5

Quiescent Current, I_q versus Supply Voltage V_S

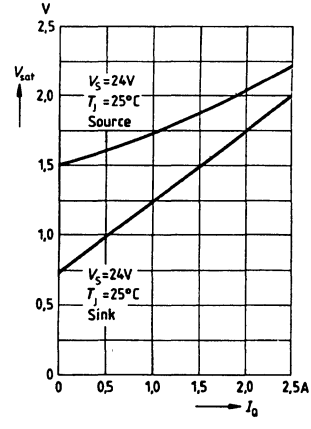


Permissible Power Dissipation P_{tot} versus Package Temperature T_C

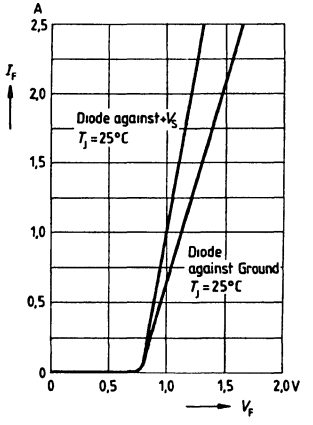


0158-1

Output Saturation Voltages V_{sat} versus Output Current I_Q

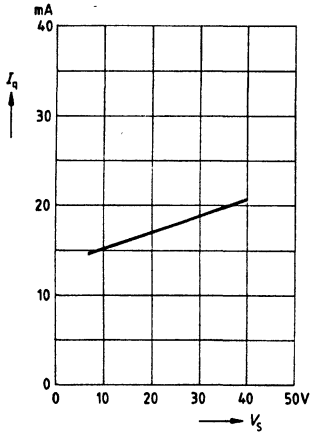


Forward Current I_F of Clamp Diodes versus Forward Voltages V_F

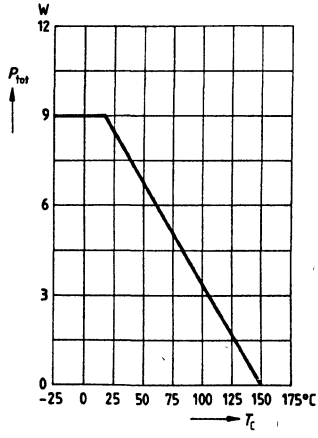


0158-10

Quiescent Current I_q versus Supply Voltage V_S

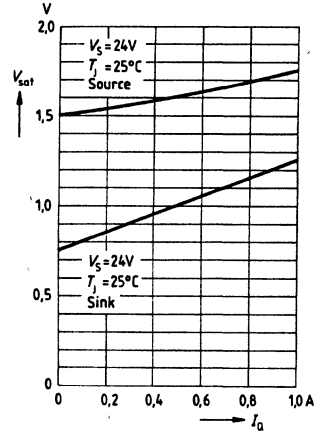


Permissible Power Dissipation P_{tot} versus Package Temperature T_C

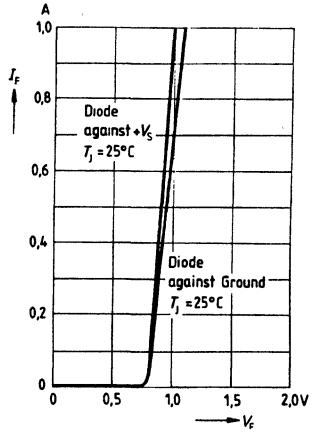


0158-11

Output Saturation Voltages V_{sat} versus Output Current I_Q

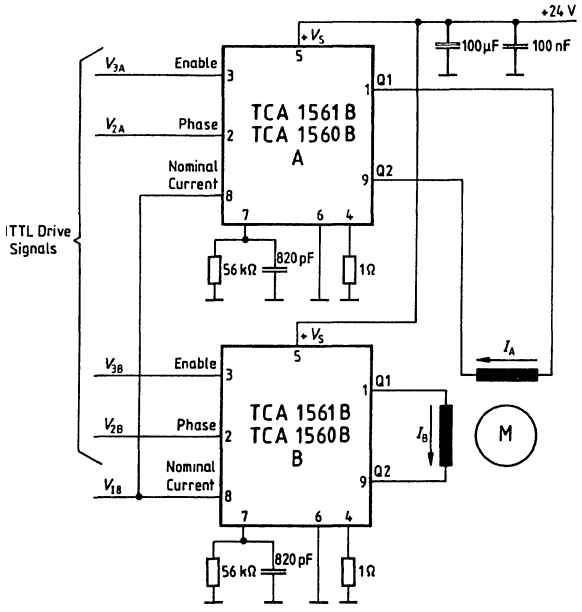


Forward Current I_F of Clamp Diodes versus Forward Voltages V_F



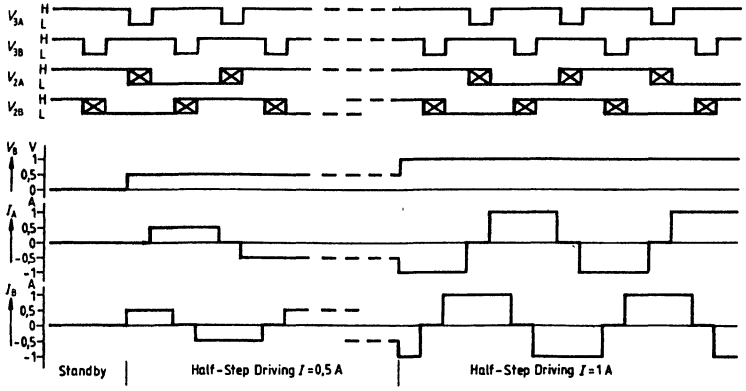
0158-12

Application Circuit



0158-13

Pulse Diagram for Application Circuit



0158-14

Calculation of Power Dissipation

The total power dissipation P_{tot} comprises

Saturation Losses P_{sat}	(Transistor saturation voltage and diode forward voltages)
Quiescent Current Losses P_Q	(Quiescent current multipled by supply voltage)
Switching Losses P_S	(Turn-on/Turn-off operation)

The following equations give the power dissipation for chopper operation without phase reversal. This can be regarded as "worst case", as, in addition to the switching losses, full-load current flows for the entire time.

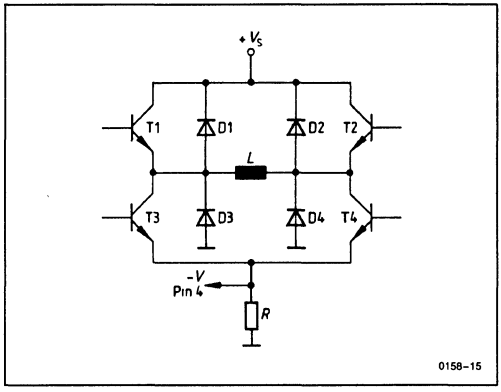
$$P_{tot} = P_{sat} + P_q + P_s$$

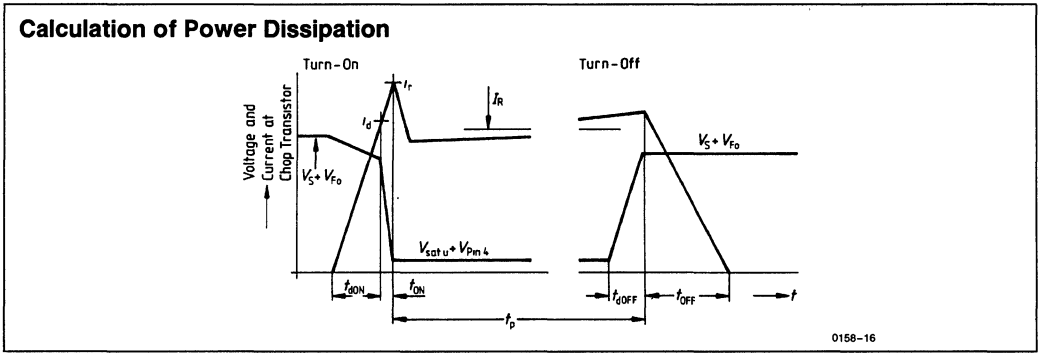
with $P_{sat} \cong I_R \{V_{satu} \bullet \upsilon + V_{Fo}(1 - \upsilon) + V_{sato}\}$

$$P_q = I_q \bullet V_S$$

$$P_S \cong \frac{V_S}{T}\left\{\frac{i_d \bullet t_{dON}}{2} + \frac{(i_d + i_r)}{4} + \frac{I_R}{2}\left(t_{dOFF} + tOFF\right)\right\}$$

I_R = Rated Current (Mean Value)
I_q = Quiescent Current
i_d = Reverse Current During Turn-On Delay Time
i_r = Peak Reverse Current
t_p = Conducting Time of Chop Transistor
t_{ON} = Turn-On Time
t_{OFF} = Turn-Off Time
t_{dON} = Turn-On Delay Time
t_{dOFF} = Turn-Off Delay Time
T = Cycle Duration
υ = Duty Cycle t_p/T
V_{satu} = Saturation Voltage of Sink Transistor (T3, 4)
V_{sato} = Saturation Voltage of Source Transistor (T1, 2)
V_{Fo} = Forward Voltage of Clamp Diode (D1, 2)
V_S = Supply Voltage

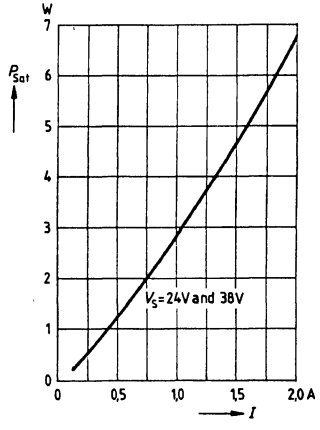




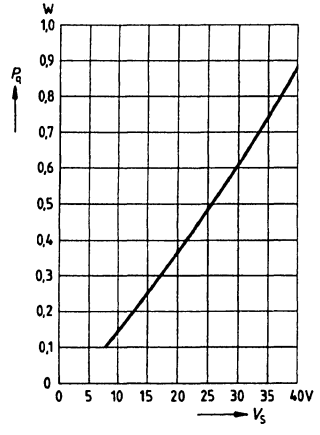
Characteristics for determining the typical power dissipation during chopper operation without phase reversal.

Parameters: L_{load} = 10 mH, C_7 = 820 pF; R_7 = 33 kΩ; T_C = 25°C

Saturation Loss P_{sat} versus Phase Current I



Quiescent Current Loss P_q versus Supply Voltage V_S

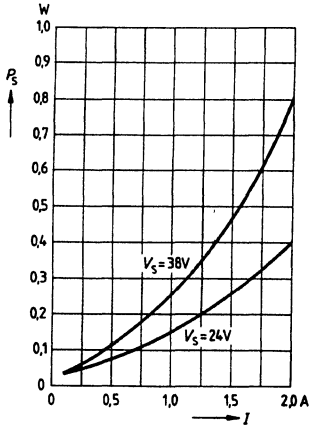


0158-17

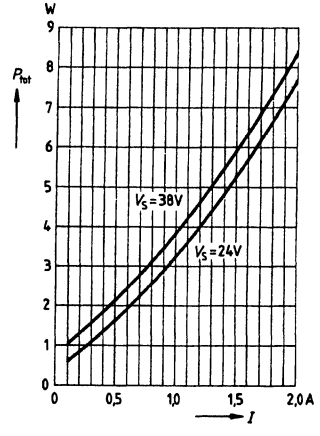
Characteristics for determining the typical power dissipation during chopper operation without phase reversal.

Parameters: L_{load} = 10 mH, C_7 = 820 pF; R_7 = 33 kΩ; T_C = 25°C

Switching Loss P_S versus Phase Current I



Total Power Dissipation P_{tot} versus Phase Current I



0158-18

Ordering Information

Type	Ordering Code	Package
TCA 1561 B	Q67000-A8209	P-SIP-9
TCA 1560 B	Q67000-A8208	P-DIP-18-L9

SIEMENS

TLE 4201 A, TLE 4201 S
DC Motor Driver

The TLE 4201 IC is a dual comparator that is particularly suitable as a driver for reversible dc motors and may also be used as a versatile power driver.

The push-pull power-output stages work in a switch mode and can be combined into a full bridge configuration.

The driving of the comparators may be analog in the form of a window discriminator, or it can be accomplished very simply with digital logic.

Typical applications are follow-up controls, servo drives, servo motors, drive mechanisms, etc.

Features

- Max. output current 2.5 A
- Open-loop gain 80 dB typ.
- PNP input stages
- Large common-mode input-voltage range
- Wide control range
- Low saturation voltages
- SOA protective circuit
- Temperature protection

The TLE 4201 IC comes in two different packages: with the SIP 9 package it is possible to remove the heat by way of a cooling fin to a suitable heatsink, whereas with the DIP 18-L9 package the pins 10 through 18 are thermally linked to the chip and provide for heat dissipation by way of the circuit board.

Block diagram

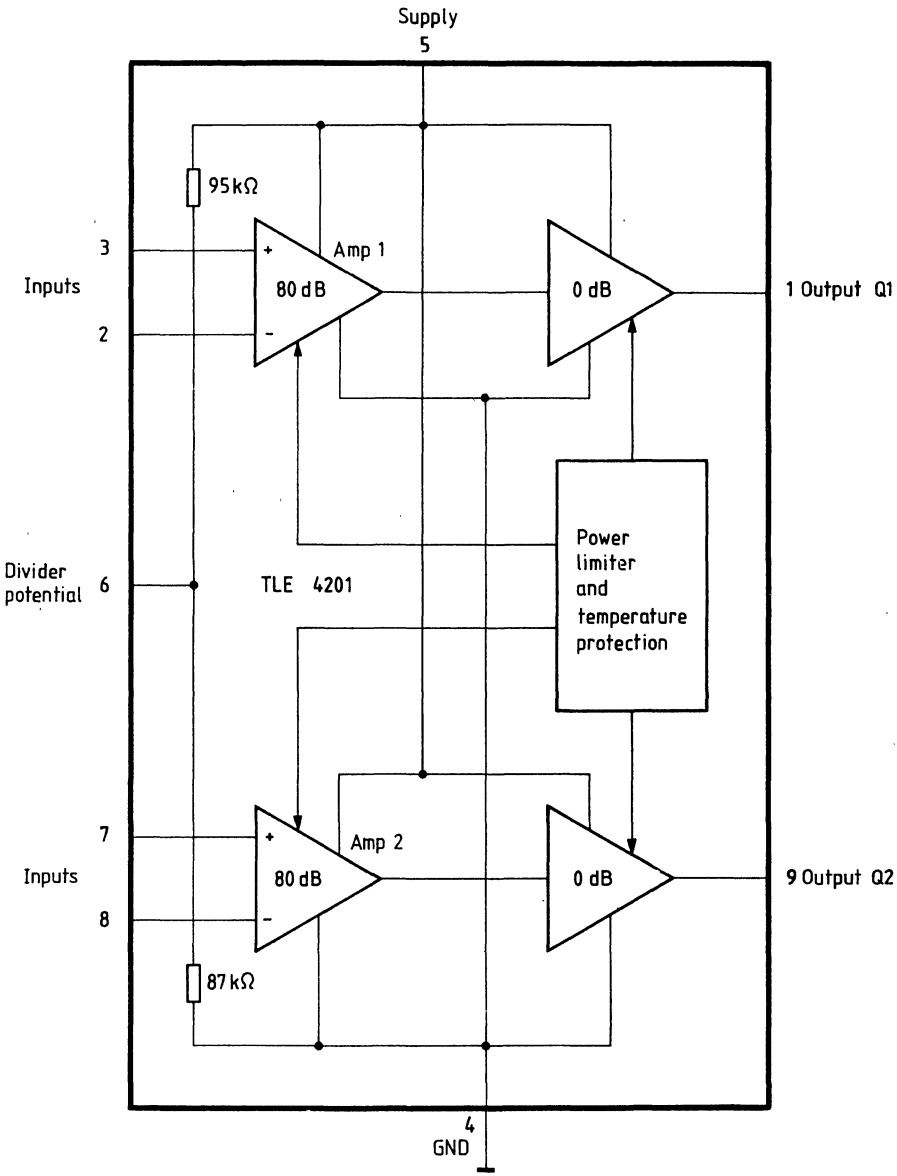


Figure 1

Pin configuration

TLE 4201 A Pin No.	TLE 4201 S Pin No.	Function
1	1	Output of 1st amplifier
2	2	Inverting input of 1st amplifier
3	3	Non-inverting input of 1st amplifier
4	4	Ground
5	5	Supply voltage
6	6	Divider potential
7	7	Non-inverting input of 2nd amplifier
8	8	Inverting input of 2nd amplifier
9	9	Output of 2nd amplifier
10 to 18	—	Ground; to be connected to pin 4

Circuit description

The IC contains two amplifiers featuring a typical open-loop voltage gain of 80 dB at 500 Hz. The input stages are PNP differential amplifiers. This results in a common-mode input voltage range from 0 V to almost the value of V_S, and in a maximum input differential voltage of I V_S I. To obtain low saturation voltages, the sink transistor (lower transistor) of the push-pull AB output stage is internally bootstrapped. An SON protective circuit protects the IC against motor short circuits and ground short circuits. An internal overtemperature protection protects the IC against overheating in case of failure due to insufficient cooling or overload.

For logic control, a divider potential of approx. $V_S/2$ is available at pin 6 (see application circuit 2). This makes the IC particularly suitable for digital circuits, as power driver.

Application

Figure 2 shows a window discriminator operation with the control voltage V_I.
The window within which the motor is to stop is set by R_2.

Figure 3 shows driving by logic inputs A and B. The motor is controlled according to the following truth table.

A	B	Output
L	L	Motor stopped (slowed down)
L	H	Motor turns right
H	L	Motor turns left
H	H	Motor stopped (slowed down)

Application circuits

Operated as window discriminator

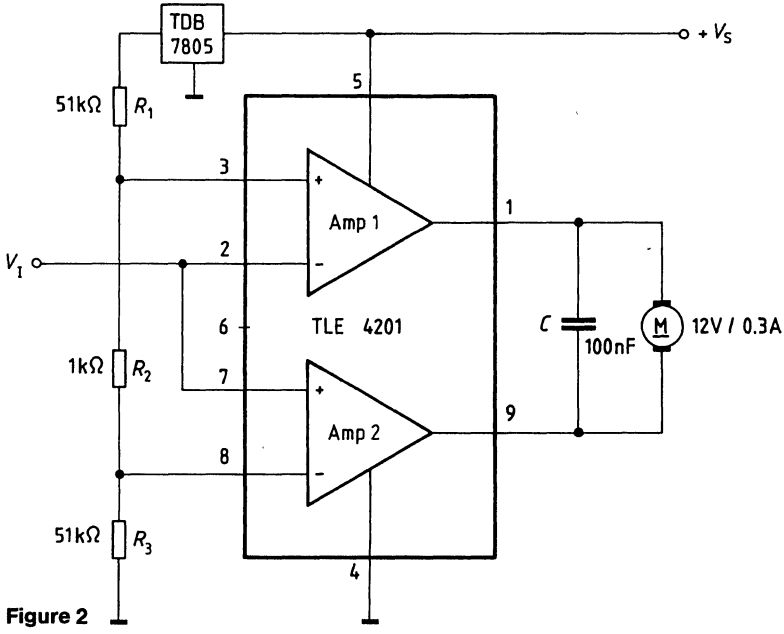


Figure 2

Digital control

for input signals applies: H ≥ 0.6 V_S
L ≤ 0.3 V_S

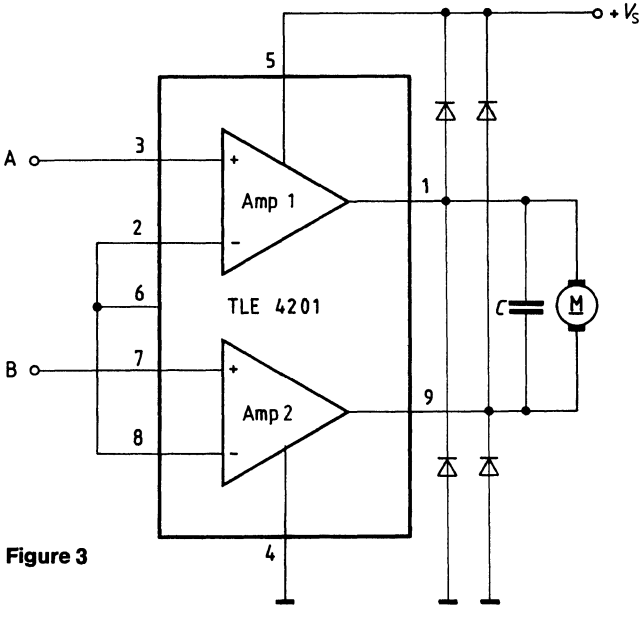


Figure 3

Maximum ratings

$T_{case} = -35$ °C to 85 °C

		Lower limit B	Upper limit A	
Supply voltage	V_S		25	V
Supply voltage ($t \leq 50$ ms)	V_S		36	V
Output current	I_Q		2.5	A
Voltage of pins 2, 3, 6, 7, 8	V	−0.3	V_S	V
Voltage of pins 1, 9	V	−0.3		V
Junction temperature	T_j		150	°C
Storage temperature	T_{stg}	−55	125	°C
Thermal resistance				
TLE 4201 S: system-air	$R_{th\,JA}$		65	K/W
system-case	$R_{th\,JC}$		8	K/W
TLE 4201 A: system-air[1]	$R_{th\,JA}$		60	K/W
system-PC board[1]	$R_{th\,JA1}$		44[1]	K/W

Operating range

Supply voltage	V_S	3.5	17	V
Case temperature	T_{case}	−35	85	°C
Voltage gain (at negative feedback with external components)	G_V	25		dB

Characteristics

$V_S = 13$ V, $T_{case} = 25$ °C

		Test conditions		Lower limit B	typ	Upper limit A	
Supply current	I_S	Figure 4: S = 1			20	30	mA
Open-loop voltage gain	G_{V0}	$f = 500$ Hz			80		dB
Input resistance	R_I	$f = 1$ kHz		1	5		MΩ
Saturation voltages,		Figure 5:	S1				
source operation	$V_{Q\,10}$	$I_Q = 0.3$ A	1		1.0	1.1	V
		$I_Q = 1.0$ A	1		1.2	1.6	V
sink operation	$V_{Q\,20}$	$I_Q = -0.3$ A	2		0.35	0.5	V
		$I_Q = -1.0$ A	2		0.7	1.0	V
Rise time of V_Q	t_r	Figure 4 and 6			1.5		µs
Fall time of V_Q	t_f	Figure 4 and 6			1.5		µs
Turn-on delay time	t_{on}	Figure 4 and 6			3.0		µs
Turn-off delay time	t_{off}	Figure 4 and 6			1.5		µs
Input current		Figure 5					
(pins 2, 3, 7, 8)	I_I	$V_{2,3,7,8} = 0$			1.5	3.0	µA
Input offset voltage	V_{IO}	Figure 7		−20		20	mV

1) see figure 8

Test circuits

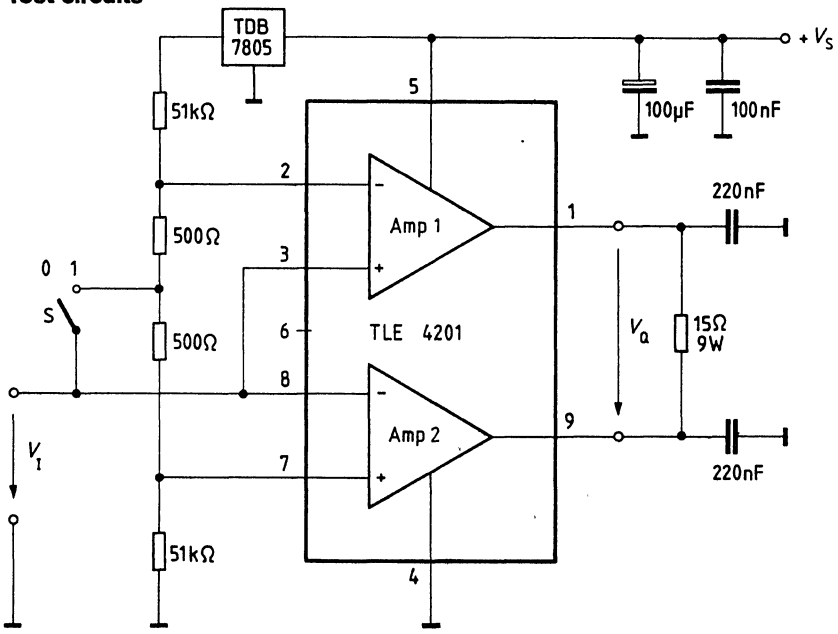


Figure 4

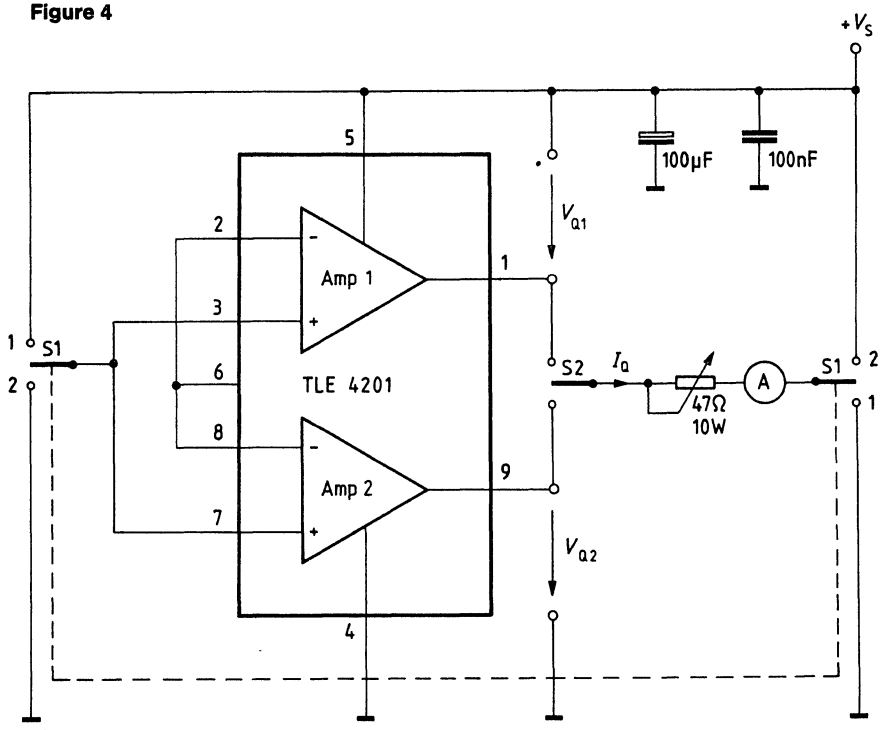


Figure 5

Pulse diagram

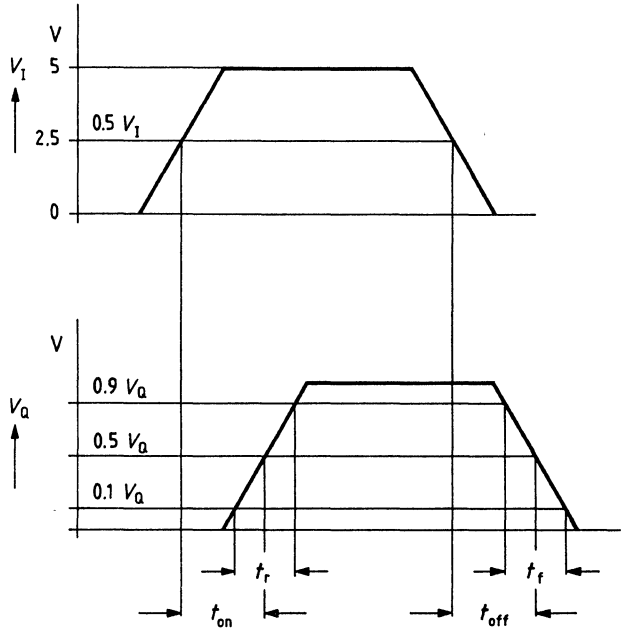


Figure 6

Test and measurement circuit

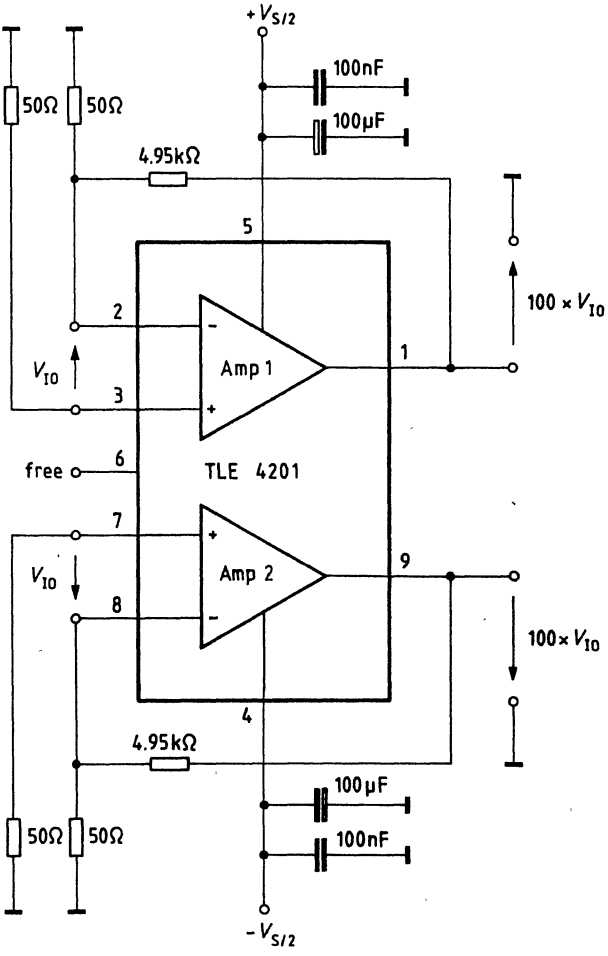


Figure 7

Thermal resistance of TLE 4201 A

Thermal resistance, junction-air, $R_{th\ JA\ 1}$ (standard) versus side length l of a square copper-clad cooling surface (35 µm copper plate)

$R_{th\ JA}$ ($l = 0$) = 60 K/W
$T_{amb} \leq 70$ °C
$P_V = 1$ W
substrate vertical
circuit vertical
static air

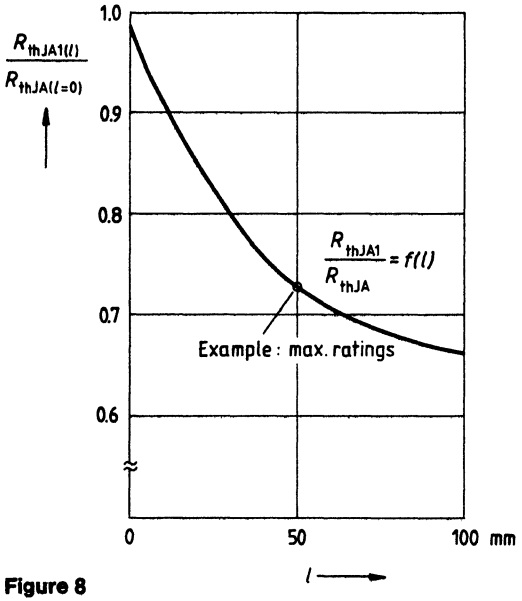


Figure 8

SIEMENS

Preliminary

TLE 4202
Power Bridge

- Max Output Current 2.5A
- Open-Loop Gain 80 dB Typ
- PNP Input Stages
- Large Common-Mode Input-Voltage Range
- Wide Control Range
- Low Saturation Voltages
- SOA Protective Circuit
- Temperature Protection

Pin Definitions

Pin	Symbol	Function
1	I_1	Input 1
2	T	Input 3 Inverted
3	Q_1	Output
4	GND	Ground
5	Q_2	Output
6	V_S	Supply Voltage
7	I_2	Input 2

4

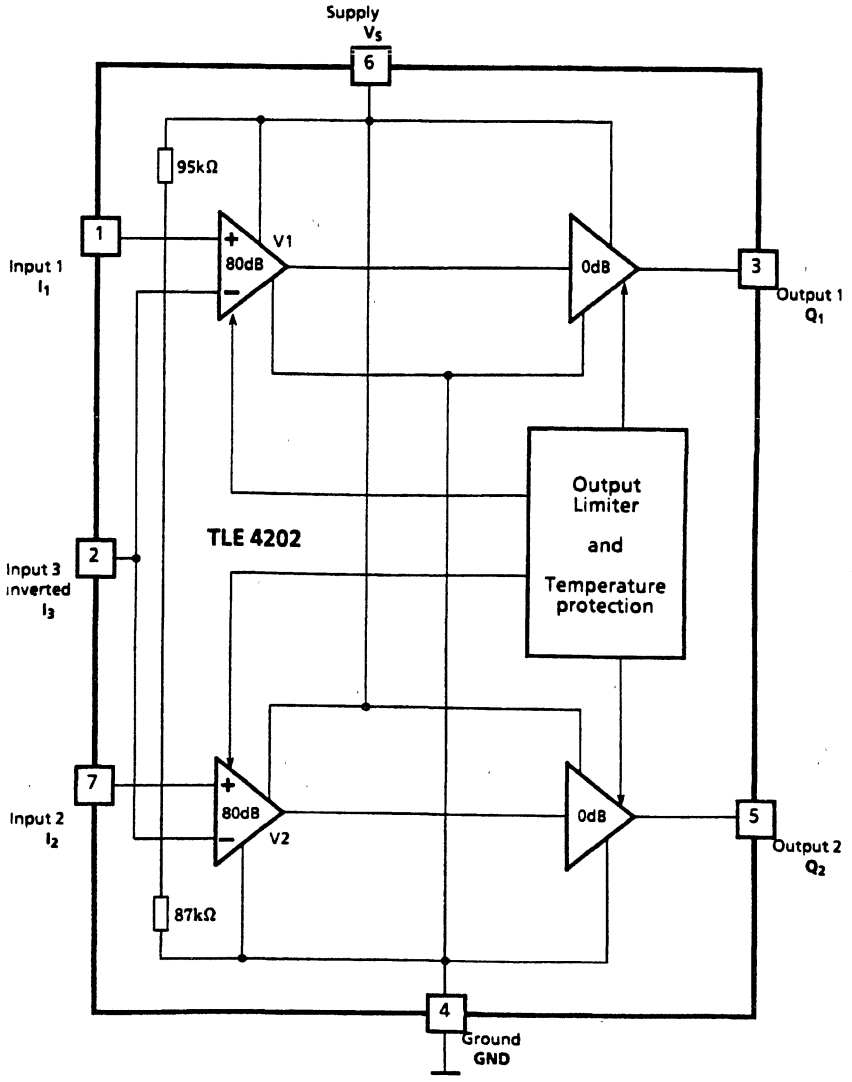
The TLE 4202 IC is a power dual comparator that is particularly suitable as a driver for reversible DC motors and may also be used as a versatile power driver.

The two power comparators may, either in combination in a full bridge, or separately, switch magnets, motors and other loads. The IC is designed for automotive applications. It functions at package temperatures from −40°C to +130°C.

The driving of the comparators may be analog in the form of a window discriminator, or it can be accomplished very simply with digital logic.

Typical applications are follow-up controls, servo drives, servo motors, drive mechanisms, etc.

Block Diagram



Circuit Description

The IC includes two amplifiers with an open loop gain of 80 dB at 500 Hz.

The input stages consist of PNP differential amplifiers. This results in an input common mode range of 0V to almost V_S and a maximum differential input voltage of V_S. In order to achieve lower saturation voltages the sink transistor ("low transistor") of the push-pull-AB-output stage is internally loaded (boot strapped). The IC is protected against short circuits to ground using an SOA protection circuit.

Absolute Maximum Ratings*

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Maximum ratings for case Temperature $-40°C < T_C < 130°C$

Pos	Parameter	Symbol	Conditions	Limits		Units
				Min	Max	
1	Supply Voltage	V_S			25	V
2	Supply Voltage ($t \leq 50$ ms)	V_S			36	V
3	Output Current	I_Q	$T_C \leq 85°C$	−3.0	3.0	A
4	Voltage at the Pins I_1, I_2, T	$V_{1,2,7}$		−0.3	V_S	V
5	Voltage at the Pins Q_1, Q_2	$V_{3,5}$		−0.7	$V_S + 0.7$	V
6	Junction Temperature	T_J			150	°C
7	Storage Temperature	T_S		−55	125	°C

Operating Range

Maximum ratings are absolute limiting values; any of which if exceeded may result in destroying the integrated circuit.

Pos	Parameter	Symbol	Conditions	Limits		Units
				Min	Max	
1	Supply Voltage	V_S		3.5	17	V
2	Case Temperature During Operation	T_C		−40	+85	°C
3	Voltage Gain (with Feedback with External Circuit)	V_U		30		dB
Thermal Resistances						
4	System-Case	$R_{th\,SC}$			5.0	K/W

Outputs Q_1 and Q_2 short circuit protected to GND.

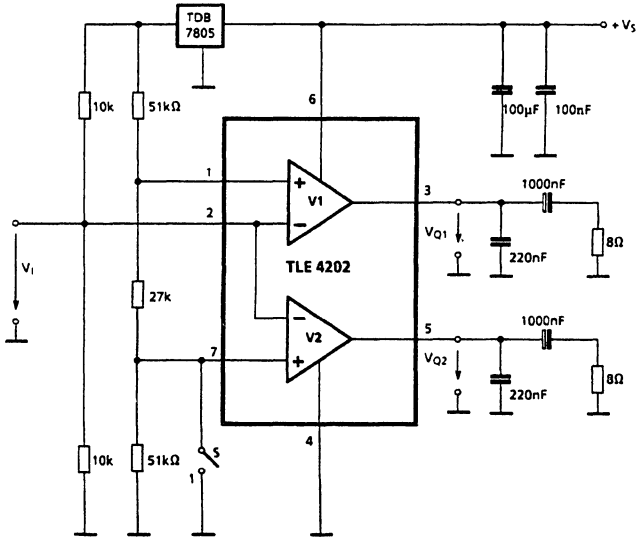
Ratings

Ratings encompass the reproducibility of the values as limited by the stated operating range of the integrated circuits. Mid-range values to be expected from a production run are noted under typical ratings. Unless otherwise indicated, typical ratings apply at T_C = 25°C and a supply voltage V_S of 13V.

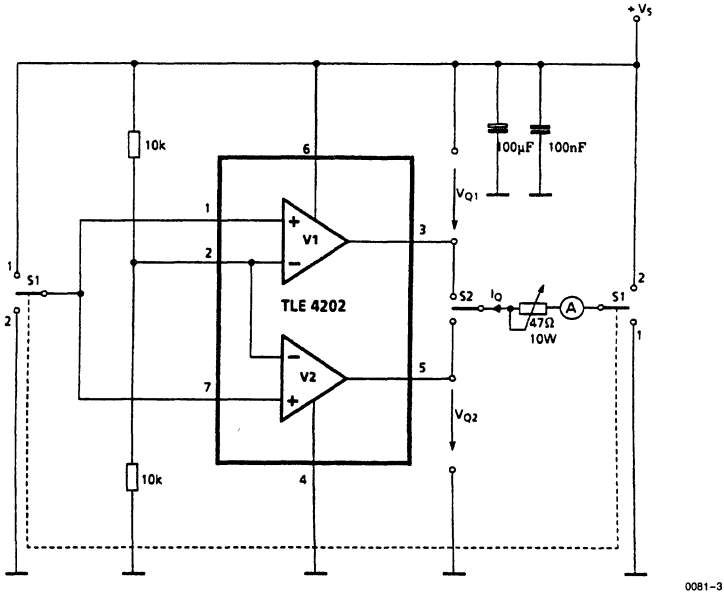
Pos	Parameter	Symbol	Conditions	Measuring Circuit	Limits			Units
					Min	Typ	Max	
General Characteristics								
1	Quiescent Current	I_S	S = 1	1		30	40	mA
2	Open Loop Gain	V_{UO}	f = 500 Hz	1	70	80		dB
Input Characteristics								
3	Input Current (Pins I_1, I_2)	$I_{I1,7}$	$V_{I1,I2}$ = 0	2		1.5	3.0	µA
4	Input Impedance	$R_{I1,7}$	f = 1 kHz	1	1	5		MΩ
5	Input Off-Set Voltage	V_{I0}		3	−20		20	mV
Output Characteristics								
6	Source Drive	V_Q	I_Q = −0.3A S1 = 1 I_Q = −1.0A S1 = 1	2 2		1.0 1.2	1.1 1.6	V V
7	Sink Drive	V_Q	I_Q = +0.3A S1 = 2 I_Q = +1.0A S1 = 2	2 2		0.35 0.7	0.5 1.0	V V
8	Current Limit	I_{Qmax}	Source Drive	2	2.0	2.5		A
9	Short Circuit Current	I_{Sh}	V_S = 7V; V_O = 0V	2	1.8	2.3	3.0	A
Switching Times								
10	Rise-Time from V_Q	t_r	Figure 1	1		1.5		µs
11	Fall-Time from V_Q	t_f	Figure 1	1		1.5		µs
12	Turn-On Delay	t_{on}	Figure 1	1		3.0		µs
13	Turn-Off Delay	t_{off}	Figure 1	1		1.5		µs

Test Circuits

Test Circuit 1

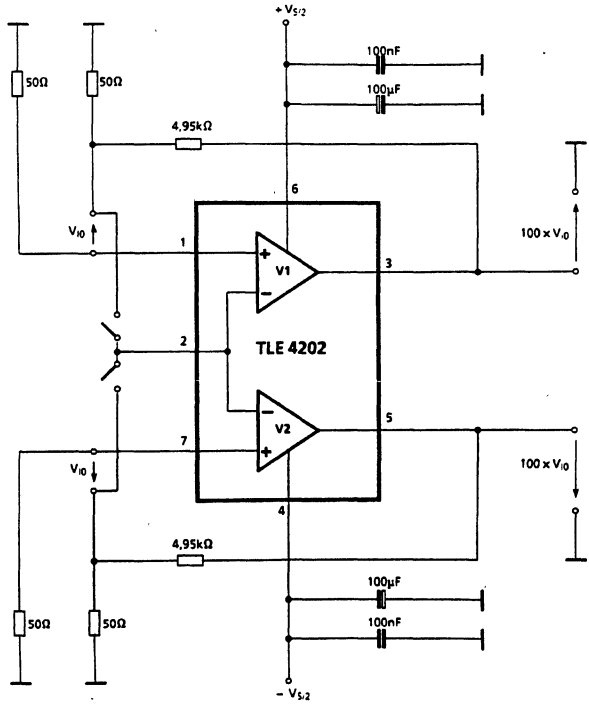


Test Circuit 2

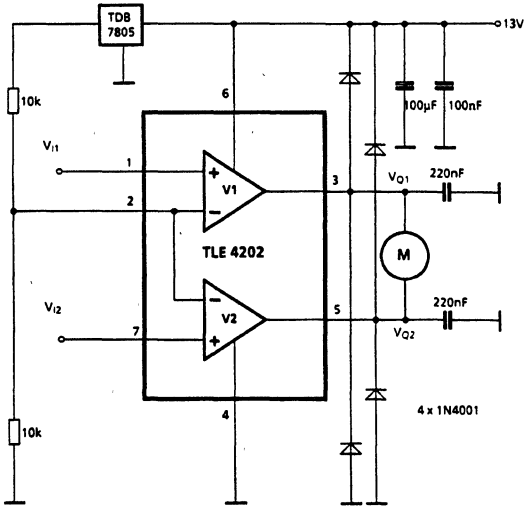


Test Circuits (Continued)

Test Circuit 3



Application Circuit



Diagram

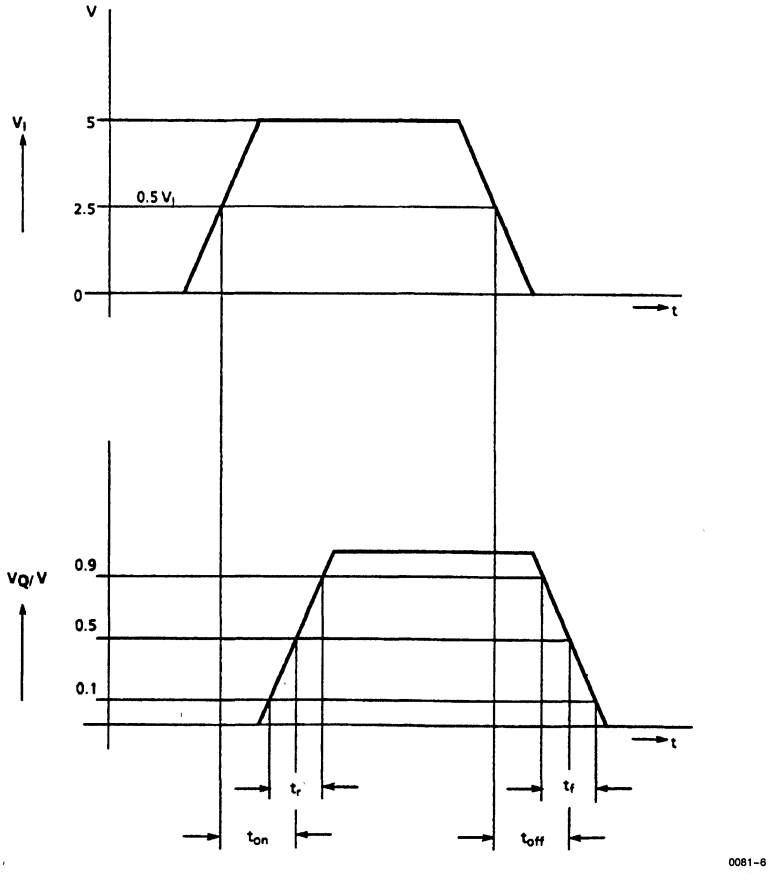


Figure 1

Ordering Information

Type	Ordering Code	Package
TLE 4202	Q 67000-A8007	Sim. to TO 220, 7 Pins

SIEMENS

Preliminary

TLE 4211
Intelligent Low-Side Driver

- Double Low Side Driver, 2 x 2A
- Protection Against Reversed Polarity
- Output Power Limiting
- Overtemperature Protection
- Integrated Power-Z-Diodes
- Failure Monitoring
- Supply Voltage 5.0V . . . 32V
- Temperature Range −40°C . . . 125°C

Pin Definitions

Pin	Symbol	Function
1	Q_S	Status Output
2	I1	Control Input 1
3	Q1	Output 1
4	GND	Ground
5	Q2	Output 2
6	I2	Control Input 2
7	V_S	Supply Voltage

This device has been designed for the industrial and automotive electronics application field requiring intelligent power switches activated by logic signals, which are also short-circuit resistant and provide for error feedback.

The TLE 4211 includes two of these power switches (low-side driver). During inductive loads, the integrated power Z-diodes clamp the self-induced voltage.

By means of the TTL signals at the control inputs (active low), both switches can be activated independently of one another.

The status output (open collector) signals the following interferences through low potential:

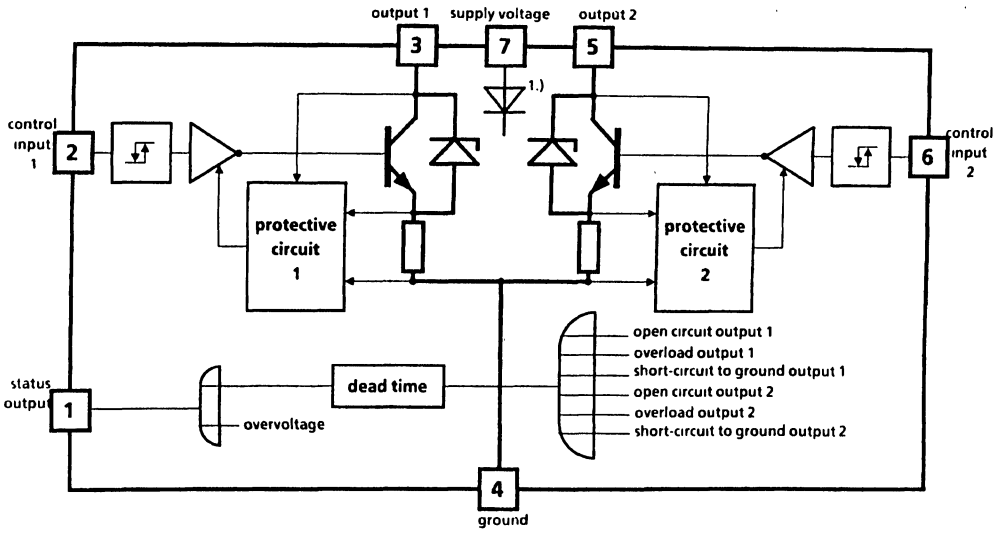
— Overload

— Open circuit

— Short-circuits to ground

— Overvoltage

Block Diagram



Note:
1. Reverse biased diode

Description of Circuitry

Input Circuits

The control inputs comprise TTL compatible Schmitt triggers with hysteresis. Driven by these stages, the inverted buffer amplifiers convert the logic signal for driving the power NPN transistors.

Switching Stages

The output stages comprise NPN power transistors with open collectors. Since the protective circuitry allocated to each stage limits the power dissipation, the outputs are short-circuit proof to the supply voltage over the entire functional range. Positive voltage peaks, which occur during the switching of inductive loads, are limited by the integrated power Z-diodes.

Monitoring and Protective Functions

The outputs during the activated status are monitored for open circuit, overload, and short-circuit to ground. In addition large sections of the circuit are deactivated in response to unduly high supply voltages V_S. Linked to the OR gate, the information regarding these malfunctions effects the status output (open collector, normally high). An internally established dead time applied to all malfunctions with the exception of overvoltage prevents the output of messages for short-term malfunctions.

Furthermore, a temperature protection circuit avoids thermal destruction. An integrated reverse diode protects the supply voltage against reversed polarities. Similarly the load is protected against reversed polarities within the limits established by the maximum ratings (no short-circuit of the load at the same time!).

At supply voltages below the functional range an undervoltage detector avoids activating of status or outputs.

Absolute Maximum Ratings

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Position	Parameter	Symbol	Conditions	Limits		Units
				Min	Max	
Voltages						
1	Supply Voltage (Pin 7)	V_S		−45	+45	V
		V_S	t ≤ 500 ms		+80	V
2	Input Voltage (Pin 2; Pin 6)	V_I		−5	+45	V
3	Output Voltage (Pin 1)	V_O		−0.3	+45	V
Currents						
4	Output Current (Pin 3; Pin 5)	I_O	$V_I = V_{IL}$; $T_G \leq 85°C$		+2.8	
5	Current with Reversed Polarity (Pin 3; Pin 5)	I_O	$T_G \leq 85°C$	−2.8		A
6	Z-Current (Pin 3; Pin 5)	I_O	$V_I = V_{IH}$, V = 1(1)		+0.5	A
7	Z-Current (Pin 3; Pin 5)	I_O	$V_I = V_{IH}$, t = 10 ms, V = 0.2(1)		+1.5	A
8	Z-Current (Pin 3; Pin 5)	I_O	$V_I = V_{IH}$, t = 1 ms, V = 0.2(1)		+2.2	A
9	Ground Current (Pin 4)	I_{GND}		−5.6	+5.6	A
10	Output Current (Pin 1)	I_{O1}			+10	mA
11	Junction Temperature	T_j			+150	°C
12	Storage Temperature	T_s		−50	+150	°C

Note:
1. See page 12. The optimal reliability and operating life of the integrated circuit is ensured, if the junction temperature does not exceed 125°C during operation. Although it is possible in principle to operate the system at a max. junction temperature of 150°C, the reliability of the IC may diminish in proportion to the duration of the max. junction temperature.

Functional Range

Within the functional range, the IC operates as described; deviations from the characteristic data are possible.

Position	Parameter	Symbol	Conditions	Limits		Units
				Min	Max	
1	Supply Voltage	V_S	(Note 1)	5.0	32	V
2	Case Temperature	T_C		−40	125	°C
Thermal Resistances						
3	System-Casing	R_{thSC}			5	K/W
4	System-Air	R_{thSA}			65	K/W

Notes
1. Lower limit = 4.2V, if $V_S \geq 5V$ before (hysteresis)

Characteristics

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not stated otherwise, typical characteristics will apply at T_C = 25°C and V_S = 12V.

Position	Parameter	Symbol	Conditions	Test Circuit	Limits			Units
					Min	Typ	Max	
General Characteristics								
1	Quiescent Current	I_S	$V_I = V_I' = V_{IH}$	1		2	4	mA
2	Quiescent Current	I_S	$V_I = V_I' = V_{IL}$	1		80	120	mA
3	Overvoltage Threshold	V_{ST}	I_O = 5 mA; V_O < 0.4V	1	34	36	38	V
4	Underload Voltage Threshold	V_{OT}	I_O = 5 mA; V_O < 0.4V	1	75	100	125	mV
5	Underload Current	I_{OU}	$V_O = V_{OU}$	1			50	mA
Logic								
	Control Input							
6	H-Input Voltage	V_{IH}		1	2.0			V
7	L-Input Voltage	V_{IL}		1			1.0	V
8	Hysteresis of Input Voltage	ΔV_I		1		0.7		V
9	H-Input Current	I_{IH}	V_I = 5V	1			10	µA
10	L-Input Current	$-I_{IL}$	V_I = 0.5V	1			10	µA
Status Output (Open Collector)								
11	L-Saturation Voltage	V_{OL}	I_O = 5 mA	1			0.4	V
12	Status Dead Time	t_{ds}	(Note 1)	1	12	20	30	µs
Switching Stages								
20	Saturation Voltage	V_{OL}	I_O = 2A; $V_I = V_{IL}$	1		0.6	0.8	V
21	Short-Circuit Current	I_{sh}	$V_O = V_S$; $V_I = V_{IL}$	1	2.2	2.5		A
22	Leakage Current	I_O	$V_O = V_S$; $V_I = V_{IH}$	1			300	µA
23	Switch-On Time	t_{dE}	Figure 2	1		50		µs
24	Switch-Off Time	t_{dA}	Figure 2	1		50		µs
25	Flow Voltage of Substrate Diode	V_{OF}	$I_O = -2.5A$	1		1.3	1.5	V
Power Z-Diode (V_S = 40V; S_1 Open)								
26	Z-Voltage	V_O	I_O = 0.1A	1	34	36	38	V
27	L-Internal Impedance	r_Z	0A < I_O < 2A	1		2		Ω

Note:
1. Time from the beginning of the interference at one channel (exception: overvoltage) until the 50% value of the status switching edge.

Test Circuit (1)

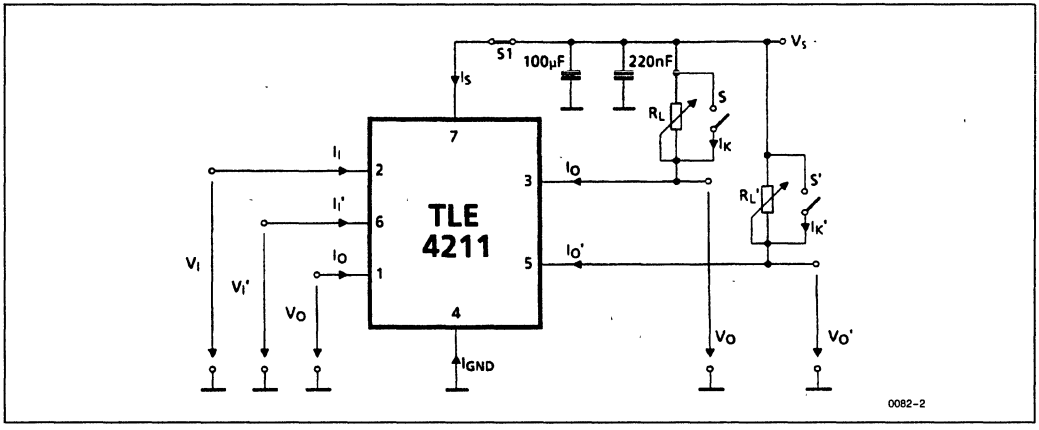


Figure 1

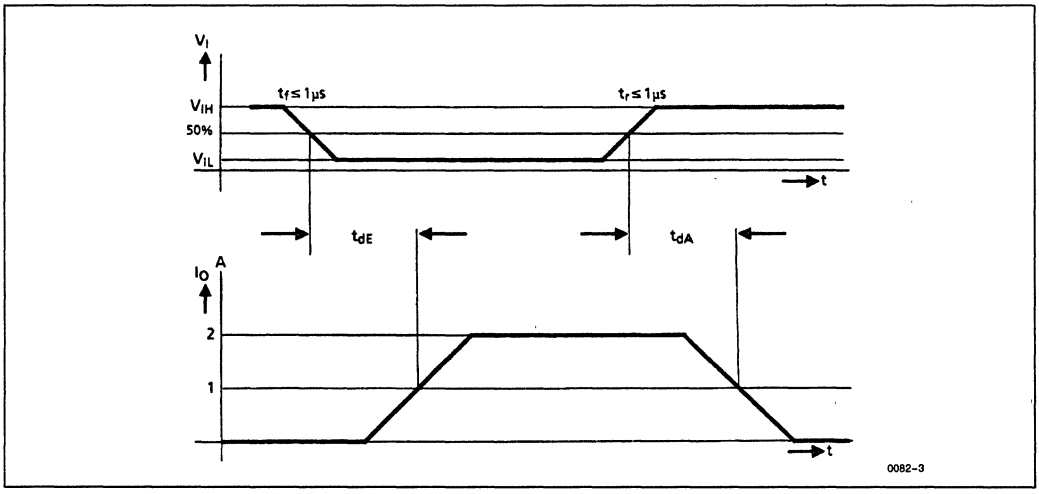
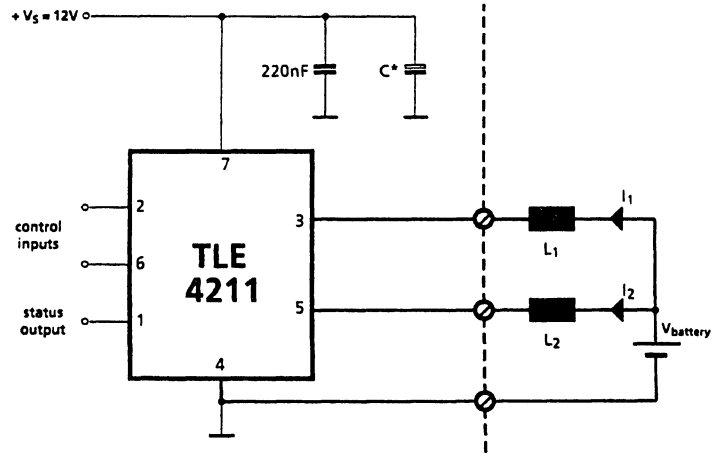


Figure 2

Application Circuit



$$C^* \geq \frac{L_1 I_1 2 + L_2 I_2 2}{(45V - V_S)^2}$$

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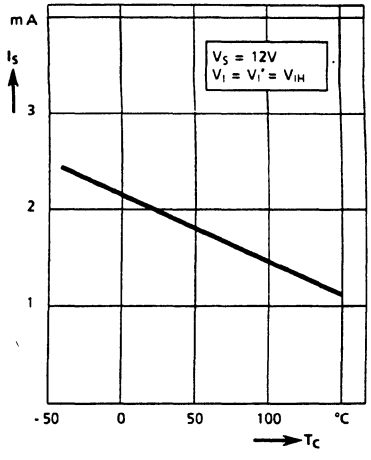
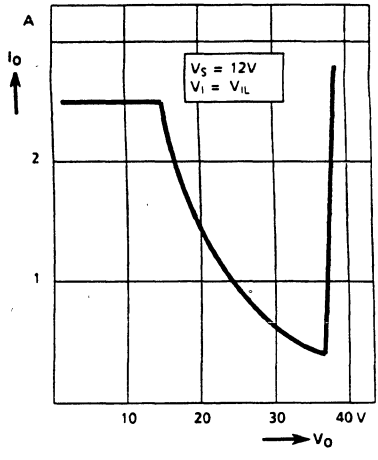
4

Diagrams

Quiescent Current I_S as a Function of the Casing Temperature T_C in the OFF Status

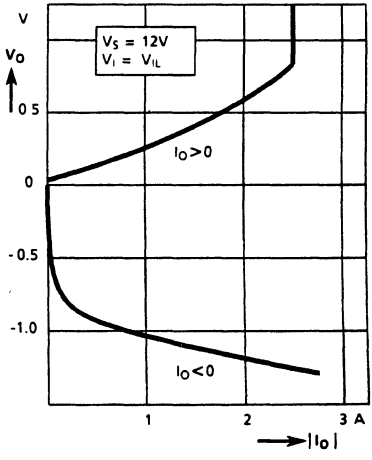


Short Current I_O as a Function of the Output Voltage V_O

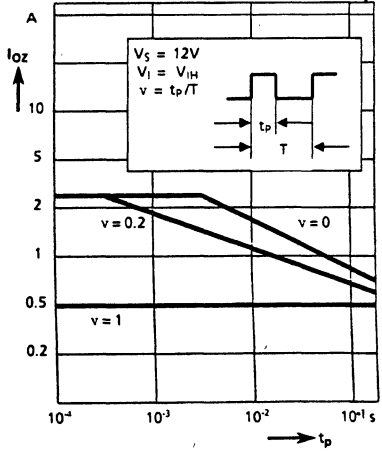


0082-5

Output Voltage V_O as a Function of the Output Currrent I_O



Permissable Z-Current I_{OZ} as a Function of the Pulse Duration t_p



0082-6

Ordering Information

Type	Ordering Code	Package
TLE 4211	Q67000-AXXXX	Similar to TO-220/7

ICs for Communications

5

SIEMENS

TBB 042 G
Mixer

The TBB 042 G is a symmetrical mixer applicable for frequencies up to 200 MHz. It can be driven either by an external source or by a built-in oscillator.

Common applications are in receivers, converters, and demodulators for AM and FM signals.

Features

- Wide range of supply voltage
- Few external components
- High conversion transconductance
- High pulse strength
- Low noise

5

Maximum ratings

Supply voltage	V_S	15	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	–40 to 125	°C
Thermal resistance (system - air)	$R_{th\,SA}$	125	K/W

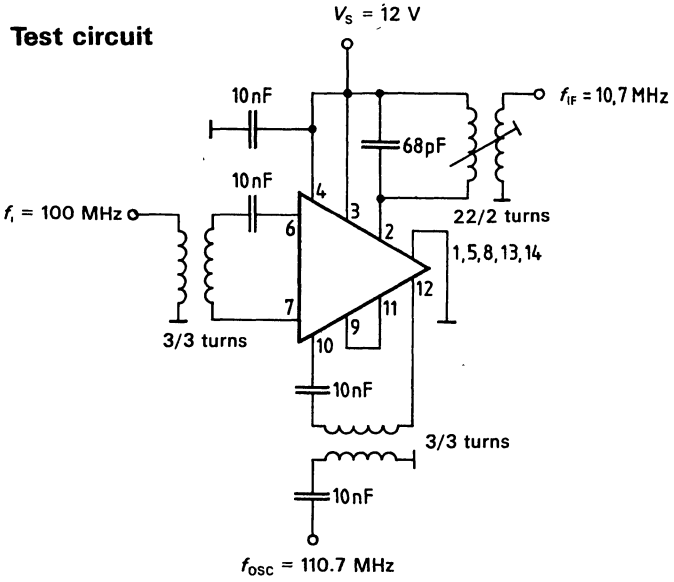
Operating range

Supply voltage range	V_S	4 to 15	V
Ambient temperature range	T_A	–15 to 70	°C

Characteristics
V_S = 12 V, T_A = 25°C

		min.	typ.	max.	
Current consumption	$I_S = I_2 + I_3 + I_5$	1.4	2.15	2.9	mA
Output current	$I_2 = I_3$	0.36	0.52	0.68	mA
Output current difference	$I_3 - I_2$	–60		60	mA
Supply current	I_5	0.7	1.1	1.6	mA
Power gain (f_i = 100 MHz, f_{OSC} = 110.7 MHz)	G_P	14	16.5		dB
Breakdown voltage ($I_{2,3}$ = 10 mA; $V_{7,8}$ = 0 V)	V_2, V_3	25			V
Output capacitance	$C_{2\text{-}M}$, $C_{3\text{-}M}$		6		pF
Conversion transductance (f = 455 kHz)	$S = \frac{I_2}{V_7\text{-}V_8} = \frac{I_3}{V_7\text{-}V_8}$		5		mS
Noise figure	NF		7		dB

Test circuit



Application circuit

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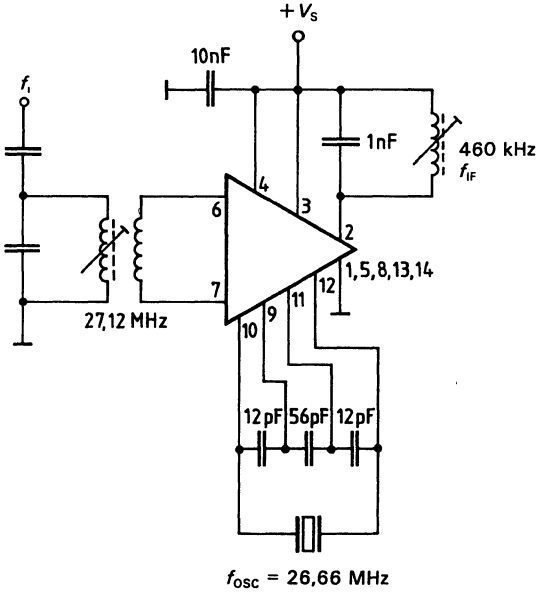
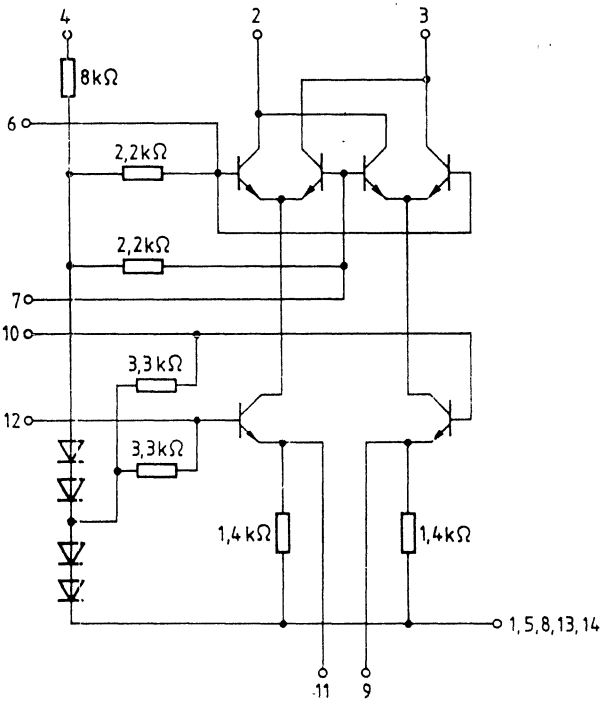
Mixer for remote control receiver

self-oscillating



For harmonic crystals, an inductor between pins 9 and 11 which will prevent oscillations on the fundamental is recommended.

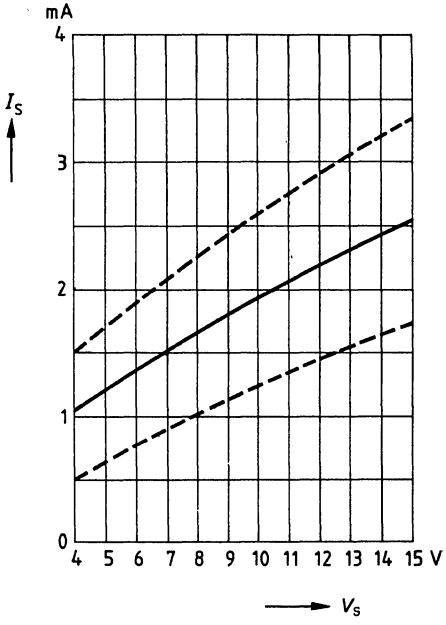
Circuit diagram



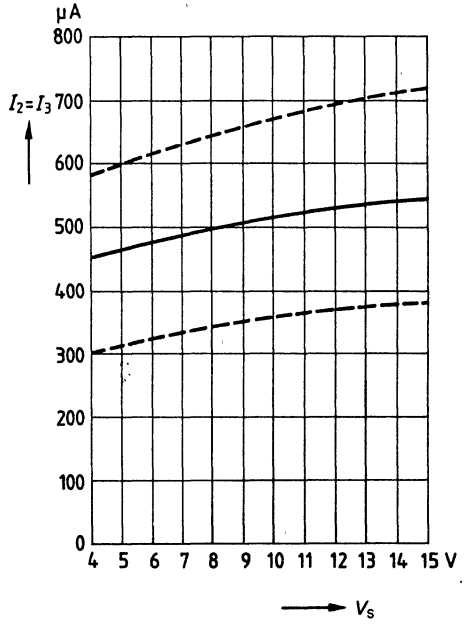
It is recommendable to establish a galvanic connection between pins 6 and 7 and pins 10 and 12 through coupling windings.

A resistor of at least 220 Ω may be connected between pins 9 and 14 (GND) and pins 11 and 14 to increase the currents and thus the conversion transconductance. Pins 9 and 11 may be connected via any impedance. In case of a direct connection between pins 9 and 11 the resistance from this connection to pin 14 may be at least 100 Ω. Depending on the layout, a capacitor (10 to 50 pF) may be required between pins 6 and 7 to prevent oscillations in the VHF band.

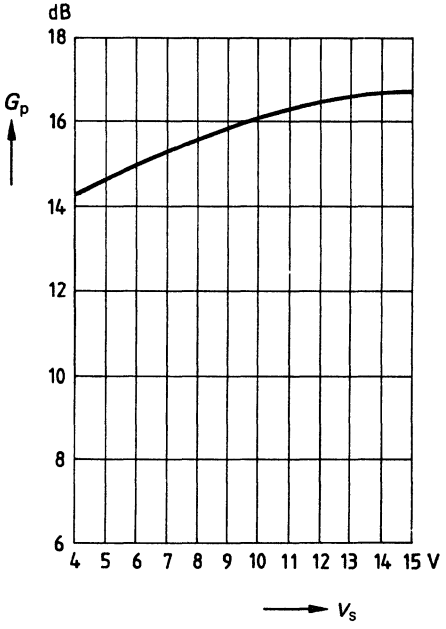
Total current consumption versus supply voltage



Output current versus supply voltage



Power gain versus supply voltage



5

SIEMENS

TBB 200, TBB 200 G
PLL Frequency Synthesizer

Type	Ordering code	Package
TBB 200	Q67100-H8215	P-DIP-14
TBB 200 G	Q67100-H8216	P-DSO-14 (SMD)

The TBB 200 is a CMOS IC which has been specially developed for use in radio equipment. It is both suitable for single frequency synthesis and dual modulus synthesis.

Features

- Bit serial control with 2 lines (I^2C bus)
- Modulus switching
- Voltage doubler for high phase-detector output voltage
- Direct VCO drive without operational amplifier
- High input sensitivity (10 mV), and high input frequencies (70 MHz) for single modulus operation
- Low supply voltage, wide temperature range
- Standby circuit
- Extremely fast phase-detector with very short anti-backlash pulse
- Large dividing ratios
  - A divider 1 to 127
  - N divider 3 to 4095
  - R divider 3 to 65535
- Switchable phase-detector polarity
- Switchable phase-detector fine tuning rate
- PORT output addressable via I^2C bus
  - for prescaler standby
  - for programming the prescaler (128 or 64)

^2C bus is a patented bus system of Philips.

Circuit Description

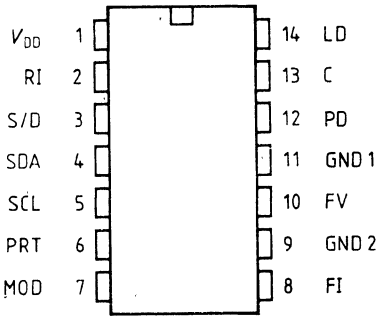
The TBB 200 is a complex PLL component in CMOS technology for processor controlled frequency synthesis. The S/D pin sets the operating mode, i.e. **S**ingle or **D**ual modulus operation. The function settings and selection of the divider ratios are made via an I²C bus interface on the SDA and SCL pins. A PRT output port enables the control of further circuits (e.g. standby). The reference frequency is supplied via the RI input; this may be up to 30 MHz. The VCO frequency is supplied via the FI pin; in single modulus operation this may up to a max. of 70 MHz and in dual modulus operation up to a max. of 30 MHz. The PLL can be operated with or without the voltage doubler as required, depending on the desired frequency variation (varicap). For operation with a voltage doubler a capacitor of typically 1 µF (MKH) should be connected to pin C. C must be grounded if the voltage doubler is not used.

The frequency f_{VD} is derived from RI. The divider factor is set via the I²C bus. The PD output supplies the phase detector signal with especially short anti-backlash pulses for the compensation of even the smallest deviations in phase. The polarity and current level of the PD output are selectable via the I²C bus. The LD output provides a static lock detector signal and the FV output supplied the divided VCO frequency. LD and FV are open drain outputs.

Operating mode	S/D	MOD
Single modulus	L	H
Dual modulus	H	L/H

5

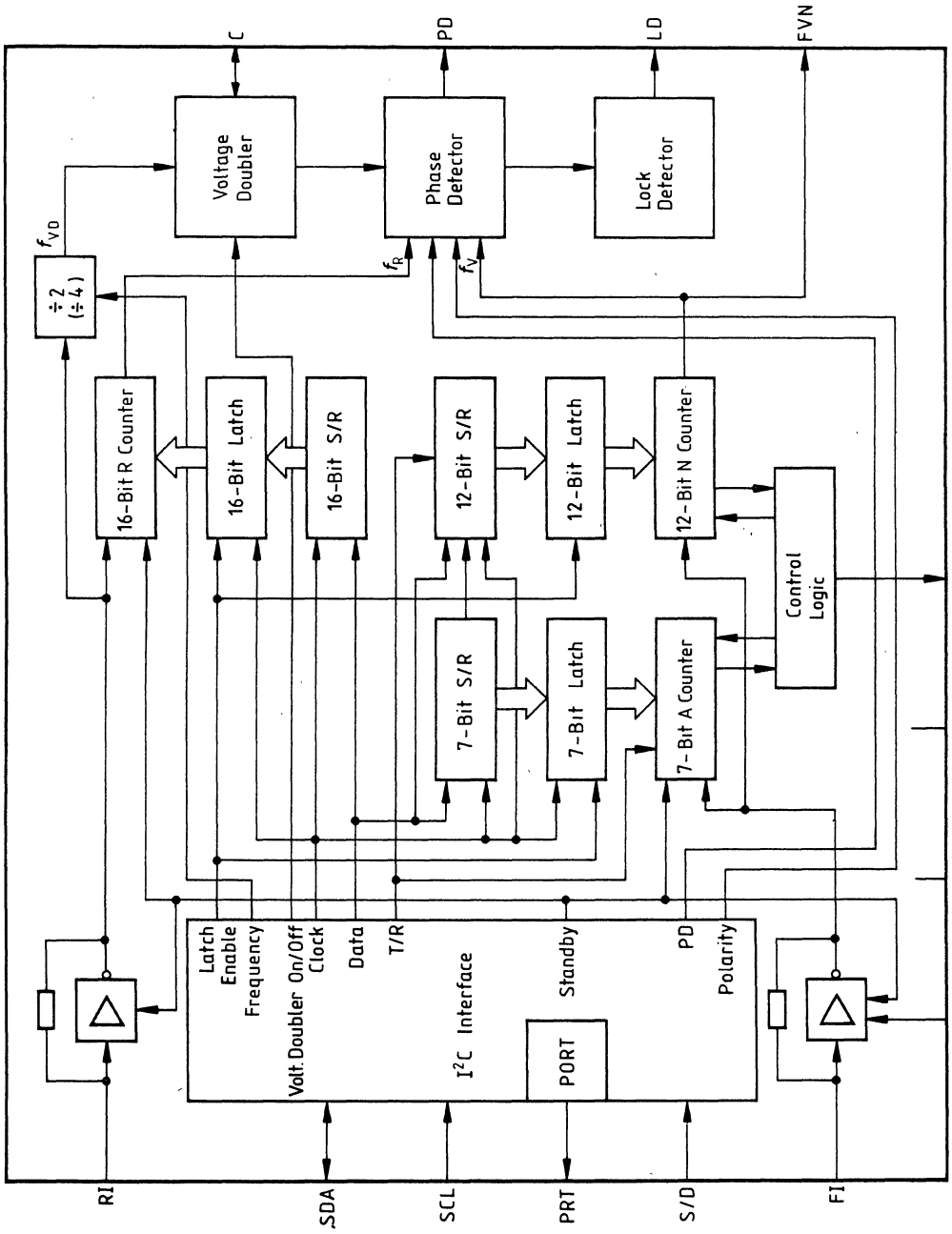
Pin Configuration
(top view)



Pin Description

Pin	Symbol	Function
1	V_{DD}	Supply voltage
2	RI	Reference frequency
3	S/D	Operating mode (single modulus/dual modulus)
4	SDA	I²C bus data
5	SCL	I²C bus clock
6	PRT	I²C PORT
7	MOD	Modulus control
8	FI	VCO frequency
9	GND 2	Ground
10	FV	Comparison frequency
11	GND	Ground
12	PD	Phase detector
13	C	Voltage doubler capacitor
14	LD	Lock detector

Block Diagram



5

Maximum Ratings

		min.	typ.	max.	Unit	Notes
Supply voltage	V_{DD}	−0.3		6	V	
Input voltage	$V_{IM\,1}$	−0.3		V_{DD} +0.3	V	
Output voltage at C	$V_{IM\,2}$	$-V_{DD}$		0	V	Exception: C
Power dissipation per output	P_Q			10	mW	(internally
Total power dissipation	P_{tot}			300	mW	generated)
Storage temperature	T_{stg}	−50		125	°C	

Operating Range

$V_{DD} = 5$ V, $T_A = 25$ °C

Supply voltage	V_{DD}	3	5	5.5	V	
Supply current single mode	I_{DD}		2.5	3.5	mA	①
dual mode	I_{DD}		2	3	mA	②
standby	I_{DD}			1	µA	③
standby preamp. on prescaler off	I_{DD}		1.5		mA	③
Ambient temperature	T_A	−40		85	°C	

Test conditions, PLL locked, RI = 10 MHz

for ①	for ②	for ③
$f_I = 50$ MHz	$f_I = 10$ MHz	$f_I = 50$ MHz
$V_{FI} = 150$ mV	$V_{FI} = 500$ mV	$V_{FI} = 150$ mV
NT, RT >1000	NT, RT >1000	Output circuitry
Operation without	Operation without	see application circuit
voltage doubler	voltage doubler	

Characteristics

		Test conditions	min.	max.	Unit
Input signals SDA, SCL					
H input voltage	V_{IH}		0.7 x V_{DD}	V_{DD}	V
L input voltage	V_{IL}		0	0.3 x V_{DD}	V
Input capacitance	C_I			10	pF
Input current	I_{IM}	$V_I = V_{DD} = 5.5$ V		10	µA
Input signal S/D					
Input voltage	V_{IH}		0.7 x V_{DD}	V_{DD}	V
L input voltage	V_{IL}		0	0.3 x V_{DD}	V
Input capacitance	C_I			10	pF
Input current	I_{IM}	$V_I = V_{DD} = 5.5$ V		10	µA
Input signal RI					
Max. input frequency	f_I	$V_{DD} = 4.5$ V	30		MHz
Input voltage	$V_{I\,rms}$	(sine)	100		mV
Input capacitance	C_I			10	pF
Input current	I_{IM}	$V_I = V_{DD} = 4.5$ V		10	µA
Input signal FI (dual modulus)					
Max. input frequency	f_I	$V_{DD} = 4.5$ V	30		MHz
Input voltage	$V_{I\,rms}$	(sine)	50		mV
Input current	I_{IM}	$V_I = V_{DD} = 4.5$ V		10	µA
Input capacitance	C_I			10	pF
Input signal FI (single modulus)					
Max. input frequency	f_I	$V_{DD} = 4.5$ V	70		MHz
Input voltage	$V_{I\,rms}$	(sine)	10		mV
Input capacitance	C_I			10	pF
Input current	I_{IM}	$V_I = V_{DD} = 4.5$ V		10	µA
Input frequency	f_I	$V_{DD} = 3$ V		35	MHz
Output signal SDA, LD (open-drain output)					
L output voltage	V_{QL}	$I_Q = 3.0$ mA $V_{DD} = 3$ V $C_L = 400$ pF		0.4	V

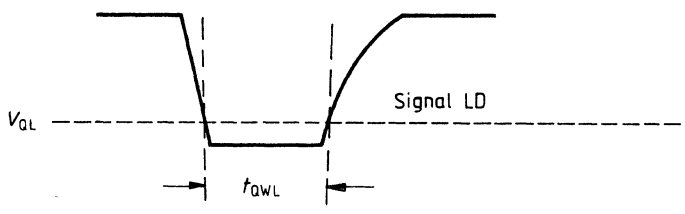
5

Characteristics

V_{DD} = 4.5 V to 5.5 V; T_A = −40 to 85 °C

		Test conditions	max.	typ.	max.	Unit
Output signal PD (tristate output)						
H current mode	I_{QH}	V_{DD} = 5 V	±1.9	±2.5	±3.1	mA
L current mode	I_{QL}		±0.475	±0.625	±0.775	mA
Tristate	I_Q	T_A = −25 to 60 °C		±50		nA
Output signal FV (open-drain output)						
L output voltage	V_{QL}	I_{QL} = 1 mA V_{DD} = 5 V C_L = 30 pF			0.4	V
L output pulse width	t_{QWL}				1/FI	
Output signals MOD, PRT (push-pull output)						
H output voltage	V_{QH}	I_{QH} = 0.5 mA V_{DD} = 5 V	V_{DD}−0.4			V
L output voltage	V_{QL}	I_{QL} = 0.5 mA V_{DD} = 5 V			0.4	V
Output signal MOD (open-drain output)						
L output voltage	V_{QL}	I_{QL} = 0.5 mA V_{DD} = 5 V			0.4	V
Output signal LD (open-drain output)						
L output voltage	V_{QL}	I_{QL} = 3 mA V_{DD} = 5 V C_L = 30 pF			0.4	V
L output pulse width	t_{QWL}			10		ns

Pulse Diagram



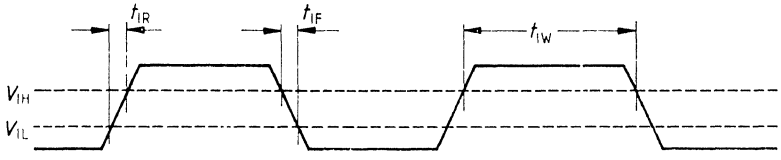
Dynamic Characteristics

$V_{DD} = 5$ V; $T_A = -40$ to 85 °C

		Test conditions	min.	max.	Unit
Input signal RI					
Rise time	t_{IR}	$V_{DD} = 5$ V	5		ns
Fall time	t_{IF}	$V_{DD} = 5$ V	5		ns
Pulse width	t_{IW}	$V_{DD} = 5$ V	5		ns
Input signal FI					
Dual modulus					
Rise time	t_{IR}	$V_{DD} = 5$ V	3.5		ns
Fall time	t_{IF}	$V_{DD} = 5$ V	3.5		ns
Pulse width	t_{IW}	$V_{DD} = 5$ V	3.5		ns
Single modulus					
Rise time	t_{IR}	$V_{DD} = 5$ V	5		ns
Fall time	t_{IF}	$V_{DD} = 5$ V	5		ns
Pulse width	t_{IW}	$V_{DD} = 5$ V	10		ns

5

Pulse Diagram



Dynamic Characteristics

$V_{DD} = 5$ V; $T_A = -40$ to 85 °C

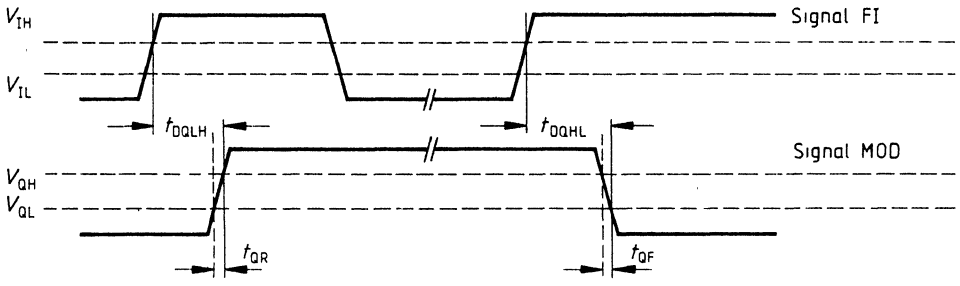
		Test conditions	min.	typ.	max.	Unit
Voltage doubler						
Output voltage	V_{QC}	$f_{VD} = 2$ MHz $I_{QC} = 0$ µA $V_{DD} = 5$ V	$-V_{DD} + 0.8$ V		V_{DD}	V
	V_{QC}	$f_{VD} = 2$ MHz $I_{QC} = 100$ µA $V_{DD} = 5$ V	$-V_{DD} + 1.5$ V		V_{DD}	V
	V_{QC}	$f_{VD} = 2$ MHz $I_{QC} = 0$ µA $V_{DD} = 3$ V	$-V_{DD} + 0.8$ V		V_{DD}	V
	V_{QC}	$f_{VD} = 2$ MHz $I_{QC} = 100$ µA $V_{DD} = 3$ V	$-V_{DD} + 1.5$ V		V_{DD}	V
Current consumption	I_{DD}	$V_{DD} = 5$ V $I_{QC} = 0$ µA $f_{VD} = 2$ MHz		250		µA
	I_{DD}	$V_{DD} = 3$ V $I_{QC} = 0$ µA $f_{VD} = 2$ MHz		180		µA

Dynamic Characteristics

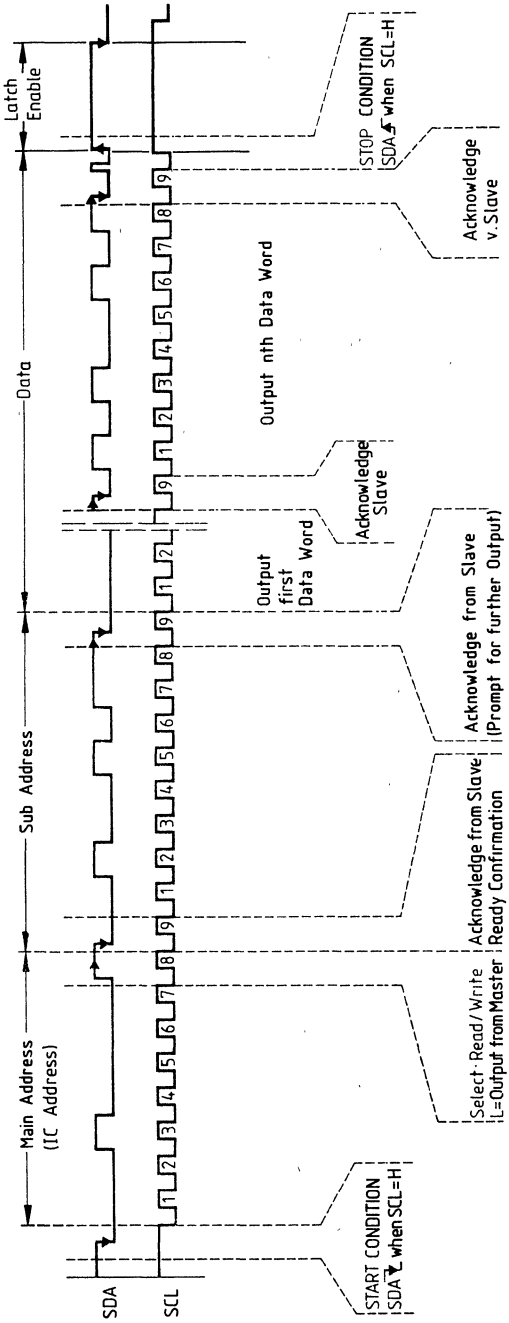
$V_{DD} = 5$ V; $T_A = -40$ to 85 °C

		Test conditions	min.	max.	Unit
Output signal PRT					
Rise time	t_{QR}	$V_{DD} = 5$ V; $C_L = 30$ pF		1	µs
Fall time	t_{QF}	$V_{DD} = 5$ V; $C_L = 30$ pF		1	µs
Output signal FV					
Fall time	t_{QF}	$V_{DD} = 5$ V, $C_L = 30$ pF		20	ns
Output signal MOD					
Rise time	t_{QR}	$V_{DD} = 5$ V, $C_L = 30$ pF		10	ns
Fall time	t_{QF}	$V_{DD} = 5$ V, $C_L = 30$ pF		10	ns
Delay time L-H on FI	t_{DQLH}	$V_{DD} = 5$ V, $C_L = 30$ pF		25	ns
Delay time H-L on FI	t_{DQHL}	$V_{DD} = 5$ V, $C_L = 30$ pF		15	ns

Pulse Diagram



Transmission Protocol for I²C Bus



Transmission Protocol for Programming

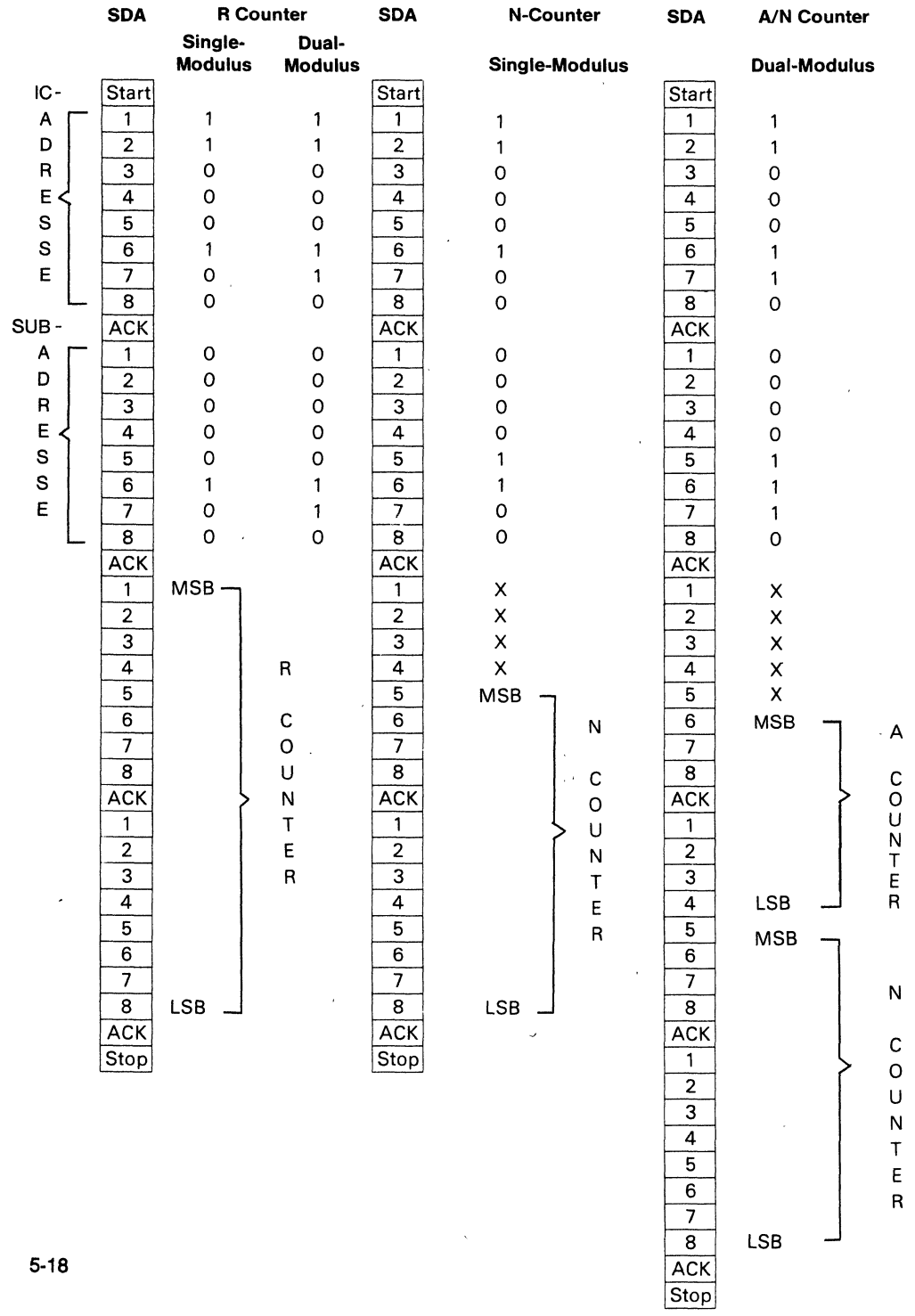
SDA		STATUS Single Modulus	Dual Modulus
Start	IC-		
1	A	1	1
2	D	1	1
3	R	0	0
4	E	0	0
5	S	0	0
6	S	1	1
7	E	0	1
8		0	0
ACK	SUB-		
1	A	0	0
2	D	0	0
3	R	0	0
4	E	0	0
5	S	1	1
6	S	0	0
7	E	0	1
8		0	0
ACK			
1		PORT	
2	S	Counter	
3	T	FI, RI	
4	A	PD-Polarity	
5	T	PD-Current	
6	U	Voltage-Doubler Frequency	
7	S	Voltage-Doubler Status	
8		Modulus Output	
ACK			
Stop			

Statusbit 0	1
Low**	High**
off*	on
off*	on
neg.	pos.
0,625 mA	2,5 mA
÷ 2	÷ 4
off	on
push pull	open drain

5

* Standby
** PORT-output state

Transmission Protocol for Programming

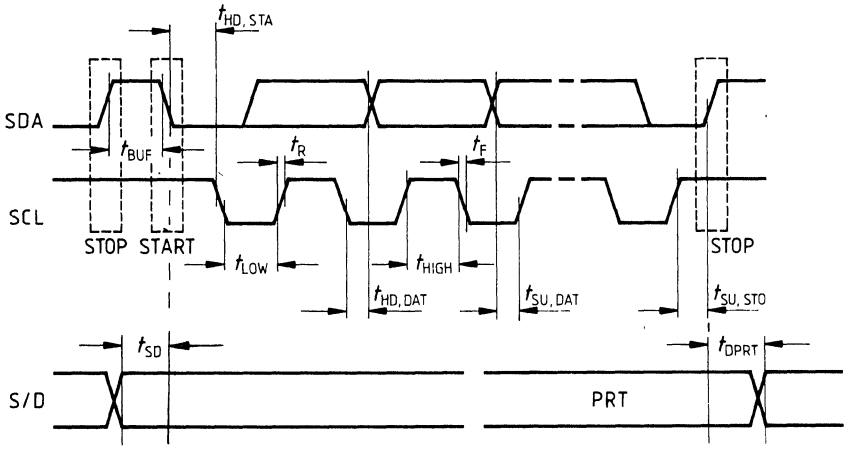


		min.	max.	Unit
Clock frequency	f_{SCL}	0	100	kHz
Hold period for data at SCL LOW	$t_{HD, DAT}$	0		µs
Inaktive period before restart of transmission	t_{BUF}	4.7		µs
Start condition hold time (the first CLOCK pulse is generated after this period)	$t_{HD, STA}$	4.0		µs
Clock LOW phase	t_L	4.7		µs
Clock HIGH phase	t_H	4.0		µs
DATA set-up time	$t_{SU, DATA}$	250		ns
SDA and SCL signal rise time	t_R		1	µs
SDA and SCL signal fall time	t_F		300	ns
SCL clock set-up time on STOP condition	$t_{SU, STOP}$	4.7		µs
Set-up time for status (S/D) programming	t_{SD}	500		ns
PRT delay time relative to stop condition	t_{DPRT}		500	µs

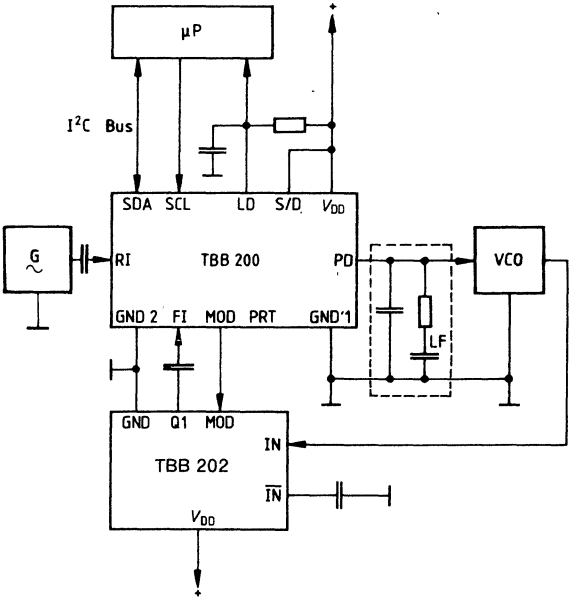
All figures are referred to the specified input levels V_{IH} and V_{IL}.

5

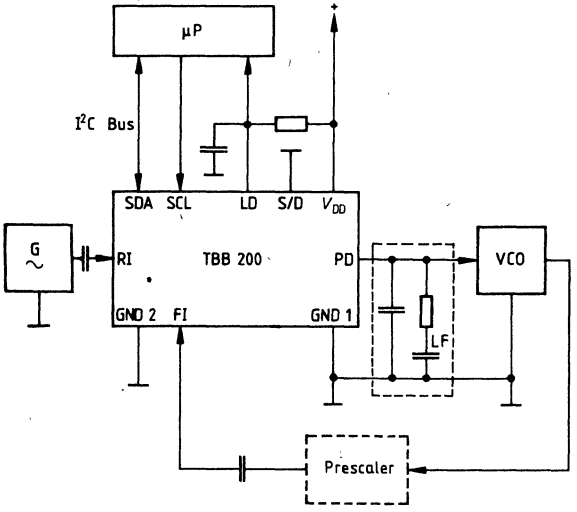
Pulse Diagrams for I²C Bus, S/D, PRT



Application Circuits

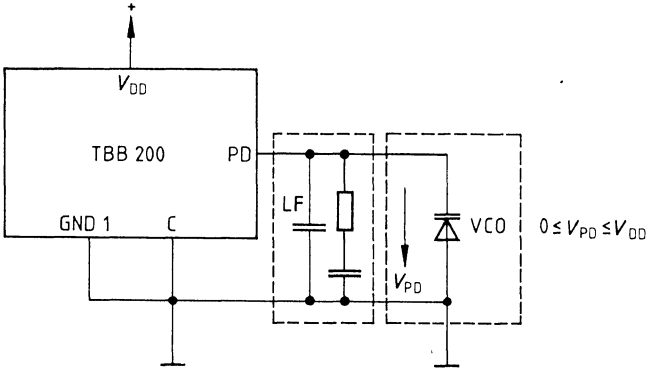


Operation: Dual modulus (f_{max} = 30 MHz on FI)

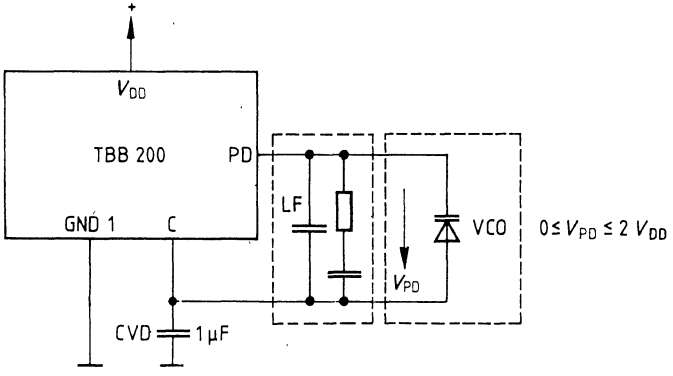


Operation: Single modulus (f_{max} = 70 MHz on FI)
LF: loop filter

Application Circuit for VCO Coupling

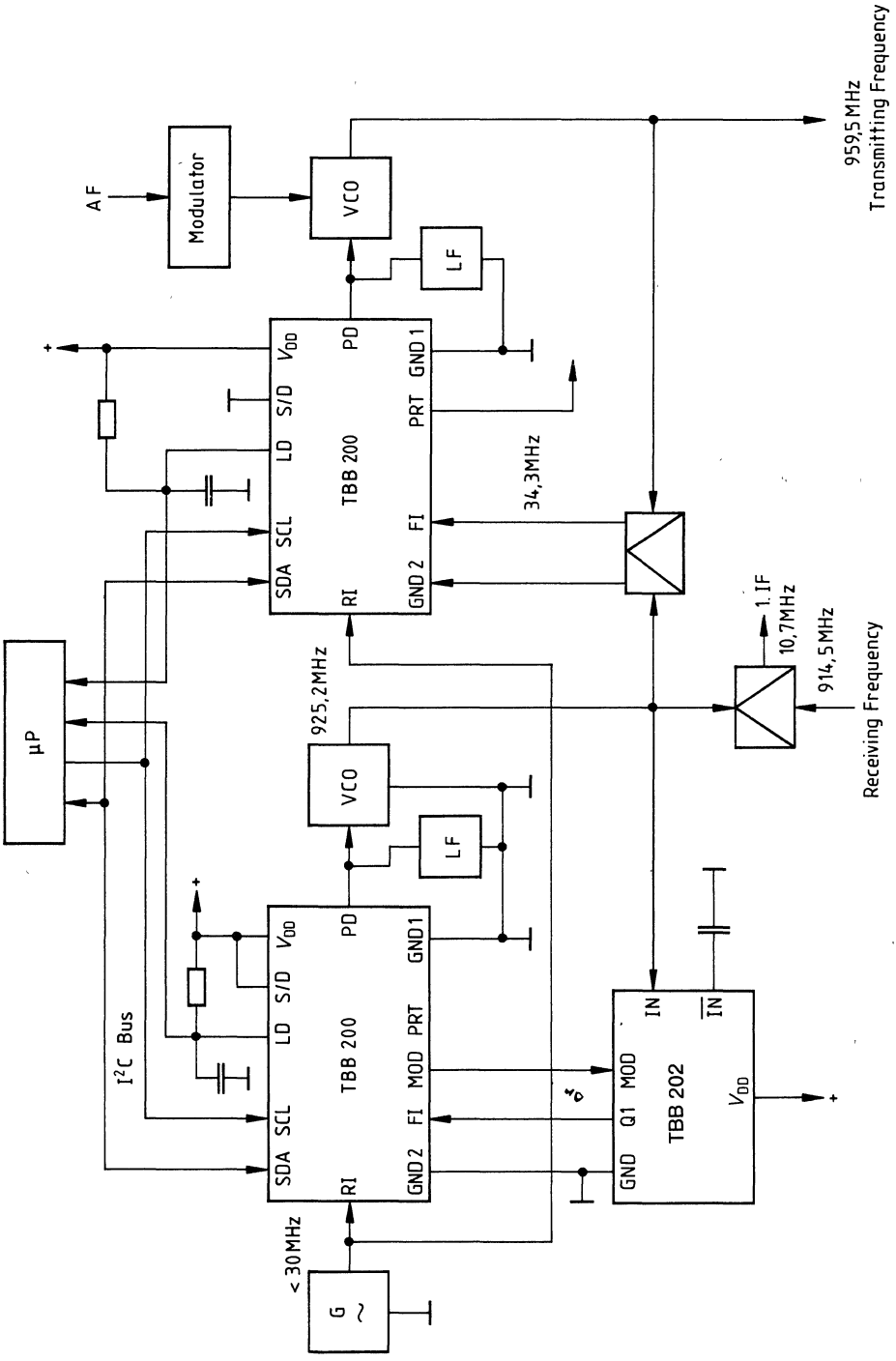


Operation without voltage doubler (status bit 7 = 0)



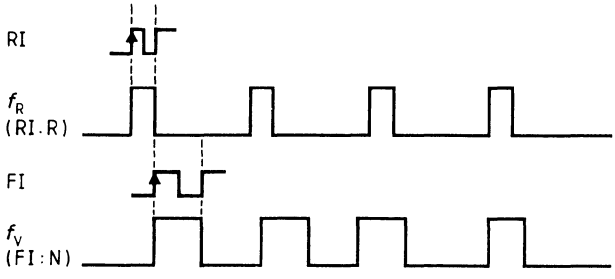
Operation without voltage doubler (status bit 1 = 0)
LF: loop filter

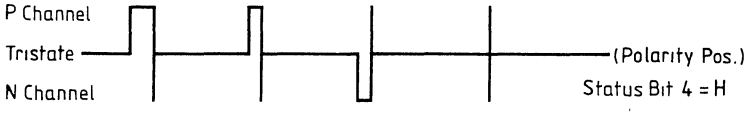
Application Example for Radio Equipment and Radio Telephones in the 900 MHz Region



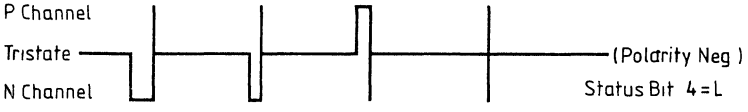
Pulse Diagram

Phase Detector

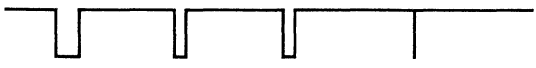




PD



LD



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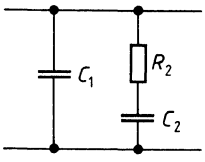
The following requirements are made for the loop filter configuration:

a) the PLL should behave as a PT_2 network,
b) an additional time constant should provide effective attenuation of the reference frequency lines in the spectrum.

The network shown satisfies these requirements.

Loop filter



$$F(S) = \frac{1 + s\tau_2}{sC_1\,(1 + s\tau_2 \frac{1}{K})} \qquad (1)$$

$$\tau_2 = C_2 \times R_2$$

Fig. 1

According to Gardner /1/ this circuit corresponds to a PLL, type 2, 3rd order. A deeper examination of this control circuit can be made in the Bode diagram **(fig. 3)**.

Complete control circuit with corresponding frequency response of the open loop circuit.

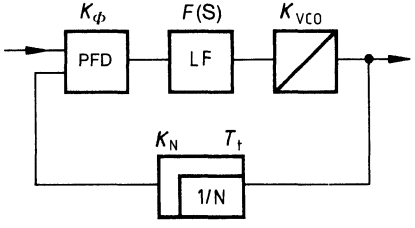


Fig. 2

$$F_O = \frac{K_{VCO}\,K_\phi\,K_N\,(1 + s\tau_2)e^{sT_t}}{sC_1\,(1 + s\tau_2 \frac{1}{K})} \qquad (2)$$

$$K = \frac{C_2}{C_1} + 1$$

Bode diagram for the open loop control circuit, normalised to $\omega_N = 1$

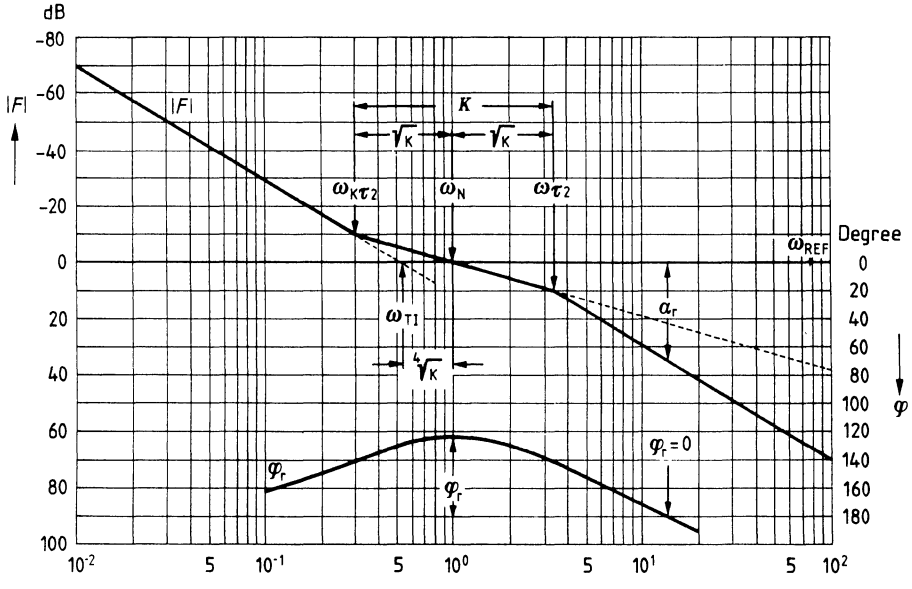


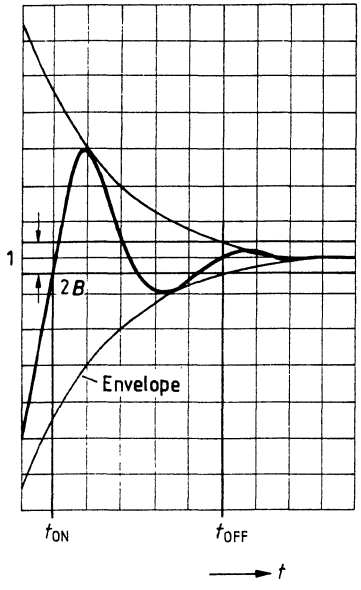
Fig. 3

In this diagram a point ω_N is indicated where the true curve cuts the asymptotic amplitude characteristic. Also the phase edge ω_r reaches its maximum exactly at this point, which can be calculated from $\omega_N = \sqrt{\omega\tau_2 \times \omega\tau_2 \times K}$ (3)

In the region of this point the amplitude characteristic approaches a positive slope of 20 dB/dec. There is therefore the possibility of being able to describe the control circuit with the PT_2 parameter attenuation d and the self-resonant frequency ω_N. In order to obtain the required phase edge at the point ω_N, the ratio K of the time constants **(see fig. 2)** is varied.

With regard to applications it is interesting to know after which period *t* a given tolerance band *B* is entered but not left again for a step change in frequency. The step response of a PT_2 network is therefore analysed with $d < 1$.

Transient Response



$$h(t) = M\left[1 + \frac{e^{-d\omega t}}{\sqrt{1-d^2}} \sin\left(\sqrt{1-d^2}\ \omega_N t + \varphi\right)\right] \qquad (4)$$

Fig. 4

The computational formulae result from these observations. The chosen attenuation factor *d*, the stabilization period T_{OFF} and the tolerance band *B*. The natural frequency ω_N can be calculated from these given parameters.

$$\omega_N = \frac{-\ln (B\sqrt{1-d^2})}{d \times T} \quad (5)$$

$$A = \mathrm{tg}\left(\frac{\omega_N}{\omega_{REF}} + \arctan(2d)\right) \quad (6)$$

$$K = (A + \sqrt{A^2+1})^2 \quad (7)$$

The relationship 7 can be simplified for the case $\omega_N \ll \omega_{REF}$ to

$$K = (2d + \sqrt{4d^2+1})^2$$

If the parameters K_Φ, K_{VCO} and N are known, the loop filter elements C_1, C_2 and R_2 can be calculated.

$$C_1 = \frac{K_{VCO} \times K_\Phi}{N \omega_{N^2} \times \sqrt{K}} \quad (8)$$

$$C_2 = (K-1)\, C_1 \quad (9)$$

$$R_2 = \frac{\sqrt{K}}{\omega_N \times C_2} \quad (10)$$

5

Application Example

The frequency range should be varied in steps of 25 kHz with half channel displacement. The reference frequency is therefore set to f_{REF} = 12.5 kHz. The IF bandwidth is 6 kHz. For a change of channel, the oscillator frequency should have be so close to the final frequency in the given time of 10 ms, that the channel can be evaluated. The tolerance band is chosen as ¼ of the IF bandwidth.

$$B = \frac{1{,}5\ \text{kHz}}{25\ \text{kHz}} = 0{,}06$$

Phase detector constant $K_\Phi = \frac{I - (-I)}{4\pi} = 0{,}318\ \frac{\text{mA}}{\text{rad}}$

VCO constant $K_{VCO} = 5{,}03 \times 10^6\ \frac{\text{rad}}{\text{Vs}}$

$d = d_{opt} = 0{,}7$

$f_{min} = 900,0125\ \text{MHz}$ $\quad$ $f_{max} = 900{,}9875\ \text{MHz}$

$N_{min} = \frac{f_{min}}{f_{REF}} = 72001$ $\quad$ $N_{max} = \frac{f_{max}}{f_{REF}} = 72079$

The PLL should be designed for the average dividing factor N:

$$\overline{N} = \sqrt{N_{max} \times N_{min}} = 72040$$

$$\omega_N = \frac{-\ln (B\sqrt{1 - d^2})}{d \times T_{off}} = 450\ 1/\text{s}$$

$$A = \tan \left(\frac{\omega_N}{\omega_{REF}} + \arctan (2d) \right)$$

$$K = (A + \sqrt{A^2 + 1})^2$$

$$C_1 = \frac{K_\Phi\ K_{VCO}}{N \times \omega_N^2 \times \sqrt{K}} = 34{,}8\ \text{nF}$$ $\quad$ 33 nF selected

$$C_2 = (K - 1)\ C_1 = 308\ \text{nF}$$ $\quad$ 300 nF selected

$$R_2 = \frac{\sqrt{K}}{\omega_N \times C_2} = 22{,}6\ \text{k}\Omega$$ $\quad$ 22.6 kΩ selected

Explanation of Symbols:

PFD	Phase Frequency Detector
N	Divider ratio
f_{VCO}	VCO frequency
K_N	Transfer coefficient of the divider
K_Φ	Transfer coefficient of the PFD
K_{VCO}	Transfer coefficient of the VCO
T_d	Dead time
f_{REF}	Reference frequency
F_o	Frequency response of the open loop control circuit
K	Ratio relationship of the time constants
B	Tolerance band
T_{off}	Setting time
d	Attenuation damping factor
ω_N	Natural frequency of the loop
I	Output current of the PFD

5

Literature:

Gardner, Floyd: Charge-Pump Phase Locked Loops
IEEE Vol. COM-28, 11.80

ICs for Sensing Applications

6

SIEMENS

HKZ 101
Hall-Effect Vane Switch

The Hall-effect vane switch HKZ 101 is a contactless switch consisting of a monolithic integrated Hall-effect circuit and a special magnetic circuit hermetically sealed in a plastic package. The switch is actuated by a shoft-iron vane which is passed through the air gap between magnet and Hall sensor.

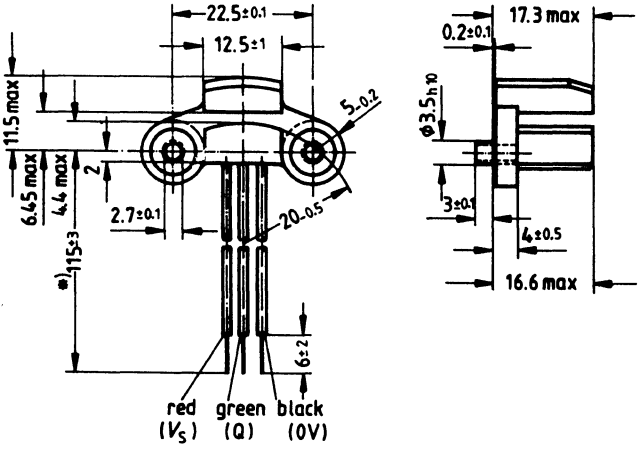
The main application field is in cars, i.e. as a breakerless trigger in electronic ignition systems. Numerous industrial applications can be found in control engineering, especially in those areas where switches must operate maintenance-free under harsh environmetal conditions (e.g. rpm sensor, limit switch, position sensor, speed measurement, shaft encoder, scanning of coding disks, etc.).

Features

- Contactless switch with open collector output (40 mA)
- Static switching
- High switching frequency
- Hermetically sealed with plastic
- Unaffected by dirt, light, vibration
- Large temperature and voltage range
- Integrated overvoltage protection
- High interference immunity

6

Special package



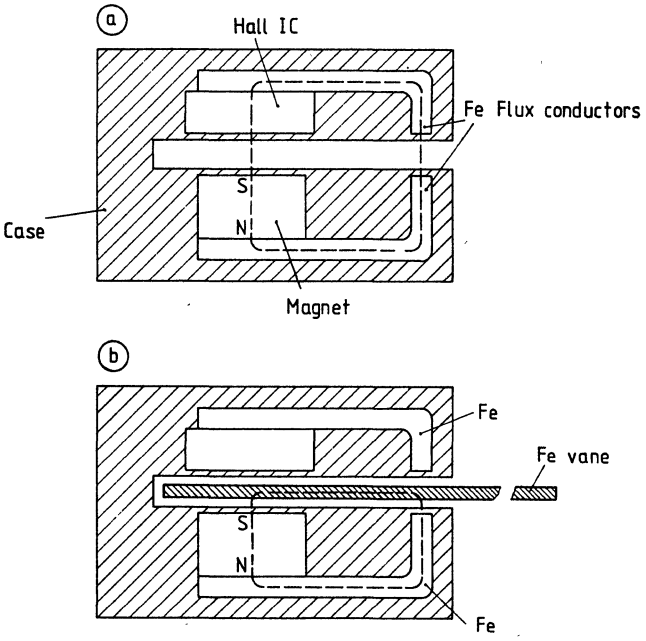
*) Change to 130±3 mm in preparation

Function

The Hall-effect switch is actuated by a soft-iron vane that passes through the air gap between magnet and Hall-effect sensor. The vane short-circuits the magnetic flux before the Hall-effect sensor, as shown in figure 1. The open collector output is conductive (LOW) when the vane is outside the air gap, and blocks (HIGH) when the vane is introduced into the air gap. The output remains HIGH as long as the vane remains in the air gap. This static function does not require a minimum operating frequency. The output signal shape is independent of the operating frequency.

The circuit features integrated overvoltage protection against most of the voltage peaks occurring in automotive and industrial applications. The output stage has a Schmitt trigger characteristic. Most electronic circuits can be driven directly due to the open collector output current of max. 40 mA.

Principle of operation



a) Magnetic flux through the Hall-effect switch with no vane in the gap

b) Magnetic flux short-circuited by the soft-iron vane

Figure 1

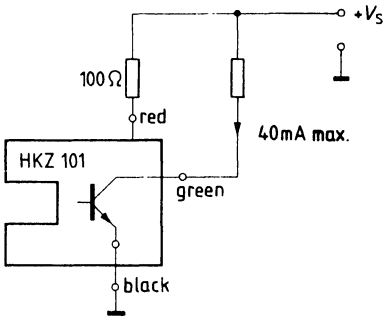
Mechanical characteristics

The Hall-effect vane switch is hermetically sealed in a special plastic, so that it can also be used under harsh environmental conditions. The package is waterproof, vibration-resistant and resistant to gasoline, oil and salt. Two tubular rivets are incorporated in the package to mount the sensor on its carrier plate. The circuit has three flexible leads for power supply and output.

Application notes

The output current of the "open collector" must be limited to the maximum permissible value by a load resistor adapted to the application.

For optimum efficiency of the integrated overvoltage protection, it is suggested that a resistor of approx. 100 Ω be provided in the component's power supply to limit the current.



Maximum ratings		Test conditions	Lower limit B	Upper limit A	
Supply voltage	V_S		−1.2	24	V
		T_{amb} = 25 °C		30	V
Output voltage in OFF-state	V_Q		−0.8	30	V
Inverse supply current (limited externally)	$-I_S$	$T_{amb} \leq 80$ °C $t \leq 1$ h		200	mA
Output current	I_Q	without vane		40	mA
Inverse output current	$-I_Q$			30	mA
Ambient temperature during operation	T_{amb}		−40	135	°C
Storage temperature	T_{stg}		−40	150	°C
Thermal resistance (system-air)	$R_{th\,SA}$			170	K/W

Operating range					
Ambient temperature	T_{amb}		−40	130	°C
Supply voltage	V_S		4.5	24	V
Vane[1]: thickness	a		0.5		mm
width	b		8		mm
gap length	c		8		mm
immersion depth	h		4.6	9	mm
gap height	d		17.3−h		mm

1) see figure 3

Characteristics V_S = 5 V to 18 V; T_{amb} = −30 °C to 130 °C		Test conditions	Lower limit B	Upper limit A	
Output saturation voltage	$V_{Q\,sat}$	without vane I_Q = 40 mA T_{amb} = −30 to 110 °C T_{amb} = 110 to 130 °C		0.4 0.6	V V
Output reverse current	I_{QR}	with vane		10	µA
Supply current	I_S	without vane		12	mA
Delay time	t_{LH}, t_{HL}	I_Q = 40 mA		1	µs
Overvoltage protection					
– Supply voltage (V_S)	V_{SZ}	I_S = 16 mA	32	42	V
– Output (V_Q)	V_{SO}	I_S = 16 mA	32	42	V

Switching point characteristics

Definitions

In most applications, the switching point is set exactly by mechanical adjustment, thus compensating all mechanical tolerances in the system including the scatter of the Hall-effect vane switch. For the function of the device in operation, only the deviations of those characteristics depending on temperature and operating voltage are important.

The characteristic values of the switching points are, therefore, not directly referred to the mechanical dimensions of the vane switch, but to an electrically defined symmetry B_0 according to formula 1):

1) $B_0 = (ON_{left} + OFF_{left} + ON_{right} + OFF_{right}) : 4$
$B_0 = A_0 \pm 0.3$ mm

The definition of the operate and release points is shown in figure 2.

Operate point f_{ON} is obtained by subtracting the measured ON operate value from the reference point B_0:

2) $f_{ON} = ON_{right} - B_0 = B_0 - ON_{left}$

The release point f_{OFF} is calculated from the difference between the appropriate ON and OFF points:

3) $f_{OFF} = ON_{right} - OFF_{right} = OFF_{left} - ON_{left}$

$f_{ON\,0}$ and $f_{OFF\,0}$ are the switching points measured for the individual component under normal conditions (V_S = 12 V, T_{amb} = 25 °C) within the characteristic device deviation

The deviations of the operate and release points are defined according to 4):

4) $\Delta f_{ON} = f_{ON} - f_{ON\,0}$
$\Delta f_{OFF} = f_{OFF} - f_{OFF\,0}$

Switching point definitions

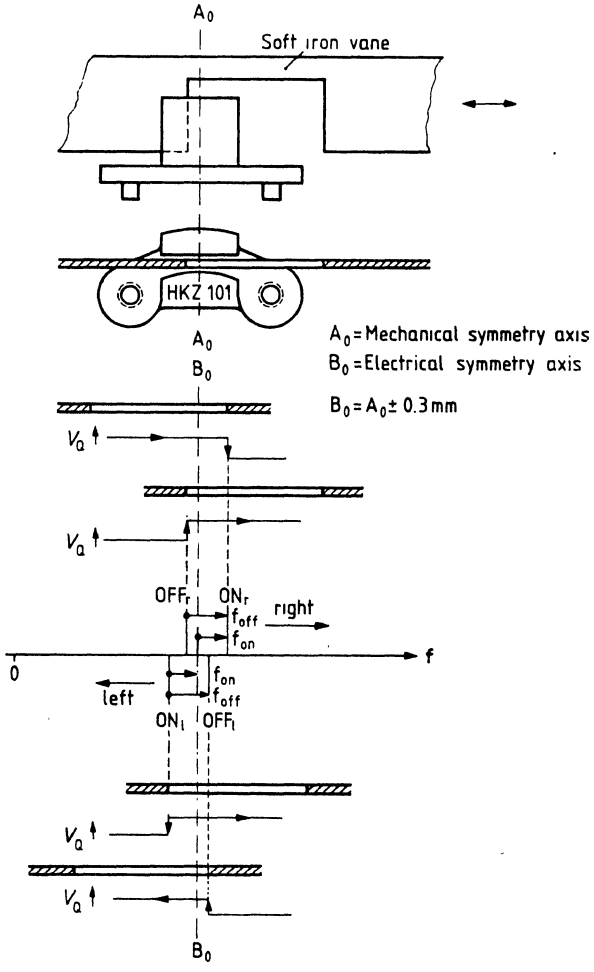


Figure 2

Mechanical measurement conditions

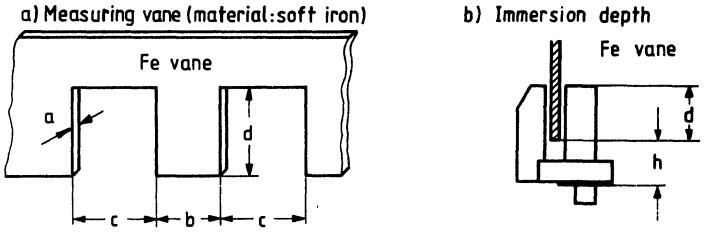


Figure 3

Switching point characteristics

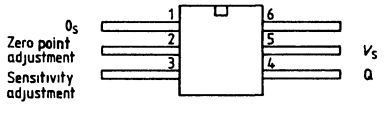
Vane: a = 0.75 mm, b = 8 mm, c = 10 mm
Position: center of air gap
V_S = 5 V to 18 V

		Test conditions	Lower limit B	typ	Upper limit A	
HKZ 101						
Operate point	$f_{ON\,0}$	V_S = 12 V, T_{amb} = 25 °C	0.85	1.45	2.05	mm
Deviations	Δf_{ON}	T_{amb} = −30 to 25 °C	−0.4	+0.15	+0.7	mm
		T_{amb} = 25 to 80 °C	−0.2	+0.15	+0.4	mm
		T_{amb} = 80 to 130 °C	−0.4	+0.2	+0.7	mm
Release point	$f_{OFF\,0}$	V_S = 12 V, T_{amb} = 25 °C	1.54	2.54	3.54	mm
Deviations	Δf_{OFF}	T_{amb} = −30 to 25 °C	−0.8	+0.3	1.4	mm
		T_{amb} = 25 to 80 °C	−0.4	+0.3	0.8	mm
		T_{amb} = 80 to 130 °C	−0.8	+0.4	1.4	mm

SIEMENS

SAS 231 W
Hall-Effect IC with Output Voltage Proportional to Magnetic Field

Pin Configuration



The IC SAS 231 generates an output voltage proportional to the magnetic flux density. The output voltage increases when the south pole of a magnet approaches the top surface of the chip. The zero point is adjusted by external components. The steepness of the characteristic curve V_Q as a function of B can be varied by external components.

Absolute Maximum Ratings*

Supply Voltage (V_S) ..... 0V to +18V
Output Current (I_Q) ..... 10 mA
Storage Temperature (T_{stg}) ..... −40°C to +125°C

Operating Range

Supply Voltage (V_S) ..... 4.75V to 15V
Output Current (I_Q) ..... 5 mA
Ambient Temperature (T_A) ..... 0°C to 70°C

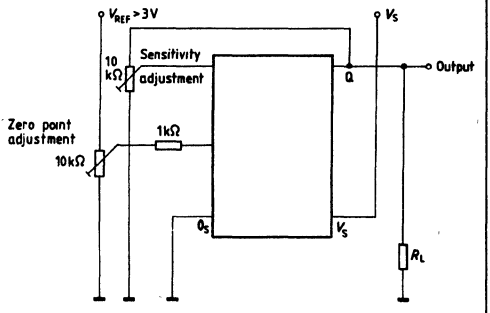
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

6

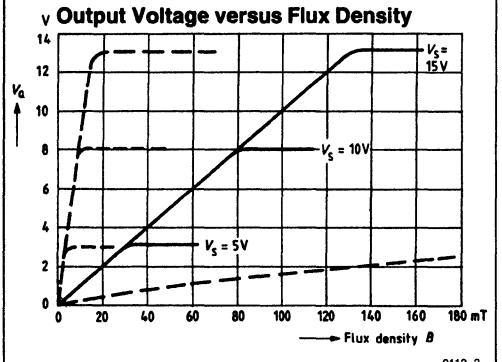
Electrical Characteristics V_S = 10V, T_A = 25°C, unless otherwise specified

Parameter	Symbol	Conditions	Limits			Units
			Min	Typ	Max	
Open-Loop Supply Current Consumption	I_S	$R_L = \infty$		6	10	mA
Output Voltage	V_Q	R_L = 10 kΩ	0.05		$V_S - 2$	V
Steepness (without Adjustment)	S		60	100	140	mV/mT
"Zero" Component Linearity Error	B_0	V_Q = 0.5V	−35		35	mT
$\left(\text{Referred to } V_Q = \frac{V_S}{2}\right)$				2		%
Temperature Coefficient	α	T_A = 0°C to +70°C		0.4		mT/k

Application Circuit



Output Characteristic without Adjustment

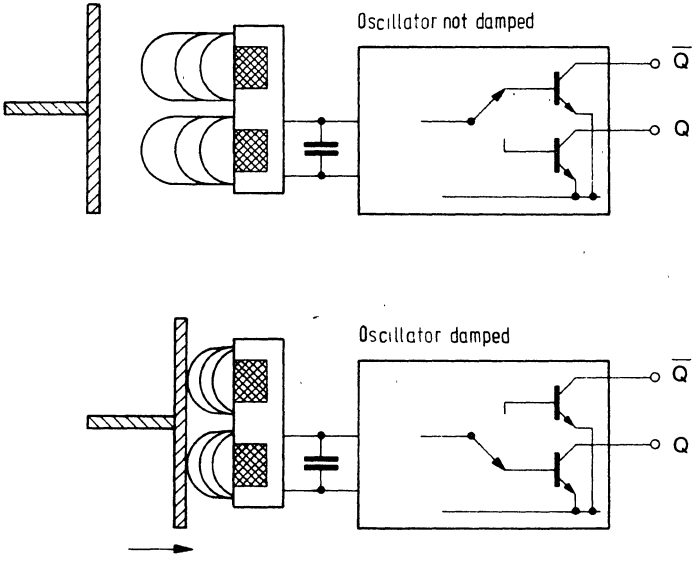


SIEMENS

TCA 205 A; K
Proximity Switch

This IC is intended for applications in inductive proximity switches. The outputs switch when the oscillation is damped, e.g. by the approach of a metal object.

Operation schematic



Features

- Large supply voltage range
- High output current
- Antivalent outputs
- Adjustable switching distance
- Adjustable hysteresis
- Turn-on delay

Maximum ratings

Supply voltage	V_S	30	V
Output voltage	V_Q	30	V
Output current	I_Q	50	mA
Junction temperature	T_j	125	°C
Storage temperature range	T_{stg}	−55 to 125	°C
Thermal resistance (system-air) TCA 205 A	$R_{th\,SA}$	85	K/W

Operating range

Supply voltage	V_S	4.75 to 30	V
Ambient temperature	T_A	−25 to 85	°C

Characteristics

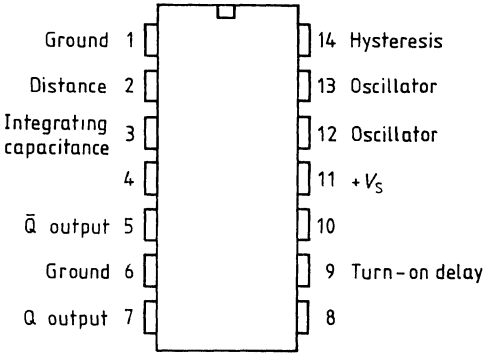
$V_S = 12$ V; $T_A = 25$ °C

		Test conditions	Lower limit B	typ	Upper limit A	
Open-loop supply current consumption	I_S	open pins		1	2	mA
L output voltage per output	V_{QL}	$I_{QL} = 5$ mA		0.8	1	V
	V_{QL}	$I_{QL} = 50$ mA		1.25	1.5	V
H output current per output	I_{QH}	$V_{QH} = 30$ V			10	µA
Integrating capacitance	C_I			10		nF
Internal resistance at 3	R_{j3}		200	350	660	kΩ
Threshold voltage at 3	V_{S3}			1.3	1.5	V
Distance adjustment (circuit 1)	R_{di}		6			kΩ
Hysteresis adjustment (circuit 1)	R_{hy}		0			kΩ
Distance adjustment (circuit 2)	R_{di}	$R_{hy} \rightarrow \infty$	6[1]			kΩ
Hysteresis adjustment (circuit 2)	R_{hy}	$R_{di} \rightarrow \infty$	6[1]			kΩ
Turn-on delay	t_{don}			200		ms/µF
Oscillating frequency	f_{OSC}		0.015		1.5	MHz
Switching frequency without C_I	f_s				5	kHz

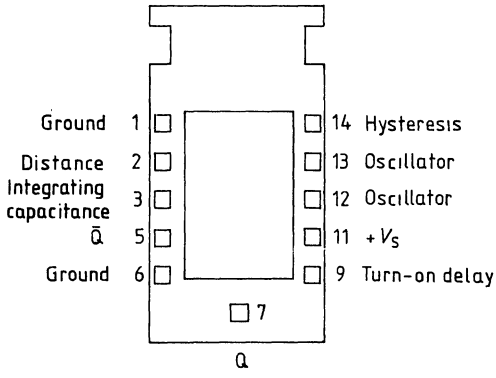
1) Parallel connection of R_{hy} to R_{di} may at least amount to 6 kΩ

Pin configurations

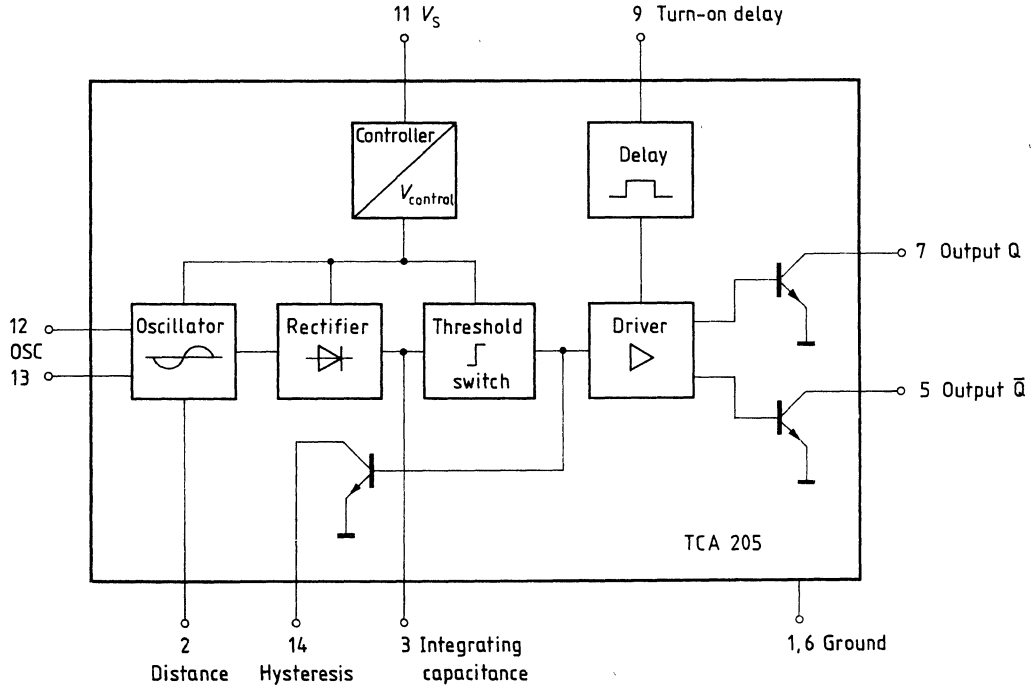
TCA 205 A



TCA 205 K

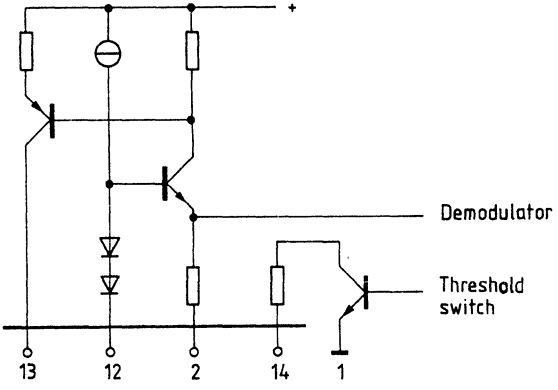


Block diagram

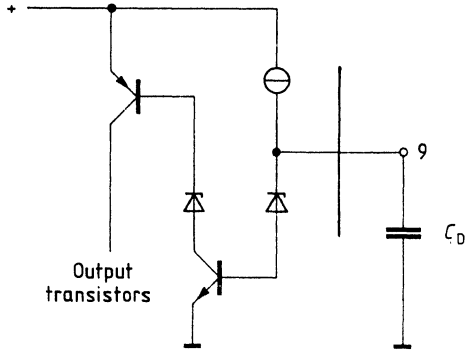


Schematic circuit diagrams

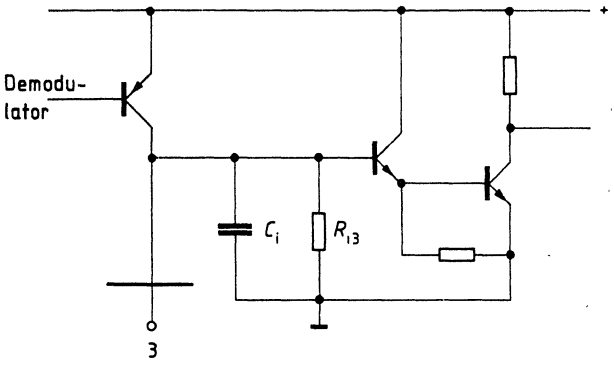
Oscillator



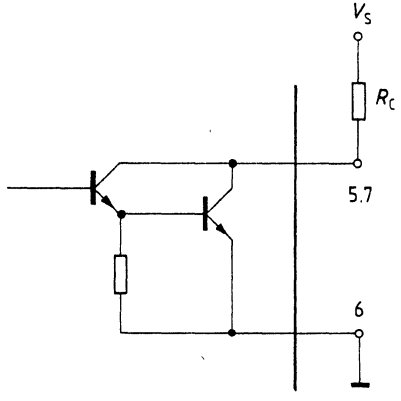
Turn-on delay



Integrating capacitor

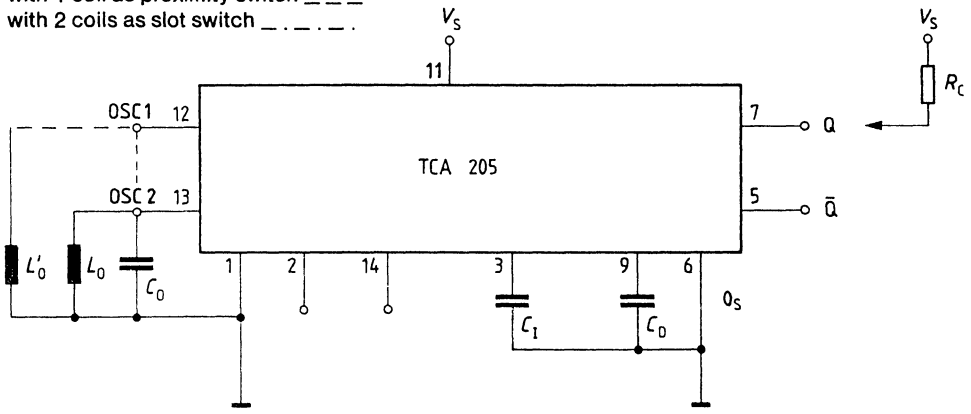


Outputs



Application circuit

with 1 coil as proximity switch _ _ _
with 2 coils as slot switch _ . _ . _ .

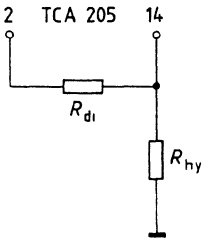


L_0, C_0	oscillator
R_{di}	distance adjustment
R_{hy}	hysteresis adjustment
C_I	integrating capacitor
C_D	delay capacitor

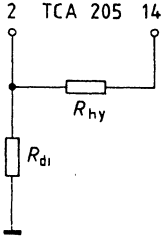
6

The resistance of distance and hysteresis R_{di} and R_{hy}, for proximity switch TCA 205 A; K may be applied as follows:

1. Series hysteresis



2. Parallel hysteresis

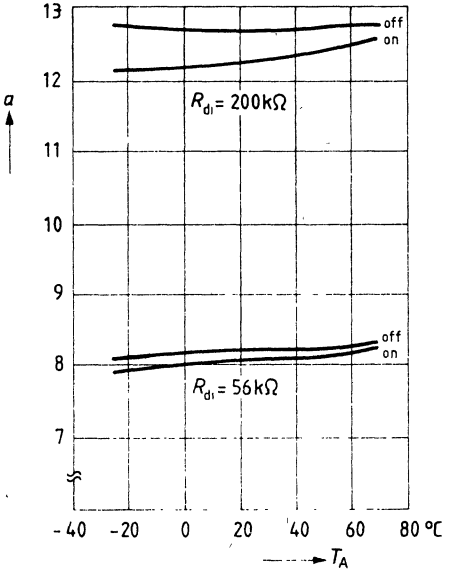


Circuit 1 is more suitable for proximity switches with oscillator frequencies of $f > 200$ kHz to 300 kHz, and small distances. Circuit 2 is more favorable for AF proximity switches having larger distances. This is due to the lower R_{hy} values enabled by circuit 1 (min. 0 Ω) compared with circuit 2 (min. 6 kΩ). Starting at frequencies of 200 kHz, high R_{hy} values effect in addition to the hysteresis also the oscillator phase. Practical applications, however, require little phase response to receive a clear evaluation.

Application example for a proximity switch

Coil data	pot core B65939-A-X22 coil former B65940-A-M1 Ø = 25 mm x 8.9 mm L = 642 µH n = 100 CuLS 30 x 0.05	
Measuring plate	30 mm x 30 mm x 1 mm, Fe	
Circuitry	R_{di} = 56 to 200 kΩ, metal layer R_{hy} = ∞ C_0 = 1500 pF, STYROFLEX f = 162 kHz	circuit 2

Switching distance versus ambient temperature



TCA 305 A; G
TCA 355 B; G
Proximity Switch

The devices TCA 305 and TCA 355 contain all the functions necessary to design inductive proximity switches. By approaching a standard metal plate to the coil, the resonant circuit is damped and the outputs are switched.

Operation schematic: see TCA 205

The types TCA 305 and TCA 355 have been developed from the type TCA 205 and are outstanding for the following characteristics:

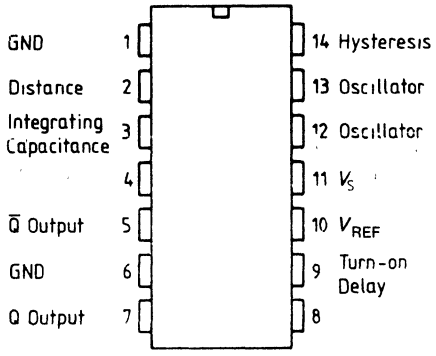
- Lower open-loop current consumption; $I_S < 1$ mA
- Lower output saturation voltage
- The temperature dependency of the switching distance is lower and the compensation of the resonant circuit TC (temperature coefficient) is more easily possible.
- The sensitivity is greater, so that larger switching distances are possible and coils of inferior quality can be used.
- The switching hysteresis remains constant as regards temperature, supply voltage and switching distance.
- The TCA 305 even functions without external integrating capacitance. With an external capacitance (or with RC combination) good noise suppression can be achieved.
- The outputs are temporarily short-circuit proof (approx. 10 s to 1 min depending on the package)
- The outputs are disabled when $V_S <$ approx. 4.5 V and they are enabled when the oscillator is working steadily (from $V_{S\,min} = 5$ V)
- Higher switching frequencies can be obtained.
- Miniature packages

Logic functions

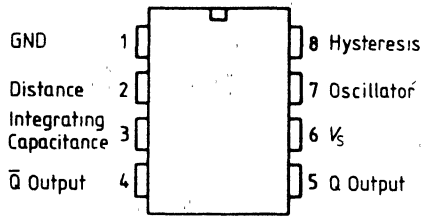
Oscillator	Outputs	
	Q	$\overline{Q}$
not damped	H	L
damped	L	H

Pin configuration

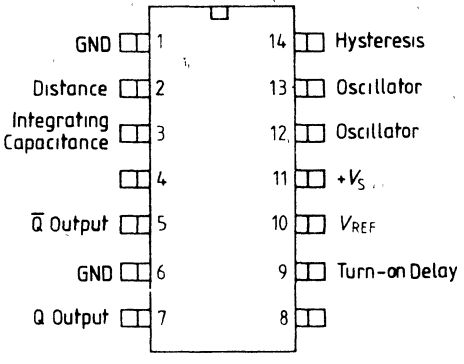
TCA 305 A



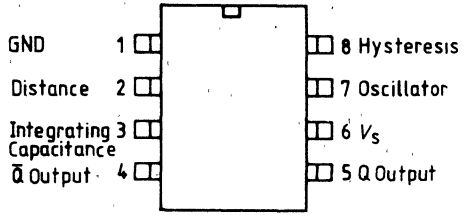
TCA 355 B



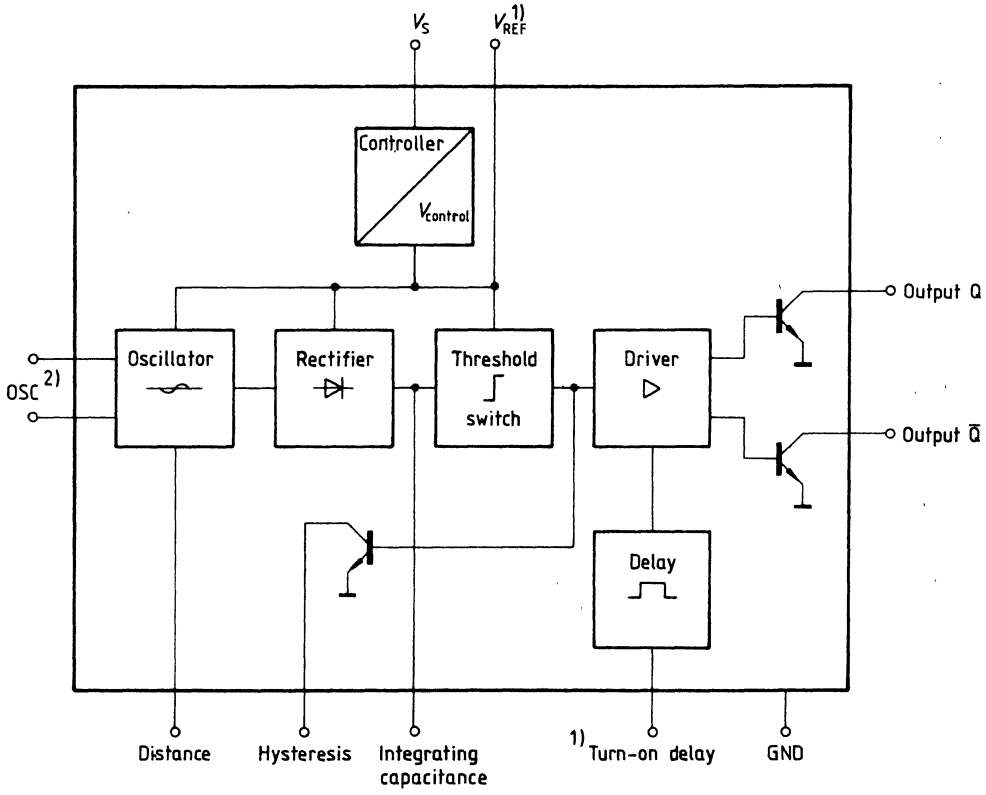
TCA 305 G



TCA 355 G



Block diagram



1) TCA 305 only
2) Connected internally in case of TCA 355

Maximum ratings

Supply voltage		V_S	35	V
Output voltage		V_Q	35	V
Output current		I_Q	50	mA
Distance, hysteresis resistance		R_{di}, R_{hy}	0	Ω
Capacitances		C_I, C_d	5	µF
Junction temperature		T_j	125	°C
Storage temperature range		T_{stg}	−55 to 125	°C
Thermal resistance (system-air)	TCA 305 A	$R_{th\,SA}$	85	K/W
	TCA 305 G	$R_{th\,SA}$	140	K/W

Operating range

Supply voltage	V_S	5 to 30	V
Oscillator frequency	f_{OSC}	0.015 to 1.5	MHz
Ambient temperature	T_A	−25 to 85	°C

Characteristics

$V_S = 12$ V, $T_A = -25$ °C to 85 °C

		Test conditions	Lower limit B	typ	Upper limit A	
Open-loop current consumption	I_S	outputs open		0.6	1.0	mA
Reference voltage	V_{ref}	$I_{ref} < 10$ µA		3.2		V
L output voltage	V_{QL}	$I_{QL} = 5$ mA		0.04	0.15	V
per output	V_{QL}	$I_{QL} = 25$ mA		0.10	0.35	V
	V_{QL}	$I_{QL} = 50$ mA		0.22	0.75	V
H output current per output	I_{QH}	$V_{QH} = 30$ V			10	µA
Threshold at 3	V_{S3}			2.1		V
Hysteresis at 3	V_{hy}		0.4	0.5	0.6	V
Turn-on delay	$t_{d\,on}$	$T_A = 25$ °C	−25%	600	−25%	ms/µF
Switching frequency w/o C_I	f_s				5	kHz

Maximum ratings

Supply voltage		V_S	35	V
Output voltage		V_Q	35	V
Output current		I_Q	50	mA
Distance, hysteresis resistance		R_{dI}, R_{hy}	0	Ω
Junction temperature		T_j	125	°C
Storage temperature range		T_{stg}	−55 to 125	°C
Thermal resistance (system-air)	TCA 355 B	$R_{th\,SA}$	135	K/W
	TCA 355 G	$R_{th\,SA}$	200	K/W

Operating range

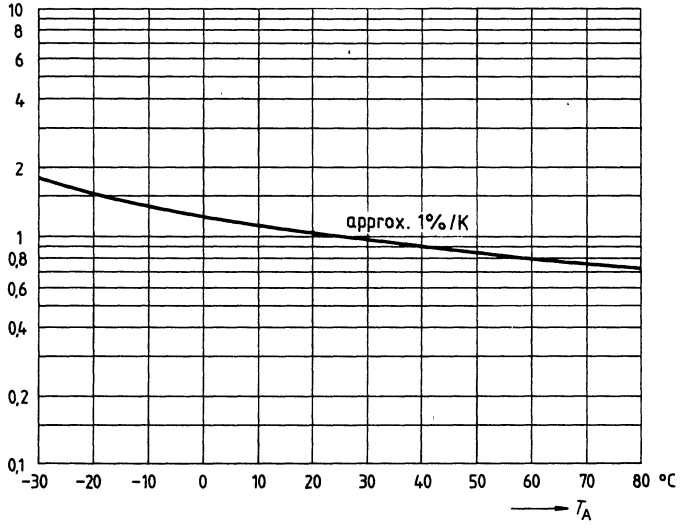
Supply voltage	V_S	5 to 30	V
Oscillator frequency	f_{OSC}	0.015 to 1.5	MHz
Ambient temperature	T_A	−25 to 85	°C

Characteristics

$V_S = 12$ V; $T_A = -25$ to 85 °C

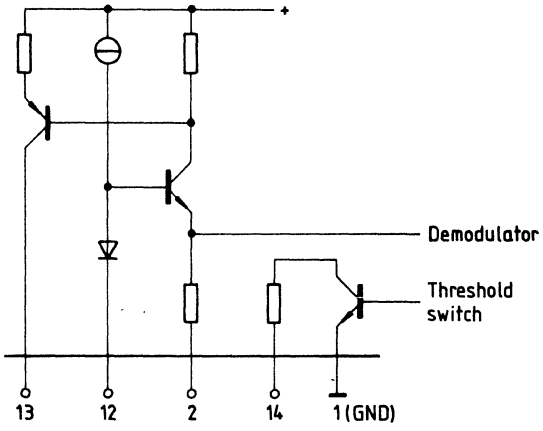
		Test conditions	Lower limit B	typ	Upper limit A	
Open-loop current consumption	I_S	outputs open		0.6	1.0	mA
L output voltage	V_{QL}	$I_{QL} = 5$ mA		0.04	0.15	V
per output	V_{QL}	$I_{QL} = 25$ mA		0.10	0.35	V
	V_{QL}	$I_{QL} = 50$ mA		0.22	0.75	V
H output reverse current per output	I_{QH}	$V_{QH} = 30$ V			10	µA
Threshold at 3	V_{S3}			2.1		V
Hysteresis at 3	V_{hy}		0.4	0.5	0.6	V
Switching frequency w/o C_I	f_s				5	kHz

Standard turn-on delay referred to $T_A = 25$ °C

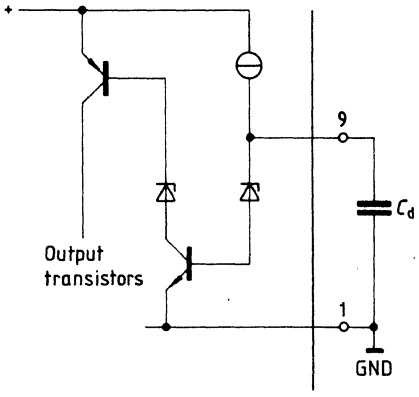


Schematic circuit diagrams

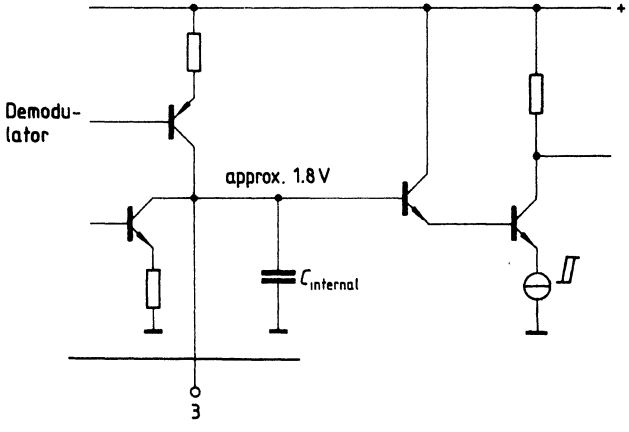
Oscillator



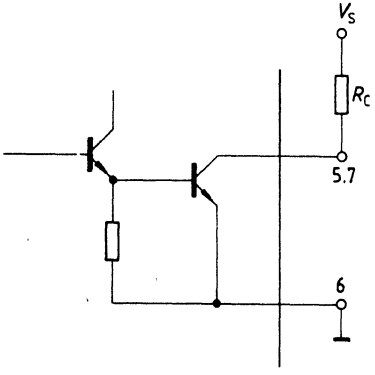
Turn-on delay for TCA 305



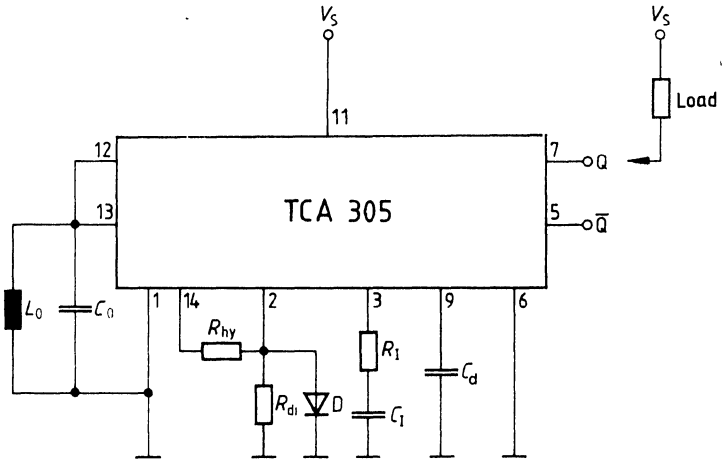
Integrating capacitor

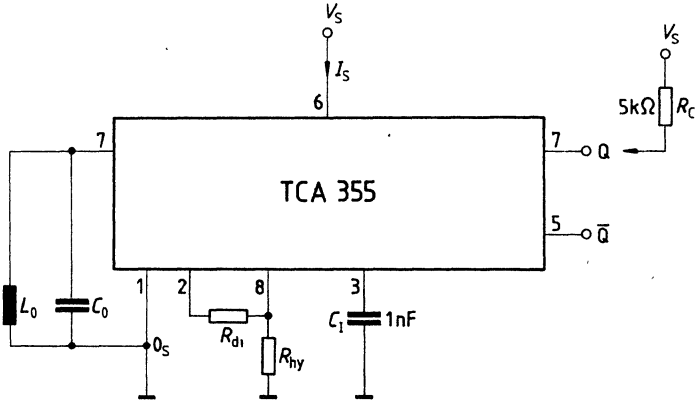


Outputs



Application circuits





L_0, C_0	Resonant circuit
R_{hy}	Hysteresis adjustment
R_{di}	Distance adjustment
D	Temperature compensation of the resonant circuit; possibly with series resistance for the purpose of adjustment. The diode is not absolutely necessary. Whether it is used or not depends on the temperature coefficient of the resonant circuit.
R_I; C_I	Integration element
C_d	Delay capacitor

Dimensioning examples in accordance with CENELEC Standard (flush)

	M 12	M 18	M 30
Ferrite pot core	M33 (7.35x3.6) mm	N22 (14.4x7.5) mm	N22 (25x8.9) mm
Number of turns	100	80	100
Cross section of wire	0.1 CuL	20x0.05	10x0.1
L_0	206 µH	268 µH	585 µH
C_0 (STYROFLEX®)	1000 pF	1.2 nF	3.3 nF
f_{OSC}	appr. 350 kHz	appr. 280 kHz	appr. 115 kHz
Sn	4 mm	8 mm	15 mm
R_A (Metal)	8.2 kΩ + 330 Ω	33 kΩ	22 kΩ + 2.7 kΩ
C_d	100 nF	100 nF	100 nF

Note:

At pin 3 (integrating capacitance) we recommend a capacitor of typ. 1 nF. To increase noise immunity this capacitor can be substituted by an RC circuit with, e.g., $R_I = 1$ MΩ and $C_I = 10$ nF.

SIEMENS

TFA 1001 W
Photodiode with Amplifier

The bipolar IC TFA 1001 W contains a photodiode and an amplifier. At its output (open NPN collector), the TFA 1001 W supplies a current directly proportional to the illuminance. Another pin permits a linearized characteristic curve at low illuminances and can be used to inhibit the output.

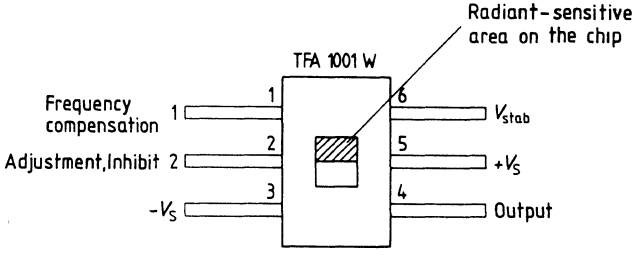
Application

- Exposure meters
- Exposure control systems
- Electronic flashes
- Optical follow-up control
- Smoke detectors
- Linear optocouplers
- Color identification

Features

- High sensitivity
- High output current linearity
- Good spectral sensitivity
- Low current consumption
- Wide modulation range
- Large operating voltage range

Pin configuration



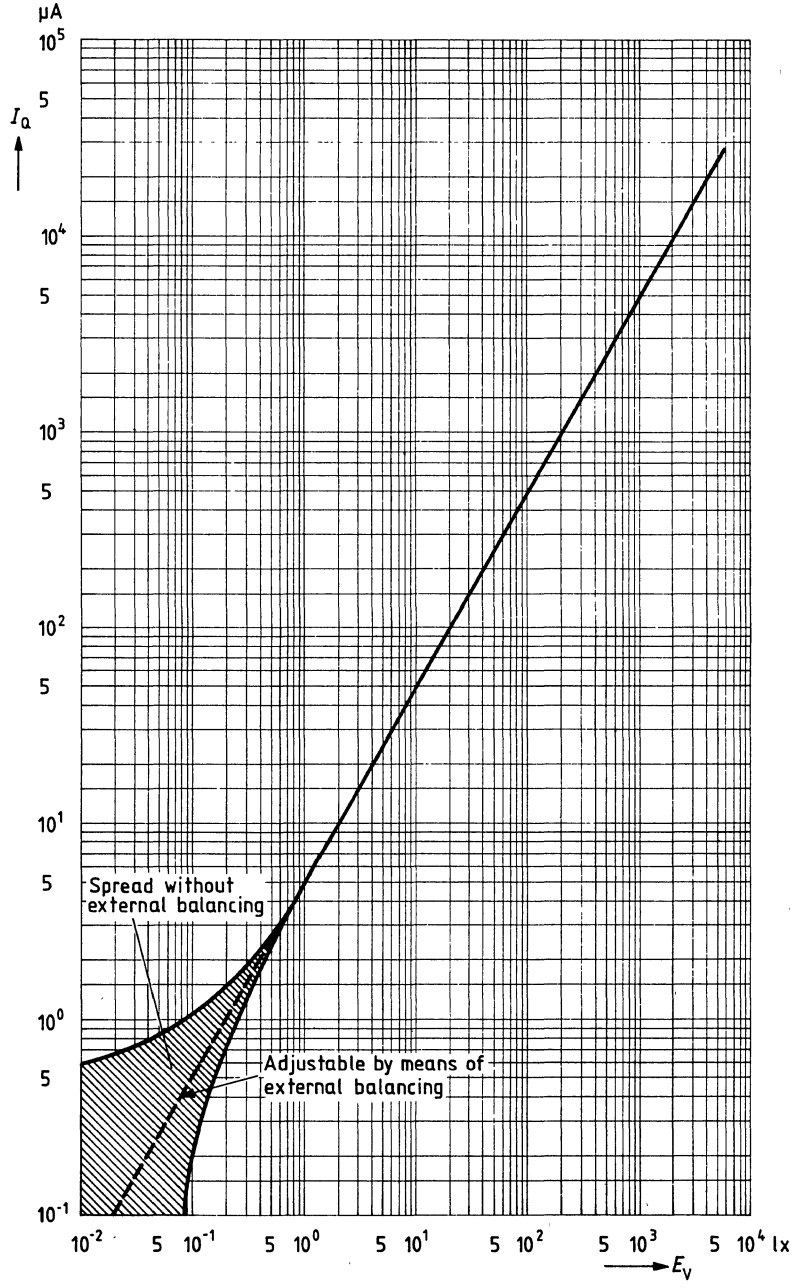
Maximum ratings

		Lower limit B	Upper limit A	
Supply voltage	V_S		15	V
Output current	I_Q		50	mA
Power dissipation	P_{tot}		200	mW
Junction temperature	T_j		100	°C
Storage temperature	T_{stg}	−40	85	°C
Thermal resistance (system-air)	$R_{th\,SA}$		250	K/W

Characteristics at $T_{amb} = 25$ °C, supply voltage applied to pin 5

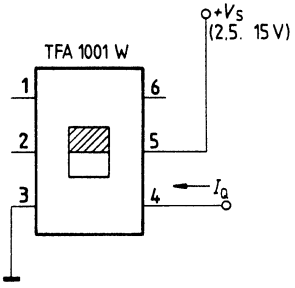
		Lower limit B	typ	Upper limit A	
Supply voltage	V_S	2.5		15	V
Current consumption at $E_v = 0$ lx	I_S	−10		1	mA
Ambient temperature (during operation)	T_{amb}			70	°C
Illuminance	E_v	0		5000	lx
Sensitivity in range $E_v = 1$ lx to 1000 lx	S	2.5	5	7.5	µA/lx
Output current at					
$E_v = 0.05$ lx	I_Q		0.25		µA
$E_v = 1$ lx	I_Q	2.5	5	7.5	µA
$E_v = 1000$ lx	I_Q	2.5	5	7.5	mA
$E_v = 5000$ lx	I_Q		25		mA
Stabilized voltage at pin 6	V_{stab}	1.2	1.35	1.5	V
Supply voltage dependence of stabilized voltage V_{stab}	$\Delta V_{stab}/\Delta V_S$		2		mV/V
Temperature dependence of stabilized voltage V_{stab}	$\Delta V_{stab}/\Delta T_{amb}$		−0.3		mV/°C

Photocurrent versus illuminance

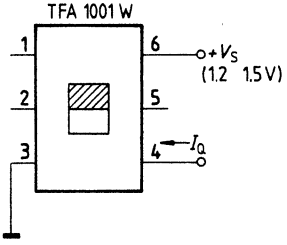


Possible applications of TFA 1001 W as light/current transducer

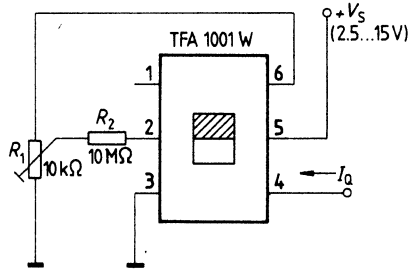
1) for operating voltage 2.5 to 15 V



2) for low operating voltage 1.2 to 1.5 V

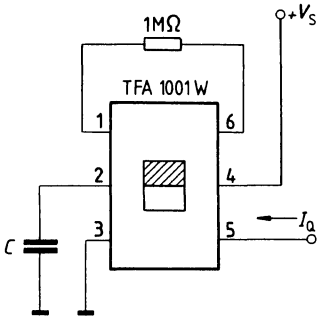


3) for especially low illuminance down to 0.01 lx

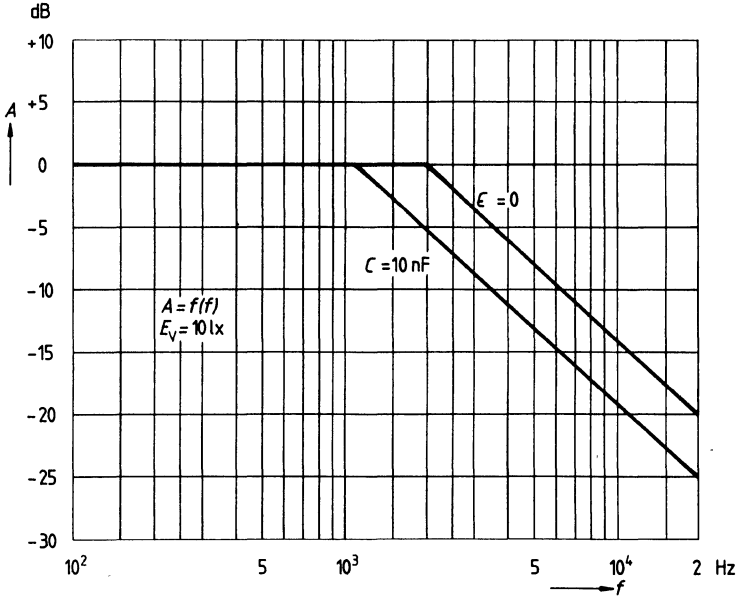


In case of low illuminance (see characteristic: output current versus illuminance), the output current can be balanced by means of the adjustment control R_1. The lower range of the output characteristic can be linearized even more by setting a dark current of about 5 nA.

Dynamic behavior

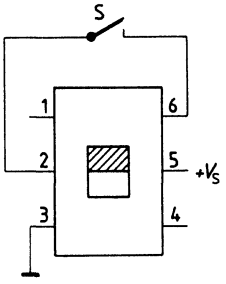


The dynamic behavior can be influenced at connection 2 by connecting capacitors.



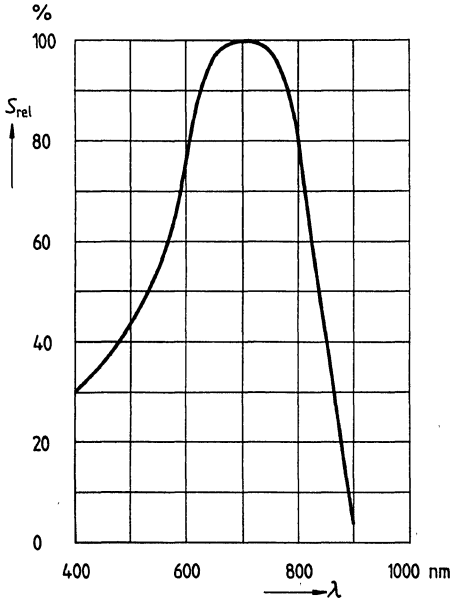
Attenuation $A = \frac{I_Q(f)}{I_Q(f=0)}$

Inhibiting the output

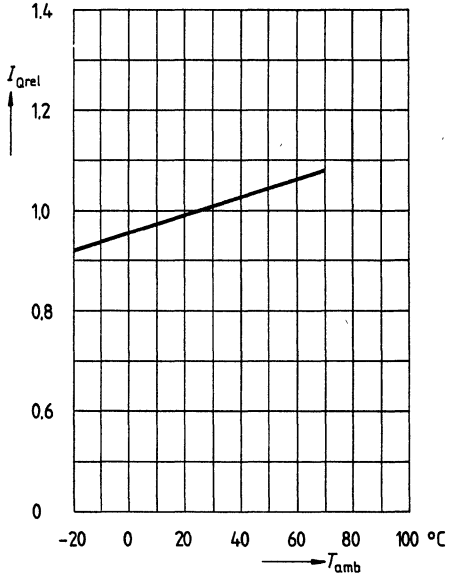


The output can be inhibited by connecting the balancing input with the stabilized voltage (switch, PNP transistor, FET).

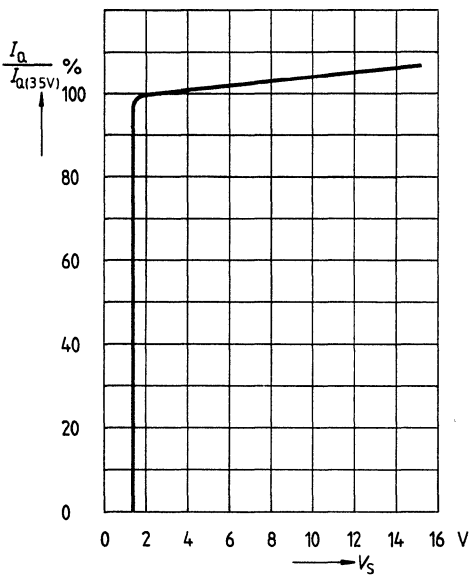
Relative spectral sensitivity versus wavelength



Relative output current versus ambient temperature
in range $E_v = 1$ lx to 1000 lx

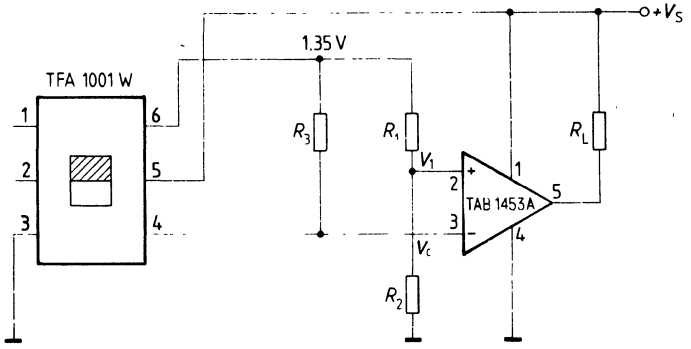


Output current versus supply voltage



Application examples

Simple threshold switch with TAB 1453 A op amp

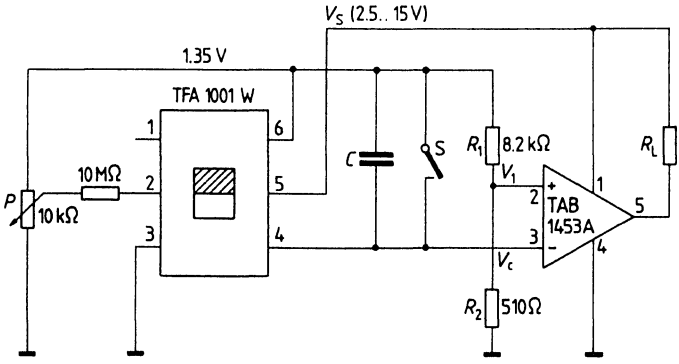


The illustration shows a simple threshold switch as can, for example, be used in cameras to change the aperture or indicate the illuminance. Operational amplifier TAB 1453 A serves as comparator. It has a PNP input and is able to operate at very low supply voltage.

The output is an open collector which can switch currents up to 70 mA.

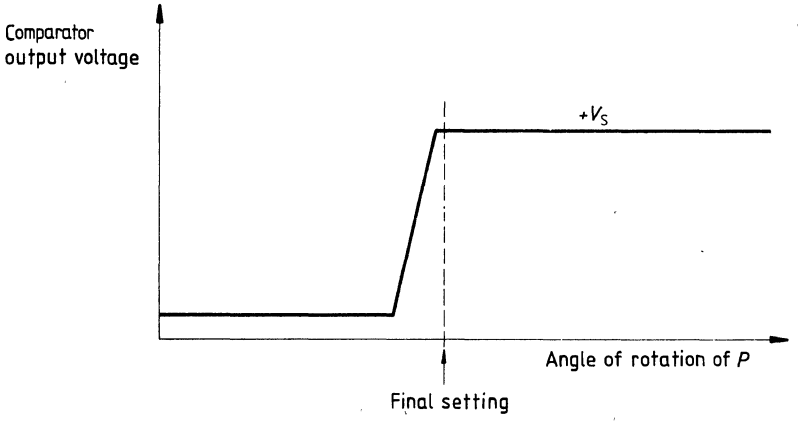
Since the stabilized voltage at pin 6 is used as reference voltage, the circuit is highly independent of the supply voltage.

Shutter speed or exposure control

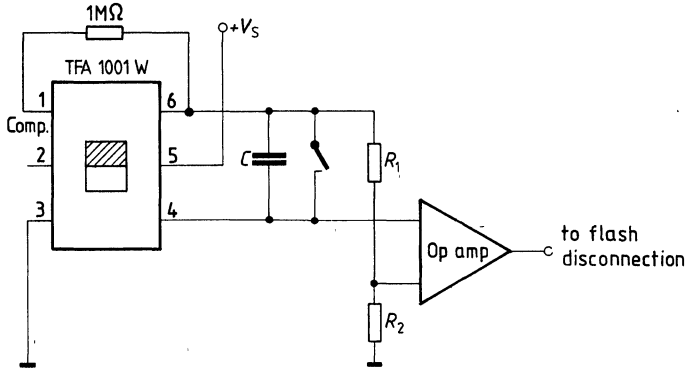


The illustration above shows a light/time control which can, e.g. be used to control the shutter speed in cameras or for exposure time control in enlargers. This circuit operates also largely independently of the supply voltage. A further essential advantage is, that for the major part of the exposure time the comparator input current is insignificant as the corresponding input transistor remains fully off-state. By means of potentiometer P, the operating range can be extended to lower illuminance values. Opening the switch starts the exposure, and capacitor C is charged from pin 4 of the photo IC. The comparator switches if the voltage V_C falls below the reference voltage determined by resistors R_1 and R_2. The relationship between illuminance and time is defined by capacitor C and precision adjustment is possible by means of V_1; V_1, however, must not become less than 0.4 V.

The dark current may be set in the circuit by means of potentiometer *P*. For this purpose, capacitor *C* is removed. *P* is then adjusted in darkness such that the output of the comparator is just blocked. Capacitor C is then inserted. (See illustration below).

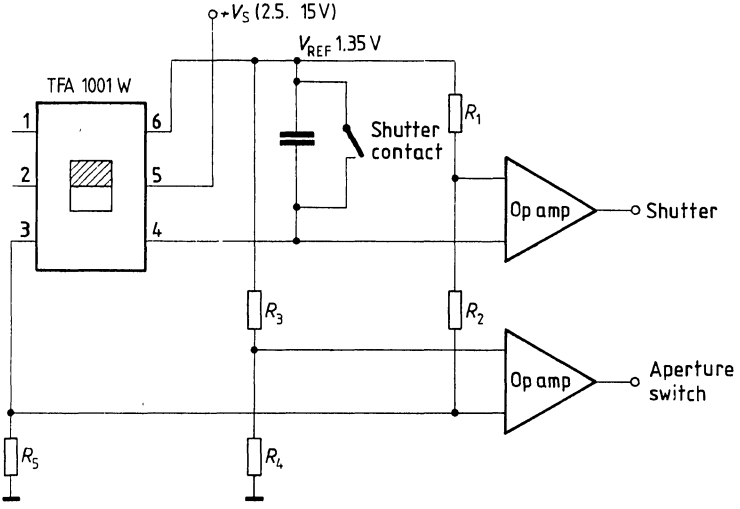


Schematic circuit diagram for an electronic flash control



TFA 1001 W can also be used for electronic flash control. It must, however, be ensured that the illuminance does not exceed 5 klx; use a grey filter if necessary. To be able to control very short times, it is useful to connect an additional capacitor to pin 1.

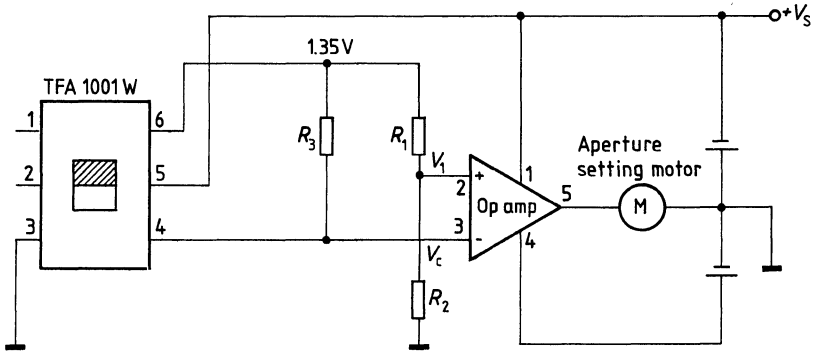
Combined aperture and exposure control



The aperture and exposure control may be combined, with the information for aperture switching being taken from the total current of the photo IC (voltage drop at R_5).

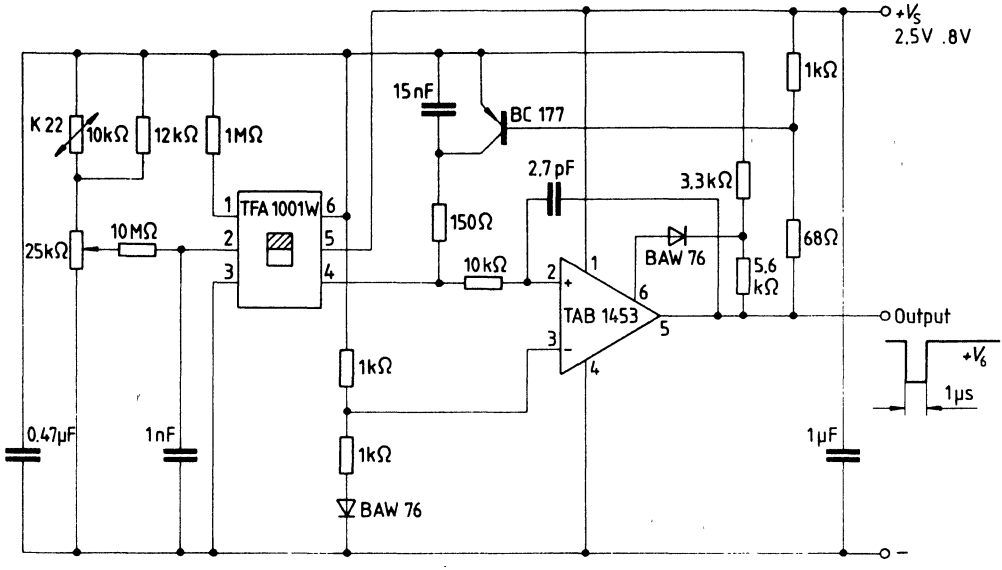
6

Aperture follow-up control for cine cameras



The op amp compares the voltage drop at R_3, generated by the photoelectric current, with a reference voltage derived from the stabilized voltage, and controls the aperture via motor M.

Light/frequency transducer



Sensitivity: approx. 600 Hz/lx
Range: 4 Hz to 400 000 Hz

- High resolution
- Fully temperature-compensated
- Wide operating voltage range
- High operating voltage suppression
- Wide dynamic range (5 decades)

Particularly suitable for digital processing.

SIEMENS

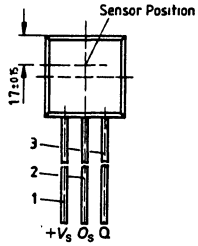
Preliminary

TLE 4901 F, TLE 4901 K
Integrated Hall-Effect Switch for Alternating Magnetic Fields

- Low Switching Thresholds with Good Long-Term Stability
- High Interference Immunity
- Overvoltage Protection
- Extended Temperature Range −40°C to +135°C
- Insensitive to Mechanical Stress
- Flat Plastic Package (1.5 mm) or Micropack

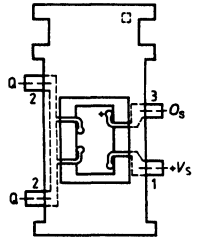
Pin Configurations

TLE 4901 F



0085-1

TLE 4901 K



0085-10

Dimensions in mm

Pin Definitions

TLE 4901 F

Pin	Symbol	Function
1	$+V_S$	Supply Voltage
2	O_S	Ground
3	Q	Output

TLE 4901 K

Pin	Symbol	Function
1	$+V_S$	Supply Voltage
2	Q	Output
3	O_S	Ground

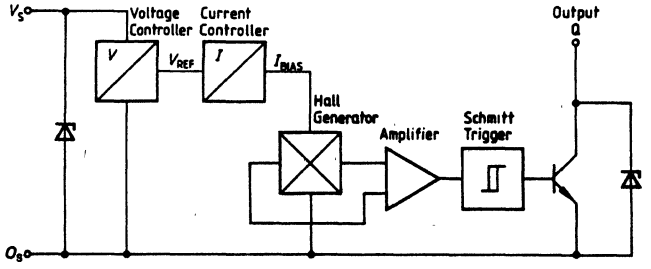
6

The Hall-effect IC TLE 4901 is a static contactless switch operated by an alternating magnetic field. The output is switched to the conducting state by the south pole of the magnetic field and blocked by its north pole.

The IC is provided with an integrated overvoltage protection against most of the transients occuring in automotive and industrial applications.

The IC is particularly intended as an rpm sensor or an angle indicator. Multiple pole ring magnets are especially suited to switching the !C.

Block Diagram



Circuit Description

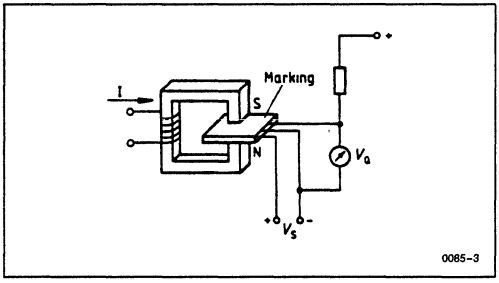
The circuit includes a Hall generator, amplifier and a Schmitt trigger. The supply and the output terminals have protection circuits with Z characteristics to prevent overvoltage.

A magnetic field perpendicular to the chip surface induces a voltage at the sensor contacts of the integrated Hall generator. This voltage is amplified, Schmitt triggered, and used to control an NPN transistor with a collector output. The output-stage transistor conducts when the applied flux density exceeds the switching level. If the flux density is reduced by the hysteresis flux density, the output stops conducting.

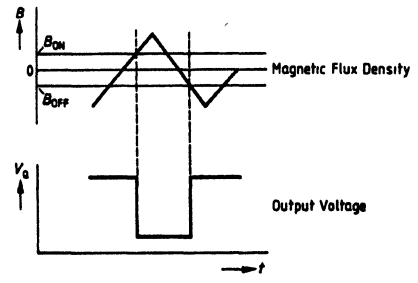
To minimize the effects of supply voltage and temperature variations on the switching level, the Hall sensor is supplied by a stabilized current source, which is in turn derived from a reference voltage.

Functional Description

When a magnetic field is applied in the direction shown, and the turn-on flux density is exceeded, the IC's output conducts. Reversal of the current direction in the electromagnet (i.e., reversal of the magnetic field) and falling below the turn-off flux density, leaves the output non-conducting.



Switching Characteristics



Absolute Maximum Ratings*

T_A = −40°C to +135°C

Supply Voltage (V_S) ..... −1.2V to 30V

Output Voltage
Output Off-State (V_Q) 30V

Output Current
Output On-State (I_Q) ..... 40 mA

Flux Density Range (B) ..... unlimited T

Junction Temperature
t < 70,000h (T_j) ..... 150°C

Storage Temperature
t < 70,000h (T_{stg}) ..... −55°C to +150°C

Thermal Resistance
System-Air ($R_{th\ SA}$) ..... 250 k/W(1)

Overvoltage Limits

Current through Protection Devices (I_Z) t < 2 ms .... −200 mA to +200 mA

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Operating Range

Supply Voltage (V_S) ..... 4.5V to 30V

Ambient Temperature (T_A) ..... −40°C to +135°C

Notes:
1. Thermal resistance of TLE 4901K depends on type of mounting.
2. An optimal reliability and lifetime of the IC are assured as long as the junction temperature does not exceed 125°C. Though operation of the IC at the given max. junction temperature of 150°C is possible, a continuous operation at this rating could nevertheless impair the reliability of the IC considerably.

Characteristics V_S = 6V to 16V; T_A = −30°C to +125°C

Parameter	Symbol	Measurement Circuit	Limits			Units
			Min	Typ	Max	
Supply Current $B \leq B_{OFF}$ $B \geq B_{ON}$	I_S	 2 2	 2 3		 8 13	 mA mA
Flux Density for "ON" T_A = 25°C	B_{ON}	2			10	mT
Flux Density for "OFF" T_A = 25°C	B_{OFF}	2		−10		mT
Flux Density for "ON" T_A = −25°C to +85°C	B_{ON}	2			12	mT
Flux Density for "OFF" T_A = −25°C to +85°C	B_{OFF}	2		−12		mT
Hysteresis T_A = −25°C to +85°C	B_H	2	3		14	mT
Flux Density for "ON"	B_{ON}	2			15	mT
Flux Density for "OFF"	B_{OFF}	2	−15			mT
Hysteresis	B_H	2	2		15	mT
Output Leakage Current $B \leq B_{OFF}$	I_{QH}	2			10	μA
Output Voltage I_{QL} = 16 mA, $B \geq B_{ON}$	V_{QL}	2			0.4	V
Transition Times of Output Fall Time Rise Time	 t_{HL} t_{LH}	 1 1	 	 0.3 0.5	 1 1	 μs μs

Note:
The listed characteristics are ensured over the operating range of the IC when using the supply voltage and ambient temperature stated. Typical characteristics specify mean values expected over the production spread.

6

Measurement Circuits

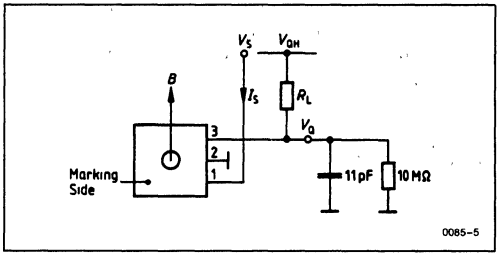


Figure 1

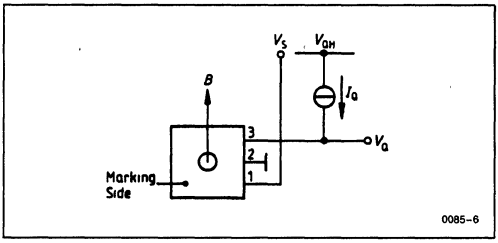
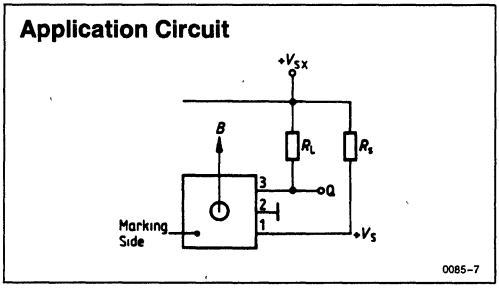


Figure 2

Application Circuit



For optimum protection against destruction, R_S is required to be as high as possible.

Dimensioning: $R_s = \frac{V_{SX\,min} - V_{S\,min}}{I_S\,max}$

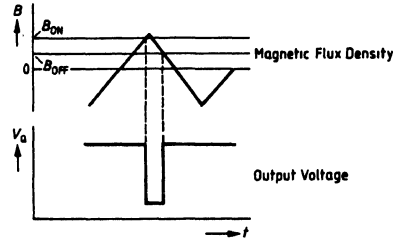
$V_{SX\,min}$ is the minimum supply voltage in each application.

Pulse Diagrams

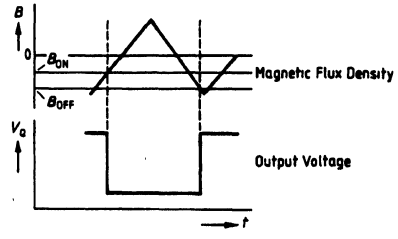
Flux Density	Q
$B > B_{ON}$	L
$B < B_{OFF}$	H

The characteristics include the following extreme cases:

$B_{ON} = B_{ON\,max}$



$B_{OFF} = B_{OFF\,min}$



Ordering Information

Type	Ordering Code	Package
TLE 4901 F	Q67000-A2518	Plastic Flatpack
TLE 4901 K	Q67000-A2399	MIKROPACK (SMD)

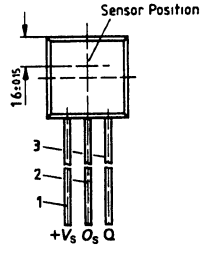
SIEMENS

Preliminary

TLE 4902 F
Integrated Hall-Effect Switch for Alternating Magnetic Fields

- Low Switching Threshold With Good Long-Term Stability
- Extended Temperature Range −40°C to +125°C
- Flat Plastic Package (1.5 mm)
- Suited To Low-Cost Applications, e.g. Electronic Commutation of Electric Motors
- Insensitive to Mechanical Stress

Pin Configuration



0086-1

Pin Definitions

Pin	Symbol	Function
1	$+V_S$	Supply Voltage
2	O_S	Ground
3	Q	Open Collector Output

6

The Hall-Effect IC TLE 4902 F is a static contactless switch operated by an alternating magnetic field. The output is switched to the conducting state by the south pole of a magnetic field and is blocked by its north pole.

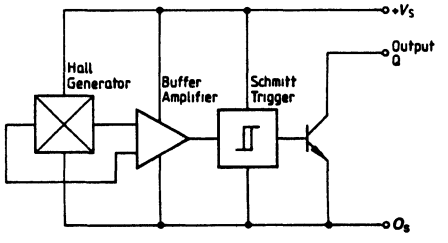
The IC is especially suited to applications as an rpm sensor or an angle indicator.

Circuit Description

The circuit includes a Hall generator, amplifier, a Schmitt trigger and an open collector output.

A magnetic field perpendicular to the chip surface induces a voltage at the sensor contacts of the integrated Hall generator. This voltage is amplified, Schmitt triggered, and used to control an NPN transistor with a collector output. The output-stage transistor conducts when the applied flux density exceeds the switching level. If the flux density is reduced by the hysteresis flux density, the output stops conducting.

Block Diagram

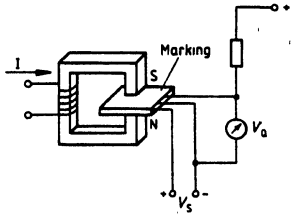


0086-2

Functional Description

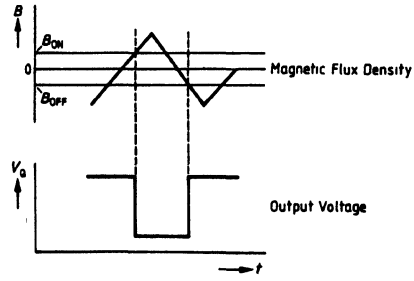
When a magnetic field is applied in the direction shown, and the turn-on flux density is exceeded, the IC's output conducts.

Reversal of the current direction in the electromagnet (i.e. reversal of the magnetic field) and falling below the turn-off flux density, leaves the output non-conducting.



0086-3

Switching Characteristics



0086-4

Absolute Maximum Ratings*

T_A = −40°C to +125°C

Supply Voltage (V_S) ..... −0.5V to +7V

Output Voltage (V_Q)
Output Off-State 30V

Output Current (I_Q)
Output On-State ..... 20 mA

Magnetic Flux Density Range (B) ..... Unlimited T

Junction Temperature (T_J)
t < 70,000h ..... 150°C

Storage Temperature (T_{stg})
t < 70,000h ..... −40°C to +150°C

Thermal Resistance ($R_{th\ SA}$)
System-Air ..... 240 k/W

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Operating Range

Supply Voltage (V_S) ..... 4.5V to 6.8V

Ambient Temperature (T_A) ..... −40°C to +125°C

Notes:
Maximum Ratings—Maximum ratings are absolute rated values; exceeding only one value may destroy the IC.
Operating Range—Within the functional range, the integrated circuit operates as described; deviations from the characteristic data are possible.

Characteristics

T_A = 0°C to 85°C; V_S = 4.5V to 5.5V (unless otherwise specified)

Parameter	Symbol	Measurement Circuit	Limits			Units
			Min	Typ	Max	
Flux Density for "ON" T_A = 25°C	B_{ON}	2			10	mT
Flux Density for "OFF" T_A = 25°C	B_{OFF}	2	10			mT
Flux Density for "ON"	B_{ON}	2			15	mT
Flux Density for "OFF"	B_{OFF}	2	−15			mT
Hysteresis	B_H	2	3		14	mT
Flux Density for "ON" T_A = −40°C to +125°C V_S = 4.5V to 6.8V	B_{ON}	2			20	mT
Flux Density for "OFF" T_A = −40°C to +125°C V_S = 4.5V to 6.8V	B_{OFF}	2	−20			mT
Hysteresis T_A = −40°C to +125°C V_S = 4.5V to 6.8V	B_H	2	2		15	mT
Output Current B ≤ B_{OFF}	I_{QH}	2			10	µA
Output Voltage I_{QL} = 16 mA; B ≥ B_{ON}	V_{QL}	2			0.4	V

Characteristics (Continued)

T_A = 0°C to 85°C; V_S = 4.5V to 5.5V (unless otherwise specified)

Parameter	Symbol	Measurement Circuit	Limits			Units
			Min	Typ	Max	
Transition Times of Output						
Fall Time	t_{HL}	1		0.3	1	µs
Rise Time	t_{LH}	1		0.5	1	µs
Supply Current						
$B \leq B_{OFF}$	I_S	2	2		5.5	mA
$B \geq B_{ON}$	I_S	2	3		6.5	mA

Note:
The listed characteristics are ensured over the operating range of the IC when using the supply voltage and ambient temperature stated. Typical characteristics specify mean values expected over the production spread.

Measurement Circuits

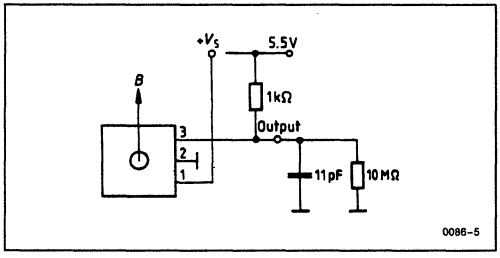


Figure 1

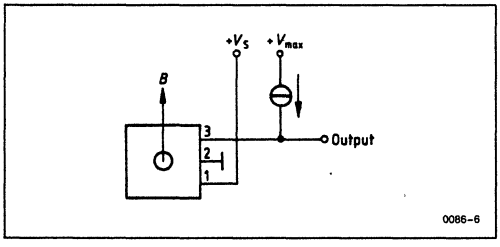
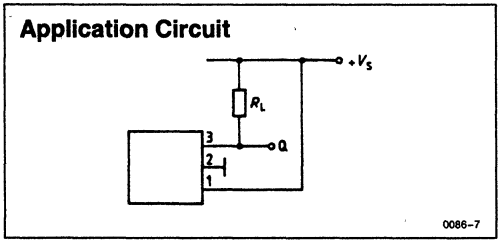


Figure 2

Application Circuit

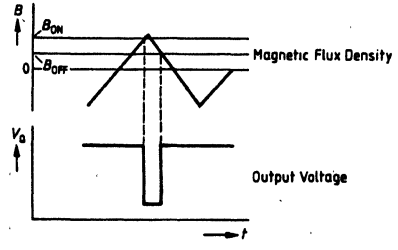


Pulse Diagrams

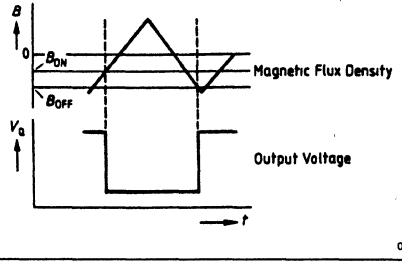
Flux Density	Q
$B > B_{ON}$	L
$B < B_{OFF}$	H

The characteristics include the following extreme cases:

$B_{ON} = B_{ON\ max}$



$B_{OFF} = B_{OFF\ min}$



Ordering Information

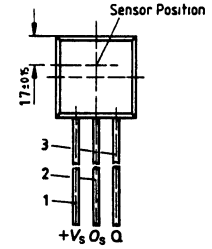
Type	Ordering Code	Package
TLE 4902 F	Q67000-A8048	Plastic Flatpack

SIEMENS

TLE 4903 F
Integrated Hall-Effect Switch for Unipolar Magnetic Fields

- Low Switching Thresholds with Good Long-Term Stability
- High Interference Immunity
- Overvoltage Protection
- Extended Temperature Range −40°C to +130°C
- Insensitive to Mechanical Stress
- Flat Plastic Package (1.5 mm)

Pin Configuration



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Dimensions in mm

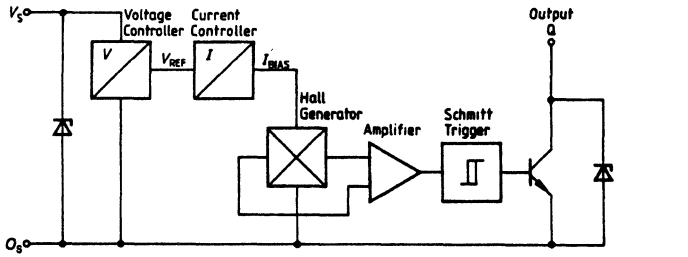
Pin Definitions

Pin	Symbol	Function
1	$+V_S$	Supply Voltage
2	O_S	Ground
3	Q	Open Collector Output

6

The integrated Hall IC TLE 4903 F is a contactless switch operated by a magnetic field. On reaching the turn-on flux density of the south-pole of a magnetic field, the output conducts. As the flux density strength sinks below the turn-off level, the output stops conducting. The IC is provided with an integrated overvoltage protection against most of the transients occurring in automotive and industrial applications.

Block Diagram



Circuit Description

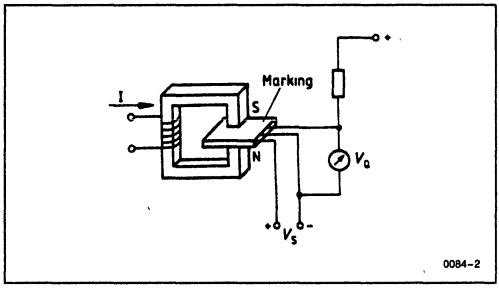
The circuit includes a Hall generator, amplifier, Schmitt trigger and an open collector output. The supply and the output terminals have protection circuits to prevent overvoltage.

A magnetic field perpendicular to the chip surface induces a voltage at the sensor contacts of the integrated Hall generator. This voltage is amplified, Schmitt triggered and used to control an NPN transistor with a collector output. The output-stage transistor conducts when the applied flux density exceeds the switching level. If the flux density is reduced by the hysteresis flux density, the output stops conducting.

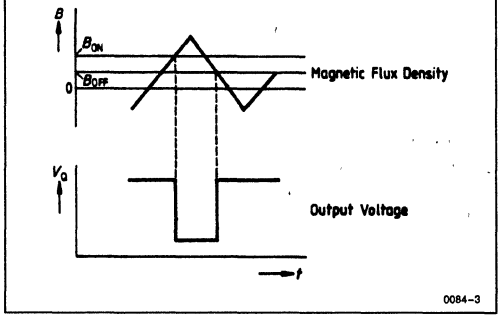
To minimize the effects of supply voltage and temperature variations on the switching level, the Hall sensor is supplied by a stabilized current source, which is in turn derived from a reference voltage.

Functional Description

When a magnetic field is applied in the direction shown, and the turn-on flux density is exceeded, the IC's output conducts. Reduction of the current and falling below the turn-off flux density, leaves the output non-conducting.



Switching Characteristics



Absolute Maximum Ratings*

T_A = −40°C to +130°C

Supply Voltage (V_S) ..... −1.2V to 30V
Output Current (I_Q) ..... 40 mA
Junction Temperature
t < 70,000h (T_j) ..... −40°C to +150°C
Storage Temperature (T_{stg}) ..... −55°C to +125°C
Thermal Resistance
System-Air ($R_{th\ SA}$) ..... 240 k/W
Flux Density Range (B) ..... −∞ to +∞
Output Voltage (V_Q) 30V

Overvoltage Limits

Current through Protection
Devices at Pins 1
and 3, t < 10 µs ..... −200 mA to +200 mA

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Operating Range

Supply Voltage (V_S) ..... 4.3V to 24V
Ambient Temperature (T_A) ..... −40°C to +130°C

Note:
An optimal reliability and lifetime of the IC are assured as long as the junction temperature does not exceed 125°C. Though operation of the IC at the given max. junction temperature of 150°C is possible, a continuous operation at this rating could nevertheless impair the reliability of the IC considerably.

Characteristics V_S = 14V; T_A = 25°C

Parameter	Symbol	Conditions	Test Circuit	Limits			Units
				Min	Typ	Max	
Magnetic Parameters*							
Flux Density "ON"	B_{ON}	T_A = 25°C		20		50	mT**
		T_A = 0°C to +70°C		18		52	mT
		T_A = −30°C to +100°C		18		57	mT
		T_A = −30°C to +125°C	2	12		58	mT
Flux Density "OFF"	B_{OFF}	T_A = 25°C		15		35	mT
		T_A = 0°C to +70°C		19		34	mT
		T_A = −30°C to +100°C		8		42	mT
		T_A = −30°C to +125°C	2	7		43	mT
Hysteresis ($B_{ON} - B_{OFF}$)	B_H		2	5		15	mT
Output Junction Current	I_{QO}	B < B_{OFF}; V_{OH} = 24V T_A = 25°C				10	µA
Supply Current	I_S	B < B_{ON}	1			13	mA
		B > B_{OFF}	1			14	mA
Output Voltage	V_Q	I_Q = 30 mA	2			0.4	V
Rise Time	t_{LH}	I_Q = 10 mA				1	µs
Fall Time	t_{HL}	I_Q = 10 mA				1	µs
Overvoltage Limit							
Supply Voltage	V_{SZ}	I_S = 16 mA		32		42	V
Output	V_{QZ}	I_{QZ} = 16 mA		32		42	V

Notes:
*The magnetic parameters are specified for a homogenous magnetic field at the sensor center as per Figure 3.
**1 mT = 10G
The listed characteristics are ensured over the operating range of the IC when using the supply voltage and ambient temperature stated. Typical characteristics specify mean values expected over the production spread.

Measurement Circuits

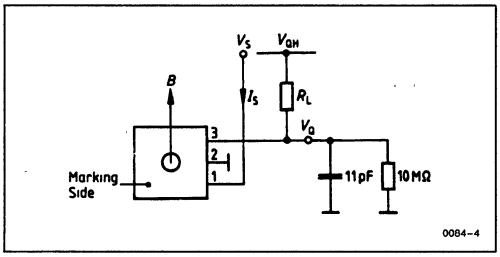


Figure 1

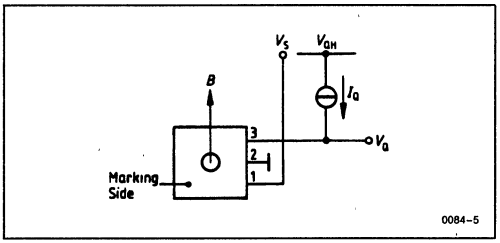
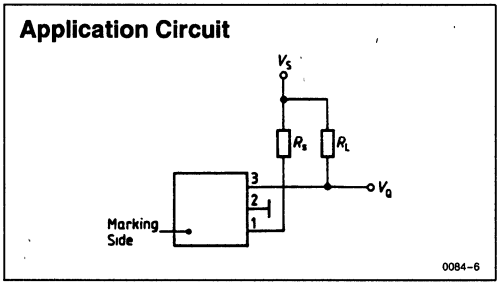
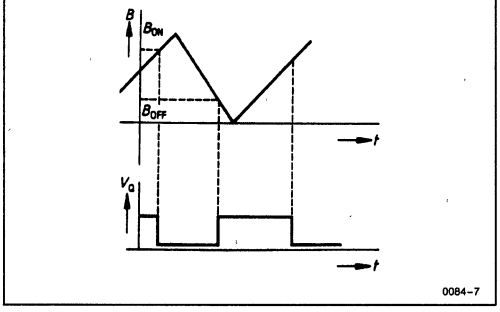


Figure 2

Application Circuit



Pulse Diagram



For optimum protection against destruction, R_S is required to be as high as possible.

Dimensioning: $R_S = \frac{V_{SX\,min} - V_{S\,min}}{I_S\,max}$

$V_{SX\,min}$ is the minimum supply voltage in each application.

Ordering Information

Type	Ordering Code	Package
TLE 4903 F	Q67000-A8047	Plastic Flatpack

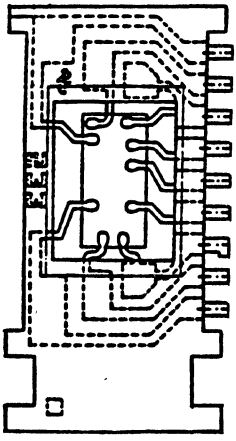
SIEMENS

Preliminary

TLE 4910 K
Bipolar Hall-Effect IC with Analog Output

Pin Configurations

(Top View)



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Pin Definitions

Pin	Function
1	V_S
2	V_{ref}
3	Ground
4	Zero Adj., $+V_{adj}$
5	Zero Adj., $-V_{adj}$
6	Sensitivity adj.
7	V_{probe}
8	V_{temp}
9	V_O

6

The IC TLE 4910 K generates an output voltage proportional to the magnetic flux density.

The IC is made northpole or southpole active by adjusting the zero point. The zero point of the transfer characteristics and the sensitivity of the device is adjusted with external components (Figure 4). The IC is suited as sensor for professional applications requiring enhanced temperature and improved data ranges e.g., measurement of pressure, acceleration, distance and torsion.

Absolute Maximum Ratings*

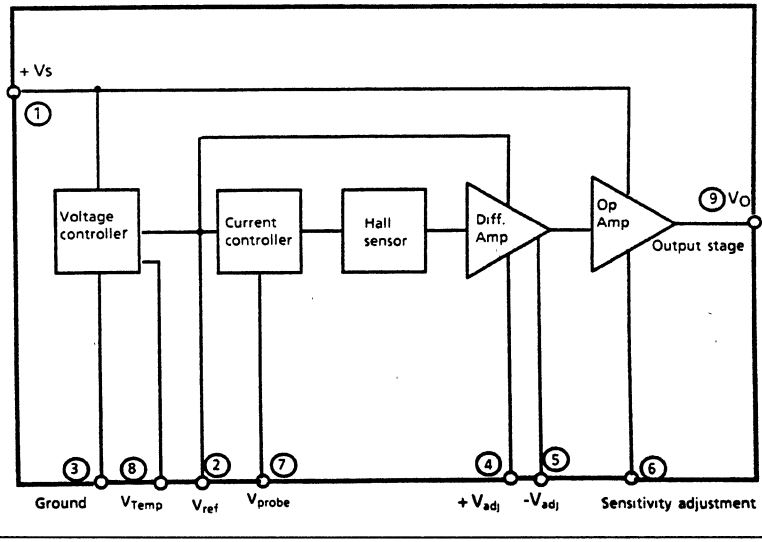
Maximum Ratings are absolute limits. The integrated circuit may be destroyed if only a single value is exceeded.

Parameter	Symbol	Limits			Units
		Min	Typ	Max	
Ambient Temperature	T_A	−40		+150	°C
Supply Voltage	V_S		30		V
Output Current	I_O		10		mA
Junction Temperature	T_J		+125		°C
Storage Temperature	T_S	−40		+125	°C
Thermal Resistance (Junction-Air)	R_{thJA}	Mounting Dependent			
Induction	B	−∞		+∞	
Zero Adjustment Current	I_{adj}	−1		+1	mA

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Reliability and lifetime of the IC is assured as long as the junction temperature does not exceed 125°C, though operation of the IC at the given maximum junction temperature of 150°C is possible. Nevertheless, a continuous operation at this rating could impair the reliability of the IC considerably.

Block Diagram



Functional Description

The IC TLE 4910 K can be operated at supply voltages between 4.75V to 18V. It's output signal is a voltage with reference to ground which can supply up to 5 mA.

As shown in the block diagram the Hallsensor is fed with regulated current from an internal current controller. The output signal of the Hallsensor is first amplified in a differential amplifier to a sufficiently high level and then converted into a grounded signal.

The endstage comprises of an operational amplifier with internal feedback whose inverting input is led out and can be used for tuning the sensitivity of the device.

Functional Range

The functions stated in the circuit description are fulfilled within the range of the operating data.

Parameter	Symbol	Conditions	Limits		Units
			Min	Max	
Supply Voltage	V_S		4.75	18	V
Output Current	I_O			5	mA
Ambient Temperature	T_A		−40	135	°C

Electrical Characteristics

The electrical characteristics include the guaranteed tolerances of the values maintained by an IC for the specified operating range.

V_S = 4.75V to 15V; T_A = −25°C to +125°C unless otherwise specified.

Parameter	Symbol	Conditions	Figure	Limits			Units
				Min	Typ	Max	
Supply Current	I_S	B < −20 mT	1			10	mA
Output Voltage Range	V_O	R_L = 10k V_S = 5V	1	0.05		V_S − 2	V
Sensitivity	S		1		30		mV/mT
Magnetic Offset	B_O		1	−20		+20	mT
Linearity Error	L	B = 0 mT to 100 mT			1	2	%
Temperature Coefficient of the Magnetic Offset	$\propto B_O$		1		±0.03		mT/k
Temperature Coefficient of the Sensitivity	$\propto S$				±0.5		%/k
Reference Voltage	V_{ref}	T_A = 25°C	1	2.9	30	3.1	V
Output Voltage/Adjustment Current (Pin 4)	V_O/I_{adj}	T_A = 25°C	2		+0.3		V/µA
Output Voltage/Adjustment Current (Pin 5)	V_O/I_{adj}	T_A = 25°C	2		−0.3		V/µA
Voltage at Pin 4 and Pin 5	V_{adj}	T_A = 25°C	2	30	70	110	mV
Temperature Voltage	V_{temp}	V_S = 5V, R = 5.1L T_A = 25°C	3	1.4		1.7	V
Temperature Coefficient of the V_{temp}	$\propto V_{temp}$	V_S = R = 5.1k	3	+3.5		4.5	mV/k
Output Impedance	R_O	V_S = 5V I_O < 5 mA				10	Ω
Sensitivity Change Due to V_S Changes	$\Delta S/\Delta V_S$	T_A = 25°C	1			0.2	%/V
Magnetic Offset Change Due to V_S Changes	$\Delta B_O/\Delta V_S$	T_A = 25°C	1			20	µT/V

6

Test Circuits

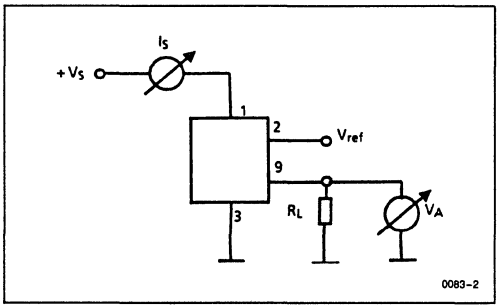


Figure 1

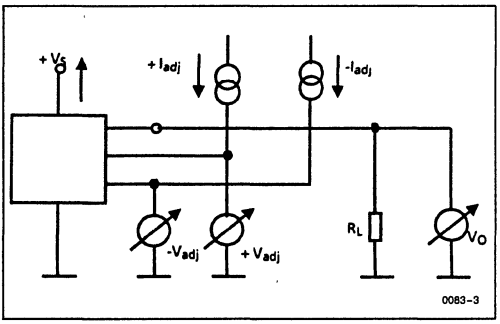


Figure 2

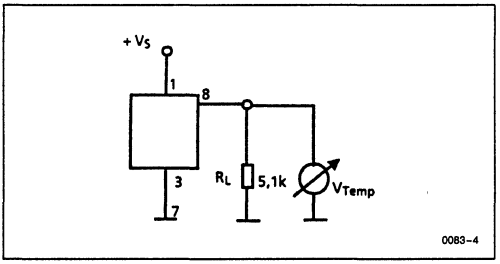


Figure 3

Application Circuits

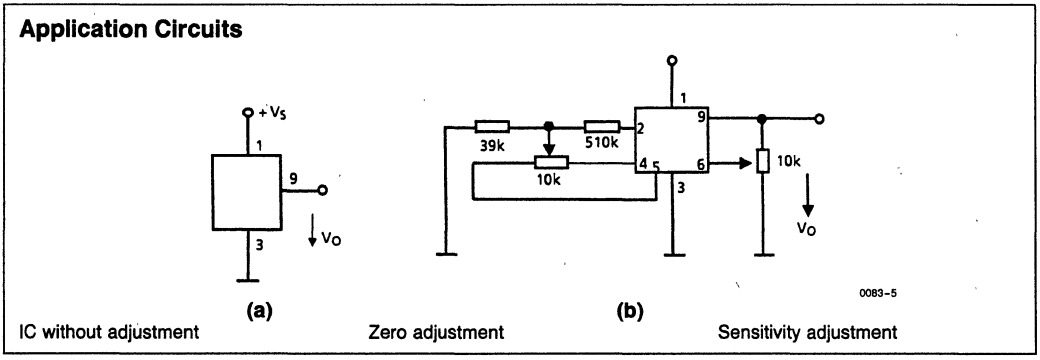


Figure 4

Functional Diagram

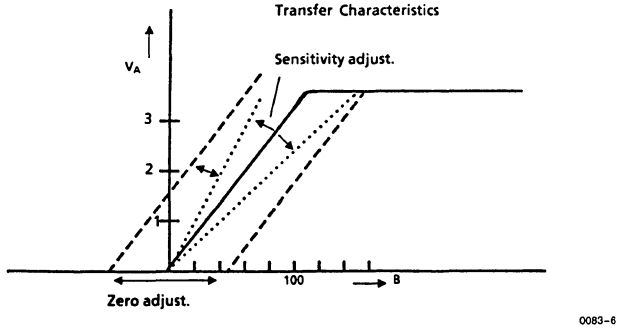


Figure 5

Ordering Information

Type	Ordering Code	Package
TLE 4910 K	Q67000-A 2398	Micropack

6

ICs for Video Applications

7

SIEMENS

SDA 2112-2
TV PLL for 125 kHz Resolution

The SDA 2112-2 is fabricated in ASBC technology. In connection with a VCO (tuner) and a high-speed 1:64 divider, it forms a digitally programmable phase-locked loop for TV sets designed to use the PLL frequency sythesis tuning principle. The PLL enables crystal-controlled setting of the tuner oscillator frequency for a 125 kHz resolution in the frequency bands I/III, IV, and V.

A serial interface provides for simple connection to a microprocessor. The latter loads the programmable divider and the band-selection outputs with the appropriate information.

Features

- No external integrator necessary
- Internal buffer
- Microprocessor compatible

Maximum ratings

Supply voltage pin 18	V_{S1}	−0.3 to 7.5	V
Inputs			
Q 1, Q 2, F, $\overline{F}$ pin 1, 2, 15, 16	V_I	−0.3 to V_{S1} + 0.2	V
CPL, IFO, PLE pin 7, 8, 10	V_I	−0.3 to 5.5	V
Outputs			
UHF, VHF, Bd I/III pin 3, 4, 5	V_Q	−0.3 to 16	V
CLK (pin 6)	V_6	−0.3 to 16	V
	I_6	3	mA
$\overline{LDM}$ (pin 17)	V_{17}	−0.3 to 7.5	V
	I_{17}	3	mA
LOCK IND (pin 12)	V_{12}	−0.3 to V_{S1} + 0.2	V
PD (pin 14)	I_{14}	1	mA
V_D (pin 11)	V_{11}	−0.3 to 33	V
OSC (pin 13)	V_{13}	−0.3 to V_{S1} + 0.2	V
	I_{13}	8	mA
Junction temperature	T_j	140	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\,SA}$	80	K/W

Operating range

Supply voltage range	V_{S1}	4.5 to 7.15	V
Input frequency	$f_{F,\overline{F}}$	16	MHz
Divider factor	N	256 to 8191	
Crystal frequency	f_Q	3	MHz
Tuning voltage	V_D	0.3 to 33	V
Ambient temperature	T_A	0 to 70	°C

Characteristics

$V_{S1} = 5$ V; $T_A = 25$ °C

		Test circuit	min	typ	max	
Supply current, pin 18	I_{S1}			20	35	mA
Oscillator output, pin 13	V_{13H}	4	4.5			V
$R_{L2} = 3.5$ kΩ						
OSC	V_{13L}	4			0.7	V
$R_{L2} = 3.5$ kΩ						
Signal inputs F/$\bar{F}$, pin 15, 16						
Input voltage	V_{15H}	1	4.1		$V_{S1}+0.2$	V
	V_{15L}	1	3.8		$V_{S1}-0.1$	V
Input current	I_{15}	1			50	µA
$V_{15} = 5$ V						
Input sensitivity (peak-to-peak)	$V_{15,16}$	1	300		1200	mV
Sine push-pull $f = 16$ MHz						
Bus inputs CPL, IFO, PLE, pin 7, 8, 10						
Upper threshold voltage	V_{7u}	2	1.0	1.3	1.6	V
Lower threshold voltage	V_{7l}	2	0.5	0.7	1.0	V
Hysteresis	ΔV_7	2		0.6		V
H input current	I_{7H}	2			8	µA
$V_{7H} = 5$ V						
L input current	I_{7L}	2	−50			µA
$V_{7L} = 0.4$ V						
Band selection outputs UHF, VHF, Bd I/III pins 3, 4, 5						
Reverse current	I_{3H}	3			10	µA
$V_{3H} = 15$ V						
Forward current (current drain)	I_{3L}	3	0.8		1.7	mA
$2\text{V} \leq V_3 \leq 15$ V						
Clock output CLK, pin 6						
H output voltage	V_{6H}	4	14			V
$V_{S3} = 15$ V						
L output voltage	V_{6L}	4			1.5	V
$R_{L1} = 6.8$ kΩ						
Tuning section V_D, PD, pins 11, 14						
Tuning voltage	V_{11}	5	0.3		32.5	V
$V_{S2} = 33$ V						
Charge-pump current	I_{14}	5	−150	±100	150	µA
PLL locked						
PLL unlocked	I_{14}	5	−450	±300	450	µA

7

Characteristics (cont'd)
$V_{S1} = 15$ V; $T_A = 25$ °C

		Test circuit	min	typ	max	
Lock indication, pin 12						
H output voltage	$V_{12\,H}$	5	2.8			V
L output voltage	$V_{12\,L}$	5			0.4	V
Carry synchronous divider $\overline{\text{LDM}}$ Pin 17 (open collector)						
Reverse current $V_{17\,H} = 5$ V	I_{17}	1			10	µA
L output voltage $R_L = 5$ kΩ	$V_{17\,L}$				0.4	V
Switching times						
IFO, PLE						
Set-up time	t_S	2	2	1.5		µs
Hold time	t_H	2	2	1.5		µs
CLK						
H pulse width	t_{TH}	4		8.0		µs
L pulse width	t_{TL}	4		8.0		µs
HL transition time $R_{L1} = 6.8$ kΩ	t_{THL}	4	0		0.5	µs
LH transition time $C_{L1} = 50$ pF	t_{TLH}		0		1.5	µs
CPL						
H pulse width	t_{CH}	2	2	1.5		µs
L pulse width	t_{CLH}	2	2	1.5		µs
OSC						
H pulse width	t_{OH}	4	133			ns
L pulse width	t_{OL}	4			200	ns
HL transition time $R_{L2} = 3.5$ kΩ	t_{OHL}	4			20	ns
LH transition time $C_{L2} = 8$ pF	t_{OLH}	4			50	ns

Circuit description (refer to block diagram)

F, $\overline{F}$ A switchable 16/17 counter is triggered by the ECL signal inputs F/$\overline{F}$. The counter, in connection with a 4-bit and a 9-bit programmable, synchronous counter, forms a programmable, 13-bit synchronous divider using the dual-modulus technique, the 4-bit counter controlling the switchover from 16 to 17. Divider ratios of $N = 256$ to 8191 are possible. For test purposes the carry of the synchronous

$\overline{LDM}$ divider is available at the $\overline{LDM}$ output (open collector).

The 16-bit shift register and latch is subdivided into 13 bits for storing the divider

IFO ratio N and 3 bits for controlling the three band-selection outputs.

CPL The telegram is shifted in via the serial data input IFO with the HL edge of the

PLE shift clock CPL when the enable input PLE is also on high level. First the complement of the divider ratio N, beginning with the LSB, is inserted in binary code, followed by the three control bits for the band-selection switching (see truth table). The 16-bit latch takes the data from the shift register when the enable input PLE is on low level.

Q1, Q2 The IC includes a crystal-controlled, 3-MHz clock oscillator. The output signal is divided down to 1.953125 kHz (reference signal) by a 1/1536 reference divider.

OSC The oscillator frequency appears at the TTL output OSC.

CLK The clock of 62.5 kHz is available at the open-collector output CLK.

PD The divided input signal is compared with the reference signal in a digital phase detector. If the falling edge of the input signal appears prior to the falling edge of the reference signal, the DOWN output of the phase detector turns to high level for the duration of this phase difference. In the reverse case the UP output turns to high level. If the two signals are in phase, both outputs remain at low level. The UP/DOWN outputs control the two current sources I^+ und I^- (charge pump). If the two outputs are low (PLL locked), the charge-pump output PD will turn to the high-impedance state (TRISTATE).

LOCK An L signal appears at the LOCK IND output if frequency and phase are

IND synchronous. The current sources I^+ and I^- are then reduced from 300 to 100 µA.

V_D The current pulses generated by the charge pump are integrated to form the tuning voltage by means of an active lowpass filter (external pull-up resistor to supply V_{S2} and external RC circuitry). The dc output signal appears at V_D and serves as a tuning voltage for the VCO.

UHF The band-selection outputs (UHF, VHF, Bd I/III) contain current drains with open

VHF collectors. In this way PNP transistors working as band-selection switches can be

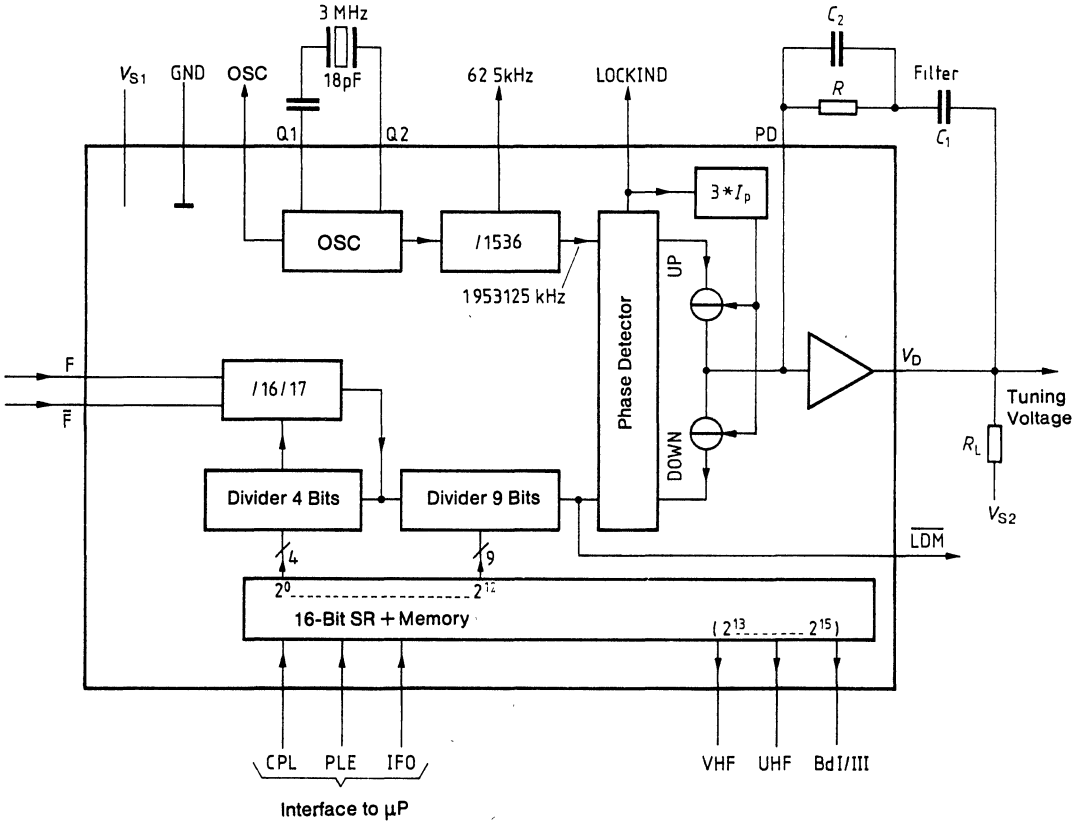
Bd I/III connected directly without current-limiting resistors (see application circuit).

7

Pin description

Pin	Symbol	Function
1	Q 2	Crystal
2	Q 1	Crystal
3	UHF	} Band selection outputs
4	VHF	
5	Bd I/III	
6	CLK	Clock output
7	CPL	Clock input
8	IFO	Data input
9	GND	Ground
10	PLE	Shift register enable input
11	V_D	Tuning voltage
12	LOCK IND	Lock indication output
13	OSC	Oscillator output
14	V_{PD}	Phase detector voltage
15	$\overline{F}$	Inverted input
16	F	Input
17	$\overline{LDM}$	Carry
18	V_{S1}	Supply voltage

Block diagram



7

Computation for loop filter

Loop bandwidth: $\omega_R = \sqrt{\frac{I_p \times K_{VCO}}{C_1 \times P \times N}}$

Attenuation: $\xi = 0.5 \times \omega_R \times R \times C_1$

P = Prescaler
N = Programmable divider
I_p = Pump current
K_{VCO} = Tuner slope
R, C_1 = Loop filter

Example for channel 47:

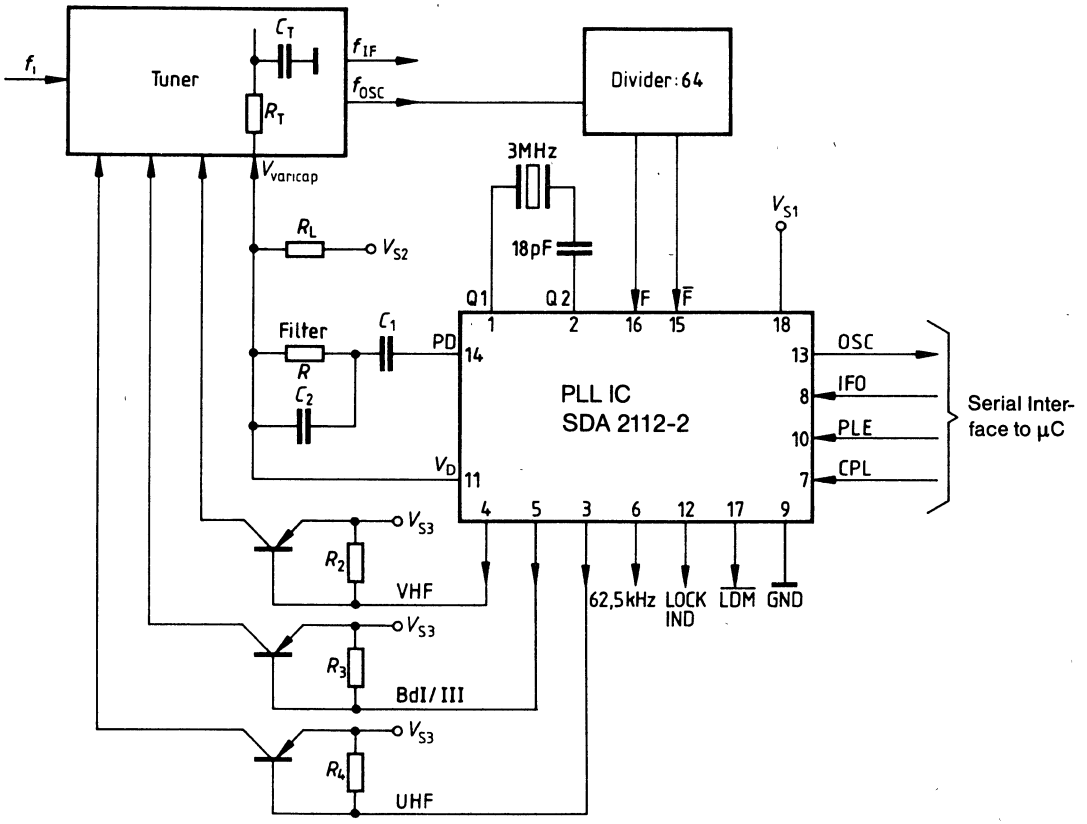
$P = 64$; $N = 5760$; $I_p = 100\ \mu A$; $K_{VCO} = 18.7$ MHz/V; $R = 33\ k\Omega$
$C_1 = 330$ nF; $\omega_R = 124$ Hz; $f_n = 20$ Hz; $\xi = 0.675$

Post filter: $R_t = 10\ k\Omega$; $C_t = 47$ nF

Standard dimensioning: $C_2 = C_{1/5}$

$V_{S1} = 5$ V; $V_{S2} = 33$ V; $V_{S3} = 12$ V; R_2 to $R_4 = 22\ k\Omega$; $R_L = 22\ k\Omega$

Application circuit

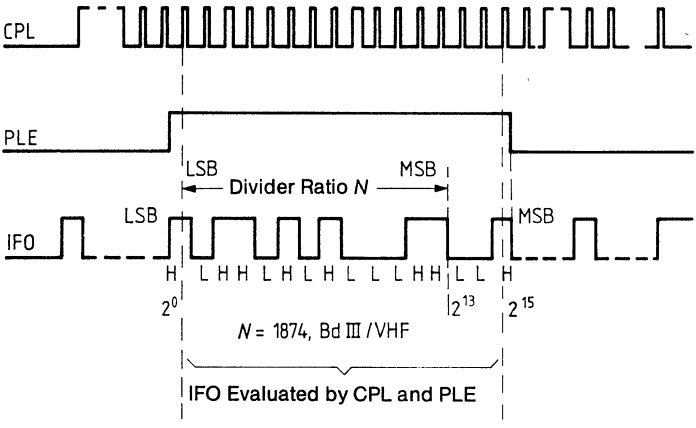


Truth table

Input "IFO" bit			Outputs			Meaning
2^{13}	2^{14}	2^{15}	Bd I/III	VHF	UHF	
H	H	L	H	H	L	"UHF"
H	L	H	H	L	H	"Bd I/VHF"
L	L	H	L	L	H	"Bd III/VHF"
L	H	H	L	H	H	"Bd III/VHF"

At positive logic, the "IFO" bits $2^0 \ldots 2^{12}$ complement the dual code from divider ratio *N*.

Pulse diagram



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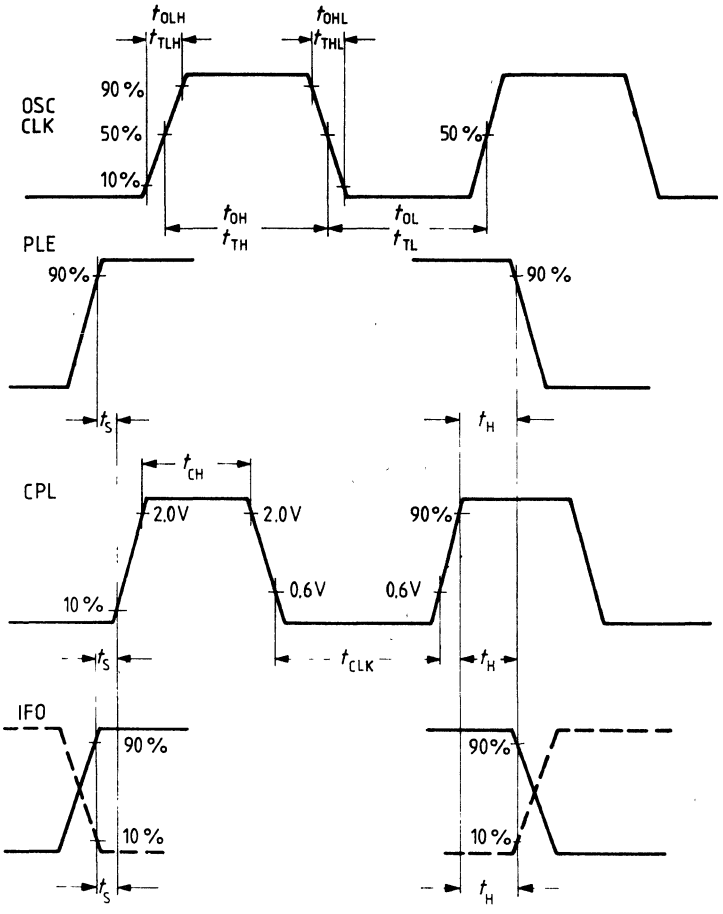
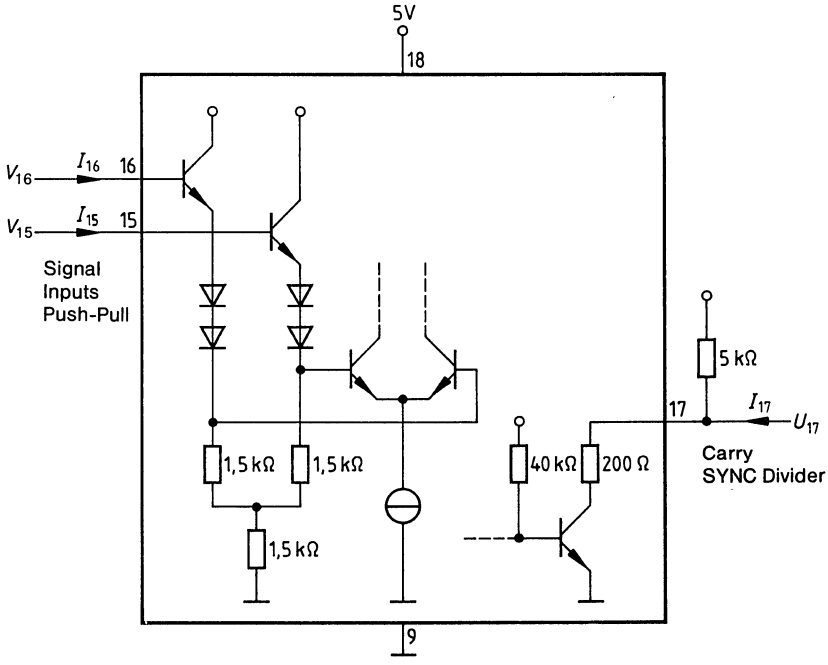
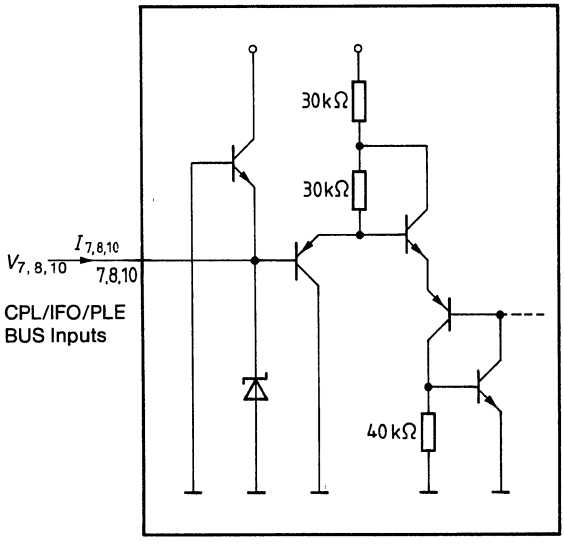
Pulse diagram



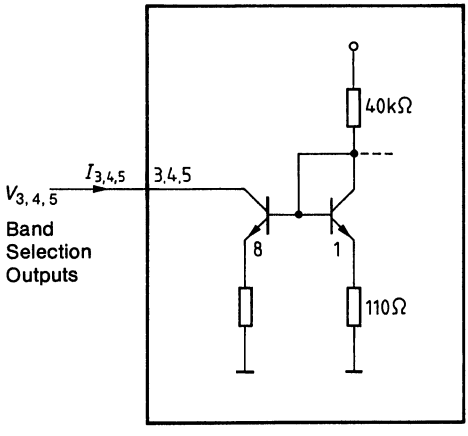
Test and measurement circuits



Test circuit 1

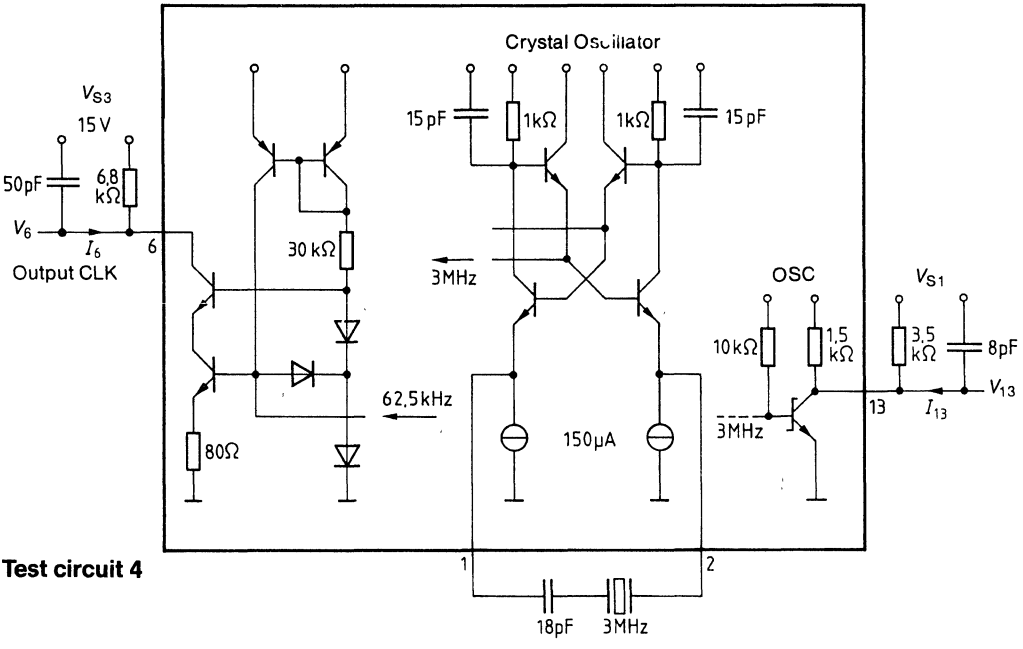


Test circuit 2

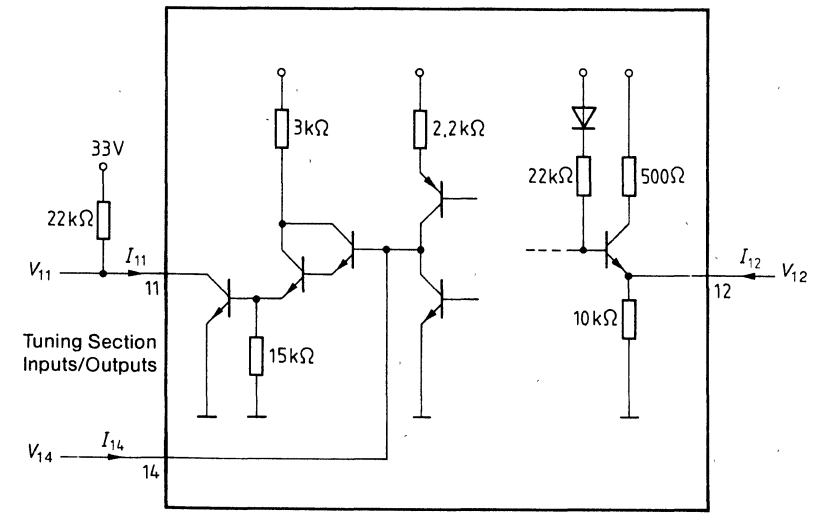


Test circuit 3

Test and measurement circuits



Test circuit 4



Test circuit 5

SIEMENS

SDA 2211
Pre-scaler 1:64 for 1.3 GHz with Low Current Consumption

Preliminary data

The IC has been designed for application in TV receivers using the frequency control of the frequency synthesis rough copy concept. It includes a pre-amplifier and an ECL pre-scaler with a 1:64 scaling rate and symmetrical ECL push-pull outputs. The operating range of the IC extends to an input frequency of 1.3 GHz.

- Minimal current consumption
- High input sensitivity

Maximum ratings

Supply voltage	V_S	– 0.3 to 6	V
Input voltage	$V_{i2,3}$	2.5	V_{PP}
Output voltage	$V_{q6,7}$	V_S	V
Output current	$-I_{q6,7}$	10	mA
Junction temperature	T_j	125	°C
Storage temperature range	T_{stg}	40 to 125	°C
Thermal resistance:			
System-air	R_{thSA}	115	K/W

Range of operation

Supply voltage	V_S	4.5 to 5.5	V
Input frequency	f	70 to 1300	MHz
Ambient temperature range	T_{amb}	0 to 70	°C

7

Characteristics (V_S = 4.5 - 5.5 V; T_{amb} = 0 - 70°C)

		min	typ	max	
Current consumption inputs blocked, outputs free	I_S		23	29	mA
Output voltage shift (at each output)	V_q				
$C_L \leq 15$ pF		0.5	1	1.2	dBm
$C_L = 60$ pF		0.35			dBm
Input level ("Input sensitivity")	V_I				
70 MHz		-26		3	dBm
80 MHz		-27		3	dBm
120 MHz		-30		3	dBm
250 MHz		-32		3	dBm
600 MHz		-27		3	dBm
1000 MHz		-27		3	dBm
1100 MHz		-27		3	dBm
1200 MHz		-21		3	dBm
1300 Mhz		-15		3	dBm

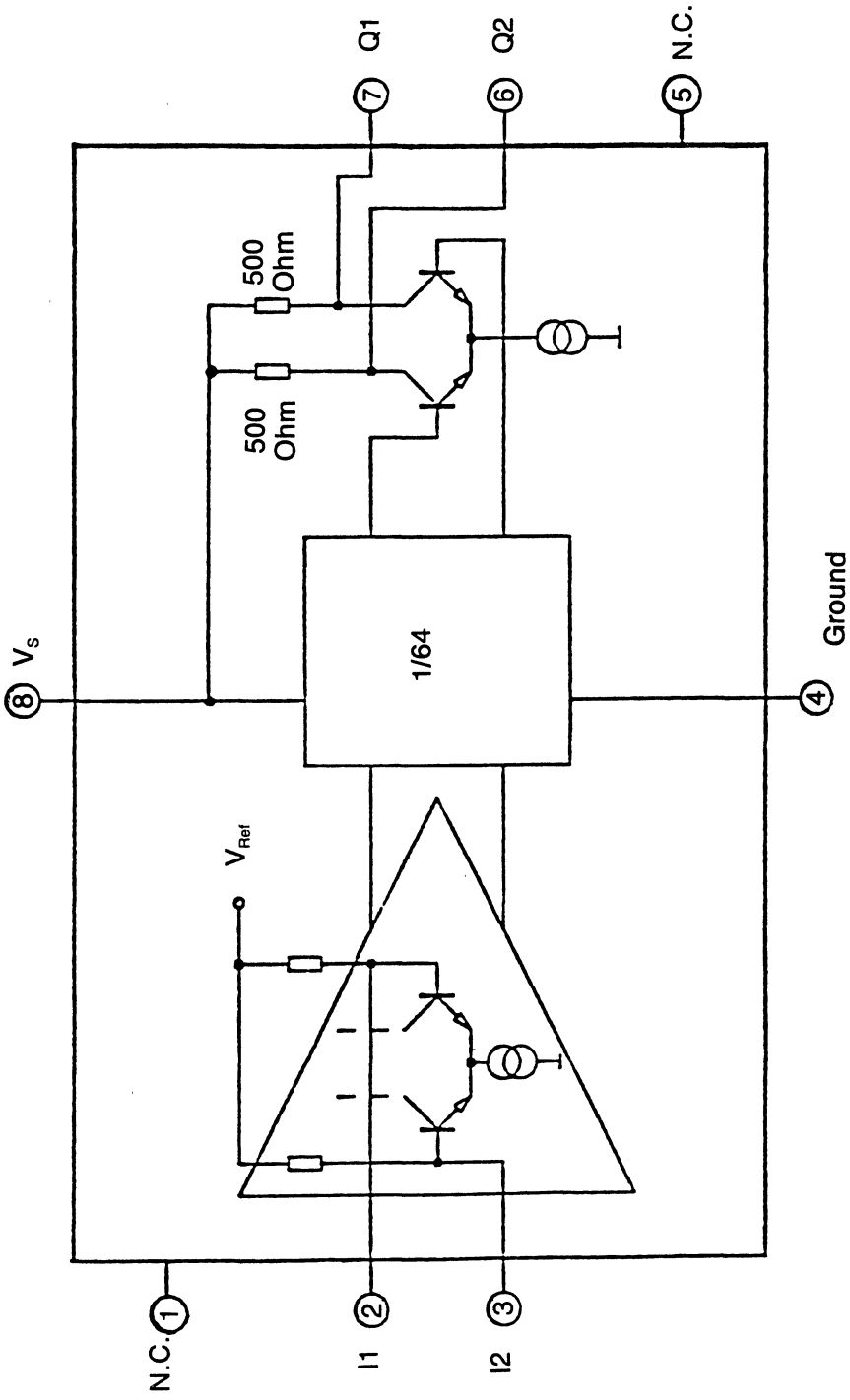
Circuit description

The pre-amplifier of the IC features symmetrical push-pull outputs. If one of the signal inputs is in an asymmetrical driving mode the other input should be grounded by a capacitor (~1.5 nF) with low series inductivity. The pre-scaler of the IC consists of several status controlled master slave flip flops with a 1:64 scaling rate.
The asymmetrical push-pull outputs of the pre-scaler have been designed with an internal resistance of 500Ω each. The DC voltage level of the outputs is connected to the supply voltage V_S (output "high" = V_S). The typical shift is 1 V_{PP}.

Pin configuration

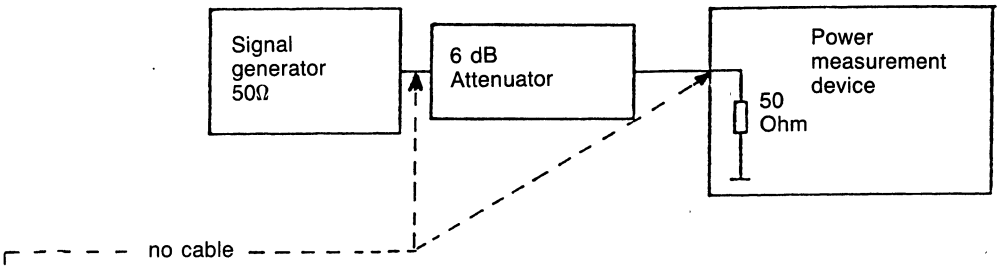
Pin-No.	Function
1	N.C.
2	Input I1
3	Input I2
4	Ground
5	N.C.
6	Output Q2
7	Output Q1
8	Supply voltage V_S

Block diagram

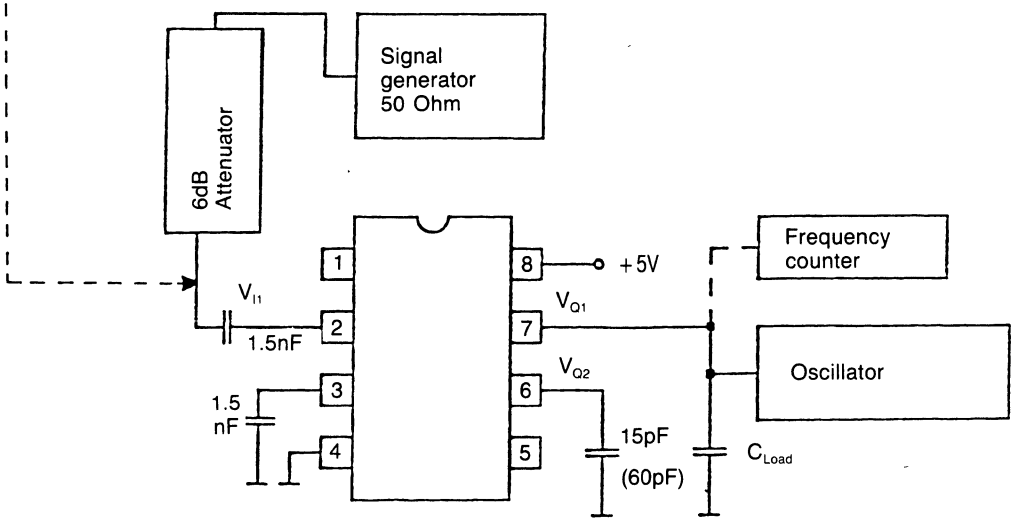


Test and measurement circuits

Signal generator calibration



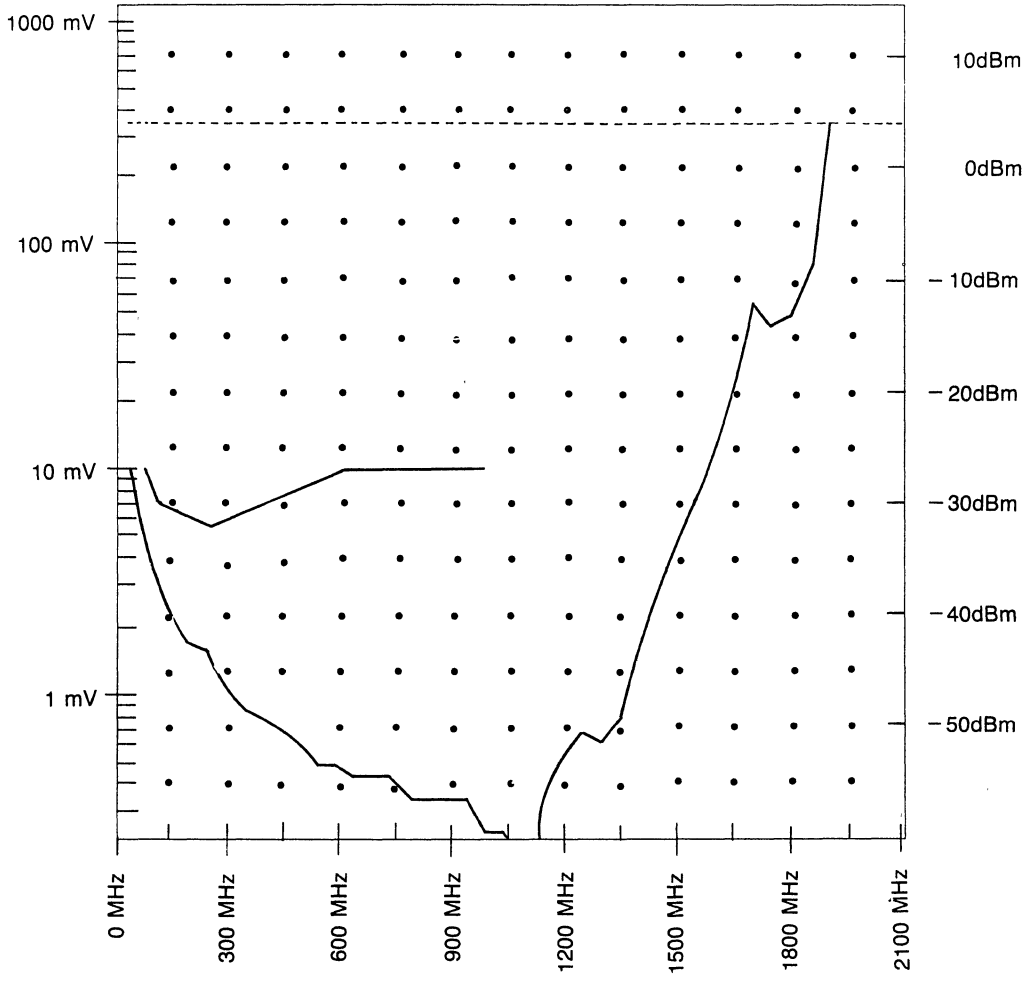
Measurement configuration for input sensitivity and the output voltage swing



Test circuit 1

Capacitive load definition for output voltage swing measurement:
C_{Load} + capacities of the measurement devices = 15 pF (60 pF)

Typical input sensitivity of pre-scaler
$V_S = 5$ V; $T_{amb} = 25°C$



7

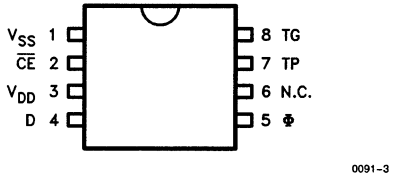
SIEMENS

Preliminary

SDA 2506
Nonvolatile Memory 1-kbit E²PROM

- Word-Organized Programmable Nonvolatile Memory in N-Channel Floating-Gate Technology
- 128 x 8 Bit Organization
- Supply Voltage 5V
- A Total of Three Lines Between Control Processor and the E²PROM for Data Transfer and Chip Control
- Data (8 Bits), Address (7 Bits), and Control Information Input (1 Bit) as well as Serial Data Output
- More than 10^4 Reprogramming Cycles Per Address
- Data Retention in Excess of 10 Years (Operating Temperature Range)
- Unlimited Number of Reads without Refresh
- Erase and Write in 10 ms

Pin Configuration



0091-3

Pin Description

Pin	Symbol	Function
1	V_{SS}	GND
2	$\overline{CE}$	Chip Enable
3	V_{CC}	Supply Voltage 5V
4	D	Data Input/Output
5	Φ	Clock Input
6	N.C.	Not Connected
7	TP	Test Input, at V_{SS}
8	TG	Test Input, Remains Open

The SDA 2506 is a serial E²PROM organized as 128 words by 8 bits. Packaged in an 8-pin plastic dual-in-line package, the device is controlled via a three-wire serial bus. The device requires only a single 5V supply for operation.

Data Transfer and Chip Control

The total data transfer between the control processor and the E²PROM requires three lines, each of which has several functions:

a. Data Line D
— Bidirectional serial data transfer
— Serial address input
— Clocked input of control information
— Direct control input

b. Clock Line Φ
— Data, address, and control bit input
— Data output
— Start of read with transfer of data from memory into shift register and/or start of data change during reprogramming

c. Chip Enable Line $\overline{CE}$
— Chip reset and data input (active high)
— Chip enable (active low)

Prior to chip enable, the data, address, and control information is clocked via the bidirectional data bus. During the reprogramming and read process, this data is retained in the shift register up to the second clock pulse. The following data formats must be entered:

a. Read Memory:
one 8-bit control word comprising:
— 7 address bits A0 to A6 (A0 goes first as LSB)
— 1 control bit, SB = "0", after A6

b. Reprogram Memory:
(erase and/or write operation)
16-bit input information comprising:
— 8 bits, D0 to D7 new memory information (D0 goes first as LSB)
— 7 bits, A0 to A6 address information (A0 as LSB goes first after D7)
— 1 bit, control information, SB = "1", after A6

Read (Figure 1)

Subsequent to data input and with SB = "0", the read process of the selected word address is started when $\overline{CE}$ changes from "1" to "0". The information on the data line is not effective during chip enable.

With the first clock pulse after $\overline{CE}$ = "0", the data word of the selected memory address is transferred into the shift register. After the first Φ pulse has ended, the data output becomes low in impedance and the first data bit can be read at the data pin. During each additional clock pulse, a data bit is shifted to the output. The data line returns to high-impedance mode when $\overline{CE}$ transitions from "0" to "1".

Reprogramming (Figure 2)

A full reprogramming process comprises an erase and a subsequent write process. During the erase process, all bits of the selected word are set to the "1" state. During a write process, the "0" states are set according to the information in the shift register.

The reprogramming process is started after data input during chip enable when the information SB = "1" is available in the relevant cell of the shift register. The selection of an erase or write process depends on the information on data line D during chip enable.

An erase process in the "1" state requires a "1" at the data input when $\overline{CE}$ transitions to low. Similarly, a write process in the "0" state requires that a "0" be present on the data line during chip enable.

To start the programming process, a start pulse must be present at clock input Φ. The control information on D must remain stable up to the rising edge of the start pulse. The active data change begins with the trailing edge of the start pulse. The programming process is ended by terminating chip enable, that is, when $\overline{CE}$ = "1".

The reprogramming of a word begins during the start and execution of the erase process. The erase process is ended when $\overline{CE}$ = "1". The control bit SB = "1" also required for the write process remains stable in the shift register after the erase process is terminated. The writing of the selected word, therefore, requires nothing more than changing data line D from"1" to "0", enabling the chip again with $\overline{CE}$ = "0" and starting the data change with the start pulse.

The erase and write processes can be performed separately. In order to ensure a uniform "1" state for all eight bits of the selected memory address during the erase process, a data word with eight times "1" must be entered prior to the erase process. When writing a word which was not erased previously, the "0" states of old and new information are added up.

Reset

A non-selected memory is automatically in the reset state due to $\overline{CE}$ = "1". All flipflops of the process control are reset. However, the information in the shift register is retained and changed only by shifting the data. The reset state is also set by on-chip circuitry during memory power on.

Certain applications require a "clear all" function. This can be done in the test mode as follows:

1) activate test mode by connecting TP (Pin 7) to V_{CC} (5V).
2) send address 0 ($A_0 \ldots A_6$) and control bit SB = 1.
3) set $\overline{CE}$ to "0" for 25 ms. The device will then "clear all".
4) The process is terminated by switching $\overline{CE}$ to "1", and connecting TP to ground.

Absolute Maximum Ratings*

Supply Voltage Range (V_{CC}) ..... −0.3V to 6V
Input Voltage Range (V_i) ..... −0.3V to 6V
Power Dissipation (P_V) ..... 40 mW
Storage Temperature Range (T_{stg}) . −40°C to 125°C
Thermal Resistance
(System-Air) (R_{thSA}) ..... 100 K/W

Operating Range

Supply Voltage (V_{CC}) ..... 4.75V to 5.25V
Ambient Temperature (T_A) ..... 0°C to 70°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Static Characteristics

Parameter	Symbol	Limits			Units
		Min	Typ	Max	
Supply Voltage	V_{CC}	4.75	5	5.25	V
Supply Current	I_{CC}			3	mA
Inputs	V_L			0.8	V
D, Φ, $\overline{CE}$	V_H	2.4			V
V_H = 5.25V	I_H			10	µA
Data Output D (Open Drain)					
V_L = 0.8V	I_L			0.5	mA
V_H = 5.25V	I_H			10	µA
Clock Pulse Φ					
High Duration Low Duration	Φ_H	2.5		60	µs
Before/After Φ_H	Φ_L	5			µs
Before/After $\overline{CE}$ Transition	Φ_L	5			µs
Before/After D Change	Φ_L	2.5			µs
Data D					
Before/After Φ Trailing Edge	D_H D_L	2.5 2.5			µs µs
Time Between Rising and Trailing Edge					
$\overline{CE}$ Referenced to D	Δt	2.5			µs
Erase Time	t_{er}	10		20	ms
Write Time	t_{wr}	10		20	ms

Read Cycle (1-kbit E²PROM)

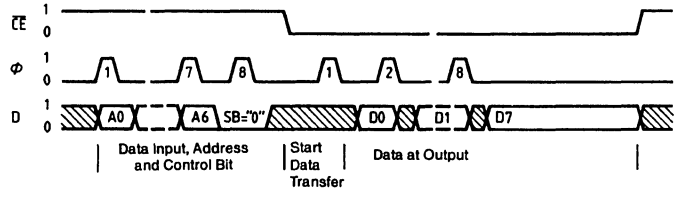


Figure 1

Reprogramming Cycle (1-kbit E²PROM)

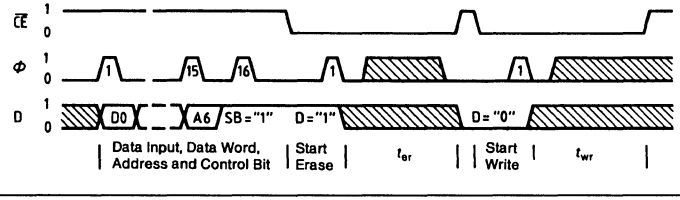


Figure 2

Ordering Information

Type	Ordering Code	Package
SDA 2506	Q67100-H8115	DIP 8

SIEMENS

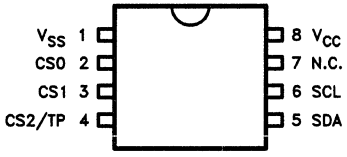
Preliminary

SDA 2516
Nonvolatile Memory 1-kbit E²PROM with I²C Bus Interface

- Word-Organized Programmable Nonvolatile Memory in n-Channel Floating-Gate Technology (E²PROM)
- 128 x 8 Bit Organization
- Supply Voltage 5V
- Serial 2-Line Bus for Data Input and Output (I²C Bus)
- Reprogramming Mode, 15 ms Erase/Write Cycle
- Reprogramming by Means of On-Chip Control (without External Control)
- Data Retention in Excess of 10 Years
- More than 10^4 Reprogramming Cycles per Address

Pin Configuration

(Top View)



0092-3

Pin Definitions

Pin	Symbol	Function
1	V_{SS}	GND
2	CS0	Chip Select Inputs / Test Operation Control
3	CS1	
4	CS2/TP	
5	SDA	Data Line (I²C Bus)
6	SCL	Clock Line (I²C Bus)
7	N.C.	Not Connected
8	V_{CC}	Supply Voltage

The I²C bus is a bidirectional 2-line bus for the transfer of data between various integrated circuits. It consists of a serial data line SDA and a serial clock line SCL. Both lines require an external pull-up resistor to V_{DD} (open drain output stages).

The possible operational states of the I²C bus are shown in Figure 1. In the quiescent state, both lines SDA and SCL are high, i.e. the output stages are disabled. As long as SCL remains "1", information changes on the data bus indicate the start or the end of a data transfer between two components. The transition on SDA from "1" to "0" is a start condition, the transition from "0" to "1" a stop condition. During a data transfer the information on the data bus will only change while the clock line SCL is "0". The information on SDA is valid as long as SCL is "1".

In conjunction with an I²C bus system, the memory component can operate as a receiver, and as a transmitter (slave receiver/listener, or slave transmitter/talker). Between a start and a stop condition, information is always transmitted in byte-organized form (8 bits). Between the trailing edge of the eighth transmission pulse and a ninth acknowledge clock pulse, the memory component sets the SDA line to low as a confirmation of reception, if the chip select conditions have been met. During the output of data, the data output becomes high in impedance if the master receiver leaves the SDA line high during the acknowledge clock pulse.

The signal timing required for the operation of the I²C bus is summarized in Figure 2 (high-speed mode).

Control Functions of the I²C Bus

The memory component is controlled by the controller (master) via the I²C bus in two operating modes: read cycle, and reprogramming cycle, including erase and write to a memory address. In both operating modes, the controller, as transmitter, has to provide 3 bytes and an additional acknowledge clock pulse to the bus after the start condition. A rapid read mode enables the reading of data immediately after the slave address has been input. During a memory read, at least eight additional clock pulses are required to accept the data from the memory, before the stop condition may follow. In the programming case, the active programming process is only started by the stop condition after data input.

With a 3-bit chip select word (CS0, CS1, CS2) it is possible for the user to individually address 8 memory components connected in parallel. Chip select is achieved when the three control bits logically correspond to the selected conditions at the three select inputs CS0, CS1, CS2.

Memory Read

After the input of the first two control words and 18 SCL pulses, a resetting of the start condition and the input of a third control word, the memory is set ready to read. During acknowledge clock nine, the memory information is transferred in parallel mode to the internal data register. Subsequent to the trailing edge of the acknowledge clock, the data output is low-ohmic and the first data bit can be sampled. With each shift clock, an additional bit reaches the output. After reading a byte, the internal address counter is automatically incremented through the master receiver acknowledge, so that any number of memory locations can be read one after the other. At address 127, an overflow to address 0 is initiated. With the stop condition, the data output returns to high-impedance mode. The internal sequence control of the memory component is reset from the read to the quiescent state with the stop condition.

Memory Reprogramming

The reprogramming cycle of a memory word comprises an erase and a subsequent write process. During erase, all eight bits of the selected word are set into the "1" state. During write, "0" states are generated according to the information in the internal data register, i.e. according to the third input control word.

After the 27th and last clock of the control word input, the active programming process is started by the stop condition. The active reprogramming process is executed under on-chip control and can be terminated by addressing the component via SCL and SDA.

The time required for reprogramming depends on component deviation and data patterns. Therefore, with rated supply voltage the erase/write process extends over maximum 30 ms or, more typically, 15 ms. For the input of a data word without write request (write request is defined as data bit in the data register set to "0"), the write process is suppressed and the programming time is shortened. During a subsequent programming of an already erased memory address, the erase process is suppressed again, so that the reprogramming time is also shortened.

Switch-On Mode and Chip Reset

After the supply voltage V_{CC} has been connected, the data output will be in the high impedance mode. As a rule, the first operating mode to be entered should be the read process of a word address. Subsequent to data output and the stop condition, the internal control logic is reset. However, in case of a subsequent active programming operation, the stop condition will not reset the control logic.

Test Mode—Total Erase

The address register is loaded with address 0, the data register with FF (hex) by entering the control word "programming". However, immediately prior to generating the stop condition, input CS2/TP is connected from 0V to 12V. The subsequent stop condition triggers a total erase procedure. which has to be performed under the component address 0 (CS0 = L, CS1 = L, CS2 = L).

Absolute Maximum Ratings*

Supply Voltage Range (V_{CC}) ..... −0.3V to +6V
Input Voltage Range (V_i) ..... −0.3V to +6V
Power Dissipation (P_V) ..... 50 mW
Storage Temperature
Range (T_{stg}) ..... −40°C to +125°C
Thermal Resistance (R_{thSA})
(System-Air) ..... 100 K/W

Operating Range

Supply Voltage (V_{CC}) ..... 4.75V to 5.25V
Ambient Temperature (T_A) ..... 0°C to +70°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Characteristics

Parameter	Symbol	Limits			Units
		Min	Typ	Max	
Supply Voltage	V_{CC}	4.75		5.25	V
Supply Current	I_{CC}			8	mA
Inputs SCL/SDA					
Low Level Input	V_{IL}			1.5	V
High Level Input	V_{IH}	3.0		V_{DD}	V
High Current ($V_{IH} = V_{DD\ Max}$)	I_{IH}			10	µA
Output SDA					
Low Current (V_{QL} = 0.4V)	I_{QL}			3.0	mA
Leakage Current ($V_{QH} = V_{DD\ Max}$)	I_{QH}			10	µA
Inputs CS0, CS1, CS2/TP					
Low Level Input	V_{IL}			0.2	V
High Level Input	V_{IH}	4.5		V_{CC}	V
High Current Input	I_{IH}			100	µA
Clock Frequency	f_{SCL}			100	KHz
Reprogramming Duration (Erasing and Writing)	t_{prog}		15	30	ms
Input Capacity	C_I			10	pF
Full Erase Duration (Test Mode Full Erase)	t_{er}			50	ms

Operational States of the I²C Bus

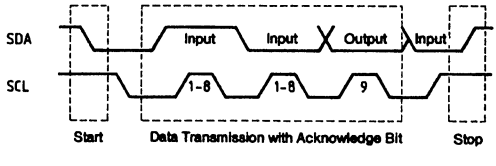


Figure 1

Timing Conditions for the I²C Bus (High-Speed Mode)

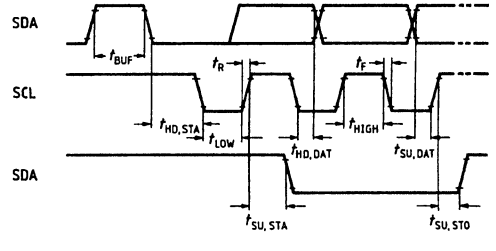


Figure 2

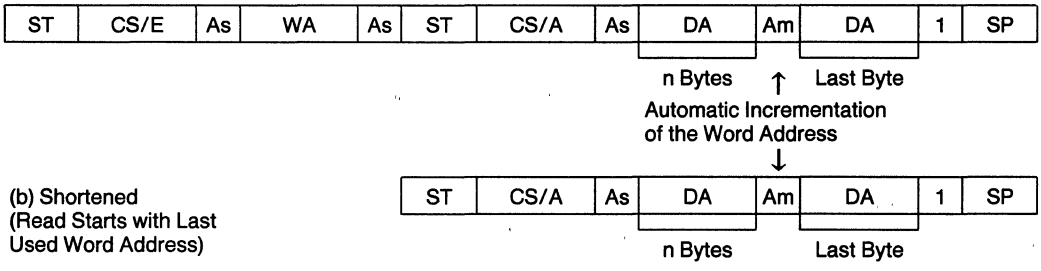
t_{BUF}	$t > t_{LOW\ Min}$	The minimum time the bus must be free before a new transmission can start
$t_{HD;\ STA}$	$t > t_{HIGH\ Min}$	Start Condition Hold Time
$t_{LOW\ Min}$	4.7 µs	Clock LOW Period
$t_{HIGH\ Min}$	4 µs	Clock HIGH Period
$t_{SU;\ STA}$	$t > t_{LOW\ Min}$	Start condition set-up time, only valid for reported start code
$t_{HD;\ DAT}$	$t > 0$ µs	Data Hold Time
$t_{SU;\ DAT}$	$t > 250$ ns	Data Set-Up Time
t_R	$t < 1$ µs	Rise Time of both the SDA and SCL Line
t_F	$t < 300$ ns	Fall Time of both the SDA and SCL Line
$t_{SU;\ STO}$	$t > t_{LOW\ Min}$	Stop Condition Set-Up Time

Note:
All values refer to V_{IH} and V_{IL} levels.

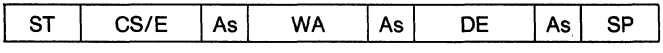
7

Control Word Input Read

a) Complete (with Word Address Input)



Control Word Input Program



(Reprogramming Starts after This Stop Condition)

Control Word Table

Clock No.	1	2	3	4	5	6	7	8	9	(Acknowledge)
CS/E	1	0	1	0	CS2	CS1	CS0	0	0	Through Memory
CS/A	1	0	1	0	CS2	CS1	CS0	1	0	Through Memory
WA	X	A6	A5	A4	A3	A2	A1	A0	0	Through Memory
DE	D7	D6	D5	D4	D3	D2	D1	D0	0	Through Memory
DA	D7	D6	D5	D4	D3	D2	D1	D0	0	Through Master

Control Word Input Key:

CS/E	Chip Select for Data Input into Memory
CS/A	Chip Select for Data Output out of Memory
WA	Memory Word Address
DE	Data Word for Memory
DA	Data Word Read out of Memory
D0 to D7	Data Bits
ST	Start Condition
SP	Stop Condition
As	Acknowledge Bit from Memory
Am	Acknowledge Bit from Master
CS0, CS1, CS2	Chip Select Bits
A0 to A6	Memory Word Address Bits

Ordering Information

Type	Ordering Code	Package
SDA 2516	Q67100-H8133	DIP 8

SIEMENS

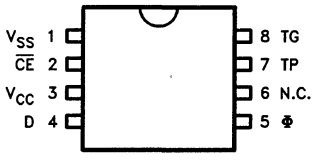
Preliminary

SDA 2526
Nonvolatile Memory 2-kbit E²PROM with I²C Bus Interface

- Word-Organized Programmable Nonvolatile Memory in n-Channel Floating-Gate Technology (E²PROM)
- 256 x 8 Bit Organization
- Supply Voltage 5V
- Serial 2-Line Bus for Data Input and Output (I²C Bus)
- Reprogramming Mode, 15 ms Erase/Write Cycle
- Reprogramming by Means of On-Chip Control (without External Control)
- Data Retention in Excess of 10 Years
- More than 10^4 Reprogramming Cycles per Address

Pin Configuration

(Top View)



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Pin Definitions

Pin	Symbol	Function
1	V_{SS}	Ground
2	$\overline{CE}$	Chip Enable
3	V_{CC}	Supply Voltage 5V
4	D	Data Input/Output
5	Φ	Clock Input
6	N.C.	Not Connected
7	TP	Test Input to V_{SS}
8	TG	Test Input, Remains Open

7

The I²C bus is a bidirectional 2-line bus for the transfer of data between various integrated circuits. It consists of a serial data line SDA and a serial clock line SCL. Both lines require an external pull-up resistor to V_{DD} (open drain output stages).

The possible operational states of the I²C bus are shown in Figure 1. In the quiescent state, both lines SDA and SCL are high, i.e. the output stages are disabled. As long as SCL remains "1", information changes on the data bus indicate the start or the end of a data transfer between two components. The transition on SDA from "1" to "0" is a start condition, the transition from "0" to "1" a stop condition. During a data transfer the information on the data bus will only change while the clock line SCL is "0". The information on SDA is valid as long as SCL is "1".

In conjunction with an I²C bus system, the memory component can operate as a receiver, and as a transmitter (slave receiver/listener, or slave transmitter/talker). Between a start and a stop condition, information is always transmitted in byte-organized form (8 bits). Between the trailing edge of the eighth transmission pulse and a ninth acknowledge clock pulse, the memory component sets the SDA line to low as a confirmation of reception, if the chip select conditions have been met. During the output of data, the data output becomes high in impedance if the master receiver leaves the SDA line high during the acknowledge clock pulse.

The signal timing required for the operation of the I²C bus is summarized in Figure 2 (high-speed mode).

Control Functions of the I²C Bus

The memory component is controlled by the controller (master) via the I²C bus in two operating modes: read cycle, and reprogramming cycle, including erase and write to a memory address. In both operating modes, the controller, as transmitter, has to provide 3 bytes and an additional acknowledge clock pulse to the bus after the start condition. A rapid read mode enables the reading of data immediatley after the slave address has been input. During a memory read, at least eight additional clock pulses are required to accept the data from the memory, before the stop condition may follow. In the programming case, the active programming process is only started by the stop condition after data input.

With a 3-bit chip select word (CS0, CS1, CS2) it is possible for the user to individually address 8 memory components connected in parallel. Chip select is achieved when the three control bits logically correspond to the selected conditions at the three select inputs CS0, CS1, CS2.

Memory Read

After the input of the first two control words and 18 SCL pulses, a resetting of the start condition and the input of a third control word, the memory is set ready to read. During acknowledge clock nine, the memory information is transferred in parallel mode to the internal data register. Subsequent to the trailing edge of the acknowledge clock, the data output is low-ohmic and the first data bit can be sampled. With each shift clock, an additional bit reaches the output. After reading a byte, the internal address counter is automatically incremented through the master receiver acknowledge, so that any number of memory locations can be read one after the other. At address 255, an overflow to address 0 is initiated. With the stop condition, the data output returns to high-impedance mode. The internal sequence control of the memory component is reset from the read to the quiescent state with the stop condition.

Memory Reprogramming

The reprogramming cycle of a memory word comprises an erase and a subsequent write process. During erase, all eight bits of the selected word are set into the "1" state. During write, "0" states are generated according to the information in the internal data register, i.e. according to the third input control word.

After the 27th and last clock of the control word input, the active programming process is started by the stop condition. The active reprogramming process is executed under on-chip control and can be terminated by addressing the component via SCL and SDA.

The time required fro reprogramming depends on components deviation and data patterns. Therefore, with rated supply voltage the erase/write process extends over maximum 30 ms or, more typically, 15 ms. For the input of a data word without write request (write request is defined as data bit in the data register set to "0"), the write process is suppressed and the programming time is shortened. During a subsequent programming of an already erased memory address, the erase process is suppressed again, so that the reprogramming time is also shortened.

Switch-On Mode and Chip Reset

After the supply voltage V_{CC} has been connected, the data output will be in the high impedance mode. As a rule, the first operating mode to be entered should be the read process of a word address. Subsequent to data output and the stop condition, the internal control logic is reset. However, in case of a subsequent active programming operation, the stop condition will not reset the control logic.

Test Mode—Total Erase

The address register is loaded with address 0, the data register with FF (hex) by entering the control word "programming". However, immediately prior to generating the stop condition, input CS2/TP is connected from 0V to 12V. The subsequent stop condition triggers a total erase procedure. which has to be performed under the component address 0 (CS0 = L, CS1 = L, CS2 = L).

Absolute Maximum Ratings*

Supply Voltage Range (V_{CC}) ..... −0.3V to +6V
Input Voltage Range (V_i) ..... −0.3V to +6V
Storage Temperature
Range (T_{stg}) ..... −40°C to +125°C
Thermal Resistance (R_{thSA})
(System-Air) ..... 100 k/W

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Operating Range

Supply Voltage (V_{CC}) ..... 4.75V to 5.25V
Ambient Temperature (T_A) ..... 0°C to +70°C

Characteristics

Parameter	Symbol	Limits			Units
		Min	Typ	Max	
Supply Voltage	V_{CC}	4.75		5.25	V
Supply Current	I_{CC}			10	mA
Inputs SCL/SDA					
Low Level	V_{IL}			0.8	V
High Level	V_{IH}	3.0		V_{DD}	V
High Current ($V_{IH} = V_{DD\ Max}$)	I_{IH}			10	μA
Output SDA					
Low Current (V_{QL} = 0.4V)	I_{QL}			2.0	mA
Leakage Current ($V_{QH} = V_{DD\ Max}$)	I_{QH}			10	μA
Inputs CS0, CS1, CS2/TP					
Low Level	V_{IL}			0.2	V
High Level	V_{IH}	4.5		V_{DD}	V
High Current	I_{IH}			100	μA
Clock Frequency	f_{SCL}			100	kHz
Reprogramming Duration (Erasing and Writing)	t_{prog}		15	30	ms
Input Capacity	C_I			10	pF
Full Erase Duration (Test Mode Full Erase)	t_{er}			50	ms
Condition	$V_{CS2/TP}$	11	12	13	V

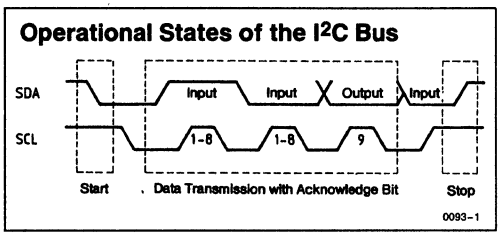


Figure 1

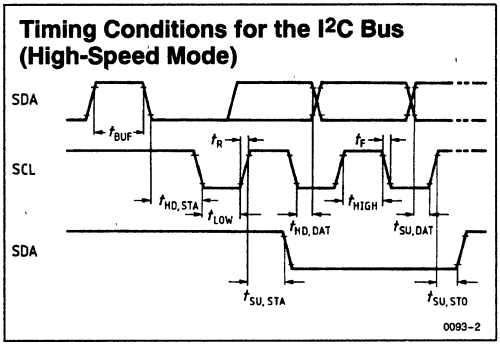


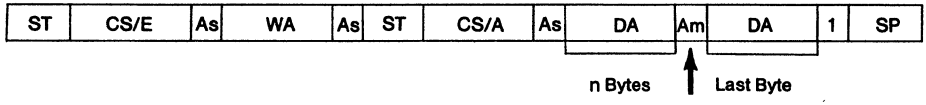
Figure 2

t_{BUF}	$t > t_{LOW\ Min}$	The minimum time the bus must be free before a new transmission can start
$t_{HD;\ STA}$	$t > t_{HIGH\ Min}$	Start Condition Hold Time
$t_{LOW\ Min}$	4.7 µs	Clock LOW Period
$t_{HIGH\ Min}$	4 µs	Clock HIGH Period
$t_{SU;\ STA}$	$t > t_{LOW\ Min}$	Start condition set-up time, only valid for reported start code
$t_{HD;\ DAT}$	$t > 0$ µs	Data Hold Time
$t_{SU;\ DAT}$	$t > 250$ ns	Data Set-Up Time
t_R	$t < 1$ µs	Rise Time of both the SDA and SCL Line
t_F	$t < 300$ ns	Fall Time of both the SDA and SCL Line
$t_{SU;\ STO}$	$t > t_{LOW\ Min}$	Stop Condition Set-Up Time

Note:
All values refer to V_{IH} and V_{IL} levels.

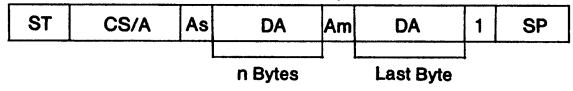
Control Word Input Read

a) Complete (with Word Address Input)

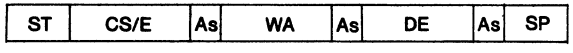


Automatic Incrementation of the Word Address

b) Shortened (Read Starts with Last Used Word Address)



Control Word Input Program



(reprogramming starts after this stop condition)

0093-3

Control Word Table

Clock No.	1	2	3	4	5	6	7	8	9	(Acknowledge)
CS/E	1	0	1	0	CS2	CS1	CS0	0	0	Through Memory
CS/A	1	0	1	0	CS2	CS1	CS0	1	0	Through Memory
WA	X	A6	A5	A4	A3	A2	A1	A0	0	Through Memory
DE	D7	D6	D5	D4	D3	D2	D1	D0	0	Through Memory
DA	D7	D6	D5	D4	D3	D2	D1	D0	0	Through Master

Control Word Input Key:

CS/E	Chip Select for Data Input into Memory
CS/A	Chip Select for Data Output out of Memory
WA	Memory Word Address
DE	Data Word for Memory
DA	Data Word Read out of Memory
D0 to D7	Data Bits
ST	Start Condition
SP	Stop Condition
As	Acknowledge Bit from Memory
Am	Acknowledge Bit from Master
CS0, CS1, CS2	Chip Select Bits
A0 to A6	Memory Word Address Bits

Ordering Information

Type	Ordering Code	Package
SDA 2526	Q67100-H8184	DIP 8

7

SIEMENS

SDA 3112
TV PLL

The SDA 3112 is produced in ASBC technology. In connection with VCO (tuner) and a fast prescaler (prescaler factor 1:64), it represents a digitally programmable PLL for a TV set with frequency synthesis tuning. The PLL enables a crystal exact adjustment of the tuner oscillator frequencies for the TV ranges band III/IV/V in 125 kHz resolution (frequency range: 128 to 2000 MHz). A serial interface enables a simple connection to a microprocessor. This microprocessor loads the prescaler and band selection outputs with the appropriate information. At the output LOCK the PLL supplies a state information (locked/released).

Features

- No need for an external integrator
- Noise free telegram transmission
- Integration time constant controlled by software
- Microprocessor compatible

Maximum ratings

Supply voltage	V_S	−0.3 to 7.5	V
Inputs			
Q1, Q2, I_{ref}	V_I	−0.3 to V_S	V
IFO, CPL, PLE	V_I	−0.3 to V_S +0.5	V
PLE	V_I	−0.3 to 7.8	V
F, $\overline{F}$	V_I	−0.3 to V_S + 0.5	V
Outputs			
PD	V_Q	−0 3 to V_S	V
UD	V_Q	−0.3 to 33	V
	I_{QL}	−7	mA
$\overline{BS1}$....$\overline{BS5}$	V_Q	−0.3 to 16	V
LOCK	I_Q	−1 to 5	mA
Internal pull-up $R_L = 3\ k\Omega$			
Junction temperature	T_j	140	°C
Storage temperature range	T_{stg}	−55 to 150	°C
Thermal resistance (system-air)	R_{thSA}	80	K/W

Operating range

Supply voltage range	V_S	4.5 to 5.5	V
Input frequency	$f_F, f_{\overline{F}}$	32	MHz
Divider ratio	N	1024 to 16383	
Resistance for I_{ref} $I_{ref} = (V_S - 0.8)R_I$	R_I	80	kΩ
Tuning voltage range open collector	V_D	0.3 to 33	V
Ambient temperature range	T_{amb}	0 to 85	°C

Characteristics ($V_S = 5\ V \pm 0.5\ V$; $T_{amb} = 0$ to 70 °C)

		min	typ	max	
Supply current	I_S	15	22	35	mA
Crystal frequency Series C = 18 pf	f_q		4		MHz
Signal inputs F/$\overline{F}$					
Input voltage	V_{16H}	3.92		$V_S + 0.12$	V
	V_{16L}	3.8		V_S	V
Input current	I_{16}			50	μA
$V_{16} = 5$ V					
Input sensitivity at sine push-pull triggering ; $f = 32$ MHz	V_{16}	120		1200	mV_{pp}
Inputs (IFO, CPL, PLE)					
Upper threshold voltage	V_{8H}	2.4			V
Lower threshold voltage	V_{8L}			0.8	V
Input current					
$V_{8H} = 5$ V	I_{8H}			8	μA
$V_{8L} = 0.4$ V	I_{8L}			−550	μA
$V_{8L} = 0.8$ V	I_{8L}			−500	μA
Band select outputs (BS1. . . . BS5)					
Reverse current	I_{3H}			10	μA
$V_{3H} = 15$ V					
Current drain	I_{3H}	0.5		3	mA
$2\ V \leqq V_3 \leqq 15\ V$					
Tuning section PD, UD, I_{ref}, LOCK					
Charge pump current	I_{13}	±250		±550	μA
$I_{pump} = 10 \times I_{ref}$; $R_I = 120\ k\Omega$; $V_S = 5V$					
Tuning voltage	V_{15L}			0.3	V
$I_{15L} = 1.5$ mA					
Reverse current	I_{15H}			20	μA
$V_{15H} = 33$ V					
Reference current	I_{14}	30		40	μA
ext. $R = 120\ k\Omega$					
Output voltage	V_{12H}	4.5			V
int. $R_L = 3\ k\Omega$					
$I_{12H} = -100\ \mu A$					
$I_{12L} = 100\ \mu A$	V_{12L}			0.7	V
IFO, PLE					
Set-up time for					
release	t_{VE}	2			μs
data	t_{VD}	2			μs
Hold time for:					
release	t_{HE}	2			μs
data	t_{HD}	2			μs
CPL					
H pulse width	t_{CH}	2			μs
L pulse width	t_{CL}	2			μs

7

Circuit description

Triggered by the ECI inputs F/$\overline{F}$ a switchable 32/33 counter operates as a 14 bit synchronous prescaler in the dual modulus method by combining it with a 5 and 9 bit programmable synchronous counter. In this combination the 5 bit counter controls the switch-over from 32 to 33 (block diagram 1). Dividing ratios of $N = 1024$ to 16383 are possible.

The 18 bit deep shift register latch is subdivided into 14 bits for storing the dividing ratio N, as well as 1 bit for selecting the pump current and 3 bits for controlling the 5 band selection outputs.

The telegram is inserted over the serial data input IFO with the H-L slope of the shift clock CPL, when the enable input is set at H. Beginning with LSB, the complement of the dividing ratio is inserted in binary code, then the select bit 2^{14} for the pump current and the band selection control bits 2^{15}, 2^{16}, 2^{17} (please refer to enclosed table).

An integrated control circuit checks the world length (18 bit) of the data telegram. The 18 bit latch accepts the data from the shift register during the L state of the enable input PLE.

A 4 MHz crystal controlled clock oscillator has been integrated in the IC. An internal reference divider divides the output signal of the crystal oscillator ($f_{OSC} = 4$ MHz) by 2048 resulting in 1.953125 kHz (reference signal), providing a frequency resolution of 125 kHz by means of the asynchronous permanent prescaler (dividing factor 1:64).

In a digital phase detector the divided VCO input signal is compared with the reference signal. If the falling slope of the VCO input signal appears before the falling slope of the reference signal, the output DOWN of the phase detector will be in the H state for the duration of the phase difference. However, if above signal sequence is reversed, the output UP will be in the H state instead. The outputs UP/DOWN control the two current sources I+ and I− (charge pump). In case both outputs are in the L state, the charge pump output will be in the high impedance mode (TRI-STATE). Information with respect to either the H or L state will be provided at the LOCK output by the logical "NOR" of the outputs UP/DOWN.

The output current of the charge pump (source current = drain current) is adjusted by an external resistor between pin I_{ref} and V_{CC}. In addition, this output current can be generated by the control bit for the pump current at the same value or at a value increased by a factor of 10 (refer to enclosed table).

The current pulses generated by the charge pump are integrated into the tuning voltage by means of an active low pass filter (on-chip loop amplifier and external RC circuit). The dc output signal of the low pass filter is available at V_D and is used as tuning voltage for the VCO. In order to provide tuning voltages higher than $V_{CC} = 5$ V, the output stage of the amplifier consists of a transistor with an open collector. The external collector resistor can be connected to voltages up to 33 V.

To switch voltages higher than $V_S = 5$ V, the band selection outputs (BS1, BS2, BS3, BS4, BS5) include current drains with open collectors. It is therefore possible to directly connect transistors operating as band selection switches without the use of current limiting resistors (please refer to enclosed application current).

Pin configuration

Pin No.	Symbol	Function
1	Q1	Crystal
2	Q2	Crystal
3	BS1	Standard switchover output
4	BS2	Band selection output BS
5	BS3	Band selection output VHF
6	BS4	Band selection output UHF
7	BS5	Band selection output I/III
8	PLE	Release input for shift register
9	GND	Ground
10	CPL	Shift clock pulse input
11	IFO	Data input
12	LOCK	Lock output
13	PD	Amplifier input/charge pump output
14	I_{ref}	Current adjustment for charge pump
15	V_D	Tuning voltage output
16	$\underline{F}$	Signal input
17	$\overline{F}$	Signal input
18	V_S	Supply voltage

Loop-filter calculations

Loop bandwidth: $\sqrt{\frac{I_p \times K_{VCO}}{C_1 \times P \times N}} = \omega_R$

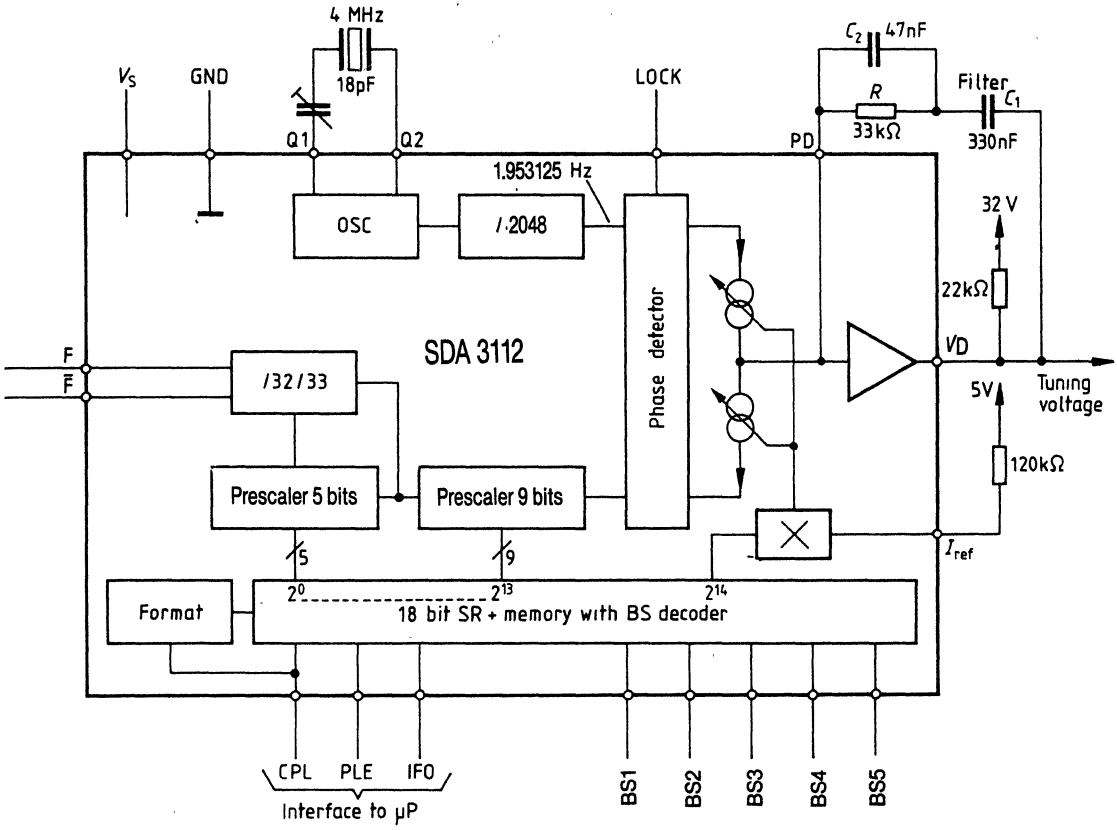
Attenuation $1/2 \times \omega_R \times R \times C_1 = \xi$

P = prescaler
N = programmable divider ratio
I_p = pump current
S_{VCO} = tuner voltage characteristic
R_1 C_1 = loop filter

Example for channel 47:

P = 64 N = 11520 I_p = 200 µA S_{VCO} = 18.7 MHz/V R = 33 kΩ C_1 = 330 nF
ω_R = 124 Hz f_R = 20 Hz ξ = 0.675 Standard dimensioning: $C_2 \approx C1/5$

Block diagram

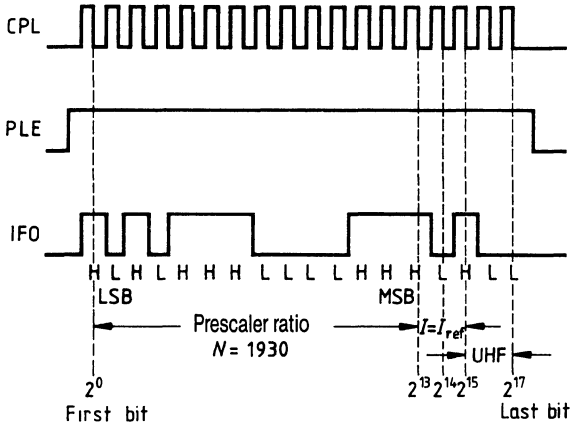


Truth Table

"IFO" bit 2^{14}	Pump Current I_p
L	I_{ref}
H	10 x I_{ref}

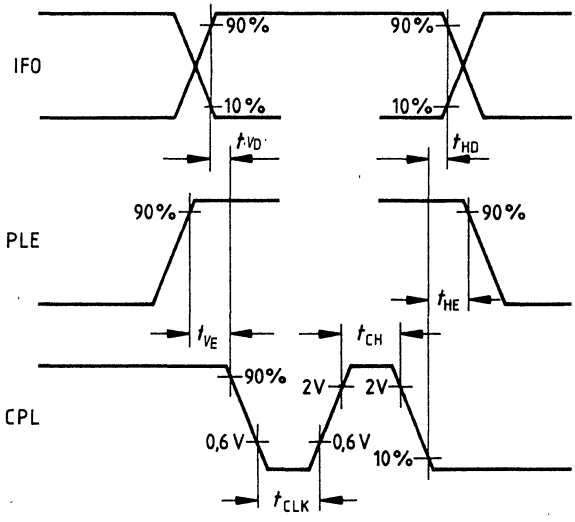
"IFO" bit			Band selection outputs (L = conducting, H = blocking)				
2^{15}	2^{16}	2^{17}	BS1	BS2	BS3	BS4	BS5
L	L	L	L	L	L	L	H
L	L	H	L	L	H	H	H
L	H	L	L	H	L	H	L
L	H	H	L	H	H	H	H
H	L	L	H	L	L	L	H
H	L	H	H	L	H	H	H
H	H	L	H	H	L	H	L
H	H	H	H	H	H	H	H

Pulse diagram

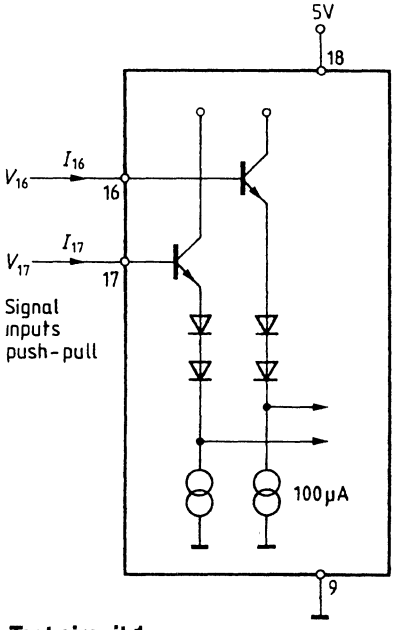


Pulse diagram

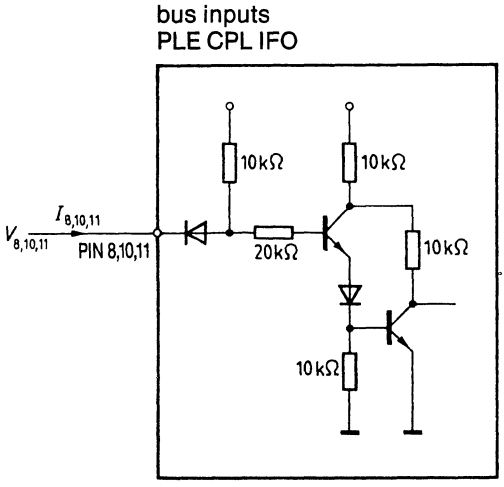
Set-up and hold times



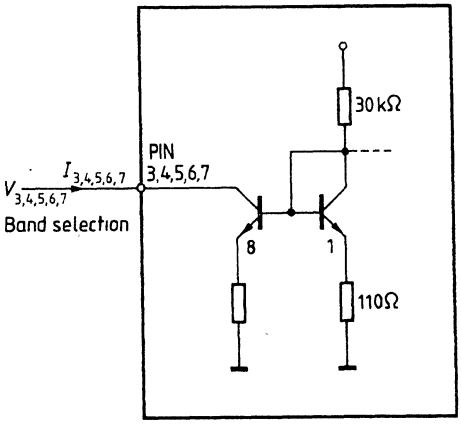
Test and measurement circuits



Test circuit 1



Test circuit 2



Test circuit 3

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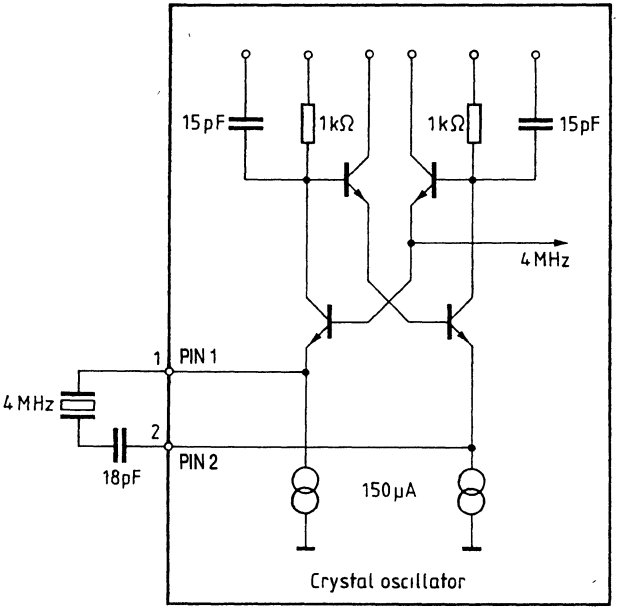
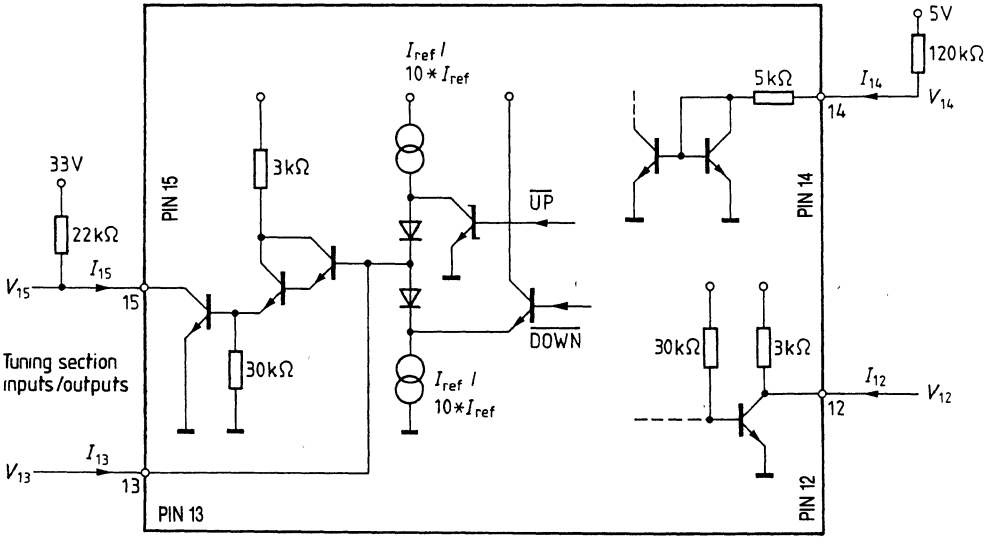
Test and measurement circuits



Test circuit 4

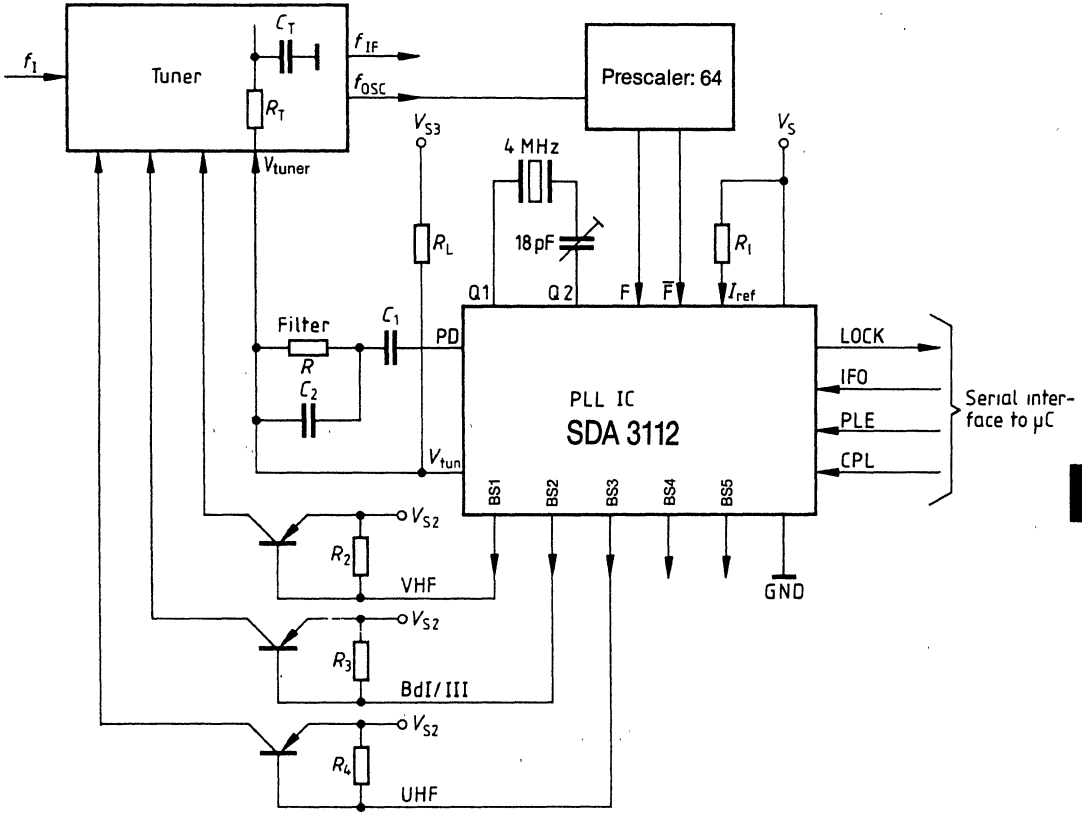


Test circuit 5

Application circuit

Design proposal

$R_I = 120\ k\Omega$ ($I_p = 35/350\ \mu A$)
$R_L = 22\ k\Omega$, $R_2 \ldots R_4 = 22\ k\Omega$
Loop filter: $R = 33\ k\Omega$, $C_1 = 330\ nF$, $C_2 = 47\ nF$
Post filter (in the tuner): $R_T = 10\ k\Omega$, $C_T = 47\ nF$



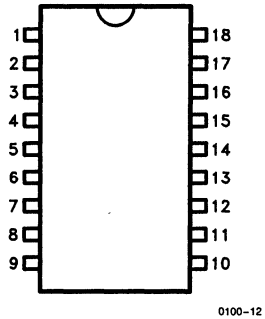
SIEMENS

SDA 3202
1.3 GHz PLL with I²C Bus

- Low Current Consumption
- Message Transmission Via I²C Bus
- 4 Software-Controlled Outputs
- Cost-Effective and Space-Saving Design
- Prescaler Output Frequency is Free from Interference Radiation

Pin Configuration

Top View



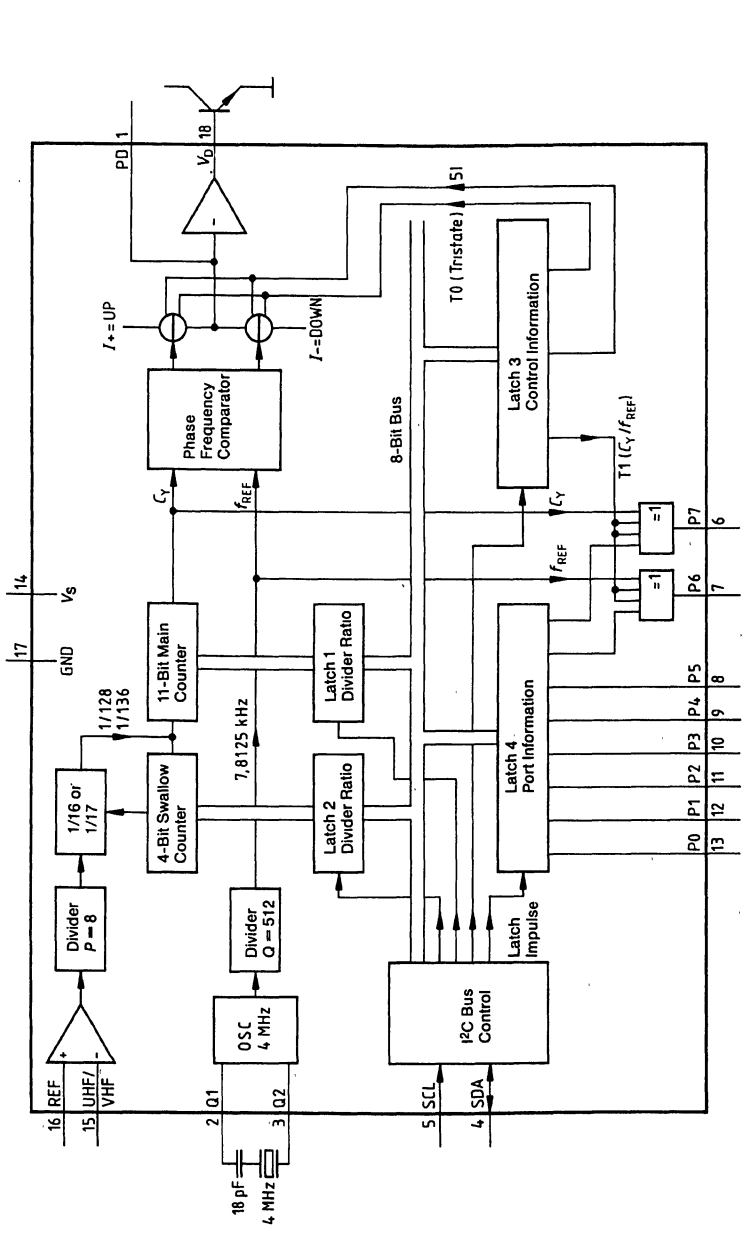
Pin Definitions

Pin	Symbol	Function
1	PD	Input for Active Filter/Output for Charge Pump
2	Q1	Crystal
3	Q2	Crystal
4	SDA	Data I/O for I²C Bus
5	SCL	Clock Input for I²C Bus
6	P7	Port Output (Open Collector)
7	P6	Port Output (Open Collector)
8	P5	Port Output (Open Collector)
9	P4	Port Output (Open Collector)
10	P3	Port Output (Current Sink)
11	P2	Port Output (Current Sink)
12	P1	Port Output (Current Sink)
13	P0	Port Output (Current Sink)
14	V_S	Supply Voltage
15	UHF/VHF	Signal Input
16	REF	Amplifier-Reference Input
17	GND	Ground
18	V_D	Output of Active Filter

Combined with a VCO (tuner), the SDA 3203 comprises a digital programmable phase-locked loop for television devices designed to use the PLL frequency synthesis tuning principle.

The PLL provides a cyrstal-stable frequency for tuner oscillators between 16 ... 1300 MHz in the 62.5 KHz raster. By including an external prescaler 1/2, the component can also be used for synthesizing applications of up to 2.4 GHz (e.g. satellite receivers). As a result, the resolution is doubled to 125 KHz. The tuning process is controlled via an I²C bus by the microprocessor.

Block Diagram



Circuit Description

Tuning Section (refer to block diagram)

UHF/VHF The tuner signal is capacitively coupled at the UHF/VHF input and subsequently amplified.

REF The reference input REF should be disabled by a capacitor of low series inductance. The amplified signal passes through an asynchronous divider with a fixed ratio of P = 8 and an adjustable divider N = 256...32767. Subsequent to this process, the signal is compared in a digital frequency phase detector with a reference frequency f_{REF} = 7.8125 kHz.

Q1, Q2 This frequency has been derived from a 4 MHz crystal oscillator (pin Q1, Q2) by dividing its output signal by Q = 512.

The phase detector includes two outputs UP and DOWN which control the two current sources I+ and I− of a charge pump. If the negative edge of the divided VCO signal appears prior to the negative edge of the reference signal, the current source I+ will pulsate for the duration of the phase difference. However, during the reversed sequence of the negative edges, the current source I− will begin to pulsate.

PD, V_D If both signals are in phase, the charge pump output PD changes into the high impedance state (PLL in lock). An active low pass filter (internal amplifier, external output transistor at V_D, and RC combination) integrates the current pulses as the tuning voltage for the VCO.

With the control bit 5 I the pump current can be switched between two values per software. Through this switch-over, the control characteristics of the PLL during lock-in can be changed, i.e. varying tuner characteristics in the various TV bands can be adjusted.

P0 . . . P3 The software-controllable outputs P0, P1, P2 and P3 can drive external PNP transistors (internal current limit) which operate as band selection switch.

P4 . . . P7 The open collector outputs P4, P5, P6, P7 can be used for a variety of different applications.

I²C Bus Interface

SCL, SDA An asynchronous bidirectional data bus is used for data transfer between the processor and the PLL. As a rule, the clock pulse is supplied by the processor (input SCL), while pin SDA operates as input or output depending on the direction of data flow (open collector, external pull-up resistor).

The data from the processor pass through an I²C bus control. Depending on their function, the data are subsequently filed in registers (latch 0–3). If the bus is free, both lines will be in the marking state (SDA, SCL are HIGH). Each tele- begins with the start conditions of SDA returning into Low, while SCL remains in High. All additional information transfer takes place during SCL = Low and the data is forwarded to the control with the positive clock edge. However, if SDA returns to High, while SCL is in High, the message is ended since the PLL acknowledges a stop condition.

For the following, also refer to table "Logic allocation".

All messages are transmitted byte-by-byte, followed by a 9. clock pulse, while the control returns the SDA line to Low (acknowledge conditions). The first byte is comprised of 7 address bits. These are used by the processor to select the PLL from several peripheral components (chip-select). The 8. bit is always Low.

In the data portion of the message the 1. bit of the 1. or 3. data byte determines whether a divider ratio or a control information is to follow. In each case, the 2. byte of the same data type or a stop condition has to follow the 1. byte.

V_S, GND When the supply voltage is injected, a Power on Reset circuit prevents the PLL from setting the SDA line at Low which would disable the bus.

Absolute Maximum Ratings*

Supply Voltage (V_S) ..... −0.3V to 6V
Output PD (V_1) ..... −0.3V to V_S
Crystal Q1 (V_2) ..... −0.3V to V_S
Crystal Q2 (V_3) ..... −0.3V to V_S
Bus Input/Output SDA (V_4) ..... −0.3V to V_S
Bus Input SCL (V_5) ..... −0.3V to V_S
Port Output P7 (V_6) ..... −0.3V to +16V
Port Output P6 (V_7) ..... −0.3V to +16V
Port Output P5 (V_8) ..... −0.3V to +16V
Port Output P4 (V_9) ..... −0.3V to +16V
Port Output P3 (V_{10}) ..... −0.3V to +16V
Port Output P2 (V_{11}) ..... −0.3V to +16V
Port Output P1 (V_{12}) ..... −0.3V to +16V
Port Output P0 (V_{13}) ..... −0.3V to +16V
Signal Input UHF/VHF (V_{15}) ..... −0.3V to +2.5V
Reference Input REF (V_{16}) ..... −0.3V to +2.5V
Output Active Filter V_D (V_{18}) ..... −0.3V to V_S
Bus Output SDA (I_{4L})
Open Collector ..... −1 mA to +5 mA
Port Output P7 (I_{6L})
Open Collector ..... −1 mA to +5 mA
Port Output P6 (I_{7L})
Open Collector ..... −1 mA to +5 mA

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Port Output P5 (I_{8L})
Open Collector ..... −1 mA to +5 mA
Port Output P4 (I_{9L})
Open Collector ..... −1 mA to +5 mA
Junction Temperature (T_j) ..... 125°C
Storage Temperature
Range (T_{stg}) ..... −40°C to +125°C
Thermal Resistance
System-Air ($R_{th\ SA}$) ..... 80 K/W

Operating Range

Supply Voltage (V_S) ..... 4.5V to 5.5V
Ambient Temperature (T_A) ..... 0°C to 85°C
Input Frequency (f_{15}) ..... 16 MHz to 1300 MHz
Crystal Frequency ($f_{2,3}$) ..... 4 MHz
Divider Factor (N) ..... 256 to 32767

Characteristics V_S = 5V; T_A = 25°C

Parameter	Symbol	Test Circuit	Limits			Units
			Min	Typ	Max	
Current Consumption	I_S	1	35	55	75	mA
Crystal Frequency Series Capacitance 18 pF	$f_{2,3}$*	1			4	MHz
Input Sensitivity UHF/VHF						
f_{15} = 80 ... 500 MHz	a_{15}	2	−27/10		3/315	dBm/*
f_{15} = 500 ... 1000 MHz	a_{15}	2	−24/14		3/315	dBm/*
f_{15} = 1200 MHz	a_{15}	2	−15/40		3/315	dBm/*
Band Selection Outputs P0 ... P3 (current sinks with internal resistance R_i = 12 kΩ)						
Leakage Current, V_{13H} = 13.5V	I_{13H}	3			10	µA
Sink Current, V_{13H} = 12V	I_{13L}	3	0.7	1	1.5	mA
Port Outputs P4 ... P7 (switch with open collector)						
Leakage Current, V_{9H} = 13.5V	I_{9H}	4			10	µA
Residual Voltage, I_{9L} = 1.7 mA	V_{9L}	4			0.3	V

*Listed as mV_{rms} with 50Ω

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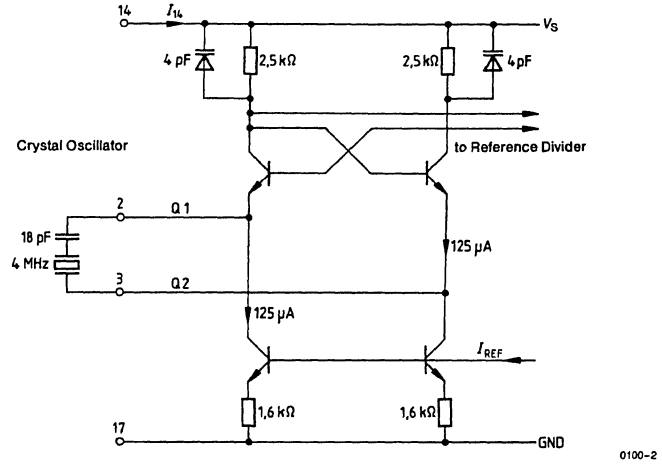
Characteristics V_S = 5V; T_A = 25°C (Continued)

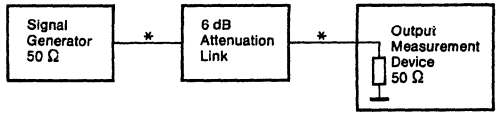
Parameter	Symbol	Test Circuit	Limits			Units
			Min	Typ	Max	
Phase Detector Output PD (V_S = 5V)						
Charge Pump Current 5 I = High; V_1 = 2V	I_{1H}	5	±90	±220	±300	µA
Charge Pump Current 5 I = Low; V_1 = 2V	I_{1H}	5	±22	±50	±75	µA
Output Voltage Locked	V_{IL}	5	1.5		2.5	V
Active Filter Output V_D (Test modus T0 = 1, PD = Tristate)						
Output Current V_{18} = 0.8V; I_{14} = 90 µA	I_{18}	5	500			µA
Output Voltage, V_{1L} = 0V	V_{18}	5			100	mV
Bus Inputs SCL, SDA						
Input Voltage	V_{5H} V_{5L}	6	3		5.5 1.5	V V
Input Current V_{5H} = V_S V_{5L} = 0V	 I_{5L} I_{5L}	 6 6			 50 −100	 µA µA
Output SDA (open collector)						
Output Voltage V_{4H} = 5.5V I_{4L} = 2 mA	 V_{4H} V_{4L}	 6 6			 12 0.4	 V V
Edges SCL, SDA						
Rise Time	t_R	6			15	µs
Fall Time	t_F	6			15	µs
Shift Register Clock Pulse SCL						
Frequency	f_5	6	0		100	KHz
H-Pulse Width	$t_{5\ HIGH}$	6	4			µs
L-Pulse Width	$t_{5\ LOW}$	6	4			µs
Start						
Set-Up Time	t_{SUSTA}	6	4			µs
Hold Time	t_{HDSTA}	6	4			µs
Stop						
Set-Up Time	t_{SUSTO}	6	4			µs
Bus Free Time	t_{BUF}	6	4			µs
Data Transfer						
Set-Up Time	t_{SUDAT}	6	0.3			µs
Hold Time	t_{HDDAT}	6	0			µs

Measurement Circuit 1

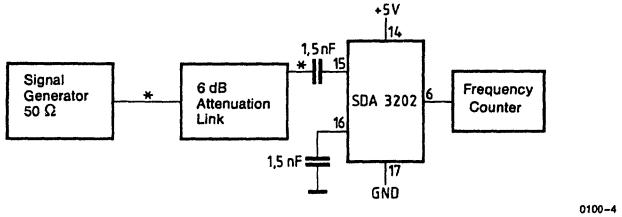


Measurement Circuit 2

Calibration of Signal Generator

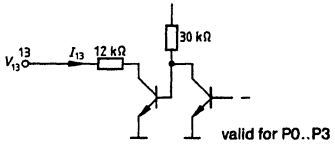


Measurement of Input Sensitivity

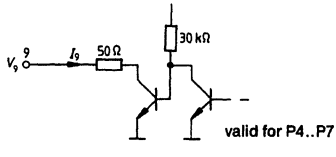


Test mode: T1 = High
* no cable

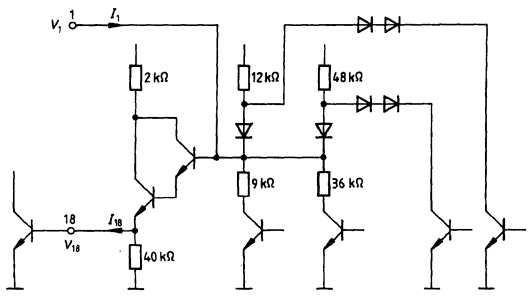
Measurement Circuit 3



Measurement Circuit 4

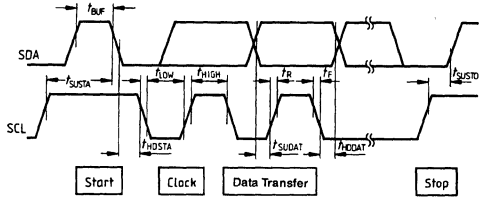


Measurement Circuit 5



Measurement Circuit 6a

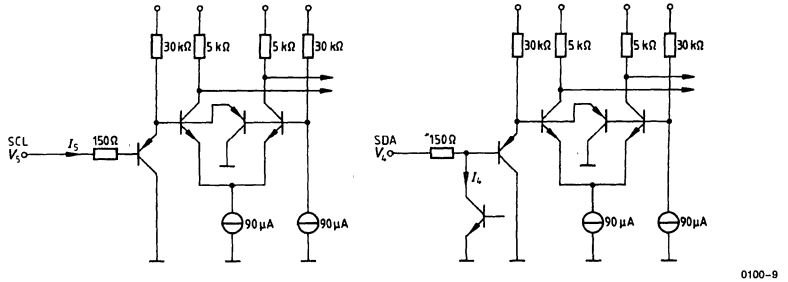
I²C Bus Time Diagram



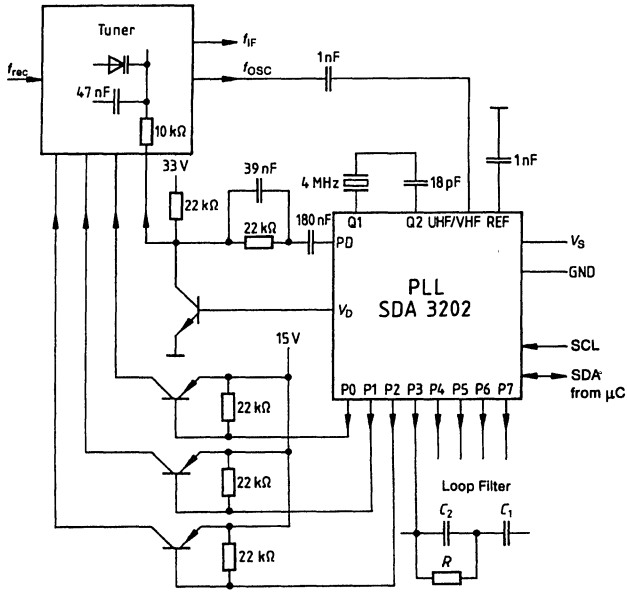
t_{SUSTA}	Set-up time (start)
t_{HDSTA}	Hold time (start)
t_{HIGH}	H-pulse width (clock)
t_{LOW}	L-pulse width (clock)
t_{SUDAT}	Set-up time (Data transfer)
t_{HDDAT}	Hold time (Data transfer)
t_{SUSTO}	Set-up time (Stop)
t_{BUF}	Bus free time
t_F	Fall time
t_R	Rise time

Above times are referenced to V_{IH} and V_{IL} values

Measurement Circuit 6b



Application Circuit



Computation for Loop Filter

Loop bandwidth: $\omega_R = \sqrt{\frac{I_p \times K_{VCO}}{C_1 \times P \times N}}$

Attenuation: $\zeta = 0.5 \times \omega_R \times R \times C_1$

P = Prescaler
N = Progr. divider
I_P = Pump current
K_{VCO} = Tuner slope
R, C_1 = Loop filter

Example for Channel 47

P = 8; N = 11520; I_p = 100 µA;
K_{VCO} = 18.7 MHz/V; R = 22 kΩ;
C_1 = 180 nF; ω_R = 336 Hz;
f_n = 54 Hz; ζ = 0.67

Standard dimensioning: $C_2 = C_{1/5}$

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Description of Function, Application and Circuit

Logic Allocation

	MSB								A = Acknowledge
Address byte	1	1	0	0	0	0	1	0	A
Prog. divider byte 1	0	n14	n13	n12	n11	n10	n9	n8	A
Prog. divider byte 2	n7	n6	n5	n4	n3	n2	n1	n0	A
Control info byte 1	1	5I	T1	T0	1	1	1	0	A
Control info byte 2	P7	P6	P5	P4	P3	P2	P1	P0	A

Divider ratio:

$N = 16384 \times n14 + 8192 \times n13 + 4096 \times n12 + 2048 \times n11 + 1024 \times n10 + 512 \times n9 + 256 \times n8 + 128 \times n7 + 64 \times n6 + 32 \times n5 + 16 \times n4 + 8 \times n3 + 4 \times n2 + 2 \times n1 + n0$

Band selection:

P3 . . . P0 = 1 Current sink is active

Port outputs:

P7 . . . P4 = 1 Open collector output is active

Switch-over of pump current:

5I =1 High current

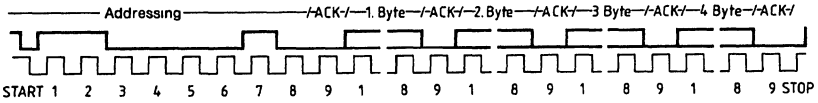
Test Mode:

T1,T0 =0,0 Normal operation

T1 =1 P6 = f_{REF}; P7 = Cy

T0 =1 Tristate charge pump

Pulse Diagram



0100-11

Command Samples

Start-Adr-Tv1-Tv2-St1-St2-Stop
Start-Adr-St1-St2-Tv1-Tv2-Stop
Start-Adr-Tv1-Tv2-St1-Stop
Start-Adr-St1-St2-Tv1-Stop
Start-Adr-Tv1-Tv2-Stop
Start-Adr-St1-St2-Stop
Start-Adr-Tv1-Stop
Start-Adr-St1-Stop

Start = start condition
Adr = addressing
Tv1 = divider ratio 1. byte
Tv2 = divider ratio 2. byte
St1 = control word 1. byte
St2 = control word 2. byte
Stop = stop condition

Ordering Information

Type	Ordering Code	Package
SDA 3202	Q67000-Y904	P-DIP 18

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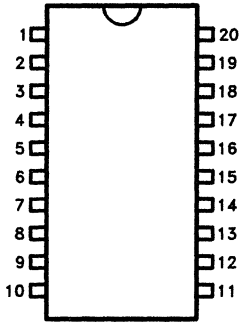
SIEMENS

SDA 3203
1.3 GHz PLL with 3-Wire Bus

- Low Current Consumption
- Command Transmission Via a 3-Wire Bus
- 4 Software-Controlled Outputs
- Cost-Effective and Space-Saving Design
- Prescaler Output Frequency is Free from Interference Radiation

Pin Configuration

Top View



0101-12

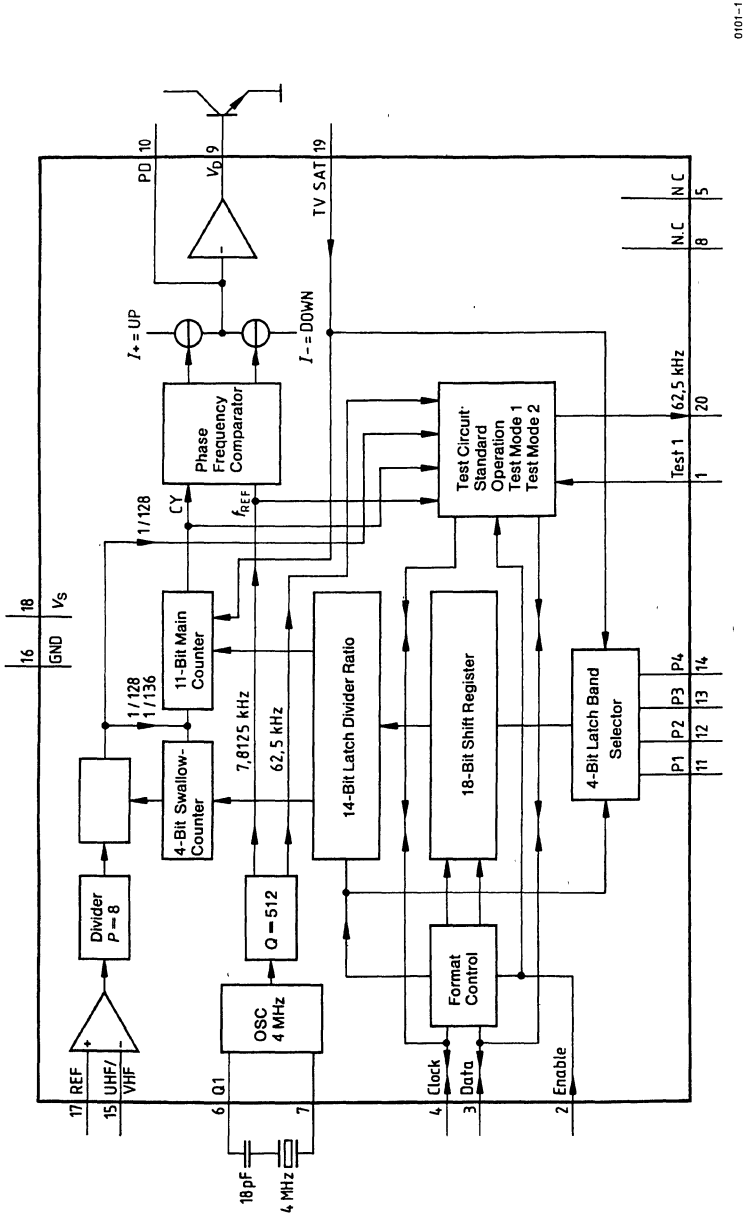
Pin Definitions

Pin	Symbol	Function
1	TEST1	Test Input 1
2	ENABLE	Enable Input—Shift Register
3	DATA	Data Input—Shift Register
4	CLOCK	Clock Input—Shift Register
5	N.C.	Not Connected
6	Q1	Crystal
7	Q2	Crystal
8	N.C.	Not Connected
9	V_D	Auxiliary Output for Active Filter
10	PD	Phase Detector Output
11	P1	Port Output
12	P2	Port Output
13	P3	Port Output
14	P4	Port Output
15	UHF/VHF	Signal Input
16	GND	Ground
17	REF	Amplifier-Reference Input
18	V_S	Supply Voltage
19	TVSAT	Switch-Over TVSAT Range
20	KHz 62.5	62.5 KHz Output/Test Output

Combined with a VCO (tuner), the SDA 3203 comprises a digital programmable phase-locked loop for television devices designed to use the PLL frequency synthesis tuning principle.

The PLL provides a crystal-stable frequency for tuner oscillators between 16 MHz–1300 MHz in the 62.5 KHz raster. By including an external prescaler 1/2, the component can also be used for synthesizing applications of up to 2.4 GHz (e.g. satellite receivers). As a result, the resolution is doubled to 125 KHz. The tuning process is controlled via a 3-wire bus by the microprocessor.

Block Diagram



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Circuit Description

Tuning Section (Refer to Block Diagram)

UHF/VHF The tuner signal is capacitively coupled at the UHF/VHF input and subsequently amplified.

REF The reference input REF should be disabled by a capacitor of low series inductance. The amplified signal passes through an asynchronous divider with a fixed ratio of P = 8. An anti-oscillation circuitry prevents the first divider stage from oscillating when the input signal is missing. As a result, the PLL maintains the correct control direction should the tuner oscillation be terminated. Subsequently, a switchable 16/17 counter is activated. The combination of this counter with a 4-bit and 10-bit programmable counter provides an adjustable divider operating in the dual modulus mode. The 4-bit counter drives the switchover from 17 to 16. Divider ratios of N = 256–16383 are possible. The divided signal is compared in a digital frequency phase detector with a frequency f_{REF} = 7.8125 KHz. This frequency has been derived from a 4 MHz crystal oscillator (pin Q1, Q2 Q1, Q2) by dividing its output signal by Q = 512.

The phase detector includes two outputs UP and DOWN which control the current sources I+ and I− of a charge pump. If the negative edge of the divided VCO signal appears prior to the negative edge of the reference signal, the current source I+ will pulsate for the duration of the phase difference. However, during the reversed sequence of the negative edges, the current source I− will begin to pulsate.

Pd, V_D If both signals are in phase, the charge pump output PD changes into the high impedance state (PLL in lock). An active low pass filter (internal amplifier, external output transistor at V_D, and RC combination) integrates the current pulses as the tuning voltage for the VCO.

P1–P4 The software-controllable outputs P1, P2, P3 and P4 drive the external PNP transistors (internal current limiting) which operate as band selection switch.

TVSAT In the TVSAT mode (pin TVSAT = 0V), the command bit for P1 becomes the 15. Divider bit providing divider ratios of N = 256–32767.

3-Wire Bus Interface (Refer to Description of Functions)

DATA CLOCK ENABLE Via the serial data input DATA the command is read into an 18-bit deep shift register with the positive edge of the CLOCK supplied by the processor when the ENABLE input is also in High. To further ensure the prevention of interference products, a format control discards all commands which exceed eighteen clock pulses during the Enable-High cycle.

Beginning with the MSB, the four band selection control bits for the port outputs and the divider ratio are inserted in binary code. An 18-bit latch accepts the data from the shift register with the negative edge of the Enable pulse.

TEST1 KHz 62.5 During standard operation TEST1 = Low an eight-fold reference frequency 62.5 KHz is present at pin KHz 62.5. During test operation TEST1 = High, a distinction is made between test mode 1 (ENABLE = Low) and test mode 2 (ENABLE = High).

Data	Clock	KHz 62.5	Operating Mode
Shift Data	Shift Clock	62.5 KHz	Standard Operation
Output Progr. Divider	Output Ref. Divider	62.5 KHz	Test Mode 1
Input Phase Detector	Input Phase Detector	1/128 (Fixed)	Test Mode 2
Var. Frequency	Ref. Frequency		

Absolute Maximum Ratings*

Supply Voltage (V_S) ..... −0.3V to +6V
Test Input TEST1 (V_1) ..... −0.3V to V_S
ENABLE (V_2) ..... −0.3V to +6V
DATA (V_3) ..... −0.3V to +6V
(I_3) ..... 3 mA
CLOCK (V_4) ..... −0.3V to +6V
(I_4 ..... 3 mA
Crystal Q1 (V_6) ..... −0.3V to V_S
Crystal Q2 (V_7) ..... −0.3V to V_S
Output Active Filter V_D (V_9) ..... −0.3V to V_S
Output Charge Pump PD (V_{10}) ..... −0.3V to V_S
Port Output P1 (V_{11}) ..... −0.3V to +16V
Port Output P2 (V_{12}) ..... −0.3V to +16V
Port Output P3 (V_{13}) ..... −0.3V to +16V
Port Output P4 (V_{14}) ..... −0.3V to +16V
Signal Input UHF/VHF (V_{15}) ..... −0.3V to +3V

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Reference Input REF (V_{20}) ..... −0.3V to +3V
Output 62.5 KHz (V) ..... −0.3V to V_S
Junction Temperature (T_j) ..... 125°C
Storage Temperature Range (T_{stg}) ..... −40°C to +125°C
Thermal Resistance System-Air ($R_{th\ SA}$) ..... 60 K/W

Operating Range

Supply Voltage (V_S) ..... 4.5V to 5.5V
Ambient Temperature (T_A) ..... 0°C to +70°C
Input Frequency (f_{15}) ..... 16 MHz to 1300 MHz
Crystal Frequency ($f_{6,7}$) ..... 4 MHz
Divider Factor (N) ..... 256 to 32767

Characteristics V_S = 5V; T_A = 25°C

Parameter	Symbol	Test Circuit	Limits			Units
			Min	Typ	Max	
Current Consumption, V_S = 5V	I_S	1	20	50	70	mA
Crystal Frequency Series Capacity 18 pF	$f_{6,7}$	1			4	MHz
Input Sensitivity UHF/VHF						
f_{15} = 80 MHz–100 MHz	a_{15}	2	−24/14		3/315	dBm*
f_{15} = 100 MHz–1000 MHz	a_{15}	2	−27/10		3/315	dBm*
f_{15} = 1300 MHz	a_{15}	2	−15/40		3/315	dBm*
Input DC Voltage UHF/VHF and REF not connected	V_{15}	2		2		
Band Selection Outputs P1–P4 (Current Sinks with Internal Resistance R_I = 12 kΩ)						
Leakage Current, V_{11H} = 13.5V	I_{11H}	3			10	µA
Sink Current, V_{11L} = 12V	I_{11L}	3	0.7	1.0	1.5	mA
Phase Detector Output PD V_S = 5V						
Pump Current Lock In	I_{10}	5	±90	±150	±220	µA
Output Voltage Lock In	V_{10}	5	1.5		2.5	V
Leakage Current Lock In	I_{10}	5	−0.2		0.2	µA
Active Filter Output V_D						
Output Current, V_D = 0.8V	I_9	5	500			µA

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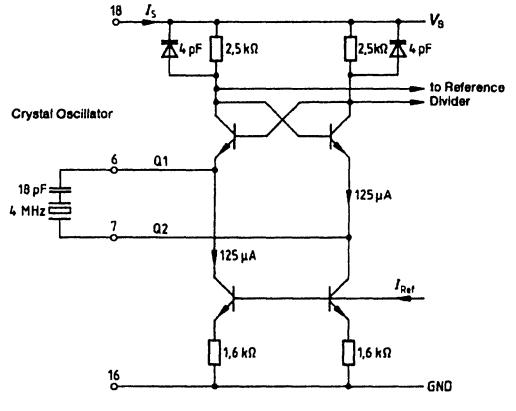
Characteristics $V_S = 5V; T_A = 25°C$ (Continued)

Parameter	Symbol	Test Circuit	Limits			Units
			Min	Typ	Max	
Test Input TEST1						
Input Voltage	V_{1H}	6	3		V_S	V
Input Current $V_{1H} = 5V$ $V_{1L} = 0V$	V_{1L} I_{1H} I_{1L}	6 6 6			0.8 50 −100	V µA µA
Test Output CLOCK, DATA (Open Collector)						
Output Voltage, $I_{2L} = 1$ mA	V_{2L}	6			0.4	V
Leakage Current $V_{2H} = 5V$	V_{2H} I_{2H}	6 6	 10		5.5	V µA
Output 62.5 kHz (Current Sink with Open Collector)						
Output Voltage Output Current	V_{20} I_{20}	4 4	0.4 100		5.5 200	V µA
Bus Input CLOCK, DATA, ENABLE						
Input Voltage	V_{2H} V_{2L}	6 6	3		V_S 0.8	V V
Input Current $V_{2H} = 5V$ $V_{2L} = 0V$	 I_{2H} I_{2L}	 6 6			 50 −100	 µA µA
Data Transfer						
Set-Up Time DATA	t_{SUDAT}	6	2			µs
Hold Time DATA	t_{HDDAT}	6	2			µs
CLOCK						
H-Pulse Width CLOCK	t_{HIGH}	6	2			µs
ENABLE						
Set-Up Time ENABLE	t_{SUEN}	6	2			µs
Hold Time ENABLE	t_{HDEN}	6	2			µs

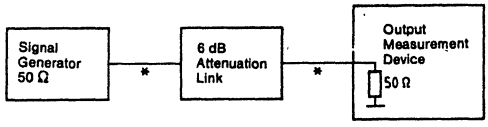
*Listed as mVrms with 50Ω.

Measurement Circuit 1

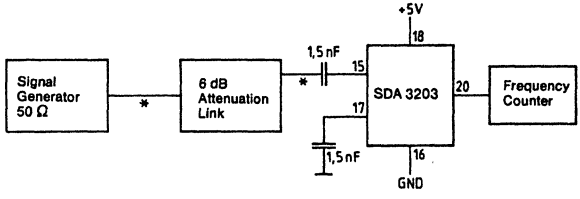


Measurement Circuit 2

Calibration of Signal Generator



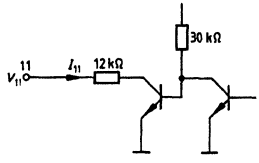
Measurement of Input Sensitivity



Test Mode 2

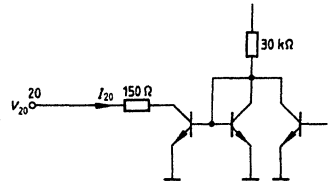
*No Cable

Measurement Circuit 3



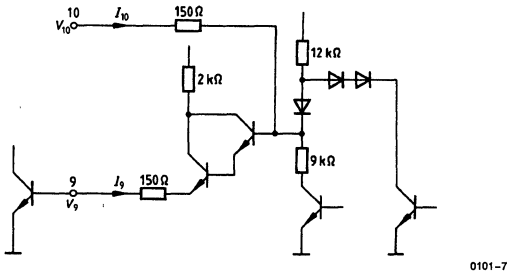
Valid for P1–P4

Measurement Circuit 4



62.5 kHz Output

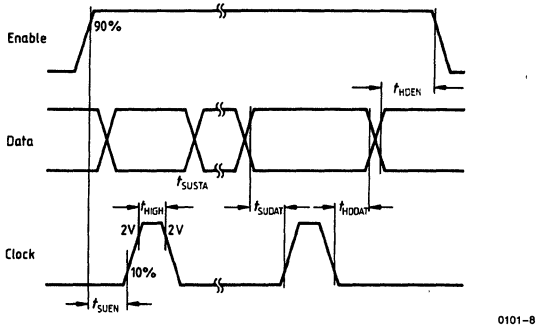
Measurement Circuit 5



Charge Pump Outputs PD, V_D

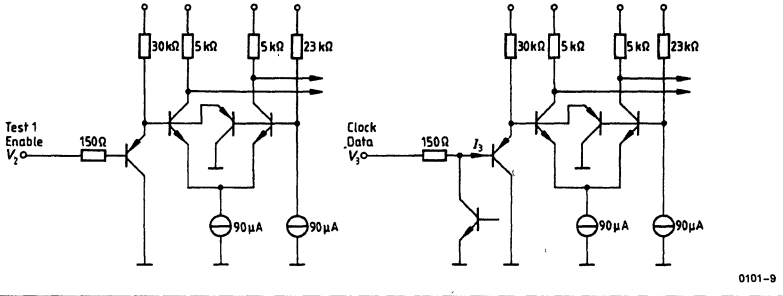
Measurement Circuit 6a

I²C Bus Time Diagram

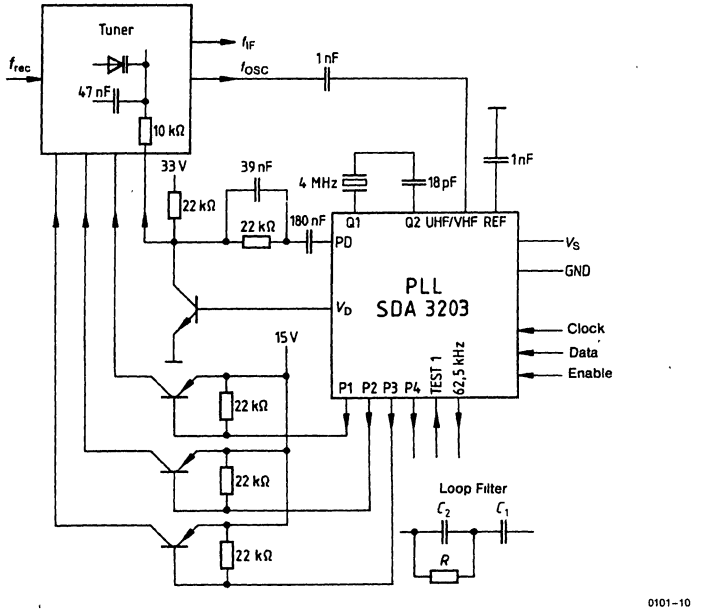


t_{SUEN}	Set-Up Time (Enable)
t_{HDEN}	Hold Time (Enable)
t_{HIGH}	H Pulse Width (Clock)
t_{SUDAT}	Set-Up Time (Data Transfer)
t_{HDDAT}	Hold Time (Data Transfer)

Measurement Circuit 6b



Application Circuit



Computation for Loop Filter

Loop bandwidth: $\omega_R = \sqrt{\frac{I_p \times K_{VCO}}{C_1 \times P \times N}}$

Attenuation: $\xi = 0.5 \times \omega_R \times R \times C_1$

P = Prescaler
N = Progr. Divider
I_P = Pump Current
K_{VCO} = Tuner Slope
R, C_1 = Loop Filter

Example for Channel 47

P = 8; N = 11520; I_p = 100 µA;
K_{VCO} = 18.7 MHz/V; R = 22 kΩ;
C_1 = 180 nF; ω_R = 336 Hz;
f_n = 54 Hz; ξ = 0.67

Standard Dimensioning: $C_2 = C_{1/5}$

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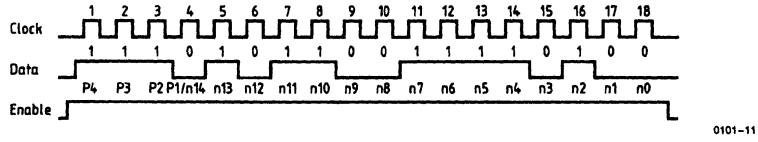
Pulse Diagram



Divider Ratio $N = n13 \times 8192 + n12 \times 4096 + n11 \times 2048 + n10 \times 1024 + n9 \times 512 + n8 \times 256 + n7 \times 128 + n6 \times 64 + n5 \times 32 + n4 \times 16 + n3 \times 8 + n2 \times 4 + n1 \times 2 + n0$

Example: $N = 11508$

Band Selection P1–P4 = 1 Current Sinks are Active

VCO (Tuner) Frequency $f_{VCO} = 8 \times N \times 7.8125$ KHz

Example: $f_{VCO} = 719.25$ MHz

TVSAT = N.C. Bit 4 is P1

TVSAT = 0V Bit 4 is n14

Ordering Information

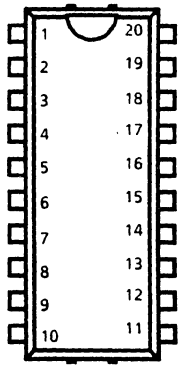
Type	Ordering Code	Package
SDA 3203	Q67000-A2526	P-DIP 20

Preliminary

SDA 3252
1.3 GHz-PLL with Digital Tuner Alignment

Pin Configuration

(Top View)



0098-2

Pin Definitions

Pin	Function
1	Supply Voltage V_{S2} (5V)
2	Signal Input RF
3	Band Selection Output BW1
4	Band Selection Output BW2
5	Band Selection Output BW3
6	Phase Detector Output PD
7	Tuning Output V_{D3}
8	Output Active Filter V_D
9	Tuning Output V_{D2}
10	Tuning Output V_{D1}
11	Supply Voltage V_{S1} (33V)
12	Bus Input/Output SDA
13	Bus Input SCL
14	Crystal Q2
15	Crystal Q1
16	Port Output P0
17	Port Output P1
18	Port Output P2
19	Port Output P3
20	Ground (GND)

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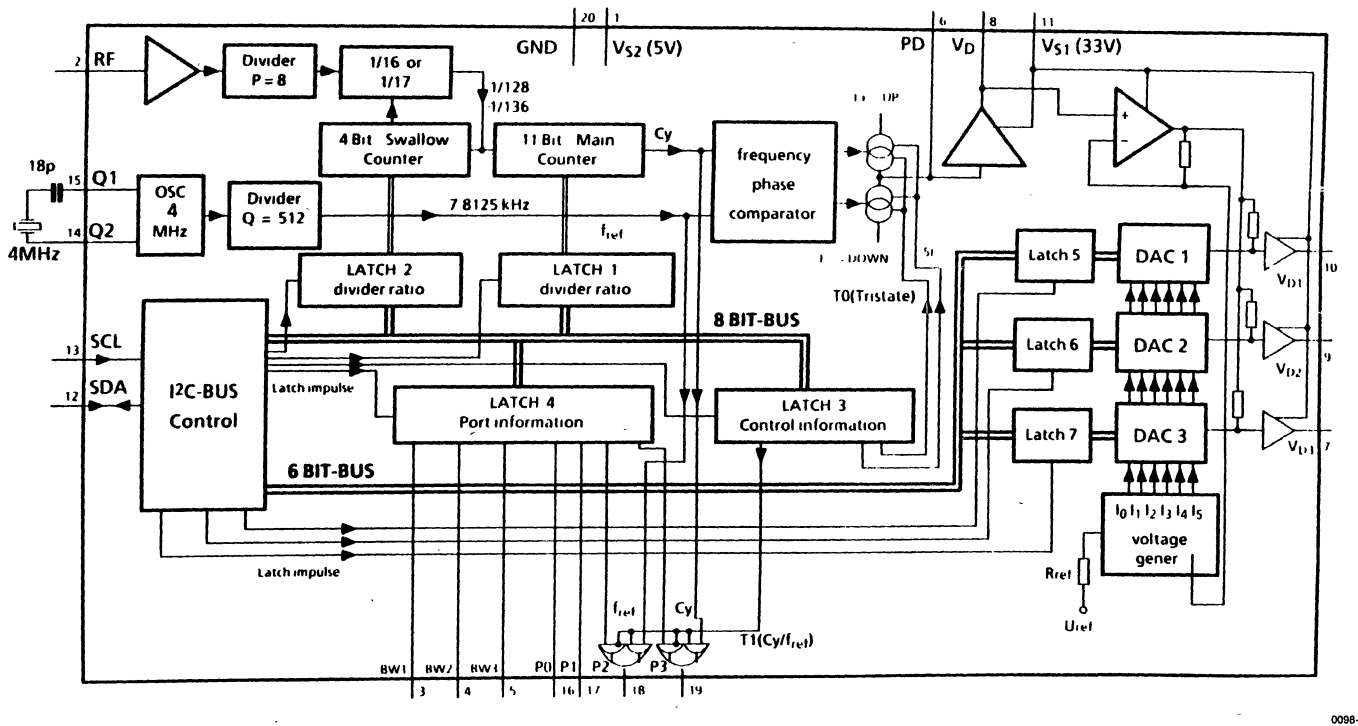
Combined with a VCO (tuner), the SDA 3252 comprises a digital programmable phase looked loop for television devices designed to use the PLL frequency synthesis tuning principle.

The PLL provides:

- The tuner oscillator with a crystal-stable frequency between 16 MHz–1300 MHz providing a 62.5 KHz raster, as well as a 2.4 GHz pre-scaler 1:2 for TVSAT applications, providing in this case a 125 KHz raster

SDA3252 Block Diagram



Description of Functions, Applications and Circuitry

Functions and Applications

Combined with a VCO (tuner), the SDA 3252 comprises a digital programmable phase-locked loop for television devices designed to use the PLL frequency synthesis tuning principle.

The PLL provides the tuner oscillator with a crystal-stable frequency between 16 MHz–1300 MHz providing a 62.5 KHz raster, as well as with a 2.4 GHz prescaler 1:2 in the TVSAT range, providing in this case a 125 KHz raster. The three outputs V_{D1}, V_{D2}, and V_{D3} control the vector diodes of the circuitry. These tuning voltages differ from the oscillator tuning voltages by a programmable amount. The tuning process as well as the difference between the tuning voltages are controlled by a microprocessor via an I²C bus.

Operating voltage V_S = 5V.

Description of Circuitry

Tuning Section (See Block Diagram)

RF — The tuner signal is capacitively coupled at the RF input and amplified. Subsequently, the signal passes through an asynchronous divider with a fixed ratio of P = 8, and an adjustable divider N = 2546 ... 32767. The signal is then compared in a digital frequency phase detector with a reference frequency f_{ref} = 7.8125 KHz. This frequency has been derived from a 4 MHz crystal

Q_1, Q_2 — oscillator (Pin Q_1, Q_2) by dividing its output signal by Q = 512.

The phase detector includes two outputs UP and DOWN which control the two current sources I+ and I− of a charge pump. If the negative edge of the divided VC signal occurs prior to the negative edge of the reference signal, the current source I+ will pulsate for the duration of the phase difference. However, during the reversed sequence of the negative edges, current source I− will begin to pulsate. If both signals are in phase, the charge pump output PD changes into the high-impedance state (PLL in lock). An active low pass filter (internal amplifier, external

PD, V_D — output transistor at VD, and RC combination) integrates the current pulses as the tuning voltage for the VCO.

With the control bit 5I the pump current can be switched between two values per software. Through this switch-over, the control characteristics of the PLL during lock in can be changed, i.e., varying tuner characteristics in the various TV bands can be adjust.

BW1 ... BW3 — The software-controllable band selection outputs BW1, BW2 and BW3 can drive external PNP transistors operating as band selection switch (internal current limiting).

P0 ... P3 — P0, P1 and P3 are open collector output which can be used for a variety of applications.

V_{D1}, V_{D2}, V_{D3} — The circuitry for the digital tuner alignment includes three digital-to-analog converters and a logic circuit which can store three 8-bit information. Six of these bits are forwarded to one digital-to-analog converter each. The three output magnitudes are added to the tuning voltage V_D.

I²C-BUS-Interface

The PLL (output VD) and the alignment of the tuner circuitry (outputs V_{D1}, V_{D2}, and V_{D3}) are accessed via two separate addressed which are injected via common interface SCL, SDA.

Data bytes can be read in any number and order after the respective address bytes input for PLL-tuning function or for digital tuner alignment.

I²C-BUS-Interface for PLL-Tuning Section (Outputs, V_{D1}, V_{D2}, and V_{D3})

SCL, SDA — The processor and the PLL exchange information via an asynchronous, bi-directional data bus. The clock is always supplied by the processor (input SCL). Pin SDA operates as input or output depending on the direction of the data stream (open collector, external pull-up resistor).

The data from the processor passes through an I²C bus control. Depending on their function, the data are subsequently latched in registers 0–3. If the bus is not in the busy state, both lines are in the marking

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state (SDA, SCL are high). Each telegram begins with the start conditions of SDA returning to LOW, while SCL remains in HIGH. All additional information is transferred during SCL = LOW, and the data is forwarded to the control with the positive clock edge. However, if SDA returns to HIGH, while SCL is in HIGH, the telegram is ended since the PLL acknowledges a stop condition.

In what follows the "logical allocation" table is used as basis.

All telegrams are transmitted byte-by-byte, followed by a 9th clock pulse, while the control returns the SDA line to LOW (acknowledge condition). The first byte comprises 7 address bits. These are used by the processor to select the PLL from several peripheral components (chip-select). The 8th bit is always LOW. In the data portion of the telegram, the first bit of the first or third data byte determines whether a divider ratio or a control information is to follow. In each case, the second byte of the same data type or a stop condition has to follow the first byte.

I²C-BUS-Interface for Digital Tuner Alignment (Outputs V_{D1}, V_{D2}, and V_{D3})

Each data transfer begins with a START condition: SDA goes to LOW, while SCL remains HIGH.

The data is accepted with a positive clock edge and transferred byte-by-byte. Each byte requires nine clock pulses. During the first eight pulses, the data is transferred, and during the ninth clock pulses the addressed component generates an acknowledge signal (ACK). (The SDA line is returned to LOW.) The first byte after a start condition contains the component address.

The subsequent bytes contain the sub-addresses for the three digital-to-analog converters (D7, D6) and the 6-bit information which determines the (analog) voltage value (D5 ... D0). The data transfer is ended with the STOP condition. SDA goes to HIGH, while SCL remains in LOW. Subsequently, SCL returns to HIGH as well.

V_{S2}, GND — A POWER ON RESET circuitry prevents SDA from going into LOW and blocking the bus, when the supply voltage V_{S2} is injected.

Description of Functions, Applications and Circuitry

Logical Allocation—PLL Alignment

	MSB							LSB	
Address Byte	1	1	0	0	0	0	1	0	ACK
Prog. Divider Byte 1	0	n14	n13	n12	n11	n10	n9	n8	ACK
Prog. Divider Byte 2	n7	n6	n5	n4	n3	n2	n1	n0	ACK
Control Info. Byte 1	1	5I	T1	T0	1	1	1	0	ACK
Control Info. Byte 2	P3	P2	P1	P0	X	BW3	BW2	BW1	ACK

Divider Ratio:

$$N = 16384*n14 + 8192*n13 + 4096*n12 + 2048*n11 + 1024*n10 + 512*n9 + 256*n8 + 128*n7 + 64*n6 + 32*n5 + 16*n4 + 8*n3 + 4*n2 + 2*n1 + n0$$

Description of Functions, Applications and Circuitry (Continued)

Band Selection:
BW1 . . . BW3 = 1 Current Sink is Active

Port Outputs:
P3 . . . P0 = 1 Open Collector Output is Active

Pump Current Switch-Over:
5I = 1 High Current

Test Mode:
T1, T0 = 0,0 Standard Operation
T1 = 1 P2 = fref; P3 = Cy
T0 = 1 TRI-STATE Charge Pump

	MSB							LSB	
Address Byte	1	1	0	0	0	0	0	0	ACK
	.....			Address	.....			R/W	

Data Byte	D7	D6	D5	D4	D3	D2	D1	D0	ACK
	•	•							Offset-
	•	•							Spg./V
	•	•							
	•	•	0	0	0	0	0	0	−2.650
	•	•	0	0	0	0	0	1	−2.566
	•	•							
	•	•				etc.			
	•	•							
	•	•							
	•	•	0	1	1	1	1	1	−0.084
	•	•	1	0	0	0	0	0	0.000
	•	•	1	0	0	0	0	0	+0.084
	•	•							
	•	•							
	•	•				etc.			
	•	•							
	•	•							
	•	•	1	1	1	1	1	1	+2.566
	•	•	.....						
	0	0				D/A-Converter 1			
	0	1				D/A-Converter 2			
	1	0				D/A-Converter 3			
	1	1	X	X	X	X	X	X	

7

Absolute Maximum Ratings*

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Operating Range T_U = 25°C

Pos	Parameter	Symbol	Min	Max	Units	Remarks
1	Supply Voltage 1	V_{S1}	−0.3	+36	V	
2	Supply Voltage 2	V_{S2}	−0.3	+6	V	
3	Output PD	V_{PD}	−0.3	V_{S2}	V	
4	Crystal Q_1	V_{Q1}	−0.3	V_{S2}	V	
5	Crystal Q_2	V_{Q2}	−0.3	V_{S2}	V	
6	Bus I/O SDA	V_{SDA}	−0.3	+6	V	
7	Bus Input SCL	V_{SCL}	−0.3	+6	V	
8	Port Input P3	V_{P3}	−0.3	+16	V	
9	Port Input P2	V_{P2}	−0.3	+16	V	
10	Port Input P1	V_{P1}	−0.3	+16	V	
11	Port Input P0	V_{P0}	−0.3	+16	V	
12	Band Selection BW3	V_{BW3}	−0.3	+16	V	
13	Band Selection BW2	V_{BW2}	−0.3	+16	V	
14	Band Selection BW1	V_{BW1}	−0.3	+16	V	
15	Signal Input RF	V_{HF}	−0.3	+2.5	V	
16	Output Active Filter V_D	V_{VD}	−0.3	V_{S1}	V	
17	Output $V_{D1} \ldots V_{D3}$	V_{VD1}, U_{VD2}, U_{VD3}	−0.3	V_{S1}	V	
18	Bus Output SDA	I_{SDAL}	−1	+5	mA	Open Collector
19	Port Output P3	I_{P3L}	−1	+5	mA	Open Collector
20	Port Output P2	I_{P2L}	−1	+5	mA	Open Collector
21	Port Output P1	I_{P1L}	−1	+5	mA	Open Collector
22	Port Output P0	I_{P0L}	−1	+5	mA	Open Collector
23	Output Current	$I(V_{D1, 2, 3})$		1	mA	(Short Circuit)
24	Chip Temperature	(T_C)		+125	°C	
25	Storage Temperature Thermal Resistance:	T_S	−40	+125	°C	
26	System-Air	(R_{thSU})		56	K/W	

Functional Range

Within the function range integrated circuit operates as described; derivations from the characteristic data are possible

Pos	Functional Range	Symbol	Conditions	Limits		Units
				Min	Max	
1	Supply Voltage 1	V_{S1}		+31.5	+36	V
2	Supply Voltage 2	V_{S2}		+4.5	+5.5	V
3	Ambient Temperature	T_{amb}		0	+70	°C
4	Input Frequency	f_{RF}		16	1300	MHz
5	Crystal Frequency	$f_{Crystal}$			4	MHz
6	Divider Factor	N		256	32767	—

Characteristics

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not stated otherwise, typical characteristics will be apply at T_{amb} = 25°C and mean supply voltage.

Characteristics of the Operating Range: V_{S1} = 33V, V_{S2} = 5V, T_C = 25°C

Pos	Parameter	Symbol	Conditions	Test	Limits			Units
					Min	Typ	Max	
1	Current Consumption 1	I_{S1}		5		4		mA
2	Current Consumption 2	I_{S2}		2		60		mA
3	Output Voltage	V_D, $V_{D1,2,3}$		5	0.3		27.5	V
4	Tuning Voltage **See Definition 1	$\Delta V_{D1,2,3}$		5	±2.5	±2.65	±2.8	V
5	Temperature Deviation of Tuning Voltage in Temperature Range **See Definition 2			5	−60		+60	mV
6	Crystal Frequency	$f_{Crystal}$	Series Capacity 18 pF	2			4	MHz
Input Sensitivity								
7		a_{RF}	f_{RF} = 80 MHz–500 MHz	1	−27/10		3/315	dBm/*
8		a_{RF}	f_{RF} = 500 MHz–1000 MHz	1	−24/14		3/315	dBm/*
9		a_{RF}	f_{RF} = 1200 MHz	1	−15/40		3/315	dBm/*
Band Selection BW1–BW3 (Current Sink with Internal Resistance RI = 12k)								
10	Leakage Current	I_{BW}	V_{BW} = 13.5V	3			10	µA
11	Sink Current	I_{BW}	V_{BW} = 12V	3	0.7	1	1.5	mA
Port Outputs P0–P3 (Switch with Open Collector)								
12	Leakage Current	I_{P1H}	U_{P1H} = 13.5V	4			10	µA
13	Residual Voltage	V_{P1L}	I_{P1L} = 1.7 mA	4			0.5	V
Phase Detector Output PD (V_S = 5V)								
14	Pump Current	I_{PDH}	5I = HIGH; V_{PD} = 2V	5	±90	±220	±300	µA
15	Pump Current	I_{PDH}	5I = LOW; V_{PD} = 2V	5	±22	±50	±75	µA
16	Output Voltage	V_{PDL}	Lockin	5	1.5		2.5	V
Bus Inputs SCL, SDA								
20	Input Voltage	V_{SCLH}		6	3		5.5	V
21		V_{SCLL}		6			1.5	V
22	Input Current	I_{SCLH}	V_{SCLH} = U_{S2}	6			50	µA
23		I_{SCLL}	V_{SCLL} = 0V	6			−100	µA
Output SDA (Open Collector)								
24	Output Voltage	I_{SDAH}	V_{SDAH} = 5.5V	6			10	µA
25		V_{SDAL}	I_{SDAL} = 2 mA	6			0.4	V
Edges SCL, SDA								
26	Rise Time	T_R		6			1	µs
27	Fall Time	T_F		6			0.3	µs

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Characteristics (Continued)

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not stated otherwise, typical characteristics will be applied at T_{amb} = 25°C and mean supply voltage.

Characteristics of the Operating Range: V_{S1} = 33V, V_{S2} = 5V, T_C = 25°C

Pos	Parameter	Symbol	Conditions	Test	Limits			Units
					Min	Typ	Max	
Shift Register Clock SCL								
28	Frequency	f_{SCL}		6	0		100	KHz
29	H-Pulse Width	T_{HIGH}		6	4			µs
30	L-Pulse Width	T_{LOW}		6	4			µs
Start								
31	Set-Up Time	T_{SUSTA}		6	4			µs
32	Hold Time	T_{HDSTA}		6	4			µs
Stop								
33	Set-Up Time	T_{SUSTO}		6	4			µs
34	T_{off} Time	T_{BUF}		6	4			µs
Data Transfer								
35	Set-Up Time	T_{SUDAT}		6	0.3			µs
36	Hold Time	T_{HDDAT}		6	0			µs

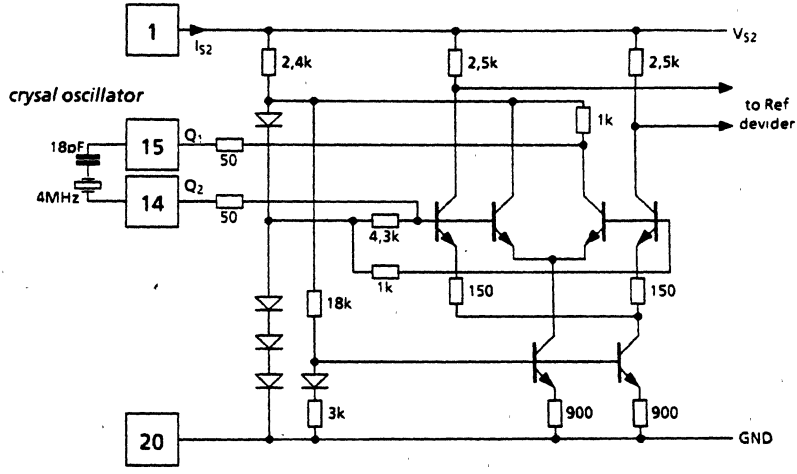
Definition 1: $\Delta V_{D1} = V_{D1} - V_D$
$\Delta V_{D2} = V_{D2} - V_D$
$\Delta V_{D3} = V_{D3} - V_D$

Definition 2: Reference Voltage $V_{D1, 2, 3}$ @ 25°C

*Unit in mVrms @ 50Ω

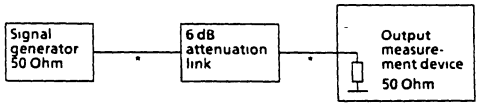
**Not more than 1 driver will be driven simultaneously.

Internal Circuit (Crystal Oscillator)

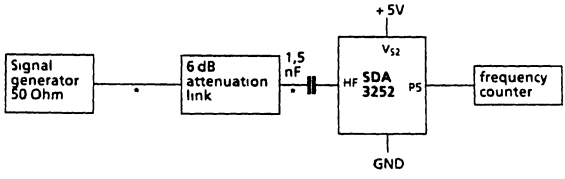


Measurement Circuit 1

Signal Generator Calibration



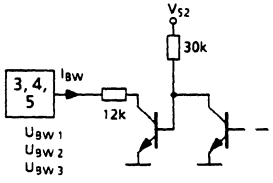
Input Sensitivity Measurement



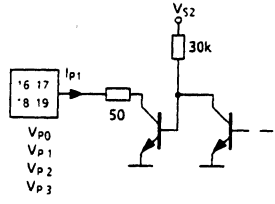
Test Mode: T1 = HIGH

*without cable.

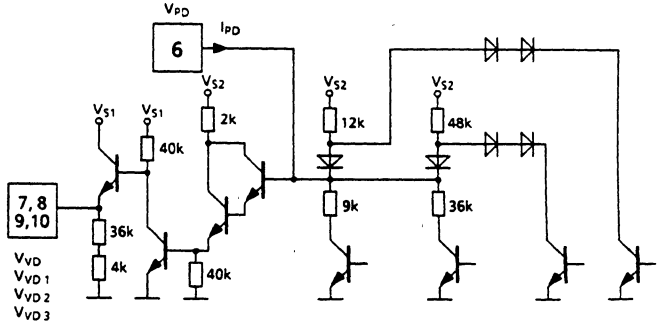
Internal Circuit (Band Selection BW1, BW2, BW3)



Internal Circuit 4 (Port Output P0, P1, P2, P3)



Internal Circuit 5 (Outputs PD, V_D, $V_{D1, 2, 3}$)



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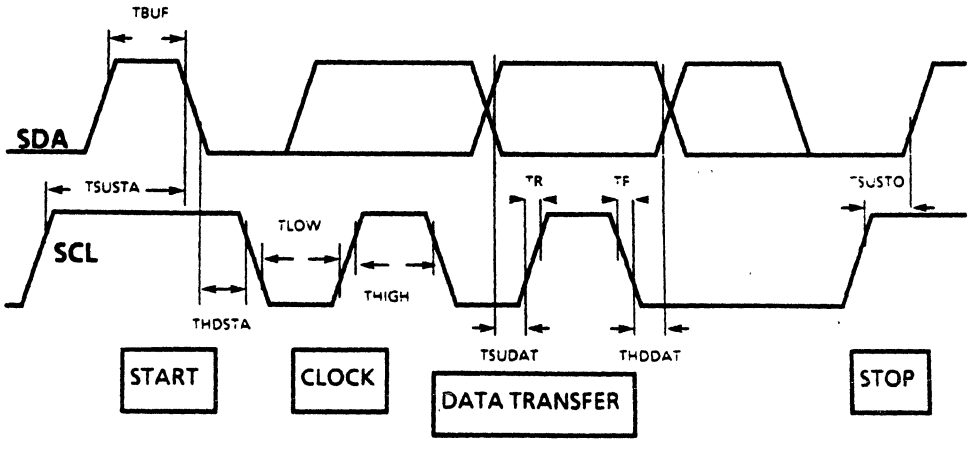
Internal Circuit (Bus Input SDA, SCL)

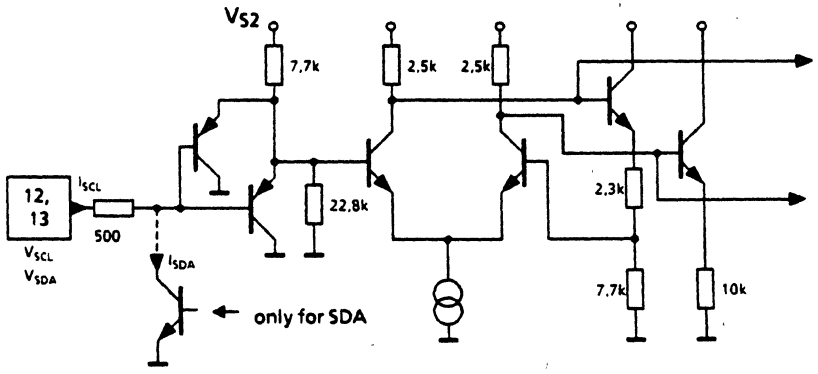
I²C-BUS-Time Diagram



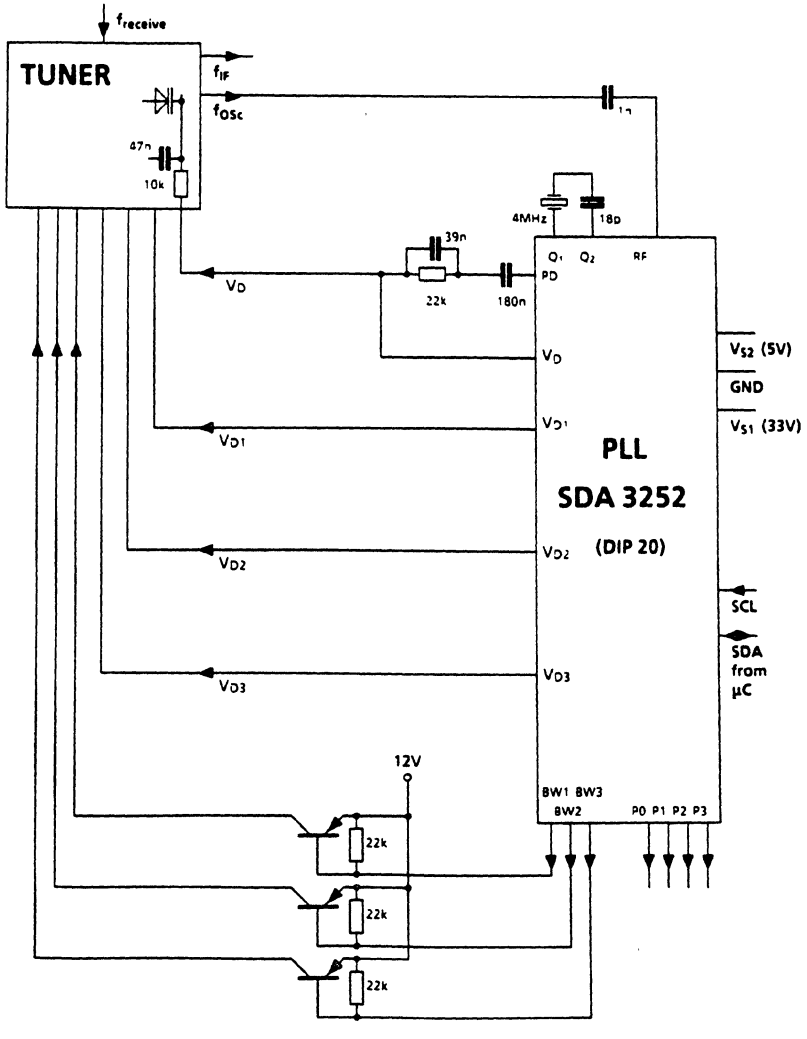
TSUSTA	Setup Time (Start)
THDSTA	Hold Time (Start)
THIGH	H-Pulse Width (Clock)
TLOW	L-Pulse Width (Clock)
TSUDAT	Set-Up Time (Data Transfer)
THDDAT	Hold Time (Data Transfer)
TSUSTO	Set-Up Time (Stop)
TBUF	T_{Off} Time
TF	Fall Time
TR	Rise Time

Above times are referenced to V_{IH} and V_{IL} values.

SCL, SDA

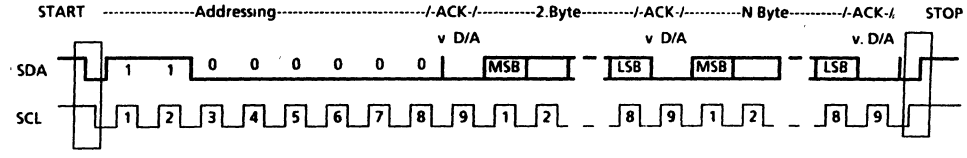


Application Circuit

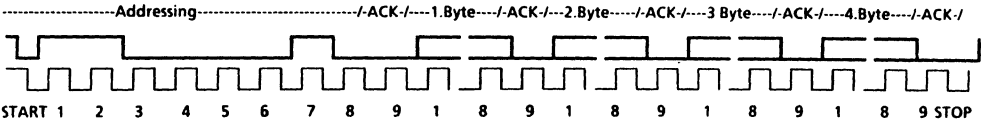


Tuner Section Pulse Diagram

Telegram Samples



0098-11



0098-12

Telegram Samples

Start-Adr-Tv1-Tv2-St1-St2-Stop
Start-Adr-St1-St2-Tv1-Tv2-Stop
Start-Adr-Tv1-Tv2-St1-Stop
Start-Adr-St1-St2-Tv1-Stop
Start-Adr-Tv1-Tv2-Stop
Start-Adr-St1-St2-Stop
Start-Adr-Tv1-Stop
Start-Adr-St1-Stop

Start = Start Conditions
Adr = Addressing
Tv1 = Divider Ratio 1 Byte
Tv2 = Divider Ratio 2 Byte
St1 = Control Word 1 Byte
St2 = Control Word 2 Byte
Stop = Stop Conditions

Ordering Information

Type	Order-Nr.	Package
SDA 3252	Q67000-A8039	DIP 20

SIEMENS

SDA 4212
Divider 1:64 / 1:256 up to 1.3 GHz

Preliminary Data

Type	Ordering code	Package
SDA 4212	Q67000-A8049	P-DIP 8

The SDA 4212 has been designed for application in television receivers operating according to the frequency synthesis tuning principle. It includes a preamplifier and an ECL divider stage with symmetrical ECL push-pull outputs. It can be operated with a divider ratio of 1:64 or 1:256.

The operating range of the IC extends to an input frequency of 1.3 GHz.

Features

- Pin programmable divider ratio of 1:64 or 1:256
- Symmetrical push-pull input
- Low harmonic wave
- Minimal current consumption of 23 mA

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Circuit Description

The preamplifier of the component has been designed with symmetrical push-pull inputs. During the asymmetrical drive of one of the inputs, the other input has to be disabled to ground by a capacitor (approx. 1.5 nF) of low series inductance.

The divider stage of the component is comprised of several status-controlled master-slave flipflops. Their divider ratio can be set with the switch-over input M as follows:

M to V_S = 1:64
M to ground = 1:256

The symmetrical push-pull outputs of the divider include an internal resistor of 500 Ω each. The DC voltage level at the outputs is connected to the supply voltage V_S (output "High" = V_S). The typical voltage swing is 1.0 V (peak-to-peak).

Maximum Ratings

		min	max	Unit
Supply voltage	V_S	−0.3	6	V
Input voltage (peak-to-peak) (pin 2, pin 3)	V_i		2.5	V
Output voltage (pin 6, pin 7)	V_q		V_S	V
Output current (pin 6, pin 7)	$-I_q$		10	mA
Input voltage (pin 5)	V_M	−0.3	V_S	V
Junction temperature	T_j		125	°C
Storage temperature range	T_{stg}	−55	125	°C
Thermal resistance System-air	$R_{th\,SA}$		115	K/W
Overload resistance[1] (ESD protection single discharge of 220 pF capacitor through a 1 kΩ resistor to each pin)	V_{MOS}	−600	1000	V

Operating Range

Supply voltage	V_S	4.5	5.5	V
Input frequency	f_i	70	1300	MHz
Ambient temperature	T_A	0	70	°C

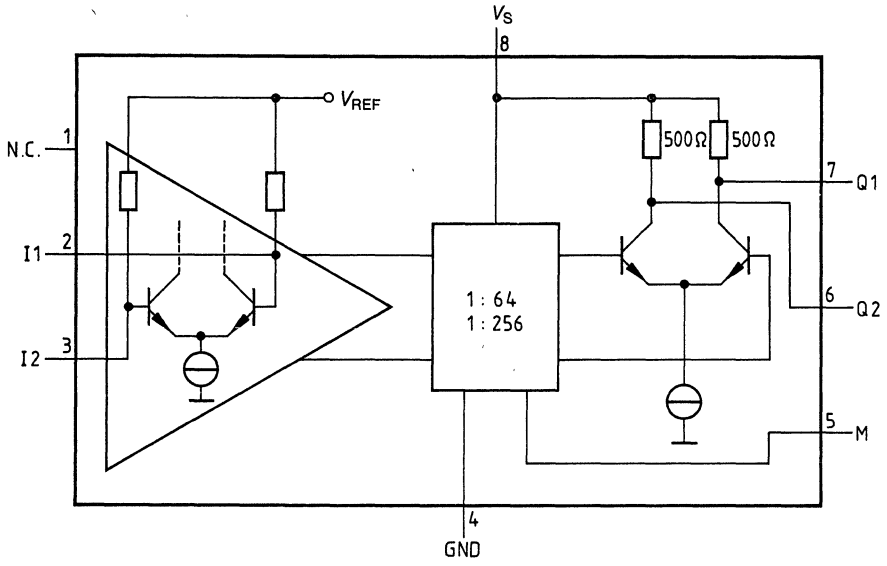
[1] not required pins float; pin 4 always to ground

Characterics

$V_S = 5$ V; $T_A = 25$ °C

		Test circuit	min	typ	max	Unit
Current consumption inputs decoupled outputs enabled; M enabled	I_S			23.5	29.5	mA
Input level ("input sensitivity")	V_i					
70 MHz		1	−26/11		3/315	dBm/mV
80 MHz		1	−27/10		3/315	dBm/mV
120 MHz		1	−30/7		3/315	dBm/mV
250 MHz		1	−32/5.5		3/315	dBm/mV
600 MHz		1	−27/10		3/315	dBm/mV
1000 MHz		1	−27/10		3/315	dBm/mV
1100 MHz		1	−22/18		3/315	dBm/mV
1200 MHz		1	−15/40		3/315	dBm/mV
1300 MHz		1	− 9/80		3/315	dBm/mV
Output voltage swing (peak-to-peak) $C_L \leq 15$ pF; $f \leq 1000$ MHz	V_q	1	0.4	0.6		V
DC voltage offset of outputs	ΔV_q	3			100	mV
M-input current "Low" (divider ratio 1:256) M = ground	I_M	1		2	100	µA
M-input current "High" (divider ratio 1:64) M = V_S	I_M	1		0	50	µA
M-input voltage "High"	V_{MH}	1	3			V
M-input voltage "Low"	V_{ML}	1			0.2	V
Amplitude of the 3rd harmonic at output (referenced to 1st harmonic) $f = 700 \ldots 900$ MHz; M=V_S	a_3	1.4 2.4		−30 −35		dB dB

Block Diagram

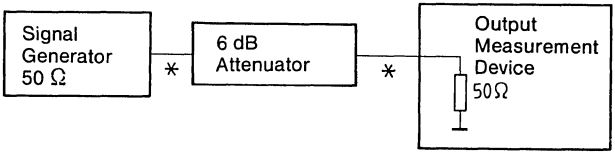


Pin Definitions

Pin	Function
1	Not connected
2	Input I1
3	Input I2
4	Ground
5	Switch-over input M for divider ratio
6	Output Q2
7	Output Q1
8	Supply voltage V_S

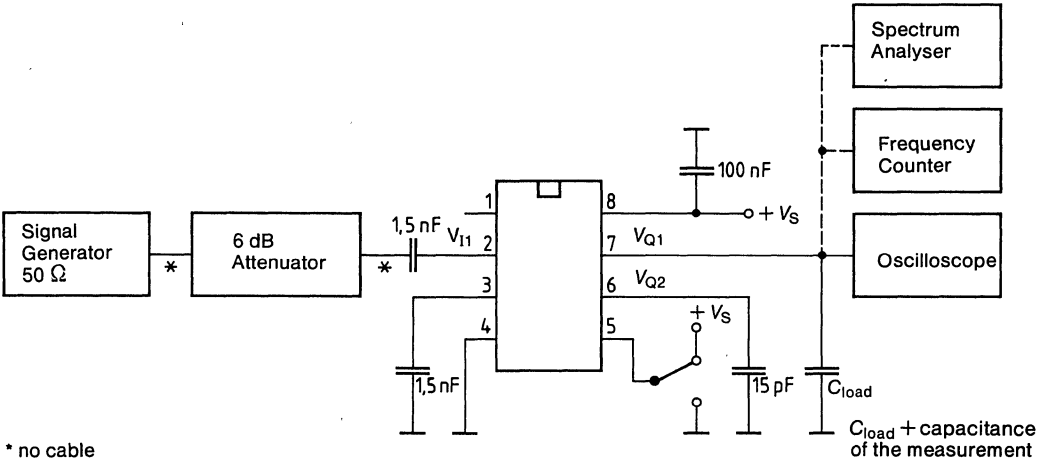
Measurement Circuit 1

Calibration of Signal Generator



* no cable

Measurement of Input Sensitivity and Output Voltage Swing



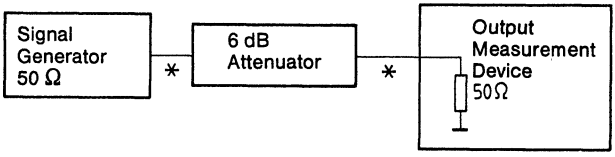
* no cable

C_{load} + capacitance of the measurement devices = 15 pF (For output voltage swing measurement)

7

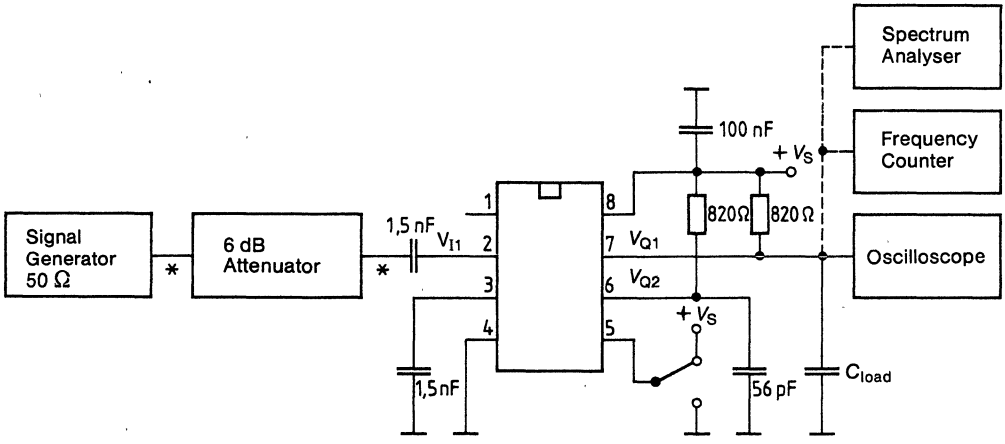
Measurement Circuit 2

Calibration of Signal Generator



* no cable

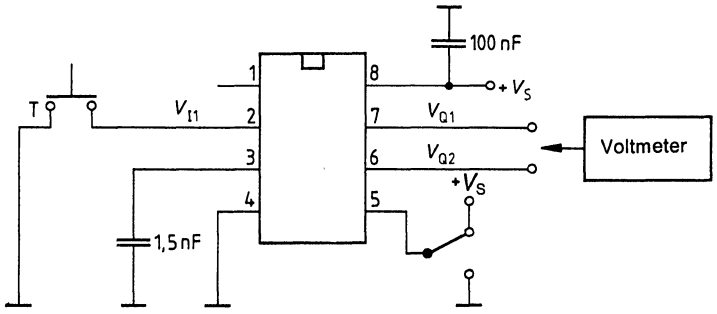
Measurement of Input Sensitivity and Output Voltage Swing



no cable

C_{load} + capacities of the measurement devices = 56 pF (for output voltage swing measurement)

Measurement Circuit 3

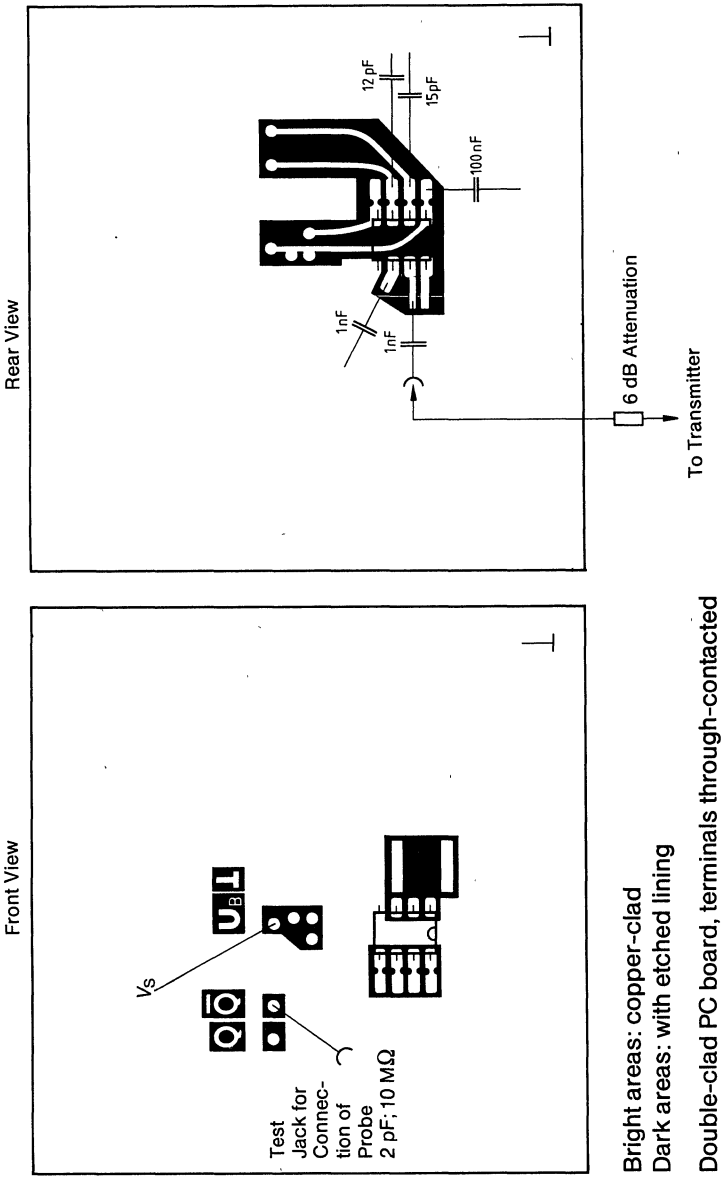


Note: press key T until outputs turn over

7

Measurement Circuit 4

PC Board of Measurement of 3rd Harmonic



Bright areas: copper-clad
Dark areas: with etched lining

Double-clad PC board, terminals through-contacted

TDA 4282 T
Quasi-Parallel Sound IC with FM IF, Sym. Input and Volume Control

The TDA 4282 T is a controlled AM amplifier with FM demodulator (to produce an intercarrier) and subsequent sound-IF limiting amplifier with coincidence demodulator, standard VCR connection and separate AF-output with volume control.

- Outstanding limiting qualities
- Connection for video recorder
- Little external circuitry

Maximum ratings

Supply voltage	V_S	15	V
$t \leq 1$ min	V_S	16.5	V
Thermal resistance (system-ambient air)	$R_{th\ SA}$	65	K/W
Junction temperature	T_j	150	°C
Storage temperature	T_{stg}	−40 to 125	°C

Operational range

Supply voltage	V_S	11 to 15	V
Frequency range AM part	f_{AM}	10 to 60	MHz
FM part	f_{FM}	0.01 to 12	MHz
Control voltage AM part	V_2	0 to 5	V
Switch current FM part	I_8	0.3 to 1	mA
Ambient temperature in operation	T_{amb}	0 to 60	°C

Characteristics (V_S = 15 V, T_{amb} = 25°C)

		min	typ	max	
Current consumption	I_5		60	80	mA
AM-part:					
AGC-range	ΔG		55		dB
AGC-voltage	V_2	0		5	V
Input resistance	$R_{i\,3\text{-}4}$		10		kΩ
Input impedance at max. gain	$Z_{i\,20\text{-}21}$		1.8/2		kΩ/pF
at min. gain	$Z_{i\,20\text{-}21}$		1.9/0		kΩ/pF
Output resistance	$R_{q\,6}$		500		Ω
	$R_{q\,7}$		500		Ω
FM-part: (f_Z = 5.5 MHz; f_{mod} = 1 kHz)					
Input impedance	$Z_{i\,9\text{-}10}$		800		Ω
AM-suppression	a_{AM}		42		dB
($V_{i\,9\text{-}10}$ = 1 mV; f = 12.5 MHz; m = 30%)					
Signal-to-noise ratio ($V_{i\,9\text{-}10}$ = 10 mV)	$a_{S/N}$		85		dB
Input voltage for limiting	$V_{i\,lim}$		60		μV
(Δf = 30 kHz)					
Demodulator output resistance	$R_{q\,15\text{-}16}$		5.4		kΩ
Output resistance for VCR-recording	$R_{q\,12}$			500	Ω
Input resistance for VCR-playback	$R_{i\,12}$	10			kΩ
Integrated resistor for deemphasis	R_{17}		10		kΩ
AF-output voltage	$V_{q\,12}$		600		mV_{rms}
(V_i = 10 mV; with CDA 5.5 MC 10, $R_{q\,11}$ = 2.9 Ω)	$V_{q\,11}$	260	300		mV_{rms}
(Δf = 12.5 kHz)					
AF-gain during VCR-playback	$V_{12\text{-}11}$		0.5		
Total harmonic distortion	THD_{12}		1		%
Cross talk (V_i = 1 mV)					
V_{12} = 2 V_{rms}	$C_{12\text{-}11}$	50	52		dB
V_{12} = 0.3 V_{rms}	$C_{12\text{-}11}$	60	65		dB
Range of volume control	$\frac{V_{AF\,max}}{V_{AF\,min}}$	70	85		dB

Circuit description

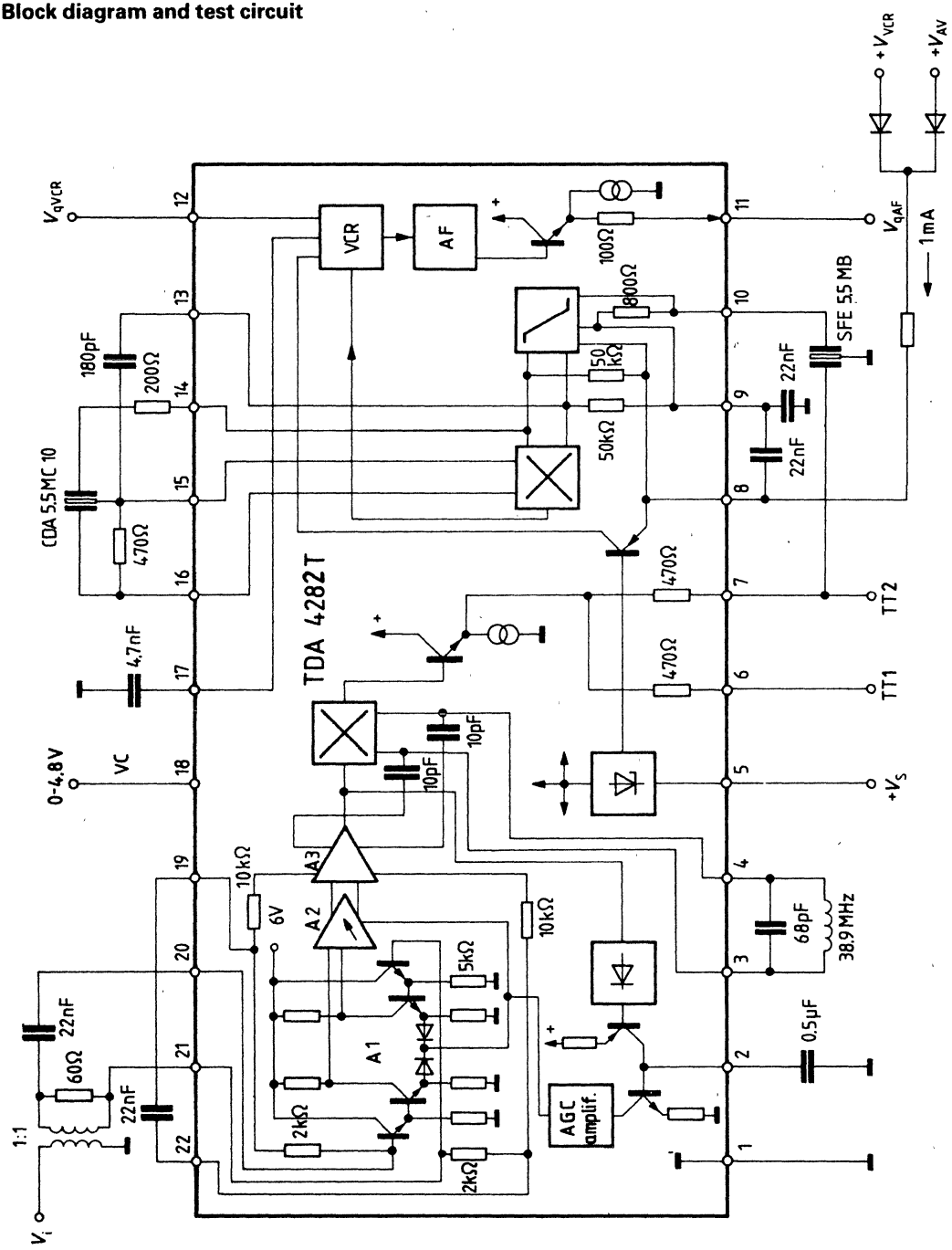
The TDA 4282 T contains essentially two functional blocks:

1. A regulated AM amplifier with a peak rectifier to generate the AGC voltage. The AM amplifier drives an FM demodulator, at the output of which the differential sound carrier (38.9 MHz−33.4 MHz = 5.5 MHz) is available. The double sideband portions close to the carrier are suppressed. The 5.5 MHz carrier reaches the functional block via an external selection.
2. An FM limiter amplifier with coincidence demodulator, a standard VCR connector and a separate AF output with volume control.

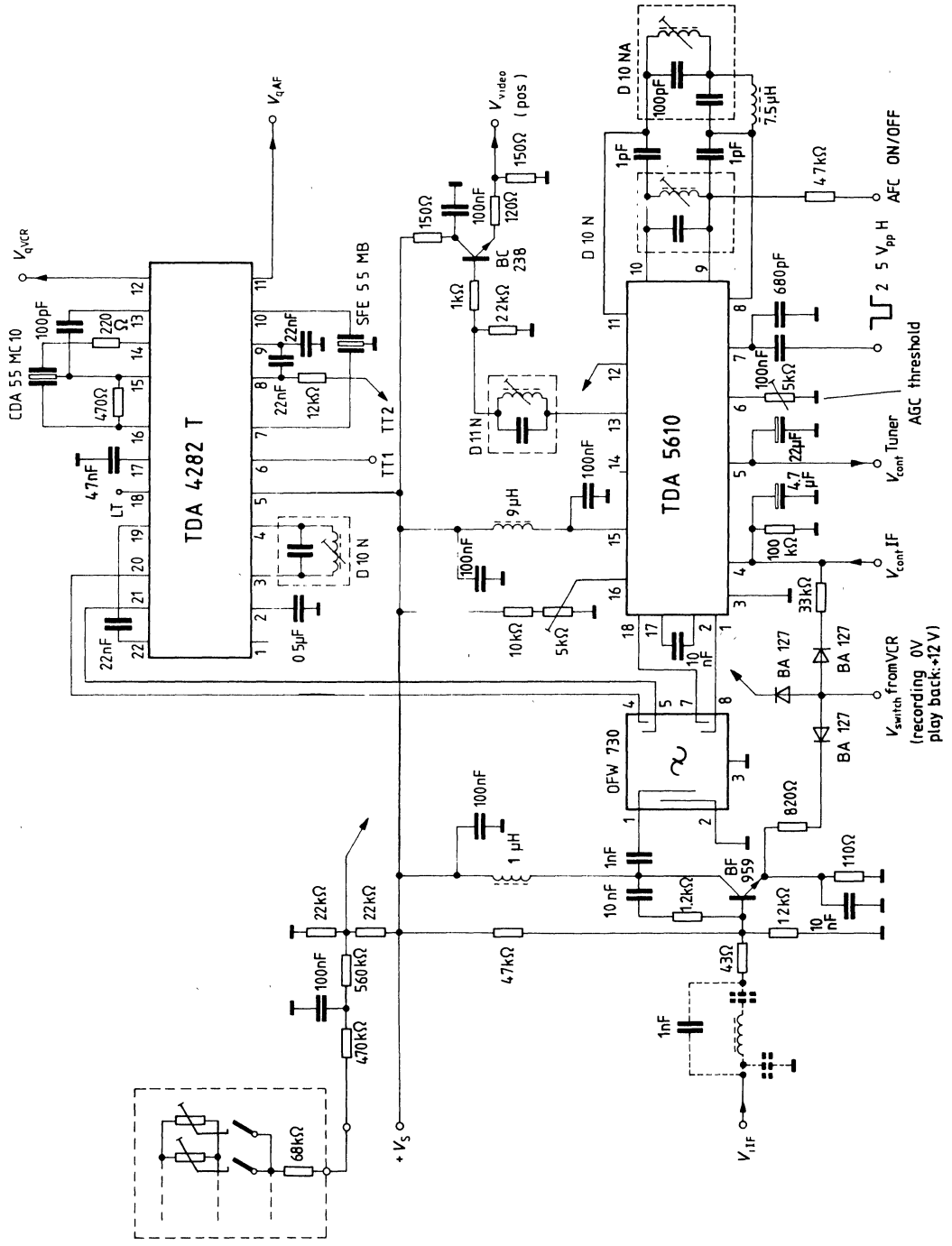
Pin assignment

Pin No.	Pin designation
1	Ground
2	AM-IF control
3	AM amplifier demodulator
4	AM amplifier demodulator
5	Supply voltage (plus)
6	AM amplifier sound carrier output TT 1
7	AM amplifier sound carrier output TT 2
8	AM-IF amplifier negative feedback for working point
9	AM-IF amplifier negative feedback for working point
10	FM-IF amplifier IF input
11	AF output
12	VCR connection
13	FM-IF amplifier emitter follower output
14	FM-IF amplifier emitter follower output
15	FM amplifier demodulator
16	FM amplifier demodulator
17	Deemphasis condensator
18	Volume control
19	AM-IF negative feedback for working point
20	AM-IF amplifier IF input
21	AM-IF amplifier IF input
22	AM-IF negative feedback amplifier for working point

Block diagram and test circuit



Application circuit



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SIEMENS

TDA 5400-2
Video IF IC with AFC

The high gain, controlled video IF amplifier with controlled demodulator includes low-impedance outputs for the positive and negative video signal, gated control as well as delayed tuner control and an AFC output.

TDA 5400-2: for PNP tuners

Features

- High degree of integration
- Extensive control range
- High input sensitivity

Maximum ratings

Supply voltage	V_S	16.5	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\ SA}$	70	K/W

Operational range

Supply voltage	V_S	10 to 15.8	V
IF frequency	f_{IF}	15 to 75	MHz
Ambient temperature	T_A	0 to 70	°C

Characteristics

$V_S = 13$ V; $T_A = 25$ °C

Current consumption	I_{13}	60	mA
Stabilized reference voltage	$V_{14/12}$	6.0	Vdc
Control current for tuner $V_{16} = 0.5\ V_{13}$	I_{16}	4.0	mA
Tuner AGC threshold	$V_{15/12}$	0 to 4	Vdc
Gating pulse voltage			
pos. gating pulse	V_1	+3.0	V
neg. gating pulse	V_1	−3.0	V
Input voltage at G_{max} $V_3 = 3\ V_{pp}$	$V_{i17/18}$	max 100	µV
AGC range	ΔG	60	dB
IF control voltage			
V_{max}	$V_{2/12}$	min 0	Vdc
V_{min}	$V_{2/12}$	max 4.0	Vdc
AFC output current	I_{q6}	±1.0	mA
AFC switching			
$V_8 = V_9; R = 10$ kΩ OFF	$V_{8/12}$	max 4.0	Vdc
$V_8 = V_9; R = \infty$ ON	$V_{8/12}$	6.0	Vdc
AFC direction			
$di/df > 0$	$V_{5/12}$	4.0 to V_{13}	Vdc
$di/df < 0$	$V_{5/12}$	0 to 1.0	Vdc
Video output voltage (pos.) $R_L = \infty$	$V_{q3\,pp}$	3.0	V
Sync pulse level	$V_{3/12}$	2.0	Vdc
DC voltage $V_2 = 4$ V; $V_{17/18} = 0$	$V_{3/12}$	5.3	Vdc
Output current			
to ground through R	I_{q3}	−5.0	mA
to plus $V_3 = 7$ V	I_{q3}	+2.0	mA
Video output voltage (neg.) ($R_L = \infty$)	$V_{q4\,pp}$	3.0	V
Sync pulse level	$V_{4/12}$	V_{13} −2.0	Vdc
DC voltage ($V_2 = 4$ V; $V_{17/18} = 0$)	$V_{4/12}$	V_{13} −5.3	Vdc
Output current			
to ground through R	I_{q4}	−5.0	mA
to plus $V_4 = V_{13}$	I_{q4}	+1.0	mA

Additional application data[1])

Input impedance	$Z_{i17/18}$	1.8/2	kΩ/pF
Output impedance	$Z_{q10/11}$	6.6/2	kΩ/pF
AFC input impedance	$Z_{i8/9}$	20	kΩ
Output resistance	R_{q3}	150	Ω
Output resistance	R_{q4}	150	Ω
Residual IF (basic frequency)	$V_3; V_4$	10	mV
Video bandwidth (−3 dB)	B_{video}	6.0	MHz
Intermodulation ratio with reference to f_{CC} (sound-color-beat frequency)	a	45	dB

1) not measured

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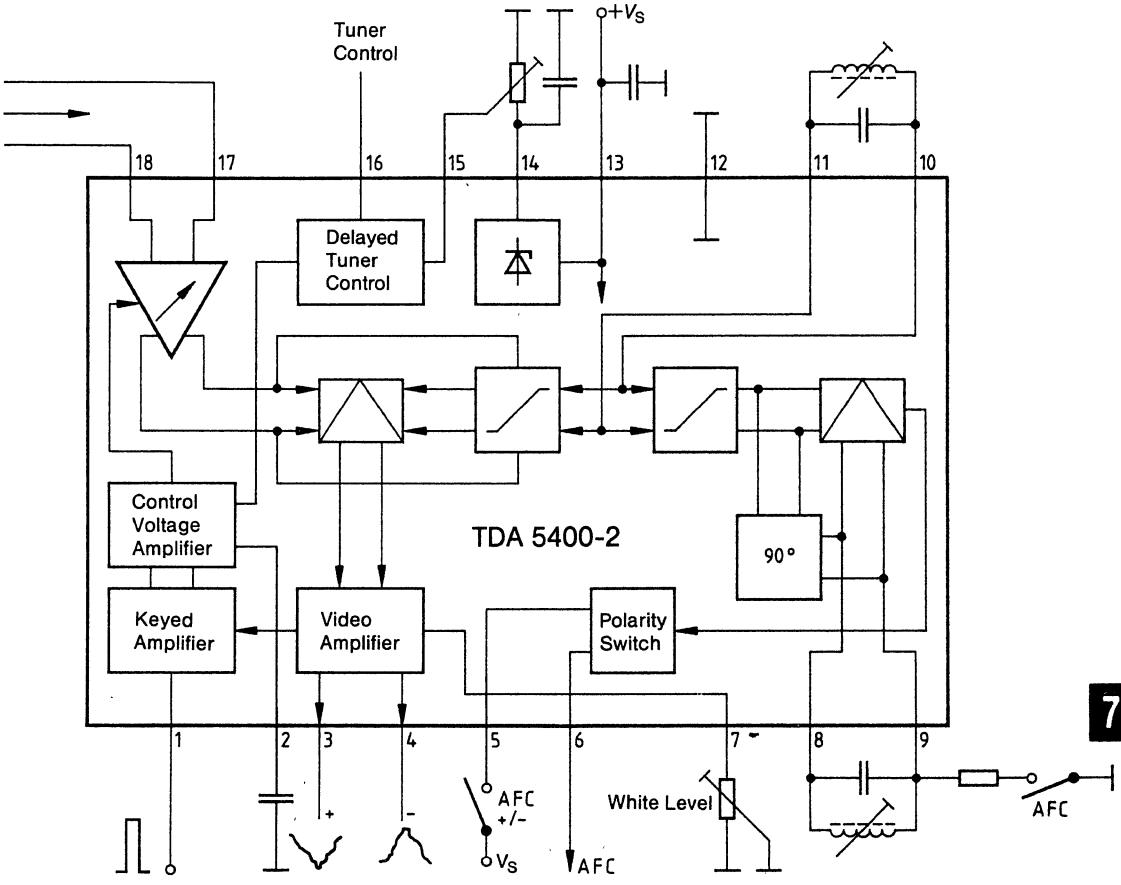
Circuit description

The integrated circuit is comprised of a 4-stage controlled AM amplifier, a limiter and mixer for synchronous demodulation of the video signals as well as an FM demodulator to generate positive or negative AFC voltages. In addition, an amplifier for both the positive and negative video output signal is included. The positive video signal together with the positive flyback pulse are used for gated control.

Pin description

Pin	Function
1	Gating pulse
2	Time constant AGC
3	Positive video output
4	Negative video output
5	AFC polarity switch
6	AFC output
7	White level adjustment
8	AFC circuit
9	AFC circuit
10	Tank circuit
11	Tank circuit
12	GND
13	Supply voltage
14	Reference voltage
15	Tuner AGC
16	Delayed AGC output
17	Video IF input
18	Video IF input

Block diagram



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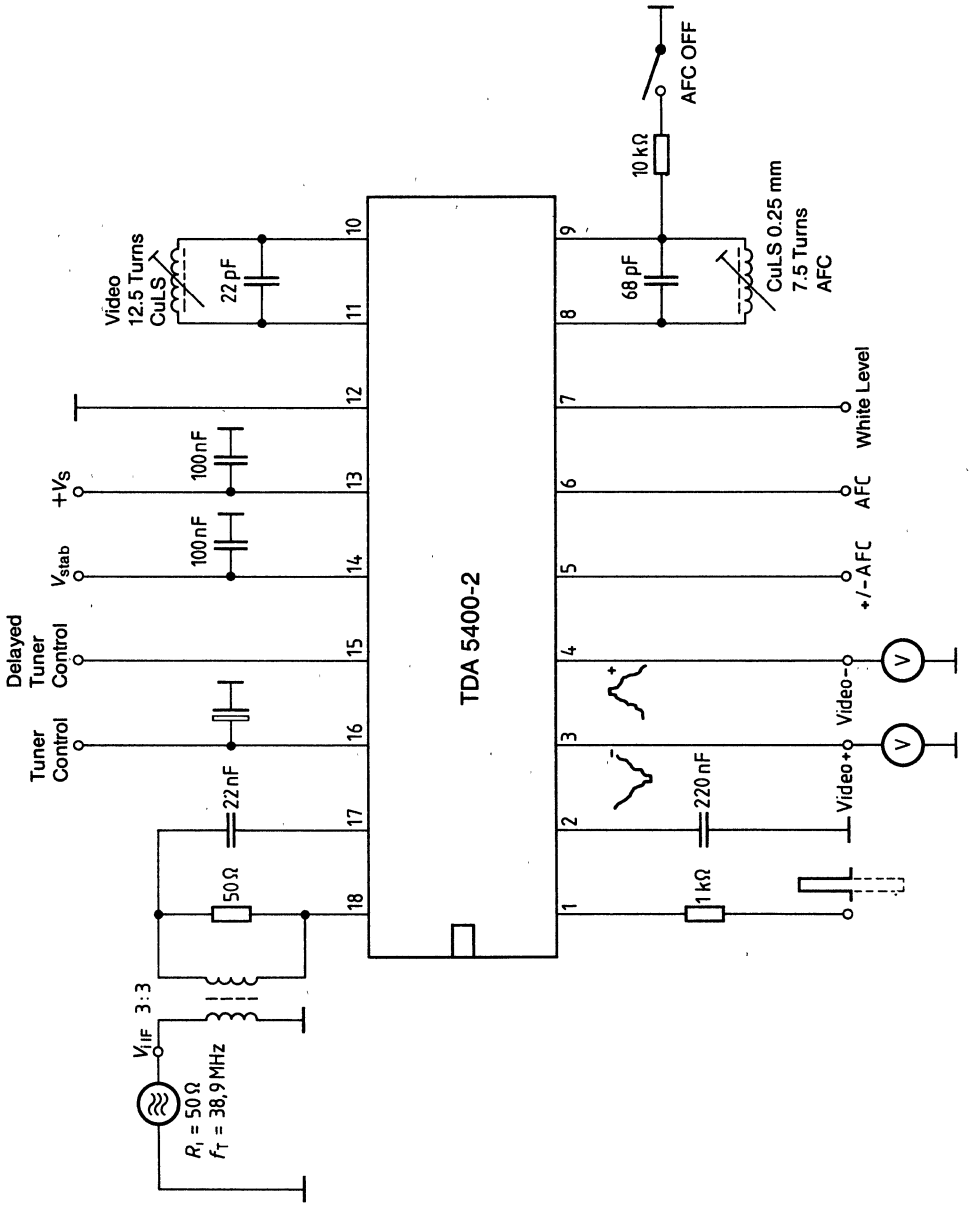
Measurement circuit



TDA 5660 P
Modulator for TV, Video and Sound Signals

The monolithically integrated circuit TDA 5660 P is especially suitable as modulator for the 48 to 860 MHz frequency range and is applied e.g. in video recorders, cable converters, TV converter installations, demodulators, video generators, video security systems, amateur TV applications, as well as personal computers.

- Synchronizing level-clamping circuit
- Peak white value gain control
- Continuous adjustment of modulation index for positive and negative modulation
- Dynamic residual carrier setting
- FM sound modulator
- AM sound modulator
- Picture carrier to sound carrier adjustment
- Symmetrical mixer output
- Symmetrical oscillator with own RF ground
- Low radiation
- Superior frequency stability of main oscillator
- Superior frequency stability of sound oscillator
- Internal reference voltage

Circuit description

Via pin 1, the sound signal is capacitively coupled to the AF input for the FM modulation of the oscillator. An external circuitry sets the preemphasis. This signal is forwarded to a mixer which is influenced by the AM modulation input of pin 16. The picture to sound carrier ratio can be changed by connecting an external voltage to pin 16, which deviates from the internal reference voltage. In case, the sound carrier should not be FM but AM modulated, pin 1 should be connected to pin 2, while the AF signal is capacitively coupled to pin 16. Through an additional external dc voltage at pin 16, the set AM modulation index can be changed by overriding the internally adjusted control voltage for a fixed AM modulation index. At the output of the above described mixer the FM and/or AM modulated sound signal is added to the video signal and mixed with the oscillator signal in the RF mixer. A parallel resonant circuit is connected to the sound carrier oscillator at pin 17, 18. The unloaded Q of the resonant circuit must be $Q = 25$ and the parallel resistor $R_T = 6.8\ k\Omega$ to ensure a picture to sound carrier ratio of 12.5 dB. At the same time, the capacitative and/or inductive reactance for the resonance frequency should have a value of $X_C \approx X_L \approx 800\ \Omega$.

The video signal with the negative synchronous level is capacitively connected to pin 10. The internal clamping circuit is referenced to the synchronizing level. Should the video signal change by 6 dB, this change will be compensated by the resonant circuit which is set to the peak white value. At pin 11, the current pulses of the peak white detector are filtered through the capacitor which also determines the control time constant. When pin 12 is connected to ground, the RF carrier switches from negative to positive video modulation.

With the variable resistor of $R = \infty$ ....0 Ω at pin 12, the modulation depth, beginning with $R = \infty$ and a negative modulation of $m_{D/N} = 80\%$, can be increased to $m_{D/N} = 100\%$ and continued with a positive modulation of $m_{D/P} = 100\%$ down to $m_{D/P} = 88\%$ with $R = 0$ Ω. The internal reference voltage has to be capacitively blocked at pin 2.

The amplifier of the RF oscillator is available at pins 3-7. The oscillator operates as a symmetrical ECO circuit. The capacitive reactance for the resonance frequency should be $X_C \approx 70$ Ω between pins 3, 4 and 6, 7 and $X_C \approx 26$ Ω between pins 4, 6. In order to set the required residual carrier suppression, pin 9 is used to compensate for any dynamic asymmetry of the RF mixer during high frequencies of > 300 MHz. The oscillator chip ground, pin 5, should be connected to ground at the oscillator resonant circuit shielding. Via pin 3 and 7 an external oscillator signal can be injected inductively or capacitively. The peripheral layout of the pc board should be provided with a minimum shielding attenuation of approx. 80 dB between the oscillator pins 3-7 and the modulator outputs 13-15.

For optimum residual carrier suppression, the symmetric mixer outputs at pins 13, 15 should be connected to a matched balanced-to-unbalanced broadband transformer with excellent phase precision at 0 and 180 degrees, e.g. a Guanella transformer. The transmission loss should be less than 3 dB. In addition, an LC low pass filter combination is required at the output. The cut-off frequency of the low pass filter combination must exceed the maximum operating frequency.

If the application circuit according to figure 1, 2 is used, a multiplication factor V/RF (application) = V/RF (data sheet) 3.9 must be used to convert a 300 Ω symmetrical impedance to an asymmetrical impedance of 75 Ω for the stated RF output voltage V_q of the type specification in order to ensure a transmission attenuation of 0 dB for the balanced-to-unbalanced mixer.

Maximum ratings

		min	max		Remarks
Supply voltage	V_S	−0.3	14.5	V	
Current from pin 2	$-I_2$	0	2	mA	$V_2 = 7$ to 8 V $V_S = 9.5$ to 13.5 V
Voltage at pin 1	V_1	$V_2 - 2$	$V_2 + 2$	V	$V_S = 9.5$ to 13.5 V
Voltage at pin 9	V_9	−4	1	V	
Voltage at pin 10	$V_{10\,pp}$		1.5	V	only via C (max. 1 µF)
Capacitance at pin 2	C_2	0	100	nF	
Capacitance at pin 11	C_{11}	0	15	µF	
Voltage at pin 12	V_{12}	−0.3	1.4	V	
Voltage at pin 13	V_{13}	V_2	V_S	V	
Voltage at pin 15	V_{15}	V_2	V_S	V	
Voltage at pin 16	V_{16}	$V_2 - 1.5$	$V_2 + 1.5$	V	$V_S = 9.5$ to 13.5 V
Only the external circuitry shown in application circuits 1 and 2 may be connected to pins 3, 4, 6, 7, 17 and 18					
Junction temperature	T_j		150	°C	
Storage temperature	T_{stg}	−40	125	°C	
Thermal resistance (system-air)	$R_{th\,SA}$		80	K/W	

Operating range

Supply voltage	V_S	9.5	13.5	V	
Video input frequency	f_{VIDEO}	0	5	MHz	
Sound input frequency	f_{AF}	0	20	kHz	
Output frequency	f_q	48	860	MHz	depending on the oscillator circuitry at pins 3-7
Ambient temperature	T_A	0	70	°C	
Sound oscillator	f_{OSC}	4	7	MHz	
Voltage at pin 13, 15	$V_{13,15}$	V_2	V_S	V	

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Characteristics

V_S = 11 V; T_A = 25 °C

		Test conditions	Figure	min	typ	max	
Current consumption	I_8	I_2 = 0 mA	1; 2	22	30	40	mA
Reference voltage	V_2	$0 \leq I_2 \leq 1$ mA	1; 2	7	7.5	8	V
Oscillator frequency range	f_{OSC}	External circuitry adjusted to frequency		48		860	MHz
Turn-on start-up drift	Δf_{OSC}	TC value of capacitor in osc. circuit is 0; drift is referenced only to self-heating of the component t = 0.5-10 s; T_A = const.					
		Ch 30	1; 2	0	−50	−500	kHz
		Ch 40	1; 2	0	−200	−500	kHz
Frequency drift as function of V_S	$-\Delta f_{OSC}$	V_S = 9.5-13.5 V; T_A = const.	1; 2	0			
		Ch 40		−150		150	kHz
Video input current at pin 10	$-I_{10}$	$C_{10} \leq 1$ µF	5	0		10	µA
Video input voltage at pin 10	$V_{10\,pp}$	at coupling capac. $C \leq 1$ µF $I_{leak} \leq \pm 0.3$ µA	21; 22	0.7		1.4	V
Modulation depth	$m_{D/N}$	neg. mod.	1; 16	75	80	85	%
$V_{VIDEO\,pp}$ = 1 V; f_{VIDEO} = 200 kHz sine signal	$m_{D/P}$	pos. mod.	2; 16	83	88	93	%
Output impedance	Z_{13}; Z_{15}	static	24	10			kΩ
RF output voltage	$V_{q\,rms}$	Ch 40	1b	2.5	3.5	5.5	mV
Modulation signal in neg. modulation pin 12 open							
Output capacitance	C_{13}=C_{15}		25	0.5	1	2.0	pF
S parameter at pins 3, 4 and 6, 7			26				
RF output phase	$\alpha_{13,15}$			140	180	220	degrees
RF output voltage change; adjustment range	ΔV_q	f = 543.25-623.25 Δf = 80 MHz Ch 30-Ch 40	1	0		1.5	dB
RF output voltage change	ΔV_q	f = 100-300 MHz	6	0		1.5	dB
RF output voltage change	ΔV_q	f = 48-100 MHz	6	0		1.5	dB
Oscillator interference FM caused by AM modulation and coupling of the modulator output with the oscillator resonant circuit; $V_{VIDEO\,pp}$ = 1 V; f_{VIDEO} = 10 kHz; sine signal							
	Ch 30		1; 9	0	5	15	kHz
	Ch 40		1; 9	0	7	21	kHz

Characteristics

$V_S = 11$ V; $T_A = 25$ °C

		Test conditions	Figure	min	typ	max	
Intermodulation ratio	a_{MR}	$f_P + 1.07$ MHz	1; 7; 15	54	75		dB
Harmonic wave ratio	a_H	$f_P + 8.8$ MHz without video signal 19, 20, 21 unmodulated video and sound carrier, measured with the spectrum analyzer as difference between video carrier signal level and sideband signal level without video and sound modulation.	1; 7; 15	35			dB
Harmonic wave ratio	a_H	$f_P + 2f_S$	1; 7	35	48		dB
Harmonic wave ratio	a_H	$f_P + 3f_S$ V_q with spectrum analyzer; loaded Q factor Q_L of the sound oscillator resonant circuit adjusted by R_S to provide the required picture to sound carrier ratio of 12.5 dB; $R_S = 6.8$ kΩ; $Q_U = 25$ of the sound oscillator circuit.	1; 7	42	48		dB
Sound carrier ratio	$a_{P/S}$		1; 7; 17	10	12.5	15	dB
Color picture to sound carrier ratio	a_P	$f_P + 4.4$ MHz (dependent on video signal)	1		17		dB
All remaining harmonic waves	a	Multiple of fundamental wave of picture carrier, without video signal, measured with spectrum analyzer; $f_{P/S} = 523.25$-623.25 MHz	1	15			dB
Amplitude response of the video signal	a_V	$V_{VIDEO\,pp} = 1$ V with additional modulation $f = 15$ kHz-5 MHz sine signal between black and white	1; 13	0		1.5	dB
Residual carrier suppression	a_R	With adjustment at pin 9 Ch 30...Ch 40	1; 12	32			
Static mixer balance characteristic	$\Delta V_{13/15}$	V_9 adjusted to $\Delta V_{13/15}$ minimum	21; 23	−100	0	+100	mV
Dynamic mixer balance characteristics	$V_{13\,rms}$	V_9 adjusted to $V_{13\,rms}$ minimum	21; 23		0	10	mV
Stability of set modulation depth	Δm_D	Video input voltage changes with sine signals $f = 0.2$ MHz; $\Delta V_{VIDEO\,pp} = 1$ V ± 3 dB; Ch 30...Ch 40; $V_S = 12$ V; T_A = const.			1	±2.5	%
Stability of set modulation depth	Δm_D	$f = 48$...100 MHz	6		1	±2.5	%
Stability of set modulation depth	Δm_D	$f = 100$...300 MHz	6		2	±4	%
Stability of set modulation depth	Δm_D	$T_A = 0$-60 °C; $V_S = 12$ V	1		1	±2.5	%

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Characteristics

$V_S = 11$ V; $T_A = 25$ °C

		Test conditions	Figure	min	typ	max	
Stability of set modulation depth	Δm_D	$V_S = 9.5\text{-}13$; 5 V; T_A = const.	1		1	±2.5	%
Interference product ratio sound in video; sound carrier FM mod.	$a_{S/P}$	Ch 30...Ch 40	1;11	48	60		dB
Signal-to-noise ratio in video; sound carrier unmodulated	$a_{N/P}$	Ch 30...Ch 40	1;11	48	74		dB
Interference product ratio sound in video sound carrier AM mod.	$a_{S/P}$	Ch 30...Ch 40	1;11	20	33		dB
Umweighted FM noise level ratio video in sound; FuBK test picture as video signal	$a_{P/S}$	Ch 39	1a; 8	48	54		dB
Unweighted FM noise level ratio video in sound	$a_{P/S}$	Ch 39; test picture VU G-Y; U/V	2; 8	48	56		dB
		Ch 39; color bar	2; 8	46	52		dB
		Ch 39; uniform red level	2; 8	48	58		dB
		Ch 39; uniform white level	2; 8	45	51		dB
		Ch 39; test pattern	2; 8	48	55		dB
		Ch 39; white bar	2; 8	46	52		dB
		Ch 39; bar	2; 8	45	50.8		dB
		Ch 39; 20T/2T	2; 8	43	49		dB
		Ch 39; 30% white level	2; 8	48	58		dB
		Ch 39; 250 kHz	2; 8	46	52		dB
		Ch 39; multiburst	2; 8	46	53		dB
		Ch 39; ramp	2; 8	44	50		dB
Signal-to-noise ratio of sound oscillator	$a_{S/N}$		1a; 8	48	54		dB
Differential gain	G_{dif}	measured with measurement demodulator, video test signals and vector scope	1			10	%
Differential phase	φ_{dif}		1			15	%
Period required for peak white detector to reach steady state for full modulation depth with 1 white pulse per half frame with control in steady state	t	C at pin 11 = 10 µF; $I_{leak} \leq 2$ µA	1		6	50	µs

Characteristics

$V_S = 11$ V; $T_A = 25$ °C

		Test conditions	Figure	min	typ	max	
Setting time for video signal change from 0 V_{pp} to 1.4 V_{pp}	t	Video blanking signal content is uniform white level	1		120	500	µs
Setting time for video blanking signal from 100% white level to 42% grey level with subsequent rise in grey level to 71% of video blanking signal (due to decontrol process)	t		1		2.25	5	s
Sound oscillator frequency range	$f_{S/OSC}$	Unloaded Q factor of resonant circuit $Q_U = 25$; resonance frequency 5.66 MHz	1	4		7	MHz
Turn-on start-up drift	$\Delta f_{S/OSC}$	Capacitor TC value in sound oscillator circuit is 0, drift is based only on component heating T_A = const.; $f_{S/OSC} = 5.5$ MHz	1		5	15	kHz
Sound oscillator frequency operating voltage	$\Delta f_{S/OSC}$	$V_S = 9.5$-13.5 V; $f_{S/OSC} = 5.5$ MHz; T_A = const.; $Q_U = 25$	1		5	15	kHz
FM mod. harmonic distortion	THD_{FM}	$V_{1\,rms} = 150$ mV	19; 19a		0.6	1.5	%
Audio preamplifier input impedance (dyn.); FM operation	Z_1		1	200			kΩ
FM sound modulator, static modulation characteristic	$\Delta f_{S/OSC}$	$\Delta V_{1/2} = V_1 - V_2 = \pm 1$ V; $f_{S/OSC} = 5.5$ MHz; $Q_U = 25$	1; 14	±210	±270	±330	kHz
FM sound modulation characteristic (dynamic)	$\Delta f_M/\Delta V_1$		1a; 10a	0.3	0.38	0.46	kHz/mV
AM sound modulation factor	m	$V_{AF} = 0.3$ V	2; 3; 4a, b	30	40	50	%
AM sound modulation harmonic distortion	THD_{AM}	$m = 86\%$; $V_{AF} = 0.64$ V; $f_{AF} = 1$ kHz			0.7	3	%
AM audio preamplifier input impedance	Z_{16}		2	25	50	75	kΩ
AM sound modulator input voltage	V_{AF}	$m = 90\%$; $f_{AF} = 1$ kHz	2	0.5	0.67	0.84	V

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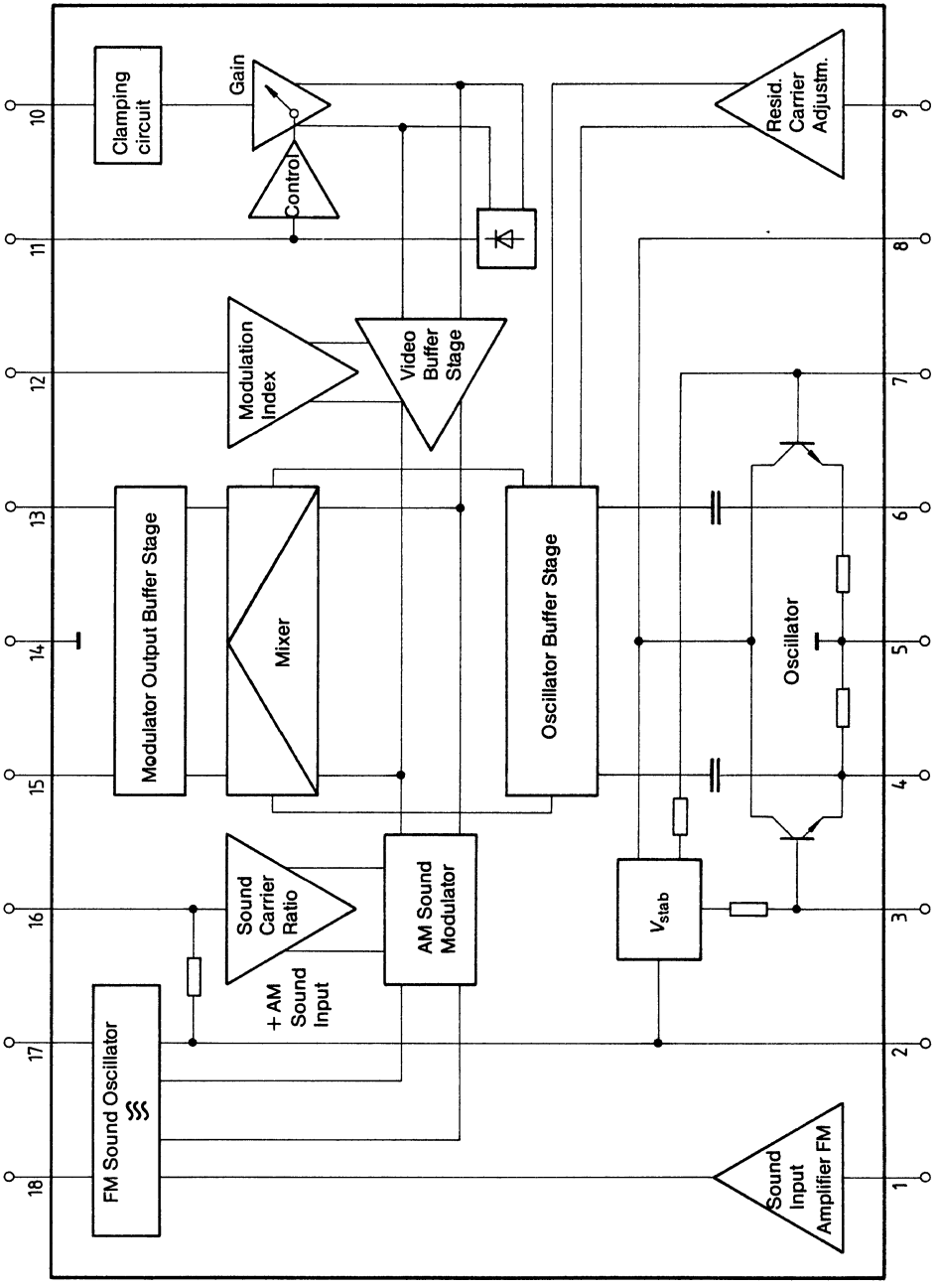
Pin description

Pin	Function
1	AF input for FM modulation
2	Internal reference voltage
3	Symmetrical oscillator input
4	Symmetrical oscillator output
5	Oscillator ground
6	Symmetrical oscillator output
7	Symmetrical oscillator input
8	Supply voltage
9	Dynamic residual carrier adjustment
10	Video input with clamping
11	Connection for smoothing capacitor for video control loop
12	Switch for positive and negative modulation as well as residual carrier control
13	Symmetrical RF output
14	Remaining ground of component
15	Symmetrical RF output
16	Picture to sound carrier ratio (adjustment and AM sound input)
17	Sound oscillator symmetrical input for tank circuit
18	Sound oscillator symmetrical input for tank circuit

Block diagram



Test and measurement circuit 1 for FM sound carrier and negative video modulation

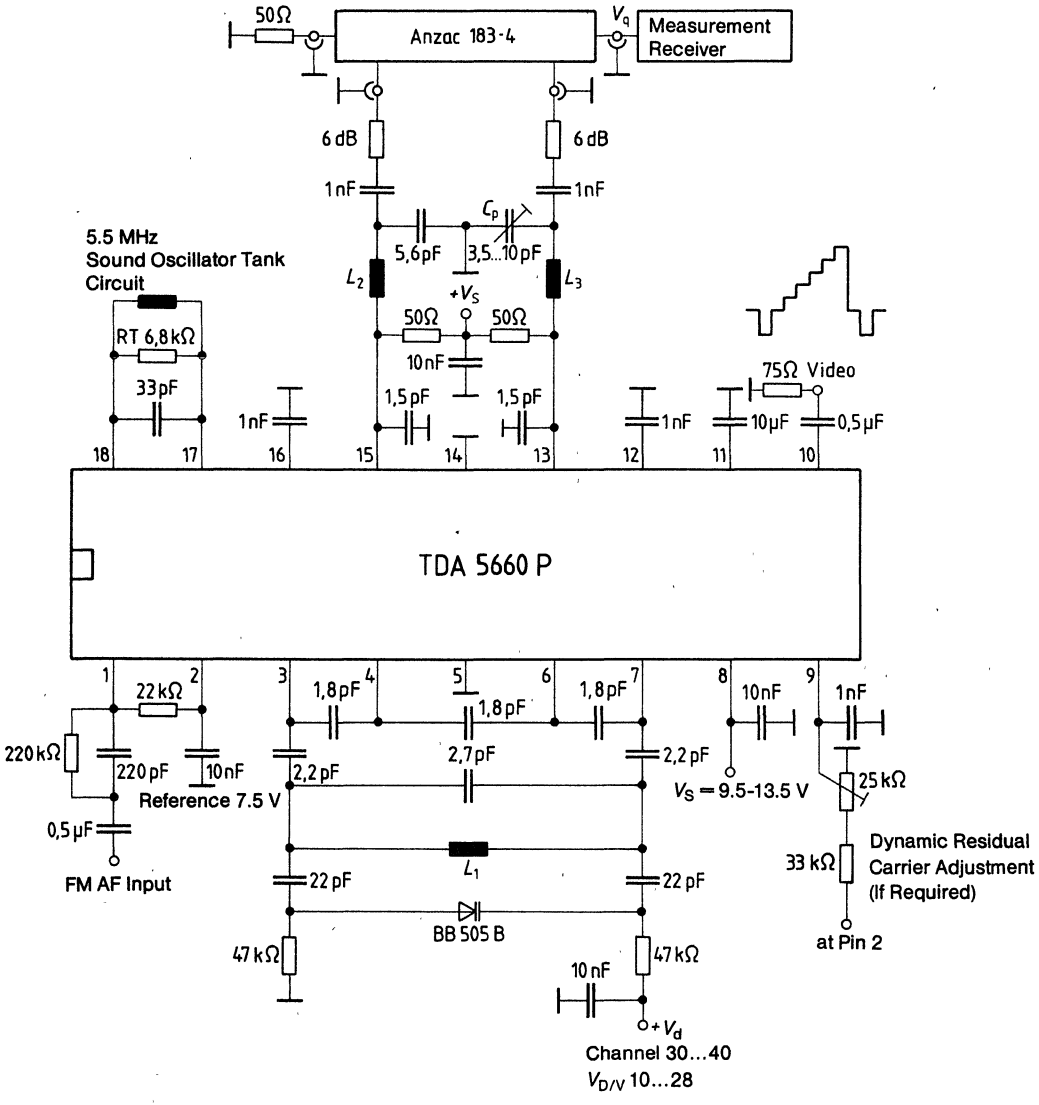


Figure 1

Test and measurement circuit 1 for FM sound carrier and negative video modulation

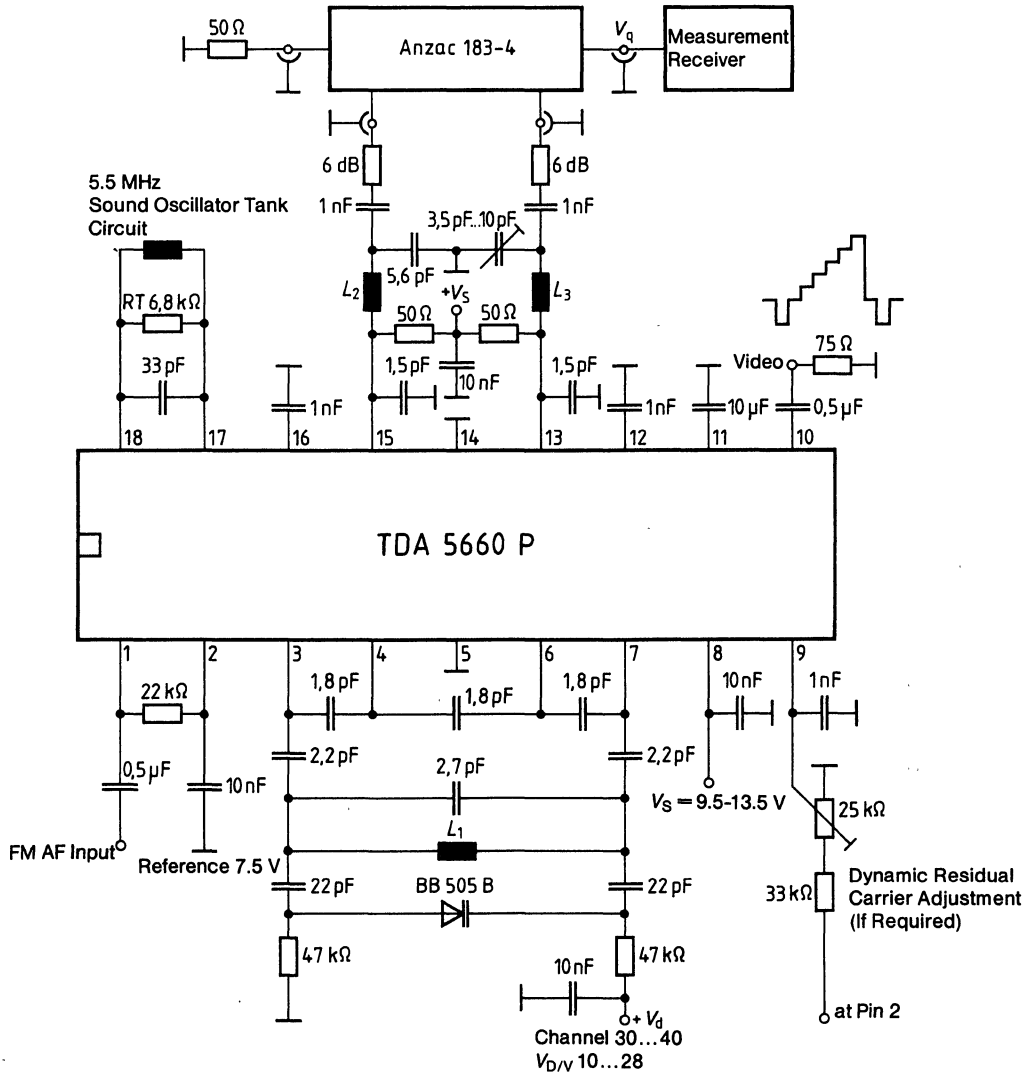


Figure 1a

Test and measurement circuit 1 for FM sound carrier and negative video modulation

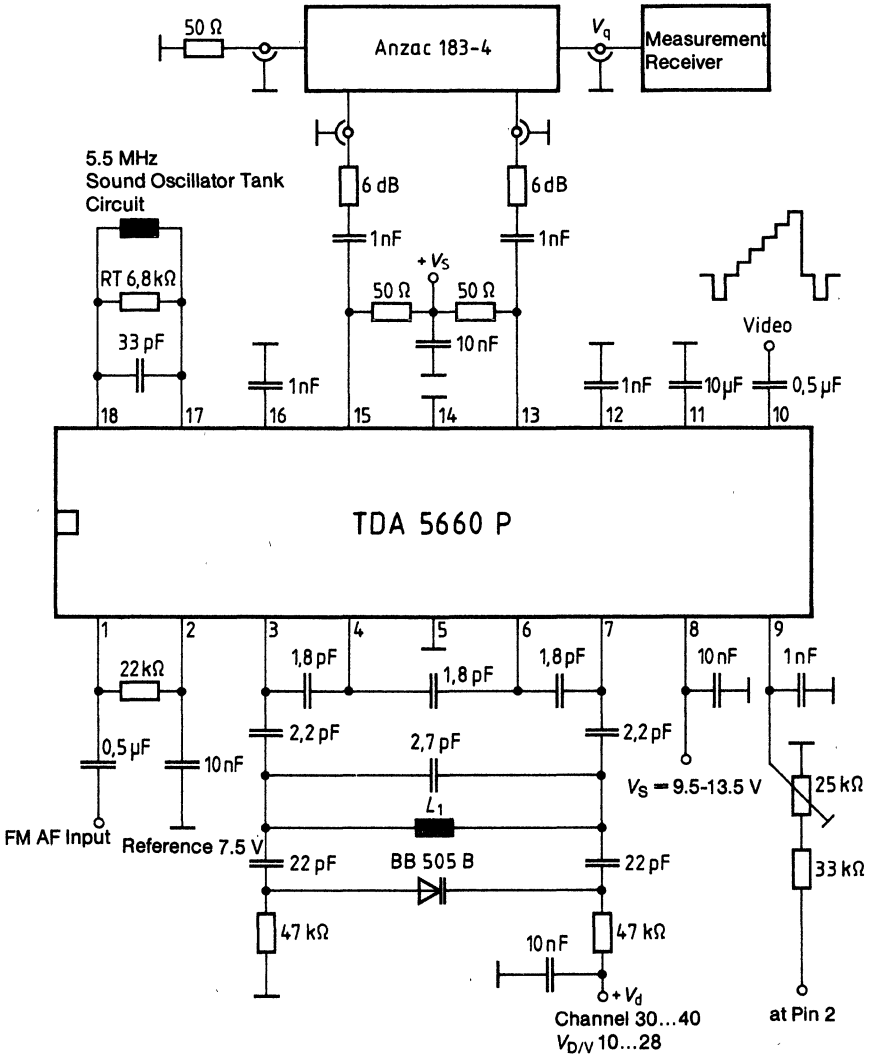


Figure 1b

Test and measurement circuit 2 for FM sound carrier and negative video modulation

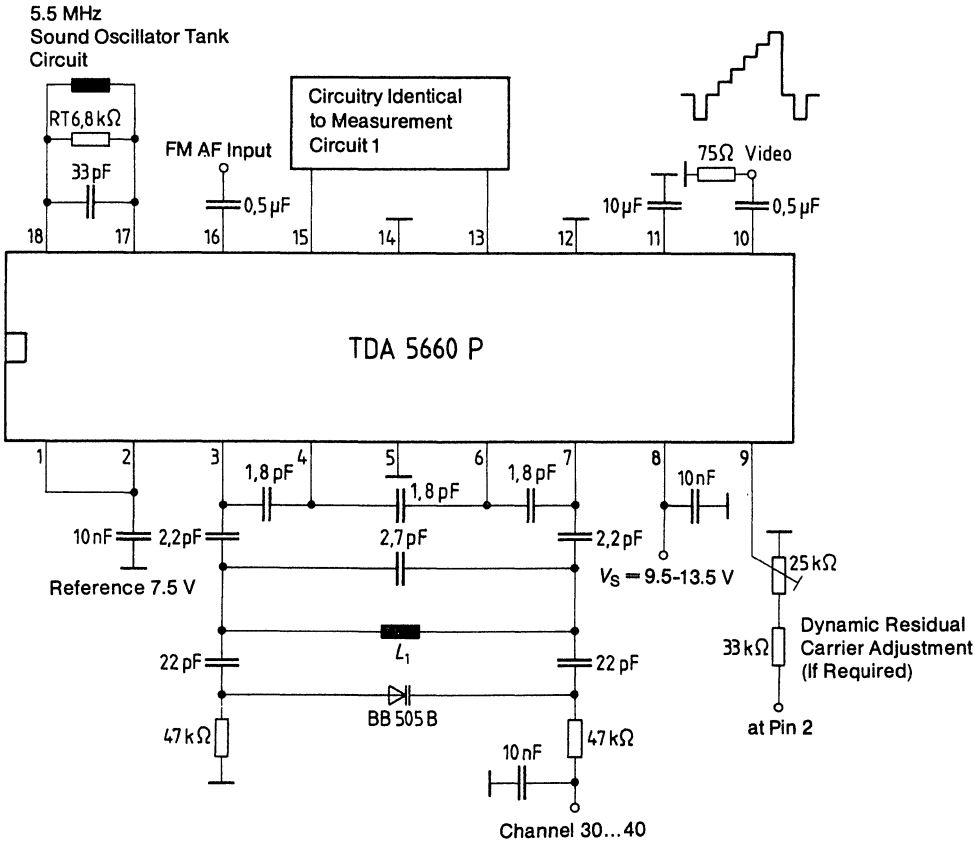


Figure 2

AM sound modulation measurement

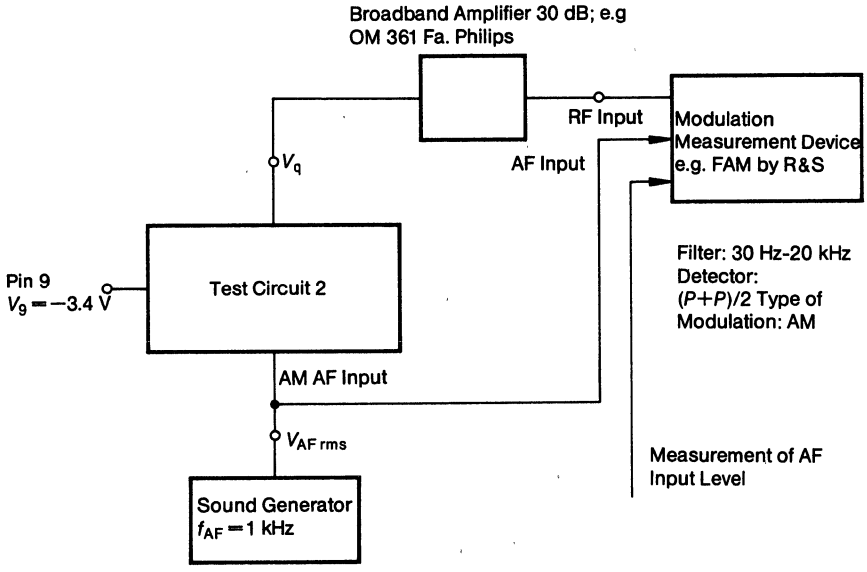


Figure 3

AM sound carrier modulation index versus AF input voltage at pin 16

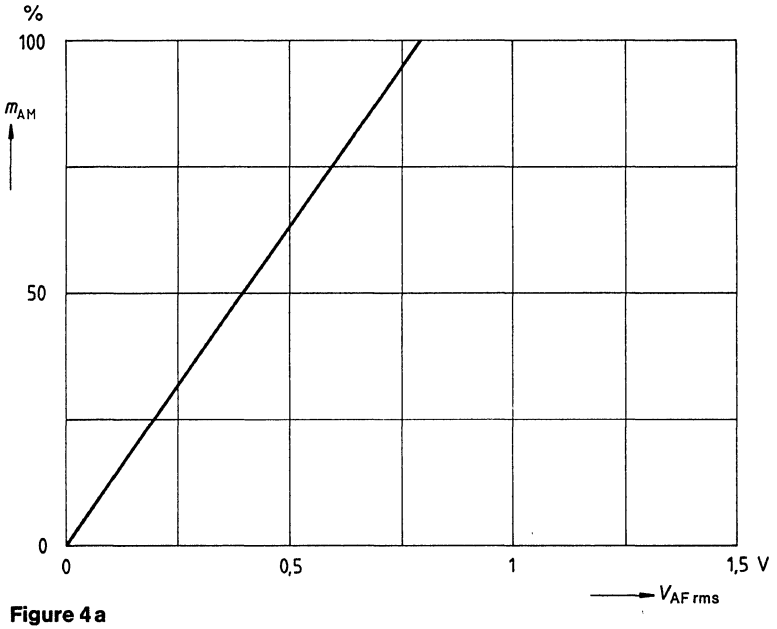


Figure 4a

AM sound carrier modulation index versus dc voltage offset at pin 16

$V_{AF\,rms} \doteq 0.6$ V; $\Delta V_{16/2}$ (V) $= V_2 - V_{16}$

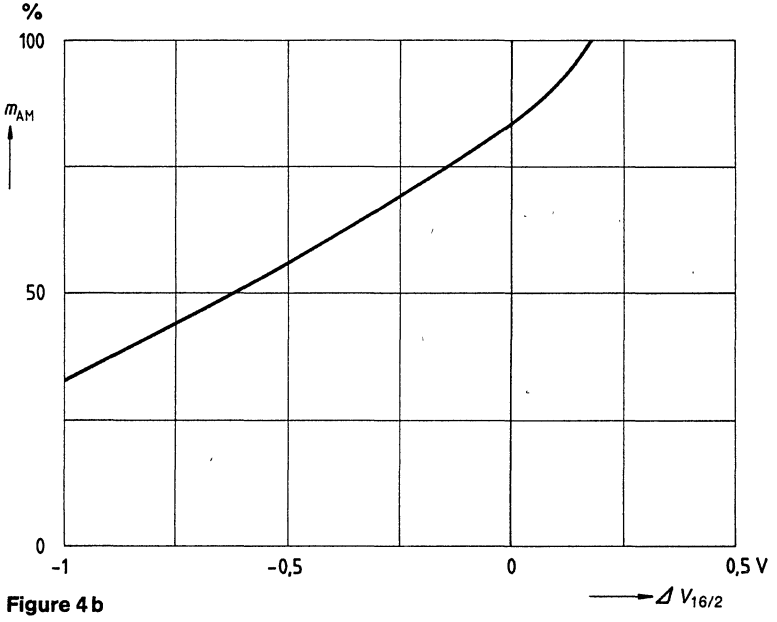


Figure 4b

7

Measurement circuits

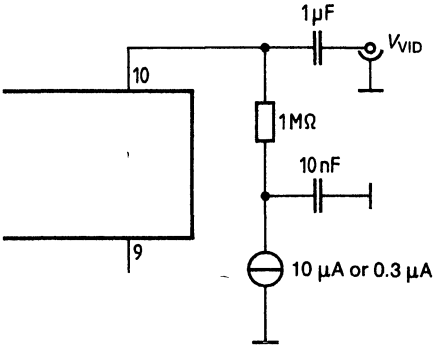
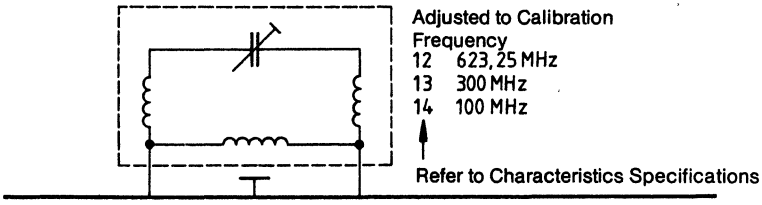


Figure 5



TDA 5660 P Remaining External Circuitry as Fig. 1

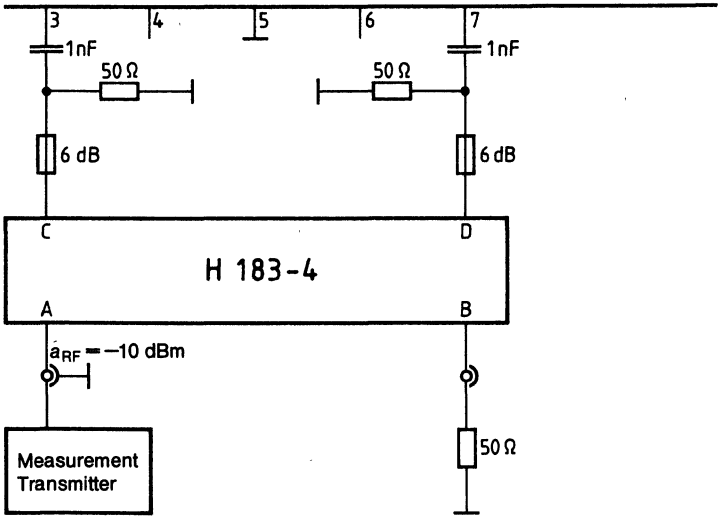


Figure 6

Frequency spectrum above the video carrier, measured at clamp V_q with a spectrum analyzer

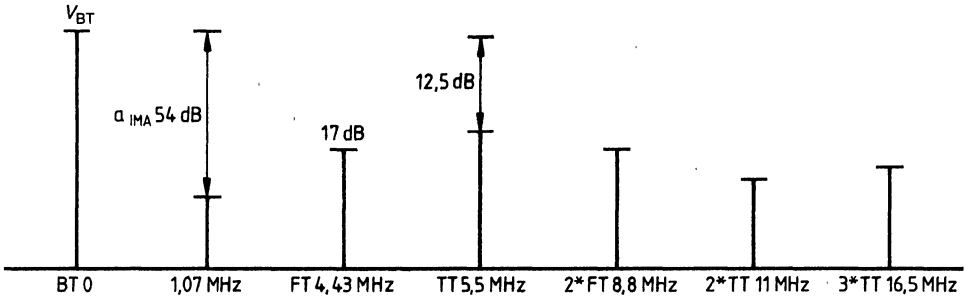


Figure 7

BT = Video Carrier
FT = Frequency Carrier
TT = Sound Carrier

7

Description of the measurement configuration to measure the noise voltage, video in sound

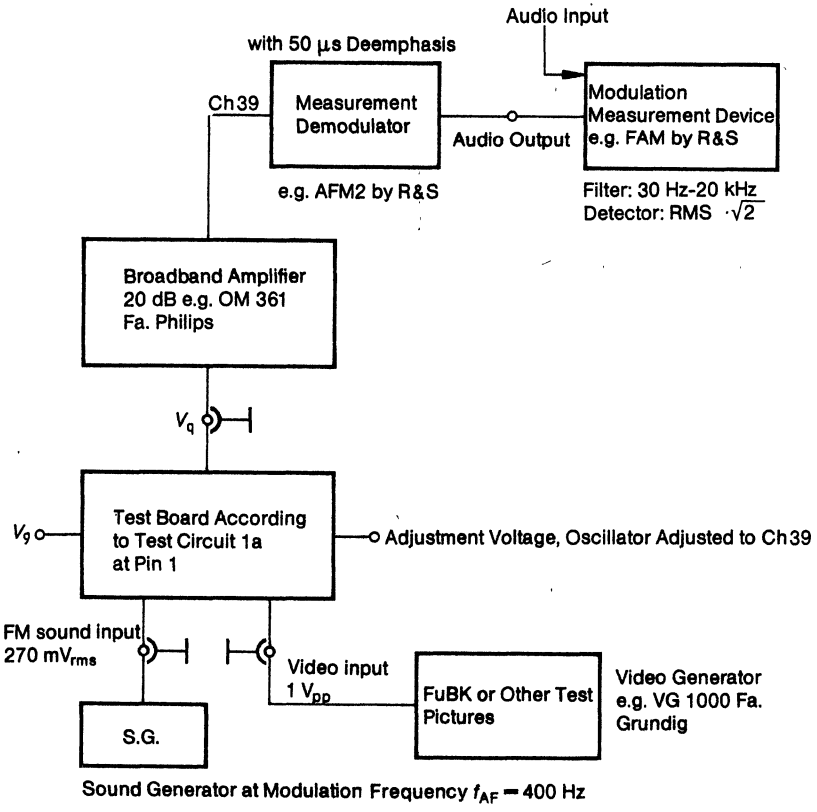


Figure 8

Calibration: A signal of $V_{AF\ rms}$ = 270 mV and f = 0.4 kHz, corresponding to a nominal deviation of 30 kHz, is connected to the sound input, and the demodulated AF reference level at the audio measurement device is defined as 0 dB. No video signal is pending.

Measurement: 1) The AF signal is switched off and the FuBK video signal is connected to the video input with $V_{VIDEO\ pp}$ = 1 V. The audio level in relation to the reference calibration level is measured as ratio $a_{p/s} = 20 \log (V_{FUBK})/(V_{nominal})$.

2) AF and video signal are switched off. The noise ratio in relation to the AF reference calibration level is measured as signal-to-noise ratio $a_{S/N}$.

Description of the measurement configuration to measure the oscillator interference FM

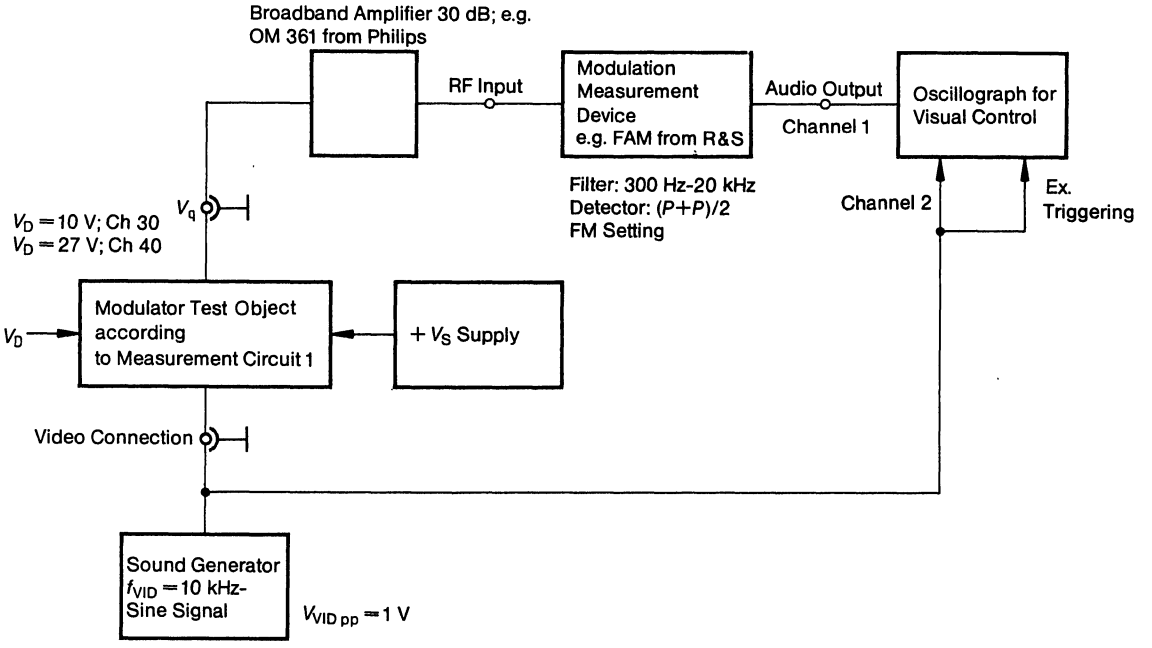


Figure 9

7

Description of the measurement configuration to measure the total harmonic distortion during FM operation of the sound carrier

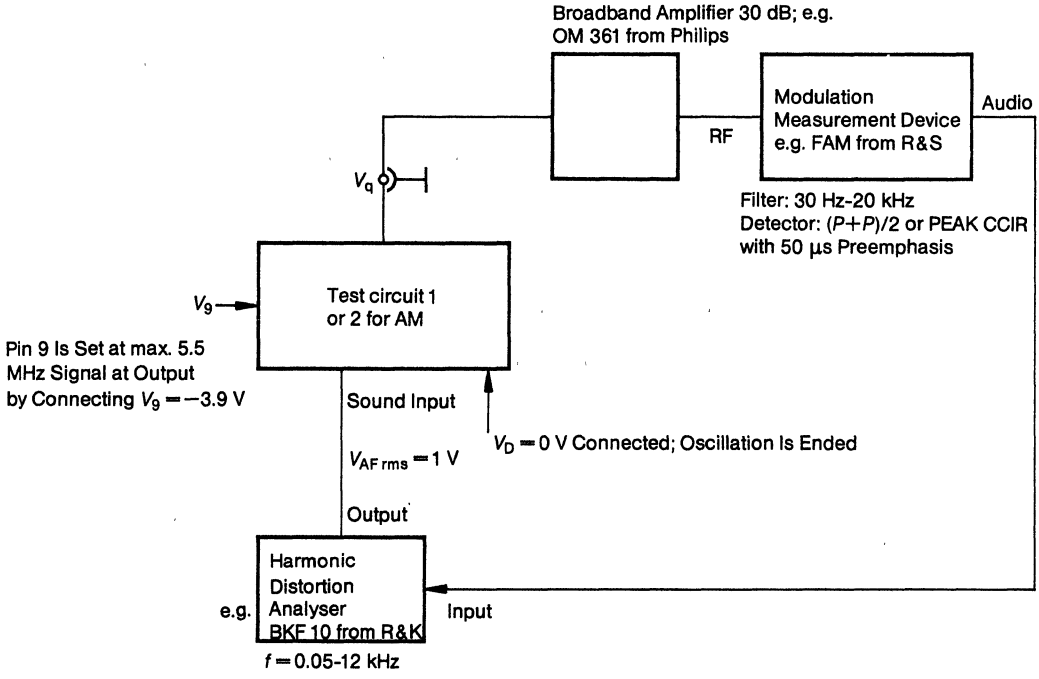


Figure 10

Description of the measurement configuration to measure the total harmonic distortion during FM operation of the sound carrier

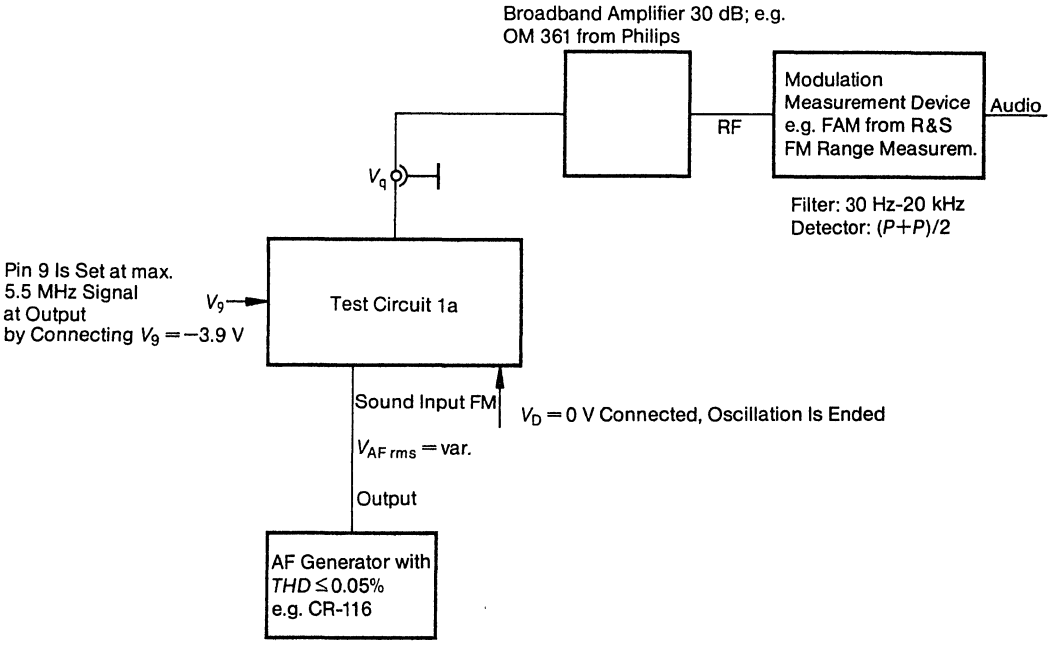


Figure 10a

7

Description of the measurement configuration to measure the sound and/or noise in video during FM and/or AM sound carrier modulation

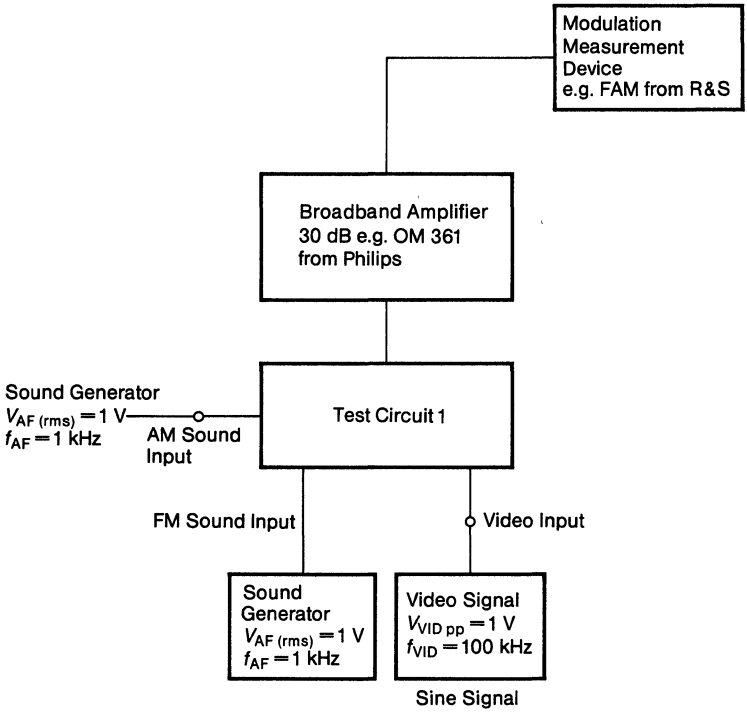


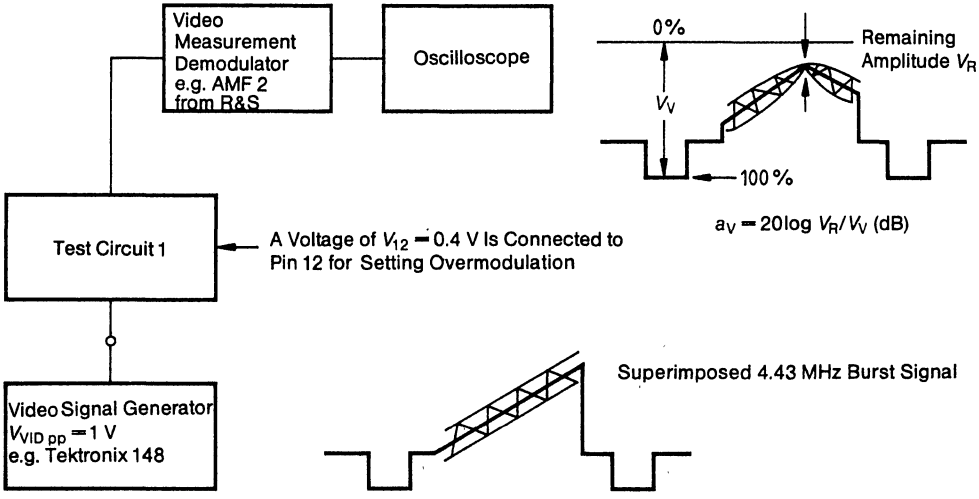
Figure 11

Calibration: AF signals are switched off; video signal is pending at the video input; device to measure modulation set at AM is adjusted to video carrier; filter: 300 Hz...200 kHz; detector $(P+P)/2$; resulting modulation index is defined as $m_V = 0$ dB.

Measurement:

1) Measurement of interference product ratio sound in video during FM modulation of the sound carrier: AF signal is connected to FM sound input; video signal is switched off; device to measure modulation is set to AM; filter: 300 Hz...3 kHz; detector: $(P+P)/2$; a ratio of $a_{S/P} = 20$ log $m_{V/S}$/mV) is derived from the resulting modulation index $m_{V/S}$.
2) Measurement of interference product ratio sound in video during AM modulation of sound carrier: AF signal is connected to AM sound input; otherwise identical with measurement 1.
3) Measurement of signal-to-noise ratio in video without AM/FM modulation of sound carrier: AF signals are switched off; video signal is switched off; control voltage at pin 11 is clamped to value present during connected video signal; modulation device is set to AM; filter: 300 Hz...3 kHz; detector: RMS $\sqrt{2}$; readout in dB to reference level of calibration is $a_{S/P}$.

Description of the measurement configuration to measure the residual carrier suppression



Adjust Cp in Circuit 1 and Dynamic Residual Carrier Suppression to Suppression Maximum.

Figure 12

7

Description of the measurement configuration to measure the video amplitude response

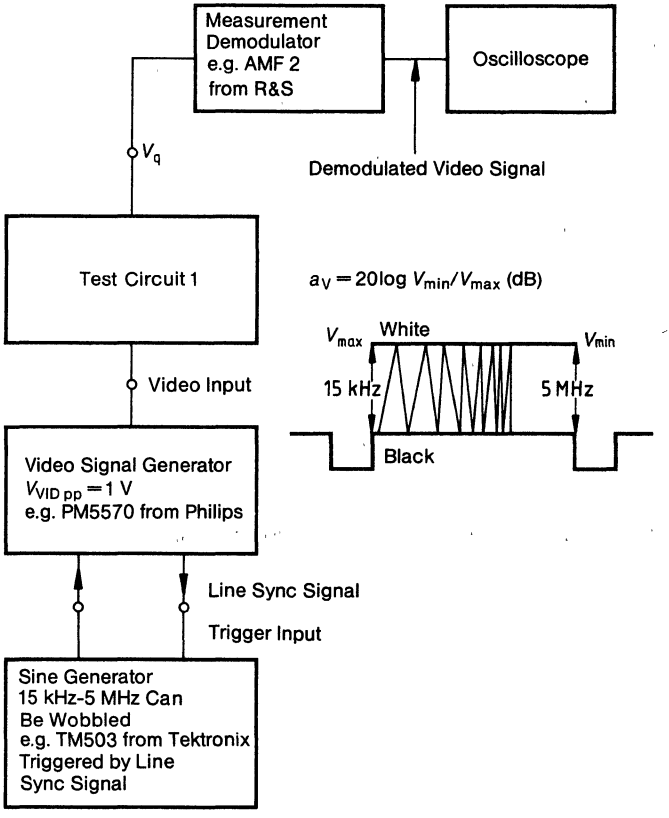
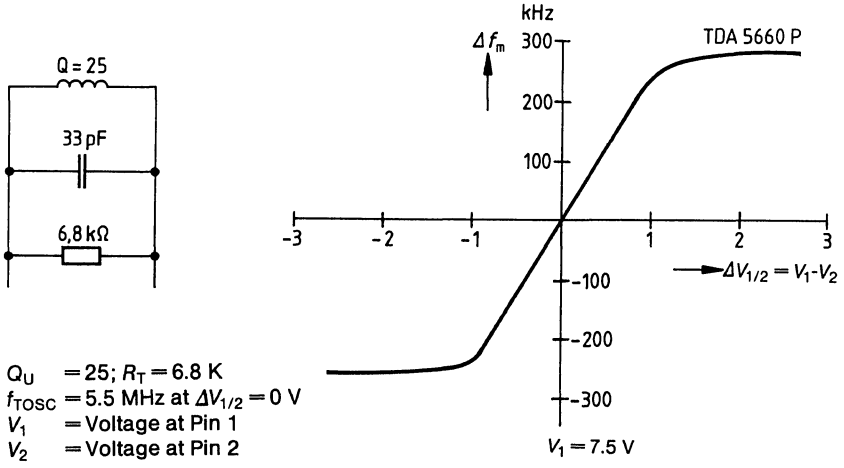


Figure 13

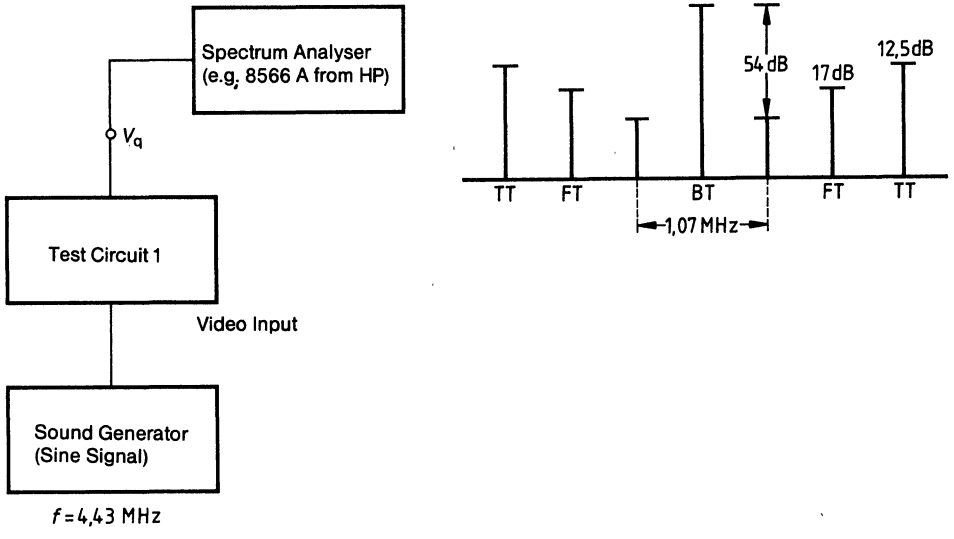
Static modulation characteristic of the FM sound modulator



Q_U = 25; R_T = 6.8 K
f_{TOSC} = 5.5 MHz at $\Delta V_{1/2}$ = 0 V
V_1 = Voltage at Pin 1
V_2 = Voltage at Pin 2

Figure 14

Description of the measurement configuration to measure the 1.07 MHz moires



$V_{VID\ pp}$ = 250 mV: Frequency carrier level lies below the activation point of the video amplitude control and has been set to provide a ratio of 17 dB with respect to the video carrier.

Figure 15

Modulation index during negative video modulation and/or the voltage at pin 12 versus current at pin 12

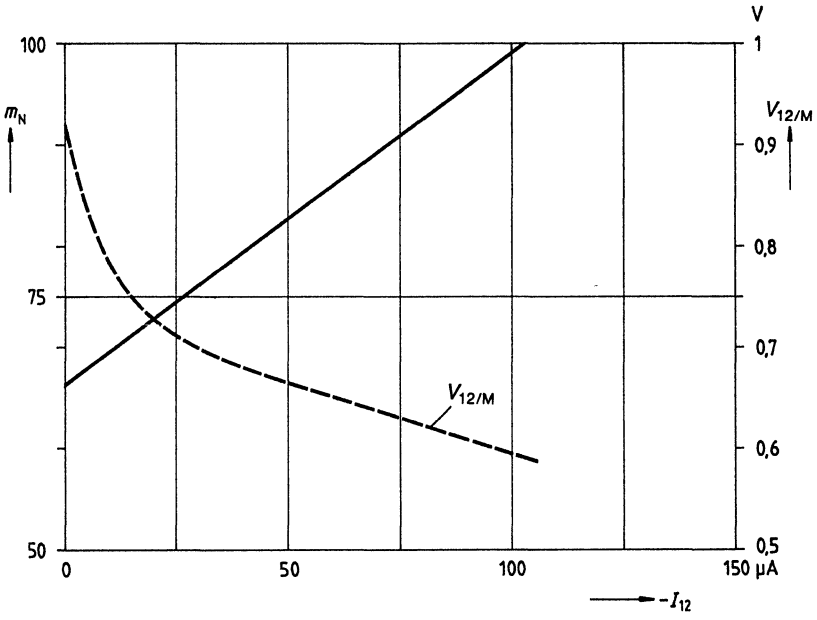


Figure 16a

Modulation depth is calculated as $m_D = (2 \times m)/(1 + m)$ from the modulation index. Prerequisite is a sine-shaped modulation.

m_N = modulation index for negative modulation
m_P = modulation index for positive modulation

If a resistor is connected to ground at pin 12 to adjust modulation depth, the resistor is calculated as $R_{12/M} = (V_{12/M})/I_{12})$.

Modulation index during positive video modulation and/or the voltage at pin 12 versus current at pin 12

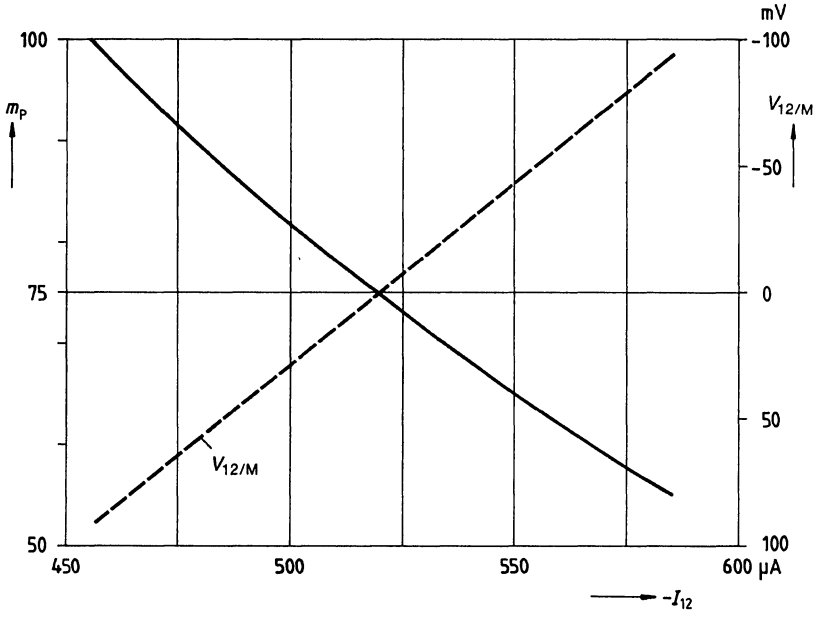


Figure 16

7

Modulation depth is calculated as $m_D = (2 \times m)/(1 + m)$ from the modulation index. Prerequisite is a sine-shaped modulation.

m_N = modulation index for negative modulation
m_P = modulation index for positive modulation

If a resistor is connected to ground at pin 12 to adjust modulation depth, the resistor is calculated as $R_{12/M} = (V_{12/M})/I_{12}$.

Picture to sound carrier ratio versus dc voltage offset at pin 16
unloaded Q factor of resonant circuit $Q_U = 25$, $R_T = 6.8$ k; $f = 5.5$ MHz.
The picture to sound carrier ratio of $a_{P/S} = 13$ dB was set via the loaded Q factor Q_L without external voltage at pin 16.

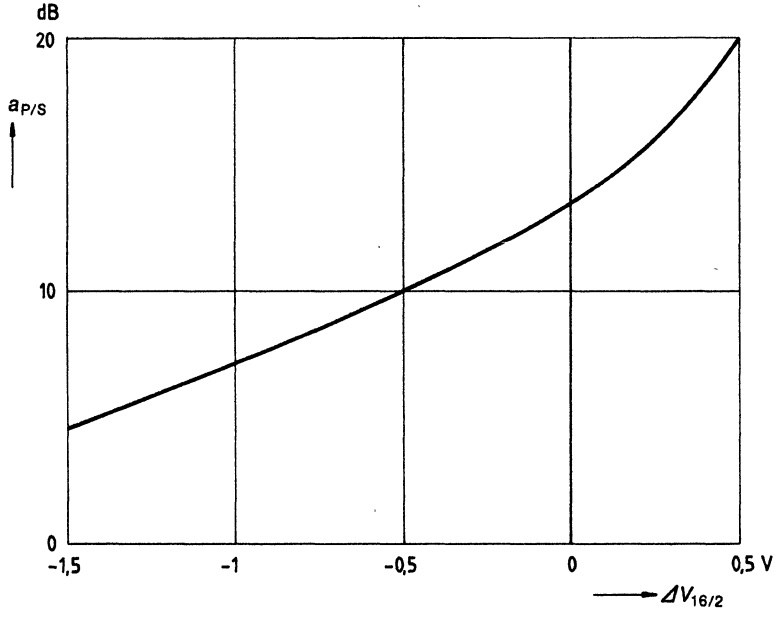


Figure 17

To adjust the picture to sound carrier ratio, a component was used with a resistance of typ. 11.5 kΩ at pins 17, 18.
The loaded Q factor of the resonant circuit was derived from the internal resistance $R_{17/18}$ connected in parallel with the external resistor R_s.

Measurement of the sound oscillator FM deviation without preemphasis and deemphasis; f_{AF} = 1 kHz; modulation deviation, sensitivity $(\Delta f_{AF})/(\Delta V_{AF})$ = 0.38 kHz/mV; V_{AF} = var; detector (P+P)/2; AF filter 30 Hz to 20 kHz, measurement in accordance with CCIR 468-2 DIN 45405; test circuit 1a.

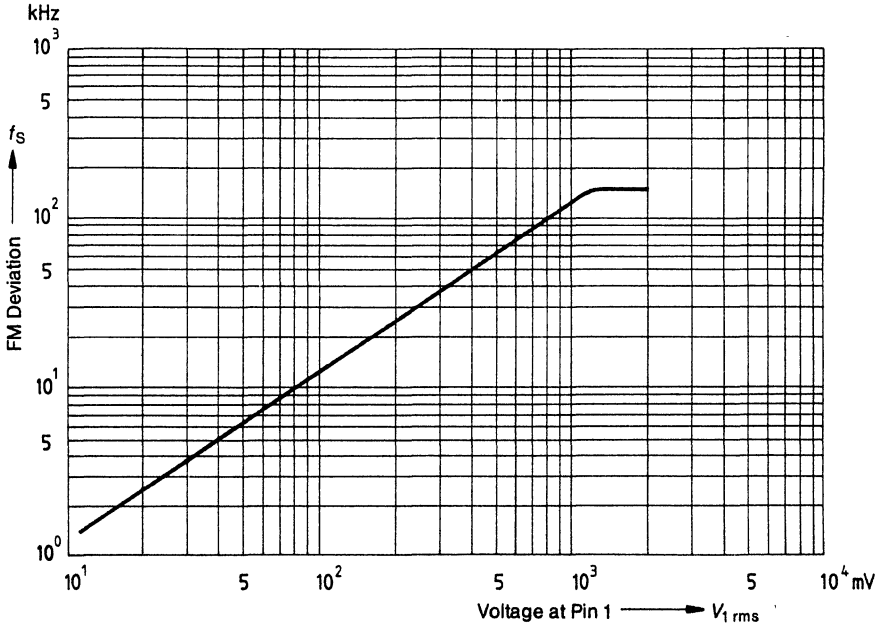


Figure 18

7

Measurement of the sound oscillator FM deviation without preemphasis and deemphasis; f_{AF} = 1 kHz; modulation deviation, sensitivity $(\Delta f_{AF})/(\Delta V_{AF})$ = 0.38 kHz/mV; V_{AF} = var; detector (P+P)/2; AF filter 30 Hz to 20 kHz, measurement in accordance with CCIR 468-2 DIN 45405; test circuit 1a

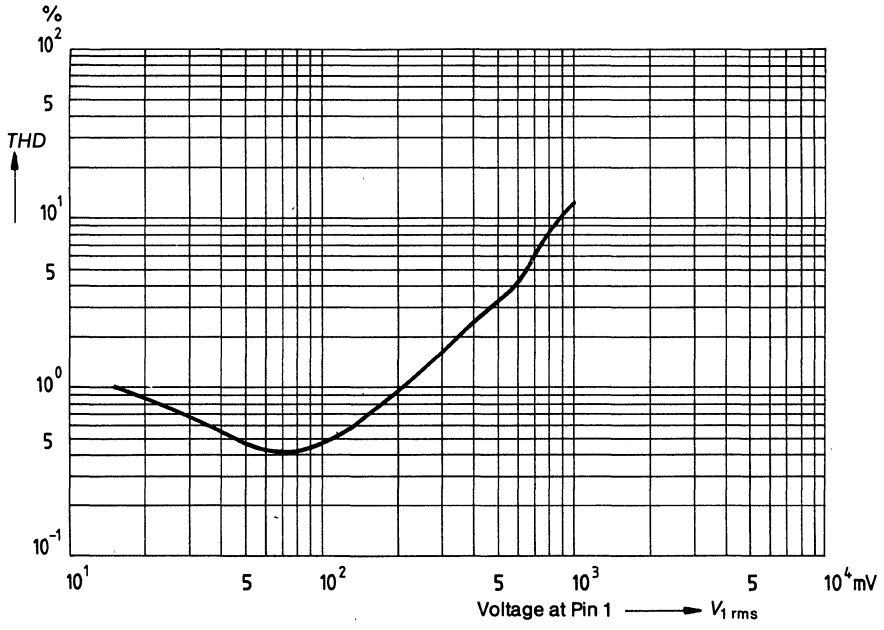


Figure 18a

Sound oscillator harmonic distortion without preemphasis and deemphasis;
AF signal routed in at pin 1; AF amplitude = 150 mV_{rms}; AF filter 30 Hz to 20 kHz; detector $(P+P)/2$; measurement in accordance with CCIR 468-2 DIN 45405; test circuit 1a

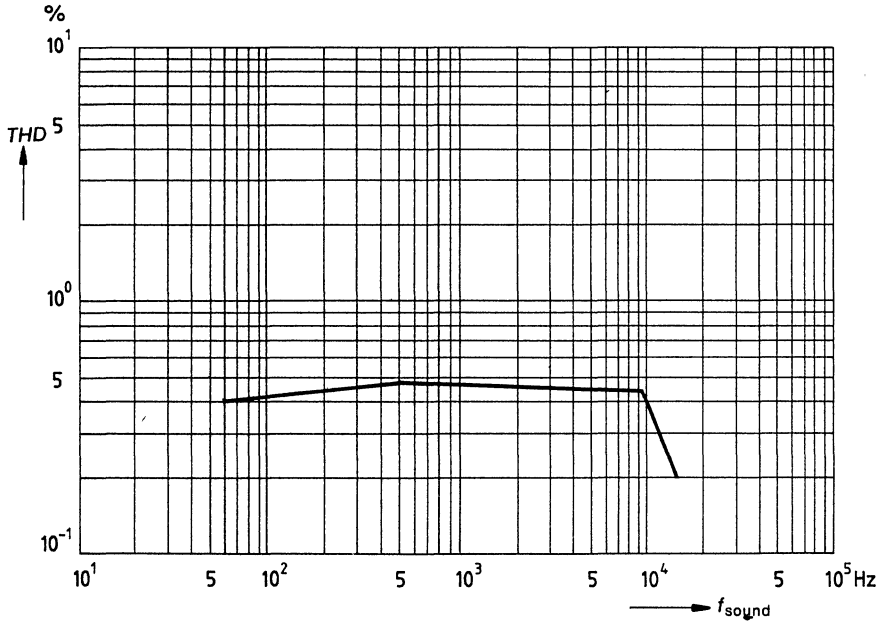


Figure 18 b

Sound oscillator frequency without preemphasis and deemphasis;
AF signal routed in at pin 1; AF amplitude = 150 mV_{rms}; AF filter 30 Hz to 20 kHz; detector $(P+P)/2$; measurement in accordance with CCIR 468-2 DIN 45405; test circuit 1a

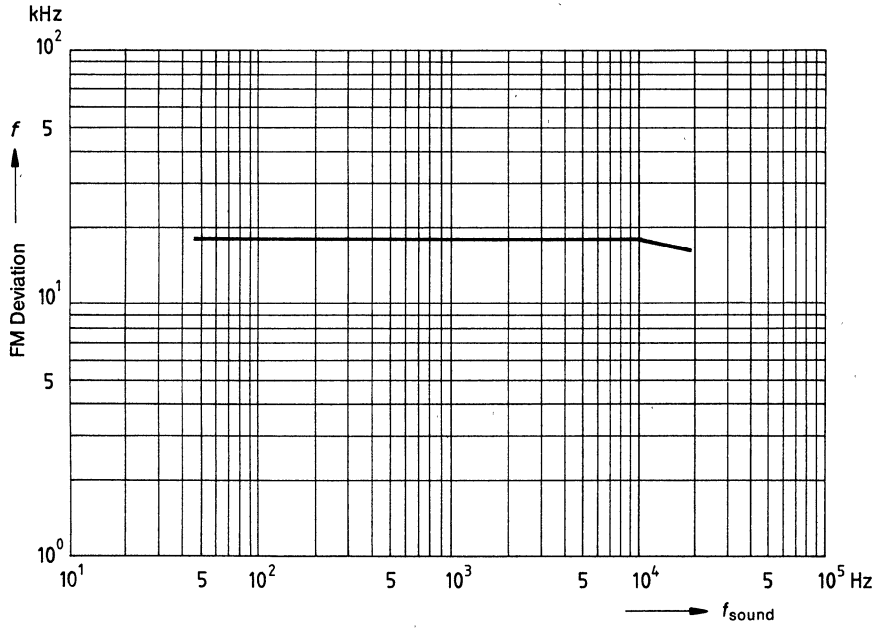


Figure 18 c

Sound oscillator frequency with pre-/deemphasis;
AF filter 30 Hz to 20 kHz; measurement in accordance with CCIR 468-2 DIN 45405; test circuit 1; $V_{AF} = 1\ V_{rms}$

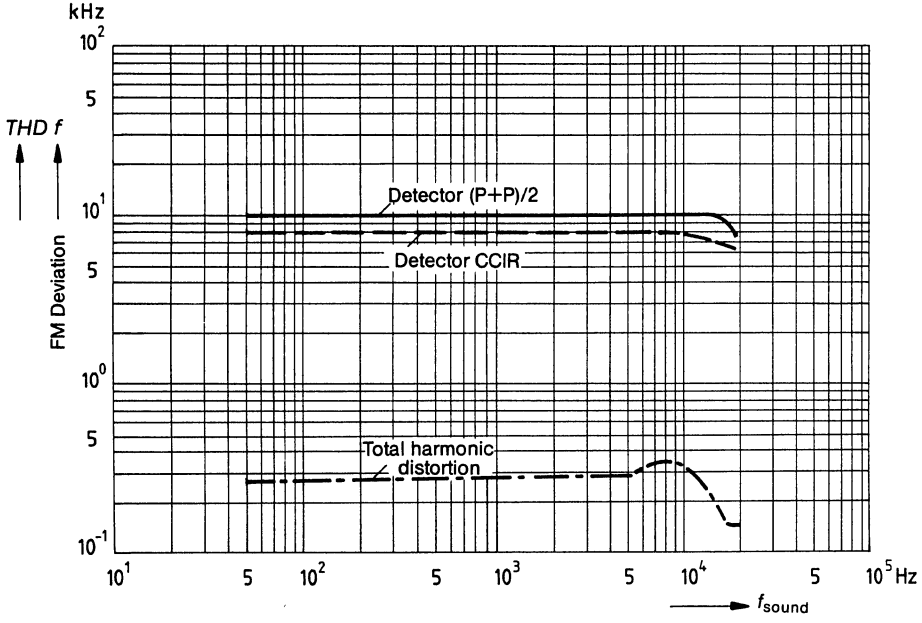


Figure 18 d

7

Description of the measurement configuration to measure the video signal control characteristics and the dynamic signal suppression in video frequencies

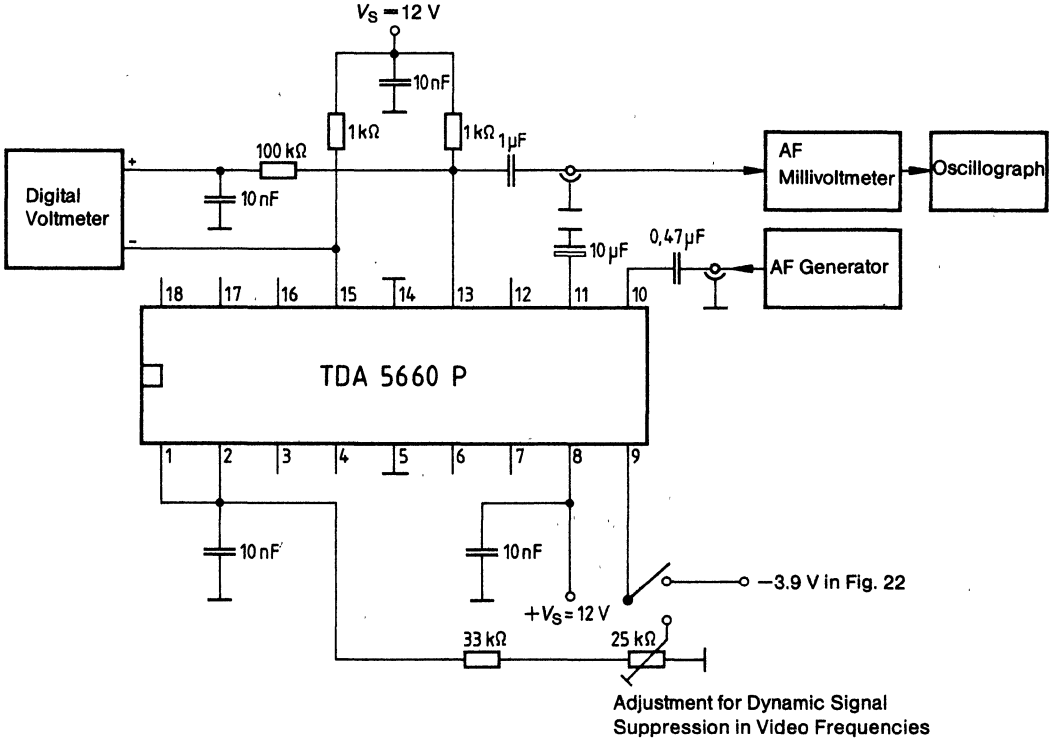
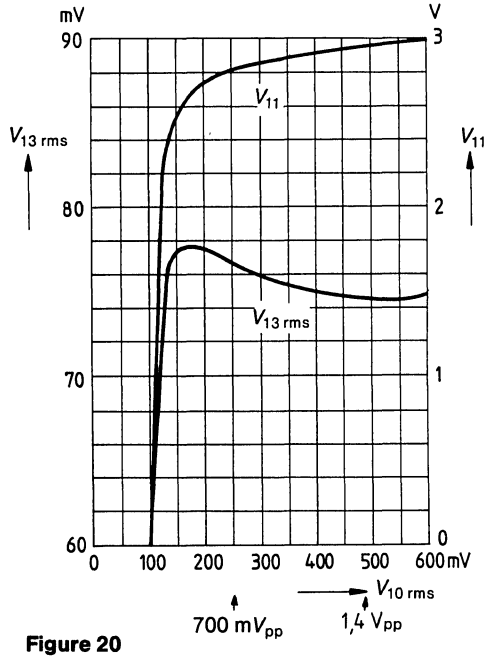


Figure 19

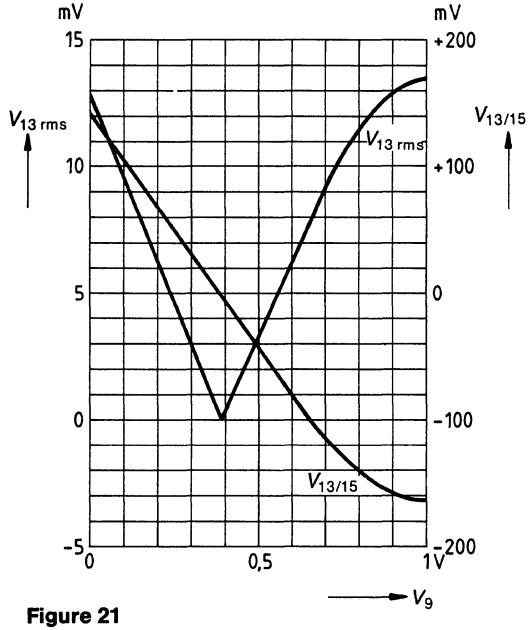
Characteristic of the video signal control circuit



a) $V_{13\,rms} = f(V_{10\,rms})$; $f_{mod} = 100$ kHz
b) $V_{11} = f(V_{10\,rms})$; $V_9 = 3.9$ V

Figure 20

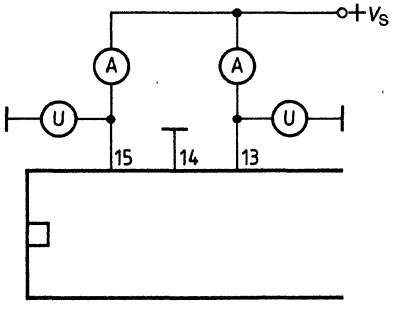
Static and dynamic mixer test with respect to balance characteristics based on a typical component



$V_{13/15} = f(V_9)$
$V_{13\,rms} = f(V_9)$
$f = 10$ kHz

Figure 21

Measurement of the static output impedance



$$Z_{15} = \frac{\Delta V_{15}}{\Delta I_{15}}$$

$$Z_{13} = \frac{\Delta V_{13}}{\Delta I_{13}}$$

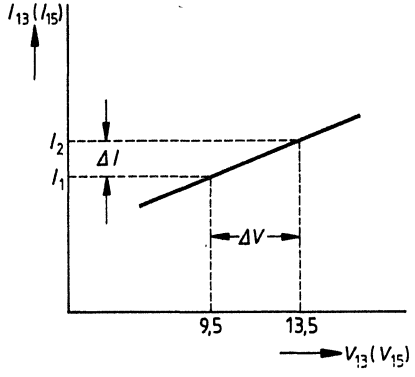
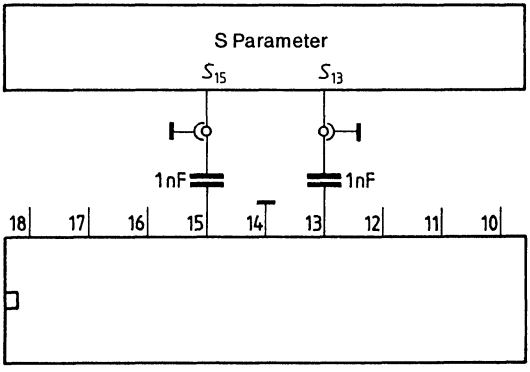


Figure 22

Output circuit S parameter



Typ. output capacity is approx. 1 pF

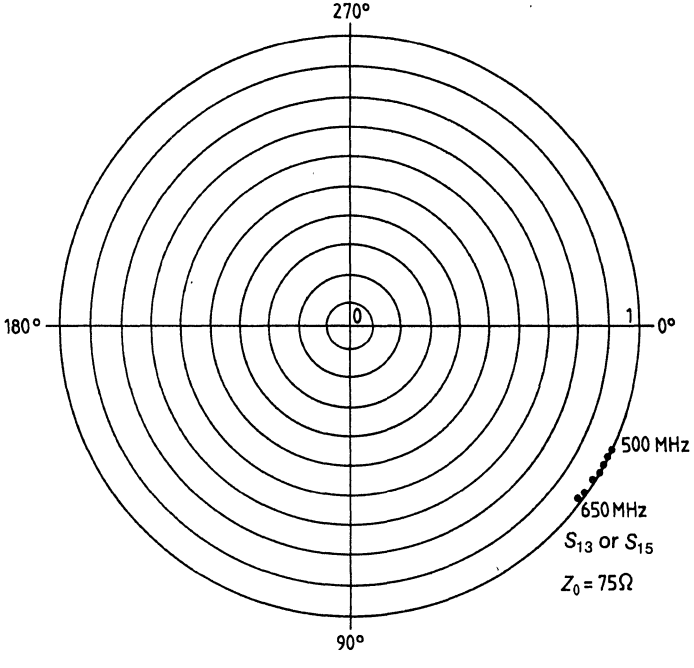
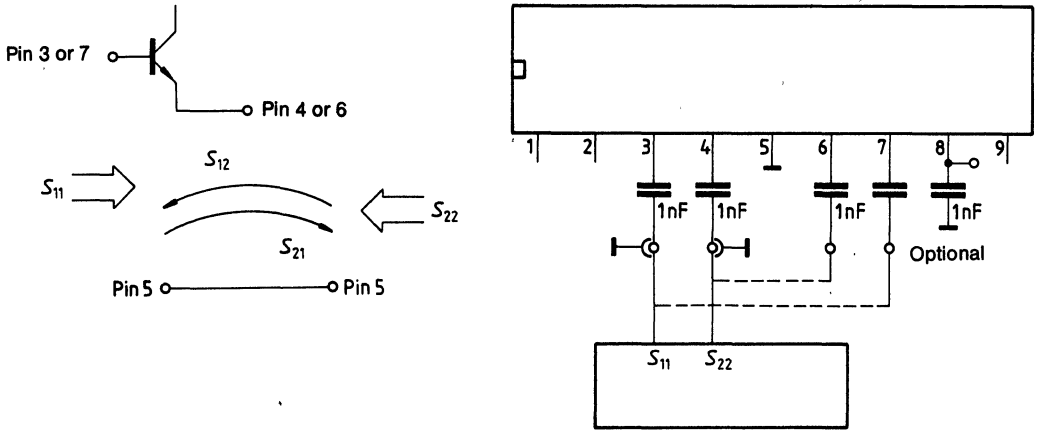


Figure 23

Oscillator section S parameter



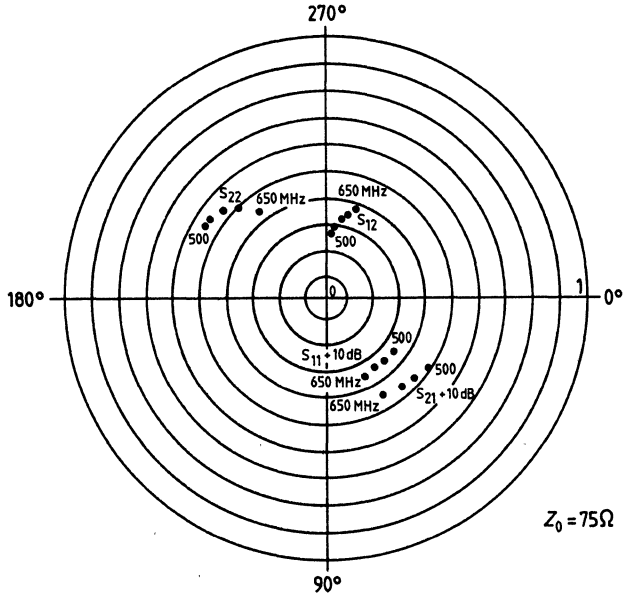
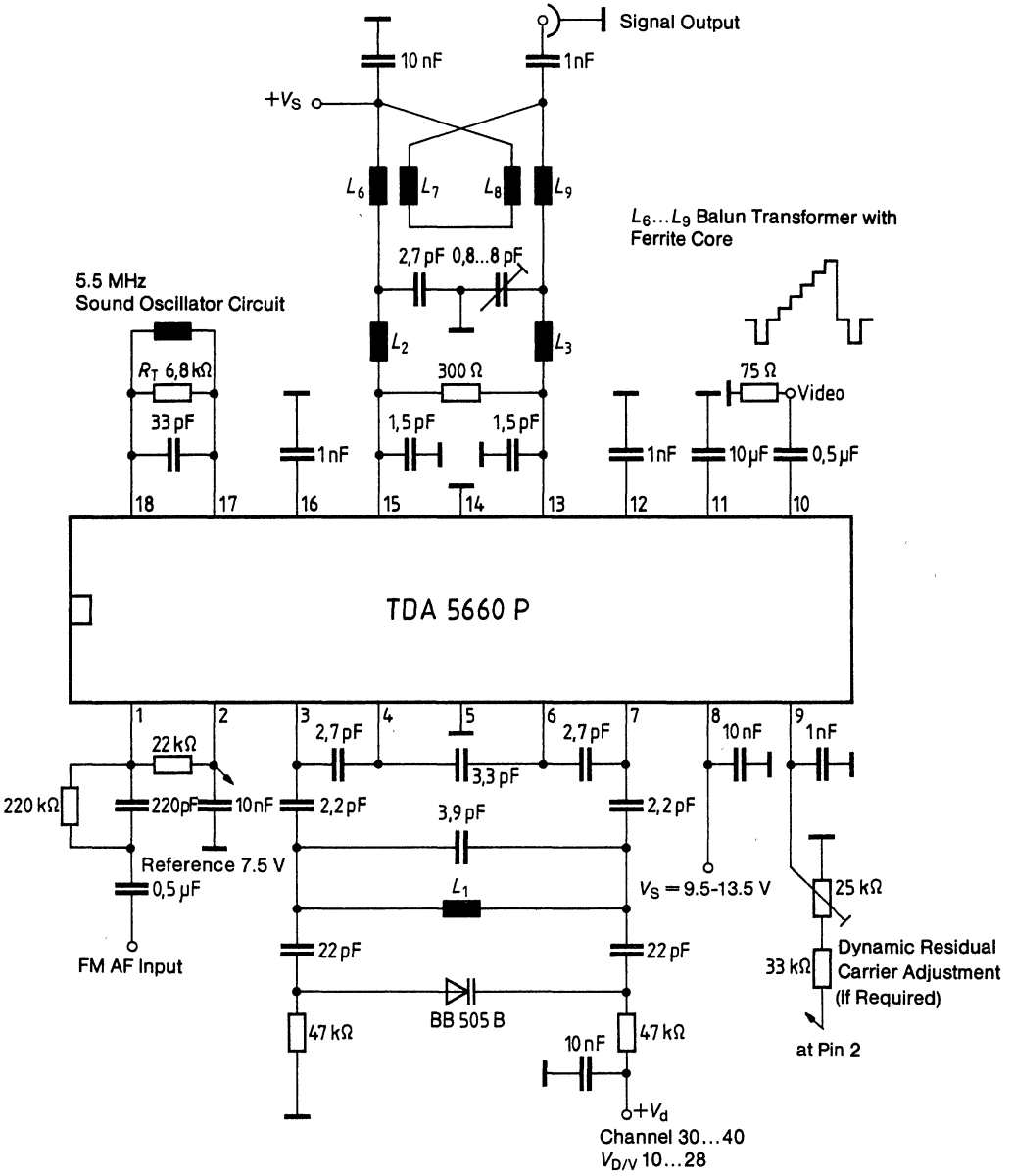


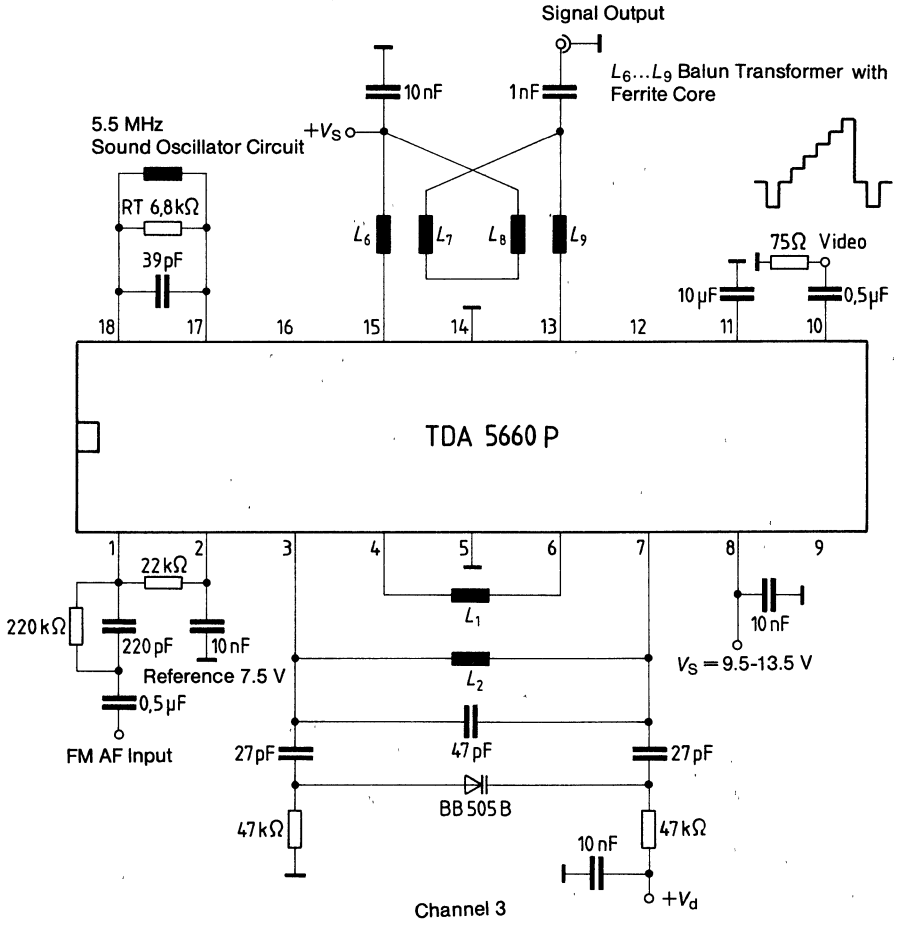
Figure 24

Application circuit 1

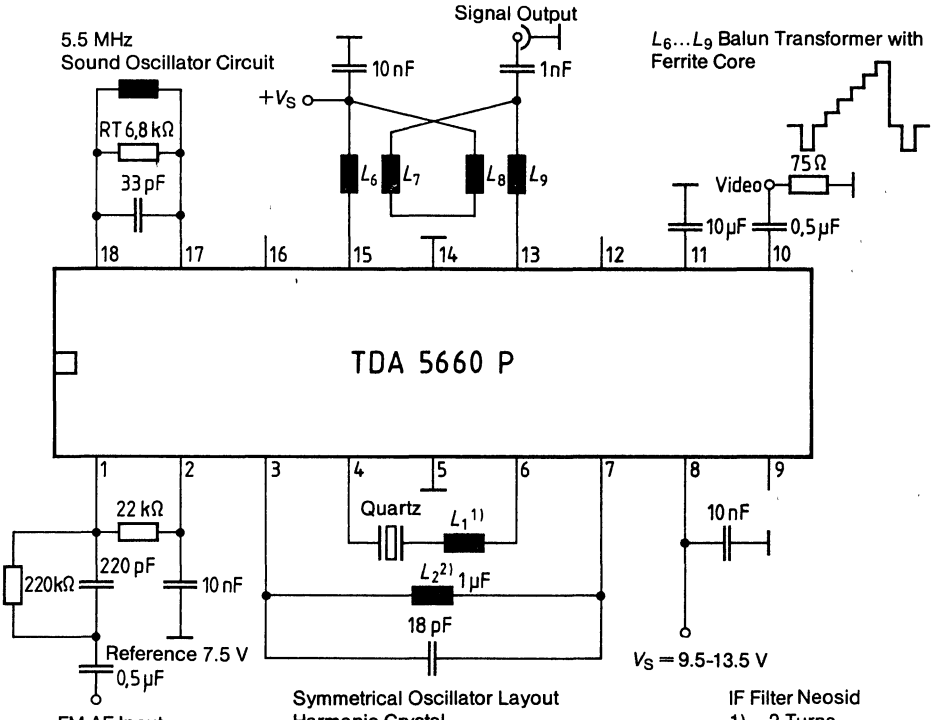


7

Application circuit 2



Application circuit 3



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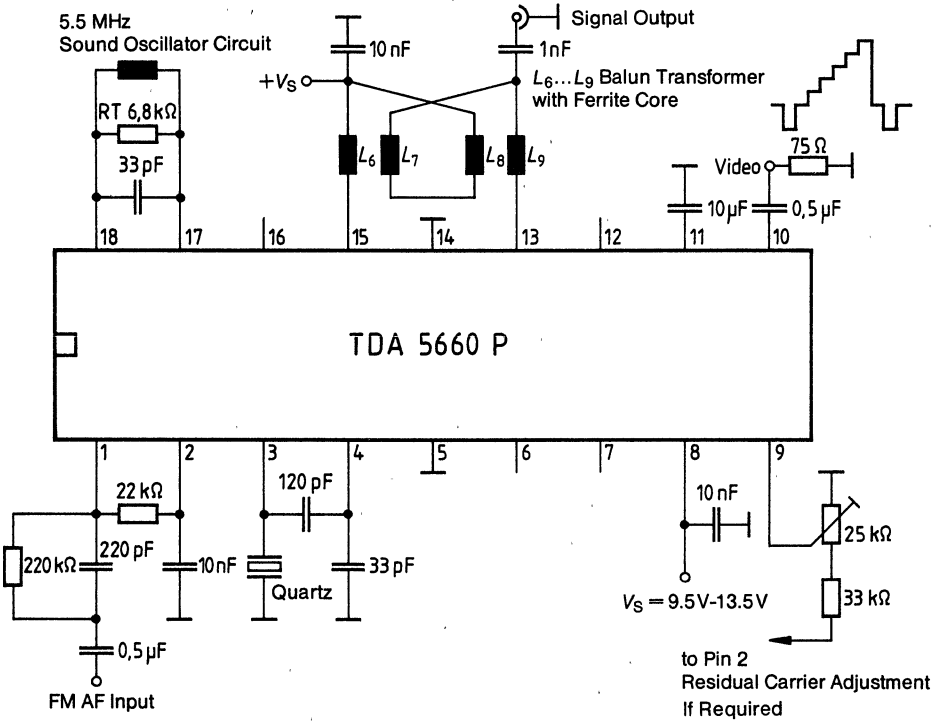
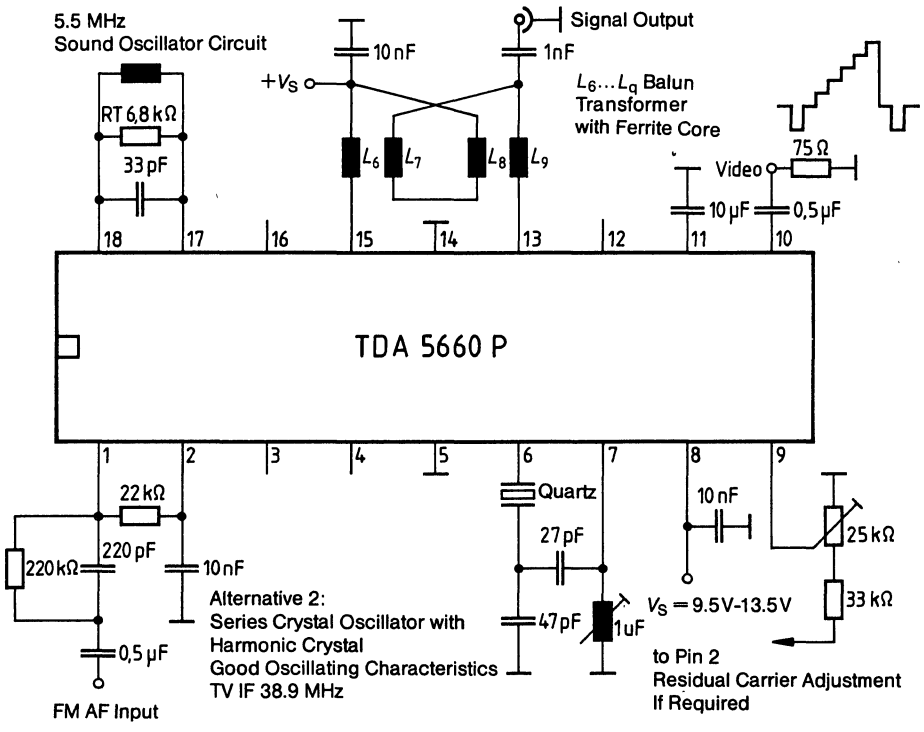
Application circuit 4

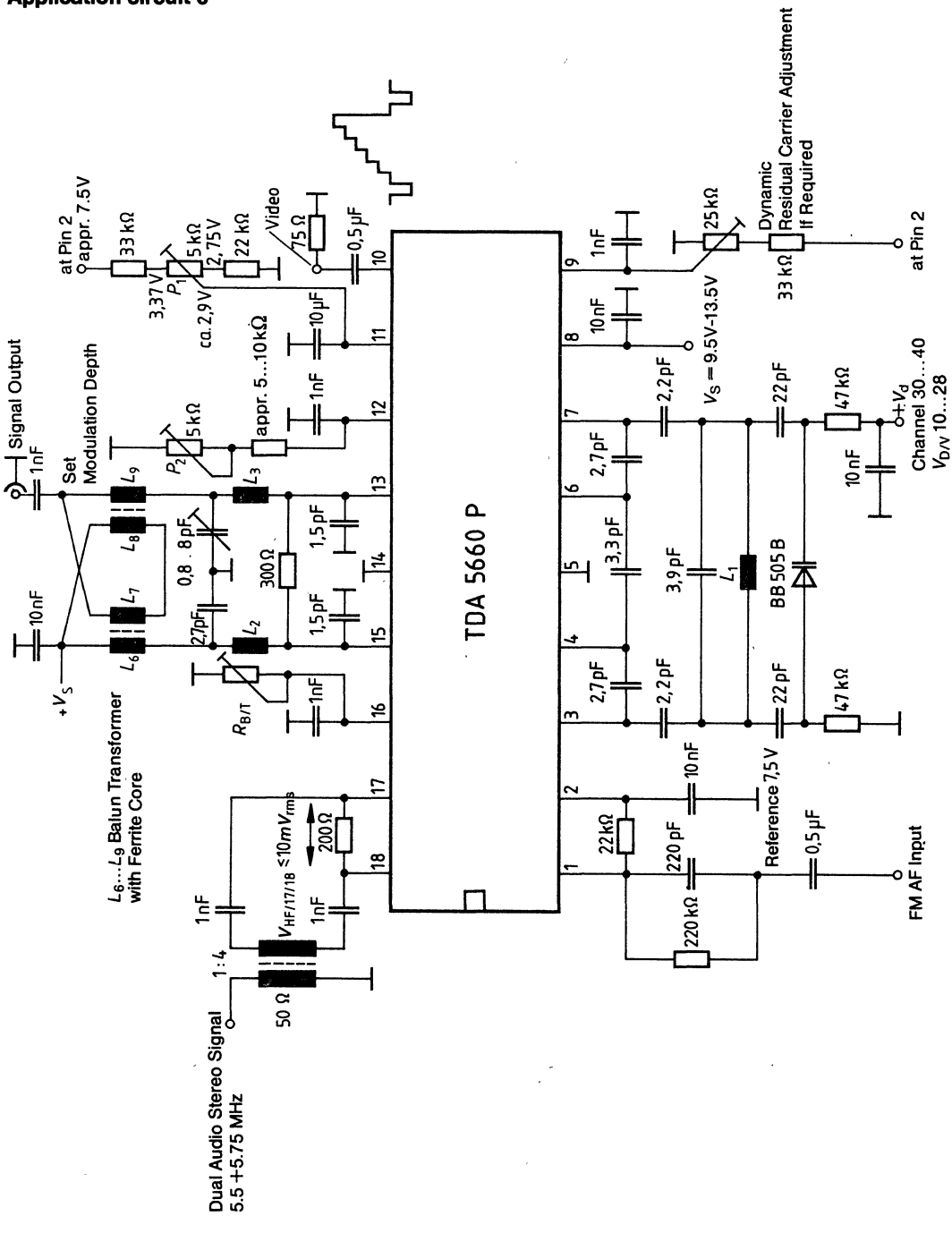


Application circuit 5



7

Application circuit 6

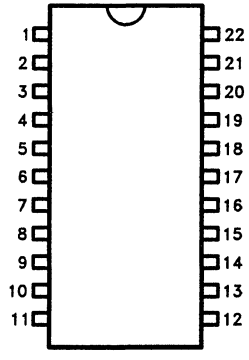


SIEMENS

TDA 5835
Video IF IC with Quasi-Parallel Sound and AFC

Pin Configuration

Top View



0157-18

Pin Definitions

Pin	Function
1	Supply Voltage
2	Demodulator Tank Circuit QPS
3	Demodulator Tank Circuit QPS
4	Push-Pull Current Output AFC
5	Demodulator Tank Cirucit AFC
6	Demodulator Tank Circuit AFC and Switch-Off
7	Tuner AGC Threshold
8	Reference Voltage
9	Demodulator Tank Circuit Video IF
10	Demodulator Tank Circuit Video IF
11	Video Output
12	Gating Pulse Input
13	AGC Time Constant Video IF
14	Delayed Tuner AGC
15	Video IF Input
16	Video IF Input
17	GND
18	QPS IF Input
19	QPS IF Input
20	AGC Time Constant QPS
21	Sound Carrier Output
22	GND

7

Video IF Section

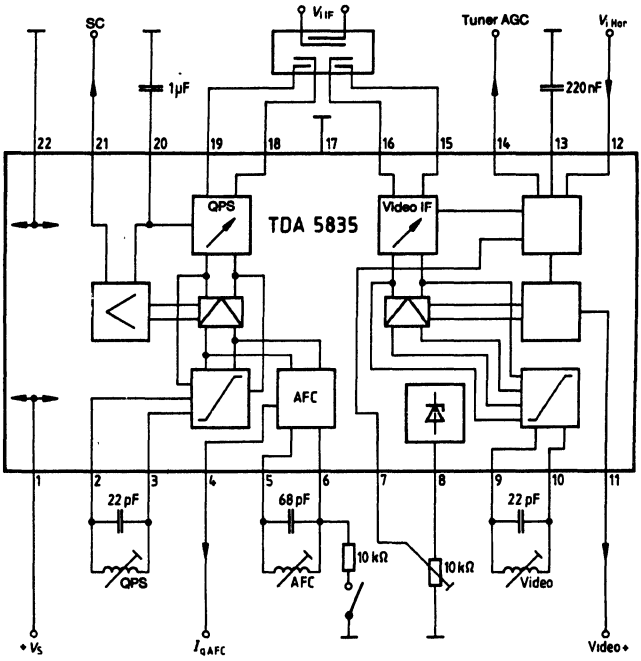
Controlled AM broadband amplifier with synchronous demodulator, video amplifier, and AGC voltage generation for the video IF amplifier and tuner.

Quasi-Parallel Sound Section

Controlled AM broadband amplifier with quadrature demodulator, sound carrier output, internal AGC voltage generation, and an AFC section which can be disabled.

The TDA 5835 is especially suitable for application with black and white or color television receivers and/or VTR systems with PNP/MOS tuners for TV standards with negative video modulation and FM sound.

Block Diagram



Circuit Description

The video IF section is comprised of a 4-stage controllable AM amplifier, a limiter, and a mixer for the synchronous demodulation of video signals as well as an amplifier for the positive video output signal. The positive signal is used for gated control and a threshold amplifier to derive the delayed tuner AGC from the AGC voltage.

The quasi-parallel sound section also includes a 4-stage AM amplifier, a limiter, and a mixer for the quadrature demodulation of the 1st sound IF with subsequent sound carrier output for the 1st sound IF. The control voltage is generated by a peak value rectifier from the 2nd sound IF signal. The quasi-parallel sound also drives the AFC section.

Alignment Procedures

VIDEO IF

At a video carrier input level of $V_{15/16\,rms}$ = 10 mV and a superimposed AGC voltage of V_{13} = 3V, the demodulator tank circuit is preliminarily aligned so that the demodulated video signal V_{11pp} reaches its maximum output level at the positive video output.

Any suitable video test signal can be used for modulation. Subsequently, the AGC voltage V_{13} is reduced until the video signal equals approx. 3V (peak-to-peak). By fine-aligning the demodulator tank circuit, the maximum output level of the video signal is reached.

The flat response characteristic of the demodulator ensures a non-critical alignment procedure.

QPS

At an input signal of $V_{18/19\,rms}$ = 10 mV the demodulator tank circuit is preliminarily aligned until a max. AM suppression of the demodulated video signal V_{21} is reached at the sound carrier output. A video signal critical for the sound-interference ratio should be used for modulation (white/staircase, FuBK). Subsequent fine-aligning is performed by measuring the sound-interference ratio at the output of a FM demodulator and fine-aligning the demodulator tank circuit for a max. interference ratio. If several sound carriers are used in a device, the sound carrier with the lowest level should be used for alignment purposes.

Absolute Maximum Ratings*

Supply Voltage (V_1) 13V
Maximum DC Voltage ($V_{2,3}$) ..... V_8 to V_1
Maximum DC Voltage (V_4) ..... 0V to V_1
Maximum DC Voltage ($V_{5,6}$) ..... V_8 to V_1
Maximum DC Voltage (V_7) ..... 0V to V_1
Maximum DC Current (I_8) ..... −2 mA to +2 mA
Maximum DC Voltage ($V_{9,10}$) ..... V_8 to V_1
Maximum DC Current ($-I_{11}$) ..... −1 mA to +3 mA
Maximum DC Voltage (V_{12}) ..... −10V to V_1
Maximum DC Voltage ($V_{13,14,15}$) ..... 0V to V_1
Maximum DC Voltage ($V_{16,18}$) ..... 0V to V_1
Maximum DC Voltage ($V_{19,20}$) ..... 0V to V_1
Maximum DC Current (I_{21}) ..... −1 mA to +2 mA
Junction Temperature (T_j) ..... 150°C
Storage Temperature
Range (T_{stg}) ..... −40°C to +125°C
Thermal Resistance
(System-Air) ($R_{th\ SA}$) ..... 55 K/W

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Operating Range

Supply Voltage (V_S) ..... 10.5V to 12.6V
IF Frequency (f_{IF}) ..... 15 MHz to 75 MHz
Ambient Temperature (T_A) ..... 0°C to +70°C

Characteristics V_S = 12V; T_A = 25°C

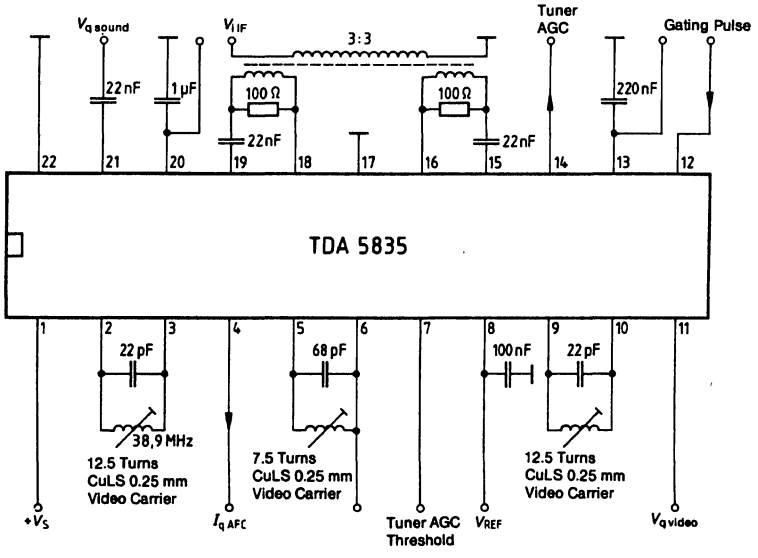
Parameter	Symbol	Conditions	Min	Typ	Max	Units
Current Consumption	I_1			102	134	mA
Stab. Reference Voltage	$V_{8/22}$			6.7	7.0	V
Video IF						
Control Current for Tuner	I_{14}			4.5		mA
Tuner AGC Threshold	$V_{7/22}$		0		4.0	V
Gating Pulse Voltage	V_{12} V_{12}	Positive Gating Pulse Negative Gating Pulse	4.0 −10		V_1 −4.0	V V
Input Voltage at G_{max}	$V_{i\ 15/16}$	$V_{11\ pp}$ = 3V		30	60	μV
AGC Range	ΔG			60		dB
IF Control Voltage	$V_{13/22}$ $V_{13/22}$	G_{max} G_{min}	0		 4.0	V V
Video Output Voltage	$V_{q\ 11\ pp}$	R_L = ∞		3.0		V
Sync Pulse Level	$V_{11/22}$			2.0		V
DC Voltage						
V_{13} = 4V; $V_{15/16}$ = 0V	$V_{11/22}$			5.3		V
Output Current	$I_{q\ 11}$ $I_{q\ 11}$	to ground via R to plus V_{11} = 7V		−5.0 +2.0		mA mA

7

Characteristics V_S = 12V; T_A = 25°C (Continued)

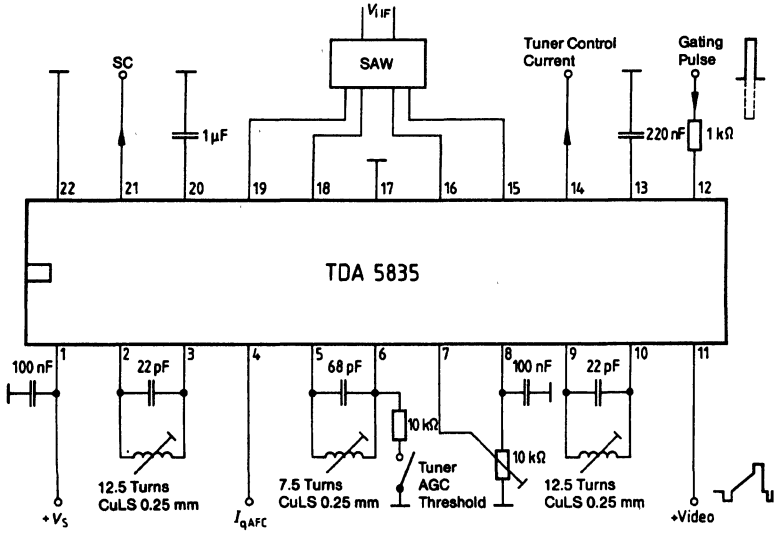
Parameter	Symbol	Conditions	Min	Typ	Max	Units
AFC Output Current	I_{q4}	di/df < 0		±1		mA
AFC OFF	$V_{5/22}$	$V_5 = V_6$; R = 10 kΩ	0		4.0	V
ON	$V_{5/22}$	$V_5 = V_6$; R = ∞		6.0		V
Quasi-Parallel Sound						
Sound Carrier Output Voltage	V_{q21}	V_{iPC} = 1 mV V_{iSC} = 300 μV	10			mV
Input Voltage at G_{max}	$V_{i18/19}$	$V_{21} = V_{21}$ −3 dB		50	100	μV
AGC Range	ΔG	$V_{21} = V_{21}$ ±3 dB		60		dB
Signal-To-Noise-Ratio		IEC 468				
White/Staircase Signal		Peak Weighting		61		dB
Black Picture				66		dB
Test Conditions						
Video Carrier/Sound Carrier				10		dB
Modulation Frequency				1		KHz
Frequency Deviation				50		KHz
IF Input Voltage				20		mV
Design-Related Characteristics						
Input Impedance	$Z_{i15/16}$ $Z_{i18/19}$			1.8/2 1.8/2		kΩ/pF kΩ/pF
Output Impedance	$Z_{q2/3}$ $Z_{q9/10}$ $Z_{q5/6}$			6.6/2 6.6/2 20		kΩ/pF kΩ/pF kΩ
Output Resistance	R_{q11}			150		Ω
Residual IF (Fundamental Wave)	V_{11}			10		mV
Video Bandwidth (−3 dB)	B_{video}			6.0		MHz
Intermodulation Ratio with Reference to f_{CC}	α_{IM}	Sound Color Interference		50		dB
Output Resistance	R_{q21}			200		Ω
IF Control Voltage	$V_{20/22}$ $V_{20/22}$	G_{max} G_{min}	0		 4	V V

Measurement Circuit



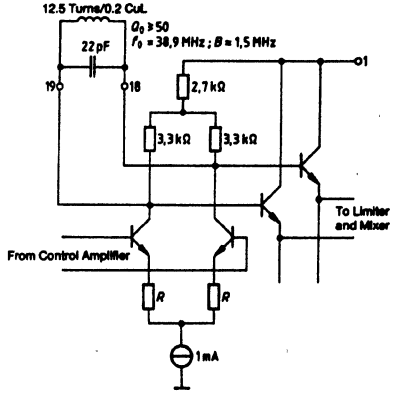
0157-2

Application Circuit

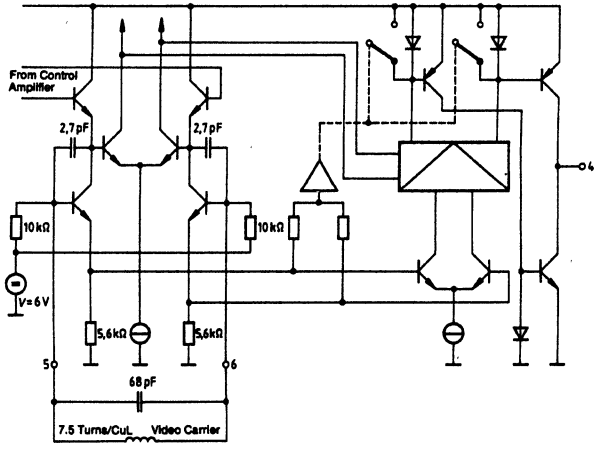


0157-3

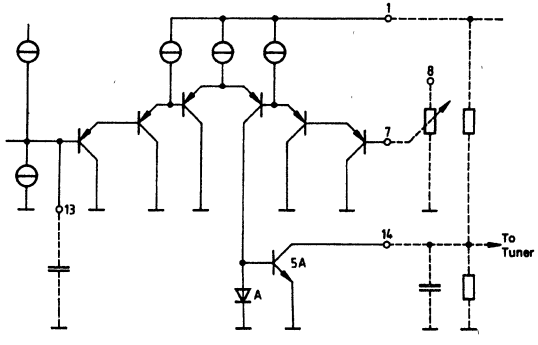
Demodulator Tank Circuit QPS



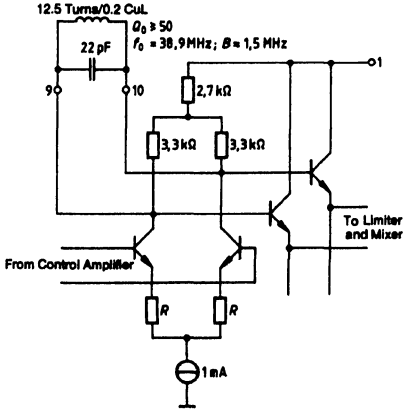
Demodulator Tank Circuit AFC



Tuner AGC Threshold and Output

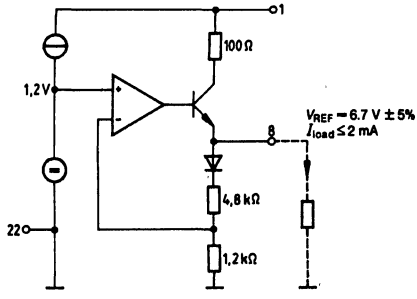


Demodulator Tank Circuit Video IF



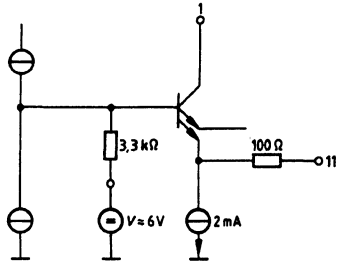
0157-8

Reference Voltage



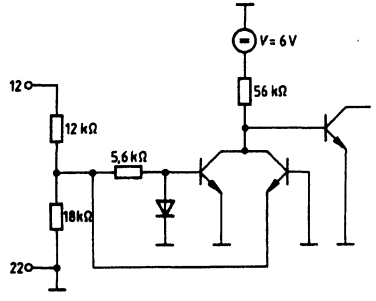
0157-7

Positive Video Output



0157-9

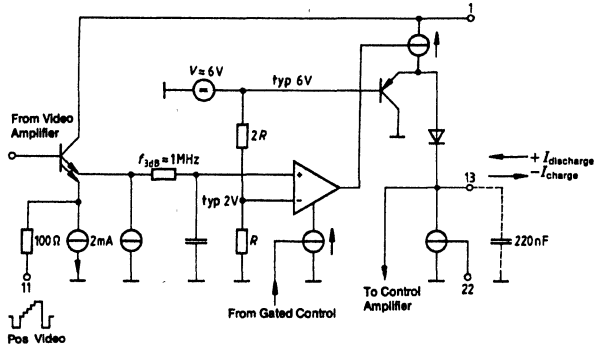
Gating Pulse Input



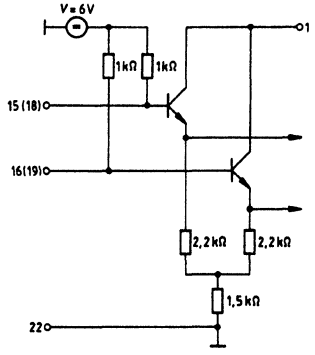
0157-10

7

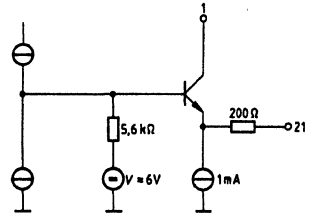
AGC Time Constant Video IF



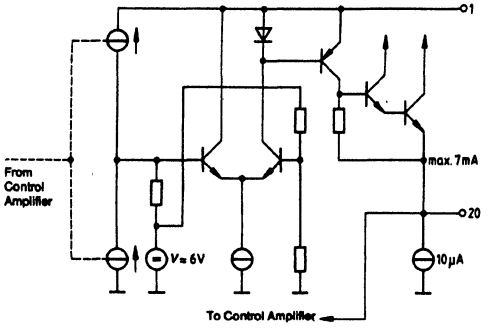
IF Input Video IF
IF Input QPS



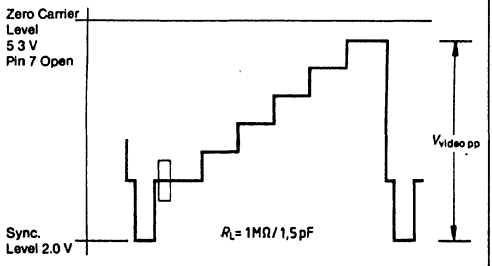
Sound Carrier Output QPS



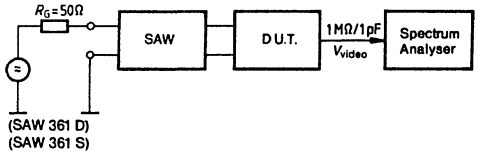
AGC Time Constant QPS



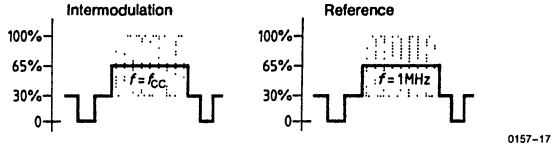
Positive Video Output



Measurement Configuration



Test signal: f_{VC} = 38.9 MHz with test signal modulated with 10% residual carrier; sound carrier −13 dB (Transmitter Side)



Intermodulation ratio: $a_{IM} = 20 \log \frac{V_{video}\,(f = 1\,MHz)}{V_{video}\,(f = f_{SC} - f_{CC})}$

The 50% IRE signal with ±50% IRE color carrier corresponds to Cyan with 75% color saturation.

Ordering Information

Type	Ordering Code	Package

7

SIEMENS

TDA 5850
Video Switch IC

The TDA 5850 is a switchable video amplifier with connections for the French and IEC VCR standards.

Features

- Standard connection for VCR (CCIR) and Peri TV sets
- Input clamping
- Positive and negative video outputs

Maximum ratings

Supply voltage	V_S	16.5	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\,SA}$	70	K/W

Operating range

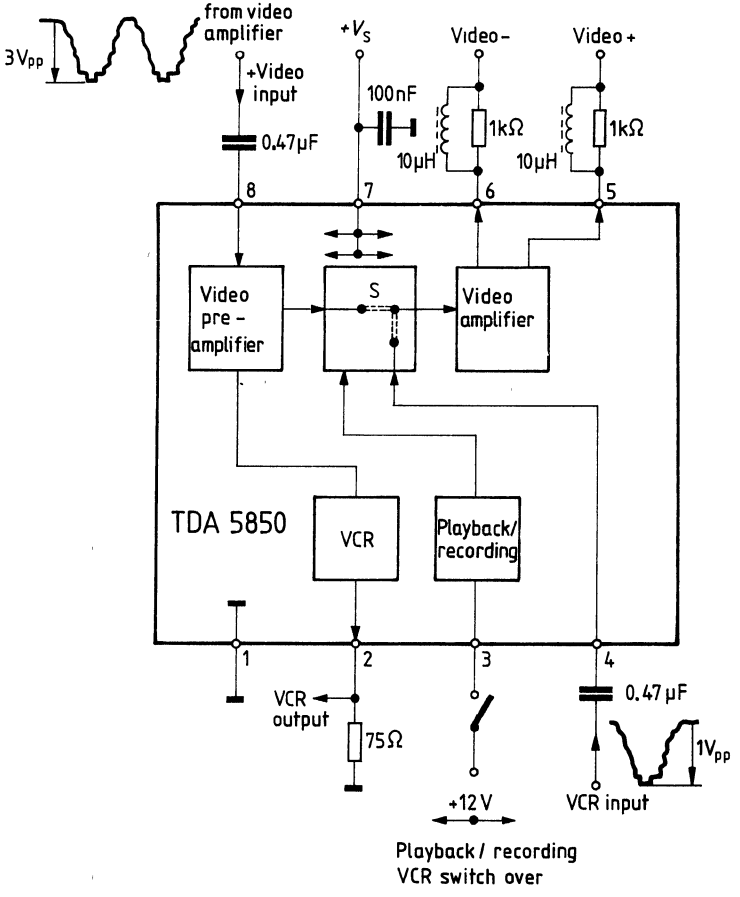
Supply voltage range	V_S	10 to 15.8	V
Video bandwidth	B_{video}	6	MHz
Ambient temperature range	T_{amb}	0 to 70	°C

Characteristics ($V_S = 13$ V; $T_{amb} = 25$ °C)

		min	typ	max	
Current consumption (pin 2 open)	I_7		23.0		mA
Switch input VCR recording	$V_{3/1}$	0		1.2	Vdc
Switch input VCR playback	$V_{3/1}$	3.0		V_7	Vdc
Switch input $V_{3/1} = 15$ V	I_3			1.0	mA
Video output voltage pos. ($V_3 = 1.2$ V; $V_{8\,pp} = 3$ V)	$V_{5\,pp}$		3.0		V
Video output voltage pos. ($V_3 \geqq 3$ V; $V_4 = 1$ V_{pp})	$V_{5\,pp}$		3.0		V
Sync pulse level	$V_{5/1}$		2.0		Vdc
Output current (to ground)	I_5		–5.0		mA
Output current (to +)	I_5		2.0		mA
Output resistance	R_5		150		Ω
Video output voltage neg. ($V_3 = 1.2$ V; $V_8 = 3$ V_{pp})	$V_{6\,pp}$		3.0		V
Video output voltage neg. ($V_3 \geqq 3$ V; $V_4 = 1$ V_{pp})	$V_{6\,pp}$		3.0		V
Sync pulse level	$V_{6/1}$		V_7–2		Vdc
Output current (to ground)	I_6		–5.0		mA
Output current (to +)	I_6		1.0		mA
Output resistance	R_6		150		Ω
Video output voltage pos. ($V_{8\,pp} = 3$ V; $R_{2/1} = 75$ Ω)	$V_{2\,pp}$		1.0		V
Sync pulse level ($R_{2/1} = 75$ Ω)	$V_{2/1}$		1.0		Vdc
Output current (to ground)	I_2		–30.0		mA
Output current (to +)	I_2		2.0		mA
Output resistance	R_2		75		Ω
Video input current ($V_{8\,pp} = 3$ V)	I_8			40	µA
Video input current ($V_{4\,pp} = 1$ V)	I_4			20	µA
Video gain ($V_{8\,pp} = 3$ V; $R_{2/1} = 75$ Ω)	$G_{2/8}$		1/3		
Video gain ($V_{8\,pp} = 3$ V; $V_3 = 1.2$ V)	$G_{5/8}$		1		
Video gain ($V_{8\,pp} = 3$ V; $V_3 = 1.2$ V)	$G_{6/8}$		–1		
Video gain ($V_{4\,pp} = 1$ V; $V_3 \geqq 3$ V)	$G_{5/4}$		3		
Video gain ($V_{4\,pp} = 1$ V; $V_3 \geqq 3$ V)	$G_{6/4}$		–3		
Video bandwidth (–3 dB)	B_{video}	6.0			MHz
Cross talk rejection referred to $V_{5\,pp} = 3$ V ($f = 50$ Hz . . 6.0 MHz; $V_3 = 1.2$ V; $V_{4\,pp} = 1$ V)	a		50		dB

7

Block diagram, test circuit and application circuit



SIEMENS

Preliminary

TUA 2005
Bipolar Television Tuner IC for Frequency Ranges up to 700 MHz

RF Section

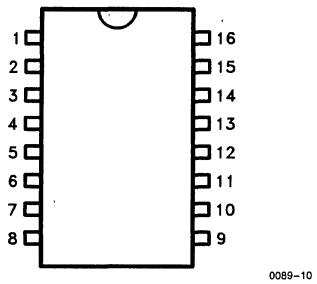
- Few External Components
- Frequency and Amplitude-Stable Oscillator
- Optimal Suppression of Oscillator and Input Frequency at IF Output
- High Resistance to Interference Voltages
- High-Impedance Symmetrical Mixer Input
- IF Post-Amplifier for UHF-IF Signal
- Symmetrical Mixer Output
- Low-Noise, Internal Reference Voltage

IF SAW Driver Section

- Optimal Crosstalk Suppression
- High-Impedance, Asymmetrical Input with High Signal Modulation Capability
- Low-Impedance Symmetrical Output for Driving SAW Filters

Pin Configuration

(Top View)



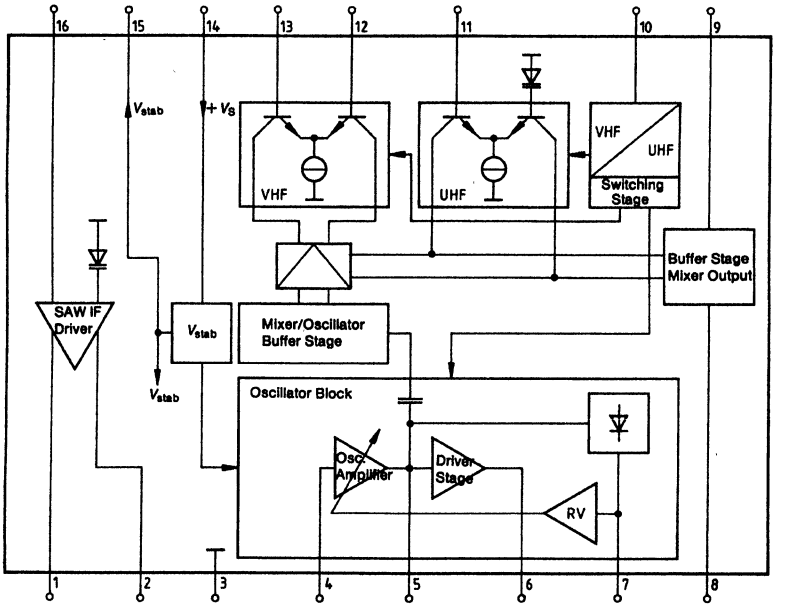
Pin Definitions

Pin	Function
1	Low-Impedance Symmetrical Output of SAW Driver
2	Low-Impedance Symmetrical Output of SAW Driver Anti-Phased to Pin 1
3	GND
4	High-Impedance Input of Oscillator Amplifier
5	Low-Impedance Output of Oscillator Amplifier
6	Oscillator Signal Output for PLL Systems with Possible Open Collector Output
7	Blocking Capacitor for Controlling Oscillator Amplitude
8	Symmetrical Mixer Output
9	Symmetrical Mixer Output Anti-Phased to Pin 8
10	Switching Voltage Input for VHF/UHF Switch-Over
11	High-Impedance Asymmetrical RF Input for UHF-IF Signal
12	High-Impedance Symmetrical RF Input of VHF Mixer
13	High-Impedance Symmetrical RF Input of VHF Mixer, Anti-Phased to Pin 12
14	Supply Voltage
15	Blocking Point of Internal Reference Voltage
16	High-Impedance Asymmetrical IF Input of SAW Driver

7

The TUA 2005 has been designed as a monolithically integrated circuit suitable as a TV tuner for a CATV frequency range extended to 700 MHz.

Block Diagram



Circuit Description

RF Section

The integrated circuit includes a symmetrical high-impedance, low-noise mixer input and a multiplicative mixer.

The amplitude of the oscillator is controlled for maintaining suitable resonant circuit voltages of the oscillator circuit. All operating currents and voltages of the oscillator are internally stabilized. The amplitude and the frequency of the oscillator are therefore largely independent of changes in temperature or operating voltages.

During UHF operation the oscillator and the mixer are disabled and the asymmetrical, low-noise UHF-IF coupling stage is activated.

IF SAW Driver Section

The IF SAW driver includes a high-impedance, asymmetrical input. The low-impedance symmetrical output of the IF SAW driver has two open collectors. The basic volume and the output resistance can be further reduced by an ohmic symmetrical load resistor. When the operating voltage is not connected to the collectors, the current consumption of the IF SAW driver section is zero. The signal modulation capability of the IC depends on the connected supply voltage.

Absolute Maximum Ratings*

V_S = 10V to 13.5V

Supply Voltage (V_S) ..... −0.3V to +14V
Current from Pin 15 ($-I_{15}$) ..... 0 mA to 2 mA
Voltage at Pin 1 (V_1) ..... −0.3V to V_S
Voltage at Pin 2 (V_2) ..... −0.3V to V_S
Voltage at Pin 8 (V_8) ..... V_{14} to V_S
Voltage at Pin 9 (V_9) ..... V_{14} to V_S
Voltage at Pin 10 (V_{10}) ..... −0.3V to V_S
Capacitance at Pin 15 (C_{15}) ..... 0 nF to 100 nF
Capacitance at Pin 7 (C_3) ..... 0 µF to 1 µF
Only the provided external components can be connected to pins 4, 5, 6, 11, 12, 13, 16.
Junction Temperature (T_j) ..... 150°C
Storage Temperature (T_{stg}) ..... −40°C to +125°C
Thermal Resistance (R_{thSA}) (System-Air) ..... 80 K/W

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Operating Range

Supply Voltage (V_S) ..... 10V to 13.5V
Mixer Input Frequency (f_M) ..... 20 MHz to 650 MHz
UHF-IF Input Frequency (f_{UHF}) ..... 20 MHz to 650 MHz
Mixer IF Output Frequency (f_{MIF}) ..... 20 MHz to 650 MHz
Oscillator Frequency (f_{OSC}) .... 20 MHz to 700 MHz
Voltage at Pin 8, 9 ($V_{8,9}$) ..... V_{14} to V_S
Voltage at Pin 1, 2 ($V_{1,2}$) ..... 5V to V_S
Ambient Temperature (T_A) ..... 0°C to +70°C

Characteristics V_S = 12V, T_A = 25°C

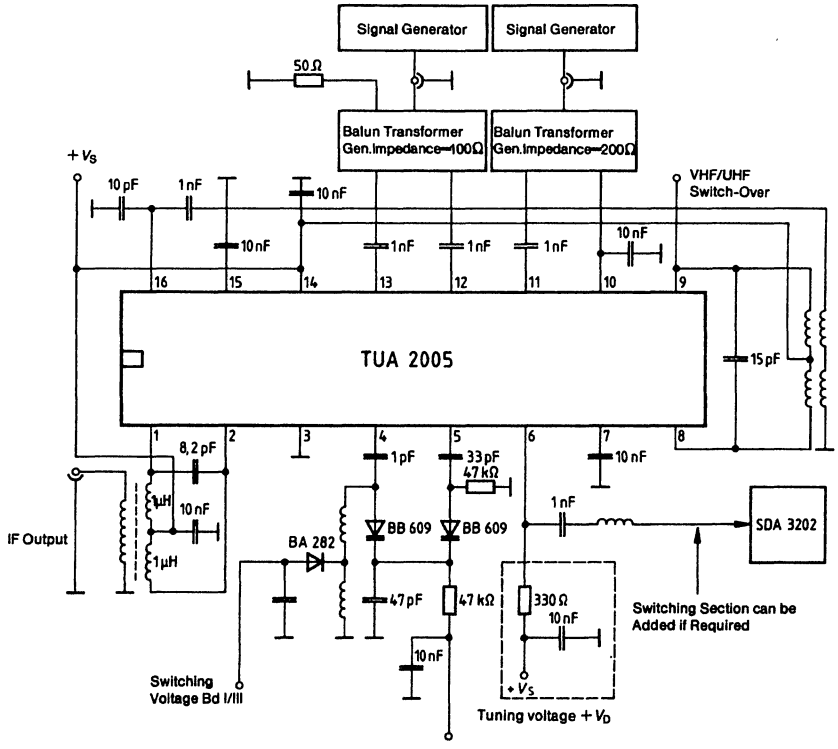
Parameter	Symbol	Test Conditions	Test Circuit	Limits			Units
				Min	Typ	Max	
RF Section							
Current Consumption	I_{14}	I_{15} = 0 mA; V_{10} = V_S	1	18	28	37	mA
Reference Voltage	V_{15}	0 ≤ I_{15} ≤ 1 mA	1	7.5	8	8.5	V
Oscillator Frequency Range	f_{OSC}	External Circuitry Tuned to Frequency	1	48		700	MHz
Turn-On Start-Up Drift	Δf_{OSC}	TC Value of Cap. in Osc. Circuit is 0; Drift is Only Referenced to Self-Heating of Component. t = 0.5s to 10s Channel S20	1	0	−100	−500	kHz
Frequency Drift versus V_S	$-\Delta f_{OSC}$	V_S = 10V to 13.5V S20	1	−250		+250	kHz
UHF Switching Voltage	V_{10}	$V_{I(U)}$ = −25 dBm; V_Q ≥ −5 dBm	1	7		V_S	V
VHF Switching Voltage	V_{10}	$V_{I(U)}$ = −25 dBm; V_Q ≤ −30 dBm	1	0		3	V
Output Impedance	Z_8; Z_9	Static	7	10			kΩ
Output Capacitance	C_8 = C_9		6	0.5	1	2.0	pF

7

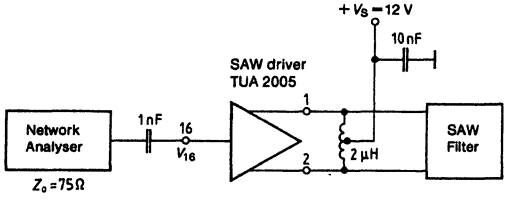
Characteristics V_S = 12V, T_A = 25°C (Continued)

Parameter	Symbol	Test Conditions	Test Circuit	Limits			Units
				Min	Typ	Max	
RF Section (Continued)							
RF Output Phase	$\alpha_{8,9}$			140	180	220	degrees
Mixer Gain	G_3	Channel 3; R_G = 100Ω	1	25	27	29	dB
Mixer Gain		Channel 9; R_G = 100Ω f = 294.25 MHz					
Mixer Gain	G_{S20}	Channel S20; R_G = 100Ω f = 294.25 MHz	1	25	27	29	dB
Mixer Gain	G_{21} Wt21	Channel Wt21; R_G = 100Ω f = 421.25 MHz	1	25	27	29	dB
UHF-IF Gain	UHF	R_G = 200Ω; f_{IF} = 36.5 MHz	1	31	33	35	dB
Mixer Noise Figure	NF_9	Channel 9; R_G = 100Ω f = 203.25 MHz					
Mixer Noise Figure	NF_3	Channel 3; R_G = 100Ω	1			8	dB
Mixer Noise Figure	NF_{S20}	Channel S20; R_G = 100Ω	1			10	dB
Mixer Noise Figure	NF_{21}	Channel 21; R_G = 100Ω	1			14	dB
UHF-IF Noise Figure	NF_{UHF}	R_G = 200Ω	1			7	dB
Oscillator Output Signal for PLL or Frequency Divider	V_6	R_L = 200Ω; Channel 3 S20	1	−27		−17	dBm
SAW IF Driver							
Current Consumption	$I_1 + I_2$	V_S = 12V		17	22	28	mA
Input Impedance	Z_{16}	S-Parameter Measurement	2		3		kΩ
Input Capacitance	C_{16}	S-Parameter Measurement	2		1.5		pF
Symmetrical Output Resistance	$\lvert Z_{1/2}\rvert$	S-Parameter Measurement	5	50	100	200	Ω
Linearity (Permissible Input Signal)	V_{16}	m_s = 80%; f_S = 36.5 MHz Total Harmonic Distortion of Output Signal V_Q is THD = 1%	3		250		mV
Noise Figure	NF	R_G = 200Ω	4		10		dB
Gain	G	$R_L = R_G$ = 50Ω	3		−16		dB

Measurement Circuit 1



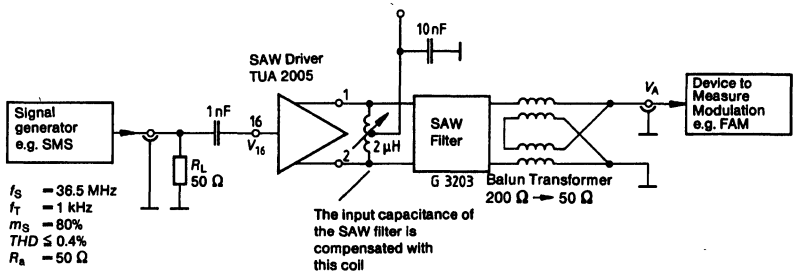
Measurement Circuit 2



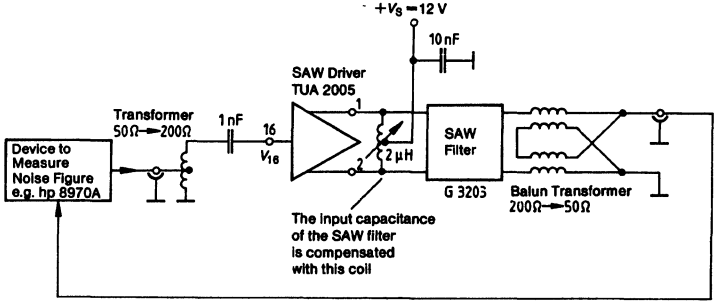
The input reflection factor S_{16} is measured at 36.5 MHz for computing the parallel equivalent circuit.

7

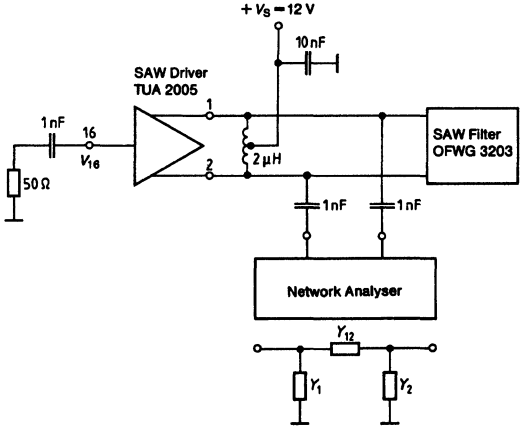
Measurement Circuit 3



Measurement Circuit 4

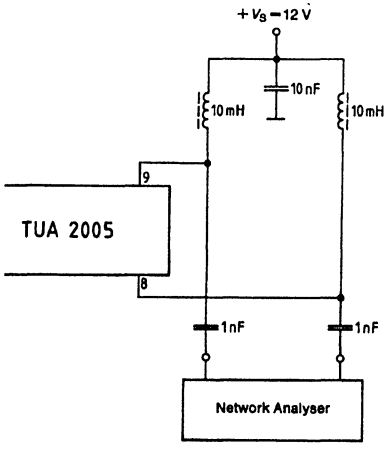


Measurement Circuit 5



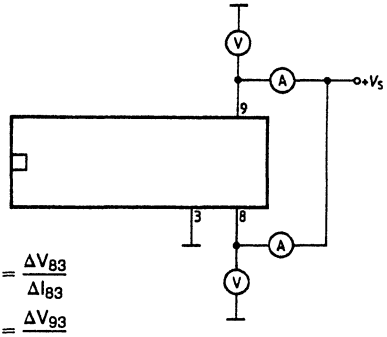
The 4-pole matrix S_{11}, S_{12}, S_{21}, S_{22} is measured at 36.5 MHz for computing that π equivalent circuit.

Measurement Circuit 6



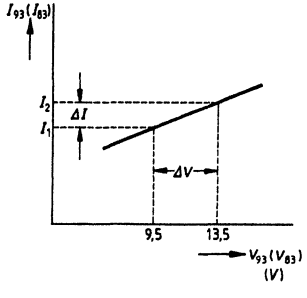
The 4-pole matrix S_{81}, S_{82}, S_{91}, S_{92} is measured at 100 MHz for computing the output capacitance.

Measurement Circuit 7 Measurement of Static Output Impedance



$$Z_{83} = \frac{\Delta V_{83}}{\Delta I_{83}}$$

$$Z_{93} = \frac{\Delta V_{93}}{\Delta I_{93}}$$



Ordering Information

Type	Ordering Code	Package
TUA 2005	Q67000-A8033	DIP 16

SIEMENS

Preliminary

TUA 2006
Television Tuner for Frequency Ranges up to 700 MHz

RF Section

- Few External Components
- Frequency and Amplitude-Stable Oscillator
- Optimal Suppression of Oscillator and Output Frequency at IF Output
- High Resistance to Interference Voltages
- High-Impedance Symmetrical Mixer Input
- IF Post-Amplifier for UHF-IF Signal
- Symmetrical Mixer Output
- Low-Noise, Internal Reference Voltage

IF SAW Driver Section

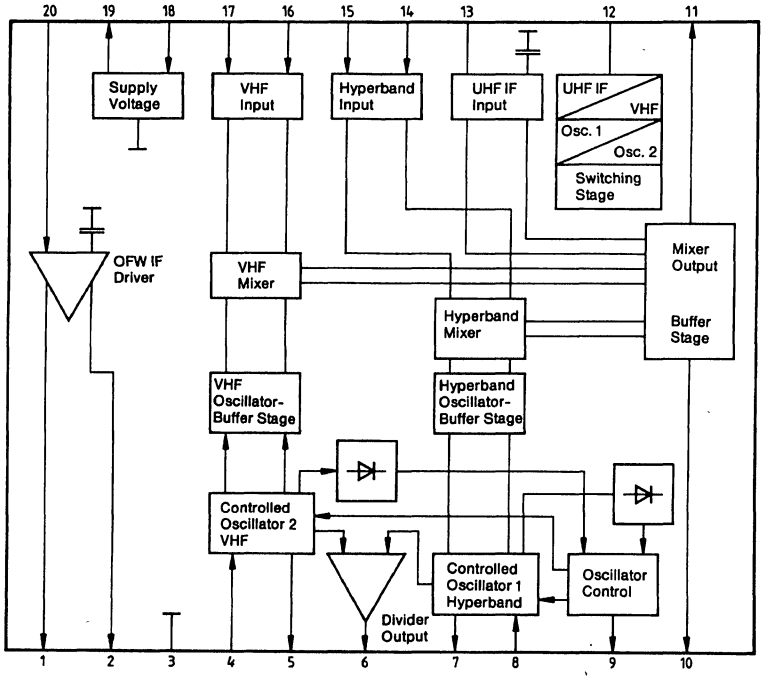
- Optimal Crosstalk Suppression
- High-Impedance, Asymmetrical Input with High Signal Modulation Capability
- Low-Impedance Symmetrical Output for Driving SAW Filters

Pin Definitions

Pin	Function
1	Low-impedance symmetrical output of SAW driver
2	Low-impedance symmetrical output of SAW driver anti-phased to pin 1
3	GND
4	High-impedance input of oscillator amplifier (VHF)
5	Low-impedance output of oscillator amplifier (VHF)
6	Oscillator signal output for PLL system and divider
7	Low-impedance output of oscillator amplifier (hyperband)
8	High-impedance input of oscillator amplifier (hyperband)
9	Blocking capacitor for controlling oscillator amplitude
10	Symmetrical mixer output
11	Symmetrical mixer output anti-phased to pin 10
12	Switching voltage input for VHF/hyperband/UHF switch-over
13	High-impedance asymmetrical RF input for UHF-IF signal
14	High-impedance symmetrical RF input of hyperband mixer
15	High-impedance symmetrical RF input of hyperband mixer anti-phased to pin 14
16	High-impedance symmetrical RF input of VHF mixer
17	High-impedance symmetrical RF input of VHF mixer anti-phased to pin 16
18	Supply voltage
19	Blocking point of internal reference voltage
20	High-impedance asymmetrical IF input of SAW driver

The TUA2006 has been designed as a monolithically integrated tuner circuit suitable as a TV tuner for a CATV frequency range extended to 700 MHz.

Block Diagram



Circuit Description

RF Section

The integrated circuit includes a symmetrical high-impedance, low-noise mixer input and a multiplicative mixer.

The amplitude of the operating oscillator is controlled for maintaining suitable resonant circuit voltages of the oscillator circuit. All operating currents and voltages of the oscillator are internally stabilized. The amplitude and the frequency of the oscillator are therefore largely independent of changes in temperature or operating voltages.

During UHF operation both the oscillator and the mixer are disabled and the asymmetrical, low-noise UHF-IF coupling stage is activated.

IF SAW Driver Section

The IF SAW driver includes a high-impedance, asymmetrical input. The low-impedance symmetrical output of the IF SAW driver has two open collectors. The basic volume and the output resistance can be further reduced by an ohmic symmetrical load resistor. When the operating voltage is not connected to the collectors, the current consumption of the IF SAW driver section is zero. The signal modulation capability of the IC depends on the connected supply voltage.

Absolute Maximum Ratings*

V_S = 10V to 15.5V

Supply Voltage (V_S) ..... −0.3V to +14V
Current Form Pin 15 ($-I_{15}$) ..... 0 mA to 2 mA
Voltage at Pin 1 (V_1) ..... −0.3V to V_S
Voltage at Pin 2 (V_2) ..... −0.3V to V_S
Voltage at Pin 8 (V_8) ..... V_{14} to V_S
Voltage at Pin 9 (V_9) ..... V_{14} to V_S
Voltage at Pin 10 (V_{10}) ..... −0.3V to V_S
Capacitance at Pin 15 (C_{15}) ..... 0 nF to 100 nF
Capacitance at Pin 7 (C_3) ..... 0 µF to 1 µF

Only the provided external components can be connected to pins 4, 5, 6, 11, 12, 13, 16.

Junction Temperature (T_j) ..... 150°C
Storage Temperature (T_{stg}) ..... −40°C to +125°C
Thermal Resistance
System-Air (R_{thSA}) ..... 80 K/W

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Operating Range

Supply Voltage (V_S) ..... 10V to 13.5V
Mixer Input Frequency (f_M) ..... 20 MHz to 650 MHz
UHF-IF Input
Frequency (f_{UHF}) ..... 20 MHz to 650 MHz
Mixer IF Output
Frequency (f_{MIF}) ..... 20 MHz to 650 MHz
Oscillator Frequency (f_{OSC}) .... 20 MHz to 700 MHz
Voltage at Pin 8, 9 ($V_{8,9}$) ..... V_{14} to V_S
Voltage at Pin 1, 2 ($V_{1,2}$) ..... 5V to V_S
Ambient Temperature (T_A) ..... 0°C to 70°C

Characteristics V_S = 12V; T_A = 25°C

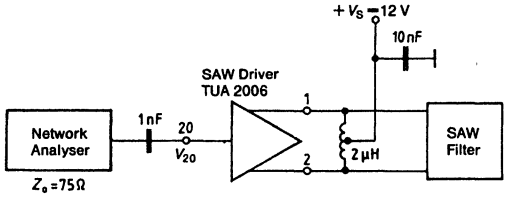
Parameter	Symbol	Conditions	Test Circuit	Limits			Units
				Min	Typ	Max	
RF Section							
Current Consumption	I_{18}	I_{19} = 0 mA, V_{12} = V_S		18	30	40	mA
Reference Voltage	V_{19}	0 ≤ I_{19} ≤ 1 mA		7.5	8	8.5	V
Oscillator Frequency Range	$f_{OSC\ VHF}$	Ext. Circuitry Tuned to Frequency		48 48		500 700	MHz MHz
Turn-On Start-Up Drift	$\Delta f_{OSC\ hyperb.}$	TC Value of Cap. in Osc. Circuits is 0; Drift is Only Referenced to Self-Heating of Component t = 0.5 sec. to 10 sec.; Channel S20		0	−100	−500	kHz
Frequency Drift versus V_S	$-\Delta f_{OSC}$	V_S = 10V to 13.5V S20		−250		+250	kHz
UHF Switching Voltage	V_{12}	$V_{I(U)}$ = −25 dBm; V_Q ≥ −5 dBm;		8.5		V_S	V
VHF Switching Voltage	V	$V_{I(U)}$ = −25 dBm; V_Q ≤ −30 dBm;		0		3	V
Hyperband Switching Voltage	V			4.5		7.5	V
Output Impedance	Z_{10}; Z_{11}	Static	6	10			kΩ
Output Capacitance	C_{10} = C_{11}		5	0.5	1	2.0	pF
RF Output Phase	$\alpha_{10,11}$			140	180	220	degrees
Mixer Gain VHF	G_3	Channel 3; R_G = 100Ω f = 55.25 MHz		25	27	29	dB

Characteristics V_S = 12V; T_A = 25°C (Continued)

Parameter	Symbol	Conditions	Test Circuit	Limits			Units
				Min	Typ	Max	
RF Section (Continued)							
Mixer Gain VHF	G_9	Channel 9; R_G = 100Ω f = 203.25 MHz					
	G_{S20}	Channel S20; R_G = 100Ω f = 294.25 MHz		25	27	29	dB
Mixer Gain Hyperband	G_3	Channel 3; R_G = 100Ω f = 55.25 MHz	1	25	27	29	dB
	G_9	Channel 9; R_G = 100Ω f = 203.25 MHz					
	G_{S20}	Channel S20; R_G = 100Ω f = 294.25 MHz	1	25	27	29	dB
UHF-IF Gain	G_{UHF}	R_G = 200Ω; f_{IF} = 36.5MHz		31	33	35	dB
Mixer Noise Figure VHF	NF_3	Channel 3; R_G = 100Ω f = 55.25 MHz				8	dB
	NF_9	Channel 9; R_G = 100Ω f = 203.25 MHz					
	NF_{S20}	Channel S20; R_G = 100Ω f = 294.25 MHz				10	dB
Mixer Noise Figure Hyperband	NF_3	Channel 3; R_G = 100Ω f = 55.25 MHz				8	dB
	NF_9	Channel 9; R_G = 100Ω f = 203.25 MHz					
	NF_{S20}	Channel S20; R_G = 100Ω f = 294.25 MHz				10	dB
Mixer Noise Figure	NF_{UHF}	UHF; R_G = 200Ω				14	dB
Oscillator Output Signal for PLL or Frequency Divider	V_6	R_L = 50Ω; Channel 3...S20		−20		−6	dBm
SAW IF Driver							
Current Consumption	$I_1 + I_2$			19	25	32	mA
Input Impedance	Z_{20}	S-Parameter, Measurement	1		3		kΩ
Input Capacitance	C_{20}	S-Parameter, Measurement	1		1.5		pF
Symmetrical Output Resistance	$\lvert Z_{1/2}\rvert$	S-Parameter, Measurement	4	50	100	200	Ω
Linearity (Permissible Input Signal)	V_{20}	m_s = 80%; f_s = 36.5 MHz Total Harmonic Distortion of Output Signal V_Q is THD = 1%	2		250		mV
Noise Figure	NF	R_G = 200Ω	3		10		dB
Gain	G	R_L = R_G = 50Ω	2		−16		dB

7

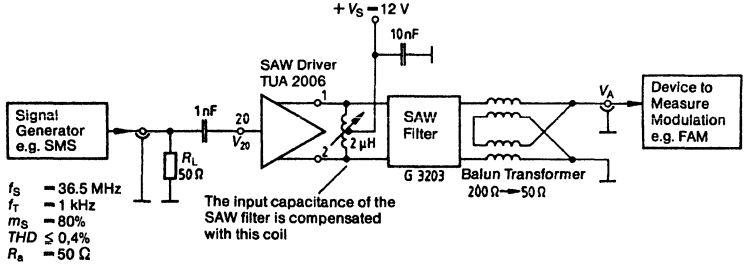
Measurement Circuit 1



0090-2

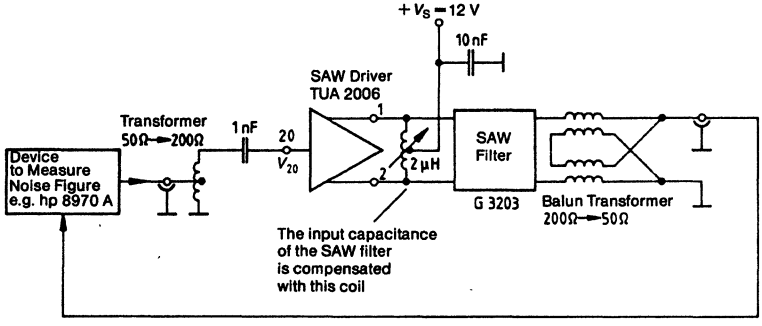
The input reflection factor S_{16} is measured at 36.5 MHz for computing the parallel equivalent circuit.

Measurement Circuit 2



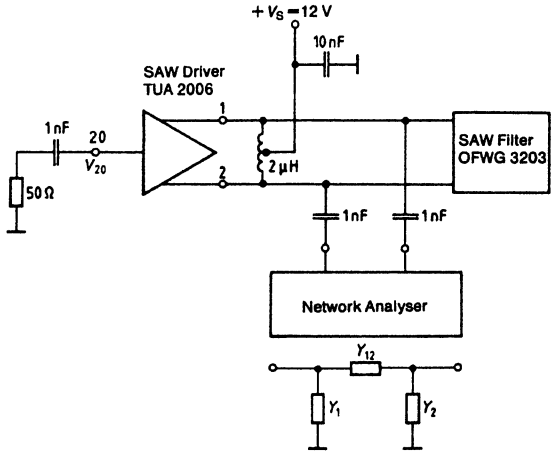
0090-3

Measurement Circuit 3



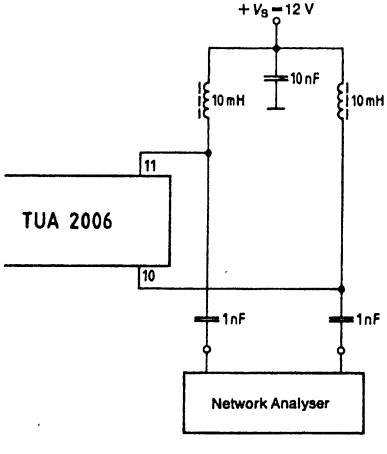
0090-4

Measurement Circuit 4



The 4-pole matrix S_{11}, S_{12}, S_{21}, S_{22}, is measured at 36.5 MHz for computing the π equivalent circuit.

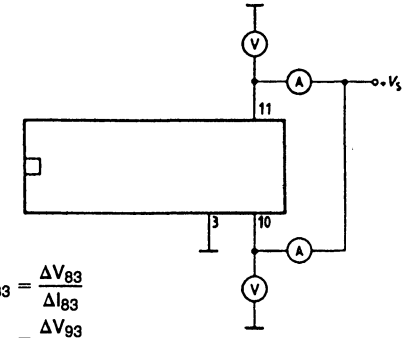
Measurement Circuit 5



The 4-pole matrix S_{81}, S_{82}, S_{91}, S_{92}, is measured at 100 MHz for computing the output capacitance.

7

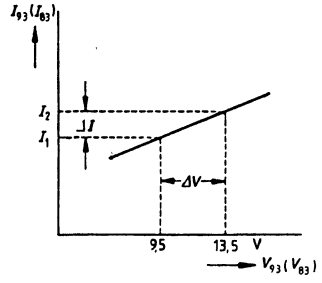
Measurement Circuit 6



$$Z_{83} = \frac{\Delta V_{83}}{\Delta I_{83}}$$

$$Z_{93} = \frac{\Delta V_{93}}{\Delta I_{93}}$$

0090-7



0090-8

Ordering Information

Type	Ordering Code	Package
TUA 2006	Q67000-A8045	DIP 20

ICs for Radio/Audio Applications

8

SIEMENS

S 041 P
FM IF Amplifier with Demodulator

S 041 P is a symmetrical, six-stage amplifier with symmetrical coincidence demodulator for amplifying, limiting, and demodulating frequency-modulated signals. The IC is particularly suited for sets where low current consumption is of importance, or where major supply fluctuations occur.

The pin configuration corresponds to the well-known TBA 120. Pin 5 of S 041 P, however, is not connected internally. These types are especially suited for applications in narrow-band FM systems (455 kHz) and in conventional or standard FM IF systems (10.7 MHz).

Features

- Good limiting properties
- Wide voltage range
- Low current consumption
- Few external components

Maximum ratings

Supply voltage	V_S	15	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air) S 041 P	$R_{th\,SA}$	90	K/W

Operating range

Supply voltage range	V_S	4 to 15	V
Frequency range	f_i	0 to 35	MHz
Ambient temperature range	T_{amb}	−25 to 85	°C

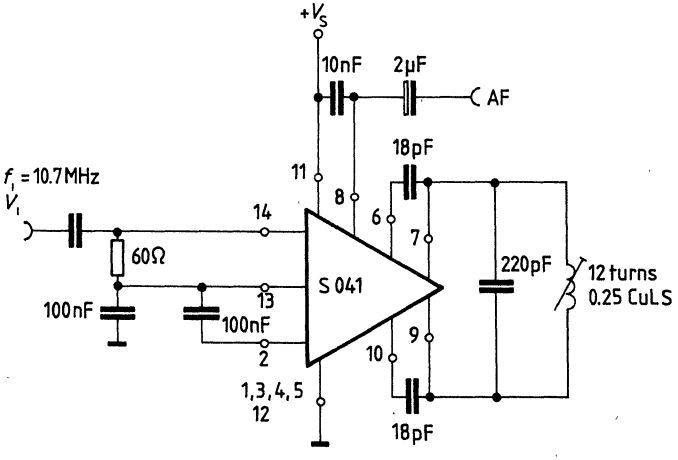
8

Characteristics (V_S = 12 V, Q approx. 35, f_{mod} = 1 kHz, T_{amb} = 25 °C)

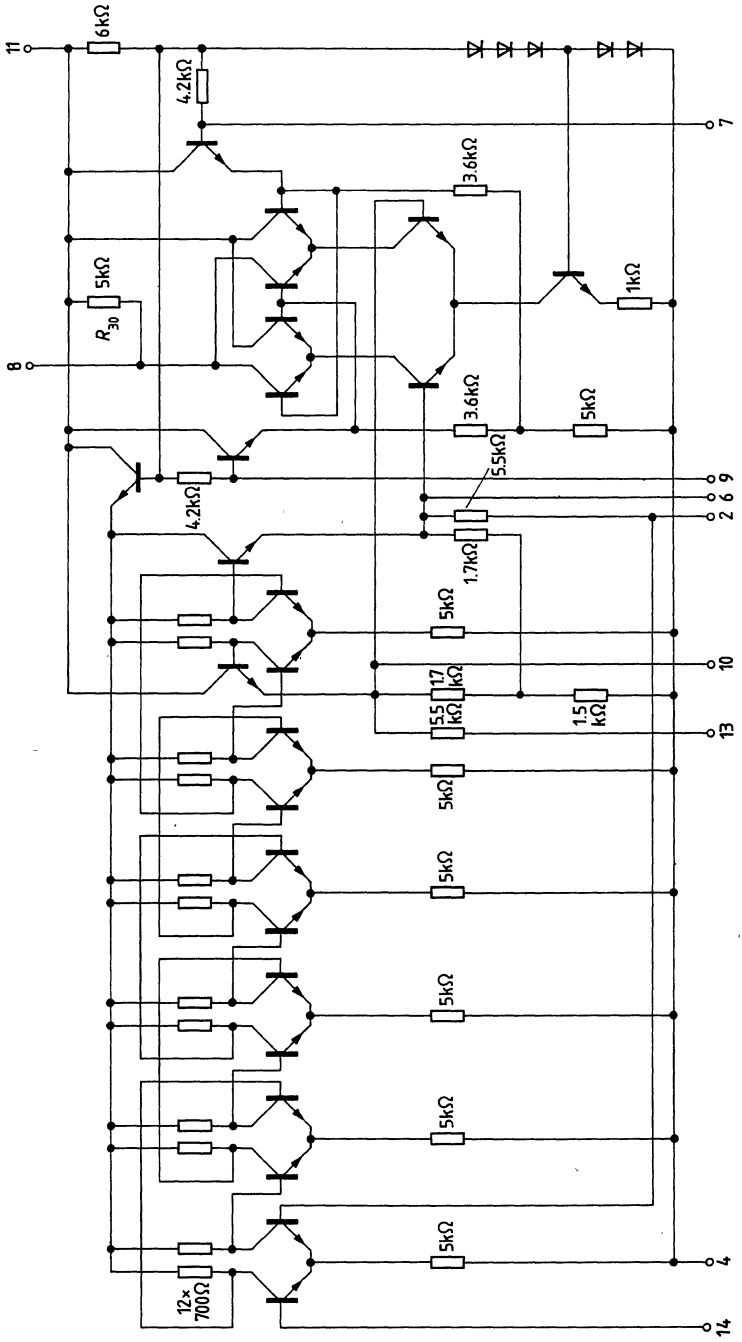
		min	typ	max	
Current consumption	I_S	4.0	5.4	6.8	mA
AF output voltage (f_i = 10.7 MHz, Δf = ± 50 kHz, V_i = 10 mV)	$V_{q\,rms}$	100	170		mV
Total harmonic distortion (f_i = 10.7 MHz, Δf = ± 50 kHz, V_i = 10 mV)	THD		0.55	1.0	%
Deviation of AF output voltage (V_S = 15 V → 4 V, f_i = 10.7 MHz, Δf = ± 50 kHz)	ΔV_q		1.5		dB
Input voltage for limiting (f_i = 10.7 MHz, Δf = ± 50 kHz)	$V_{i\,lim}$		30	60	µV
IF voltage gain (f_i = 10.7 MHz)	G_v		68		dB
IF output voltage for limiting (each output)	$V_{q\,pp}$		130		mV
Input impedance f_i = 10.7 MHz	Z_i		20/2		kΩ/pF
f_i = 455 kHz	Z_i		50/4		kΩ/pF
Output resistance (pin 8)	R_q	3.5	5	8.5	kΩ
Voltage drop at AF ballast resistance	V_{11-8}		1.5		V
AM suppression (V_i = 10 mV, Δf = ± 50 kHz, m = 30%)	a_{AM}		60		dB

All connections mentioned in the index refer to S 041 P (e.g. V_{11})

Test circuit

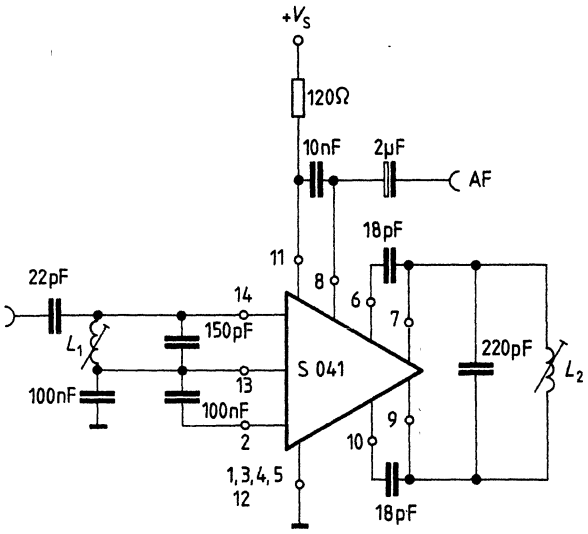


Circuit diagram



8

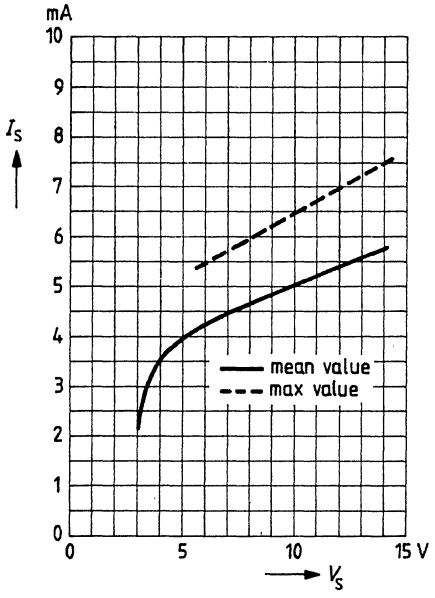
Application circuit for 10.7 MHz (FM IF)
and 455 kHz (narrow-band FM)



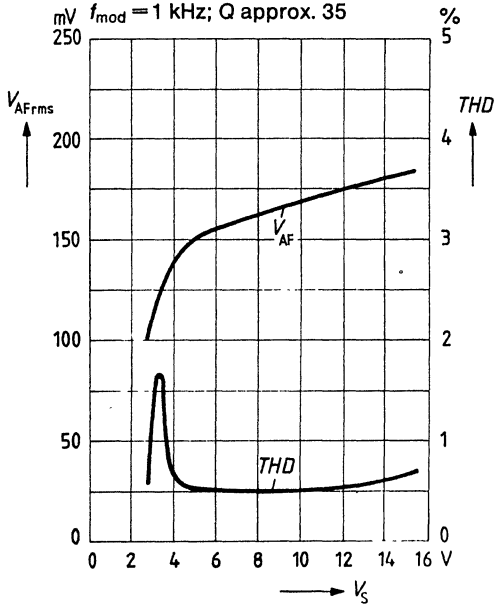
Data in parentheses for 455 kHz (narrow-band FM)

Coils	10.7 MHz	455 kHz
L_1	15 turns/0.15 CuLS	71.5 turns/12 x 0,04 CuLS
L_2	12 turns/0.25 CuLS	71.5 turns/12 x 0.04 CuLS
Coil set	D 41-2165	D 41-2393 of Messrs. Vogt

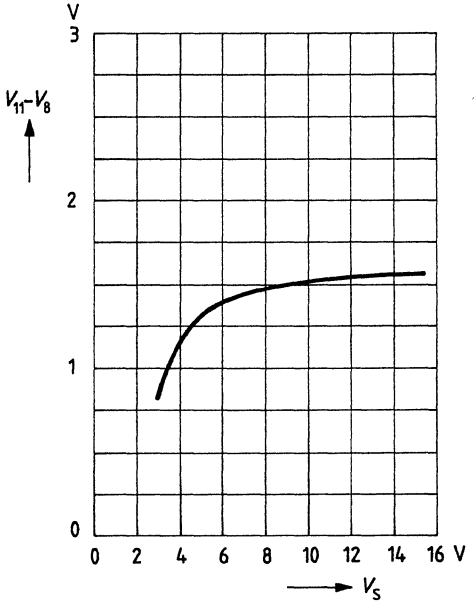
Current consumption versus supply voltage



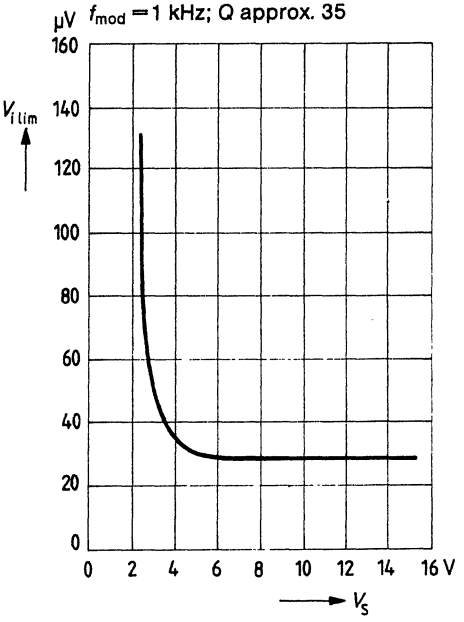
AF output voltage and total harmonic distortion versus supply voltage
f_i = 10.7 MHz; Δf = ± 50 kHz
f_{mod} = 1 kHz; Q approx. 35



DC output voltage difference versus supply voltage
(without signal)



Input voltage for limiting versus supply voltage
f_i = 10.7 MHz; Δf = ± 50 kHz
f_{mod} = 1 kHz; Q approx. 35



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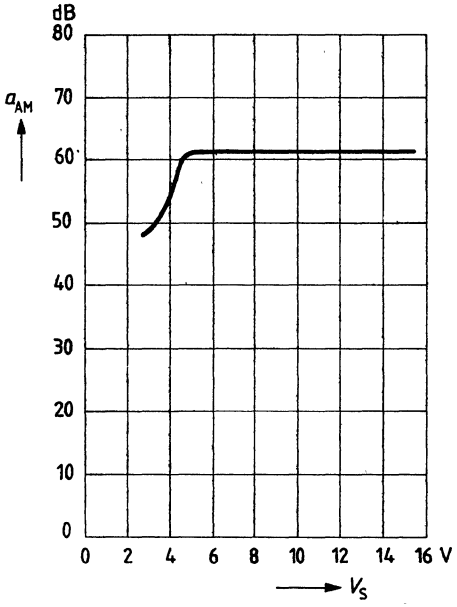
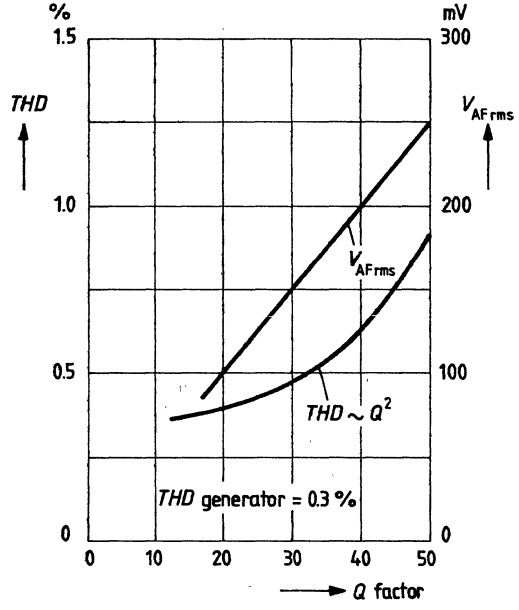
AM suppression versus supply voltage
$f_i = 10.7$ MHz; $\Delta f = \pm 50$ kHz;
$V_i = 10$ mV, $f_{mod} = 1$ kHz, $m = 30\%$



AF output voltage and total harmonic distortion versus Q-factor
$V_S = 12$ V; $f_i = 10.7$ MHz,
$\Delta f = \pm 50$ kHz, $f_{mod} = 1$ kHz



SIEMENS

S 042 P
Mixer

Symmetrical mixer for frequencies up to 200 MHz. It can be driven by an external source or by the built-in oscillator. The input signals are suppressed at the outputs. In addition to the usual mixer applications in receivers, converters, and demodulators for AM and FM, the S 042 P can also be used as electronic polarity switches, multipliers, etc.

Features

- Versatile application
- Wide range of supply voltage
- Few external components
- High conversion transconductance
- Low noise figure

Maximum ratings

Supply voltage	V_S	15	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air) S 042 P:	$R_{th\ SA}$	90	K/W

Operating range

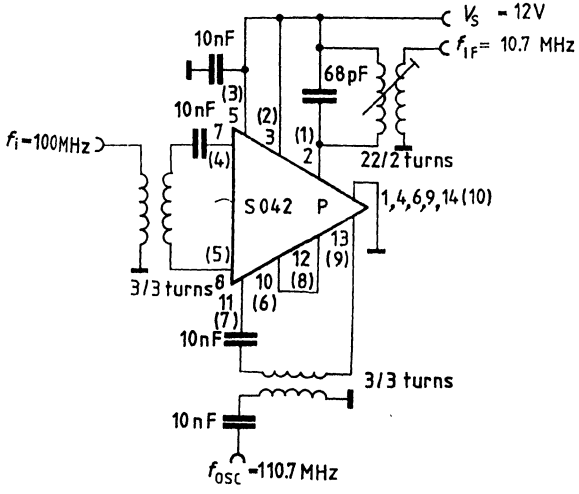
Supply voltage range	V_S	4 to 15	V
Ambient temperature range	T_{amb}	−15 to 70	°C

Characteristics (V_S = 12 V, T_{amb} = 25 °C)

		min	typ	max	
Current consumption	$I_S = I_2 + I_3 + I_5$	1.4	2.15	2.9	mA
Output current	$I_2 = I_3$	0.36	0.52	0.68	mA
Output current difference	$I_3 - I_2$	−60		60	mA
Supply current	I_5	0.7	1.1	1.6	mA
Power gain (f_i = 100 MHz, f_{osc} = 110.7 MHz)	G_p	14	16.5		dB
Breakdown voltage ($I_{2,3}$ = 10 mA; $V_{7,8}$ = 0 V)	V_2, V_3	25			V
Output capacitance	$C_{2\text{-}M}$, $C_{3\text{-}M}$		6		pF
Conversion transconductance (f = 455 kHz	$S = \frac{I_2}{V_7 - V_8} = \frac{I_3}{V_7 - V_8}$		5		mS
Noise figure	NF		7		dB

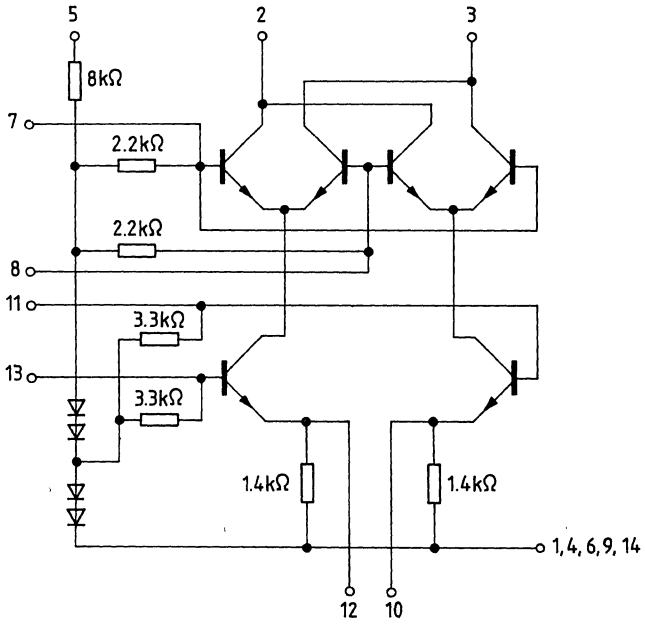
All connections mentioned in the index refer to S 042 P (e.g. I_2)

Test circuit



Connections in parentheses apply to S 042E

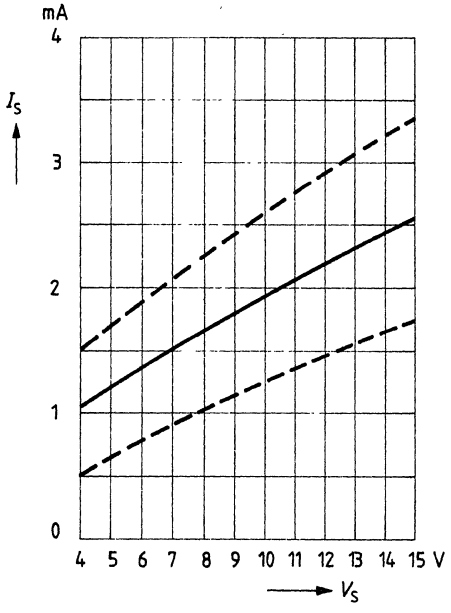
Circuit diagram



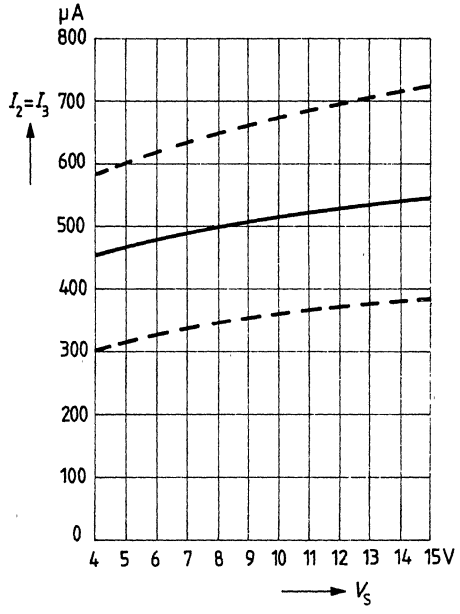
A galvanic connection between pins 7 and 8 and pins 11 and 13 through coupling windings is recommended.

Between pins 10 and 14 (ground) and between pins 12 and 14, one resistance each of at least 220 Ω may be connected to increase the currents and thus the conversion transconductance. Pins 10 and 12 may be connected through any impedance. In case of a direct connection between pins 10 and 12, the resistance from this pin to 14 may be at least 100 Ω. Depending on the layout, a capacitor (10 to 50 pF) may be required between pins 7 and 8 to prevent oscillations in the VHF band.

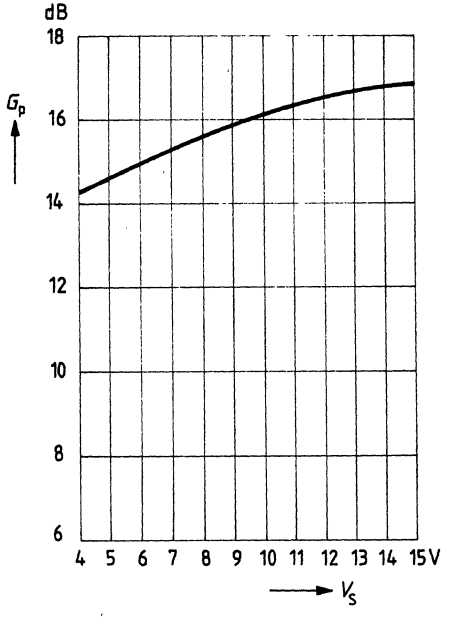
Total current consumption versus supply voltage



Output current versus supply voltage

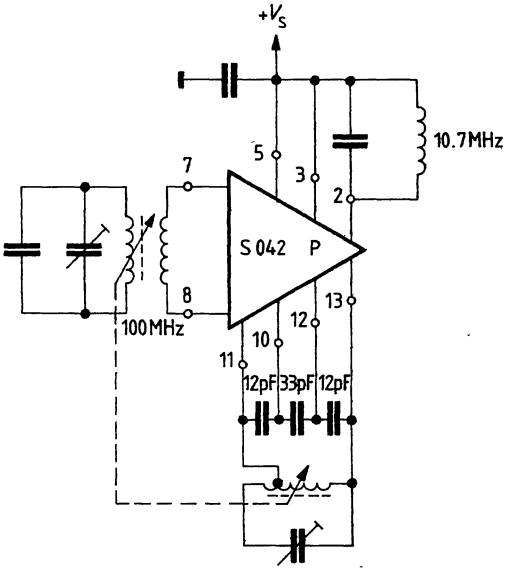


Power gain versus supply voltage

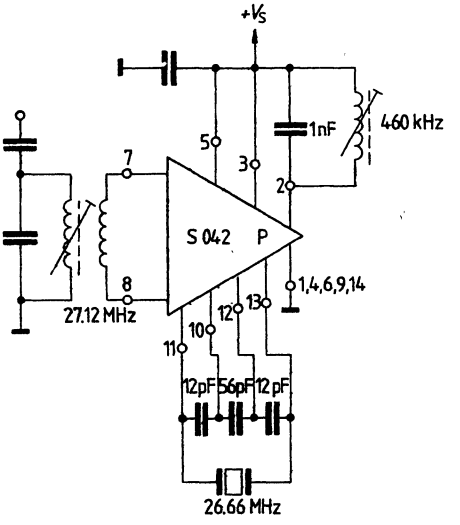


Application circuits

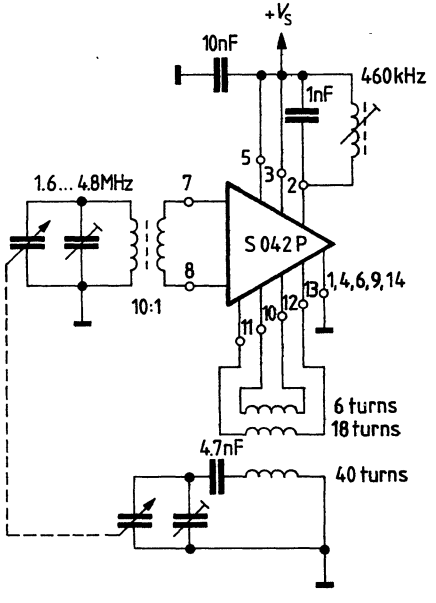
VHF mixer with inductive tuning



Mixer for remote control receivers
without oscillator

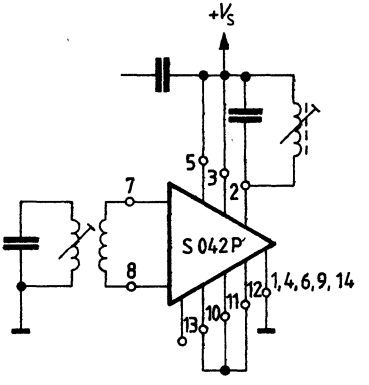


Mixer for short-wave application
in self-oscillating operation



For overtone crystals an adequate inductance is recommended between pins 10 and 12 to avoid oscillations to the fundamental tone.

Differential amplifier with internal neutralization, also suited for use as limiter for frequencies up to 50 MHz or at higher currents up to 100 MHz



8

SIEMENS

Preliminary

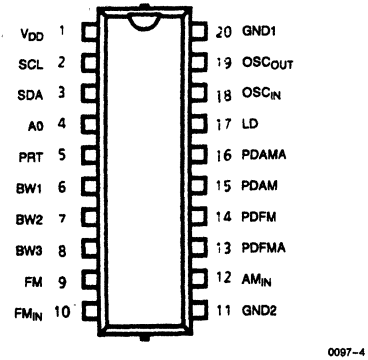
SDA 2121
CMOS PLL with I²C Bus for AM/FM Receivers

- High Input Sensitivity (50 mV_{rms} on FM and 10 mV_{rms} on AM)
- High Input Frequencies (150 MHz on FM and 35 MHz on AM)
- Extremely Fast Phase Detector with Very Short Anti-Backlash Pulses
- I²C Bus
- Large Divider Rations:
  - — 16 Bit N Divider
  - — 16 Bit R Divider
  - — Divider Factor Without Vacancy
    OSC_{IN} 2-65535
    AM_{IN} 2-65535
    $FM_{IN}/2$ 2-65535
- Adjustable Raster Width (<1 KHz for AM, <12.5 KHz for FM)*
- Two-Pin Oscillator Provides Connection of a Piezoelectric Crystal for Reference Frequency Generation
- Switchable Phase Detector Polarity
- Switchable Phase Detector Current (0.25/1 mA)
- One Phase Detector Output Each for FM and AM with the Corresponding Analog Phase Detector Outputs
- Open Drain Band Selection Outputs for 10V

*Raster width = Input Frequency/Divider Factor
[On FM_{IN} input frequency/2 is to be used due to the prescaler]

Pin Configuration

(Top View)



The SDA 2121 is an integrated circuit in CMOS technology which has been especially designed for application in radio equipment. It serves as a PLL for frequency synthesis concepts.

Pin Definitions

Pin	Symbol	Function
1	V_{DD}	Supply Voltage
2	SCL	I²C Bus Clock
3	SDA	I²C Bus Data Input and Acknowledge Output
4	A0	Address Input
5	PRT	Port Output (Only with 20-Pin Packages)
6 7 8	BW1 BW2 BW3	Band Selection Output (Open Drain Output for 10V)
9	FM	Band Selection Output (Open Drain Output, 10V) Switching AM/FM Operation
10	FM_{IN}	FM Input
11	GND2	Ground Connection for AM and FM Amplifier
12	AM_{IN}	AM Input
13	PDFMA	Analog Output Corresponding to the Phase Detector Output, in Test Operation Open Drain Output of FVN Signal
14 15	PDFM PDAM	Phase Detector Output for AM or FM Active or Tristate Depending on Operating Mode
16	PDAMA	Analog Output Corresponding to the Phase Detector Output, in Test Operation Open Drain Output of FRN Signal
17	LD	Lock-Detect Output (Only with 20-Pin Packages)
18 19	OSC_{IN} OSC_{OUT}	Connection for Reference Oscillator Input or Output
20	GND1	Ground

Circuit Description

The SDA 2121 is a complex PLL component in CMOS technology for processor controlled frequency synthesis.

Function and dividing ratios are selected via an I²C bus interface (licensed by Philips) at pins SCL, SDA and A0. The chip address is set via address input A0. Thus it is possible to address two components via the I²C bus. The reference frequency can be applied at input OSC IN or it can be gererated internally by a piezoelectric crystal. Its maximum value is 15 MHz. The VCO frequency is applied at input FM or AM respectively. Its maximum value is 150 MHz at the FM input and 35 MHz at the AM input. The FM input signal is divided by two by an asynchronous prescaler.

Outputs PDFM and PDAM supply the phase detector signal with especially short anti-backlash pulses to neutralize even the smallest phase deviations. Polarity and current of the PD outputs can be switched. The component also has corresponding analog phase detector outputs. A lock-detect output (LD) and a port output (PRT) are provided on the 20-pin version.

Absolute Maximum Ratings*

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Supply Voltage (V_{DD}) ..... −0.3V to 6V
Input Voltage (V_I) ..... −0.3V to V_{DD} + 0.3V
Power Dissipation per Output (P_Q) ..... 10 mW
Total Power Dissipation (P_{tot}) ..... 300 mW
Storage Temperature (T_S) ..... −40°C to + 125°C
Output Voltage Band Selection Outputs (V_{QH}) 10.5V

Operating Range

Within the functional range, the integrated circuit operates as described; deviations from the characteristics data are possible.

Pos	Parameter	Symbol	Limits			Units
			Min	Typ	Max	
1	Supply Voltage	V_{DD}	4.5	5	5.5	V
2	Supply Current	I_{DD}			10	mA
3	Bias Current	I_{DD}			30	µA
4	Ambient Temperature	T_A	−25		+85	°C
5	Output Voltage Band Selection Outputs	V_{QH}			10	V

Test Conditions for pos. 2
— V_{DD} = 5.5V
— T_A = 25°C
— Outputs not connected
— No test operation
— Max. permissible operating frequency on AM, FM, OSC_{IN}
— V_{IFM}, V_{IAM}, V_{IOSCIN} minimal
— Minimal divider ratios
— PLL in in-lock condition

Test conditions for pos. 3
— V_{DD} = 5.5V
— T_A = 25°C
— FM, AM, OSC_{IN} on V_{DD}
— Outputs not connected
— No test operation

Characteristics

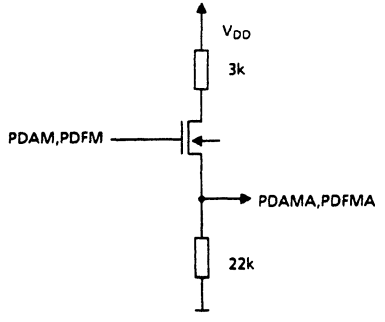
The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not stated otherwise, typical characteristics will apply at T_A = 25°C and the listed supply voltage. (All voltages referenced to GND.)

Pos	Parameter	Symbol	Conditions	Limits			Units
				Min	Typ	Max	
Input Signals SCL, SDA, A0							
1	H Input Voltage	V_{IH}		0.7 × V_{DD}		V_{DD}	V
2	L Input Voltage	V_{IL}		0		0.3 × V_{DD}	V
3	Input Capacitance	C_I				10	pF
4	Input Current	I_I	V_I = V_{DD}			10	µA
Input Signal OSC_{IN}							
9	Input Frequency	f	V_{DD} = 4.5V			15	MHz
10	Input Voltage	V_I	(Sine Wave)	100			mV_{rms}
11	Input Capacitance	C_I				10	pF
12	Input Current	I_I	V_I = V_{DD}			10	µA

Characteristics (Continued)

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not stated otherwise, typical characteristics will apply at T_A = 25°C and the listed supply voltage. (All voltages referenced to GND.)

Pos	Parameter	Symbol	Conditions	Limits			Units
				Min	Typ	Max	
Input Signal AM							
13	Input Frequency	f	V_{DD} = 4.5V			35	MHz
14	Input Voltage	V_I	(Sine Wave)	10			mV_{rms}
15	Input Capacitance	C_I				10	pF
16	Input Current	I_I	$V_I = V_{DD}$			10	µA
Input Signal FM							
17	Input Frequency	f	V_{DD} = 4.5V			150	MHz
18	Input Voltage	V_I	(Sine Wave)	50			mV_{rms}
19	Input Capacitance	C_I				10	pF
20	Input Current	I_I	$V_I = V_{DD}$			10	µA
Output Signal PDFM (Tristate Output)							
21	PD Current "High"	I_Q	V_{DD} = 5V		±1		mA
22	PD Current "Low"	I_Q	T_A = −25°C to +60°C		±0.25		mA
23	PD Current "Tristate"	I_Q			±50		nA
Output Signal PDAM (Tristate Output)							
24	PD Current "High"	I_Q	V_{DD} = 5V		±1		mA
25	PD Current "Low"	I_Q	T_A = −25°C to +60°C		±0.25		mA
26	PD Current "Tristate"	I_Q			±50		nA
Output Signal PDAMA, PDFMA (Analog Output)							
27	H Output Current	I_{QH}	$V_{PD} = V_{DD}$		1	2	mA
28	L Output Current	I_{QL}	V_{PD} = GND	0.1	0.5		mA



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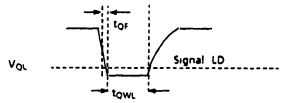
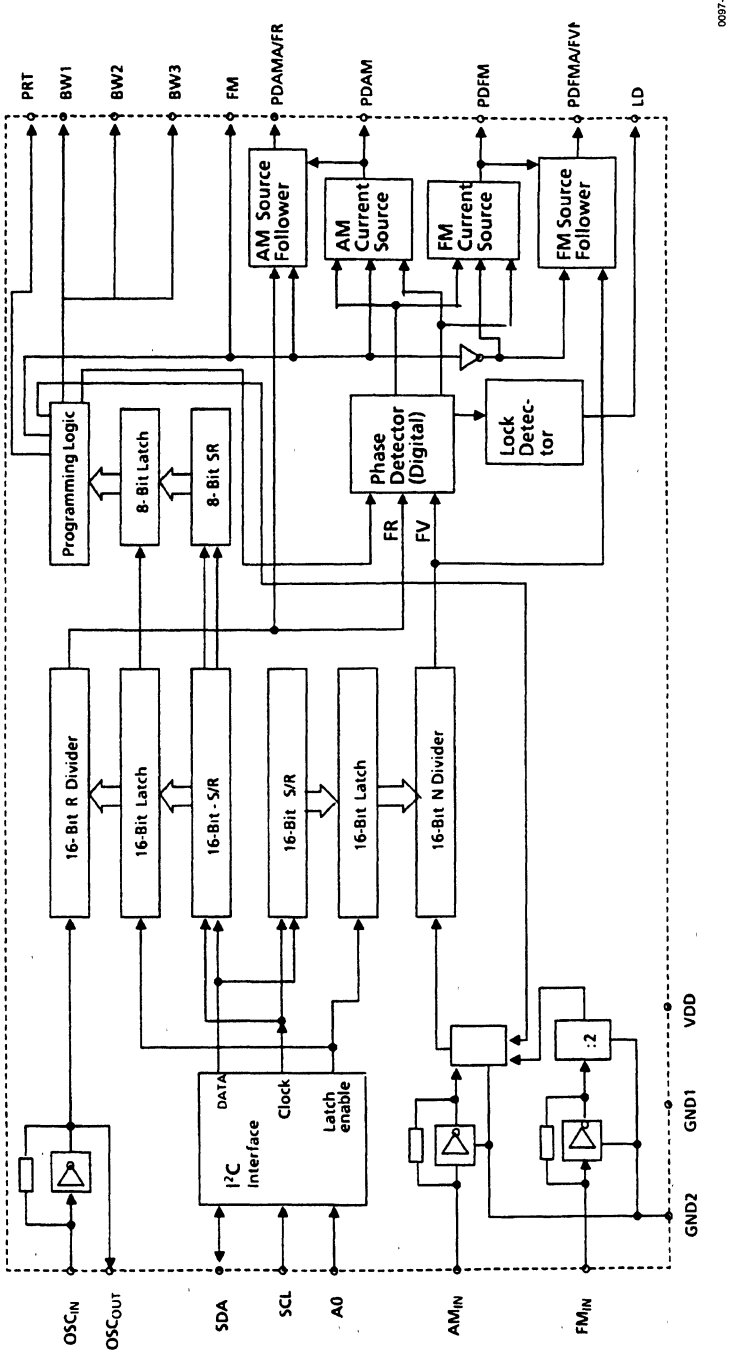
Characteristics (Continued)

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not stated otherwise, typical characteristics will apply at T_A = 25°C and the listed supply voltage. (All voltages referenced to GND.)

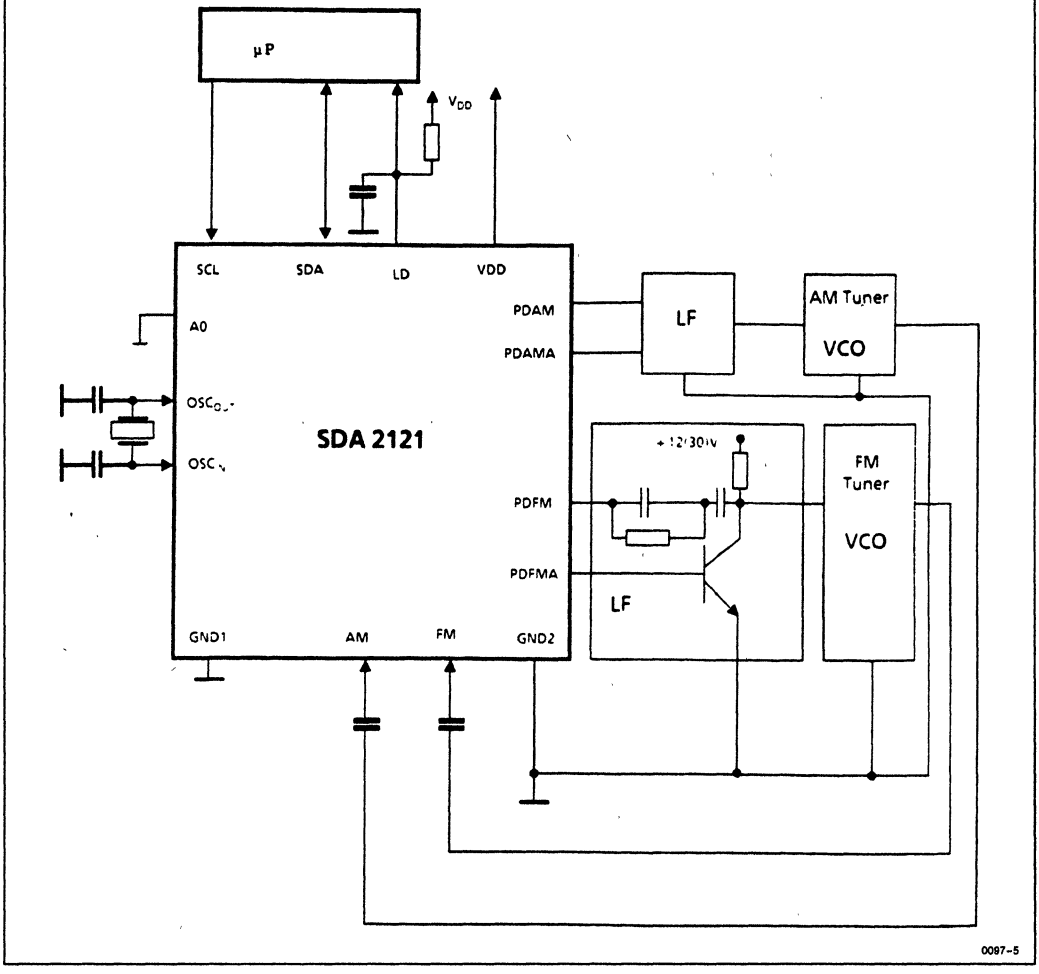
Pos	Parameter	Symbol	Conditions	Limits			Units
				Min	Typ	Max	
Output Signal FVN, FRN (Open Drain Outputs, Active only in Test Operation)							
29	L Output Voltage	V_{QL}			*		V
30	H Output Voltage	V_{QH}			*		V
31	Fall Time	t_{QF}			*		ns
32	Rise Time	t_{QR}			*		ns
Output Signal LD (Open Drain Output)							
33	L Output Signal	V_{QL}	I_{QL} = 3 mA V_{DD} = 5V CL = 20 pF			0.4	V
34	L Output Pulse Width	t_{QWL}			*		ns
	 0097-2						
Output Signal PRT							
35	H Output Voltage	V_{QH}	I_{QH} = 0.5 mA	V_{DD} − 0.4			V
36	L Output Voltage	V_{QL}	I_{QL} = 0.5 mA			0.4	V
Output Signal OSC_{OUT}							
37	H Output Voltage	V_{QL}			*		
38	L Output Voltage	V_{QL}			*		
Output Signal BW 1, 2, 3 and FM (Open Drain Band Selection Outputs)							
39	L Output Voltage	V_{QL}	I_{QL} = 1 mA V_{DD} = 5V			0.4	V
Output Signal SDA							
40	L Output Voltage	V_{QL}	I_{QL} = 3 mA V_{DD} = 5V CL = 400 pF			0.4	V

*Values not available at this time.

Block Diagram



Application Circuit



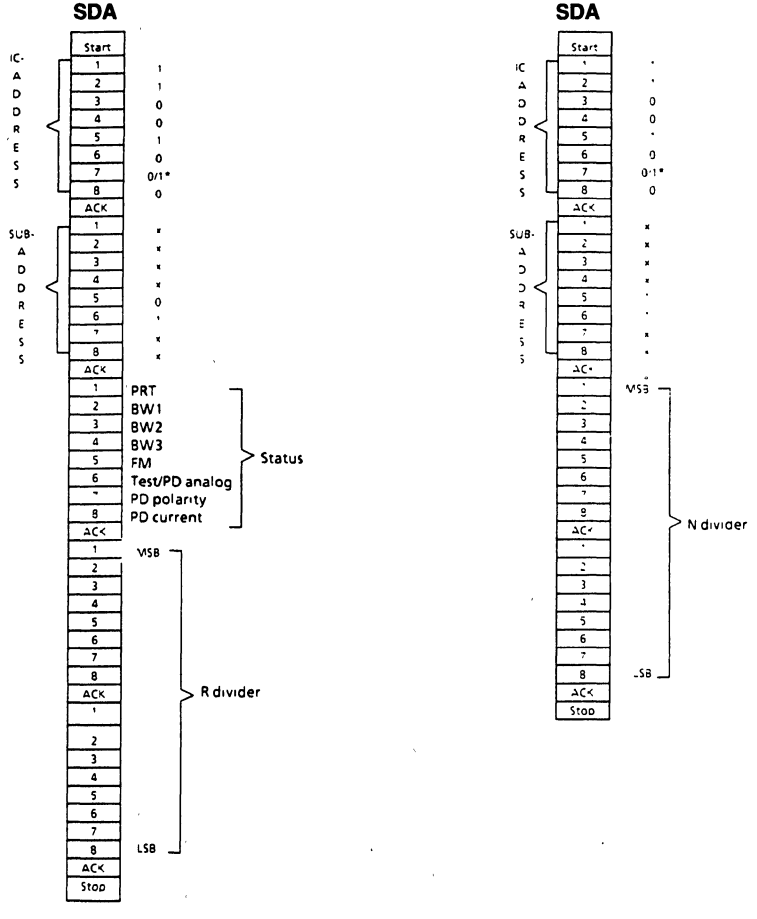
Status Programming Table

Bit	Parameter	Status Bit	
		0	1
1	PRT	L	H
2	BW1	L	H
3	BW2	L	H
4	BW3	L	H
5	FM	L (FM operation)	H (AM operation)*
6	PD analog/test	PD analog	Test**
7	PD polarity	neg.	pos.
8	PD current	0.25 mA	1 mA (AM or FM operation)

*When the band selection output FM is switched from "H" to "L" via bit 5 (FM), operation is switched from AM to FM PDAM is in tristate and vice versa

**In test operation PDFMA and PDAMA outputs are switched as FVN and FRN outputs respectively

I²C Transfer Protocol

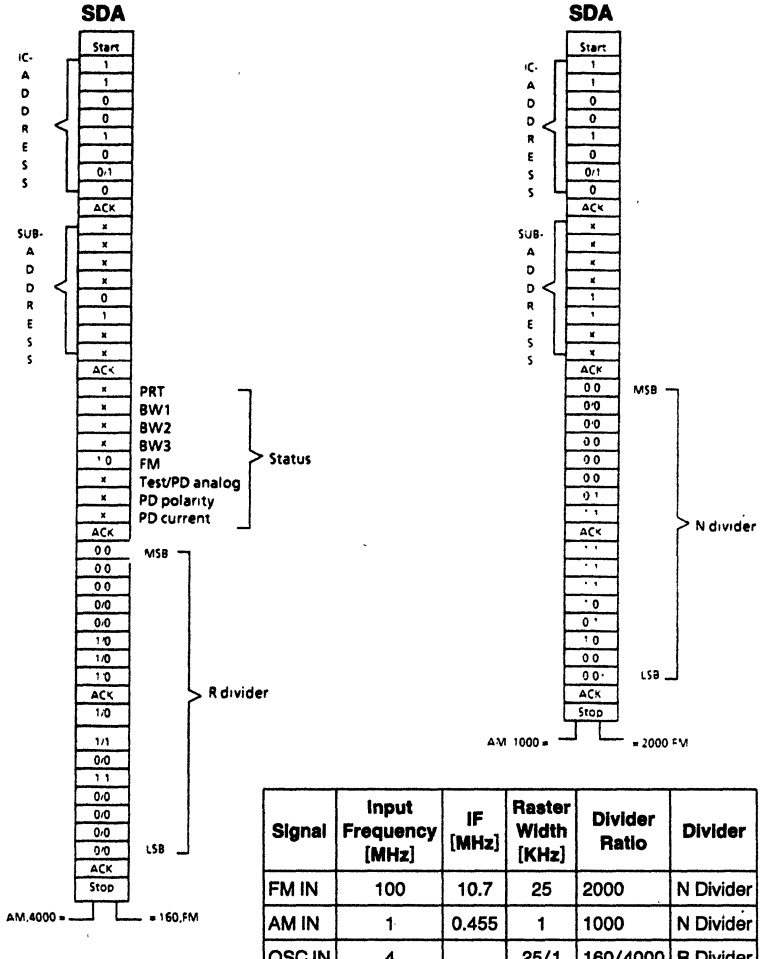


0097-6

*Chip select is achieved via bit 7 for the IC address. The contents are compared with the value set on Pin A0. If the values are identical, the respective chip is selected.

8

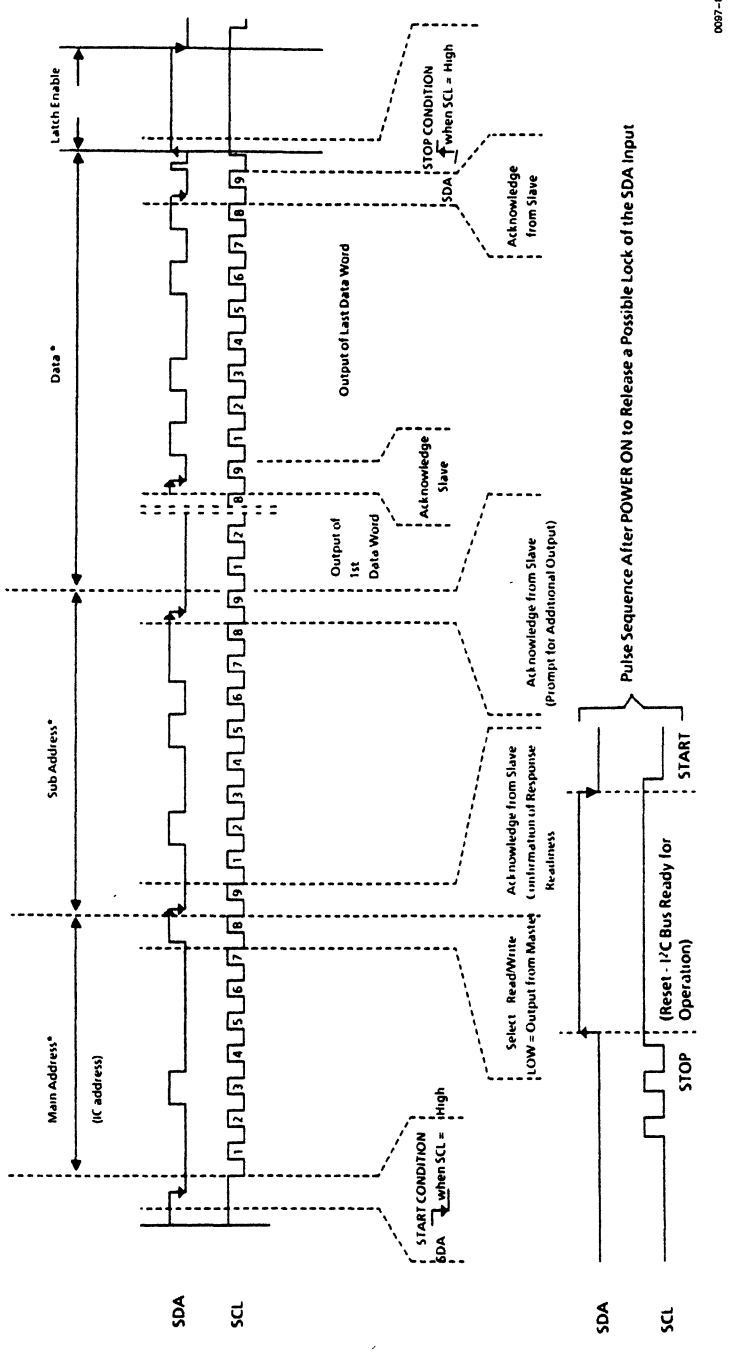
Programming Example



Signal	Input Frequency [MHz]	IF [MHz]	Raster Width [KHz]	Divider Ratio	Divider
FM IN	100	10.7	25	2000	N Divider
AM IN	1	0.455	1	1000	N Divider
OSC IN	4		25/1	160/4000	R Divider

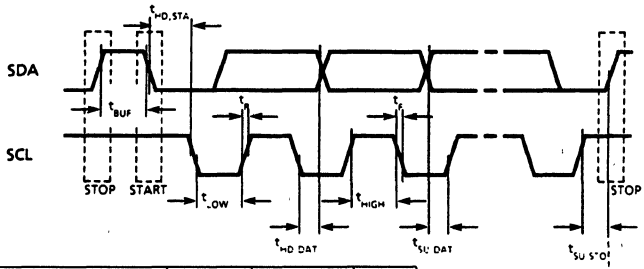
0097-7

Transfer Protocol for I²C Bus

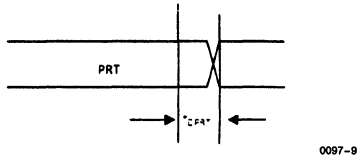


*See K 18 + K 19

I²C Bus Timing, PRT



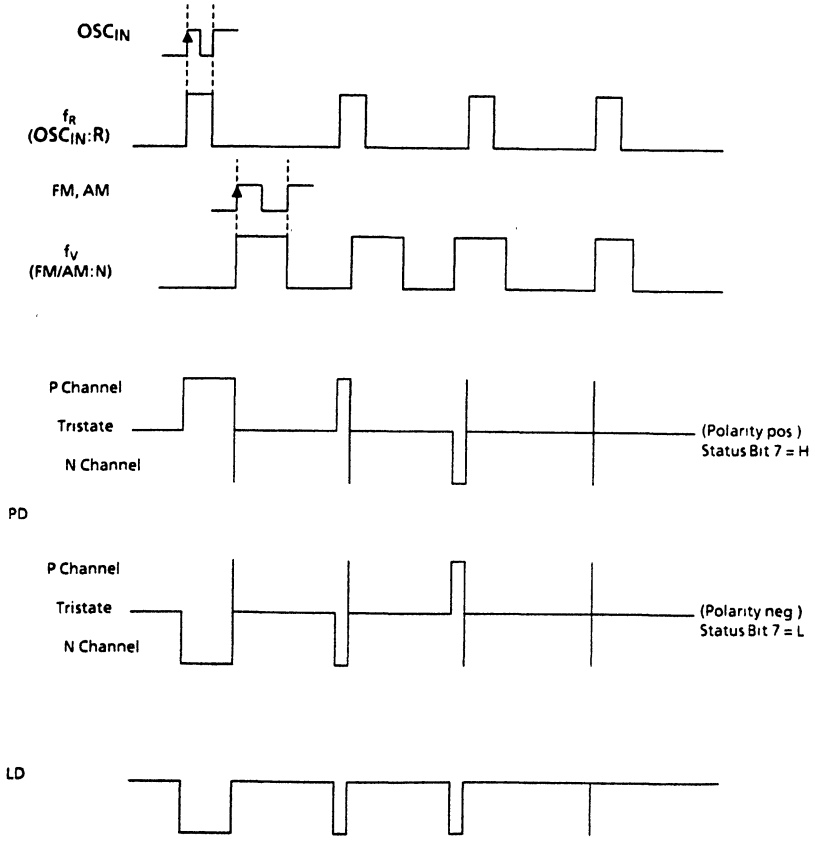
Parameter	Symbol	Limits		Units
		Min	Max	
Clock Frequency	f_{SCL}	0	100	KHz
Hold Time Data to SCL_{LOW}	$t_{HD;\,DAT}$	0		µs
Inactive Time Prior to Next Transfer	t_{BUF}	4.7	—	µs
Hold Time During Start Condition (First CLOCK Pulse is Generated after This Time Period)	$t_{HD;\,STA}$	4.0	—	µs
LOW Clock Phase	t_{LOW}	4.7	—	µs
HIGH Clock Phase	t_{HIGH}	4.0	—	µs
Set-Up Time for DATA	$t_{SU;\,DAT}$	250	—	ns
Rise Time for SDA and SCL Signal	t_R	—	1	µs
Fall Time for SDA and SCL Signal	t_F	—	300	ns
Set-Up Time for SCL Clock during Stop Condition	$t_{SU;\,STO}$	4.7	—	µs
PRT Delay Time Relative to Stop Condition	t_{DPRT}	—	500	µs



0097-9

All values are referenced to specified input levels V_{IH} and V_{IL}.

Pulse Diagram: Phase Detector/Lock Detector



Ordering Information

Type	Order No.	Package
SDA 2121	Q67100-H8621	DIP 20

8

SIEMENS

TCA 440
AM Receiver Circuit

AM receiver circuit for LW, MW, and SW in battery and line operated radio receivers. It includes an RF prestage with AGC, a balanced mixer, separate oscillator, and an IF amplifier with AGC. Because of its internal stabilization, all characteristics are largely independent of the supply voltage. For use in high quality radio sets the TDA 4001 should be preferred to the TCA 440.

Features

- Separately controlled prestage
- Multiplicative push-pull mixer with separate oscillator
- High large signal capability from 4.5 V supply voltage on
- 100 dB feedback control range in 5 stages
- Direct connection for tuning meter
- Few external components

Maximum ratings

Supply voltage	V_S	15	V
Storage temperature range	T_{stg}	−40 to 125	°C
Junction temperature	T_j	150	°C
Thermal resistance (system-air)	R_{thSA}	120	K/W

Operating range

Supply voltage	V_S	4.5 to 15	V
Ambient temperature	T_A	−15 to 80	°C

Characteristics

$V_S = 9$ V; $T_A = 25$ °C; $f_{IRF} = 600$ kHz; $f_{mod} = 1$ kHz

Total current consumption		I_S	10.5	mA
RF level deviation for	$\Delta V_{AF} =$ 6 dB	ΔG_{RF}	65	dB
$m = 80\%$	$\Delta V_{AF} = 10$ dB	ΔG_{RF}	80	dB
AF output voltage for V_{IRF} (symm. measured at 1–2)				
for $m = 80\%$	$V_{IRF} = 20$ µV	$V_{AF\,rms}$	140	mV
	$V_{IRF} = 1$ mV	$V_{AF\,rms}$	260	mV
	$V_{IRF} = 500$ mV	$V_{AF\,rms}$	350	mV
for $m = 30\%$	$V_{IRF} = 20$ µV	$V_{AF\,rms}$	50	mV
	$V_{IRF} = 1$ mV	$V_{AF\,rms}$	100	mV
	$V_{IRF} = 500$ mV	$V_{AF\,rms}$	130	mV
Input sensitivity (measured at 60 Ω, $f_{IRF} = 1$ MHz, $m = 30\%/0\%$, $R_G = 540$ Ω)				
at signal-to-noise ratio $\frac{S+N}{N} = 6$ dB (in acc. with DIN 45405)		V_{IRF}	1	µV
	$\frac{S+N}{N} = 26$ dB	V_{IRF}	7	µV
	$\frac{S+N}{N} = 58$ dB	V_{IRF}	1	mV

RF stage

Input frequency range	f_{IRF}	0 to 50	MHz
Output frequency $f_{IF} = f_{OSC} - f_{IRF}$	f_{IF}	460	kHz
Control range	ΔG_V	38	dB
Input voltage (for 600 kHz, $m = 80\%$) for overdrive ($THD_{AF} = 10\%$), symmetrically measured at pins 1 and 2	$V_{IRF\,pp}$	2.6	V
(mean carrier value)	$V_{IRF\,rms}$	0.5	V
IF suppression between 1–2 and 15	a_{IF}	20	dB
RF input impedance			
a) unsymmetrical coupling			
at $G_{RF\,max}$	Z_I	2/5	kΩ/pF
at $G_{RF\,min}$	Z_I	2.2/1.5	kΩ/pF
b) symmetrical coupling			
at $G_{RF\,max}$	Z_I	4.5	kΩ/pF
at $G_{RF\,min}$	Z_I	4.5/1.5	kΩ/pF
Mixer output impedance (pins 15 or 16)	Z_Q	250/4.5	kΩ/pF

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IF stage

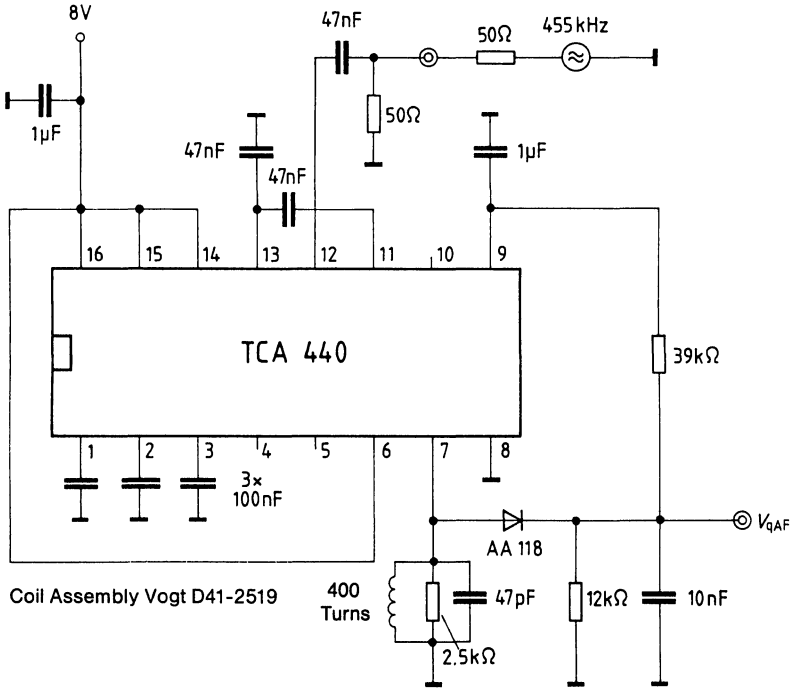
Input frequency range	f_{iIF}	0 to 2	MHz
Control range at 460 kHz	ΔG_V	62	dB
Input voltage (mean carrier value) at G_{min} for overdrive (THD_{AF} = 10%), measured at pin 12 (60 Ω to ground, f_{iIF} = 460 kHz, m = 80%; f_{mod} = 1 kHz)	$V_{IF\,rms}$	200	mV
AF output voltage for V_{iIF} at 60 Ω (pin 12)			
V_{iIF} = 30 µV, m = 80%; f_{mod} = 1 kHz	$V_{7\,AF\,rms}$	50	mV
V_{iIF} = 3 mV, m = 80%; f_{mod} = 1 kHz	$V_{7\,AF\,rms}$	200	mV
V_{iIF} = 3 mV, m = 30%; f_{mod} = 1 kHz	$V_{7\,AF\,rms}$	70	mV
V_{iIF} = 200 µV; m = 30%, f_{IF} = 455 kHz; $f_{q\,AF}$ = 1 kHz	$V_{7\,AF\,rms}$	35 to 60	mV
IF input impedance (unsymm. coupling)	Z_i	3/3	kΩ/pF
IF output impedance	Z_{q7}	200/8	kΩ/pF

Tuning meter

Recommended instruments: 500 µA (R_i = 800 kΩ)
or 300 µA (R_i = 1.5 kΩ)

The IC offers a tuning meter voltage of 600 mV_{EMF} max. with a source impedance of approx. 400 Ω.

Measurement circuit for output voltage



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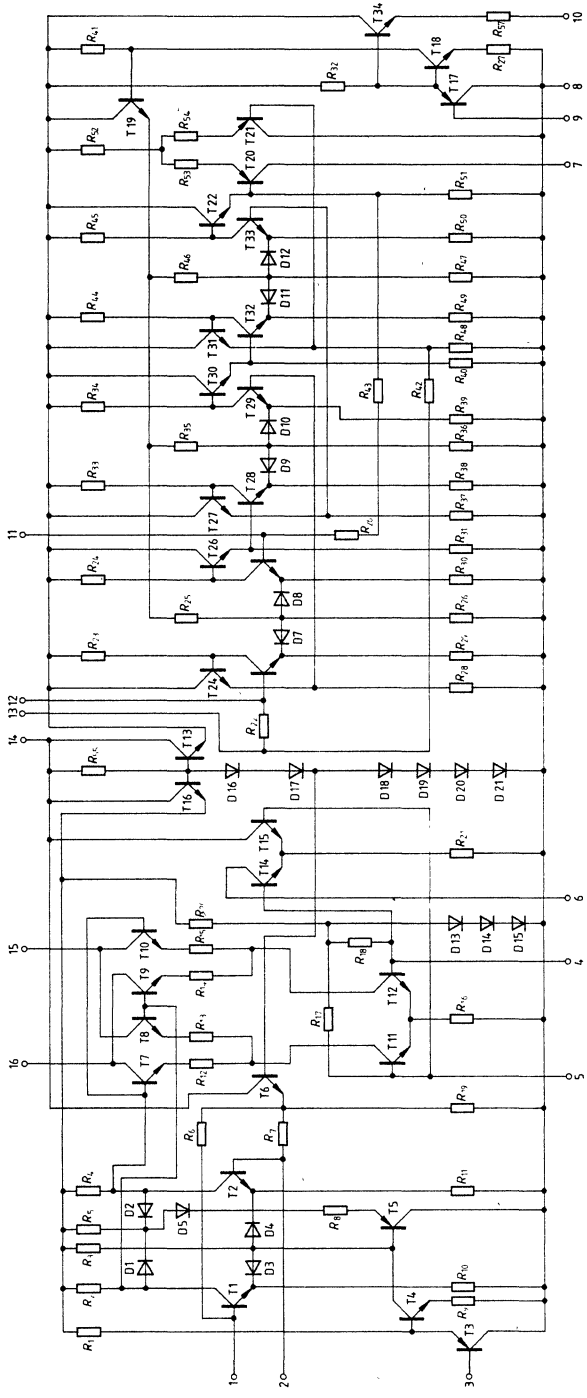
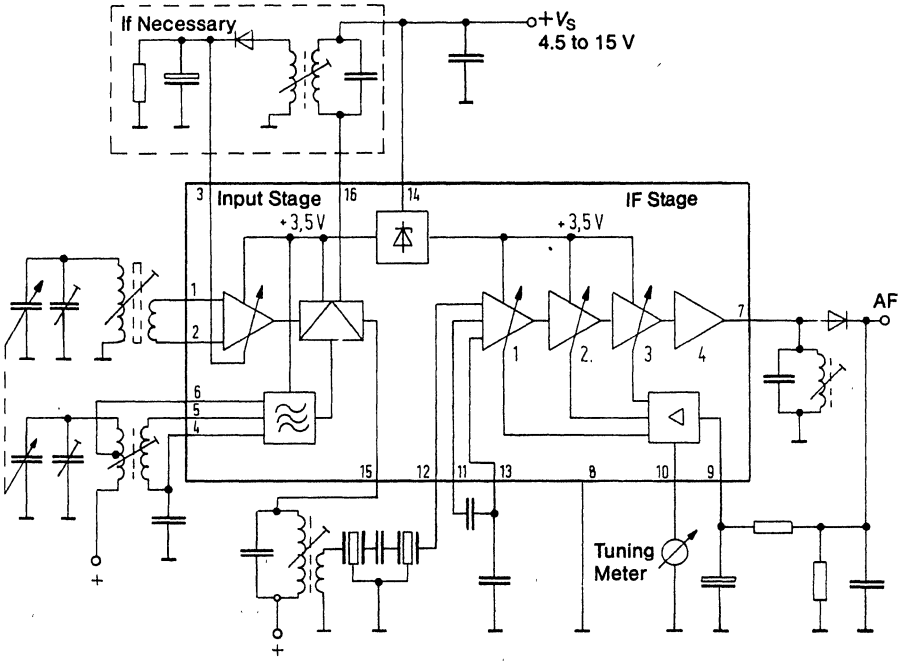
Circuit diagram



Block diagram



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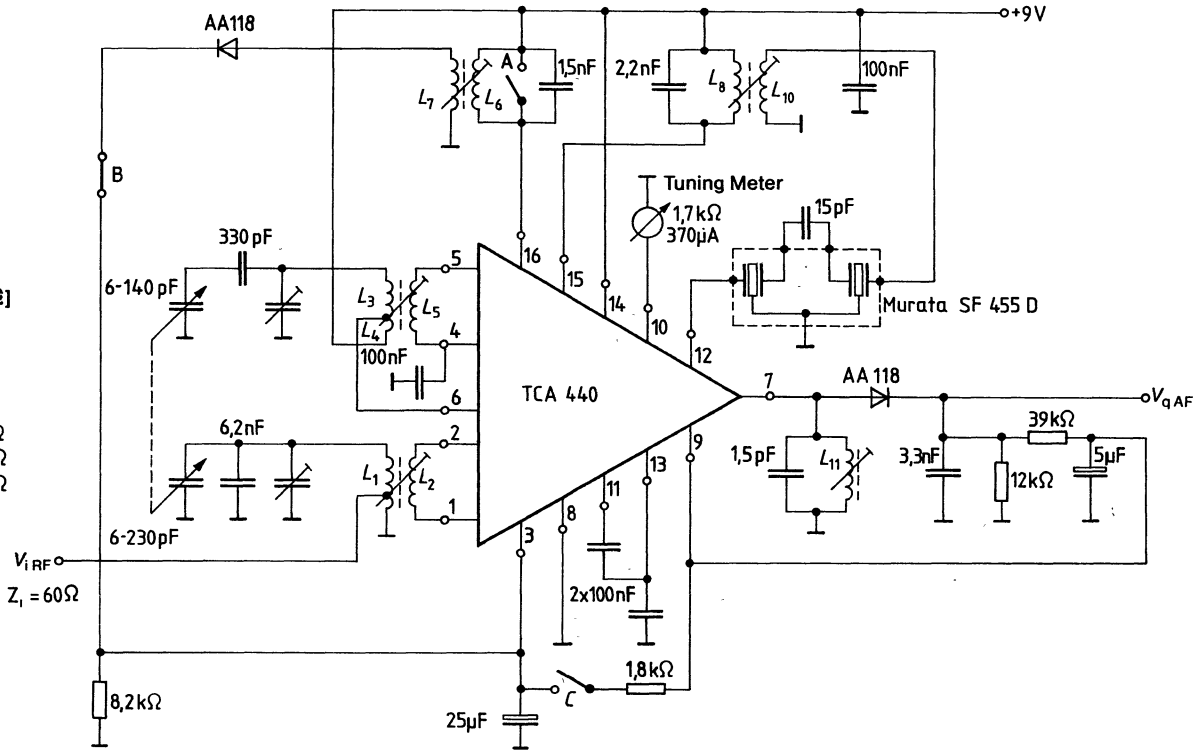
Measurement circuit for signal-to-noise ratio



n[Turns]	R_G [Ω]
1	15
2	60
4	240
6	540
9	1,2kΩ
12	2,2kΩ
18	4,8kΩ

L_1-L_2 M 25 pot core
L_3-L_{11} with coil assembly Vogt D41-2519

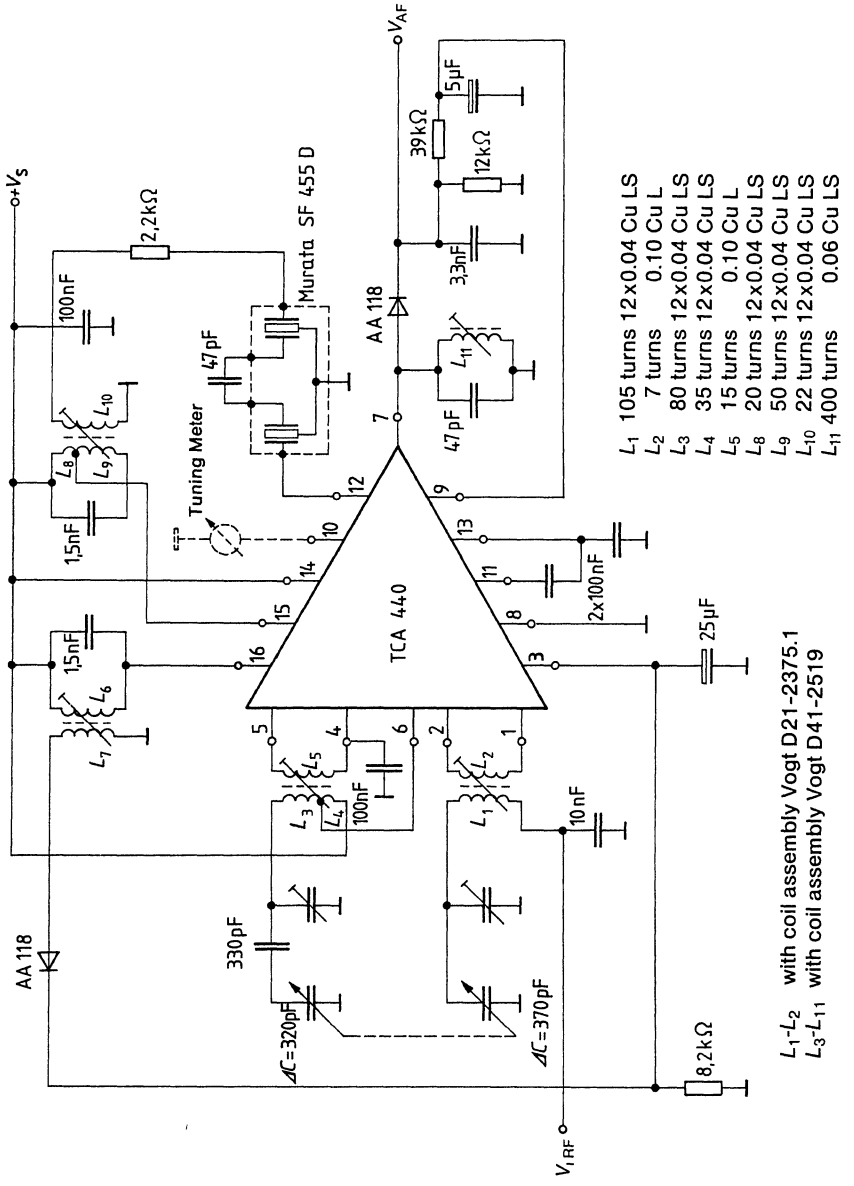
L_1 2+6 turns 6x12x0.04 Cu LS
L_2 n turns 0.15 Cu L
L_3 90 turns 12x0.04 Cu LS
L_4 35 turns 12x0.04 Cu LS
L_5 15 turns 0.10 Cu L
L_6 70 turns 12x0.04 Cu LS
L_7 35 turns 12x0.04 Cu LS
L_8 60 turns 12x0.04 Cu LS
L_{10} 22 turns 12x0.04 Cu LS
L_{11} 68 turns 0.06 CuL

Switch

A	B	C		
off	on	off	separate prestage control	①
on	off	on	prestage control voltage derived from IF control voltage	②

$f_i = 1$ MHz; $m = 30\%$

Application example for MW with TCA 440



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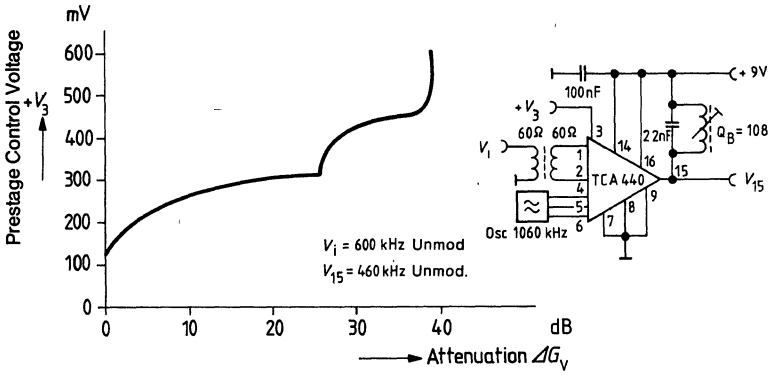
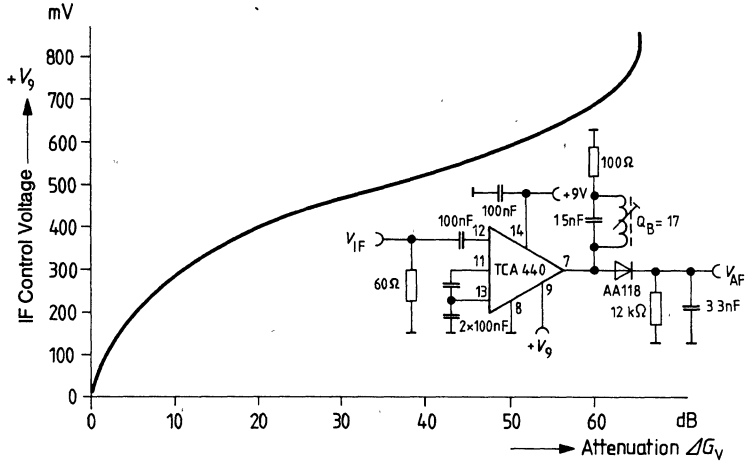
Prestage control TCA 440



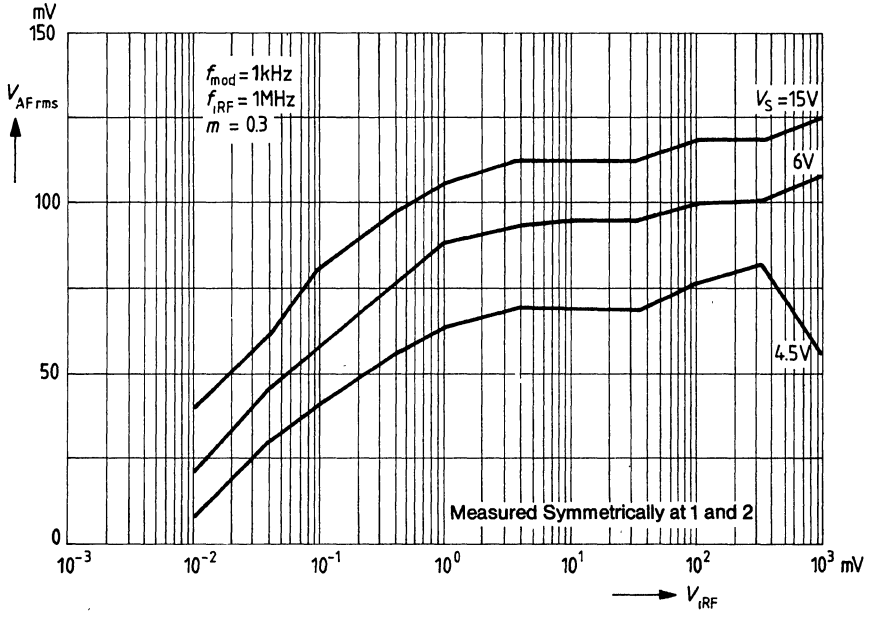
The input ist not power matched and can be driven with a higher resistance. The selected V_i ensures a constant V_{15} (50 mV peak-to-peak).

IF control



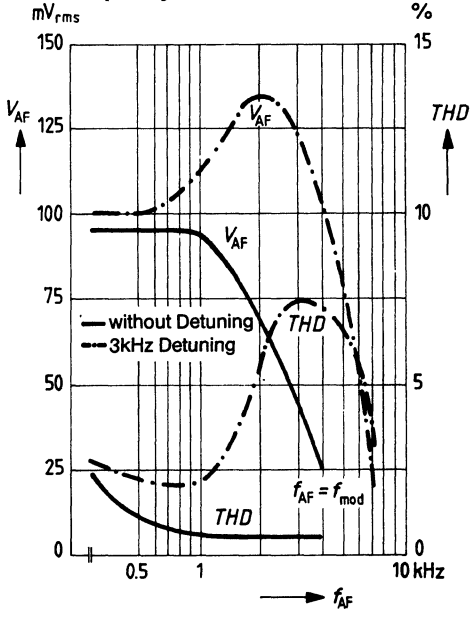
The selected V_{IF} (469 kHz; m = 80%; f_{mod} = 1 kHz) ensures a constant V_{AF} (200 mV, rms).

AF output voltage versus RF input voltage

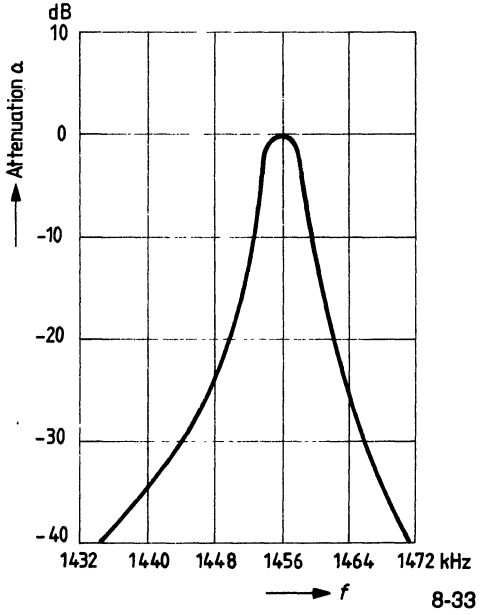


Example for medium wave applications

AF output voltage versus output frequency
Total harmonic distortion versus modulation frequency



Passband characteristic versus input frequency, measured from input to output of the circuit



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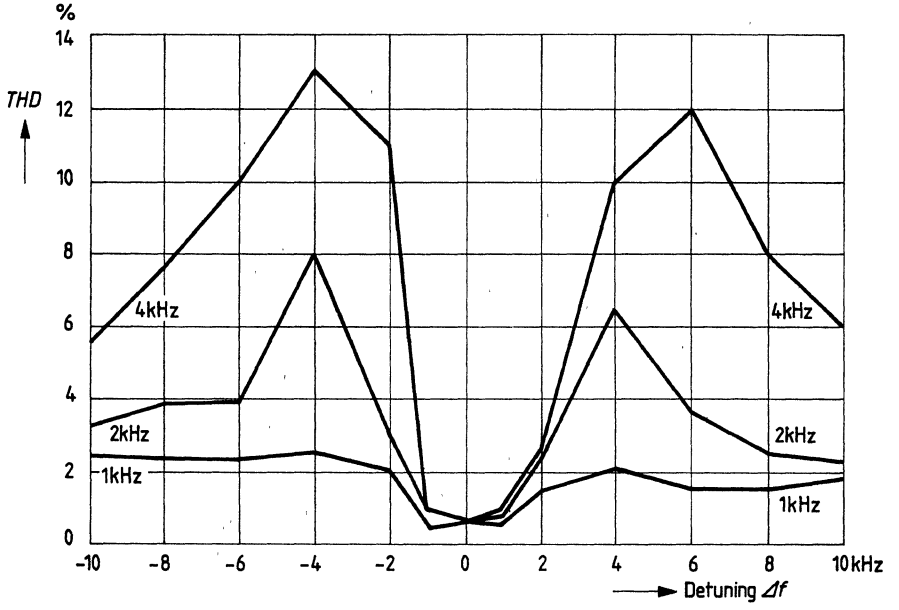
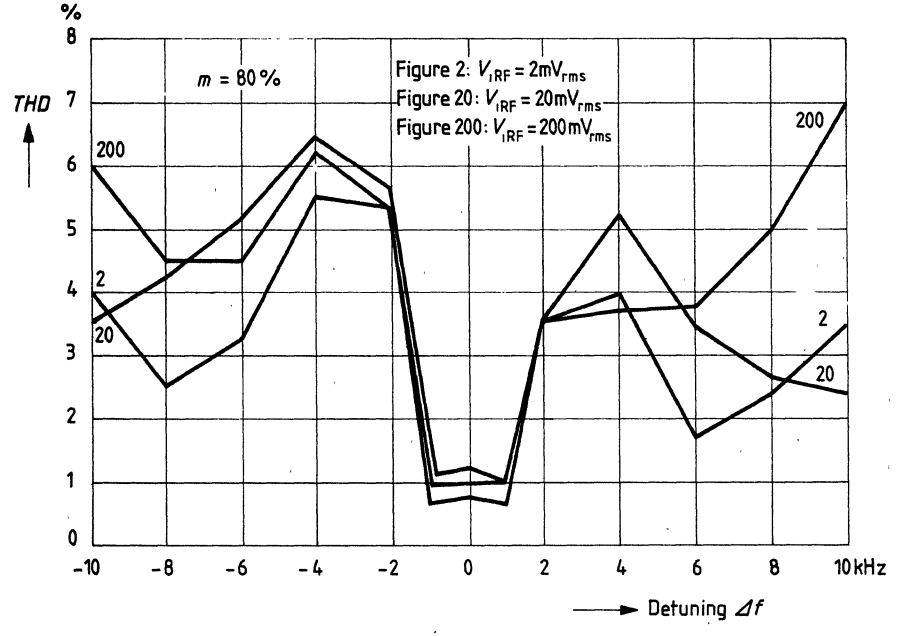
Total harmonic distortion versus detuning (parameter: modulation frequency)

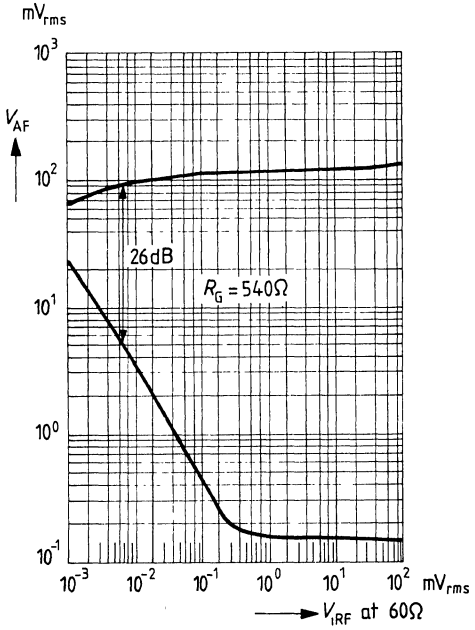
$V_S = 9$ V $f_{OSC} = 1.455$ MHz ± Δf $m = 30\%$
$f_{IRF} = 1$ MHz $f_{IF} = 455$ kHz $V_{IRF} = 20$ mV$_{rms}$



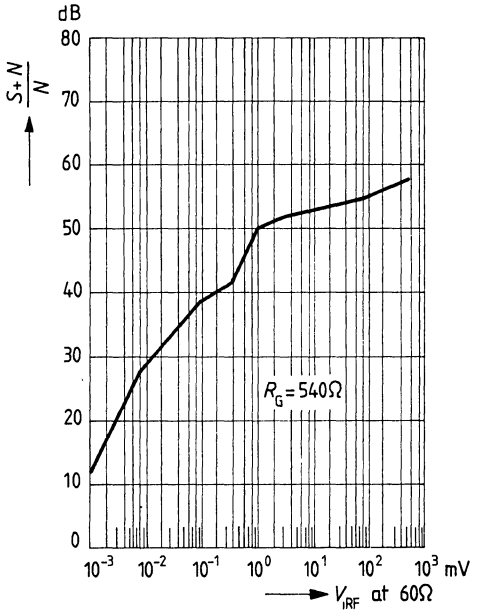
Total harmonic distortion versus detuning (parameter: RF input voltage)



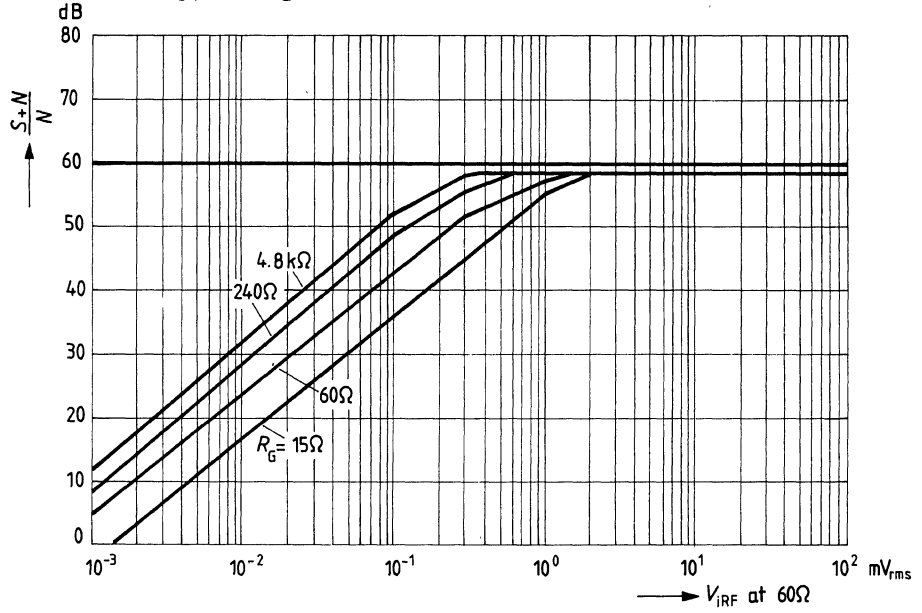
AF output voltage and noise figure versus RF input voltage
switching position ①



Signal-to-noise ratio versus RF input voltage
switching position ②



Signal-to-noise ratio versus RF input voltage
(parameter is generator impedance)
switching position ①



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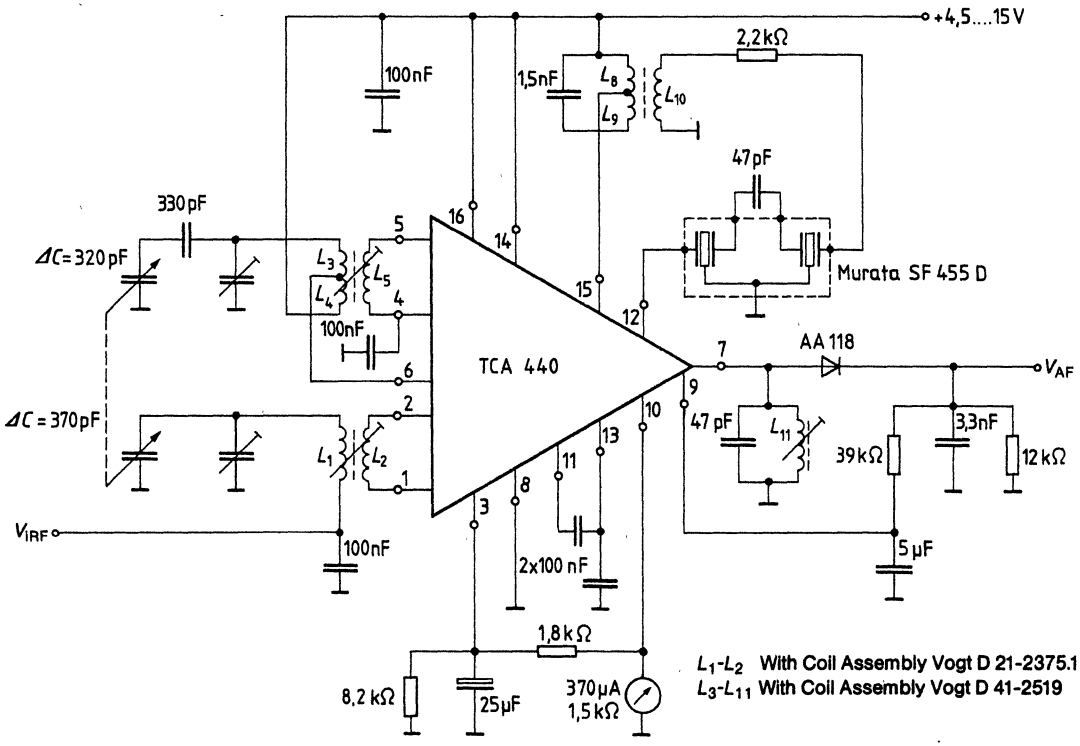
Application example for MW

Prestage control is derived from IF control

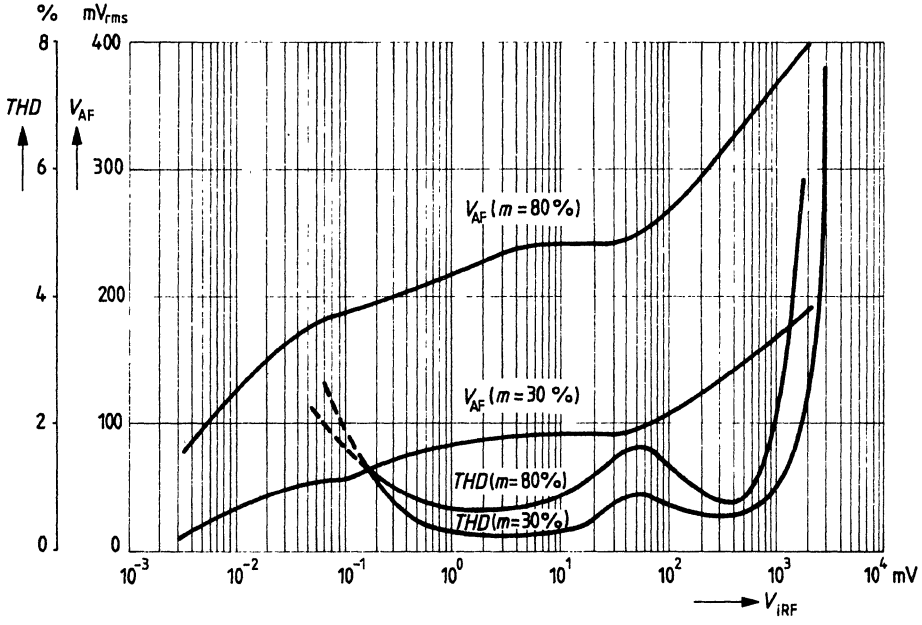


L_1 105 turns 12x0.04 Cu LS
L_2 7 turns 0.10 Cu L
L_3 80 turns 12x0.04 Cu LS
L_4 35 turns 12x0.04 Cu LS
L_5 15 turns 0.10 Cu L
L_8 20 turns 12x0.04 Cu LS
L_9 50 turns 12x0.04 Cu LS
L_{10} 22 turns 12x0.04 Cu LS
L_{11} 400 turns 0.04 Cu L

Test figures for application example for MW

Total harmonic distortion and AF output voltage versus RF input voltage measured symmetrically at pins 1 and 2

$f_i = 1$ MHz, $f_{mod} = 1$ kHz, $f_{IF} = 455$ kHz, $V_S = 9$ V



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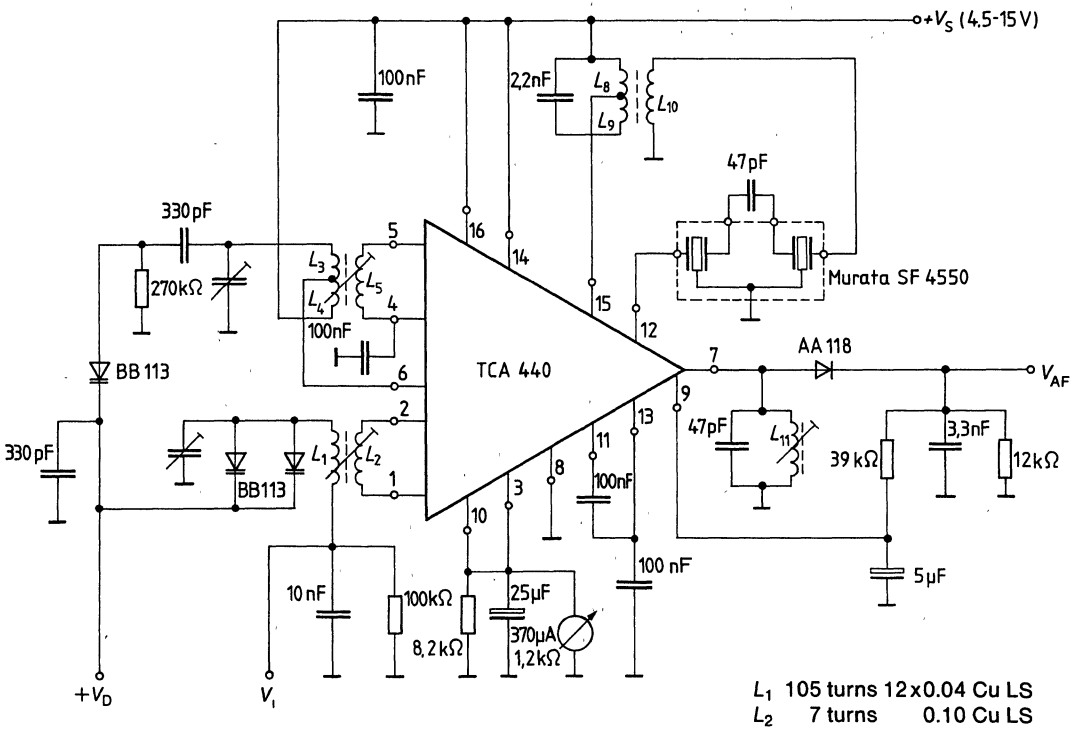
Application example for MW using BB 113 varicap diodes

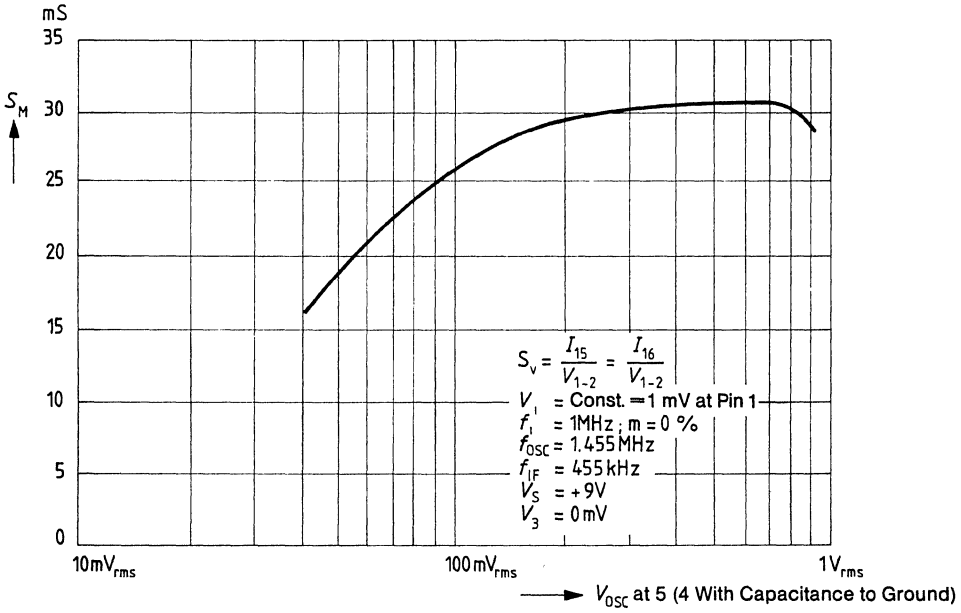


L_1-L_2 With Coil Assembly Vogt D21-2375.1
L_3-L_{11} With Coil Assembly Vogt D41-2519

V_{tun} = 8.5 V ⟶ f_t = 800 kHz
V_{tun} = 30 V ⟶ f_t = 1620 kHz

L_1	105 turns	12x0.04 Cu LS
L_2	7 turns	0.10 Cu LS
L_3	80 turns	12x0.04 Cu LS
L_4	35 turns	12x0.04 Cu LS
L_5	15 turns	0.10 Cu LS
L_8	20 turns	12x0.04 Cu LS
L_9	50 turns	12x0.04 Cu LS
L_{10}	22 turns	12x0.04 Cu LS
L_{11}	400 turns	0.06 Cu L

Conversion transconductance versus oscillator voltage



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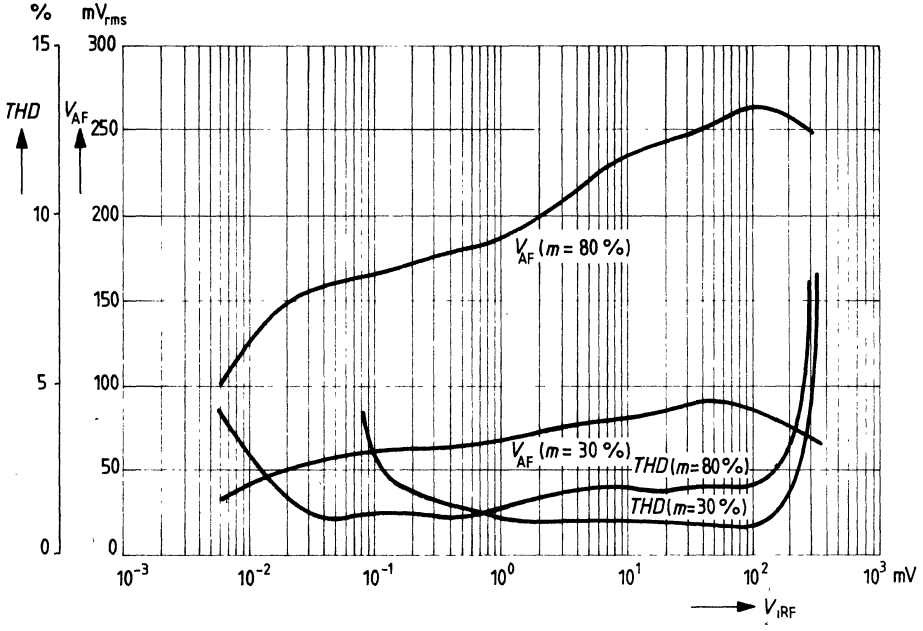
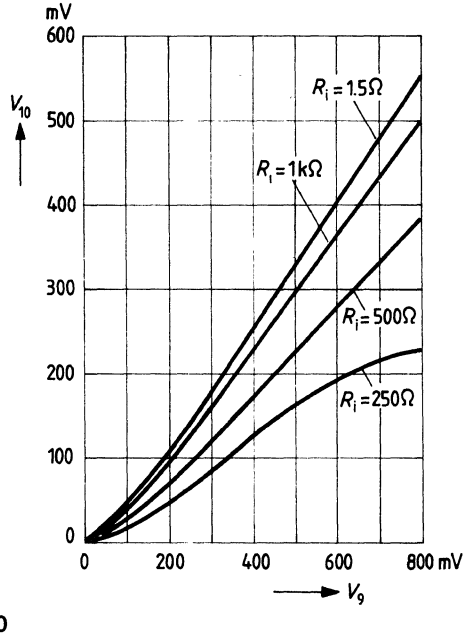
Measured values for application example for MW using diode BB 113

AF output voltage and total harmonic distortion versus RF input voltage
$f_i = 1$ MHz; $f_{mod} = 1$ kHz; $f_{IF} = 455$ kHz
$V_S = 9$ V; V_{iRF} symmetrically measured at pins 1 and 2



Tuning meter voltage versus IF control voltage
(parameter: impedance of tuning meter)



Example for moving coil instruments

R_i	Full-service deflection
1.5 kΩ	100 µA
1.5 kΩ	170 µA
2 kΩ	200 µA
350 Ω	500 µA

SIEMENS

TDA 1037
AF Power Amplifier IC with Thermal Shutdown

AF power amplifier designed for a wide range of supply voltages to enable versatile application in entertainment electronics. The amplifier operates in the push-pull B mode and is available in the SIP 9 package. The integrated shutdown protects the IC from overheating.

Features

- Wide supply voltage range: 4 V to 28 V
- High output power up to 8 W
- Large output current up to 2.5 A
- Simple mounting

Maximum ratings

Supply voltage $R_L \geq 16\ \Omega$	V_S	30	V
Supply voltage $R_L \geq 8\ \Omega$	V_S	24	V
Supply voltage $R_L \geq 4\ \Omega$	V_S	20	V
Output peak current (not repetitive)	I_q	3.5	A
Output current (repetitive)	I_q	2.5	A
Junction temperature*)	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance			
junction-case	$R_{th\,JC}$	12	K/W
system-air	$R_{th\,SA}$	70	K/W

Operating range

Supply voltage	V_S	4 to 28	V
Ambient temperature	T_A	−25 to 85	°C

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*) May not be exceeded even as instantaneous value.

Characteristics

with reference to test circuit

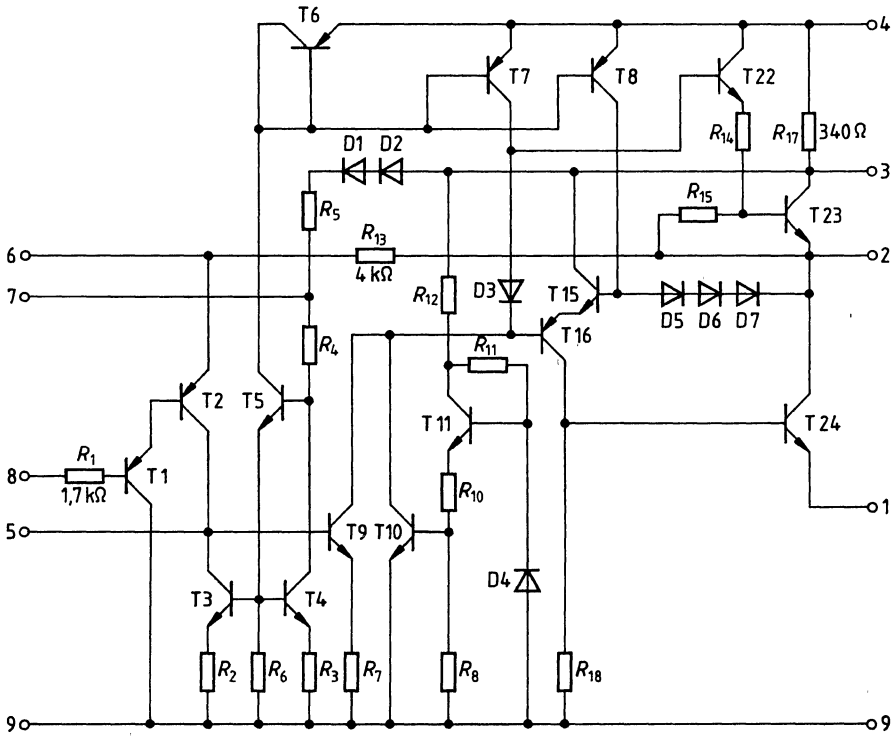
1. $V_S = 12$ V; $R_L = 4\ \Omega$; $C_1 = 1000\ \mu$F; $f_i = 1$ kHz; $T_A = 25$ °C

		min	typ	max	
Quiescent output voltage	V_{q2}	5.4	6.0	6.6	V
Quiescent drain current	$I_3 + I_4$		12	20	mA
Input DC current	I_{i8}		0.4	4	μA
Output power $THD = 1\%$	P_q	2.5	3.5		W
$THD = 10\%$	P_q	3.5	4.5		W
Voltage gain (closed loop)	G_V	37	40	43	dB
Voltage gain (open loop)	G_{V0}		80		dB
Total harmonic distortion ($P_q = 0.05$ to 2.5 W)	THD		0.2		%
Noise voltage referred to input ($f_i = 3$ Hz to 20 kHz)	V_n		3.8	10	μV_S
Disturbance voltage in acc. with DIN 45405 referred to input	V_d		2.5		μV
Hum suppression ($f_{hum} = 100$ Hz)	a_{hum}		48		dB
Frequency range (−3 dB)					
$C_4 = 560$ pF	f	40		20,000	Hz
$C_4 = 1000$ pF	f	40		10,000	Hz
Input resistance	R_{i8}	1	5		MΩ

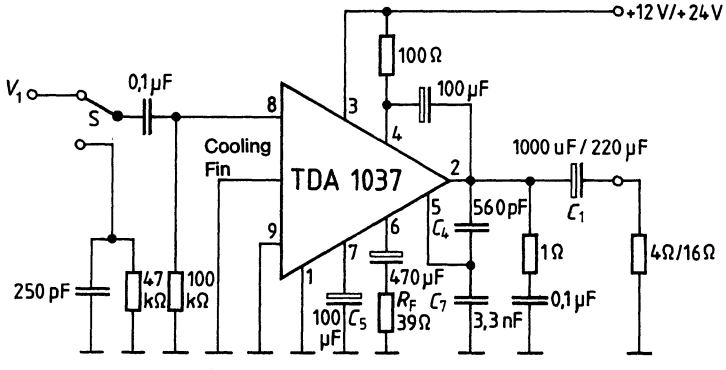
2. $V_S = 24$ V; $R_L = 16\ \Omega$; $C_1 = 220\ \mu$F; $f_i = 1$ kHz; $T_A = 25$ °C

Quiescent output voltage	V_{q2}	11	12	13	V
Quiescent drain current	$I_3 + I_4$		18	30	mA
Input DC current	I_{i8}		0.8	8	μA
Output power $THD = 1\%$	P_q		3.5		W
$THD = 10\%$	P_q	4.5	5.0		W
Voltage gain (closed loop)	G_V	37	40	43	dB
Voltage gain (open loop)	G_{V0}		80		dB
Total harmonic distortion ($P_q = 0.05$ to 3 W)	THD		0.2	0.5	%
Noise voltage with reference to input $f_i = 3$ Hz to 20 kHz	V_n		5	15	μV_S
Disturbance voltage in acc. with DIN 45405 referred to input	V_d		3.8		μV
Hum suppression ($f_{hum} = 100$ Hz)	a_{hum}		40		dB
Frequency range (−3 dB)					
$C_4 = 560$ pF	f	40		20,000	Hz
$C_4 = 1000$ pF	f	40		10,000	Hz
Input resistance	R_{i8}	1	5		MΩ

Circuit diagram

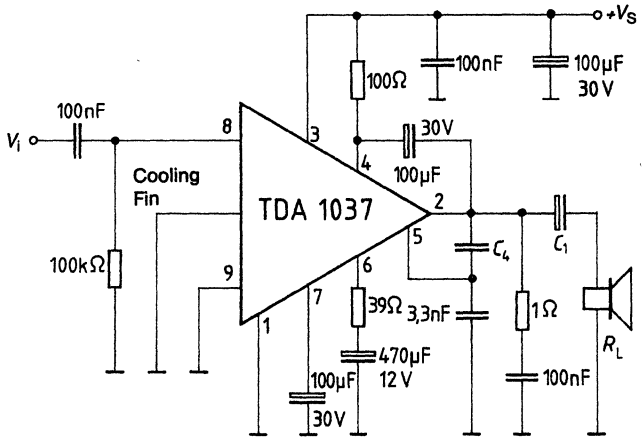


Measurement circuit



S Closed for Noise Measurement

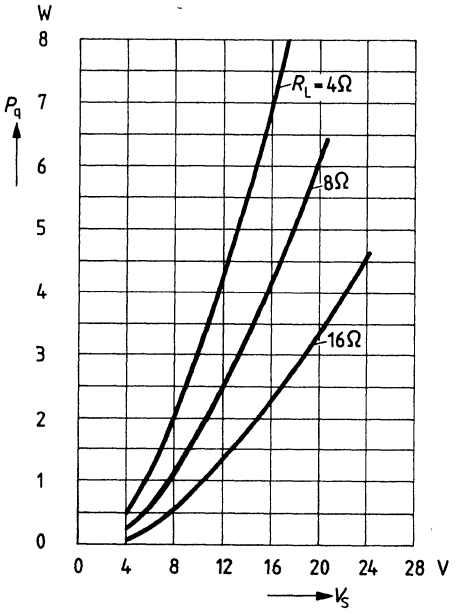
Application circuit



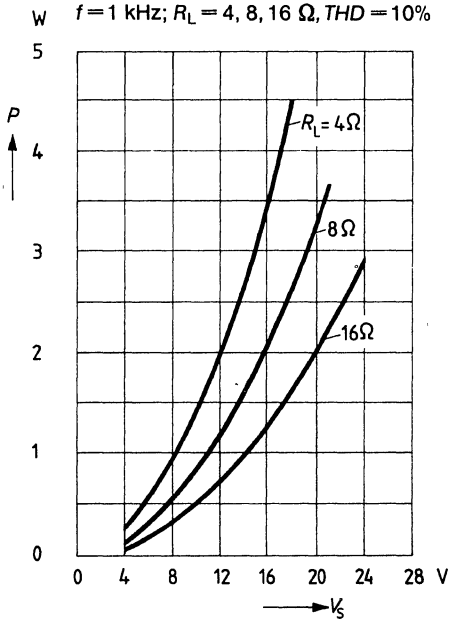
V_S	12 V	18 V	24 V
R_L	4 Ω	8 Ω	16 Ω
C_1	1000 µF	470 µF	220 µF

f_{max}	10 kHz	20 kHz
C_4	1000 pF	560 pF

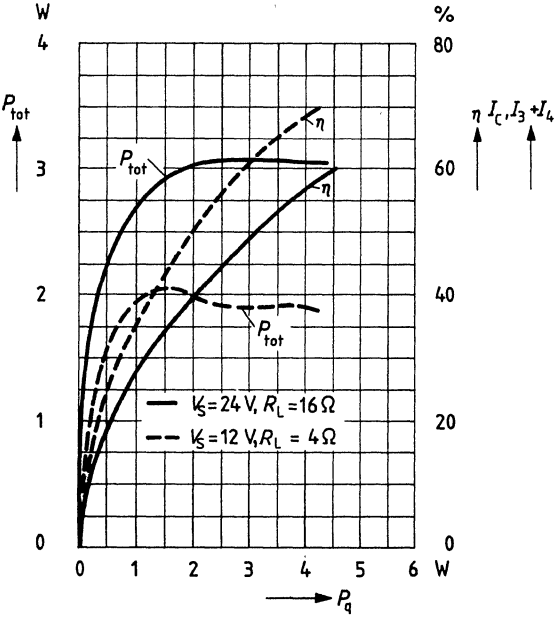
Output power versus supply voltage
THD = 10%; R_L = 4, 8, 16 Ω; *f* = 1 kHz



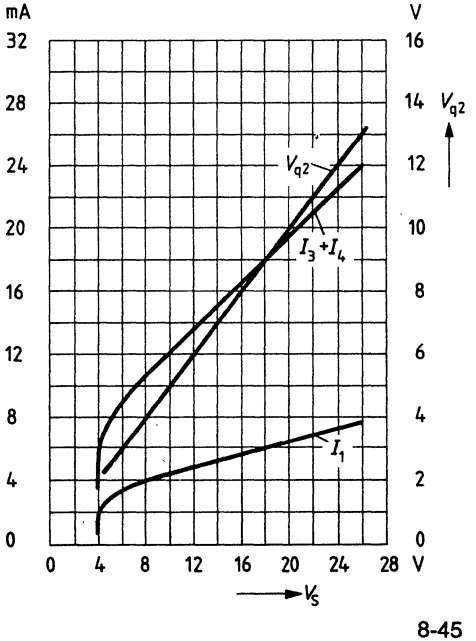
Max. power dissipation versus supply voltage at sine-shaped driving
f = 1 kHz; R_L = 4, 8, 16 Ω, *THD* = 10%



Total power dissipation and efficiency versus output power
THD = 10%; *f* = 1 kHz



Quiescent drain current, quiescent current of output transistors, quiescent output voltage versus supply voltage



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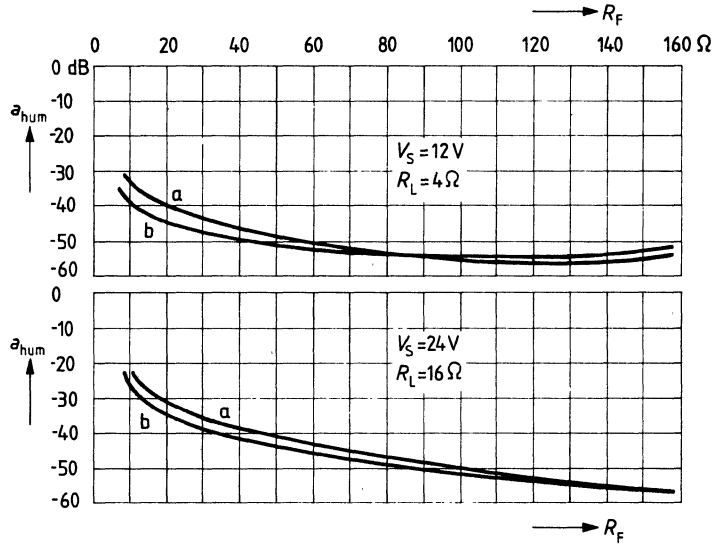
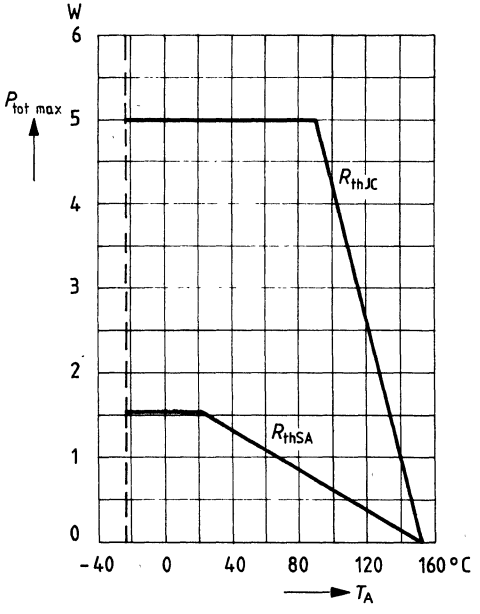
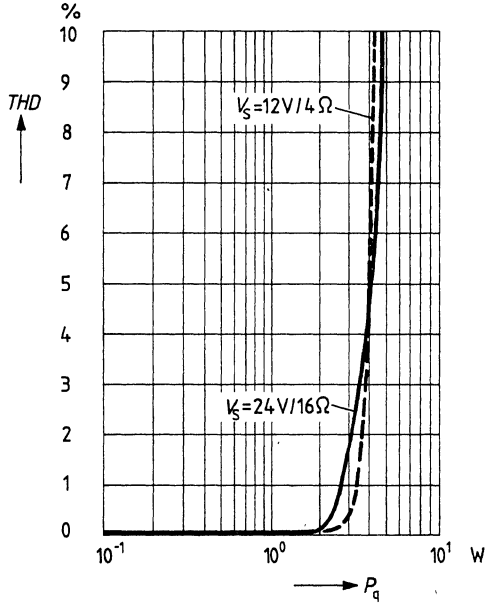
Hum suppression versus feedback resistance
f_{hum} = 100 Hz; C_5 = 100 µF
a: input short-circuited
b: input open



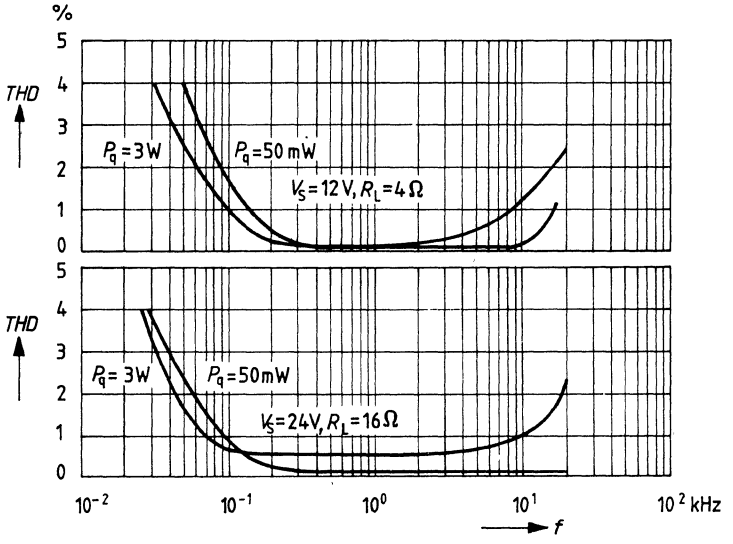
Max. total power dissipation versus ambient temperature



Total harmonic distortion versus output power
$f = 1$ kHz

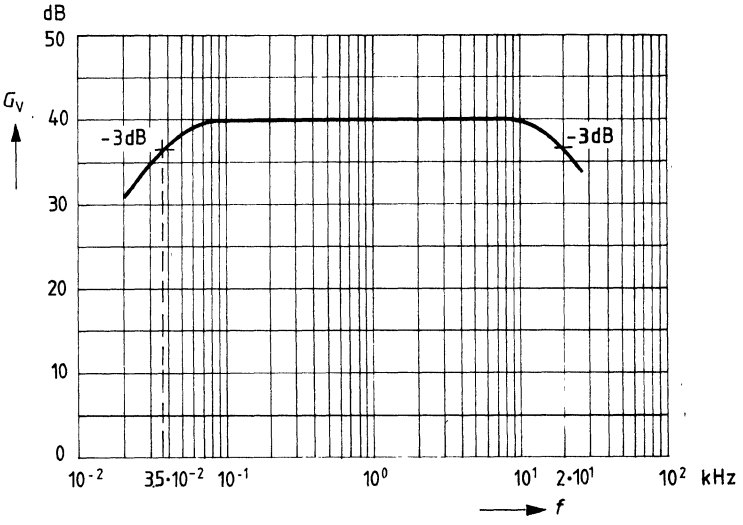


Total harmonic distortion versus frequency

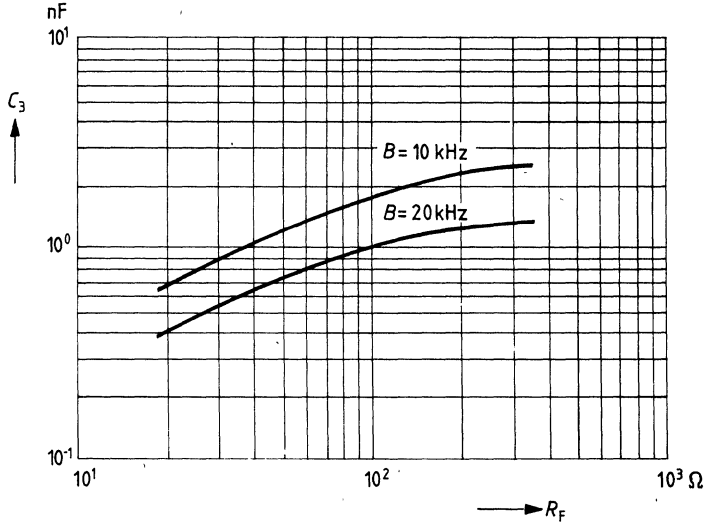


8

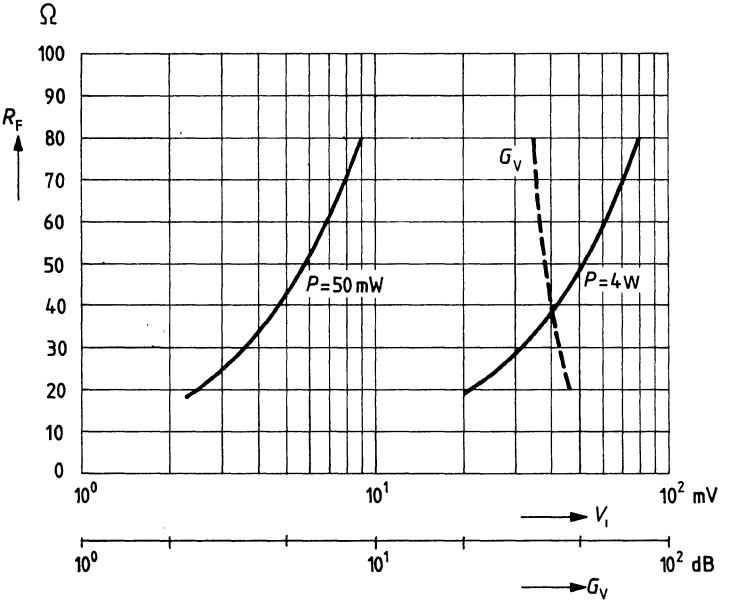
Voltage gain versus frequency
$V_S = 12$ V; $R_L = 4\ \Omega$



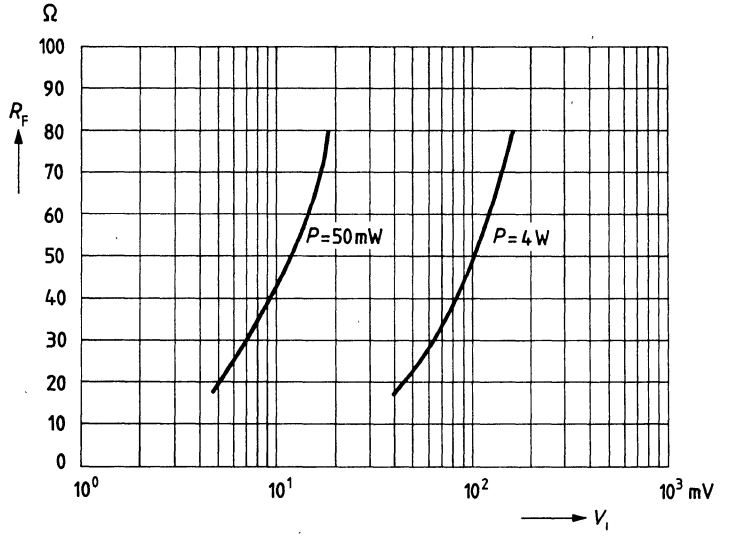
Bandwidth C_3 versus feedback resistance
$V_S = 12$ V; $R_L = 4\ \Omega$, $G_V = 40$ dB
$C_1 = 5 \cdot C_4$



Output power and voltage gain versus feedback resistance and input voltage
$V_S = 12$ V; $R_L = 4\ \Omega$; $f = 1$ kHz



Output power versus feedback resistance and input voltage
$V_S = 24$ V; $R_L = 16\ \Omega$; $f = 1$ kHz



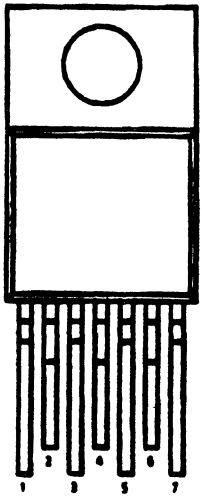
8

SIEMENS

Preliminary

TDA 2025
50 Watt Power Amplifier

Pin Configuration



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Pin Definitions

Pin	Function
1	Non-Inverting Output
2	Input
3	V_S
4	Power Ground
5	Hum Suppression
6	Pre-Stage Ground
7	Inverting Output

The TDA 2025 is a 20W to 50W watt power amplifier for Automotive and Entertainment applications featuring full protection from external thermal and electrical malfunctions.

The IC combines 2 complete power amplifiers configured as a class A-B bridge. The integrated resistor network in the positive and negative feedback loops set the gain for each amplifier to 30 dB. The inputs for the inverting and non-inverting gain (pre-amp) stages are tied in parallel resulting in a full bridge configuration with 36 dB of gain and superior "switch-on"/"switch-off" characteristics.

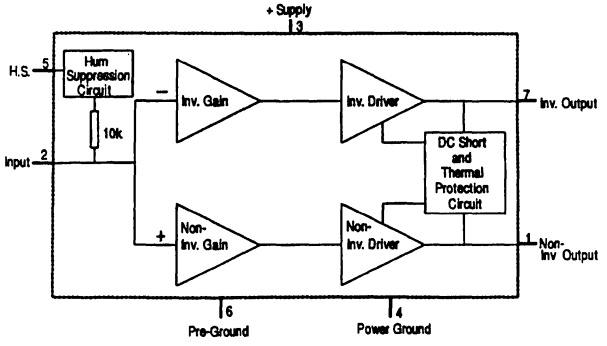
The output power drivers are designed to drive either 4Ω (V_S < 24V) or 8Ω (V_S < 45V) speakers at currents up to 4A.

An internal hum suppression circuit using an external capacitor is also available at pin 5 with 100 μF at 3V used as a typical value.

The output driver stages are short circuit protected to both ground and V_S, and an internal thermal "fuse" circuit protects the output stage against thermal damage.

An internal DC protection circuit prevents speaker overload if one output is shorted to ground.

Block Diagram



Absolute Maximum Ratings*

Supply Voltage (V_S) ..... 0.3V to 45V
Output Current ($I_{1,7}$) ..... −4.0A to +4.0A
Input Voltage (Pin 5) (V_5) ..... −0.3V to 6.0V
Input Voltage (Pin 2) (V_2) ..... −0.3V to V_S
Junction Temperature (T_j) ..... +150°C
Storage Temperature (T_{stg}) ..... −50°C to +150°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Caution

Exceeding absolute maximum ratings may result in irreversible damage to the integrated circuit.

Recommended Operating Range

Parameter	Symbol	Conditions	Limits		Units
			Min	Max	
Supply Voltage	V_S		8	42	V
Case Temperature	T_c	P_V = 25W	−25	+75	°C
Thermal Resistance	R_{thSC}			3	K/W

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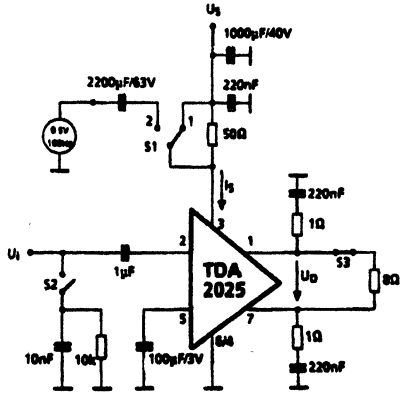
Characteristics

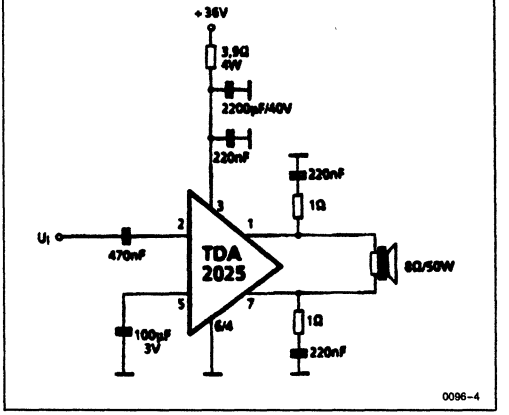
Parameter	Symbol	Conditions	Limits			Units
			Min	Typ	Max	
Quiescent Current	I_S	S3 Open		40	60	mA
Differential Output	V_D			±0.5		V
Input Impedance	R_i			10		kΩ
Output Power	P_q	V_S = 14.4V; R_L = 4Ω; THD = 1%	12	15		W
	P_q	V_S = 14.4V; R_L = 4Ω; THD = 10%	18	20		W
	P_q	V_S = 32V; R_L = 8Ω; THD = 1%	36	40		W
	P_q	V_S = 32V; R_L = 8Ω; THD = 10%	45	50		W
Hum Suppression	a_{SVR}	S1 pos. 2, S2 closed	37	40		dB
Supply Current	I_S	P_q = 50W, f = 1 KHz		2.3		A
Efficiency	n	P_q = 50W, f = 1 KHz		70		%
Total Harmonic Distortion	THD	P_q = 0.1W to 30W, f = 40 Hz to 15 KHz		0.2		%
Power Bandwidth	B	P_q = 30W, −3 dB at 1 KHz	20 Hz to 50 KHz			
Noise	V_n	DIN 45405, S2 Closed		5		μV
Voltage Gain	A_V	R_L = 8Ω, P_q = 10W	34	36	38	dB
Output Protection (Activation Level)	$V_{1(7)}$	Pin 1 or 7 shorted to GND and V_S > 10V		0.25	0.5	V

The Characteristics listed above are ensured over the operating range of the TDA 2025. Typical Characteristics specify mean values expected over the production spread. Typical characteristics apply to T_a = 25°C at mean supply voltage unless otherwise stated.

Test Circuit



Typical Application



Performance Characteristics

Test Conditions: Frequency = 1 KHz, Load Resistance = 4Ω

V_s (V)	I_s (A)	P_v (W)	P_q (W)	n (%)	THD (%)
8.06	0.453	2.64	3.65	28	0.10
8.02	0.801	3.24	6.42	50	0.59
8.02	0.835	3.23	6.69	52	0.99
8.01	0.940	3.19	7.53	58	5.01
8.00	0.997	3.20	7.98	60	10.02
14.46	1.448	10.43	20.93	50	0.12
14.44	1.630	10.12	23.53	57	0.59
14.43	1.677	10.10	24.20	58	0.99
14.42	1.830	9.81	26.38	63	5.00
14.40	1.942	9.66	27.98	65	10.01
22.15	1.742	23.60	38.59	39	0.11
22.09	2.316	24.39	51.17	52	0.59
22.09	2.368	24.31	52.31	54	0.99
22.07	2.562	24.10	56.54	57	4.99
22.05	2.725	24.02	60.10	60	10.01

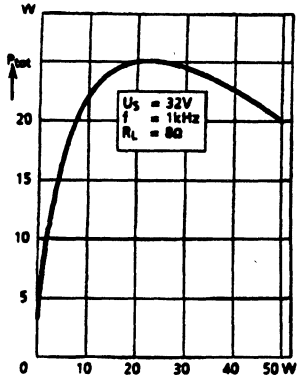
Note:
V_S = 24V Max. with R_L = 4Ω.

Test Conditions: Frequency = 1 KHz, Load Resistance = 8Ω

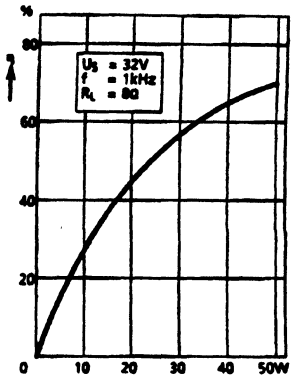
V_s (V)	I_s (A)	P_v (W)	P_q (W)	n (%)	THD (%)
28.06	1.512	19.93	42.43	53	0.05
28.03	1.735	18.66	42.64	62	0.12
28.02	1.880	17.33	52.68	67	0.99
28.00	2.016	16.21	56.44	71	5.00
27.99	2.135	15.33	59.76	74	10.01
32.15	1.613	26.87	51.86	48	0.04
32.12	1.888	25.62	60.63	58	0.10
32.09	2.140	23.08	68.66	66	0.99
32.07	2.281	21.75	73.15	70	5.00
32.06	2.423	20.56	77.67	74	10.00
36.15	1.787	34.57	64.62	46	0.05
36.12	2.033	33.47	73.45	54	0.10
36.09	2.357	29.90	85.06	65	0.99
36.07	2.510	28.20	90.53	69	4.99
36.06	2.667	26.70	96.18	72	9.99

Note:
V_S = 45V Max. with R_L = 8Ω.

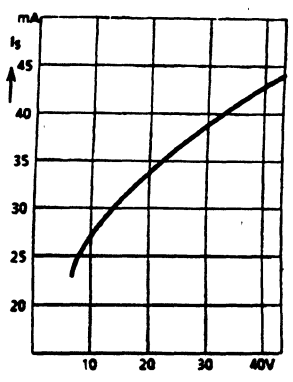
Power Dissipation vs Output Power



Efficiency vs Output Power



Quiescent Current vs Power Supply Voltage



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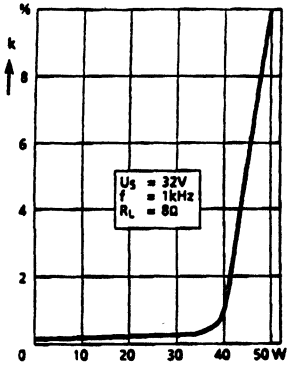
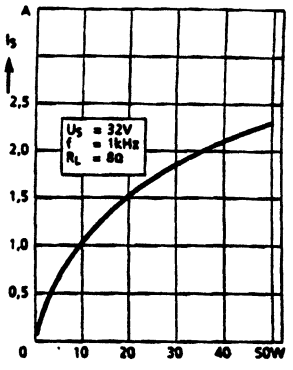
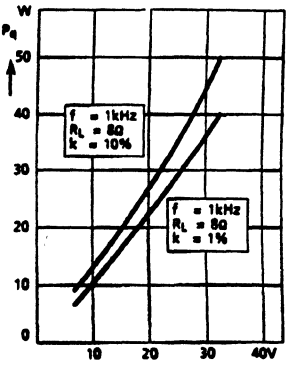
THD vs Output Power



Supply Current vs Output Power



Output Power vs Power Supply Voltage



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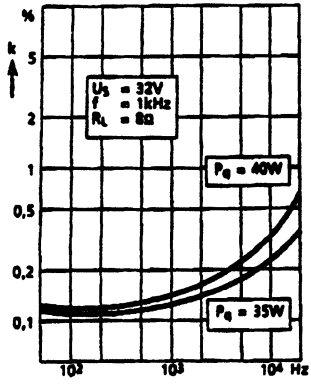
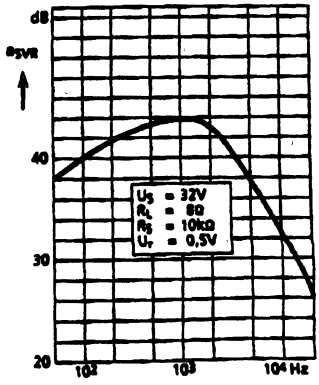
THD vs Frequency



Hum Suppression vs Frequency



0096-8

Ordering Information

Type	Ordering Code	Package
TDA 2025	Q67000-A8186	TO220/7

TDA 4010
AM Receiver for AM Stereo

Compare to TDA 4001 the TDA 4010 is an extended AM-receiver. This type is suitable for applications in car radios.

The IF-output V_{IQF} is at pin 15.

Features
- Internal demodulation
- Search tuning stop signal
- Low total harmonic distortion
- Minimal IF leakage at the AF output
- 2-stage ingrated low pass
- Standard IF-output

Function description
The monolithic integrated bipolar receiver has been designed to convert, amplify and demodulate AM - signals. In addition, the component provides a search tuning pulse.

The search tuning stop pulses are processed from the input signal.

The standard AM-IF signal is available at the output of the IR-receiver.

Circuit description
The impedance converter forwards the input signal V_{iRF} to the symmetrical double balanced mixer. Subsequently the signal is converted to IF with the amplitude-controlled oscillator. An external filter forwards the IF signal to the controlled IF amplifier. The amplifier IF signal and the carrier signal will be converted to AF in the subsequent synchronous demodulator. The 2-stage low pass filter forwards the available AF to the AF output.

Via an additional limiter amplifier (LA), the AF uses the carrier signal to control the coincidence demodulator (CD). The output signal of the coincidence demodulator provides the stop pulse during exact tuning and sufficient field strength.

Maximum Ratings

Maximum ratings cannot be exceeded without causing irreversible damage to the integrated ciruit.

Pos.	Maximum rating for $T_{amb} = 25°C$	Symbol	min	max	dim	remarks
1	Operating voltage	V_S		15.6	V	
2	Current consumption	I_S		33.0	mA	
3	Junction temperature	T_j		150	°C	
4	Storage temperature	T_S	− 40	+ 125	°C	
Thermal resistance						
5	chip ambient	R_{thSU}		78	K/W	
6	chip package	R_{thSG}				

Functional Range

Within the functional range, the integrated circuit operates as described; deviations from the characteristic data are possible.

Pos.	Maximum rating for $T_{amb} = 25°C$	Symbol	min	max	dim	remarks
1	Operating voltage	V_{Batt}	7	15	V	
2	Temperature range	$\Delta\delta$	− 25	+ 85	°C	

8

Characteristics

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not stated otherwise, typical characteristics will apply at $t_{amb} = 25°C$ and the listed supply voltage.

Pos.	Parameter	Symbol	Test conditions	Test circuit	Min	Typ	Max	Dim
Supply voltage			$V_S = 12V$					
Ambient temperature			$T_V = 25°C$					
1	Current consumption	I_S				15		mA
2	Reference voltage	V_{STAB}				4.8		V
3	IF-output voltage	V_{qNF}	m = 0.8			800		mV_{eff}
			m = 0.3					
4	Total harmonic		k	m = 0.8				2%
			m = 0.3				1	%
5	IF-output voltage	V_{qNF}	20 • lg (V_{qNF}/30mV: V_{qNF}/1mV				+3	dB
6	Input sensitivity	V_{IHF}	V_{qNF} for V_{IHF} = 1mV – 3dB			30		μV_{eff}
7	Signal-to-noise ratio	$\frac{S+N}{N}$	m = 0.3 $V_{IHF} = 10\mu V_{eff}$			6		dB
8	Signal-to-noise	$\frac{S+N}{N}$	m = 0.3 V_{IHF} = 1mV			46		dB
9	Oscillator voltage	V_{Osc}				100		mV_{SS}
10	Counter output voltage	V_{qZ}					100	mV_{SS}
11	Control range (ΔV_{qIF} = 6dB)	a				60		dB
12	3dB limit frequency of the integrated TP	f_g				5		kHz

Characteristics

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not stated otherwise, typical characteristics will apply at $t_{amb} = 25°C$ and the listed supply voltage.

Pos.	Parameter	Symbol	Test conditions	Test circuit	Min	Typ	Max	Dim
Supply voltage			$V_S = 12V$					
Ambient temperature			$T_V = 25°C$					
13	IR-suppression	A_{IF}				40		dB
14	Conversion gain	V_m				30		dB
15	IF-output Pin 15	V_{qiF}				10		m_{eff}
16	AFC-Offset current without signal	I_{AFC}				± 10		µA
17	AFC-Offset current over control range	ΔI_{AFC}					± 10	µA
18	AFC-current	I_{AFC}	$f_{IHF} = 1MHz \pm 3kHz$				± 80	µA
19	SLS-output voltage	V_{12}	$f_{ZF} = 455kHz$				0.4	V
20	SLS-output voltage	V_{12}	$F_{ZF} = 0V$		11			V
21	SLS-output voltage	V_{12}	$f_{ZF} > 455kHz + 3kHz$		11			C
22	SLS-output voltage	V_{12}	$f_{ZF} > 455kHz - 3kHz$		11			V
23	Input impedance	Z_{IHF}	Pin 3, 4			10/1.5		kΩ//pF
24	Input impedance	Z_{IHF}	Pin 18			3.3/1.5		kΩ//pF

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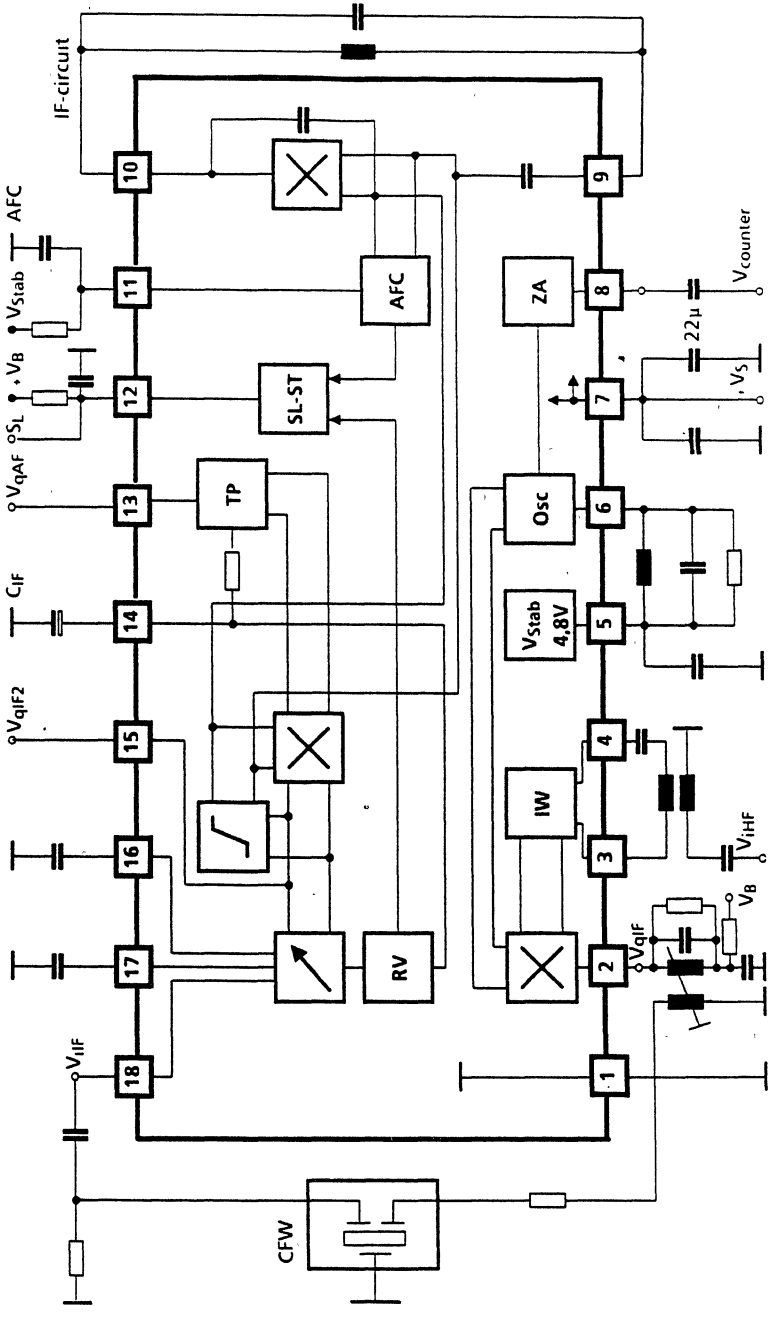
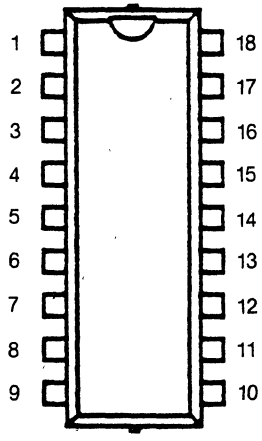
Block diagram

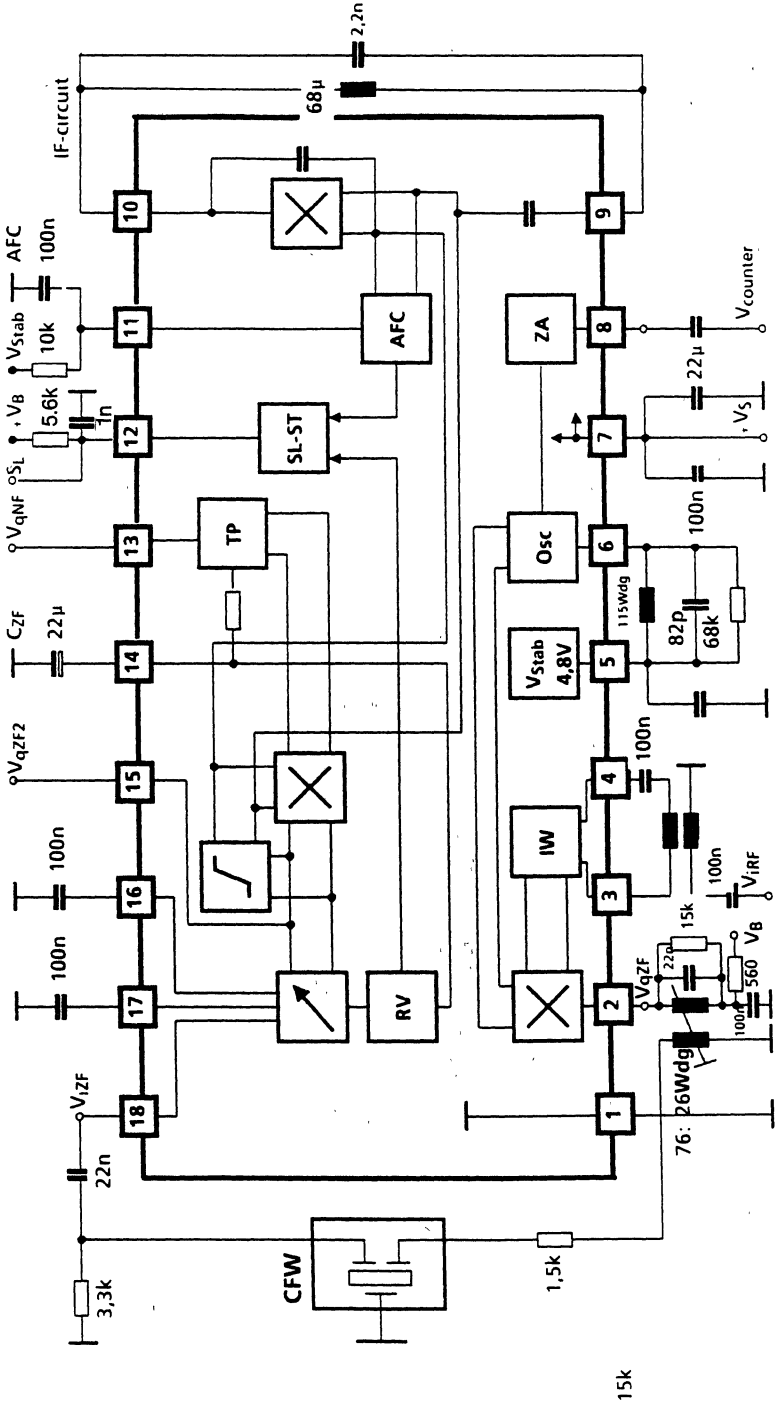


Pin configuration

Pin-Nr.	pin function
1	Ground
2	Mixer output, IF-circuit
3	RF-input
4	RF-input
5	V_{Stap}
6	Oscillator
7	Supply voltage
8	counter output
9	FM-Demodulator circuit IF-circuit
10	FM-Demodulator circuit IF-circuit
11	AFC-output
12	Search tuning stop output
13	AF-output
14	IF-time constant
15	min. IF-output
16	IF-AP follow up device
17	IF-AP follow up device
18	IF-input



measuring circuit



SIEMENS

TDA 4210-3
FM IF IC with Search Tuning Stop Pulse, Field Strength Indicator, Mute Setting and Multipath Detector

The TDA 4210-3 has been designed as FM IF component with a special demodulator for application in car radios. The sensitivity level of the input amplifier can be adjusted for applications with search tuning mode. In addition, a search tuning stop pulse is generated. Moreover, the included multipath identification circuit activates an interference suppression circuit in case of multipath interference. The TDA 4210-3 is especially suitable for application in car radios and home receivers which require a search tuning stop pulse and include an interference suppression circuit.

Features

- Multipath identification circuit
- 7-stage limiter amplifier
- Product demodulator
- AFC output
- Field strength dependent volume control
- Generation of search tuning stop pulse
- Adjustable limiter threshold
- Adjustable muting depth

Circuit description

The integrated circuit includes a 7-stage limiter amplifier with demodulator and non-controlled AF output. The limiter threshold can be raised by approx. 44 dB by means of external circuitry. Within this range the AF output signal can be continuously attenuated by max. 39 dB to eliminate the usually occurring noise products.

To suppress variable interference products, e.g. multipath interference, the TDA 4210-3 includes an identification circuit with an externally adjustable time constant.

Also included are a field strength output, an AFC output, as well as an open collector output. The latter will be activated at the zero crossing of the detector S-curve.

Maximum ratings

Ground	V_1	0	V
MUTE input	V_2	V_S	V
Muting depth	V_3	V_S	V
AF output	V_4	V_S	V
Search tuning stop signal output	I_5	5	mA
AFC output	V_6	V_S	V
Reference voltage output	I_7	5	mA
Phase shift	V_8	V_S	V
Phase shift	V_9	V_S	V
Field strength	I_{10}	5	mA
Identification output	I_{11}	5	mA
Demodulator time constant	V_{12}	V_S	V
Supply voltage	V_S	18	V
Identification input	V_{14}	V_8	V
Limiter threshold	V_{15}	V_8	V
Operating point feedback	$V_{16,17}$	V_8	V
IF input	V_{18}	V_8	V
Junction temperature	T_j	125	°C
Storage temperature range	T_{stg}	−40 to 125	°C

Operating range

Supply voltage	V_S	7.5 to 15	V
IF section demodulator	f_{IF}	0.4 to 15	MHz
Overall frequency	f	0.4 to 15	MHz
AF ($V_{qAF} = 1$ dB)	f_{AF}	0.02 to 150	kHz
Ambient temperature	T_A	−25 to 85	°C

Characteristics

$V_S = 8.5\,V$; $V_{i\,IF\,rms} = 10\,mV$; $f_{i\,IF} = 10.7\,MHz$; $\Delta f = \pm 75\,kHz$; $f_{mod} = 1\,kHz$; $Q_B \approx 20$; $T_A = 25\,°C$; adjustment when $I_7 = 0$; test circuit 1

		Test conditions	min	typ	max	
Current consumption	I_{13}			27	33	mA
Field strength output voltage	V_{10}	$V_{i\,IF\,rms} = 50\,mV$	3.0	3.8		V
	V_{10}	$V_{i\,IF\,rms} = 0\,V$		0	0.1	V
AF output voltage	$V_{q4\,rms}$		270	380	520	mV
Total harmonic distortion during FM IF mode	THD	$I_{AFC} = 0$		0.7	1.5	%
Input voltage for limiter threshold	$V_{i\,IF\,rms}$	V_{q4} −3 dB		15	30	µV
AM suppression	a_{AM}	$m = 30\%$	60			dB
Signal-to-noise ratio	$a_{S/N}$		70			dB
Current deviation of AFC output	ΔI_7	$f = f_{i\,IF} \pm 50\,kHz$		±110		µA
AFC offset	Δf_{off}	$V_i = 20\,\mu V..10\,mV$			±15	kHz
Search tuning stop window	Δf_{ST}	$R_{6-7} = 22\,k\Omega$		±18		kHz
Search tuning stop threshold FM	$V_{i\,ST}$	$V_6 = V_{S/2}$			70	µV
Search tuning stop threshold AM	$V_{i\,ST}$	$V_6 = V_{S/2}$			500	µV
Stabilized voltage	V_7		3.6	4.1	4.6	V
Adjustable range of limiter threshold via pin 15	$V_{i\,IF}$	$V_{15} = 0$; $V_{15} = V_{REF}$		44		dB
AF mute	a_{AF}	$V_2 = 0$; $R_{3-1} = \infty$	3	7	11	dB
	a_{AF}	$V_2 = 0$; $R_{3-1} = 0$	31	39	47	dB
AF mute switch-off voltage	V_2			0.5	0.75	V
MP sensitivity for full drive at pin 1	$V_{i\,14\,rms}$	$f = 20\,kHz$		5		mV
Charge current pin 12	I_{12}	pin 14 to ground		3		mA
Discharge current pin 12	I_{12}	pin 14 open, $V_{12} < 1\,V$		10		µA

Additional data with respect to application

(data does not apply to series measurement)

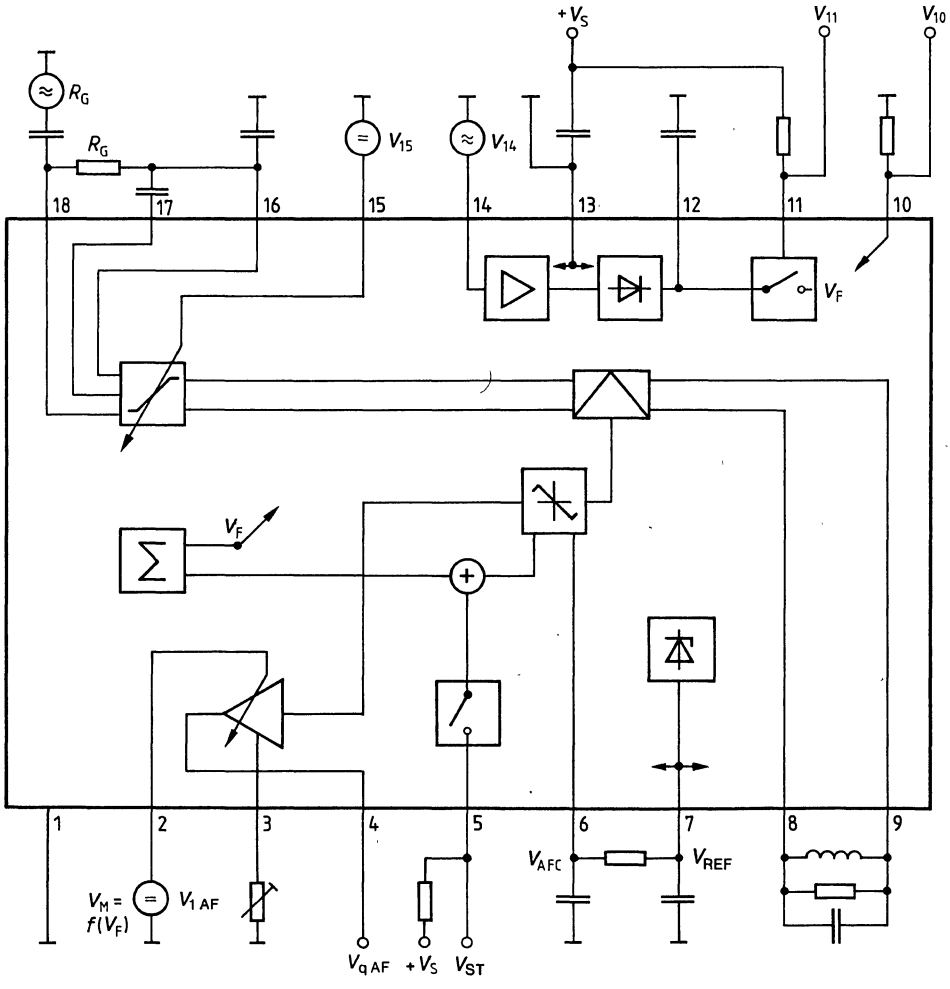
DC voltage AF output	V_{q5}		2.8	3.8	4.8	V
Internal DC current of emitter follower output	I_4		0.75	1		mA
Input resistance for demodulator circuit	R_{9-10}		27	35		kΩ
Search tuning stop "low"	V_6				1.3	V
Search tuning stop "high"	V_6		7			V

8

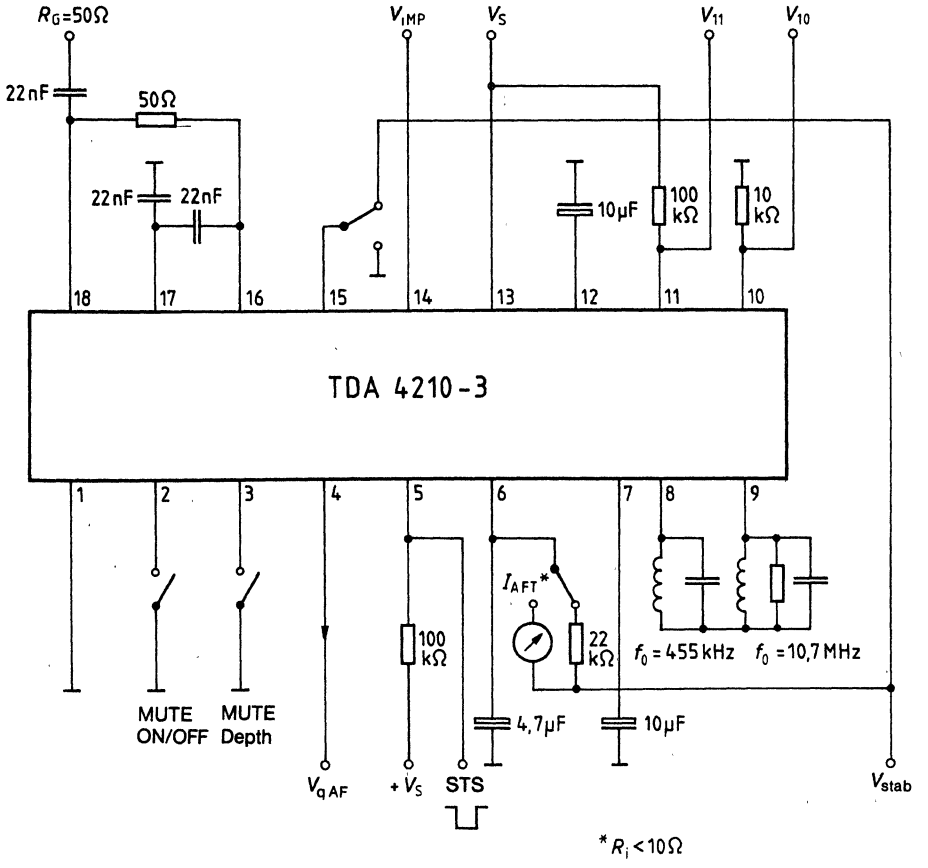
Pin description

Pin	Function
1	Ground: capacitors for operating point feedback, V_S, and V_{REF} decoupling are to be connected directly to pin 1
2	Mute input for (usually derived from field strength output voltage) dc voltage which attenuates the AF output voltage by the set muting depth (pin 4). Max. attenuation when $V_2 = 0$ V, no attenuation when $V_2 \geq 0.75$ V
3	Muting depth adjustment: by connecting a resistor to ground the requested muting depth can be set. Maximal attenuation of AF output voltage with $R = 0$ (approx. 39 dB), minimal attenuation with $R = \infty$ (approx. 7 dB)
4	AF output for demodulated FM-IF
5	Search tuning stop (ST) output is connected when the input field strength exceeds the search tuning stop pulse threshold and the input frequency lies within the search tuning stop pulse window.
6	AFC output: push-pull current output, referenced via a resistor connected to a fixed voltage source (e.g. V_{REF}). The voltage generated at the resistor is in proportion to the deviation from the nominal input frequency and can be applied for retuning purposes.
7	Reference voltage: should be RF decoupled to pin 1. The AFC resistor and the potentiometer for the limiter threshold are referenced to V_{REF}.
8/9	Demodulator tank circuit: driven via two integrated capacitors (approx. 40 pF ±25%). The circuit voltage should be approx. 200 mV (peak-to-peak)
10	Field strength output: supplies a dc voltage proportional to the input level, which quickly adjusts to changes in the input voltage
11	Identification output: designed as an open NPN collector output, which connects an additional time constant in parallel to pin 2 during multipath interference, or activates another circuit to suppress variable interference.
12	Demodulator time constant: determines the response and hold time of the identification circuit.
13	Supply voltage: to be RF decoupled to pin 1
14	Identification input: high impedance input ($R_i \sim 10$ kΩ). This input receives variable interference forwarded on the field strength voltage via a high-pass filter.
15	Input for setting limiter threshold: with a potential between V_{REF} and 0 V, the limiter threshold can be varied by approx. 44 dB.
16/17	Operating point feedback to be RF decoupled. For efficient push-push suppression, pin 16 should be blocked against pin 17 and latter to ground (pin 1).
18	IF input: frequency modulated IF voltage is injected at pin 18.

Block diagram



Measurement circuit



SIEMENS

TDA 4930
Stereo/Bridge AF Amplifier 2 x 10 W/20 W

The TDA 4930 can be applied as a class B stereo amplifier or mono amplifier in bridge configuration for AF signals. In addition, the component is provided with a protective circuitry against overtemperature and overload.

Features

- Universal application as stereo amplifier or mono amplifier in bridge configuration
- Wide supply voltage range
- Minimum of external components
- Outputs AC and DC short-circuit resistant

Maximum ratings

Supply voltage	V_S	32	V
Output peak current	I_1; $I_{9\,pp}$	2.5	A
Input voltage range	V_2; V_3; V_7	−0.3 to V_S	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-case)	$R_{th\,JC}$	6	K/W

Operating range

Supply voltage			
$R_L \geq 8\ \Omega$	V_S	8 to 26	V
$R_L = 4\ \Omega$	V_S	8 to 22	V
Case temperature	T_C	−20 to 85	°C
$P_V = 10$ W			

8

Characteristics

$V_S = 19$ V; $T_A = 25$ °C

		Test circuit	min	typ	max	
Quiescent current ($V_i = 0$)	I_5	1		30	60	mA
Output voltage ($V_i = 0$)	$V_{q\,9;1}$	1	9	9.5	10	V
Input resistance[1]	$R_{i\,7;3}$	1		20		kΩ
Output power ($f = 1$ kHz)						
– stereo operation						
$THD = 1\%$	$P_{q\,9;1}$	1	7	8		W
$THD = 10\%$	$P_{q\,9;1}$	1	9	10		W
– bridge operation						
$THD = 1\%$	$P_{q\,9;1}$	2	14	16		W
$THD = 10\%$	$P_{q\,9;1}$	2	18	20		W
Line hum suppression[2] $f_r = 100$ Hz; $V_r = 0.5$ V	a_{hum}	1	40	46		dB
Current consumption $P_9 = P_1 = 10$ W; $f_i = 1$ kHz	I_5	1		1.5		A
Efficiency $P_9 = P_1 = 10$ W; $f_i = 1$ kHz	η	1		70		%
Total harmonic distortion $P_{9/1} = 0.05$ to 6 W $f_i = 40$ Hz to 15 kHz	THD	1		0.2	0.5	%
Cross-talk rejection $f_i = 1$ kHz; P_9 or $P_1 = 10$ W	a_{cr}	1		50		dB
Transmission range[3]	B	1	40 Hz to 60 kHz			
Disturbance voltage ($B = 30$ Hz to 20 kHz) in acc. with DIN 45405 referred to input[4]	V_d	1		5		μV
Noise voltage (CCIR filter) in accordance with DIN 45405 referred to the input[4]	V_n	1		15		μV_S
Difference in transmission measure $P_9 = P_1 = 7$ W $f_i = 40$ Hz to 20 kHz	ΔG_V	1			1	dB
Voltage gain stereo	G_V	1		30		dB
Voltage gain bridge configuration	G_V	2		36		dB
DC output voltage at active DC protection if S1/9 is closed; $V_S \geq 10$ V	$V_{q\,9;1}$	2		0.15	0.30	V

1) S2a(b) open/closed
2) S1a(b) and S3 in position 2
3) $P_{9/1} = 6$ W; −3 dB referred to 1 kHz
4) S1a(b) in position 2

Circuit description

The IC contains 2 complete amplifiers and can be used for a wide variety of applications with a minimum of external circuitry.

The TDA 4930 can be applied as stereo amplifier or amplifier in bridge configuration for operating voltages ranging between 8 V and 26 V, with speakerload impedance from 1 to 16 Ω.

The prestages are differential amplifiers with strong negative feedback. Internal frequency compensation in the driver amplifier limits the gain-bandwidth product to 4.5 MHz.

The power output stages are comprised of quasi PNP transistors (small saturation voltage).

Each power element is equipped with an independent protective circuit, rendering the outputs of the amplifiers AC and DC short-circuit resistant.

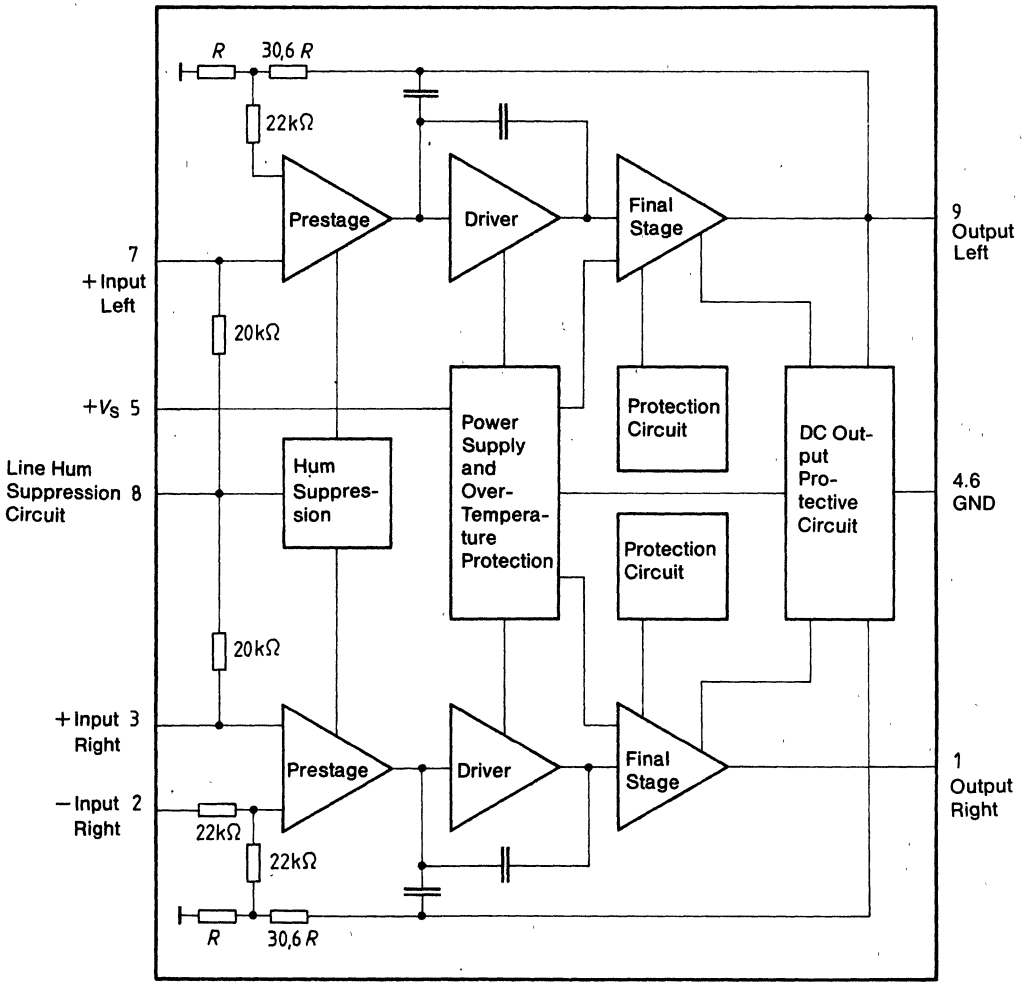
A DC protective circuit of the outputs prevents overloading of the loudspeakers, if ground connections become apparent during bridge operations. To avoid overheating, a temperature fuse affecting both amplifiers prevents current supply to the power output stages during inadmissibly high chip temperatures.

As a special economic feature, the negative feedback resistances for $G_V = 30$ dB and the input voltage reference divider have been integrated.

Pin description

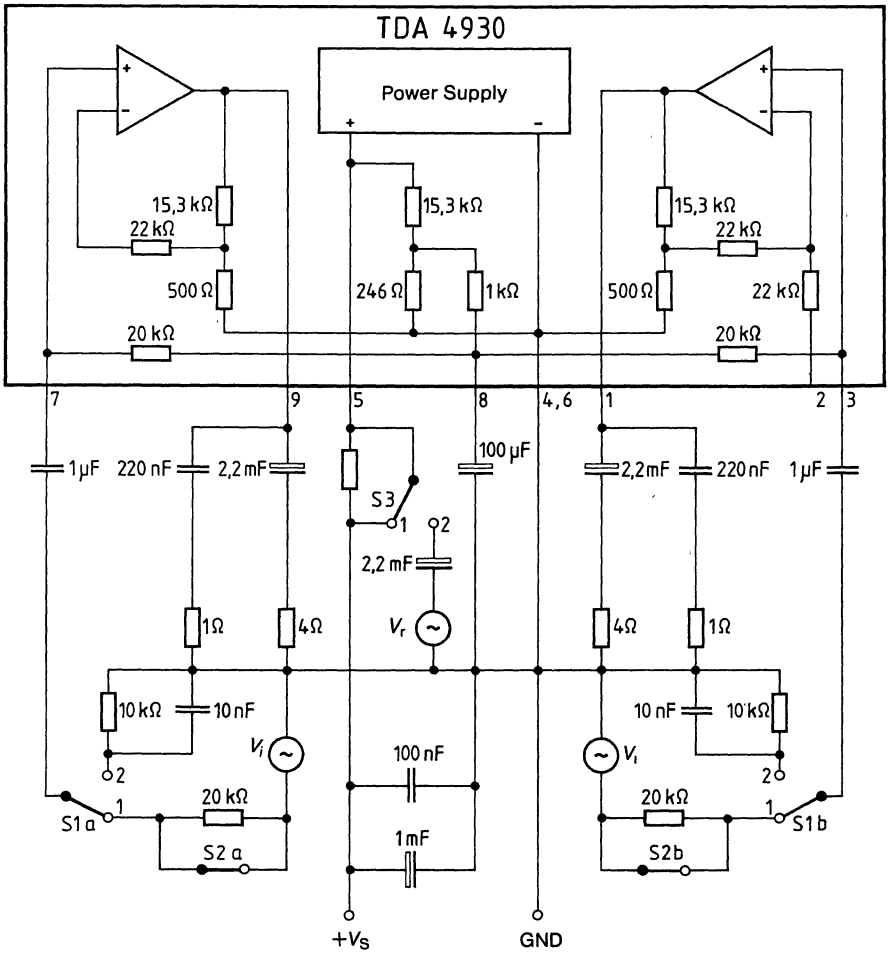
Pin	Function
1	Output right channel
2	Inverting input right channel (more than 22 kΩ)
3	Non-inverting input right channel
4	GND
5	$+V_S$
6	GND
7	Non-inverting input left channel
8	Line hum suppression right and left channel
9	Output left channel

Block diagram



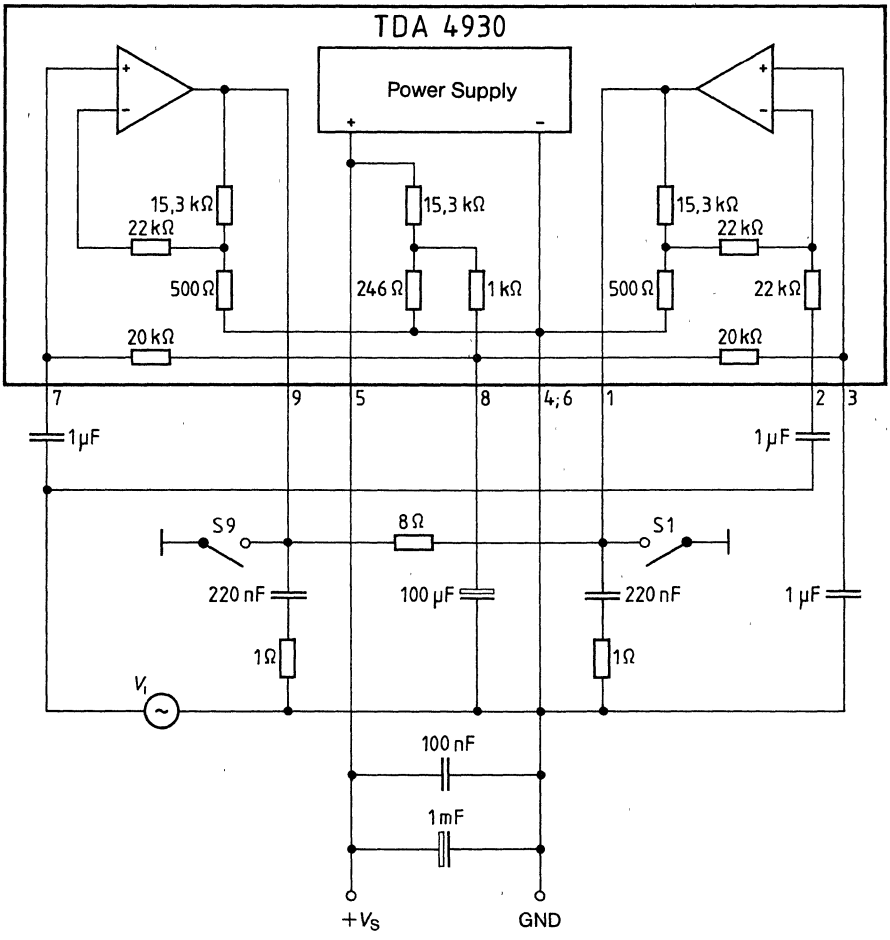
Test and measurement circuit

1. Stereo operation



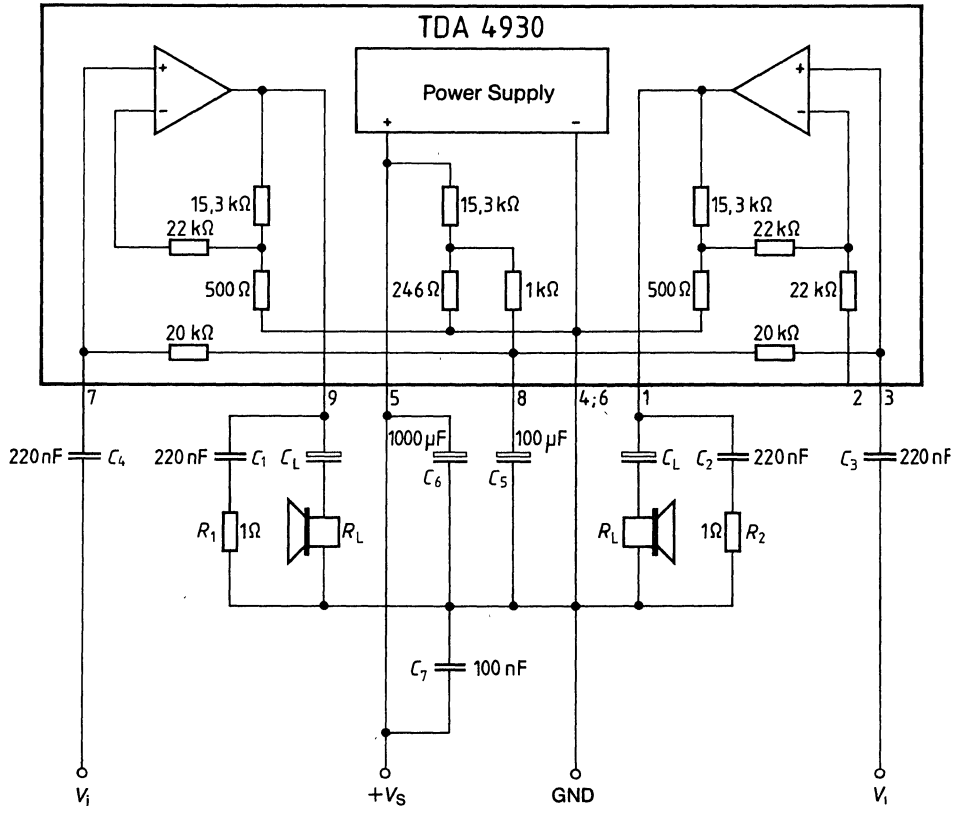
Test and measurement circuit

2. Bridge operation



Application circuit

1. Stereo operation



V_S	19 V	26 V
R_L	4Ω	8Ω
C_L	1000µF	470µF

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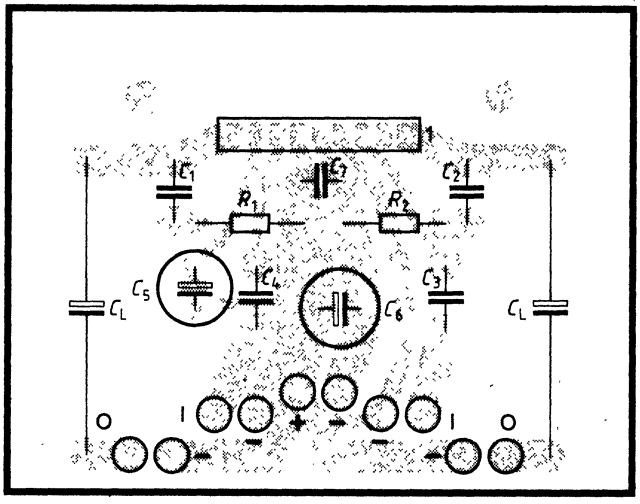
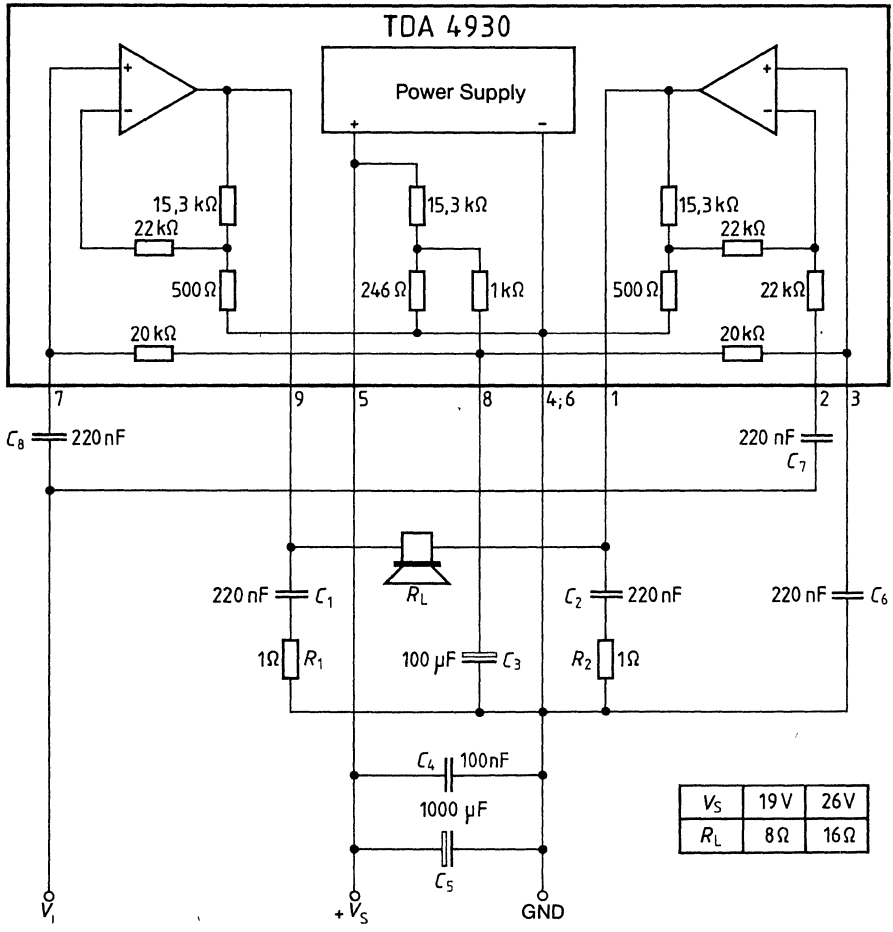
Layout/Plug-in location plan



Application circuit

2. Bridge operation (only one channel)



V_S	19 V	26 V
R_L	8 Ω	16 Ω

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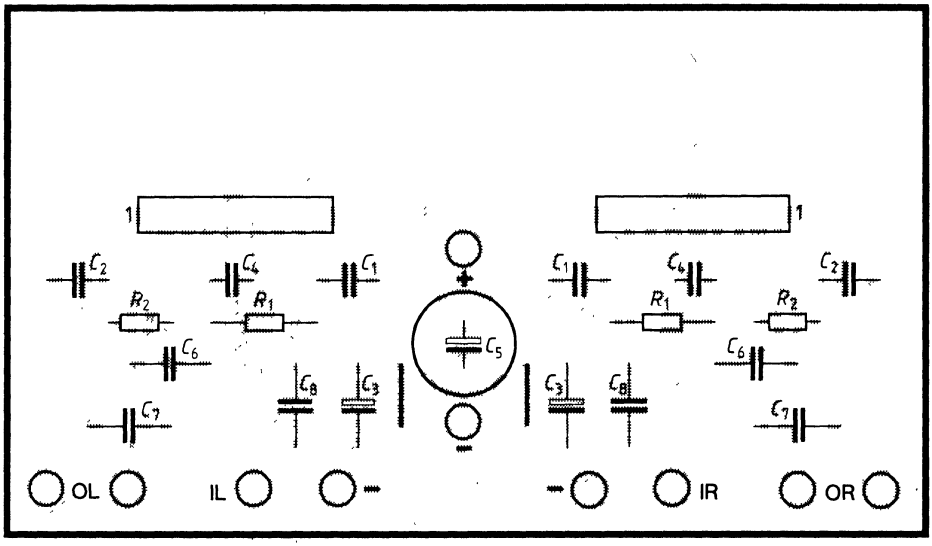
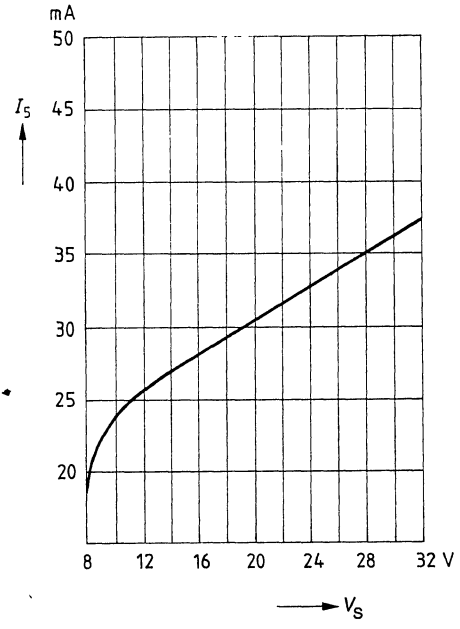
Layout/Plug-in location plan

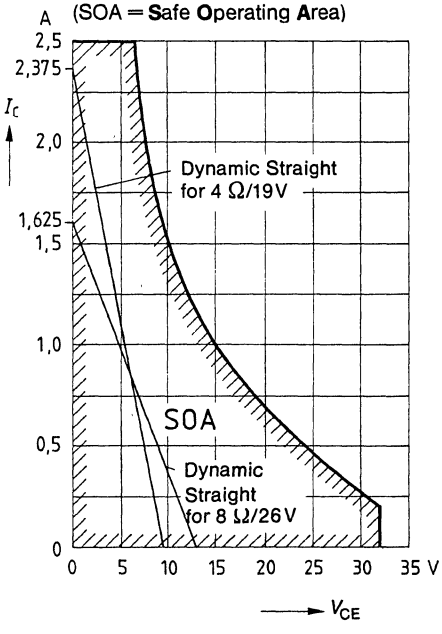


Quiescent current versus supply voltage



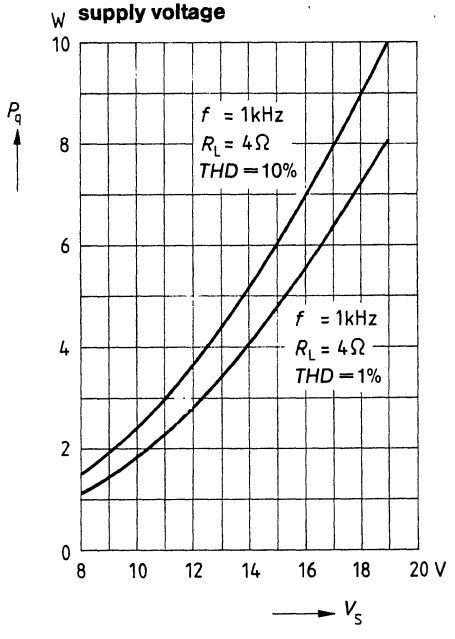
Typical operating range of the final transistors adjusted by internal protective circuits

(SOA = **S**afe **O**perating **A**rea)



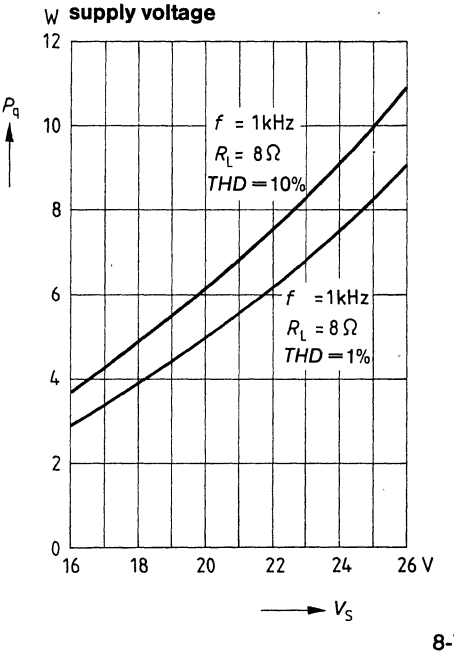
Stereo operation

Output power versus supply voltage



Stereo operation

Output power versus supply voltage



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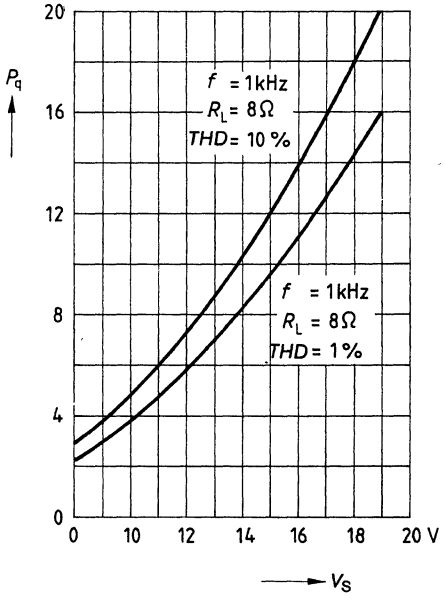
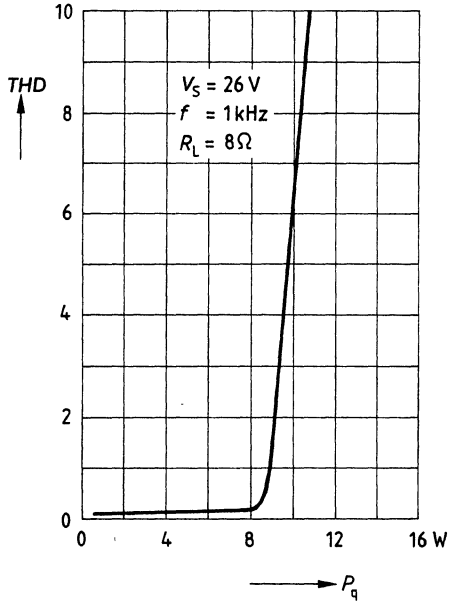
Bridge operation

Output power versus supply voltage



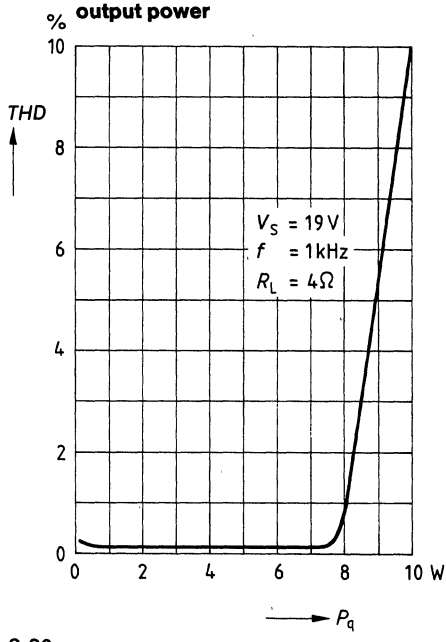
Stereo operation

Total harmonic distortion versus output power



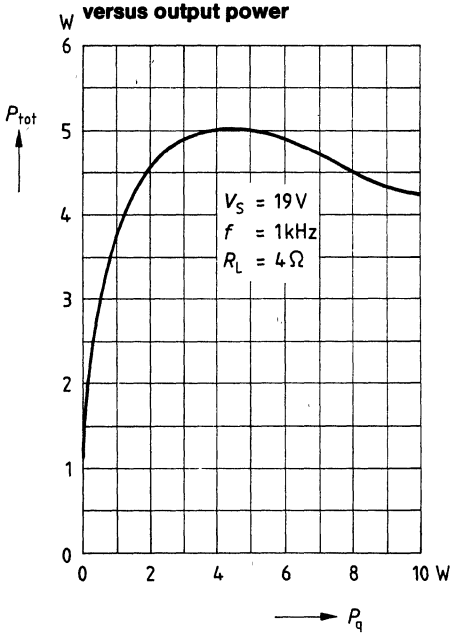
Stereo operation

Total harmonic distortion versus output power



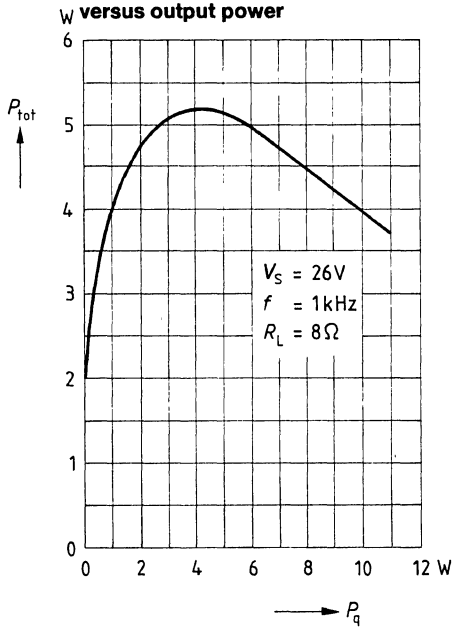
Stereo operation

Power dissipation (each channel) versus output power



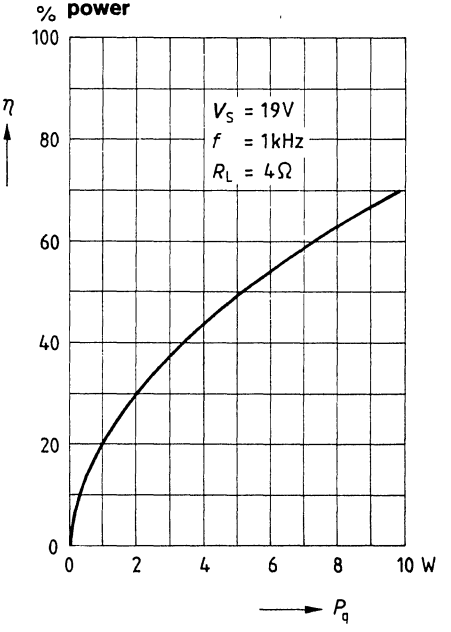
Stereo operation

Power dissipation (each channel) versus output power



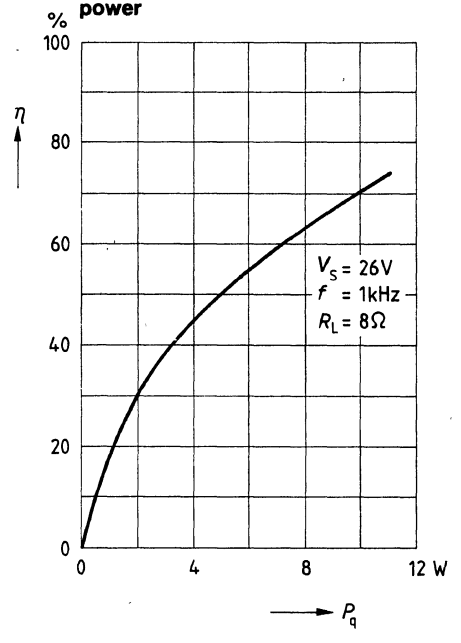
Stereo operation

Efficiency versus output power



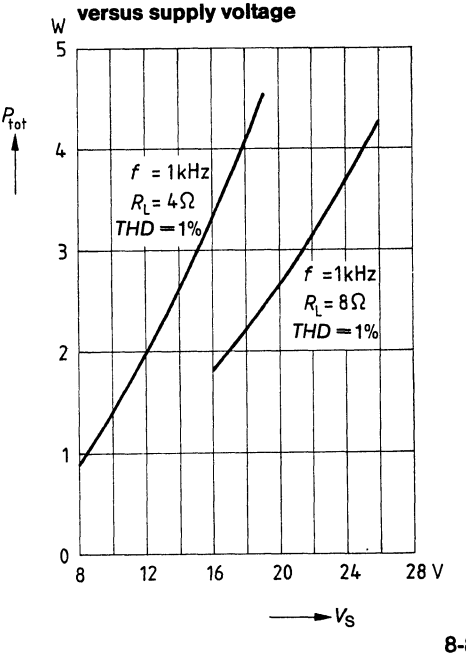
Stereo operation

Efficiency versus output power



Stereo operation

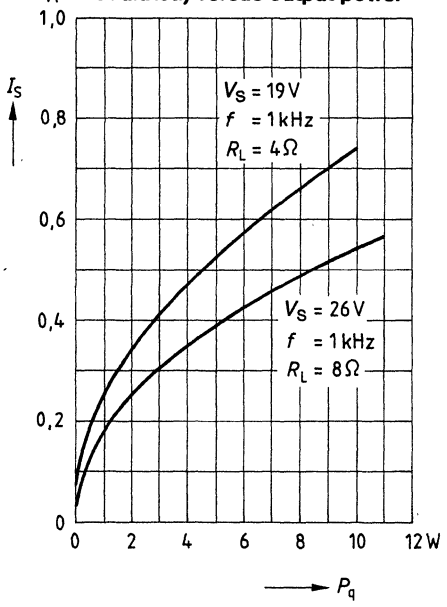
Power dissipation (each channel) versus supply voltage



8

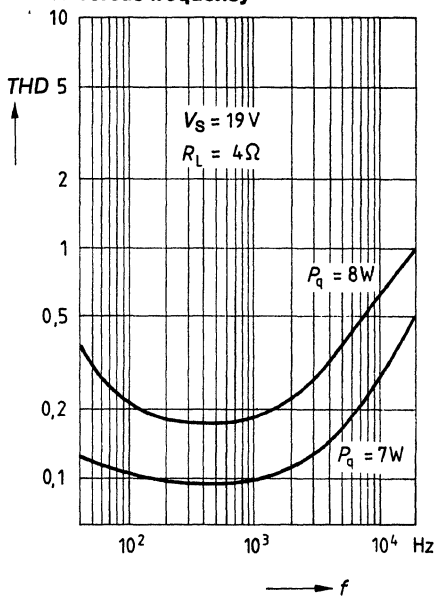
Stereo operation

Supply current (one channel modulated) versus output power

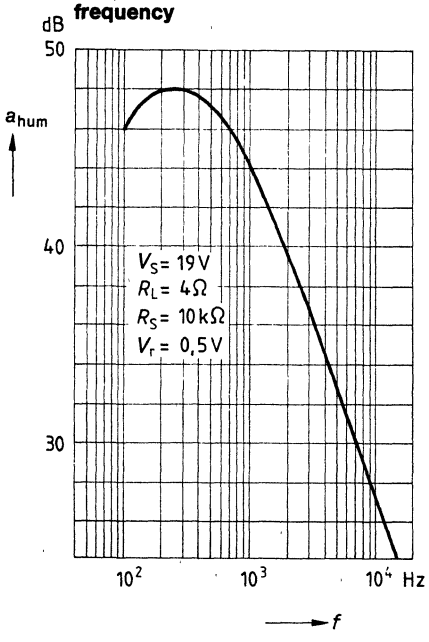


Stereo operation

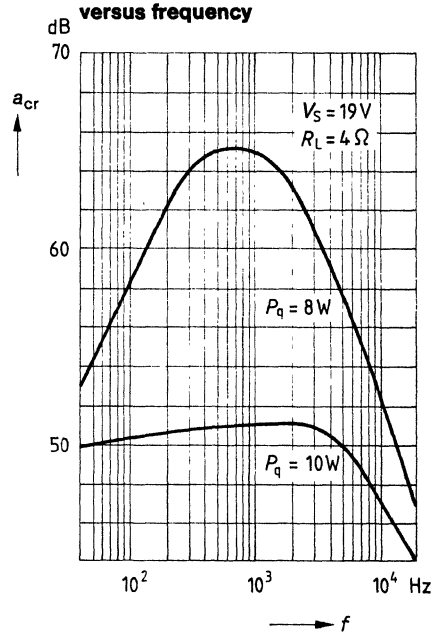
Total harmonic distortion versus frequency



Line hum suppression versus frequency



Cross-talk rejection versus frequency



SIEMENS

TDA 4935
Stereo/Bridge AF Amplifier 2 x 15 W/30 W

The TDA 4935 can be applied as a class B stereo amplifier or mono amplifier in bridge configuration for AF signals. In addition, the component is provided with a protective circuitry against overtemperature and overload.

Features

- Universal application as stereo amplifier or mono amplifier in bridge configuration
- Wide supply voltage range
- Minimum of external components

Maximum ratings

Supply voltage	V_S	32	V
Output peak current	I_1; I_9	2.8	A
Input voltage range	V_2; V_3; V_7	−0.3 to V_S	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-case)	$R_{th\,JC}$	4	K/W

Operating range

Supply voltage	V_S		
$R_L \geq 8\ \Omega$	V_S	8 to 30	V
$R_L = 4\ \Omega$	V_S	8 to 24	V
Case temperature	T_C	−20 to 85	°C
$P_V = 15$ W			

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Characteristics

$V_S = 24$ V; $T_C = 25$ °C

		Test circuit	min	typ	max	
Quiescent current $V_i = 0$	I_5	1		40	80	mA
Output voltage $V_i = 0$	$V_{q1;9}$	1	11	12	13	V
Input resistance[1]	$R_{i3;7}$	1		20		kΩ
Output power $f = 1$ kHz						
— stereo operation						
$THD = 1\%$	$P_{q1;9}$	1	10	12		W
$THD = 10\%$	$P_{q1;9}$	1	13	15		W
— bridge operation						
$THD = 1\%$	$P_{q1;9}$	2	20	24		W
$THD = 10\%$	$P_{q1;9}$	2	26	30		W
Line hum suppression[2] $f_R = 100$ Hz; $V_R = 0.5$ V	a_{hum}	1	40	46		dB
Current consumption $P_9 = P_1 = 15$ W; $f_i = 1$ kHz	I_5	1		1.8		A
Efficiency $P_9 = P_1 = 10$ W; $f_i = 1$ kHz	η	1		70		%
Total harmonic distortion $P_{9/1} = 0.05 - 10$ W $f_i = 40$ Hz to 15 kHz	THD	1		0.2	0.5	%
Cross-talk rejection $f_i = 1$ kHz; P_9 or $P_1 = 15$ W	a_{cr}	1		50		dB
Transmission range[3]	B	1		40 Hz to 60 kHz		
Disturbance voltage (B = 30 Hz to 20 kHz) in acc. with DIN 45405 referred to input[4]	V_d	1		5		μV
Noise voltage (CCIR filter) in acc. with DIN 45405 referred to the input[4]	V_n	1		15		μV_S
Difference in transmission measure $P_9 = P_1 = 10$ W $f_i = 40$ Hz to 20 kHz	ΔG_V	1			1	dB
Voltage gain						
stereo	G_V	1		30		dB
bridge configuration	G_V	2		36		dB

1) S2a (b) open/closed
2) S1a (b) and S3 in position 2
3) $P_{9/1} = 6$ W; −3 dB referred to 1 kHz
4) S1a (b) in position 2

Circuit description

The IC contains 2 complete amplifiers and can be used for a wide variety of applications with a minimum of external circuitry.

The TDA 4935 can be applied as stereo amplifier or amplifier in bridge configuration for operating voltages ranging between 8 V and 26 V.

The prestages are differential amplifiers with strong negative feedback. Internal frequency compensation in the driver amplifier limits the gain-bandwidth product to 4.5 MHz.

The power output stages are comprised of quasi PNP transistors (small saturation voltage).

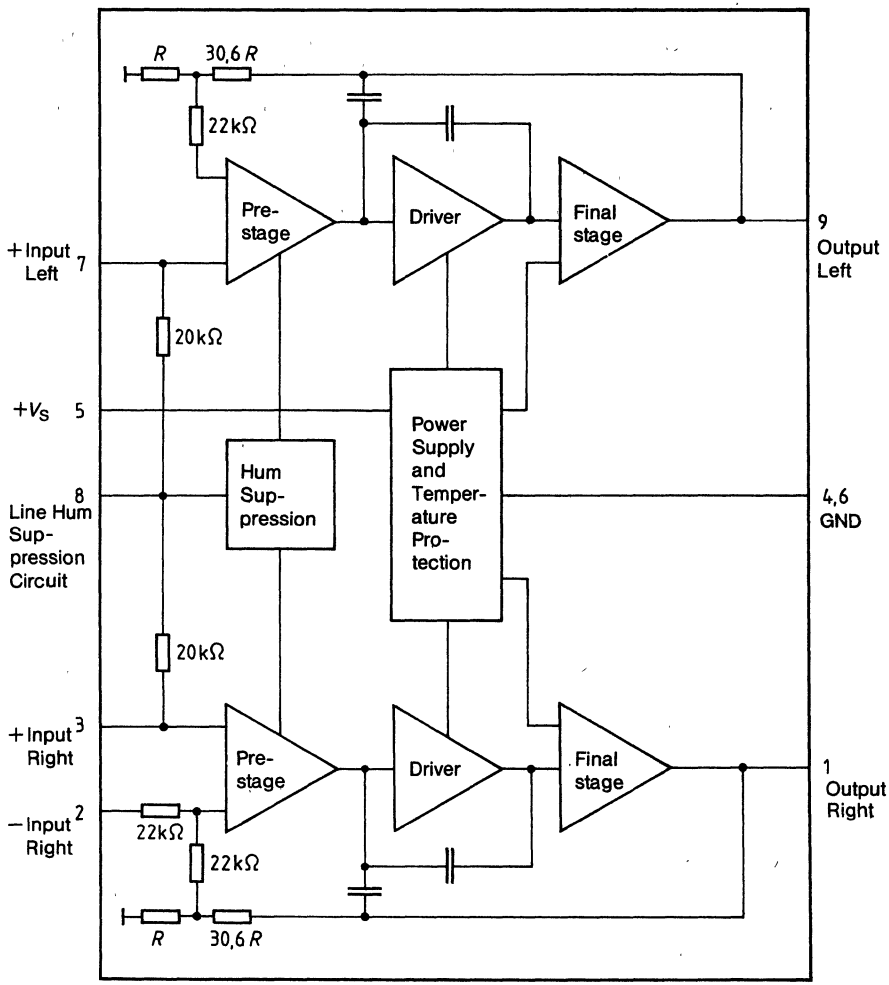
To avoid overheating, a temperature fuse affecting both amplifiers prevents current supply to the power output stages during inadmissibly high chip temperatures.

As a special economic feature, the negative feedback resistances for $G_V = 30$ dB and the input voltage reference divider have been integrated.

Pin description

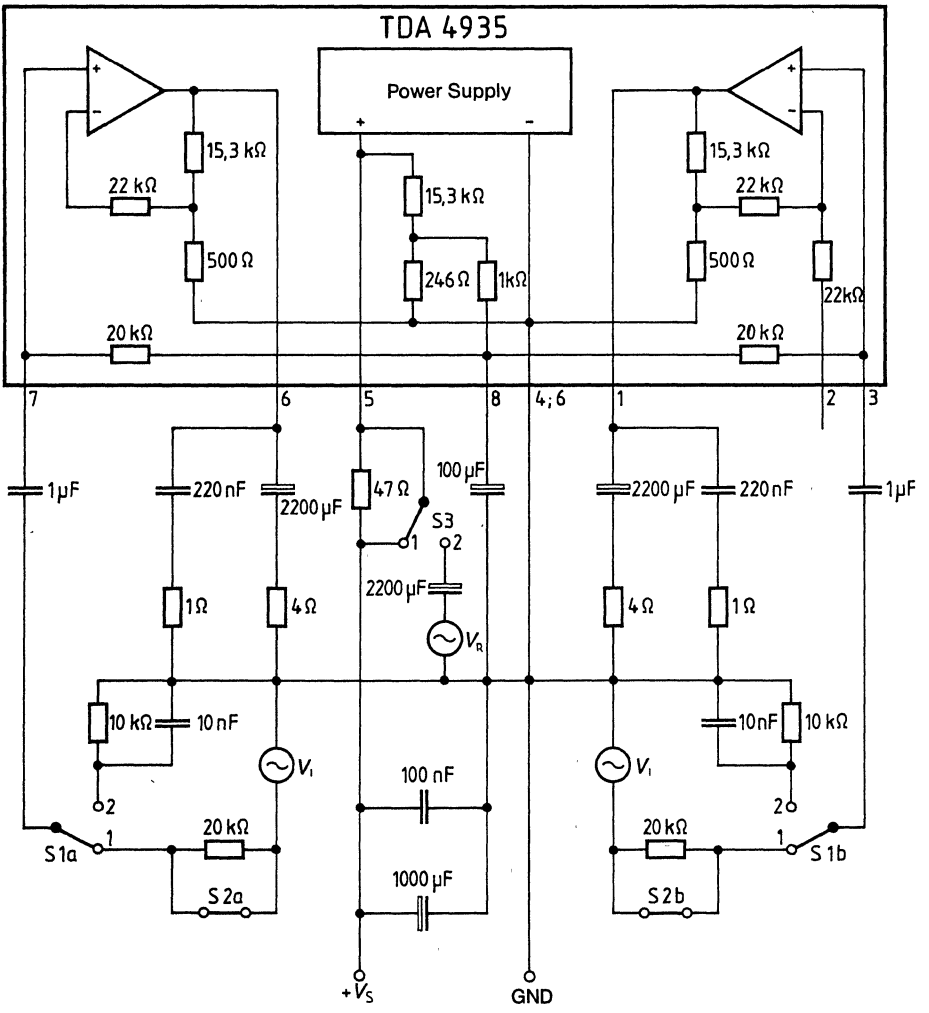
Pin	Function
1	Output right channel
2	Inverting input right channel (more than 22 kΩ)
3	Non-inverting input right channel
4	GND
5	$+V_S$
6	GND
7	Non-inverting input left channel
8	Line hum suppression right and left channel
9	Output left channel

Block diagram



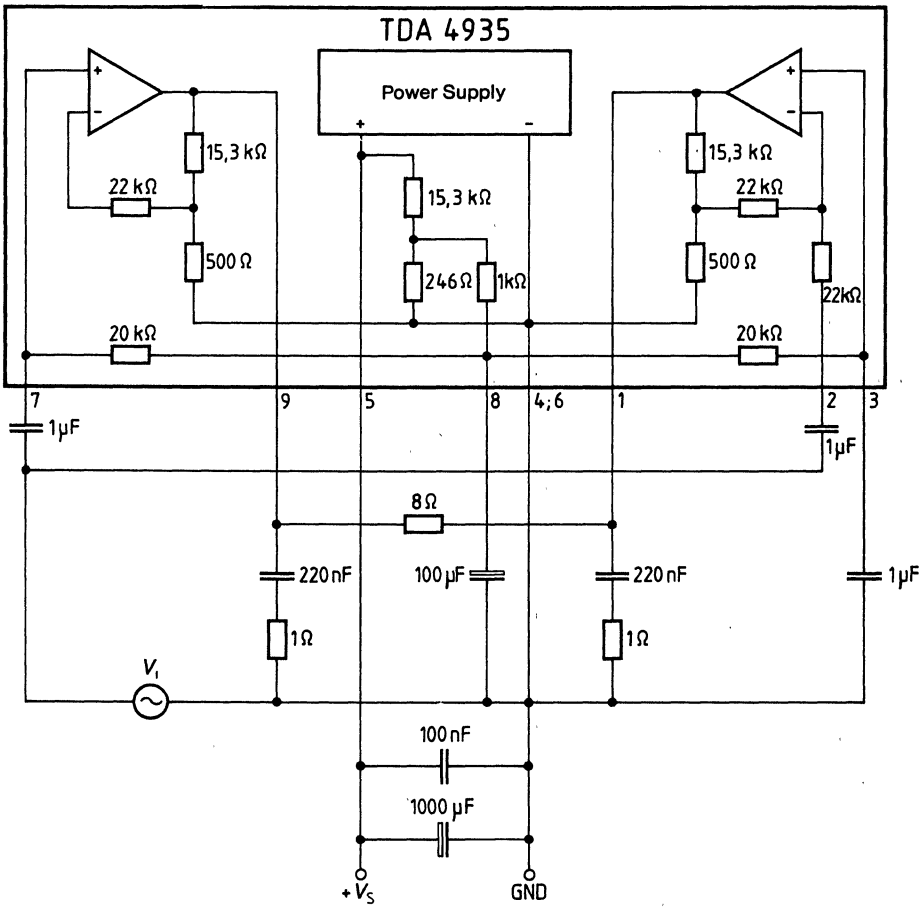
Test and measurement circuit

1. Stereo operation



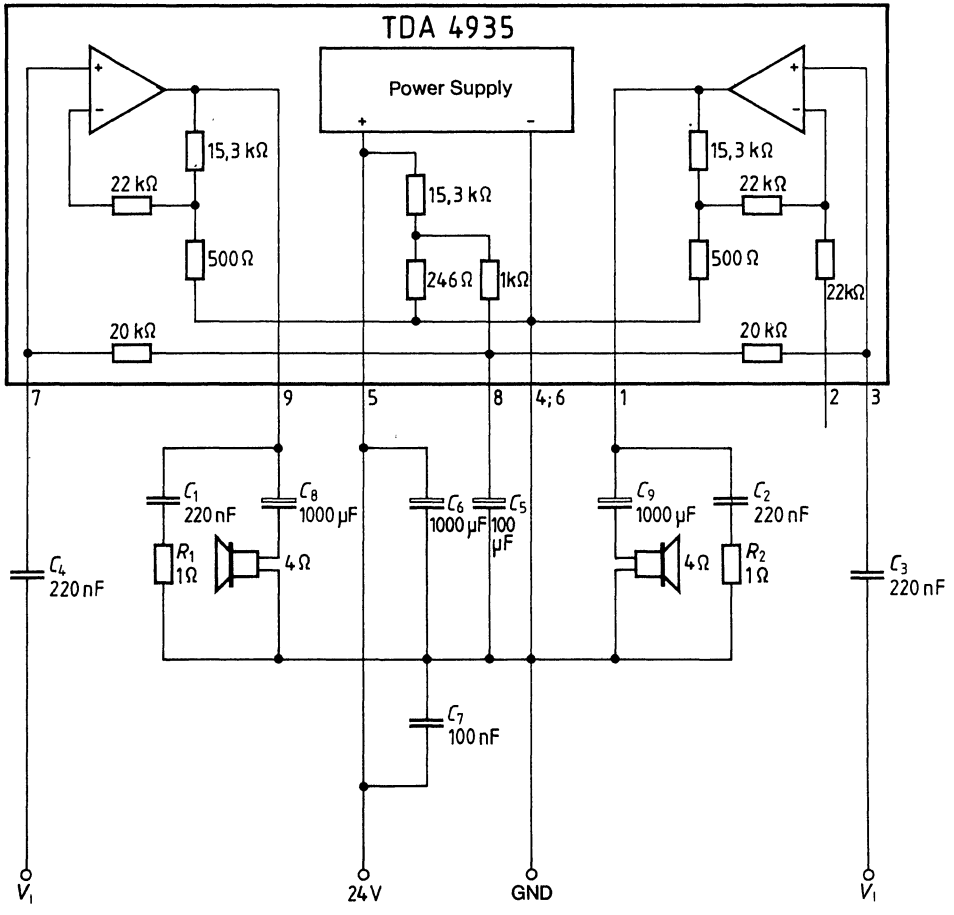
Test and measurement circuit

2. Bridge operation

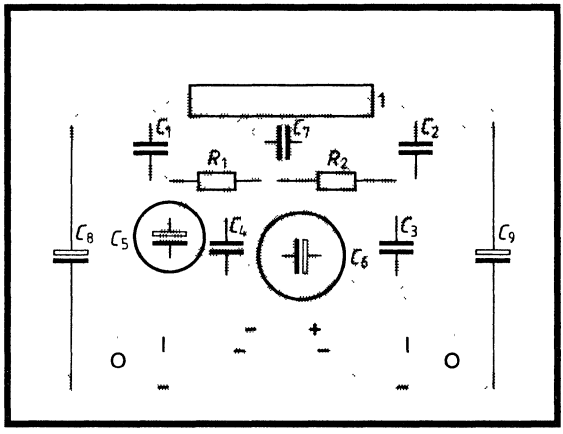


Application circuit

1. Stereo operation

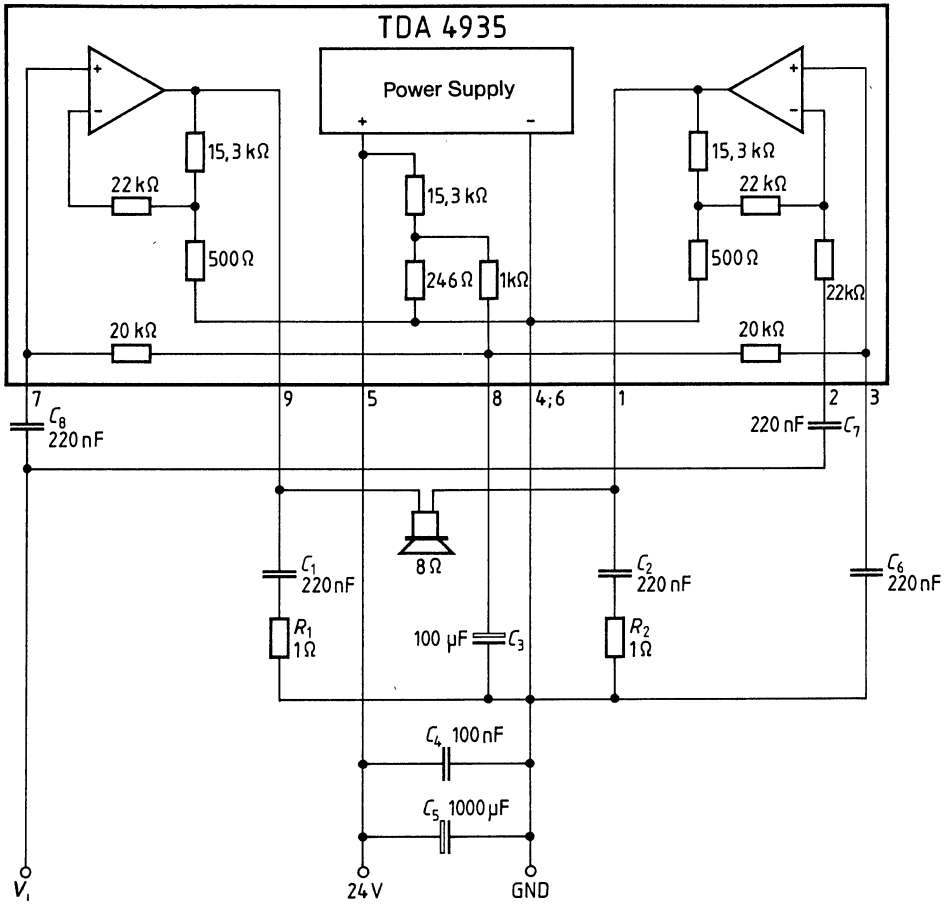


Layout/Plug-in location plan

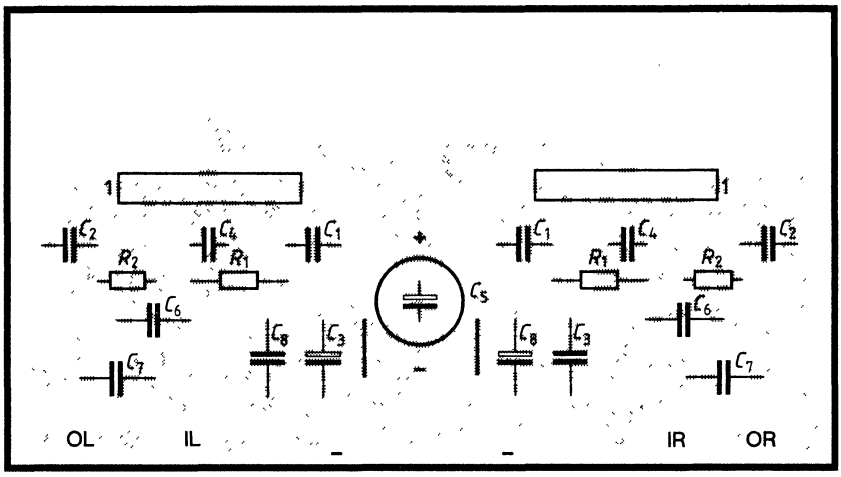


Application circuit

2. Bridge operation (only one channel)

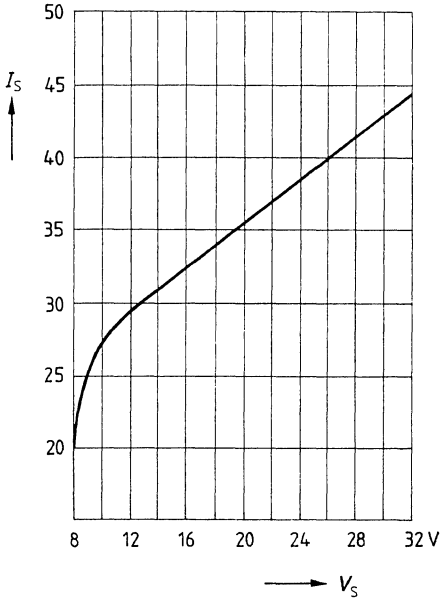


Layout/Plug-in location plan



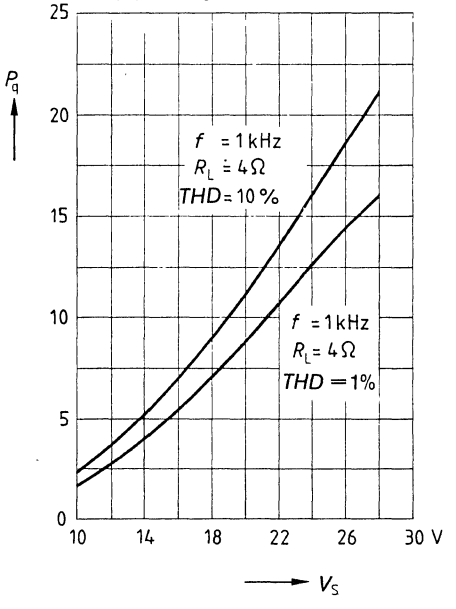
2 x 30W

Quiescent current versus supply voltage



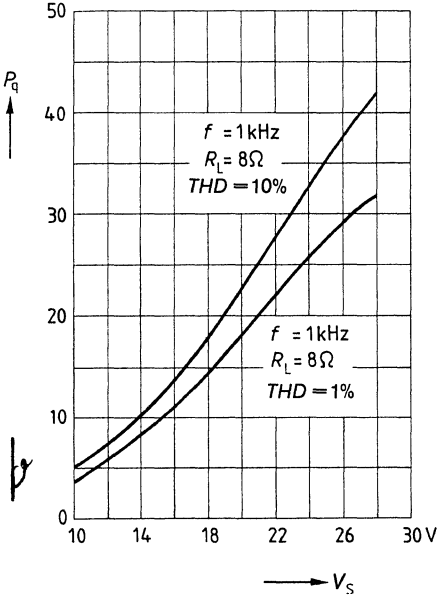
Stereo operation

Output power versus supply voltage



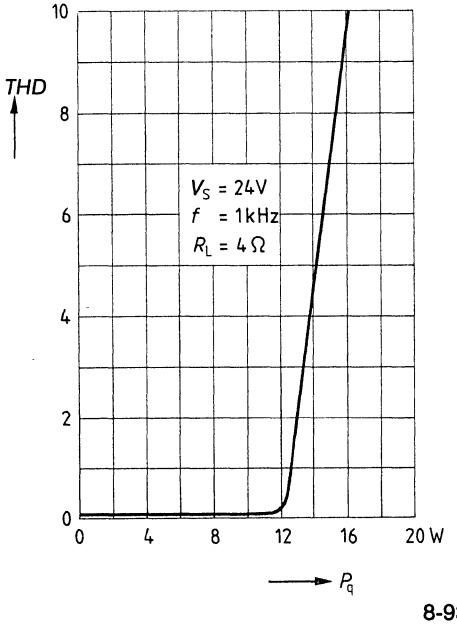
Bridge operation

Output power versus supply voltage



Stereo operation

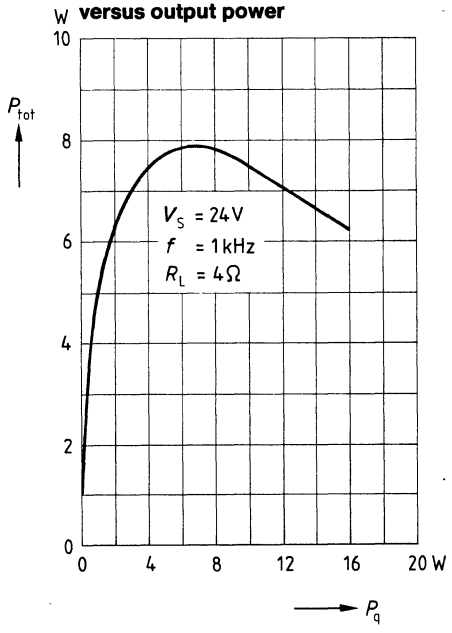
Total harmonic distortion % versus output power



8

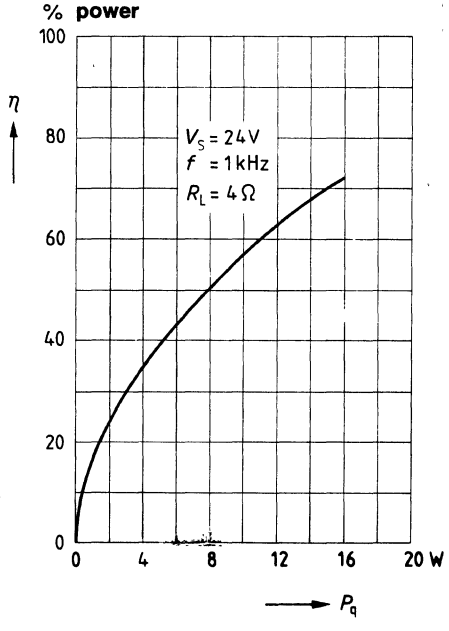
Stereo operation

Power dissipation (each channel) versus output power



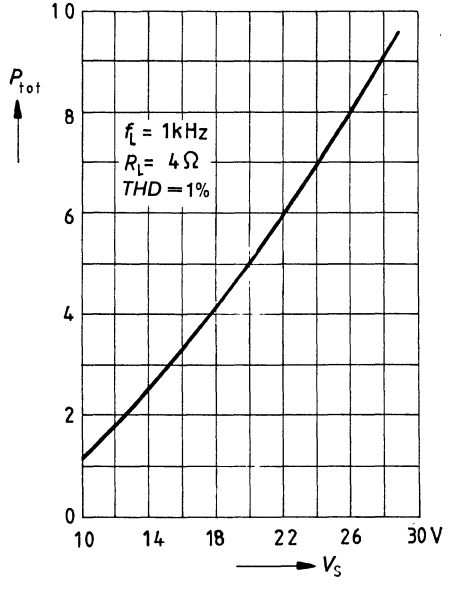
Stereo operation

Efficiency versus output power



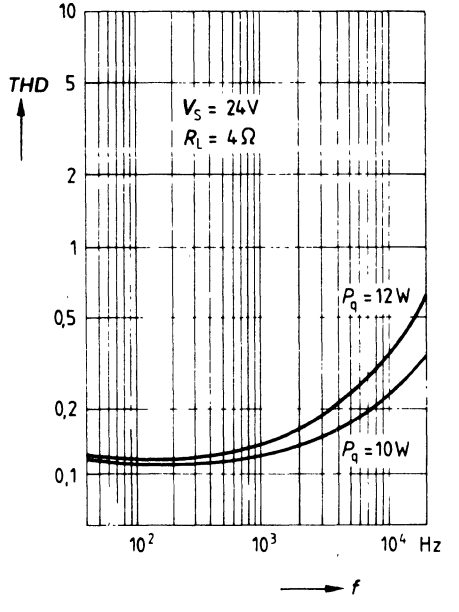
Stereo operation

Power dissipation (each channel) versus supply voltage



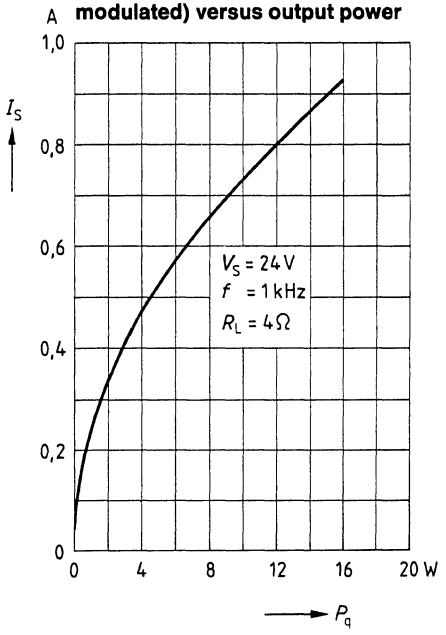
Stereo operation

Total harmonic distortion versus frequency



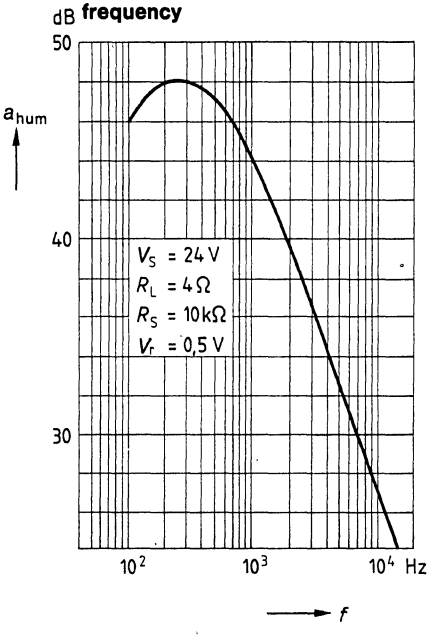
Stereo operation

Supply current (one channel) modulated) versus output power

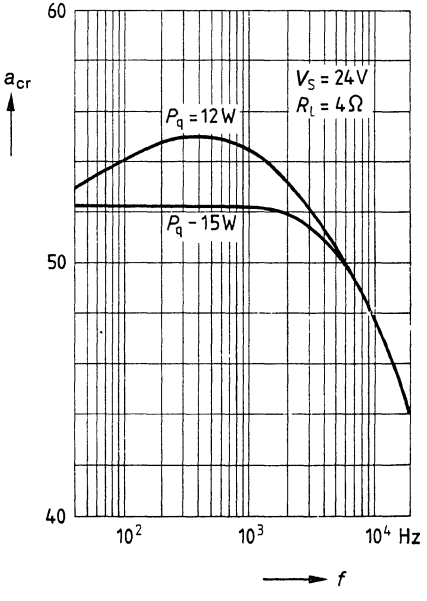


Stereo operation

Line hum suppression versus frequency



Cross-talk rejection versus frequency



8

SIEMENS

TUA 1574
FM Tuner IC

The TUA 1574 has been designed as monolithic integrated tuner with strictly symmetrical RF parts for use in car radios and home receivers. In addition the IC provides a pre-stage control by means of narrow and wideband information and IF post amplification.

Features
- double-balanced mixer
- AGC generation
- strictly symmetrical RF parts
- Stand-by switch
- decoupled counter output

Description of function and applications

Description of functions:
The TUA 1574 has been designed as a monolithic integrated tuner with strictly symmetrical RF parts for use in car radios and home receivers. In addition the IC rovides a pre-stage control by means of narrow and wideband information and an IF post amplificication.

- double-balanced mixer
- AGC generation
- strictly symmetrical RF parts
- stand-by switch
- decoupled counter output

Description of applications:
The TUA 1574 is especially suitable for use in car radios and home receivers with pre-stage control and distributed IF selection.

Description of circuitry:
The integrated circuit includes an oscillator with symmetrical input, buffered output and a double balanced mixer for frequency conversion. The resulting IF is post-amplified in a linear IF driver. The AGC stage integrated for pre-stage control generates combined wide and narrowband information. The IC also includes a reference voltage source and a stand-by switch.

Maximum Ratings
Exceeded maximum ratings cause irreversible damage to the IC.

Pos.	Maximum rating for ambient temperature $T_{amb} = +25°C$	Symbol	min	max	unit
1	Supply voltage	V_{15}	− 0.3	+ 13.5	V
2	Mixer	V_{16}, V_{17}		+ 25	V
3	Stand-by switch	V_{11}	− 0.3	+ 13.5	V
4	Reference voltage	V_5	− 0.3	+ 7	V
5	Currents: all pins are short-circuit protected against ground.				

Functional Range

Within the functional range, the IC operates as described; deviations from the characteristic data are possible.

Pos.	functional range	Symbol	min	max	unit
1	Supply voltage	V_{15}	7	12	V
2	Ambient temperature	T_{amb}	−25	85	°C

Characteristics

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not stated otherwise, typical characteristics will apply at t_{amb} = 25°C and V_S 8.5V.

Pos.	Parameter	Symbol	Measurement circuit	Min	Typ	Max	Unit
1	Current Consumption (without mixer)	I_{15}		14	23	28	mA
2	Reference voltage				4.2		V
Mixer							
3	Third order	I_{P3}			115		dB/µV
4	Noise figure	F			11		dB
5	Mixer gain	V			14		dB
Oscillator							
6	DC characteristics	V_7, V_8			1.3		V
7	DC characteristics	U_6			2		V
8	Interference	Δf			2.2		Hz
9	Output signal 75Ω			25		MV_{eff}	
10	Output signal open	V_9			110	mV_{eff}	
11	Output impedance	R_9			2.9		kΩ
Control voltage generation							
12	Control voltage for prestage	V_{18}	0.5		(VP - 0.3)	0.3	V
13	Output current (V_3 = 0 or V_{12} = 550V and V_{18} = $V_{P/2}$)	$-I_{18}$			50		µA
14	Output current (V_3 = 2V and V_{12} = 1V)	I_{18}			2...5	mA	
15	Narrowband-control threshold when V_3 = 2V)	V_{12}			500		mV

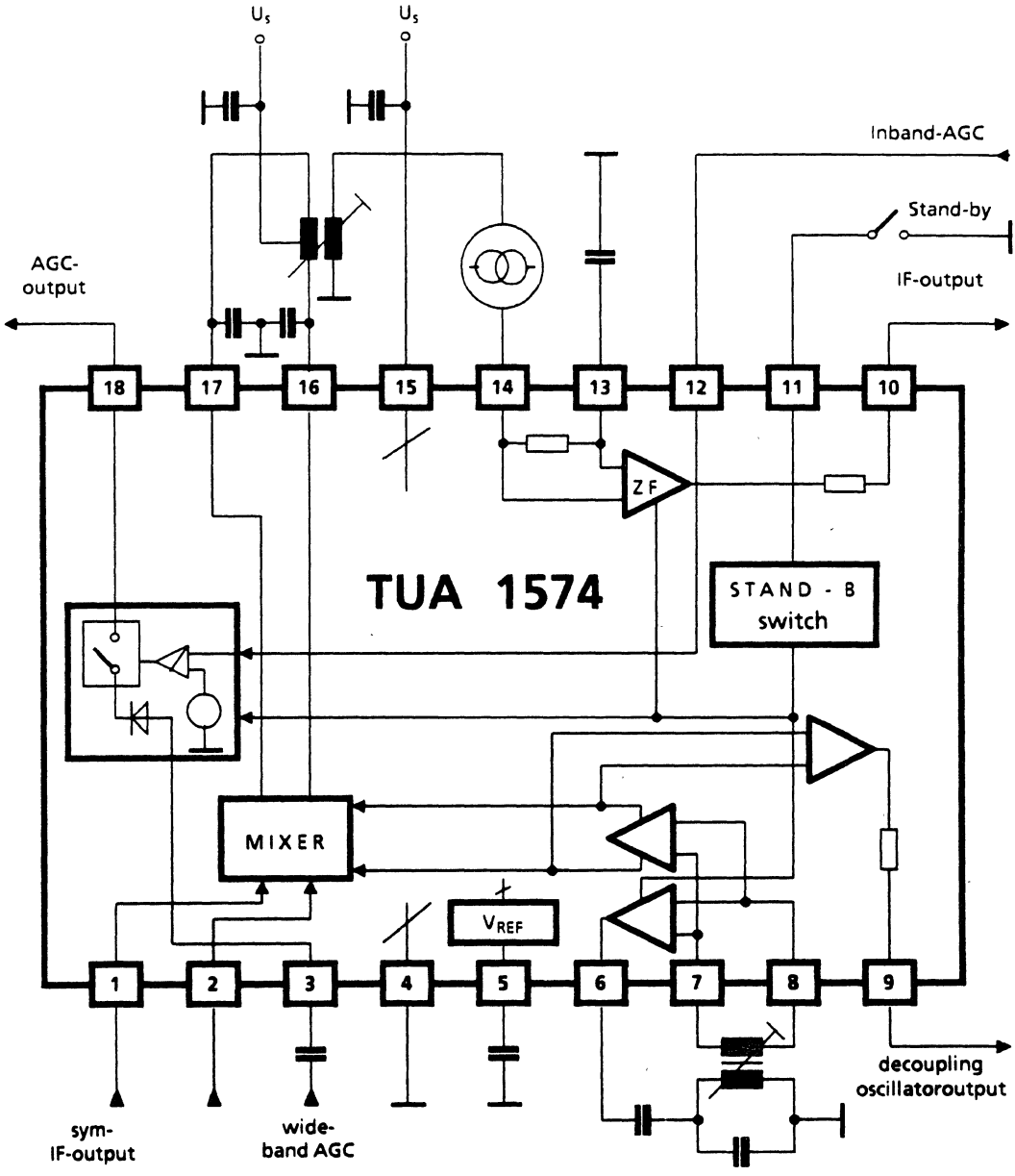
8

Characteristics

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not stated otherwise, typical characteristics will apply at $t_{amb} = 25°C$ and V_S≙8.5V.

Pos.	Parameter	Symbol	Measurement circuit	Min	Typ	Max	Unit
16	Wideband control threshold when $V_{12} = 0.7V$		$V_{IHF\ EMK2}$		19		mV
Linear IF amplifier							
17	Input DC voltage	$V_{13,14}$			1.2		V
18	Output DC voltage	V_{10}			3.5		V
19	Input resistance	$R_{I\ 13}$			300		Ω
20	Input capacitance	$C_{I\ 13}$			13		pF
21	Output impedance	R_{10}			300		Ω
22	Output capacitance	C_{10}			3		pF
23	Voltage gain	G_V			30		dB
24	Noise figure at $R_S = 300Ω$	F			6.5		dB
25	Reference voltage	V_5			4.2		V
26	Stand-by	V_{11}			3.3...VS		V

Block diagram



Pin functions

Pin 1/2: *RF input for mixer:*
low impedance (basic circuitry) input directly to the mixer pair.

Pin 3: *Input for wideband information:*
RF signal is present after pre-stage selection. Strong adjacent channel transmitter activates control.

Pin 4: *Ground:*
Decoupling should be referenced to this pin.

Pin 5: *Reference voltage:*
To be decouple to pin 4.

Pin 6/7/8: *Oscillator:*
3 point oscillator with low levels especially for tuning vector diodes.

Pin 9: *Decoupled oscillator output:*
Buffered output specially designed for synthesizer.

Pin 10: *Output IR driver:*
Output with 300Ω corresponding to impedance of conventional IF ceramic filters.

Pin 11: *Stand-by switch:*
The tuner is activated when this pin is tied to ground.

Pin 12: *Input for narrowband information:*
Field strength information of inband signal is forwarded to this pin for use in pre-stage control.

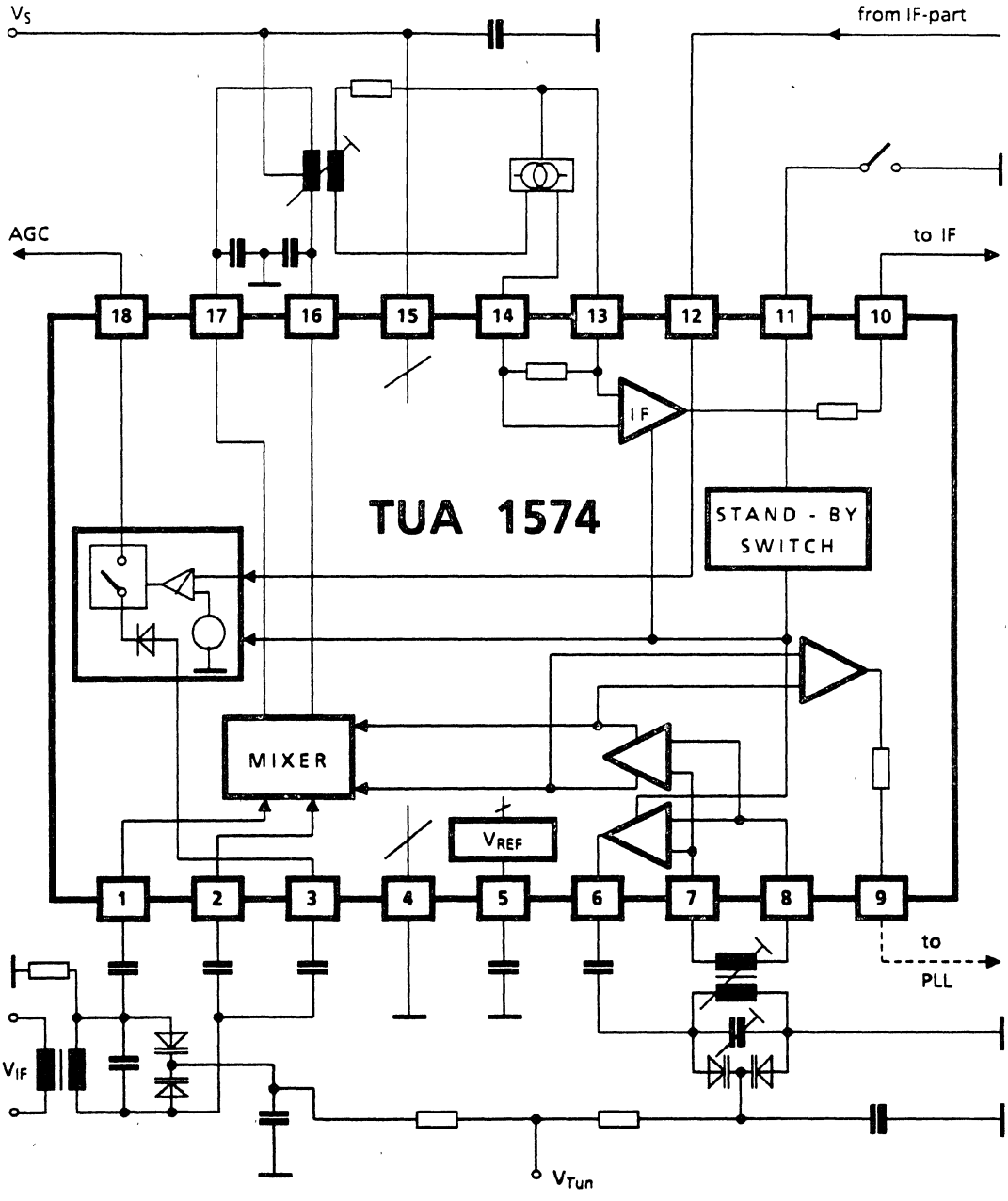
Pin 13/14: *IF driver input:*
IF signal is forwarded to mixer via selection.

Pin 15: *Supply voltage:*
Pin should be RF decoupled against pin 4.

Pin 16/17: *Mixer output:*
Symmetrical open collector output.

Pin 18: *C output:*
Output can be used as current output (pin diodes)
or as voltage output (for bipolar
and/or field effect transistors.

Application circuit



ICs for Universal Applications

9

SIEMENS

Preliminary

SAE 0530, SAE 0531
Programmable Digital Timer

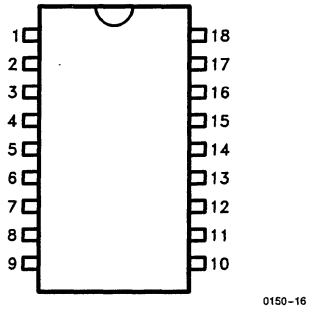
SAE 0530 for 50 Hz frequency

SAE 0531 for 60 Hz frequency

- Direct Operation with AC or DC Supply Possible
- 50 Hz or 60 Hz Supply Frequency as Time Base
- Triac Triggering with Voltage Synchronization for Resistive Loads, or with Current Synchronization for Inductive and Capacitive Loads

Pin Configuration

(Top View)



Pin Definitions

Pin	Symbol	Function
1	0	Circuit-Ground
2	N	Line Voltage via Series Resistor
3	S	Start
4	FC	Function Changeover
5	A	Base Time
6	B	Base Time
7	C	Base Time
8	R	Reset
9	D	Base Time Unit × 1
10	E	Base Time Unit × 2
11	F	Base Time Unit × 4
12	G	Base Time Unit × 8
13	H	Base Time Unit × 16
14	I	Base Time Unit × 32
15	TC	Triac Operation Mode Setting
16	T	Triac Triggering
17	TS	Triac Synchronization
18	V_S	Positive Supply Voltage

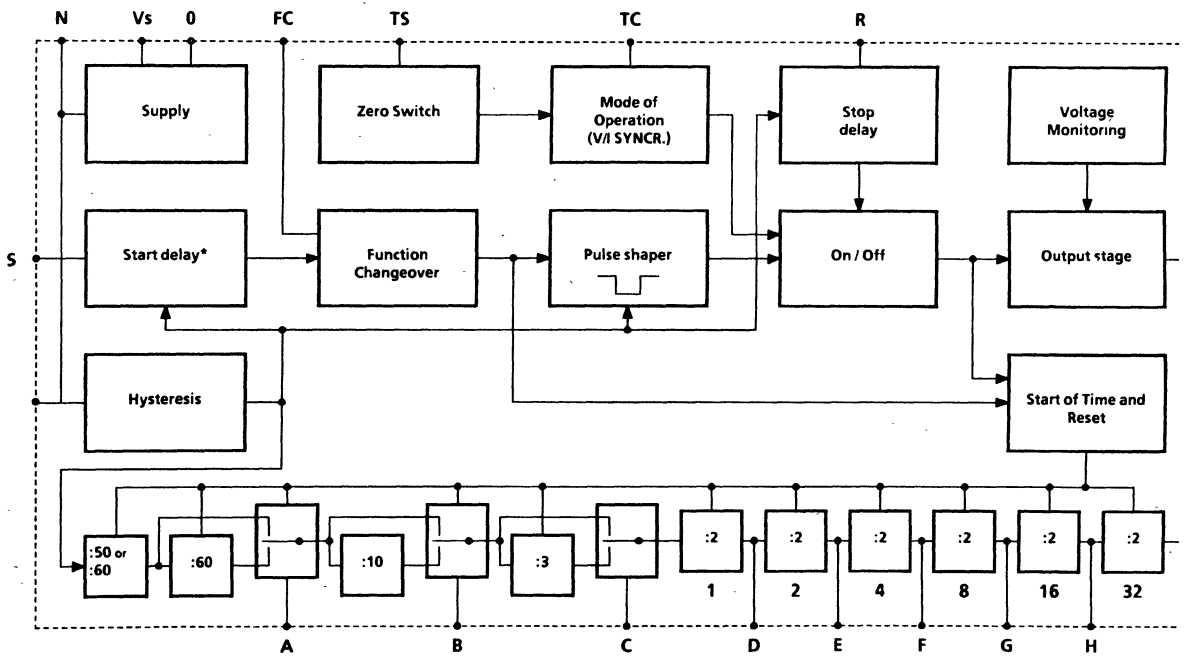
9

The digital timer SAE 0530/SAE 0531 can be programmed for delay times between 1s and 31.5 hrs. It is suited for triggering of triacs, transistors and relays. The IC can be operated direct from mains or DC-supply and requires 50 Hz (SAE 0530) or 60 Hz (SAE 0531) as time base.

Two operational modes are possible with these timers: "momentary switching" and "switch-off delay" (according to DIN 46 120). In the first mode, a rising edge at the start input activates the triac and starts the timing period. In the switch-off delay mode, the rising edge at the start input activates the triac; but the falling edge starts the timing period.

The versatile IC SAE 0530/SAE 0531 covers a great variety of applications, e.g. electronic timers, cooking equipment control, espresso machines, hand-driers, coin-operated machines and slot machines, stairwell light time switches, industrial controls, developing systems for photographic labs, automatic starters (e.g. for oil heating systems), and operating-hour counters.

Block Diagram



0150–1

*For position and Neg. edge.

Functional Description

Through division of the mains frequency by factors 1:50(1:60)*, 1:60, 1:10, and 1:3, the basis for 8 timing periods is created. This timing period is selected via inputs A, B and C, according to the following truth table:

Timing Range	A	B	C	Basic Timing Unit	Max. Time at 50(60)* Hz Line
1	L	L	L	1s	63s (ca. 1 min.)
2	L	L	H	3s	189s (ca. 3 min.)
3	L	H	L	10s	630s (10.5 min.)
4	L	H	H	30s	1890s (31.5 min.)
5	H	L	L	1 min.	63 min. (ca. 1 hr)
6	H	L	H	3 min.	189 min. (ca. 3 hrs)
7	H	H	L	10 min.	630 min. (10.5 hrs)
8	H	H	H	30 min.	1890 min. (31.5 hrs)

Note:
L and H potentials are referred to terminal 0, e.g. L = 0, H = V_S.

The time basis of the set period is multiplied by the corresponding value in the flipflops 1, 2, 4, 8, 16, 32. The flipflops are connected to pins D, E, F, G, H, I so that each pin has the value corresponding to the connected flipflop. The delay time at output T results from connecting a terminal between D and I with terminal R and may be calculated with the formula: Delay time = base time × value of flipflop D . . . I. Should several of the pins D to I be connected to R, the corresponding delay times are added.

Example:

Mains frequency = 50(60)* Hz; set range 1 (base time = 1s); D, F and I are connected to R (value = 37): resulting delay time is 37 seconds.

The timer allows two operation modes which are set through pin FC (function changeover):

1. The **"momentary switching function"** in accordance with DIN 46120.

   The triac at pin T turns "on" with the rising edge at the start input S and turns "off" when the set time has passed, independent of the start pulse length.

2. The **"switch-off-delay"** in accordance with DIN 46120.

   The triac turns "on" with the rising edge at S. The falling edge at S starts the timing period. The triac remains in on-state until the set period has passed.

Function Changeover:

FC	Operation Mode
L	Momentary Switch Function
H	Switch-Off-Delay

To protect the start input S against external interference and contact bounce, it has a **dead time** of between 20 and 40 ms (1/60s to 1/30s)* for positive switching edge, depending on the phase of the 50(60)* Hz line. Both operation modes are retriggerable during the timing period.

Circuit Description

Reset during a timing period is accomplished by interrupting the connection to R, or by applying a high potential to R, or by turning on and off V_S. The reset input R has a dead time of 40 ms (1/30s)*.

Application Note

If R is connected to one of the pins D through I via a multiposition switch, and if during the changeover a reset of the timing period is to be avoided, a suitable capacitor is required between R and 0, if the interruption is > 40 ms (1/30s)*.

With connection of the supply voltage, the circuit is automatically reset. A timing period does not commence if 0 potential is applied to S.

Triac Stage

Pin TS (triac synchronization) is the input of a zero voltage switch and serves to synchronize the output T (open collector) with the load voltage or the load current.

With V_S < 3V, the output current is disconnected.

The input TC has a double function:

- To change TS over to voltage synchronization.
- To adjust the triac trigger pulse width (by connecting a capacitor C_e to TC) in case of current synchronization.

Three operation modes are possible by varying the connection of the pins TC and/or TS:

Operation Mode 1:

TC to V_S: Output T is connected to the zero voltage switch. T operates when $V_S - 1.3V \leq V_{TS} \leq V_S + 1.3V$.

Is utilized in case of voltage synchronization; see application circuit 1 (operation with resistive loads) and pulse diagram.

Note:
*Valid for 60 Hz version.

Operation Mode 2:

TC via C_e to Q: Output T is connected to the zero voltage switch via a monoflop. If V_S −1.3V is fallen below or V_S +1.3V exceeded at TS, the output T releases a triac gate trigger pulse determined by C_e.

Is utilized in case of current synchronization; see application circuit 2 and pulse diagram.

Operation Mode 3:

TC and TS to V_S: Output T conducts after release of start pulse.

Is utilized for any load in case of continuous triac triggering (e.g. low performance), or if any other load is to be operated instead of the triac (see application circuits 3, 4, 5).

Operation with Line Voltage

A series resistor R_S and a charging capacitor C_{ch} serve for line voltage supply. If a diode is connected in series with R_S (anode to N), the rms current consumption is halved. The series resistor may also be an RC combination (see application circuit 6).

Operation with DC Voltage

This IC can also be operated with DC voltage or current (see application circuits 4 and 5).

Dimensioning the Application Circuits

The following formulas give reference values for operation with sine-shaped DC voltages of 50(60)* Hz. The triac is always triggered with negative gate current.

$$\text{Trigger Pulse Length Z:Z} = \frac{5(4.18)^* \times \text{Holding Current}}{\text{rms Load Current}}\ [\text{ms}];$$

Applies to Z ≤ 1 ms

Note:

*Valid for 60 Hz version.

$$R_G = \frac{V_S - V_{TL} - \text{Gate Trigger Voltage}}{\text{Gate Trigger Current}}$$

$$R_V = \frac{0.5 \times \text{rms Line Voltage} \times -V_S}{I_S + \text{Average Gate Trigger Current}}$$

(With or Without Diode D)

Average Gate Trigger Current = $0.1(0.12)^*$ × Gate Trigger Current × Z (Z in ms)

$$\text{Power Dissipation at } R_S \text{ (Without Diode D)} = \frac{(\text{rms Line Voltage})^2}{R_S}$$

$$\text{Power Dissipation at } R_S \text{ (With Diode D)} = 0.5\,\frac{(\text{rms Line Voltage})^2}{R_S}$$

$$C_L = \frac{20(17)^* \times \text{rms Line Voltage}}{R_S}\ [\mu\text{F, V, k}\Omega]$$

(Residual AC Voltage at $V_S \leq 0.5\ V_{SS}$)

Note for C_L:

If short-term line failures are to be compensated, C_L has to be accordingly larger. (Approx. 1000 µF for ≤ 5s line failure.)

Note:

*Valid for 60 Hz Version.

Application Circuit 1 (Voltage Synchronization for Resistive Load)

$$R_{Syn} = \frac{0.22(0.27)^* \times Z \times \text{rms Line Voltage} - 1.3}{0.04}$$

$$\geq \frac{\text{Peak Line Voltage}}{4}\ [\text{k}\Omega, \text{V, ms}]$$

(Valid for Z ≤ 1.5 ms)

Notes for Application Circuit 1

An average ITS of 0.04 mA was inserted into the formulas approximating RSYNC. As ITS+ and ITS− contain production deviations, utilizing the determined RSYNC requires certain tolerances to be taken into account for pulse length Z.

To minimize the effect of these tolerances, a resistor may be connected between VS and TS, which generates a constant current of $\frac{V_{TS}}{R}$ to be added to I_{TS}.

However, a TC of −4 mV/K should be noted.

Note:

*Valid for 60 Hz version.

Application Circuit 2 (Current Synchronization)

$C_e = 22 \times Z$ [nF, ms]

$$R_{SYNC} \geq \frac{\text{Max. On} - \text{State Voltage} - 1.3}{I_{TSmin}} \text{ [k}\Omega\text{, V, mA]}$$

$$R_{SYNC} \geq \frac{\text{Peak Line voltage}}{4} \text{ [k}\Omega\text{, V]}$$

$$R_{SYNC} \leq \frac{\text{GateTrigger Voltage} - 1.3}{I_{TSmax}} \text{ [k}\Omega\text{, V, mA]}$$

Notes for Application Circuit 2

In this circuit, an even shorter pulse length than determined for Z is sufficient to trigger the triac. This is possible by the trigger pulse being automatically repeated until the holding current is reached. Overdimensioning of Z for safety reasons is, therefore, not necessary. The disadvantage of multiple trigger pulses, however, is a somewhat larger interference band during the triggering.

The interference band and/or the interference amplitude generated also depend on the amount of the gate trigger voltage necessary to trigger the triac after each current zero passage. That voltage is determined by the size of R_{SYNC} and should not be more than 20V.

Application Circuit 3

Dimensioning of R_S, R_G and C_{ch} as described at the beginning of this section.

Application Circuit 4

$R_N \approx 15 \times$ AC Voltage 50(60)* Hz [kΩ, V_{eff}]

Application Circuit 5

R_N see above. The AC voltage for the timing base must be greater than (supply voltage -4.8V).

$$R_0 = \frac{+ \text{ Supply Voltage} - 6.8\text{V}}{I_S + I_{R1}} \qquad I_{R1} = I_{B\,(TQ)} + I_{R2}$$

$$R_1 = \frac{6.8\text{V} - V_{TL} - V_{B(TQ)}}{I_{R1}} = I_{R2} \approx 0.05\, I_{B(TQ)}$$

$$R_2 = \frac{V_{B(TQ)}}{I_{R2}}$$

Application Circuit 6

$$C_S \approx \frac{4(3.3)^*}{R_S} \text{ [}\mu\text{F, k}\Omega\text{]}$$

$R_{SS} = 0.2 \times R_S$

To limit the inrush current, R_{SS} has to be $\geq 0.2\, R_S$. Otherwise, the circuit may be damaged.

Note:
*Valid for 60 Hz version.

Absolute Maximum Ratings*

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit. Max. ratings for case temperature -25°C to $+85$°C.

Parameter	Symbol	Limits		Units	Notes
		Min	Max		
Supply Voltage at Impressed DC Voltage	V_S	-0.3	$+5.5$	V	
Peak Current at N	$-I_{NP}$		18	mA	50 Hz Operation with $V_S \leq 7.5$V
DC Current from N (rms)	$-I_{Nrms}$	-50	$+50$	mA	50 or 60 Hz Operation
AC at N with Impressed Current	I_{Nrms}		35	mA	rms Value
Peak Current at N	I_{NP} I_{NP}	-200 -350	$+200$ $+350$	mA mA	2 ms/100 ms Duty Cycle 0.3 ms/100 ms Duty Cycle
Voltage at A, B, C, FC, R, S	V_A	-0.3	7.5	V	

Absolute Maximum Ratings* (Continued)

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit. Max. ratings for case temperature −25°C to +85°C.

Parameter	Symbol	Limits		Units	Notes
		Min	Max		
Voltage at D, E, F, G, H, I	V_D	−0.3	7.5	V	D . . . I Off-State
Voltage at N, with N Utilized as Clock Input	V_{NT}	−0.3	V_S	V	
Voltage at T	V_T	−0.3	7.5	V	
Voltage at TC	V_{TC}	−0.3	V_S	V	
Current in D, E, F, G, H, I	I_D		0.5	mA	D . . . I On-State
Continuous Current in T	I_T		100	mA	
Peak Current in T	I_{TS}		150	mA	1 ms/10 ms Duty Cycle
Current at TS	I_{TS}	−4	+4	mA	
Junction Temperature	T_j		125	°C	
Storage Temperature	T_{stg}	−55	+125	°C	
Thermal Resistance: System Air	R_{thSA}		70	K/W	

All the voltages refer to pin 0, unless otherwise specified.

Operating Range

Within the functional range, the IC operates as described; deviations from the characteristic data are possible.

Parameter	Symbol	Limits		Units	Notes
		Min	Max		
Supply Voltage	V_S	4.5	5.5 (8.2)	V	*
DC Supply at N(rms)**	$-I_N$	2.5	18	mA	*
AC Supply at N(rms)**	I_{Neff}	5	35	mA	*
Ambient Temperature	T_A	−25	85	°C	

Notes:

*The operating voltage should not exceed 5.5V when AC voltage is impressed. The IC can also be operated with AC or DC current. In case current is impressed at N the V_S is limited between 6V and 8.2V (typ. 7.5V). The IC functions, however, up to 4.5V.

**Only the supply current for the IC, i.e. without triac gate current. The rms gate current flows additionally through N.

Characteristics

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not stated otherwise, typical characteristics will apply at $4.5 \leq V_S \leq 5.5$ (7.5)* V; $-25°C \leq T_A \leq 85°C$.

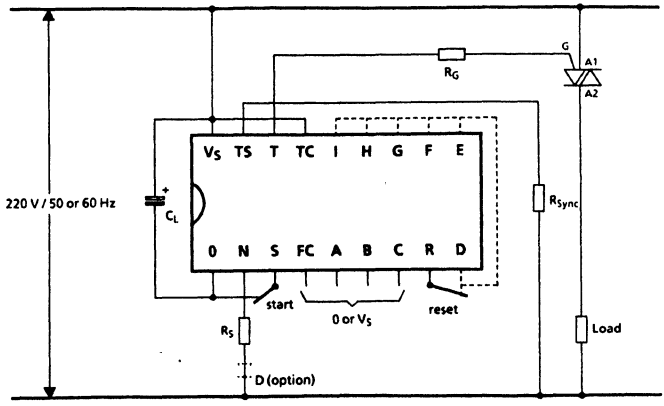
Parameter	Symbol	Conditions	Test Circuit	Limits			Units
				Min	Typ	Max	
Supply Current	I_S	$V_{Input\,S} = 0V$			1.5	2.5	mA
V_S with Impressed Current at N:* V_S Impressed AC* V_S Impressed DC	 V_S V_S	 $I_{Neff} = 5$ mA $-I_N = 2.5$ mA			 7.5 7.5	 8.2 8.2	 V V
Switching Threshold at: A, B, C, S, FU, R	 V_A			 1.1	 1.8	 2.2	 V
H-Switching Threshold at N**	V_N				2	2.4	V
L-Switching Threshold at N**	V_N			0.8	1.1		V
Switching Threshold at TC	V_{TC}				3.4	4.5	V
Switching Threshold at TS (For Voltages > V_S)	V_{TS+}				$V_S+1.3$		V
Switching Threshold at TS (For Voltages < V_S)	V_{TS-}				$V_S-1.3$		V
L-Input Current at: A, B, C, FC, R	$-I_A$	$V_A = 0V$			20	30	µA
L-Input at S	$-I_{InS}$	$V_{Input\,S} = 0V$			60	90	µA
L-Input Current at N**	$-I_N$	$V_N = 0V$			40	60	µA
H-Input Current at: A, B, C, S, FU, R	I_A	$V_A = V_S$				1	µA
H-Input Current at N**	I_N	$V_N = V_S$				1	µA
H-Input Current at TC	I_{TC}	$4.5 \leq V_{TC} \leq V_S$			20	40	µA
Positive Switching Current at TS	I_{TS+}			20	40	80	µA
Negative Switching Current at TS	I_{TS-}			20	40	80	µA
L-Voltage at D, E, F, G, H, I	V_D	$I_D = 0.5$ mA			0.2	0.4	V
H-Reverse Current at D, E, F, G, H, I	I_D					1	µA
L-Output Voltage at T	V_O V_O V_O	$I_T = 1$ mA $I_T = 10$ mA $I_T = 100$ mA			0.7 0.8 1	1.1 1.2 1.5	V V V

Notes:
*With current impressed at N
**For N as clock input

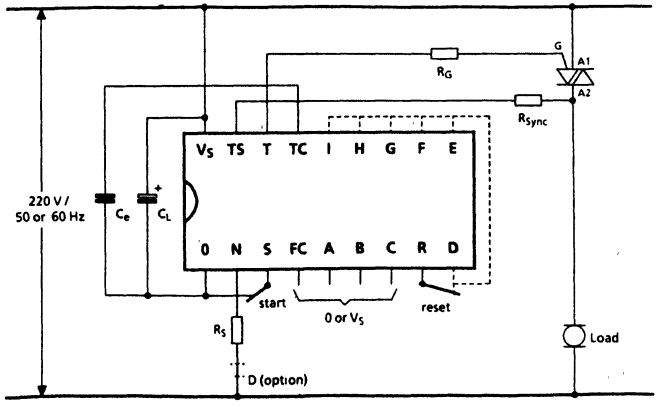
9

Application Circuits

Operation with Resistive Load

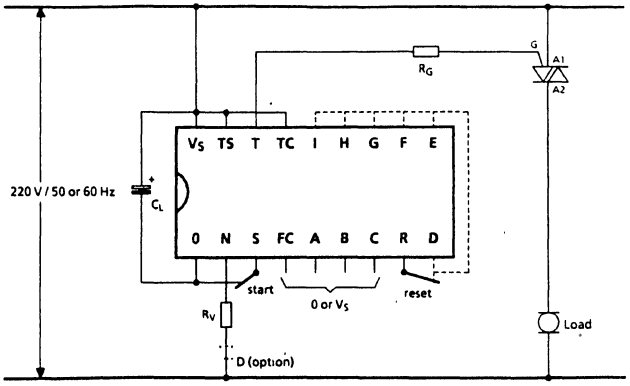


Operation with Resistive, Capacitive or Inductive Loads

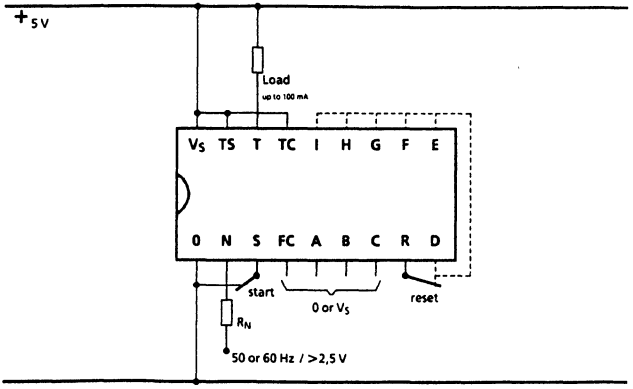


Application Circuits (Continued)

Operation with Any Load and Continuous Triac Triggering



Operation with 5V DC Voltage



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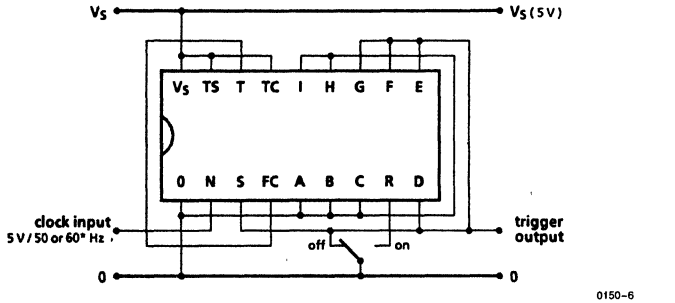
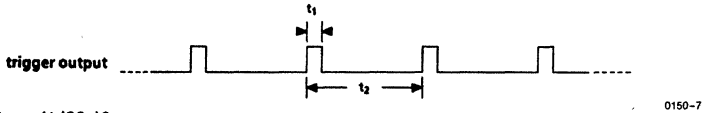
Application Circuits (Continued)

Pulse Generator

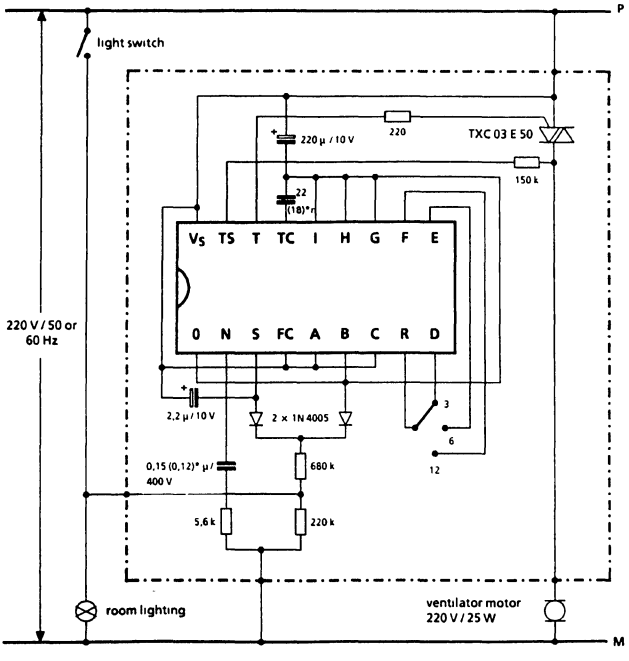




t_1 (Pulse Width) = 40 ms (1/30s)*
t_2 (Selected Time) = 15s

Notes:
*Valid for 60 Hz version.
The pulse width t_1 is determined by the clock frequency at clock input N:
$t_1 = 2/f = 2/50\ (2/60)^* = 40$ ms (1/30s)*
Direct after switch on the pulse width t_1 and the first time period t_2 can be shorter by 20 ms (1/60s)* depending on the phase of 50 Hz or 60 Hz clock input.
The output T is conducting after switch on and remains on L-potential throughout the operating time.

Time Control for Bathroom Ventilator Motor, (Adjustable to 3, 6 or 12 minutes ventilation)



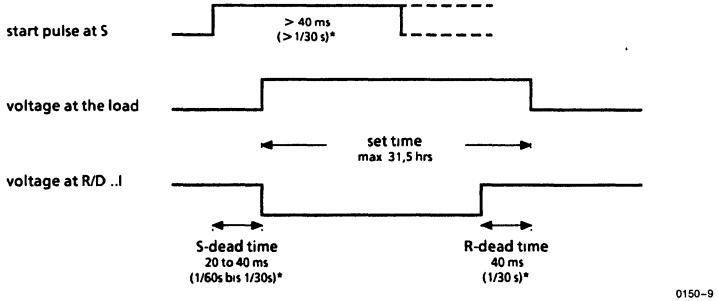
Application Description of a Ventilator Motor Control:
The ventilator is activated with the light switch and automatically switches the motor off after a programmable time delay of 3, 6 or 12 minutes after the light switch is turned off.
(We don't take any responsibility for the component values in this application.)

*Valid for 60 Hz version.

Diagrams

Pulse diagrams of the two operation modes set with pin FC:

Momentary Switching Function



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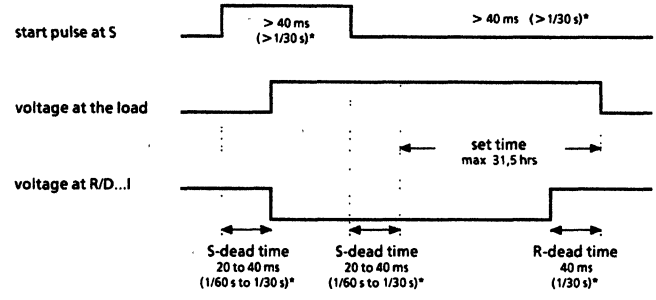
Diagrams (Continued)

Pulse Diagrams of the two operation modes set with pin FC (Continued)

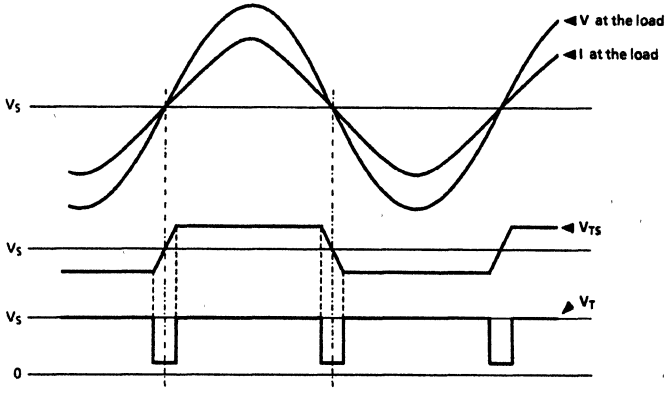
Switch-Off-Delay



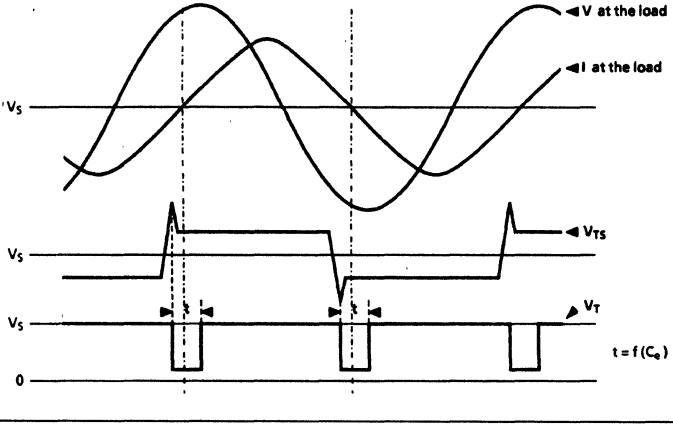
*Valid for 60 Hz version.

Pulse Diagrams for Triac Operation Modes 1 and 2

Operation Mode 1 Voltage Synchronization with Resistive Loads (TC to V_S)

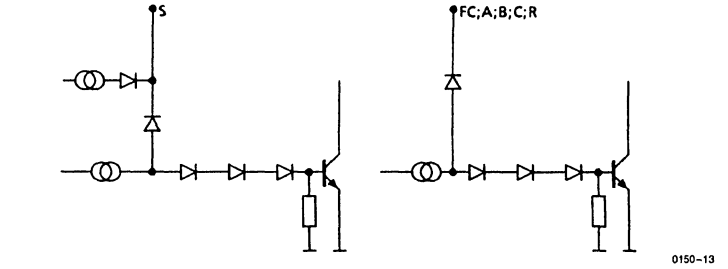


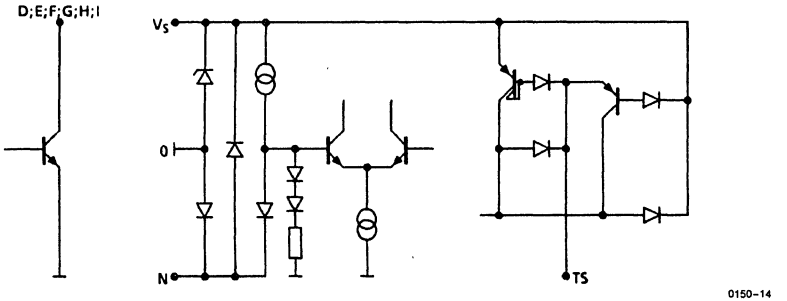
Operation Mode 2 Current Synchronization with Nonresistive Loads (Capacitance C_e to TC)

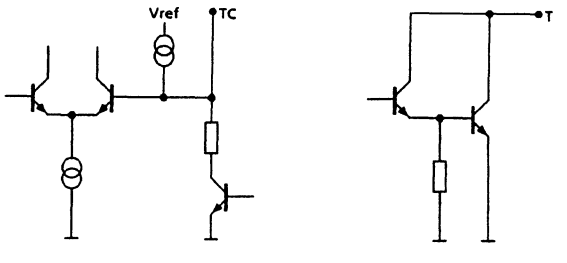


Appendix

Internal Connection of the Input, Output and Supply Pins







Comparison of the Different Timers

Characteristics	Type	SAB 0529	SAE 0530	SAE 0531
Package		DIP 18, SO 20	DIP 18, SO 20	DIP 18, SO 20
		Same Pin Configuration		
Mains Frequency		50 Hz	50 Hz	60 Hz
Temperature Range		0°C to +70°C		−25°C to +85°C
Switch in Delay at S		For Leading Edge	For Leading as Well as Trailing Edge	
Switch in Delay at R		No		Yes
Start Response after Connecting V_S	S = L	No Start		No Start
	S = H	Undefined		Timer Starts

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Comparison of the Different Timers (Continued)

Characteristics	Type	SAB 0529	SAE 0530	SAE 0531
Integrated Pull-Up Resistance at S		No		Yes
Switching Threshold at A, B, C, S, FU, R		0.6V		1.8V
Switching Threshold at N		1.2V		1, ½V, Hysteresis of 0.9V
State of Pins D to I after Reset		L		H
Output Voltage at T by 100 mA		1.8V		1V
Operation as Pulse Generator		With External Components		Without External Components

Note:
For other minor deviation please see max. ratings and characteristics of the components.

Ordering Information

Type	Ordering Code	Package
SAE 0530	Q 67000-H8403	DIP 18
SAE 0531	Q 67000-H8431	DIP 18

SIEMENS

SAE 81 C 52
256 x 8-Bit Static CMOS RAM
NMOS-Compatible

Preliminary data

Type	Ordering code	Package
SAE 81C52 P	Q67100-H8003	DIP 16
SAE 81C52 G	Q67100-H8004	SO-20

The SAB 81C52P is a CMOS silicon gate, static random access memory (RAM), organized as 256 words by 8 bits. The multiplexed address and data bus allows to interface directly to 8-bit NMOS microprocessors/microcomputers without any timing or level problems, e.g. the families SAB 8085, SAB 8088, SAB 8048, SAB 8051, and SAB 80515.

All inputs and outputs are fully compatible with NMOS circuits, except CS 1. Data retention is given up to $V_{DD} \geq 1.0$ V. The SAB 81C52P has three different inputs for two chip select modes which allow to inhibit either the address/data lines (AD 0...AD 7) and the control lines ($\overline{WR}$, $\overline{RD}$, ALE, CS 2, $\overline{CS\ 3}$), or only the control lines $\overline{RD}$, $\overline{WR}$.

The power consumption is max. 5.5 µW in standby mode and max. 2.75 mW in operation. In standby mode, the power consumption will not increase if the control inputs are on undefined potential.

Features

- 256 x 8-bit organization
- standby mode
- compatible with the µC/µP families SAB 8085, SAB 8088, SAB 8048, SAB 8051, the new SAB 80515, etc.
- very low power dissipation
- data retention up to V_{DD} = 1 V
- three different chip select inputs for two chip select modes
- no increasing power consumption in standby mode if the control inputs are on undefined potential
- Temperature range: SAB 81C52 0°C to 70°C
  SAE 81C52 −40°C to +85°C *)
- Package: DIP 16 or SO-20

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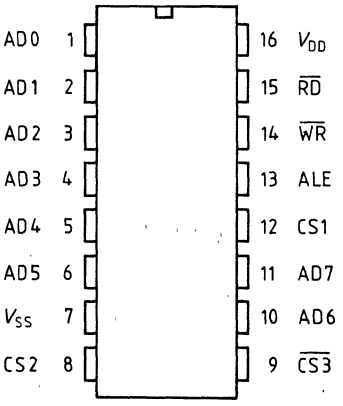
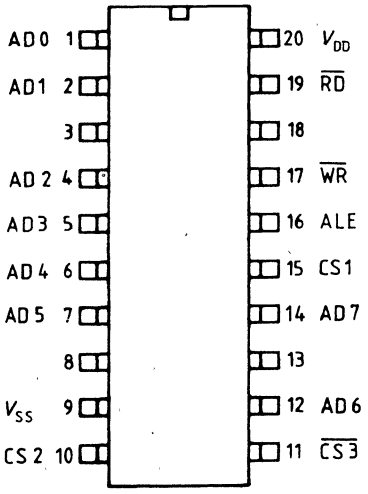
*) Values for applications up to −40°C to +110°C upon request.

Pin configurations
(top view)

SAB 81C52 P
SAE 81C52 P



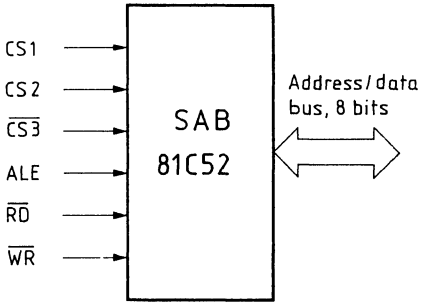
SAE 81C52 G



Pin designation

Pin No.		Symbol	Function
SAE 81C52 G	**SAB 81C52 P SAE 81C52 P**		
1, 2, 4, 5, 6 7, 12, 14	1...6 10, 11	AD 0...7	Address/data lines
15	12	CS 1	Chip select 1 (standby) active low; inhibits all lines including control lines
16	13	ALE	Address latch enable
17	14	$\overline{WR}$	Write enable
19	15	$\overline{RD}$	Read enable
20	16	V_{DD}	Power supply
9	7	V_{SS}	GND
10	8	CS 2	Chip select 2; inhibits control inputs $\overline{RD}$, $\overline{WR}$
11	9	$\overline{CS\ 3}$	Counterpart to CS 2

Logic symbol



Truth table

CS 1	CS 2	$\overline{CS\ 3}$	ALE	$\overline{RD}$	$\overline{WR}$	AD Ø...AD 7	Function
L	✳	✳	✳	✳	✳	floating (tristate)	standby
H	X	X	H	H	H	addresses to memory	store addresses
H	H	L	L	L	H	data from memory	read
H	H	L	L	H	L	data to memory	write
H	L	X	L	X	X	floating (tristate)	none
H	X	H	L	X	X	floating (tristate)	none

✳: Level = V_{SS}...V_{DD}
X: Level = LOW or HIGH

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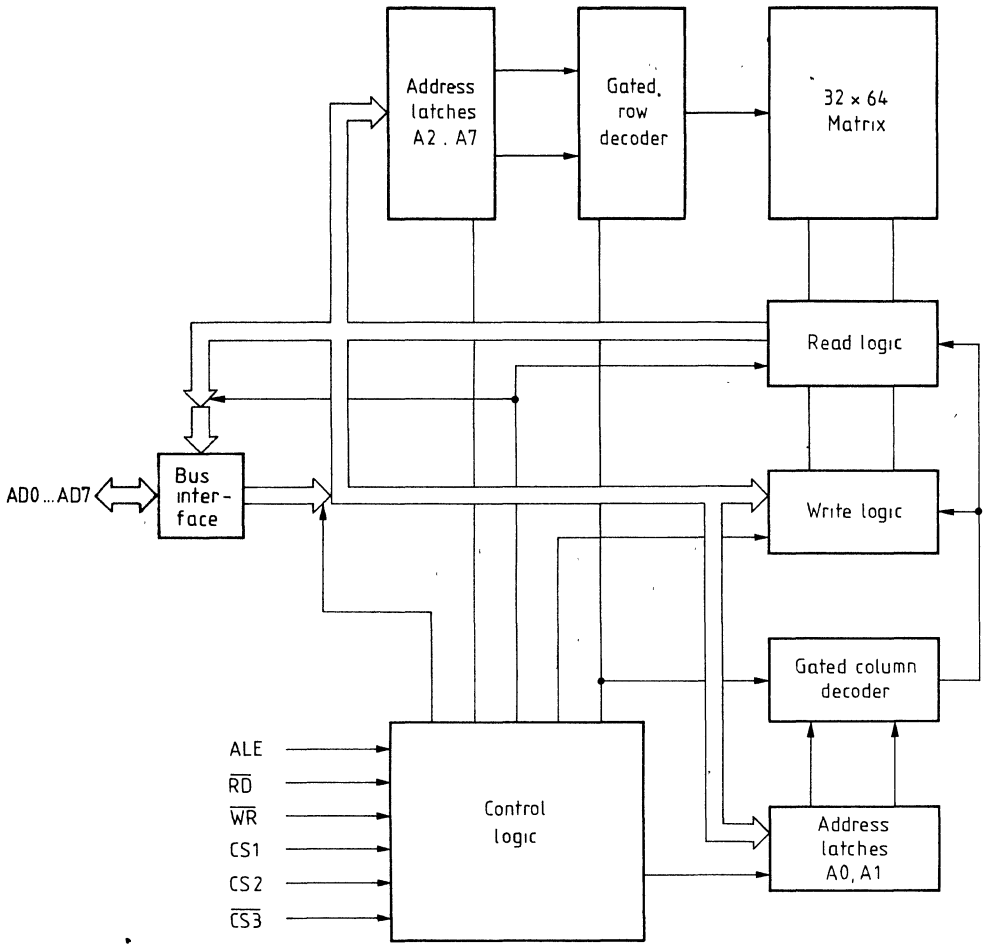
Block diagram



Maximum ratings

Maximum ratings are absolute limits. The integrated circuit may be destroyed if only a single value is exceeded.

Supply voltage reffered to GND (V_{SS})	V_{DD}	−0.3 to 6	V
All input and output voltages	V_{IM}	V_{SS} −0.3	V
		V_{DD} +0.3	V
Total power dissipation	P_{tot}	250	mW
Power dissipation for each output	P_Q	50	mW
Junction temperature	T_j	125	°C
Storage temperature	T_{stg}	−55 to 125	°C
Thermal resistance	$R_{th\,SA}$	70	K/W

Operating range

In the operating range, the functions shown in the circuit description will be fulfilled. Deviations from the electrical characteristics may be possible.

Supply voltage	V_S	4.5 to 5.5	V
Ambient temperature: SAE 81C52	T_{amb}	−40 to 85*)	°C
SAB 81C52	T_{amb}	0 to 70	°C

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*) Values for applications up to 110°C upon request

Electrical Characteristics

The electrical characteristics include the guaranteed tolerance of the values which the IC stays within for the specified operating range.

The typical characteristics are average values which can be expected from production. Unless otherwise specified, the typical characteristics apply to T_{amb} and the specified supply voltage.

DC characteristics

SAE 81C52: T_{amb} = –40°C to +85°C;
SAB 81C52: T_{amb} = 0°C to 70°C;
} V_{DD} = 4.5 V to 5.5 V, V_{SS} = 0 V

		Test conditions	min.	max.	
Standby supply current	I_{DD}			1	µA
Supply current	I_{DD}	f = 1 MHz		500	µA
Standby voltage for data retention	V_{DD}		1.0		V
L input current (for each input)	I_{IL}	V_I = 0 to V_{DD}		1	µA
Output leakage current	I_{QIK}	V_Q = 0 to V_{DD} tristate		1	µA
L input voltage	V_{IL}	except CS1		0.8	V
H input voltage	V_{IH}	except CS1	2.2		V
L output voltage	V_{QL}	I_{QL} = 1 mA		0.4	V
H output voltage	V_{QH}	I_{QH} = 1 mA	2.6		V
L input voltage CS1	V_{IL}			1	V
H input voltage CS1	V_{IH}		V_{DD} –1		V

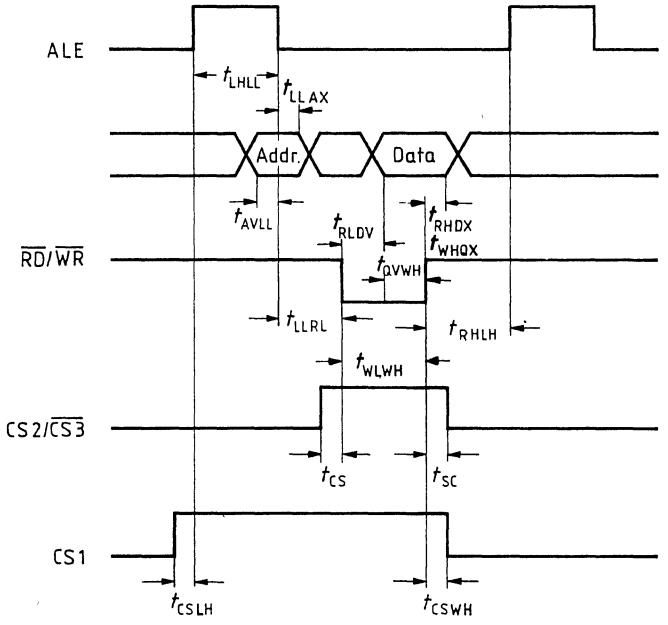
AC characteristics

SAE 81C52: T_{amb} = –40°C to +85°C*);
SAB 81C52: T_{amb} = 50°C to 70°C;
} V_{DD} = 4.5 V to 5.5 V; V_{SS} = 0 V

		min.	max.	
ALE pulse width	t_{LHLL}	100		ns
ALE LOW to $\overline{RD}$ LOW	t_{LLRL}	50		ns
$\overline{RD}$ HIGH to ALE HIGH	t_{RHLH}	30		ns
ALE LOW to $\overline{WR}$ LOW	t_{LLWL}	50		ns
$\overline{WR}$ HIGH to ALE HIGH	t_{WHLH}	30		ns
Address setup before ALE	t_{AVLL}	25		ns
Address hold after ALE	t_{LLAX}	20		ns
$\overline{WR}$ or $\overline{RD}$ pulse width	t_{WLWH}	250		ns
Data setup before $\overline{WR}$	t_{QVWH}	100		ns
Data hold after $\overline{WR}$	t_{WHQX}	30		ns
Data hold after $\overline{RD}$	t_{RHDX}		90	ns
Chip select (2, 3) before $\overline{RD}$, $\overline{WR}$	t_{CS}	50		ns
Chip select (2, 3) after $\overline{RD}$, $\overline{WR}$	t_{SC}	50		ns
Chip select 1 before ALE	t_{CSLH}	20		ns
Chip select 1 after $\overline{RD}$, $\overline{WR}$	t_{CSWH}	50		ns
Output delay time	t_{RLDV}		200	ns
Input capacitance against V_{SS} (for each input)	C_I		10	pF

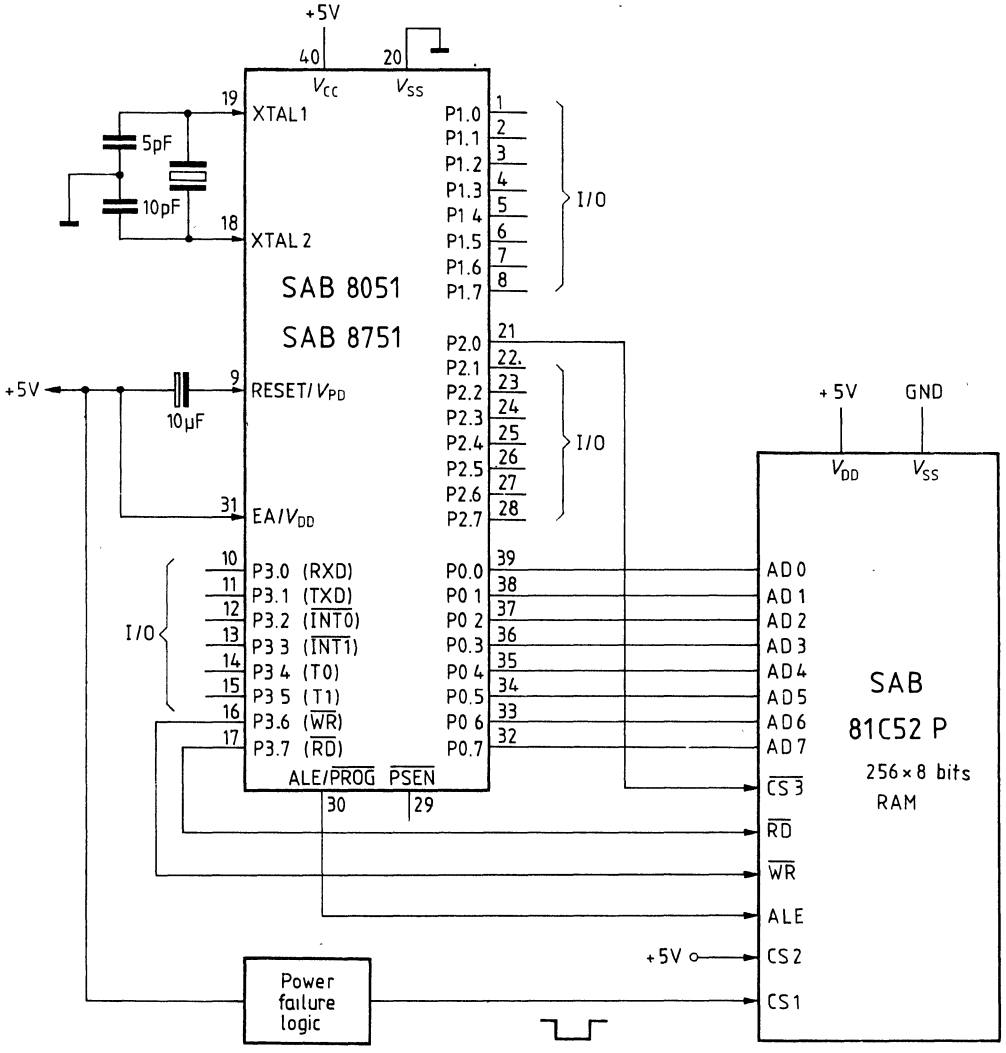
*) Values for applications up to 110°C upon request

Timing diagram



Application circuit

SAB 81C52 P with the µC SAB 8051



SIEMENS

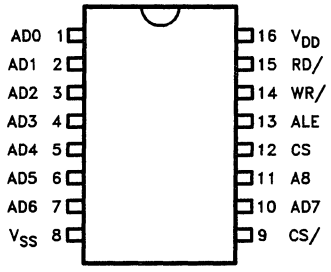
Preliminary

SAE 81C54
CMOS Static RAM

- 512 x 8-Bit Organization
- Multiplexed Address and Data Bus
- Tri-State Address/Data Lines
- On-Chip Address Register
- Very Low Power Consumption
  Standby 1 μA at 6V
- Two Chip Select
- Wide Supply Voltage Range: 2.5V to 6V
- Data Retention 1.0V
- Package: DIP 16, SO-20

Pin Configuration

(Top View)



0114-1

Pin Definitions

Pin	Symbol	Function
1–7, 10	AD 0–7	Address/Data Lines
8	V_{SS}	Ground (0V)
9	CS/	Chip Select
11	A8	Address Line
12	CS	Chip Select
13	ALE	Address Latch Enable
14	WR/	Write Enable
15	RD/	Read Enable
16	V_{DD}	Power Supply (2.5V–6V)

The SAE 81C54 is a 4096-bit static random access memory (RAM) organized as 512 words by 8 bits, manufactured using advanced CMOS technology. The multiplexed address and data bus allows direct interface with 8-bit organized processors and microcomputers, for example with SAB 8085, SAB 8086, SAB 8088, SAB 8048, SAB 0C48, SAB 8051 and SAB 80C482. Low standby power dissipation (<1 μA) minimizes system power requirements.

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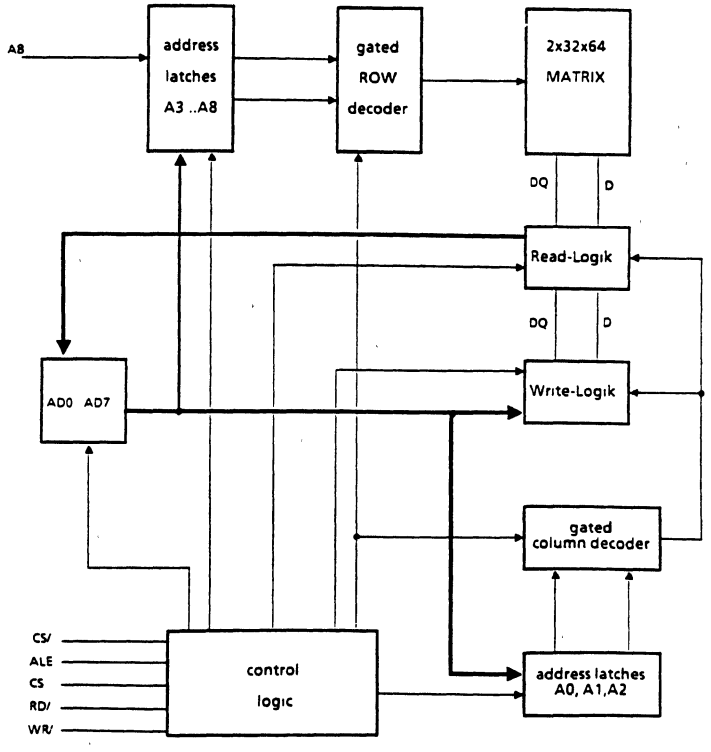
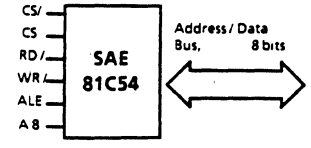
Block Diagram



Logic Symbol



Truth Table for Control and Data Bus Pin Status

CS/	CS	RD/	WR/	AD 0–AD 7 During Data Portion of Cycle	Function
H	X	X	X	Floating	No Function
X	L	X	X	Floating	No Function
L	H	L	H	Data from Memory	Read
L	H	H	L	Data to Memory	Write

Absolute Maximum Ratings*

Ambient Temperature under Bias (T_A) ..... −40°C to +110°C

Storage Temperature (T_{stg}) ..... −55°C to +125°C

Supply Voltage with Respect to GND (V_{SS}) (V) ..... 0V to 7V

Total Power Dissipation (P_{tot}) ..... 250 mW

All Input and Output Voltage . −0.8V to V_{DD} + 0.8V

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics $T_A = -40°C$ to $+85°C$*; ($V_{DD} = 2.5V$ to $6V$; $V_{SS} = 0V$)

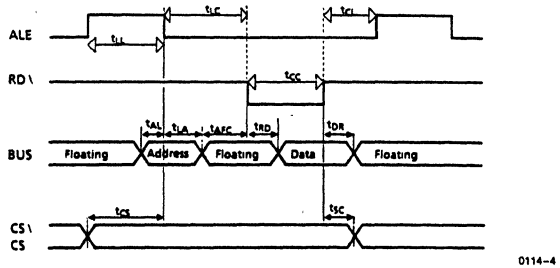
Parameter	Symbol	Conditions	Limits			Units
			Min	Typ	Max	
Standby Supply Current	I_{DD}				1	μA
Operating Supply Current	I_{DD}	100 kHz ALE		500		μA
Operating Supply Voltage	V_{DD}		2.5		6	V
Standby Voltage	V_{DD}	for Data Retention	1.0		6	V
Input Current	I_{IL}	VI = 0V to 6V			1	μA
Output Leakage Current	I_{OL}	V0 = 0V to 6V High Impedance			1	μA
L Input Voltage ($V_{DD} < 4.5V$)	V_{IL}		−0.8		0.6	V
L Input Voltage ($V_{DD} > 4.5V$)	V_{IL}		−0.8		0.8	V
H Input Voltage	V_{IH}		$0.6 \times V_{DD}$		$V_{DD} + 0.8$	V
H Input Voltage	V_{IH}	$V_{DD} = 5V$	2.0		$V_{DD} + 0.8$	V
L Output Voltage ($V_{DD} < 4.5V$)	V_{OL}	$I_{OL} = 1$ mA			0.4	V
L Output Voltage ($V_{DD} > 4.5V$)	V_{OL}	$I_{OL} = 2$ mA			0.4	V
H Output Voltage ($V_{DD} < 4.5V$)	V_{OH}	$I_{OH} = 1$ mA	$0.75 \times V_{DD}$			V
H Output Voltage ($V_{DD} > 4.5V$)	V_{OH}	$I_{OH} = 2$ mA	$0.75 \times V_{DD}$			V

A.C. Characteristics $T_A = -40°C$ to $+85°C$, $V_{DD} = 5V$; $V_{SS} = 0V$

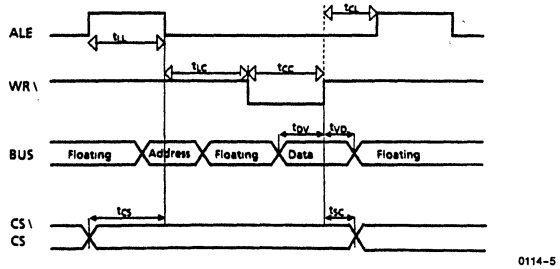
Parameter	Symbol	Limits			Units
		Min	Typ	Max	
ALE Pulse Width	t_{LL}	60			ns
Address Set-Up before ALE	t_{AL}	10			ns
Address Hold from ALE	t_{LA}	45			ns
$\overline{RD}$, $\overline{WR}$ Pulse Width	t_{CC}	150			ns
Data Set-Up before $\overline{WR}$	t_{DW}	100			ns
Data Hold after $\overline{WR}$	t_{WD}	25			ns
Data Hold after $\overline{RD}$	t_{DR}	0		95	ns
$\overline{RD}$ to Data Out Access Time	t_{RD}			150	ns
Address Float to $\overline{RD}$	t_{AFC}	0			ns
CS before ALE	t_{CS}	30			ns
CS After $\overline{WR}$ or $\overline{RD}$	t_{SC}	30			ns
ALE to $\overline{RD}$-$\overline{WR}$ control	t_{LC}	100			ns
$\overline{RD}$-$\overline{WR}$ Control to ALE High	t_{CL}	30			ns

Timing Waveforms

Read



Write



Ordering Information

Type	Ordering Code	Package
SAE 81C54 P	Q 67100-H8486	DIP 16
SAE 81C54 G	Q 67100-H8487	SO-20

SIEMENS

SAE 81 C 80
Dual Port RAM

Preliminary Data

Type	Ordering Code	Package
SAE 81C80	Q67100-H8390	PLCC 44

The SAE 81C80 dual port RAM (DPR) is a CMOS memory IC with two processor interfaces and a capacity of 504 bytes. It enables the exchange of data between two processors without handshake signals and without wait states. Eight scheduling registers support the management of data areas or external resources.

Features

- ACMOS technology
- All functions fully static
- SAB 8048/8051/80515 and 8096 compatible
- Memory capacity 504 bytes and 8 scheduling registers
- On-chip oscillator with separate clock output
- 3 loadable counters for processor monitoring or as longterm counters
- Hardware watchdog
- Both processors can operate fully asynchronously
- Data retention down to 1 V
- TTL-, NMOS- and CMOS-compatible
- Extended temperature range from −40 °C to +85 °C
- Package: PLCC 44

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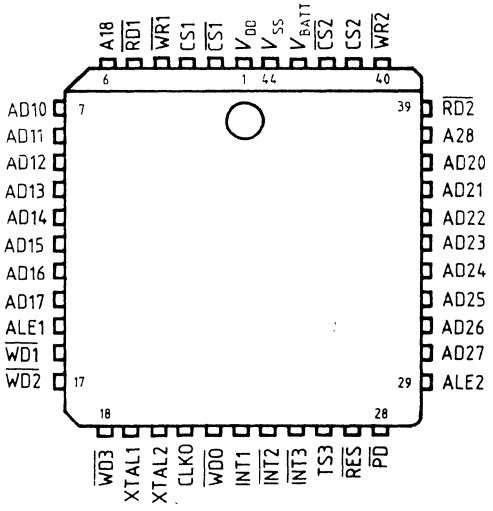
Edition 3.87

SMD = Surface Mounted Device

Pin Configuration



Pin Description

Pin	Symbol	Function
7	AD10	Data and address bus port 1
8	AD11	
9	AD12	
10	AD13	
11	AD14	
12	AD15	
13	AD16	
14	AD17	
6	A18	Address 8 port 1
37	AD20	Data and address bus port 2
36	AD21	
35	AD22	
34	AD23	
33	AD24	
32	AD25	
31	AD26	
30	AD27	
38	A28	Address 8 port 2

Pin Description

Pin	Symbol	Function
15 29	ALE1 ALE2	Address latch enable port 1 Address latch enable port 2 These signals serve to separate data from addresses on the bus. The address is stored on the falling edge of the signal.
5 39	$\overline{RD1}$ $\overline{RD2}$	Read signal port 1 (active low) Read signal port 2 (active low)
4 40	$\overline{WR1}$ $\overline{WR2}$	Write signal port 1 (active low) Write signal port 2 (active low)
3	CS1	Chip select port 1
2	$\overline{CS1}$	Chip select port 1 (active low)
41	CS2	Chip select port 2 Chip select port 2 (active low)
42	$\overline{CS2}$	The chip select inputs select a port when both inputs have active level.
27	$\overline{RES}$	Reset input Resets the IC to a defined start state. Simultaneously, the outputs $\overline{WDO}$, $\overline{WD1}$, $\overline{WD2}$, $\overline{WD3}$ are switched to low for the duration of the reset pulse. The oscillator is not affected.
28	$\overline{PD}$	Power down. Disables all inputs and the oscillator
44 1 43	V_{SS} V_{DD} V_{BATT}	Negative supply voltage Positive supply voltage Connection for battery (negative pole, positive pole of the battery must be connected to V_{DD})
19 20 21	XTAL1 XTAL2 CLKO	Quartz connection (must be open for external clock supply) Quartz connection or external clock supply Clock output
22	$\overline{WDO}$	Oscillator watchdog (open drain output) High indicates that oscillator is in operation
16 17 18	$\overline{WD1}$ $\overline{WD2}$ $\overline{WD3}$	(Open drain output) (Open drain output) (Open drain output) } outputs of the 3 timers
26	TS3	Hardware signal to start timer B
23 24	$\overline{INT1}$ $\overline{INT2}$	(Open drain output, active low) (Open drain output, active low)
25	$\overline{INT3}$	(Open drain output, active low) Outputs that can be controlled via the port, for example, to generate an interrupt at one of the processors.

Functional Description

Dual Port RAM

The dual port RAM has a capacity of 504 bytes, which can be accessed by both processors. The memory locations are selected via a multiplexed address and data bus and two chip select inputs. The $\overline{RD}$ and $\overline{WR}$ inputs define the direction of data transfer. During simultaneous access to the same memory location, no undefined states occur, especially not in such cases, when both processors write to the same memory location. Depending on the internal status of the access control, and of the real physical sequence, the value of one of the ports will be stored. Even during simultaneous reading of and writing to the same memory location, there will be no mixing of data, i.e. either the old data or the new data will be read.

Interrupt Outputs

The dual port RAM has three outputs that can be directly set and reset by writing to an address **(table 1)**. The interrupt outputs are located in the same address range as the scheduling registers. However, only bit 2 and bit 3 are relevant for the interrupt outputs.

In order not to affect the scheduling registers, at least one of the bits 0 or 1 should not be "0". The function of the outputs is shown in the diagram to follow.

RES	Bit 3	Bit 2	Output
1	0	0	no change
1	0	1	1
1	1	0	0
1	1	1	undefined
0	—	—	1

Reset

The reset is necessary to set the DPR control circuits into a defined start state. During a reset, the timer mode registers are loaded with the value $0000XXX0_8$ (for timers 1 and 2), or with $00000XX0_8$ (for timer 3). The $\overline{INT}$ outputs are set to "1".

While the reset input is low, outputs $\overline{WD1}$, $\overline{WD2}$ and $\overline{WD3}$ are set low. After the reset pulse these outputs are high.

A reset is also necessary when the DPR is activated again from the power down mode. The contents of the RAM and the oscillator are not affected by the reset.

Power Down

When the power down pin is activated, all inputs and the oscillator are disabled, so that any levels are allowed at the remaining inputs.

Battery Connection

An external battery can be connected to pin V_{BATT}. The negative pole connects to pin V_{BATT}, the positive pole to V_{DD}. During failure of the normal supply voltage at V_{DD} the RAM will be automatically supplied from the battery so that the RAM contents are saved. All other information is lost. If no battery is used, V_{BATT} must be connected to V_{DD}.

Scheduling Register

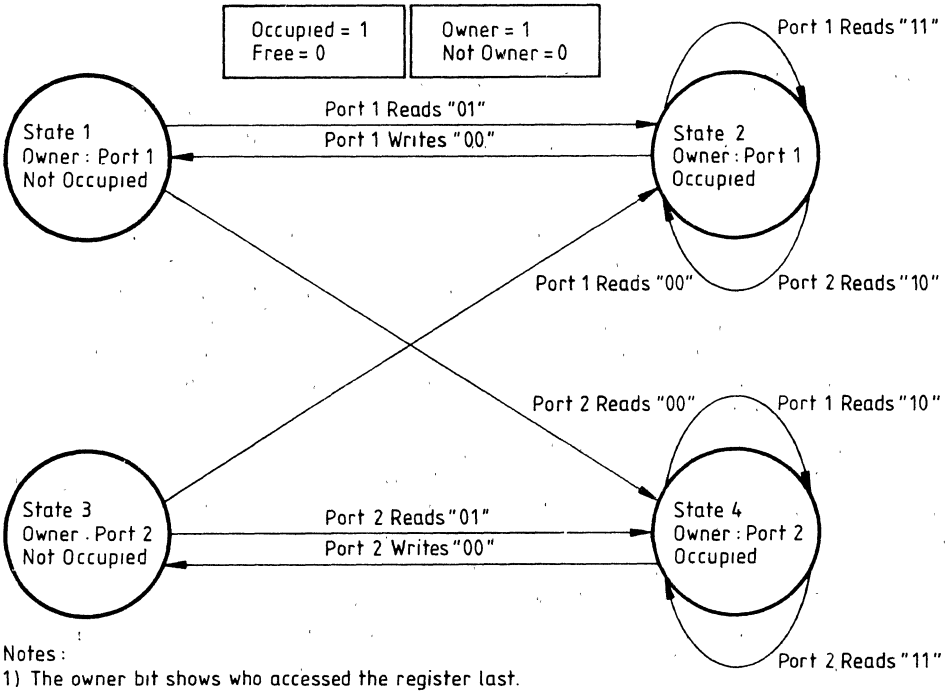
Special circuits within the dual port RAM prevent a mixing of data from the two ports. With continuous data over several bytes, it is possible that old and new data is read at one port if the other port writes to the same memory region at the same time. In order to avoid this conflict, the dual port RAM has 8 scheduling registers. Any of these registers can be used by a processor to indicate that it is accessing a data region assigned to this register. In order to make the operation with these registers as simple as possible, they have special features:

They are 2 bit registers (bit 0, bit 1 of the byte). Bit 0 indicates who "owns" the register and bit 1 indicates that it is occupied. The appropriate bits are already set during a reading of these registers, and the processor receives the correct values **(fig. 1).** Reset is achieved by writing the value "XXXXXX11$_B$". If a read access is attempted from both ports simultaneously, port 1 is given priority and port 2 receives the corresponding message.

The assignment of the scheduling registers to a location in the RAM is done by software. This means, the user is completely flexible in the assignment of the registers. It is, for example, also possible to use these registers as access management for external resources.

The addresses of the scheduling registers are listed in **table 1.** The unused six bits will read all "0".

Status Diagram of the Scheduling Registers



Notes :
1) The owner bit shows who accessed the register last.
2) During simultaneous access, port 1 has priority
3) A write is only possible if the respective port is "owner" of the register.

Figure 1

Oscillator Watchdog

This output provides a means to control the oscillator circuit and the crystal.
Whenever the clock frequency drops below a threshold of approx. 100 kHz, this output switches to low.

Timer

The three timers are 24-bit counters with a clock frequency of $f_{CLK}/6$. Each of the counters can be set by writing to 3 specific RAM addresses. The value is simultaneously stored in the RAM and in a buffer register of the timer. When writing to the low byte, all three bytes are transferred to the reload register. The value in the reload register is maintained in all modes until the corresponding low byte is written again. The counters are down counters. The counters can be started by setting bit 7 in the corresponding TMR. Additionally, counter 3 can be started by an external trigger signal (TS 3). Each counter can be configured by a timer mode register (TMR). The meaning of the bits of the TMR is described below.

Bit 0: Protects the reload register against overwriting.
Application: After writing to the reload register, the parallel RAM region can be used after the timer is started – by writing to the corresponding protection bit – without influencing the reload register (reset state = 0).

Bit 4: Serves to switch output signal polarity (reset state = 0)
Bit 4 = 0; idle state 1, active 0
Bit 4 = 1; idle state 0, active 1

Bit 5: Selects the mode (reset state = 0):
Bit 5 = 0 single shot, i.e. when the counter is started, the output signal goes active. After zero is reached, the output signal returns to idle. To generate another count period, the timer must be started again. During this, the values from the reload register are loaded into the counter.
Bit 5 = 1 auto-reload, i.e. the value of the reload register is loaded into the counter when the counter is started. When reaching zero, the counter outputs a pulse (~4 µs) and reloads the old value automatically, starting the process again, so that a frequency can be adjusted with a 24-bit resolution. If a new start pulse occurs during the counting period (even without "STOP"), no pulse is output and the counter is reloaded.

Bit 6: In the reload mode the timer can be stopped by setting this bit. (During a new start the contents of the counter are lost, but not the contents of the reload register).

Bit 7: Setting this bit starts the counter.

Only for Timer 1 and 2

Bit 1-3: In conjunction with bit 0 serve to switch the watchdog mode on or off.

Only for Timer 3

Bit 1-2: Reserved (must always be 0 for proper operation)

Bit 3: Switches **all 3** timers to test mode, i.e. only the upper 12 bits are used to generate the output signal. (Reset state = 0).

Watchdog Mode

A special mode is provided for timers 1 and 2, which can be used to monitor the two processors that are connected. For this mode, an additional register **(address see table 1)** – referred to as control register (CR) in the following – is used per timer. Watchdog mode is enabled by loading the TMR with the value "$101X1111_B$", bit 4 being used to freely select the polarity of the output signal. This mode operates in a similar manner as the auto-reload mode, except that in this case, neither the contents of the reload register nor the TMR can be changed.

In the watchdog mode the timer can only be restarted (and thus suppressing the output pulse) when first 055_H and then $0AA_H$ is written into the control register. There is no time limit between these two write accesses, however no other value must be written into the timer mode register nor into the control register between these two operations, otherwise the sequence must be started again.

In order to reset the timer into the normal mode, the following sequence must be performed. First the value 055_H must be written into the control register, then the value $011X0000_B$ into the TMR, and finally the value $0AA_H$ into the control register. The same condition applies for this sequence; if any other value is written into one of the two registers, the total operation must be started over again. There is no time limit between the accesses.

The appendix shows the operation of the timer in watchdog mode as an example program for the 8051.

Figure 2: Bit Assignment of the Timer Mode Registers for Timer 1 and Timer 2

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Software start (= 1)	Timer stop (= 1) for auto-reload	Mode (auto-reload = 1 single shot = 0)	Polarity of the output pulse (high = 0)	Only for watchdog mode (normal mode = 0)	Only for watchdog mode (normal mode = 0)	Only for watchdog mode (normal mode = 0)	Protection (=1) write protects the reload register

Figure 3: Bit Assignment of the Timer Mode Register for Timer 3

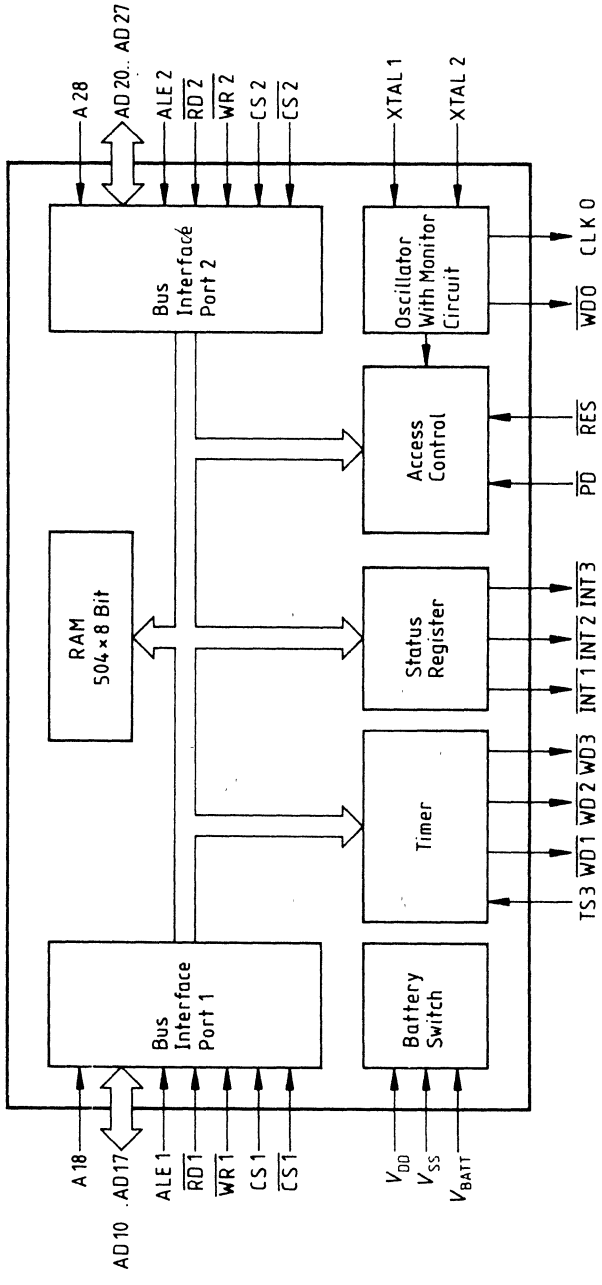
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Software start (= 1)	Timer stop (= 1) for auto-reload	Mode (auto-reload = 1 single shot = 0)	Polarity of the output pulse (high = 0)	Test (= 1) switches timer into test mode	Reserved (normal mode = 0)	Reserved (normal mode = 0)	Protection (=1) write protects the reload register

Address Assignment of the DPR Registers (Preliminary)

Register		Address
Scheduling register	1	$1F8_H$
Scheduling register	2	$1F9_H$
Scheduling register	3	$1FA_H$
Scheduling register	4	$1FB_H$
Scheduling register	5	$1FC_H$
Scheduling register	6	$1FD_H$
Scheduling register	7	$1FE_H$
Scheduling register	8	$1FF_H$
Timer mode register	1	$1E0_H$
Timer mode register	2	$1E4_H$
Timer mode register	3	$1E8_H$
High byte timer	1	$1E3_H$
Medium byte timer	1	$1E2_H$
Low byte timer	1	$1E1_H$
High byte timer	2	$1E7_H$
Medium byte timer	2	$1E6_H$
Low byte timer	2	$1E5_H$
High byte timer	3	$1EB_H$
Medium byte timer	3	$1EA_H$
Low byte timer	3	$1E9_H$
Control register timer	1	$1EC_H$
Control register timer	2	$1ED_H$
Interrupt output	1	$1F8_H$
Interrupt output	2	$1F9_H$
Interrupt output	3	$1FA_H$

Table 1

Block Diagram



Maximum Ratings

$T_A = -40$ to $+85$ °C

		min.	typ.	max.	Unit
Supply voltage	V_{DD}	−0.3		6	V
Input voltage	V_R	−0.3		V_{DD} +0.3	V
Power dissipation per output	P_Q			50	mW
Total power dissipation	P_{tot}			500	mW
Storage temperature	T_{stg}	−50		125	°C

Operating Range

Supply voltage	V_{DD}	4.5	5	5.5	V
Supply current (without output loading)	I_{DD}			20	mA
Operating frequency	f_s			12	MHz
Ambient temperature	T_A	−40		+85	°C
Standby current	I_{DD}, I_{BATT}			1	µA
Data retention voltage	V_{DR}	1			V
Battery voltage (referred to V_{DD}) (with sufficiently low internal impedance)	V_{BATT}	−1		−3	V

9

Maximum Ratings

Maximum ratings are absolute ratings. Exceeding even one of them may result in the destruction of the integrated circuit. All voltages refer to V_{SS}.

Operating Range

Within the operating range the functions mentioned in the circuit description will be fulfilled. Deviations from the characteristics are possible. All voltages refer to V_{SS}.

Characteristics

$T_A = 25\,°C$

		min.	max.	Unit
All input signals				
H input voltage	V_{IH}	2.2	V_{DD}	V
L input voltage	V_{IL}	0	0.8	V
Input capacitance	C_I		10	pF
Input current	I_I		1	µA
Output signals AD10-17, AD20-27				
H output voltage $I_Q = 0.5$ mA	V_{QH}	2.4	V_{DD}	V
L output voltage $I_Q = 1.6$ mA	V_{QL}	V_{SS}	0.4	V
Output signals $\overline{WD1}$, $\overline{WD2}$, $\overline{WD3}$, $\overline{WDO}$ (Open-drain outputs)				
L output voltages $I_Q = 1.6$ mA	V_{QL}	V_{SS}	0.4	V
Output signal CLKO				
H output voltage $I_{QH} = 0.5$ mA	V_{QH}	2.4	V_{DD}	V
L output voltage $I_{QL} = 1.6$ mA	V_{QL}	V_{SS}	0.4	V
Load capacitance	C_L		80	pF

DC Characteristics

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics will apply at $T_A = 25\,°C$ and mean supply voltage. All voltages refer to V_{SS}.

AC Characteristics

$T_A = 25\,°C$

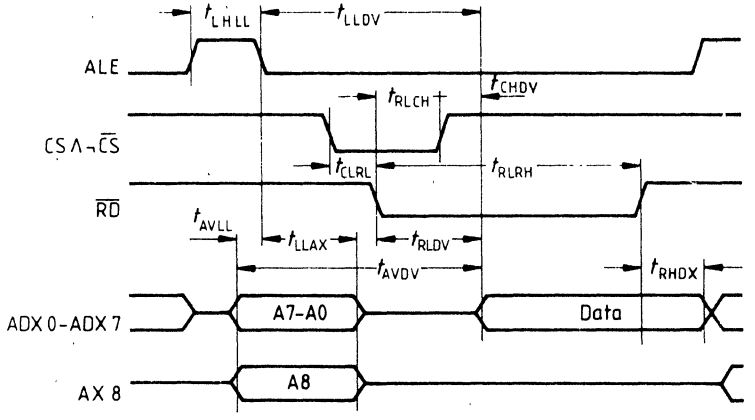
		min.	max.	Unit
ALE pulse width	t_{LHLL}	60		ns
Address setup to ALE low	t_{AVLL}	30		ns
Address hold time after ALE low	t_{LLAX}	40		ns
$\overline{RD}$ pulse width	t_{RLRH}	2 T_{OSC} +20		ns
$\overline{WR}$ pulse width	t_{WLWH}	2 T_{OSC} +20		ns
ALE low to $\overline{RD}$ or $\overline{WR}$ active	t_{LLWL}	60		ns
$\overline{RD}$ active valid data out (chip select active)	t_{RLDV}		2 T_{OSC}	ns
Data hold after $\overline{RD}$ inactive	t_{RHDX}		30	ns
ALE low to valid data out	t_{LLDV}		3 T_{OSC} +20	ns
Valid data in after $\overline{WR}$ low	t_{DVWL}	1/2 T_{OSC}	2 T_{OSC}*)	ns
$\overline{WR}$ low to ALE high	t_{WLLL}	3 T_{OSC}		ns
Data setup before $\overline{WR}$ high	t_{QVWH}	30		ns
Data hold after $\overline{WR}$ high	t_{WHQX}	40		ns
Delay $\overline{RD}$ low to both chip selects active	t_{RLCH}		40	ns
Delay $\overline{WR}$ low to both chip selects active	t_{WLCH}		40	ns
Chip-select setup to $\overline{RD}$	t_{CLRL}	0		ns
Chip-select setup to $\overline{WR}$	t_{CLWL}	0		ns
Active pulse width of timer outputs	t_{ACT}	48 T_{OSC}		ns
Pulse width TS 3	t_{THTL}	2 T_{OSC}		ns
Oscillator pulse width	t_{OSC}	83		ns
High time	t_{OSCH}	25		ns
Low time	t_{OSCL}	25		ns
Rise time	t_r		40	ns
Fall time	t_f		40	ns

The AC characteristics apply throughout the operating range.

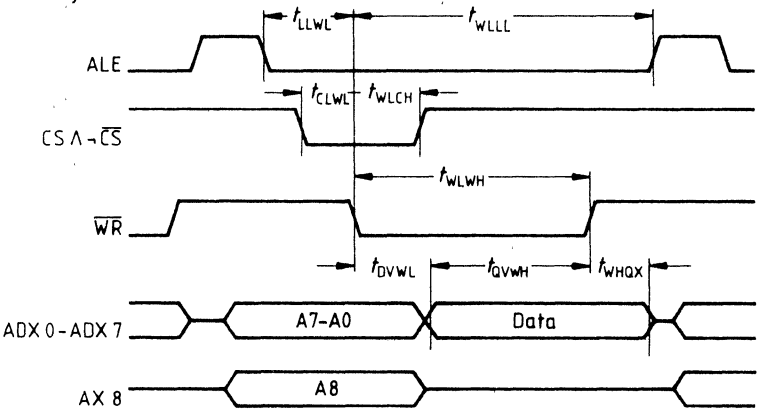
*) Only applies if the $\overline{WR}$ signal is longer than 2 T_{OSC}.
Changes of the data bus signals after this time will have no effect.

Pulse Diagrams

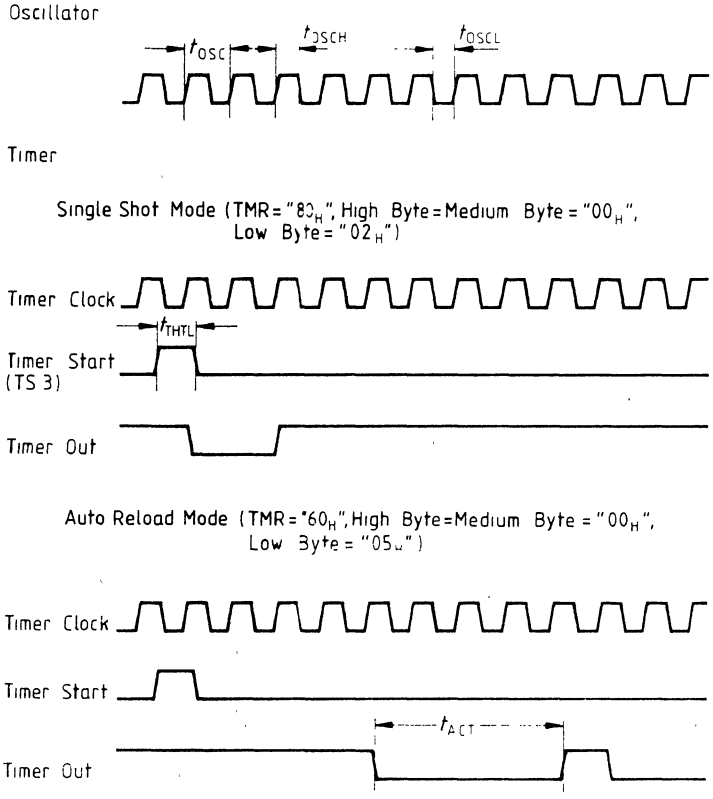
Read Cycle



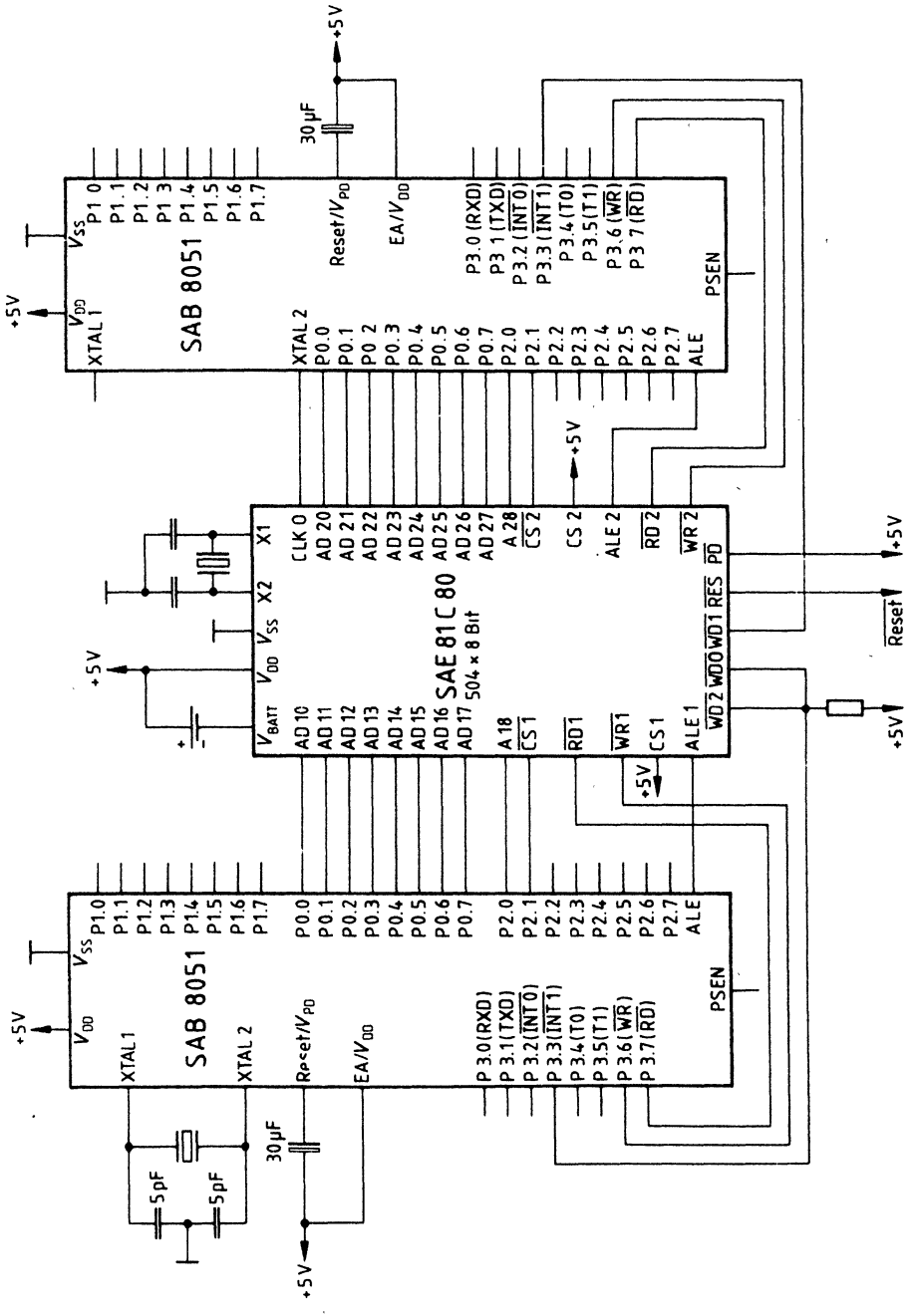
Write Cycle



Pulse Diagram



Application Circuit



8051 – Program for Timer Operation in Watchdog Mode

```
HBYTE   EQU   1E3H    : Address high byte reload register
TMR     EQU   1E0H    : Address timer mode register
KR      EQU   1ECH    : Address control register
REST1   EQU   055H    : 1 value to restart timer
REST2   EQU   0AAH    : 2 value to restart timer
WDAUS   EQU   060H    : Value to switch off watchdog mode

: Load reload register

MOV     DPTR, # HBYTE
CLR     A
MOVX    @ DPTR,A
DEC     DPL
MOV     A, # 0FFH
MOVX    @ DPTR,A
DEC     DPL
MOVX    @ DPTR,A

: Switch on watchdog mode and start timer

MOV     A, # 0AFH
DEC     DPL
MOVX    @ DPTR,A

: Reset timer

MOV     DPTR, # KR
MOV     A, # REST1
MOVX    @ DPTR,A
MOV     A, # REST2
MOVX    @ DPTR,A

: Switch off watchdog mode and stop timer

MOV     DPTR, # KR
MOV     A, # REST1
MOVX    @ DPTR,A
MOV     A, # WDAUS
MOV     DPTR, # TMR
MOVX    @ DPTR,A
MOV     A, # REST2
MOV     DPTR, # KR
MOVX    @ DPTR,A

;

END
```

SIEMENS

SDA 2208-2
IR Remote Control Transmitter with IR Diode Driver

The SDA 2208 is designed as a remote control transmitter for direct driving of infrared transmitter diodes. The instructions are generated by an input matrix (i.e. keyboard) in the form of biphase codes. Distributed over 8 levels, there are a max. of 512 instructions available.

Maximum ratings

Supply voltage range	V_S	−0.3 to 10.5	V
Matrix rows	V_{row}	−0.3 to U_S	V
Matrix columns	V_{col}	−0.3 to U_S	V
Programming pin (PPIN)	V_{PP}	−0.3 to U_S	V
Oscillator input (CLKI)	$V_{i\,OSC}$	−0.3 to 2	V
Infrared output (IRA)			
inhibited	V_q	−0.3 to 10.5	V
in operation	V_q	−0.3 to 8	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\,SA}$	60	K/W

Operating range

Supply voltage	V_S	4 to 10	V
Ambient temperature	T_A	0 to 70	°C
Oscillator frequency	f_{CLK}	430 to 530	kHz

Characteristics

$V_S = 7$ V; $T_A = 25$ °C

		min	typ	max	
Current consumption*)					
transmitting phase	I_S		19		mA
standby mode	I_S		< 1	10	µA
Output current IRA $2\,V < V_2 < 6\,V$	I_2	500	900	1000	mA
Connecting resistance (row-column or column-PPIN)	$R_{row\,col}$			500	Ω

*) Arithmetic mean value incl. transmitter diode

Pin description

Pin	Function
1	GND
2	Output IRA
3	Supply voltage V_S
4	R2
5	R7
6	R1
7	R6
8	R8
9	R4
10	R3
11	R5
12	PPIN
13	CH
14	CE
15	CB
16	CC
17	CG
18	CD
19	CF
20	Oscillator input CLKI

Description of functions

Voltage supply

Voltage consumption ceases in the quiescent state and is activated subsequent to connecting the component's matrix. When the matrix is disconnected, the IC automatically completes the message and returns into the quiescent state.

Clock input

The clock input is equipped with a ceramic resonator. This resonator oscillates with its parallel resonace. In addition, the clock signal can be injected at pin CLK I. The oscillator can be also operated by using an LC circuit with an isolating capacitor.

Input matrix

The matrix is comprised of 8 rows and 8 columns. Column A is used as supply voltage V_S. In order to transmit a message, the respective rows and columns have to be connected. The sender is switched on and a message is output. The length of the message depends on the duration of the matrix connection. A message is comprised of a start instruction, a variable number of information instructions (depending on the duration of the matrix connection) and an end instruction.

Programming via PPIN

The programming pin is used to provide access to all instruction sets or 512 instructions since the 8x8 matrix limits the use to one instruction set or 64 different instructions. By subdividing the instruction sets into 8 levels of 64 instructions each, a specific level can be selected by either keeping the PPIN open or by combining it with one of the seven column inputs (SPB to SPH). When connecting PPIN with one column alone, the standby supply current I_S does not increase.

Safety features against incorrect operation

As a prerequisite for an error-free message output with at least one information instruction, the matrix connection has to be free of interferences and its clock-frequency-dependent, minimal duration should be approx. 60 ms at a clock frequency of 500 kHz. The applied integrated circuit is equipped with a preventive mechanism (key bouncing) against erroneous outputs, which automatically resets the circuit during each detected interference. Equally, operating errors caused by connecting more than one row and one column are detected. The message will be ended through continuous transmitting of end instructions. Operating errors can be cancelled only by disconnecting all matrix connections. The level selection key (PPIN function) will be effective only if it is pressed prior to or simultaneously with the matrix key. Also, a simultaneous pressing of several selection keys has the same effect on the message as an erroneous matrix operation. The protective mechanism becomes effective at $V_S \geq 6\,V$.

Composition of a message

Subsequent to switch-on, the instruction No. 511 (10-bit word length with start bit) is output as start instruction to indicate to the receiver the onset of transmission. Depending on the duration of the matrix connection, a series of identical instructions will follow. If a message is ended by disconnecting the matrix connection, not more than one additional information instruction will be issued to be followed immediately by the end instruction. This end instruction is identical with the start instruction.

Instruction structure

Each instruction consists of a presignal, an infrared pause, a start bit and 9 information bits. During the duration of the presignal (256/fCLK), the receiver performs a simple amplitude adjustment of the input amplifier.

The infrared pause appears between the end of the presignal and the onset of the start bit. Again, the receiver is provided with enough time to recognize transmission distortions based on the limits of the transmission range.

The start bit has been permanently programmed as :1: and is used as synchronization support for the receiver.

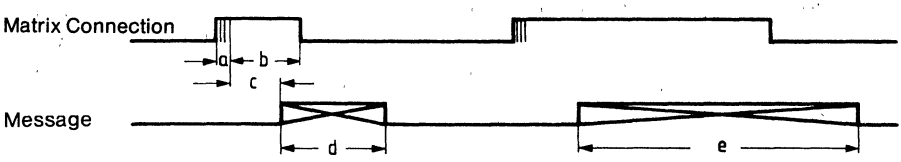
The bit structure has been illustrated in the pulse diagram.

Output driver stage

The fully integrated driver stage enables the direct connection of the infrared transmitter diodes to the infrared output IRA. The diode current is maintained at a constant level within a defined range to stabilize the transmitting power of the infrared diodes.

Pulse diagrams

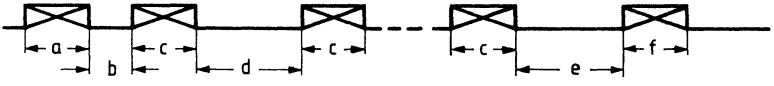
Basic operating process



for 500 kHz
b = 60.928 ms
c = 26.624 ms
d = 177.664 ms

a) bounce
b) minimum key operating time to complete message with one information instruction
c) delay between the on-set of interference-free matrix connection and begin of message transmission
d) message with one information instruction
e) message with several identical information instruction

Composition of message



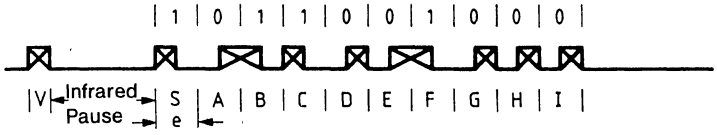
for 500 kHz
a = c = f = 13.312 ms
b = 19.968 ms
d = e = 177.76 ms

a) start instruction 10 bits
b) time interval between start and information instruction
c) information instruction 10 bits
d) time interval between identical information instruction
e) time interval between information and end instruction
f) end instruction 10 bits

The timespan of an interference-free matrix connection determines the number of identical information instructions.

Pulse diagrams

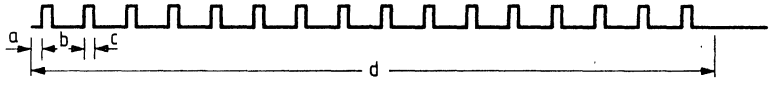
Instruction structure in biphase code



Time duration single bit e: $512/f_{CLK}$
presignal V: $256/f_{CLK}$
infrared pause: $5x256/f_{CLK}$

start bit S is always 1
bits A to I are addressable

Structure of the modulated half bit (as well as the presignal)



$a = c = 4/f_{CLK}$
$b = 16/f_{CLK}$
$d = 256/f_{CLK}$
16 pulses per half bit

The H signal indicates a constant current source at Q_{IRA}. The infrared transmitter diode is then active.

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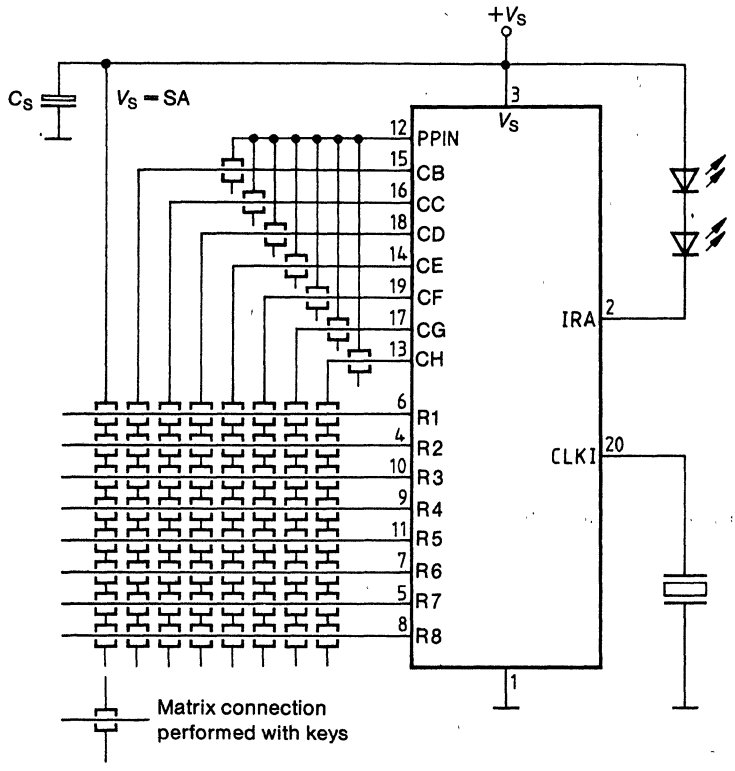
Block diagram



Since the infrared transmitter diodes have to be driven with pulse currents of approx. 1 A, the following has to be complied with during the layout of the PC board:

1) The smoothing capacitor between V_S and ground should be located as closely as possible to the pins of the IC.
2) The supply line to the transmitter diodes is not to cause cross-talk in the key matrix.
3) No residual currents are to flow over the connection ceramic oscillator/ground pin.

Truth table

No. of the instruction	Matrix connection row–column	Binary code IRA information instruction A B C D E F G H I
0	1A	0 0 0 0 0 0 0 0 0
1	1B	1 0 0 0 0 0 0 0 0
2	1C	0 1 0 0 0 0 0 0 0
3	1D	1 1 0 0 0 0 0 0 0
4	1E	0 0 1 0 0 0 0 0 0
5	1F	1 0 1 0 0 0 0 0 0
6	1G	0 1 1 0 0 0 0 0 0
7	1H	1 1 1 0 0 0 0 0 0
8	2A	0 0 0 1 0 0 0 0 0
9	2B	1 0 0 1 0 0 0 0 0
10	2C	0 1 0 1 0 0 0 0 0
11	2D	1 1 0 1 0 0 0 0 0
12	2E	0 0 1 1 0 0 0 0 0
13	2F	1 0 1 1 0 0 0 0 0
14	2G	0 1 1 1 0 0 0 0 0
15	2H	1 1 1 1 0 0 0 0 0
16	3A	0 0 0 0 1 0 0 0 0
17	3B	1 0 0 0 1 0 0 0 0
18	3C	0 1 0 0 1 0 0 0 0
19	3D	1 1 0 0 1 0 0 0 0
20	3E	0 0 1 0 1 0 0 0 0
21	3F	1 0 1 0 1 0 0 0 0
22	3G	0 1 1 0 1 0 0 0 0
23	3H	1 1 1 0 1 0 0 0 0
24	4A	0 0 0 1 1 0 0 0 0
25	4B	1 0 0 1 1 0 0 0 0
26	4C	0 1 0 1 1 0 0 0 0
27	4D	1 1 0 1 1 0 0 0 0
28	4E	0 0 1 1 1 0 0 0 0
29	4F	1 0 1 1 1 0 0 0 0
30	4G	0 1 1 1 1 0 0 0 0
31	4H	1 1 1 1 1 0 0 0 0
32	5A	0 0 0 0 0 1 0 0 0
33	5B	1 0 0 0 0 1 0 0 0
34	5C	0 1 0 0 0 1 0 0 0
35	5D	1 1 0 0 0 1 0 0 0
36	5E	0 0 1 0 0 1 0 0 0
37	5F	1 0 1 0 0 1 0 0 0
38	5G	0 1 1 0 0 1 0 0 0
39	5H	1 1 1 0 0 1 0 0 0
40	6A	0 0 0 1 0 1 0 0 0

Truth table (cont'd)

No. of the instruction	Matrix connection row – column	Binary code IRA information instruction A B C D E F G H I
41	6B	1 0 0 1 0 1 0 0 0
42	6C	0 1 0 1 0 1 0 0 0
43	6D	1 1 0 1 0 1 0 0 0
44	6E	0 0 1 1 0 1 0 0 0
45	6F	1 0 1 1 0 1 0 0 0
46	6G	0 1 1 1 0 1 0 0 0
47	6H	1 1 1 1 0 1 0 0 0
48	7A	0 0 0 0 1 1 0 0 0
49	7B	1 0 0 0 1 1 0 0 0
50	7C	0 1 0 0 1 1 0 0 0
51	7D	1 1 0 0 1 1 0 0 0
52	7E	0 0 1 0 1 1 0 0 0
53	7F	1 0 1 0 1 1 0 0 0
54	7G	0 1 1 0 1 1 0 0 0
55	7H	1 1 1 0 1 1 0 0 0
56	8A	0 0 0 1 1 1 0 0 0
57	8B	1 0 0 1 1 1 0 0 0
58	8C	0 1 0 1 1 1 0 0 0
59	8D	1 1 0 1 1 1 0 0 0
60	8E	0 0 1 1 1 1 0 0 0
61	8F	1 0 1 1 1 1 0 0 0
62	8G	0 1 1 1 1 1 0 0 0
63	8H	1 1 1 1 1 1 0 0 0

	G	H	I
Instruction 0 to 63: PPIN free	0	0	0
Instruction 64 to 127: PPIN connected with CB	1	0	0
Instruction 128 to 191: PPIN connected with CC	0	1	0
Instruction 192 to 255: PPIN connected with CD	1	1	0
Instruction 256 to 319: PPIN connected with CE	0	0	1
Instruction 320 to 383: PPIN connected with CF	1	0	1
Instruction 384 to 447: PPIN connected with CG	0	1	1
Instruction 448 to 511: PPIN connected with CH	1	1	1

In every instruction set, the assignment instruction – matrix connection (row – column) is analogous to the group 0 to 63.

Example:

Instruction 64 is generated, when PPIN is connected with CB, and R1 with CA.

SIEMENS

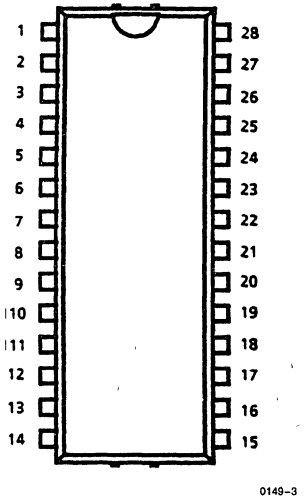
Preliminary

SDA 3208
Infrared Transmitter

- CMOS-Silicon Gate Technology
- Supply Voltage 3.0V–5.5V
- Standby Current < 1 μA
- Number of Commands: 25600 Commands Distributed over 8 System Levels with 16 Addresses Each and 200 Commands per Address
- High Transmit Reliability Due to Bi-Phase Encoding
- On-Chip Key Debouncing Circuitry
- Protection against Erroneous Operation
- Two Separate Outputs for Modulated and Unmodulated Signals
- Single Pin Oscillator for Connecting a Ceramic Resonator or LC Resonant Circuitry

Pin Configuration

Top View



0149–3

Pin Definitions

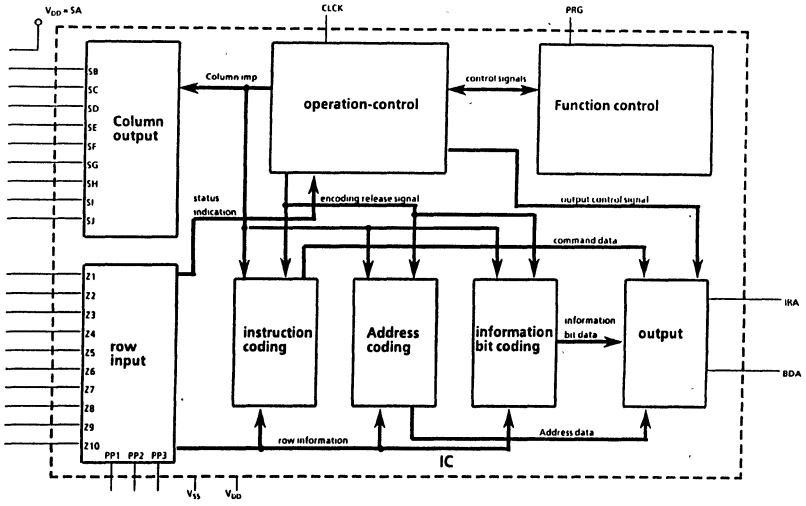
Pin	Symbol	Function
1	SPD	Column Outputs
2	SPE	
3	SPF	
4	SPG	
5	SPH	
6	SPI	
7	SPJ	
8	Z10	Row Inputs for Command Matrix
9	Z9	
10	Z8	
11	Z7	
12	Z6	
13	Z5	
14	Z4	
15	Z3	
16	Z2	
17	Z1	
18	PP3	Row Inputs for Address Coding Matrix
19	PP2	
20	PP1	Row Inputs for Indentification Bit Matrix
21	U_{DD}	Positive Voltage Supply as well SPA Oscillator
22	CLCK	Input/Output
23	BDA	Unmodulated Data Output
24	IRA	Modulated Data Output
25	U_{SS}	Negative Voltage Supply
26	PRG	Programming Pin
27	SPB	Column Outputs
28	SPC	

The integrated circuit has been designed as remote-controlled transmitter using bi-phase encoding and an on-chip driver circuitry.

An additional output transmits the command encoding without carrier signals for e.g. direct transmission to a line. The command information is established via a 10 x 13 input matrix. In addition to four freely-selectable identification bits (SH, S1–S3), a maximum of 14 different addresses with 100 commands each are possible. Two different operating modes can be selected via a programming input.

9

Block Diagram



Circuit Description

Supply Voltage

The current consumption of the component is <1 μA during the quiescent state. The circuit is activated and transmits a telegram according to the keyboard matrix input signal and the programming pin configuration.

Clock Input

A ceramic resonator has been connected to the clock input. The ceramic resonator oscillates at its parallel resonance. In addition, a clock signal present at PIN CLCK can be injected via a coupling capacitor. The oscillator can also be operated with an LC circuit, a serial capacitor, or dc decoupling.

Programming via PRG

Since the IC is normally operated via the input-matrix only, the programming mode should be considered as means to define the basic operating mode of the transmitter.

There are two possibilities:

1. Input PRG strapped to LOW

   This configuration represents the standard operating mode. In order to transmit a telegram, the address as well as a command key should be activated. As an alternative, the address can be hard-wired via a switch. The command key must be depressed to enable the address matrix. The circuit takes on current and the key debounce function goes into effect for the matrix keys of the address and command matrix.

2. Input PRG strapped to HIGH

   This configuration is defined as latch mode. In this case, a telegram is transmitted by simply activating one of the matrix keys. When depressing an address key, the circuitry transmits the requested address together with the command code 255 (according to the shift key depressed in the identification bit matrix). The two command codes cannot be set via the command matrix. The requested address is also stored in the circuitry. When the command keys are subsequently depressed, the command codes are always transmitted together with the internally stored address. The address can be changed by depressing a new address key. No telegram is transmitted when the address and command key are simultaneously depressed. However, since the matrix fields are activated, the quiescent current increases.

Command Matrix

This matrix comprises 10 rows (Z1–Z10) and 10 columns (SA–SJ), whereby SA = V_{DD}. The matrix operating mode is valid when a row is connected to a column. 100 different command codes can be realized. The length of a telegram depends on the duration of a valid matrix connection. The telegram com-

prises a start command, a varying number of information commands (depending on the duration of the matrix connection) and an end command.

Address Coding Matrix

The 8 x 2 address coding matrix comprises columns A through H and program rows PP1 and PP2. The 4 address bits G–7J are programmed via this address coding matrix. In the standard mode (PRG = LOW), the rows and columns of the address coding matrix can be permanently connected (without increasing the standby current), since an additional command matrix key has to be depressed to activate the transmitter.

Identification Bit Matrix

The 4 point matrix comprises 4 columns SG–SI and the programming row PP3. Both, the single or multiple operating mode for this matrix directly effect the 4 allocated command bits S1–S3 and SH.

Protection Against Erroneous Operation

In order to prevent accidental telegrams, the circuitry includes the following lock-out features:

1. To avoid the use of expensive bounce-free matrix keys, a debouncing circuitry was integrated which resets the internal sequence control within the first 18 ms (for f_{CL} = 500 kHz) in the case of faulty matrix connections. Command encoding is therefore only performed after satisfactory row-column connections.
2. Simultaneous multiple operations in the command or address coding matrix are recognized as erroneous operations. The end command is output continuously until all keys contributing to the erroneous operation are released. However, multiple operations can be executed in the identification bit matrix without resulting in an erroneous operating status, if the columns have been decoupled by means of diodes.
3. In the standard operating mode (PRG = LOW), a telegram is transmitted only when establishing connection in both the command and the address coding matrix.

   The telegram is not transmitted by just activating the command matrix, although the standby current increases noticeably.

Telegram Structure

After switch-on, the start command is output (address 15, command 254, all identification bits + 1) to indicate the beginning of information transfer to the receiver. The command output is followed by a number of identical information commands, the number of which depends on the duration of the matrix connection. If a telegram is ended by terminating the matrix connection, a maximum of 1 additional information command will output followed by an end command. The end command is identical to the start command.

Command Structure

Each command comprises a pilot signal, an infrared interval, 1 start bit, 7 command bits, 1 shift bit, 4 address bits, and 3 freely-selectable identification bits (the shift bit is part of the 4 freely-selectable bits of the identification bit matrix).

The pilot has a duration of $256/f_{CL}$ and allows for easy control of the input amplifier level in the receiver section. The infrared interval lies between the end of the pilot signal and the beginning of the start bit and enables the receiver to recognize interferences when reaching the limit of the transmission range. The start bit is permanently set to log. "1" and functions as synchronization support for the receiver. The bit structure is shown in the pulse diagram.

Output Stages

The control signal for an IR driver stage (with pnp driver transistor) is present at output IRA. The signal is modulated with the frequency $f_{CLK/128}$ and the pulse duty factor 1:4.

The unmodulated binary signal (envelope) is supplied at the second output BDA for e.g. direct transmission to a line (quiescent level is HIGH).

Absolute Maximum Ratings*

Maximum ratings cannot be exceeded without causing irreversible damage to the integrated circuit.

Maximum Rating for T_A = 25°C

Pos	Parameter	Symbol	Limits		Units
			Min	Max	
1	Storage Temperature	T_S	−50	+125	°C
2	Total Power Dissipation	P_{tot}		500	mW
3	Power Dissipation per Output	P_Q		50	mW
4	Input Voltage	V_{IN}	−0.3	V_{DD} + 0.3	V
5	Supply Voltage	V_{DD}	−0.3	6	V

Functional Range

Within the functional range, the integrated circuit operates as described; deviations from the characteristic data are possible.

Pos	Parameter	Symbol	Limits		Units
			Min	Max	
1	Supply Voltage	V_{DD}	3.0	5.5	V
2	Operating Frequency	f_{CL}	160	560	KHz
3	Operating Temperature	T_A		70	°C

Characteristics

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not stated otherwise, typical characteristics will apply at T_A = 25°C and the listed supply voltage.

Pos	Parameter	Symbol	Conditions	Limits			Units
				Min	Typ	Max	
1	Current Consumption without IR Output Stage	I_{DDB}			1.5	10	mA
2	Leakage Current in Standby Mode	I_{DDS}		0	1	1	µA
3	Output Current at IRA	I_{QL} I_{QH}	$V_{QL} = V_{DD} - 1V$ $V_{QH} = V_{DD} - 0.5V$	4 200	6 1000		mA µA
4	Output Current at BDA	I_{QL} I_{QH}	$V_{QL} = 0.5V$ $V_{QH} = V_{DD} - 0.5V$	1 1	6 4		mA mA
5	Connection Resistance Row-Column or Column-PRG	R_C		0		1000	Ω(1)
6	Load Capacitance of Row and Column Pins (Z1–10, SA–SJ, PP1/2, PRG)	C_L		0		20	pF

Note:

1. When applying the muptiple operating mode in the identification bit matrix, the columns involved should be decoupled by diodes to prevent error recognition. The anodes should be tied to PP3.

Code-Table for the Command Bit

Row	Column	Bit ABCDEFX	Command No.	Row	Column	Bit ABCDEFX	Command No.
1	A	0000000	0	6	A	0001010	40
1	B	1000000	1	6	B	1001010	41
1	C	0100000	2	6	C	0101010	42
1	D	1100000	3	6	D	1101010	43
1	E	0010000	4	6	E	0011010	44
1	F	1010000	5	6	F	1011010	45
1	G	0110000	6	6	G	0111010	46
1	H	1110000	7	6	H	1111010	47
1	I	0000101	80	6	I	0101101	90
1	J	1000101	81	6	J	1101101	91
2	A	0001000	8	7	A	0000110	48
2	B	1001000	9	7	B	1000110	49
2	C	0101000	10	7	C	0100110	50
2	D	1101000	11	7	D	1100110	51
2	E	0011000	12	7	E	0010110	52
2	F	1011000	13	7	F	1010110	53
2	G	0111000	14	7	G	0110110	54
2	H	1111000	15	7	H	1110110	55
2	I	0100101	82	7	I	0011101	92
2	J	1100101	83	7	J	1011101	93
3	A	0000100	16	8	A	0001110	56
3	B	1000100	17	8	B	1001110	57
3	C	0100100	18	8	C	0101110	58
3	D	1100100	19	8	D	1101110	59
3	E	0010100	20	8	E	0011110	60
3	F	1010100	21	8	F	1011110	61
3	G	0110100	22	8	G	0111110	62
3	H	1110100	23	8	H	1111110	63
3	I	0010101	84	8	I	0111101	94
3	J	1010101	85	8	J	1111101	95
4	A	0001100	24	9	A	0000001	64
4	B	1001100	25	9	B	1000001	65
4	C	0101100	26	9	C	0100001	66
4	D	1101100	27	9	D	1100001	67
4	E	0011100	28	9	E	0010001	68
4	F	1011100	29	9	F	1010001	69
4	G	0111100	30	9	G	0110001	70
4	H	1111100	31	9	H	1110001	71
4	I	0110101	86	9	I	0000011	96
4	J	1110101	87	9	J	1000011	97
5	A	0000010	32	10	A	0001001	72
5	B	1000010	33	10	B	1001001	73
5	C	0100010	34	10	C	0101001	74
5	D	1100010	35	10	D	1101001	75
5	E	0010010	36	10	E	0011001	76
5	F	1010010	37	10	F	1011001	77
5	G	0110010	38	10	G	0111001	78
5	H	1110010	39	10	H	1111001	79
5	I	0001101	88	10	I	0100011	98
5	J	1001101	89	10	J	1100011	99

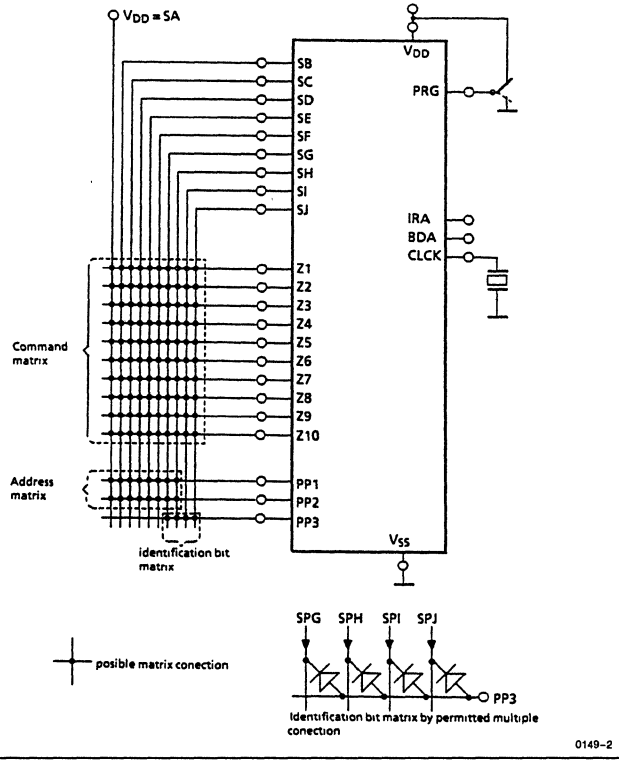
Code-Table for the Address Bit

Connection		Bit Output			
Row	Column	G	H	I	J
PP1	A	0	0	0	0
PP1	B	1	0	0	0
PP1	C	0	1	0	0
PP1	D	1	1	0	0
PP1	E	0	0	1	0
PP1	F	1	0	1	0
PP1	G	0	1	1	0
PP1	H	1	1	1	0
PP2	A	0	0	0	1
PP2	B	1	0	0	1
PP2	C	0	1	0	1
PP2	D	1	1	0	1
PP2	E	0	0	1	1
PP2	F	1	0	1	1
PP2	G	0	1	1	1
PP2	H	1	1	1	1

Code-Table for the Identification Bit (S1–S3, SH) (by Permitted Multiple Operation)

Connection				Output			
PP3-SPG	PP3-SPH	PP3-SPI	PP3-SPJ	S1	S2	S3	SH
0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0
0	1	0	0	0	1	0	0
1	1	0	0	1	1	0	0
0	0	1	0	0	0	1	0
1	0	1	0	1	0	1	0
0	1	1	0	0	1	1	0
1	1	1	0	1	1	1	0
0	0	0	1	0	0	0	1
1	0	0	1	1	0	0	1
0	1	0	1	0	1	0	1
1	1	0	1	1	1	0	1
0	0	1	1	0	0	1	1
1	0	1	1	1	0	1	1
0	1	1	1	0	1	1	1
1	1	1	1	1	1	1	1

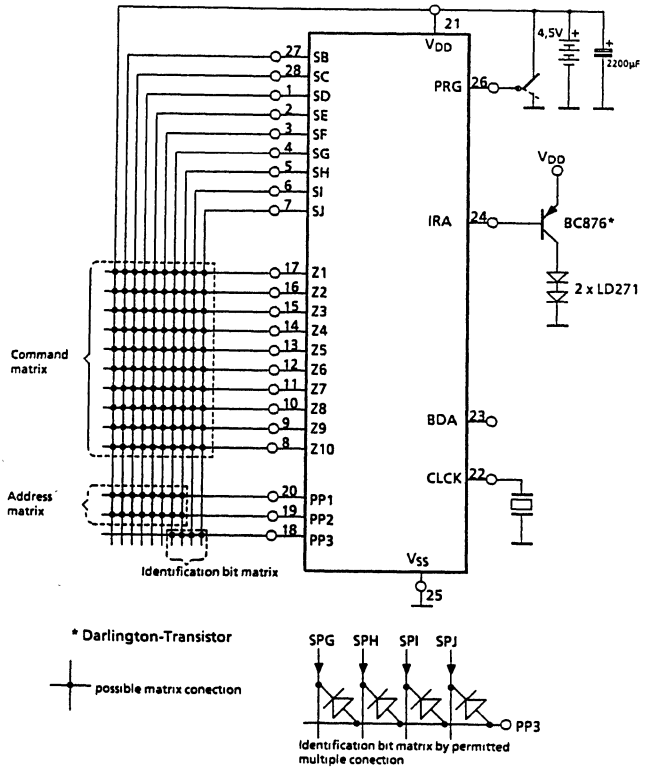
Application Diagram



Pin Description

Symbol	Description
V_{SS}	Ground
V_{DD}	Positive supply voltage as well as column SA
SPB to SPJ	Column outputs for command, address coding, and identification bit matrix
Z1 to Z10	Row inputs for command matrix
PP1 and PP2	Row inputs for address coding matrix
PP3	Row inputs for identification bit matrix
PRG	Programming pin for selecting the latch mode (PRG = High) or standard mode (PRG = Low)
CLCK	Oscillator input/output for connecting a ceramic resonator or injecting an external clock
BDA	Data output; the binary signal (envelope) of the telegram is present at the output without a 30 kHz carrier (the transmit diodes are **destroyed** when the output is connected to the IR output stage).
IRA	Output for driving an IR output stage with a pnp driver transistor

Measurement Circuit



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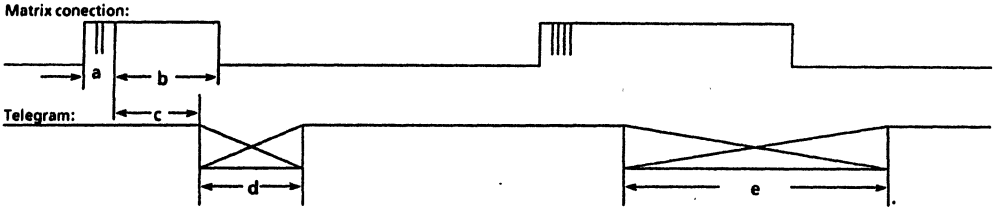
Basic Operating Sequence

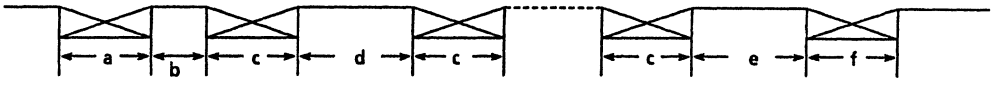


0149-5

Times for:
f_{CL} = 500 kHz
b ≈ 62 ms
c ≈ 19 ms
d ≈ 180 ms

a) Key bouncing
b) Minimum time key must be depressed to complete telegram with one information command
c) Satisfactory matrix connection required for transmitting a telegram
d) Telegram with one information command
e) Telegram with several identical information commands

Telegram Structure



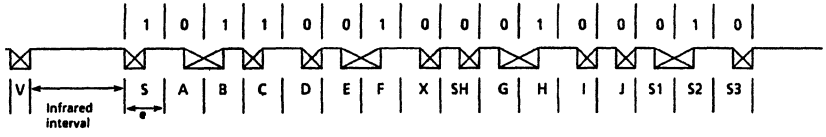
0149-6

Times for:
f_{CL} = 500 kHz
a = c = f ≈ 19.5 ms
b ≈ 14 ms
d = e ≈ 110 ms

a) Start command 16-Bit
b) Time interval between start and information command
c) Information command 16-Bit
d) Time interval between information command/information command
e) Time interval between information command and end command
f) End command 16-Bit

The number of identical information commands depends on the duration of the interference-free matrix connection.

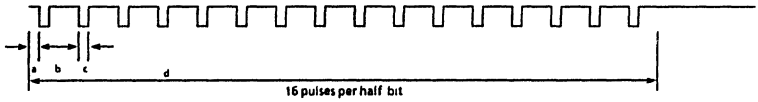
Command Structure in Bi-Phase Code (Example is Based on an Information Command)



0149-7

Time Duration:
Single Bit e: $512/f_{CLK}$
Pilot Signal V: $256/f_{CLK}$
Infrared Interval: $5 \times 256/f_{CLK}$

Structure of Modulated Half Bit (as Well as Pilot Signal)



0149-8

a = c = $4/f_{CLK}$
b = $16/f_{CLK}$
d = $256/f_{CLK}$
L—Signal indicates a current source at IRA

Ordering Information

Type	Order Number	Package
SDA 3208	Q67100-A8095	DIP 28

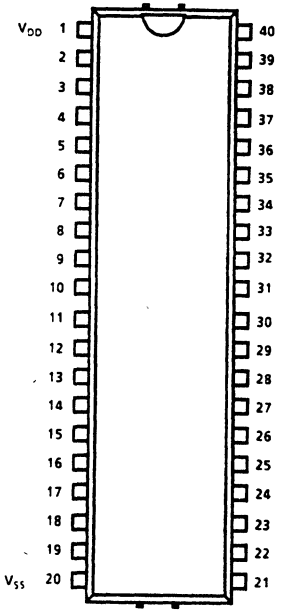
9

Preliminary

SLE 5001, SLE 5002
Universal IR Locking System

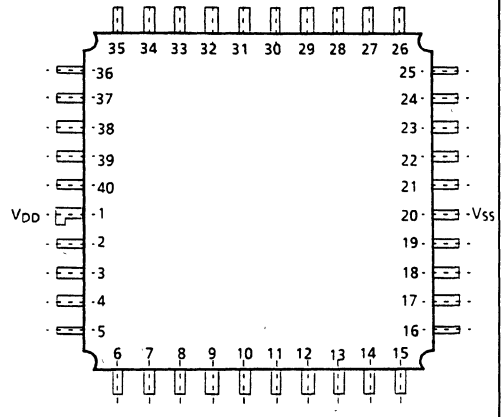
Pin Configuration

DIP 40 Package



0153-2

Micropack Package



0153-3

The CMOS components SLE 5001 and SLE 5002 are designed as transmitter and receiver for a universally applicable locking system. This system has been developed to minimize external components, offer maximum security and provide high user comfort.

By using a micropack package for the transmitter, it is possible to reduce its dimensions to the size of mechanical keys.

The data from the transmitter to the receiver is transferred by means of infrared light. Depending on the hardware periphery, the data can also be transferred via RF or ultrasound.

By pressing a key for a short time (approximately 100 μs) the door locking system is triggered on or off. For application in vehicles as remote controlled central power locking systems the following additional features are possible:

Control of glove compartment, sun roof, windows, trunk and driver seat as well as rear mirror position.

The information flow from the transmitter to the receiver is based on a code scrambling technique. When synchronized,this method offers the user a high level of security.

Description of System

Depending on the configuration of several optional inputs and the peripheral hardware of the SLE 5001/5002, the following operating modes are available.

— Locking system with uni-directional synchronization and hardwired matrix as basic code memory

— Locking system with uni-directional synchronization and E²PROM SDE 2506 as basic code memory

— Locking system with dialog synchronization and hardwired matrix as basic code memory

— Locking system with dialog synchronization and E²PROM SDE 2506 as basic code memory

Code Replacement

A new code is used for each opening/locking process. After receiving a valid code, the lock is automatically set to the next code to be transmitted by the key. As a result, the code received a moment ago by the lock causes all previous codes to become ineffective, including secretly recorded codes.

The code sequence differs for each key/lock combination. The code sequence is mathematically derived from a number, characteristic for the combination in question, that is, from a "basic code". In principle, this method corresponds to the configuration of key notches and tumblers in mechanical systems. The "basic code" is stored in a hardwired matrix or in a non-volatile E²PROM.

Programming of the "Basic Code" and "Key Number"

a) With a Hardwired Matrix

Each matrix, both in the transmitter and receiver, must have the same knots. Minimum is one knot. Each matrix input may have only one knot (electrical connection).

b) With EEPROM SDE 2506

For programming the EEPROM a programming device is necessary for sending the data and the cycle. With this device it is possible to program the EEPROM. A description of this device is available.

In addition, a sample and hold range "N" = 9 has been defined to the effect that the lock does not only accept the actual code but also a number "N" of successively transmitted codes. This means that 8 successive codes can be transmitted without influencing synchronization. The synchronization established between a lock and each key fitting this lock must be ensured independent of all other invalid keys which fit the lock. Five different keys for one lock are possible. To this end, the status of the code sequence of each key fitting the lock is stored in the lock. Each key has been assigned with a number which is transmitted together with the code.

Depending on the hardware periphery and the level of security required, there are two possibilities of recovering lost synchronization. For both methods synchronization is initiated by depressing the transmit key for approximately 5 seconds. During this time 9 pulses are sent out at the output "Monitor-LED".

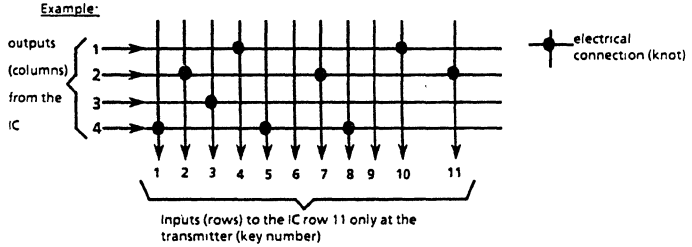
a) Uni-Directional Method

This method uses the "basic code" as the only fixed common characteristic for the lock/key combination. Synchronization is reestablished by deriving a "reset code" from the basic code. However, in view of secret recording (electronic wax impression) this method is not without risk since the reset code forms a sequence with the next code which opens the lock.

b) Dialog Method

This type of synchronization provides the user with a high level of security. However, an additional transmitter/receiver is required. Although their low output power requires the user to move closer to the lock,

Example:



this inconvenience is alleviated by the fact that this type of synchronization is rarely necessary (e.g., when changing batteries).

Synchronization Process

Initially, the key should be located close to the lock (several cm). The dialog begins when the key transmits an initiation code to the lock. The lock acknowledges the code with a random number which is linked to the basic code in the lock and key. The key transmits the resulting identification number to the lock where the number is compared to the one computed by the lock. If the two numbers correspond, the lock is activated, reestablishing synchronization.

Since the key has to accurately acknowledge the particular random number transmitted at that moment by the lock, it cannot be activated by secretly recorded dialogs. It can be seen, the dialog method constitutes a high level of security which cannot be attained with the uni-directional method. Anyone attempting to misuse the opening/locking system is faced with the difficulty of solving the "basic code" and an unknown, complicated mathematical law.

Transmitter (Key)

The basic version of the transmitter comprises the SLE 5001, a basic code memory and an IR transmit stage with the IR transmitter diode SFH 484.

An additional IR receiver (with limited output power) is required for dialog synchronization. For monitoring the function 3 pulses are sent out on the output "Monitor-LED".

Receiver (Lock)

The receiver comprises the SLE 5002, the IR preamplifier TDE 4061 and a low-power IR receiver for dialog synchronization.

The basic code is stored in either a hardwired matrix or in the E²PROM SDE 2506.

Following outputs (active low) are available:

1 × Close 1 × Open 5 × Key No. (1, 2, 3, 4, 5)	Duration Approx. 1.2 seconds
1 × Trigger Pulse	Duration: 20 ms, Delay: 20 ms

1 × Error Indicator (Blink Signal):

a) Data line low (short circuit against ground); intermitted 4 blink signals with 0.5 seconds duration and 4 seconds break.

b) More than one knot in a hardwired matrix input of the receiver occurs a constant blink signal with a break of 1 second.

c) More than one knot in a hardwired matrix input of the transmitter occurs a constant signal 4 periods long like a).

Description of the Data Transfer

(Figure 2)

One full IR transmit cycle comprises 4 bytes and 4 synchronization pulses. Each byte is preceded by a synchronization pulse. The transmitted byte is stored during the delay time (1.5 ms) following each byte transfer. The individual data bits are modulated with a carrier frequency of 125 kHz and transmitted as infrared light pulses by a transmit diode (SFH 484). Each data bit consists of 12 IR pulses of 2.4 µs duration and has a peak current of approximately 2A. Since the next bit will be transmitted after approximately 1.5 ms, the resulting maximum peak current is approximately 38 mA (12 × 2.4 µs/1500 µs) × 2000 mA. The bit transmission is ended with a logic "0". Under worst case conditions (all bits "1") a battery of 2 mA (12 × 2.4 µs × 2000 mA × 36) is required for transmitting a 4 byte data word.

The infrared pulses emitted by the transmit diode are converted into current pulses by the IR receive diode SFH 205. The IR pre-amplifier amplifies and demodulates the received signal. Figure 3 shows a possible discrete solution for this purpose.

However the application of the TDE 4061 provides the highest level of integration. The demodulator is integrated, and the TDE 4061 can be connected directly to the receiver SLE 5002.

The processed data word is forwarded to the receiver in the lock and compared to the valid code in the sample and hold (9) range. If the data word and the stored code correspond, the lock is either open end or locked.

Absolute Maximum Ratings*

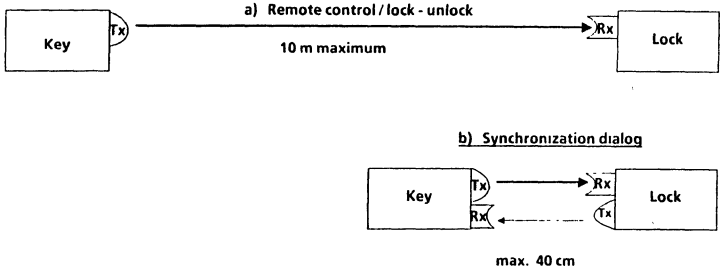
Ambient Temperature ..... −40°C to +85°C
Storage Temperature ..... −55°C to +125°C
Supply Voltage V_{DD} ..... 0V to +7V
Power Consumption 1W
Input/Output Voltages ..... −0.8V to V_{DD} +0.8V

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Operating Specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage	V_{DD}	V_{SS} = 0V, 2.5V to 6V				
Current Consumption	I_{DD}	3 MHz, 5V 1 MHz, 5V 500 kHz, 5V $V_{SS} \le V_{IL} \le 0.4V$ $4.8V \le V_{IH} \le V_{DD}$	3.1 0.7	1.4	3.75 0.9	mA mA mA
Standby	I_{DDS}	V_{DD} = 5V $V_{SS} \le V_{IL} \le 0.4V$ $4.8V \le V_{IH} \le V_{DD}$		1	2	µA
Input Level Low	V_{IL}		−0.5		0.75	V
Input Level High	V_{IH}		$0.7 \times V_{DD}$		V_{DD} + 0.5	V
Output Level Low	V_{OL}	I_{OL} = 1.0 mA			0.45	V
Output Level High	V_{OH}	I_{OH} = −1.0 mA	$0.75 \times V_{DD}$			V

Infrared Code Transmission

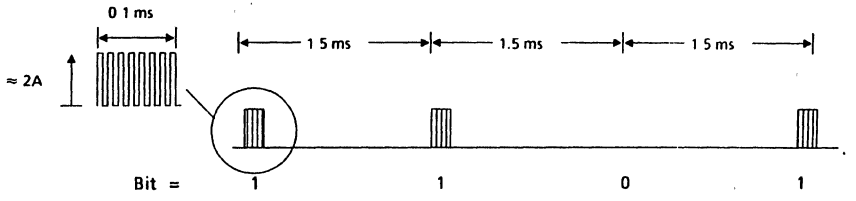


a) Remote Control for Lock (Locking & Unlocking)
b) Dialog for Synchronization of Remote Control

Figure 1

Data Frame

Single IR-Transmit Pulse



Complete IR-Transmission (4 Bytes)

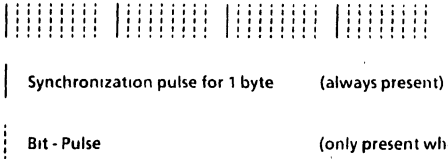


Figure 2

Discrete IR Pre-Amplifier Application

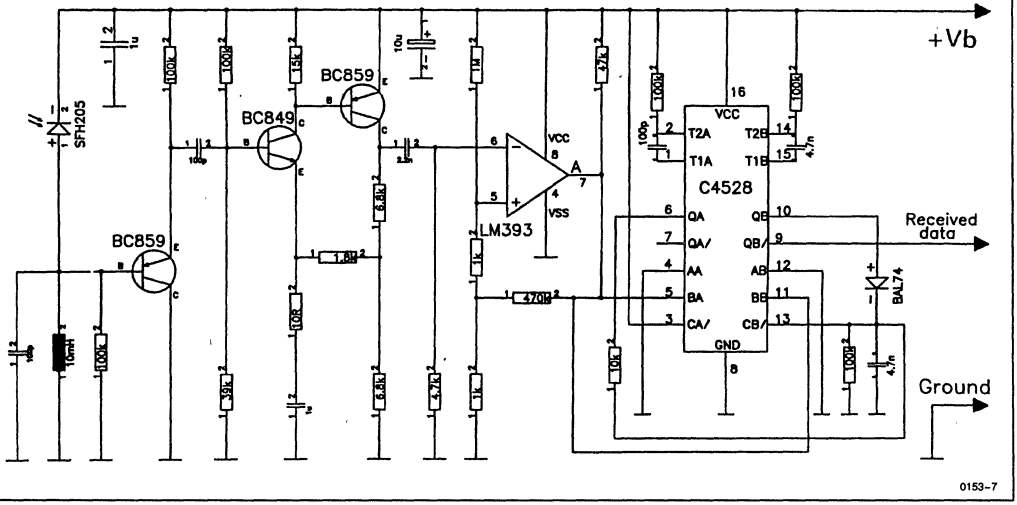
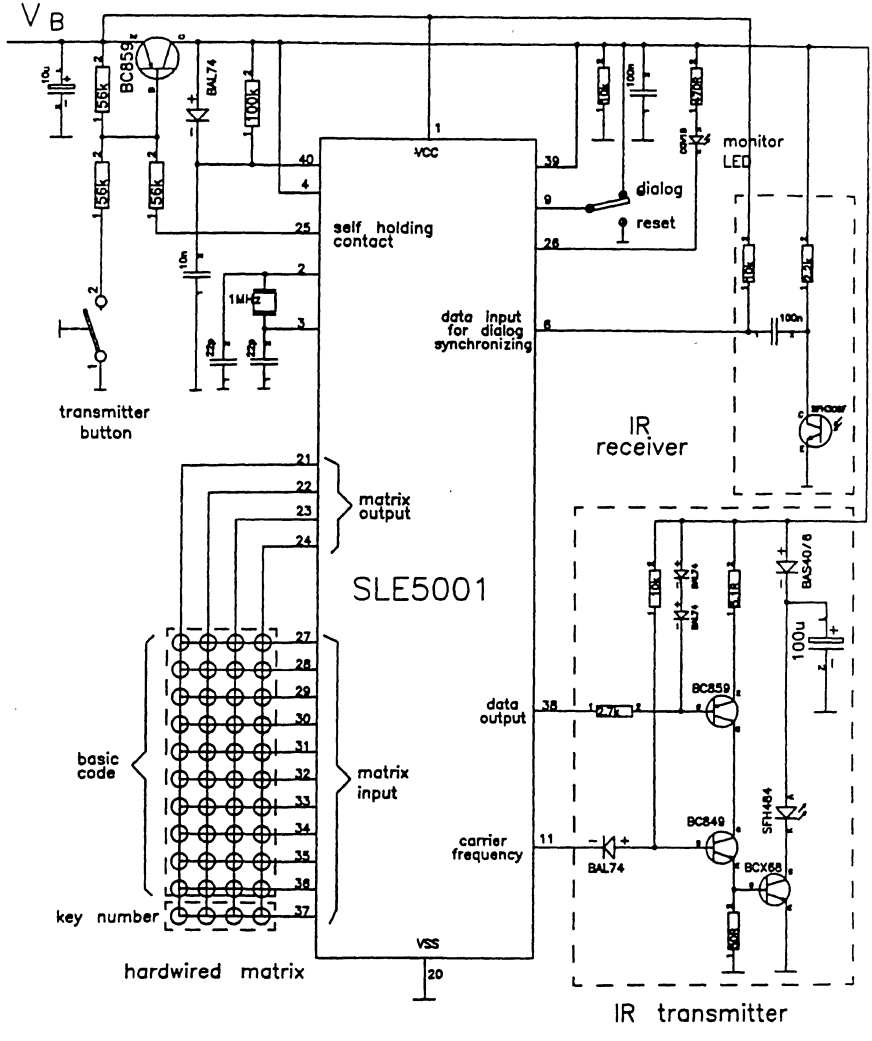


Figure 3

Application Circuit with Hardwired Matrix as Basic Code Memory

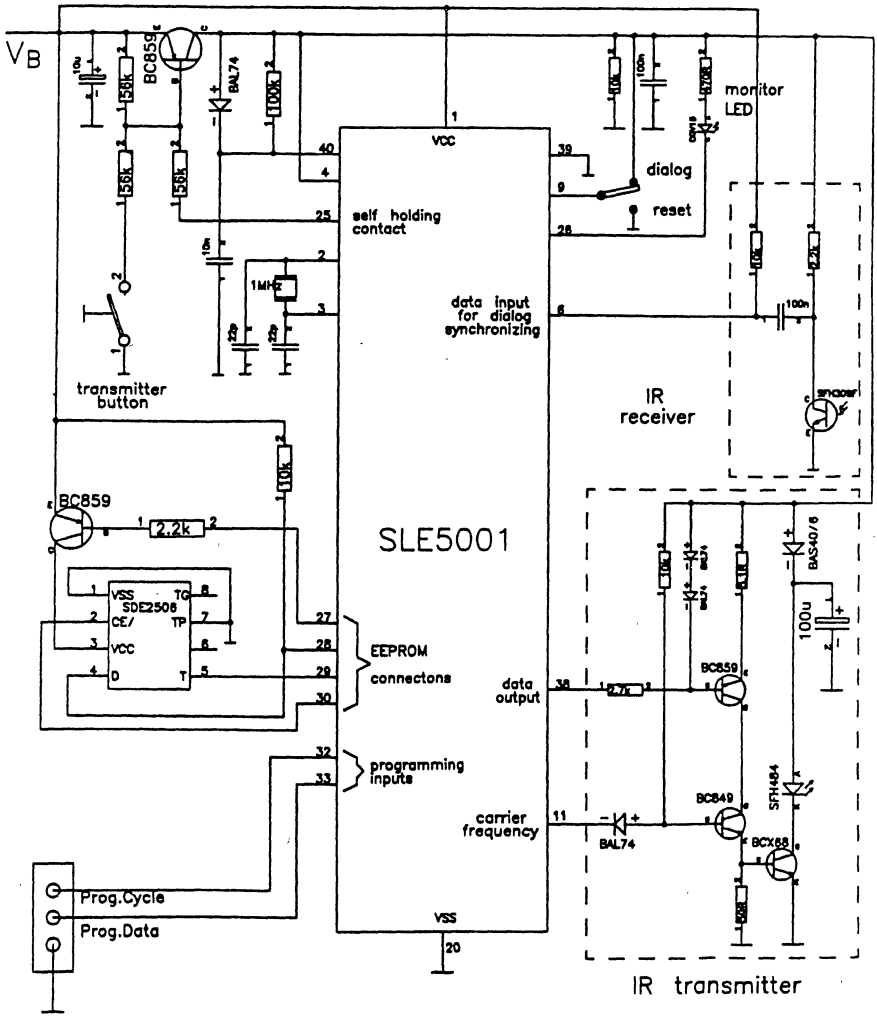


Transmitter (Key) SLE 5001

*The IR receiver can be omitted for uni-directional synchronization.
Not used pin's remain unconnected.

9

Application Circuitry with E²PROM SDE 2506 as Basic Code Memory

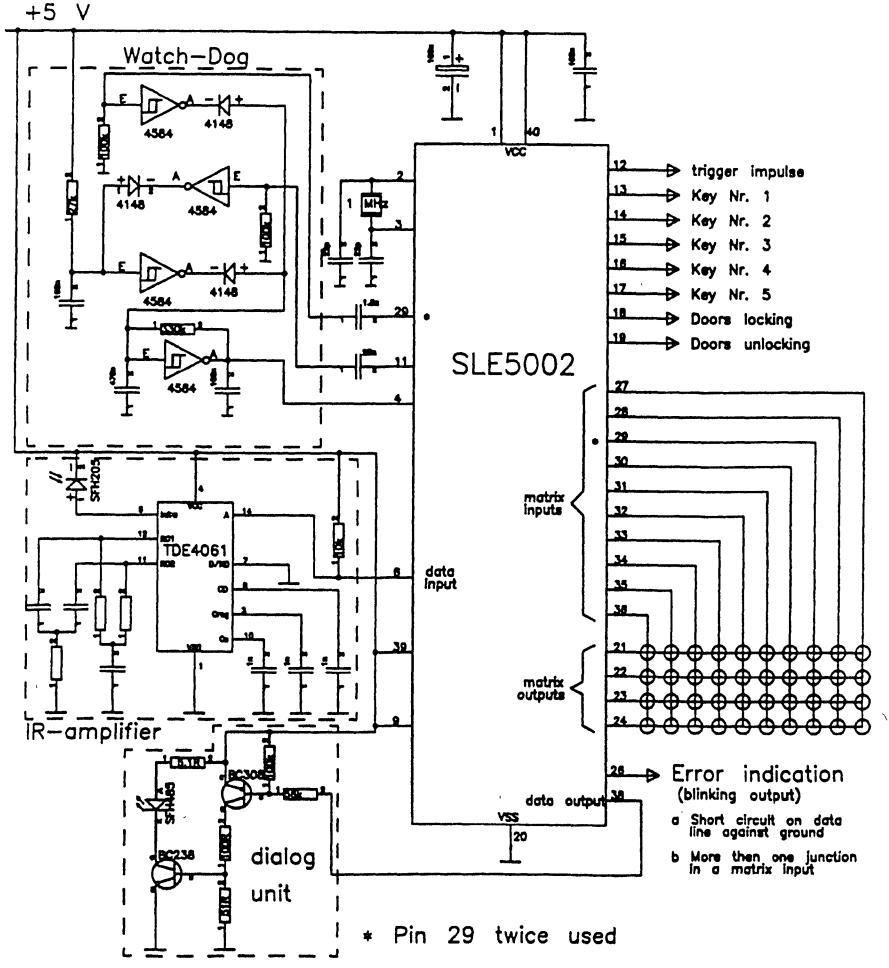


0153-9

Transmitter (Key) SLE 5001

*The IR receiver can be omitted for uni-directional synchronization.
Not used pins remain unconnected.

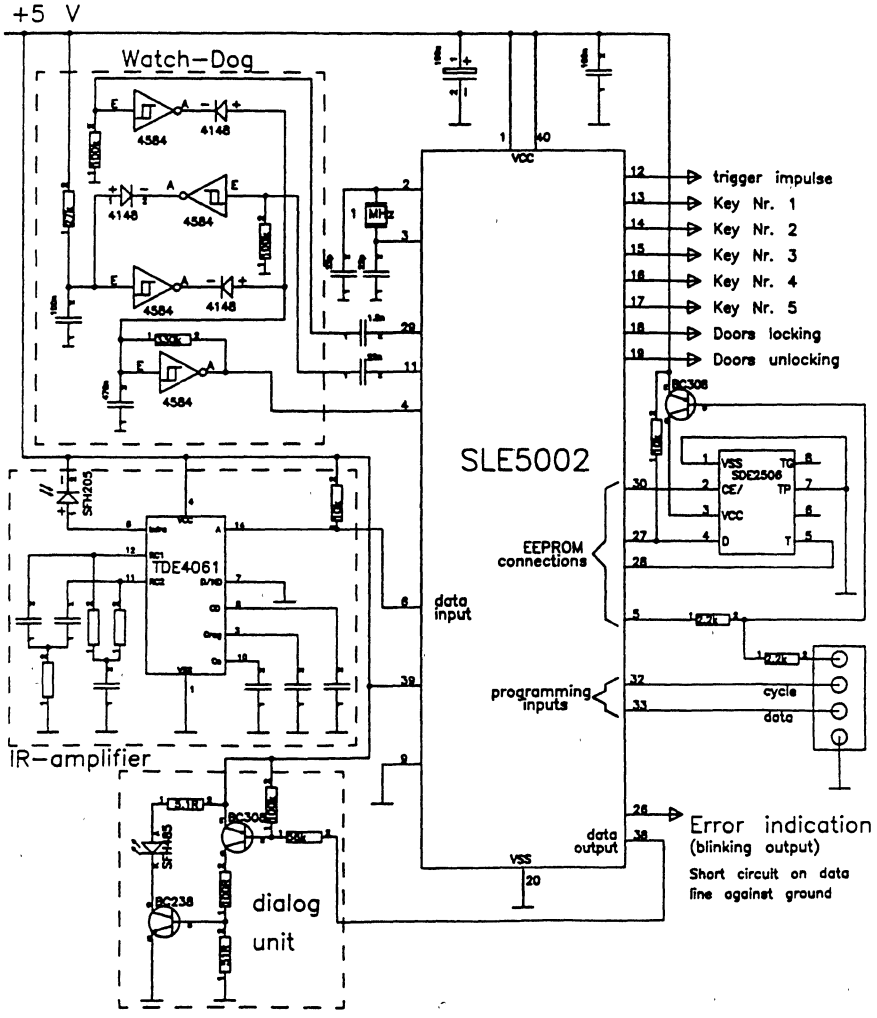
Application Circuit with Hardwire Matrix as Basic Code Memory



Receiver (Lock) SLE 5002
*Dialog-synchronization
Dialog unit can be omitted for uni-directional synchronization.
Not used pins remain unconnected.

9

Application Circuitry with E²PROM as Basic Code Memory



Transmitter (Lock) SLE 5002

*The IR receiver can be omitted for uni-directional synchronization.
Not used pins remain unconnected.

Ordering Information

Type	Function	Ordering Code	Package
SLE 5001	Transmitter	Q 67100-H 8532	DIP 40
SLE 5001 K	Transmitter	Q 67100-H 8533	Micropack
SLE 5001 W	Transmitter	Q 67100-H 8534	PLCC 44
SLE 5002	Receiver	Q 67100-H 8529	DIP 40
SLE 5002 K	Receiver	Q 67100-H 8530	Micropack
SLE 5002 W	Receiver	Q 67100-H 8531	PLCC 44

SIEMENS

TDA 4050 B
Infrared Preamplifier

The TDA 4050 B is suitable for use as infrared preamplifier in remote control facilities for radio and TV sets.

The IC includes a controlled driver stage with subsequent amplifier stage as well as an amplifier for the threshold value. The circuit is largely balanced.

Features

- Internal AGC
- Superior large signal stability
- Short-circuit proof signal output
- Simple connection for an active band filter
- Few external components

Maximum ratings

Supply voltage	V_S	16[1])	V
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\,SA}$	140	K/W

Operating range

Supply voltage range	V_S	9 to 16	V
Ambient temperature range	T_{amb}	0 to 70	°C
Input frequency range	f_i	0 to 100	kHz

9

1) intermittently 17.5 V

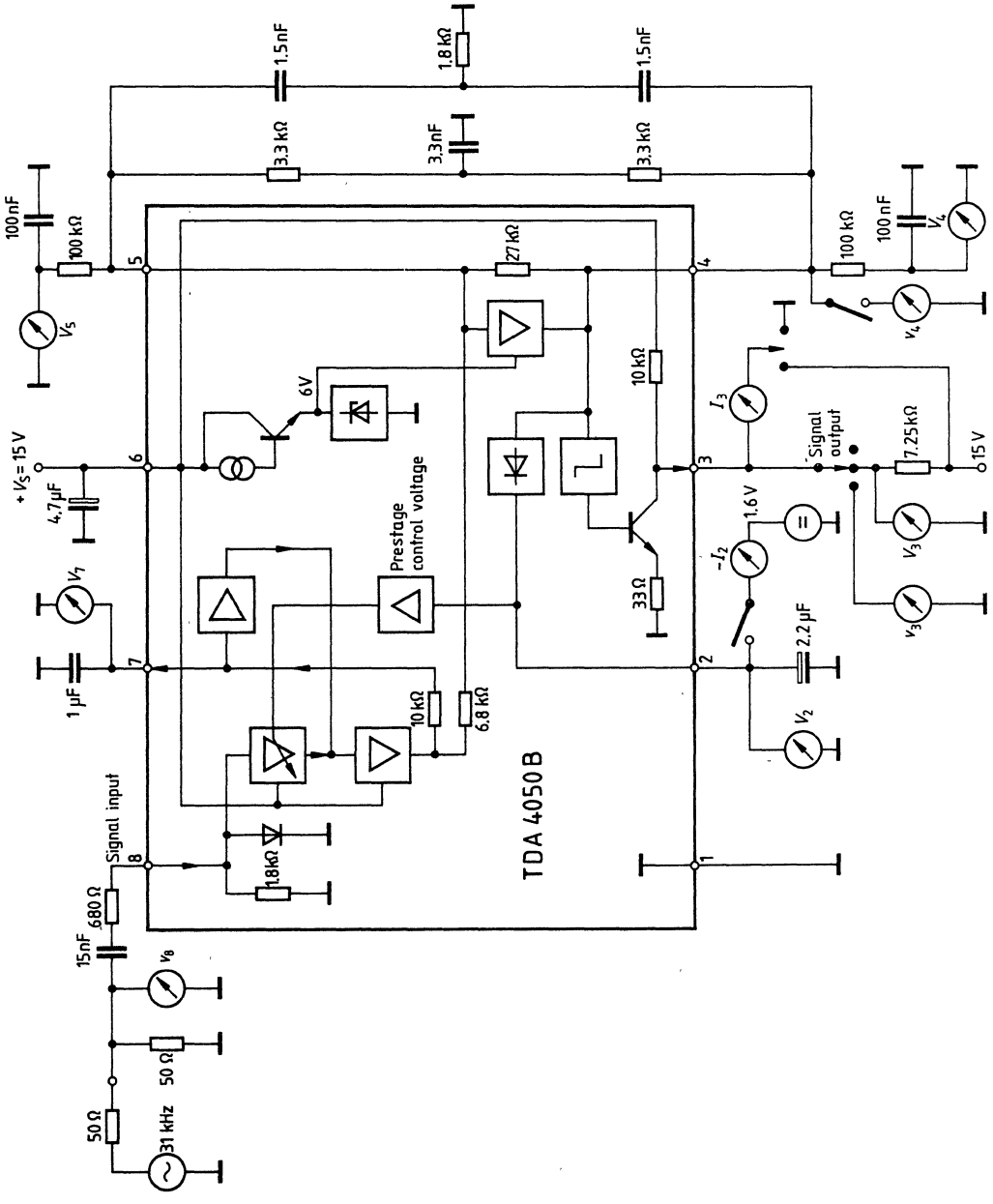
Characteristics ($V_S = 15$ V; $T_{amb} = 25$ °C; $f_{IR} = 31$ kHz) referred to measurement circuit

		min	typ	max	
Current consumption ($R_L \geqq 10$ kΩ)	I_6	6	9	12	mA
Input voltage for control start	v_{8rms}		50		µV
Input voltage for output signal	v_{8rms}			85	µV
Filter output voltage (in control range)	v_{4rms}	350	450	550	mV
Gain	$G_{4/8}$	74	77	85	dB
Gain	$G_{3/4}$		21		dB
Total control range	ΔG	74	77	85	dB
Control voltage without input signal	V_2	1325	1425	1525	mV
Control voltage ($v_{8rms} = 100$ µV)	V_2	1.5		2.1	mV
Control voltage ($v_{8rms} = 10$ mV)	V_2	1.9		2.45	V
Control voltage ($v_{8rms} = 1$ V)	V_2	2.1		2.6	V
Operating points	$V_{4/5/7}$	2.2		2.8	V
Output current ($V_3 = V_S$)	I_3		20		mA
Output dc voltage for L level	V_{3L}		150	500	mV
Output dc voltage for H level	V_{3H}	14.6			V
Charge current ($v_{8rms} = 100$ mV; $V_2 = 1.6$ V)	$-I_2$	0.4		1.0	mA
Discharge current (v_{8rms} from 1 mV to 0) ($T = 50$ ms)	I_2	0.4		3.0	µA
Input resistance	R_{i8}		1.8		kΩ
Output resistance	R_{q3}		10		kΩ
Rated resistance of the double-T network at pin 4 (unbalanced to ground)	R_4	2			kΩ

Pin configuration

Pin No.	Function
1	Ground
2	Connection for capacitance for prestage control
3	Output threshold amplifier
4	Output active filter
5	Input active filter
6	Supply voltage, positive
7	Unlocking of operating point control
8	Signal input

Measurement circuit and block diagram



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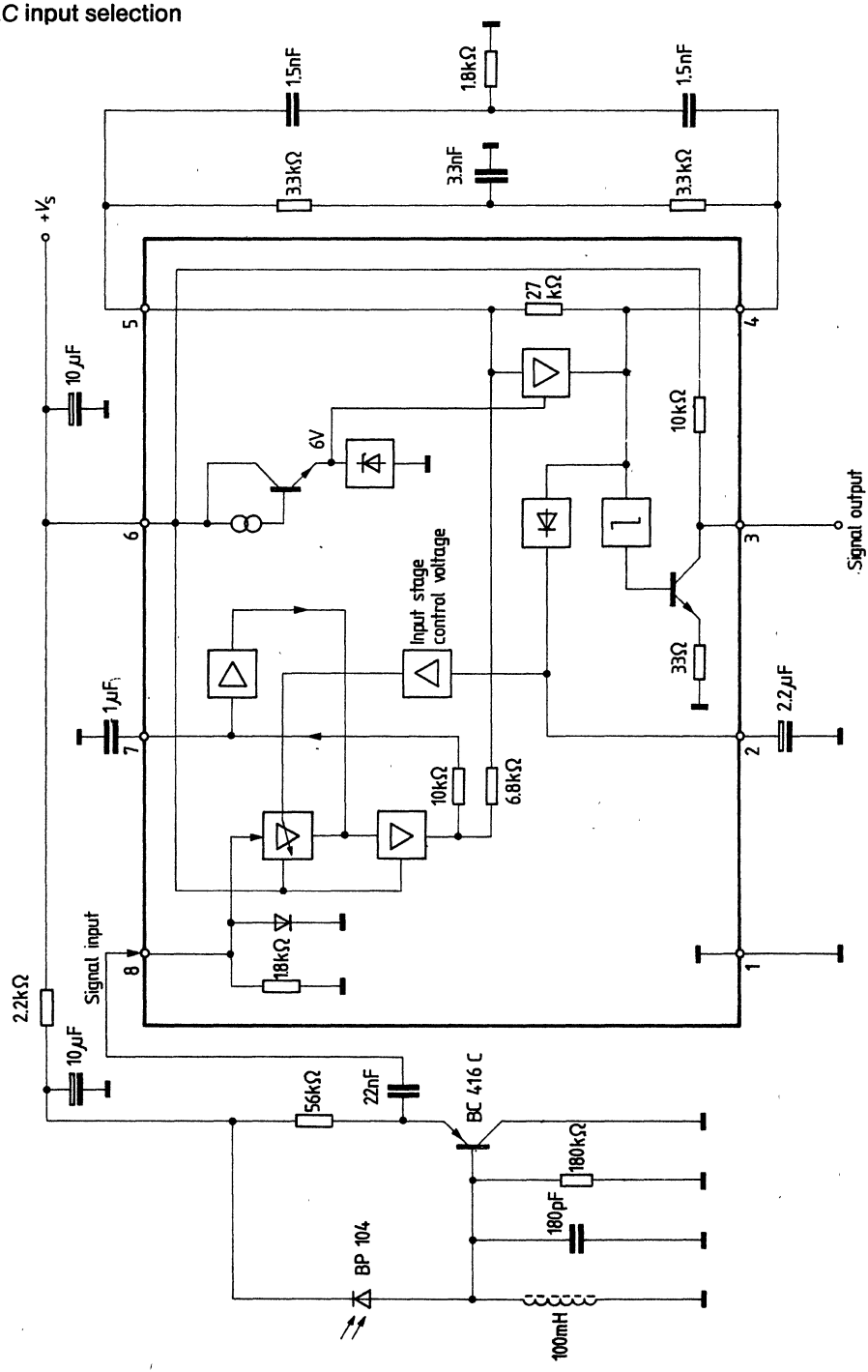
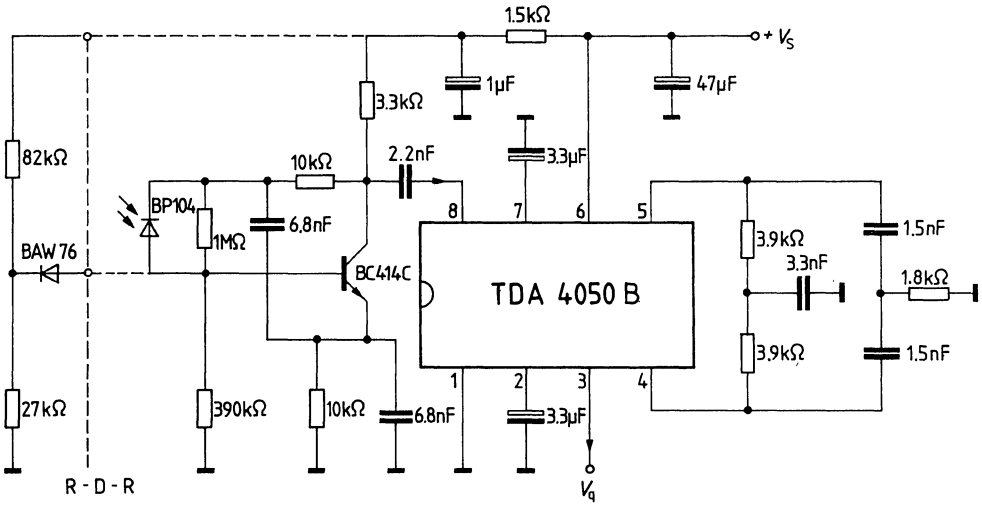
Application circuit I
incl. *LC* input selection



Application circuit II
without coil



Notes

Circuit I uses an LC resonant circuit and is of superior quality due to its high selectivity feature (approx. 3 kHz bandwidth at −3 dB).

Circuit 2 offers the lower cost solution without coil incl. broadband input selection. Higher requirements as to steady radiation and large signal stability can be met by means of resistor-diode-resistor connection (RDR).

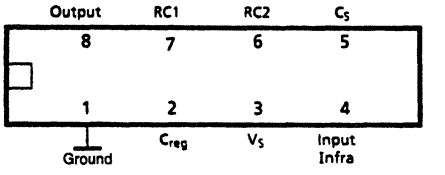
SIEMENS

Preliminary

TDA 4060/TDE 4060/TDE 4060 G
Infrared Signal Receiver

- Only 5V Supply Voltage
- Supply Current Max. 0.6 mA
- DIP 8 or SO 8 Package
- Simplified Bandpass Circuitry without External Inductance
- Extended Temperature Range −40°C to +110°C (TDE 4060)

Pin Configuration



0075-5

Pin Description

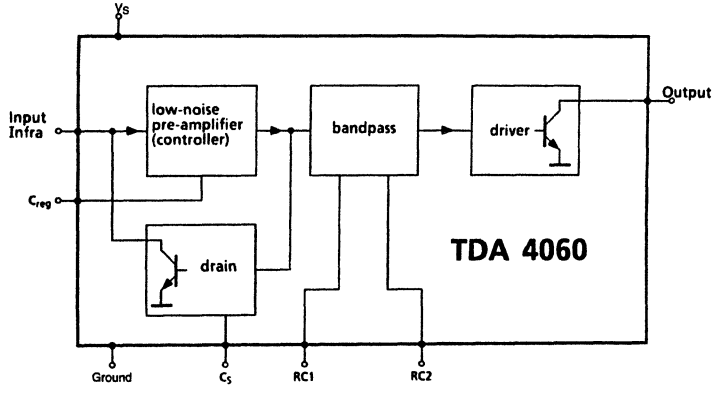
Pin Function for Package DIP 8

Pin	Function
1	Ground
2	C_{reg}
3	V_S
4	Input Infra
5	C_S
6	RC2
7	RC1
8	Output

The digital signals transmitted to an infrared receiving diode must be amplified. The application range of the TDA 4060 designed for this purpose covers the entire area of infrared signal transmission. The IC is therefore especially suitable for use in radio, TV, video as well as automobile electronics.

Through the application of a high-speed bipolar circuitry, high frequencies are processed at low curent consumption. The number of external components used with older versions has also been reduced.

Block Diagram



0075-4

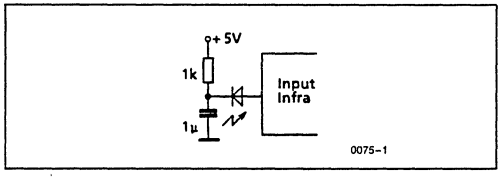
Description of Functions and Applications

Dimension and Structure

The IC can be used in all infrared systems. Depending on the chosen carrier frequency, several optimal applications are possible.

Infrared Receiver Diode

This diode, together with the cathode, leads, for example, to the supply voltage of the IC. This means that any interference of this line is delivered to the input infra by the junction capacitance of the diode. Therefore, we recommend to put an RC low pass between the plus supply and the cathode of the diode.



Input Infra

This input is high-impedance and requires only nanoampere driving currents. Therefore, we recommend to put the anode of the IR diode directly at the input.

Capacitance C_S

This capacitance C_S causes the preamplifier to become an RC-high pass filter; moreover, it also works in connection with C_{reg} and the double T-element. The transient response in particular is influenced by the application used. When working with standard IR systems the following values should be observed:

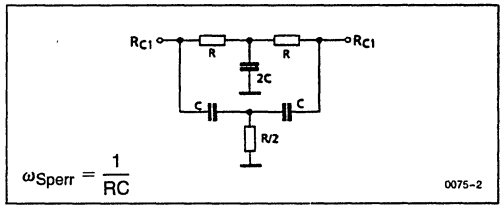
Carrier Frequency Approx. 30 KHz: C_S = 100 nF
Carrier Frequency Approx. 120 KHz: C_S = 10 nF

Capacitance C_{reg}

It is possible to control the gain of the preamplifier: the higher the IF input signal the higher the gain control. The time constant is determined by C_{reg}. If a biphase code is used (i.e. TV sets), we recommend to have 470 nF. If signal codes, which do not have any presignals for regulation, are used, C_{reg} can be decreased to 10 nF. It may happen that the IC oscillates if low capacitances are used.

Double-T-Element at RC1 and RC2

The double-T-Filter solution has proven to be the best one. The junction frequency is calculated according to the formula



The junction frequency has to be identical with the carrier frequency of the IR signal. This can be obtained by different combinations of R + C. The maximum value for R should not exceed 100 kΩ; otherwise the voltage drop at the DC current path circuit would be too large. If an oscillation occurs, it may be reduced by a lower resistance R for amplifying the circuit.

Output

The output is an open collector. If the transistor is conducted, the maximum collector current is 1 mA. We recommend to keep the collector current as small as possible since it may happen that the circuitry oscillates due to a direct feedback of the input and output. If the collector current does not exceed 200 µA, it is very unlikely that the circuitry oscillates—even in case of a poor p.c. board layout.

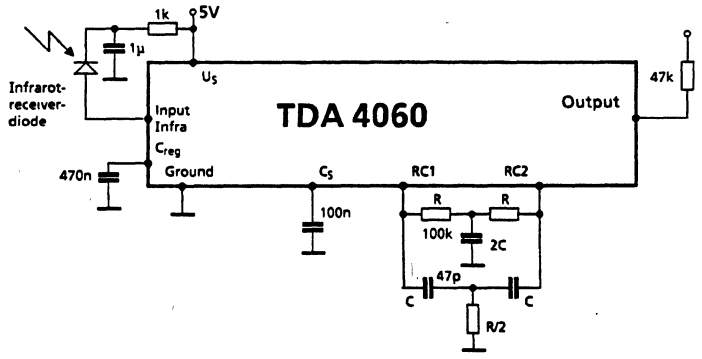
In General

The pin connection has been chosen because it keeps a crosstalk, which may occur between critical pins, as small as possible. This fact should be taken into consideration of when any layout is developed. Perhaps the supply voltage has to be blocked with a capacitance, primarily due to the current deviation, which is generated by the output.

Application Circuit

Application Example

TV remote control with mit biphase code.
Carrier frequency approx. 30 KHz; output signal non-demodulated.



Measurement Circuit

The infrared diode receives the signal as well as the infrared spectrum of emitted daylight, the 100 Hz line noise of light bulbs and portions from the spectrum of fluorescent lights.

The current sink, shown in the block diagram, drains the unwanted low frequency diode currents and, at the same time, stabilizes the operating point at the input of the low-noise preamplifiers to approximately 1.4V.

In the low-noise preamplifier the signal is sufficiently amplified to provide the bandpass filter with a suitable amplitude. The gain of the low-noise preamplifier is regulated in accordance with the input amplitude. When the signal amplitude is larger than the interference amplitude (e.g. of fluorescent light), this type of gain control prevents that the interference amplitude alone overdrives the amplifier and the useful signal is "swallowed". It is therefore possible (with limited sensitivity) to evaluate distorted signals as well.

The bandpass filter improves the signal-to-noise ratio of the signal. The edge jitter of the output signal is therefore reduced. The external RC combination should include band trap characteristics and a DC current path. The cut-off frequency of the external RC combination is identical with the carrier frequency of the useful signal.

The driver includes an open collector output. The output is in high without an input signal.

The modulated signals will not be demodulated at the output.

Absolute Maximum Ratings*

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Maximum ratings cannot be exceeded without causing irreversible damage to the integrated circuit.

Position	Parameter Maximum Rating for $T_A = 25°C$	Symbol	Conditions	Limits		Units
				Min	Max	
1	Supply Voltage	V_S		−0.3	7	V
2	Input Infra	I_{Infra}			10	mA
3	C_S, C_{reg}	$I_{Cs, Creg}$			10	mA
4	RC1, RC2	$V_{RC1, RC2}$		−0.3	U_S	V
5	Output	V_Q		−0.3	7	V
		I_Q		0	3	mA
6	Thermal Resistance	R_{thSU}	DIP 8		100	K/W
	System-Casing		SO 8		200	K/W
7	Storage Temperature	T_S		−40	+125	°C

Range of Functions

Within the functional range, the integrated circuit operates as described; deviations from the characteristic data are possible.

Position	Parameter	Symbol	Conditions	Limits		Units
				Min	Max	
1	Supply Voltage	U_S		−4.0	6.5	V
2	Current Sink Input Infra	I_{Sink}		0	2.0	mA
3	Input Voltage	V_{Infra}	$Z_{iGen} < 100\Omega$	0.6	600	mV_{eff}
4	Frequency Range (for Modulation)			20	200	KHz
5	Ambient Temperature	T_A	TDA 4060	0	+70	°C
			TDE 4060	−40	+110	°C

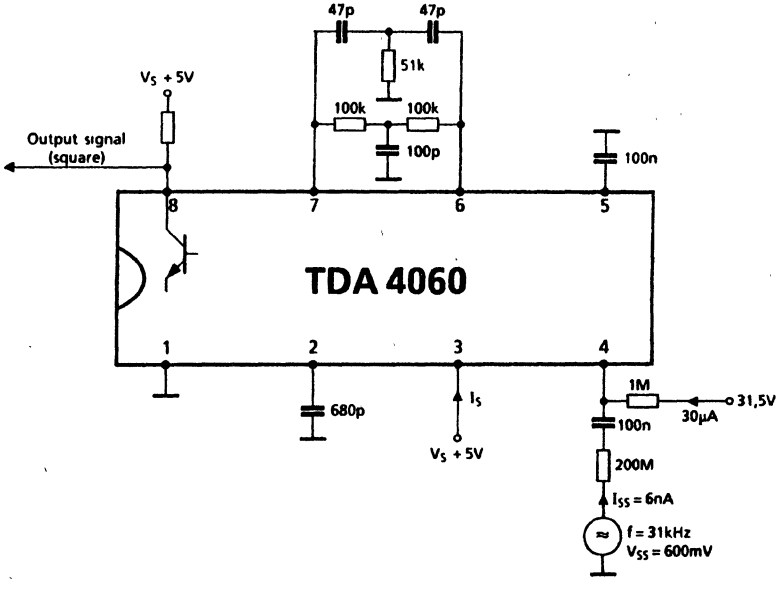
9

Characteristics

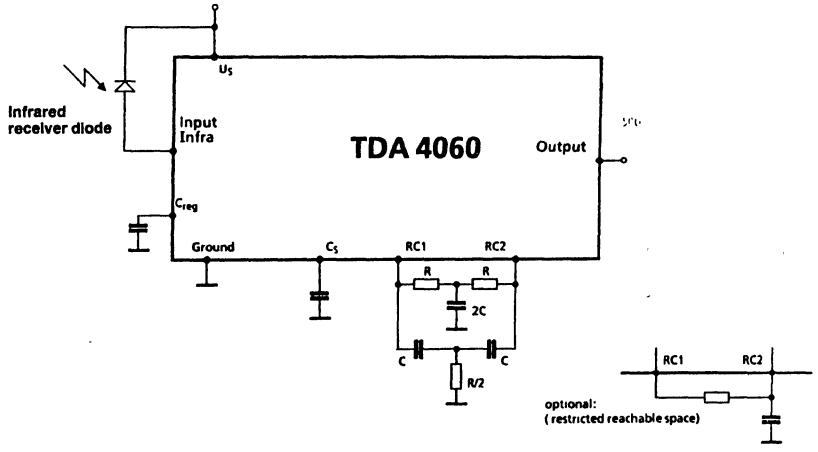
The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not stated otherwise, typical characteristics will apply at T_A = 25°C and the listed supply voltage.

Position	Parameter	Symbol	Conditions	Test Circuit	Limits			Units
					Min	Typ	Max	
Supply Voltage **Ambient Temperature**			V_S = 5V T_A = +25°C					
1	Current Consumption	I_S					600	µA
2	Input Sensitivity by Assured Signal at the Output	I_{Infra}	Diode DC Current I_{Diode} < 1 µA			1.3		nA_{SS}
			I_{Diode} < 10 µA			3.4		nA_{SS}
			I_{Diode} < 30 µA		6.0			nA_{SS}
			I_{Diode} < 100 µA		12			nA_{SS}
			I_{Diode} < 1000 µA		15			nA_{SS}
3	Output Current (Output High)	I_Q	$0 < V_Q < 7V$				10	µA
4	Output Current (Output Low)	U_Q	$0 < I_Q < 1$ mA				0.4	V

Measurement Circuit



Application Circuit



Measurement Circuit

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The current sink, shown in the block diagram, drains the unwanted low frequency diode currents and, at the same time, stabilizes the operating point at the input of the low-noise preamplifiers to approximately 1.4V.

In the low-noise preamplifier the signal is sufficiently amplified to provide the bandpass filter with a suitable amplitude. The gain of the low-noise preamplifier is regulated in accordance with the input amplitude. When the signal amplitude is larger than the interference amplitude (e.g. of fluorescent light), this type of gain control prevents that the interference amplitude alone overdrives the amplifier and the useful signal is "swallowed". It is therefore possible (with limited sensitivity) to evaluate distorted signals as well.

The bandpass filter improves the signal-to-noise ratio of the signal. The edge jitter of the output signal is therefore reduced. The external RC combination should include band trap characteristics and a DC current path. The cut-off frequency of the external RC combination is identical with the carrier frequency of the useful signal.

The driver includes an open collector output. The output is in high without an input signal.

The modulated signals will not be demodulated at the output.

Ordering Information

Type	Order No.	Package
TDA 4060	Q 67000-A 8050	DIP 8
TDE 4060	Q 67000-A 8134	DIP 8
TDE 4060 G	Q 67000-A 8135	SO 8

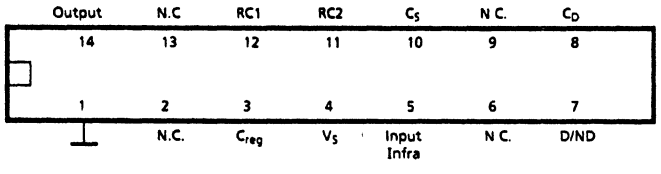
9

SIEMENS

TDA 4061/TDE 4061/TDE 4061 G
Infrared Signal Receiver

- Only 5V Supply Voltage
- Supply Current Max. 0.6 mA
- Extended Temperature Range
  −40°C to +110°C (TDE 4061)
- Simplified Bandpass Circuitry without External Inductance
- DIP 14 or SO 14 Package

Pin Configuration



0076-5

Pin Definitions

Pin	Function
1	Ground
2	N.C.
3	C_{reg}
4	V_S (Supply)
5	Input Infra
6	N.C.
7	D/ND
8	C_D
9	N.C.
10	C_S
11	RC2
12	RC1
13	N.C.
14	Output

The digital signals transmitted to an infrared receiving diode must be amplified and demodulated. The application range of the TDA 4060 designed for this purpose covers the entire area of infrared signal transmission. The IC is therefore especially suitable for use in radio, TV, video and automobile electronics.

Through the application of a high-speed bipolar circuitry, high frequencies are processed at low current consumption. The number of external components used with older versions has also been reduced.

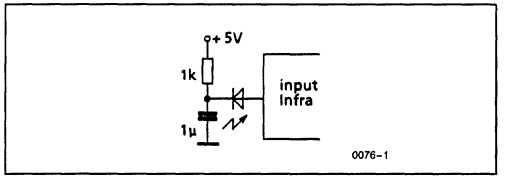
Description of Functions, Applications and Circuitry

Dimension and Structure

The IC can be used in all infrared systems. Depending on the chosen carrier frequency, several optimal applications are possible.

Infrared Receiver Diode

This diode, together with the cathode, leads, for example, to the supply voltage of the IC. This means that any interference of this line is delivered to the input infra by the junction capacitance of the diode. Therefore, we recommend to put an RC low pass between the plus supply voltage and the cathode of the diode.



Input Infra

This input is high-impedance and requires only nanoampere driving currents. Therefore, we recommend to put the anode of the IR diode directly at the input.

Capacitance C_S

This capacitance C_S causes the preamplifier to become an RC-high pass filter; moreover, it also works in connection with C_{reg} and the double T-element. The transient response in particular is influenced by the application used. When working with standard IR systems the following values should be observed:

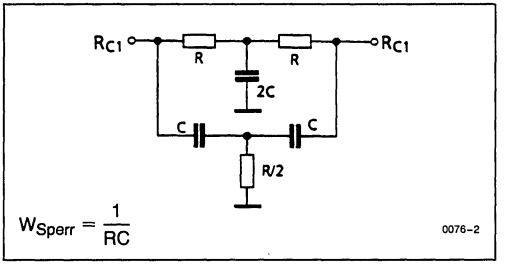
Carrier Frequency Approx. 30 KHz: C_S = 100 nF
Carrier Frequency Approx. 120 KHz: C_S = 10 nF

Capacitance C_{reg}

It is possible to control the gain of the preamplifier: the higher the IF input signal the higher the gain control. The time constant is determined by C_{reg}. If a biphase code is used (i.e. TV sets), we recommend to have 470 nF. If signal codes, which do not have any presignals for regulation, are used, C_{reg} can be decreased to 10 nF. It may happen that the IC oscillates if low capacitances are used.

Double-T-Element at RC1 and RC2

The double-T-Filter solution has proven to be the best one. The junction frequency is calculated according to the formula:



The junction frequency has to be identical with the carrier frequency of the IR signal. This can be obtained by different combinations of R + C. The maximum value for R should not exceed 100 kΩ; otherwise the voltage drop at the DC current path would be too large. If an oscillation occurs, it may be reduced by a lower resistance R for amplifying the circuit.

Demodulator Capacitance C_D

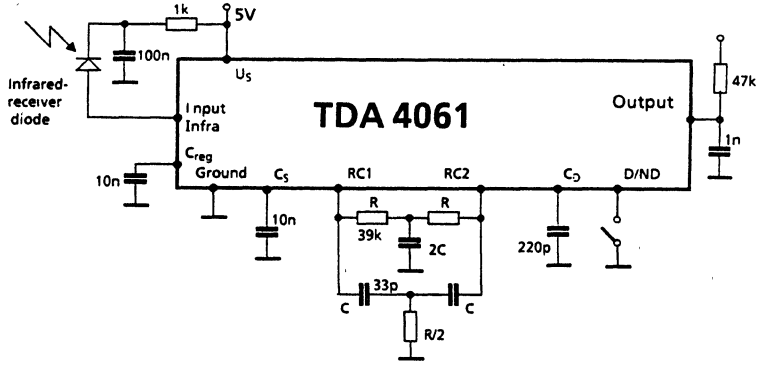
If the signal between the input and the output is wanted to be the same one, pin C_D and D/ND should not be connected. The signal has to be modulated if the triggering of the input signal is not wanted to appear at the output. Pin D/ND has to be grounded for that, and moreover, C_D has to be connected with a capacitance. Capacitance values between 100 pF and 1 nF are recommended—depending on the code transmitted.

Output

The output is an open collector. If the transistor is conducted, the maximum collector current is 1 mA. We recommend to keep the collector current as small as possible since it may happen that the circuitry oscillates due to a direct feedback of the input

Application Example

Electrical door key.
Carrier frequency approx. 120 KHz; output signal demodulated.



and output. If the collector current does not exceed 200 μA, it is very unlikely that the circuitry oscillates—even in case of a poor p.c. board layout.

In General

The pin connection has been chosen because it keeps a crosstalk, which may occur between critical pins, as small as possible. This fact should be taken into consideration when any layout is developed. Perhaps the supply voltage has to be blocked with a capacitance, primarily due to the current deviation, which is generated by the output.

Description of Circuitry

The infrared diode receives the signal as well as the infrared spectrum of emitted daylight, the 100 Hz line noise of light bulbs and portions from the spectrum of fluorescent lights.

The current sink shown in the block diagram drains the unwanted low frequency diode currents and, at the same time, stabilizes the operating point at the input of the low-noise preamplifiers to approx. 1.4V.

In the low-noise preamplifier the signal is sufficiently amplified to provide the band passfilter with a suitable amplitude. The gain of the low-noise preamplifier is regulated in accordance with the input amplitude. When the signal amplitude is larger than the interference amplitude (e.g. of fluorescent light), this type of gain control prevents that the interference amplitude alone overdrives the amplifier and the useful signal is "swallowed". It is therefore possible (with limited sensitivity) to evaluate distorted signals as well.

The bandpass filter improves the signal-to-noise ratio of the signal. The edge jitter of the output signal is therefore reduced. The external RC combination should include band trap characteristics and a DC current path. The cut-off frequency of the external RC combination is identical with the carrier frequency of the useful signal.

The driver includes an open collector output. The output is in high without an input signal.

It is possible to select between demodulated or non-demodulated output signals. The selection "demodulated-non demodulated" is programmed via the input D/ND. When the input D/ND is not connected, the non-demodulated signal is present at the output. The pin capacitor C_D is left open. For generating demodulated signals, D/ND should be tied to ground and pin "C_D" connected.

Absolute Maximum Ratings*

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Position	Parameter Maximum Rating for T_A = 25°C	Symbol	Conditions	Limits		Units
				Min	Max	
1	Supply Voltage	V_S		−0.3	7	V
2	Input Infra	I_{Infra}			10	mA
3	C_S, C_D, C_{reg}	$I_{Cs, Cd, Creg}$			10	mA
4	D/ND	$V_{D/ND}$		−0.3	V_S	V
5	RC1, RC2	$V_{RC1, RC2}$		−0.3	V_S	V
6	Output	V_Q		−0.3	7	V
		I_Q		0	3	mA
7	Thermal Resistance System-Casing	R_{thSC}	DIP 14		65	K/W
			SO 14		125	K/W
8	Storage Temperature	T_S		−40	+125	°C

Functional Range

Within the functional range, the integrated circuit operates as described; deviations from the characteristic data are possible.

Position	Parameter	Symbol	Conditions	Limits		Units
				Min	Max	
1	Supply Voltage	V_S		4.0	6.5	V
2	Current Sink Input Infra	I_{Sink}		0	2.0	mA
3	Input Voltage	V_{Infra}	$Z_{iGen} < 100\Omega$	0.6	600	mV_{rms}
4	Frequency Range (for Modulation)			20	200	KHz
5	Ambient Temperature	T_A	TDA 4061	0	+70	°C
			TDE 4061	−40	+110	°C

9

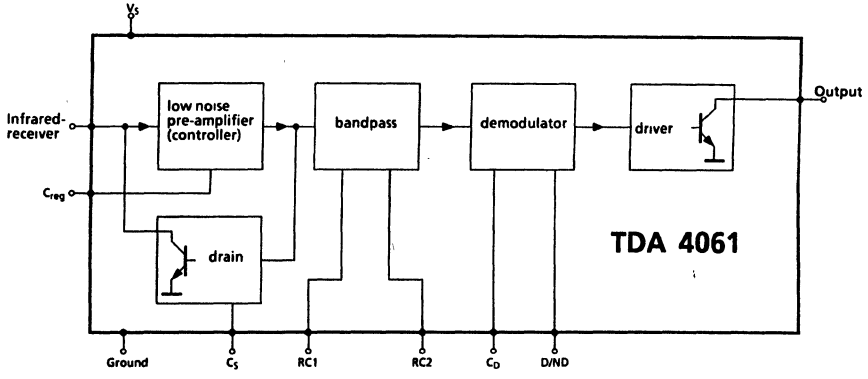
Characteristics

The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not stated otherwise, typical characteristics will apply at T_A = 25°C and the listed supply voltage.

Position	Parameter	Symbol	Conditions	Test Circuit	Limits			Units
					Min	Typ	Max	
Supply Voltage **Ambient Temperature**			V_S = 5V T_A = +25°C					
1	Current Consumption	I_S					600	µA
2	Input Sensitivity (Constant Current Source)	I_{Infra}	Diode DC Current I_{Diode} < 1 µA			1.3		nA_{SS}
			I_{Diode} < 10 µA			3.4		nA_{SS}
			I_{Diode} < 30 µA		6.0			nA_{SS}
			I_{Diode} < 100 µA		12			nA_{SS}
			I_{Diode} < 1000 µA		15			nA_{SS}
3	Switch over Input D/ND Output Demodulated Output Not-Demodul.	 $-I_{D/ND}$ $I_{D/ND}$	 $0 < V_{D/ND} < 0.4V$ $1V < V_{D/ND} < V_S$			10	 1	 µA mA*
4	Output Current (Output High)	I_Q	$0 < I_Q < 7V$				10	µA
5	Output Current (Output Low)	V_Q	$0 < I_Q < 1$ mA				0.4	V

*Normally, the pin D/ND is not connected, for "output non-demodulated", this means $I_{D/ND}$ = 0.

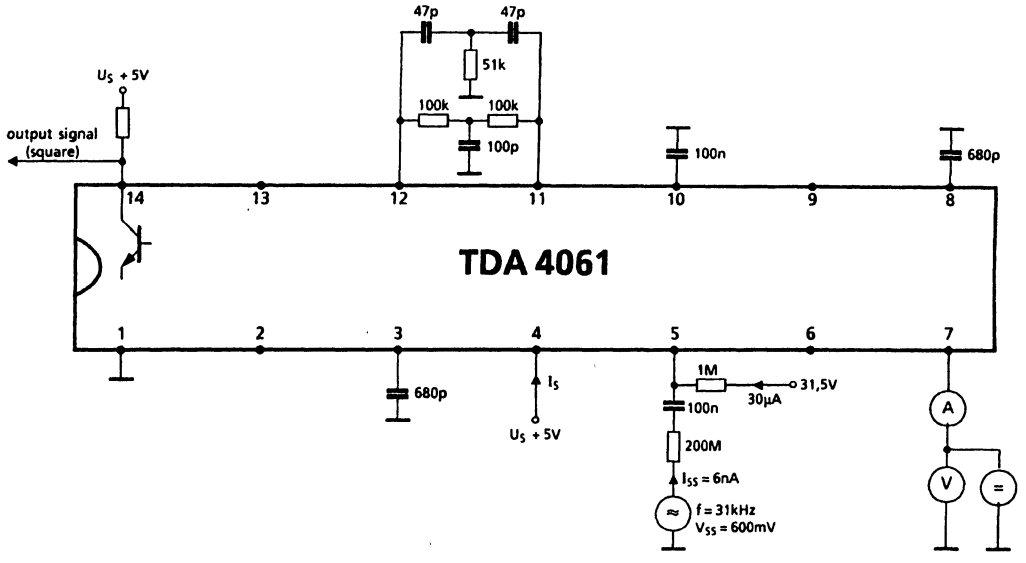
Block Diagram



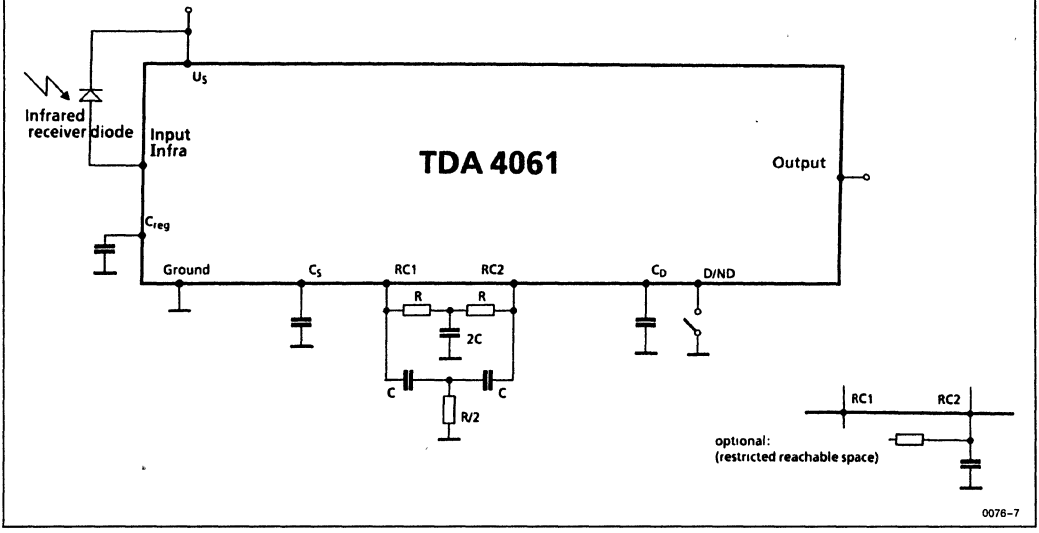
Ordering Information

Type	Order No.	Package
TDA 4061	Q 67000-A 8124	DIP 14
TDE 4061	Q 67000-A 8136	DIP 14
TDE 4061 G	Q 67000-A 8137	SO 14

Measurement Circuit



Application Circuit



9

SIEMENS

UAA 170
LED Driver for Light Spot Displays

IC for driving 16 light emitting diodes. Depending on the input voltage, the individual LEDs are driven within one row in form of a light spot. The UAA 170 provides a linear relation between control voltage and the driven LED.

By using an appropriate circuitry, the brightness of the LEDs can be varied and the crossing over of the light spot can be set between "smooth" and "abrupt". By connecting two ICs in parallel, up to 30 LEDs can be driven.

Maximum ratings

Supply voltage	V_S	18	V
Input voltages	V_{11}, V_{12}, V_{13}	6	V
Load current	I_{14}	5	mA
Junction temperature	T_j	150	°C
Storage temperature range	T_{stg}	−40 to 125	°C
Thermal resistance (system-air)	$R_{th\,SA}$	90	K/W

Operating range

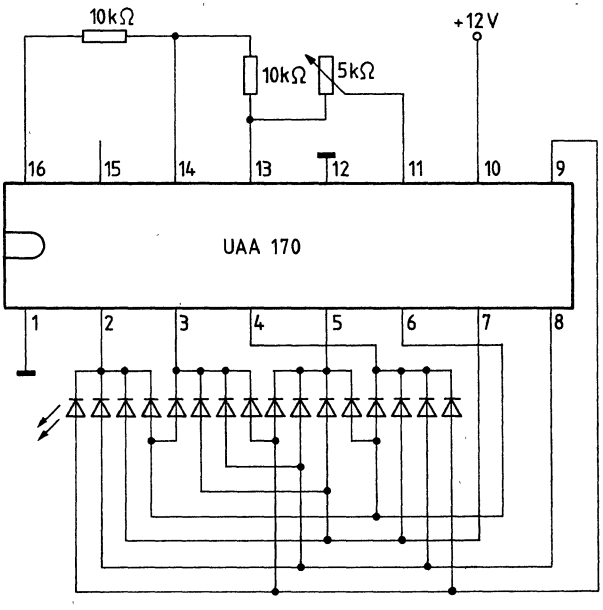
Supply voltage range (LED red)[1]	V_S	11 to 18	V
Ambient temperature range	T_{amb}	−25 to 85	°C

1) The lower limit only applies to a forward voltage of the LEDs of approx. 1.5 V (red LEDs); the lower limit increases with higher forward voltage

Characteristics ($V_S = 12$ V; $T_{amb} = 25$ °C)

		min	typ	max	
Current consumption ($I_{14} = 0$; $I_{16} = 0$)	I_S	2	4	10	mA
Control input current	I_{11}	−2			µA
Reference input current	I_{12}, I_{13}	−2			µA
Voltage difference	$\Delta V_{12/13}$	1.4		6	V
Voltage difference for smooth light transition	$\Delta V_{12/13}$	1.4			V
Voltage difference for abrupt light transition	$\Delta V_{12/13}$	4			V
Voltage difference	$\Delta V_{12/13}$	4			V
Stabilized voltage $I_{14} = 300$ µA	V_{14}		5	6	V
$I_{14} =$ 5 mA	V_{14}	4.5			V
Reference input voltage	$V_{ref\,max}$	1.4		6	V
	$V_{ref\,min}$	0		4.6	V
Tolerance of forward voltages of LEDs, mutually	ΔV_D			0.5	V
Output current for LEDs	ΣI_D		25		mA

Test circuit



Scale display with light emitting diodes

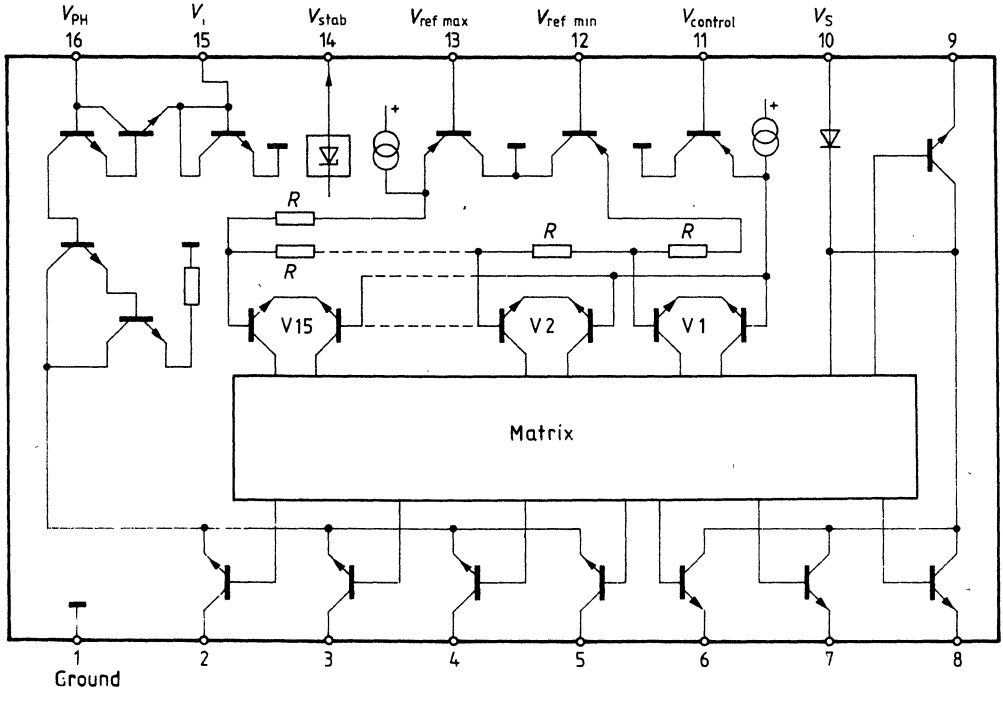
Scale displays by means of a wandering light spot are particularly suitable for indicating approximate values. Applications of this kind are level sensors, VU-meters, tachometers, radio scales etc. When applying the displays in measuring equipment, multicolored light emitting diodes can be used as range limitation. Ring scales are obtained by a circular arrangement of the diodes. The IC UAA 170 has especially been developed for driving a scale of 16 LEDs.

The input voltages at pins 11, 12 and 13 are freely selectable between 0 and 6 V. Any kind of adjustment becomes possible by suitable voltage drivers. The DC value $V_{control}$ is always assigned to a certain spot of the diode chain.

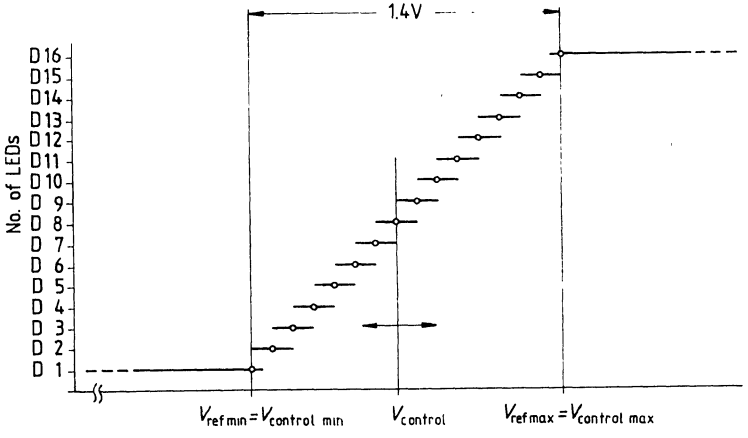
The voltage difference between pins 12 and 13 thereby corresponds to the possible indication range. $\Delta V_{12/13}$ defines at the same time the light transition between two diodes. With $\Delta V_{12/13}$ approx. 1.4 V, the light point glides smoothly along the scale. With increasing voltage difference, the passage becomes more abrupt. With $\Delta V_{12/13}$ approx. 4 V, the light point jumps from diode to diode.

Input voltages beyond the selected indication range cause the diodes D1 or D16 respectively, to light up, identifying only that the range has been exceeded.

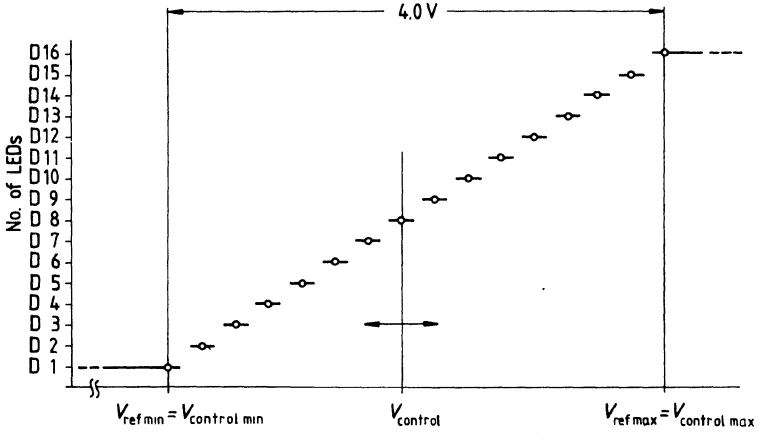
Block diagram



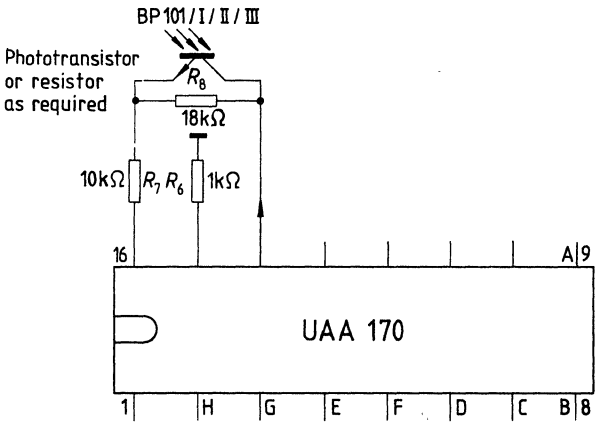
Indication for smooth transition UAA 170



Indication for abrupt transition UAA 170



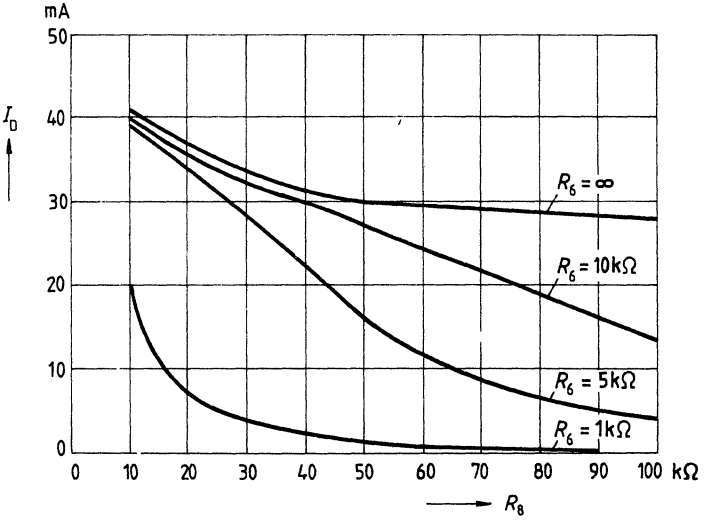
Brightness control



Pins 14, 15, and 16 serve to determine the diode current. Corresponding to the desired light intensity, the forward current of the diodes is linearly variable in the range I_f approx. 0 to 50 mA. The resistance at pin 15 defines the adjusting range. The resistances between pin 14 and 16 determine the current.

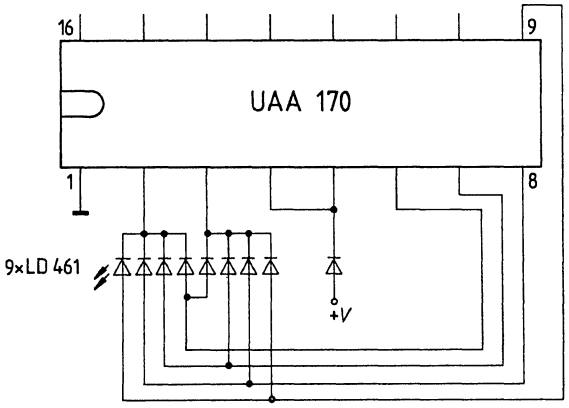
With the aid of a phototransistor, such as BP 101, the light intensity of the LEDs can be adjusted to the light fluctuations of the environment.

Diode current versus base emitter resistance
$V_S = 12$ V; $T_{amb} = 25$ °C; $V_{14} = 5.4$ V; red LEDs

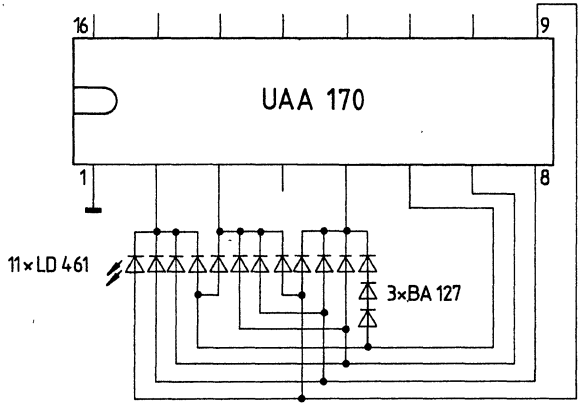


Operation of less than 16 LEDs

Control of 9 LEDs

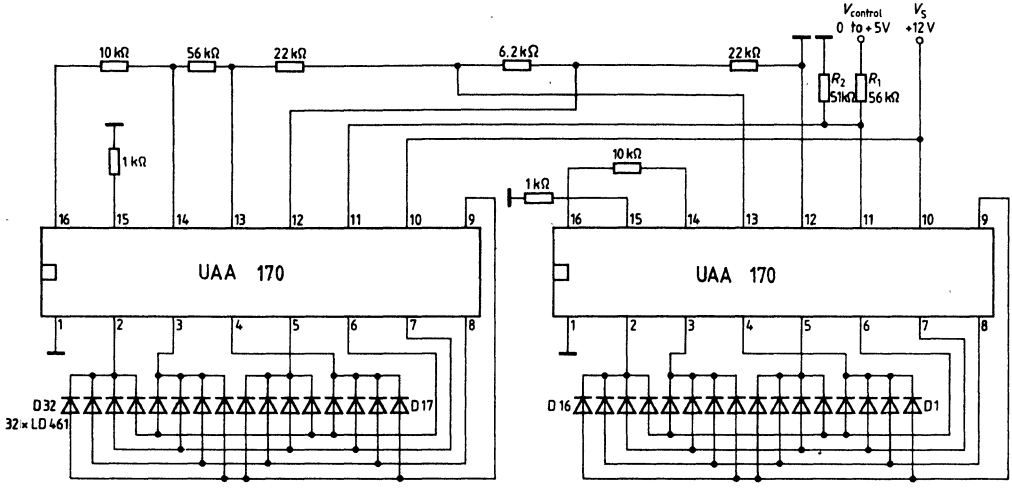


Control of 11 LEDs



Application circuit for the control of 30 LEDs with 2 x UAA 170

Range of control voltage $V_{control} = 0$ to 5 V
Voltage difference $V_{12/13} = 2 \times 1.2\ V = 2.4\ V$
Since the diodes D16 or D17 are permanently lit when the maximum or minimum voltages V_{13} or V_{12} adjusted by R_3, R_4, R_5, are exceeded or fall short the diodes should be covered, if necessary.



The figure shows an expansion of the circuit to 30 diodes with 2 ICs UAA 170. The diodes D16 or D17 light permanently, when the reciprocal absolute ratings are exceeded. They should be covered. The reference voltage $\Delta V_{12/13} = 2 \times 1.2 = 2.4$ V is derived from a stabilized dc voltage of typ. 5 V available at pin 14. A resistance of 6.2 kΩ provides an overlapping of the ranges in order to ensure a smooth transition from D15 to D18. The control voltage $V_{control}$ is forwarded in a parallel mode to pins 11 via a divider $R_1 : R_2$. The voltage divider is to be dimensioned according to the desired input voltage. With a divider current of $I = 100\ \mu A$ and a control voltage of $V_{control} = 10$ V, the following is valid:

$$R_2 = \frac{\Delta V_{12/13}}{I} = \frac{2.4}{0.1} = 24\ k\Omega \text{ and}$$

$$R_1 = \frac{V_{control} - \Delta V_{12/13}}{I} = \frac{7.6}{0.1} = 76\ k\Omega$$

The nearest standard value is $R_1 = 75$ kΩ. The voltage difference for switching an incremental step is then $\Delta V_{control} = \frac{10\ V}{30} = 0.16$ V.

SIEMENS

UAA 180
LED Driver for Light Band Displays

Integrated circuit for driving 12 light emitting diodes. Corresponding to the input voltage the LEDs forming a light band are controlled similar to a thermometer scale.

By using an appropriate circuitry the brightness of the LEDs can be varied and the light passage between two adjacent LEDs can be arranged between "smooth" and "abrupt".

Maximum ratings

Supply voltage	V_S	18	V
Input voltage	V_3	6	V
	V_{16}	6	V
	V_{17}	6	V
Storage temperature range	T_{stg}	−40 to 125	°C
Junction temperature	T_j	150	°C
Thermal resistance (system-air)	$R_{th\,SA}$	78	K/W

Operating range

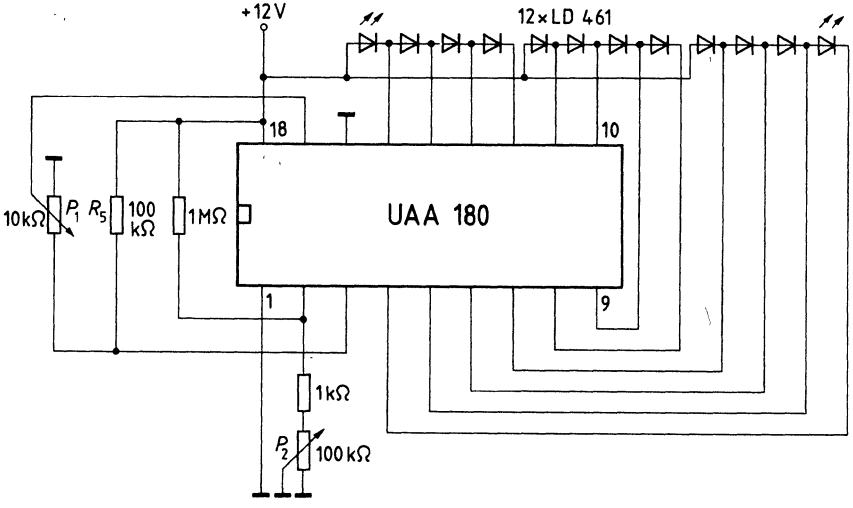
Supply voltage range	V_S	10 to 18	V
Ambient temperature range	T_{amb}	−25 to 85	°C

9

Characteristics ($V_S = 12$ V, $T_{amb} = 25$ °C)

		min	typ	max	
Current consumption ($I_2 = 0$) (without LED current)	I_{18}		5.5	8.2	mA
Input currents	I_3		0.3	1	µA
($V_3 - V_{16} < 2$ V)	I_{16}		0.3	1	µA
	I_{17}		0.3	1	µA
Voltage difference for smooth light transition	$V_{16/3}$	1			V
Voltage difference for abrupt light transition	$V_{16/3}$	4			V
Diode current per diode	I_D		10		mA
Tolerance of LED forward voltages	ΔV_D			1	V

Measurement circuit



P_1 light band test
P_2 brightness test

Scale display with light emitting diodes

Scale displays by means of a growing light band are particularly suitable for the measuring of approximate values. Applications of this kind are level sensors, VU meters, tachometers, field strength indicators etc. When applying the displays in measuring equipment, multi-colored LEDs can be used as range limitation.

The voltage difference between pins 16 and 3 thereby corresponds to the possible indication range. $\Delta V_{16/3}$ defines at the same time the light passage between two diodes. With $\Delta V_{16/3} \geqq 1$ V, the light band glides smoothly along the scale. With increasing voltage difference, the passage becomes more abrupt. With $\Delta V_{16/3}$ approx. 4 V, the light band jumps from diode to diode.

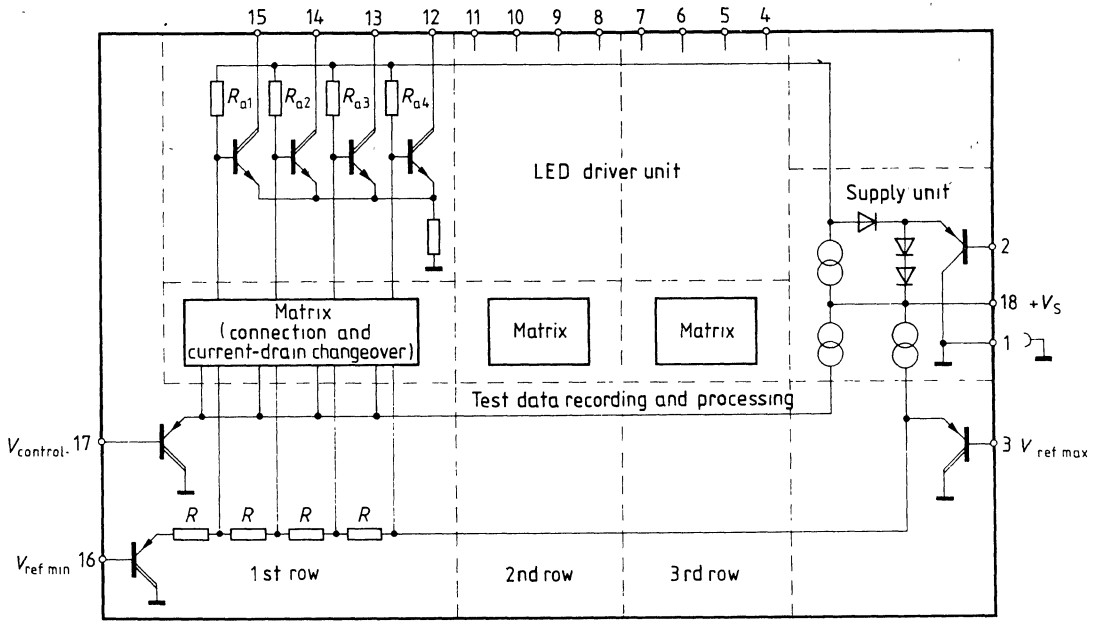
Each quartet must consist of identical diodes in order to maintain its functional characteristics.

It is therefore possible to design the first and third quartet as diodes emitting the color red and the second quartet as diodes emitting the color green to delineate a certain operational area.

Pin 2 serves to determine the diode current. Corresponding to the desired light intensity, the forward current of the diodes is variably linear in the range I_f approx. 0 to 10 mA.

Application circuit 1 shows the possibility of designing this resistance, adjustable by means of a phototransistor BP 101, in order to adapt the light intensity to changing ambient brightness. The adjusting range of the diode current lies between I_f approx. 5 mA (BP 101 not lit) and I_f approx. 10 mA (BP 101 fully lit). If pin 2 is open the diode current is 10 mA.

Block diagram



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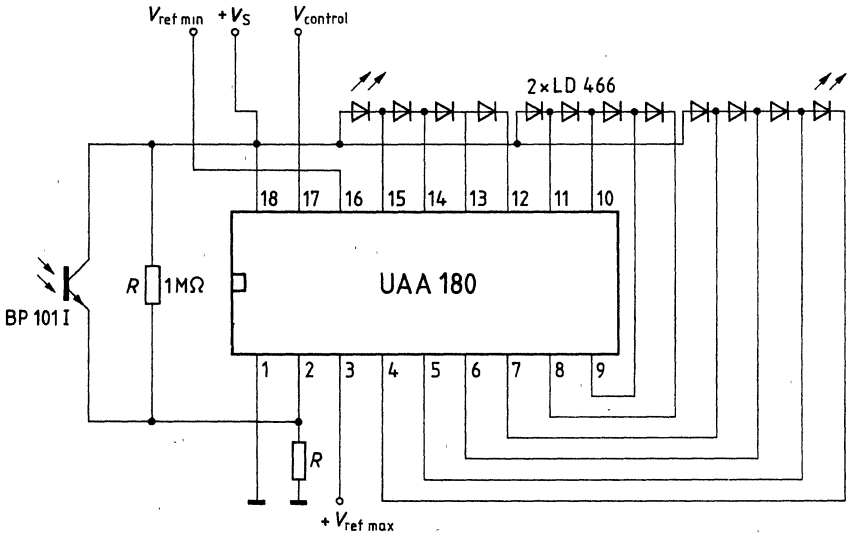
Application circuit 1

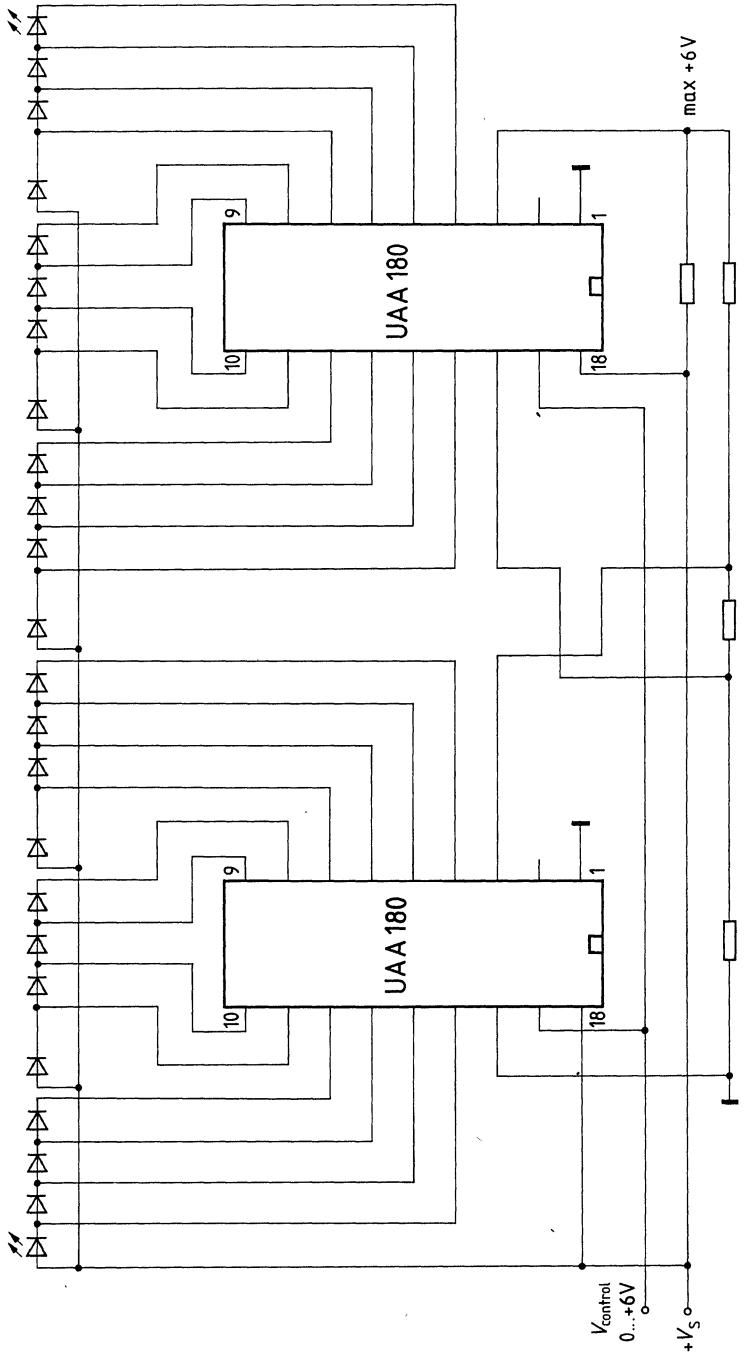


Depending on the actual maximum ratings, the resistances R_1 to R_7 can be varied widely as follows:

$R_3 = 820\ \Omega$
$R_4 = 56\ k\Omega$
$R_5 = 220\ k\Omega$
$R_6 = 2.2\ k\Omega \ldots 100\ k\Omega$

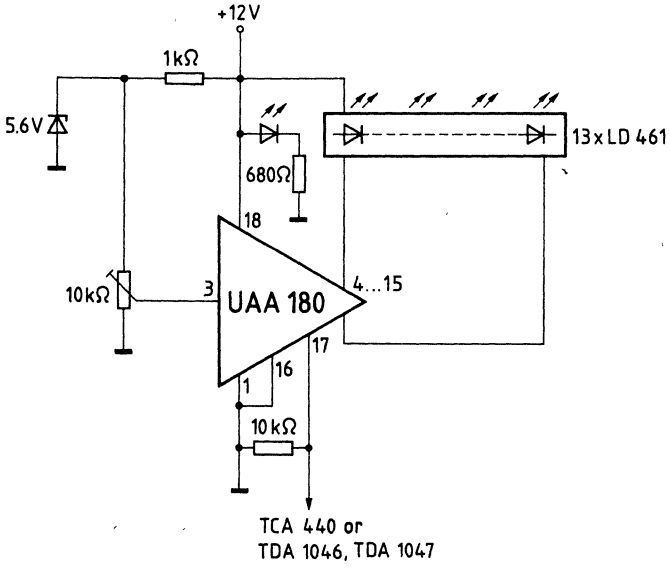
If a quartet does not need the full number of display diodes and if the first wired diodes shall be left luminous at full driving, bridges have to be inserted replacing the missing LEDs. Otherwise the first diodes of the quartet switch off when their display range is exceeded.

Application circuit 2
for cascading several UAA 180 ICs (up to 7)



Application circuit 3

for field strength indication



ICs for Power Supply Control

10

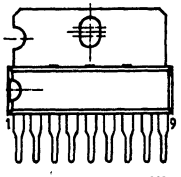
SIEMENS

TDA 4601, TDA 4601 D
Control ICs for Switched-Mode Power Supplies

- Direct Control of the Switching Transistor
- Low Start-Up Current
- Reversing Linear Overload Characteristic
- Base Current Drive Proportional to Collector Current
- Protective Circuit for Case of Disturbance

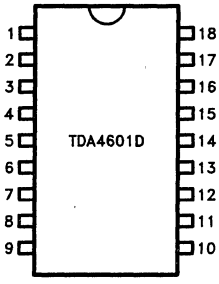
Pin Configurations

SIP 9



0094-19

DIP 18



0094-20

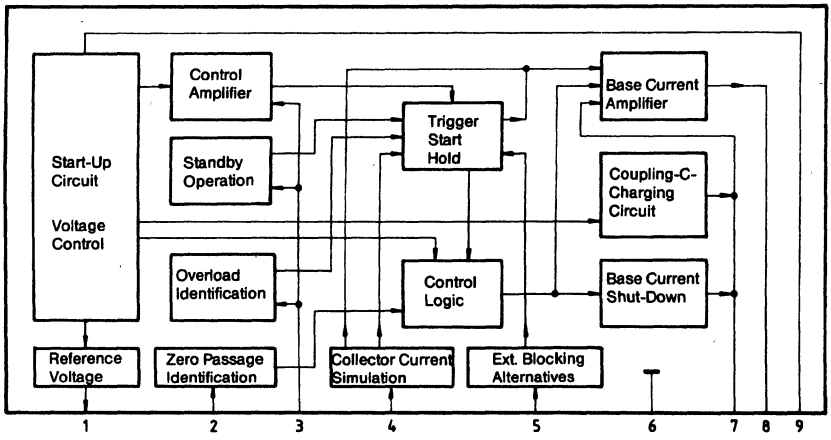
Pin Descriptions

Pin	Function
1	V_{REF} Output
2	Zero Passage Identification
3	Input Control Amplifier, Overload Amplifier
4	Collector Current Simulation
5	Connection for Additional Protective Circuit
6	Ground (Rigidly Connected to Substrate Mounting Plate)
7	DC Output for Charging Coupling Capacitor
8	Pulse Output—Driving of Switching Transistor
9	Supply Voltage
10–18	Ground (TDA 4601 D)

The integrated circuit TDA 4601/D is designed for driving, controlling and protecting the switching transistor in self-oscillating flyback converter power supplies as well as for protecting the overall power supply unit. In case of disturbance the rise of the secondary voltage is prevented. In addition to the IC's application range including TV receivers, video tape recorders, hifi devices and active loud speakers, it can also be used in power supply units for professional applications due to its wide control range and high voltage stability during increased load changes.

10

Block Diagram



Circuit Description

The TDA 4601 is designed for driving, controlling and protecting the switching transistor in flyback converter power supplies during start-up, normal and overload operations as well as during disturbed operation. In case of disturbance the drive of the switching transistor is inhibited and a secondary voltage rise is prevented.

I. Start-Up

The start-up procedures (on-mode) include three consecutive operating phases as follows:

1. **Build-Up of Internal Reference Voltage**

   The internal reference voltage supplies the voltage regulator and effects charging of the coupling electrolytic capacitor connected to the switching transistor. Current consumption will remain at $I_9 <$ 3.2 mA with a supply voltage up to V_9 approx. 12V.

2. **Enabling of Internal Voltage—Reference Voltage V_1 = 4V**

   Simultaneously with V_9 reaching approx. 12V, an internal voltage becomes available, providing all component elements, with the exception of the control logic, with a thermally stable and overload-resistant current supply.

3. **Enabling of Control Logic**

   In conjunction with the generation of the reference voltage, the current supply for the control logic is activated by means of an additional stabilization circuit. The integrated circuit is then ready for operation.

The above described start-up phases are necessary for ensuring the charging of the coupling electrolytic capacitor, which in turn supplies the switching transistor. Only then is it possible to ensure that the transistor switches accurately.

II. Normal Operating Mode/Control Operating Mode

At the input of pin 2 the zero passage of the frequency provided by the feedback coil is registered and forwarded to the control logic. Pin 3 (control input, overload and standby identification) receives the rectified amplitude fluctuations of the feedback coil. The control amplifier operates with an input voltage of approx. 2V and a current of approx. 1.4 mA. Depending on the internal voltage reference, the overload identification limits in conjunction with collector current simulator pin 4 the operating range of the control amplifier. The collector current is simulated by an external RC combination present at pin 4 and internally set threshold voltages. The largest possible collector current applicable with the switching transistor (point of return) increases in proportion to the increased capacitance (10 nF). Thus the required operating range of the control amplifier is established. The range of control lies between a DC voltage clamped at 2V and a sawtooth-shaped rising AC voltage, which can vary up to a max. amplitude of 4V (reference voltage). During secondary load reduction to approx. 20W, the switching frequency is increased (approx. 50 kHz) at an almost constant pulse duty factor (1:3). During additional secondary load decreases to approx. 1W, the switching frequency increases to approx. 70 kHz and pulse duty factor to approx. 1:11. At the same time collector peak current is reduced to <1A.

The output levels of the control amplifier as well as those of the overload identification and collector current simulator are compared in the trigger and forwarded to the control logic. Via pin 5 it is possible to externally inhibit the operations of the IC. The output at pin 8 will be inhibited when voltages of $\leq \frac{V_{REF}}{2} - 0.1V$ are present at pin 5.

Flipflops for controlling the base current amplifier and the base current shut-down are set in the control logic depending on the start-up circuit, the zero passage identification as well as enabling by the trigger. The base current amplifier forwards the sawtooth-shaped V_4 voltage to the output of pin 8. A current feedback with an external resistor ($R = 0.68\Omega$) is present between pin 8 and pin 7. The applied value of the resistor determines the max. amplitude of the base driving current for the switching transistor.

III. Protective Operating Mode

The base current shut-down activated by the control logic clamps the output of pin 7 to 1.6V. As a result, the drive of the switching transistor is inhibited. This protective measure is enabled if the supply voltage at pin 9 reaches a value $\leq 6.7V$ or if voltages of $\leq \frac{V_{REF}}{2} - 0.1V$ are present at pin 5.

In case of short-circuits occurring in the secondary windings of the switched-mode power supply, the integrated circuit continuously monitors the fault conditions. During secondary, completely load-free operation only a small pulse duty factor is set. As a result the total power consumption of the power supply is held at N = 6W ... 10W during both operating modes. After the output has been inhibited for a voltage supply of $\leq 6.7V$, the reference voltage (4V) is switched off if the voltage supply is further reduced by $\Delta V_9 = 0.6V$.

Protective Operating Mode at Pin 5 in Case of Disturbance

The protection against disturbance such as primary undervoltages and/or secondary over voltages (e.g., by changing the component parameters for the switched-mode power supply) is realized as follows:

*In application circuit 1; 10 kΩ/3W.

Protective Operating Mode with Continuous Fault Condition Monitoring

In case of disturbance the output pulses at pin 8 are inhibited by falling below the protective threshold V_5, with a typical value of $V_1/2$. As a result current consumption is reduced ($I_9 \geq 14$ mA at $V_9 = 10V$).

With a corresponding **high-impedance** start-up resistor*, supply voltage V_9 will fall below the minimum shut-down threshold (5.7V) for reference voltage V_1. V_1 will be switched off and current consumption is further reduced to $I_9 \leq 3.2$ mA at $V_9 \leq 10V$.

Because of these reductions in current consumption, the supply voltage can rise again to reach the switch-on threshold of $V_9 \geq 12.3V$. The protective threshold at pin 5 is released and the power supply is again ready for operation.

In case of continuing problems of disturbance ($V_5 \leq V_1/2 - 0.1V$) the switch-on mode is interrupted by the periodic protective operating mode described above, i.e., pin 8 is inhibited and V_9 is falling, etc.

IV. Switch-On in the Wide Range Power Supply (90 Vac to 270 Vac)

(Application Circuit 2)

Self-oscillating flyback converters designed as wide range power supplies require a power source independent of the rectified line voltage for TDA 4601. Therefore the winding polarity of winding 11/13 corresponds to the secondary side of the flyback converter transformer. Start-up is not as smooth as with an immediately available supply voltage, because TDA 4601 has to be supplied by the start-up circuit until the entire secondary load has been charged. This leads to long switch-on times, especially if low line voltages are applied.

However, the switch-on time can be shortened by applying the special start-up circuit (dotted line). The uncontrolled phase of feedback control winding 15/9 is used for activating purposes. Subsequent to activation, the transistor T1 begins to block when winding 11/13 generates the current supply for TDA 4601. Therefore, the control circuit cannot be influenced during operation.

Absolute Maximum Ratings*

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Supply Voltage (V_9) ..... 0V to 20V

Voltages

Reference Output (V_1) ..... 0V to +6V
Zero Passage Identification (V_2) ..... −0.6V to +0.6V
Control Amplifier (V_3) ..... 0V to +3V
Collector Current Simulation (V_4) ..... 0V to +8V
Blocking Input (V_5) ..... 0V to +8V
Base Current Cut-Off Point (V_7) ..... 0V to V_9
Base Current Amplifier Output (V_8) ..... 0V to V_9

Currents

Zero Passage Identification (I_{i2}) ..... −5 mA to +5 mA
Control Amplifier (I_{i3}) ..... −3 mA to +3 mA
Collector Current Simulation (I_{i4}) ..... 0 mA to +5 mA
Blocking Input (I_{i5}) ..... 0 mA to +5 mA
Base Current Cut-Off Point (I_{q7}) ..... −1A to +1.5A
Base Current Amplifier Output (I_{q8}) ..... −1.5A to 0A
Junction Temperature (T_j) ..... 125°C
Storage Temperature Range (T_{stg}) ..... −40°C to +125°C
Thermal Resistances
System-Air TDA 4601 (R_{thSA}) ..... 70 K/W
System-Case TDA 4601 (R_{thSC}) ..... 15 K/W
System-Air(1) TDA 4601 D (R_{thSA}) ..... 66 K/W
System-Air(1) TDA 4601 D (R_{thSA1}) ..... 44 K/W

Operating Range

Supply Voltage (V_9) ..... +7.8V to +18V
Case Temperature TDA 4601 (T_C) ..... 0°C to +85°C
Ambient Temperature(3) TDA 4601 D (T_A) ..... 0°C to +70°C

Notes:
1. Case soldered on PC board without cooling surface.
2. Case soldered on PC board with copper-clad 35 µm layer, cooling surface 25 cm^2.
3. R_{thSA1} = 44 K/W and P_V = 1W.

Characteristics T_A = 25°C; according to measurement circuit 1 and diagram

Parameter	Symbol	Limits			Units
		Min	Typ	Max	
Start Operation					
Current Consumption (V_1 not yet Switched On)					
V_9 = 2V	I_9			0.5	mA
V_9 = 5V	I_9		1.5	2.0	mA
V_9 = 10V	I_9		2.4	3.2	mA
Switching Point for V_1	V_9	11.0	11.8	12.3	V
Normal Operation V_9 = 10V; V_{cont} = −10V; V_{clock} = ±5.0V; f = 20 kHz; Duty Cycle 1:2 after Switch-On					
Current Consumption					
V_{cont} = −10V	I_9	110	135	160	mA
V_{cont} = 0V	I_9	50	75	100	mA
Reference Voltage					
I_1 < 0.1 mA	V_1	4.0	4.2	4.5	V
I_1 = 5 mA	V_1	4.0	4.2	4.4	V
Temperature Coefficient of Reference Voltage	TC_1		10^{-3}		1/K

Characteristics T_A = 25°C; according to measurement circuit 1 and diagram (Continued)

Parameter	Symbol	Limits			Units
		Min	Typ	Max	
Normal Operation (Continued) V_9 = 10V; V_{cont} = −10V; V_{clock} = ±5.0V; f = 20 kHz; Duty Cycle 1:2 after Switch-On					
Control Voltage V_{cont} = 0V	V_3	2.3	2.6	2.9	V
Collector Current Simulation Voltage V_{cont} = 0V V_{cont} = 0V/−10V	 V_4* ΔV_4*	 1.8 0.3	 2.2 0.4	 2.5 0.5	 V V
Clamping Voltage	V_5	6.0	7.0	8.0	V
Output Voltages V_{cont} = 0V V_{cont} = 0V V_{cont} = 0V/−10V	 V_{q7}* V_{q8}* ΔV_{q8}	 2.7 2.7 1.6	 3.3 3.4 2.0	 4.0 4.0 2.4	 V V V
Feedback Voltage	V_2		0.2		V
Protective Operation V_9 = 10V; V_{cont} = −10V; V_{clock} = ±0.5V; f = 20 kHz; Duty Cycle 1:2					
Current Consumption V_5 < 1.9V	I_9	14	22	28	mA
Switch-Off Voltage V_5 < 1.9V	V_{q7}	1.3	1.5	1.8	V
Switch-Off Voltage V_5 < 1.9V	V_4	1.8	2.1	2.5	V
Blocking Input Blocking Voltage V_{cont} = 0V	V_5	$\frac{V_1}{2} - 0.1$	$\frac{V_1}{2}$		V
Supply Voltage Blocked for V_8 V_{cont} = 0V	V_9	6.7	7.4	7.8	V
V_1 Off (with Further Reduction of V_9)	ΔV_9	0.3	0.6	1.0	V

Note:
*DC component only

Characteristics T_A = 25°C; according to measurement circuit 2

Parameter	Symbol	Limits			Units
		Min	Typ	Max	
Switching Time (Secondary Voltage)	t_{on}		350	450	ms
Voltage Variation S3 = Closed ΔN_3 = 20W	ΔV_{2sec}		100	500	mV
Voltage Deviation S2 = Closed ΔN_2 = 15W	ΔV_{2sec}		500	1000	mV
Standby Operation S1 = Open Secondary Useful Load = 3W	 ΔV_{2sec} f $N_{primary}$	 70 	 20 75 10	 30 12	 V kHz VA

The cooling conditions have to be optimized with regard to maximum ratings (T_C; T_j; R_{thSC}; R_{thSA}).

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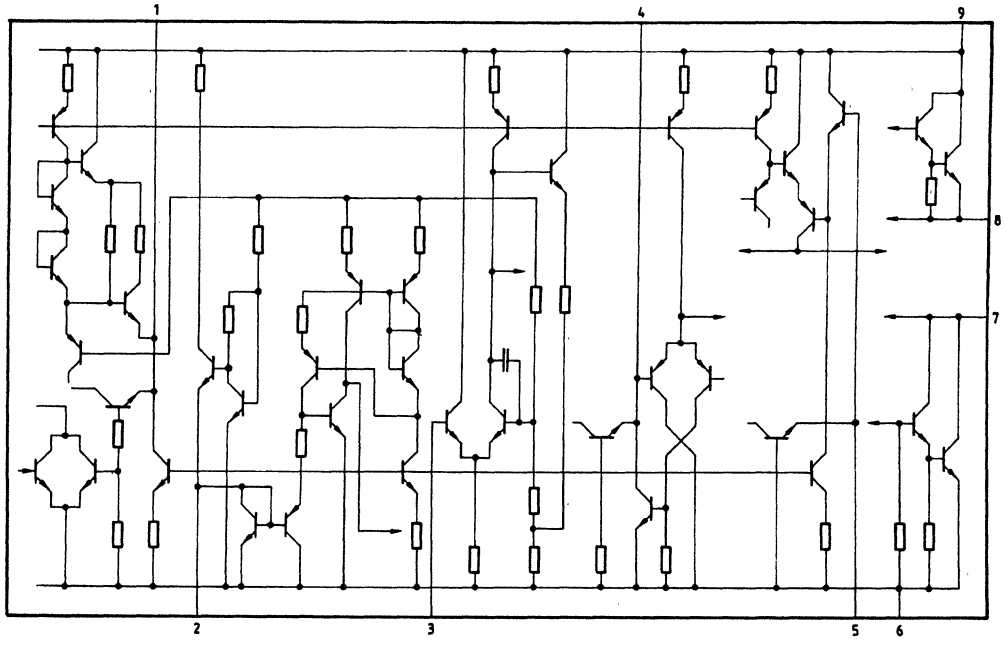
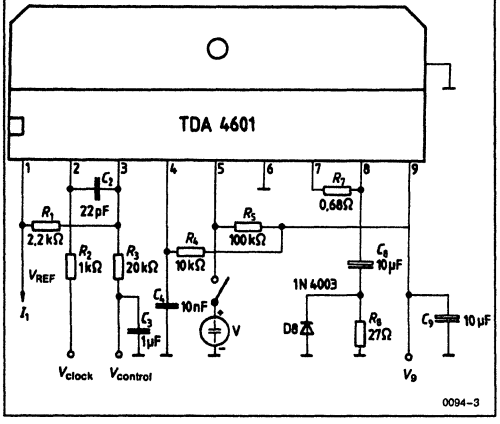
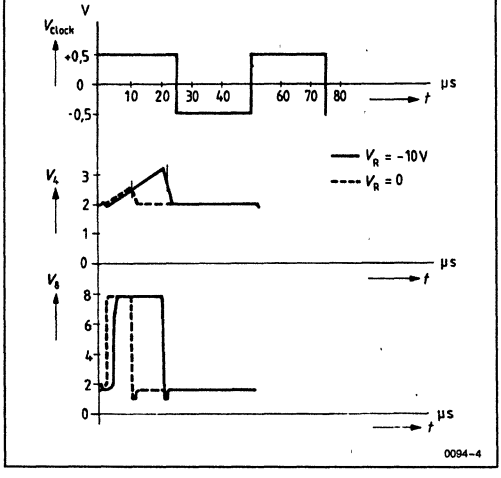
Circuit Diagram



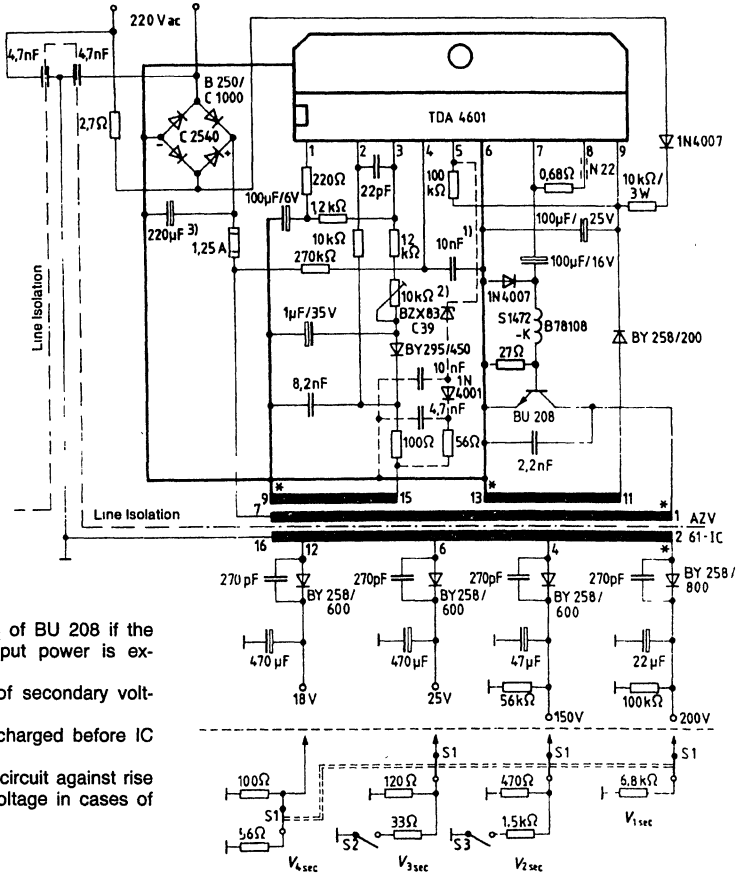
Test and Measurement Circuit 1



Test Diagram: Overload Operation



Test and Measurement Circuit 2



Notes:
1. Limits $I_{C\ max}$ of BU 208 if the permissible output power is exceeded.
2. Adjustment of secondary voltage.
3. Must be discharged before IC Change.
- - - Protective circuit against rise of secondary voltage in cases of disturbance.

Notes on application circuit 1

Protective Circuit Against Secondary Voltage Rise even in Case of Disturbance

During standby this circuit type is necessary only under certain conditions. If switch S1 is open and the secondary side is loaded with no more than 1W to 5W, a secondary voltage overshoot of approx. 20% will occur.

In case of disturbance (e.g., if the potentiometer is loosely contacted resulting in 10 kΩ(2), if the capacitor exhibits a 1 µF loss in capacitance, or if the 2 kΩ resistor increases to a high-impedance value of 32 kΩ), the protective effect of the standard turn-off is not active before the point of return has been reached. The result is that during disturbance energy is pumped into the secondary side, which will not ease off before reaching the point of return and, in the worst case, entails an instantaneous doubling of the voltage to 300V (endangering the secondary electrolytic capacitors).

This additional protective circuit, which identifies the energy surge as voltage overshoot, is directly active at control winding 9/15. Through the 56Ω resistor and the 1N4001 rectifier the negative portion is deducted and stored in the 10 nF capacitor. If the amplitude exceeds the voltage of Z diode BZX 83/39, pin 5 is drawn below the turn-off threshold, inhibiting further control pulses at pin 8. During disturbance conditions the voltage overshoot on the secondary side will assume maximum values of approx. 30%.

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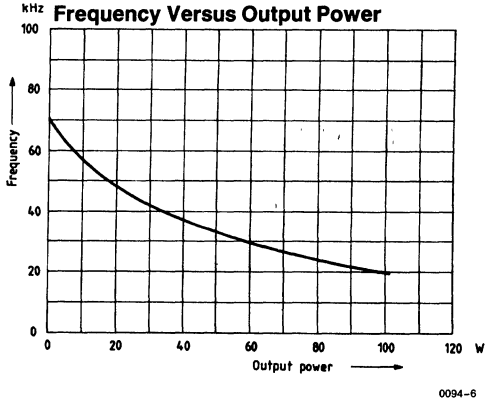
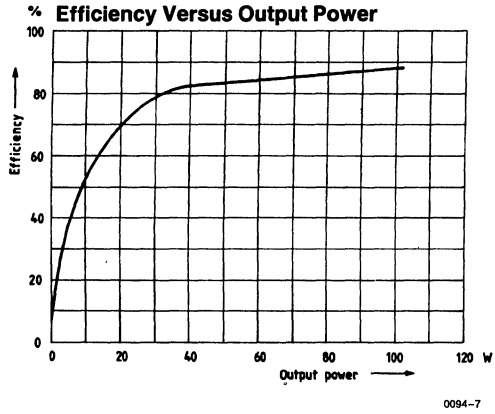
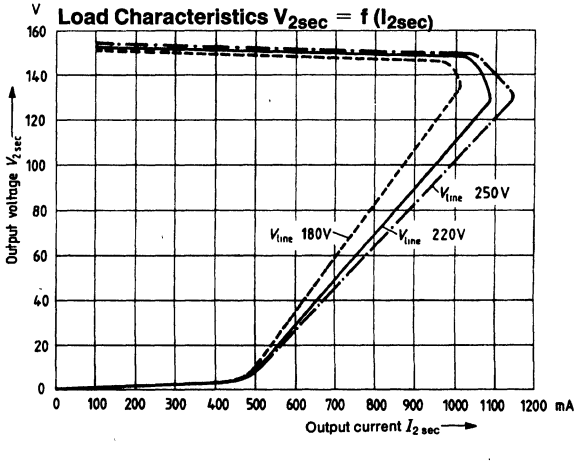
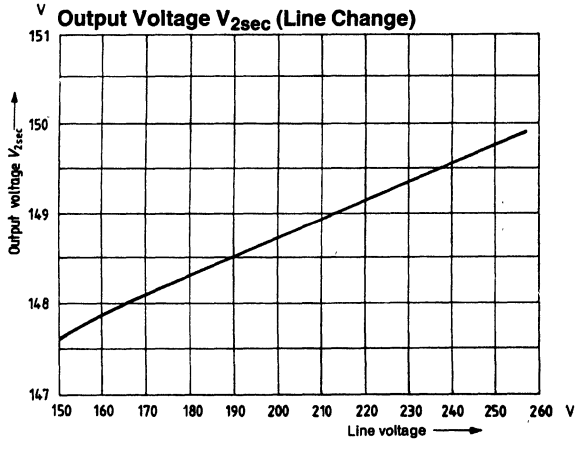
Supplements to Test and Measurement Circuit 2

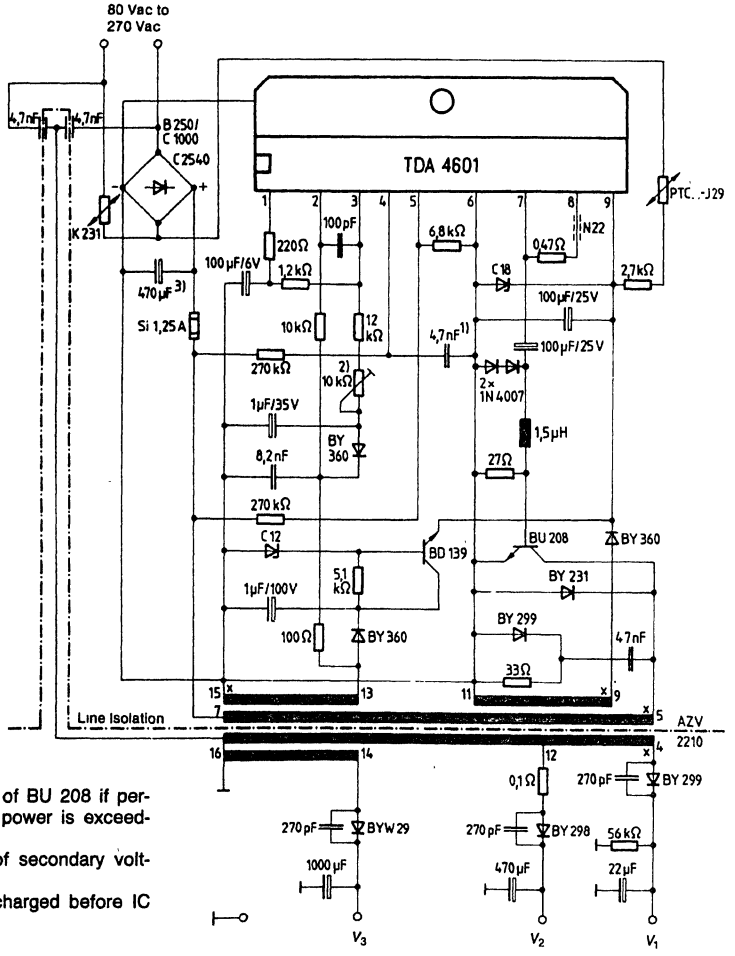








Application Circuit 2 Wide Range from 80 Vac to 270 Vac



Notes:
1. Limits $I_{C\ max}$ of BU 208 if permissible output power is exceeded.
2. Adjustment of secondary voltage.
3. Must be discharged before IC change.

Notes on application circuit 2

Wide Range SMPS

Filtering of the rectified AC voltage has been increased up to 470 µF to ensure an constant and hum-free supply at V_{line} = 80 Vac. The stabilized phase is tapped for supplying the IC. In order to ensure good start-up conditions for the SMPS in the low voltage range, the non-stabilized phase of winding 13/15 is used as a starting aid (BD 139), which is turned off after start-up by means of Z diode C12.

In comparison to the 22 Vac standard circuit, however, the collector-emitter circuit had to be altered to improve the switching behavior of BU 208 for the entire voltage range (80 Vac to 270 Vac). Diode BY 231 is necessary to prevent inverse operation of BU 208 and may be integrated for switching times with a secondary power <75W (BU 208 D).

Compared to the IC TDA 4600-2, the TDA 4601 has been improved in turn-off during undervoltage at pin 5. The TDA 4601 is additionally provided with a differential amplifier input at pin 5 enabling precise turn-off at the output of pin 8 accompanied by hysteresis. For wide range SMPS, TDA 4601 is recommendable instead of TDA 4600-2. If a constant quality standard like that of the standard circuit is to be maintained, wide range SMPS (80 Vac to 270 Vac) with secondary power of 120W can only be implemented at the expense of time.

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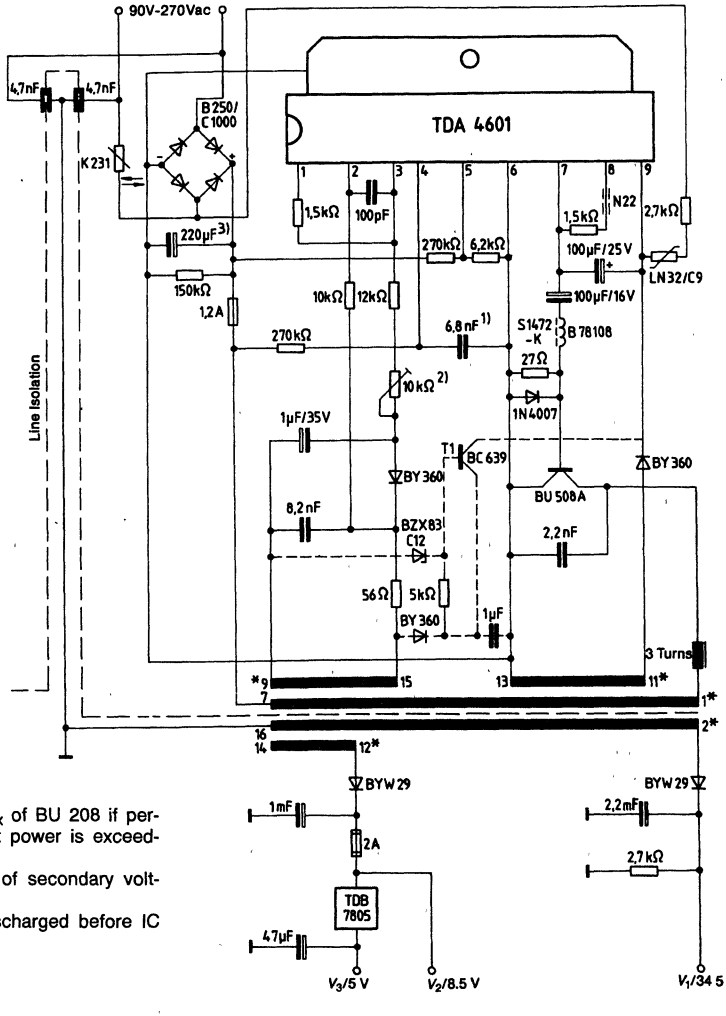
Further Application Circuits

Application Circuit 3



Notes:
1. Limits $I_{C\ max}$ of BU 208 if permissible output power is exceeded.
2. Adjustment of secondary voltage.
3. Must be discharged before IC change.

Notes on application circuit 3

Fully Insulated, Clamp-Contacted PTC Thermistor Suitable for SMPS Applications at Increased Start-Up Currents

The newly developed PTC thermistor **Q63100-P2462-J29** is designed for applications in SMPS as well as in various other electronic circuits, which, for example, receive the supply voltage directly from the rectified line voltage and require an increased current during turn-on. Used in the flyback converter power supply of TV sets, an application proved millions of times over, the new PTC thermistor in the auxiliary circuit branch has resulted in a power saving of no less than 2W. This increase in efficiency has a highly favorable effect on the standby operation of TV sets.

The required turn-on current needs only 6s to 8s until the operating temperature of the PTC thermistor is reached. Low thermal capacitance of the PTC thermistor allows the circuit to be operated again after no more than 2s. Another positive feature is the improved short-circuit strength. The clamp contacts

permit more or less unlimited switching operations and thus guarantee high reliability. A flame-retardant plastic package and small dimensions are additional advantages of this newly developed PTC thermistor.

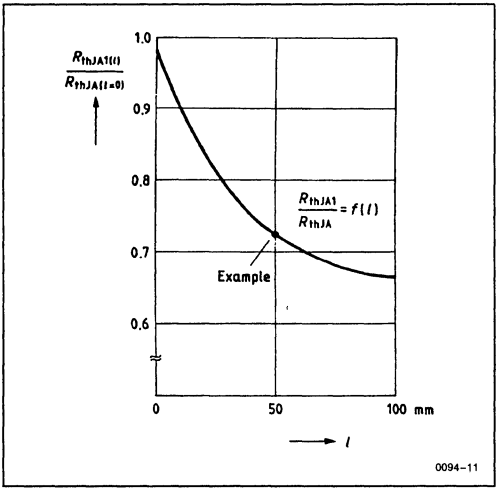
Technical Data

Breakdown Voltage at
T_A = 60°C ($V_{BR\ rms}$) 350V
Resistance at T_A = 25°C (R_{25}) ..... 5 kΩ
Resistance Tolerance (ΔR_{25}) 25%
Trip Current (Typ) (I_K) ..... 20 mA
Leakage Current at $V_{A\ max}$ (I_{lk}) ..... 2 mA
Max. Application Voltage ($V_{op\ max\ rms}$) 265V
Reference Temperature (typ) (T_{ref}) ..... 190°C
Temperature Coefficient (typ) (TC) ..... 26 %/K
Max. Operating Current (I_{max}) 0.1A
Storage Temperature
Range (T_{stg}) ..... −25°C to +125°C

Thermal Resistance

Standardized, ambient-related thermal resistance R_{thJA1} lateral length l of a square copper-clad cooling area (35 µm copper cladding).

R_{thJA} (l = 0) = 60 K/W
$T_A \leq 70°C$
P_d = 1W
PC board in vertical position
Circuit in vertical position
Still air



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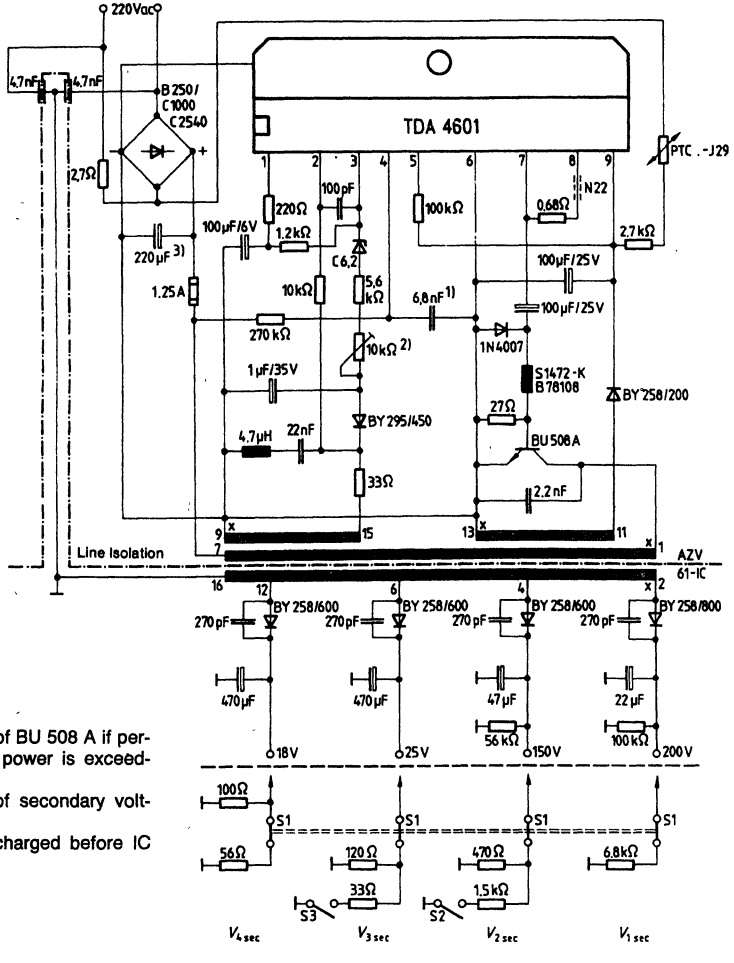
Application Circuit 4



Notes:
1. Limits $I_{C\,max}$ of BU 508 A if permissible output power is exceeded.
2. Adjustment of secondary voltage.
3. Must be discharged before IC change.

Notes on application circuit 4

Improved Load Control and Short-Circuit Characteristics

Turn-on is the same as for circuit 3.

To make the price more attractive, switching transistor BU 508 A was selected.

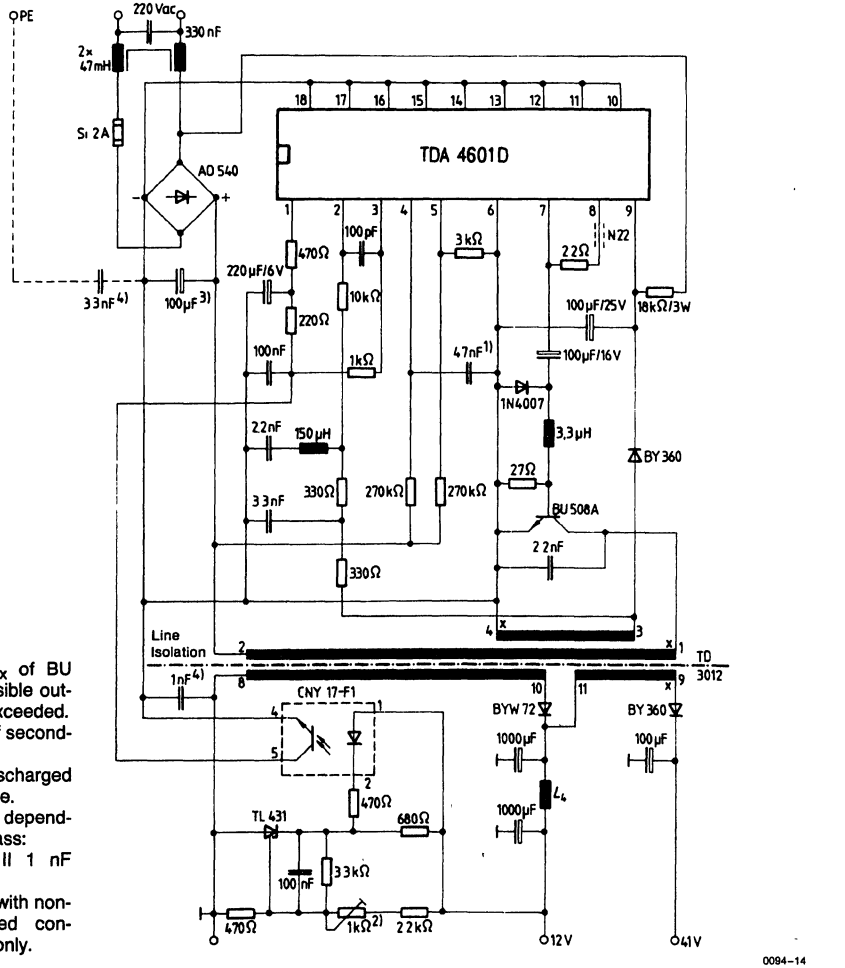
To ensure optimum standby conditions, the capacitance between pins 2 and 3 was increased to 100 pF.

Z diode C6.2 transfers control voltage ΔV_{cont} directly to pin 3 resulting in improved load control.

Design and coupling conditions of various flyback transformers were sometimes a reason for overshoot spectra, which, despite the RC attenuating element 33Ω x 22 nF and the 10 kΩ resistor, even penetrated across feedback winding 9/15 to the zero passage indicator input (pin 2) and activated double and multiple pulses in the IC. Double and multiple pulses, however, lead to magnetic saturation in the flyback transformer and thus increase the risk of damaging the switched-mode power supply.

These overshoots are produced in particular when high power is being carried, this occuring in the vicinity of the point of return. The switched-mode power supply, however, reduces its own power to a minimum for all cases of overload or short-circuit. A series resonant circuit, whose resonance corresponds

Application Circuit 5



Notes:

1. Limits $I_{C\ max}$ of BU 508 A if permissible output voltage is exceeded.
2. Adjustment of secondary voltage.
3. Must be discharged before IC change.
4. Optional use, depending on safety class:
   Safety Class II 1 nF only.
   Safety Class I with non-fused grounded conductor 3.3 nF only.

to the transformer's self-oscillation, was created through combination of the 4.7 µH inductance and the 22 nF capacitance. This resonant circuit short-circuits overshoots via a 33Ω resistor.

$$\left(f = \frac{1}{2\pi\sqrt{LC}} \approx 500\ \text{kHz}\right)$$

Notes on application circuit 5

Highly Stable Secondary Side

Power supplies for commercial purposes require highly constant low voltages and high currents which, on the basis of the flyback converter principle, can be realized only under certain conditions, but, on the other hand, are implemented for economical reasons. An electrically isolated flyback converter with a highly stable secondary side must receive the control information from this secondary side. There are only two possibilities of meeting this requirement: either through a transformer which is magnetically isolated from the flyback converter or by means of an optocoupler. The development of CNY 17 has enabled the manufacture of a component suitable for electrical isolation and characterized by high reliability and long-term stability.

IC TDA 4601 D is the successor of the TDA 4600 D. It is compatible with its predecessor in all operational functions and in the control of a self-oscillating flyback converter. Pin 3 is the input for the control information, where the latter is compared with the

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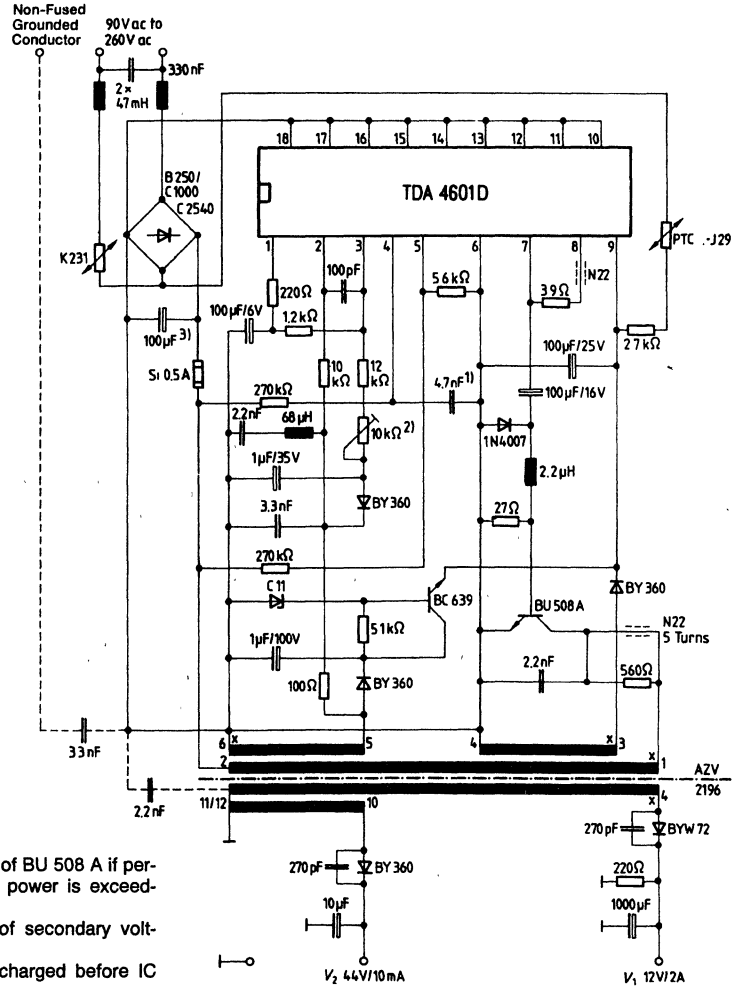
Application Circuit 6



Notes:

1. Limits $I_{C\ max}$ of BU 508 A if permissible output power is exceeded.
2. Adjustment of secondary voltage.
3. Must be discharged before IC change.

reference voltage prevailing at pin 1 and the control information from the optocoupler and subsequently transformed into a frequency/pulse width control.

The previous feedback and control information winding is not necessary. The feedback information (zero passage) is obtained from winding 3/4—supply winding. The time constant chain 330Ω/3.3 nF and 330Ω/2.2 nF was implemented in series with 150 µH to prevent interference at pin 2. The LC element forms a series resonant circuit for overshoots of the flyback converter and short-circuits them.

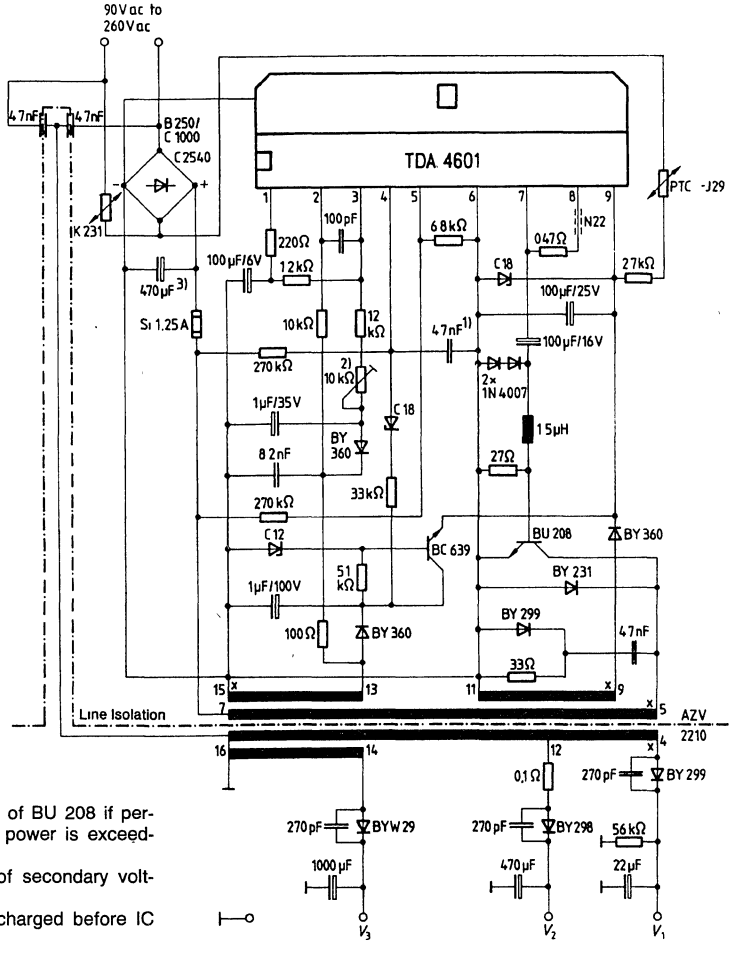
Notes on application circuit 6

Wide Range Plug SMPS up to 30W

Due to their volume and weight, plug SMPS were so far limited to a restricted primary voltage and a secondary power of no more than 6W.

The line-isolated wide range flyback converter presented here has a variable frequency and is capable of producing a secondary power of 30W. It is characterized by a compact design with an approx. weight of 400g. The entire line voltage range of 90 Vac to 260 Vac is stabilized by to ±1.5% on the secondary side. Load fluctuations between 0.1A and 2.0A are regulated to within 5%. The output (secondary side) is overload, short-circuit, and open-loop-proof.

Application Circuit 7



Notes:
1. Limits $I_{C\ max}$ of BU 208 if permissible output power is exceeded.
2. Adjustment of secondary voltage.
3. Must be discharged before IC change.

0094-16

Notes on application circuit 7

Wide Range—SMPS with Reducing Peak Collector Current $I_{CBU\ 208}$ for Rising Line Voltage (Variable Point of Return)

Wide range SMPS have to be dimensioned at line voltages of 90 Vac to 260 Vac. The difference between the maximum collector current $I_{C\ BU\ 208\ max}$ and the largest possible limit current $I_{C\ BU\ 208\ limit}$ which causes magnetic saturation of the flyback transformer and flows through the primary inductance winding 5/7 is to be determined at Vac_{min} ($I_{C\ BU\ 308\ limit} \geq 1.2 \times I_{C\ BU\ 208\ max}$). Then, the transmissible power of the flyback transformer and its value at Vac_{max} is to be determined. In the standard circuit the collector current $I_{CBU\ 208\ max}$ is almost constant at the point of return independently of the line voltage. The transmissible power on the secondary side, however, increases at the point of return in proportion to the rising rectified line voltage applied (Figures 1 and 2).

In the wide range SMPS a line voltage ratio of 270/90 = 3/1 is obtained causing doubling of the transmissible power on the secondary side, i.e., in the wide range SMPS a flyback transformer had to be implemented that was much too large.

The point of return protecting the SMPS against overloads or short circuits, is derived from the time constant at pin 4. $\tau_4 = 270\ k\Omega \times 4.7\ nF$. Thus, the largest possible pulse width is determined.

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With the introduction of the 33 kΩ resistor this time constant is reduced as a function of the control voltage applied to winding 13/15, rectified by diode BY 360 and filtered by the 1 μF capacitance, which means that the pulse time becomes shorter. By means of the Z diode C18 the line voltage level can be defined at which the influence of the time constant correction becomes noticeable. The change in the rectified voltage of winding 13/15 is proportional to the change in the rectified line voltage.

At the point of return $I_{C\ BU\ 208}$ the peak collector current has been reduced with the aid of the given values from 5.2A at 90 Vac to 3.3A at 270 Vac. The transmissible power at the point of return remains stable between 125 Vac and 270 Vac due to the set activation point of the point of return correction (unbroken curve in Figure 2).

Load Characteristic

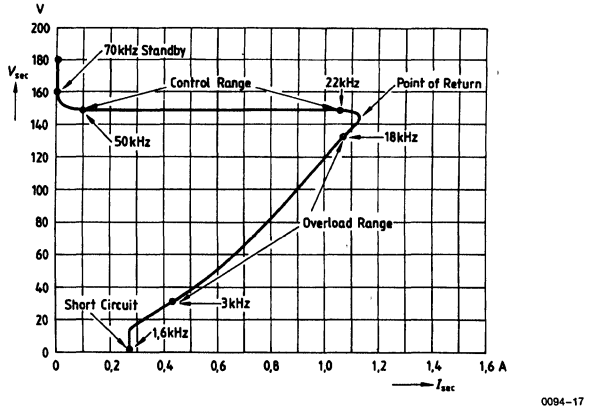


Figure 1

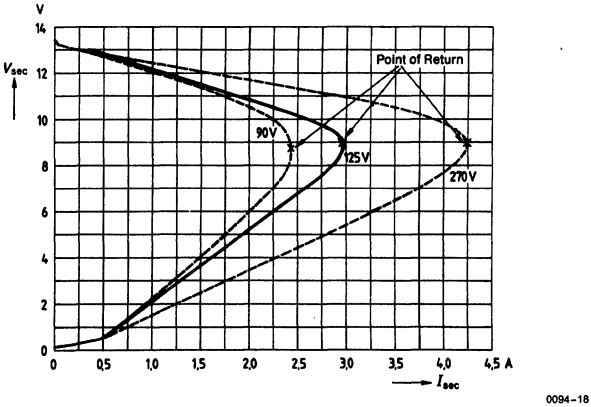


Figure 2

Ordering Information

Type	Ordering Code	Package
TDA 4601	Q67000-A2379	SIP 9
TDA 4601 D	Q67000-A2390	DIP 18 L9 (Pin 6 and Pins 10 to 18 Grounded)

SIEMENS

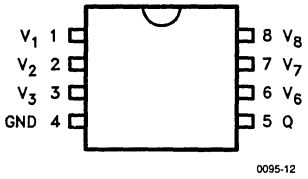
Preliminary

TDA 4605
SMPS IC for Control of SIPMOS Transistors

- Direct Control of the Switching Transistor
- Reversing Linear Overload Characteristic

Pin Configuration

(Top View)



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Pin Description

Pin	Designation	Function
1	Control Voltage	Information input for secondary voltage. By comparison of the control voltage derived from the control winding of the transformer with the internal reference voltage the output pulse width at pin 5 is matched to the load on the secondary side (normal, overload, short-circuit, open-circuit).
2	Primary-Current Simulation	Information input for primary voltage. The primary-current rise in the primary winding is simulated as a voltage rise at pin 2 by means of an external RC network. When a value derived from the control voltage at pin 1 is reached, the output pulse at pin 5 is terminated. The maximum power in the point of return is set with the RC network.
3	Undervoltage Detector	Input for primary-voltage monitoring. The IC is cut out upon line undervoltage by comparison with an internal reference. The voltage at pin 3 is used for point-of-return correction.
4	Ground	
5	Output	Push-pull C output supplies ±1.5 A for fast charge reversal of the gate capacitances of the power MOS transistor.
6	Supply Voltage	Input for the supply voltage. From this a stable internal reference V_{REF} and the switching thresholds V_{6A}, V_{6E}, V_{6max} and V_{6min} for monitoring of the operating voltage are derived. V_{REF} is turned on for $V_6 < V_{6E}$ and turned off for $V_6 < V_{6A}$. The logic is only enabled for $V_{6min} < V_6 < V_{6max}$.
7	Point-of-Return Correction	Input for point-of-return correction. The network on this pin to ground influences internal correction (slope and response).
8	Zero-Passage Detector	Input for oscillator feedback. After build-up each zero passage of the feedback voltage (falling edge) triggers an output pulse at pin 5. The trigger threshold is typ. + 50 mV.

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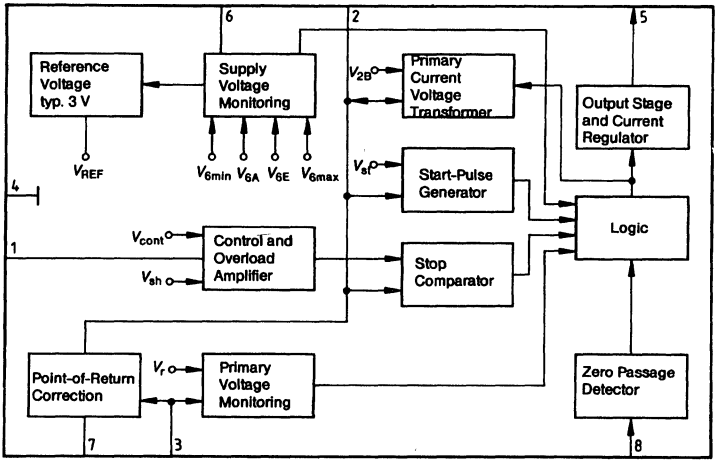
This IC is designed for controlling an MOS power transistor and performing all necessary protective and control functions in self-oscillating flyback converter power supplies. Owing to the IC's outstanding voltage stability, which is maintained even at substantial fluctuations, the IC is suited for consumer as well as for industrial applications.

Block Diagram



Functional Description

The power transistor and primary winding of the flyback transformer, which are connected in series, receive direct supply of the input voltage. During the on-phase of the transistor, energy is stored in the primary winding and during the off-phase it is released to the consumer via the secondary winding. The IC controls the power transistor in such a way that the secondary voltages are kept at constant values independently of input or load changes. The control information required is obtained from the input voltage during the on-phase and from a control winding (secondary winding) during the off-phase. Load differences are compensated by altering the frequency, input voltage fluctuations are additionally counteracted by altering the pulse duty factor. This results in the following load-dependent modes of the SMPS:

— Open-loop or small load: Output voltage slightly above set value

— Control: Load-independent output voltage

— Overload: In case of overload or short-circuit, the secondary voltage is decreased from the point of return as a function of the load current, following a reversing characteristic

Typical values of pulse duty factor v, switching frequency f and duration of primary phase t of the power transistor:

Mode	v	f/KHz	t/µs
Open-Loop	0.1	150	0.7
Small Load (5W)	0.33	80	2.5
Control Mode (30W–100W)	0.33	40	5.6
Reversing Point 150W	<0.5	20	<25
Short-Circuit	0.02	1.5	<15

Description of Operation

A flyback converter designed for color TV sets, applicable between 30W and 120W and for line voltages ranging from 90V to 140V, is shown in one of the following figures. On the subsequent pages the major pulses can be found.

The line voltage is rectified by bridge rectifier Gr1 and smoothed by C_3.

During start-up the IC current is supplied via resistors R_2 and R_3, and in the post-transient condition it is additionally supplied via winding 13/11 and rectifier D3. The size of filter capacitor C_6 determines the turn-on behavior.

Switching transistor T1 is a BUZ 45. Parallel capacitance C_9 and primary winding 1/7 form a resonant circuit, thus limiting the frequency and amplitude of drain-source voltage overshoots during turn-off of T1. Self-oscillation is attenuated by R_{14}. Diode D5 limits positive overshoots. R_{12} prevents static charging of the gate of T1. D1 improves the turn-off be-

havior. The current rise in T1 is determined by the inductance of the primary winding. This sawtooth-shaped rise is simulated at network R_7 C_4 and applied to pin 2 of the IC.

Depending on the dimensioning of the primary inductance, timing element R_7C_4 is to be adapted to the current rise angle in T1. Thus, during the on-phase, the IC receives the control information in the form of the simulated energy content of the primary winding at pin 2 as a function of line voltage versus time.

The control deviation at pin 1 is recorded by control winding 9/15. This measure requires fixed coupling with the secondary winding 2/16. The control winding is also used for feedback and permits self-oscillation of the parallel circuit C_9/primary inductance if the power transistor is inhibited. Thus, the maximum possible open-loop frequency is determined.

The control voltage required for pin 1 is rectified by diode D4 and smoothed by capacitor C_7. Furthermore, R_{13} and C_8 form a timing element, which serves for filtering fast changes in the control voltage, i.e. the final element does not become active until several periods have occurred. By means of the voltage divider formed of resistors R_8, R_9, R_{10}, the secondary voltage can be set. Reason: in the IC the control voltage produced at pin 1 is compared with a stable, internal reference voltage.

According to the result of this comparison, frequency and pulse duty factor are corrected until the secondary voltage selected by R_{10} has established itself. For all operating modes of the SMPS, the zero passages of the voltage at the control winding contain information on pulse duty factor and switching frequency of the switching transistor T1, or the open-loop frequency. Conditioning of the corresponding signal at pin 8 is performed by series resistor R11 and by integrated limiter diodes.

An SMPS based on these principles would have a point of return dependent on the line voltage. With respect to the distance to the saturation point, the transformer must be dimensioned for maximum power, i.e. for maximum line voltage and the power then occurring at the point of return.

In order to keep the size of the transformer as small as possible, the IC makes the point of return largely independent of the rectified line voltage. If necessary, the reverse point correction of the IC can be altered by a network from pin 7 to ground. The information on the line voltage is applied to pin 3. Before the line voltage falls below its minimum value, the SMPS must be turned off by the IC in order to obtain defined turn-off conditions.

During undervoltage, the information required for turn-off is applied to pin 3 via the resistive divider R_4/R_5. On the secondary side the output voltages $V_{1\ sec}$ to $V_{4\ sec}$ are available. If the secondary side is further deloaded, standby is set automatically. Resistor R_{15} forms a basic load of voltage $V_{1\ sec}$ and contributes to maintaining standby conditions (V_{sec} rise 20%). Capacitors C_{10} and C_{13} prevent spikes generated by reversing the rectifiers D7 through D9. The secondary voltages are smoothed by charging electrolytic capacitors C_{14} through C_{17}.

1.0 Start-up Behavior

In Figure 1, the start-up behavior of the application circuit is illustrated for a line voltage that is barely above the value for undervoltage.

After application of the line voltage at the point in time t_0, the following voltages build up:

— V_6 according to the halfwave charge across R_2 and R_3

— V_2 to $V_{2\ max}$ (typ. 6.2V)

— V_3 to the value given by divider R_4/R_5.

The current consumption of the IC in this mode of operation is smaller than 1.5 mA. When V_6 reaches the threshold V_{6E} (time t_1), the IC turns on the internal reference voltage. The current consumption increases to typically 12 mA. The primary-current voltage transformer reduces V_2 to V_{2B} and between time t_5 and t_6 the start-pulse generator will produce the start pulse. The feedback at pin 8 starts the next pulse and so on. All pulses, including the start pulse, are controlled in width by the control voltage at pin 1. Upon turn-on this corresponds to the case of short-circuit, i.e. V_1 = 0V. Thus, the IC starts with "short-circuit pulses" that widen according to the feed-back control voltage. The IC operates in the point of return. Afterwards the peak values rapidly drop to V_2 because the IC is operating in the control range. The control loop is stabilized. If voltage V_6 falls below the output threshold V_{6min} before the point of return is reached, the start will be interrupted (pin 5 goes Low). The IC remains turned on, so V_6 drops further to V_{6A}. Then the IC turns off, V_6 can build up again (time t_4) and a new turn-on attempt begins at time t_1. If the rectified line AC voltage (primary voltage) breaks down because of the load, V_3 can, as happens at time t_3, fall below V_{3A} (turn-on attempt with undervoltage). The primary-voltage monitoring then clamps V_3 to V_{3S} until the IC turns off ($V_6 < V_{6A}$). Then a new turn-on attempt is started at time t_1.

2.0 Control, Overload and Open-Circuit Behavior

When the IC has started up, it operates in the control range. The voltage on pin 1 is typically 400 mV.

When the output is loaded, the control amplifier permits wider charge pulses (V_5 = H). The peak value of the voltage at pin 2 increases to $V_{25\ max}$. If the secondary load is increased further, the overload amplifier will start to reduce the pulse width. Because the change in pulse width reverses, this is called the point of return of the power supply. The IC supply voltage V_6 is directly proportional to the secondary voltage, so it breaks down according to the overload control response. If V_6 falls below the value $V_{6\ min}$, the IC will go into sampling operation. The time constant of the halfwave start-up is relatively large, so the short-circuit power remains small. The overload amplifier reduces to the pulse width t_{psh}. This pulse width must remain possible so that the IC can start without any problems from the virtual short-circuit, i.e. the turn-on with V_1 = 0.

If the load is reduced on the secondary side, the charge pulses (V_5 = H) become narrower. The frequency increases up to the natural frequency of the system. If the load is reduced further, the secondary voltages build up to V_6. At V_6 = $V_{6\ max}$ the logic is blocked. The IC goes into sampling operation. Thus the circuit is absolutely open-circuit-proof.

3.0 Overtemperature Response

An integrated temperature cutout blocks the logic if the chip temperature becomes inadmissibly high. The IC automatically samples the temperature and starts as soon as it drops to an admissible level.

Absolute Maximum Ratings*

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter	Symbol	Limits		Units	Remarks
		Min	Max		
Voltages					
Pin 1	V_1	−0.3	+3	V	
Pin 2	V_2	−0.3		V	
Pin 3	V_3	−0.3		V	
Pin 5	V_5	−0.3	V_6	V	
Pin 6	V_6	−0.3	+20	V	Supply Voltage
Pin 7	V_7	−0.3		V	
Pin 8	V_8	−0.3		V	
Currents					
Pin 1	I_1	−3	+1	mA	
Pin 2	I_2	−3	+3	mA	
Pin 3	I_3	−3	+3	mA	
Pin 4	I_4	−1.5		A	$t_p \leq 50\ \mu s;\ \nu \leq 0.5$
Pin 5	I_5	−1.5	+1.5	A	$t_p \leq 50\ \mu s;\ \nu \leq 0.5$
Pin 6	I_6	−0.01	+1.5	A	$t_p \leq 50\ \mu s;\ \nu \leq 0.5$
Pin 7	I_7	−3	+1	mA	
Pin 8	I_8	−3	+3	mA	
Junction Temperature	T_J		125	°C	
Storage Temperature Range	T_{stg}	−40	+125	°C	
Thermal Resistances Junction-Air Junction-Case Measured at Pin 4	 R_{thJA} R_{thJC}		 100 70	 K/W K/W	
Operating Range					
Supply Voltage	V_6	7.5	15	V	
Case Temperature	T_C	−20	+85	°C	

Characteristics $T_A = 25°C$

Parameter	Symbol	Measurement Circuit	Limits			Units
			Min	Typ	Max	
Start-Up Hysteresis						
Start-Up Current Consumption $V_6 = 5V$	$I_{6/5}$	1		0.5	0.75	mA
Start-Up Current Consumption $V_6 = 8V$	$I_{6/8}$	1		1	1.5	mA
Turn-On Voltage	V_{6E}	1	11	12	13	V
Turn-Off Voltage	V_{6A}	1	6	6.5	7	V
Turn-On Current $V_6 = V_{6E}$	I_{6E}	1		12	16	mA
Turn-Off Current $V_6 = V_{6A}$	I_{6A}	1		10		mA
Voltage Limiter ($V_6 = 10V$, IC Turned Off) at Pin 2 ($V_6 < V_{6E}$) $I_2 = 1$ mA	V_{4max}	1	5.6	6.6	7.6	V
Voltage Limiter ($V_6 = 10V$, IC Turned Off) at Pin 3 ($V_6 < V_{6E}$) $I_3 = 1$ mA	V_{5max}	1	5.6	6.6	7.6	V
Control Range						
Control Input Voltage	V_{1cont}	2		400		mV
Gain in Control Range $G_{cont} = \frac{d(V_{2S} - V_{2B})}{dV_1}$	G_{cont}	2		−400		mV
Primary-Current Simulation Voltage						
Basic Value	V_{2B}	2		1		V
Maximum Peak Value $G_1 = V_{1cont}(2\ V/V_{cont})$	$V_{2S\ max}$	2		3		V
Overload and Short-Circuit Operation						
Overload Range Upper Limit	V_{1U}	2		400		mV
Overload Range Lower Limit	V_{1L}	2		150		mV
Gain in Overload Range $G_{over} = \frac{d(V_{2S} - V_{2B})}{dV_1}$	G_{over}	2		2		
Input Voltage in Overload Range $V_{cont} = 3.5V$	V_1	2		360		mV
Input Current in Short-Circuit Operation $V_{cont} = 0V$	I_1	2		−140		μA

Characteristics T_A = 25°C (Continued)

Parameter	Symbol	Measurement Circuit	Limits			Units
			Min	Typ	Max	
Overload and Short-Circuit Operation (Continued)						
Peak Value in Overload Range V_{cont} = 3.5V	V_{2over}	2		3.0		V
Peak Value in Short-Circuit Operation V_{cont} = 0V	V_{2sh}	2		2.7		V
Output Pulse Width in Overload Range V_{cont} = 3.5V	$t_{p\ over}$	2		8.5		µs
Output Pulse Width in Short-Circuit Operation V_{cont} = 0V	$t_{p\ sh}$	2		7.5		µs
Current Consumption in Overload Range V_{cont} = 3.5V	I_6	2		12		mA
Current Consumption in Short-Circuit Operation V_{cont} = 0V	I_6	2		10		mA
Generally Valid Data (V_6 = 10V)						
Point-of-Return Correction						
Point-of-Return Correction Voltage V_3 = 5V; V_2 = 0V	V_7	2		5		V
Point-of-Return Correction Current V_3 = 5V; V_2 = 0V	V_4	1		−460		µA
Zero-Passage Detector Voltage						
Positive Value	V_{8P}	2		0.7		V
Negative Value	V_{8N}	2		−0.2		V
Delay between V_8 and V_2	t_{d4}	2		2		µs
Output-Stage Data						
Saturation Voltages						
S in Setting 1 of Upper Transistor I_5 = −1.5A	V_{satU}	1		2		V
S in Setting 1 of Lower Transistor I_5 = +1.5A	V_{satL}	1		2		V
Slew Rate of Output Voltage						
Rising Edge V_{cont} = 3.5V	$+dV_5/dt$	2		10		V/µs
Falling Edge V_{cont} = 3.5V	$-dV_5/dt$	2		50		V/µs

Characteristics T_A = 25°C (Continued)

Parameter	Symbol	Measurement Circuit	Limits			Units
			Min	Typ	Max	
Protective Circuits						
1. Undervoltage protection for V_6: Voltage on Pin 5 = V_{5min} When $V_6 < V_{6min}$ (With $V_{6min} = V_{6A} + \Delta V_6$)	ΔV_6	2	0.3	0.5	1	V
2. Overvoltage Protection for V_6: Voltage on Pin 5 = V_{5min} When $V_6 < V_{6min}$	V_{6max}		14	15	16	V
3. Undervoltage Protection for V_{line}: Voltage on Pin 5 = V_{5min} When $V_3 > V_{3A}$, $V_2'' = 0V$	V_{3A}	1		1		V
4. Overtemperature: Chip Temperature at Which IC Switches V_5 to V_{5min}	T_J	2		125		°C
Voltage on Pin 3 after Response of Protective Function (V_3 is Clamped Until $V_6 < V_{6A}$) I_3 = 3 mA	V_3	1		0.2	0.4	V
Sampling Current Consumption $V_3 = V_2 = 0V$	I_6	1		12		mA
Normal Operation (V_{line} = 220V; S1, S2, S3, S4 closed)						
1. Secondary Voltage	V_{1S}	3		95		V
2. Secondary Voltage	V_{2S}	3		26		V
3. Secondary Voltage	V_{3S}	3		15		V
4. Secondary Voltage	V_{4S}	3		8.5		V
Turn-On Time for Secondary Voltages	t_{on}	3		120		ms
Voltage Alteration between S5 Open and S5 Closed	ΔV_{1S}	3		100	500	mV
Load Variation Cross-Talk Voltage Alteration between S6 Open and S6 Closed	ΔV_{1S}	3		500	1000	mV
Standby Operation (V_{line} = 220V; $P_{sec} \leq$ 2W)						
Voltage Build-Up	δV_{1S}	3		20	30	V
Frequency	f	3	75	80		KHz
Power Consumption	P_{prim}	3		10	15	VA
Point-of-Return Stability						
Maximum Secondary Current (secondary point of return) S1 Closed I_{1Smax} is set with R_{17} V_{1S} = 85V	I_{1Smax}	3		1.85		A
Relative Alteration of I_{1Smax} 80V < V_{line} < 140V	ΔI_{1Smax}	3			±10	%

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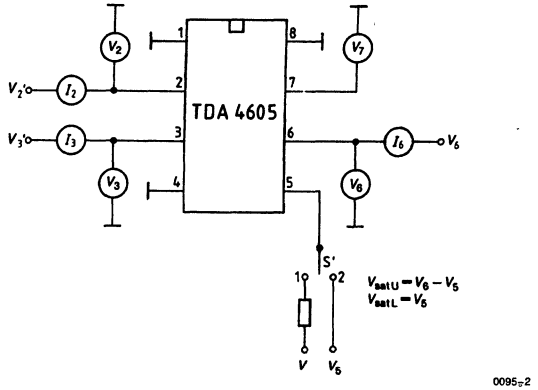
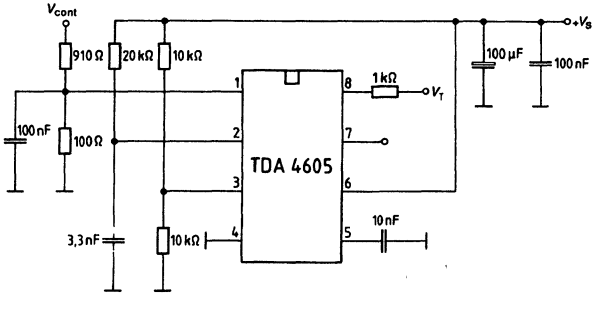
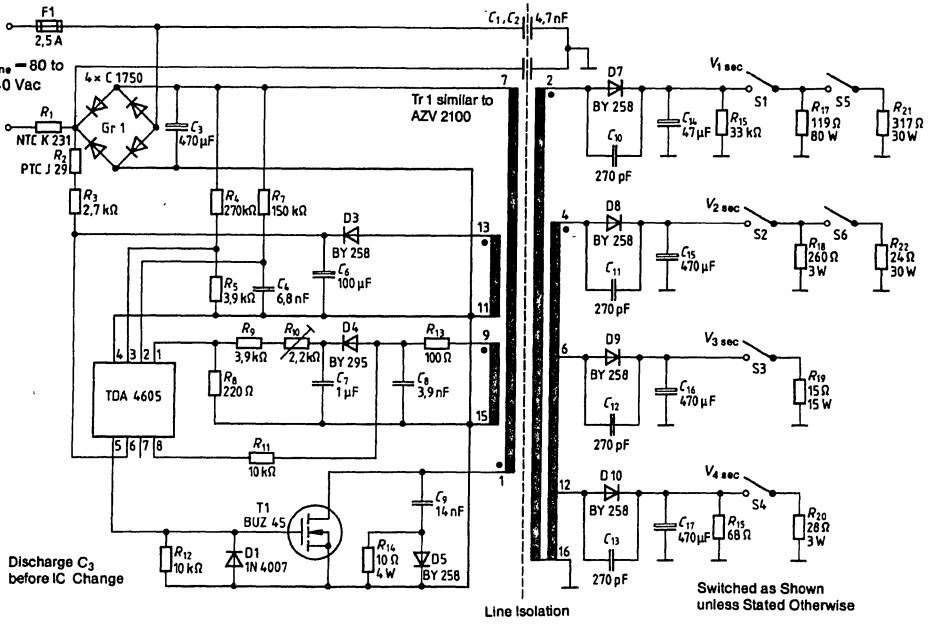
Measurement Circuit 1



Measurement Circuit 2



Measurement Circuit 3



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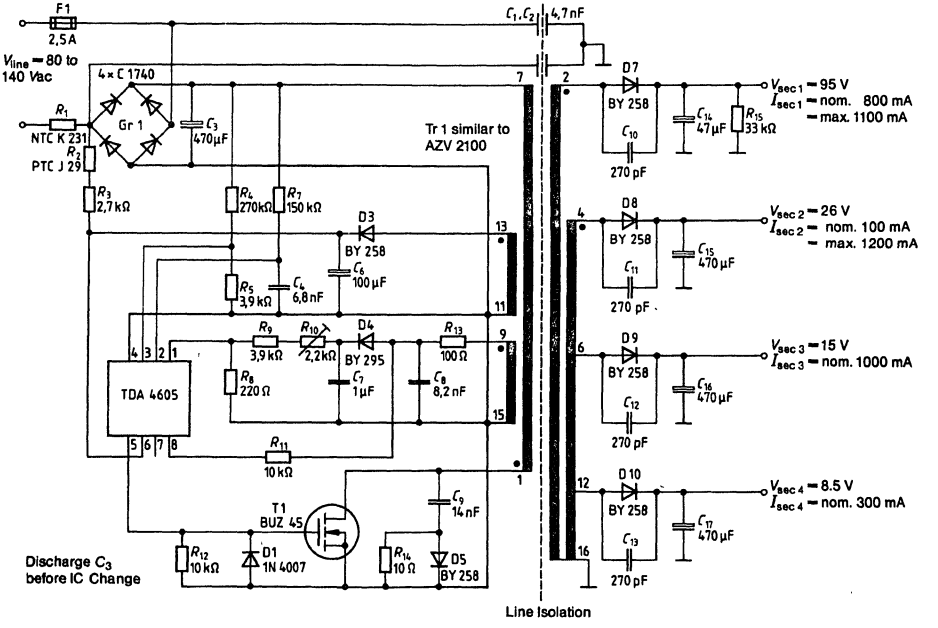
Application Circuit



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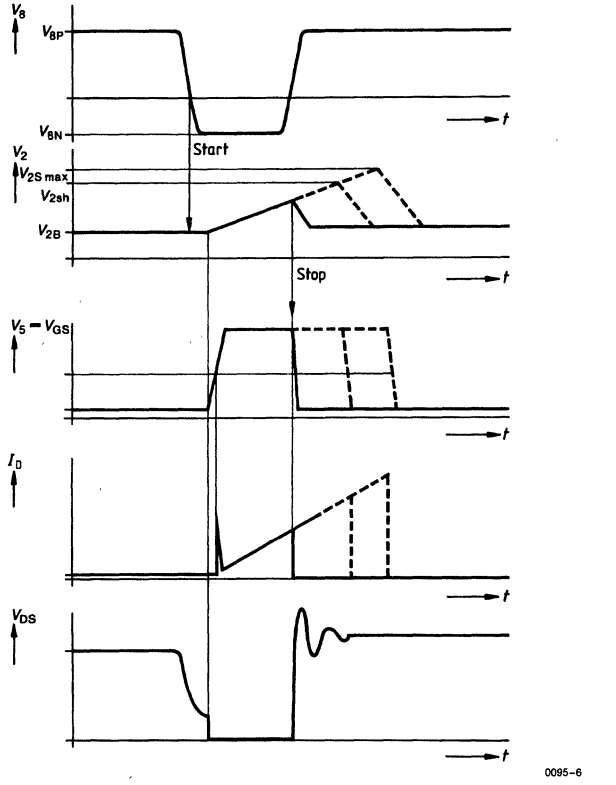


Figure 1

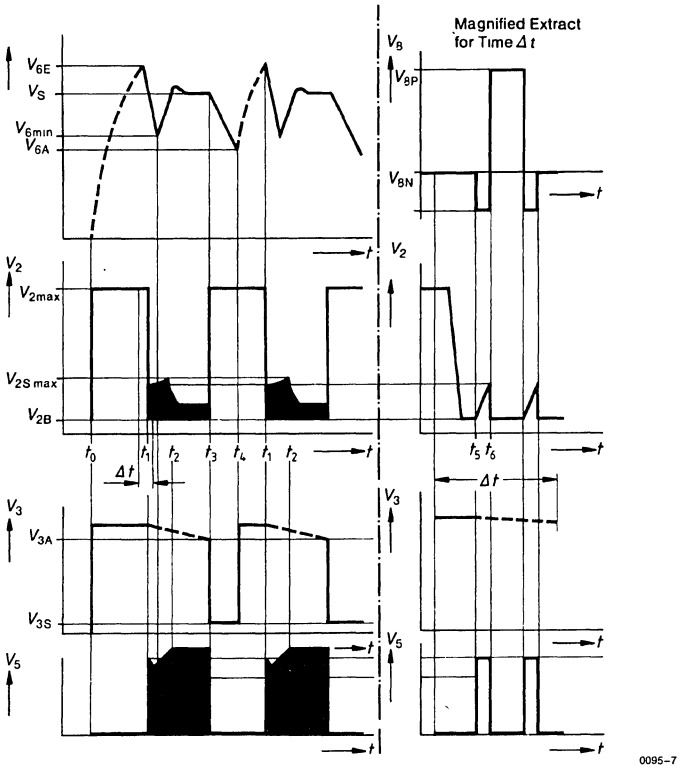
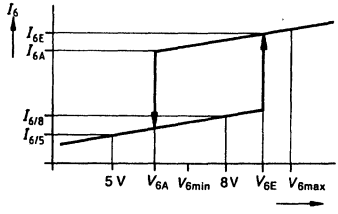
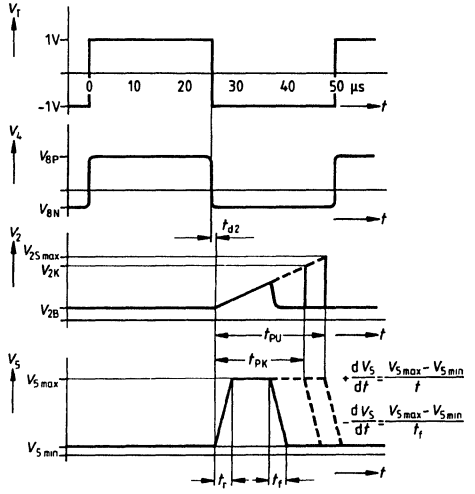

Magnified Extract
for Time Δ t
V6E
VS
V6min
V6A
V2
V2max
V2S max
V2B
V3
V3A
V3S
V5
VB
VBP
VBN
t0
t1
t2
t3
t4
t1
t2
t5
t6
Δ t
0095-7

Figure 2

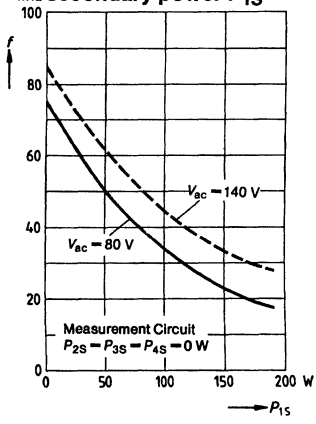
1. Start-Up Hysteresis



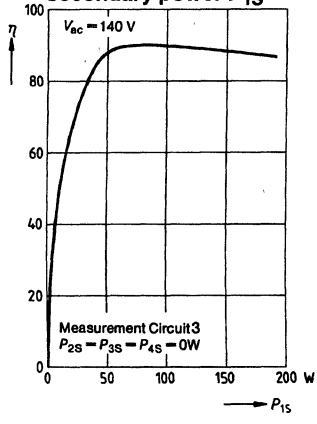
2. Operation in Measurement Circuit 2



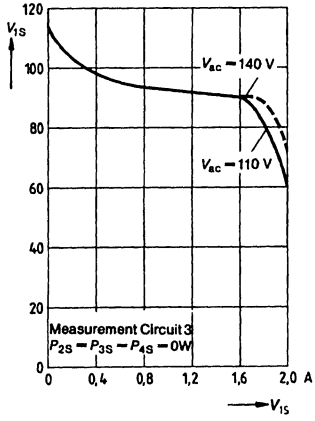
Frequency f versus kHz secondary power P_{1S}



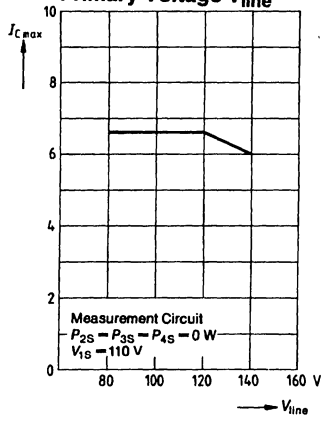
Efficiency η versus % secondary power P_{1S}



Secondary Voltage V_{1S} versus Secondary Current I_{1S}



Peak Collector Current $I_{C\,max}$ of Switching Transistor versus Primary Voltage V_{line}



0095-11

Ordering Information

Type	Ordering Code	Package
TDA 4605	Q67000-A8078	DIP 8

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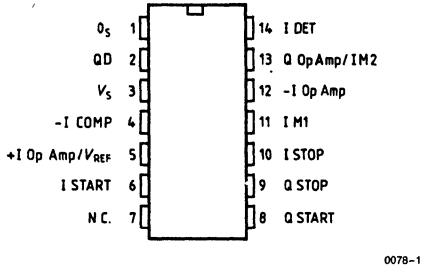
Preliminary

TDA 4814 A
IC for Active Line Filters

Pin Configuration

(Top View)



Pin Definitions

Pin	Symbol	Function
1	O_S	Ground
2	QD	Driver Output
3	V_S	Supply voltage
4	−I COMP	Negative Comparator Input
5	+I Op Amp/V_{REF}	Positive Input Op Amp/V_{REF}
6	I START	Start Input
7	N.C.	Not Connected
8	Q START	Start Output
9	Q STOP	Stop Output
10	I STOP	Stop Input
11	I M1	Multiplier Input
12	−I OP Amp	Negative Input Op Amp
13	Q Op Amp/I M2	Op Amp Output/Multiplier Input 2
14	I DET	Detector Input

This device contains the components for designing a switched-mode power supply with sinusoidal line-current consumption. Sinusoidal line current is drawn from the supply network in particular when there is high power consumption. One possible application is in electronic ballasts for fluorescent lamps, especially when a large number of these lamps are concentrated on one supply point. This IC is additionally suitable for general driving of switched-mode power supplies. The possibility for regulating the output voltage will enable operation on different line voltages (110 Vac/220 Vac) without any switchover.

A monitoring circuit makes it possible to control various turn-on and turn-off functions of different units of equipment.

Circuit Description

The IC switches from standby to full current consumption when the turn-on threshold on V_S is exceeded. Turn-off is controlled by hysteresis. The integrated Z diode limits the voltage on V_S when impressed current is fed.

The operational amplifier (op amp) can be wired as a control amplifier. It will then compare the divided output voltage V_Q to a reference voltage V_{REF} that is stable with temperature. The output voltage of the op amp that is produced in this way is multiplied by a sine-magnitude voltage in the multiplier (M). At the output of the latter a sine-magnitude voltage then appears that is variable in amplitude. This nominal voltage is applied to the plus input of the comparator. The nominal voltage at the multiplier output can then be compared via the comparator to a voltage derived from the actual line current. The output of the comparator feeds the reference signal via a logic circuit to the driver that switches the SIPMOS transistor. No current gaps may appear in the choke, otherwise the line current would no longer be sinusoidal. To achieve that, the detector input I DET senses when the choke current has fallen to zero after turn-off of the SIPMOS transistor. This ensures that the SIPMOS transistor does not turn on too early and that no current gaps occur.

When the detector input I DET is on High potential, the SIPMOS driver Q is blocked. At the same time the flipflop can be set by the comparator.

When I DET is Low, the Q output is enabled and can be disabled again by the comparator by resetting the flipflop.

Consequently the choke is always currentless when the SIPMOS transistor turns on and no current gaps appear in the choke.

Driver Output Q for SIPMOS Transistors

The output driver is designed as a push-pull stage. There is a resistor of 10Ω in series with the output for the purpose of current limiting. Between Q and ground there is a resistor of 10kΩ. This keeps the SIPMOS transistor reliably turned off during standby.

The Q output is additionally connected to the supply voltage V_S and to ground by way of diodes.

When the supply voltage to the switched-mode power supply is turned on, the diode towards V_S conducts the capacitive displacement currents from the gate of the SIPMOS transistor into the smoothing capacitor on V_S. The voltage V_S may not exceed 0.7V if the SIPMOS transistor is to remain turned off.

The diode towards ground clamps negative voltages on Q to −0.7V. Capacitive currents produced by voltage incursion on the drain of the SIPMOS transistor are thus able to flow away unhindered.

Reference Voltage (V_{REF})

The reference-voltage source is highly stable with temperature. It can be used if additional, external components are wired.

Monitoring Circuit (I START, I STOP, Q START, Q STOP)

The monitoring circuit guarantees the secure operation of a unit of equipment. Any circuitry that is shut down because of a fault, for instance, cannot be started up again until the monitoring start (I START/ Q START) has turned on and a positive voltage pulse has been impressed on Q START.

If there is a defect present, the monitoring stop (I STOP/Q STOP) will turn on and shut down either the entire unit or simply the circuitry that has to be protected. No restart is then possible until the hold current impressed on I START or I STOP has been interrupted (e.g., by a power-down).

Absolute Maximum Ratings*

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter	Symbol	Conditions	Limits		Units
			Min	Max	
Supply Voltage	V_S	. V_Z = Z Voltage	−0.3	V_Z	V
Inputs					
Comparator	$V_{I\ COMP}$ $V_{-I\ COMP}$		−0.3 −0.3	33 33	V V
Op Amp	$V_{I\ Op\ Amp}$ $V_{-I\ Op\ Amp}$		−0.3 −0.3	6 6	V V
Multiplier M1	V_{M1}		−0.3	33	V
Output Op Amp	$V_{Q\ Op\ Amp}/I_{M2}$		−0.3	6	V
Z Current V_S GND	I_Z	Observe P_{max}	0	300	mA
Driver Output	V_Q		−0.3	V_S	V
Q Clamping Diodes	I_{QD}	$V_Q > V_S$ or $V_Q < -0.3V$	−10	10	mA
Input START STOP	$V_{I\ START}$ $V_{I\ STOP}$	See Characteristics See Characteristics	−0.3 −0.3	25 33	V V
Output START STOP	$V_{Q\ START}$ $V_{Q\ STOP}$		−10 −0.3	3 6	V V
Detector Input	$V_{I\ DET}$		0.9	6	V
Detector Clamping Diodes	$V_{I\ DET}$	$V_{I\ DET} > 6V$ or $V_{I\ DET} < 0.9V$	−10	10	mA
Capacitance at I START to Ground	$C_{I\ START}$			150	µF
Junction Temperature	T_j			125	°C
Storage Temperature	T_{stg}		−55	125	°C
Thermal Resistance System-Air	$R_{th\ SA}$			65	K/W
Operating Range					
Supply Voltage	V_S	Values for $V_{S\ ON}$, V_Z See Characteristics	$V_{S\ ON}$	V_Z	V
Z Current	I_Z	Observe P_{max}	0	200	mA
Driver Current	I_{QD}		−300	+300	mA
Operating Temperature	T_A		−25	+85	°C

Characteristics ($V_{S\,ON}$* < V_S < V_Z; − 25°C < T_A < +85°C)

Parameter	Symbol	Limits			Units
		Min	Typ	Max	
Current Consumption					
Without Load on Driver Q and V_{REF}; Q Low 0V < V_S < $V_{S\,ON}$ $V_{S\,ON}$ < V_S < V_Z	I_S	 2.5	 5	 0.5 6.5	 mA mA
Load on QD with SIPMOS gate; Dynamic Operation 50 kHz V_S = 12V; Load on Q = 10 nF	I_S			 15	 mA
Hysteresis on V_S					
Turn-On Threshold for V_S Rising	$V_{hy\,H}$	9.6	10.4	11.2	V
Switching Hysteresis	$V_{S\,hy}$	1.0		1.7	V
Comparator (COMP)					
Input Offset Voltage	V_{IO}	−10		+10	mV
Input Current	$-I_I$			2	μA
Common-Mode Input Voltage Range	V_{IC}	0		3.5	V
Operational Amplifier (Op Amp)					
Open-Loop Voltage Gain	G_{VO}	60	80		dB
Input Offset Voltage	V_{IO}	−30		−10	mV
Input Current	$-I_I$			2	μA
Common-Mode Input Voltage Range	V_{IC}	0		3.5	V
Output Current	$I_{Q\,Op\,Amp}$	−3		+1.5	mA
Output Voltage	$V_{Q\,Op\,Amp}$	1.2		4	V
Transition Frequency	f_T		2		MHz
Transition Phase	ϕ_T		120		degrees
Output Driver (QD)					
Output Voltage High I_Q = −10 mA	V_{QH}	5			V
Output Voltage Low I_Q = +10 mA	V_{QL}			1	V
Output Current Rising Edge C_L = 10 nF Falling Edge C_L = 10 nF	 $-I_Q$ I_Q	 200 250	 300 350	 400 450	 mA mA

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Characteristics ($V_{S\,ON}$* < V_S < V_Z; −25°C < T_A < +85°C) (Continued)

Parameter	Symbol	Limits			Units
		Min	Typ	Max	
Reference-Voltage Source					
Voltage 0 < I_{REF} < 3 mA	V_{REF}	1.8	2	2.2	V
Load Current	$-I_L$	0		3	mA
Voltage Change 10V < V_S < V_Z 0 mA < I_{REF} < 3 mA	ΔV_{REF}			 5 20	 mV mV
Temperature Response	$\Delta V_{REF}/\Delta T$	−0.5		+0.5	mV/K
Z-Diode (V_S−GND)					
Z Voltage I_Z = 200 mA Observe P_{max}	V_Z	13	15.5	17	V
Multiplier (M1)(1)					
Quadrant for Input Voltages			1		qu.
Input Voltage M1	V_{M1}	0		1	V
Reference Level for M1	$V_{REF\,M1}$		0		V
Input Voltage M2	V_{M2}	V_{REF}		V_{REF}+1	V
Reference Level for M2	$V_{REF\,M2}$		V_{REF}		V
Input Current M1, M2	$-I_I$	0		2	µA
Coefficient for Output-Voltage Source	C_Q	0.4	0.6	0.8	I/V
Temperature Response of Output-Voltage Coefficient	$\Delta TC/C_Q$	−0.3	−0.1	0.1	%/K
Monitoring Circuit					
Input I START Turn-On Voltage Turn-On Current Turn-Off Voltage Turn-Off Current	 $V_{I\,ON\,START}$ $I_{I\,ON\,START}$ $V_{I\,OFF\,START}$ $I_{I\,OFF\,START}$	 17 50 2 70	 22 90 3.5 110	 26 130 5 150	 V µA V µA
Input I STOP** Turn-On Voltage Turn-On Current Turn-Off Voltage Turn-Off Current	 $V_{I\,ON\,STOP}$ $I_{I\,ON\,STOP}$ $V_{I\,OFF\,STOP}$ $I_{I\,OFF\,STOP}$	 27 100 4.5 175	 30 150 6.5 250	 33 200 8.5 320	 V µA V µA
Transfer I START−Q START Output Current on Q START V_{START} = 15V; $V_{Q\,START}$ = 2V	$-I_{Q\,START}$	 400	 600	 800	 mA

**The turn-on voltage of I_{STOP} exceeds the turn-on voltage of I_{START} by at least 3V.

Characteristics ($V_{S\,ON}$* < V_S < V_Z; −25°C < T_A < +85°C) (Continued)

Parameter	Symbol	Limits			Units
		Min	Typ	Max	
Monitoring Circuit (Continued)					
Transfer I STOP – Q STOP Output Current on Q STOP I_{STOP} = 1.5 mA; V_{STOP} = 18V; $V_{Q\,STOP}$ = 1.2V	$-I_{Q\,STOP}$	0.9	1.2		mA
I_{STOP} = 0.4 mA; V_{STOP} ≈ 7V; $V_{Q\,STOP}$ = 1.2V		90	150		μA
Detector (I DET)					
Upper Switching Voltage for Voltage Rising (H)	$V_{DET\,H}$	1	1.3	1.6	V
Lower Switching Voltage for Voltage Falling (L)	$V_{DET\,L}$	0.95			V
Switching Hysteresis	$V_{S\,hy}$	50		300	mV
Input Current 0.9 V < V_{DET} < 6V	$-I_{DET}$		5		μA
Clamping-Diode Current V_{DET} > 6V or V_{DET} < 0.9V	I_{DET}	−3		3	mA
Delay Times					
Input Comparator → Q(2)	t		200	500	ns

Notes:
1. Calculation of the output voltage V_{QM}: V_{QM} = C • V_{M1}* • V_{M2}* in V. The voltages of V_{M1}* and V_{M2}* are referred to the particular reference level.
2. Step functions at comparator input ΔV_{COMP} = −100 mV → ΔV_{COMP} = +100 mV.
*$V_{S\,ON}$ means that V_{SH} has been exceeded but that the voltage is still greater than V_{SL}.

Use and Advantages of IC TDA 4814 in Switched Mode Power Supplies and Electronic Ballasts

1.0 Switched Mode Power Supplies

The "active harmonics filter" consists of a rectifier arrangement in a bridge circuit followed by an up-converter. Through a controller action it is possible to draw a virtually sinusoidal current from the single-phase line and produce a regulated dc voltage at the output.

In the case of an SMPS with conventional line rectification it is possible to achieve a power factor (ratio of active power to apparent power) of 0.5 to 0.7. The active harmonics filter serves for improving the power factor, which reaches a value of almost 1, and for reducing the load on the line produced by harmonics. The losses caused by the active harmonics filter are more than compensated by the fact that a subsequent converter can constantly be operated at an optimal operating point because of the input control of the operating voltage.

The extra effort that is necessary, compared to an SMPS without an active harmonics filter, is made good upwards of about 500W by savings elsewhere (e.g., smaller smoothing capacitance and transistors of a higher resistance in the SMPS). With the wide-ranging power supplies that are in increasing demand, i.e., power supplies that can work on a line of 90 Vac through 240 Vac without any switching changes, the power pay-off limit reduces markedly.

2.0 Electronic Ballasts for Fluorescent Lamps

The VDE and the EVUs require of **industrial** consumers that these take "sinusoidal current" from the

line, i.e., exhibit a purely ohmic response. This is the case with incandescent lamps, cooker rings and heating fixtures.

In all electronic devices with rectification and a CR load the current drain is pulsed, i.e., afflicted by a large harmonic content and impermissible according to VDE. The reflected current ripple can interfere with installations for AF power-line carrier control for instance, i.e., lead to faulty switching. The harmonic content of the current consequently may not exceed certain values.

In the line current for a ballast operating with a stable fluorescent lamp must be such that the share of harmonics in relation to the fundamental does not exceed the values given in Table 1.

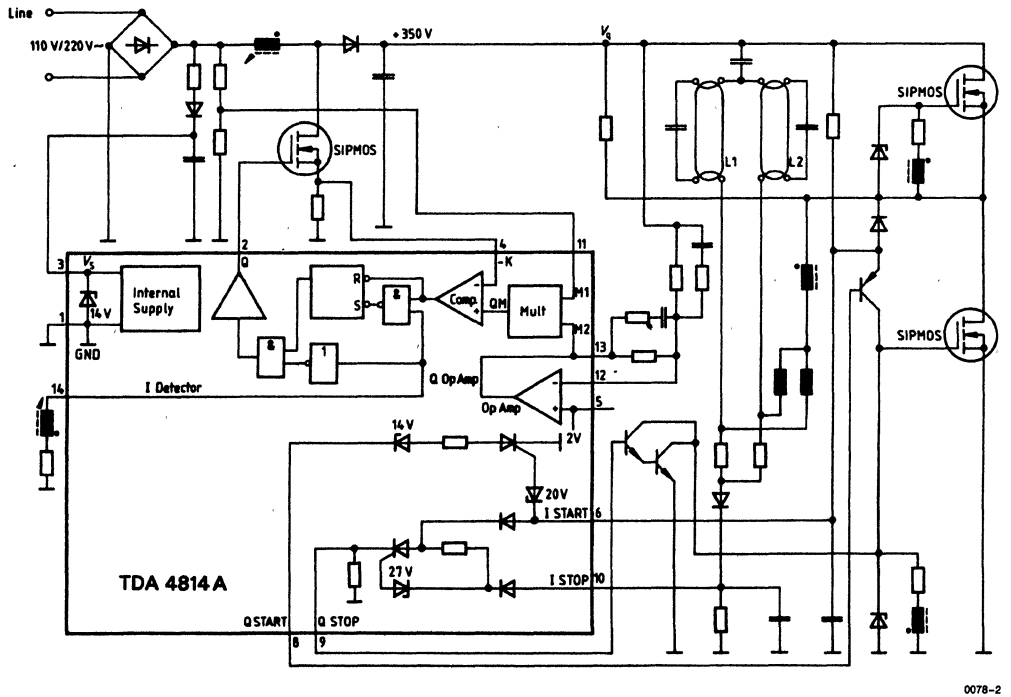
Table 1. Line-Current Harmonic Content According to VDE 0712, Part 2

Harmonics	Admissible Harmonic Content(1) in %
3rd Harmonic	$25 \times \frac{\lambda}{0.9}$
5th Harmonic	7
7th Harmonic	4
9th Harmonic	3
11th Harmonic	2
13th Harmonic and Higher	1

Note:
1. λ is the power factor.
The values given here are achieved using the TDA 4814 A to drive a SIPMOS in an up-converter regulating circuit.

Application Example

Electronic Ballast



Remark:
Kindly note that the SIEMENS AG holds patents on electronic ballasts for fluorescent lamps, published in "Siemens Energy and Automation", Vol. II, No. 2. March/April 1985.

Ordering Information

Type	Ordering Code	Package
TDA 4814 A	Q67000-A8163	P-DIP-14

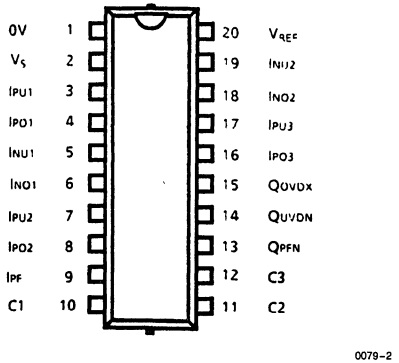
SIEMENS

Preliminary

TDA 4917 A/TDA 4917 G
Monitoring IC for Power Supplies

- Monitors 5 + 2 Independent Voltages
- Freely Selectable Tolerance Width of Five Input
- Overvoltage and Undervoltage Signaling
- Power-Fail Signal
- DIP 20 or SO 20 Package
- Three-Independent, Variable Timing Networks for Three Signaling Outputs
- Supply Undervoltage Monitoring
- AC Monitoring
- Balanced Reference-Voltage Source 2.5V ±1%

Pin Configuration



0079-2

Pin Definitions

Pin	Symbol	Function
P-DIP 20 Package (TDA 4917 A) or SO 20 Package (TDA 4917 G)		
1	0V	Ground
2	V_S	Supply Voltage
3	I_{PU1}	Input Positive Undervoltage 1
4	I_{PO1}	Input Positive Overvoltage 1
5	I_{NU1}	Input Negative Undervoltage 1
6	I_{NO1}	Input Negative Overvoltage 1
7	I_{PU2}	Input Positive Undervoltage 2
8	I_{PO2}	Input Positive Overvoltage 2
9	I_{PF}	Power-Fail
10	C1	Capacitor C1
11	C2	Capacitor C2
12	C3	Capacitor C3
13	Q_{PFN}	Output Power-Fail
14	Q_{UVDN}	Output Undervoltage Shutdown
15	Q_{OVDX}	Output Overvoltage Shutdown
16	I_{PO3}	Input Positive Overvoltage 3
17	I_{PU3}	Input Positive Undervoltage 3
18	I_{NO2}	Input Negative Overvoltage 2
19	I_{NU2}	Input Negative Undervoltage 2
20	V_{REF} 2.5V	Reference Voltage

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With integrated circuit TDA 4917A/G it is possible, depending on the grade of function required, to monitor a maximum of 5 + 2 independent voltages. This monitoring establishes whether preset limit values are exceeded or, at the lower end, not maintained.

Circuit Description

The following circuit description is best understood by reference to the block diagram and timing diagrams.

PNP comparators K1 through K12 are internally connected with one input to V_{REF1} or V_{REF2} or ground. The other input is in each case brought out on a pin. K11 serves for monitoring the supply voltage of the circuit itself.

Overvoltages are to trigger different functions to undervoltages, so the comparators are routed by way of different logic circuits to the three outputs.

Three positive voltage levels, referred to ground, with magnitudes of more than 2.5V can be detected for overvoltage. In the same way two negative voltages, referred to ground, can be monitored for overvoltage.

Of the voltages that are to be monitored for undervoltage, likewise three can be positive (switching threshold > 2.5V) and two can be negative, referred to ground.

Comparators K6 through K12 possess switching hysteresis on their inputs. The values for this hysteresis can be matched by the sum resistance of the external voltage divider to the particular monitoring function.

Three different signal delay times can be freely selected within wide limits by means of three external capacitors. The minimum delays that are possible are obtained if pins C1 through C3 remain unwired. When current sources $I_{SOURCE2}$, $I_{SOURCE4}$ or $I_{SOURCE8}$ are active, the voltage on C1, C2 or C3 drops to approximately 50 mV.

The available outputs are "Overvoltage shutdown" (Q_{OVDX}), "Undervoltage shutdown" (Q_{UVDN}) and "Power-fail" (Q_{PFN}). The "Power-fail" output (Q_{PFN}) is Low for supply undervoltage on the device.

With the command designations in the block diagram the code is as follows:

— X as final letter means effect for High level

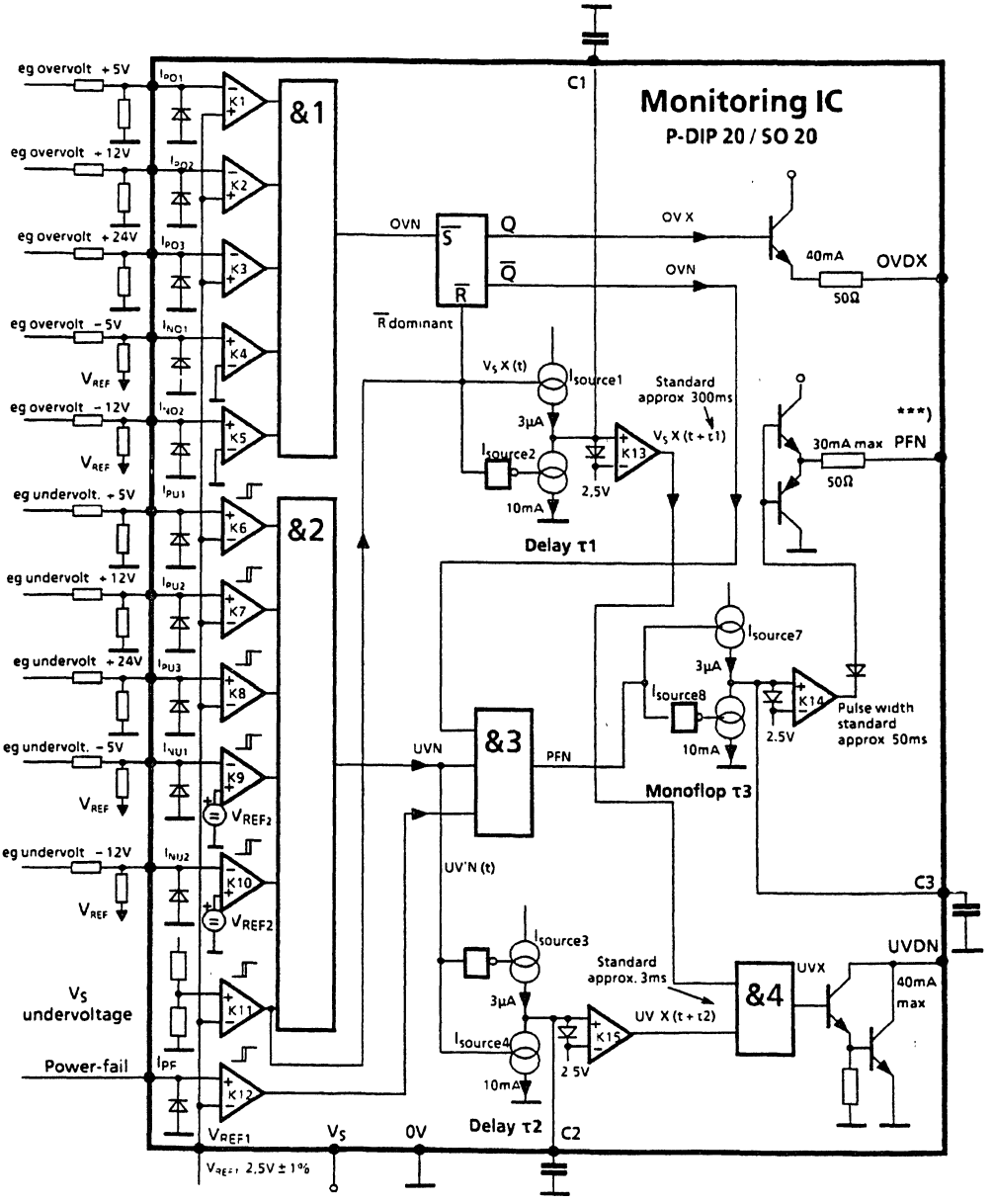
— N as final letter means effect for Low level

— Current sources produce current when driven High

Calculation of $\tau 1$, $\tau 2$, $\tau 3$:

$$\tau_n[ms] = C_n[nF] \times 0.83$$

Block Diagram



0079-1

*** Output Q_{PFN} shown simplified; TTL-compatible

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Absolute Maximum Ratings*

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Pos	Parameter	Symbol	Conditions	Limits		Units
				Min	Max	
Maximum Ratings for Ambient Temperature T_A = −40°C to +85°C						
1	Input Comparator K1 through K12	V_{IKn}		−0.3	30	V
2	Clamping Diodes on Inputs of K1 through K12	I_{Kn}	$-0.3V > V_{Kn}$	−1		mA
3	Supply Voltage	V_S		−0.3	30	V
4	C1, C2, C3	$V_{C1, C2, C3}$		−0.3	2.5	V
5	Output Overvoltage Q_{OVDX}	V_{QOVDX} I_{QOVDX}	$0 > I_{OVDX} > -70$ mA $-0.3V > V_{OVDX} > V_S + 0.3V$	−0.3 −10	V_S + 0.3V +10	V mA
6	Output Undervoltage Q_{UVDN}	V_{QUVDN} I_{QUVDN}	50 mA > I_{UVDN} > 0 $-0.3V > U_{UVDN}$	−0.3 −10	30	V mA
7	Output Power-Fail Q_{PFN}	V_{QPFN} I_{QPFN}	50 mA > I_{PFN} > −50 mA $-0.3V > V_{PFN} > V_S + 0.3V$	−0.3 −10	V_S + 0.3V +10	V mA

Operating Range

Within the operating range the functions stated in the circuit description are fulfilled. Here deviations from the characteristics are possible.

Pos	Parameter	Symbol	Limits		Units	Notes
			Min	Max		
1	Supply Voltage	V_S	4.5	+30	V	
2	Input Voltage K1 through K12	V_{IKn}	−0.3	+30	V	
3	Ambient Temperature	T_A	−40	+85	°C	
4	Junction Temperature	T_j		125 150	°C °C	 *
5	Storage Temperature	T_{stg}	−60	125	°C	
6	Thermal Resistance System-Air	R_{thSA}		60 90	K/W K/W	P-DIP 20 SO 20

*Admissible by limiting useful life to 70,000 h.

Characteristics

The characteristics cover the variance of the values maintained by the integrated circuit at the stated supply voltage and ambient temperature. The typical values are average values that are expected from a manufacturing viewpoint.

Pos	Parameter	Symbol	Conditions	Limits			Units
				Min	Typ	Max	
Supply Voltage $4.5V < V_S < 30V$ **Ambient Temperature** $-40°C < T_A < +85°C$							
1	Current Drain	I_S		3.5		6.5	mA
Inputs I_{PO1}, I_{PO2}, I_{PO3}, I_{NO1}, I_{NO2}, I_{PU1}, I_{PU2}, I_{PU3}, I_{NU1}, I_{NU2}, I_{PF}							
2	Input Current	I_I		-0.5		0.5	µA
3	Switching Voltage of I_{PO1}, I_{PO2}, I_{PO3}, I_{PU1}, I_{PU2}, I_{PU3}, I_{PF}	V_{swp}		V_{REF1} − 10 mV		V_{REF1} + 10 mV	V
4	Switching Voltage of I_{NO1}, I_{NO2}	U_{swno}		-10	0	$+10$	mV
5	Switching Voltage of I_{NU1}, I_{NU2}	V_{swnu}		V_{REF2} − 10 mV		V_{REF2} + 10 mV	V
Voltage Supply on V_S							
6	Level on V_S for Supply Undervoltage (Voltage Dropping)			4.5	4.6	4.7	V
	Switching Hysteresis of Supply Undervoltage (on V_S)*			90	100	110	mV
Switching Hysteresis							
7	Comparators K6, K7, K8, K12 Hysteresis Current	I_{hyh} I_{hyl}	$V(+K) < V_{swp}$ $V(+K) > V_{swp}$	7	10	13 0.1	µA µA
8	Comparators K9, K10 Hysteresis Current	$-I_{hyh}$ $-I_{hyl}$	$V(-K) > V_{swn}$ $V(-K) < V_{swp}$	7	10	13 0.1	µA µA
Delay $\tau 1$							
9	Charge Current on C1 (V_{C1} rising)	$-I_{C1ch}$		2.1	3	3.9	µA
10	Discharge Current on C1 (V_{C1} Dropping)	I_{C1dis}		7	10	13	mA
Delay $\tau 2$							
11	Charge Current on C2 (V_{C2} Rising)	$-I_{C2ch}$		2.1	3	3.9	µA
12	Discharge Current on C2 (V_{C2} Dropping)	I_{C2dis}		7	10	13	mA

*Set with K11

Characteristics (Continued)

The characteristics cover the variance of the values maintained by the integrated circuit at the stated supply voltage and ambient temperature. The typical values are average values that are expected from a manufacturing viewpoint.

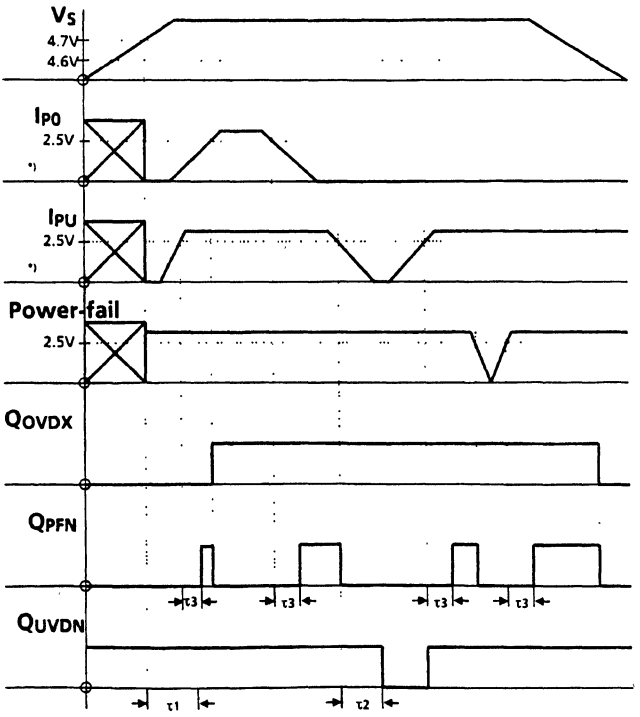
Pos	Parameter	Symbol	Conditions	Limits			Units
				Min	Typ	Max	
MONOFLOP $\tau 3$							
13	Charge Current on C3 (V_{C3} Rising)	$-I_{C3ch}$		2.1	3	3.9	µA
14	Discharge Current on C3 (V_{C3} Dropping)	I_{C3dis}		7	10	13	mA
OUTPUT OVERVOLTAGE (Q_{OVDX})							
15	Output High	$-I_{OVDX}$	V_S = 5V V_{OVDX} = 1V		40		mA
16	Output High	$V_{H\,OVDX}$	$-I_{OVDX}$ = 10 mA		$V_S - 1$		V
OUTPUT UNDERVOLTAGE (Q_{UVDN})							
17	Output Low	$V_{L\,UVDN}$	I_{UVDN} = 40 mA		1.5		V
OUTPUT POWER-FAIL (Q_{PFN})							
18	Output High	$-I_{PFN}$	V_S = 5V V_{PFN} = 1V	20	30	40	mA
19	Output High*	$V_{H\,PFN}$	$-I_{PFN}$ = 10 mA $-I_{PFN}$ = 40 µA		$U_S - 2.5$ $U_S - 1.5$		V V
20	Output Low	I_{PFN}	V_{PFN} = 3V	20	30	40	mA
21	Output Low	$V_{L\,PFN}$	I_{PFN} = 10 mA I_{PFN} = 1.6 mA		1.5	 0.4	V V
REFERENCE VOLTAGE 1 (V_{REF1})							
22	Voltage**	V_{REF1}	I_{REF1} = 1 mA; T_{amb} = 25°C; V_S = 12V	2.475	2.5	2.525	V
23	Load Current	$-I_{REF1}$		0		3	mA
24	Voltage Alteration	ΔV_{REF1}	V_S ±20% I_{REF1} ±20%			10 5	mV mV
25	Temperature Response	$\Delta V_{REF1}/\Delta T$		−0.3		+0.3	mV/k
26	Shortcircuit Current (Admissable Sustained)	I_{SC}	V_{REF1} = 0V		10		mA
REFERENCE VOLTAGE 2 (V_{REF2})							
27	Voltage***	V_{REF2}	T_{amb} = 25°C; V_S = 12V; V_{REF1} = 2.5V	97	100	103	mV

*Max. 6.5V however

**When adjusted (±1%); without adjustment ±6%

***V_{REF2} is derived by voltage divider (R1 + R2)/R2 = 25 from V_{REF1}.

Diagram



*I_{NO} and I_{NU} are logically identical like I_{PO} and I_{PU}, but have switching levels 0V.
During $\tau 1$ Q_{UVDN} cannot go low (turn-on procedure).
$\tau 2$ suppresses undervoltage spikes.
$\tau 3$ ensures minimum duration of power-fail signal (Q_{PFN}).

Ordering Information

Type	Ordering Code	Package
TDA 4917 A	Q67000-A8131	P-DIP 20
TDA 4917 G	Q67000-A8132	SO 20

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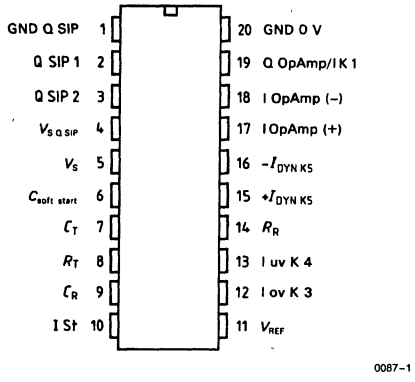
SIEMENS

Preliminary

TDA 4918 A; G
IC for Push-Pull Switched-Mode Power Supplies with SIPMOS Driver Output

Pin Configuration

Top View

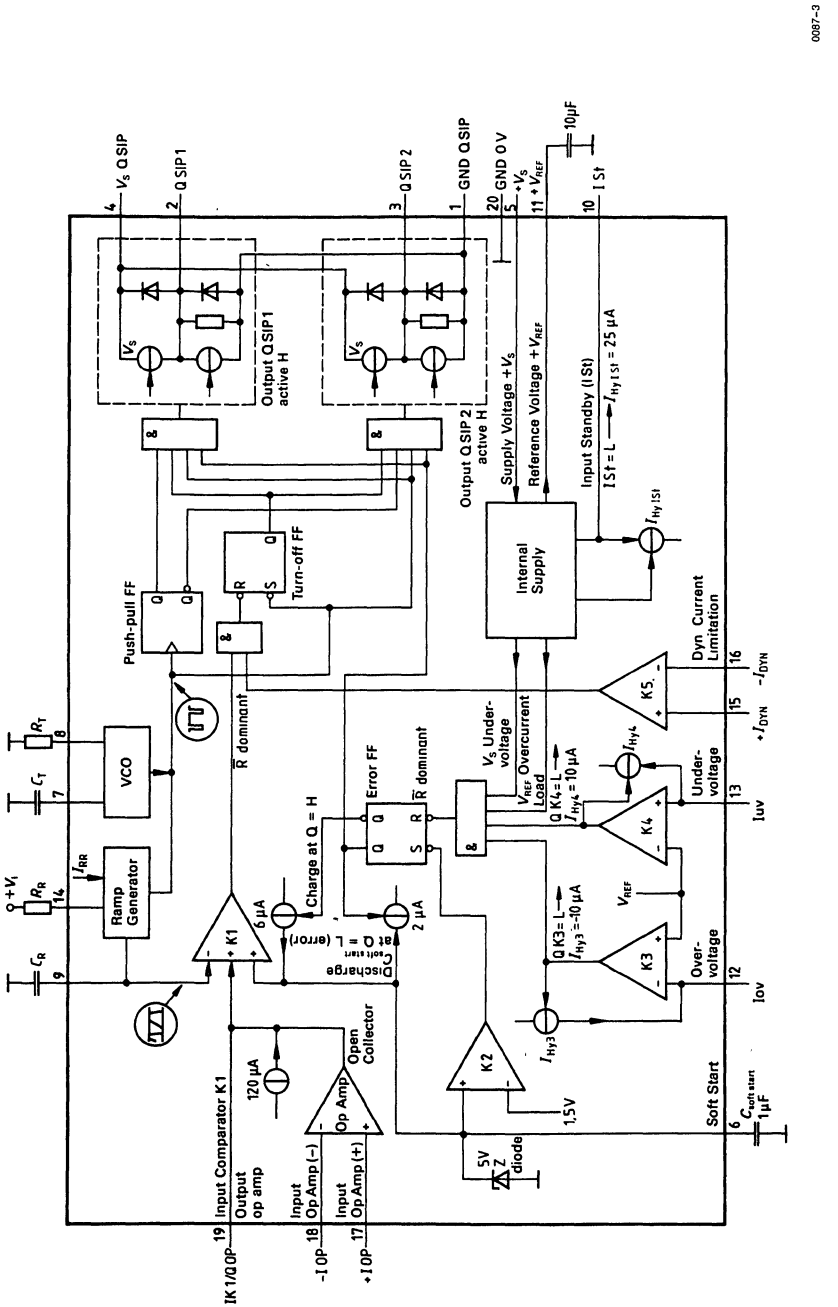


Pin Definitions

Pin	Function
1	GND Q SIP
2	Output SIPMOS driver Q SIP 1
3	Output SIPMOS driver Q SIP 2
4	Supply Voltage $V_{S\,Q\,SIP}$
5	Supply Voltage V_S
6	Soft Start $C_{soft\ start}$
7	VCO C_T
8	VCO R_T
9	Ramp Generator C_R
10	Input Standby I St
11	Reference Voltage V_{REF}
12	Input Overvoltage K 3
13	Input Overvoltage K 4
14	Ramp Generator R_R
15	Input Dynamic Current Limitation K 5 (+)
16	Input Dynamic Current Limitation K 5 (–)
17	Input Operational Amplifier (+)
18	Input Operational Amplifier (–)
19	Output Operational Amplifier Q OpAmp/I COMP K 1
20	GND 0V

This versatile switched-mode power supply control IC for the control of SIPMOS power transistors comprises digital and analog functions. These functions are required in the design of high quality flyback and forward converters in single-phase and push-pull operation in normal, half-bridge and full bridge circuits. The component can also be used for single-ended voltage multipliers and speed-controlled motors. Malfunctions in the electrical operation of the switched-mode power supply are recognized by the comparators in the SMPS IC and activate protective functions.

Block Diagram



Circuit Description

The various functional units of the component and their interaction are described in the following.

Supply Voltage V_S

The IC enables the two outputs not before the turn-on threshold ($V_{S\ ON}$) at V_S is exceeded. The duty cycle (active time/disable time) at the enabled outputs can then rise from zero to the value set with K 1 in the time specified by the soft start.

An undervoltage at the standby input causes the current consumption I_S to remain at the very low standby current level independent of the voltage V_S.

Voltage Controlled Oscillator (VCO)

The VCO is connected with the capacitor C_T and the resistor R_T. The charge current at C_T flows continuously and is set with resistor R_T. The discharge current is active during the discharge of C_T and is set internally.

In the typical mode of operation the duration of the rising edge is considerably greater than that of the falling edge. During the falling edge the VCO passes a trigger signal to the ramp generator thus discharging the ramp generator capacitance. Additionally, the trigger signal is routed to other parts of the IC.

Ramp Generator

The ramp generator is controlled by the VCO and operates at the same frequency as the VCO. The duration of the ramp generator falling edge must be shorter than the VCO fall time. Only then do the ramp generator upper and lower switching levels reach their rated values.

To control the pulse width at the output, the voltage of the ramp generator rising edge is compared with an externally adjustable dc voltage at comparator K 1. The slope of the rising edge is adjusted via the current by means of R_R. This provides the possibility of an additional superimposed control of the output duty cycle. This control capability (feed-forward control) permits the compensation of known interference (e.g., input voltage ripple). A superimposed load current control **(current mode control)** however, can also be implemented.

Push-Pull FlipFlop

The push-pull flipflop is switched by the falling edge of the VCO. This ensures that only one output of the two push-pull outputs is enabled at a time.

Comparator K 1 (Duty Cycle Control)

The two plus inputs of the comparator are switched such that the lower plus level is always compared with the level of the minus input. As soon as the voltage of the rising sawtooth edge (minus input) exceeds the lower level of the two plus inputs, the currently active output is disabled via the turn-off flipflop. The "high"-duration of the respectively active output can thus be infinitely varied. As the frequency remains constant, this process corresponds to a change in duty cycle.

Operational Amplifier (Op Amp)

The op amp is a high quality operational amplifier. It can be used in the control circuit to transmit the amplified variations of the voltage to be regulated to the free plus input of comparator K 1. A voltage change is thus converted to a duty cycle change.

Turn-Off FlipFlop

The falling edge of the VCO causes a pulse at the turn-off flipflop set input. It can, however, only be actually set if no reset signal is pending. With the turn-off flipflop set, the two outputs are enabled and one of them can be active. Upon an error signal from K 5 or upon a turn-off signal from K 1 the flipflop disables the outputs.

Z Diode

The Z diode limits the voltage at capacitor $C_{soft\ start}$ to a maximum of 5V. The ramp generator voltage can reach 5.5V. For an appropriate slope of the rising ramp generator edge, the duty cycle can be limited to a desired maximum value. This can be a possible advantage in flyback converter operation.

Comparator K 2

The comparator has its switching threshold at 1.5V at the plus input, and with its output sets the error flipflop if the voltage at capacitor $C_{soft\ start}$ is below 1.5V. The error flipflop, however, will only accept the set pulse if no reset pulse (error) is pending. This prevents a restart of the outputs as long as an error signal is pending.

Soft Start

The lower of the two voltages at the K 1 plus inputs—compared with the ramp generator voltage—is a measure for the duty cycle at the output. At component turn-on, the voltage at capacitor $C_{soft\ start}$ is equal to 0V. As long as no error exists,

the capacitor will be charged to the maximum value of 5V with a current of 6 μA.

In the case of an error, $C_{soft\ start}$ is discharged with a current of 2 μA. The currently active output, however, is immediately disabled by the error flipflop. Below a charge voltage of 1.5V, a set signal is pending at the error flipflop and the outputs are enabled if no reset signal is pending at the same time. As the minimum ramp generator voltage, however, is 1.8V, the duty cycle at the outputs is actually only increased slowly and continuously after the voltage at $C_{soft\ start}$ exceeds 1.8V.

Error FlipFlop

Error signals, routed to the error flipflop reset input, cause an immediate disabling of the output (low), and after elimination of the error, a restart of the component by soft start.

Comparators K 3 (Overvoltage), V_{REF} Overcurrent, V_S Undervoltage

These are error detectors that on error, cause the error flipflop to immediately disable the outputs. After elimination of the error, the duty cycle is raised again using the soft start. Upon overvoltage, a current is impressed at the input of K 3, that can be used to enable an adjustable hysteresis or a holding function.

Comparator K 4 (Undervoltage)

Comparator K 4 switches with an adjustable hysteresis. The value of the hysteresis is derived from the internal resistance of the external control source and the current impressed internally at the input of K 4. In the undervoltage case, the set current flows into the component in the technical direction of current flow. In the error case (undervoltage), both outputs are disabled. The component restarts by soft start.

Comparator K 5 (Dynamic Current Limiter)

K 5 serves to recognize overcurrents at the switching transistors. Both inputs of the comparator are externally accessible. After elimination of the error, the outputs are enabled with the VCO trigger pulse at the turn-off flipflop. The delay time between occurrence of an error and disabling of the outputs is only approximately 250 ns.

Standby Input (I St)

This input switches with voltage and current hysteresis. The voltage levels for switching from standby to active operation can be set with an external voltage divider between V_S–standby input–ground.

Reference Voltage (V_{REF})

The reference voltage source is a highly constant source with regard to its temperature behavior. It can be used for the external wiring of the op amp; the error comparators, the ramp generator, or other external components.

SIPMOS Driver Output (QSIP)

The two outputs operate in the push-pull mode. They are active high. The duration during which one of the outputs is active, can be varied infinitely. The duration of the falling edge at the frequency generator is equal to the minimum duration during which both outputs are simultaneously low.

The output driver is designed as a push-pull stage. The output current is internally limited to the specified values.

A 10 kΩ resistor is connected between the output and ground. This resistor holds the SIPMOS transistor reliably disabled during standby operation (undervoltage at I St). Output Q SIP is connected with the supply voltage $V_{S\ Q\ SIP}$ and with ground via diodes. The diode connected to $V_{S\ Q\ SIP}$ routes the capacitive shift currents from the SIPMOS transistor gate to the filter capacitor at $V_{S\ Q\ SIP}$ during turning on the SMPS supply voltage. The voltage at $V_{S\ Q\ SIP}$ can reach approximately 2.3V without the SIPMOS transistor being turned on.

The diode connected to ground connects negative voltages at Q SIP to -0.7V. This provides an unimpeded flow off of capacitive currents occuring during voltage breakdown at the SIPMOS transistor drain connection.

For supply voltages starting at approximately 2V, both outputs are active low in the disabled state. The function of the diode connected to $V_{S\ Q\ SIP}$ is then taken over by the pull-down source.

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Absolute Maximum Ratings*

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter	Symbol	Limits		Units
		Min	Max	
Supply Voltage				
Inputs K 1, Op Amp, K 3, K 4, K 5, I St	V_S	−0.3	33	V
Frequency Generator (VCO)				
Voltage at R_T/C_T	V_{CT}, V_{RT}	−0.3	6	V
$V_{CT} > 6V$	I_{CT}		3	mA
Ramp Generator				
Voltage at C_R/R_R	V_{CR}, V_{RR}	−0.3	6	V
Reference Voltage	V_{REF}	−0.3	6	V
Output Op Amp	$V_{Q\ op\ amp}$	−0.3	6	V
Driver Output Q SIP	$V_{Q\ SIP}$(1)	−0.3	6	V
Q SIP Clamp Diodes at Q SIP $V_{Q\ SIP} > V_S$ or $V_{Q\ SIP} < -0.3V$	$I_{Q\ SIP}$	−10	10	mA
Soft Start	$V_{C\ soft\ start}$	−0.3	6	V
Junction Temperature	T_j(2)		125	°C
Storage Temperature	T_{stg}	−65	125	°C
Thermal Resistance TDA 4918 A (System-Air) TDA 4918 G	$R_{th\ SA}$ $R_{th\ SA}$		63 90	K/W K/W
Operating Range				
Supply Voltage	V_S(3)	$V_{S\ ON}$	30	V
Frequency Generator (VCO)	f_{VCO}		300	KHz
Ramp Generator	f_R		300	KHz
Ambient Temperature	T_A	−40	85	°C

Notes:
1. With this, the maximum power dissipation or junction temperature must be taken into account!
2. At a planned maximum operating time of 70,000 hours a continuous maximum junction temperature of 150°C is permitted.
3. For $V_{S\ ON}$ values refer to characteristic data.

Characteristics $V_{S\ ON}$(1) < V_S < 30V; T_A = −40°C to +85°C

Parameter	Symbol	Conditions	Limits			Units
			Min	Typ	Max	
Current Consumption						
Without Load at V_{REF} Q OP, Q SIP 1, 2	I_S	C_T = 1 nF Frequency Generator with 100 kHz			20	mA
Standby Operation	I_{St}				3.5	mA
Hysteresis at V_S						
Turn-On Threshold for V_S Rising	$V_{S\ H}$	$V_{on\text{-}THR} \geq V_{on\text{-}THR\ H}$		8.3	9.6	V
Turn-Off Threshold for V_S Falling	$V_{S\ L}$			7.6		V
Reference Voltage						
Voltage	V_{REF}	I_{REF} = 1 mA T_A = 25°C V_S = 15V	2.475	2.5	2.525	V
Load Current	$-I_{REF}$		0		3	mA
Voltage Change	ΔV_{REF}	V_S ±20%			10	mV
Voltage Change	ΔV_{REF}	I_{REF} ±20%			3	mV
Temperature Response	$\Delta V_{REF}/\Delta T$		−0.3		+0.3	mV/K

Characteristics $V_{S\,ON}$[1] < V_S < 30V; T_A = −40°C to +85°C (Continued)

Parameter	Symbol	Conditions	Limits			Units
			Min	Typ	Max	
Reference Voltage (Continued)						
Response Threshold for I_{REF} Overcurrent	I_{OV}			7		mA
Short-Circuit Current	I_{SC}	V_{REF} = 0V		10		mA
Frequency Generator (VCO)						
Frequency Range	f_{VCO}				300	KHz
Frequency Change	Δf/fo	V_S ±20%			1	%
Tolerance	Δf/fo	C_T = 0.2 nF R_T = 50 kΩ T_A = 25°C	−7		+7	%
Charging Current for C_T (perm) = Current at Pin R_T	I_{RT}	$I_{RT} = V_{REF/RT}$	0		1	mA
Discharging Current for C_T	I_{dch}	Internally Fixed		2		mA
C_T Range[2]					1000	nF
Upper Switching Threshold	V_u			5		V
Lower Switching Threshold	V_l			2		V
Ramp Generator						
Frequency Range	f_R				300	KHz
Maximum Voltage at C_R	$V_{CR\,H}$			5.5		V
Minimum Voltage at C_R	$V_{CR\,L}$		1.65	1.8	1.95	V
Charging Current for C_R (perm) = Current at Pin R_R	I_{ch}	V_{RR} Approx. 0.7V	0		1	mA
Discharging Current for C_R	I_{dch}	Internally Fixed		3		mA
Ratio $I_{RR}/I_{CR\,charge}$		I_{RR} = 0.5 mA	0.95		1.1	
Comparator K1						
Input Current	$I_{I\,K\,1}$				2	μA
Turn-Off Delay Time[3] (Signal Transit Time Input K 1 to Q SIP)					500	ns
Common-Mode Input Voltage Range	V_{IC}		0		V_{CRH}	V
Operational Amplifier						
Open-Loop Voltage Gain	G_{VO}		60	80		dB
Input Offset Voltage	V_{IO}	Pin 10 n.c.	−10		+10	mV
Input Current	$-I_{I\,op\,amp}$				2	μA
Common-Mode Input Voltage Range	V_{IC}		0		4	V
Output Current	$I_{Q\,op\,amp}$		0		2	mA
Output Voltage Range	$V_{Q\,op\,amp}$	0 mA < I_Q < 2 mA	0.5		V_{CRH}	V
Transition Frequency	f_T			3		MHz
Transition Phase	ϕ_T			120		degrees

Notes:
1. $V_{S\,ON}$ means that $V_{S\,HIGH}$ has been exceeded, while $V_{S\,LOW}$ has not yet been exceeded.
2. C_T = 0.2 nF corresponds to a fall time of 0.2 μs (±30%) if the discharge current largely exceeds the charge current. The fall time equals the minimum dead time at the output.
3. Step function ΔV = −100 mV ⌐ ΔV = +100 mV, for transit time from input comparator to Q SIP.

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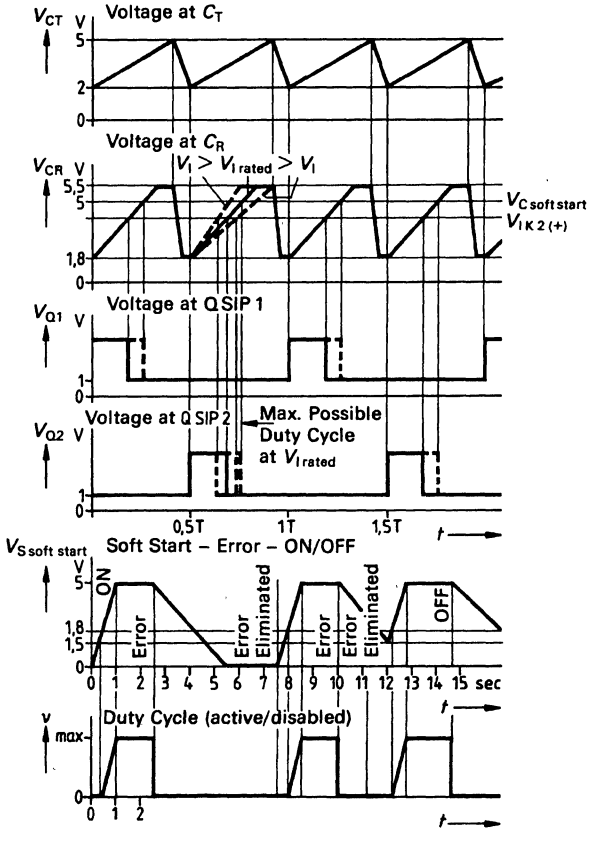
Characteristics $V_{S\,ON}$[1] < V_S < 30V; T_A = −40°C to +85°C (Continued)

Parameter	Symbol	Conditions	Limits			Units
			Min	Typ	Max	
Operational Amplifier (Continued)						
Temperature Coefficient of V_{IO}	TC		−30		+30	μV/K
Source Current at Q Op Amp	$I_{op\ amp}$	0.5V < V_Q < 5.5V		120		μA
Soft Start						
Charging Current for $C_{soft\ start}$	$-I_{ch}$			6		μA
Discharging Current for $C_{soft\ start}$	I_{dch}			2		μA
Upper Limiting Voltage	V_{lim}			5		V
Switching Voltage of K 2	$V_{K\,2}$			1.5		V
Dynamic Current Limitation K 5						
Input Current	$-I_{I\,DYN}$				2	μA
Input Offset Voltage	V_{IO}		−10		+10	mV
Common-Mode Input Voltage Range	V_{IC}		0		V_S − 3	V
Turn-Off Delay Time[6]	t	Rated Load 3 nF at Q SIP		250	400	ns
Undervoltage K 4						
Input Current at K 4	$-I_{I\,K\,4}$				0.2	μA
Switching Voltage at K 4	V_{SW}		V_{REF} − 10 mV		V_{REF} + 10 mV	V
Hysteresis Current	$I_{Hy\,4\,H}$ $I_{Hy\,4\,L}$	$V_{(+K\,4)}$ V_{SW} $V_{(+K\,4)}$ V_{SW}	12	18	25 0.1	μA μA
Turn-Off Delay Time[5]	t				3	μs
Overvoltage K 3						
Input Current	$-I_{I\,K\,3}$				0.2	μA
Switching Voltage	V_{Sw}		V_{REF} − 10 mV		V_{REF} + 10 mV	V
Turn-Off Delay Time[5]	t				3	μs
Hysteresis Current	$-I_{Hy\,3\,H}$ $-I_{Hy\,3\,L}$	$V_{(-K\,3)} > V_{SW}$ $V_{(-K\,3)} < V_{SW}$	7	10	13 0.1	μA μA
Output Driver Q SIP 1, 2						
Output Voltage High	V_{QH}	$I_{Q\,SIP}$ = −300 mA	V_S − 3			V
Output Voltage Low	V_{QL} V_{QL}	$I_{Q\,SIP}$ = +300 mA $I_{Q\,SIP}$ = +10 mA			2.1 1.4	V V
Output Current[4]	$I_{Q\,SIP}$ $-I_{Q\,SIP}$			500 300	700 500	mA mA
Input Standby I St						
Turn-On Threshold for $V_{I\,St}$ Rising	$V_{I\,St\,H}$	$V_S > V_{S\,ON}$	6.2	6.8	7.4	V
Turn-Off Threshold for $V_{I\,St}$ Falling	$V_{I\,St\,L}$		5.6	6.2	6.8	V
Hysteresis Current	$-I_{Hy\,St\,H}$ $I_{Hy\,St\,L}$	$V_{I\,St} > V_{I\,St\,H}$ $V_{I\,St} < V_{I\,St\,L}$	35	50	2 65	μA μA

Notes:
4. Dynamic maximum current during rising of falling edge.
5. Step function V_{REF} = −100 mV ↙ V_{REF} = +100 mV } for transit time from
6. Step function ΔV = −100 mV ↙ ΔV = +100 mV } input comparator to Q SIP.

Pulse Diagram



Ordering Information

Type	Ordering Code	Package
TDA 4918 A	Q67000-A8021	DIP 20
TDA 4918 G	Q67000-A8142	SO-20

10

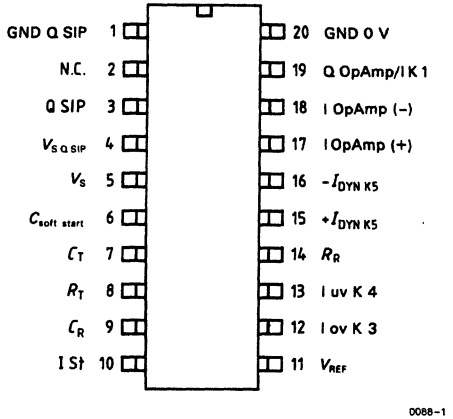
SIEMENS

Preliminary

TDA 4919 A; G
Bipolar IC for Single-Phase Switched-Mode Power Supplies with SIPMOS Driver Output

Pin Configuration

(Top View)



Pin Definitions

Pin	Function
1	GND Q SIP
2	N.C.
3	SIPMOS driver Q SIP
4	Supply Voltage $V_{S\,Q\,SIP}$
5	Supply Voltage V_S
6	Soft Start $C_{soft\ start}$
7	VCO C_T
8	VCO R_T
9	Ramp Generator C_R
10	Input Standby I St
11	Reference Voltage V_{REF}
12	Input Overvoltage K 3
13	Input Overvoltage K 4
14	Ramp Generator R_R
15	Input Dynamic Current Limitation K 5 (+)
16	Input Dynamic Current Limitation K 5 (−)
17	Input Operational Amplifier (+)
18	Input Operational Amplifier (−)
19	Output Operational Amplifier/Input Comparator
20	GND 0V

This versatile single-phase switched-mode power supply control IC for the direct control of SIPMOS power transistors comprises digital and analog functions. These functions are required in the design of high quality flyback, forward, and choke converters with switching frequencies up to 300 kHz. The IC can also be used for single-ended voltage multipliers and speed-controlled motors. Malfunctions in the electrical operation of the switched-mode power supply are recognized by the comparators in the SMPS IC and activate protective functions.

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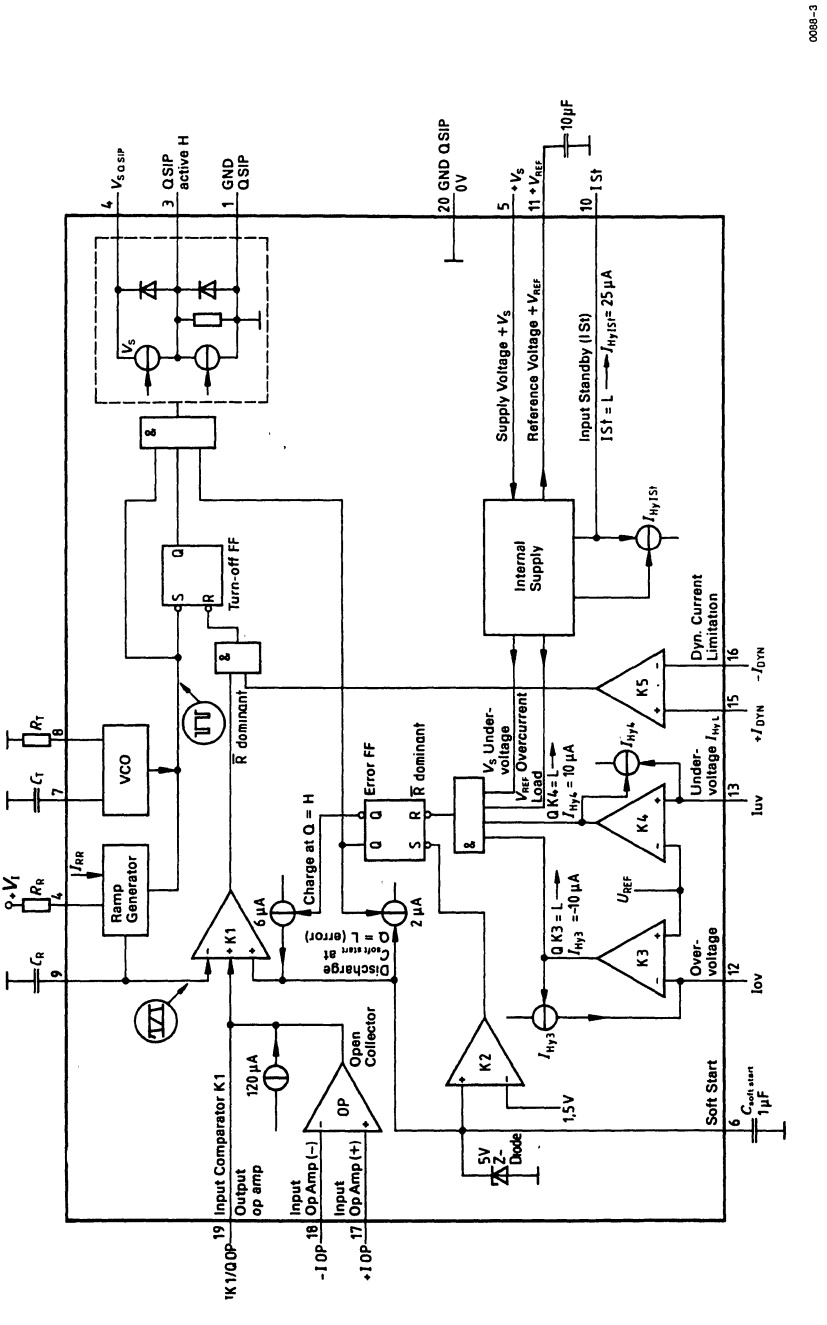

Circuit Description

The various functional units of the component and their interaction are described in the following.

Supply Voltage V_S

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Voltage Controlled Oscillator (VCO)

The VCO is connected with the capacitor C_T and the resistor R_T. The charge current at C_T flows continuously and is set with resistor R_T. The discharge current is active during the discharge of C_T and is set internally.

In the typical mode of operation the duration of the rising edge is considerably greater than that of the falling edge. During the falling edge the VCO passes a trigger signal to the ramp generator thus discharging the ramp generator capacitance. Additionally, the trigger signal is routed to other parts of the IC.

Ramp Generator

The ramp generator is controlled by the VCO and operates at the same frequency as the VCO. The duration of the ramp generator falling edge must be shorter than the VCO fall time. Only then do the ramp generator upper and lower switching levels reach their rated values.

To control the pulse width at the output, the voltage of the ramp generator rising edge is compared with an externally adjustable dc voltage at comparator K 1. The slope of the rising edge is adjusted via the current by means of R_R. This provides the possibility of an additional superimposed control of the output duty cycle. This control capability (feed-forward control) permits the compensation of known interference (e.g., input voltage ripple). A superimposed load current control **(current mode control)** however, can also be implemented.

Comparator K 1 (Duty Cycle Control)

The two plus inputs of the comparator are switched such that the lower plus level is always compared with the level of the minus input. As soon as the voltage of the rising sawtooth edge (minus input) exceeds the lower level of the two plus inputs, the output is disabled via the turn-off flipflop. The "high"-duration of the output can thus be infinitely varied. As the frequency remains constant, this process corresponds to a change in duty cycle.

Operational Amplifier (Op Amp)

The op amp is a high quality operational amplifier. It can be used in the control circuit to transmit the amplified variations of the voltage to be regulated to the free plus input of comparator K 1. A voltage change is thus converted to a duty cycle change.

Turn-Off FlipFlop

The falling edge of the VCO causes a pulse at the turn-off flipflop set input. It can, however, only be actually set if no reset signal is pending. With the turn-off flipflop set, the output is enabled and can be active. Upon an error signal from K 5 or upon a turn-off signal from K 1 the flipflop disables the output.

Z Diode

The Z diode limits the voltage at capacitor $C_{soft\ start}$ to a maximum of 5V. The ramp generator voltage can reach 5.5V. For an appropriate slope of the rising ramp generator edge, the duty cycle can be limited to a desired maximum value. This can be a possible advantage in flyback converter operation.

Comparator K2

The comparator has its switching threshold at 1.5V at the plus input, and with its output sets the error flipflop if the voltage at capacitor $C_{soft\ start}$ is below 1.5V. The error flipflop, however, will only accept the set pulse if no reset pulse (error) is pending. This prevents a restart of the outputs as long as an error signal is pending.

Soft Start

The lower of the two voltages at the K 1 plus inputs—compared with the ramp generator voltage—is a measure for the duty cycle at the output. At

component turn-on, the voltage at capacitor $C_{soft\ start}$ is equal to 0V. As long as no error exists, the capacitor will be charged to the maximum value of 5V with a current of 6 μA.

In the case of an error, $C_{soft\ start}$ is discharged with a current of 2 μA. The output, however, is immediately disabled by the error flipflop. Below a charge voltage of 1.5V, a set signal is pending at the error flipflop and the output is enabled if no reset signal is pending at the same time. As the minimum ramp generator voltage, however, is 1.8V, the duty cycle at the outputs is actually only increased slowly and continuously after the voltage at $C_{soft\ start}$ exceeds 1.8V.

Error FlipFlop

Error signals, routed to the error flipflop reset input, cause an immediate disabling of the output (low), and after elimination of the error, a restart of the component by soft start.

Comparators K 3 (Overvoltage), V_{REF} Overcurrent, V_S Undervoltage

These are error detectors that on error, cause the error flipflop to immediately disable the outputs. After elimination of the error, the duty cycle is raised again using the soft start. Upon overvoltage, a current is impressed at the inputs of K 3 and K 4, that can be used to enable an adjustable hysteresis or a holding function.

Comparator K 4 (Undervoltage)

Comparator K 4 switches with an adjustable hysteresis. The value of the hysteresis is derived from the internal resistance of the external control source and the current impressed internally at the input of K 4. In the undervoltage case, the set current flows into the component in the technical direction of current flow. In the error case (undervoltage), both outputs are disabled. The component restarts by soft start.

Comparator K 5 (Dynamic Current Limiter)

K 5 serves to recognize overcurrents at the switching transistor. Both inputs of the comparator are externally accessible. After elimination of the error, the output is enabled with the VCO trigger pulse at the turn-off flipflop. The delay time between occurrence of an error and disabling of the output is only approximately 250 ns.

Standby Input (I St)

This input switches with voltage and current hysteresis. The voltage levels for switching from standby to active operation can be set with an external voltage divider between V_S–standby input–ground.

Reference Voltage (V_{REF})

The reference voltage source is a highly constant source with regard to its temperature behavior. It can be used for the external wiring of the op amp; the error comparators, the ramp generator, or other external components.

SIPMOS Driver Output (QSIP)

The output is active high. The duration during which the output is active, can be varied infinitely. The duration of the falling edge at the frequency generator is equal to the minimum duration during which output is low (dead time).

The output driver is designed as a push-pull stage. The output current is internally limited to the specified values.

A 10 kΩ resistor is connected between the output and ground. This resistor holds the SIPMOS transistor reliably disabled during standby operation (undervoltage at I St). Output Q SIP is connected with the supply voltage $V_{S\ Q\ SIP}$ and with ground via diodes. The diode connected to $V_{S\ Q\ SIP}$ routes the capacitive shift currents from the SIPMOS transistor gate to the filter capacitor at $V_{S\ Q\ SIP}$ during turning on the SmPS supply voltage. The voltage at $V_{S\ Q\ SIP}$ can reach approximately 2.3V without the SIPMOS transistor being turned on.

The diode connected to ground connects negative voltages at Q SIP to −0.7V. This provides an unimpeded flow off of capacitive currents occuring during voltage breakdown at the SIPMOS transistor drain connection.

For supply voltages starting at approximately 2V, the output is active low in the disabled state. The function of the diode connected to $V_{S\ Q\ SIP}$ is then taken over by the pull-down source.

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Absolute Maximum Ratings*

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter	Symbol	Limits		Units
		Min	Max	
Supply Voltage				
Inputs K 1, Op Amp, K 3, K 4, K 5, I St	V_S	−0.3	33	V
Frequency Generator (VCO)				
Voltage at R_T/C_T	V_{CT}, V_{RT}	−0.3	6	V
$V_{CT} > 6V$	I_{CT}		3	mA
Ramp Generator				
Voltage at C_R/R_R	V_{CR}, V_{RR}	−0.3	6	V
Reference Voltage	V_{REF}	−0.3	6	V
Output Op Amp	$V_{Q\ op\ amp}$	−0.3	6	V
$V_{Q\ op\ amp} > 6V$	$I_{Q\ op\ amp}$		2	mA
Driver Output Q SIP(1)	$V_{Q\ SIP}$	−0.3	V_S	V
Q SIP Clamp Diodes at Q SIP	$I_{Q\ SIP}$	−10	10	mA
$V_{Q\ SIP} > V_S$ or $V_{Q\ SIP} < -0.3V$				
Soft Start	$V_{C\ soft\ start}$	−0.3	6	V
$V_{C\ soft\ start} > 6V$	$I_{C\ soft\ start}$		100	µA
Junction Temperature	T_j		125	°C
Storage Temperature	T_{stg}	−65	125	°C
Thermal Resistance (System-Air) TDA 4919 A TDA 4919 G	 $R_{th\ SA}$ $R_{th\ SA}$		 63 90	 K/W K/W
Operating Range				
Supply Voltage(2)	V_S	$V_{S\ ON}$	30	V
Frequency Generator (VCO)	f_{VCO}		300	KHz
Ramp Generator	f_R		300	KHz
Ambient Temperature	T_A	−40	85	°C

Notes:
1. With this, the maximum power dissipation or junction temperature must be taken into account!
2. For $V_{S\ ON}$ values refer to characteristic data.

Characteristics $V_{S\ ON}$(1) $< V_S < 30V$; $T_A = -40°C$ to $+85°C$

Parameter	Symbol	Conditions	Limits			Units
			Min	Typ	Max	
Current Consumption						
Without Load at V_{REF} QOP, QSIP	I_S	C_T = 1 nF Frequency Generator with 100 kHz			20	mA
Standby Operation	I_{St}				3.5	mA
Hysteresis at V_S						
Turn-On Threshold for V_S Rising	V_{SH}	$V_{on\text{-}THR} \geq V_{on\text{-}THR\ H}$		8.3	9.6	V
Turn-Off Threshold for V_S Falling	V_{SL}			7.6		V
Reference Voltage						
Voltage	V_{REF}	I_{REF} = 1 mA T_A = 25°C V_S = 15V	2.475	2.5	2.525	V
Load Current	$-I_{REF}$		0		3	mA
Voltage Change	ΔV_{REF}	V_S ±20%			10	mV
Voltage Change	ΔV_{REF}	I_{REF} ±20%			3	mV

Characteristics $V_{S\,ON}$[1] < V_S < 30V; T_A = −40°C to +85°C (Continued)

Parameter	Symbol	Conditions	Limits			Units
			Min	Typ	Max	
Reference Voltage (Continued)						
Temperature Response	$\Delta V_{REF}/\Delta T$		−0.3		+0.3	mV/k
Response Threshold for I_{REF} Overcurrent	I_{OV}			7		mA
Short-Circuit Current	I_{SC}	V_{REF} = 0V		10		mA
Frequency Generator (VCO)						
Frequency Range	f_{VCO}				300	kHz
Frequency Change	Δf/fo	V_S ±20%			1	%
Tolerance	Δf/fo	C_T = 0.2 nF R_T = 50 kΩ T_A = 25°C	−7		+7	%
Charging Current for C_T (perm) = Current at Pin R_T	I_{RT}	$I_{RT} = V_{REF/RT}$	0		1	mA
Discharging Current for C_T	I_{dch}	Internally Fixed		2		mA
C_T Range[2]					1000	nF
Upper Switching Threshold	V_u			5		V
Lower Switching Threshold	V_l			2		V
Ramp Generator						
Frequency Range	f_R				300	kHz
Maximum Voltage at C_R	$V_{CR\,H}$			5.5		V
Minimum Voltage at C_R	$V_{CR\,L}$		1.65	1.8	1.95	V
Charging Current for C_R (perm) = Current at Pin R_R	I_{ch}	V_{RR} Approx. 0.7V	0		3	mA
Discharging Current for C_R	I_{dch}	Internally Fixed		3		mA
Ratio $I_{RR}/I_{CR\,charge}$		I_{RR} = 0.5 mA	0.95		1.1	
Comparator K 1						
Input Current	$I_{I\,K\,1}$				2	µA
Turn-Off Delay Time[3] (Signal Transit Time Input K 1 to Q SIP)					500	ns
Common-Mode Input Voltage Range	V_{IC}		0		V_{CRH}	V
Operational Amplifier						
Open-Loop Voltage Gain	G_{VO}		60	80		dB
Input Offset Voltage	V_{IO}	Pin 10 n.c.	−10		+10	mV
Input Current	$-I_{I\,op\,amp}$				2	µA
Common-Mode Input Voltage Range	V_{IC}		0		4	V
Output Current	$I_{Q\,op\,amp}$		0		2	mA
Output Voltage Range	$V_{Q\,op\,amp}$	0 mA < I_Q < 2 mA	0.5		V_{CRH}	V
Transition Frequency	f_T			3		MHz
Transition Phase	ϕ_T			120		degrees

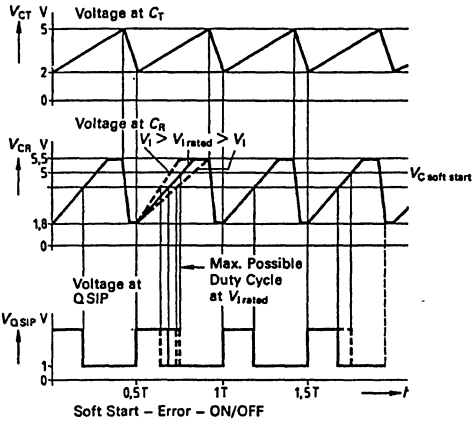
Notes:
1. $V_{S\,ON}$ means that $V_{S\,HIGH}$ has been exceeded, while $V_{S\,LOW}$ has not yet been exceeded.
2. C_T = 0.2 nF corresponds to a fall time of 0.2 µs (±30%) if the discharge current largely exceeds the charge current. The fall time equals the minimum dead time at the output.
3. Step function ΔV = −100 mV ⌐ ΔV = +100 mV, for transit time from input comparator to Q SIP.

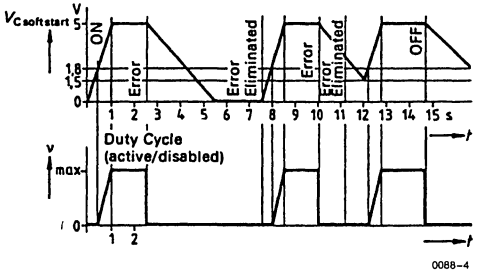
Characteristics $V_{S\,ON}$[1] < V_S < 30V; T_A = −40°C to +85°C (Continued)

Parameter	Symbol	Conditions	Limits			Units
			Min	Typ	Max	
Operational Amplifier (Continued)						
Temperature Coefficient of V_{IO}	TC		−30		+30	µV/K
Source Current at Q Op Amp	$I_{op\ amp}$	0.5V < V_Q < 5.5V		120		µA
Soft Start						
Charging Current for $C_{soft\ start}$	$-I_{ch}$			6		µA
Discharging Current for $C_{soft\ start}$	I_{dch}			2		µA
Upper Limiting Voltage	V_{lim}			5		V
Switching Voltage of K 2	$V_{K\,2}$			1.5		V
Dynamic Current Limitation K 5						
Input Current	$-I_{I\,DYN}$				2	µA
Input Offset Voltage	V_{IO}		−10		+10	mV
Common-Mode Input Voltage Range	V_{IC}		0		V_S − 3	V
Turn-Off Delay Time[6]	t	Rated Load 3 nF at Q SIP		250	400	ns
Undervoltage K 4						
Input Current at K 4	$-I_{I\,K\,4}$				0.2	µA
Switching Voltage at K 4	V_{SW}		V_{REF} − 10 mV		V_{REF} + 10 mV	V
Hysteresis Current	$I_{Hy\,4\,H}$ $I_{Hy\,4\,L}$	$V_{(+K\,4)}$ V_{SW} $V_{(+K\,4)}$ V_{SW}	12	18	25 0.1	µA µA
Turn-Off Delay Time[5]	t				3	µs
Overvoltage K 3						
Input Current	$-I_{I\,K\,3}$				0.2	µA
Switching Voltage	V_{SW}		V_{REF} − 10 mV		V_{REF} + 10 mV	V
Turn-Off Delay Time[5]	t				3	µs
Hysteresis Current	$-I_{Hy\,3\,H}$ $-I_{Hy\,3\,L}$	$V_{(-K\,3)} > V_{SW}$ $V_{(-K\,3)} < V_{SW}$	7	10	13 0.1	µA µA
Output Driver Q SIP						
Output Voltage High	V_{QH}	$I_{Q\,SIP}$ = −300 mA	V_S − 3			V
Output Voltage Low	V_{QL} V_{QL}	$I_{Q\,SIP}$ = +300 mA $I_{Q\,SIP}$ = +10 mA			2.1 1.4	V V
Output Current	$I_{Q\,SIP}$ $-I_{Q\,SIP}$	$C_{Q\,SIP}$ = 10 nF		500 300	700 500	mA[4] mA[4]
Input Standby I St						
Turn-On Threshold for $V_{I\,St}$ Rising	$V_{I\,St\,H}$	$V_S > V_{S\,ON}$	6.3	6.9	7.5	V
Turn-Off Threshold for $V_{I\,St}$ Falling	$V_{I\,St\,L}$		5.6	6.2	6.8	V
Hysteresis Current	$-I_{Hy\,St\,H}$ $I_{Hy\,St\,L}$	$V_{I\,St} > V_{I\,St\,H}$ $V_{I\,St} < V_{I\,St\,L}$	35	50	2 65	µA µA

Notes:
4. Dynamic maximum current during rising of falling edge.
5. Step function V_{REF} = −100 mV ↝ V_{REF} = +100 mV } for transit time from
6. Step function ΔV = −100 mV ↝ ΔV = +100 mV } input comparator to Q SIP.

Pulse Diagram





Ordering Information

Type	Ordering Code	Package
TDA 4919 G	Q67000-A8018	SO-20L
TDA 4919 A	Q67000-A8143	P-DIP 20

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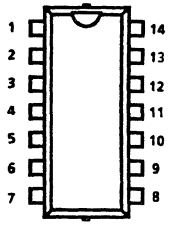
Preliminary

TLE 4950
Current Monitoring IC

- Input Currents Max. 25 μA, Meaning That Protective Resistors Can Be Connected in Series
- Effective Protection against Destruction by Voltage Surges in Automobiles
- Range of Supply Voltage 4.5V to 32V
- DIP 14 or SO 14 Package (TLE 4950 T)
- Input-Voltage Range Up to 32V, Independent of Supply Voltage
- Switching Threshold of Comparators Dependent on Supply Voltage, Corresponding to the Characteristic of Lamps
- Temperature Range $-40°C$ to $+125°C$

Pin Configuration

(Top View)



0110-8

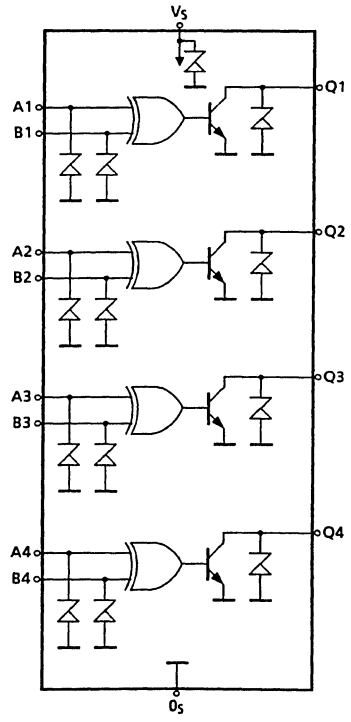
Pin Definitions

Pin	Symbol	Function
1	Q1	Output 1
2	A1	Input A1
3	B1	Input B1
4	Q2	Output 2
5	A2	Input A2
6	B2	Input B2
7	O_S	GND
8	Q3	Output 3
9	A3	Input A3
10	B3	Input B3
11	Q4	Output 4
12	A4	Input A4
13	B4	Input B4
14	V_S	Supply Voltage

This integrated circuit serves to monitor the performance of circuits, in particular the functioning of filament lamps in automobiles. The IC comprises four identical **comparator stages**, the logic function of which corresponds to an exclusive-OR gate. With each comparator, it is possible to monitor pairs of lamps or single lamps by means of the voltage drops across shunt resistors (R_S) in the positive supply line (See Application Circuits 1 and 2).

The inputs and outputs are protected internally by zener diodes. Protective resistors (R_P) can be connected in series because of small differential input currents. This provides a high degree of **protection against destruction** by the interfering voltages produced in an automobile.

Block Diagram



Current Monitoring of:

- Filament Lamps
- Electric Motors
- Relays
- Glow Plugs
- Circuits

Especially Suitable for:

- Automotive Electronics
- Industrial Plants

Circuit Description

The IC incorporates four identical comparator circuits. Each of these functional blocks has two equivalent inputs and an open-collector output Q. If the voltages differ by more than approximately 15 mV, the status changes from H (off-state) to L (on-state).

For an input voltage of <7V on both inputs the output can go H independent of the differential input voltage.

For an input voltage of <2.5V the output is securely off-state.

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Absolute Maximum Ratings*

Maximum ratings are absolute ratings; exceeding even one of these values may cause irreversible damage to the integrated circuit.

Maximum ratings for ambient temperature T_A of −40°C to +125°C.

Supply Voltage (V_S) ..... −0.5V to +32V
Input Voltages ($V_{A,B}$) ..... −0.5V to +32V
Output Voltages (V_Q) ..... −0.5V to +32V
Current through Protective Structures:
On Inputs A, B
(t < 2 ms) ($I_{SA,B}$) ..... −200 mA to +200 mA
On Inputs A, B
(t < 200 ms) ($I_{SA,B}$) ..... −50 mA to +50 mA
On Supply Pin V_S
(t < 2 ms) (I_{SV_S}) ..... −600 mA to +600 mA
On Output Q
(t < 2 ms) (I_{SQ}) ..... −400 mA to +400 mA
Voltage Surges Permissible Short-Term with Series Resistors R_P:

$$+V_{A,B,V_S,Q} = I_{SA,B,V_S,Q} \times R_{PA,B,V_S,Q} + 32V$$
$$-V_{A,B,V_S,Q} = -I_{SA,B,V_S,Q} \times R_{PA,B,V_S,Q}$$

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Operating Range

In the operating range the functions given in the circuit description will be fulfilled. However, deviations from the characteristics are possible.

Supply Voltage (V_S) ..... 4.5V to 32V
Ambient Temperature (T_A) ..... −40°C to +125°C
Common-Mode Input Range (V_{GI})
(Independent of V_S) ..... 7V to 32V

Characteristics

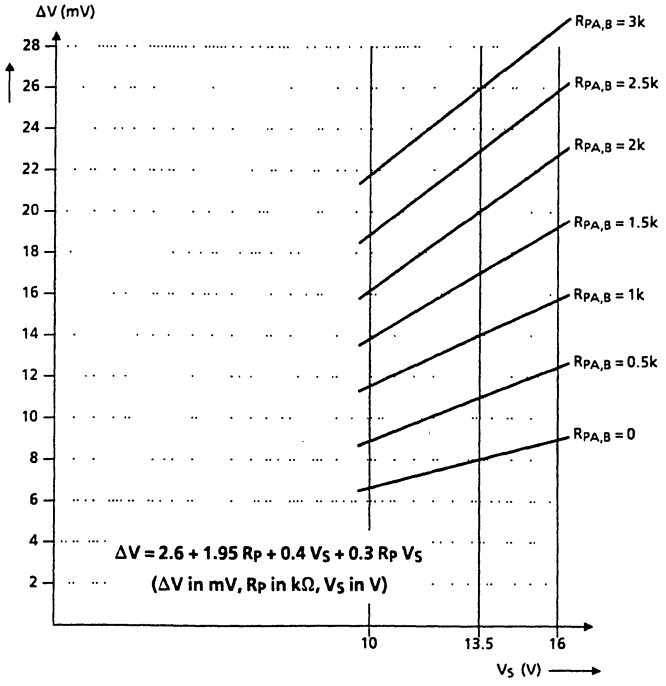
Characteristics are ensured over the operating range of the integrated circuit at the given supply voltage and ambient temperature. Typical characteristics specify mean values expected over the production spread.

Supply Voltage; V_S = 10V to 16V, Ambient Temperature; T_A = −30°C to +110°C

Parameter	Symbol	Test Circuit	Limits			Units
			Min	Typ	Max	
Current Consumption	I_S					
Q1 = Q2 = Q3 = Q4 = H		1			3	mA
Q1 = Q2 = Q3 = Q4 = L					8	mA
Switching Threshold						
with R_P = 1k; V_S = 13.5V	V_{Diff}*	2	7	14	20	mV
without R_P V_S = 13.5V	V_{Diff}*	1	4	8	12	mV
Input Current $V_A = V_B$	$I_{A,B}$	1			25	µA
Output Saturation Voltage I_Q = 30 mA	V_{QL}	1			0.4	V
Output Leakage Current V_{QH} = 32V	I_{QH}	1			10	µA

*$V_{Diff} = |V_A - V_B|$

Diagrams

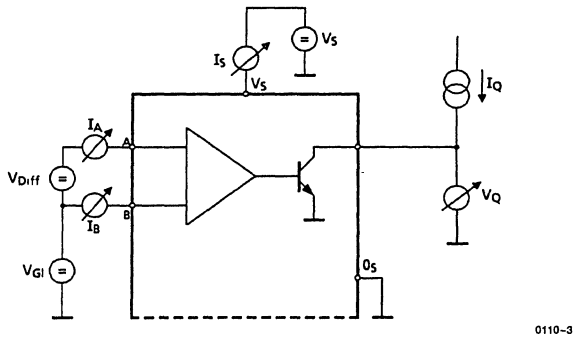


Differential Switching Voltage $\Delta V = f$(Supply Voltage V_S)

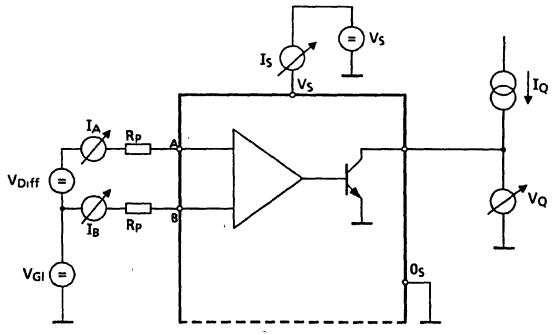
Parameter: Protective Resistors On
Inputs $R_{PA,B}$

The above function approximates to the function "Current Consumption vs. Supply Voltage" of a gas-filled tungsten filament lamp commonly found in automobiles.

Test Circuit 1

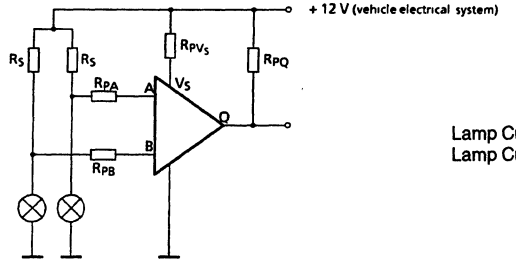


Test Circuit 2



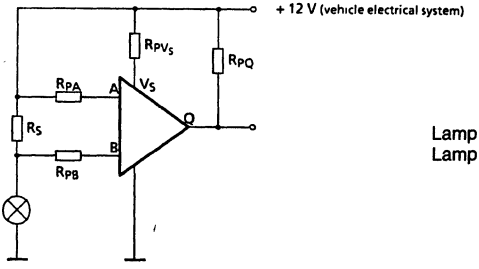
Application Circuits

Difference Measurement



Lamp Currents Same: Q = H
Lamp Currents Not Same: Q = L

Absolute-Value Measurement

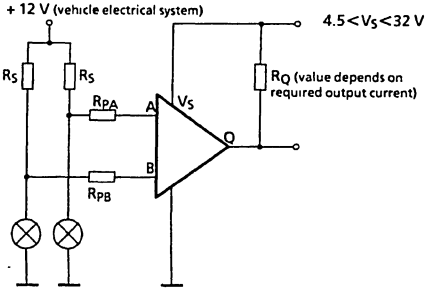


Lamp OK: Q = L
Lamp Defective: Q = H

Recommended Protective Resistors: RPA, B = 1 kΩ
RPVS = 100Ω
RPQ ≥ 500Ω

Application Circuits (Continued)

Voltage Supply Separate from Vehicle Supply



Recommended Protective Resistors: $R_{PA,B} = 1\ k\Omega$

With this application circuit it is also possible to prevent a so-called load dump ($R_{PA,B}$ may have to be chosen somewhat larger, see dimensioning notes under maximum ratings).

Ordering Information

Type	Ordering Code	Package
TLE 4950	Q 67000-A8171	DIP 14
TLE 4950 T	Q 67000-A8172	SO 14

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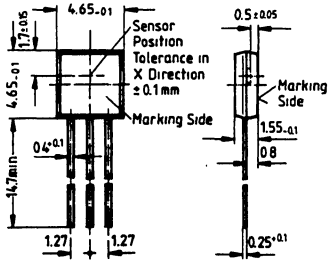
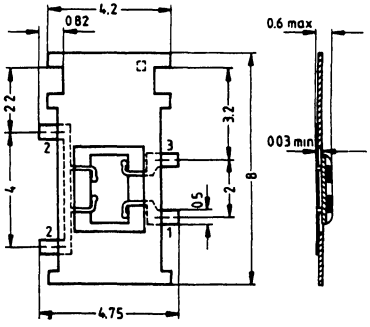
Package Outlines

Plastic flatpack, 3 pins

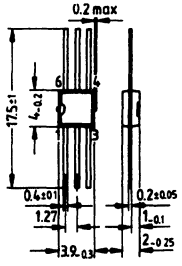


Approx. weight 0.1 g

Mikropack, 3 pins

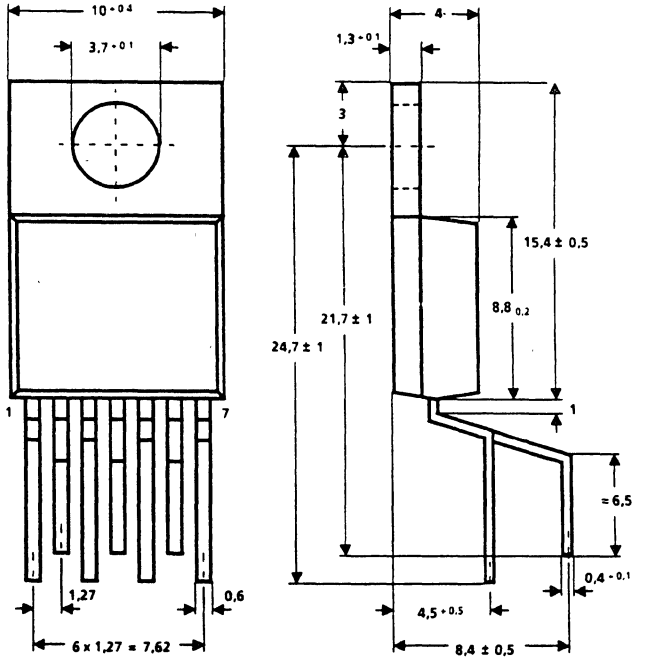


Miniature plastic package
6 pins



Approx. weight 0.1 g

Plastic power package, similar to TO-220
(with cooling strip and 7 pins)



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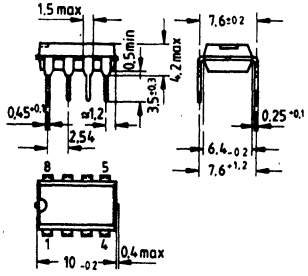
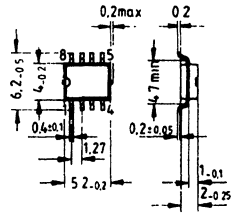
Package Outlines

Plastic package, P-DIP, 8 pins
20 A 8 DIN 41866



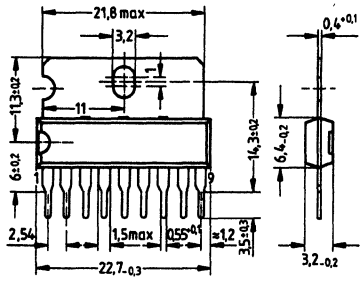
Approx. weight 0.7 g

Miniature plastic package SO-8 pins



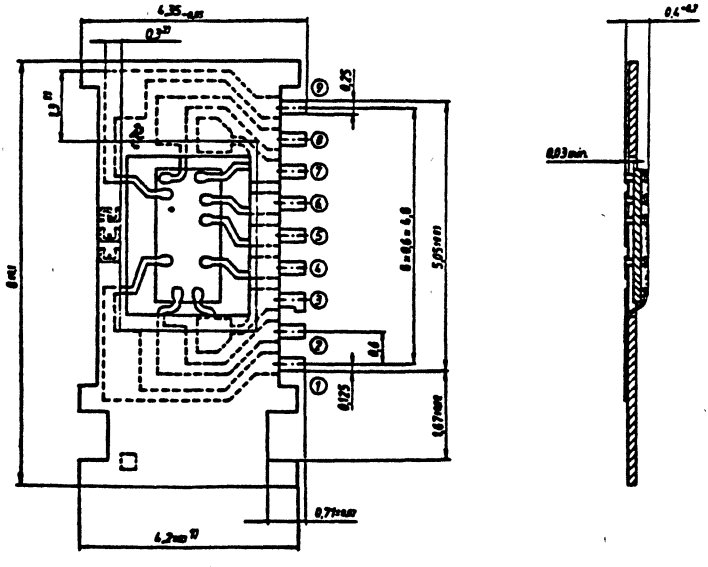
Approx. weight 0.15 g

Plastic power package with cooling fin
and 9 pins, SIP

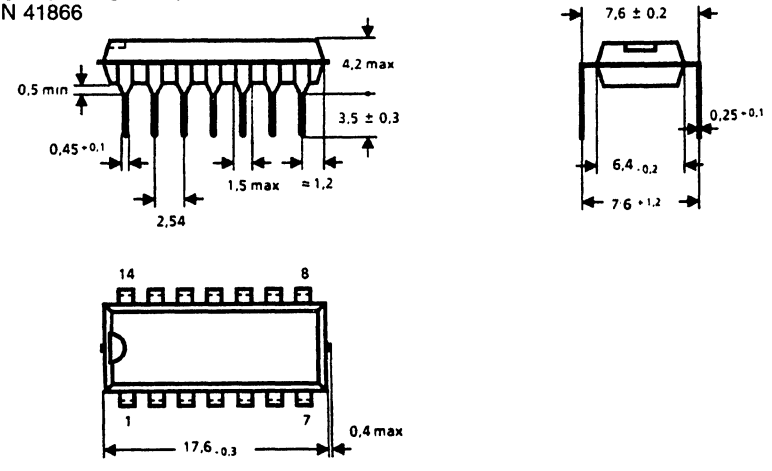


Approx. weight 1.9 g

Mikropack, 9 pins

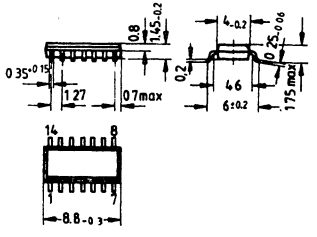


Plastic plug-in package, 14 pins, DIP
20 A 14 DIN 41866



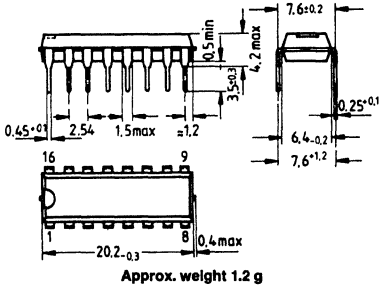
Approx. weight 1.1 g

Miniature plastic package (SMD),
14 pins (SO-14)



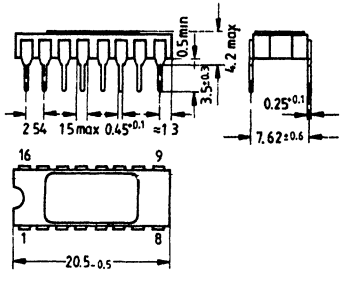
Approx. weight 0.13 g

Plastic package, P-DIP, 16 pins
20 A 16 DIN 41866



Approx. weight 1.2 g

Ceramic package, C-DIP, 16 pins



Approx. weight 1.4 g

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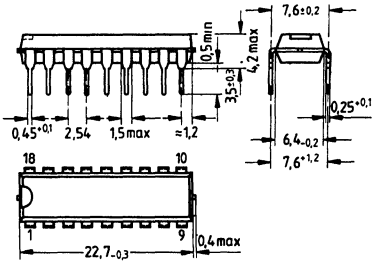
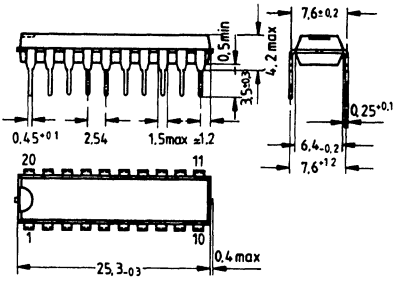
Plastic plug-in package, P-DIP, 18 pins
20 A 18 DIN 41866



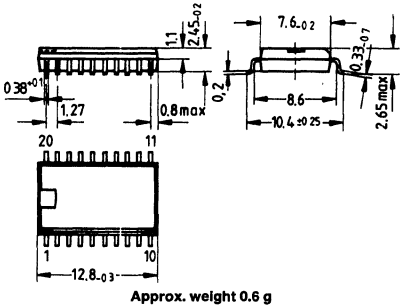
Approx. weight 1 3 g

Plastic package, P-DIP, 20 pins
20 A 20 DIN 41866



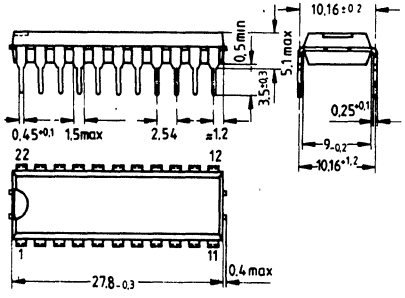
Approx. weight 1.5 g

Miniature plastic package (G), 20 pins
SO-20L (SMD)



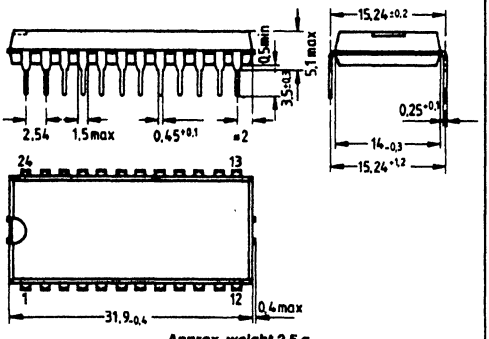
Approx. weight 0.6 g

Plastic package, P-DIP, 22 pins
20 D 22 DIN 41866



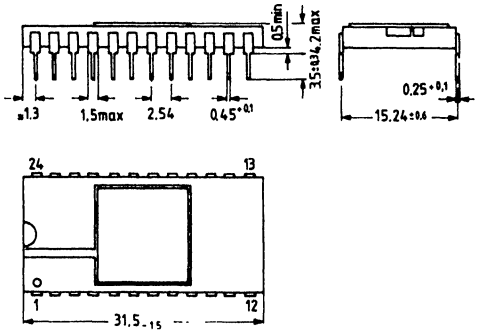
Approx. weight 2.1 g

Plastic package, P-DIP, 24 pins
20 B 24 DIN 41866



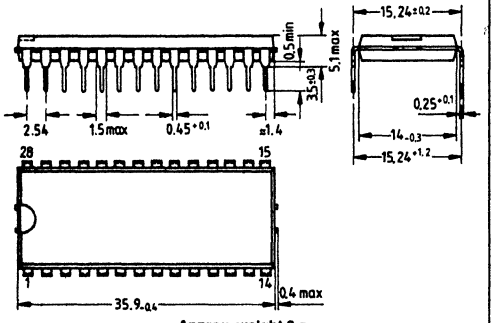
Approx. weight 2.5 g

Ceramic package, C-DIP, 24 pins



Approx. weight 3 g

Plastic package, P-DIP, 28 pins
20 B 28 DIN 41866



Approx. weight 3 g

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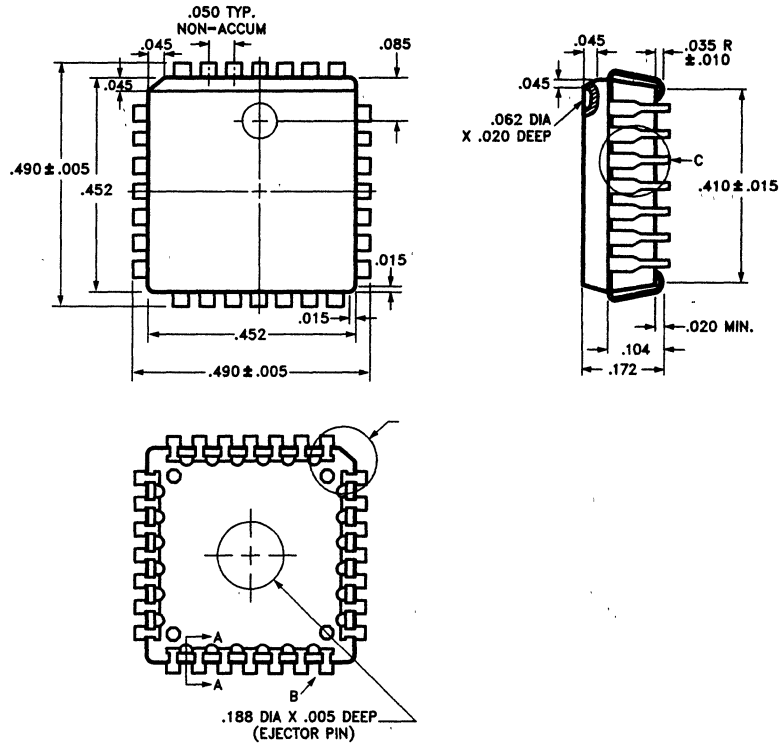
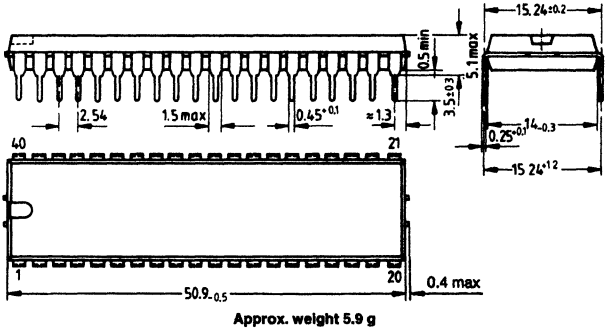
Plastic package, LCC, 28 pin

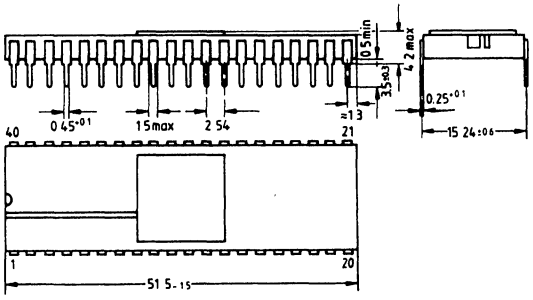


Plastic package, P-DIP, 40 pins
20 B 40 DIN 41866



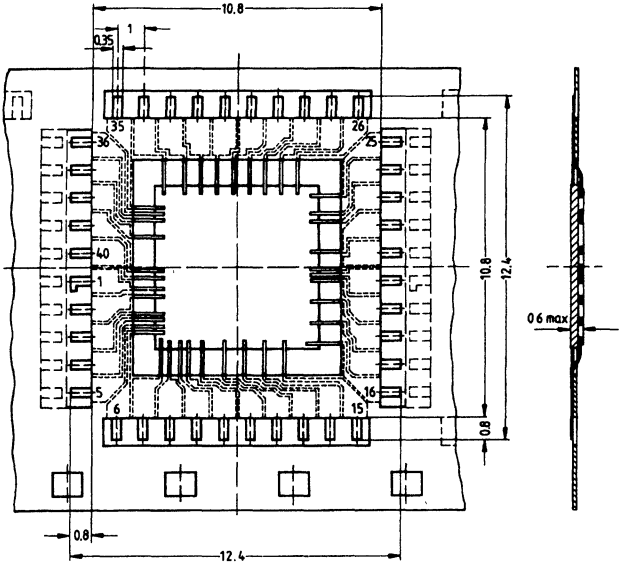
Approx. weight 5.9 g

Ceramic package, C-DIP, 40 pins



Approx. weight 6.8 g

Mikropack, 16mm, 40 pins (SMD)
20 B 40 DIN 41866



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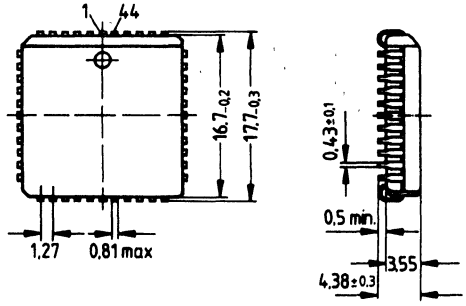
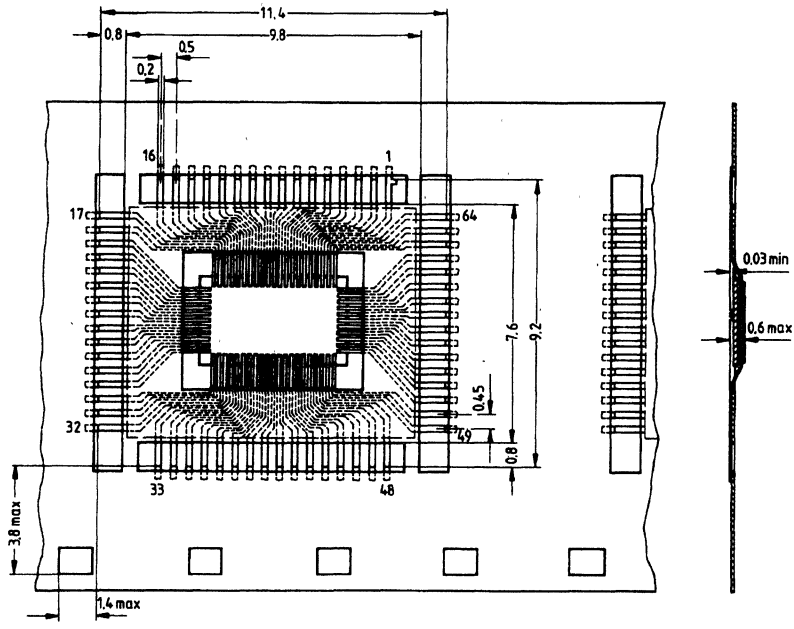
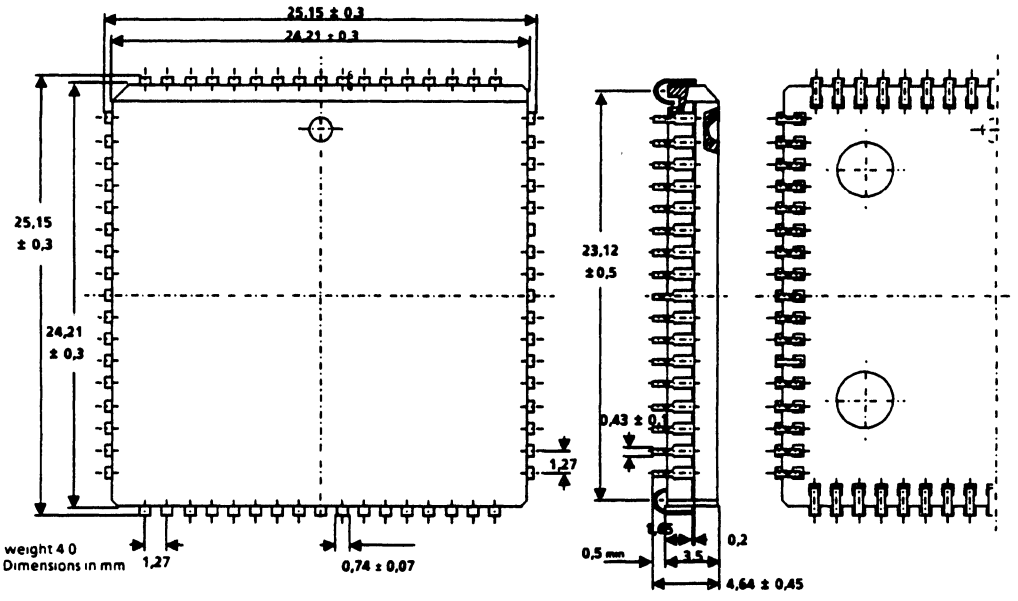
Plastic package, 44 pins, PLCC (SMD)



Mikropack, 16 mm, 64 pins (SMD)



Plastic package, 68 pins, PLCC (SMD)



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