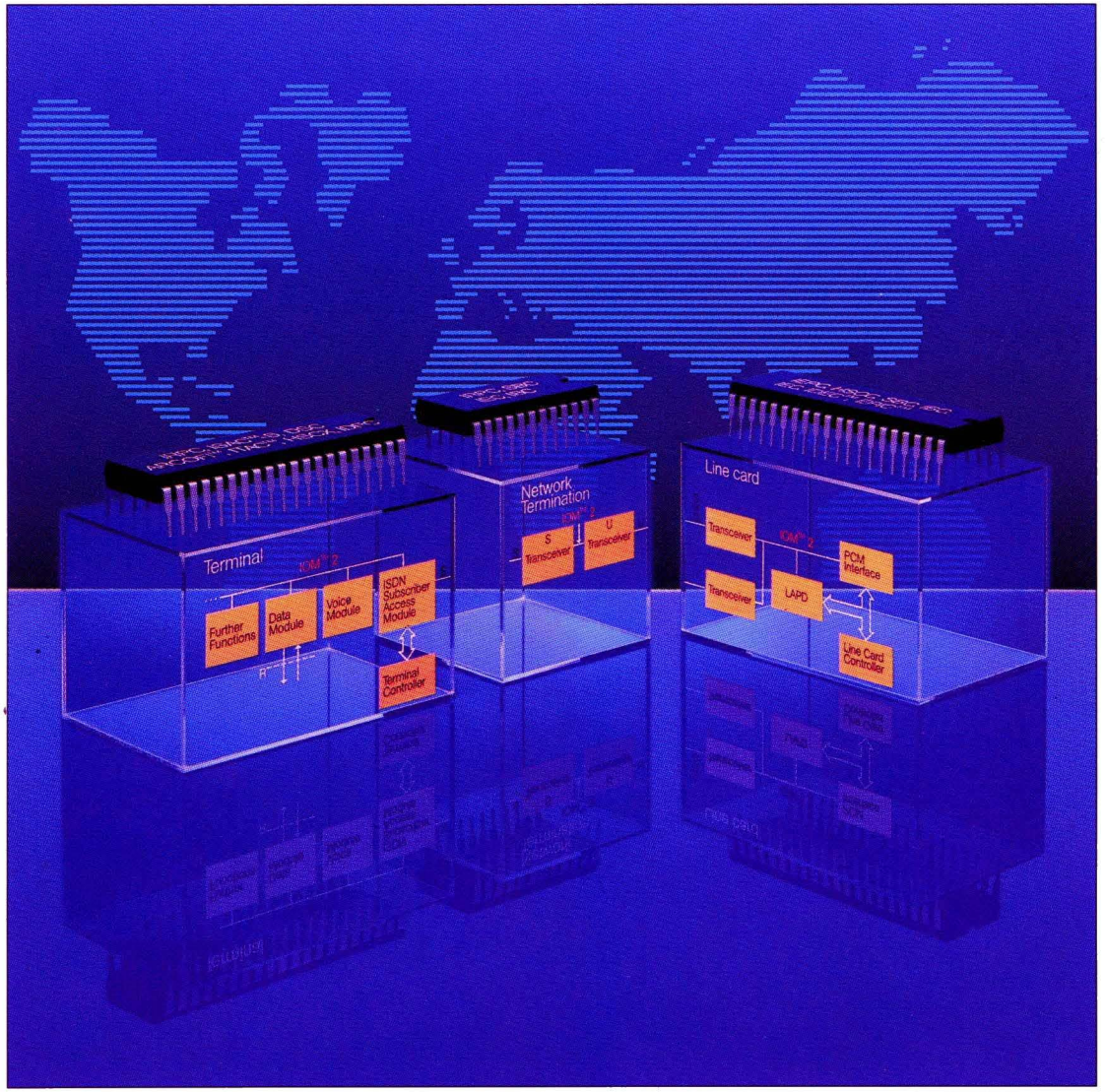
SIEMENS

ICs for Communications

Databook 1990/91



ICs for Communications

Data Book 1990/91

Siemens Components, Inc.

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▼= New Type
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1.2 Types in Application-Oriented Order

ICs for Data Communication **Page**

Advance Information

General Information

1. Type-Designation Code for ICs

IC type designations are based on the European Pro Electron system. The code system is explained in the Pro Electron brochure D 15*), edition 1988.

*) Available from Pro Electron, Avenue Louise, 430 (B.12)
B-1050 Brussels, Belgium.

2. Mounting Instructions

Plastic and Ceramic Packages

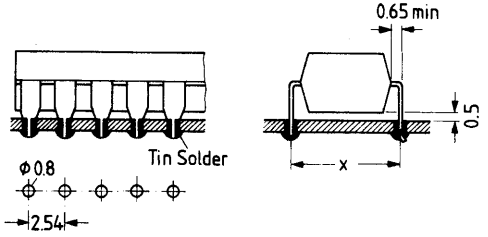
The pins of the cases are bent downwards by an angle of 90° and fit into holes with a diameter of between 0.7 and 0.9 mm spaced 2.54 mm apart. The dimension x is given in the corresponding drawing.

The bottom of the package will not touch the PC board after insertion because the pins have shoulders just below the package **(see figure 1).**

After insertion of the package into the PC board it is advisable to bend the ends of two pins at an angle of approx. 30° to the board so that the package does not have to be pressed down during soldering. The packages are soldered on that side of the PCB facing away from the package.

The maximum permissible soldering temperature is 350 °C (max. 3 s) for manual soldering and 260 °C (max. 10 s) for dip soldering and wave soldering.

Figure 1



Dimensions in mm

Plastic Packages (P-DSO and PL-CC) for Surface Mounting (SMD)

Iron soldering:	soldering temperature 350 °C for max. 3 s; minimum distance between package and soldering point 1.5 mm package temperature max. 150 °C; no mechanical stress on the pins
Vapor phase soldering:	soldering temperature 215 °C, max. soldering time 40 s, 2 x.
Wave soldering:	soldering temperature 260 °C, max. soldering time 8 s. (pins and package are dipped into the tin bath)

Storage, Pretreatment for Processing of ICs in PL-CC Packages

The components are to be stored in a dry place. For soldering methods which may lead to a thermal shock stress (e.g. vapor phase soldering) it is recommended to dry the ICs in PL-CC package at 125 °C for a period of 24 hours.

Other Points to Note

Ensure that no current is able to flow between the solder bath or soldering iron and the PCB. It is advisable to ground the pins that are to be soldered as well as the solder bath or soldering iron.

When they are being prepared and inserted in a PCB, circuits should be protected against static charging. Under no circumstances may the components be removed or inserted whilst the operating voltage is switched on.

The increase in chip temperature during the soldering process results in a temporary increase in electrostatic sensitivity of integrated circuits. Special precautions should therefore be taken against line transients, e.g. through the switching of inductances on magnetic chutes, etc.

MIKROPACK (SMD)

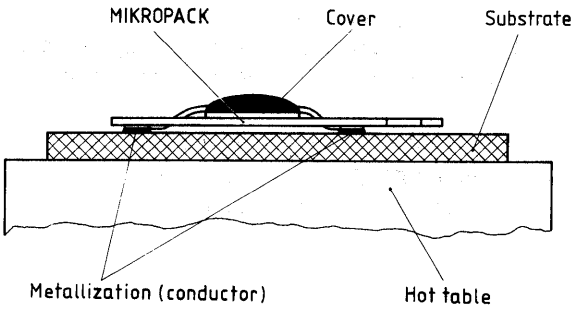
MIKROPACK components are delivered on film reels.

Mounting Suggestions

a) We recommend vapor phase soldering: soldering temperature 215 °C, soldering time max. 40 s.

b) For prototypes and small quantities (up to approximately 50.0 items/y), the hot table soldering method can also be used **(figure 2).**

Figure 2



Required Equipment and Accessories

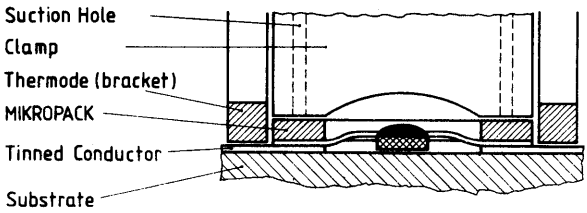
- cutting device
- hot table, temperature regulated (e.g. Weld-Equip, Unitek)
- stereo microscope (e.g. Wild, Zeiss, magnification 6...40 times)
- substrate material: epoxy resin; hard paper; ceramic (thick thin film)

Soldering Data

- soldering temperature: 210 °C max.
- solder coating on substrate: Pb/Sn (e.g. 60/40) wave-tinned or electrodeposited
- soldering time: approx. 10 s
- flux: e.g. colophony, dissolved in alcohol
- cleaning agents (as required): e.g. Freon TP-35, TE, TF

c) For large quantities (e.g. more than 50.0 items/y) thermode soldering is also suitable **(figure 3).**

Figure 3



Required Equipment

- soldering equipment (e.g. Weld-Equip, Farco, Jade)
- substrate material: epoxy resin; hard paper; flexible materials, e.g. polyamide

Soldering Data

- soldering temperature: 220 °C max.
- solder coating on the substrate: Pb/Sn (e.g. 60/40), wave-tinned or electro-deposited
- soldering time: approx. 10 s
- flux: e.g. colophony dissolved in alcohol
- cleaning agents (as required); e.g. Freon TP-35, TE, TF

3. Processing Guidelines for ICs

Integrated circuits (ICs) are **e**lectrostatic-**s**ensitive (ESS) devices. The demand for greater packing density has led to smaller structures on semiconductor chips, with the result that today every IC, whether bipolar, MOS, or CMOS, has to be protected against electrostatics.

MOS and CMOS devices generally have integrated protective circuits and it is virtually impossible for them to be destroyed by purely static electricity. On the other hand, there is acute danger from **e**lectrostatic **d**ischarges (ESD).

Of the multitude of possible sources of discharge, charged devices should be mentioned in addition to charged persons. Low-resistive discharges can produce peak powers amounting to kilowatts.

For the protection of devices the following principles should be observed:

a) Reduction of charging voltage, below 200 V if possible.
Means which are effective here are an increase in relative humidity to $\geq 60\%$ and the replacement of highly charging plastics by antistatic materials.

b) With every kind of contact with the device pins a charge equalization is to be expected. This should always be highly resistive (ideally $R = 10^6$ to $10^9\ \Omega$).

All in all this means that ICs call for special handling, because uncontrolled charges, voltages from ungrounded equipment or persons, surge voltage spikes and similar influences can destroy a device. Even if devices have protective circuits (e.g. protective diodes) on their inputs, the following guidelines for their handling should nevertheless be observed.

Identification

The packing of ESS devices is provided with the following label by the manufacturer: 

Scope

The guidelines apply to the storage, transport, testing, and processing of all kinds of ICs, equipped and soldered circuit boards that comprise such components.

Handling of Devices

1. ICs must be left in their containers until they are processed.
2. ICs may only be handled at specially equipped work stations. These stations must have work surfaces covered with a conductive material of the order of 10^6 to $10^9\ \Omega$/cm.
3. With humidity of $> 50\%$ a coat of pure cotton is sufficient. In the case of chargeable synthetic fibers the clothing should be worn close-fitting. The wrist strap must be worn snugly on the skin and be grounded across a resistor of 50 to 100 kΩ.
4. If conductive floors, $R = 5 \times 10^4$ to $10^7\ \Omega$ are provided, further protection can be achieved by using so-called MOS chairs and shoes with a conductive sole ($R \approx 10^5$ to $10^7\ \Omega$).

5. All transport containers for ESS devices and assembled circuits boards must first be brought to the same potential by being placed on the work surface or touched by the operator before the individual devices may be handled. The potential equalization should be across a resistor of 10^6 to 10^8 Ω.
6. When loading machines and production devices it should be noted that the devices come out of the transport magazine charged and can be damaged if they touch metal, e.g. machine parts.

   Example 1) conductive (black) tubes.
   The devices may be destroyes in the tube by charged persons or come out of the tube charged if this is emptied by a charged person.
   Conductive tubes may only be handled at ESS work stations (high-resistance work-station and person grounding).

   Example 2) anti-static (transparent) tubes.
   The devices cannot be destroyed in the tube by charged persons (there may be a rare exception in the case of custom ICs with unprotected gate pins). The devices can be engangered as in 1) when the tube is emptied if the latter, especially at low humidity, is no longer sufficiently anti-static after a long period of storage (> 1 year).

   In both cases damage can be avoided by discharging the devices across a grounded adapter of high-resistance material (≈ 10^6 to 10^8 Ω/cm) between the tube and the machine.

   The use of metal tubes – especially of anodized aluminium – is not advisable because of the danger of low-resistance device discharge.

Storage

ESS devices should only be stored in identified locations provided for the purpose. During storage the devices should remain in the packing in which they are supplied. The storage temperature should not exceed 60 °C.

Transport

ESS devices in approved packing tubes should only be transported in suitable containers of conductive or longterm anti-static-treated plastic or possibly unvarnished wood. Containers of both high-charging plastic or very low-resistance materials are unsuitable.

Transfer cars and their rollers should exhibit adequate electrical conductivity ($R < 10^6$ Ω). Sliding contacts and grounding chains will not reliably eliminate charges.

Incoming Inspection

In incoming inspection the above guidelines should be observed. Otherwise any right to refund or replacement if devices fail inspection may be lost.

Material and Mounting

1. The drive belts of machines used for the processing of the devices, in as much as they come into contact with them (e.g. bending and cutting machines, conveyor belts), should be treated with anti-static spray (e.g. anti-static spray 100 from Kontakt-chemie). It is better, however, to avoid the contact completely.

2. If ESS devices have to be soldered or desoldered manually, soldering irons with thyristor control may not be used. Siemens EMI-suppression capacitors of the type B 81711-B31...-B36 have proven very effective against line transients.
3. Circuit boards fitted and soldered with ESS devices are always to be considered as endangered.

Electrical Tests and Application Circuit

1. The devices should be processed with observation of these guidelines. Before assembled and soldered circuit boards are tested, remove any shorting rings.
2. The sockets or integrated circuits must not be conducting any voltage when individual devices or assembled circuit boards are inserted or withdrawn, unless works' specifications state otherwise. Ensure that the test devices and power supplies do not produce any voltage spikes, either when being turned on and off in normal operation or if the power fuse blows or other fuses respond.
3. When supplying bipolar integrated circuits with current, the negative voltage ($-V_S$ or GND) has first to be connected. In general, an interruption of this potential during operation is not permissible.
4. Signal voltages may only be applied to the inputs of ICs when or better after the supply voltage is turned on. They must be disconnected when or better before the supply voltage is turned off.
5. Power supplied of integrated circuits are to be blocked as near as possible at the supply terminals of the IC. With bipolar ICs it is recommended to use a low-inductance electrolytic capacitor or at least a paralleled cermaic capacitor of 100 nF to 470 nF for example.

   Using ICs with high output currents, the necessary value of the electrolytic capacitor must be adapted to the test or application circuit. Transient behavior and dynamic output resistance of the power supplied, line inductances in the supply and load circuit and in particular inductive loads or motors have to be considered. When switching off line inductances of inductive loads, the stored power has to be consumed externally, unless otherwise specified (e.g. by an electrolytic capacitor, diodes, Z diodes or the power supply). Also a switching off of the supply voltage prior to the load rejection should be taken into account.
6. ICs with low-pass character of the output stages (e.g. PNP drivers or PNP/NPN end stages), normally need an additional external compensation at the output. This applies particularly to complex loads. The output of AF power amplifiers is compensated by the Boucherot element. In individual cases, bridge circuits only need a capacitance for bypassing the load. Depending on the application it is, however, also recommended to connect one capacitor from each output to ground.
7. Observe any notes and instructions in the respective data books.

Packing of Assembled PC Boards or Flatpack Units

The packing material should exhibit low volume conductivity:
$10^5\ \Omega/cm < \rho < 10^{10}\ \Omega/cm$.

In most cases – especially with humidity of > 40% – this requirement is fulfilled by simple corrugated board. Better protection is obtained with bags of conductive polyethylene foam (e.g. RCAS 1200 from Richmond of Redlands, California).

One should always ensure that boards cannot touch.

In special cases it may be necessary to provide protection against strong electric fields, such as can be generated by conveyor belts for example. For this purpose a sheath of aluminium foil is recommended, although direct contact between the film and the PCB must be avoided. Cardboard boxes with an aluminium-foil lining, such as those used for shipping our devices, are available from Laber of Munich.

Ultrasonic Cleaning of ICs

The following recommendation applies to plastic packages. For cavity packages (metal and also ceramic) separate regulations have to be observed.

Freon and isopropyl alcohol (trade name: propanol) can be used as solvents. These solvents can also be used for plastic packages because they do not eat into the plastic material.

An ultrasonic bath in double halfwave operation is advisable because of the low component stress.

The ultrasonic limits are as follows:

sound frequency	f	> 40 kHz
exposure	t	< 2 min
alternating sound pressure	p	< 29 kPa
sound power	N	< 0.5 W/cm²/liter

4. Data Classification

Maximum Ratings

Maximum ratings are absolute ratings; exceeding any one of these values may cause irreversible damage to the integrated circuit.

Characteristics

The listed characteristics are ensured over the operating range of the integrated circuit. Typical charateristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at $T_A = 25\,°C$ and the given supply voltage.

Operating Range

In the operating range the functions given in the circuit description are fulfilled.

5. Quality Assurance

The high quality and reliability of integrated circuits from Siemens are the results of carefully managed design and production which is systematically checked and controlled at each stage.

The procedures are subject to a quality assurance system; full details are given in the brochure "Quality Assurance – Integrated Circuits".

Figure 1 and 2 show the most important stages of QA system. Quality assurance (QA) department independent of production and development are responsible for the selected measures, acceptance procedures and information feedback loops. Operating QA departments have stat-of-the-art test and measuring equipment at is disposal, work according to approved methods of statistical quality control, and provided with facilities for accelerate life and are environmental tests used for both qualification and routine monitoring tests.

The latest methods and equipment for preparation and analysis are employed to achieve continuity of quality and reliability.

Conformance

Each integrated circuit is subjected to a final test at the end of the production process. These are carried out by computer-controlled, automatic test systems because hundreds of thousands of operating conditions as well as a large number of static and dynamic parameters have to be considered. Moreover, the test systems are extremely reliable and reproducible. The quality assurance department carries out a final check in the form of a lot-by-lot sampling inspection to additionally ensure this minimum percent defectives as well as the acceptable quality level (AQL). Sampling inspection is performed in accordance with the inspection plans of DIN 40080, as well as of the identical MIL-STD-105 or IEC 410.

Figure 1

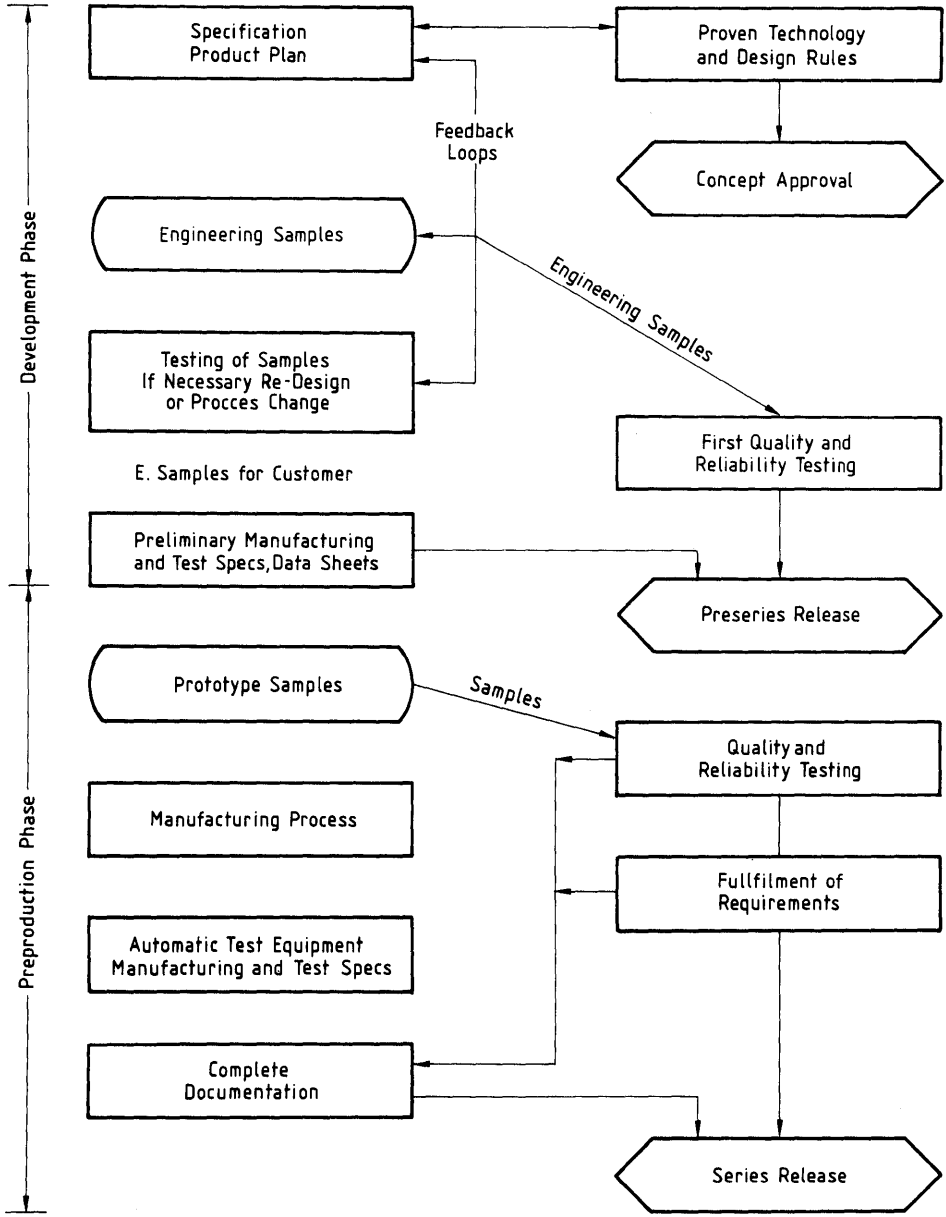
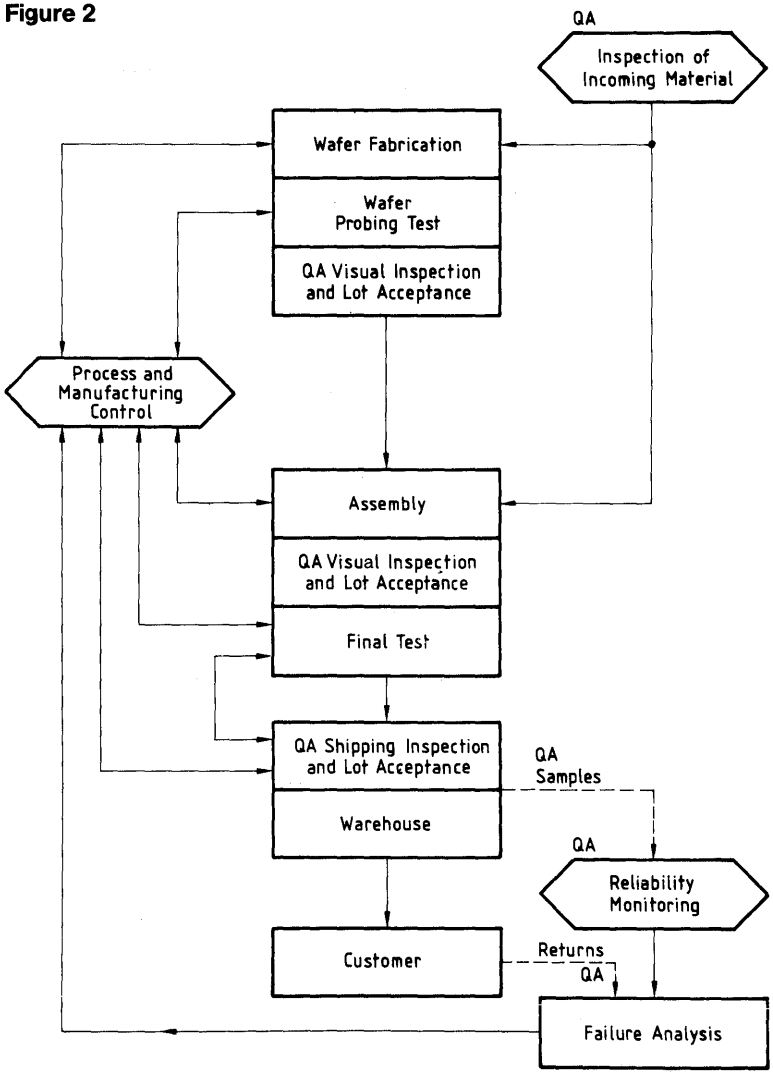

Development Phase
Preproduction Phase
Specification
Product Plan
Proven Technology
and Design Rules
Feedback
Loops
Concept Approval
Engineering Samples
Engineering Samples
Testing of Samples
If Necessary Re-Design
or Procces Change
First Quality and
Reliability Testing
E. Samples for Customer
Preliminary Manufacturing
and Test Specs,Data Sheets
Preseries Release
Prototype Samples
Samples
Quality and
Reliability Testing
Manufacturing Process
Fullfilment of
Requirements
Automatic Test Equipment
Manufacturing and Test Specs
Complete
Documentation
Series Release

Figure 2



Reliability

Measures Taken during Development

The reliability of ICs is already considerably influenced at the development stage. Siemens has, therefore, fixed certain design standards for the development of circuit and layout, e.g. specifying minimum width and spacing of conductive layers on a chip, dimensions and electrical parameters of protective circuits for electrostatic charge, etc. An examination with the aid of carefully arranged programs operated on large-scale computers, guarantees the immediate identification and elimination of unintentional violations of these designs standards.

In-Process Control during Production

The manufacturing of integrated circuits comprises several hundred production steps. As each step is to be executed with utmost accuracy, the in-process control is of outstanding importance. Some processes require more than a hundred different test measures. The tests have been arranged such that the individual process steps can be reproduced continuously.

The decreasing failure rates reflect the never ending effort in this direction; in the course of the years they have been reduced considerably despite an immense rise in IC complexity.

Reliability Monitoring

The general course of the IC failure rate versus time is shown by a so-called "bathtub" curve. The failure rate has its peak during the first few operating hours (early failure period). After the early failure period has decayed, the "constant" failure rate period starts during which the failures may occur at an approximately uniform rate. This period ends with a repeated rise of the curve during the wear-out failure period. For ICs, however, the latter period usually lies far beyond the service life specified for the individual equipment.

Reliability tests for ICs are usually desctructive examinations. They are, therefore, carried out with samples. Most failure mechanisms can be accelerated by means of higher temperatures. Due to the temperature dependence of the failure mechanisms, it is possible to simultane future operational behavior within a short time by applying high temperatures; this is called life test.

The acceleration factor B for the life test can be obtained from the Arrhenius equation

$$B = \exp\left(\frac{E_A}{k}\left(\frac{1}{T_1} - \frac{1}{T_2}\right)\right)$$

where T_2 is the temperature at which the life test is performed, T_1 is the assumed operating temperature, and k is the Boltzmann constant.

Important for factor B is the activation energy E_A. It lies between 0.3 and 1.3 eV and differs considerably for the individual failure mechanisms.

For all Siemens ICs, the reliability data from life tests is converted to an operating temperature of $T_A = 40\,°C$, assuming an average activation energy of 0.4 eV. The acceleration factor for life tests at 125 °C is thus 24, compared with operational behavior. This method considers also failure mechanisms with low activation energy, i.e. which are only slightly accelerated by the temperature effect.

Various reliability tests are periodically performed with IC types that are representative of a certain production line – this is described in the brochure "Quality Assurance-Integrated Circuits". Such tests are e.g. humidity test at 85 °C and 85% relative humidity, pressure cooker test, as well as life tests up to 1000 hours and more. Test results are available in the form of summary reports.

6. Summary of the Most Important Symbols

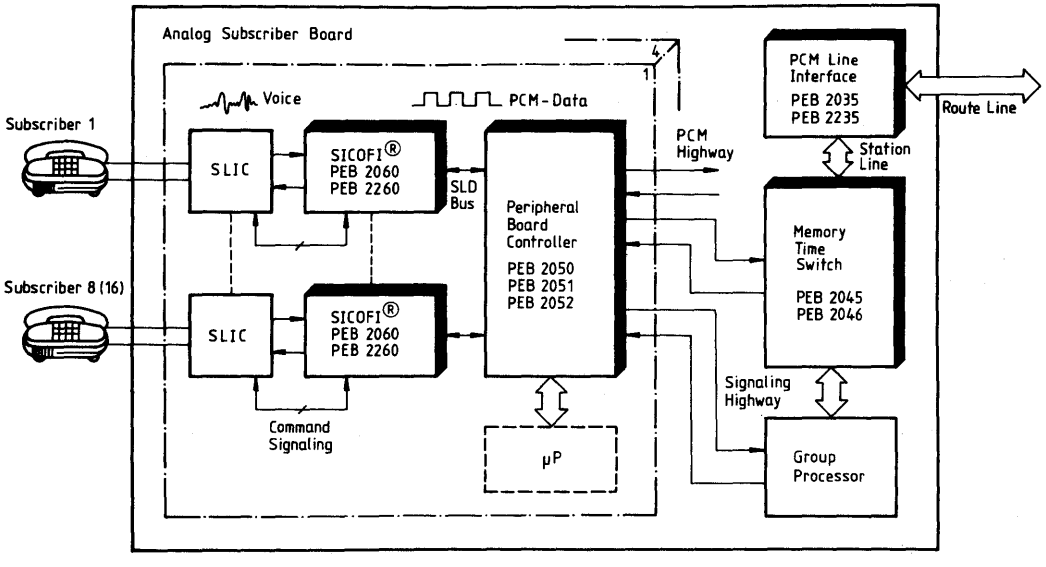
b	Pulse duration
B	Current gain
B	Bandwidth
BI	Input of output amplifier
BO	Output of output amplifier
C	Capacitance
C_I	Input capacitance
C_{ICLK}	Input capacitance of the clock input
C_L	Load capacitance
D	Data input
DO	Data output
E	Enable
F_I	Input load factor
F_O	Output load factor
F_{OH}	Output load factor, H signal
F_{OL}	Output load factor, L signal
f_I	Input frequency
f_{CL}, f_Φ	Clock frequency
f	Maximum counter frequency
I_{DD}	Drain supply current
I_I	Input current
I_{IH}	H-input current
I_{IL}	L-input current
I	Input
I1	Input 1
I2	Input 2
I	Input bias current
I_{OO}	Output offset current
I_O	Short-circuit output current
I_{OH}	H-output current
I_{OL}	L-output current
I_{SH}	H-supply current
I_{SL}	L-supply current
MO	Mixer output
0_S, GND	Ground, earth
P_{tot}	Total power consumption
P_O	Output power
CLK	Clock
O	Output
$\overline{O}$	Output, inverted

R	Resistance
R_G	Generator resistance
R_I	Input resistance
R_{CL}	Collector load resistance
R_L	Load resistance
R_P	Adjustmente resistance
R_{thJA}	Therminal resistance (Junction to ambient)
R_{OH}	H-output resistance
R_{OL}	L-output resistance
R_O	Load resistance at output
T_A	Ambient temperature
T_{stg}	Storage temperature
T_{case}	Case temperature
T_j	Junction temperature
TC	Temperature coefficient
t_d	Pulse delay time
$t_{DHL\ O}$	Delay time of the HL transition of the output signal
$t_{DLH\ O}$	Delay time of the LH transition of the output signal
t_{DLH}	Delay time
t_H	Hold time
t_I	Input pulse duration
t_n	Bit time before clock pulse
t_{n+1}	Bit time after clock pulse
t_P	Average signal propagation time
t_{SYD}	Delay time
t_{CLKY}	Clock period
t_{PHL}	Signal propagation time (from H to L)
$t_{PHLR,S}$	Signal propagation time (set, reset input)
t_{PD}	Pair-delay time
t_{pR}	Reset pulse duration
$t_{PR,S}$	Average signal propagation time (set, reset input)
t_{pS}	Set pulse duration
t_d	Key debounce time
t_p	Key depression period
t_{pC}	Counting pulse duration
t_T	Transmission time – t_r rise time, t_f fall time
t_r	Recovery time
t_S	Setup time
t_O	Output pulse duration
t_{THL}	Signal transition time (from H to L)
t_{TLH}	Signal transition time (from L to H)
$t_{THL\ O}$	Signal transition time H-L of the output signal
$t_{TLH\ O}$	Signal transition time L-H of the output signal

t_{SH}	H-setup time
t_{SHI}	H-setup time, left shift pulse
t_{SHr}	H-setup time, right shift pulse
t_{SL}	L-setup time
t_{SLI}	L-setup time, left shift pulse
t_{SLr}	L-setup time, right shift pulse
$t_{WH\,I}$	Pulse width of the H-input signal
$t_{WL\,I}$	Pulse width of the L-input signal
$t_{THL\,I}$	HL-transition time of the input signal
$t_{TLH\,I}$	LH-transition time of the input signal
$t_{WH\,O}$	Pulse width of the H-output signal
t_W	Pulse width
V	Voltage, general
V_S	Supply voltage
V_{nm}	Noise margin
V_{BB} V_{EE}	Negative supply voltage
V_{CC}	Positive supply voltage
V_{SS}	Substrate supply voltage
V_{DD}	Drain supply voltage
V_{GG}	Gate supply voltage
V_{IH}	H-input voltage at information input
V_{IL}	L-input voltage at information input
V_{OH}	H-output voltage
$\overline{V_{OH}}$	Inverted output voltage V_{OH}
V_{OL}	L-output voltage
$\overline{V_{OL}}$	Inverted output voltage V_{OL}
V_{DI}	Differential input voltage
V_{cm}	Input common mode voltage
V_n	Noise voltage
V_F	Functional voltage range
V_I	Input voltage at information input
V_R	Reset voltage
Z_I	Input impedance
Z_O	Output impedance

ICs for Digital Exchange Systems

- **Analog Subscriber Boards**
- **Switching Network**
- **Primary Access**



In a digital exchange system the subscriber line boards provide the link between the subscriber and the switching network. The basic functions of analog line boards are known under the acronym BORSHT (**b**attery, **o**vervoltage, **r**ising, **s**upervision, **h**ybrid, **t**esting). Moreover, further important tasks are voice frequency band limitation, analog to digital conversion into time discrete digital equivalents, time-slot assignment on the PCM highways and handling of signaling and control information.

Up to now implementation has been characterized by fixed adjustment of line interface conditions although telephone line conditions vary considerably with national standards and even with subscriber line installations. Under adverse conditions telecommunication equipment must match the subscriber line and termination impedances while suppressing return echoes in the two- to four-wire hybrid network. Compensating for line attenuation is just as critical for balancing the voice signals in the transmission and reception paths.

To improve voice quality, subscriber line boards have to be matched to different line conditions by means of interchangeable discrete components. This approach is very costly regarding line board design and manufacturing. Furthermore, the reliability of a board filled with parts, wires and connections will decrease rapidly.

The subscriber line board architecture proposed by Siemens Components Group and supported by several other companies is geared to eliminate many of these line board trouble spots.

Optimized Line Board Architecture

The key device for both analog and digital subscriber line boards is the **P**eripheral **B**oard **C**ontroller (PBC) PEB 2050/51. Basically the PBC is a highly intelligent multiplexer/ demultiplexer chip which performs the variable time-slot assignment for up to 16 PCM channels and handles the data streams for control and signaling. It constitutes the interface between the subscriber line devices such as decoded filter or ISDN communication controller, the PCM lines, the central control unit and the optional onboard microprocessor.

As a characteristic architectural feature, for test, monitoring and control purposes, the device permits efficient switching of data streams between all these interfaces and, therefore, ensures transparency between the PCM channels and control or signaling data. This opens up attractive possibilities such as common-channel signaling and microprocessor access to PCM data.

Due to the importance of reliability in system design, the PBC provides a backplane interface with two or four fully redundant PCM highways. For the exchange of information between a central control unit and the PBC working as a "slave" in a point-to-multipoint configuration, the device supports a subset of the CCITT's High Level Data Link Control (HDLC) communications protocol so that it can respond to certain HDLC frames without microprocessor intervention or software supervision.

The hardwired implementation of the physical level of the HDLC protocol (e.g. cyclic redundancy check) and of parts of the logical level (e.g. evaluation of HDLC commands and preparation of response packets) in the on-chip HDLC controller permits very high data rates of up to 4 Mbaud via the serial link to the central processor. By using a local standard microprocessor, such as the SAB 8051, it is possible to expand the range of the HDLC protocol to the full X.25 level, while still maintaining procedure handling, buffering and distribution of data packets hardwired in the PBC. Furthermore, the PBC is able, in conjunction with a microprocessor, to take over the "primary" function of a highspeed HDLC communication link.

The PBC communicates with the subscriber line devices via a three-wire Subscriber Line Data (SLD) bus based on a ping-pong type of protocol. The SLD bus ensures reduced line board wiring.

To cover a broad range of applications the PBC is adaptable to all standard commercial PCM systems (with 24, 32, 48, 64 channels per frame). Independently of the system clock used, the circuit computes all timing signals required for the standardized SLD bus, thus decoupling the subscriber line devices from the system clock. The PBC is an excellent example of the efficient realization of standard functions through the use of hardwired logic in order to increase real-time processing and speed without loss of flexibility.

A further device for interfacing subscriber line devices with PCM lines is the **P**CM **I**nterface **C**ontroller (PIC) PEB 2052. This CMOS device performs the **T**ime-**S**lot **A**ssignment (TSA) and the PCM interface functions. It is pin and software-compatible to the PBC PEB 2050, but leaves out the HDLC controller and the hardwired last look logic.

The **E**xtended **P**CM **I**nterface **C**ontroller (EPIC™) PEB 2055 is intended to be used as central PCM processor in new architectures. The CMOS device can be programmed to operate at different data rates between 128 and 8192 kbit/s the system interface consists of up to four duplex ports with a tristate indication signal for each output line. The configurable interface can be selected to incorporate either four duplex (IOM®) or eight bidirectional I/O ports (SLD).

The EPIC can therefore be programmed to communicate either with SLD or with IOM (ISDN Oriented Modular) and IOM-2-compatible devices. In both cases the device handles the layer-1 functions of buffering the C/I and monitor channels for IOM-compatible devices and the feature control and signaling channels for SLD compatible devices.

The EPIC can handle up to 32 ISDN subscribers with their 2B+D channel structure or 64 analog subscribers in IOM configuration or up to 16 subscribers in SLD configuration. Since its interfaces can operate at different data rates, the EPIC is an ideal device for data rate adaptation.

Moreover, the EPIC is one of the fundamental building blocks for networks with either central, decentral or mixed signaling and packet data handling architectures.

Siemens Components therefore offer the optimum solution of PCM Interface Controller for every application:

- **PCB 2050/51:** for up to eight ISDN and 16 analog subscribers.
  Especially suitable for powerful PABX.
- **PIC PEB 2052:** for up to eight ISDN and 16 analog subscribers.
  Ideal for price sensitive systems, e.g. small PAX and public exchanges (CO).
- **EPIC PEB 2055:** for up to 32 ISDN and 64 analog subscribers.
  Suitable as the central PCM processor in new architectures.

The second device used in the advantageous analog line board architecture is the highly sophisticated **Si**gnal Processing **Co**dec **F**ilter (SICOFI®) PEB 2060, fabricated in advanced CMOS technology. Based on Digital Signal Processing (DSP) methods, in addition to the standard functions of PCM coding and voice-band limitation that any codec filter features, the SICOFI provides a variety of user-programmable filters for impedance matching, 2/4-wire hybrid balancing, analog and digital gain adjustment as well as frequency response correction.

A sophisticated level of performance can therefore be achieved under complete software control. The use of external components or trimming procedures is completely avoided.

For impedance adjustments, the related filter implements a feedback loop to modify the SLIC's termination impedance. It can handle any complex impedance level, resulting in optimized return loss for all subscriber line conditions. In a similar manner, the hybrid balance filter can be programmed for optimal balance between the transmit and receive side and for minimum echoes.

For accurate adjustment of the gain in receive and transmit directions, four independently programmable filters can vary the level of the analog voice signal in a range of ± 22 dB.

Independently of the actual gain setting, the device still holds the specified transmission performance. Similar to the level control, the SICOFI contains digital filters in receive and transmit directions, which allow modification of the frequency response characteristics. Further features attractive for the realization of flexible exchange systems are selectable A/μ law coding, three-party conference support, supply voltage supervision, hardware and software reset, power-down mode and on-chip reference voltage. Different loopback modes enable both the line board and the total system to be tested during operation. The SICOFI can hook up directly to virtually any commercial SLIC, because of its flexible signaling interface consisting of ten ports. Three are dedicated to the status of voice transmissions and three to receptions. The remaining four can be programmed individually as either transmit or receive ports.

Due to the fact that the SIFOFI needs extended control information, a message-oriented protocol is used for byte transfer via the SLD bus. Two bits in each control byte are used to define three different classes of commands, which contain information about the configuration of the SICOFI, the coefficient exchange and the number of subsequently transmitted data bytes. Per frame and direction, one control byte is transferred between the SICOFI and the PBC. With the appropriate commands, data can be written into or read back from the SICOFI. Selection of one of the two SICOFIs connected to one SLD port is accomplished by an address bit in the feature control byte. For programming the device in the information usually is transferred via the HDLC link to the PBC, but all programming can also be done by means of an onboard microprocessor.

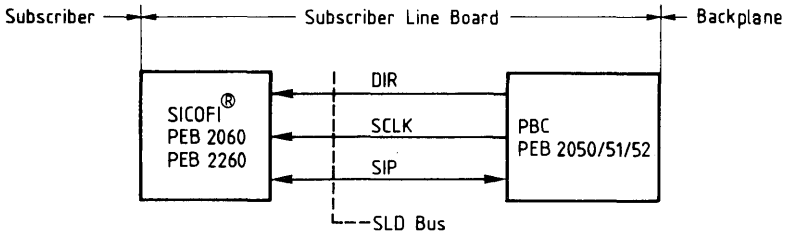
There are numerous good reasons why, the world over, major attention is given to digital signal processing methods. Compared to analog filtering, digital processing does not need precision elements, allows much higher accuracy along with precisely predictable transmission behavior including noise. It makes the device less sensitive to parameter fluctuations such as drift with temperature or aging, and, moreover, it provides excellent power supply rejection, better testability and crosstalk behavior of the circuit.

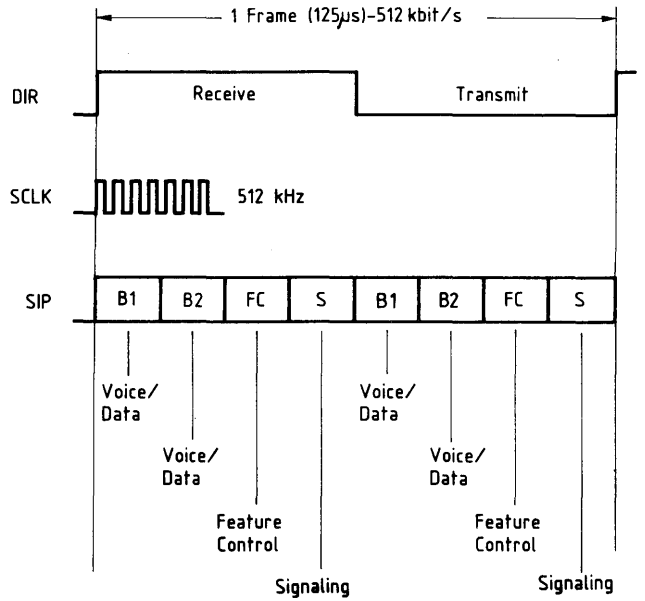
In addition, the DSP technique allows a better and easier shrinking of the device and the implementation of codec/filter functions for two and more subscribers on one chip, which is not economical or completely unpossible with switched capacitor methods. The next development stage will produced a Dual Channel Codec Filter (SICOFI-2) PEB 2260 that performs the functions of the SICOFI-1 PEB 2060 for two subscribers in one chip. Moreover the CMOS device can be programmed to communicate either with SLD (PBC/PIC) or with IOM-2 (EPIC) compatible PCM interface controller.

As shown with the SICOFI the DSP approach, in a costsaving and programmable manner, allows the realization of new functions which would be very expensive or impractical in the analog domain.

The all-over flexibility of the unique device concept gives the user the capability for designing a standard line card which can be customized for each application under software control. The SLD architecture leads to a highly modular line board configuration with low wiring, reduced board area and, depending only on the SLIC to be used, very few discrete elements. Moreover, since the peripheral board controller an the SLD bus concept are also key elements of Siemens IOM (ISDN Oriented Modular) VLSI family, a high degree of upward compatibility and modularity is achieved in fully digital voice and data communication systems.

Frame Structure of the SLD Bus

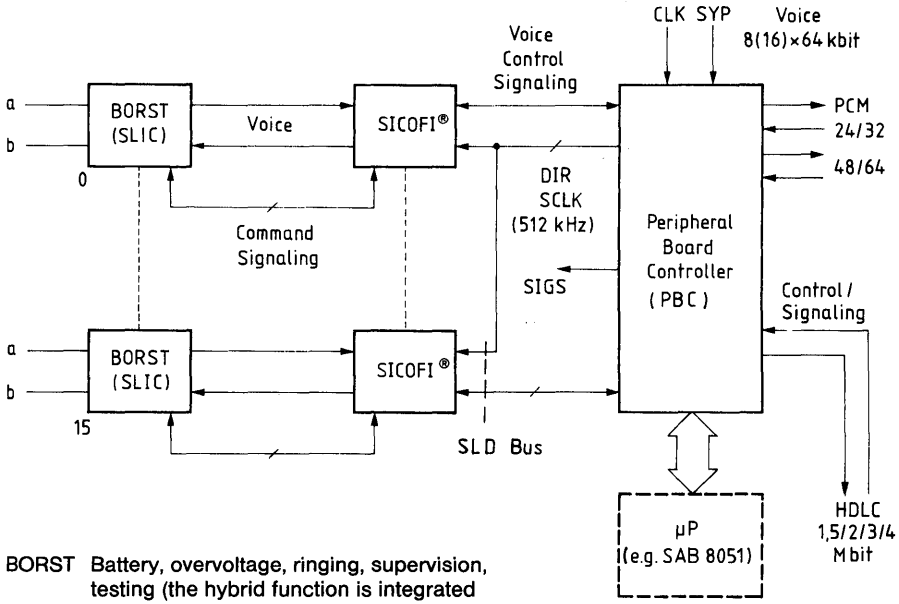




Advantages of Siemens Line Board Concept

- System specific PCM interface is represented by a simple general line board internal interface (SLD bus)
- Pin and hardware reduction for codec filter circuit
- Reduced line board wiring; per-line structure avoids cross-wiring
- Design of one standard line board which can be customized for each requirement through complete software control
- Decoupling of subscriber line devices from the system clock
- Transparency between control and PCM data
- SLD concept is upward-compatible with Siemens ISDN circuit family
- Multiple source for SLD circuits

Analog Subscriber Board for up to 16 Subscribers



BORST	Battery, overvoltage, ringing, supervision, testing (the hybrid function is integrated in the SICOFI)
CLK	Clock
DIR	Direction
SCLK	Slave clock
SICOFI	Signal-processing codec filter
SIGS	Signal strobe
SLIC	Subscriber line interface circuit
SYP	Synchronization

The SLD Interface

The SLD bus is used by the PBC to interface with the subscriber line devices. A **S**erial **I**nterface **P**ort (SIP) is used for the transfer of all digital voice and data, feature control and signaling information between the individual subscriber line devices, the PCM highways and the control backplane. The SLD approach provides a common interface for analog or digital per-line components. Through the PBC, which will be the key device in the SLD architecture, the PCM data is transparently switched onto the PCM highways. The PBC will make analog and digital subscriber line boards plug-compatible in a line equipment rack.

There are three leads connecting each subscriber line device and the PBC: two common clock signals shared among all devices, and a unique bidirectional data lead for each of the eight SIP lines. The **Dir**ection signal (DIR) is an 8-kHz clock output from the PBC (master) that serves as a frame sync to the subscriber line devices (slave) as well as a transfer indicator. The data are transferred at a 512-kHz rate, clocked by the **S**ubscriber **Clock** (SCLK). When DIR is high (first half of the SLD 125 µs frame), four bytes of digital

data are transmitted on the SLD bus from the PBC to the slave (receive direction). During the second half of the frame when DIR is low, four bytes of data are transferred from the slave back to the PBC (transmit direction).

Channel B1 and B2 are 64-kbit/s channels reserved for voice or data to be routed to and from the PCM highways. In an application where one SICOFI is connected to a SIP, voice is received on channel B1 and transmitted on channel B1 and B2. For a three-party conference, channel B2 is the third-party voice channel. If two SICOFIs are connected to one SIP, channel B1 is assigned to one and channel B2 to the other SICOFI. Conferencing is not possible in this configuration. With digital subscriber line devices the two bytes can be used to carry 64-kbit/s data channels. The third and sixth byte locations are used to transmit and receive control information for programming the slave devices The last byte in each direction is reserved for signaling data.

Switching Network

Supervision and control of the entire system, including connection setup, maintenance and testing, is performed in a powerful central processing unit. Besides this, the through-switching of PCM channels is done in a switching network unit, whereas the tasks of a frame alignment unit are to interface PCM transmission routes with the switching system.

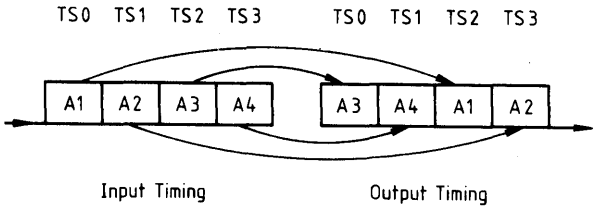
Digital exchanges put calls through by newly arranging the speech signals coded with 8-bit words (PCM slots). The code words are transmitted serially on PCM lines. The sampling frequency of 8 kHz produces PCM frames with a duration of 125 µs. The transmission rate on the line determines how many code words (speech channels) can be accommodated within a sampling period. With a data rate of 2048 kbit/s for example, there are 32 time slots of 8 bits each. Four lines with a data rate of 8192 kbit/s have a transmission capacity of 512 channels.

In a digital switching matrix one distinguishes betwen two basic switching principles:

- time division multiplex
- space division multiplex

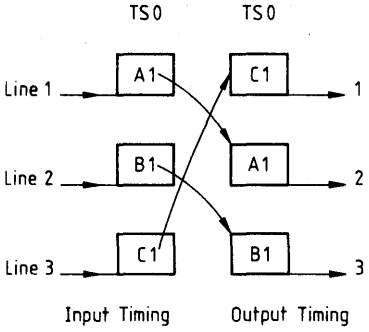
A method that is frequently used involves a combination of the two principles, this being called space/time division multiplex. The figure illustrates the different principles.

Time/Division Multiplex



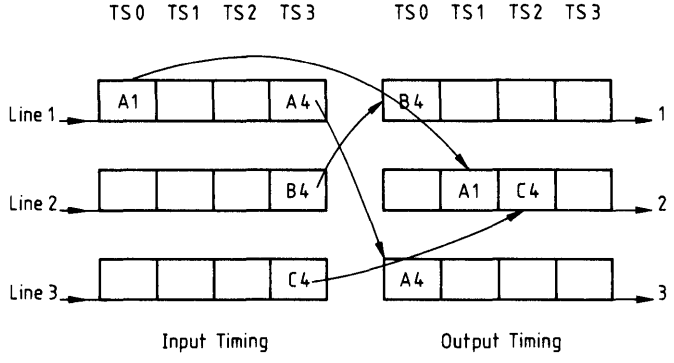
Characteristic: the timing of the code words is changed

Space/Division Multiplex



Characteristic: the code words retain their timing,
but the lines are changed

Space/Time-Division Multiplex



In time division multiplex only the time slot is altered during switching. All signals from a certain input PCM line are switched to a fixed output line, only the time-slot sequence may change.

In space division multiplex incoming PCM data are only rearranged in space. The input time slot equals the output time slot. However, input from one PCM line can be switched to different output lines.

Siemens Components Group offers devices which take into consideration the needs for efficient realization of these tasks. One of the switching network circuits offered is the **M**emory **T**ime **S**witch in **C**MOS (MTSC) PEB 2045, which has the ability to connect any of 512 incoming PCM channels to any of 256 outgoing PCM channels on a single chip. A non-blocking switch for 512 subscribers can be built up with two devices only. A further expansion can be realized very easily too. Different kinds of operation modes enable the use of the MTSC PEB 2045 in 2.048 Mbit/s, 4.096 Mbit/s and 8.192 Mbit/s or mixed PCM systems.

As an additional feature the MTSC PEB 2045 together with an **A**dvanced **C**MOS **F**rame **A**ligner (ACFA) PEB 2035 can realize the system interface of up to four primary multiplex access lines.

The **M**emory **T**ime **S**witch **S**mall (MTSS) PEB 2046 is a smaller version of the MTSC PEB 2045 performing time/space switch functions for a non-blocking switch of 256 subscribers.

Primary Access Applications

Applications for the primary rate interface include trunk lines between public central office (CO) exchanges, from a PBX to a CO, interlinking PBXs, the gateway connecting a LAN to the public network or a PBX, interlinking LANs, interfacing a large computer or data intensive terminal (e.g. CAD graphics) with CO or a PBX, etc.

To facilitate the design of equipment for these applications, Siemens has developed an architecture which optimizes the required functions on the following four integrated circuits:

PEB 2235	ISDN Primary Access Transceiver (IPAT™)
PEB 2035	Advanced CMOS Frame Aligner (ACFA)
PEB 2045	Memory Time Switch CMOS (MTSC)
SAB 82520/SAB 82525	High-level Serial Communications Controller (HSCC/HSCX)

The functional architecture for the primary access chip set is shown on page 42.

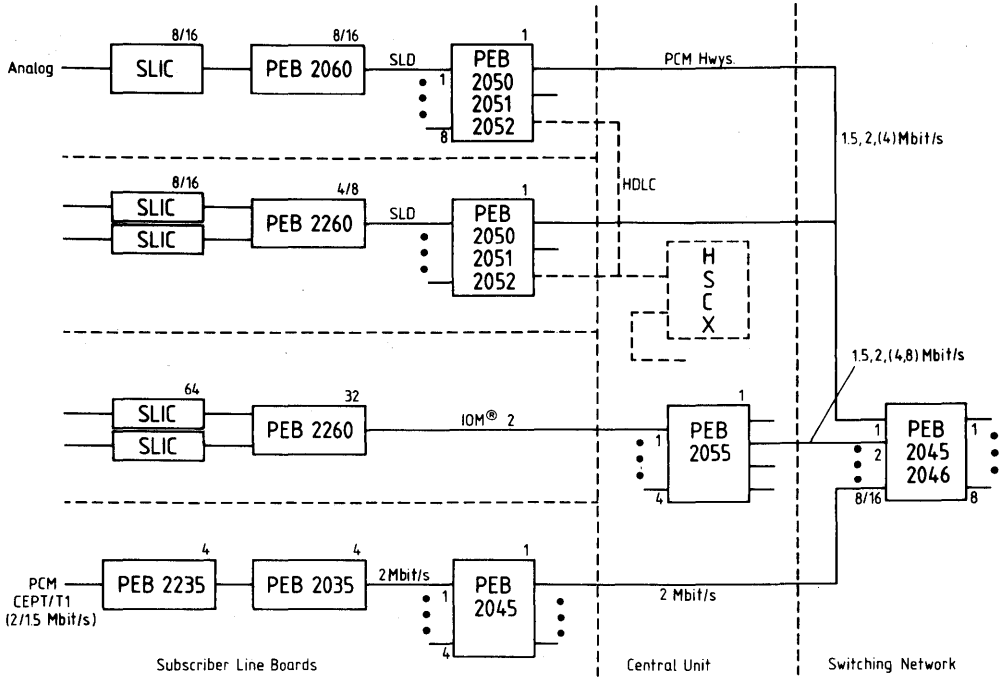
The IPAT, together with the ACFA, implement the layer-1 physical interface. They are connected to the other primary access devices over the internal primary highway. The HSCC/HSCX is a powerful communications controller which handles protocol oriented signaling (X.25 LAPB, ISDN LAPD) by accessing the signaling channel on the internal primary highway. The MTSC is an equally powerful switching device which connects the internal primary highway to a variety of possible system interfaces (2048, 4096, 8192 kbit/s. All of these devices can be readily accessed and controlled via the microprocessor interface.

The IPAT is a monolithic line driver for primary access lines of either the PCM 24 (T1, N. America/Japan) or PCM 30 (CEPT, W. Europe) standards. In the receive direction, the device recovers the clock and data signals from the line and forwards them to the ACFA.

The IPAT is transparent to the received line code. In the transmit direction, the device takes the signal received from the ACFA and forms it into transmission pulses according to CCITT recommendations for the PCM 30 or AT&T's DMI specifications for PCM 24.

Correspondingly, input/output jitter requirements comply with both CCITT and AT&T specifications.

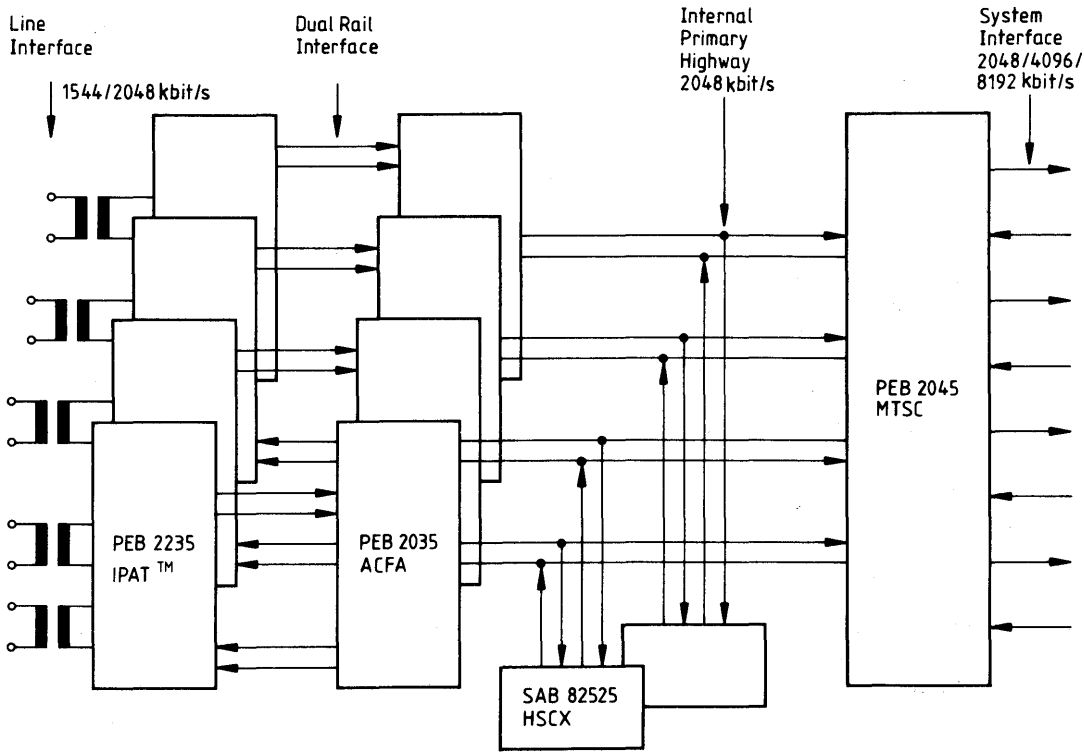
Basic Connections in a Digital Switching System



Frame alignment for all commonly used framing and multiframing formats is performed by the ACFA. The device synchronizes the transmit and receive signals, interfaces the data rate from the line to the 2048 kbit/s internal highway and codes/decodes one of three selectable line codes.

For PCM 24, this transmission code can be either B8ZS or AMI-ZCS whereas for PCM 30, it is always HDB3. Alarms and error conditions are reported to the microprocessor via a maskable interrupt line. The ACFA can also be used for various signaling schemes. Rather than using the HSCC/HSCX, signaling information can be handled by a less intelligent communications controller without programmable time-slot access. For such devices, the ACFA provides the required signaling information via special purpose pins. Additionally, the ACFA has a DMA interface for transferring signaling information to/from a microprocessor controlled memory. Finally, signaling data can be accessed directly via the microprocessor interface.

A Quad Primary Access Interface and Switch realized with 11 CMOS Devices.



Advanced CMOS Frame Aligner (ACFA) PEB 2035

Preliminary Data **CMOS IC**

Type	Ordering Code	Package
PEB 2035-C	Q67100-H8358	C-DIP 40
PEB 2035-N	Q67100-H8684	PL-CC 44
PEB 2035-P	Q67100-H8359	P-DIP 40

Introduction (PEB 2035; Version A)

The Advanced CMOS Frame Aligner PEB 2035 (ACFA) is a monolithic CMOS device which implements the interface to primary rate PCM carriers. It may be programmed to operate in 24-channel (T1) and 32-channel (CEPT) carrier systems.

The ACFA features include: selectable multiframe (six multiframe formats), error checking (CRC4, CRC6), multiple line codes (HDB3, B8ZS, AMI), and programmable signaling paths. The device meets the newest CCITT recommendations for primary rate interfaces and the AT&T Digital Multiplexed Interface specifications (DMI). Controlling and monitoring of the device is performed via a parallel eight-bit microprocessor bus.

The circuit contains a two-frame elastic memory which ensures wander absorption between the PCM carrier and a synchronous, system internal highway.

All signaling types – CCS, CAS and bit-robbed signaling – are supported by the ACFA. In addition, the ACFA allows flexible access to facility data link and service channels. Extensive testing capabilities are included.

The ACFA is suitable for use in a wide range of voice and data applications such as the connection of digital switches and PABX's to host computers (S1/S2 interfaces), the implementation of primary ISDN subscriber loops, and the connection to primary rate fibre optical transmission systems.

The ACFA is available in either 40 pin DIP or 44 pin PL-CC packages. As with all of the ISDN circuits from Siemens, the ACFA has been implemented in advanced CMOS technology. Total power consumption is less than 100 mW.

Features

Serial Interface to Line Interface Unit

- Frame alignment/synthesis for 2048 kbit/s (CEPT, PCM 30) and 1544 kbit/s (T1, PCM 24) PCM
- Meets newest CCITT Rec's (G703, 704, 732, 733, Nov. 1984) and AT&T technical advisories (DMI, April 1985)
- Programmable formats for: PCM 30: Doubleframe, CRC Multiframe
  PCM 24: 4-Frame Multiframe (F4), 12-Frame Multiframe (F12, D3/4), Extended Superframe (ESF), Remote Switch Mode (F72)
- Selectable line codes (HDB3, B8ZS, AMI with ZCS)
- Unipolar NRZ for interfacing fibre optical transmission routes
- Error checking via CRC4 or CRC6 procedures
- Insertion and extraction of alarms and facility signaling

Serial Interface to System Internal Highway

- System clock frequency of either 4096 kHz or 8192 kHz
- Selectable 2048/4096 kbit/s system internal highway with programmable receive/transmit shifts
- Two-frame deep elastic receive memory for receive route clock wander and jitter compensation
- One frame elastic transmit memory (PCM 24 mode only) for transmit route clock wander and jitter compensation
- Two different time-slot assignment procedures in PCM 24 mode
- Support for different signaling schemes
- Channel loop back capabilities
- Channel parity error monitoring

Microprocessor Interface

- Parallel, demultiplexed microprocessor interface for random access to control and status registers
- Alarm interrupt capabilities
- Access to different signaling information:
  -Sn, Si-bits (register)
  -SN-bits (5 byte stack)
  -FDL bits with the possibility of mixed insertion
  -CCS, CAS-CC (common channel), CAS-BR (bit robbing) via 2/3 byte stacks with DMA/interrupt support
- Extensive test and diagnostic capabilities

General

- Advanced CMOS technology
- Low power consumption (< 100 mW)
- Packaging: 40-pin DIP/DIC, 44-pin PL-CC

Important Remarks

If it is planned to use future design versions of the ACFA (e.g. ACFA- VB1) which will meet newest CCITT recommendations and actual requirements of the market, SOFTWARE development should take into account that

- **unused control bits** have to be programmed with a **logical '0',** although they are set to logical '1' when reading the assignend registers,
- future design versions will have **more status bits** than now,
- future design versions **will no longer** support the **HDB3 Full Error Detection** mode.

Introduction; (PEB 2035; Version B)

In addition to the features of PEB 2035 (ACFA) version A, the version B includes functions which meet the newest CCITT and FTZ recommendations plus some additional features requested by the market.

The most important new functions are the clear channel capability (PCM 24) and the extented support of the synchronization algorithm recommended by FTZ (PCM 30, Deutsche Bundespost).

There are no differences in packaging, pin functions or hardware interfaces between the ACFA's version A and version B.

General

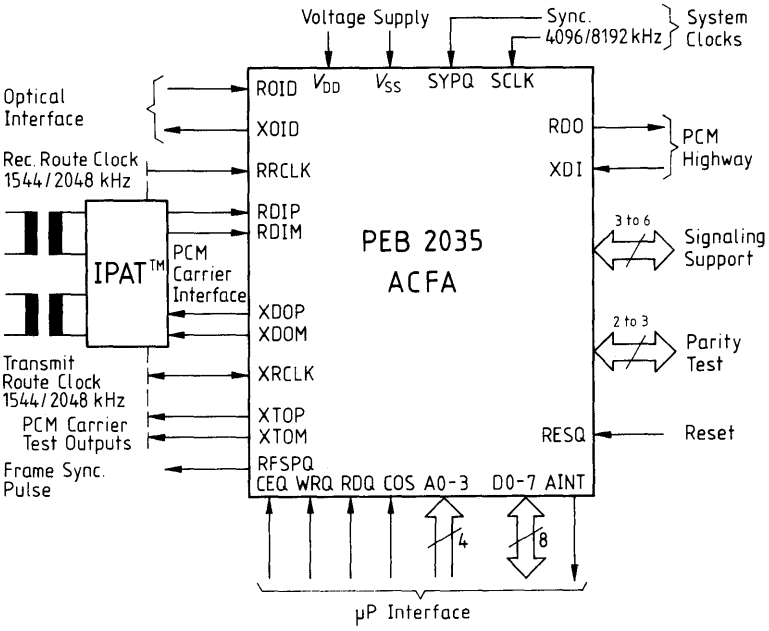
Additions to PCM 30 Mode

- Slip direction indication [RSR.SDI].
- Extended HDB3 error detection ['0000' string detection, CCR.EXTD]. HDB3 full detection mode no longer supported.
- Indication of a CRC error in received submultiframes [SEI.SI1, SEI.SI2] and selectable automatic insertion in Si bit position of outgoing CRC multiframe [XSP.AXS].
- Multiframe synchronous updating of Si bit information.
- Additional alarm interrupt sources for start of transmit and receive CRC multiframes [XSP.MXMB,XSP.MRMB] in conjunction with auto-reset multiframe status flags enable multiframe synchronous access to Si and Sn bit information.
- Extension of CRC error counting (switchable 10-bit counter) simplifies CRC error limit detection [CECX,CE8,CECX.CE9,RC0.ECE].
- Two transparent modes for time-slot 0 in transmit direction [XSP.TT0,XSP.TT0S] extend test capabilities and access to Sn and Si bit information via the system interface.
- Improved sychronization procedures.
- Single frame mode [LOOP.SFM] of receive speech memory for short data delays in master/slave applications.
- Error on receive line [ARS.ERL] flags that signals at line inputs RDIP,RDIM) are both active. This alarm may occur if line interface unit (e.g. PEB 2235, IPAT) detects bad signal levels on receive line.
- Repeated transmission of the signaling information (last byte of XSIG, transmit signaling stack) simplifies realization of HDLC procedures via board processor.

Additions to PCM 24 Mode

- Clear channel capabilities for applications in mixed voice/data or data-only environments, especially when using bit robbing signaling schemes and pure AMI line coding with zero code suppression (B7 stuffing). Selection of 'clear' channels is done by programming three byte register bank CCB1... CCB3 [enabled by CPY.SWTCH].
- Extension of CRC error counting (switchable 10-bit counter) simplifies CRC error limit detection [CECX,CE8, CECX.CE9, RC0.ECE].
- Error on receive line [ARS.ERL] flags that signals at line inputs RDIP, RDIM are both active. This alarm may occur if line interface unit (e.g. PEB 2235, IPAT) detects bad signal levels on receive line.
- Repeated transmission of the last signaling information (last byte of XSIG, transmit signaling stack) simplifies realization of HDLC procedures via board processor.

Logic Symbol



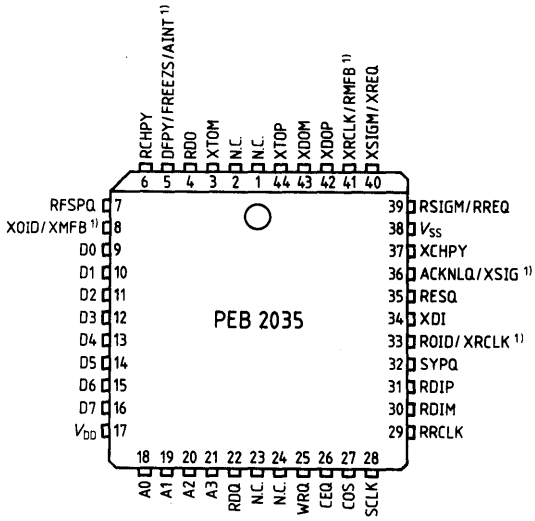
ISDN Primary Access Transceiver (IPAT) PEB 2235 for receive line clock recovery, TTL/line voltage translation and pulse shaping.

Note: Some pins have mode dependent functions and thus may appear more than once in the logic symbol.

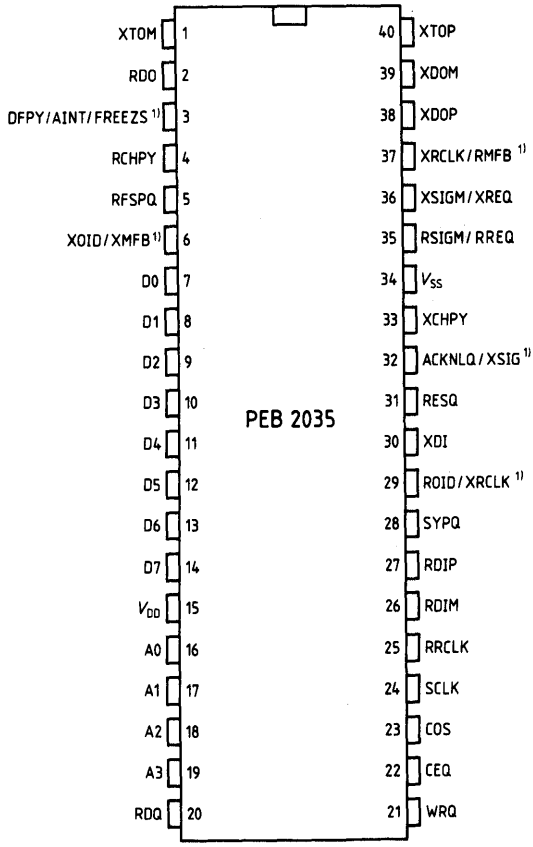
Pin Configurations

(top view)

PL-CC-44



P-DIP-40



1) The function of the pin is mode dependent (2048/1544 kbit/s PCM)

Pin Definitions and Functions

PL-CC Pin No.	P-DIP Pin No.	Symbol	Input (I) Output (O)	Function
44 3	40 1	XTOP XTOM	O	**Transmit Text Data OUT Plus** **Transmit Test Data OUT Minus** **PCM** (+) and **PCM** (−) output signals which may be used for diagnostic loopback. Data will continue to be transmitted during AIS transmission at XDOP/XDOM. The line code is determined by the bits MODE.PMOD and MODE.CODE. Output sense is selected via bit XC0.XTDS (after RESET: active low). Timing specifications are equivalent to XDOP/XDOM.
4	2	RDO	O	**Receive Data OUT** Received data which is sent to the system internal highway with 4096 kbit/s or 2048 kbit/s (bit MODE.IMOD). Data is clocked with the falling edge of SCLK. The delay between the beginning of time-slot 0 and the initial edge of SCLK (after SYPQ goes active) is determined by the values of Receive Time-slot Offset RC1.TRO and Receive Clock Offset RC0.RCO. Additionally for PCM 24, the time-slot assignment between route and system side is selected via bit MODE.CTM.
5	3	DFPY FREEZS AINT	O	**PCM 30: Doubleframe Parity** Every parity signal which supplements the number of ones of a received doubleframe to an even quantity. The parity signal is sent out during the following doubleframe (data changes four SCLK cycles before the next doubleframe begins). **PCM 24: Freeze Signaling** Synchronization status signal which informs the signaling processor that current signaling should be frozen. This signal goes actife if – one or more framing bit errors are found in a superframe, – loss or receiver synchronization, or – a receipe slip is detected It is cleared after an error-free superframe. FREEZS will be inhibited by setting bit RC0. DFRZ. During alarm simulation, this signal goes active during simulation steps 2 and 6 if not disabled via RCO.DFRZ.

Pin Definitions and Functions (cont'd)

PL-CC Pin No.	P-DIP Pin No.	Symbol	Input (I) Output (O)	Function
5	3	AINT	O	**Alarm Interrupt** Setting bit CCR.AINT switches the output to the Alarm Interrupt function. It is triggered by any of the alarm sources which are enabled via register MASK. Acknowledging is done by writing a "1" to bit LOOP.AIA.
6	4	RCHPY	O	**Receive Channel Parity** Even/Odd parity signal which supplements the number of ones of a received channel to an even/odd quantity while sending channel data to output RDO. The parity type is programmed by bit RC0.RPYS.
7	5	RFSPQ	O	**Receive Frame Synchronous Pulse** (Active Low) Framing pulse derived from the received PCM route signal. During loss of synchronization (bit RSR.LOS), this pulse is suppressed (not influenced during alarm simulation). Pulse Frequency: 8 kHz Pulse Width: 488 ns [PCM 30] 648 ns [PCM 24]
8	6	XOID/ XMFB	O	**PCM 30: Transmit Optical Interface Data** Unipolar NRZ data sent to fiber optical interface with 2048 kbit/s. The output sense is programmed via bit XC0.XDOS. Data is clocked with the rising edge of XRCLK. **PCM 24: Transmit Multiframe Begin** Marks the beginning of every transmitted superframe (used for synchronizing). Additional pulses are provided which mark – frame 13 of the ESF-format to allow access to the data link channel. The flag MRF.XMB marks the multiframe begin. – every 12 frames when using the F72 format. The additional status flag MFR.XRS marks the beginning of the DL-channel. The pulses which are normally two frames long may be reset by writing a "1" to the acknowledge bit XFDL.XMAK.

Pin Definitions and Functions (cont'd)

PL-CC Pin No.	P-DIP Pin No.	Symbol	Input (I) Output (O)	Function Bus
9 10 11 12 13 14 15 16	7 8 9 10 11 12 13 14	D0 D1 D2 D3 D4 D5 D6 D7	I/O	**Data Bus** 8-bit bi-directional tristate data lines which interface with the system's data bus. These lines carry data and control/status information to and from the ACFA.
17	15	V_{DD}	I	**Power** +5 V Power Supply
18 19 20 21	16 17 18 19	A0 A1 A2 A3	I	**Address Bus** These inputs interface with four lines of the system's address bus to select one of the internal registers. Write access to address "0E" and "0F" is not allowed.
22		RDQ	I	**Read Enable** (Active Low) This signal indicates a read operation. If both CEQ and RDQ are active, status information of the registers selected via A0-A3 will be read from the ACFA. If access to the internal signaling stacks is enabled by setting bit XC0.ISIG, the data from the stack: RSIG may be read when ACKNLQ and RDQ are active.
25	21	WRQ	I	**Write Enable** (Active Low) This signal indicates a write operation. If both CEQ and WRQ are active control information may be written to the registers selected via A0-A3. If access to the internal signaling stacks is enabled by setting bit XC0.ISIG data may be written to the stack XSIG when ACKNLQ and WRQ are active.
26	22	CEQ	I	**Chip Enable** (Active Low) A low signal enables normal read/write access to the internal registers.
27	23	COS	I	**Carrier OUT of Service** A high signal at this input enables transmission of AIS via outputs XDOP, XDOM, and XOID without any framing structure.

Pin Definitions and Functions (cont'd)

PL-CC Pin No.	P-DIP Pin No.	Symbol	Input (I) Output (O)	Function
28	24	SCLK	I	**System Clock** Working clock for the ACFA with a frequency of 4096 kHz or 8192 kHz (selected by bit MODE.SCLK)
29	25	RRCLK	I	**Receive Route Clock** Extracted from the incoming data pulses by the line interface unit (e.g., IPAT, PEB 2235). Clock Frequency: 2048 kHz [PCM 30] 1544 kHz [PCM 24]
30 31	26 27	RDIM RDIP	I	**Receive Data in Minus** **Receive Data in Plus** Inputs for received dual rail PCM (+) and PCM (–) route signals which will be latched on negative transitions of RRCLK. Input sense is selected by bit RC0.RDIS (after RESET: active low). Signal decoding depends on the PCM mode selected via bit MODE.PMOD: – PCM 30: HDB3 line code with 2048 kbit/s – PCM 24: If optical interface mode is disabled the selected line code with 1544 kbit/s depends on bit MODE.CODE (B8ZS or AMI with B7 stuffing). After enabling optical interface mode via bit MODE.OPT port RDIP will be switched to input for single rail unipolar data. In this case, port RDIM has no function.
32	28	SYPQ	I	**Synchronous Pulse** Defines the beginning of time-slot 0 at system highway ports RDO, and XDI in conjunction with the values of registers RC0.RCO, RC1.RTO, CX0.CXO, and XC1.XTO. Pulse Cycle: Integer multiple of 125 µs.
33	29	ROID	I	**PCM 30: Receive Optical Interface Data** Unipolar data received from fiber optical interface with 2048 kbit/s. The input sense is programmed via bit RC0.RDIS. Data is clocked on the falling edge of RRCLK if optical interface mode is enabled via bit MODE.OPT.

Pin Definitions and Functions (cont'd)

PL-CC Pin No.	P-DIP Pin No.	Symbol	Input (I) Output (O)	Function
33	29	XRCLK	I	**PCM 24: Transmit Route Clock** Input for 1544 kHz transmit route clock provided from an external clock generator. To avoid transmit slips it must be phase locked to a common submultiple of the system clock SCLK such as 8 kHz. In case of an error condition reported via bit ASR.XSLP the transmit time-slot counter has to be set to its initial start position by programming its offset value XC1.XTO.
34	30	XDI	I	**Transmit Data IN** Transmit data received from the system internal highway with 4096 kbit/s or 2048 kbit/s (bit MODE.IMOD). Data is clocked on the falling edge of SCLK. The delay between the beginning of time slot 0 and the initial edge of SCLK (after SYPQ goes active) is determined by the values of Transmit Time-Slot Offset XC1.XTO and Transmit Clock-Slot Offset XC0.XCO. Additionally, for PCM 24 the channel/time slot correspondence between route and system side ist selected via bit MODE.CTM.
35	31	RESQ	I	**RESET** (Active Low) A low signal will initialize all internal flipflops. The ACFA is switched to PCM 30 mode. All output stages are tristated while RESQ is active.
36	32	ACKNLQ	I	**DMA Acknowledge** (Active Low) If access to internal signaling stacks is enabled via bit XCO.ISIG this input acts as an "access enable" to the internal stacks RSIG and XSIG in conjunction with a read/write command without the need of generating the chip enable signal CEQ. In this case is should be connected to the acknowledge output of the DMA controller to enable I/O-to-memory transfers. **PCM 30** No function if XCO.ISIG is set to "0". In that case this input has to be fixed either to V_{DD} or to V_{SS}.

Pin Definitions and Functions (cont'd)

PL-CC Pin No.	P-DIP Pin No.	Symbol	Input (I) Output (O)	Function
36	32	XSIG	I	**PCM 24: Transmit Signaling Data** If XCO.ISIG is set to "0" the external signaling mode is enabled. This port acts as input for the signaling data requested by the marker XSIGM. Data is clocked on the falling edge of SCLK. If not used port XSIG should be tied to port XDI.
37	33	XCHPY	I	**Transmit Channel Parity** Externally generated even/odd parity signal which supplements the number of ones of each transmit channel on XDI to an even/odd quantity. Latching of data on XCHPY is coincident with latching of the LSB (bit 8) of the corresponding time slot if the external transmit channel parity mode is enabled via bit XCO.EPY. The parity type is programmed by bit XC0.EPYS. **NOTE:** To avoid difficulties for external parity generation the parity signal related to channels with signaling information is adjusted internally.
38	34	V_{SS}	I	**GND** (0 V)
39	35	RSIGM	O	**Receive Signaling Marker** – **PCM 30:** Marks time slot 16 of every received frame at pin RDO. – **PCM 24:** When using CCS or CAS-CC signaling schemes (bit MODE.SIGM = 0) RSIGM marks a) time slot 31 (speech channel 24) in channel translation mode 0 (bit MODE.CTM = 0) b) time slot 23 (speech channel 24) in channel translation mode 1. Setting bit FMR.SM24 shifts the marker to time slot 16 (speech channel 17). When using the CAS-BR signaling scheme, every six frames the robbed bit of each channel is marked.

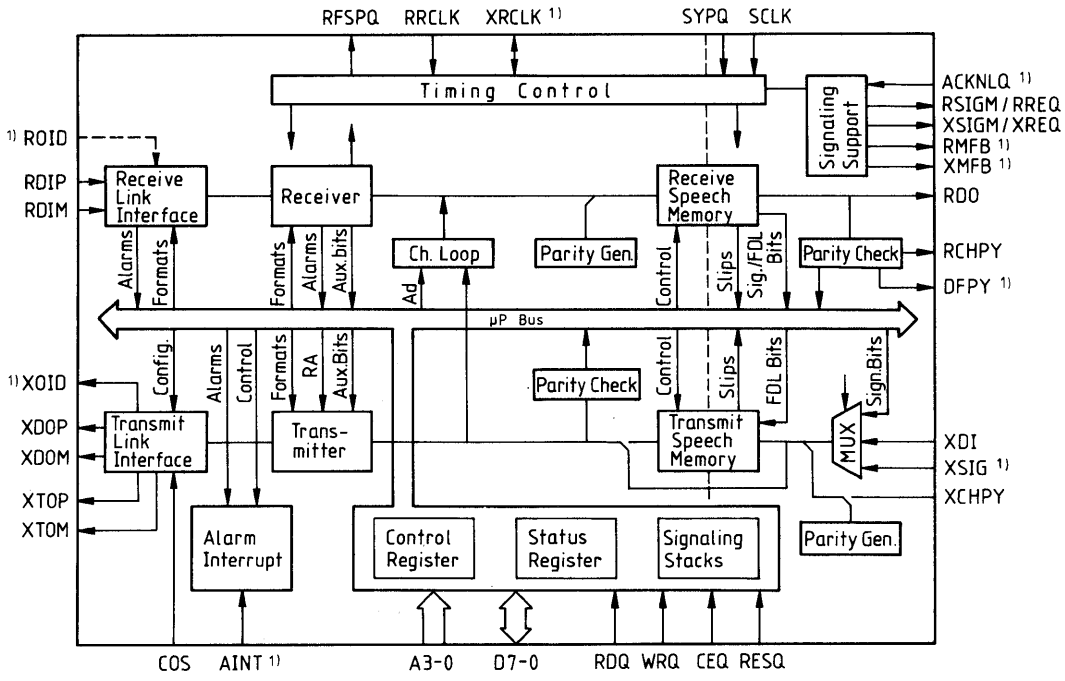
Pin Definitions and Functions (cont'd)

PL-CC Pin No.	P-DIP Pin No.	Symbol	Input (I) Output (O)	Function
39	35	RREQ	O	**Receive Request** If access to the internal signaling stacks RSIG and XSIG is enabled via bit XC0.ISIG, this pin acts as a DMA or interrupt request. It requires the controller to read the stack RSIG. RREQ will be held active until the first read access to RSIG is finished. It will be generated – **PCM 30:** once a double frame – **PCM 24:** every three frames in CCS/CAS-CC mode, or once a signaling frame (every six frames) at CAS-BR mode. The output will be cleared with the first read access to RSIG.
40	36	XSIGM/ XREQ	O	**Transmit Signaling Marker** Its function is equivalent to RSIGM for the data stream at ports XDI and XSIG (XSIG: PCM 24 mode only). **Transmit request** Its function is equivalent to RREQ for writing data to the stack XSIG.
41	37	XRCLK/ RMFB	O	**PCM 30: Transmit Route Clock** 2048 kHz clock derived from the internal clock of 4086 kHz. **PCM 24: Receive Multiframe Begin** Marks the beginning of every received superframe (used for synchronizing). Additional pulses are provided which mark – frame 13 of the ESF format to allow access to the data link channel. The flag MFR.RMB marks the multiframe begin. – every 12 frames when the F72 format is used. The additional status flag MFR.RRS signals that the first six bits of the DL-channel have been received (RMFB goes active with the beginning of frame 37 of the F72 multiframe). The pulses which normally are two frames long may be reset by writing a "1" to the acknowledge bit XFDL.RMAK.

Pin Definitions and Functions (cont'd)

PL-CC Pin No.	P-DIP Pin No.	Symbol	Input (I) Output (O)	Function
42	38	XDOP	O	**Transmit Data OUT Plus**
43	39	XDOM		**Transmit Data OUT Minus** Outputs for transmitted dual rail PCM (+) and PCM (−) route signals which will be clocked on rising edge of XRCLK. Output sense is selected by bit XC0.XDOS (after RESET: active low). Signal encoding depends on the selected PCM mode (MODE.PMOD): – **PCM 30:** HDB3 line code with 2048 kbit/s – **PCM 24:** If optical interface mode is disabled the selected line code with 1544 kbit/s depends on programming bit MODE.CODE (B8ZS or AMI with B7 stuffing). After enabling optical interface mode via bit MODE.OPT port XDOP will be switched to output single rail unipolar data with 100% duty cycle.

Block Diagram



The ACFA comprises complete paths for receive and transmit direction for connecting the primary access line interface unit to the system internal PCM highway:

The receive/transmit link interface with encoder/decoder and alarm detectors connects the ACFA to the line interface unit (e.g. IPAT, PEB 2235).

The receiver/transmitter perform frame alignment/synthesis, CRC checking/generation, alarm and signaling extraction/insertion.

The receive/transmit speech memory compensates the wander and jitter of the assigned route clock. Time-slot assigment to the system internal highway is also handled via this memory.

The parallel microprocessor interface can be used for controlling and monitoring of all functions and alarms as well as extraction and insertion of signaling data. Additionally, a Direct Memory Access (DMA) interface and bundel of specific signals enable powerfull support for a varity of possible external signaling controllers.

Functional Description

General Functions and Device Architecture

1 Receive Path

Receive Link Interface

For data input, two different data types with selectable input sense are supported:

- Dual rail data (PCM[+], PCM[–]) at ports RDIP, RDIM received from a line interface unit (e.g. PEB 2235, Siemens ISDN Primary Access Transceiver, IPAT)
- Unipolar data at port ROID (PCM 30) or at port RDIP (PCM 24) received from a fibre optical interface.

Latching of data is done using the falling edges of the Receive Route Clock (RRCLK, 2048 kHz or 1544 kHz) recovered from the PCM receive data stream. Dual rail data is subsequently converted into a single rail, unipolar bit stream. In PCM 30 mode, the HDB3 line code is used along with double violation detection or full code violation detection (selectable). In PCM 24 mode, a selection between B8ZS or simple AMI (ZCS) coding is provided. In this case, all code violations that do not correspond to zero substitution rules will be detected.

These errors increment the code violation counter.

When using the unipolar input mode, the decoder is by-passed and no code violations will be detected.

Additionally, the receive link interface comprises the alarm detection for AIS (Alarm Indication Signal: unframed bit stream with constant logical 'one') and NOS (no signal: input signal with an insufficient bit rate or an insufficient density of ones).

The single rail bit stream is then processed by the receiver.

Receiver

For both the PCM 30 mode and the PCM 24 mode the following functions are performed:

- Synchronization on pulse frame
- Synchronization on multiframe
- Error indication when synchronization is lost. In this case, AIS is sent to the system side.
- Initiating and controlling of resynchronization after reaching the asynchronous state. This may be automatically done by the ACFA, or user controlled via the microprocessor interface.
- Detection of remote alarm indication from the incoming data stream.
- Separation of service bits and data link bits. This information is stored in special status registers.
- Generation of control signals to synchronize the CRC checker, the parity generator, and the receive speech memory write control unit.

If programmed and applicable to the selected multiframe format, CRC checking of the incoming data stream is done by generating check bits for a CRC submultiframe (or ESF multiframe) according to either the CRC 4 procedure (PCM 30, refer to CCITT Rec. G704 § 2.3.3) or the CRC 6 procedure (PCM 24, refer to CCITT Rec. G704 § 3.1.1.3). These bits are compared with those check bits that are received during the next CRC (sub-)multiframe. If there is at least one mismatch, the CRC error counter will be incremented.

Receive Speech Memory

The speech memory is organized as a two-frame elastic buffer with a size of 64 x 9 bit or 48 x 9 bit for PCM 30 or PCM 24, respectively (8-bit channel data plus one parity bit).

The functions are:

- Clock adaption between system clock (SCLK) and route clock (RRCLK).
- Compensation of input wander and jitter. Maximum of wander amplitude:
  PCM 30: 95 UI (1 UI = 488 ns)
  PCM 24: 63 UI in channel translation mode 0
  39 UI in channel translation mode 1
  (1 UI = 644 ns)
- Frame alignment between system frame and receive route frame
- Reporting and controlling of slips

Controlled by special signals generated by the receiver, the unipolar bit stream is converted into bit-parallel, channel-serial data which is circularly written to the speech memory using the receive route clock (RRCLK). At the same time, a parity signal is generated over each channel and also stored in the speech memory.

Reading of stored data is controlled by the system clock (SCLK) and the synchronous pulse (SYPQ) in conjunction with the programmed offset values for the receive time-slot/clock-slot counters. After conversion into a serial data stream and parity checking (errors are reported via the status registers), the data is given out via port RDO. Channel parity information is output at port RCHPY with selectable output sense. In PCM 24 mode, two channel translation modes are provided (refer to § 2.3.4). Unequipped time-slots will be set to 'FF' hex. For both PCM modes, two bit rates (2048/4096 kbit/s) are selectable via the microprocessor interface.

A slip condition is detected when the write address pointer and the read address pointer of the speech memory are nearly coincident. In this case, a negative slip (the next received frame is skipped) or a positive slip (the previous received frame is read out twice) is performed, depending on the difference between RRCLK and SCLK.

2 Transmit Path

The inverse functions are performed for the transmit direction.

The PCM data is received from the system internal highway at port XDI with 2048 kbit/s or 4096 kbit/s. The channel assignment is equivalent to the receive direction. All unequipped time-slots will be ignored. Latching of data is controlled by the system clock (SCLK) and the synchronous pulse (SYPQ) in conjunction with the programmed offset values for the transmit time slot/clock-slot counters.

Transmit Speech Memory

The transmit speech memory is operational only in the PCM 24 mode. This one-frame elastic buffer with a size of 24 x 9 bit (8-bit channel data plus 1 parity bit) serves as a temporary store for the PCM data to adapt the system clock (SCLK) to the externally generated transmit route clock (XRCLK), and to re-translate channel structure used in the system to that of the line side. Its optimal start position is initiated when programming the above offset values. Normally, XRCLK has to be phase locked to a common submultiple of SCLK such as 8 kHz. A difference in the effective data rates of system side and

transmit side may lead to an overflow/underflow of the transmit speech memory: thus, errors in data transmission to the remote end may occur. This error condition (transmit slip) is reported to the microprocessor via the status registers. It signals that the external clock generation is defective.

Maximum wander amplitude in PCM 24 mode:

- Channel translation mode 0: 29 UI
- Channel translation mode 1: 23 UI

  (1 UI = 644 ns)

Because this is, under normal circumstances, a rare error condition no automatic action is taken by the transmit speech memory as opposed to the receive speech memory in the case of a positive or negative slip. In this case the ACFA requires a re-initialization of the transmit memory by re-programming of the transmit time-slot counter. After that, this memory has its optimal start position.

In PCM 30 mode, the transmit route clock (XRCLK) is derived directly from the system clock by an internal clock divider. Consequently, the data received from the system interface is switched through without the need of intermediate storage.

The parity generation/checking mechanism is symmetrical to the receive path. The channel data is checked with the channel parity information generated internally or externally (input at port XCHPY with selectable input sense). Errors are reported to the microprocessor interface. To avoid difficulties with external parity generation, the parity signal for non-speech data (e.g. signaling data or channels with bit robbing information) is computed internally.

Transmitter

The serial bit stream is then processed by the transmitter which has the following functions:

- Frame/multiframe synthesis of one of the six selectable framing formats
- Insertion of service and data link information
- Remote alarm generation

Transmit Link Interface

Similar to the receive link interface two different data types with selectable output sense are supported:

- Dual rail data (PCM[+], PCM[–]) at ports XDOP, XDOM with 50% duty cycle transmitted to a line interface unit (e.g. PEB 2235, Siemens ISDN Primary Access Transceiver, IPAT). Single rail data is converted into a dual rail bit stream. In PCM 30 mode, the HDB3 line code is employed. In PCM 24 mode, selection between B8ZS or simple AMI coding with zero code suppression (B7 stuffing) is provided.
- Unipolar data at port XOID (PCM 30) or at port XDOP (PCM 24) with 100% duty cycle transmitted to a fibre optical interface.

Clocking of data is done with the positive transitions of the transmit route clock: XRCLK (2048 kHz or 1544 kHz). In PCM 30 mode, XRCLK is generated by the ACFA, whereas in PCM 24 mode it must be generated by an external clock generator.

Additionally, the dual rail outputs XTOP and XTOM are provided for test applications.

3 Additional Functions

Signaling Support

Generation of all supporting signals to achieve simple access to signaling information (CCS, CAS-CC, CAS-BR, FDL) at the system interface. In PCM 24 mode, the additional input XSIG is provided for connection to a bit-robbed signaling controller. Furthermore, the controlling of the internal signaling stacks is done by this unit.

Alarm Interrupt

Normally, the control of data transmission via the PCM line is done by polling the internal status registers of the ACFA at equidistant time intervals.

However, for fast error handling the option exists to configure a specific output port as interrupt port (AINT). This signal may be connected to an interrupt input of the board processor. Triggering of this output may be caused by up to eight maskable interrupt sources.

Single Channel Loop Back

As one of the extended test options, the single channel loop back enables reflection of a selected channel back to the system interface at port RDO.

Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Ambient temperature under bias	T_A	0 to 70	°C
Storage temperature	T_{stg}	−65 to 125	°C
Voltage on any pin with respect to ground	V_S	−0.4 V to V_{DD} +0.4 V	V

DC Characteristics

$T_A = 0$ to 70 °C; $V_{DD} = 5\ V \pm 5\%$; $V_{SS} = 0\ V$

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit	Test Conditions
L-input voltage	V_{IL}	−0.4	0.8	V	
H-input voltage	V_{IH}	2.0	V_{DD} +0.4	V	
L-output voltage	V_{OL}		0.45	V	$I_{OL} = 2$ mA
H-output voltage H-output voltage	V_{OH} V_{OH}	2.4 V_{DD} −0.5		V V	$I_{OH} = -400\ \mu A$ $I_{OH} = -100\ \mu A$
Power supply current	I_{CC}		18	mA	$V_{DD} = 5$ V Inputs at 0V/V_{DD}, no output loads
Input leakage current Output leakage current	I_{LI} I_{LO}		10	µA	$0V < V_{IN} < V_{DD}$ to 0V $0V < V_{OUT} < V_{DD}$ to 0V

Characteristics

$T_A = 25$ °C; $V_{DD} = 5\ V \pm 5\%$; $V_{SS} = 0\ V$

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit
Input capacitance	C_{IN}	5	10	pF
Output capacitance	C_{OUT}	10	20	pF
I/O	C_{IO}	8	15	pF

AC Characteristics

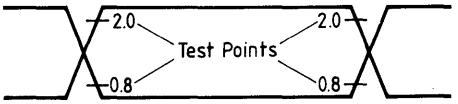
$T_A = 0$ to 70 °C; $V_{DD} = 5\ V \pm 5\%$, $V_{SS} = 0\ V$

Inputs are driven to 2.4 V for a logical '1' and to 0.4 V for a logical '0'. Timing measurements are made at 2.0 V for a logical '1' and at 0.8 V for a logical '0'.

The AC testing input/output waveforms are shown in the **figure 1**.

Figure 1

Input/Output Waveform for AC Tests

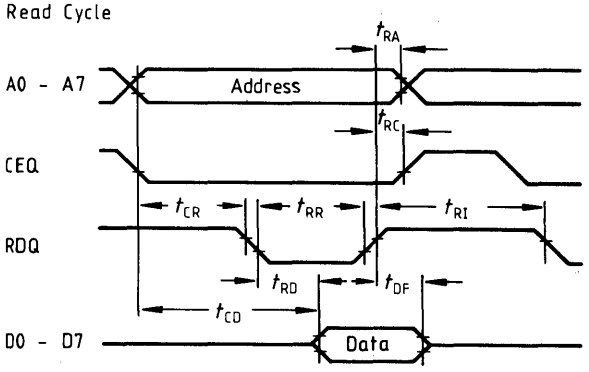


Output load: 150 pF load capacitance in connection with resistive loads for $I_{OL} = 2$ mA and $I_{OH} = -100$ uA.

Rise/fall times: 20 ns max.

µP Interface Timing

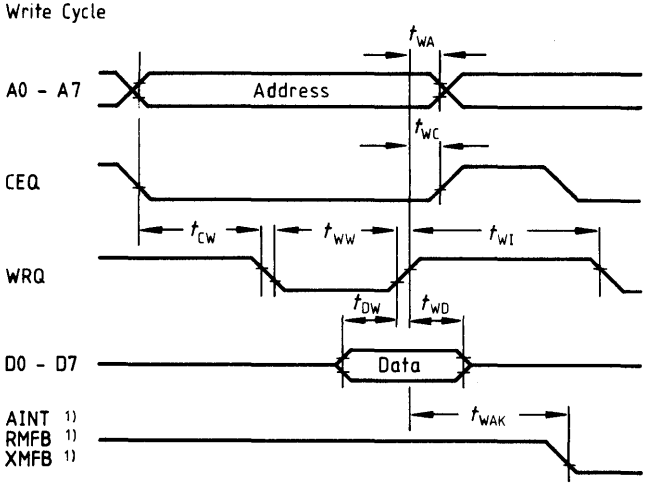
Figure 2
µP Read Timing



µP Read Timing

Parameter	Symbol	Limit Values		Unit
		min.	max.	
CEQ and ADDRESS valid to DATA valid	t_{CD}		120	ns
CEQ and ADDRESS stable before RDQ	t_{CR}	0		ns
RDQ to DATA valid	t_{RD}		110	ns
RDQ pulse width	t_{RR}	120		ns
DATA float after RDQ	t_{DF}	10	30	ns
CEQ hold after RDQ	t_{RC}	0		ns
ADDRESS hold after RDQ	t_{RA}	0		ns
RDQ control interval	t_{RI}	70		ns

Figure 3
µP Write Timing

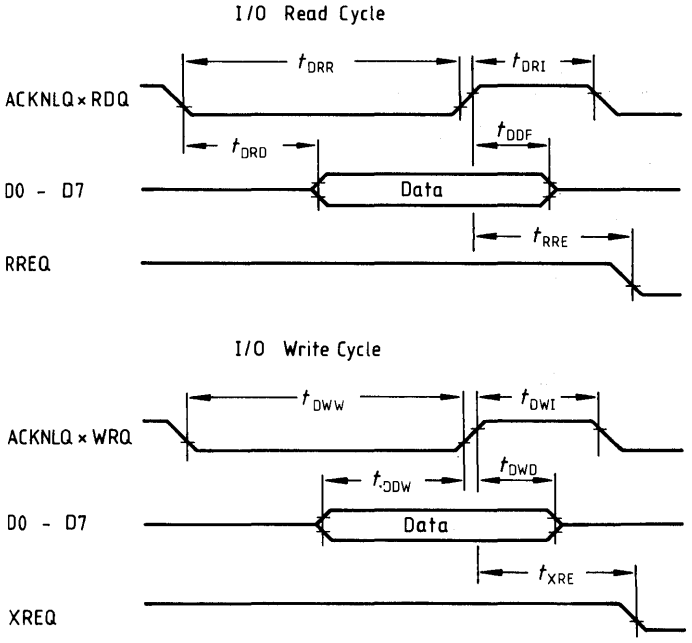


1) : In connection with assigned values of A0-A3 and D0-D7

µP Write Timing

Parameter	Symbol	Limit Values		Unit
		min.	max.	
CEQ and ADDRESS valid to WRQ valid	t_{CW}	30		ns
DATA setup before end of write	t_{DW}	30		ns
DATA hold after WRQ	t_{WD}	10		ns
WRQ pulse width	t_{WW}	70		ns
CEQ hold after WRQ	t_{WC}	10		ns
ADDRESS hold after WRQ	t_{WA}	10		ns
WRQ control interval	t_{WI}	70		ns
Interrupt acknowledge delay	t_{WAK}		$2 \times t_{CP4} + 60$ $4 \times t_{CP8} + 80$	ns

Figure 4
DMA Timing

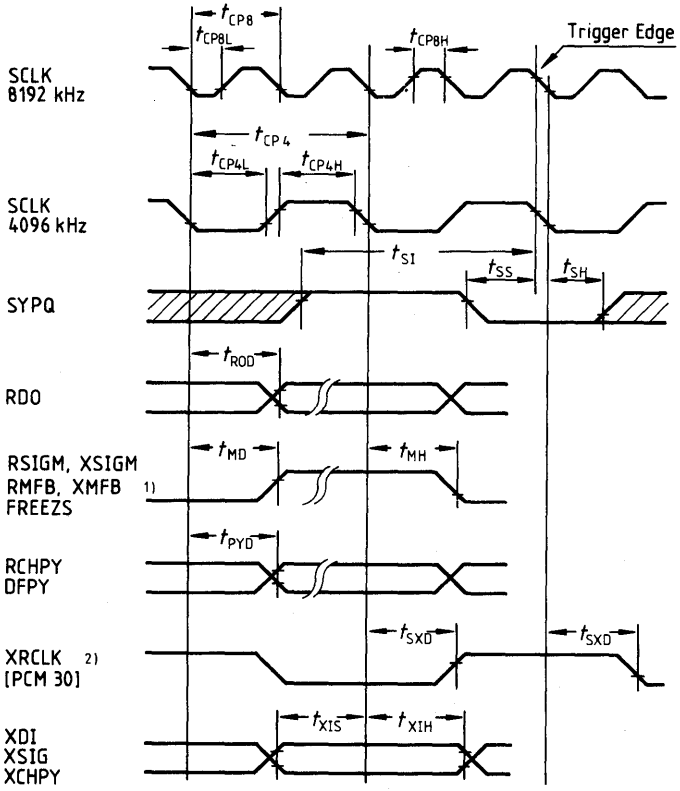


DMA Timing

Parameter	Symbol	Limit Values		Unit
		min.	max.	
RDQ to DATA valid	t_{DRD}		110	ns
DATA float after RDQ	t_{DDF}	10	30	ns
RDQ pulse width	t_{DRR}	120		ns
RDQ control interval	t_{DRI}	70		ns
RREQ reset after RDQ	t_{RRE}		130	ns
DATA setup before end of write	t_{DDW}	30		ns
DATA hold after WRQ	t_{DWD}	10		ns
WRQ pulse width	t_{DWW}	70		ns
WRQ control interval	t_{DWI}	70		ns
XREQ reset after WRQ	t_{XRE}		130	ns

Serial Interface Timing

Figure 5
System Interface Timing



1) : If not Reset via µP Interface
2) : For Even Values of XCO.XCO, Otherwise Inverted

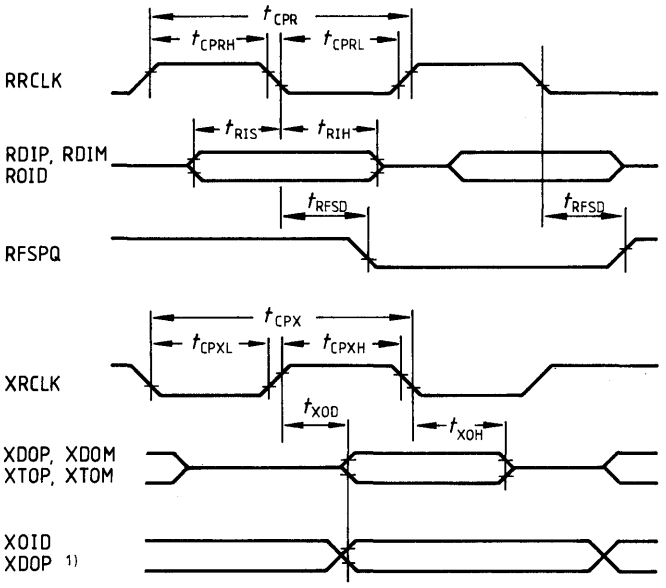
System Interface Timing

Parameter	Symbol	Limit Values				Unit
		4096 kHz SCLK		8192 kHz SCLK		
		min.	max.	min.	max.	
SCLK period 8 MHz	t_{CP8}			typ. 122		ns
SCLK period 8 MHz low	t_{CP8L}			40		ns
SCLK period 8 MHz high	t_{CP8H}			40		ns
SCLK period 4 MHz	t_{CP4}	typ. 244				ns
SCLK period 4 MHz low	t_{CP4L}	110				ns
SCLK period 4 MHz high	t_{CP4H}	110				ns
SYPQ setup time	t_{SS}	40	$t_{CP4}-30$	$t_{CP8}-40$	$t_{CP8}+40$	ns
SYPQ hold time	t_{SH}	40		40		ns
SYPQ inactive setup	t_{SI}	$t_{CP4}+30$		$2xt_{CP8}+30$		ns
RDO propagation delay	t_{ROD}		90		110	ns
Marker propagation delay	t_{MS}		100		120	ns
Marker hold	t_{MH}		100		120	ns
Parity propagation delay	t_{PYD}		100		120	ns
XRCLK to SCLK delay	t_{SXD}		110		130	ns
Transmit data setup	t_{XIS}	30		30		ns
Transmit data hold	t_{XIH}	30		30		ns

Reset Timing

Parameter	Symbol	Limit Values		Unit
		min.	max.	
RESQ low	t_{REL}	2000		ns

Figure 6
Line Interface Timing



1) : PCM 24, Optical Interface Mode

Line Interface Timing

Parameter	Symbol	Limit Values				Unit
		PCM 30		PCM 24		
		min.	max.	min.	max.	
RRCLK clock period	t_{CPR}	typ. 488		typ. 648		ns
RRCLK clock period low	t_{CPRL}	220		300		ns
RRCLK clock period high	t_{CPRH}	220		300		ns
Receive data setup	t_{RIS}	30		30		ns
Receive data hold	t_{RIH}	30		30		ns
RFSPQ propagation delay	t_{RFSD}		130		130	ns
XRCLK clock period	t_{CPX}	$2 \times t_{CP4}$ $4 \times t_{CP8}$		typ. 648		ns
XRCLK clock period low	t_{CPXL}			300		ns
XRCLK clock period high	t_{CPXH}			300		ns
Transmit data output delay	t_{XOD}		50		90	ns
Transmit data output hold	t_{XOH}	0*	50	20*	90	ns

* Test conditions: 0 °C, $C_L = 50$ pF

ISDN Primary Access Transceiver (IPAT) PEB 2235

Preliminary Data **CMOS IC**

Type	Ordering code	Package
PEB 2235-C	Q67100-H8604	C-DIP-28
PEB 2235-N	Q67100-H8685	PL-CC-28 (SMD)
PEB 2235-P	Q67100-H8603	P-DIP-28

The ISDN Primary Access Transceiver IPAT™ (PEB 2235) is a monolithic CMOS device which implements the analog receive and transmit line interface functions to primary rate PCM carriers. It may be programmed or hard wires to operate in 24 channel (T1) or 32 channel (CEPT) carrier systems.

The IPAT recovers clock and data using an adaptively controlled receiver threshold. It is transparent to ternary codes and shapes the output pulse following the AT&T Technical Advisory # 34 or CCITT G.703. The jitter tolerance of the device meets the latest CCITT (I.431 DRAFT), latest US recommendations (TR-TSY-000312), NTT specification and many other specifications by AT&T/BELLCORE. Diagnostic facilities are included.

Specially designed line interface circuits simplify the tedious task of protecting the device against overvoltage damage while still meeting the return loss requirements.

The IPAT is suitable for use in a wide range of voice and data applications such as for connections of digital switches and PABX's to host computers, for implementations of primary ISDN subscriber loops as well as for terminal applications. The maximum range is determined by the maximum allowable attenuation.

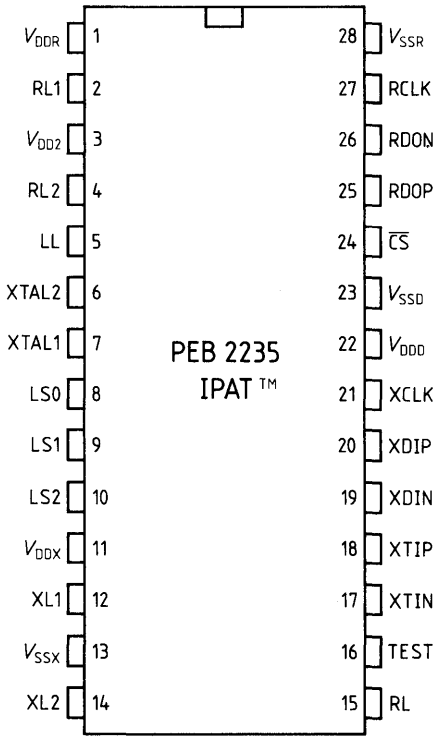
The IPAT's power consumption is mainly determined by the line length and type of the cable.

Features

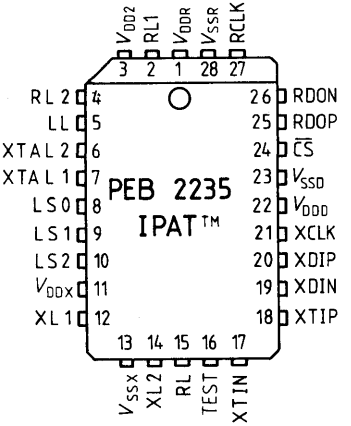
- ISDN line interface for 1544 and 2048 kbit/s (T1 and CEPT)
- Data and clock recovery
- Transparent to ternary codes
- Low transmitter output impedance for a high return loss with reasonable protection resistors (CCITT G.703 requirements for the line input return loss fulfilled).
- Adaptively controlled receiver threshold
- Programmable pulse shape for T1 applications
- Jitter specifications of CCITT I.431 DRAFT, TR-TSY-000312 and many AT&T / BELLCORE publications met.
- Jitter tolerance of receiver: 0.43 UI s
- Implements local – and remote loops for diagnostic purposes
- Monolithic line driver for a minimum of external components
- Low power, reliable 2 µ CMOS technology

Pin Configurations
(top view)

P-DIP-28



PL-CC-28



Pin Definition and Functions

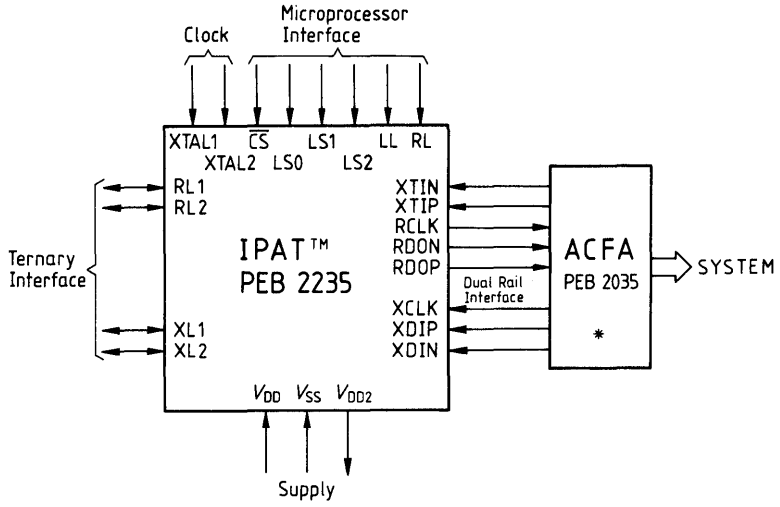
Pin No.	Symbol	Input (I) Output (O)	Function
1	$V_{DD\,R}$	I	Positive power supply for the receive subcircuits
2	RL1	I	Line receiver pin 1
3	$V_{DD\,2}$	O	Reference voltage output for tapping the input transformer
4	RL2	I	Line receiver pin 2

Pin Definition and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
5	LL	I	Local loopback: A high level selects the device for the local loopback mode
6 7	XTAL2 XTAL1	I I	Reference clock input: A 24704 or 32768 kHz crystal reference should be connected to these pins for T1 or CEPT applications, respectively. It is also possible to connect an external precision clock to XTAL1 leaving XTAL2 unconnected. The external reference must be provided at full CMOS levels.
8 9 10	LS0 LS1 LS2	I I I	Line length select: determine to what extent the line output signals are preshaped prior to transmission
11	$V_{DD\,X}$	I	Positive power supply for transmit subcircuits
12	XL1	O	Line transmitter pin 1
13	$V_{SS\,X}$	I	Ground for transmit subcircuits
14	XL2	O	Line transmitter pin 2
15	RL	I	Remote loopback: A high level puts the device to the remote loopback mode
16	TEST	I	Test input not connected or connected to V_{DD}
17 18	XTIP XTIN	I I	Positive and negative transmit test data inputs, active low, half or fully bauded
19 20	XDIP XDIN	I I	Positive and negative transmit data inputs, active low, half or fully bauded
21	XCLK	I	Transmit clock
22	$V_{DD\,D}$	I	Positive power supply for the digital subcircuits
23	$V_{SS\,D}$	I	Power ground supply for the digital subcircuits
24	$\overline{CS}$	I	$\overline{\text{Chip Select}}$: A low level selects the PEB 2235 for a register write operation
25 26	RDOP RDON	O O	Receive data output positive and negative, fully bauded, active low
27	RCLK	O	Receive clock
28	$V_{SS\,R}$	I	Power ground supply for receive subcircuits

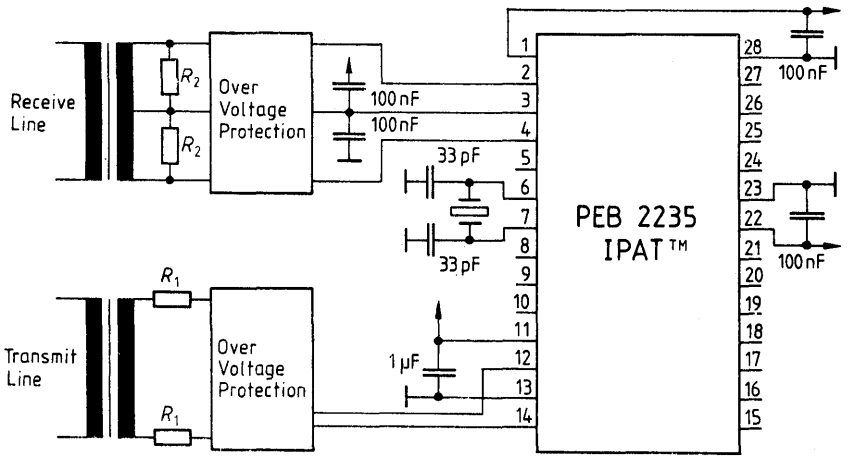
Logic Symbol and Wiring

Figure 1
Logic Diagram of the IPAT



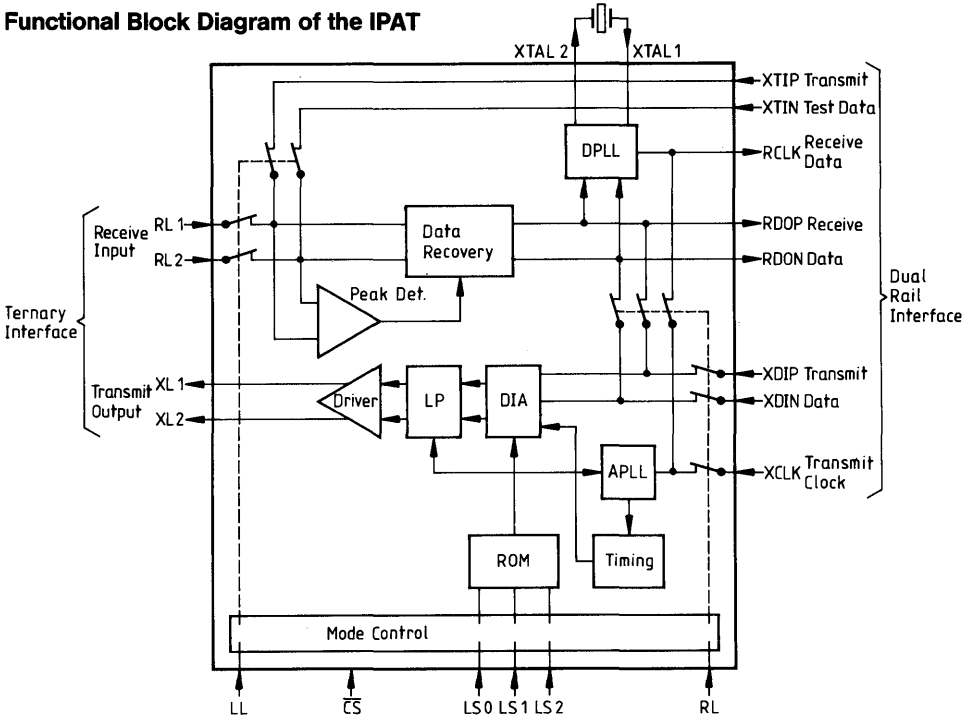
* Advanced CMOS Frame Aligner ACFA (PEB 2035) for frame alignment, coding/decoding, error checking, elastic buffering and facility signaling

Figure 2
External Wiring of the IPAT



Functional Description

Figure 3
Functional Block Diagram of the IPAT



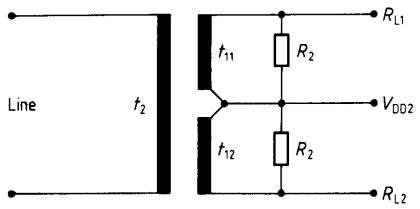
Receiver

Basic Functionally

The receiver recovers data from the ternary coded signal at the ternary interface and outputs it as two unipolar signals at the dual rail interface. One of the lines carries the positive pulses, the other the negative pulses of the ternary signal.

The signal at the ternary interface is received at both ends of a center-tapped transformer as shown in **figure 4.**

Figure 4
Receiver Configuration



The transformer is center-tapped at the IPAT-B side. The recommended transmission factors for the different line characteristic impedances are listed in **table 1.**

Table 1

Recommended Receiver Configuration Values

Application	T1	CEPT	
Characteristic Impedances [Ω]	100	120	75
$R_2 \pm (2.5\%)$ [Ω]	28.7	60	60
$t_2 : t_1 = t_2 : (t_{11} + t_{12})$	69 : 52 69 : (26 + 26)	52 : 52 52 (26 + 26)	41 : 52 41 : (26 + 26)

Wired in this way the receiver has a return loss

$a_r > 12$ dB for $0.025\, f_b \leq f \leq 0.05\, f_b$,

$a_r > 18$ dB for $0.05\, f_b \leq f \leq 1.0\, f_b$ and

$a_r > 14$ dB for $1.0\, f_b \leq f \leq 1.5\, f_b$,

with f_b being 2048 kHz. Thus is complies with CCITT G.703.

The receiver is transparent to the logical 1's polarity and outputs positive logical 1's on RDOP and negative logical 1's on RDON. RDON and RDOP are active low and fully bauded. The comparator threshold to detect logical 1's and logical 0's is automatically adjusted to be 56% of the peak signal level.

Provided the noise is below 10 $\mu V/\sqrt{Hz}$ the bit error rate will be less than 10^{-7}. The data is stable, and hence may be sampled at the falling edge of the recovered clock RCLK.

PLL

A digital PLL extracts the receive clock RCLK from the data stream received at the RL1 and RL2 lines. The PLL uses as a reference either a crystal at XTAL1 and XTAL2 or an external oscillator at XTAL1. The IPAT-B does not remove any jitter. Since the crystal frequency is 16 times the input data frequency the digital PLL adds an jitter of max. 0.0625 UI (unit intervals). In the absence of an input signal the jitter of clock, and recovered data lies within the tolerance range of the used reference.

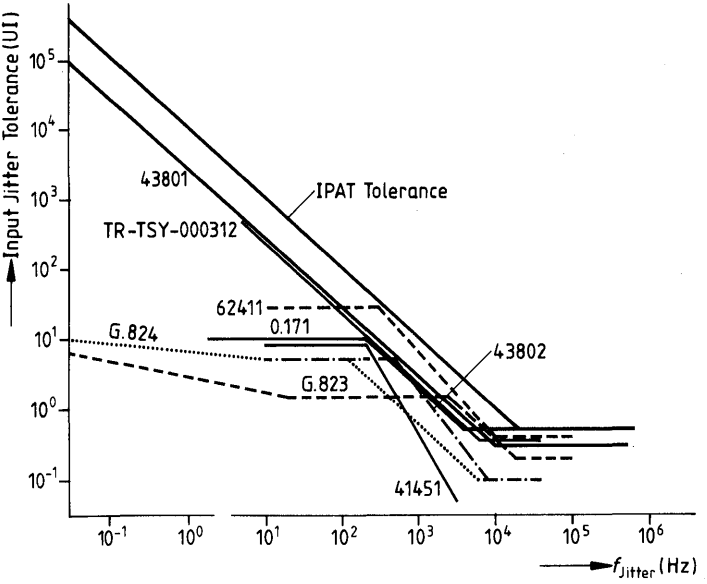
Input Jitter Tolerance

The IPAT-B receiver's tolerance to input jitter complies to CCITT and AT&T requirements for CEPT and T1 application.

Figure 5 shows the curves of the different input jitter specifications stated above as well as the IPAT-B performance at the S1/S2 interfaces.

As can be seen in **figure 5**, the curve for the IPAT-B at low frequencies describes a 20 dB/decade fall off, and at high frequencies are horizontal (at least 0.43 UI).

Figure 5
Comparison of Input Jitter Specification and IPAT Performance



Transmitter

Basic Functionality

The transmitter transforms unipolar data to ternary (alternate bipolar) return to zero signals of the appropriate shape. The unipolar data is provided at XDIP (positive pulses) and XDIN (negative pulses), synchronously with the transmit clock XCLK. XDIP and XDIN are active low and can be half or fully bauded.

The transmitter includes a programmable pulse shaper to satisfy the requirements of the AT&T Technical Advisory # 34 at the cross connect point for T1 applications. The pulse shaper is programmed via the line length selection pins LS0, LS1 and LS2. The pulse shape is formed using an analog PLL, which multiplies by four the transmit clock XCLK. This signal is used internally to generate the four segment/bit transmit pulse (CEPT: two segment/bit).

For T1 application the line length selection supports both low capacitance cable with a characteristic line capacitance of C' ≤ 40 nF/km = 65 nF/mile (e.g. MAT, ICOT) and higher capacitance cable with a characteristic line capacitance of 40 nF/km ≤ C' ≤ 54 nF/km (65 nF/mile ≤ C' ≤ 87 nF/mile) e.g. ABAM, PIC and PULP cables. This ensures that for various cable types the signal at the DSX-1 cross connect point complies with the pulse shape of the AT&T Technical Advisory # 34.

The line length is selected programming the LS0, LS1 and LS2 pins as shown in **table 2.**

Table 2
Line Length Selection

LS2 LS1 LS0		PIC/PULP-Cable range/m	ICOT-Cable range/m*
0 0 0	CEPT	–	–
0 0 1	T1/NTT	0 – 35	0 – 80
0 1 0	T1	25 – 65	65 – 145
0 1 1	T1	55 – 95	130 – 210
1 0 0	T1	85 – 125	195 – 275
1 0 1	T1	115 – 155	260 – 340
1 1 0	T1	145 – 185	325 – 405
1 1 1	T1	175 – 210	390 – 470

Note: For ICOT-cable the characteristic impedance is 140 Ω

By selecting an all-zero code for LS0, LS1 and LS2 the IPAT-B can be adopted for CEPT applications.

The pulse shape for NTT applications is achieved by using the same line length selection code as for the lowest T1 cable range. To switch the device into a low power dissipation mode, XDIP and XDIN should be held high.

The transmitter requires an external step up transformer to drive the line. The transmission factor and the source serial resistor values can be seen in **figure 6** and **table 3** for the various applications.

Figure 6
Transmitter Configuration

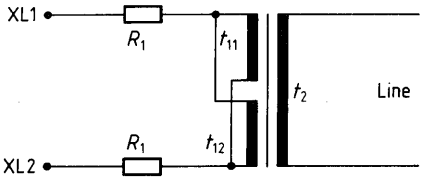


Table 3
Transmitter Configuration Values

Application	T1	CEPT	
Characteristic line impedance [Ω]	100	120	75
$t_{11}:t_2 = t_{12}:t_2$	26:69	26:52	26:41
R_1 (± 2.5%) [Ω]	4.3	15	15

Wired in this way the transmitter has a return loss

$a_r >$ 8 dB for $0.025\ f_b \leq f \leq 0.05\ f_b$,

$a_r > 14$ dB for $0.05\ f_b \leq f \leq f_b$ and

$a_r > 10$ dB for $1.0\ f_b \leq f \leq 1.5\ f_b$.

with f_b being 2048 kHz (CEPT applications). A termination resistor of 120 Ω is assumed.

In T1 applications the return loss is heigher than 10 dB.

Please note, that the transformer ratio at the receiver is half of that at the transmitter. The same type of transformer can thus be used at the receiver and at the transmitter. At the transmitter the two windings are connected in parallel, at the receiver in series. Thus, unbalances are avoided.

Output Jitter

In the absence of any input jitter the IPAT-B generates an output jitter at most 0.014 UI in CEPT and 0.01 UI in T1 applications.

Local Loopback

The local loopback mode disconnects the receive lines RL1 and RL2 from the receiver. Instead of the signals coming from the line the data provided at XTIP and XTIN is routed through the receiver. The XDIN and XDIP signals continue to be transmitted on the line. The local loopback occurs in response to LL going high.

Remote Loopback

In the remote loopback mode the clock and data recovered from the line inputs RL1 and RL2 are routed back to the line outputs XL1 and XL2 via the transmitter. As in normal mode they are also output at RDOP, RDON and RCLK. XDIP and XDIN are disconnected from the transmitter. In this mode a device jitter of 0.0765 UI for CEPT and 0.0725 UI for T1 is added.

The remote loopback mode is selected by a high RL signal.

Please keep in mind that the IPAT-B is not capable of removing jitter. Therefore in remote loopback mode jitter is not reduced. In normal applications, however, the data stream being output from the IPAT-B runs through an elastic buffer (e.g. the ACFA PEB 2035) which itself reduces jitter.

Microprocessor Interface

The IPAT-B is fully controlled by five parallel data lines (LS0, LS1, LS2, LL and RL) and one control line ($\overline{CS}$). To adapt the device to a standard microprocessor interface the low state of $\overline{CS}$ is decoded from the microprocessor address, $\overline{CS}$, $\overline{WR}$ and $\overline{ALE}$ lines.

To hardwire the chip, $\overline{CS}$ must be fixed to ground.

Loss of Signal Indication

In the case that the signal at the line receiver input (pins RL1, RL2) becomes smaller than $V_{IN} \leq 0.4\ V_{OP}$ loss of signal is indicated. This voltage value correspondings to a line attenuation of about 12 dB in the CEPT case. This is performed by turning both signals RDOP, RDON after at least 16 bits simultaneously to 5 V, i.e. a logical 0 or both lines. The following ACFA processes this indication for the system.

Operational Description

- **Reset**

  In order to work properly, the IPAT™-B needs to be started with a software reset. This is done by simultaneously setting the pins RL and LL to logical 1 (i.e. 5 V) far at least one bit period and releasing both lines thereafter simultaneously.

  It is possible to connect the pins RL and LL to V_{DD} and to consequently turn on the power supply. In this way a power-up reset is achieved.

- **Selection of CEPT of T1 Application**

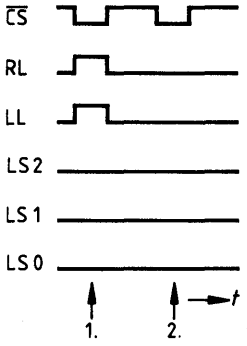
  Besides the crystal frequency the selections of CEPT or T1 application is achieved by setting the pins LS2, LS1, LS0 simultaneously with the reset to 000 for CEPT application or to a T1 line length code (001...111 **see table 2**).

- **Line Length Selection**

  In the second step the line selection code has to be given. This will be normally the same one as in the first step.

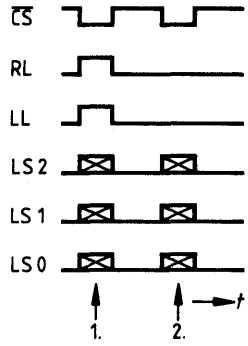
The following figures explain the procedure in some examples.

Figure 7
Timing of Software Programming for CEPT Applications



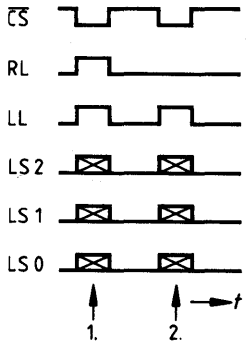
1. Reset and selection of CEPT application
2. Regular operation in CEPT application

Figure 8
Timing of Software Programming for T1 Application



1. Reset and selection of T1 application
2. Regular operation in T1 application with selected line code

Figure 9
Timing of Software Programming for LL Operation at CEPT or T1 Application



1. Reset
2. Local loop and line code selection

DC Characteristics

$T_A = 0$ to 70 °C; $V_{DD} = 5\ V \pm 5\%$, $V_{SS} = 0\ V$.

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit	Test Conditions	Pins
L-input voltage	V_{IL}	−0.4	0.8	V		All pins except RLx, XLx, XTALx, $V_{DD\,2}$
H-input voltage	V_{IH}	2.0	V_{DD}+0.4	V		
L-output voltage	V_{OL}		0.45	V	$I_{OL} = 2$ mA	
H-output voltage H-output voltage	V_{OH} V_{OH}	2.4 V_{DD}−0.5		V V	$I_{OH} = -400\ \mu A$ $I_{OH} = -100\ \mu A$	
Input leakage current Output leakage current	I_{LI} I_{LO}		10	µA	$0\ V < V_{IN} < V_{DD}$ to 0 V $0\ V < V_{OUT} < V_{DD}$ to 0 V	
Peak voltage of a mark (CEPT) Peak voltage of a mark (T1)	$V_{X\,CEPT}$ $V_{X\,T1}$	2.7 1.8 1.8	3.3 3.4 3.4	V V V	wired according **figure 6** and **table 3** T1 application: depending on line length	XL1, XL2
Transmitter output impedance	R_X		0.3	Ω		
Transmitter output current	I_X		50 150	mA mA	CEPT application T1 application: depending on line length	
Receiver input peak voltage of a mark	V_R*	0.4	2.5	V	BER 10^{-7}, wired according **figure 4** **table 1**	RL1, RL2
Receiver input threshold	$V_{R\,TH}$		56	%	of mark peak	
Voltage at V_{DD2}	$V_{DD\,2}$	2.4	2.6	V		
L-input voltage	$V_{XTAL\,IL}$	−0.4	1.0	V		XTAL1, XTAL2
H-input voltage	$V_{XTAL\,IH}$	4.0	V_{DD}+0.4	V		
Input leakage current	I_{XTALI}		10	µA	$0\ V \le V_{IN} \le V_{DD}$ to 0 V	
Operation power supply current	I_{CC}	40 55	100 220	mA mA	CEPT application T1 application, min value for all zeros, max value for all ones and max lines length for T1 appl	

* measured against V_{DD2}

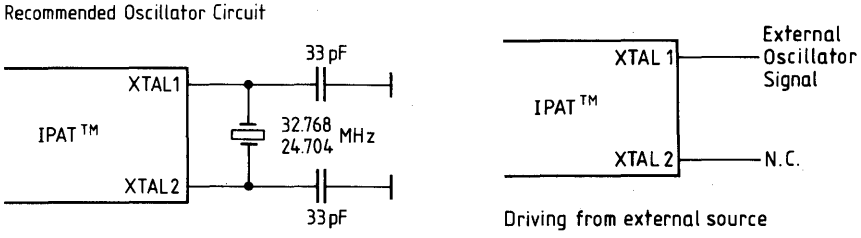
Capacitances

$T_A = 25\,°C$, $V_{DD} = 5\,V \pm 5\%$, $V_{SS} = 0\,V$

Parameter	Symbol	Limit Values		Unit	Pins
		min.	max.		
Input capacitance	C_{IN}		10	pF	all except RLx, XLx, XTALx
Output capacitance	C_{OUT}		15	pF	all except RLx, XLx, XTALx
Input capacitance	C_{IN}		7	pF	RLx
Output capacitance	C_{OUT}		20	pF	XLx
Load capacitance	C_{LD}		10	pF	XTALx

Recommended Oscillator Circuits

Figure 10
Oscillator Circuits



If no crystal is used XTAL1 has to be connected to an external precision clock source and XTAL2 left unconnected.

In CEPT applications, the oscillator circuit should provide a 32768 kHz clock, in T1 applications 24704 kHz.

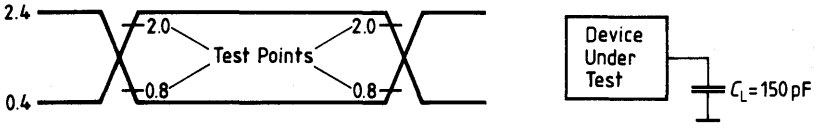
If no signal is received, a ± 50 ppm frequency range of the oscillator circuit transforms into a ± 50 ppm range of the RCLK signal.

AC Characteristics

$T_A = 0$ to 70 °C, $V_{DD} = 5\ V \pm 5\%$

Figure 11

Oscillator Circuits



Except from the ternary and clock interface, inputs are driven at 2.4 V for a logical 1 and at 0.4 V for a logical 0. Timing measurements are made at 2.0 V for a logical 1 and at 0.8 V for a logical 0. The AC testing input/output waveforms are shown in **figure 13.**

In the receive direction the IPAT-B adds at most 0.0625 UI intrinsic jitter. This is true for both jitter free as well as jitterized inputs. In transmit direction the IPAT-B adds at most 0.014 UI of jitter in CEPT and 0.01 UI in T1 applications measured in the frequency range 20 Hz...185 kHz.

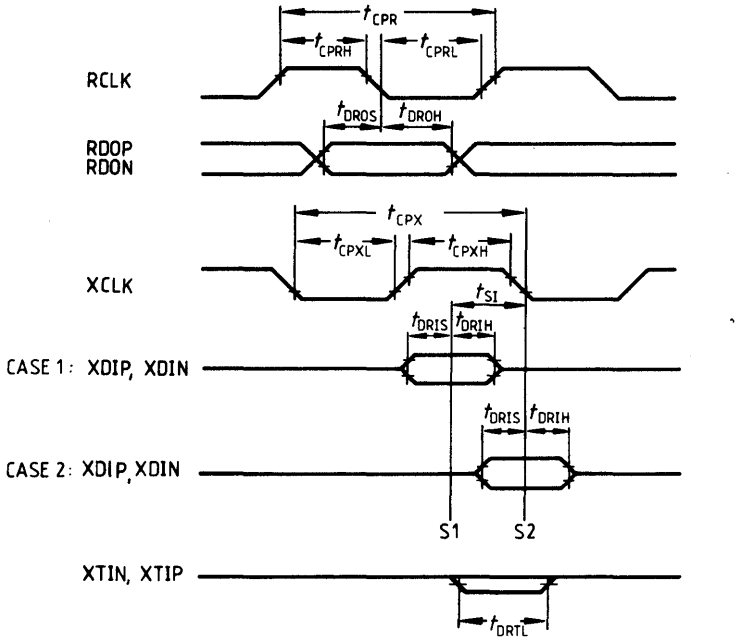
In both directions the device does not remove or attenuate the accumulated jitter.

Dual Rail Interface

RDOP, RDON, XDIP, XDIN, XTIP, XTIN are active low.

Figure 12

Timing of the Dual Rail Interface

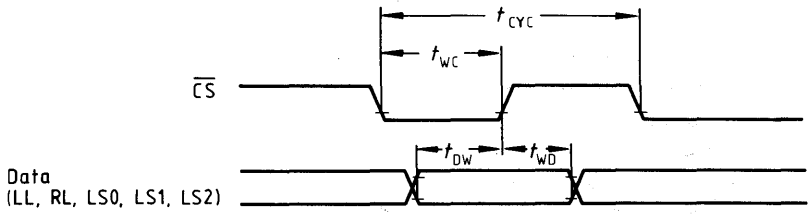


Dual Rail Interface Timing Parameter Values

Parameter	Symbol	Limit Values				Unit
		PCM 30		PCM 24		
		min.	max.	min.	max.	
RCLK clock period	t_{CPR}	typ. 488		typ. 648		ns
RCLK clock period low	$t_{CPR\,L}$	235		310		ns
RCLK clock period high	$t_{CPR\,H}$	235		310		ns
Dual rail output setup	$t_{DRO\,S}$	230		300		ns
Dual rail output hold	$t_{DRO\,H}$	230		300		ns
XCLK clock period	t_{CPX}	typ. 488		typ. 648		ns
XCLK clock period low	$t_{CPX\,L}$	80	300	100	430	ns
XCLK clock period high	$t_{CPX\,H}$	125	350	170	500	ns
Sampling intervall	t_{SI}	55	67	75	87	ns
Dual rail input setup	$t_{DRI\,S}$	25		25		ns
Dual rail input hold	$t_{DRI\,H}$	25		25		ns
Dual rail test low	$t_{DRT\,L}$	170		220		ns

Microprocessor Interface

Figure 13
Timing of the Microprocessor Interface

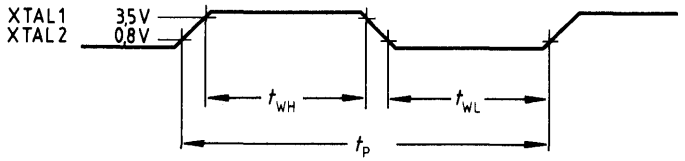


Parameter	Symbol	Limit Values		Unit
		min.	max.	
$\overline{CS}$ pulse width	t_{WC}	60		ns
Data set up time to $\overline{CS}$	t_{DW}	35		ns
Data hold time from $\overline{CS}$	t_{WD}	10		ns
Cycle Time	t_{CYC}	120		ns

XTAL Timing

Figure 14

Timing of XTAL1/XTAL2



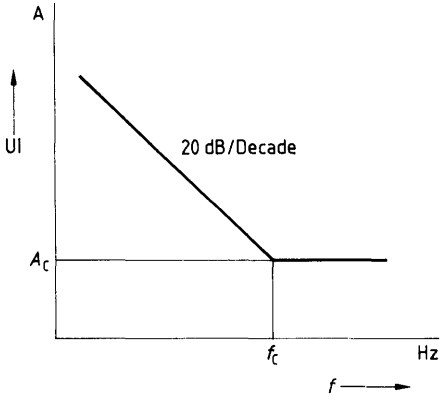
Clock Rail Interface Timing Parameter Values

Parameter		Symbol	Limit Values min.	typ.	max.	Unit
Clock period of crystal/clock	CEPT	t_P		30.5		ns
	T1	t_P		40.5		ns
High phase of crystal/clock	CEPT	t_{WH}	10			ns
	T1	t_{WH}	14			ns
Low phase of crystal/clock	CEPT	t_{WL}	10			ns
	T1	t_{WL}	14			ns

Ternary Interface – Receiver

Figure 15

IPAT Receive Jitter Tolerance



IPAT Receive Jitter Tolerance

Parameter		Symbol	Limit Values min.	max.	Unit
Corner frequency	CEPT	f_C	40		kHz
	T1	f_C	30		kHz
Corner amplitude	CEPT	A_C	0.43		UI
	T1	A_C	0.43		UI

Ternary Interface – Transmitter

The IPAT-B meets both CCITT and T1 pulse template requirements.

Figure 16

Pulse Template at the Transmitter Output for CEPT Applications

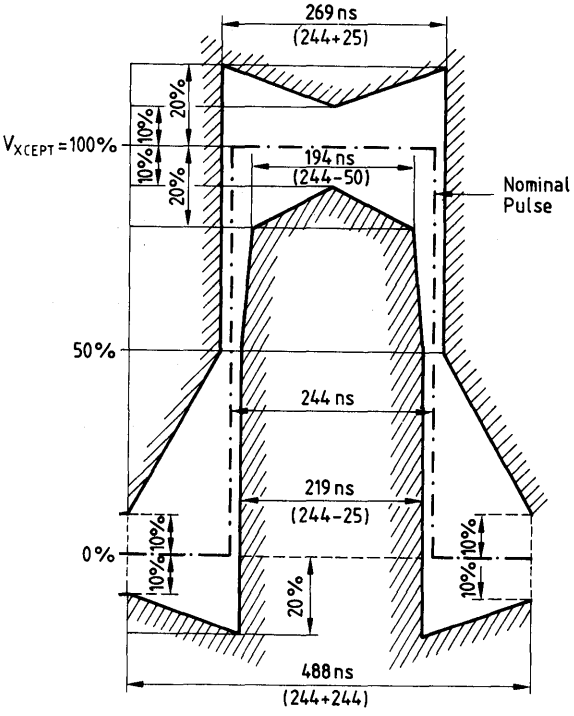


Figure 17

T1 Pulse Shape at the Cross Connect Point

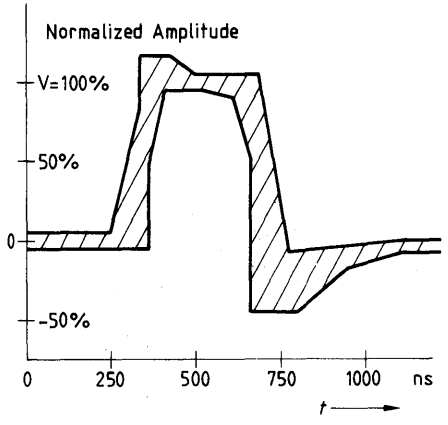


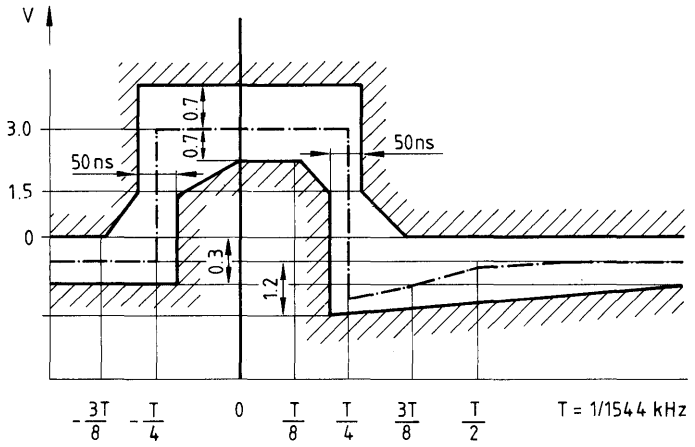
Table 4

T1 Pulse Template Corner Points at the Cross Connect Point

Maximum Curve	Minimum Curve
(0, 0.05)	(0, -0.05)
(250, 0.05)	(350, -0.05)
(325, 0.80)	(350, 0.50)
(325, 1.15)	(400, 0.95)
(435, 1.15)	(500, 0.95)
(500, 1.05)	(600, 0.90)
(675, 1.05)	(650, 0.50)
(725, -0.07)	(650, -0.45)
(1100, 0.05)	(800, -0.45)
(1250, 0.05)	(925, -0.20)
	(1100, -0.05)
	(1250, -0.05)

Figure 18

Pulse Shape at NTT Interface



Overvoltage Tolerance

To prevent the IPAT from being damaged by overvoltage (i.e. from lightning), external devices like diodes or resistors have to be connected to one or both sides of the line interface transformers. Thus, overvoltage peaks are cut off. However, some residual overvoltage may remain.

The IPAT simplifies the task of designing external protection circuit. Its transmitter exhibits a low line impedance so that reasonable external resistors can be connected to the line outputs. **Figure 6** with the element values of **table 3** gives an example of how an overvoltage protection against residual overvoltages at the ternary interface can be accomplished. The solution shown also meets the stated return loss requirements.

A similar consideration applies to the receiver. The resistors R2 of **figure 4** provide protection against residual overvoltages by attenuating voltages of both polarities across RL1 and RL2.

The maximum input current allowed to reach the IAPT pins under overvoltage conditions is given as a function of the width of a rectangular input current pulse according to **figure 18. Figure 19** shows the curve of the maximum allowed input current across the pins RL1 and RL2, **figure 20** across the pins XL1 and XL2.

Figure 18

Measurement of Overvoltage Stress

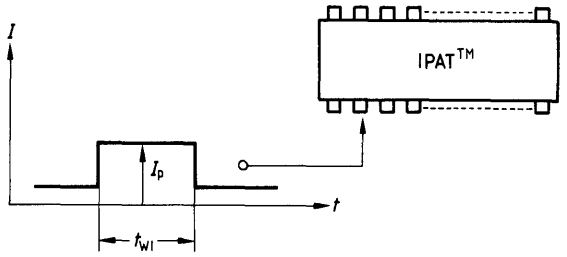


Figure 19

Tolerated Input Current at the RL1,2 Pins

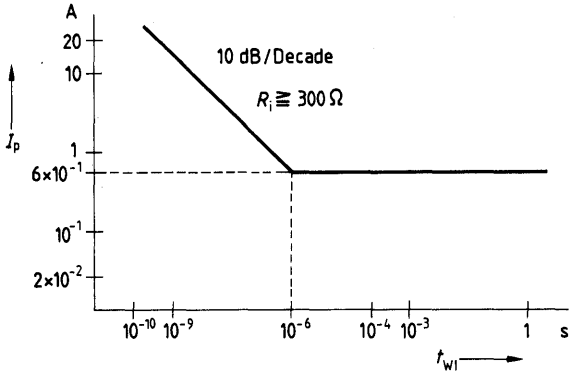
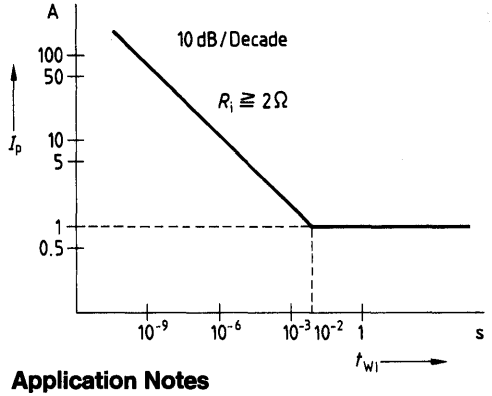


Figure 20

Tolerated Input Current at the XL1,2 Pins



Application Notes

The high transmitter output currents of up to 160 mA require a careful consideration of the on board power supply and ternary interface output line routing.

Memory Time Switch CMOS (MTSC)

PEB 2045
PEF 2045

Preliminary Data

CMOS IC

Type	Ordering Code	Package
PEB 2045 P	Q67100-H8322	P-DIP-40
PEB 2045 C	Q67100-H8323	C-DIP-40
PEB 2045 N	Q67100-H8602	PL-CC-44 (SMD)
PEF 2045 P	Q67100-H6056	P-DIP-40
PEF 2045 C	Q67100-H6054	C-DIP-40
PEF 2045 N	Q67100-H6055	PL-CC-40 (SMD)

The Siemens memory time switch is a monolithic CMOS circuit connecting any of 512 incoming PCM channels to any of 256 outgoing PCM channels. The on-chip connection memory is accessed via the 8 bit µP interface.

The components are fabricated using the advanced CMOS technology from Siemens and is mounted in a C-DIP-40, P-DIP-40 or a PL-CC-44 package. Inputs and outputs are TTL-compatible.

The PEB 2045 works with either a 8192 kHz clock or a 4096 kHz clock. Henceforth, the respective clock periods are referred to as t_{CP8} and t_{CP4}.

The bits of a time slot are numbered 0 through 7. Bit 0 of a time slot is the first bit to be received or transmitted by the MTSC, bit 7 the last.

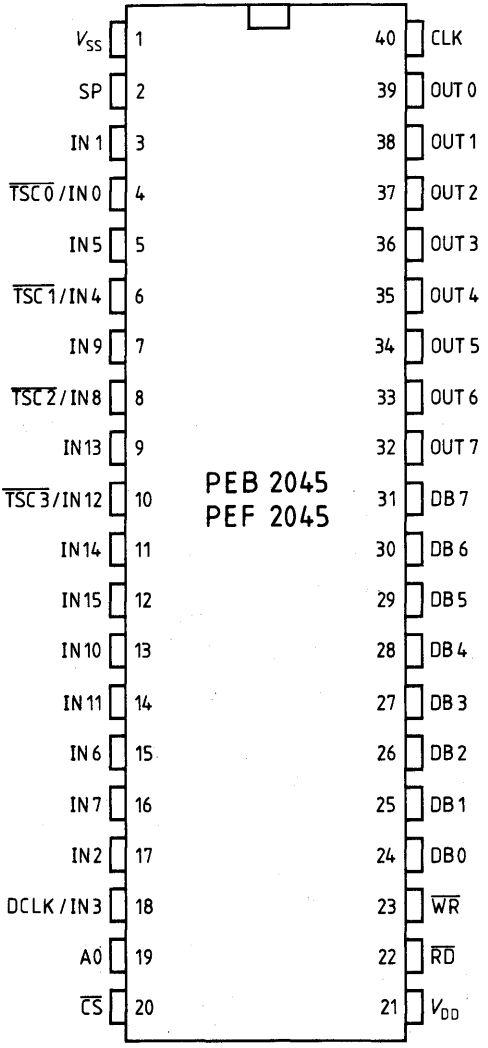
The components PEB 2045 and PEF 2045 are functionally identical. The difference between the two types lies in the temperature range. The PEB 2045 operates in the temperature range 0 to 70 °C, the PEF 2045 in the range −40 to +85 °C.

Features

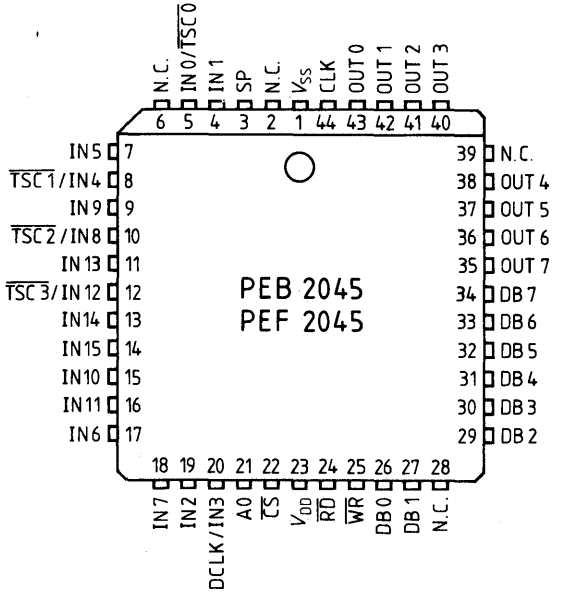
- Time/space switch for 2048, 4096 or 8192 kbit/s PCM systems
- Switching of up to 512 incoming PCM channels to up to 256 outgoing PCM channels
- 16 input and 8 output PCM lines
- Different kinds of modes (2048, 4096, 8192 kbit/sec or mixed mode)
- Configurable for primary access and standard applications
- Programmable clock shift with half clock step resolution for input and output in primary access configuration
- Configurable for a 4096 and 8192 kHz device clock
- Tristate function for further expansion and tandem operation
- Tristate control signals for external drivers in primary access configuration
- 2048 kHz clock output in primary access configuration
- Space switch mode
- 8 bit µP interface
- Single +5 V power supply
- Advanced low power CMOS technology
- Pin and software compatible to the PEB 2040

Pin Configurations
(top view)

P-DIP-40
C-DIP-40



PL-CC-44



Pin Definition and Functions

P-DIP Pin No.	PL-CC Pin No.	Symbol	Input (I) Output (O)	Function
1	1	V_{SS}	I	**Ground** (OV)
2	3	SP	I	**Synchronization Pulse:** The PEx 2045 is synchronized relative to the PCM system via this line.
3	4	IN1	I	**PCM Input Ports:** Serial data is received at these lines at standard TTL levels.
5	7	IN5	I	
7	9	IN9	I	
9	11	IN13	I	
11	13	IN14	I	
12	14	IN15	I	
13	15	IN10	I	
14	16	IN11	I	
15	17	IN6	I	
16	18	IN7	I	
17	19	IN2	I	
4	5	IN0/$\overline{TSC0}$	I/O	**PCM Input Port / Tristate Control:** In standard configuration these pins are used as input lines, in primary access configuration they supply control signals for external devices.
6	8	IN4/$\overline{TSC1}$	I/O	
8	10	IN8/$\overline{TSC2}$	I/O	
10	12	IN12/$\overline{TSC3}$	I	
18	20	IN3/DCLK	I/O	**PCM Input Port / Data Clock:** In standard configuration IN3 is the PCM input line 3, in primary access configuration it provides a 2048 kHz data clock for the synchronous interface.
19	21	AO	I	**Address 0:** When high, the indirect register access mechanism is enabled. If A0 is logical 0 teh mode and status registers can be written to and read respectively.
20	22	$\overline{CS}$	I	**Chip Select:** A low level selects the PEx 2045 for a register access operation.
21	23	V_{DD}	I	**Supply Voltage:** 5 V ± 5%.
22	24	$\overline{RD}$	I	**Read:** This signal indicates a read operation and is internally sampled only if $\overline{CS}$ is active. The MTSC puts data from the selected internal register on the data bus with the falling edge of $\overline{RD}$. $\overline{RD}$ is active low.

Pin Definition and Functions (cont'd)

P-DIP Pin No.	PL-CC Pin No.	Symbol	Input (I) Output (O)	Function
23	25	$\overline{WR}$	I	**Write:** This signal initiates a write operation. The $\overline{WR}$ input is internally sampled only if $\overline{CS}$ is active. In this case the MTSC loads an internal register with data from the data bus at the rising edge of $\overline{WR}$. $\overline{WR}$ is active low.
24	26	DB0	I/O	**Data Bus:** The data bus is used for communication between the MTSC and a processor.
25	27	DB1	I/O	
26	29	DB2	I/O	
27	30	DB3	I/O	
28	31	DB4	I/O	
29	32	DB5	I/O	
30	33	DB6	I/O	
31	34	DB7	I/O	
32	35	OUT7	0	**PCM Output Port:** Serial data is sent by these lines at standard CMOS or TTL levels. These pins can be tristated.
33	36	OUT6	0	
34	37	OUT5	0	
35	38	OUT4	0	
36	40	OUT3	0	
37	41	OUT2	0	
38	42	OUT1	0	
39	43	OUT0	0	
40	44	CLK	I	**Clock:** 4096 or 8192 kHz device clock

Figure 1
Functional Symbol for the Standard Configuration

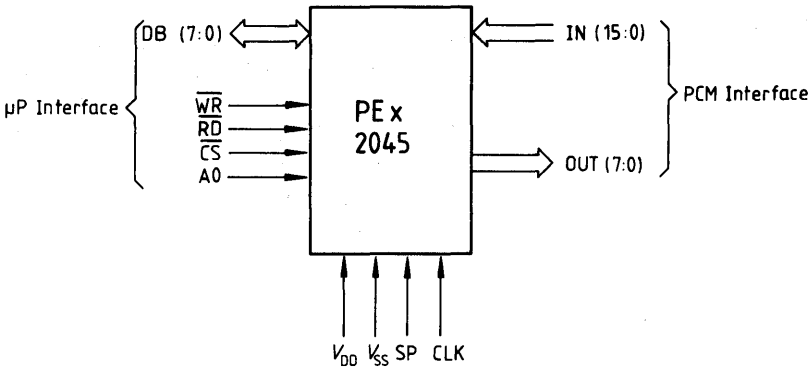
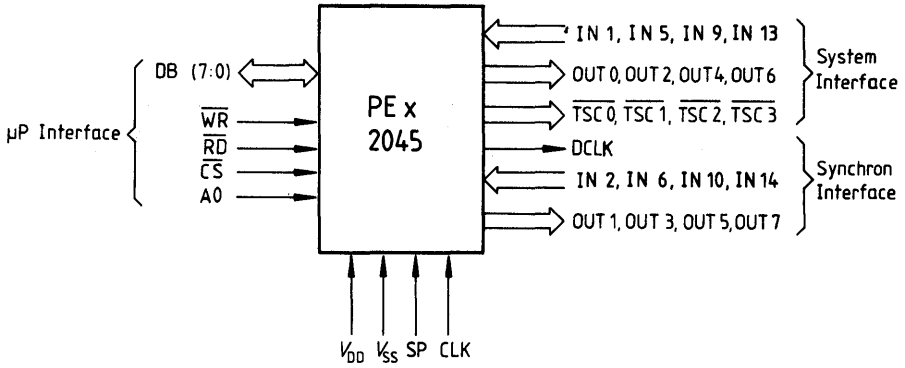


Figure 2
Functional Symbol Primary Access Configuration

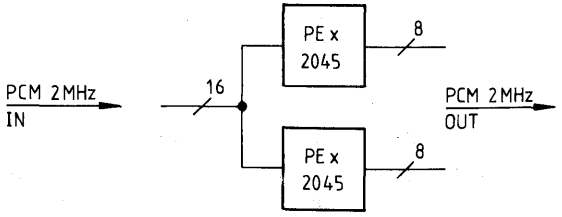


System Integration

The main application fields for the PEx 2045 are in switches and primary access units. **Figure 3** shows a non-blocking switch for 512 input and 512 output channels using only two devices. **Figure 4** shows how eight devices can be arranged to form a non-blocking 1024 channel switch.

Figure 3

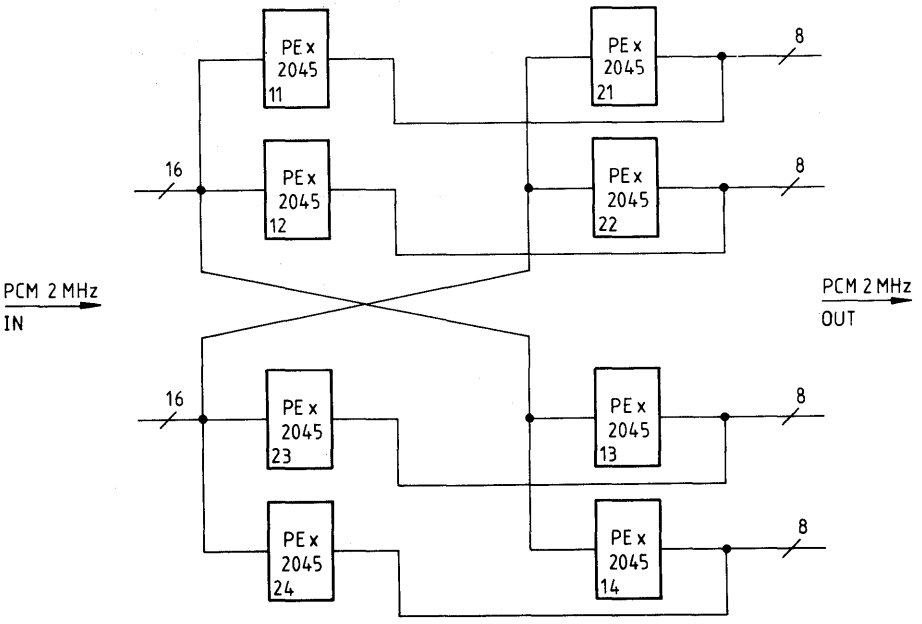
Memory Time Switch 16/16 for a Non-blocking 512-Channel Switch



This is possible due to the tristate capability of the PEx 2045.

Figure 4

Memory Time Switch 32/32 for a Non-blocking 1024-Channel Switch



Functional Description

The PEx 2045 is a memory time switch device. It can connect any of 512 PCM input channels to any of 256 output channels.

The input information of a complete frame is stored in the on-chip 4 kbit speech memory SM. (**See figure 5**). The incoming 512 channels of 8 bits each are written in sequence into fixed positions in the SM. This is controlled by the input counter in the timing control block with a 8 kHz repetition rate.

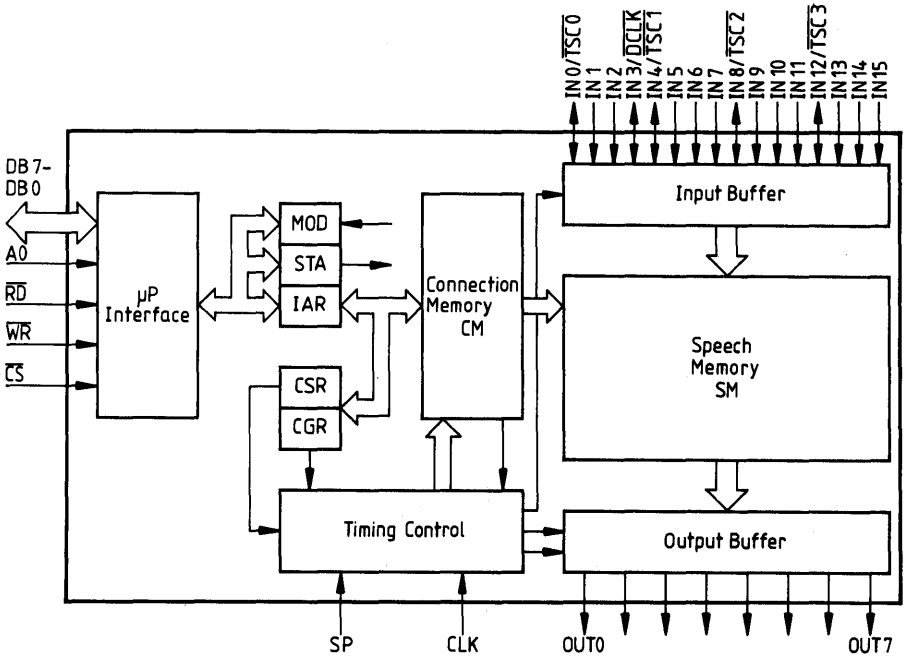
For outputting, the connection memory (CM) is read in sequence. Each location in CM points to a location in the speech memory. The byte in this speech memory location is read into the current output time slot. The read access of the CM is controlled by the output counter which also resides in the timing control block.

Hence the CM needs to be programmed beforehand for the desired connection. The CM address corresponds to one particular output time slot and line number. The contents of this CM address points to a particular input time slot and line number (now resident in the SM).

The PEx 2045 works in standard configuration for usual switching applications, and in the primary access configuration where it realizes, together with the PEB 2035 (ACFA) and the PEB 2235 (IPAT), the system interface for up to four primary multiplex address lines.

Figure 5

Block Diagram of the PEx 2045



Operational Description

Power Up

Upon power up the PEx 2045 is set to its initial state. The mode and configuration register bits are all set to logical 1, the clock shift register bits to logical 0. The status register **B**-bit is undefined, the **Z**-bit contains logical 0, the **R**-bit is undefined.

This state is also reached by pulling the $\overline{WR}$ and $\overline{RD}$ signals to logical 0 at the same time, (software reset). For the software reset the state of $\overline{CS}$ is of no significance.

Initialization Procedure

After power up a few internal signals and clocks need to be initialized. This is done with the initialization sequence. To give all signals and clocks a defined value the MTSC must encounter three falling and two rising edges of the SP signal. The resulting SP pulses may be of any length allowed in normal operation, the time interval between the two SP pulses may be of any length down to 250 nsec.

With all signals being defined, the CM needs to be reset. To do that a logical 0 is written into **MOD:RC. STA:B** is set. The resulting CM reset is finished after at most 250 µsec and is indicated by the status register **B**-bit being logical 0. Changing the pulse shaping factor N during CM reset may result in a CM reset time longer than 250 µsec.

To prepare the PEx 2045 for programming the CM, the **RI**- bit in the mode register must be reset. Note that one mode register access can serve to reset both **RC** and **RI** bits as well as configurating to chip (i.e. selecting operating mode etc.).

Figure 6
Initializing the PEx 2045 for a 8192-kHz-Device Clock

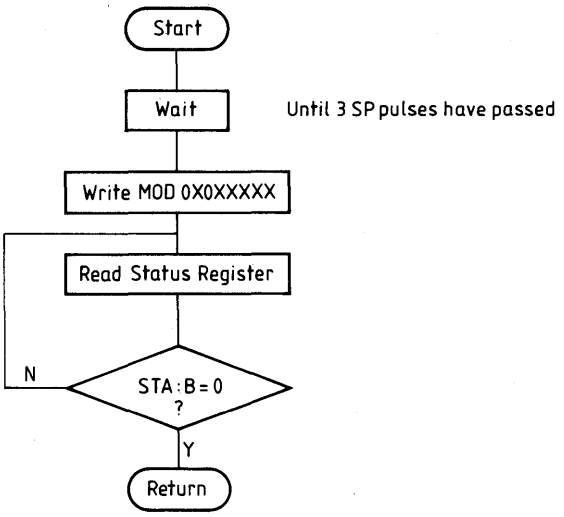
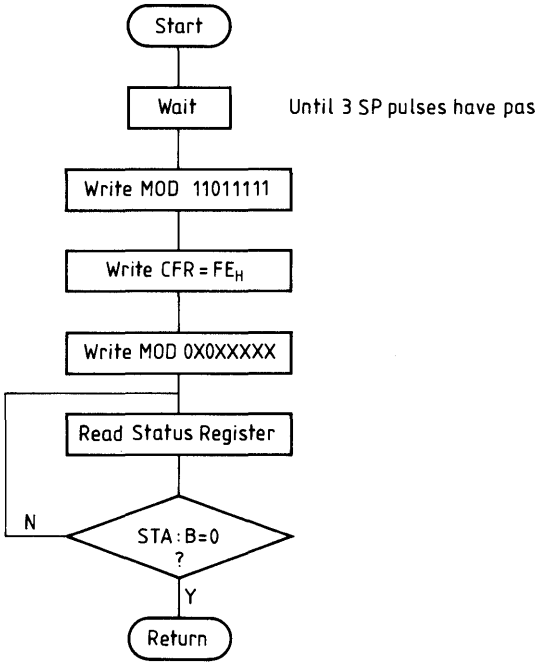


Figure 7
Initializing the PEx 2045 for a 4096-kHz-Device Clock



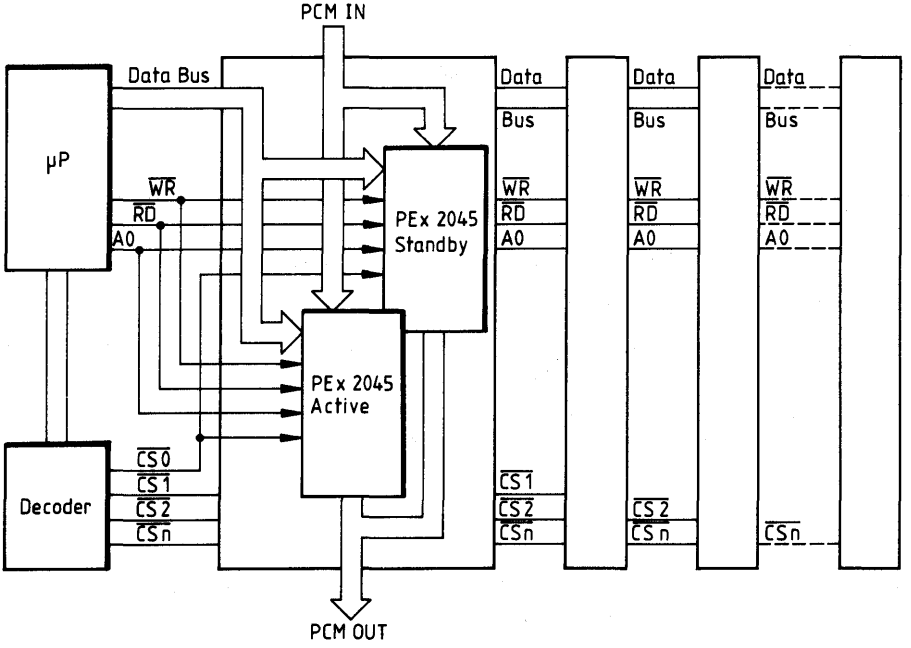
Operation with a 4096-kHz-Device Clock

In order for the MTSC to operate with a 4096-kHz-device clock the **CPS**-bit in the **CFR** register needs to be reset. This has to be done before the CM reset and needs up to 1.8 µsec. Please keep in mind, **MOD:RI** has to be reset prior to performing an indirect register access. For a flow chart of this process refer to **figure 7**.

Standby Mode

With **MOD:SB** being logical 1 the PEx 2045 works as a backup device in redundant systems. It can be accessed via the µP interface and works internally like an active device. However, the outputs are high impedance. If the **SB**-bit is reset the outputs are switched to low impedance for the programmed active channels and this MTSC can take over from another device which has been recognized as being faulty. **See figure 8.**

Figure 8
Device Setup in Redundant Systems



Detailed Register Description

The following registers may be accessed:

Table 1

Addressing the Direct Registers

Address A0	Write Operation	Read Operation
0	MOD	STA
1	IAR	IAR

The chapters in this section cover the registers in detail.

Mode Register (MOD)

Access: write on address 0

DB 7							DB 0
RC	TE	RI	SB	MI1	MI0	MO1	MO0

Value after power up: FF_H

RC: **R**eset **C**onnection memory; writing a zero to this bit causes the complete connection memory to be overwritten with 200_H (tristate). During this time **STA:B** is set. The maximum time for resetting the connection memory is 250 µs.

TE: **T**ristate **E**nable; this bit determines which tristating scheme is activated:

TE = 1: If the speech memory address written into the connection memory is S8 – S0 = 0, the output channel is tristated.

TE = 0: The S9 bit written into the connection memory is interpreted as a validity bit: S9 = 0 enables the programmed connection, S9 = 1 tristates the output.

Note: If TE = 1, time slot 0 of the logical input line 0 cannot be used for switching.

RI: **R**eset **I**ndirect access mechanism; setting this bit resets the indirect access mechanism. RI has to be cleared before writing/reading IAR after reset.

SB: **S**tand **B**y; by selecting SB = 1 all outputs are tristated The connection memory works normally. The PEx 2045 can be activated immediately by resetting SB.

MI1/0:

MO1/0: Input/Output Operation Mode; these bits define MO1/0 the bit rate of the input and output lines. The bit rates are given in **table 2**, the corresponding pin functions in **table 3** (standard configuration) and **table 4** (primary multiplex access configuration).

Table 2
Input/Output Operating Modes

MI1	MI0	MO1	MO0	Input Mode		Output Mode	
0	0	0	0	16x2	Mbit/s	8x2	Mbit/s**
0	0	0	1	16x2	Mbit/s	2x8	Mbit/s
0	0	1	0	16x2	Mbit/s	4x2/1x8	Mbit/s
0	1	0	0	4x8	Mbit/s	8x2	Mbit/s
0	1	0	1	4x8	Mbit/s	2x8	Mbit/s
0	1	1	0	4x8	Mbit/s	4x2/1x8	Mbit/s
1	0	0	0	2x8/8x2	Mbit/s	8x2	Mbit/s
1	0	0	1	2x8/8x2	Mbit/s	2x8	Mbit/s
1	0	1	0	2x8/8x2	Mbit/s	4x2/1x8	Mbit/s**
0	0	1	1	8x4	Mbit/s	4x4	Mbit/s
0	1	1	1	4x8	Mbit/s	4x4	Mbit/s
1	1	1	1	4x4/8x2	Mbit/s	4x2/2x4	Mbit/s**
1	0	1	1	8x4	Mbit/s	2x8	Mbit/s
1	1	0	1	16x8	Mbit/s	2x8	Mbit/s*
1	1	0	0	unused			
1	1	1	0	unused			

* for space switch application only
** can also be used for primary access configuration

In the mixed modes the first bit rate refers to the odd line numbers, the second one to the even line numbers.

Table 3
Input and Output Pin Arrangement for the Standard Configuration

Input Pin Arrangement

Pin No. P-DIP	Pin No. PL-CC	16x8 Mbit/s 16x2 Mbit/s	4x8 Mbit/s	8x2 + 2x8 Mbit/s		8x4 Mbit/s	8x2 + 4x4 Mbit/s	
3	4	IN 1						
4	5	IN 0		IN 0			IN 0	
5	7	IN 5						
6	8	IN 4		IN 4			IN 4	
7	9	IN 9				IN 1		IN 1
8	10	IN 8		IN 8		IN 0	IN 8	
9	11	IN 13	IN 1		IN 1	IN 5		IN 5
10	12	IN 12	IN 0	IN 12		IN 4	IN 12	
11	13	IN 14	IN 2	IN 14		IN 6	IN 14	
12	14	IN 15	IN 3		IN 3	IN 7		IN 7
13	15	IN 10		IN 10		IN 2	IN 10	
14	16	IN 11				IN 3		IN 3
15	17	IN 6		IN 6			IN 6	
16	18	IN 7						
17	19	IN 2		IN 2			IN 2	
18	20	IN 3						

Note: The input line numbers shown are the logical line numbers to be used for programming the connection memory. In the case of 16 input lines the logical line numbers are identical to the pin names.

Output Pin Arrangement

Pin No. P-DIP	Pin No. PL-CC	8x2 Mbit/s	2x8 Mbit/s	4x2 + 1x8 Mbit/s		4x4 Mbit/s	4x2 + 2x4 Mbit/s	
32	35	OUT 7		OUT 7			OUT 7	
33	36	OUT 6						
34	37	OUT 5		OUT 5			OUT 5	
35	38	OUT 4						
36	40	OUT 3		OUT 3		OUT 3	OUT 3	
37	41	OUT 2				OUT 2		OUT 2
38	42	OUT 1	OUT 1	OUT 1		OUT 1	OUT 1	
39	43	OUT 0	OUT 0		OUT 0	OUT 0		OUT 1

Note: The logical output line numbers shown above are identical to the pin names.

Table 4
Input, Output and Tristate Pin Arrangement for the Primary Access Configuration

	Pin No.		System	Interface Mode		
Pin-name	**P-DIP**	**PL-CC**	**2 MHz**	**4 MHz**	**8 MHz**	
TSCO TSC1 TSC2 TSC3	4 6 8 10	5 8 10 12	TSC0 TSC1 TSC2 TSC3	TSC0 TSC1	TSC0	System interface tristate control signals, clock shift programmable
OUT 0 OUT 2 OUT 4 OUT 6	39 37 35 33	43 41 38 36	OUT 0 OUT 1 OUT 2 OUT 3	OUT 0 OUT 1	OUT 0	System interface outputs clock shift programmable
IN 13 IN 9 IN 5 IN 1	9 7 5 3	11 9 7 4	IN 3 IN 2 IN 1 IN 0	IN 1 IN 0	IN 0	System interface inputs, clock shift programmable
OUT 1 OUT 3 OUT 5 OUT 7	38 36 34 32	42 40 37 35	OUT 0 OUT 1 OUT 2 OUT 3	OUT 0 OUT 1 OUT 2 OUT 3	OUT 0 OUT 1 OUT 2 OUT 3	Synchronous 2 MHz interface outputs
IN 14 IN 10 IN 6 IN 2	11 13 15 17	13 15 17 19	IN 3 IN 2 IN 1 IN 0	IN 3 IN 2 IN 1 IN 0	IN 3 IN 2 IN 1 IN 0	Synchronous 2 MHz interface inputs
Mode			0000	1111	1010	MI1, MI0, MO1, MO0

Note: The input, output and tristate control line numbers shown in the center columns of this table are logical line numbers. The corresponding pin names are listed in the left most column.

Status Register (STA)

Access: read at address 0

DB 7							DB 0
B	Z	R	0	0	0	0	0

B Busy: the chip is busy resetting the connection memory (B = 1) B is undefined after power up and logical 0 after the device initialization.

Note: The maximum time for resetting the connection memory is 250 µs.

Z incomplete instruction; a three byte indirect instruction is not completed (Z = 1). Z is 0 after power up.

Note: Z is reset and the indirect access is cancelled by setting **MOD:RI** or resetting **MOD:RC**

R initialization Request. The connection memory has to be reset due to loss of data (R = 1). The R bit is set after power failure or inappropriate clocking and reset when the connection memory reset is finished. R is undefined after power up and logical 0 after the device initialization.

Indirect Access Register (IAR)

(Read or Write Operation with Address A0 = 1)

An indirect access is performed by reading/writing three consecutive bytes (first byte = control byte, second byte = data byte, third byte = address byte) to/from IAR. The structure is shown in **table 5.**

Table 5

The 3 Bytes of the Indirect Access

Bit 7							Bit 0	
0	0	K1	K0	0	0	C1	C0	Control Byte
D7	D6	D5	D4	D3	D2	D1	D0	Data Byte
IA7	IA6	IA5	IA4	IA3	IA2	IA1	IA0	Address Byte

The control byte bits K1, K0, C1 and C0 together with the address byte determine the type of access being performed according to **table 6.**

Table 6

Encoding the Different Types of Indirect Accesses

K1	K0	C1	C0	Address Byte	Type of Access	
0	0	D9	D8	CM-Address	Read	CM
1	0	D9	D8	CM-Address	Write	CM
0	1	D9	D8	CM-Address	Write	CM
1	1	0	0	FE_H	Write	CFR
1	1	0	1	FE_H	Read	CFR
1	1	0	0	FF_H	Write	CSR
1	1	0	1	FF_H	Read	CSR

Connection Memory Access

For a connection memory access the control byte bits C1 and C0 contain the data bits D9 and D8, respectively. D9 is the validity bit which together with D8 and the data byte D7-D0 is written to the CM address IA7-IA0.

The function of the validity bit is controlled by **STA:TE**. D8-D0 and IA7-IA0 contain the information for the logical line and time-slot numbers of the programmed connection, D8-D0 for the inputs, IA7-IA0 for the outputs. **Tables 7 through 11** show the programming of these bits for the different configurations and modes.

Standard Configuration

Table 7

Time Slot and Line Programming for Standard Configuration

Standard Configuration, all Modes Except, Space Switch Mode					
2 Mbit/s input lines	Bit Bit Bit	D3 D8 D9	to to	D0 D4	Logical line number Time-slot number Valididy bit
4 Mbit/s input lines	Bit Bit Bit	D2 D8 D9	to to	D0 D3	Logical line number Time-slot number Validity bit
8 Mbit/s input lines	Bit Bit Bit	D1 D8 D9	to to	D0 D2	Logical line number Time-slot number Validity bit
2 Mbit/s output lines	Bit Bit	IA2 IA7	to to	IA0 IA0	Line number Time-slot number
4 Mbit/s output lines	Bit Bit	IA1 IA7	to to	IA0 IA2	Line number Time-slot number
8 Mbit/s output lines	Bit Bit	IA0 IA7	to	IA1	Line number time-slot number

Space Switch Mode

Table 8
Time Slot and Line Programming for Space Switch Mode

Space-Switch-Mode	(MI1 = 1, MI0 = 1; MO1 = 0, MO0 = 1)				
8 Mbit/s input lines	Bit	D0	to	D3	Logical line number.
	Bit	D4	to	D8	The lower 5 bits of the time-slot number
	Bit	D9			Validity bit
8 Mbit/s output lines	Bit	IA0			Logical line number
	Bit	IA1	to	IA7	Time-slot number

N is fixed to 70. The selection of one specific input time slot is possible by writing the connection memory (CM) as shown below.

Table 9
Programming Input and Output Lines and Time Slots in Space Switch Mode

In CM address 00-3F:	D8-D4 (SM addr.)	=	TS0 - TS3
In CM address 40-7F:	D8-D4 (SM addr.)	=	TS32 - TS63
In CM address 80-BF:	D8-D4 (SM addr.)	=	TS6 - TS95
In CM address C0-FF:	D8-D4 (SM addr.)	=	TS96 - TS127

In space switch mode the leading edge of the SP pulse must be applied with the first bit of time slot 125. The input and output time-slot number must match.

Primary Access Configuration

Table 10
Time Slot and Line Programming for the Primary Access Configuration

2 Mbit/s input lines	Bit	D1	to	D0	Interface select in
	Bit	D3	to	D2	line number
	Bit	D8	to	D4	Time-slot number
	Bit	D9			Validity bit
4 Mbit/s input lines	Bit	D1	to	D0	Fixed to 01 (system interface)
	Bit	D2			Line numbers
	Bit	D8	to	D3	Time-slot number
	Bit	D9			Validity bit
8 Mbit/s input lines	Bit	D1	to	D0	Fixed to 01 (system interface)
	Bit	D8	to	D2	Line number
	Bit	D9			Validity bit
2 Mbit/s output lines	Bit	IA0			Interface select out
	Bit	IA2	to	IA1	Line number
	Bit	IA7	to	IA3	Time-slot number
4 Mit/s output lines	Bit	IA0			Fixed to 0 (system interface)
	Bit	IA1			Line number
	Bit	IA7	to	IA2	Time-slot number
8 Mbit/s output lines	Bit	IA0			Fixed to 0 (system interface)
	Bit	IA7	to	IA1	Time-slot number

The interface select bits have to be programmed as shown in the following table:

Table 11
Interface Selection Bits

	System Interface	Synchronous 2 MHz Interface
input lines	01	10
output lines	0	1

Configuration Register Access (CFR)

Access: read or write at indirect address FE_H

For a read access the bit 0 of the control byte must be set to logical 1 and for a write access to logical 0.

Value after power up or software reset: FF_H

DB 7							DB 0
1	1	1	1	1	1	CFS	CPS

CPS.. **C**lock **P**eriod **S**elect: device clock is set to 8192 kHz (logical 1) or 4096 kHz (logical 0)

CFS.. **C**on**F**iguration **S**elect: The PEx 2045 works in either the primary access configuration (logical 0) or in standard configuration (logical 1). Setting this bit to logical 1 resets the **CSR** to 00_H.

Clock Shift Register Access (CSR)

Access: read or write at indirect address FE_H

For a read access the bit 0 of the control byte has to be set to logical 1 and for a write access to logical 0.

The value after power up is 00_H

DB 7							DB 0
RS2	RS1	RS0	RRE	XS2	XS1	XS0	XFE

RS2..RS0.. **R**eceive clock **S**hift, bits 2-0. The received data stream is shifted in bit period steps as shown in **figure 9.**

RRE... **R**eceive with **R**ising **E**dge. The data is sampled with the falling (RRE = 0) or rising edge (RRE = 1) of the **data equivalent** clock. **(See figure 9).**

XS0..XS2.. **T**ransmit clock **S**hift, bits 2-0. The transmitted data stream is shifted as shown in **figure 9.**

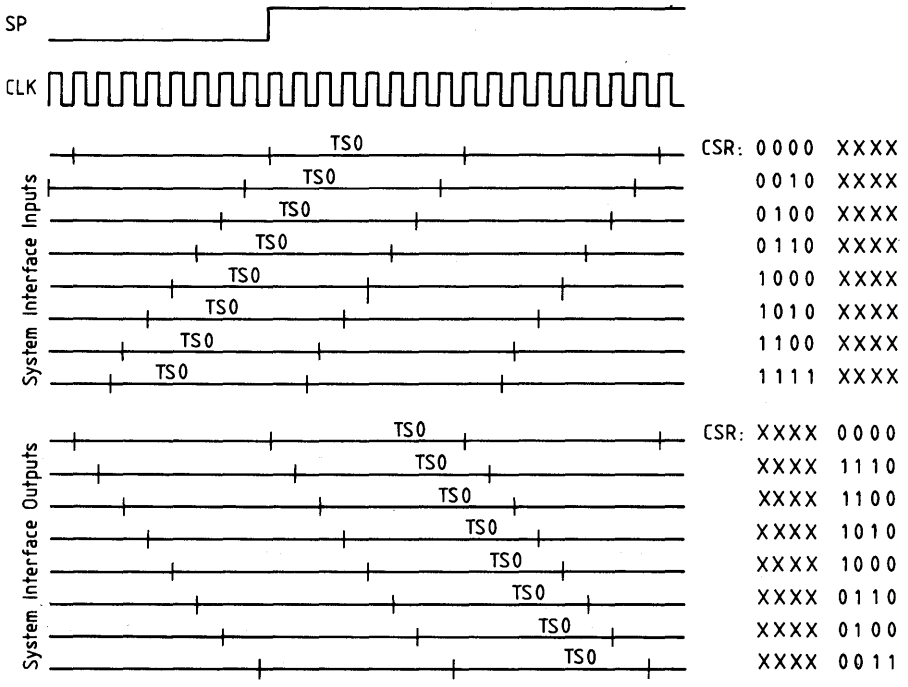
XFE... **T**ransmit with **F**alling **E**dge; data is transmitted with the rising (XFE = 0) or falling edge (XFE = 1) of the **device** clock.

Data stream manipulation according to these register entries only affects the system interface and only in the primary access configuration. The frame structure can be moved relative to the SP slope by up to seven clock periods in half clock period steps. This register can hold non-zero values only for a **CFR:CFS** value of logical 0. **Figure 9** illustrates the clock shifting facility.

Identical non-zero entries for RS2-RS0 and XS2-XS0 as well as identical RRE and XFE generate an output time-slot structure which is 1 time slot late relative to the input time-slot structure.

Identical 000 entries RS2-R0 and XS2-XS0 as well as RRE and XFE being logical 0 cause the input and output frames to coincide in time.

Figure 9
Clock Shifting



Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Ambient temperature under bias PEB 2045	T_A	0 to 70	°C
Storage temperature PEB 2045	T_{stg}	−65 to 125	°C
Ambient temperature under bias PEF 2045	T_A	−40 to 85	°C
Storage temperature PEF 2045	T_{stg}	−65 to 125	°C
Voltage on any pin with respect to ground	V_S	−0.4 to V_{DD} +0.4	V

DC Characteristics

Ambient temperature under bias range; $V_{DD} = 5\ V \pm 5\%$, $V_{SS} = 0\ V$.

Parameter	Symbol	Limit Values		Unit	Test Conditions
		min.	max.		
L-input voltage	V_{IL}	−0.4	0.8	V	
H-input voltage	V_{IH}	2.0	V_{DD}+0.4	V	
L-output voltage	V_{OL}		0.45	V	$I_{OL} = 2$ mA
H-output voltage H-output voltage	V_{OH} V_{OH}	2.4 −0.5		V V	$I_{OH} = -400\ \mu A$ $I_{OH} = -100\ \mu A$
Operational power supply current	I_{CC}		10	mA	$V_{DD} = 5$ V, inputs at 0 V or V_{DD}, no output loads
Input leakage current Output leakage current	I_{LI} I_{LO}		10	µA	$0V < V_{IN} < V_{DD}$ to 0V $0V < V_{OUT} < V_{DD}$ to 0V

Capacitances

$T_A = 25\ °C$, $V_{DD} = 5\ V \pm 5\%$, $V_{SS} = 0\ V$.

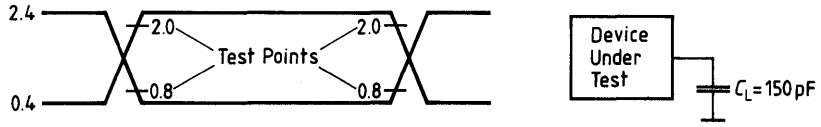
Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance	C_{IN}		10	pF
I/O capacitance	C_{IO}		20	pF
Output capacitance	C_{OUT}		15	pF

AC Characteristics

Ambient temperature under bias range, $V_{DD} = 5\ V \pm 5\%$

Inputs are driven at 2.4 V for a logical 1 and at 0.4 V for a logical 0. Timing measurements are made at 2.0 V for a logical 1 and at 0.8 V for a logical 0. The AC testing input/output waveforms are shown below.

Figure 10
I/O Waveform for AC Tests



µP Interface Timing

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Address stable before RD	t_{AR}	0		ns
Address hold after $\overline{RD}$	t_{RA}	0		ns
$\overline{RD}$ width	t_{RR}	90		ns
$\overline{RD}$ to data valid	t_{RD}		90	ns
Address stable to data valid	t_{AD}		90	ns
Data float after $\overline{RD}$	t_{DF}	5	25	ns
Read cycle time	t_{RCY}	160		ns
Address stable before $\overline{WR}$	t_{AW}	0		ns
Address hold time	t_{WA}	0		ns
$\overline{WR}$ width	t_{WW}	60		ns
Data setup time	t_{DW}	5		ns
Data hold time	t_{WD}	15		ns
Write cycle time	t_{WCY}	160		ns

Figure 11
µP Read Cycle

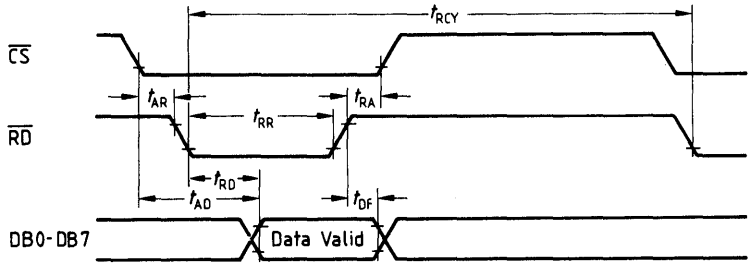
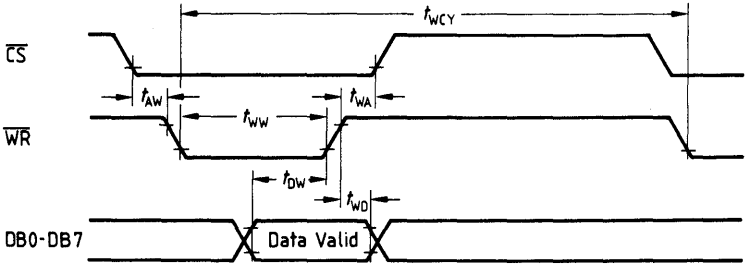


Figure 12
µP Write Cycle



PCM Interface Timing

Parameter	Symbol	Limit Values		Unit
		min.	max.	
PCM input setup	t_S	0		ns
PCM input hold	t_H	30		ns
PEB 2045 output delay	t_D		45	ns
PEF 2045 output delay	t_D		50	ns
PEB 2045 tristate delay	t_T		55	ns
PEF 2045 tristate delay	t_T		60	ns

Clock and Synchronization Timing

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Clock period 8 MHz high	$t_{CP8\,H}$	40		ns
Clock period 8 MHz low	$t_{CP8\,L}$	48		ns
Clock period 8 MHz	t_{CP8}	120		ns
Synchronization pulse setup 8 MHz	t_{SS8}	10	$t_{CP8}-20$	ns
Synchronization pulse delay 8 MHz	t_{SH8}	0	$t_{CP8}-20$	ns
Clock period 4 MHz high	$t_{CP4\,H}$	90		ns
Clock period 4 MHz low	$t_{CP4\,L}$	90		ns
Clock period 4 MHz	t_{CP4}	240		ns
Synchronization pulse setup 4 MHz	t_{SS4}	10	$t_{CP4}-30$	ns
Synchronization pulse delay 4 MHz	t_{SH4}	30	$t_{CP4}-10$	ns
Data clock delay	t_{DCD}		100	ns

Figure 13

PCM Line Timing in Standard Configuration with a 8-MHz-Device Clock

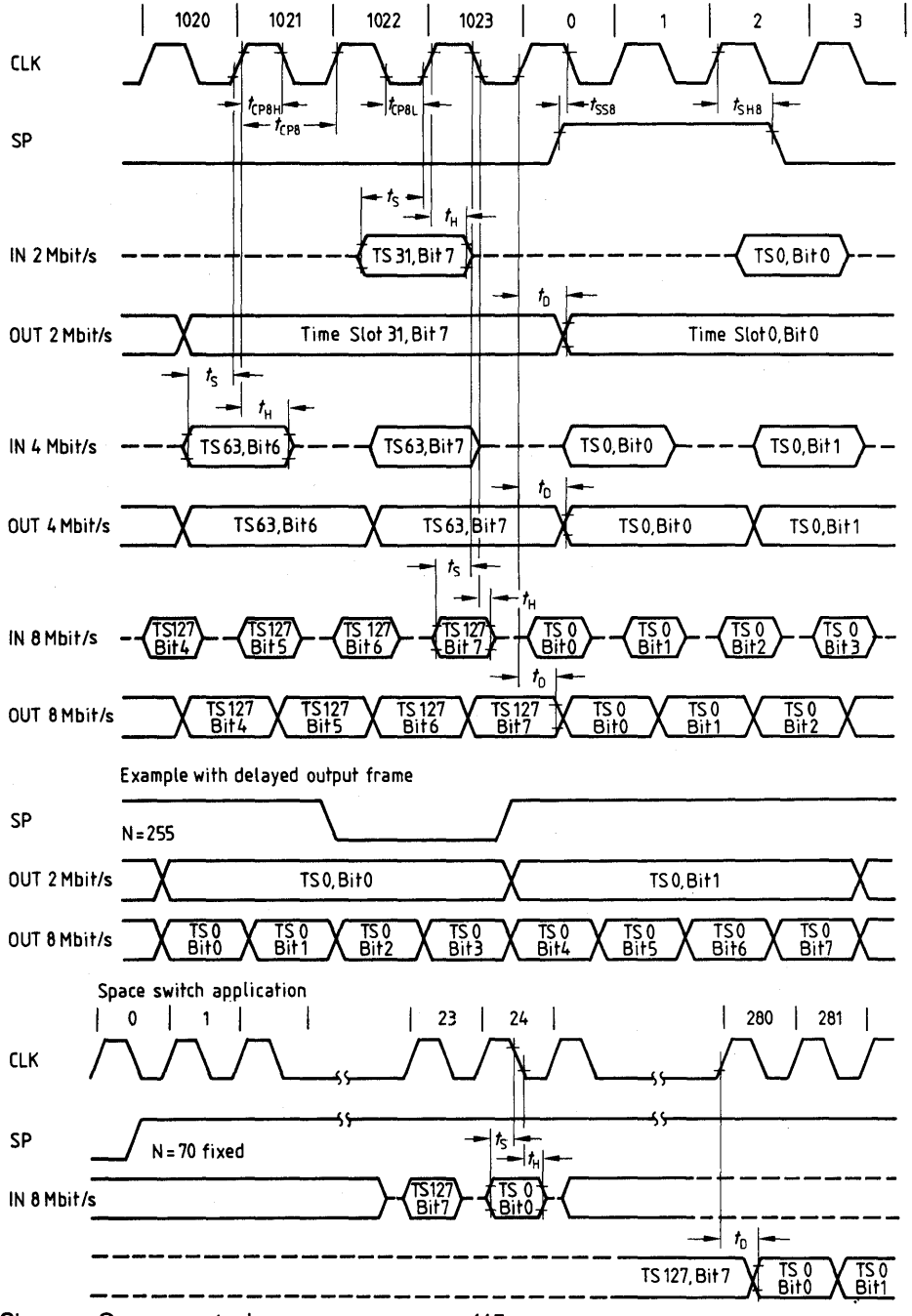


Figure 14

PCM Line Timing in Primary Access Configuration with a 8-MHz-Device Clock and a CSR Entry (00010001)

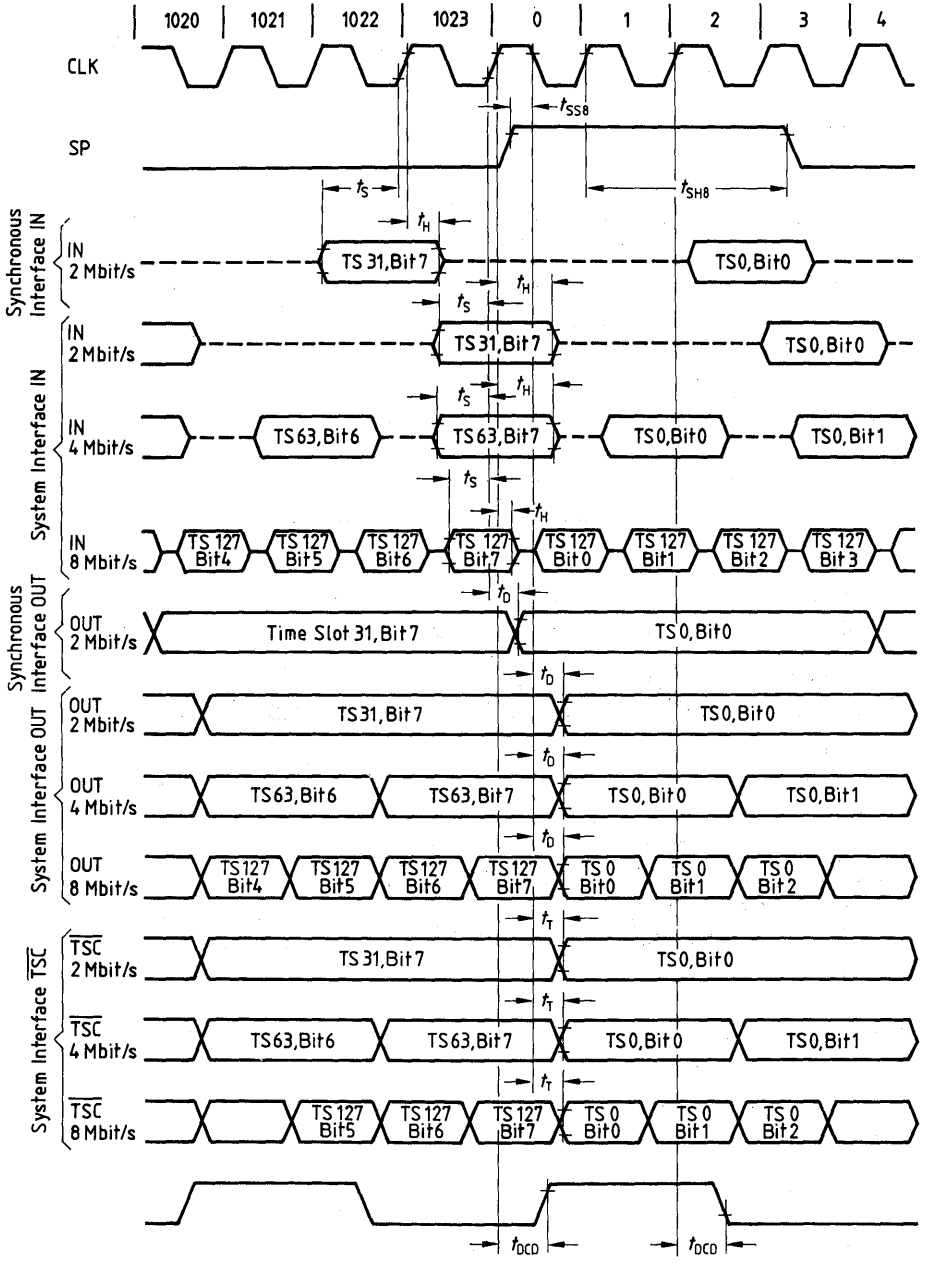


Figure 15

PCM Line Timing in Standard Configuration with a 4-MHz-Device Clock

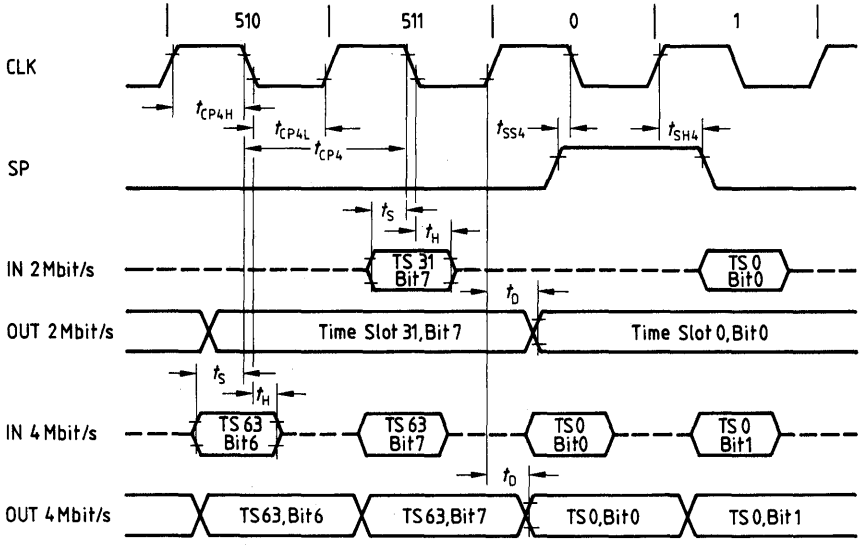


Figure 16

PCM Line Timing in Primary Access Configuration with a 4-MHz-Device Clock and a CSR Entry (00010001)

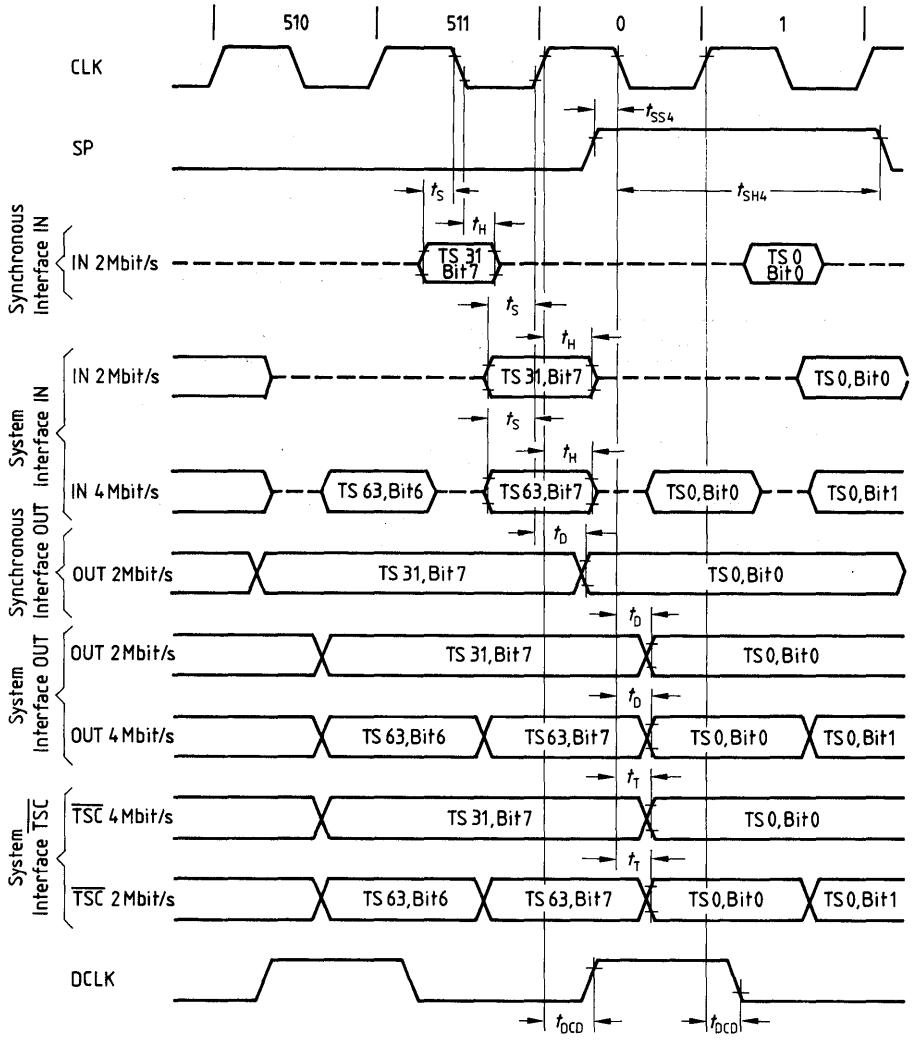


Table 12

Busy Times

Operation	Max. Value	Unit
Indirect register access	900	ns
Connection memory reset	250	µs

Memory Time Switch Small (MTSS)

PEB 2046
PEF 2046

Preliminary Data

CMOS IC

Type	Ordering Code	Package
PEB 2046 C	Q67100-H6103	C-DIP-40
PEB 2046 N	Q67100-H6104	PL-CC-44 (SMD)
PEB 2046 P	Q67100-H6105	P-DIP-40
PEF 2046 C	Q67100-H6106	C-DIP-40
PEF 2046 N	Q67100-H6107	PL-CC-40 (SMD)
PEF 2046 P	Q67100-H6108	P-DIP-40

The Siemens memory time switch PEx 2046 is a monolithic CMOS circuit connecting any of 256 incoming PCM channels to any of 256 outgoing PCM channels. The on-chip connection memory is accessed via the 8 bit µP interface.

The PEx 2046 is fabricated using the advanced CMOS technology from Siemens and is mounted in a C-DIP-40, P-DIP-40 or a PL-CC-44 package. Inputs and outputs are TTL-compatible.

The PEB 2046 works with either a 8192 kHz clock or a 4096 kHz clock. Henceforth, the respective clock periods are referred to as t_{CP8} and t_{CP4}.

The bits of a time slot are numbered 0 through 7. Bit 0 of a time slot is the first bit to be received or transmitted by the MTSC, bit 7 the last.

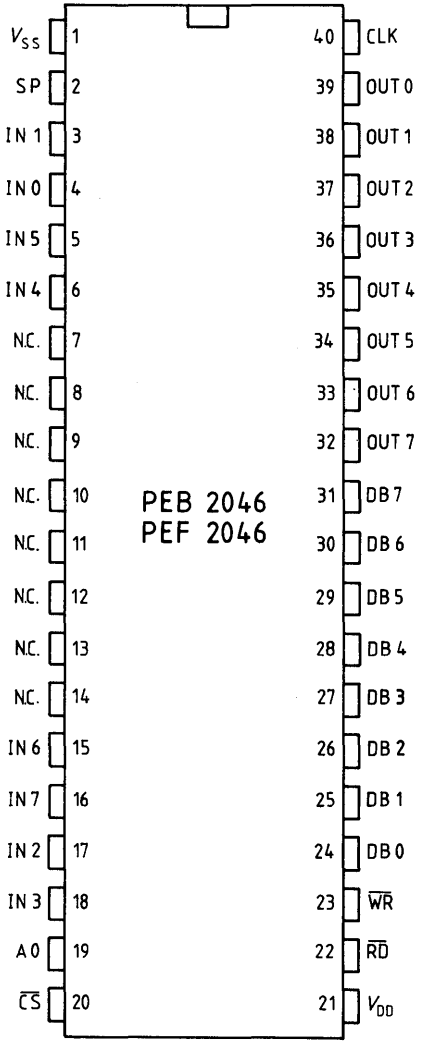
The components PEB 2046 and PEF 2046 are functionally identical. The difference between the two types lies in the temperature range. The PEB 2046 operates in the temperature range 0 to 70 °C, the PEF 2046 in the range −40 to +85 °C.

Features

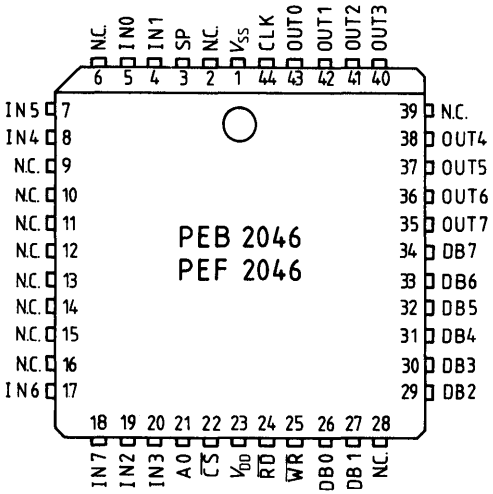
- Time/space switch for 2048 kbit/s PCM systems
- Switching of up to 256 incoming PCM channels to up to 256 outgoing PCM channels
- 8 input and 8 output PCM lines
- Configurable for a 4096 and 8192 kHz device clock
- Tristate function for further expansion and tandem operation
- 8 bit µP interface
- Single +5 V power supply
- Advanced low power CMOS technology

Pin Configuration
(top view)

P-DIP-40



PL-CC-44



Pin Definitions and Functions

P-DIP Pin No.	PL-CC Pin No.	Symbol	Input (I) Output (O)	Function
1	1	V_{SS}	I	**Ground** (0V)
2	3	SP	I	**Synchronization Pulse:** The PEx 2046 is synchronized relative to the PCM system via this line.
3	4	IN1	I	**PCM Input Ports:** Serial data is received at these lines at standard TTL levels.
4	5	IN0	I	
5	7	IN5	I	
6	8	IN4	I	
15	17	IN6	I	
16	18	IN7	I	
17	19	IN2	I	
18	20	IN3	I	
19	21	AO	I	**Address 0:** When high, the indirect register access mechanism is enabled. If A0 is logical 0 the mode and status registers can be written to and read respectively.
20	22	$\overline{CS}$	I	**Chip Select:** A low level selects the PEx 2046 for a register access operation.
21	23	V_{DD}	I	**Supply Voltage:** 5 V ± 5%.
22	24	$\overline{RD}$	I	**Read:** This signal indicates a read operation and is internally sampled only if $\overline{CS}$ is active. The MTSC puts data from the selected internal register on the data bus with the falling edge of $\overline{RD}$. $\overline{RD}$ is active low.
23	25	$\overline{WR}$	I	**Write:** This signal initiates a write operation. The $\overline{WR}$ input is internally sampled only if $\overline{CS}$ is active. In this case the MTSC loads an internal register with data from the data bus at the rising edge of $\overline{WR}$. $\overline{WR}$ is active low.
24	26	DB0	I/O	**Data Bus:** The data bus is used for communication between the MTSC and a processor.
25	27	DB1	I/O	
26	29	DB2	I/O	
27	30	DB3	I/O	
28	31	DB4	I/O	
29	32	DB5	I/O	
30	33	DB6	I/O	
31	34	DB7	I/O	

Pin Definitions and Functions (cont'd)

P-DIP Pin No.	PL-CC Pin No.	Symbol	Input (I) Output (O)	Function
32	35	OUT7	0	**PCM Output Port:** Serial data is sent by these lines at standard CMOS or TTL levels. These pins can be tristated.
33	36	OUT6	0	
34	37	OUT5	0	
35	38	OUT4	0	
36	40	OUT3	0	
37	41	OUT2	0	
38	42	OUT1	0	
39	43	OUT0	0	
40	44	CLK	I	**Clock:** 4096 or 8192 kHz device clock

Functional Description

The PEx 2046 is a memory time switch device. It can connect any of 256 PCM input channels to any of 256 output channels.

The input information of a complete frame is stored in the on-chip 2 kbit speech memory SM. **(see figure 1)**. The incoming 256 channels of 8 bits each are written in sequence into fixed positions in the SM. This is controlled by the input counter in the timing control block with a 8 kHz repetition rate.

For outputting, the connection memory (CM) is read in sequence. Each location in CM points to a location in the speech memory. The byte in this speech memory location is read into the current output time slot. The read access of the CM is controlled by the output counter which also resides in the timing control block.

Hence the CM needs to be programmed beforehand for the desired connection. The CM address corresponds to one particular output time slot and line number. The contents of this CM address points to a particular input time slot and line number (now resident in the SM).

Figure 1
Block Diagram of the PEx 2046

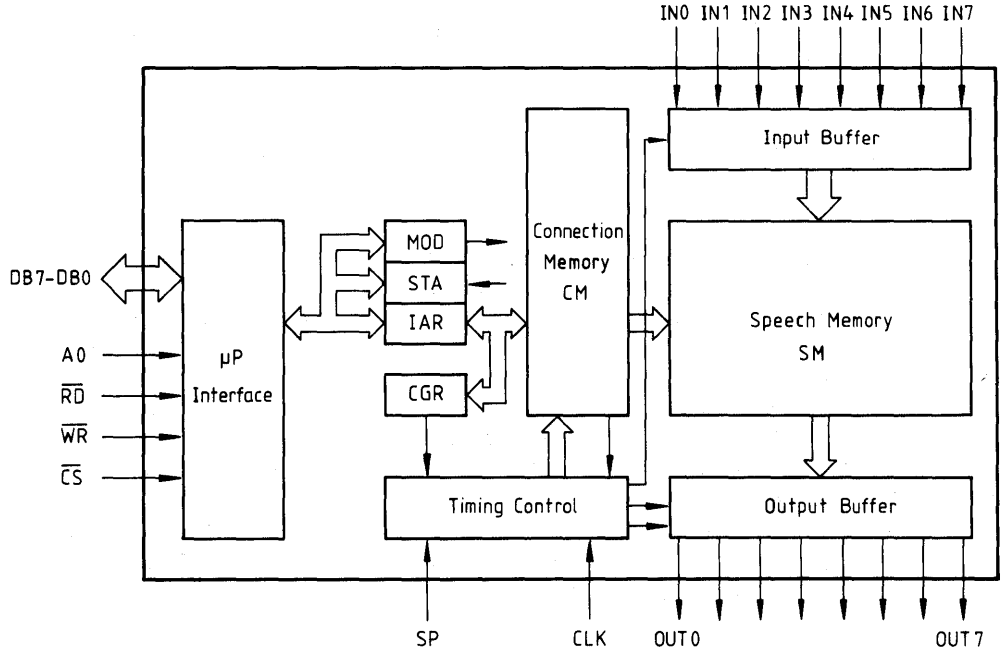
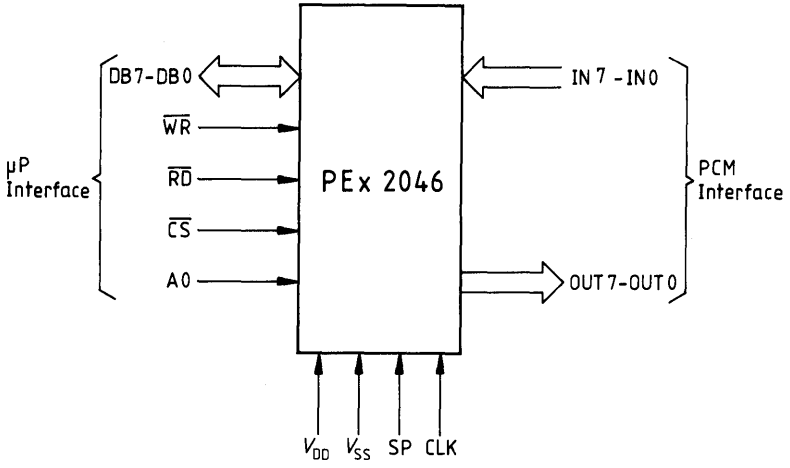


Figure 2
Functional Symbol for the Standard Configuration



Operational Description

Power Up

Upon power up the PEx 2046 is set to its initial state. The mode and configuration register bits are all set to logical 1. The status register **B**-bit is undefined, the **Z**-bit contains logical 0, the **R**-bit is undefined.

This state is also reached by pulling the $\overline{WR}$ and $\overline{RD}$ signals to logical 0 at the same time, (software reset). For the software the state of $\overline{CS}$ is of no significance.

Initialization Procedure

After power up a few internal signal and clocks need to be initialized. This is done with the initialization sequence. To give all signals and clocks a defined value the MTSC must encounter three falling and two rising edges of the SP signal. The resulting SP pulses may be of any length allowed in normal operation, the time interval between the two SP pulses may be of any length down to 250 nsec.

With all signals being defined, the CM needs to be reset. To do that a logical 0 is written into **MOD:RC. STA:B** is set. The resulting CM reset is finished after at most 250 µsec and is indicated by the status register **B**-bit being logical 0. Changing the pulse shaping factor N during CM reset may result in a CM reset time longer than 250 µs.

To prepare the PEx 2046 for programming the CM, the **RI**-bit in the mode register must be reset. Note that one mode register access can serve to reset both **RC** and **RI** bits as well as configuring to chip (i.e. selecting operating mode etc.).

Figure 3
Initializing the PEx 2046 for a 8192-kHz-Device Clock

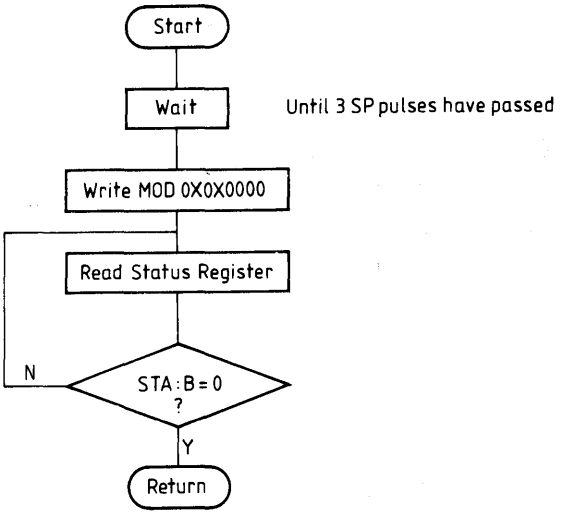
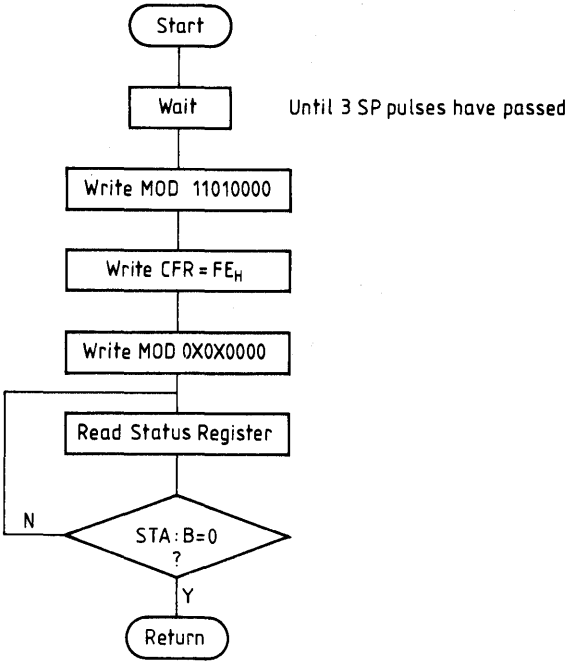


Figure 4
Initializing the PEx 2046 for a 4096-kHz-Device Clock



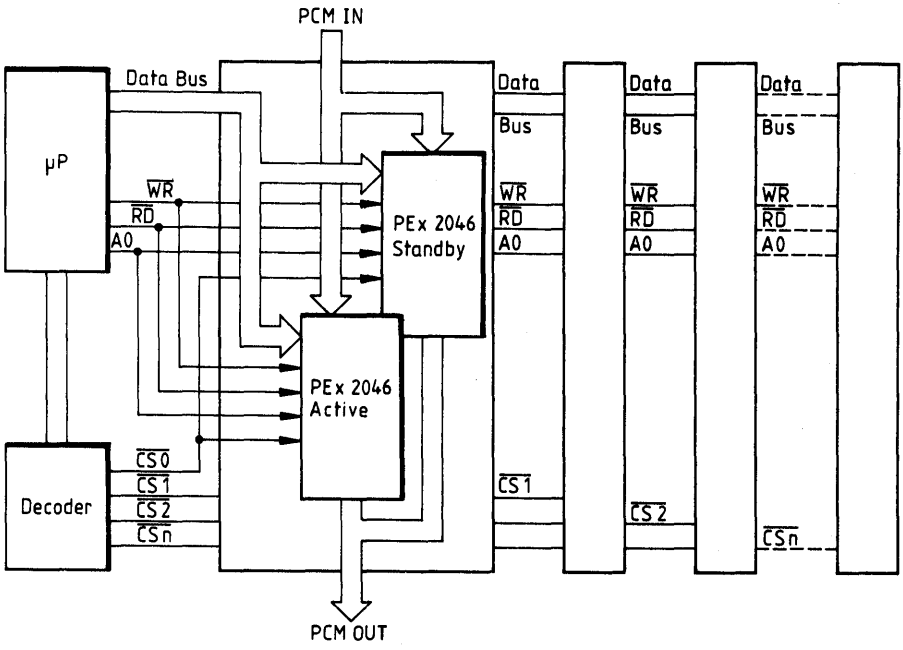
Operation with a 4096-kHz-Device Clock

In order for the MTSC to operate with a 4096-kHz-device clock the **CPS**-bit in the **CFR** register needs to be reset. This has to be done before the CM reset and needs up to 1.8 µs. Please keep in mind, **MOD:RI** has to be reset prior to performing an indirect register access. For a flow chart of this process refer to **figure 4.**

Standby Mode

With **MOD:SB** being logical 1 the PEx 2046 works as a backup device in redundant systems. It can be accessed via the µP interface and works internally like an active device. However, the outputs are high impedance. If the **SB**-bit is reset the outputs are switched to low impedance for the programmed active channels and this MTSC can take over from another device which has been recognized as being faulty. **See figure 5.**

Figure 5
Device Setup in Redundant Systems



Detailed Register Description

The following registers may be accessed:

Table 1
Addressing the Direct Registers

Address A0	Write Operation	Read Operation
0	MOD	STA
1	IAR	IAR

The chapters in this section cover the registers in detail.

Mode Register (MOD)

Access: write on address 0

DB 7							DB 0
RC	TE	RI	SB	MI1	MI0	MO1	MO0

Value after power up: FF_H

RC **R**eset **C**onnection memory; writing a zero to this bit causes the complete connection memory to be overwritten with 200_H (tristate). During this time **STA:B** is set. The maximum time for resetting the connection memory is 250 µs.

TE: **T**ristate **E**nable; this bit determines which tristating scheme is activated.

TE = 1: If the speech memory address written into the connection memory is S8 – S0 = 0, the output channel is tristated.

TE = 0: The S9 bit written into the connection memory is interpreted as a validity bit: S9 = 0 enables the programmed connection, S9 = 1 tristates the output.

Note: If TE = 1, time slot 0 of the logical input line 0 cannot be used for switching.

RI: **R**eset **I**ndirect access mechanism; setting this bit resets the indirect access mechanism. RI has to be cleared before writing/reading IAR after reset.

SB: **S**tand **B**y; by selecting SB = 1 all outputs are tristated. The connection memory works normally. The PEx 2045 can be activated immediately by resetting SB.

Table 2
Input and Output Pin Arrangement

Input Pin Arrangement

Pin-No. P-DIP	Pin-No. PL-CC	8x2 Mbit/s
3	4	IN 1
4	5	IN 0
5	7	IN 5
6	8	IN 4
15	17	IN 6
16	17	IN 7
17	19	IN 2
18	20	IN 3

Output Pin Arrangement

Pin-No. P-DIP	Pin-No. PL-CC	8x2 Mbit/s
32	35	OUT 7
33	36	OUT 6
34	37	OUT 5
35	38	OUT 4
36	40	OUT 3
37	41	OUT 2
38	42	OUT 1
39	43	OUT 0

Status Register (STA)

Access: read at address 0

DB 7							DB 0
B	Z	R	0	0	0	0	0

B **B**usy: the chip is busy resetting the connection memory (B = 1). B is undefined after power up and logical 0 after the device initialization.

Note: The maximum time for resetting the connection memory is 250 µs.

Z incomplete instruction; a three byte indirect instruction is not completed (Z = 1). Z is 0 after power up.

Note: Z is reset and the indirect access is cancelled by setting **MOD:RI** or resetting **MOD:RC**

R initialization **R**equest. The connection memory has to be reset due to loss of data (R = 1). The R bit is set after power failure or inappropriate clocking and reset when the connection memory reset is finished. R is undefined after power up and logical 0 after the device initialization.

Indirect Access Register (IAR)

(Read or Write Operation with Address A0 = 1)

An indirect access is performed by reading/writing three consecutive bytes (first byte = control byte, second byte = data byte, third byte = address byte) to/from IAR. The structure is shown in **table 3.**

Table 3

The 3 Bytes of the Indirect Access

Bit 7							Bit 0	
0	0	K1	K0	0	0	C1	C0	Control Byte
D7	D6	D5	D4	D3	D2	D1	D0	Data Byte
IA7	IA6	IA5	IA4	IA3	IA2	IA1	IA0	Address Byte

The control byte bits K1, K0, C1 and C0 together with the address byte determine the type of access being performed according to **table 4.**

Table 4

Encoding the Different Types of Indirect Accesses

K1	K0	C1	C0	Address Byte	Type of Access	
0	0	D9	D8	CM-Address	Read	CM
1	0	D9	D8	CM-Address	Write	CM
0	1	D9	D8	CM-Address	Write	CM
1	1	0	0	FE_H	Write	CFR
1	1	0	1	FE_H	Read	CFR

Connection Memory Access

For a connection memory access the control byte bits C1 and C0 contain the data bits D9 and D8, respectively. D9 is the validity bit which together with D8 and the data byte D7-D0 is written to the CM address IA7-IA0.

The function of the validity bit is controlled by **STA:TE**. D8-D0 and IA7-IA0 contain the information for the logical line and time-slot numbers of the programmed connection, D8-D0 for the inputs, IA7-IA0 for the outputs. **Table 5** shows the programming of these bits.

Standard Configuration

Table 5
Time Slot and Line Programming

2 Mbit/s input lines	Bit	D3	to	D0	Logical line number
	Bit	D8	to	D4	Time slot number
	Bit	D9			Valididy bit
2 Mbit/s output lines	Bit	IA2	to	IA0	Line number
	Bit	IA7	to	IA0	Time slot number

Configuration Register Access (CFR)

Access: read or write at indirect address FE_H

For a read access the bit 0 of the control byte must be set to logical 1 and for a write access to logical 0.

Value after power up or software reset: FF_H

DB 7							DB 0
1	1	1	1	1	1	1	CPS

CPS.. **C**lock **P**eriod **S**elect: device clock is set to 8192 kHz (logical 1) or 4096 kHz (logical 0)

Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Ambient temperature under bias PEB 2046	T_A	0 to 70	°C
Storage temperature PEB 2046	T_{stg}	−65 to 125	°C
Ambient temperature under bias PEF 2046	T_A	−40 to 85	°C
Storage temperature PEF 2046	T_{stg}	−65 to 125	°C
Voltage on any pin with respect to ground	V_S	−0.4 to V_{DD} +0.4	V

DC Characteristics

Ambient temperature under bias range; $V_{DD} = 5\ V \pm 5\%$, $V_{SS} = 0\ V$.

Parameter	Symbol	Limit Values		Unit	Test Conditions
		min.	max.		
L-input voltage	V_{IL}	−0.4	0.8	V	
H-input voltage	V_{IH}	2.0	V_{DD} +0.4	V	
L-output voltage	V_{OL}		0.45	V	$I_{OL} = 2$ mA
H-output voltage H-output voltage	V_{OH} V_{OH}	2.4 V_{DD} −0.5		V V	$I_{OH} = -400\ \mu A$ $I_{OH} = -100\ \mu A$
Operational power supply current	I_{CC}		10	mA	$V_{DD} = 5$ V, inputs at 0 V or V_{DD}, no output loads.
Input leakage current Output leakage current	I_{LI} I_{LO}		10	µA	$0\ V < V_{IN} < V_{DD}$ to 0 V $0\ V < V_{OUT} < V_{DD}$ to 0 V

Capacitances

$T_A = 25\,°C$, $V_{DD} = 5\ V \pm 5\%$, $V_{SS} = 0\ V$.

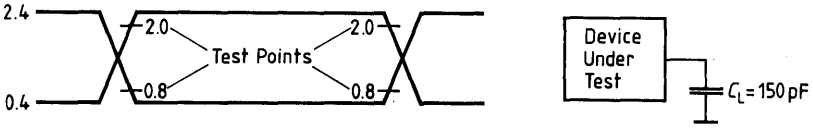
Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance	C_{IN}		10	pF
I/O capacitance	C_{IO}		20	pF
Output capacitance	C_{OUT}		15	pF

AC Characteristics

Ambient temperature under bias range, $V_{DD} = 5\ V \pm 5\%$

Inputs are driven at 2.4 V for a logical 1 and at 0.4 V for a logical 0. Timing measurements are made at 2.0 V for a logical 1 and at 0.8 V for a logical 0. The AC testing input/output waveforms are shown below.

Figure 5
I/O Waveform for AC Tests



µP Interface Timing

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Address stable before $\overline{RD}$	t_{AR}	0		ns
Address hold after $\overline{RD}$	t_{RA}	0		ns
$\overline{RD}$ width	t_{RR}	90		ns
$\overline{RD}$ to data valid	t_{RD}		90	ns
Address stable to data valid	t_{AD}		90	ns
Data float after $\overline{RD}$	t_{DF}	5	25	ns
Read cycle time	t_{RCY}	160		ns
Address stable before $\overline{WR}$	t_{AW}	0		ns
Address hold time	t_{WA}	0		ns
$\overline{WR}$ width	t_{WW}	60		ns
Data setup time	t_{DW}	5		ns
Data hold time	t_{WD}	15		ns
Write cycle time	t_{WCY}	160		ns

Figure 6
µP Read Cycle

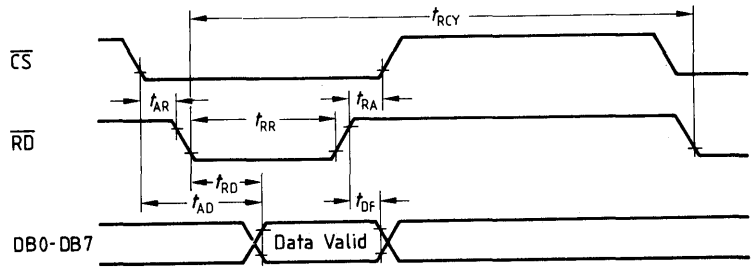
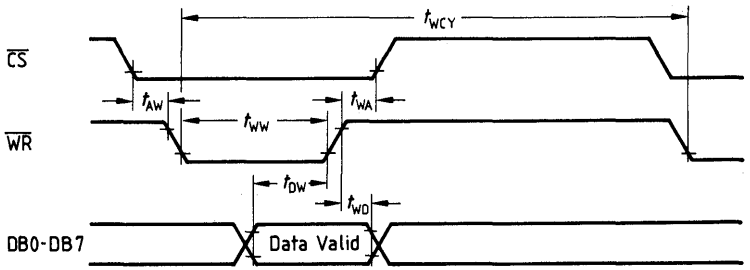


Figure 7
µP Write Cycle



PCM Interface Timing

Parameter	Symbol	Limit Values		Unit
		min.	max.	
PCM input setup	t_S	0		ns
PCM input hold	t_H	30		ns
PEB 2046 output delay	t_D		45	ns
PEF 2046 output delay	t_D		50	ns

Clock and Synchronization Timing

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Clock period 8 MHz high	t_{CP8H}	40		ns
Clock period 8 MHz low	t_{CP8L}	48		ns
Clock period 8 MHz	t_{CP8}	120		ns
Synchronization pulse setup 8 MHz	t_{SS8}	10	$t_{CP8}-20$	ns
Synchronization pulse delay 8 MHz	t_{SH8}	0	$t_{CP8}-20$	ns
Clock period 4 MHz high	t_{CP4H}	90		ns
Clock period 4 MHz low	t_{CP4L}	90		ns
Clock period 4 MHz	t_{CP4}	240		ns
Synchronization pulse setup 4 MHz	t_{SS4}	10	$t_{CP4}-30$	ns
Synchronization pulse delay 4 MHz	t_{SH4}	30	$t_{CP4}-10$	ns

Figure 8
PCM Line Timing with a 8-MHz-Device Clock

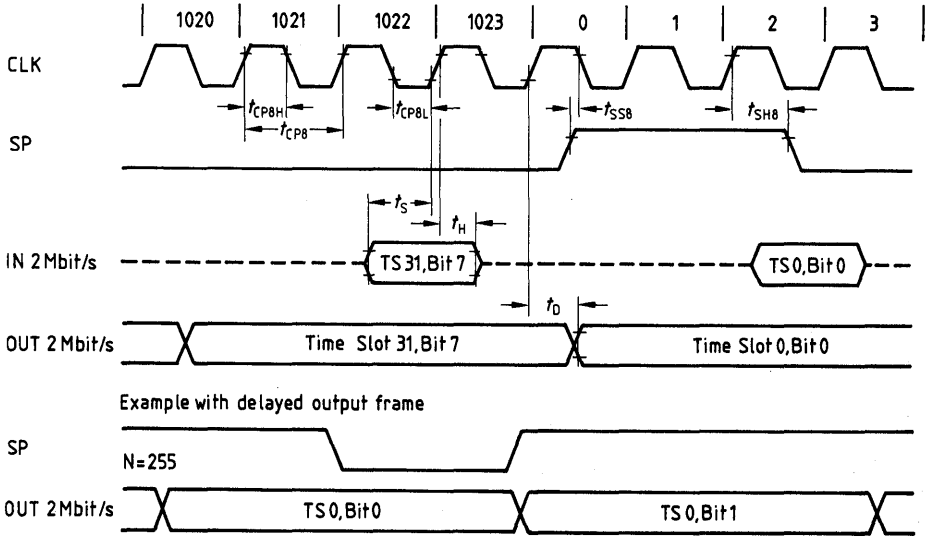
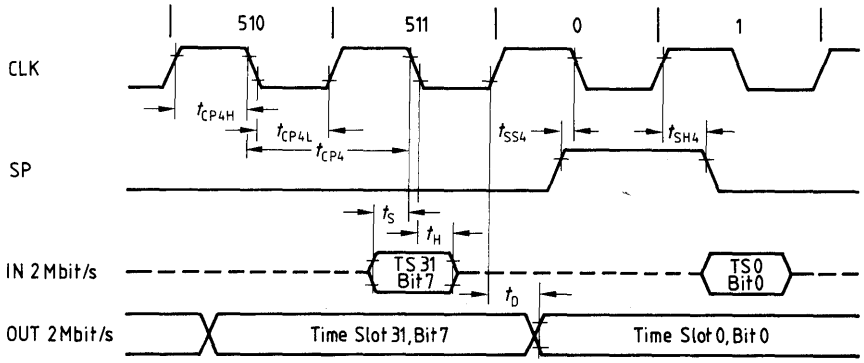


Figure 9
PCM Line Timing with a 4-MHz Device Clock



Busy Time

Table 6
Busy Time

Operation	Max. Values	Unit
Indirect register access	900	ns
Connection memory reset	250	µs

Peripheral Board Controller (PBC) PEB 2050

Preliminary Data **MOS IC**

Type	Ordering Code	Package
PEB 2050-C	Q67100-Z157	C-DIP-40
PEB 2050-N	Q67100-H8392	PL-CC-44 (SMD)
PEB 2050-P	Q67100-H3022	P-DIP-40

The peripheral board controller PEB 2050 is a device for the control of voice, data, and signaling paths of up to 16 subscribers on peripheral component boards in digital telephone systems. In combination with the highly flexible Signal Processing Codec Filter (SICOFI® PEB 2060) it forms an optimized analog subscriber-line board architecture. Its flexibility allows operation as general-purpose controller for data switching and MUX/ De MUX applications.

The PBC controls space and time switching functions between subscriber-line devices and time-division multiplex highways. Further, it controls the flow of information between the subscriber interface ports and a processor which can be an optional line card local processor or the central processor directly. Last, it performs all protocol control functions, using the HDLC protocol format for all information passing between the line card and the central processor via a dedicated HDLC line or via interleaved time slots on the PCM lines.

To meet the different requirements the PBC PEB 2050 provides the following interfaces:

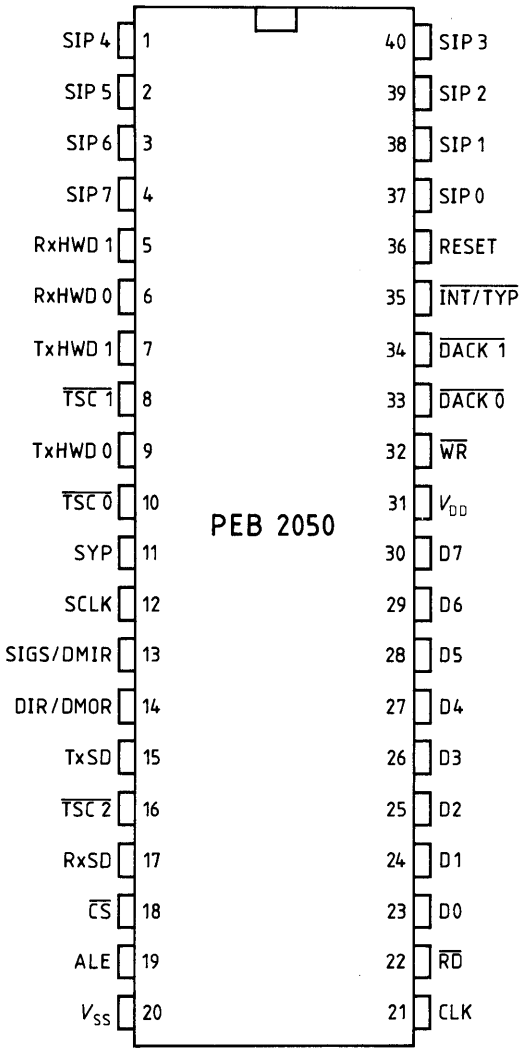
- 8 serial, bidirectional I/O ports for the transfer of voice, data, control, and signaling information between the PBC and codec filters (e.g. SICOFI PEB 2060), digital interface circuits or signal processors
- Double-constructed PCM interface
- Fast serial communication link to the central processor
- Bit-parallel interface for the connection of 8-bit standard microcomputers such as the SAB 8051. The interface is characterized by an interrupt control and two independent DMA channels, one for the transmit and one for the receive direction.

Features

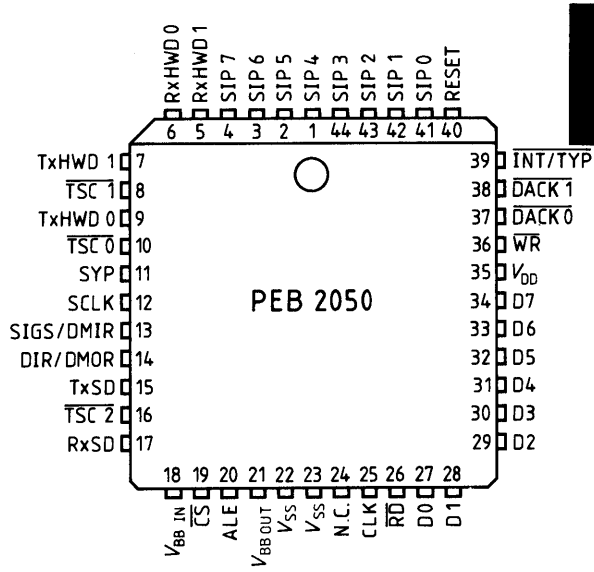
- Board controller for up to 16 subscribers of a digital switching system
- Designed for different PCM systems
- Time-slot assignment freely programmable for all subscribers connected
- Control of voice, data, signaling and line board parameters to minimize hardware requirements and to simplify software
- Provides two full duplex PCM highways for the system interface
- System control uses the HDLC protocol with X.25 level 2 functions performed by the PBC
- Standard µP interface
- Two DMA channels for expansion of internal buffer capability of 16 bytes per direction
- µP access to all internal data streams including time-slot oriented data streams
- Support of subscriber circuits by generating timing signals
- Single +5 V power supply
- Low power consumption

Pin Configuration
(top view)

P-DIP-40
C-DIP-40



PL-CC-44



$V_{BB\ IN}$ and $V_{BB\ OUT}$ Have to be Short Circuited.

Pin Definitions and Functions

Pin No. PL-CC	Pin No. P-DIP	Symbol	Name	Function
1 4	1 4	SIP 4 . . . . SIP 7	Subscriber interface port (input/output)	These interface ports are used for bi-directional, bit-serial transfer of speech, data and control words to and from the signal processing codec Filter (SICOFI) or standard codec. Corresponding with the direction signal, the PBC PEB 2050 is transmitting during the high level of DIR within the first half of a 125 µs frame.
5	5	RxHWD 1	Receive highway data (input)	Receive PCM highway 1 interface.
6	6	RxHWD 0	Receive highway data (input)	Receive PCM highway 0 interface. The PBC serially receives a PCM word (8 bits) through one of these leads at the programmed time slot.
7	7	TxHWD 1	Transmit highway data (output)	Output of the transmit side onto the send PCM highway 1 (serial bus). The 8-bit PCM word is serially sent out on this pin at the programmed time slot. Tristate output.
8	8	$\overline{\text{TSC 1}}$	Tristate control (output, active low)	Normally high, this signal goes low while the PBC is transmitting an 8-bit PCM word on the PCM highway 1.
9	9	TxHWD 0	Transmit highway data (output)	Output of the transmit side onto the send PCM highway 0.
10	10	$\overline{\text{TSC 0}}$	Tristate control (output, active low)	Tristate control of highway 0.
11	11	SYP	Synchronization	SYP is a frame synchronization pulse which resets the on-chip time-slot counters.
12	12	SCLK	Slave clock (output)	Clock output for the peripheral devices. The signals between the codec filter and the PBC are latched and transmitted with the rising edge of SCLK.
13	13	SIGS/DMIR	Signal strobe (output, active high)/ direct memory input request (output, active high)	The SIGS output supplies a programmable strobe signal. In the DMA mode, this pin is used as DMA input request.

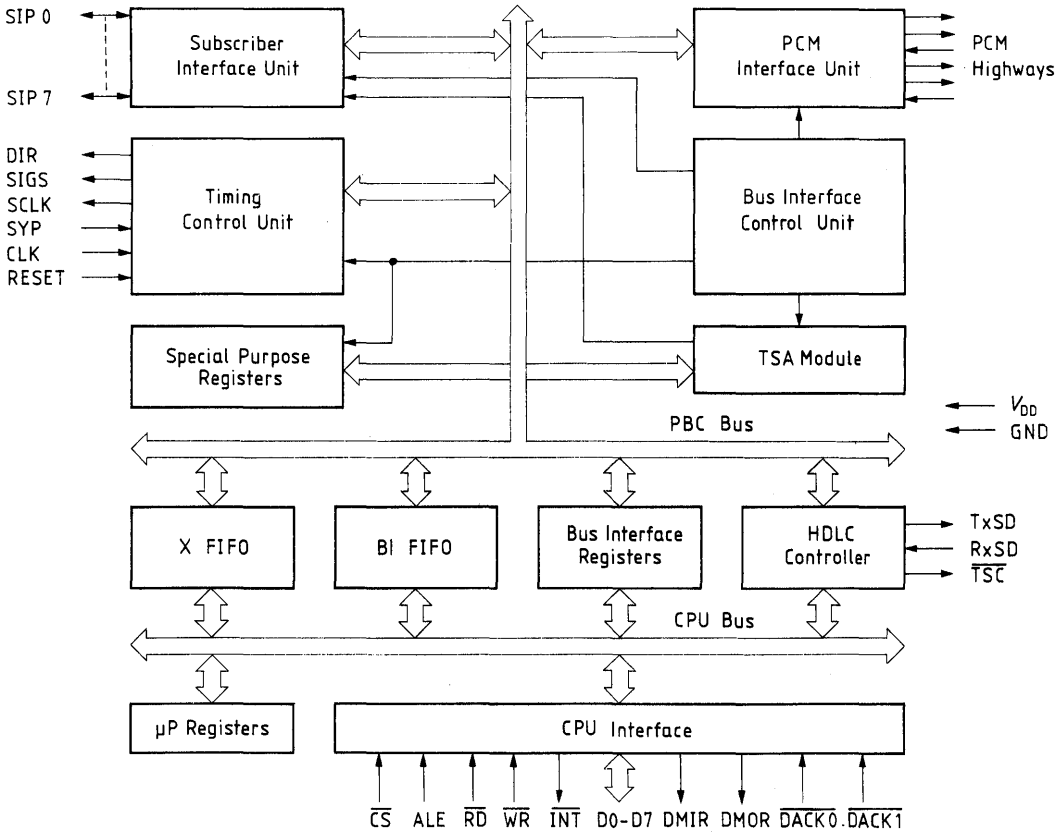
Pin Definitions and Functions (cont'd)

Pin No. PL-CC	Pin No. P-DIP	Symbol	Name	Function
14	14	DIR/DMOR	Direction (output, active high)/direct memory output request (output, active high)	DIR is an 8-kHz symmetric frame signal which controls the direction of data transfer from and to the peripheral devices. The PBC is able to receive data during the low state of DIR. In the DMA mode this pin is used as DMA output request. DMIR and DMOR are generated by the PBC-internal HDLC receiver or transmitter and are used for handshaking during the DMA transfer.
15	15	TxSD	Transmit signaling data (output)	This line transmits the serial data to the dedicated HDLC channel.
16	16	$\overline{TSC\,2}$	Tristate control to 2 (output, active low)	Normally high, this signal goes low while the PBC is transmitting an HDLC message.
17	17	RxSD	Receive signaling data (input)	This line receives the serial data from the HDLC channel.
19	18	$\overline{CS}$	Chip select (input, active low)	$\overline{CS}$ is used to address the PBC. A low level at this input enables the PBC to accept commands or data from a µP within a write cycle, or to transmit data during a read cycle.
20	19	ALE	Address latch enable (input, active high)	A high level at this input indicates that the data on the external bus is an address selecting one of the PBC-internal sources or destinations. Latching into the address latch occurs during the high-low transition.
22	20	V_{SS}		Ground (0 V)
25	21	CLK	Clock (input)	A standard TTL clock provides the basic timing of the controller. The clock is synchronous to the PCM clock.
26	22	$\overline{RD}$	Read strobe (input, active low)	$\overline{RD}$ is used together with $\overline{CS}$ to transfer data from the PBC to a µP or memory.

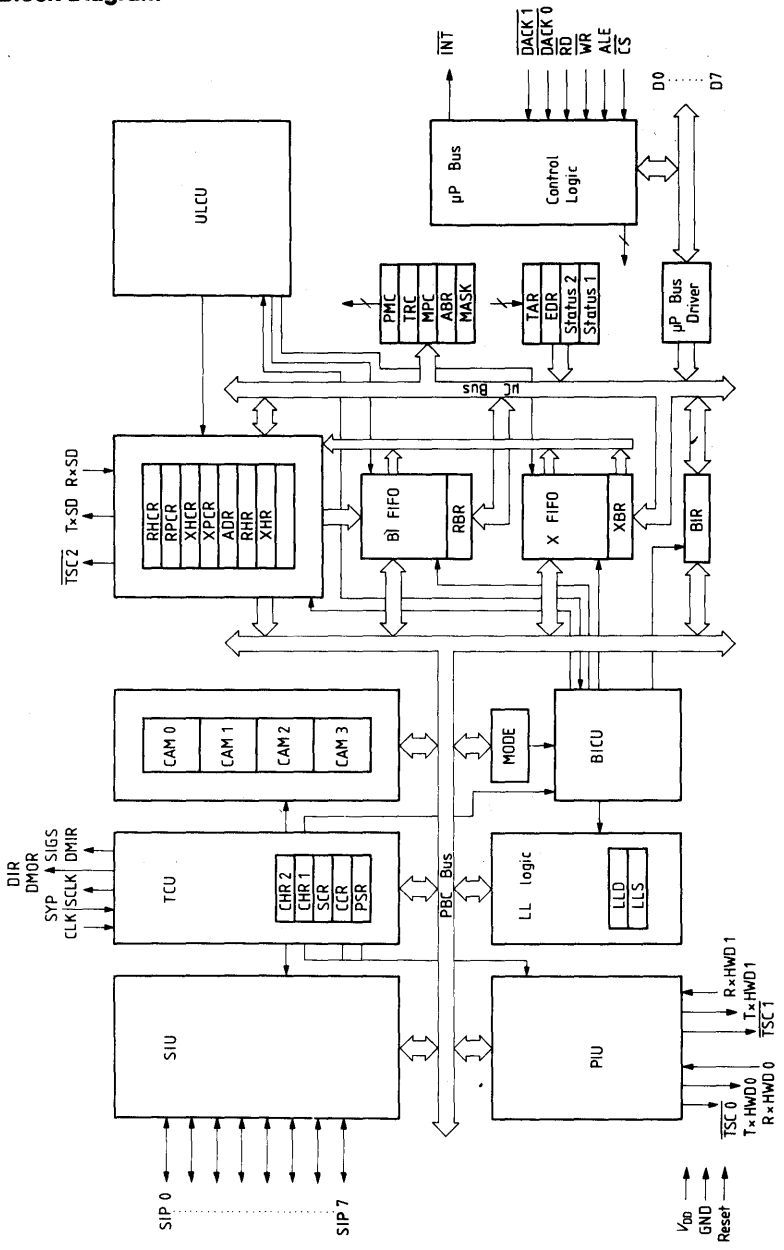
Pin Definitions and Functions (cont'd)

Pin No. PL-CC	Pin No. P-DIP	Symbol	Name	Function
27 34	23 30	D0 . . . . . D7	System data bus	The data bus transfers data and commands between the µP or memory and the PBC.
35	31	V_{DD}		Power supply: $V_{DD} = 5.0 \pm 0.25$ V
36	32	$\overline{WR}$	Write strobe (input, active low)	During the low state of $\overline{WR}$ data can be transferred from the µP or memory to the PBC.
37 38	33 34	$\overline{DACK\ 0}$ $\overline{DACK\ 1}$	DMA acknowledge (inputs, active low)	$\overline{DACK\ 0}$ and $\overline{DACK\ 1}$ are used to acknowledge the DMA output and DMA input request, respectively.
39	35	$\overline{INT/TYP}$	Interrupt request (output, active low)	The signal is pulled down, when the PBC is requesting an interrupt. In that case, the µP should enter an interrupt routine for reading status register 1.
40	36	RESET	Reset (input, active high)	A high on this input forces the PBC into reset state. The minimum reset pulse is 16 complete clock cycles.
41 33	37 40	SIP 0 . . . . . SIP 3		These interface ports are used for bi-directional, bit-serial transfer of speech, data and control words to and from the signal processing codec filter (SICOFI) or standard codec. Corresponding with the direction signal, the PBC PEB 2050 is transmitting during the high level of DIR within the first half of a 125 µs frame.

Block Diagram



Block Diagram



Description of the Functional Blocks

The PBC has been designed especially for use in peripheral subscriber boards, but its functional flexibility also permits its application in various parts of a digital exchange telecommunications system.

Used in peripheral subscriber boards it performs two essential functions:

1) Exchange of control data between a central processing unit, an on-board processing unit and individual subscriber connections. The PBC supports the ISO/CCITT's HDLC communication-line protocol. An application-specific, PBC-internal controller controls the distribution of data on the board.
2) The time-slot controlled transfer of PCM data (64 Kbaud channels) between the PCM highways and the subscriber connections.

Data transfer between both parts, such as signaling through PCM highways (common channel) or the access of the on-board µP to 64 Kbaud channels, are considerably simplified by the IC.

The two central functional blocks are reflected in the circuit structure: The PCM synchronous portion constitutes the interfaces to the subscribers and the PCM highways. It comprises the following functional blocks:

- SIU (Serial Interface Unit) with last look logic
- PIU (PCM Interface Unit)
- CAM (Contents-Addressable Memory)
- TCU (Timing Control Unit)
- MODE register
- PBC bus

The asynchronous portion constitutes the interface to the local microprocessor (8-bit parallel). and to the central control (serial HDLC interface) and comprises the following functional blocks:

- HDLC controller
- µP interface
- µP control and status register
- ULCU (User Level Control Unit)

The two portions are interconnected by the following functional blocks:

- X FIFO (Transmit FIFO)
- Bidirectional FIFO
- BICU (Bus Interface Control Unit)
- BIR (Bus Interface Register)

Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Storage temperature	T_{stg}	−65	125	°C

Range of Operation

Operating temperature	T_A	0	70	°C
Voltage at any pin referred to ground	V_S	−0.5	7	V
Total power consumption	P_{tot}		625	mW

DC Characteristics

$T_A = 0$ to 70 °C; $V_{CC} = 5\ V \pm 0.25\ V$; GND = 0 V

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
L-input voltage	V_{IL}	−0.5		0.8	V
H-input voltage	V_{IH}	2.0		5.5	V
L-output voltage $I_{OL} = +1.6$ mA	V_{OL}			0.45	V
H-output voltage $I_{OH} = -400\ \mu A$	V_{OH}	2.4			V
Input leakage current $V_{IN} = V_{CC}$ to 0 V	I_{IL}	−10		10	µA
Output leakage current $V_{OUT} = V_{CC}$ to 0 V	I_{OL}	−10		10	µA
V_{CC} supply current $V_{CC} = 5$ V	I_{CC}		70	125	mA

Capacitance

$T_A = 25\,°C$; $V_{CC} = GND = 0\,V$

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Input capacitance $f_C = 1$ MHz	C_{IN}		5	10	pF
Input/output capacitance	$C_{I/O}$		10	20	pF
Output capacitance unmeasured pins returned to GND	C_{OUT}		8	15	pF

AC Characteristics

$T_A = 0$ to $70\,°C$; $V_{CC} = 5\,V \pm 0.25\,V$; $GND = 0\,V$

Microprocessor Interface

Read Cycle

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Address hold after ALE	t_{LA}	20		ns
Address to ALE setup	t_{AL}	30		ns
Data delay from $\overline{RD}$	t_{RD}		150	ns
$\overline{RD}$ pulse width	t_{RR}	150	10^7	ns
Output float delay	t_{DF}		25	ns
$\overline{RD}$ control interval case 1[1])	t_{RI}	2 x CP		ns
$\overline{RD}$ control interval case 2[2])	t_{RI}	100		ns
ALE pulse width	t_{AA}	60		ns

Write Cycle

$\overline{WR}$ pulse width	t_{WW}	100		ns
Data setup to $\overline{WR}$	t_{DW}	50		ns
Data hold after $\overline{WR}$	t_{WD}	25		ns
$\overline{WR}$ control interval case 1[1])	t_{WI}	2 x CP		ns
$\overline{WR}$ control interval case 2[2])	t_{WI}	50		ns

[1]) Case 1: read, write of BI FIFO and X FIFO
[2]) Case 2: all other registers

DMA Read

Parameter	Symbol	Limit Values		Unit
		min.	max.	
DMA read time*)	t_{DMA}		7 x CP	ns
DMOR hold time	t_{DH}		75	ns
Address stable before $\overline{RD}$	t_{AR}	0		ns
Data delay from $\overline{RD}$	t_{RD}		150	ns
Output floating delay	t_{DF}		25	ns
Address hold after $\overline{RD}$	t_{RA}	0		ns
$\overline{RD}$ pulse width	t_{RR}	150	10^4	ns

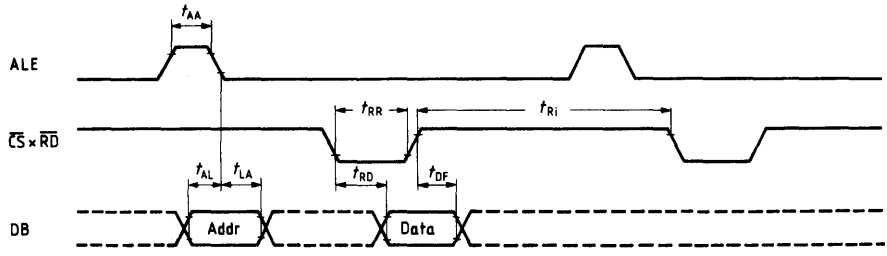
DMA Write

DMA write time*)	t_{DMA}		7 x CP	ns
DMSIR hold time	t_{IH}		90	ns
Address stable before $\overline{WR}$	t_{AW}	0		ns
Address hold after $\overline{WR}$	t_{WA}	0		ns
Data setup to $\overline{WR}$	t_{DW}	50		ns
Data hold after $\overline{WR}$	t_{WD}	25		ns
$\overline{WR}$ pulse width	t_{WW}	100		ns

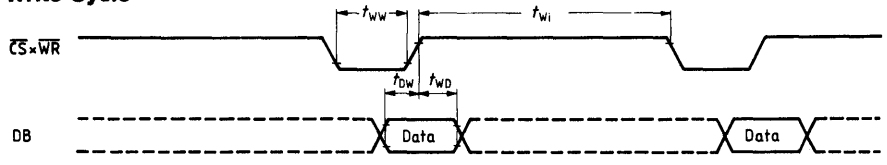
*)

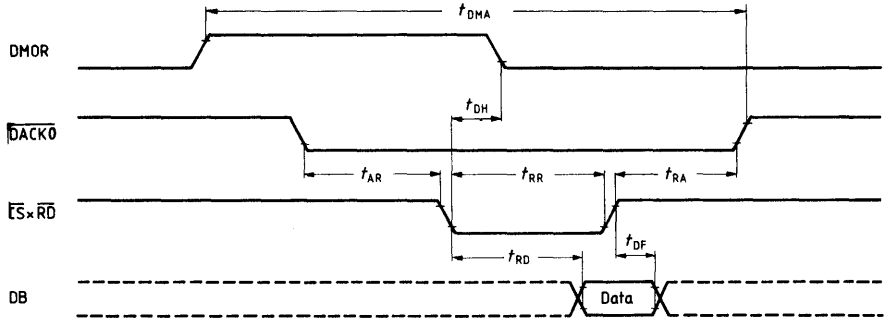
PBC clock/MHz	2.048	4.096	1.536	3.072
2 x CP/ns	980	490	1300	650
7 x CP/µs	3.4	1.7	4.56	2.3

Read Cycle

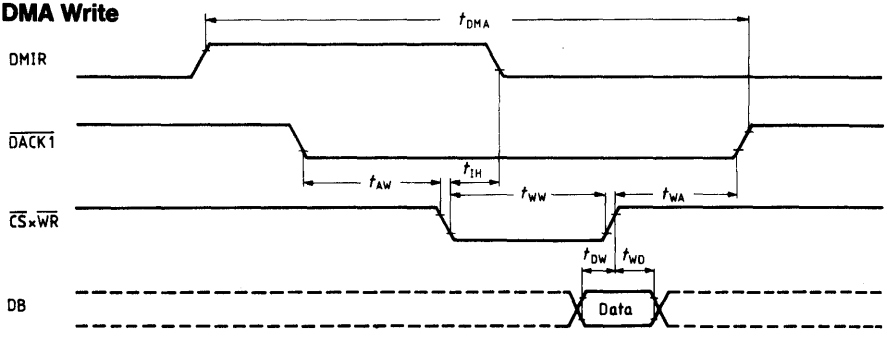


Write Cycle





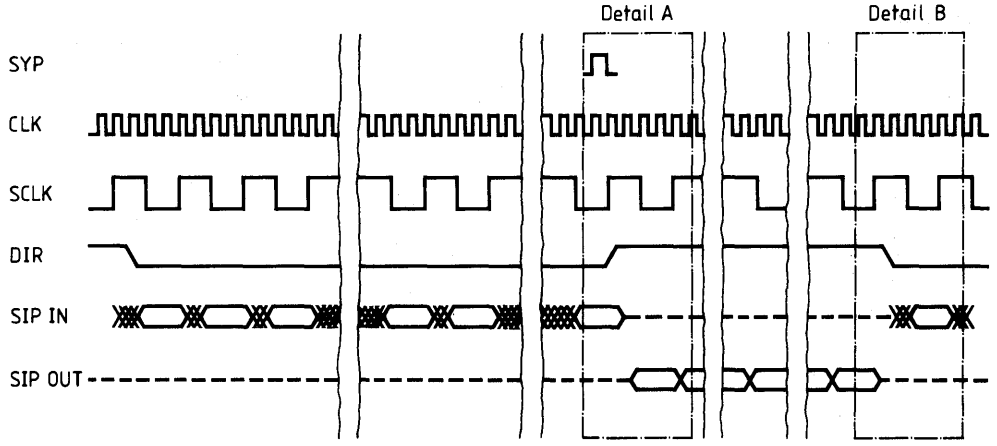
DMA Write

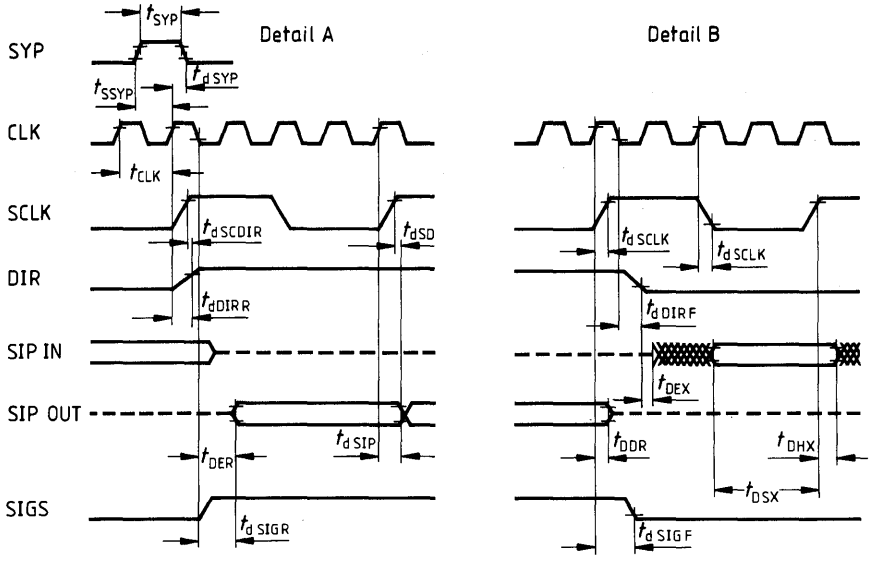


Clock Timing

Parameter	Symbol	Limit Values		Unit
		min.	max.	
System Clock				
System clock frequency	f_{CLK}	1	4.2	MHz
Duty cycle		45	55	%
Sync pulse period	t_{SPP}	125	N x 125	µs
Sync pulse width	t_{SYP}	60	t_{CLK}	ns
Pulse delay to CLK	t_{dSYP}	10		ns
Setup time to CLK	t_{sSYP}	50		ns
Clock rise/fall time	$t_{r\,CLK}$/ $t_{f\,CLK}$		10	ns
Slave Clock				
Clock frequency	f_{SCLK}	512	512	kHz
Clock delay time	t_{dSCLK}	100	165	ns
Delay time SCLK to data	t_{dSD}	20		ns
DIR Clock				
Delay time to CLK (rising edge)	$t_{dDIR\,R}$	120	190	ns
Delay time to CLK (falling edge)	$t_{dDIR\,F}$	30	110	ns
Delay time SCLK to DIR	t_{dSCDIR}	−10	70	ns
SIU Interface				
SIP data delay	t_{dSIP}	160	300	ns
Data enable receive	t_{DER}	100	180	ns
Data disable receive	t_{DDR}	100	180	ns
Data enable transmit	t_{DEX}	0		ns
Data hold transmit	t_{DHX}	0		ns
Data setup transmit (control data)	t_{DSX}	CP/+200		ns
Data setup transmit	t_{DSX}	200		ns
Signaling strobe delay (falling edge)	$t_{DSIG\,F}$	90	200	ns
Signaling strobe delay (rising edge)	$t_{DSIG\,R}$	140	220	ns

SIP Interface Timing



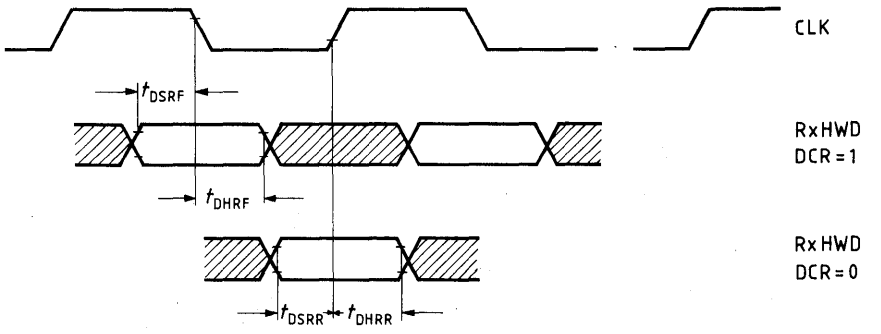


Serial Port Timing

PCM Interface

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Receive Timing				
Receive data setup DCR = 1	t_{DSRF}	20		ns
Receive data setup DCR = 0*	$t_{DS\ RR}$	40		ns
Receive data hold DCR = 1	$t_{DH\ RF}$	40		ns
Receive data hold DCR = 0	$t_{DH\ RR}$	10		ns

Receive Timing

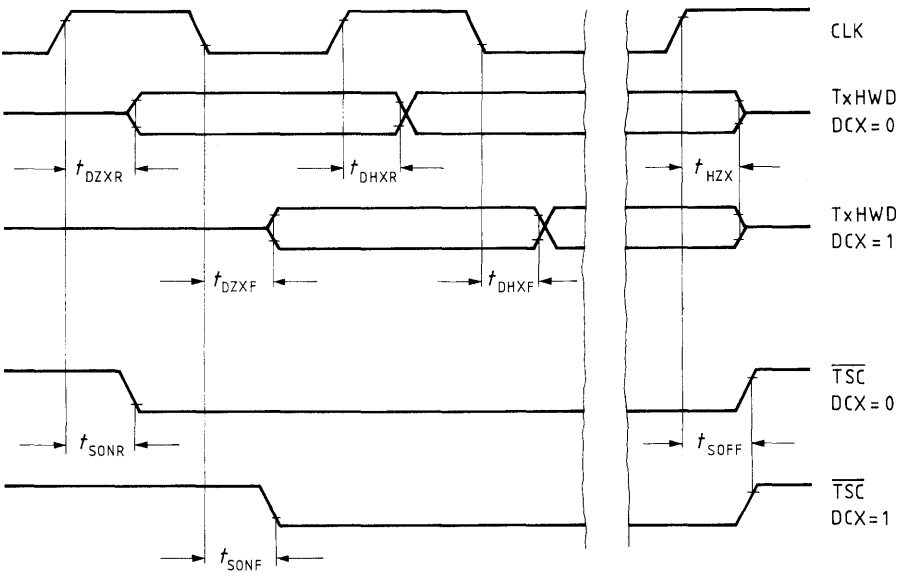


*) Common channel mode t_{DSRR} 75 ns

PCM Interface (cont'd)

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit	Test Conditions
Transmit Timing					
Data enable DCX = 0	t_{DZXR}	80	160	ns	C_L = 200 pF
Data enable DCX = 1	t_{DZXF}	40	100	ns	C_L = 200 pF
Data hold time DCX = 0	t_{DHXR}	45	160	ns	C_L = 200 pF
Data hold time DCX = 1	t_{DHXF}	40	100	ns	C_L = 200 pF
Data float on TS EXIT	t_{HZX}	35	80	ns	C_L = 150 pF
Time slot x to enable DCX = 0	t_{SONR}	70	130	ns	C_L = 150 pF
Time slot x to enable DCX = 1	t_{SONF}	40	100	ns	C_L = 150 pF
Time slot x to disable	t_{SOFF}	40	100	ns	C_L = 150 pF

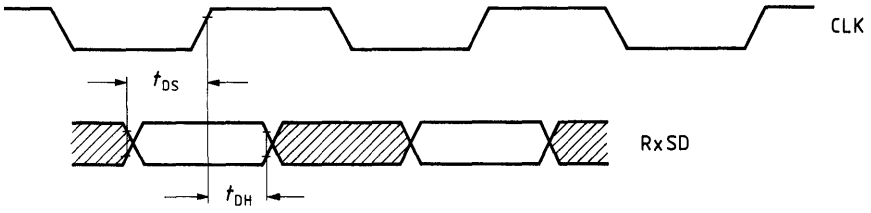
Transmit Timing



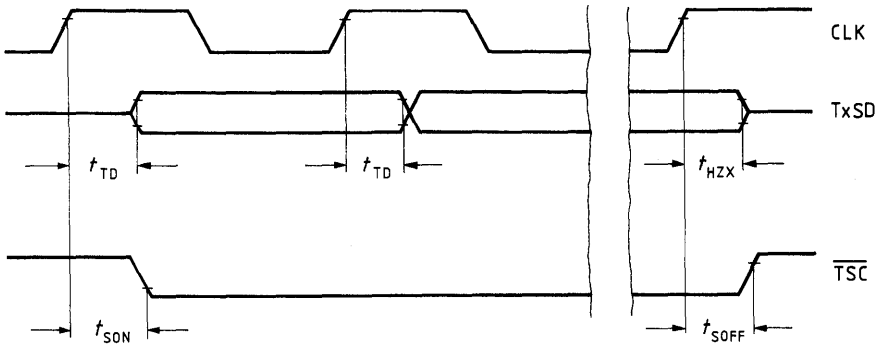
HDLC Interface

Parameter	Symbol	Limit Values		Unit	Test Conditions
		min.	max.		
Receive Timing					
Receive data setup	t_{DS}	40		ns	
Receive data hold	t_{DH}	10		ns	
Transmit Timing					
Transmit data delay	t_{TD}	40	100	ns	$C_L = 200$ pF
Data float on TS EXIT	t_{HZX}	35	80	ns	$C_L = 200$ pF
Time slot x to enable	t_{SON}	40	95	ns	$C_L = 150$ pF
Time slot x to disable	t_{SOFF}	35	90	ns	$C_L = 150$ pF

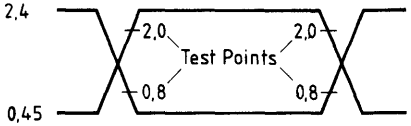
Receive Timing



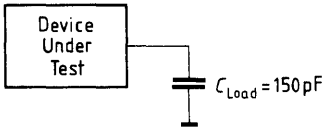
Transmit Timing



AC Testing Input, Output Waveform



AC Testing Load Circuit



AC testing: inputs are driven at 2.4 V for a logic "1" and at 0.45 V for a logic "0".
Timing measurements are made at 2.0 V for a logic "1" and at 0.8 V for a logic "0".

PCM Interface Controller (PIC) PEB 2052

Preliminary Data **CMOS IC**

Type	Ordering Code	Package
PEB 2052-C	Q67100-H6059	C-DIP-40
PEB 2052-N	Q67100-H6060	PL-CC-44 (SMD)
PEB 2052-P	Q67100-H6061	P-DIP-40

The PCM interface controller PEB 2052 is a device for the control of voice, data, and signaling paths of up to 16 subscribers on peripheral component boards in digital telephone systems. In combination with the highly flexible Signal Processing Codec Filter (SICOFI® PEB 2060) it forms an optimized analog subscriber-line board architecture. Its flexibility allows operation as general-purpose controller for data switching and MUX/De MUX applications.

The PIC controls space and time switching functions between subscriber-line devices and time-division multiplex highways. Further, it controls the flow of information between the subscriber interface ports and a local line card processor.

To meet the different requirements the PIC PEB 2052 provides the following interfaces:

- 8 serial, bidirectional I/O ports for the transfer of voice, data, control, and signaling information between the PBC and codec filters (e.g. SICOFI PEB 2060), digital interface circuits or signal processors.
- Double-constructed PCM interface.
- Bit-parallel interface for the connection of 8-bit standard microcomputers such as the SAB 8051.

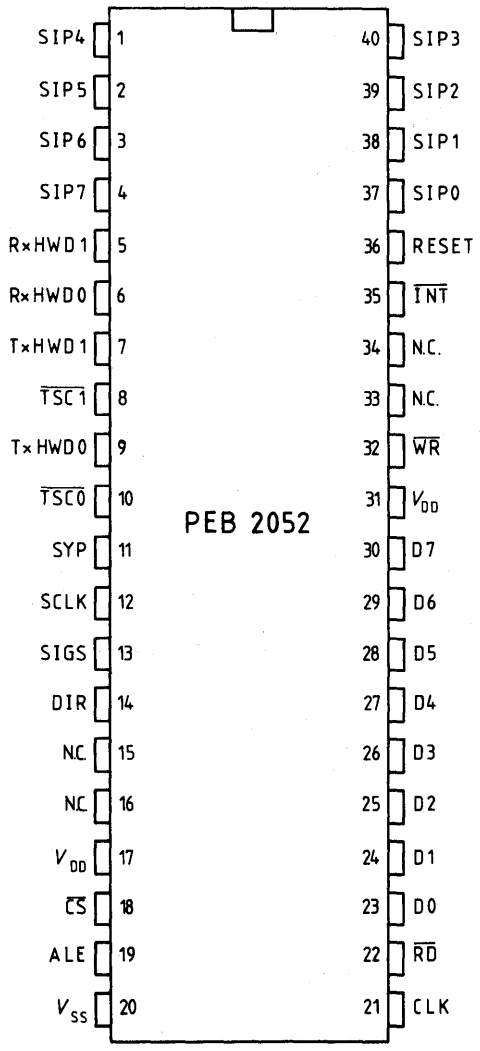
The PIC PEB 2052 is pin and software compatible with PEB 2050 and is optimized for applications without an HDLC signaling link. It is fabricated using Siemens ACMOS 3 technology.

Features

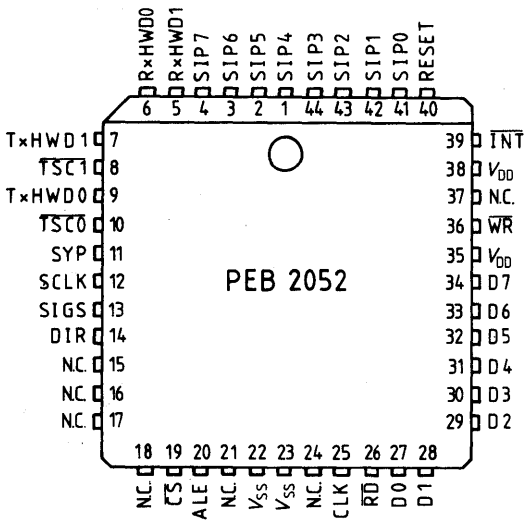
- Board controller for up to 16 subscribers of a digital switching system
- Designed for different PCM systems
- Time-slot assignment freely programmable for all subscribers connected
- Control of voice, data, signaling and line board parameters to minimize hardware requirements and to simplify software
- Provides two full duplex PCM highways for the system interface
- Pin and software compatible with PEB 2050
- Standard µP interface
- µP access to all internal data streams including time-slot oriented data streams
- Support of subscriber circuits by generating timing signals
- Single +5 V power supply
- Advanced CMOS technology
- Low power consumption

Pin Configurations
(top view)

P-DIP



PL-CC



Pin Definitions and Functions

Pin No. PL-CC	Pin No. P-DIP	Symbol	Name	Function
1 4	1 4	SIP 4 . . . . SIP 7	Subscriber interface port (input/output)	These interface ports are used for bi-directional, bit-serial transfer of speech, data and control words to and from the signal processing codec filter (SICOFI) or standard codec. Corresponding with the direction signal, the PIC PEB 2052 is transmitting during the high level of DIR within the first half of a 125 µs frame.
5	5	RxHWD 1	Receive highway data (input)	Receive PCM highway 1 interface.
6	6	RxHWD 0	Receive highway data (input)	Receive PCM highway 0 interface. The PIC serially receives a PCM word (8 bits) through one of these leads at the programmed time slot.
7	7	TxHWD 1	Transmit highway data (output)	Output of the transmit side onto the send PCM highway 1 (serial bus). The 8-bit PCM word is serially sent out on this pin at the programmed time slot. Tristate output.
8	8	$\overline{\text{TSC 1}}$	Tristate control (output, active low)	Normally high, this signal goes low while the PIC is transmitting an 8-bit PCM word on the PCM highway 1.
9	9	TxHWD 0	Transmit highway data (output)	Output of the transmit side onto the send PCM highway 0.
10	10	$\overline{\text{TSC 0}}$	Tristate control (output, active low)	Tristate control of highway 0.
11	11	SYP	Synchronization	SYP is a frame synchronization pulse which resets the on-chip time-slot counters.
12	12	SCLK	Slave clock (output)	Clock output for the peripheral devices. The signals between the codec filter and the PIC are latched and transmitted with the rising edge of SCLK.
13	13	SIGS	Signal strobe (output, active high)	The SIGS output supplies a programmable strobe signal.

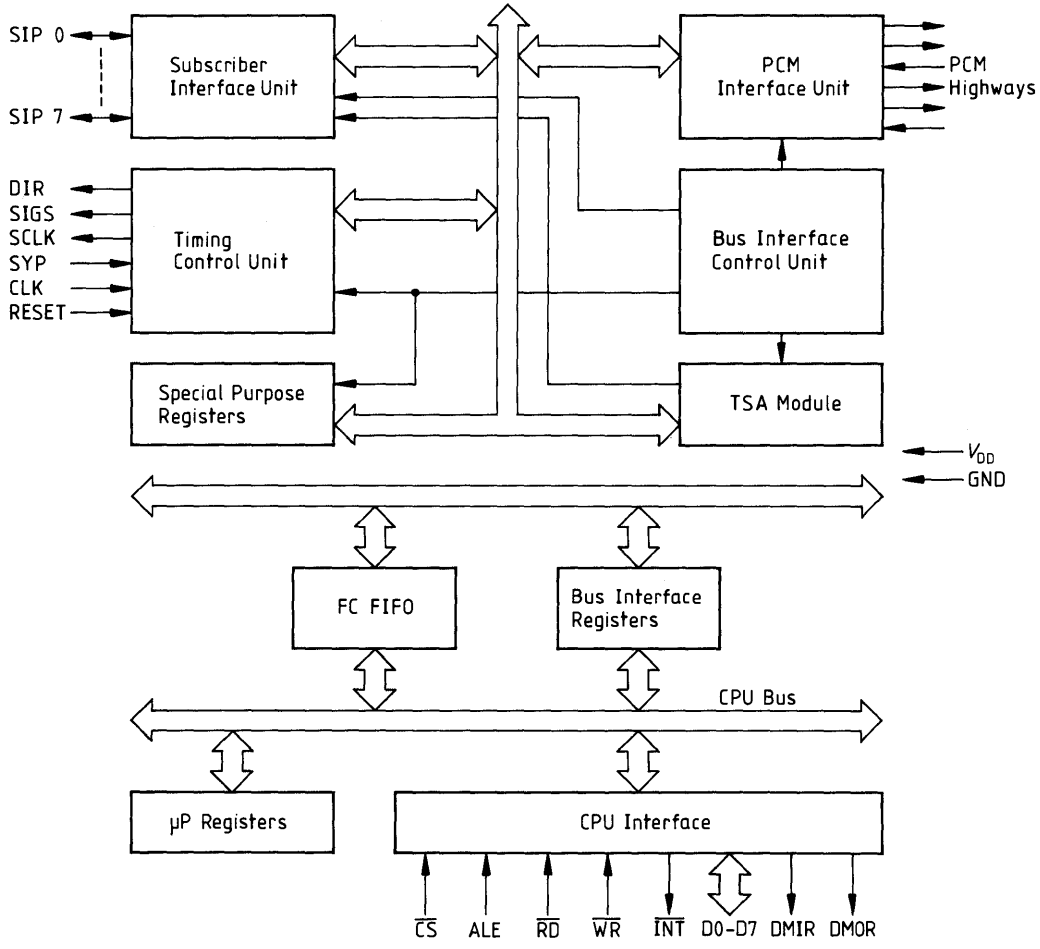
Pin Definitions and Functions (cont'd)

Pin No. PL-CC	Pin No. P-DIP	Symbol	Name	Function
14	14	DIR	Direction (output, active high)	DIR is an 8-kHz-symmetric frame signal which controls the direction of data transfer from and to the peripheral devices. The PIC is able to receive data during the low state of DIR.
15	15	N.C.		Not connected
16	16	N.C.		Not connected
38	17	V_{DD}		Power supply: $V_{DD} = 5.0\,V \pm 0.25\,V$
19	18	$\overline{CS}$	Chip select (input, active low)	CS is used to address the PIC. A low level at this input enables the PIC to accept commands or data from a µP within a write cycle, or to transmit data during a read cycle.
20	19	ALE	Address latch enable (input, active high)	A high level at this input indicates that the data on the external bus is an address selecting one of the PIC-internal sources or destinations. Latching into the address latch occurs during the high-low transition.
22, 23	20	V_{SS}		Ground (0 V)
25	21	CLK	Clock (input)	A standard TTL clock provides the basic timing of the controller. The clock is synchronous to the PCM clock.
26	22	$\overline{RD}$	Read strobe (input, active low)	$\overline{RD}$ is used together with $\overline{CS}$ to transfer data from the PBC to a µP or memory.
27 34	23 30	D0 . . . . . . D7	System data bus	The data bus transfers data and commands between the µP or memory and the PIC.
35	31	V_{DD}		Power supply: $V_{DD} = 5.0 \pm 0.25\,V$

Pin Definitions and Functions (cont'd)

Pin No. PL-CC	Pin No. P-DIP	Symbol	Name	Function
36	32	$\overline{WR}$	Write strobe (input, active low)	During the low state of $\overline{WR}$ data can be transferred from the µP or memory to the PBC.
37	33 34	N.C. N.C.		Not connected Not connected
39	35	$\overline{INT}$	Interrupt request (output, active low)	The signal is pulled down, when the PIC is requesting an interrupt. In that case, the µP should enter an interrupt routine for reading status register 1.
40	36	RESET	Reset (input, active hogh)	A high on this input forces the P/C into reset state. The minimum reset pulse is 16 complete clock cycles.
41 44	37 40	SIP 0 . . . . . . SIP 3	Subscriber interface port (input/output)	These interface ports are used for bi-directional, bit-serial transfer of speech, data and control words to and from the Signal Processing Filter (SICOFI) or standard codec. Corresponding with the direction signal, the PIC PEB 2052 is transmitting during the high level of DIR within the first half of a 125 µs frame.

Block Diagram



Description of the Functional Blocks

The PIC has been designed especially for use in peripheral subscriber boards, but its functional flexibility also permits its application in various parts of a digital exchange telecommunications system.

Used in peripheral subscriber boards it performs two essential functions:

1) Exchange of control data between an on-board processing unit and individual subscriber connections.
2) The time-slot controlled transfer of PCM data (64-Kbaud channels) between the PCM highways and the subscriber connections. Data transfers between both parts, such as the access of the on-board µP to 64-Kbaud channels, are considerably simplified by the IC.

The PIC Consists of the Following Functional Blocks

- Subscriber Interface Unit
- PCM Interface Unit
- TSA Module (Contents-Addressable Memory)
- Timing Control Unit
- µP Interface
- µP Control and Status Register
- Feature Control FIFO (16 byte)
- Bus Interface Register

Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Storage temperature	T_{stg}	−65	125	°C

Range of Operation

Operating temperature	T_A	0	70	°C
Voltage at any pin referred to ground	V_S	−0.5	7	V
Total power consumption	P_{tot}		35	mW

DC Characteristics

$T_A = 0$ to 70 °C; $V_{CC} = 5\ V \pm 0.25\ V$; GND = 0 V

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
L-input voltage	V_{IL}	−0.5		0.8	V
H-input voltage	V_{IH}	2.0		5.5	V
L-output voltage $I_{OL} = +1.6$ mA	V_{OL}			0.45	V
H-output voltage $I_{OH} = -400\ \mu A$	V_{OH}	2.4			V
Input leakage current $V_{IN} = V_{CC}$ to 0 V	I_{IL}	−10		10	µA
Output leakage current $V_{OUT} = V_{CC}$ to 0 V	I_{OL}	−10		10	µA
V_{CC} supply current $V_{CC} = 5$ V	I_{CC}			7	mA

Capacitance

$T_A = 25$ °C; V_{CC} = GND = 0 V

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Input capacitance $f_C = 1$ MHz	C_{IN}		5	10	pF
Input/output capacitance	$C_{I/O}$		10	20	pF
Output capacitance unmeasured pins returned to GND	C_{OUT}		8	15	pF

AC Characteristics

$T_A = 0$ to 70 °C; $V_{CC} = 5\ V \pm 0.25\ V$; GND = 0 V

Microprocessor Interface

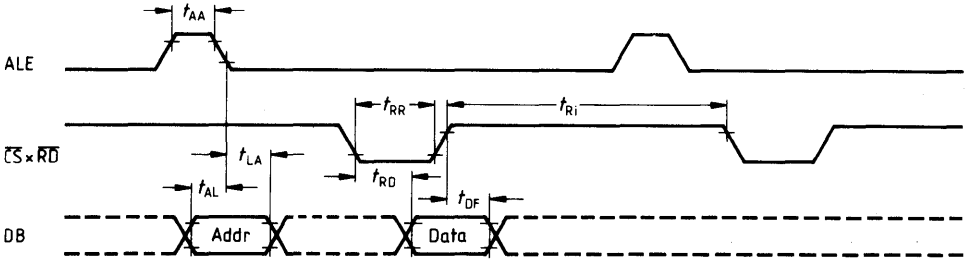
Read Cycle

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Address hold after ALE	t_{LA}	20		ns
Address to ALE setup	t_{AL}	30		ns
Data delay from $\overline{RD}$	t_{RD}		120	ns
$\overline{RD}$ pulse width	t_{RR}	120		ns
Output float delay	t_{DF}		25	ns
$\overline{RD}$ control interval	t_{RI}	80		ns
ALE pulse width	t_{AA}	60		ns

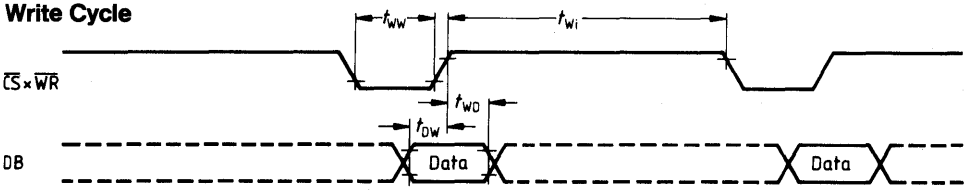
Write cycle

$\overline{WR}$ pulse width	t_{WW}	100		ns
Data setup to $\overline{WR}$	t_{DW}	50		ns
Data hold after $\overline{WR}$	t_{WD}	25		ns
$\overline{WR}$ control interval	t_{WI}	50		ns

Read Cycle



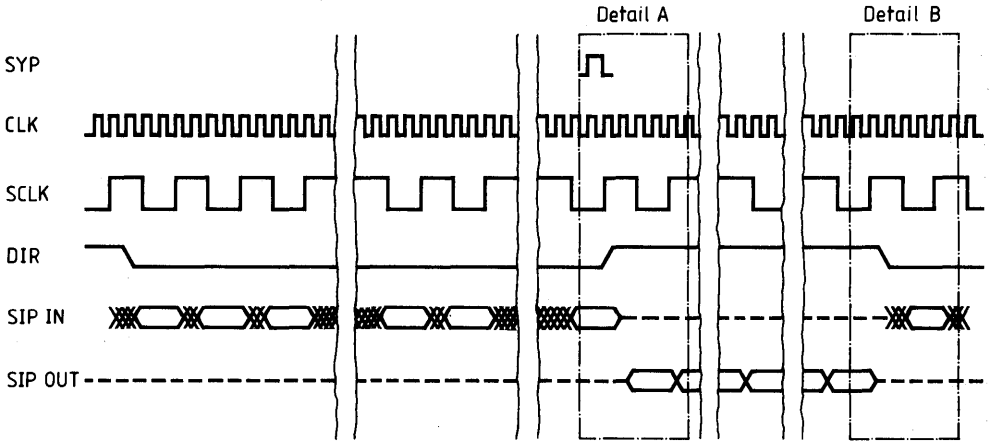
Write Cycle

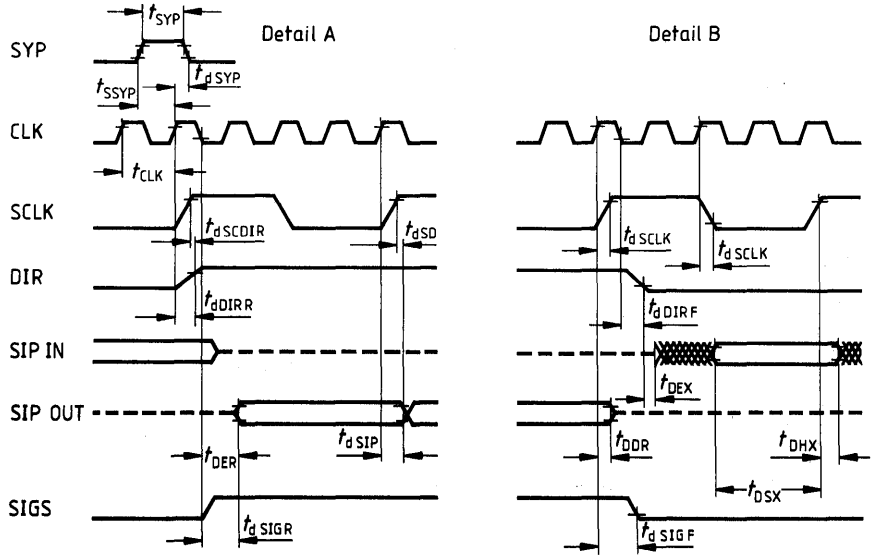


Clock Timing

Parameter	Symbol	Limit Values		Unit
		min.	max.	
System Clock				
System clock frequency	f_{CLK}		4.2	MHz
Duty cycle		40	60	%
Sync pulse period	t_{SPP}	125	N x 125	µs
Sync pulse width	t_{SYP}	60	t_{CLK}	ns
Pulse delay to CLK	t_{dSYP}	10		ns
Setup time to CLK	t_{sSYP}	50		ns
Slave Clock				
Clock frequency	f_{SCLK}	512	512	kHz
Clock delay time	t_{dSCLK}		150	ns
DIR Clock				
Delay time to CLK (rising edge)	$t_{dDIR\ R}$		150	ns
Delay time to CLK (falling edge)	$t_{dDIR\ F}$		110	ns
SIU Interface				
SIP data delay	t_{dSIP}		200	ns
Data enable receive	t_{DER}		120	ns
Data disable receive	t_{DDR}		120	ns
Data enable transmit	t_{DEX}	0		ns
Data hold transmit	t_{DHX}	0		ns
Data setup transmit (control data)	t_{DSX}	CP/2+200		ns
Data setup transmit	t_{DSX}	100		ns
Signaling strobe delay (falling edge)	$t_{DSIG\ F}$		150	ns
Signaling strobe delay (rising edge)	$t_{DSIG\ R}$		150	ns

SIP Interface Timing



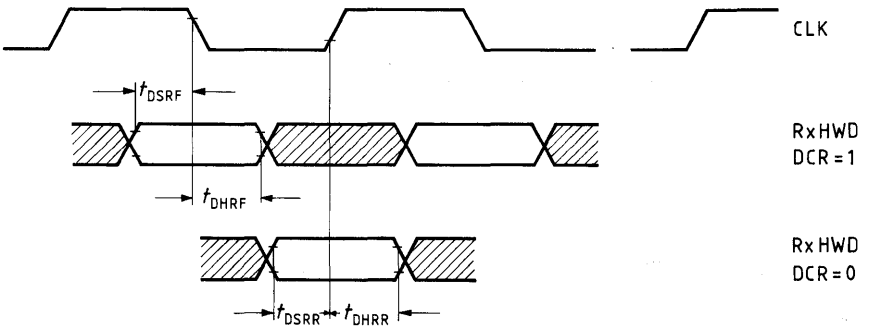


Serial Port Timing

PCM Interface

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit
Receive Timing				
Receive data setup DCR = 1	t_{DSRF}	20		ns
Receive data setup DCR = 0	$t_{DS\,RR}$	40		ns
Receive data hold DCR = 1	$t_{DH\,RF}$	40		ns
Receive data hold DCR = 0	$t_{DH\,RR}$	10		ns

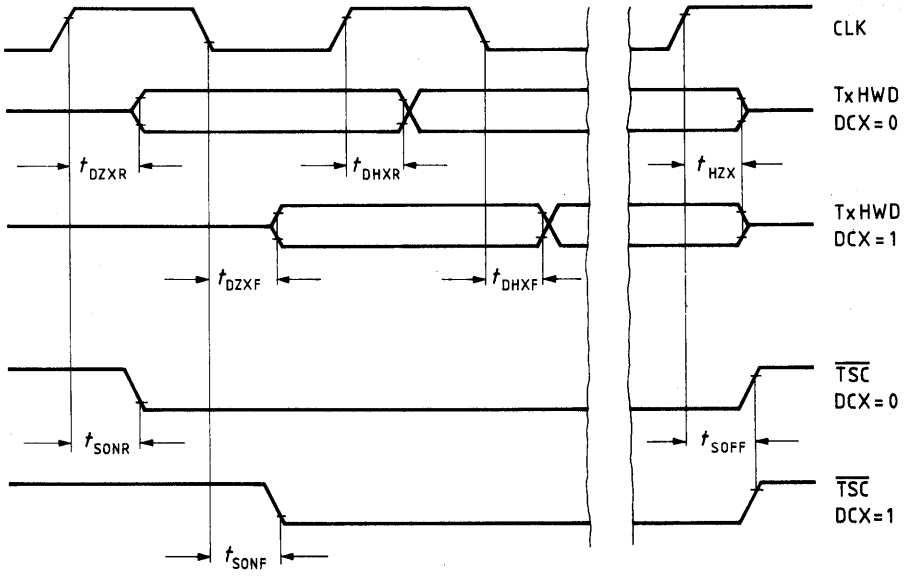
Receive Timing



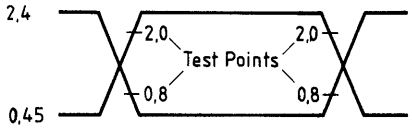
PCM Interface (cont'd)

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit	Test Conditions
Transmit Timing					
Data enable DCX = 0	t_{DZXR}		160	ns	C_L = 200 pF
Data enable DCX = 1	t_{DZXF}		100	ns	C_L = 200 pF
Data hold time DCX = 0	t_{DHXR}		160	ns	C_L = 200 pF
Data hold time DCX = 1	t_{DHXF}		100	ns	C_L = 200 pF
Data float on TS EXIT	t_{HZX}		80	ns	C_L = 150 pF
Time slot x to enable DCX = 0	t_{SONR}		130	ns	C_L = 150 pF
Time slot x to enable DCX = 1	t_{SONF}		100	ns	C_L = 150 pF
Time slot x to disable	t_{SOFF}		100	ns	C_L = 150 pF

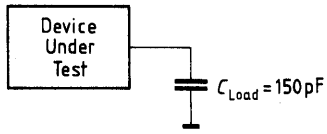
Transmit Timing



AC Testing Input, Output Waveform



AC Testing Load Circuit



AC testing: inputs are driven at 2.4 V for a logic "1" and at 0.45 V for a logic "0". Timing measurements are made at 2.0 V for a logic "1" and at 0.8 V for a logic "0".

Signal Processing Codec Filter (SICOFI) PEB 2060

Preliminary Data **CMOS IC**

Type	Ordering Code	Package
PEB 2060-P	Q67100-Z170	P-DIP-22
PEB 2060-N	Q67100-Z8393	PL-CC-28 (SMD)

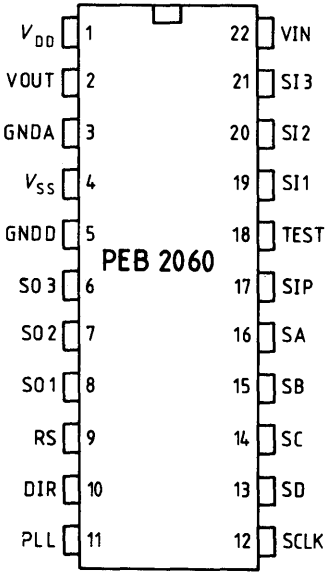
The Signal Processing Codec Filter (SICOFI®) PEB 2060 is a fully integrated PCM codec (coder/decoder) and transmit/receive filter fabricated in advanced CMOS technology for applications in digital telecommunication systems. Based on a digital filter concept, the PEB 2060 provides improved transmission performance and high flexibility. The digital signal processing approach supports software controlled adjustment of the analog behavior, including attractive features such as programmable transhybrid balancing, impedance matching, gain and frequency response correction.

Features

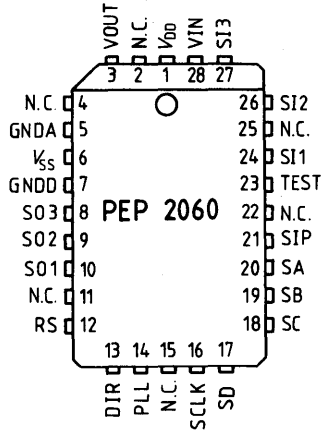
- Single chip codec and filter
- Band limitation according to CCITT and AT&T recommendations
- Digital Signal Processing techniques
- Digital voice transmission
  - PCM encoded (A-law or μ-law)
  - linear (16 bit 2s complement)
- Programmable digital filters for
  - impedance matching
  - transhybrid balancing
  - gain
  - frequency response correction
- Configurable three pin serial interface
  - 512-kHz-SLD-Bus (e.g. to PEB 2050/51)
  - burst mode with bit rates up to 8 MHz
- Programmable signaling interface to peripherals (e.g. SLIC)
- High performance A/D and D/A conversion
- Programmable analog gain
- Advanced test capabilities
  - three digital loop back modes
  - two analog loop back modes
  - on chip sine wave generation
- No trimming or adjustments
- No external components
- Variable SICOFI Master Clock selection
- Signaling expansion possible
- Prepared for three-party conferencing
- Advanced low power 2 μCMOS technology
- Power supply +/−5 V

Pin Configuration
(top view)

P-DIP-22



PL-CC-28



Pin Definitions and Functions

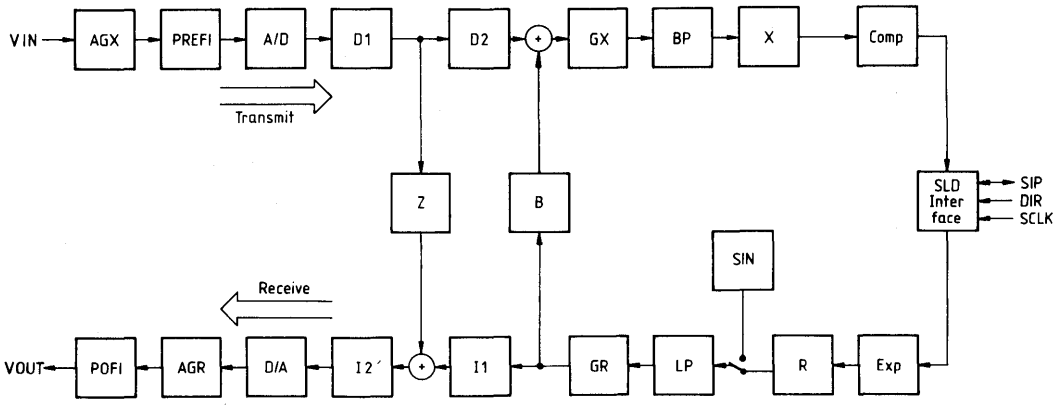
Pin No. P-DIP	Pin No. PL-CC	Symbol	Input (I) Output (O)	Function
1	1	V_{DD}	I	Power supply +5 V
4	6	V_{SS}	I	Power supply −5 V
3	5	GNDA	I	Ground analog, not internally connected to GNDD. All analog signals are referred to this pin.
5	7	GNDD	I	Ground digital, not internally connected to GNDA. All digital signals are referred to this pin.
22	28	VIN	I	Analog voice input to transmit path.
2	3	VOUT	O	Analog voice output of the received digital voice.
12	16	SCLK	I	Slave clock.
10	13	DIR	I	Frame synchronisation signal (direction signal).
17	21	SIP	I/O	Serial Interface Port, bidirectional serial data port.
9	12	RS	I	Reset input, active high, RS forces the SICOFI to power down mode and resets the configuration registers.
18	23	TEST	I	Test input, normally connected to GNDD.
11	14	PLL	I	Master clock selection (PLL/external clock).
19	24	SI1	I	Signaling Inputs. Data present at SI is sampled and transmitted via the serial interface.
20	26	SI2	I	
21	27	SI3	I	
8	10	SO1	O	Signaling Outputs. Data received via the serial interface is latched and fed to these outputs.
7	9	SO2	O	
6	8	SO3	O	
16	20	SA	I/O	Programmable I/O signaling pins. Each of these pins may be declared input or output individually with adequate SICOFI status settings. If 2 SICOFIs are connected to 1 serial interface, pin SA (high/low) assigns voice, control and signaling bytes.
15	19	SB	I/O	
14	18	SC	I/O	
13	17	SD	I/O	

SICOFI Principles

The SICOFI codec filter solution is a highly digital approach utilizing the advantages of digital signal processing such as excellent performance, high flexibility, easy testing, no sensitivity to fabrication and temperature variations, no problems with crosstalk and power supply rejection.

Figure 1

SICOFI Signal Flow Graph



Transmit Direction

The analog input signal is A/D converted, digitally filtered and transmitted either PCM-encoded or linear. Antialiasing is done with a 2nd order Sallen-Key prefilter (PREFI). The A/D Converter (ADC) is a modified slopeadaptive interpolative sigma-delta modulator with a sampling rate of 128 kHz. Digital downsampling to 8 kHz is done by subsequent decimation filters D1 and D2 together with the PCM bandpass filter (BP).

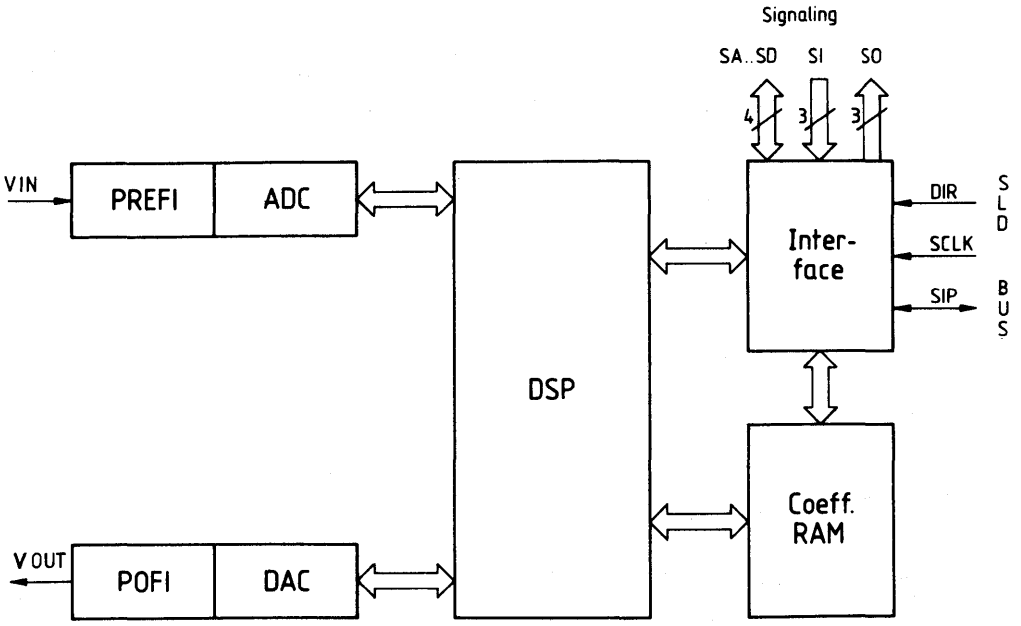
Receive Direction

The digital input signal is received PCM-encoded or linear, digitally filtered and D/A converted to generate the ananlog output signal. Digital interpolation up to 128 kHz is done by the PCM lowpass filter (LP) and the interpolation filters I1 and I2. The D/A Converter (DAC) output is fed to the 2nd order Sallen-Key postfilter (POSI).

Programmable Functions

The high flexibility of the SICOFI is based on a variety of user programmable filters, which are analog gain adjustment AGR and AGX, digital gain adjustment GR and GX, frequency response adjustment R and X, impedance matching filter Z and the transhybrid balancing filter B.

Figure 2
SICOFI Block Diagram



The SICOFI bridges the gap between analog and digital voice signal transmission in modern telecommunication system.

High performance oversampling analog-to-digital converter (ADC) and digital-to-analog converter (DAC) provide the conversion accuracy required. An analog antialiasing prefilter (PREFI) and smoothing postfilter (POFI) is included. The dedicated on chip digital signal processor (DSP) handles all the algorithms necessary, e.g. PCM bandpass filtering, sample rate conversion and PCM companding. The three pin serial SLD-Bus interface handles digital voice transmission and SICOFI feature control. Specific filter programming is done by downloading coefficients to the coefficient ram (CRAM).

The ten pin parallel signaling interface provides for a powerful per line SLIC control.

Serial Interface

The exchange of data on the SLD-Bus is based on a bidirectional, bitserial interface consisting of three pins: SIP, DIR and SCLK.

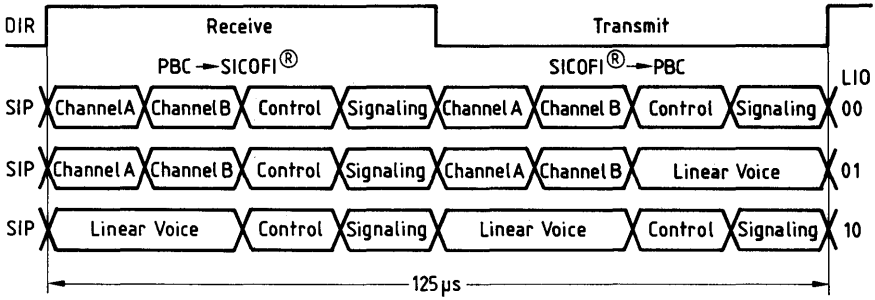
Data is written or read out on the Serial Interface Port (SIP) under control of the frame synchronisation signal DIR with a period of 125 µs*). The interface clock frequency supplied at the Slave CLocK pin SCLK is 512 kHz*). The rate of the serial data stream on the SIP pin is 512 kbit/s, that is 64 bits per each 8 kHz frame*).

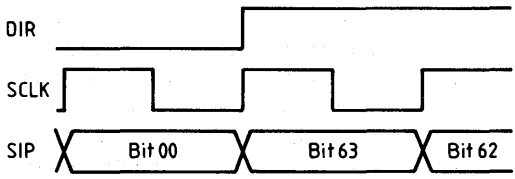
Starting with the rising edge DIR, four bytes of information are transfered on the SLD-Bus to the SICOFI, followed by four bytes from the SICOFI to the SLD-Bus.

Bit 7 is the first bit transfered and bit 0 is the last one of each byte.

Figure 3

Byte Sequence and Timing at Serial Interface Port SIP





LIO: Field LIO (Linear Operating Mode) in CR3

*) for applications with other clock rates see appendix A

Programming

A message-orientated byte transfer is used, due to the fact that the SICOFI needs extended control information. One control byte per frame and direction is transfered. With the appropriate received commands, data can be written to the SICOFI or read from the SICOFI onto the SLD-bus.

Data transfer to the SICOFI starts with a write command, followed by up to 8 bytes of data. The SICOFI responds to a read command with the requested information, starting at the next transmission period. If no status modification or data exchange is required a NOP byte is transfered **(see Programming Procedure)**.

Classes of Control Bytes

The 8-bit control bytes consist of either commands, status information or data. There are three different classes of SICOFI commands:

NOP NO OPERATION:
no status modification or data exchange

SOP STATUS OPERATION:
SICOFI status setting/monitoring

COP COEFFICIENT OPERATION:
filter coefficient setting/monitoring

The class of command is selected by bit 2 and 3 of the control byte as shown below. Due to the extended SICOFI feature control facilities, SOP- and COP-commands contain additional information.

BIT	7	6	5	4	3	2	1	0
NOP	1	1	1	1	1	1	1	1
SOP					0	1		
COP					X	0		

NOP Command

If no status modification of the SICOFI or control data exchange is required, a No Operation Byte NOP is transfered.

BIT	7	6	5	4	3	2	1	0
	1	1	1	1	1	1	1	1

X .... don't care

SOP Command

To modify or evaluate the SICOFI status, the contents of up to four configuration registers CR1, CR2, CR3 and CR4 may be transfered to or from the SICOFI. This is done by a SOP-Command (Status Operation Command).

BIT	7	6	5	4	3	2	1	0
	AD	R/W	PU	TR	0	1	LSEL	

AD Address Information
AD = 0 A-SICOFI addressed
AD = 1 B-SICOFI addressed
This bit is evaluated if two SICOFIs are connected to one SLD-port.
A SICOFI is accessed, if AD is consistent with the level at pin SA
(see Signaling Byte, Programming Procedure).

R/W Read/Write Information
R/W = 0 Write to SICOFI
R/W = 1 Read from SICOFI
Enables reading from the SICOFI or writing information to the SICOFI.

PU Power Up/Power Down **(see also CR3)**
PU = 1 Sets the SICOFI to power-up mode (operating)
PU = 0 Resets the SICOFI to power-down (standby mode)

TR Three Party Conference
TR = 1 The received voice bytes of Channel A and Channel B are added (A+B). The result is filtered, D/A converted and transfered to Analog Output VOUT **(see also CR3)**.

LSEL Length Select Information **(see also Programming Procedure)**
This two bit field identifies the number of subsequent data bytes
LSEL = 0 0 no byte following
LSEL = 1 1 CR1 is following
LSEL = 1 0 CR2 and CR1 are following
LSEL = 0 1 CR4, CR3, CR2 and CR1 are following in this case the PU and TR bits are not overwritten.

CR1 Configuration Register 1

This configuration register is used for enabling/disabling the programmable digital filters (DB..RG) and for accessing tesmodes (TM1).

BIT	7	6	5	4	3	2	1	0
	DB	RZ	RX	RR	RG		TM1	

DB Disable B-Filter
DB = 0 : B-Filter enabled
DB = 1 : B-Filter disabled

RZ Restore Z-Filter
RZ = 0 : Z-Filter disabled
RZ = 1 : Z-Filter enabled

RX Restore X-Filter
RX = 0 : X-Filter disabled
RX = 1 : X-Filter enabled

RR Restore R-Filter
RR = 0 : R-Filter disabled
RR = 1 : R-Filter enabled

RG Restore GX-GR-Filter
RG = 0 : GX-GR-Filter disabled
RG = 1 : GX-GR-Filter enabled

TM1			TESTMODES
0	0	0	No test mode
0	0	1	Analog loop back via Z-filter (H (Z) = 1)[1]
0	1	0	Disable highpass filter (part of bandpass BP)
0	1	1	Cut off receive path
1	0	0	Initialize data ram
1	1	0	Digital loop back via B-filter (H (B) = 1)[2]
1	1	1	Digital loop back via PCM-register[3]

[1] Output of the interpolation filter 1 I1 is set to 0.
Value of transfer function of the Z-filter is 1 (not programmable).

[2] Output of the low pass decimation filter 2 D2 is set to 0.
Value of transfer function of the B-filter is 1 (not programmable).

[3] PCM in = PCM out. This testmode is also available in standby mode.

CR2 Configuration Register 2

BIT	7	6	5	4	3	2	1	0
	D	C	B	A	EL	AM	µ/A	PCS

The first four bits D...A in this register, program the four bidirectional signaling pins SD...SA. With two SICOFIs on one SLD port only pin SD can be used, pin SA is always input in this case and indicates the address of the SICOFI.

SA = 0 : A-SICOFI, SA = 1 : B-SICOFI **(see also bit AD in SOP-command).**

D	Signaling Pin SD	D = 0	SD is output
		D = 1	SD is input
C	Signaling Pin SC	C = 0	SC is output
		C = 1	SC is input
B	Signaling Pin SB	B = 0	SB is output
		B = 1	SB is input
A	Signaling Pin SA	A = 0	SA is output
		A = 1	SA is input
EL	Signaling Expansion Logic	EL = 0	No expansion logic
		EL = 1	Expansion logic provided

signaling expansion logic is only possible with one SICOFI on port **(see also Signaling Byte)**

AM	Address Mode	AM = 0	Two SICOFIs on SLD port
		AM = 1	One SICOFI on SLD port

The SICOFI access to the SLD-Bus voice channel is controlled by AM and TR.

		Receive (SLD-Bus → SICOFI)		**Transmit (SICOFI → SLD-Bus)**	
AM	TR	SICOFI A	SICOFI B	SICOFI A	SICOFI B
0	0	channel A	channel B	channel A	channel B
0	1	channel B	channel A	channel B	channel A
1	0	channel A	–	channel A, B[1]	–
1	1	channel A + B[2]	–	channel A, B[1]	–

µ/A	PCM-Law	µ/A = 0	A-Law
		µ/A = 1	µ-Law (µ255 PCM)
PCS	Programmed B-Filter Coefficient		
		PCS = 0	Programmed coefficients
		PCS = 1	Fixed coefficients

[1] The SICOFI transmits the same byte in channel A and B.
[2] Three Party Conference.

CR3 Configuration Register 3

BIT	7	6	5	4	3	2	1	0
	AGX		AGR		PU	TR	LIO	

AGX	Analog Gain Control Transmit-Path	
	AGX = 0 0	0 dB
	AGX = 0 1	6 dB amplification
	AGX = 1 0	12 dB amplification
	AGX = 1 1	14 dB amplification

AGR	Analog Gain Control Receive-Path	
	AGR = 0 0	0 dB
	AGR = 0 1	6 dB attenuation
	AGR = 1 0	12 dB attenuation
	AGR = 1 1	14 dB attenuation

PU	Power Up/Power Down[1]	
	PU = 0	Power Down (standby)
	PU = 1	Power Up (operating)

TR Three Party Conference/Reverse Operating Mode **(see CR2)**[1]

LIO	Linear Operating Mode **(see serial interface)**	
	LIO = 0 0	PCM mode
	LIO = 0 1	Linear mode 1[2]
	LIO = 1 0	Linear mode 2

(Change of linear mode becomes valid in the next DIR-cycle).

[1] The bits PU and TR may also be overwritten by a SOP command with LSEL = 0 1 (PU and TR are part of the SOP command). With LSEL = 0 1, the bits PU and TR in the SOP command are ignored.

[2] Subsequent to a SOP/COP-read command the control and signaling information is transmitted instead of linear voice.

CR4 Configuration Register 4

BIT	7	6	5	4	3	2	1	0
		TM3		0	0		TM4	

TM3	TEST MODES
0 0 0	No test mode
0 0 1	Additional + 6 dB digital gain in transmit direction (GX)
0 1 1	Additional + 12 dB digital gain in transmit direction (GX)
1 0 0	Enable on chip sine wave generation[1]
1 1 0	Far analog loop back[2]

TM4	TEST MODES
0 0 0	No test mode
1 0 0	Digital loop back via analog port ($V_{IN} = V_{OUT}$)

COP Command

With a COP command coefficients for the programmable filters can be written to the SICOFI coefficient ram or transmitted on the SLD-bus for verification.

BIT	7	6	5	4	3	2	1	0
	AD	R/W			CODE			

AD Address Information AD = 0 A-SICOFI addressed
AD = 1 B-SICOFI addressed

This bit is evaluated with two SICOFIs on one SLD-port only.
With two SICOFIs on port, a SICOFI is identified, if AD is consistent with the level at pin SA **(see Signaling Byte, Programming Procedure).**

R/W Read/Write Information R/W = 0 Write to SICOFI
R/W = 1 Read from SICOFI

This bit indicates whether filter coefficients are written to the SICOFI or read from the SICOFI.

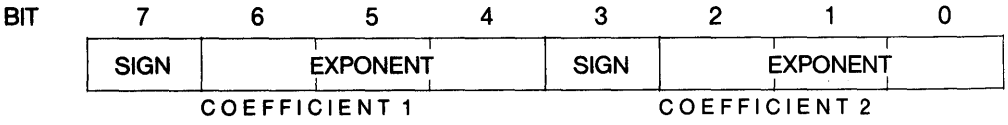
---

[1] With the R-Filter disabled a 2 kHz, 0 dBm0 sine wave signal is fed to the input of the receive Lowpass Filter LP (other frequencies see Appendix B).
[2] The output of the X-Filter is fed to the input of the R-Filter (8 kHz, 16 bit linear).

CODE							
0	0	0	0	1	1	B-Filter coefficients part 1	(followed by 8 bytes of data)
0	0	1	0	1	1	B-Filter coefficients part 2	(followed by 8 bytes of data)
0	1	0	0	1	1	Z-Filter coefficients	(followed by 8 bytes of data)
0	1	1	0	0	0	B-Filter delay coefficients	(followed by 4 bytes of data)
1	0	0	0	1	1	X-Filter coefficients	(followed by 8 bytes of data)
1	0	1	0	1	1	R-Filter coefficients	(followed by 8 bytes of data)
1	1	0	0	0	0	GX- and GR-Filter coefficients	(followed by 4 bytes of data)

Other codes are reserved for future use.

Data Byte Format



Each four bit coefficient represents a factor of $\mathbf{SIGN \times 2^{-EXPONENT}}$

Subsequent to reading the filter coefficients form the SICOFI CR2 and CR1 are transmitted additionally!!

Signaling Byte

The signaling interface of the SICOFI consists of 10 pins.

3 transmit signaling inputs: SI1, SI2 and SI3
3 receive signaling outputs: SO1, SO2 and SO3
4 bidirectional programmable signaling pins: SA, SB, SC and SD

Data present at SI1..SI3 and possibly at some or all of SA..SD (if programmed as inputs) are sampled and transfered serially on SIP onto the SLD-bus. Data received serially on SIP from the SLD-Bus are latched and fed to SO1..SO3 and possibly to some of SA..SD if programmed as output.

The signaling field format is generally:

In Receive Direction:

BIT	7	6	5	4	3	2	1	0
	SO1	SO2	SO3	SD	SC	SB	SA	SEL

In Transmit Direction:

BIT	7	6	5	4	3	2	1	0
	SI1	SI2	SI3	SD	SC	SB	SA	SEL

where SEL is the signaling expansion bit if EL = 1 in CR2.

For the different cases possible, the signaling byte format at SIP is

	Receive Signaling Byte								**Transmit Signaling Byte**							
Bit / Case	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
1	SO1	SO2	SO3	X	X	X	X	X	SI1	SI2	SI3	SD	SC	SB	SA	0
2	SO1	SO2	SO3	X	X	X	X	X	SI1	SI2	SI3	SD	SC	SB	SA	Z
3	SO1	SO2	SO3	SD	SC	SB	SA	X	SI1	SI2	SI3	0	0	0	0	0
4	SO1	SO2	SO3	SD	SC	SB	SA	X	SI1	SI2	SI3	Z	Z	Z	Z	Z
5 A-SIC	SO1	SO2	SO3	X	X	X	X	X	SI1	SI2	SI3	SD	Z	Z	Z	Z
B-SIC	X	X	X	X	SO1	SO2	SO3	X	Z	Z	Z	Z	SI1	SI2	SI3	SD
6 A-SIC	SO1	SO2	SO3	SD	X	X	X	X	SI1	SI2	SI3	0	Z	Z	Z	Z
B-SIC	X	X	X	X	SO1	SO2	SO3	SD	Z	Z	Z	Z	SI1	SI2	SI3	0

Z...high impedance, X...don't care

Signaling Byte

Cases

1 One SICOFI is connected to one SLD port, EL = 0 (no signaling expansion logic provided); SA..SD are programmed as transmit signaling inputs.

2 One SICOFI connected to one SLD port, EL = 1 (signaling expansion logic provided); SA..SD are programmed as transmit signaling inputs.

3 One SICOFI is connected to one SLD port; EL = 0 (no signaling expansion logic provided); SA..SD are programmed as receive signaling outputs.

4 One SICOFI is connected to one SLD port; EL = 1 (signaling expansion logic provided); SA..SD are programmed as receive signaling outputs.

If a signaling expansion logic is provided (see case 2 and 4), the signaling bits SA..SD which are programmed as signaling inputs or outputs can be used as additional expansion bits in receive or transmit direction, respectively. As far as SICOFI is concerned, SIP is in a high-impedance (Z) state or "don't care" (Y) state while these bits are transfered.

5 Two SICOFIs are connected to one SLD port; SD is programmed as transmit signaling input.

6 Two SICOFIs are connected to one SLD port; SD is programmed as receive signaling output.

If two SICOFIs are connected to one SLD port, no signaling expansion logic is possible. SA is programmed as input automatically, and defines the addressed SICOFI:

SA = 0 : A-SICOFI
SA = 1 : B-SICOFI.

SB and SC are not usable with two SICOFIs on one SLD port.

Programming Procedure

The following table shows some control byte sequences. If the SICOFI has to be configured completly during initialization, up to 60 bytes will be transfered.

DIR	Receive	Transmit	Receive	Transmit	Receive	Transmit	Receive	Transmit	Receive	Transmit	Receive

No Operation

	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP

SOP Write

LSEL = 00	SOP	NOP									
LSEL = 11	SOP	NOP	CR1	NOP							
LSEL = 10	SOP	NOP	CR2	NOP	CR1	NOP					
LSEL = 01	SOP	NOP	CR4	NOP	CR3	NOP	CR2	NOP	CR1	NOP	

SOP Read

LSEL = 00	SOP	NOP									
LSEL = 11	SOP	CR1									
LSEL = 10	SOP	CR2	X	CR1							
LSEL = 01	SOP	CR4	X	CR3	X	CR2	X	CR1			

COP Write

4 Bytes	COP	NOP	DB4	NOP	DB3	NOP	DB2	NOP	DB1	NOP	
8 Bytes	COP	NOP	DB8	NOP	DB7			NOP	DB1	NOP	

COP Read

4 Bytes	COP	DB4	X	DB3		DB1	X	CR2	X	CR1	
8 Bytes	COP	DB8	X	DB7		DB1	X	CR2	X	CR1	

X .... don't care

DB1, DB2...DB8...coefficient Data Byte 1..8

Operating Modes

Basic Setting

Upon initial application of V_{DD} or reseting pin RS to "1" while operating, the SICOFI enters a basic setting mode. Basic setting means, that the SICOFI configuration registers CR1...CR4 are initialized. All CR1 bits are set to "0" (all programmable filters are disabled except the B-Filter where fixed coefficients are used, no test mode); CR2 is set to "1" (SA...SD are inputs, signaling expansion logic is provided, one SICOFI on SLD-port, μ-law chosen and fixed B-Filter coefficients used). All CR3 and CR4 bits are reset to "0" (no additional amplification or attenuation, no linear mode, power down, no test mode). Receive signaling registers are cleared. SIP is in high-impedance state, the analog output V_{OUT} and the receive signaling outputs SO1...SO3 are forced to ground.

The serial interface is active to receive commands starting with the next 8-kHz SLD-bus frame. The serial interface port SIP remains tristate until CR2 has been defined.

If two SICOFIs are connected to one SLD port, both SICOFIs get the same SOP and CR2 information during initialization. The subsequent CR1 byte is assigned to the addressed SICOFI only. If the two SICOFIs need different CR2 information, the SOP-CR2 sequence has to be provided once again (each SICOFI knows its address now).

Standby Mode

Upon reception of a SOP command to load CR2 from the basic setting, the SICOFI enters the standby mode (basic setting replaced by individual CR2). Being in the operating mode, the SICOFI is reset to standby mode with a Power-Up bit PU = 0 (in CR3 or in the SOP-command directly). The serial interface is active to receive and transmit new commands and data.

Operating Mode

From the standby mode, the operating mode is entered upon recognition of a Power-Up bit PU = 1 (in CR3 or in the SOP-command directly).

Gain Adjustment

The transmit gain values are digitally programmable in the range of 0 to 8 dB in steps of ≤ 0.25 dB.

The receive gain values are digitally programmable in the range of 0 to −8 dB in steps of ≤ 0.25 dB.

Transmission Characteristics – Preliminary

The target figures in this specification are based on the subscriber-line board requirements. The proper adjustment of the programmable filters (transhybrid balancing: B; line termination: Z; frequency-response correction: X, R) needs a complete knowledge of the SICOFI®'s analog environment. Unless otherwise stated, the programmable filters have the following transfer functions:

$H(Z) = H(B) = 0$; $H(X) = H(R) = 1$; $H(Gx) = 0$ dB to 8 dB
$H(GR) = 0$ dB to -8 dB; $H(AGX) = 0$ dB to 14 dB; $H(AGR) = 0$ dB to -6 dB;

A 0 dBm0 signal is equivalent to 1.5763 [1.5710] Vrms.
A 3.14 [3.17] dBm0 signal is equivalent to 2.263 Vrms which corresponds to the overload point of 3.2 V. (A-law,[μ-law]).

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Gain (either value) Gain absolute $R_L > 1$ kΩ 1000 Hz at 0dBm0 300 Ω < R_L < 1 kΩ	G	 −0.2 −0.3	 ±0 −0.05	 0.2 0.20	dB
Gain variation with supply voltage and temperature 1000 Hz at 0dBm0	G_V	−0.2	0	0.2	dB
Total harmonic distortion[1]	THD			−44	dB
Intermodulation $2f_1-f_2$ [2] $2f_1-f_2$ [3]	IMD			 −42 −56	dB
Crosstalk Transmit to receive 0dBm0 f = 300 Hz to 3400 Hz Receive to transmit 0dBm0 f = 300 Hz to 3400 Hz	 CT_{XR} CT_{XR}			 −70 −70	 dB dB
Idle channel noise psophometric weighted Transmit, VIN = 0 V Receive, idle code +0	 N_{RP} N_{RP}			 −67 −78	 dBm0p dBm0p

[1]) Single-frequency components between 300 Hz and 3400 Hz produced by a 0 dBm0 sine wave in the range between 300 Hz and 3400 Hz.
[2]) Equal input levels in the range between −4 dBm0 and −21 dBm0; different frequencies in the range between 300 Hz and 3400 Hz.
[3]) Input level −9 dBm0, frequency range 300 Hz to 3400 Hz and −23 dBm0, 50 Hz.

Attenuation Distortion

Attenuation deviations stay within the limits in the figures below.

Figure 3

Receive: Reference frequency 1 kHz, input signal level 0 dBm0

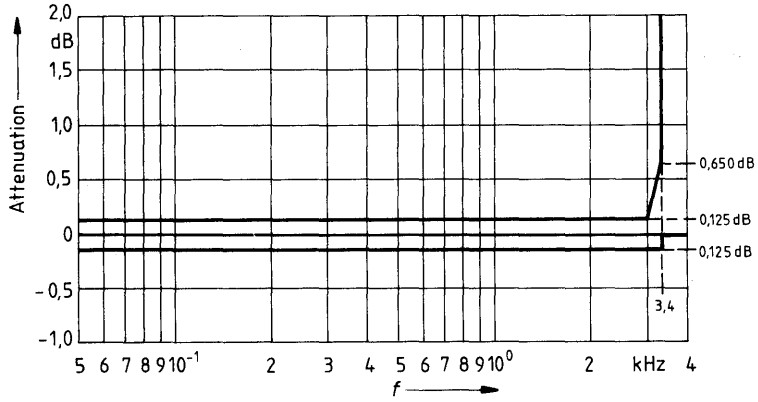
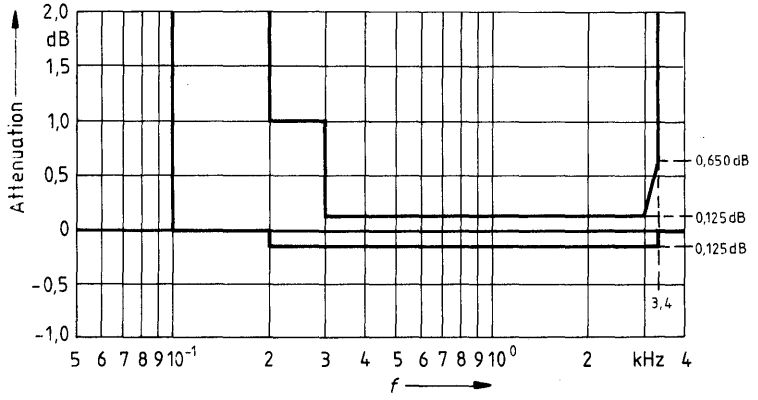


Figure 4

Transmit: Reference frequency 1 kHz, input signal level 0 dBm0



Group Delay

Maximum delays for operating the SICOFI with H(B) = H(Z) = 0 and H(R) = H(X) = 1, including delay through A/D- and D/A converters. Specific filter programming may cause additional group delays.

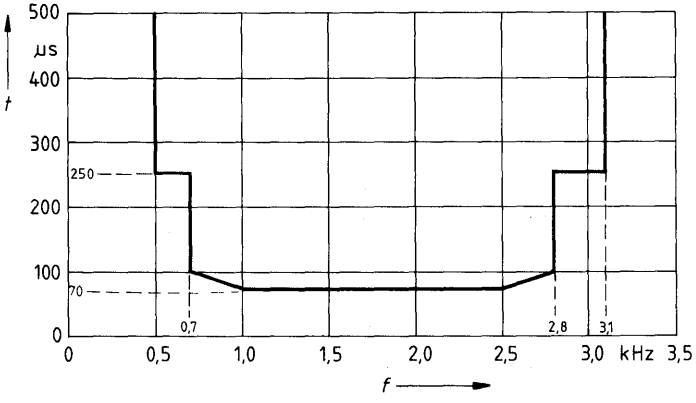
Group delay deviations stay within the limits in the figures below.

Group Delay Absolute Values: Input signal level 0 dBm0

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Transmit Delay $f = 1.4$ kHz	D_{XA}			300	µs
Receive Delay $f = 300$ Hz	D_{RA}			240	µs

Figure 5

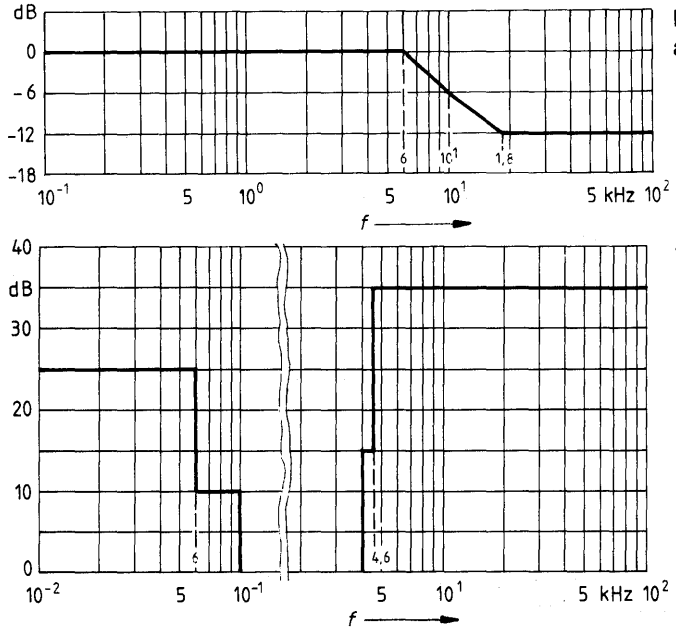
Group Delay Distortion: Input signal level 0 dBm0



Out-of-Band Signals at Analog Input

With an out-of-band sine wave signal with frequency *f* and level A applied to the analog input, the level of any resulting frequency component at the digital output will stay at least X dB below level A.

Figure 6



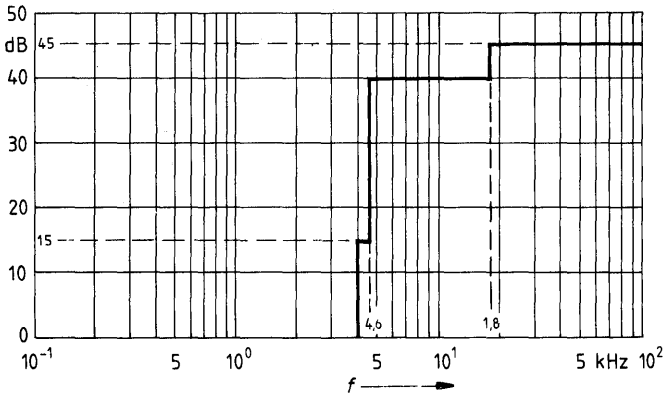
Maximum input level A at analog input

Transmit out-of-band discrimination X

Out-of-Band Signals at Analog Output

With a 0 dBm0 sine wave of frequency *f* applied to the digital input, the level of any resulting out-of-band signal at the analog output will stay at least X dB below a 0 dBm0, 1 kHz sine wave reference signal at the analog output.

Figure 7



Receive out-of-band discrimination X

Gain Tracking (receive and transmit)

The gain deviations stay within the limits in the figures below.

Figure 8

Gain Tracking: Measured with noise signal according to CCITT recommendations
Reference level is −10 dBm0

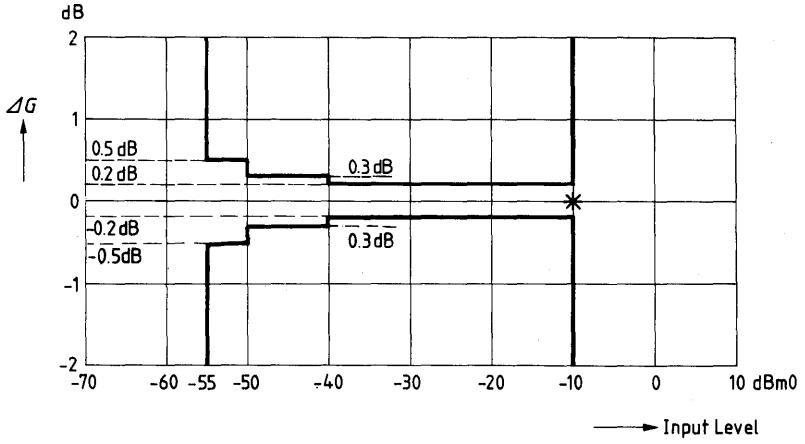
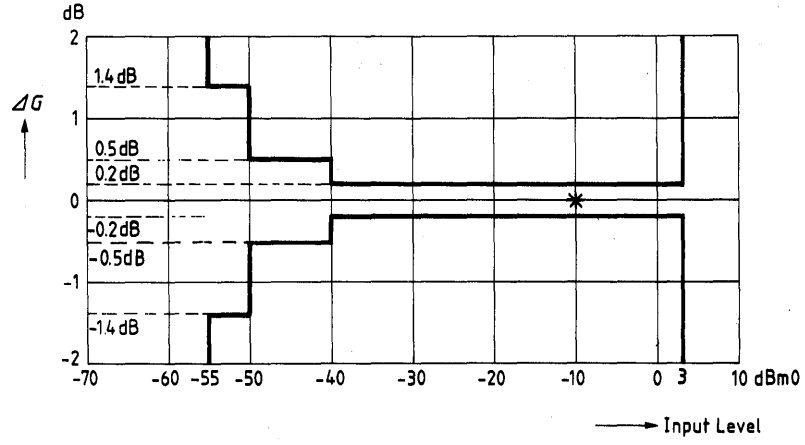


Figure 9

Gain Tracking: Measured with sine wave in the range 700 to 1100 Hz
Reference level is −10 dBm0



Total Distortion (The signal-to-distortion ratio exceeds the limits in the following figures).

Figure 10

Receive: Measured with noise signal according to CCITT recommendations

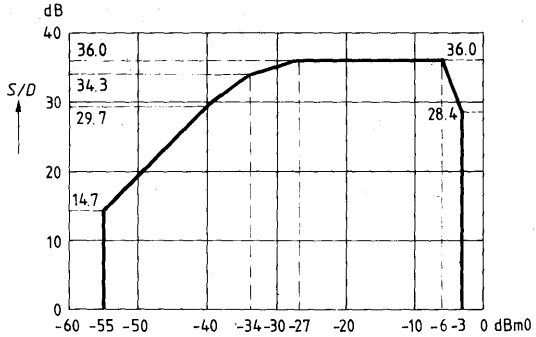


Figure 11

Transmit: Measured with noise signal according to CCITT recommendations

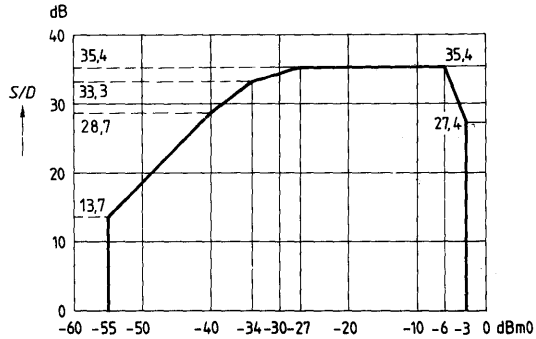
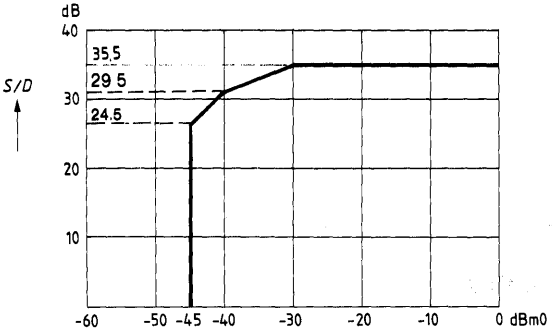


Figure 12

Receive & Transmit: Measured with sine wave in the range 700 to 1100 Hz excluding submultiples of 8 kHz



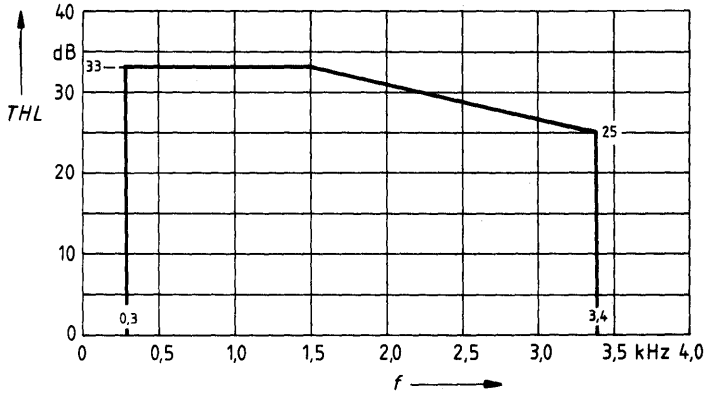
Transhybrid Loss

The quality of transhybrid-balancing is very sensitive to deviations in gain and group delay-deviations inherent to the SICOFI A/D- and D/A-converters as well as to all external components used on a line card (SLIC, OP's etc.).

The SICOFI transhybrid-loss is measured the following way: A sine wave signal with level A and a frequency in the range of 300-3400 Hz is applied to the digital input. The resulting analog output signal at pin V_{OUT} is directly connected to V_{IN}, e.g. with the SICOFI testmode "Digital Loop Back via Analog Port" **(see CR4).** The programmable filters R, Gr, X, Gx and Z are disabled, the balancing filter B is enabled with coefficients optimized for this configuration ($V_{OUT} = V_{IN}$).

The resulting echo measured at the digital output is at least X dB below the level of the digital input signal as shown in the following figure.

Figure 13



Note:

B-filter coefficients recommended for transhybrid loss measurement ($V_{OUT} = V_{IN}$)
B-filter part 1 (03) = DE, 12, 2B, 23, 15, 21, 31, D1
B-filter part 2 (03) = 00, 14, 4E, 5B, AC, DB, 1B, A3
B-filter delay (18) = 19, 19, 11, 19

Absolute Maximum Ratings

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit
V_{DD} referred to GNDD		−0.3	5.5	V
V_{SS} referred to GNDD		−5.5	0.3	V
GNDA to GNDD		−0.3	0.3	V
Analog input and output voltage				
referred to $V_{DD} = 5$ V; $V_{SS} = -5$ V	V_{IN}	−10.3	0.3	V
referred to $V_{SS} = -5$ V; $V_{DD} = 5$ V	V_{IN}	−0.3	10.3	V
All digital input voltages				
referred to GNDD = 0 V; $V_{DD} = 5$ V	V_{IN}	−0.3	5.3	V
referred to $V_{DD} = 5$ V; GNDD = 0 V	V_{IN}	−5.3	0.3	V
Power dissipation	P_D		1	W
Storage temperature	T_{stg}	−60	125	°C
Ambient temperature under bias	T_A	−10	80	°C

Operating Range

$T_A = 0$ to 70 °C; $V_{DD} = 5$ V ± 5%; $V_{SS} = -5$ V ± 5%; GNDD = 0 V; GNDA = 0 V

Parameter	Symbol	Limit Values min.	Limit Values typ.	Limit Values max.	Unit	Test Conditions
V_{DD} supply current	I_{DD}					
standby			2.1	4	mA	± 5% supply
operating			8	12	mA	± 5% supply
V_{SS} supply current	I_{SS}					
standby			1.7	3	mA	± 5% supply
operating			5	8	mA	± 5% supply
Power supply rejection (of either supply/direction)	*PSRR*	35			dB	1 kHz 80 mV_{rms} ripple
Power dissipation standby	P_{Ds}		20	37	mW	± 5% supply
Power dissipation operating	P_{Do}		70	105	mW	± 5% supply

Digital Interface

$T_A = 0$ to 70 °C; $V_{DD} = 5\ V \pm 5\%$; $V_{SS} = -5\ V \pm 5\%$; GNDD = 0 V; GNDA = 0 V

Parameter	Symbol	Limit Values		Unit
		min.	max.	
L-input voltage	V_{IL}	−0.3	0.8	V
H-input voltage	V_{IH}	2.0	V_{DD} +0.3	V
L-output voltage $I_O = -2$ mA	V_{OL}		0.45	V
H-output voltage $I_O = 400\ \mu A$		2.4		V
Input leakage current $-0.3 \le V_{IN} \le V_{DD}$	I_{IL}		±1	µA

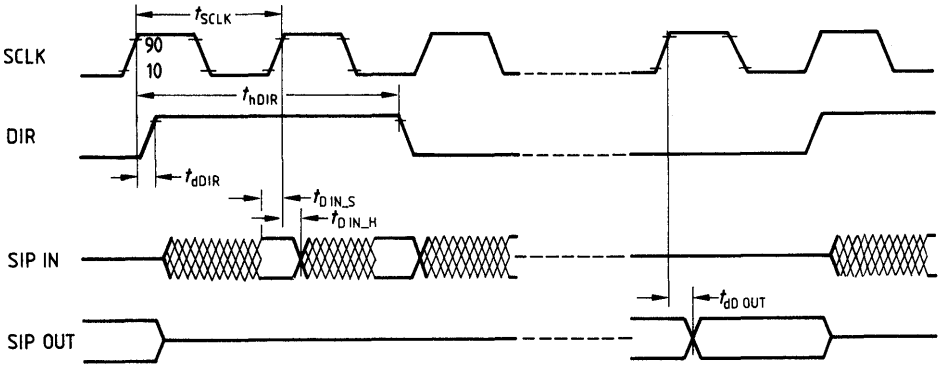
Analog Interface

$T_A = 0$ to 70 °C; $V_{DD} = 5\ V \pm 5\%$; $V_{SS} = -5\ V \pm 5\%$; GNDD = 0 V; GNDA = 0 V

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Analog input resistance	R_I	10		MΩ
Analog output resistance	R_O		10	Ω
Input offset voltage	V_{IO}		±50	mV
Output offset voltage	V_{OO}		±50	mV
Input voltage range	V_{IR}		±3.2	V
Output voltage range $R_L \ge 300\ \Omega$; $C_L \le 10$ pF	V_{OR}	±3.1		V

SIP Interface Timing (SLD-Bus)

Figure 14

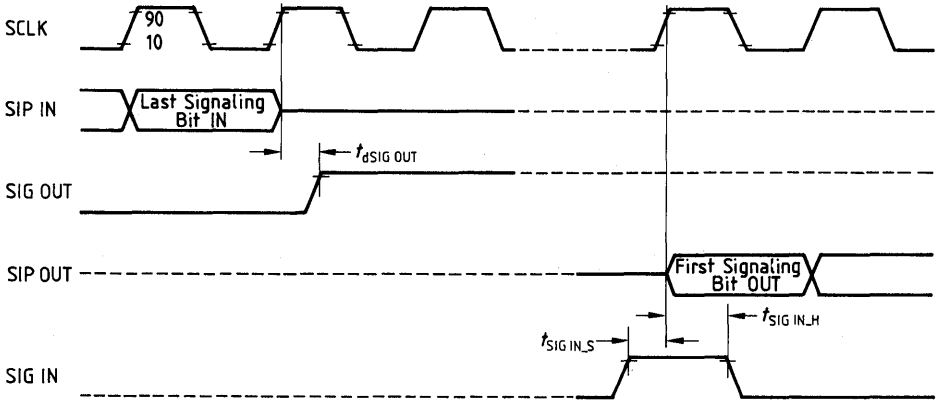


Switching Characteristics

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Period SCLK	t_{SCLK}	−10%	1/512 kHz	+10%	
Duty Cycle		10		90	%
Period DIR	t_{DIR}		125		µs
DIR delay time	t_{dDIR}	−20		80	ns
DIR high time	t_{hDIR}	500			ns
SIP data in setup time	$t_{DIN\ S}$	50			ns
SIP data in hold time	$t_{DIN\ H}$	20			ns
SIP data out delay	t_{dDOUT}			200	ns
SIP data out tristate delay vs. SCLK				50	ns
RS high time		250			ns

Signaling Interface Timing

Figure 15



Switching Characteristics

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Delay signaling out vs. SCLK[1])	$t_{dSIGout}$			200	ns
SIG in setup time[2])	$t_{SIGin\ S}$	50			ns
SIG in hold time[2])	$t_{SIGin\ H}$	100			ns

[1]) Pins SO1..SO3; Pins SA..SD as output
[2]) Pins SI1..SI3; Pins SA..SD as input

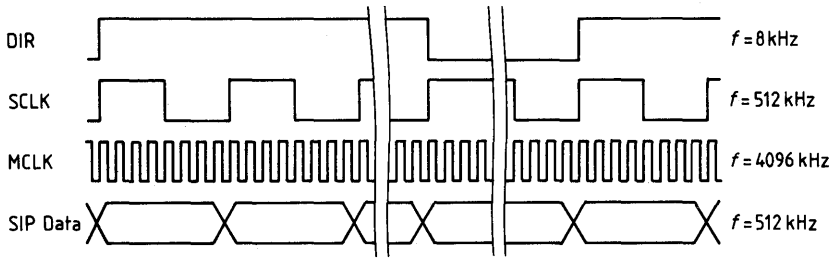
Appendix A

The SICOFI can be used with three different SLD-bus type interfaces.
A specific interface type is selected with three pins: TEST, SI3 and PLL.

Figure 16

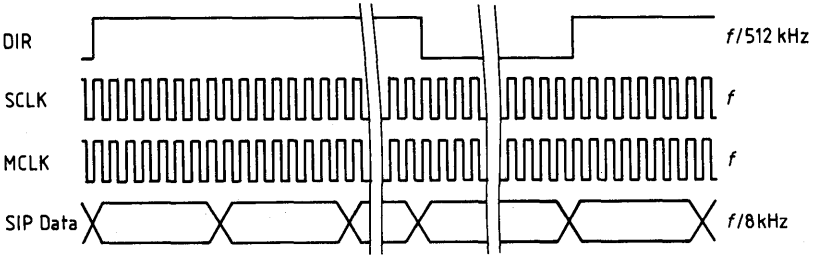
1) SLD-bus Interface[1)]

TEST	SI3	PLL
0	X	X



2) SLD-bus Interface with Variable Clock-frequencies[2)]

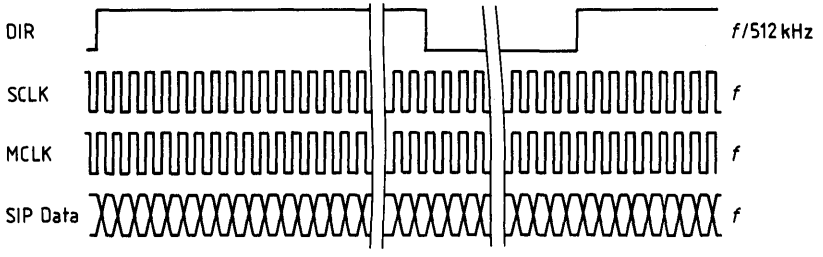
TEST	SI3*	PLL
1	0	0



3) Burst Mode Interface[2)]

TEST	SI3*	PLL
1	0	1

*) SI3 cannot be used as Signalling pin

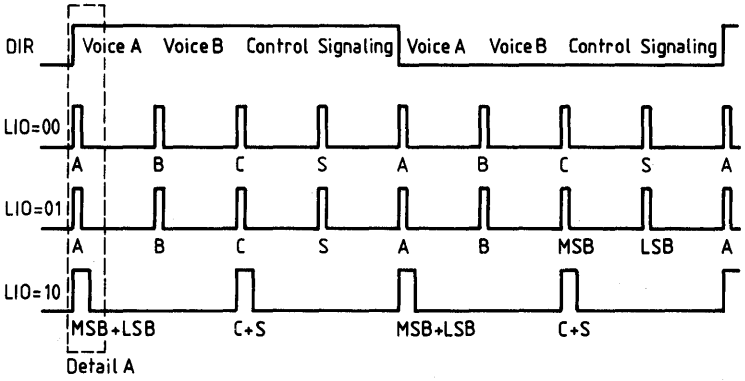


1) 4096-kHz Masterclock MCLK is generated from 512-kHz SCLK by on chip PLL
2) Maximum MCLK-frequency = 8 MHz

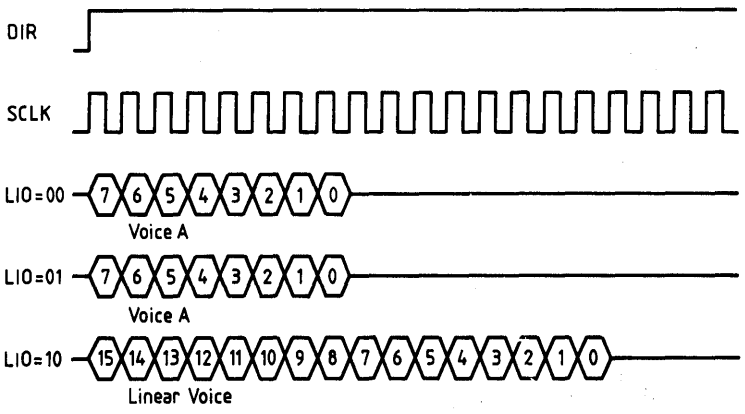
Appendix A (cont'd)

In burst-mode 8- or 16-bit bursts are received or transmitted, depending on the linear mode selected (**see** field LIO in **CR3**).

Figure 17



Detail A



A... voice A C...control
B... voice B S...signaling
MSB... bit 15 – 18 of linear in- or output
LSB... bit 7 – 0 of linear in- or output

Appendix B

On Chip Sine-Wave Generation

By setting field TM3 in CR4 to '100' the on-chip sine-wave generator is activated with a fixed frequency of 2 kHz. The frequency f_{SIN} may be programmed via the R-filter coefficients (R-filter enabled) in the range of 0..4 kHz. The gain may be adjusted with the programmable GR-filter.

The trapezoidal sine-wave generation algorithm used, provides for a harmonic distortion better than 27 dB.

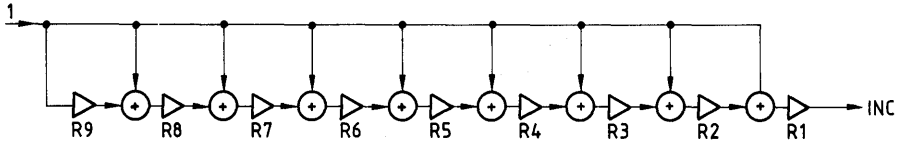
Calculation of the R-filter Coefficients:

f_{SIN}: $= 8192 * INC/f_{MCLK}$ with f_{MCLK}, f_{SIN} [kHz]

$INC := S_{R1} * 2^{-EXP_{R1}} * (1 + S_{R2} * 2^{-EXP_{R2}} * (1 + S_{R3} * 2^{-EXP_{R3}} * (..(.. (1 + S_{R9} * 2^{-EXP_{R9}}) ..))$

S...SIGN, EXP...EXPONENT

Figure 18



$A_1 = INC$

FOR i: = 1 TO 9 DO

FIND S_i, EXP_i : FOR $(|A_i - S_i * 2^{-EXPi}|) = MIN$; $S_i \epsilon (-1,1)$, $EXP_i \epsilon (0...7)$

$A_{i+1} := (A_i/S_i * 2^{-EXPi}) - 1$

$R_i := [(-S_i + 1)/2), BIN(EXP_i)]$ (to be transfered to the SICOFI)

NEXT i

Programming Byte Sequence for Selected Frequencies

Frequency	2000	1000	800	697	700	852	941	1209	1336	1477	1633
COP write	AB	AB	AB	AB	AB	AB	AB	AB	AB	AB	AB
X	00	00	00	00	00	00	00	00	00	00	00
X X	00	00	00	00	00	00	00	00	00	00	00
X X	00	00	00	00	00	00	00	00	00	00	00
R_1 X	00	10	10	20	10	10	10	10	10	10	00
R_3 R_2	8F	8F	AA	A1	CA	3B	CC	B2	22	D1	1B
R_5 R_4	8F	8F	AA	2B	32	C1	BB	22	A1	C1	5C
R_7 R_6	8F	8F	AA	4B	2D	BB	12	5F	5F	BB	CA
R_9 R_8	8F	8F	AA	B1	B3	12	DA	8F	1B	12	13

X...don't care

Dual Channel Codec Filter (SICOFI-2) PEB 2260

Preliminary Data CMOS IC

Type	Ordering Code	Package
PEB 2260-N	Q67100-H6067	PL-CC-28 (SMD)

The Dual Channel Codec Filter PEB 2260 (SICOFI®-2) is a fully integrated PCM codec and filter fabricated in low power CMOS technology for applications in digital communication systems. Based on an advanced digital filter concept, the PEB 2260 provides excellent transmission performance and high flexibility. The digital signal processing approach includes attractive programmable features such as transhybrid balancing, impedance matching, gain and frequency response correction.

The SICOFI-2 can be programmed to communicate either with SLD or with IOM®2 compatible PCM interface controllers (e.g. PEB 2050/51/52/55).

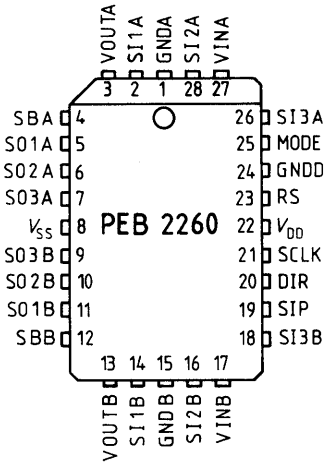
The device bridges the gap between analog and digital voice signal transmission in modern telecommunication systems.

High performance oversampling Analog-to-Digital Converter (ADC) and Digital-to-Analog Converter (DAC) provide the conversion accuracy required. Analog antialiasing Prefilters (PREFI) and smoothing Postfilters (POFI) are included. The dedicated on chip Digital Signal Processor (DSP) handles all the algorithms necessary, e.g. PCM bandpass filtering, sample rate conversion and PCM companding. The SLD/IOM-2 interface handles digital voice transmission, SICOFI-2 feature control and access to the SICOFI-2 signal pins. Specific filter programming is done by downloading coefficients to the coefficient RAM (CRAM).

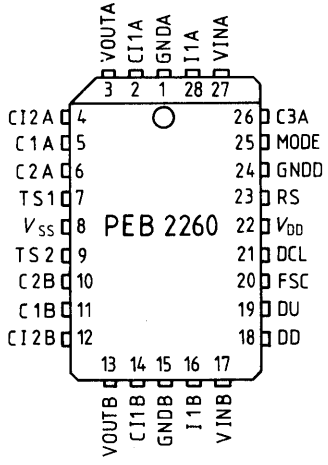
Features

- Dual channel single chip codec and filter
- Band limitation according to CCITT and AT&T recommendations
- Digital signal processing techniques
- PCM encoded digital voice transmission (A-law or μ-law)
- Programmable digital filters for
  - Impedance matching
  - transhybrid balancing
  - gain
  - frequency response correction
- SLD- and IOM2-interface
- Programmable signaling interface to peripherals (e.g. SLIC)
- High performance A/D and D/A conversion
- Programmable analog gain
- Advanced test capabilities, per channel
  - three digital loop back modes
  - two analog loop back modes
  - two programmable tone generators
- No trimming or adjustments
- No external components
- Advanced low power CMOS technology
- Power supply +/−5 V

Pin Configuration for SLD Mode
(top view)



Pin Configuration for IOM-2 Mode
(top view)



Pin Definitions and Functions for SLD Mode

Pin No.	Symbol	Input (I) Output (O)	Function
22	V_{DD}	I	Power supply +5 V
8	V_{SS}	I	Power supply −5 V
24	GNDD	I	Ground digital. Not internally connected to GNDA or GNDB. All digital signals are referred to this pin.
1	GNDA	I	Ground analog channel A. Not internally connected to GNDD or GNDB. All channel A analog signals are referred to this pin.
15	GNDB	I	Ground analog channel B. Not internally connected to GNDD or GNDA. All channel B analog signals are referred to this pin.
27	VINA	I	Channel A analog voice input
3	VOUTA	O	Channel A analog voice output
17	VINB	I	Channel B analog voice input
13	VOUTB	O	Channel B analog voice output
25	MODE	I	Operating mode selection, connected to ground.

Pin Definitions and Functions for SLD Mode (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
21	SCLK	I	Slave clock
20	DIR	I	Direction signal, 8-kHz-frame synchronization.
19	SIP	I/O	Serial interface port, bidirectional serial data port.
23	RS	I	Reset input, RS forces the SICOFI-2 to basic settings.
2 28 26 14 16 18	SI1A SI2A SI3A SI1B SI2B SI3B	I I I I I I	Signaling input: Data present at SI1A...SI3B are sampled and transmitted via the serial interface
5 6 7 11 10 9	SO1A SO2A SO3A SO1B SO2B SO3B	O O O O O O	Signaling output: Data received via the serial interface are latched and fed to SO1A...SO3B.
4 12	SBA SBB	I/O I/O	Bidirectional signaling pin: SBA, SBB pins may be programmed as input or output individually with adequate SICOFI-2 status settings.

Pin Definitions and Functions for IOM-2 Mode (cont'd)

Pin No.	Symbol	Input I Output (O)	Function
22	V_{DD}	I	Power supply +5 V
8	V_{SS}	I	Power supply −5 V
24	GNDD	I	Ground digital. Not internally connected to GNDA and GNDB. All digital signals are referred to this pin.
1	GNDA	I	Ground digital channel A. Not internally connected to GNDD and GNDB. All channel A analog signals are referred to this pin.
15	GNDB	I	Ground analog channel B. Not internally connected to GNDD and GNDA. All channel B analog signals are referred to this pin.

Pin Definitions and Functions for IOM-2 Mode (cont'd)

Pin No.	Symbol	Input I Output (O)	Function
25	MODE	I	Operating mode selection, connected to V_{DD}.
27	VINA	I	Channel A analog voice input to transmit path
3	VOUTA	O	Channel A analog voice output of the received digital voice
17	VINB	I	Channel B analog voice input to transmit path
13	VOUTB	O	Channel B analog voice output of the received digital voice
21	DCLK	I	Data clock
20	FSC	I	Frame synchronisation clock
19	DU	O	Data upstream, serial data port output
18	DD	I	Data downstream, serial data port input
23	RS	I	Reset input, active high RS forces the SICOFI-2 to power down mode and resets the configuration registers
28 16	I1A I1B	I I	Indication input: Data present at I1A...I1B are sampled and transmitted via the serial interface.
5 6 26 11 10	C1A C2A C3A C1B C2B	O O O O O	Command output: Data received via the serial interface are latched and fed to C1A...C3A and C1B...C2B.
2 4 14 12	CI1A CI2A CI1B CI2B	I/O I/O I/O I/O	Bidirectional command/indication pin: C/1A...CI2B pins may be programmed as input or output individually with adequate SICOFI-2 status settings.
7 9	TS1 TS2	I I	Time-slot selection pin 1..2.

IOM-2 – Operating Modes

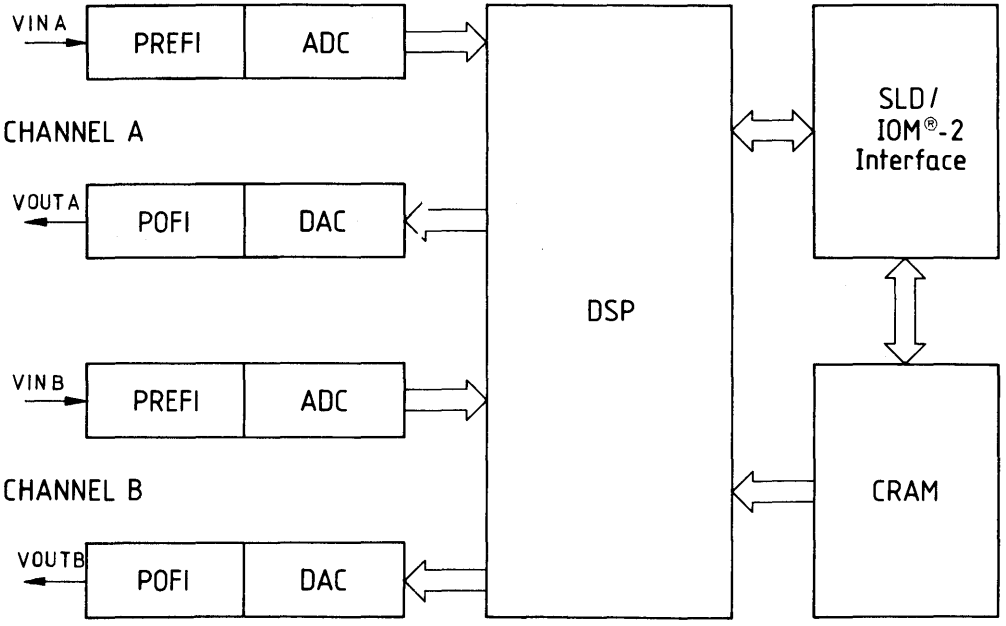
The SICOFI-2 is able to operate IOM-2-interfaces with two different Data Clock (DCL) frequencies (512 kHz or 4096 kHz). Time-Slot Assignment of 8 time slots is available with 4096-kHz DCLK frequency.

The IOM-2-operating mode and time-slot selection is set up by pin-strapping of two pins TS1 and TS2, which work with ternary logic (–5 V, 0 V and +5 V).

TS1	TS2	
N	N	'Slow' IOM-mode (DCLK = 512 kHz)
O	O	'Fast' IOM-mode, time slot 0 selected
O	N	'Fast' IOM-mode, time slot 1 selected
P	O	'Fast' IOM-mode, time slot 2 selected
P	N	'Fast' IOM-mode, time slot 3 selected
O	P	'Fast' IOM-mode, time slot 4 selected
N	O	'Fast' IOM-mode, time slot 5 selected
P	P	'Fast' IOM-mode, time slot 6 selected
N	P	'Fast' IOM-mode, time slot 7 selected

N... –5 Volt (V_{SS}) applied to pin TS1/TS2
0... 0 Volt (GNDD) applied to pin TS1/TS2
P... +5 Volt (V_{DD}) applied to pin TS1/TS2

Block Diagram



Transmission Characteristics

The target figures in this specification are based on the subscriber-line board requirements. The proper adjustment of the programmable filters (transhybrid balancing B; line termination Z; frequency-response correction: X, R) needs a complete knowledge of the SICOFI-2's analog environment. Unless otherwise stated, the programmable filters have the following transfer functions:

$H(Z) = H(B) = 0$; $H(X) = H(R) = H(GR) = H(GX) = H(AGR) = H(AGX) = 1$

A 0 dBm0 signal is equivalent to 1.5763 [1.5710] Vrms. A 3.14 [3.17] dBm0 signal is equivalent to 2.263 Vrms which corresponds to the overload point of 3.2 V. (A-law,[μ-law]).

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Gain (either value) $R_L > 1$ kΩ Gain absolute 1 kHz at 0 dBm0 300 Ω $< R_L <$ 1 kΩ	G	−0.15 −0.25	0 0	0.15 0.15	dB
Gain variation with supply voltage and temperature 1 kHz at 0 dBm0	G_V	−0.15	0	0.15	dB
Total harmonic distortion[1]	THD			−44	dB
Intermodulation $2f_1 - f_2$ [2] $2f_1 - f_2$ [3]	 IMD IMD			 −44 −50	 dB dB
Crosstalk between individual channels 0 dBm0 f = 300 Hz to 3400 Hz	CT			−70	dB
Idle channel noise psophometric weighted transmit receive[4]	 N_{RP} N_{RP}			 −67 −78	 dBm0p dBm0p

1) Single-frequency components between 300 Hz and 3400 Hz produced by a 0 dBm0 sine wave in the range between 300 Hz and 3400 Hz.
2) Equal input levels in the range between −4 dBm0 and −21 dBm0; different frequencies in the range between 300 Hz and 3400 Hz.
3) Input level −9 dBm0, frequency range 300 Hz to 3400 Hz and −23 dBm0, 50 Hz.
4) Test conditions to be defined.

Attenuation Distortion

Attenuation deviations stay within the limits in the figures below.

Figure 1

Receive: Reference frequency 1 kHz, input signal level 0 dBm0

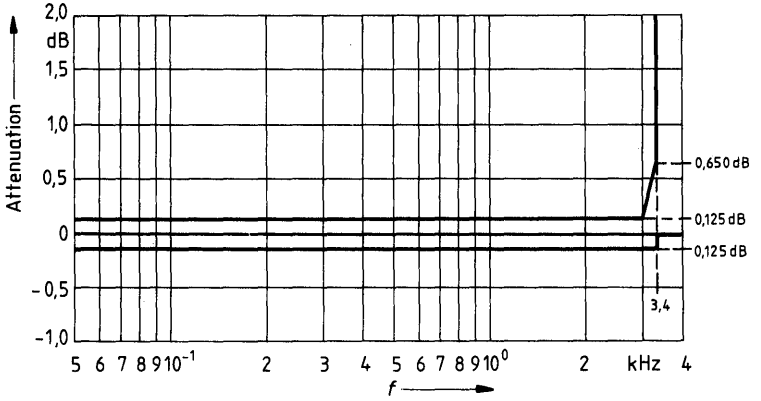
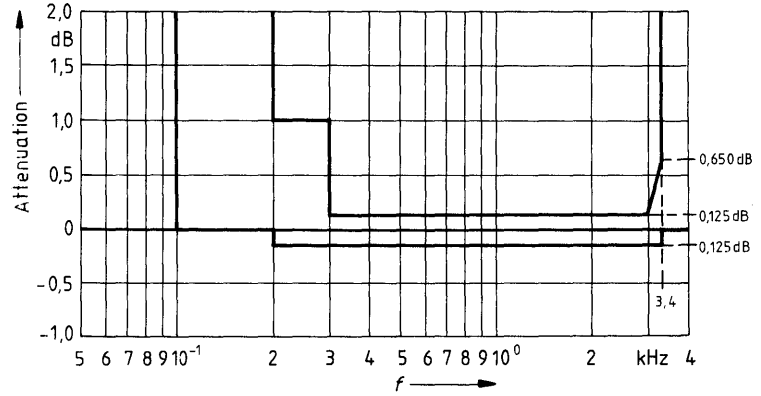


Figure 2

Transmit: Reference frequency 1 kHz, input signal level 0 dBm0



Gain Adjustment

Transmit gain values GX are programmable from 0 to 8 dB in steps ≤0.25 dB. Receive gain values GR are programmable from 0 to −8 dB in steps ≤0.25 dB. Together with the analog gain adjustments AGX, AGR (0, 6, 12, 14 dB) the SICOFI-2 offers a programming range of 22 dB.

Group Delay

Maximum delays for operating the SICOFI-2 with H(B) = H(Z) = 0 and H(R) = H(X) = 1, including delay through A/D- and D/A converters. Specific filter programming may cause additional group delays.

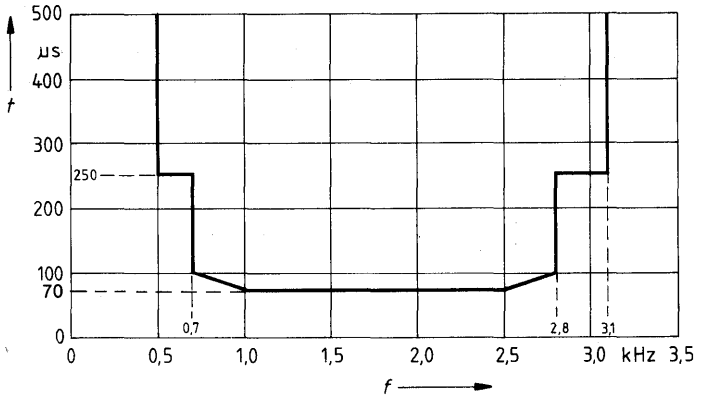
Group delay deviations stay with the limits in the figures below.

Group Delay Absolute Values: Input signal level 0 dBm0

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Transmit Delay $f = 1.4$ kHz	D_{XA}			340	µs
Receive Delay $f = 300$ Hz	D_{RA}			280	µs

Figure 3

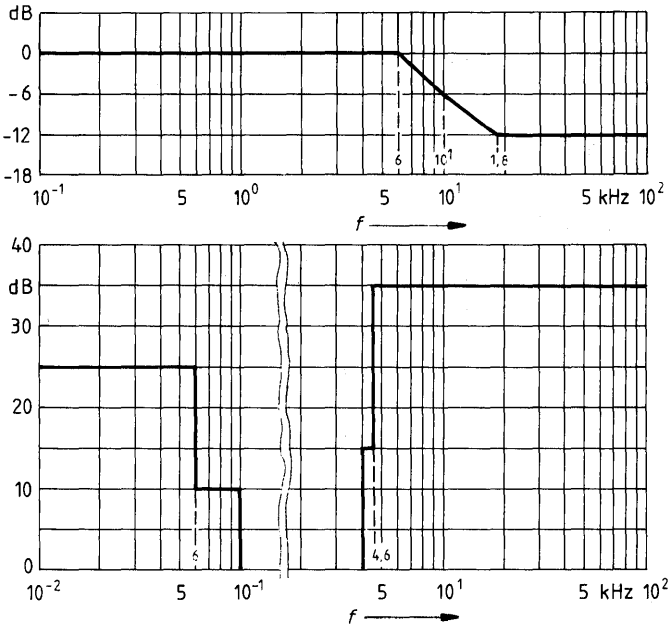
Group Delay Distortion: Input signal level 0 dBm0



Out-of-Band Signals at Analog Input

With an out-of-band sine wave signal with frequency *f* and level A applied to the analog input, the level of any resulting frequency component at the digital output will stay at least X dB below level A.

Figure 4



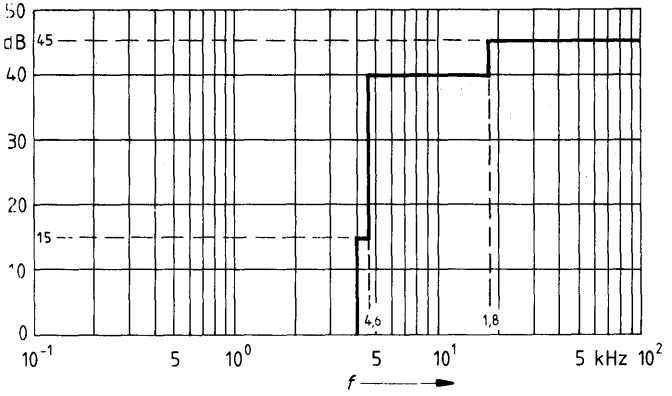
Maximum input level A at analog input

Transmit out-of-band discrimination X

Out-of-Band Signals at Analog Output

With a 0 dBm0 sine wave of frequency *f* applied to the digital input, the level of any resulting out-of-band signal at the analog output will stay at least X dB below a 0 dBm0, 1 kHz sine wave reference signal at the analog output.

Figure 5



Receive out-of-band discrimination X

Gain Tracking (Receive and Transmit)

The gain deviations stay within the limits in the figures below

Figure 6

Gain Tracking: Measured with noise signal according to CCITT recommendations
Reference level is −10 dBm0

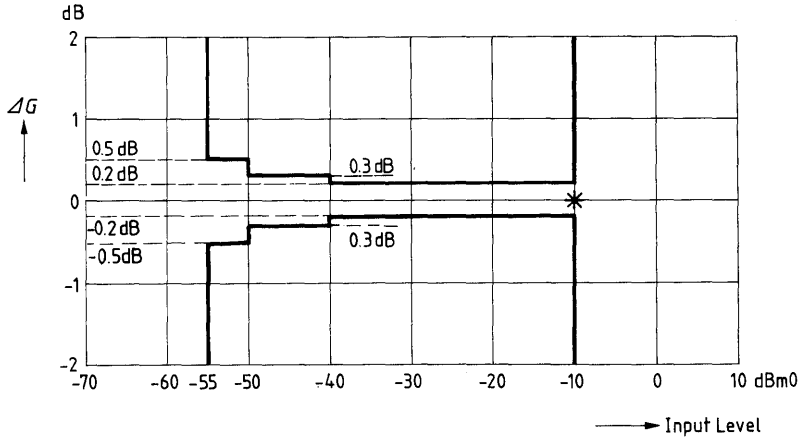
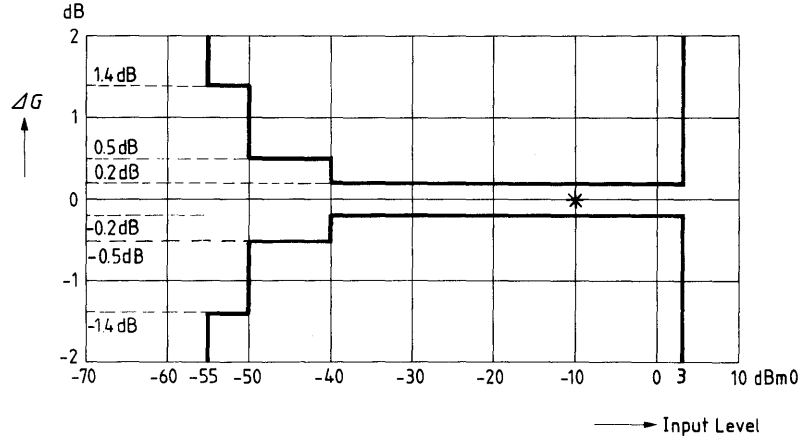


Figure 7

Gain Tracking: Measured with sine wave in the range 700 to 1100 Hz
Reference level is −10 dBm0



Total Distortion (Receive and Transmit)

The signal-to-distortion ratio exceeds the limits in the following figures.

Figure 8

Total Distortion: Measured with noise signal according to CCITT recommendations

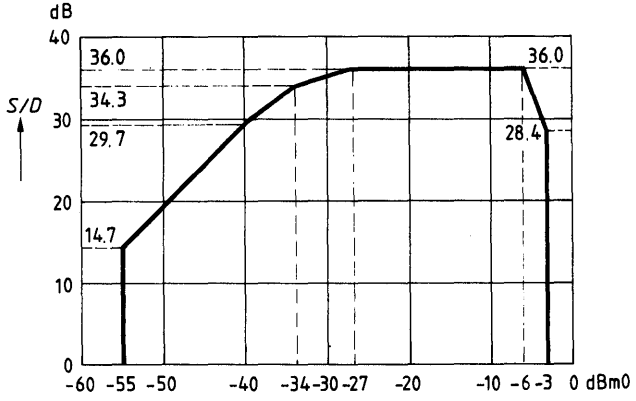
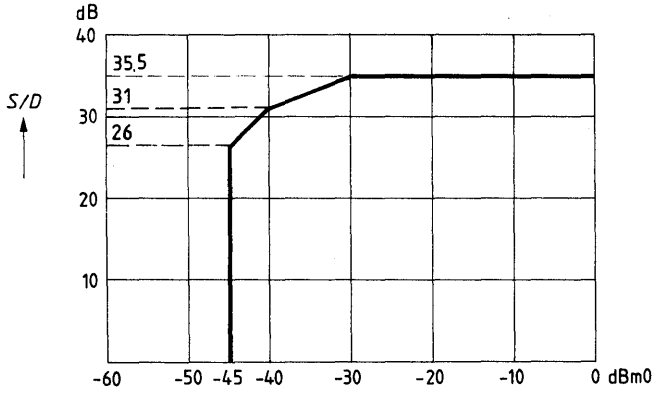


Figure 9

Total Distortion: Measured with sine wave in range 700 to 100 Hz



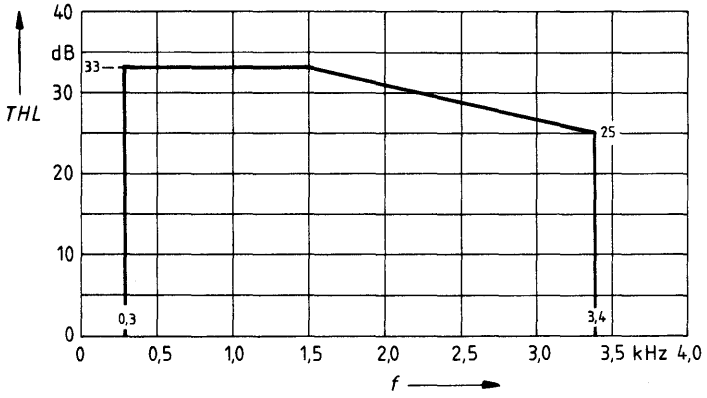
Transhybrid Loss

The quality of transhybrid-balancing is very sensitive to deviations in gain and group delay.

The SICOFI-2 transhybrid-loss is measured the following way: A sine wave signal with level A and a frequency in the range of 300-3400 Hz is applied to the digital input. The resulting analog output signal at pin V_{OUT} is directly connected to V_{IN} e.g. with the SICOFI-2 testmode "Digital Loop Back via Analog Port" **(see CR3)**. The programmable filters R, Gr, X, Gx and Z are disabled, H(AGR) = H(AGX) = 1 and the balancing filter B is enabled with coefficients optimized for this configuration $V_{IN} = V_{OUT}$).

The resulting echo measured at the digital output is at least X dB below the level of the digital input signal as shown in the following figure.

Figure 10



Note:

B-filter coefficients recommended for transhybrid loss measurement with $V_{OUT} = V_{IN}$:

B-filter part 1 (03) = see PEB 2060 pp. 185
B-filter part 2 (08) = see PEB 2060 pp. 185
B-filter Delay (18) = see PEB 2060 pp. 185

Absolute Maximum Range

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit
V_{DD} referred to GNDD		−0.3	5.5	V
V_{SS} referred to GNDD		−5.5	0.3	V
GNDA, GNDB to GNDD		−0.3	0.3	V
Analog input and output voltage				
referred to $V_{DD} = 5$ V; $V_{SS} = -5$ V	V_{IN}	−10.3	0.3	V
referred to $V_{SS} = -5$ V; $V_{DD} = 5$ V	V_{IN}	−0.3	10.3	V
All digital input voltages				
referred to GNDD = 0 V; $V_{DD} = 5$ V	V_{IN}	−0.3	5.3	V
referred to $V_{DD} = 5$ V; GNDD = 0 V	V_{IN}	−5.3	0.3	V
Power dissipation	P_D		1	W
Storage temperature	T_{stg}	−60	125	°C
Ambient temperature under bias	T_A	−10	80	°C

Operating Range

$T_A = 0$ to 70 °C; $V_{DD} = 5$ V ± 5%; $V_{SS} = -5$ V ± 5%; GNDD = 0 V; GNDA = 0 V

Parameter	Symbol	Limit Values min.	Limit Values typ.	Limit Values max.	Unit	Test Conditions
V_{DD} supply current	I_{DD}					
standby			0.5	0.8	mA	± 5% supply
operating			14	20	mA	± 5% supply
V_{SS} supply current	I_{SS}					
standby			0.1	0.2	mA	± 5% supply
operating			10	15	mA	± 5% supply
Power supply rejection (of either supply/direction)	*PSRR*	35			dB	1 kHz 80 mV_{rms} ripple
Power dissipation standby	P_{Ds}		3	5	mW	± 5% supply
Power dissipation operating	P_{Do}		120	175	mW	± 5% supply

Digital Interface

$T_A = 0$ to 70 °C; $V_{DD} = 5\ V \pm 5\%$; $V_{SS} = -5\ V \pm 5\%$; GNDD = 0 V; GNDA = 0 V

Parameter	Symbol	Limit Values		Unit
		min.	max.	
L-input voltage	V_{IL}	−0.3	0.8	V
H-input voltage	V_{IH}	2.0	V_{DD} +0.3	V
L-output voltage $I_O = -2$ mA	V_{OL}		0.45	V
H-output voltage $I_O = 400\ \mu A$	V_{OH}	2.4		V
Input leakage current $-0.3 \le V_{IN} \le V_{DD}$	I_{IL}		±1	µA

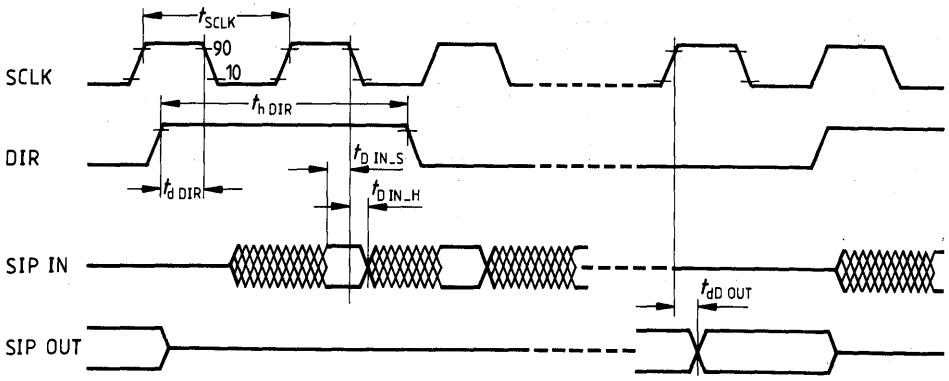
Analog Interface

$T_A = 0$ to 70 °C; $V_{DD} = 5\ V \pm 5\%$; $V_{SS} = -5\ V \pm 5\%$; GNDD = 0 V; GNDA = 0 V

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Analog input resistance	R_I	10		MΩ
Analog output resistance	R_O		10	Ω
Input offset voltage	V_{IO}		±50	mV
Output offset voltage	V_{OO}		±50	mV
Input voltage range	V_{IR}		±3.2	V
Output voltage range $R_L \ge 300\ \Omega$; $C_L \le 50$ pF	V_{OR}	±3.1		V

SLD-Bus Interface Timing

Figure 11

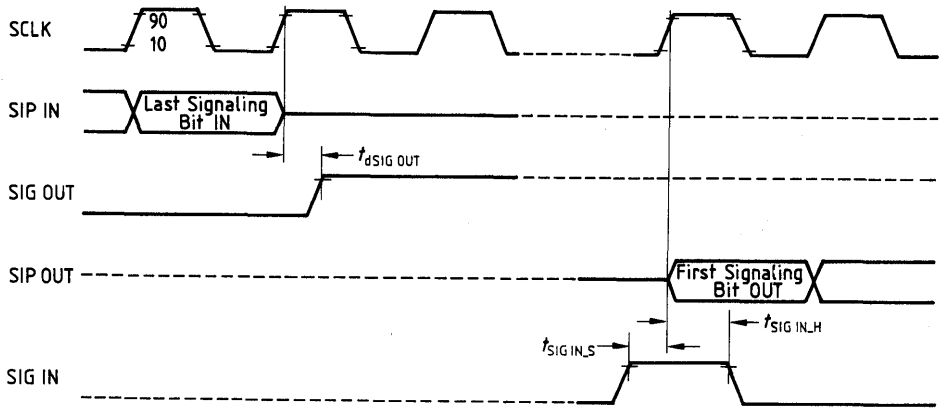


Switching Characteristics

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Period SCLK	t_{SCLK}		1/512 kHz		
Duty Cycle		10		90	%
Period DIR	t_{DIR}		125		µs
DIR delay timw	t_{dDIR}	+20			ns
DIR high time	t_{hDIR}	500			ns
SIP data in setup time	$t_{DIN\,S}$	50			ns
SIP data in hold time	$t_{DIN\,H}$	0			ns
Thermal resistance junction to ambient	t_{dDOUT}			200	ns
SIP data out tristate delay vs. SCLK				50	ns
RS high time		250			ns

Signaling Interface Timing

Figure 12



Switching Characteristics

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Delay signaling out vs. SCLK[1])	$t_{dSIGout}$			200	ns
SIG in setup time[2])	$t_{SIGin\ S}$	50			ns
SIG in hold time[2])	$t_{SIGin\ H}$	100			ns

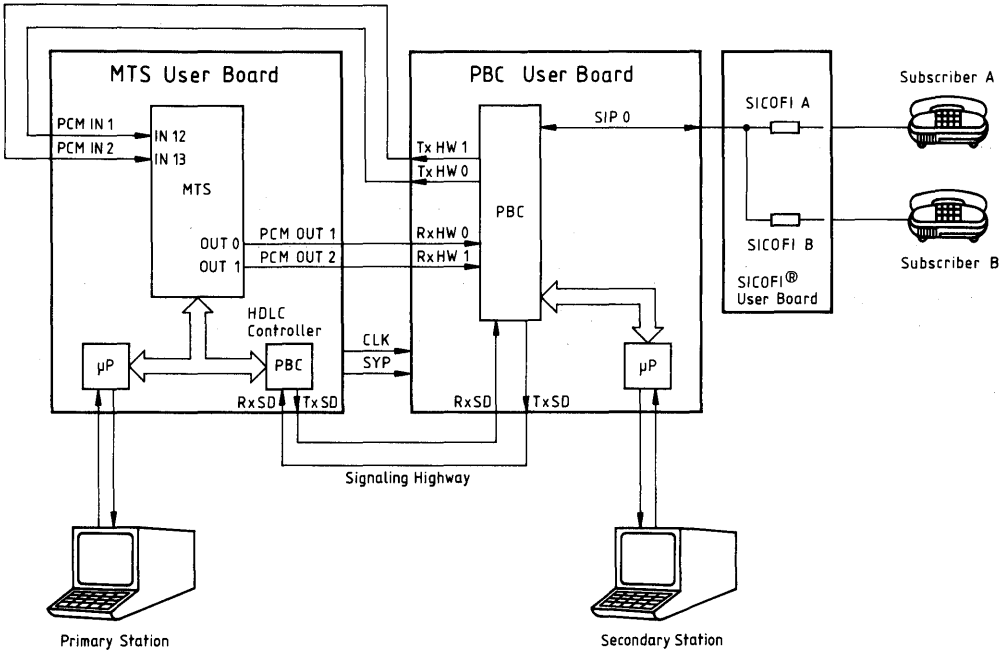
1) Pins SO1A...SO3B; Pins SBA, SBB as output
2) Pins SI1A...SI3B; Pins SBA, SBB as input

Application Support for Exchange ICs STU 2050

The Siemens Telecom User Boards (STU 20xx family) provide quick and convenient introduction to the complex device functions. They allow all important functions to be tested in a system-like configuration with the existing software and a terminal with an RS 232 C/V.24 serial interface as well as application specific software to be developed with a microprocessor system.

The Siemens Telecom Software (STS 2060) is a FORTRAN program for calculating the coefficients of the programmable filters in the SICOFI® PEB 2060 in consideration of the various subscriber line parameters.

MTS, PBC and SICOFI® Boards



PBC User Board STU 2050

Type	Ordering Code
STU 2050	Q67100-Z166

The PBC is connected as a peripheral device to a SAB 8031 µP system. This allows the user to do programming himself. Thus the PBC caters for special application conditions. This requires the use of a µC development system with an ICE-51 in-circuit emulator. The I/O unit has an RS 232 C/V.24 interface (receiver, transmitter). Without a µC development system the user board can also be used with the existing software, connected to a terminal with a serial interface. The terminal acting as an I/O unit calls the PBC registers by the corresponding names e.g. ABR = 78. By this means, the different PBC functions can be set or data can be read or written (e.g. time-slot assignment, PCM-mode switching, HDLC protocol, reading of status register).

The User Board Circuit Provides the Following Functions:

- PCB: Peripheral Board Controller PEB 2050
- µC: microcomputer SAB 8031 (SAB 8051) with program memory and driver
- MUX: multiplexer for selecting the SIP serial interface port lines
- EX1, EX2: two exchange connections with control logic

The following interfaces help execute the various functions on the board:

- Dual PCM interface (highway HW 0, HW 1)
- Fast serial interface (HDLC)
- Serial interface with the microcomputer (receiver, transmitter)
- Codec interface (CHA Rec, CHB Rec and so on) via exchange connection 1, (EX 1)

Serial Interface with Microcomputer

Any terminal or teletype with an RS 232 C/V.24 interface (25-pin D-subminiature connector) can be connected to the serial interface. The following baud rates can be set by DIL switches:

300, 1200, 2400, 3600 Bd.

Codec Interface
(exchange connections 1 and 2)

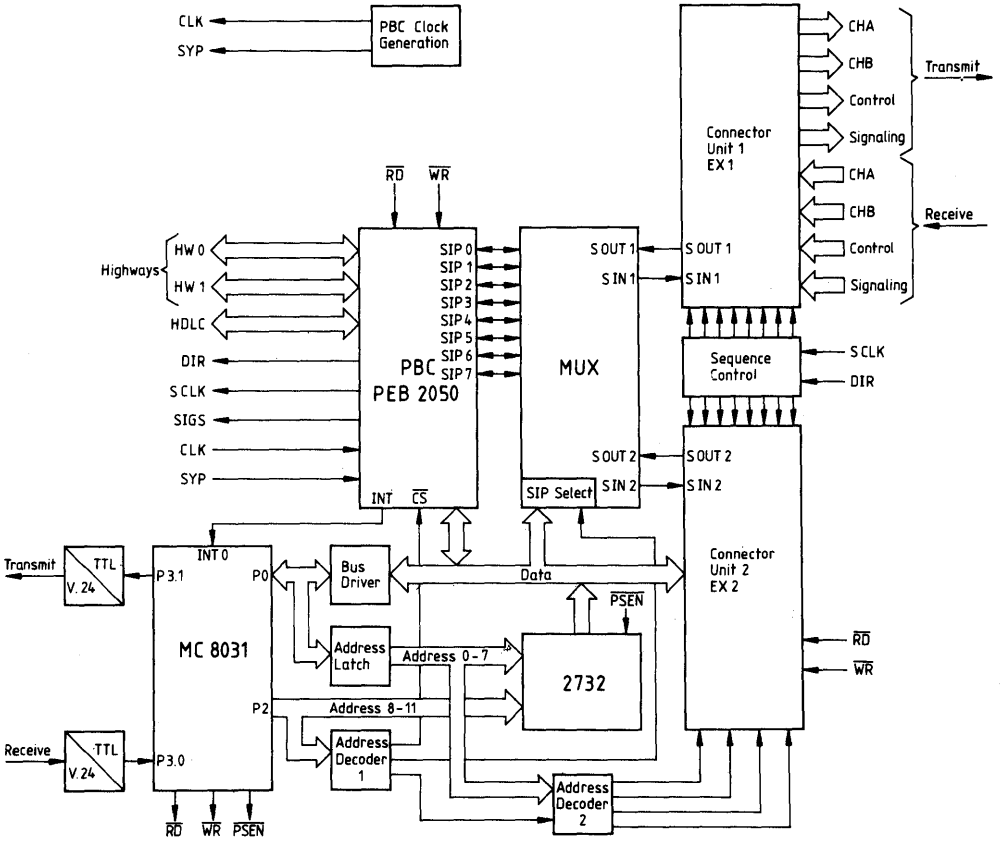
In the exchange connections the serial data coming from the PBC are converted to parallel form and loaded into the corresponding registers. Thus data for channel A (CHA), channel B (CHB), control and signaling are then ready for use as parallel 8-bit data (receive direction). In the reverse direction the parallel 8-bit data are converted into serial form and transmitted to the PBC (transmit direction). The 8-bit receive and transmit data of connection 1 are fed to a plug connector and are available for the user in the hardware. Here the user can connect different codecs and peripheral circuits.

Exchange connection 2 feeds the data to the µC data bus. The microcomputer can call the data with a corresponding address.

Features

- PBC PEB 2050 onboard
- SAB 8031 microprocessor system
- 32-Kbyte EPROM (program memory)
- Two universal interfaces for connecting peripheral circuits and PCM or signaling highways
- Serial interface RS 232 C/V.24 with selectable baud rates of 300, 1200, 2400, 9600 Bd
- Selectable PCM clock (2.048 MHz or 4.096 MHz)
- Power supply:
  +5 V ± 5%, 1.5 A central supply
  ± 12 V ± 5%, 0.1 A for RS 232 C interface
- Delivered with a detailed user manual

PBC User Board



SICOFI User Board STU 2060

Type	Ordering Code
STU 2060	Q67100-H3238

With the SICOFI® and the PBC user board an analog subscriber line circuit is generally implemented. A subscriber branch contains a **S**ubscriber **L**ine **I**nterface **C**ircuit (SLIC) and a **S**ignal **P**rocessing **C**odec **F**ilter (SICOFI).

Telephone terminals are connected by the a and b wires to the subscriber line circuit, which implements primarily the line matching, the 2/4-wire conversion and A/D or D/A conversion of the voice signals. Control and supervision functions can additionally be performed by means of programmable input/output pins of the SICOFI.

STU 2060 can be broken down into four subscriber line circuits, connected by the SIP lines of the SICOFI devices of the PBC on the STU 2050. The latter handles the switching function for the individual voice channels and, in addition, the programming of the SICOFI devices is performed by way of the PBC.

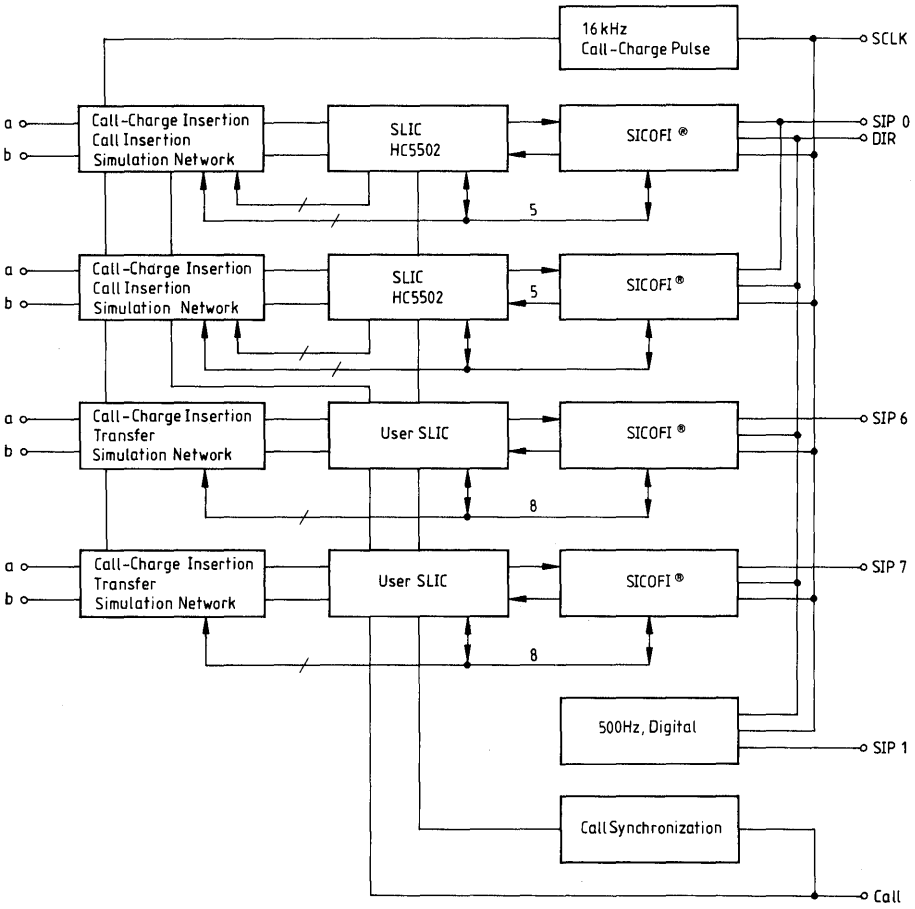
On the user board the Harris SLIC HC5502 is incorporated in two of the four subscriber branches, while the other two subscriber branches are fitted with a user SLIC. Seeing as the two supplied transformer SLICs are plugged into the user board, the user can simply plug a self developed SLIC into a socket in order to check in transfer functions of the SLIC in conjunction with the SICOFI.

The advantage of the SICOFI user board is thus that the user can quickly become familiar with the functioning of the SICOFI and also with the use of the SICOFI in a system environment made up of SLIC and PBC.

Features

- Four SICOFI PEB 2060 on board
- Four analog subscriber lines
- Two electronic SLICs
  Harris HC 5502 on board
- Two transformer SLICs on board
- Customer can develop his own SLICs on two plug-in modules
- Interface for four telephones
- Digital 500-Hz tone
- 16-kHz pulse for maintenance
- Zero level detection for switching the ring voltage

SICOFI User Board



SICOFI Test Board STUT 2060

Type	Ordering Code
STUT 2060	Q67100-H6058

The SICOFI® test board STUT 2060 offers the possibility of connecting any external customer specific SLICs with the SICOFI for evaluation of customer specific combinations of SLIC and SICOFI. This setup allows measurements and tests covering the transfer functions of the complete subscriber line module.

The board is programmable via an RS 232 interface by a terminal or PC. The registers of PBC and SICOFI can be accessed and therefore the SLIC can be programmed.

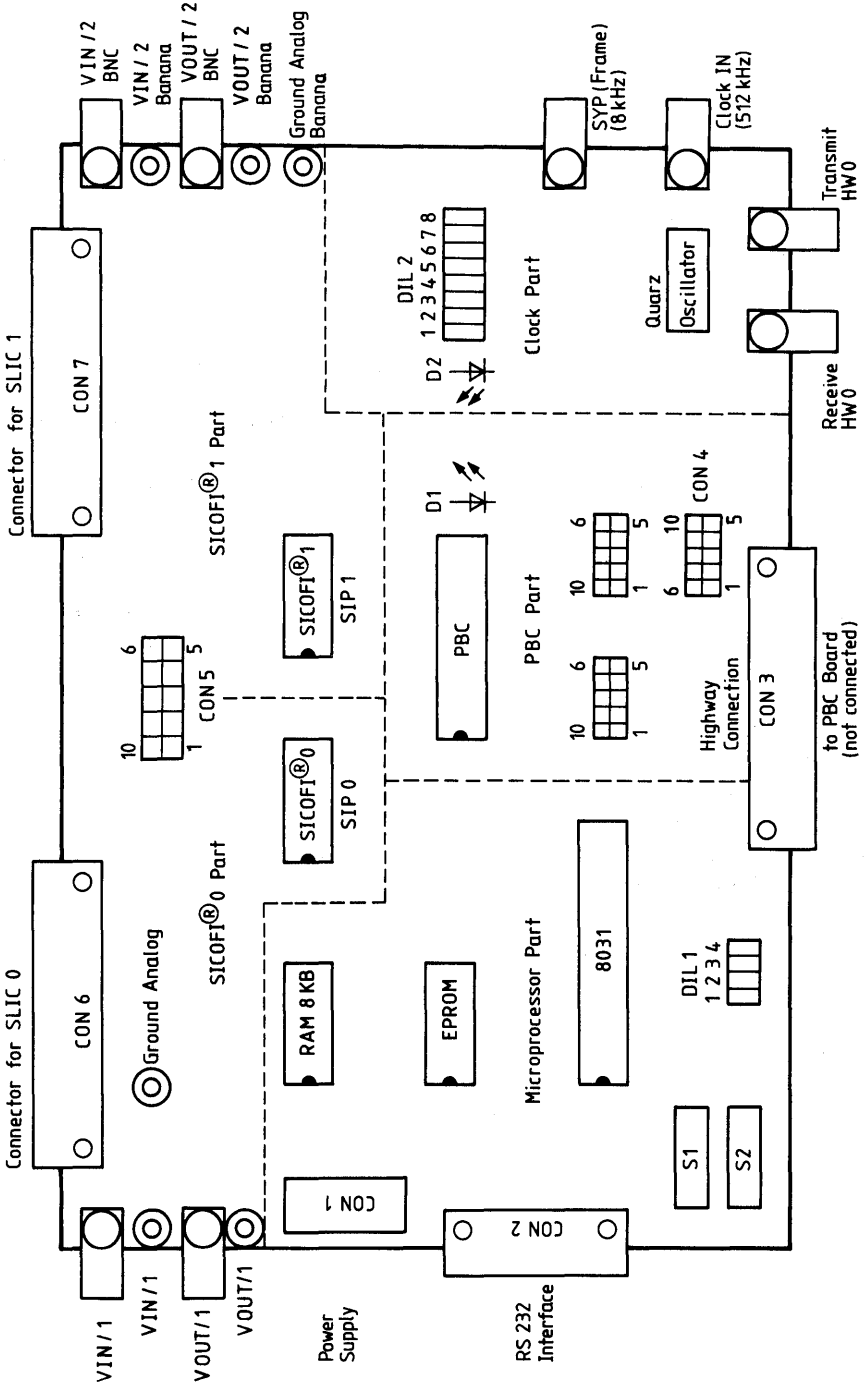
Different customer specific SLICs may be built up separately and may be connected to the SICOFI test board STUT 2060 via a 64-pin connector.

With his specific SLIC program and together with the SICOFI coefficient program STS 2060, the customer is able to calculate SLIC specific programming bytes in order to program and test his SLIC hardware.

Features

- Two SICOFI PEB 2060 and one PBC PEB 2050 on board
- SAB 8031 microprocessor system
- Serial interface RS 232 C
- Two interfaces for connecting customer specific SLIC boards

SICOFI Test Board



ICs for ISDN Exchange Systems

Introduction

The advent of the **I**ntegrated **S**ervices **D**igital **N**etwork (ISDN) and the office of the future has emphasized the need for cost-effective silicon solutions to the problems of simultaneous transmission of digitized voice and data over existing twisted-pair copper wiring. Basic access ISDN can be considered as an international concept which supports two circuit switched 64-kbit/s B channels and a message oriented 16-kbit/s D channel for packetized data, signaling and telemetry information. According to CCITT recommendations, the basic architecture for the subscriber access consists of an exchange and line termination (ET, LT), a remote network termination (NT), a two-wire loop (U interface) between NT and LT and the four-wire link (S interface) which connects the subscriber terminal (TE) with the network termination. The NT equipment serves as a link between the U interface on the exchange and the S interface on the user side.

Typical problems which have to be overcome during the initial phase of ISDN are:

- System implementation calls for a complete chip set supporting the subscriber access.
- Technical and economical demands dictate the use of advanced VLSI technology; manual designs to achieve small chip size result in high development effort.
- The lack of international standards for full-duplex two-wire transmission as well as different application configurations call for highly flexible system architecture.

ISDN Oriented Modular System Architecture

The IOM® architecture and the interfacing of the VLSI circuits are designed according to the following criteria:

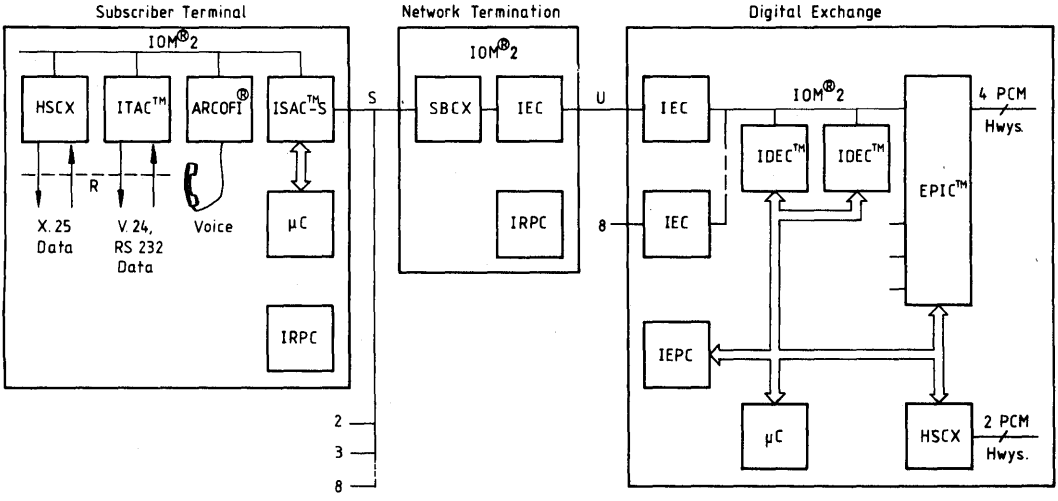
- High modularity ensures flexible interconnection of the devices for different applications.
- Use of identical devices in different applications by mode switching results in a minimum number of individual ICs. The resulting increase in device quantity enables the price reduction crucial to initial ISDN introduction.
- Suitable partitioning in the initial phase permits the implementation of devices of easily managed complexity with regard to development risk, resources and time.
- A well defined **I**SDN **O**riented **M**odular (IOM) interface simplifies system design, provides the security of an industry standard, supports flexible interconnection of the different devices and, moreover, makes the use of different compatible transceivers possible.

Based on the IOM architecture, the product development strategy allowed a step by step introduction of ISDN systems. While in the first step the layer-1 and layer-2 functions for all applications were implemented in separate devices, further optimization and cost reduction has been achieved in a second step by forward integration. The combination of layer-1, layer-2 and further functions on single devices was planned from the beginning of development and was taken into account in the circuit design.

The IOM architecture as introduced, supports the design of equipment for ISDN terminals, terminal adaptors, network terminations and line cards for digital exchange equipment (see figure on the following page).

ISDN Oriented Modular (IOM) Architecture

Second Generation ISDN ICs, IOM®-2 Interface



PEB 2025	ISDN Exchange Power Controller	IEPC
PEB 2055	Extended PCM Interface Controller	EPIC™-1
PEB 2056	Extended PCM Interface Controller	EPIC™-2
PEB 2075	ISDN D-Channel Exchange Controller	IDEC™
PEB 2081	S/T Bus Interface Circuit Extended	SBCX
PEB 2085	ISDN Subscriber Access Controller	ISAC™-S
PEB 2090	ISDN Echo-Cancellation Circuit (4B3T)	IEC-T
PEB 2091	ISDN Echo-Cancellation Circuit (2B1Q)	IEC-Q
PEB 2095	ISDN Burst Transceiver Circuit	IBC
PEB 20950	ISDN Subscriber Access Controller	ISAC™-P
PSB 2110	ISDN Terminal Adaptor Circuit	ITAC™
PSB 2120	ISDN Remote Power Controller	IRPC
PSB 2160	Audio Ringing Codec Filter	ARCOFI®
SAB 82525	High-Level Serial Communications Controller Extended	HSCX

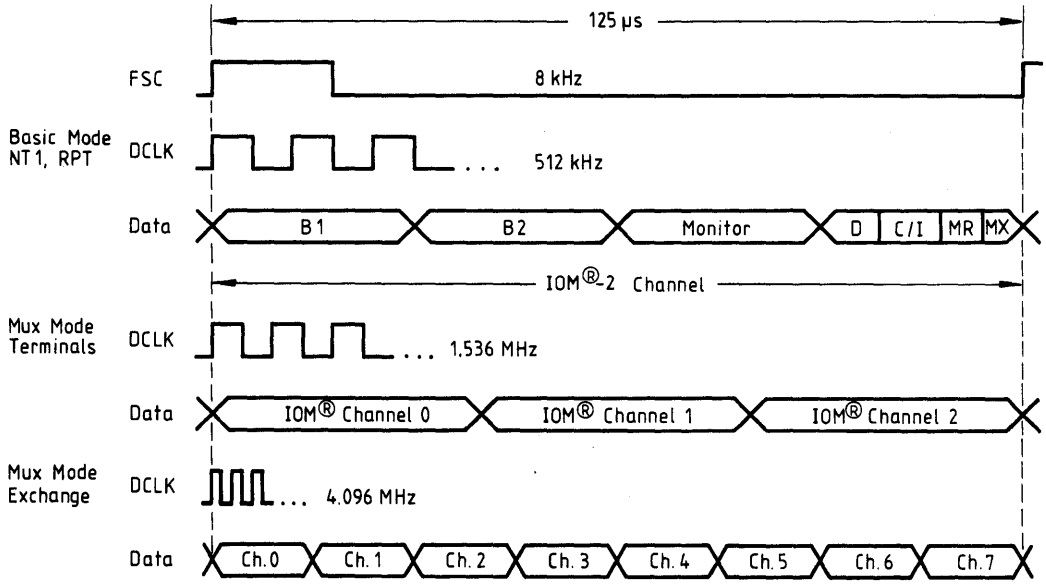
Note: The ISAC-P is used for 2-wire PBX terminals in place of the ISAC-S. Four different transceivers (IEC-T, IEC-Q, SBCX, IBC) are available for different digital exchange subscriber loops (PBX or public, 2- or 4-wire, short or long lines).

The standardized interface which makes all of this flexibility possible is the same IOM interface that was developed by Siemens Semiconductor, but now with some additional features suggested by ALCATEL, Siemens, Plessey and ITALTEL systems designers. The IOM-2 interface is identical to the General Circuit Interface (GCI). GCI is the working name that was used within the "Group of Four" for this interface specification.

The IOM interface now has a flexible data clock. In this way, data transmission requirements are optimized for different applications. Three different clock speeds are used with the Siemens architecture shown below. For a network termination (NT 1), a 512-kHz-clock is used resulting in a data transmission speed of 256 kbit/s. In a single 125 µs frame, one "IOM channel" is transmitted containing the 2B+D channels plus maintenance and control information for a single ISDN subscriber. For terminals, a 1536-kHz clock and a 768-kbit/s data rate enable three complete IOM channels to be transmitted in a single frame. The extra bit rate is used for communication within the terminal (see ISDN terminals). On line cards, a 4096-kHz clock has been selected so that up to eight IOM channels and thus, eight ISDN subscribers can be multiplexed over a single interface.

The C/I channel is used for passing command and indication information for controlling activation/deactivation and switching of test loops. The monitor channel can be used for transmitting maintenance and additional control information. Data transfer in the monitor channel is facilitated by using the bits MR and MX for a "handshaking protocol" to acknowledge the transmission and reception of messages.

IOM-2 Frame Structure



NT 1: Network Termination
RPT: Repeater
C/I : Command / Indication
FSC : Frame Synchronization Clock
DCLK: Data Clock

ICs for the Digital Exchange

In 1985 Siemens introduced the world's first integrated circuits for ISDN system design. Since then, a tremendous amount of experience has been gained both by Siemens and by system designers using these devices.

Building upon this experience, Siemens has now developed a family of second generation ISDN ICs which represents a natural evolution and is based on the tried and proven existing devices.

In 1988, four of the world's largest manufactures of telecommunications equipment (ALCATEL, Siemens, Plessey and ITALTEL systems houses) announced a cooperation on ISDN system design. Recognizing that international and national ISDN standards still leave lots of room for incompatible solutions, these systems houses decided to define key elements of ISDN system design – such as how different ISDN ICs communicate with each other.

Much of this type of definition had already been done by Siemens Semiconductor – and already realized in silicon. On the condition that the standardization agreed upon be compatible with already existing devices, Siemens Semicontuctor participated in the new definition. The resulting specification for ISDN devices and interchip interfacing goes a long way towards simplifying system design, reducing dependence on a single vendor's chips and establishing a badly needed industry standard. Siemens has, available today, the ICs which realize this specification. They are based on tried and proven devices and represent a logical second generation evolution.

A flexible architecture with a well defined interchip interface, enables flexible designs which can support a variety of different transmission lines. Siemens offers four different ISDN transceivers and an advanced codec filter, all compatible with the same industry standard interface.

- **PEB 2081 S/T Bus Interface Circuit Extended (SBCX)**
  Digital transceiver for 4-wire S/T interface according to CCITT recommendations. Based on the PEB 2080 SBC, with enhanced functions like automatic handling of S and Q maintenance bits, extended loop lengths and IOM-2 compability.

- **PEB 2090 ISDN Echo-Cancellation Circuit (IEC-T)**
  Digital transceiver for 2-wire U interface as specified by German Bundespost (4B3T line code). Loop lengths of up to 9.5 km with 0.6 mm wire.

- **PEB 2091 ISDN Echo-Cancellation Circuit (IEC-Q)**
  Digital transceiver for 2-wire U interface as specified by American national standard (2B1Q line code). Loop lengths typically of up to 8 km with 0.6 mm wire.

- **PEB 2095 ISDN Burst Transceiver Circuit (IBC)**
  Digital transceiver for 2-wire U interface for PBX equipment as specified by the German Central Association for Electronics Industry (ZVEI). Loop lengths of up to 3.5 km with 0.6 mm wire.

- **PEB 2260 Signal Processing Codec Filter-2 Channel (SICOFI-2)**
  Advanced codec filter with software programmable digital filters (DSP) and two channels on a single chip. IOM-2 compatible.

D channel signaling information (LAPD) can be optimally handled on exchange line cards by the following device.

- **PEB 2075 ISDN D Channel Exchange Controller (IDEC)**
  Quad HDLC controller for processing of D channels from four separate ISDN subscriber lines.

The interfacing for a large number of subscriber lines, both analog and digital, with internal PCM communications highways can be handled by either of the following key devices.

- **PEB 2055 Extended PCM Interface Controller (EPIC-1)**
  Handles interfacing and time-slot assignment onto internal PCM highways for up to 32 digital (64 analog) subscribers.

- **PEB 2056 Extended PCM Interface Controller (EPIC-2)**
  Smaller version of EPIC-1 with only one IOM-2 interface and two PCM highways. Handles interfacing for up to 8 digital (16 analog) subscribers.

This architecture is completed by the SAB 82825 high-level serial communications controller extended (HSCX). This device is a two-channel HDLC controller which can be used on line cards for interprocessor signaling and processing of D channel data packets.

SIEMENS

ISDN Exchange Power Controller (IEPC) PEB 2025

Preliminary Data **CMOS IC**

Type	Ordering Code	Package
PEB 2025-P	Q67100-H6038	P-DIP-22

The IEPC is an integrated power controller especially designed for feeding two and four wire transmission lines. The IEPC is fully compatible to the CCITT recommendations on power feed at the "S" interface. So the IEPC can be used in PBX/Central Office and in intelligent NTs.

The IEPC supplies power to up to four transmission lines. Each line is individually powered and controlled via a microprocessor interface. An interrupt output signals any malfunction to the microprocessor.

The High Voltage CMOS Technology (60 V) Ensures a Wide Field of Applications

- Two and four wire transmission
- Point-to-point configurations
- Point-to-multipoint configurations

Programmable output current and thermal shut down guards the IEPC against overloads.

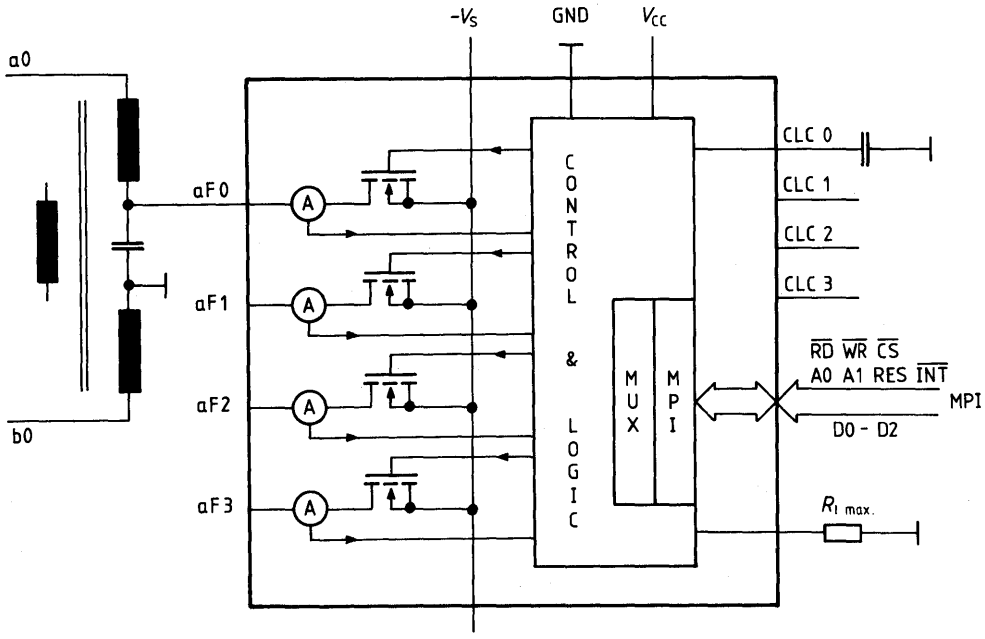
The IEPC offers a special transient permitted overload state. Momentary overloads within a specified range e.g. by connecting a TE to a powered line, will not activate the current limit circuits of the power controller. If overload is detected, the linedriver will turn off according to the time and current dependent turn off characteristic as described in FTZ 1R211.

The IEPC offers an automatic restart mode. In this case, the IEPC tries to power up the line periodically every 10 s, thus the feeding of a line will return automatically after the overload conditions are removed.

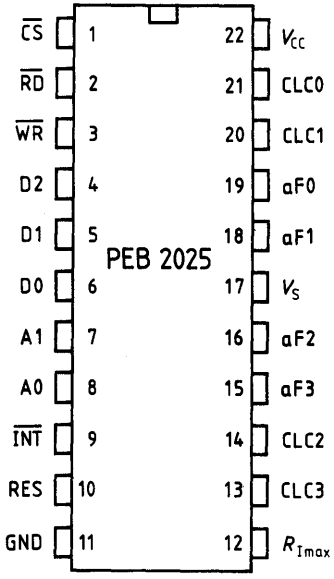
Features

- Supplies power to up to four transmission lines.
- CCITT recommendations compatible for power feed at the "S" interface.
- Each line is individually powered and controlled.
- Wide field of applications.
- Maximum output current programmable up to 100 mA.
- Programmable switch-off-characteristic by overcurrent detection.
- Automatic restart after removing overload conditions.
- Status detectors for each linedriver.
- Microprocessor compatible interface.
- Interrupt output for detection of any malfunction.
- High voltage CMOS technology (60 V).

Figure 1
IEPC Functional Diagram



Pin configuration
(top view)



Pin Definitions and Functions

Pin No.	Symbol	Input (I) Output (O)	Function
17	$-V_S$	I	**Supply Voltage:** This pin has to be connected to the negative supply voltage. $-V_S$ supplies power to all linedrivers.
22 17	V_{CC} GND	I I	**Digital Supply Voltage:** +5 V **Ground** Digital Note: GND has to be connected to ground battery (positive supply voltage).
19, 18 16, 15	aF0-aF3	O	**a**-Line **F**eeding: aF_i are the linedriver outputs
12	$R_{I\ max}$	I	**Current Limit:** Using an external resistor connected between $R_{I\ max}$ and GND, the maximum line current is programmed. This programmed limit is the same to all linedrivers.
21, 20, 14, 13	CLC0-CLC3	I	**C**urrent **L**imit **C**haracteristic: By connecting external capacitors between CLC_i and GND, the time-dependent turn off-characteristics of the linedrivers are defined.
1	$\overline{CS}$	I	**Chip Select:** A logic low on $\overline{CS}$ enables $\overline{RD}$ and $\overline{WR}$ communication between the processor and the IEPC.
3	$\overline{WR}$	I	**Write:** A logic low on this pin when $\overline{CS}$ is low enables the IEPC to accept command words from the processor.
2	$\overline{RD}$	I	**Read:** A low on this pin (if $\overline{CS}$ is low) enables the IEPC to release status onto the data bus for the processor.
6, 5, 4	D0-D2	I/O	**Data Bus:** Control, status and command information is transfered via this bus between IEPC and processor.
8, 7	A0, A1	I	**Address Bus:** These inputs select the internal registers while chip select is active.
10	RES	I	**Reset:** A logic high on the RES input sets the device into the initial state.
9	INT	O	**Interrupt:** Open-drain output. If any malfunction is detected by the IEPC, this interrupt-pin is activ low.

Figure 2
IEPC Architecture

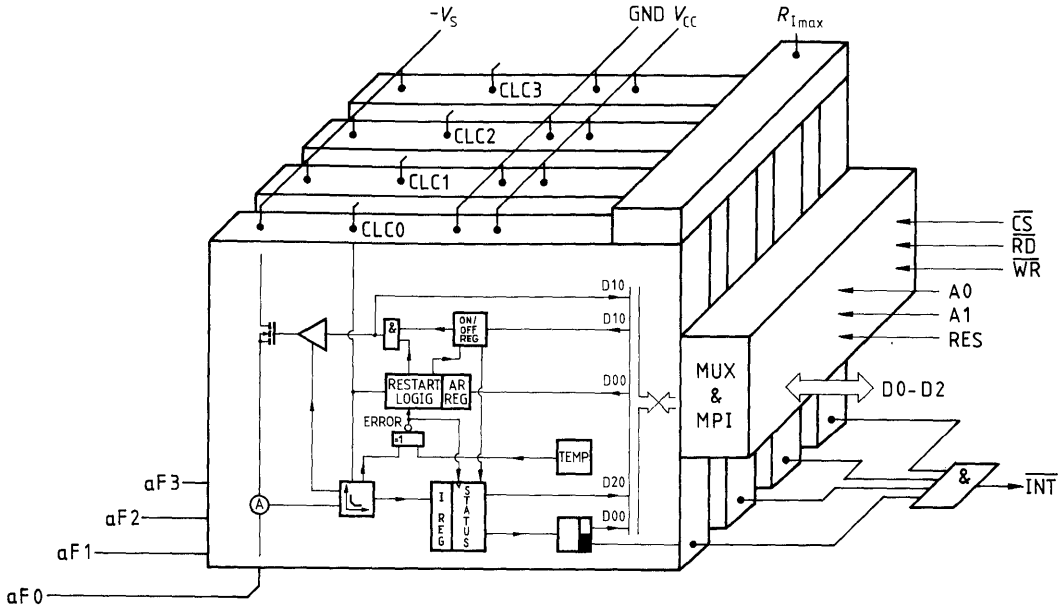
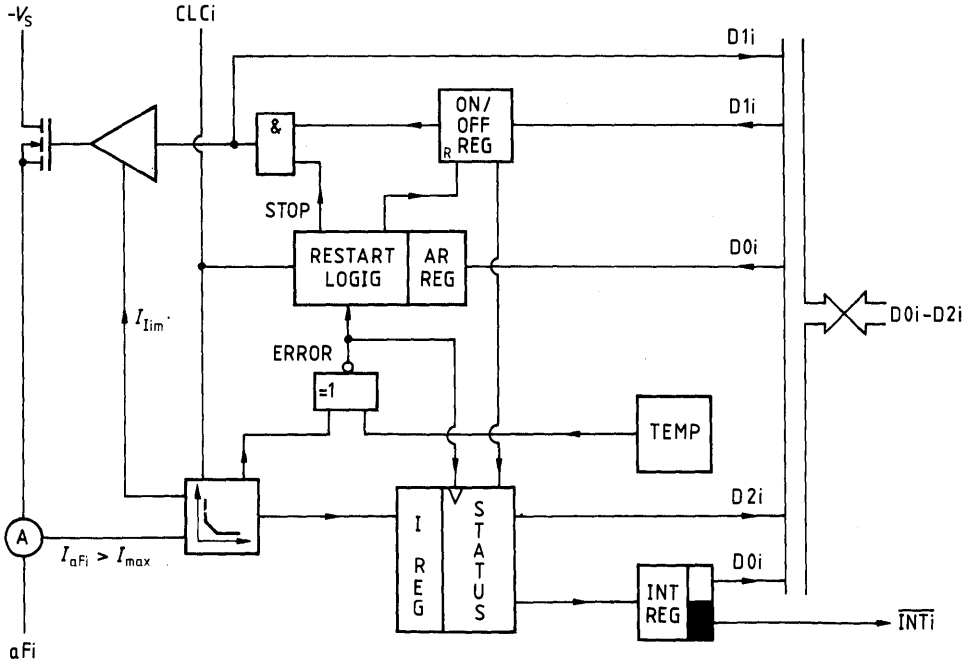


Figure 3
Functional Diagram of One Linedriver i



Functional Description

Figure 2 shows the IEPC organization. The exchange power controller contains one linedriver for each of the four transmission lines. A line oriented register architecture allows very simple software control. **Figure 3** shows the functional diagram of one of the four linedrivers. The IEPC consists of a high voltage analog part and a low voltage digital part. The ground battery (positive supply voltage) has to be connected to GND (Pin 11).

When powering up the IEPC, the linedrivers are switched off and all registers are cleared. The same initialized state can be achieved by an external high signal applied to the reset RES.

Analog Part

Power Switches

The negative pole of the supply, e.g. an exchange battery, has to be connected to the pin $-V_S$. After an ON-command to line i, a high voltage MOS-FET will connect the negative supply voltage from $-V_S$ to aF_i. The ON-resistance of each transistor is less than 10 Ω.

Current Control

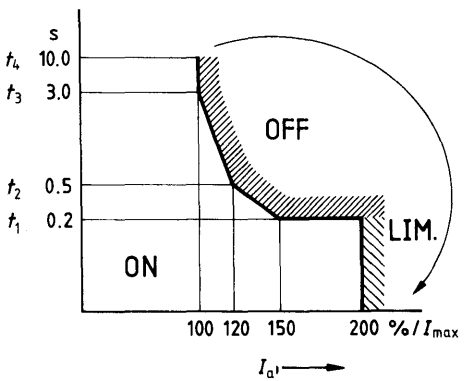
The current of each negative wire (aF_i) is controlled individually. The maximum feeding current is programmed by an external resistor R_I connected between pin $R_{I\ max}$ and GND **(figure 1)** and is the same to all four lines.

$$R_I\ [k\Omega] \approx 700/I_{max}\ [mA]$$

aF_i line control: Connecting an external capacitor between CLC and GND **(figure 1)**, the IEPC offers a special time and current dependent turn off characteristic. To meet the FTZ 1R211 recommendations, the value of the capacitor should be 10 µF. Additionally, the IEPC will limit the aF_i line current to 2.0 I_{max}, in order to protect the IEPC against over currents and to avoid discharging of the feeding source. **Figure 4** shows this transient permitted overload (TPO) state.

During the first 200 ms since overload of the negative wire aF_i was detected ($IaF_i \geq I_{max}$), the current will be limited to 2.0 I_{max}. Within the next 300, ms the current must drop from 1.5 I_{max} to 1.2 I_{max}, otherwise the linedriver turns off. After 3 s, any current above I_{max} results in turn off the linedriver. 10 s after overload is detected, if no turn off of the linedriver has accured, the current limiting characteristic becomes active again and will be prepared for detection of further overload conditions.

Figure 4
Diagram of the Transient Permitted Overload (TPO) State



The time dependence of the turn-off characteristic is based on the value of the external capacitor C_t at pin CLC:

$$t_1\,[\text{sec}] \approx C_t\,[\mu\text{F}]/50$$
$$t_2 \approx 2.5\,t_1;\; t_3 \approx 15\,t_1;\; t_4 \approx 50\,t_1.$$

If pin CLC is connected to GND, the time and current dependent turn off characteristic is disabled and the IEPC limits the driver current to 2 I_{max}.

Temperature Shut-Off

The temperature of each linedriver is monitored separately. If the temperature of one linedriver exceeds shut-off temperature, the transmission line will turn off. The shut-off temperature of the other three linedrivers will be increased.

Autorestart

In connection with the time-dependent-current-limitation, the IEPC offers an autorestart mode. If overload was detected and the linedriver has been switched off, an automatic restart can be programmed (see digital part). It should be noticed, however, that autorestart is only possible if the time- and current-dependent-turn off mode is used, i.e. a capacitor is connected between CLC_i and GND. The delay time depends on value of the capacitor.

Digital Part

The microprocessor interface (MPI) communicates with a processor which controls the IEPC. This MPI contains a 3-bit data bus, 2-bit address bus, read-, write-, chip select- and reset lines.

If chip select is inactive (logic high) the data bus is in a high impedance state and no communication between the processor and IEPC is possible. The IEPC contains a line oriented register architecture, i.e. one read and one write register for each line. A read or write cycle affects the addressed register, which is related to the corresponding linedriver.

The write register consists of three control bits per line i:

D0: Autorestart-bit (AR)
D1: ON/OFF-bit (ON)
D2: must be 0

The read register consists of three status bits per line i:

D0: Interrupt-bit (INT)
D1: Actual ON/OFF driver status-bit (AO)
D3: Current overload-bit

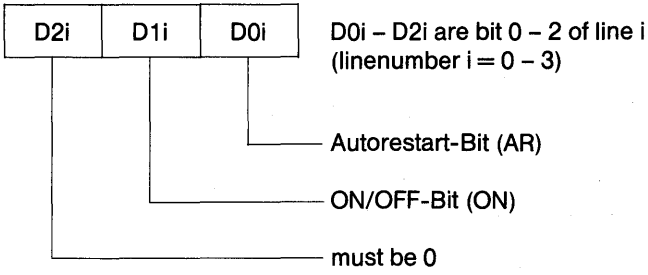
A logic high on the RES pin sets the device into an initial state: all registers of the IEPC are cleared (D0i – D2i are low).

Address Table

$\overline{CS}$	A1	A0	Selected Line
0	0	0	Line 0
0	0	1	Line 1
0	1	0	Line 2
0	1	1	Line 3
1	x	x	No Access

Write Register

The write register is organized as shown below:



Autorestart-Bit: If autorestart-mode is needed an external capacitor must be connected between pin CLCi and GND. If D0 is high, autorestart mode is enabled.

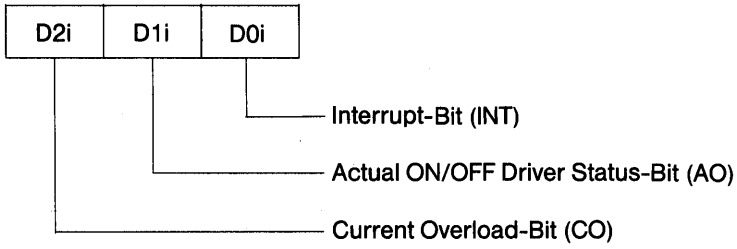
	D2i	D1i	D0i
AR Enabled	0	x	1
AR Disbaled	0	x	0

ON/OFF-Bit: To turn on a linedriver, D1i must be set to high, to turn off it must be set to low. An off command resets the time and current dependent turn off characteristic by discharging the external capacitor at pin CLCi.

	D2i	D1i	D0i
ON	0	1	x
OFF	0	0	x

Read Register

The read register is organized as shown below:



Interrupt-Bit: If malfunctions have been detected (current- or thermal overload) and the linedriver of line i has been turned off the interrupt-bit will be set:

	D2i	D1i	D0i
Interrupt	x	x	1
Operational	x	x	0

The interrupts $\overline{INT0}$ – $\overline{INT3}$ are ANDed to the device output-signal $\overline{INT}$. Thus if any malfunction is detected an interrupt signal is sento the the microprocessor.

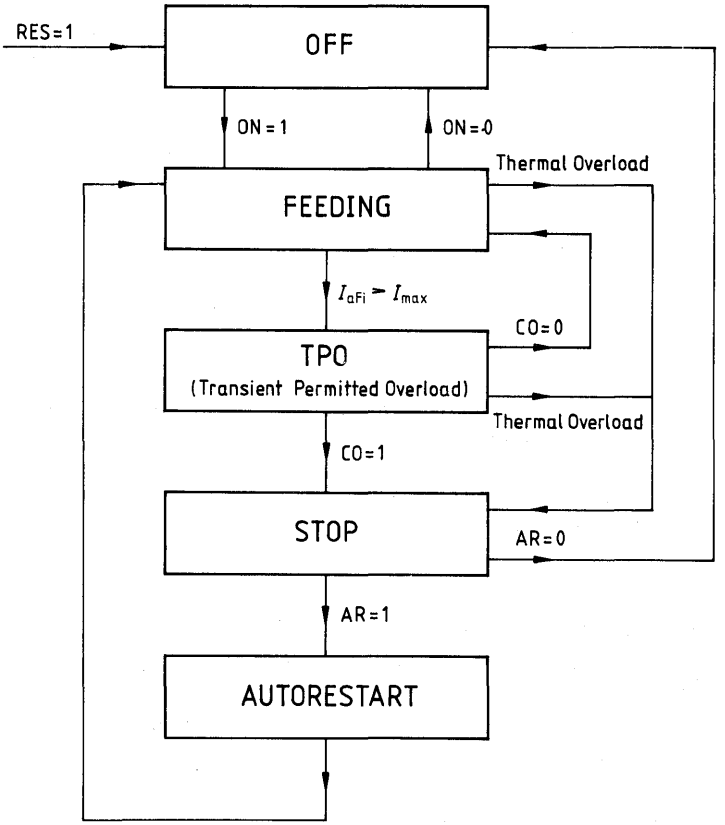
Actual ON/OFF Driver Status-Bit: D1i shows the actual status of the linedrive on line i:

Driver	D2i	D1i	D0i
DRIVER ON	x	1	x
Driver OFF	x	0	x

Current Overload-Bit: If $IaF_i \geq I_{max}$ is detected and the linedriver has been switched off the current overload bit will be set.

	D2i	D1i	D0i
Current overload	1	x	x
Operational	0	x	x

Figure 5
Linedriver State Diagram



State Diagram

Figure 5 shows the diagram of one IEPC linedriver.

A logic high on the RES input sets the device into the initial state. The linedriver is switched off and all registers are cleared. The same initialized state is achieved by powering up the IEPC. After an ON-command (ON = 1), the linedrivers will turn on and the IEPC is the FEEDING-state. To return to the OFF-state the ON-bit must be cleared (ON = 0).

In the FEEDING-state, the current IaF_i is controlled. If overcurrent is detected, one of the following cases happens:

1. If an external capacitor is connected between CLC_i and GND and $IaF_i \geq I_{max}$ is detected, the IEPC stays in the **Transient P**ermitted **O**verload-state (TPO). Exceeding the time-current-limit, the linedriver turns off and the IEPC is in the STOP-state. The current overload-bit will be set (CO = 1). If no exceeding happens, the linedriver returns to the FEEDING-state.

2. If $IaF_i \geq I_{max}$ is detected and CLC_i is connected to GND, the IEPC limits the driver current to 2 I_{max}. The current overload bit will not be set.

The temperature of each linedriver is controlled separately. If the temperature of one linedriver exceeds the shut-off temperature, the transmission line will turn off and the linedriver is in the STOP-state. In this case, the shut-off temperature of the other three linedrivers will be increased.

There are two different ways to leave the STOP-state:

1. If the autorestart bit is set (AR = 1), the IEPC returns after a delay time to the FEEDING-state automatically. The ON/OFF register will not be cleared.
2. If no autorestart mode is selected (AR = 0), the IEPC returns to the OFF-state. In this case, the ON/OFF register will be cleared.

As soon as the STOP-state is reached the IEPC sends an interrupt signal to the microprocessor (interrupt-pin is active low).

If the linedriver i is not in the thermal overload state, every rising edge of the read signal resets the interrupt bit INT_i (DOi) of the selected line i. The current overload-bit COi (D2i) is reset too.

If the linedriver i is in the thermal overload state, the rising edge of the read signal has no effect on the interrupt bit.

The internal interrupts $\overline{INT0}$ - $\overline{INT3}$ are ANDed to the open drain output pin $\overline{INT}$. So the interrupt pin stays active low until all interrupt bits INT_i are reseted.

Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Supply voltage referred to GND	$-V_S$	−70	V
V_{CC} referred to GND	V_{CC}	6	V
On any other pins referred to GND	V_S	−0.5 to 6	V
Reverse current on pins aF0 – aF3	I_S	0	mA
Power dissipation	P_D	1	W
Ambient temperature under bias	T_A	−25 to 85	°C
Storage temperature	T_{stg}	−40 to 125	°C
Thermal resistance junction to ambient	T_j	50	K/W

Operating Range

$T_A = 0$ to 70 °C, $V_S = -60$ V, $V_{CC} = 5$ V ± 5%, GND = 0 V

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Linedrivers				
Operating voltage ($-V_S$ – GND)	$-V_S$	−12	−60	V
Feeding current (aF_i)	I_F		100	mA
Current limiting (aF_i)	I_{LIM}		200	mA
Turn-on resistance ($-V_S$ – aF_i)	R_{DSON}		10	Ω
Delay: ON-Command to turn on linedriver[1])	t_{ON}		0.5	ms
Delay: OFF-Command to turn off linedriver	t_{OFF}		2	ms

[1]) for res. loads

Operating Range (cont'd)
$T_A = 0$ to 70 °C, $V_S = -60$ V, $V_{CC} = 5$ V ± 5%, GND = 0 V

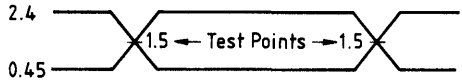
Parameter	Symbol	Limit Values min.	Limit Values max.	Unit
Control & Logic				
Autorestart period $I_O = 2$ mA	t_{ar}	10		s
MPI				
L-input voltage	V_{IL}	−0.5	0.8	V
H-input voltage	V_{IH}	2.0	V_{CC}	V
L-output voltage $I_O = 2$ mA	V_{OL}		0.45	V
H-output voltage $I_O = 1$ mA	V_{OH}	2.4		V
Reset pulse width	t_{RES}	5		µs

Switching Times

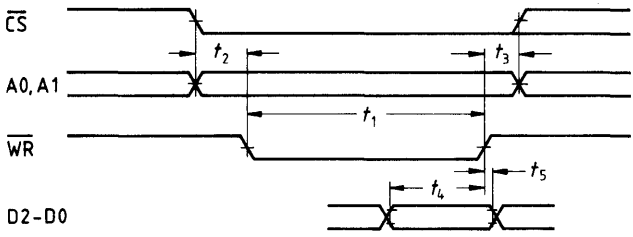
Parameter	Symbol	Limit Values min.	Limit Values max.	Unit
$\overline{RD}$ or $\overline{WR}$ pulse width	t_1			ns
Address and $\overline{CS}$ setup time to $\overline{RD}\downarrow$ or $\overline{WR}\downarrow$	t_2			ns
Address and $\overline{CS}$ hold timer after $\overline{RD}\uparrow$ or $\overline{WR}\uparrow$	t_3			ns
Data setup time to $\overline{WR}\uparrow$	t_4			ns
Data hold time after $\overline{WR}\uparrow$	t_5			ns
Data valid after $\overline{RD}\downarrow$	t_6			ns
Data valid after $\overline{RD}\uparrow$	t_7			ns
Data bus inactive after $\overline{RD}\uparrow$	t_8			ns

Waveforms

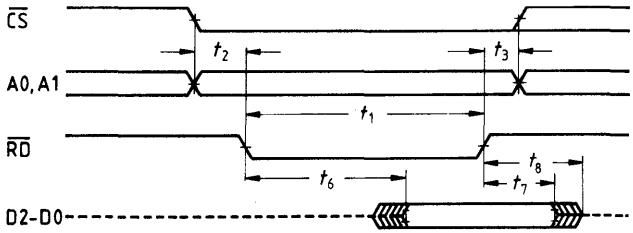
AC Testing Input, Output Waveform



Write Timing



Read Timing



SIEMENS

Extended PCM Interface Controller (EPIC-1) PEB 2055

Preliminary Data **CMOS IC**

Type	Ordering Code	Package
PEB 2055-C	Q67100-H6034	C-DIP-40
PEB 2055-N	Q67100-H6035	PL-CC-44 (SMD)
PEB 2055-P	Q67100-H6036	P-DIP-40

Information from subscriber lines needs to be transferred to time slots on system internal PCM communication highways. The EPIC™ concentrates the circuitry necessary to do this interfacing for a large number of transmission lines on a single IC. Therefore, it is not necessary to repeat this PCM interface circuitry for every line. Since the system cost of the EPIC is divided by the number of lines it controls, powerful and comfortable functions can be economically performed.

The basic functions of the EPIC were defined by the system houses of ALCATEL, Siemens Plessey and ITALTEL as part of their ISDN cooperation.

Features

- PCM interface controller for up to 32 ISDN or 64 analog subscribers
- Time-slot assignment freely programmable for all subscribers
- Non-blocking switch for 128 channels
- Switching of 16-, 32-, 64-kbit/s channels (128-kbit/s via two consecutive 64-kbit/s channels)
- Two serial interfaces: PCM and configurable (IOM®-1, IOM®-2, SLD, PCM)
- Interfacing with four full-duplex PCM highways (2, 4 or 8 Mbit/s)
- Data rates of PCM and configurable interfaces independent of each other
- Change detection ("last-look") logic for C/I or feature control channels
- 16-byte FIFO for monitor or signaling channels
- Standard µP interface with multiplexed (P-DIP-40) or demultiplexed (PL-CC-40) address/data bus
- Advanced low power CMOS technology

General

Up Stream Direction from the subscriber to the PCM highways in the exchange.

Down Stream Direction from the PCM highways to the subscribers.

Time Slot Defined period of time the PCM, IOM or SLD frame consisting of 8 bits. Time slots are allocated to the frames in such away that the time slot boundaries coincide with the frame boundaries. The time slots do not overlap. The lowest time-slot number is 0. This time slot is the first in the frame.

Sub Time Slot A quarter or half a time slot. These are allocated to the time slots in such a way that time slot and subtime slot boundaries match. The subtime slots are non overlapping.

Channel Sequence of bits which is exchanged between the subsriber, the exchange equipment and/or the microprocessor. It occupies a definied number of bits at a definied position within a frame as long as a connection pervails. Both time slots and subtime slots are channels and hence a channel may offer a bandwidth of 16, 32 or 64 kbit/s.

Bit Numbering The bits in a slot are numbered 7 (MSB) through 0 (LSB). Bit 7 is the first bit to be transmitted or received, bit 0 the last.

General Device Overview

The Extended PCM Interface Controller EPIC (PEB 2055) is a monolithic switching device for the path control of up to 128 channels of 16, 32 or 64 kbit/s bandwidth. Two consecutive 64 kbit/s channels may also be handled as a quasi single 128 kbit/s channel. For these channels the EPIC performs nonblocking space time switching between two serial interfaces, the system and the configurable interface.

Both interfaces can be programmed to operate data rates between 8 and 8192 kbit/s. The system interface consists of up to four duplex ports with a tristate indication signal for each output line. The configurable interface can be selected to incorporate either four duplex or eight bidirectional I/O ports (SLD).

The EPIC can therefore be programmed to communicate either with SLD or with IOM (ISDN Oriented Modular) compatible devices. In both cases the device handles the layer-1 functions buffering the C/I and monitor channels for IOM compatible devices and the feature control and signaling channels for SLD compatible devices.

Due to its capability to switch channels of different bandwidths, the EPIC can handle up to 32 ISDN subscribers with their 2B+D channel structure in IOM configuration or up to 16 subscribers in SLD configuration. Since its interfaces can operate at different data rates, the EPIC is an ideal device for data rate adaption.

Moreover, the EPIC is one of the fundamental building blocks for networking with either central, decentral or mixed signaling and packet data handling architectures. The other key devices are the IDEC™ (ISDN D-channel Exchange Controller, PEB 2075) and the HSCX (High-Level Serial Communication Controller Enhanced, SAB 82525).

Applications of the EPIC include communication multiplexers, concentrators, central switches as well as peripheral ISDN and analog line cards.

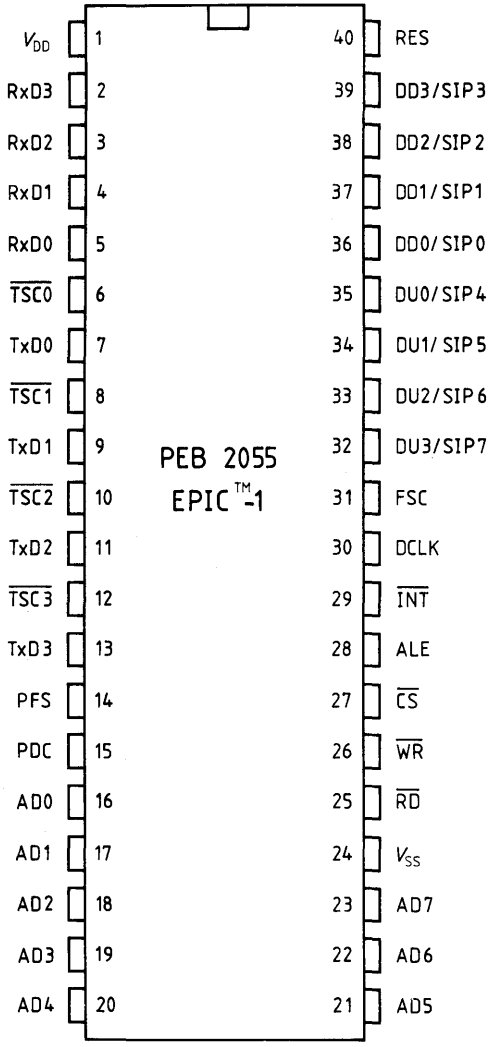
The EPIC is available in a P-DIP-/C-DIP 40 or a PL-CC-44 package.

The P-DIP/C-DIP-40 version is controlled by a standard 8-bit-parallel microprocessor interface with a multiplexed address-data bus. In the PL-CC-44 package the device may optionally be controlled by separate address and data buses.

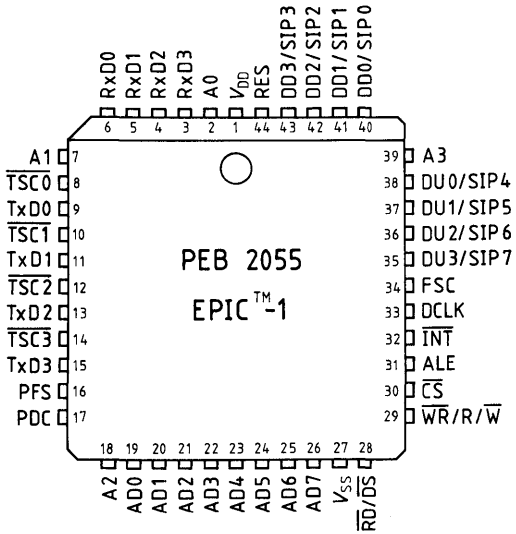
The PEB 2056 EPIC-2 is a smaller version of the EPIC-1. The EPIC-2 has been optimized for digital line cards with up to eight subscriber lines. In contrast to the EPIC-1, the EPIC-2 has only one IOM interface, only two PCM highway connections and comes in P-DIP-28 or PL-CC-44 packages.

Pin Configuration
(top view)

P-DIP-40



PL-CC-44



Pin Defintions and Functions

Pin No. P-DIP	Pin No. PL-CC	Symbol	Input (I) Output (O) In/Output (IO) Open Drain (OD)	Function
1	1	V_{DD}		Supply Voltage 5 V ± 5%
	2	A0	I	**Address Bus Bit 0:** This input interfaces to the system's address bus to select an internal register for a read or write access. This pin is only provides in the PL-CC package and only active if a demultiplexed µP interface mode is selected.
2 3 4 5	3 4 5 6	RxD3 RxD2 RxD1 RxD0	I	**Receive PCm Interface Data:** Serial data is received at these lines at standard TTL or CMOS levels.
	5	A1	I	**Address Bus Bit 1:** This input interfaces to the system's address but to select an internal register for a read or write access. This pin is only provides in the PL-CC package and only active if a demultiplexed µP interface mode is selected.
6 8 10 12	8 10 12 14	$\overline{TSC0}$ $\overline{TSC1}$ $\overline{TSC2}$ $\overline{TSC3}$	O	Tristate control for the PCM interface. These lines are low when the corresponding TxD outputs are valid.
7 9 11 13	9 11 13 15	TxD0 TxD1 TxD2 TxD3	O	**Transmit PCM Interface Data:** Serial data is sent by these lines at standard TTL or CMOS levels. These pins can be tristated.
14	16	PFS	I	PCM interface frame synchronization pulse.
15	17	PDC	I	PCM interface data clock, signle or double rate.

Pin Definitions and Functions (cont'd)

Pin No. P-DIP	Pin No. PL-CC	Symbol	Input (I) Output (O) In/Output (IO) Open Drain (OD)	Function
–	18	A2	I	**Address Bus Bit 2:** This input interfaces to the system's address bus to select an internal register for a read or write access. This pin is only provides in the PL-CC package and only active if a demultiplexed µP interface mode is selected.
16 17 18 19 20 21 22 23	19 20 21 22 23 24 25 26	AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7	I/O	**Address Data Bus.** If the multiplexed address/data µP interface bus mode is selected these pins transfer data and commands between the µP and the EPIC. If a demultiplexed mode is used, these bits interface with the system data bus.
24	27	V_{SS}	I	**Ground:** 0 V
25	28	$\overline{RD}$	I	**Read:** The signal indicates a read operation, active low.
26	29	$\overline{WR}$	I	**Write:** This signal indicates a write operation, active low.
27	30	$\overline{CS}$	I	**Chip Select.** A low on this line selects the EPIC for a read/write operation.
28	31	ALE	I	**Address Latch Enable.** In the Intel type multiplexed µP interface mode a logical high on this line indicates an address of an EPIC internal register on the external address/data bus. In the Intel type multiplexed µP interface mode this line is fixed to logical 0, in the demultiplexed Motorola type µP interface mode it should connected to 5 V.
29	32	$\overline{INT}$	OD	Interrupt line, active low
30	33	DCLK	IO	Data Clock input or output in IOM/slave clock in SLD configuration.

Pin Definitions and Functions (cont'd)

Pin No. P-DIP	Pin No. PL-CC	Symbol Output (O)	Input (I) In/Output (IO) Open Drain (OD)	Function
31	34	FSC	IO	Frame Synchronization input or output in IOM configuration / Direction indication signal in SLD configuration.
32 33 34	35 36 37	DU3/SIP7 DU2/SIP6 DU1/SIP5	O/IO	Data Upstream outputs in IOM configuration. Serial interface port 4, 5, 6 and 7 in bidirection configuration.
–	39	A3	I	**Address Bus Bit 3:** This input interfaces to the system's address bus to select an internal register for a read or write access. This pin is only provides in the PL-CC package and only active if a demultiplexed µP interface mode is selected.
36 37 38 39	40 41 42 43	DD0/SIP0 DD1/SIP1 DD2/SIP2 DD3/SIP3	I/IO	Data Downstream inputs in IOM configuration. Serial interface ports 0, 1, 2 and 3 in bidirectional configuration.
40	44	RES	I	**Reset.** A logical high on this input forces the EPIC into the reset state.

Logic Symbol

Figure 1
Functional Symbol for the Duplex Configuration

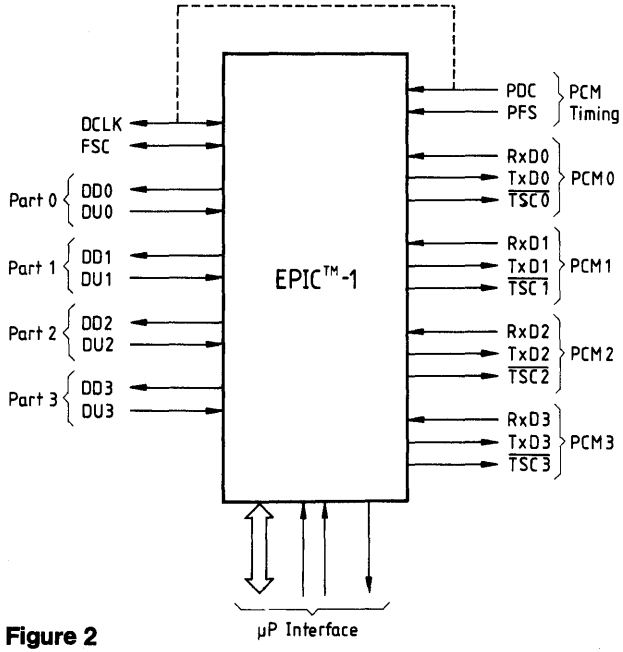
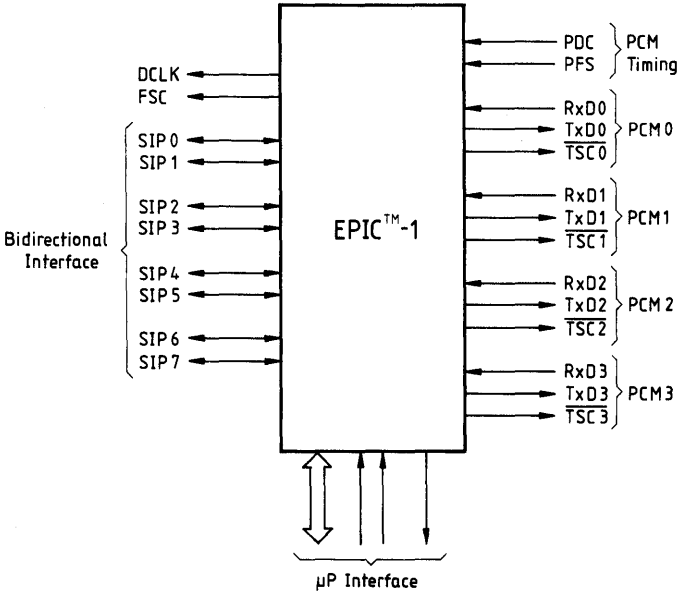


Figure 2
Functional Symbol for the Bidirectional Configuration



System Integration

Communication Multiplexers

The nonblocking switching capability for various bandwidth implemented in the EPIC makes the circuit suitable for use in communication multiplexers. Due to the data rate programmability of the configurable and PCM interfaces, data rate adaption (e.g. between 1544 and 2048 kbit/s systems can be accomplished.

Concentrators

Due to the high data rates of up to 8192 kbit/s, the EPIC can be used in concentrator applications.

Central Switches

The EPIC is a nonblocking switch for up to 128 channels per direction. The channel bandwidth can be programmed to 16, 32 or 64 kbit/s. The PCM and configurable interfaces are programmable for a wide variety of data rates from 8 to 8192 kbit/s. PCM and configurable interfaces can be operated with different clock frequences. Thus, the EPIC can be used in central switches and for data rate adaption.

Line Cards

The EPIC is designed to operate in 3 digital or analog line card architectures. For a schematic summary of these possible line card configuration refer to **figure 3.**

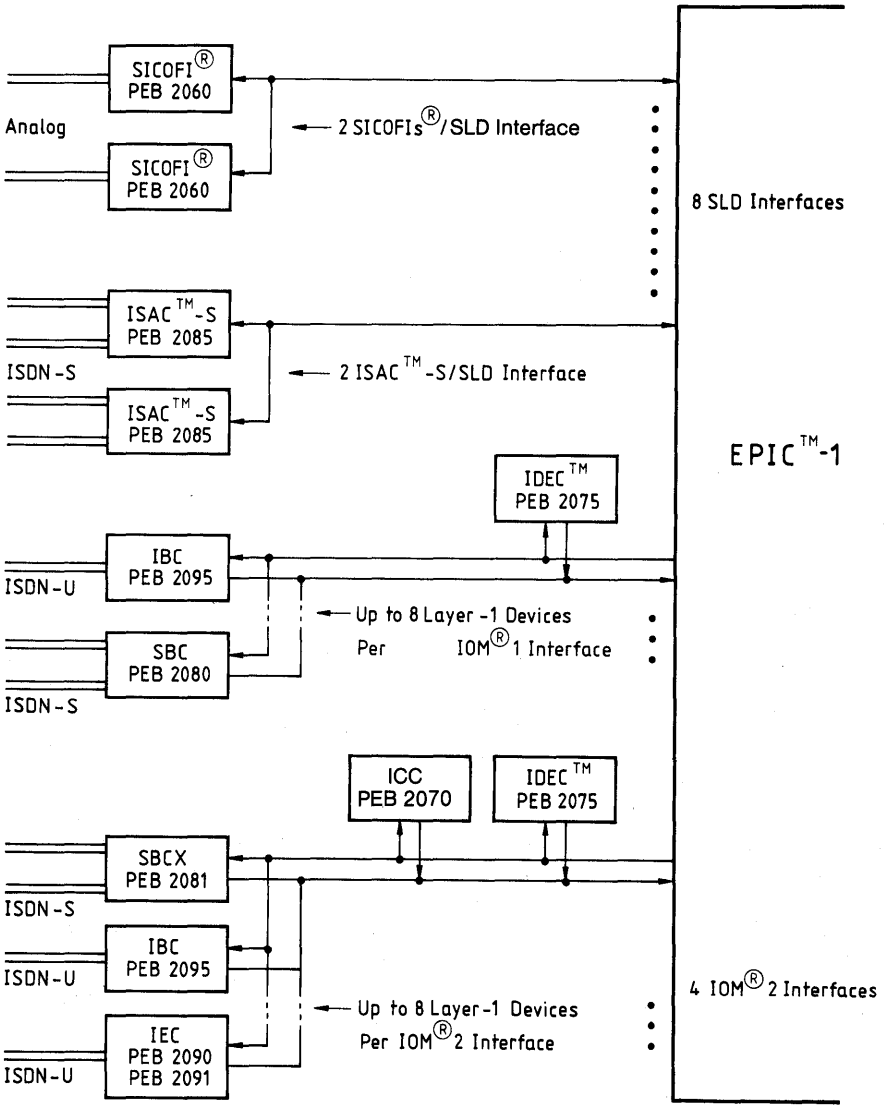
With its **configurable interface** being programmed as a **SLD interface**, it can communicate with SLD compatible devices (e.g. Siemens Codec Filter, SICOFI®, PEB 2060 or ISDN Subscriber Access Controller ISAC™-S, PEB 2085). Connected to up to 16 SICOFIs, the EPIC can serve up to 16 analog lines. Used together with ISAC-S, the EPIC provides the signals for up to 16 ISAC-S, to support up to 16 S-interfaces.

Alternately, the configurable interface may be selected as **IOM interface**, which is compatible to both the **multiplexed IOM-1** and the **IOM-2 interface**.

In the **multiplexed IOM-1 interface** is chosen, the EPIC supports up to 32 ISDN subscribers on the digital line card. The interface lines are then connected to the EPIC, an IOM-1 compatible layer-1 device e.g. the S-bus controller (SBC, PEB 2080), the ISDN Burst Transceiver Circuit (IBC, PEB 2095) or the ISDN Echo Cancellation Circuit (IEC, PEB 2090) and, optionally, an IOM-1 compatible layer-2 device e.g. the ISDN D Channel Exchange Controller (IDEC, PEB 2075).

In the case of an **IOM-2 interface**, the EPIC supports up to 32 ISDN or 64 voice subscribers. They are connected via the SBCX (PEB 2081), IBC (PEB 2095) or IEC (PEB 20901 and PEB 20902) and a digital loop. In both cases, either the ICC (PEB 2070) or the IDEC (PEB 2075) may perform the D channel handling.

Figure 3
Schematic Summary of the Line Card



Analog Line Card

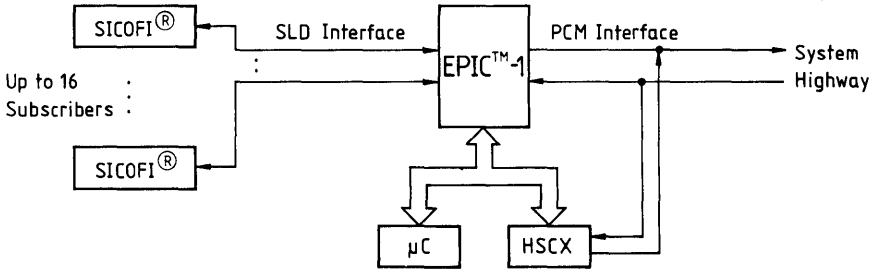
In analog line cards, the EPIC controls the signaling, voice and data paths of 64 kbit/s channels.

In combination with SLD compatible devices e.g. the highly flexible Siemens codec filter (PEB 2060), it forms an optimized analog subscriber line board architecture as shown in **figure 4.** The HSCX (High Level Serial Communication Controller, SAB 82525) handles the signaling information contained in a time slot of programmable bandwidth at the PCM interface or on a dedicated signaling highway.

Moreover, the EPIC controls the feature control and signaling channels and buffers these channels to the µC.

Figure 4

Example of an Analog Line Card Architecture



Digital Line Cards

On digital line cards, the EPIC performs the switching function for up to 32 ISDN subscribers between the PCM system highways and the IOM interfaces. Moreover, it has the layer-1 controlling capability of buffering the C/I and monitor channels of the IOM interface.

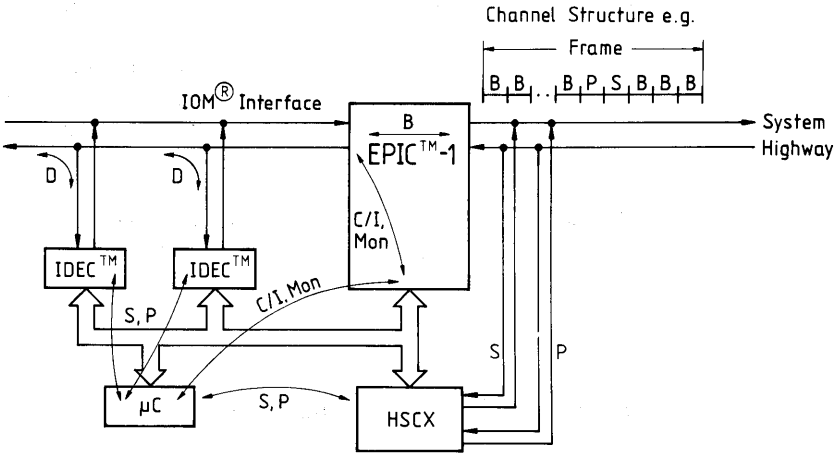
The EPIC can be operated in tandem, i.e. one device is active, another one is a backup device. The backup device can instantaneously take over from the active device when the active device fails. Due to this tandem operation capability and the high number of ISDN subscribers which can be connected to one EPIC, the use of single line cards is feasable.

Several architectures are possible.

In **completely decentral** D channel processing architectures **(figure 5)**, the processing capacity of a line card is usually dimensioned to avoid blocking situations even under maximum conceivable D channel traffic conditions. In such an architecture, the EPIC switches the B channels and performs C/I and monitor channel control. The IDECs handle the layer-2 functions for signaling and data packets in the D channel and transfer the extracted data via the µP and an HDLC controller, e.g. the HSCX (High Level Serial Communication Controller Enhanced SAB 82525) to the system. One of the channels of the HSCX may be used for example for the signaling information, the other for data packets. The HSCX may access either a time slot of programmable bandwidth on one of the system highways **(figure 5)** or a separate signaling highway **(figure 6)**. In both cases, the highway capacity used for packet traffic can be shared among several line cards due to the statistical multiplexing capabilities of the HSCX.

Figure 5

Completely Decentral Packet Switching Digital Line Card Architecture

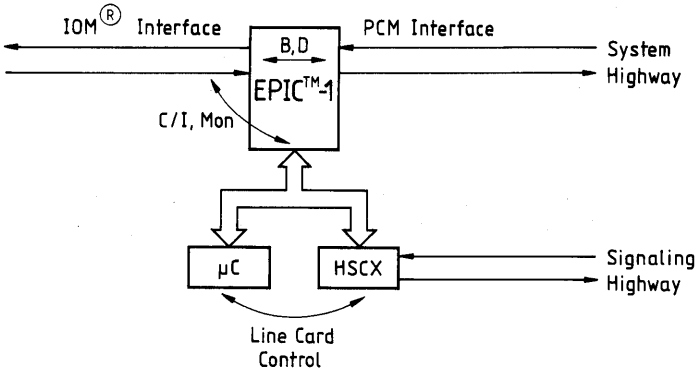


In an architecture with **completely central** D channel handling **(figure 6)**, the EPIC switches the B and D channels and performs the C/I and monitor channel control functions.

The line card microcontroller programs the EPIC and is connected to the group control via a signaling highway and an HSCX. Moreover the EPIC controls the layer-1 protocol on the IOM interface, buffering the C/I and monitor channels to the microprocessor.

Figure 6

Digital Line Card Architecture with a Completely Central D Channel Handling



A third possibility is a **mixed architecture** with central packet data and decentral signal handling. This is a very flexible architecture which reduces the dynamic load of central processing units by evaluating the signaling information on the line card. For this case, any increase of packet data traffic does not necessitate any changes in the architecture since the line cards do not have to be modified. The central packet handling unit can simply be expanded.

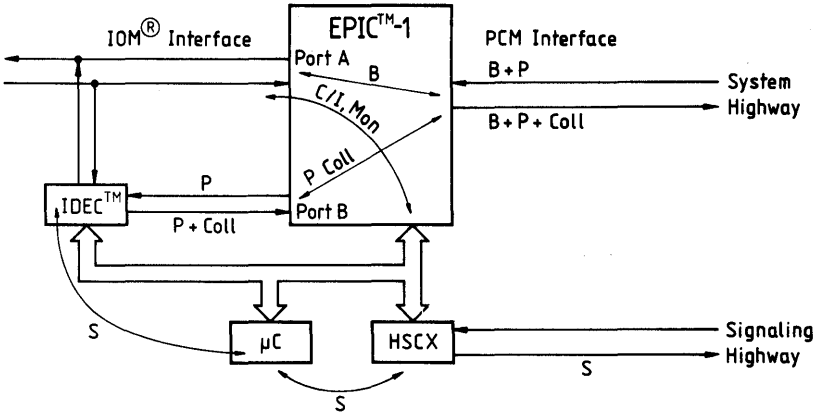
For such an architecture, the EPIC performs B and D channel switching in addition to C/I and monitor channel control. The IDECs handle the signaling data of the D channel. These messages are transferred to the group controller via the microprocessor and an HDLC controller. The packet data of the D channel are switched to the system highways and processed by the central packet unit.

In this architecture, the EPIC switches the B channels from IOM port A **(figure 7)** to the PCM interface. The IDEC works in a master/slave configuration. Therefore, an additional collision resolution line is needed. The IDEC separates signaling from data packets. The signaling messages are transferred to the µC, which in turn hands them over to the group controller using the HSCX.

The packet data are processed differently. Together with the collision resolution line they are handled by the IDEC at another IOM port (port B). The EPIC switches the channels of these ports to the PCM interface as shown in **figure 7.**

Figure 7

Line Card Architecture for Mixed Packet Handling, 2 IOM Ports of the EPIC

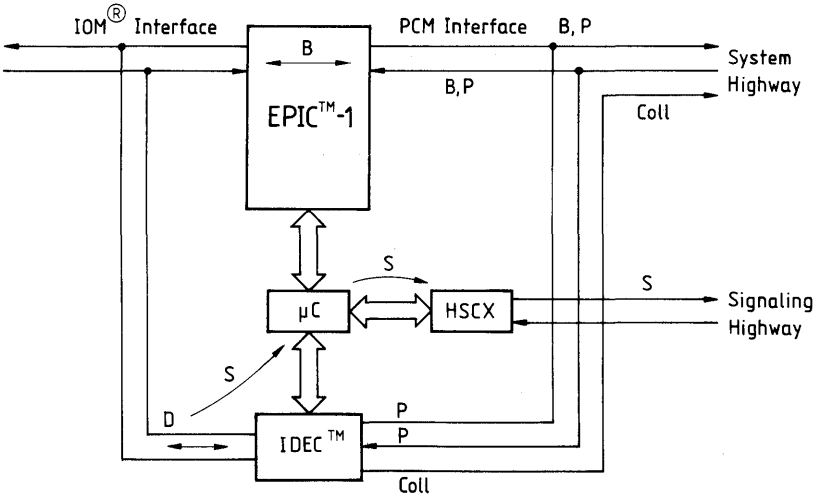


In such a configuration, the p packets and the collision resolution signal occupy one of the IOM ports available at the configurable interface. This reduces the total switching capability of the EPIC to 24 ISDN subscribers.

Alternately, the packet data and the collision line can be directly exchanged between the IDEC and the PCM highway. The EPIC then simply switches the B channels **(see figure 8)**. The packet data are separated by the IDEC and placed on the PCM highway. Thus, the full 32 subscriber switching capability of the EPIC is retained.

Figure 8

Digital Line Card Architecture for Mixed Packet Handling Using a Collision Highway



Packet Handlers

The EPIC is an important building block for networks based on either central, decentral or mixed signaling and packet data handling architectures. Its flexibility allows for the modification of the packet handling architecture according to the changing needs.

Thus, it may be useful to add central packet handling groups to a network originally based on decentral signaling packet handling. This may be the case if growing data packet traffic exceeds the initial capacity of the network. The result is a mixed architecture.

On the other hand, increasing packet handling demand on a few dedicated subscriber lines calls for solutions which back up the capacity at these few decentral line cards.

In both of these cases and several other applications, the EPIC is a powerful device for solving the problem of packet handling. In most applications,it is used together with the IDEC (ISDN D Channel Exchange Controller).

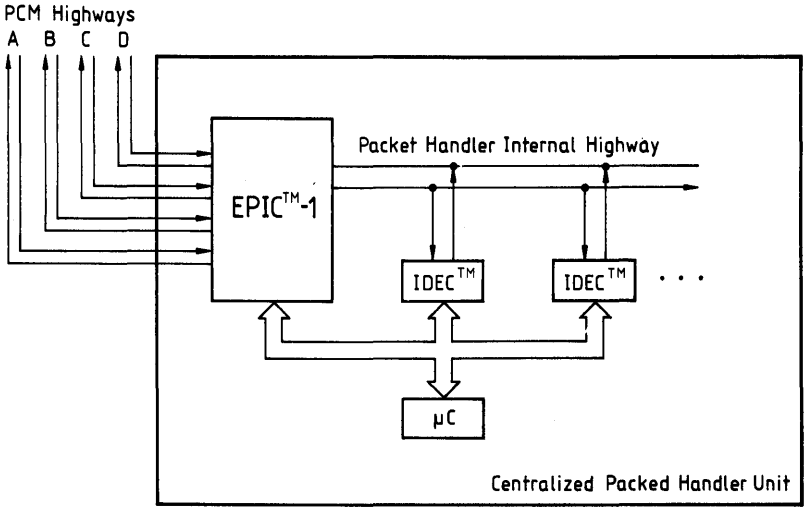
Decentralized and mixed packet handling has already been covered in the line card chapter. In the following, the centralized signaling/data packet handlers built up with the EPIC will be described.

Central packet handling is used if many subscribers with a generally low demand for packet switching are to be connected to a system. Concentrating the packet servers for multiple users eliminates the need to provide a packet server channel for every user. The overall number of packet server channels can thus be reduced.

In such a central packet handling group, the EPIC performs the switching and concentrator function. It connects a variable number of PCM highways to the packet handler internal highway. HDLC controllers are also connected to this internal highway as illustrated in **figure 9.**

Figure 9

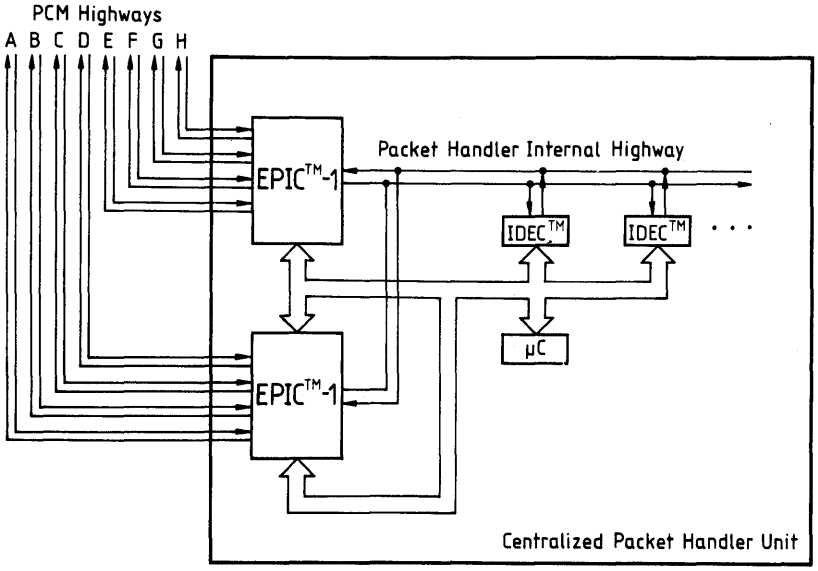
Centralized Packet Handler with a Single Internal Highway Connected to 4 PCM Highways



This figure shows one EPIC connecting four PCM highways to one packet handler internal highway. These highways are accessed by the IDECs (ISDN D channel Exchange Controller) which are 4 channel HDLC controllers and handle the packets. If more than four PCM highways shall be connected to the centralized packet handler, further EPICs are necessary. Such a situation is shown in **figure 10**, where 8 highways are switched to one packet handler internal highway. In this case the two EPICs are connected in parallel at the packet handler internal side.

Figure 10

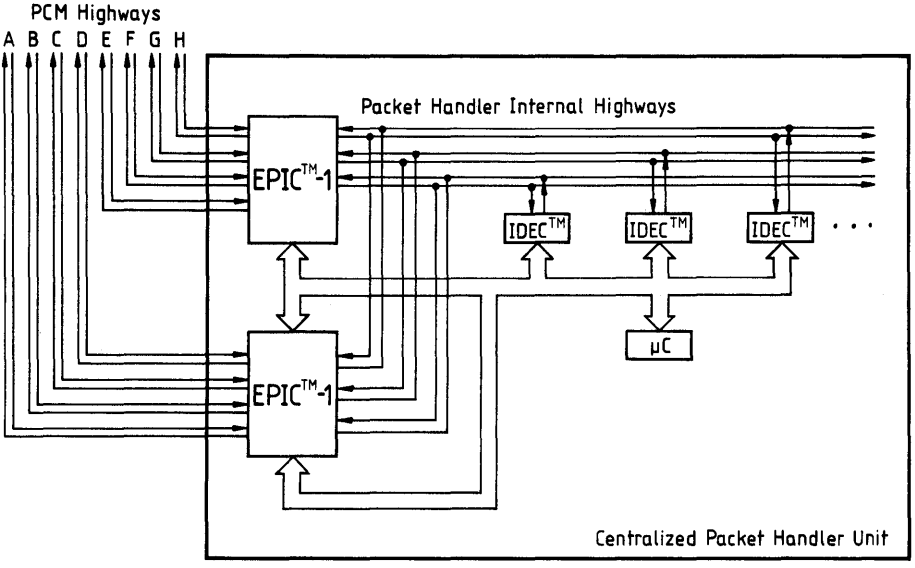
Centralized Packet Handler with 1 Internal Highway Connected to 8 PCM Highways



The data rate of the packet handler internal highway can be up to 4096 kbit/s. If this capacity is not sufficient, other packet handler internal highways may be added as shown in **figure 11.**

Figure 11

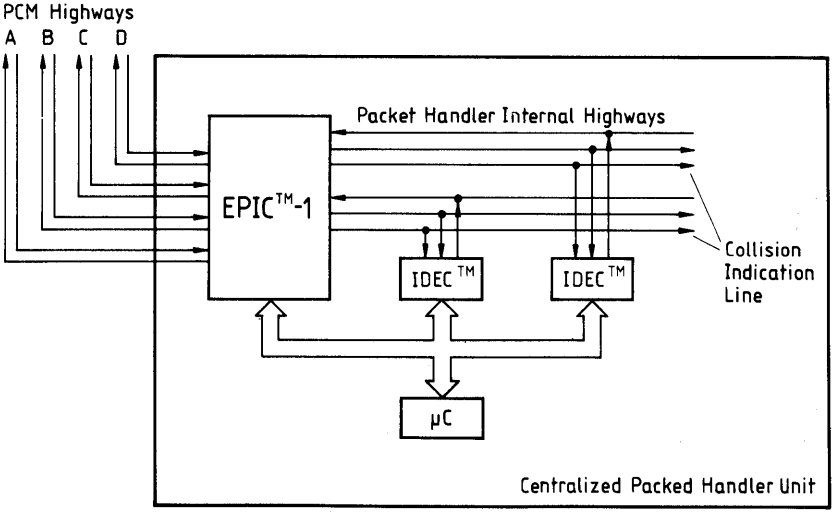
Centralized Packet Handler with 3 Internal Highways



In some applications an additional collision resolution signal is required for the HDLC controllers. This information can be demultiplexed from the PCM highways to a third line for each packet handler internal highway **(see figure 12).**

Figure 12

Centralized Packet Handler with Internal Collision Line



The applications illustrated apply equally to centralized signaling as well as to data packet handlers.

Functional Description

The EPIC is a peripheral board controller. It combines the nonblocking switching function between the PCM and the configurable interfaces for 128 channels per direction with the layer-1 control function for connection set-up/termination/maintenance on one chip.

A general block diagramm of the EPIC is shown in **figure 13.**

In the downstream direction, the input information of a complete frame is stored in the data memory. The incoming channels are written in sequence into fixed positions in the data memory. This is controlled by the downstream input counter with an 8-kHz-repetition rate. A cyclic write sequence results.

For the downstream switching, the control memory (CM) is read in sequence. The addressed location contains a pointer to a location in the data memory. The byte in this data memory location is read into the current configurable interface time slot, resulting in a random read sequence.

The read access of the control memory is controlled by the downstream output counter, correlating the data memory read operations with the downstream output time-slot sequence.

In the upstream direction, the data is written to the data memory randomly, under CM control and read from there cyclically.

Hence, for the desired connection the control memory needs to be programmed beforehand using the MAAR, MADR and MACR registers **(see chapter Memory Access Register)**. The control memory address corresponds to one particular configurable interface time slot and line number. The contents of this control memory address point to a particular PCM interface time slot and line number now resident in the data memory.

For upstream output, four control bits per time-slot are provided in the data memory. These control the output driver state of any possible subtime slot.

Besides the data memory address, each CM address also points to four code bits determining the bandwidth of the switched channel. These code bits are also used to mark the signaling channels at the CFI.

The EPIC can be used in two different set-ups:

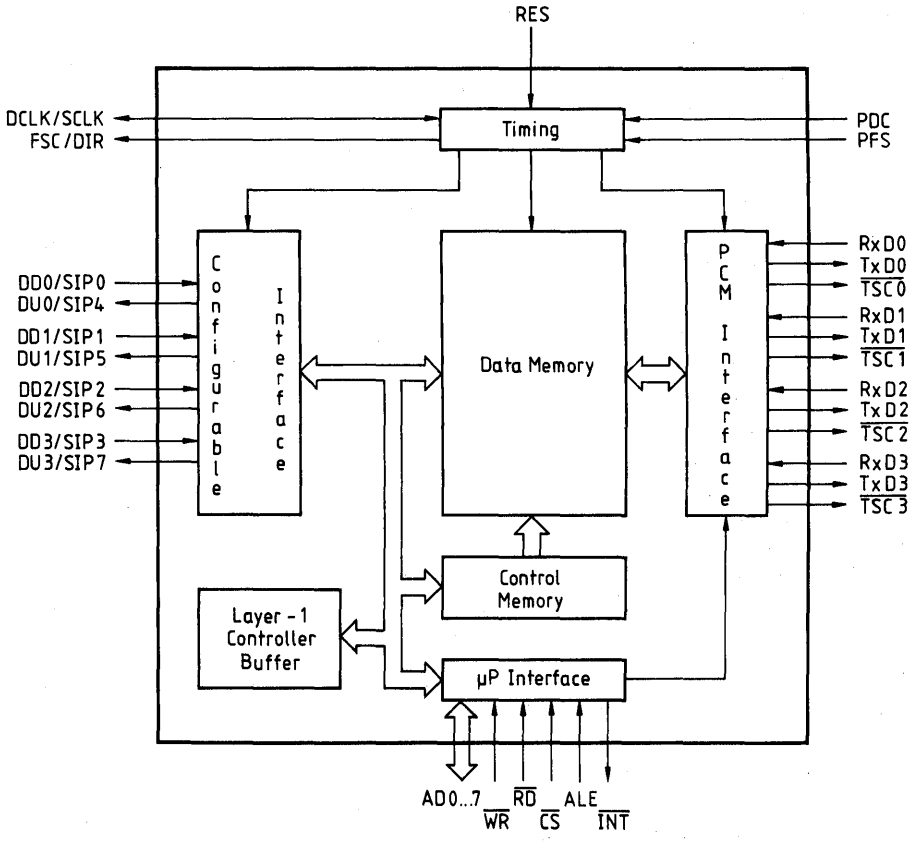
- In the bidirectional set-up, every channel at the configurable interface can be programmed to be either input or output. 8 equivalent bidirectional ports at the configurable interface result.
- In the duplex set-up, 4 of the 8 lines of the configurable interface are predetermined as outputs, 4 as inputs. 4 duplex ports result.

In both of these set-ups, the EPIC provides a switching capability for up to 128 channels and direction.

The IOM and the SLD configurations previously mentioned are special cases of these set-ups:

- In the IOM, the EPIC switches the B and D channels of up to 32 subscribers working in the duplex set-up. Additionally, the device handles the monitor and C/I channel buffering to the µP.
- In the SLD configuration, the EPIC switches up to sixty four 64 kbit/s channels operating in bidirectional set-up. Additionally, the device handles the feature control and signaling channels buffering to the µP.

Figure 13
Functional Block Diagram of the EPIC



In the IOM configuration, upon proper programming, the EPIC checks the incoming C/I channels and generates interrupts if changes occur. In the case of the bidirectional configuration, it implements the double last look algorithm with a period adaptable to a wide range of system needs.

For handling the monitor or feature control channel, the EPIC is equipped with a FIFO buffering up to 16 bytes of information. The contents can be transferred or received upon a special command. Or, they can be dealt with largely autonomously according to the IOM handshake procedure.

Operational Description

Principles

Every time slot at the configurable interface is controlled by a control memory entry. Thus, the functionality of every time slot may be chosen from the choices of **table 1**.

Table 1

CFI Time Slot Functionality Choices

Functionality			Application
Transparent	64 kbit/s 32 kbit/s 16 kbit/s	to/from PCM interface	Switching
Transparent	64 kbit/s	from µP interface	Idle code
Signaling channel bits 5..2			IOM C/I channel
Signaling channel bits 7..2			e.g. analog IOM channel
Signaling channel bits 7..0			e.g. SLD signaling channel
MFFIFO channel			Monitor channel in IOM Feature control channel in SLD

Every channel may be selected in either upstream or downstream direction. The selections for the time slots are nearly independent of each other.

The only restriction is that MFFIFO and signaling channels must be programmed to adjacent time slots, starting with the MFFIFO channel at the even time slot.

The choices of **table 1** may be programmed independently of the selected mode.

By programming the time slots, the configurable interface may be configured e.g. as a

- transparent PCM interface (plain switching function)
- IOM interface
- SLD interface

Register Description*

The following symbols are used throughout this chapter

x... don't care

u... used to ensure the intended function

n... not used. It has to be set to logical 0 in write accesses but may be switched by the EPIC to either logical level in read accesses.

Table 2
Register Set

Group	Register Name	Access Write (WR) Read (RD)	µP Interface Mode MUX. AD7..AD0	DEMUX. A3..A0/RBS	Reset Value	Register Content
PCM	PMOD	RD/WR	20_H	0_H/1	00	PCM Mode Register
	PBNR	RD/WR	22_H	1_H/1	FF	PCM Bit Number Register
	POFD	RD/WR	24_H	2_H/1	00	PCM Offset Downstream Register
	POFU	RD/WR	26_H	3_H/1	00	PCM Offset Upstream Register
	PCSR	RD/WR	28_H	4_H/1	00	PCM Clock Shift Register
	PICM	RD/WR	$2A_H$	5_H/1	–	PCM Input Comparison Mismatch Register
CFI	CMD1	RD/WR	$2C_H$	6_H/1	00	CFI Mode Register 1
	CMD2	RD/WR	$2E_H$	7_H/1	00	CFI Mode Register 2
	CBNR	RD/WR	30_H	8_H/1	FF	CFI Bit Number Register
	CTAR	RD/WR	32_H	9_H/1	00	CFI Time Slot Adjustment Register
	CBSR	RD/WR	34_H	A_H/1	00	CFI Bit Shift Register
	CSCR	RD/WR	36_H	B_H/1	00	CFI Subchannel Register
MAR	MACR	RD/WR	00_H	0_H/0	–	Memory Access Control Register
	MAAR	RD/WR	02_H	1_H/0	–	Memory Access Address Register
	MADR	RD/WR	04_H	2_H/0	–	Memory Access Data Register

* For a detailed register description, refer to the EPIC Data Sheet 10/88

Group	Register Name	Access Write (WR) Read (RD)	µP Interface Mode mux. AD7..AD0	demux. A3..A0/RBS	Reset Value	Register Content
STR	STDA	RD/WR	06_H	$3_H/0$	–	Synchron Transfer Data Register A
	STDB	RD/WR	08_H	$4_H/0$	–	Synchron Transfer Data Register B
	SARA	RD/WR	$0A_H$	$5_H/0$	–	Synchron Transfer Receive Address Register A
	SARB	RD/WR	$0C_H$	$6_H/0$	–	Synchron Transfer Receive Address Register B
	SAXA	RD/WR	$0E_H$	$7_H/0$	–	Synchron Transfer Transmit Address Register A
	SAXB	RD/WR	10_H	$8_H/0$	–	Synchron Transfer Transmit Address Register B
	SRCR	RD/WR	12_H	$9_H/0$	00	Synchron Transfer Control Register
MFCH	MFAIR	RD	14_H	$A_H/0$	Undef.	MF Channel Actice Indication Register
	MFSAR	WR	14_H	$A_H/0$	Undef.	MF Channel Subscriber Address Register
	MFFIFO	RD/WR	16_H	$B_H/0$	Empty	MF Channel FIFO
SCR	C/I FIFO	RD	18_H	$C_H/0$	Validity 0	Signaling Channel FIFO
	TIMR	WR	18_H	$C_H/0$	00	Timer Register
	STAR	RD	$1A_A$	$D_H/0$	05	Status Register
	CMDR	WR	$1A_H$	$D_H/0$	00	Command Register
	ISTA	RD	$1C_H$	$E_H/0$	00	Interrupt Status Register
	MASK	WR	$1C_H$	$E_H/0$	00	Mask Register
	OMDR	RD/WR	$1E_H/3E_H$	F_H/X	00	Operation Mode Register
	VNSR	RD	$3A_H$	$D_H/1$		Version Number Register

Note: In the multiplexed µP interface mode AD0 is not used for address coding.

Absolute Maximum Ratings

Description	Symbol	Limit Values	Unit
Ambient temperature under bias	T_A	0 to 70	°C
Storage temperature	T_{stg}	−65 to 125	°C

DC Characteristics

$T_A = 0$ to 70 °C; $V_{DD} = 5$ V, $V_{SS} = 0$ V

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit	Test Conditions
L-input voltage	V_{IL}	−0.4	0.8	V	
H-input voltage	V_{IH}	2.0	V_{DD} +0.4	V	
L-output voltage	V_{OL}		0.45	V	$I_{OL} = 2$ mA
H-output voltage	V_{OH}	2.4		V	$I_{OH} = -400$ µA
H-output voltage	V_{OH}	V_{DD} −0.5		V	$I_{OH} = -100$ µA
Operational power supply current					$V_{DD} = 5$ V, input at 0 V or V_{DD}, no output loads
	I_{CC}		9.5	mA	clock frequency > 4096 kHz
	I_{CC}		6.5	mA	clock frequency ≤ 4096 kHz
Input leakage current	I_{LI}		10	µA	$0 V < V_{IN} < V_{DD}$ to 0 V
Output leakage current	I_{LO}		10	µA	$0 V < V_{OUT} < V_{DD}$ to 0 V

Capacitances

$T_A = 25\,°C$; $V_{DD} = 5\,V$, $V_{SS} = 0\,V$

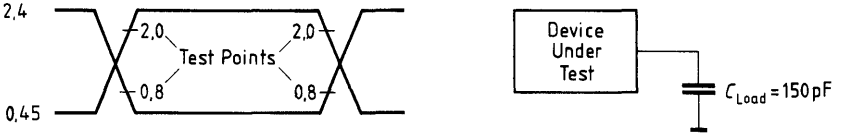
Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input capacitance	C_{IN}		10	pF
I/O capacitance	C_{IO}		20	pF
Output capacitance	C_{OUT}		15	pF

AC Characteristics

Ambient temperature under bias range, $V_{DD} = 5\,V \pm 5\%$

Inputs are driven at 2.4 V for a logical 1 and at 0.4 V for a logical 0. Timing measurements are made at 2.0 V for a logical 1 and at 0.8 V for a logical 0. The AC testing input/output waveforms are shown below.

Figure 21
I/O Waveform for AC Tests

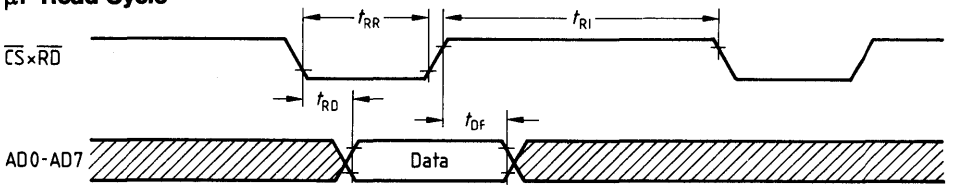


Microprocessor Interface Timing Parameters

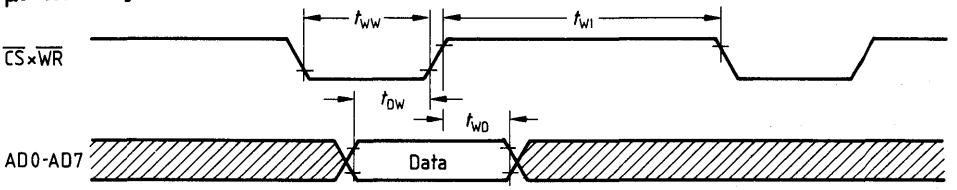
Parameter	Symbol	Limit Values		Unit
		min.	max.	
ALE pulse width	t_{AA}	30		ns
Address setup time to ALE	t_{AL}	10		ns
Address hold time form ALE	t_{LA}	20		ns
Address latch setup time to $\overline{WR}$, $\overline{RD}$	t_{ALS}	0		ns
Address setup time to $\overline{WR}$, $\overline{RD}$	t_{AS}	10		ns
Address hold time from $\overline{WR}$, $\overline{RD}$	t_{AH}	25		ns
$\overline{RD}$ delay after WR setup	t_{DSD}	0		ns
$\overline{RD}$ pulse width	t_{RR}	120		ns
Data output delay from $\overline{RD}$	t_{RD}		100	ns
Data float from $\overline{RD}$	t_{DF}		25	ns
$\overline{RD}$ control interval	t_{RI}	70		ns
$\overline{WR}$ pulse width	t_{WW}	60		ns
Data setup time to $\overline{WR}$ + $\overline{CS}$	t_{DW}	30		ns
Data hold time from $\overline{WR}$ + $\overline{CS}$	t_{WD}	10		ns
$\overline{WR}$ control interval	t_{WI}	70		ns

INTEL Bus Mode

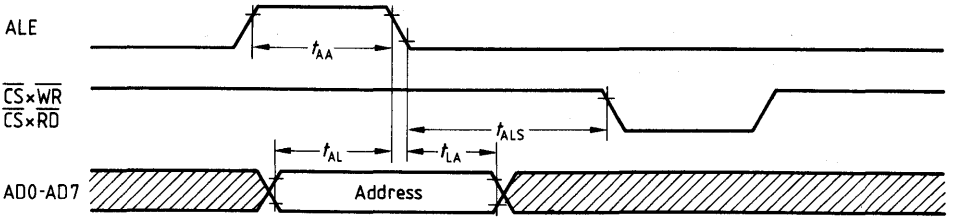
µP Read Cycle



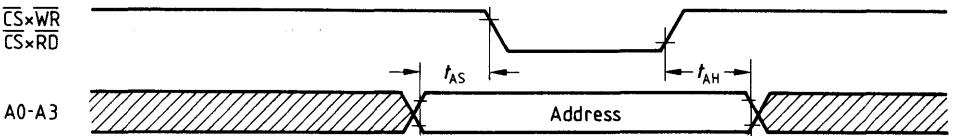
µP Write Cycle



Multiplexed Address Timing

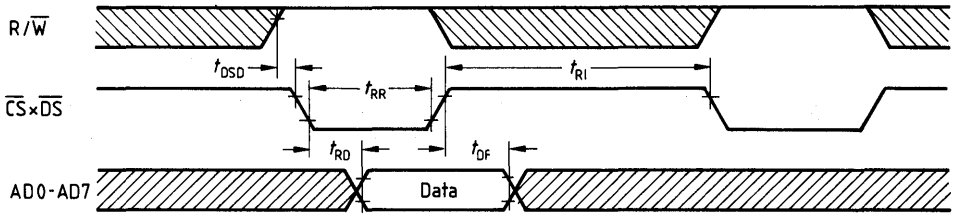


Demultiplexed Address Timing

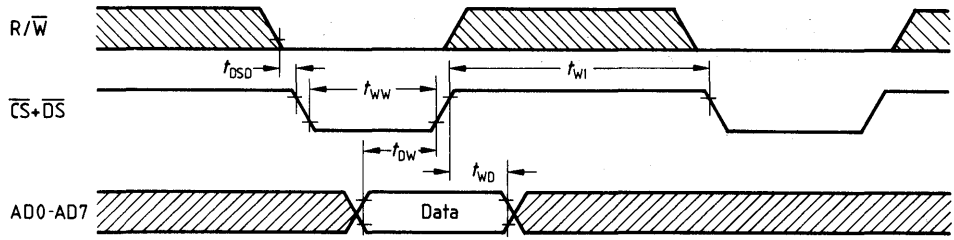


Motorola Bus Mode

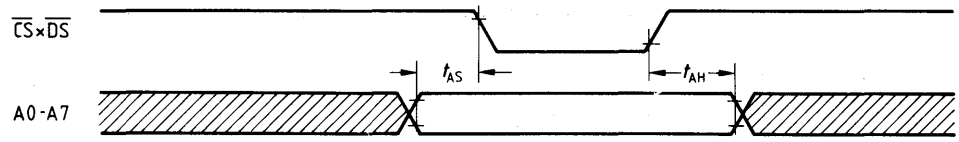
µP Read Cycle



µP Write Cycle



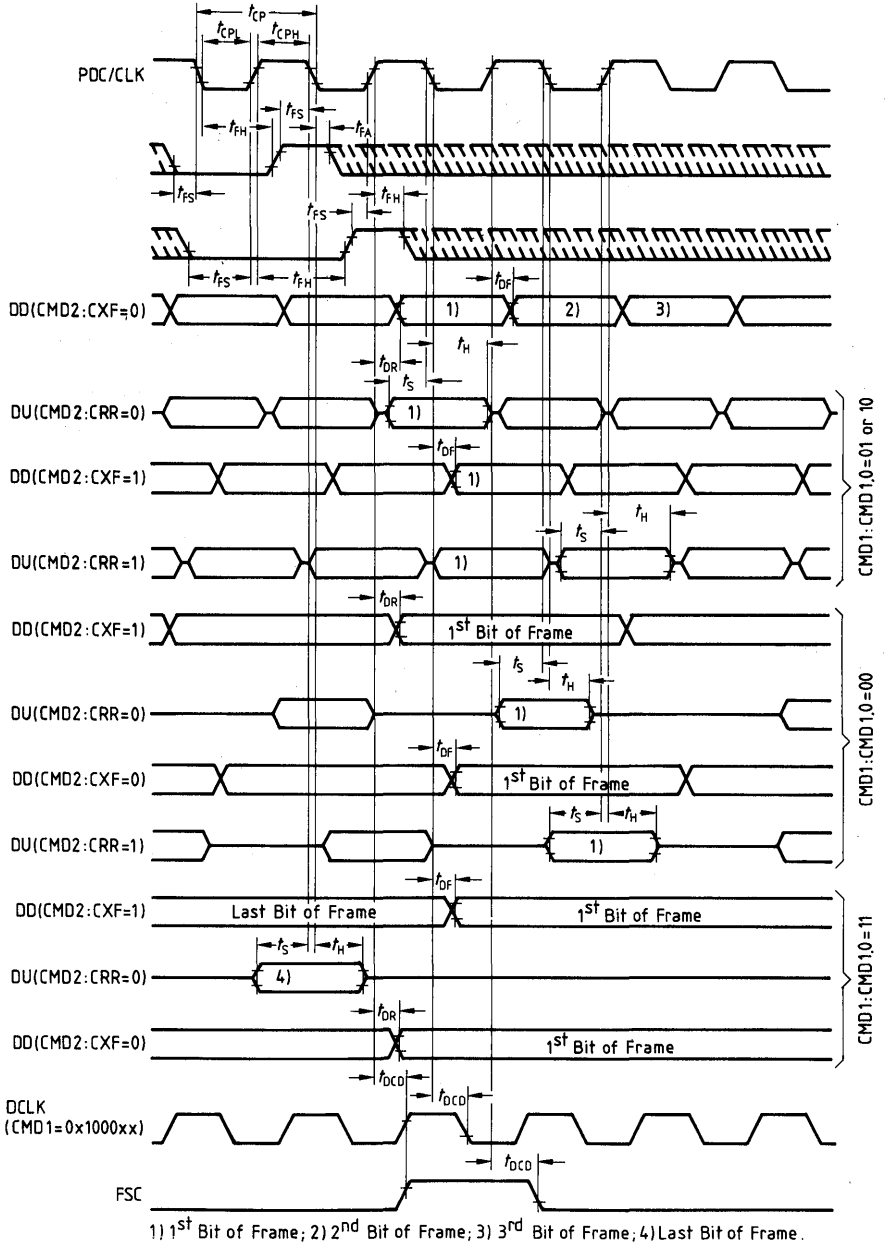
Address Timing



Timing of PCM and Configurable Interfaces

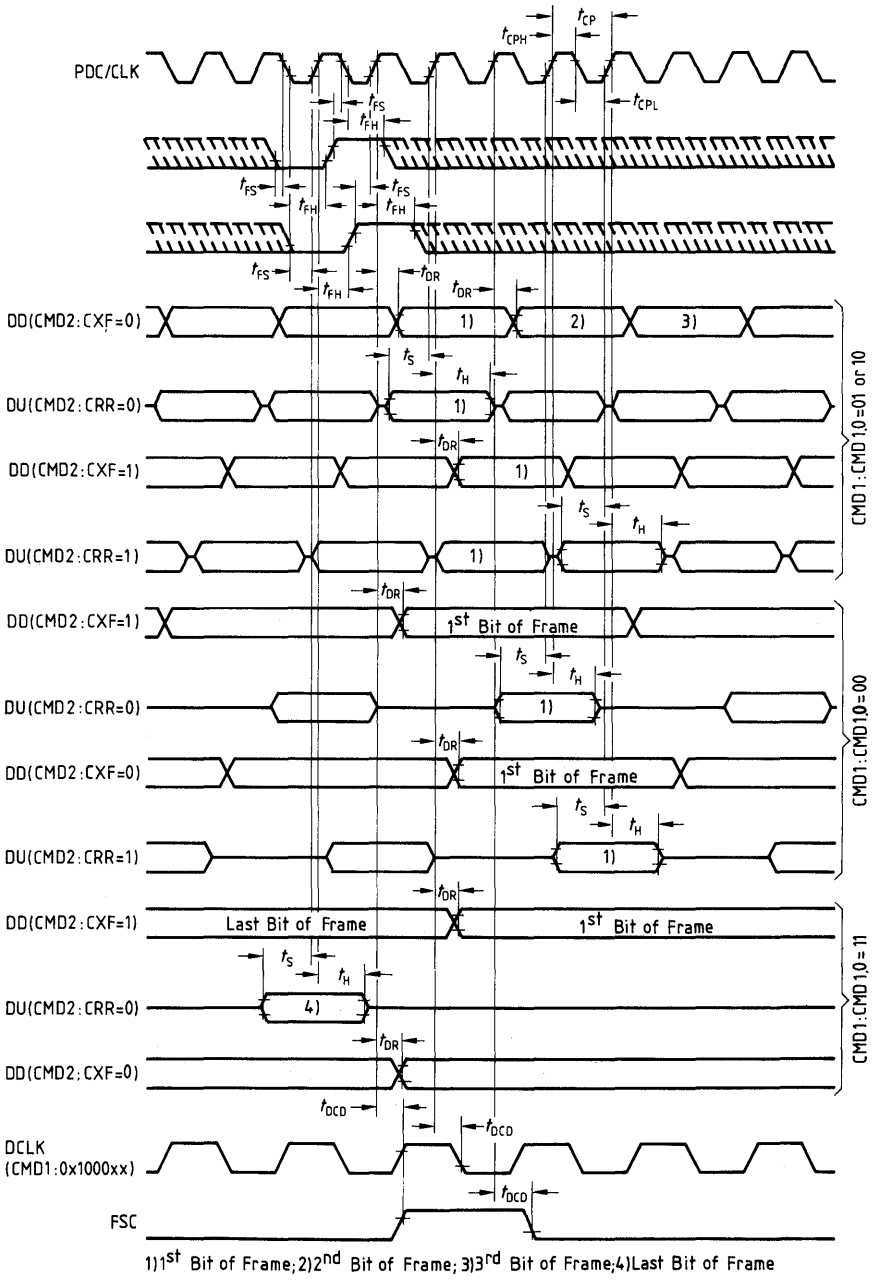
Parameter	Symbol	Limit Values min.	Limit Values max.	Unit	Conditions
Clock period Clock period low Clock period high	t_{CP} t_{CPL} t_{CPH}	240 80 100		ns ns ns	clock frequency ≤ 4096 kHz
Clock period Clock period low Clock period high	t_{CP} t_{CPL} t_{CPH}	120 50 50		ns ns ns	clock frequency > 4096 kHz
Frame setup time Frame hold time	t_{FS} t_{FH}	15 50		ns ns	
Data clock delay time	t_{DCD}		125	ns	
Serial data input setup time Serial data input hold time	t_S t_H	5 35		ns ns	PCM input data frequency > 4096 kbit/s
Serial data input setup time Serial data input hold time	t_S t_H	15 50		ns ns	PCM input data frequency ≤ 4096 kbit/s
Serial data input setup time Serial data input	t_S t_H	15 50		ns ns	CFI input data frequency > 4096 kbit/s
Serial data input setup time Serial data input hold time	t_S t_H	0 75		ns ns	CFI input data frequency ≤ 4096 kbit/s
PCM serial data output delay time	t_D		55	ns	
Tristate control delay	t_T		60	ns	
CFI serial data output delay time (falling clock edge)	t_{DF}		60	ns	
CFI serial data output delay time (rising clock edge)	t_{DR}		80	ns	

AC Characteristics at the CFI with CMD: CSP 1.0 = 10 (Prescaler Divisor = 1)



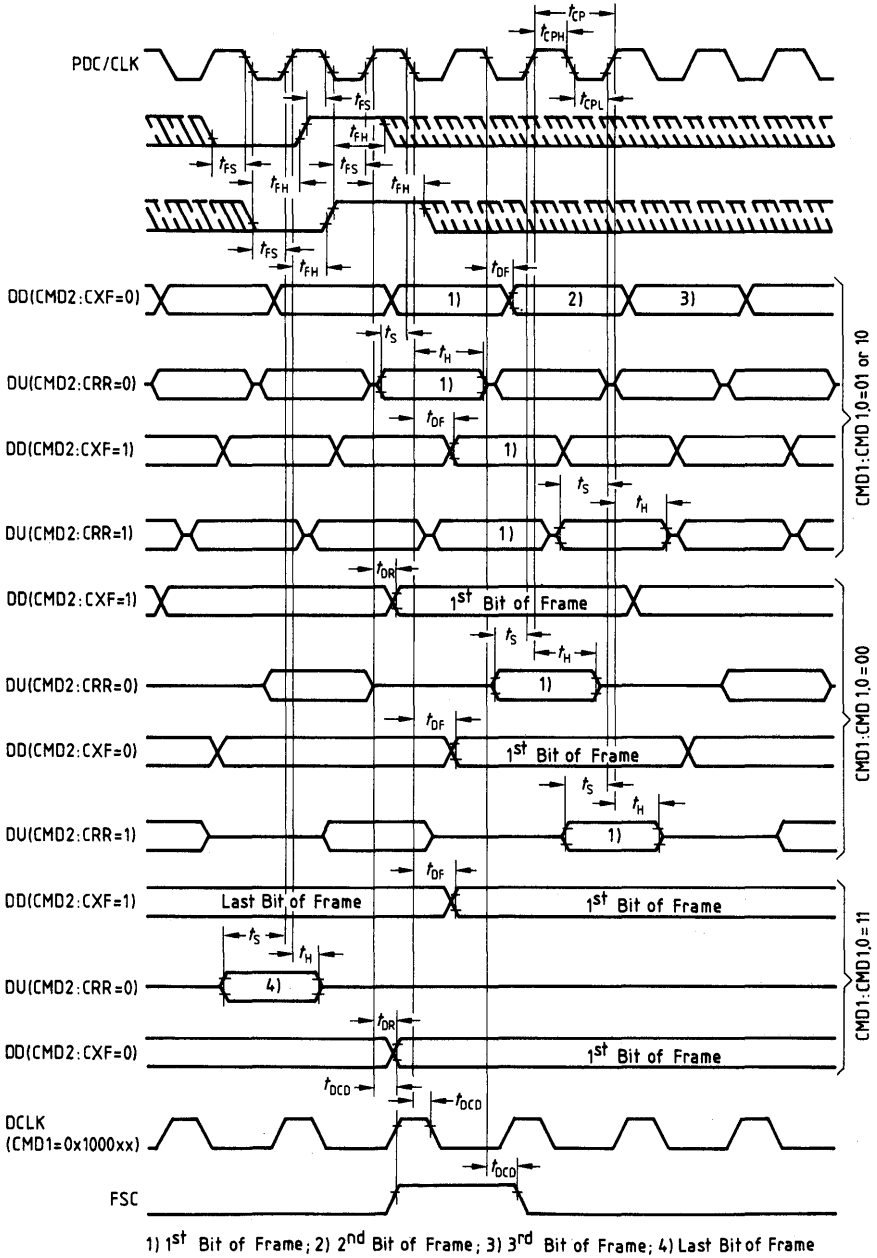
1) 1st Bit of Frame; 2) 2nd Bit of Frame; 3) 3rd Bit of Frame; 4) Last Bit of Frame.

AC Characteristics at the CFI with CMD: CSP 1.0 = 00 (Prescaler Divisor = 2)



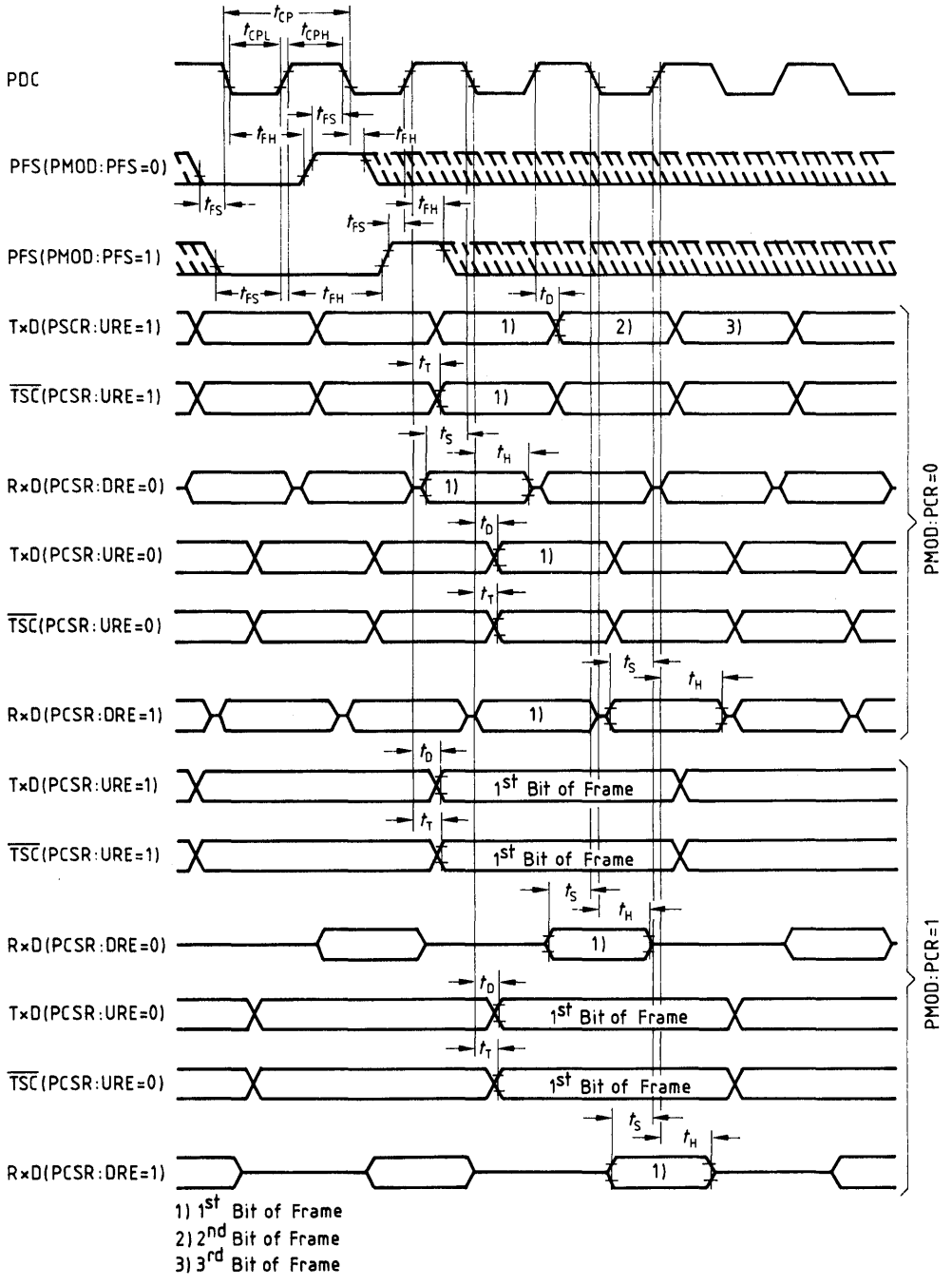
1)1st Bit of Frame; 2)2nd Bit of Frame; 3)3rd Bit of Frame; 4)Last Bit of Frame

AC Characteristics at the CFI with CMD1 : CSP = 01 (Prescaler Divisor)



1) 1st Bit of Frame; 2) 2nd Bit of Frame; 3) 3rd Bit of Frame; 4) Last Bit of Frame

AC Characteristics at the PCM Interface



1) 1st Bit of Frame
2) 2nd Bit of Frame
3) 3rd Bit of Frame

Extended PCM Interface Controller (EPIC-2) PEB 2056

Preliminary Data **CMOS IC**

Type	Ordering Code	Package
PEB 2056-C	Q67100-H6117	C-DIP-28
PEB 2056-N	Q67100-H6116	PL-CC-44 (SMD)
PEB 2056-P	Q67100-H6115	P-DIP-28

The EPIC™-2 is a smaller version of the EPIC™-1. The functions that are performed remain essentially the same but the EPIC-2 has been optimized for time-slot assignment and switching functions on line cards with up to 8 ISDN subscriber lines:

EPIC™-1:
4 IOM® interfaces
4 PCM highways

Up to 32 ISDN subscribers

P-DIP-40/PL-CC-44 packages

EPIC™-2:
1 IOM® interfaces
2 PCM highways

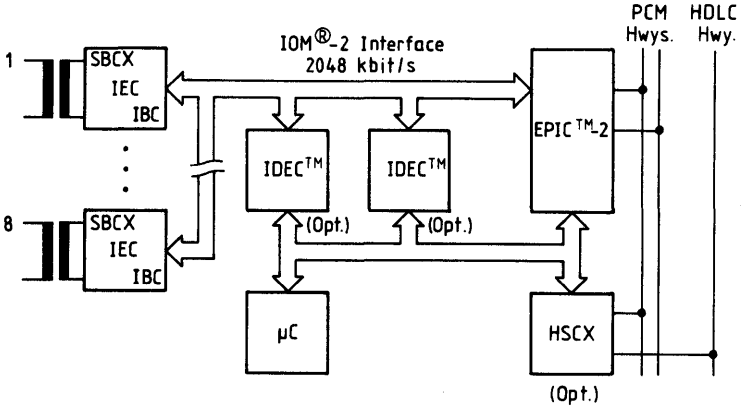
Up to 8 ISDN subscribers

P-DIP-44/PL-CC-44 packages

Features

- PCM interface controller for up to 8 ISDN or 16 analog subscribers
- Time-slot assignment freely programmable for all subscribers
- Non-blocking switch for 24 channels (16B + 8D)
- Switching of 16 and 64 kbit/s channels
- Two serial interfaces: PCM and IOM®-2
- Interfacing to two full duplex PCM highways (1.5, 2 or 4 Mbit/s)
- Change detection ("last-look") logic for C/I channel
- Buffering for monitor channel
- Standard parallel µP interface
- Advanced low power CMOS technology

8 ISDN Subscribers per PCM Interface Controller (EPIC-2)



SIEMENS

ISDN Communication Controller (ICC) PEB 2070

Preliminary Data **CMOS IC**

Type	Ordering Code	Package
PEB 2070-C	Q67100-H8328	C-DIP-24
PEB 2070-N	Q67100-H8394	PL-CC-28 (SMD)
PEB 2070-P	Q67100-H2953	P-DIP-24

The transmission and protocol functions in an ISDN basic access can all be implemented using the CMOS circuits of the ISDN Oriented Modular (IOM® -1) chip set. While three chips, the S Bus interface Circuit SBC (PEB 2080), the ISDN Echo Cancellation circuit IEC (PEB 2090) and the ISDN Burst Controller IBC (PEB 2095) perform the transmission functions in different applications (S- and U-Interface), the ISDN Communication Controller ICC (PEB 2070) acts as the D-channel-link-access protocol controller.

The IOM architecture makes possible a wide range of configurations for the basic access, using the basic devices. These configurations essentially differ in the implementation of the layer-1 OSI functions, while the layer-2 functions are provided by the ICC for all configurations.

In addition to that, the PEB 2070 provides the interface to B-channel sources in the terminal and to a peripheral board controller (PEB 2050, 51, 52 etc.) at the exchange.

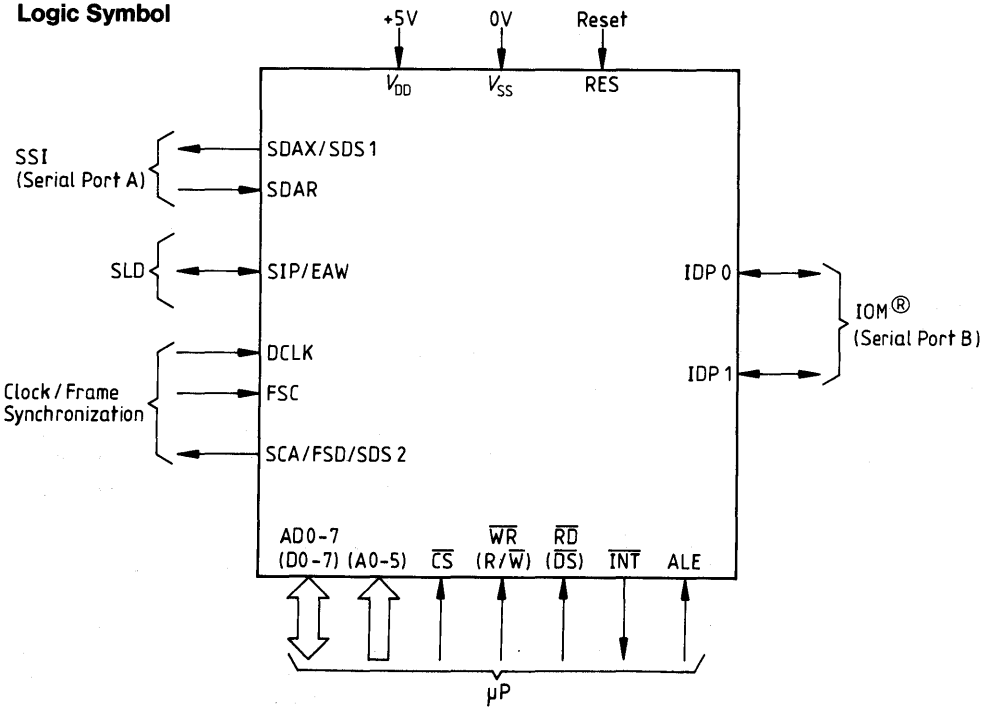
The HDLC packets of the ISDN D channel are handled by the ICC which transfers them to the associated microcontroller. The ICC has on-chip buffer memories (64 bytes per direction) for the temporary storage of data packets. Because of the overlapping I/O operations the maximum length of the D-channel packets is not limited. In one of its operating modes the device offers high level support of layer-2 functions of the LAPD protocol.

A side from ISDN applications, the ICC can be used as a general purpose communication controller in all applications calling for LAPD, LAPB or other HDLC/SDLC based protocols.

Features

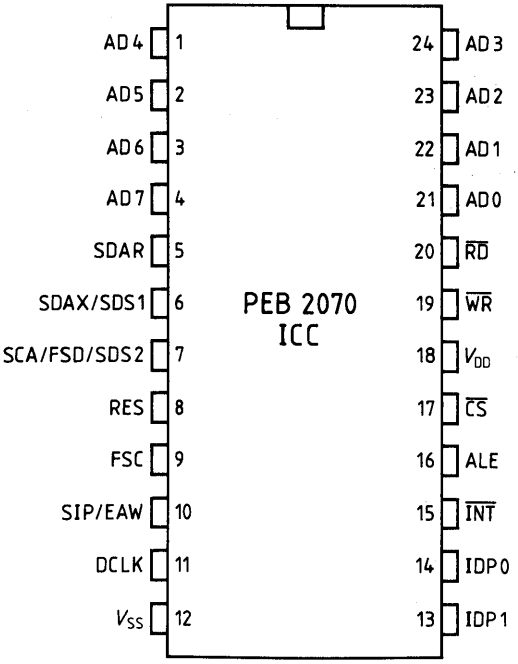
- Support of LAPD protocol
- Different types of operating modes for increased flexibility
- FIFO buffer (2 x 64 bytes) for efficient transfer of data packets
- Serial Interfaces: IOM-1, SLD, SSI
  IOM-2
- General purpose HDLC communication interface
- Implementation of IOM-1/IOM-2 monitor and C/I channel protocol to control layer-1 and peripheral devices
- D-channel access with contention resolution mechanism
- µP access to B channels and intercommunication channels
- B-channel switching
- Watchdog timer
- Test loops
- Advanced CMOS technology
- Low power consumption: active :17 mW (IOM-2)
  : 8 mW (IOM-1)
  standby : 3 mW

Logic Symbol

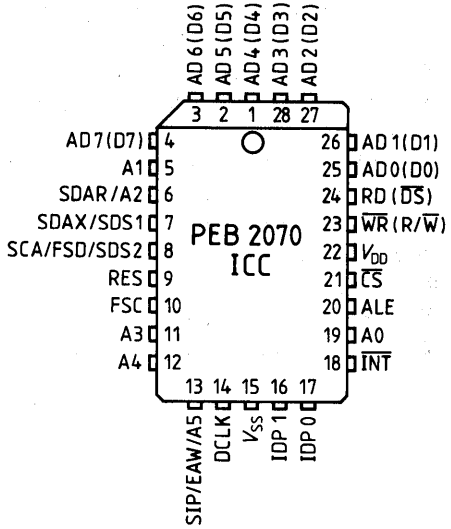


Pin Configuration
(top view)

P-DIP-24



PL-CC-28



Pin Definitions and Functions

Pin No. P-DIP	Pin No. PL-CC	Symbol	Input (I) Output (O)	Function
21	25	AD0/D0	I/O	**Multiplexed Bus Mode:** Address/Data bus. Transfers addresses from the µP system to the ICC and data between the µP system and the ICC. **Non Multiplexed Bus Mode:** Data bus. Transfers data between the µP system and the ICC.
22	26	AD1/D1	I/O	
23	27	AD2/D2	I/O	
24	28	AD3/D3	I/O	
1	1	AD4/D4	I/O	
2	2	AD5/D5	I/O	
3	3	AD6/D6	I/O	
4	4	AD7/D7	I/O	
17	21	$\overline{CS}$	I	**Chip Select.** A "Low" on this line selects the ICC for a read/write operation.

Pin Definitions and Functions (cont'd)

Pin No. P-DIP	Pin No. PL-CC	Symbol	Input (I) Output (O)	Function
–	23	R/$\overline{W}$	I	**Read/Write.** When "High", identifies a vaild µP access as a read operation. When "Low", identifies a valid µP access as a write operation (Motorola bus mode).
19	23	$\overline{WR}$	I	Write. This signal indicates a write operation (Siemens/Intel bus mode).
–	24	$\overline{DS}$	I	**Data Strobe.** The rising edge marks the end of a valid read or write operation (Motorola bus mode).
20	24	$\overline{RD}$	I	Read. This signal indicates a read operation (Siemens/Intel bus mode).
15	18	$\overline{INT}$	OD	**Interrupt Request.** The signal is activated when the ICC request an interrupt. It is an open drain output.
16	20	ALE	I	**Address Latch Enable.** A high on this line indicates an address on the external address bus (Multiplexed bus type only).
7	8	SCA	O	**Serial Clock Port A,** IOM-1 timimg mode. A 128-kHz-data clock signal for serial port A (SSI).
7	8	FSD	O	**Frame Sync Delayed,** IOM-1 timing mode 1. An 8-kHz-synchronization signal, delayed by 1/8 of a frame, for IOM-1 is supplied. In this mode a minimal round-trip delay for B1 and B2 channels is guaranteed.
7	8	SDS2	O	**Serial Data Strobe 2,** IOM-2 mode. A programmable strobe signal, selecting either one or two B or IC channels on IOM-2 interface, is supplied via this line. After reset, SCA/FSD/SDS2 takes on the function of SDS2 until a write access to SPCR is made.
8	9	RES	I/O	**Reset.** A "High" on this input forces the ICC into reset state. The minimum pulse length is four clock periods. If the terminal specific functions are enabled, the ICC may also supply a reset signal.

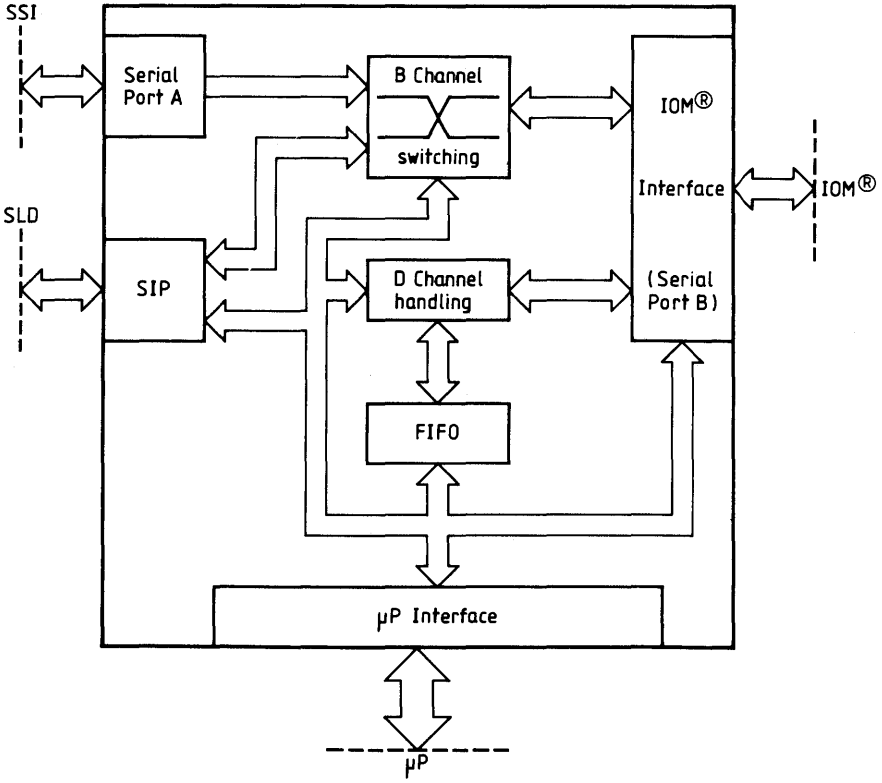
Pin Definitions and Functions (cont'd)

Pin No. P-DIP	Pin No. PL-CC	Symbol	Input (I) Output (O)	Function
9	10	FSC	I	**Frame Sync.** Input synchronization signal. IOM-2 mode: Indicates the beginning of IOM frame. IOM-2 mode: Indicates the beginning of IOM and, if TSF = 0, frame (timing mode 0). Indicates the beginning of SLD frame (timing mode 1). HDLC mode: Strobe signal of programmable polarity
11	14	DCLK	I	**Data Clock.** IOM modes: Clock of frequency equal to twice the data rate on the IOM interface. HDLC mode: Clock of frequency equal to the data rate on serial port B.
	19	A0	I	**Address** bit 0 (Non-multiplexed bus type).
	5	A1	I	**Address** bit 1 (Non-multiplexed bus type).
	6	A2	I	**Address** bit 2 (Non-multiplexed bus type).
6	6	SDAR	I	**Serial Data Port Receive.** Serial data is received on this pin at standard TTL or CMOS level. An integrated pull-up circuit enables connection of an open-drain/ open collector driver without an external pull-up resistor. SDAR is used only if IOM-1 mode is selected.
	11	A3	I	**Address** bit 3 (Non-multiplexed bus type).
	12	A4	I	**Address** bit 4 (Non-multiplexed bus type).
	13	A5	I	**Address** bit 5 (Non-multiplexed bus type).
10	13	SIP	I/O	SLD Interface Port, IOM-1 mode. This line transmits and receives serial data at standard TTL or CMOS levels.
10	13	EAW	I	**External Awake** (terminal specific function). If a falling edge on this input is detected, the ICC generates an interrupt and, if enabled, a reset pulse.

Pin Definitions and Functions (cont'd)

Pin No. P-DIP	Pin No. PL-CC	Symbol	Input (I) Output (O)	Function
6	7	SDAX	0	**Serial Data Port A** transmit, IOM-1 mode. Transmit data is shifted out via this pin at standard TTL or CMOS levels.
6	7	SDS1	0	**Serial Data Strobe** 1, IOM-2 mode. A programmable strobe signal, selecting either one or two B or IC channels on IOM-2 interface, is supplied via this line. After reset, SDAX/SDS1 takes on the function of SDS1 until a write access to SPCR is made.
12	15	V_{SS}	–	Ground (0 V)
18	22	V_{DD}	–	Power supply (5 V ± 5%)
14	17	IDP0	I/O	**IOM Data Port 0, 1**
13	16	IDP1	I/O	

Block Diagram



System Integration

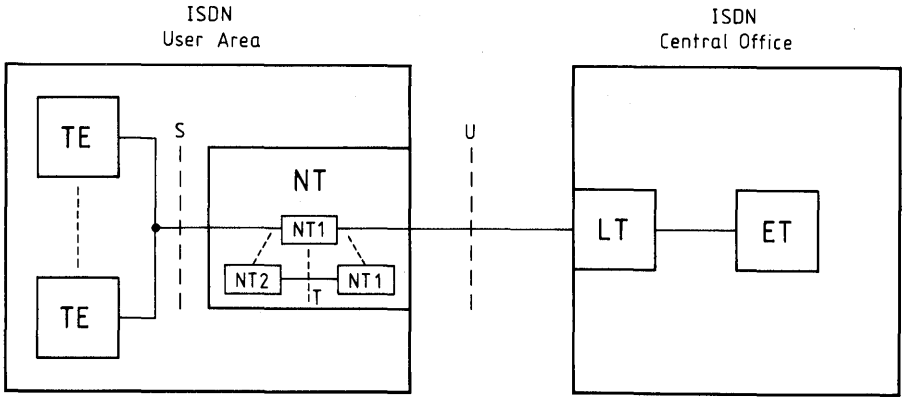
ISDN Applications

The reference model for the ISDN basic access according to CCITT I series recommendations consists of

- an exchange and trunk line termination in the central office (ET, LT)
- a remote network termination in the user area (NT)
- a two-wire loop (U interface) between NT and LT
- a four-wire link (S interface) which connects subscriber terminals and the NT in the user area as depicted in **figure 1.**

Figure 1

ISDN Subscriber Basic Access Architecture

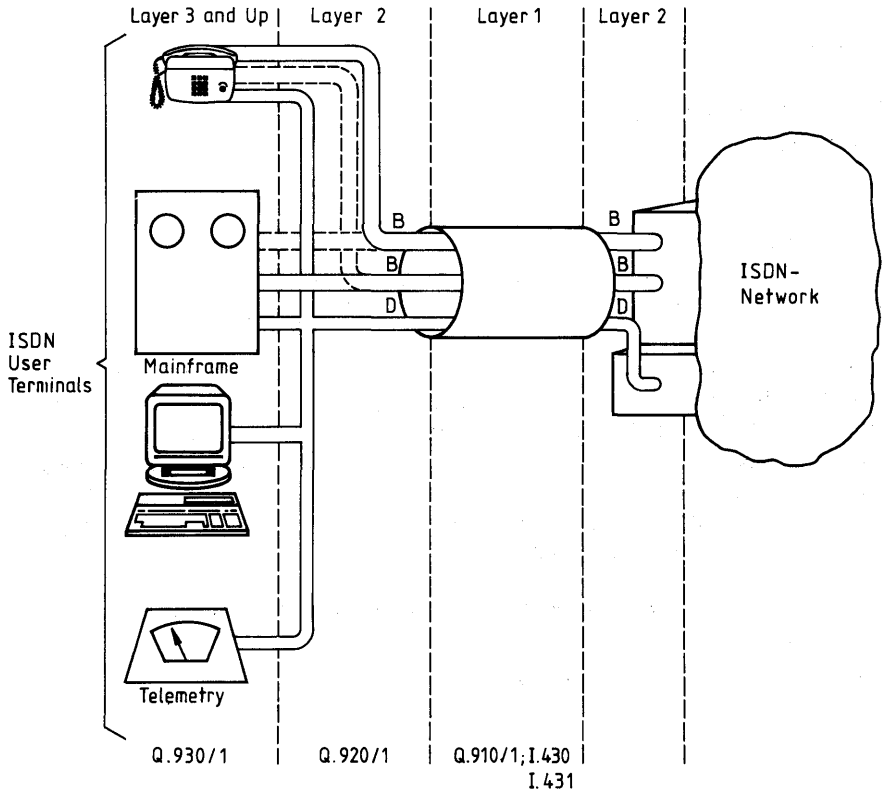


The NT equipment serves as a converter between the U interface at the exchange and the S interface at the subscriber premises. The NT may consist of either an NT1 only or an NT1 together with an NT2 connected via the T interface which is physically identical to the S interface. The NT1 is a direct transformation between layer-1 of S and layer-1 of U. NT2 may include higher level functions like multiplexing and switching as in a PBX.

In terms of channels the ISDN access consists of:

- a number of 64 kbit/s bearer channels (n x B)
  e.g. n = 2 for basic rate ISDN access
  n = 30 or 23 for primary rate ISDN access;
- and a signaling channel (D), either 16 (basic rate) or 64 (primary rate) kbit/s.

Figure 2
ISDN Basic Access Channel Structure



The B channels are used for end-to-end circuit switched digital connections between communicating stations.

The D channel is used to carry signaling and data via protocols defined by the CCITT. These protocols cover the network services layers of the open system interconnection model (layers 1-3). At layer-2, the data link layer, an HDLC type protocol is employed, the Link Access Procedure on the D channel LAPD (CCITT Rec. Q.920/1).

The ISDN communication controller PEB 2070 can be used in all ISDN applications involving establishment and maintenance of a data link connection in either the D channel or B channel. It also provides the interface to layer-1 functions controlled via the IOM which links the ICC to any transceiver or peripheral device. Depending on the interface mode, the ICC supports three serial interfaces and offers switching functions and µP access to voice/data channels.

The applications comprise:
- Use as a signaling controller for the D channel
- Access to the D channel for data transmission
- Source/sink for secured B channel data

and the target equipment include:
- ISDN terminal
- ISDN PBX (NT2) and Central Office (ET) line card
- ISDN packet switches
- "Intelligent" NT1.

Terminal Applications

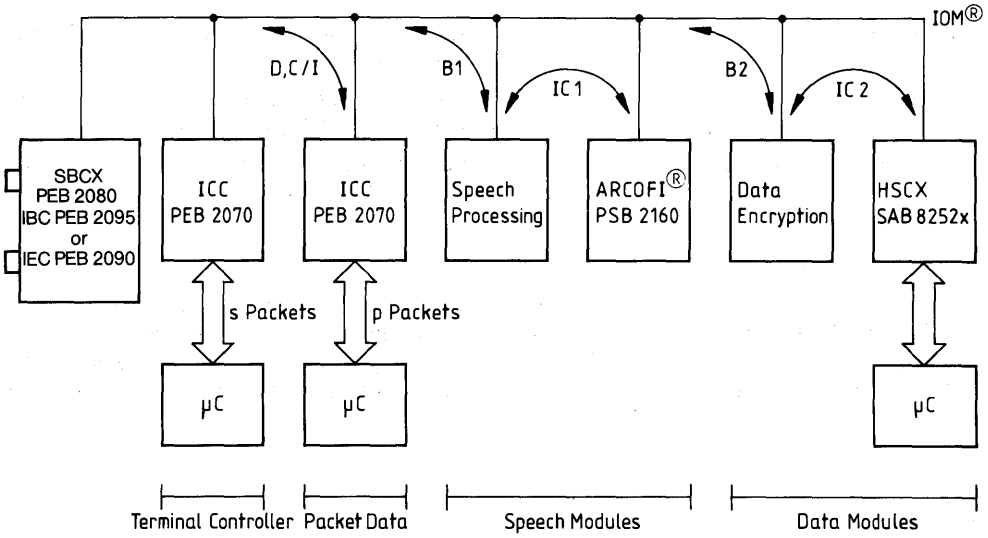
The concept of the ISDN basic access is based on two circuit-switched 64-kbit/s B channels and a message oriented 16-kbit/s D channel for packetized data, signaling and telemetry information.

Figure 3 shows an example of an integrated **multifunctional ISDN** terminal using the ICC. The transceiver provides the layer-1 connection to the transmission line, either an S or a U interface, and is connected to the ICC and other, peripheral modules via the IOM interface.

The D channel, containing signaling data and packet switched data, is processed by the ICC LAPD controller and routed via a parallel µP interface to the terminal processor. The high level support of the LAPD protocol which is implemented by the ICC allows the use of a low cost processor in cost sensitive applications.

The IOM interface is used to connect diverse voice/data application modules:
- sources/sinks for the D channel
- sources/sinks for the B1 and B2 channels.

Figure 3
Example of ISDN Voice/Data Terminal



Different D channel services (for different SAPI's) can be simply implemented by connecting an additional ICC in parallel to the first one, for instance for transmitting p-packets in the D channel.

Up to eight ICCs may thus be connected to the D and C/I (Command/Indication) channels. The ICCs handle contention autonomously.

Data transfers between the terminal controller and the different modules are done with the help of the IOM monitor channel protocol. Each voice/data module can be accessed by an individual address. The same protocol enables the control of terminal modules that do not have an associated microcontroller (such as the Audio Ringing Codec Filter ARCOFI®: PSB 2160) and the programming of intercommunication inside the terminal. Two intercommunication channels IC1 and IC2 allow a 2 x 64 kbit/s transfer rate between voice/data modules.

In the example above **(figure 3)**, one ICC is used for data packets in the D channel. A voice processor is connected to a programmable digital signal processing codec filter via IC1 and a data encryption module to a data device via IC2. B1 is used for voice communication, B2 for data communication.

The ICC ensures full upward compatibility with IOM-1 devices. It provides the additional strobe, clock and data lines for connecting standard combos or data devices via IOM, or serial SLD and SSI interfaces. The strobe signals and the switching of B channels is programmable.

Line Card Applications

An example of the use of the ICC on an **ISDN LT + ET line card** (decentralized architecture) is shown in **figure 4.**

The transceivers (ISDN Echo Cancellation Circuit IEC: PEB 2090) are connected to an Extended PCM interface Controller (EPIC PEB 2055) via an IOM interface.

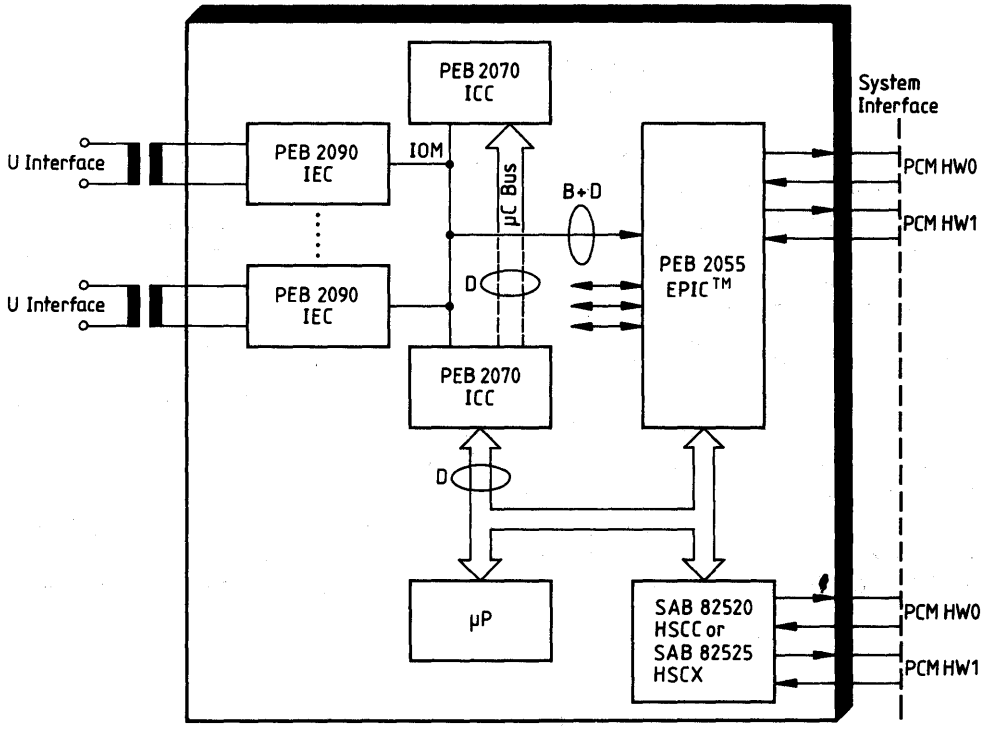
This interface carries the control and data for up to eight subscribers using time division multiplexing. The ICCs are connected in parallel on IOM, one ICC per subscriber.

The EPIC performs dynamic B and D channel assignment on the PCM highways. Since this component supports four IOM interfaces, up to 32 subscribers may be accommodated.

Other Applications

If programmed in non-ISDN mode, the ICC serial port B operates as an HDLC communication link without IOM frame structure. This allows the use of the ICC as a general purpose communication controller. The valid HDLC data is marked by a strobe signal on serial port B. Examples of the use of the ICC are: X.25 packet controllers, terminal adaptors, and packet transmission e.g. in primary rate/DMI systems.

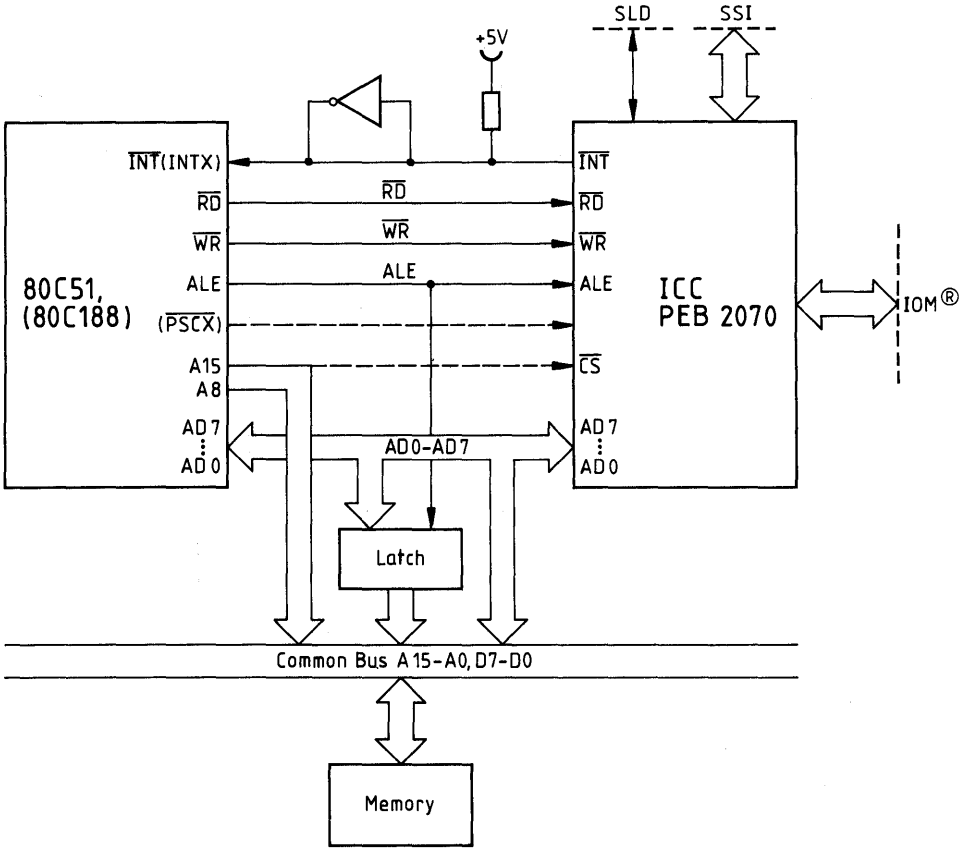
Figure 4
ISDN Line Card Implementation



Microprocessor Environment

The ICC is especially suitable for cost-sensitive applications with single-chip microcontrollers (e.g. 8048, 8031, 8051). However, due to its programmable micro interface and non-critical bus timing, it fits perfectly into almost any 8-bit microprocessor system environment. The microcontroller interface can be selected to be either of the Motorola type (with control signals $\overline{CS}$, R/$\overline{W}$, $\overline{DS}$), of the Siemens/Intel non-multiplexed bus type (with control signals CS, WR, RD) or of the Siemens/Intel multiplexed address/data bus type ($\overline{CS}$, $\overline{WR}$, $\overline{RD}$, ALE).

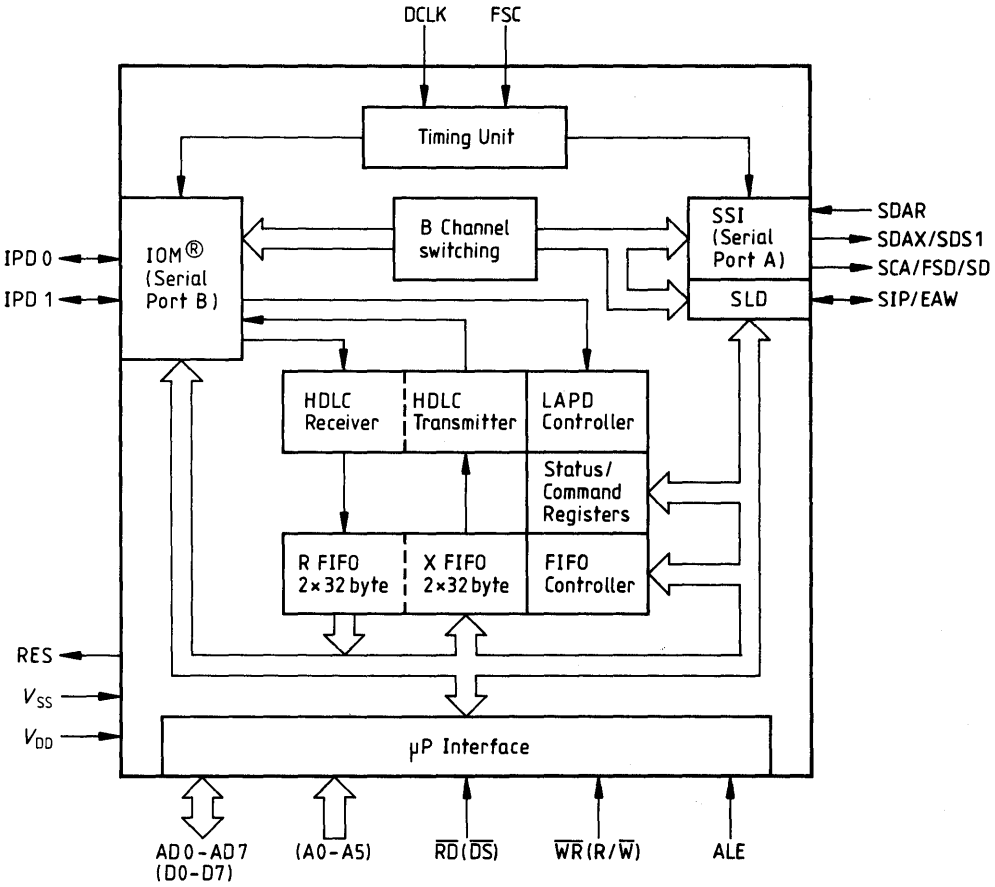
Figure 5
Example of ICC Microcontroller Environment



Functional Description

General Functions and Device Architecture

Figure 6
Architecture of the ICC



The functional block diagram in **figure 6** shows the ICC to consist of:

- serial interface logic for the IOM, SLD and SSI interfaces with B channel switching capabilities
- logic necessery to handle the D channel messages (layer 2).

The latter consists of an HDLC receiver and an HDLC transmitter together with 64-byte deep FIFO's for efficient transfer of the messages to/from the user's CPU.

In a special HDLC controller operating mode, the auto mode, the ICC processes protocol handshakes (I- and S-frames) of the LAPD (Link Access Procedure on the D channel) autonomously.

Control and monitor functions as well as data transfers between the user's CPU and the D and B channels are performed by the 8-bit parallel µP interface logic.

The IOM interface logic allows interaction between layer-1 and layer-2 functions. It implements D-channel collision resolution for connecting other layer-2 devices to the IOM interface, and the C/I and monitor channel protocols (IOM-1/IOM-2) to control peripheral devices.

The timing unit is responsible for the system clock and frame synchronization.

Serial Interface Modes

The PEB 2070 can be used in different modes of operation:

- IOM-1 Mode
- IOM-2 Mode
- HDLC Controller Mode.

These modes are selected via bit IMS (Interface Mode Select) in ADF2 register and bits DIM 2-0 (Digital Interface Mode) in MODE register. **See table 1.**

Table 1
Interface Modes

IMS	DIM2	Mode
0	0	IOM-1 Mode
	1	HDLC Mode
1	X	IOM-2 Mode

IOM 1 Mode (IMS = 0, DIM2 = 0)

Serial Port B is used as the IOM-1 interface, which connects the ICC to a layer-1 component.

The HDLC controller is always connected to the D channel of IOM-1 interface.

Two additional serial interfaces are available in this mode, the Synchronous Serial Interface SSI (serial port A) and the Subscriber Line Datalink (SLD) interface.

The SSI is used especially in ISDN terminal applications for the connection of B channel sources/sinks. It is available if timing mode 0 (bit SPM = 0, SPCR register) is programmed.

The SLD is used:

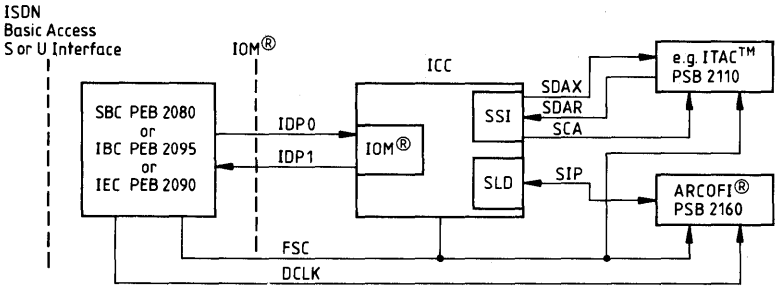
- in ISDN terminal applications for the connection of SLD compatible B channel devices
- in line card applications for the connection of a peripheral line board controller (e.g. PEB 2050).

The connections of the serial interfaces in both terminal and exchange applications are shown in **figure 7.**

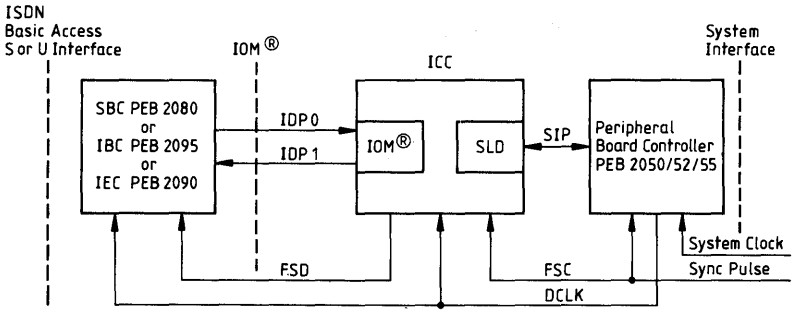
The SSI interface is only available in timing mode 0 (SPM = 0). Timing mode 1 (SPM = 1) is only applicable in exchange applications **(figure 7b)** and is used to minimize the B channel round-trip delay time for the SLD interface. Refer to section **ISDN Oriented Modular Interface.**

Figure 7

ICC Interface in IOM-1 Mode



(a) Timing Mode 0 (SPM = 0)



(b) Timing Mode 1 (SMP = 1)

The characteristics of the IOM interface are determined by bits DIM1, 0 as shown in **table 2.**

Table 2
IOM-1 Interface Mode Characteristics

DIM1	DIM0	Characteristics
0	0	Monitor channel upstream is used for TIC bus access.
0	1	Monitor channel upstream is used for TIC bus access. Bit 3 of monitor channel downstream is evaluated to control D-channel transmissions.
1	0	Monitor channel is used for TIC bus access and for data transfer.
1	1	Monitor channel is used for TIC bus access, for data transfer and for D-channel access control.

IOM-2 Mode (IMS = 1)

Serial port B is operated as an IOM-2 interface for the connection of layer-1 devices, and as a general purpose backplane bus in terminal equipment. The auxiliary serial SSI and SLD interfaces are not available in this case.

The functions carried out by the IOM are determined by bits SPM (terminal mode/non terminal mode) and DIM2-0, as shown in **table 3**.

Table 3
IOM-2 Interface Mode Characteristics

DIM2	DIM1	DIM0	Characteristics
HDLC in D channel:			Last octet of IOM channel 2 is used for TIC bus access.
0	0	0	Applicable in terminal mode (SPM = 0).
0	0	1	Last octet of IOM channel 2 is used for TIC bus access, bit 5 of last octet is evaluated to control D-channel transmission. Applicable in terminal mode (SPM = 0).
0	1	0	No TIC bus access and no S bus D-channel access control. Applicable in terminal and non-terminal mode.
0	1	1	Bit 5 of last octet is evaluated to control D-channel transmission. Applicable in terminal mode (SPM = 0).
HDLC in B or IC channel:			No transmission/reception in D channel.
1	1	0	HDLC channel selected by D1C2-0.

Note: In IOM-2 terminal mode (SPM = 0, 12-byte IOM-2 frame), all DIM2-0 combinations are meaningful. When IOM-2 non-terminal mode is programmed (SPM = 1), the only meaningful combination is "10".

HDLC Controller Mode (IMS = 0, DIM2 = 1)

In this case serial port B has no fixed frame structure, but is used as a serial HDLC port. The valid HDLC data is marked by a strobe signal input via pin FSC. The data rate is determined by the clock input DCL (maximum 4096 Mbit/s). The characteristics of the serial port B are determined by bits DIM1, 0 as shown in **table 4**.

Table 4

HDLC Mode Characteristics

DIM1	DIM0	Characteristics
0	0	reserved
0	1	FSC strobe active low
1	0	FSC strobe active high
1	1	FSC strobe ignored

Interfaces

The ICC serves three different user-oriented interface types:

- parallel processor interface to higher layer functions
- IOM interface: between layer 1 and layer 2, and as a universal backplane for terminals
- SSI and SLD interfaces for B channel sources and destinations (in IOM-1 mode only).

µP Interface

The ICC is programmed via an 8-bit parallel microcontroller interface. Easy and fast microprocessor access is provided by 8-bit address decoding on chip. The interface consists of 13 (18) lines and is directly compatible with multiplexed and non-multiplexed microcontroller interfaces (Siemens/Intel or Motorola type buses). The microprocessor interface signals are summarized in **table 5**.

Table 5

µP Interface of the ICC

Pin No. P-DIP	Pin No. PL-CC	Symbol	Input (I) Output (O)	Function
21 22 23 24 1 2 3 4	25 26 27 28 1 2 3 4	AD0/D0 AD1/D1 AD2/D2 AD3/D3 AD4/D4 AD5/D5 AD6/D6 AD7/D7	I/O I/O I/O I/O I/O I/O I/O I/O	**Multiplexed Bus Mode:** Address/Data bus. Transfers addresses from the µP system to the ICC and data between the µP system and the ICC. Non-Multiplexed Bus Mode: Data bus. Transfers data between the µP system and the ICC.
17	21	$\overline{CS}$	I	**Chip Select.** A 0 ("low") on this line selects the ICC for a read/write operation.
–	23	R/$\overline{W}$	I	**Read/Write.** At 1 ("high"), identifies a valid µP access as a read operation. At 0, identifies a valid µP access as a write operation (Motorola bus mode).
19	23	$\overline{WR}$	I	Write. This signal indicates a write operation (Siemens/Intel bus mode).
–	24	$\overline{DS}$	I	**Data Strobe.** The rising edge marks the end of a valid read or write operation (Motorola bus mode).
20	24	$\overline{RD}$	I	Read. This signal indicates a read operation (Siemens/Intel bus mode).
15	18	$\overline{INT}$	OD	**Interrupt Request.** The signal is activated when the ICC requests an interrupt. It is an open drain output.
16	20	ALE	I	**Address Latch Enable.** A high on this line indicates an address on the external address bus (Multiplexed bus type only).
	19	A0	I	Address bit 0 (Non-multiplexed bus type).
	5	A1	I	Address bit 1 (Non-multiplexed bus type).
	6	A2	I	Address bit 2 (Non-multiplexed bus type).
	11	A3	I	Address bit 3 (Non-multiplexed bus type).
	12	A4	I	Address bit 4 (Non-multiplexed bus type).
	13	A5	I	Address bit 5 (Non-multiplexed bus type).

ISDN Oriented Modular (IOM-1) Interface

IOM-1

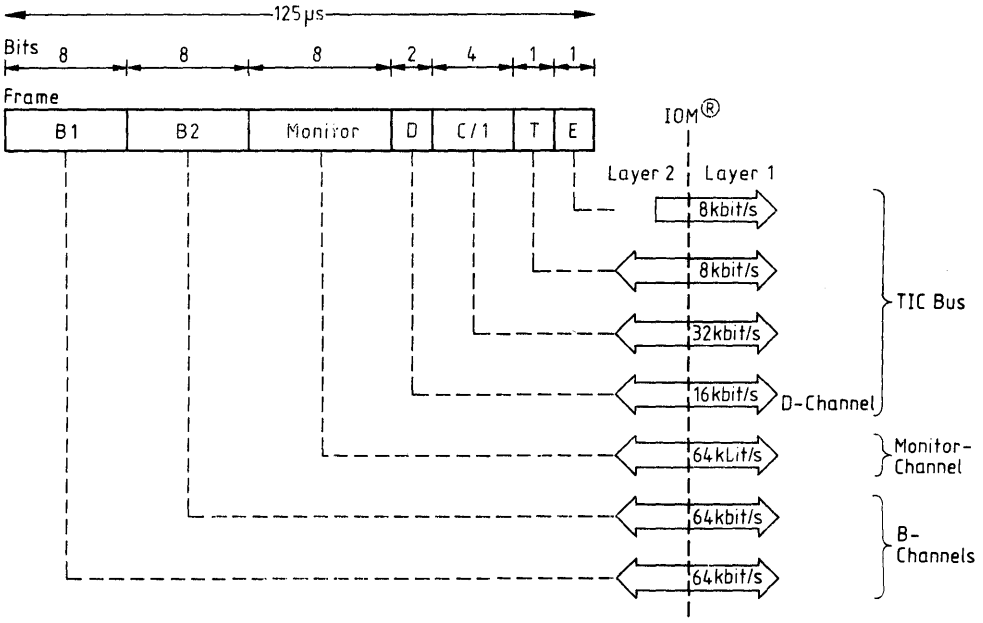
This interface consists of one data line per direction (IOM Data Ports 0 and 1: IDP0,1). Three additional signals define the data clock (DCL) and the frame synchronization (FSC/FSD) at this interface. The data clock has a frequency of 512 kHz (twice the data rate) and the frame sync clock has a repetition rate of 8 kHz.

Via this interface four octets are transmitted per 125 µs frame **(figure 8)**:

- The first two octets constitute the two 64 kbit/s B channels.
- The third octet is the monitor channel. It is used for the exchange of data using the IOM-1 monitor channel protocol which involves the E bit as a validation bit. In addition, it carries a bit which enables/inhibits the transmission of HDLC frames (IDP0) and it serves to arbitrate the access to the last octet (IDP1).
- The fourth octet is called the Telecom IC (TIC) bus because of the offered busing capability. It is constituted of the 16 kbit/s D channel (2 bits), a four-bit Command/ Indication channel and the T and E bits. The C/I channel serves to control and monitor layer-1 functions (e.g. activation/deactivation of a transmission line..). The T bit is a transparent 8 kbit/s channel which can be accessed from the ICC, and the E bit is used in monitor byte transfer.

Figure 8

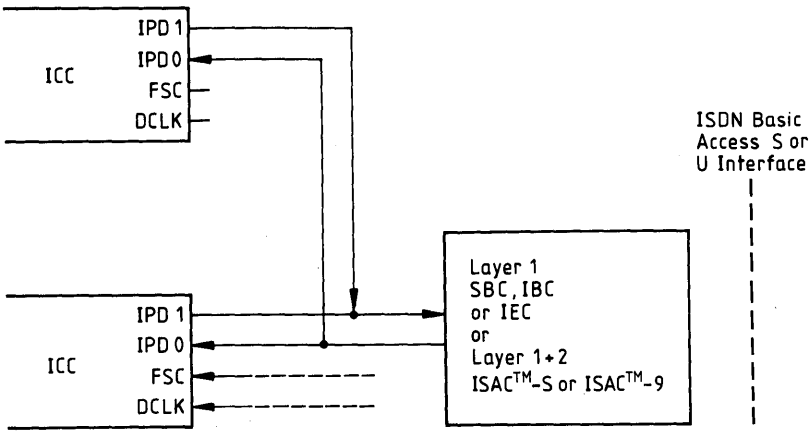
IOM®-1 Frame Structure



TIC Bus and Arbitration via Monitor Channel

The arbitration mechanism implemented in the monitor channel allows the access of more than one (up to eight) ICC to the last octet of IOM (TIC). This capability is useful for the modular implementation of different ISDN services (different service access points) e.g. in ISDN voice/data terminals. The IDP1 pins are connected together in a wired-or configuration, as shown in **figure 8.**

Figure 9
IOM Bus (TIC Bus) Configuration

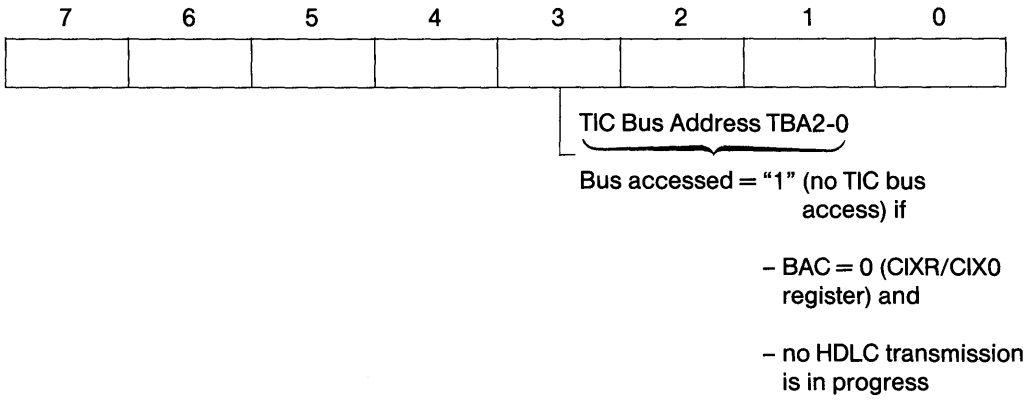


The arbitration mechanism is described in the following.

An access request to the TIC bus may either be generated by software (µP access to the C/I channel) or by the ICC itself (transmission of an HDLC frame). A software access request to the bus is effected by setting the BAC bit (CIXR/CIX0 register) to "1".

In the case of an access request, the ICC checks the bus accessed-bit (bit 3 of IDP1 monitor octet, **see figure 10)** for the status "bus free", which is indicated by a logical "1". If the bus is free, the ICC transmits its individual TIC bus address programmed in STCR register. The TIC bus is occupied by the device which is able to send its address error-free. If more than one device attempt to seize the bus simultaneously, the one with the lowest address value wins.

Figure 10
Monitor Channel Structure on IDP1



When the TIC bus is seized by the ICC, the bus is identified to other devices as occupied via the IDP1 monitor channel bus accessed bit state "0" until the access request is withdrawn. After a successful bus access, the ICC is automatically set into a lower priority class, that is, a new bus access cannot be performed until the status "bus free" is indicated in two successive frames.

If none of the devices connected to the IOM interface request access to the D and C/I channels, the TIC bus address 7 will be present. The device with this address will therefore have access, by default, to the D and C/I channels.

Note Bit BAC (CIXR/CIX0 register) should be reset by the µP when access to the C/I channel is no more requested, to grant other devices access to these channels.

Monitor channel

When the ICC is used in connection with an S interface layer-1 transceiver, an indication must be given to the ICC whether the D channel is available for transmission (TE applications with short passive or extended bus configuration).

This indication is assumed to be given in bit 3 "Stop/Go" (S/G) of the monitor input channel on IDP0 **(figure 11)**. When a HDLC frame is to be transmitted in the D channel, the ICC automatically starts, proceeds with, or stops frame transmission according to the S/G bit value:

Figure 11

Monitor Channel Structure on IDP0

S/G = 1: stop
S/G = 0: go

7	6	5	4	3	2	1	0
1	1	1	1	S/G	1	1	1

IOM-1 Timing

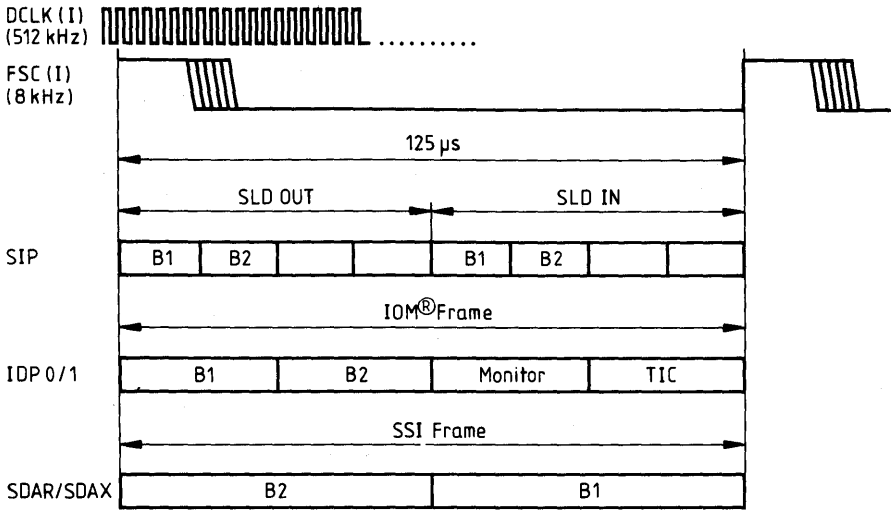
In IOM-1 mode, the ICC may be operated either in timing mode 0 or timing mode 1. The selections is via bit SPM in SPCR register.

Timing mode 0 **(SPM = 0)** is used in terminal applications. Timing mode 1 **(SPM = 1)** is only meaningful in exchange applications when the SLD is used. Programming timing mode 1 minimizes the B channel round-trip delay time on the SLD interface.

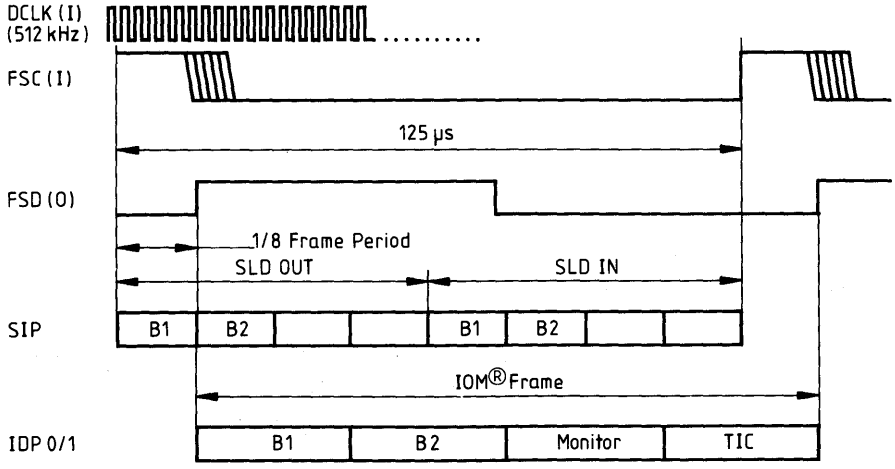
In timing mode 0 the IOM frame begin is marked by a rising edge on the FSC input. It simultaneously marks tthe beginning of the SLD frame **(figure 11)**.

In timing mode 1 the IOM frame begin is marked by a rising edge on FSD output. The FSD output is delayed by the ICC by 1/8 th of a frame with respect to FSC **(figure 12)**.

Figure 12
Interface Timing in IOM-1 Mode



(a) Timing Mode 0



(b) Timing Mode 1

IOM-2

The IOM-2 is a generalization and enhancement of the IOM-1. While the basic frame structure is very similar, IOM-2 offers further capacity for the transfer of maintenance information. In terminal applications, the IOM-2 constitutes a powerful backplane bus offering intercommunication and sophisticated control capabilities for peripheral modules.

The channel structure of the IOM-2 is depicted in **figure 13**:

Figure 13
Channel Structure of IOM-2

B1	B2	Monitor	D	C/I	MR	MX

- The first two octets constitute the two 64 kbit/s B channels.
- The third octet is the monitor channel. It is used for the exchange of data between the ICC and the other attached device(s) using the IOM-2 monitor channel protocol.
- The fourth octet (control channel) contains
  - two bits for the 16 kbit/s D channel
  - a four-bit command/indication channel
  - two bits MR and MX for supporting the monitor channel protocol.

In the case of an IOM-2 interface, the frame structure depends on whether TE- or non-TE is selected, via bit SPM in SPCR register.

Non-TE timing mode (SPM = 1)

In this case, the frame is a multiplex of eight IOM-2 channels **(figure 14)**, each channel has the structure in **figure 13**.

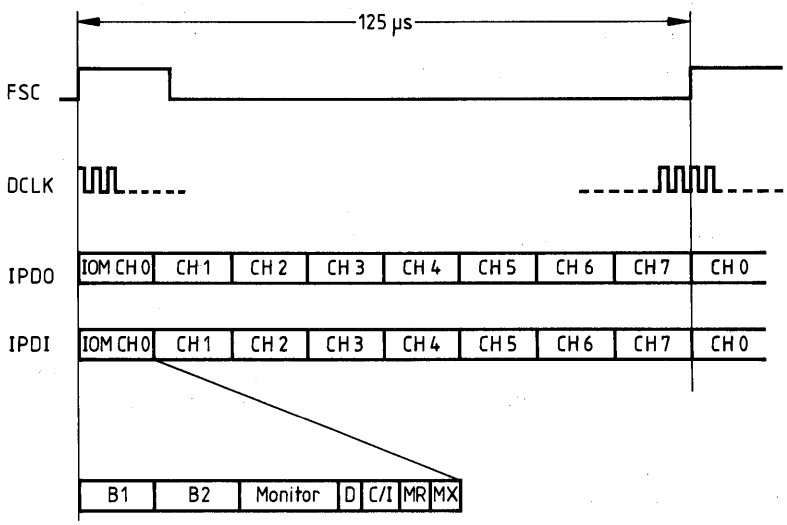
Thus the data rate per subscriber connection (corresponding to one channel) is 256 kbit/s, whereas the bit rate is 2048 kbit/s. The IOM-2 interface signals are:

IDP0,1: 2048 kbit/s

DCLK 4096 kHz-input

FSC: 8 kHz-input

Figure 14
Multiplexed Frame Structure of the IOM-2 Interface in Non-TE Timing Mode



The ICC is assigned to one of the eight channels (0 to 7) via register programming.
This mode is used in ISDN exchange/line card applications.

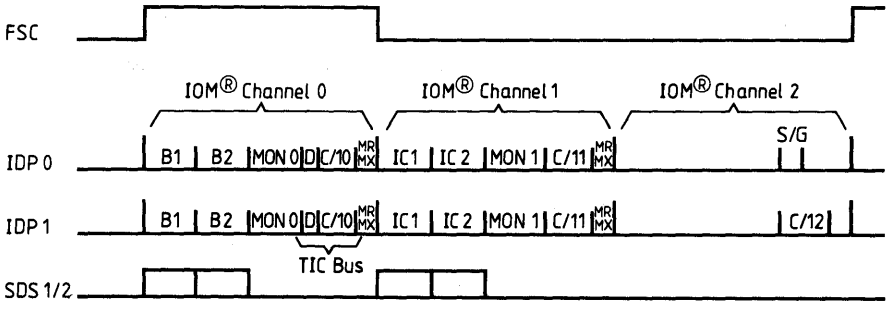
TE Timing Mode (SPM = 0)

The frame is composed of three channels **(figure 14)**:

- Channel 0 contains 144 kbit/s (for 2B + D) plus monitor and command/indication channels for layer-1 devices.
- Channel 1 contains two 64-kbit/s intercommunication channels plus monitor and command/indication channels for other IOM-2 devices.
- Channel 2 is used for enabling/inhibiting the transmission of HDLC frames. This bit is typically generated by an S-bus transceiver (stop/go: bit 5, or 3rd MSB of the last octet on IDP0). On IDP1, bits 2 to 5 of the last octet are used for TIC bus access arbitration.

As in the IOM-1 case **(figure 9)**, up to eight ICCs can access the TIC bus (D and C/I channels). The bus arbitration mechanism is identical to that described previously, except that it involves bits 2 to 5 in channel 2.

Figure 15
Definition of IOM-2 Channels in Terminal Timing Mode



The IOM-2 signals are:

IDP0,1: 768 kbit/s

DCLK: 1536-kHz input

FSC: 8-kHz input.

In addition, to support standard combos/data devices the following signals are generated as outputs:

SDS1/2: 8-kHz programmable data strobe signals for selecting one or both B/IC channel(s).

SSI (Serial Port A)

The SSI (Serial Synchronous Interface) is available in IOM-1 interface mode. Timing mode 0 (SPM = 0) has to be programmed.

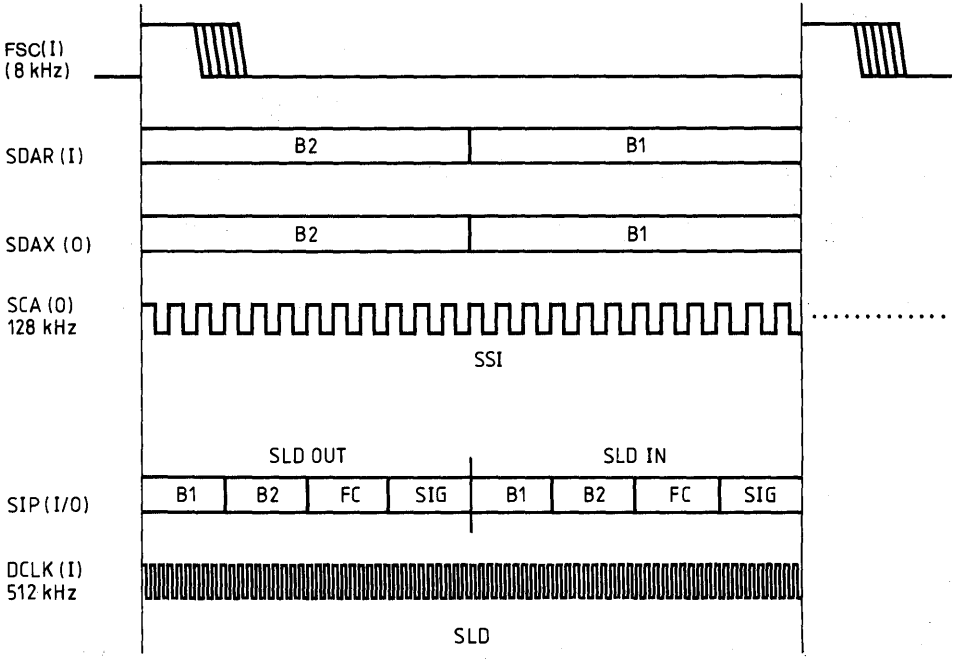
The serial port SSI has a data rate of 128 kbit/s. It offers a full duplex link for B channels in ISDN voice/data terminals. Examples: serial synchronous transceiver devices (USART's, HSCX SAB 82525, ITAC PSB 2110, ...), and CODEC filters.

The port consists of one data line in each direction (SDAX and SDAR) and the 128 kHz clock output (SCA). The beginning of B2 is marked by a rising edge on FSC, **see figure 15.**

The µC system has access to B-channel data via the ICC registers BCR1/2 and BCX1/2.

The µC access must be synchronized to the serial transmission by means of the Synchronous Transfer Interrupt (STCR).

Figure 16
SSI and SLD Interface Lines



SLD

The SLD is available in IOM-1 interface mode.

The standard SLD interface is a three-wire interface with a 512-kHz clock input (DCL), an 8-kHz frame direction signal input (FSC), and a serial ping-pong data lead (SIP) with an effective full duplex data rate of 256 kbit/s.

The frame is composed of four octets per direction. Octets 1 and 2 contain the two B channels, octet 3 is a feature control byte, and octet 4 is signaling byte **(figure 16)**.

The SLD interface can be used in:

– **Terminal applications** as a full duplex time-multiplexed (ping-pong) connection to B-channel sources/destinations.

  CODEC filters, such as the SICOFI (PEB 2060) or the ARCOFI (PSB 2160) as well as other SLD compatible voice/data modules may be connected directly to the ICC. Terminal specific functions have to be deselected (TSF = 0), so that pin SIP/EAW takes on its proper function as SLD data line. Moreover, in TE applications timing mode 0 has to be programmed.

– **Digital exchange applications** as a full duplex time-multiplexed connection to convey the B channels between the layer-1 devices and a Peripheral Board Controller (e.g. PBC PEB 2050 or PIC PEB 2052), which performs time-slot assignment on the PCM highways, forming a system interface to a switching network.

  Timing mode 1 (SPM = 1) can be programmed in order to minimize the B channel round-trip delay.

The µC system has access to B-channel data, the feature control byte and the signaling byte via the ICC registers:

– C1R,C2R → B1/B2
– CFCR and SFCX → FC
– SSCR and SSCX → SIG

The µP access to C1R,C2R,SFCR, SFCR,SSCR and SSCX must be synchronized to the serial transmission by means of the Synchronous Transfer Interrupt (STCR) and the BVS-bit (STAR).

Register Description

The parameterization of the ICC and the transfer of data and control information between the µP and ICC is performed through the R- and XFIFO and two register sets. The address map is shown in **table 6**.

The two FIFOs have an identical address range 00-1F$_H$.

The register set in the address range 20-2A pertains to the HDLC transceiver and LAPD controller. The register set ranging from 30 to 3B pertains to the control of layer-1 functions and of the IOM interface.

For a detailed register description please refer to the ICC Technical Manual.

Table 6
ICC Address Map and Register Summary

Address (hex)	Read		Write	
	Name	**Description**	**Name**	**Description**
00 . . 1F	RFIFO	Receive FIFO	XFIFO	Transmit FIFO
20	ISTA	Interrupt Status Register	MASK	Mask Register
21	STAR	Status Register	CMDR	Command Register
22	MODE	Mode Register		
23	TIMR	Timer Register		
24	EXIR	Extended Interrupt Register	XAD1	Transmit Address 1
25	RBCL	Receive Frame Byte Count Low	XAD2	Transmit Address 2
26	SAPR	Received SAPI	SAP1	Individual SAPI 1
27	RSTA	Receive Status Register	SAP2	Individual SAPI 2
28			TEI1	Individual TEI 1
29	RHCR	Receive HDLC Control	TEI2	Individual TEI 2
2A	RBCH	Receive Frame Byte Count High		
30	SPCR	Serial Port Control Register		
31	CIRR/ CIR0	Command/Indication Receive (0)	CIXR/ CIX0	Command/Indication Transmit (0)
31	MOR/ MOR0	Monitor Receive (0)	MOX/ MOX0	Monitor Transmit (0)
33	SSCR/ CIR1	SIP Signaling Code Receive/ Command/Indication Receive 1	SSCX/ CIX1	SIP Signaling Code Transmit/ Command/Indication Transmit 1
34	SFCR/ MOR1	SIP Feature Control Read/ Monitor Receive 1	SFCW/ MOX1	SIP Feature Control Write/ Monitor Transmit 1
35	C1R	Channel Register 1		
36	C2R	Channel Register 2		
37	B1CR	B1 Channel Register	STCR	Sync Transfer Control Register
38	B2CR	B2 Channel Register	ADF1	Additional Feature Register 1
39	ADF2	Additional Feature Register 2		
3A	MOSR	Monitor Status Register	MOCR	Monitor Control Register

Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Voltage on any pin with respect to ground	V_S	-0.4 to $V_{DD}+0.4$	V
Ambient temperature under bias	T_A	0 to 70	°C
Storage temperature	T_{stg}	-65 to 125	°C

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

$T_A = 0$ to 70 °C, $V_{DD} = 5$ V, $V_{SS} = 0$ V.

Parameter		Symbol	Limit Values min.	Limit Values max.	Unit	Test Conditions	
L-input voltage		V_{IL}	-0.4	0.8	V		
H-input voltage		V_{IH}	2.0	$V_{DD}+0.4$	V		
L-output voltage		V_{OL}		0.45	V	$I_{OL} = 7$ mA pin IDP0, IDP1 $I_{OL} = 2$ mA all other pins	
H-output voltage H-output voltage		V_{OH} V_{OH}	2.4 $V_{DD}-0.5$		V V	$I_{OH} = -400$ µA $I_{OH} = -100$ µA	
Power supply current	operational	I_{CC}		1.6 3.5 8.0	mA mA mA	DCLK: 512 kHz DCLK: 1536 kHz DCLK: 4096 kHz	$V_{DD} = 5$ V, inputs at 0 V/V_{DD} no output loads
	power down			0.6	mA		
Input leakage current Output leakage current		I_{LI} I_{LO}		10	µA	$0 \text{ V} < V_{IN} < V_{DD}$ to 0 V $0 \text{ V} < V_{OUT} < V_{DD}$ to 0 V	

Capacitances

$T_A = 25\,°C$, $V_{DD} = 5\,V \pm 5\%$, $V_{SS} = 0\,V$, $f_C = 1\,MHz$, unmeasured pins returned to GND.

Parameter	Symbol	Limit Values		Unit
		typ.	max.	
Input capacitance	C_{IN}	5	10	pF
Output capacitance $f_C = 1$ MHz	C_{OUT}	10	20	pF
I/O capacitance $f_C = 1$ MHz	C_{IO}	8	15	pF

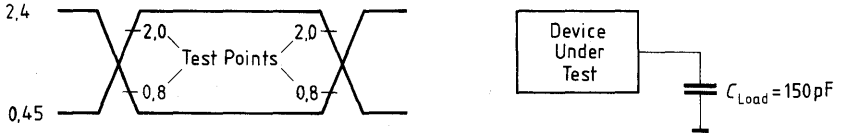
AC Characteristics

$T_A = 0$ to $70\,°C$, $V_{DD} = 5\,V \pm 5\%$

Inputs are driven to 2.4 V for a logical "1" anf to 0.4 V for a logical "0". Timing measurements are made at 2.0 V for a logical "1" and 0.8 V for a logical "0". The AC testing input/output waveforms are shown below.

Figure 17

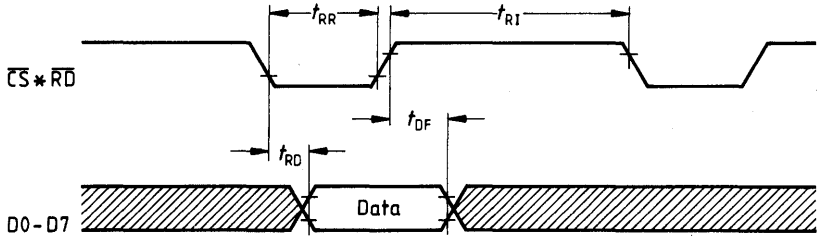
Input/Output Waveform and Load Circuit for AC Tests



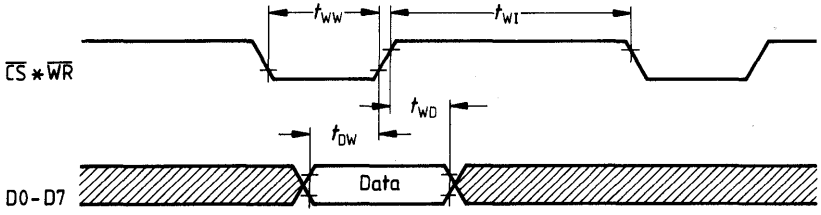
Microprocessor Interface Timing

Siemens/Intel Bus Mode

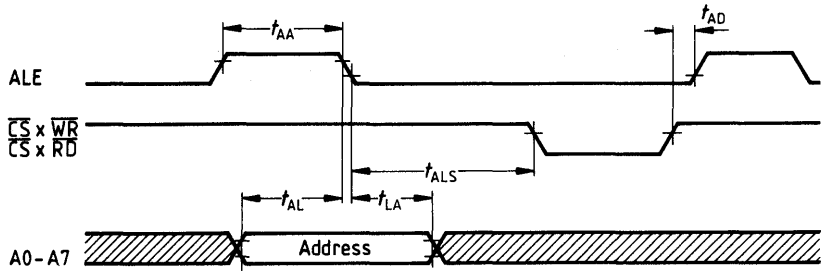
µP Read Cycle



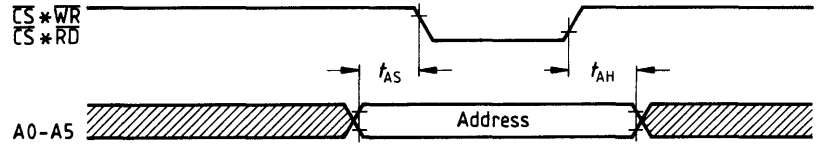
µP Write Cycle



Multiplexed Address Timing

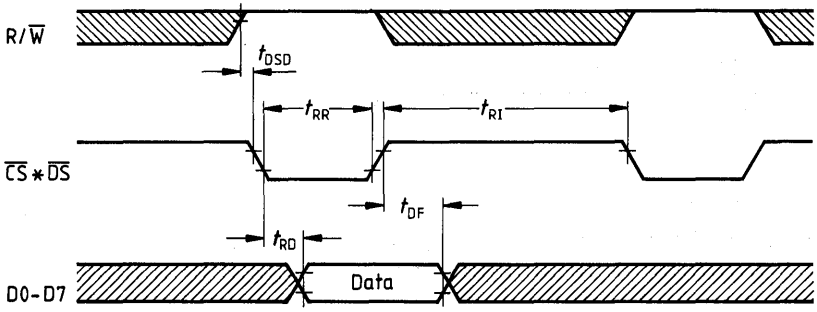


Non-Multiplexed Address Timing

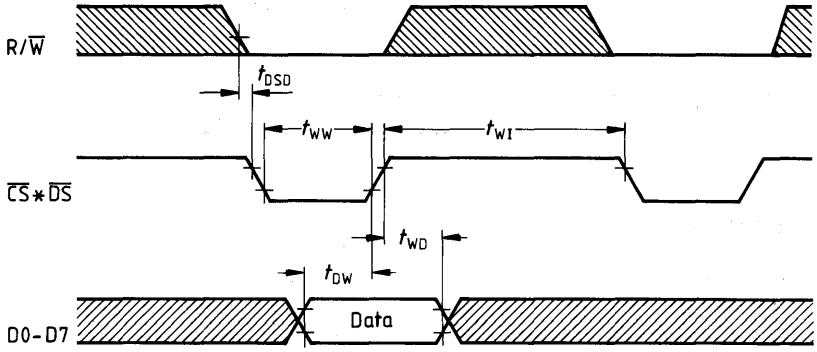


Motorola Bus Mode

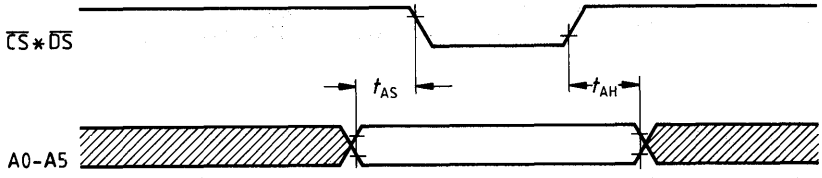
µP Read Cycle



µP Write Cycle



Address Timing



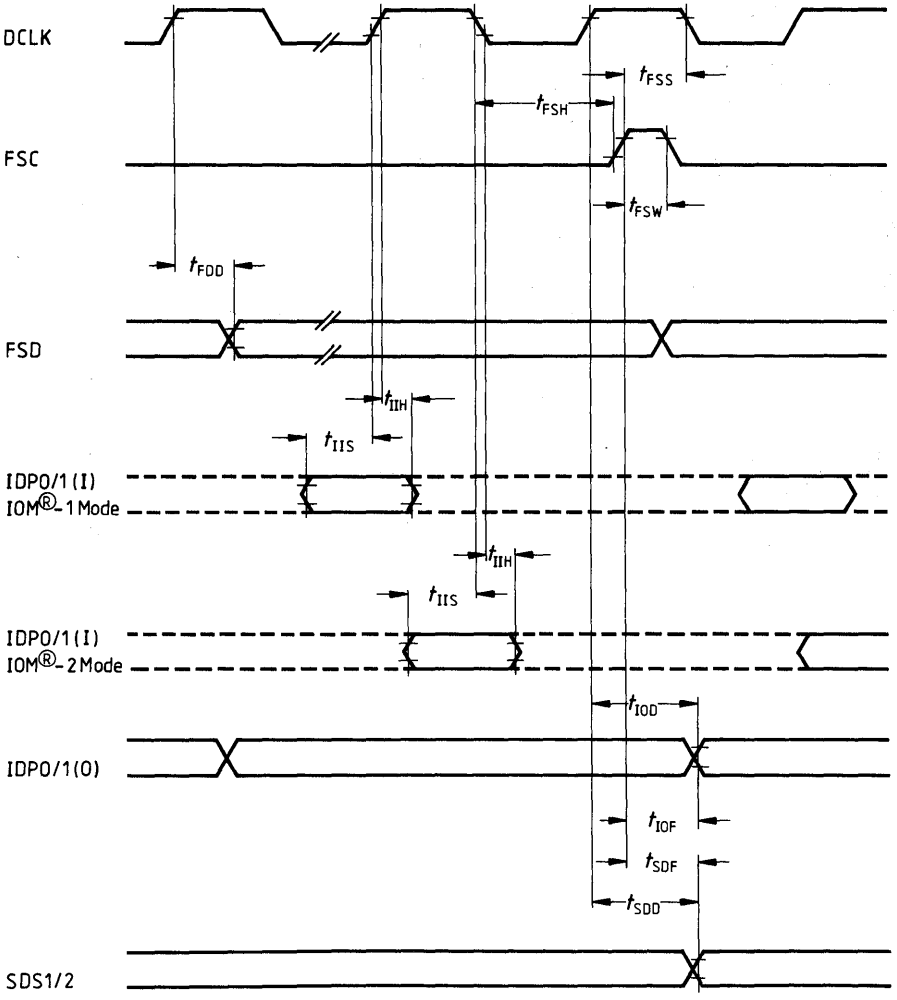
Parameters and Values of the Bus Modes

Parameter	Symbol	Limit Values		Unit
		min.	max.	
ALE pulse width	t_{AA}	50		ns
Address setup time to ALE	t_{AL}	20		ns
Address hold time from ALE	t_{LA}	10		ns
Address latch setup time to $\overline{WR}$, $\overline{RD}$	t_{ALS}	0		ns
Address setup time to $\overline{WR}$, $\overline{RD}$	t_{AS}	10		ns
Address hold time from $\overline{WR}$, $\overline{RD}$	t_{AH}	20		ns
ALE pulse delay	t_{AD}	15		ns
DS delay after R/$\overline{W}$ setup	t_{DSD}	0		ns
$\overline{RD}$ pulse width	t_{RR}	110		ns
Data output delay from $\overline{RD}$	t_{RD}		110	ns
Data float from $\overline{RD}$	t_{DF}		25	ns
$\overline{RD}$ control interval	t_{RI}	70		ns
$\overline{WR}$ pulse width	t_{WW}	60		ns
Data setup time to $\overline{WR}$* $\overline{CS}$	t_{DW}	35		ns
Data hold time from $\overline{WR}$* $\overline{CS}$	t_{WD}	10		ns
$\overline{WR}$ control interval	t_{WI}	70		ns

Serial Interface Timing

IOM Mode

IOM Timing



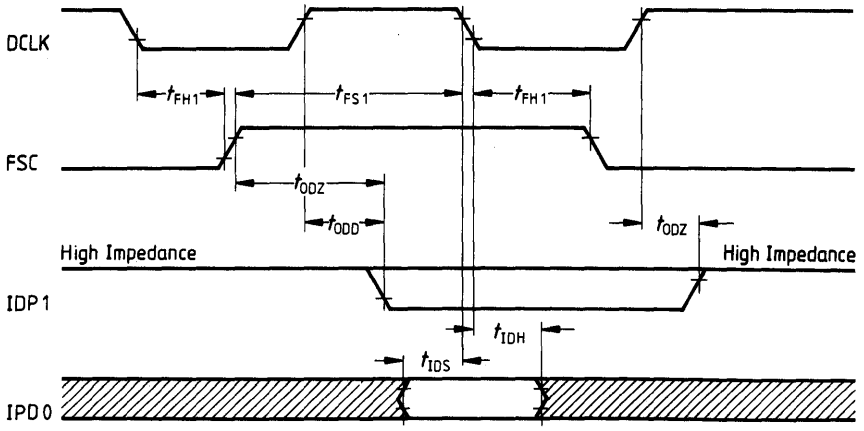
Parameters and Values of IOM Mode

Parameter	Symbol	Limit Values		Unit	Test Conditions
		min.	max.		
IOM output data delay	t_{IOD}	20 20	140 100	ns ns	IOM-1 IOM-2
IOM input data setup	t_{IIS}	40 20		ns ns	IOM-1 IOM-2
IOM input data hold	t_{IIH}	20		ns	
IOM output from FSC	t_{IOF}		80	ns	See note
Strobe signal delay	t_{SDD}		120	ns	
Strobe delay from FSC	t_{SDF}		120	ns	See note
Frame sync setup	t_{FSS}	50		ns	
Frame sync hold	t_{FSH}	30		ns	
Frane sync width	t_{FSW}	40		ns	
FSD delay	t_{FDD}	20	140	ns	

Note: This delay is applicable in two cases only:
1) When FSC appears for the first time, e.g. at system power-up
2) When FSC appears before the excepted start of a frame

HDLC Mode

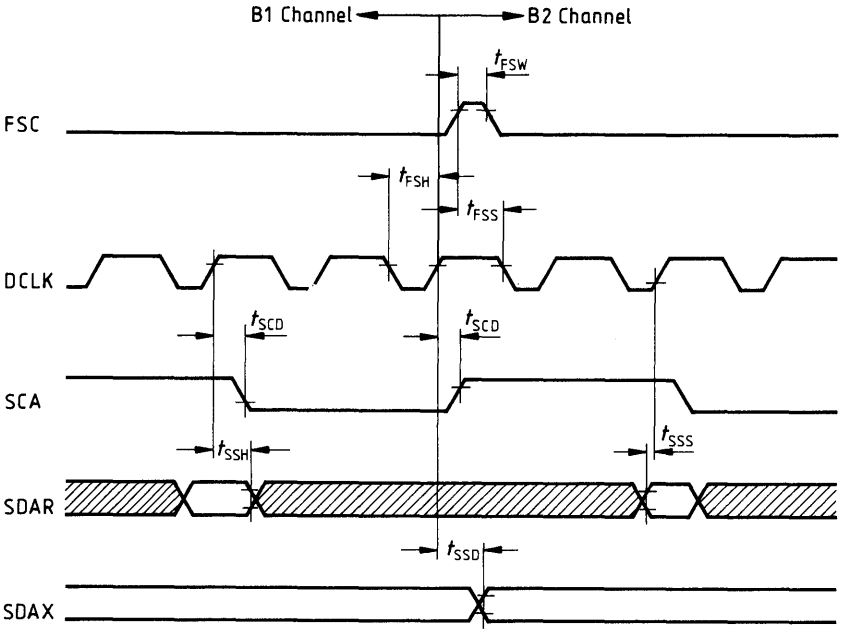
FSC (Strobe) Characteristics



Parameter	Symbol	Limit Values		Unit
		min.	max.	
FSC set-up time	t_{FS1}	100		ns
FSC hold time	t_{FH1}	30		ns
Output data from high impedance to active	t_{OZD}		80	ns
Output data from active to high impedance	t_{ODZ}		40	ns
Output data delay from DCL	t_{ODD}	20	100	ns
Input data setup	t_{IDS}	10		ns
Input data hold	t_{IDH}	30		ns

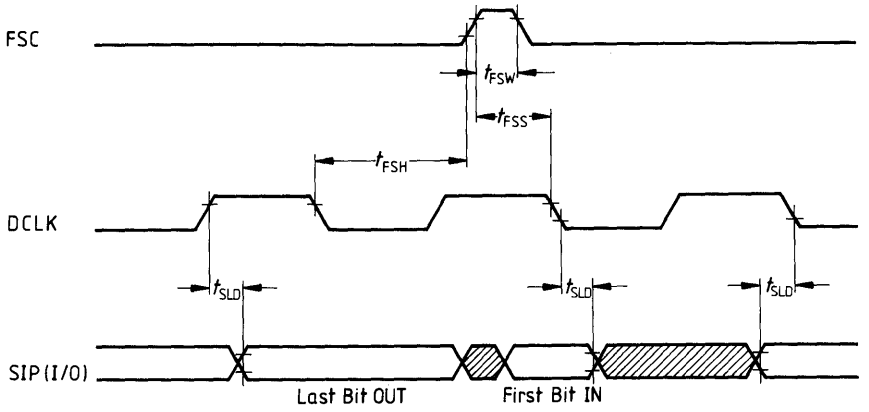
Serial Port A (SSI) Timing

SSI Timing



Parameter	Symbol	Limit Values		Unit
		min.	max.	
SCA clock delay	t_{SCD}	20	140	ns
SSI data delay	t_{SSD}	20	140	ns
SSI data setup	t_{SSS}	40		ns
SSi data holf	t_{SSH}	20		ns
Frame sync hold	t_{FSH}	30		ns
Frame sync width	t_{FSW}	40		ns

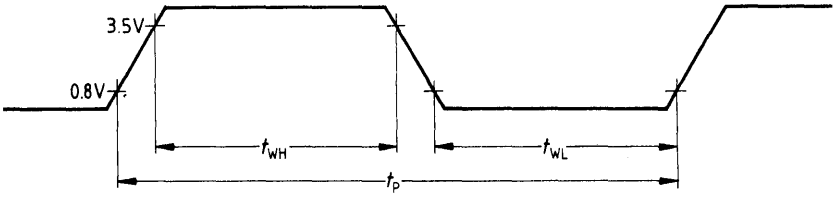
SLD Timing



Parameter	Symbol	Limit Values		Unit
		min.	max.	
SLD data delay	t_{SLD}	20	140	ns
SLD data setup	t_{SLS}	30		ns
SLD data hold	t_{SLH}	30		ns
Frame sync setup	t_{FSS}	50		ns
Frame sync hold	t_{FSH}	30		ns
Frame sync width	t_{FSW}	40		ns

Clock Time

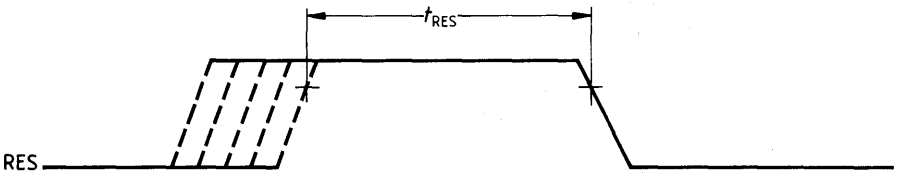
Definition of Clock Period and Width



Parameter	Symbol	Limit Values		Unit	Test Conditions
		min.	max.		
Clock period	t_P	1000		ns	IOM-1
Clock width high	t_{WH}	200		ns	IOM-1
Clock width low	t_{WL}	200		ns	IOM-1
Clock period	t_P	240		ns	IOM-2
Coock width high	t_{WH}	100		ns	IOM-2
Clock width low	t_{WL}	100		ns	IOM-2

Reset

Reset Signal Characteristics



Parameter	Symbol	Limit Values	Test Conditions
		min.	
Length of active high state	t_{RES}	2*DCL clock cycles	During power up

SIEMENS

ISDN D-Channel Exchange Controller (IDEC) PEB 2075

Preliminary Data **ACMOS IC**

Type	Ordering code	Package
PEB 2075-P	Q67100-H8682	P-DIP-28
PEB 2075-N	Q67100-H8683	PL-CC-44 (SMD)

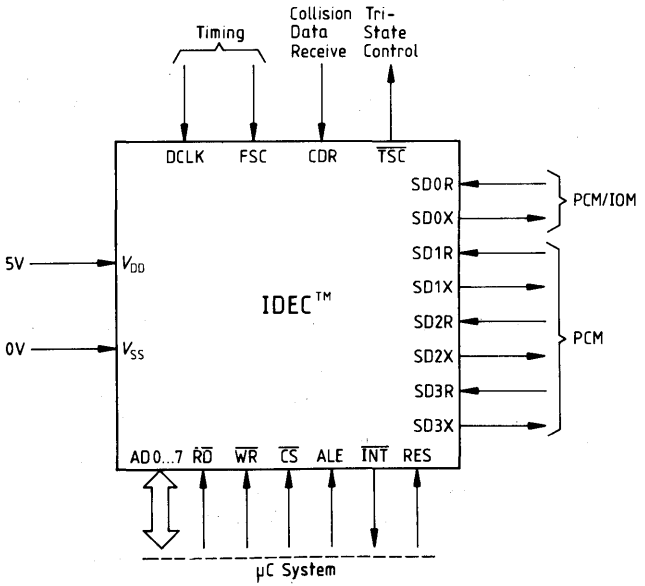
The ISDN Digital Exchange Controller PEB 2075 (IDEC™) is a serial HDLC data communication circuit with four independent channels. Its telecommunication specific features make it especially suited for use in variable data rate PCM systems. In addition, the device contains spohisticated switching functions and it implements automatic contention resolution between packet data from different sources.

Its applications include: communication multiplexers, peripheral ISDN line cards, packet handlers, X.25 packet switching devices. The IDEC is a fundamental building block for networks with either centralized, de-centralized or mixed signaling/ packet data handling architectures.

Features

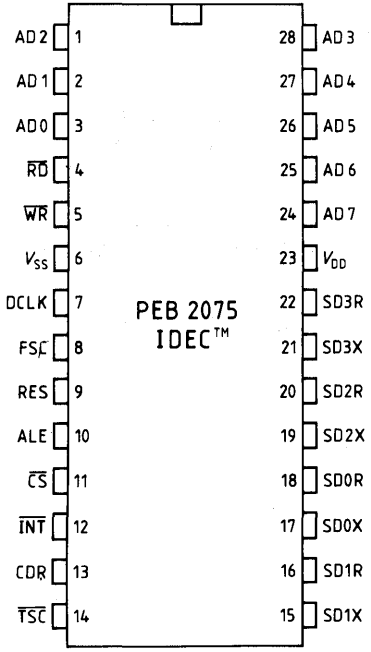
- Four independent HDLC channels
- 64 byte FIFO storage per channel and direction
- Handling of basic HDLC functions
  Flag detection/generation
  Zero deletion/insertion
  CRC checking/generation
  Check for abort
- Single connection and quad connection modes
- IOM® interface or PCM interface
- Programmable time slots and channel data rates (up to 4 Mbit/s)
- Different methods of contention resolution
- 8-bit parallel microcontroller interface with vectored interrupt
- Advanced CMOS technology
- Power consumption less than 50 mW.

Logic Symbol



Pin Configuration

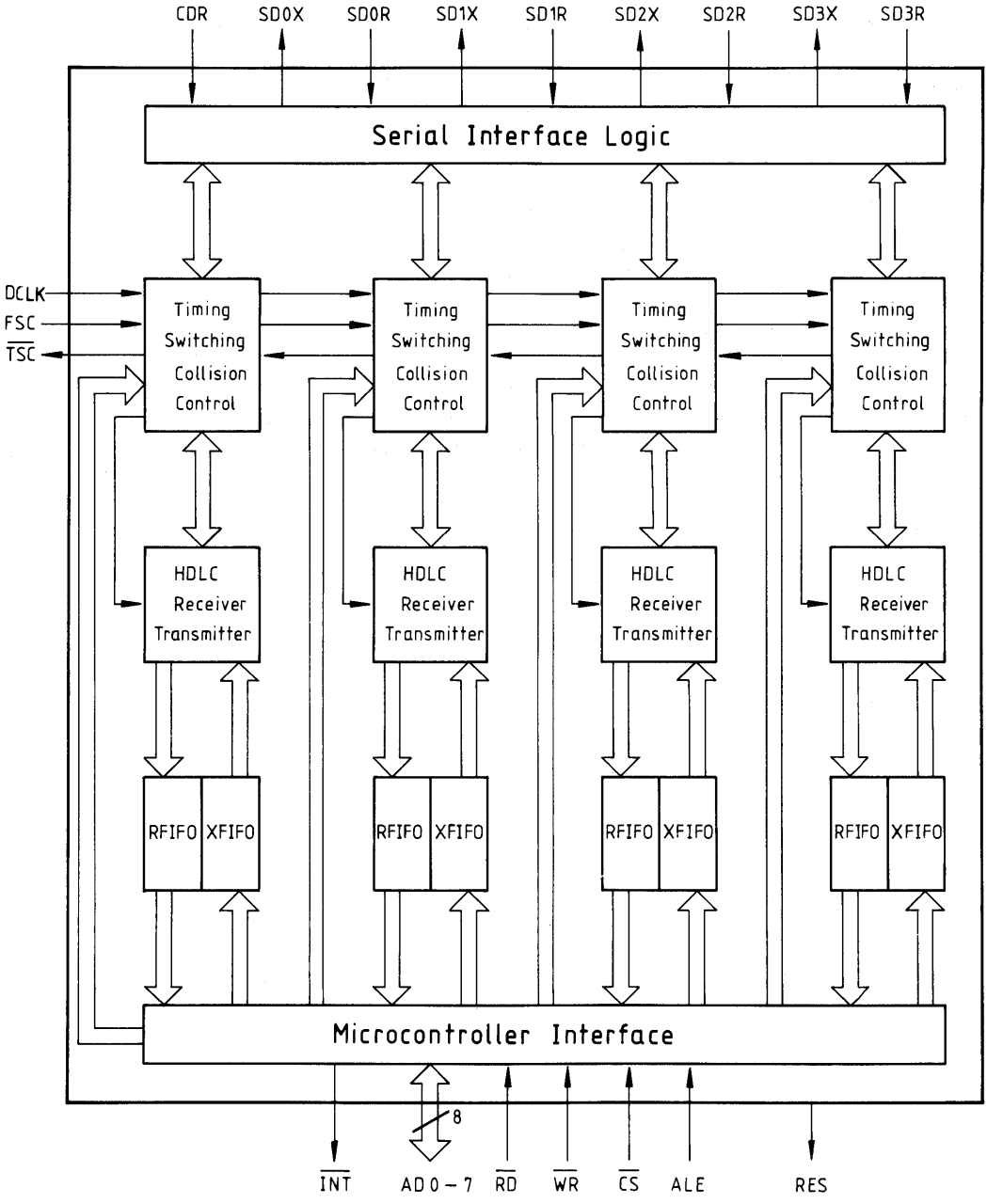
(top view)



Pin Definitions and Functions

Pin No.	Symbol	Input (I) Output (O)	Functions
3 2 1 28 27 26 25 24	AD 0 AD 1 AD 2 AD 3 AD 4 AD 5 AD 6 AD 7	I/O I/O I/O I/O I/O I/O I/O I/O	**Address-Data Bus.** The multiplexed address-data bus transfers data and commands between the µP system and the IDEC.
11	$\overline{CS}$	I	**Chip Select.** A low on this line selects the IDEC for a read/write operation.
5	$\overline{WR}$	I	**Write.** A low on this line indicates a write operation.
4	$\overline{RD}$	I	**Read.** A low on this line indicates a read operation.
12	$\overline{INT}$	OD	**Interrupt Request.** This line is activated when the IDEC requests an interrupt. It is an open drain output.
10	ALE	I	**Address Latch Enable.** A high on this line indicates an address on the external address-data bus, selecting one of the internal sources or destinations.
18 16 20 22	SD0R SD1R SD2R SD3R	I	Serial Data Receive
17 15 19 21	SD0X SD1X SD2X SD3X	O	Serial Data transmit Serial Data transmit Serial Data transmit Serial Data transmit Serial Data transmit Serial Data transmit Collision output
7	DCLK	I	**Data Clock;** supplies a clock signal either equal to or twice the data rate.
8	FSC	I	Frame Synchronization or data strobe signal
14	$\overline{TSC}$	O	**Time-Slot Control.** Supplies a control signal for an external driver.
13	CDR	I	**Collision Data Receive.**
9	RES	I	Reset
6	V_{SS}	I	Ground
23	V_{DD}	I	Supply voltage +5 V

Figure 1
Block Diagram



1. System Integration

Communication Multiplexers

The four independent serial HDLC communication channels implemented in the IDEC make the circuit suitable for use in communication multiplexers.

The collision detection/resolution capability of the circuit allows statistical multiplexing of packets in one or several physical data communication channels, for example in DMI (mode 3) applications.

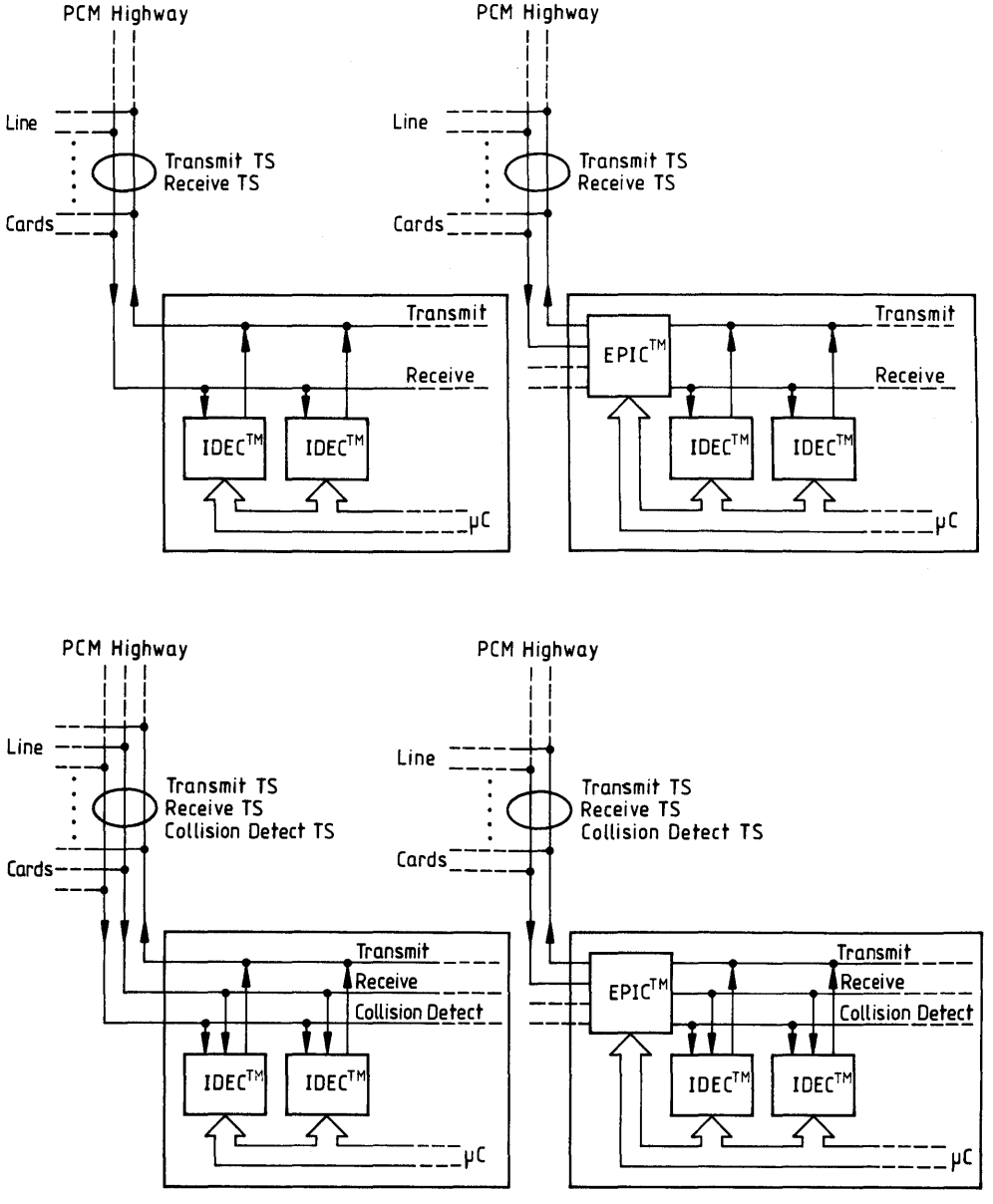
Centralized Signaling Data Packet Handlers

The IDEC can be used in central packet handlers of ISDN networks to process signaling or packet data of four ISDN subscribers. In this application, it may be used with or without the Extended PCM Interface Controller (EPIC) PEB 2055.

The IDEC can be connected to the IOM interface of the EPIC, which is itself connected to the PCM system highway. The EPIC implements concentration and time-slot assignment functions. As an alternative, the IDEC may be directly connected to PCM highways **(figure 2)**.

The size (from 1 to 8 bits) and the position of the time slot associated with each HDLC controller are software programmable. In addition to the receive and transmit data highways, the IDEC accepts a third input connection for collision detection purposes. The mode of collision detection is programmable. A "collision highway" (or time slot) can be used for remote collision control, as a "clear to send" lead, or for local contention resolution among several IDECs.

Figure 2
Use of IDEC in Central Signaling Data Packet Handlers



Line Cards De-Centralized or Mixed Signaling/Data Packet Handling Architectures

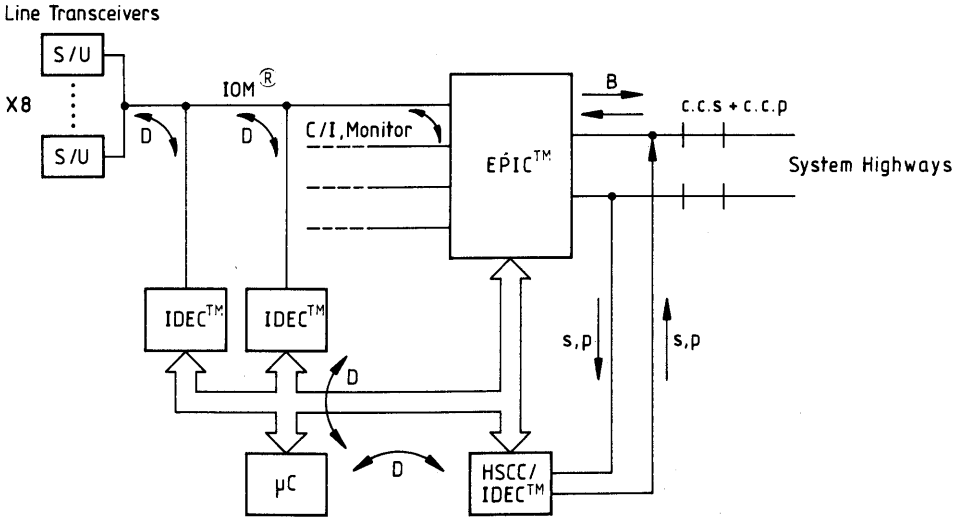
The IDEC can be used on peripheral line cards to process D-channel packets for ISDN subscribers. An Extended PCM Interface Controller PEB 2055 has the layer 1 controlling capacity and a B and D channel switching capacity for a total of 32 subscribers. The B and D channels and the control information for eight subscribers are carried over one IOM interface. Thus a line card dimensioned for 32 ISDN subscribers may employ up to eight IDECs, two for each IOM connection **(figure 3)**. A High Level Serial Communication Controller (HSCC) SAB 82520 with two HDLC channels, or another IDEC may be used to transmit and receive signaling over the system highway in a common channel. Again, such a common channel may be shared among several line cards, due to the statistical multiplexing capability of these controllers.

In completely de-centralized D-channel processing architectures, the processing capacity of a line card is usually dimensioned to avoid blocking situations even under maximum conceivable D-channel traffic conditions. It may sometimes be more advantageous to perform p-packet handling in a centralized manner while keeping s-packet handling on the line cards. A statistical increase in p-packet traffic has then no effect on the line card, and can be easily dealt with by one of the modular architectures for a central packet handler shown in the previous section. A more effective sharing of the total p-packet handling capacity is the result, especially in a situation where p-packet traffic patterns vary widely from one subscriber group to another.

The use of IDEC in the mixed D-channel processing architecture is illustrated in **figure 4)**.

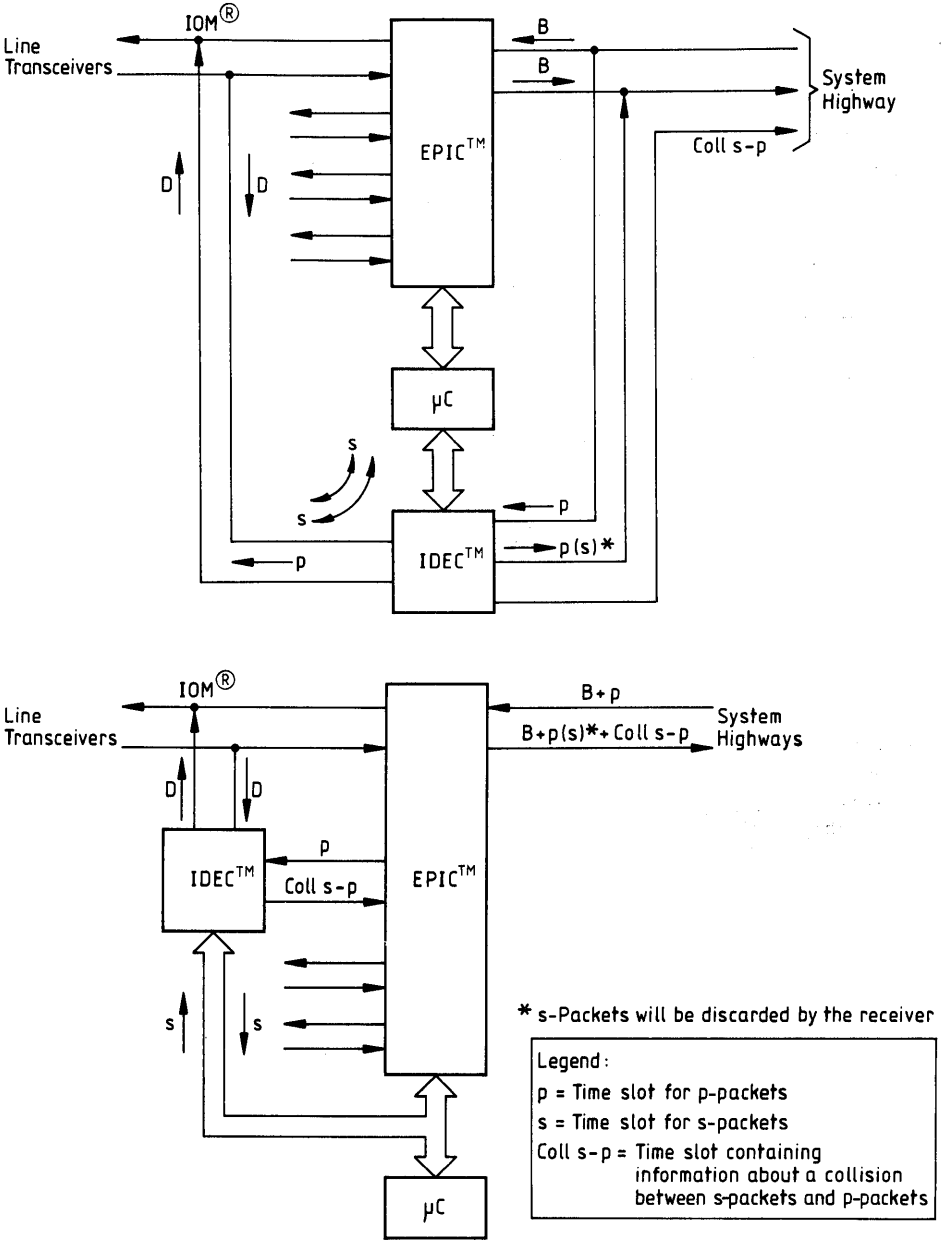
The additional "transparent data" connections supported by the IDEC enable a merging of p- and s-packets into one D-channel. Possible collision situations are dealt with by the IDEC which uses either the additional collision detect line **(figure 4a)** or a time slot on the system highway **(figure 4b)** from the line card to the central packet handler.

Figure 3
Line Card in a De-Centralized D-Channel Handling Architecture



Legend:
c.c.s/p = Common channel for signaling and for packed data, respectively
C/I,Mon = Control/Indication and Monitor channels of the IOM interface

Figure 4a; 4b
IDEC on a Line Card in a Mixed D-Channel Processing Architecture



2. Functional Description

General Functions and Device Architecture

The IDEC is an HDLC controller which handles four HDLC communication channels, each channel fully independent and programmable by its own register set. The circuit performs the following functions:

- Extraction (reception) and insertion (transmission) of the HDLC data packets in a time division multiplex bit stream.
- Implementation of the basic HDLC functions of the layer-2 protocol.
- Interfacing of the data packets to the microprocessor bus. For the temporary storage of data packets overlapping FIFO structures are used per channel and direction.
- Switching of data between serial interfaces.
- Implementation of different types of collision resolution.
- Test functions.

Operating Modes

Each HDLC controller of the IDEC is assigned to one time channel governed either by time slot assignment or by an external strobe signal.

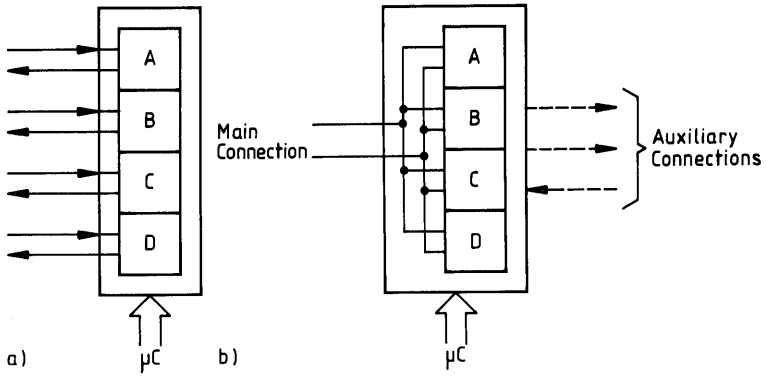
Two basic configurations are distinguished **(figure 5):**

- In the quad connection configuration the four HDLC controllers (A-D) are connected to individual time multiplexed communication lines;
- In the single connection configuration the four HDLC channels are all connected to one time multiplexed communication line.

Figure 5

(a) Quad Connection and

(b) Single Connection Configuration.



In the quad connection configuration two modes are distinguished as follows:

- Each connection is a time slotted highway, the lengths and positions of the time slot are programmable (quad connection time-slot mode);
- Each connection is a communication line, the time channels are marked by an external strobe signal (quad connection common control mode).

Two modes are distinguished in turn for the single connection configuration as follows:

- The connection is a standard IOM interface with predefined channel positions (single connection IOM mode);
- The connection is a time slotted highway (single connection time-slot mode).

For simplicity, a time slotted highway will sometimes be referred to as a "PCM highway", or PCM for short.

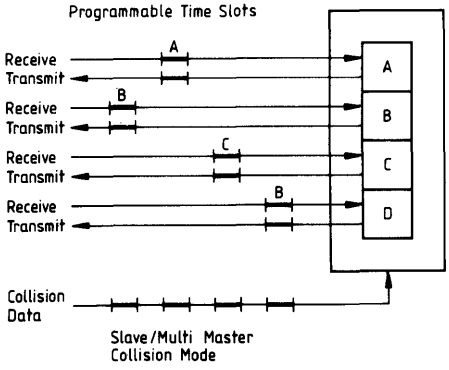
Table 1
Four Basic Operating Modes of the IDEC

MDS1	MDS0	Mode Description
0	0	Single connection time-slot mode
0	1	Quad connection common control mode
1	0	Single connection IOM mode
1	1	Quad connection time-slot mode

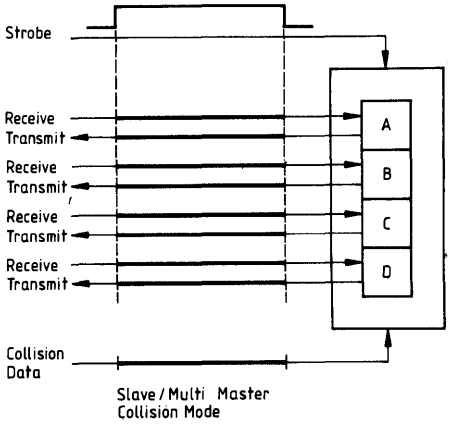
The four modes of operation are illustrated in **figure 6**. Via channel-by-channel programming, one of a number of collision detection modes may be selected in each of the basic modes of operation. For future reference, they are also depicted in **figure 6**.

Figure 6
Operating modes of the IDEC

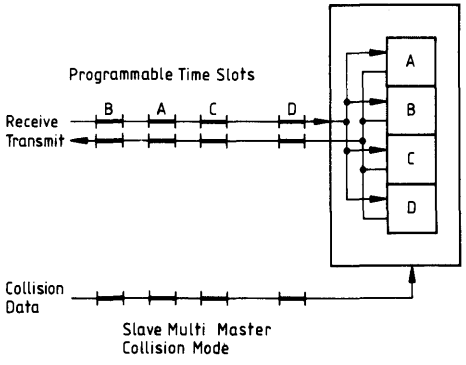
a. Quad Connection TS Mode



b. Quad Connection Common Control Mode



c. Single Connection TS Mode



d. Single Connection IOM Mode

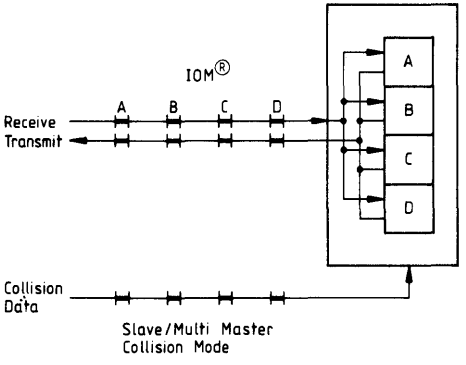
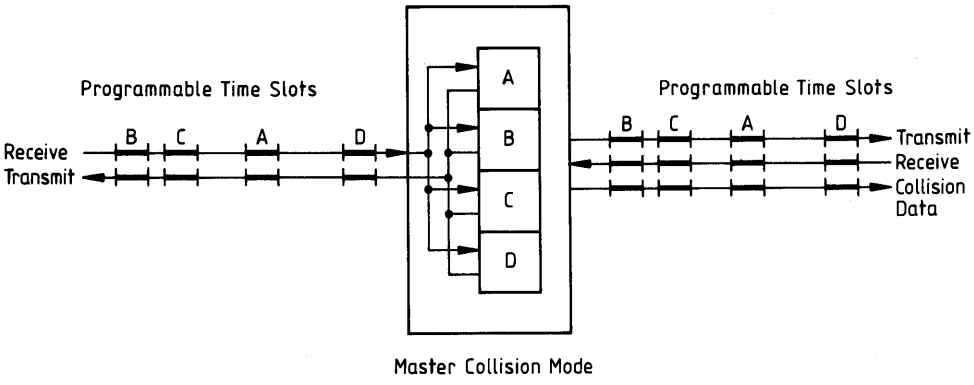


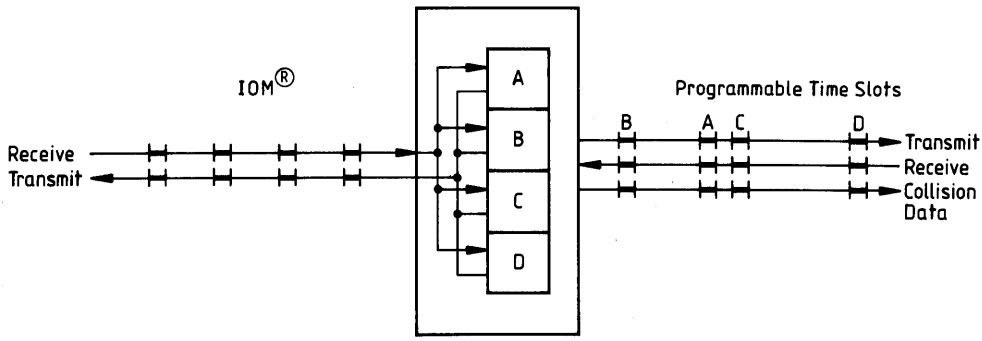
Figure 6 (continued overleat)

e. Single Connection TS Mode



Master Collision Mode

f. Single Connection IOM Mode



Master Collision Mode

Interfaces

Microcontroller Interface

The IDEC is programmable over an 8-bit parallel microcontroller interface. Easy and fast microprocessor access is provided by 8-bit address decoding on chip. The interface consists of 13 lines and is directly compatible with processors of the multiplexed address/ data bus type.

Table 2
Microcontroller Interface Signals of the IDEC

Symbol	Type	Name and Functions
AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7	I/O I/O I/O I/O I/O I/O I/O I/O	**Address-Data bus.** The multiplexed address/data bus transfers data and commands between the µC system and the IDEC.
$\overline{CS}$	I	**Chip Select.** A low on this signal selects the IDEC for a read/write operation.
$\overline{WR}$	I	**Write.** This signal indicates a write operation.
$\overline{RD}$	I	**Read.** This signal indicates a read operation.
$\overline{INT}$	OD	**Interrupt Request.** The signal is activated when the IDEC requests an interrupt. It is an open drain output.
ALE	I	**Address Latch Enable.** A high on this line indicates an address on the external address/data bus.

In addition to 8-bit processors, the IDEC supports a direct connection to 16-bit processors. Thus, through an internal address transformation, it is possible to access all IDEC registers using either even microprocessor addresses only or odd microprocessor only.

Note: The IDEC is now also available in a PL-CC-44 package with a demultiplexed address-data bus. For more information, see the latest IDEC Technical Manual.

Serial Interface

Depending on the selected mode, the IDEC supports four physically separate, full duplex serial interfaces, or one full duplex interface.

In addition to the data input and data output lines, the serial interface requires a common data clock (input DCLK) and a frame synchronization signal (input FSC). Input data is latched on the falling edge of DCLK and output data is clocked off on the rising edge of DCLK. The IDEC may be programmed so that the data clock rate is either equal to data rate, or twice the data rate.

Register Description

Register Address Layout

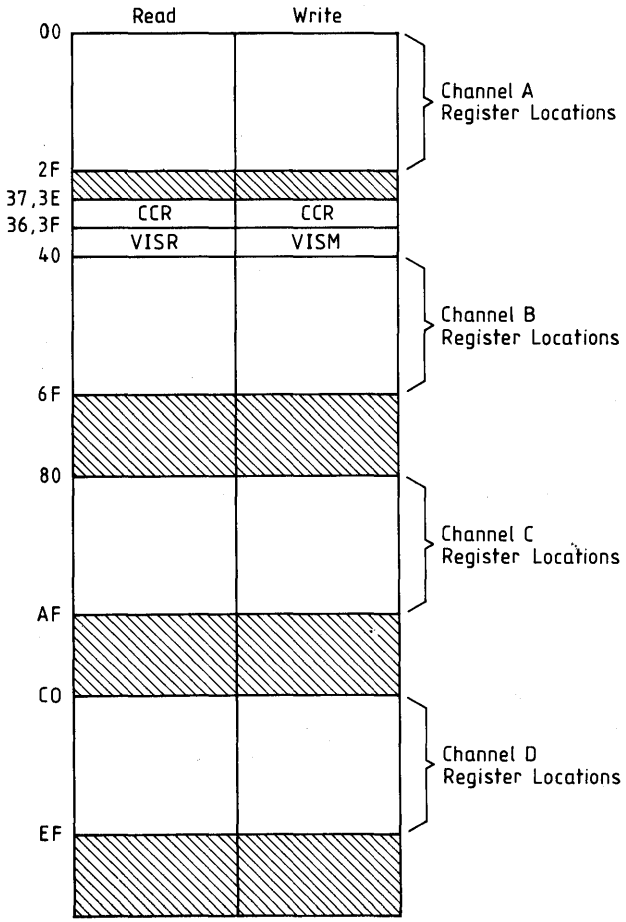
The register set consists of:

- one configuration register common to all four channels (CCR)
- a maskable vectored interrupt status register (VISR, VISM)

and, for each of the four channels, a set of individual registers **(figure 7)**.

In order to support the use of a 16-bit microcontroller, each register can be accessed with an even and an odd address value.

Figure 7
IDEC Register Map



The address map of the individual registers of each channel is shown in **table 2.** In order to obtain the actual address of a register, a "base" has to be added to the address given in the table, as follows:

Base = 00 for channel A
40 for channel B
80 for channel C
C0 for channel D.

Table 2

Address			Read	Write
Even		Odd		
00	to	1F	RFIFO	XFIFO
20		29	ISTA	ISM
28		21	STAR	CMDR
22		2B	MODE	MODE
2C		25	RFBC	TSR

For a detailed register description, see the IDEC data sheet.

Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Ambient temperature under bias	T_A	0 to 70	°C
Storage temperature	T_{stg}	−65 to 125	°C
Voltage on any pin with respect to ground	V_S	−0.4 to V_{DD} +0.4	V

DC Characteristics

$T_A = 0$ to 70 °C; $V_{DD} = 5\ V \pm 5\%$, $V_{SS} = 0\ V$

Parameter		Symbol	Limit Values min.	Limit Values max.	Unit	Test Conditions
L-input voltage		V_{IL}	−0.4	0.8	V	
H-input voltage		V_{IH}	2.0	V_{CC}+0.4	V	
L-output voltage		V_{OL}		0.45	V	$I_{OL} = 2$ mA
H-output voltage H-output voltage		V_{OH} V_{OH}	2.4 V_{DD}−0.5		V V	$I_{OH} = -400$ µA $I_{OH} = -100$ µA
Power supply current	operational	I_{CC}			mA	$V_{DD} = 5$ V, input at 0 V/V_{DD}, no output loads
	power down				mA	
Input leakage current Output leakage current		I_{LI} I_{LO}		+10 µA		0 V < V_{IN} < V_{DD} to 0 V 0 V < V_{OUT} < V_{DD} to 0 V

Capacitances

$T_A = 25$ °C, $V_{DD} = 5\ V \pm 5\%$, $V_{SS} = 0\ V$

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit	Test Conditions
Input capacitance	C_{IN}		7	pF	
I/O	C_{IO}		7	pF	

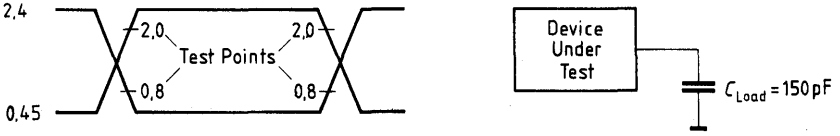
AC Characteristics

$T_A = 0$ to 70 °C, $V_{DD} = 5\ V \pm 5\%$

Inputs are driven to 2.4 V for a logical "1" and to 0.4 V for a logical "0". Timing measurements are made at 2.0 V for a logical "1" and at 0.8 V for a logical "0".

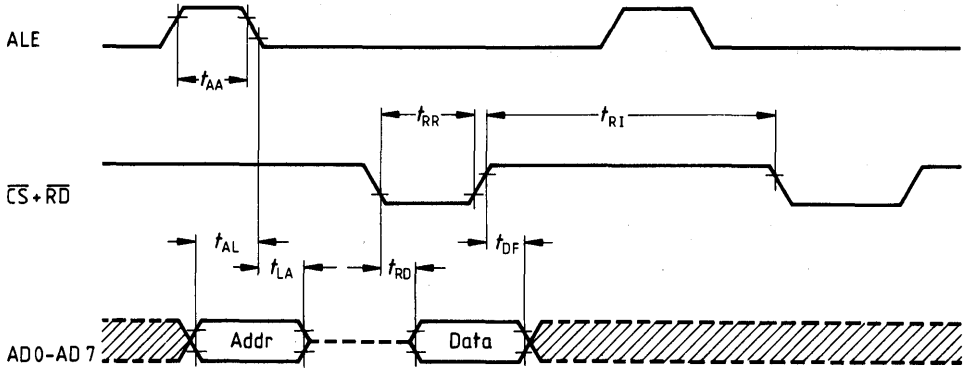
The AC testing input/output waveforms are shown below.

Figure 8
Input/Output Waveform for AC Tests

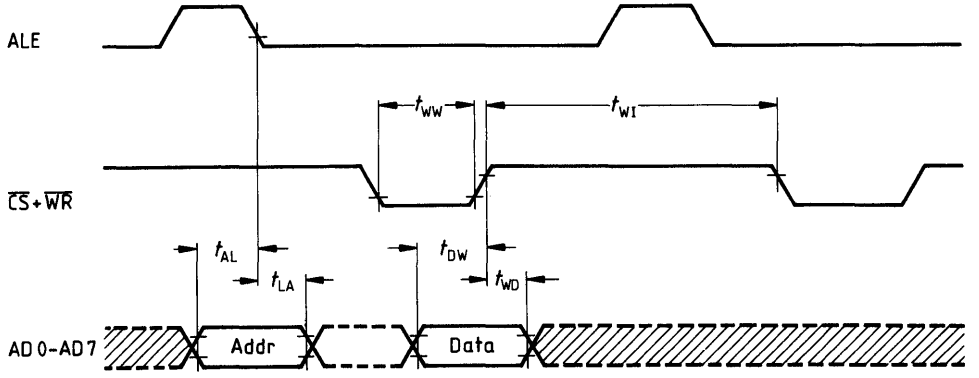


Microcontroller Interface Timing

µP Read Cycle



µP Write Cycle



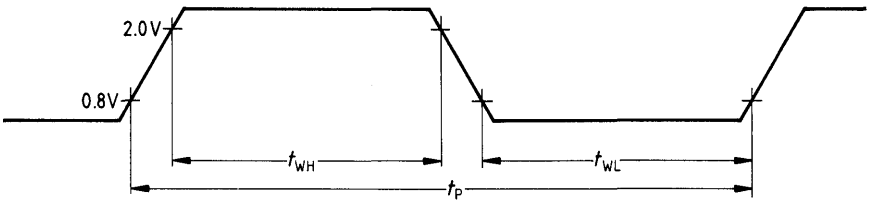
Interface Timing

Parameter	Symbol	Limit Values		Unit
		min.	max.	
ALE pulse width	t_{AA}	50		ns
Address setup time to ALE	t_{AL}	20		ns
Address hold time from ALE	t_{LA}	10		ns
$\overline{RD}$ pulse width	t_{RR}	120		ns
Data output delay from $\overline{RD}$	t_{RD}		120	ns
Data float delay from $\overline{RD}$	t_{DF}		25	ns
$\overline{RD}$ control interval	t_{RI}	75		ns
$\overline{WR}$ pulse width	t_{WW}	60		ns
Data setup time to $\overline{WR} + \overline{CS}$	t_{DW}	30		ns
Data hold time from $\overline{WR} + \overline{CS}$	t_{WD}	10		ns
$\overline{WR}$ control interval	t_{WI}	70		ns

Serial Interface Timing

DCLK Characteristics

Definition of DCLK Period and Width



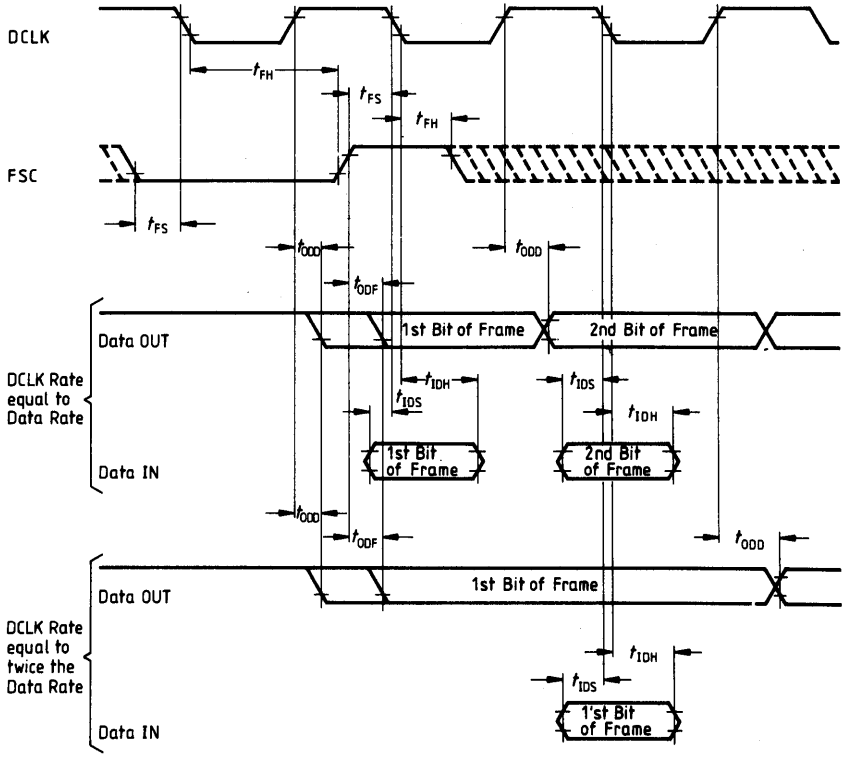
DCLK Characteristics

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
DCL period	t_P	230 160			ns ns	single clock rate double clock rate
DCL high	t_{WH}	90 50			ns ns	single clock rate double clock rate
DCL low	t_{WL}	70			ns	

Input/Output Characteristics

FSC in Single Connection Modes and Quad Connection TS Mode.

FSC Timing Characteristics



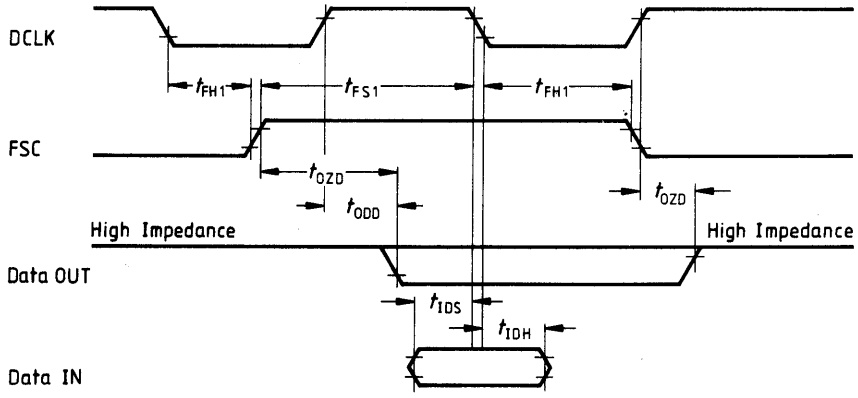
Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
FSC set-up time	t_{FS}	60			ns
FSC hold time	t_{FH}	30			ns
Output data delay from DCLK	t_{ODD}			60	ns
Input data set-up	t_{IDS}	25			ns
Input data hold	t_{IDH}	20			ns
Output data delay from FSC*	t_{ODF}			150	ns

* This delay is applicable in two cases only:

1) When FSC appears for the first time, e.g. at system power-up.
2) When the number of bits in the PCM frame is not equal to either 256 or 512

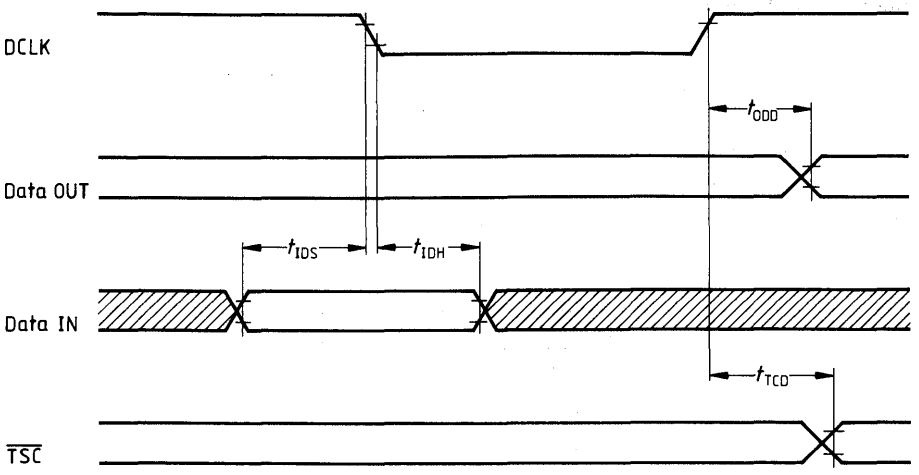
FSC in Quad Connection Common Control Mode

FSC (strobe) Characteristics



Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
FSC set-up time	t_{FS1}	60			ns
FSC hold time	t_{HF1}	30			ns
Output data from high impedance to active	t_{OZD}			80	ns
Output data from active to high impedance	t_{ODZ}			40	ns
Output data delay from DCL	t_{ODD}			60	ns
Input data set-up	t_{IDS}	25			ns
Input data hold	t_{IDH}	20			ns

Data I/O Characteristics



Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Output data delay from DCLK	t_{ODD}			60	ns
Input data set-up	t_{IDS}	25			ns
Input data hold	t_{IDH}	20			ns
TSC delay from DCLK	t_{TCD}			60	ns

Data OUT: SD0X in single connection modes
SD0X, SD1X, SD2X, SD3X in quad connection modes
SD1X, SD2X in master mode

Data IN: SD0R in single connection mode
SD0R, SD1X, SD2R, SD3R in quad connection modes

CDR in slave, multi-master and master modes

RES Characteristics

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
RES high	t_{RWL}	4 x t_P			ns

SIEMENS

S-Bus Interface Circuit (SBC) PEB 2080

Preliminary Data **CMOS-IC**

Type	Ordering Code	Package
PEB 2080-C	Q67100-H8329	C-DIP-22
PEB 2080-N	Q67100-H8395	PL-CC-28 (SMD)
PEB 2080-P	Q67100-H2954	P-DIP-22

The S-Bus Interface Circuit (SBC) PEB 2080 implements the four-wire S/T-interface used to link voice/data terminals to an ISDN. Through selection of operating mode, the device may be employed in all types of applications involving an S-interface. Two or more SBCs can be used to build a point-to-point, passive bus, extended passive bus or star configuration.

Specific ISDN applications of the SBC include: ISDN terminals, ISDN network termination (Central Office and PBX applications), and PBX trunk lines to Central Office.

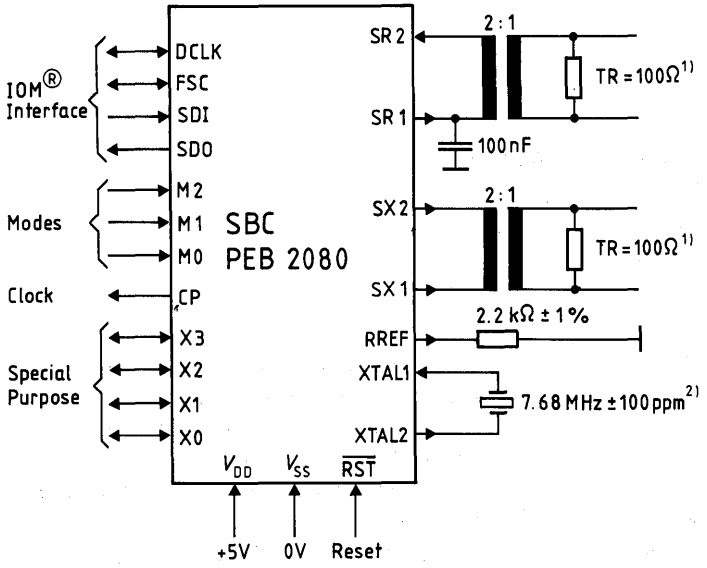
The device provides all electrical and logical functions according to CCITT recommendation I.430. These include: mode-dependent receive timing recovery, D-channel access and priority control, and automatic handling of activation/deactivation procedures. The SBC does not require direct microprocessor control.

The SBC is an IOM® compatible, 22-pin CMOS device. It operates from a single +5 V supply and features a power-down state with very low power consumption.

Features

- Full duplex 2B + D S/T-interface transceiver according to CCITT I.430
- Conversion of the frame structure between the S/T and IOM interfaces
- D-channel access control
- Activation and deactivation procedures according to CCITT I.430
- Built-in wake-up unit for activation from powerdown state
- Adaptively switched receive threshold
- Control via IOM interface
- Several operating modes
- Receive timing recovery according to selected operating mode
- Frame alignment with absorption of phase wander in trunk line applications
- Switching of test loops
- Advanced CMOS technology
- Low power consumption: standby less than 4 mW
  active max 60 mW

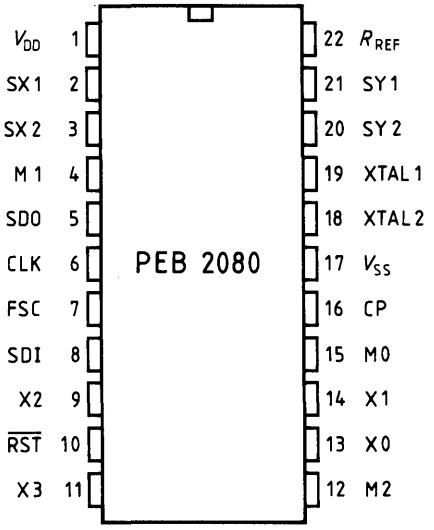
Logic Symbol



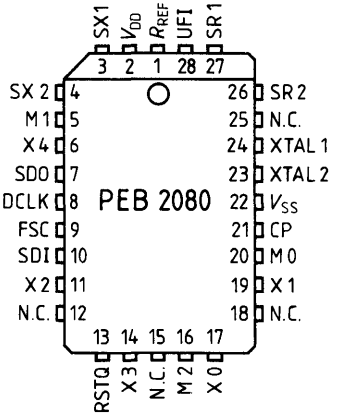
* Terminating resistors only at the far ends of the connection

Pin Configurations
(top view)

P-DIP-22; C-DIP-22



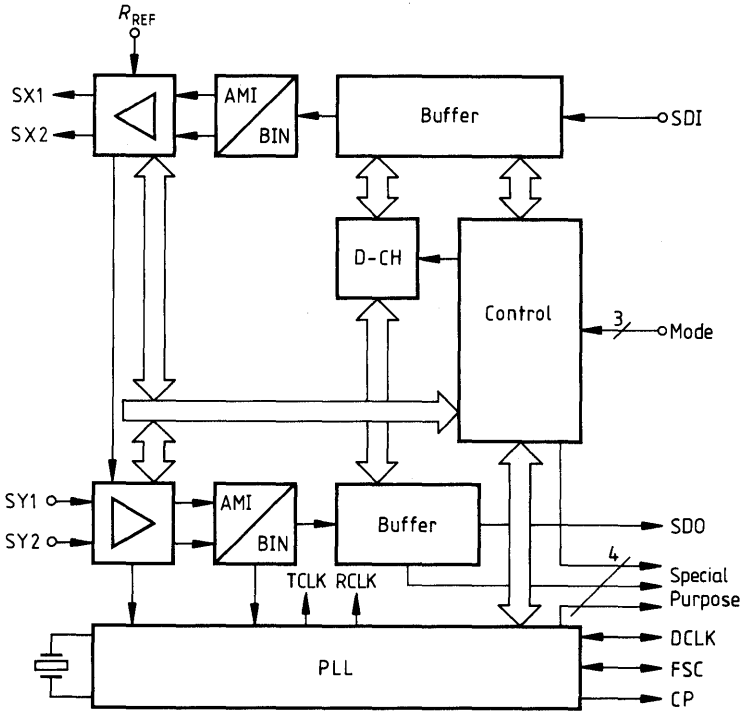
PL-CC-28



Pin Definitions and Functions

Pin No.	Symbol	Input (I) Output (O)	Function
2	SX1	O	Positive output S-bus transmitter
3	SX2	O	Negative output S-bus transmitter
5	SDO	O	Serial data out, IOM interface
8	SDI	I	Serial data in, IOM interface
6	DCLK	I/O	Serial data clock, IOM interface
7	FSC	I/O	Frame Sync, IOM interface
12 4 15 11	M2 M1 M0 X3	I I I I	} Setting of operating mode
9 14 13	X2 X1 X0	I/O I/O I/O	Functions depending on the selected operating mode **see chapter Operating Modes**
16	CP	I/O	Clock Pulse/special purpose
19	XTAL1	I	Connection for external crystal, or input for external clock generator
18	XTAL2	O	Connection for external crystal, N.C., when external clock generator is used.
20	SR2	I	S-bus Receiver, signal input
21	SR1	O	S-bus Receiver, 2.5 V reference output
22	R_{REF}	O	Connection of reference resistor to ground (2.2 kΩ ± 1%)
1	V_{DD}	I	Power supply, +5 V ± 5%
17	V_{SS}	I	Power supply, ground
10	$\overline{RST}$	I	Reset, active low

Block Diagram



System Integration

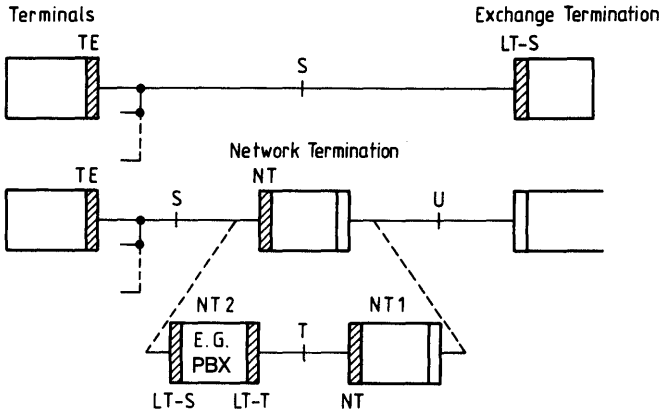
The SBC implements the four-wire S and T interfaces used in the ISDN basic access. It may be used at both ends of these interfaces.

The Applications Include

ISDN terminals (TE)
ISDN network termination (NT)
ISDN subscriber line termination (LT-S)
ISDN trunk line termination (LT-T)
(PBX connection to Central Office).

These applications are shown in **figure 1,** where the usual nomenclature as defined by the CCITT for the basic access functional blocks and reference points has been used.

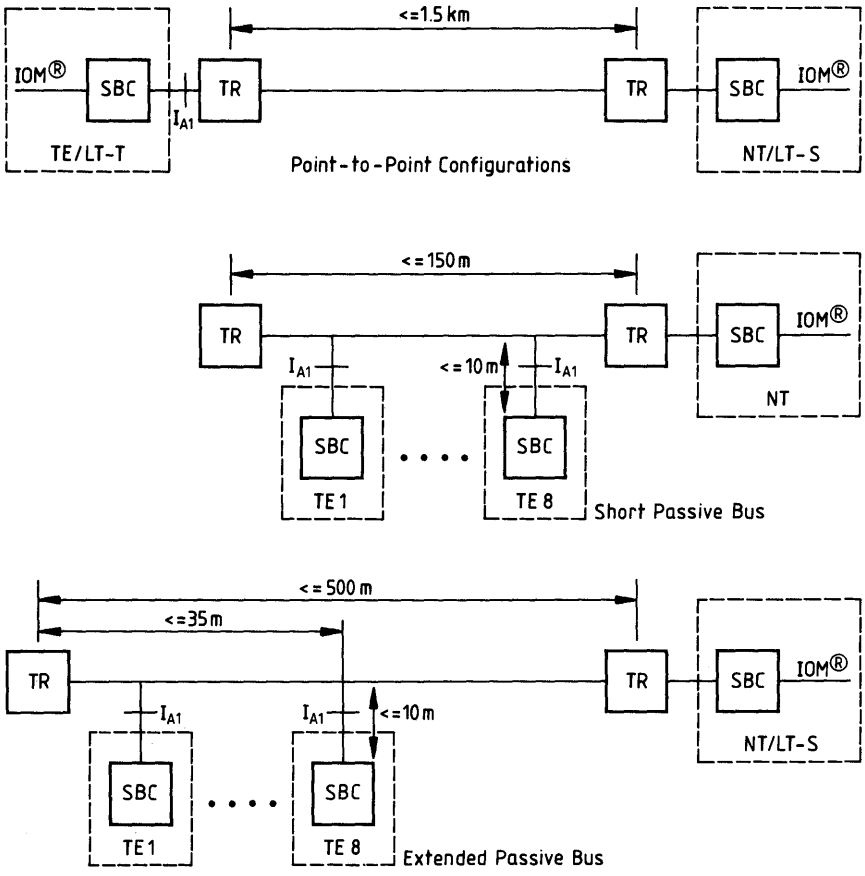
Figure 1
Applications of the SBC



Some of the S interface wiring configurations possible with the SBC are shown in **figure 2**, with approximate typical distances.

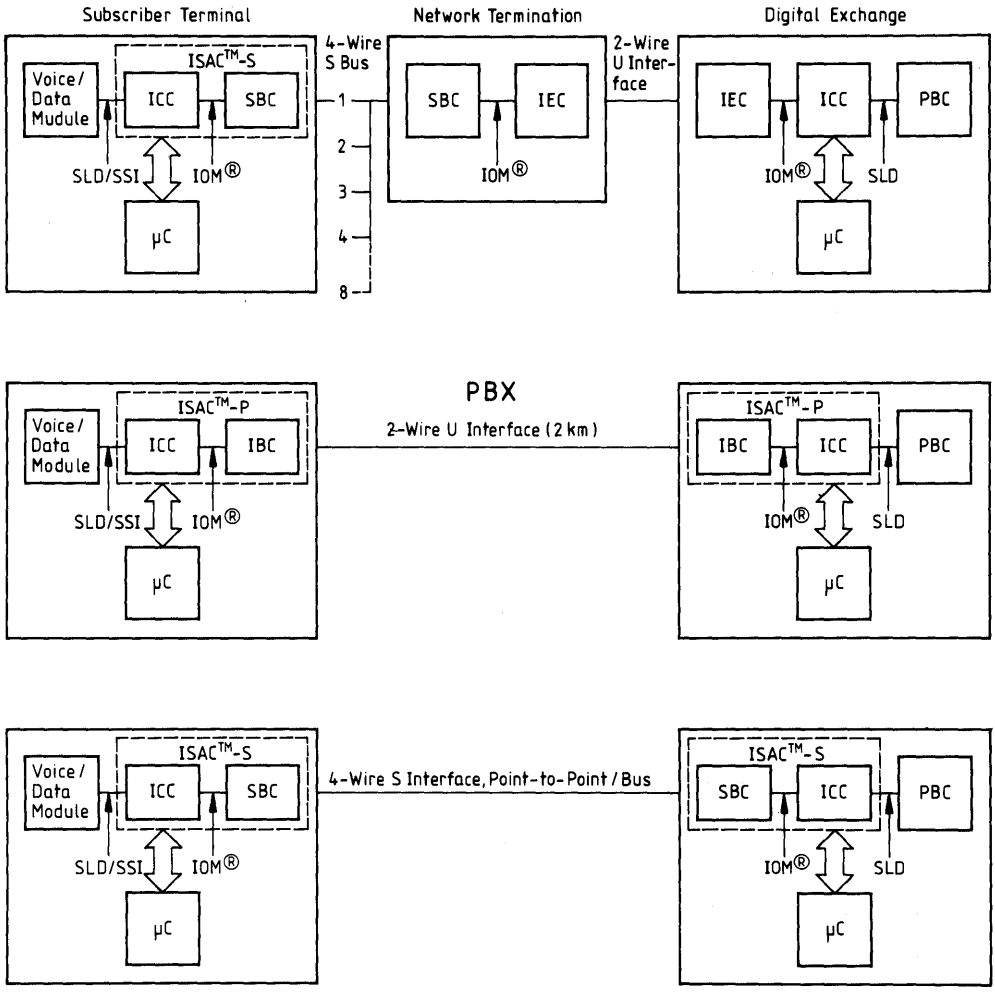
*) (N.B.: "TR" stands for terminating resistor of value 100 Ω).

Figure 2
Some S-Interface Wiring Configuration



*) The maximum line attenuation tolerated by the SBC is 15 dB at 96 kHz.

Figure 3
ISDN Oriented Modular (IOM) Architecture



PEB 2050	Peripheral Board Controller	PBC
PEB 2070	ISDN Communication Controller	ICC
PEB 2080	S Bus Interface Circuit	SBC
PEB 2085	ISDN Subscriber Access Controller (S Bus)	ISAC™-S
PEB 2090	ISDN Echo Cancellation Circuit	IEC
PEB 2095	ISDN Burst Transceiver Circuit	IBC
PEB 20950	ISDN Subscriber Access Controller (PBX, U Interface)	ISAC™-P

Figure 3 gives an example of an application of the SBC in an IOM (ISDN Oriented Modular) architecture.

By separate implementation of OSI layer-1 and layer-2 functions, and through unified control procedures, the architecture provides flexibility with respect to various transmission techniques. The IOM devices are all low-power, high integration, single +5 V supply CMOS devices. Through mode switching, each devices may be used in several applications: thus with one and the same limited set of devices all ISDN basic access configurations are covered. Note that none of the compatible layer-1 devices (SBC, IBC, IEC) requires direct microprocessor control. This is due to the fact that IOM interface provides all the necessary functions for layer-1 – layer-2 communication.

Functional Description

The S-bus interface circuit PEB 2080 performs the layer 1 functions for the S/T interface of the ISDN basic access.

General Functions and Device Architecture

The common functions for all operating modes are:

- line transceiver functions for the S interface according to the electrical specifications of CCITT I.430;
- dynamically adaptive threshold control for the receiver;
- conversion of the frame structure between IOM and S interfaces;
- conversion from/to binary to/from pseudo-ternary code.

Mode specific functions are:

- receive timing recovery;
- S timing generation using IOM timing synchronous to system, or vice versa;
- D-channel access control and priority handling;
- D-channel echo bit generation;
- activation/deactivation procedures, triggered by primitives received over the IOM interface or by INFO's received from the line;
- frame alignment according to CCITT Q.503;
- execution of test loops.

For a block diagram, **see figure Block Diagram**

Analog Functions

The full-bauded pseudo-ternary pulse shaping is achieved with the integrated transmitter which is realized as a voltage limited current source. A current of 7.5 mA is delivered over SX1-SX2, which yields a voltage 1.5 V over 200 Ω.

The receiver is designed as a threshold detector with adaptively switched threshold levels. Pin SR1 delivers 2.5 V as an output, which is the virtual ground of the input signal on pin SR2.

An external transformer of ratio 2:1 is needed in both receive and transmit direction to provide for isolation and transform voltage levels according to CCITT recommendations.

Digital Functions

A DPLL circuitry working with a frequency of 7.68 MHz ±100 ppm serves to generate the 192-kHz-line-clock from the reference clock delivered by the network and to extract the 192-kHz-line clock from the receive data stream.

The 7.68-MHz-clock may be generated with the use of an external crystal between pins XTAL1 and XTAL2. It may also be provided by an external oscillator, in which case XTAL2 is left unconnected.

The "Control" block includes the logic to detect layer-1 commands and to communicate with external layer-1 or layer-2 devices via the IOM interface.

An incorporated finite state machine controls ISDN layer-1 activation/deactivation.

The D-channel access procedure according to CCITT I.430 including priority management is fully implemented in the SBC. When used as an S-bus master in a multipoint configuration, the device generates the echo bits necessary for D-channel collision detection. In the NT-mode, moreover, the echo channel may be made externally available through an auxiliary pin and thus "intelligent NT's" (star configuration) may be implemented.

In terminal applications (TE) the Q channel as specified by I.430 is supported*).

The buffer memory serves to adapt the different bit rates of the S and the IOM interface. In addition, in trunk line applications it absorbs the possible deviation between two system clocks, according to CCITT Q.503 (slip detection).

Operating Modes

The operating modes are determined by pin strapping on pins M0 to M2. The four basic operating modes are: TE, NT, LT-S, LT-T.

In three of these operating modes, the IOM may be programmed to function in the normal mode, in the inverted mode (clock frequency 512 kHz) or in the inverted mux mode (clock frequency 4096 kHz). To see which IOM timing mode is applicable in the four basic operating modes, refer to **table 1.**

In **table 1**, the functions of the operating mode specific pins are given: these pins are DCLK (IOM interface data clock, input/output), FSC (IOM interface frame sync, input/output), CP (auxiliary clock/test pin), and X0 to X3.

Depending on the selected mode, pins CP, X2 and X1 provide auxiliary clocks, either asynchronous or synchronous to the S-interface:

3840 kHz
2560 kHz
1280 kHz
} clocks derived from the 7680-kHz-crystal

1536 kHz
512 kHz
} clocks synchronized to S-interface.

These auxiliary clocks may be used to drive, e.g. a codec filter, or a microprocessor system (TE applications).

*) Stepping A 6 and up. The SBC sends a binary one in FA bit position to allow another terminal to use the extra transmission capacity.

The other uses of the auxiliary pins are:

$\overline{\text{ENCK}}$	input	Enable clock. At "0", forces the SBC to deliver IOM timing at all times, regardless of SDI input level; in TE mode, pin X3.
Bus	input	At "1", specifies a bus configuration (as opposed to point to point or extended passive bus); in NT and LT-S modes, pin X3.
ECHO	output push-pull	Reproduces the E-bits received from the S-interface synchronously to IOM frame "D"-bits (bit positions 24 and 25 of IOM frame). All other bit positions are binary "1"; in TE mode, pin X2.
$\overline{\text{SSZ}}$	input	Send Single Zeros. At "0", forces the SBC to transmit alternating pulses at 250 µs intervals (period 2 kHz) on S-interface for test purposes; X2 in NT mode.
RDY	output push pull	Ready. Provides a signal logically equal to bit 3 of monitor channel. Signals the D-channel status ("0" = occupied, "1" = free) to layer 2 component; X0 in TE mode.
CON	input	Connected. At "0", prevents the SBC from activating and transmitting on the S-interface. Indicates whether the device is connected to the S-interface or not; X0 in TE and LT-T modes.
DEX	input	External D-channel echo enable. At "1", makes the E-bit dependent on the DE (X0) input. Used in NT mode to build a star configuration; X1 in NT mode.
DE	input/ output open drain with integrated pull-up resistor	D-channel Echo. The DE outputs should be tied together (open drain) in an NT star configuration, to obtain the global echo bit; X0 in NT mode.
TS0 to TS 2	inputs	Time slot 0 to 7. IOM interface time slot to be used = 4 x TS2 + 2 x TS1 + TS0; LT-T and LT-S in IOM mux mode.

Table 1
Operating Modes and Functions of Mode Specific Pins of PEB 2080

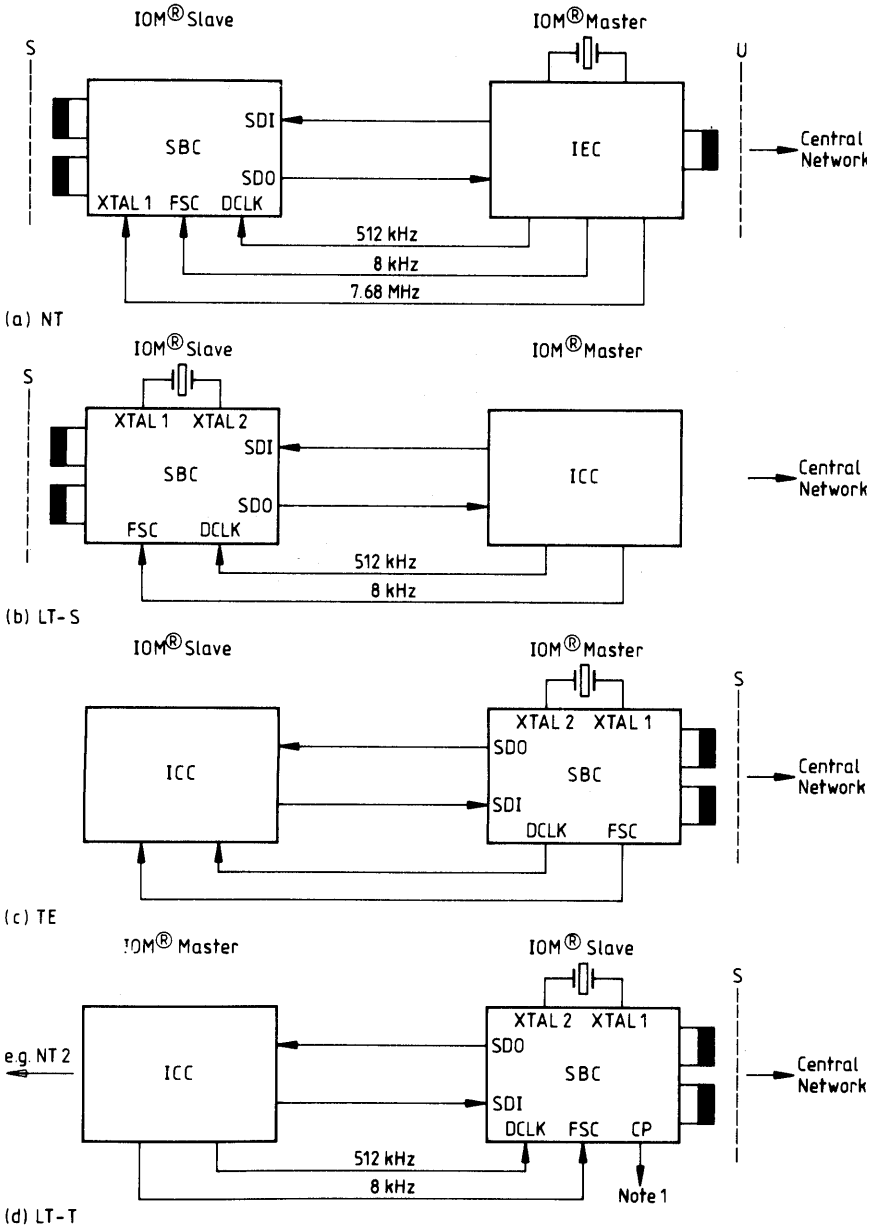
	Application								
	TE	**TE**	**TE**	**LT-T**	**LT-T**	**NT**	**LT-S**	**LT-S**	**LT-S**
Operation of IOM Interface	Inverted Mode	Inverted Mode	Normal Mode	Mux Mode Inverted	Normal Mode	Normal Mode	Mux Mode Inverted	Normal Mode	Normal Mode
M2 M1 M0	0 0 0	0 0 1	0 1 0	0 1 1	0 1 1	1 1 1	1 0 0	1 1 0	1 1 0
DCLK	o:512kHz*	o:512kHz*	o:512kHz*	i:4096kHz	i:512kHz	i:512kHz	I:4096kHz	i:512kHz	i:512kHz
FSC	o:8kHz*	o:8kHz*	o:8kHz*	i:8kHz	i:8kHz	i:8kHz	i:8kHz	i:8kHz	i:8kHz
CP	o: 1536kHz*	o: 1536kHz*	o: 1536kHz*	o:512kHz*	o:512kHz*	i:$\overline{SCZ}$	i: fixed at 0	i: fixed at 0	i: fixed at 0
X3	i:$\overline{ENCLK}$	i:$\overline{ENCLK}$	i:$\overline{ENCLK}$	i: fixed at 1	i: fixed at 0	I: BUS	i: BUS	i: BUS	i: BUS
X2	o: 2560kHz	o: 1280kHz	o:ECHO	i: TS2	i: fixed at 0	i:$\overline{SSZ}$	i:TS2	i: fixed at 0	o:192kHz
X1	o: 3840kHz	o: 3840kHz	o: 3840kHz	i:TS1	i: fixed at 0	i:DEX	i:TS1	o: 7680kHz	o: 7680kHz
X0	o:RDY	o:RDY	i:CON	i:TS0	i:CON	i/o:DE	i:TS0	i: fixed at 0	i:fixed at 1

*) synchronized to S i: input o: output

$\overline{SCZ}$	Send continuous binary zeros (96 kHz)
ENCLK	Enable clock at all times
BUS	Bus configuration specified
TS2-0	Time-slot number of IOM
$\overline{SSZ}$	Send single binary zeros (2 kHz)
DEX	D-channel echo external/internal
RDY	D-channel status on S-interface
CON	Connected to S bus
DE	D-channel echo bit in NT star configuration

Figure 4

Clocking of SBC in Different Operating Modes



IEC = ISDN Echo Cancellation Circuit PEB 2090
ICC = ISDN Communication Controller PEB 2070

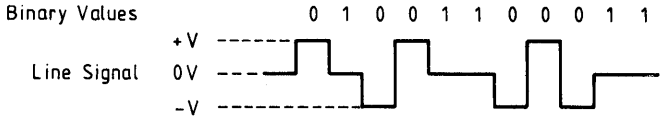
Note 1: Reference clock (512 kHz, duty cycle 1:2) may be used to drive, e.g. NT 2 clock generator

Interfaces

S Interface

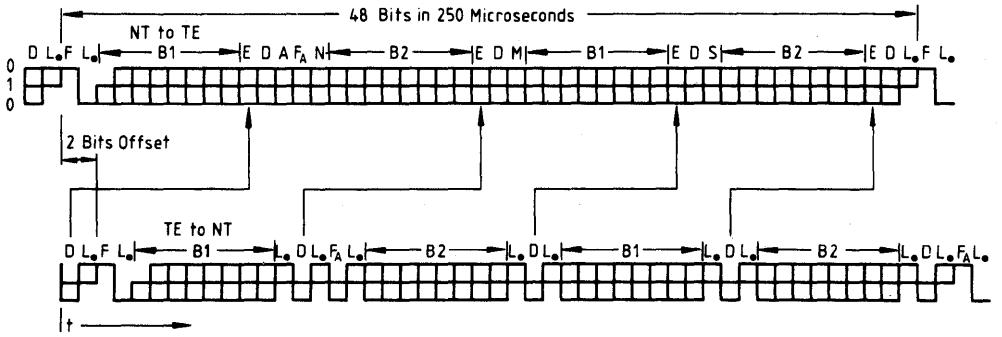
According to CCITT recommendation I.430, pseudo-ternary encoding with 100% pulse width is used on the S interface. A logical 1 corresponds to a neutral level (no current), whereas logical 0's are encoded as alternating positive and negative pulses. An example is shown in **figure 5**.

Figure 5
S Interface Line Code



One S-frame consists of 48 bits, at a nominal bit rate of 192 kbit/s. Thus each frame carries two octets of B1, two octets of B2, and four D-bits, according to the B1+B2+D structure defined for the ISDN basic access (total useful data rate: 144 kbit/s). Frame begin is marked using a code violation (no mark inversion). The frame structures (from network to subscriber, and subscriber to network) are shown in **figure 6**.

Figure 6
Frame Structure at Reference Points S and T (CCITT I.430)



F = Framing Bit
L = DC Balancing Bit
D = D-Channel Bit
E = D-Echo-Channel Bit
F = Auxiliary Framing Bit or Q-Bit
N = Bit Set to a Binary Value N = $\overline{F_A}$

B1 = Bit within B-Channel 1
B2 = Bit within B-Channel 2
A = Bit Used for Activation
S = S-Channel Bit
M = Multiframing Bit

Note: Dots Demarcate those Parts of the Frame that are Independently DC-Balanced.

Digital Interface

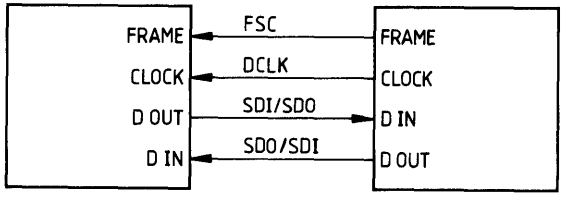
IOM Frame Structure

The SBC is provided with a digital interface, the IOM interface, for communication with other ISDN devices, in other words with units realizing OSI layer-1 functions (such as the ISDN Echo Cancellation Circuit IEC PEB 2090) or layer-2 functions (such as the ISDN Communication Controller ICC PEB 2070).

The IOM interface is a four-wire serial interface with: a bit clock, a frame clock and one data line per direction **(figure 7)**.

The ISDN data rate of 144 kbit/s (B1 + B2 + D) is transmitted transparently in both directions over the interface. In addition, it is necessary to interchange control information for activation and deactivation of OSI layer-1 and for switching of test loops. This information is transferred using time division multiplexing with a 125-µs total frame length.

Figure 7
IOM Interface Signals

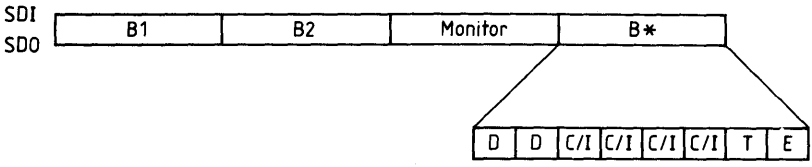


In LT-S :	SBC	ICC
In NT :	SBC	IEC
In LT-T :	SBC	ICC
In TE :	ICC	SBC

The basic frame consists of a total of 32 bits, or four octets: B1 + B2 + D (18 bits) plus 14 bits of monitor and control information. The data in both directions are synchronous and in phase **(figure 8)**.

Figure 8

IOM Interface Frame Structure



1st octet B1: B channel (64 kbit/s), most significant bit first
2nd octet B2: B channel (64 kbit/s), most significant bit first
3rd octet: monitor channel (64 kbit/s), most significant bit first
4th octet B*: 2 bit D channel (16 kbit/s)
4 bit C/I channel
T channel: not used with SBC
E bit: not used with SBC.

The C/I channel is used for communication between the SBC and a processor via a layer-2 device, to control and monitor layer-1 functions. The codes originating from layer-2 devices are called "commands", those sent by the SBC are called "indications". For a list of the C/I codes and their use, see the SBC Technical Manual.

Three modes of the IOM are distinguished. These modes differ only with respect to the physical data rate (256 or 8 x 256 kbit/s) and to polarity of the clocks.

Normal Mode

This timing mode is applicable in all operating modes of the SBC.

Nominal bit rate of data (SDI and SDO): 256 kbit/sec

Nominal frequency of DCLK: 512 kHz

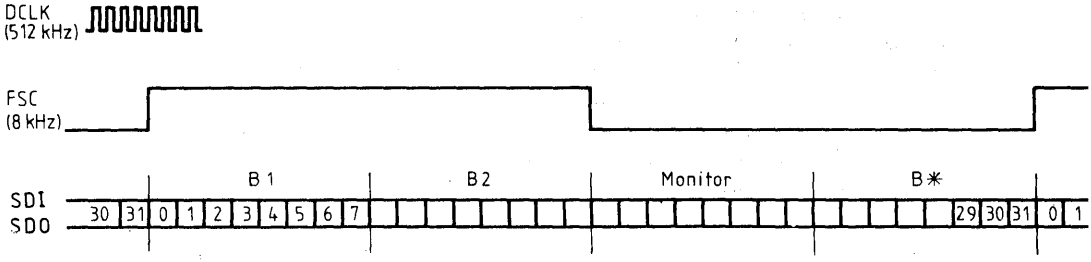
Nominal frequency of FSC: 8 kHz

Transitions of the data occur after even-numbered rising edges of DCLK. Even-numbered rising edges of the clock are defined as the second rising edge following the rising edge of FSC and every second rising edge thereafter.

The frame is earmarked by the rising edge of FSC.

Figure 9

Timing of Data and Clocks of IOM in the Normal Mode



Inverted Mode

This timing mode is only applicable in TE mode.

The characteristics are the same as above, except that FSC is not a signal with 50% duty cycle but an active low pulse, one DCLK clock period long, which occurs in the middle of bit 27 (fourth bit of B*).

Inverted Mux Mode

This timing mode is applicable in the LT-T and LT-S operating modes.

Nominal bit rate of data bursts (SDI and SDO)	2048 kbit/sec
Nominal frequency of DCLK	4096 kHz
Nominal frequency of FSC	8 kHz.

The frame clock FSC is an active low strobe clock. The strobe earmarks the second half of bit no. 251 in the frame. The low state of the strobe is detected with the rising edge of DCLK. Refer to **figure 10**.

The data at the input SDI is valid on the even-numbered rising edges of DCLK. Transitions of the data on SDO occur after even-numbered falling edges of DCLK. The rising edge earmarked by the frame strobe is an even-numbered rising edge of DCLK. The following falling edge is an even-numbered falling edge.

The bursts are allocated to consecutive time slots in a frame by the static inputs X0(TS0), X1(TS1), X2(TS2). **Table 2** indicates the allocations. **Figure 11** gives the positions of the respective frames.

Figure 10

Timing of Data and Clocks of IOM in the Inverted Mux Mode

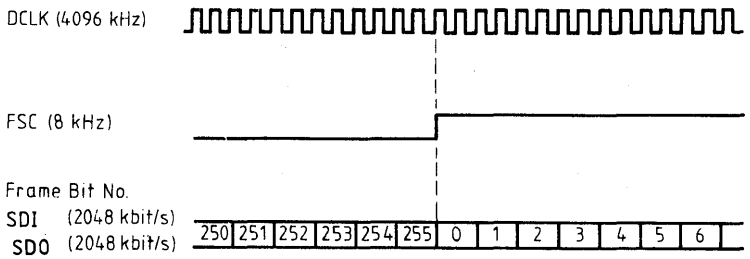
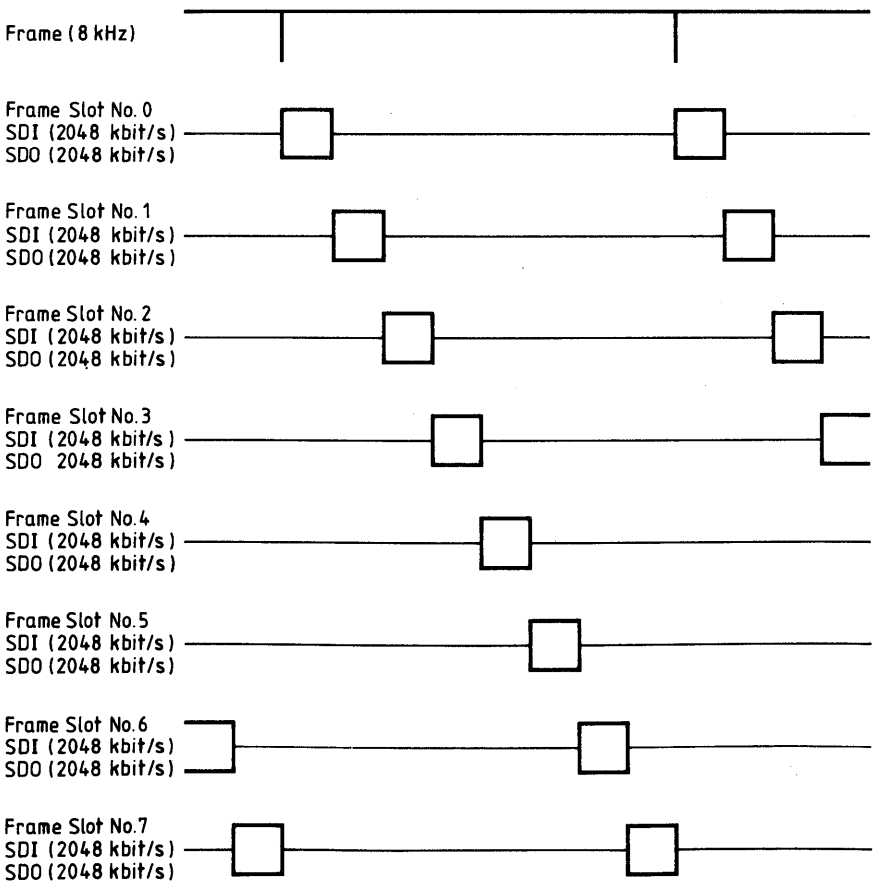


Table 2
Allocation of Time Slots

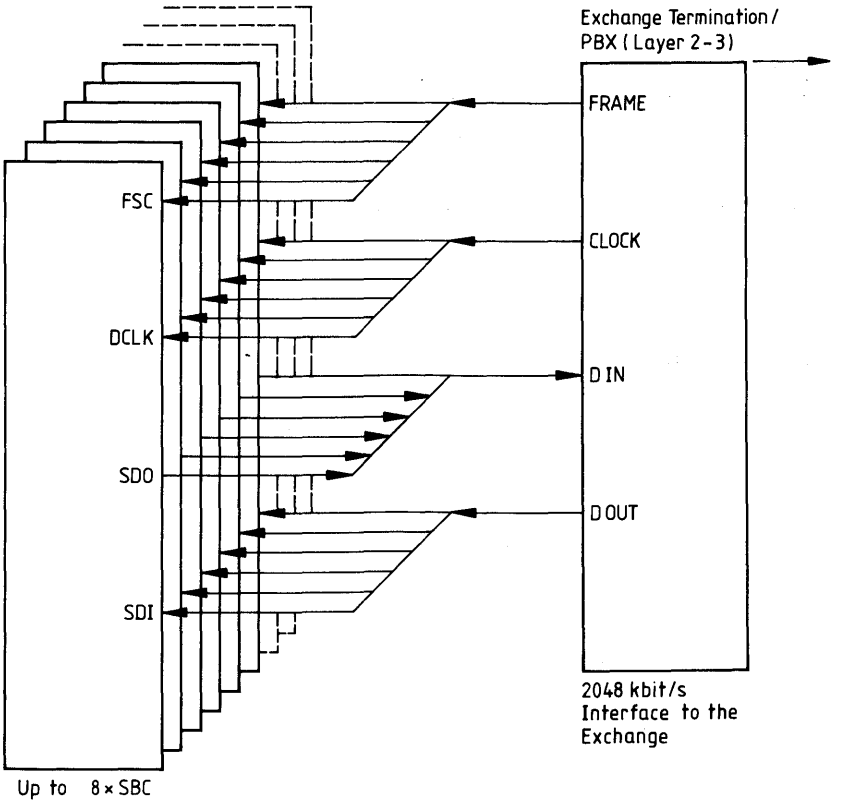
Time Slot No.	TS2	TS1	TS0	Bit No.
0	0	0	0	0 ... 31
1	0	0	1	32 ... 63
2	0	1	0	64 ... 95
3	0	1	1	96 ... 127
4	1	0	0	128 ... 159
5	1	0	1	160 ... 191
6	1	1	0	192 ... 223
7	1	1	1	224 ... 255

Figure 11
Position of IOM Frames as a Function of Time-Slot Allocation in Inverted Mux Mode



The mux mode may be used to link up to eight SBC's over a single 2048 kbit/s interface to an exchange or PBX **(figure 12)**.

Figure 12
IOM Interface 2048 kbit/s Mux Mode



Absolute Maximum Ratings

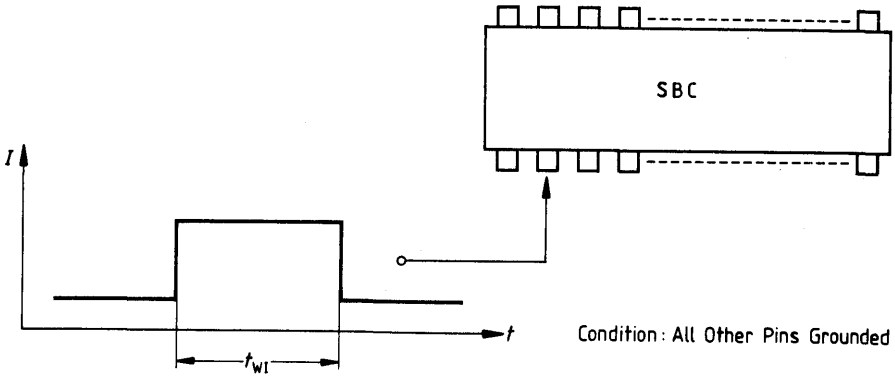
Parameter	Symbol	Limit Values	Unit
Voltage on any pin with respect to ground	V_S	-0.4 to $V_{DD}+0.4$	V
Power dissipation	P_D	1	W
Ambient temperature under bias	T_A	0 to 70	°C
Storage temperature	T_{stg}	−65 to 125	°C

Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Line Overload Protection

The maximum input current (under overvoltage conditions) is given as a function of the width of a rectangular input current pulse **(figure 13)**.

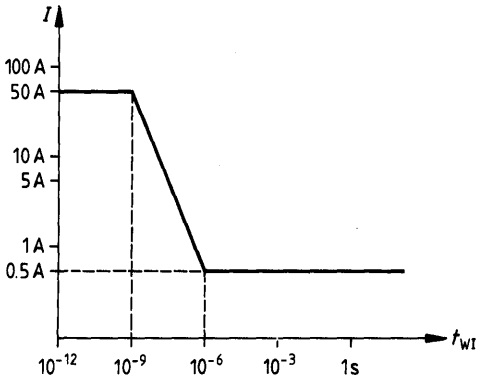
Figure 13
Test Condition for Maximum Input Current



Transmitter Input Current

The destruction limits are given in **figure 14.**
$R_i \geq 2\ \Omega$.

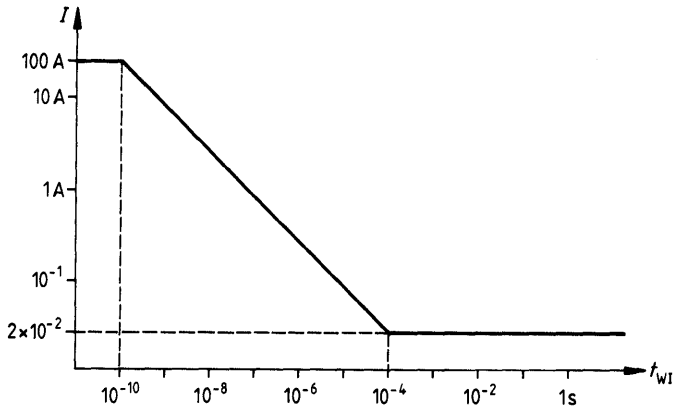
Figure 14



Receiver Input Current

The destruction limits are given in **figure 15.**
$R_i \geq 300\ \Omega$.

Figure 15



DC Characteristics

$T_A = 0$ to 70 °C; $V_{DD} = 5\ V \pm 5\%$, $V_{SS} = 0\ V$

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit	Test Conditions	
L-input voltage	V_{IL}	−0.4	0.8	V		
H-input voltage	V_{IH}	2.0	V_{DD} +0.4	V		All pins
L-output voltage	V_{OL}		0.45	V	$I_{OL} = 2$ mA	ex-
L-output voltage (SDO)	V_{OL1}		0.45	V	$I_{OL} = 7$ mA	cept
H-output voltage	V_{OH}	2.4		V	$I_{OH} = -400\ \mu A$	SX1,2
H-output voltage	V_{OH}	V_{DD} −0.5		V	$I_{OH} = -100\ \mu A$	SR1,2
						RREF
Power supply current — operational	I_{CC}		12	mA	$V_{DD} = 5$ V, inputs at V_{SS}/V_{DD}, no output loads	
Power supply current — power down	I_{CC}		0.8	mA	$V_{DD} = 5$ V, inputs at V_{SS}/V_{DD}, no output loads	
Input leakage current	I_{LI}		10	µA	$0\ V < V_{IN} < V_{DD}$ to 0 V	
Output leakage current	I_{LO}		10	µA	$0\ V < V_{OUT} < V_{DD}$ to 0 V	
Absolute value of output pulse amplitude (VSX2 − VSX1)	V_X	1.35	1.65	V	$R_L = 50\ \Omega$ [1]	
		1.35	2.4	V	$R_L = 400\ \Omega$ [1]	
		2.03	2.31	V	$R_L = 50\ \Omega$ [1] [2]	
		2.10	2.39	V	$R_L = 400\ \Omega$ [1] [2]	
Transmitter output current	I_X	7.5	13.4	mA	$R_L = 5.6\ \Omega$ [1]	
Transmitter output impedance	R_X	10		kΩ	inactive or during binary one	SX1,2
		80		Ω	during binary zero [3] $R_L = 50\ \Omega$	
Receiver output voltage	V_{SR1}	2.4	2.6	V	$I_O < 5\ \mu A$	SR1,2
Receiver threshold voltage VSR1 − VSR2	V_{TR}	225	375	mV	dependent on peak level	
Voltage at RREF	V_O	1.0	1.2	V	$R_{REF} = 2.2\ k\Omega \pm 1\%$	RREF [4]
Output current	I_O	450	550	µA	$R_{REF} = 2.2\ k\Omega \pm 1\%$	

Notes: 1) Due to the transformer, the load resistance as seen by the circuit is four times R_L.
2) From SBC A7 onwards.
3) From A7 onwards, the 80 Ω output impedance is external.
4) Applies only up to A6.

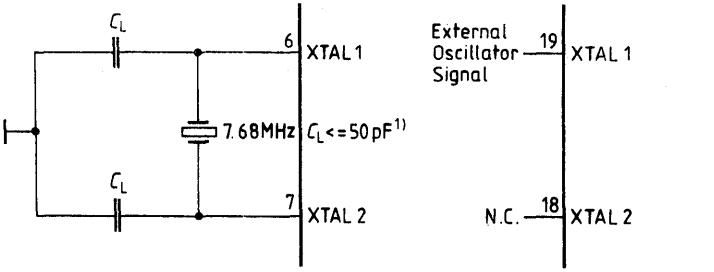
Cpacitances

$T_A = 25\,°C$, $V_{DD} = 5\,V \pm 5\%$, $V_{SS} = 0\,V$

Parameter	Symbol	Limit Values		Unit	
		min.	max.		
Input capacitance I/O capacitance	C_{IN} C_{IO}		7 7	pF pF	All pins except SR1,2 XTAL1,2
Output capacitance against V_{SSA}	C_{OUT}		10	pF	SX1,2
Input capacitance	C_{IN}		7	pF	SR1,2
Load capacitance	C_{LD}		50*)	pF	XTAL1,2

Recommended Oscillator Circuit

Figure 16



Crystal Oscillator Mode

Driving from External Source

*) for the version up to and including A4 this value should not exceed 20 pF. This maximum capacitance is determined by the maximum oscillator startup time of 4 ms.

Table 3
Output Stages

	Application								
	TE	**TE**	**TE**	**LT-T**	**LT-T**	**NT**	**LT-S**	**LT-S**	**LT-S**
Operation of IOM Interface	Inverted Mode	Inverted Mode	Normal Mode	Mux Mode Inverted	Normal Mode	Normal Mode	Mux Mode Inverted	Normal Mode	Normal Mode
M2 M1 M0	0 0 0	0 0 1	0 1 0	0 1 1	0 1 1	1 1 1	1 0 0	1 1 0	1 1 0
DCLK	Push/Pull	Push/Pull	Push/Pull						
FSC	Push/Pull	Push/Pull	Push/Pull						
CP	Push/Pull	Push/Pull	Push/Pull	Push/Pull	Push/Pull				
X2	Push/Pull	Push/Pull	Push/Pull						Push/Pull
X1	Push/Pull	Push/Pull	Push/Pull					Push/Pull	Push/Pull
X0	Push/Pull	Push/Pull				open drain*			
SDO	Push/Pull	Push/Pull	Push/Pull	open drain	Push/Pull	open drain*	open drain	Push/Pull	

*) with integrated Pull-up

Table 4
SBC Clock Signals

	Application								
	TE	**TE**	**TE**	**LT-T**	**LT-T**	**NT**	**LT-S**	**LT-S**	**LT-S**
Operation Of IOM Interface	Inverted Mode	Inverted Mode	Normal Mode	Mux Mode Inverted	Normal Mode	Normal Mode	Mux Mode Inverted	Normal Mode	Normal Mode
M2 M1 M0	0 0 0	0 0 1	0 1 0	0 1 1	0 1 1	1 1 1	1 0 0	1 1 0	1 1 0
DCLK	o:512kHz* 1:2	o:512kHz* 1:2	o:512kHz* 2:1	i:4096kHz	i:512kHz	i:512kHz	i:4096kHz	i:512kHz	i:512kHz
FSC	o:8kHz* 63:1	o:8kHz* 63:1	o:8kHz*	i:8kHz	i:8kHz	i:8kHz 1:1	i:8kHz	i:8kHz	i:8kHz
CP	o: 1536kHz* 3:2	o: 1536kHz* 3:2	o: 1536kHz* 3:2	o:512kHz* 2:1	o:512kHz* 2:1				
X2	o: 2560kHz 1:2	o: 1280kHz 1:2							o: 192kHz 1:1
X1	o: 3840kHz 1:1	o: 3840kHz 1:1	o: 3840kHz 1:1					o: 7680kHz 1:1	o: 7680kHz 1:1
X0								i: fixed at 0	i: fixed at 1

*) synchronized to S line

Input and Output Pin Configurations

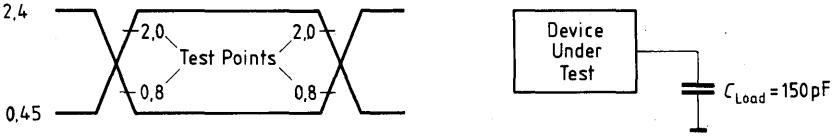
In TE, LT-T and LT-S IOM normal modes an integrated pull-up resistor is connected to SDI. For output pin configurations, **see table 3.**

AC Characteristics

$T_A = 0$ to 70 °C, $V_{DD} = 5\ V \pm 5\%$

The AC testing input/output waveform is shown below.

Figure 17



Jitter

In TE mode, the timing extraction jitter of the SBC conforms to CCITT Recommendation I.430 (−7% to +7% of the S-interface bit period).

In the NT and LT-S applications, the clock input DCLK is used as reference clock to provide the 192-kHz-clock for the S line interface. In the case of a plesiochronous 7.68-MHz-clock generated by an oscillator, the clock DCLK should have a jitter of less than 100 ns peak-to-peak. (In the case of a zero input jitter on DCLK, SBC generates at most 130 ns "self-jitter" on S interface.)

In the case of a synchronous*) 7.68-MHz-clock (input XTAL1), the SBC transfers the input jitter of XTAL1, DCLK and FSC to the S interface. The maximum jitter of the NT/LT-S output is limited to 260 ns peak-to-peak (CCITT I.430).

*) fixed divider ratio of 15 between XTAL1 and DCLK

Clock timing

The clocks in the different operating modes are summarized in **table 4**, with duty ratios.

Clock CP is phase-locked to the receive S signal, and is derived using the internal DPLL and the 7.68 MHz ± 100 ppm crystal (TR and LT-T).

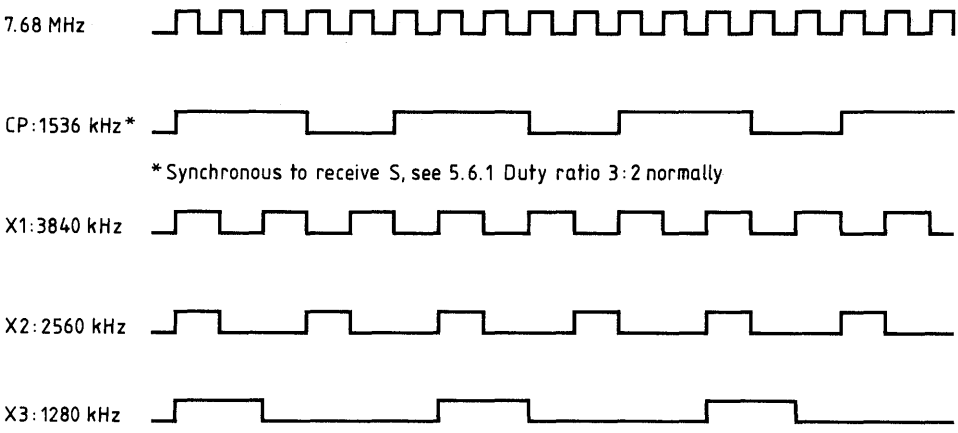
A phase tracking of CP with respect to "S" is performed once in 250 µs. As a consequence of this DPLL tracking, the high state of CP may be either reduced or extended by one 7.68-MHz-period (CP duty ratio 2:2 or 4:2 instead of 3:2) once every 250 ns.

Since DCLK and FSC are derived from CP (TE mode), the high state (FSC) or the high or low state (DCLK) may likewise be reduced or extended by the same amount once every 250 µs.*)

The phase relationships of the auxiliary clocks are shown in **figure 18**.

Figure 18

Phase Relationships of Auxiliary Clocks



*) The phase adjustment may take place either in the sixth, seventh or eight CP cycle counting from the beginning of an IOM frame in TE.

Tables 5 to 9 give the timing characteristics of the clock.

Figure 19
Definition of Clock Period and Width

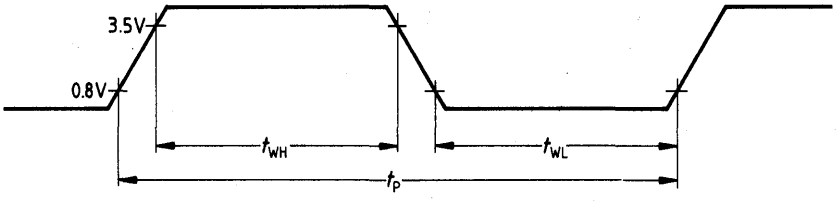


Table 5
XTAL1,2

Parameter	Symbol	Limit Values		Unit
		min.	max.	
High phase of crystal/clock	t_{WH}	20		ns
Low phase of crystal/clock	t_{WL}	20		ns

Table 6
DCLK

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
(TE) 512 kHz	t_{PQ}	1822	1953	2084	ns	OSC ±100 ppm
(TE) 512 kHz 2:1	$t_{W\,HQ}$	1121	1302	1483	ns	OSC ±100 ppm
(TE) 512 kHz 2:1	$t_{W\,LQ}$	470	651	832	ns	OSC ±100 ppm
(TE) 512 kHz 1:2	$t_{W\,HQ}$	470	651	832	ns	OSC ±100 ppm
(TE) 512 kHz 1:2	$t_{W\,LQ}$	1121	1302	1483	ns	OSC ±100 ppm
(NT, LT-S, LT-T)	$t_{W\,HI}$	90			ns	
(NT, LT-S, LT-T)	$t_{W\,LI}$	90			ns	

Table 7
CP

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
(TE) 1536 kHz	t_{PQ}	520	651	782	ns	OSC ±100 ppm
(TE) 1536 kHz	$t_{W\,HQ}$	240	391	541	ns	OSC ±100 ppm
(TE) 1536 kHz	$t_{W\,LQ}$	240	260	281	ns	OSC ±100 ppm
(TE, LT-T)	t_R, t_F			20 10	ns ns	C_L = 100 pF C_L = 50 pF
(LT-T) 512 kHz	t_{PQ}	1822	1953	2084	ns	OSC ±100 ppm
(LT-T) 512 kHz	$t_{W\,HQ}$	1121	1302	1483	ns	OSC ±100 ppm
(LT-T) 512 kHz	$t_{W\,LQ}$	470	651	832	ns	OSC ±100 ppm

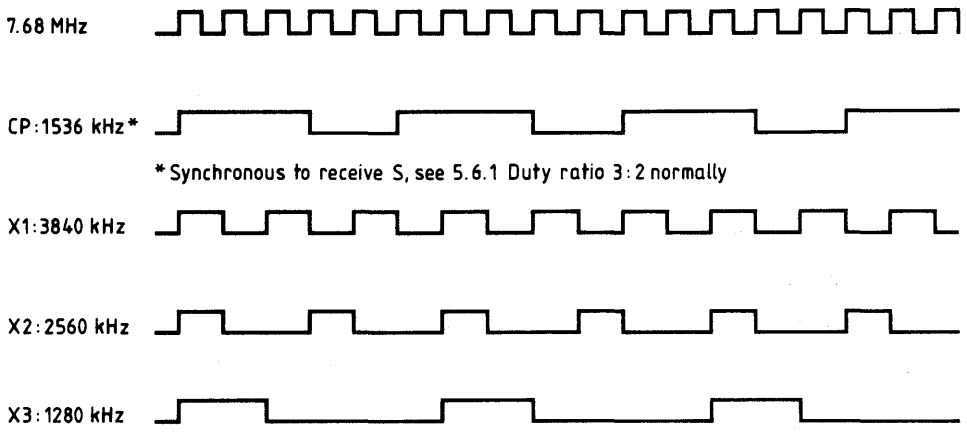
Table 8
X1

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
(TE) 3840 kHz	t_{PQ}	−100 ppm	260	100 ppm	ns	OSC ±100 ppm
(TE) 3840 kHz	$t_{W\,HQ}$	120	130	140	ns	OSC ±100 ppm
(TE) 3840 kHz	$t_{W\,LQ}$	120	130	140	ns	OSC ±100 ppm

Table 9
X2

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
(TE) 2560 kHz	t_{PQ}	−100 ppm	391	100 ppm	ns	OSC ±100 ppm
(TE) 2560 kHz	$t_{W\,HQ}$	110	130	150	ns	OSC ±100 ppm
(TE) 2560 kHz	$t_{W\,LQ}$	250	260	270	ns	OSC ±100 ppm
(TE) 1280 kHz	t_{PQ}	−100 ppm	781	100 ppm	ns	OSC ±100 ppm
(TE) 1280 kHz	$t_{W\,HQ}$	250	260	270	ns	OSC ±100 ppm
(TE) 1280 kHz	$t_{W\,LQ}$	511	521	531	ns	OSC ±100 ppm

CP, DCLK and FSC Relationships in IOM Master Mode

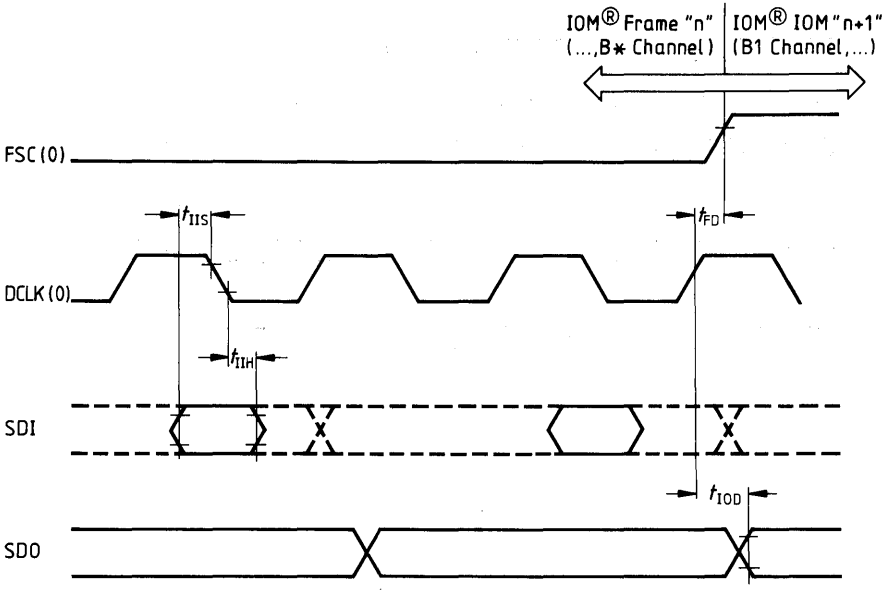


Parameter	Symbol	Limit Values		Unit	Test Conditions
		min.	max.		
Clock delay CP – DCLK	t_{DC}	0	50	ns	$C_L = 100$ pF
Clock delay CP – FSC	t_{FC}	0	50	ns	$C_L = 100$ pF
Delay DCLK – FSC	t_{FD}	−20	20	ns	$C_L = 100$ pF

IOM Interface

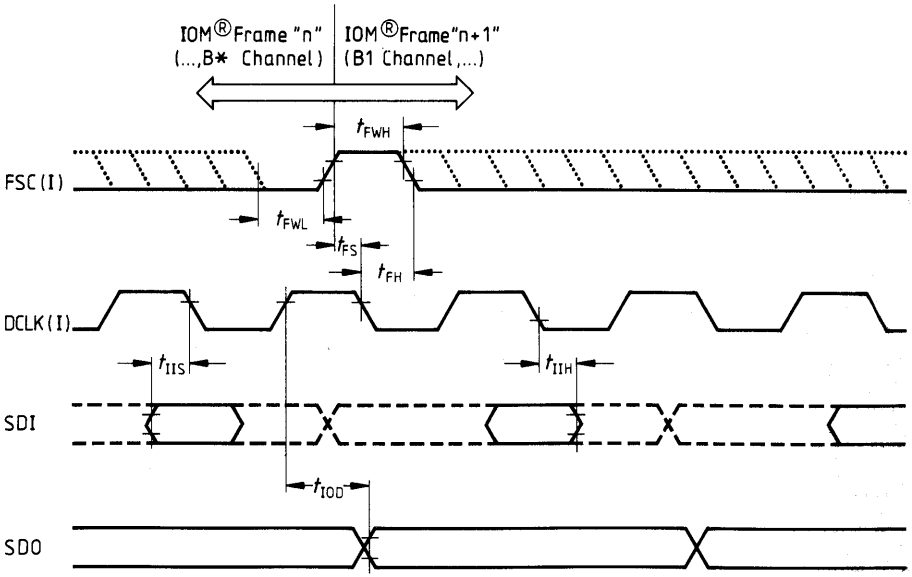
Normal mode

Master mode (TE)



Parameter	Symbol	Limit Values		Unit
		min.	max.	
Frame sync delay C_L = 100 pF	$t_{F\,D}$	−20	20	ns
IOM output data delay C_L = 100 pF	$t_{I\,OD}$		200	ns
IOM input data setup	$t_{I\,IS}$	20		ns
IOM input data hold	$t_{I\,IH}$	50		ns

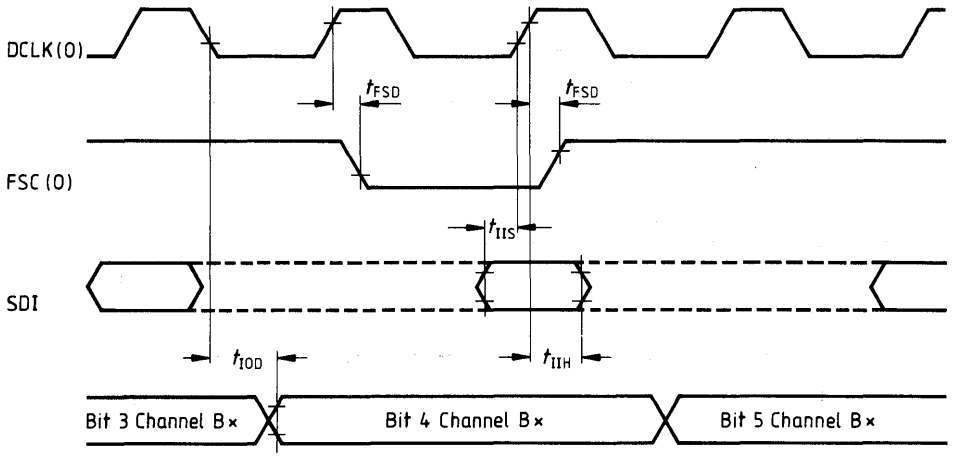
Slave Mode (NT, LT-S, LT-T)



Parameter	Symbol	Limit Values		Unit
		min.	max.	
Frame sync hold	t_{FH}	30		ns
Frame sync setup	t_{FS}	50		ns
Frame sync high	t_{FWH}	40		ns
Frame sync low	t_{FWL}	2150		ns
IOM output data delay	t_{IOD}		200	ns*)
IOM input data setup	t_{IIS}	20		ns
IOM input data hold	t_{IIH}	50		ns

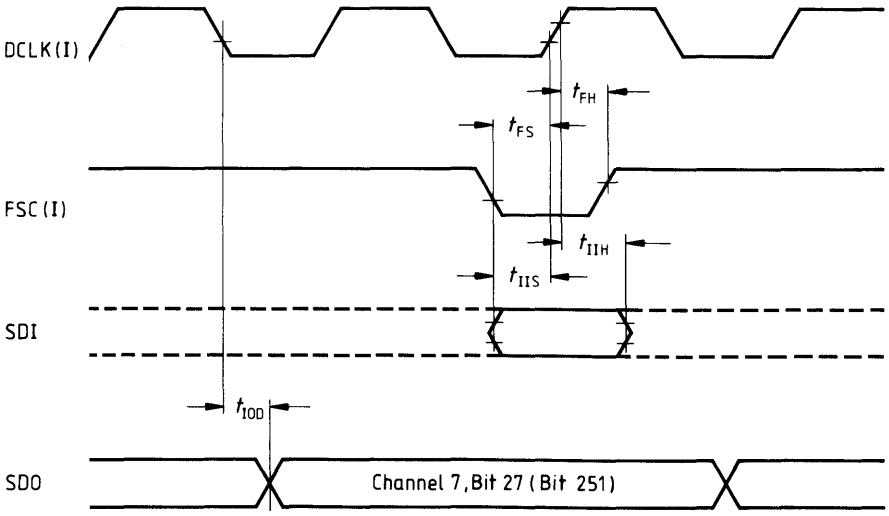
*) For push-pull output. For open drain output with integrated pull-up resistor, the maximum value is 900 ns.

Inverted Mode



Parameter	Symbol	Limit Values		Unit
		min.	max.	
Frame sync delay $C_L = 100$ pF	$t_{F\,SD}$	−20	20	ns
IOM output data delay $C_L = 100$ pF	$t_{I\,OD}$		200	ns
IOM input data setup	$t_{I\,IS}$	20		ns
IOM input data hold	$t_{I\,IH}$	50		ns

Inverted Mux Mode



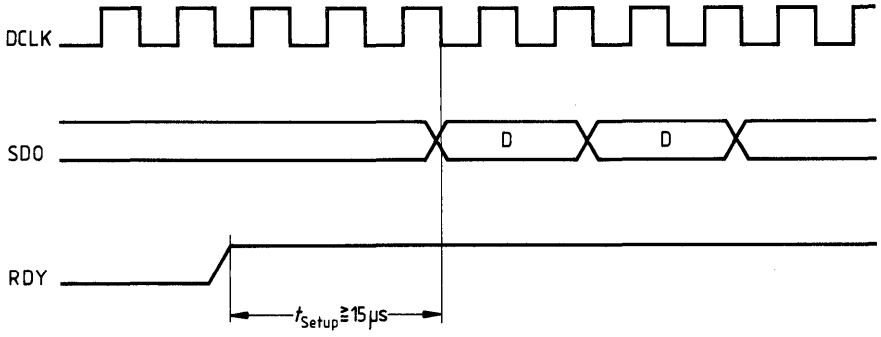
Parameter	Symbol	Limit Values		Unit
		min.	max.	
Frame sync hold	t_{FH}	50		ns
Frame sync setup	t_{FS}	20		ns
Frame sync high	t_{FWH}	124.8		µs
Frame sync low	t_{FWL}	70	200	ns
IOM output data delay $C_L = 150$ pF; $I_{OL} = 7$ mA	t_{IOD}		200	ns
IOM input data setup	t_{IIS}	20		ns
IOM output data hold	t_{IIH}	50		ns

Timing of Special Function Pins

$\overline{\text{RST}}$ Characteristics

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Length of active (low) state	t_{WL}	1		µs

RDY Characteristics

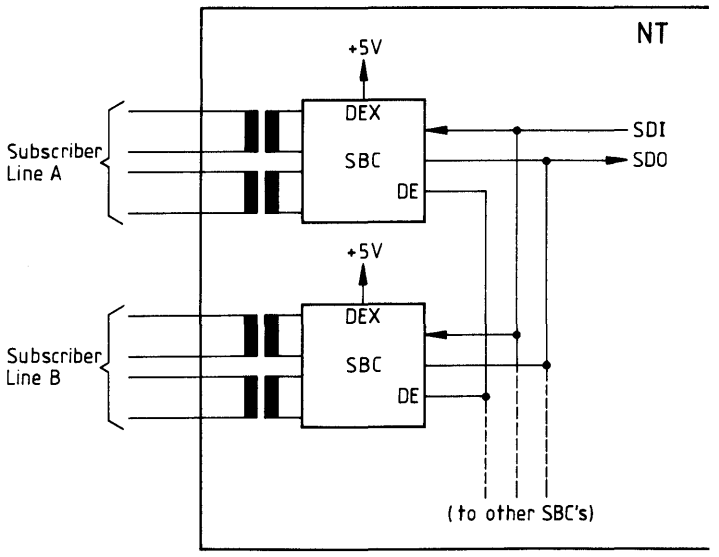


Parameter	Symbol	Limit Values		Unit
		min.	max.	
Length of low state	t_{WL}	360		µs
Length of high state	t_{WH}	60		µs

DE Characteristics

The form of the DE input/output (pin XO, NT mode) is given by **figure 20** for the case of two S interfaces having a minimum frame delay and a maximum frame delay, respectively.

Figure 20



The AC characteristics of DE output and input are shown in **figures 21** and **22** and **table 10.**

Figure 21
Timing of DE Output

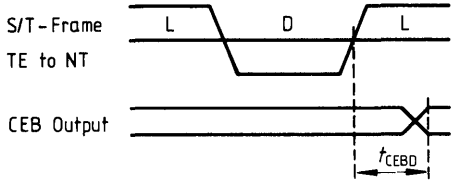


Figure 22
Timing of DE Input

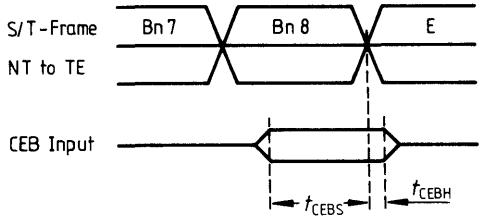


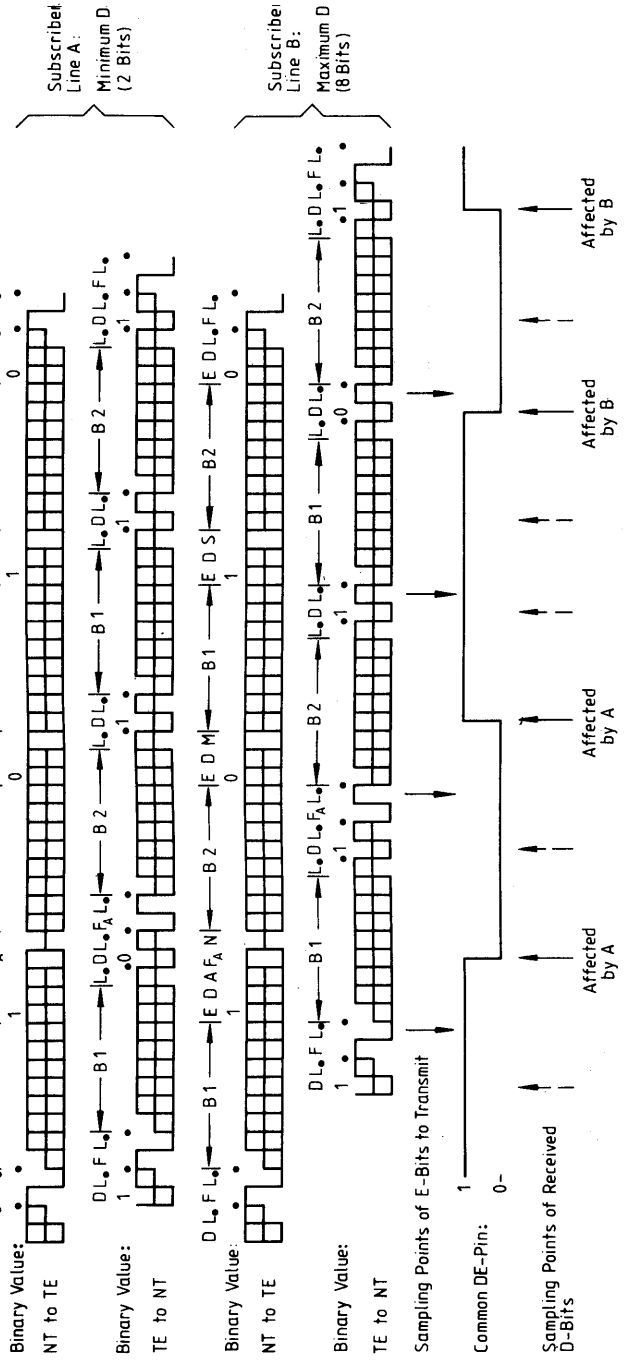
Table 10

Parameter	Symbol	Limit Values		Unit
		min.	max.	
DE delay $C_L = 100$ pF	t_{DED}		2	µs
DE setup	t_{DES}	5		µs
DE hold	t_{DEH}	0		µs

ECHO Characteristics

The timing of the ECHO output (pin X2, TE mode) is identical with that of output SDO: however, the signal is "1" everywhere except in bit positions 24 and 25 ("D"-bit positions) of IOM frame, where it is equal to the E-bits received from the S interface.

Figure 23
Timing of DE

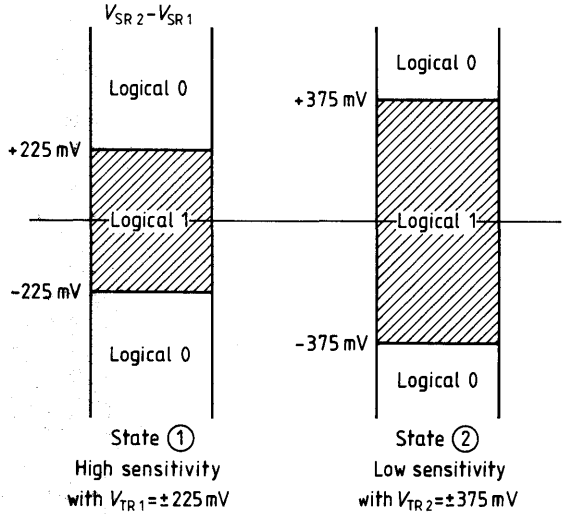


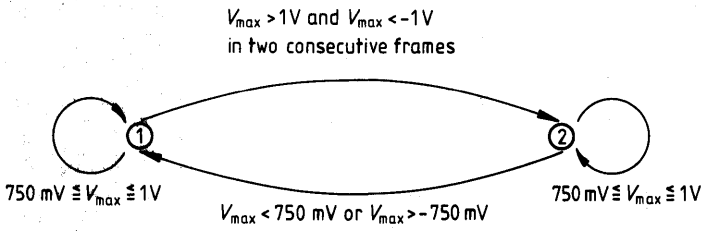
Adaptive Receiver Characteristics

The integrated receiver uses an adaptively switched threshold detector. The detector controls the switching of the receiver between two sensitivity levels. The hysteresis characteristics of the receiver are shown in **figure 23.**

Figure 24

Switching of the Receiver between High Sensitivity and Low Sensitivity





$V_{SR2}-V_{SR1}$ = Input voltage
V_{TR1}, V_{TR2} = Threshold voltages of the receiver threshold detector

V_{max} = maximum value of $V_{SR2}-V_{SR1}$ during one frame

SIEMENS

S/T Bus Interface Circuit Extended (SBCX) PEB 2081

Preliminary Data **CMOS IC**

Type	Ordering Code	Package
PEB 2081-N	Q67100-H6093	PL-CC-28 (SMD)
PEB 2081-P	Q67100-H6091	P-DIP-28
PEB 2081-P	planned	P-DIP-22

The S/T Bus Interface Circuit Extended (SBCX) PEB 2081 implements the four-wire S/T interface used to link voice/data ISDN terminals, network termination (Central Office and PBX applications), and PBX trunk lines to Central Office. Through selection of operating modes, the device may be employed in all types of applications involving an S/T interface. Two or more PEB 2081 SBCX can be used to build a point-to-point, passive bus, extended passive bus or star configuration.

The PEB 2081 SBCX provides the electrical and functional link between the analog S/T interface according to CCITT recommendation I.430 and T1D1 Basic User Network Interface Specification, respectively and the ISDN Oriented Modular (IOM®) interface Rev. 2.

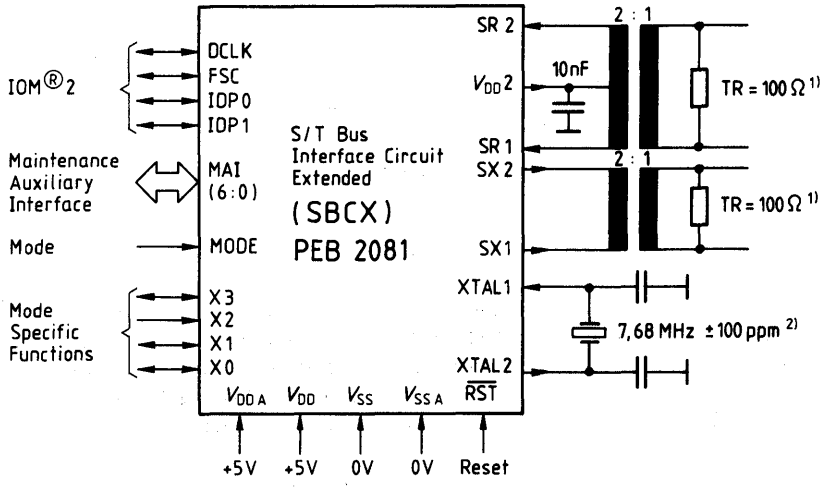
The PEB 2081 SBCX exceeds both the electrical and functional requirements of the S/T interface in order to provide high flexibility to the user with respect of S/T interface wiring configuration and implementation of layer-1 maintenance functions. By provision of some additional features at the IOM-2 interface the user is able to combine the SBCX with other IOM-2 devices in various configurations.

The PEB 2081 SBCX is a 28-pin CMOS device offered in both DIP and PL-CC packages It operates from a single 5 V supply and features a power-down state with very low power consumption.

Features

- Full duplex 2B + D S/T interface transceiver according to CCITT I.430
- Adaptive equalizer
- Receive timing recovery
- Built-in wake-up unit for activation from power-down state
- Conversion of the frame structure between the S/T interface and IOM-2 interface
- Activation and deactivation procedures according to CCITT I.430
- D-channel access control, also in trunk application
- Access to S and Q bits of S/T interface
- Automatic handling of S and Q bit messages
- Software controlled maintenance interface (i/o ports)
- Frame alignment with absorption of phase wander in NT2 network side applications
- Switching of test loops
- Several operating modes
- Advanced CMOS technology
- Low power consumption: standby less than 6 mW
  active max. 80 mW

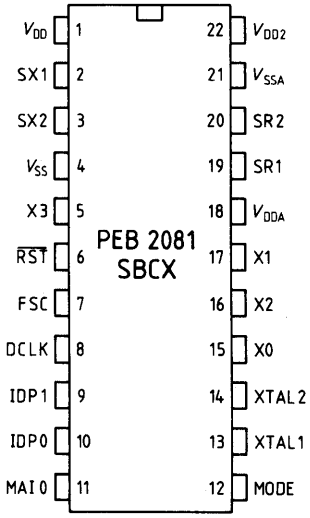
Logic Symbol



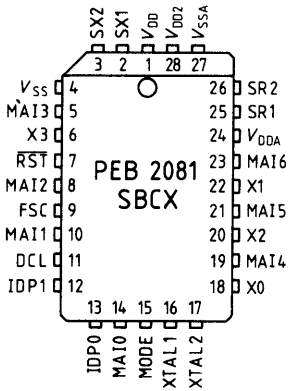
1) Terminating resistors only at the far end
2) For details of crystal **see figures 22 and 25**
3) 10 nF required only for A1 silicon.
Further versions will have a symmetrical receiver.

Pin Configurations
(top view)

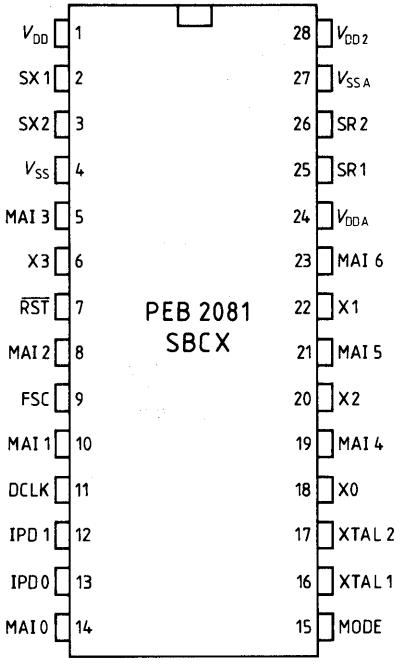
P-Dip-22



PL-CC-28



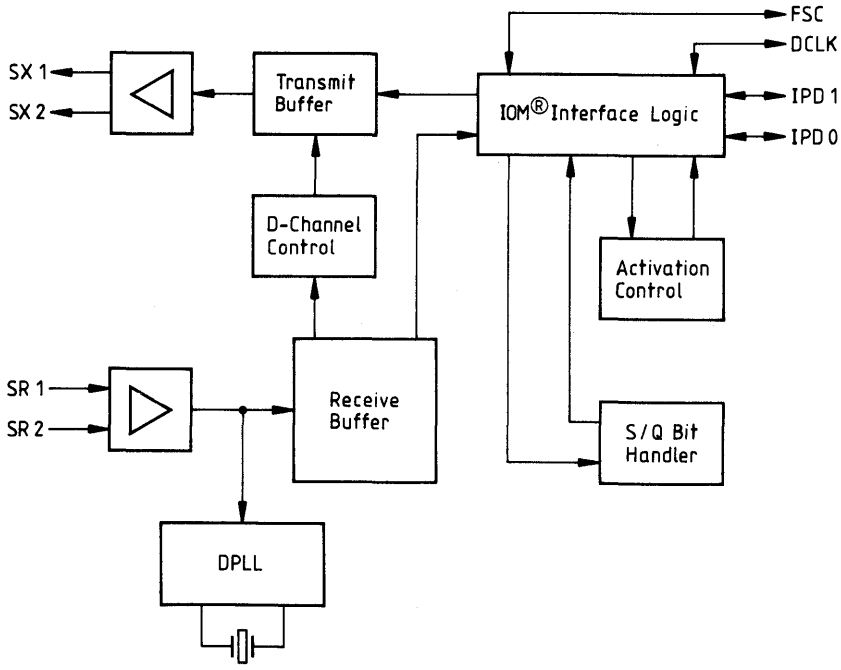
P-DIP-28



Pin Definitions and Functions

Pin No. P-DIP-28 PL-CC-28	Pin No. P-DIP-22	Symbol	Input (I) Output (O)	Function
2	2	SX1	O	Positive transmitter output
3	3	SX2	O	Negative transmitter output
13	10	IDP0	I/O	IOM Data Port 0
12	9	IDP1	I/O	IOM Data Port 1
11	8	DCLK	I/O	Data clock, IOM interface
9	7	FSC	I/O	Frame Sync, IOM interface
15	12	MODE	I	Setting of operating mode
6 20 22 18	5 16 17 15	X3 X2 X1 X0	I/O I/O I/O I/O	Functions dependant on the selected operation mode, **see chapter 2.**
23, 21, 19		MAI (6:4)	O	Maintenance output pins controlled by monitor channel
5, 8, 10, 14	11	MAI (3:0)	I	Maintenance input pins
16	13	XTAL1	I	Connection for external crystal, or input for external clock generator
17	14	XTAL2	O	Connection for external crystal, n.c. when external clock generator is used
25	19	SR1	I	Receiver, signal input
26	20	SR2	I	Receiver, signal input
28	22	V_{DD2}	O	2.5 V reference voltage output; 10 nF to V_{SS}
27	21	V_{SSA}	I	Analog ground
24	18	V_{DDA}	I	Analog power supply +5 V ± 5%
1	1	V_{DD}	I	Digital power supply +5 V ± 5%
4	4	V_{SS}	I	Digital ground
7	6	$\overline{RST}$	I	Reset, active low

Figure 1
Block Diagram



System Integration

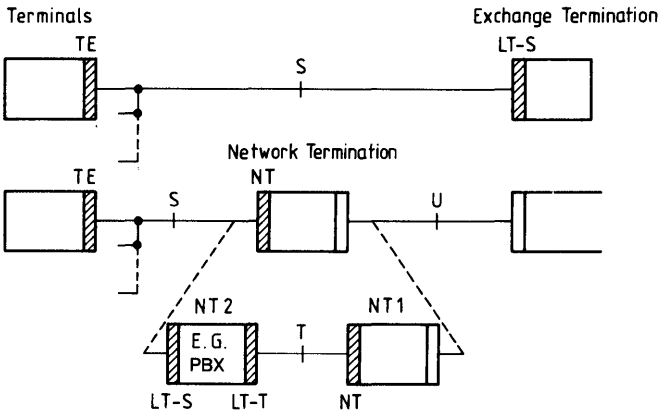
The PEB 2081 SBCX implements the four-wire S and T interfaces used in the ISDN basic access. By programming the corresponding operating mode it may be used at both ends of these interfaces.

The operating modes are:

ISDN terminals (TE)
ISDN network termination (NT)
ISDN subscriber line termination (LT-S)
ISDN trunk line termination (LT-T)
(PBX connection to Central Office).

The basic use of these modes is shown in **figure 2** where the usual nomenclature as defined by the CCITT for the basic access functional blocks and reference points, has been used.

Figure 2
Operating Modes



Terminals and Network Terminations

By adding IOM-2 compatible devices to the PEB 2081 SBCX different configurations are possible ranging from the standard TE and NT implementations shown in **figure 3** and **4** to more complex applications.

Figure 3
ISDN Voice/Data Terminal using the IOM-2 Architecture

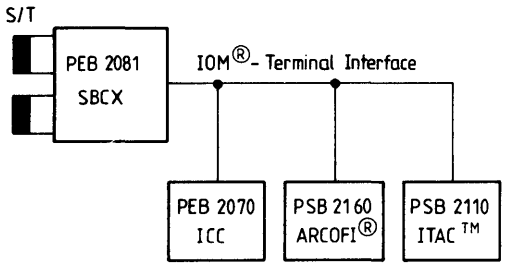
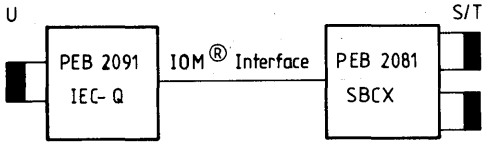
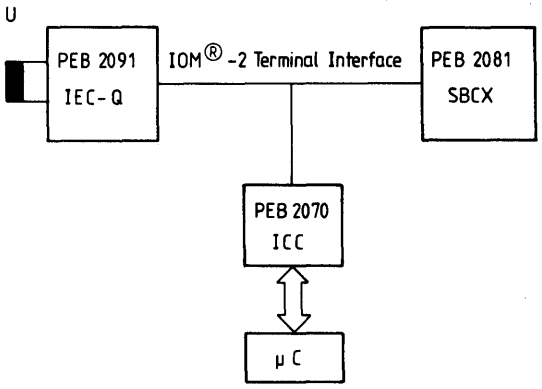


Figure 4
Network Termination with only two Devices



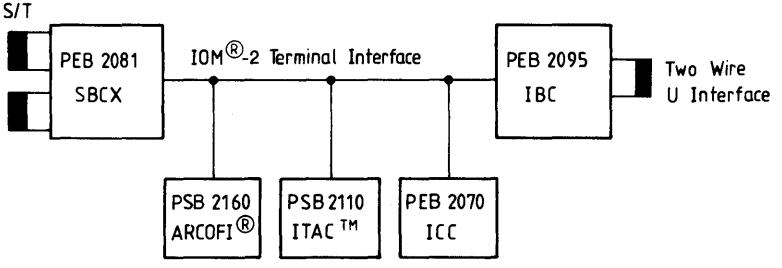
A more complex application is a microcontrolled NT using the PEB 2070 ICC to provide software controlled layer-1 maintenance functions **(figure 5)**. The U and S/T interface maintenance data is conveyed via the IOM interface's monitor channel to the PEB 2070 ICC.

Figure 5
The µC Controls all Layer-1 Maintenance Functions of the NT



More terminal functions can be added to the NT resulting in a U interface terminal with an S/T interface terminal (intelligent NT) **(figure 6)**. The functionality of such a configuration includes D-channel collision resolution in upstream direction and B channel switching functions for internal communications.

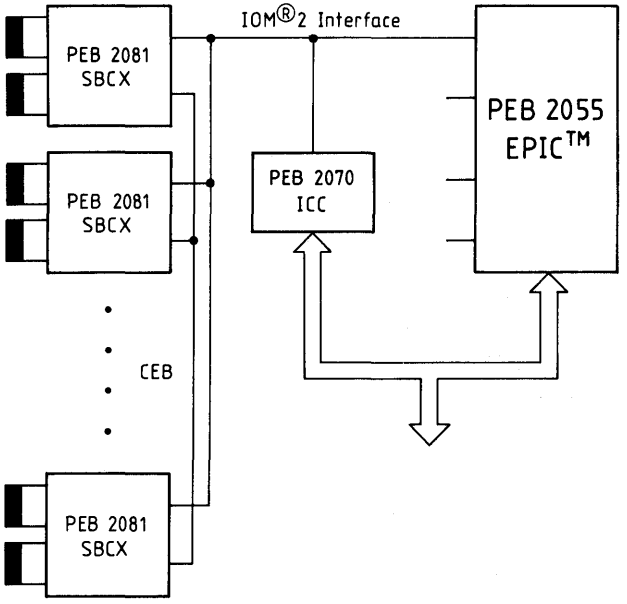
Figure 6
An Intelligent NT Provides Both Terminal (voice/data) and Network Terminating Functions (S/T interface)



Line Terminations

The standard implementation of an S/T interface line card includes one D-channel controller. per line. Due to the S/T interface's ECHO bit function this can be reduced to one D-channel controller per up to eight lines. The PEB 2081 SBCX supports this architecture by handling the ECHO bit externally as a common ECHO Bit (CEB) to all S/T interfaces (**figure 7**)

Figure 7
One LAP-D Controller is Sufficient for up to Eight S/T Interfaces.

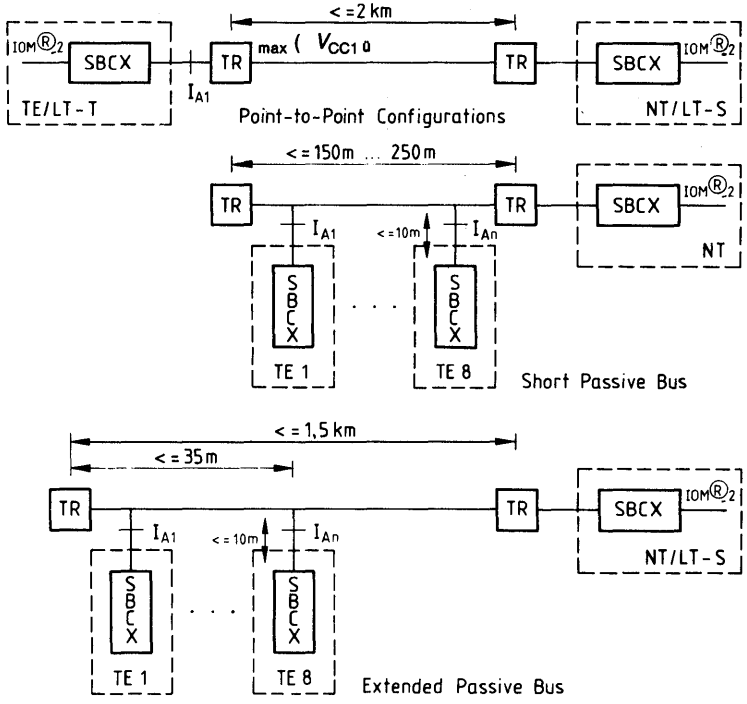


S/T Interface Configurations

The adaptive equalizer integrated in the receiver of the PEB 2081 SBCX exceeds the electrical requirements of the S/T interface. An overview of the different wiring configurations is given in **figure 8.**

Since maximum attenuation of the line is not the limiting factor, the maximum length of a point-to-point configuration depends on the round trip delay. For special applications it is possible to exceed this limitation by switching the upstream D channel to a transparent mode. Obviously, the extended passive bus configuration benefits from the enhanced receiver characteristic resulting by increasing the loop length.

Figure 8
S/T Interfacing Wiring Configurations
(N.B.: "TR" stands for terminating resistor of value 100 Ω).



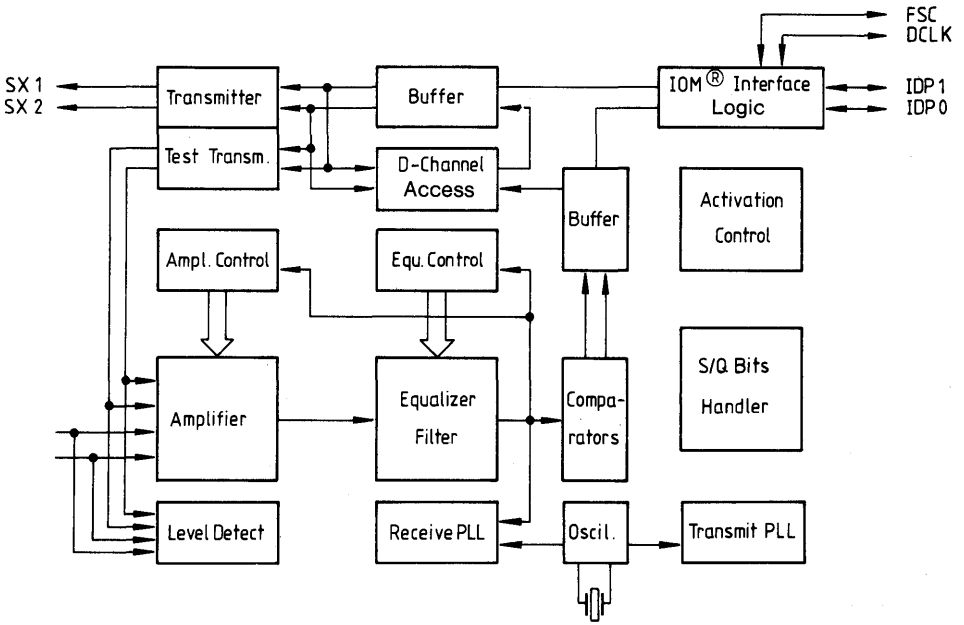
Functional Description

The PEB 2081 SBCX performs the layer-1 functions for the S/T interface of the ISDN basic access.

SBCX Device Architecture and General Functions

The SBCX performs the layer-1 functions of the S/T interface according to CCITT recommendation I.430 and T 1D1 Basic User Network Interface Specification, respectively. It can be used at all ends of the S/T interface. **Figure 9** depicts the device architecture.

Figure 9
SBCX Device Architecture



The Common Functions for all Operating Modes

- Line transceiver functions for the S/T interface according to the electrical specifications of CCITT I.430;
- Conversion of the frame structure between the IOM interface and S/T interface;
- Conversion from/to binary to/from pseudo-ternary code.
- Access to S and Q bits
- Handling of S and Q channel messages
- Level detect.

Mode Specific Functions

- Receive timing recovery for point-to-point, passive bus and extended passive bus configuration.
- S/T timing generation using IOM timing synchronous to system, or vice versa;
- D-channel access control and priority handling;
- D-channel echo bit generation by handling of the common echo bit.
- Activation/deactivation procedures, triggered by primitives received over the IOM interface or by INFO's received from the line;
- Frame alignment according to CCITT Q.503;
- Execution of test loops.

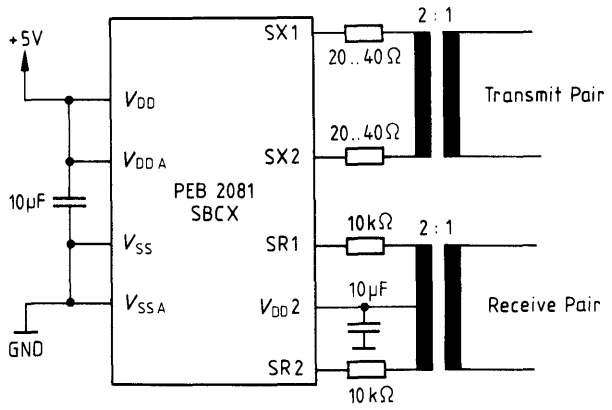
Analog Functions

For both receive and transmit direction, a 2:1 transformer is used to connect the PEB 2081 SBCX to the 4 wire S/T interface. The pseudo-ternary pulse shaping which meets the I.430 pulse templates, is achieved with the integrated transmitter.

The integrated adaptive equalizer is designed to cope with all wiring configuration of the S/T interface, point-to-point, passive bus, and extended passive bus. The maximum allowable line attenuation is increased to more than 20 dB, with the corresponding distortion equalized, and out-of-band noise suppressed.

The level detect block monitors the receive line and therefore initiates switching into power down or power up state. **Figure 10** depicts the analog connections of the PEB 2081 SBCX.

Figure 10
Connection of the Line Transformers and Power Supply to the SBCX



Digital Functions

DPLL circuitry working with a frequency of 7.68 MHz ± 100 ppm in S/T interface master modes generates the 192-kHz-line clock from the reference clock delivered by the network (FSC: 8 kHz) and in S/T interface slave modes extracts the 192-kHz line clock from the receive data stream.

The 7.68 MHz clock may be generated with the use of an external crystal between pins XTAL1 and XTAL2, or by an external oscillator, in which case XTAL2 is not connected.

The D-channel access procedure according to CCITT I.430, including priority management, is fully implemented in the SBCX. When used as an S/T interface master, the device generates the E bits necessary for D-channel collision detection. The received D-bits are provided at pin CEB (common echo bit) for a wired-AND connected NT star configuration.

The buffer memory serves to adapt the different bit rates of the S/T interface and the IOM interface. In addition, in trunk line applications it absorbs the possible deviation between two system clocks, according to CCITT Q.503 (slip detection).

In all applications, the PEB 2081 SBCX gives access to the S and Q bits via the monitor channel. According to its specific S/Q mode, it handles the S and Q channel messages autonomously, i.e. without the aid of a µC (e.g. in NT).

Table 1
Operating Modes and Functions of Mode Specific Pins of the SBCX.

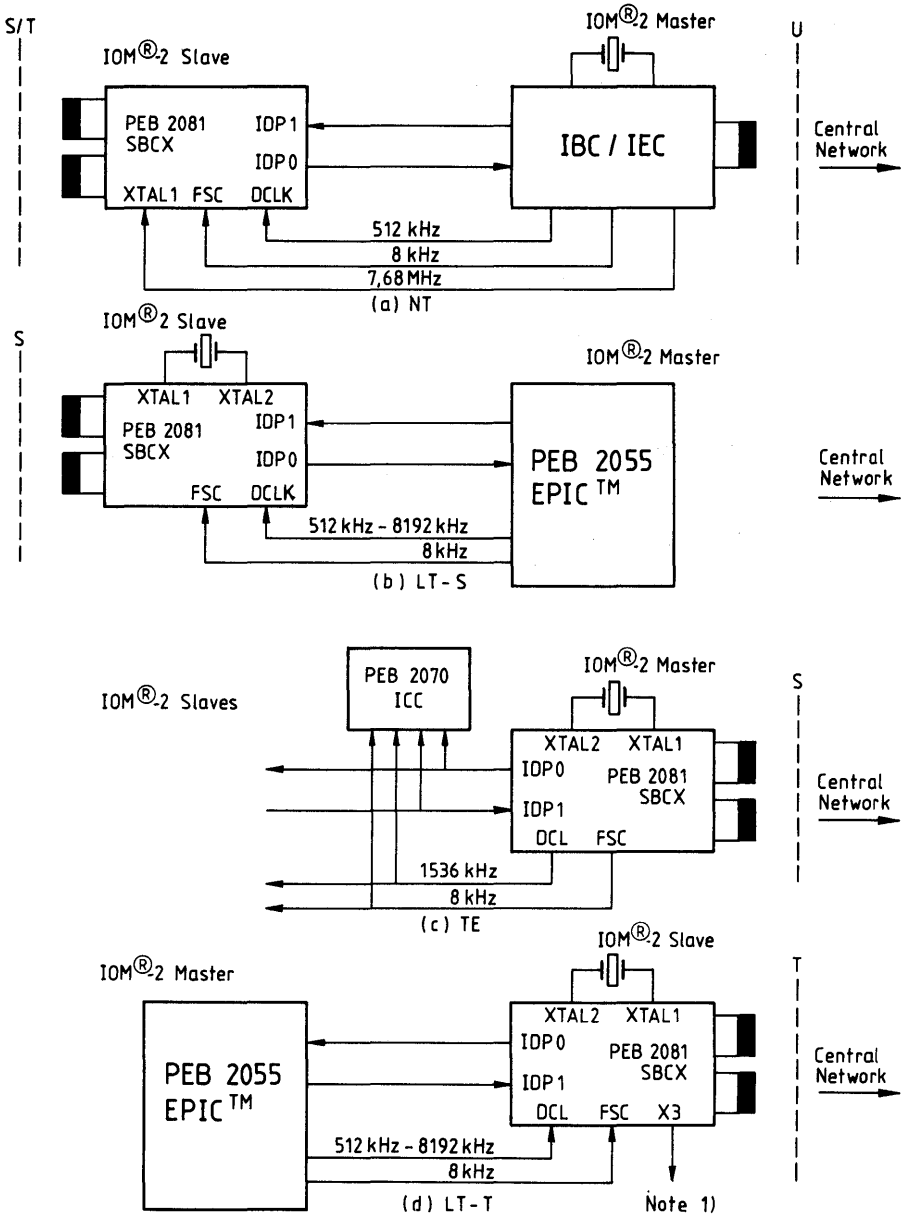
	Application			
	TE	**LT-T**	**NT**	**LT-S**
MODE	i: V_{SS}	i: V_{DD}	i: V_{SS}	i: V_{DD}
DCLK	o: 1536 kHz[1)]	i: 512 kHz to 8192 kHz	i: 512 kHz to 8192 kHz	i: 512 kHz to 8192 kHz
FSC	o: 8 kHz[1)]	i: 8 kHz	i: 8 kHz	i: 8 kHz
X3	o: 768 kHz[1)]	o: 1536 kHz[1)]	i/o: CEB	i/o: CEB
X2	i: V_{SS}	i: ICN2	i: V_{DD}	i: ICN2
X1	i: V_{SS}	i: ICN1	i: V_{SS}	i: ICN1
X0	o: PCK	i: ICN0	i: BUS	i: ICN0

[1)] synchronized to S/T interface
i: input o: output

PCLK Power Converter Clock
BUS Bus configuration specified
CEB Common Echo Bit in NT1 star

Note: Differentiation between LT-T mode and LT-S mode is done by software programming of data bit 0 of the configuration register.

Figure 11
Clocking of the SBCX in Different Operation Modes



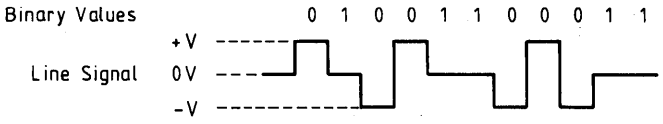
Note 1: Reference clock (1536 kHz), may be used to drive NT2 clock generator.

Interfaces

S/T Interface

According to CCITT recommendation I.430, pseudo-ternary encoding with 100% pulse width is used on the S/T interface. A logical 1 corresponds to a high impedance level (no current), whereas logical 0's are encoded as alternating positive and negative pulses. An example is shown in **figure 12.**

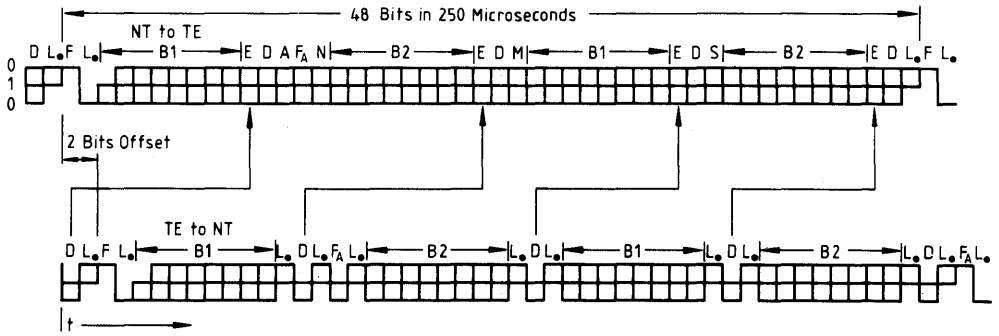
Figure 12
S/T Interface Line Code



One S/T frame consists of 48 bits, at a nominal bit rate of 192 kbit/s. Thus each frame carries two octets of B1, two octets of B2, and four D-bits, according to the B1 + B2 + D structure defined for the ISDN basic access (total useful data rate: 144 kbit/s). Frame begin is marked using a code violation (no mark inversion). The frame structures (from network to subscriber, and subscriber to network) are shown in **figure 13.**

A multi-frame is realized by use of F_A, N, and M bits in the NT to TE direction. **Table 2** shows the S and Q bit positions within the multiframe.

Figure 13
Frame Structure at Reference Points S and T (CCITT I.430)



F = Framing Bit
L = DC Balancing Bit
D = D-Channel Bit
E = D-Echo-Channel Bit
F = Auxiliary Framing Bit or Q-Bit
N = Bit Set to a Binary Value $N = \overline{F_A}$

B1 = Bit within B-Channel 1
B2 = Bit within B-Channel 2
A = Bit Used for Activation
S = S-Channel Bit
M = Multiframing Bit

Note: Dots Demarcate those Parts of the Frame that are Independently DC-Balanced.

Table 2
S and Q Bit Position Identification and Multiframe Structure

Frame Number	NT-to-TE F_A Bit Position	NT-to-TE M Bit	NT-to-TE S Bit	TE-to-NT F_A Bit Position
1	ONE	ONE	SC11	Q1
2	ZERO	ZERO	SC21	ZERO
3	ZERO	ZERO	SC31	ZERO
4	ZERO	ZERO	SC41	ZERO
5	ZERO	ZERO	SC51	ZERO
6	ONE	ZERO	SC12	Q2
7	ZERO	ZERO	SC22	ZERO
8	ZERO	ZERO	SC32	ZERO
9	ZERO	ZERO	SC42	ZERO
10	ZERO	ZERO	SC52	ZERO
11	ONE	ZERO	SC13	Q3
12	ZERO	ZERO	SC23	ZERO
13	ZERO	ZERO	SC33	ZERO
14	ZERO	ZERO	SC43	ZERO
15	ZERO	ZERO	SC53	ZERO
16	ONE	ZERO	SC14	Q4
17	ZERO	ZERO	SC24	ZERO
18	ZERO	ZERO	SC34	ZERO
19	ZERO	ZERO	SC44	ZERO
20	ZERO	ZERO	SC54	ZERO
1	ONE	ONE	SC11	Q1
2	ZERO	ZERO	SC12	ZERO
etc.				

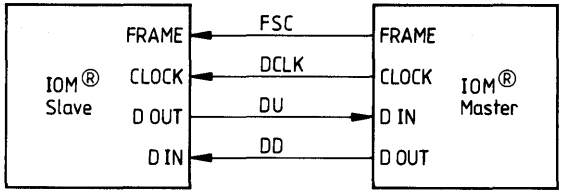
Digital Interface

The PEB 2081 SBCX is provided with a digital (IOM-2) interface, for communication with other ISDN devices to realize OSI layer-1 functions (such as a U transceiver) or upper layer functions (such as ICC, ARCOFI, ITAC and EPIC).

The IOM interface is a four-wire serial interface with: a bit clock, a frame clock, and two data lines per direction **(figure 14)**.

The ISDN user data rate of 144 kbit/s (B1 + B2 + D) is transmitted transparently in both directions over the interface. In addition, it is necessary to interchange control information for activation/deactivation of OSI layer-1 and maintenance functions. This information is transferred using time division multiplexing of the 125 µs S/T interface frame.

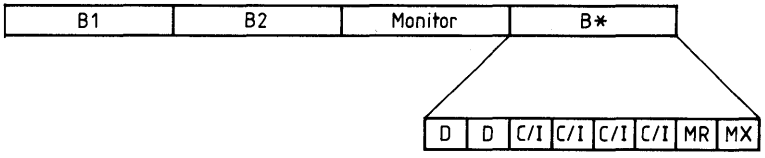
Figure 14
IOM Interface Signals



FSC: Frame synchronization
DCLK: Data clock
DU: Data upstream
DD: Data downstream

The basic frame consists of a total of 32 bits, or four octets: B1 + B2 + D (18 bits) plus 14 overhead bits for maintenance of monitor and control information. The data in both directions is synchronous and in phase **(figure 15)**.

Figure 15
IOM Frame Structure



1st octet B1: B channel (64 kbit/s)
2nd octet B2: B channel (64 kbit/s)
3rd octet: Monitor channel (64 kbit/s), most significant bit first
4th octet B*: 2 bit D channel (16 kbit/s)
4 bit C/I channel
MR, MX bit: used for monitor channel control.

The C/I channel is used for communication between the PEB 2081 SBCX and a processor via a layer-2 device, to control and monitor layer-1 functions. The codes originating from layer-2 devices are called "commands", those from the PEB 2081 SBCX are called "indications". For a list of the C/I codes and their use, refer to the SBCX Tech. Manual.

The monitor channel is used to convey S and Q maintenance bit information and message oriented local functions such as software programming or access to internal registers (e.g. MAI-status).

The PEB 2081 SBCX has implemented the monitor channel protocol according to the IOM-2 specification. It also performs a last look function on the monitor byte and, in transmit direction, a monitor channel access procedure for bus configurations.

For the transfer of S and Q channel information, the PEB 2081 SBCX will autonomously start the monitor channel procedure. Device internal registers are only transferred as a result of a "read" command.

Nominal bit rate of data (IDP1 and IDP0):

256 kbit/sec ...4096 kbit/sec

Nominal frequency of DCLK:

512 kHz ...8192 kHz

Nominal frequency of FSC: 8 kHz

For the exact electrical definition **see page 419** and the IOM-2 interface specification.

Figure 16
Timing of Data and Clocks of the IOM Interface in the 512-kHz-Mode

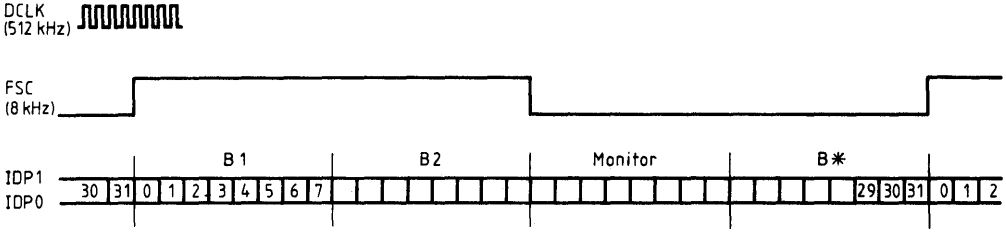


Figure 17
Timing of Data and Clocks of the IOM Interface in the 4096-kHz-Mode

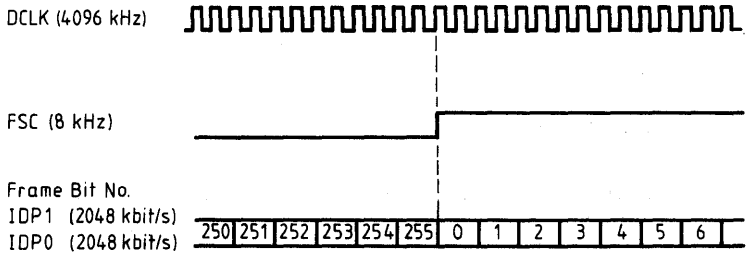
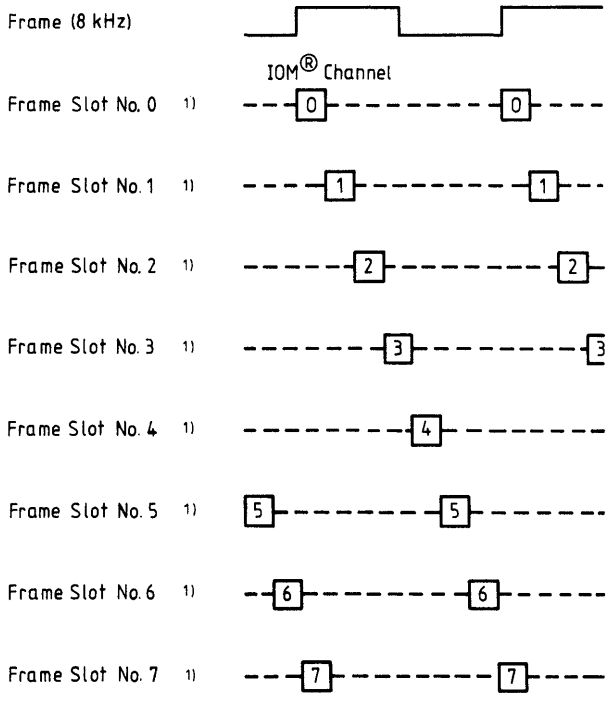


Table 3
Allocation of IOM Channels

IOM Channel No.	ICN2	ICN1	ICN0	Bit No.
0	0	0	0	0... 31
1	0	0	1	32... 63
2	0	1	0	64... 95
3	0	1	1	96...127
4	1	0	0	128...159
5	1	0	1	160...191
6	1	1	0	192...223
7	1	1	1	224...255

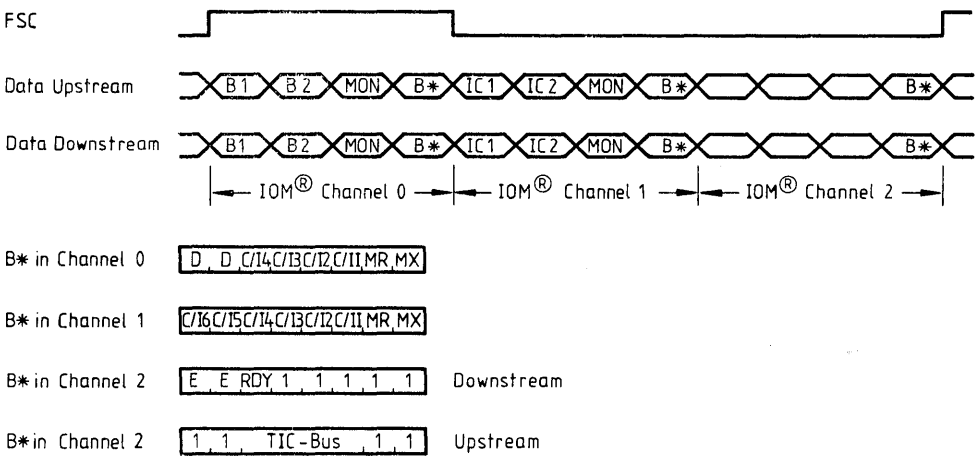
Figure 18
Position of IOM Channels as a Function of Time-Slot Allocation in 4096-kHz-Mode



1) IDP1 (2048 kbit/s)
IDP0 (2048 kbit/s)

In TE mode, the data clock DCLK has a frequency of 1.536 MHz. As a consequence, the IOM interface provides three channels. The PEB 2081 SBCX only uses IOM channel 0, and for D-channel access control, the C/I field of IOM channel 2. The remaining two IOM channels are for the use of other devices within the TE **(figure 19)**.

Figure 19
Definition of the IOM-2 Terminal Interface



Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Ambient temperature under bias	T_A	0 to 70	°C
Storage temperature	T_{stg}	−65 to 125	°C
Voltage on any pin with respect to ground	V_S	−0.4 to V_{DD} +0.4	V
Power dissipation	P_D	1	W

DC Characteristics

$T_A = 0$ to 70 °C; $V_{DD} = 5\ V \pm 5\%$; $V_{SS} = 0\ V$

All pins except SX1,2; SR1,2; XTAL1,2; V_{DD2}

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit	Test Conditions
L-input voltage	V_{IL}	−0.4	0.8	V	
H-input voltage	V_{IH}	2.0	V_{DD} +0.4	V	
L-output voltage (IDP1,0 only)	V_{OL} V_{OL1}		0.45 0.45	V V	$I_{OL} = 2$ mA $I_{OL} = 7$ mA
H-output voltage H-output voltage	V_{OH} V_{OH}	2.5 V_{DD} −5		V V	$I_{OH} = -400$ µA $I_{OH} = -100$ µA
Power supply current: operational	I_{CC}		12	mA	$V_{DD} = 5$ V, inputs at V_{SS}/V_{DD}, no output loads
Power supply current: power down			0.8	mA	
Input leakage current	I_{LI}		10	mA	$0\ V \le V_{IN} \le V_{DD}$
Output leakage current	I_{IO}				$0\ V \le V_{OUT} \le V_{DD}$

DC Characteristics

Pin SX1; SX2

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit	Test Conditions
Absolute value of output pulse amplitude ($V_{SX2}-V_{SX1}$)	V_X V_X	2.03 2.10	2.31 2.39	V V	$R_L = 50\ \Omega$ [1] $R_L = 400\ \Omega$ [1]
Transmitter output current	I_X	7.5	13.4	mA	$R_L = 5.6\ \Omega$ [1]
Transmitter output impedance	Z_X	10 80		kΩ kΩ	inactive or during binary one ($V_{DD} = 0...5$ V) during binary zero [2] $R_L = 50\ \Omega$

Pin VDD 2

Receiver output voltage	V_R	2.4	2.6	V	$I_O \leq 5\ \mu A$

Pin 5 R; SR 2

Receiver input impedance	Z_R	10 100		kΩ Ω	$V_{DD} = 5$ V $V_{DD} = 0$ V

Pin XTAL1

H-input voltage L-input voltage	V_{HI} V_{IL}	3.5 −0.4	V_{DD} +0.4 1.5	V V	

Pin XTAL2

H-output voltage	V_{OH}	4.5		V	$I_{OH} = 5$ mA, $C_L \leq 50$ pF
L-output voltage	V_{OL}		0.4	V	$I_{OH} = 5$ mA, $C_L \leq 50$ pF

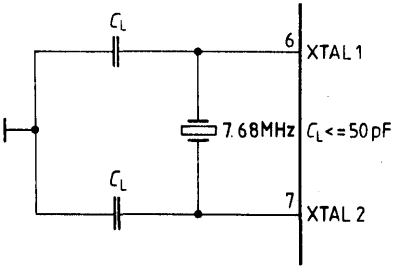
Notes: 1) Due to the transformers, the load resistance as seen by the circuit is four times R_L.
2) 80...100 Ω external resistance required

Capacitances

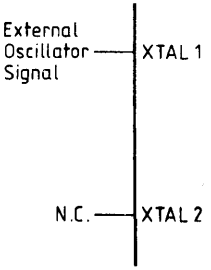
$T_A = 25\,°C$, $V_{DD} = 5\,V \pm 5\%$, $V_{SS} = 0\,V$
All pins except SX1,2

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Pin capacitance			7	pF
SX1,2				
Output capacitance against V_{SS}	C_O		10	pF
XTAL1,2				
Load capacitance	C_D		50	pF

Recommended Oscillator Circuits



Crystal Oscillator Mode



Driving from External Source

Clock Signals of the SBCX. Duty Ratios are Indicated High: Low

	Operating Mode			
	TE	**LT-T**	**NT**	**LT-S**
DCLK	o: 1.536 MHz 3:2	i: 512 kHz to 6172 kHz	i: 512 kHz to 6172 kHz	i: 512 kHz to 6172 kHz
FSC	o: 8 kHz 1:2	i: 8 kHz	i: 8 kHz	i: 8 kHz
X3	o: 768 kHz 1:1	o: 1536 MHz 3:2		
X0	o: 32 kHz/16 kHz 1:1			

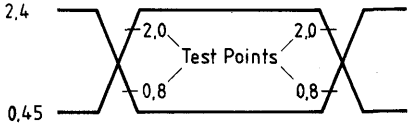
Input and Output Pin Configurations

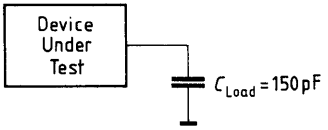
IDP (1:0) are open drain outputs.
CEB is an open drain output/input.
All other output pins are push/pull outputs.

AC Characteristics

$T_A = 0$ to 70 °C, $V_{DD} = 5\ V \pm 5\%$

AC testing: inputs are driven at 2.4 V for a logic "1" and 0.45 V for a logic "0". Timing measurements are made at 2.0 V for a logic "1" and at 0.8 V for a logic "0".





Jitter

In TE mode, the timing extraction jitter of the PEB 2081 SBCX conforms to CCITT Recommendation I.430 (−7% to +7% of the S/T-interface bit period).

In the NT and LT-S applications, the clock input FSC is used as reference clock to provide the 192-kHz-clock for the S/T interface. In the case of a plesiochronous 7.68-MHz-clock generated by an oscillator, the clock FSC should have a jitter of less than 100 ns peak-to-peak. (In the case of a zero input jitter on FSC, the PEB 2081 SBCX generates 130 ns "self-jitter" on the S/T interface.)

In the case of a synchronous 7.68-MHz-clock (input XTAL1), the PEB 2081 SBCX transfers the input jitter of XTAL1 and FSC to the S/T interface. The maximum jitter of the NT/LT-S output is limited to 260 ns peak-to-peak (CCITT I.430).

Clock Timing

The clocks in the different operating modes are summarized in **table 4**, with duty ratios. The 1.536-MHz-clock is phase-locked to the receive S signal, and is derived using the internal DPLL and the 7.68 MHz ± 100 ppm crystal (TE and LT-T).

As a consequence of this DPLL tracking, the high state of CP may be either reduced or extended by one 7.68-MHz-period (duty ratio 2:2 or 4:2 instead of 3:2). Since X3 and FSC are derived from DCLK (TE mode), the high state or the low state may likewise be reduced or extended by the same amount.

Figure 20
Definition of Clock Period and Width

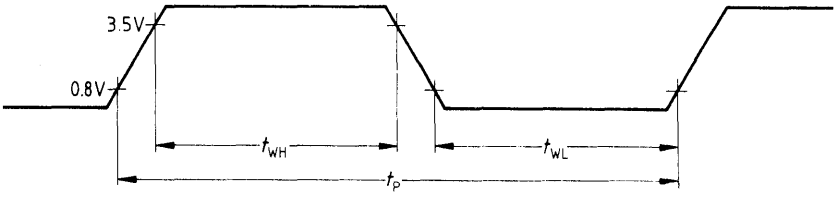


Table 4 to 8 give the timing characteristics of the clocks

Table 4
XTAL1,2

Parameter	Symbol	Limit Values		Unit
		min.	max.	
High phase of crystal/clock	t_{WH}	20		ns
Low phase of crystal/clock	t_{WL}	20		ns
Clock period	t_p	130.08	130.34	ns

Table 5
DCLK

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
(TE) 1.536 MHz	t_{PO}	520	651	782	ns	OSC ± 100 ppm
(TE) 1.536 MHz	t_{WHO}	240	391	541	ns	OSC ± 100 ppm
(TE) 1.536 MHz	t_{WLO}	240	260	281	ns	OSC ± 100 ppm
(NT, LT-S, LT-T)	t_{WHI}	90			ns	
(NT, LT-S, LT-T)	t_{WLI}	90			ns	

Table 6

X3

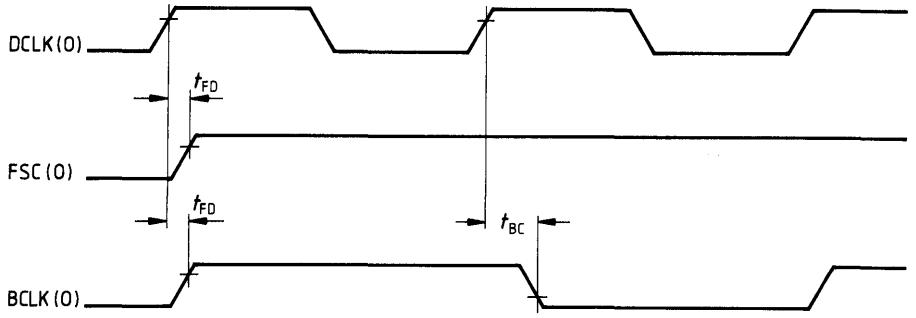
(LT-T) 1536 kHz	t_{PO}	520	651	782	ns	OSC ± 100 ppm
(LT-T) 1536 kHz	t_{WHO}	240	391	541	ns	OSC ± 100 ppm
(LT-T) 1536 kHz	t_{WLO}	240	260	281	ns	OSC ± 100 ppm
(TE) 768 kHz	t_{PO}	1150	1302	1450	ns	OSC ± 100 ppm
(TE) 768 kHz	t_{WHO}	520	651	782	ns	OSC ± 100 ppm
(TE) 768 kHz	t_{WLO}	520	651	782	ns	OSC ± 100 ppm

Table 7

X0

(TE) 32 kHz	t_{PO}	31.1	31.25	31.4	µs	OSC ± 100 ppm
(TE) 32 kHz	t_{WHO}	15.4	15.6	15.8	µs	OSC ± 100 ppm
(TE) 32 kHz	t_{WLO}	15.4	15.6	15.8	µs	OSC ± 100 ppm

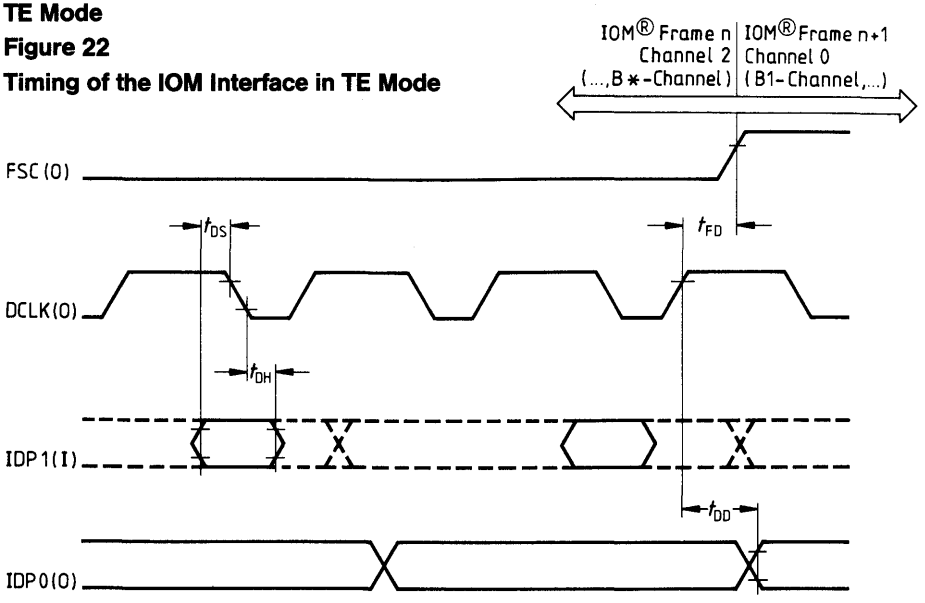
Figure 21
DCLK, BCLK and FSC Relationship in TE Mode



Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Delay DCLK – BCLK	t_{BD}	–200		50	ns	C_L = 150 pF
Delay DCLK – FSC	t_{FD}	–200		50	ns	C_L = 150 pF

IOM Interface

TE Mode
Figure 22
Timing of the IOM Interface in TE Mode

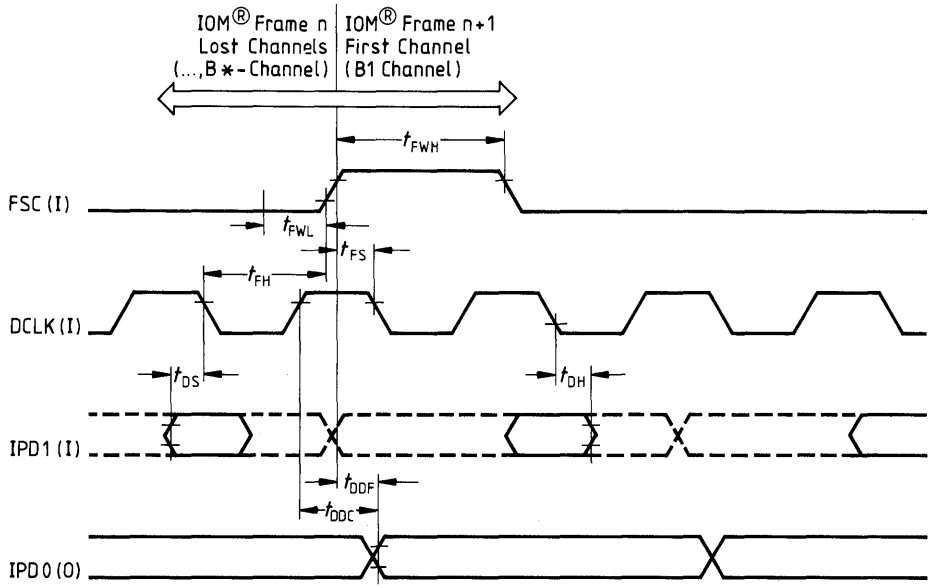


IOM Interface in TE Mode

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Frame sync delay	t_{FD}	−200		−50	ns	C_L = 150 pF
Data delay	t_{DD}			100	ns	C_L = 150 pF
Data setup	t_{DS}	20			ns	
Data hold	t_{DH}	50			ns	

TE Mode
NT, LT-S, and LT-T Modes

Figure 23
Timing of the IOM Interface in NT Mode



IOM Interface in NT Mode

Parameter	Symbol	Limit values			Unit
		min.	typ.	max.	
Frame sync hold	t_{FH}	30			ns
Frame sync setup	t_{FS}	70			ns
Frame sync high	t_{FWH}	130			ns
Frame sync	t_{FWL}	t_{DCL}			
Data delay to clock	t_{DDC}			100	ns
Data delay to frame	t_{DDF}			150	ns
Data setup	t_{DS}	20			ns
Data hold	t_{DH}	50			ns

Timing of Special Function Pins

$\overline{\text{RST}}$ Characteristics

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Length of active (low) state	t_{WL}	1		µs

CEB Characteristics

The form of the CEB input/output (pin X3, NT and LT-S mode) is given by **figure 27** for the case of two S/T interfaces having a minimum loop delay and a maximum loop delay, respectively.

Figure 24
Star Configuration in NT and LT-S Mode

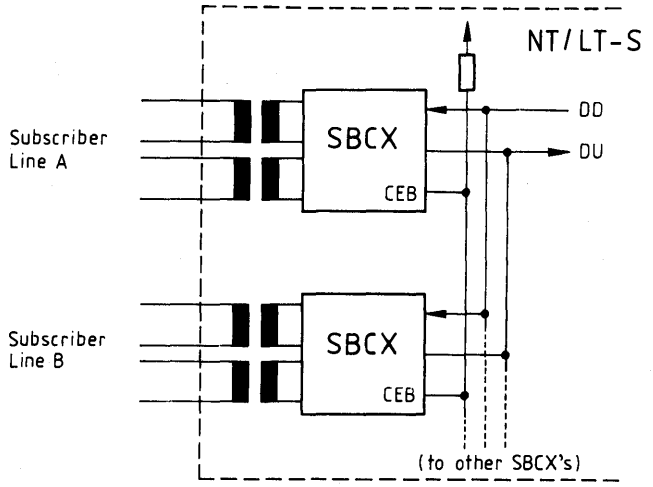


Figure 25
Timing of CEB Output

The AC Characteristics of CEB Output and Input are shown in Figures 5.8-9 and Table 11.

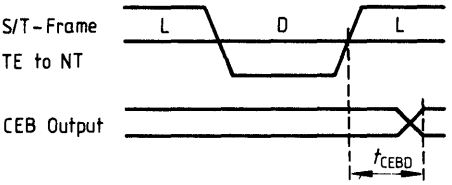


Figure 26
Timing of CEB Input

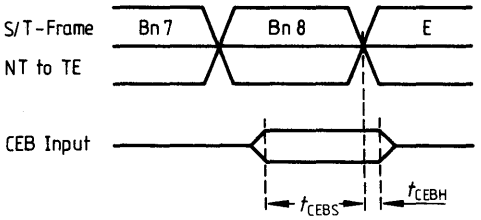
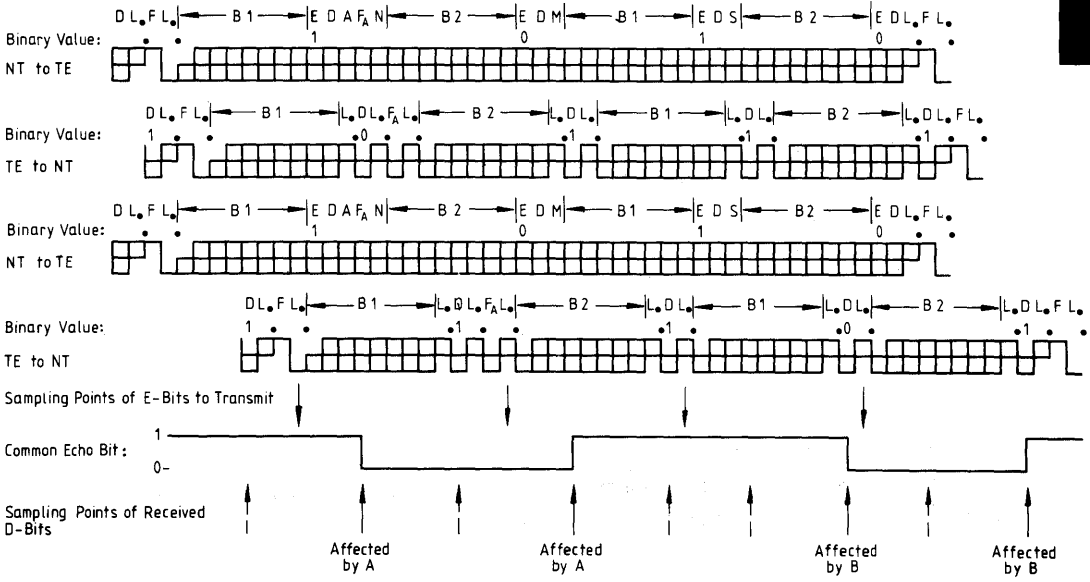


Table 8

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
CEB delay	t_{CEBD}	3		5	µs	$C_L = 100$ pF
CEB setup	t_{CEBS}	5			µs	
CEB hold	t_{CEBH}	0			µs	

Figure 27
Timing of CEB



Condition: All Transmit Frames NT→TE are in Phase.

S/T Interface Transformer

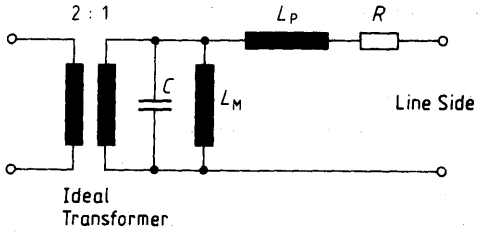
The PEB 2081 SBCX is connected to the 4 wire S/T interface by use of two transformers. Both sides of the transformers must be center tapped.

Transformer Model

The model parameters of the transformer are defined below (all measurements at 10 kHz):

primary to secondary transformer ratio:	1:2 ± 1%
primary total DC resistance:	$R \leq 10\ \Omega$
primary inductance:	$L_M > 20$ mH
primary inductance with secondary short-circuited:	$L_P < 20\ \mu H$
primary capacitance with secondary open:	$C < 40$ pF

Figure 28
Transformer Model



Transmitter Characteristics

The DC characteristics of the transmitter are given in **page 419 and 420.** Rising and falling edges of pulses on 50 Ω load are typically 300 ns.

SIEMENS

ISDN Echo-Cancellation Circuit (IEC-T)

PEB 20901
PEB 20902

Preliminary Data

CMOS IC

Type	Ordering Code	Package
PEB 20901-C	Q67100-H8679	C-DIP-40
PEB 20901-N	Q67100-H6113	PL-CC-44 (SMD)
PEB 20901-P	Q67100-H8678	P-DIP-40
PEB 20902-C	Q67100-H8680	C-DIP-24
PEB 20902-N	Q67100-H6114	PL-CC-28 (SMD)
PEB 20902-P	Q67100-H8681	P-DIP-24

The PEB 2090 ISDN Echo-Cancellation Circuit (IEC-T) is an advanced CMOS circuit for transmission over public telephone lines. The transmission technique used is according to the U_{k0} interface specification of the Deutsche Bundespost. The adaptive filter concept of the IEC-T is based on a highly digital approach which utilizes sophisticated digital signal processing capability.

The PEB 2090 enables digital full duplex voice/data transmission via the standard twisted pair telephone cable (U interface) with a user bit rate of 144 kbit/s according to the ISDN standards. Together with the flexible IOM® interface, it is fully compatible to operate with the PEB 2070 (ICC) and PEB 2080 (SBC) devices and also enables a repeater (two IEC's back to back) for longer telephone loops.

The IEC-T is capable of operating in the following applications by means of pin strapping: the exchange, the network termination, the terminal equipment, and the trunk module connecting a PBX to the public network.

At present, the complete U interface functions are available in a two-chip set.

Features

- Full duplex transmission and reception of the U_{k0} interface signals according to the FTZ Guideline 1 TR 220 of the Deutsche Bundespost (DBP).
- Adaptive echo cancellation.
- Adaptive equalization.
- Automatic polarity adaptation.
- Clock recovery (frame and bit synchronization) in all applications.
- Transposition of ternary to binary data (4B 3T) and vice versa (coding, decoding, scrambling, descrampling, phase adaptation).
- Built in wake-up unit for activation from power-down state.
- Activation and deactivation procedure according to CCITT I.430 and to FTZ Guideline 1 TR 210 of the DBP.
- Optimized for working in conjunction with SBC and ICC telecom IC's via IOM interface.
- Handling of commands and indications contained in the IOM C/I channel for (de-)activation, supervision of power supply unit and equipment for wire testing.
- Data availability via the MONITOR channel.
- Switching of test loops.
- Generation of a synchronized 7.68-MHz clock for the SBC in the NT mode.

The IEC-T in a Two-Chip Set

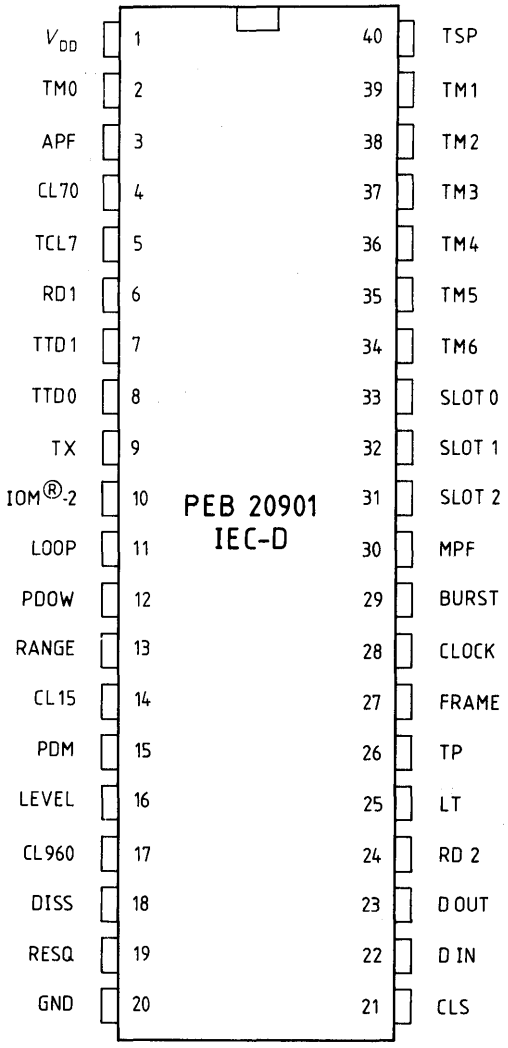
A 'Digital' Circuit, called IEC-D (PEB 20901) contains the digital receiver functions and the IOM-U_{k0} interface functions.

An 'Analog' Circuit, called IEC-A (PEB 20902) contains the crystal oscillator and all of the analog functions of the line port, namely the A/D converter in the receive path and pulse shaping D/A converter and line driver in the transmit path.

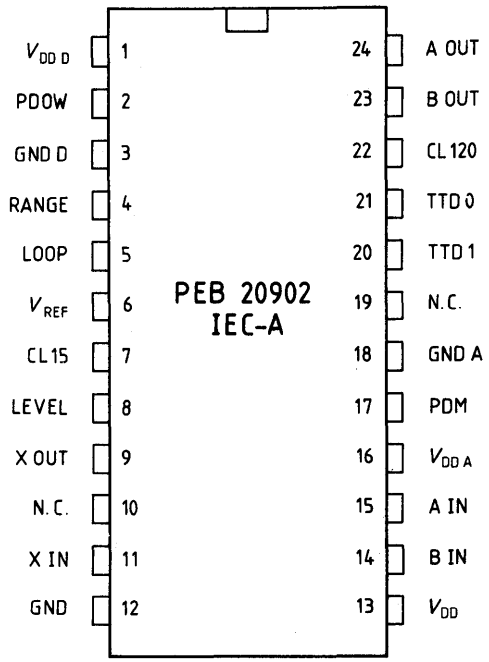
Pin Configurations

(top view)

PEB 2091 IEC Digital Part



PEB 20902 IEC Analog Part



Pin Definitions and Functions of PEB 20901

Pin. No.	Symbol	Input (I) Output (O)	Function
19	RESQ	I	**Power On Reset** (active low) must be low at least 300 µs. The clock on CLOCK pin has to be applied during reset in the LT modes and in NT-PBX mode. If not used, the RESQ pin must be clamped to high.
40	TSP	I	**Test Single Pulses.** IEC transmits single pulses of equal polarity spaced 1 ms (active high). If not used, the TSP pin must be clamped to low.
10	IOM-2	I	**Enable IOM-2 Mode.** If pin is high, the IEC is in the IOM-2 mode, otherwise it is in original IOM-1 mode.
18	DISS	O	**Disable Supply** (active high).
30	MPF	I	**Monitor Power Feed.** Serial data of power feed current (active high).
3	APF	I	**Alarm Power Feed.** Power feed overload with short response time. If not used, the APF pin must be clamped to low (active high).
6, 24	RD1, RD2	O	Two pins to control independently two relay drivers. They are set via IOM MONITOR channel.
20	GND	I	Ground-pin for digital functions of IEC.
1	V_{DD}	I	V_{DD} pin for digital functions of IEC.
26	TP	I	**Testpin.** Only for internal test purposes. Must be clamped to low during normal operations.
2,39,38, 37,36,35, 34	TM0...TM6	I	**Testpins.** Only for internal test purposes. Must be clamped to high during normal operations.
5	TCL7	I	**Testpin.** Only for internal test. Must be clamped to low during normal operation.
4	CL7O	O	**Testpin.** Only for internal test.
25	LT	I	Programs the IEC-D to LT mode (LT pin high) or NT mode (LT pin low).
29	BURST	I	Programs the IEC-D to 256-kbit/s-LT, LT-RP, NT, NT-PBX, NT-RP, or NT-TE mode (BURST pin low) or to 2048-kbit/s-LT-BURST, NT-PBX-BURST mode (BURST pin high).

Pin Definitions and Functions of PEB 20901 (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
33, 32, 31	SLOT0, SLOT1, SLOT2	I	These pins program the IEC-D to the different 256-kbit/s modes if BURST pin is low or assign the time slot in the BURST modes.
22	DIN	I	IOM data input synchronous to CLOCK.
23	DOUT	O	IOM data output synchronous to CLOCK.
28	CLOCK	I/O	Double IOM data clock.
27	FRAME	I	IOM frame signal.
21	CLS	I/O	In all LT modes: Power feed off signal from power controller. Must be clamped to low, if not used. In NT modes: 7.68-MHz clock output synchronized to the line signal. In NT-PBX modes: 512-kHz clock output synchronized to the line signal. In TE (IOM-2) mode: 768-kHz clock synchronized to the line signal. In TE (IOM-1) mode: 1.536-MHz clock synchronized to the line signal.
12	PDOW	O	Activates power-down mode of the IEC-A.
13	RANGE	O	Activates 6 dB attenuation for the ADC input signal.
11	LOOP	O	Activates the analog test loop.
17	CL 960	O	960-kHz clock. The TX signal is derived from this clock by dividing it by 8.
9	TX	O	120-kHz clock. The transmitted data are synchronized to this clock. In the one-chip solution, this clock is given out on pin TM0 during normal operation.
7	TTD1	O	Ternary data to be transmitted.
8	TTD0	O	Ternary data to be transmitted. TTD0 and TTD1 are binary coded. The combination TTD0 = 1 and TTTD1 = 0 is not used. They change with the rising edge ± 10 ns of CL120.
14	CL15	I	15.36-MHz clock.
16	LEVEL	I	Gives the polarity of the differential input signal and is used to awake signal detection.
15	PDM	I	15.36 Mbit/s output signal of the ADC in phase with C15.

Pin Definitions and Functions of PEB 20902

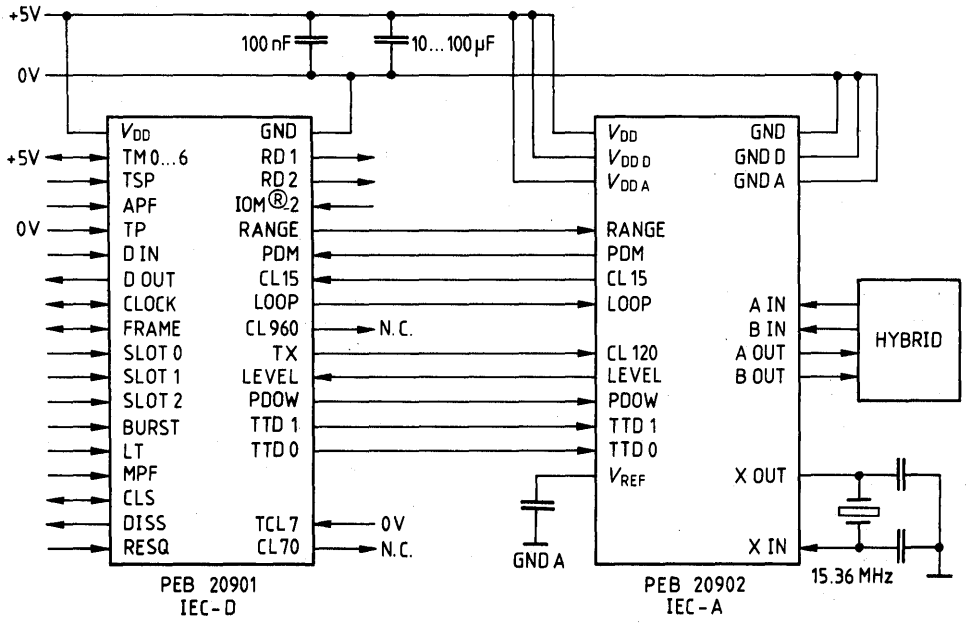
Pin No.	Symbol	Input (I) Output (O)	Function
2	PDOW	I	Activates power-down mode, only oscillator and level detect are operating during power-down.
4	RANGE	I	Activates 6 dB attenuation for the ADC input signal.
5	LOOP	I	Activates the analog test loop.
22	CL120	I	120 kHz clock input. Transmitter is synchronized to this clock.
20	TTD1	I	Digital input signal to the DAC.
21	TTD0	I	Digital input signal to the DAC. TTD0 and TTD1 are interchangeable. They must change with the rising edge (± 10 ns) of CL120.
7	CL15	O	15-MHz clock. Capacitive load should be minimized.
8	LEVEL	O	Detects the zero crossing of the differential input signal and is used to activate the IEC-D.
17	PDM	O	15 MHz, 1-bit output signal of the ADC in phase with CL15. Changes with rising edge of CL15 +2..4 ns. Capacitive load should be minimized.
15, 14	AIN, BIN	I	Received line-signal from hybrid.
24, 23	AOUT, BOUT	O	Transmitted line-signal to hybrid.
3	DGND	I	Ground-pin for digital functions of IEC-A.
1	$V_{DD\,D}$	I	V_{DD}-pin for digital functions of IEC-A.
18	AGND	I	Ground-pin for digital functions of IEC-A.
16	$V_{DD\,A}$	I	V_{DD}-pin for digital functions of IEC-A.
12	GND	I	Ground-pin for digital functions of IEC-A.
13	V_{DD}	I	V_{DD}-pin for digital functions of IEC-A.
6	V_{REF}	O	V_{REF}-pin to buffer internally generated voltage with capacitor 10 nF versus AGND.
11	XIN	I	In all NT modes, crystal connection. In all LT modes, 15.36-MHz clock input synchronized to IOM clocks.
9	XOUT	O	In all NT modes, crystal connection. In all LT modes, to be left open.

All digital outputs use positive logic and CMOS levels. Drive capability is 10 pF for CL15 and PDM and 25 pF for LEVEL. All input signals are active high and use CMOS logical levels. XIN and XOUT supply a load of 2-3 pF vs. ground to the crystal.

The maximum power consumption without load at CL15 is 15 mW in power-down mode, 100 mW with open outputs AOUT/BOUT and 150 mW during normal transmission.

The sensitivity of the ADC can be reduced, if necessary, by putting a resistor between AIN and BIN (10..20 kΩ).

Application Diagram of IEC-D and IEC-A (Two-Chip Solution)



Operation Modes and Functions

IOM Concept and Applications of the IEC-T

The IEC-T is designed to be used in: the Line Terminator (LT) part of the Digital Subscriber Module (DSM), the Network Termination (NT), the Digital Trunk Basic Access (PBX) and in the Terminal Equipment (TE).

Figure 1

Connecting S-Bus to Public Network

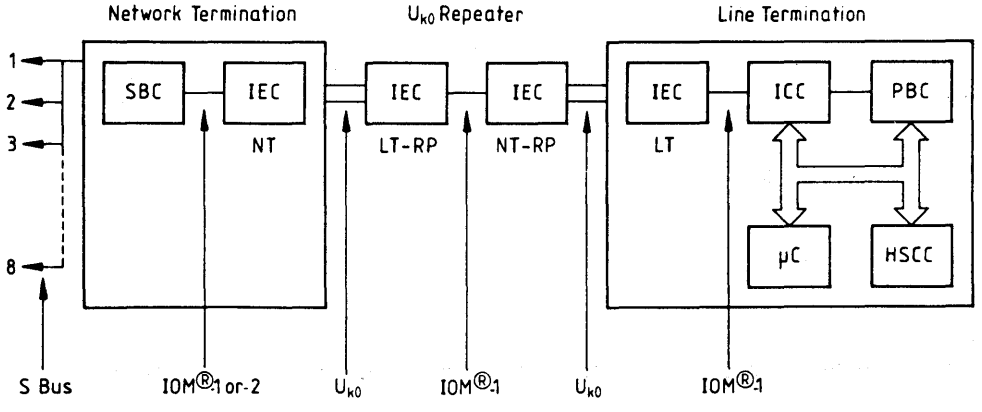


Figure 2

Connecting Private to Public Network

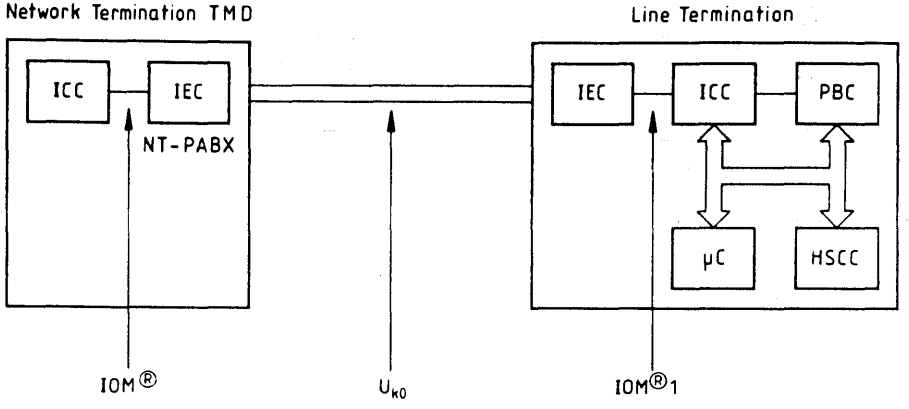


Figure 3
Connecting Terminal Equipment within Private Network (1st Generation)

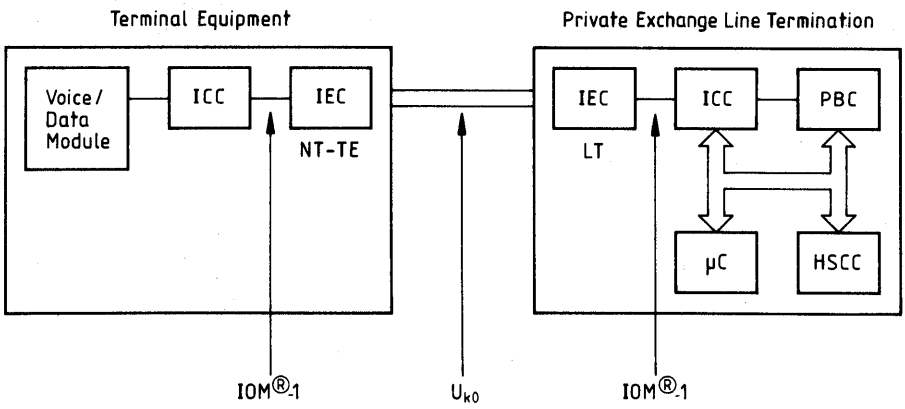
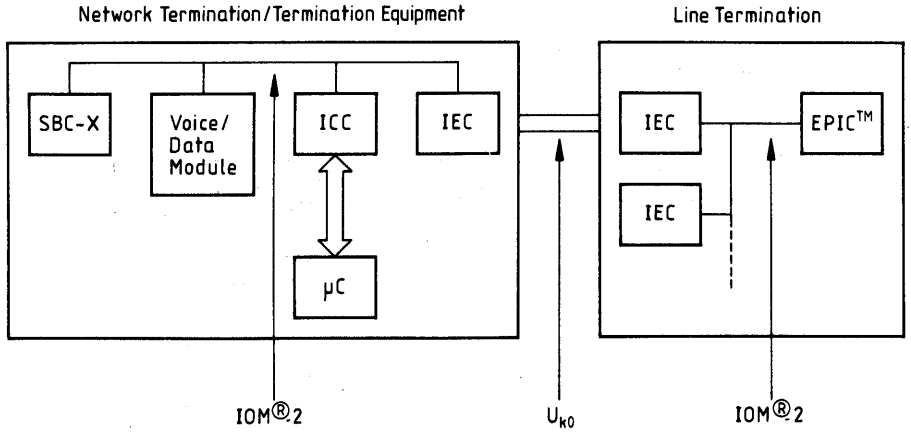


Figure 4
Connecting Network Termination or Terminal Equipment to Exchange (2nd Generation)

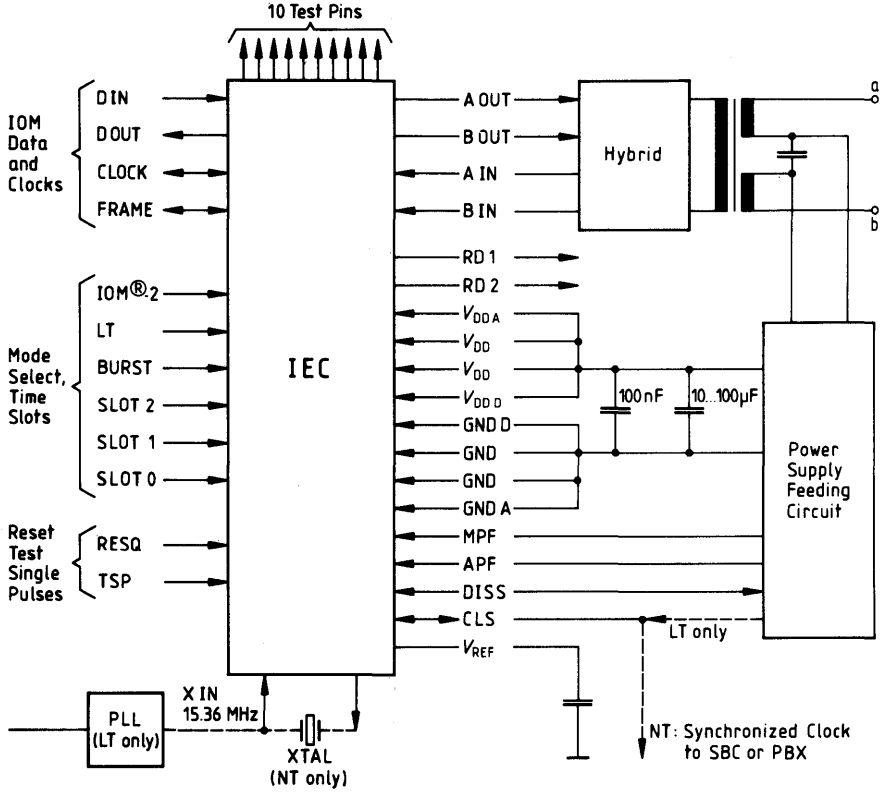


To cater to these various applications, the IEC-T can be programmed via pin strapping to different modes **(see following table)**.

Table 1
Programming the IEC-T Operation Modes

Signal on Input Pin					MODE
LT	BURST	SLOT2	SLOT1	SLOT0	
0	0	0	0	0	LT
1	0	0	0	1	LT-RP: Repeater downstream
1	1	*	*	*	LT-BURST: LT MUX mode
0	0	0	0	0	NT
0	0	0	0	1	NT-RP: Repeater upstream
0	0	1	0	0	NT-PBX: PBX continuous mode
0	0	1	0	1	NT-TE: Terminal Equipment
0	1	*	*	*	NT-PBX BURST: PBX MUX mode

Figure 5
Interfaces of the IEC-T



* In these modes SLOT2, SLOT1, SLOT0 are used for selecting the time slot rather than the mode.

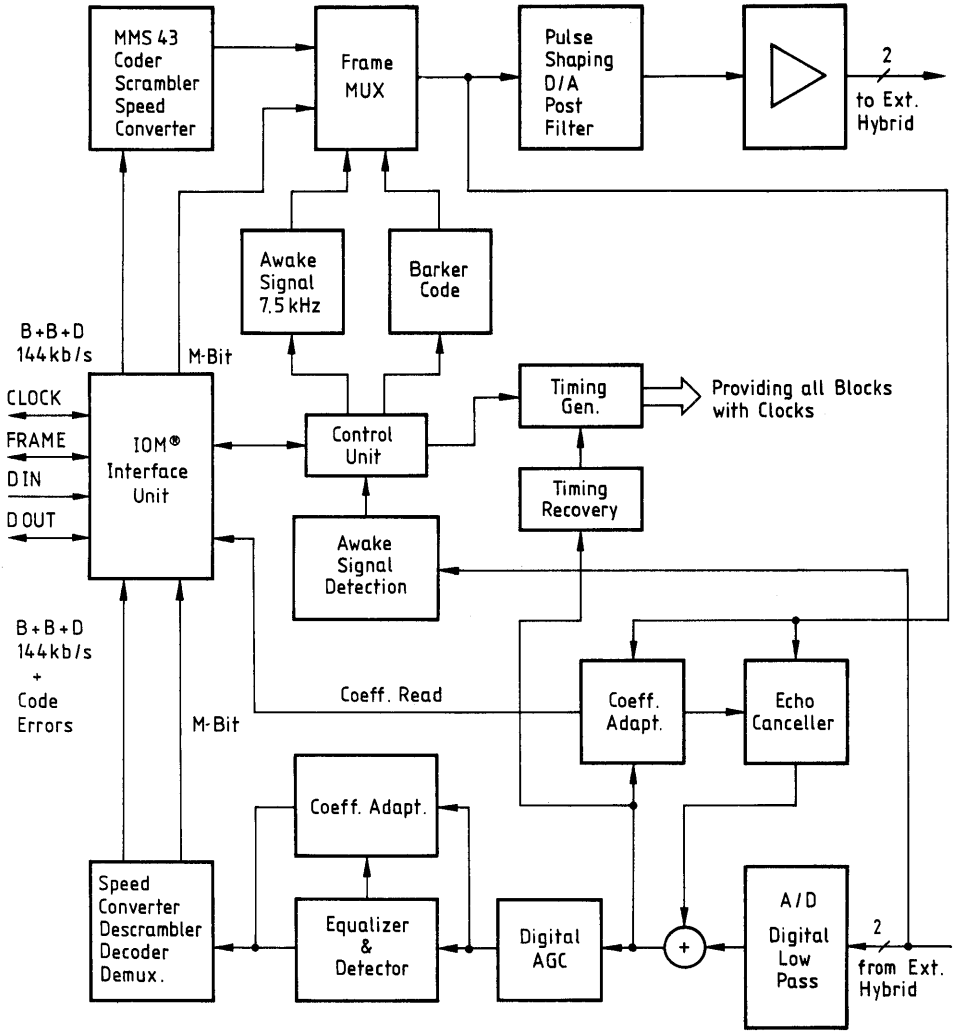
Mode Dependent Functions

Table 2
Mode Dependent Functions

Pin	LT	LT-BURST1	LT-BURST2	LT-RP	NT-RP	NT	NT-PBX	NT-PBX-BURST1	NT-PBX-BURST2	NT-TE1	NT-TE2
LT	1	1	1	1	0	0	0	0	0	0	0
BURST	0	1	1	0	0	0	0	1	1	0	0
IOM-2	0 or 1	0	1	0	0	0 or 1	0 or 1	0	1	0	1
SLOT 0	0	Time-	Time-	1	1	0	0	Time-	Time-	1	1
SLOT 1	0	Slot	Slot	0	0	0	0	Slot	Slot	0	0
SLOT 2	0	select	select	0	0	0	1	select	select	1	1
DIN	256 kbit/s	2048 Mbit/s	256..2500 Mbit/s	256 kbit/s	256 kbit/s	256 kbit/s	256 kbit/s	2048 Mbit/s	256..2500 Mbit/s	256 kbit/s	768 kbit/s
DOUT	256 kbit/s	2048 Mbit/s	256..2500 Mbit/s	256 kbit/s	256 kbit/s	256 kbit/s	256 kbit/s	2048 Mbit/s	256..2500 Mbit/s	256 kbit/s	768 kbit/s
CLOCK	512 kHz IN	4096 kHz IN	512..5000 kHz IN	512 kHz IN	512 kHz OUT	512 kHz OUT	512 kHz IN	4096 kHz IN	512..5000 kHz IN	512 kHz OUT	1536 kHz OUT
FRAME	8 kHz IN	8 kHz IN	8 kHz IN	8 kHz IN	8 kHz 1:1 OUT	8 kHz 1:1 OUT	8 kHz IN	8 kHz IN	8 kHz IN	8 kHz 1:1 OUT	8 kHz 1:1 OUT
CLS	PFOFF IN	PFOFF IN	PFOFF IN	PFOFF IN	7.68 MHz OUT	7.68 MHz OUT	512 kHz OUT	512 kHz OUT	512 kHz OUT	1536 MHz OUT	768 kHz OUT
XIN	15.36 MHz	15.36 MHz	15.36 MHz	15.36 MHz	XTAL	XTAL	XTAL	XTAL	XTAL	XTAL	XTAL
XOUT	NC	NC	NC	NC	XTAL	XTAL	XTAL	XTAL	XTAL	XTAL	XTAL

Survey of IEC Functional Blocks

Figure 6
Functional Block Diagram of IEC-T



Description of the Digital Module Interface

The IEC-T is provided with an IOM interface which operates in both a continuous and a burst mode in order to interface units which realize OSI layer-1 functions like the SBC (PEB 2080) and to layer-2 functions like the ICC (PEB 2070).

The IEC-T is designed for the original IOM interface (IOM-1), but with the IOM-2 pin it is possible to give the IEC-T some physical features of the IOM-2 interface. Logically, the IEC-T behaves like in IOM-1 mode.

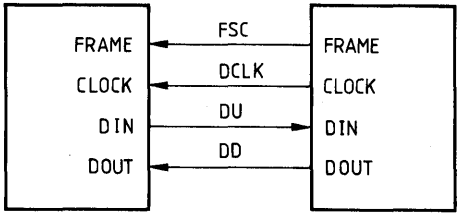
There are three differences between IOM-1 and IOM-2 operation modes:

- In the BURST modes, IOM-2 frame synchronization is the same as in the 256-kbit/s modes. Additionally, the IEC-T enables clock frequencies on DCLK ranging from 512 to 5000 kHz in increments of 8 kHz.
- Each E-bit (MX-bit) is reflected in the T-bit (MR-bit) in the next IOM-2 frame. For IOM-2 interfaces, the E-bit is always used to access the MONITOR channel, which is acknowledged in the T-bit.
- The transparent channel on U_{k0} can't be used, because the T-bit is used for MONITOR channel access.

All other features of IOM-2, like other C/I and MONITOR channel codes, are not implemented in the IEC-T.

Figure 7

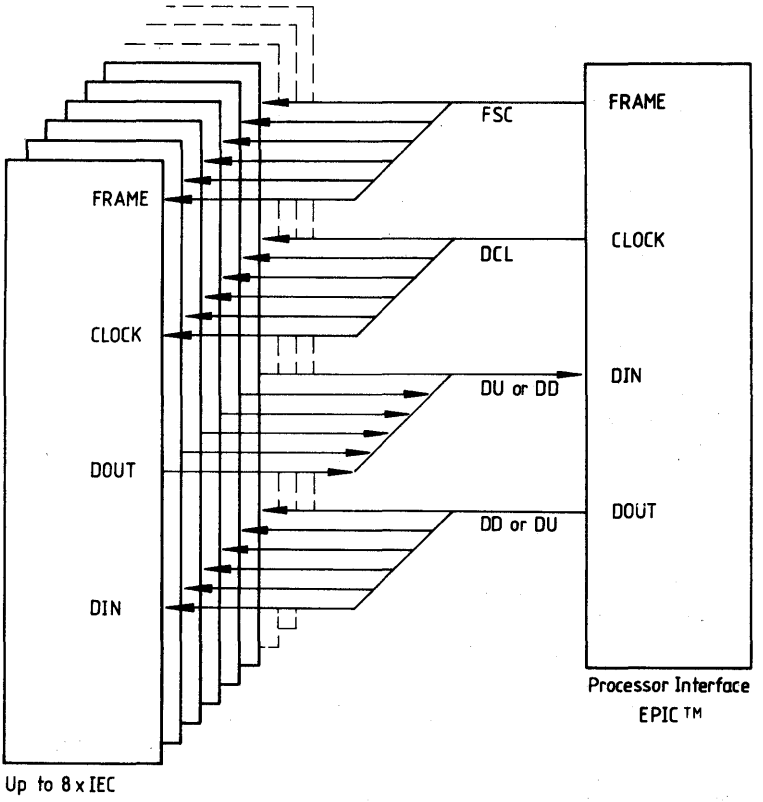
IOM Interface in Different Applications of the IEC-T



In the Exchange:	IEC	ICC
In the Repeater:	IEC	IEC
In the NT :	SBC	IEC
In the TMD :	IEC	ICC
In the TE :	ICC	IEC

Figure 8

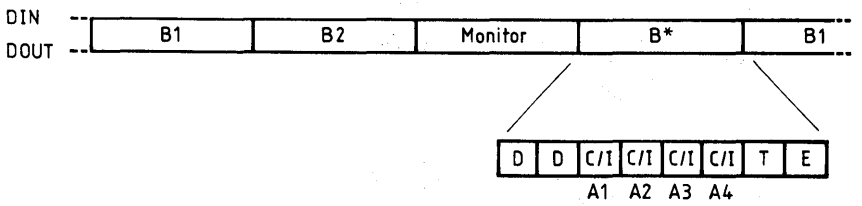
IOM Interface MUX Mode



For each application, the ISDN data rate of 144 kbit/s (2 B + D) is transmitted transparently via the modular interface. It is necessary to exchange control information for means of activation and deactivation of OSI layer-1 functions and switching of testloops. In some applications, access to maintenance information is additionally provided.

This information is transferred in a time multiplex procedure based on an 8-kHz frame-structure **(see following figure)**.

Figure 9
Frame Structure of the Digital Interface of IEC-T



Four octets are transmitted in each frame:

1st octet B1: B channel (64-kbit/s data) MSB first.

2nd octet B2: B channel (64-kbit/s data) MSB first.

3rd octet: MONITOR (8-bit monitor address for DIN, 8-bit monitor data with MSB first for DOUT.

4th octet B*: 2 bit D channel 16-kbit/s data

4 bit C/I channel.

T channel for 1-kbit/s transparent data with IOM-1 or for the handling of the monitor channel with IOM-2 (MX-bit).

E extension bit for control of monitor channel and to hand over the maintenance bit of U_{k0}.

In the multiplexed modes, the IOM data of up to eight IEC-Ts are multiplexed. The data streams consist of bursts of 4 octets per frame. The bursts are allocated to consecutive time slots in a frame by the static inputs SLOT0, SLOT1, SLOT2. Outside of the allocated time slot, the IEC-T must not read from DIN-pin and the DOUT-pin remains high impedance. The next table indicates the allocations.

Table 3
Allocation of Time Slots in IOM-1 and IOM-2 Modes

Time Slot No.	SLOT0	SLOT1	SLOT2	Bit No.
0	0	0	0	0...31
1	0	0	1	32...63
2	0	1	0	64...95
3	0	1	1	96...127
4	1	0	0	128...159
5	1	0	1	160...191
6	1	1	0	192...223
7	1	1	1	224...255

Clock Generation

The master clock is the clock signal with the highest frequency in the system.

NT Modes

The master clock is derived from a built-in crystal oscillator in the NT operating modes. The crystal is connected to the pins XIN and XOUT. The maximum capacitive load at XIN and XOUT is 60 pF each.

Nominal frequency:	15.36 MHz
Overall tolerance:	± 100 ppm

We recommend using a crystal (serial resonance) which meets the following specification:

Nominal frequency:	15.36 MHz
Overall tolerance:	± 60 ppm
Load capacitance:	20 pF
Resonance resistance:	20 Ω
Shunt capacitance:	7 pF

LT Modes

In the LT modes, the timing signal is derived from the clock via an external phase locked loop. The master clock is fed to pin XIN.

Nominal frequency:	15.36 MHz
Duty ratio:	0.4...0.6
Rise and fall times:	< 10 ns
Max. Difference of phase deviations of master clock/1920 and FSC:	± 18 µs
Max. low freq. phase wander within 1 period:	± 0.85 ps
Jitter (peak-to-peak):	see following figure

In the deactivated state, while no data has to be recognized on the line, no particular jitter requirements have to be kept.

Figure 10
Maximum Sinusoidal Input Jitter of Master Clock 15.36 MHz

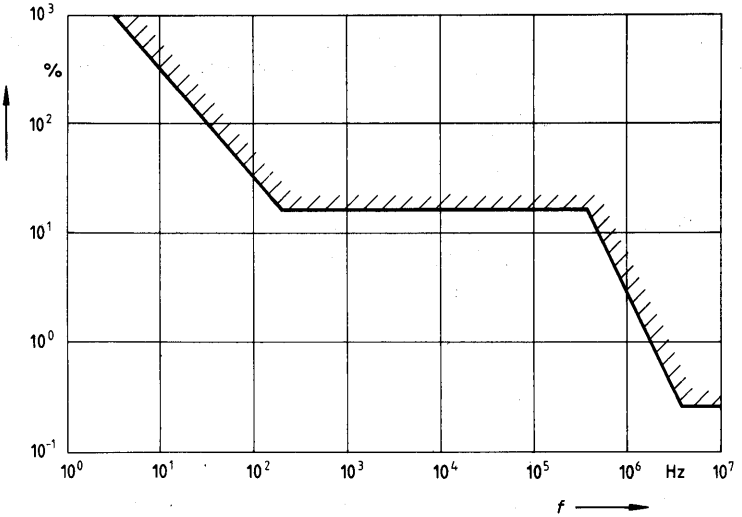
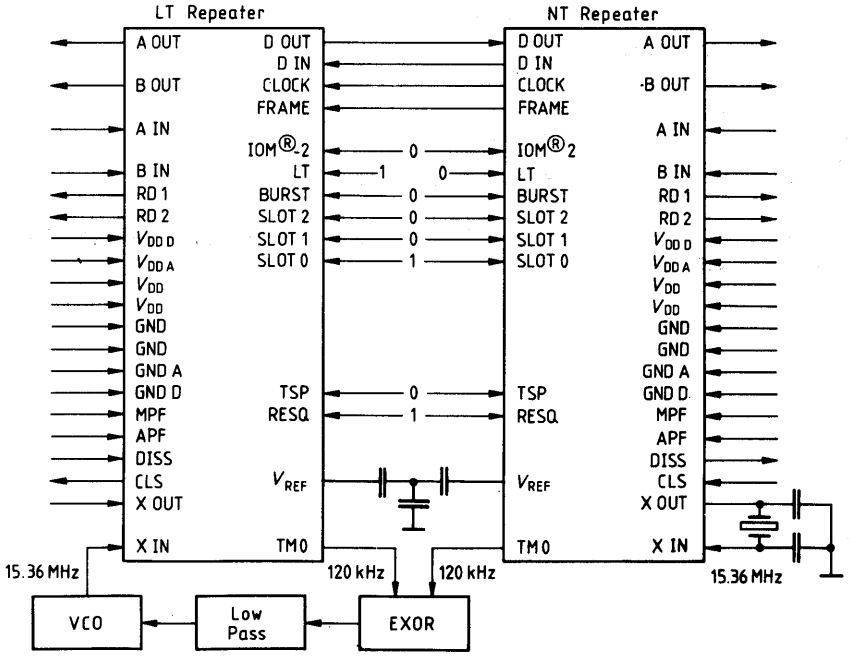


Figure 11
Interfaces of the IEC-T in NT-RP Mode



Description of the Line Port

The U_{k0} interface is designed for data transmission on twisted pair wires in local telephone loops, with basic access to ISDN and a user bit rate of 144 kbit/s.

Separation of the transmitted and received signals is done by means of echo cancellation.

The following functions are transmitted over the twisted pair:

- Bidirectional
  - B1, B2, D, T data channels
  - 120-kHz symbol clock
  - 1-kHz frame and 40-kHz block clock
  - Activation
- From LT to NT side:
  - Power feeding
  - Deactivation
  - Remote control of test loops
- From NT to LT side:
  - Indication of monitored code violations

On the U_{k0} interface, transmission ranges of 4.2 km on wires of 0.4 mm diameter and 8 km on 0.6 mm wires are achieved without additional signal regeneration on the loop.

The transmission ranges can be doubled by inserting one repeater for signal regeneration.

Frame Structure of the U_{k0} Interface

1 ms frames are transmitted via the U_{k0} interface, each consisting of:

- 108 symbols: 144-bit scrambled and coded B+B+D data
- 11 symbols: Barker code for both symbol and frame synchronization (not scrambled)
- 1 symbol: Ternary maintenance symbol (not scrambled)

The 108 user data symbols are split into four equally structured groups. Each group (27 ternary symbols, 36 bits) contains the user data of two IOM frames in the same order (8B + 8B + 2D) + (8B + 8B + 2D).

Different synchwords are used for each direction:

- Downstream from LT to NT +++−−−+−−+−
- Upstream from NT to LT −+−−+−−−+++

On the NT side, the transmitted Barker code begins 60 symbols after the received Barker code and vice versa.

After successful synchronization, resynchronization will occur if the synchword is found to be consecutively 64 times in another position in the frame than the one expected after successful synchronization.

Coding from Binary to Ternary Data

Each 4-bit block of binary data is coded into 3 ternary symbols of MMS 43 block code according to the following table.

The number of the next column to be used, is given at the right hand side of each block. The left hand signal elements in the table (both ternary and binary) are transmitted first.

Table 4
MMS 43 Coding Table

	S1	S2	S3	S4
t ⟶	t ⟶	t ⟶	t ⟶	t ⟶
0 0 0 1	0 − + 1	0 − + 2	0 − + 3	0 − + 4
0 1 1 1	− 0 + 1	− 0 + 2	− 0 + 3	− 0 + 4
0 1 0 0	− + 0 1	− + 0 2	− + 0 3	− + 0 4
0 0 1 0	+ − 0 1	+ − 0 2	+ − 0 3	+ − 0 4
1 0 1 1	+ 0 − 1	+ 0 − 2	+ 0 − 3	+ 0 − 4
1 1 1 0	0 + − 1	0 + − 2	0 + − 3	0 + − 4
1 0 0 1	+ − + 2	+ − + 3	+ − + 4	− − − 1
0 0 1 1	0 0 + 2	0 0 + 3	0 0 + 4	− − 0 2
1 1 0 1	0 + 0 2	0 + 0 3	0 + 0 4	− 0 − 2
1 0 0 0	+ 0 0 2	+ 0 0 3	+ 0 0 4	0 − − 2
0 1 1 0	− + + 2	− + + 3	− − + 2	− − + 3
1 0 1 0	+ + − 2	+ + − 3	+ − − 2	+ − − 3
1 1 1 1	+ + 0 3	0 0 − 1	0 0 − 2	0 0 − 3
0 0 0 0	+ 0 + 3	0 − 0 1	0 − 0 2	0 − 0 3
0 1 0 1	0 + + 3	− 0 0 1	− 0 0 2	− 0 0 3
1 1 0 0	+ + + 4	− + − 1	− + − 2	− + − 3

Signal Elements used for Activation and Deactivation

Certain signal elements are used for activation and deactivation which cannot appear during normal operation. In this section, only the coding is described.

Table 5
Coding of the U_{k0} Signal Elements

Upstream from NT to LT	Downstream from LT to NT
INFO U1W: 16 times ternary +++++++−−−−−−−− A tone of: Frequency: 7.5 kHz Width: 2.13 ms	INFO U2W: 16 times ternary +++++++−−−−−−−− A tone of: Frequency: 7.5 kHz Width: 2.13 ms
INFO U1A: Binary continuous "0" before scrambling. No frame, ternary "0" instead of Barker code	INFO U2A: Binary continuous "0" before scrambling. No frame, ternary "0" instead of Barker code
INFO U1: Binary continuous "0" before scrambling. Frame (Transmitting Barker code)	INFO U2: Binary continuous "0" before scrambling. Frame (Transmitting Barker code)
INFO U3: Binary continuous "1" before scrambling. Frame (Transmitting Barker code)	INFO U4H: Binary continuous "1" before scrambling with duration of 1 ms. Frame (Transmitting Barker code)
INFO U5: Binary data from the digital interface. Frame (Transmitting Barker code)	INFO U4: Binary data from the digital interface. Frame (Transmitting Barker code)
INFO U0: Ternary continuous "0" No frame, no signal level	INFO U0: Ternary continuous "0" No frame, no signal level

The IEC detects an INFO U1, U2, or U3 if the contnuous binary data is found on the descrambler output after 8 subsequent U_{k0} frames. These INFO's are detected after 8 to 9 ms.

INFO U4H is recognized if the NT finds 16 subsequent binary 1's in the data stream.

INFO U0 is recognized if the IEC-T finds one complete frame with continuous zero level.

Analog Functions of the Line Port

Input signal

The peak input signal, measured between AIN and BIN, must be below 4 V peak-to-peak. The maximum SNR is achieved with 1.3 V_{pp} (range inactive) or 2.6 V_{pp} (range active) input signal voltage.

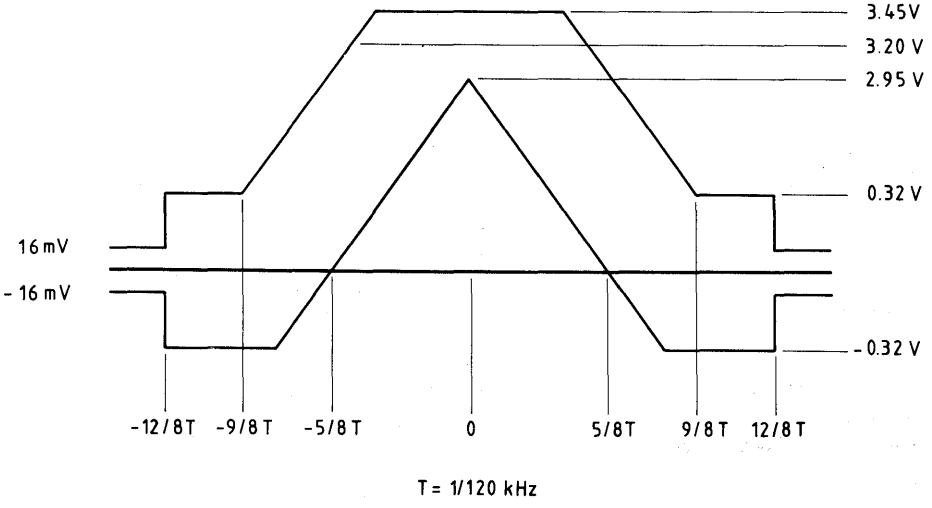
The input impedance, measured between AIN and BIN, is at least 50 k.

For short lines, the input signal to the ADC is automatically attenuated by 6 dB ± 1 dB in order to lower the high receive signal.

An external loop command in the C/I channel activates an internal analog test loop from the output pins to the input pins of the IEC-T. The signal is attenuated by 12 dB within this loop.

The pulse mask for a single positive pulse measured between AOUT and BOUT with a load of 172 Ω is given in the following figure.

Figure 12
Pulse Mask for a Single Positive Pulse



The peak-to-peak voltage of a single positive pulse measured between AOUT and BOUT terminated with 172 Ω is 3.20 V ± 8%.

The offset voltage, measured under the same conditions as above, is less than 2% of the peak amplitude.

The signal amplitude measured over a period of one minute varies less then 1%.

The output impedance measured between AOUT and BOUT is below 5 Ω in power-up and below 18 Ω in power-down mode. The required impedance of 150 Ω ± 5% seen from the line side of the transformer is established by putting two resistors of 41 Ω ± 1% each in the hybrid.

The load is given by the hybrid, the transformer and the subscriber line.

The transformer ratio should be 1 : 1.32 (circuit/line side) and the total inductivity seen from the line side between 5 and 10 mH.

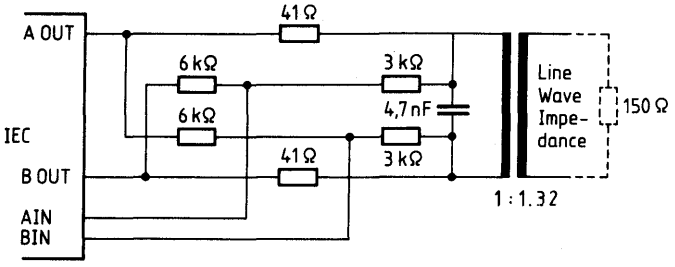
The sum of noise and total harmonic distortion, weighted with a low pass filter 0 to 100 kHz, is at least 60 dB below the signal for an evenly distributed but otherwise random sequence of + 1, 0, and -1.

External Hybrid

The hybrid balancing circuit is external to the IEC-T chip. Suggestions for the circuit configuration and dimensioning of the hybrid are given in the following figure.

Each resistor has to keep an absolute tolerance of 1%.

Figure 13
Example for Hybrid Balancing Circuit



Maintenance Functions

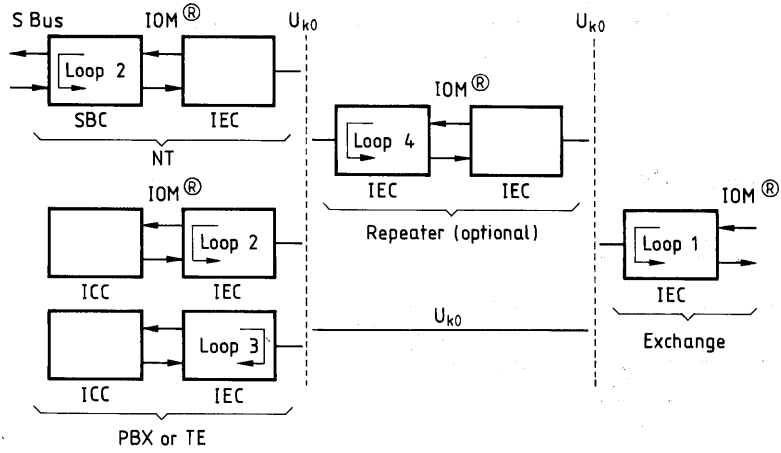
Loops

For test of the line cards, several test loops are provided which can be controlled from the exchange. When a test loop is closed, all channels (B + B + D) are looped back and data from the other end of the line is ignored. There are no separate loops for single channels.

All test loops are transparent loops. During test loops, the line signal is still transmitted. Nevertheless, the IEC-T NT or NT-RP receives this signal and synchronizes to it. The IEC-T NT or NT-RP cannot distinguish between line signals sent from LT or LT-RP during loop 1 or loop 4, and signals sent during normal operation.

Figure 14

Test Loops Closed by the IEC-T or Under its Remote Control



Loop 1, loop 4, and loop 3 are closed in the IEC-T as near to the U_{k0} interface as possible. Using internal switches, the signal from the line driver is fed back directly to the input. It is like a short-circuit between the pins AOUT and AIN as well as between BOUT and BIN. The input signal from the hybrid is ignored in this mode.

The analog loop mode is controlled via the IOM C/I channel

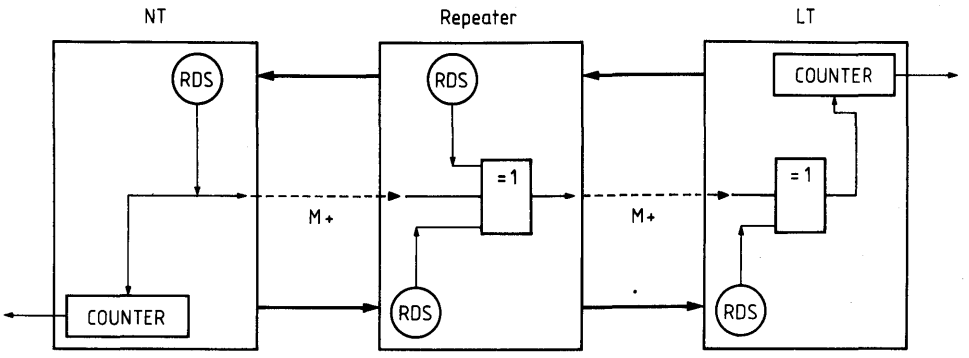
Monitoring of Code Violations

The RDS monitor computes the running digital sum from the received ternary symbols by adding the polarity of the received user data (+1,0,–1). At the end of each block, the running digital sum is the number of the next column in **table 4** which should contain the next received block. A code violation has occured if the running digital sum is less than one or more than four at the end of a ternary block, or if the ternary block 0 0 0, three user symbols with zero polarity, is found in the received data.

In the NT modes, a positive M symbol is transmitted upstream if any code error has been detected within a frame (position 25 upstream in the U_{k0} frame from NT to LT).

The IEC-T contains an error counter which counts U_{k0} frames with at least one detected code violation. In the LT mode, additionally, the frames with a received positive M symbol are counted. The error counter can be read and simultaneously be reset from a certain state of activation via the IOM interface in all modes except the repeater modes. The counter is always stopped after reaching 255 which is the maximum value passed to the monitor channel.

Figure 15
Transmission of Detected Frame with RDS Errors



The counter is automatically reset during deactivation of the U_{k0} line. In the LT modes, it is enabled again to count code violations from the moment the RDS or AIU code is written into the IOM C/I channel, indicating that the line is synchronized. In the NT modes, it is enabled again from the moment the AID code is written into the IOM C/I channel.

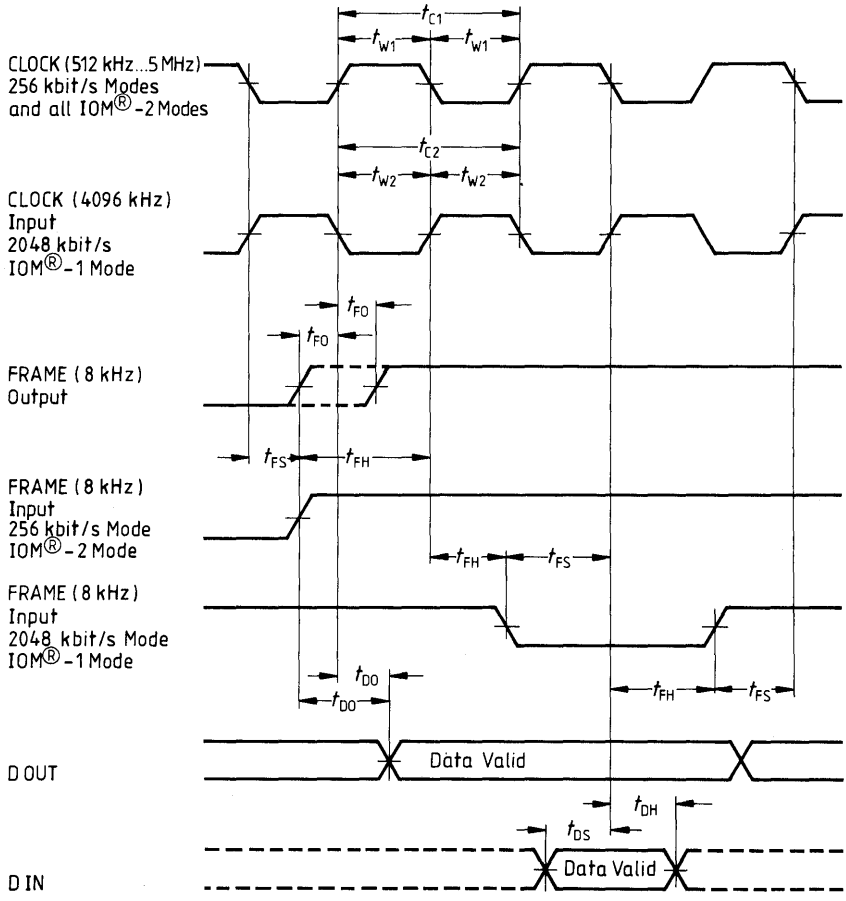
Each counted frame with a detected code violation leads to 10 to 20 binary bit errors on average. So a bit error rate of 10^{-7} in both directions leads to about 2 detected frame errors within 1000 s in the LT (1 frame error detected in the NT and transmitted via M symbol).

Static Characteristics

V_{DD} = 4.75 to 5.25 V

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
H-input voltage	V_{IH}	3.5			V	
L-input voltage	V_{IL}			1.0	V	
L-input leakage current	I_{IL}	−10			µA	V_{in} = DGND
H-input leakage current all inputs except AIN, BIN, XIN, XOUT, VREF	I_{IH}			10	µA	V_{in} = DVDD
H-output voltage all outputs except DOUT	V_{OH1}	4.0			V	I_{OH1} = 0.4 mA
H-output voltage DOUT (Open Drain)	V_{OH2}			V_{DD}	V	R to V_{DD}
L-output voltage all outputs except DOUT	V_{OL1}			0.33	V	I_{OL1} = 0.4 mA
L-output voltage DOUT (Open Drain)	V_{OL2}			0.5	V	I_{OL2} = 6 mA
Input capacitance DIN, MPF. CLOCK, FRAME, CLS (input) DOUT (open)	C_{IN}			10	pF	

Figure 26
Timing of Externals Signals on Digital Interface of IEC-T



Note: The rise and fall times are to be measured between 10% and 90%. A pulse width or delay is to be measured from $V_{DD}/2$ to $V_{DD}/2$ levels.

Dynamic Input Requirements

Parameter	Symbol	Limit Values		Unit
		min.	max.	
CLOCK, FRAME, DIN, MPF	t_{rise}		30	ns
CLOCK, FRAME, DIN, MPF	t_{fall}		30	ns
FRAME	t_{fs}	30		ns
FRAME	t_{fh}	30		ns
DIN, MPF	t_{ds}	30		ns
DIN, MPF	t_{dh}	30		ns
CLOCK	t_{w1}	100		ns
CLOCK	t_{w2}	100		ns

Dynamic Output Characteristics

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
CLOCK, FRAME, DISS, CLS, RD1, RD2	t_{rise}			30	ns	$C = 25$ pF
CLOCK, FRAME, DISS, CLS, RD1, RD2	t_{fall}			30	ns	$C = 25$ pF
DOUT	t_{fall}	0		200	ns	$C = 150$ pF $R = 1$ kΩ to V_{DD}
CLOCK 512 kHz 1536 kHz	t_{cl}	1875 565	1953 651	2035 735	ns ns	$C = 25$ pF
CLOCK 512 kHz 1536 kHz	t_{w1}	880 230		1075 420	ns ns	$C = 25$ pF
FRAME	t_{fo}	−30	0	30	ns	$C = 25$ pF
DOUT (high-low transition)	t_{do}	0 0		200 150	ns ns	$C = 150$ pF $R = 1$ kΩ to V_{DD} $C = 50$ pF $R = 1$ kΩ to V_{DD}

Analog Characteristics

$T_A = 70\,°C$, $V_{DD} = 4.75\,V$

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
Receive Path					
Signal / (noise and distortion)	*SN*	57	62		dB
DC-level at AD-output relative to V_{DD}		0.45	0.5	0.55	
Threshold of level detect		12		41	mV
Transmit Path					
Signal / (noise distortion)	*SN*	60	65		dB
Output DC level		2,05	2.375	2.6	V
Offset between AOUT/BOUT				34.5	mV
Signal amplitude		2.95		3.45	V
Output impedance between AOUT/BOUT					
in power-up			3	5	Ω
in power-down			10	18	Ω

Power Consumptuion

Device	State of Operation	Limit Values		Unit	Test Conditions
		typ.	max.		
IEC-D	Power-up	140	160	mW	$V_{DD} = 5\,V$ open outputs
	Power-down	10	15	mW	
IEC-A	Power-up	125	140	mW	during normal transmission CL15 open
	Power-down	10	15	mW	

Environmetal Requirements

Storage and Transportation

The rated (limiting capability) storage and transportation temperature range prior to printed board assembly shall be as follows:

−60 °C to 125 °C (without supply voltage)
−10 °C to 80 °C (with applied voltages)

Operating Ambient Temperature

The operating ambient temperature shall be from 0 °C to 70 °C.

SIEMENS

ISDN Ech-Cancellation Circuit (IEC-Q) PEB 2091

Preliminary Data **CMOS IC**

Type	Ordering Code	Package
PEB 2091-N	Q67100-H6119	PL-CC-44 (SMD)

The PEB 2091 ISDN Echo-Cancellation Circuit (IEC-Q) is an advanced CMOS transceiver for ISDN Basic Access Digital Subscriber Loops with 2B1Q line code.

Control and algorithmic requirements are implemented according to the layer-1 specification of the American National Standard Institute (ANSI) for a 144 bit/s full duplex data transmission.

Together with the flexible IOM-2 interface, the IEC-Q is fully compatible with the PEB 2081 (SBCX), PEB 2055 (EPIC™) and PEB 2075 (IDEC™) devices.

Features

- U Transceiver with 2B1Q line code according to layer-1 specification of ANSI
- Activation and deactivation procedure according to T1D1 layer-1 specification and CCITT I.430
- Programmable operation modes
- IOM-2 interface
- Adaptive echo cancellation
- Adaptive equalization
- Automatic polarity adaptation
- Clock recovery (frame and bit synchronization)
- Low power consumption

Basic System Functions

- Full duplex data transmission and reception at the U reference point according to the layer-1 specification of the American National Standard Institute:
  - 144 bit/s user bit rate over a two-wire subscriber loop
  - 2B1Q block code (2 binary, 1 quaternary)
  - 4 bit/s maintenance channel for transmission of data loop back commands and detected transmission errors
  - monitoring of transmission errors
  - operating at telephone loop plant LOOP#1 up to LOOP#15 as defined by American National Standard
- Transposition of quaternary to binary data and vice versa (coding, decoding, scrambling, descrambling, phase adaption)
- Built-in wake up unit for activation from power down state
- Activation and deactivation procedure according to T1D1 layer-1 specification and CCITT I.430
- Adaption of internal interfaces to the current signal direction by programmable operation modes:

LT:	Line termination in public or private exchange
TE:	Terminal mode
NT:	Network termination connected to SBCX
NT-PBX:	Trunk module (TDM)

- Adaptive echo cancellation
- Adaptive equalization
- Automatic polarity adaption
- Clock recovery (frame and bit synchronization) in all applications
- Optimized for working in conjunction with SBCX, ICC, EPIC and IDEC telecom ICs via IOM-2 interface
- Data speed conversion between the U reference point and the IOM frames
- Handling of the commands and indications contained in the IOM-2 C/I channel for deactivation, activation, supervision of power supply unit and equipment for testing
- Data availability via monitor-channel:
  - CRC transmission errors
  - Measurement value of the loop current
  - Echo canceler coefficients and status values, which can be used to indicate the state of the loop
- Switching test loops
- Generation of synchronized 7.68-MHz clock for SBCX in NT mode
- Low power consumption: standby: max. 30 mW
  active: max. 300 mW

Functional Description

The IEC-Q can be subdivided into three main blocks:

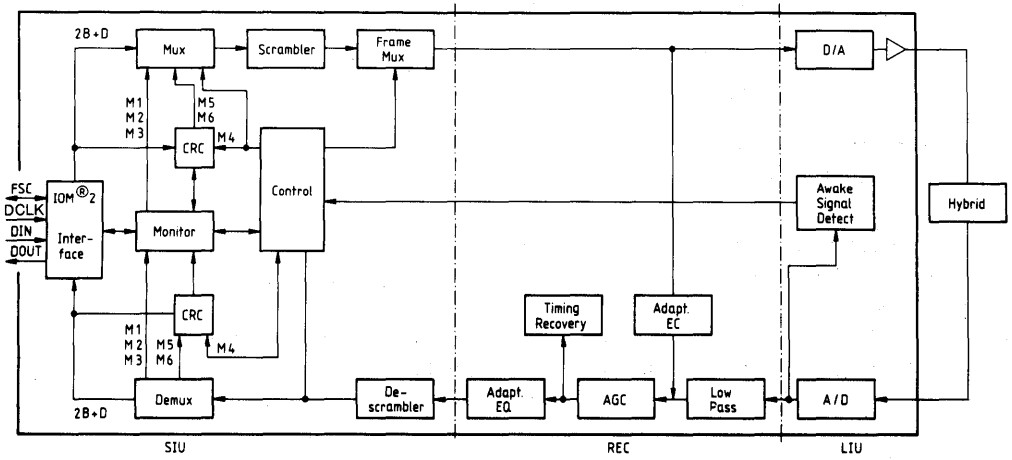
- LIU Line Interface Unit
- SIU System Interface Unit
- REC Receiver

The Line Interface Unit (LIU) contains the crystal oscillator and all of the analog functions, namely the A/D converter in the receive path, pulse shaping D/A converter and line driver in the transmit path.

The System Interface Unit (SIU) features the activation and deactivation procedures, the timing recovery and synchronization, maintenance data handling, frame conversion and speed adaption.

The Receiver block (REC) performs the filter algorithmic functions using digital signal processing techniques. In a modular multi-processor concept modules for echo cancellation, pre- and post-equalization, phase adaption and frame detection are implemented.

Block Diagram of IEC-Q



Pin Definitions and Functions

Pin No.	Symbol	Input (I) Output (O)	Function
7, 8	V_{DDA1}	S	Analog supply voltage 5 V ± 5%
13	V_{DDA2}	S	Analog supply voltage 5 V ± 5%
5	GNDA1	S	Analog 0 V
16	GNDA2	S	Analog 0 V
1, 2	V_{DDD}	S	Digital supply voltage 5 V ± 5%
23	GNDD	S	Digital 0 V
11	XTAL0	I	Crystal connection or external clock input
10	XTAL1	I	Crystal connection. Left unconnected if external clock is used
15	AIN	I	Received line signal to hybrid
14	BIN	I	Received line signal to hybrid
6	AOUT	O	Transmitted line signal to hybrid
4	BOUT	O	Transmitted line signal to hybrid
9	V_{REF}	O	V_{REF}-pin to buffer internally generated voltage with capacitor 10 nF vs GNDA
31	DCLK	I/O	IOM-2 device clock
30	FSC	I/O	IOM-2 frame clock
26	DIN	I	IOM-2 data input synchronous to DCLK
22	LT	I	LT mode (HIGH input = LT mode) (LOW input = NT mode)
24	BURST	I	NT-, NT-TE mode (LOW) LT-, NT-PBX mode (HIGH)
36	SLOT0	I	256 kbit/s modes select Allocation of time slot for BURST mode
35	SLOT1	I	256 kbit/s modes select Allocation of time slot for BURST mode
33	SLOT2	I	256 kbit/s modes select Allocation of time slot for BURST mode
32	PFCLE	I/O	TE/NT: 7.68-MHz clock out sync to line signal NT-PBX: 512-kHz clock out sync to line signal LT: Power feed off must be clamped to LOW if not used

Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
21	PS1	I	NT: Power status (primary)
22	PS2	I	NT: Power status (secondary)
18	PFC	I	Monitor power feed (active HIGH) serial data of power feed current
3	TSP	I	Test single pulses must be clamped to LOW if not used
28	RESQ	I	Power-on reset (active LOW) must be LOW at least 300 usec. The clock on the DCLK pin has to be applied during RESET in the LT-modes and in the NT-PBX-mode. Must be clamped to HIGH if not used.
27	DOUT	O	IOM-2 data output synchronous to DCLK
37	DISS	O	Disable supply (active HIGH)
19	RD1	O	Relay driver control (via IOM monitor)
20	RD2	O	Relay driver control (via IOM monitor)
29	TP	I	Test pin (must be clamped to LOW during normal operation)
44	TM0	I/O	Test pin (must be clamped to HIGH during normal operation)
43	TM1	I/O	Test pin (must be clamped to HIGH during normal operation)
42	TM2	I/O	Test pin (must be clamped to HIGH during normal operation)
41	TM3	I/O	Test pin (must be clamped to HIGH during normal operation)
30	TM4	I/O	TE mode (HIGH) Auto mode (LOW)
39	TM5	I/O	Test pin (must be clamped to HIGH during normal operation)
38	TM6	I/O	Test pin (must be clamped to HIGH during normal operation)
17	TP2	O	Test pin

Slot Assignment

TM4	BURST	LT	SLOT0	SLOT1	SLOT2	Mode		SFR Marker on FSC
0	0	0	0	0	0	NT	automode	no
0	0	0	0	1	0	TE	automode	no
0	0	0	1	0	0	NT	automode	yes
0	0	0	1	1	0	TE	automode	yes
0	1	0	slot assignment			PBX	automode	
0	1	1	slot assignment			LT	automode	
1	0	0	0	0	0	NT	transparent	no
1	0	0	0	1	0	TE	transparent	no
1	0	0	1	0	0	NT	transparent	yes
1	0	0	1	1	0	TE	transparent	yes
1	1	0	slot assignment			PBX	transparent	
1	1	1	slot assigment			LT	transparent	

Time Slot No.	SLOT0	SLOT1	SLOT2	Bit No.
0	0	0	0	0..31
1	0	0	1	32..63
2	0	1	0	64..95
3	0	1	1	96..127
4	1	0	0	128..159
5	1	0	1	160..191
6	1	1	0	192..223
7	1	1	1	224..255

Interfaces of the IEC-Q

The specifications for the U interface with respect to layer-1 maintenance functions are based on the "T1 Basic Access Interface for Application at the Network Side of NT-Layer-1". The IOM-2 interface is described in the "ISDN Oriented Modular Interface Specification.

U Interface

Frame Structure

		FRAMING	2B+D	Overhead Bits (M1-M6)					
	Quat Positions	1-9	10-117	118s	118m	119s	119m	120s	120m
	Bit Positions	1-18	19-234	235	236	237	238	239	240
Super Frame #	Basic Frame #	Sync Word	2B+D	M1	M2	M3	M4	M5	M6
1	1	ISW	2B+D	eoc_{a1}	eoc_{a2}	eoc_{a3}	atc / act	1	1
	2	SW	2B+D	eoc_{dm}	eoc_{i1}	eoc_{i2}	dea / ps1	1	febe
	3	SW	2B+D	eoc_{i3}	eoc_{i4}	eoc_{i5}	1 / ps2	crc_1	crc_2
	4	SW	2B+D	eoc_{i6}	eoc_{i7}	eoc_{i8}	1 / ntm	crc_3	crc_4
	5	SW	2B+D	eoc_{a1}	eoc_{a2}	eoc_{a3}	1 / cso	crc_5	crc_6
	6	SW	2B+D	eoc_{dm}	eoc_{i1}	eoc_{i2}	1	crc_7	crc_8
	7	SW	2B+D	eoc_{i3}	eoc_{i4}	eoc_{i5}	1	crc_9	crc_{10}
	8	SW	2B+D	eoc_{i6}	eoc_{i7}	eoc_{i8}	1	crc_{11}	crc_{12}
2,3,...									

LT-to-NT direction — NT-to LT direction

"1" = reserve = reserve bit for future standard; set = 1
eoc = embedded operations channel
a = address bit
dm = data/message indicator
i = information (data/message)

act = activation bit
ps1, ps2 = power status bits
ntm = Nt1 in test mode bit
crc = cyclic redundancy check
covers 2B+D & M4
febe = far end block error bit

2B1Q superframe technique & overhead bit assignments
(8x1.5 ms "basic frames" = 12 ms superframe)

Embedded Operation Channel (EOC)

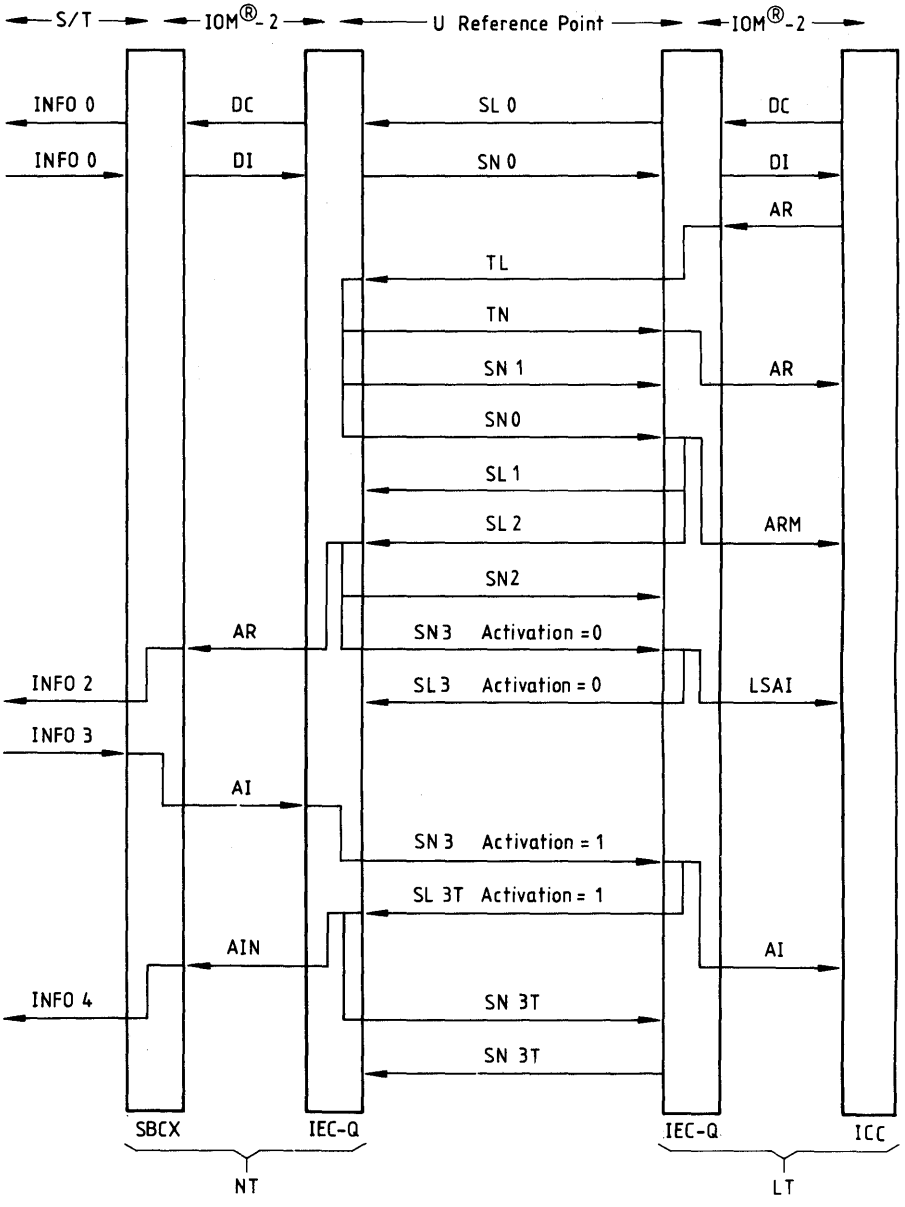
24 bits per superframe are allocated to an embedded operation channel supporting operation communication between network and NT. Two EOC frames of 12 bits are contained within a superframe:

$a_1 - a_3$	dm	$i_1 - i_8$		(o) Origin. (d) Dest.		Message
Address Field	**Data/Msg Indicator**	**Info**	**Field**	**LT**	**NT**	
000						NT Address
111						Broadcast
	1					Message
	0					Data
		0101	0000	o	d	Operate 2B+D Loopback
		0101	0001	o	d	Operate B1 Loopback
		0101	0010	o	d	Operate B2 Loopback
		0101	0011	o	d	Request Corrupted CRC
		0101	0100	o	d	Notify of Corrupted CR
		1111	1111	o	d	Return to Normal
		0000	0000	d/o	o/d	Hold State
		1010	1010	d	o	Unable to Comply
						Acknowledgement

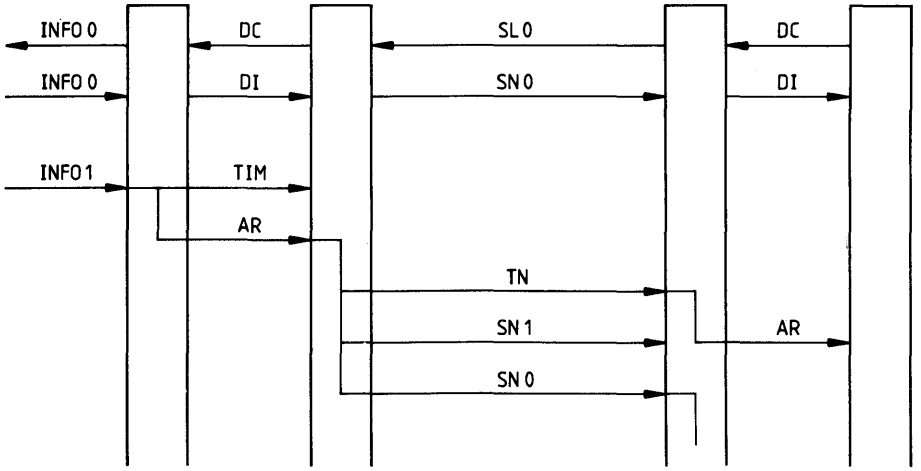
Activation and Deactivation Procedures

Activation occurs either by the LT or NT side.
Deactivation starts always from the LT side.

Activation from LT

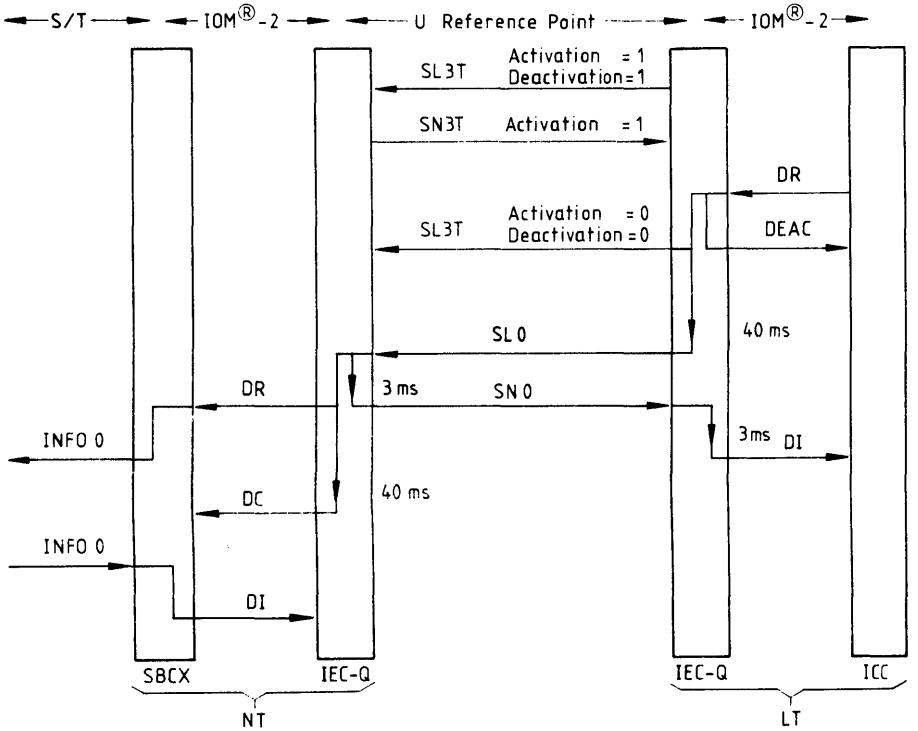


Activation from NT



the following as on previous page

Deactivation Procedure

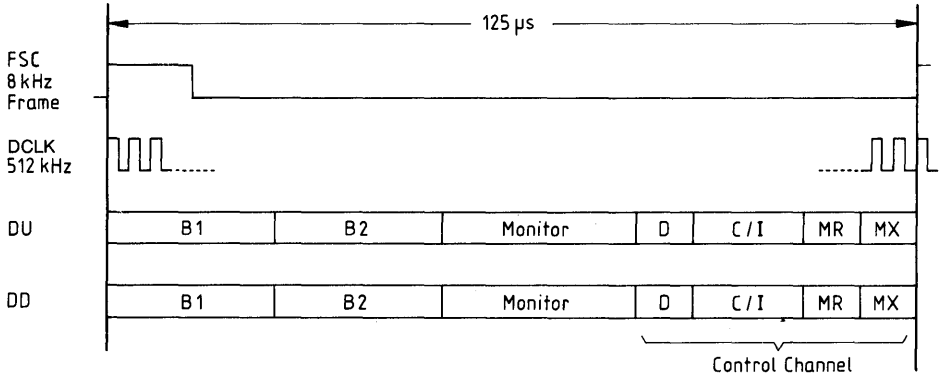


Signal	Synch Word	Super Frame	2B+D	M
TN	+−3	+−3	+−3	+−3
SN0	No Signal	No Signal	No Signal	No Signal
SN1	Present	Absent	1	1
SN2	Present	Absent	1	1
SN3	Present	Present	1	Normal
SN3T	Present	Present	Normal	Normal
TL	+−3	+−3	+−3	+−3
SL0	No Signal	No Signal	No Signal	No Signal
SL1	Present	Absent	1	1
SL2	Present	Present	0	Normal
SL3T	Present	Present	Normal	Normal

* TL/TN alternate +−3 for 10-kHz tone
* SN_x signal from NT to LT
* SL_x signal from LT to NT

The IOM-2 Interface

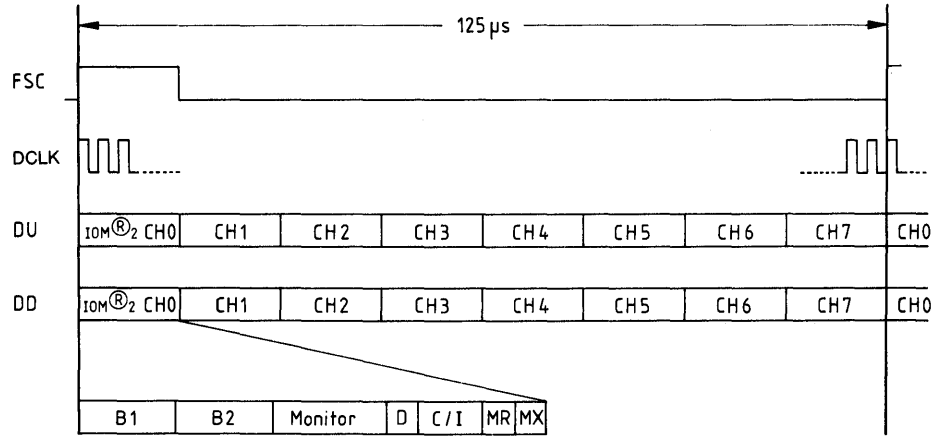
The Frame Structure of IOM-2



B1, B2: Circuit switched voice/data
D: D-channel for signaling and packet switched data
C/I: Command/indication bits for control
MR, MX: Monitor handshake bits

* DCL is programmable for values from 512 kHz to 8.192 MHz

Multiplexed Frame Structure of the IOM-2 Interface (shown for 2.048 kbit/s)



The IOM-2 Interface Monitor Channel

The monitor channel of the IOM-2 interface is designed for safe message oriented data transfer including rate adaption and synchronization features. The dedicated transfer procedure enables the link of several bytes to multi-byte message. For easy identification of the messages, each one starts with a four bit field indicating the structure of the following data. For ISDN basic access layer-1 maintenance four identifier codes are used within the IEC-Q:

MON-0	0 0 0 0	for U interface eoc message
MON-1	0 0 0 1	for S/T interface S1/Q messages and one part of U interface single maintenance bits.
MON-2	0 0 1 0	for the second part of U interface single maintenance bits and the S/T interface S2 channel
MON-8	1 0 0 0	for local messages

if unspecified codes are passed, their receipt is acknowledged, but disregarded by the chip.

EOC Messages on the IOM-2 Interface

The twelve bit eoc messages are transferred over the IOM interface in two monitor channel bytes according to the following structure (cf. T1 U interface specification)

MON-0

0 0 0 0 a a a d	e e e e e e e e

a: address, d: d/m bit, e: eoc command

This monitor message is transferred either only once and then handled autonomously by the device.

Code repetition is performed within the chip by EOC processor.

Only one pending command is allowed, i.e. one may pass (valid for MON- and EOC-channel).

Single Maintenance Bits of the U Interface on the IOM Interface

There are twelve single maintenance bits defined. Some of them have a relationship to the S/T interface such as NTM or FEBE, others are assigned to the layer-1 activation procedure. As a consequence, some are transferred with the identifier "0001" to link U and S/T interfaces maintenance functions, others are transferred separately:

MON-1

0 0 0 1 0 0 0 0	s s s s 1 - - m

s: S1/Q code, m: NTM polarity

S1/Q code	NT		LT	
	d	u	d	u
1 1 1 1		NORM	–	–
0 0 0 1	–	ST	–	–
0 0 1 0	STP	–	–	–
0 1 0 0	FEBE	–	–	–
1 0 0 0	NEBE	–	–	–
1 1 0 0	FNBE	–	–	–

d: Downstream (LT-TE), u: Upstream (TE-LT)

ST: Self test

STP: Self test pass

FEBE, NEBE, FNBE indicates block errors

MON-2

				M_{41}	M_{51}
0	1	1	0	M_{61}	M_{42}

M_{52}	M_{62}	M_{45}	M_{46}
M_{43}	M_{44}	M_{47}	M_{42}

Remaining M-bits (M_{xy}: M_x in frame y)

Local Messages

1	0	0	0	r	a	0	0

b	b	b	b	b	b	b	b

b: Local command

Possible local commands are:

RBEF: Read block error counter far end

RBEN: Read block error counter near end

RDi: Relay driver i activated

RECC: Read echo canceler coefficients

RID: Read identification

RPFC: Read power feed current value

The IEC-Q supplies the desired information in a two byte message with local address.

The IOM-2 Interface C/I Channel

C/I Channel Codes

Code	NT-Mode		LT-Mode	
	IN	OUT	IN	OUT
0000	TIM	DR	DR	–
0001	RES	–	RES	DEAC
0010	–	FJ	–	FJ
0011	–	–	LTD	HI
0100	SI1	EI1	RES1	EI1
0101	SSP	–	SSP	EI2
0110	DT	–	DT	INT
0111	–	PU	–	LSAI
1000	AR	AR	AR	AR
1001	–	–	–	ARM
1010	ARL	ARL	ARL	–
1011	–	–	–	–
1100	AI	AI	–	AI
1101	–	–	–	–
1110	–	AIL	–	–
1111	DI	DC	DC	DI

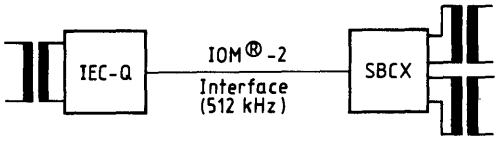
AIL	Activation Indication Local Loop
AI	Activation Indication
AR	Activation Request
ARL	Activation Request Local Loop
ARM	Activation Request Maintenance Bits
DC	Deactivation Confirmation
DR	Deactivation Request
DEAC	Deactivation Accepted
DI	Deactivation Indication
DT	Test Mode (Data Through)
EI1	Error Indication 1 (Error on U)
EI2	Error Indication 2 (Error on S/T)
HI	High Impedance (Set by Pin PFOFF)
INT	Interupt (Set by Power Controler)
LTD	LT Disable (Control of Pin DISS)
LSAI	Line System Activation Indication
RES	Circuit Reset
RES1	Receiver Reset
PU	Power Up
SSP	Test Mode (Send Single Pulses)
TIM	Timing Required

Application

Different hardware configurations as well as different operating modes of the device are selected to cope with different system requirements.

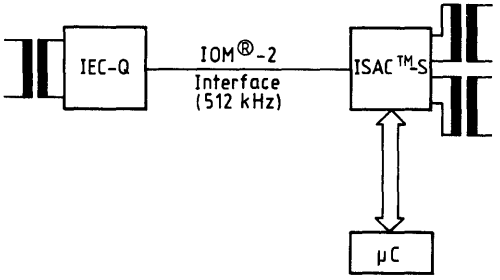
NT1 Mode

T1 S/T and U interface procedure specification by SBCX and IEC-Q



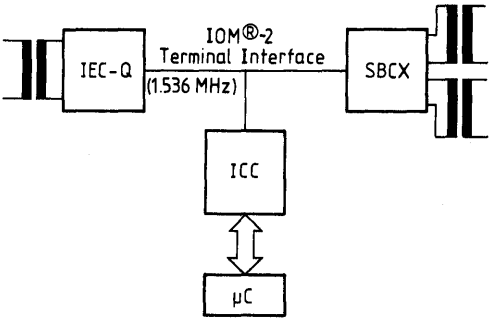
NT2 Mode

Using the ISAC-S together with the IEC-Q it is possible to handle all maintenance functions at the µC. The S1/Q bits are accessed directly in the specific ISAC™-S register, the U interface maintenance data are transferred via monitor channel to the µC. In this configuration, the IEC-Q can be programmed either in automode or in transparent mode.

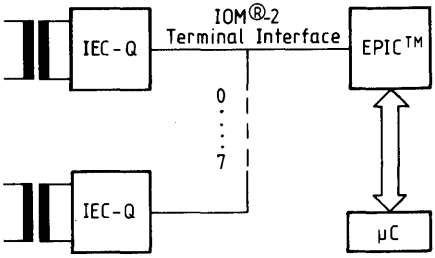


NT Mode, Handling the Complete S Channel

The SBCX is used to get access to the S channel. Since both SBCX and IEC-Q need a monitor channel for transfer of maintenance information to the ICC, a data clock of 1.536 MHz is required for the IOM interface (TE mode of IEC-Q). The SBCX occupies the monitor channel of the second IOM interface channel and runs in the transparent mode.

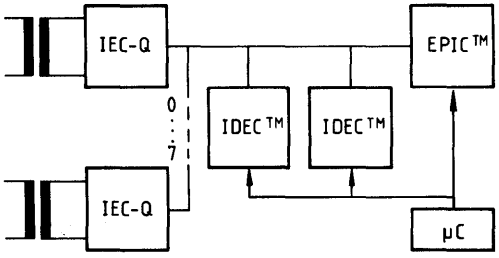


LT Line Termination in Public or Private Exchange or NT-PBX



The EPIC performs the control of voice, data and signaling for up to eight subscribers on digital line boards with one IOM-2 interface. Since every IEC-Q needs a monitor channel transfering maintenance information to the µP and a data-channel, a time-slot procedure with variable data clock up to 6.176 MHz is required. Each IEC-Q is assigned to one time and runs either in the auto-mode or in the transparent-mode.

Using the IDEC, Handling the D-Channel Protocol for up to Four Subscriber Lines.



SIEMENS

ISDN Burst Tranceiver Circuit (IBC) PEB 2095

Preliminary Data **CMOS IC**

Type	Ordering Code	Package
PEB 2095-C	Q67100-H8398	C-DIP-24
PEB 2095-N	Q67100-H8396	PL-CC-28 (SMD)
PEB 2095-P	Q67100-H8397	P-DIP-24

The PEB 2095 ISDN Burst Transceiver Circuit (IBC) is a half duplex transceiver for the 2-wire transmission line (CCITT U-reference point). Full duplex transmission is achieved using a time compression multiplex (ping-pong) technique. Furthermore, the device links the 2-wire transmission line to the ISDN Oriented Modular (IOM) interface and hence to the powerful Siemens ISDN device family. From the point of view of the OSI communications protocol model, the device manages layer-1 of the interface protocol and can communicate with other layer-1 or layer-2 devices over the IOM interface.

A second device, the PEB 2090 ISDN Echo Cancellation Circuit (IEC), may also be used at the U-reference point. The device chosen depends on the application. The IBC proves more cost-effective for shorter range transmission applications (2 – 3.5 km), especially PBX.

The IBC is available as a 24-pin CMOS device.

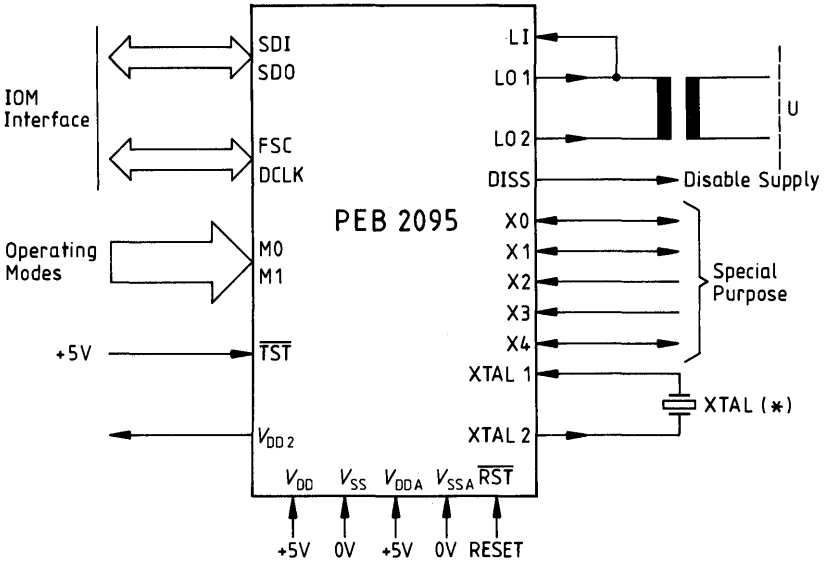
The device operates from a single 5-V power supply.

The maximum power consumption is 80 mW.

Features:

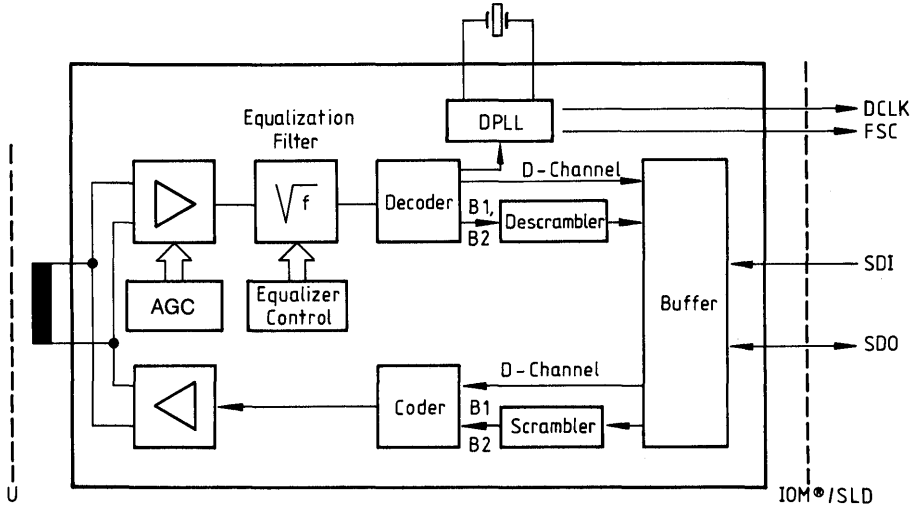
- Half duplex burst mode 2-wire U-interface transceiver
- Mode configurable to function at both ends of the line
- 144 kbit/s user bit rate (2B + D)
- 384-kHz line clock rate
- IOM compatible
- Clock and frame recovery
- Adaptive line equalization and amplification at receiver
- Implementation of activation/deactivation procedures
- Built-in wake-up function for activation from power down state
- Switching of test loops
- Typical length of loop: up to 3.5 km with 0.6 mm diameter wire
- Advanced CMOS technology
- Low power consumption: 6 mW power down
  80 mW power up (maximum)

Logic Symbol



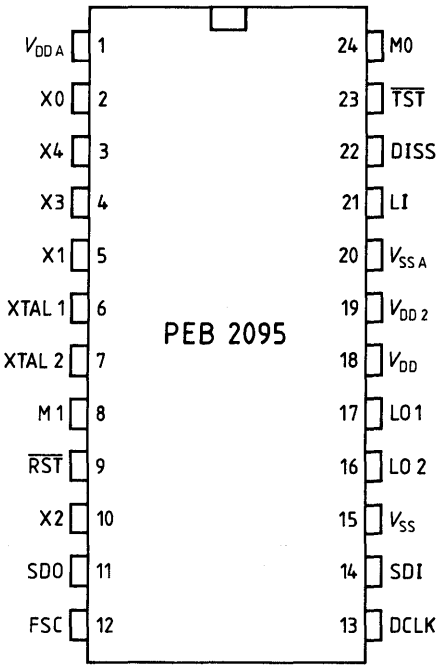
*) An external oscillator can also be used as a clock input to XTAL1.
In this configuration XTAL2 is not connected.

Block Diagram

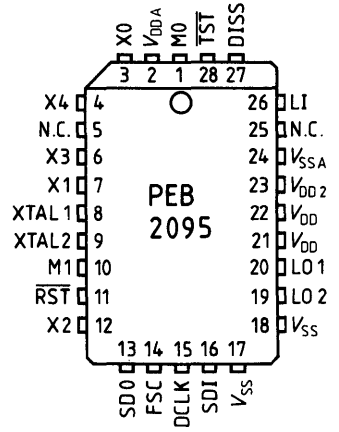


Pin Configurations
(top view)

P-DIP; C-DIP



PL-CC



*) XTAL2 not connected when external oscillator is used

Pin Definitions and Functions

Pin No. P-DIP	Pin No. PL-CC	Symbol	Input (I) Output (O)	Function
16	20	LO1		Line transmitter; output 1
17	19	LO2	O	Line transmitter; output 2 — U interface
21	26	LI	I	Line receiver
11	13	SDO	O	Serial data out
14	16	SDI	I	Serial data in — IOM interface
13	15	DCLK	I/O	Serial data clock
12	14	FSC	I/O	Frame sync.
24	1	M0	I	Operating mode setup pins
8	10	M1	I	
2	3	X0	I/O	Multifunctional pins; mode specific functions
5	7	X1	I/O	
10	12	X2	I	
4	6	X3	I	
3	4	X4	I/O	
6	8	XTAL1	I	External crystal or external oscillator input.
7	9	XTAL2	O	External crystal connection (n.c. when external oscillator is used).
23	28	$\overline{TST}$	I	Device test pin; not for general use; tie high always.
22	27	DISS	O	Disable supply
9	11	$\overline{RST}$	I	Hardware reset pin; active low
18	21, 22	V_{DD}	I	Digital power supply 5 V ± 5%
15	17, 18	V_{SS}	I	Digital ground
1	2	V_{DDA}	I	Analog power supply 5 V ± 5%
20	24	V_{SSA}	I	Analog ground
19	23	V_{DD2}	O	2.5 V output; connected to V_{DD} via 10 nF capacitor connected to V_{SSA} via 10 nF capacitor
	5; 25	N.C.		Not connected internally

System Integration

There are three operating modes:

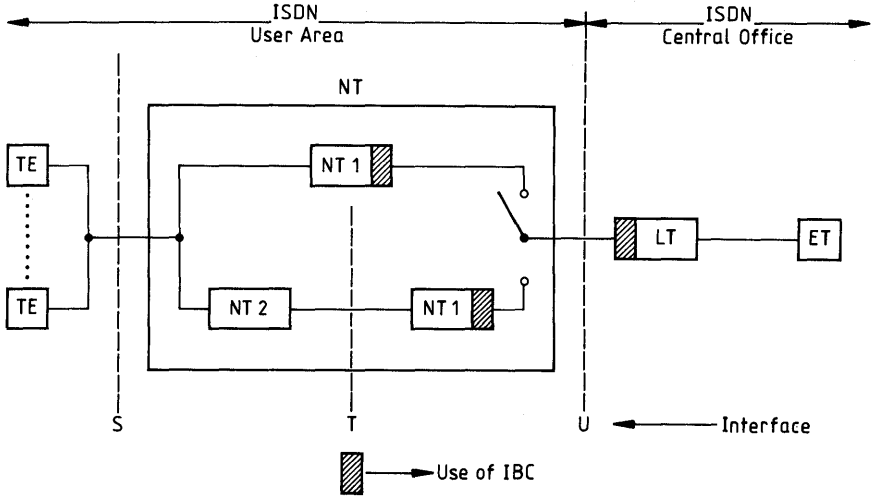
LT: Line Termination i.e. in the Local Exchange/PBX
TE: Terminal Equipment i.e. in the Subscriber Terminal
NT: Network Termination

Two examples of LT mode are illustrated, one connected directly to the terminal, one connected to a network termination. In the latter case, the terminal is connected over the S interface for the network termination. Because of the multiplexing facility on the S-bus to eight terminals may be connected to one network termination and hence to one subscriber line. In the former case (without a network termination) only one terminal per subscriber line is possible. The diagram also indicates that either the IBC or the IEC may be used for 2-wire transmission. Choice is dependent upon the transmission line characteristics, but in general the IBC is the more cost-effective for shorter range transmission applications (especially PBX).

In the LT mode, the IBC managers layer-1 functions and communicates over the IOM interface with the ICC (ISDN Communication Controller) which handles most layer-2 functions. A microprocessor (handling higher layer functions) controls and communicates with the ICC. A similar configuration is required in the TE mode, employing the same division of tasks.

In the NT mode, however, the configuration is much different. In this case the network termination is acting as an NT1 (according to CCITT notation). **Figure 1** illustrates two possible NT configurations.

Figure 1
NT Configuration



In both cases, NT1 refers to a simple layer-1 translation between the U interface and the S/T interface. This is achieved by the simple pairing of the IBC with an IOM compatible S-bus interface circuit (e.g. the SBC PEB 2080).

In this configuration, no ICC or microprocessor is required because layer-2 and higher are passed transparently through NT1. The IOM interface acts as an intermediate interface common to both devices.

On the other hand NT2 in **figure 1** differs from NT1 in that it includes higher level OSI functions. It could, for example, be a PBX. In this case the PBX would be connected directly over the S interface (not U interface) to the subscriber terminal(s).

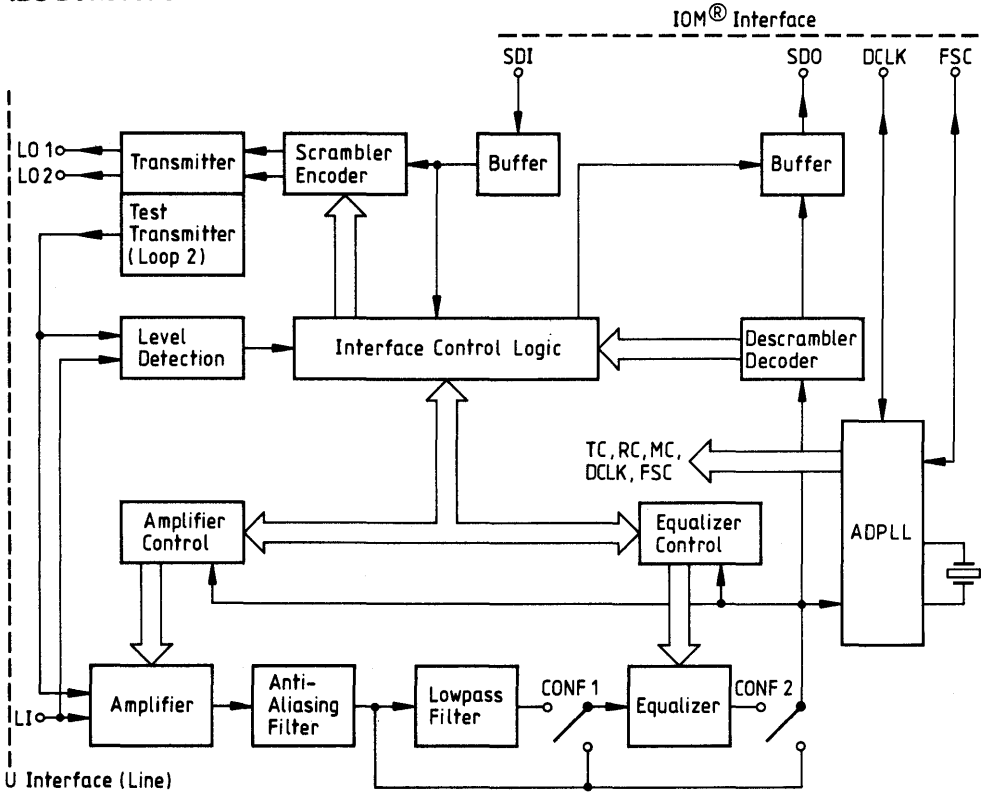
Note: **Figure 1** illustrates the CCITT defintion of the U reference point i.e. between a local exchange and a network termination. The direct connection of terminals to a PBX over a 2-wire loop is not considered by CCITT since it is not in the public network domain. Since the IBC can be used in both the aforementioned configurations, this document, for simplicity, will use the term U reference point for both. Furthermore the term U interface will refer only to the time division multiplexing technique for transmission over a 2-wire loop.

Functional Description

IBC Device Architecture and General Functions

The ISDN Burst Transceiver Circuit (IBC PEB 2095) performs the layer-1 functions of the time-division multiplex implementation of the U interface. This is a half duplex technique (ping-pong) involving transmission by only one device at any one time. Furthermore the IBC acts a link between the U interface to the IOM interface and hence to other layer-1 or layer-2 devices within the system. **Figure 2** depicts the device architecture.

Figure 2
IBC Device Architecture



TC = Transmitter Clock
RC = Receiver Clock
MC = Master Clock

Some of the relationships between the blocks of the device architecture and the IBC functions outlined below can be traced at this stage. This section, however, will deal in more detail with these relationships.

The following are the main functions of the IBC

- Activation/deactivation procedures. Activation may be initialized by either infos from the line or primitives from the IOM interface
- To increase the quality of signal received from the line, the receiver stage contains both an adaptive amplifier and equalizer
- Synchronous timing must be maintained on both sides of the device. All internal clocks are synchronized to the upstream data clock (system clock). All generated downstream clocks are synchronized, in turn, to these internal clocks.
- Testing and diagnostic functions: Testloops may be closed, test signals may be generated.

Furthermore, the IBC must also link 2 different interfaces, the IOM interface and the U interface. To do this transparently, the IBC must compensate for the following main differences between them:

- The U interface is a burst mode interface while the IOM interface is continuous
- The frame structure and data transmission techniques on both interfaces are different
- The B channels are scrambled on the U interface and unscrambled on the IOM interface
- The clock rates are different and are transmitted in a different manner. In the U interface the clock is implicit in the data stream; in the IOM interface 2 separate clocks, DCLK and FSC, must be provided.

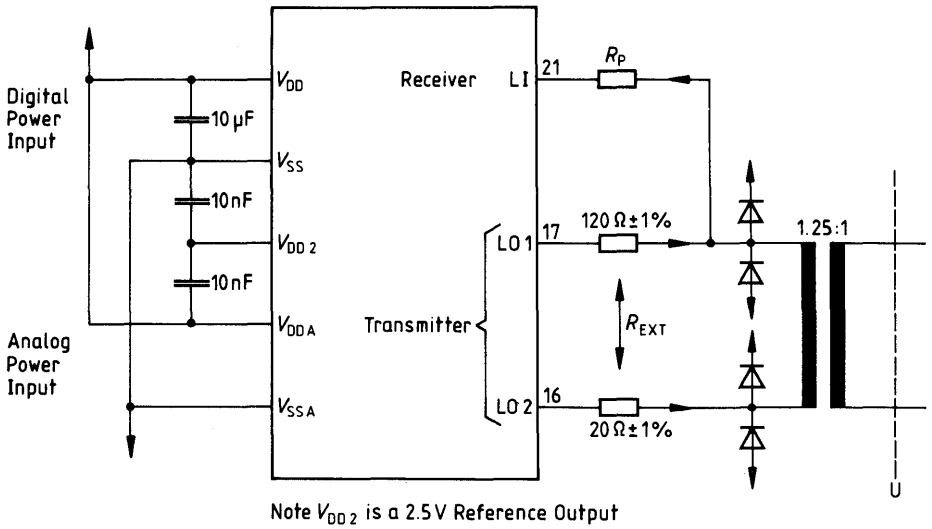
Analog Functions

Figure 3 depicts the analog and power connections to the IBC. Both analog and digital power may be connected to a single power source. The reference voltage V_{DD2} must be linked by two 10 nF capacitors to V_{SS} and V_{DDA}. External to the transmitter and receiver a transformer (ratio 1.25:1) and external resistance (R_{EXT} = 140 Ω ± 1%) are connected as shown. Voltage overload protection is achieved by splitting R_{EXT} into 120 Ω and 20 Ω (for current limitation) and adding clamping diodes. If required a resistor may be added to the signal input line for current limitation.

The transmitter stage is realized as a voltage source with an internal resistance R_i = 15 Ω ± 40%. It delivers a pulse of amplitude 2 V ± 10% (0-to-peak). Assuming a transformer winding resistance of the order of 1 Ω, the output resistance seen from the U interface will be 100 Ω.

Referring again to **figure 2**, the receiver input stages can be seen. They consist of a variable gain amplifier, to compensate for signal losses on the line (dynamic range 30 dB). This is followed by an anti-aliasing filter and a switched capacitor low pass filter. Finally a switched capacitor equalizer suppresses the out-of-band noise, which has passed the (anti-aliasing) filter stage, while keeping the pulse distortion low (dynamic range 15.36 dB).

Figure 3
IBC Analog Connections



Note V_{DD2} is a 2.5V Reference Output

Both the amplifier and the equalizer are adaptive. The amplifier has 128 possible settings and the equalizer 8 (in this sense they are digital). The adaptive logic can be stopped by externally setting the amplifier and equalizer over the IOM interface. Once set in this way, the settings remain constant. The monitor channel can also be used to program some other functions.

The level detection block monitors the receive line and informs the interface logic when an incoming signal is present. It also monitors the test transmitter to perform a similar function during test loop implementation.

Digital Functions

The DPLL circuitry works with an external oscillator or crystal of 15.36 MHz ±100 ppm. This is used to synchronize all bit and frame clocks with the incoming system clock (i.e. from upstream). In the LT mode, the system clock is supplied over the IOM interface. Generation of half-bauded AMI pulses for the line is accomplished by deriving a synchronous transmitter clock using the DPLL. At the NT/TE end of the line, the data clock of 384 kHz is implicitly received in the data stream and is extracted by the IBC. From this all synchronous clocks are derived with the aid of the DPLL.

An incorporated finite state machine controls ISDN layer-1 activation/deactivation. This includes wake signal recognition in the "deactivated" state.

Due to the burst nature of U interface communication and the continuous nature of communication on the IOM interface, a buffer memory is required to compensate for timing differences.

The digital control logic also sets the adaptive coefficients on the AGC amplifier and the SC equalization filter.

Scrambler/Descrambler

B channel data on the U interface is scrambled to give a flat continuous power density spectrum and to ensure enough pulses are present on the line for a reliable clock extraction to be performed at the downstream end.

The IBC therefore, contains a scrambler and descramber, in the transmit and receive directions respectively. The basic form of these are illustrated in **figure 4** and **figure 5**.

The form is in accordance with the CCITT V.27 scramber/descrambler and contains supervisory circuitry which ensures no periodic patterns appear on the line.

Figure 4
IBC Scrambler

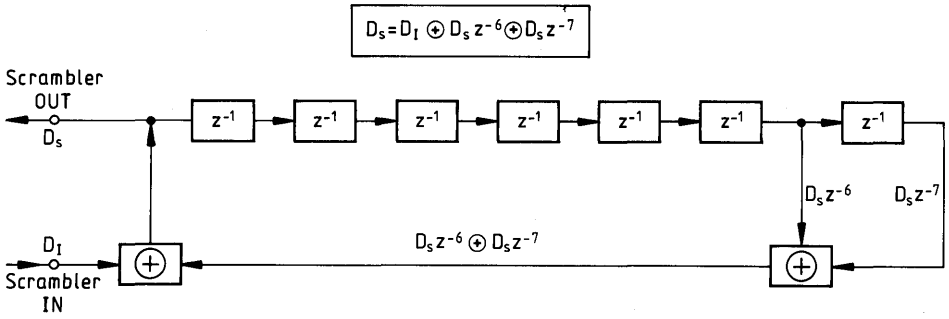
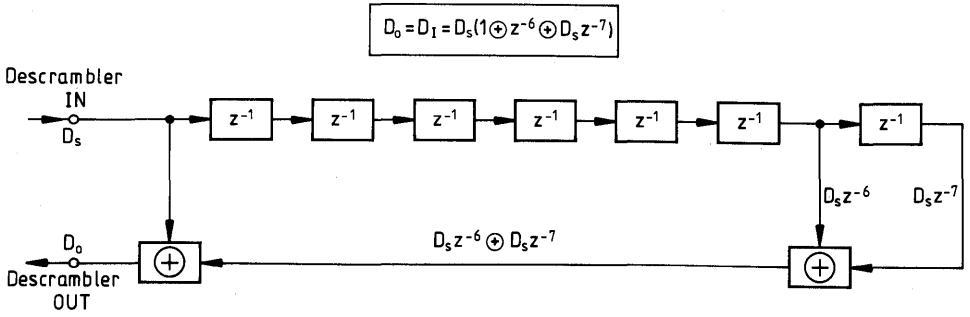


Figure 5
IBC Descrambler



Interfaces

The IBC operates 3 interfaces:

- U interface
- IOM interface
- SLD interface

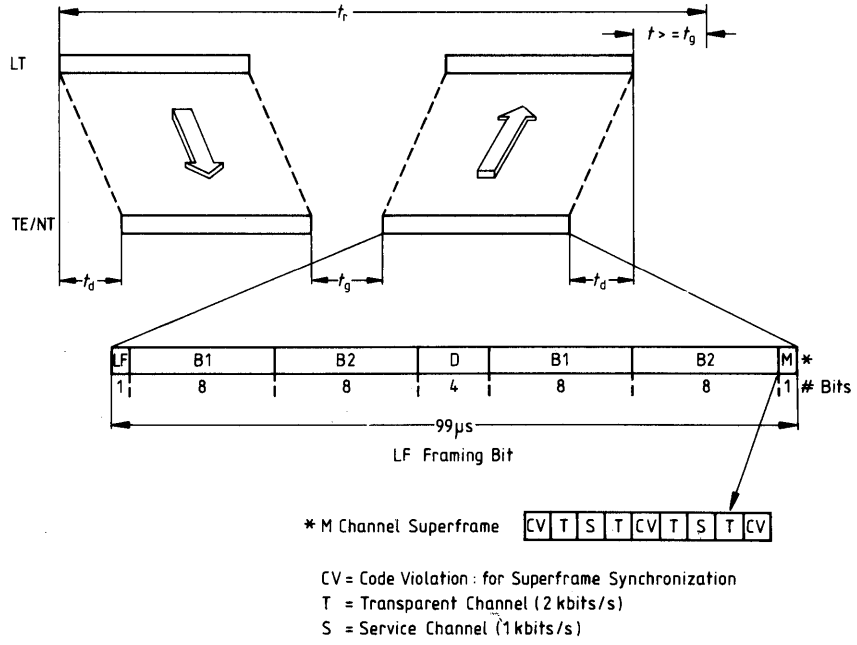
U Interface

Figure 6 demonstrates the general principles of the U interface burst mode communication technique. A frame transmitted by the exchange (LT) is received by the terminal equipment (TE) after a given propagation delay. The terminal equipment waits a minimum guard time (5.2 µs) while the line clears. It then transmits a frame to the exchange. The exchange will begin a transmission every 250 µs (known as the burst repetition period). However, the time between the reception of a frame from the TE and the beginning of transmission of the next frame by the LT must be greater than the minimum guard time. Communication between an LT and an NT follows the exact same procedure.

Within a burst, the data rate is 384 kbit/s and the 38-bit frame structure is as shown in **figure 4**. The framing bit (LF) is always logical "1". The frame also contains the user channels (2B + D). Note that the B channels are scrambled. It can readily be seen that in the 250 µs burst repetition period, 4 D bits, 16 B1 bits and 16 B2 bits are transferred in each direction. This gives an effective full duplex data rate of 16 kbit/s for the D channel and 64 kbit/s for each B channel.

The final bit of the frame is called the M bit. Four successive M bits, from four successive U frames, constitute a superframe **(figure 6)**. Three signals are carried in this superframe. Every fourth M bit is a code violation (CV) and is used for superframe synchronization. This can be regarded as the first bit of the superframe. From this reference, bit 3 of the superframe is the service channel bit (S). The S channel bit is transmitted once in each direction in every fourth burst repetition period. Hence the duplex S channel has a data rate of 1 kbit/s. It conveys test loop control information from the LT to the TE/NT and reports of transmission errors from the TE/NT to the LT. Bit 2 and bit 4 of the superframe are T bits. These constitute the 2 kbit/s T channel which extends the T channel of the IOM frame **(figure 7)** onto the U interface.

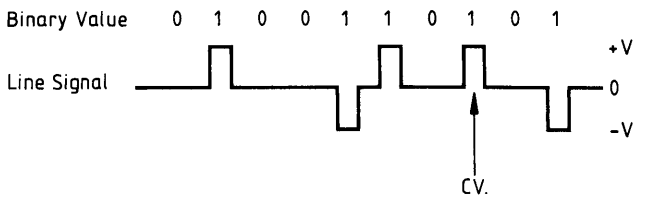
Figure 6
U Interface Transmission/Reception



Timings : t_r = Burst Repetition Period = 250 µs
t_d = Line Delay = 20.8 µs max.
t_g = Guard Time = 5.2 µs min.

The coding technique used on the U interface is half-bauded AMI code (i.e. with a 50% pulse width). **Figure 7** illustrates the code. As can be seen, a logical '0' corresponds to a neutral level, a logical '1' is coded as alternate positive and negative pulses. The figure also illustrated how a code violation may be achieved (CV); either two successive positive (as shown) or negative pulses.

Figure 7
Half-Bauded AMI Code



Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Ambient temperature under bias	T_A	0 to 70	°C
Storage temperature	T_{stg}	−65 to 125	°C
Voltage on any pin with respect to ground	V_S	−0.3 to V_{DD} +0.3	V

Line Overload Protection

The maximum input current (under overvoltage conditions) is given as a function of the width of a rectangular input current pulse **(figure 8).**

Figure 8

Test Condition for Maximum Input Current

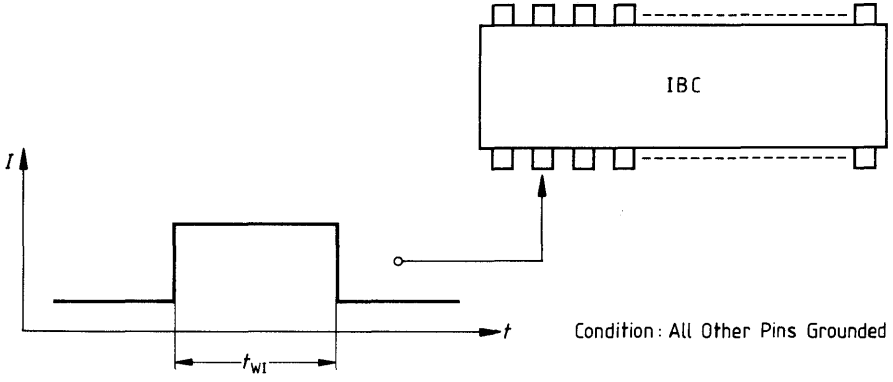


Figure 9

Transmitter Input Current

The destruction limits are given in **figure 9**
$R_1 \geq 250\ \Omega$.

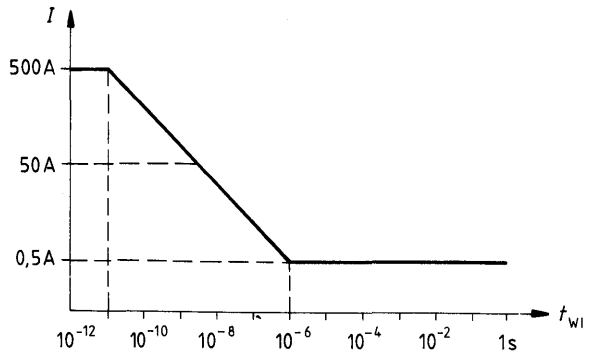
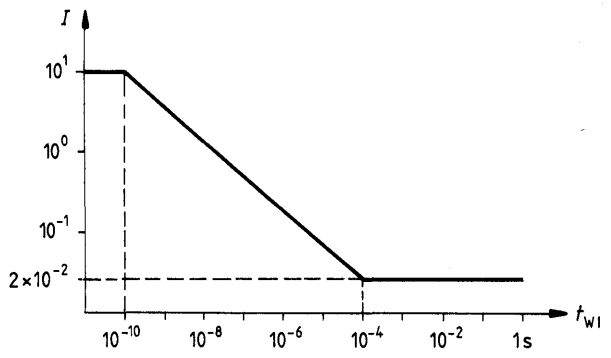


Figure 10

Receiver Input Current

The destruction limits are given in **figure 10**
$R_1 \geq 250\ \Omega$.



DC Characteristics

$T_A = 0$ to 70 °C; $V_{DD} = 5\ V \pm 5\%$; $V_{SS} = 0\ V$; $V_{SSA} = 0\ V$

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit	Test Conditions	Remarks
L-input voltage	V_{IL}	V_{SS}-0.4	0.8	V		
H-input voltage	V_{IH}	2.0	V_{DD}+0.4	V		
L-output voltage[1)] L-output voltage[2)]	V_{OL1} V_{OL2}		0.45 0.45	V V	$I_{OL} = 2$ mA $I_{OL} = 7$ mA	All pins except L01,2 LI XTAL1 XTAL2
H-output voltage H-output voltage	V_{OH} V_{OH}	2.4 V_{DD}-0.5		V V	$I_{OH} = -400\ \mu A$ $I_{OH} = -200\ \mu A$	
Power supply current operational Power supply current power down	I_{CC} I_{CC}		13 1.3	mA mA	$V_{DD} = 5$ V, inputs at 0 V or V_{DD}, no output loads.	
Input leakage current	I_{LI}		10	µA	$0V < V_{IN} < V_{DD}$ to 0V	
Output leakage current	I_{LO}		10	µA	$0V < V_{OUT} < V_{DD}$ to 0V	
Absolute value of[3)] output pulse amplitude[4)] ($V_{L01} - V_{L02}$)[5)]	V_X	4.45 −5.25 0	5.25 −4.45 0	V V V	$I_O \le 16$ mA $I_O \le 16$ mA $I_O = 0$	L01,2
Pulse width	P_W	1.22	1.38	µs		
Transmitter output impedance	R_X	9	21	Ω		
L-input voltage H-input voltage	V_{IL} V_{IH}	V_{DD}-0.5 V_{DD}-0.5	0.5	V V		XTAL1
L-output voltage H-output voltage	V_{OL} V_{OH}	 V_{DD}-0.5	0.5	V V	$I_O \le 100\ \mu A$ $C_L \le 100$ pF	XTAL2

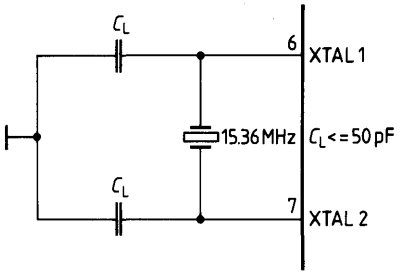
Notes: 1) All outputs except SDO
2) Output SDO only
3) Positive pulse
4) Negative pulse
5) No pulse

Capacitances

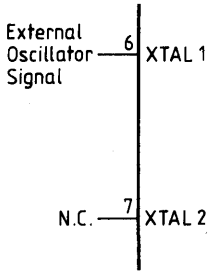
$T_A = 0$ to 70 °C; $V_{DD} = 5\ V \pm 5\%$; $V_{SS} = 0\ V$; $V_{SSA} = 0\ V$

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Input capacitances Output capacitance	C_{IN} C_{IO}		7 7	pF pF	
Output capacitance against V_{SSA}	C_{OUT}		10	pF	L01,2
Load capacitance	C_L		50	pF	XTAL1,2

Figure 11
Recommended Oscillator Circuits



Crystal Oscillator Mode



Driving from External Source

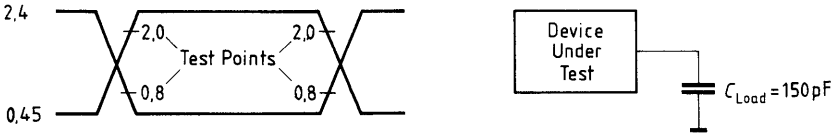
AC Characteristics

$T_A = 0$ to 70 °C, $V_{DD} = 5\ V \pm 5\%$

Inputs are driven at 2.4 V for a logic "1" and at 0.4 V for a logic "0". Timing measurements are made at 2.0 V for a logic "1" and at 0.8 V for a logic "0".

The AC testing input/output waveforms are shown below.

Figure 12
Input/Output Waveform for AC Tests



Clock Timing

The following timing-descriptions summarizes the clocks produced in the different operating modes and their respective duty cycles. The table also indicates which clocks are derived directly from the crystal and which are synchronized to the line using the on-board DPLL circuitry.

Table 1
Mode Specific Pin Functions

Mode	Name	Description	Pin	I/O	Function
LT	PFOFF	Power Feed OFF	X4	I	Puts the IBC into a powerfeed off state. This state is indicated by C/I code HI.
LT	MPF	Main Power Feed	X3	I	The 8-bit supply current equivalent is read serially through this pin into I (7:0) from the local power supply. The read is synchronous to the B1 channel in the IOM frame (time slot 0 in LT:mux mode). Used for power supply control by the layer-2 device. Tie low when not in use.
TE/NT	$\overline{\text{ENCK}}$	Enable Clocks	X3	I	Enables clocks in 'deactivated' state. Also during RST = 0, outputs are low impedance when $\overline{\text{ENCK}}$ = 0 and high impedance otherwise.
NT	$\overline{\text{SSP}}$	Send Single Pulses	X1	I	Test mode 1
	$\overline{\text{SCP}}$	Send Contin. Pulses	X2	I	Test mode 2
LT norm. or SLD	CONF4	Programmable Output Pin	X0	O	Programmed over monitor channel. Useful to control other devices.
LT	TS0-2	Time Slot 0 – 2	X0, 1,2	I	In MUX mode, one of eight possible time slots is selected to be read by the device (TS0 – LSB)

Figure 13
Output Clock Relationships

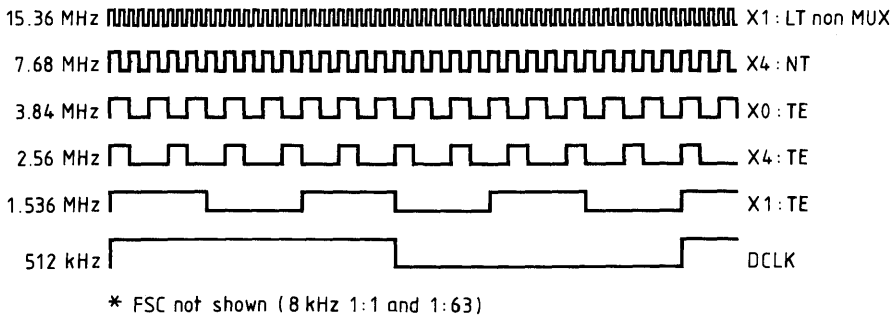


Figure 13 shows the relationship between the various clock outputs form the IBC. The crystal frequency is 15.36 MHz. All clock outputs have a duty cycle of 1:1 except 2.56 MHz (1:2). Note that the following are derived directly from the crystal oscillator; 15.36 MHz, 3.84 and 2.56 MHz. They are not synchronized to the line. Their accuracy will be, to a first order, governed by the crystal accuracy (± 100 ppm maximum).

The following clocks are derived both from the crystal and, with the help of the DPLL, from the line; 7.68 MHz, 1.536 MHz, DCLK and FSC. Synchronization may be regarded as a two stage process. Firstly, a synchronous 7.68 MHz signal is derived using the DPLL. Secondly, all other syncronous clocks are derived, by simple division, from 7.68 MHz synchronous. Because of the internal method of synchronization employed, the 7.68 MHz signal may "step forward or back" by 1 crystal period **(see figure 14)**. Hence the period of 7.68 MHz, and all synchronous clocks derived from it, may vary by one crystal period (± 65 ns). This, to a first order, gives the accuracy of the various synchronous clocks. **Table 2** to **table 6** detail the accuracy of the clock outputs with respect to the symbols.

Figure 14
Possible 7.68 MHz Clocks

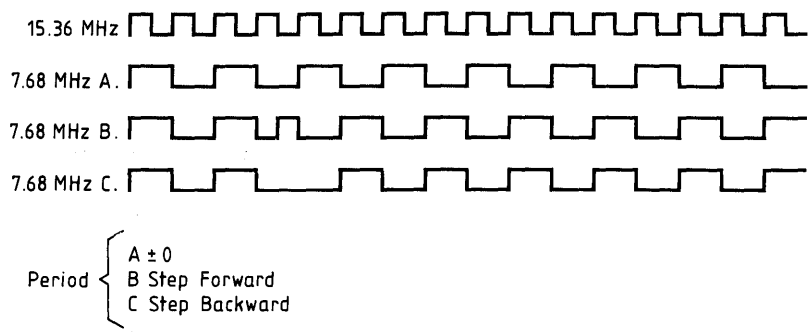


Figure 15
Clock Timing Symbols

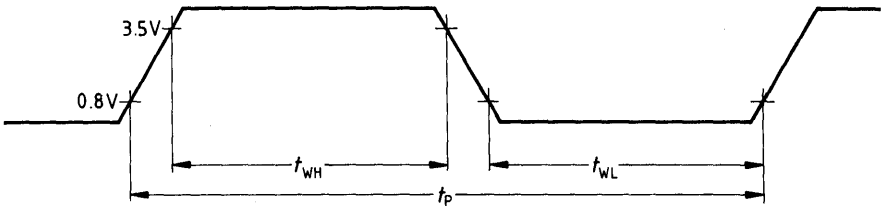


Table 2
DCLK Timing

Parameter	Symbol	Limit Values min.	typ.	max.	Unit	Test Conditions
TE/NT 512 kHz	t_P	1888	1953	2019	ns	Output
TE/NT 512 kHz	t_{WH}	944	977	1009	ns	
TE/NT 512 kHz	t_{WL}	944	977	1009	ns	
LT mode	t_{WH}	90			ns	Input
LT mode	t_{WL}	90			ns	

Table 3
FSC Timing

Parameter	Symbol	Limit Values min.	typ.	max.	Unit	Test Conditions
TE/NT 8 kHz 1:1	t_P	124.93	125	125.07	µs	Output
TE/NT 8 kHz 1:1	t_{WH}	62.46	62.5	62.54	µs	
TE/NT 8 kHz 1:1	t_{WL}	62.46	62.5	62.54	µs	
TE (SEL) 8 kHz 63:1	t_P	124.93	125	125.07	µs	
TE (SEL) 8 kHz 63:1	t_{WH}	122.08	123.05	124.02	µs	
TE (SEL) 8 kHz 63:1	t_{WL}	1888	1953	2019	ns	

Table 4
X4 Clock Timing

Parameter	Symbol	Limit Values min.	typ.	max.	Unit	Test Conditions
TE 2.56 MHz 1:2	t_P	−100	390	+100	ns	OSC ± 100 ppm
TE 2.56 MHz 1:2	t_{WH}	−100	130	+100	ns	OSC ± 100 ppm
TE 2.56 MHz 1:2	t_{WL}	−100	260	+100	ns	OSC ± 100 ppm
NT 7.68 MHz 1:1	t_P	65	130	196	ns	
NT 7.68 MHz 1:1	t_{WH}	65	65	131	ns	
NT 7.68 MHz 1:1	t_{WL}	65	65	131	ns	

Table 5
X1 Clock Timing

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
TE: 1.536 MHz	t_P	585	651	717	ns	
TE: 1.536 MHz	t_{WH}	260	326	391	ns	
TE: 1.536 MHz	t_{WL}	260	326	391	ns	
LT* 15.36 MHz	t_P	−100	65.1	+100	ns	OSC ± 100 ppm
LT* 15.36 MHz	t_{WH}	−100	65.1	+100	ns	OSC ± 100 ppm
LT* 15.36 MHz	t_{WL}	−100	65.1	+100	ns	OSC ± 100 ppm

* in normal and SLD modes only

Table 6
X0 Clock Timing

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
TE: 3.84 MHz	t_P	−100	260	+100	ns	OSC ± 100 ppm
TE: 3.84 MHz	t_{WH}	−100	130	+100	ns	OSC ± 100 ppm
TE: 3.84 MHz	t_{WL}	−100	130	+100	ns	OSC ± 100 ppm

Finally table 7 defined the rise and fall times of DCLK and FSC clocks in the various modes.

Table 7
DCLK/FSC Rise and Fall Timing

Parameter	Symbol	Limit Values			Unit	Mode
		min.	typ.	max.		
TRD; DCLK rise time	t_r			50	ns	NT/TE
				60	ns	LT normal
				25	ns	LT MUX
TFD; DCLK fall time	t_f			50	ns	NT/TE
				60	ns	LT normal
				25	ns	LT MUX
TFR; FSC rise time	t_r			50	ns	NT/TE
				60	ns	LT normal
				50	ns	LT MUX
TFF; FSC fall time	t_f			50	ns	NT/TE
				60	ns	LT normal
				50	ns	LT MUX

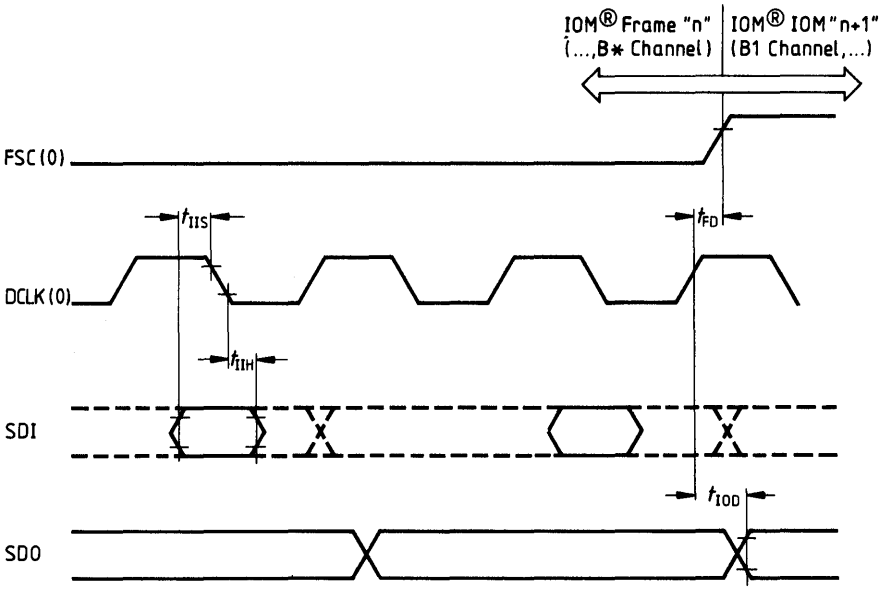
IOM Interface

Given the clock accuracies defined in the previous section, the following paragraphs define the timing relationship between the data and the DCLK and FSC clocks.

Normal Mode

Master Mode (TE/NT mode)

Normal TE/NT Mode Timing Diagram

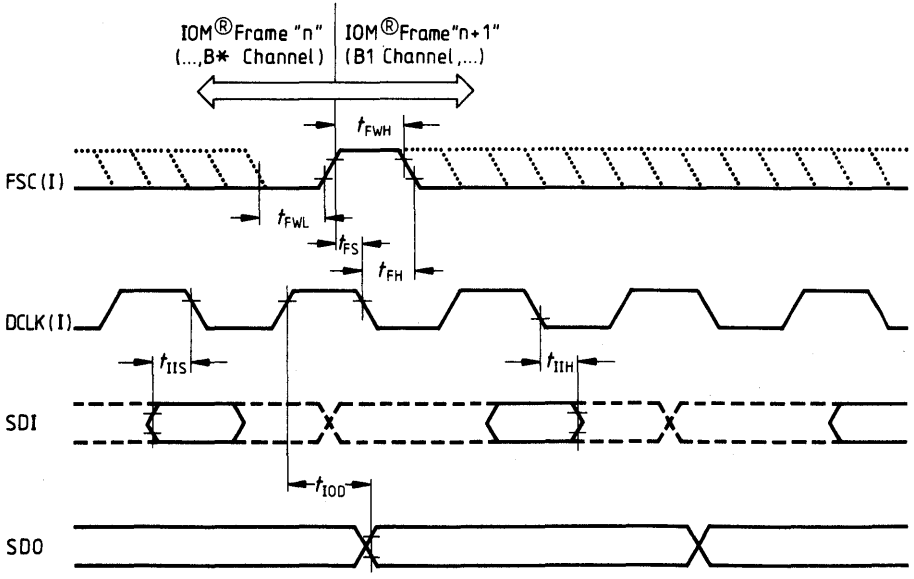


Normal TE/NT Mode Timing

Parameter	Symbol	Limit Values		Unit	Test Conditions
		min.	max.		
Frame sync. delay	t_{FD}	−20	20	ns	C_L = 100 pF
IOM output data delay	t_{IOD}		200	ns	C_L = 100 pF
IOM input data setup	t_{IIS}	20		ns	
IOM input data hold	t_{IIH}	50		ns	

Slave Mode (LT)

Normal LT Mode Timing Diagram

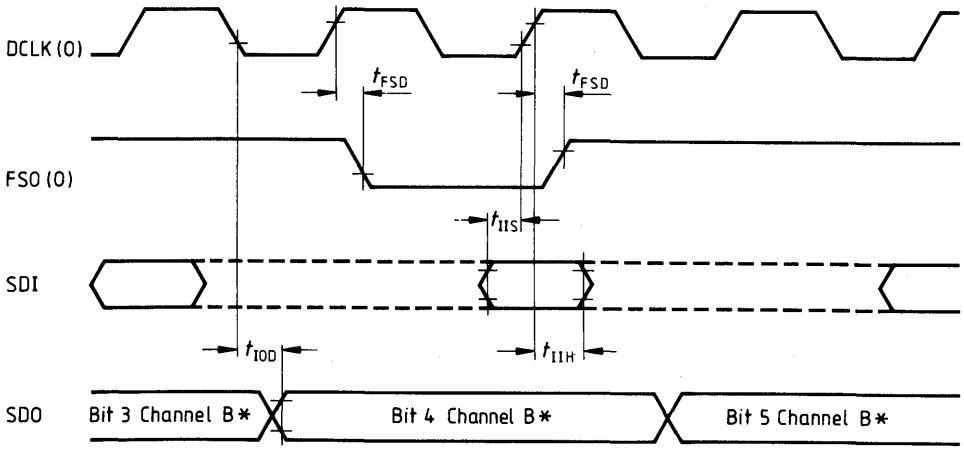


Normal LT Mode Timing

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Frame sync hold	t_{FH}	50		ns
Frame sync setup	t_{FS}	30		ns
Frame sync high	t_{FWH}	80		ns
Frame sync low	t_{FWL}	2150		ns
IOM output data delay	t_{IOD}		200	ns
IOM input data setup	t_{IIS}	20		ns
IOM input data hold	t_{IIH}	50		ns

TE Inverted Mode

Inverted TE Mode Timing Diagram

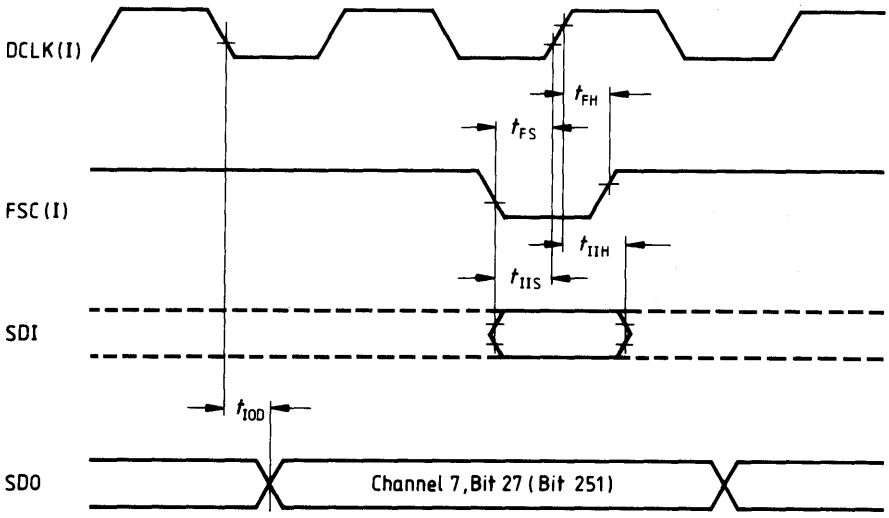


Inverted TE Mode Timing

Parameter	Symbol	Limit Values		Unit	Test Conditions
		min.	max.		
Frame sync delay	t_{FSD}	−20	20	ns	$C_L = 100$ pF
IOM output data delay	t_{IOD}		200	ns	$C_L = 100$ pF
IOM input data setup	t_{IIS}	20		ns	
IOM input data hold	t_{IIH}	50		ns	

LT MUX Mode

Inverted LT MUX Mode Timing Diagram



Inverted LT MUX Mode Timing

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Frame sync hold	t_{FH}	50		ns
Frame sync setup	t_{FS}	20		ns
Frame sync high	t_{FH}	124.8		µs
Frame sync low	t_{EL}	70	200	ns
IOM output data delay	t_{IOM}		200	ns
IOM input data setup	t_{IIS}	20		ns
IOM output data hold	t_{IIH}	50		ns

Receiver Stage Properties

Receiver Stage Properties

Input Stage / Measured Property		dB
Line amplifier	– dynamic range	0 – 30
	– resolution (128 setting)	0.236
Anti-aliasing filter and low pass filters		
> 1.1 MHz	– minimum attenuation	30
> 1.1 MHz	– typical attenuation	35
Equalizer	– dynamic range	0 – 15.36 dB
	– resolution (8 settings)	2.194

SIEMENS

ISDN Subscriber Access Controller (ISAC-P) — PEB 20950

Preliminary Data — **CMOS IC**

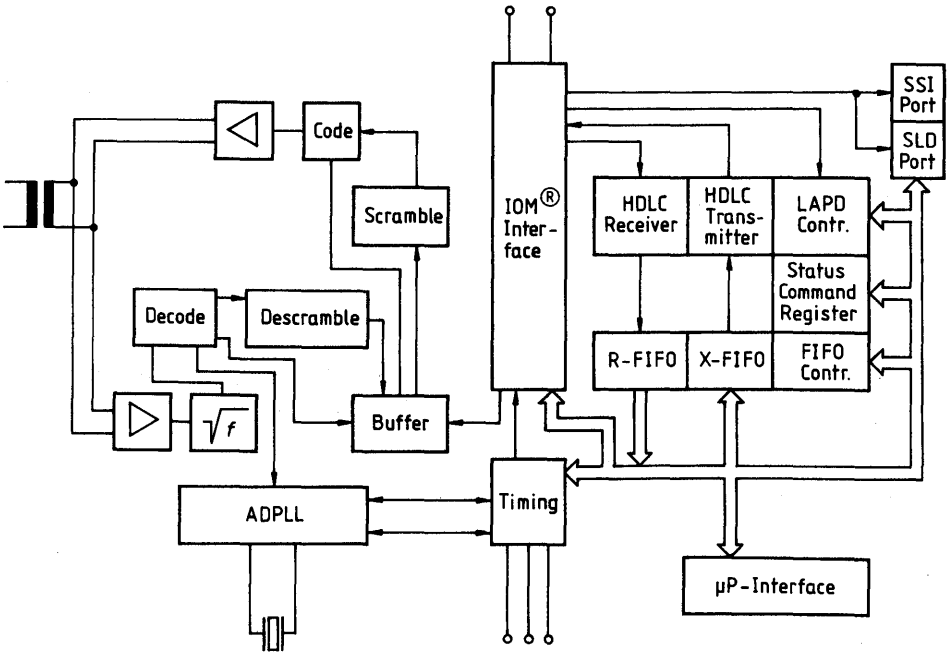
Type	Ordering Code	Package
PEB 20950-C	Q67100-H8613	C-DIP-40
PEB 20950-N	Q67100-H8614	PL-CC-44 (SMD)
PEB 20950-P	Q67100-H8550	P-DIP-40

The PEB 20950 ISAC™-P is a combination transceiver/HDLC controller for ISDN terminals in a two-wire PBX environment. Transceiver functions are performed according to the two-wire PBX industry standard U_{p0} interface. This corresponds to all of the functions available on the PEB 2095 IBC. Similarly, the HDLC protocol is processed as described for the PEB 2070 ICC. The ISAC-P represents both the IBC and ICC on a single IC.

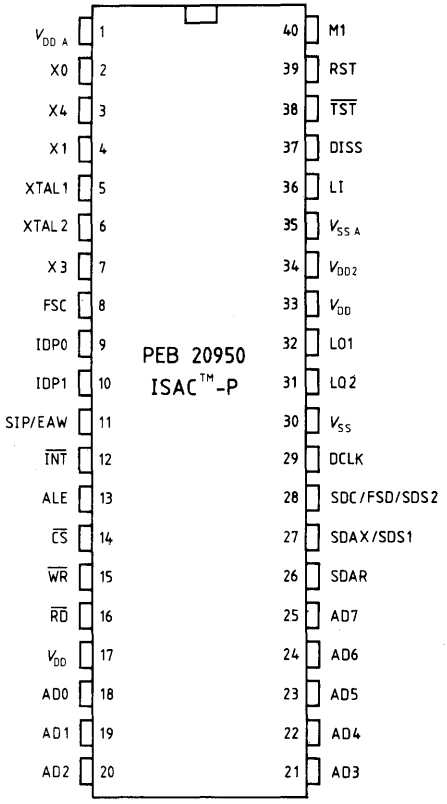
Features

- Half duplex burst mode two-wire transceiver
- AMI line code
- Adaptive line equalization
- High-level support of LAPD protocol
- FIFO buffer (2x64 bytes) for efficient transfer of D-channel packets
- IOM® interface to other ICs
- Switching of test loops
- 8-bit µP interface
- Advanced CMOS technology
- Low power consumption

ISAC-P Block Diagram



Pin Configuration **P-DIP; C-DIP**
(top view)



Pin Definitions and Functions

Pin No. P-DIP	Symbol	Input (I) Output (O)	Function
1	V_{DD}	I	Analog power supply (+5 V)
2	X0	O	**Multifunctional Pin** M1 = 1: Software programmable output M1 = 0: 3.84-MHz clock output
3	X4	I/O	**Multifunctional Pin** M1 = 1: PFOFF M1 = 0: 2.56-MHz clock output
4	X1	O	**Multifunctional Pin** M1 = 1: 15.36-MHz clock output M1 = 0: 1.536-MHz clock output in IOM-1 mode; 768-kHz clock output in IOM-2 mode

Pin Definitions and Functions (cont'd)

Pin No. P-DIP	Symbol	Input (I) Output (O)	Function
5	XTAL1	I	**External Crystal** or external clock input
6	XTAL2	O	**External Crystal** output
7	X3	I	**Multifunctional Pin** M1 = 1: MPF input M1 = 0: $\overline{\text{ENCK}}$ input
8	FSC	I/O	**IOM Interface Frame Synchronization** M1 = 1: 8-kHz input clock M1 = 0: 8-kHz output clock
9	IDP0	I/O	**IOM Interface Data Port 0** LT application: Data upstream line TE application: Data downstream line
10	IDP1	I/O	**IOM Interface Data Port 1** LT application: Data downstream line TE application: Data upstream line
11	SIP/EAW	I/O	**SLD Interface Port,** IOM-1 mode This line transmits and receives serial data at standard TTL or CMOS level. External Awake, terminal specific functions If a falling edge on this input is detected, the ISAC-P generates an interrupt and/or a reset pulse
12	$\overline{\text{INT}}$	OD	**Interrupt Request** The signal is activated, when the ISAC-P requests an interrupt. The CPU may determine the particular source and cause of interrupt by reading the ISAC-P interrupt status register (ISTA, EXIR). $\overline{\text{INT}}$ is an open drain output, thus the interrupt request outputs of several ISAC-P's can be connected to one interrupt input in a "wired-or" combination. This pin must be connected to a pull up resistor.
13	ALE	I	**Address Latch Enable** A high on this line indicates an address on the external address/data bus, which will select one of the ISAC-P's internal registers. The address is latched with the falling edge of ALE.

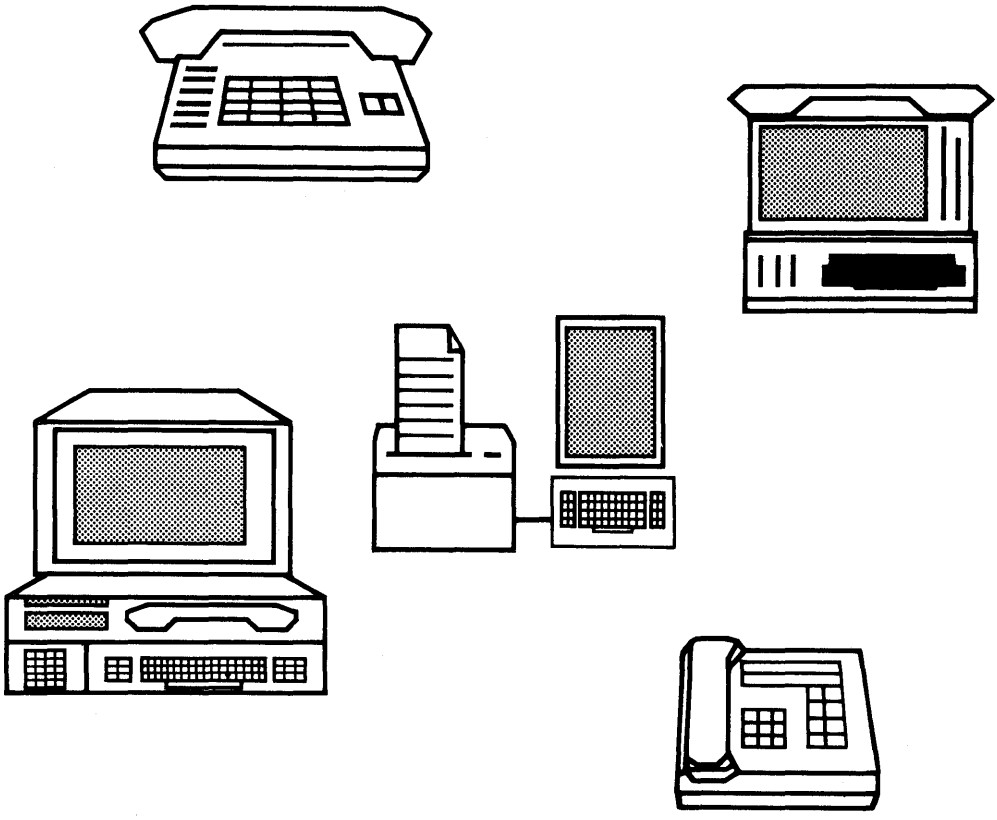
Pin Definitions and Functions (cont'd)

Pin No. P-DIP	Symbol	Input (I) Output (O)	Function
14	$\overline{CS}$	I	**Chip Select** A low signal selects the ISAC-P for a read/write operation.
15	$\overline{WR}$	I	**Write** This signal indicates a write operation. When $\overline{CS}$ is active, the ISAC-P loads an internal register with data provided via the address/data bus.
16	$\overline{RD}$	I	**Read** This signal indicates a read operation. When the ISAC-P is selected via $\overline{CS}$ the read signal enables the bus drivers to put data from an internal register on the address/data bus.
17	V_{DD}	I	Power supply (+5 V)
18 19 20 21 22 23 24 25	AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7	I/O I/O I/O I/O I/O I/O I/O I/O	**Address Data Bus** The multiplexed address data bus transfers data and command/status information between the ISAC-P and the µP system.
26	SDAR	I	**Serial Data Port A Receive** Serial data is received on this pin at standard TTL or CMOS level. An integrated pull-up circuit enables connection of an open drain/open collector driver without an external pull-up resistor. SDAR is used only if IOM-1 mode is selected.
27	SDAX/ SDS1	O	**Serial Data Port A Transmit,** IOM-1 mode Transmit data is shifted out via this pin at standard TTL or CMOS level. **Serial Data Strobe 1,** IOM-2 mode A programmable strobe signal, selecting either one of two B/IC channels on IOM-2 interface, is supplied via this line. After reset SDAX/SDS1 remains at logical 0 until a write access to SPCR is made.

Pin Definitions and Functions (cont'd)

Pin No. P-DIP	Symbol	Input (I)	Function
28	SCA/FSD SDS2	O	**Serial Clock Port A,** IOM-1 timing mode 0 A 128-kHz data clock signal for serial port A is supplied. **Frame Sync Delayed,** IOM-1 timing mode 1 A 8-kHz synchronization signal, delayed by 1/8 of a frame, for serial port B (IOM-1 interface) is supplied. In this mode a minimal delay for B1 and B2 channels is guaranteed. **Serial Data Strobe 2,** IOM-2 mode A programmable strobe signal, selecting either one or two B/IC channels on IOM-2 interface, is supplied via this line. After reset, SCA/FSD/SDS2 remains at logical 0 until a write access to SPCR is made.
29	DCLK	I/O	**IOM Interface Data Clock** M1 = 1: input 512-kHz IOM-1 mode input 4.096-kHz IOM-2 mode M1 = 0: output 512-kHz IOM-1 mode output 1.536-MHz IOM-2 mode
30	V_{SS}	I	Ground (0 V)
31	LO2	O	**Line Transmitter Output**
32	LO1	O	**Line Transmitter Output**
33	V_{DD}	I	Power supply (+5 V)
34	V_{DD2}	O	2.5 V output; connected to both V_{DD} and V_{SS} via 10 nF capacitor.
35	V_{SSA}	I	Analog ground (0 V)
36	LI	I	**Line Receiver Input**
37	DISS	O	**Disable Supply Indication**
38	$\overline{TST}$	I	**Device Test Pin:** tie always high
39	RES	I/O	**RESET** A high signal on this input forces the ISAC-P into reset state. The minimum pulse length is four clock periods of DCLK. If the terminal specific functions are enabled, the ISAC-P may also supply a reset signal.
40	M1	I	**Operating Mode for IBC-Part.** M1 = 1: IBC in LT mode M1 = 0: IBC in TE mode

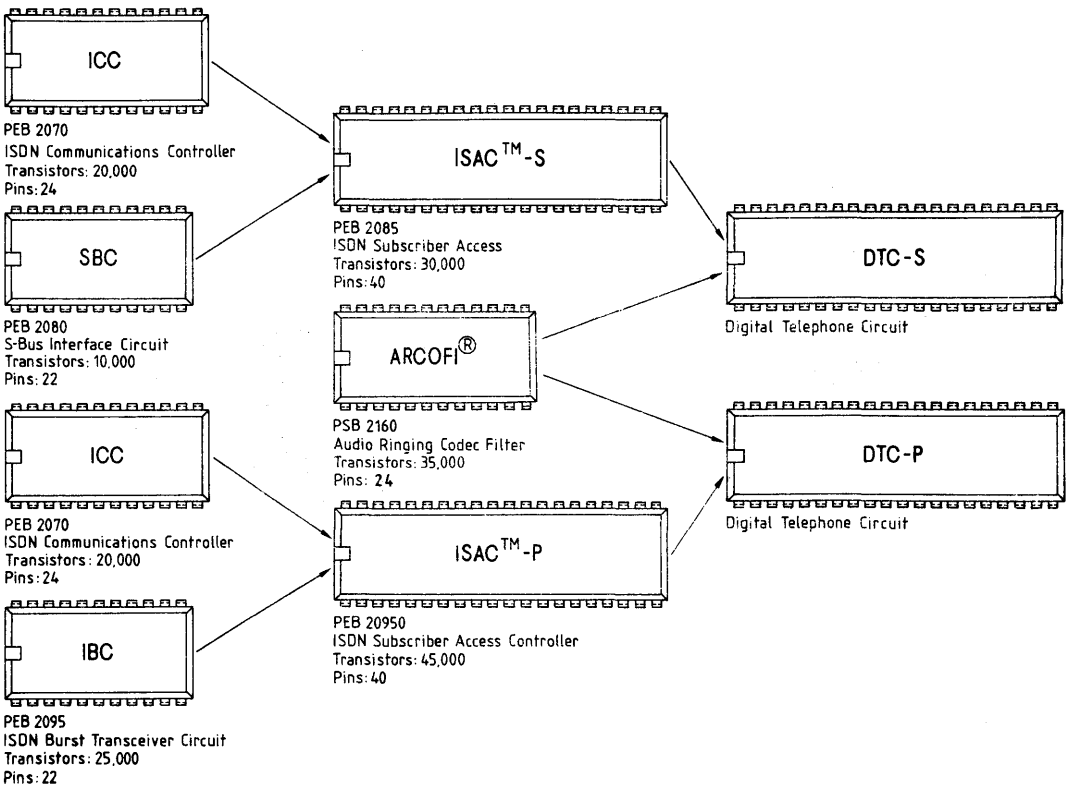
ICs for ISDN Terminals



Steps of Integration

As mentioned, the development of modularized chips has been made from a strategical point of view to reduce development time, risk and effort; to enhance volume for cost reduction; and to achieve high flexibility with regard to different system needs. In the follow-up step for forward integration, the layer-1 and layer-2 functions consequently will be put together in order to optimize the cost structure for high-volume applications. This step has been taken into account in the present circuit topology and therefore will require little effort. Nevertheless, the single components will continue to be available for realizing specific functions without overheads. The combination of SBC and ICC will result in the ISDN subscriber access controller with S interface (ISAC™-S); the IBC and ICC will result in the ISAC-P. Further integration of these chips with the ARCOFI®-(**a**udio **r**inging **co**dec **fi**lter) will lead to digital telephone controller chips supporting the S and U burst interface (DTC-S and DTC-P).

Integration Strategy



SIEMENS

ISDN Subscriber Access Controller (ISAC-S) PEB 2085

Preliminary Data **CMOS IC**

Type	Ordering Code	Package
PEB 2085-N	Q67100-H8399	PL-CC-44 (SMD)
PEB 2085-P	Q67100-H8401	P-DIP-40

The PEB 2085 ISAC™-S implements the four-wire S/T interface used to link voice/data terminals to an ISDN.

The PEB 2085 combines the functions of the S-Bus Interface Circuit (SBC: PEB 2080) and the ISDN Communications Controller (ICC: PEB 2070) on one chip.

The component switches B and D channels between the S/T and the ISDN Oriented Modular (IOM®) interfaces, the latter being a standard backplane interface for ISDN basic access.

The device provides all electrical and logical functions of the S/T interface, such as: activation/deactivation, mode dependent timing recovery and D-channel access and priority control.

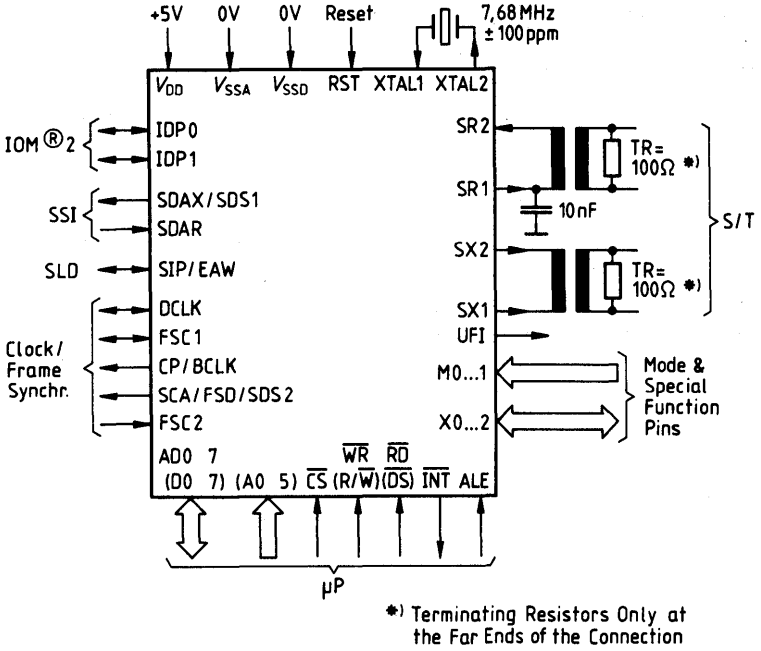
The HDLC packets of the ISDN D channel are handled by the ISAC-S which interfaces them to the associated microcontroller. In one of its operating modes the device offers high level support of layer-2 functions of the LAPD protocol.

The ISAC-S is a CMOS device, available in a P-DIP-40 or PL-CC-44 package. It operates from a single +5 V supply and features a power-down state with very low power consumption.

Features

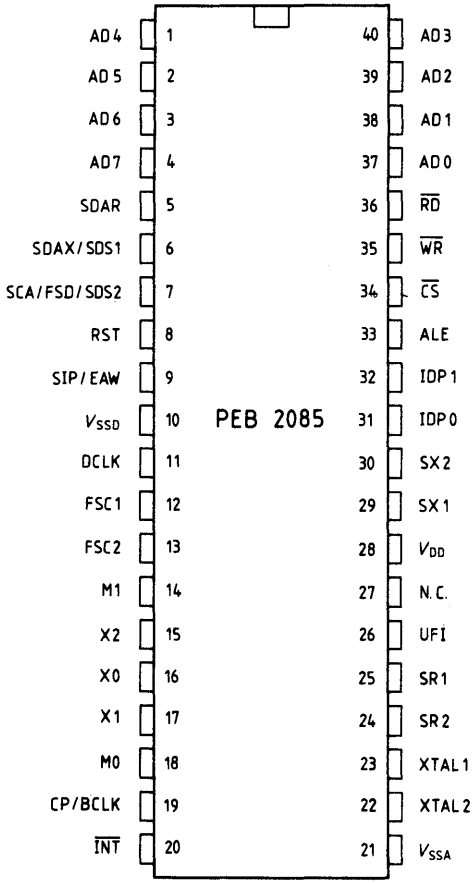
- Full duplex 2B + D S/T interface transceiver according to CCITT I.430
- Conversion of the frame structure between the S/T interface and IOM
- Receive timing recovery according to selected operating mode
- D-channel access control
- Activation and deactivation procedures, with automatic wake-up from power-down state
- Access to S and Q bits of S/T interface
- Adaptively switched receive thresholds
- Frame alignment with absorption of phase wander in NT2 network side applications
- Support of LAPD protocol
- FIFO buffer (2x64 bytes) for efficient transfer of D-channel packets
- 8-bit microprocessor interface, multiplexed or non-multiplexed
- Serial interfaces: IOM-1, SLD, SSI
  IOM-2
- Implementation of IOM-1/IOM-2 monitor and C/I channel protocol to control peripheral devices
- µP access to B channels and intercommunication channels
- B-channel switching
- Watchdog timer
- Test loops
- Advanced CMOS technology
- Low power consumption

Figure 1
Logic Symbol

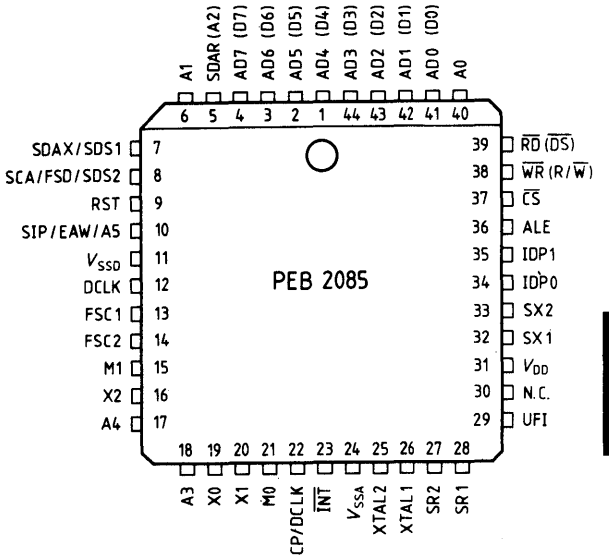


Pin Configuration
(top view)

P-DIP-40



PL-CC-44



Pin Definitions and Functions (cont'd)

Pin No. P-DIP	Pin. No. PL-CC	Symbol	Input (I) Output (O)	Function
37 38 39 40 1 2 3 4	41 42 43 44 1 2 3 4	AD0/D0 AD1/D1 AD2/D2 AD3/D3 AD4/D4 AD5/D5 AD6/D6 AD7/D7	I/O I/O I/O I/O I/O I/O I/O I/O	**Multiplexed Bus Mode:** Address/Data bus Transfers addresses from the µP system to the ISAC-S and data between the µP system and the ISAC-S. Non-multiplexed bus mode: Data bus. Transfers data between the µP system and the ISAC-S.
34	37	$\overline{CS}$	I	**Chip Select.** A "Low" on this selects the ISAC-S for a read/write operation.
–	36	R/$\overline{W}$	I	**Read/Write.** When "High", identifies a valid µP access as a read operation. When "Low", identifies a valid µP access as a write operation (Motorola bus mode).
35	36	$\overline{WR}$	I	**Write.** This signal indicates a write operation (Intel bus mode).
–	39	$\overline{DS}$	I	**Data Strobe.** The rising edge marks the end of a valid read or write operation (Motorola bus mode).
36	39	$\overline{RD}$	I	**Read.** This signal indicates a read operation (Intel bus mode).
20	23	$\overline{INT}$	OD	**Interrupt Request.** The signal is activated when the ISAC-S requests an interrupt. It is an open drain output.
33	36	ALE	I	**Address Latch Enable.** A high on this line indicates an address on the external address bus (multiplexed bus type only).
10	11	V_{SSD}	–	Digital ground
21	24	V_{SSA}	–	Analog ground
28	31	V_{DD}	–	Power supply (5 V ± 5%)
23 22	26 25	XTAL1 XTAL2	I O	Connection for crystal or external clock input. Connection for external crystal. Left unconnected if external clock is used.
24 25	27 28	SR2 SR1	I O	**S Bus Receiver Input** **S Bus receiver Output** (2.5 V reference)
26	29	UFI	O	Connection for external pre-filter for S bus receiver, if used.

Pin Definitions and Functions (cont'd)

Pin No. P-DIP	Pin No. PL-CC	Symbol	Input (I) Output (O)	Functions
29 30	32 33	SX1 SX2	O O	**S Bus Transmitter** output (positive) **S Bus Transmitter** output (negative)
31 32	34 25	IDP0 IDP1	I/O I/O	**IOM Data Port 0, 1**
7	8	SCA	O	**Serial Clock Port A,** IOM-1 timing mode 0. A 128-kHz data clock signal for serial port A (SSI).
7	8	FSD	O	**Frame Sync Delayed,** IOM-1 timing mode 1. An 8-kHz synchronization signal, delayed by 1/8 of a frame, for IOM-1 is supplied. In this mode a minimal round trip delay for B1 and Bs channels is guaranteed.
7	8	SDS2	O	**Serial Data Strobe 2,** IOM-2 mode. A programmable strobe signal, selecting either one or two B or IC channels on IOM-2 interface, is supplied via this line. After reset, SCA/FSD/SDS2 takes on the function of SDS2 until a write access to SPCR is made.
8	9	RST	I/O	**Reset.** A "High" on this input forces the ISAC-S into reset state. The minimum pulse length is four clock periods. If the terminal specific functions are enabled. The ISAC-S may also supply a reset signal.
12	13	FSC1	I/O	**Frame Sync. 1** LT-S/NT/LT-T: input synchronization signal, IOM-1 and IOM-2 mode. TE: a programmable strobe output, selecting either one or two B channels on IOM-1 interface, IOM-1 mode. TE: frame sync output, "High" during channel 0 on IOM-2 interface, IOM-2 mode.
13	14	FSC2	I/O	**Frame Sync 2,** IOM-1 mode. LT-S/LT-T/NT: input synchronization signal TE: programmable strobe output, selecting either one or two B channels in IOM-1 interface.

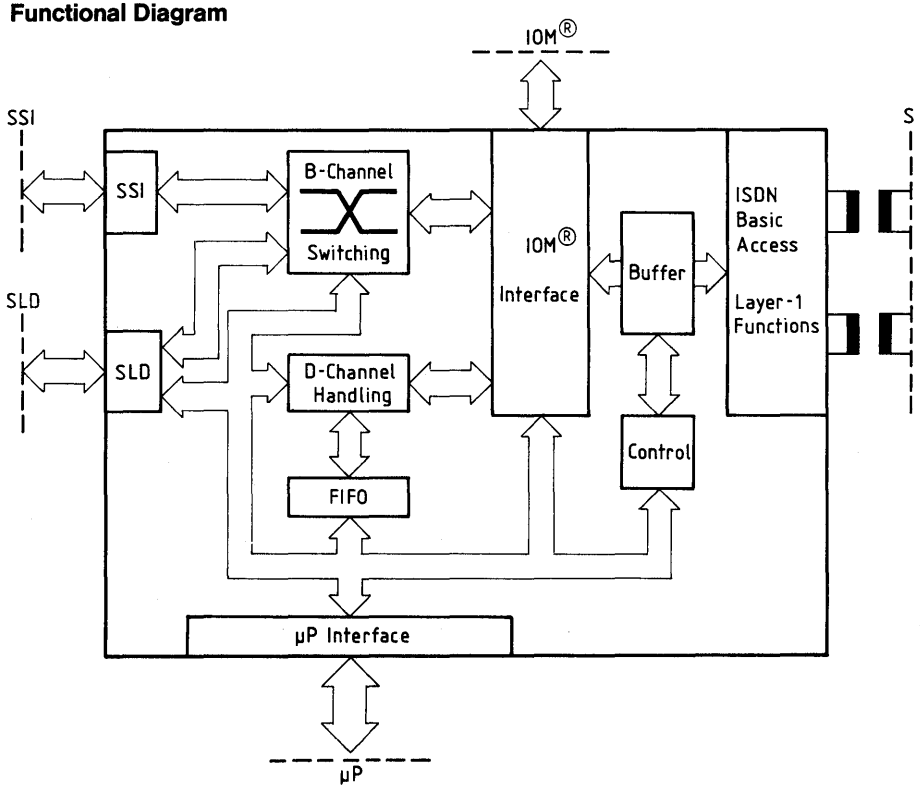
Pin Definitions and Functions (cont'd)

Pin No. P-DIP	Pin No. PL-CC	Symbol	Input (I) Output (O)	Function
11	12	DCLK	I/O	**Data Clock.** Clock of frequency equal to twice the data rate on the IOM interface. LT-S/LT-T: clock input 512-kHz IOM-1 mode max 4096-kHz IOM-2 mode TE: clock output 512-kHz IOM-1 mode 1536-kHz IOM-2 mode NT: clock input 512 kHz
–	40	A0	I	**Address Bit 0** (non-multiplexed bus type).
–	6	A1	I	**Address Bit 1** (non-multiplexed bus type).
– 5	5 5	A2 SDAR	I I	**Address Bit 2** (non-multiplexed bus type). **Serial Data Port A Receive.** Serial data is received on this pin at standard TTL or CMOS level. An integrated pull-up circuit enables connection of an open-drain/ open collector driver without an external pull-up resistor. SDAR is used only if IOM-1 mode is selected.
–	18	A3	I	**Address Bit 3** (non-multiplexed bus type).
–	17	A4	I	**Address Bit 4** (non-multiplexed bus type).
– 9 9	10 10 10	A5 SIP EAW	I I/O I	**Address Bit 5** (non-multiplexed bus type). **SLD Interface Port,** IOM-1 mode. This line transmits and receives serial data at standard TTL or CMOS levels. **External Awake** (terminal specific function). If a falling edge on this input is detected, the ISAC-S generates an interrupt and, if enabled, a reset pulse.
6 6	7 7	SDAX SDS1	0 0	**Serial Data Port A Transmit,** IOM-1 mode. Transmit data is shifted out via this pin at standard TTL or CMOS levels. **Serial Data Strobe 1,** IOM-2 mode. A programmable strobe signal, selecting either one or two B or IC channels on IOM-2 interface, is supplied via this line. After reset, SDAX/SDS1 takes on the function of SDS1 until a write access to SPCR is made.

Pin Definitions and Functions (cont'd)

Pin No. P-DIP	Pin No. PL-CC	Symbol	Input (I) Output (O)	Function
14 18	15 21	M1 M0	I I	Setting of operating mode
15 17 16	16 20 19	X2 X1 X0	I/O I/O I	Mode specific function pins
19	22	CP	I/O	**Clock Pulses.** Special purpose pin, IOM-1 mode and IOM-2 (except TE) mode.
19	22	BCLK	O	**Bit Clock.** Clock of frequency 768 kHz, IOM-2 mode in TE.

Figure 2
Functional Diagram



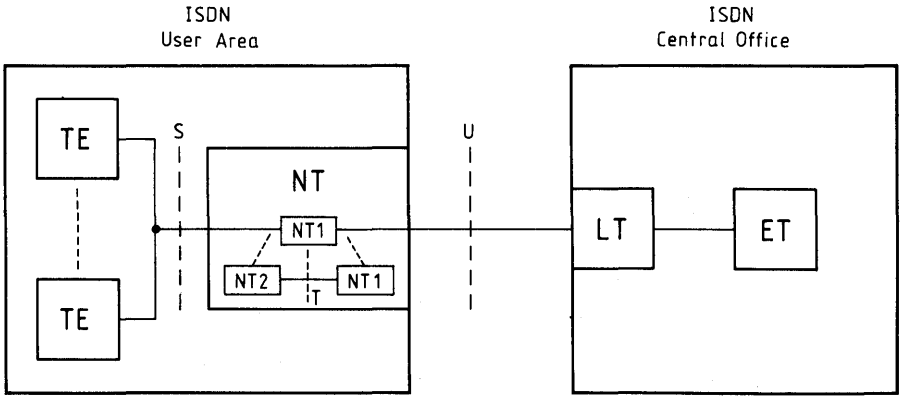
System Integration

ISDN Applications

The reference model for the ISDN basic access according to CCITT I series recommendations consists of

- an exchange and trunk line termination in the central office (ET, LT)
- a remote network termination in the user area (NT)
- a two-wire loop (U interface) between NT and LT
- a four-wire link (S interface) which connects subscriber terminals and the NT in the user area as depicted in **figure 3**.

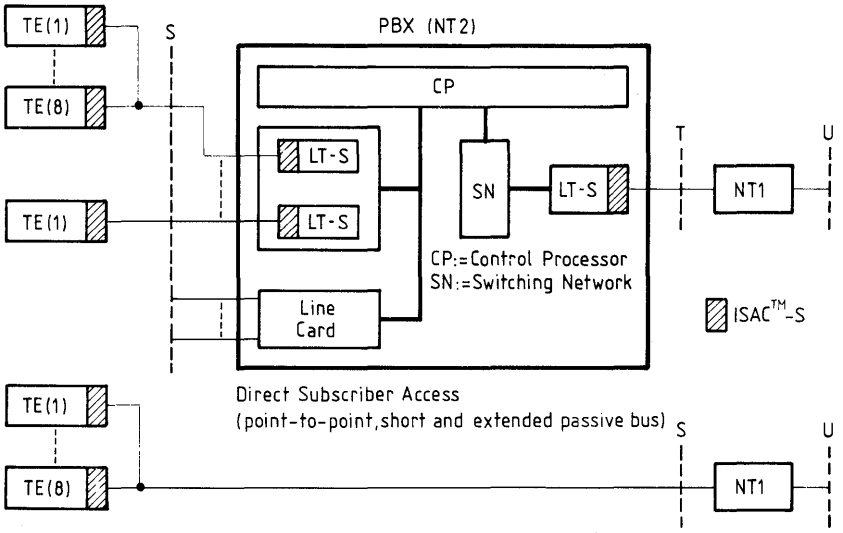
Figure 3
ISDN Basic Subscriber Access Architecture



The NT equipment serves as a converter between the U interface at the exchange and the S interface at the user premises. The NT may consist of either an NT1 only or an NT1 together with an NT2 connected via the T interface which is physically identical to the S interface. The NT1 is a direct transfomation between layer 1 of S and layer 1 of U. NT2 may include higher level functions like multiplexing and switching as in a PBX.

The ISAC-S designed for the user area of the ISDN basic access, especially for subscriber terminal equipment and for exchange equipment with S interfaces. **Figure 4** illustrates the general application of the ISAC-S.

Figure 4
Applications of ISAC-S (ISDN Basic Access)



Terminal Applications

The concept of the ISDN basic access is based on two circuit-switched 64 kbit/s B channels and a message oriented 16 kbit/s D channel for packetized data, signaling and telemetry information.

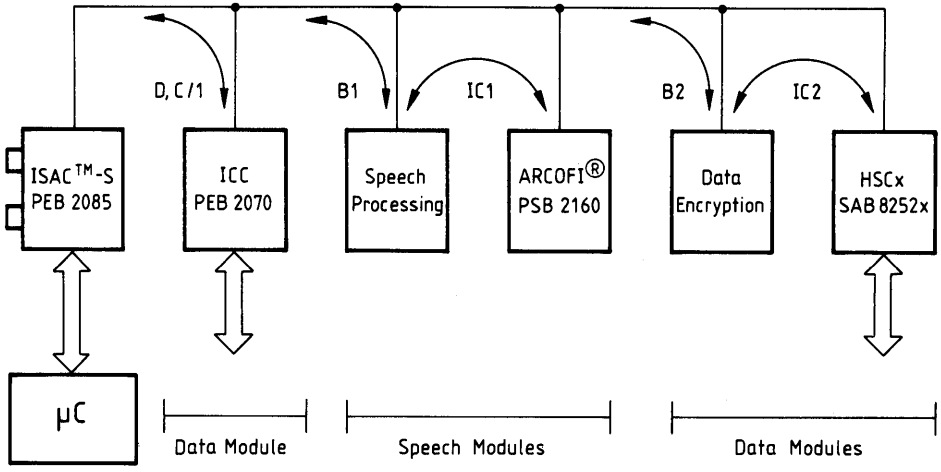
Figure 5 shows an example of an integrated multifunctional ISDN-S terminal using the ISAC-S. The ISAC-S provides the interface to the bus and separates the B and D channels.

The D channel, containing signaling data and packet switched data, is processed by the LAPD controller contained in the ISAC-S and routed via a parallel µP interface to the terminal processor. The high level support of the LAPD protocol is implemented by the ISAC-S allows the use of a low cost processor in cost sensitive applications.

The IOM interface generated by the ISAC-S is used to connect diverse voice/data application modules:

- sources/sinks for the D channel
- sources/sinks for the B1 and B2 channels.

Figure 5
Example of ISDN-S Voice/Data Terminal



Up to eight D channel components (ICC: ISDN Communication Controller PEB 2070) may be connected to the D and C/I (Command/Indication) channels. The ISAC-S and ICC handle contention autonomously.

Data transfers between the ISAC-S and the voice/data modules are done with the help of the IOM monitor channel protocol. Each V/D module can be accessed by an individual address. The same protocol enables the control of IOM terminal modules and the programming of intercommunication inside the terminal. Two intercommunication channels IC1 and IC2 allow a 2 x 64 kbit/s transfer rate between voice/data modules.

In the example above **(figure 5)**, one ICC is used for data packets in the D channel. A voice processor is connected to a programmable digital signal processing codec filter via IC1 and a data encryption module to a data device via IC2. B1 is used for voice communication, B2 for data communication.

The ISAC-S ensures full upward compatibility with IOM-1 devices. It provides the additional strobe, clock and data lines for connecting standard combos or data devices via IOM, or serial SLD and SSI interfaces. The strobe signals and the switching of B channels is programmable. **Figure 6** shows the implementation of a basic ISDN feature telephone using the ISAC-S and the Audio Ringing Codec Filter (ARCOFI®: PSB 2160).

Line Card Applications

An example of the use of the ISAC-S on an ISDN PBX line card (decentralized architecture) is shown in **figure 7**.

The ISAC-S is connected to an Extended PCM Interface Controller (EPIC PEB 2055) via an IOM interface.

This interface carries the control and data for up to eight subscribers using time division multiplexing. The ISAC-S's are connected in parallel on IOM (IDP0 output; IDP1, DCLK, FSC1 as inputs), one ISAC-S per subscriber.

The EPIC performs dynamic B and D channel assignment on the PCM highways. Since this component supports four IOM interfaces, up to 32 subscribers may be accomodated.

Microprocessor Environment

The ISAC-S is especially suitable for cost-sensitive applications with single-chip microcontrollers (e. g. 8048, 8031, 8051). However, due to its programmable micro interface and non-critical bus timing, it fits perfectly into almost any 8-bit microprocessor system environment. The microcontroller interface can be selected to be either of the Motorola type (with control signals $\overline{CS}$, R/$\overline{W}$, $\overline{DS}$), of the Siemens/Intel non-multiplexed bus type (with control signals $\overline{CS}$, $\overline{WR}$, $\overline{RD}$) or of the Siemens/Intel multiplexed address/data bus type ($\overline{CS}$, $\overline{WR}$, $\overline{RD}$, ALE).

Figure 6
Basic ISDN Feature Telephone

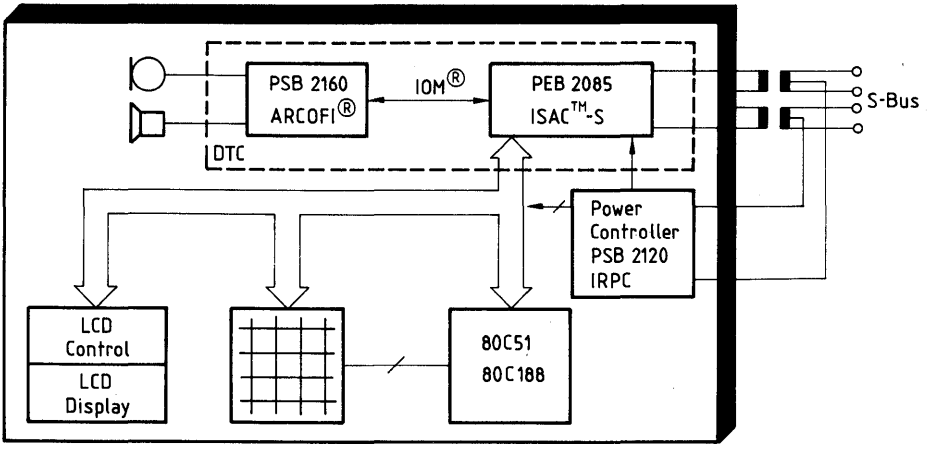


Figure 7
ISDN PBX Line Card Implementation

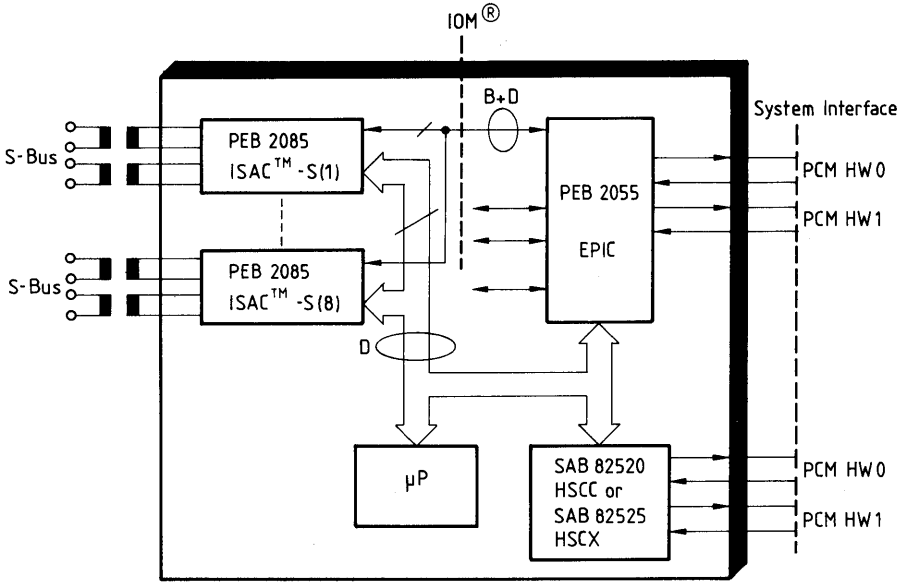
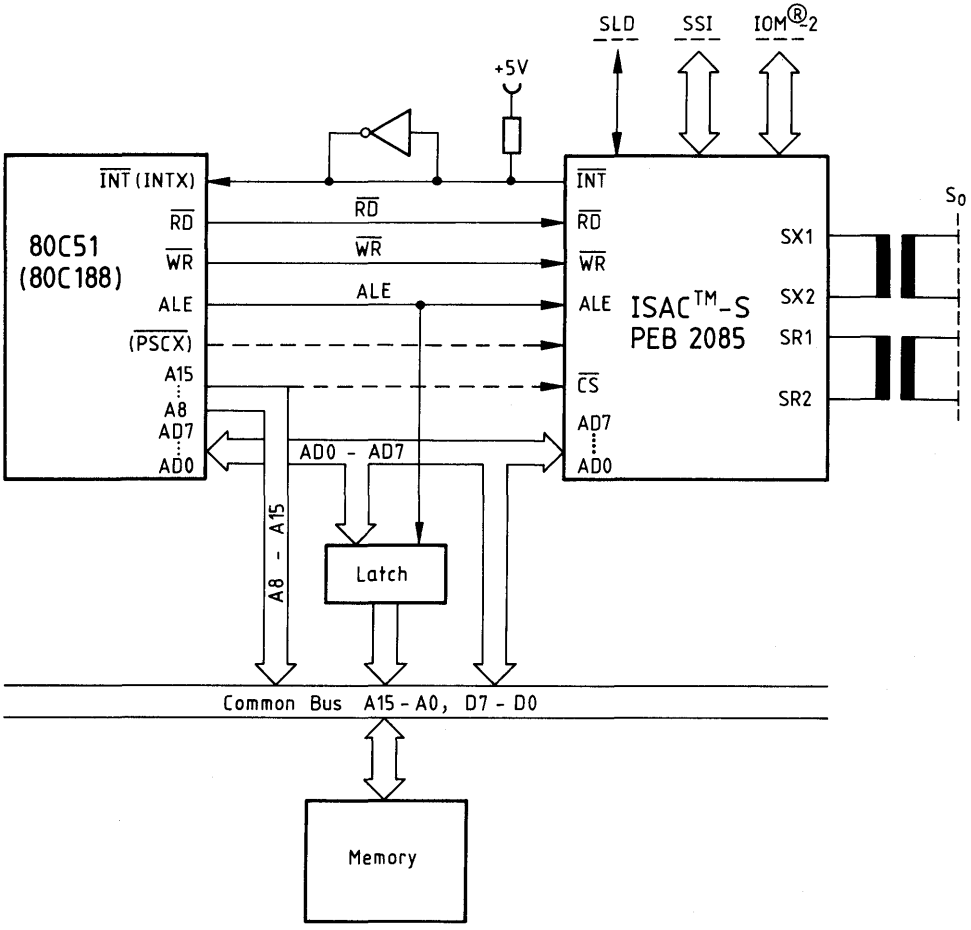


Figure 8


SLD
SSI
IOM®-2
+5V
80C51
(80C188)
INT (INTX)
RD
WR
ALE
(PSCX)
A15
A8
AD7
AD0
ISAC™-S
PEB 2085
INT
RD
WR
ALE
CS
AD7
AD0
SX1
SX2
SR1
SR2
S0
AD0 - AD7
A8 - A15
Latch
Common Bus A15 - A0, D7 - D0
Memory

Functional Description

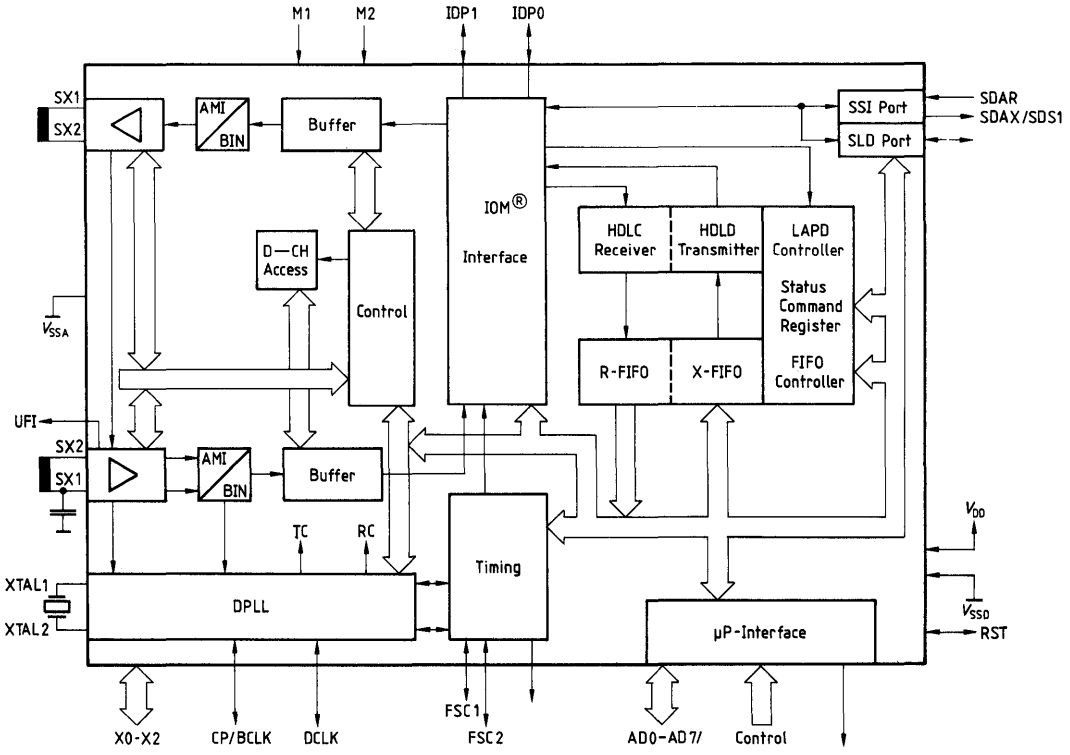
General Functions and Device Architecture

The functional block diagram of the ISAC-S is shown in **figure 9**.

The left-hand side of the diagram contains the layer-1 functions, according to CCITT I series recommendations:

- S-bus transmitter and receiver
- riming recovery and synchronization by means of digital PLL circuitry
- activation/deactivation
- access to S and Q channels
- handling of D channel
- test loops
- send single/continuous AMI pulses (diagnostics).

Figure 9
Architecture of the ISAC-S



The right-hand side consists of:

- the serial interface logic for the IOM and the SLD and SSI interfaces, with B channel switching capabilities
- the logic necessary to handle the D-channel messages (layer 2).

The latter consists of an HDLC receiver and an HDLC transmitter together with 64-byte deep FIFO's for efficient transfer of the messages to/from the user's CPU.

In a special HDLC controller operating mode, the auto mode, the ISAC-S processes protocol handshakes (I- and S-frames) of the LAPD (Link Access Procedure on the D channel) autonomously.

Control and monitor functions as well as data transfers between the user's CPU and the D and B channels are performed by the 8-bit parallel µP interface logic.

The IOM interface allows interaction between layer-1 and layer-2 functions. It implements D-channel collision resolution for connecting other layer-2 devices to the IOM interface, and the C/I and monitor channel protocols (IOM-1/IOM-2) to control peripheral devices.

The timing unit is responsible for the system clock and frame synchronization.

Interface Modes

Two basic modes are distinguished, according to whether the ISAC-S is programmed to operate with IOM-1 or with IOM-2 interface. This programming is performed via bit IMS in ADF2 register.

IOM-1 Interface Mode (IMS = 0)

The ISAC-S is configurable for the following applications:

- ISDN Terminals → TE Mode
- ISDN subscriber line termination → LT-S mode
- ISDN trunk line termination (PBX connection to Central Office) → LT-T mode
- ISDN network termination → NT mode

Configuration is performed by pin-strapping (pins M1, M0), yielding different meanings to the multifunctional pins (X0, X1, X2) as well as the clock and framing signal pins (DCLK, FSC1, FSC2, CP) **see table 1**.

Table 1
Operating Modes and Functions of Mode Specific Pins of ISAC-S PEB 2085 (IOM-1)

Application	M1	M0	DCLK	FSC1/2	CP	X2	X1	X0
TE	0	0	o: 512 kHz*	o: 8 kHz*	o: 1536 kHz*	o: ECHO	o: 3840 kHz	I: CON
LT-S	1	0	i: 512 kHz	i: 8 kHz	i: fixed at 0	i: fixed at 0	o: 7680 kHz	i: fixed at 0
LT-T	0	1	i: 512 kHz	i: 8 kHz	o: 512 kHz*	i: fixed	i: fixed at 0	I: CON
NT	1	1	i: 512 kHz	i: 8 kHz	i: $\overline{SCZ}$	i: $\overline{SSZ}$	i: fixed at 0	–

* synchronized to S i: input o: output

ECHO Reproduces the E-bits received from the S interface synchronously to IOM frame "D"-bits (bit positions 24 and 25 of IOM frame). All other bit positions are binary 1.

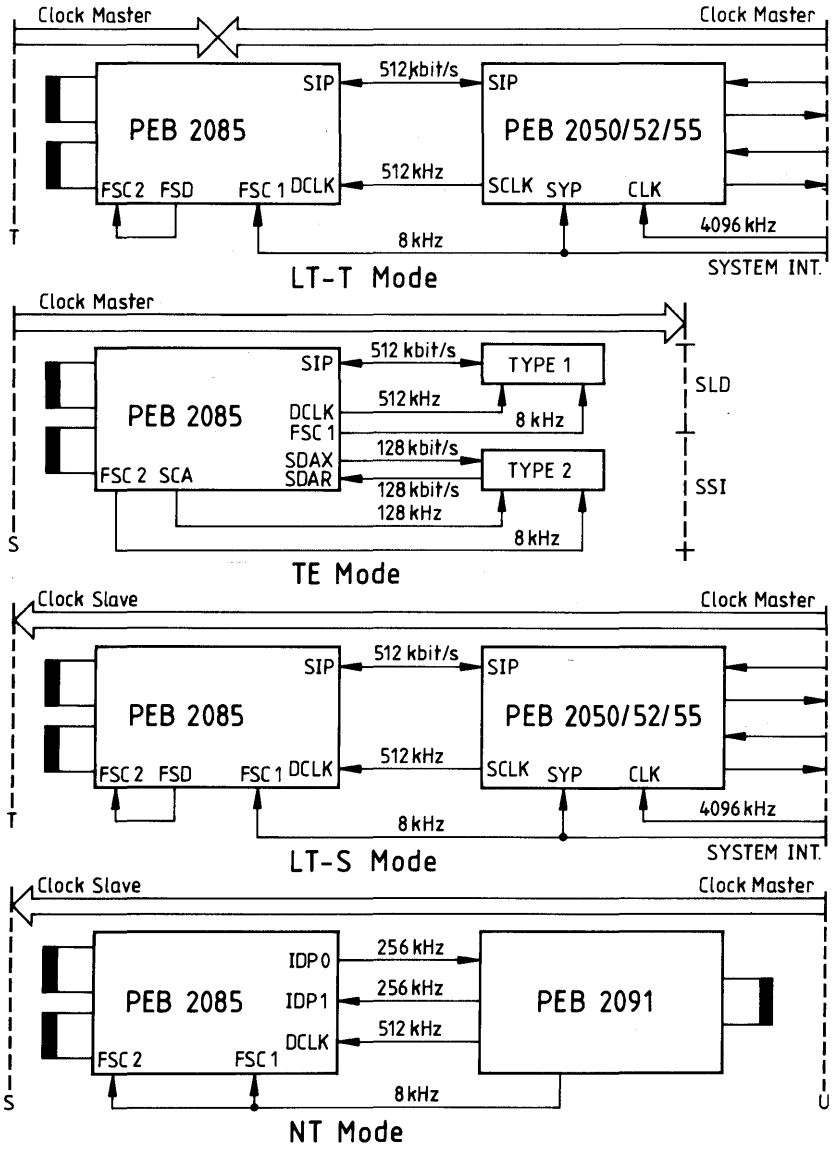
CON Connected to S bus.

$\overline{SCZ}$ Send continuous binary zeros (96 kHz)

$\overline{SSZ}$ Send single binary zeros (2 kHz)

Figure 10
Operating Modes of ISAC-S (IOM-1)

The different operating modes in relation to the timing recovery are illustrated in **figure 10.**



IOM-2 Interface Mode (IMS = 1)

In this mode the IOM interface has the enhanced functionally of IOM-2. Moreover, the auxiliary serial SSI and SLD interfaces are not longer available (as in IOM-1 mode), since they are functionally replaced by the general purpose IOM-2 interface.

Table 2
Operating Modes and Functions of Mode Specific Pins of ISAC-S PEB 2085 (IOM-2)

Application	M1	M0	DCLK	FSC1	CP/BCLK	X2	X1	X0
TE	0	0	o: 1536 kHz*	o: 8 kHz*	o: 768 kHz*	o: ECHO	o: 3840 kHz	i: CON
LT-S	1	0	i: 4096 kHz	i: 8 kHz	i: fixed at 0	i: fixed at 0	o: 7680 kHz	i: fixed at 0
LT-T	0	1	i: 4096 kHz	i: 8 kHz	o: 512 kHz*	i: fixed at 0	i: fixed at 0	i: CON
NT	1	1	i: 512 kHz	i: 8 kHz	i: SCZ	i: $\overline{SSZ}$	i: fixed at 0	–

* synchronized to S i: input o: output

ECHO: Reproduces the E-bits received from the S interface synchronously to IOM frame "D"-bits (bit positions 24 and 25 of IOM frame). All other bit positions are binary 1.

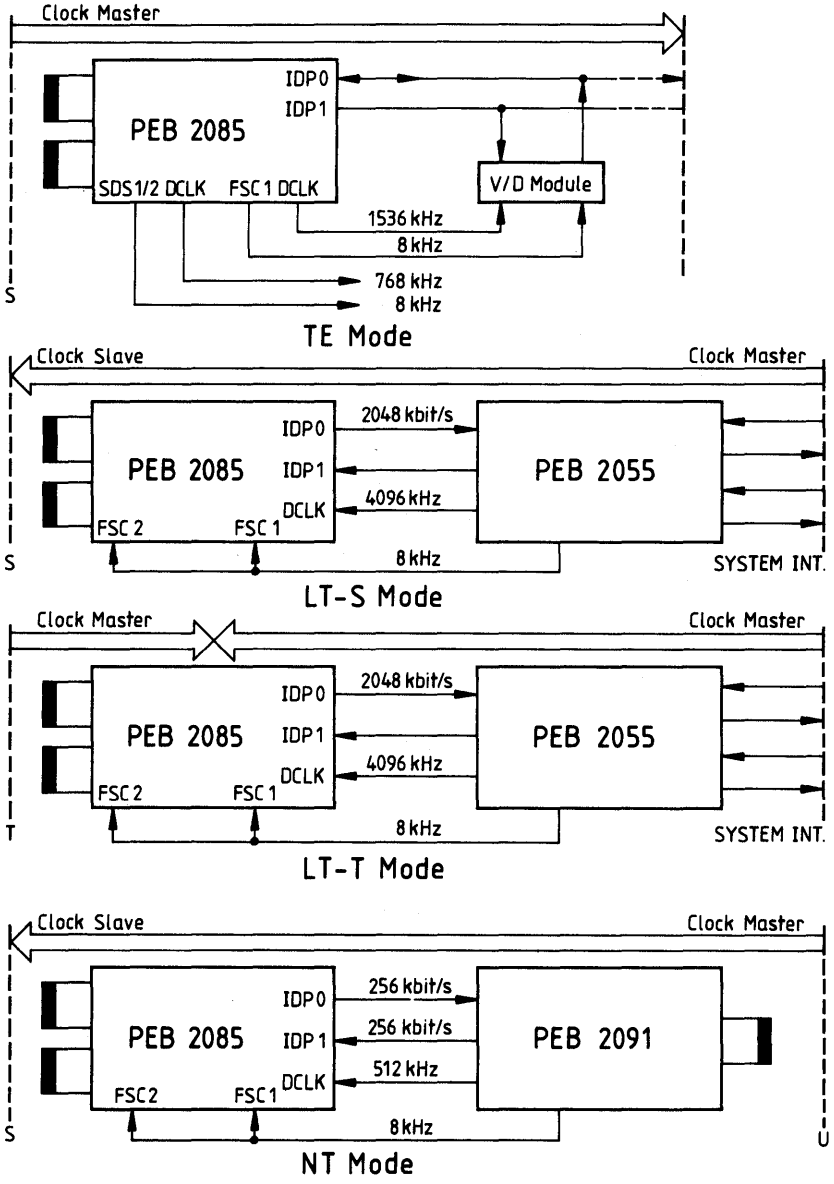
CON Connected to S bus.

$\overline{SCZ}$ Send continuous binary zeros (96 kHz)

$\overline{SSZ}$ Send single binary zeros (2 kHz)

Figure 11
Operating Modes of ISAC-S (IOM-2)

The different operating modes in relation to the timing recovery are illustrated in **figure 11.**



Interfaces

The ISAC-S serves three different user-oriented interface types:

- parallel processor interface to higher layer functions
- IOM interface: between layer 1 and layer 2, and as a universal backplane for terminals
- SSI and SLD interfaces for B channel sources and destinations (in IOM-1 mode only).

µP Interface

The ISAC-S is programmed via an 8-bit parallel microcontroller interface. Easy and fast microprocessor access is provided by 8-bit address decoding on chip. The interface consists of 13 (18) lines and is directly compatible with multiplexed and non-multiplexed microcontroller interfaces (Intel or Motorola type buses). The microprocessor interface signals are summarized in **table 3.**

Table 3

Pin No. P-DIP	Pin No. PL-CC	Symbol	Input (I) Output (O)	Function
37	41	AD0/D0	I/O	**Multiplexed Bus Mode: Address/Data Bus.** Transfers addresses from the µP system to the ISAC-S and data between the µP system and the ISAC-S. **Non-Multiplexed Bus Mode: Data Bus.** Transfers data between the µP system and the ISAC-S.
38	42	AD1/D1	I/O	
39	43	AD2/D2	I/O	
40	44	AD3/D3	I/O	
1	1	AD4/D4	I/O	
2	2	AD5/D5	I/O	
3	3	AD6/D6	I/O	
4	4	AD7/D7	I/O	
34	37	$\overline{CS}$	I	**Chip Select.** A 0 ("low") on this line selects the ISAC-S for a read/write operation.
–	36	R/$\overline{W}$	I	**Read/Write.** At 1 ("high"), identifies a valid µP access as a read operation. At 0, identifies a valid µP access as a write operation (Motorola bus mode).
35	36	$\overline{WR}$	I	**Write.** This signal indicates a write operation (Intel bus mode).
–	39	$\overline{DS}$	I	**Data Strobe.** The rising edge marks the end of a valid read or write operation (Motorola bus mode).
36	39	$\overline{RD}$	I	**Read.** This signal indicates a read operation (Intel bus mode).

Table 3 (cont'd)

Pin No. P-DIP	Pin No. PL-CC	Symbol	Input (I) Output (O)	Function
20	23	$\overline{INT}$	OD	**Interrupt Request.** The signal is activated when the ISAC-S requests an interrupt. It is an open drain output.
33	36	ALE	I	**Address Latch Enable.** A high on this line indicates an address on the external address bus (Multiplexed bus type only).
–	40	A0	I	Address bit 0 (non-multiplexed bus type).
–	6	A1	I	Address bit 1 (non-multiplexed bus type).
–	5	A2	I	Address bit 2 (non-multiplexed bus type).
–	18	A3	I	Address bit 3 (non-multiplexed bus type).
–	17	A4	I	Address bit 4 (non-multiplexed bus type).
–	10	A5	I	Address bit 5 (non-multiplexed bus type).

ISDN Oriented Modular (IOM) Interface

IOM-1

This interface consists of one data line per direction (IOM Data Ports 0 and 1: IDP0,1). Two additional signals define the data clock (DCLK) and the frame synchronization (FSC1/2) at this interface. The data clock has a frequency of 512 kHz (twice the data rate) and the frame sync clock has a repetition rate of 8 kHz.

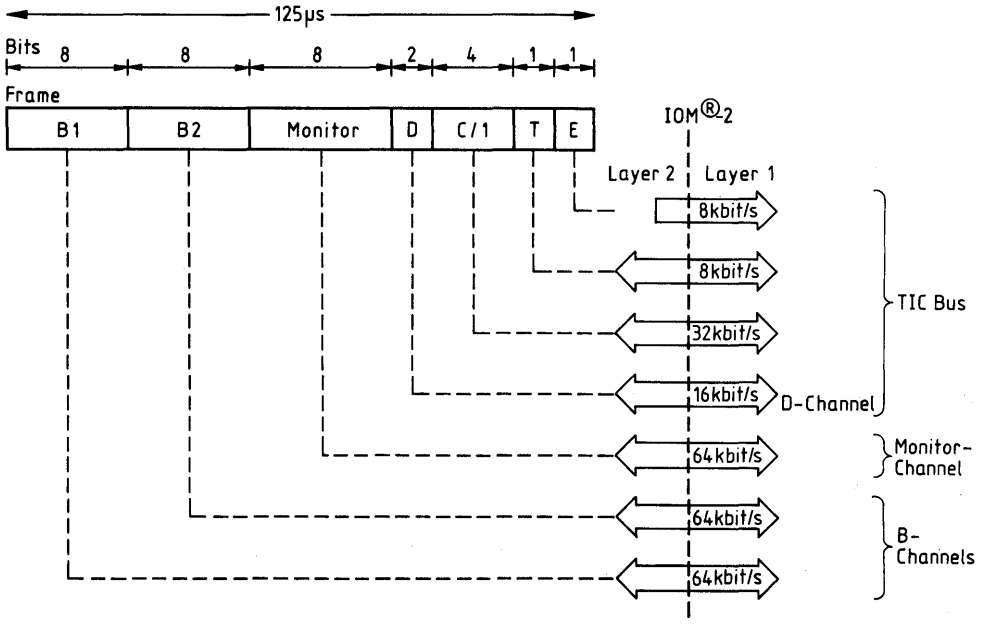
Via this interface four octets are transmitted per 125 µs frame **(figure 12)**. The first two octets constitute the two 64 kbit/s B channels. In the ISAC-S the monitor channel (third octet) serves:

- for arbitration of the access to IOM-TIC bus on IPD1 in case several layer-2 components are connected together **(figure 14)**.
- to indicate the status on the S bus D channel (IDP0, bit 3 of the monitor octet), "stop/go"
- for the exchange of data using the IOM-1 monitor channel protocol which involves the E bit as data validation bit.

Two bits in the fourth octet are used for the 16 bit/s D channel. The controling and monitoring of layer-1 functions (activation/deactivation of the S interface...) is done via the command/indication bits. The T bis is not used in ISAC-S IOM-1 applications.

The last octet in the IOM frame is called the Telecom IC bus (TIC) because of the offered busing capability.

Figure 12
IOM-1 Frame Structure



IOM-1 Timing

In TE mode the IOM timing is internally generated by DPLL circuitry from the S interface and DCLK and FSC 1/2 are outputs.

In LT-S, NT and LT-T modes the clock and frame synchronization signals are inputs.

The IOM interface can be operated either in timing mode 0 or in timing mode 1, selected by SPM bit in SPCR register.

Timing mode 0 **(SPM = 0)** must be programmed when ISAC-S is in TE mode.

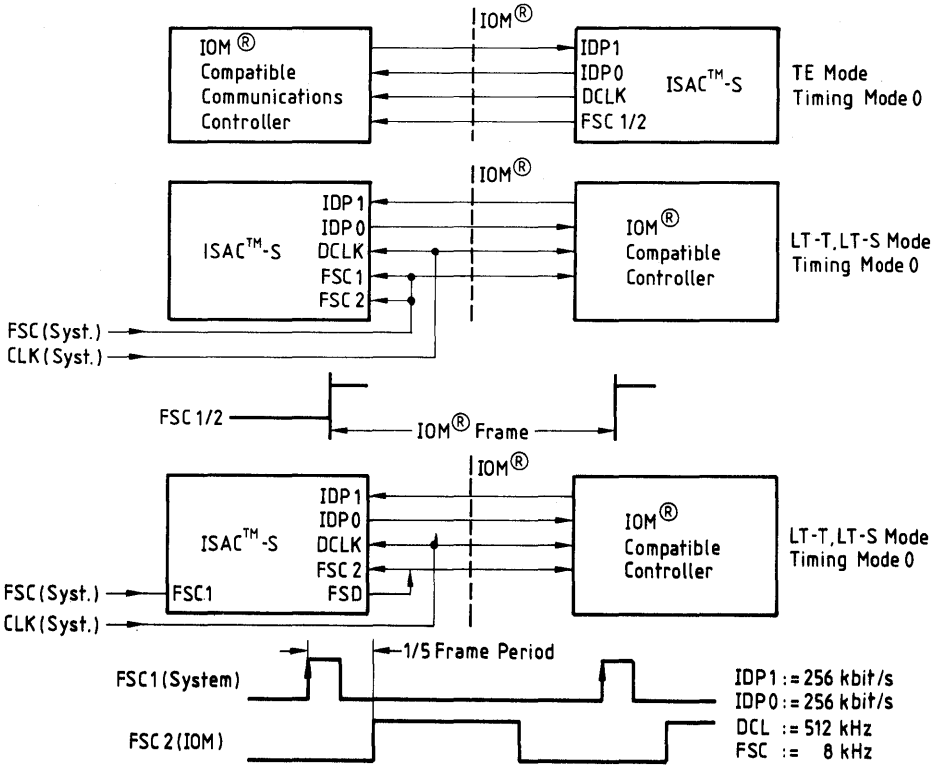
Timing mode 1 **(SPM = 1)** is only meaningful in exchange applications (LT-S, LT-T) when the SLD is used.

In timing mode 0 FSC1 and FSC2 should be connected to one another for correct operation (when FSC1/2 are input, i.e. in non-TE modes).

In timing mode 1 the IOM is synchronized by a frame signal FSD delayed in time with respect to the frame sync pulse input via FSC1. This reduces the B channel round-trip delay time when the SLD is used **(figure 13)**.

For correct operation in timing mode 1, the output FSD should be connected to FSC2 input **(see figure 10)**.

Figure 13
IOM-1 Interface Signals



The IOM interface has two different clocking states:

- Idle state → FSC1/2 and DCLK are disabled and both data lines are "High" (Power Down)
- Clocked state → FSC1/2 and DCLK are enabled (Stand By).

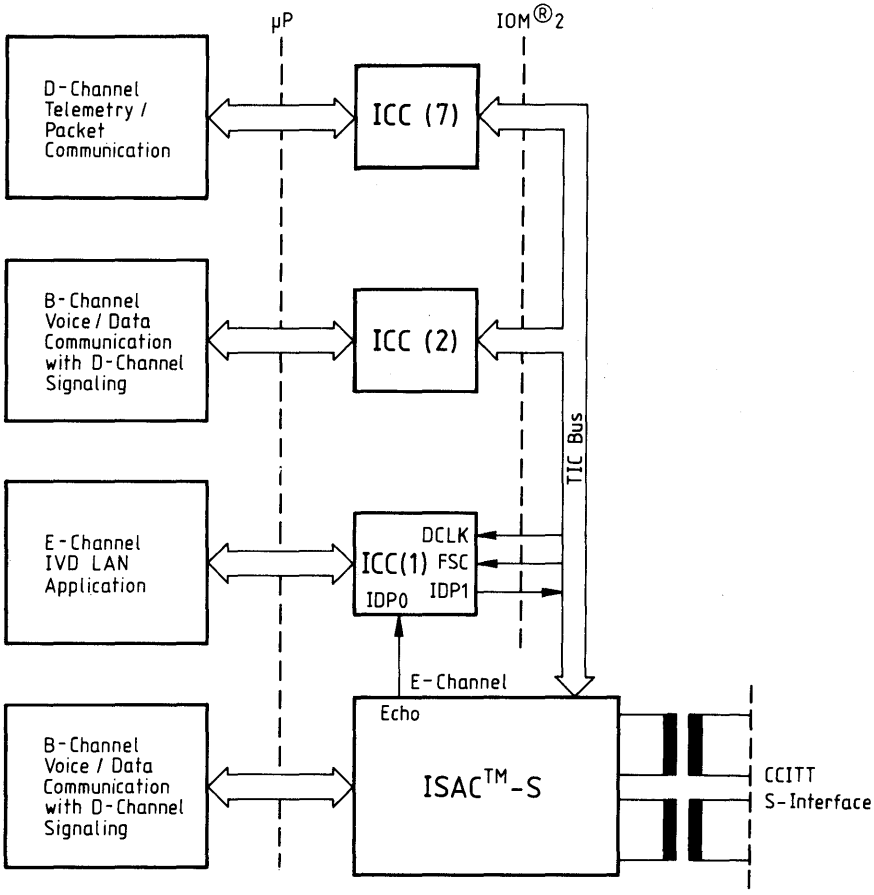
Unlike in digital exchange configurations, in which the IOM interface always remains in the synchronized state, in terminal equipment both clocking states can be selected.

The idle state is reached if the CFS (Configuration Select) bit in register SQXR is set to "1" and the S/T interface is inactive.

The transition from idle state to clocked state will be automatically initiated by an incoming call from network side. An activation of the IOM interface from the subscriber end has to be programmed by setting and resetting the SPU (Software Power Up) bit in the SPCR register, before the IOM interface can be used (e.g. for the activation/deactivation procedure at the S interface.

The arbitration mechanism implemented in the monitor channel of the IOM allows the access of external communication controllers (up to 7) to the layer-1 functions provided in the ISAC-S and to the D channel. (TIC bus; **see figure 14)**. To this effect the outputs of the controllers (ICC:ISDN Communication Controller 2070) are wired-or-ed and connected to pin IDP1, a pull-up resistor being already provided in the ISAC-S. The inputs of the ICCs are connected to pin IDP0.

Figure 14
Applications of IOM Bus Configuration



IOM-2

The IOM-2 is a generalisation and enhancement of the IOM-1. While the basic frame structure is very similar, IOM-2 offers further capacity for the transfer of maintenance information. In terminal applications, the IOM-2 constitutes a powerful backplane bus offering inter-communication and sophisticated control capabilities for peripheral modules.

Figure 15
Channel Structure of IOM-2

B1	B2	Monitor	D	C/I	MR	MX

- The 64 kbit/s channels, B1 and B2, are conveyed in the first two octets.
- The third octet (monitor channel) is used for transferring maintenance information between the layer-1 functional blocks (SBC, IBC, IEC) and the layer-2 controller.
- The fourth octet (control channel) contains
  - two bits for the 16 kbit/s D channel
  - four command/indication bits for controlling activation/deactivation and for additional control functions
  - two bits MR and MX for supporting the handling of the monitor channel.

In the case of an IOM-2 interface the frame structure depends on whether TE- or non-TE mode is selected, via bit SPM in SPCR register.

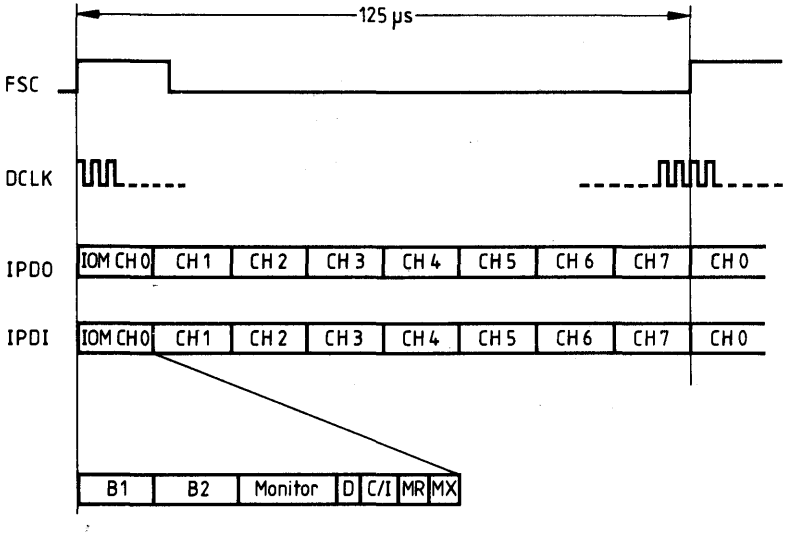
Non-TE Timing Mode (SPM = 1)

This mode is used in LT-S and LT-T applications. The frame is a multiplex of eight IOM-2 channels **(figure 16)**, each channel has the structure in **figure 15**.

Thus the data rate per subscriber connection (corresponding to one channel) is 256 kbit/s, whereas the bit rate is 2048 kbit/s. The IOM-2 interface signals are:

IDP0,1: 2048 kbit/s
DCLK: 4096 kHz input
FSC1: 8 kHz input

Figure 16
Multiplexed Frame Structure of the IOM-2 Interface in Non-TE Timing Mode



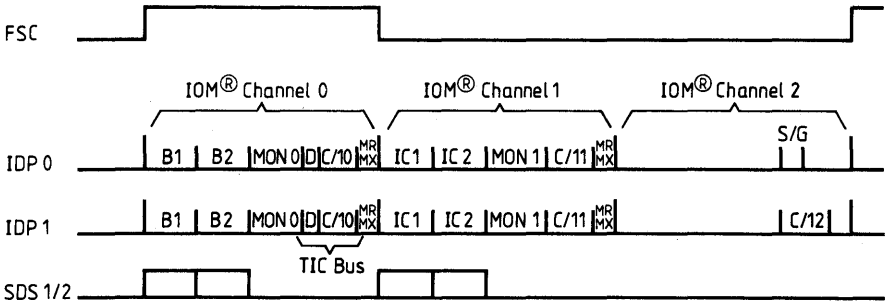
The ISAC-S is assigned to one of the eight channels (0 to 7) via register programming.

The Timing Mode (SPM = 0)

The frame is composed of three channels **(figure 17)**:

- Channel 0 contains 144 kbit/s (for 2B + D) plus monitor and command/indication channels for the layer-1 device.
- Channel 1 contains two 64 kbit/s intercommunication channels plus monitor and command/indication channels for other IOM-2 devices.
- Channel 2 is used for IOM bus arbitration (access to the TIC bus).

Figure 17
Definition of IOM-2 Channels in Terminal Mode



The IOM-2 signals are:

IDP0,1:	768 kbit/s	
DCLK:	1536 kHz	output
FSC1:	8 kHz	output.

In addition, to support standard combos/data devices the following signals are generated as outputs:

BCLK:	768 kHz	bit clock
SDS1/2:	8 kHz	programmable data strobe signals for selecting one or both B/IC channel(s).

The clocking states (idle/clocked) are identical to the IOM-1 case and are controlled in the same manner via bits CFS and SPU.

Important Note: If the ISAC-S is configured in NT mode, the IOM frame structure is identical to that of the IOM-1 case.

SSI (Serial Port A)

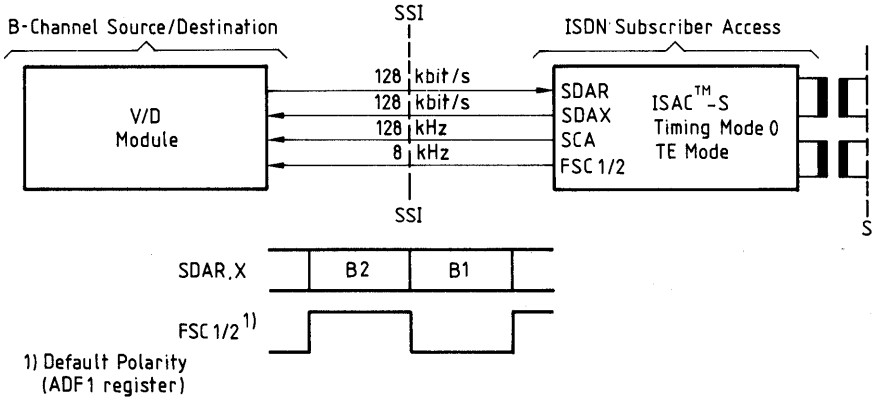
The SSI (Serial Synchronous Interface) is available in IOM-1 interface mode. Timing mode 0 (SPM = 0) and TE operation has to be programmed.

The serial port SSI serves as a full duplex connection to B- channel sources/destinations in terminal equipment with a data rate of 128 kbit/s.

It consists of one data line in each direction (SDAX and SDAR), an 8-kHz strobe output (FSC1 and/or FSC2) and the 128-kHz clock output (SDA).

Figure 18

Connection of B-Channel Sources/Destinations to the ISAC-S via SSI



This serial interface allows the connection of voice/data modules, such as serial synchronous transceiver devices (USART's, ICC PEB 2070, HSCX SAB 82525, ITAC PSB 2110,...) and various codec filters directly to the ISAC-S, as illustrated in **figure 18**.

By programming the ADF1 register it is possible to independently set the strobe signal FSC1/2 polarities so that either B1 or B2 is selected by the V/D module.

The µC system has access to B-channel data via the ISAC-S registers BCR1/2 and BCX1/2.

The µC access must be synchronized to the serial transmission by means of the Synchronous Transfer Interrupt (STCR).

SLD

The SLD is available in IOM-1 interface mode.

The standard SLD interface is a three-wire interface with a 512-kHz clock (DCLK), an 8-kHz frame direction signal (TE mode: FSC1/2 output; LT-S/LT-T modes: FSC1 sync input), and a serial ping-pong data lead (SIP) with an effective full duplex data rate of 256 kbit/s.

The frame is composed of four octets per direction. Octets 1 and 2 contain the two B channels, octet 3 is a feature control byte, and octet 4 is a signaling byte **(figure 19)**.

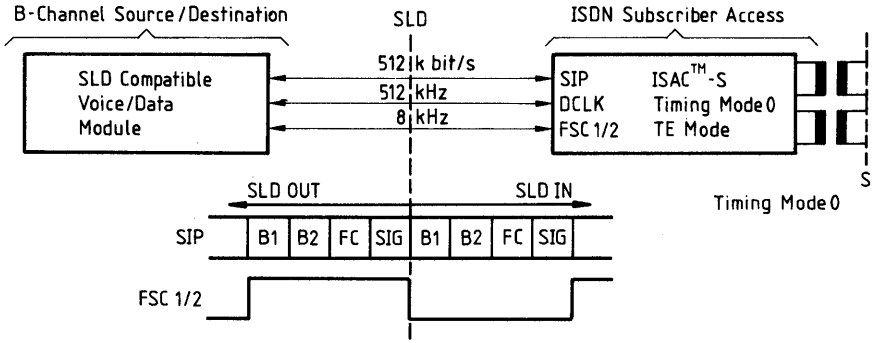
The SLD interface can be used in:

– **Terminal applications** (TE) as a full duplex time-multiplexed (ping-pong) connection to B-channel sources/destinations.

  Codec filters, such as the SICOFI (PEB 2060) or the ARCOFI (PSB 2160) as well as other SLD compatible voice/data modules may be connected directly to the ISAC-S as depicted in **figure 19.** In TE applications timing mode 0 has to be programmed, hence SLD operates in master mode. Moreover, terminal specific functions have to be deselected (TSF = 0).

Figure 19

Connection of B-Channel Destinations to the ISAC-S via SLD

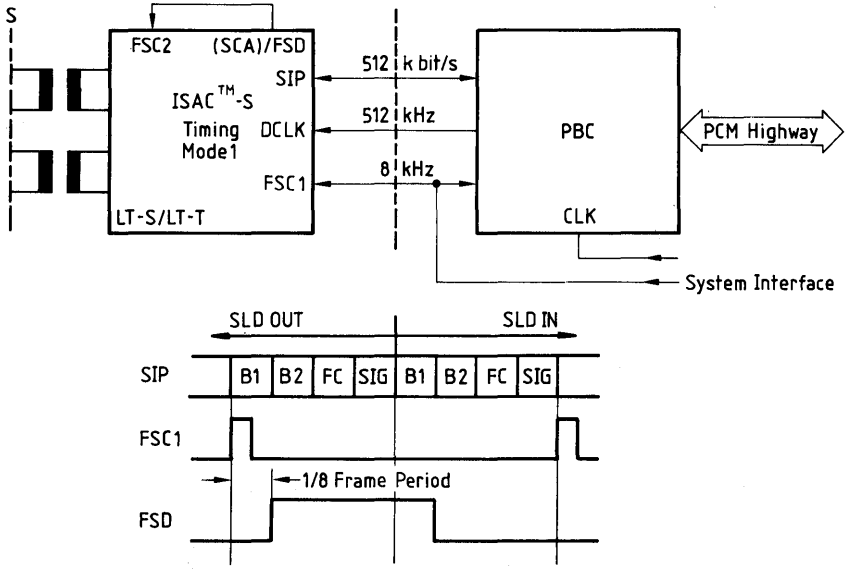


– **Digital exchange applications** (LT-S/LT-T) as a full duplex time-multiplexed connection to convey the B channels between the S/T interface and a Peripheral Board Controller (e.g. PBC PEB 2050 or PIC PEB 2052), which performs time-slot assignment on the PCM highways, forming a system interface to a switching network **(figure 20)**.

Timing mode 1 (SPM = 1) has to be programmed, hence SLD operates in slave mode.

Figure 20

Connection of the ISAC-S as B-Channel Source/Destination to a Peripheral Board Controller via SLD



The µC system has access to B-channel data, the feature control byte and the signaling byte via the ISAC-S registers:

– C1R, C2R → B1/B2
– MOR1 and MOR2 → FC
– CIR1 and CIR1 → SIG

The µP access to C1R, C2R, MOR1/MOX1, CIR1 and CIX1 must be synchronized to the serial transmission by means of the Synchronous Transfer Interrupt (STCR) and the BVS-bit (STAR).

Individual Functions

Layer-1 Functions for the ISDN Basic Access

The common functions in all operating modes are:

- line transceiver functions for the S/T interface according to the electrical specifications of CCITT I.430;
- conversion of the frame structure between IOM and S/T interface;
- conversion from/to binary to/from pseudo-ternary code;
- level detect.

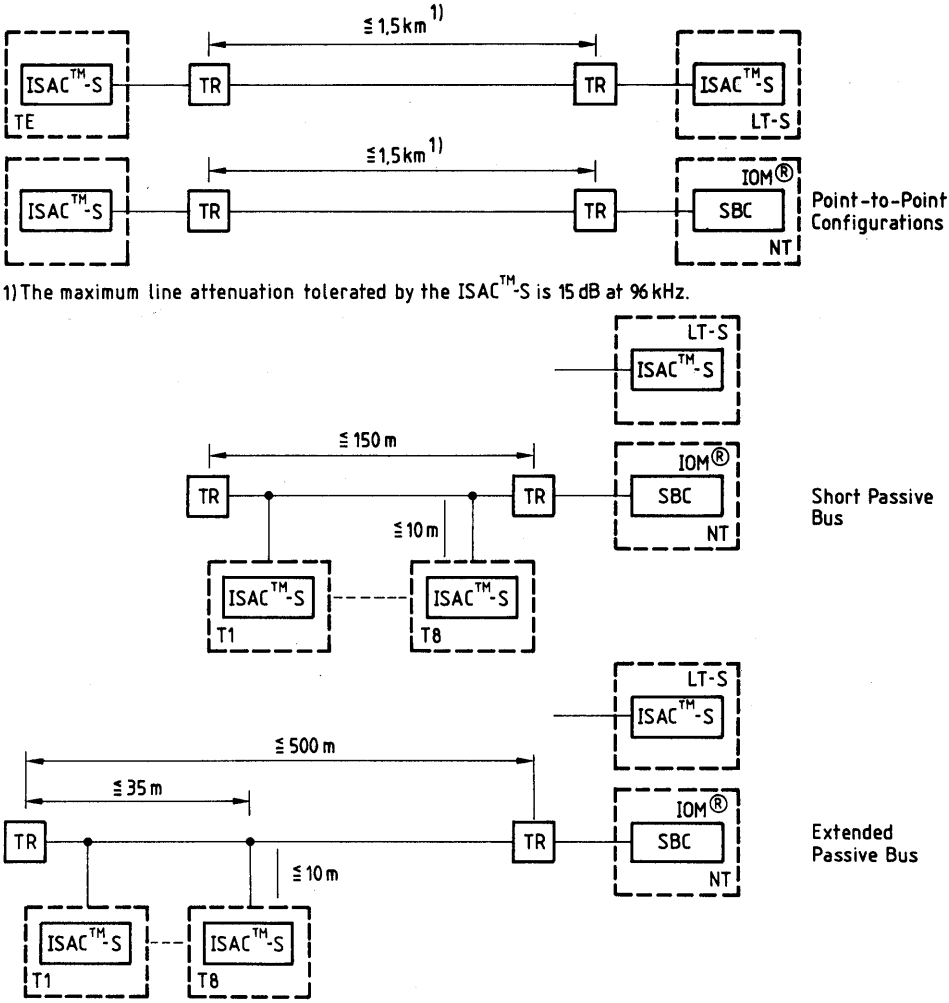
Mode specific functions are:

- receive timing recovery for point-to-point, passive bus and extended passive bus configuration;
- S/T timing generation using IOM timing synchronous to system, or vice versa;
- D-channel access control and priority handling;
- D-channel echo bit generation by handling of the global echo bit;
- activation/deactivation procedures, triggered by primitives received over the IOM C/I channel or by INFO's received from the line;
- frame alignment according to CCITT Q.503;
- execution of test loops.

For a block diagram, **see figure 9**.

The wiring configurations in user premises, in which the ISAC-S can be used are illustrated in **figure 21**.

Figure 21
Wiring Configurations in User Premises



1) The maximum line attenuation tolerated by the ISAC™-S is 15 dB at 96 kHz.

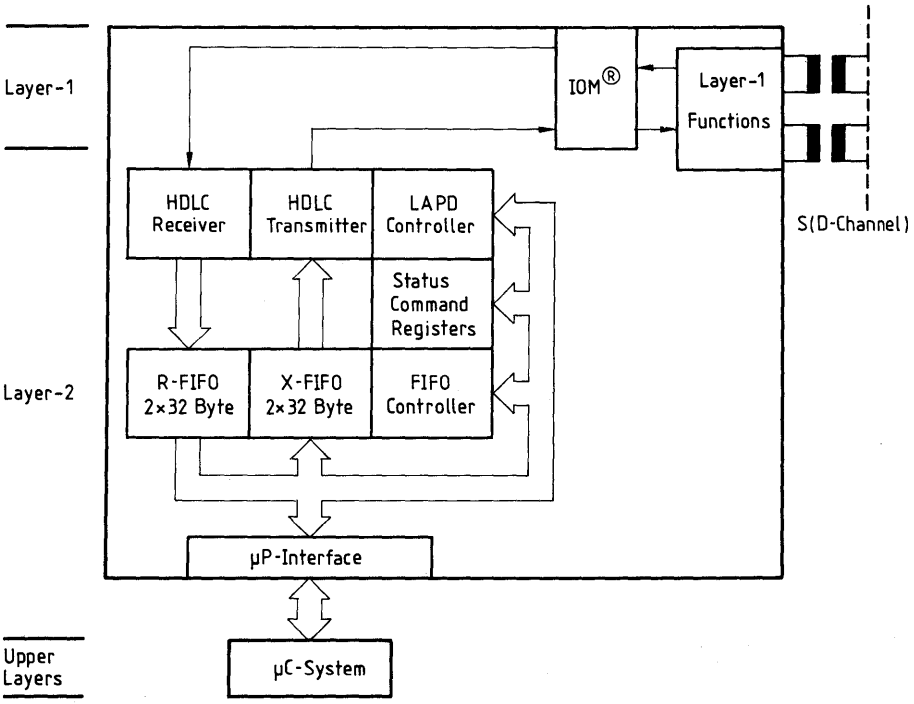
Layer-2 Functions for the ISDN Basic Access

LAPD, layer 2 of the D-channel protocol (CCITT .441) includes functions for:

- Provision of one or more data link connections on a D channel (multiple LAP). Discrimination between the data link connections is performed by means of a data link connection identifier (DLCI = SAPI + TEI)
- HDLC-framing
- Application of a balanced class of procedure in point-multipoint configuration.

The simplified block diagram in **figure 22** shows the functional blocks of the ISAC-S which support the LAPD protocol.

Figure 22
D-Channel Processing of the ISAC-2



For the support of LAPD the ISAC-S contains an HDLC transceiver which is responsible for flag generation/recognition, bit stuffing mechanism, CRC check and address recognition.

A powerful FIFO structure with two 64-byte pools for transmit and receive directions and an intelligent FIFO controller permit flexible transfer of protocol data units to and from the µC system.

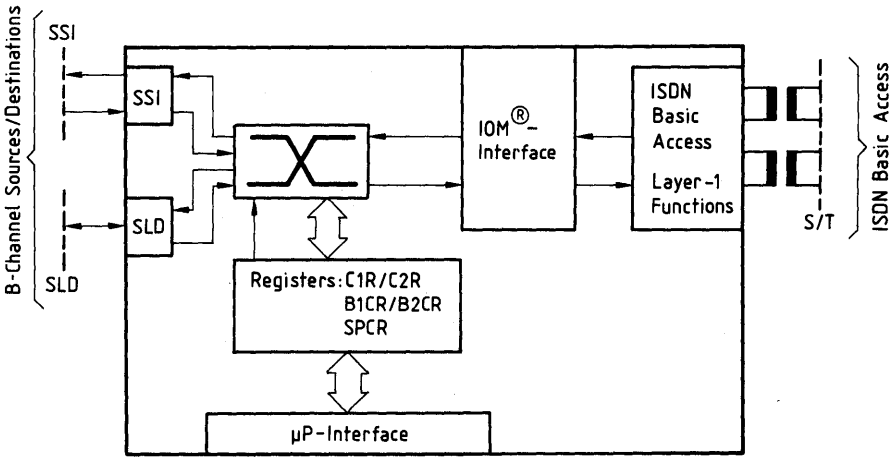
B Channel Switching (IOM-1)

The ISAC-S contains two serial interfaces, SLD and SSI, which can serve as interfaces to B channel sources/destinations. Both channels B1 and B2 can be switched independently of one another to the IOM interface and to the four-wire S/T interface **(figure 23)**.

The following possibilities are provided:

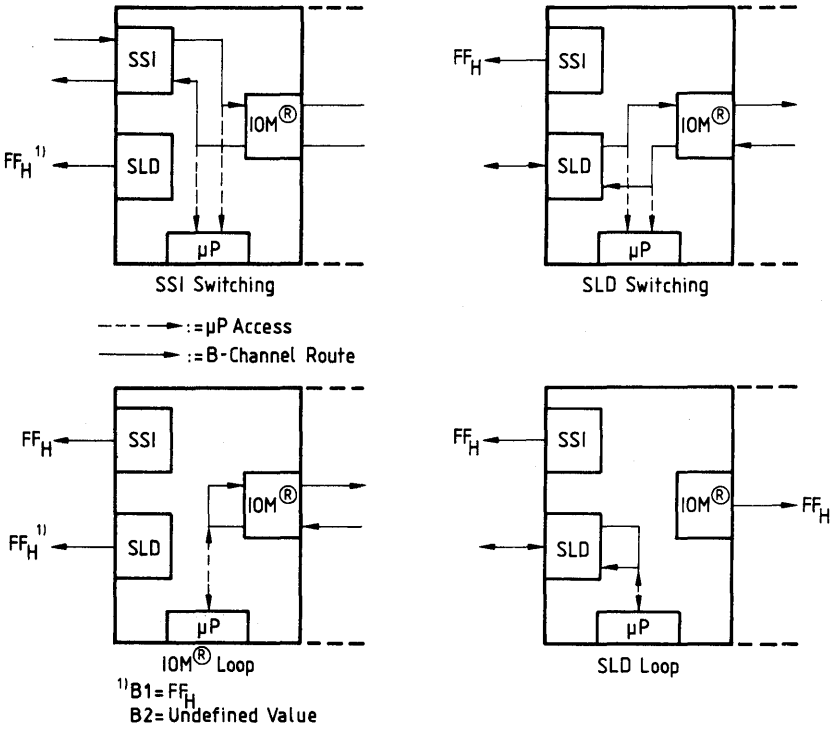
- Switching from/to SSI
- Switching from/to SLD
- IOM looping
- SLD looping

Figure 23
Principle of B-Channel Switching



The microcontroller can select the B-channel switching in the SPCR register. In **figure 24** all possible selections of the B-channel routes and access to B-channel data via the microprocessor interface are illustrated. This access from the microcontroller is possible by writing or reading the C1R/C2R register on reading the B1CR/B2CR register.

Figure 24
B-Channel Routes and Access to B-Channel Data



Access to B/IC Channels

IOM-1 Mode (IMS = 0)

The B1 and/or B2 channel is accessed by reading the B1CR/B2CR or by reading and writing the C1R/C2R registers. The µP access can be synchronized to the serial interface by means of a synchronous transfer programmed in the STCR register.

The read/write access possibilities are shown in **table 4**.

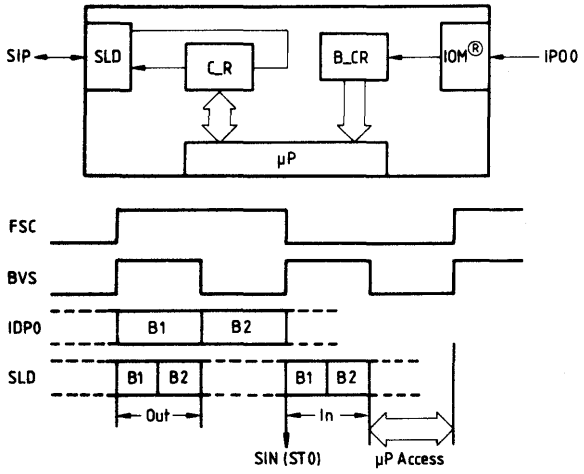
Table 4
µP Access to B Channel

		C_R		B_CR	
C_C1	**C_C0**	**Read**	**Write**	**Read**	**Application(s)**
0	0	SLD	SLD	IOM	B_not switched, SLD looping
0	1	SLD	–	IOM	B_switched to/from SLD
1	0	SSI	–	IOM	B_switched to/from SSI
1	1	IOM	IOM	–	IOM looping

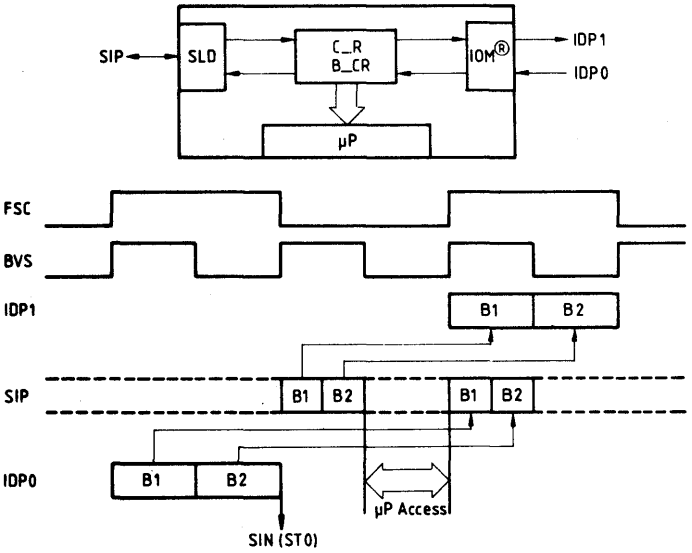
The synchronous transfer interrupt (SIN, ISTA register) can be programmed to occur at either the beginning of a 125 µs frame or at its center, depending on the channel(s) to be accessed and the current configuration, **see figure 25.**

Figure 25
B-Channel Access

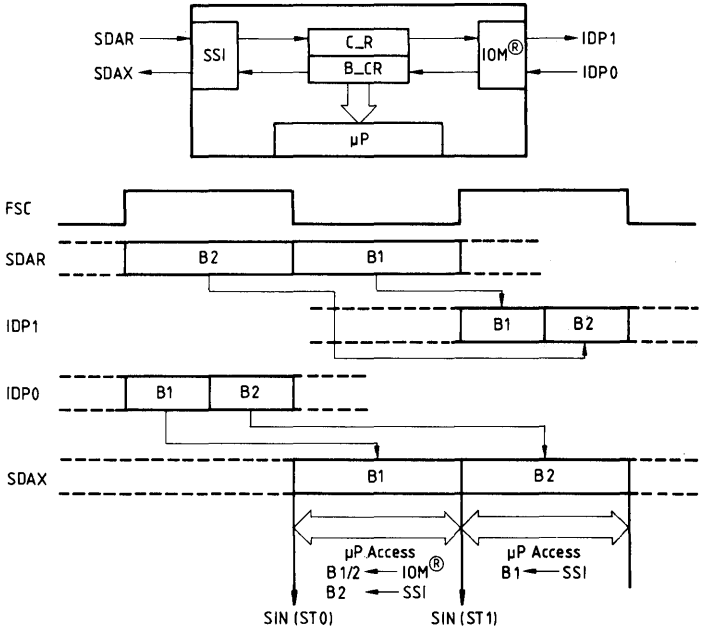
(a) C_C1, C_C0 = 00
SLD loop



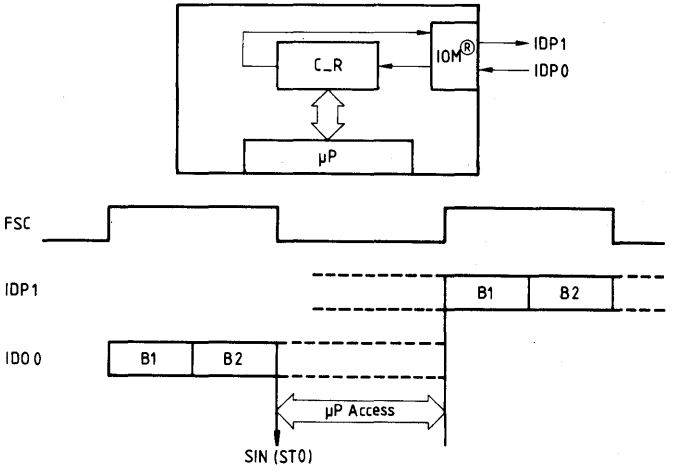
(b) C_C1, C_C0 = 01
SLD – IOM connection



(c) C_C1, C_C0 = 10
SSI – IOM connection



(d) C_C1, C_C0 = 11
IOM loop



IOM-2 Mode (IMS = 1)

The B1, B2 and/or IC1, IC2 channels are accessed by reading the B1CR/B2CR or by reading and writing the C1R/C2R registers. The µP access can be synchronized to the IOM interface by means of a synchronous transfer programmed in the STCR register.

The read/write access possibilities are shown in **table 5**.

Table 5
µP Access to B/IC Channels

C_C1	C_C0	C_R Read	C_R Write	B_CR Read	Output to IOM-2	Application(s)
0	0	IC_	–	B_	–	B_monitoring, IC_ monitoring
0	1	IC_	IC_	B_	IC_	B_monitoring, IC_looping from/to IOM-2
1	0	–	B_	B_	B_	B_access from/to S_0; transmission of a constant value in B_channel to S_0.
1	1	B_	B_	–	B_	B_looping from S_0; transmission of a variable pattern in B_channel to S_0.

The general sequence of operations to access the B/IC channels is:

(set configuration, register SPCR)

→ Program synchronous interrupt (ST0)

SIN → Read register (B_CR, C_R)
(write register)

Acknowledge SIN (SC0)

C/I Channel Handling

The command/indication channel carries real-time status information between the ISAC-S and another device connected to the IOM.

1) One C/I channel (called C/I0) conveys the commands and indications between a layer-1 device and a layer-2 device. This channel is available in all timing modes (IOM-1 or IOM-2). It can be accessed by an external layer-2 device e.g. to control the layer-1 activation/deactivation procedures. C/I0 channels access is arbitrated via the TIC bus access protocol:

– in IOM-1 mode, this arbitration is done in the monitor channel
– in IOM-2 TE timing mode, this arbitration is done in C/I channel 2 **(figure 17)**.

The C/I0 channel is accessed via register CIR0 (in receive direction, layer 1 to layer 2) and register CIX0 (in transmit direction, layer 2 to layer 1). The C/I0 code is four bits long.

In the receive direction, the code from layer 1 is continuously monitored, with an interrupt being generated anytime a change occurs. A new code must be found in two consecutive IOM frames to be considered valid and to trigger a C/I code change interrupt status (double last look criterion).

In the transmit direction, the code written in CIX0 is continuously transmitted in C/I0.

2) A second C/I channel (called C/I1) can be used to convey real time status information between the ISAC-S and various non-layer-1 peripheral devices e.g. PSB 2160 ARCOFI. The channel consists of six bits in each direction. It is available only in the IOM-2 TE timing mode **(see figure 17)**.

   The C/I1 channel is accessed via registers CIR1 and CIX1. A change in the received C/I1 code is indicated by an interrupt status without double last look criterion.

Monitor Channel Handling

IOM-1

The monitor channel protocol can be used to exchange one byte of information at a time between the ISAC-S and another device (e.g. a layer-1 transceiver).

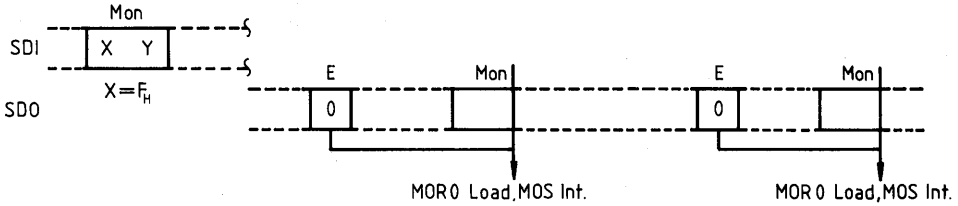
The procedure is as follows:

Monitor transmit channel 0 (MOX0) register is loaded with the value to be sent in the outgoing monitor channel. (Bytes of the form Fx_H are not allowed for this purpose because of the TIC bus collision resultion procedure).

The receiving device interprets the incoming monitor value as a control/information byte, Fx_H excluded. If no response is excepted, the procedure is complete. If the receiving device shall react by transmitting information to the ISAC-S, it should set the E bit to 0 and send the response in the monitor channel of the following frame. The ISAC-S

- latches the value in the monitor channel of the frame immediately following a frame with "E = 0" into MOR0 register.
- generates a monitor status interrupt MOS (EXIR register) to indicate that the MOR0 register has been loaded **(see figure 26)**.

Figure 26
Monitor Channel Protocol (IOM-1)



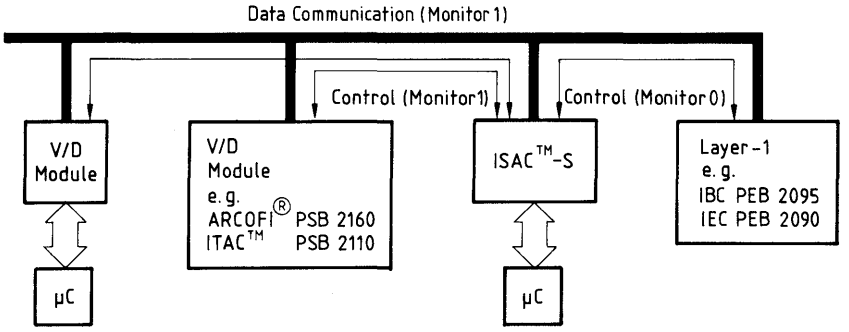
IOM-2

In this case, the monitor channel protocol is a handshake protocol used for high speed information exchange between the ISAC-S and other devices, in monitor channel 0 or 1 **(see figure 17)**. In the non-TE mode, only one monitor channel is available ("monitor channel 0").

The monitor channel protocol is necessary **(see figure 27)**:

- For programming and controlling devices attached to the IOM. Examples of such devices are: layer-1 transceivers (using monitor channel 0), and peripheral V/D modules that do not have a parallel microcontroller interface (monitor channel 1), such as the audio ringing codec filter PSB 2160.
- For data exchange between two microcontroller systems attached to two different devices on one IOM-2 backplane. Use of the monitor channel avoids the necessity of a dedicated serial communication path between the two systems. This greatly simplifies the system design of terminal equipment **(figure 27)**.

Figure 27
Examples of Monitor Channel Applications



The monitor channel operates on an asynchronous basis. While data transfers on the bus take place synchronized to frame sync, the flow of data is controlled by a handshake procedure using the Monitor Channel Receive (MR0 or 1) and Monitor Channel Transmit (MX0 or 1) bits. For example: data is placed onto the monitor channel and the MX bit is activated. This data will be transmitted repeatedly once per 8-kHz frame until the transfer is acknowledged via the MR bit.

The microprocessor may either enforce a "1" (idle) in MR, MX by setting the control bit MRC1,0 or MXC1,0 to "0" (MOnitor Control Register MOCR), or enable the control of these bits internally by the ISAC-S according to the monitor channel protocol. Thus, before a data exchange can begin, the control bit MRC(1,0) or MXC(1,0) should be set to "1" by the microprocessor.

The monitor channel protocol is illustrated in **figure 28**. Since the protocol is identical in monitor channel 0 and monitor channel 1 (available in TE mode only), the index 0 or 1 has been left out in the illustration.

The relevant status bits are:

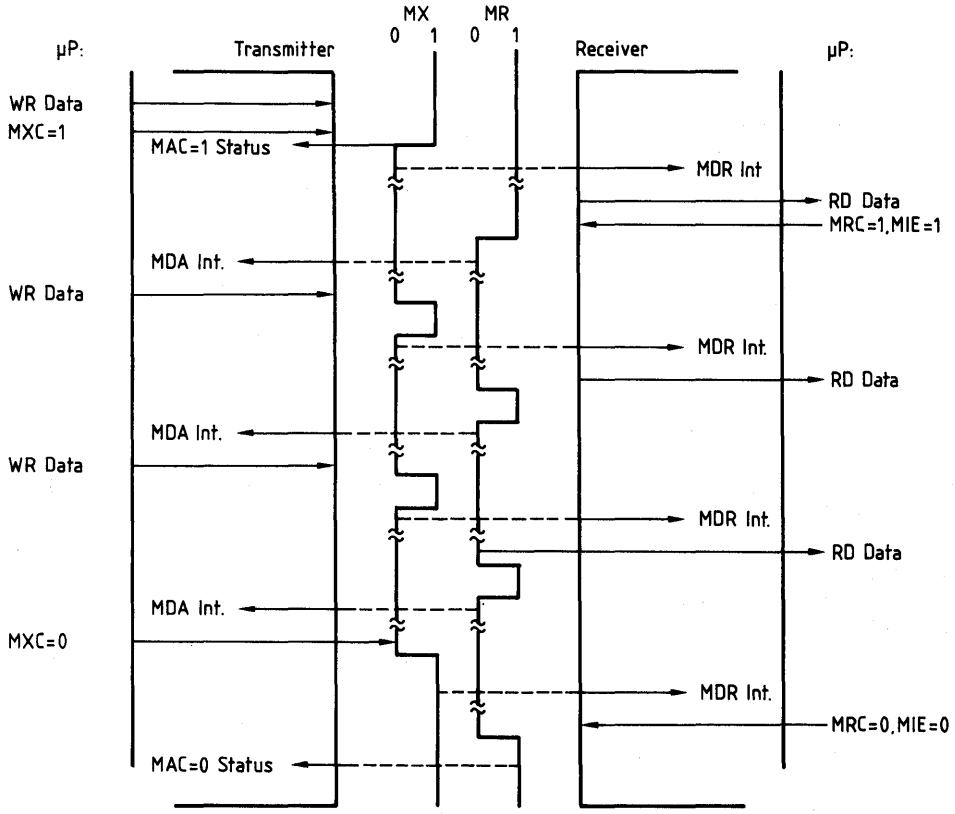
Monitor Channel Data Received MDR (MDR0, MDR1)
Monitor Channel End of Reception MER (MER0, MER1)

for the reception of monitor data, and

Monitor Channel Data Acknowledged MDA (MDA0, MDA1)
Monitor Channel Data Abort MAB (MAB0, MAB1)

for the transmission of monitor data (Register: MOSR).
In addition, the status bit:
Monitor Channel Active MAC (MAC0, MAC1)
indicates whether a transmission is in progress (Register: STAR).

Figure 28
Monitor Channel Protocol



Before starting a transmission, the microprocessor should verify that the transmitter is inactive, i.e. that a possible previous transmission has been terminated. This is indicated by a "0" in the monitor channel active MAC status bit.

After having written the monitor data transmit (MOX) register, the microprocessor sets the monitor transmit control bit MXC to 1. This enables the MX bit to go active (0), indicating the presence of valid monitor data (contents of MOX) in the corresponding frame. As a result, the receiving device stores the monitor byte in its monitor receive MOR register and generates a MDR interrupt status.

Alerted by the MDR interrupt, the microprocessor reads the monitor receive (MOR) register. When it is ready to accept data (e.g. based on the value in MOR, which in a point-to-multipoint application might be the address of the destination device), it sets the MR control bit MRC to "1" to enable the receiver to store succeeding monitor channel bytes and acknowledge them according to the monitor channel protocol. In addition, it enables other Monitor channel interrupts by setting monitor interrupt enable to "1".

As a result, the first monitor byte is acknowledged by the receiving device setting the MR bit to "0". This causes a monitor data acknowledge MDA interrupt status at the transmitter.

A new monitor data byte can now be written by the microprocessor in MOX. The MX bit is still in the active (0) state. The transmitter indicates a new byte in the monitor channel by returning the MX bit active after sending it once in the inactive state. As a result, the receiver stores the monitor byte in MOR and generates a new MDR interrupt status. When the microprocessor has read the MOR register, the receiver acknowledges the data by returning the MR bit active after sending it once in the inactive state. This in turn causes the transmitter to generate a MDA interrupt status.

This "MDA interrupt – write data – MDR interrupt – read data – MDA interrupt" handshake is repeated as long as the transmitter has data to send. Note that the monitor channel protocol imposes no maximum reaction times to the microprocessor.

When the last byte has been acknowledged by the receiver (MDA interrupt status), the microprocessor sets the monitor transmit control bit MXC to 0. This enforces an inactive ("1") state in the MX bit. Two frames of MX inactive signifies the end of a message. Thus, a monitor channel end of reception MER interrupt status is generated by the receiver when the MX is received in the inactive state in two consecutive frames. As a result, the microprocessor sets the MR control bit MRC to 0, which in turn enforces an inactive state in the MR bit. This marks the end of the transmission, making the monitor channel active MAC bit return to "0".

During a transmission process, it is possible for the receiver to ask a transmission to be aborted by sending a inactive MR bit value in two consecutive frames. This is effected by the microprocessor writing the MR control bit MRC to 0. An aborted transmission is indicated by a monitor channel data abort MAB interrupt status at the transmitter.

Terminal Specific Functions

In addition to the ISAC-S standard functions supporting the ISDN basic access, the ISAC-S contains optional functions, useful in various terminal configurations.

The terminal specific functions are enabled by setting bit TSF (STCR register) to "1". This has two effects:

- The SIP/EAW line is defined as external awake input (and not as SLD line);
- Second, the interrupts SAW and WOV (EXIR register) are enabled:
  - SAW (subscriber awake) generated by a falling edge on the EAW line
  - WOV (watchdog timer overflow) generated by the watchdog timer. This occurs when the processor fails to write two consecutive bit patterns in ADF1:

ADF1	WTC1	WTC2	

Watchdog Timer Control 1, 0.

The WTC1 and WTC2 bits have to be successively written in the following manner within 128 ms:

	WTC1	WTC2
1.	1	0
2.	0	1

As a result the watchdog timer is reset and restarted. Otherwise a WOV is generated.

Deactivating the terminal specific functions is only possible with a hardware reset.

Having enabled the terminal specific functions via TSF = 1, the user can make the ISAC-S generate a reset signal by programming the Reset Source Select **RSS** bit (CIX0 register), as follows:

0 → A reset signal is generated as a result of
  - a falling edge on the EAW line (subscriber awake)
  - a C/I code change (exchange awake).

  A falling edge on the EAW line also forces the IDP1 line of the IOM interface to zero. The consequence of this is that the IOM interface and the ISAC-S leaves the power-down state.

  A corresponding interrupt status (CISQ or SAW) is also generated.

1 → A reset signal is generated as a result of the expiration of the watchdog timer (indicated by the WOV interrupt status).

  Note that the watchdog timer is not running when the ISAC-S is in the power-down state (IOM not clocked).

Note: Bit RSS has a signifinace only if terminal specific functions are activated (TSF = 1).

The RSS bit should be set to "1" by the user when the ISAC-S is in power-up to prevent an edge on the EAW line or a change in the C/I code from generating a reset pulse.

Switching RSS from 0 to 1 or from 1 to 0 resets the watchdog timer.

The reset pulse generated by the ISAC-S (output via RST pin) has a pulse width of:

- 125 µs when generated by the watchdog timer
- 16 ms when generated by EAW line or C/I code change.

Test Functions

The ISAC-S provides several test and diagnostic functions which can be grouped as follows:

- Digital loop via TLP (test loop, SPCR register) command bit: IDP1 is internally connected with IDP0, output from layer 1 (S/T) on IDP0 is ignored; this is used for testing ISAC-S functionality excluding layer 1;
- Test of layer-2 functions while disabling all layer-1 functions and pins associated with them (including clocking, in TE mode), via bit TEM (test mode, SQXR register); the ISAC-S is the fully compatible to the ICC (PEB 2070) seen at the IOM interface.
- Loop at the analog end of the S interface; either info 0 (non-transparent loop: TE/LT-T modes) or info 4 transparent loop: NT/LT-S modes) is sent over the S/T interface during the loop, which is closed via a C/I command written in CIX0 register;
- Special loops programmed via C2C1-0 and C1C1-0 bits (register SPCR);
- Transmission of special test signals on the S/T interface according to the modified AMI code, initiated via a C/I command written in CIX0 register:
  - Single pulses of alternating polarity, one S/T interface bit period wide, with a 2-kHz repetition frequency;
  - Continuous pulses of alternating polarity, one S/T interface bit period wide, with a 96-kHz repetition frequency.

Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Voltage on any pin with respect to ground	V_S	−0.4 to V_{DD} +0.4	V
Ambient temperature under bias	T_A	0 to 70	°C
Storage temperature	T_{stg}	−65 to 125	°C

DC Characteristics

$T_A = 0$ to 70 °C; $V_{DD} = 5\ V \pm 5\%$, $V_{SSA} = 0\ V$, $V_{SSD} = 0\ V$

Parameter		Symbol	Limit Values min.	Limit Values max.	Unit	Test Conditions	Remarks
L-input voltage		V_{IL}	−0.4	0.8	V		All pins except SX1,2, SR1,2
H-input voltage (all except X1 and RST)		V_{IH}	2.0	V_{DD} +0.4	V		All pins except SX1,2 SR1,2
L-output voltage L-output voltage (IDPO)		V_{OL} V_{OL1}		0.45 0.45	V V	$I_{OL} = 2$ mA $I_{OL} = 7$ mA	All pins except SX1,2 SR1,2
H-output voltage H-output voltage		V_{OH} V_{OH}	2.4 V_{DD} −0.5		V V	$I_{OH} = -400$ µA $I_{OH} = -100$ µA	All pins except SX1,2 SR1,2
Power supply current	operation	I_{CC}		15 17 27	mA mA mA	DCLK = 512 kHz DCLK = 1536 kHz DCLK = 4096 kHz	$V_{DD} = 5$ V Inputs at V_{SS}/V_{DD} No output loads
	power down	I_{CC}		1.5	mA		
Input leakage current Output leakage current		I_{LI} I_{LO}		10	µA	0 V < V_{IN} < V_{DD} to 0 V 0 V < V_{OUT} < V_{DD} to 0 V	All pins except SX1,2, SR1,2
Absolute value of output pulse amplitude $V_{SX2} - V_{SX1}$		V_X	2.03 2.10	2.31 2.39	V V	$R_L = 50\ \Omega$ [1] $R_L = 400\ \Omega$ [1]	SX1,2
Transmitter output current		I_X	7.5	13.4	mA	$R_L = 5.6\ \Omega$ [1]	SX1,2
Transmitter output impedance		R_X	10		kΩ	Inactive or during binary one	SX1,2
			0		Ω	during binary zero $R_L = 50\ \Omega$	
Receiver output voltage		V_{SR1}	2.4	2.6	V	$I_O < 5$ µA	SR1,2
Receiver threshold voltage $V_{SR2} - V_{SR1}$		V_{TR}	+225	+375	mV	Dependent on peak level	SR1,2

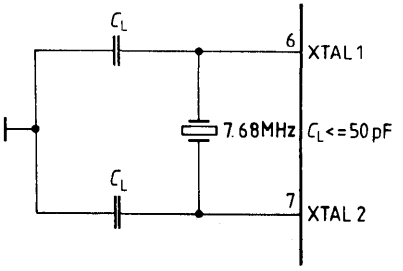
[1]) Due to the transformer, the load resistance seen by the circuit is four times R_L.

Capacitances

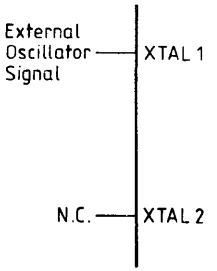
$T_A = 25\,°C$; $V_{DD} = 5\,V \pm 5\%$, $V_{SSD} = 0\,V$

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Input capacitance I/O capacitance	C_{IN} C_{IO}		7 7	pF pF	All pins except SR1,2, XTAL1,2
Output capacitance against V_{SSA}	C_{OUT}		10	pF	SX1,2
Input capacitance	C_{IN}		7	pF	SR1,2
Load capacitance	C_L		50	pF	XTAL1,2

Recommended Oscillator Circuits



Crystal Oscillator Mode



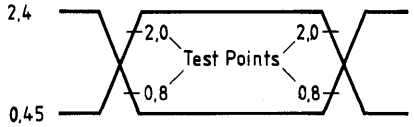
Driving from External Source

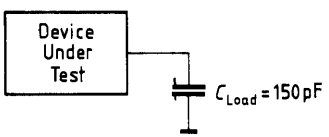
AC Characteristics

$T_A = 0$ to $70\,°C$; $V_{DD} = 5\,V \pm 5\%$

Inputs are driven to 2.4 V for a logical "1" and to 0.4 V for a logical "0". Timing measurements are made at 2.0 V for a logical "1" and 0.8 V for a logical "0". The AC testing input/output waveforms are shown below.

Figure 29
Input/Output Waveform for AC Test

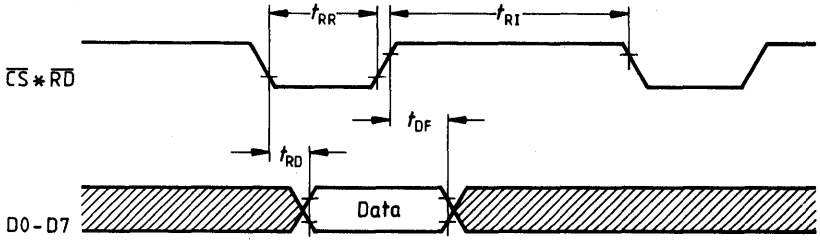




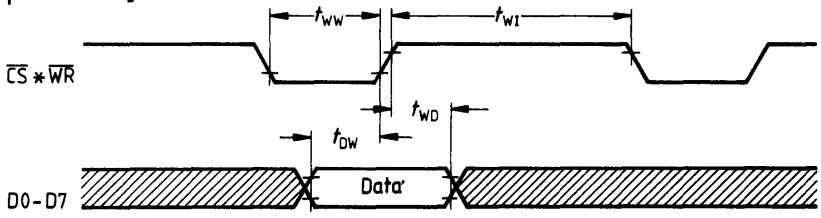
Microprocessor Interface Timing

Intel Bus Mode

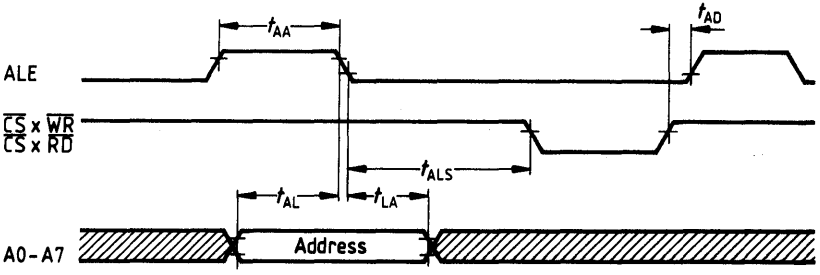
µP Read Cycle



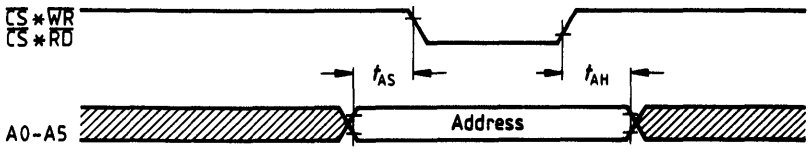
µP Write Cycle



Multiplexed Address Timing

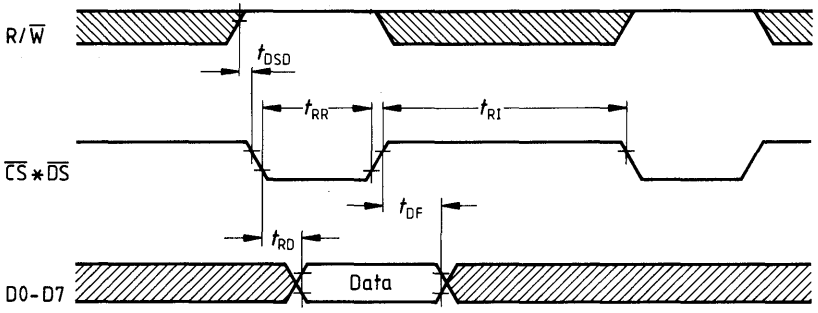


Non-multiplexed Address Timing

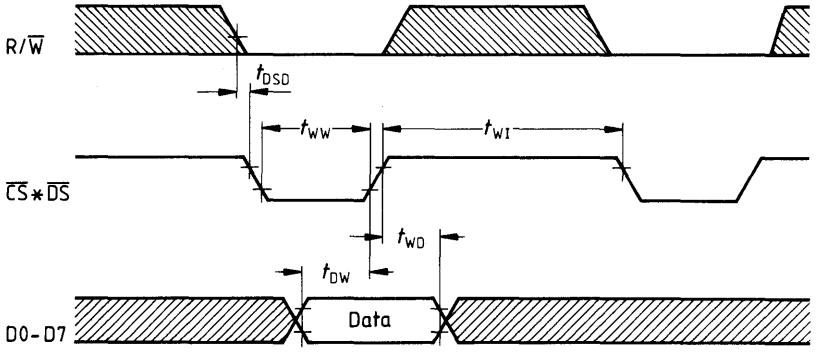


Motorola Bus Mode

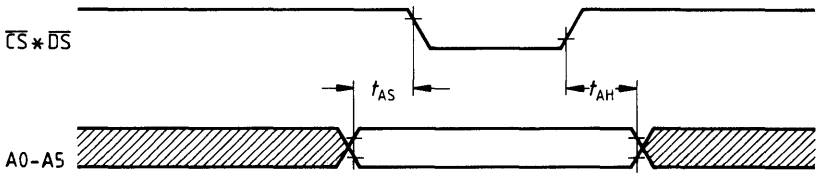
µP Read Cycle



µP Write Cycle



Address Tming

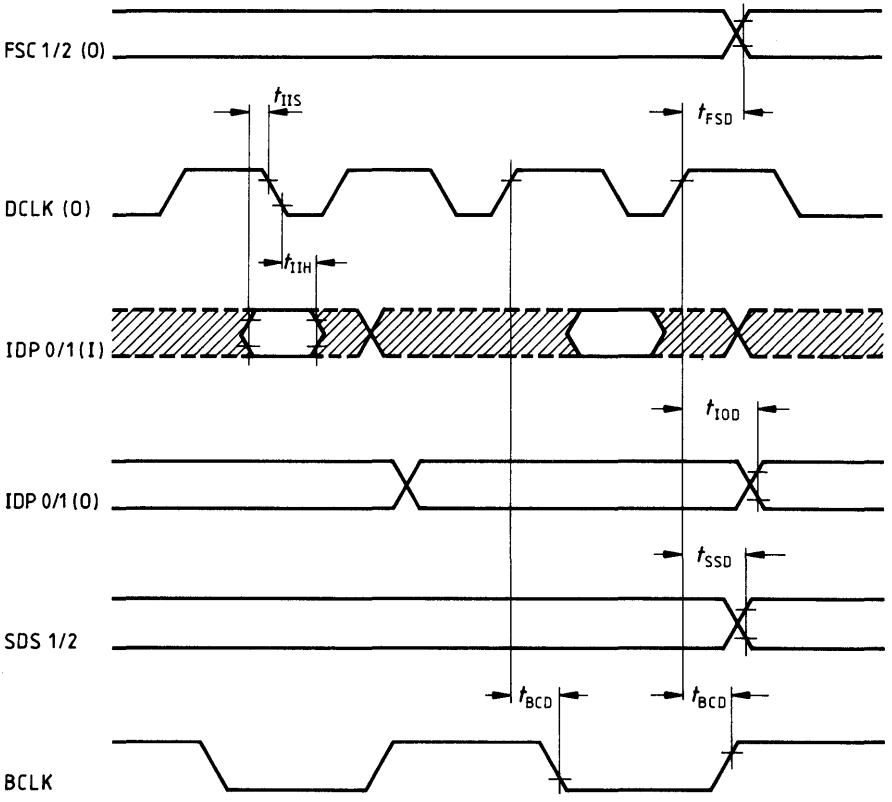


Switching Times

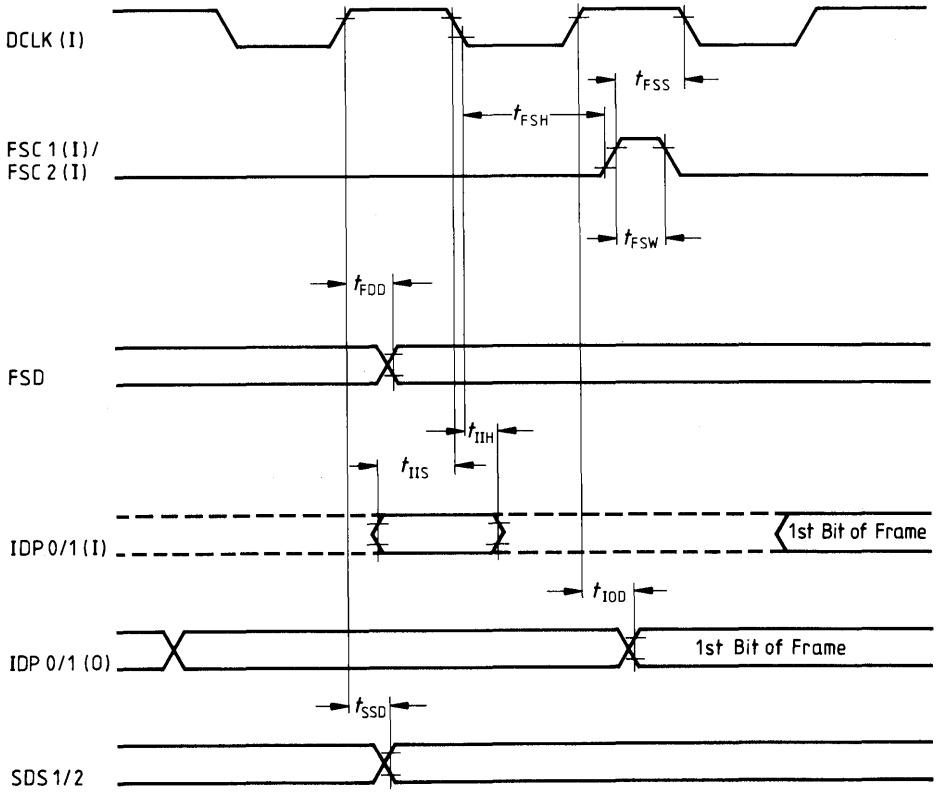
Parameter	Symbol	Limit Values		Unit
		min.	max.	
ALE pulse width	t_{AA}	50		ns
Address setup time to ALE	t_{AL}	20		ns
Address hold time from ALE	t_{LA}	10		ns
Address latch setup time to $\overline{WR}$, $\overline{RD}$	t_{ALS}	0		ns
Address setup time to $\overline{WR}$, $\overline{RD}$	t_{AS}	10		ns
Address hold time from $\overline{WR}$, $\overline{RD}$	t_{AH}	20		ns
ALE pulse delay	t_{AD}	15		ns
$\overline{DS}$ delay after R/$\overline{W}$ setup	t_{DSD}	0		ns
$\overline{RD}$ pulse width	t_{RR}	110		ns
Data output delay from $\overline{RD}$	t_{RD}		110	ns
Data float from $\overline{RD}$	t_{DF}		25	ns
$\overline{RD}$ control interval	t_{RI}	70		ns
$\overline{WR}$ pulse width	t_{WW}	60		ns
Data setup time to $\overline{WR}$ * $\overline{CS}$	t_{DW}	35		ns
Data hold time from $\overline{WR}$ * $\overline{CS}$	t_{WD}	10		ns
$\overline{WR}$ control interval	t_{WI}	70		ns

Serial Interface Timing
IOM Timing
IOM Mode

IOM Timing (TE Mode)



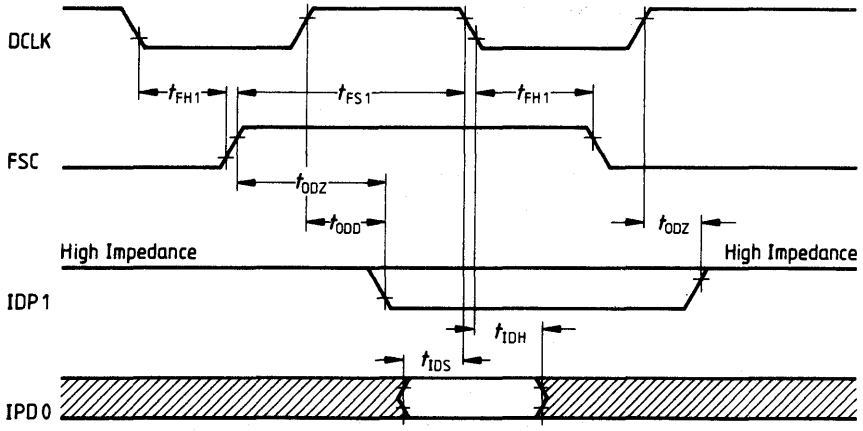
IOM Timing (LT-S, LT-T, NT Mode)



Parameter	Symbol	Limit Values min.	Limit Values max.	Unit	Test Conditions
IOM output data delay	t_{IOD}	20 20	140 100	ns ns	IOM-1 IOM-2
IOM input data setup	t_{IIS}	40 + t_{WH} 20		ns ns	IOM-1 IOM-2
IOM input data hold	t_{IIH}	20		ns	
FSC1/2 strobe delay	t_{FSD}	−20	20	ns	
Strobe signal delay	t_{SDD}		120	ns	
Bit clock delay	t_{BCD}	−20	20	ns	
Frame sync setup	t_{FSS}	50		ns	
Frame sync hold	t_{FSH}	30		ns	
Frame sync width	t_{FSW}	40		ns	
FSD delay	t_{FDD}	20	140	ns	

HDLC Mode

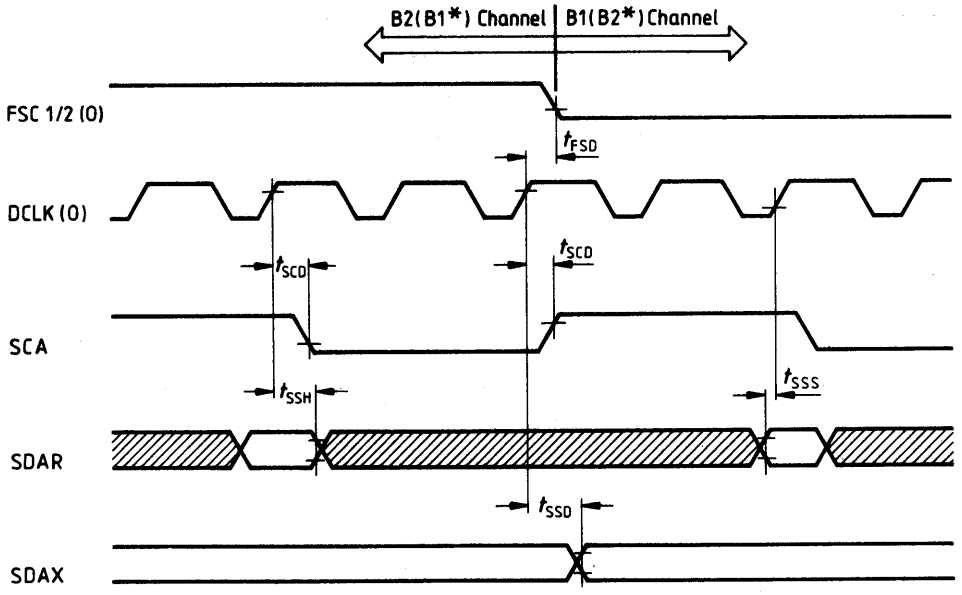
FSC1 (Strobe) Characteristics



Parameter	Symbol	Limit Values		Unit
		min.	max.	
FSC1 setup time	t_{FS1}	100		ns
FSC1 hold time	t_{FH1}	30		ns
Output data from high impedance to active	t_{OZD}		80	ns
Output data from active to high impedance	t_{ODZ}		40	ns
Output data delay from DCL	t_{ODD}	20	100	ns
Input data setup	t_{IDS}	10		ns
Input data hold	t_{IDH}	30		ns

Serial Port A (SSI) Timing

SSI Timing (TE, Timing Mode 0)



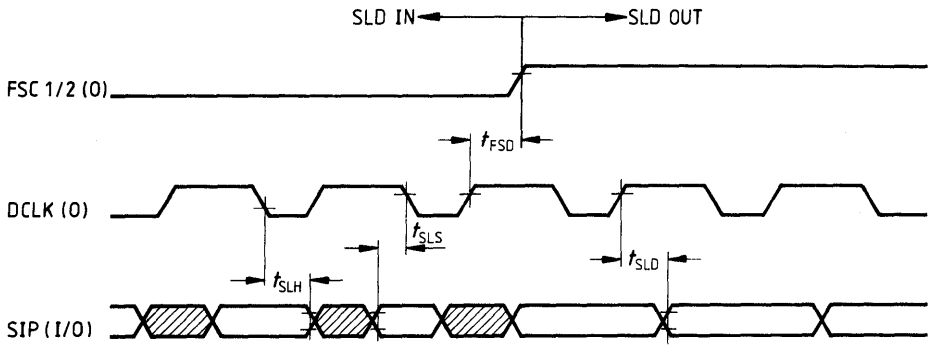
* Default polarity
Individual B channel switching to the B1- or B2 channel can be selected by programming the output polarity of FSC 1 and FSC 2 in the ADFR register

0: = Output

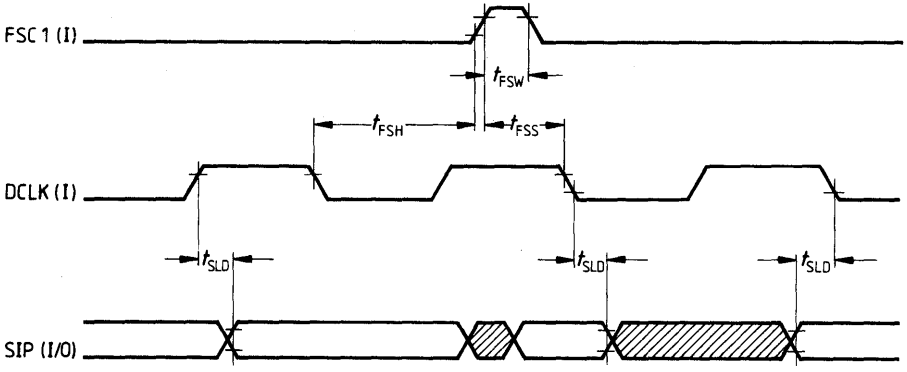
Parameter	Symbol	Limit Values		Unit
		min.	max.	
SCA clock delay	t_{SCD}	20	140	ns
SSI data delay	t_{SSD}	20	140	ns
SSI data setup	t_{SSS}	40		ns
SSI data hold	t_{SSH}	20		ns
FSC1/2 strobe delay	t_{FSD}	−20	20	ns

SLD Timing

SLD Timing (TE Mode)



SLD Timing (LT-S/LT-T Mode)



SLD Timing

Parameter	Symbol	Limit Values		Unit
		min.	max.	
SLD data delay	t_{SLD}	20	140	ns
SLD data setup	t_{SLS}	30		ns
SLD data hold	t_{SLH}	30		ns
FSC1/2 strobe delay	t_{FSD}	−20	20	ns
Frame sync setup	t_{FSS}	50		ns
Frame sync hold	t_{FSH}	30		ns
Frame sync width	t_{FSW}	40		ns

Clock Timing

The clocks in the different operating modes are summarized in **table 7-8,** with the respective duty ratios.

Table 7
ISAC-S Clock Signals (IOM-1 Mode)

Application	M2	M0	DCLK	FSC1/2	CP	X1
TE	0	0	o: 512 kHz* 2:1	o: 8 kHz* 1:1	o: 1536 kHz* 3:2	o: 3840 kHz 1:1
LT-S	1	0	i: 512 kHz	i: 8 kHz		o: 7680 kHz 1:1
LT-T	0	1	i: 512 kHz	i: 8 kHz	o: 512 kHz* 2:1	
NT	1	1	i: 512 kHz	i: 8 kHz		

* synchronized to S i: input o: output

Table 8
ISAC-S Clock Signals (IOM-2 Mode)

Application	M1	M0	DCLK	FSC1	CP/BCLK	X1	SDS1/2
TE	0	0	o: 1536 kHz* 3:2	o: 8 kHz* 1:1	o: 768 kHz* 1:1	o: 3840 kHz 1:1	o: 8 kHz 1:11 2:10
LT-S	1	0	i: 4096 kHz	i: 8 kHz		o: 7680 kHz 1:1	o: 8 kHz 1:11 2:10
LT-T	0	1	i: 4096 kHz	i: 8 kHz	o: 512 kHz* 2:1		o: 8 kHz 1:11 2:10
NT	1	1	i: 512 kHz	i: 8 kHz			o: 8 kHz 1:11 2:10

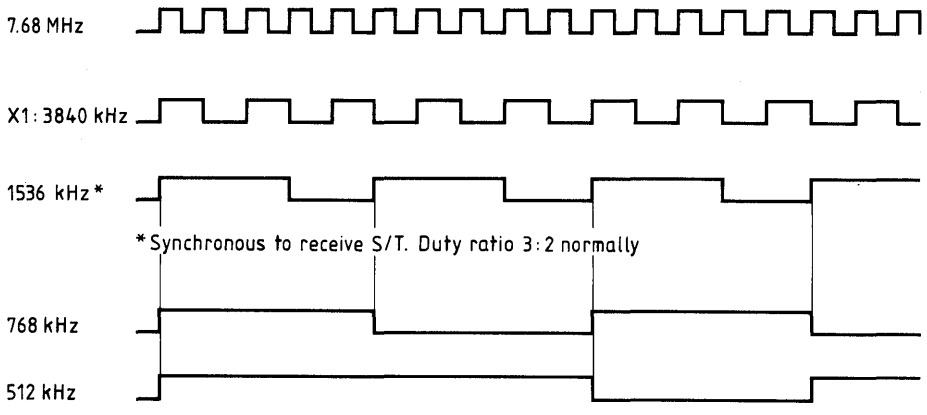
* synchronized to S i: input o: output

The 1536-kHz clock (TE mode) and the 512-kHz clock (LT-T mode) are phase-locked to the receive S signal, and derived using the internal DPLL and the 7.68 MHz ±100 ppm crystal.

A phase tracking with respect to "S" is performed once in 250 µs. As a consequence of this DPLL tracking, the "high" state of the 1536-kHz clock may be either reduced or extended by one 7.68-MHz period (duty ratio 2:2 or 4:2 instead of 3:2) once every 250 µs. Since the other signals are derived from this clock (TE mode), the "high" or "low" states may likewise be reduced or extended by the same amount once every 250 µs.

The phase relationships of the clocks are shown in

Figure 30



The timing relationship between the clocks are specified in **figure 31** and **table 9.**

Figure 31

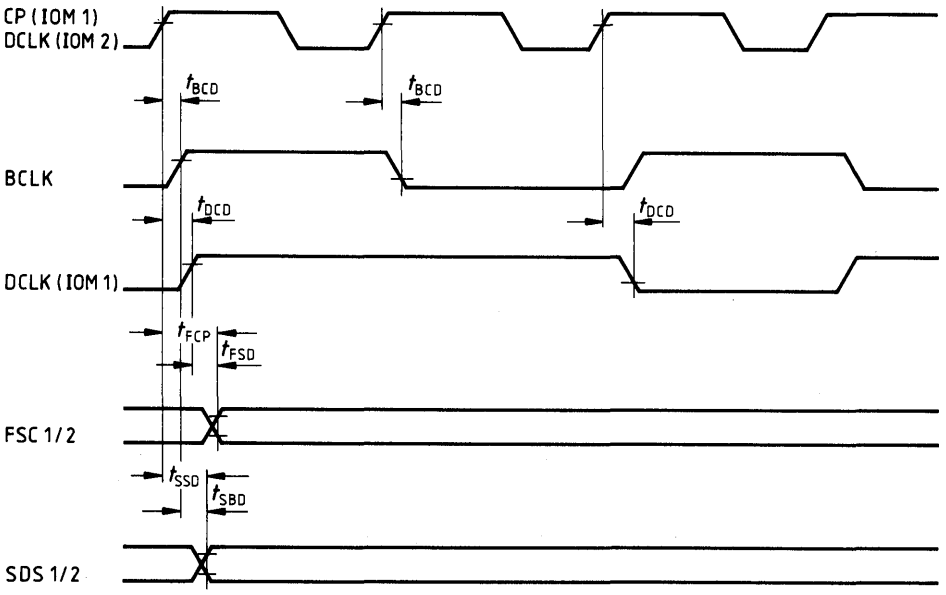


Table 9

Parameter	Symbol	Limit Values		Unit	Test Conditions
		min.	max.		
Bit clock delay	t_{BCD}	−20	20	ns	IOM-2
SDS1/2 delay from DCLK	t_{SDD}		120	ns	IOM-2
SDS1/2 delay drom BCLK	t_{SBD}		120	ns	IOM-2
DCLK delay from CP	t_{DCD}	0	50	ns	IOM-1
FSC1/2 delay from CP	t_{FCP}	0	50	ns	IOM-1
FSC1/2 delay from DCLK	t_{FSD}	−20	20	ns	IOM-1

Tables 10 to 15 gives the timing characteristics of the clock.

Definition of Clock Period and Width

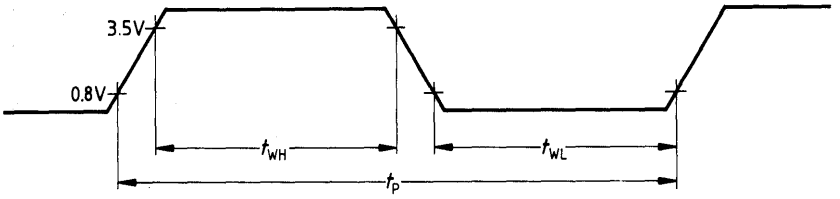


Table 10
DCLK Clock Characteristics (IOM-1)

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
(TE) 512 kHz	$t_{P\,O}$	1822	1953	2084	ns	OSC ± 100 ppm
(TE) 512 kHz 2:1	$t_{WH\,O}$	1121	1302	1483	ns	OSC ± 100 ppm
(TE) 512 kHz 2:1	$t_{WL\,O}$	470	651	832	ns	OSC ± 100 ppm
(NT, LT-S, LT-T)	$t_{P\,I}$	1853		2053	ns	
(NT, LT-S, LT-T)	$t_{WH\,I}$	200			ns	
(NT, LT-S, LT-T)	$t_{WL\,I}$	200			ns	

Table 11
DCLK Clock Characteristics (IOM-2)

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
(TE) 1536 kHz	$t_{P\,O}$	520	651	782	ns	OSC ± 100 ppm
	$t_{WH\,O}$	240	391	541	ns	OSC ± 100 ppm
	$t_{WL\,O}$	240	260	281	ns	OSC ± 100 ppm
(LT-S, LT-T)	$t_{P\,I}$	240	244		ns	
	$t_{WH\,I}$	100			ns	
	$t_{WL\,I}$	100			ns	

Note: For NT characteristics, see IOM-1 case.

Table 12
CP Clock Characteristics (IOM-1 TE Mode)

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
(TE) 1536 kHz	t_{PO}	520	651	782	ns	OSC ± 100 ppm
	t_{WHO}	240	391	541	ns	OSC ± 100 ppm
	t_{WLO}	240	260	281	ns	OSC ± 100 ppm
	t_R, t_F			20	ns	C_L = 100 pF
				10	ns	C_L = 50 pF

Table 13
CP Clock Characteristics (LT-T Mode)

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
(LT-T) 512 kHz	t_{PO}	1822	1953	2084	ns	OSC ± 100 ppm
	t_{WHO}	1121	1302	1483	ns	OSC ± 100 ppm
	t_{WLO}	470	651	832	ns	OSC ± 100 ppm
	t_R, t_F			20	ns	C_L = 100 pF
				10	ns	C_L = 50 pF

Table 14
X1 Clock Characteristics (TE Mode)

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
(TE) 3840 kHz	t_{PO}	−100	260	100	ns	OSC ± 100 ppm
	t_{WHO}	120	130	140	ns	OSC ± 100 ppm
	t_{WLO}	120	130	140	ns	OSC ± 100 ppm

Table 15

X1 Clock Characteristics (LT-S Mode)

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
(LT-S) 7680 kHz	$t_{P\,O}$	−100	130.21	100	ns	OSC ± 100 ppm
	$t_{WH\,O}$		65		ns	OSC ± 100 ppm
	$t_{WL\,O}$		65		ns	OSC ± 100 ppm

Jitter

In TE mode, the timing extraction jitter of the ISAC-S conforms to CCITT Recommendation I.430 (−7% to +7% of the S interface bit period).

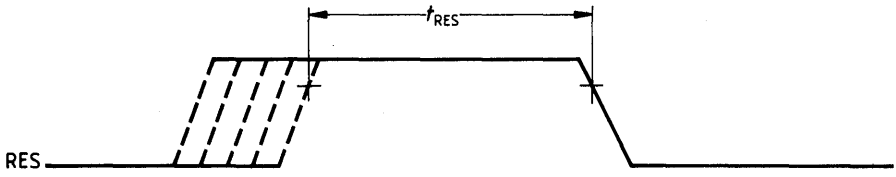
In the NT and LT-S applications, the clock input DCLK is used as reference clock to provide the 192-kHz clock for the S line interface. In the case of a plesiochronous 7.68-MHz clock generated by an oscillator, the clock DCLK should have a jitter less than 100 ns peak-to-peak. (In the case of a zero input jitter on DCLK, ISAC-S generates at most 130 ns "self-jitter" on S interface.)

In the case of a synchronous*) 7.68-MHz clock (input XTAL1), the ISAC-S transfers the input jitter of XTAL1, DCLK and FSC1 to the S interface. The maximum jitter of the NT/LT-S output is limited to 260 ns peak-to-peak (CCITT I.430).

* fixed divider ratio between XTAL1 and DCLK

Reset

Reset Signal Characteristics



Parameter	Symbol	Limit Values min.	Unit	Test Conditions
Length of active high state (Input)	t_{DCLK}	4	ms	Power On/Power Down to Power Up (Standby)
		2* DCLK clock cycles		During Power Up (Standby)

SIEMENS

Audio Ringing Codec Filter (ARCOFI)

PSB 2160

Preliminary Data

CMOS IC

Type	Ordering Code	Package
PSB 2160-N	Q67100-H6031	PL-CC-28 (SMD
PSB 2160-P	Q67100-H8503	P-DIP-24

The PSB 2160 ARCOFI® provides the subscriber with an optimized Audio, Ringing, Codec, Filter processor solution for a digital telephone. The ARCOFI fulfils all necessary requirements for the completion of a low cost digital telephone. Full featured applications including hands-free telephony are carried out by the addition of a voice switched speakerphone circuit. The ARCOFI performs all coding, decoding and filtering functions according to CCITT and AT&T norms.

The ARCOFI integrates a DTMF generator in the transmit direction and a tone generator plus a ringing generator in the receive path. The interfacing to a handset mouth and earpiece is facilitated by a flexible analog front end. A loudspeaker output has also been integrated on chip as well as a secondary input for a handsfree microphone. The microphone analog gains is user programmable under microprocessor control.

Features

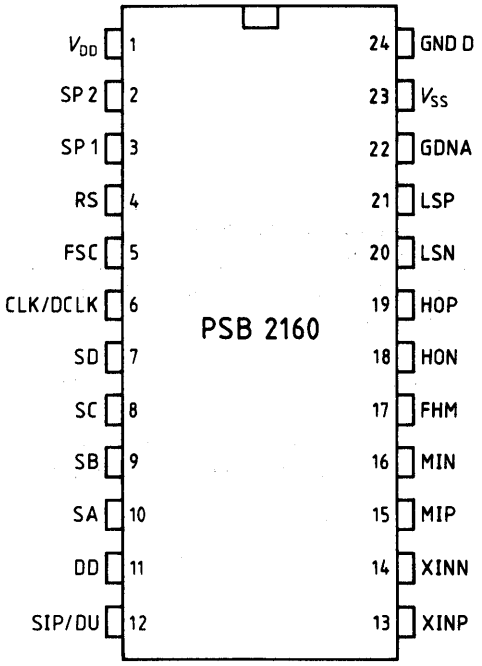
- Audio, ringing, codec, filter for digital telephone
- Programmable codec filter
- Programmable DTMF, tone and ringing generators
- Programmable A- and μ-law
- Test and maintenance loopbacks in the analog front end and the digital processor
- SLD or IOM®-2 serial interface bus
- Flexible Peripheral Control Interface (PCI)
- Separate output for piezo ringer
- Dual analog inputs for handset and "hands-free" microphones plus an auxiliary differential analog input
- Two sets of differential outputs for a handset earpiece and a loudspeaker
- Low power CMOS technology
- Power dissipation: active 150 mW, standby 10 mW
- Temperature range: −25 to 70 °C

Applications

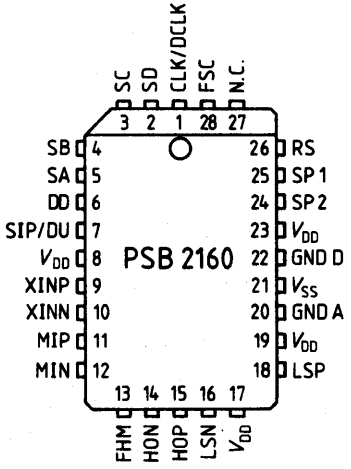
Digital terminal equipment including a voice path.

Pin Configurations
(top view)

P-DIP-24



PL-CC-28



Pin Definitions and Functions

Pin No. P-DIP	Pin No. PL-CC	Symbol	Function
1	8,17,19,23	V_{DD}	+5 V; Positive power supply
2 3	24 25	SP2 SP1	**Supplementary Function:** Appropriate pin strapping access supplementary functions including test modes.
4	26	RS	**Reset Input:** When pin RESET is forced high the ARCOFI is placed in a power down mode. All configuration registers are reset to default values. I/O pins SA-SD and SIP/DU are programmed as inputs until the ARCOFI is reconfigured.
5	28	FSC	**Frame Sync:** 8-kHz signal, phase lockes to CLK. When high, SIP behaves as an input and the ARCOFI can receive data through pin SIP. When low, SIP behaves as an output and data can be transferred from the ARCOFI to the system via pin SIP. When in IOM-2 mode FSC supplies to the ARCOFI a synchronization signal according to the IOM-2 specification.
6	1	CLK/DCLK	**CLK System Clock:** 512 kHz supplied by the application system clock when SLD mode is selected. **DCLK System Clock:** 1.536 MHz supplied by the application system clock when IOM-2 mode is selected.
7 8 9 10	2 3 4 5	SD SC SB SA	**Programmable I/O PCI Pins:** With the appropriate bit setting in configuration register CR2, each SA-SD pin can be declared independently as input or as output. The data are received from or forwarded to the signaling channel according to the programming of the PCI pins. When selected, the tone generator signals can be directed to pins SA & SB. (SA & SB then in opposite phase).
11	6	DD	**DD; Data Downstream:** Receive data from a layer-1 controlling device when IOM-2 made is selected.
12	7	SIP/DU	**SIP; Serial Interface Port:** This serial bidirectional port is clocked by CLK when SLD mode is selected. **DU; Data Upstream:** Transmit data to the layer-1 controlling device when IOM-2 made is selected.
13 14	9 10	XINP XINN	**X Input:** These auxiliary inputs provide a normalized differential audio input for an additional analog device.
15 16	11 12	MIP MIN	**Hand-set Microphone Inputs:** MIP & MIN provides highly symmetrical differential inputs for commonly used telephone microphones.

Pin Definitions and Functions (cont'd)

Pin No. P-DIP	Pin No. PL-CC	Symbol	Function
17	13	FHM	**Hands-Free Microphone:** This single ended input can be used to interface an electret microphone for speakerphone applications.
18 19	14 15	HON HOP	**Hand-set Earpiece Outputs:** HOP & HON are differential output pins which can drive handset earpiece transducers directly.
20 21	16 18	LSN LSP	**Loudspeaker Outputs:** LSN and LSP are differential output pins which can drive a 50 Ω loudspeaker directly. A piezo transducer connected via SA and SB can also be used for ringing signals instead of a loudspeaker.
22	20	GNDA	**Analog Ground:** Not internally connected to GNDD. All analog signals are referred to this pin.
23	21	V_{SS}	−5 V; Negative power supply
24	22	GNDD	**Digital Ground:** (0 V) not internally connected to GNDA. All digital signals are referred to this pin.

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
V_{DD} referred to GNDA	V_S	−0.3	5.5	V
V_{SS} referred to GNDA	V_S	−5.5	0.3	V
GNDA to GNDD	V_S	−0.3	0.3	V
Analog input and output voltages referred to V_{DD} referred to V_{SS}	 V_S V_S	 −10.3 −0.3	 0.3 10.3	 V V
All digital input and output voltages referred to GNDD referred to V_{DD}	V_S	 −0.3 −5.3	 5.3 0.3	 V V
Power dissipation	P_D		1	W
Storage temperature	T_{stg}	−60	125	°C
Ambient temperature under bias	T_A	−30	80	°C

DC Characteristics

$V_{DD} = 5\ V \pm 5\%$, $V_{SS} = -5\ V \pm 5\%$, GNDD = 0 V, $T_A = -25$ to 70 °C

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
DIGITAL Input leakage current	I_{IL}			±1	µA	$-0.3 <= V_{IH} <= V_{DD}$
H-input level	V_{IH}	2.4		V_{DD}+0.3	V	
L-input level	V_{IL}	−0.3		0.8	V	
H-output level	V_{OH}	2.4			V	$I_O = 400\ \mu A$
L-output level	V_{OL}			0.45	V	$I_O = -2$ mA
V_{DD} supply current standby standby operating*)	I_{DD}		 11	 2 TBD 15	 mA mA mA	 $V_{SS} = 0$ V $V_{DD} = 5.25$ V ±5% supply ±5% supply
V_{SS} supply current standby operating*)	I_{SS}		 −8	 TBD −13	 mA mA	 ±5% supply ±5% supply
Standby power dissipation	P_{DO}			TBD	mW	±5% supply
Standby power dissipation	P_{DO}			10	mW	V_{SS}=0V, V_{DD}=5.25V Clock = 512 kHz
Standby power dissipation	P_{DO}			5	mW	V_{SS}=0V; V_{DD}=5.25V No clock
Operating power dissipation*)	P_{D1}		100	150	mW	±5% supply
Input capacitance	C_I			10	pF	
Output capacitance	C_O			15	pF	

TBD: To Be Determined

*) Operating power dissipation is measured with all analog outputs open.

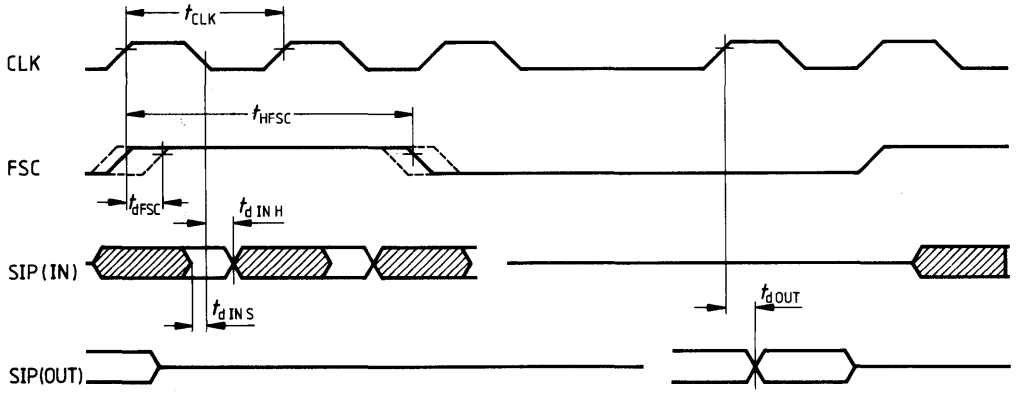
DC Characteristics (cont'd)

SLD Bus Switching Characteristics

Parameter	Symbol	Limit Values			Unit
		min.	typ.	max.	
CLK period	t_{CLK}	1.76	1.953	2.15	µs
CLK duty cycle	$t_{d\ CLK}$	30	50	70	%
FSC Period	t_{FSC}		125		µs
FSC delay time	$t_{d\ FSC}$	−20		80	ns
FSC high time	$t_{H\ FSC}$	0.5	62.5		µs
SIP data in setup time	$t_{d\ IN\ S}$	50			ns
SIP data in hold time	$t_{d\ IN\ H}$	80			ns
SIP data out delay	$t_{d\ OUT}$			200	ns
SIP data out tristate delay				50	ns

Note: SIP is an I/O pin; SIP IN denotes timings for incoming data and SIP OUT denotes timings relation with outgoing data.

SLD Bus Timing Diagram



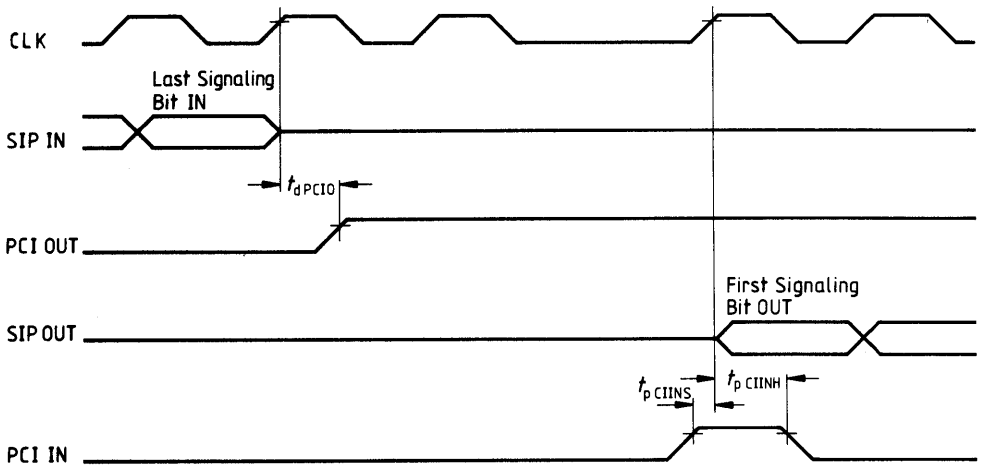
PCI Switching Characteristics

Parameter	Symbol	Limit Values		Unit
		min.	max.	
SIP IN to PCI OUT	$t_{d\,PCIO}$		300	ns
PCI IN setup time	t_{pCIINS}	50		ns
PCI IN hold time	t_{pCIINH}	100		ns

Reset Timing

Parameter	Symbol	Limit Values		Unit
		min.	max.	
V_{DD} rise time	t_{RVDD}	0	20	ms
Reset pulse width	t_{RS}	1		µs
Power stable to reset low	t_{SRS}	1		µs
Reset transition time	t_{tr}		1	ms

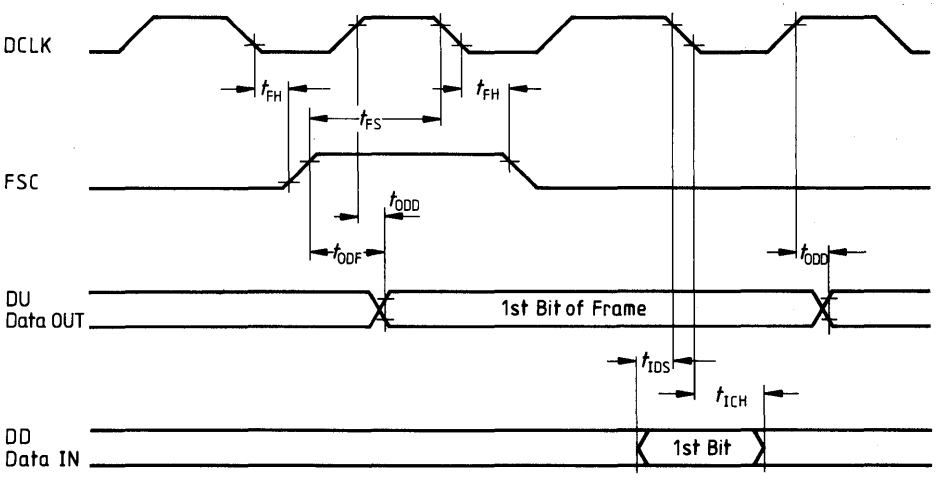
PCI Timing Diagram



IOM Bus Switching Characteristics

Parameter	Symbol	Limit Values		Unit
		min.	max.	
FSC setup time	t_{FS}	60		ns
FSC hold time	t_{FH}	30		ns
Output data delay from DCLK	t_{ODD}		60	ns
Input data set-up time	t_{IDS}	25		ns
Input data hold	t_{IDH}	20		ns
Output data delay from FSC	t_{ODF}	30		ns

IOM-2 Bus Timing Diagram



Analog Front End Electrical Interface Inputs

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit	Test Conditions
Hand-set microphone input impedance	Z_{HM}	150		kΩ	300-3400 Hz
Hand-set microphone max. input voltage swing*	V_{HM}		7.58	mVpk	
Hand-set microphone amplifier gain AHM + HR	G_{AHM+AR}	16	52.0	dB	pin MIP, MIN 386 mV 1 kHz
Hands-free microphone input impedance	Z_{FHM}	150		kΩ	300-3400 Hz
Hands-free microphone max. input voltage swing*	V_{FHM}		127	mVpk	
Hands-free microphone amplifier gain	G_{AFHM}		28.0	dB	pin FHM 19.5 mV 1 kHz
Auxiliary pin input impedance	Z_{XIN}	150		kΩ	300-3400 Hz
Auxiliary XIN max. input voltage swing*	V_{XIN}		563	mVpk	
Auxiliary XIN amplifier gain AX + AR	G_{AXIN}		15.1	dB	pin XINN & XINP 270 mV 1 kHz

* A maximum swing signal corresponds to a 3.14 dBm0 signal at the A/D converter. This corresponds also to a PCM code overload ±127. (3.14 dBm0 = 2.26 V_{rms} = 3.2 V_p = 6.4 V_{pp}).

Analog Front End Electrical Interface Outputs

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit	Test Conditions
Hand-set earpiece output impedance	Z_{HO}		1	Ω	300-3400 Hz
Hand-set earpiece max. output voltage swing*	V_{HO}		457	mVpk	load measured from HOP to HON
Hand-set earpiece output high voltage*	V_{HOH}		455	mVpk	input load −1 mA HOP/HOP
Hand-set earpiece output low voltage*	V_{HOL}		455	mVpk	input load +1 mA HOP/HOP
Loudspeaker output impedance	Z_{LS}		2	Ω	300-3400 Hz
Loudspeaker max. output voltage swing*	V_{LS}		2.75	Vpk	load measured from LSN to LSP
Loudspeaker output high voltage*	V_{LSOH}		2.55	V	input load −100 mA LSN/LSP
Loudspeaker output low voltage*	V_{LSOL}		2.55	V	input load +100 mA LSN/LSP

* The max. output voltage swing corresponds to a max. incoming PCM code (±127).

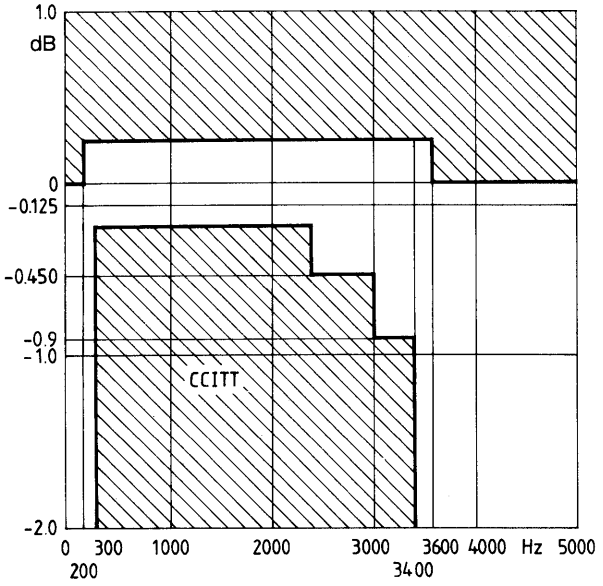
Analog Front End Attenuation Plan

Transmit	min.	typ.	0 dBmO	max.	peak	Unit	Ref.
MIP/MIN	2.15E-04	1.21E-03	5.60E-03	6.81E-03	8.04E-03	Vpk	V
Microphone	1.52E-04	8.56E-04	3.96E-03	4.82E-03	5.68E-03	Vrms	V
Input level at	−80.3	−65.3	−52	−50.3	−48.86	dBmO	1.576V
Max gain	−74.13	−59.13	−45.83	−44.13	−42.69	dBm	0.775V
AHM+AR = 52 dB[1])	52	52	52	52	52	dB	gain
Xin	1.51E-02	8.48E-02	3.92E-01	4.77E-01	5.63E-01	Vpk	V
Input level	1.07E-02	5.99E-02	2.77E-01	3.37E-01	3.98E-01	Vrms	V
	−43.4	−28.4	−15.1	−13.4	−11.96	dBmO	1.576V
	−37.23	−22.23	−8.93	−7.23	−5.79	dBm	0.775V
AX−AR gain[1])	15.1	15.1	15.1	15.1	15.1	dB	gain
FHM	3.41E-03	1.92E-02	8.87E-02	1.08E-01	1.27E-01	Vpk	V
Input level	2.41E-03	1.36E-02	6.28E-02	7.63E-02	9.01E-02	Vrms	V
	−56.3	−41.3	−28	−26.3	−24.86	dBmO	1.576V
	−50.13	−35.13	−21.83	−20.13	−18.69	dBm	0.775V
AFHM gain[1])	28	28	28	28	28	dB	gain
A/D	8.57E-02	4.82E-01	2.23E+00	2.71E+00	3.20E+00	Vpk	V
Input level	6.06E-02	3.41E-01	1.58E+00	1.92E+00	2.26E+00	Vrms	V
ARCOFI	−28.3	−13.3	0	1.7	3.14	dBmO	1.576V
(Bypass mode)	−22.13	−7.13	6.17	7.87	9.31	dBm	0.775V
PCM value	±43	±83	±118	±123	±127	PCM word	

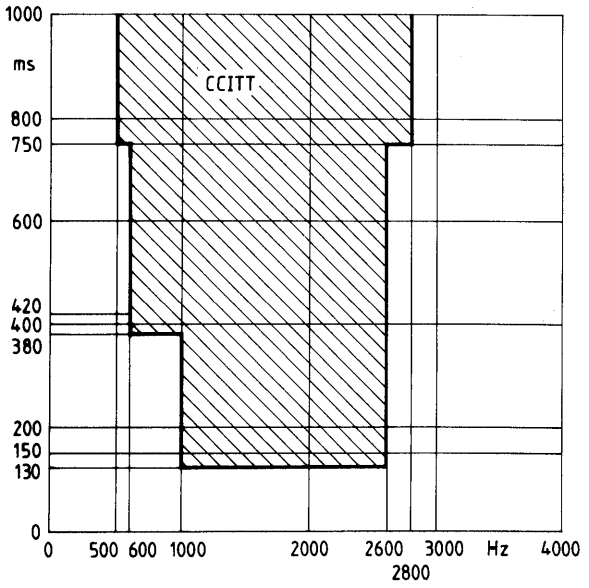
Receive	min.	typ.	0 dBmO	max.	Peak	Unit	Ref.
LSN/LSP	8.57E-02	4.82E-01	2.23E+00	2.71E+00	3.20E+00	Vpk	V
Output level	6.06E-02	3.41E-01	1.58E+00	1.92E+00	2.26E+00	Vrms	V
Symmetric in	−28.3	−13.3	0	1.7	3.14	dBmO	1.576V
a 50 Ω load	−22.13	−7.13	6.17	7.87	9.31	dBm	0.775V
ALS gain	0	0	0	0	0	dB	attenuat.
HOP/HON[1])	6.81E-02	3.83E-01	1.77E+00	2.15E+00	2.54E+00	Vpk	V
Output level	4.82E-02	2.71E-01	1.25E+00	1.52E+00	1.80E+00	Vrms	V
Symmetric in	−30.3	−15.3	−2	−0.3	1.14	dBmO	1.576V
a 200 Ω load	−24.13	−9.13	4.17	5.87	7.31	dBm	0.775V
AHO attenuation	2	2	2	2	2	dB	attenuat.
D/A	8.57E-02	4.82E-01	2.23E+00	2.71E+00	3.20E+00	Vpk	V
Output level	6.06E-02	3.41E-01	1.58E+00	1.92E+00	2.26E+00	Vrms	V
ARCOFI	−28.3	−13.3	0	1.7	3.14	dBmO	1.576V
(Bypass mode)	−22.13	−7.13	6.17	7.87	9.31	dBm	0.775V

[1]) The HOP/HON attenuation values can be changed in future versions of ARCOFI.

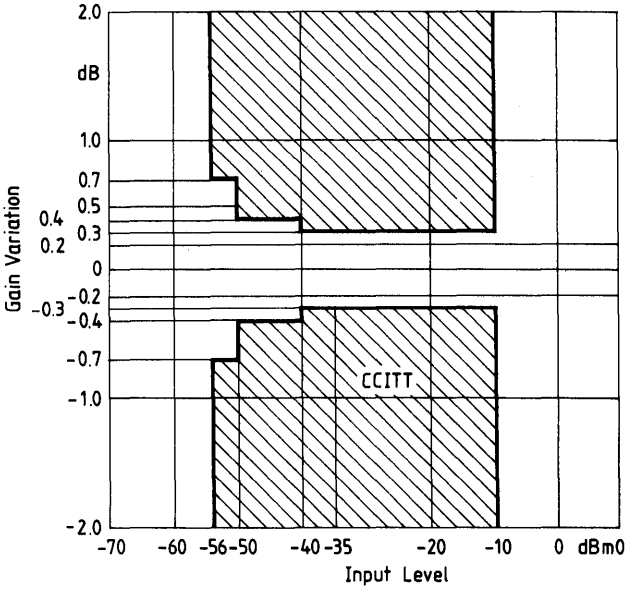
Attenuation Distortion in Transmit & Receive Direction



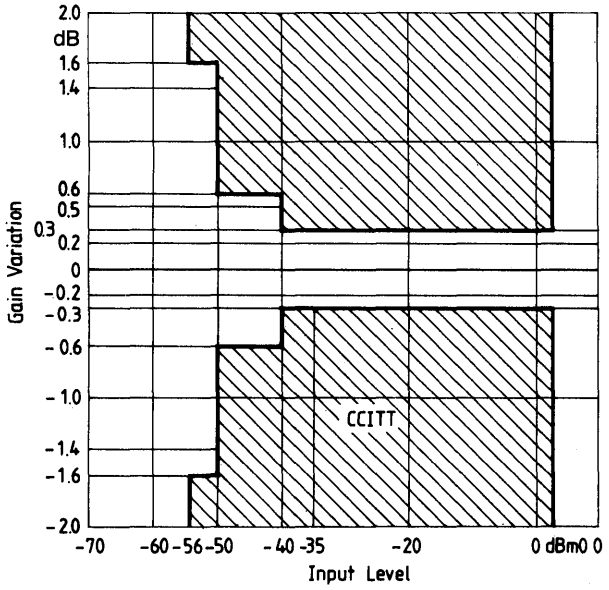
Group Delay Distortion in Transmit & Receive Direction (ref. 1500 Hz)



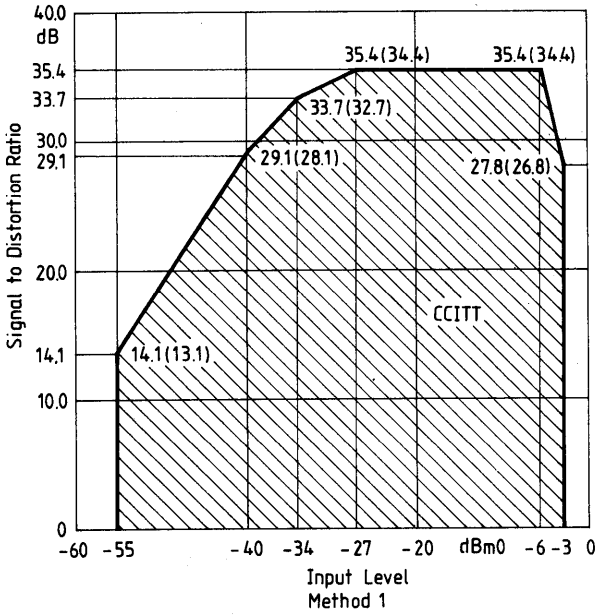
Gain Tracking in Transmit & Receive Direction (Method 1; Noise)



Gain Tracking in Transmit & Receive Direction (Method 2; Sinus)

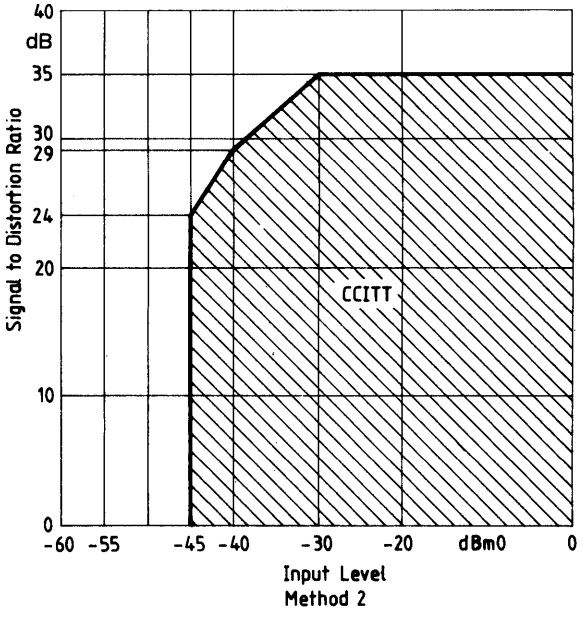


Total Harmonic Distortion in Receive and Transmit *) Direction (Method 1; Noise)



*) Remark: Between brackets, values for transmit direction

Total Harmonic Distortion in Receive and Transmit Direction (Method 2; Sinus)



Out-of-Band Signals at Analog Inputs

When applying an out-of-band sine-wave signal with frequency *f* and level *A* to the analog inputs, the level of any frequency component below 4 kHz at the digital output is attenuated according to the following table.

The reference level used for this measurement is a 800 Hz, 0dBmO signal applied to the FHM analog input in by-pass mode. The digital gain GX in configuration register CR1 has to be set to a flat 0dB.

Out-of-Band Input Frequency *f*	**Out-of-Band Input Level *A***	**Attenuation at Digital Output**
0 Hz <= *f* <= 60 Hz	−45 dBmO <= *A* <= 0 dBmO	25 dB
60 Hz <= *f* <= 100 Hz	−45 dBmO <= *A* <= 0 dBmO	10 dB
3400 Hz <= *f* <= 4000 Hz	−45 dBmO <= *A* <= 0 dBmO	0 dB
4000 Hz <= *f* <= 4600 Hz	−45 dBmO <= *A* <= 0 dBmO	14 dB
4600 Hz <= *f* <= 12 kHz	−45 dBmO <= *A* <= −15.8 dBmO	35 dB
12 kHz <= *f* <= 20 kHz	−45 dBmO <= *A* <= −23.2 dBmO	35 dB
20 kHz <= *f*	−45 dBmO <= *A* <= −25 dBmO	35 dB

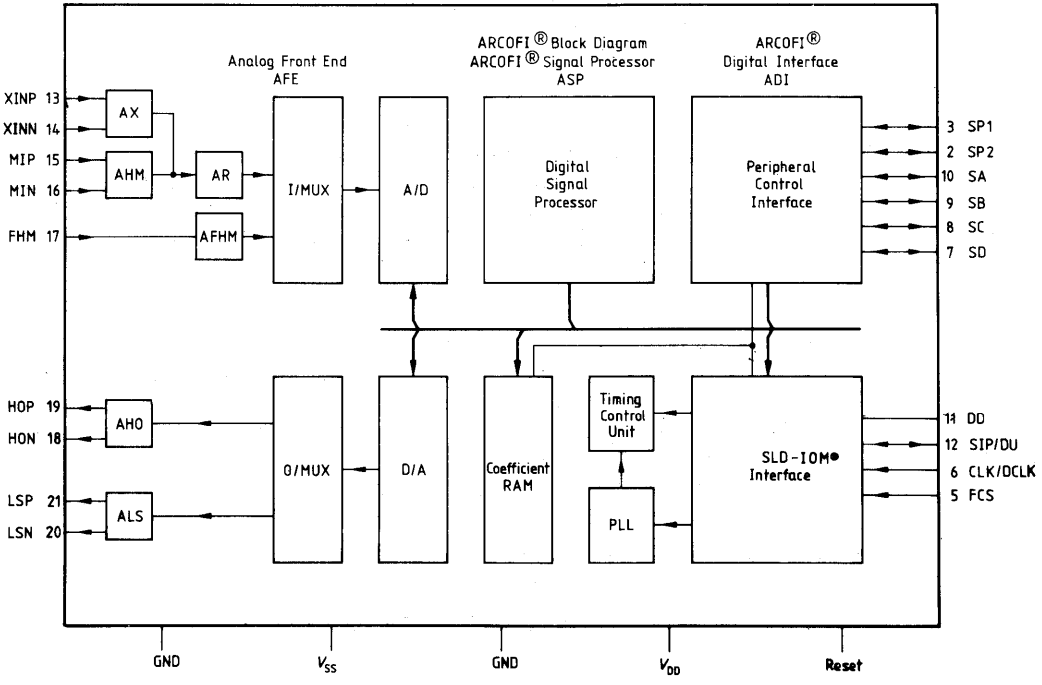
Functional Description

The ARCOFI bridges the gap between the audio world of microphones, earphones, loudspeakers and the PCM digital world by providing a full PCM CODEC (coder + decoder) with all the necessary transmit and receive filters. A block diagram of the ARCOFI is shown in **figure 1.**

The ARCOFI can be subdivided in three main blocks;

- The ARCOFI Analog Front End (AFE)
- The ARCOFI Signal Processor (ASP)
- The ARCOFI Digital Interface (ADI)

Figure 1
Block Diagram



Analog Front End

The **Analog Front End** section of the ARCOFI interfaces the analog transducers with the subsequent signal processor. In the transmit direction the AFE function is to amplify the transducer input signals (microphones) and convert them into digital signals. In the AFE receive section, the incoming digital signals are converted to analog signals output to an earpiece and a loudspeaker. The attenuation plan and electrical characteristics of the AFE are adapted to meet commonly used voice transducers.

Analog Inputs

A high sensitive differential input MIP and MIN connects a handset microphone to a gain programmable amplifier AHM. When selected, the differential X inputs can be activated (amplifier AX) while deselecting the MIP/MIN inputs;

Coming from AHM or AX the signal is forwarded via a fixed amplification stage AR to the input of the analog multiplexer driving the oversampling A/D converter. A third analog input source is provided through pin FHM. This "hands-free" microphone input connects the multiplexer via amplifier AFHM. The programmable amplifier AHM provides a first gain adjustment allowing a perfect adaptation to various types of microphone transducers. This gain adjustment is then tuned in the digital domain via the programmable gain adjustment filter GX (see ARCOFI signal processing section).

Analog Outputs

Fully differential outputs HOP and HON connect the amplifier AHO to the hand-set earpiece. Differential outputs LSN & LSP are provided for use with a 50 Ω loudspeaker. Up to 100 mW of power can be delivered to the loudspeaker via amplifier ALS. The power amplifier ALS is short-circuit protected. All outputs are sourced by a digital-to-analog converter via an output analog multiplexer. The selection of the output source is performed through the configuration register CR3 via the SLD interface.

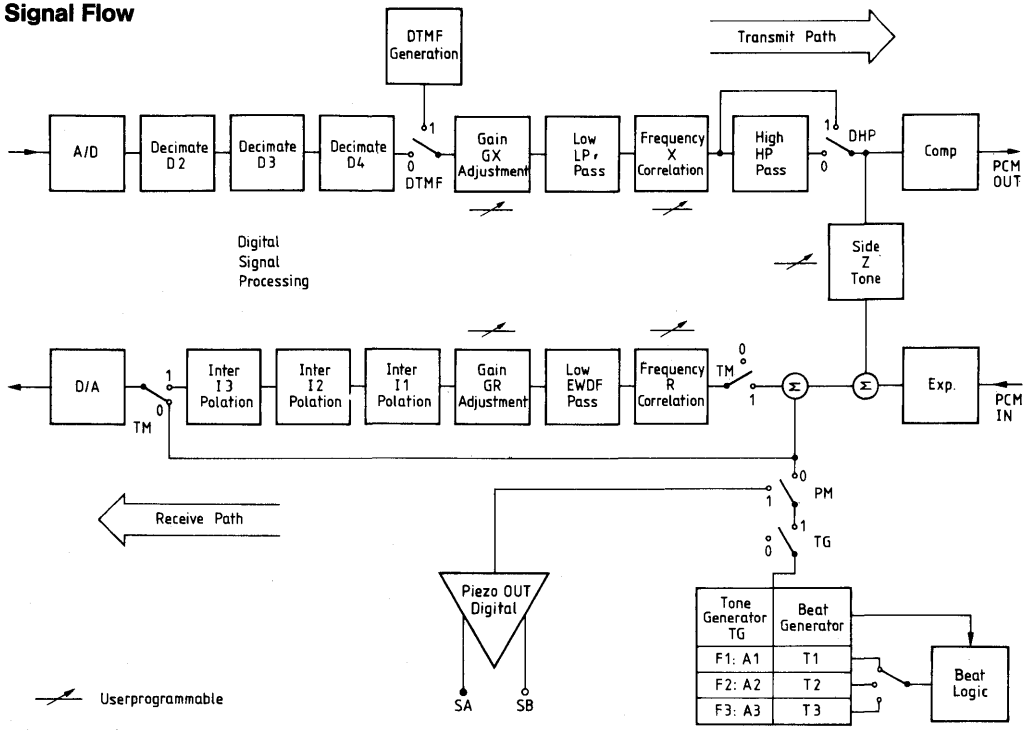
ARCOFI Signal Processor (ASP)

The **ARCOFI Signal Processor** (ASP) has been conceived to perform all CCITT recommended filtering in both the transmit and receive path and is therefore fully compatible to the G.714 CCITT specification. The code processed by the ASP is provided in the transmit direction by an oversampling A/D converter situated in the analog front end (AFE). Once processed the speech signal is converted into an 8 bit A-law or μ-law PCM format or remains a 16-bit linear word according to the bit setting in the configuration register 3.

In the receive direction the incoming PCM-signal is expanded in a linear format and subsequently processed until passed to the D/A converter.

The entire ARCOFI signal flow plan is shown in **figure 2.**

Figure 2
Signal Flow



Transmit Path Signal Processing

In the transmit direction a series of decimation filters reduces the sampling rate down to the 8-kHz PCM rate. These filters attenuate out-of-band noise by limiting the received signal to the voiceband.

The decimation stages end with a low-pass filter which band limits the voice signal according to the CCITT recommendation G.714. A high-pass filter is also provided to remove power line frequencies. The ARCOFI meets or exceeds all CCITT, and North American recommendation on attenuation distortion and group delay distortion.

The GX gain adjustment stage is digitally programmable allowing the gain to be programmed from −45 to +12 dB within a ±0.25 dB tolerance range. However the CCITT templates are not guaranteed in the whole area.

The voice signal after being linearly processed can be output as an 8-bit PCM word according to the CCITT G.711 A-Law or the North American μ-Law format. If desired the compression stage can be by-passed, a 16-bit linear word is then outputed to the ARCOFI digital interface.

The transmit path contains a frequency correction filter FX allowing an optimum adaptation to different type of microphones (dynamic, piezoelectric or electret).

Receive Path Signal Processing

In the receive path the incoming PCM signal is expanded into a linear code according to the selected A or μ-Law. If the linear mode is chosen, the PCM expander circuit is by-passed and a 16-bit linear word has to be provided to the processor.

A programmable sidetone gain stage Z adds a sidetone signal to the incoming voice signal. The sidetone gain can be programmed from −50 to −2.5 dB within a ±1 dB tolerance range (0 dB is also possible).

The FR frequency correction filter is similar to the FX filter allowing an optimum adaptation to different type of loudspeakers and earpieces.

A low-pass EWDF filter limits the signal bandwidth in the receive direction according to CCITT recommendations. The GR gain adjustment stage is digitally programmable from −45 dB to +12 dB within a 0.25 dB tolerance range. However the CCITT templates are not guaranteed in the whole area.

A series of low-pass interpolation filters increase the sampling frequency up to 128 kHz. The last interpolator feeds the D/A converter.

Tone Ring and Tone Generator

The ASP receive path contains two signal generators; a tone ring and a beat tone generator (TG & BT). Those generators can be used for tone alerting; call progress tones or other audible feedback tones. All generated tones can be provided at either the handset earpiece, the loudspeaker output or the piezo ringer output (SA & SB).

Distinctive alerting signals allowing for example the use of different multitone ringing patterns, are all programmable using the beat tone generator in conjucntion with the tone ringer. In the case of a two or three tone ringing signal, the tone ring generator controls the output frequency pitch whilst the beat tone generator controls the repetition rate.

ARCOFI Digital Interface (ADI)

The ADI features are:

- A selectable SLD or IOM-2 serial bus interface through which the ARCOFI transfers voice channels and communicates with the system microcontroller.
- A programmable multipurpose interface PCI (Peripheral Control Interface) which provides 4 programmable I/O pins to control peripheral devices.

SLD Bus

The SLD serial interface consists of a bidirectional data line SIP, a synchronization clock input CLK and a data direction input FSC. Data bits are loaded or read out of the serial interface pin SIP under control of a direction signal FSC. Bits are clocked in or clocked out on the rising edge of the slave clock pin CLK (512 kHz). FSC and CLK inputs must be phase locked.

An SLD frame lasts 125 µs and consists of 32 bits transferred to the ARCOFI (FSC high) followed by 32 bits transferred from the ARCOFI to the SLD bus (FSC low).

The SLD interface thus provides a full duplex 256 kbit/s communication capacity. This capacity is subdivided in two 64 kbit/s voice/data channels reserved for the ISDN B1 and B2 channels. The remaining bandwidth is used by a feature control channel (64 kbit/s) and a signaling channel (64 kbit/s). Bytes in all channels are serialized MSB first.

A command received over the SLD-bus can cause a response over the SLD-bus within the same frame. This leaves the ARCOFI 31.25 µs to interpret the command and generate the appropriate answer in the following SLD half-frame.

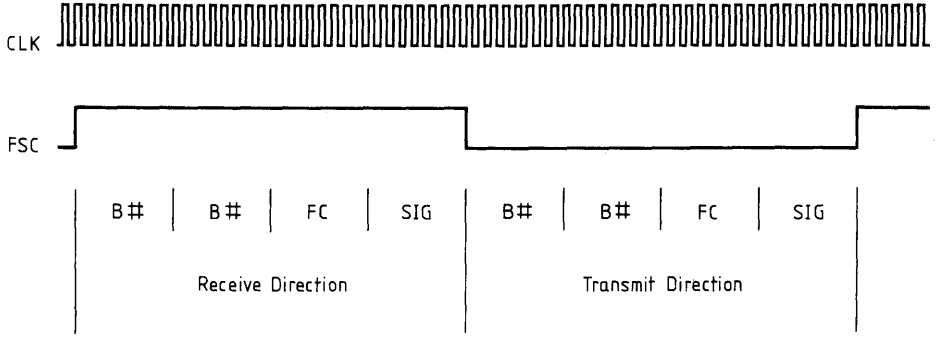
All ARCOFI internal registers are accessible via the SLD-bus in the time slot allocated to the command channel. The first byte transferred in the command channel specifies the type of operation and the number of bytes allocated to the transfer set-up.

When in power down (PU=0 ;CMDR), the command channel remains active in both transmit and receive direction providing that the address bit (AD ;CMDR) matches the address strapped on SP1, SP2.

In power down however both data channels are disabled; SIP being tristated during data channel transmit time slots.

Receive direction (RX)
SLD → ARCOFI

Transmit direction (TX)
ARCOFI → SLD



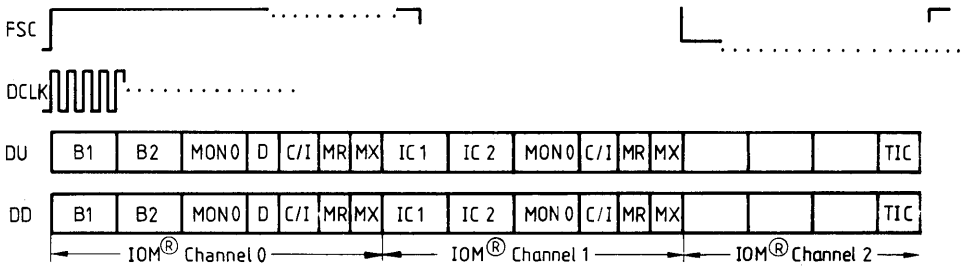
B# 1,2: Data Channel
FC : Feature Control Channel
SIG : Signaling Channel

IOM-2 Interface

The IOM-2 interface consists of two data lines and two clock lines. DU: Data Upstream carries data from the ARCOFI to the layer-1 device and DD: Data Down stream carries data from the layer-1 device to the ARCOFI. A FSC Frame Synchronization Clock is supplied to the ARCOFI as well as a DCLK 1.536-MHz data clock for bit clocking.

In terminal mode the IOM-2 frame consists of three IOM channels numbered respectively 0,1 and 2. The ARCOFI can receive and transmit voice data in the IOM B1 & B2 channels as well as in the IC1 and IC2 intercommunication channels located in IOM channel 0 and 1 respectively.

The IC1 and IC2 intercommunication channels can be used in the terminal for local bearer data communication. This makes post-processing of voice/data information possible.



IOM-2 Monitor Channel

All programming data required by the ARCOFI including coefficients are transmitted exclusively in the monitor 1 time slot in the IOM channel 1. The MON1 monitor channel allows a point to multi-point access where the layer-1 component acts as master to programmable devices like the ARCOFI. Each programmable device is accessed by sending a specific address byte at the start of each command stream followed by an identification byte. The programmable device compares the received address byte with its own internally wired IOM address before executing a command.

All programmed coefficients can be read back when issuing an appropriate CMDR read. The ARCOFI responds by sending two IOM-2 specific bytes unambiguously identifying the chip type and version followed by the issued SOP or COP read sequence.

Monitor Transfer Protocol

The transfer of a low of commands in the MON1 channel is regulated by a handshake protocol mechanism implemented by two bits MX and MR in the fourth slot of the IOM channel 1. The maximum effective transfer rate in the MON1 channel is 32 kbit/s. Thanks to the implemented handshake mechanism a command sequence can be delayed at the convenience of the transmitting IOM bus master device and resumed subsequently. An abort mechanism allows the interruption of a command sequence. In that case the command may be partially executed by the ARCOFI (i.e. coefficients partially modified in the ARCOFI CRAM). If use of the abort mechanism is made, a new command has to be issued to program the ARCOFI.

C/I Channel

The first four bits of the IOM Channel 1 C/I channel are transparently routed to the four ARCOFI PCI pins SA-SD. SA & SB from the presently addressed ARCOFI are shown in the 3rd and 4th C/I bit position. The SP1 and SP2 strapping as well as the AD-bit in the CMDR register determine which ARCOFI is adressed.

Pins SA-SD can be configured individually as input or output and will appear respectively in the DD or DU CH1-C/I channel.

Tihe mapping of the peripheral control interface (PCI) pins SA,SB,SC,SD into the six C/I channel bits depends on the hardwired SP1 address as follows:

SP1 = 1

DD and DU	–	–	SB	SA	SD	SC	–	–

SP1 = 0 (AM = 0; two chip mode)

DD and DU	SD	SC	–	–	–	–	–	–

SP1 = 0 (AM = 1; one chip mode)

DD and DU	SD	SC	SB	SA	–	–	–	–

The ARCOFI with the address pin SP1 strapped to 0 transmits/receives the SD and SC values on DU/DD

In case a reset has been asserted, the SA to SD pins are programmed as input, however the SA to SD values are not switched to the C/I channel unless a CR1 to CR4 SOP_0 write command is issued.

Programmable Registers

The SLD or the IOM-2 bus mode is used to control and program the operations performed by the ARCOFI. The following lists the ARCOFI internal registers.

ARCOFI Digital Interface (ADI)

- CMDR: 8-bit command register
- CR1-4: four 8-bits configuration registers

ARCOFI Signal Processor (ASP)

- Two transmit gain registers (GX)
- Two receive gain registers (GR)
- 10 FX filter coefficient registers
- 10 FR filter coefficient registers
- One Z sidetone gain register
- Two DTMF frequency tone registers
- 6 Tone ring/tone generator frequency register
- 3 Tone ring/tone generator amplitude register
- 6 Beat tone generator timing register

To familiarize the user with ARCOFI, a program, named ARCOS, is available. (see description of ARCOS page 602).

This software tool allows the user to program the different ARCOFI registers and to evaluate the chip in a real environment.

Filter Programming Ranges

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit	Tolerance
GX-filter[1])		0	6	dB	0.25 dB
GR-filter		−6	0	dB	0.25 dB
Z-filter		−∞	0	dB	± 1 dB
Tone generator gain	G_{Tone}	−∞	0	dB	
Tone generator frequency	f_{Tone}	0	4000	Hz	
Tone generator time	t_{Tone}	1	16384	ms	
DTMF generator		380	1630	Hz	± 1%

[1]) Remark: The programming of GX-filter depends on the programming of the half-channel (AFE).

A DTMF generator is also built into the ARCOFI transmit path.

A preemphasis of 2 dB is guaranteed between the high and the low DTMF frequency groups. The total power level of all unwanted frequency components is at least 20 dB below the level of the low frequency group component of the signal.

The level of any unwanted frequency component does not exceed the following limits:

- In the frequency band 0-300 Hz: > −33 dB
- In the frequency band 300-3400 Hz: > 20 dB
- In the frequency band 3400-4000 Hz: > −33 dB

All generated DTMF frequencies are guaranteed within a ± 1% deviation.

DTMF Frequency Programming

CCITT Q.23	ARCOFI Nominal	Relative Deviation from CCITT*	Hex Coefficient H nibble/L nibble
Low Group			
697	697.754	+1081 ppm	F8
770	773.438	+4464 ppm	A8
852	852.783	− 513 ppm	F9
941	939.453	−1646 ppm	BA
High Group			
1209	1203.125	−4883 ppm	21
1336	1339.844	+2877 ppm	40
1477	1476.563	− 295 ppm	10
1633	1632.813	− 114 ppm	00

*: The deviations due to the inaccuracy of the incoming clock CLK, when added to the nominal deviations tabulated above give the total absolute deviation from the CCITT recommended frequencies.

Command Register (CMDR)

	Logical 1	Logical 2
BIT 7	AD=1; if bit AD matches the address convention strapped on SP1; pin SIP is active as output during SLD transmit time slots.	AD=0; if address bit is not consistent with the logical level strapped on SP1; SIP is tristated during SLD transmit time slots.
BIT 6	R/W=1; reading from CR1, CR2, CR3, CR4 or CRAM.	R/W=0; writing to CR1, CR2, CR3, CR4 or CRAM.
BIT 5	PU=1; The ARCOFI is in a normal operating mode (powered up).	PU=0; The ARCOFI is placed in stand by (powered down). All register contents are saved.
BIT	RCS=1; receive and transmit in CH-B2.	RCS=0; receive and transmit in CH-B1.

Note: RCS versus AM bit

a) In case of one chip mode (AM=1) RSC operates as described above.

b) In case of two chip mode (AM=0) and pin SP1 is strapped to 0 same as above. If SP1 is strapped to 1, RCS operates in reverse order:

RCS=1 RX and TX in channel B1
RCS=0 RX and TX in channel B2

This provides a contention-free switching of the B1 & B2 channels while in two-chip mode.

A full sequence consists of a command byte followed by <..>n byte coefficients.

BIT 3 2 1 0	CMD Name	Status Mode	CMD Sequence Length	CMD Sequence Description	; Comments
0 0 0 0	SOP_0	R/W	5	<CR4><CR3><CR2><CR1>	; Reset F flag
0 0 0 1	COP_1	R/W	5	<t1><t1><f1><f1>	; Beat tone time span ; T1 & tone generation ; frequency F1
0 0 1 0	COP_2	R/W	3	<gx1><gx2>	; GX gain
0 0 1 1	COP_3	R/W	5	<t2><t2><f2><f2>	; Beat tone time span ; T2 & tone generation ; frequency F2
0 1 0 0	SOP_4	R/W	2	<CR1>	; Configuration reg. 1
0 1 0 1	SOP_5	R/W	2	<CR2>	; Configuration reg. 2
0 1 1 0	SOP_6	R/W	2	<CR3>	; Configuration reg. 3
0 1 1 1	SOP_7	R/W	2	<CR4>	; Configuration reg. 4
1 0 0 0	COP_8	R/W	3	<dtmf_high><dtmf_low>	; DTMF frequencies
1 0 0 1	COP_9	R/W	5	<gz><a3><a2><a1>	; GZ gain & tone ; generator amplitudes ; A1, A2, A3
1 0 1 0	COP_A	R/W	9	<fx1><fx2><fx3><fx4> <fx5><fx6><fx7><fx8>	; FX frequency correc- ; tion coefficient set 1
1 0 1 1	COP_B	R/W	3	>gr1><gr2>	; GR gain
1 1 0 0	COP_C	R/W	9	<fr1><fr2><fr3><fr4> <fr5><fr6><fr7><fr8>	; FR frequency correc- ; tion coefficient set 1
1 1 0 1	COP_D	R/W	5	<fr9><fr10><fx9><fx10>	; FX & FR coefficient ; set 2
1 1 1 0	COP_E	R/W	5	<t3><t3><f3><f3>	; Beat tone time span ; T3 & tone generation ; frequency F3
1 1 1 1	NOP	R		<hFF>	; No operation; CMDR ; bits 7,6,5,4 ; are masked
		W			; No operation, CMDR ; bits 7,6,5,4 can be ; written

W: ; write
R: ; read
<..> ; mandatory byte coefficient sequence

BITS

7	6	5	4	3	2	1	0
AD	R/W	PU	RCS	CMB3	CMB2	CMB1	CMB0

Initial value on RESET: $0F_H$ (NOP)

Configuration Register 2 (CR2)

	Logical 1	Logical 0
BIT 7	SD=1; SD pin programmed as input.	SD=0; SD pin programmed as output.
BIT 6	SC=1; SC pin programmed as input.	SC=0; SC pin programmed as output.
BIT 5	SB=1; SB pin programmed as input.	SB=0; SB pin programmed as output.
BIT 4	SA=1; SA pin programmed as input.	SA=0; SA pin programmed as output.
BIT 3	ELS=1; PCI pins SA-SD, which are not programmed as TX-SIG transmit inputs, tristate SIP in TX direction.	ELS=0; pins SA-SD, which are not TX-SIG inputs, are sending zeros.
BIT 2	AM=1; only one device is connected to the SLD bus, send NOP's during TX-FC.	AM=0; two devices are to the SLD bus, tristate SIP during TX-FC.
BIT 1	TR=1; Three party conferencing enabled CH-B1 is added to CH-B2 in the RX direction.	TR=0; Three party conferencing disabled.
BIT 0	SLD Mode EFC=1; Enable feature control. TX-FC channel is enabled.	EFC=0; TX-FC channel disabled (high Z).
	IOM-2 Mode SEL=1; Bearer channels transmit & receive in IOM channel 0.	SEL=0; B channels transmit & receive in IOM channel 1.

BITS	7	6	5	4	3	2	1	0
	SD	SC	SB	SA	ELS	AM	TR	EFC/SEL

Initial value on RESET: $F9_H$

Configuration Register 1 (CR1)

	Logical 1	Logical 0
BIT 7	GR=1; GR gain loaded from CRAM	GR=0; GR gain set to 0 dB
BIT 6	GZ=1; Z gain loaded from CRAM	GZ=0; Z gain set to −18 dB
BIT 5	FX=1; X filter loaded from CRAM	FX=0; X filter set to 0 dB flat
BIT 4	FR=1; R filter loaded from CRAM	FR=0; R filter set to 0 dB flat
BIT 3	GX=1; GX gain loaded from CRAM	GX=0; GX gain set to 0 dB

BIT 2	1	0	Test Mode	Configuration Description
0	0	0	NOT	No test mode
0	0	1	ALS	Analog loop back via converter registers.
0	1	0	ALM	The MIC/XIN input is looped back to HON & HOP. (AHO amplifier) the FHM input is looped back to analog MUX. FHM input is looped back to LSN & LSP. (ALS amplifier)
0	1	1	BYP	By-pass: the analog front end is by-passed. FHM serves as a direct single ended input to the A/D-converter while HOP outputs the single ended signal generated by the D/A converter.
1	0	0	IDR	Data RAM initialisation, reset all data RAM locations to hex 00.
1	0	1	DLS	Digital loop back via converter registers.
1	1	0	DLM	The D/A output is looped back to the A/D input via the analog I/O MUX.
1	1	1	DLP	Digital loop back via PCM registers.

BITS	7	6	5	4	3	2	1	0
	GR	GZ	FX	FR	GX	TMB2	TMB1	TMB0

Initial value on RESET: 00_H

Configuration Register 3 (CR3)

BIT 7 6 5 — Analog gain adjustment in transmit direction for the MIC input. Gain factor tolerance range ± 0.5 dB

0	0	0	52.0 dB default on RESET	0	1	1	34.0 dB
0	0	1	46.0 dB	1	0	0	28.0 dB
0	1	0	40.0 dB	1	0	1	22.0 dB
1	1	1	X input enabled with a 15.1 dB amplification factor MIC input disabled	1	1	0	17.0 dB

BIT 4 3 2 — Operating mode — Configuration description: Analog Front End Control (AFEC)

Code	State	MIC/IN	FHM	H OUT	L OUT	Comments
0 0 0	POR	OFF	OFF	OFF	OFF	Power on reset
0 0 1	RDY	ON	OFF	ON	OFF	Ready
0 1 0	LH1	OFF	OFF	OFF	ON	Loud hearing 1
0 1 1	LH2	ON	OFF	OFF	ON	Loud hearing 2
1 0 0	LH3	ON	OFF	ON	ON	Loud hearing 3
1 0 1	HFS	OFF	ON	OFF	ON	Hands-free
1 1 0	MUT	OFF	OFF	ON	OFF	Mute
1 1 1	RES	X	X	X	X	Reserved

BIT 1 0 — Operating Mode — Linear Input/Output (LIO)

0 0	LIO 0 Normal I/O Mode	B#1	B#2	FC	SIG	B#1	B#2	FC	SIG
0 1	LIO 1; ELS = 0 Mixed I/O Mode	B#1	B#2	FC	SIG	B#1	B#2	MSB	LSB
1 0	LIO 2 Linear I/O Mode	MSB	LSB	FC	SIG	MSB	LSB	FC	SIG
1 1	LIO 3 Reserved								

BITS

7 6 5	4 3 2	1 0
AGX	AFEC	LIO

Initial value on RESET: 00_H

Configuration Register 4 (CR4)

	Logical 1	Logical 0
BIT 7	DHF=1; digital high-pass in TX direction enabled	DHF=0; digital high-pass in TX disabled
BIT 6	DTMF=1; DTMF generator enabled	DTMF=0; DTMF generator enabled
BIT 5	TG=1; tone ring enabled	TG=0; tone ring disabled
BIT 4	BT=1; beat tone generator enabled	BT=0; beat tone generator disabled
BIT 3	TM=1; tone mode bit set, incoming voice is activated	TM=0; incoming voice is blocked
BIT 2	BM=1; beat mode. 3 tone ring activated when BT generator enabled.	BM=0; 2 tone ring activated when BT generator enabled.
BIT 1	PM=1; piezo mode bit set, tone generator is outputed to the piezo ring pins SA & SB	PM=0; the tone generator is directed to the loudspeaker (D/A out)
BIT 0	A/μ=1; μ law enabled	A/μ=0; A law enabled

BITS

7	6	5	4	3	2	1	0
DHF	DTMF	TG	BT	TM	BM	PM	A/μ

X: don't care

Initial value of RESET: 00_H

ARCOFI Software Tool: ARCOS

The ARCOS program kit provides the means to exercise the PSB 2160 ARCOFI in a real environment. The ARCOFI capabilities are made easily understandable thanks to a "DIALOG MODE" allowing direct programming of the component. Various operating conditions can be programmed into the ARCOFI registers so as to evaluate ist performances. The support software has also been designed to generate all the necessary coefficients to program the Siemens PSB 2160 ARCOFI signal processor.

ARCOS supports:

- Generation of coefficients for the three ARCOFI tone generator registers
- Generation of coefficients for the ARCOFI DTMF tone generator registers
- Generation of coefficients for the two ARCOFI programmable gain registers GX and GR.
- Generation of coefficients for the Z side tone gain register
- Generation of coefficients for the FX and FR correction filter registers. Adaptive software calculates coefficients to fit a target amplitude frequency response. All these features are provided under the "Search Coefficient" mode.
- A user friendly dialogue mode allowing full programming of the ARCOFI configuration registers and coefficient RAM.
- Statistical information menus allowing users to explore the programming possibilities of the ARCOFI
- ARCOFI transmission measurements using the Wandel & Goltermann PCM-4.

Figure 3
ARCOS Main Menu

```
ARCOFI® COEFFICIENT SOFTWARE
A R C O S                                   Version 3.0

Copyright 1988      Siemens AG      Munich,      West-Germany

Search Coefficient ..... (S)
Statistical Information ..... (I)
Dialog-Mode ..... (D)

Quit ..... (Q)

ARCOS>
```

Search Coefficient Mode

With this mode the user can ask whether a specific value of a filter is available or not. The answer is the closest values available, their corresponding coefficient as well as the deviation from the desired value.

Figure 4
Search Coefficient Mode

Search Coefficient

Syntax		Unit		Example	Range
D[TMF]	{Frequency}	[Hz]	D	660 1200	380 .. 1650 Hz
F[req]S	{Frequency}	[Hz]	FS	500 600.5	0 .. 8000 Hz
F[req]	{Frequency}	[Hz]	FT	500 600.5	0 .. 4000 Hz
T[ime]	{Time}	[ms]	T	1000 20 333	1 .. 16400 ms
					- ∞ .. 0 dB
GZ or G[ain]	{Gain}	[dB]	GZ	8	- ∞ .. 14 dB
GX or GR	{Gain}	[dB]	GX	12 2 -4	0 .. 1
GZ> or G>	{Value}	[--]	GZ>	0.34	0 ..
GX> or GR>	{Value}	[--]	GX>	2.34 0.54	

FX or FR A gain Fb freq Fc freq [A gain Fb freq Fc freq]
FX or FR Filename [Fast I Middle I Best]
FX or FR ? [Filename I =]

S[ound]	--	Sounds last specified Square-Frequencies and Times
O[utput]	--	Output to PRN, Harddisk, Screen
Q[uit]	--	Quit
<CR>	--	This Picture

ARCOS>

Statistical Information Mode

The **"Statistical Information"** mode permits the generation of tables showing the coefficients of different filters or generators and makes analysis of accuracy possible.

Figure 5
Statistical Information Menu

Statistical Information

Frequency DTMF-Tone Generator ..... (D)
Frequency Tone Generator (Trapezoid) ..... (F)
Frequency Tone Generator (Square) ..... (S)
Time Tone Generator ..... (T)
Gain Tone Generator and GZ-Filter ..... (G, Z)
Gain GX- and GR-Filter ..... (X, R)

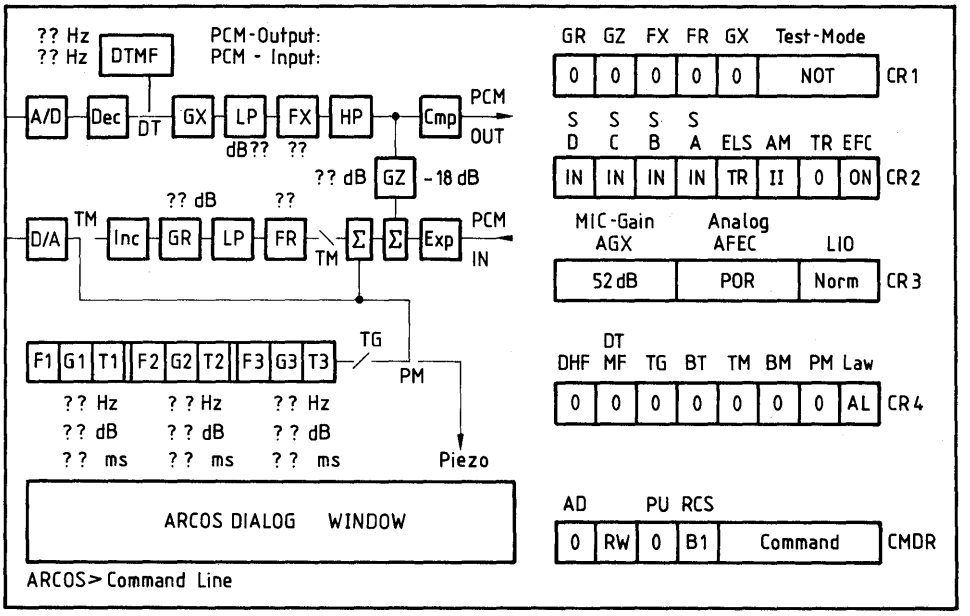
Output to PRN, Harddisk, Screen ..... (O)
Quit ..... (Q)

ARCOS > **T**

Dialog Mode

With the dialog mode the user becomes familiar with the ARCOFI chip in a real environment. The configuration registers as well as coefficients in CRAM can be read and written. Any change of register content is instantaneously carried out and the new status of ARCOFI is displayed on the screen.

Figure 6
Dialog Mode



The program ARCOS runs on IBM- and IBM-compatible PC when the last is equipped with a Siemens ISDN User Board SIPB 5000.

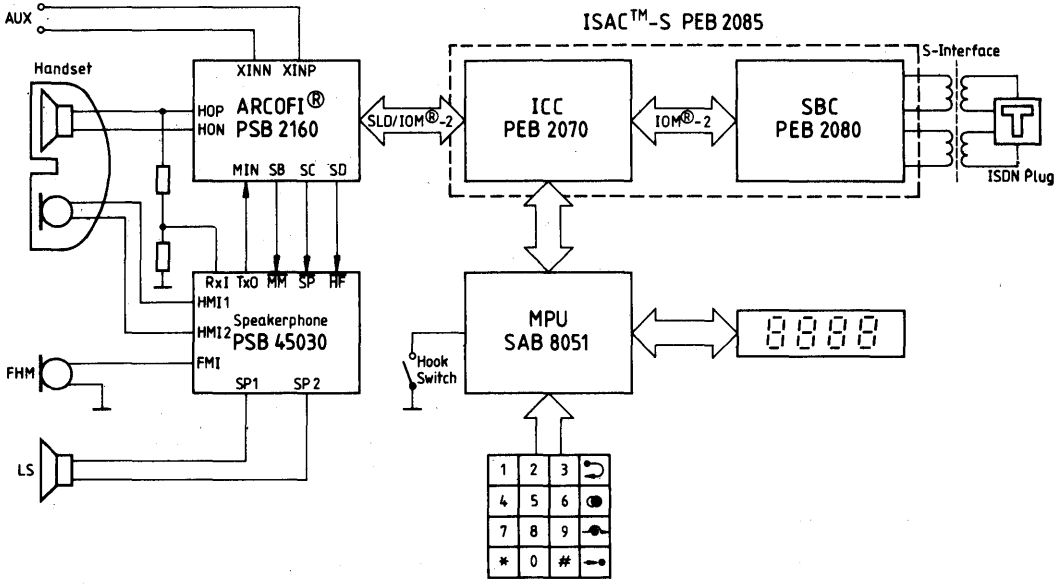
Nevertheless a shrinked version of ARCOS, named ARCOSD (ARCOS-DEMO), works without user board and provides the user with the modes "Search Coefficient" and "Statistical Information".

Application Suggestions

The ARCOFI forms, together with a PEB 2070 ICC and a PEB 2080 SBC (resp. a PEB 2085 ISAC-S) a solution for a complete digital telephone as specified in the CCITT I-series recommendation at the "S" reference point.

The digital telephone can be expanded for hands-free applications by adding the voice switched speakerphone circuit PSB 45030.

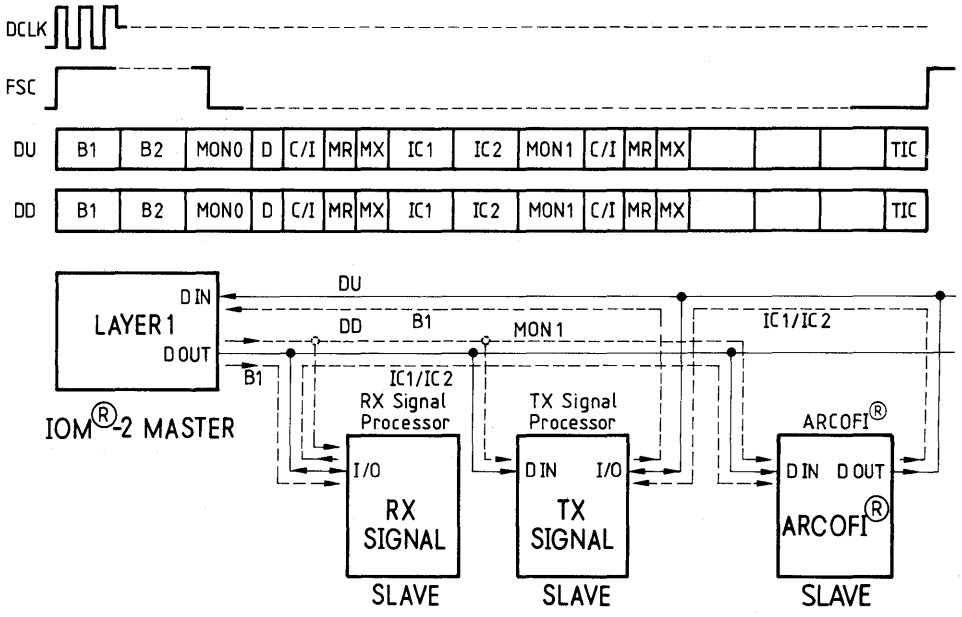
Application Circuit



The terminal mode IOM-2 frames consist of three IOM channels numbered respectively 0,1 and 2. The ARCOFI can receive and transmit voice data in the IOM B1 & B2 channels as well as in the IC1 and IC2 intercommunication channels located in IOM channels 0 and 1 respectively.

The IC1 and IC2 intercommunication channels can be used in the terminal for local data communication. This makes postprocessing of voice/data information possible **(see figure 7)**.

Figure 7
Post Processing the ARCOFI Voice Channels



IOM-2 Digital Subscriber Controller (DSC/E) PSB 70C30E

ADVANCE INFORMATION

General Description

The PSB 79C30E Digital Subscriber Controller (DSC) provides the Terminal Equipment access to the ISDN. The PSB 79C30E is compatible with the CCITT I-Series recommendations at the 'S'- reference point allowing the user of the device to design TEs which conform to the international ISDN standards.

The PSB 79C30E provides a 192 kbit/s full duplex digital path between the TE located in the subscriber's premises and the NT or PABX line card over 4-wires. The PSB 79C30E separates the bit stream into the B1- (64 kbit/s), B2- (64 kbit/s) and D- (16 kbit/s) channels. The B channels are routed to different sections of the PSB 79C30E under user control. The D channel is partially processed in the PSB 79C30E and passed to the microprocessor for further processing.

The transmission rate of 192 kbit/s provides a 48-bit frame every 250 µs for framing and maintenance. The frame structure provides for frame synchronization and multiple terminal contention resolution as described in the CCITT I-series recommendations. Both point-to-point and point-to-multipoint connections are supported.

The PSB 79C30E can be used as a voice telephone, a digital data terminal, or a voice and data terminal.

The audio processor in the PSB 79C30E, uses Digital Signal Processing (DSP) to implement the codec and filter functions. The audio processor interfaces to a speaker, an earpiece, and two separate audio inputs. In the receive and transmit paths the user may program gain or alter the frequency response.

A serial port gives the user access to the B-channels of the PSB 79C30E multiplexer. This serial port may be used by data terminals and provides, with additional circuitry, access to the CCITT 'R' reference point.

The PSB 79C30E is controlled via an interrupt driven microprocessor bus interface by an external microprocessor. Using this interface, the microprocessor processes the D-channel information and programs the PSB 79C30E accordingly. This includes programming a multiplexer within the PSB 79C30E to route the B-channels as specified by the D-channel control information. The microprocessor can interrogate and program the PSB 79C30E via its mode, status, and error registers.

Features

- Combines CCITT I.430 S/T interface transceiver, D-channel LAPD processor, and audio processor in a single chip
- Interrupt-driven microprocessor interface
- CMOS technology, TTL compatible
- 'S' 'T' interface transceiver
  Level-1 physical layer controller
  Supports point-to-point, short or extended passive bus configurations
  Multiframe support
- D-channel processing capability
  Flag generation/detection
  CRC generation/checking
  Zero insertion/deletion
  Four 2-byte address detectors
  Random number generation
  16-byte transmit and 32-byte receive FIFOs
- Audio processing capability
  Dual audio inputs
  Earpiece and loudspeaker drivers
  Filter/codec with A/μ-law selection
  Programmable gain and equalization filters
  Programmable sidetone level
  Programmable DTMF, single tone, and ringer tone generation
- IOM-2 interface

- Packages: PSB 79C30E-P: P-DIP-40
  PSB 79C30E-N: PL-CC-44

SIEMENS

ISDN Terminal Adaptor Circuit (ITAC) PSB 2110

Advanced Information **CMOS IC**

Type	Ordering Code	Package
PSB 2110-N	Q67100-H8644	PL-CC-44 (SMD)
PSB 2110-P	Q67100-H8643	P-DIP-40

General Device Overview

The ISDN Terminal Adaptor Circuit (ITAC™) is a circuit designed to interface existing standard Data Terminal Equipment (DTE) to an ISDN via the R reference point (CCITT I.411).

The circuit autonomously adapts asynchronous or synchronous data according to CCITT V.110, X.30 and I.460.

It also supports rate adaption according to V.120 or DMI as well as in-band signaling.

System Implementation

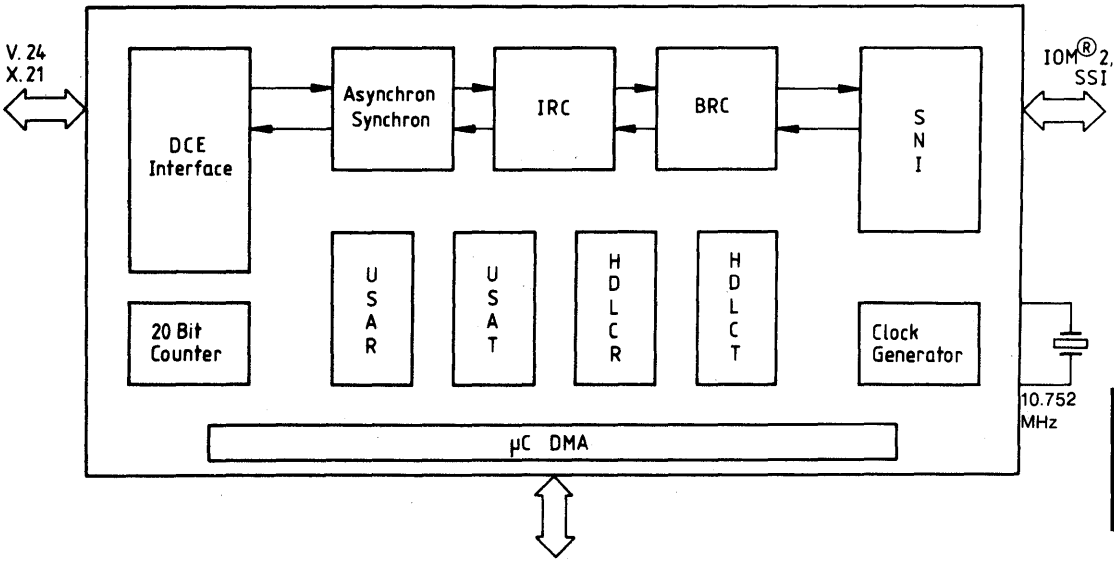
A typical implementation of an ISDN S-interface access for a conventional X-or V-series terminal using the ITAC is shown in the block diagram (terminal adaptor according to V.110, X.30, ECMA.102).

The ITAC can be connected via a serial synchronous interface to an S-bus transceiver/LAPD controller (in this case, the ISDN Subscriber Access Controller ISAC™-S). These two devices, together with the terminal controller, convert V- and X-series interface characteristics to the functional and procedural interface characteristics required by an ISDN at the S interface.

Features

- Terminal adaptor for ISDN (R interface), PCSN and CSPDN
- Support of async and sync interfaces (X.21, X.21 bis, V.25 bis, V.24, RS232C).
- Programmable speeds from 300 bit/s to 64 kbit/s
- Bit stuffing rate adaption according to latest standards (X.30, V.110, ECMA.102)
- Programmable subchannels for intermediate rates
- IOM® SSI compatible interface to network (up to 4 Mbit/s)
- Parallel 8-bit microcontroller interface
- DMA interface
- Programmable test options
- Higher protocol support
- In-band signaling
- V.120, DMI (bit transparent)
- Single +5 V supply, low power CMOS technology

Block Diagram



SIEMENS

ISDN Remote Power Controller (IRPC) PSB 2120

Preliminary Data **CMOS IC**

Type	Ordering Code	Package
PSB 2120-P	Q67100-H8645	P-DIP-22

The PSB 2120 is a pulse width modulator circuit designed for fixed-frequency switching regulators especially for telefony and ISDN environments.

The PSB 2120 is fully compatible with the CCITT power recommendations on the S interface.

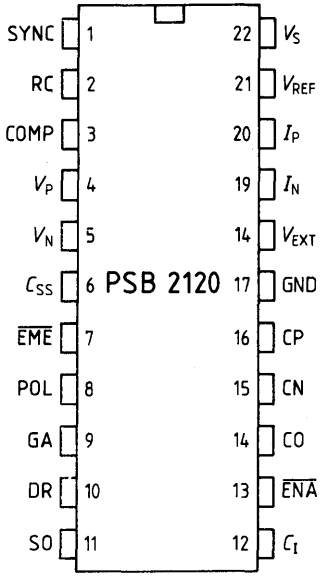
Coupled with few external components it provides a stable DC 5 V supply for subscriber terminals (TEs) or network terminations (NTs). It can also be programmed for higher output voltages, e.g. to supply the S-lines with 40 V. In telefony and ISDN systems a high conversion yield is crucial to maintain functionality in all supply conditions via "S" or "U" interfaces. The PSB 2120 design and technology realize high conversion efficiency and low power dissipation.

It should be recognized that the PSB 2120 can also be used in numerous DC/DC conversion systems other than ISDN power supplies.

Features

- Switched mode DC/DC-converter
- CCITT (I.430) ISDN compatible
- Integrated 200 V power FET
- Low power dissipation
- Supply voltage range 10 V to 60 V
- Input undervoltage protection
- Programmable overcurrent protection
- Soft start
- Control circuit achieve minimum start-up current
- Power housekeeping input
- Oscillator synchronization input/output
- Polarity reversal detection
- High voltage CMOS technology 60 V

Pin Configuration
(top view)



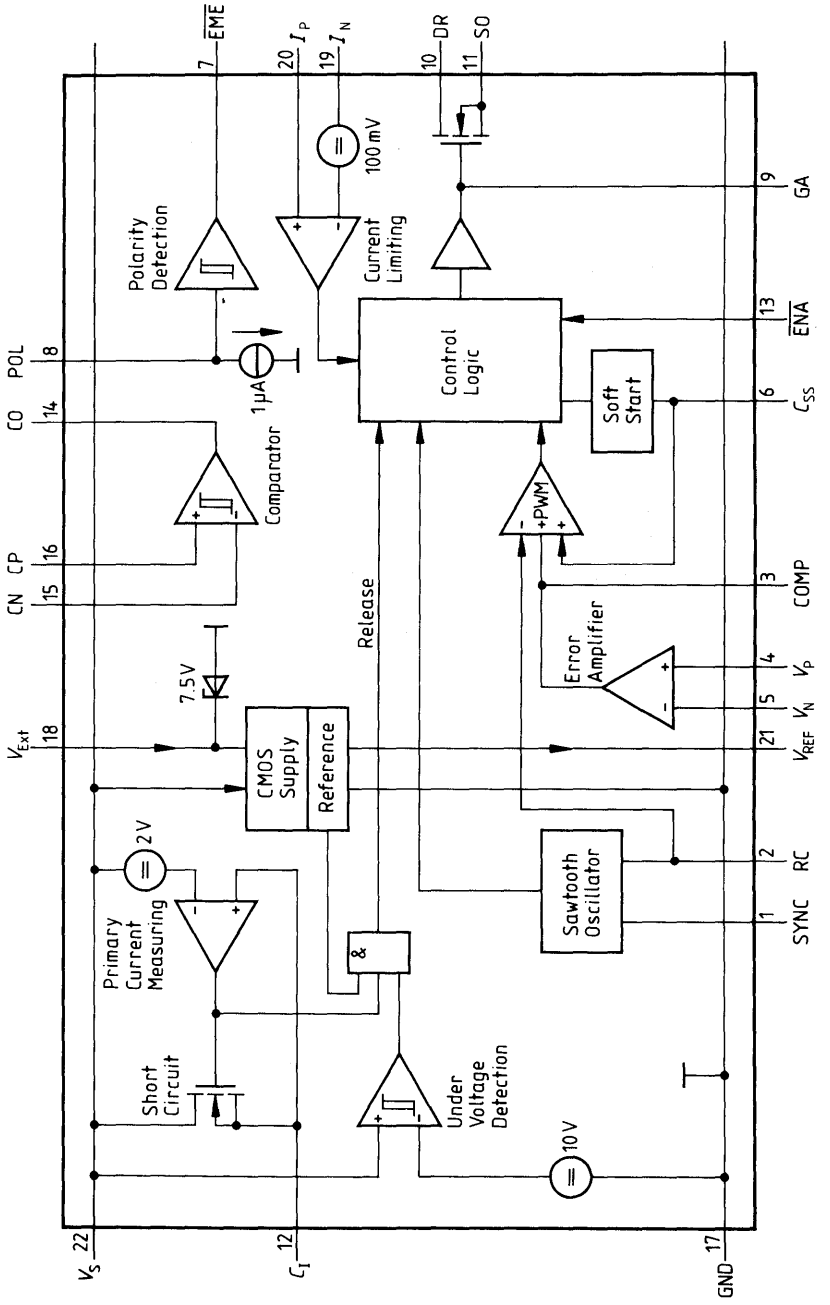
Pin Definitions and Functions

Pin No.	Symbol	Input (I) Output (O)	Definition	Function
1	SYNC	I/O	Synchronization	Input for synchronization of the oscillator to an external frequency, or output to synchronize multiple devices.
2	RC	I	RC-Oscillator	The external timing components of the ramp generator are attached to thin pin.
3	COMP	O	Compensation	Error amplifier output and **P**ulse **W**idth **M**odulator (PWM) input for loop stabilization network.
4 5	V_P V_N	I I	Pos. voltage sense Neg. voltage sense	Non inverting input of the error amp. Inverting input of the error amplifier.
6	C_{SS}	I	Soft start capacitor	The capacitor at this pin determines the soft start characteristics.
7	$\overline{EME}$	O	$\overline{Emergency}$	A low input voltage at POL will active the output $\overline{EME}$.

Pin Definitions and Functions (cont'd)

Pin No. P-DIP	Symbol	Input (I) Output (O)	Definition	Function
8	POL	I	Polarity detection	POL is the input to a non inverting Schmitt-trigger.
9	GA	O	Gate	Output of the FET driver.
10	DR	O	Drain	Drain connection of the power FET.
11	SO	I	Source	Source connection of the power FET.
12	C_I	I	Input capacitor	C_I has to be connected to the input buffer-capacitor and a current limiting charging-resistor.
13	$\overline{\text{ENA}}$	I	$\overline{\text{Enable}}$	A high input voltage at this pin will stop the IRPC function.
14	CO	O	Comparator output	Connection of the universal usable comparator.
15	CN	I	Comparator negative input	
16	CP	I	Comparator positive input	
17	GND	I	Ground	All analog and digital signals are referred to this pin.
18	$V_{S\,EXT}$	I/O	Externally supply	Output of the internal CMOS supply. Via V_{EXT} the internal CMOS circuits can be supplied from an external DC supply in order to reduce chip power dissipation.
19	I_N	I	Neg. current sense	When the voltage difference between these two pins exceeds 100 mV, the digital current limiting becomes active.
20	I_P	I	Pos. current sense	
21	V_{REF}	O	Reference voltage	Output of the 4.0 V reference voltage.
22	V_S	I	Supply voltage	V_S is the positive input voltage.

Figure 1
IRPC Functional Diagram



Functional Description

The reference provides a 4.0 V voltage for the regulation loop. A high gain error amplifier compares the reference voltage with the switch mode supply output voltage. The output of the error amplifier is compared with a periodic linear ramp, generated by the sawtooth-oscilator circuit. The comparator output is a fixed-frequency, variable pulse width logic signal, which passes through logic circuits to the high voltage power-switching-FET.

A digital current limiting device suppresses the PWM logic signal when the voltage difference at the current limit sense input reaches 100 mV. In this case the control logic inhibits double pulses during one oscillator period.

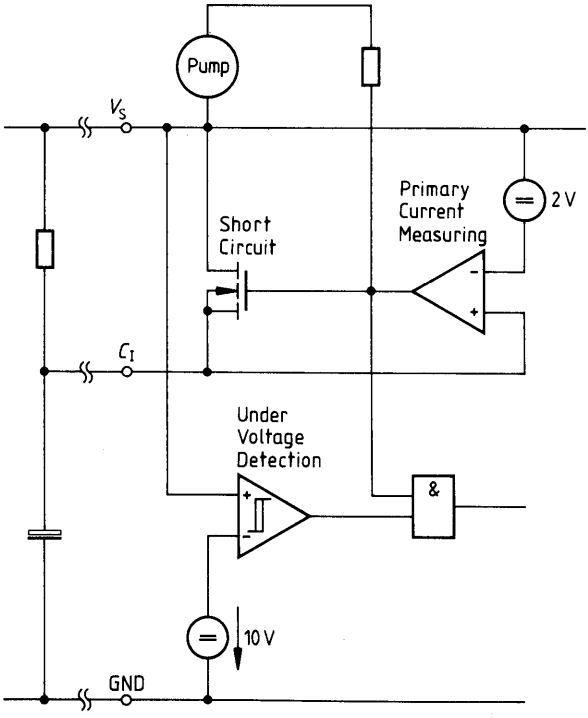
1. Start-Up Procedure

Before the switched-mode DC/DC-converter starts, a sequence of several conditions has to be passed in order to avoid any system malfunction. The primary undervoltage detection inhibits the converter function. This insures that all control functions have stabilized in the proper state when the turn on voltage (ca. 10 V) is reached, and it prevents from start-up glitches. In case of connectig the TE to powered lines or if a line is powered up, the charge current of the primary buffer capacitor is limited by an external resistor **(figure 2)**.

This resistor is short-circuited by the PSB 2120 when the voltage drop across it falls below about 2.0 V. The residual resistance of this short-circuit is about 3 Ω. In case of a primary undervoltage detection the short-circuit will be always deactivated. So the DC/DC-converter does not start until the charging of the primary buffer capacitor is completed, and the maximum line input voltage is reached. (If this feature is not desired, C_I has to be connected to GND. In this case the primary current measuring circuit turns off, to reduce chip-power dissipation from 9 mW to 6 mW). In order to avoid high current peaks during the charging of the secondary capacitors or line capacitors in case of supplying a S interface, a soft start circuit is implemented in the PSB 2120. This circuit requires an external capacitor, connected between C_{SS} and GND.

In addition, the Enable input ($\overline{ENA}$) allows an external switch-on/switch-off control. In the DC/DC-converter is disabled via $\overline{ENA}$, the soft start-capacitor at pin C_{SS} is discharged. This input can also be used for several other functions, e. g. secondary overvoltage protection.

Figure 2



2. DC/DC-Conversion

The PSB 2120 contains a SIPMOS transistor for power handling. Non-isolated and isolated SMPS configurations are possible. Logic and analog circuits are implemented in CMOS in order to achieve low power dissipation.

The error amplifier compares the sensed voltage with a reference attached to V_P and thus controls the Pulse With Modular (PWM). The conversion frequency is generated by a sawtooth oscillator which can be controlled by external RC-components or by an external synchronization signal. The PSB 2120 is synchronized by the rising edge of the SYNC signal, whose frequency must be 10 % higher than the free run frequency, determented by the RC-components. The SYNC pin can also be used as a trigger-output. As long as the capacitor of the sawtooth oscillator is discharged, SYNC is high.

The output of the PWM is processed by the control logic and fed to the SIPMOS transistor The control logic suppresses higher oscillations of the regulation loop caused e.g. in case of current limit detection.

3. Polarity Detection

Emergency conditions are signaled to the TE by the reversed polarity of the line feeding voltage. When polarity reversal is detected via pin POL of the PSB 2120, emergency conditions are signaled to the microprocessor via pin $\overline{EME}$, which should shut down all activity except simple telephony functions to minimize power dissipation.

The polarity detection circuit can also be used for other detection or protection functions, e. g. programmable primary undervoltage detection.

4. Power Housekeeping

An integrated 6 V linear voltage supplies the internal circuits during the start-up phase. Power dissipation of this regulator can be reduced, if an auxiliary winding of the transformer or an external supply is used for that purpose by connecting it to V_{EXT}. If the input voltage at V_{EXT} reaches 6.3 V the internal linear voltage regulator turns off and the internal circuits are fed from this external voltage. In this case the input current at V_{EXT} is approx. 0.5 mA.

Note: An internal 7.5 V Z-diode protects the V_{EXT} input against overvoltages. The maximum Z-current is 2 mA! If the external supply isn't stabilized, the input current must be limited (e. g. by a resistor)!

5. Interface to Microprocessor

The PSB 2120 offers two TTL-compatible signals: $\overline{EME}$ and CO.$\overline{EME}$ (Emergency) becomes active, if polarity reversal is detected. CO is the output of a universal useable comparator; e. g.: to generate a microprocessor-reset signal.

6. PSB 2120 Application in ISDN Environments

Figure 3 shows an example out of the wide application field of the PSB 2120. In the network termination one PSB 2120 supplies the internal ICs directly from the "U" interface. A second IRPC, also powered from the "U" interface. A second IRPC, also powered from the "U"-line, supplies the "S" interface if the main supply of the NT is out of order. A third IRPC is used in the main supply to regulate the "S"-line feeding voltage.

In the subscriber terminal the PSB 2120 is used for feeding the internal circuits. The PSB 2120 accomodates both galvanically isolated and non-isolated configurations. Considering the diversity of DC/DC-converter applications, this part of the specification only shows how to use the special ISDN features of the PSB 2120.

The simpliest form of a flyback converter is shown in **figure 4**. The time constant of the soft start circuit is programmed by a capacitor at pin 6 (C_{SS}).

Figure 3
IRPC in ISDN Concept

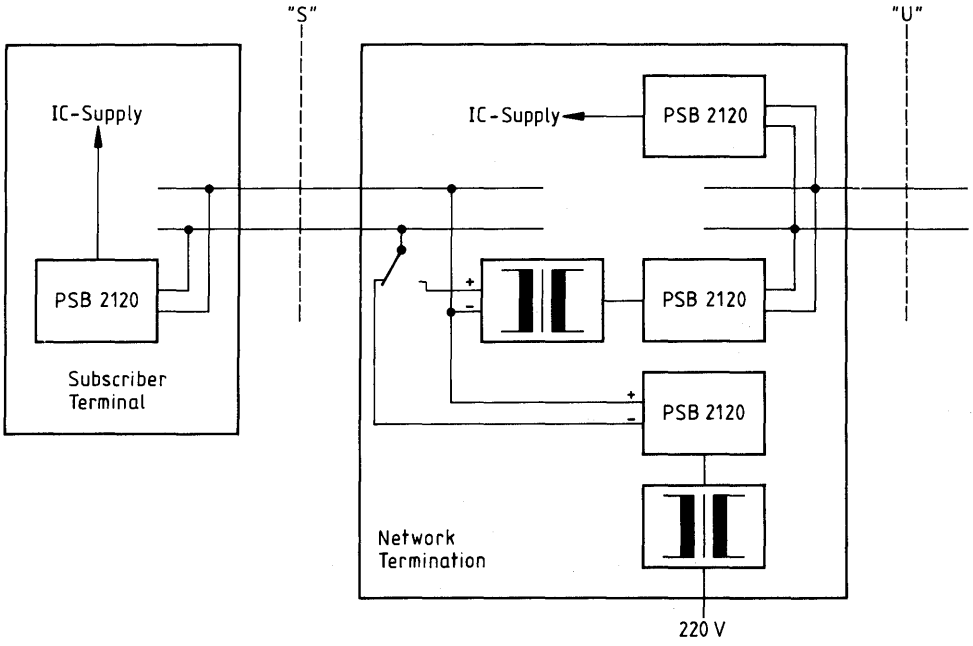


Figure 4
PSB 2120 Minimum Configuration

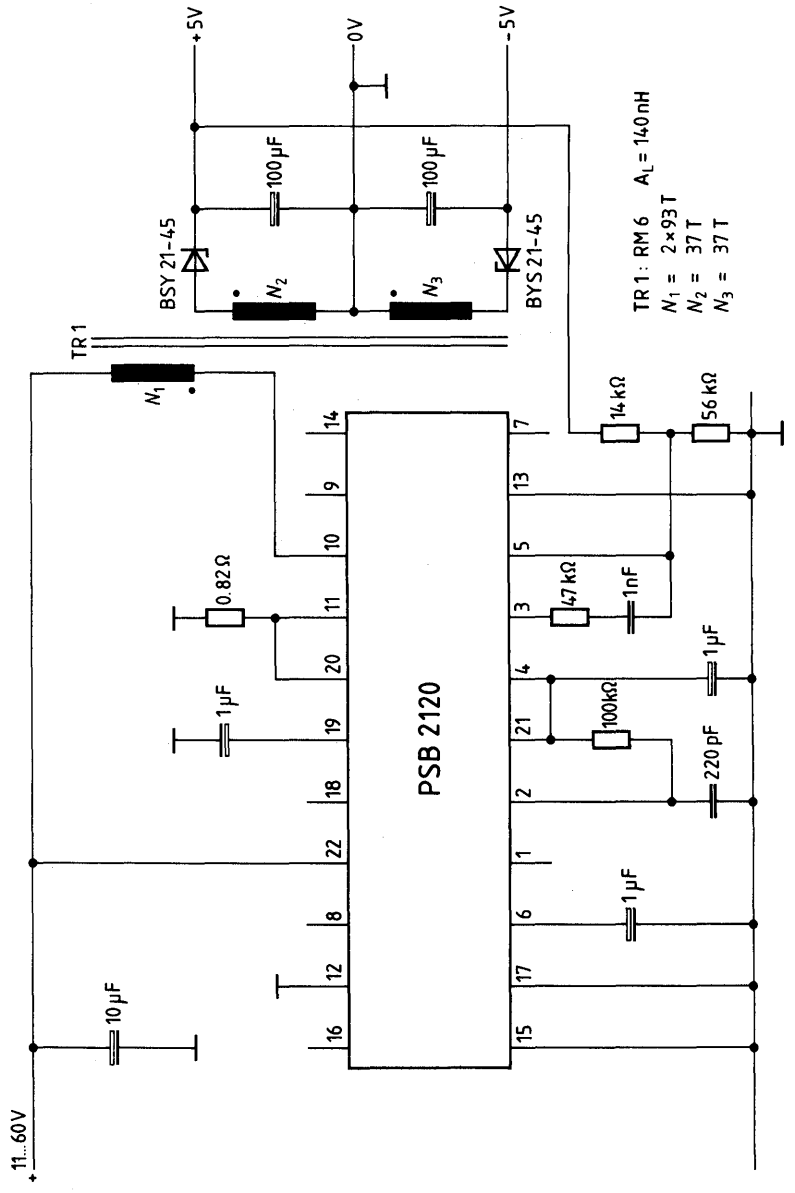


Figure 5

Advanced IRPC Application with Power Housekeeping and Polarity Reversal Detection

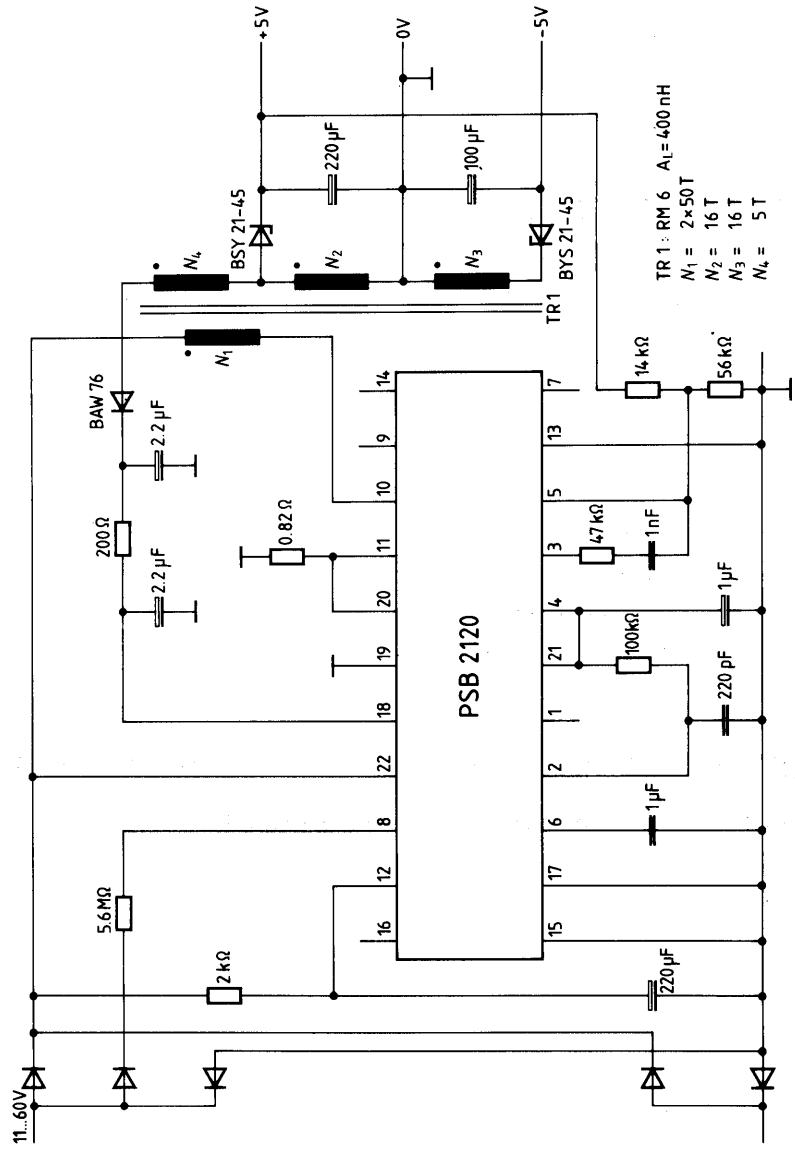


Figure 5 shows the primary start-up current limitation by connecting pin 12 (C_I)
To reduce chip power dissipation, an auxiliary winding of the transformer is used to switch off the internal linear CMOS supply (pin 18 V_{EXT}). Polarity reversal is detected by pin POL.

Figure 6
Generation of a µP Reset Signal with the PSB 2120

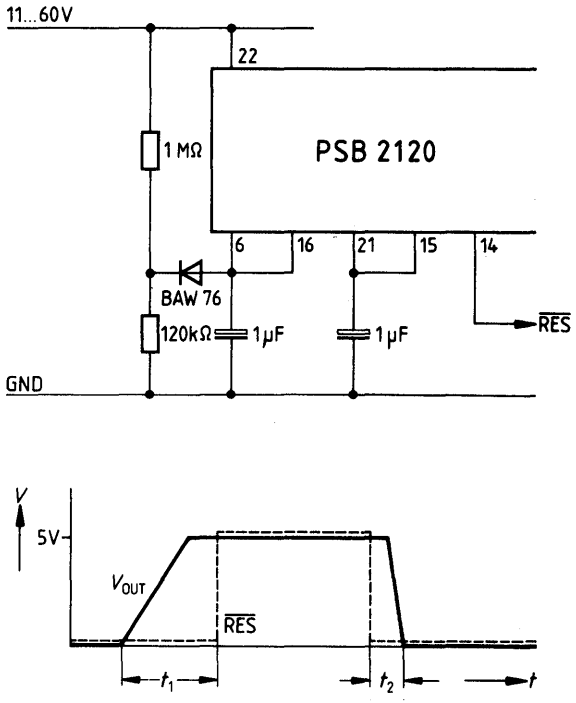


Figure 6 shows the realization of a microprocessor reset signal with the universal useable comparator of the IRPC.

Two galvanically isolated applications are shown in **figure 7** and **figure 8.**

Figure 7
PSB 2120 in Flyback Configuration with Transformer Isolation

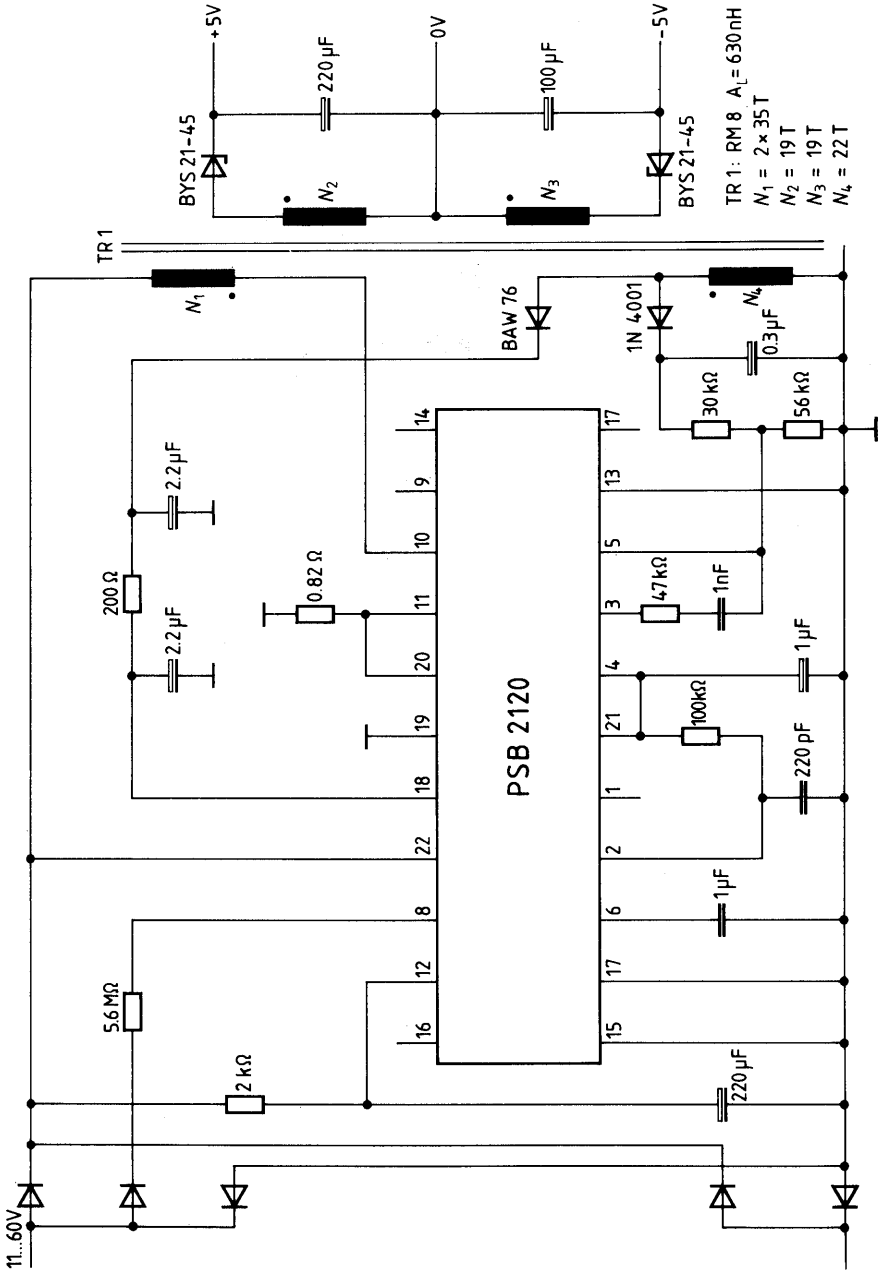
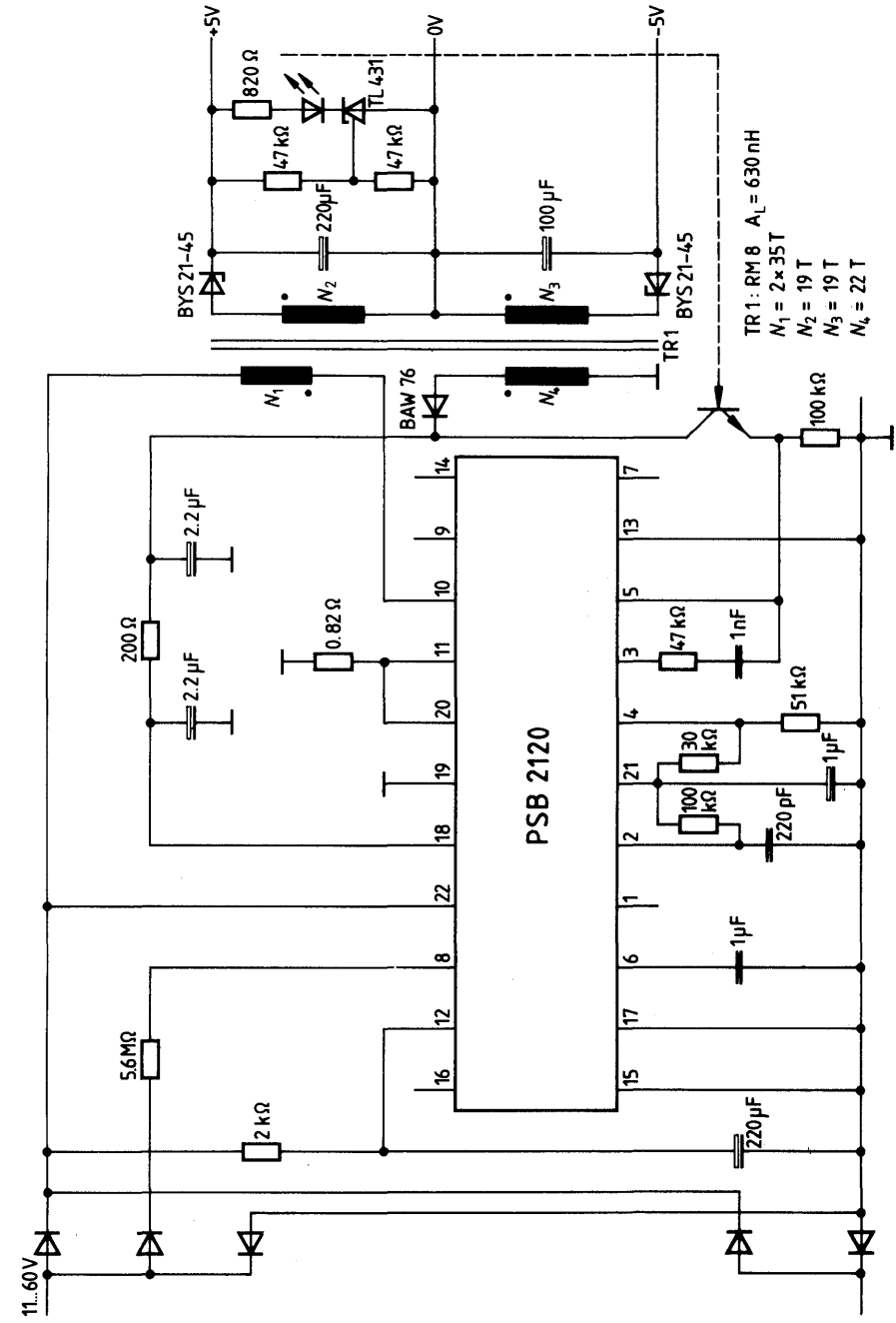


Figure 8
PSB 2120 in Flyback Configuration with Opto Isolation



Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Supply voltage V_S (pin 22) referred to GND	V_S	60	V
Analog/digital input voltage referred to GND (pins 2, 3, 4, 5, 7, 8, 13, 15, 16, 19, 20)	$V_{I\ A/D}$	6	V
Reference output current (pin 21)	$I_{O\ REF}$	−5	mA
V_{EXT} input Z-current	$I_{I\ Z}$	2	mA
V_{EXT} output current	I_O	−5	mA
SYNC output current (pin 1)	$I_{O\ SYNC}$	−5	mA
Driver output current (pin 9)	$I_{O\ DR}$	−5	mA
Ambient temperature under bias	T_A	−25 to 85	°C
Storage temperature	T_{stg}	−40 to 125	°C
Thermal resistance Junction – ambient	T_j	50	K/W

MOS-Handling

Pin 9 must be protected against voltages of ± 10 V. All other pins are protected against ESD.

DC Characteristics

$T_A = 0$ to 70 °C, $V_S = 11$ to 60 V

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Reference V_{REF} (pin 21) $T_j = 25$ °C						
Output voltage	$V_{REF\ O}$	3.92	4.0	4.08	V	$I_L = 0$ mA, $V_S = 40$ V
Line regulation	$V_{REF\ Line}$			60	mV	$V_S = 20$ to 60 V $I_L = 0$ mA
Load regulation	$V_{REF\ Load}$		20	40	mV	$I_L = 0.1$ to 0.3 mA $V_S = 40$ V
Temperature stability	$V_{REF\ TS}$		25		mV	over operating T_j
Load current	$I_{REF\ Load}$			0.5	mA	

DC Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Oscillator SYNC (pin 1), **RC** (pin 2) $f_{OSC} = 20$ kHz, $R_C = 39$ kΩ ± 1%, $C_T = 1$ nF ± 1%, $T_A = 25$ °C						
Initial accuracy			± 10		%	
Voltage stability			1	3	%	
Temperature stability			5		%	
Max. frequency	f_{max}	200			kHz	$R_C = 27$ kΩ $C_T = 39$ pF
H-sawtooth voltage	V_H		3.2		V	$V_S = 40$ V
L-sawtooth voltage	V_L		1.8		V	$V_S = 40$ V
H-sync output level	V_{OH}	2.4		5.25	V	$I_L = 0.5$ mA $V_{S\,EXT} \leq 6.3$ V
L-sync output level	V_{OL}		0.4	0.8	V	$I_L = 20$ µA
Error Amplifier **COMP** (pin 3), V_P (pin 4), V_N (pin 5)						
Input offset voltage	V_{IO}		3	10	mV	
Input current	I_I			10	nA	
Common mode range	V_C	1.8		4.5	V	
DC open loop gain	G_{VO}	60	70		dB	
Common mode rejection	k_{CMR}	60	70		dB	
Unit gain bandwidth	f		0.5		MHz	C_L (pin) 10 pF
Supply voltage rejection			70		dB	
H-output voltage	V_{OH}	4			V	$I_L = 100$ µA
L-output voltage	V_{OL}			1	V	$I_L = 10$ µA
Current Limit Comparator I_P (pin 20), I_N (pin 19) $T_A = 25$ °C						
Sense voltage	V_{Sense}	85	100	115	mV	$V_S = 40$ V
Input current	I_I			10	nA	
Input voltage range	V_I	0		1	V	
Reponse time to signal at GA (pin 9)	t_{Res}		1	2	µs	

DC Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Pulse Width Modulator						
Duty cycle	t_d	0		50	%	
Undervoltage Detection						
Start-up threshold	$V_{UV\ St}$	9	10	11	V	
Threshold hysteresis	$V_{UV\ Hy}$		0.3		V	
Soft Start C_{ss} (pin 6)						
C_T Charging Current	I_C	2	4	8	µA	
Output Driver G_A (pin 9) $T_j = 25\,°C$						
H-output voltage	V_{OH}	4.5			V	$I_{Source} = 5$ mA
H-output voltage	V_{OH}			$V_{S\ EXT}$	V	$I_{Source} = 0$ mA
L-output voltage	V_{OL}			0.4	V	$I_{Sink} = 5$ mA
Rise time	t_r		130	200	ns	$C_L = 220$ pF
Fall time	t_f		130	200	ns	$C_L = 220$ pF
Output current	I_O			5	mA	
External Supply V_{EXT} (pin 18)						
Output voltage	V_O		6		V	$I_{Source} = 1$ mA
Output current	I_O			2	mA	
Input voltage	V_I	6.0		7.5	V	
Z-current	I_Z			2	mA	
Enable Input $\overline{ENA}$ (pin 13)						
H-input voltage	V_{IH}	2.0		5.25	V	
L-input voltage	V_{IL}			0.8	V	
Response time to signal at G_A (pin 9)	t_{Res}		0.5	1	µs	$T_j = 25\,°C$
H-input current	I_{IH}		2.5		µA	

DC Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Comparator CN (pin 15), **CP** (pin 16), $T_j = 25\,°C$						
Input offset voltage	V_{IO}		3	10	mV	
Input bias current	I_I			10	nA	
Input voltage range	V_I	1.5		4.5	V	
Response time to signal at CO (pin 14)	t_{Res}		2.0	1	µs	
Short Circuit C_I (pin 12), $T_j = 25\,°C$						
Sense voltage	V_{Sense}	1	2	3	V	$(V_s\text{-}V_{CI})$
	$R_{DS\ (on)}$		3	4	Ω	
Polarity Detection POL (pin 8), **$\overline{\text{EME}}$** (pin 7)						
H-input voltage	V_{IH}	2.0		5.25	V	
L-input voltage	V_{IL}			0.8	V	
H-input current	I_{IH}		1	10	µA	
Response time to signal at $\overline{\text{EME}}$ (pin 7)	t_{RES}		0.2	1	µs	
Digital Outputs $\overline{\text{EME}}$ (pin 7), **CO** (pin 14) $I_{OUT} = 0.5$ mA						
H-output voltage	V_{OH}	2.4		5.25	V	$V_{S\ EXT} \leq 6.3$ V
L-input voltage	V_{IL}			0.4	V	
Power FET GA (pin 9), **DR** (pin 10), **SO** (pin 11)						
	V_{DS}			200	V	
	I_D			350	mA	
	$R_{DS\ (on)}$		6		Ω	
$t_{on} = t_{d(on)} + t_r$	$t_{d\ (on)}$ t_r		15 40		ns ns	
$t_{off} = t_{d(off)} + t_f$	$t_{d\ (off)}$ t_f		70 40		ns ns	
Leakage current	I_{Leak}			200	nA	$V_{DS} = 200$ V
Power consumption	P_{tot}		9	10	mA	$V_S = 40$ V $f_{OSC} = 20$ kHz $V_{S\ EXT} = 6.3$ V

SIEMENS

General Purpose Power Controller (GPPC) PSB 2121

Preminimary Data **CMOS IC**

Type	Ordering Code	Package
PSB 2121-P	Q67100-H8646	P-DIP-16
PSB 2121-T	Q67100-H6032	P-DSO-20 (SMD)

The PSB 2121 is a pulse width modulator circuit designed for fixed-frequency switching regulators with very low power consumption.

In telefony and ISDN systems a high conversion yield is crucial to maintain functionality in all supply conditions via "S" or "U" interfaces. The PSB 2121 design and technology realize high conversion efficiency and low power dissipation.

It should be recognized that the PSB 2121 can also be used in numerous DC/DC conversion systems other than ISDN power supplies.

The PSB 2121 Contains the Following Functional Blocks

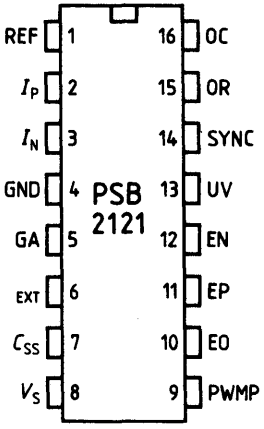
- Undervoltage lockout
- Temperature compensated voltage reference
- Sawtooth oscillator
- Error amplifier
- Pulse width modulator
- Digital current limiting
- Soft start
- Double pulse inhibit
- Power driver

Together with few external components it provides a stable 5 V DC supply for subscriber terminals (TEs) or network terminations (NTs). It can also be programmed for higher output voltages, e.g. to supply S-lines with 40 V.

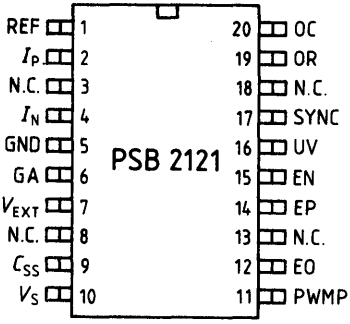
- Switched mode DC/DC-converter
- CCITT ISDN compatible
- Low power dissipation
- Supply voltage range 8 V to 70 V
- Programmable input undervoltage protection
- Programmable overcurrent protection
- Soft start
- Power housekeeping input
- Oscillator synchronization input/output
- High voltage CMOS technology 70 V

Pin Configurations
(top view)

P-DIP-16



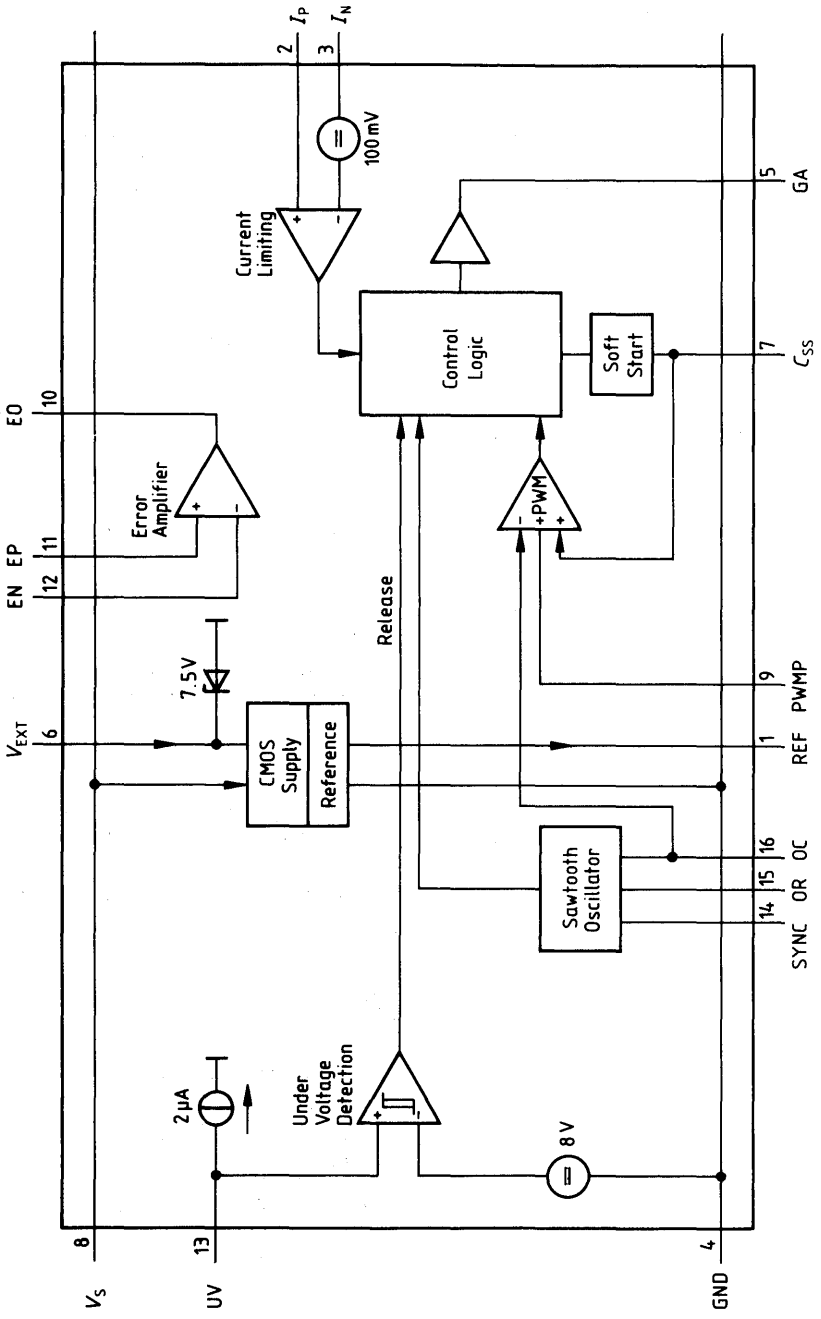
P-DSO-20



Pin Definitions and Functions

Pin No. P-DIP	Symbol	Input (I) Output (O)	Definition	Function
1	REF	O	Reference voltage	Output of the 4.0 V reference voltage.
2	I_P	I	Positive current sense	When the voltage difference between these two pins exceeds 100 mV, the digital current limiting becomes active.
3	I_N	I	Negative current sense	
4	GND	I	Ground	All analog and digital signals are referred to this pin.
5	GA	O	Gate	Totem-pole output driver, has to be connected with the gate of an external power switch.
6	V_{EXT}	I/O	External supply	Output of the internal CMOS supply. Via V_{EXT} the internal CMOS circuits can be supplied from an external DC-supply in order to reduce chip power dissipation.
7	C_{SS}	I	Soft start capacitor	The capacitor at this pin determines the soft start characteristic.
8	V_S	I	Supply voltage	V_S is the positive input voltage.
9	PWMP	I	Pulse width modulator	Non inverting input of the pulse width modulator.
10	EO	O		Error amplifier output.
11	EP	I	Positive voltage sense	Non inverting input of the error amplifier.
12	EN	I	Negative voltage sense	Inverting input of the error amplifier.
13	UV	I	Undervoltage detection	The undervoltage lockout can be programmed via UV.
14	SYNC	I/O	Synchronization	This pin can be used as an input for synchronization of the oscillator to an external frequency, or as an output to synchronize multiple devices.
15	OR	I	R-Oscillator	The external timing components of the ramp generator are attached to OR and OC.
16	OC	I	C-Oscillator	

Figure 1
GPPC Functional Diagram



Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Supply voltage (pin V_S) referred to GND	V_S	80	V
Analog input voltage (pins I_P, I_N, PWMP, EP, EN, SYNC, OR, OC) referred to GND	$V_{I\,A}$	6	V
Reference output current (pin REF)	$I_{O\,REF}$	−5	mA
SYNC output current (pin SYNC)	$I_{O\,SYNC}$	−5	mA
Error amplifier output current (pin EO)	$I_{O\,Amp}$	−5	mA
Z-current (pin V_{EXT})	$I_{Z\,EXT}$	2	mA
Output current (pin V_{EXT})	$I_{O\,EXT}$	−5	mA
Driver output current (pin GA)	$I_{D\,R}$	−5	mA
Ambient temperature under bias	T_A	−25 to 85	°C
Storage temperature	T_{stg}	−40 to 125	°C

DC Characteristics

$T_A = 0$ to 70 °C, $V_S = 8$ to 70 V

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Supply current	I_S		30		µA	$V_{S\,EXT} \geq 6.3$ V
Reference V_{REF}						
Output voltage	$V_{REF\,O}$	3.92	4.0	4.08	V	$T_j = 25$ °C, $I_L = 0$ mA, $V_S = 40$ V
Line regulation	$V_{REF\,Line}$			60	mV	$V_S = 20$ to 60 V $T_j = 25$ °C, $I_L = 0$ mA
Load regulation	$V_{REF\,Load}$		20	40	mV	$I_L = 0.1$ to 0.3 mA $V_S = 40$ V, $T_j = 25$ °C
Temperature stability	$V_{REF\,TS}$		25		mV	0...70 °C
Load current	$I_{REF\,Load}$			0.5	mA	

DC Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Oscillator/SYNC/OC						
$f_{OSC} = 20$ kHz, $R_C = 39$ kΩ ± 1%, $R_D = 0$ Ω, $C_r = 1$ nF ± 1%						
Initial accuracy $T_j = 25$ °C			± 10		%	
Voltage stability			1	3	%	
Temperature stability			5		%	
Max. frequency	f_{max}	200			kHz	$R_C = 27$ kΩ $C_r = 39$ pF
Sawtooth peak voltage	V_S		3.2		V	$V_S = 40$ V
Sawtooth valley voltage	V_S		1.8		V	$V_S = 40$ V
H-sync output level	$V_{SYNC\ H}$	2.4		5.25	V	$I_L = 0.5$ mA $V_{EXT} \leq 6.3$ V
L-sync output level	$V_{SYNC\ L}$		0.4	0.8	V	$I_L = 20$ µA
Error Amplifier/EO/EP/EN						
Input offset voltage	V_{IO}		3	10	mV	
Input current	I_I			10	nA	
Common mode range	CMR	1.8		4.5	V	
DC open loop gain	G_{VO}	60	70		dB	
Common mode rejection	k_{CMR}	60	70		dB	
Unity gain bandwidth	f		0.5		MHz	C_L (pin) ≤ 10 pF
Supply voltage rejection	k_{SVR}		70		dB	
H-output voltage	V_{OH}	4			V	$I_L = -100$ µA
L-output voltage	V_{OL}			1	V	$I_L = 10$ µA
Current Limit Comparator I_P/I_N,						
$T_j = 25$ °C						
Sense voltage	V_{Sense}	85	100	115	mV	$V_S = 40$ V
Input bias current	I_I			10	nA	
Input voltage range	V_I	0		1	V	
Response time (signal at GA)	t_{Res}		1	2	µs	

DC Characteristics (cont'd)

Parameter	Symbol	Limit Values			Unit	Test Conditions
		min.	typ.	max.		
Pulse Width Modulator						
Duty cycle	t_d	0		50	%	
Under Voltage Detection UV						
Start up threshold	V	7	8	9	V	pin UV = V_S
Threshold hysteresis	H_y		0.3		V	pin UV = V_S
Soft Start C_{SS}						
Charging current	C_T	2	4	8	µA	
Output Driver GA $T_j = 25\,°C$						
High output voltage	V_{OH}	4.5			V	$I_{Source} = 5$ mA
Low output voltage	V_{OL}			0.4	V	$I_{Sink} = 5$ mA
Rise time	t_r		130	200	ns	$C_L = 220$ pF
Fall time	t_f		130	200	ns	$C_L = 220$ pF
Output current	I_O			5	mA	
External Supply V_{EXT}						
Output voltage	V_O		6		V	$I_{Source} = 1$ mA
Output current	I_O			2	mA	
Input voltage	V_I	6.0		7.5	V	
Z-current	I_Z			2	mA	
Power Consumption	P_{tot}		5	6	mW	$V_S = 40$ V $f_{OSC} = 20$ kHz $V_{EXT} = 6.3$ V

Application Information

Undervoltage Lockout

The undervoltage lockout circuit protects the PSB 2121 and the power devices from inadequate supply voltage. If V_S is too low, the circuit disables this output driver. This ensures that all control functions have been stabilized in the proper state when the turn on voltage (8 V) is reached, and it prevents from the possibility of start up glitches. The undervoltage lockout is programmable by connecting a Z-diode between V_S and UV from 8 V up to 70 V. If UV is connected to V_S the default undervoltage lockout is 8 V.

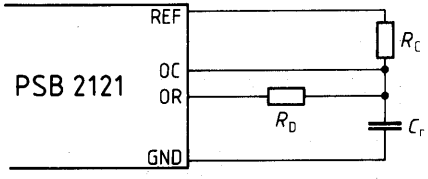
Voltage Reference

The reference regulator of the PSB 2121 is based on a temperature compensated bandgap. This circuitry is fully active at supply voltages above +6.0 V and provides up to 0.5 mA of load current to external circuitry at +4.0 V. This reference has to be buffered by an external capacitor > 0.5 µF.

Oscillator

The oscillator frequency is programmed by three components: R_C, C_r and R_D as shown in **figure 2**. The oscillator timing capacitor C_T is charged by V_{REF} through R_C and discharged by R_D. (R_D is series-connected with an internal 9 kΩ discharge-resistor). So the rise-time and the fall-time of the sawtooth oscillator can be programmed individually.

Figure 2



The PSB 2121 could be synchronized by the rising edge of the SYNC signal, whose frequency must be 10% higher than the free run frequency, determined by the RC-components. The SYNC pin can also be used as a trigger-output. As long as the capacitor of the sawtooth oscillator is discharged, SYNC is high. So multiple devices can be synchronized together by programming one master unit for the desired frequency.

Notice that the frequency of the output driver is half the oscillator frequency.

Soft Start Circuit

The soft start circuit protects the power transistors and rectifier diodes from high current surges during power supply turn-on. When the supply voltage is connected to the PSB 2121 the undervoltage lockout circuit holds the soft start capacitor voltage at zero. When the supply voltage reaches normal operating range an internal 4 µA current source will charge the external soft start capacitor. As the soft start voltage ramps up to +5 V, the duty cycle of the PWM linearly increases to whatever value regulation loop requires.

Pulse Width Modulator

The pulse width modulator compares the sawtooth-voltage of the oscillator output with the input signal at PWMP and with the voltage of the external soft start capacitor at C_{SS} **(see figure 1)**.

Error Amplifier

Conventional operational amplifier for closed-loop gain and phase compensation. Low output impedance: unity-gain stable.

Control Logic

The control logic inhibits double pulses during one duty cycle and limits the maximum duty cycle to 50%.

Current Limiting

A differential input comparator terminates individual output pulses each time when the sense voltage rises above threshold.

When sense voltage rises to 100 mA above threshold a shutdown signal is sent to the control logic.

CMOS Supply

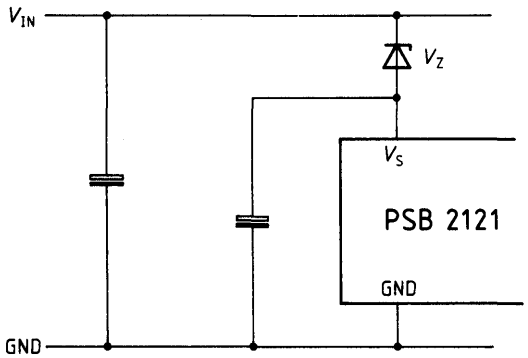
An integrated 6 V linear voltage regulator supplies the internal low-voltage CMOS circuits from the input voltage. This supply voltage is connected to pin V_{EXT} and has to be buffered by an external capacitor (C_{min} = 1 µF). Power dissipation of the linear voltage regulator can be reduced, if an external supply is used for that purpose by connecting it to pin V_{EXT}. If the input voltage at V_{EXT} reaches 6.3 V the internal linear voltage regulator turns off and the internal CMOS circuits are fed from the external voltage. In this case the input current at V_{EXT} is approx. 0.5 mA.

Note: An internal 7.5 V Z-diode protects the V_{EXT} input against overvoltage. The maximum Z-current is 2 mA! So if the external CMOS supply isn't stabilized the input current must be limited (e.g. by a resistor).

Extended Input Voltage Range

Some DC/DC-converter applications require a higher input voltage than the maximum supply voltage of the PSB 2121 which is limited to 70 V. **Figure 3** shows a method to extend the input voltage range by connecting a Z-diode between the input voltage and V_S of the PSB 2121.

Figure 3



If the PSB 2121 is fed via V_{EXT}, the input current at pin V_S is approx. 30 µA. The additional power losses are accordingly 30 µA · V_Z; the minimum input voltage is V_Z + 8 V.

Support Tools

Overview

This document is an introduction to the new **Siemens ISDN PC Development System.**

The system consists of:

- Modular hardware in the form of the **Siemens ISDN User Board (SIPB)**

  and of several software packages:

- **Mainboard Firmware (MF)** to drive the Siemens ISDN PC Board hardware
- Extensive user friendly **Menu Software** on PC
- **ISDN Operational Software (IOS)** including ready-to-use ISDN Layer-2 and Layer-3 protocols for the Link Access Procedure and Call Control functions according to CCITT standards.

The above hardware and software makes a PC look like a terminal capable of communicating with the outside world via a voice/data ISDN network.

Finally, the

- **Siemens ISDN Software Development and Evaluation System (SIDES)** contains all the tools for the customer to develop and test new protocol software using a high-level language based on CITT's Functional Specification and Description Language (SDL, CCITT Z. 100 Series).

In short, the use of the Siemens hardware and software tools provides significant savings in R & D time when designing a customer specific ISDN application.

The following first section of this overview document gives the scope of applications of the ISDN software tools.

1 Introduction

1.1 Design Challenges in ISDN System Development

Designing an ISDN application is a time-consuming task in terms of hardware and software development and testing. Proper tools can provide significant reductions in R & D costs.

Some of the challenges that engineer implementing an ISDN application has to face are as follows:

A) Design of Hardware
A stable hardware environment is an absolute requirement to start developing any ISDN communication application. Meaningful testing of hardware is often possible only with a dedicated development system.

B) Creation of Firmware
The testing of firmware (including device drivers and interrupt handlers) is complicated by the fact that firmware is, by definition, real-time. Dynamic hardware errors are difficult to distinguish from errors in the firmware. An emulator often is necessary to detect, analyze, and correct these errors.

C) Creation of a Software Development Environment
The entire development environment should ideally be inexpensive, for instance a PC, for which compilers, editors and other tools are widely available.

D) Protocol Modifications
Without additional tools, the smallest change in the initial protocol often entails time-consuming coding and verification. All modifications should be automatically documented.

E) Static and Dynamic Testing
Initial static and dynamic testing of the software should be possible independent of the hardware, but without the need of an expensive emulator.

1.2 The Siemens ISDN PC Development System

The new Siemens ISDN PC Board and the associated software packages have been created to considerably simplify the implementation of such highly complex and wide-ranging tasks. To this end, the **Siemens ISDN PC Development System** offers the user:

- A flexible, modular hardware architecture with options that cover virtually all ISDN applications, based on the advanced Siemens **ISDN Oriented Modular (IOM®)** architecture.
- Comprehensive software according to the **Open Systems Interconnection (OSI)** layered model.
- Clear interface between the protocol software modules and the outside world.
- Complete programm generation tools that enable the user to create his own protocol software using a high-level SDL-like description language.
- An advanced testing concept which allows software test on the PC before running it on the target ISDN hardware.

1.3 What a Customer Needs

All the customer needs to provide to use the Siemens ISDN PC Development System is:

- an IBM PC XT/AT or compatible including:
- 512 Kbyte of RAM
- harddisk drive and diskette unit
- Microsoft© C-compiler V4.0 or upwards.

Siemens provides the necessary ISDN hardware and the various software packages according to the particular needs and applications of the customer. The software is available on 5¼" diskettes (double sided double density).

1.4 Summary of the Hardware and Software Packages

Hardware is provided in the form of a modular **Siemens ISDN PC User Board (SIPB)** which can be configured:

- as an **ISDN Voice/Data Terminal (TE)**
- as an **ISDN Network Termination Simulator (NT-S)**
- or as an **ISDN Line Card (LC)** in a **Telephone Switching System.**

The SIPB is accompanied by resident **Mainboard Firmware (MF)** which includes the necessary device drivers, memory management and interrupt handlers for the ISDN hardware.

Extensive **Menu Software (MS)** allows the customer to program the ISDN components directly from a PC.

Off-the-shelf protocol software is available in different packages known under the generic name of **ISDN Operational Software (IOS).** This software includes:

- data link layer for the ISDN user-network interface, in other words, the Layer-2 Link Acces Procedure on the D channel (LAPD)
- Layer-3 generic call control software, executing the basic voice and data service call control procedures
- switch specific call control software.

Although the IOS is essentially hardware independent, the highest possible efficiency can be reached with the Siemens ISDN components based on the IOM architecture.

Finally, a comprehensive set of software tools is provided in the form of the **Siemens ISDN Software Development and Evaluation System (SIDES)** that runs on a PC.

SIDES consists of:

- the **Program Coding Tools (PCT),** and
- the **Siemens ISDN Protocol Software Test Tools (SITEST).**

The PCT's enable the user to create complex protocol software for Layer 2 and Layer 3 of the OSI communications model in a simple fashion. Thus, they allow:

- to define the protocol using a language similar to SDL
- to create object coede by applying only a few generators and a standard C compiler
- to create on line and hardcopy documentation.

SITEST is an efficient software package for verifying the operation of protocol software before it is downloaded on customer specific communication hardware. The package consists of:

- A **Static Test Tool for Protocol Software (STEP).**
  This tool runs on a PC independent of any other hardware to provide a single step test of the protocol.

- A **Dynamic Real-Time Communication Tester (DYRECT).**
  This programm on a PC allows to verify the dynamic of the protocol software in association with the firmware and a peer station.

In conclusion, with the new ISDN PC Development System Siemens offers the customer the same flexibility as known from the ISDN IOM concept:

- **A modular ISDN PC Board**
- **Off-the-shelf ISDN Protocol Software with clear interfaces**
- **A complete set of ISDN Software Development Tools.**

In **chapter 2** of this overview document you will find a description of the SIPB hardware. The firmware and the ready-to-use ISDN Operational Software and Menu Software are explained in **chapter 3**. In **chapter 4** a general step-by step strategy is outlined for developing user specific protocol software using the SIDES. A list of manuals provided on the hardware and software is given at the end of the document.

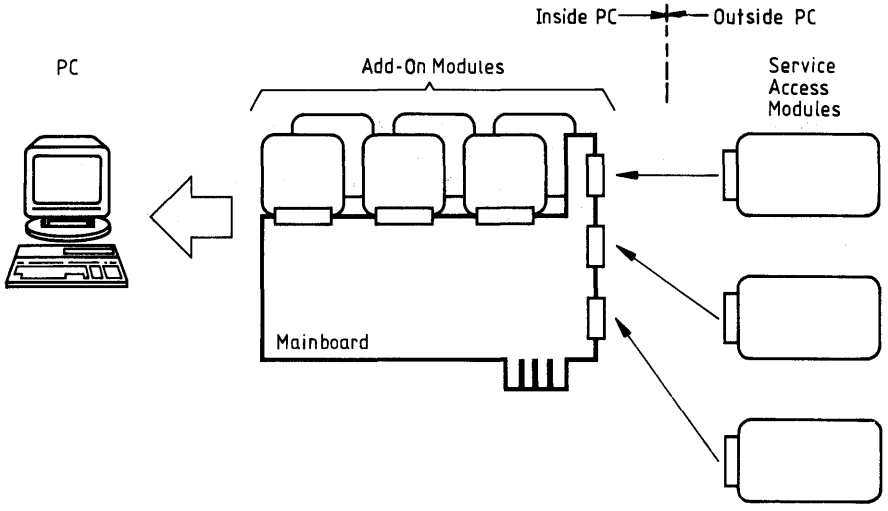
2 Hardware Description

The heart of the **Siemens ISDN PC Board (SIPB)** is a mainboard designed to fit in a full-sized card slot of a personal computer IBM XT/AT. The board includes a complete microcomputer system with:

- an SAB 80188 microprocessor
- a 128 Kbyte (optional 64 Kbyte) EPROM which contains the **Mainboard Firmware**
- 256 Kbyte of RAM to which **ISDN Operational Software** from the PC is down – loaded
- PC bus interface with a dual port RAM and DMA capability.
  This interface allows the PC application software to control the SIPB.

As shown in **figure 1,** six connectors are provided for daughter boards. These contain the Siemens VLSI circuits of the **ISDN Oriented Modular (IOM)** family to fulfill different user specific ISDN applications.

Figure 1
Siemens ISDN PC Board



Add-On Modules

All daughter boards that need direct microprocessor control have to be plugged into a 96-pin **Add-On Module** connector.

Such add-on modules contain an EPROM. This EPROM can be read by the microprocessor to identify the hardware of the add-on module.

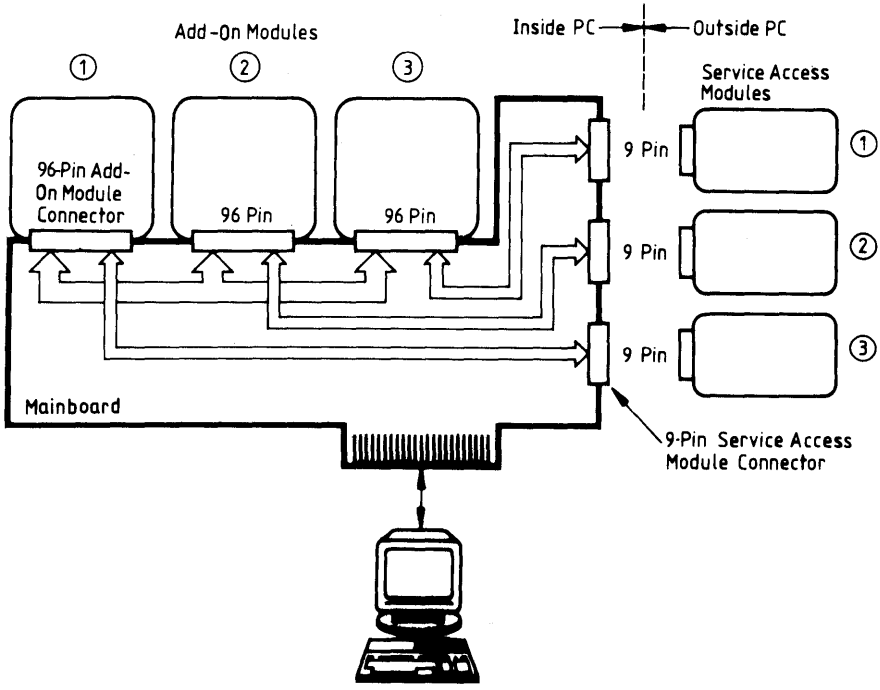
E.g. layer-2, or audio interface add-on module.

Universal Service Access Modules

Daughter boards that do not require microprocessor control but are controlled by an add-on module via a serial port are called **Service Access Modules**. A service access module is a module which can be connected to a 9 pin service access slot corresponding to the controlling add-on module slot. There is a one-to-one correspondence between add-on module slots and service access module slots **(see figure 2)**.

Universal service access modules can also be plugged into an add-on slot if the user so desires, because they have additionally a 96 pin connector. In this case the position of the daughter boards in the add-on slots is not critical.

Figure 2

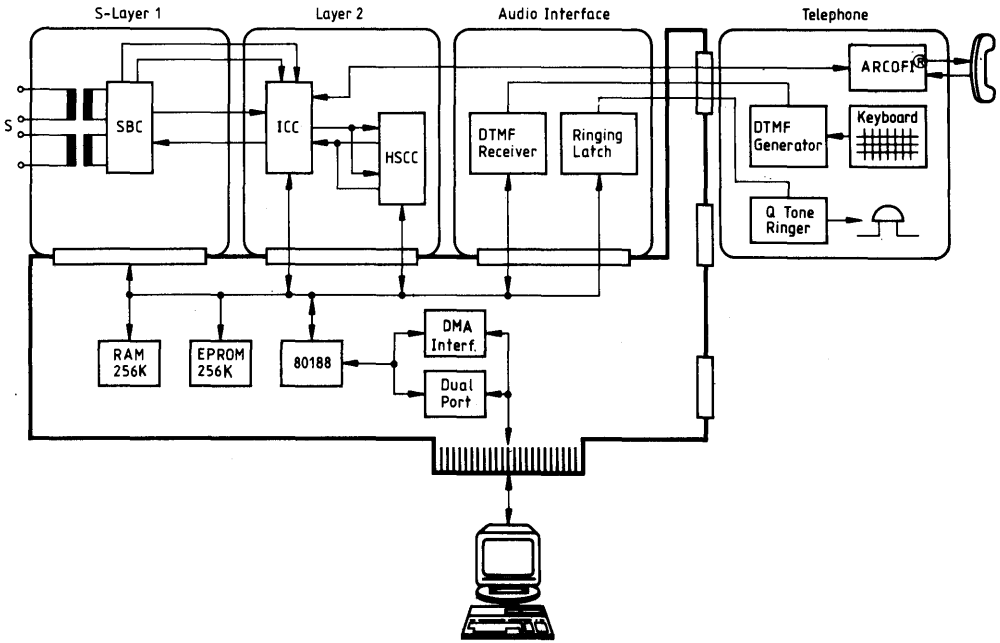


Special Service Access Modules

These **Service Access Modules** can only reside outside the PC, because of their size or the fact that they have only a 9-pin access connector. E.g. telephone module, or primary rate line interface module.

An example of the SIPB in a terminal application is shown in **figure 3**. The board is configured as an ISDN TE connected to the basic access S bus via the layer-1 S bus service access module. A layer-2 module contains an ISDN communication controller (ICC: PEB 2070) which offers the access to the ISDN signaling channel (D channel). The module also contains a High Level Serial Communication Controller (HSCC: SAB 82520) which may be used as a source/sink for data in one or both of the ISDN circuit-switched B channels. The audio interface module contains the circuitry to interface the telephone into the SIPB architecture. The telephone module contains the PSB 2160 Audio Ringing Codec Filter (ARCOFI) to perform the A/D conversion, compensation filtering and ringing functions. It also contains a DTMF generator to transfer the keypad information to the audio interface module where it is decoded for microprocessor access.

Figure 3
SIPB in a Voice/Data Terminal



Through the modularity of design, the ISDN PC Board offers the user flexibility inherent in the IOM concept.

Kits of hardware and software are available for commonly used ISDN applications such as:

- an ISDN Voice/Data Terminal for the S Basic Access
- an ISDN Voice/Data Terminal for the two-wire (U) subscriber loop (using echo cancellation)
- an ISDN Voice/Data Terminal for the two-wire (U*) subscriber loop (using time compression multiplexing)
- an ISDN Network Termination Simulator (NT-S) for the S interface
- an ISDN Line Card for Basic (S, U or U*) or Primary Access (1544 kbit/s S1/T1 or 2048 kbit/s S2/CEPT interface).

3 Software Description

The following software packages are available to support the ISDN PC Board hardware:

- **Object Code:**
  - the Mainboard Firmware (MF) resident on SIPB
  - the ISDN Operational Software (IOS) executed on the PC or downloaded and executed on the SIPB hardware
  - the Menu Software (MS) executed on PC.

  These are briefly discussed in this chapter.

- **Tools** which run on a PC namely
  - the Siemens ISDN Software Development and Evaluation System (SIDES).

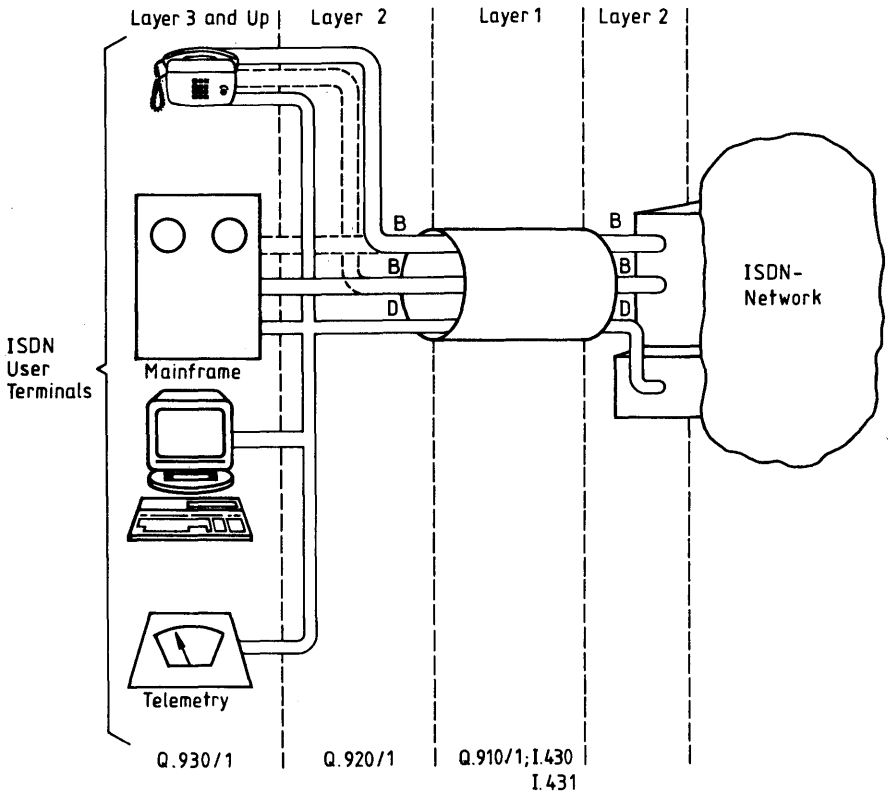
The use of these tools is explained in **chapter 4**, where a general step-by step development strategy is outlined for the design and testing of user specific ISDN protocol software.

3.1 Access to ISDN and Layered Protocol Architecture

The User Access to the ISDN consists of:

- a number of 64 kbit/s bearer channels **(n x B)**
  e.g. n = 2 for basic rate ISDN access
  n = 30 or 23 for primary rate ISDN access;
- and a signaling channel (D), either 16 (basic rate) or 64 (primary rate) kbit/s **(see figure 4).**

Figure 4



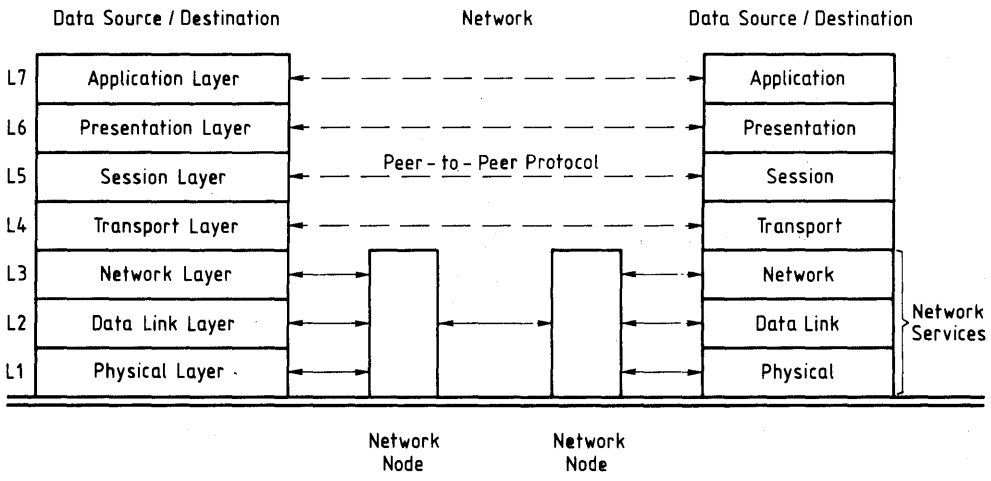
The B channels are used for end-to-end circuit switched digital connections between communicating stations. The D channel is used for transferring signaling information via CCITT (Q series) and switch specific signaling protocols.

These protocols can be viewed in terms of the Open Systems Interconnection (OSI) model of the International Standards Organisation, as shown in **figure 5**.

The three lowest layers of the OSI model are the services provided by the network (in this case, the ISDN) for the transfer of information between the end user systems.

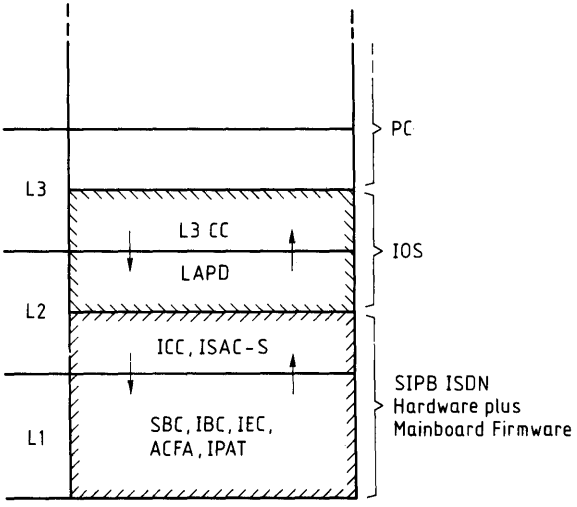
- Each layer communicates with a peer layer via a **Peer-to-Peer Protocol** transmitted over the physical link (L1).
- Each layer interfaces only with the layer immediately above and immediately below it via a Service Access Point, e.g. L1↔L2↔L3.
- The communication between two adjacent layers is done by the use of a set of **Service Primitives**, e.g. DL-EST-RQ data link establish request (L3→L2) and DL-EST-IN data link establish indication (L2→L3).

Figure 5
Layered ISDN Protocol Structure according to the Open Systems Interconnection Model



The relationship of the Siemens ISDN PC Board and the associated software to the layered communication model is depicted in **figure 6**.

Figure 6



L3 CC = Layer-3 Call Control
LAPD = Link Access Procedure for the D channel
ICC = ISDN Communication Controller PEB 2070
ISAC™-S = ISDN Subscriber Access Controller for the S interface PEB 2085
SBC = S Bus Interface Circuit PEB 2080
IBC = ISDN Burst Transceiver Circuit PEB 2095
IEC = ISDN Echo Cancellation Circuit PEB 2090
ACFA = Advanced CMOS Frame Aligner PEB 2035
IPAT™ = ISDN Primary Access Transceiver PEB 2235

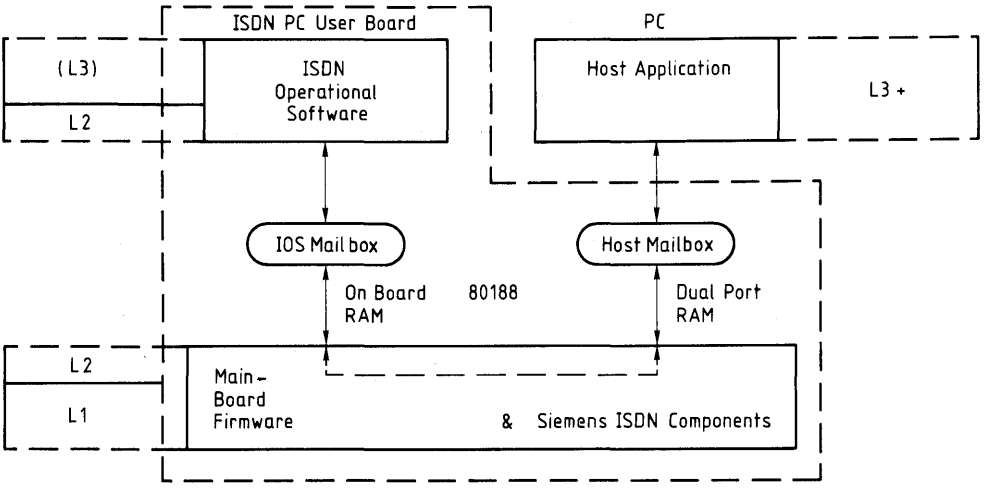
The advanced Siemens ISDN devices offer the PC the physical access to the B and D channels, e.g. the S Bus Interface Circuit (SBC: PEB 2080) or the ISDN Primary Access Transceiver (IPAT: PEB 2235) and the Advanced CMOS Frame Aligner (ACFA: PEB 2035). As shown in **figure 6** part of the layer 2 is handled by the hardware. Specifically, the ISDN Communication Controller (ICC:PEB 2070) and the ISDN Subscriber Access Controller (ISAC-S: PEB 2085) offer efficient support for the handling of the link access protocol (auto-mode).

The Mainboard Firmware (MF) provides the functions necessary to drive the user specific hardware on the board.

The ISDN Operational Software (IOS) implements the layer-2 Link Access Protocol for the D channel (LAPD) and the layer-3 call control functions. It can be run either on the PC or downloaded and run on the SIPB 5000.

Figure 7 shows in the general SIPB structure.
Messages are transferred between the mainboard firmware and the IOS via a 16 byte mailbox. 8 bytes are used for commands from the IOS to the MF and 8 bytes for responses from the MF to the IOS.
When the IOS is running on the PC, the host mailbox is used for the commands/responsed to the mainboard firmware. When running on the SIPB 5000, the IOS mailbox is used for the commands/responses to the MF and the host mailbox is used for controlling functions, such as execution start/stop or upper layer services running on the PC.

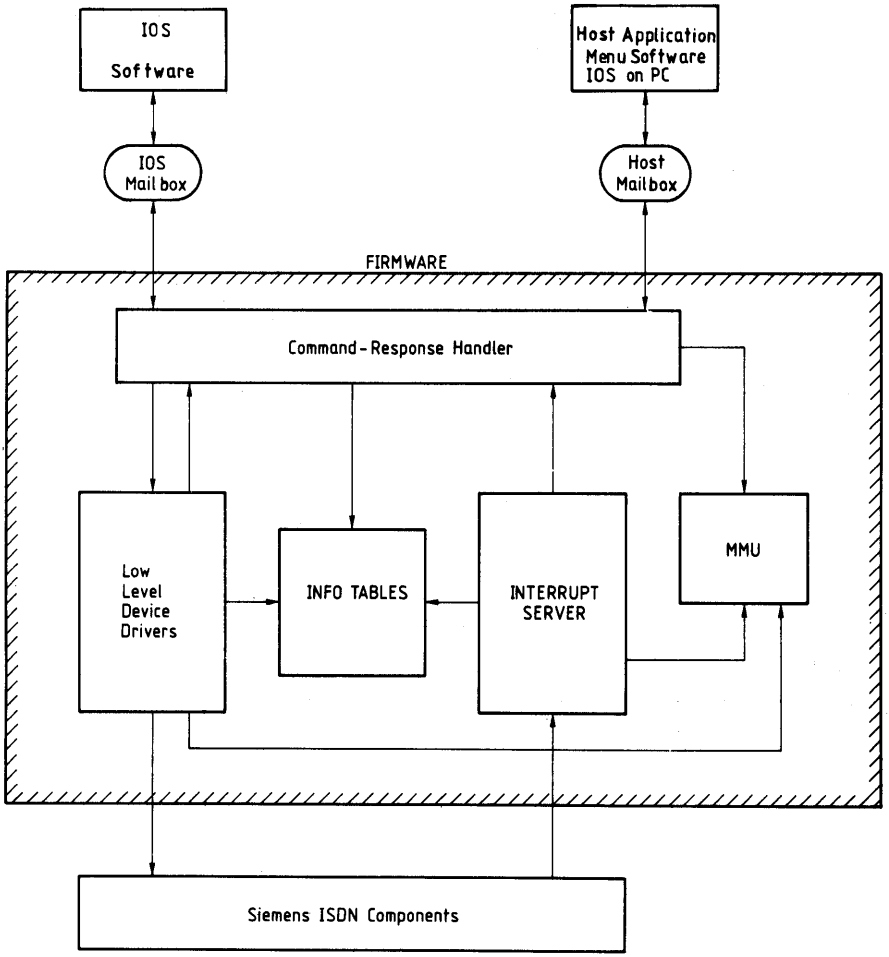
Figure 7
General SIPB Software Structure



3.2 Mainboard Firmware

The firmware is contained in a part of a 128 Kbyte (or 64 Kbyte) EPROM on the SIPB 5000 mainboard. It includes an interrupt handler with dedicated interrupt service routines, a memory management for data, drivers for the Siemens ISDN devices and information tables to keep track of the hardware configuration. In addition, a command/response handler forms the interface to the PC and IOS command/response mailboxes. These serve as a communication interface between the firmware and the application software on PC, and between the firmware and the downloaded protocol software (IOS), making the IOS independent of the hardware. Refer to **figure 8**.

Figure 8
Mainboard Firmware Architecture



3.3 ISDN Operational Software (IOS)

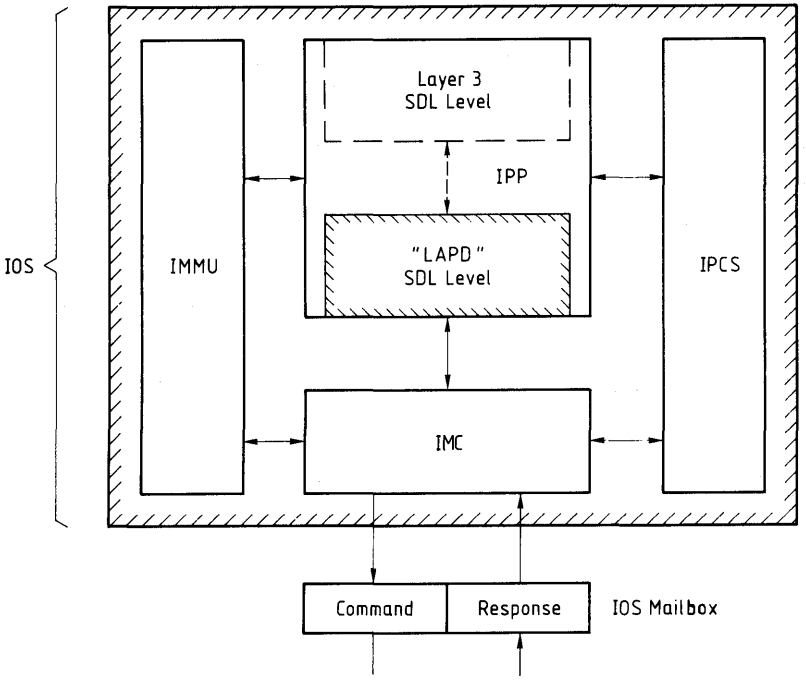
The **ISDN Operational Software (IOS)** contains:

- a complete protocol software for the Link Access Procedure in the D channel LAPD according to CCITT and the switch specific requirements
- and, optionally, Layer-3 Basic Voice and Data Service Call Control Software according to CCITT and the Switch Specific Requirements (SIEMENS EWSD, AT & T 5ESS . . .).

The portability is ensured by a clear interface to layer 1 (and to the layers above IOS) via service primitives that are transferred via the IOS mailbox **(figure 7)**.

The IOS has a highly modular structure. As shown in **figure 9,** it consists of four blocks:

Figure 9
General IOS Architecture



- **IOS Protocol Part (IPP)** with layer 2 and layer 3

  The layer 2 is composed of five subblocks (called processes):

  - The **Multiple Frame Control (MFC)** process is responsible for acknowledged information transfer according to the 'Multiple Frame Operation' specified in the CCITT recommendations
  - The **Unacknowledged Information Transfer Control (UTC)** process for handling the transfer of unnumbered information (UI) frames in case of link establishment from network side (SETUP UI – Frame)
  - The **TEI Assign Control (TAC)** process responsible for the automatic or non-automatic terminal endpoint identifier value assignment
  - The **Physical Link Control (PLC)** responsible for the supervision and control of layer 1
  - The **Error Control (ERC)** process to support user programming for error processing and statistical functions.

  Similary, the layer 3 consists of four processes:

  - **Call Controll (CC1)** process to execute call control transaction with the exchange (switch specific) and interpret message types of the layer-3 call control frames
  - **Layer-3 Management (L3M)** process
  - **Terminal 1 (TM1)** process which supervises and controls the state of the terminal
  - **Layer-3 Error Control (L3-ERC)** process.

- **IOS Mailbox Control (IMC)** block which builds the general interface of the IOS to the outside environment

- **IOS Memory Management Unit (IMMU)** is responsible of memory allocation and de-allocation within the IOS

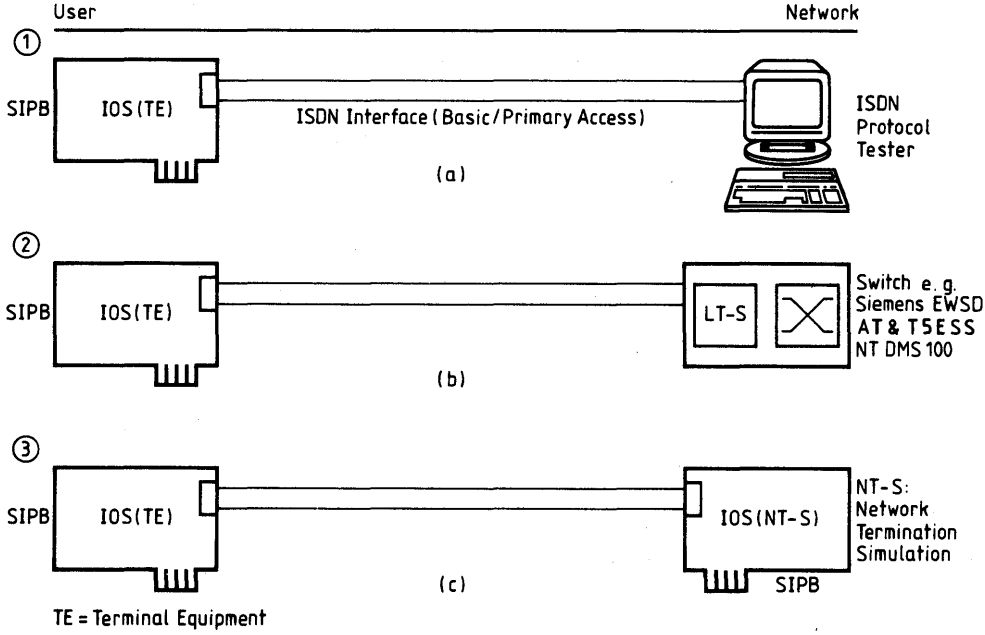
- **IOS Process Control System (IPCS)** controls all processing within IOS through a task scheduler and a task queue.

The IOS is written in C language and is available in different packages:

- Full layer 2 for **Terminal Equipment (TE)**
- Full layer 2 plus layer 3 **Basic Voice and Data Service (TE)** call control software (e.g. for interaction with Siemens, AT & T, or Northern Telecom switches).
- **Network Termination Simulator (NT-S)**
  Software for layers 2 and 3 corresponding to the TE packages.

The scope of the IOS is summarized in **figure 10**. The NT-S version of the IOS provides a user with a tool test **user defined** layer-2 and layer-3 software by setting up a voice/data link between two ISDN PC Boards, as shown in **figure 10c**. For more details, refer to **chapter 4.**

Figure 10
Scope of Application of the IOS



3.4 ISDN Menu Software (MS)

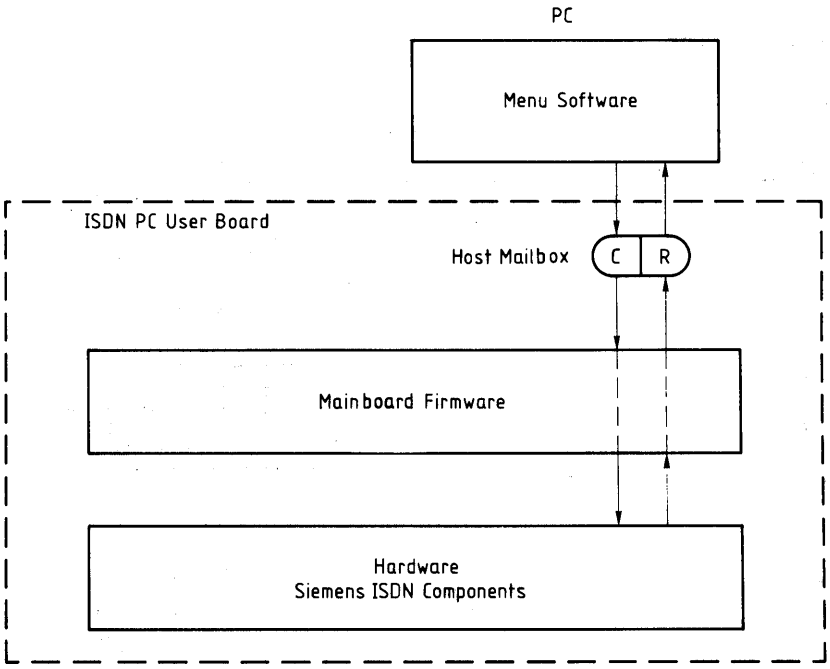
The **ISDN Menu Software (MS)** is a user-friendly software package that enables the user to program and evaluate the Siemens devices on the user board. In order to run the menu software, the customer needs a SIPB 5000 plus the applicable modules.

The interface to the user is window-driven. Help functions can be called for information on the hardware so that a novice can quickly get acquainted with the functions of the registers on the hardware modules, and test them. No special boot-up procedure is required for the different configurations as the firmware determines the hardware configuration at power-up and the menu software adjusts accordingly.

The menu software communicates with the firmware via the host mailbox **(see figure 11)**.

To guide the user, a list of current instruction options constantly appears on the bottom line.

Figure 11



Track files of all user register accesses are created, which can be saved and edited (if required) using the track window or a standard text editor, and re-run later.

These and other advanced features make the menu software an indispensable tool for anyone wishing to save time when evaluating, programming, and debugging ISDN hardware.

Because the menu software obtains the register information from the firmware this package will support both current and future Siemens devices.

4 Siemens ISDN Software Development and Evaluation System (SIDES)

Based on the general IOS architecture, a user is able to design his own ISDN protocol software by following the development steps listed below:

⓪ protocol description (4.1)

① static testing (4.2)

② dynamic testing (4.3)

③ downloading on user hardware (4.4)

④ final testing in real environment

The **Siemens ISDN Software Development and Evaluation System (SIDES),** described in the following sections, will accelerate the implementation of software.

4.1 Protocol Development Using the Program Coding Tools (PCT)

The general idea of the **Program Coding Tools (PCT)** is to allow the user to specify a protocol in a simple form similar to the CCITT functional **Specification** and **Description Language (SDL)**. This can be done on an IBM PC (AT, XT or compatible) with any standard text editor, as illustrated in **figure 12.**

It is important to take a structured approach when designing ISDN protocol software.

In such an approach the protocol is described as a combination of interacting **processes**. This approach is taken further in that each process is described as a combination of **states**.

Transitions can be defined between the states. Finally **messages** are used for communication between the processes. The PCT implementation of protocol software is based on the use of a specially tailored task scheduler and message passing system (namely, the **IOS Process Control System IPCS**, cf. **section 3.3**) which renders the processes independent of one another, testable and easily modifiable.

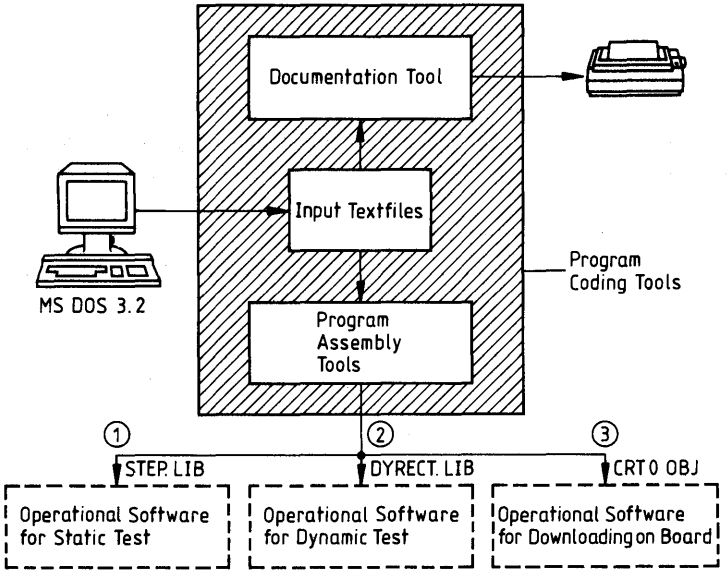
The above protocol description elements are entered by the protocol designer in the form of text files with a simple syntax. The text input files (one per process) are then automatically translated by the PCTs into 'C' source code files.

For documentation and debugging purposes an additional graphic tool generates SDL drawings in a format compatible with Ventura Publisher® and AutoCAD®. They enable the user to verify immediately that the protocol behaves as it was intended to do.

The files can be linked together with object files **(figure 12)**, which results in executable code for the purpose of:

- static test of the protocol behaviour on PC (IOS with STEP.LIB)
- dynamic test of the protocol behaviour on PC (IOS with DYRECT.LIB)
- downloading and execution on Siemens ISDN PC user board (IOS linked with CRT0.OBJ).

Figure 12

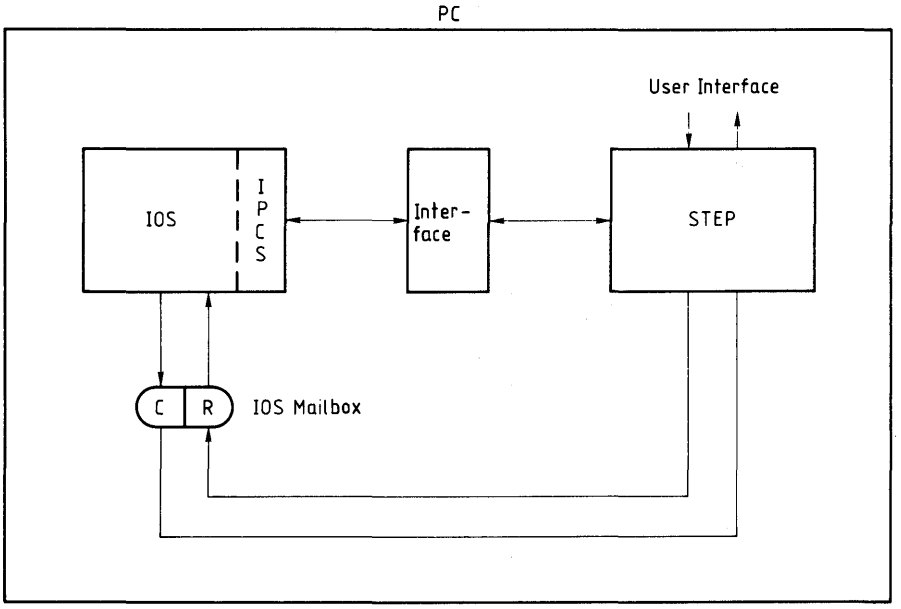


4.2 Static Test Using the Static Test Tool for Protocol Software (STEP)

The **Static Test Tool** allows to test complete protocol behaviour in single step mode independent of any ISDN hardware.

The user's test interface communicates with the IOS over the IOS mailbox **(figure 13**, in this case in PC-RAM).

Figure 13
Static Protocol Test on PC



Thus, the user is able to send stimuli to the IOS (service primitives from the layer above **or** below IOS) via the STEP user interface and check if the IOS reacts as expected. If not, the user may examine the current states of the processes or the contents of the IOS task queue in IPCS via an additional interface.

All interactions through the IOS mailbox are recorded in an 'Echo' and a 'Logging' file. After the user has modified his protocol using the PCT, he may re-run the same test using the 'Echo' file. 'Echo' and 'Logging' files are in standard ASCII format.

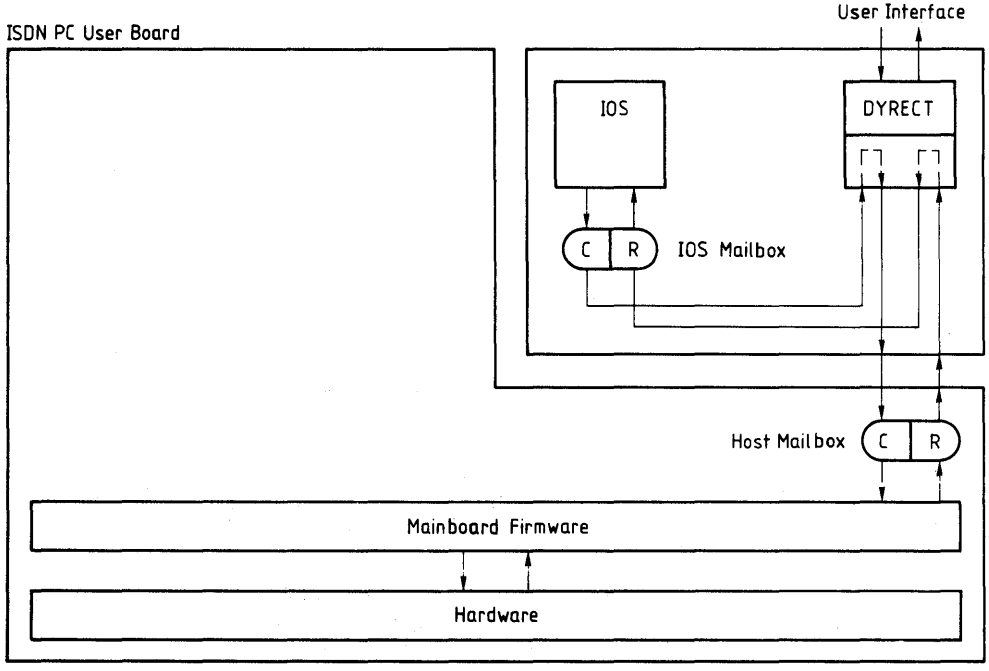
4.3 Dynamic Test Using the Dynamic Real-Time Communication Tester (DYRECT)

In the next step the same protocol can be combined with a test environment which allows to run the IOS inside the PC and use in real-time the functions of the ISDN PC Board via the host mailbox **(figure 14)**. As in the static case, the user is able to send stimuli (such as layer-3-to-layer-2 commands if layer 3 is not included in IOS) to the IOS via the mailbox.

All interactions via the host mailbox are visible on screen (if desired). All the details, including time stamps, are stored in a file and can be examined afterwards with a special screening tool (Screening Tool for Report files, STORY).

This test facility gives the opportunity to test the software in a real system environment (e.g. switch, or a network termination simulator with IOS available from Siemens, cf. **section 3.3**) by examining the debugging information contained in the report file. As a result, in most cases an expensive protocol analyzer is not necessary.

Figure 14
Dynamic Protocol Test on PC



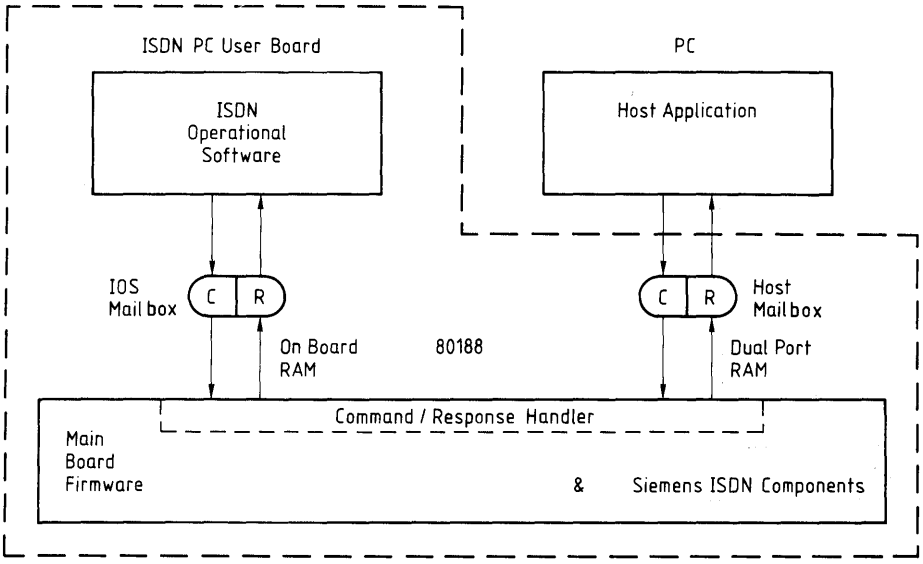
4.4 Downloaded IOS on SIPB

In this case, both the IOS mailbox and the host mailbox are located on the SIPB **(figure 15)**.

Again, the host mailbox serves as the interface between the higher layers ('Host Application') and the IOS protocol layer. The execution of the downloaded IOS is started and controlled by primitives (e.g. suspend, continue . . .) sent from the PC via the host mailbox. These primitives are recognized and delivered to the IOS by the C/R handler in the firmware.

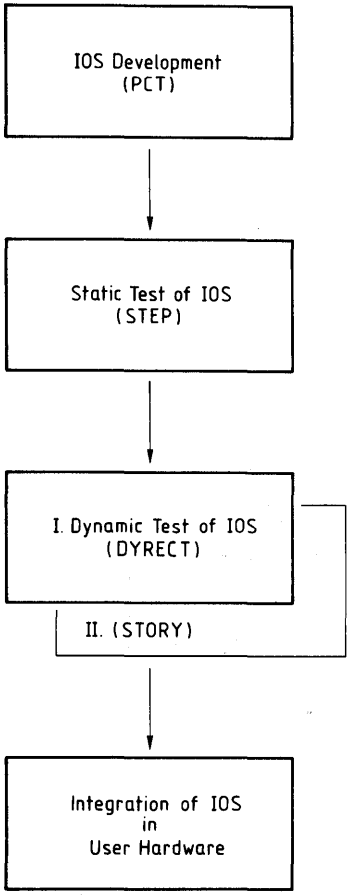
The downloaded ISDN operational software can be tested by using an SIPB 5000 with a specially tailored NT-S version of IOS as counterpart as well as with a protocol analyzer (e.g. Siemens K1195) and, finally, against an ISDN switching network.

Figure 15
Communication between IOS, Firmware and PC



The Siemens ISDN Software Development and Evaluation System (SIDES is not only a consistent set of tools, but represents a complete methodology for the implementation of ISDN protocol software (figure 16). Use of SIDES considerably reduces software design cycles. As a consequence, it entails a major reduction (up to 80 %) in overall R & D costs.

Figure 16
Development Strategy for ISDN Operational Software



5 Hard- and Software Packages

5.1 Hardware Sets

The various hardware sets and modules which are offered are listed below:

Basic Rate Configuration
Primary Rate Configuration
S-Interface Kit
S-Interface Terminal Equipment
S-Interface NT-Simulator (NT-S)
S-Interface Kit (ISAC-S)
S-Interface Terminal Equipment (ISAC-S)
S-Interface NT-Simulator (NT-S) (ISAC-S)
U_{k0}-Interface Kit
U_{k0}-Interface Terminal Equipment
U_{k0}-Interface NT-Simulator (NT-S)
U_{p0}-Interface Kit
U_{p0}-Interface Terminal Equipment
U_{p0}-Interface NT-Simulator (NT-S)
Primary Rate Kit
Hardware Options

Basic rate kits differ from each other only in the physical transmission module. The general structure is shown in **figure 17**. These kits include hardware, firmware (on EPROM), and menu software.

The block diagram of the primary rate kit is depicted in **figure 18**. This kit supports T1 and CEPT applications and includes hardware and menu software as well as firmware on EPROM.

Figure 17
Configurations Supporting S-, U_{k0}-, U_{p0}-Interfaces

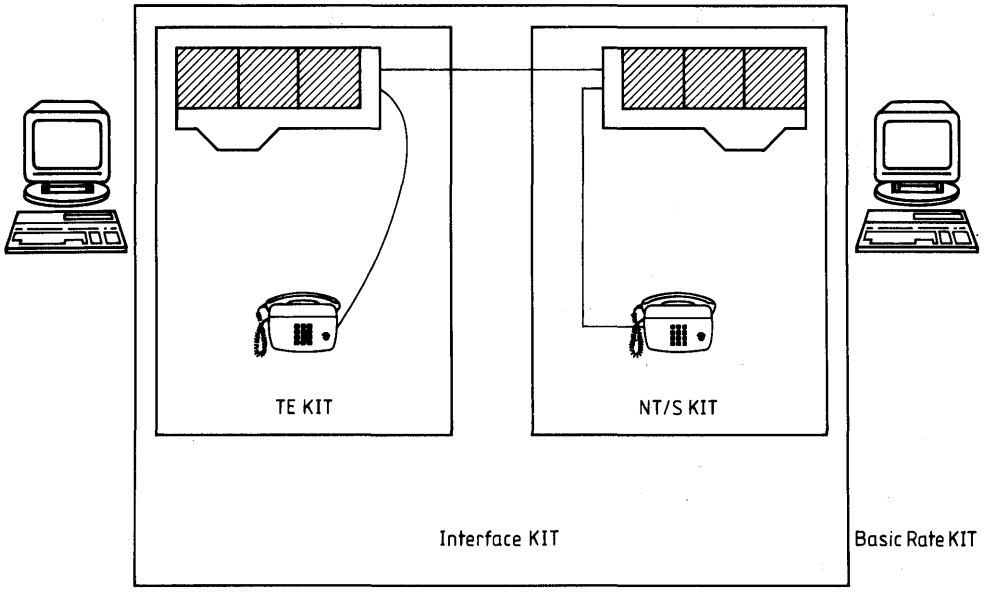
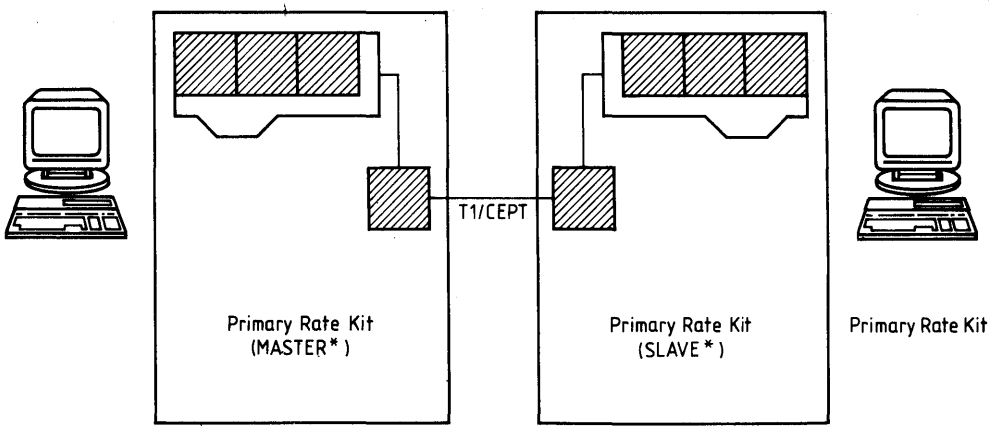


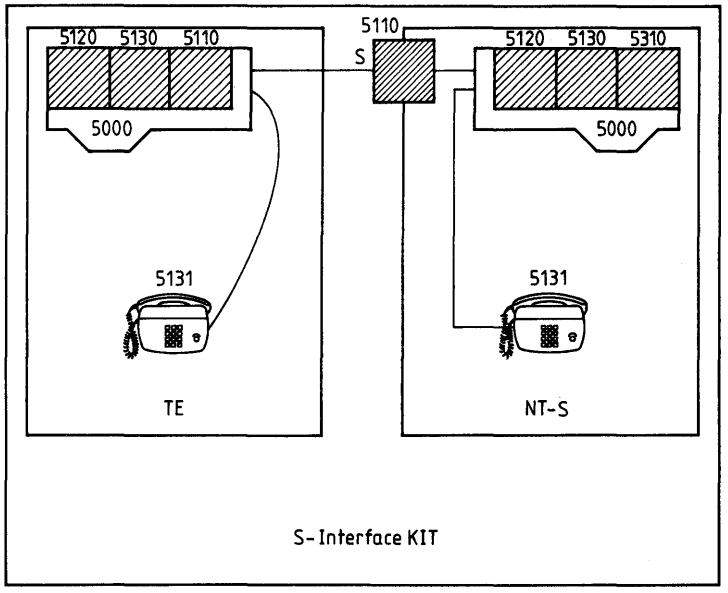
Figure 18
Primary Rate Kit



* MASTER+SLAVE Configurations differ only in Jumper Settings.

As a particular example the configuration of an S-Interface Kit is given in **figure 19** below.

Figure 19
S-Interface Kit Configuration



Description	Part Number	Ordering Code
S-Interface Kit	SIPB 7030	Q67100-H8652
2 x Mainboard SIPB (includes Mainboard Firmware + Menu Software)		
2 x S-Layer-1 Module (SBC)	SIPB 5110	
2 x Layer-2 Module (ICC/HSCC)	SIPB 5120	
2 x Audio Interface Module	SIPB 5130	
2 x Telephone Module (SICOFI®) (Optional telephone casing may be requested)	SIPB 5131	
1 x Timing Module	SIPB 5310	

5.2 Software Kits

The IOS is available in source and/or object code. The code for L3 consists of call control software for basic voice and data services.

Table 1
Protocol Software Packages

Kit	Layer 2	Layer 2/3
TE	according to CCITT, AT&T	according to CCITT, AT&T
NT-S	according to CCITT, AT&T	according to CCITT, AT&T
Interface	i.e. TE & NT-S	i.e. TE & NT-S

The SIDES is available in object code. The program BOARD.EXE is used to verify the firmware and IOS when it is downloaded to the SIPB.

Several possible packages are shown in **table 2**.

Table 2
Packages

Name	Single	Set
BOARD.EXE	incl. BYT files	
STEP	Library and EXE files	
DYRECT/STORY	Library and EXE files	
SITEST		*)
PCT		Δ)

*) SITEST = STEP + DYRECT / STORY + BOARD.EXE

Δ) Incl. IPCS, C-Source Code Generator and Documentation Generator

5.3 Applications

The main applications are again summarized in **table 3**. This table also reflects the normal steps of development, beginning with hardware evaluation and ending in complete user system with adapted software.

Table 3

SIPB - IOS - SIDES Application Overview

1.

HW	ISDN development platform including a coprocessor system
Menu SW	Access to all registers
FW	Clear functional interface to user developed protocol SW.

2.

HW	Functional unit, with specific layer-2 & -3 SW.
Menu SW	Allows customer to run various applications for voice and data. Control via terminal or host-mailbox programming
FW	
L2 & L3	

3.

HW	Allows to establish a voice and / or data communication to a peer station.
Menu SW	Simulation and analysation of protocol
FW	
L2 & L3	
SITEST	Control of MF and IOS on board

4.

HW	Enables the customer to modify and adapt the delivered SW packages to this own requirements.
Menu SW	
FW	
L2	
L3	
SITEST	
PCT	

6 Literature References, Abbreviations and Definitions

Literature References

a) General Literature

CCITT Recommendation	Q.920 / 1
CCITT Recommendation	I.440 / 1
CCITT Recommendation	Q.930 / 1

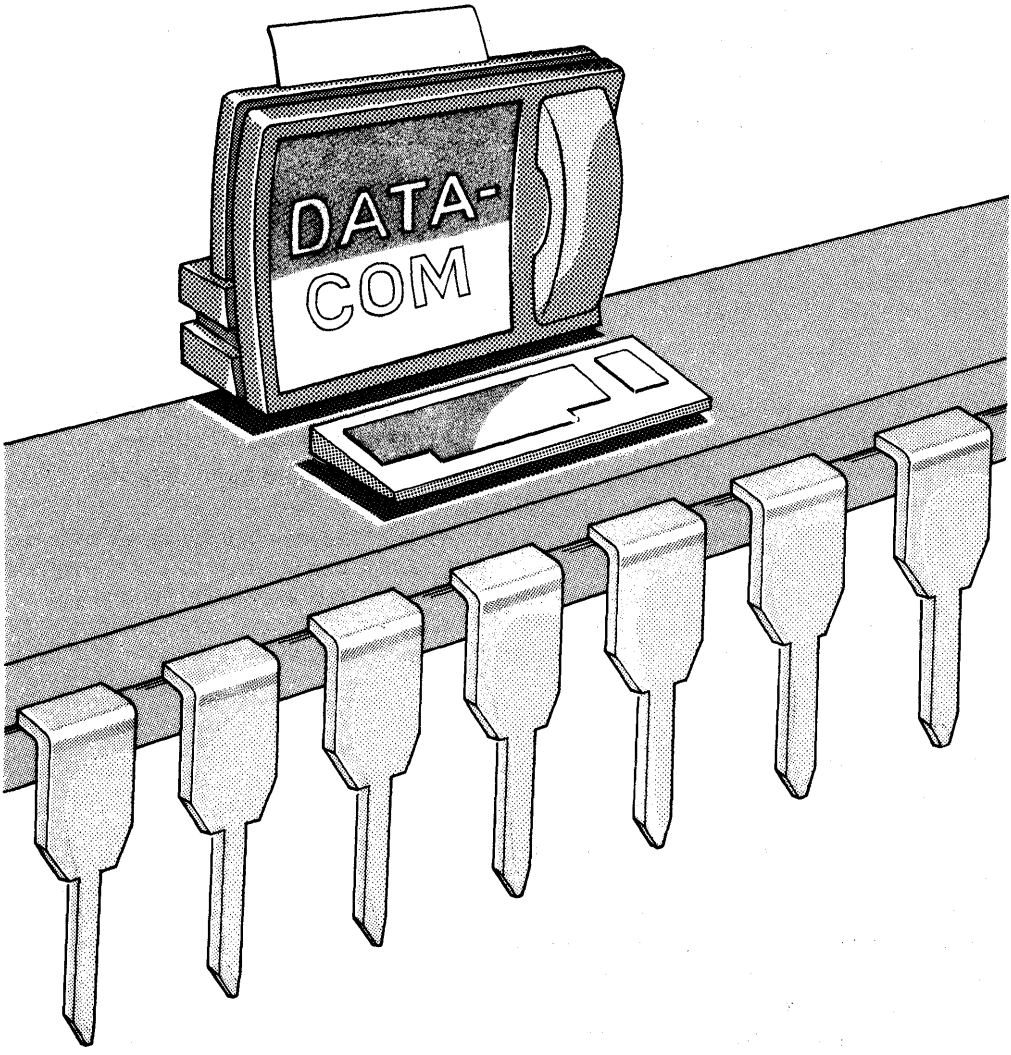
b) Literature from Siemens

PCT Demo Guideline Rev. 1.0
SIPB C / R-Mailbox Interface Specification, Volume 3,2.89
SIPB User Manual, Volume 2, 4.89
SITEST Manual Rev. 1.1
PCT User Manual Rev. 2.1
IOS LAPD Protocol Reference Spec. Rev. 1.0
IPCS Technical Description Rev. 1.0
SIPB Firmware Manual, Volume 5; 1.89

Abbreviations, Definitions

LAPD	: =	Link Access Procedure on the D channel
IOS	: =	ISDN Operational Software
IOM®	: =	ISDN Oriented Modular
IPCS	: =	IOS Process Control System
SDL	: =	Functional Specification and Description Language
SIPB	: =	Siemens ISDN PC User Board
STEP	: =	Static Test Tool for Protocol software
DYRECT	: =	Dynamic Real-Time Communication Tester
STORY	: =	Screening Tool for Report Files
SITEST	: =	Siemens ISDN Protocol Software Test Tools
SIDES	: =	Siemens ISDN Software Development and Evaluation System
PCT	: =	Program Coding Tools

Data Communication ICs


DATA-
COM

High-Level Serial Communications Controller (HSCC)

SAB 82520
SAF 82520

Type	Ordering Code	Package
SAB 82520-C	Q67100-H8830	C-CIP-28
SAB 82520-N	Q67100-H8400	PL-CC-28 (SMD)
SAB 82520-P	Q67100-H8014	P-DIP-28
SAF 82520-C	Q67100-H8325	C-DIP-28
SAF 82520-N	Q67100-H8610	PL-CC-28 (SMD)
SAF 82520-P	Q67100-H8512	P-DIP-28

SAB 82520, a High-level Serial Communications Controller (HSCC), has been designed to free the user from tasks occuring in communication via networks and trunk lines.

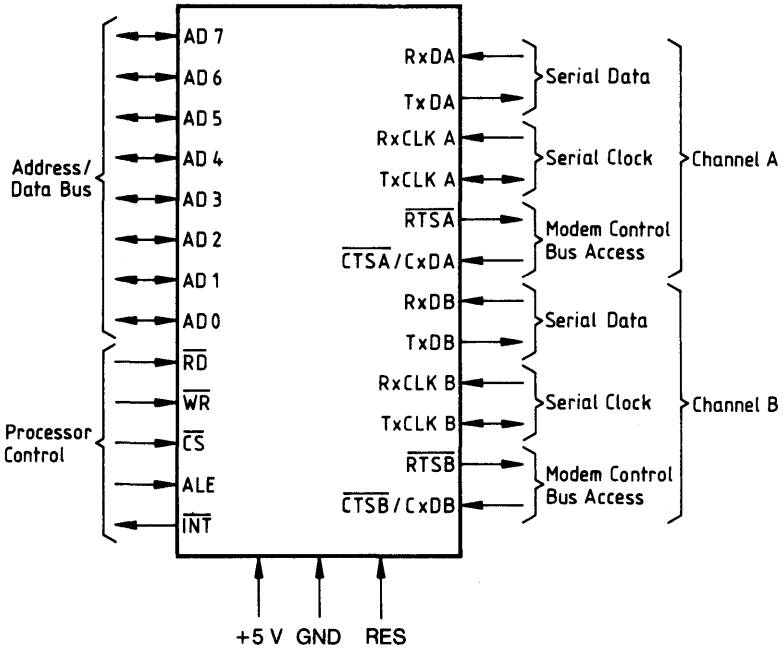
SAB 82520 is an X.25 LAPB/LAPD controller which, to a large degree performs communications procedures independently of CPU support.

A parallel processor bus constitutes the µC system. The communications interface is implemented by two full-duplex HDLC channels, which can be operated independently from one another. The HSCC is connected to the transmission line via additional line drivers or modems. External logic is cost-effective because clock recovery can be performed by an on-chip oscillator, DPLL circuits and a programmable baudrate generator.

Features

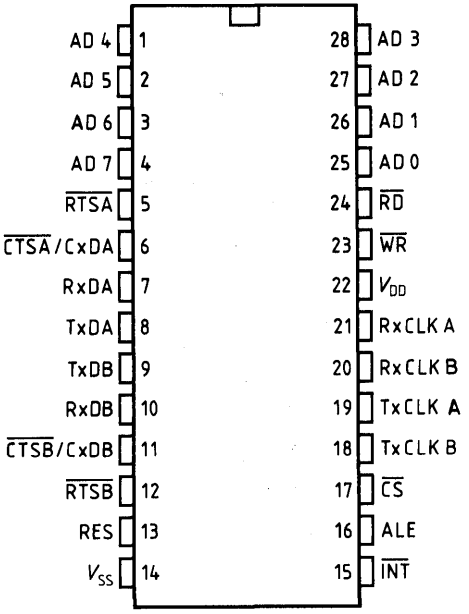
- Two independent HDLC channels
- Implementation of X.25 LAPB/LAPD protocol
- Programmable timeout and retry conditions
- FIFO buffers for efficient transfer of data packets
- Digital phase-locked loop for each channel
- Baudrate generator and oscillator
- Different modes for clock recovery and data encoding
- High-speed data rate (up to 4 MHz)
- Supports bus configuration by collision resolution
- Telecom-specific features programmable
- 8-bit parallel µP interface
- Advanced CMOS technology
- Low power consumption; active: 25 mW at 4 MHz
  standby: 3 mW
- SAB 82520: operating temperature 0 to 70 °C
- SAF 82520: operating temperature −40 to 85 °C

Logic Symbol

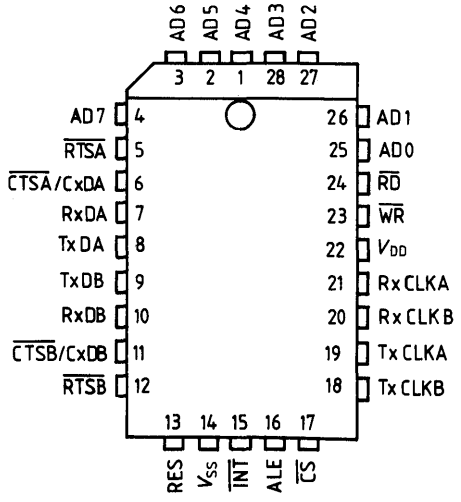


Pin Configurations
(top view)

P-DIP; C-DIP



PL-CC



Pin Definitions and Functions

Pin No.	Symbol	Input (I) Output (O)	Functions
25 26 27 28 1 2 3 4	AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7	I/O I/O I/O I/O I/O I/O I/O I/O	**Address Data Bus** The multiplexed address data bus transfers data and commands between the µP system and the HSCC.
5 12	$\overline{\text{RTSA}}$ $\overline{\text{RTSB}}$	O O	**$\overline{\text{Request to Send}}$** When the RTS bit in MODE is set, the $\overline{\text{RTS}}$ signal goes low. When the RTS bit is reset, the signal goes high of the transmitter has finished and there is no further request for a transmission. In a bus configuration, RTS goes low during the actual transmission of a frame shifted by a clock period, excluding collision bits.
6 11	$\overline{\text{CTSA}}$/C x DA $\overline{\text{CTSB}}$/C x DB	I I	**$\overline{\text{Clear to Send}}$/Collision Data** A low on the inputs enables the respective transmitter. If the transmitters are always enabled, $\overline{\text{CTS}}$ should be connected to V_{SS}. In a bus configuration the external serial bus must be connected to the respective C x D pin.
7 10	R x DA R x DB	I I	**Receive Data** These lines receive serial data at standard TTL or CMOS levels.
8 9	T x DA T x DB	O O	**Transmit Data** These lines transmit serial data at standard TTL or CMOS levels. They can be programmed as push-pull or open-drain outputs.
13	RES	I	**RESET** A high on this input forces the HSCC into reset state. The HSCC is in power-up mode during reset and in power-down mode after reset. The minimum pulse length is 1.8 µs.
14	V_{SS}		Ground (0 V)
15	$\overline{\text{INT}}$	O	**$\overline{\text{Interrupt Request}}$** The signal is activated when the HSCC requests an interrupt. It is an open-drain output.

Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Functions
16	ALE	I	**Address Latch Enable** A high on this line indicates an address on the external address data bus, selecting one of the HSCC internal sources or destinations
17	$\overline{CS}$	I	**$\overline{\text{Chip Select}}$** A low on this signal selects the HSCC for a read/write operation.
18 19	T x CLKB T x CLKA	I/O I/O	**Transmit Clock** These pins can be programmed in several different modes of operation. T x CLK may supply the transmit clock for the respective channel, a receive strobe signal (T x CLKA) and a transmit strobe signal (T x CLKB) or a frame synchronization signal (T x CLKA, clock mode 5). Programmed as outputs, T x CLK supply the transmit clock of the respective channel or a tristate control signal, indicating the programmed transmit time slot (T x CLKB, clock mode 5).
20 21	R x CLKB R x CLKA	I I	**Receive Clock** These pins can be programmed in several different modes of operation. In each channel R x CK may supply the receive clock, the receive and transmit clock, the clock for the baud rate generator or the clock for the DPLL. They also can be programmed for use as a crystal oscillator.
22	V_{DD}		Power +5 V power supply.
23	$\overline{WR}$	I	**$\overline{\text{Write}}$** This signal indicates a write operation.
24	$\overline{RD}$	I	**$\overline{\text{Read}}$** This signal indicates a read operation.

Applications

Figure 1a
Point-to-Point Configuration

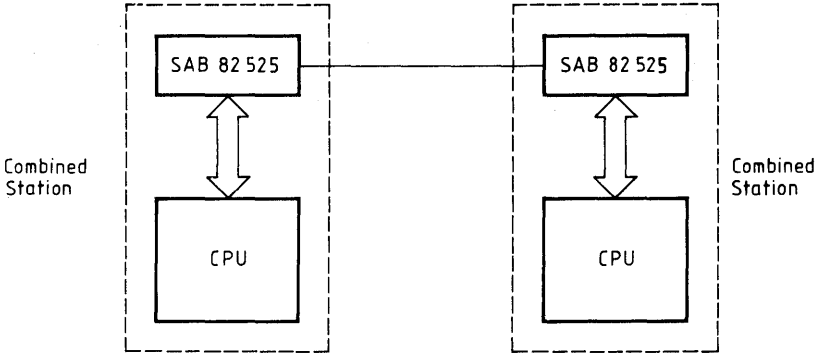


Figure 1b
Point-to-Multipoint Configuration

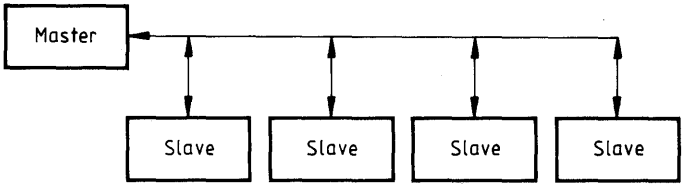
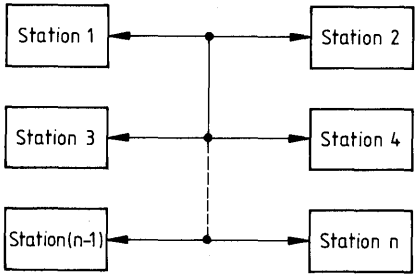


Figure 1c
Multimaster Configuration



Description

In a point-to-multipoint or in a multimaster configuration the HSCC can be used as a central station (master) or a peripheral station. As a peripheral station the HSCC can initiate the transmission of data. An internal function block provides for collision avoidance, which may occur if several stations start the transmitting simultaneously.

Furthermore, in a special operating mode the HSCC can transmit or receive data packets in programmable time slots; this makes SAB 82520 especially suitable for applications in systems designed for packet switching. In this application in particular, the integrated collision-resolution mechanism provides optimal utilization of system-internal PCM paths.

Characteristics

A number of characteristics which distinguish the SAB 82520 from conventional lowlevel HDLC devices are described below.

Support of Layer-2 Functions by HSCC

"Low-level" HDLC devices usually support various of protocols. When applying the HDLC protocol mainly bit-oriented functions such as bit stuffing, CRC check, flag and address recognition are performed. SAB 82520 has been especially designed to support the ISO HDLC protocol. In addition to the bit-oriented functions, the device provides a high degree of procedural support and evaluates the layer-2 control field. The communications procedures are processed between the communications controllers and not between the processors. As a result procedure handshaking is no longer necessary. The processor is informed of the status of the procedure however. The dynamic load of the processor is thus largely reduced. To maintain cost effectiveness and flexibility, not all layer-2 functions have been implemented as hardware. Instead, functions such as connection setup/connection clear-down and error recovery in case of protocol errors are performed by the processor software.

Operating Modes

The distribution of functions between HSCC and CPU applies to the auto mode. As a prerequiste for this operating mode, the window size between transmitted and acknowledged frames has to be limited to 1. Alternatively, transparent modes can be applied, the data field as well as the layer-2 headers are forwarded directly to the CPU. The reception and transmission of messages is fully controlled by the CPU. This operating mode is selected when the component is used as a central station (master) or if the accepted distance between transmitted and received frames (window size) is larger than 1.

Furthermore, there is a possibility to bypass the receiver and to get access to the received data directly.

FIFO Buffers for Efficient Transfer of Data Packets

Another feature of the SAB 82520 can be seen in the buffers that are used for temporary storage of data packets which are transferred between the serial communication interface and the parallel system bus. Due to the overlapping input/output operation (dual-port behavior), the maximum length of the data packets is not limited by the buffer size. The dynamic load of the processor is reduced by transferring the data packets block by block.

One FIFO buffer with a total capacity of 64 bytes per direction and channel is divided into two memory pools of 32 bytes each. When a pool is filled (receive mode) or emptied (transmit mode) via the serial interface, the processor is prompted by interrupt to read or write this pool. Subsequently the second pool is filled or emptied. During this time the CPU can transfer the first block thereby ensuring availability of the pool. With a serial transfer rate of 1 Mbit/s the reaction time between the first prompting and data overflow with loss of data is 256 µs. In addition, the transmit FIFO provides the flexibility for temporarily storing blocks of various lengths, which can be received in rapid succession. The FIFO will also store a data packet when a preceding short data packet stored in the memory has not yet been read by the processor.

The HSCC is especially suitable for cost-critical applications with single chip processors due to its memory organization and on-chip memory control.

Move string commands are available for high-performance applications where fast data rates at the communication interface and a high level of processor performance are required. The FIFO can then be addressed by the automatically incremented address.

Serial Interface

The serial interface provides two independent, high-performance communication interfaces. As already mentioned, the ISO HDLC layer-2 protocol is supported by the HSCC. In addition, layer-1 functions are provided by means of on-chip circuits. Eight different operating modes can be selected to clock the serial data stream.

- During the self-clocked operating mode, the transfer clock is recovered from the received data stream by means of an external crystal only. On-chip oscillator and DPLL circuits sample the received bit stream and adjust the clock edge to the center of the data bit.

- The bit stream is synchronized in the externally clocked operation mode by external clock signals. One the whole, 4 different clock signals separated by direction and channel, can be forwarded.

  In addition to the data clock, an externally supplied strobe signal can be applied to determine the time period during which data is to be received or transmitted. Using another operating mode, a time slot (up to 64 bit) can be programmed for transmitting data and another time slot for receiving data. One time slot consists of eight clock cycles.

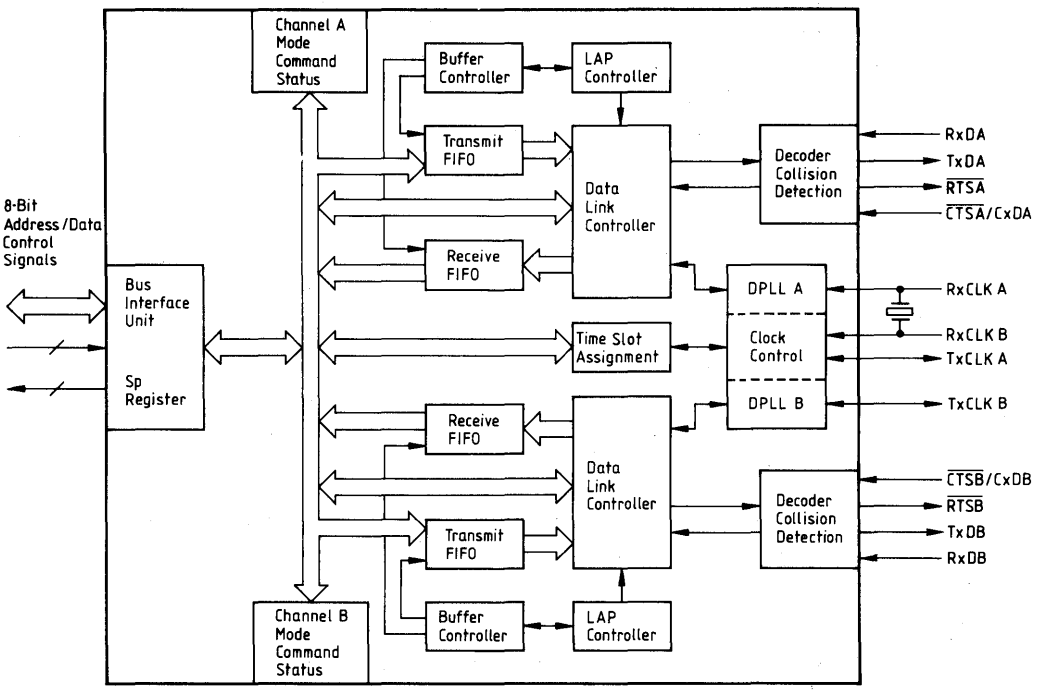
- With the point-to-multipoint configuration, comprising a central station (master) and several peripheral stations (slaves), data transmission can be initiated by a slave. If several stations (slaves) transmit data simultaneously, the bus is assigned to one station by a collision-resolution procedure implemented by the HSCC. The bus assignment functions in accordance with the principle applied with the ISDN S bus. Its collision-resolution procedure helps to ensure a sharing of priority among the slave stations.

- The maximum data rate of the externally clocked operating mode is 4 Mbits per second. In the self-clocked operating mode with an external reference clock or the crystal oscillator, the maximum clock rate is 12 MHz, the maximum data rate will be 750 kbit/s.

Description of Block Diagram

The chip contains a serial interface for two channels, including a DPLL and collision-detection block, a data-link controller and the FIFO buffers. The µP interface, including the status and command registers, is used for both channels. These functions are implemented in 2 µm CMOS technology.

Block Diagram



Absolute Maximum Ratings

Parameter		Symbol	Limit Values min.	Limit Values max.	Unit
Storage temperature		T_{stg}	−65	125	°C
Operating temperature:	SAB 82520	T_A	0	70	°C
Operating temperature:	SAF 82520	T_A	−40	85	°C
Voltage at any pin vs. ground		V_S	−0.4	V_{CC} +0.4	V

DC Characteristics

SAB 82520: $T_A = 0$ to 70 °C; $V_{CC} = 5\ V \pm 10\%$; GND = 0 V
SAF 82520: $T_A = -40$ to 85 °C; $V_{CC} = 5\ V \pm 5\%$; GND = 0 V

Parameter	Symbol	Limit Values min.	Limit Values typ.	Limit Values max.	Unit	Test Conditions
L-input voltage	V_{IL}	V_{SS}−0.4		0.8	V	
H-input voltage	V_{IH}			V_{CC}+0.4	V	
L-output voltage	V_{OL}			0.45	V	$I_{OL} = 2$ mA
H-output voltage	V_{OH}	2.4			V	$I_{OH} = -400\ \mu A$
		V_{CC}−0.5	V_{CC}		V	$I_{OH} = -100\ \mu A$
Input leakage current	I_{IL}	−10		10	µA	$V_{IN} = V_{CC}$ to 0 V
Output leakage current	I_{OL}	−10		10	µA	$V_{OUT} = V_{CC}$ to 0 V
V_{CC} supply current						
p. d.	I_{CC}		0.5	1.8	mA	
p. u.	I_{CC}		5	7	mA	$V_{CC} = 5$ V, $C_P = 4$ MHz, Inputs at V_{SS}/V_{CC}, No output loads

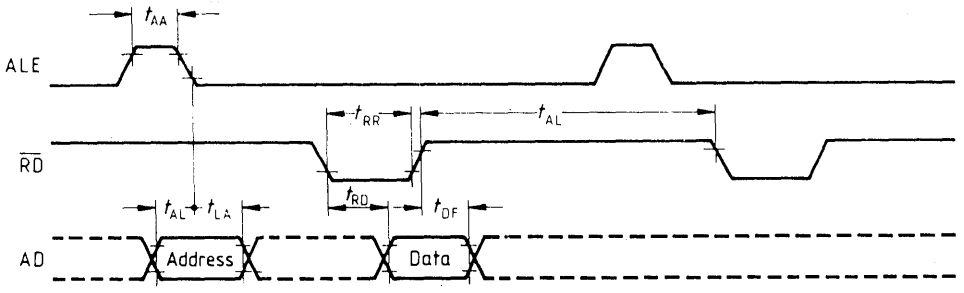
Capacitance

$T_A = 25$ °C; V_{CC} = GND = 0 V

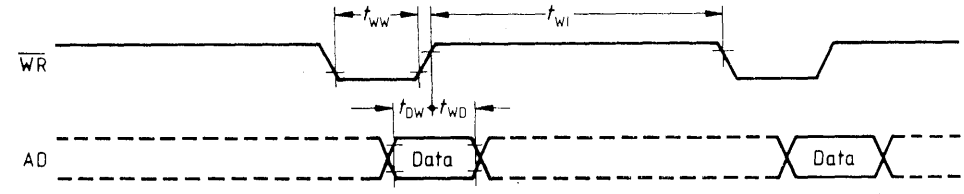
Parameter	Symbol	Limit Values min.	Limit Values typ.	Limit Values max.	Unit
Input capacitance $f_C = 1$ MHz	C_{IN}		5	10	pF
Input/output capacitance	$C_{I/O}$		10	20	pF
Output capacitance unmeasured pins returned to GND	C_{OUT}		8	15	pF

µP Interface Timing

Read Cycle



Write Cycle



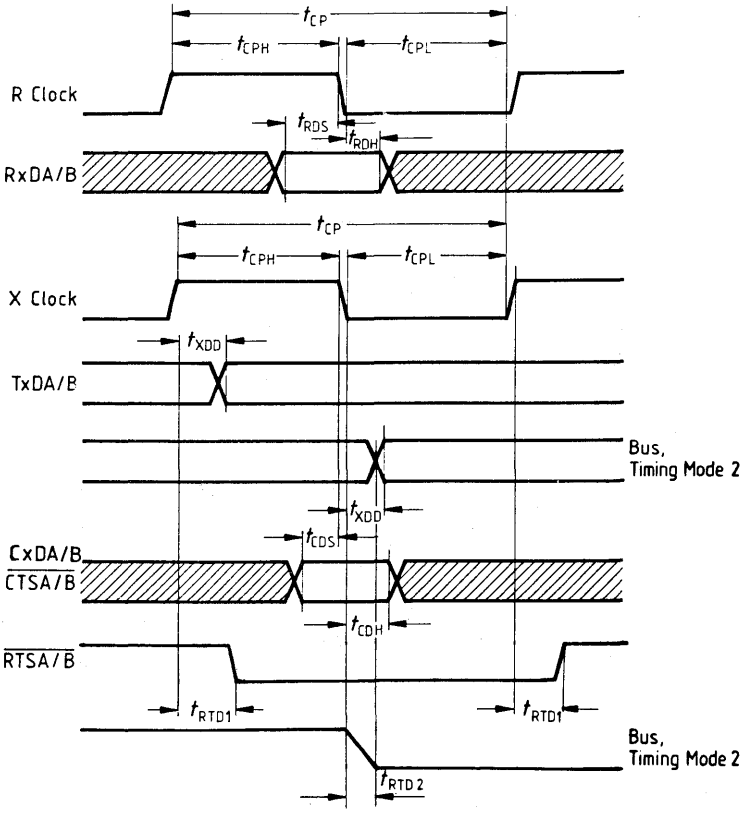
Read Cycle

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit
Address hold after ALE	t_{LA}	25		ns
Address to ALE setup	t_{AL}	20		ns
Data delay from RD	t_{RD}		110	ns
RD pulse width	t_{RR}	110		ns
Output float delay	t_{DF}		25	ns
RD control interval	t_{RI}	60		ns
ALE pulse width	t_{AA}	50		ns

Write Cycle

Parameter	Symbol	Limit Values min.	Limit Values max.	Unit
WR pulse width	t_{WW}	60		ns
Data setup to WR	t_{DW}	30		ns
Data hold after WR	t_{WD}	10		ns
WR control interval	t_{WI}	60		ns

Serial Interface Timing

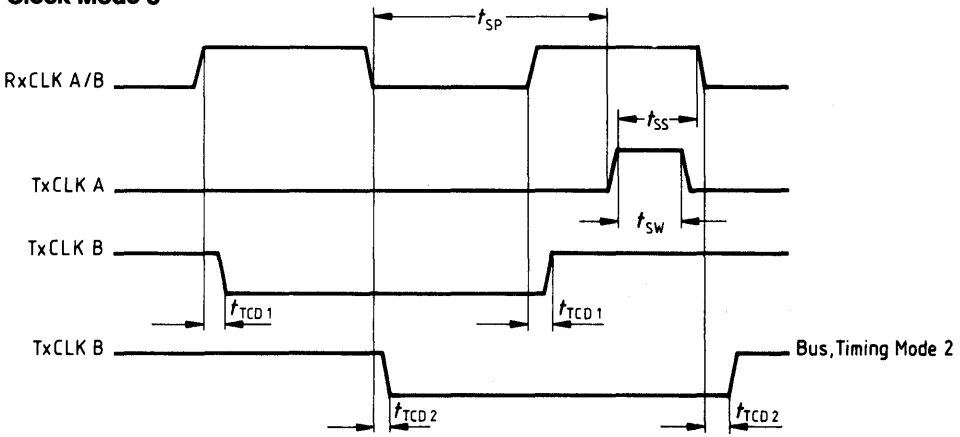


AC Characteristics

SAB 82520: $T_A = 0$ to 70 °C; $V_{CC} = 5\ V \pm 10\%$; GND = 0 V
SAF 82520: $T_A = -40$ to 85 °C; $V_{CC} = 5\ V \pm 5\%$; GND = 0 V

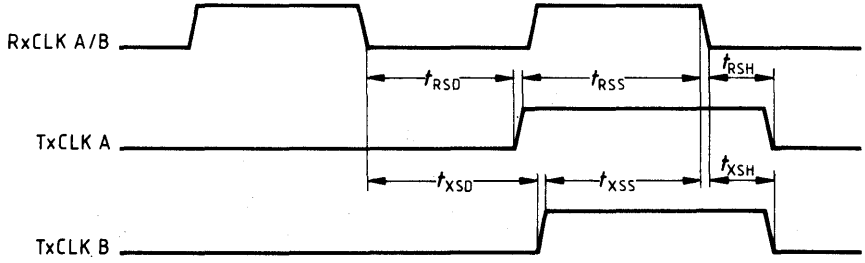
Parameter	Symbol	Limit Values		Unit
		min.	max.	
Receive data setup	t_{RDS}	0		ns
Receive data hold	t_{RDH}	30		ns
Collision data setup	t_{CDS}	0		ns
Collision data hold	t_{CDH}	30		ns
Transmit data delay	t_{XDD}	20	68	ns
Request to send delay 1	$t_{RTD\,1}$	30	130	ns
Request to send delay 2	$t_{RTD\,2}$	20	85	ns
Clock period	t_{CP}	240		ns
Clock period Low	t_{CPL}	90		ns
Clock period High	t_{CPH}	100		ns

Clock Mode 5



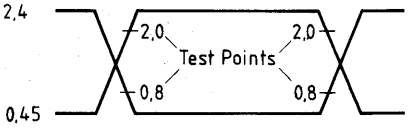
Parameter	Symbol	Limit Values min.	Limit Values max.	Unit
Sync pulse delay	t_{SD}	30		ns
Sync pulse setup	t_{SS}	30		ns
Sync pulse width	t_{SW}	40		ns
Time-slot control 2 delay	$t_{TCD\,2}$	20	95	ns
Time-slot control 1 delay	$t_{RCD\,1}$	30	120	ns

Clock Mode 1

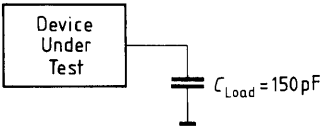


Parameter	Symbol	Limit Values min.	Limit Values max.	Unit
Receive strobe delay	t_{RSD}	30		ns
Receive strobe setup	t_{RSS}	70		ns
Receive strobe hold	t_{RSH}	30		ns
Transmit strobe delay	t_{XSD}	30		ns
Transmit strobe setup	t_{XSS}	90		ns
Transmit strobe hold	t_{XSH}	30		ns

AC Testing Input, Output Waveform



AC Testing Load Circuit



AC Testing

Inputs are driven at 2.4 V for logic "1" and 0.45 V for logic "0".
Timing measurements are made at 2.0 V for logic "1" and at 0.8 V for logic "0".

SIEMENS

High-Level Serial Communication Controller Extended (HSCX)

SAB 82525
SAB 82526
SAF 82525
SAF 82526

Preliminary Data

CMOS IC

Type	Ordering Code	Package
SAB 82525 N	Q67100-H8590 A401	PL-CC-44 (SMD)
SAB 82526 N	Q67100-H6111	PL-CC-44 (SMD)
SAF 82525 N	Q67100-H6057	PL-CC-44 (SMD)
SAF 82526 N	Q67100-H6129	PL-CC-44 (SMD)

The SAB 82525 is a High-Level Serial Communications Controller compatible to the SAB 82520 HSCC with extended features and functionality (HSCX).

The SAB 82526 is pin and software compatible to the SAB 82525, realizing one HDLC channel (channel B).

The HSCX has been designed to implement high-speed communication links using HDLC protocols and to reduce the hardware and software overhead needed for serial synchronous communications.

Due to its 8-bits demultiplexed adaptive bus interface it fits perfectly into every SIEMENS/ INTEL or Motorola 8- or 16-bit microcontroller or microprocessor system. The data throughput from/to system memory is optimized transfering blocks of data (usually 32 bytes) by means of DMA or interrupt request. Together with the storing capacity of up to 64 bytes in on- chip FIFO's, the serial interfaces are effectively decoupled from the system bus which drastically reduces the dynamic load and reaction time of the CPU.

The HSCX directly supports the X.25 LAP B, the ISDN LAP D, and SDLC (normal response mode) protocols and is capable of handling a large set of layer-2 protocol functions independently from the host processor.

Furthermore, the HSCX opens a wide area for applications which use time division multiplex methods (e.g. time-slot oriented PCM systems, systems designed for packet switching, ISDN applications) by its programmable telecom-specific features.

The HSCX is fabricated using SIEMENS advanced ACMOS 3 technology and available in a PL-CC-44 pin package.

Features

Serial Interface

- Two independent full-duplex HDLC channels (SAB 82526: one channel)
  - On chip clock generation or external clock source
  - On chip DPLL for clock recovery for each channel
  - Two independent baudrategenerators (SAB 82526: one baudrate generator)
  - Independent time-slot assignment for each channel with programmable time-slot length (1 - 256 bit)
- Different modes of data encoding
- Modem control lines (RTS, CTS, CD)
- Support of bus configuration by collision resolution
- Programmable bit inversion
- Transparent receive/transmit of data bytes without HDLC framing
- Continuous transmission of 1 to 32 bytes possible
- Data rate up to 4 Mbit/s

Protocol Support

- Various types of protocol support depending on operating mode
  - Auto mode
  - Non auto mode
  - Transparent mode
- Handling of bit oriented functions in all modes
- Support of LAPB/LAPD/SDLC/HDLC protocol in auto mode (I- and S-frame handling)
- Modulo 8 or modulo 128 operation
- Programmable timeout and retry conditions
- Programmable maximum packet size checking

µP Interface

- 64 byte FIFO's per channel and direction
- Storage capacity of up to 17 short frames in receive direction
- Efficient transfer of data blocks from/to system memory by DMA or interrupt request
- 8-bit demultiplexed or multiplexed bus interface
- Intel or Motorola type MP interface

General

- Compatible to SAB 82520 (HSCC)
- Advanced CMOS technology
- Low power consumption: active 25 mW at 4 MHz
  standby 4 mW

The data link controller handles all functions necessary to establish and maintain an HDLC data link, such as

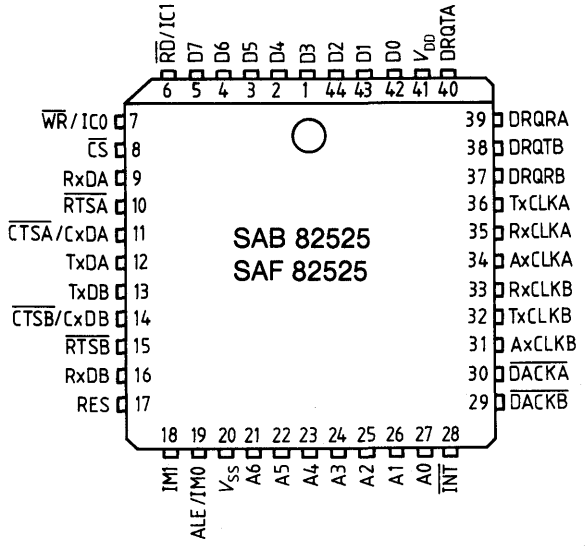
- Flag insertion and detection,
- Bit stuffing,
- CRC generation and checking,
- Address field recognition.

Associated with each serial channel is a set of independent command and status registers (SP-REG) and 64-byte deep FIFO's for transmit and receive direction.

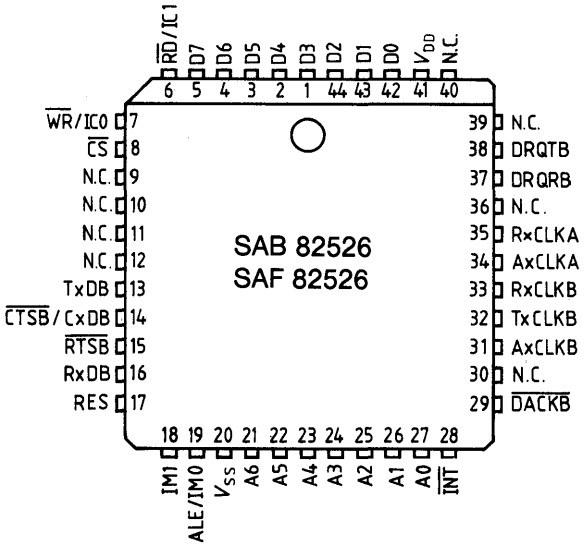
DMA capability has been added to the HSCX by means of a 4-channel DMA interface (SAB 82525) with one DMA request line for each transmitter and receiver of both channels.

Pin Configurations
(top view)

PL-CC-44



PL-CC-44



Pin Definitions and Functions

Pin No.	Symbol	Input (I) Output (O)	Function
42 43 44 1 2 3 4 5	D0 D1 D2 D3 D4 D5 D6 D7	I/O	**Data Bus** The data bus lines are bidirectional threestate lines which interface with the system's data bus. These lines carry data and command/status to and from the HSCX.
6	$\overline{RD}$/IC1	I	**Read**, Intel bus mode, IM1 connected to low This signal indicates a read operation. When the HSCX is selected via CS the read signal enables the bus drivers to put data from an internal register adressed via A0-A6 on the data bus. When the HSCX is selected for DMA transfers via DACK, the RD signal enables the bus driver to put data from the respective receive FIFO on the data bus. Inputs to A0-A6 are ignored. **Input Control 1,** Motorola bus mode IM1 connected to high. If Motorola bus mode has been selected this pin serves either as E = Enable, active high (IM0 tied to low) or DS = Data Strobe, active low (IM0 tied to high) input (depending on the selection via IM0) to control read/write operations.
7	$\overline{WR}$/IC0	I	**Write**, Intel bus mode This signal indicates a write operation. When CS is active the HSCX loads an internal register with data provided via the data bus. When DACK is active for DMA transfers the HSCX loads data from the data bus on the top of the respective transmit FIFO. **Input Control** Motorola bus mode In Motorola bus mode, this pin serves as the R/W input to distinguish between read or write operations.
8	$\overline{CS}$	I	**Chip Select** A low signal selects the HSCX for a read/write operation.

Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
9 16	$\overline{\text{RXDA}}$ $\overline{\text{RXDB}}$	I	**Receive Data** (channel A/channel B) Serial data is received on these pins at standard TTL or CMOS levels.
10 15	$\overline{\text{RTSA}}$ $\overline{\text{RTSB}}$	O	**Request to Send** (channel A/channel B) When the RTS bit in the mode register is set, the RTS signal goes low. When the RTS i reset, the signal goes high if the transmitter has finished and there is no further request for a transmission. In a bus configuration, this pin can be programmed via CCR2 to: – go low during the actual transmission of a frame shifted by one clock period, excluding collision bits – go low during the reception of a data frame – stay always high (RTS disabled).
11 14	$\overline{\text{CTSA}}$/ CXDA $\overline{\text{CTSB}}$/ CXDB	I	**Clear to Send** (channel A/channel B) A low on the CTS inputs enables the respective transmitter. Additionally, an interrupt may be issued if a state transition occurs at the CTS pin (programmable feature). If no "Clear To Send" function is required, the CTS inputs can be connected directly to GND. **Collision Data** (channel A/channel B) In a bus configuration, the external serial bus must be connected to the respective CxD pin for collision detection.
12 13	TXDA TXDB	O	**Transmit Data** (channel A/channel B) Transmit data is shifted out via these pins at standard TTL or CMOS levels. These pins can be programmed to work either as push-pull, or open drain outputs supporting bus configurations.
17	RES	I	**RESET** A high signal on this input forces the HSCX into the reset state. The HSCX is in power-up mode during reset and in power-down mode after reset. The minimum pulse width is 1.8 ms.

Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
18	IM1	I	**Input Mode 1** Connecting this pin to either V_{SS} or V_{DD} the bus interface can be adapted to either SIEMENS/INTEL or Motorola environment. IM1 = LOW: Intel bus mode IM1 = HIGH: Motorola bus mode
19	ALE/IM0	I	**Address Latch Enable** (Intel bus mode) A high on this line indicates an address on the external address/data bus, which will select one of the HSCX's internal registers. The address is latched by the HSCX with the falling edge of ALE. This allows the HSCX to be directly connected to a CPU with multiplexed address/ data bus compatible to SAB 82520 HSCC. The address input pins A0-A6 must be externally connected to the data bus pins (D0-D6 for 8-bit CPU's, D1-D7 for 16-bit CPU's, i.e. multiply all internal register addresses by 2). **Input Mode 0**, Motorola bus mode In Motorola Bus Mode, the level at this pin determines the function of the IC1 pin (see description of pin 6).
20	V_{SS}	I	**Ground** (0 V)
27 26 25 24 23 22 21	A0 A1 A2 A3 A4 A5 A6	I	**Address Bus** These inputs interface with seven bits of the system's address bus to select one of the internal registers for read or write. They are usually connected at A0-A6 in 8-bit systems or at A1-A7 in 16-bit systems.
28	$\overline{INT}$	O	**Interrupt Request** The signal is activated, when the HSCX requests an interrupt. The CPU may determine the particular source and cause of the interrupt by reading the HSCX's interrupt status registers. (ISTA, EXIR). $\overline{INT}$ is an open drain output, thus the interrupt requests outputs of several HSCX's can be connected to one interrupt input in a "wired-or" combination. This pin must be connected to a pull-up resistor.

Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
30 29	$\overline{\text{DACKA}}$ $\overline{\text{DACKB}}$	I	**DMA Acknowledge** (channel A/channel B) When low, this input signal from the DMA controller notifies the HSCX, that the requested DMA cycle controlled via DRQxx (pins 37-40) is in progress, i.e. the DMA controller has achieved bus mastership from the CPU and will start data transfer cycles (either read or write). Together with RD, if DMA has been requested from the receiver, or with WR, if DMA has been requested from the transmitter, this input works like $\overline{\text{CS}}$ to enable a data byte to be read from or written to the top of the receive or transmit FIFO of the specified channel. If DACKn is active, the input to pins A0-A6 is ignored and the FIFOs are implicitly selected. If the DACKn signals are not used, these pins must be connected to V_{DD}.
34 31	AxCLKA AxCLKB	I	**Alternative Clock** (channel A/channel B) These pins realize several input functions. Depending on the selected clock mode, they may supply either a – CD (= Carrier Detect) modem control or general purpose input. This pin can be programmed to functions as receiver enable if the "auto start" feature is selected (CAS bit in XBCH set). The state at this pin can be read from VSTR register, – or a receive strobe signal (clock mode 1) – or a frame synchronization signal in time-slot oriented operation mode (clock mode 5) – or, together with RxCLK, a crystal connection for the internal oscillator (clock mode 4, 6, 7, AxCLKA) only).

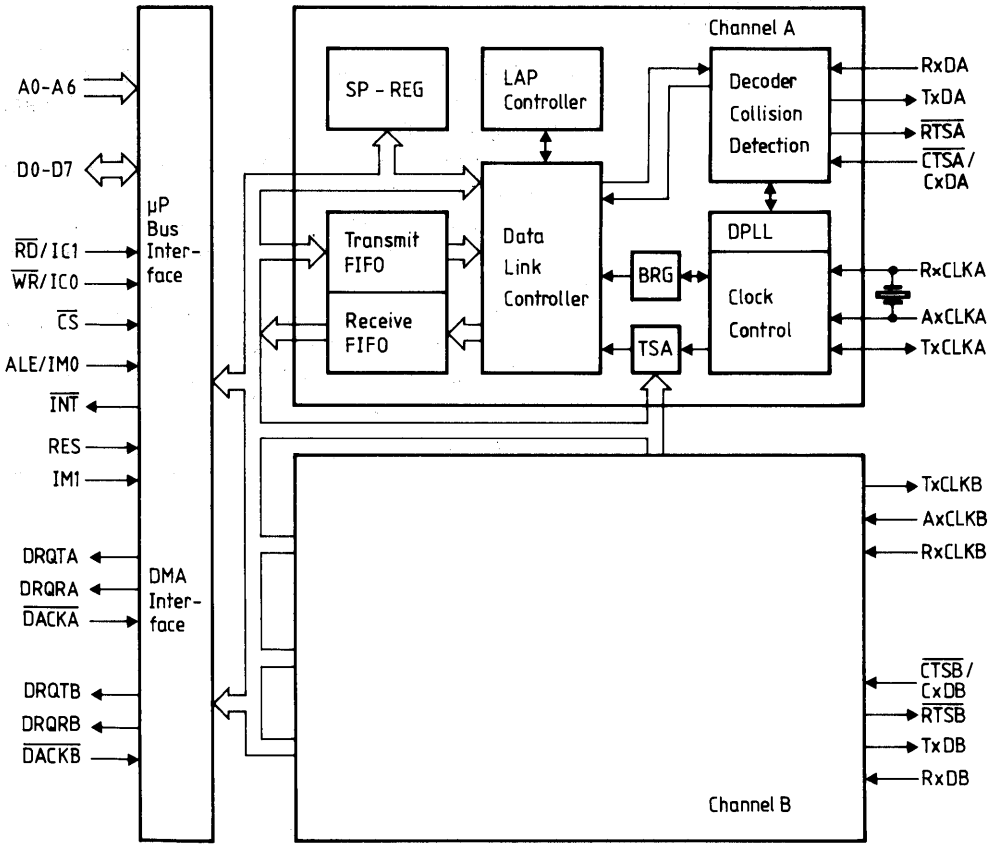
Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
36 32	TxCLKA TxCLKB	I/O	**Transmit Clock** (channel A/channel B) The functions of these pins depend on the programmed clock mode, provided that the TSS bit in the CCR2 register is reset. Programmed as inputs (if the TIO bit in CCR2 is reset), they may supply either – the transmit clock for the respective channel (clock mode 0, 2, 6), – or a transmit strobe signal (clock mode 1). Programmed as outputs (if the TIO bit in CCR2 is set), the TxCLK pins supply either the – transmit clock of the respective channel which is generated either ● from the baud rate generator (clock mode 2, 6; TSS bit in CCR2 set), ● or from the DPLL circuit (clock mode 3, 7), ● or from the cristal oscillator (clock mode 4) – or a tristate control signal indicating the programmed transmit time slot (clock mode 5).
35 33	RxCLKA RxCLKB	I	**Receive Clock** (channel A/channel B) The functions of these pins also depend on the programmed clock mode. In each channel, RxCLK may supply either – the receive clock (clock mode 0) – or the receive and transmit clock (clock mode 1, 5) – or the clock for the baud rate generator (clock mode 2, 3), – or a crystal connection for the internal oscillator (clock mode 4, 6, 7, RxCLKA/B together with AxCLKA)
39 37	DRQRA DRQRB	O	**DMA Request Receiver** (channel A/channel B) The receiver of the HSCX requests a DMA data transfer by activating this line. The DRQRn remains high as long as the receive FIFO requires data transfers, thus always blocks of data (32, 16, 8 or 4 bytes) are transfered. DRQRn is deactivated immediately following the falling edge of the last read cycle.

Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
40 38	DRQTA DRQTB	O	**DMA Request Transmitter** (channel A/channel B) The transmitter of the HSCX requests a DMA data transfer by activating this line. The DRQTn remains high as long as the transmit FIFO requires data transfers. The amount of data bytes to be transfered from system memory to the HSCX (= byte count) must be written first to the XBCH, XBCL registers. Always blocks of data (n * 32 bytes + REST, n = 0,1,...) are transfered till the byte count is reached. DRQTn is deactivated immediately following the falling edge of the last $\overline{WR}$ cycle.
41	V_{DD}	I	Power +5 V power supply.

Block Diagram SAB 82525/SAB 82526



The HSCX SAB 82526 comprises one (channel B), the SAB 82525 two completely independent full-duplex HDLC channels (channel A and channel B), supporting various layer-1 functions by means of internal oscillator, Baud Rate Generator (BRG), Digital Phase Locked Loop (DPLL), and Time-Slot Assignment (TSA) circuits.

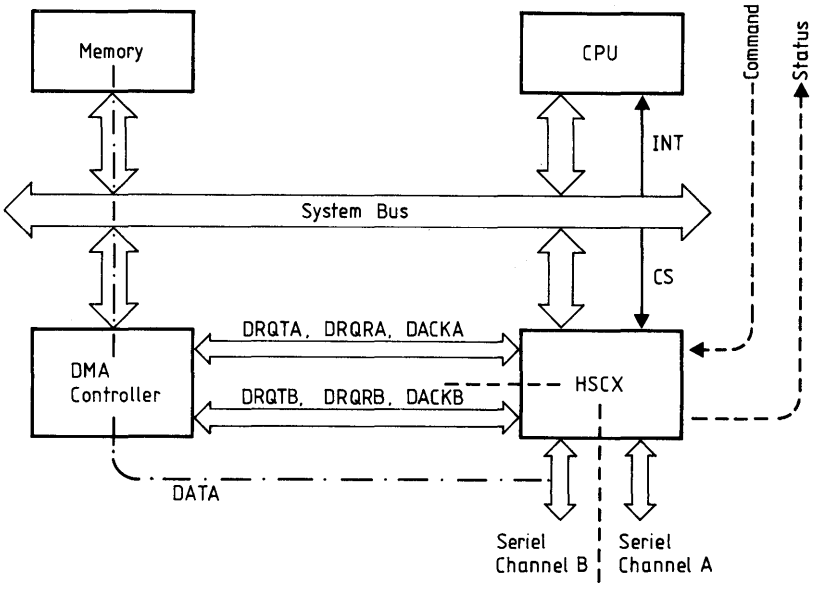
Furthermore, layer-2 functions are performed by an on-chip LAP (Link Access Procedure, e.g. LAP B or LAP D) controller.

System Integration

General Aspects

Figure 1 gives a general overview of the system integration of HSCX.

Figure 1
General System Integration of HSCX



The HSCX bus interface consists of an 8-bit bidirectional data bus (D0 – D7), seven address line inputs (A0 – A6), three control inputs ($\overline{RD}$/DS, $\overline{WR}$/R/W, $\overline{CS}$), one interrupt request output (INT) and a 4-channel DMA interface (DRQTA, DRQRA, DACKA, DRQTB, DRQRB, DACKB). Mode input pins (strapping options) allow the bus interface to be configured for either SIEMENS/INTEL or Motorola environment.

Generally, there are two types of transfers occuring via the system bus:

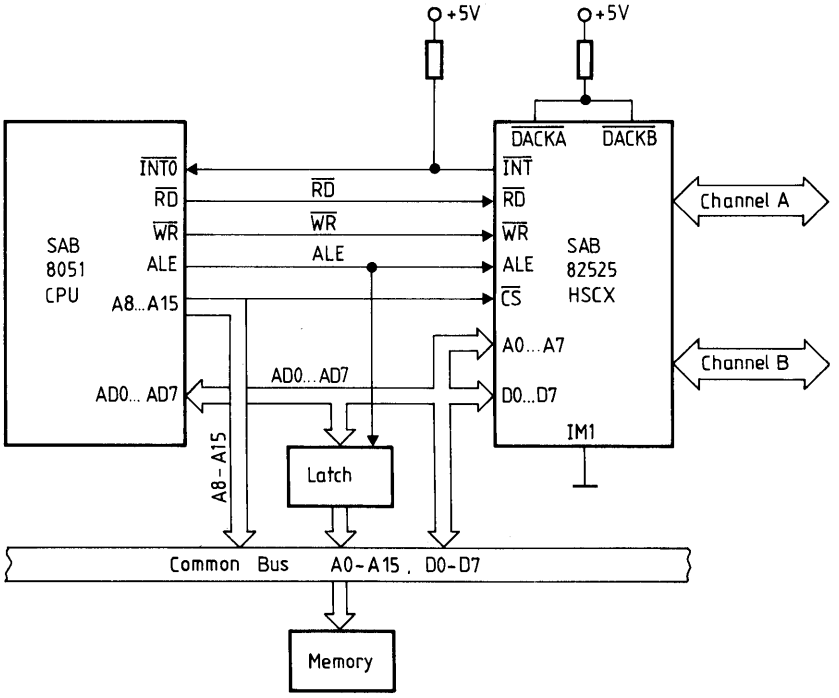
- command/status transfers, which are always controlled by the CPU. The CPU sets the operation mode (initialization), controls function sequences and gets status information by writing or reading the HSCX's registers (via $\overline{CS}$, $\overline{WR}$ or $\overline{RD}$, and register address via A0-A6).
- data transfers, which are effectively performed by DMA without CPU interaction using the HSCX's DMA interface (DMA Mode). Optionally, interrupt controlled data transfer can be done by the CPU (interrupt mode).

Specific Applications

HSCX with SAB 8051 Microcontroller

For cost-sensitive applications, the HSCX can be interfaced with a small SAB 8051 microcontroller system (without DMA support) very easily as shown in **figure 2.**

Figure 2
HSCX with 8051 CPU



Although the HSCX provides a demultiplexed bus interface, it can optionally be connected directly to the local multiplexed bus of SAB 8051 because of the internal address latch function (via ALE, compatibility to SAB 82520 HSCC).

The address lines A0 . . . A6 must be wired externally to the data lines D0 . . . D6 (direct connection) in this case.

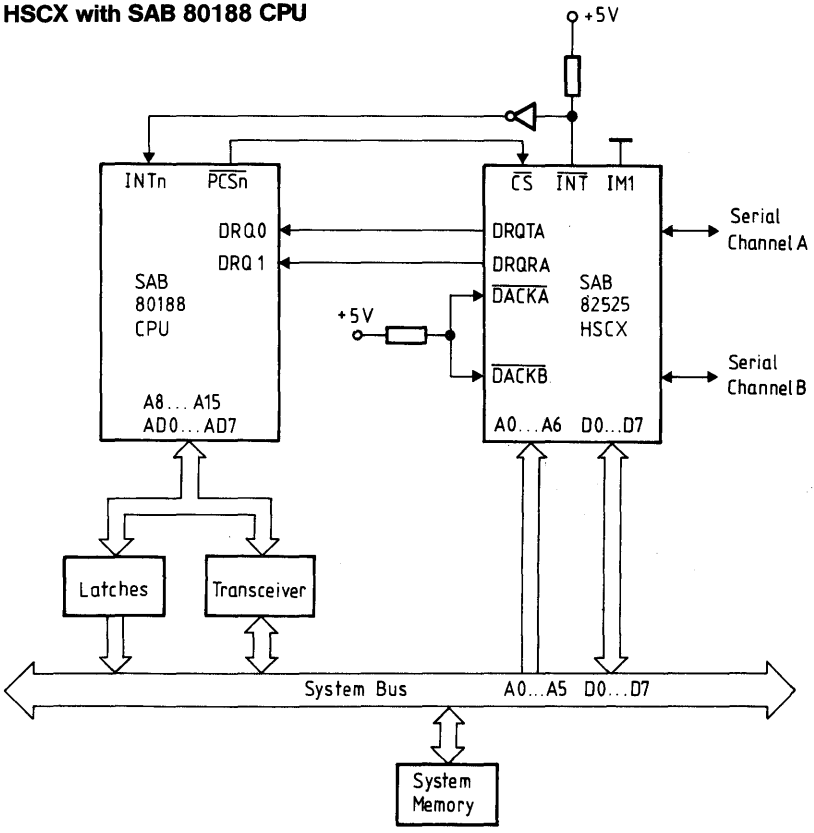
Intel bus mode is selected connecting IM1 pin to low (V_{SS}). Since data transfer is controlled by interrupt, the DMA acknowledge inputs (DACKA, DACKB) are connected to V_{DD} (+5 V).

HSCX with SAB 80188 Microprocessor

A system with minimized additional hardware expense can be with a SAB 80188 microprocessor as shown in **figure 3.**

Figure 3

HSCX with SAB 80188 CPU



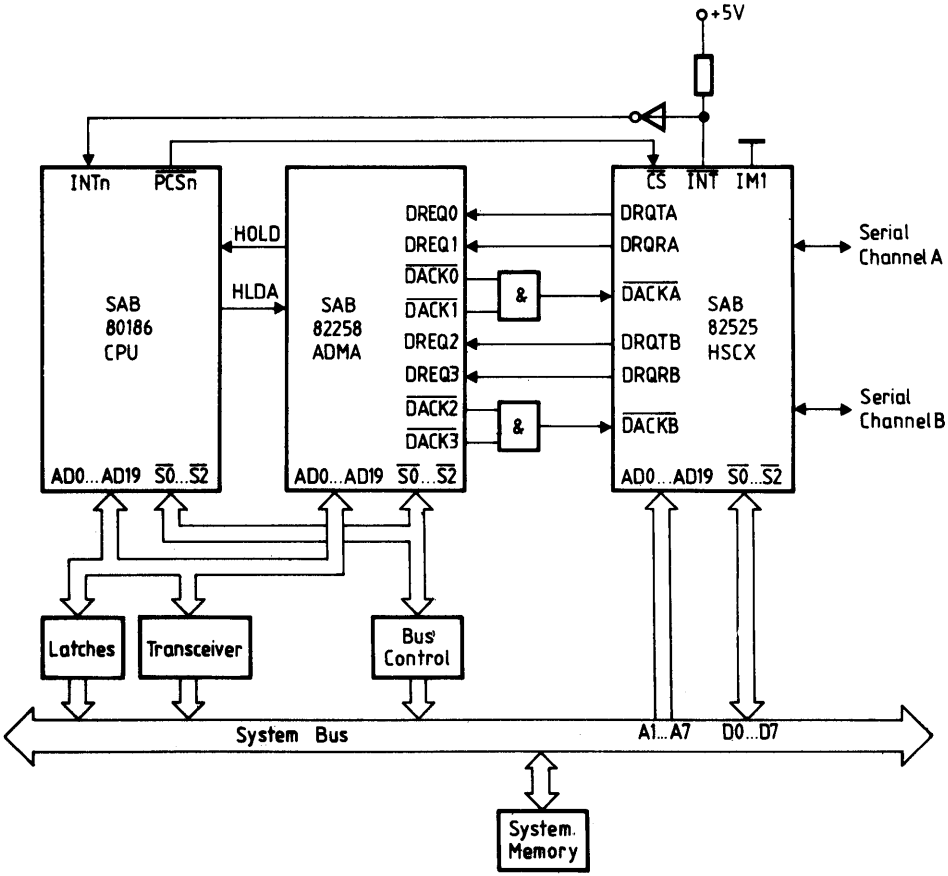
The HSCX is connected to the demultiplexed system bus. Data transfer for one serial channel can be done by the 2-channel on-chip DMA controller of the SAB 80188, the other channel is serviced by interrupt. Since the SAB 80188 does not provide DMA acknowledge outputs, data transfer from/to HSCX is controlled via CS, RD or WR address information (A0...A6) and the DACKA, DACKB inputs are not used.

This solution supports applications with a high speed data rate in one serial channel with minimum hardware expense making use of the on-chip peripheral functions of the SAB 80188 (chip select logic, interruptcontroller, DMA controller).

HSCX with SAB 80186 Microprocessor and SAB 82258 Advanced DMA Controller (ADMA)

In applications, where two high-speed channels are required, a 16-bit system with SAB 80186 CPU and SAB 82258 ADMA is suitable. This shown in **figure 4.**

Figure 4
HSCX with SAB 80186 CPU/SAB 82258 ADMA



The four selector channels of ADMA are used for serving the four DMA request sources of HSCX, allowing very high data rates at both the system bus and the serial channels.

Another big advantage of the ADMA is it's data chaining feature, providing an optimized memory management for receive and transmit data. Recording the HSCX, a linked chain of 32 byte deep buffers can be set up, which are subsequently filled with the contents of the HSCX's FIFOS during reception. Not used buffers can be saved and linked to another buffer chain reserved for the reception of the next frame.

As a result, it's not necessary to reserve a very large space in system memory, determined by the maximum frame length of every received frame.

In this example, the ADMA works directly at the CPU's local bus and shares the same bus interface logic (address latches, transceivers, bus controller) with the SAB 80186. Since one DMA acknowledge line is provided for each DMA request, two $\overline{\text{DACK}}$ outputs must be ANDed together for input to the HSCX.

The HSCX's data lines are connected to the lower half of the system data bus (D0...D7) and the address lines to A1...A7, thus (from the CPU's point of view) all internal register addresses must be multiplied by two (even register addresses only).

e.g. CMDR register: HSCX address 61_H <=> system address $C2_H$.

Functional Description

General

The HSCX distinguishes from other low level HDLC devices by its advanced characteristics. The most important are:

- Enlarged support of link configurations.

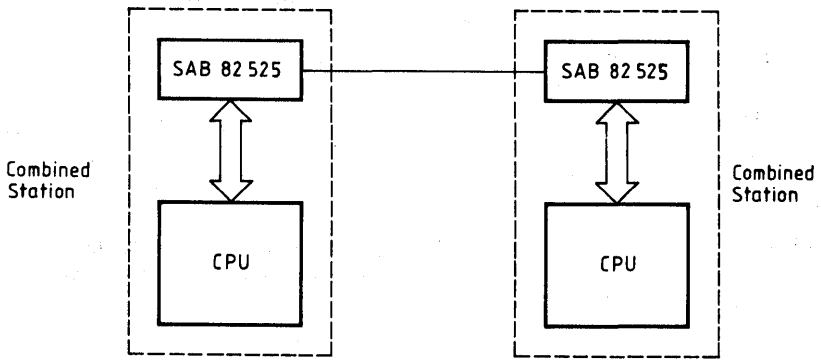
Beyond the point-to-point configurations, the HSCX directly enables point-to-multipoint or multimaster configurations without additional hardware or software expense.

In point-to-multipoint configurations, the HSCX can be used as a master as well as a slave station. Even when working as slave station, the HSCX can initiate the transmission of data at any time. An internal function block provides means of idle and collision detection and collision resolution, which are necessary if several stations start transmitting simultaneously.

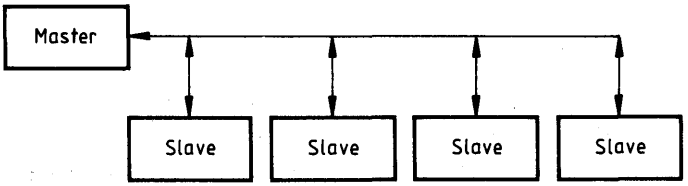
Thus also a multimaster configuration is possible.

Figure 5
Link Configuration

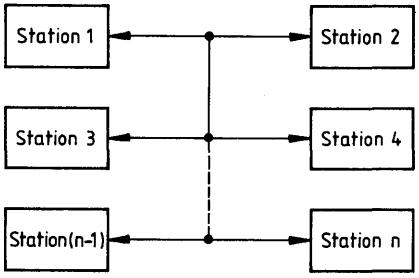
Point-to-Point Configuration



Point-to-Multipoint Configuration



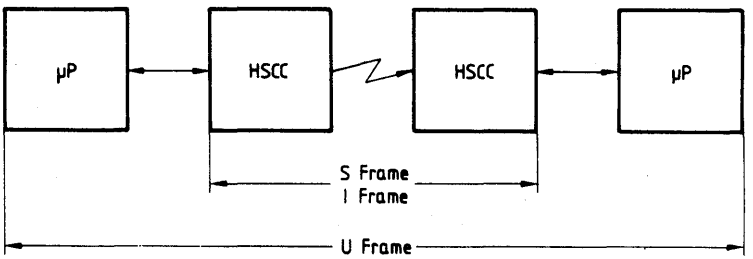
Multimaster Configuration



● Support of layer-2 functions by HSCX

Beside those bit-oriented functions usually supported with the HDLC protocol, such as bit stuffing, CRC check, flag and address recognition, the HSCX provides a high degree of procedural support. In a special operating mode (auto-mode), the HSCX processes the information transfer and the procedure handshaking (I-, and S-frames of HDLC protocol) autonomously. The only restriction is, that the window size (= number of outstanding unacknowledged frames) is limited to 1, which will be sufficient in most applications. The communication procedures are mainly processed between the communication controllers and not between the processors, thus the dynamic load of the CPU and the software expensive is largely reduced.

Figure 6
Procedural Support in Auto-Mode



The CPU is informed about the status of the procedure and has to manage the receive and transmit data mainly. In order to maintain cost effectiveness and flexibility, such functions as link setup/disconnection and error recovery in case of protocol errors (U frames of HDLC protocols) are not implemented in hardware and must be done by user's software.

● Telecomspecific features

In a special operating mode, the HSCX can transmit or receive data packets in one of up to 64 time slots of programmable width (clock mode 5). Furthermore, the HSCX can transmit or receive variable data portions within a defined window of one or more clock cycles, which has to be selected by an external strobe signal (clock mode 1). These features make the HSCX especially suitable for all applications using time division multiplex methods, such as time-slot oriented PCM systems, systems designed for packet switching, or in ISDN applications.

● FIFO buffers to efficient transfer of data packets.

A further speciality of HSCX are the FIFO buffers used for the temporary storage of data packets transfered between the serial communications interface and the parallel system bus. Also because of the overlapping input/output operation (dual- port behaviour), the maximum message length is not limited by the size of the buffer. Together with the DMA capability, the dynamic load of the CPU is drastically reduced by transfering the data packets block by block via direct memory access. The CPU only has to initiate the data transmission by the HSCX and determine the status in case of completely received frames, but is not involved in data transfers.

Operational Description

RESET

The HSCX is forced into the reset state if a high signal is input to the RES pin for a minimum period of 1.8 ms. During RESET, the HSCX is temporarily in the power-up mode, and a subset of the registers is initialized with defined values.

After RESET, the HSCX is in power down mode, and the following registers contain defined values:

Table 1
RESET Values

Register	RESET Value	Meaning
CCR1	00_H	– power down mode serial port configuration; pt-pt, NRZ coding, transmit data pins are open drain outputs – clock mode 0
CCR2	00_H	RTS pin normal function – CTS and RFS interrupts disabled no data inversion
MODE	00_H	auto mode 1 byte address field external timer mode – receivers inactive RTS output controlled by HSCX, timer resolution: k = 32.768, no testloop
STAR	48_H	XFIFO write enable receive line inactive no commands executing
ISTA EXIR	00_H	– no interrupts masked
CMDR	00_H	no commands
XBCH RBCH	00_H	– interrupt controlled data transfer (DMA disabled) – full-duplex LAPB/LAPD operation of LAP controller – carrier detect auto start of receiver disabled
XCCR RCCR	00_H	1-bit time slot

Detailed Register Description

Register Address Arrangement

Table 2
Layout of Register Addresses

ADDRESS		REGISTER		
Channel A	Channel B	Read	Write	
00 ⋮ 1F	40 ⋮ 5F	RFIFO	XFIFO	Receive/Transmit FIFO
20	60	ISTA	MASK	Interrupt STAtus/Mask
21	61	STAR	CMDR	STAtus/CoMnaD
22	62	MODE		MODE
23	63	TIMR		TIMer
24	64	EXIR	XAD1	EXtended Interrupt/Transmit ADdress 1
25	65	RBCL	XAD2	Receive Byte Count Low/Transmit ADdress 2
26	66	–	RAH1	Receive Address High 1
27	67	RSTA	RAH2	Receive STAtus/Rec. Addr. High 2
28	68	RAL1		Receive Address Low 1
29	69	RHCR	RAL2	Receive HDLC Control/Receive Addr. Low 2
2A	6A	–	XBCL	Transmit Byte Count Low
2B	6B	–	BGR	Baudrate Generator Register
2C	6C	CCR2		Channel Configuration Register 2
2D	6D	RBCH	XBCH	Reveive/Transmit Byte Count High
2E	6E	VSTR	RLCR	Version STatus/Receive frame Length Check
2F	6F	CCR1		Channel Configuration Register 1
30	70	–	TSAX	Time-Slot Assignment Transmit
31	71	–	TSAR	Time-Slot Assignment Receive
32	72	–	XCCR	Transmit Channel Capacity
33	73	–	RCCR	Receive Channel Capacity

Note: Channel A is not implemented in SAB 82526

Register Definitions

Receive FIFO (Read) RFIFO (00...1F/40...5F)

- Interrupt Controlled Data Transfer (Interrupt Mode)
  selected if DMA bit in XBCH is reset.

Up to 32 bytes of receive data can be read from the RFIFO following an RPF or an RME interrupt.

RPF Interrupt: Exactly 32 bytes to be read.
RMA Interrupt: Number of bytes to be determined by reading the RBCL, RBCH registers.

- DMA Controlled DataTransfer (DMA Mode)
  selected if DMA bit in XBCH

If the RFIFO contains 32 bytes, the HSCX autonomously requests a block data transfer by DMA activating the DRQR line as long as the start of the 32nd read cycle. This forces the DMA controller to continously perform bus cycles till 32 bytes are transfered from the HSCX to the system memory. (level triggered, demand transfer mode of DMA controller).

If the RFIFO contains less than 32 bytes (one short frame or the last of a long frame) the HSCX requests a block data transfer depending on the contents of the RFIFO according to the following table:

RFIFO Contents (Bytes)	**DMA Request (Bytes)**
(1) 2, 3	4
4–7	8
8–15	16
16–32	32

Additionally an RME interrupt is issued after the last byte has been transfered.

As a result, the DMA controller may transfer more bytes as actually valid in the current received frame. The valid byte count must therefore be determined reading the RBCH, RBCL registers following the RME interrupt.

Transmit FIFO (WRITE) XFIFO (00...1F/40...5F)

- Interrupt Mode
  selected if DMA bit in XBCH is reset.

Up to 32 bytes of transmit data can be written to the XFIFO following an XPR interrupt.

- DMA Mode
  selected if DMA bit in XBCH is set.

Prior to any data transfer, the actual byte count of the frame to be transmitted must be written to the XBCH, XBCL registers by the user.

If data transfer is then initiated via the CMDR register (command XTF or XIF), the HSCX autonomously requests the correct amount of block data transfers (n*32+REST, n=0,1, . . .).

Note: Addresses within the address space of the FIFO's are interpreted equally, i.e. the actual data byte can be accessed with any address within the valid scope.

Interrupt Status Register (READ)

	7							0	
IST A	REM	RPF	RSC	XPR	TIN	ICA	EXA	EXB	(20/60)

Value after RESET: 00_H

RME . . . Receive Message End

One message up to 32 bytes or the last part of a message greater then 32 bytes has been received and is now available in the RFIFO. The message is complete!
The actual message lengh can be determined reading the RBCH, RBCL registers.
Additional information is available in the RSTA register.

RPF . . . Receive Pool Full

A block of 32 bytes of a message is stored in the RFIFO. The message is not yet completed!
Note: This interrupt is only generated in interrupt Mode!

RSC . . . Receive Status Change (significant in auto mode only!)

A status change (receiver ready/receiver not ready) of the opposite station has been detected in auto mode. (i.e. the HSCX has received a RR/RNR supervisory frame according to the HDLC protocol.) The current status can be read from the STAR register (RRNR bit).

XPR . . . Transmit Pool Ready

A data block of up 32 bytes can be written to the transmit FIFO.

TIN . . .Timer Interrupt

The internal timer and repeat counter has been expired. (See also description of TIMR register!)

ICA . . . Interrupt of Channel A (Channel B only)

Indicates, that an interrupt is caused by channel A and the interrupt source(s) is (are) indicated in the ISTA register of channel A (i.e. at least one bit of the ISTA register of channel A is set).

EXA . . . Extended Interrupt of Channel A (Channel B only)

An interrupt is caused by channel B and source(s) is (are) indicated in the EXIR register of channel B.

Note: The ICA, EXA, and EXB bit are present in channel B only and point to the ISTA (CHA), EXIR (CHA), and EXIR (CHB) registers.

After the HSCX has requested an interrupt by turning its INT pin to low, the CPU must first read the ISTA register of channel B and check the state of these bits in order to determine which interrupt source(s) of which channel(s) has caused the interrupt. More than one interrupt source may be indicated by a single interrupt request.

After the respective register has been read, EXA, and EXB are reset. All other bits will be reset after reading ISTA. To prevent malfunctions, each bit is individually monitored and reset.

Mask Register (WRITE)

	7							0	
MASK	RME	RPF	RSC	XPR	TIN	ICA	EXA	EXB	(20/60)

Value after RESET: 00_H (all interrupts enabled)

Each interrupt source can be selectively masked by setting the respective bit in MASK (bit positions corresponding to ISTA register). Masked interrupts are not indicated when reading ISTA. Instead, they remain internally stored and will be indicated after the respective MASK bit is reset.

Note: In the event of an extended interrupt, no interrupt request will be generated with a masked EXA, EXB bit, although this bit is set in ISTA.

Extended Interrupt Register (READ)

Value after RESET: 00_H

	7							0	
EXIR	XMR	XDU EXE	PCE	RFO	CSC	RFS	0	0	(24/64)

XMR . . . Transmit Message Repeat

The transmission of the last message has to be repeated because

– the HSCX has received a negative acknowledgment in auto mode,

– or a collision has occured after sending the 32nd data byte of a message in a bus configuration.

– or CTS (transmission enable) has been withdrawn after sending the 32nd data byte of a message in point-to-point configuration.

XDU/EXE . . . Transmit Data Underrun/Extended Transmission End

The actual frame has been aborted with IDLE, because the XFIFO holds no further data, but the frame is not yet complete!

In extended transparent mode, this bit indicates the transmission-end condition.

Note: It is not possible to send transparent-, or I-frames when a XMR or XDU interrupt is indicated.

PCE . . . Protocol Error (significant in auto mode only!)

The HSCX has detected a protocol error, i.e. it has received

– an S-, or I-frame with incorrect N (R)

– an S-frame containing an I-field.

RFO . . . Receive Frame Overflow

One frame could not be stored due to occupied RFIFO (i.e. whole frame has been lost). This interrupt can be used for statistical purposes and indicates, that the CPU does not respond quickly enough to an incoming RPF, or RME interrupt.

CSC . . . Clear To send Status Change

Indicates, that a state transition has occured at the CTS pin. The actual state can be read from STAR register (CTS bit)

This interrupt must be enabled setting the CIE bit in CCR2.

RFS . . . Receive Frame Start

This is an early receiver interrupt activated after the start of a valid frame has been detected, i.e. after a valid address check in operation modes providing address recognition, otherwise after the opening flag (transparent mode 0), delayed by two bytes.

After an RFS interrupt, the contents of

- RHCR
- RAL1
- RSTA – bit 3-0

  are valid and can be read by the CPU.

This interrupt must be enabled setting the RIE bit in CCR2.

Status Register (READ)

Value after RESET: 48_H

	7							0	
STAR	XDOV	XFW	XRNR	RRNR	RLI	CEC	CTS	WFA	(21/61)

XDOV . . . Transmit Data Overflow

More than 32 bytes have been written to the XFIFO.

XFW . . . Transmit FIFO Write Enable

Data can be written to the XFIFO.

XRNR . . . Transmit RNR (significant in auto mode only!)

Indicates the status of the HSCX.

0 . . . receiver ready

1 . . . receiver not ready

RRNR . . . Received RNR (significant in auto mode only!)

Indicates the status of the remote station.

0 . . . receiver ready

1 . . . receiver not ready

RLI . . . Receive Line Inactive

Neither FLAGs as interframe time fill nor frames are received via the receive line.

Note: Significant in point-to-point configurations!

CEC . . . Command Executing

0 . . . no command is currently executed, the CMDR register can be written to.

1 . . . a command (written previously to CMDR) is currently executed, no further command can be temporarily written via CMDR register.

Note: CEC will be active at most 2.5 transmit clock periods. If the HSCX is in power down mode CEC will stay active.

CTS . . . Clear To Send State

If the CIE bit in CCR2 is set, this bit indicates the state of the CTS pin.

0 . . . CTS is inactive (high signal at CTS)

1 . . . CTS is active (low signal at CTS)

WFA . . . Waiting For Acknowledgement (significant in auto mode only).

Indicates the 'Waiting for Acknowledgement' status of HSCX.

Command Register (WRITE)

Value after RESET: 00_H

	7							0	
CMDR	RMC	RHR	RNR XREP	STI	XTF	XIF	XME	XRES	(21/61)

RMC . . . Receive Message Complete

Confirmation from CPU to HSCX, that the actual frame or data block has been fetched following an RPF or RME interrupt, thus the occupied space in the RFIFO can be released.

Note: In DMA mode, this command is only issued once after a RME interrupt. The HSCX does not generate further DMA requests prior to the reception of this command.

RHR . . . Reset HDLC Receiver

All data in the RFIFO and the HDLC receiver deleted.

In auto mode, additionally the transmit and receive sequence number counters are reset.

RNR/XREP . . . Receiver Not Ready/Transmission Repeat

The function of this command depends on the selected operation mode (MDS1, MDS0, ADM bit in MODE):

- Auto mode: RNR

The status of the HSCX receiver is set. Determines, whether a received frame is acknowled via an RR, or RNR supervisory frame in auto mode.

0 . . . Receiver Ready (RR)

1 . . . Receiver Not Ready (RNR)

- Extended transparent mode 0,1: XREP

Together with XTF and XME set (write $2A_H$ to CMDR), the HSCX repeatedly transmits the contents of the XFIFO (1 . . . 32 bytes) without HDLC framing fully tranparent, i.e. without FLAG, CRC insertion, bit stuffing.

The cyclic transmission is stopped with an XRES command!

STI . . . Start Timer

The internal timer is started.

Note: The timer is stopped by rewriting the TIMR register after start.

XTF . . . Transmit Transparent Frame

- Interrupt mode

After having written up to 32 bytes the XFIFO, this command initiates the transmission of a transparent frame. An opening flag sequence is automatically added to the data by the HSCX.

- DMA mode

After having written the length of the frame to be transmitted to the XBCH, XBCL registers, this command initiates the data transfer form system memory to HSCX by DMA. Serial data transmission starts as soon as 32 bytes are stored in the XFIFO.

XIF . . . Transmit I-Frame (used in auto mode only!)

Initiates the transmission of an I-frame in auto mode. Additional to the opening flag sequence, the address and control field of the frame is automatically added by HSCX.

XME . . . Transmit Message End (used in interrupt mode only!)

Indicates, that the data block written last to the transmit FIFO completes the actual frame. The HSCX can terminate the transmission operation properly by appending the CRC and the closing flag sequence to the data.

In DMA mode, the end of the frame is determined by the transmit byte count in XBCH, XBCL!

XRES . . . Transmit Reset

The contents of the XFIFO is deleted and IDLE is transmitted. This command can be used by the CPU to abort a frame currently in transmission. After setting XRES an XPR interrupt is generated in every case.

Note: The maximum time between writing to the CMDR register and the execution of the command is 2.5 clock cycles. Therefore, if the CPU operates with a very high clock in comparison with the HSCX's clock, it's recommended that the CEC bit of the STAR register is checked before writing to the CMDR register to avoid any loss of commands.

Mode Register (READ/WRITE)

Value after RESET: 00_H

	7							0	
MODE	MDS1	MDS0	ADM	TMD	RAC	RTS	TRS	TLP	(22/62)

MDS1, MDS0 . . . Mode Select

The operating mode of the HDLC controller is selected.

00 . . . auto mode
01 . . . non-auto mode
10 . . . transparent mode
11 . . . extended transparent mode

ADM . . . Address Mode

The meaning of this bit varies depending on the selected operating mode:

● Auto mode, non-auto mode

Defines the length of the HDLC address field.

0 . . . 8-bit address field

1 . . . 16-bit address field

In transparent modes, this bit differentiates between two sub-modes:

● Transparent mode

0 . . . transparent mode 0; no address recognition.

1 . . . transparent mode 1; high byte address recognition.

● Extended transparent mode; without HDLC framing.

0 . . . extended transparent mode 0

1 . . . extended transparent mode 1

Note: In extended transparent modes, the RAC bit must be reset to enable fully transparent reception!

TMD . . . Timer Mode

The operation mode of the internal timer is set.

0 . . . external mode

The timer is controlled by the CPU and can be started at any time setting the STI bit in CMDR.

1 . . . internal mode

The timer is used internally by the HSCX for timeout and retry conditions in auto-mode. (refer to the description of the TIMR register)

RAC . . . Receiver Active

Switches the receiver to inoperational state.

0 . . . receiver inactive

1 . . . receiver active

In extended transparent modes this bit must be reset to enable fully transparent reception!

RTS . . . Request To Send

Defines the state and control of RTS pin.

0 . . . The RTS pin is controlled by the HSCX autonomously.

RTS is activated when a frame transmission starts and deactivated after the transmission operation is completed.

1 . . . The RTS pin is controlled by the CPU.

If this bit is set, the RTS pin is activated immediately and remains active till this bit is reset.

TRS . . . Timer Resolution

The resolution of the internal timer (factor *k*, see description of TIMR register) is selected

0 . . . $k = 32.768$

1 . . . $k = 512$

TLP . . . Test Loop

Input and output of the HDLC channels are intenally connected (transmitter channel A – receiver channel A/ transmitter channel B – receiver channel B)

Timer Register (READ/WRITE)

	7	5	4	0	
TIMR	CNT		VALUE		(23/63)

VALUE . . . Sets the time period t_1 as follows:

$t_1 = k$ x (VALUE + 1) x TXP

where

– *k* is the timer resolution factor which is either 32.768 or 512-clock cycles dependent on the programming of TRS bit in MODE.

– TCP is the clock period of transmit data.

CNT . . . Interpreted differently dependent on the selected timer mode (bit TMD in MODE).

● Internal timer mode (MODE.TMD = 1)

– retry counter (in HDLC known as N2)

CNT indicates the number of S-commands (max. 6) which are transmitted autonomously by the HSCC after expiration of time period t_1, in case an I-frame is not acknowledged by the opposite station.

If CTN is set to 7, the number of S-commands is unlimited.

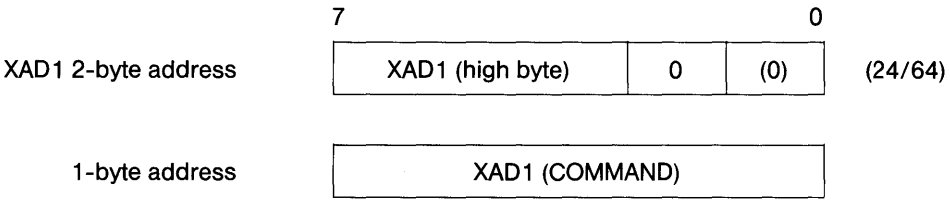
● External timer mode (MODE, TMD = 0)

CNT plus VALUE indicates the time period t2 after which a timer interrupt will be generated. The time period t_2 is

$t_2 = 32$ x k x CNT x TCP + 11

If CTN is set to 7, a timer interrupt periodically generated after the expiration of t_1.

Transmit Address Byte 1 (WRITE)



XAD1 (and XAD2) can be programmed with one individual address byte which is appended automatically to the frame by HSCX in auto mode. The function depends on the selected address mode (bit ADM in MODE).

– 2-byte address field (MODE. ADM = 1)

XAD1 builds up the high byte of the 2-byte address field. Bit 1 must be set to 0! According to the ISDN LAP D protocol, bit 1 is interpreted as the C/R (COMMAND/RESPONSE) bit. This is manipulated automatically by the HSCX dependet on the setting of the CRI bit in RAH1:

	Bit 1 (C/R)	
Commands transmit	1	0
Responses transmit	0	1
	CRI = 1	CRI = 0

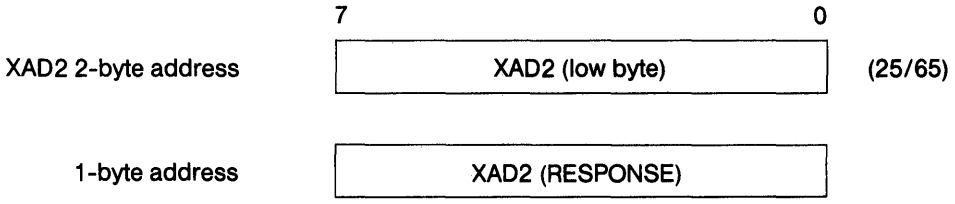
(In the ISDN, the high address byte is known as SAPI).

In accordance with the HDLC protocol, bit 0 should be set to 0, indicating the extension of the address field to two bytes.

– 1-byte address field (MODE.ADM = 0)

According with the X.25 LAP B protocol, XAD1 indicates a COMMAND.

Transmit Address Byte 2 (WRITE)



Second individually programmable address byte.

– 2-byte address (MODE.ADM = 1)

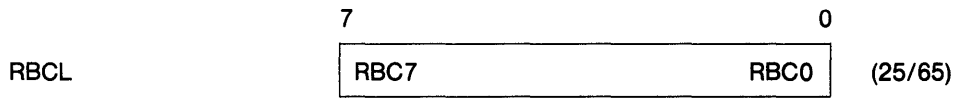
  XAD2 builds up the low byte of the 2-byte address field
  (In the ISDN, the low address byte is known as TEI)

– 1-byte address (MODE.ADM = 0)

  According to the X.25 LAP B protocol, XAD2 indicates a RESPONSE,

Note: XAD1, XAD2 registers are used only if the HSCX is operated in auto-mode.

Receive Byte Count Low (READ)



Together with RBCH (bits RBC11 – RBC8), the length of the actual received frame (1 . . . 4095 bytes) can be determined. These registers must be read by the CPU following a RME interrupt.

Receive Address Byte High Register 1 (WRITE)

	7			0	
RAH1	RAH1		CRI	0	(26/66)

In operating modes that provide high byte address recognition, the high byte of the received address is compared with the individual programmable values in RAH1, or RAH2.

RAH1 . . . Value of the first individual high address byte

CRI . . . Command/Response Interpretation
The setting of the CRI bit affects the meaning of the C/R bit in RSTA as follows:

C/R meaning	C/R value	
Commands received	0	1
Responses received	1	0
	CRI = 1	CRI = 0

Important: If the 1 byte address field is selected in auto mode, RAH1 must be set to 00_H.

Receive Address Byte High Register 2 (WRITE)

	7			1	0	
RAH2	RAH2			MCS	0	(27/67)

RAH2 . . . Value of second individual programmable high address byte.

MCS . . . – Module Count Select –; valid in auto mode only.

The MCS bit adjusts the control field format according to the HDLC (ISDN/LAPD).

0 . . . basic operation (modulo 8)

1 . . . extended operation (modulo 128)

Note: When modulo 128 is selected, in auto mode the "RHCR" register contains compressed information of the extended control field (see RHCR, register description). RAH1, RAH2 registers are used in auto- and non-auto operating modes when a 2-byte address field has been selected (MODE.ADM = 1) and in the transparent mode 0.

Receive Status Register (READ)

	7							0	
RSTA	VFR	RDO	CRC	RAB	HA1	HA0	C/R	LA	(2)/67)

VFR . . . Valid Frame

Determines whether a valid frame has been received.

1 . . . Valid

0 . . . Invalid

An invalid frame is either

– a frame which is not an integer number of 8 bits (n * 8 bits) in length (e.g. 25 bit), or

– a frame which is too short depending on the selected operation mode via MODE (MDS1, MDS0, ADM) as follows:

- Auto-/non-auto mode (16-bit address): 4 bytes
- Auto-/non-auto mode (8-bit address): 3 bytes
- Transparent mode 1:3 bytes.
- Transparent mode 0:2 bytes.

Note: Shorter frames are not reported.

RDO . . .Receive Data Overflow

A data overflow has occured within the actual frame.

CRC . . . CRC compare/check

0 . . . CRC check failed; received frame contains errors.
1 . . . CRC check o.k.; received frame is error-free.

RAB . . . Receive Message Aborted

The received frame was aborted from the transmitting station.
According to the HDLC protocol, this frame must be discarded by the CPU.

HA1, HA0 . . . High Byte Address Compare; significant only if 2-byte address mode has been selected.

In operating modes which provide high byte address recognition, the HSCX compares the high byte of a 2-bytes address with the contents of two individual programmable registers (RAH1, RAH2) and the fixed values FE_H and FC_H (group address).

Dependent on the result of this comparison, the following bit combinations are possible:
10 . . . RAH1 has been recognized
00 . . . RAH2 has been recognized
01 . . . group address has been recognized

Note: If RAH1, RAH2 contain the identical values, the combination 00 will be omitted.

C/R . . . Command/Response; significant only, if 2-byte address mode has been selected.

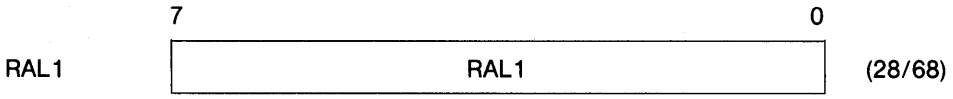
Value of the C/R bit (bit of high address byte) in the received frame. The interpretation depends on the setting of the CRI bit in the RAH1 register. Refer also to the description of RAH1 register.

LA . . . Low Byte Address Compare; not significant in transparent and extended transparent operating modes.

The low byte address of a 2-byte address field, or the single address byte of a 1-byte address field is compared with two programmable registers (RAL1, RAL2)
0 . . . RAL2 has been recognized
1 . . . RAL1 has been recognized
According to the X.25 LAP B protocol, RAL1 is interpreted as COMMAND and RAL2 interpreted as RESPONSE.

Note: RSTA corresponds to the last received HDLC fram; it is duplicated into RFIFO for every frame (last byte of frame).

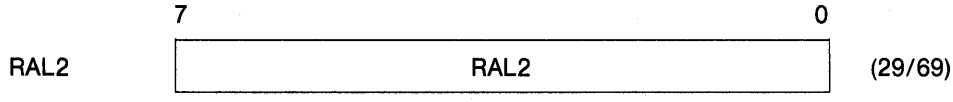
Receive Address Byte Low Register 1 (READ/WRITE)



The general function (READ/WRITE) and the meaning or contents of this register depends on the selected operating mode:

- Auto-/non-auto mode (16-bit address) – WRITE:
  RAL1 can be programmed with the value of the first individual low address byte.
- Auto-/non-auto mode (8-bit address) – WRITE:
  According to X.25 LAP B protocol, the address in RAL1 is recognized as COMMAND address.
- Transparent mode 1 (high byte address recognition) – READ:
  RAL1 contains the byte following the high byte of the address in the receive frame (i.e. the second byte after the opening flag).
- Transparent mode 0 (no address recognition) – READ:
  RAL1 contains the first byte after the opening flag (first byte of received frame).
- Extended transparent modes 0,1 – READ:
  RAL1 contains the actual data byte currently assembled at the RxD pin, by passing the HDLC receiver (fully transparent reception without HDLC framing).

Receive Address Byte Low Register 2 (WRITE)



Value ot the second individual programmable low address byte. If a one byte address field is selected, RAL2 is recognized as RESPONSE according to X.25 LAP B protocol.

Receive HDLC Control Register (READ)

	7		0	
RHCR	RHCR			(29/69)

Value of the HDCL control field of the last received frame.

Note: RHCR is duplicated into RFIFO for every frame.

Transmit Byte Count Low (WRITE)

	7		0	
XBCL	XBC7		XBC0	(2A/6A)

Together with XBCH (bits XBC11 . . . XBC8) this register is used in DMA mode only, to programm the length (1 . . . 4095 bytes) of the next frame to be transmitted.
This allows the HSCX to request the correct amount of DMA cycles after an XTF or XIF command via CMDR.

Baud Rate Generator Register (WRITE)

	7		0	
BGR	BR7		BR0	(2B/6B)

BR7 – BR0 . . . Baude Rate, bit 7-0

Together with bits BR9, BR8 of CCR2, the division factor of the baud rate generator is adjusted.
Dependent on the programmed value N in BR9 – BR8 (N = 0 . . . 1023), the division factor *k* results as follows:

$$k = (N+1) \times 2$$

Channel Configuration Register 2 (READ/WRITE)

Value after RESET: 00_H

The meaning of the individual bits in CCR2 depends on the selected clock mode via CCR1 as follows:

CCR2 clock mode 0,1	SOC1	SOC0	0	0	0	CIE	RIE	DIV	(2C/6C)
clock mode 2,6	BR9	BR8	BDF	TSS	TIO	CIE	RIE	DIV	
clock mode 3,7	BR9	BR8	BDF	0	TIO	CIE	RIE	DIV	
clock mode 5	SOC1	SOC0	XCS0	RCS0	TIO	CIE	RIE	DIV	
clock mode 4	SOC1	SOC0	0	0	TIO	CIE	RIE	DIV	

SOC1, SOC0 . . . Special Output Control

In a bus configuration (selected via CCR1) the function of pin RTS can be defined

0 0 . . . RTS output is activated during the transmission of a frame.

1 0 . . . RTS output is always high (RTS disabled).

1 1 . . . RTS indicates the reception of a data frame (active low).

In point to point configuration (selected via CCR1) the T x D and R x D pins may be flipped

0 X . . . data is transmitted on T x D, received on R x D pin (normal case)

1 X . . . data is transmitted on R x D, received on T x D pin

BR9, BR8 . . . Baud Rate, Bit 9-8 (higher significant bits, refer to description of BGR register).

BDF . . . Baud Rate Division Factor

0 . . . The division factor of the baud rate generator is set to 1 (constant).

1 . . . The division fachtor is adjusted with BR9 – BR0 bits of CCR2 and BRG register.

TSS . . . Transmit Clock Source Select

0 . . . The transmit clock is input to the T x CLKA/T x CLKB pins

1 . . . The transmit clock is derived from the baud rate generators output divided by 16.

TIO . . . Transmit Clock Input Output Switch

0 . . . T x CLKA, T x CLKB pins are inputs

1 . . . T x CLKA, T x CLKB pins are outputs

CIE . . . Clear To Send Interrupt Enable

Any state transition at the CTS input pin may cause an interrupt which is indicated in the EXIR register (CSC bit). The actual state at the CTS pin can be determined reading the CTS bit of the STAR register.

0 . . . disable

1 . . . enable

RIE . . . Receive Frame Start Interrupt Enable

When, the RFS interrupt (via EXIR) is enabled!

DIV . . . Data Inversion

Only valid if NRZ data encoding is selected. Data is transmitted and received inverted.

XCS0, RCS0 . . . Transmit/Receive Clock Shift, Bit 0

Together with bits XCS2, XCS1 (RCS2, RCS1) in TSAX (TSAR) the clock shift relative to the frame synchronization signal of the transmit (receive) time slot can be adjusted.

A clock shift of 0 . . . 7 bits is programmable (clock mode 5 only!).

Transmit Byte Count High (WRITE)

Value after RESET: 000xxxxx

	7				3	0	
XBCH	DMA	NRM	CAS	XC	XBC11	XBC8	(2D/6D)

DMA . . . DMA Mode

Selects the data transfer mode of HSCX to system memory.
0 . . . Interrupt controlled data transfer (interrupt mode)
1 . . . DMA controlled data transfer (DMA mode)

NRM . . . Normal Response Mode

Valid in auto mode only!
Determines the function of the LAP controller:
0 . . . full-duplex LAP B/LAP D operation
1 . . . half-duplex NRM operation

CAS . . . Carrier Detect Auto Start

When set, a high at the CD (AxCLK) pin enables the respective receiver and data reception is started.

XC . . . Transmit Continuously

Only valid if DMA mode is selected!

If the XC bit is set, the HSCX continuously requests for transmit data ignoring the transmit byte count programmed via XBCX, XBCL.

XBC11 . . .XBC8 . . . Transmit Byte Count (most significant bits)

Valid only if DMA mode is selected!
Together with XBC7 . . . XBC0) the length of the frame to be programmed.

Received Byte Count High (READ)

Value after RESET: 000xxxxx

	7				3	0	
RBCH	DMA	NRM	CAS	OV	RBC11	RBC8	(2D/6D)
	see XBCH						

DMA, NRM, CAS . . . These bits represent the read-back value programmed in XBCH (see XBCH!)

OV . . . Counter Overflow

More than 4095 bytes received!
The received frame exceeded the byte count in RBC11 . . . RBC0.

RBC11 . . . RBC8 . . . Receive Byte Count (most significant bits)

Together with RBCL (bits RBC7 . . . RBC0) the length of the received frame can be determined.

Version Status Register (READ)

	7				3	0	
VSTR	CD	0	0	0	VN3	VN0	(2E/6E)

CD . . . Carrier Detect

This bit represents the inverted state at the CD (AxCLK) pin.
1 . . . CD active (LOW)
0 . . . CD inactive (HIGH)

VN3 . . . VN0 . . . Version Number of Chip

0 . . . Version A1
2 . . . Version A2
4 . . . Version A3

Receive Length Check Register (WRITE)

	7							0	
RLCR	RC	RL6						RL0	(2E/6E)

RC . . . Receive Check (on/off)

0 . . . receive length check feature disabled
1 . . . receive length check feature enabled

RL . . . Receive Length

The maximum receive length after which data reception is suspended can be programmed here. Depending on the value RL programmed via RL6 . . . RL0, the receive length is (RL + 1)x32 bytes! A frame exceeding this length is treated as if it was aborted by the opposite station (RME Interrupt, RAB bit set).

In this case, the Receive Byte Count (RBCH, RBCL) is greater than the programmed receive length.

Channel Configuration Register 1 (READ/WRITE)

Value after RESET: 00_H

	7						0	
CCR1	PU	SC1 SC0	ODS	ITF OIN	CM2 CM1 CM0			(2F/6F)

PU . . . Switches between Power Up and Power Down mode

0 . . . power down (standby)
1 . . . power up (active)

SC1, SC0 . . . Serial Port Configuration

00 . . . NRZ data encoding
10 . . . NRZI data encoding
01 . . . bus configuration, timing mode 1
11 . . . bus configuration, timing mode 2

Note: It bus configuration is selected, only NRZ coding is supported.

ODS . . . Output Driver Select

Defines the function of the transmit data pins (TxDA, TxDB)
0 . . . TxD pins are open drain outputs
1 . . . TxD pins are push-pull outputs

ITF/OIN . . . Interface Time Fill/One Insertion

The function of this bit depends on the selected serial port configuration (bit SC1)

- Point-to-point configurations: ITF

Determines the idle (= no data to send) state of the transmit data pins (TxDA, TxDB)
0 . . . Continuous IDLE sequences are output (TxD pins remain in the "1" state)
1 . . . Continuous FLAG sequences are output ("01111110" bit patterns)

- Bus configurations: OIN

In bus configurations, the ITF is implicitly set to 0, i.e. continuous "1"s are transmitted, and data encoding is NRZ!

When this bit is set, a "ONE" insertion (deletion) mechanism is activated, inserting a "1" after seven consecutive"0"s in the transmit data stream or deleting a "1" in the receive data stream.

Similar to the HDLC's bit-stuffing mechanism (inserting a "0" after five consecutive "1"s), this method proves to be advantageous when the receive clock is recovered from the receive data stream by means of DPLL, because it is guaranted that at least after seven bits a transition occurs in the receive data in case of long "0" sequences!

CM2, CM1, CMO . . . Clock Mode

Selects one of the 8 different clock modes

000	clock mode 0
.	.
.	.
.	.
111	clock mode 7

Time-Slot Assignment Register Transmit (WRITE)

This registers is only used in clock mode 5!

	7	2	1	0	
TSAX	TSNX		XCS2	XCS1	(30/70)

TSNX . . . Time-Slot Number Transmit

Selects one of up 64 possible time slots (00_H-$3F_H$) in which data is transmitted. The number of bits per time slot can pe programmed via XCCR.

XCS2, XCS1 . . . Transmit Clock Shift, Bit 2-1

Together with bet XCS0 in CCR2, the transmit clock shift can be adjusted.

Time-Slot Assignment Register Receive (WRITE)

This register is only used in clock mode 5!

	7			0	
TSAR	TSNR		RCS2	RCS1	(31/71)

TSNR . . . Time-Slot Number Receive

Defines one of up to 64 possible time slots (00_H-$3F_H$) in which data is received. The number of bits per time slot can be programmed via RCCR.

RCS2, RCS1 . . . Receive Clock Shift, Bit 2-1

Together with bit RCS0 in CCR2, the receive clock shift can be adjusted.

Transmit Channel Capacity Register (WRITE)

Value after RESET: 00_H

	7		0	
XCCR	XBC7		XBC0	(32/72)

XBC7 . . . XBC0 . . . Transmit Bit Count, Bit 7-0

Defines the number of bits to be transmitted with a time slot:
Number of bits = XBC + 1. (1 . . . 256 bits/time slot)

Receive Channel Capacity Register (WRITE)

	7		0	
RCCR	RBC7		RBC0	(33/73)

Value after RESET: 00_H

RBC7 . . . RBC0 . . . Receive Bit Count, Bit 7-0

Defines the number of bits to be received within a time slot:
Number of bits = RBC + 1. (1 . . . 256 bits/time slot)

Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Ambient temperature under bias: SAB	T_A	0 to 70	°C
SAF	T_A	−40 to 85	°C
Storage temperature	T_{stg}	−65 to 125	°C
Voltage on any pin with respect to ground	V_S	−0.4 to V_{DD} +0.4	V

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

Characteristics

$T_A = 0$ to 70 °C; $V_{DD} = 5\ V \pm 5\%$, $V_{SS} = 0$ V.

Parameter		Symbol	Limit Values min.	Limit Values max.	Unit	Test Conditions
L-input voltage		V_{IL}	−0.4	0.8	V	
H-input voltage		V_{IH}	2.0	V_{CC}+0.4	V	
L-output voltage		V_{OL}		0.45	V	$I_{OL} = 7$ mA (pins TxD, RxD) $I_{OL} = 2$ mA (all other)
H-output voltage		V_{OH}	2.4		V	$I_{OH} = -400\ \mu A$
H-output voltage		V_{OH}	V_{DD}−0.5		V	$I_{OH} = -100\ \mu A$
Power supply current	operational	I_{CC}		8	mA	$V_{DD} = 5$ V, $C_P = 4$ MHz Inputs at 0 V/V_{DD}, no output loads
	power down			1.5	mA	
Input leakage current		I_{LI}		10	µA	0 V < V_{IN} < V_{DD} to 0 V
Output leakage current		I_{LO}				0 V < V_{OUT} < V_{DD} to 0 V

Capacitances

$T_A = 25\,°C$, $V_{DD} = 5\,V \pm 5\%$, $V_{SS} = 0\,V$, $f_C = 1\,MHz$, unmeasured pins returned to GND.

Parameter	Symbol	Limit Values		Unit
		typ.	max.	
Input capacitance $f_C = 1$ MHz	C_{IN}	5	10	pF
Output capacitance	C_{OUT}	10	20	pF
I/O	$C_{I/O}$	8	15	pF

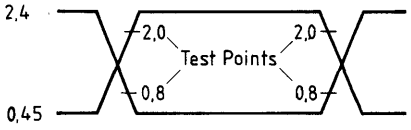
Characteristics

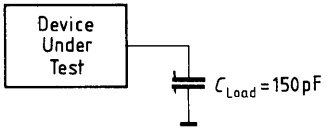
$T_A = 0$ to $70\,°C$, $V_{DD} = 5\,V \pm 5\%$

Inputs are driven to 2.4 V for a logical "1" and to 0.4 V for a logical "0". Timing measurements are made at 2.0 V for a logical "1" and at 0.8 V for a logical "0".

The AC testing inpugt/output waveforms are shown below.

Input/Output Waveform for AC Tests

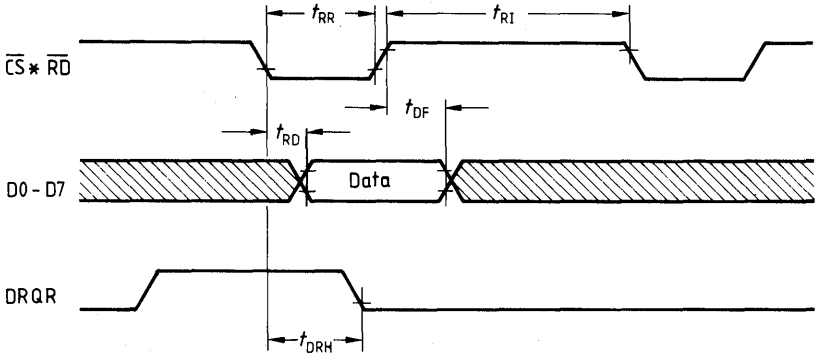




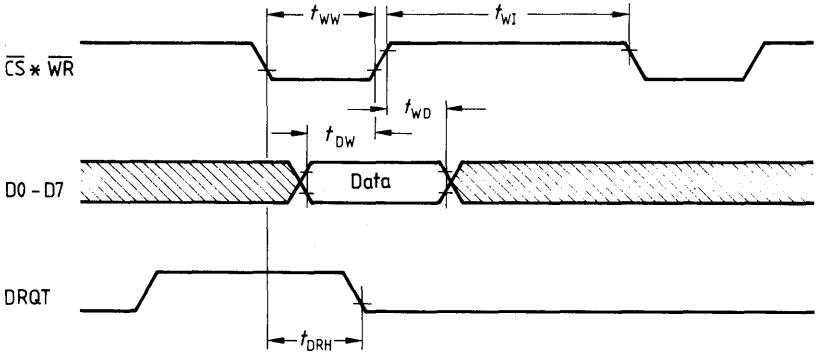
Microcontroller Interface Timing

Intel Bus Mode

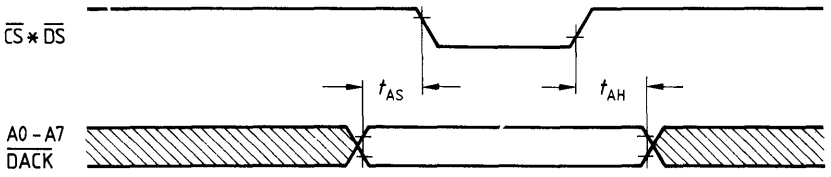
µP Read Cycle



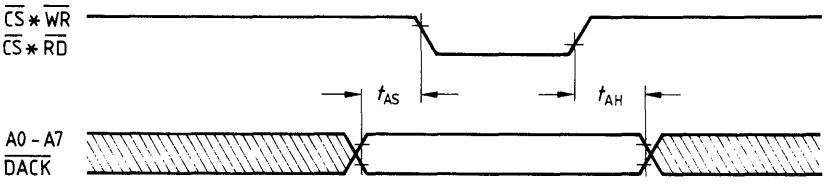
µP Write Cycle



Multiplexed Address Timing

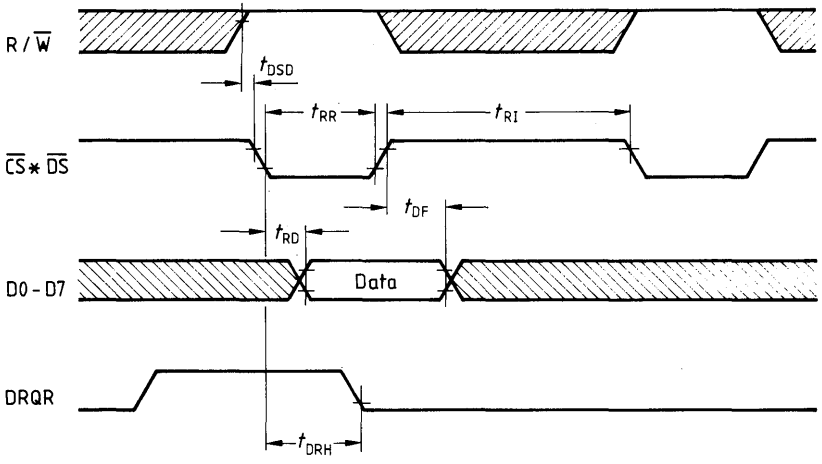


Address Timing

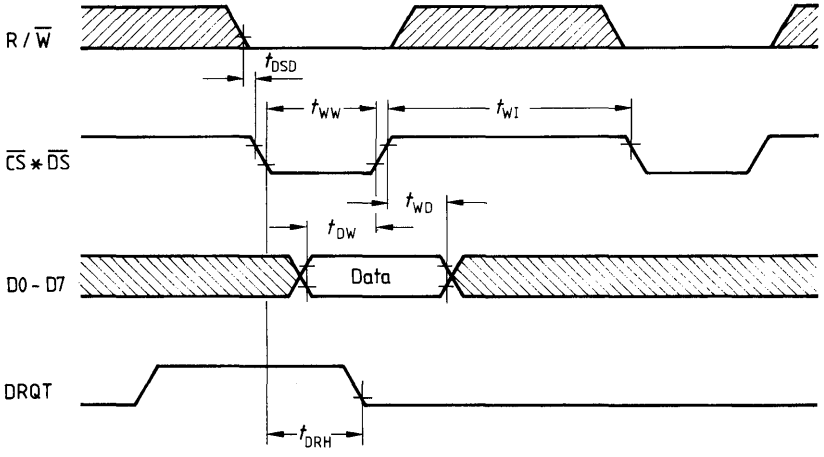


Motorola Bus Mode

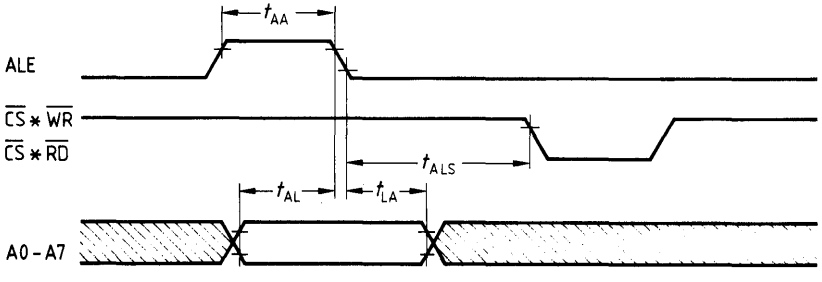
µP Read Cycle



µWrite Cycle



Address Timing

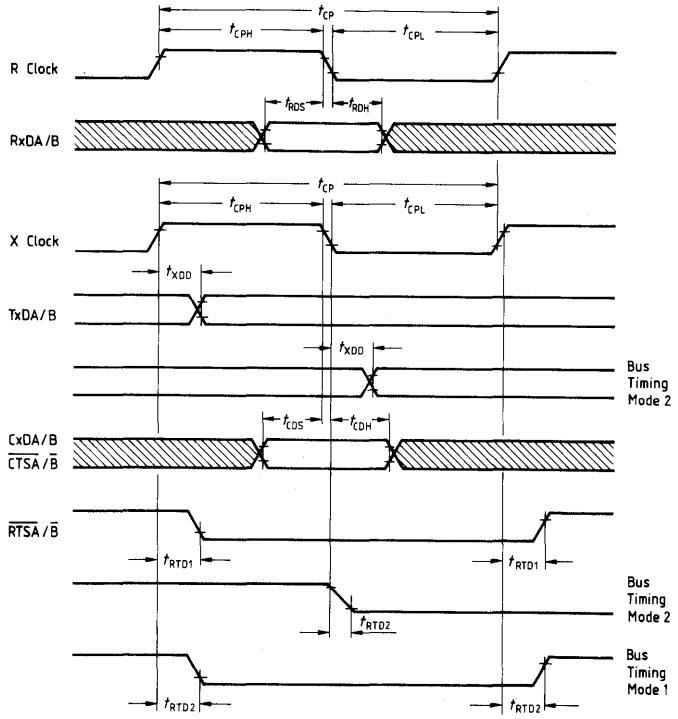


Interface Timing

Parameter	Symbol	Limit Values		Unit
		min.	max.	
ALE pulse width	t_{AA}	50		ns
Address setup time to ALE	t_{AL}	10		ns
Address hold time from ALE	t_{LA}	20		ns
Address latch setup time to $\overline{WR}$, $\overline{RD}$	t_{ALS}	0		ns
Address setup time to $\overline{WR}$, $\overline{RD}$	t_{AS}	10		ns
Address hold time from $\overline{WR}$, $\overline{RD}$	t_{AH}	20		ns
DMA request delay: SAB SAF	t_{DRH}		85 90	ns ns
$\overline{RD}$ pulse width	t_{RR}	120		ns
Data output delay from $\overline{RD}$	t_{RD}		120	ns
Data float delay from $\overline{RD}$	t_{DF}		25	ns
$\overline{RD}$ control interval	t_{RI}	60		ns
$\overline{WR}$ pulse width	t_{WW}	60		ns
Data setup time to $\overline{WR}+\overline{CS}$	t_{DW}	30		ns
Data hold time from $\overline{WR}+\overline{CS}$	t_{WD}	10		ns
$\overline{WR}$ control interval	t_{WI}	60		ns

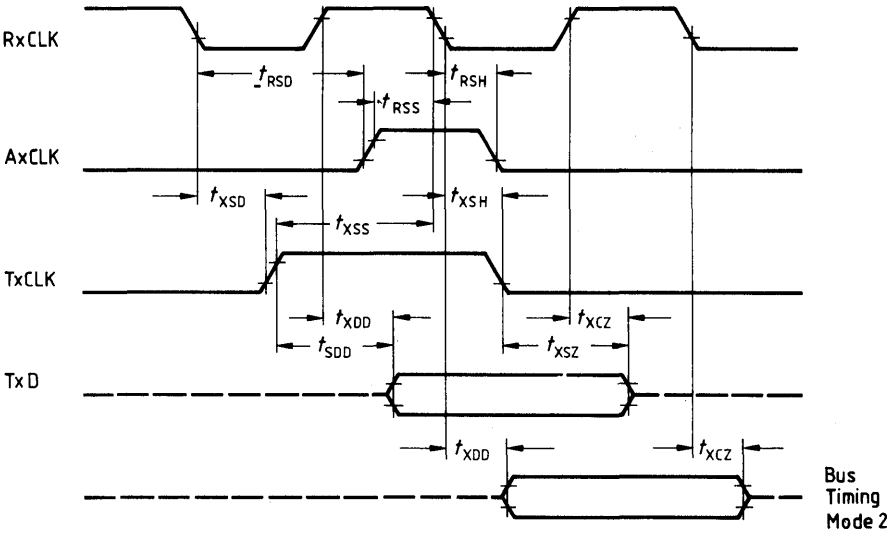
Serial Interface Timing

Clock Mode 1



Parameter	Symbol	Limit Values		Unit
		min.	max.	
Receive data setup	t_{RDS}	5		ns
Receive data hold	t_{RDH}	30		ns
Collision data setup	t_{CDS}	0		ns
Collision data hold	t_{CDH}	30		ns
Transmit data delay	t_{XDD}	20	70	ns
Request to send delay 1	t_{RTD1}	30	120	ns
Request to send delay 2	t_{RTD2}	20	85	ns
Clock period	t_{CP}	240		ns
Clock period Low	t_{CPL}	90		ns
Clock period High	t_{CPH}	90		ns

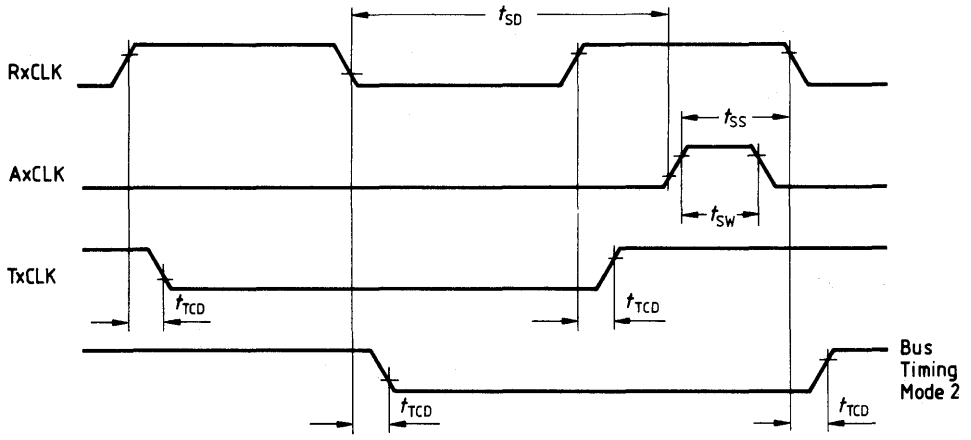
Strobe Timing



Parameter	Symbol	Limit Values		Unit
		min.	max.	
Receive strobe delay	t_{RSD}	30		ns
Receive strobe setup	t_{RSS}	60		ns
Receive strobe hold	t_{RSH}	30		ns
Transmit strobe delay	t_{XSD}	30		ns
Transmit strobe setup	t_{XSS}	60		ns
Transmit strobe hold	t_{XSH}	30		ns
Transmit data delay	t_{XDD}		70	ns
Strobe data delay	t_{SDD}		90	ns
High impedance from clock	t_{XCZ}		50	ns
High impedance from strobe	t_{XSZ}		50	ns

Clock Mode 5

Figure 17
Synchronization Timing



Parameter	Symbol	Limit Values		Unit
		min.	max.	
Sync pulse delay	t_{SD}	30		ns
Sync pulse setup	t_{SS}	30		ns
Sync pulse width	t_{SW}	40		ns
Time-slot control delay	t_{TCD}	20	75	ns

Clock Mode 2, 3, 6, 7

Internal Clocking

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Clock frequency Baudrate generator used	f_{CLK}		12.3	MHz
Clock frequency Baudrate generator not used	f_{CLK}		19.3	MHz

Reset Timing

RES Characteristics

Parameter	Symbol	Limit Values		Unit
		min.	max.	
RES high	t_{RWH}	1800		ns

Appendix A

Upgrades of HSCX Version A3

The HSCX Version A3 is fully upward compatible to Version A2. The differences with respect to HSCX Technical Manual Rev. 2.89 are shown in **table 3**.

Table 3
Differences HSCX A2 – HSCX A3

Differences	Ver. A2	Ver. A3	Data Book Chapter
TRI, TWI value	70 ns	60 ns	Microcontroller Interface Timing
IOL value, pin TxD	2 mA	6 mA	Characteristics
VSTR value	02_H	04_H	VSTR, Register Definition

The following additional are implemented in HSCX A3

- Transmission of back to back frames
  Two or more frames may be transmitted continuously without interframe time fill
- TxD, RxD flip
  In clock modes 0, 1, 4 and 5 pins RxD and Tx may be flipped
- Status Register
  In auto mode, STAR: bit 0 indicates the 'Waiting for Acknowledgement' status

SIEMENS

Integrated Data Protocol Controller (IDPC) SAB 79C401

ADVANCE INFORMATION

General Description

The SAB 79C401 Integrated Data Protocol Controller (IDPC) provides many of the essential building blocks for construction of a variety of communications systems. When combined with ROM, RAM, a microprocessor, and the appropriate physical layer transceiver, a complete ISDN, X.25, SNA, or similar system can be constructed.

The IDPC contains hardware and software support features for use in a single-processor environment (such as a terminal adaptor to an ISDN network) or a multi-processor application (such as a communication interface for a PC or integrated voice/data work station application). For multi-processor applications, the IDPC controls access to an external "shared" RAM which serves as a data buffer and communications area ("mailbox" concept). The IDPC arbitrates simultaneous requests for RAM access and supports an inter-processor interrupt scheme.

Functionally, the IDPC consists of four sections: Data Link Controller (DLC), Universal Synchronous/Asynchronous Receiver/Transmitter (USART), Dual-Port Memory Controller (DPMC), and Microprocessor Interface (MPI).

Data Link Controller (DLC)

The DLC is a high-speed, bit-oriented protocol processor that supports either multiplexed or non-multiplexed data transfer rates up to 2.048 Mbit/s.

The DLC provides full-duplex (simultaneous transmit and receive) data transfer between the chip's serial bus port and internal parallel bus. Through the use of a 32-byte receive FIFO, 16-byte transmit FIFO, and two external DMA channels, the DLC provides efficient movement of data to and from external memory and the serial bus port (network interface).

The DLC supports data transfers via DMA, interrupts, or polled I/O. The use of the FIFO buffers minimize interrupt latency and frequency of interrupts.

Universal Synchronous/Asynchronous Receiver/Transmitter (USART)

The IDPC contains a built-in USART for exchanging data between terminals and the ISDN network in applications where there is no host processor. The USART provides a superset of 8250 UART features and supports both synchronous and asynchronous serial communications. The USART is capable of full-duplex operation at speeds up to 56 bit/s using an internal programmable baud rate generator (or optional external clock sources).

The USART supports the following functions

- Program-selectable synchronous/asynchronous modes
- Software reset
- Line break recognition and generation
- Special character recognition
- Selectable stop bits (1-, 1.5-, or 2-stop bits)
- Full modem control handshake lines (RTS, CTS, DSR, and DTR)
- "Local Loopback" and "Stick Parity" test features

Dual-Port Memory Controller (DPMC)

The DPMC provides RAM access control and an inter-processor interrupt mechanism that permits two processors to share common RAM memory without the expense of dual-port RAM. These features are used in developing network interface applications for PCs and Integrated Voice/Data Workstations (IVDWs).

Microprocessor Interface (MPI)

The MPI consists of an 8-bit non-multiplexed data bus that allows the IDPC to function with a 12.5-MHz 80188 processor (or other similar microprocessor) with zero wait states.

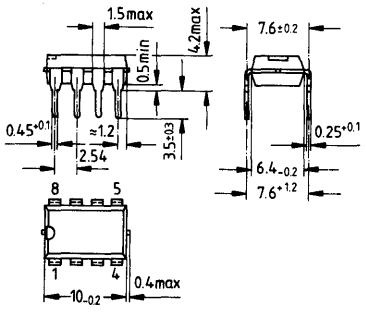
Features

- **Data Link Controller**
  - Full featured bit-oriented communication controller supporting HDLC, SDLC, LAPB, LAPD, and DMI
  - Data transfer rate: 2.048 Mbit/s
  - 32-byte receive FIFO and 16-byte transmit FIFO with programmable thresholds and DMA handshakes
  - Multiple (four plus broadcast) address recognition modes
  - Multiplexed serial interface with up to thirty-one 8-bit channels or non-multiplexed serial interface
  - Local and remote loopback modes
  - Transparent mode
  - 56 kbit/s mode
- **USART**
  - Superset of Industry-Standard 8250 UART features
  - 4-byte transmit/receive FIFOs
  - Special character recognition (up to 128 programmable)
  - Synchronous mode provides a transparent serial data path
  - Local loopback mode
- **Dual-Port Memory Controller**
  - Memory bus arbitrator provides dual-port access to standard low-cost static RAM
  - Programmable inter-processor interrupts support RAM-based inter-processor mailboxed
- **Microprocessor Interface**
  - 8-bit non-multiplexed data bus
  - Operates with 12.5-MHz 80188 processor with zero wait states
- **General Features**
  - Compatible with PSB 79C30 DSC
  - CMOS technology, single +5-V supply
  - Power-down mode
  - 68-pin PL-CC

Package Outlines

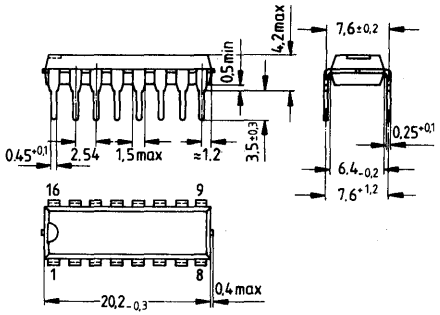
Package Outlines

Plastic Dual-in-Line Package, P-DIP-8
20 A 8 DIN 41870 T9



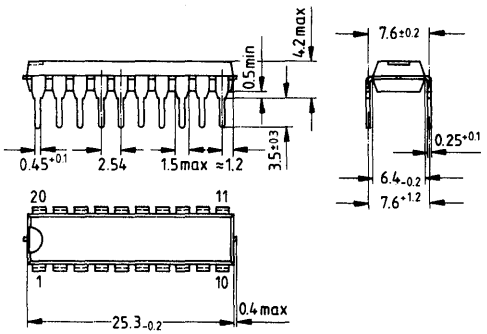
Approx. weight 0.7 g

Plastic Dual-in-Line Package, P-DIP-16
20 A 16 DIN 41870 T9



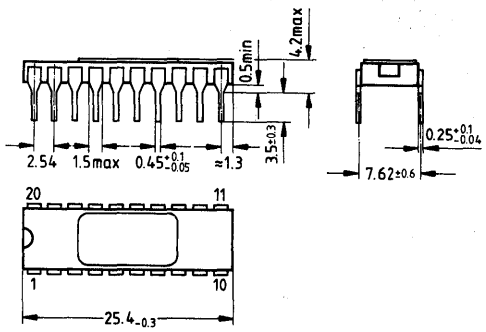
Approx. weight 1.2 g

Plastic Dual-in-Line package, P-DIP-20
20 A 20 DIN 41870 T9



Approx. weight 1.5 g

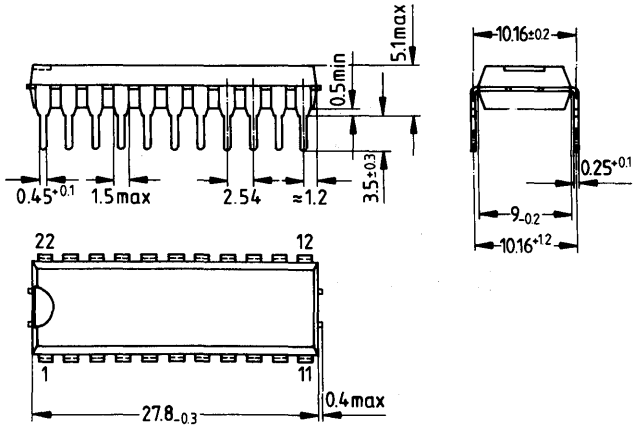
Ceramic Dual-in-Line package, C-DIP-20
20 A 20 DIN 41870 T9



Apprix. weight 1.7 g

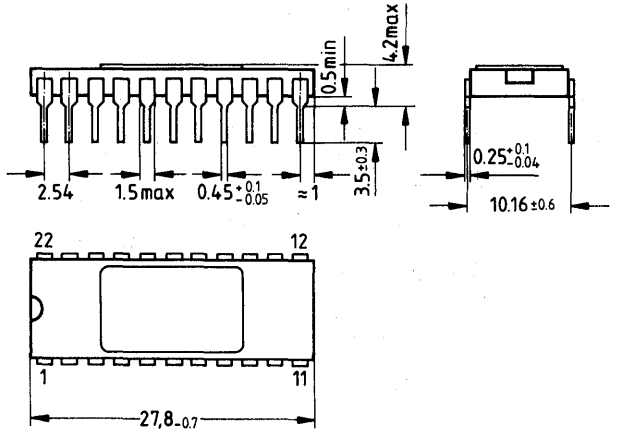
Dimensions in mm

Plastic Dual-in-Line Package, P-DIP-22
20 D 22 DIN 41870 T11



Approx. weight 2.1 g

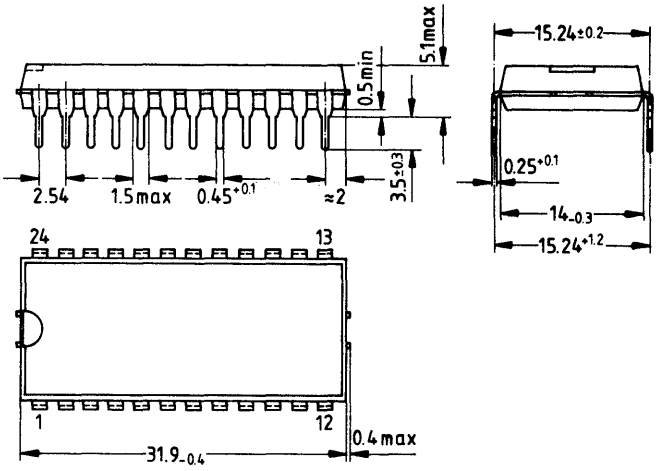
Ceramic Dual-in-Line Package, C-DIP-22
20 D 22 DIN 41870 T11



Approx. weight 2.5 g

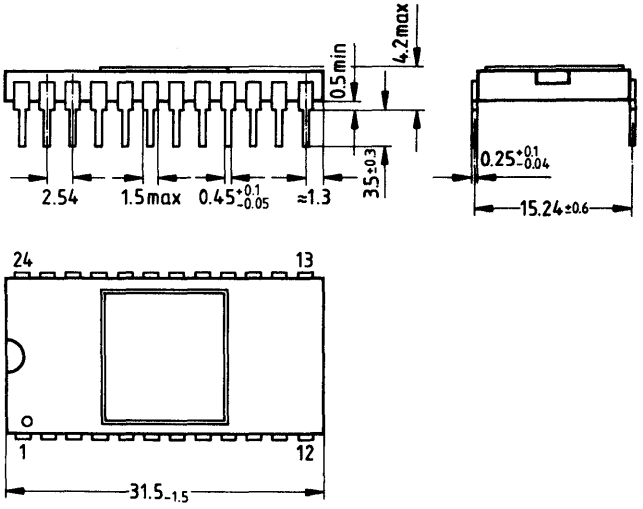
Dimensions in mm

Plastic Dual-in-Line Package, P-DIP-24
20 B 24 DIN 41870 T10



Approx. weight 2.5 g

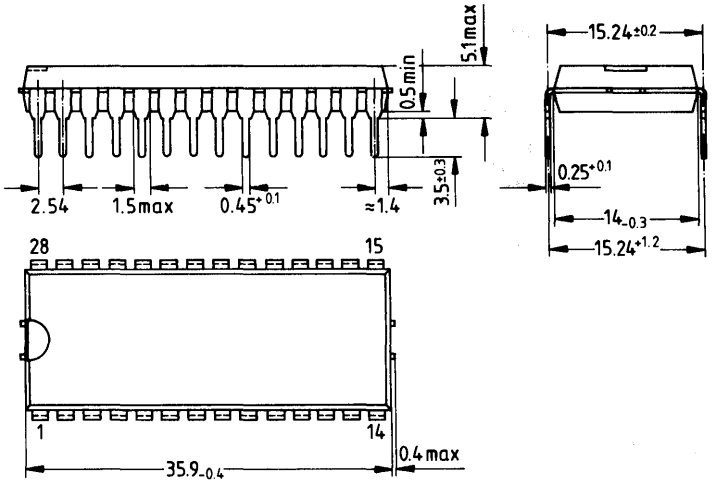
Ceramic Dual-in-Line Package, C-DIP-24
20 B 24 DIN 41870 T10



Approx. weight 3 g

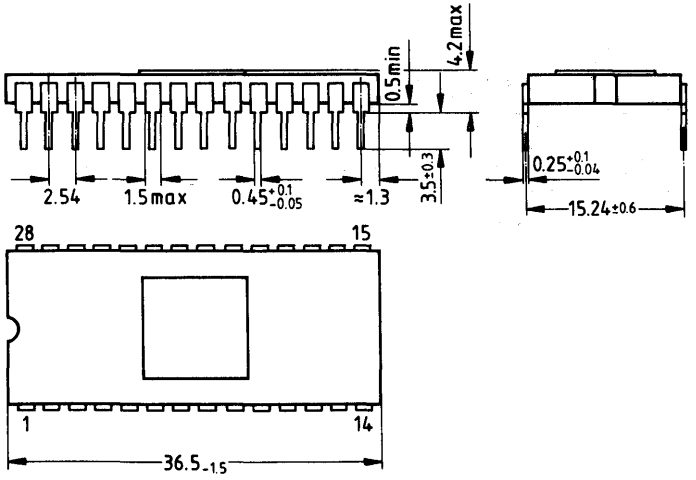
Dimensions in mm

Plastic Dual-in-Line Package, P-DIP-28
20 B 28 DIN 41870 T10



Approx. weight 3 g

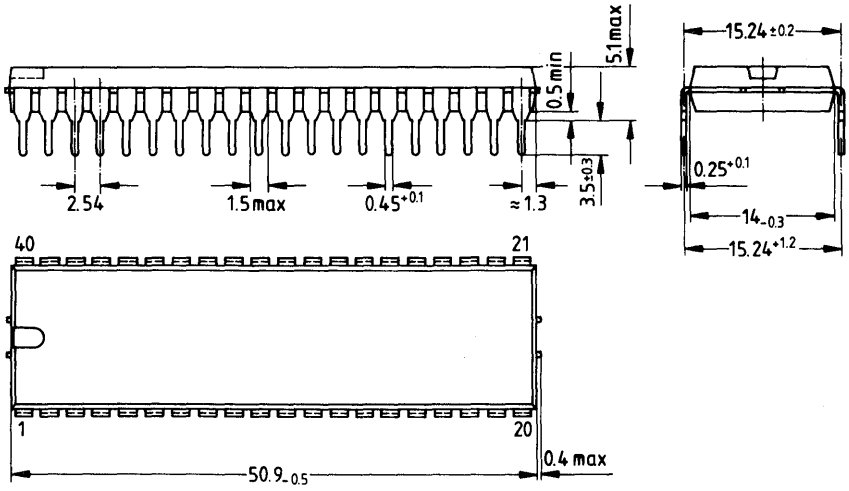
Ceramic Dual-in-Line Package, C-DIP-28
20 B 28 DIN 41870 T10



Approx. weight 3.5 g

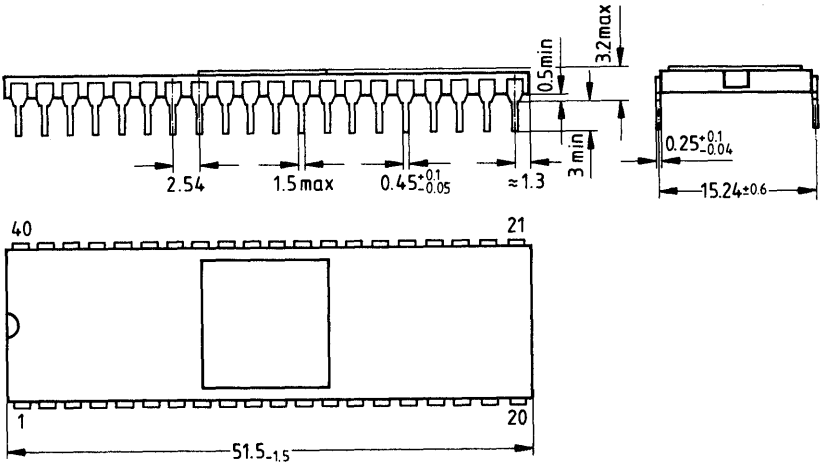
Dimensions in mm

Plastic Dual-in-Line Package, P-DIP-40
20 B 40 DIN 41870 T10



Approx. weight 5.9 g

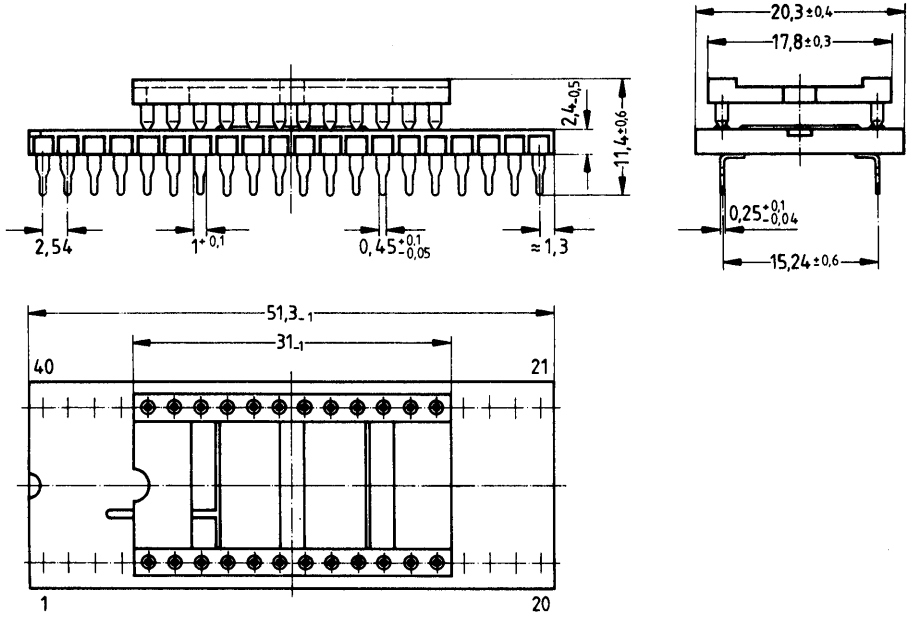
Ceramic Dual-in-Line Package, C-DIP-40
20 B 40 DIN 41870 T10



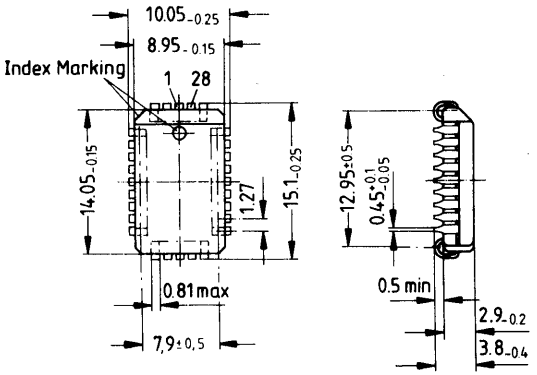
Approx. weight 6.8 g

Dimensions in mm

Piggyback



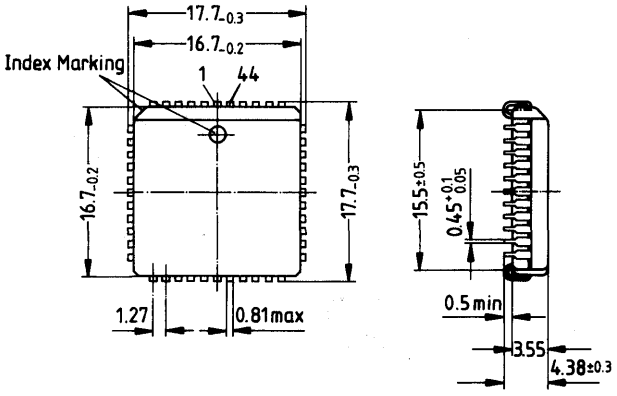
Plastic-Leaded Chip Carrier, PL-CC-28-R (SMD)



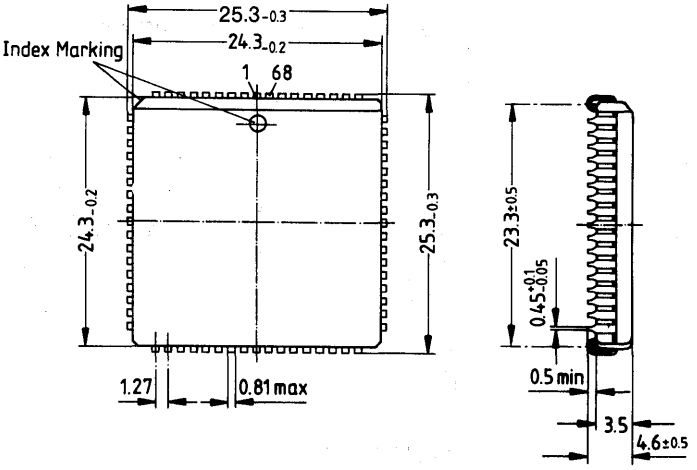
Dimensions in mm

SMD = Surface Mounted Device

Plastic-Leaded Chip Carrier, PL-CC-44 (SMD)

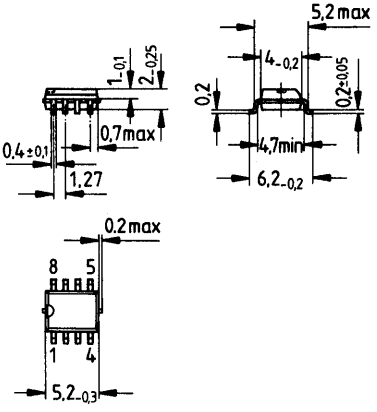


Plastic-Leaded Chip Carrier, PL-CC-68 (SMD)

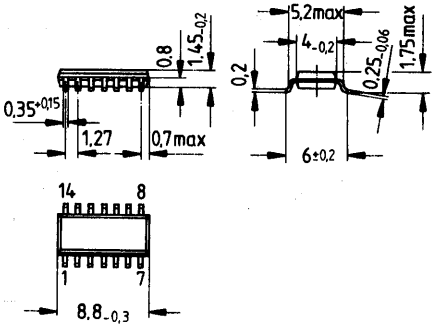


Dimensions in mm

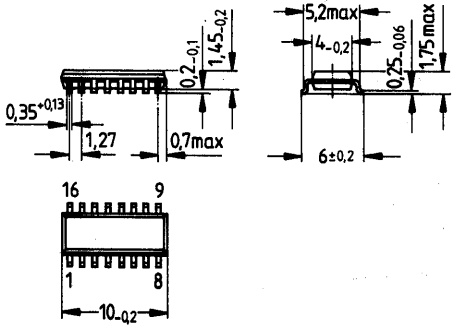
Miniature Plastic Dual-in-Line Package, P-MIP-8-G (SMD)
(Small Outlines)
(similar to P-DSO-8)
24 A 8 DIN 41870 T16



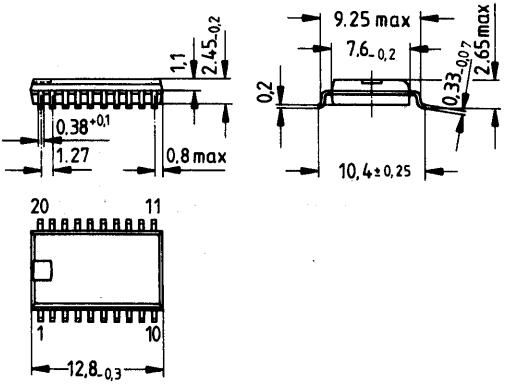
Miniature Plastic Dual-in-Line Package, P-DSO-14 (SMD)
(Small Outlines)
24 A 14 DIN 41870 T16



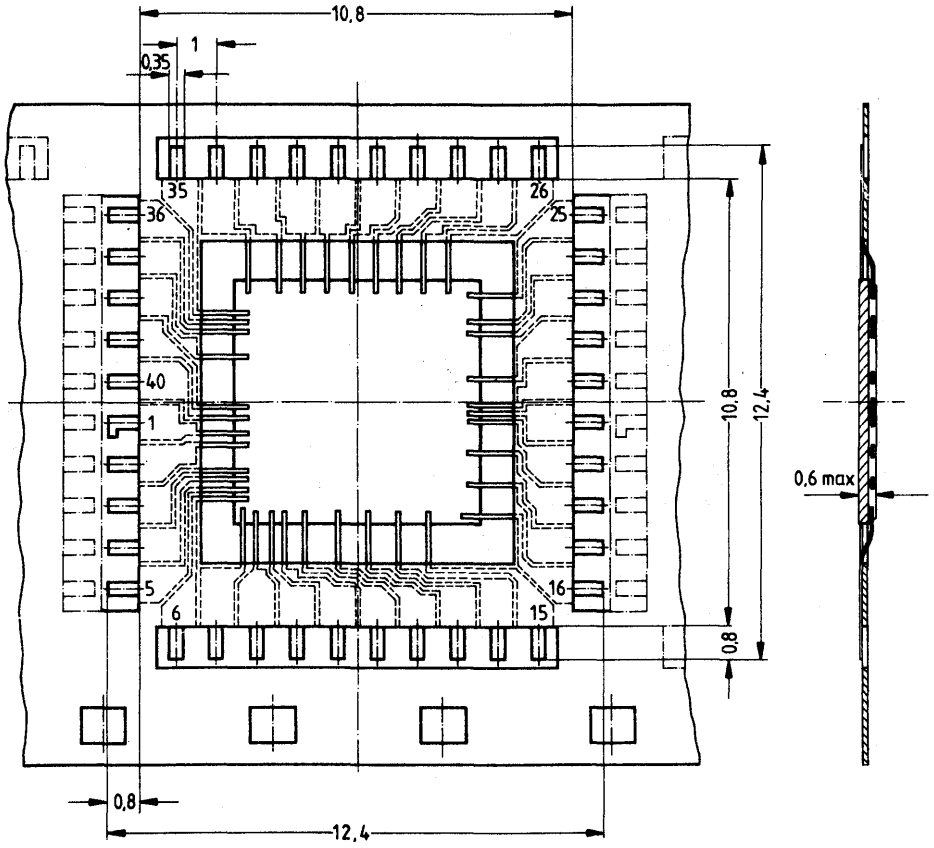
Miniature Plastic Dual-in-Line Package, P-DSO-16 (SMD)
(Small Outlines)
24 A 16 DIN 41870 T16



Miniature Plastic Dual-in-Line Package, P-DSO-20 (SMD)
(Small Outlines)
24 B 20 DIN 41870 T17

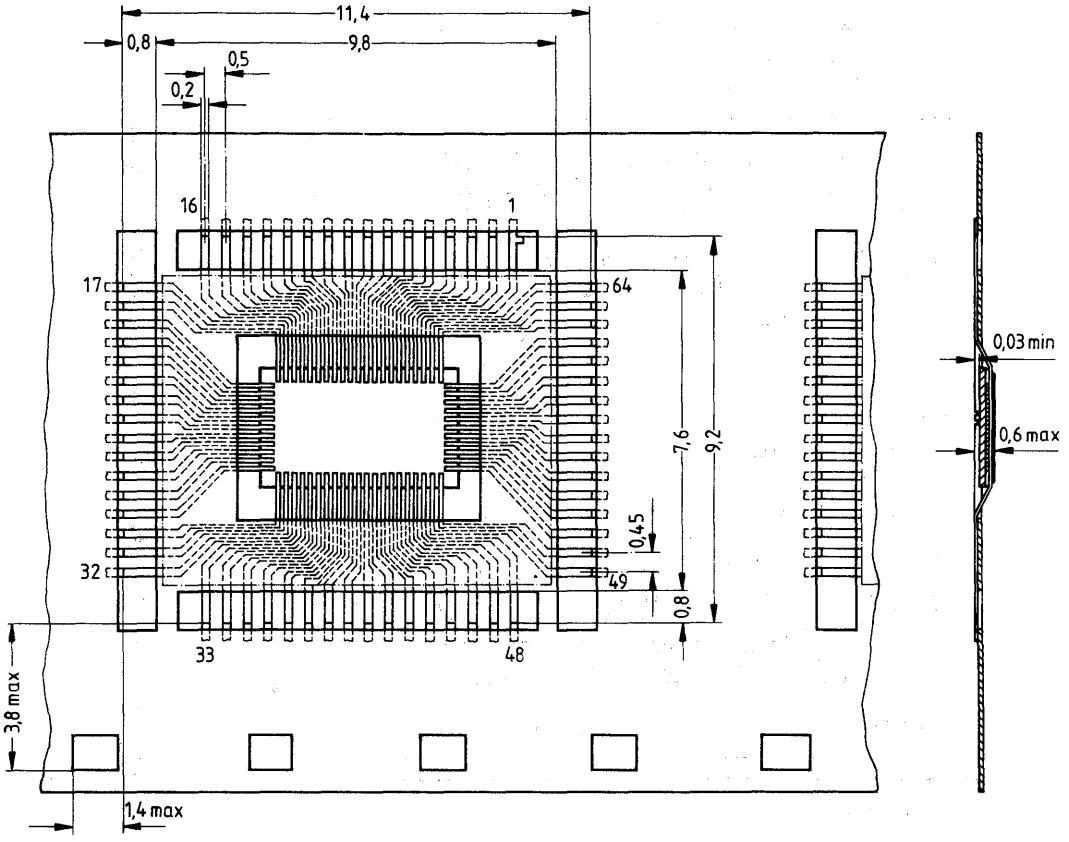


MIKROPACK (SMD)
16 mm, 40 pins



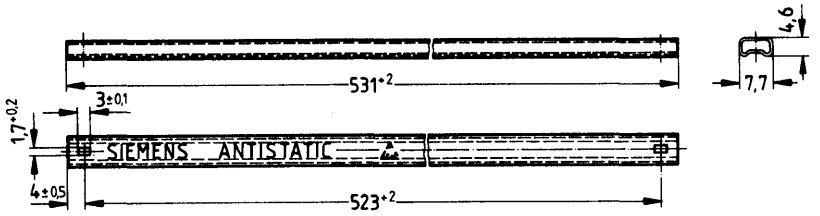
Dimensions in mm

MIKROPACK (SMD)
16 mm, 64 pins

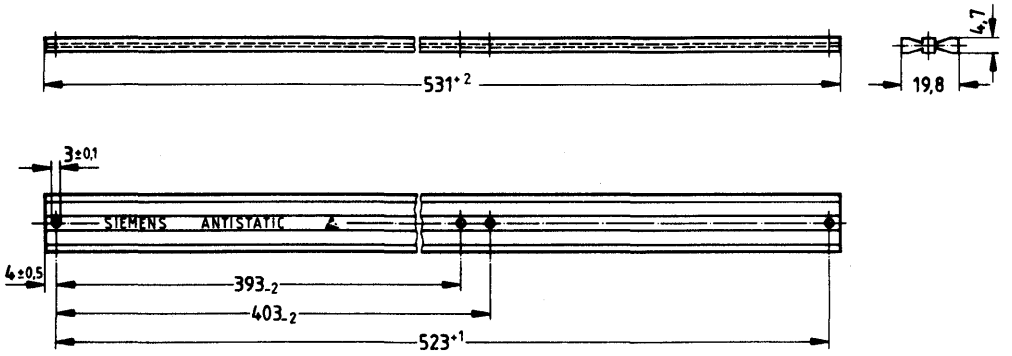


Dimensions in mm

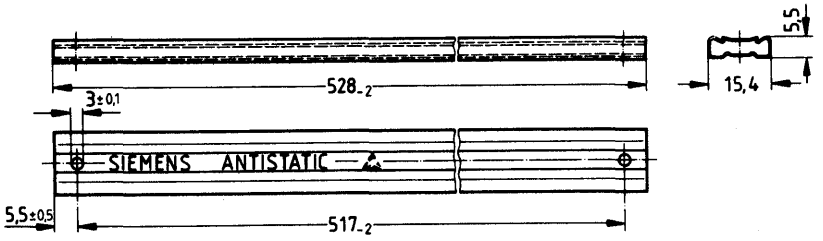
Packages: P-DSO-6; 8; 14; P-MIP-6-G; 8-G



Packages: P-MIP-6; 8



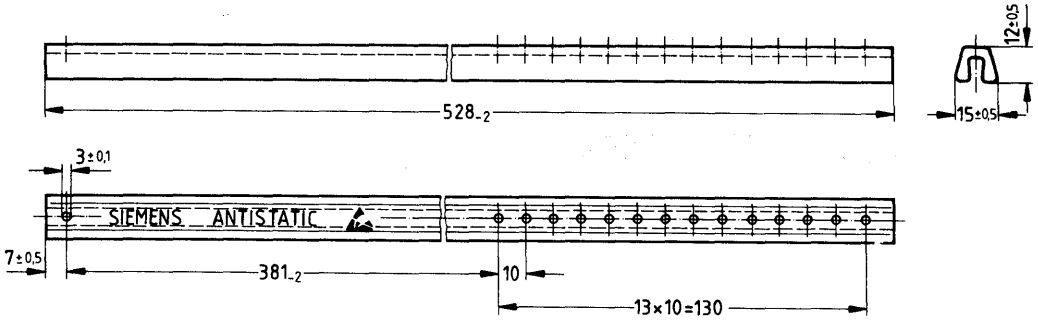
Packages: P-DSO-20



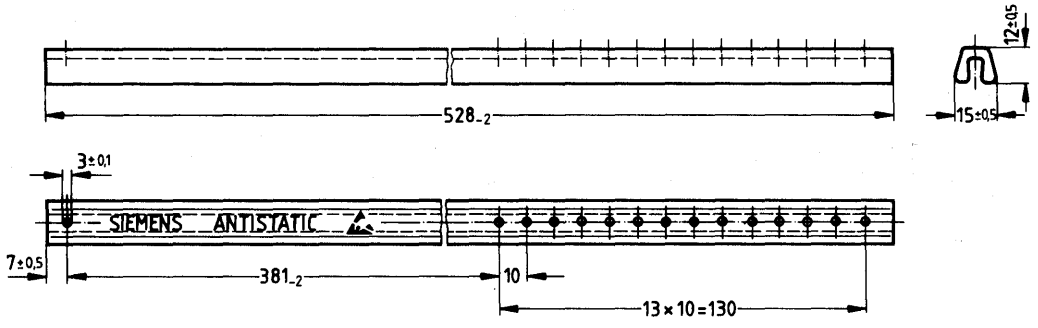
Dimensions in mm

Packaging Rails

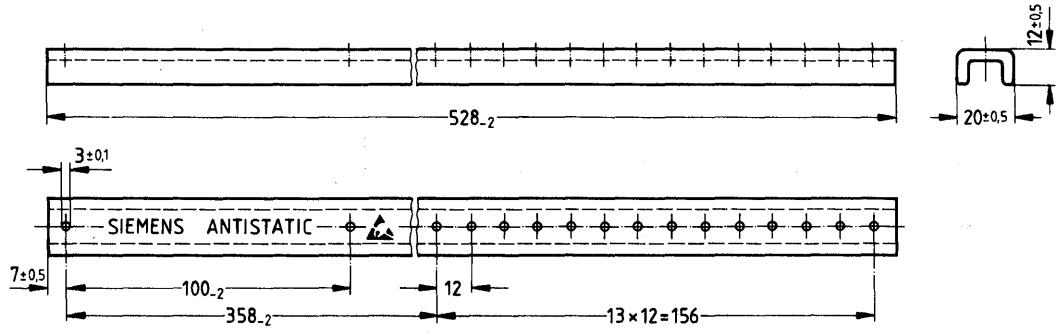
Packages: P-DIP-4; 6; 8; 14; 16; 18; 20



Packages: C-DIP-14; 16; 18; 20



Packages: C-DIP-24; 28; 40; 48



Dimensions in mm

Packaging Rails

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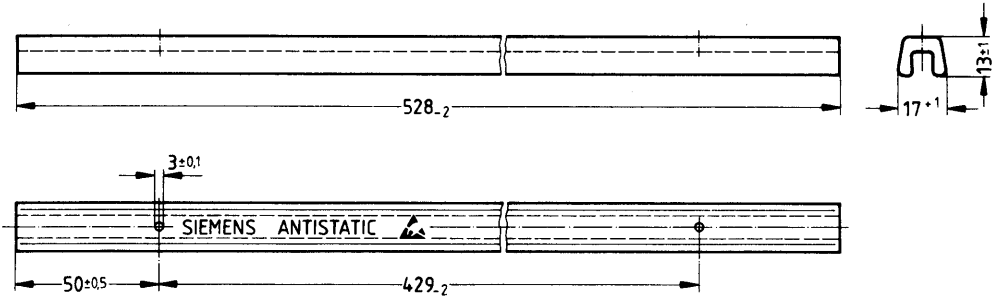

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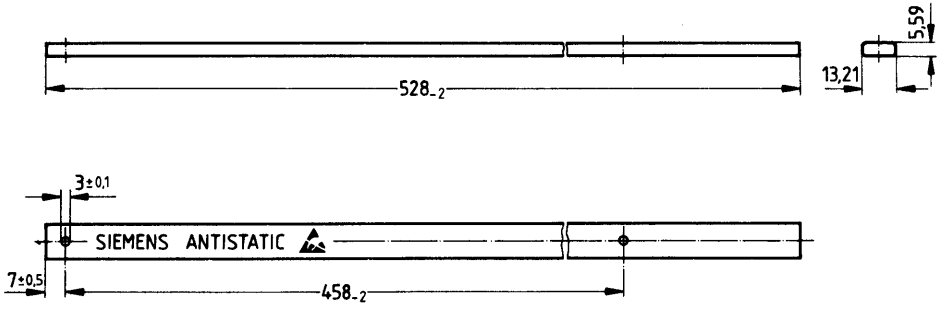

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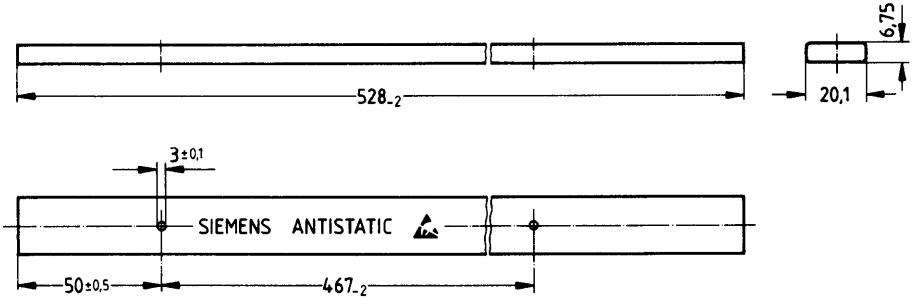
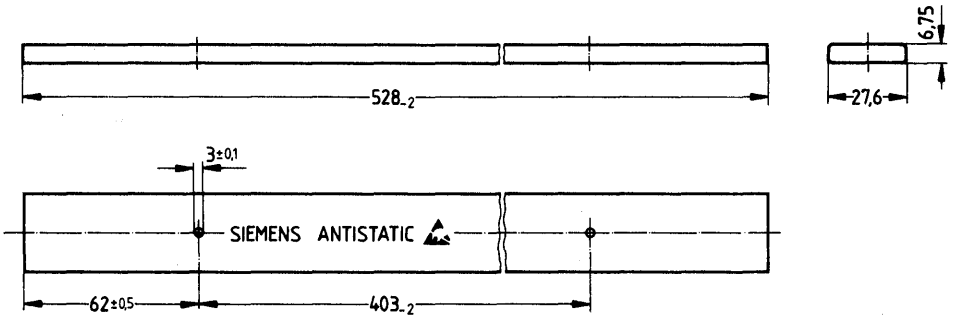


Dimensions in mm

Packages: PL-CC-68



Dimensions in mm

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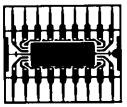

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