INTEGRATED CIRCUITS

DATA HANDBOOK

ABT
Advanced BiCMOS
Interface Logic

Signetics

Philips Components

PHILIPS

Advanced BiCMOS Interface Logic

Signetics

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Preface

ABT Products

Philips Components–Signetics would like to thank you for your interest in our products.

This handbook contains information and specifications on our Advanced BiCMOS interface components.

We have selected a group of bus interface parts ideally suited to take advantage of our new QUBiC BiCMOS process. QUBiC is not a compromise of two processes, rather a truly integrated combination of our fastest Bipolar modules and an exciting new sub-micron CMOS. QUBiC allows us to offer the fastest bus interface products available. This high performance, speed and high output drive, is enhanced with low, low CMOS power dissipation and excellent noise immunity.

Product Status

ABT Products

DEFINITIONS		
Data Sheet Identification	**Product Status**	**Definition**
Objective Specification	Formative or In Design	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	Preproduction Product	This data sheet contains preliminary data and supplementary data will be published at a later date. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	Full Production	This data sheet contains Final Specifications. Signetics reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

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Alphanumeric Index

74ABTXXX FAMILY

† For more information on this device, please contact the factory.

Functional Index

74ABTXXX FAMILY

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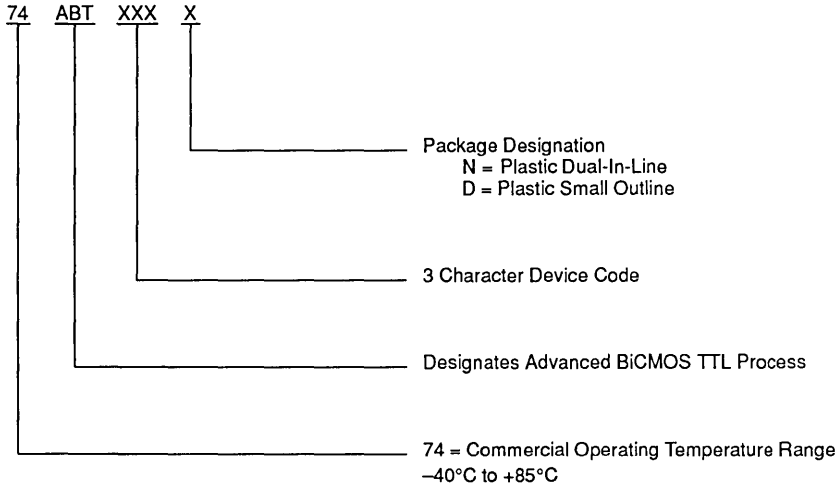
Ordering Information

ABT Products



TEMPERATURE RANGE	DEVICE NUMBER	PACKAGE STYLE
T_{amb} = –40°C to +85°C	74ABTXXX	D = Plastic Small Outline N = Plastic Dual-In-Line

Section 1
Introduction

ABT Products

INTRODUCTION

A true BiCMOS process, such as QUBiC, gives and integrated circuit designer a great deal of freedom in approaching the optimum requirement goals of the system designer. The input and output structures can be designed in such a way that they are optimum from a system standpoint. Noise characteristics such as ground bounce and EMI can be minimized without performance degradation. Speed can be maximized towards that of the fastest bipolar devices and power dissipation can be greatly reduced below even pure CMOS approaches.

QUBiC PROCESS

The QUBiC BiCMOS process from Philips Components–Signetics is truly a major achievement in semiconductor process technology. With equal emphasis on optimization of the CMOS as well as the bipolar devices, the process offers 13 GHz bipolar NPN devices, one micron NMOS devices, and one micron PMOS devices, altogether with three layers of Al/Cu interconnect. The devices are completely free of latch-up, have high ESD protection, show no electromigration, and due to low bipolar reverse leakage currents and lightly doped CMOS drains, show extremely long reliability lifetimes. From an electrical performance standpoint the results of this process are clear.

AC CHARACTERISTICS

Speed is almost always the first characteristic considered when choosing an integrated circuit. With bus frequencies constantly on the rise and the demand for greater data transfer rates continuously increasing, bus interface devices have become especially sensitive to speed. Figure 1 clearly shows the advantage of Philips Components–Signetics ABT Advanced BiCMOS interface devices.

Supply voltage and temperature stability is also an important feature of a product. Figure 1 shows the propagation delay versus change in the supply voltage and change in temperature. The temperature stability of ABT devices is again a by-product of the process technology. A bipolar transistor generally becomes stronger with increases in temperature and a CMOS transistor slows down with an increase in temperature. The effective addition of these two phenomena create the desirable feature shown in the figure. The flat slope of these curves essentially removes the variables of power supply and temperature from a designer's list of considerations. It also ensures that the device will be more resistant to unexpected system deviations from supply and temperature norms.

INPUT CHARACTERISTICS

The ABT Advanced BiCMOS interface devices have TTL input electrical levels, guaranteed switching between 0.8V and 2.0V (typically 1.6V) in order to be driven by TTL or CMOS level buses. They have the desired CMOS characteristic of very low input current loading and input capacitance in the 3 - 4 pF range. This feature ensures that the devices lightly load the buses they are interfacing to, allowing the devices to be driven from lower output current devices on a local bus, thus allowing higher system integration.

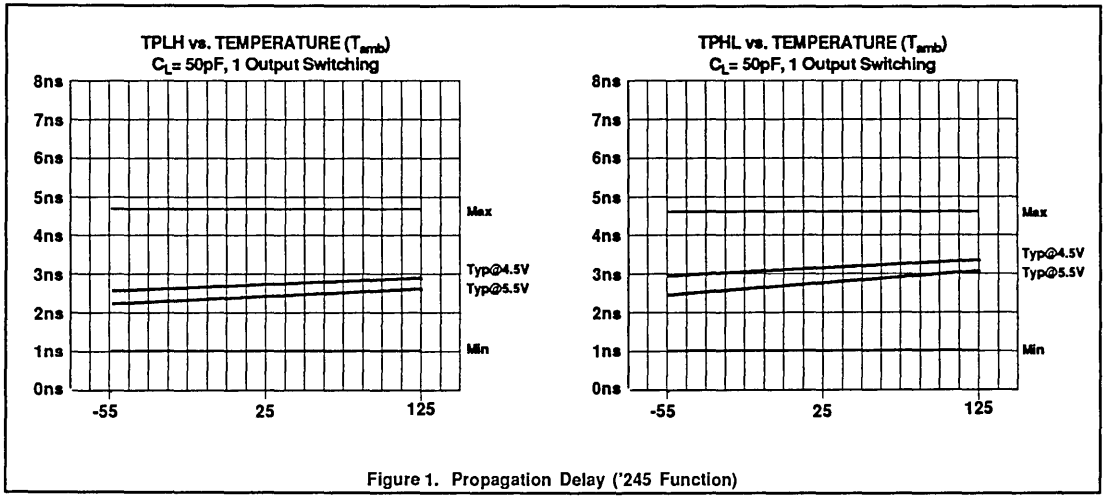


Figure 1. Propagation Delay ('245 Function)

Introduction

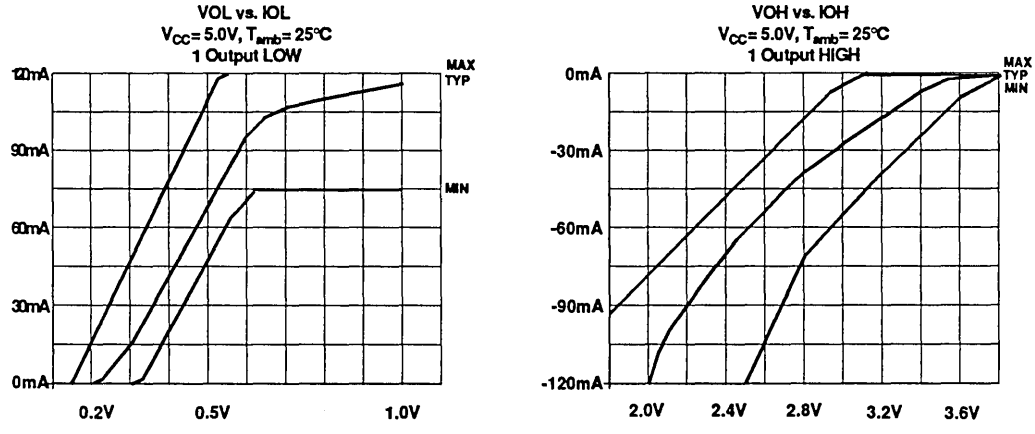


Figure 2. V_{OL} versus I_{OL} and V_{OH} versus I_{OH} (74ABT245)

OUTPUT CHARACTERISTICS

The BiCMOS interface devices have TTL output electrical levels, guaranteeing a V_{OL} of 0.55V (typically 0.4V) while sinking 64mA and guaranteeing a V_{OH} level of 2.0V (typically 3.1V) while sourcing 32mA. Unlike a pure bipolar output structure, these outputs will effectively "turn-off" when the output is in the high state or the disabled state and will no contribute to I_{CC}. **This causes I_{CCH} and I_{CCZ} values to be essentially zero.** When the output is in the low state, the device will show some I_{CCL} but this value is less than most equivalent bipolar devices by a factor of three to four.

In order to effectively drive heavily loaded local bus applications or almost all backplane or system bus applications, high output current drivers are required. The Philips Components–Signetics ABT devices provide as standard 64mA I_{OL}, enough current for nearly all bus driving applications. Figure 2 shows the output current versus voltage characteristic for an ABT output structure. This clearly shows the ability of the output to source and sink large amounts of current to and from the bus to which it is interfaced.

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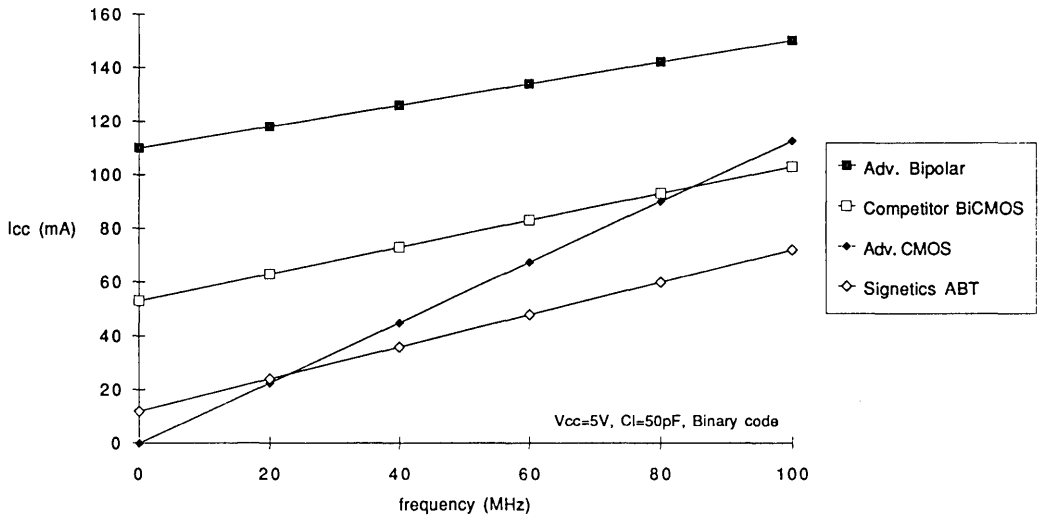

Figure 3. Current Consumption vs. Frequency ('245 Function)

POWER DISSIPATION

Device power dissipation is of greater concern now than is was only a few years ago. The largest influence on this trend is almost certainly the move towards smaller, more compact systems and their related reliability concerns. Along with this, the increased popularity of surface mount devices has driven heat dissipation specifications towards zero. No longer can ten interface devices sitting disabled on a bus be allowed to dissipated five watts of power. The ABT Advanced BiCMOS interface devices from Philips Components–Signetics will be guaranteed to dissipate typically zero power (microwatts) when disabled or in the high state.

It is certainly true that static power dissipation is not the entire story. The device, after all, will be in a critical path and will, therefore, be under some pressure from the devices to which they are interfaced to operate. Figure 3 illustrates the relative current consumption of a popular octal device when the devices is under operation. Each output is loaded with a 50pF load and counts through a binary code from 00000000 to 11111111 at the given frequency.

It is common knowledge that pure CMOS devices perform rather poorly with respect to power dissipation at very high frequencies. It can also be noted, however, that pure bipolar devices also show a positive, non-zero slope of I_{CC} versus frequency. It can be seen in the figure that the ABT BiCMOS parts will consume roughly the same amount of **delta** current versus **delta** frequency (slope) as bipolar/other BiCMOS, but its overall magnitude is approximately 100 mA less than a pure bipolar approach over the entire frequency range and 40 mA less than a competing BiCMOS approach.

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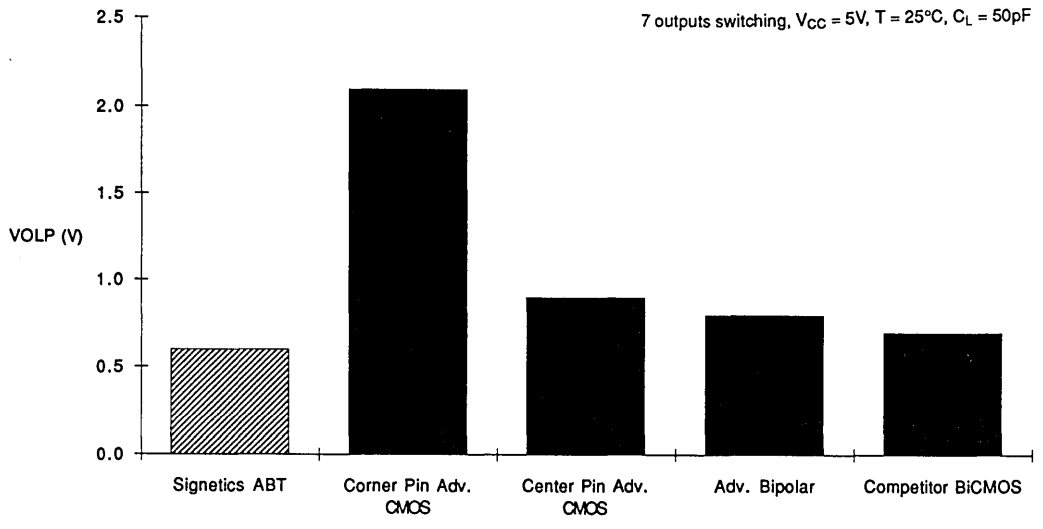

Figure 4. Ground Bounce Voltage ('245 Function)

NOISE

Ground and V_{CC} noise generated by an integrated circuit has been greatly recognized as an undesirable feature that needs to be addressed by the IC manufacturer and not by the system designer alone. Supply noise causes numerous problems ranging from propagation delay degradation to logic errors to EMI/FCC failures. Considerable attention has been focused on noise and its related issues and Figure 4 shows a comparison of various devices available and their equivalent ground bounce voltage (V_{OLP}). Philips Components–Signetics ABTXXX devices have been responsibly designed to exhibit less than 800mV of ground noise which can be observed in Figure 4.

CONCLUSION

Philips Components–Signetics Advanced BiCMOS interface logic begins a new chapter in interface logic performance. Using a new revolutionary integrated bipolar and CMOS process, the devices allow for faster, high drive applications while lowering power dissipation to previously unreachable levels. High speed and high drive were not acquired at the cost of high power dissipation, increased bus loading, or increased noise. Together with support from the widest range international supplier of logic devices in the world, Philips Components–Signetics ABTXXX Advanced BiCMOS interface logic devices have become the high performance interface logic of choice.

Section 2
Quality and Reliability

ABT Products

AMIC PHILIPS COMPONENTS–SIGNETICS ASSURANCE PROGRAM

PHILIPS COMPONENTS–SIGNETICS QUALITY PROGRAM

In 1979, Philips Components–Signetics recognized that quality was becoming a major competitive issue, not only in the semiconductor business but also in other industries. Increases in the volume of products imported from the Far East (steel, automobiles, and consumer products) sent strong signals that new competitive forces were at work.

Philips Components–Signetics quickly began to investigate a variety of quality programs. The company realized that quality improvement would require a contribution from all employees. Management commitment and participation, however, was recognized as the primary prerequisite for this program to work successfully. Resources required for the resolution of defects under management control.

In 1980, Philips Components–Signetics developed a program which focused on quality management. Rearranging previous quality control philosophies, Philips Components–Signetics developed a decentralized, distributed quality organization and simultaneously installed a quality improvement process based on the 14–Step improvement program advocated by Phil Crosby. The process was formally begun company–wide in 1981. Since then substantial progress has been made in every aspect of Philips Components–Signetics' operations. From incoming raw material conformance to improvements in clerical errors — every department and individual is involved and striving for Zero Defects. Zero Accept sampling plans and Zero Defects warranties are evidence of Philips Components–Signetics' ongoing commitment and progress in quality.

Today, Philips Components–Signetics' quality improvement process has had a far–reaching impact on all aspects of our business. Philips Components–Signetics provided its customers with products of refined electrical and mechanical quality. And through continual use and modification of the Crosby program, Philips Components–Signetics is providing itself with well–defined method of managing ongoing improvement efforts.

PHILIPS COMPONENTS–SIGNETICS' ZERO DEFECTS WARRANTY

In recent years, American industry has demanded increased product quality of its IC suppliers in order to meet growing international competitive pressure. As a result of this quality focus, it is becoming clear that what once thought to be unattainable— Zero Defects— is, in fact achievable.

Philips Components–Signetics offers a Zero Defects Warranty which states that it will take back an entire lot if a single defective part is found. This precedent setting warranty has effectively ended the IC industry's " war of the AQLs" (Acceptable Quality Levels). The ongoing efforts of IC suppliers to reduce PPM (Parts Per Million) defect levels is now a competitive customer service measure. This intense commitment to quality provides an advantage to today's electronics OEM. That advantage can be summed up in four words: ***Reduced Cost of Ownership.***

As IC customers look beyond purchase price to the total cost of doing business with a vendor, it is apparent that a quality–conscious supplier like Philips Components–Signetics, represents a viable cost reduction resource. Consistent high–quality circuits reduce requirements for expensive test equipment and personnel, and allow for smaller inventories, less rework, and fewer field failures.

PHILIPS COMPONENTS–SIGNETICS' STATISTICAL PROCESS CONTROL (SPC)

Although application of statistics in our process development and manufacturing activities goes back to the early 1970's, the corporate–wide emphasis on Statistical Process Control (SPC) did not come until mid–1984.

A natural evolution of our quality process made introduction of SPC and other related programs an inevitable event. SPC was, therefore, introduced under the quality umbrella.

The objective of the SPC programs to introduce a systematic and scientific approach to business and manufacturing activities. This approach utilizes sound statistical theory. Managers are expected to be able to turn data into information, and make decisions solely on data (not perception).

The most critical and challenging aspect of implementing SPC is establishment of a discipline within the operating areas so that decision making is fundamentally based on verifiable data, and actions are documented. The other is realization of the fact that statistical tools merely point out the problems and are not solutions by themselves. The burden of action on the process is still on the implementers' shoulders. In order to implement SPC effectively, three steps are continually followed:

Documenting and understanding the process, using process flow charts and component diagrams.

Establishing data collection systems, and using SPC tools to identify process problems and opportunities for improvement.

Acting on the process, and establishing guidelines to monitor and maintain process control.

Repeating steps 1–3 again.

These fundamentals are the basis of establishing Philips Components–Signetics' specifications and operating philosophy with respect to SPC. Philips Components–Signetics believes a solid foundation creates a permanent system and accelerates our quality improvement process.

PHILIPS COMPONENTS–SIGNETICS QUALITY PERFORMANCE

Philips Components–Signetics Quality Improvement Program has influenced our entire production cycle – from the purchases of raw materials to the shipment of finished product. The involvement of all areas of the company has resulted in impressive quality improvements. A traditional quality gauge is final product electrical and visual–mechanical defect levels as measured upon first submittal results at Philips Components–Signetics outgoing Quality Assurance gates; Estimated Process Quality (This is the PPM Level at our first outgoing inspection for all accepted and rejected lots.). Current product shipments routinely record below 20PPM (Parts Per Million) electrical defect levels and 150PPM visual–mechanical defect levels. Since Philips Components–Signetics utilizes zero accept sampling on all finished production inspection, any lot with one or more rejects is 100 percent rejected.

Quality and Reliability

The most meaningful measure in our product quality is how we measure up to our customer's expectations. Many customers routinely send us incoming inspection data on our products. One major mainframe manufacturer has reported zero defects in electrical, visual–mechanical, and hermeticity and has reported a 100 percent lot acceptance rate on Philips Components–Signetics' Standard Products Group product for over a year. Due to this type of performance, an increasing number of our customers are eliminating expensive incoming inspection testing and have begun implementation of Philips Components–Signetics' Ship–to Stock Program.

PHILIPS COMPONENTS–SIGNETICS SHIP–TO–STOCK PROGRAM

Ship–to–Stock is a formal program developed at the request of our customers to help them reduce their costs by eliminating incoming test and inspection. Through close work with these customers in our quality improvement program, they became confident that our defect rates were so low that the redundancy of incoming inspections and testing was not only expensive, but unnecessary. They also saw that added component handling increased the potential of causing defects.

Ship–to–Stock is a joint program between Philips Components–Signetics and a customer which formally certifies specific parts to go directly into the customer's assembly line or inventory. This program was developed at the request of several major manufacturers after they had worked with us and had a chance to experience the data exchange and joint corrective action occurring as part of our quality improvement program.

Manufacturer using large volumes of ICs, those who are evaluating Just–in–Time delivery programs, or those who want to reduce or avoid high–cost incoming inspection are strongly encouraged to participate in this worthwhile program. Contact your local Philips Components–Signetic's sales representative for further assistance and information on how to participate in this program.

SUMMARY

The Philips Components–Signetics Quality Improvement Program has had a far–reaching impact on all aspects of our business. It has, of course, provided our customers with products of improved electrical and mechanical quality and has provided Philips Components–Signetics with a method of managing product reliability improvement to ensure that Philips Components–Signetics' products continue to perform as specified.

The corrective action teams that work to eliminate the cause of defects in Philips Components–Signetics' products are committed to producing highly reliable integrated circuits and, as demonstrated by our continually improved product reliability performance, we are well on the way to achieving our objective, **ZERO DEFECTS**.

RELIABILITY ASSURANCE PROGRAMS

FOCUS ON PRODUCT RELIABILITY

During the period from 1981 to 1984, continuing improvements in process and material quality had a significant impact on product reliability.

Since 1984, Philips Components–Signetics has intensified its effort to markedly improve product reliability. Corporate Reliability Engineering, Group and Plant Reliability Units, Philips Research Labs–Sunnyvale, and Manufacturing Engineering work jointly on numerous improvement activities. These focused activities enhance the reliability of Philips Components–Signetics future products by providing improved methods for reliability assessment, increased understanding of failure physics, advanced analytical techniques, and aid in the development of material and processes.

RELIABILITY MEASUREMENT PROGRAMS

Philips Components–Signetics has developed comprehensive product and process qualification programs to assure that its customers are receiving highly reliable products for their critical applications. Additionally, ongoing reliability monitoring programs, SURE III and Product Monitor, sample standard production on a regularly established basis (see Table I below).

Table I Reliability Assurance Programs

Reliability Function	Typical Stress	Frequency
New Process Qualification	High Temperature Operating Life Temperature–Humidity, Biased, Static High Temperature Storage Life Pressure Pot Temperature Cycle	Each new wafer fab process
New Product Qualification	High Temperature Operating Life Temperature–Humidity, Biased, Static High Temperature Storage Life Pressure Pot Temperature Cycle Electrostatic Discharge Characterization	Each new product family
SURE III	High Temperature Operating Life Temperature–Humidity, Biased, Static High Temperature Storage Life Pressure Pot Temperature Cycle	Each fab process family, every four weeks
Product Monitor	Pressure Pot	Each package types and technology family at each assembly plant, every week

DESCRIPTION OF STRESSES

SHTL–Static High Temperature Life:
SHTL stressing applies static DC bias to the device. This has specific merit in detecting ionic contamination problems which require continuous uninterrupted bias to drive contaminants to the silicon surface. The voltage bias must be maintained until the device are cooled down to room temperature from the elevated life test temperature. DHTL stressing is not as effective in detecting such problems because the bias continuously changes, intermittently generating and healing the problem. For this reason, SHTL has typically been used as the accelerated life stress for Standard Product products.

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HTSL–High Temperature Storage Life:
This stress exposes the parts to elevated temperatures (150°C–175°C) with no applied bias. For plastic packages, 175°C is the high end and of its safe temperature region without accelerating untypical failure mechanisms. This test is intended to accelerate mechanical package– related failure mechanism such as Gold–Aluminium bond integrity and other process instabilities.

THBS–Temperature–Humidity, Biased, Static:
The accelerated temperature and humidity bias is performed at 85°C and 85% relative humidity (85°C/ 85% RH). In general, the worst case bias condition is the one which minimizes the device power dissipations and maximizes the applied voltages. Higher power dissipations tend to lower the humidity level at the chip surface and lessen the corrosion susceptibility.

TMCL–Temperature–Cycling, Air to Air:
The device is cycled between the specified upper and lower temperature without power in an air or Nitrogen environment. Normal temperature extremes are –65°C and +150°C with a minimum 10 minute dwell and 5 minute transition per MIL–STD–883C, Method 1010.5, Condition C. This is a good test to measure the overall package to die mechanical compatibility, because the thermal expansion coefficients of the plastic are normally very much higher than those of the die and leadframe. However, for large die the stress may be too severe and induce failures that would not be expected in a real application.

PPOT–Pressure Pot:
This stress exposes the devices to saturated steam at elevated temperature and pressure. The standard condition is 20 PSIG which occurs at a temperature of 127°C and 100% RH. The stress is used to test the moisture resistance of plastic encapsulated devices. The plastic encapsulant is not a moisture barrier and will saturate with moisture within 72 hours. Since the chip is not powered up the chip temperature and relative humidity will be the same as the autoclave once equilibrium is reached. Because the steam environment has an unlimited supply of moisture and ample temperature to catalyze thermally activated events, it is effective at detecting corrosion problems, contamination induced leakage problems, and general glassivation stability and integrity. It is also a good test for both package integrity (cracks in the package), and for die cracks (the moisture swells the plastic enough to stress the die–also the moisture causes leakage paths in the crack itself).

PRODUCT AND PROCESS PROGRAMS

Qualification activity is centered around new products and processes and changes in products and processes. The goal is to assure that the products can meet the qualification requirements prior to general release, and on an ongoing basis to demonstrate conformance to those requirements. The nature and extent of reliability stressing required depends on the type of change and the amount of applicable reliability data available.

A full qualification may include Early Failure Rate (EFR), intrinsic Failure Rate (IFR), and Environmental Endurance Stressing. Such stress plans are reserved for introductions or changes that involve new or untested material or processes and, as such should be subjected to the maximum reliability interrogation. This normally entails a full range of biased and unbiased temperature and humidity stresses along with thermo–mechanical stresses.

For changes that are of limited scope, the full range of qualification stressing may not be warranted. In these instances, the nature and extent of the change is examined and only those stresses which provide a valuable measure of the change, or those which will detect potential weaknesses, are performed.

PHILIPS COMPONENNTS–SIGNETICS' SELF–QUAL PROGRAM (SSQP)

Self–Qual is a joint program between Philips Components–Signetics and a customer which formally communicates Philips Components–Signetics' qualification activities for a new or changed product, process, or material. The Philips Components–Signetics Self Qual process provides our customer's engineering groups an opportunity to participate in the development of the qualification plan. During the qualification process, customers may audit the project, and can receive interim updates of qualification progress. Upon completion, formal detailed engineering reports are provided.

The major impact to the customer comes from the reduced workload on the component engineering and qualification groups. These engineering resources generally divide their time between routine qualification activity and problem resolution on critical components. By eliminating the need to perform qualification for one of the basic vendor changes the customer component engineer can spend more of his time resolving the critical product issues. In addition, the total amount of stress hardware needed to perform qualification life tests and other environmental evaluations can be reduced, saving the customer facility costs and reducing operating expense.

Self–Qual is a no–risk proposition for the customer. Each Self–Qual proposal provides a detailed description of what we are changing and why. It includes a detailed plan of what we intend to do to establish the reliability of the products affected. If the customer wishes to have product added to the plan or select some additional stresses, or prefers alternative stress conditions, Philips Components–Signetics will do everything possible to accommodate those requests. After that, if the customer is still uncomfortable with the recommended change, they are under no obligation to accept our data, and they may perform their own qualification program in addition to Philips Components–Signetics.

Customers who are interested in participating in this program should contact their local Signetics sales representative or Philips Components–Signetics Corporate Reliability Engineering department directly.

SURE III RELIABILITY MONITORING PROGRAM

In order to implement an improvement program, a standard measure of performance was needed. Philips Components–Signetics uses the results from the SURE III Reliability Monitoring Program as its basic ongoing measure of product reliability performance. This program samples all generic families of products manufactured by Philips Components–Signetics, and utilizes standardized stress methods and test procedures. This system is augmented by new product and process qualification activities and infant mortality monitoring programs.

Philips Components–Signetics adopted a measurement philosophy based on the premise of continual improvement toward our performance standard of zero defects.

We also increased our standard Pressure Pot stress conditions from 15 PSIG/121°C to 20 PSIG/127°C. This reduced stress duration from 168 hours to 72 hours, and increased high volume sampling, which increased sensitivity to low defect levels.

Our standard monitoring program, SURE III, includes the stress conditions as described in Table II.

PRODUCT MONITOR

In addition to the SURE III program, each Philips Components–Signetics assembly plant performs Pressure Pot (20PSIG, 127°C, 72hours) reliability monitors on a weekly basis for each molded package type by pin count. The purpose of this program is to monitor the consistency of the assembly operations for

Quality and Reliability

such attributes as molding quality and die attach and wire bond integrity. This data is reported back to manufacturing operations and corporate and group reliability and quality assurance departments by electronic mail each week.

RELIABILITY EVALUATIONS

In addition to the product performance monitors encompassed in the SURE III program, Philips Components–Signetics' Corporate and Group Reliability Engineering departments sustain a broad range of evaluation and qualification activities.

Included in the engineering process are:

Evaluation and qualification of new or changed materials, assembly/wafer–fab processes and equipment, product designs, facilities, and subcontractors.

Devices or generic group failure rate studies.

Advanced environmental stress development.

Failure mechanism characterization and corrective action/prevention reporting.

The environmental stresses utilized in the engineering programs are similar to those utilized for the SURE III program, however, more highly –accelerated conditions and extended durations typify these engineering projects. Additional stress systems such as biased pressure pot, power–temperature cycling, and cycle–biased temperature–humidity, are often included in some evaluation programs.

STRESS FACILITY QUALITY

Philips Components–Signetics quality improvement has reached all functional areas of the company, and the reliability stress laboratories are no exception. Corporate Reliability Laboratory (CRL) is one of the many areas where the benefits of the quality improvement process pays repeated dividends.

Table II SURE III Reliability Monitoring Programs

Reliability Function	Stress Conditions
Static High Temperature Operating Life (SHTL)	$T_j \geq 150°C$, $T_A = 125°C$ to 150°C, Biased condition = Static, V_{CC} = MAX, Duration = 1000 hours
High Temperature Storage Life (HTSL)	$T_A = 150°C$, Biased condition = None, Duration = 1000 hours
Temperature–Humidity, Biased, Static (THBS)	$T_A = 85°C \pm 3°C$, Humidity = 85% RH ± 5%, Biased condition = Static, V_{CC} = MAX, Duration = 1000 hours
Temperature Cycling (TMCL)	T_A = –65°C (+0°C –10°C) to +150°C (+10°C –0°C), Air–to–Air, Dwell time = 10 minutes minimum each extreme, Biased condition = None, Duration = 1000 cycles for plastic package, 300 cycles for ceramic package
Pressure Pot	$T_A = 127°C \pm 2°C$, 20 PSIG ±0.5 PSIG (PPOT). 100% saturated steam, Biased condition = None, Duration = 72 hours

NOTE : V_{CC} = MAX is generally equal to V_{CC} = MAX as specified in Data Manual

CRI utilizes stress which accelerate failure rates hundreds to thousands of times, requiring precision and control to make reliability data meaningful. Stress loading schedules are maintained with absolute regularity and chambers are never off–line beyond scheduled loading plans. Board currents are recorded prior to and at each interval on biased stresses, and monitoring of in–oven currents is conducted daily.

Thermal modeling of the Temperature Cycling systems has been accomplished and all loads are carefully weighed to ensure that thermal ramps are consistent.

Pressure Pot and Biased Pressure Pot systems utilize microprocessor controllers, and are accurate to within 0.1 degree centigrade. Saturation is guaranteed via automatic timing circuits, and a host of fail–safe controls ensure that test groups are never damaged.

Electrostatic discharge (ESD) handling precautions are standard procedures in the laboratories, and the occurrences of devices lost, zapped, or overstressed have become almost non–existent.

RELIABILITY IMPROVEMENT PROGRAMS

Currently, Philips Components–Signetics is involved in a number of reliability improvement programs intended to enhance product reliability performance. A series of activities are currently addressing failure rate reduction in thermal cycling stresses, particularly on large die. Other reliability improvement programs involve the use of Silicon Nitride and other technologically advanced passivation systems to increase the high humidity resistance of sensitive products.

Reducing early life failures has become a major focus at Philips Components–Signetics. Numerous corrective action teams are in the process of establishing high volume monitors capable of accurately describing parts per million (PPM) level infant failure rates. From data produces via these monitors, improvement in wafer fabrication process and assembly process technologies are developed to minimize integrated circuits defect levels.

RELIABILITY PUBLICATIONS

Data from from all these activities is made available to all Philips Components–Signetics customers in a variety of publications:

PRODUCT RELIABILITY SUMMARIES AND QUARTERLY UPDATES

Yearly, each Product Group's SURE III monitoring data is summarized and published in a Product Reliabilty Summary.

Quality and Reliability

SSQP – PHILIPS COMPONENTS–SIGNETICS SELF–QUAL PROGRAM

In addition to the regular publications of reliability monitor results, a special program for the publication of qualification proposals and final engineering reports has been in place since January of 1984.

SMD RELIABILITY

In support of Philips Components–Signetics' leadership in Surface Mount Device (SMD) technology, we have published in–depth studies and evaluations on the reliability of numerous combinations of SMD packages and IC process technologies. These reports cover not only the basic product performance, but also evaluate products after exposure to the unique environments created by the various SMD soldering and cleaning processes.

SPECIAL RELIABILITY REPORTS

In addition to our standard reports, special reliability evaluation results are available on a wide variety of Philips Components–Signetics' products and processes. Custom reports can be generated to meet specific customer needs and the most accurate failure rate estimates can be prepared for your specific system application and environment.

DATA AVAILABILITY

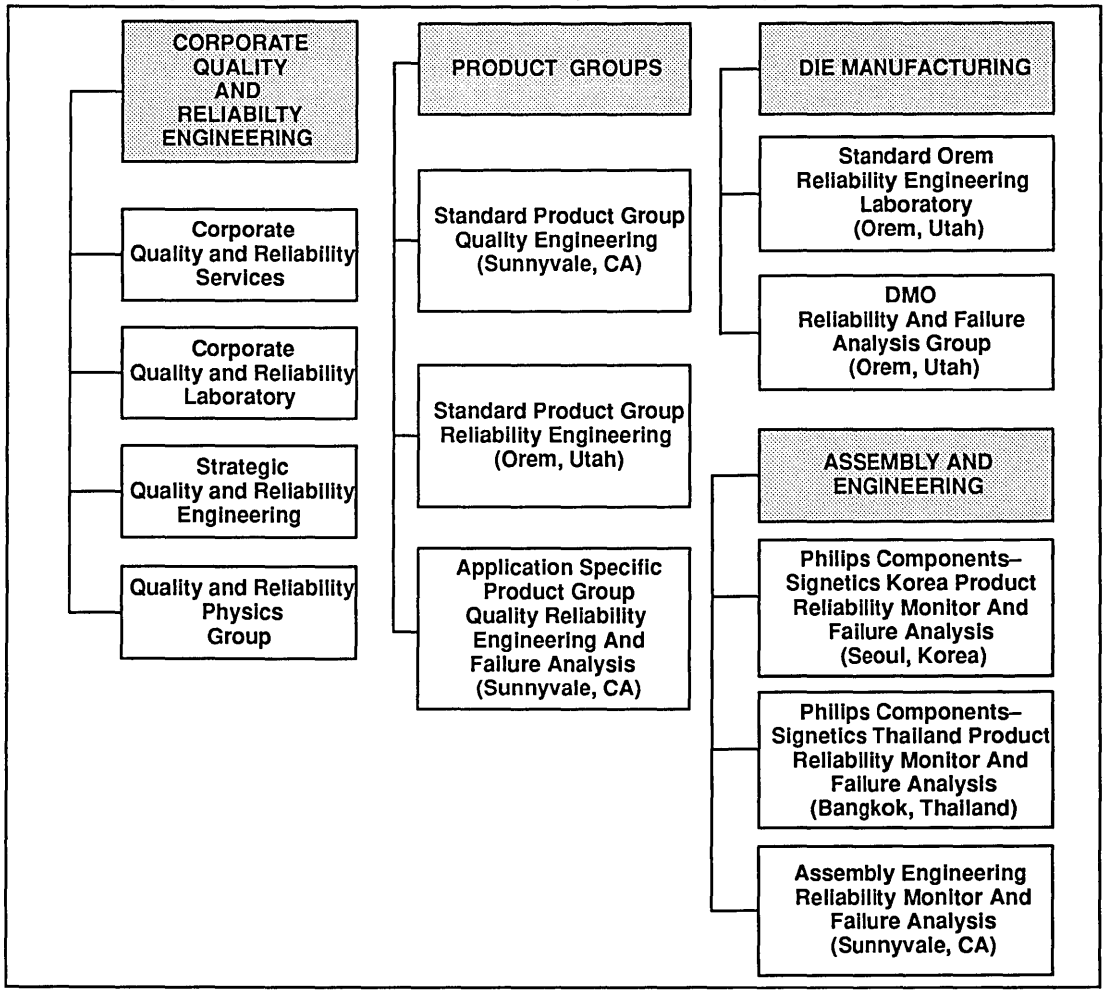
The previously referenced documents are available to all Philips Components–Signetics customers. Many are available in your local Philips Components–Signetics sales office, or:

Corporate Reliability Services
Reliability Publications Group
Department 9205, Mail Stop #34
Arques Avenue
P. O. Box 3409
Sunnyvale, CA 94088–3409, USA

where you can be placed on a standard mailing list for all documentation which meet your requirement(s).

The Table III below depicts the current organization for Philips Components–Signetics' Quality and Reliabilty Group.

Table III Philips Components–Signetics Quality And Reliability Organization Chart



Quality and Reliability

SIGNETICS' MANUFACTURING FACILITIES

Philips Components–Signetics, as part of a multinational corporation, utilize manufacturing facilities for wafer fabrication, package assembly, and test in threes states and three overseas countries as shown in Table I. All wafer fabrication is performed in Philips Components–Signetics operated fabs which report to the Vice President of Die Manufacturing Operations (DMO) in Sunnyvale. Similarly, Signetics Assembly operations in Utah, Korea, and Thailand, report to the Vice President of Assembly Manufacturing Operations (AMO). Assembly subcontractors, Anam, Hyundai, MEC, Peibei, and Team are scheduled and controlled through the AMO organization. Assembly subcontractors process all product to Philips Components–Signetics' specifications and materials. Philips Components–Signetics has onsite quality assurance personnel at each subcontractor to audit assembly processes and procedures.

Table IV Philips Components–Signetics Product Manufacturing

Facilities	Designation	Location	Process or Package Families
Wafer Fabrication	Fab 01	Sunnyvale, California, USA	Bipolar Junction Isolated and Quality Assurance
	Fab 16	Sunnyvale, California, USA	Oxide Isolated, BICMOS and Quality Assurance
	Fab 21	Orem, Utah, USA	Bipolar Gold Doped, Schottky, Oxide Isolated, ECL, and Quality Assurance
	Fab 22	Albuquerque, New Mexico, USA	ACMOS, EPROM and Quality Assurance
Assembly	Anam	Seoul, Korea	SO, PLCC, Metal Can and Quality Assurance
	Hyundai	Ichon, Kyungki, Korea	Ceramic DIP (CERDIP) and Quality Assurance
	MEC	Osaka, Japan	SO EIAJ, QFP 44 and Quality Assurance
	Orem	Orem, Utah, USA	Military Final Test and Quality Assurance
	Pebel	Kaomsiung, Taiwan	PDIP, SO, PLCC, and Quality Assurance
	SigKor	Seoul, Korea	PDIP, SO and PLCC, and Quality Assurance
	Sig Thai	Bangkok, Thailand	PDIP and Ceramic DIP(CERDIP) and Quality Assurance
	Team	Manila, Philippine	PDIP and Quality Assurance
Test	TAO3	Sunnyvale, California, USA	Wafer Sort, Final Test and Quality Assurance
	SigKor	Seoul, Korea	Final Test and Quality Assurance
	SigThai	Bangkok, Thailand	Final Test and Quality Assurance

TYPICAL IC MANUFACTURING FLOW

The manufacturing process for integrated Circuits begins with wafer fabrication. The wafers are then electrically sorted, assembled, and tested prior to customer shipment. Quality assurance inspections are utilized throughout the manufacturing process.

Table V Package Construction

Items	Plastic DIP	SO/PLCC	Ceramic DIP(CERDIP)	Ceramic Flat Pack
Lead Frame	Copper, 194 Alloy	Copper, 194 or PMC102	Alloy–42	Alloy–42
Lead Finish	Tin/Lead Solder Dip (60/40)	Tin/Lead Solder Dip (60/40) or Solder Plate (80/20)	Tin/Lead Solder Dip (60/40)	Tin/Lead Solder Dip (60/40)
Bond Area Finish	Silver Spot	Silver Spot	Silver Spot	Silver Spot
Die Attach	Silver Filled Polymide or Themoplastic	Silver Filled Polymide or Thermoplastic	Silver Filled Glass	Silver Filled Glass
Bond Wire	Gold, 1.0–1.3 mils in Diameter	Gold, 1.0–1.3 mils in Diameter	Aluminum, 1.0–1.3 mils in Diameter	Aluminum, 1.0–1.3 mils in Diameter
Wire Bonding Die Lead Frame	Thermosonic Ball Stitch	Thermosonic Ball Stitch	Ultrasonic Stitch Stitch	Ultrasonic Stitch Stitch
Package Material	Novolac Epoxy	Novolac Epoxy	Ceramic	Ceramic

Quality and Reliability

Table VI Package Code Definition (For internal use)

Pin count	Plastic DIP	Plastic SO	PLCC	Ceramic DIP	Ceramic Flat Pack
16	NJ1	DJI	–	FJ1	–
24	NN3	–	–	FN1 FN2 FN3	YN1
28	–	–	AQ1	–	–

Section 3
Family Characteristics

INDEX

Family Specifications

GENERAL

These family specifications cover the common electrical ratings and characteristics of the entire 74ABT family, unless otherwise specified in the individual device data sheet.

INTRODUCTION

The 74ABT Advanced BiCMOS family combines the low power dissipation and low noise of BiCMOS with the high speed and high output drive of our bipolar modules.

The basic family of devices designated as 74ABTXXX will operate at BiCMOS input logic levels for high noise immunity, negligible quiescent supply and input current. It is operated from a power supply of 4.5 to 5.5V.

HANDLING MOS DEVICES

Inputs and outputs are protected against electrostatic effects in a wide variety of device-handling situations. However, to be totally safe, it is desirable to take handling precautions into account.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[2]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_O	DC output voltage[2]	output in Off or High state	-0.5 to +5.5	V
I_O	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

Family Specifications

DC ELECTRICAL CHARACTERISTICS

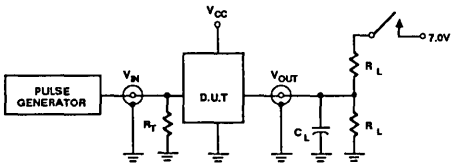
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = -18mA			-1.2		-1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5			2.5		V
		V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0			3.0		
		V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]	V_{CC} = 5.5V; V_O = 2.5V	-50	-100	-180	-50	-180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		24	30		30	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]	Outputs enabled, one input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA
		Outputs 3-State, one data input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	50		50	µA
		Outputs 3-State, one enable input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

Family Specifications

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

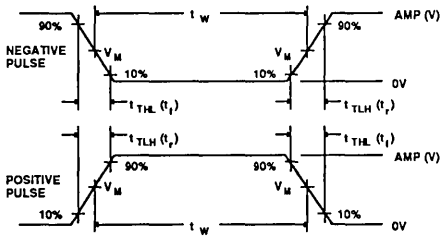
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



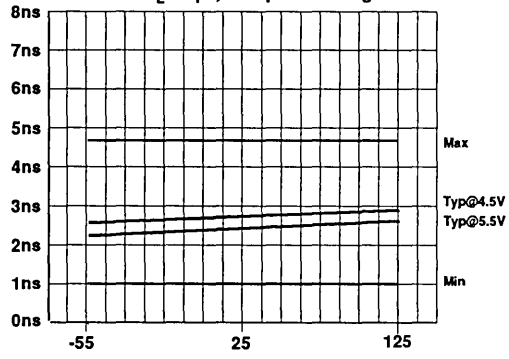
V_M = 1.5V

Input Pulse Definition

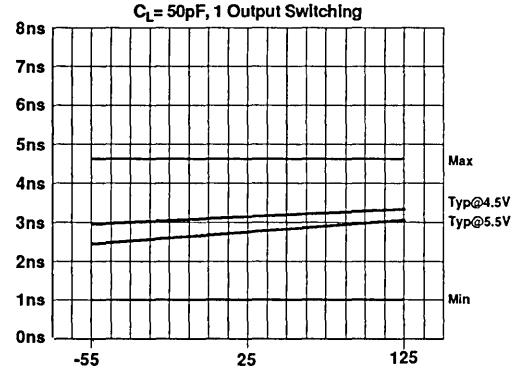
FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

Family Specifications

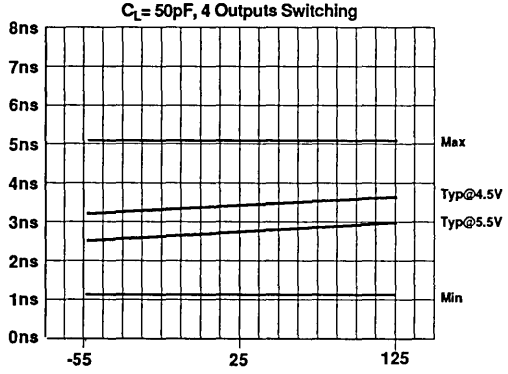
TPLH vs. TEMPERATURE (T_{amb})
C_L= 50pF, 1 Output Switching



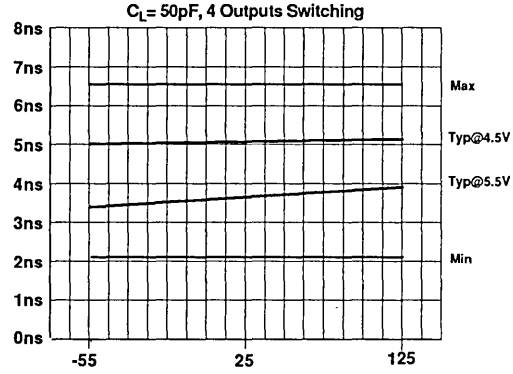
TPHL vs. TEMPERATURE (T_{amb})
C_L= 50pF, 1 Output Switching



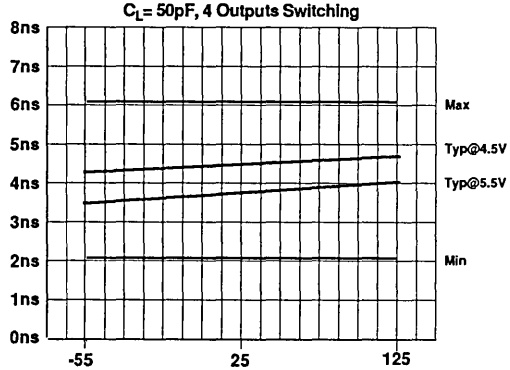
TPZH vs. TEMPERATURE (T_{amb})
C_L= 50pF, 4 Outputs Switching



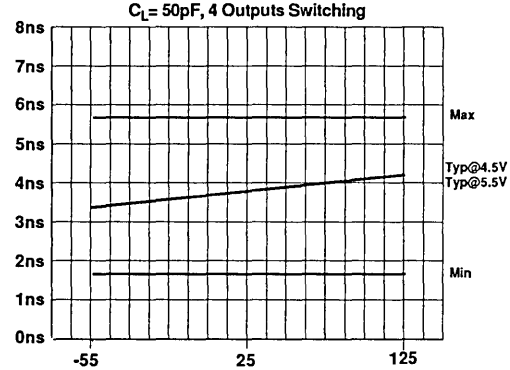
TPHZ vs. TEMPERATURE (T_{amb})
C_L= 50pF, 4 Outputs Switching



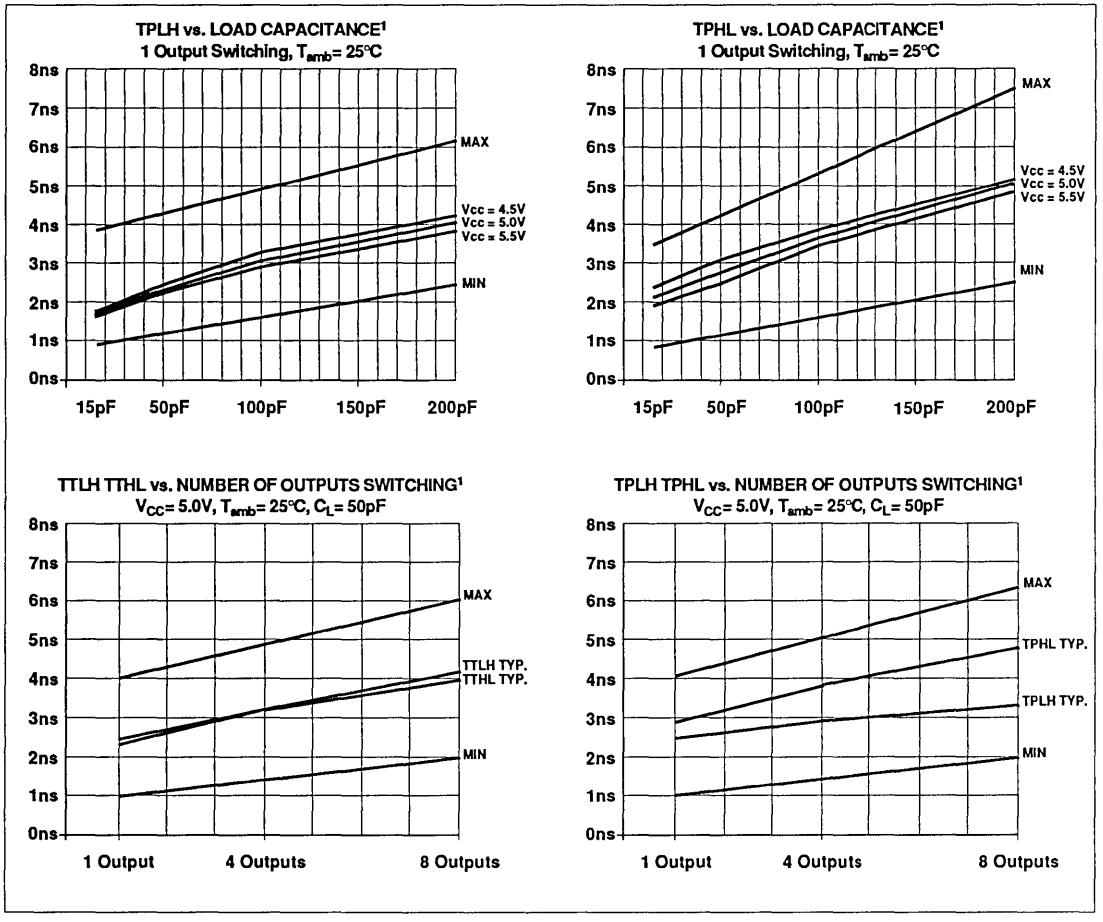
TPZL vs. TEMPERATURE (T_{amb})
C_L= 50pF, 4 Outputs Switching



TPLZ vs. TEMPERATURE (T_{amb})
C_L= 50pF, 4 Outputs Switching

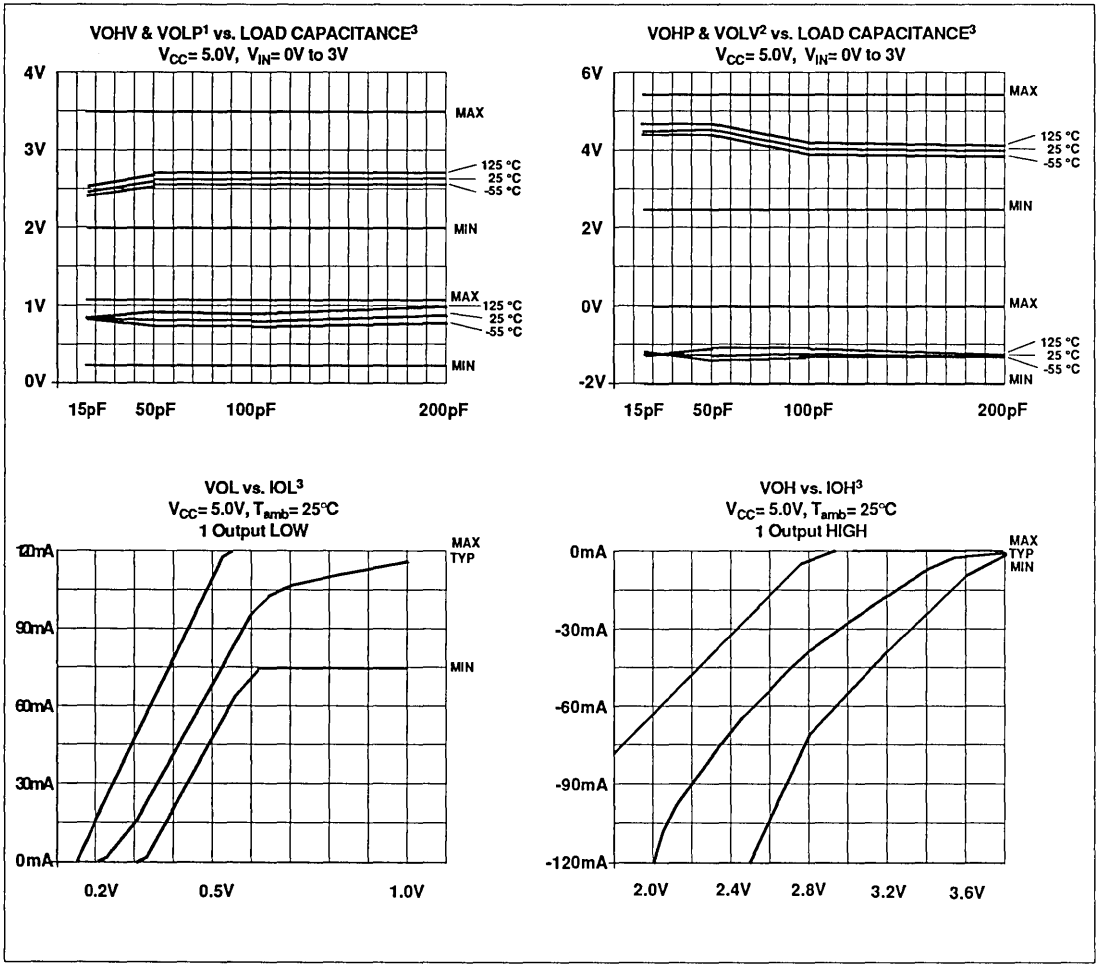


Family Specifications



NOTES:
1. MIN and MAX lines are design characteristics and are not necessarily guaranteed by test.

Family Specifications



NOTES:

1. VOHV is defined as the minimum (valley) voltage induced on a quiescent high-level output during switching of other outputs. VOLP is defined as the maximum (peak) voltage induced on a quiescent low-level output during switching of other outputs.
2. VOHP is defined as the maximum (peak) voltage induced on a quiescent high-level output during switching of other outputs. VOLV is defined as the minimum (valley) voltage induced on a quiescent low-level output during switching of other outputs.
3. MIN and MAX lines are design and process characteristics. They are not necessarily guaranteed by test.

Data Sheet Specification Guide

INTRODUCTION

The 74ABT data sheets have been designed for ease-of-use. A minimum of cross-referencing for more information is needed.

TYPICAL PROPAGATION DELAY AND FREQUENCY

The typical propagation delays listed at the top of the data sheets are the average of t_{PLH} and t_{PHL} for a typical data path through the device with a 50pF load.

For clocked devices, the maximum frequency of operation is also given. The typical operating frequency is the maximum device operating frequency with a 50% duty factor and no constraints on t_R and t_F.

LOGIC SYMBOLS

Two logic symbols are given for each device - the conventional one (Logic Symbol) which explicitly shows the internal logic (except for complex logic) and the IEEE/IEC Logic Symbol.

The IEEE/IEC has been developing a very powerful symbolic language that can show the relationship of each input of a digital logic current to each output without explicitly showing the internal logic.

ABSOLUTE MAXIMUM RATINGS

The Absolute Maximum Ratings table lists the maximum limits to which the device can be subjected without damage. This does not imply that the device will function at these extreme conditions, only that, when these conditions are removed and the device operated within the Recommended Operating Conditions, it will still be functional and its useful life will not have been shortened.

RECOMMENDED OPERATING CONDITIONS

The "Recommended Operating Conditions" table lists the operating ambient temperature and the conditions under which the limits in the "DC Characteristics" and "AC Characteristics" table will be met. The table should not be seen as a set of limits guaranteed by the manufacturer, but as the conditions used to test the devices and guarantee that they will then meet the limits in the DC and AC Characteristics tables.

TEST CIRCUITS

Good high-frequency wiring practices should be used in test circuits. Capacitor leads should be as short as possible to minimize ripples on the output waveform transitions and undershoot. Generous ground metal (preferably a ground plane) should be used for the same reasons. A V_{CC} decoupling capacitor should be provided at the test socket, also with short leads. Input signals should have rise and fall times of 3ns, a signal swing of 0V to V_{CC}; a 5MHz square wave is recommended for most propagation delay tests. The repetition rate must be increased for testing f_{MAX}. Two pulse generators are usually required for testing such parameters as setup time, hold time and removal time. f_{MAX} is also tested with 3ns input rise and fall times, with a 50% duty factor, but for typical f_{MAX} as high as 150MHz, there are no constraints on rise and fall times.

DC CHARACTERISTICS

The "DC Characteristics" table reflects the DC limits used during testing. The values published are guaranteed.

The threshold values of V_{IH} and V_{IL} are applied to the inputs, the output voltages will be those published in the "DC Characteristics" table. There is a tendency, by some, to use the published V_{IH} and V_{IL} thresholds to test a device for functionality in a "function-table exerciser" mode. This frequently causes problems because of the noise present at the test head of automated test equipment with cables up to 1 meter. Parametric tests, such as those used for the output levels under the V_{IH} and V_{IL} conditions are done fairly slowly, in the order of milliseconds, so that there is no noise at the inputs when the outputs are measured. But in functionality testing, the outputs are measured much faster, so there can be noise on the inputs, before the device has assumed its final and correct output state. Thus, never use V_{IH} and V_{IL} to test the functionality of any ABT device type; instead, use input voltages of V_{CC} (for the High state) and 0V (for the Low state). In no way does this imply that the devices are noise-sensitive in the final system.

In the data sheets, it may appear strange that the typical V_{IL} is higher than the maximum V_{IL}. However, this is because V_{ILMAX} is the maximum V_{IL} (guaranteed) for all devices that will be recognized as a logic Low. However, typically a higher V_{IL} will also be recognized as a logic Low. Conversely, the typical V_{IH} is lower than its minimum guaranteed level.

The quiescent supply current I_{CC} is the leakage current of all the reversed-biased diodes and the OFF-state MOS transistors.

AC CHARACTERISTICS

The "AC Characteristics" table lists the guaranteed limits when a device is tested under the conditions given in the AC Test Circuits and Waveform section.

PROPAGATION DELAY

The data included in this section is meant to aid the designer in understanding system performance over a wider range of operating temperatures and load conditions, as well as at varying voltages. It should be noted that these design characteristics are not 100% tested but should very closely reflect actual device performance over the ranges specified.

Definitions of Symbols

DEFINITIONS OF SYMBOLS AND TERMS USED IN ABT DATA SHEETS

Current

Positive current is defined as conventional current flow into a device.

Negative current is defined as conventional current flow out of a device.

I_{CCH} Quiescent power supply current; the current flowing into the V_{CC} supply terminal when the output is at the High level.

I_{CCL} Quiescent power supply current; the current flowing into the V_{CC} supply terminal when the output is at the Low level.

I_{CCZ} Quiescent power supply current; the current flowing into the V_{CC} supply terminal when the output is in the disabled mode.

ΔI_{CC} Additional quiescent supply current per input pin at a specified input voltage and V_{CC}.

I_{GND} Quiescent power supply current; the current flowing into the GND terminal.

I_I Input leakage current; the current flowing into a device at a specified input voltage and V_{CC}.

I_{IK} Input diode current; the current flowing into a device at a specified input voltage.

I_{IO} Input/output source or sink current; the current flowing into a device at a specified input/output voltage.

I_O Output source or sink current; the current flowing into a device at a specified output voltage.

I_{OH} High level output source current; the current into an output with input conditions applied that, according to the product specification, will establish a High level at the output. Current out of the output is given as a negative value.

I_{OL} Low level output source current; the current into an output with input conditions applied that, according to the product specification, will establish a Low level at the output. Current out of the output is given as a negative value.

I_{OK} Output diode current; the current flowing into a device at a specified output voltage.

I_{OZ} OFF-state output current; the leakage current flowing into the output of a 3-State device in the OFF-state, when the output is connected to V_{CC} or GND.

Voltages

All voltages are referenced to GND (ground), which is typically 0V.

GND Supply voltage; for a device with a single negative power supply, the most negative power supply, used as the reference level for other voltages; typically ground.

V_{CC} Supply voltage; the most positive potential on the device.

V_{EE} Supply voltage; one of two (GND and V_{EE}) negative power supplies.

V_H Hysteresis voltage; difference between the trigger levels when applying a positive and a negative-going input signal.

V_{IH} High-level input voltage; the range of input voltages that represents a logic High-level in the system.

V_{IL} Low-level input voltage; the range of input voltages that represents a logic Low-level in the system.

V_{OH} High-level output voltage; the range of voltages at an output terminal with a specified output loading and supply voltage. Device inputs are conditioned to establish a High-level at the output.

V_{OHP} Maximum (peak) voltage induced on a quiescent High-level output during switching of other outputs.

V_{OHV} Minimum (valley) voltage induced on a quiescent High-level output during switching of other outputs.

V_{OL} Low-level output voltage; the range of voltages at an output terminal with a specified output loading and supply voltage. Device inputs are conditioned to establish a Low-level at the output.

V_{OLP} Maximum (peak) voltage induced on a quiescent Low-level output during switching of other outputs.

V_{OLV} Minimum (valley) voltage induced on a quiescent Low-level output during switching of other outputs.

Definitions of Symbols

V_{T+} Trigger threshold voltage; positive-going signal.

V_{T-} Trigger threshold voltage; negative-going signal.

Capacitances

C_I Input capacitance; the capacitance measured at a terminal connected to an input of a device.

$C_{I/O}$ Input/Output capacitance; the capacitance measured at a terminal connected to an I/O pin (e.g. a transceiver).

C_L Output load capacitance; the capacitance connected to an output terminal including jig and probe capacitance.

C_{PD} Power dissipation capacitance; the capacitance used to determine the dynamic power dissipation per logic function when no extra load is provided to the device.

AC Switching Parameters

f_I Input frequency; for combinatorial logic devices the maximum number of inputs and outputs switching in accordance with the device function table. For sequential logic devices the clock frequency using alternate High and Low for data input or using the toggle mode, whichever is applicable.

f_O Output frequency; each output.

f_{MAX} Maximum clock frequency; clock input waveforms should have a 50% duty factor and be such as to cause the outputs to be switching from 10% V_{CC} to 90% V_{CC} in accordance with device function table.

t_H Hold time; the interval immediately following the active transition of the timing pulse (usually the clock pulse) or following the transition of the control input to its latching level, during which interval the data to be recognized must be maintained at the input to ensure their continued recognition. A negative hold time indicates that the correct logic level may be released prior to the timing pulse and still be recognized.

t_R, t_F Clock input rise and fall times; 10% and 90% values.

t_{PHL} Propagation delay time: The time between specified reference points on the input and the output waveforms with the output changing from the defined High-level to Low-level.

t_{PLH} Propagation delay time: The time between specified reference points on the input and the output waveforms with the output changing from the defined Low-level to High-level.

t_{PHZ} Output Disable time from High level to a 3-State output: The delay time between the specified reference points on the input and output voltage waveforms with the 3-State output changing from the High-level to a high impedance "OFF" state.

t_{PLZ} Output Disable time from Low level of a 3-State output: The delay time between the specified reference points on the input and output voltage waveforms with the 3-State output changing from the Low-level to a high impedance "OFF" state.

t_{PZH} Output Enable time to a High level of a 3-State output: The delay time between the specified reference points on the input and output voltage waveforms with the 3-State output changing from a high impedance "OFF" state to a High-level.

t_{PZL} Output Enable time to a Low level of a 3-State output: The delay time between the specified reference points on the input and output voltage waveforms with the 3-State output changing from a high impedance "OFF" state to a Low level.

t_{REC} Recovering time: The time between the reference point on the trailing edge of an asynchronous input control pulse and the reference point on the activating edge of a synchronous (clock) pulse input such that the device will respond to the synchronous input.

t_S Setup time; the interval immediately preceding the active transition of the timing pulse (usually the clock pulse) or preceding the transition of the control input to its latching level, during which interval data to be recognized must be maintained at the input to ensure their recognition. A negative setup time indicates that the correct logic level may be initiated sometime after the active transition of the timing pulse and still be recognized.

t_{THL} Output transition time; the time between two specified reference points on a waveform, normally 90% and 10% points, that is changing from High-to-Low.

t_{TLH} Output transition time; the time between two specified reference points on a waveform, normally 10% and 90% points, that is changing from Low-to-High.

t_W Pulse width: The time between the reference point on the leading and trailing edges of a pulse.

Section 4
Data Sheets

INDEX

Document No.	
ECN No.	
Date of Issue	July 1990
Status	Objective Specification
Advanced BiCMOS Products	

74ABT240

Octal inverting buffer (3-State)

FEATURES

- Octal bus interface
- 3-State buffers
- Output capability: +64mA/-32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The 74ABT240 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT240 device is an octal buffer that is ideal for driving bus lines or buffer memory address registers. The device features two Output Enables ($1\overline{OE}$, $2\overline{OE}$), each controlling four of the 3-State outputs.

FUNCTION TABLE

INPUTS				OUTPUT	
$1\overline{OE}$	$1A_n$	$2\overline{OE}$	$2A_n$	$1\overline{Y}_n$	$2\overline{Y}_n$
L	L	L	L	H	H
L	H	L	H	L	L
H	X	H	X	Z	Z

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay A_n to $\overline{Y}_n$	C_L = 50pF; V_{CC} = 5V	3.5	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

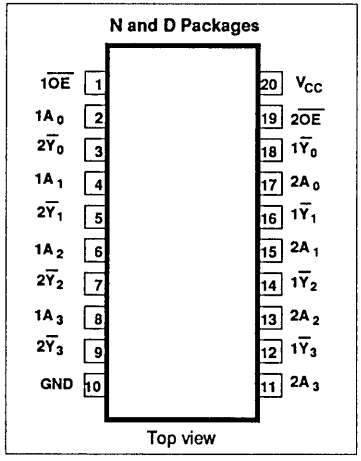
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP	-40°C to +85°C	74ABT240N
20-pin plastic SOL	-40°C to +85°C	74ABT240D

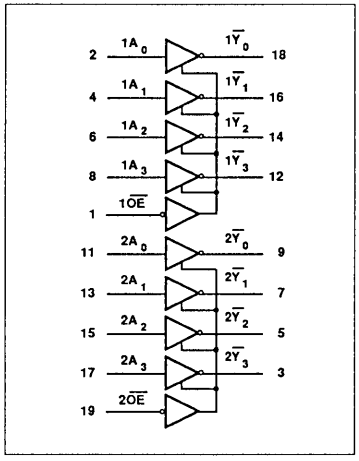
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 4, 6, 8	$1A_0$ - $1A_3$	Data inputs
11, 13, 15, 17	$2A_0$ - $2A_3$	Data inputs
18, 16, 14, 12	$1\overline{Y}_0$ - $1\overline{Y}_3$	Data outputs
9, 7, 5, 3	$2\overline{Y}_0$ - $2\overline{Y}_3$	Data outputs
1, 19	$1\overline{OE}$, $2\overline{OE}$	Output enables
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

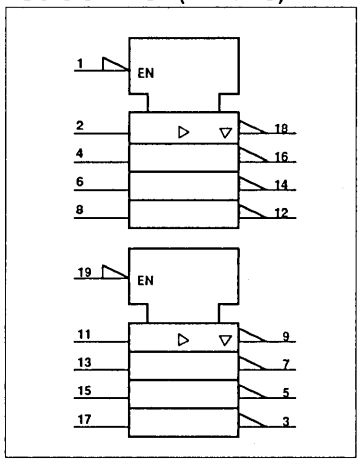
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Octal inverting buffer (3-State) 74ABT240

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[2]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_O	DC output voltage[2]	output in Off or High state	-0.5 to +5.5	V
I_O	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

Octal inverting buffer (3-State) 74ABT240

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = -18mA			-1.2		-1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5			2.5		V
		V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0			3.0		
		V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]	V_{CC} = 5.5V; V_O = 2.5V	-50	-100	-180	-50	-180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		24	30		30	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]	Outputs enabled, one input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA
		Outputs 3-State, one data input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	50		50	µA
		Outputs 3-State, one enable input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

Document No.	
ECN No.	
Date of Issue	August 20, 1990
Status	Preliminary Specification
Advanced BiCMOS Products	

74ABT241

Octal buffer/line driver (3-State)

FEATURES

- Octal bus interface
- 3-State buffers
- Output capability: +64 mA/-32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The 74ABT241 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT241 device is an octal buffer that is ideal for driving bus lines or buffer memory address registers. The device features two Output Enables ($1\overline{OE}$, 2OE), each controlling four of the 3-State outputs.

QUICK REFERENCE DATA

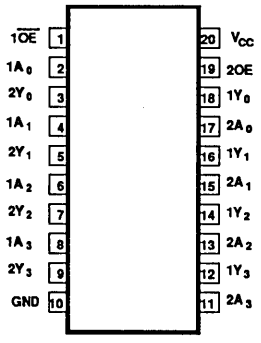
SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay A_n to Y_n	C_L = 50pF; V_{CC} = 5V	2.9	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-Pin Plastic DIP	-40°C to +85°C	74ABT241N
20-Pin Plastic SOL	-40°C to +85°C	74ABT241D

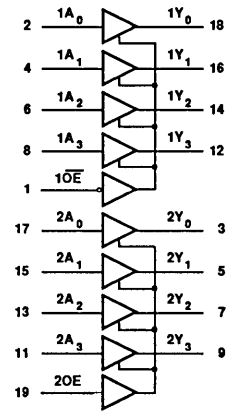
PIN CONFIGURATION

N and D Packages

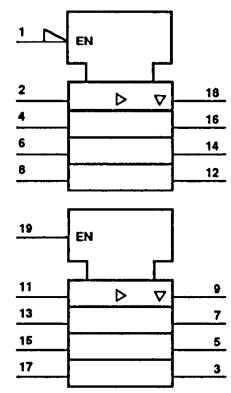


Top view

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Octal buffer/line driver (3-State) 74ABT241

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[2]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_O	DC output voltage[2]	output in Off or High state	-0.5 to +5.5	V
I_O	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

FUNCTION TABLE

INPUTS				OUTPUT	
$1\overline{OE}$	$1A_n$	2OE	$2A_n$	$1Y_n$	$2Y_n$
L	L	H	L	L	L
L	H	H	H	H	H
H	X	L	X	Z	Z

PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
2, 4, 6, 8	$1A_0$ - $1A_3$	Data inputs
17, 15, 13, 11	$2A_0$ - $2A_3$	Data inputs
18, 16, 14, 12	$1Y_0$ - $1Y_3$	Data outputs
3, 5, 7, 9	$2Y_0$ - $2Y_3$	Data outputs
1, 19	$1\overline{OE}$, 2OE	Output enables
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

Octal buffer/line driver (3-State) 74ABT241

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = -18mA			-1.2		-1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5			2.5		V
		V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0			3.0		
		V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]	V_{CC} = 5.5V; V_O = 2.5V	-50	-100	-180	-50	-180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		24	30		30	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]	Outputs enabled, one input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA
		Outputs 3-State, one data input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	50		50	µA
		Outputs 3-State, one enable input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

Octal buffer/line driver (3-State) 74ABT241

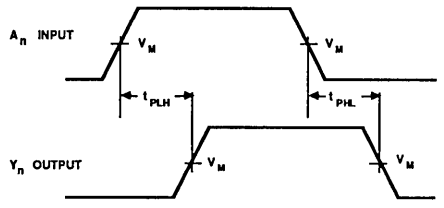
AC CHARACTERISTICS

GND = 0V; $t_R = t_F = 2.5ns$; $C_L = 50pF$, $R_L = 500\Omega$

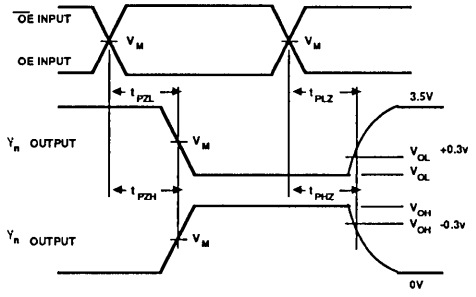
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = -40°C to +85°C, V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to Y_n	1	1.0 1.0	2.6 2.9	4.1 4.2	1.0 1.0	4.6 4.6	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.1 1.3	4.8 4.3	6.3 5.8	1.1 1.3	6.8 6.8	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	1.1 1.0	4.1 3.9	5.6 5.4	1.1 1.0	6.6 5.9	ns

AC WAVEFORMS

(V_M = 1.5V, V_{IN} = GND to 3.0V)

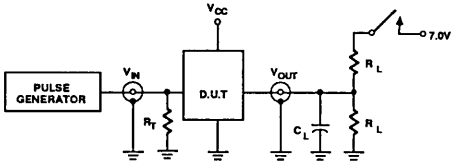


Waveform 1. Waveforms Showing the Input (A_n) to Output (Y_n) Propagation Delays



Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

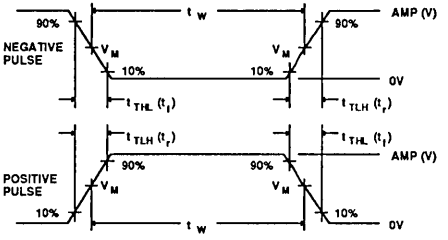
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



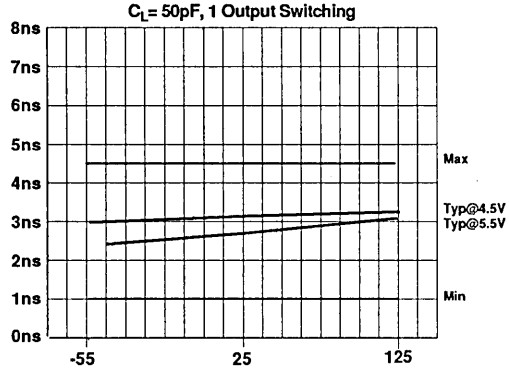
V_M = 1.5V

Input Pulse Definition

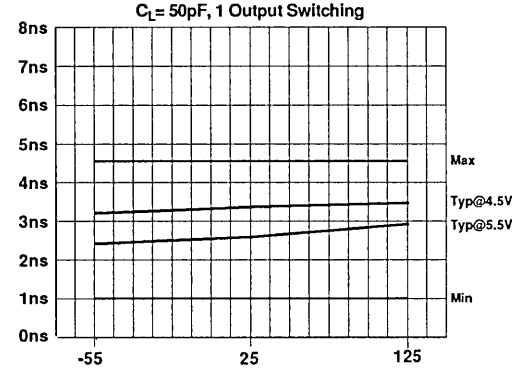
FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

Octal buffer/line driver (3-State) 74ABT241

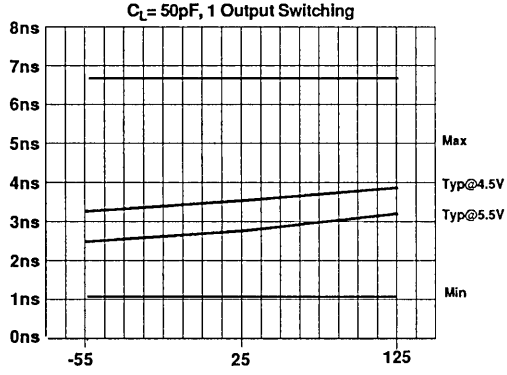
TPLH vs. TEMPERATURE (T_{amb})
C_L= 50pF, 1 Output Switching



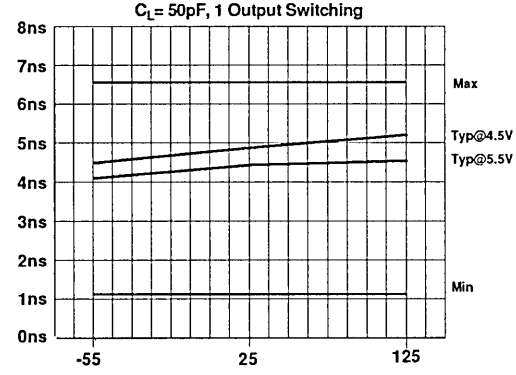
TPHL vs. TEMPERATURE (T_{amb})
C_L= 50pF, 1 Output Switching



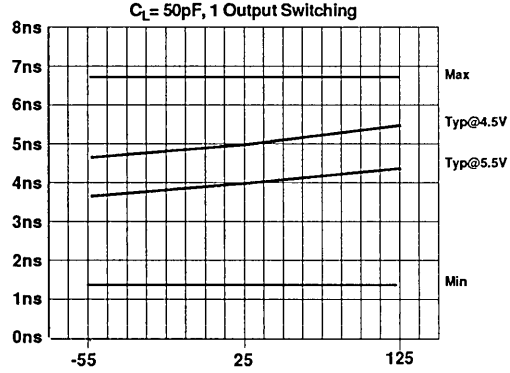
TPZH vs. TEMPERATURE (T_{amb})
C_L= 50pF, 1 Output Switching



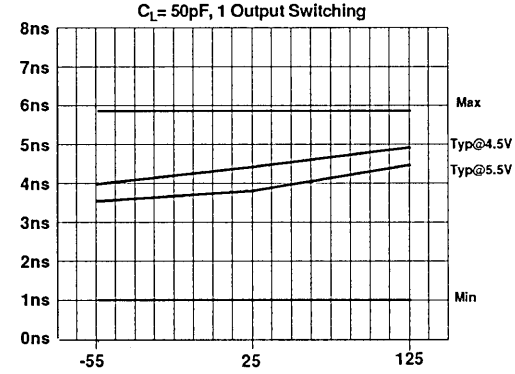
TPHZ vs. TEMPERATURE (T_{amb})
C_L= 50pF, 1 Output Switching



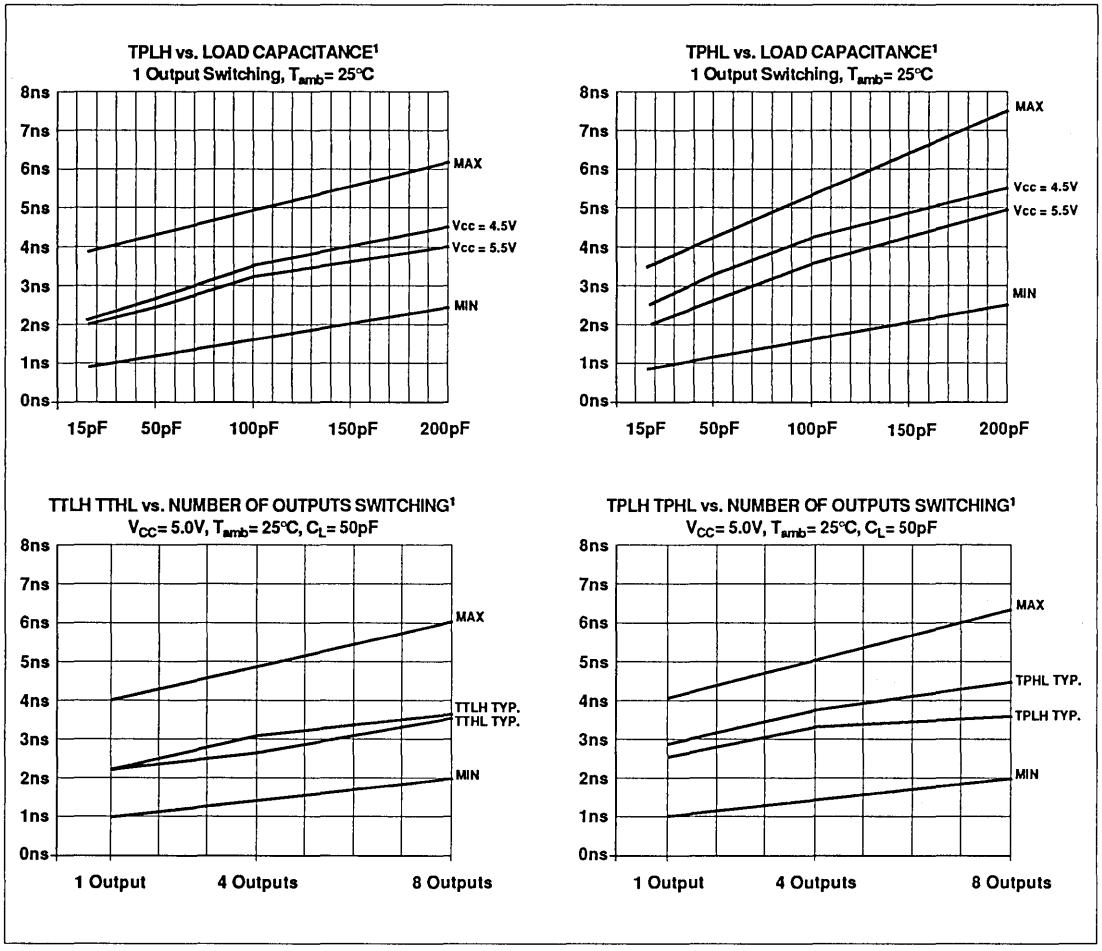
TPZL vs. TEMPERATURE (T_{amb})
C_L= 50pF, 1 Output Switching



TPLZ vs. TEMPERATURE (T_{amb})
C_L= 50pF, 1 Output Switching

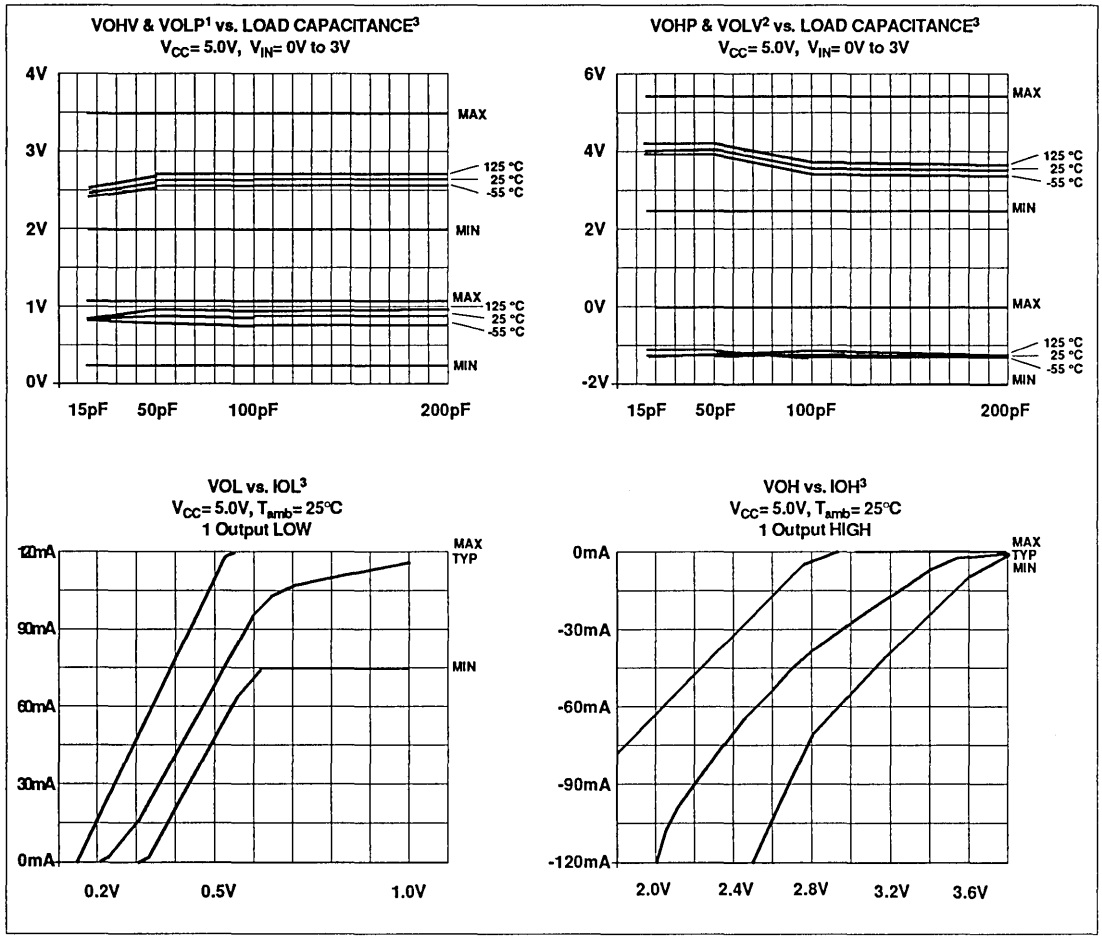


Octal buffer/line driver (3-State) 74ABT241



NOTES:
1. MIN and MAX lines are design characteristics and are not necessarily guaranteed by test.

Octal buffer/line driver (3-State) 74ABT241



NOTES:

1. VOHV is defined as the minimum (valley) voltage induced on a quiescent high-level output during switching of other outputs. VOLP is defined as the maximum (peak) voltage induced on a quiescent low-level output during switching of other outputs.
2. VOHP is defined as the maximum (peak) voltage induced on a quiescent high-level output during switching of other outputs. VOLV is defined as the minimum (valley) voltage induced on a quiescent low-level output during switching of other outputs.
3. MIN and MAX lines are design and process characteristics. They are not necessarily guaranteed by test.

Philips Components—Signetics

Document No.	
ECN No.	853-1444 00227
Date of Issue	August 20, 1990
Status	Product Specification
Advanced BiCMOS Products	

74ABT244

Octal buffer/line driver (3-State)

FEATURES

- Octal bus interface
- 3-State buffers
- Output capability: +64 mA/-32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The 74ABT244 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT244 device is an octal buffer that is ideal for driving bus lines or buffer memory address registers. The device features two Output Enables ($1\overline{OE}$, $2\overline{OE}$), each controlling four of the 3-State outputs.

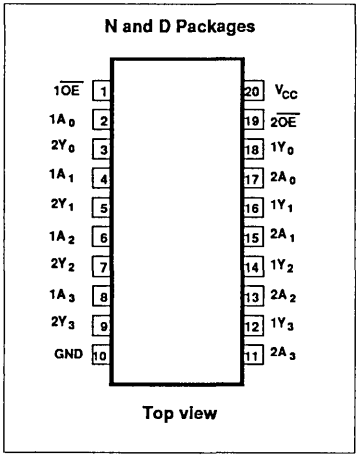
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay A_n to Y_n	C_L = 50pF; V_{CC} = 5V	2.9	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

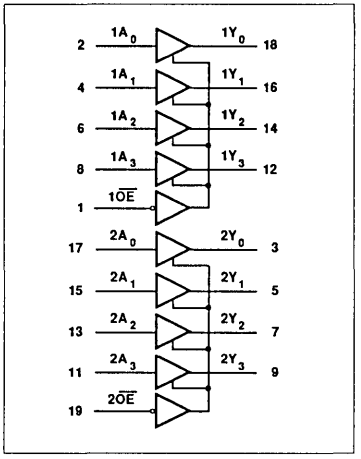
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-Pin Plastic DIP	-40°C to +85°C	74ABT244N
20-Pin Plastic SOL	-40°C to +85°C	74ABT244D

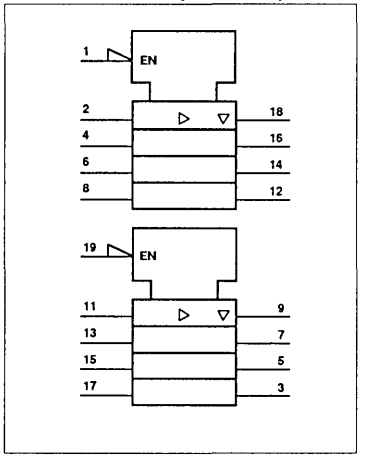
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Octal buffer/line driver (3-State) 74ABT244

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[2]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_O	DC output voltage[2]	output in Off or High state	-0.5 to +5.5	V
I_O	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

FUNCTION TABLE

INPUTS				OUTPUT	
$1\overline{OE}$	$1A_n$	$2\overline{OE}$	$2A_n$	$1Y_n$	$2Y_n$
L	L	L	L	L	L
L	H	L	H	H	H
H	X	H	X	Z	Z

PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
2, 4, 6, 8	$1A_0$ - $1A_3$	Data inputs
17, 15, 13, 11	$2A_0$ - $2A_3$	Data inputs
18, 16, 14, 12	$1Y_0$ - $1Y_3$	Data outputs
3, 5, 7, 9	$2Y_0$ - $2Y_3$	Data outputs
1, 19	$1\overline{OE}$, $2\overline{OE}$	Output enables
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = -18mA			-1.2		-1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5			2.5		V
		V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0			3.0		
		V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]	V_{CC} = 5.5V; V_O = 2.5V	-50	-100	-180	-50	-180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		24	30		30	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]	Outputs enabled, one input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA
		Outputs 3-State, one data input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	50		50	µA
		Outputs 3-State, one enable input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

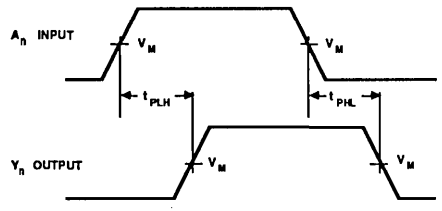
AC CHARACTERISTICS

GND = 0V; $t_R = t_F = 2.5ns$; $C_L = 50pF$, $R_L = 500\Omega$

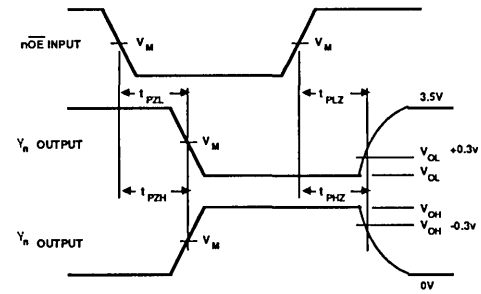
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = -40°C to +85°C, V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to Y_n	1	1.0 1.0	2.6 2.9	4.1 4.2	1.0 1.0	4.6 4.6	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.1 2.1	3.1 4.1	4.6 5.6	1.1 2.1	5.1 6.1	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	2.1 1.7	4.1 3.7	5.6 5.2	2.1 1.7	6.6 5.7	ns

AC WAVEFORMS

(V_M = 1.5V, V_{IN} = GND to 3.0V)

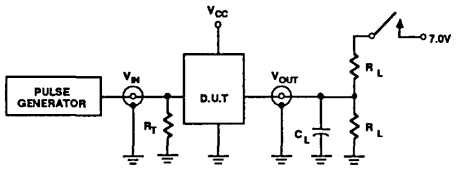


Waveform 1. Waveforms Showing the Input (A_n) to Output (Y_n) Propagation Delays



Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

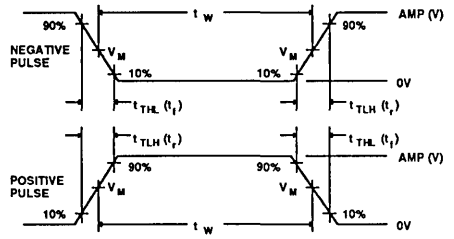
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



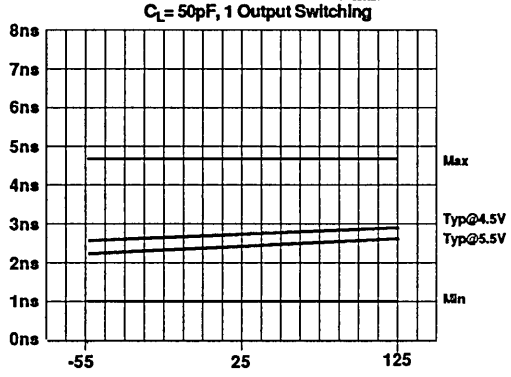
V_M = 1.5V

Input Pulse Definition

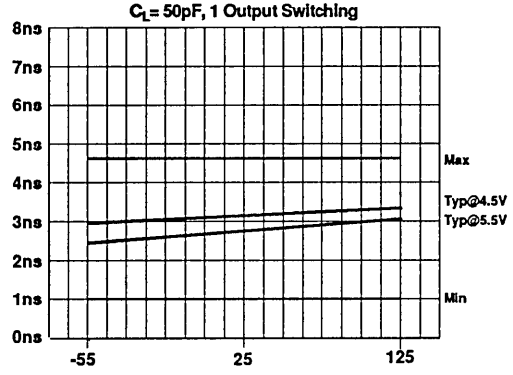
FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

Octal buffer/line driver (3-State) 74ABT244

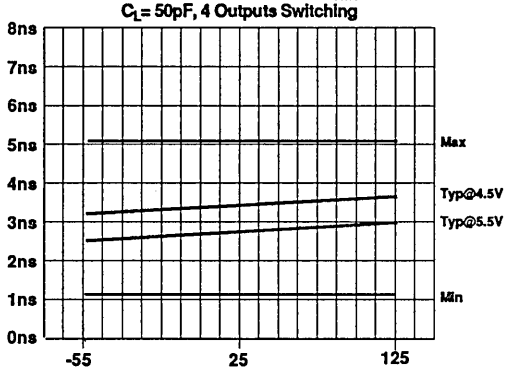
TPLH vs. TEMPERATURE (T_{amb})
C_L= 50pF, 1 Output Switching



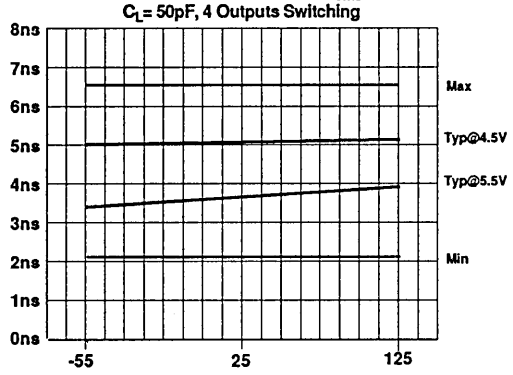
TPHL vs. TEMPERATURE (T_{amb})
C_L= 50pF, 1 Output Switching



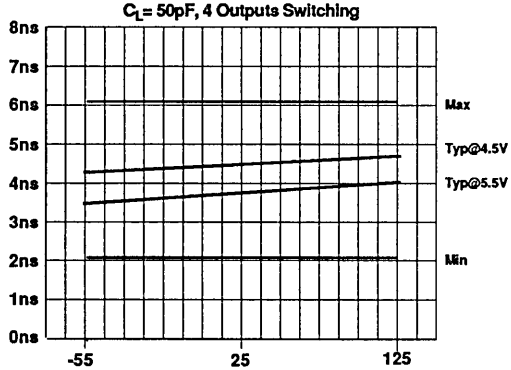
TPZH vs. TEMPERATURE (T_{amb})
C_L= 50pF, 4 Outputs Switching



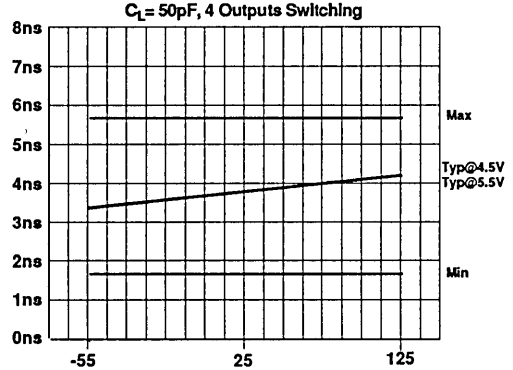
TPHZ vs. TEMPERATURE (T_{amb})
C_L= 50pF, 4 Outputs Switching



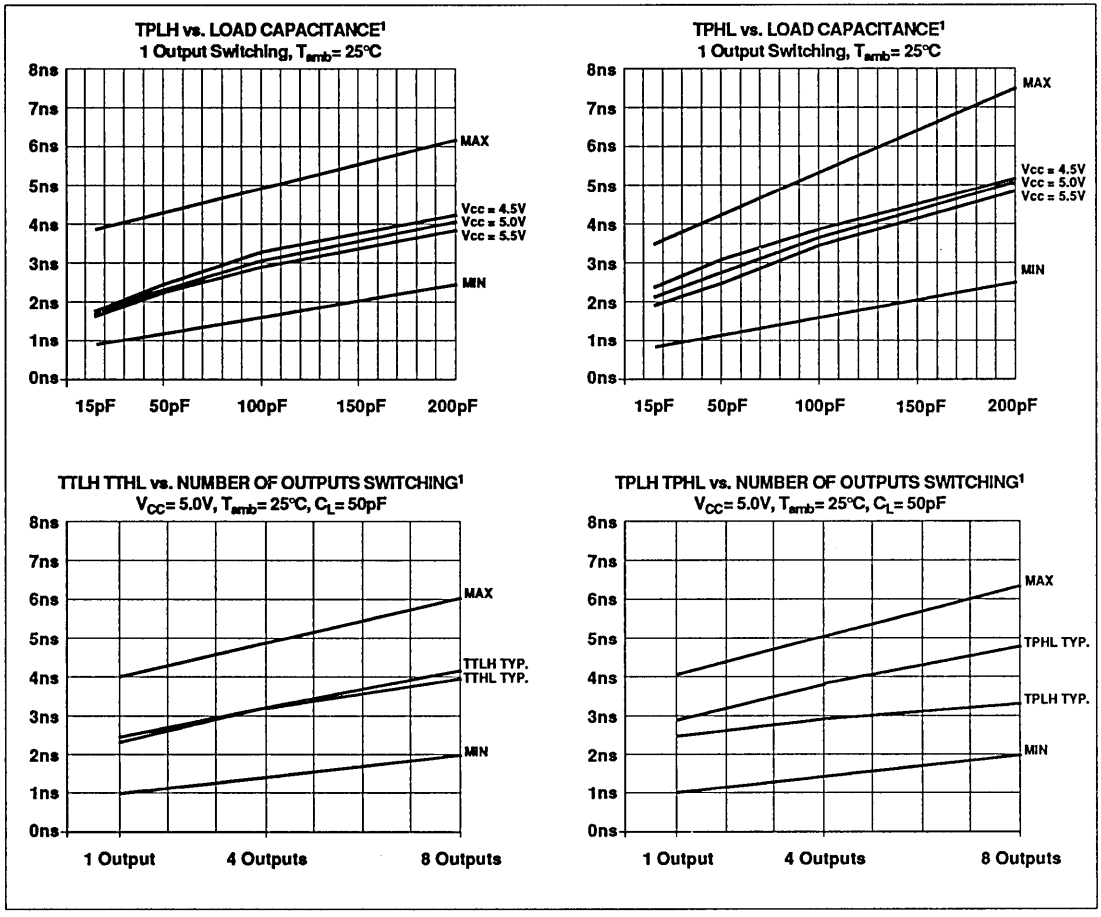
TPZL vs. TEMPERATURE (T_{amb})
C_L= 50pF, 4 Outputs Switching



TPLZ vs. TEMPERATURE (T_{amb})
C_L= 50pF, 4 Outputs Switching

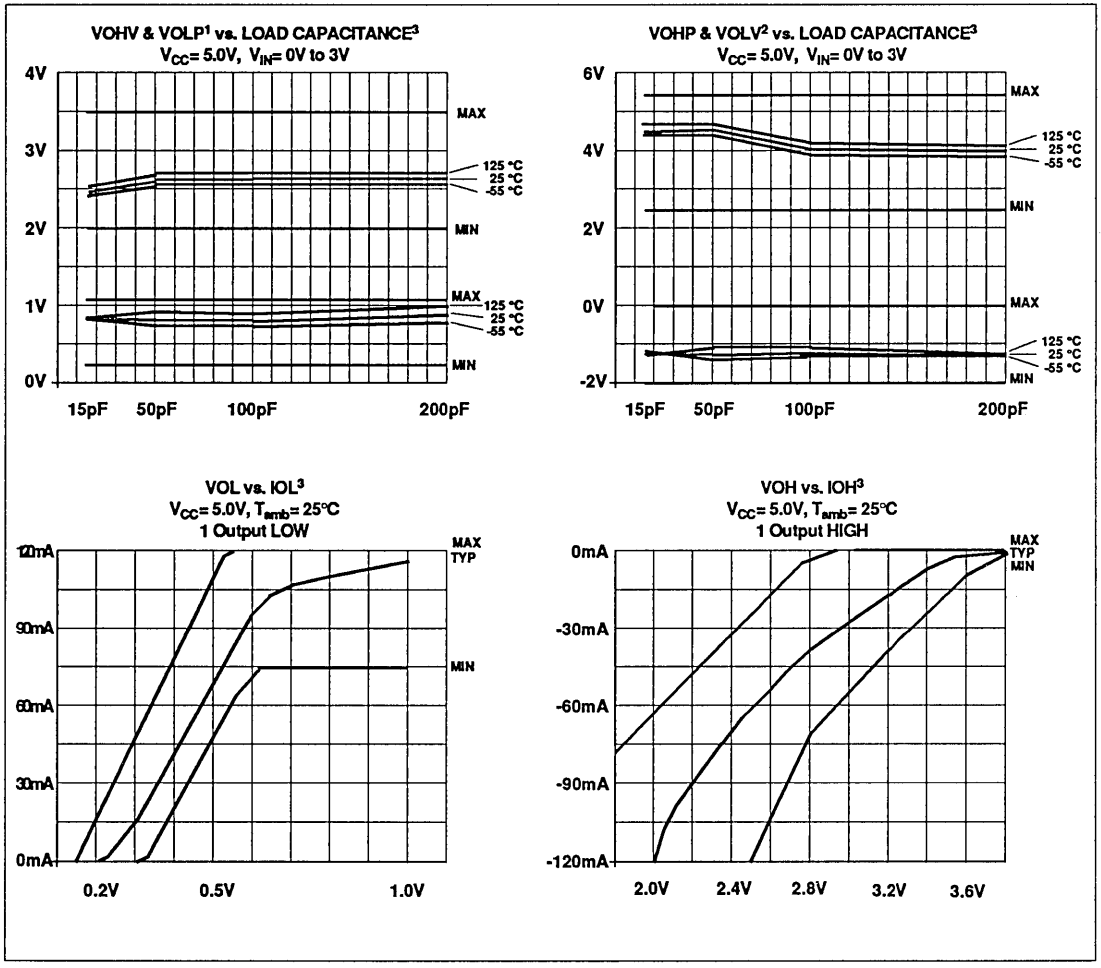


Octal buffer/line driver (3-State) 74ABT244



NOTES:
1. MIN and MAX lines are design characteristics and are not necessarily guaranteed by test.

Octal buffer/line driver (3-State) 74ABT244



NOTES:

1. VOHV is defined as the minimum (valley) voltage induced on a quiescent high-level output during switching of other outputs. VOLP is defined as the maximum (peak) voltage induced on a quiescent low-level output during switching of other outputs.
2. VOHP is defined as the maximum (peak) voltage induced on a quiescent high-level output during switching of other outputs. VOLV is defined as the minimum (valley) voltage induced on a quiescent low-level output during switching of other outputs.
3. MIN and MAX lines are design and process characteristics. They are not necessarily guaranteed by test.

Document No.	
ECN No.	853-1447 00227
Date of Issue	August 20, 1990
Status	Product Specification
Advanced BiCMOS Products	

74ABT245

Octal transceiver with direction pin (3-State)

FEATURES

- Octal bidirectional bus interface
- 3-State buffers
- Output capability: +64 mA/-32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The 74ABT245 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT245 device is an octal transceiver featuring noninverting 3-State bus compatible outputs in both send and receive directions. The control function

(continued)

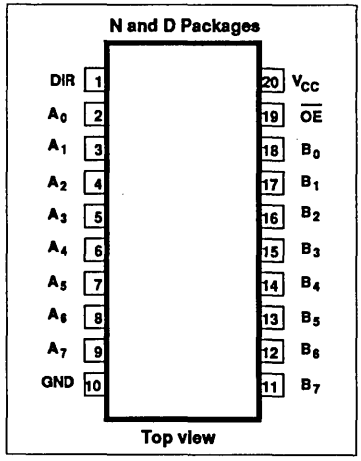
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay A_n to B_n, or B_n to A_n	C_L = 50pF; V_{CC} = 5V	2.9	ns
$C_{DIR, \overline{OE}}$	Input capacitance	V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	I/O pin capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

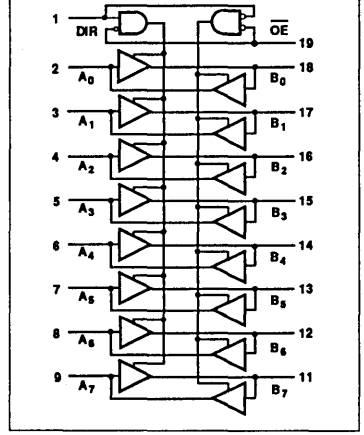
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-Pin Plastic DIP	-40°C to +85°C	74ABT245N
20-Pin Plastic SOL	-40°C to +85°C	74ABT245D

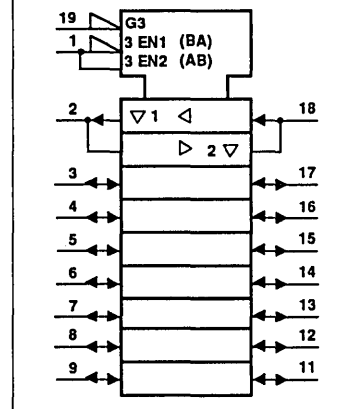
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



implementation minimizes external timing requirements. The device features an Output Enable ($\overline{OE}$) input for easy cascading and a Direction (DIR) input for direction control.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[2]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_O	DC output voltage[2]	output in Off or High state	-0.5 to +5.5	V
I_O	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
$\overline{OE}$	DIR	A_n	B_n
L	L	A = B	Inputs
L	H	Inputs	B = A
H	X	Z	Z

PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	DIR	Direction control input
2, 3, 4, 5 6, 7, 8, 9	A_0 - A_7	Data inputs/outputs (A side)
18, 17, 16, 15 14, 13, 12, 11	B_0 - B_7	Data inputs/outputs (B side)
19	$\overline{OE}$	Ouput enable
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = -18mA			-1.2		-1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5			2.5		V
		V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0			3.0		
		V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
$I_{IH} + I_{OZH}$	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
$I_{IL} + I_{OZL}$	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]	V_{CC} = 5.5V; V_O = 2.5V	-50	-100	-180	-50	-180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		24	30		30	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]	Outputs enabled, one input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA
		Outputs 3-State, one data input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	50		50	µA
		Outputs 3-State, one enable input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

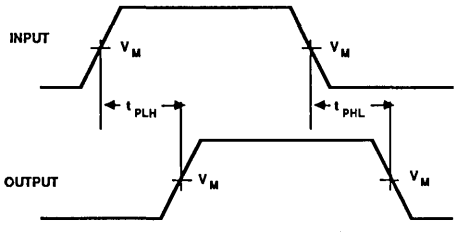
AC CHARACTERISTICS

GND = 0V; $t_R = t_F = 2.5ns$; $C_L = 50pF$, $R_L = 500\Omega$

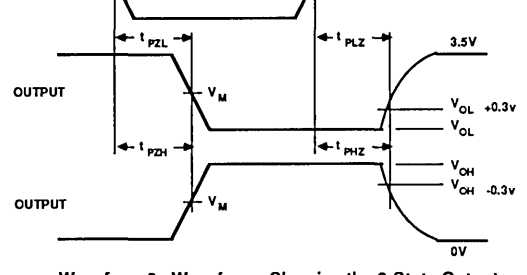
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = -40°C to +85°C, V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n or B_n to A_n	1	1.0 1.0	2.6 2.9	4.1 4.2	1.0 1.0	4.6 4.6	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.3 2.3	3.3 4.3	4.8 5.8	1.3 2.3	5.3 6.3	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	2.7 2.3	4.7 4.3	6.2 5.8	2.7 2.3	7.2 6.3	ns

AC WAVEFORMS

(V_M = 1.5V, V_{IN} = GND to 3.0V)

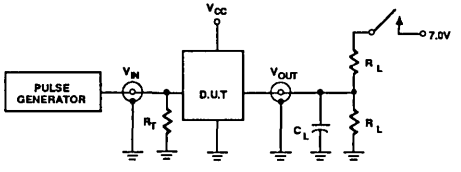


Waveform 1. Waveforms Showing the Input to Output Propagation Delays



Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

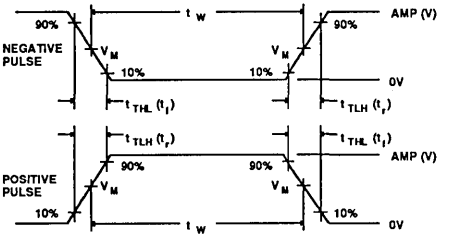
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

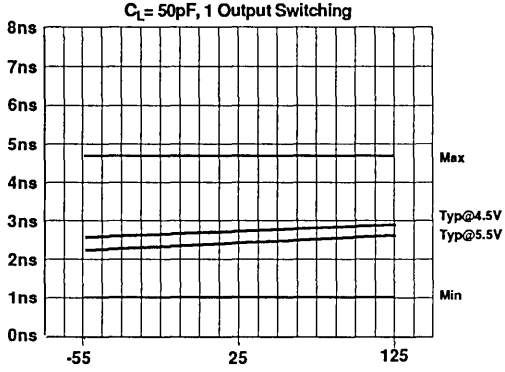


V_M = 1.5V

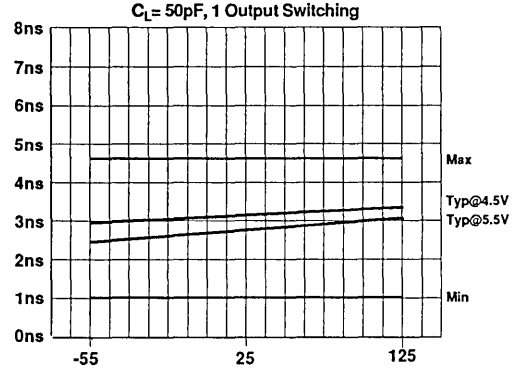
Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

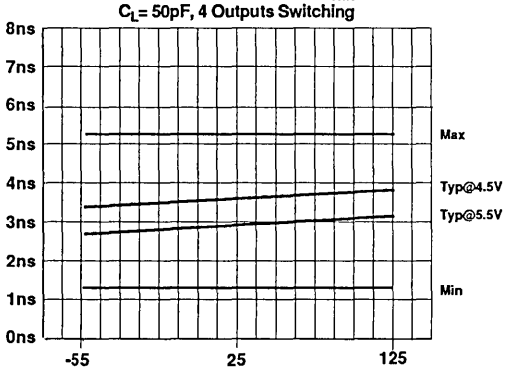
TPLH vs. TEMPERATURE (T_{amb})
C_L= 50pF, 1 Output Switching



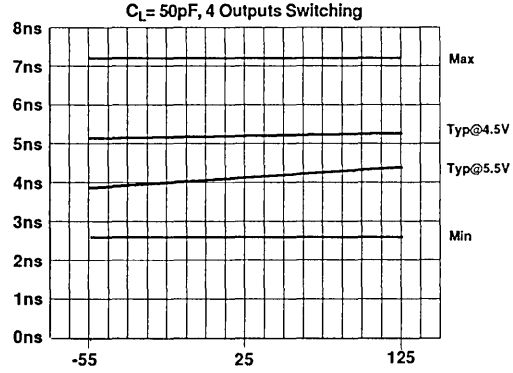
TPHL vs. TEMPERATURE (T_{amb})
C_L= 50pF, 1 Output Switching



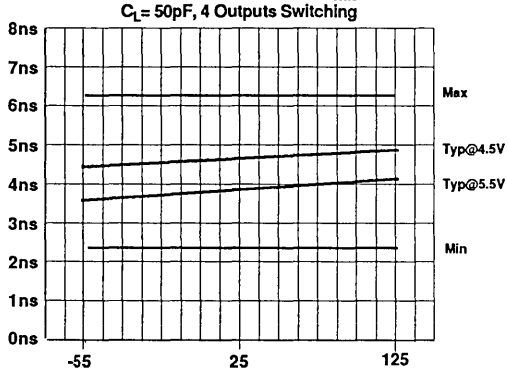
TPZH vs. TEMPERATURE (T_{amb})
C_L= 50pF, 4 Outputs Switching



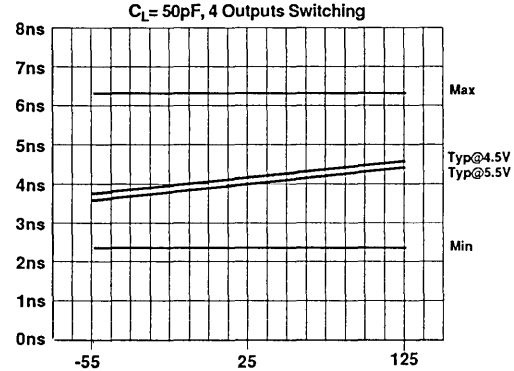
TPHZ vs. TEMPERATURE (T_{amb})
C_L= 50pF, 4 Outputs Switching

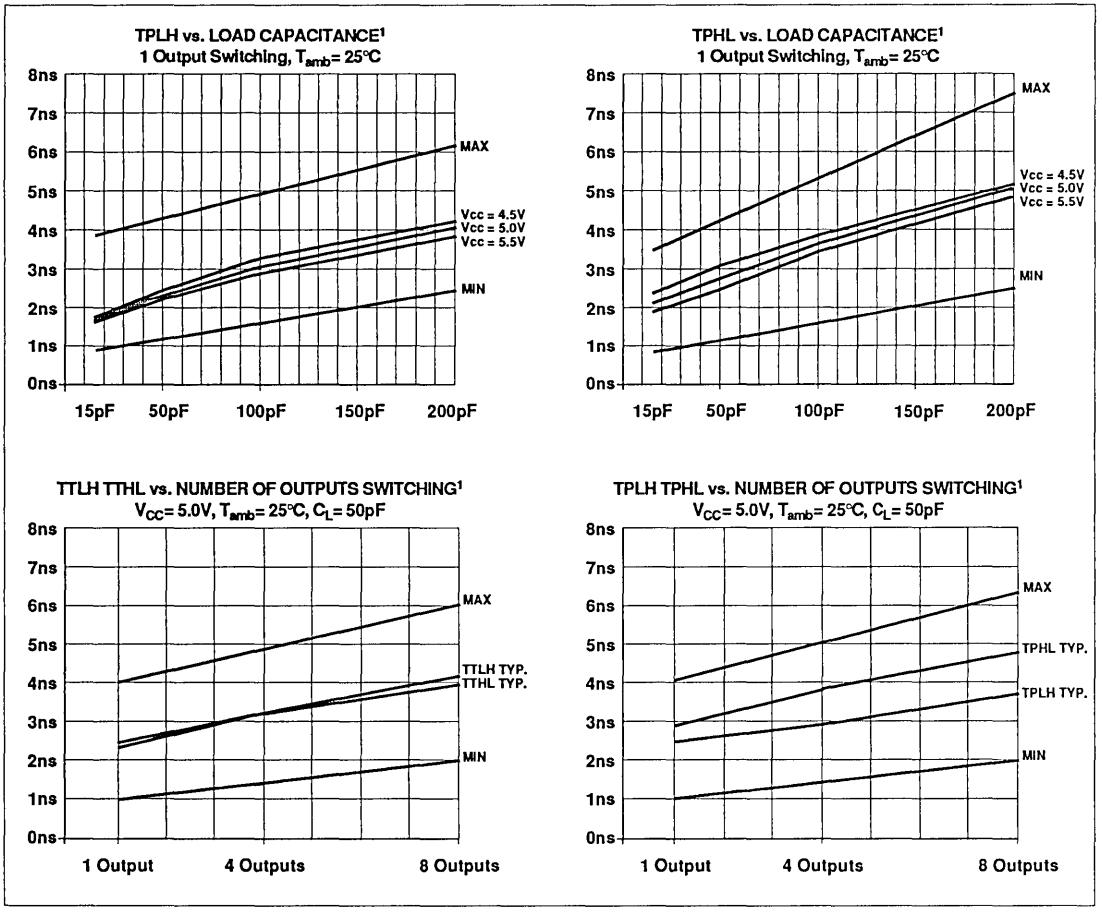


TPZL vs. TEMPERATURE (T_{amb})
C_L= 50pF, 4 Outputs Switching



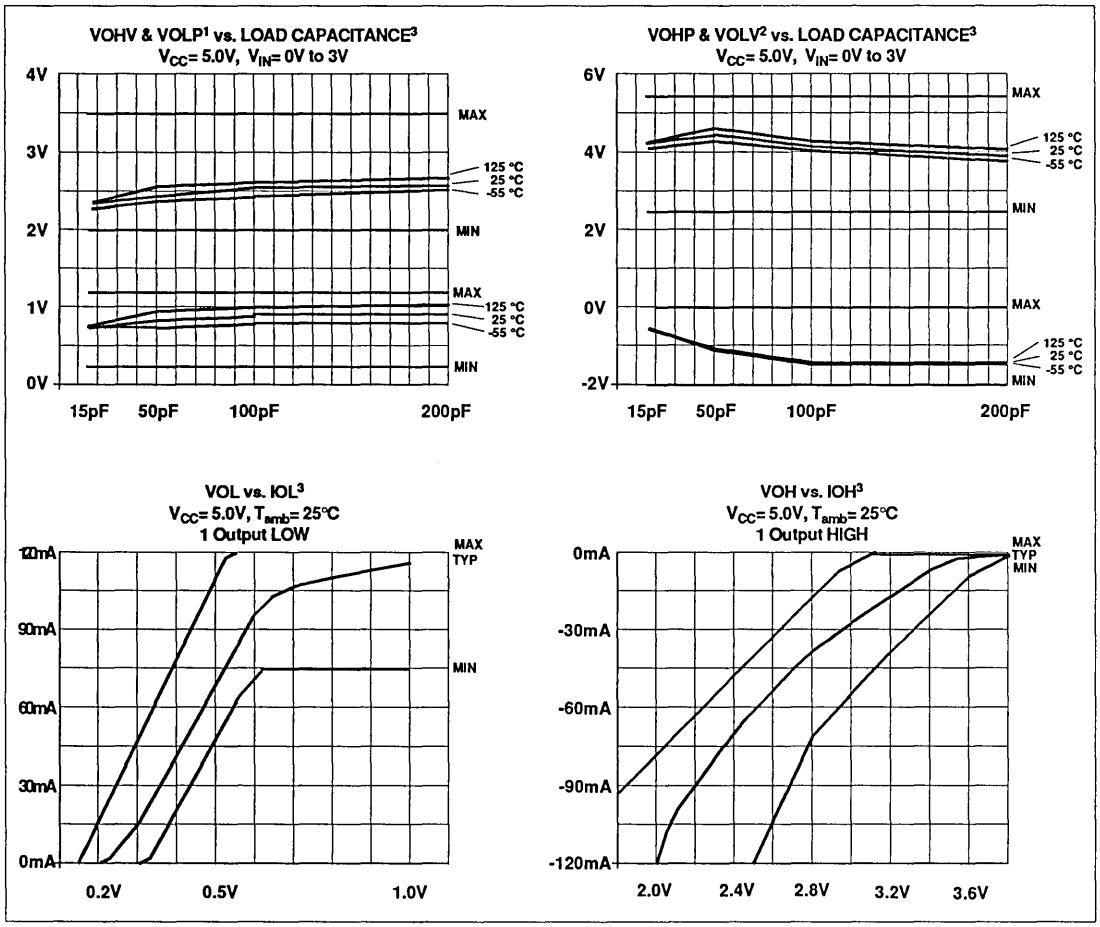
TPLZ vs. TEMPERATURE (T_{amb})
C_L= 50pF, 4 Outputs Switching





NOTES:
1. MIN and MAX lines are design characteristics and are not necessarily guaranteed by test.

Octal transceiver with direction pin (3-State) 74ABT245



NOTES:

1. VOHV is defined as the minimum (valley) voltage induced on a quiescent high-level output during switching of other outputs. VOLP is defined as the maximum (peak) voltage induced on a quiescent low-level output during switching of other outputs.
2. VOHP is defined as the maximum (peak) voltage induced on a quiescent high-level output during switching of other outputs. VOLV is defined as the minimum (valley) voltage induced on a quiescent low-level output during switching of other outputs.
3. MIN and MAX lines are design and process characteristics. They are not necessarily guaranteed by test.

Document No.	
ECN No.	
Date of Issue	August 20, 1990
Status	Preliminary Specification
Advanced BiCMOS Products	

74ABT273
Octal D-type flip-flop

FEATURES

- Eight edge-triggered D-type flip-flops
- Buffered common clock
- Buffered asynchronous Master Reset
- See 74ABT377 for clock enable version
- See 74ABT373 for transparent latch version
- See 74ABT374 for 3-state version

DESCRIPTION

The 74ABT273 has eight edge-triggered D-type flip-flops with individual D inputs and Q outputs. The common buffered Clock (CP) and Master Reset ($\overline{MR}$) inputs load and reset (clear) all flip-flops simultaneously.

The register is fully edge-triggered. The state of each D input, one setup time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output.

All outputs will be forced Low independently of Clock or Data inputs by a Low voltage level on the $\overline{MR}$ input. The device is useful for applications where the true output only is required and the CP and $\overline{MR}$ are common elements.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	C_L = 50pF; V_{CC} = 5V	5.4	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

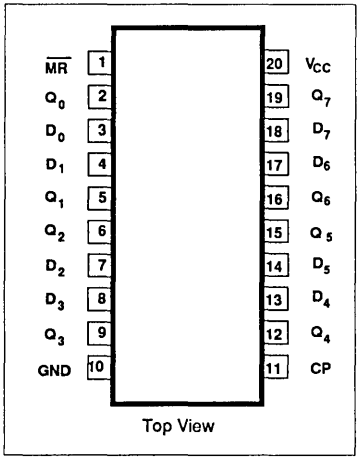
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP	-40°C to +85°C	74ABT273N
20-pin plastic SOL	-40°C to +85°C	74ABT273D

PIN DESCRIPTION

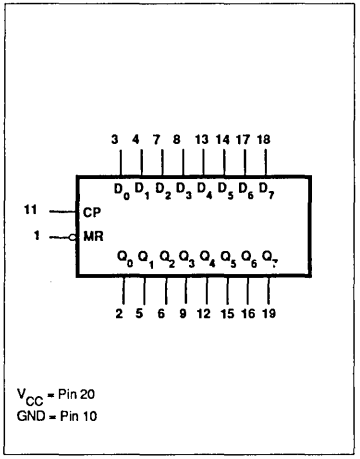
PIN NUMBER	SYMBOL	NAME AND FUNCTION
11	CP	Clock Pulse input (active rising edge)
3, 4, 7, 8 13, 14, 17, 18	D_0 - D_7	Data inputs
2, 5, 6, 9 12, 15, 16, 19	Q_0 - Q_7	Data outputs
1	$\overline{MR}$	Master Reset input (active-Low)
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

PIN CONFIGURATION



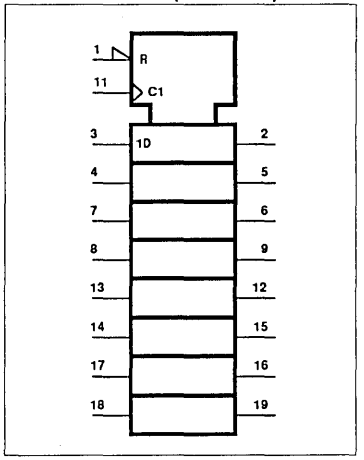
Top View

LOGIC SYMBOL



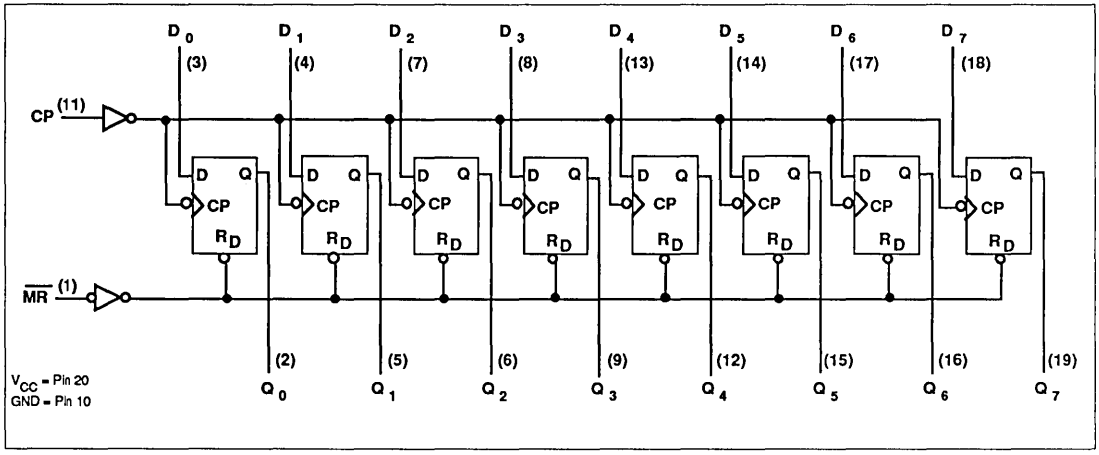
V_{CC} = Pin 20
GND = Pin 10

LOGIC SYMBOL(IEEE/IEC)



Octol D Flip-Flop 74ABT273

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUTS	OPERATING MODE
$\overline{MR}$	CP	D_n	Q_0 - Q_7	
L	X	X	L	Reset (clear)
H	↑	h	H	Load "1"
H	↑	l	L	Load "0"

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[2]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_O	DC output voltage[2]	output in Off or High state	-0.5 to +5.5	V
I_O	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

Octol D Flip-Flop | 74ABT273

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = -18mA			-1.2		-1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5			2.5		V
		V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0			3.0		
		V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_O	Short-circuit output current[1]	V_{CC} = 5.5V; V_O = 2.5V	-50	-100	-180	-50	-180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		24	30		30	mA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5V; One input at 3.4V, other inputs at V_{CC} or GND		0.5	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

AC CHARACTERISTICS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω

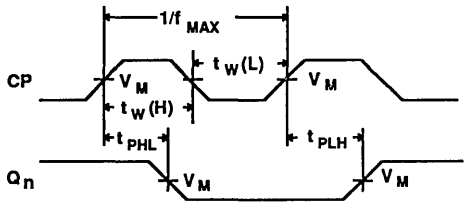
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = -40° C to +85°C, V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	150	200		150		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	Waveform 1	2.2 3.1	4.2 5.1	5.7 6.6	2.2 3.1	6.2 7.1	ns
t_{PHL}	Propagation delay MR to Q_n	Waveform 2	2.4	4.4	6.2	2.4	6.7	ns

AC SETUP REQUIREMENTS

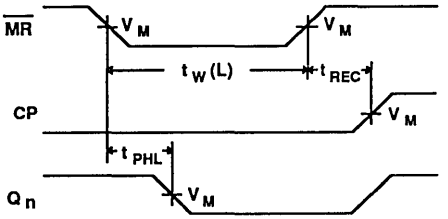
GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = -40° C to +85°C, V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to CP	Waveform 3	1.0 1.5			1.0 1.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to CP	Waveform 3	1.0 1.0			1.0 1.0		ns
$t_w(H)$ $t_w(L)$	Clock Pulse width High or Low	Waveform 1	3.3 3.3			3.3 3.3		ns
$t_w(L)$	Master Reset Pulse width, Low	Waveform 2	3.5			3.5		ns
t_{REC}	Recovery time $\overline{MR}$ to CP	Waveform 2	7.5			8.0		ns

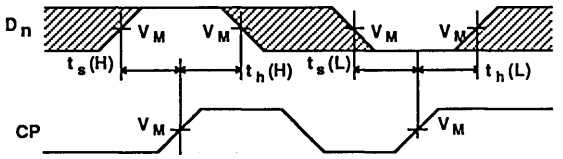
AC WAVEFORMS



Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time

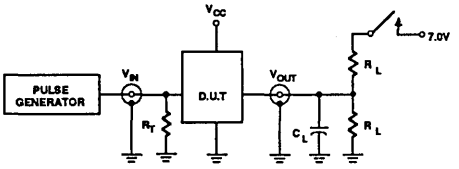


Waveform 3. Data Setup And Hold Times

NOTE: For all waveforms, V_M = 1.5V.

The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

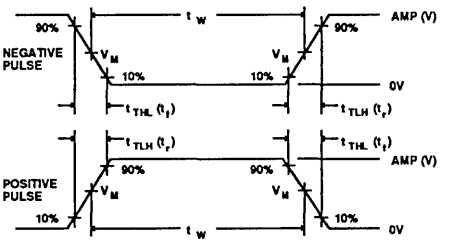
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

Document No.	
ECN No.	853-1454 00227
Date of Issue	August 20, 1990
Status	Product Specification
Advanced BiCMOS Products	

74ABT373

Octal D-type transparent latch (3-State)

FEATURES

- 8-bit Transparent Latch
- 3-State Output Buffers
- Output capability:+64mA/-32mA
- Latch-up protection exceeds 500mA per JEDEC JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The 74ABT373 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT373 device is an octal transparent latch coupled to eight 3-state output buffers. The two sections of the device are controlled independently by Enable (E) and Output Enable ($\overline{OE}$) control gates.

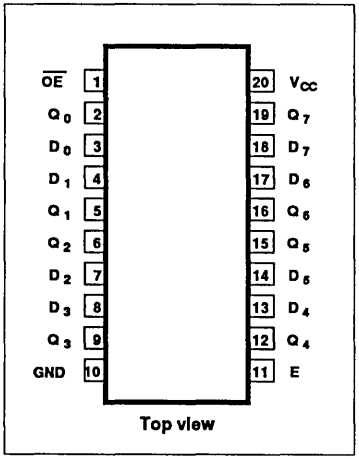
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	C_L = 50pF; V_{CC} = 5V	4.0	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

ORDERING INFORMATION

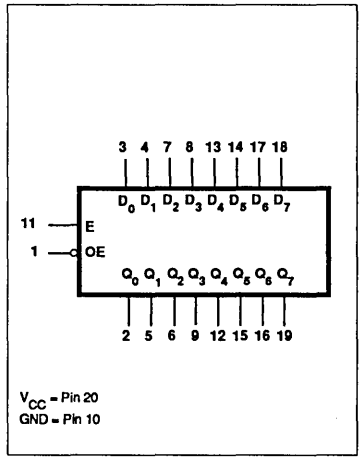
PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP	-40°C to +85°C	74ABT373N
20-pin plastic SOL	-40°C to +85°C	74ABT373D

PIN CONFIGURATION



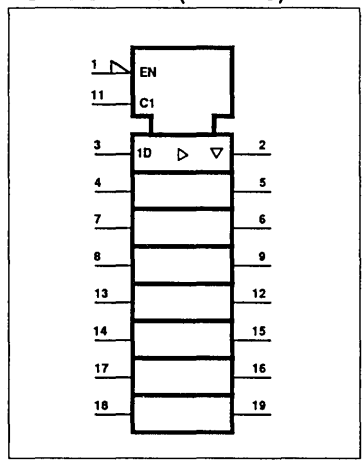
Top view

LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

LOGIC SYMBOL(IEEE/IEC)



Octal D-type transparent latch (3-State) 74ABT373

The data on the D inputs are transferred to the latch outputs when the Latch Enable (E) input is High. The latch remains transparent to the data inputs while E is High, and stores the data that is present one setup time before the High-to-Low enable transition.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active-Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation.

When $\overline{OE}$ is Low, the latched or transparent data appears at the outputs. When $\overline{OE}$ is High, the outputs are in the High-impedance "OFF" state, which means they will neither drive nor load the bus.

PIN DESCRIPTION

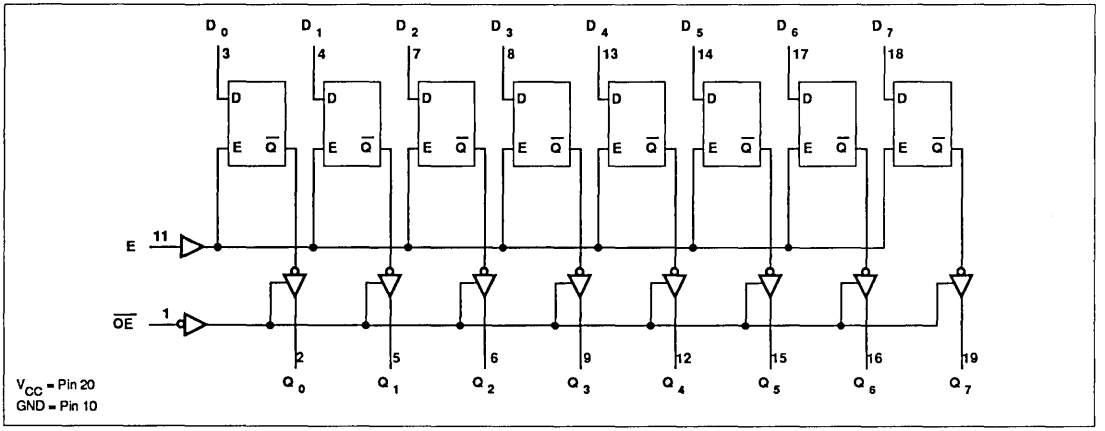
PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	Output enable input (active Low)
3, 4, 7 8, 13 14, 17, 18	D_0 - D_7	Data inputs
2, 5, 6, 9, 12 15,16,19	Q_0 - Q_7	3-State Outputs
11	E	Enable input (active High)
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

FUNCTION TABLE, 74ALS373

INPUTS			INTERNAL	OUTPUTS	OPERATING MODE
$\overline{OE}$	E	D_n	REGISTER	Q_0 - Q_7	
L L	H H	L H	L H	L H	Enable and read register
L L	↓ ↓	l h	L H	L H	Latch and read register
L	L	X	NC	NC	Hold
H H	L H	X D_n	NC D_n	Z Z	Disable outputs

H = High voltage level
h = High voltage level one set-up time prior to the High-to-Low E transition
L = Low voltage level
l = Low voltage level one set-up time prior to the High-to-Low E transition
NC = No change
X = Don't care
Z = High impedance "off" state
↓ = High-to-Low E transition

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[2]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_O	DC output voltage[2]	output in Off or High state	-0.5 to +5.5	V
I_O	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

Octal D-type transparent latch (3-State) 74ABT373

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = -18mA			-1.2		-1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5			2.5		V
		V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0			3.0		
		V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]	V_{CC} = 5.5V; V_O = 2.5V	-50	-100	-180	-50	-180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		24	30		30	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5V; One input at 3.4V, other inputs at V_{CC} or GND		0.5	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

AC CHARACTERISTICS

GND = 0V; $t_R = t_F = 2.5ns$; $C_L = 50pF$, $R_L = 500\Omega$

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = -40°C to +85°C, V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	Waveform 2	1.9 2.2	3.9 4.2	5.4 5.7	1.9 2.2	5.9 6.2	ns
t_{PLH} t_{PHL}	Propagation delay E to Q_n	Waveform 1	2.6 3.2	4.6 5.2	6.1 6.7	2.6 3.2	6.6 7.2	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	Waveform 4 Waveform 5	1.2 2.7	3.2 4.7	4.7 6.2	1.2 2.7	5.2 6.7	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	Waveform 4 Waveform 5	2.5 2.0	4.9 4.5	6.4 6.0	2.5 2.0	6.9 6.5	ns

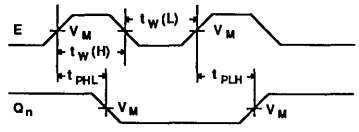
AC SETUP REQUIREMENTS

GND = 0V; $t_R = t_F = 2.5ns$; $C_L = 50pF$, $R_L = 500\Omega$

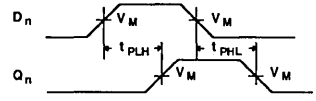
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = -40°C to +85°C, V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time D_n to E	Waveform 3	1.9 1.5			1.9 1.5		ns
$t_h(H)$ $t_h(L)$	Hold time D_n to E	Waveform 3	1.0 1.0			1.0 1.0		ns
$t_w(H)$	E pulse width, High or Low	Waveform 1	3.3			3.3		ns

AC WAVEFORMS

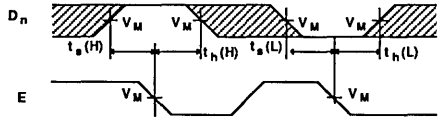
(V_M = 1.5V, V_{IN} = GND to 3.0V)



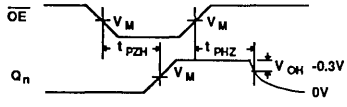
Waveform 1. Propagation Delay, Enable to Output, and Enable Pulse Width.



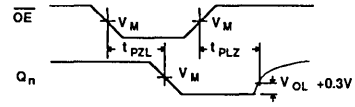
Waveform 2. Propagation Delay for Data to Outputs.



Waveform 3. Data Setup and Hold Times.



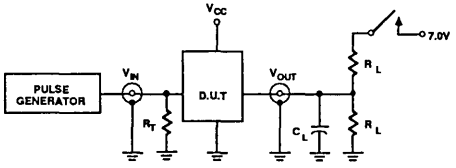
Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time From High Level.



Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level.

Octal D-type transparent latch (3-State) 74ABT373

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

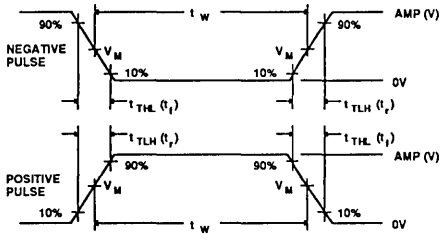
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



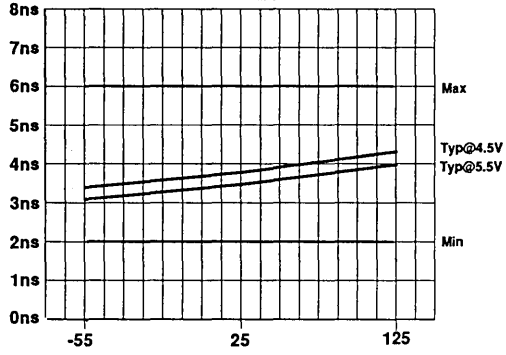
V_M = 1.5V

Input Pulse Definition

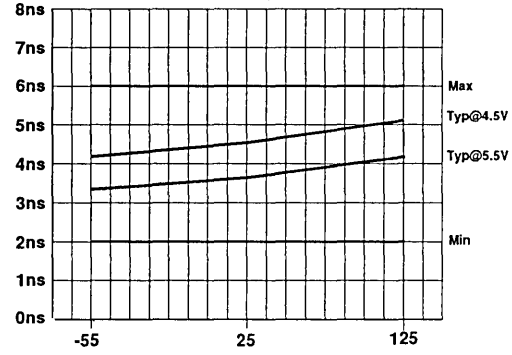
FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

Octal D-type transparent latch (3-State) 74ABT373

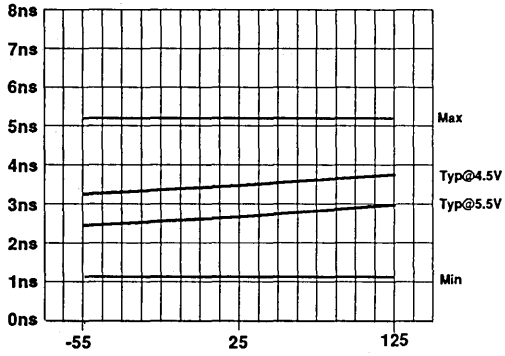
TPLH vs. TEMPERATURE (T_{amb})
C_L= 50pF, 1 Output Switching
Dn to Qn



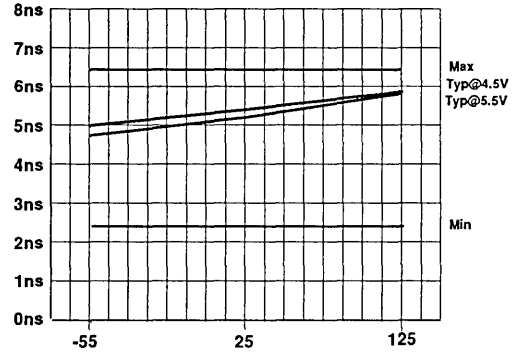
TPHL vs. TEMPERATURE (T_{amb})
C_L= 50pF, 1 Output Switching
Dn to Qn



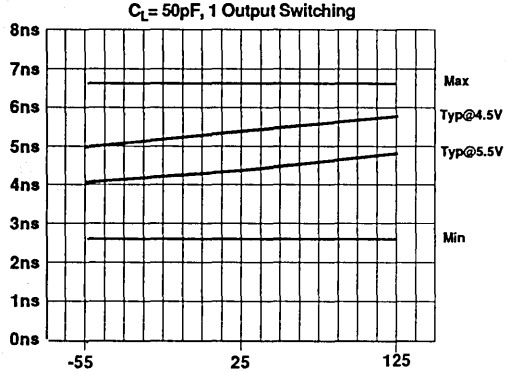
TPZH vs. TEMPERATURE (T_{amb})
C_L= 50pF, 1 Output Switching



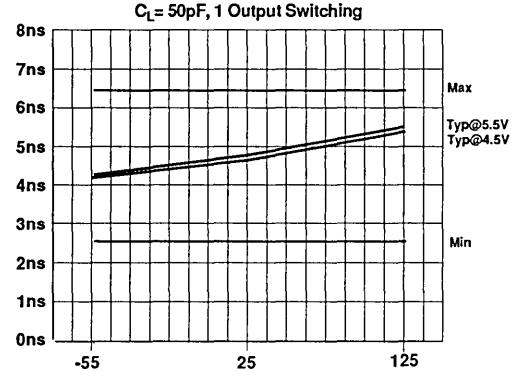
TPHZ vs. TEMPERATURE (T_{amb})
C_L= 50pF, 1 Output Switching



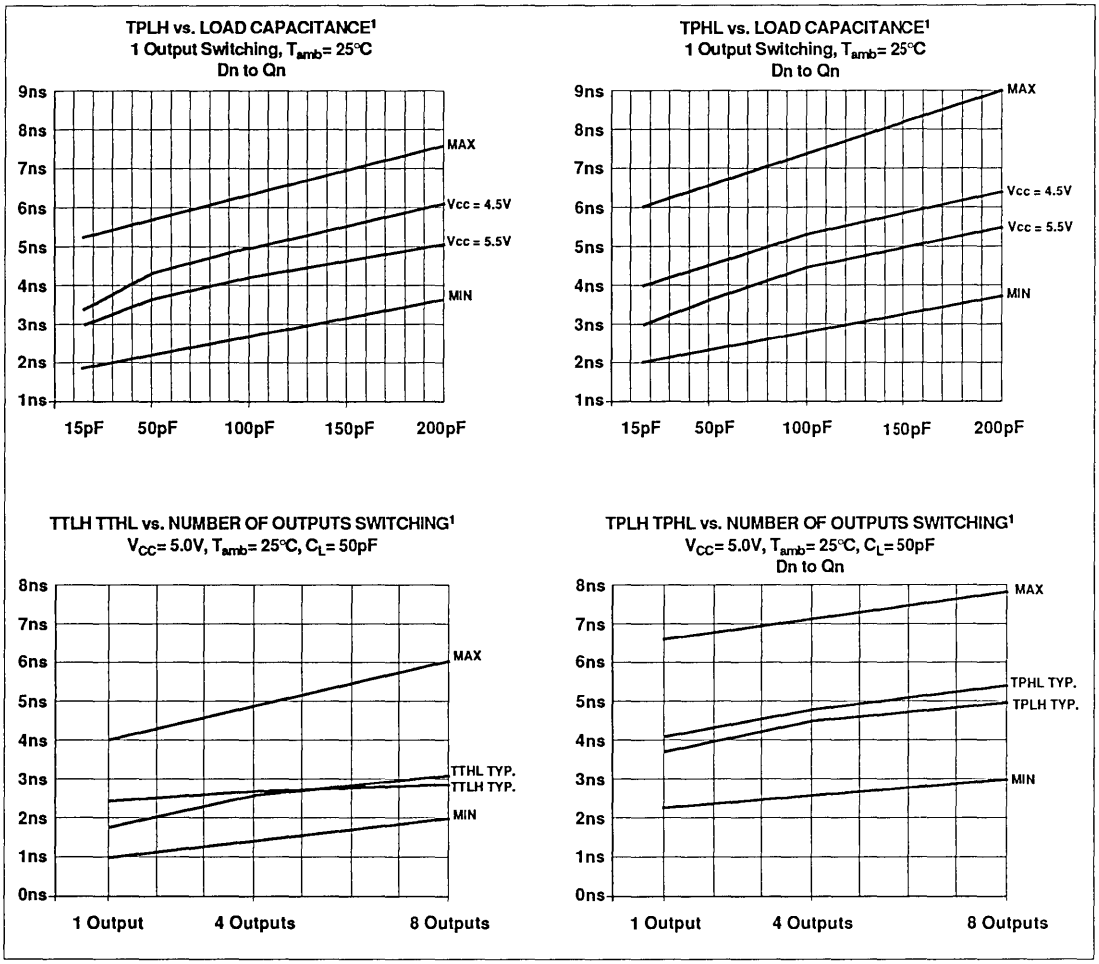
TPZL vs. TEMPERATURE (T_{amb})
C_L= 50pF, 1 Output Switching



TPLZ vs. TEMPERATURE (T_{amb})
C_L= 50pF, 1 Output Switching

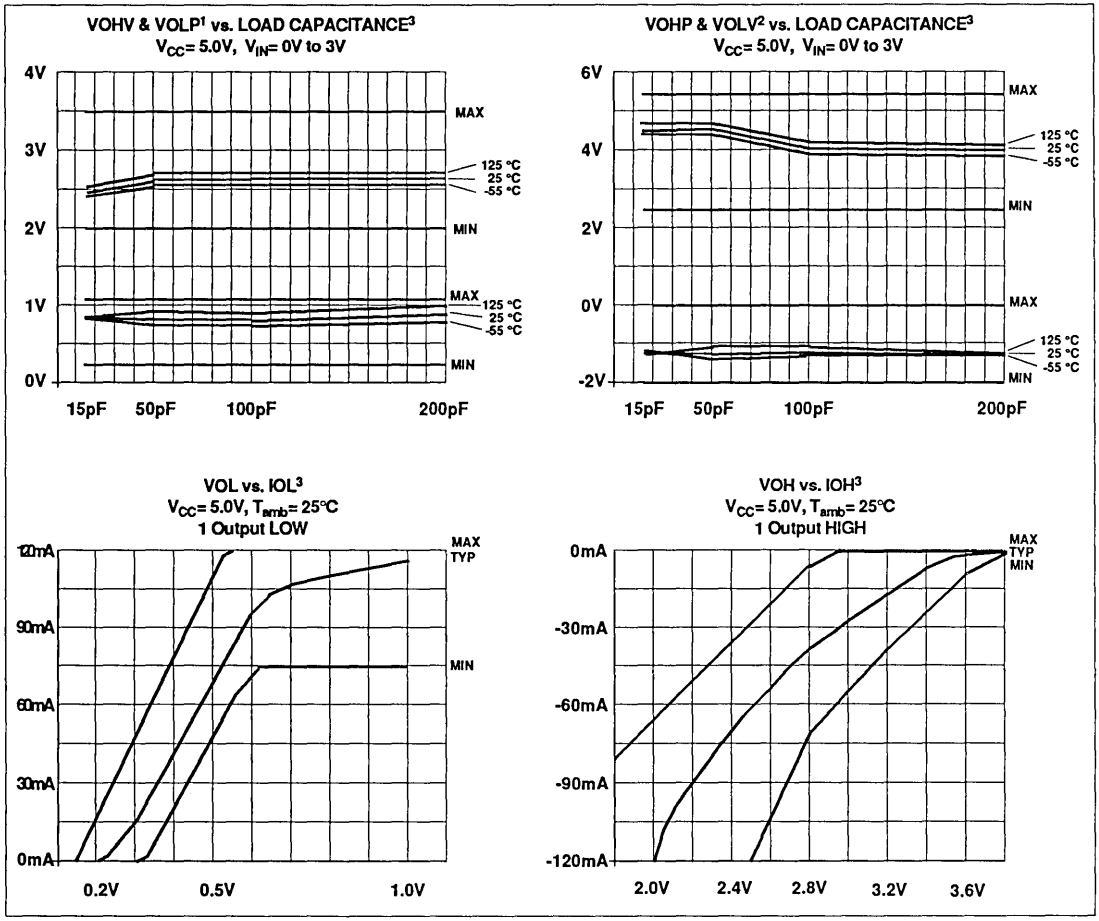


Octal D-type transparent latch (3-State) 74ABT373



NOTES:
1. MIN and MAX lines are design characteristics and are not necessarily guaranteed by test.

Octal D-type transparent latch (3-State) 74ABT373



NOTES:

1. VOHV is defined as the minimum (valley) voltage induced on a quiescent high-level output during switching of other outputs. VOLP is defined as the maximum (peak) voltage induced on a quiescent low-level output during switching of other outputs.
2. VOHP is defined as the maximum (peak) voltage induced on a quiescent high-level output during switching of other outputs. VOLV is defined as the minimum (valley) voltage induced on a quiescent low-level output during switching of other outputs.
3. MIN and MAX lines are design and process characteristics. They are not necessarily guaranteed by test.

Document No.	
ECN No.	853-1448 00227
Date of Issue	August 20, 1990
Status	Product Specification
Advanced BiCMOS Products	

74ABT374

Octal D-type flip-flop; positive-edge trigger (3-State)

FEATURES

- 8-bit positive edge triggered register
- 3-State output buffers
- Output capability: +64 mA/-32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The 74ABT374 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT374 is an 8-bit, edge triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the clock (CP) and Output Enable ($\overline{OE}$) control gates.

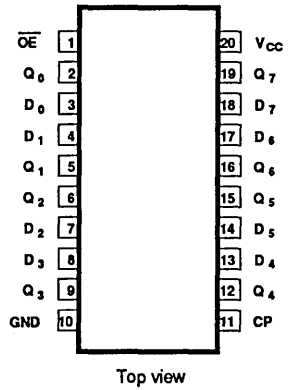
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	C_L = 50pF; V_{CC} = 5V	5.1	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

ORDERING INFORMATION

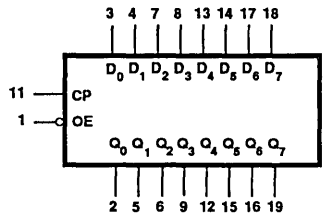
PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-Pin Plastic DIP	-40°C to +85°C	74ABT374N
20-Pin Plastic SOL	-40°C to +85°C	74ABT374D

PIN CONFIGURATION



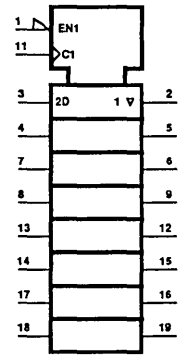
Top view

LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

LOGIC SYMBOL(IEEE/IEC)



Octal D-type flip-flop; positive-edge trigger (3-State) 74ABT374

The register is fully edge triggered. The state of each D input, one set-up time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active-Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the clock operation.

When $\overline{OE}$ is Low, the stored data appears at the outputs. When $\overline{OE}$ is High, the outputs are in the High-impedance "OFF" state, which means they will neither drive nor load the bus.

PIN DESCRIPTION

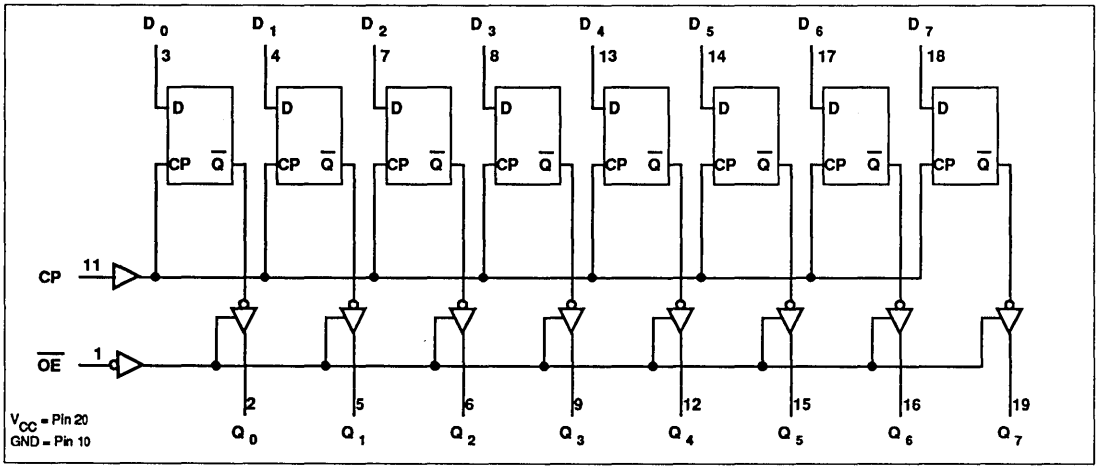
PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{OE}$	Output Enable input (active Low)
3, 4, 7, 8, 13 14, 17, 18	D_0 - D_7	Data inputs
2, 5, 6, 9, 12 15, 16, 19	Q_0 - Q_7	Data outputs
11	CP	Clock Pulse input (active rising edge)
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS			INTERNAL	OUTPUTS	OPERATING MODE
$\overline{OE}$	CP	D_n	REGISTER	Q_0 - Q_7	
L L	↑ ↑	l h	L H	L H	Load and read register
L	‡	X	NC	NC	Hold
H H	‡ ↑	X D_n	NC D_n	Z Z	Disable outputs

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
NC = No change
X = Don't care
Z = High impedance "off" state
↑ = Low-to-High clock transition
‡ = Not a Low-to-High clock transition

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[2]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_O	DC output voltage[2]	output in Off or High state	-0.5 to +5.5	V
I_O	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

Octal D-type flip-flop; positive-edge trigger (3-State) 74ABT374

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = -18mA			-1.2		-1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5			2.5		V
		V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0			3.0		
		V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]	V_{CC} = 5.5V; V_O = 2.5V	-50	-100	-180	-50	-180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		24	30		30	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5V; One input at 3.4V, other inputs at V_{CC} or GND		0.5	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

AC CHARACTERISTICS

GND = 0V; $t_R = t_F = 2.5ns$; $C_L = 50pF$, $R_L = 500\Omega$

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = -40°C to +85°C, V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum Clock frequency	Waveform 1	150	200		150		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	Waveform 1	2.2 3.1	4.2 5.1	5.7 6.6	2.2 3.1	6.2 7.1	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	Waveform 3 Waveform 4	1.2 2.7	3.2 4.7	4.7 6.2	1.2 2.7	5.2 6.7	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	Waveform 3 Waveform 4	2.5 2.0	4.5 4.5	6.0 6.0	2.5 2.0	6.5 6.5	ns

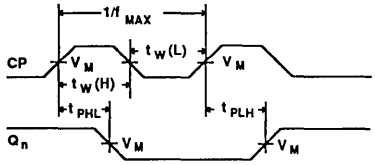
AC SETUP REQUIREMENTS

GND = 0V; $t_R = t_F = 2.5ns$; $C_L = 50pF$, $R_L = 500\Omega$

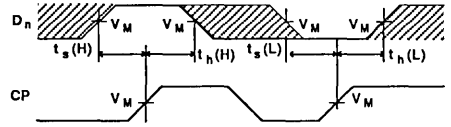
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = -40°C to +85°C, V_{CC} = +5.0V ± 0.5V		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time D_n to CP	Waveform 2	1.0 1.5			1.0 1.5		ns
$t_h(H)$ $t_h(L)$	Hold time D_n to CP	Waveform 2	1.0 1.0			1.0 1.0		ns
$t_w(H)$	CP pulse width, High or Low	Waveform 1	3.3			3.3		ns

AC WAVEFORMS

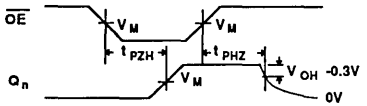
(V_M = 1.5V, V_{IN} = GND to 3.0V)



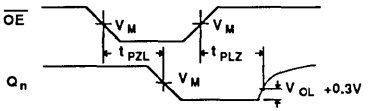
Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 2. Data Setup And Hold Times



Waveform 3. 3-State Output Enable Time To High Level And Output Disable Time From High Level



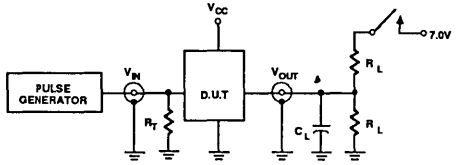
Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V

The shaded areas indicate when the input is permitted to change for predictable output performance.

Octal D-type flip-flop; positive-edge trigger (3-State) 74ABT374

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

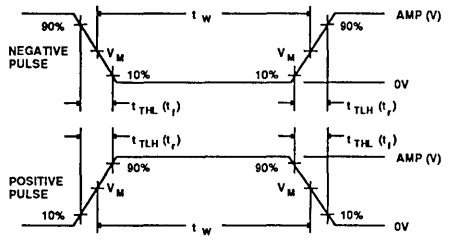
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

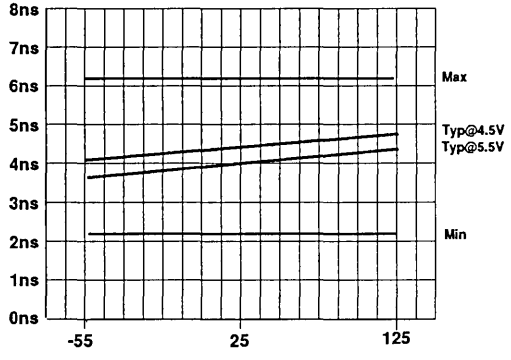


V_M = 1.5V

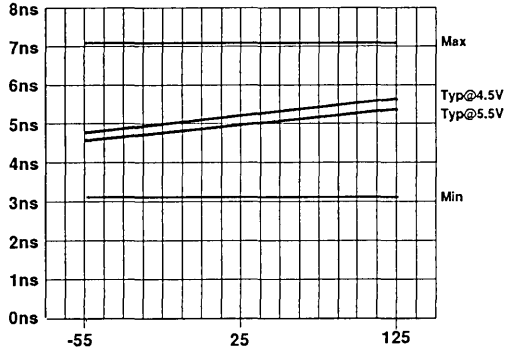
Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

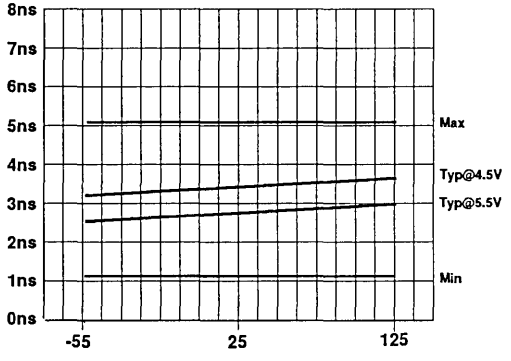
TPLH vs. TEMPERATURE (T_{amb})
C_L= 50pF, 1 Output Switching



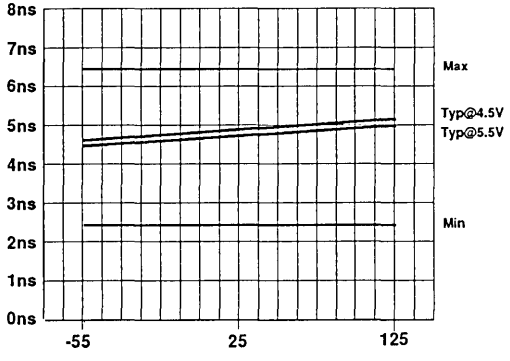
TPHL vs. TEMPERATURE (T_{amb})
C_L= 50pF, 1 Output Switching



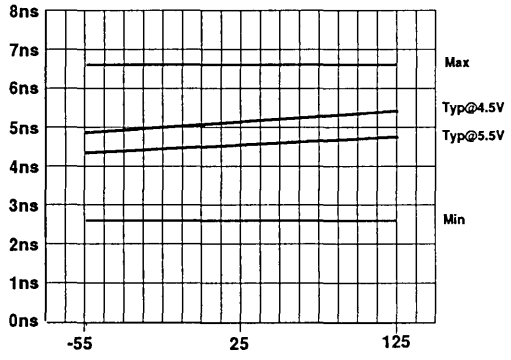
TPZH vs. TEMPERATURE (T_{amb})
C_L= 50pF, 4 Outputs Switching



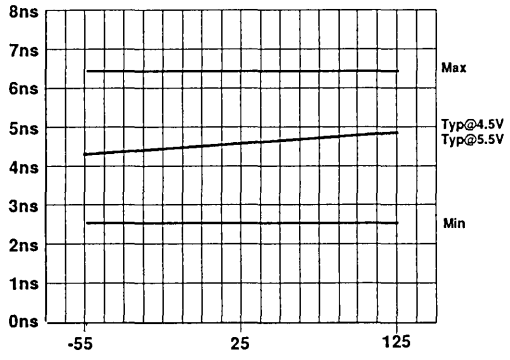
TPHZ vs. TEMPERATURE (T_{amb})
C_L= 50pF, 4 Outputs Switching



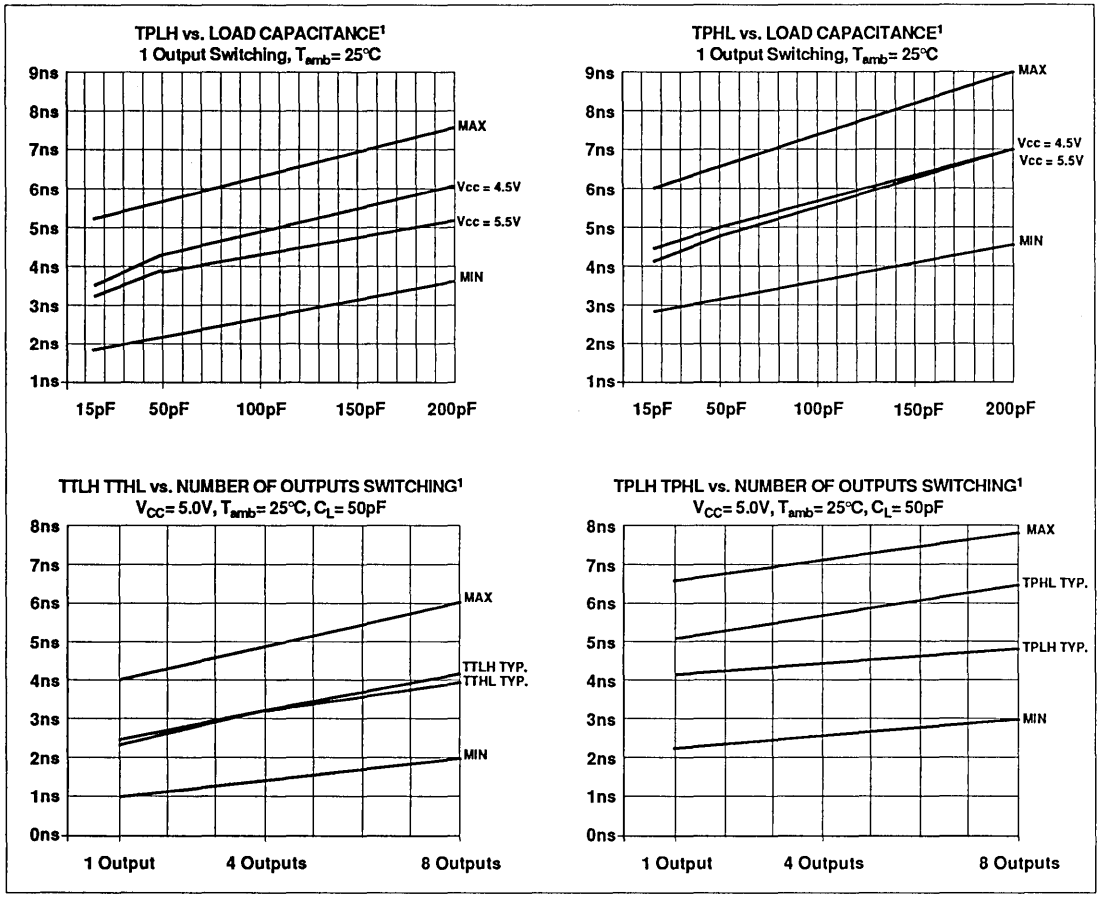
TPZL vs. TEMPERATURE (T_{amb})
C_L= 50pF, 4 Outputs Switching



TPLZ vs. TEMPERATURE (T_{amb})
C_L= 50pF, 4 Outputs Switching

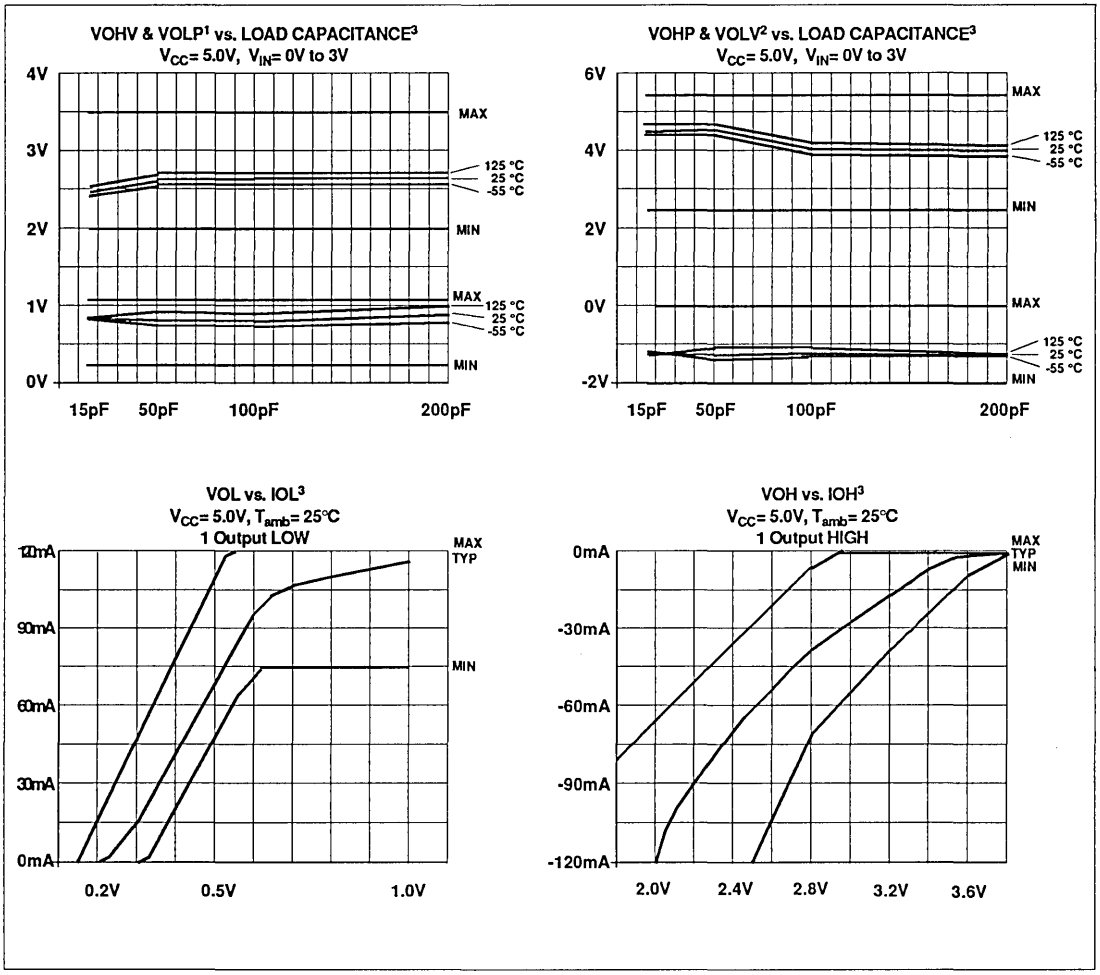


Octal D-type flip-flop; positive-edge trigger (3-State) 74ABT374



NOTES:
1. MIN and MAX lines are design characteristics and are not necessarily guaranteed by test.

Octal D-type flip-flop; positive-edge trigger (3-State) 74ABT374



NOTES:

1. VOHV is defined as the minimum (valley) voltage induced on a quiescent high-level output during switching of other outputs. VOLP is defined as the maximum (peak) voltage induced on a quiescent low-level output during switching of other outputs.
2. VOHP is defined as the maximum (peak) voltage induced on a quiescent high-level output during switching of other outputs. VOLV is defined as the minimum (valley) voltage induced on a quiescent low-level output during switching of other outputs.
3. MIN and MAX lines are design and process characteristics. They are not necessarily guaranteed by test.

Philips Components—Signetics

Document No.	
ECN No.	
Date of Issue	August 20, 1990
Status	Preliminary Specification
Advanced BiCMOS Products	

74ABT377

Octal D-type flip-flop with enable

FEATURES

- Ideal for addressable register applications
- 8-bit positive edge triggered register
- Enable for address and data synchronization applications
- Output capability: +64 mA/-32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The 74ABT377 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT377 has 8 edge-triggered D-type flip-flops with individual D inputs

(continued)

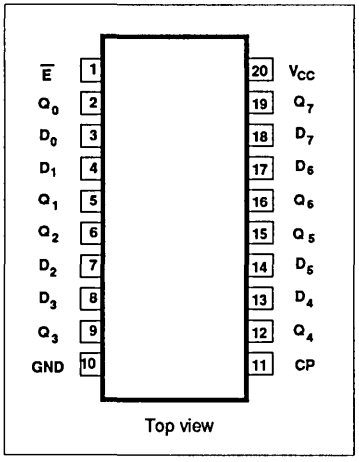
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	C_L = 50pF; V_{CC} = 5V	5.1	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

ORDERING INFORMATION

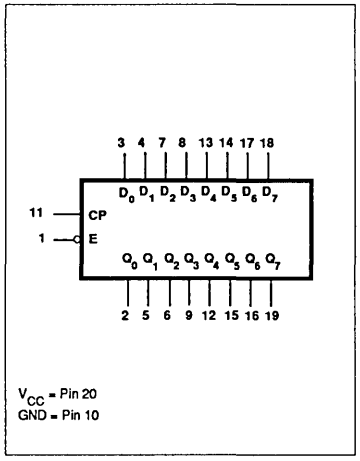
PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-Pin Plastic DIP	-40°C to +85°C	74ABT377N
20-Pin Plastic SOL	-40°C to +85°C	74ABT377D

PIN CONFIGURATION



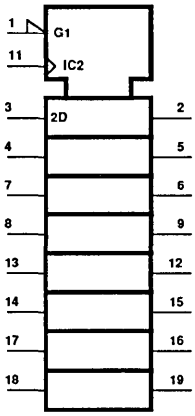
Top view

LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

LOGIC SYMBOL(IEEE/IEC)



and Q outputs. The common buffered clock (CP) input loads all flip-flops simultaneously when the Enable ($\overline{E}$) input is Low.

The register is fully edge triggered. The state of each D input, one set-up time before the Low-to-High clock transition, is transferred to the corresponding flip-flop's Q output.

The $\overline{E}$ input must be stable one setup time prior to the Low-to-High clock transition for predictable operation.

PIN DESCRIPTION

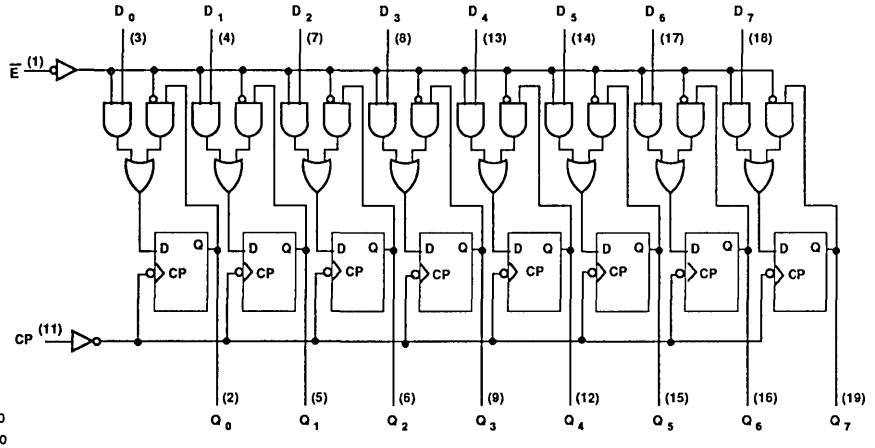
PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{E}$	Enable input (active Low)
3, 4, 7, 8, 13 14, 17, 18	D_0 - D_7	Data inputs
2, 5, 6, 9, 12 15, 16, 19	Q_0 - Q_7	Data outputs
11	CP	Clock Pulse input (active rising edge)
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS			OUTPUTS	OPERATING MODE
$\overline{E}$	CP	D_n	Q_n	
l	↑	h	H	Load "1"
l	↑	l	L	Load "0"
h H	↑ X	X X	no change no change	Hold (do nothing)

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition

LOGIC DIAGRAM



Octal D-type flip-flop with enable 74ABT377

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[2]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_O	DC output voltage[2]	output in Off or High state	-0.5 to +5.5	V
I_O	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

Octal D-type flip-flop with enable 74ABT377

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = -18mA			-1.2		-1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5			2.5		V
		V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0			3.0		
		V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]	V_{CC} = 5.5V; V_O = 2.5V	-50	-100	-180	-50	-180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		24	30		30	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5V; One input at 3.4V, other inputs at V_{CC} or GND		0.5	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

AC CHARACTERISTICS

GND = 0V; $t_R = t_F = 2.5ns$; $C_L = 50pF$, $R_L = 500\Omega$

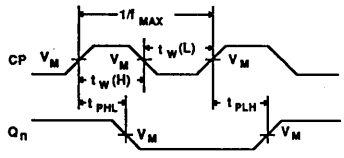
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = -40°C to +85°C, V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	150	200				MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	Waveform 1	2.5 3.7	4.5 5.3	6.0 6.8	2.5 3.3	6.5 7.3	ns

AC SETUP REQUIREMENTS

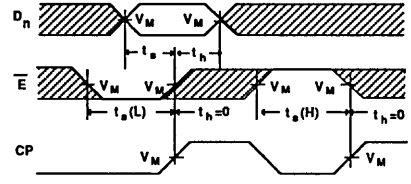
GND = 0V; $t_R = t_F = 2.5ns$; $C_L = 50pF$, $R_L = 500\Omega$

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = -40°C to +85°C, V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to CP	Waveform 2	2.0 2.0			2.0 2.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to CP	Waveform 2	1.0 1.0			1.0 1.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{E}$ to CP	Waveform 2	3.0 3.0			3.0 3.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{E}$ to CP	Waveform 2	1.0 1.0			1.0 1.0		ns
$t_w(H)$ $t_w(L)$	Clock Pulse width High or Low	Waveform 1	3.3 3.3			3.3 3.3		ns

AC WAVEFORMS



Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



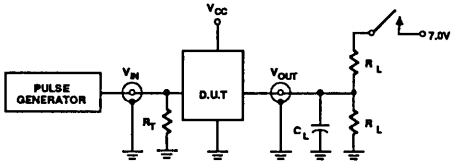
Waveform 2. Data And Enable Setup And Hold Times

NOTE: For all waveforms, $V_M = 1.5V$.

The shaded areas indicate when the input is permitted to change for predictable output performance.

Octal D-type flip-flop with enable | 74ABT377

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

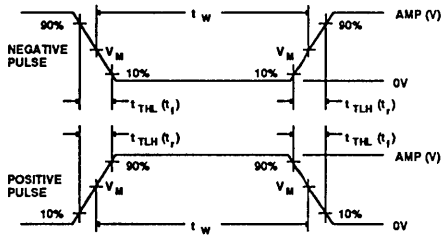
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

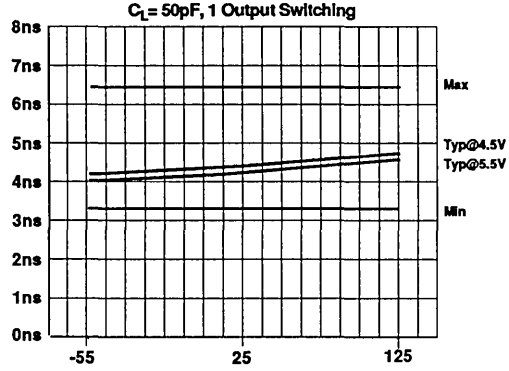


V_M = 1.5V

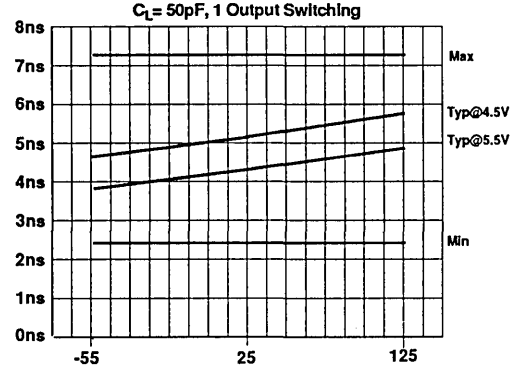
Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_w	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

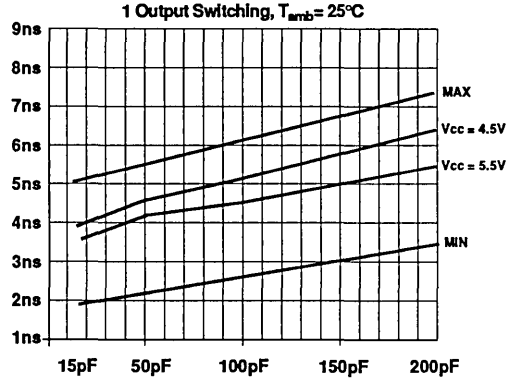
TPLH vs. TEMPERATURE (T_{amb})
C_L= 50pF, 1 Output Switching



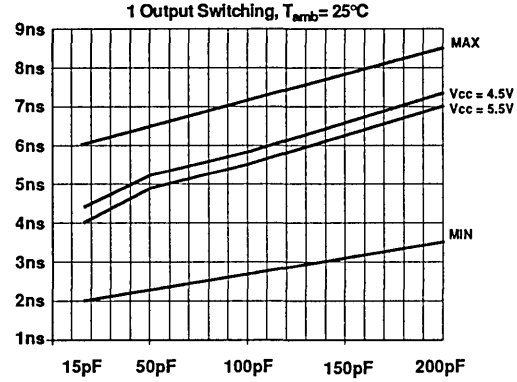
TPHL vs. TEMPERATURE (T_{amb})
C_L= 50pF, 1 Output Switching



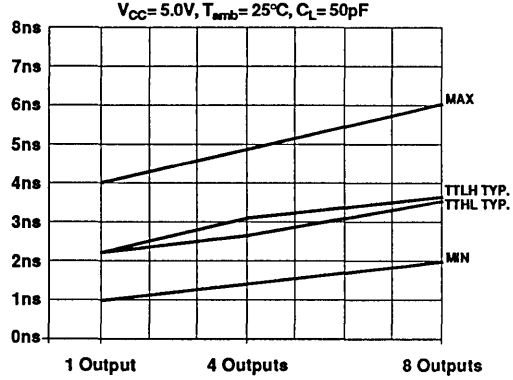
TPLH vs. LOAD CAPACITANCE[1]
1 Output Switching, T_{amb}= 25°C



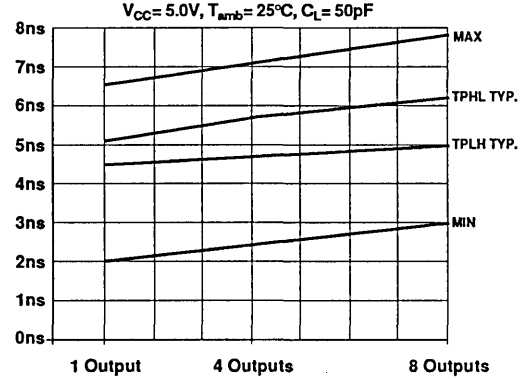
TPHL vs. LOAD CAPACITANCE[1]
1 Output Switching, T_{amb}= 25°C



TTLH TTHL vs. NUMBER OF OUTPUTS SWITCHING[1]
V_{CC}= 5.0V, T_{amb}= 25°C, C_L= 50pF



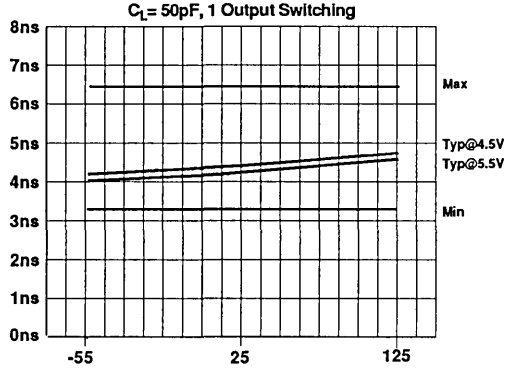
TPLH TPHL vs. NUMBER OF OUTPUTS SWITCHING[1]
V_{CC}= 5.0V, T_{amb}= 25°C, C_L= 50pF



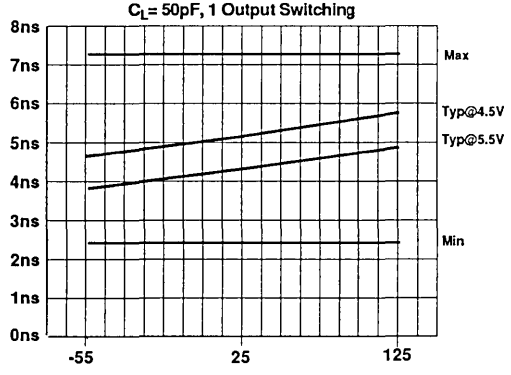
NOTES:
1. MIN and MAX lines are design characteristics and are not necessarily guaranteed by test.

Octal D-type flip-flop with enable 74ABT377

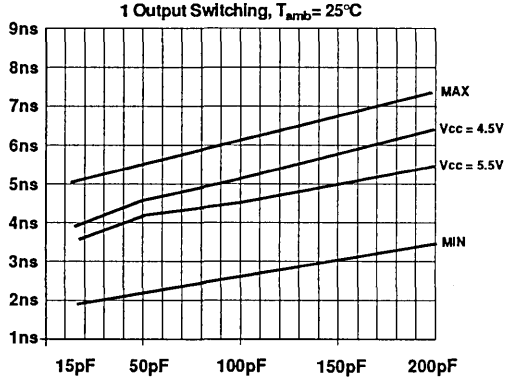
TPLH vs. TEMPERATURE (T_{amb})
C_L= 50pF, 1 Output Switching



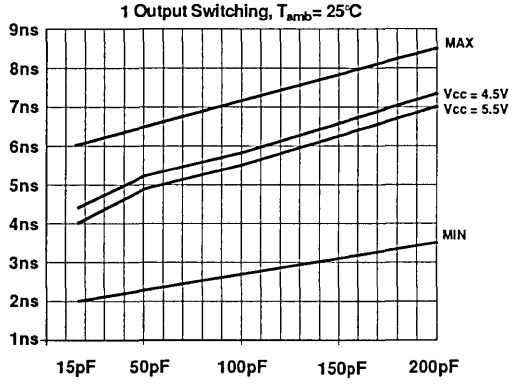
TPHL vs. TEMPERATURE (T_{amb})
C_L= 50pF, 1 Output Switching



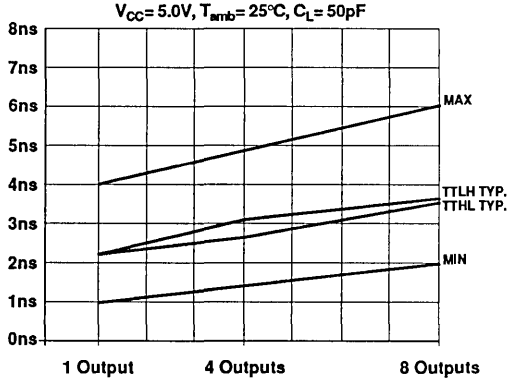
TPLH vs. LOAD CAPACITANCE[1]
1 Output Switching, T_{amb}= 25°C



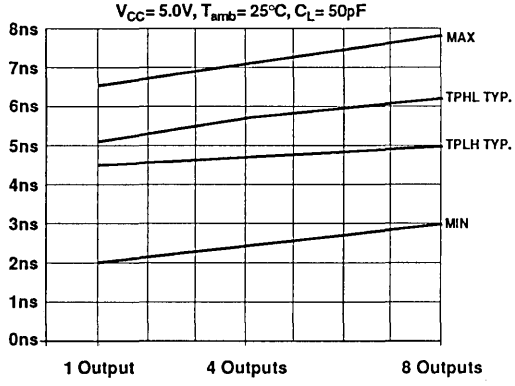
TPHL vs. LOAD CAPACITANCE[1]
1 Output Switching, T_{amb}= 25°C



TTLH TTHL vs. NUMBER OF OUTPUTS SWITCHING[1]
V_{CC}= 5.0V, T_{amb}= 25°C, C_L= 50pF



TPLH TPHL vs. NUMBER OF OUTPUTS SWITCHING[1]
V_{CC}= 5.0V, T_{amb}= 25°C, C_L= 50pF



NOTES:
1. MIN and MAX lines are design characteristics and are not necessarily guaranteed by test.

Document No.	
ECN No.	
Date of Issue	August 20, 1990
Status	Preliminary Specification
Advanced BiCMOS Products	

74ABT534

Octal D-type flip-flop, inverting (3-State)

FEATURES

- 8-bit positive edge triggered register
- 3-State output buffers
- Output capability: +64 mA/-32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The 74ABT534 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT534 is an 8-bit, edge triggered register coupled to eight 3-State output buffers. The two sections of the device are controlled independently by the clock (CP) and Output Enable ($\overline{OE}$) control gates.

The register is fully edge triggered. The state of each D input, one set-up time before the Low-to-High clock transition is transferred to the corresponding flip-flop's Q output.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	C_L = 50pF; V_{CC} = 5V	5.4	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

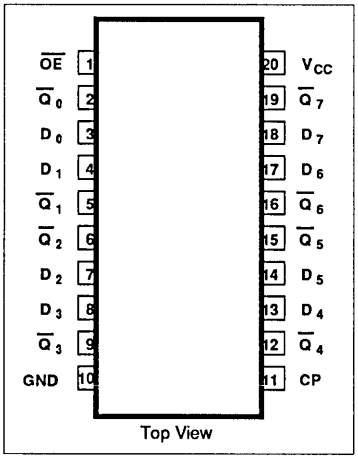
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP	-40°C to +85°C	74ABT534N
20-pin plastic SOL	-40°C to +85°C	74ABT534D

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active-Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation.

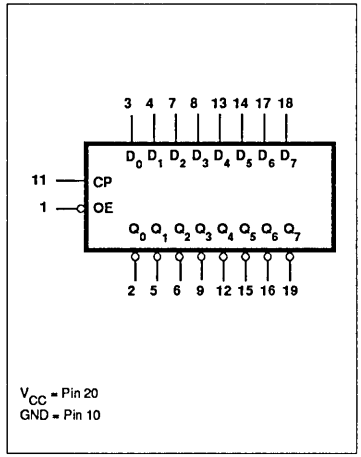
When $\overline{OE}$ is Low, the latched or transparent data appears at the outputs. When $\overline{OE}$ is High, the outputs are in the High-impedance "OFF" state, which means they will neither drive nor load the bus.

PIN CONFIGURATION

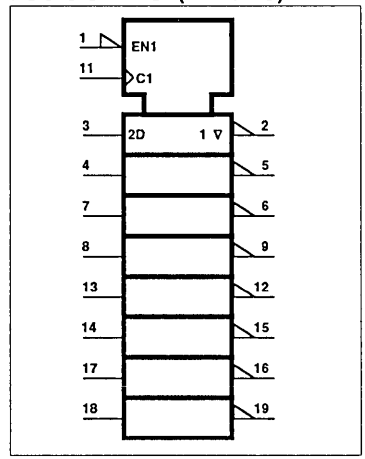


Top View

LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



Octal D-type flip-flop, inverting (3-State) 74ABT534

PIN DESCRIPTION

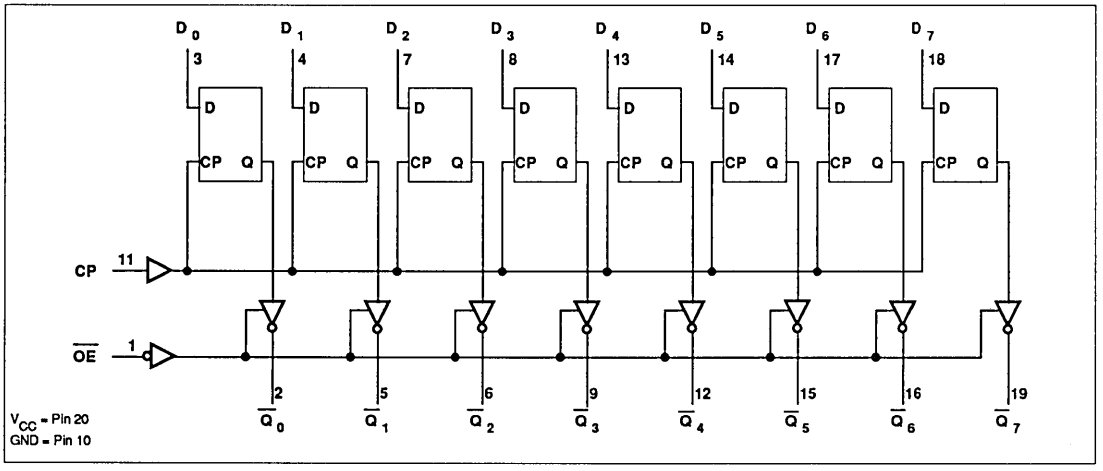
PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	Output Enable input (active Low)
3, 4, 7, 8, 13 14, 17, 18	D_0 - D_7	Data inputs
2, 5, 6, 9, 12 15, 16, 19	$\overline{Q}_0$ - $\overline{Q}_7$	Inverting 3-State outputs
11	CP	Clock Pulse input (active rising edge)
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS			INTERNAL	OUTPUTS	OPERATING MODE
$\overline{OE}$	CP	D_n	REGISTER	$\overline{Q}_0$ - $\overline{Q}_7$	
L L	↑ ↑	l h	L H	H L	Load and read register
L	↧	X	NC	NC	Hold
H H	↧ ↑	X D_n	NC D_n	Z Z	Disable outputs

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
NC = No change
X = Don't care
Z = High impedance "off" state
↑ = Low-to-High clock transition
↧ = Not a Low-to-High clock transition

LOGIC DIAGRAM



Octal D-type flip-flop, inverting (3-State) 74ABT534

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[2]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_O	DC output voltage[2]	output in Off or High state	-0.5 to +5.5	V
I_O	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

Octal D-type flip-flop, inverting (3-State) 74ABT534

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = -18mA			-1.2		-1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5			2.5		V
		V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0			3.0		
		V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]	V_{CC} = 5.5V; V_O = 2.5V	-50	-100	-180	-50	-180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		24	30		30	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5V; One input at 3.4V, other inputs at V_{CC} or GND		0.5	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

Octal D-type flip-flop, inverting (3-State) 74ABT534

AC CHARACTERISTICS

GND = 0V; $t_R = t_F = 2.5ns$; $C_L = 50pF$, $R_L = 500\Omega$

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = -40° C to +85°C		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum Clock frequency	Waveform 1	150	200		150		MHz
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{Q}_n$	Waveform 1	2.2 3.1	4.2 5.1	5.7 6.6	2.2 3.1	6.2 7.1	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	Waveform 3 Waveform 4	1.2 2.0	3.2 4.7	4.7 6.2	1.2 2.0	5.2 6.7	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	Waveform 3 Waveform 4	2.5 2.5	4.5 4.5	6.0 6.0	2.5 2.5	6.5 6.5	ns

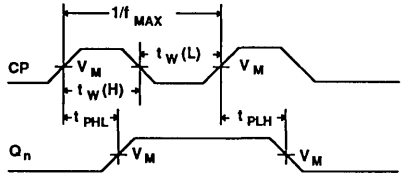
AC SETUP REQUIREMENTS

GND = 0V; $t_R = t_F = 2.5ns$; $C_L = 50pF$, $R_L = 500\Omega$

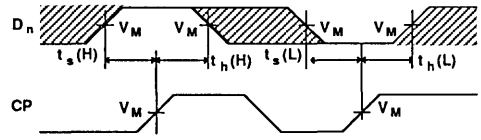
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = -40° C to +85°C, V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time D_n to CP	Waveform 2	1.0 1.5			1.0 1.5		ns
$t_h(H)$ $t_h(L)$	Hold time D_n to CP	Waveform 2	1.0 1.0			1.0 1.0		ns
$t_w(H)$	CP pulse width, High or Low	Waveform 1	3.3 3.3			3.3 3.3		ns

AC WAVEFORMS

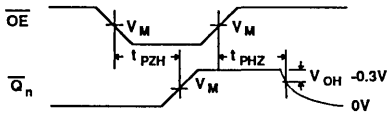
(V_M = 1.5V, V_{IN} = GND to 3.0V)



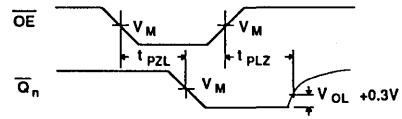
Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



Waveform 2. Data Setup And Hold Times



Waveform 3. 3-State Output Enable Time To High Level And Output Disable Time From High Level



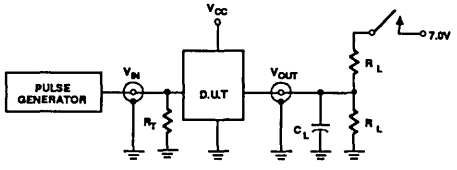
Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V

The shaded areas indicate when the input is permitted to change for predictable output performance.

Octal D-type flip-flop, inverting (3-State) 74ABT534

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

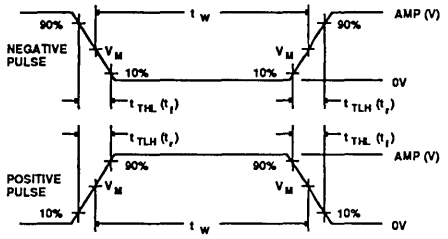
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

Document No.	
ECN No.	
Date of Issue	August 20, 1990
Status	Preliminary Specification
Advanced BiCMOS Products	

74ABT541

Octal buffer/line driver (3-State)

FEATURES

- Octal bus interface
- Functions similar to the 'ABT241
- Provides ideal interface and increases fan-out of MOS Microprocessors
- Efficient pinout to facilitate PC board layout
- 3-State buffer outputs sink 64mA and source 32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The 74ABT541 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

(continued)

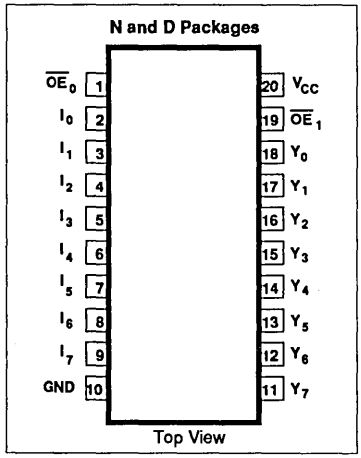
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay I_n to Y_n	C_L = 50pF; V_{CC} = 5V	2.9	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	3.5	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

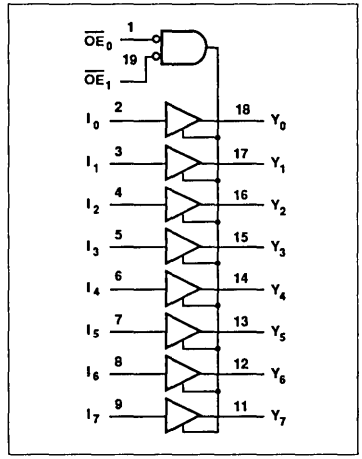
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP	-40°C to +85°C	74ABT541N
20-pin plastic SOL	-40°C to +85°C	74ABT541D

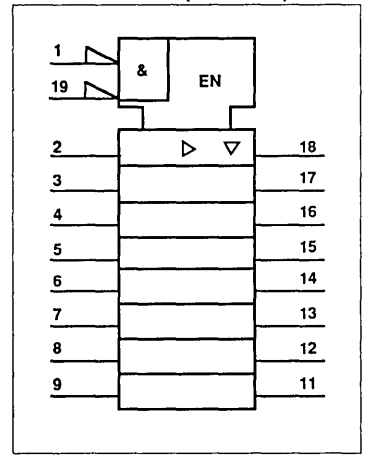
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Octal buffer/line driver (3-State) 74ABT541

The 74ABT541 is an octal buffer that is ideal for driving bus lines or buffer memory address registers. The outputs are all capable of sinking 64mA and sourcing 32mA. The device features inputs and outputs on opposite sides of the package to facilitate printed circuit board layout.

FUNCTION TABLE

INPUTS			OUTPUT
$\overline{OE}_0$	$\overline{OE}_1$	I_n	Y_n
L	L	L	L
L	L	H	H
X	H	X	Z
H	X	X	Z

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 3, 4, 5 6, 7, 8, 9	I_n	Data inputs
18, 17, 16, 15 14, 13, 12, 11	Y_n	Data outputs
1, 19	$\overline{OE}_0$, $\overline{OE}_1$	Output enables
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[2]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_O	DC output voltage[2]	output in Off or High state	-0.5 to +5.5	V
I_O	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = -18mA			-1.2		-1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5			2.5		V
		V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0			3.0		
		V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]	V_{CC} = 5.5V; V_O = 2.5V	-50	-100	-180	-50	-180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		24	30		30	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]	Outputs enabled, one input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA
		Outputs 3-State, one data input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	50		50	µA
		Outputs 3-State, one enable input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

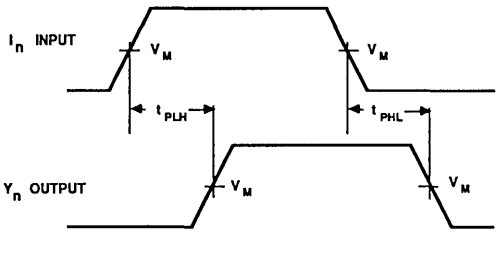
Octal buffer/line driver (3-State) 74ABT541

AC CHARACTERISTICS GND = 0V; $t_R = t_F = 2.5ns$; $C_L = 50pF$, $R_L = 500\Omega$

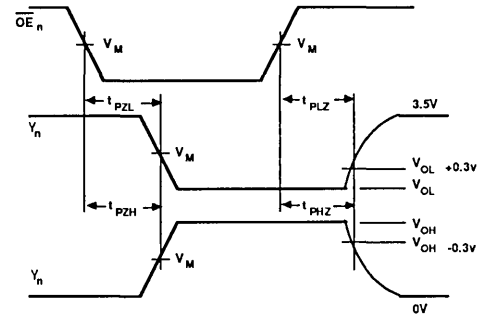
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = -40° C to +85°C, V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to Y_n	1	1.0 1.0	2.6 2.9	4.1 4.2	1.0 1.0	4.6 4.6	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.1 2.4	3.1 4.4	4.6 5.9	1.1 2.4	5.1 6.4	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	3.1 2.7	5.1 4.7	6.6 6.2	3.1 2.7	7.1 6.7	ns

AC WAVEFORMS

(V_M = 1.5V, V_{IN} = GND to 3.0V)

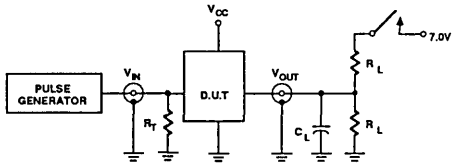


Waveform 1. Waveforms Showing the Input (I_n) to Output (Y_n) Propagation Delays



Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

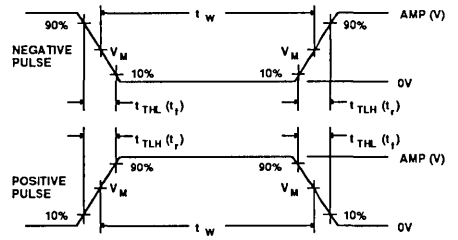
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

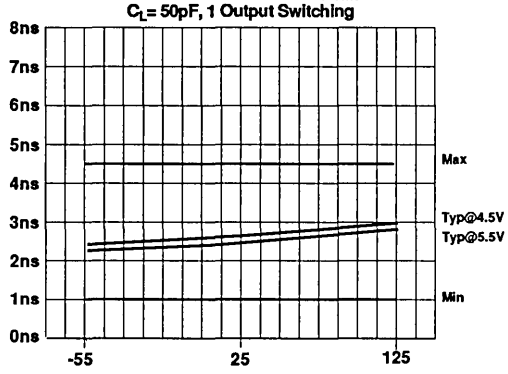


V_M = 1.5V

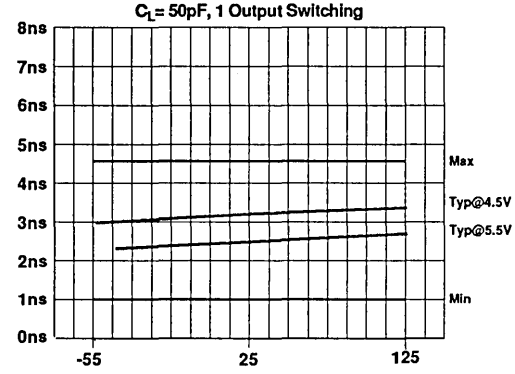
Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

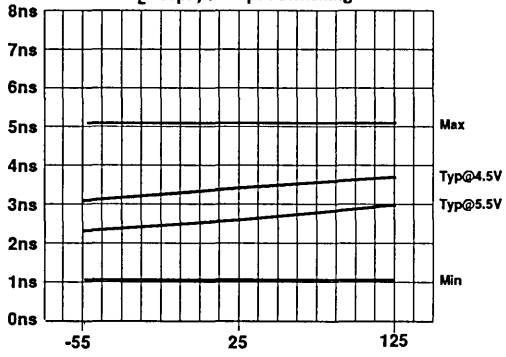
TPLH vs. TEMPERATURE (T_{amb})
C_L= 50pF, 1 Output Switching



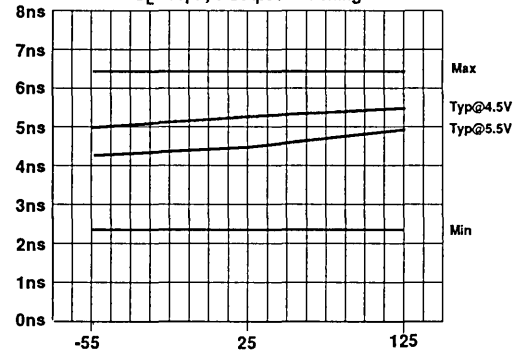
TPHL vs. TEMPERATURE (T_{amb})
C_L= 50pF, 1 Output Switching



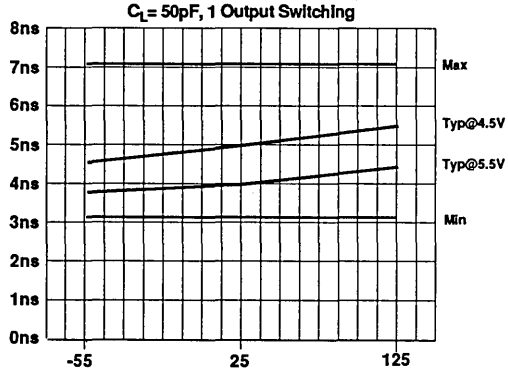
TPZH vs. TEMPERATURE (T_{amb})
C_L= 50pF, 1 Output Switching



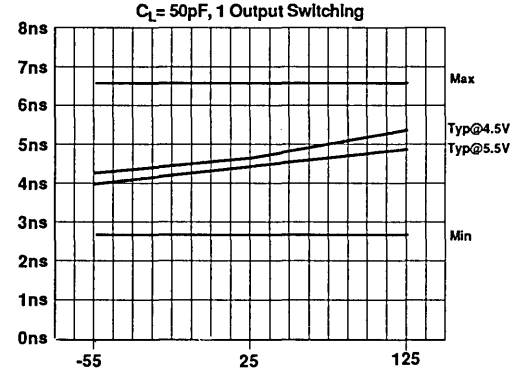
TPHZ vs. TEMPERATURE (T_{amb})
C_L= 50pF, 1 Output Switching



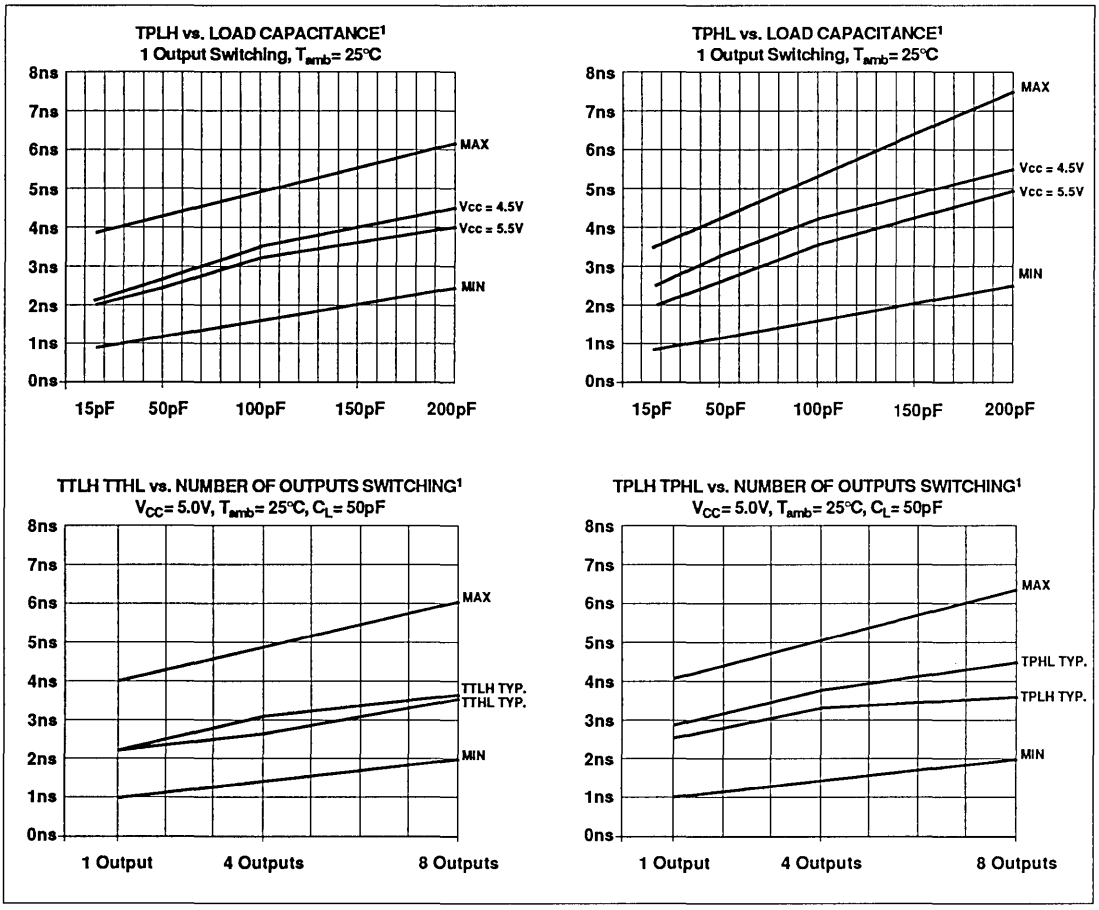
TPZL vs. TEMPERATURE (T_{amb})
C_L= 50pF, 1 Output Switching



TPLZ vs. TEMPERATURE (T_{amb})
C_L= 50pF, 1 Output Switching

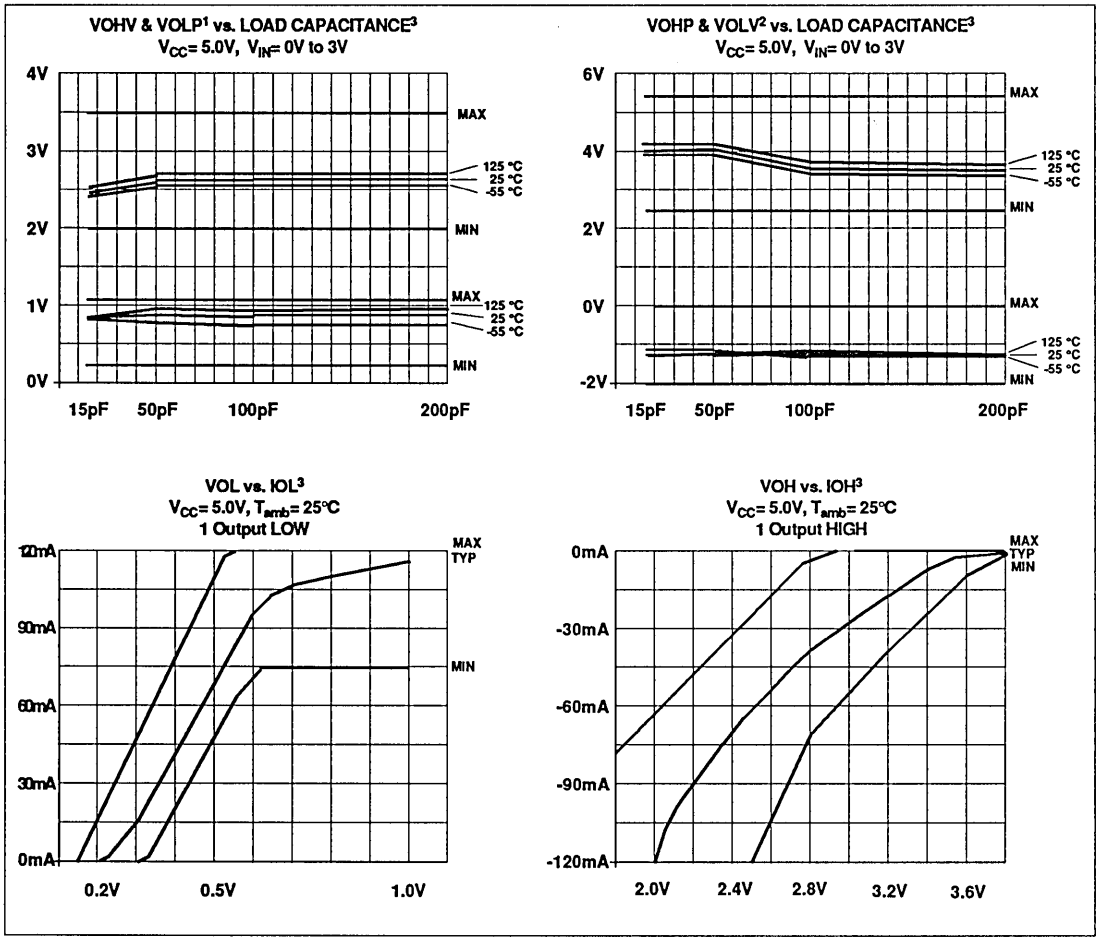


Octal buffer/line driver (3-State) 74ABT541



NOTES:
1. MIN and MAX lines are design characteristics and are not necessarily guaranteed by test.

Octal buffer/line driver (3-State) 74ABT541



NOTES:

1. VOHV is defined as the minimum (valley) voltage induced on a quiescent high-level output during switching of other outputs. VOLP is defined as the maximum (peak) voltage induced on a quiescent low-level output during switching of other outputs.
2. VOHP is defined as the maximum (peak) voltage induced on a quiescent high-level output during switching of other outputs. VOLV is defined as the minimum (valley) voltage induced on a quiescent low-level output during switching of other outputs.
3. MIN and MAX lines are design and process characteristics. They are not necessarily guaranteed by test.

Document No.	
ECN No.	
Date of Issue	November 21,1989
Status	Objective Specification
Advanced BiCMOS Products	

74ABT543

Octal latched transceiver with dual enable (3-State)

FEATURES

- Combines 74ABT245 and 74ABT373 type functions in one device
- 8-bit octal transceiver with D-type latch
- Back-to-back registers for storage
- Separate controls for data flow in each direction
- Output capability: +64 mA/-32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The 74ABT543 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT543 Octal Registered Transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable ($\overline{LEAB}$, $\overline{LEBA}$) and Output Enable ($\overline{OEAB}$, $\overline{OEBA}$) inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow. The outputs are guaranteed to sink 64mA.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay A_n to B_n	C_L = 50pF; V_{CC} = 5V	4.0	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	I/O capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

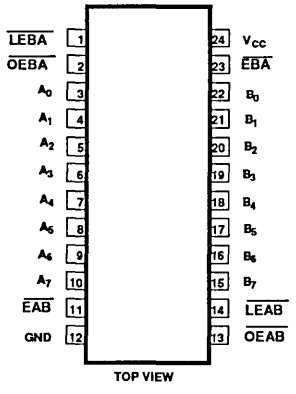
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP (300mil)	-40°C to +85°C	74ABT543N
24-pin plastic SOL (300mil)	-40°C to +85°C	74ABT543D

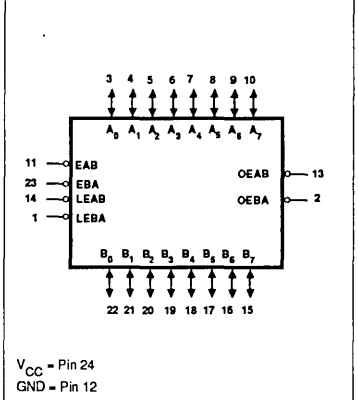
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
14, 1	$\overline{LEAB}$ / $\overline{LEBA}$	A to B / B to A Latch Enable input (Active Low)
11, 23	$\overline{EAB}$ / $\overline{EBA}$	A to B / B to A Enable input (Active Low)
13, 2	$\overline{OEAB}$ / $\overline{OEBA}$	A to B / B to A Output Enable input (Active Low)
3, 4, 5, 6 7, 8, 9, 10	A_0 - A_7	Port A, 3-State outputs
22, 21, 20, 19 18, 17, 16, 15	B_0 - B_7	Port B, 3-State outputs
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

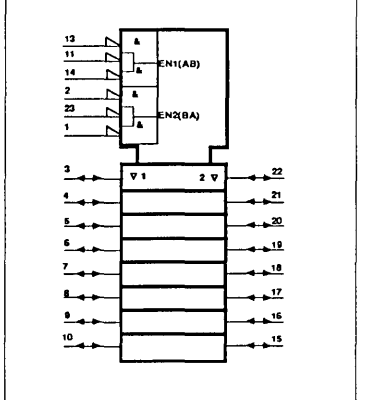
PIN CONFIGURATION



LOGIC SYMBOL

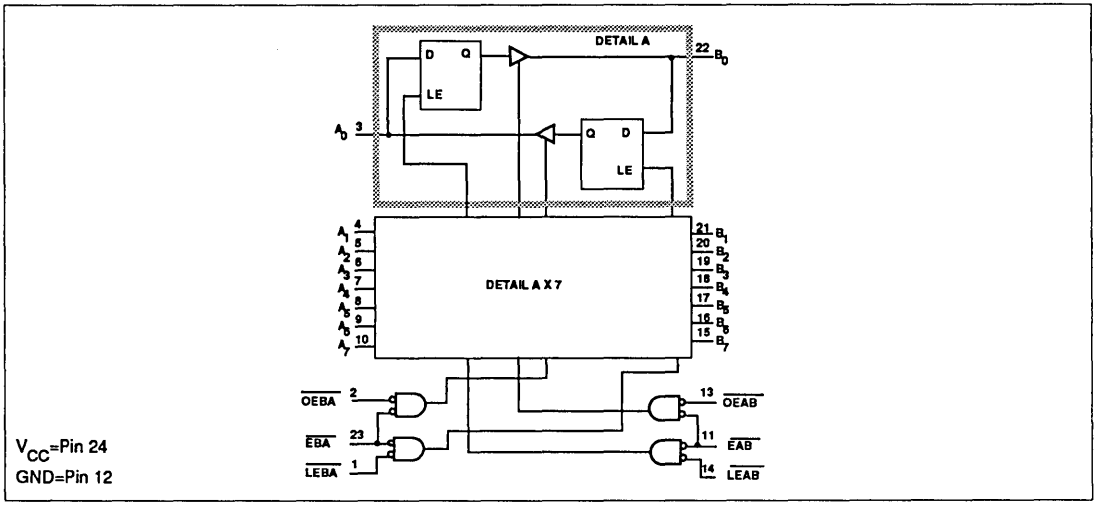


LOGIC SYMBOL(IEEE/IEC)



Octal latched transceiver with dual enable (3-State) 74ABT543

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION

The 'ABT543 contains two sets of eight D-type latches, with separate input and controls for each set. For data flow from A to B, for example, the A-to-B Enable ($\overline{EAB}$) input must be Low in order to enter data from A_0-A_7 or take data from B_0-B_7, as indicated in the Function Table. With $\overline{EAB}$ Low, a Low signal on the A-to-B Latch Enable ($\overline{LEAB}$) input makes the A-to-B latches transparent; a subsequent Low-to High transition of the $\overline{LEAB}$ signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{EAB}$ and $\overline{OEAB}$ both Low, the 3-state B output buffers are active and display the data present at the outputs of the A latches.

Control of data flow from B to A is similar, but using the $\overline{EBA}$, $\overline{LEBA}$, and $\overline{OEBA}$ inputs.

FUNCTION TABLE for 'F543 and 'F544

INPUTS				OUTPUTS	STATUS
$\overline{OEXX}$	$\overline{EXX}$	$\overline{LEXX}$	DATA		
H	X	X	X	Z	Disabled
X	H	X	X	Z	Disabled
L	↑	L	h	Z	Disabled + Latch
L	↑	L	l	Z	
L	L	↑	h	H	Latch + Display
L	L	↑	l	L	
L	L	L	H	H	Transparent
L	L	L	L	L	
L	L	H	X	NC	Hold

H= High voltage level
L= Low voltage level
h= High state must be present one setup time before the Low-to-High transition of $\overline{LEXX}$ or $\overline{EXX}$ (XX=AB or BA)
l = Low state must be present one setup time before the Low-to -High transition of $\overline{LEXX}$ or $\overline{EXX}$ (XX=AB or BA)
↑ =Low-to-High transition of $\overline{LEXX}$ or $\overline{EXX}$ (XX=AB or BA)
X=Don't care
NC=No change
Z =High impedance "off" state

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[2]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_O	DC output voltage[2]	output in Off or High state	-0.5 to +5.5	V
I_O	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

Octal latched transceiver with dual enable (3-State) 74ABT543

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = -18mA			-1.2		-1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5			2.5		V
		V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0			3.0		
		V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{IH} + I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{IL} + I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]	V_{CC} = 5.5V; V_O = 2.5V	-50	-100	-180	-50	-180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		24	30		30	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]	Outputs enabled, one input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA
		Outputs 3-State, one data input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	50		50	µA
		Outputs 3-State, one enable input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

Document No.	
ECN No.	
Date of Issue	November 21,1989
Status	Objective Specification
Advanced BiCMOS Products	

74ABT544

Octal latched transceiver with dual enable, inverting (3-State)

FEATURES

- Combines 74ABT245 and 74ABT373 type functions in one device
- 8-bit octal transceiver with D-type latch
- Back-to-back registers for storage
- Separate controls for data flow in each direction
- 3-State buffer outputs sink 64mA and source 32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The 74ABT544 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT544 Octal Registered Transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable ($\overline{LEAB}$, $\overline{LEBA}$) and Output Enable ($\overline{OEAB}$, $\overline{OEBA}$) inputs are provided for each register to permit independent control of inputting and output-

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay A_n to B_n	C_L = 50pF; V_{CC} = 5V	4.3	ns
C_{IN}	Input capacitance $\overline{LE}$, $\overline{E}$, $\overline{OE}$	V_I = 0V or V_{CC}	4	pF
C_{OUT}	I/O capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

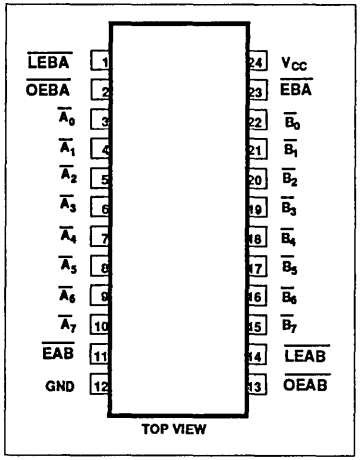
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP (300mil)	-40°C to +85°C	74ABT544N
24-pin plastic SOL (300mil)	-40°C to +85°C	74ABT544D

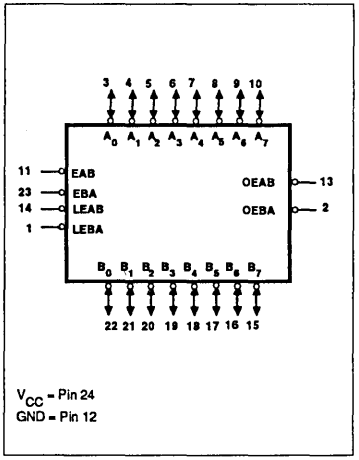
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
14, 1	$\overline{LEAB}$ / $\overline{LEBA}$	A to B / B to A Latch Enable input (Active Low)
11, 23	$\overline{EAB}$ / $\overline{EBA}$	A to B / B to A Enable input (Active Low)
13, 2	$\overline{OEAB}$ / $\overline{OEBA}$	A to B / B to A Output Enable input (Active Low)
3, 4, 5, 6 7, 8, 9, 10	$\overline{A}_0$ - $\overline{A}_7$	Port $\overline{A}$, 3-State outputs
22, 21, 20, 19 18, 17, 16, 15	$\overline{B}_0$ - $\overline{B}_7$	Port $\overline{B}$, 3-State outputs
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

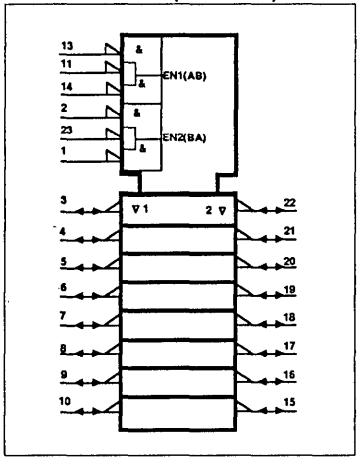
PIN CONFIGURATION



LOGIC SYMBOL

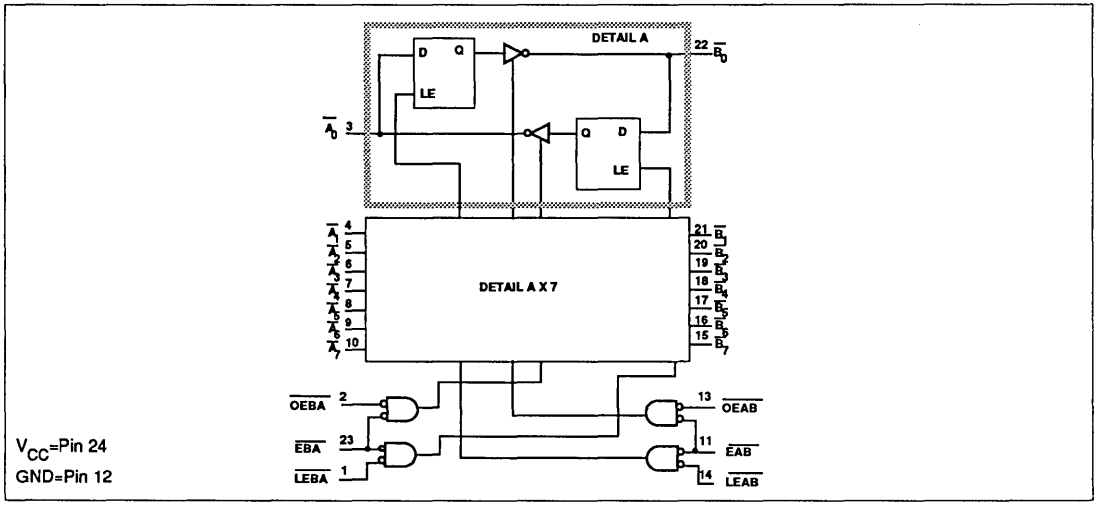


LOGIC SYMBOL(IEEE/IEC)



Octal latched transceiver with dual enable, inverting 74ABT544

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION

The 'ABT544 contains two sets of eight D-type latches, with separate input and controls for each set. For data flow from A to B, for example, the A-to-B Enable ($\overline{EAB}$) input must be Low in order to enter data from A_0-A_7 or take data from B_0-B_7, as indicated in the Function Table. With $\overline{EAB}$ Low, a Low signal on the A-to-B Latch Enable ($\overline{LEAB}$) input makes the A-to-B latches transparent; a subsequent Low-to High transition of the $\overline{LEAB}$ signal puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{EAB}$ and $\overline{OEAB}$ both Low, the 3-state B output buffers are active and display the data present at the outputs of the A latches.

Control of data flow from B to A is similar, but using the $\overline{EBA}$, $\overline{LEBA}$, and $\overline{OEBA}$ inputs.

FUNCTION TABLE for 'F543 and 'F544

INPUTS OEXX	INPUTS $\overline{EXX}$	INPUTS LEXX	INPUTS DATA	OUTPUTS	STATUS
H	X	X	X	Z	Disabled
X	H	X	X	Z	Disabled
L L	↑ ↑	L L	h l	Z Z	Disabled + Latch
L L	L L	↑ ↑	h l	L H	Latch + Display
L L	L L	L L	H L	L H	Transparent
L	L	H	X	NC	Hold

H= High voltage level
L= Low voltage level
h= High state must be present one setup time before the Low-to-High transition of $\overline{LEXX}$ or $\overline{EXX}$ (XX=AB or BA)
l = Low state must be present one setup time before the Low-to -High transition of $\overline{LEXX}$ or $\overline{EXX}$ (XX=AB or BA)
↑ =Low-to-High transition of $\overline{LEXX}$ or $\overline{EXX}$ (XX=AB or BA)
X=Don't care
NC=No change
Z =High impedance "off" state

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[2]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_O	DC output voltage[2]	output in Off or High state	-0.5 to +5.5	V
I_O	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = -18mA			-1.2		-1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5			2.5		V
		V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0			3.0		
		V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
$I_{IH} + I_{OZH}$	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
$I_{IL} + I_{OZL}$	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]	V_{CC} = 5.5V; V_O = 2.5V	-50	-100	-180	-50	-180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		24	30		30	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]	Outputs enabled, one input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA
		Outputs 3-State, one data input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	50		50	µA
		Outputs 3-State, one enable input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

Document No.	
ECN No.	853-1455 00227
Date of Issue	August 20, 1990
Status	Product Specification
Advanced BiCMOS Products	

74ABT573

Octal D-type transparent latch (3-State)

DESCRIPTION

- 74ABT573 is broadside pinout version of 74ABT373
- Inputs and Outputs on opposite side of package allow easy interface to Microprocessors
- 3-State Outputs for Bus Interfacing Common Output Enable
- Latch-up protection exceeds 500mA per JEDEC JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The 74ABT573 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT573 device is an octal transparent latch coupled to eight 3-state output buffers. The two sections of the

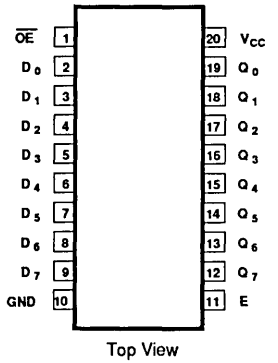
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	C_L = 50pF; V_{CC} = 5V	4.0	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

ORDERING INFORMATION

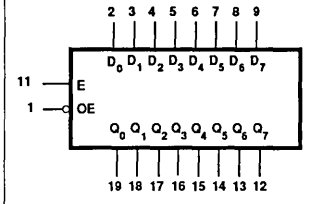
PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP	-40°C to +85°C	74ABT573N
20-pin plastic SOL	-40°C to +85°C	74ABT573D

PIN CONFIGURATION



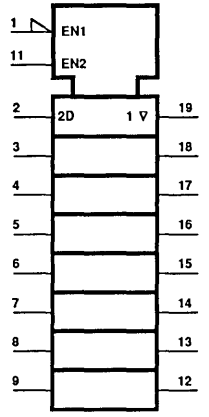
Top View

LOGIC SYMBOL



V_{CC} = Pin 20
GND = Pin 10

LOGIC SYMBOL(IEEE/IEC)



Octal D-type transparent latch (3-State) 74ABT573

device are controlled independently by Enable (E) and Output Enable ($\overline{OE}$) control gates.The 74ABT573 is functionally identical to the 74ABT373 but has a broadside pinout configuration to facilitate PC board layout and allow easy interface with microprocessors.

The data on the D inputs are transferred to the latch outputs when the Latch Enable (E) input is High. The latch remains transparent to the data inputs while E is High, and stores the data that is present one setup time before the High-to-Low enable transition.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors. The active-Low Output Enable ($\overline{OE}$) controls all eight 3-State buffers independent of the latch operation.

When $\overline{OE}$ is Low, the latched or transparent data appears at the outputs. When $\overline{OE}$ is High, the outputs are in the High-impedance "OFF" state, which means they will neither drive nor load the bus.

PIN DESCRIPTION

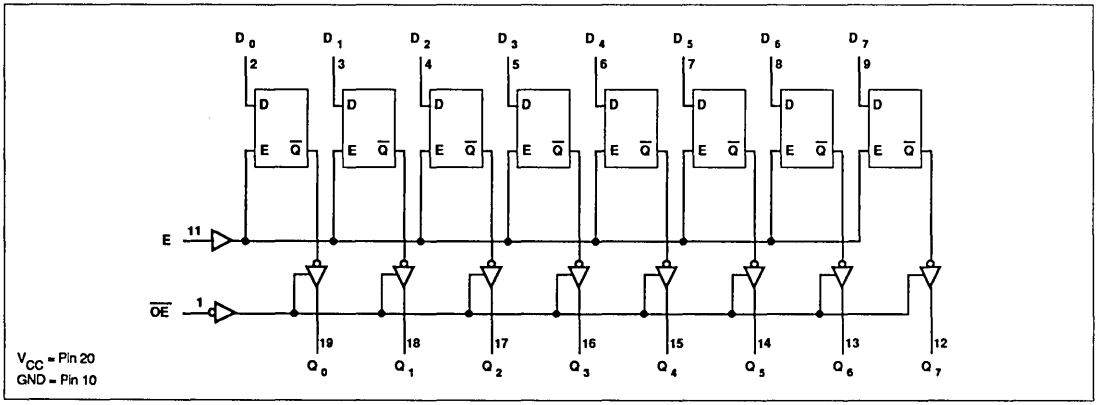
PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	Output enable input (active Low)
2, 3, 4, 5 6, 7, 8, 9	D_0 - D_7	Data inputs
19, 18, 17, 16 15, 14, 13, 12	Q_0 - Q_7	3-State Outputs
11	E	Enable input (active High)
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS			INTERNAL	OUTPUTS	OPERATING MODE
$\overline{OE}$	E	D_n	REGISTER	Q_0 - Q_7	
L L	H H	L H	L H	L H	Enable and read register
L L	↓ ↓	l h	L H	L H	Latch and read register
L	L	X	NC	NC	Hold
H H	L H	X D_n	NC D_n	Z Z	Disable outputs

H = High voltage level
h = High voltage level one set-up time prior to the High-to-Low E transition
L = Low voltage level
l = Low voltage level one set-up time prior to the High-to-Low E transition
NC = No change
X = Don't care
Z = High impedance "off" state
↓ = High-to-Low E transition

LOGIC DIAGRAM



Octal D-type transparent latch (3-State) 74ABT573

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[2]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_O	DC output voltage[2]	output in Off or High state	-0.5 to +5.5	V
I_O	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

Octal D-type transparent latch (3-State) 74ABT573

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = -18mA			-1.2		-1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5			2.5		V
		V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0			3.0		
		V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]	V_{CC} = 5.5V; V_O = 2.5V	-50	-100	-180	-50	-180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		24	30		30	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5V; One input at 3.4V, other inputs at V_{CC} or GND		0.5	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

Octal D-type transparent latch (3-State) 74ABT573

AC CHARACTERISTICS

GND = 0V; $t_R = t_F = 2.5ns$; $C_L = 50pF$, $R_L = 500\Omega$

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = -40°C to +85°C, V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	Waveform 2	1.9 2.2	3.9 4.2	5.4 5.7	1.9 2.2	5.9 6.2	ns
t_{PLH} t_{PHL}	Propagation delay E to Q_n	Waveform 1	2.6 3.2	4.6 5.2	6.1 6.7	2.2 3.2	6.6 7.2	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	Waveform 4 Waveform 5	1.2 2.7	3.2 4.7	4.7 6.2	1.2 2.7	5.2 6.7	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	Waveform 4 Waveform 5	2.5 2.0	4.9 4.5	6.4 6.0	2.5 2.0	6.9 6.5	ns

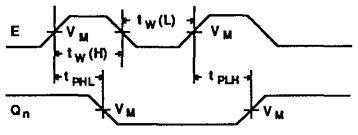
AC SETUP REQUIREMENTS

GND = 0V; $t_R = t_F = 2.5ns$; $C_L = 50pF$, $R_L = 500\Omega$

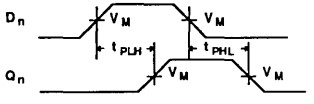
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = -40°C to +85°C, V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time D_n to E	Waveform 3	1.9 1.5			1.9 1.5		ns
$t_h(H)$ $t_h(L)$	Hold time D_n to E	Waveform 3	1.0 1.0			1.0 1.0		ns
$t_w(H)$	E pulse width, High or Low	Waveform 1	3.3			3.3		ns

AC WAVEFORMS

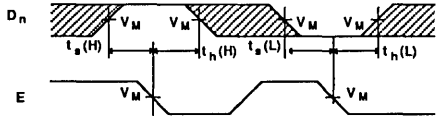
(V_M = 1.5V, V_{IN} = GND to 3.0V)



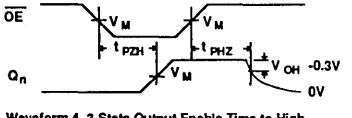
Waveform 1. Propagation Delay, Enable to Output, and Enable Pulse Width.



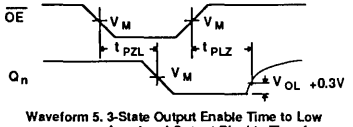
Waveform 2. Propagation Delay for Data to Outputs.



Waveform 3. Data Setup and Hold Times.



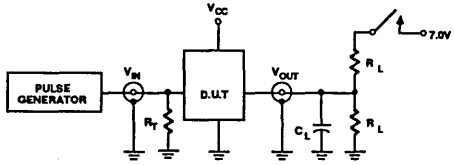
Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time From High Level.



Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level.

Octal D-type transparent latch (3-State) 74ABT573

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

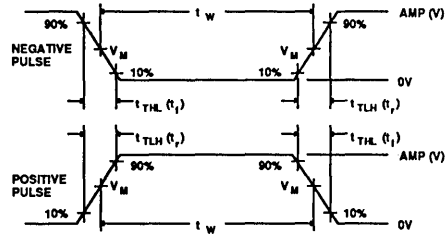
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



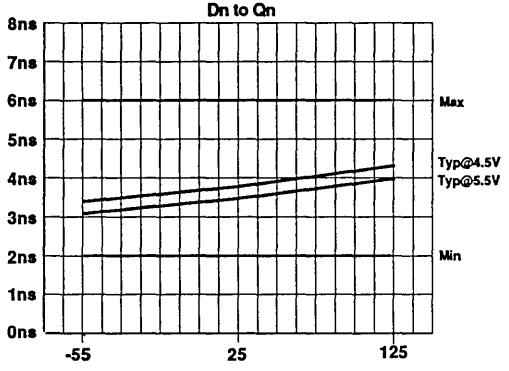
V_M = 1.5V

Input Pulse Definition

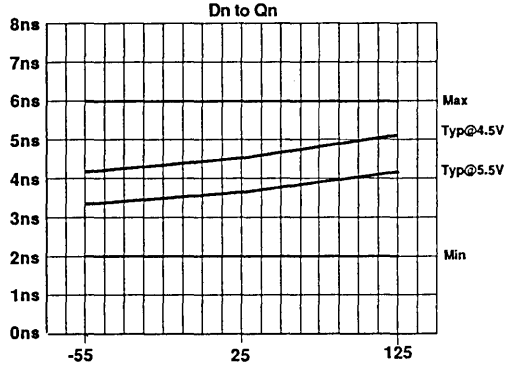
FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

Octal D-type transparent latch (3-State) 74ABT573

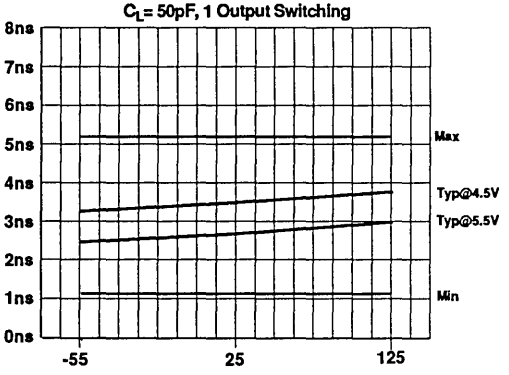
TPLH vs. TEMPERATURE (T_{amb})
C_L= 50pF, 1 Output Switching
Dn to Qn



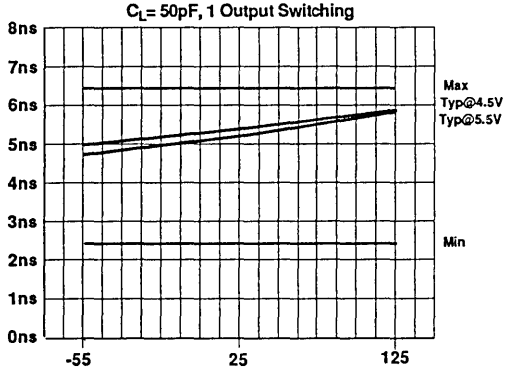
TPHL vs. TEMPERATURE (T_{amb})
C_L= 50pF, 1 Output Switching
Dn to Qn



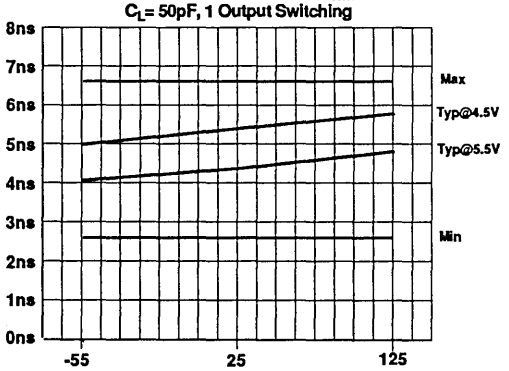
TPZH vs. TEMPERATURE (T_{amb})
C_L= 50pF, 1 Output Switching



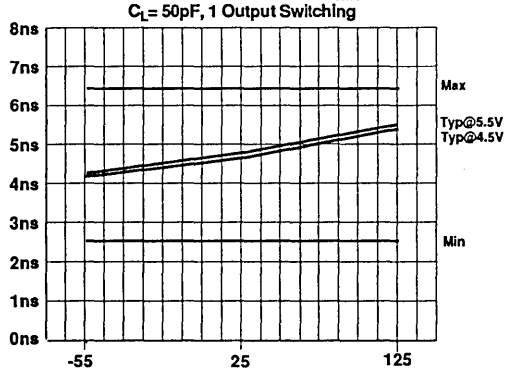
TPHZ vs. TEMPERATURE (T_{amb})
C_L= 50pF, 1 Output Switching



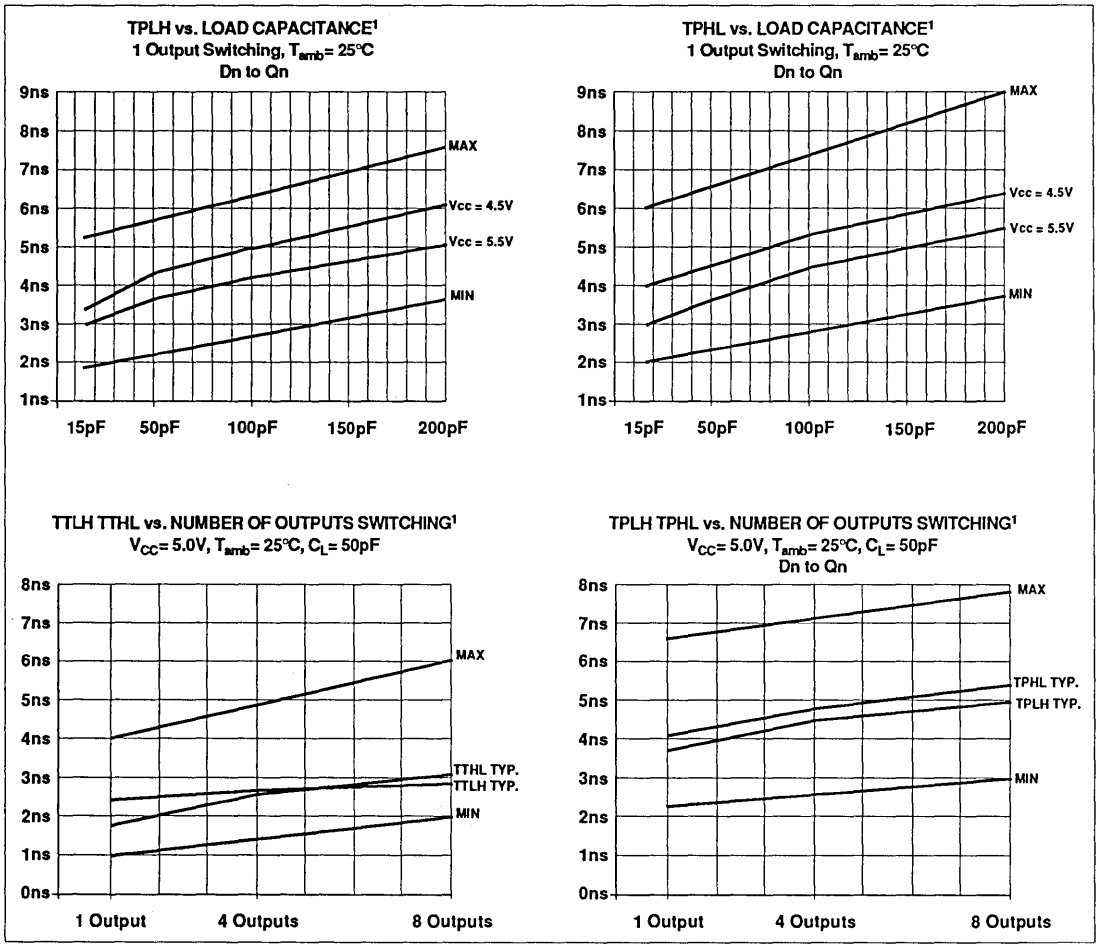
TPZL vs. TEMPERATURE (T_{amb})
C_L= 50pF, 1 Output Switching



TPLZ vs. TEMPERATURE (T_{amb})
C_L= 50pF, 1 Output Switching

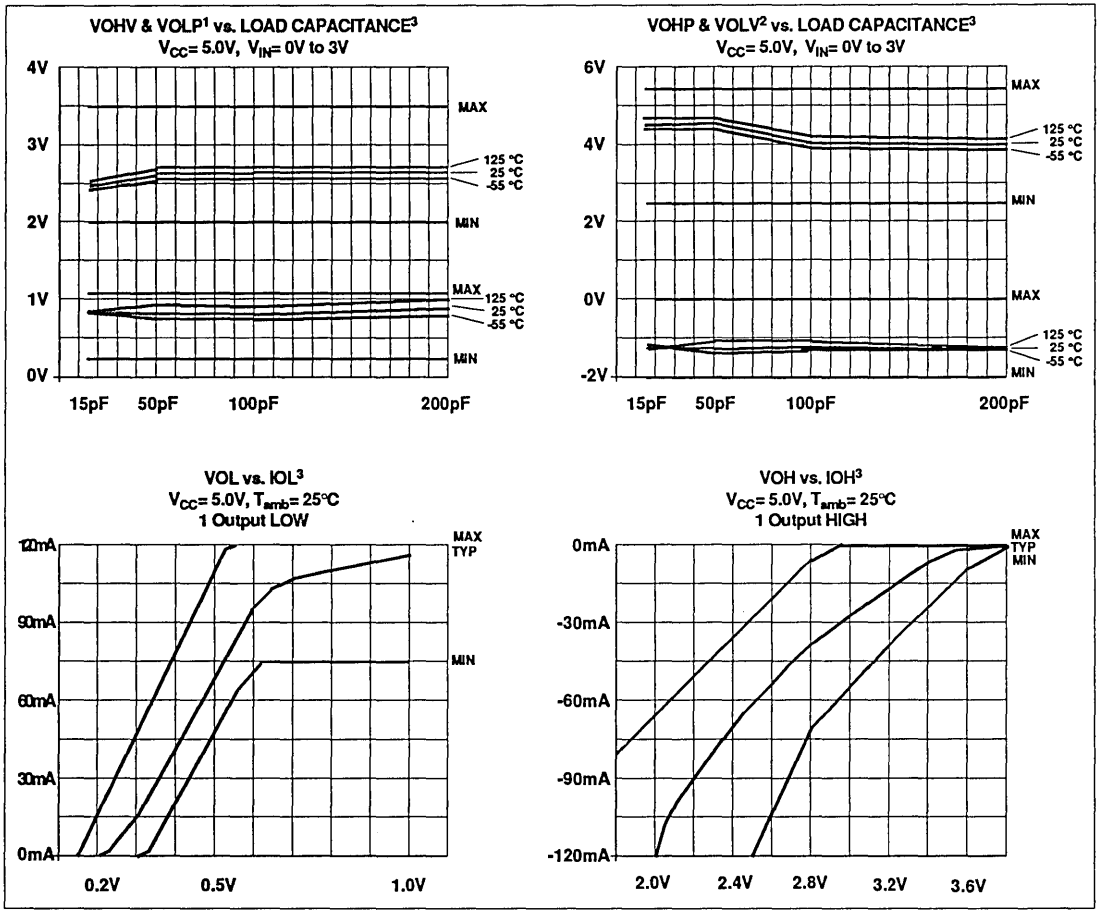


Octal D-type transparent latch (3-State) 74ABT573



NOTES:
1. MIN and MAX lines are design characteristics and are not necessarily guaranteed by test.

Octal D-type transparent latch (3-State) 74ABT573



NOTES:

1. VOHV is defined as the minimum (valley) voltage induced on a quiescent high-level output during switching of other outputs. VOLP is defined as the maximum (peak) voltage induced on a quiescent low-level output during switching of other outputs.
2. VOHP is defined as the maximum (peak) voltage induced on a quiescent high-level output during switching of other outputs. VOLV is defined as the minimum (valley) voltage induced on a quiescent low-level output during switching of other outputs.
3. MIN and MAX lines are design and process characteristics. They are not necessarily guaranteed by test.

Document No.	
ECN No.	
Date of Issue	August 20, 1990
Status	Preliminary Specification
Advanced BiCMOS Products	

74ABT574
Octal D flip-flop (3-State)

FEATURES

- 74ABT574 is broadside pinout version of 74ABT374
- Inputs and outputs on opposite side of package allow easy interface to microprocessors
- Useful as an input or output port for microprocessors
- 3-State outputs for bus interfacing common output enable
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The 74ABT574 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT574 device is an 8-bit, edge triggered register coupled to eight 3-state output buffers. The two sections of the device are controlled independently by clock (CP) and Output Enable ($\overline{OE}$) control gates.

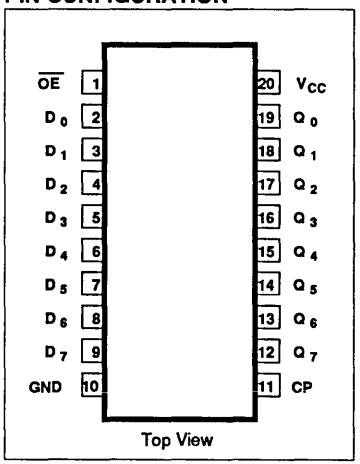
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	C_L = 50pF; V_{CC} = 5V	5.1	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

ORDERING INFORMATION

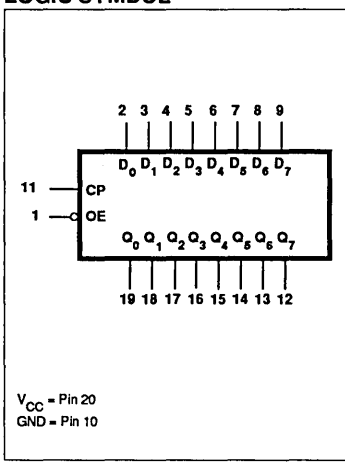
PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP	-40°C to +85°C	74ABT574N
20-pin plastic SOL	-40°C to +85°C	74ABT574D

PIN CONFIGURATION

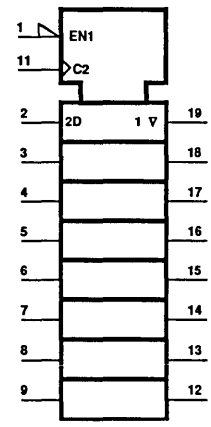


Top View

LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



Octal D flip-flop (3-State) 74ABT574

PIN DESCRIPTION

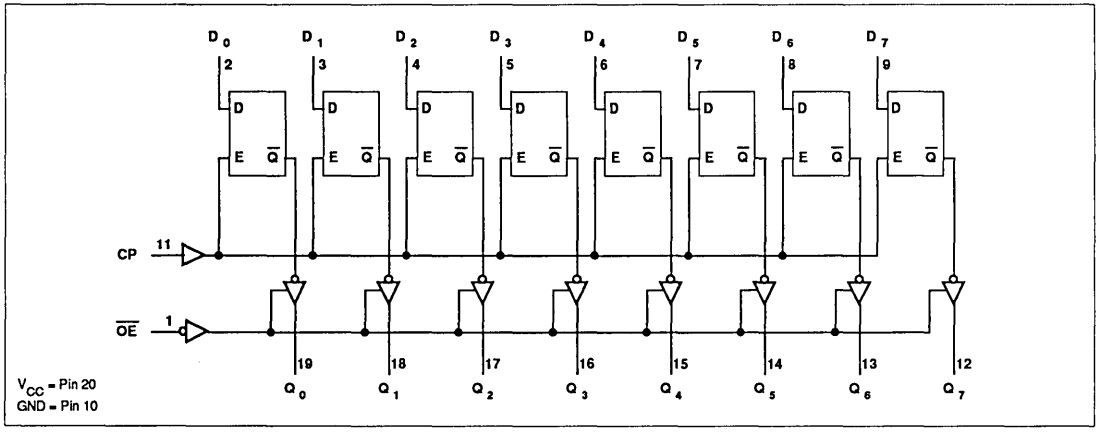
PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	Output enable input (active Low)
2, 3, 4, 5 6, 7, 8, 9	D_0 - D_7	Data inputs
19, 18, 17, 16 15, 14, 13, 12	Q_0 - Q_7	3-State Outputs
11	CP	Clock Pulse input (active rising edge)
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

FUNCTION TABLE, 74ALS373

INPUTS			INTERNAL	OUTPUTS	OPERATING MODE
$\overline{OE}$	CP	D_n	REGISTER	Q_0 - Q_7	
L L	↑ ↑	l h	L H	L H	Load and read register
L	↕	X	NC	NC	Hold
H H	↑ X	D_n X	D_n X	Z Z	Disable outputs

H = High voltage level
h = High voltage level one set-up time prior to the High-to-Low E transition
L = Low voltage level
l = Low voltage level one set-up time prior to the High-to-Low E transition
NC = No change
X = Don't care
Z = High impedance "off" state
↑ = Low-to-High clock transition
↕ = Not a Low-to-High clock transition

LOGIC DIAGRAM



Octal D flip-flop (3-State) 74ABT574

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[2]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_O	DC output voltage[2]	output in Off or High state	-0.5 to +5.5	V
I_O	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

Octal D flip-flop (3-State) 74ABT574

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = -18mA			-1.2		-1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5			2.5		V
		V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0			3.0		
		V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]	V_{CC} = 5.5V; V_O = 2.5V	-50	-100	-180	-50	-180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		24	30		30	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5V; One input at 3.4V, other inputs at V_{CC} or GND		0.5	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

Octal D flip-flop (3-State) 74ABT574

AC CHARACTERISTICS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω

SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V			T_{amb} = -40° C to +85°C V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum Clock frequency	Waveform 1	150	200		150		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	Waveform 1	2.2 3.1	4.2 5.1	5.7 6.6	2.2 3.1	6.2 7.1	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	Waveform 3 Waveform 4	1.2 2.0	3.2 4.7	4.7 6.2	1.2 2.0	5.2 6.7	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	Waveform 3 Waveform 4	2.5 2.5	4.5 4.5	6.0 6.0	2.5 2.5	6.5 6.5	ns

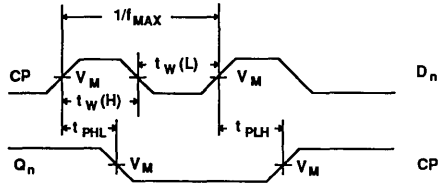
AC SETUP REQUIREMENTS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω

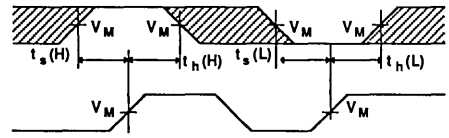
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V			T_{amb} = -40° C to +85°C V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Set-up time D_n to CP	Waveform 2	1.0 1.5			1.0 1.5		ns
$t_h(H)$ $t_h(L)$	Hold time D_n to CP	Waveform 2	1.0 1.0			1.0 1.0		ns
$t_w(H)$ $t_w(L)$	CP pulse width, High or Low	Waveform 1	3.3 3.3			3.3 3.3		ns

AC WAVEFORMS

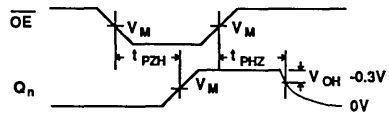
(V_M = 1.5V, V_{IN} = GND to 3.0V)



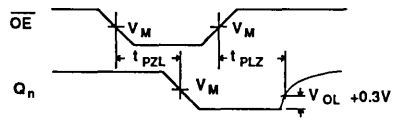
Waveform 1. Propagation Delay, Clock to Output, Clock Pulse Width and Maximum Clock Frequency.



Waveform 2. Data Setup and Hold Times.

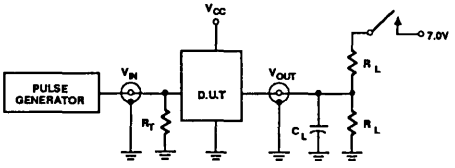


Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time From High Level.



Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

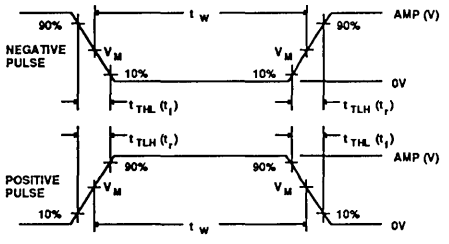
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

Document No.	
ECN No.	
Date of Issue	November 21, 1989
Status	Objective Specification
Advanced BiCMOS Products	

74ABT620

Octal transceiver with dual enable, inverting (3-State)

FEATURES

- Octal bidirectional bus interface
- 3-State buffer outputs sink 64mA and source 32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The 74ABT620 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT620 device is an octal transceiver featuring inverting 3-State bus compatible outputs in both send and receive directions. The 74ABT620 is designed for asynchronous two-way communication between data busses. The control function implementation allows for maximum flexibility in timing. This device allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic levels at the Enable inputs ($\overline{OEBA}$ and OEAB). The Enable inputs can be used to disable the device so that the busses are effectively isolated. The dual-enable configuration gives the

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay A_n to B_n, or B_n to A_n	C_L = 50pF; V_{CC} = 5V	3.5	ns
C_{IN}	Input capacitance OE, $\overline{OE}$	V_I = 0V or V_{CC}	4	pF
C_{OUT}	I/) capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

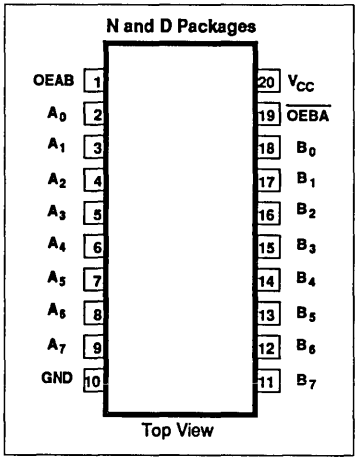
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP	-40°C to +85°C	74ABT620N
20-pin plastic SOL	-40°C to +85°C	74ABT620D

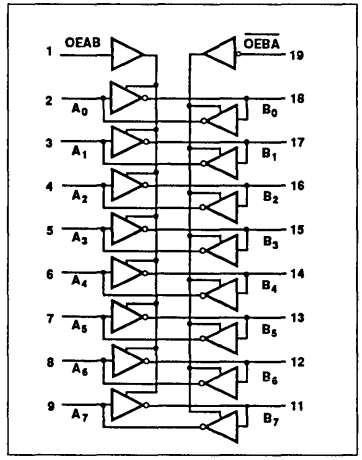
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	OEAB	Output Enable input
2, 3, 4, 5 6, 7, 8, 9	A_0 - A_7	Data inputs/outputs (A side)
18, 17, 16, 15 14, 13, 12, 11	B_0 - B_7	Data inputs/outputs (B side)
19	$\overline{OEBA}$	Ouput Enable input
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

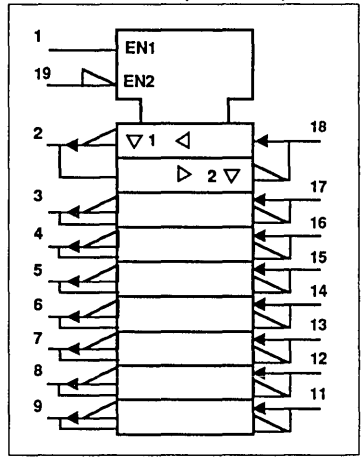
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Octal transceiver with dual enable, inverting 74ABT620

'ABT620 the capability to store data by simultaneously enabling $\overline{OEBA}$ and OEAB. Each output reinforces its input in this transceiver configuration. Thus when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states.

FUNCTION TABLE

INPUTS		INPUTS / OUTPUTS	
$\overline{OEBA}$	OEAB	A_n	B_n
L	L	$\overline{B}_n$	Inputs
H	H	Inputs	$\overline{A}_n$
H	L	Z	Z
L	H	$\overline{B}_n$ or Inputs	Inputs $\overline{A}_n$

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[2]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_O	DC output voltage[2]	output in Off or High state	-0.5 to +5.5	V
I_O	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = -18mA			-1.2		-1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5			2.5		V
		V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0			3.0		
		V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{IH} + I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{IL} + I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]	V_{CC} = 5.5V; V_O = 2.5V	-50	-100	-180	-50	-180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		24	30		30	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]	Outputs enabled, one input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA
		Outputs 3-State, one data input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	50		50	µA
		Outputs 3-State, one enable input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

Philips Components—Signetics

Document No.	
ECN No.	
Date of Issue	August 20,1990
Status	Preliminary Specification
Advanced BiCMOS Products	

74ABT623

Octal transceiver with dual enable, non-inverting (3-State)

FEATURES

- Octal bidirectional bus interface
- 3-State buffers
- Output capability: +64 mA/-32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The 74ABT623 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT623 device is an octal transceiver featuring non-inverting 3-State bus compatible outputs in both send

(continued)

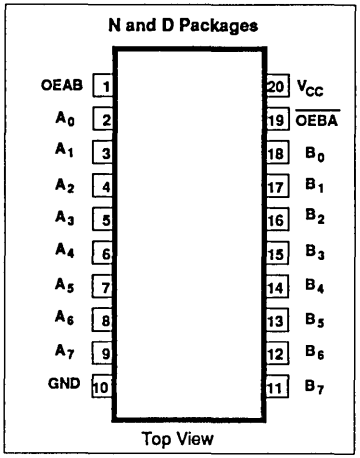
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay A_n to B_n, or B_n to A_n	C_L = 50pF; V_{CC} = 5V	2.9	ns
C_{OExx}	Input capacitance	V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	I/O pin capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

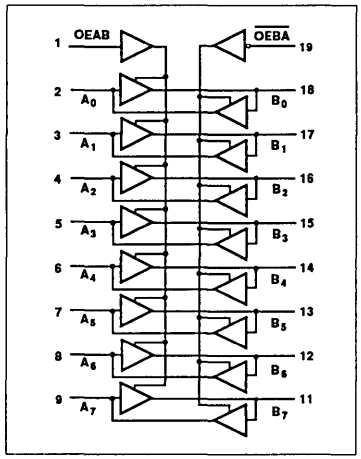
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-Pin Plastic DIP	-40°C to +85°C	74ABT623N
20-Pin Plastic SOL	-40°C to +85°C	74ABT623D

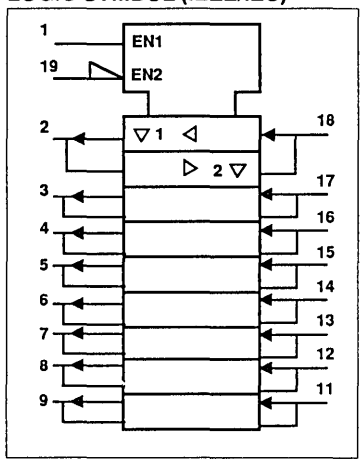
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Octal transceiver with dual enable, non-inverting (3-State) 74ABT623

and receive directions. The 74ABT623 is designed for asynchronous two-way communication between data busses.

The control function implementation allows for maximum flexibility in timing. This device allows data transmission from the A bus to the B bus or from the B bus to the A bus, depending upon the logic levels at the Enable inputs ($\overline{OEBA}$ and OEAB). The Enable inputs can be used to disable the device so that the busses are effectively isolated. The dual-enable configuration gives the 'ABT623 the capability to store data by simultaneously enabling $\overline{OEBA}$ and OEAB. Each output reinforces its input in this transceiver configuration. Thus when both control inputs are enabled and all other data sources to the two sets of bus lines are at high impedance, both sets of bus lines (16 in all) will remain at their last states.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[2]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_O	DC output voltage[2]	output in Off or High state	-0.5 to +5.5	V
I_O	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
$\overline{OEBA}$	OEAB	A_n	B_n
L	L	A = B	Inputs
H	H	Inputs	B = A
H	L	Z	Z
L	H	A=B	B=A

PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	OEAB	Output Enablel input
2, 3, 4, 5 6, 7, 8, 9	A_0 - A_7	Data inputs/outputs (A side)
18, 17, 16, 15 14, 13, 12, 11	B_0 - B_7	Data inputs/outputs (B side)
19	$\overline{OEBA}$	Ouput Enable input
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = -18mA			-1.2		-1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5			2.5		V
		V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0			3.0		
		V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{IH} + I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{IL} + I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]	V_{CC} = 5.5V; V_O = 2.5V	-50	-100	-180	-50	-180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		24	30		30	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]	Outputs enabled, one input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA
		Outputs 3-State, one data input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	50		50	µA
		Outputs 3-State, one enable input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

Octal transceiver with dual enable, non-inverting (3-State) 74ABT623

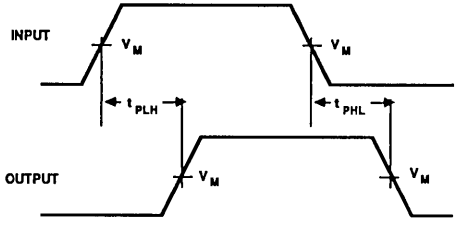
AC CHARACTERISTICS

GND = 0V; $t_R = t_F$ = 2.5ns; C_L = 50pF, R_L = 500Ω

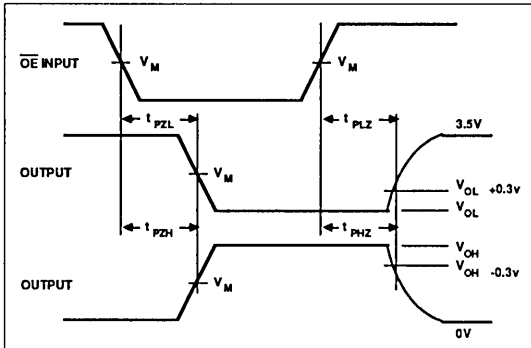
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = -40° C to +85°C, V_{CC} = +5.0V ±0.5V		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n or B_n to A_n	1	1.0 1.3	3.0 3.3	4.5 4.8	1.0 1.3	5.0 5.3	ns
t_{PZH} t_{PZL}	Output enable time to High and Low level	2	1.7 1.7	5.0 5.0	6.5 6.5	1.7 1.7	7.0 7.0	ns
t_{PHZ} t_{PLZ}	Output disable time from High and Low level	2	2.7 1.9	5.7 4.9	7.2 6.4	2.7 1.9	8.2 6.9	ns

AC WAVEFORMS

(V_M = 1.5V, V_{IN} = GND to 3.0V)

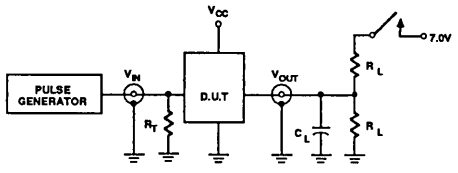


Waveform 1. Waveforms Showing the Input to Output Propagation Delays



Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

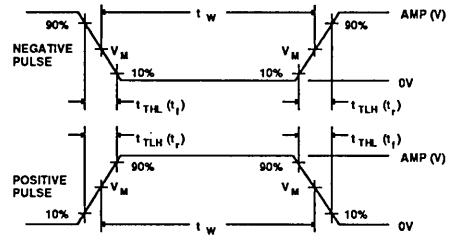
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

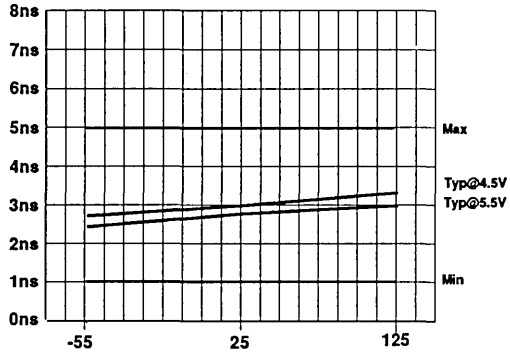


V_M = 1.5V

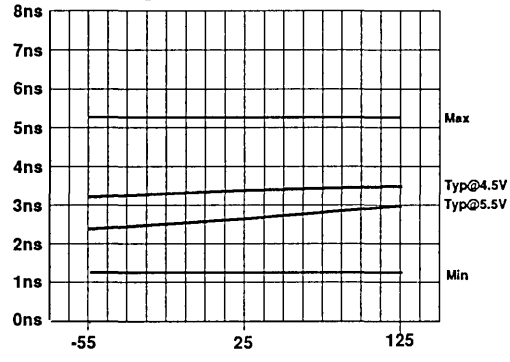
Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

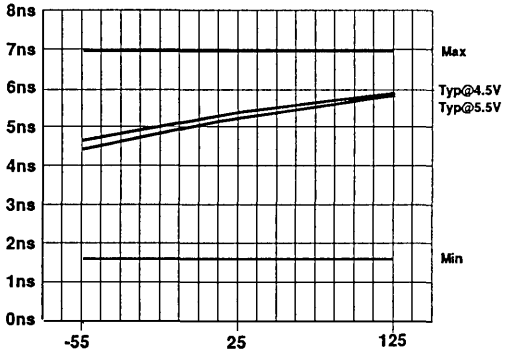
TPLH vs. TEMPERATURE (T_{amb})
C_L= 50pF, 1 Output Switching



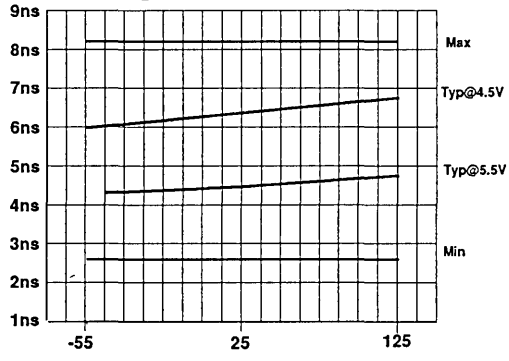
TPHL vs. TEMPERATURE (T_{amb})
C_L= 50pF, 1 Output Switching



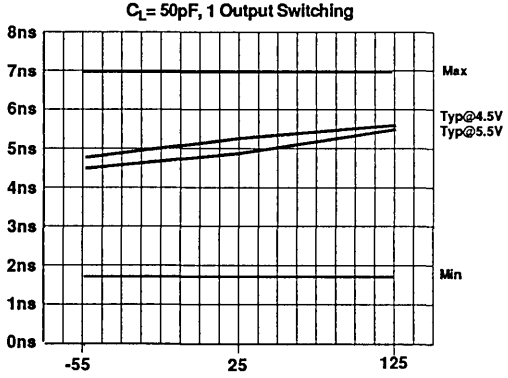
TPZH vs. TEMPERATURE (T_{amb})
C_L= 50pF, 1 Output Switching



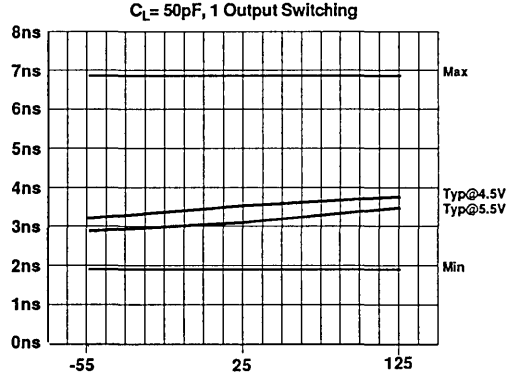
TPHZ vs. TEMPERATURE (T_{amb})
C_L= 50pF, 1 Output Switching



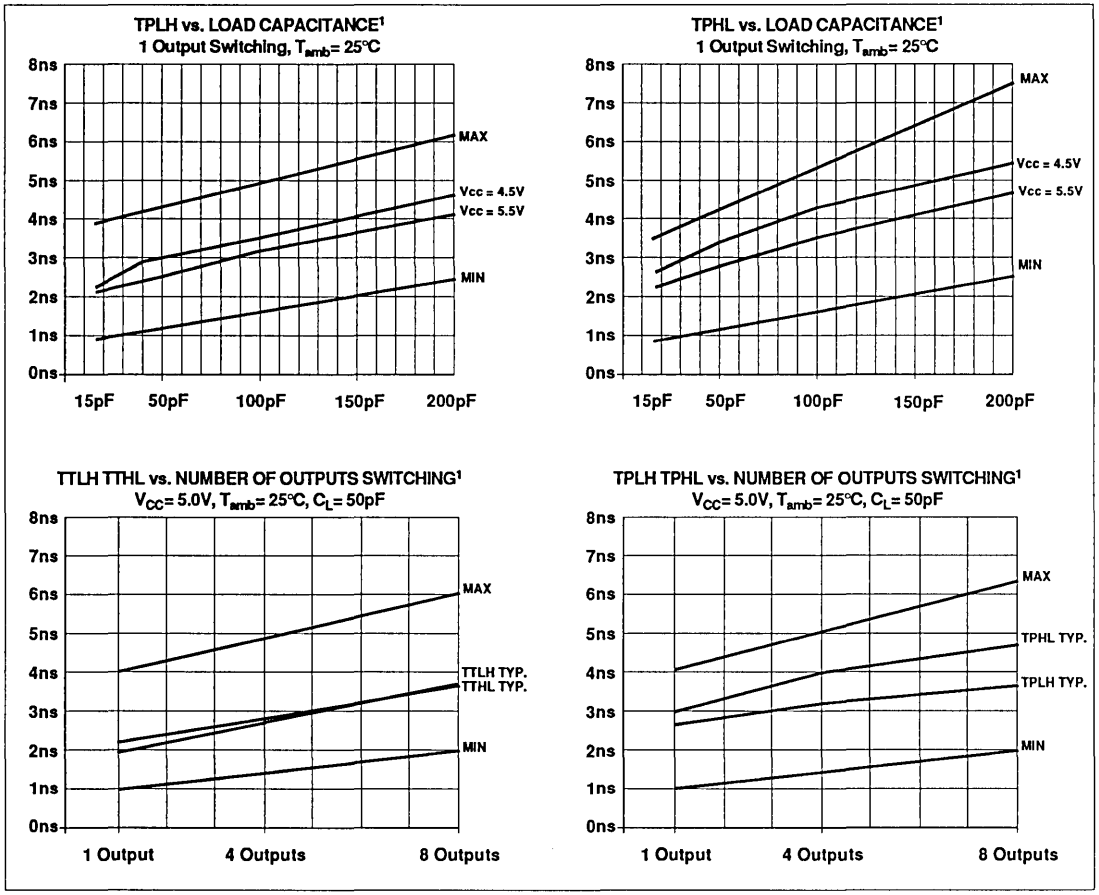
TPZL vs. TEMPERATURE (T_{amb})
C_L= 50pF, 1 Output Switching



TPLZ vs. TEMPERATURE (T_{amb})
C_L= 50pF, 1 Output Switching

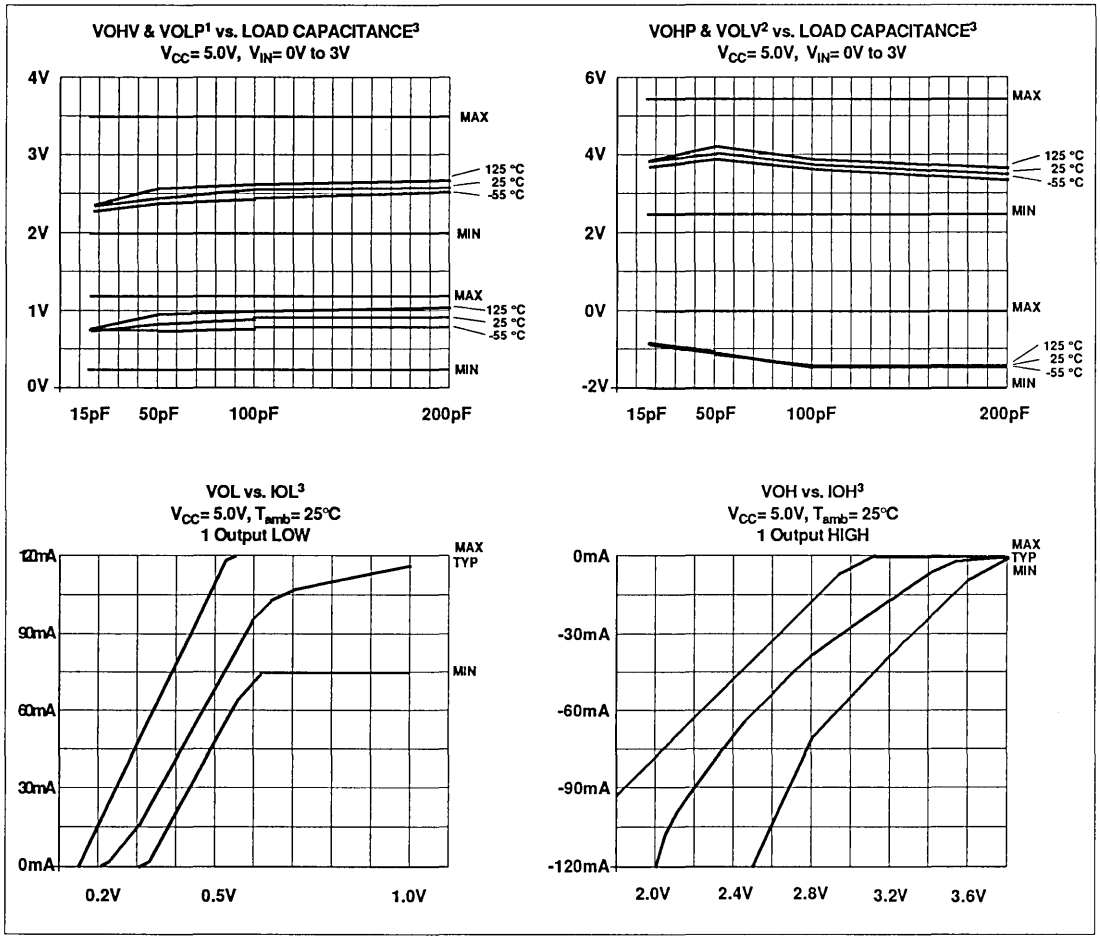


Octal transceiver with dual enable, non-inverting (3-State) 74ABT623



NOTES:
1. MIN and MAX lines are design characteristics and are not necessarily guaranteed by test.

Octal transceiver with dual enable, non-inverting (3-State) 74ABT623



NOTES:

1. VOHV is defined as the minimum (valley) voltage induced on a quiescent high-level output during switching of other outputs. VOLP is defined as the maximum (peak) voltage induced on a quiescent low-level output during switching of other outputs.
2. VOHP is defined as the maximum (peak) voltage induced on a quiescent high-level output during switching of other outputs. VOLV is defined as the minimum (valley) voltage induced on a quiescent low-level output during switching of other outputs.
3. MIN and MAX lines are design and process characteristics. They are not necessarily guaranteed by test.

Document No.	
ECN No.	
Date of Issue	November 21, 1989
Status	Objective Specification
Advanced BiCMOS Products	

74ABT640

Octal transceiver with direction pin, inverting (3-State)

FEATURES

- Octal bidirectional bus interface
- Output capability: +64 mA/-32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The 74ABT640 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT640 device is an octal transceiver featuring inverting 3-State bus compatible outputs in both send and receive directions. The control function implementation minimizes external timing requirements. The device features an Output Enable ($\overline{OE}$) input for easy cascading and a Direction (DIR) input for direction control.

FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
$\overline{OE}$	DIR	A_n	B_n
L	L	$\overline{B}_n$	Inputs
L	H	Inputs	$\overline{A}_n$
H	X	Z	Z

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay A_n to B_n, or B_n to A_n	C_L = 50pF; V_{CC} = 5V	3.5	ns
C_{IN}	Input capacitance DIR, $\overline{OE}$	V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	I/O capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

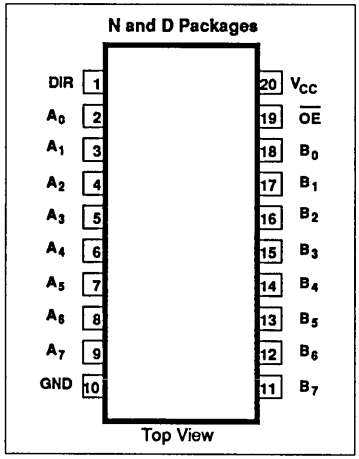
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
20-pin plastic DIP	-40°C to +85°C	74ABT640N
20-pin plastic SOL	-40°C to +85°C	74ABT640D

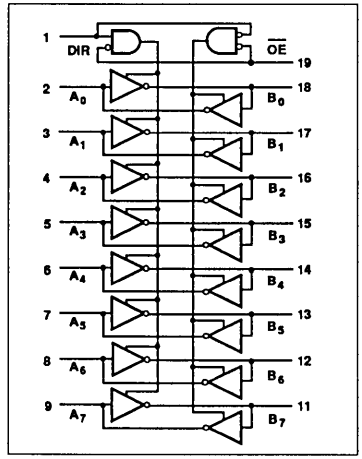
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	DIR	Direction control input
2, 3, 4, 5 6, 7, 8, 9	A_0 - A_7	Data inputs/outputs (A side)
18, 17, 16, 15 14, 13, 12, 11	B_0 - B_7	Data inputs/outputs (B side)
19	$\overline{OE}$	Ouput enable
10	GND	Ground (0V)
20	V_{CC}	Positive supply voltage

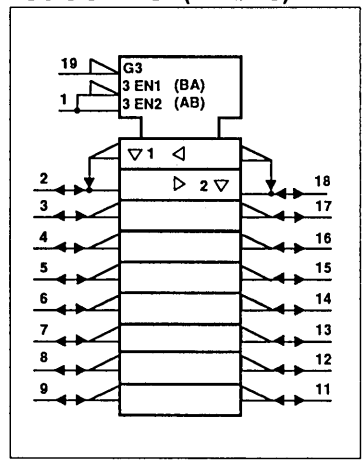
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



Octal transceiver with direction pin, inverting (3-State) 74ABT640

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[2]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_O	DC output voltage[2]	output in Off or High state	-0.5 to +5.5	V
I_O	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

Octal transceiver with direction pin, inverting (3-State) 74ABT640

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = -18mA			-1.2		-1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5			2.5		V
		V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0			3.0		
		V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
$I_{IH} + I_{OZH}$	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
$I_{IL} + I_{OZL}$	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]	V_{CC} = 5.5V; V_O = 2.5V	-50	-100	-180	-50	-180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		24	30		30	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]	Outputs enabled, one input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA
		Outputs 3-State, one data input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	50		50	µA
		Outputs 3-State, one enable input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

Philips Components—Signetics

Document No.	
ECN No.	
Date of Issue	November 21, 1989
Status	Objective Specification
Advanced BiCMOS Products	

74ABT646

Octal bus transceiver/register (3-State)

FEATURES

- Combines 'ABT245 and 'ABT374 type functions in one device
- Independent registers for A and B buses
- Multiplexed real-time and stored data
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The 74ABT646 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT646 Transceiver/Register consists of bus transceiver circuits with 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes High. Output Enable ($\overline{OE}$) and DIR pins are provided to control the transceiver function. In the transceiver mode, data present at the high impedance port may be stored in either the A or B register or both. *(continued)*

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay A_n to B_n, or B_n to A_n	C_L = 50pF; V_{CC} = 5V	4.5	ns
C_{IN}	Input capacitance CP, S, $\overline{OE}$	V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	I/O capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

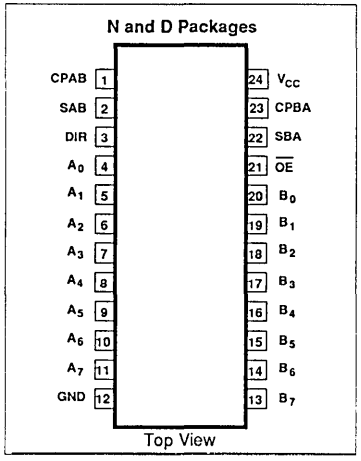
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP (300mil)	-40°C to +85°C	74ABT646N
24-pin plastic SOL (300mil)	-40°C to +85°C	74ABT646D

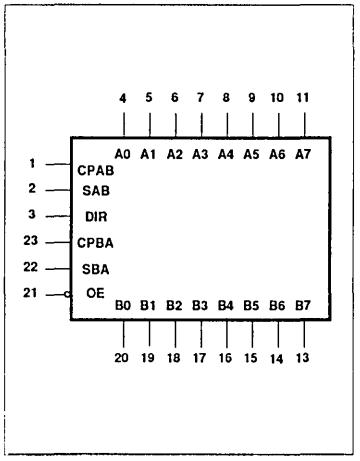
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1,23	CPAB / CPBA	Clock input A to B / Clock input B to A
2, 22	SAB / SBA	Select input A to B / Select input B to A
3	DIR	Direction control input
4, 5, 6, 7 8, 9, 10, 11	A_0 - A_7	Data inputs/outputs (A side)
20, 19, 18, 17 16, 15, 14, 13	B_0 - B_7	Data inputs/outputs (B side)
21	$\overline{OE}$	Ouput enable input
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

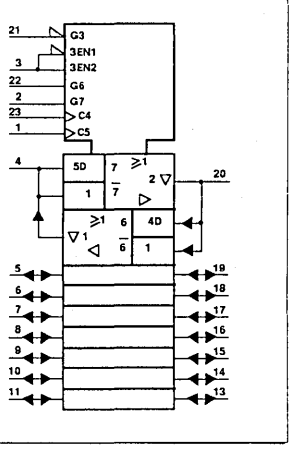
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



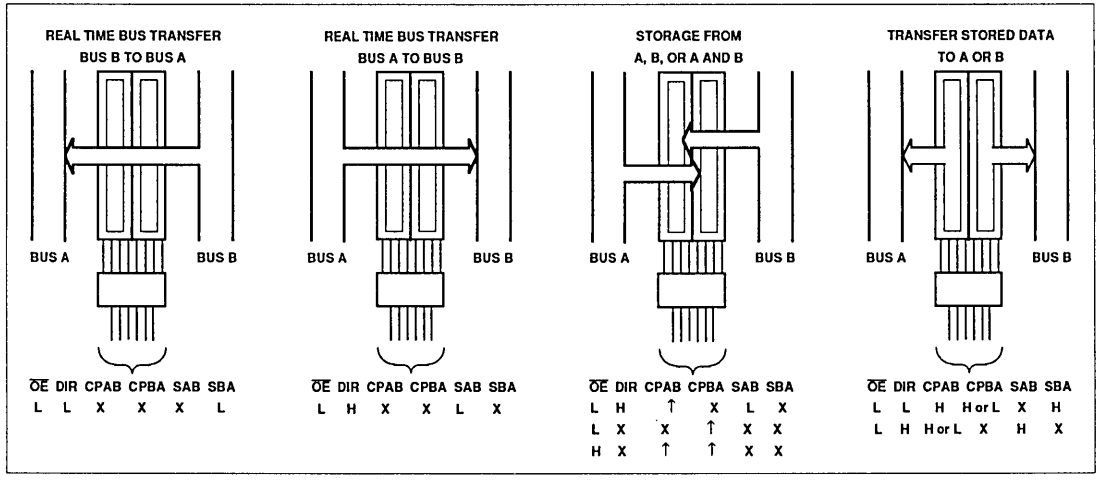
Octal bus transceiver/register (3-State) 74ABT646

FUNCTION TABLE

INPUTS						DATA I/O		OPERATING MODE
$\overline{OE}$	DIR	CPAB	CPBA	SAB	SBA	A_0-A_7	B_0-B_7	
X	X	↑	X	X	X	Input	Unspecified*	Store A, B unspecified*
X	X	X	↑	X	X	Unspecified*	Input	Store B, A unspecified*
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	H or L	H or L	X	X			Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real time B data to A bus
L	L	X	H or L	X	H			Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real time A data to B bus
L	H	H or L	X	H	X			Stored A data to B bus

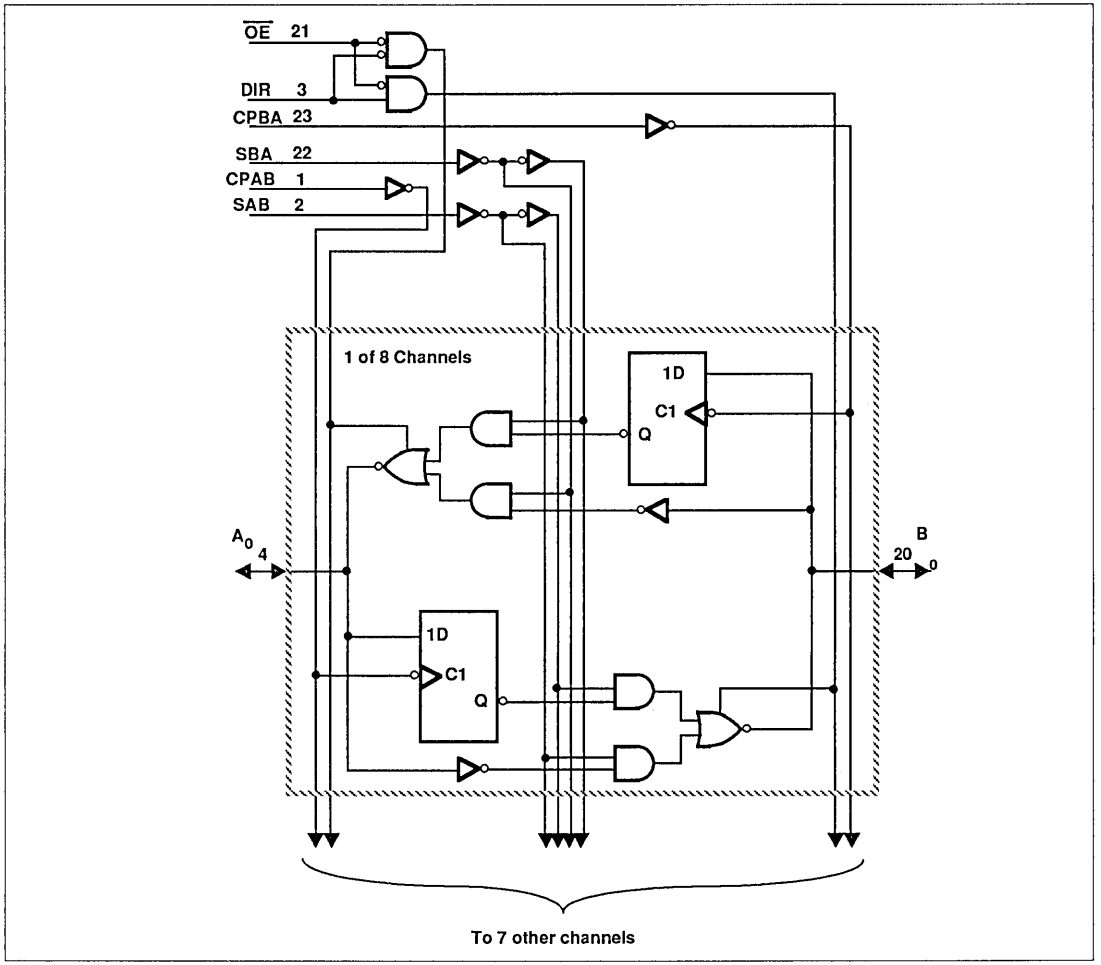
H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-toHigh clock transition
* = The data output function may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled,i.e., data at the bus pins will be stored on every Low-toHigh transition of the clock.

The select (SAB, SBA) pins determine whether data is stored or transfered through the device in real-time. The DIR determines which bus will receive data when the $\overline{OE}$ is active Low. In the isolation mode ($\overline{OE}$ = High), data from Bus A may be stored in the B register and/or data from Bus B may be stored in the A register. When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two busses, A or B may be driven at a time. The following examples demonstrate the four fundamental bus management functions that can be performed with the 74ABT646.



Octal bus transceiver/register (3-State) 74ABT646

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[2]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_O	DC output voltage[2]	output in Off or High state	-0.5 to +5.5	V
I_O	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

Octal bus transceiver/register (3-State) 74ABT646

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = -18mA			-1.2		-1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5			2.5		V
		V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0			3.0		
		V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
$I_{IH} + I_{OZH}$	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
$I_{IL} + I_{OZL}$	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]	V_{CC} = 5.5V; V_O = 2.5V	-50	-100	-180	-50	-180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		24	30		30	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]	Outputs enabled, one input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA
		Outputs 3-State, one data input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	50		50	µA
		Outputs 3-State, one enable input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

Document No.	
ECN No.	
Date of Issue	November 21, 1989
Status	Objective Specification
Advanced BiCMOS Products	

74ABT648

Octal bus transceiver/register, inverting (3-State)

FEATURES

- Combines 74ABT245 and 74ABT374 type functions in one device
- Independent registers for A and B buses
- Multiplexed real-time and stored data
- Output capability: +64 mA/-32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The 74ABT648 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT648 Transceiver/Register consists of bus transceiver circuits with Inverting 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes High. Output Enable ($\overline{OE}$) and DIR pins are provided to control the transceiver function. In the transceiver mode, data present at the

(continued)

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay A_n to B_n, or B_n to A_n	C_L = 50pF; V_{CC} = 5V	5.4	ns
C_{IN}	Input capacitance CP, S, $\overline{OE}$, DIR	V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	I/O capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

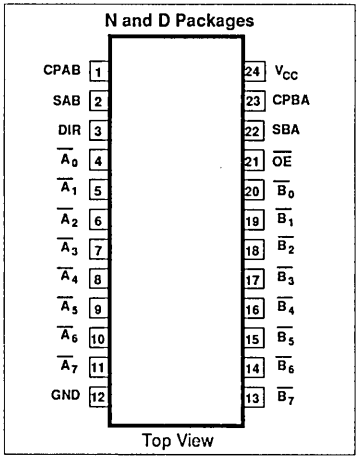
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP (300mil)	-40°C to +85°C	74ABT648N
24-pin plastic SOL (300mil)	-40°C to +85°C	74ABT648D

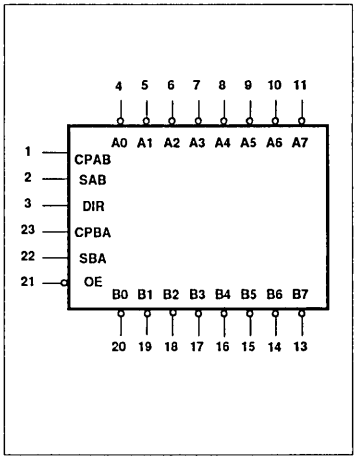
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1,23	CPAB / CPBA	Clock input A to B / Clock input B to A
2, 22	SAB / SBA	Select input A to B / Select input B to A
3	DIR	Direction control input
4, 5, 6, 7 8, 9, 10, 11	$\overline{A}_0$ - $\overline{A}_7$	Data inputs/outputs (A side)
20, 19, 18, 17 16, 15, 14, 13	$\overline{B}_0$ - $\overline{B}_7$	Data inputs/outputs (B side)
21	$\overline{OE}$	Ouput enable input
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

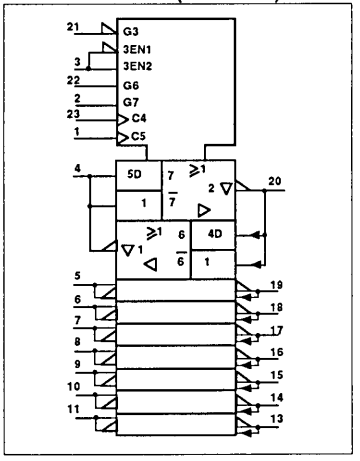
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)



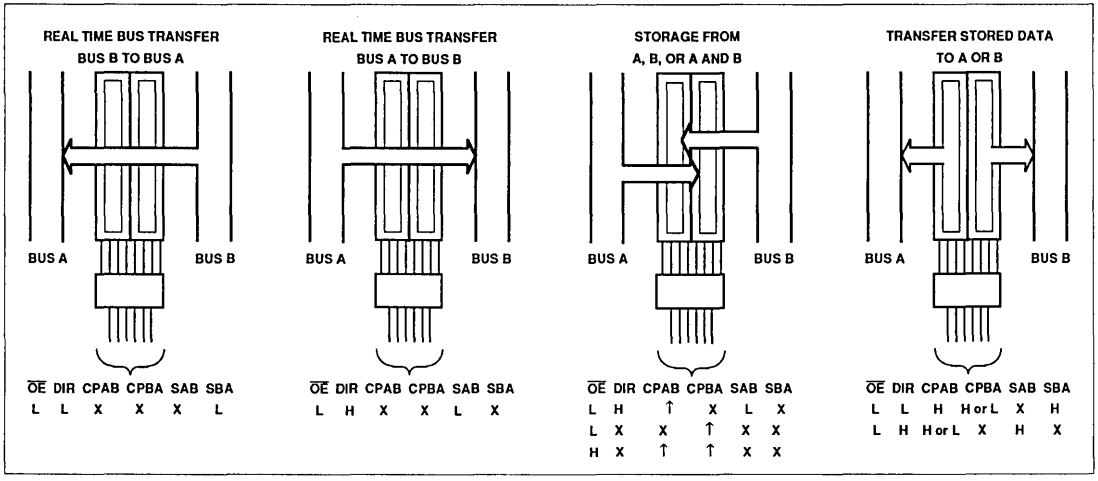
Octal bus transceiver/register, inverting (3-State) 74ABT648

FUNCTION TABLE

INPUTS						DATA I/O		OPERATING MODE
OE	DIR	CPAB	CPBA	SAB	SBA	A_0-A_7	B_0-B_7	
X	X	↑	X	X	X	Input	Unspecified*	Store A, B unspecified*
X	X	X	↑	X	X	Unspecified*	Input	Store B, A unspecified*
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	H or L	H or L	X	X			Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real time $\overline{B}$ data to A bus
L	L	X	H or L	X	H			Stored $\overline{B}$ data to A bus
L	H	X	X	L	X	Input	Output	Real time $\overline{A}$ data to B bus
L	H	H or L	X	H	X			Stored $\overline{A}$ data to B bus

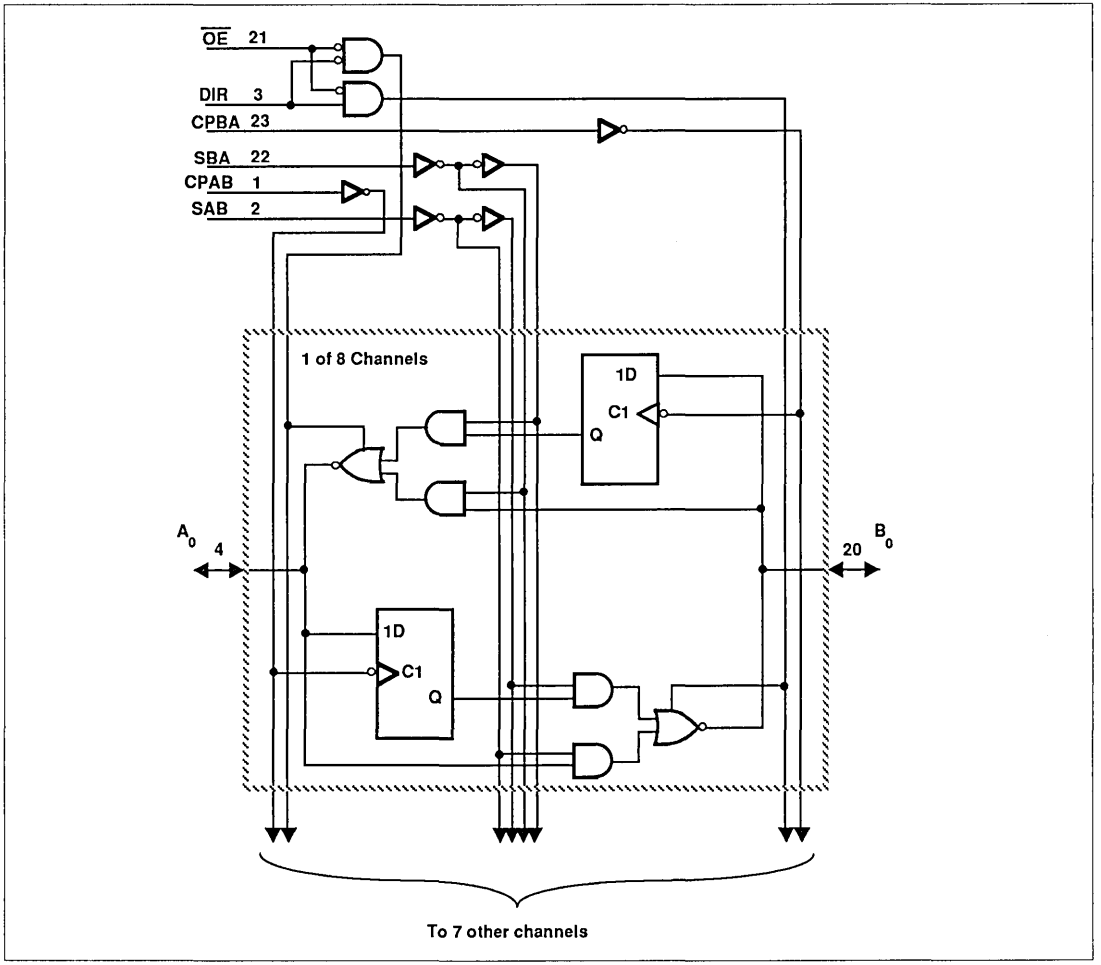
H = High voltage level
L = Low voltage level
X = Don't care
↑ = Low-toHigh clock transition
* = The data output function may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enabled,i.e., data at the bus pins will be stored on every Low-toHigh transition of the clock.

The select (SAB, SBA) pins determine whether data is stored or transfered through the device in real-time. The DIR determines which bus will receive data when the $\overline{OE}$ is active Low. In the isolation mode ($\overline{OE}$ = High), data from Bus A may be stored in the B register and/or data from Bus B may be stored in the A register. Outputs from real-time, or stored register will be inverted. When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two busses, A or B may be driven at a time. The following examples demonstrate the four fundamental bus management functions that can be performed with the 74ABT648.



Octal bus transceiver/register, inverting (3-State) 74ABT648

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[2]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_O	DC output voltage[2]	output in Off or High state	-0.5 to +5.5	V
I_O	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

Octal bus transceiver/register, inverting (3-State) 74ABT648

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = -18mA			-1.2		-1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5			2.5		V
		V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0			3.0		
		V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
$I_{IH} + I_{OZH}$	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
$I_{IL} + I_{OZL}$	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]	V_{CC} = 5.5V; V_O = 2.5V	-50	-100	-180	-50	-180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		24	30		30	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]	Outputs enabled, one input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA
		Outputs 3-State, one data input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	50		50	µA
		Outputs 3-State, one enable input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

Document No.	
ECN No.	
Date of Issue	November 22, 1989
Status	Objecctive Specification
Advanced BiCMOS Products	

74ABT651

Transceiver/register, inverting (3-State)

FEATURES

- Independent registers for A and B buses
- The 74ABT651 is the inverting version of the 74ABT652.
- Multiplexed real-time and stored data
- 3-state outputs
- Output capability: +64 mA/-32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The 74ABT651 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT651 Transceiver/ Register consists of bus transceiver circuits with 3-state, inverting outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes High. Output Enable (OEAB, $\overline{OEBA}$) and Select (SAB, SBA) pins are provided for bus management.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CPAB or CPBA to A_n or B_n	C_L = 50pF; V_{CC} = 5V	5.4	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

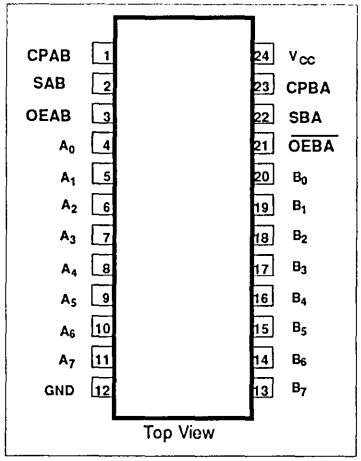
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP (300mil)	-40°C to +85°C	74ABT651N
24-pin plastic SOL (300mil)	-40°C to +85°C	74ABT651D

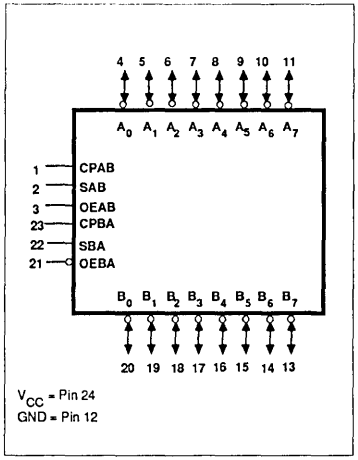
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 23	CPAB / CPBA	Clock input A to B / Clock input B to A
2, 22	SAB / SBA	Select input A to B / Select input B to A
3, 21	OEAB / $\overline{OEBA}$	Output enable inputs
4, 5, 6, 7 8, 9, 10, 11	A_0 - A_7	Data inputs/outputs (A side)
20, 19, 18, 17 16, 15, 14, 13	B_0 - B_7	Data inputs/outputs (B side)
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

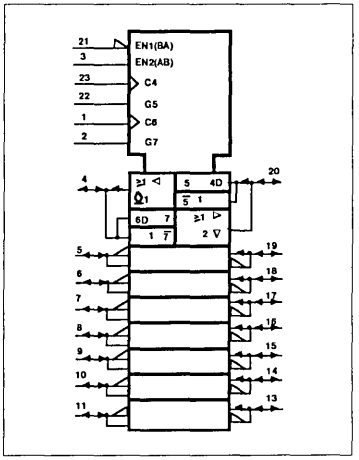
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



Transceiver/register, inverting (3-State) 74ABT651

FUNCTION TABLE

INPUTS			DATA I/O		OPERATING MODE
OEAB $\overline{OEBA}$	CPAB CPBA	SAB SBA	An	Bn	
L H L H	H or L H or L ↑ ↑	X X X X	Input	Input	Isolation Store A and B data
X H H H	↑ H or L ↑ ↑	X X ** X	Input	Unspecified output *	Store A, Hold B Store A in both registers
L X L L	H or L ↑ ↑ ↑	X X X **	Unspecified output *	Input	Hold A, Store B Store B in both registers
L L L L	X X X H or L	X L X H	Output	Input	Real time $\overline{B}$ data to A bus Stored $\overline{B}$ data to A bus
H H H H	X X H or L X	L X H X	Input	Output	Real time $\overline{A}$ data to B bus Store $\overline{A}$ data to B bus
H L	H or L H or L	H H	Output	Output	Stored $\overline{A}$ data to B bus Stored $\overline{B}$ data to A bus

H= High voltage level

L= Low voltage level

*= The data output function may be enabled or disabled by various signals at the $\overline{OEBA}$ and OEAB inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every Low-to-High transition of the clock.

↑ =Low-to-High clock transition

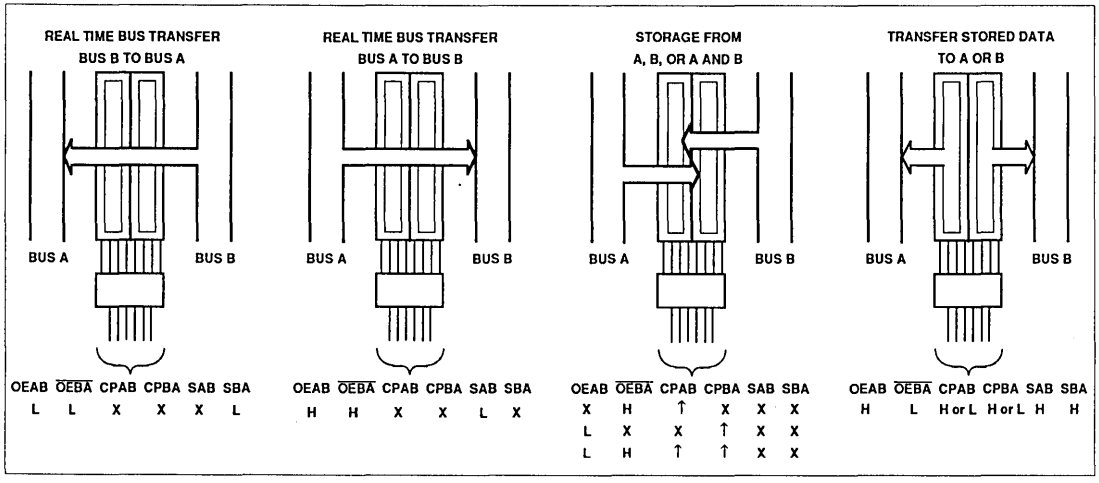
X=Don't care

** If Select control = L, then clocks can occur simultaneously. If Select control = H, the clocks must be staggered in order to load both registers.

The following examples demonstrate the four fundamental bus-management functions that can be performed with the 'ABT651.

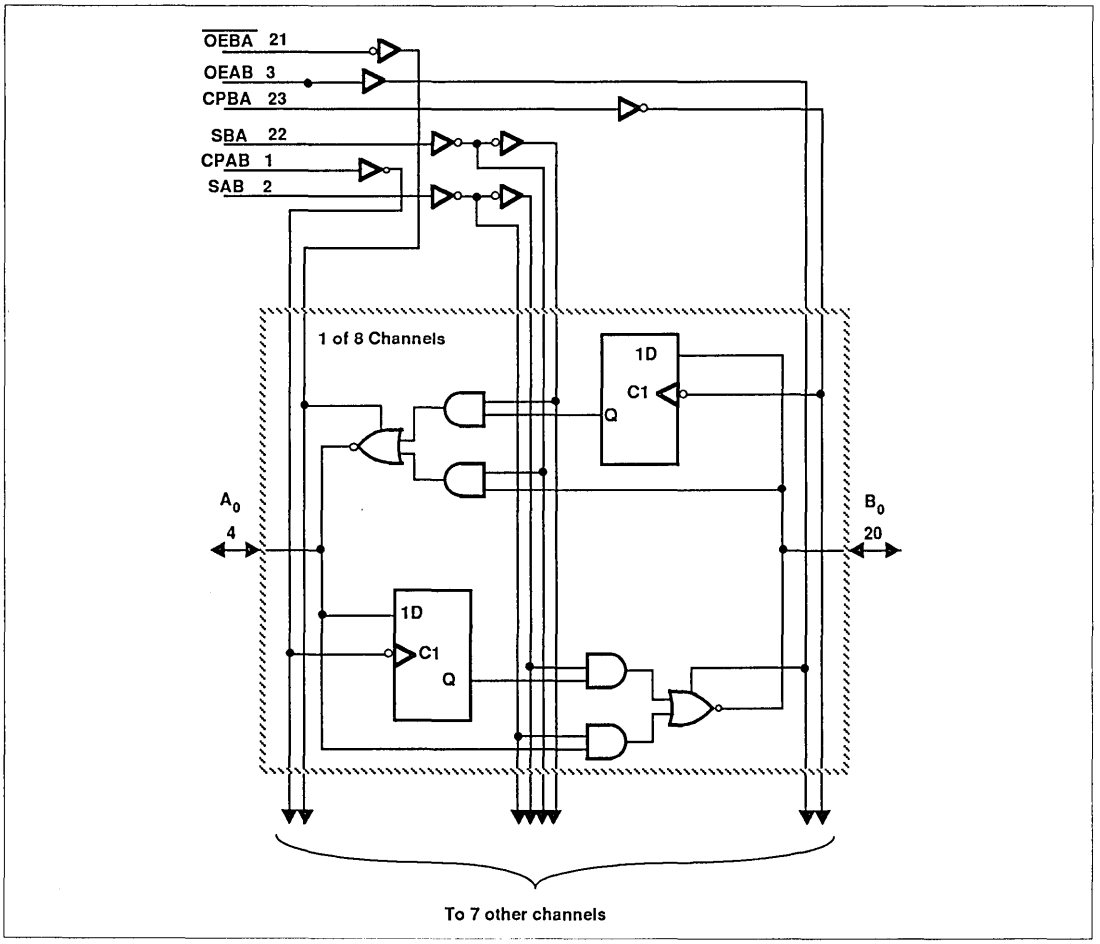
The select pins determine whether data is stored or transferred through the device in real time.

The output enable pins determine the direction of the data flow.



Transceiver/register, inverting (3-State) 74ABT651

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[2]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_O	DC output voltage[2]	output in Off or High state	-0.5 to +5.5	V
I_O	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

Transceiver/register, inverting (3-State) 74ABT651

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = -18mA			-1.2		-1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5			2.5		V
		V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0			3.0		
		V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
$I_{IH} + I_{OZH}$	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
$I_{IL} + I_{OZL}$	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]	V_{CC} = 5.5V; V_O = 2.5V	-50	-100	-180	-50	-180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		24	30		30	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]	Outputs enabled, one input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA
		Outputs 3-State, one data input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	50		50	µA
		Outputs 3-State, one enable input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

Document No.	
ECN No.	
Date of Issue	November 22, 1989
Status	Objective Specification
Advanced BiCMOS Products	

74ABT652

Transceiver/register, non-inverting (3-State)

FEATURES

- Independent registers for A and B buses
- Multiplexed real-time and stored data
- 3-state outputs
- Output capability: +64 mA/-32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The 74ABT652 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT652 Transceiver/ Register consists of bus transceiver circuits with 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes High. Output Enable (OEAB, $\overline{OEBA}$) and Select (SAB, SBA) pins are provided for bus management.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CPAB or CPBA to A_n or B_n	C_L = 50pF; V_{CC} = 5V	5.4	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

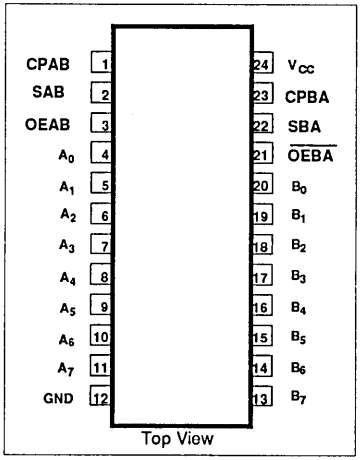
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP (300mil)	-40°C to +85°C	74ABT652N
24-pin plastic SOL (300mil)	-40°C to +85°C	74ABT652D

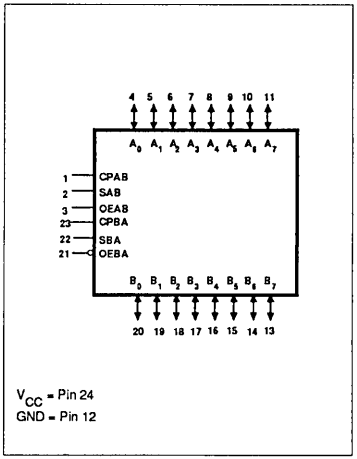
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 23	CPAB / CPBA	Clock input A to B / Clock input B to A
2, 22	SAB / SBA	Select input A to B / Select input B to A
3, 21	OEAB / $\overline{OEBA}$	Output enable inputs
4, 5, 6, 7 8, 9, 10, 11	A_0 - A_7	Data inputs/outputs (A side)
20, 19, 18, 17 16, 15, 14, 13	B_0 - B_7	Data inputs/outputs (B side)
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

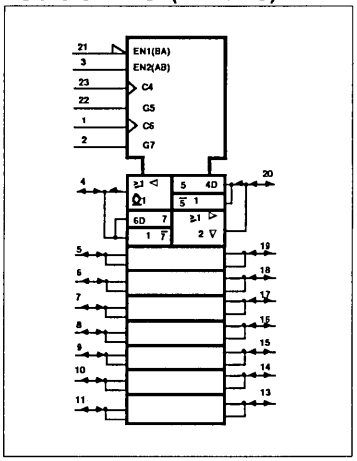
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



Transceiver/register, non-inverting (3-State) 74ABT652

FUNCTION TABLE

INPUTS			DATA I/O		OPERATING MODE
OEAB $\overline{OEBA}$	CPAB CPBA	SAB SBA	An	Bn	
L H L H	H or L H or L ↑ ↑	X X X X	Input	Input	Isolation Store A and B data
X H H H	↑ H or ↑ L ↑	X X ** X	Input	Unspecified output *	Store A, Hold B Store A in both registers
L X L L	H or L ↑ ↑ ↑	X X X **	Unspecified output *	Input	Hold A, Store B Store B in both registers
L L L L	X X X H or L	X L X H	Output	Input	Real time B data to A bus Stored B data to A bus
H H H H	X X H or L X	L X H X	Input	Output	Real time A data to B bus Store A data to B bus
H L	H or L H or L	H H	Output	Output	Stored A data to B bus Stored B data to A bus

H= High voltage level

L= Low voltage level

*= The data output function may be enabled or disabled by various signals at the $\overline{OEBA}$ and OEAB inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every Low-to-High transition of the clock.

↑ =Low-to-High clock transition

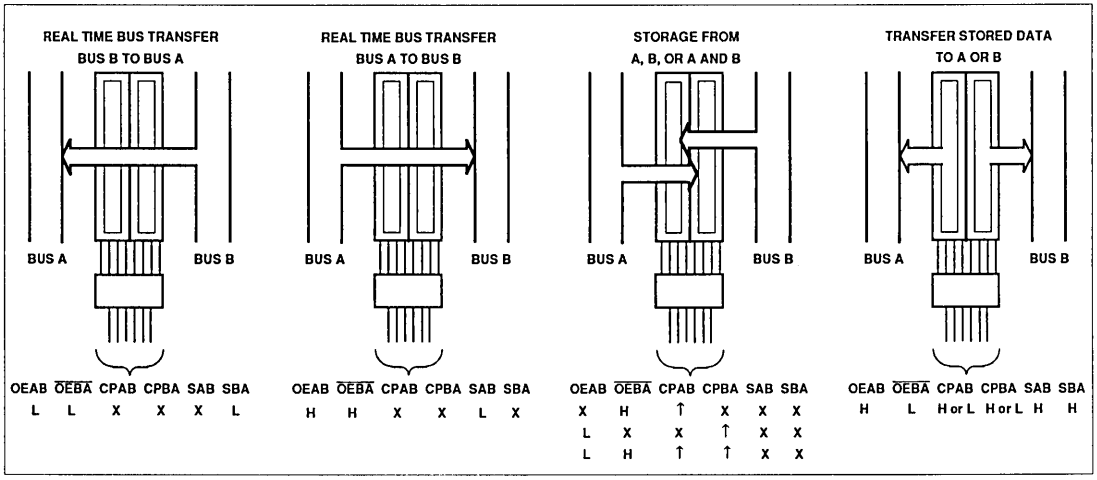
X=Don't care

** If Select control = L, then clocks can occur simultaneously. If Select control = H, the clocks must be staggered in order to load both registers.

The following examples demonstrate the four fundamental bus-management functions that can be performed with the 74ABT652.

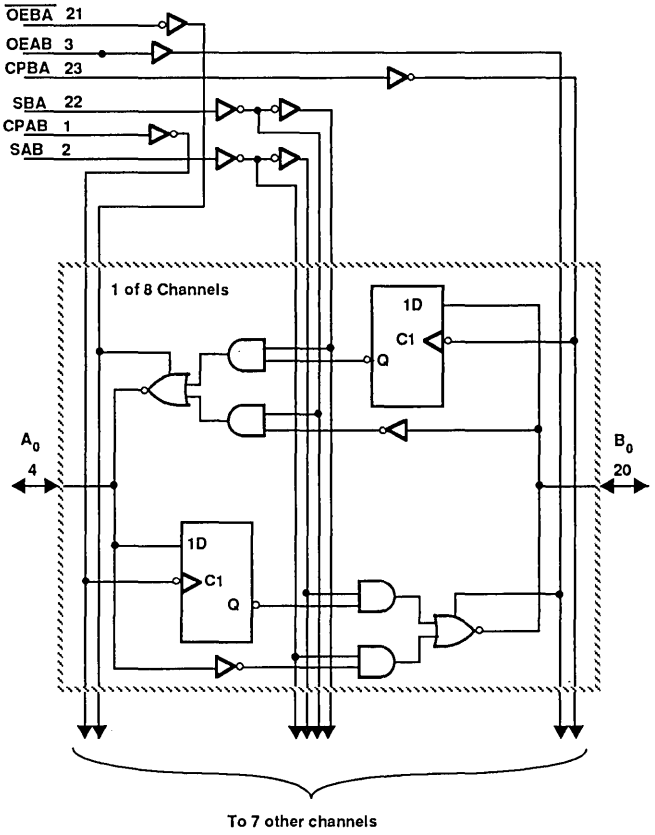
The select pins determine whether data is stored or transferred through the device in real time.

The output enable pins determine the direction of the data flow.



Transceiver/register, non-inverting (3-State) 74ABT652

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[2]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_O	DC output voltage[2]	output in Off or High state	-0.5 to +5.5	V
I_O	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

Transceiver/register, non-inverting (3-State) 74ABT652

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = -18mA			-1.2		-1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5			2.5		V
		V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0			3.0		
		V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
$I_{IH} + I_{OZH}$	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
$I_{IL} + I_{OZL}$	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]	V_{CC} = 5.5V; V_O = 2.5V	-50	-100	-180	-50	-180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		24	30		30	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]	Outputs enabled, one input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA
		Outputs 3-State, one data input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	50		50	µA
		Outputs 3-State, one enable input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

Document No.	
ECN No.	
Date of Issue	November 21, 1989
Status	Objective Specification
Advanced BiCMOS Products	

74ABT657

Octal transceiver with 8-bit parity generator/checker (3-State)

FEATURES

- Combinational functions in one package
- Low static and dynamic power dissipation with high speed and high output drive
- Output capability: +64 mA/-32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay A_n to B_n or B_n to A_n	C_L = 50pF; V_{CC} = 5V	2.9	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP (300mil)	-40°C to +85°C	74ABT657N
24-pin plastic SOL (300mil)	-40°C to +85°C	74ABT657D

DESCRIPTION

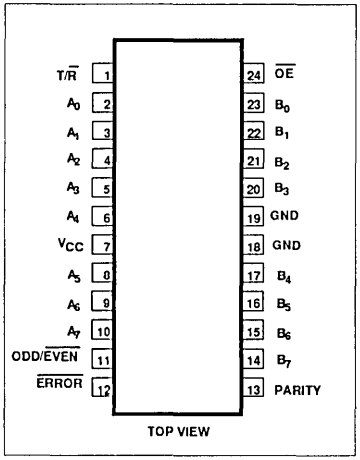
The 74ABT657 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT657 is an octal transceiver featuring non-inverting buffers with 3-state outputs and an 8-bit parity generator/checker, and is intended for bus-oriented applications. The buffers have a guaranteed current sinking capability of 64mA. The Transmit/Receive ($T/\overline{R}$) input determines the direction of the data flow through the bidirectional transceivers. Transmit (active-High) enables data from A ports to B ports; Receive (active-Low) enables data from B ports to A ports.

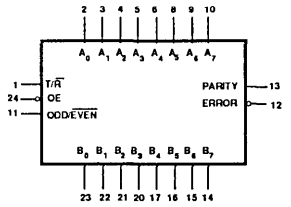
The Output Enable ($\overline{OE}$) input disables both the A and B ports by placing them in a high impedance condition when the $\overline{OE}$ input is High. The parity select (ODD/$\overline{EVEN}$) input gives the user the option of odd or even parity systems. The parity (PARITY) pin is an output from the generator/checker when transmitting from the port A to B ($T/\overline{R}$=High) and an input when receiving from port B to A port ($T/\overline{R}$=Low). When transmitting ($T/\overline{R}$=High) the parity select (ODD/$\overline{EVEN}$) input is set, then the A port data is polled to determine the number of High bits. The parity (PARITY) output then goes to the logic state determined by the parity select (ODD/$\overline{EVEN}$) setting and by the number of High bits on port A. For example, if the parity select (ODD/$\overline{EVEN}$) is set Low (even parity), and the number of High bits on port A is odd, then the parity (PARITY) output will be High, transmitting even parity. If

(Continued on next page)

PIN CONFIGURATION

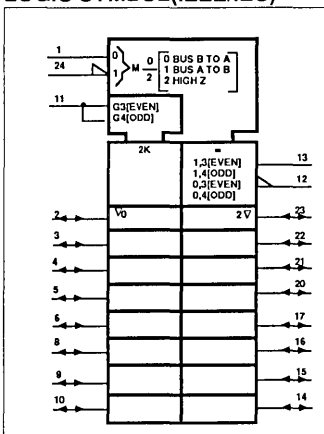


LOGIC SYMBOL



V_{CC} = Pin 7
GND = Pin 18, 19

LOGIC SYMBOL(IEEE/IEC)



Octal Transceiver with Parity Generator/Checker (3-State) 74ABT657

the number of High bits on port A is even, then the parity (PARITY) output will be Low, keeping even parity. When in receive mode (T/$\overline{R}$=Low) the B port is polled to determine the number of High bits. If parity select (ODD/$\overline{EVEN}$) is Low (even parity) and the number of Highs on port B is:

(1) odd and the parity (PARITY) input is High, then $\overline{ERROR}$ will be High, signifying no error.

(2) even and the parity (PARITY) input is High, then $\overline{ERROR}$ will be asserted Low, indicating an error.

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
13	PARITY	Parity output
11	ODD/EVEN	Parity select input
12	$\overline{ERROR}$	Error output
1	T/$\overline{R}$	Transmission/Receive input
2, 3, 4, 5, 6 8, 9, 10	A_0 - A_7	A port 3-State outputs
23, 22, 21, 20 17, 16, 15, 14	B_0 - B_7	B port 3-State outputs
24	$\overline{OE}$	Ouput enable input activelow
18, 19	GND	Ground (0V)
7	V_{CC}	Positive supply voltage

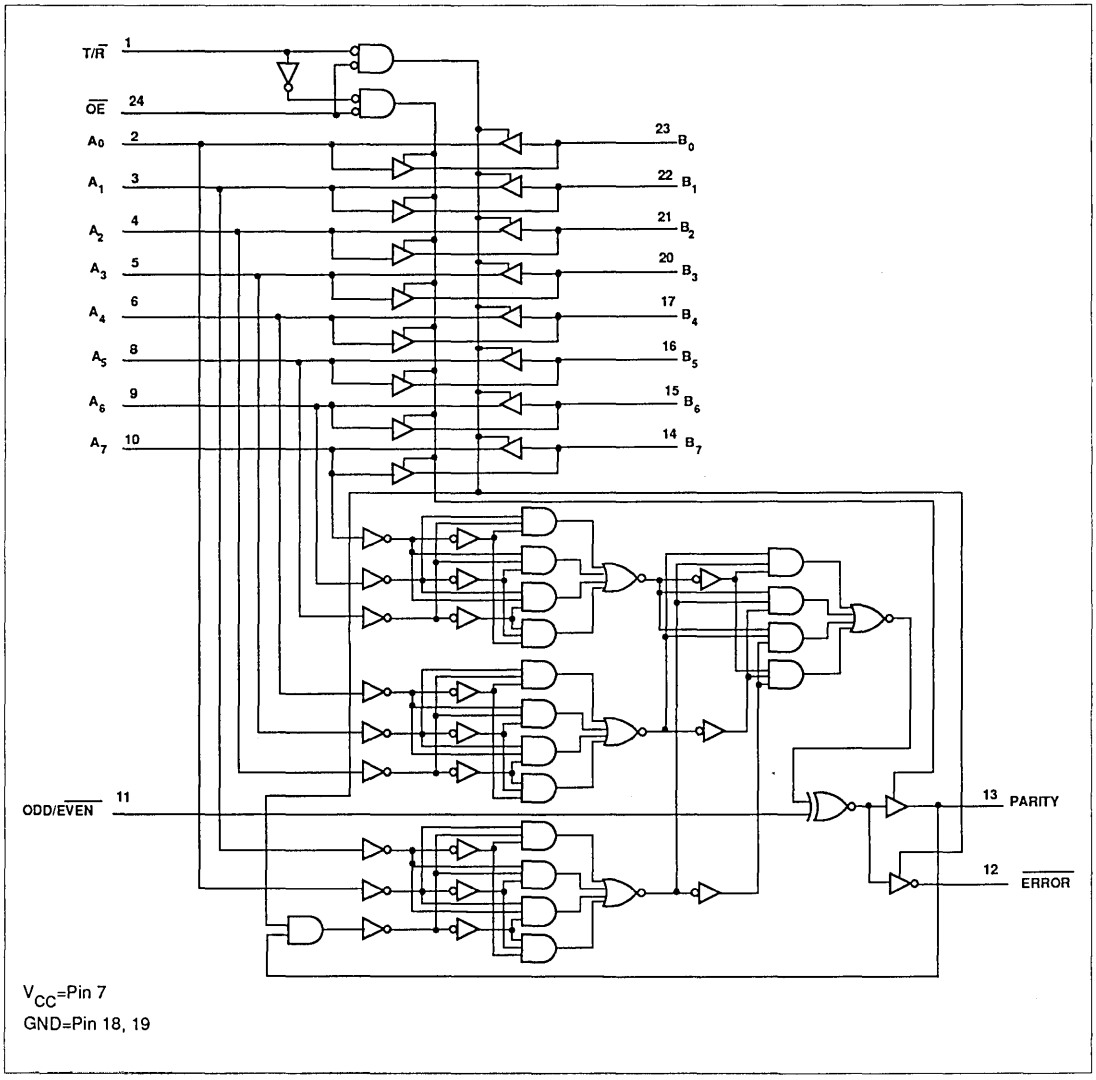
FUNCTION TABLE

NUMBER OF INPUTS THAT ARE HIGH	INPUTS			INPUT/ OUPUT	OUTPUTS	
	$\overline{OE}$	T/$\overline{R}$	ODD/$\overline{EVEN}$	PARITY	$\overline{ERROR}$	OUTPUTS MODE
0, 2, 4, 6, 8	L	H	H	H	Z	Transmit
	L	H	L	L	Z	Transmit
	L	L	H	H	H	Receive
	L	L	H	L	L	Receive
	L	L	L	H	L	Receive
	L	L	L	L	H	Receive
1, 3, 5, 7	L	H	H	L	Z	Transmit
	L	H	L	H	Z	Transmit
	L	L	H	H	L	Receive
	L	L	H	L	H	Receive
	L	L	L	H	H	Receive
	L	L	L	L	L	Receive
Don't care	H	X	X	Z	Z	3-state

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

Octal Transceiver with Parity Generator/Checker (3-State) 74ABT657

LOGIC DIAGRAM



Octal Transceiver with Parity Generator/Checker (3-State) 74ABT657

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[2]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_O	DC output voltage[2]	output in Off or High state	-0.5 to +5.5	V
I_O	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = -18mA			-1.2		-1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5			2.5		V
		V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0			3.0		
		V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{IH} + I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{IL} + I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]	V_{CC} = 5.5V; V_O = 2.5V	-50	-100	-180	-50	-180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		24	30		30	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]	Outputs enabled, one input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA
		Outputs 3-State, one data input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	50		50	µA
		Outputs 3-State, one enable input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

Document No.	
ECN No.	
Date of Issue	November 30, 1989
Status	Objective Specification
Advanced BiCMOS Products	

74ABT821

10-bit D-type flip-flop, positive-edge trigger (3-State)

FEATURES

- High speed parallel registers with positive edge-triggered D-type flip-flops
- Ideal where high speed, light loading, or increased fan-in are required with MOS microprocessors
- Output capability: +64 mA/-32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The 74ABT821 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT821 Bus interface Register is designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider data/address paths of buses carrying parity.

The 'ABT821 is a buffered 10-bit wide version of the 'ABT374/'ABT534 functions.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	C_L = 50pF; V_{CC} = 5V	5.4	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP	-40°C to +85°C	74ABT821N
24-pin plastic SOL	-40°C to +85°C	74ABT821D

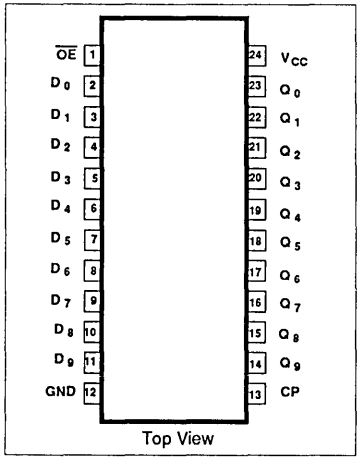
The 'ABT821 is a 10-bit, edge triggered register coupled to ten 3-State output buffers. The two sections of the device are controlled independently by the clock (CP) and Output Enable ($\overline{OE}$) control gates.

The register is fully edge triggered. The state of each D input, one set-up time before the Low-to-High clock transition is transferred to the corresponding flip-flop's Q output.

The 3-State output buffers are designed to drive heavily loaded 3-State buses, MOS memories, or MOS microprocessors.

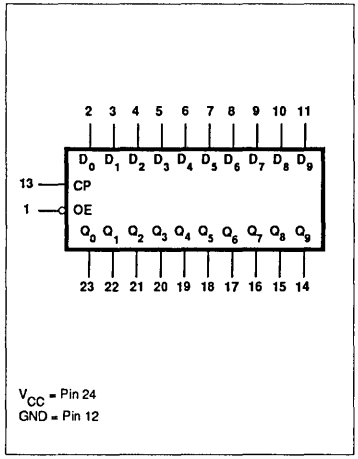
The active Low Output Enable ($\overline{OE}$) controls all ten 3-State buffers independent of the register operation. When $\overline{OE}$ is Low, the data in the register appears at the outputs. When $\overline{OE}$ is High, the outputs are in high impedance "off" state, which means they will neither drive nor load the bus.

PIN CONFIGURATION

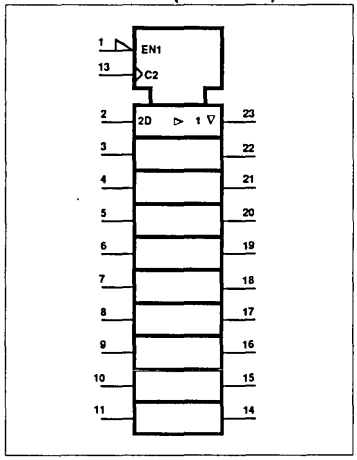


Top View

LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



10-bit D-type flip-flop; positive-edge trigger (3-State) 74ABT821

PIN DESCRIPTION

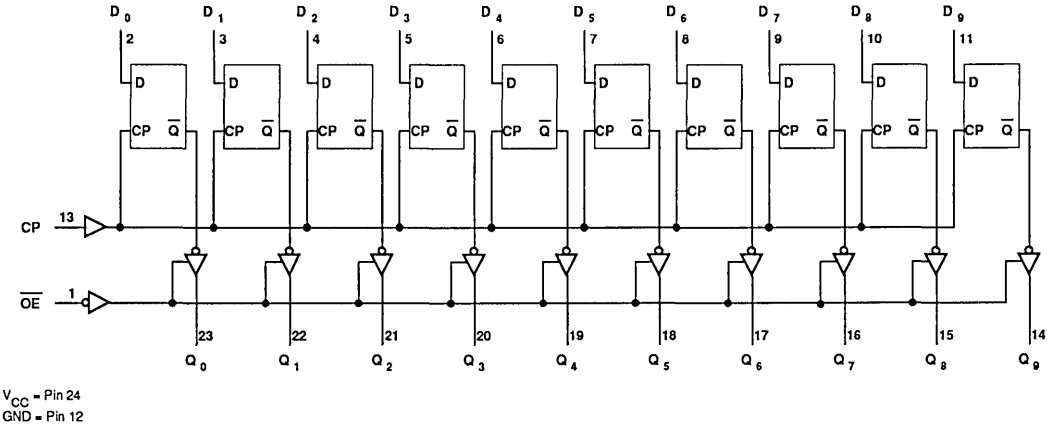
PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	Output Enable input (active Low)
2, 3, 4, 5, 6, 7 8, 9, 10, 11	D_0 - D_9	Data inputs
14, 15, 16, 17, 18, 19, 20, 21, 22, 23	Q_0 - Q_9	Data outputs
13	CP	Clock Pulse input (active rising edge)
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS			INTERNAL	OUTPUTS	OPERATING MODE
$\overline{OE}$	CP	D_n	REGISTER	Q_0 - Q_9	
L L	↑ ↑	l h	L H	L H	Load and read register
L	‡	X	NC	NC	Hold
H H	‡ ↑	X D_n	NC D_n	Z Z	Disable outputs

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
NC = No change
X = Don't care
Z = High impedance "off" state
↑ = Low-to-High clock transition
‡ = Not a Low-to-High clock transition

LOGIC DIAGRAM



V_{CC} = Pin 24
GND = Pin 12

10-bit D-type flip-flop; positive-edge trigger (3-State) 74ABT821

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[2]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_O	DC output voltage[2]	output in Off or High state	-0.5 to +5.5	V
I_O	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

10-bit D-type flip-flop; positive-edge trigger (3-State) 74ABT821

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = -18mA			-1.2		-1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5			2.5		V
		V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0			3.0		
		V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]	V_{CC} = 5.5V; V_O = 2.5V	-50	-100	-180	-50	-180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		24	30		30	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5V; One input at 3.4V, other inputs at V_{CC} or GND		0.5	1.5		1.5	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

Document No.	
ECN No.	
Date of Issue	November 30, 1989
Status	Objective Specification
Advanced BiCMOS Products	

74ABT823

9-bit D-type flip-flop; with reset and enable (3-State)

FEATURES

- High speed parallel registers with positive edge-triggered D-type flip-flops
- Ideal where high speed, light loading, or increased fan-in are required with MOS microprocessors
- Output capability: +64 mA/-32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The 74ABT823 Bus interface Register is designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider data/address paths of buses carrying parity.

The 'ABT823 is a 9-bit wide buffered register with Clock Enable ($\overline{CE}$) and Master Reset ($\overline{MR}$) which are ideal for parity bus interfacing in high microprogrammed systems.

The register is fully edge triggered. The state of each D input, one set-up time before the Low-to-High clock transition is transferred to the corresponding flip-flop's Q output.

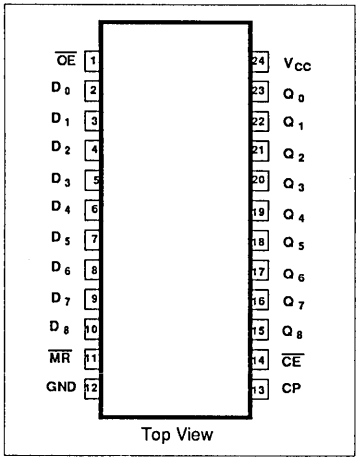
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	C_L = 50pF; V_{CC} = 5V	5.4	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

ORDERING INFORMATION

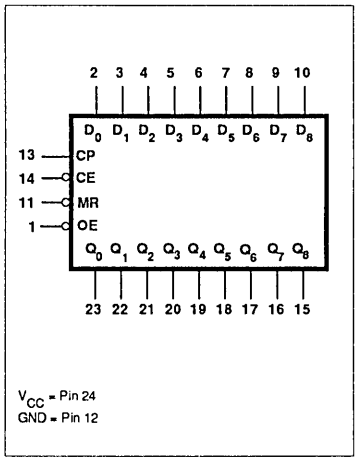
PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP	-40°C to +85°C	74ABT823N
24-pin plastic SOL	-40°C to +85°C	74ABT823D

PIN CONFIGURATION



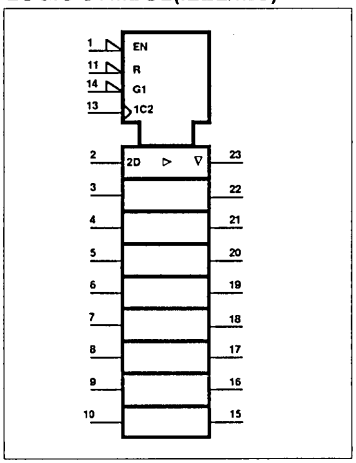
Top View

LOGIC SYMBOL



V_{CC} = Pin 24
GND = Pin 12

LOGIC SYMBOL(IEEE/IEC)



9-bit D-type flip-flop with reset and enable; (3-State) 74ABT823

PIN DESCRIPTION

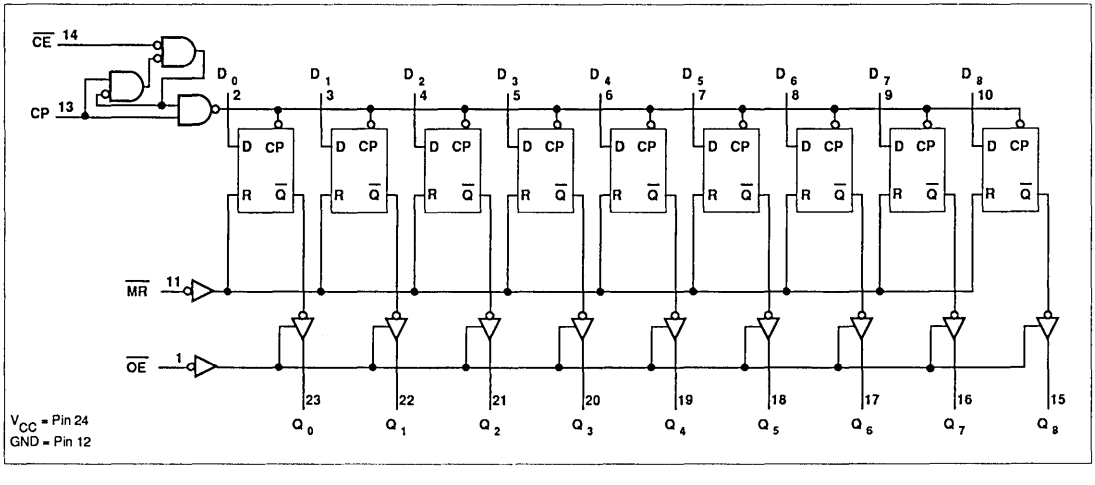
PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	Output Enable input (active Low)
2, 3, 4, 5, 6, 7 8, 9, 10	D_0 - D_8	Data inputs
15, 16, 17, 18 19, 20, 21, 22, 23	Q_0 - Q_8	Data outputs
13	CP	Clock Pulse input (active rising edge)
14	$\overline{CE}$	Clock Enable input (active Low)
11	$\overline{MR}$	Master Reset input (active Low)
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

FUNCTION TABLE

INPUTS					OUTPUTS	OPERATING MODE
$\overline{OE}$	$\overline{MR}$	$\overline{CE}$	CP	D_n	Q_0 - Q_8	
L	L	X	X	X	L	Clear
L	H	L	↑	h	H	Load and read data
L	H	L	↑	l	L	
L	H	H	↧	X	NC	Hold
H	X	X	X	X	Z	High impedance

H = High voltage level
h = High voltage level one set-up time prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one set-up time prior to the Low-to-High clock transition
NC = No change
X = Don't care
Z = High impedance "off" state
↑ = Low-to-High clock transition
↧ = Not a Low-to-High clock transition

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[2]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_O	DC output voltage[2]	output in Off or High state	-0.5 to +5.5	V
I_O	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

9-bit D-type flip-flop with reset and enable; (3-State) 74ABT823

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = -18mA			-1.2		-1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5			2.5		V
		V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0			3.0		
		V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]	V_{CC} = 5.5V; V_O = 2.5V	-50	-100	-180	-50	-180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		24	30		30	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5V; One input at 3.4V, other inputs at V_{CC} or GND		0.5	1.5		1.5	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

Document No.	
ECN No.	
Date of Issue	November 30, 1989
Status	Objective Specification
Advanced BiCMOS Products	

74ABT827

10-bit buffer/line driver, non-inverting (3-State)

FEATURES

- Ideal where high speed, light bus loading and increased fan-in are required
- Flow through pinout architecture for microprocessor oriented applications
- Outputs capability: +64mA/-32mA
- Slim 300 mil-wide plastic 24-pin package
- Pinout and function compatible with AMD 29827

DESCRIPTION

The 74ABT827 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT827 10-bit buffers provide high performance bus interface buffering for wide data/address paths or buses carrying parity. They have NOR Output Enables ($\overline{OE}_0$, $\overline{OE}_1$) for maximum control flexibility.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CP to Q_n	C_L = 50pF; V_{CC} = 5V	2.9	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

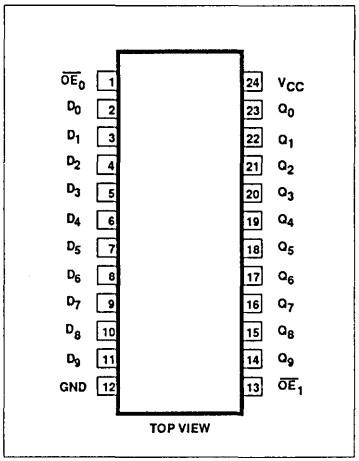
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP	-40°C to +85°C	74ABT827N
24-pin plastic SOL	-40°C to +85°C	74ABT827D

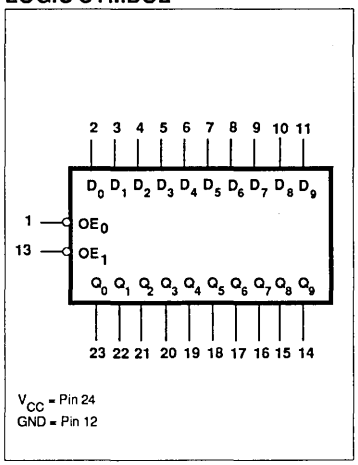
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 13	$\overline{OE}_0$, $\overline{OE}_1$	Output Enable inputs (active Low)
2, 3, 4, 5, 6, 7 8, 9, 10, 11	D_0 - D_9	Data inputs
14, 15, 16, 17, 18 19, 20, 21, 22, 23	Q_0 - Q_9	Data outputs
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

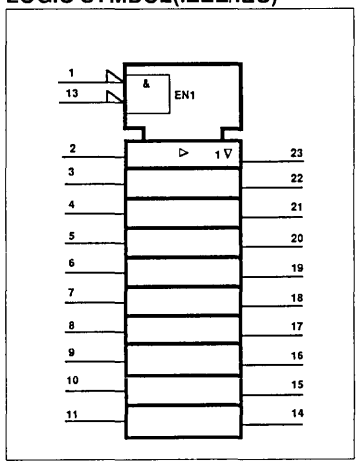
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



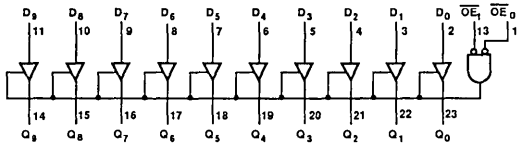
10-bit buffer/line driver, non-inverting (3-State) 74ABT827

FUNCTION TABLE

INPUTS		OUTPUTS	OPERATING MODE
$\overline{OE}_n$	D_n	Q_n	
L	L	L	Transparent
L	H	H	Transparent
H	X	Z	High impedance

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

LOGIC DIAGRAM



RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

10-bit buffer/line driver, non-inverting (3-State) 74ABT827

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[2]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_O	DC output voltage[2]	output in Off or High state	-0.5 to +5.5	V
I_O	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = -18mA			-1.2		-1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5			2.5		V
		V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0			3.0		
		V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]	V_{CC} = 5.5V; V_O = 2.5V	-50	-100	-180	-50	-180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		24	30		30	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]	Outputs enabled, one input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA
		Outputs 3-State, one data input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	50		50	µA
		Outputs 3-State, one enable input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

Philips Components—Signetics

Document No.	
ECN No.	
Date of Issue	November 30, 1989
Status	Objective Specification
Advanced BiCMOS Products	

74ABT841

10-bit bus interface latch (3-State)

FEATURES

- High speed parallel latches
- Extra data width for wide address/ data paths or busses carrying parity
- Ideal where high speed, light loading, or increased fan-in are required as with MOS microprocessors
- Output capability: +64mA/-32mA
- Slim Dip 300 mil package
- Broadside pinout
- Pin-for-pin and function compatible with AMD AM29841

DESCRIPTION

The 74ABT841 bus interface latch is designed to provide extra data width for wider address/data paths of busses carrying parity.

The 74ABT841 is functionally, and pin compatible to the AMD AM29841.

The 74ABT841 consists of ten D-type latches with 3-state outputs. The flip-flops appear transparent to the data when Latch Enable (LE) is High. This allows asynchronous operation, as the output transition follows the data in transition. On the LE High-to-Low transition, the data that meets the setup and hold time is latched.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	C_L = 50pF; V_{CC} = 5V	4.0	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

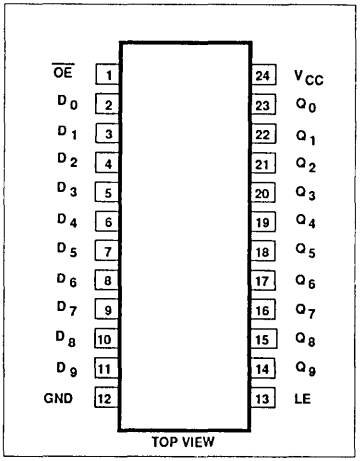
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP	-40°C to +85°C	74ABT841N
24-pin plastic SOL	-40°C to +85°C	74ABT841D

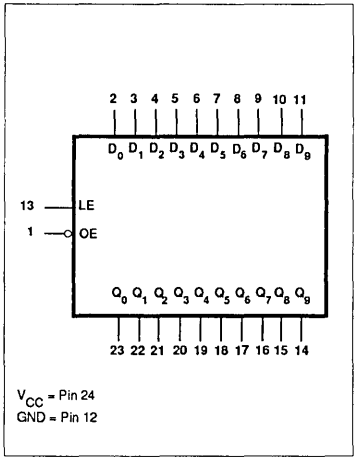
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	Output Enable input (active Low)
2, 3, 4, 5, 6, 7 8, 9, 10, 11	D_0 - D_9	Data inputs
14, 15, 16, 17, 18 19, 20, 21, 22, 23	Q_0 - Q_9	Data outputs
13	LE	Latch Enable input (active falling edge)
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

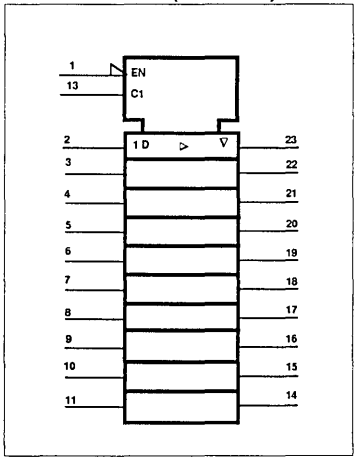
PIN CONFIGURATION



LOGIC SYMBOL

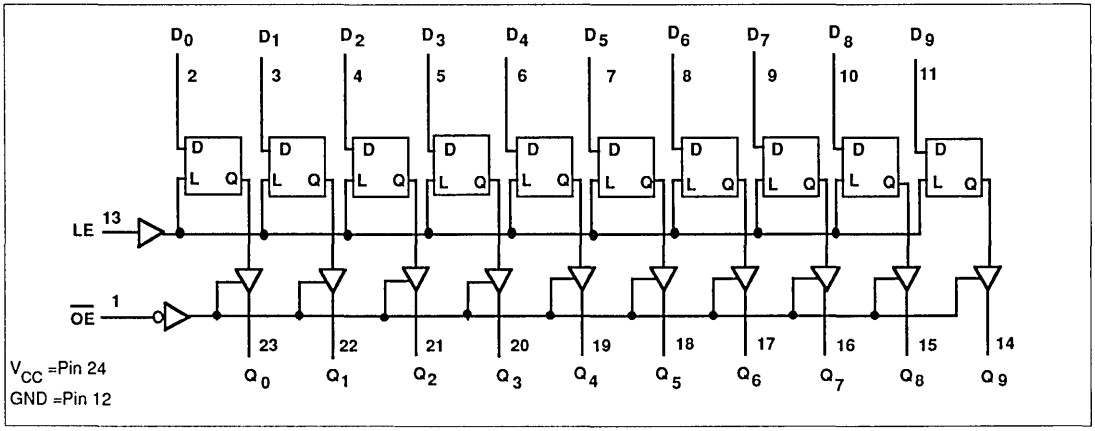


LOGIC SYMBOL(IEEE/IEC)



10-bit bus interface latch (3-State) 74ABT841

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS			OUTPUTS	OPERATING MODE
$\overline{OE}$	LE	D_n	Q_n	
L	H	L	L	Transparent
L	H	H	H	
L	↓	l	L	Latched
L	↓	h	H	
H	X	X	Z	High impedance
L	L	X	NC	Hold

H= High voltage level
L= Low voltage level
h= High state one setup time before the High-to-Low LE transition
l = Low state one setup time before the High-to-Low LE transition
↓ = High-to-Low transition
X=Don't care
NC=No change
Z =High impedance "off" state

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

10-bit bus interface latch (3-State) 74ABT841

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[2]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_O	DC output voltage[2]	output in Off or High state	-0.5 to +5.5	V
I_O	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = -18mA			-1.2		-1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5			2.5		V
		V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0			3.0		
		V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]	V_{CC} = 5.5V; V_O = 2.5V	-50	-100	-180	-50	-180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		24	30		30	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5V; One input at 3.4V, other inputs at V_{CC} or GND		0.5	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

Document No.	
ECN No.	
Date of Issue	November 30, 1989
Status	Objective Specification
Advanced BiCMOS Products	

74ABT843

9-bit bus interface latch with set and reset (3-State)

FEATURES

- High speed parallel latches
- Extra data width for wide address/ data paths or busses carrying parity
- Ideal where high speed, light loading, or increased fan-in are required as with MOS microprocessors
- Output capability: +64mA/-15mA
- Slim Dip 300 mil package
- Broadside pinout
- Pin-for-pin and function compatible with AMD AM29843

DESCRIPTION

The 'ABT843 consists of nine D-type latches with 3-state outputs. In addition to the LE and $\overline{OE}$ pins, the 'ABT843 has a Master Reset ($\overline{MR}$) pin and Preset ($\overline{PRE}$) pin. These pins are ideal for parity bus interfacing in high performance systems. When $\overline{MR}$ is Low, the outputs areLow if $\overline{OE}$ is Low. When $\overline{MR}$ is High, data can be entered ento the latch. When $\overline{PRE}$ os Low, the outputs are High, if $\overline{OE}$ is Low. $\overline{PRE}$ overrides $\overline{MR}$.

The 'ABT843 is functionally, and pin compatible to the AMD AM29843.

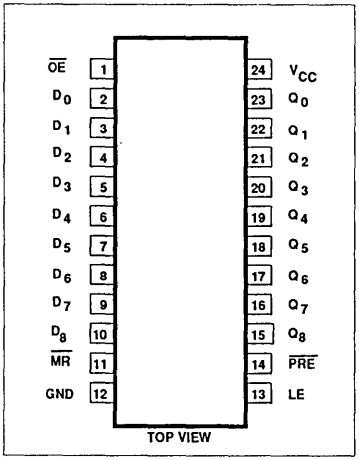
QUICK REFERENCE DATA

SYMBOL	PARAMETE	CONDITIONS $T_A = 25°C$; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	C_L = 50pF; V_{CC} = 5V	4.0	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

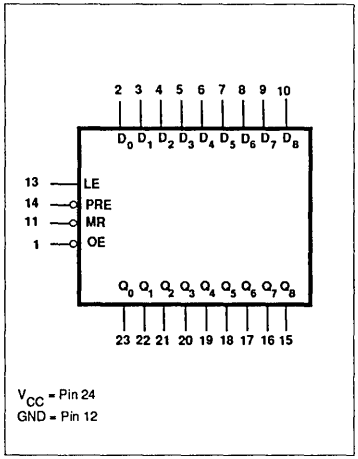
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP	-40°C to +85°C	74ABT843N
24-pin plastic SOL	-40°C to +85°C	74ABT843D

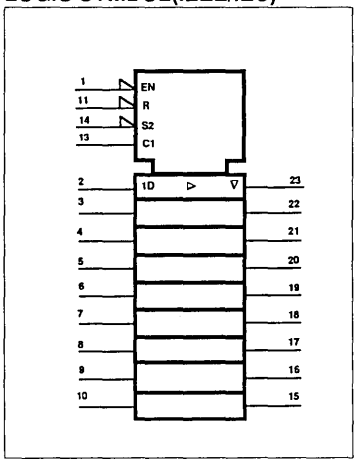
PIN CONFIGURATION



LOGIC SYMBOL

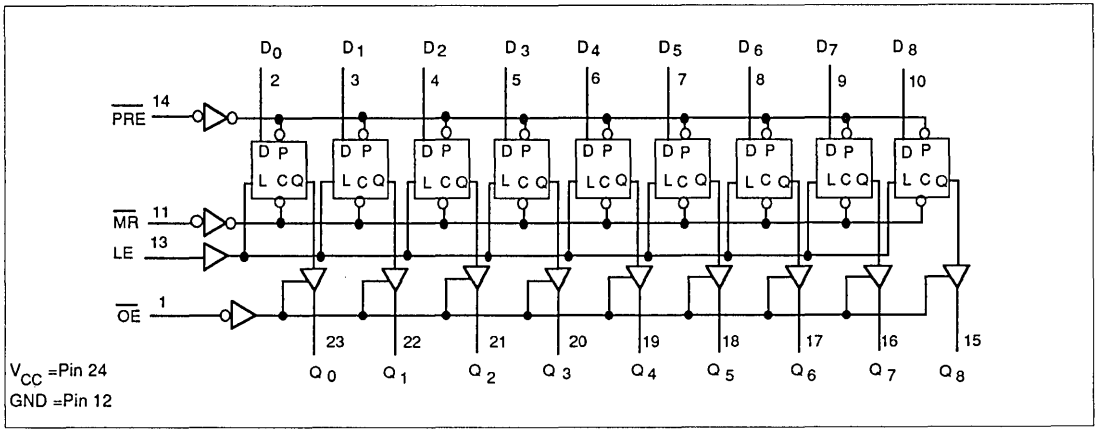


LOGIC SYMBOL(IEEE/IEC)



9-bit bus interface latch with set and reset (3-State) 74ABT843

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS					OUTPUTS	OPERATING MODE
$\overline{OE}$	$\overline{PRE}$	$\overline{MR}$	LE	D_n	Q_n	
L	L	X	X	X	H	Preset
L	H	L	X	X	L	Clear
L	H	H	H	L	L	Transparent
L	H	H	H	H	H	
L	H	H	↓	l	L	Latched
L	H	H	↓	h	H	
H	X	X	X	X	Z	High impedance
L	H	H	L	X	NC	Hold

H= High voltage level
L= Low voltage level
h= High state one setup time before the High-to-Low LE transition
l =Low state one setup time before the High-to-Low LE transition
↓ =High-to-Low transition
X=Don't care
NC=No change
Z =High impedance "off " state

PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	$\overline{OE}$	Output Enable input (active Low)
2, 3, 4, 5, 6 7, 8, 9, 10	D_0 - D_8	Data inputs
15, 16, 17, 18, 19 20, 21, 22, 23	Q_0 - Q_8	Data outputs
11	$\overline{MR}$	Master Reset input (active Low)
13	LE	Latch Enable input (active falling edge)
14	$\overline{PRE}$	Preset input (active Low)
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[2]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_O	DC output voltage[2]	output in Off or High state	-0.5 to +5.5	V
I_O	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

9-bit bus interface latch with set and reset (3-State) 74ABT843

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = -18mA			-1.2		-1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5			2.5		V
		V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0			3.0		
		V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]	V_{CC} = 5.5V; V_O = 2.5V	-50	-100	-180	-50	-180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		24	30		30	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5V; One input at 3.4V, other inputs at V_{CC} or GND		0.5	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

Document No.	
ECN No.	
Date of Issue	November 30, 1989
Status	Objective Specification
Advanced BiCMOS Products	

74ABT845

8-bit bus interface latch with set and reset (3-State)

FEATURES

- High speed parallel latches
- Extra data width for wide address/ data paths or busses carrying parity
- Ideal where high speed, light loading, or increased fan-in are required as with MOS microprocessors
- Output capability: +64mA/-32mA
- Slim Dip 300 mil package
- Broadside pinout
- Pin-for-pin and function compatible with AMD AM29845

DESCRIPTION

The 'ABT845 consists of eight D-type latches with 3-state outputs. In addition to the LE, $\overline{OE}$, $\overline{MR}$ and $\overline{PRE}$ pins, the 'ABT845 has two additional $\overline{OE}$ pins making a total of three Output Enables ($\overline{OE}_0$, $\overline{OE}_1$, $\overline{OE}_2$) pins. The multiple Output Enables ($\overline{OE}_0$, $\overline{OE}_1$, $\overline{OE}_2$) allow multiuser control of the interface, e.g., $\overline{CS}$, DMA, and RD/$\overline{WR}$.

The 'ABT845 is functionally, and pin compatible to the AMD AM29845.

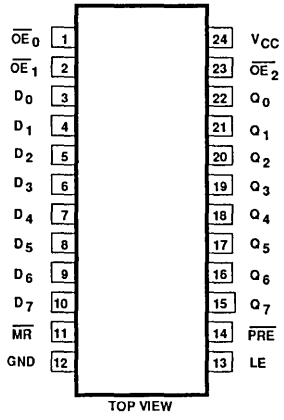
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_A = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n	C_L = 50pF; V_{CC} = 5V	4.0	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

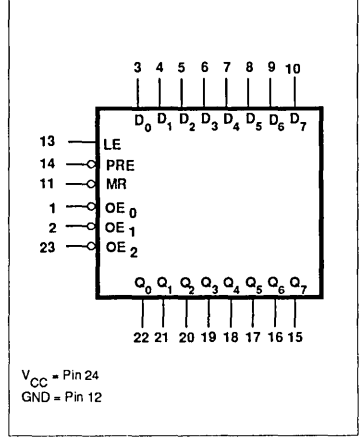
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP	-40°C to +85°C	74ABT845N
24-pin plastic SOL	-40°C to +85°C	74ABT845D

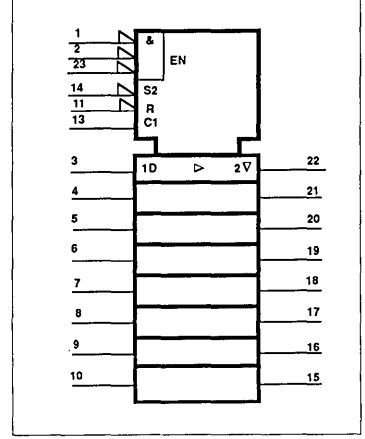
PIN CONFIGURATION



LOGIC SYMBOL

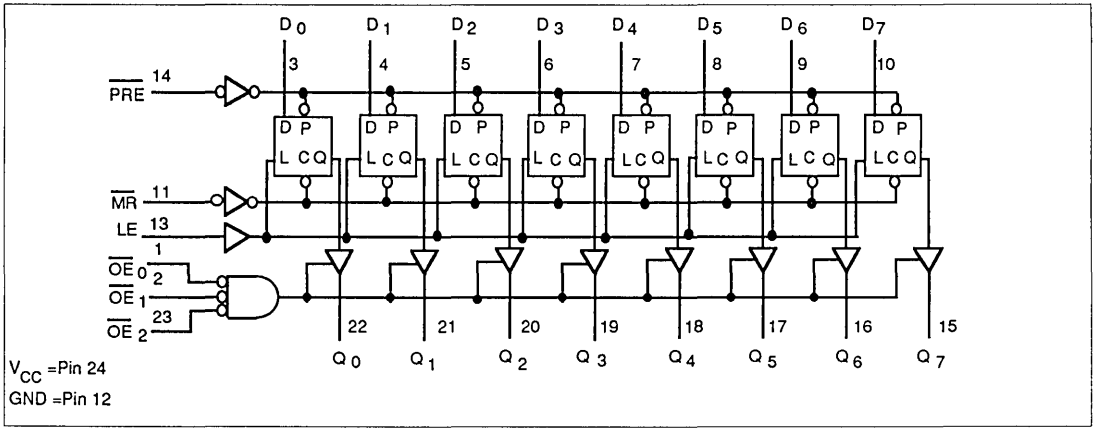


LOGIC SYMBOL(IEEE/IEC)



8-bit bus interface latch with set and reset (3-State) 74ABT845

LOGIC DIAGRAM for 'F841



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 2, 23	$\overline{OE}_n$	Output Enable input (active Low)
3, 4, 5, 6 7, 8, 9, 10	D_0 - D_8	Data inputs
15, 16, 17, 18 19, 20, 21, 22	Q_0 - Q_8	Data outputs
11	$\overline{MR}$	Master Reset input (active Low)
13	LE	Latch Enable input (active falling edge)
14	$\overline{PRE}$	Preset input (active Low)
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

FUNCTION TABLE for 'F845 and 'F846

INPUTS					OUTPUTS	OPERATING MODE
$\overline{OE}_n$	$\overline{PRE}$	$\overline{MR}$	LE	D_n	Q_n	
L	L	X	X	X	H	Preset
L	H	L	X	X	L	Clear
L	H	H	H	L	L	Transparent
L	H	H	H	H	H	
L	H	H	↓	l	L	Latched
L	H	H	↓	h	H	
H	X	X	X	X	Z	High impedance
L	H	H	L	X	NC	Hold

H= High voltage level
L= Low voltage level
h= High state one setup time before the High-to-Low LE transition
l =Low state one setup time before the High-to-Low LE transition
↓ =High-to-Low transition
X=Don't care
NC=No change
Z =High impedance "off" state

8-bit bus interface latch with set and reset (3-State) 74ABT845

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[2]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_O	DC output voltage[2]	output in Off or High state	-0.5 to +5.5	V
I_O	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

8-bit bus interface latch with set and reset (3-State) 74ABT845

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = -18mA			-1.2		-1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5			2.5		V
		V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0			3.0		
		V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]	V_{CC} = 5.5V; V_O = 2.5V	-50	-100	-180	-50	-180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		24	30		30	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]	V_{CC} = 5.5V; One input at 3.4V, other inputs at V_{CC} or GND		0.5	1.5		1.5	mA

NOTES:

1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

Document No.	
ECN No.	
Date of Issue	December 8, 1989
Status	Objective Specification
Advanced BiCMOS Products	

74ABT863

9-bit bus transceiver (3-State)

FEATURES

- Provide high performance bus interface buffering for wide data/address paths or busses carrying parity
- Buffered control inputs for light loading, or increased fan-in as required with MOS microprocessors
- Slim Dip 300 mil package
- Broadside pinout compatible with AMD AM 29863
- Output capability: +64mA/-32mA
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17
- ESD protection exceeds 2000 V per MIL STD 883C Method 3015.6 and 200 V per Machine Model

DESCRIPTION

The 74ABT863 Bus Transceiver provides high performance bus interface buffering for wide data/address paths of busses carrying parity. The 'ABT863 9-bit Bus Transceiver has NOR-ed transmit and receive output enables for maximum control flexibility.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay A_n to B_n, or B_n to A_n	C_L = 50pF; V_{CC} = 5V	4.0	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

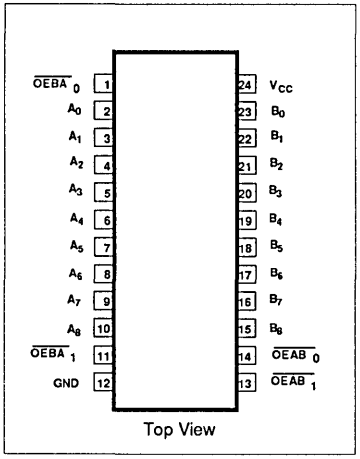
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP	-40°C to +85°C	74ABT863N
24-pin plastic SOL	-40°C to +85°C	74ABT863D

PIN DESCRIPTION

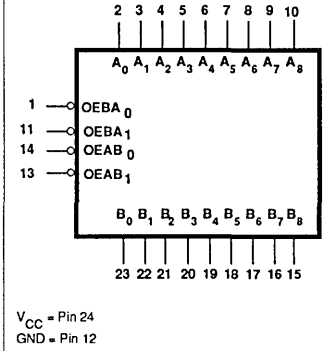
PIN NUMBER	SYMBOL	NAME AND FUNCTION
14, 13	$\overline{OEAB}_0$, $\overline{OEAB}_1$	Direction control input
2, 3, 4, 5 6, 7, 8, 9, 10	A_0 - A_7	Data inputs/outputs (A side)
15, 16, 17, 18 19, 20, 21, 22, 23	B_0 - B_7	Data inputs/outputs (B side)
1, 11	$\overline{OEBA}_0$, $\overline{OEBA}_1$	Ouput enable
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

PIN CONFIGURATION



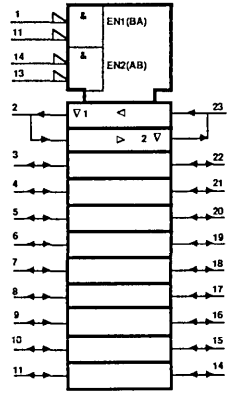
Top View

LOGIC SYMBOL



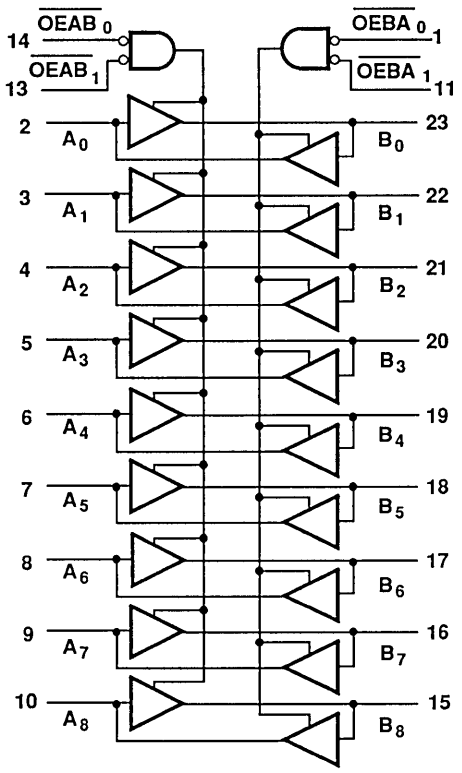
V_{CC} = Pin 24
GND = Pin 12

LOGIC SYMBOL(IEEE/IEC)



9-bit bus transceiver (3-State) 74ABT863

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS				OPERATING MODES
$\overline{OEAB}_0$	$\overline{OEAB}_1$	$\overline{OEBA}_0$	$\overline{OEBA}_1$	
L	L	H	X	A data to B bus
L	L	X	H	A data to B bus
H	X	L	L	B bus to A data
X	H	L	L	B bus to A data
H	H	H	H	Z

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

9-bit bus transceiver (3-State) 74ABT863

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[2]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_O	DC output voltage[2]	output in Off or High state	-0.5 to +5.5	V
I_O	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

9-bit bus transceiver (3-State) 74ABT863

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = -18mA			-1.2		-1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5			2.5		V
		V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0			3.0		
		V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{IH} + I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{IL} + I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]	V_{CC} = 5.5V; V_O = 2.5V	-50	-100	-180	-50	-180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		24	30		30	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin.[2]	Outputs enabled, one input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA
		Outputs 3-State, one data input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	50		50	µA
		Outputs 3-State, one enable input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

Document No.	
ECN No.	
Date of Issue	July 1990
Status	Objective Specification
Advanced BiCMOS Products	

74ABT2952

Octal registered transceiver (3-State)

FEATURES

- 8-bit Registered Transceivers
- Two 8-bit , back-to-back registers store data moving in both directions between two bidirectional busses
- Separate Clock, Clock Enable and 3-state Enable provided for each register
- AM2952 functional equivalent
- Outputs sink 64mA and source 15mA
- 300 mil wide 24-pin Slim DIP package

DESCRIPTION

The 74ABT2952 is an 8-bit Registered Transceiver. Two 8-bit back to back registers store data flowing in both directions between two bi-directional busses. Data applied to the inputs is entered and stored on the rising edge of the Clock (CPXX) provided that the Clock Enable ($\overline{CEXX}$) is Low. The data is then present at the 3-state output buffers, but is only accessible when the Output Enable ($\overline{OEXX}$) is Low. Data flow from A inputs to B outputs is the same as for B inputs to A outputs.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay CPAB or CPBA to A_n or B_n	C_L = 50pF; V_{CC} = 5V	5.0	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
C_{OUT}	Output capacitance	V_I = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs Disabled; V_{CC} = 5.5V	500	nA

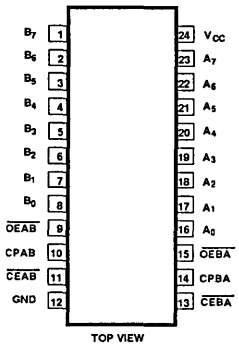
ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE
24-pin plastic DIP (300mil)	-40°C to +85°C	74ABT2952N
24-pin plastic SOL (300mil)	-40°C to +85°C	74ABT2952D

PIN DESCRIPTION

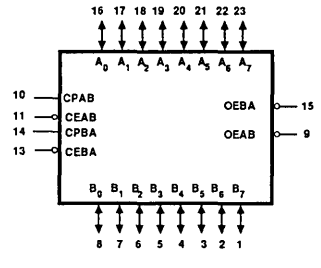
PIN NUMBER	SYMBOL	NAME AND FUNCTION
10, 14	CPAB / CPBA	Clock input A to B / Clock input B to A
11, 13	$\overline{CEAB}$ / $\overline{CEBA}$	Clock enable input A to B / Clock enable B to A
16, 17, 18, 19 20, 21, 22, 23	A_0 - A_7	Data inputs/outputs (A side)
1, 2, 3, 4 5, 6, 7, 8	B_0 - B_7	Data inputs/outputs (B side)
9, 15	$\overline{OEAB}$ / $\overline{OEBA}$	Ouput enable input
12	GND	Ground (0V)
24	V_{CC}	Positive supply voltage

PIN CONFIGURATION DIP



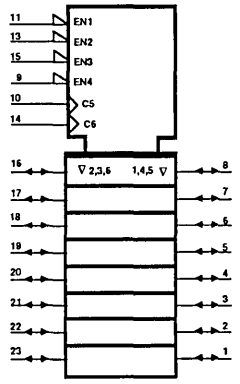
Top view

LOGIC SYMBOL



V_{CC} = Pin 24
GND = Pin 12

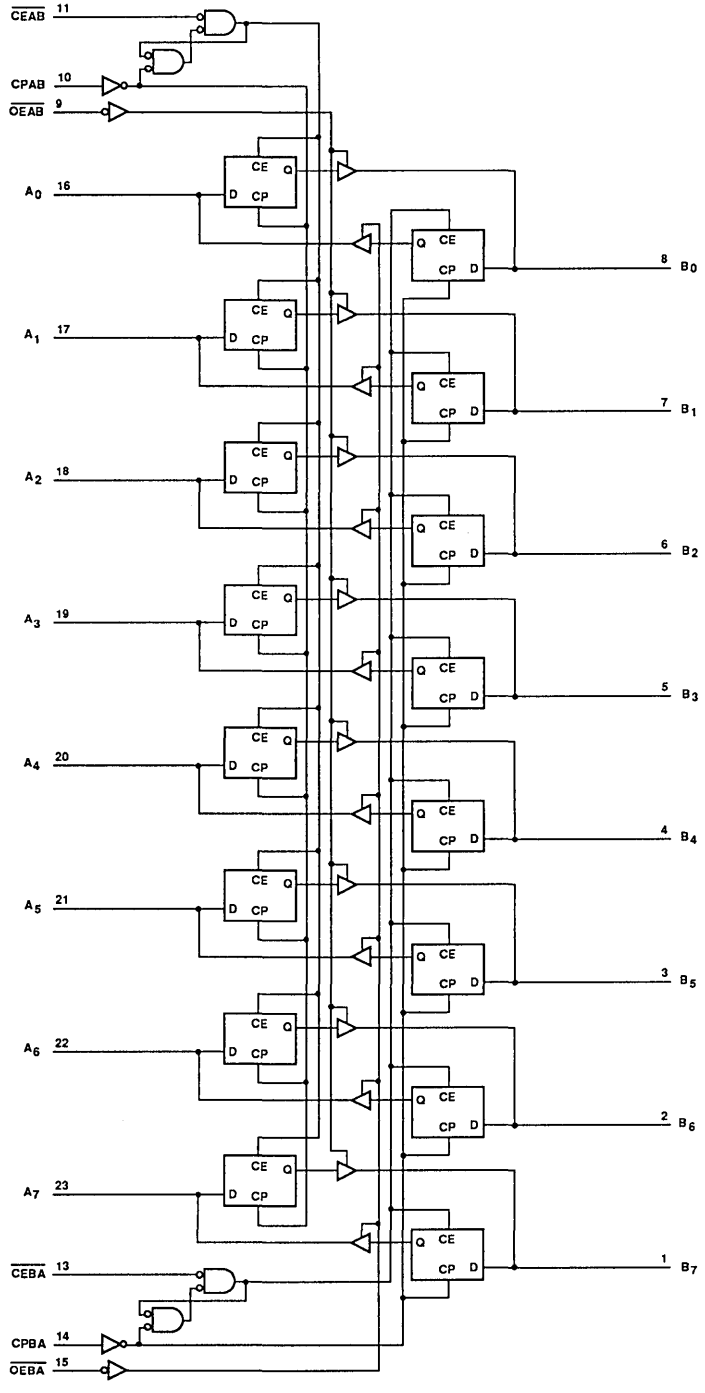
LOGIC SYMBOL(IEEE/IEC)



Octal registered transceiver (3-State)

74ABT2952

LOGIC DIAGRAM



Octal registered transceiver (3-State) 74ABT2952

FUNCTION TABLE for Register A_n or B_n

INPUTS			INTERNAL Q	OPERATING MODE
A_n or B_n	CPXX	$\overline{CEXX}$		
X	X	H	NC	Hold data
L	↑	L	L	Load data
H	↑	L	H	

H= High voltage level
L= Low voltage level
↑ =Low-to-High transition
X=Don't care
XX=AB or BA
NC=No change

FUNCTION TABLE for Output Enable

INPUTS	INTERNAL Q	A_n or B_n OUTPUTS	OPERATING MODE
$\overline{OEXX}$			
H	X	Z	Disable outputs
L	L	L	Enable outputs
L	H	H	

H= High voltage level
L= Low voltage level
X=Don't care
XX=AB or BA
Z =High impedance "off" state

ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	-18	mA
V_I	DC input voltage[2]		-1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_O	DC output voltage[2]	output in Off or High state	-0.5 to +5.5	V
I_O	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		-65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Input voltage		0.8	V
I_{OH}	High level output current		-32	mA
I_{OL}	Low level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	°C

Octal registered transceiver (3-State) 74ABT2952

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_{amb} = +25°C			T_{amb} = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage	V_{CC} = 4.5V; I_{IK} = -18mA			-1.2		-1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.5V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	2.5			2.5		V
		V_{CC} = 5.0V; I_{OH} = -3mA; V_I = V_{IL} or V_{IH}	3.0			3.0		
		V_{CC} = 4.5V; I_{OH} = -32mA; V_I = V_{IL} or V_{IH}	2.0	2.4		2.0		
V_{OL}	Low-level output voltage	V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
I_{IH} + I_{OZH}	3-State output High current	V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
I_{IL} + I_{OZL}	3-State output Low current	V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		-5.0	-50		-50	µA
I_O	Short-circuit output current[1]	V_{CC} = 5.5V; V_O = 2.5V	-50	-100	-180	-50	-180	mA
I_{CCH}	Quiescent supply current	V_{CC} = 5.5V; Outputs High; V_I = GND or V_{CC}		0.5	50		50	µA
I_{CCL}		V_{CC} = 5.5V; Outputs Low; V_I = GND or V_{CC}		24	30		30	mA
I_{CCZ}		V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	50		50	µA
ΔI_{CC}	Additional supply current per input pin[2]	Outputs enabled, one input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA
		Outputs 3-State, one data input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	50		50	µA
		Outputs 3-State, one enable input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.

Section 5
Application Notes

INDEX

Philips Components—Signetics

ApNote No.	AN602
Author	
Date of Issue	September 1990
Status	
Advanced BiCMOS Products	

AN602

Printed circuit board test fixtures for high-speed logic

INTRODUCTION

The Signetics Standard Products Group (SPG) operates a Characterization Laboratory in Orem, Utah. This Lab maintains the capability of testing the 11 logic product families the Division supports. These include: AuTTL–74XXX, Schottky-74SXXX, Low-Power Schottky-74LSXXX, FAST–74FXXX, ALS-74ALSXXX, High-Speed CMOS-74HCXXX, High-Speed CMOS/TTL-74HCTXXX, Advanced CMOS/TTL (ACL)-74ACT11XXX, Advanced CMOS (ACL)-74AC11XXX, Advanced BiCMOS (ABT)-74ABTXXX, and both 10K and 100K ECL.

In the past Signetics SPG Characterization has designed and built a series of bench test AC fixtures that provide the ability to have one fixture that addresses many product types across families. It allowed the use of a smaller fixture inventory to perform well over the majority of the devices. With the advent of the 74ACL11xxx and 74ABTXXX series the existing fixtures were no longer adequate. The largest problem with the older fixtures is the method of bypassing switching noise from V_{CC} to GND. They use bus bars running down the top and bottom sides of the PC board from the end of the device to the point of connection to the DUT V_{CC}/GND pins. Connection was then made using a copper braid to the DUT pin. While adequate for earlier logic families there is too much inductance in the power supply path to allow switching the faster transitions and higher currents of the ACL and ABT families without causing severe aberrations in output waveforms. These families of devices are also the first "TTL" types to specify operation over the entire V_{CC}/GND extremes in a simultaneous switching condition.

THEORY OF OPERATION

There are several key points in testing the ABT and ACL families. They are:

- Low inductance/high frequency power supply by-passing.

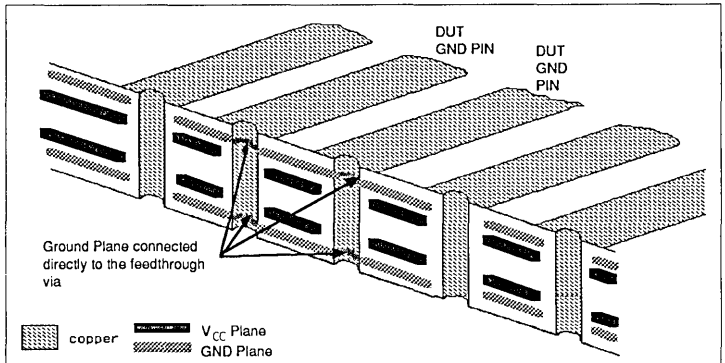


Figure 1- DUT GND/V_{CC} Connections

- Large ground and V_{CC} planes (covering virtually the entire board area).
- 50Ω signal lines for uniform impedance, high bandwidth and easy interface to test gear.
- Output AC load capacitance close to the DUT.
- Measurement point close to the DUT.

POWER SUPPLY AND GROUND

The largest difference between these fixtures and the earlier series is the inclusion of dedicated GND and other power supply planes internal to the PC board. The GND layers are used for impedance control of the signal traces and internal to the GND planes are V_{cc} and other power supply planes. In order to provide the lowest possible impedance in the power and GND connections the planes are connected directly to the DUT power/GND pad vias (See Figure #1). This feature reduces the V_{cc}/GND path inductances to a minimum and provides the highest possible frequency response under simultaneous switching conditions. This series of boards has a ring frequency of approximately 500 MHz between the power supply pins. This ensures that the output waveforms seen on the test equipment are due to the device and package, not the fixture. The trade-off for these features is that the boards must be purchased for a particular V_{cc}/GND pin combination. Signetics has designated an extension to the DUT board PC board numbers to allow calling out the separate internal layers needed for the various GND/power supply combinations. See Appendix I for the GND/V_{cc} combinations.

DEVICE SOCKETS

These boards do not use a DUT socket. All surface mount packages in this series of PC boards use a conductive polymer from Shin-Etsu for signal transmission (See Figure #3). This polymer type MAF, only conducts in the vertical direction and provides a low impedance path to connect between the DUT leads and the PC board pad. DIP pattern boards use Augat sockets soldered flush with the PC board surface. This effectively eliminates any inductance due to a socket. The trade-off is decreased insertions on the surface mount boards. In order to align an SMT device to the required DUT pads alignment blocks and alignment guides are required (See Appendix I for dimensions). They are machined from a phenolic material for over temperature operation and electrical isolation. The block is designed to align the DUT to

Printed circuit board test fixtures for high-speed logic

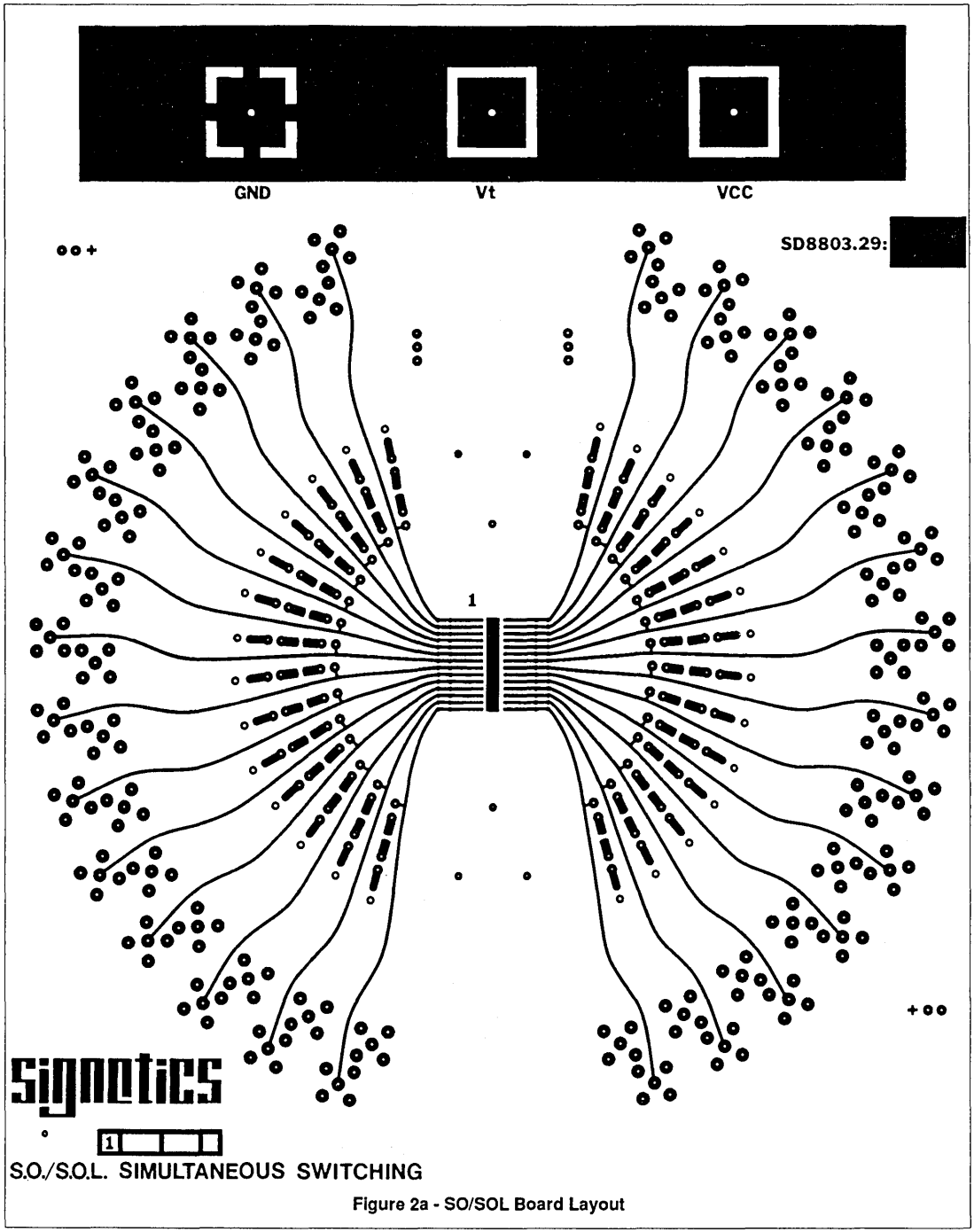


Figure 2a - SO/SOL Board Layout

Printed circuit board test fixtures for high-speed logic

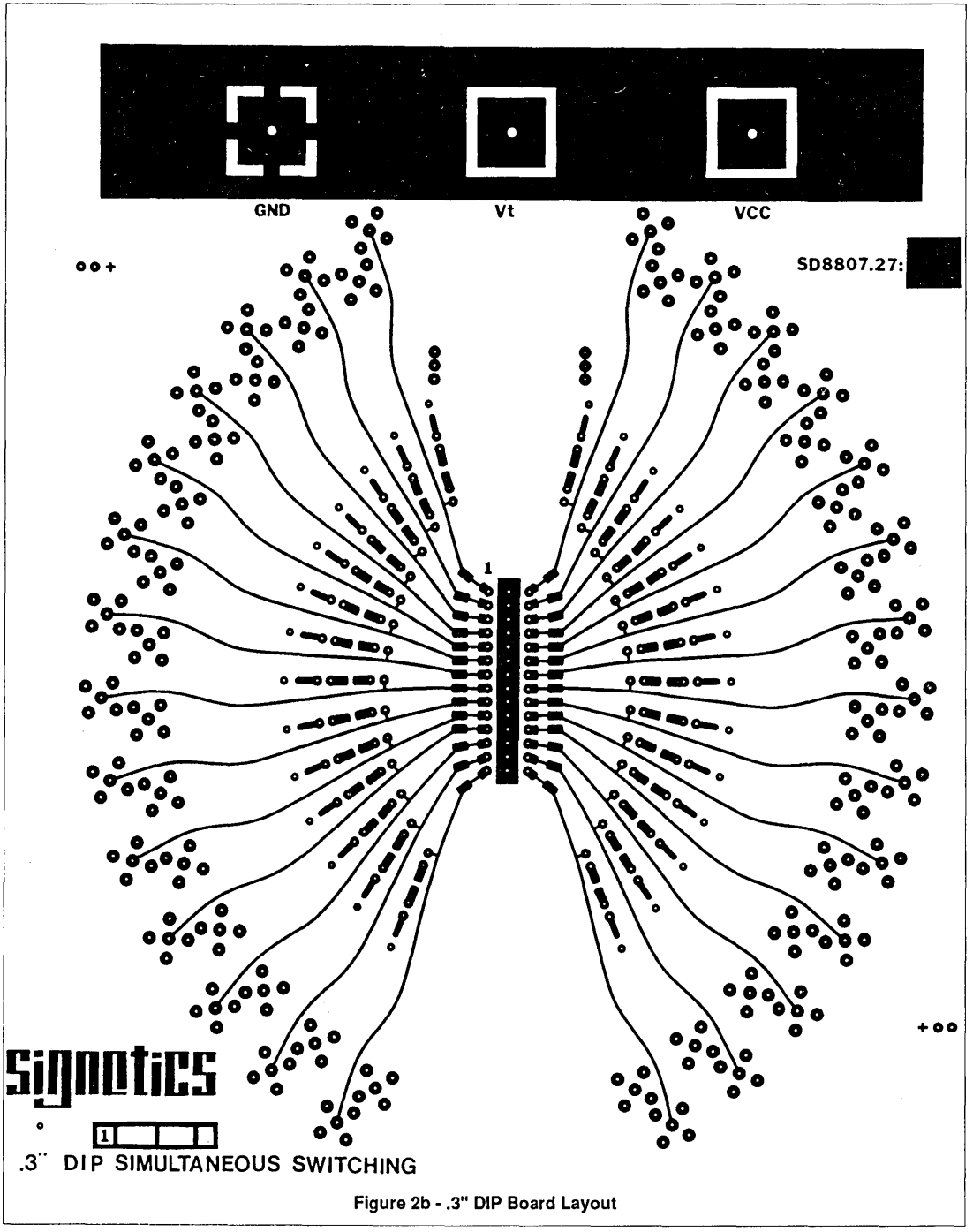


Figure 2b - .3" DIP Board Layout

Printed circuit board test fixtures for high-speed logic

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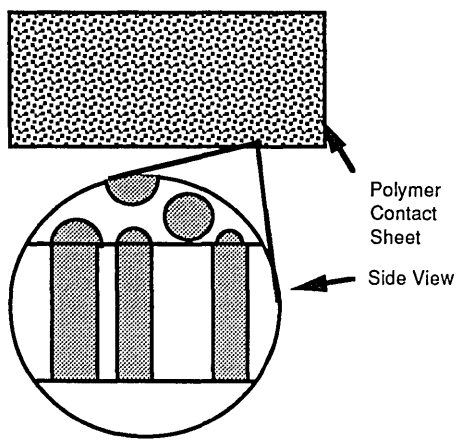
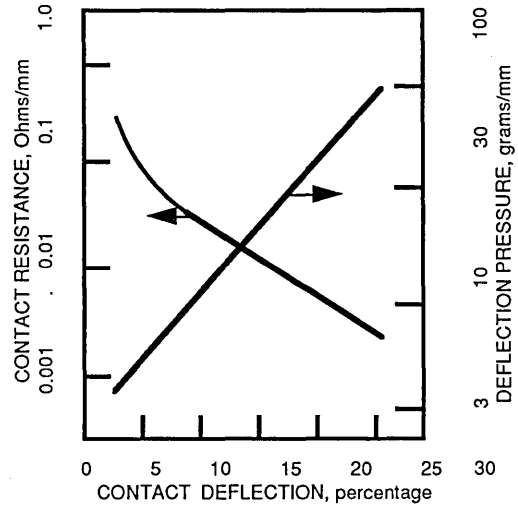
the pads, allow circulation for a temperature stream and on gull-wing devices, to provide mechanical pressure to the leads to ensure contact with the conductive polymer. The top hole in the block also doubles as the vacuum wand access to change devices. The boards are also designed to use the alignment guides to provide a mechanical clamp and hold the polymer in place and allow easy replacement. See Figure #4.

SIGNAL LINES

All signal lines have a 50Ω impedance, determined by the microstrip layout method. The 50Ω value was selected to allow easy termination for input signal generators and a 10:1 divider for outputs. The inputs are also terminated into a 10:1 divider, 50Ω terminator. This allows the boards to be built with very small stubs for signal integrity and all oscilloscope channels can be set up to the same vertical amplification.





MAF 0.4 mm thick

Current carrying capacity amps/mm:	5.0
Number of conductors/mm:	7.3
Contact resistance milli-Ohms/mm:	4.8
Minimum contact area, mm:	0.287

Sample connector: 0.4mm thick
Electrode: 1.2mm (gold plated)

Figure 3 - Shin-Etsu Polymer

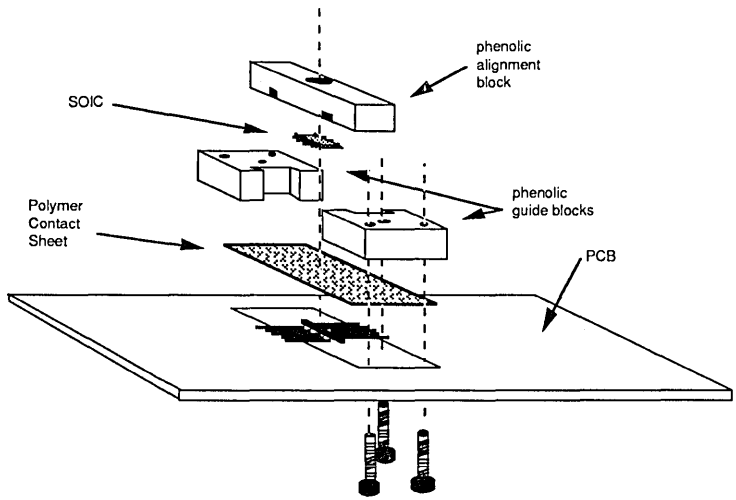


Figure #4. Illustrated Parts Breakout of SO Device Assembly

Printed circuit board test fixtures for high-speed logic

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On the top of the PC board is a trace running straight from the SMB connector to the DUT pad. The only connection to this line is a jumper allowing connection of a pull-up resistor for TTL 3-S or open-collector outputs. On the bottom of the PC board the trace has a break in it to allow mounting a 453Ω resistor (R1) for the 10:1 divider network. Since the worst case load in simultaneous switching conditions is to mount a lumped capacitance directly on the DUT pin, a direct connection to the internal GND plane is in the center of the DUT pads to allow soldering on load capacitors. For input pins it is also used for mounting termination resistors directly beneath the device. Therefor the PC boards must be assembled for a particular I/O pin combination.

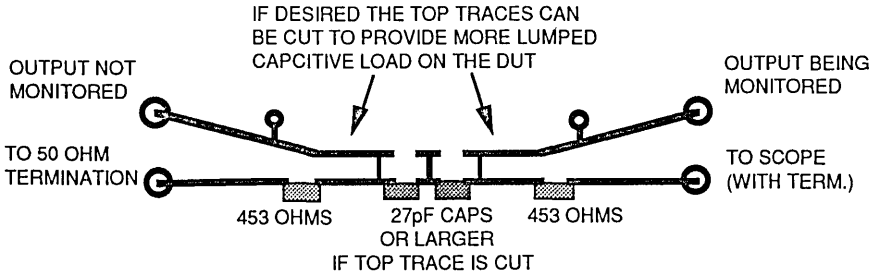

Figure 5a - Signetics SSE PC Board Input Schematics

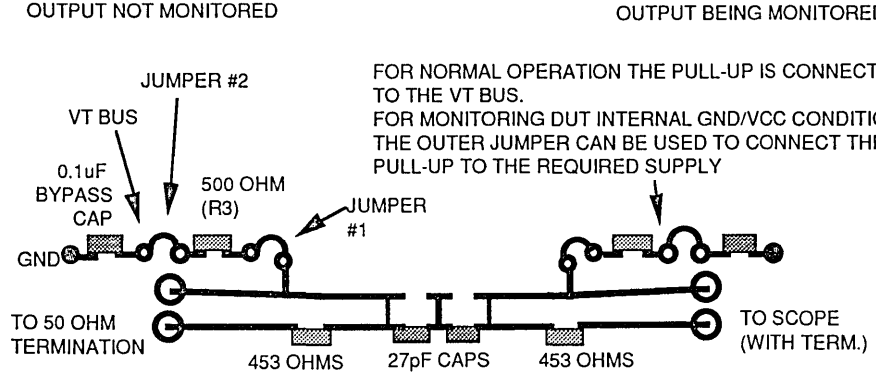

Figure 5b - Signetics SSE PC Board 2-S Output Schematics

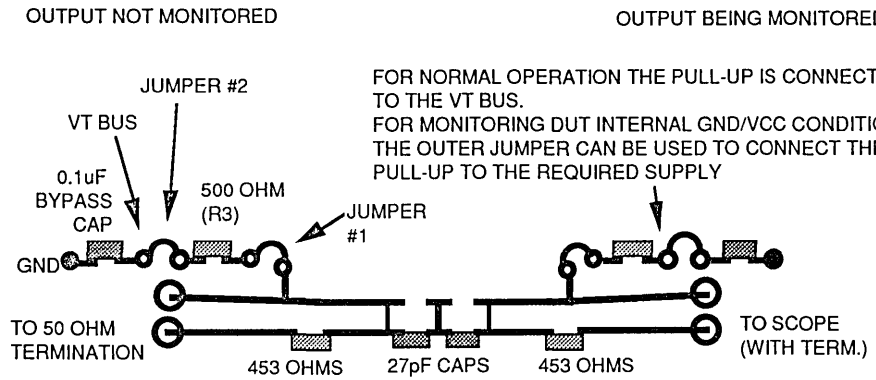

Figure 5c - Signetics SSE PC Board 3-S/O.C. Output Schematics

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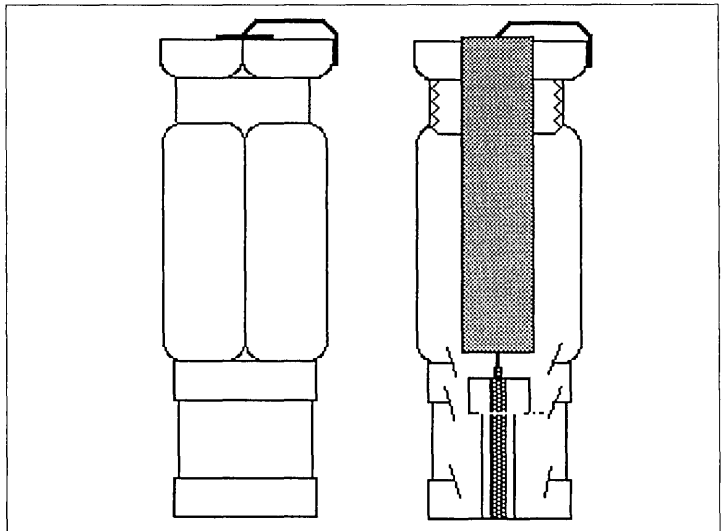
If a DUT pin is an input the board is configured in a loop through mode. The outer circle of SMB connectors is connected to the signal source. On the bottom side of the PC board a 56.2Ω (R2) resistor is soldered between the DUT pad and the GND. Across the break in the bottom trace a 453Ω resistor is soldered. In combination with a 50Ω o-scope termination or a 50Ω SMB terminator the 450 + 50Ω in parallel with the 56.2Ω provides the proper 50Ω termination for signals and a monitoring capability (See Figure 5a).

For an output pin the outer ring of SMB's is not used. The same 453Ω/50Ω pair is used as a 10:1 divider into the o-scope and still provide the specified 500Ω pull-down resistor. A chip capacitor of sufficient capacitance to bring the total to 50pF is soldered between the bottom DUT pad and the GND (See Figure 5b). For 3-S or open collector devices the 500Ω pull-up resistor (R3) on the top trace is jumpered in with a .1" jumper (#1). The outside of the pull-up resistor also has a .1" jumper (#2) to allow connection to the internal V_T bus or some other termination voltage as needed for any particular test (See Figure 5c).

The bottom trace SMB connector is always connected either to an SMB 50Ω terminator or the 50Ω terminated input of the scope to complete the load. See Figure 6 for a 50Ω terminator example.



50Ω Load Resistors Using SMB Cable Connectors

Figure 6 - Resistive Load Used on Non-monitored SMB Connectors

INPUT STIMULUS AND MEASUREMENT

As stated previously, the measurements are made with 50Ω sampling systems. The connections to these systems are made via SMB connectors. This was chosen since it is a standard connector, available from several sources, uses push-on operation, is small for easy configuration and is capable of high bandwidth operation. Figure 8 shows where the connections are made and also where the pulse generators connect to the input, also an SMB connector. Since the 450Ω resistor, R1, is soldered directly to the pin of the device, see Figure 6, the actual probe tip is at that point. This has the advantage of eliminating any distance from the device to the probe tip, thus guaranteeing accurate results.

INSERTING DEVICES

To hold surface mount devices in place the alignment block is clipped down to the PC board with brass clips mounted to the alignment guides. This provided the simplest solution to several conflicting demands. The device had to have good contact with the Shin-Etsu polymer to function. There needed to be some method of allowing a temperature stream flow around the device, and the devices needed to be changed. For SO devices the edges of the package cutout provide enough pressure to the top of the DUT leads to make good contact with the polymer, for PLCC the top of the cutout provides the same function. The hole through the middle of the alignment block allows a vacuum wand to be inserted and hold the device and block together until they are clipped to the PC board. Several models of wands are available from H-Square Company for handling devices, including one with a built in static dissipation resistor and lead for ESD protection. They also have designed a custom tip to mate with the top hole of the alignment blocks and prevent the block from bouncing up the wand tube prior to clipping it to the PC board. Cutouts around the device allow exit for the temperature stream.

VERSATILITY AND COST

At some point, there is a choice between the most technically attractive options and the cost of such options. This fixture has been designed to optimize its technical effectiveness. This was dictated by the test requirements of the ACL and ABT families, specifically the simultaneous switch specifications. It is also suitable for testing FAST, ALS and ECL product devices if the existing series of boards do not provide the needed environment to get accurate, repeatable results.

For the user the only connections being made to the fixture are:

- V_{CC} (banana jack) This is the positive DUT voltage supply.
- GND (banana jack) This is the common ground of all input supplies.
- V_T supply (banana jack) This is the 3-state/O.C. pull-up voltage and is jumpered to each pin as needed.

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- V_{GND} supply (banana jack) This is the DUT GND layer used for ECL which requires a +2V offset for proper termination on the output pins when using oscilloscope input termination.
- V_{EE} supply (banana jack) This is the negative DUT power supply layer used for ECL devices
- Input Stimulus (outside SMB connectors) This is found on every input/output pin. More than one pin may be used in this manner.
- Output Measurement or Scope Connection (inside SMB connectors). More than one pin may be used in this manner. *Remember*, if this pin is not connected to a scope, a 50Ω resistor must be connected here to ground to complete the 500Ω resistive load or input termination network. Signetics has constructed their own 50Ω load by soldering a high quality (high frequency) 50Ω resistor inside a female SMB cable connector. See Figure 6.

With these seven connection types, the fixture is capable of testing the product lines mentioned.

Included in Appendix I are the internal GND/V_{CC} connections of the existing defined layers.

In Appendix II are the dimensions of the alignment blocks and guides for the SMT packages.

In Appendix III is the parts list for these fixtures and the supplies used by Signetics.

This in no way constitutes Signetics endorsements of these suppliers and the customer may select their own supplier if they so desire. This fixture is offered to the public to duplicate and use within their own environments. Signetics will not provide any materials but will allow the manufacturers of the board and materials to build and/or supply for any requesting party. Pricing and availability are left to the vendors and Signetics has no control over those issues. The intent is to provide something for users of ACL and ABT, and other advanced logic family devices, that has been proven and tested in use, namely the characterization of these products prior to the introduction to the market place.

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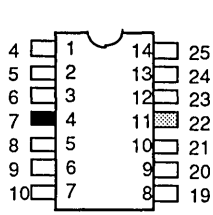
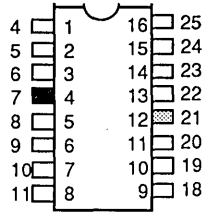
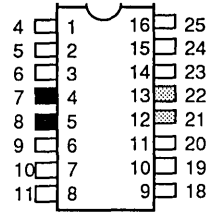
Appendix I - Internal GND/V_{CC} Connections



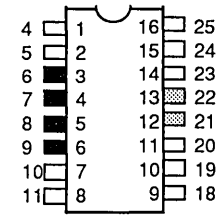
SD8803.29:001



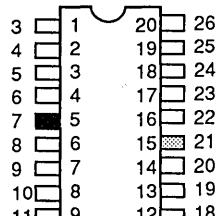
SD8803.29:002



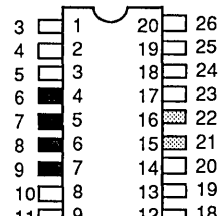
SD8803.29:003



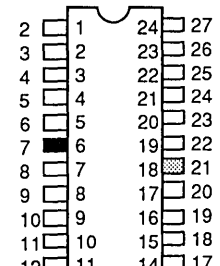
SD8803.29:004



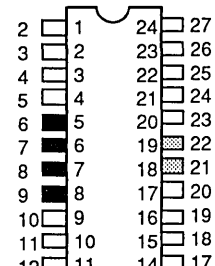
SD8803.29:002



SD8803.29:004



SD8803.29:002

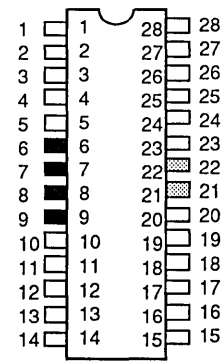


SD8803.29:004

VCC
GND

(On each package outline the outer numbers refer to the PCB footprint and the inner numbers refer to the DUT pins.)

For .3" DIP boards, substitute SD8807.27:nnn for SD8803.29:nnn



SD8803.29:004

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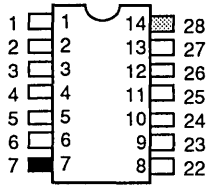
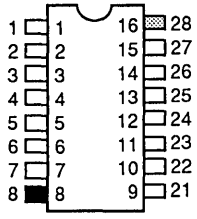
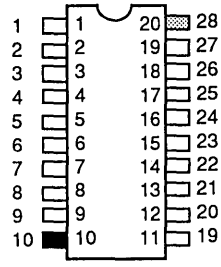


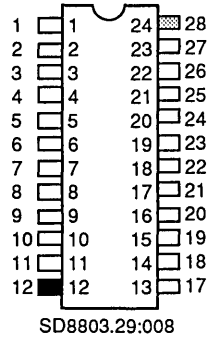
SD8803.29:005



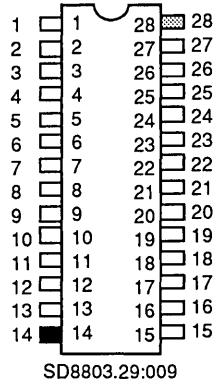
SD8803.29:006



SD8803.29:007



SD8803.29:008



SD8803.29:009

VCC GND

NOTE: The PC board/package configurations shown above require the use of the SO alignment blocks with offset package cutouts.

Defined layers and their connections for SO (SD8803.29:nnn) and .3" DIP (SD8807.27:nnn) boards are:

GROUND LAYER (2.x)		V_{CC} LAYER (3.y)	
2.1 =	7	3.1 =	22
2.2 =	7, 8	3.2 =	21, 22
2.3 =	10	3.3 =	28
2.4 =	6, 7, 8, 9	3.4 =	21
2.5 =	21, 22	3.5 =	8
2.6 =	21	3.6 =	7
2.7 =	8	3.7 =	1
2.8 =	12		
2.9 =	14		
2.A =	4, 8, 11, 18, 22, 25		

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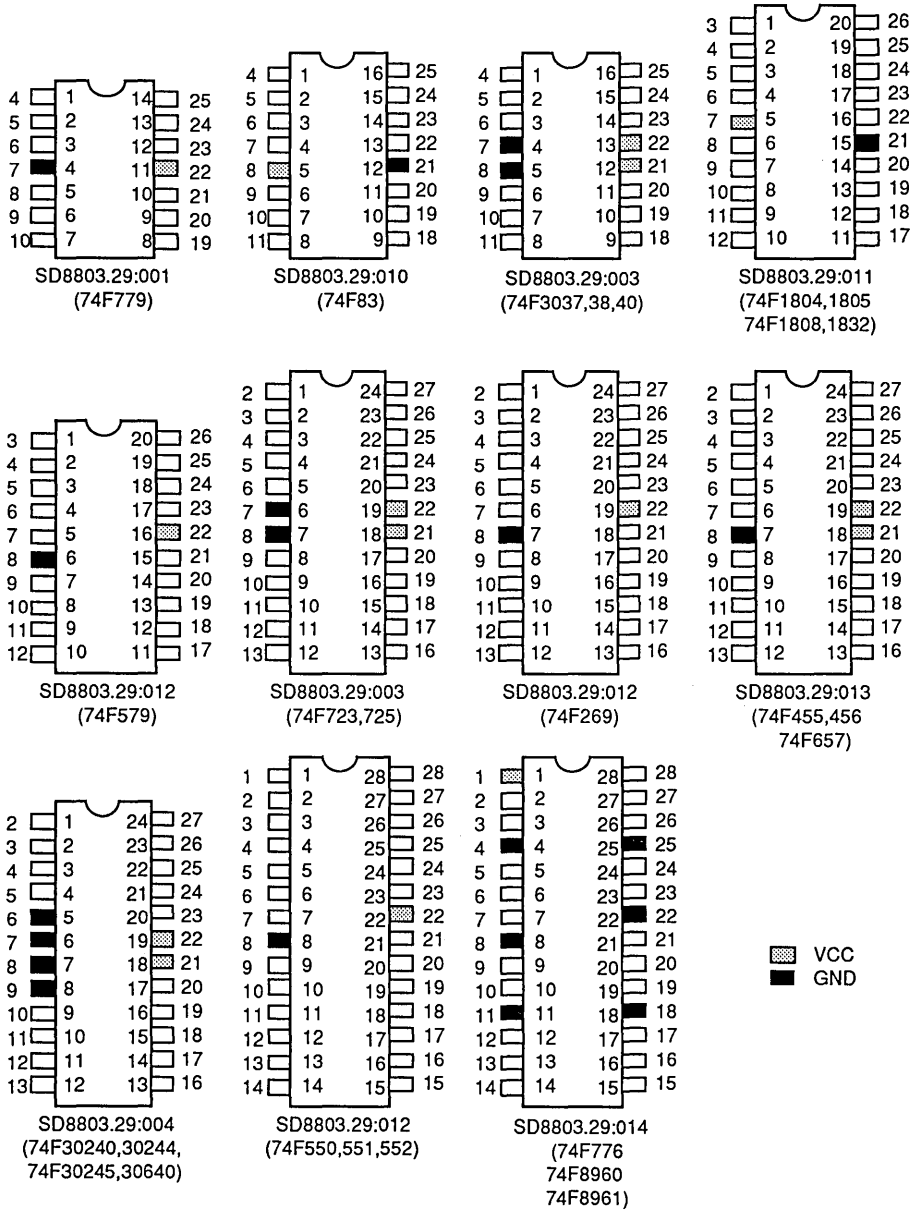

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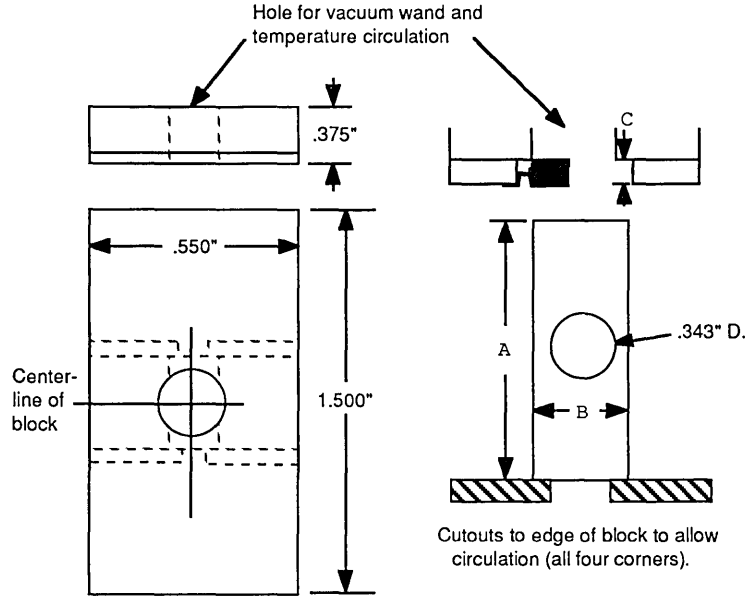
APPENDIX II - SMT Alignment Blocks and Guides



Material phenolic or other insulator able to withstand 155°C.

DIMENSIONS FOR VARIOUS SIGNETICS PRODUCED PACKAGES

PACKAGE		A	B	C	OFFSET FROM CENTERLINE
JEDEC	14 PIN .150"	.346 +-.001	.205	.055+-.001	.025
JEDEC	14 PIN .150"	.346 +-.001	.205	.055+-.001	.175
EIAJ II	14 PIN .210"	.405 +-.001	.265	.075+-.001	.025
EIAJ II	14 PIN .210"	.405 +-.001	.265	.075+-.001	.175
JEDEC	16 PIN .150"	.400 +-.001	.200	.050+-.001	.000
JEDEC	16 PIN .150"	.400 +-.001	.200	.050+-.001	.150
EIAJ II	16 PIN .210"	.405 +-.001	.265	.070+-.001	.000
EIAJ II	16 PIN .210"	.405 +-.001	.265	.070+-.001	.150
JEDEC	16 PIN .300"	.406 +-.001	.360	.090+-.003	.000
JEDEC	16 PIN .300"	.406 +-.001	.360	.090+-.003	.150
EIAJ II	20 PIN .210"	.505 +-.001	.265	.075+-.001	.000
EIAJ II	20 PIN .210"	.505 +-.001	.265	.075+-.001	.100
JEDEC	20 PIN .300"	.510 +-.001	.365	.095+-.003	.000
JEDEC	20 PIN .300"	.510 +-.001	.365	.095+-.003	.100
JEDEC	24 PIN .300"	.605 +-.001	.365	.095+-.003	.000
JEDEC	24 PIN .300"	.605 +-.001	.365	.095+-.003	.050
JEDEC	28 PIN .300"	.710 +-.001	.365	.090+-.003	.000

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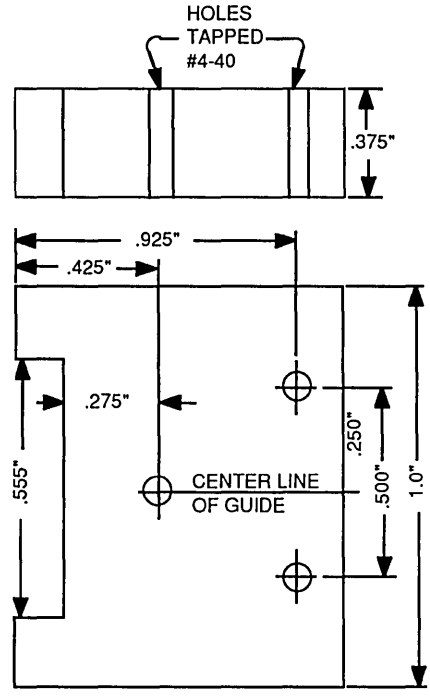
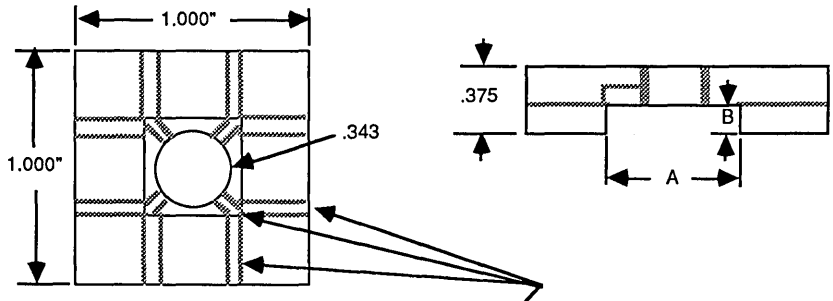


SO Alignment Guides



Cutouts from center hole to edge of block to allow circulation around device when forcing temperature (all four corners).

PACKAGE TYPE	A	B
20 PIN PLCC	.390"	.160"
20 PIN LCC	.350"	.060"
28 PIN PLCC	.494"	.160"
28 PIN LCC	.450"	.060"

Figure 12 - PLCC/LCC Alignment Block and Package Cutout Dimensions

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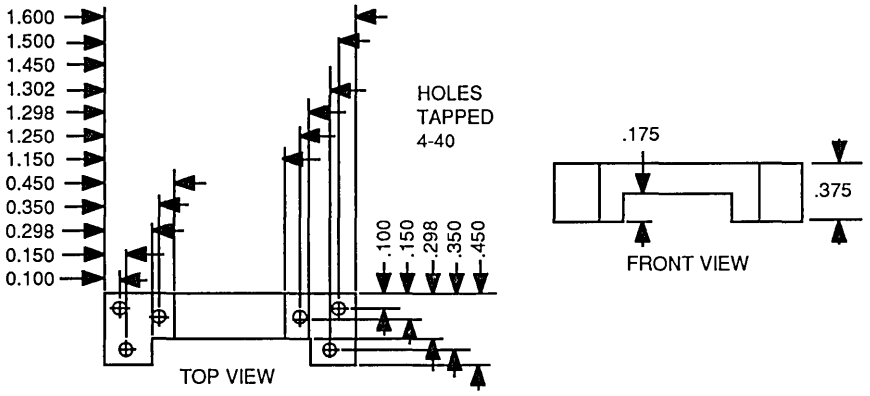
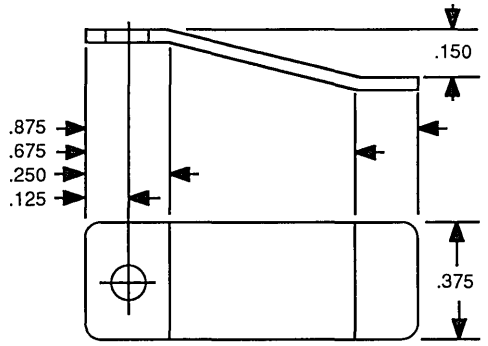


PLCC/LCC Alignment Guide



Hole .116 +- .003" diameter.
.020" Brass shim stock
Edges deburred
Corners radiused .050"

All other dimensions +- .025"

Alignment Block Retainer Clip

Printed circuit board test fixtures for high-speed logic

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APPENDIX III - Component and Vendor List and Construction Hints

The following prices have been quoted for a 10 piece build of a 28 pin test fixture and are not binding in any way.

1. Printed circuit board, requirement: 1 per part configuration.

BOARD	PART #	COST	
SO and SOL	SD8803.29:nnn	$160.00	
DIP	SD8807.27:nnn	$160.00	
PLCC (20/28 pin)	SD8901.20:nnn	$160.00	(6 layer)
PLCC (20/28 pin)	SD8901.20:nnn	$182.65	(8 layer)

Supplier:
Prototype and Production Circuits
8040 S. 1444 W.
West Jordan, UT 84084
(801) 566-5431

2. Conductive Polymer Shin-Etsu# to Available in sheets of 0.2 to 0.8 mm in thickness in 0.1 mm steps and 50 mm X 100 mm.

(0.2 mm)	MAF2tx50x100	$70.00 @	
(0.4 mm)	MAF4tx50x100	$77.00 @	(recommended)
(0.6 mm)	MAF6tx50x100	$81.00 @	

Supplier:
Shin-Etsu Polymer,
SP America Inc.
34135 7th Street
Union City, CA 94587
(415) 475-9000

3. Ceramic multilayer chip capacitors from Johanson Dialectrics.

27 pF	101R09N270JP (5%)	$0.45 @ in 1000's
33 pF	101R09N330JP (5%)	$0.45 @ in 1000's

Supplier:
Johanson Dialectrics
2220 Screenland Drive
Burbank, CA 91505
(213) 848-4465

4. Tantalum dipped capacitors from Sprague.

4.7 uF, 35 V	196D475X9035JA1	$0.63 @ 50's

Supplier: Newark Electronics

5. Ceramic chip resistors from Dale Electronics, Inc or Bourns, Inc.

453 Ohm (Dale)	CRCW0805-4530F (1%)	$137.00/Reel (1000 or 5000)
56.2 Ohm	CRCW0805-56R2F (1%)	(These are also available in a
500 Ohm	CRCW0805-4990F (1%)	CRCW1206 size.)
453 Ohm (Bourns)	CR0805-4530FVBA (1%)	$100.00/Reel (5000)
56.2 Ohm	CR0805-56R2JVBA (5%)	(These are also available in a
500 Ohm	CR0805-4990FVBA (1%)	CR1206 size.)

Suppliers:	Dale Electronics, Inc.	Bourns, Inc
	2300 Riverside Blvd.	1200 Columbia Avenue
	Norfolk, NE 68701	Riverside, CA 92507
	(402) 371-0080	(714)781-5500

6. SMB connectors from Applied Engineering Products.

SMB Straight Male Jack Receptacle		
	2009-1511-000	$2.19 @ in 100-250's
SMB Straight Female Cable Plug for RG-174 coax		
	2002-1551-003	$3.59 @ in 100-250's
SMB Tee Adaptor (Jack-Plug-Jack)		
	5215-1501-000	$12.51 @ in 50-99's
SMB Tee Adaptor (Plug-Plug-Jack)		
	5235-1501-000	$17.26 @ in 1-24's
Supplier:	Spirit Electronics, Inc 7819 East Greenway, Suite 9 Scottsdale, AZ 85206 (602) 998-1533	

7. Sockets-pins and jumpers from Augat.

Socket Terminal Pin	LSG-1AG14-14	$0.20 @ in 1000's
Jumpers (.1")	8156-651P2	$0.05 @ in 1000's
Supplier:	Augat, Inc 33 Perry Ave P.O. Box 779 Attleboro, MA 02703 (617)-222-2202	

8. Vacuum wand and tips from H-Square Co.

Vacuum wand	NOS	$28.14 @
Vacuum wand w/conductive connection for ESD protection		
	NOSCA	$66.00 @
Tip-modified (to fit Signetics alignment blocks)		
	T502VG(SPECIAL)	$186.00/6 ea
Supplier:	H-Square Co. 1289-H Reamwood Ave Sunnyvale, CA 94089 (408)734-2543	

9. Mounting screws.

Phillips pan head machine screws		
	4-40 X 3/8	$0.02 @ 100's
	4-40 X 3/4	$0.02 @ 100's
	6-32 X 3/8	$0.03 @ 100's
Supplier:	Bonneville Industry Supply Co. 45 So. 1500 W. Orem, Utah 84058 (801) 225-7770	

10. Banana Plug Jack.

H.H. Smith Type	Order #	
White 1509-101	28F1178	3/board-color your choice
Red 1509-102	35F870	3/board-color your choice
Black 1509-103	35F869	3/board-color your choice
Green 1509-104	28F1179	3/board-color your choice
Blue 1509-105	28F1180	3/board-color your choice
Yellow 1509-107	28F1182	3/board-color your choice $ .35 @ 3 's
Supplier:	Newark Electronics.	

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Construction Hints:

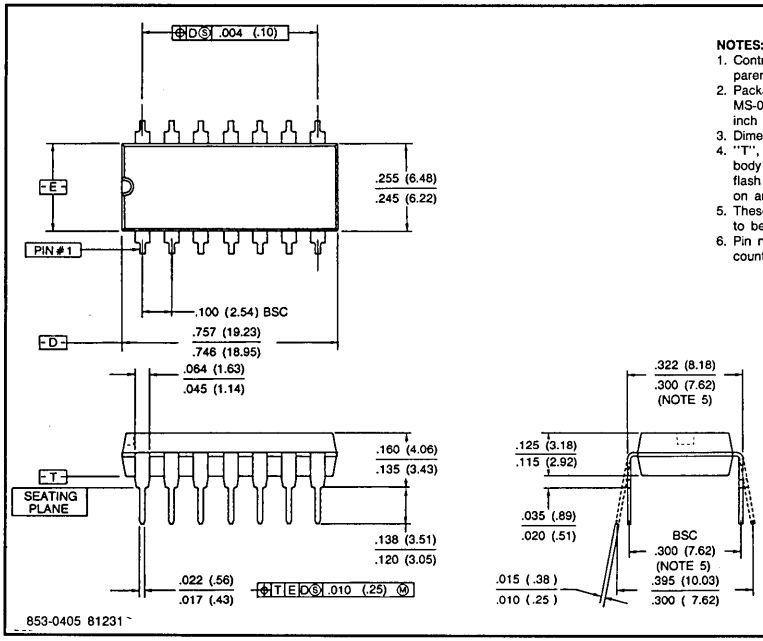
A suggested order of assembly is as follows:

1. Install SMB Connectors. Elevate base from board .05" (this can be done with a shim or the posts can be soldered flush with the bottom side of the PC board).
2. Install Augat pin-sockets (3-S or DIP boards only, use a device inserted into the sockets on the DIP boards to hold them steady or tape over the open end of the socket with masking tape and remove after soldering).
3. Install 453 Ohm load/termination resistors (for surface mount components apply a drop of solder to one pad then reflow and mount the component, then solder the other side to its pad).
4. Install the 56.2 Ohm load/termination resistors and load caps (solder the ends on the individual lines and then the common GND connections).
5. Install banana jacks.
6. Connect V_{CC}, GND, and V_T supplies from banana jacks to board.
7. Attach alignment blocks and guides with 4-40 Phillips pan head machine screws (SMT boards only).
8. Remove all remaining flux. Keep "flux-off" or other solvent from banana jacks.

Section 6
Package Outlines

Package Outlines

14-PIN PLASTIC DUAL-IN-LINE

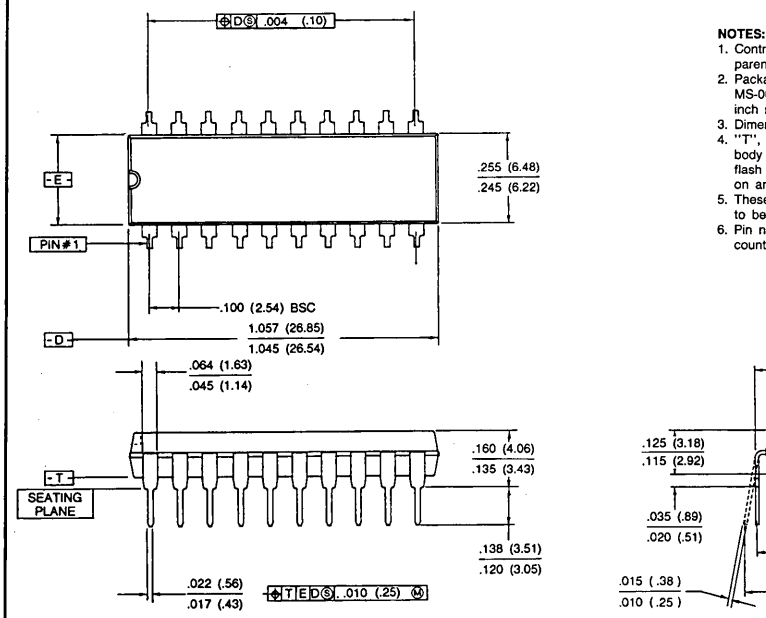


NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AC for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 14 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #14 when viewed from the top.

853-0405 81231

NH1

20-PIN PLASTIC DUAL-IN-LINE



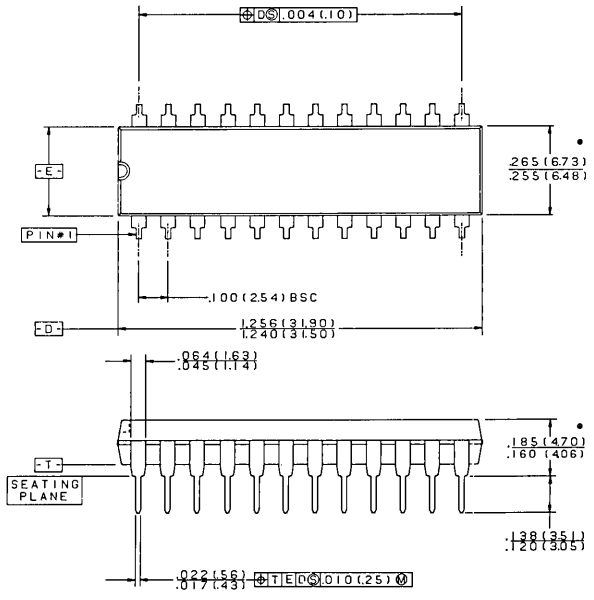
NOTES:
1. Controlling dimension: inches. Metric are shown in parentheses.
2. Package dimensions conform to JEDEC specification MS-001-AE for standard dual in-line (DIP) package .300 inch row spacing (PLASTIC) 20 leads (issue B. 7/85)
3. Dimensions and tolerancing per ANSI Y14. 5M-1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010 inch (.25mm) on any side.
5. These dimensions measured with the leads constrained to be perpendicular to plane T.
6. Pin numbers start with pin #1 and continue counterclockwise to pin #20 when viewed from the top.

853-0408 81234

NL1

Package Outlines

24-PIN PLASTIC DUAL-IN-LINE (300mil-wide)



NOTES

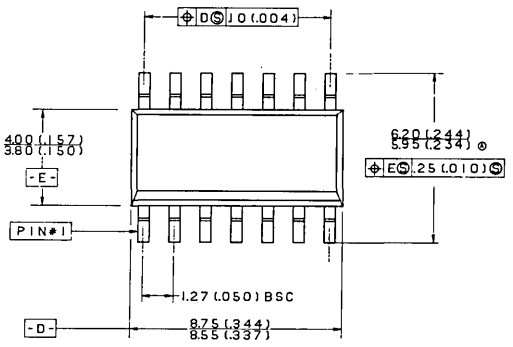
1. CONTROLLING DIMENSION: INCHES METRIC ARE SHOWN IN PARENTHESES.
2. PACKAGE DIMENSIONS CONFORM TO JEDEC SPECIFICATION MS-001-AF FOR STANDARD DUAL IN-LINE (DIP) PACKAGE 300 INCH ROW SPACING (PLASTIC) 24 LEADS (ISSUE B.7/85)
3. DIMENSION AND TOLERANCING PER ANSI Y14.5M-1982.
4. "T" "D" AND "E" ARE REFERENCE DATUMS ON THE MOLDED BODY AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (.25MM) ON ANY SIDE.
5. THESE DIMENSIONS MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO PLANE T.
6. PIN NUMBERS START WITH PIN#1 AND CONTINUE COUNTERCLOCKWISE TO PIN#24 WHEN VIEWED FROM THE TOP.

853-0410 98727

NN1

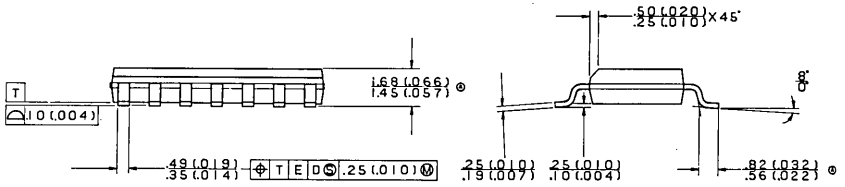
Package Outlines

14-PIN PLASTIC SMALL OUTLINE (SO)



NOTES

1. PACKAGE DIMENSIONS CONFORM TO JEDEC SPECIFICATION MS-012-AB FOR STANDARD SMALL OUTLINE (SO) PACKAGE. 14 LEADS. 3.75MM (.150") BODY WIDTH (ISSUE A. JUNE 1985).
2. CONTROLLING DIMENSIONS ARE MM. INCH DIMENSIONS IN PARENTHESES.
3. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1982.
4. "T" "D" AND "E" ARE REFERENCE DATUMS ON THE MOLDED BODY AND DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .15MM (.006") ON ANY SIDE.
5. PIN NUMBERS START WITH PIN#1 AND CONTINUE COUNTERCLOCKWISE TO PIN#14 WHEN VIEWED FROM TOP
6. SIGNETICS ORDERING CODE FOR A PRODUCT PACKAGED IN A PLASTIC SMALL OUTLINE (SO) PACKAGE IS THE SUFFIX D AFTER THE PRODUCT NUMBER.

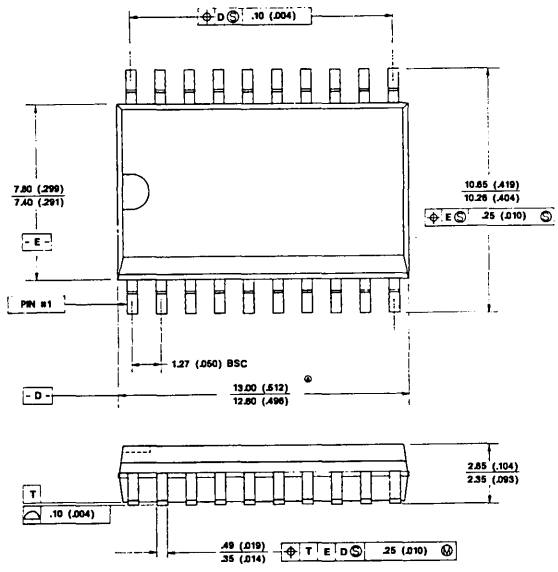


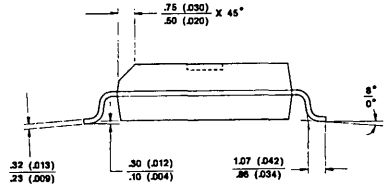
853-0175 91504

DH1

Package Outlines

20-PIN PLASTIC SMALL OUTLINE (SOL)





NOTES:

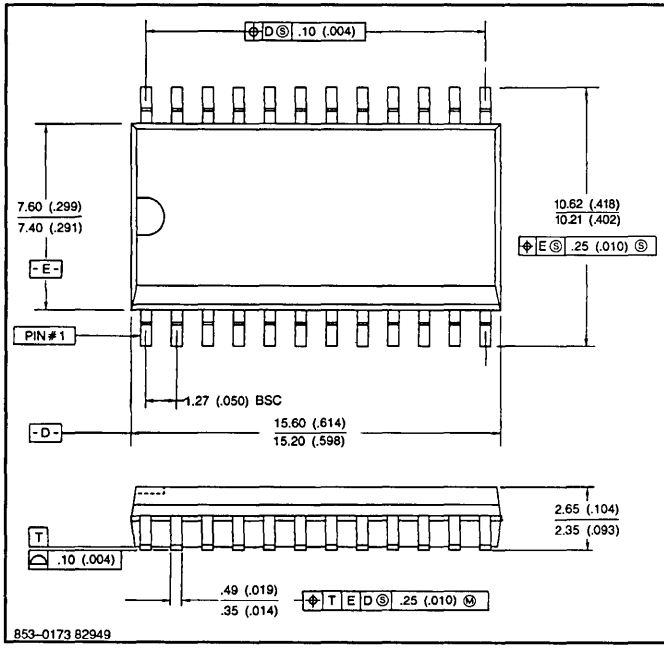
1. Package dimensions conform to JEDEC specification MS-013-AC for standard small outline (SO) package, 20 leads, 7.50mm (.300") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensioning and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #20 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

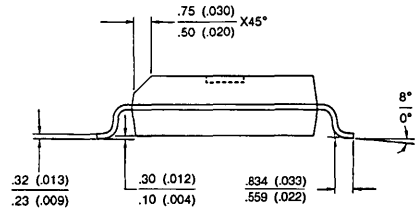
853-0172 82948

DL2

Package Outlines

24-PIN PLASTIC SMALL OUTLINE (SOL)





NOTES:

1. Package dimensions conform to JEDEC specification MS-013-AD for standard small outline (SO) package, 24 leads, 7.50mm (.300") body width (issue A, June 1985).
2. Controlling dimensions are in mm. Inch dimensions in parentheses.
3. Dimensions and tolerancing per ANSI Y14.5M- 1982.
4. "T", "D" and "E" are reference datums on the molded body and do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .15mm (.006") on any side.
5. Pin numbers start with pin #1 and continue counterclockwise to pin #24 when viewed from top.
6. Signetics ordering code for a product packaged in a plastic small outline (SO) package is the suffix D after the product number.

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