# *IMPROVING SWITCHING REGULATOR DYNAMIC RESPONSE*

Edited by Stan Dendinger
Manager, Advanced Product Development
Silicon General, Inc.

**ABSTRACT**

Recent introductions of LSI integrated circuits for P.W.M. control have offered considerable simplification to the job of optimizing the design of switching regulators. In addition to greatly reducing the necessary circuitry, the linear transfer function of these devices eases the task of stabilizing the feedback loop and offers several possibilities for improved response. Experimental methods for evaluating the response characteristics of the P.W.M. switching and output stages can be used to confirm simplifying assumptions of linear operation. With this data, several approaches to equalization networks can be compared for performance optimization.

## INTRODUCTION

The past few years have seen a major revolution take place in the field of power supply design. Whether forced upon us by the need for energy conservation or finally made practical thru recent advances in semiconductor technology, switching regulators are now the name of the game in voltage control. Novices soon learn, however, that the implementation of a well-designed switching supply involves a little more skill than that required for a linear regulator.

Although the theory of switching regulation has long been known, there is much practical technology - or art - in designing efficient and reliable systems. This is still true even though recently introduced semiconductor devices have made the job at least a little easier. It is the purpose of this discussion to cover a few of the practical aspects of implementing and stabilizing switching regulators using these newer devices.

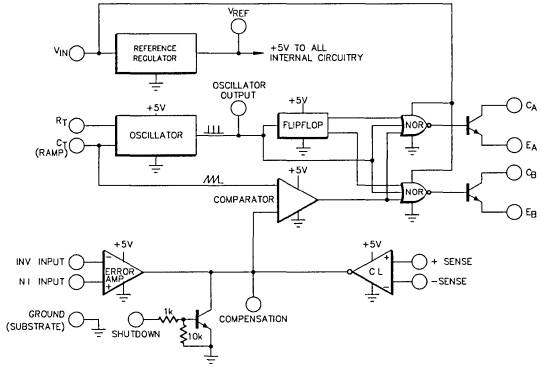


Figure 1. SG1524 Block Diagram

## INTEGRATED P.W.M. CONTROL CIRCUITS

Recognizing a rapidly growing market, many component suppliers have introduced new devices designed specifically for switching regulator applications. These include faster power transistors with improved S.O.A., low E.S.R. electrolytic capacitors, hybrid power devices which include a matched commutating diode, and monolithic IC control devices such as the SG124[1] which contain all of the P.W.M. control circuitry in a single 16-pin, dual-in-line package.

From the block diagram shown in Figure 1, it can be seen that the SG1524 contains the elements necessary to implement either single-ended switching regulators or DC to DC converters of several different configurations. This device includes a voltage reference, error amplifier, constant frequency oscillator, pulse width modulator, pulse steering logic, dual alternating output switches, and current limiting and shutdown circuitry. Since many of the different types of applications for this IC have been discussed earlier[1] it should suffice to review only two of the more common usages as shown in Figures 2 and 3.



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The single-sided regulator of Figure 2 is unique because of its simplicity. This circuit combines an SG1524 with an SM625 hybrid to build a 5 volt, 5amp regulator with all the semiconductor devices contained in only two packages. This circuit has an efficiency of over 70% with an input voltage range of 20 to 30 volts, 0.1% line and load regulation, and some added benefits of constant frequency operation and short circuit protection.

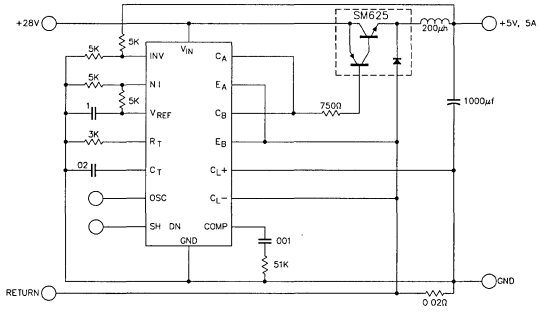



Figure 2. SG1524 Single - Ended Switching Regulator

Figure 3 shows the same 5-volt, 5amp output requirement met this time with a DC to DC converter. The use of high speed transistors and Schottky rectifiers keep the efficiency more than 80% - significant for a low-voltage output - while maintaining all the other benefits included in the single-ended circuit.

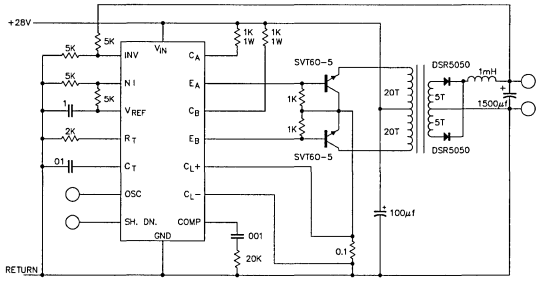



Figure 3. SG1524 Regulating DC - DC Converter

It should be recognized that the above circuits represent very basic applications of an IC control chip. Most practical power supply systems would probably incorporate many other features which may be accomplished by interfacing these IC's with a small amount of external circuitry to add characteristics such as: sift start, oscillator synchronization, dead-band controls, additional current and/or voltage step-up stages, input-output isolation, remote overvoltage or overload shutdown, and response modifying circuitry. It is this latter subject we wish to explore more fully below.

## SWITCHING REGULATOR CONTROL

The basic switching regulator control loop which applies to the most common forms of implementation is illustrated in Figure 4. In analyzing this control loop stability, the obvious immediate problem is the transfer function of the P.W.M. and output stage. A detailed and accurate analysis of the nonlinear characteristics of this stage is an extremely difficult and complex task if one is to account for all the parameters which could possibly be a factor. [2,3,4] On the other hand, if this stage could be assumed to have a linear transfer function, analysis becomes a relatively simple application of basic feedback theory.

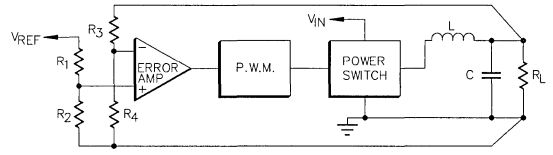



Figure 4. Basic Regulating Control Loop

A significance of the SG1524 is that it uses a design approach which makes a linear assumption accurate enough for most applications. The fact that this device features constant frequency operation, a linear-slope ramp for P.W.M., and fast-response logic and output circuitry all contribute to minimizing the errors associated with a linear assumption. Of course, there are factors external to the IC which could destroy this assumption. Such things as excessive delay in the switching transistors, parasitic ringing or oscillation in the power stages, or nonlinear operation of the magnetics could all cause a resultant nonlinear performance. A first exercise for the designer, then, is to confirm linear operation of the P.W.M. and output stages of his regulator by evaluating his early breadboard models.

## OUTPUT STAGE ANALYSIS

The pulse width modulation is accomplished in the SG1524 by comparing the output of the error amplifier with a linear ramp, or saw-tooth signal from the oscillator. Because the comparator has both high gain and high output impedance, and the error amplifier has a high output impedance, this node (pin-9) becomes a very convenient place for inserting a test signal. A voltage source applied as shown in Figure 5 will completely override the error amplifier and essentially open the loop without actually breaking any connections. In addition, the test signal is easily managed because the voltage gain from this point to the output is relatively low. (A voltage level on pin 9 of from 1 to 4 volts will change the pulse width from zero to maximum which will yield zero to maximum output voltage.)

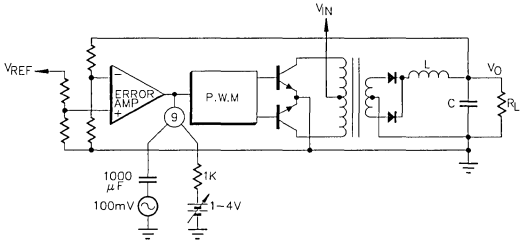



Figure 5. Measuring Output Stage Transfer Function

In experimentally attempting to confirm satisfactory operation of the output stages, the designer hopes to prove that a linear equivalent circuit model is valid for reasonable analysis. One such model as proposed by Middlebrook[5] is shown in Figure 6. This model describes the overall AC and DC transfer function and input and output impedances in terms of the duty cycle and modulation constant. This model assumes that the effects of operating frequency, switching delays, and parasitic elements are well above the frequencies of interest as defined by the output LC filter.

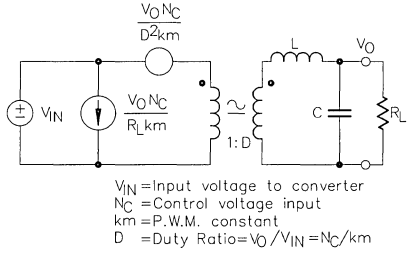



Figure 6. Linear Equivalent Circuit

Values for the inductor and capacitor are normally calculated on the basis of output ripple current and voltage as follows:

$$L = \frac{V_{IN} f(\Delta_{IL})}{V_O(V_{IN} - V_O)}$$

and

$$C = \frac{V_{IN} f(\Delta_{IL})}{8Lf^2 V_{IN}(\Delta V_O)}$$

where:

$V_{IN}$ = peak input voltage to the indicator
$V_O$ = output across the capacitor
$f$ = switching frequency
$\Delta I_L$ = peak - to - peak current variation in the inductor
$\Delta V_O$ = peak - to - peak ripple voltage across the capacitor

Note that the actual ripple voltage at the output of the filter will be $\Delta V_O$, plus $\Delta I_L$ times the capacitor E. S. R.

Regardless of the requirements for minimizing the output ripple, an additional requirement on the filter is that its cutoff frequency will be well below the switching frequency if our original goal of simple linear analysis is to be met. Specifically, the switching operation introduces a second order lag at one-half the switching frequency and for the output filter to dominate, its cutoff should be at least an order of magnitude below that number or

$$\frac{1}{2\pi\sqrt{LC}} \leq \frac{f}{20}$$

To verify the performance of the resultant hardware, a Bode plot of the output stage response can be most meaningful. Ideally, a plot as shown in Figure 7 should show a flat response to the filter cutoff and then a linear 12dB/octave rolloff with a 180° phase shift.

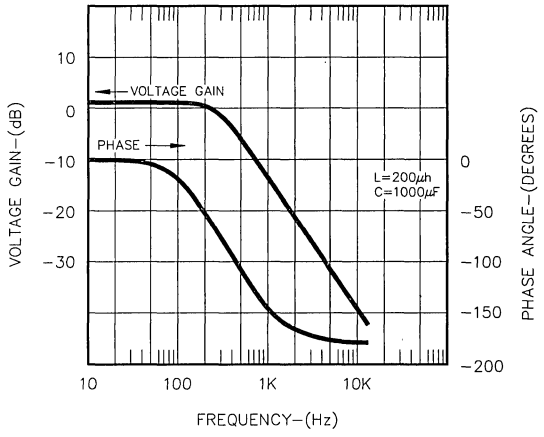



Figure 7. Linaear Output Stage Response

By making these plots with varying input voltage and load current, factors affecting stability such as leakage inductance, capacitor E.S.R., and either saturation or discontinuous operation of the magnetics may be evaluated over the operating conditions of interest. Figure 8 shows typical plots with less than ideal component parameters. With the characteristics of the output stage defined, attention can be turned to the error amplifier to develop an equalizing network which will allow satisfactory closing of the loop.

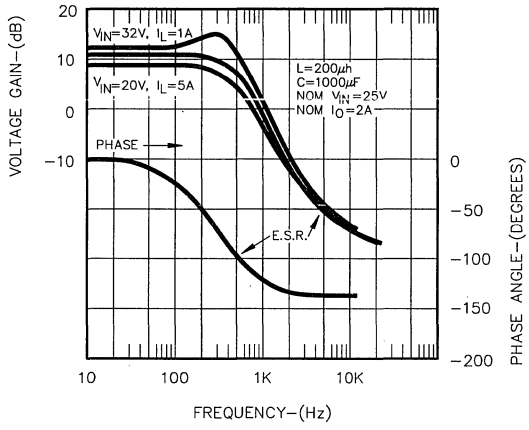



Figure 8. Measured Output Stage Response

## ERROR AMPLIFIER COMPENSATION

The error amplifier contained within the SG1524 is a transconductance amplifier in that it has a high-impedance, current source output. The gain is a function of the output loading and can be reduced from a nominal 80dB by shunt resistance as shown in Figure 9. Note also in Figure 9 that the uncompensated amplifier has a single pole at 300Hz and 90° of phase shift. The unity gain cross-over frequency is 3MHz and the large scale slew rate is 0.5 volt per microsecond.

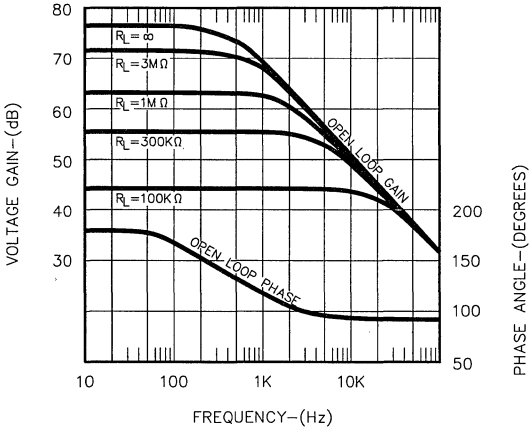



Figure 9. SG1524 Single - Ended Switching Regulator

This type of amplifier can be compensated in two ways: The compensation network can go from the output to ground so it can be connected from output back to the inverting input.[6] In the first case the voltage gain is:

$$A_V = gmZ_c = \frac{2kT}{8I_cZ_c} \approx 0.002Z_c$$

where $Z_c$ is the complex compensation network impedance. If a feedback approach is used, the gain is:

$$AV = \frac{Z_c}{Z_s}$$

where $Z_s$ is the source impedance driving the input. In cases where relatively low impedances are desired in a feedback network, it may be necessary to buffer the high output impedance of the error amplifier. Figure 10c shows the use of an external emitter follower to provide a low driving impedance for the feedback network.

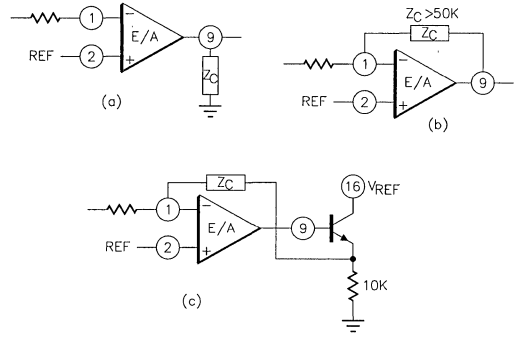



Figure 10. Error Amplifier Compensation Networks

To stabilize the overall regulator feedback loop of Figure 4, it should be apparent that the uncompensated loop contains at least two poles in the output filter and one more in the error amplifier, a situation which typically results in significant gain remaining when the total loop phase equals 360°. One of the simplest compensation schemes is to convert the error amplifier to an integrator by adding a single dominate pole at a frequency so low that the loop gain falls below unity well before the cutoff frequency of the output filter. While this approach yields a stable closed loop gain as shown in Figure 11, the response to disturbances is very slow. For example, the waveforms of Figure 12 show the response to a 20%, or one amp, step change in load to the circuit of Figure 3 when compensated with a 0.2μfd capacitor around the error amplifier.

If instead of slowing down the error amplifier, a zero, or lead network is added to cancel one of the output filter poles, we can keep the total loop phase less than 360° to well beyond the output filter cutoff.

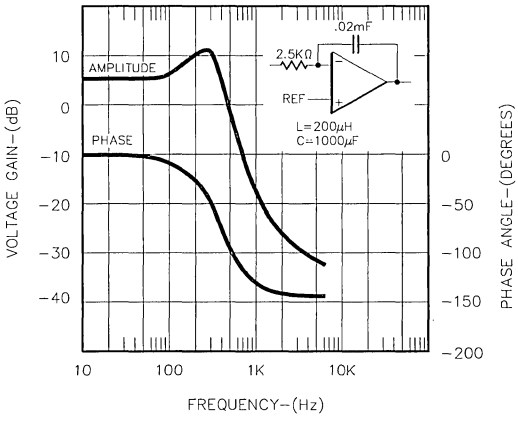



Figure 11. Closed Loop Frequency Response

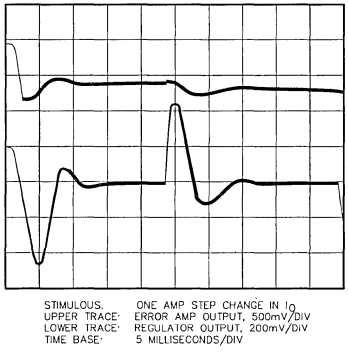



Figure 12. Integrator Compensation Step Response

Figure 13 shows a circuit for accomplishing this by moving the amplifier pole lower in frequency and adding a zero at the output filter cutoff frequency. Figure 14 shows the effects of this network on the Bode plot of the error amplifier, and Figure 15 indicates the improvement in recovery from the same one-amp load change. Note how the output of the error amplifier overshoots to give a boost to the output.

Even faster response can be achieved by providing additional lead networks. For example, another zero may be added by bypassing the sense feedback resistor. As can be seen in Figure 16, this greatly improves loop response but offers the hazard of coupling ripple noise directly into the error amplifier.

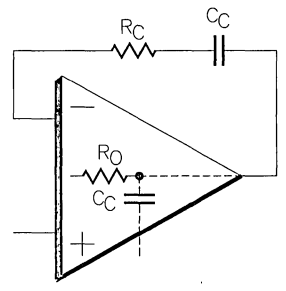



Figure 13. Series RC Phase Compensation

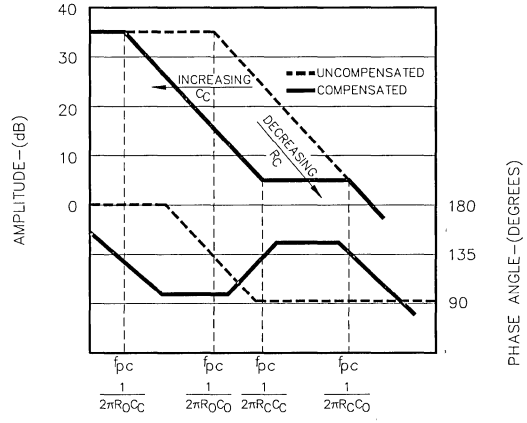



Figure 14. Phase Compensated Bode Plot

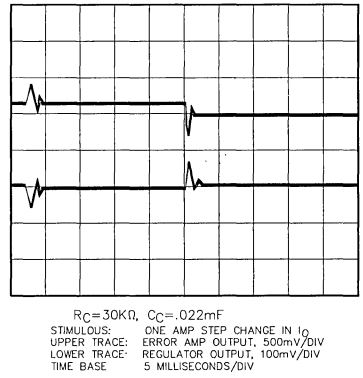
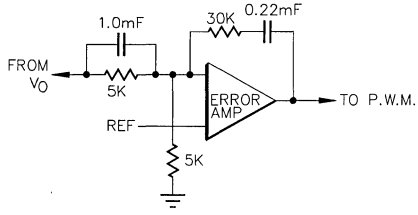



Figure 15. Phase Compensated Step Response

**TWO LOOP CONTROL**

From the examples presented above, it should be apparent that the integration method of error amplifier compensation provides good stability by making the dominate pole so low in frequency that variations in all other circuit parameters become inconsequential. This technique also provides high accuracy at DC where high gain can be used and is the type of feedback one would want to take directly from the output of a regulator since a user might add additional external capacitance, thereby changing the output filter characteristics. Another reason for using single-pole compensation is to accomodate the use of a two-stage output filter which can add phase shifts well beyond 180°.



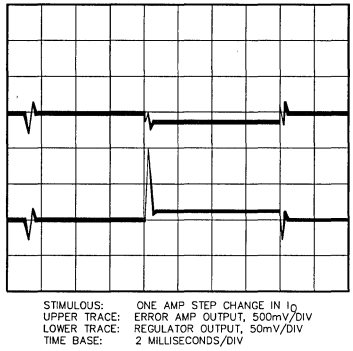




Figure 16. Double Zero Compensated Step Response

The problem of poor response can then be accommodated by adding a differentiated signal taken from somewhere else in the loop. If the time constants and gain factors are properly selected, the differentiated signal can compensate for the error in the integrated signal taken from the regulated output.

**SUMMARY**

Although integrated circuit controllers for switching supplies have removed much of the circuit complexity from this type of regulator, the dynamic analysis of the control loop must still be optimized for each application. This optimization is made easier, however, if a linear approximation of the switching stages can be shown to be valid. The SG1524 controller offers benefits in this regard as it does provide a linear transfer function through its pulse width modulation scheme. Therefore, experimental techniques can be used to simply confirm proper operation of the power switches and output filter.

With a linear output stage, conventional feedback analysis can be used to define the best equalizing network achieving a compromise between stability and fast response. In some cases it may even be desirable to provide separate signal paths for these two parameters but this, too, can be adapted to the SG1524 controller with a minimum of external circuitry.

Obviously, no recipes for optimum performance have been provided herein. Only a few directions which, it is hoped, will point the way toward the development of specific solutions for specific applications.

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