# INTEGRATED CIRCUITS FOR STORAGE PRODUCTS

• Read/Write Products • Pulse Detectors • Programmable Electronic Filters •

• Servo Motor Drivers • Servo Demodulators • Data Recovery •

• Data Separators • Servo Controllers • Time Base Generators •

• AT & SCSI Controllers • Read Channel Combos • Motor Speed Controllers •

# 1993 DATA BOOK

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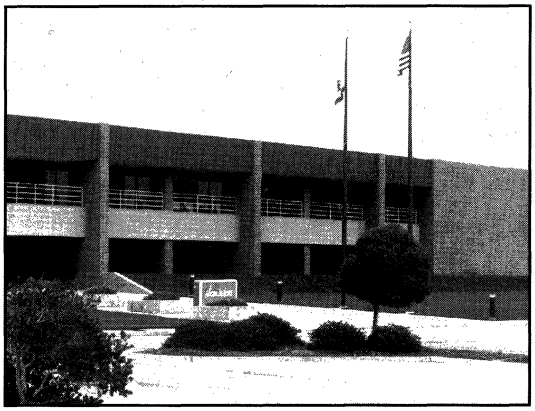
A TDK Group Company

# The Company



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# Table of Contents



**Target, Advanced and Preliminary Information**
In this data book the following conventions are used in designating a data sheet "Target," "Advanced" or "Preliminary":

**Target Specification–**
The target specification is intended as an initial disclosure of specification goals for the product. Product is in first stages of design cycle.

**Advance Information–**
Indicates a product still in the design cycle, undergoing testing processes, and any specifications are based on design goals only. Do not use for final design.

**Preliminary Data–**
Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

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# Index



* Data Sheet available upon request.

# Index (Continued)



* Data Sheet available upon request.

# Numerical Index



* Data Sheet available upon request

## Discontinued Parts List

The following parts are no longer supplied or supported by Silicon Systems. Please note alternate sources.

| Part # | Alternate Source | Part # | Alternate Source |
|---|---|---|---|
| SSI 32C260 | Cirrus SH 260 | SSI 32H4631/4632 | None |
| SSI 32C261 | None | SSI 32P3010 | None |
| SSI 32C263 | None | SSI 32P4730 | None |
| SSI 32C4650 | Cirrus SH 266 | SSI 32P4620/4622 | SSI 32P4720/4721 |
| SSI 32C4651 | Adaptec AIC 300 | SSI 32P5411B | None |
| SSI 32C9000 | None | SSI 32P546 | None |
| SSI 32C9010 | None | SSI 32P5481 | None |
| SSI 32C4010 | None | SSI 32P5482 | None |
| SSI 32D4420 | None | SSI 34R575 | None |
| SSI 32F8000 | SSI 32F8001 | | |

# STORAGE PRODUCTS REFERENCE

| Device Number | Head Type | Number of Channels | Max Input Noise (nV/ Hz) | Max Input Capacitance (pF) | Read Gain (typ) | Write Current Range (mA) | Power Supplies (V) | Write Data Ports | Min. Head Swing (V) |
|---|---|---|---|---|---|---|---|---|---|
| **HDD READ/WRITE AMPLIFIERS** | | | | | | | | | |
| SSI 32R117/117R | 3 Terminal | 2, 4, 6 | 2.1 | 20 | 100 | 10 to 50 | +5, +12 | TTL | 8.0 (0-pk) |
| SSI 32R501/501R | 3 Terminal | 4, 6, 8 | 1.5 | 23 | 100 | 10 to 50 | +5, +12 | TTL | 7.5 (0-pk) |
| SSI 32R510A/510AR | 3 Terminal | 2, 4, 6 | 1.5 | 20 | 100 | 10 to 40 | +5, +12 | TTL | 7.0 (0-pk) |
| SSI 32R511/511R | 3 Terminal | 4, 6, 8 | 1.5 | 20 | 100 | 10 to 40 | +5, +12 | TTL | 7.0 (0-pk) |
| SSI 32R516 | 3 Terminal | 4, 6, 8 | 1.3 | 18 | 120 | 10 to 60 | +5, +12 | TTL | 7.0 (0-pk) |
| SSI 32R5161R | 3 Terminal | 10 | 1.3 | 18 | 150 | 10 to 60 | +5, +12 | TTL | 7.0 (0-pk) |
| SSI 32R1200/1201 | 3 Terminal | 2, 4 | 1.2 | 17 | 200 | 15 to 50 | +5 | TTL | 6.0 (0-pk) |
| SSI 32R1220/21/22 | 3 Terminal | 2, 4 | 0.8 | 17 | 250 | 15 to 40 | +5 | TTL | 6.0 (0-pk) |
| SSI 32R512/512R | 2 Terminal | 8, 9 | 0.85 | 35 | 150 | 10 to 40 | +5, +12 | TTL | 7.0 (pk-pk) |
| SSI 32R5121/5121R | 2 Terminal | 14 | 0.85 | 35 | 250 | 10 to 40 | +5, +12 | TTL | 7.0 (pk-pk) |
| SSI 32R521/521R | 2 Terminal | 6 | 0.9 | 65 | 150 | 20 to 70 | +5, +12 | TTL | 3.4 (pk-pk) |
| SSI 32R5211 | 2 Terminal | 6 | 0.9 | 65 | 250 | 20 to 70 | +5, +12 | TTL | 3.4 (pk-pk) |
| SSI 32R522 | 2 Terminal | 4, 6 | 1.0 | 32 | 100 | 6 to 35 | +5, +12 | TTL | 3.4 (pk-pk) |
| SSI 32R524R | 2 Terminal | 8 | 0.75 | 60 | 100 | 20 to 60 | +5, +12 | TTL | 7.0 (pk-pk) |
| SSI 32R525R | 2 Terminal | 4 | 0.8 | 35 | 150 | 25 to 40 | +5, −5 | Differential / Differential | 3.8 (pk-pk) |
| SSI 32R528R | 2 Terminal | 8, 9 | 0.85 | 35 | 150 | 10 to 40 | +5, +12 | Differential | 7.0 (pk-pk) |
| SSI 32R5281 | 2 Terminal | 14 | 0.85 | 35 | 250 | 10 to 40 | +5, +12 | Differential | 7.0 (pk-pk) |
| SSI 32R1510R | MR | 8 | 0.95 | 18 | 150 | 20 to 50 | +5, +12 | Differential | 8.0 (pk-pk) |
| SSI 32R2010R | 2 Terminal | 10, 16 | 0.84 | 26 | 150 | 10 to 25 | +5, +12 | Differential | 7.0 (pk-pk) |
| SSI 32R2015R | 2 Terminal | 16 | 0.84 | 26 | 150 | 10 to 25 | +5, +12 | TTL | 7.0 (pk-pk) |
| SSI 32R2020R/2021R | 2 Terminal | 2, 4, 10 | 0.8 | 20 | 300 | 5 to 35 | +5 | TTL | 4.2 (pk-pk) |
| SSI 32R2030A/2031A | 2 Terminal | 2, 4 | 0.85 | 35 | 250 | 10 to 35 | +5 | TTL | 3.4 (pk-pk) |
| SSI 32R2040 | 2 Terminal | 14 | 0.8 | 22 | 250 | 10 to 40 | +5, +12 | Differential | 7.0 (pk-pk) |
| SSI 32R2300/2300R/2310 | 2 Terminal | 4 | 0.75 | 20 | 200 | 3 to 25 | +3.3/+5 | TTL | 3.4 (pk-pk) |
| SSI 32R4610A/4611A | 2 Terminal | 2, 4, 8 | 0.85 | 35 | 200 | 10 to 35 | +5 | TTL | 3.4 (pk-pk) |

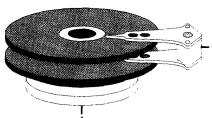
| Device Number | Circuit Function | Features |
|---|---|---|
| **HDD PULSE DETECTION** | | |
| SSI 32P541 | Read Data Processor | AGC, Amplitude & Time Pulse Qualification, RLL Compatible |
| SSI 32P541B | Read Data Processor | 32P541 pin compatible, 32P541A w/ Increased Data Rate to 24 Mbit/s |
| SSI 32P544 | Pulse Detector | 32P541-type Pulse Detector w/ Embedded Servo Electronics |
| SSI 32P547 | Pulse Detector | 32P544-type Pulse Detector w/ Filter Multiplexer, Pulse Slimming Support |
| SSI 32P549 | Read Data Processor | 32P541 pin compatible, Low Power, +5V only, Enhanced Write to Read Recovery |
| SSI 32P5491 | Read Data Processor | 32P549 pin compatible, 5 mW Idle Mode power, Pd = 170 mW |
| SSI 32P3000/3001 | Pulse Detector / Programmable Filter | 64 Mb/s Pulse Detector w/9-27 MHz Bessel filter (3000), 8-24 MHz filter (3001), +5V only |
| SSI 32P3010/3013 | Pulse Detector / Programmable Filter | 48 Mb/s Pulse Detector w/9-27 MHz Bessel filter, 4-burst servo capture |
| SSI 32P3030 | Pulse Detector / Servo Demodulator | Pulse Detector w/2-burst servo demodulator, +5V only |
| SSI 32P3040 | Pulse Detector / Programmable Filter | 24-32 Mbit/s Pulse Detector w/2.5-13 MHz Bessel Filter, +5V only |

# STORAGE PRODUCTS REFERENCE

| Device Number | Circuit Function | Features |
|---|---|---|
| **HDD READ CHANNEL COMBINATION DEVICES** | | |
| SSI 32P548 | Pulse Detector / Data Synchronizer | 32P544-type w/ 2, 7 Synchronizer, Low Power, +5V only, <700 mW |
| SSI 32P5482 | Pulse Detector / Data Synchronizer | Low power 32P548-type device (350 mW), no Write Precompensation |
| SSI 32P4720 | Pulse Detector / Data Separator | 32P548-type + 1, 7 ENDEC, Window Shift, Power-down, 52-pin QFP, 650 mW |
| SSI 32P4721 | Pulse Detector / Data Separator | 32P4720 @12 to 24 Mbit/s, <700 mW |
| SSI 32P4730 | Complete Read Channel | Pulse Detector/Filter/Servo/Time Base/Data Separator, 24 Mbit/s <500 mW, 64 TQFP |
| SSI 32P4731 | Complete Read Channel | 4730 with separate A, B, C, D servo outputs |
| SSI 32P4741 | Complete Read Channel | 4731 with 16 to 48 Mbit/s operation |
| **HDD ACTIVE FILTERS** | | |
| SSI 32F8001/8002 | Programmable Channel Filter | 7-Pole Equiripple Active Filter, Programmable Cutoff Frequency / Pulse Slimming, 9 - 27 MHz (8001), 6-18 MHz (8002) |
| SSI 32F8011/8012 | Programmable Channel Filter | 7-Pole Bessel Active Filter, Programmable Cutoff Frequency / Pulse Slimming, (5 - 13 MHz, 8011) (6-15 MHz, 8012) |
| SSI 32F8013 | Programmable Channel Filter | 7-Pole Equiripple Active Filter, Programmable Cutoff Frequency / Pulse Slimming, 5 - 13 MHz |
| SSI 32F8020A | Programmable Channel Filter | 7-Pole Equiripple Active Filter, Programmable Cutoff Frequency / Pulse Slimming, 1.5 - 8 MHz |
| SSI 32F8030 | Programmable Channel Filter | 7-Pole Equiripple Active Filter, Programmable Cutoff Frequency / Pulse Slimming, 250 kHz - 2.5 MHz |
| SSI 32F8120 | Digitally Programmable Filter | 32F8020 with serial port and DACs |
| SSI 32F8130/31 | Digitally Programmable Filter | 32F8030 with serial port and DACs / 32F8131 = 150 kHz < Fc < 1.5 MHz |
| **HDD DATA RECOVERY** | | |
| SSI 32D4040 | Data Separator | Data Synchronizer / 1, 7 RLL ENDEC, 20 to 64 Mbit/s, Write Precompensation Window Shift |
| SSI 32D5321 | Data Separator | Data Synchronizer / 2, 7 RLL ENDEC 7.5 to 10 Mbit/s |
| SSI 32D5322A | Data Separator | Data Synchronizer / 2, 7 RLL ENDEC 7.5 to 13 Mbit/s |
| SSI 32D534A | Data Separator | Data Synchronizer / MFM ENDEC / Write Precompensation |
| SSI 32D5351A | Data Separator | Data Synchronizer / 2, 7 RLL ENDEC / Write Precompensation 8 to 18 Mbit/s |
| SSI 32D5362A | Data Separator | Data Synchronizer / 1, 7 RLL ENDEC / Write Precompensation 10 to 20 Mbit/s |
| SSI 32D5371/2 | Data Separator | Data Synchronizer / 1, 7 RLL ENDEC / Write Precompensation 12 to 24 Mbit/s |
| SSI 32D5373/4 | Data Separator | Data Synchronizer / 1, 7 RLL ENDEC / Write Precompensation 15 to 32 Mbit/s |
| SSI 32D539 | Data Separator | Data Synchronizer / 1.7 RLL ENDEC / 8-bit parallel NRZ 24 to 48 Mbit/s |
| SSI 32D5391/3 | Data Separator | Data Synchronizer / 1, 7 RLL ENDEC / Serial NRZ 24 to 40 Mbit/s |
| SSI 32D5392/4 | Data Separator | Data Synchronizer / 1, 7 RLL ENDEC / Dual-bit NRZ 24 to 48 Mbit/s |
| SSI 32D4660/1/2/3/4/5/6 | Time Base Generator | Up to 100 MHz Reference Frequency PLC for Constant Density Recording |
| **HDD HEAD POSITIONING** | | |
| SSI 32H101 | Preamplifier -Ferrite head | AV = 93, BW = 10 MHz, $e_n$ = 7.0 nV/ Hz |
| SSI 32H116A | Preamplifier -Thin Film head | AV = 250, BW = 20 MHz, $e_n$ = 0.94 nV/ Hz |
| SSI 32H523AR | Servo Read/Write | Single-channel Thin Film Read/Write Device |
| SSI 32H566R | Servo Read/Write | Single-channel Ferrite Read/Write Device |
| SSI 32H569 | Servo Motor Driver | Head Parking, Spindle Motor Braking |
| SSI 32H4633 | Combo Servo & Motor Speed Control | Embedded & Hybrid Servo, Hall Sensor-less Motor Speed Control, +5V only, 5400 RPM |
| SSI 32H6110 | Preamplifier -Thin Film head | AV = 250 or 300, BW = 20 MHz, $e_n$ = 0.85 nV/ Hz |
| SSI 32H6210 | Servo Demodulator | Di-bit Quadrature Servo Pattern; PLL Synchronization AGC Adjustment |
| SSI 32H6215 | Servo 5V Demodulator | 5V, 500 kHz frame rate Dedicated Servo Demodulator |
| SSI 32H6220 | Servo Controller | Track & Seek Mode Operation; Microprocessor Interface |
| SSI 32H6230 | Servo Motor Driver | Head Parking, Spindle Motor Braking, Voltage Clamp |

| Device Number | Circuit Function | Features |
|---|---|---|
| **HDD HEAD POSITIONING (Continued)** | | |
| SSI 32H6240 | Servo Motor Driver | Predriver for Bipolar H-bridge |
| SSI 32H6510 | Servo 5V Driver | Low Voltage Retract, 1 drivers |
| SSI 32H6520 | Servo Acquisition and D/A | 10-bit A/D D/A circuits, DSP interface |
| SSI 32H6810/6811 | Servo/Spindle 5V Driver | Combo driver supports 5V @ 0.5A, Voltage IN (6810), Serial Port with DACs (6811) |
| SSI 32H6830 | Servo/Spindle DSP Controller | DSP with 10-bit A/D & Dual D/A converters |
| **HDD SPINDLE MOTOR CONTROL** | | |
| SSI 32M593A | 3-Phase Motor Speed Control | ±0.037% Speed Accuracy; Bipolar Operation, 5 1/4" Drives |
| SSI 32M594 | 3-Phase Motor Speed Control | ±0.037% Speed Accuracy; Bipolar Operation, 3 1/2" & 5 1/4" Drives |
| SSI 32M595 | 3-Phase Sensor-less MSC | Hall Sensor-less; Motor Speed Control |
| SSI 32M7010 | Motor Speed Control 5V Driver | Hall Sensor-less; Commutator Digital Speed Control, 5V 1 Driver |
| SSI 32M7011 | Motor Speed Control 5V Commutator | Hall Sensor-less; Commutator, 5V 1 Driver |
| **HDD CONTROLLER/INTERFACE** | | |
| SSI 32C9001 | PC AT Combo Controller | 48 Mbit/s; High Performance AT Disk Controller |
| SSI 32C9020 | High Perf. SCSI Combo Controller | 48 Mbit/s; SCSI-2 compatible; Fast SCSI; single ended |
| SSI 32C9022 | Dual-bit High Perf. SCSI Combo Controller | Dual-bit NRZ, 48 Mbit/s; SCSI-2 compatible; Fast SCSI |
| SSI 32C9023 | Dual-bit High Perf. SCSI Combo Controller | Dual-bit NRZ, 72 Mbit/s; SCSI-2 compatible; Fast SCSI |
| SSI 32C9301 | High Perf. PC AT Combo Controller (3V, 5V) | 32 Mbit/s (3V), 48 Mbit/s (5V); LBA mode support |
| SSI 32C9302 | Dual-bit High Perf. PC AT Combo Cont. (3V, 5V) | Dual-bit NRZ, 32 Mbit/s (3V), 48 Mbit/s (5V); LBA mode support |
| SSI 32C9340 | PCMCIA/ATA Combo Controller (3V, 5V) | 32 Mbit/s (3V), 48 Mbit/s (5V) |
| SSI 32C9342 | Dual-bit PCMCIA/ATA Combo Controller (3V, 5V) | Dual-bit NRZ, 48 Mbit/s (3V/5V) |
| **FLOPPY DISK DRIVES** | | |
| SSI 34D441 | Data Separator | High Performance Analog Data Separator, NEC 765 Compatible |
| SSI34P553/5531 | Pulse Detector / Data Synchronizer | 0.6 - 1.6 Mbit/s data rate, MFM or 2, 7 RLL code |
| SSI 34B580 | Support Logic | Port Expander, Includes SA400 Interface Drivers/Receivers |

# WINCHESTER DISK DRIVE IC PRODUCT FAMILY



**MOTOR SPEED CONTROL**

SSI 32M593A
SSI 32M594
SSI 32M595
SSI 32M7010*
SSI 32M7011

**READ/ WRITE**

| 3-TERMINAL | 2-TERMINAL |
|---|---|
| SSI 32R117 | SSI 32R512 |
| SSI 32R117A | SSI 32R5121 |
| SSI 32R1200 | SSI 32R521 |
| SSI 32R501 | SSI 32R5211 |
| SSI 32R510A | SSI 32R522 |
| SSI 32R511A | SSI 32R524 |
| SSI 32R516 | SSI 32R525 |
| SSI 32R5161 | SSI 32R528 |
| SSI 32R1220 | SSI 32R2010 |
| | SSI 32R2015 |
| **MR HEAD PREAMP** | SSI 32R2020/21 |
| SSI 32R510R | SSI 32R2030/31 |
| | SSI 32R2040* |
| | SSI 32R2300/10* |
| | SSI 32R4610/11 |
| | SSI 32R4610A/11A |
| | SSI 32R5281 |

**PULSE DETECTOR**

SSI 32P3000
SSI 32P3001*
SSI 32P3010/13*
SSI 32P3030
SSI 32P3040
SSI 32P4720/1*
SSI 32P541
SSI 32P541B
SSI 32P544
SSI 32P547
SSI 32P548
Combo - SSI 32P5482
SSI 32P549/5491
Combo - SSI 32P4730*
Combo - SSI 32P4731*
Combo SSI 32P4733*
Combo - SSI 32P4741*
Combo SSI 32P4742*
Combo - SSI 32P4743*
SSI 34P553/5531

**DATA RECOVERY**

SSI 32D4040*
SSI 32D4660
SSI 32D4661
SSI 32D4662
SSI 32D4664*
SSI 32D4665
SSI 32D4666
SSI 32D5321
SSI 32D5322
SSI 32D534A
SSI 32D535
SSI 32D5351
SSI 32D5362A
SSI 32D5371
SSI 32D5372
SSI 32D5373
SSI 32D5374
SSI 32D539
SSI 32D5391*
SSI 32D5392*
SSI 32D5393*

**CONTROLLER**

SSI 32C9000
SSI 32C9001
SSI 32C9020
SSI 32C9022
SSI 32C9023*
SSI 32C9301*
SSI 32C9302*
SSI 32C9340*
SSI 32C9342*

**ACTIVE FILTER**

SSI 32F8001
SSI 32F8002
SSI 32F8011/12
SSI 32F8013*
SSI 32F8020/20A
SSI 32F8030
SSI 32F8120
SSI 32F8130/31

**SERVO PREAMP**

SSI 32H101
SSI 32H116A
SSI 32H523AR
SSI 32H566
SSI 32H6110

**HEAD POSITIONING**

SSI 32H569
SSI 32H6210
SSI 32H6220
SSI 32H6230
SSI 32H6240
SSI 32H6510
SSI 32H4631/33*
SSI 32H6215*
SSI 32H6510*
SSI 32H6520*
SSI 32H6810/11*
SSI 32H6830*

**µP**

**RAM**

** New or In Development*

Section 1

# HDD READ/WRITE AMPLIFIERS

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# SSI 32R512/512R
## 8 & 9-Channel Thin Film Read/Write Device

1

October 1992

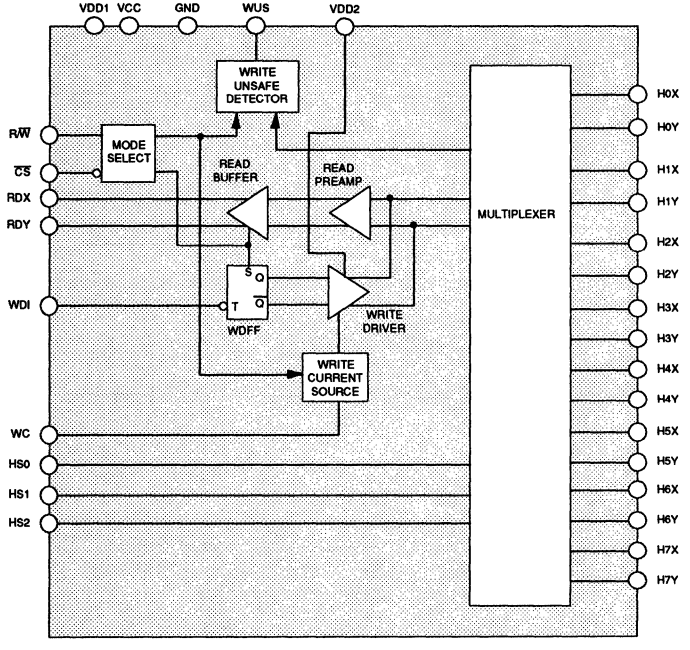
## DESCRIPTION

The SSI 32R512/512R Read/Write devices are bipolar monolithic integrated circuits designed for use with two terminal thin film recording heads. They provide a low noise read amplifier, write current control and data protection circuitry for eight or nine channels. Power supply fault protection is provided by disabling the write current generator during power sequencing. System write to read recovery time is significantly improved by controlling the read channel common mode output voltage shift in the write mode. They require +5V and +12V power supplies and are available in a variety of package configurations. A mirror image pinout option is available to simplify flex circuit layout in multiple R/W device applications. The SSI 32R512R option provides internal 1000Ω damping resistors.

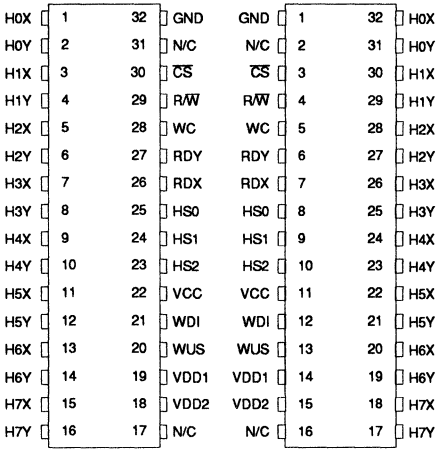
## FEATURES

- **High performance:**
  - **Read mode gain = 150 V/V**
  - **Input noise = 0.85 nV/√Hz max.**
  - **Input capacitance = 35 max.**
  - **Write current range = 10 mA to 40 mA**
  - **Head voltage swing = 7 Vpp**
  - **Write current rise time = 9 ns**
- **Enhanced system write to read recovery time**
- **Power supply fault protection**
- **Plug compatible to the SSI 32R501 & SSI 32R511**
- **Compatible with two & three terminal thin film heads**
- **Write unsafe detection**
- **+5V, +12V power supplies**
- **Mirror image pinout option**

## BLOCK DIAGRAM




## PIN DIAGRAM




**32-LEAD SOW** **32-LEAD SOW MIRROR**

CAUTION: Use handling procedures necessary for a static sensitive component.

# SSI 32R512/512R
# 8 & 9-Channel Thin Film Read/Write Device

## CIRCUIT OPERATION

The SSI 32R512 addresses up to nine two-terminal thin film heads providing write drive or read amplification. Head selection and mode control is accomplished with pins HSn, $\overline{CS}$ and R/$\overline{W}$, as shown in Tables 1 & 2. Internal resistor pullups, provided on pins $\overline{CS}$ and R/$\overline{W}$ will force the device into a non-writing condition if either control line is opened accidentally.

### WRITE MODE

The write mode configures the SSI 32R512 as a current switch and activates the Write Unsafe (WUS) detection circuitry. Write current is toggled between the X and Y direction of the selected head on each high to low transition on pin WDI, Write Data Input.

A preceding read operation initializes the Write Data Flip Flop (WDFF) to pass write current in the X-direction of the head.

The magnitude of the write current (0-pk) given by:

$$Iw = \frac{Vwc}{RWC}$$

where Vwc (WC pin voltage) = 1.65V ± 5%, is programmed by an external resistor RWC, connected from pin WC to ground. In multiple device applications, a single RWC resistor may be made common to all devices. The actual head current Ix, y is given by:

$$Ix,y = \frac{Iw}{1 + Rh/Rd}$$

where:
Rh = head resistance + external wire resistance, and
Rd = damping resistance.

Power supply fault protection improves data security by disabling the write current generator during a voltage fault or power supply sequencing. Additionally, the write unsafe detection circuitry will flag any of the conditions listed below as a high level on the open collector output pin, WUS. Two negative transitions on pin WDI, after the fault is corrected, are required to clear the WUS flag.

- WDI frequency too low
- Device not selected
- Device in read mode
- No write current

Power dissipation in Write Mode may be reduced by placing a resistor, Rw, between VDD1 and VDD2. The resistor value should be chosen such that Iw Rw ≤ 3.0V for an accompanying reduction of $(Iw)^2$ Rw in power dissipation. If a resistor is not used, VDD2 should be connected to VDD1. Note that Rw will also provide current limiting in the event of a head short.

### READ MODE

The read mode configures the SSI 32R512 as a low noise differential amplifier and deactivates the write current generator and write unsafe detection circuitry. The RDX and RDY outputs are emitter followers and are in phase with the "X" and "Y" head ports. These outputs should be AC coupled to the load. The RDX, RDY common mode voltage is maintained in the write mode, minimizing the transient between write mode and read mode, substantially reducing the write to read recovery time in the subsequent Pulse Detection circuitry.

### IDLE MODE

The idle mode deactivates the internal write current generator, the write unsafe detector and switches the RDX, RDY outputs into a high impedance state. This facilitates multiple device applications by enabling the read outputs to be wire OR'ed and the write current programming resistor to be common to all devices.

**TABLE 1: Mode Select**

| $\overline{CS}$ | R/$\overline{W}$ | MODE |
|---|---|---|
| 0 | 0 | Write |
| 0 | 1 | Read |
| 1 | 0 | Idle |
| 1 | 1 | Idle |

**TABLE 2: Head Select**

| HS3 | HS2 | HS1 | HS0 | HEAD |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 2 |
| 0 | 0 | 1 | 1 | 3 |
| 0 | 1 | 0 | 0 | 4 |
| 0 | 1 | 0 | 1 | 5 |
| 0 | 1 | 1 | 0 | 6 |
| 0 | 1 | 1 | 1 | 7 |
| 1 | 0 | 0 | 0 | 8 |

0 = Low level  1 = High level

## PIN DESCRIPTIONS

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| HS0 - HS3 | I | Head Select |
| $\overline{CS}$ | I | Chip Select: a low level enables the device |
| R/$\overline{W}$ | I | Read/Write: a high level selects Read mode |
| WUS | O* | Write Unsafe: Open collector output, a high level indicates an unsafe writing condition |
| WDI | I | Write Data In: a negative transition toggles the direction of the head current |
| H0X - H8X<br>H0Y - H8Y | I/O | X, Y Head Connections: Current in the X-direction flows into the X-port |
| RDX, RDY | O* | X, Y Read Data: differential read data output |
| WC | * | Write Current: used to set the magnitude of the write current |
| VCC | - | +5V Logic Circuit Supply |
| VDD1 | - | +12V |
| VDD2 | - | Positive Power Supply for Write current drivers |
| GND | - | Ground |

*When more than one R/W device is used, these signals can be wire OR'ed.

## ELECTRICAL SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS

| PARAMETER | | SYMBOL | VALUE | UNITS |
|---|---|---|---|---|
| DC Supply Voltage | | VDD1, 2 | -0.3 to +14 | VDC |
| | | VCC | -0.3 to +7 | VDC |
| Write Current | | Iw | 100 | mA |
| Digital Input Voltage | | Vin | -0.3 to VCC +0.3 | VDC |
| Head Port Voltage | | VH | -0.3 to VDD2 +0.3 | VDC |
| WUS Pin Voltage Range | | Vwus | -0.3 to +14 | VDC |
| Output Current | RDX, RDY | Io | -10 | mA |
| | WUS | Iwus | +12 | mA |
| Storage Temperature | | Tstg | -65 to +150 | °C |

**RECOMMENDED OPERATING CONDITIONS**

| PARAMETER | SYMBOL | VALUE | UNITS |
|---|---|---|---|
| DC Supply Voltage | VDD1 | 12 ± 10% | VDC |
| | VDD2 | VDD1 - 3.0 to VDD1 | VDC |
| | VCC | 5 ± 10% | VDC |
| Operating Temperature | Tj | +25 to +135 | °C |

**DC CHARACTERISTICS**
Unless otherwise specified, recommended operating conditions apply.

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|
| VDD1 Supply Current | Read Mode | - | - | 34 | mA |
| | Write Mode | - | - | 45 | mA |
| | Idle Mode | - | - | 15 | mA |
| VDD2 Supply Current | Read Mode | - | - | 200 | µA |
| | Write Mode | - | - | IW+0.4 | mA |
| | Idle Mode | - | - | 200 | µA |
| VCC Supply Current | Read Mode | - | - | 75 | mA |
| | Write Mode | - | - | 56 | mA |
| | Idle Mode | - | - | 60 | mA |
| Power Dissipation (Tj = +135°C) | Read Mode | - | - | 800 | mW |
| | Write Mode: Iw = 20 mA, VDD2 = VDD1 | - | - | 1000 | mW |
| | Write Mode: Iw = 40 mA, VDD1 - VDD2 = 3.0V | - | - | 1140 | mW |
| | Idle Mode | - | - | 500 | mW |
| Input Low Voltage (VIL) | | - | - | 0.8 | VDC |
| Input High Voltage (VIH) | | 2.0 | - | - | VDC |
| Input Low Current (IIL) | VIL = 0.8V | -0.4 | - | - | mA |
| Input High Current (IHL) | VIH = 2.0V | - | - | 100 | µA |
| WUS Output Low Voltage (VOL) | Iol = 8 mA | - | - | 0.5 | VDC |
| VDD Fault Voltage | | 8.5 | - | 10.0 | VDC |
| VCC Fault Voltage | | 3.5 | - | 4.2 | VDC |
| Head Current (HnX, HnY) | Write Mode, 0≤ VCC ≤3.5V<br>0 ≤ VDD1 ≤ 8.5V | -200 | - | +200 | µA |
| | Read/Idle Mode<br>0 ≤ VCC ≤ 5.5V<br>0 ≤ VDD1 ≤ 13.2V | -200 | - | +200 | µA |

**WRITE CHARACTERISTICS**
Unless otherwise specified, recommended operating conditions apply, Iw = 20 mA, Lh = 1.0 µH, Rh = 30Ω and f(WDI) = 5 MHz.

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|
| WC Pin Voltage (Vwc) | | 1.57 | 1.65 | 1.73 | V |
| Differential Head Voltage Swing | | 7 | - | - | Vpp |
| Unselected Head Current | | - | - | 1 | mA(pk) |
| Differential Output Capacitance | | - | - | 25 | pF |
| Differential Output Resistance | 32R512R | 800 | 1000 | 1350 | Ω |
| | 32R512 | 4 | - | - | kΩ |
| WDI Transition Frequency | WUS = low | 1.7 | - | - | MHz |
| Write Current Range | | 10 | - | 40 | mA |

**READ CHARACTERISTICS**
Unless otherwise specified, recommended operating conditions apply CL (RDX, RDY) < 20pF and RL (RDX,RDY) = 1 kΩ.

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|---|
| Differential Voltage Gain | | Vin=1mVpp @ 300 kHz | 125 | - | 175 | V/V |
| Bandwidth | -1dB | \|Zs\|<5Ω, Vin=1 mVpp @ 300 kHz | 25 | - | - | MHz |
| | -3dB | \|Zs\|<5Ω, Vin=1 mVpp @ 300 kHz | 45 | - | - | MHz |
| Input Noise Voltage | | BW = 15 MHz, Lh = 0, Rh = 0 | - | 0.62 | 0.85 | nV/√Hz |
| Differential Input Capacitance | | Vin = 1 mVpp, *f* = 5 MHz | - | - | 35 | pF |
| Differential Input Resistance | 32R512R | Vin = 1 mVpp, *f* = 5 MHz | 390 | - | - | Ω |
| | 32R512 | Vin = 1 mVpp, *f* = 5 MHz | 640 | - | - | Ω |
| Dynamic Range | | DC input voltage where gain falls to 90% of its 0 VDC value, Vin = VDC +0.5 mVpp, *f* = 5 MHz | -3 | - | 3 | mV |
| Common Mode Rejection Ratio | | Vin = 0 VDC+100 mVpp @ 5 MHz | 54 | - | - | dB |
| Power Supply Rejection Ratio | | 100 mVpp @ 5 MHz on VDD1<br>100 mVpp @ 5 MHz on VCC | 54 | - | - | dB |
| Channel Separation | | Unselected channels driven with 100 mVpp @ 5 MHz, Vin = 0 mVpp | 45 | - | - | dB |
| Output Offset Voltage | | | -360 | - | +360 | mV |
| RDX, RDY Common Mode Output Voltage | | Read Mode | 2.2 | 2.9 | 3.6 | VDC |
| | | Write Mode | - | 2.9 | - | VDC |
| Single Ended Output Resistance | | *f* = 5 MHz | - | - | 30 | Ω |
| Output Current | | AC Coupled Load, RDX to RDY | 3.2 | - | - | mA |

**5SWITCHING CHARACTERISTICS** (See Figure 1)
Unless otherwise specified, recommended operating conditions apply, Iw = 20 mA, Lh = 1.0 µH, Rh = 30Ω and $f$ (WDI) = 5 MHz.

| PARAMETER | CONDITIONS | MIN | MAX | UNITS |
|---|---|---|---|---|
| R/$\overline{W}$ | | | | |
| R/$\overline{W}$ to Write Mode | Delay to 90% of write current | - | 0.6 | µs |
| R/$\overline{W}$ to Read Mode | Delay to 90% of 100 mV 10 MHz Read signal envelope or to 90% decay of write current | - | 0.6 | µs |
| $\overline{CS}$ | | | | |
| $\overline{CS}$ to Select | Delay to 90% of write current or to 90% of 100mV 10MHz Read signal envelope | - | 0.6 | µs |
| $\overline{CS}$ to Unselect | Delay to 90% of write current | - | 0.6 | µs |
| HSn | | | | |
| HS0, 1, 2 to any Head | Delay to 90% of 100 mV 10 MHz Read signal envelope | - | 0.4 | µs |
| WUS | | | | |
| Safe to Unsafe - TD1 | | 0.6 | 3.6 | µs |
| Unsafe to Safe - TD2 | | - | 1 | µs |
| Head Current | | | | |
| Prop. Delay - TD3 | From 50% points, Lh=0µh, Rh=0Ω | - | 32 | ns |
| Asymmetry | WDI has 50% duty cycle and 1ns rise/fall time, Lh=0µh, Rh=0Ω | - | 1 | ns |
| Rise/Fall Time | 10% - 90% points, Lh=0µh, Rh=0Ω | - | 9 | ns |

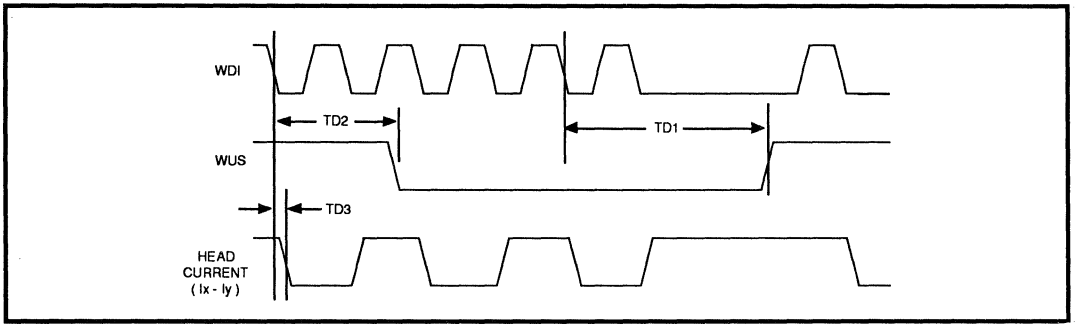



**FIGURE 1: Write Mode Timing Diagram**

## APPLICATIONS INFORMATION

The specifications, provided in the data section, account for the worst case values of each parameter taken individually. In actual operation, the effects of worst case conditions on many parameters correlate. Tables 3 & 4 demonstrate this for several key parameters. Notice that under the conditions of worst case input noise, the higher read back signal resulting from the higher input impedance can compensate for the higher input noise. Accounting for this correlation in your analysis will be more representative of actual performance.

**TABLE 3: Key Parameters Under Worst Case Input Noise Conditions**

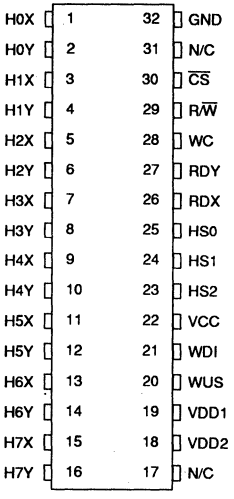
| PARAMETER | | Tj = 25°C | Tj = 135°C | UNITS |
|---|---|---|---|---|
| Input Noise Voltage (Max.) | | 0.70 | 0.85 | nV/√Hz |
| Differential Input Resistance (Min.) | 32R512R | 539 | 595 | Ω |
| | 32R512 | 1200 | 1500 | Ω |
| Differential Input Capacitance (Max.) | | 32 | 34 | pF |

**TABLE 4: Key Parameters Under Worst Case Input Impedance Conditions**

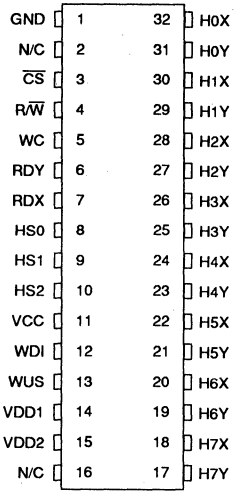
| PARAMETER | | Tj = 25°C | Tj = 135°C | UNITS |
|---|---|---|---|---|
| Input Noise Voltage (Max.) | | 0.58 | 0.71 | nV/√Hz |
| Differential Input Resistance (Min.) | 32R512R | 391 | 458 | Ω |
| | 32R512 | 643 | 846 | Ω |
| Differential Input Capacitance (Max.) | | 33 | 35 | pF |

# SSI 32R512/512R
# 8 & 9-Channel Thin Film Read/Write Device

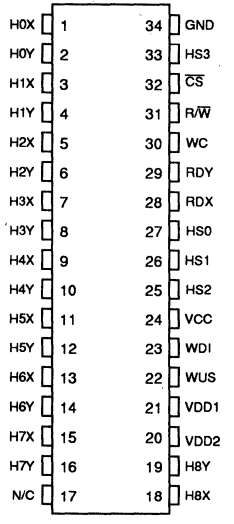
## PACKAGE PIN DESIGNATIONS (Top View)



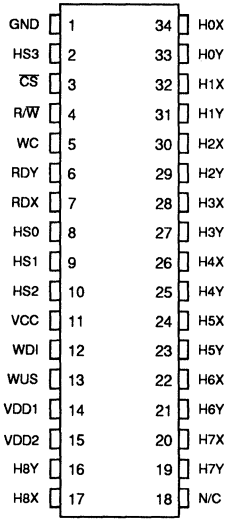

**8-Channel 32-Lead SOW**




**8-Channel 32-Lead SOW Mirror**




**9-Channel 34-Lead SOL**




**9-Channel 34-Lead SOL Mirror**

**THERMAL CHARACTERISTICS: θja**

| | |
|---|---|
| 32-Lead SOW | 55°C/W |
| 34-Lead SOL | 60°C/W |

## ORDERING INFORMATION

| PART DESCRIPTION | ORDER NO. | PKG. MARK |
|---|---|---|
| SSI 32R512 Read/Write IC | | |
| 8-Channel SOW | 32R512-8CW | 32R512-8CW |
| 9-Channel SOL | 32R512-9CL | 32R512-9CL |
| SSI 32R512R with Internal Damping Resistor | | |
| 8-Channel SOW | 32R512R-8CW | 32R512R-8CW |
| 9-Channel SOL | 32R512R-9CL | 32R512R-9CL |
| SSI 32R512M Mirror Image | | |
| 8-Channel SOW | 32R512M-8CW | 32R512M-8CW |
| 9-Channel SOL | 32R512M-9CL | 32R512M-9CL |
| SSI 32R512RM Mirror Image with Damping Resistor | | |
| 8-Channel SOW | 32R512RM-8CW | 32R512RM-8CW |
| 9-Channel SOL | 32R512RM-9CL | 32R512RM-9CL |



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**Notes:**

silicon systems®
A TDK Group Company

# SSI 32R5121/5121R
## 14-Channel Thin Film Read/Write Device

**Advance Information**

November 1991

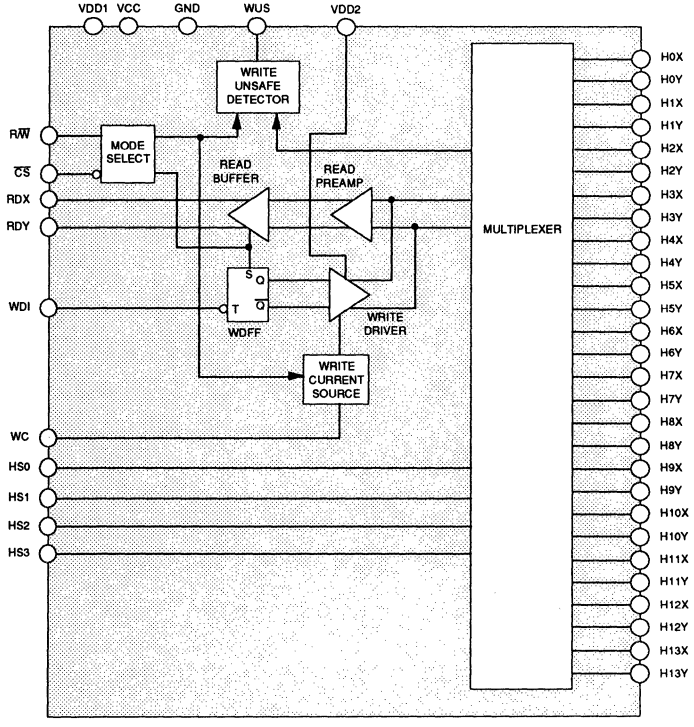
## DESCRIPTION

The SSI 32R5121/5121R Read/Write devices are bipolar monolithic integrated circuits designed for use with two terminal thin film recording heads. They provide a low noise read amplifier, write current control and data protection circuitry for up to 14 channels. Power supply fault protection is provided by disabling the write current generator during power sequencing. System write to read recovery time is significantly improved by controlling the read channel common mode output voltage shift in the write mode. They require +5V and +12V power supplies and are available in a variety of package configurations.The SSI 32R512R option provides internal 180Ω damping resistors.

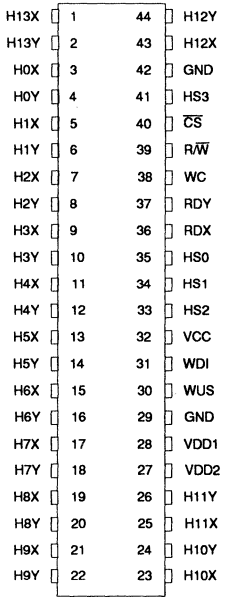
## FEATURES

- **High performance:**
  - **Read mode gain = 250 V/V**
  - **Input noise = 0.85 nV/√Hz max.**
  - **Input capacitance = 35 pF max.**
  - **Write current range = 10 mA to 40 mA**
  - **Head voltage swing = 7 Vpp**
  - **Write current rise time = 9 ns**
- **Enhanced system write to read recovery time**
- **Power supply fault protection**
- **Compatible with two & three terminal thin film heads**
- **Write unsafe detection**
- **+5V, +12V power supplies**

## BLOCK DIAGRAM




## PIN DIAGRAM




**44-LEAD SOM**

CAUTION: Use handling procedures necessary for a static sensitive component.

## CIRCUIT OPERATION

The SSI 32R5121 addresses up to 14 two-terminal thin film heads providing write drive or read amplification. Head selection and mode control is accomplished with pins HSn, $\overline{CS}$ and R/$\overline{W}$, as shown in Tables 1 & 2. Internal resistor pullups, provided on pins $\overline{CS}$ and R/$\overline{W}$ will force the device into a non-writing condition if either control line is opened accidentally.

### WRITE MODE

The write mode configures the SSI 32R5121 as a current switch and activates the Write Unsafe (WUS) detection circuitry. Write current is toggled between the X and Y direction of the selected head on each high to low transition on pin WDI, Write Data Input.

A preceding read operation initializes the Write Data Flip Flop (WDFF) to pass write current in the X-direction of the head, i.e., into the X-port.

The magnitude of the write current (0-pk) given by:

$$Iw = \frac{Vwc}{RWC}$$

where Vwc (WC pin voltage) = 1.65V ± 5%, is programmed by an external resistor RWC, connected from pin WC to ground. In multiple device applications, a single RWC resistor may be made common to all devices. The actual head current Ix, y is given by:

$$Ix,y = \frac{Iw}{1 + Rh/Rd}$$

where:
Rh = head resistance + external wire resistance, and
Rd = damping resistance.

Power supply fault protection improves data security by disabling the write current generator during a voltage fault or power supply sequencing. Additionally, the write unsafe detection circuitry will flag any of the conditions listed below as a high level on the open collector output pin, WUS. Two negative transitions on pin WDI, after the fault is corrected, are required to clear the WUS flag.

- WDI frequency too low
- Device not selected
- Open head
- Device in read mode
- No write current

Power dissipation in Write Mode may be reduced by placing a resistor, Rw, between VDD1 and VDD2. The resistor value should be chosen such that Iw Rw ≤ 3.0V for an accompanying reduction of $(Iw)^2$ Rw in power dissipation. If a resistor is not used, VDD2 should be connected to VDD1. Note that Rw will also provide current limiting in the event of a head short.

### READ MODE

The read mode configures the SSI 32R5121 as a low noise differential amplifier and deactivates the write current generator and write unsafe detection circuitry. The RDX and RDY outputs are emitter followers and are in phase with the "X" and "Y" head ports. These outputs should be AC coupled to the load. The RDX, RDY common mode voltage is maintained at the write mode valve, minimizing the transient between write mode and read mode, substantially reducing the write to read recovery time in the subsequent Pulse Detection circuitry.

### IDLE MODE

The idle mode deactivates the internal write current generator, the write unsafe detector and switches the RDX, RDY outputs into a high impedance state. This facilitates multiple device applications by enabling the read outputs to be wire OR'ed and the write current programming resistor to be common to all devices.

**TABLE 1: Mode Select**

| $\overline{CS}$ | R/$\overline{W}$ | MODE |
|---|---|---|
| 0 | 0 | Write |
| 0 | 1 | Read |
| 1 | 0 | Idle |
| 1 | 1 | Idle |

**TABLE 2: Head Select**

| HS3 | HS2 | HS1 | HS0 | HEAD |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 2 |
| 0 | 0 | 1 | 1 | 3 |
| 0 | 1 | 0 | 0 | 4 |
| 0 | 1 | 0 | 1 | 5 |
| 0 | 1 | 1 | 0 | 6 |
| 0 | 1 | 1 | 1 | 7 |
| 1 | 0 | 0 | 0 | 8 |
| 1 | 0 | 0 | 1 | 9 |
| 1 | 0 | 1 | 0 | 10 |
| 1 | 0 | 1 | 1 | 11 |
| 1 | 1 | 0 | 0 | 12 |
| 1 | 1 | 0 | 1 | 13 |

## PIN DESCRIPTION

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| HSO - HS3 | I | Head Select |
| $\overline{CS}$ | I | Chip Select: a low level enables the device |
| R/$\overline{W}$ | I | Read/Write: a high level selects Read mode |
| WUS | O* | Write Unsafe: Open collector output, a high level indicates an unsafe writing condition |
| WDI | I | Write Data In: a negative transition toggles the direction of the head current |
| H0X - H13X<br>H0Y - H13Y | I/O | X, Y Head Connections: Current in the X-direction flows into the X-port |
| RDX, RDY | O* | X, Y Read Data: differential read data output |
| WC | * | Write Current: used to set the magnitude of the write current |
| VCC | - | +5V Logic Circuit Supply |
| VDD1 | - | +12V |
| VDD2 | - | Positive Power Supply for Write current drivers |
| GND | - | Ground |

*When more than one R/W device is used, these signals can be wire OR'ed.

## ELECTRICAL SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS

| PARAMETER | | SYMBOL | VALUE | UNITS |
|---|---|---|---|---|
| DC Supply Voltage | | VDD1, 2 | -0.3 to +14 | VDC |
| | | VCC | -0.3 to +7 | VDC |
| Write Current | | Iw | 100 | mA |
| Digital Input Voltage | | Vin | -0.3 to VCC +0.3 | VDC |
| Head Port Voltage | | VH | -0.3 to VDD2 +0.3 | VDC |
| WUS Pin Voltage Range | | Vwus | -0.3 to +14 | VDC |
| Output Current | RDX, RDY | Io | -10 | mA |
| | WUS | Iwus | +12 | mA |
| Storage Temperature | | Tstg | -65 to +150 | °C |

### RECOMMENDED OPERATING CONDITIONS

| PARAMETER | SYMBOL | VALUE | UNITS |
|---|---|---|---|
| DC Supply Voltage | VDD1 | 12 ± 10% | VDC |
| | VDD2 | VDD1 - 3.0 to VDD1 | VDC |
| | VCC | 5 ± 10% | VDC |
| Operating Temperature | Tj | +25 to +135 | °C |

### DC CHARACTERISTICS

Unless otherwise specified, recommended operating conditions apply.

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|
| VDD1 Supply Current | Read Mode | - | 24 | 36 | mA |
| | Write Mode | - | 34 | 46 | mA |
| | Idle Mode | - | 11 | 16 | mA |
| VDD2 Supply Current | Read Mode | - | 0 | 200 | µA |
| | Write Mode | - | Iw | Iw + 0.4 | mA |
| | Idle Mode | - | 0 | 200 | µA |
| VCC Supply Current | Read Mode | - | 52 | 73 | mA |
| | Write Mode | - | 35 | 54 | mA |
| | Idle Mode | - | 43 | 58 | mA |
| Power Dissipation (Tj = +135°C) | Read Mode | - | - | 800 | mW |
| | Write Mode: Iw = 20 mA, VDD2 = VDD1 | - | - | 1000 | mW |
| | Write Mode: Iw = 40 mA, VDD1 - VDD2 = 3.0V | - | - | 1150 | mW |
| | Idle Mode | - | - | 500 | mW |
| Input Low Voltage (VIL) | | - | - | 0.8 | VDC |
| Input High Voltage (VIH) | | 2.0 | - | - | VDC |
| Input Low Current (IIL) | VIL = 0.8V | -0.4 | - | - | mA |
| Input High Current (IHL) | VIH = 2.0V | - | - | 100 | µA |
| WUS Output Low Voltage (VOL) | Iol = 8 mA | - | - | 0.5 | VDC |
| VDD Fault Voltage | | 8.5 | - | 10.0 | VDC |
| VCC Fault Voltage | | 3.5 | - | 4.2 | VDC |
| Head Current (HnX, HnY) | Write Mode, 0 ≤ VCC ≤ 3.5V 0 ≤ VDD1 ≤ 8.5V | -200 | - | +200 | µA |
| | Read/Idle Mode, 0 ≤ VCC ≤ 5.5V 0 ≤ VDD1 ≤13.2V | -200 | - | +200 | µA |

**WRITE CHARACTERISTICS**
Unless otherwise specified, recommended operating conditions apply, Iw = 20 mA, Lh = 500 nH, Rh = 30Ω and f(WDI) = 5 MHz.

| PARAMETER | CONDITIONS | MIN. | NOM | MAX | UNITS |
|---|---|---|---|---|---|
| WC Pin Voltage (Vwc) | | 1.57 | 1.65 | 1.73 | V |
| Differential Head Voltage Swing | Iw = 40 mA | 7 | - | - | Vpp |
| Unselected Head Current | | - | - | 1 | mA(pk) |
| Differential Output Capacitance | | - | - | 25 | pF |
| Differential Output Resistance | 32R5121R | 140 | 180 | 220 | Ω |
| | 32R5121 | 4K | - | - | Ω |
| WDI Transition Frequency | WUS = low | 1.7 | - | - | MHz |
| Write Current Range | | 10 | - | 40 | mA |

**READ CHARACTERISTICS**
Unless otherwise specified, recommended operating conditions apply CL (RDX, RDY) < 20pF and RL (RDX,RDY) = 1 kΩ.

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|---|
| Differential Voltage Gain | | Vin=1mVpp @ 300 kHz | 210 | 250 | 290 | V/V |
| Bandwidth | -1dB | \|Zs\|<5Ω, Vin=1 mVpp @ 300 kHz | - | 30 | - | MHz |
| | -3dB | \|Zs\|<5Ω, Vin=1 mVpp @ 300 kHz | 27 | 45 | - | MHz |
| Input Noise Voltage | | BW = 15 MHz, Lh = 0, Rh = 0 | - | 0.62 | 0.85 | nV/√Hz |
| Differential Input Capacitance | | Vin = 1 mVpp, f = 5 MHz | - | - | 35 | pF |
| Differential Input Resistance | 32R5121R | Vin = 1 mVpp, f = 5 MHz | 115 | - | - | Ω |
| | 32R5121 | Vin = 1 mVpp, f =5 MHz | 640 | - | - | Ω |
| Dynamic Range | | Peak-to-peak AC input voltage where gain falls to 90% of its small signal value, f = 5 MHz | 2.0 | - | - | mVpp |
| Common Mode Rejection Ratio | | Vin = 0 VDC+100 mVpp @ 5 MHz | 54 | - | - | dB |
| Power Supply Rejection Ratio | | 100 mVpp @ 5 MHz on VDD1<br>100 mVpp @ 5 MHz on VCC | 54 | - | - | dB |
| Channel Separation | | Unselected channels driven with 100 mVpp @ 5 MHz, Vin = 0 mVpp | 45 | - | - | dB |
| Output Offset Voltage | | | -600 | - | +600 | mV |
| RDX, RDY Common Mode | | Read Mode | 2.2 | 2.9 | 3.6 | VDC |
| Output Voltage | | Write Mode | - | 2.9 | - | VDC |
| Single Ended Output Resistance | | f = 5 MHz | - | - | 30 | Ω |
| Output Current | | AC Coupled Load, RDX to RDY | 3.2 | - | - | mA |

**SWITCHING CHARACTERISTICS** (See Figure 1)
Unless otherwise specified, recommended operating conditions apply, Iw = 20 mA, Lh = 500 nH, Rh = 30Ω and f(WDI) = 5 MHz.

| PARAMETER | CONDITIONS | MIN | MAX | UNITS |
|---|---|---|---|---|
| R/$\overline{W}$ | | | | |
| R/$\overline{W}$ to Write Mode | Delay to 90% of write current | - | 0.6 | µs |
| R/$\overline{W}$ to Read Mode | Delay to 90% of 100mV 10MHz Read signal envelope or to 90% decay of write current | - | 0.6 | µs |
| Write Current | | | | |
| WC Turn-on Time | Lr = 30Ω, Lh = 1µH, Iw = 20 mA | | 320 | ns |
| WC Turn-off Time | Lr = 30Ω, Lh = 1µH, Iw = 20 mA | | 160 | ns |
| $\overline{CS}$ | | | | |
| $\overline{CS}$ to Select | Delay to 90% of write current or to 90% of 100mV 10MHz Read signal envelope | - | 0.6 | µs |
| $\overline{CS}$ to Unselect | Delay to 90% of write current | - | 0.6 | µs |
| HSn | | | | |
| HS0, 1, 2 to any Head | Delay to 90 % of 100mV 10MHz Read signal envelope | - | 0.4 | µs |
| WUS | | | | |
| Safe to Unsafe - TD1 | | 0.6 | 3.6 | µs |
| Unsafe to Safe - TD2 | | - | 1 | µs |
| Head Current | | | | |
| Prop. Delay - TD3 | From 50 % points, Lh=0µh, Rh=0Ω | - | 32 | ns |
| Asymmetry | WDI has 50 % duty cycle and 1ns rise/fall time, Lh=0µh, Rh=0Ω | - | 1 | ns |
| Rise/Fall Time | 10% - 90% points, Lh=0µh, Rh=0Ω | - | 9 | ns |

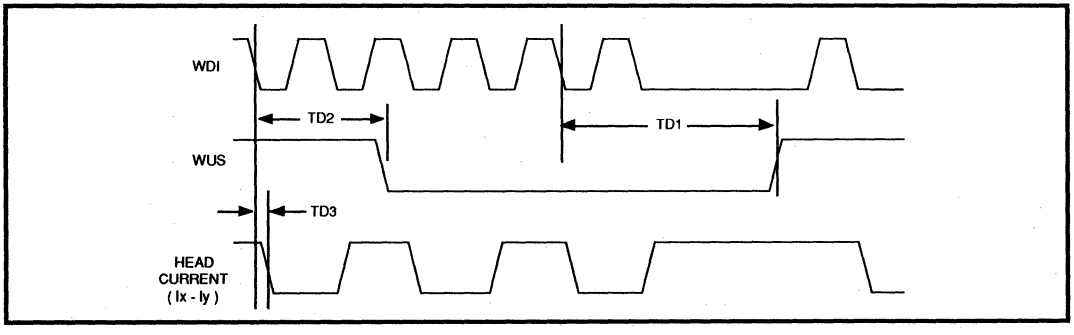



**FIGURE 1: Write Mode Timing Diagram**

## APPLICATIONS INFORMATION

The specifications, provided in the data section, account for the worst case values of each parameter taken individually. In actual operation, the effects of worst case conditions on many parameters correlate. Tables 3 & 4 demonstrate this for several key parameters. Notice that under the conditions of worst case input noise, the higher read back signal resulting from the higher input impedance can compensate for the higher input noise. Accounting for this correlation in your analysis will be more representative of actual performance.

**TABLE 3: Key Parameters Under Worst Case Input Noise Conditions**

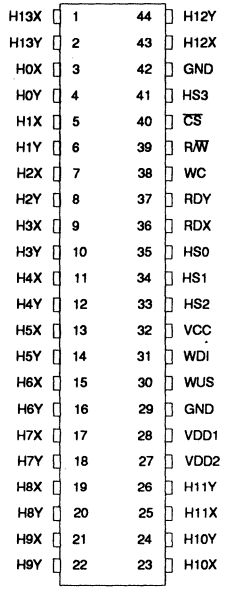
| PARAMETER | | Tj = 25°C | Tj = 135°C | UNITS |
|---|---|---|---|---|
| Input Noise Voltage (Max.) | | 0.70 | 0.85 | $nV/\sqrt{Hz}$ |
| Differential Input Resistance (Min.) | 32R5121R | 165 | 185 | Ω |
| | 32R5121 | 1200 | 1500 | Ω |
| Differential Input Capacitance (Max.) | | 32 | 34 | pF |

**TABLE 4: Key Parameters Under Worst Case Input Impedance Conditions**

| PARAMETER | | Tj = 25°C | Tj = 135°C | UNITS |
|---|---|---|---|---|
| Input Noise Voltage (Max.) | | 0.58 | 0.71 | $nV/\sqrt{Hz}$ |
| Differential Input Resistance (Min.) | 32R5121R | 115 | 125 | Ω |
| | 32R5121 | 640 | 850 | Ω |
| Differential Input Capacitance (Max.) | | 33 | 35 | pF |

# SSI 32R5121/5121R
# 14-Channel Thin Film Read/Write Device

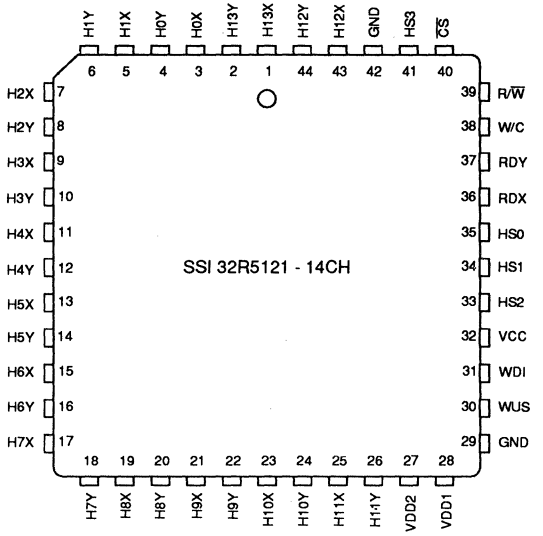
## PACKAGE PIN DESIGNATIONS
(Top View)




**44-Pin SOM**

## THERMAL CHARACTERISTICS: Øja

| | |
|---|---|
| 44-Lead SOL | 50°C/W |
| 44-PLCC | 60°C/W |




**44-Pin PLCC**

**Advance Information:** Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.



Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 573-6000, FAX (714) 573-6914

# SSI 32R516/516R
## 4, 6, 8-Channel Ferrite/MIG Read/Write Device

December 1992

## DESCRIPTION

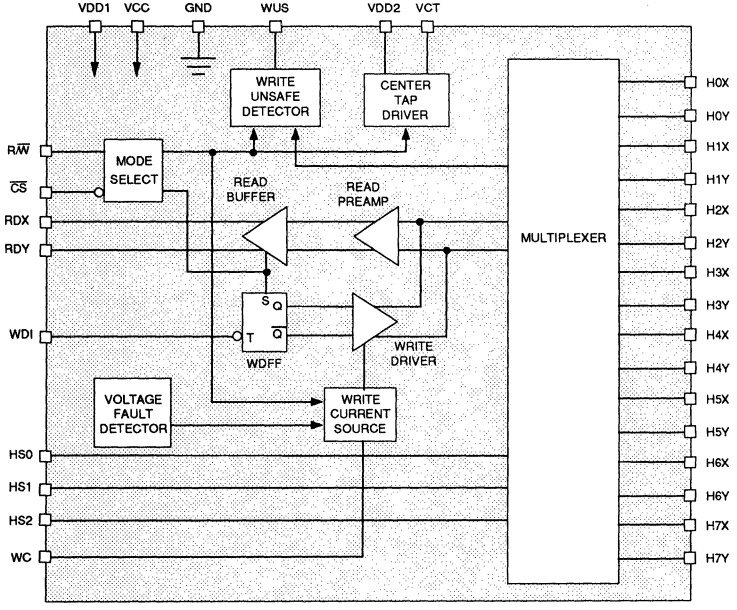
The SSI 32R516 is a bipolar monolithic integrated circuit designed for use with a center-tapped ferrite or MIG recording heads. The SSI 32R516 offers the performance upgrades of the SSI 32R511 along with improved head port characteristics and increased read gain. It provides a low noise read path, write current control, and data protection circuitry for as many as 8 channels. The SSI 32R516 requires +5V and +12V power supplies and is available in a variety of packages.

The SSI 32R516R performs the same function as the SSI 32R516 with the addition of internal 650Ω damping resistors. The SSI 32R516M and SSI 32R516RM are functionally equivalent to the SSI 32R516 and SSI 32R516R however, they have the mirror image pin arrangement to simplify layout when using multiple devices.

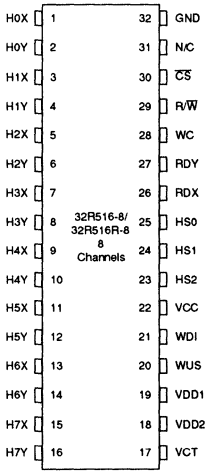
## FEATURES

- **High performance**
  - **Read mode gain = 120 V/V**
  - **Input noise = 1.3 nV/√Hz maximum**
  - **Input capacitance = 18 pF**
  - **Write current range = 10 mA to 60 mA**
- **Enhanced system write to read recovery time**
- **Power supply fault protection**
- **Pin compatible with the SSI 32R501 & SSI 32R511**
- **Designed for center-tapped ferrite or MIG heads**
- **Programmable write current source**
- **Easily multiplexed for larger systems**
- **Includes write unsafe detection**
- **TTL compatible control signals**
- **+5V, +12V power supplies**
- **Mirror image pin arrangements**

## BLOCK DIAGRAM




## PIN DIAGRAM




**32-Lead SOW**

CAUTION: Use handling procedures necessary for a static sensitive component.

## CIRCUIT OPERATION

The SSI 32R516 gives the user the ability to address up to 8 center-tapped ferrite heads and provide write drive or read amplification. Head selection and mode control is accomplished using the HSn, $\overline{CS}$ and R/$\overline{W}$ inputs as shown in tables 1 & 2. Internal pullups are provided for the $\overline{CS}$ & R/$\overline{W}$ inputs to force the device into a non-writing condition if either control line is opened accidentally.

**TABLE 1: Mode Select**

| $\overline{CS}$ | R/$\overline{W}$ | MODE |
|---|---|---|
| 0 | 0 | Write |
| 0 | 1 | Read |
| 1 | X | Idle |

**TABLE 2: Head Select**

| HS2 | HS1 | HS0 | HEAD |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 2 |
| 0 | 1 | 1 | 3 |
| 1 | 0 | 0 | 4 |
| 1 | 0 | 1 | 5 |
| 1 | 1 | 0 | 6 |
| 1 | 1 | 1 | 7 |

0 = Low level  1 = High level

### WRITE MODE

Taking both $\overline{CS}$ and R/$\overline{W}$ low selects write mode which configures the SSI 32R516 as a current switch and activates the Write Unsafe (WUS) detector circuitry. Write current is toggled between the X and Y side of the selected head on each high to low transition of the Write Data Input (WDI). Note that a preceding read mode selection initializes the Write Data Flip-Flop, WDFF, to pass write current through the "X" side of the head. The zero-peak write current magnitude is programmed by an external resistor Rwc from pin WC to GND and is given by:

Iw = K/Rwc, where K = Write Current Constant

The Write Unsafe detection circuitry monitors voltage transitions at the selected head connections and flags any of the following conditions as a high level on the Write Unsafe open collector output:

- Head open
- Head center tap open
- WDI frequency too low
- Device in read mode
- Device not selected
- No write current

Two negative transitions on WDI, after the fault is corrected, will clear the WUS flag.

To further assure data security a voltage fault detection circuit prevents application of write current during power loss or power sequencing.

To enhance write to read recovery time the change in RDX, RDY common mode voltage is minimized by biasing these outputs to a level within the read mode range when in write mode.

Power dissipation in write mode may be reduced by placing a resistor (RCT) between VDD1 & VDD2. The optimum resistor value is 82Ω x 60/Iw (Iw in mA). At low write currents (<15 mA) read mode dissipation is higher than write mode and RCT, though recommended, may not be considered necessary. In this case VDD2 is connected directly to VDD1.

### READ MODE

Taking $\overline{CS}$ low and R/$\overline{W}$ high selects read mode which configures the SSI 32R516 as a low noise differential amplifier for the selected head. The RDX and RDY outputs are driven by emitter followers and are in phase with the "X" and "Y" head ports. These outputs should be AC coupled to the load. The internal write current source is gated off in read mode eliminating the need for any external gating.

Read mode selection also initializes the Write Data Flip-Flop (WDFF) to pass write current through the "X" side of the head at a subsequent write mode selection.

### IDLE MODE

Taking $\overline{CS}$ high selects the idle mode which switches the RDX, RDY outputs into a high impedance state and deactivates the internal write current source. This facilitates multi-device installations by allowing the read outputs to be wire OR'ed and the write current programming resistor to be common to all devices.

## PIN DESCRIPTIONS

| NAME | I/O | DESCRIPTION |
|---|---|---|
| HS0-HS2 | I | Head Select |
| $\overline{CS}$ | I | Chip Select: a low level enables device |
| R/$\overline{W}$ | I | Read/Write: a high level selects read mode |
| WUS | O* | Write Unsafe: a high level indicates an unsafe writing condition |
| WDI | I | Write Data In: negative transition toggles direction of head current |
| H0X-H7X<br>H0Y-H7Y | I/O | X,Y head connections |
| RDX, RDY | O* | X, Y Read Data: differential read signal out |
| WC | * | Write Current: used to set the magnitude of the write current |
| VCT | - | Voltage Center Tap: voltage source for head center tap |
| VCC | - | +5V |
| VDD1 | - | +12V |
| VDD2 | - | Positive power supply for the center tap voltage source |
| GND | - | Ground |

*When more than one R/W device is used, these signals can be wire OR'ed.

## ELECTRICAL SPECIFICATIONS

**ABSOLUTE MAXIMUM RATINGS** (All voltages referenced to GND. Currents into device are positive.)

| PARAMETER | | VALUE | UNITS |
|---|---|---|---|
| DC Supply Voltage | VDD1 | -0.3 to +14 | VDC |
| DC Supply Voltage | VDD2 | -0.3 to +14 | VDC |
| DC Supply Voltage | VCC | -0.3 to +6 | VDC |
| Digital Input Voltage Range | VIN | -0.3 to VCC + 0.3 | VDC |
| Head Port Voltage Range | VH | -0.3 to VDD1 + 0.3 | VDC |
| WUS Pin Voltage Range | Vwus | -0.3 to +14 | VDC |
| Write Current Zero Peak | IW | 90 | mA |
| RDX, RDy Output Current | Io | -10 | mA |
| VCT Output Current | IVCT | -90 | mA |
| WUS Output Current | Iwus | +12 | mA |
| Storage Temperature Range | Tstg | -65 to 150 | °C |
| Lead Temperature PDIP, Flat Pack (10 sec Soldering) | | 260 | °C |
| Package Temperature PLCC, SO (20 sec Reflow) | | 215 | °C |

**RECOMMENDED OPERATION CONDITIONS**

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|---|
| DC Supply Voltage | VDD1 | | 10.8 | 12.0 | 13.2 | VDC |
| DC Supply Voltage | VCC | | 4.5 | 5.0 | 5.5 | VDC |
| Head Inductance | Lh | | 5 | | 10 | µH |
| Damping Resistor | RD | 32R516 only | 500 | | 2000 | Ω |
| RCT Resistor | RCT* | Iw = 60 mA | | 82 | | Ω |
| Write Current | IW | | 10 | | 60 | mA |
| Junction Temperature Range | Tj | | +25 | | +135 | °C |

*For Iw = 60 mA. At other Iw levels refer to Applications Information that follows this specification.

**DC CHARACTERISTICS**
(Unless otherwise specified, recommended operating conditions apply.)

**POWER SUPPLY**

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|
| VCC Supply Current | Read/Idle Mode | | | 30 | mA |
| | Write Mode | | | 30 | mA |
| VDD Supply Current | Idle Mode | | | 20 | mA |
| (sum of VDD1 and VDD2) | Read Mode | | | 40 | mA |
| | Write Mode | | | 20 + Iw | mA |
| Power Dissipation (Tj = +125°C) | Idle Mode | | | 400 | mW |
| | Read Mode | | | 620 | mW |
| | Write Mode, IW = 45 mA, RCT = 0Ω | | | 800 | mW |
| | Write Mode, IW = 45 mA, RCT = 110Ω | | | 610 | mW |
| | Write Mode, IW = 60 mA RCT = 82Ω | | | 680 | mW |

**DC CHARACTERISTICS** (continued)

**DIGITAL I/O**

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|---|
| VIL | Input Low Voltage | | | | 0.8 | VDC |
| VIH | Input High Voltage | | 2.0 | | VCC + 0.3 | VDC |
| IIL | Input Low Current | VIL = 0.8V | -0.4 | | | mA |
| IIH | Input High Current | VIH = 2.0V | | | 100 | µA |
| VOL | WUS Output Low Voltage | IOL = 8 mA | | | 0.5 | VDC |
| IOH | WUS Output High Current | VOH = 5.0V | | | 100 | µA |

**WRITE MODE**

| | | | | | | |
|---|---|---|---|---|---|---|
| Center Tap Voltage | VCT | Write Mode | | 6.9 | | VDC |
| Head Current (per side) | | Write Mode,<br>0 ≤ VCC ≤ 3.7V,<br>0 ≤ VDD1 ≤ 8.7V | -200 | | 200 | µA |
| Write Current Range | | | 10 | | 60 | mA |
| Write Current Constant "K" | | IW = 10 - 60 mA | 2.375 | | 2.80 | V |
| Iwc to Head Current Gain | | | | 0.99 | | mA/mA |
| Unselected Head Leakage Current | | | | | 85 | µA |
| RDX, RDY Output Offset Voltage | | Write/Idle Mode | -20 | | +20 | mV |
| RDX, RDY Common Mode Output Voltage | | Write/Idle Mode | | 5.5 | | VDC |
| RDX, RDY Leakage | | RDX, RDY = 6V<br>Write/Idle Mode | -100 | | 100 | µA |

**READ MODE**

| | | | | | |
|---|---|---|---|---|---|
| Center Tap Voltage | Read Mode | | 4.2 | | VDC |
| Head Current (per side) | Read or Idle Mode<br>0 ≤ VCC ≤ 5.5V<br>0 ≤ VDD1 ≤ 13.2V | -200 | | 200 | µA |
| Input Bias Current (per side) | | | | 45 | µA |
| Input Offset Voltage | Read Mode | -4 | | +4 | mV |
| Common Mode Output Voltage | Read Mode | 4.5 | 5.5 | 6.5 | VDC |

**DYNAMIC CHARACTERISTICS AND TIMING**
(Unless otherwise specified, recommended operating conditions apply and IW = 35 mA, Lh = 5 µH, Rd = 750Ω (32R516) only, f(WDI) = 5 MHz, CL(RDX, RDY) ≤ 35 pF.)

**WRITE MODE**

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|
| Differential Head Voltage Swing | | 7.0 | | | V(pk) |
| Unselected Head Transient Current | | | | 2 | mA(pk) |
| Differential Output Capacitance | | | | 15 | pF |
| Differential Output Resistance | 32R516 | 10K | | | Ω |
| | 32R516R | 430 | 650 | 870 | Ω |
| WDI Transition Frequency | WUS = low | 125 | | | kHz |

**READ MODE**

| | | | | | |
|---|---|---|---|---|---|
| Differential Voltage Gain | Vin = 1 mVpp @ 300 kHz, RL(RDX), RL(RDY) = 1 KΩ | 100 | 120 | 140 | V/V |
| Dynamic Range | AC Input Voltage, Vi, Where Gain Falls by 10%. V + f = 300 KHz | -3 | | | mVpp |
| Bandwidth (-3dB) | \|Zs\| < 5Ω, Vin = 1 mVpp | 30 | | | MHz |
| Input Noise Voltage | BW = 15 MHz, Lh = 0, Rh = 0 | | 1.0 | 1.3 | $nV/\sqrt{Hz}$ |
| Differential Input Capacitance | f = 5 MHz | | 14 | 18 | pF |
| Differential Input Resistance | 32R516, f = 5 MHz | 2K | | | Ω |
| Differential Input Resistance | 32R516R, f = 5 MHz | 350 | | 800 | Ω |
| Common Mode Rejection Ratio | Vcm = VCT + 100 mVpp @ 5 MHz | 50 | | | dB |
| Power Supply Rejection Ratio | 100 mVpp @ 5 MHz on VDD1, VDD2 or VCC | 45 | | | dB |
| Channel Separation | Unselected Channels: Vin=100 mVpp @ 5 MHz; Selected Channel: Vin = 0 mVpp | 45 | | | dB |
| Single Ended Output Resistance | f = 5 MHz | | | 30 | Ω |
| Output Current | AC Coupled Load, RDX to RDY | ±2.1 | | | mA |

**DYNAMIC CHARACTERISTICS AND TIMING** (continued)

**SWITCHING CHARACTERISTICS**

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|
| R/$\overline{W}$ To Write | Delay to 90% of Write Current | | .15 | .7 | µs |
| R/$\overline{W}$ to Read | Delay to 90% of 100 mV, 10 MHz Read Signal Envelope or to 90% decay of Write Current | | .25 | .7 | µs |
| $\overline{CS}$ to Select | Delay to 90% of Write Current or to 90% of 100 mV, 10 MHz Read Signal Envelope | | .2 | 1.0 | µs |
| $\overline{CS}$ to Unselect | Delay to 90% Decay of Write Current | | .1 | 1.0 | µs |
| HS0 - HS2 to any head | Delay to 90% of 100 mV, 10 MHz Read Signal Envelope | | .25 | 1.0 | µs |
| WUS, Safe to Unsafe - TD1 | Iw = 35 mA | 1.6 | | 8.0 | µs |
| WUS, Unsafe to Safe - TD2 | Iw = 35 mA | | | 1.0 | µs |
| Head Current (Lh = 0 µH, Rh = 0Ω) | | | | | |
| Prop. Delay - TD3 | From 50% Points | | | 25 | ns |
| Asymmetry | WDI has 50% Duty Cycle and 1ns Rise/Fall Time | | | 1 | ns |
| Rise/Fall Time | 10% - 90% Points | | | 20 | ns |

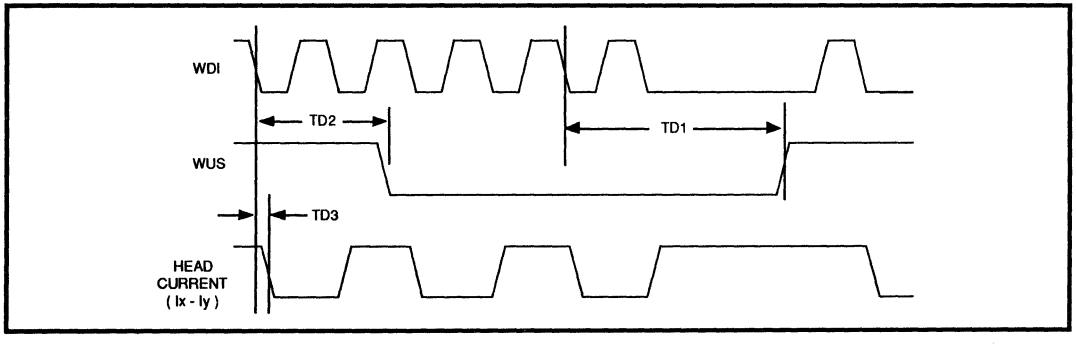
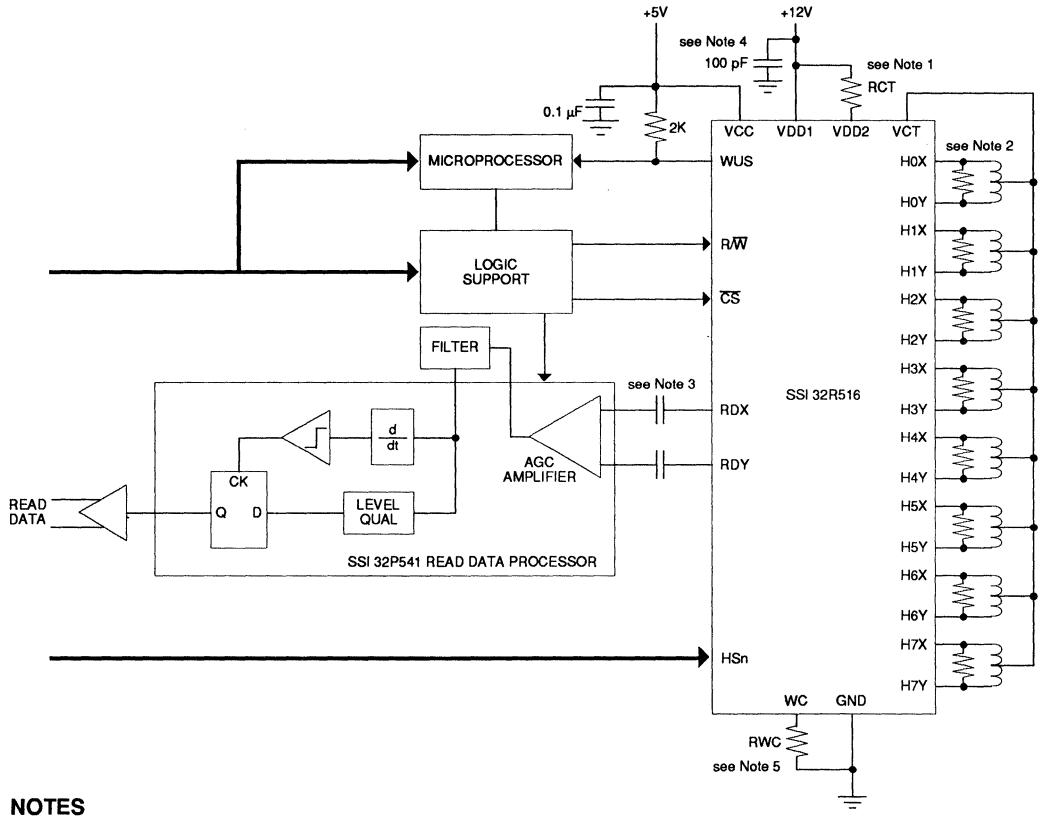



**FIGURE 1: Write Mode Timing Diagram**

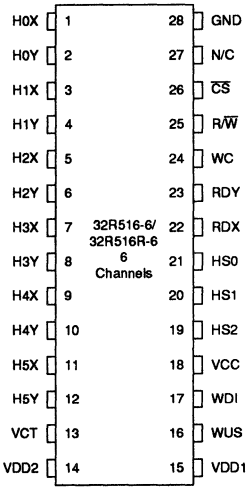



**NOTES**

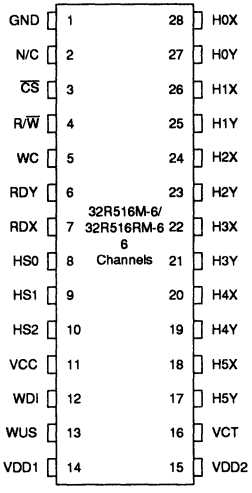
1. An external resistor, RCT, given by; RCT = 82 (60/Iw) where Iw is the zero-peak write current in mA, can be used to limit internal power dissipation. Otherwise connect VDD2 to VDD1.
2. Damping resistors not required on 32R516R versions.
3. Limit DC current from RDX and RDY to 100 µA and load capacitance to 20 pF. In multi-chip application these outputs can be wire-OR'ed.
4. The power bypassing capacitor must be located close to the 32R516 with its ground returned directly to device ground, with as short a path as possible.
5. To reduce ringing due to stray capacitance this resistor should be located close to the 32R516. Where this is not desirable a series resistor can be used to buffer a long WC line. In multi-chip applications a single resistor common to all chips may be used.

**FIGURE 2: Applications Information**

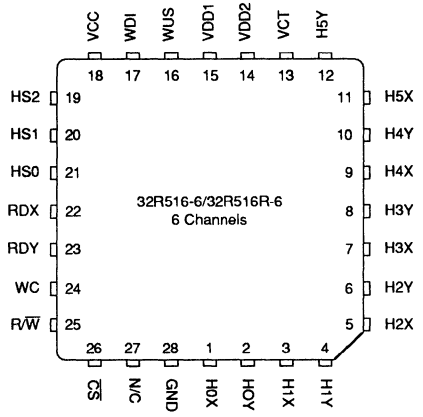
## PACKAGE PIN DESIGNATIONS (Top View)



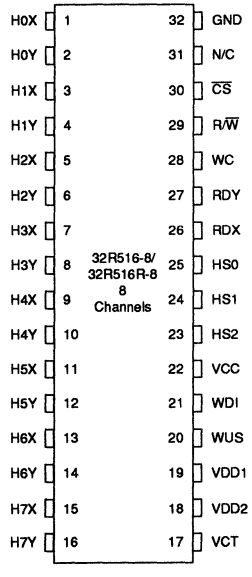

28-Lead SOL



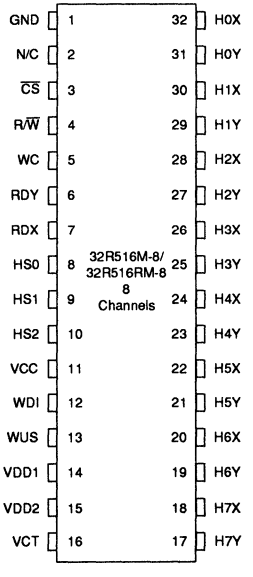

28-Lead SOL
Mirror Image



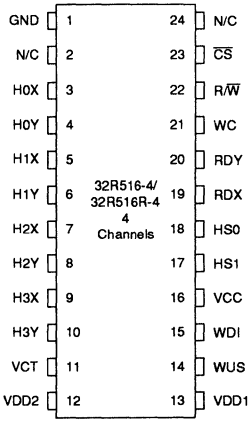

28-Lead PLCC




32-Lead SOW

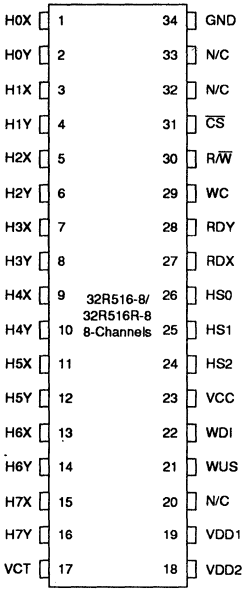



32-Lead SOW
Mirror Image

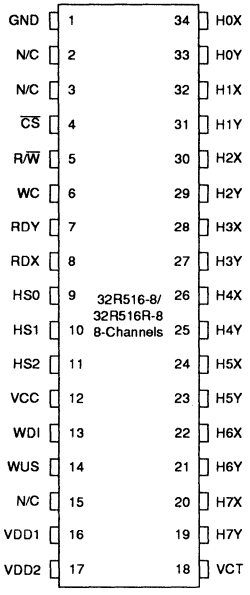



24-Lead SOL

## PACKAGE PIN DESIGNATIONS (Continued)




**34-Lead SOL**




**34-Lead SOL**
**Mirror Image**

**THERMAL CHARACTERISTICS:** θja

| | | |
|---|---|---|
| 24-lead | SOL | 75°C/W |
| 28-lead | PLCC | 65°C/W |
| | SOL | 75°C/W |
| 32-lead | SOW | 60°C/W |
| 34-lead | SOL | 70°C/W |
| 44-lead | PLCC | 50°C/W |

## ORDERING INFORMATION

| PART DESCRIPTION | ORDER NO. | PKG. MARK |
|---|---|---|
| SSI 32R516 | | |
| 4-Channel SOL | 32R516-4CL | 32R516-4CL |
| 6-Channel PLCC | 32R516-6CH | 32R516-6CH |
| 6-Channel SOL | 32R516-6CL | 32R516-6CL |
| 8-Channel SOW | 32R516-8CW | 32R516-8CW |
| 8-Channel SOL | 32R516-8CL | 32R516-8CL |
| SSI 32R516R | | |
| 4-Channel SOL | 32R516R-4CL | 32R516R-4CL |
| 6-Channel PLCC | 32R516R-6CH | 32R516R-6CH |
| 6-Channel SOL | 32R516R-6CL | 32R516R-6CL |
| 8-Channel SOW | 32R516R-8CW | 32R516R-8CW |
| 8-Channel SOL | 32R516R-8CL | 32R516R-8CL |
| SSI 32R516M | | |
| 6-Channel SOL | 32R516M-6CL | 32R516M-6CL |
| 8-Channel SOW | 32R516M-8CW | 32R516M-8CW |
| 8-Channel SOL | 32R516M-8CL | 32R516M-8CL |
| SSI 32R516RM | | |
| 6-Channel SOL | 32R516RM-6CL | 32R516RM-6CL |
| 8-Channel SOW | 32R516RM-8CW | 32R516RM-8CW |
| 8-Channel SOL | 32R516RM-8CL | 32R516RM-8CL |



Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 573-6000, FAX (714) 573-6914

**Notes:**

# SSI 32R5161R
## 10-Channel Ferrite/MIG Read/Write Device

September 1992

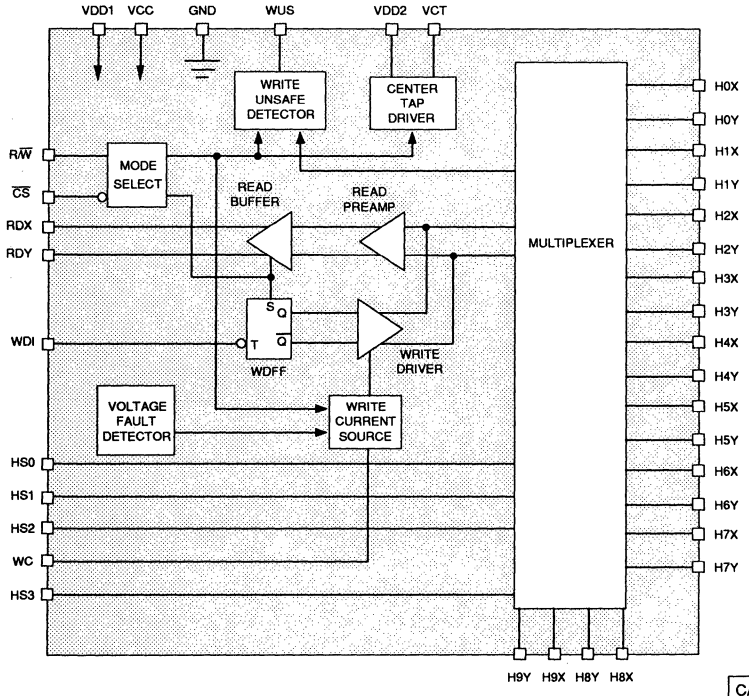
## DESCRIPTION

The SSI 32R5161R is a bipolar monolithic integrated circuit designed for use with a center-tapped ferrite or MIG recording heads. The SSI 32R5161R offers the performance upgrades of the SSI 32R511 along with improved head port characteristics and increased read gain. It provides a low noise read path, write current control, and data protection circuitry for as many as 10 channels. The SSI 32R5161R requires +5V and +12V power supplies and is available in a variety of packages.

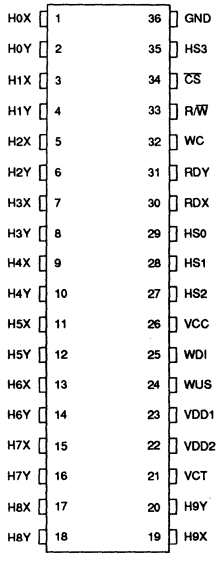
## FEATURES

- **High performance**
  - **Read mode gain = 150 V/V**
  - **Input noise = 1.3 nV/√Hz maximum**
  - **Input capacitance = 18 pF**
  - **Write current range = 10 mA to 60 mA**
- **Enhanced system write to read recovery time**
- **Power supply fault protection**
- **Designed for center-tapped ferrite or MIG heads**
- **Programmable write current source**
- **Easily multiplexed for larger systems**
- **Includes write unsafe detection**
- **TTL compatible control signals**
- **+5V, +12V power supplies**

## BLOCK DIAGRAM




## PIN DIAGRAM




**36-LEAD SOM**

CAUTION: Use handling procedures necessary for a static sensitive component.

## CIRCUIT OPERATION

The SSI 32R5161R gives the user the ability to address up to 10 center-tapped ferrite heads and provide write drive or read amplification. Head selection and mode control is accomplished using the HSn, $\overline{CS}$ and R/$\overline{W}$ inputs as shown in tables 1 & 2. Internal pullups are provided for the $\overline{CS}$ & R/$\overline{W}$ inputs to force the device into a non-writing condition if either control line is opened accidentally.

**TABLE 1: Mode Select**

| $\overline{CS}$ | R/$\overline{W}$ | MODE |
|---|---|---|
| 0 | 0 | Write |
| 0 | 1 | Read |
| 1 | X | Idle |

**TABLE 2: Head Select**

| HS3 | HS2 | HS1 | HS0 | HEAD |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 2 |
| 0 | 0 | 1 | 1 | 3 |
| 0 | 1 | 0 | 0 | 4 |
| 0 | 1 | 0 | 1 | 5 |
| 0 | 1 | 1 | 0 | 6 |
| 0 | 1 | 1 | 1 | 7 |
| 1 | 0 | 0 | 0 | 8 |
| 1 | 0 | 0 | 1 | 9 |

0 = Low level  1 = High level

### WRITE MODE

Taking both $\overline{CS}$ and R/$\overline{W}$ low selects write mode which configures the SSI 32R5161R as a current switch and activates the Write Unsafe (WUS) detector circuitry. Write current is toggled between the X and Y side of the selected head on each high to low transition of the Write Data Input (WDI). Note that a preceding read mode selection initializes the Write Data Flip-Flop, WDFF, to pass write current through the "X" side of the head. The zero-peak write current magnitude is programmed by an external resistor Rwc from pin WC to GND and is given by:

Iw = K/Rwc, where K = Write Current Constant

The Write Unsafe detection circuitry monitors voltage transitions at the selected head connections and flags any of the following conditions as a high level on the Write Unsafe open collector output:

- Head open
- WDI frequency too low
- Device not selected
- Head center tap open
- Device in read mode
- No write current

Two negative transitions on WDI, after the fault is corrected, will clear the WUS flag.

To further assure data security a voltage fault detection circuit prevents application of write current during power loss or power sequencing.

To enhance write to read recovery time the change in RDX, RDY common mode voltage is minimized by biasing these outputs to a level within the read mode range when in write mode.

Power dissipation in write mode may be reduced by placing a resistor (RCT) between VDD1 & VDD2. The optimum resistor value is 82Ω x 60/Iw (Iw in mA). At low write currents (<15 mA) read mode dissipation is higher than write mode and RCT, though recommended, may not be considered necessary. In this case VDD2 is connected directly to VDD1.

### READ MODE

Taking $\overline{CS}$ low and R/$\overline{W}$ high selects read mode which configures the SSI 32R5161R as a low noise differential amplifier for the selected head. The RDX and RDY outputs are driven by emitter followers and are in phase with the "X" and "Y" head ports. These outputs should be AC coupled to the load. The internal write current source is gated off in read mode eliminating the need for any external gating.

Read mode selection also initializes the Write Data Flip-Flop (WDFF) to pass write current through the "X" side of the head at a subsequent write mode selection.

### IDLE MODE

Taking $\overline{CS}$ high selects the idle mode which switches the RDX, RDY outputs into a high impedance state and deactivates the internal write current source. This facilitates multi-device installations by allowing the read outputs to be wire OR'ed and the write current programming resistor to be common to all devices.

## PIN DESCRIPTION

| NAME | I/O | DESCRIPTION |
|---|---|---|
| HS0-HS2 | I | Head Select |
| $\overline{CS}$ | I | Chip Select: a low level enables device |
| R/$\overline{W}$ | I | Read/Write: a high level selects read mode |
| WUS | O* | Write Unsafe: a high level indicates an unsafe writing condition |
| WDI | I | Write Data In: negative transition toggles direction of head current |
| H0X-H7X<br>H0Y-H7Y | I/O | X,Y head connections |
| RDX, RDY | O* | X, Y Read Data: differential read signal out |
| WC | * | Write Current: used to set the magnitude of the write current |
| VCT | - | Voltage Center Tap: voltage source for head center tap |
| VCC | - | +5V |
| VDD1 | - | +12V |
| VDD2 | - | Positive power supply for the center tap voltage source |
| GND | - | Ground |

*When more than one R/W device is used, these signals can be wire OR'ed.

## ELECTRICAL SPECIFICATIONS

**ABSOLUTE MAXIMUM RATINGS** (All voltages referenced to GND. Currents into device are positive.)

| PARAMETER | | VALUE | UNITS |
|---|---|---|---|
| DC Supply Voltage | VDD1 | -0.3 to +14 | VDC |
| DC Supply Voltage | VDD2 | -0.3 to +14 | VDC |
| DC Supply Voltage | VCC | -0.3 to +6 | VDC |
| Digital Input Voltage Range | VIN | -0.3 to VCC + 0.3 | VDC |
| Head Port Voltage Range | VH | -0.3 to VDD1 + 0.3 | VDC |
| WUS Pin Voltage Range | Vwus | -0.3 to +14 | VDC |
| Write Current Zero Peak | IW | 90 | mA |
| RDX, RDy Output Current | Io | -10 | mA |
| VCT Output Current | IVCT | -90 | mA |
| WUS Output Current | Iwus | +12 | mA |
| Storage Temperature Range | Tstg | -65 to 150 | °C |
| Lead Temperature PDIP, Flat Pack (10 sec Soldering) | | 260 | °C |
| Package Temperature PLCC, SO (20 sec Reflow) | | 215 | °C |

### RECOMMENDED OPERATION CONDITIONS

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|---|
| DC Supply Voltage | VDD1 | | 10.8 | 12.0 | 13.2 | VDC |
| DC Supply Voltage | VCC | | 4.5 | 5.0 | 5.5 | VDC |
| Head Inductance | Lh | | 5 | | 10 | µH |
| RCT Resistor | RCT* | Iw = 60 mA | | 82 | | Ω |
| Write Current | IW | | 10 | | 60 | mA |
| Junction Temperature Range | Tj | | +25 | | +135 | °C |

*For Iw = 60 mA. At other Iw levels refer to Applications Information that follows this specification.

### DC CHARACTERISTICS

(Unless otherwise specified, recommended operating conditions apply.)

### POWER SUPPLY

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|
| VCC Supply Current | Read/Idle Mode | | | 30 | mA |
| | Write Mode | | | 30 | mA |
| VDD Supply Current | Idle Mode | | | 20 | mA |
| (sum of VDD1 and VDD2) | Read Mode | | | 40 | mA |
| | Write Mode | | | 20 + Iw | mA |
| Power Dissipation (Tj = +125°C) | Idle Mode | | | 400 | mW |
| | Read Mode | | | 620 | mW |
| | Write Mode, IW = 45 mA, RCT = 0Ω | | | 800 | mW |
| | Write Mode, IW = 45 mA, RCT = 110Ω | | | 610 | mW |
| | Write Mode, IW = 60 mA RCT = 82Ω | | | 680 | mW |

**DC CHARACTERISTICS** (continued)

**DIGITAL I/O**

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|---|
| VIL | Input Low Voltage | | | | 0.8 | VDC |
| VIH | Input High Voltage | | 2.0 | | VCC + 0.3 | VDC |
| IIL | Input Low Current | VIL = 0.8V | -0.4 | | | mA |
| IIH | Input High Current | VIH = 2.0V | | | 100 | µA |
| VOL | WUS Output Low Voltage | IOL = 8 mA | | | 0.5 | VDC |
| IOH | WUS Output High Current | VOH = 5.0V | | | 100 | µA |

**WRITE MODE**

| | | | | | |
|---|---|---|---|---|---|
| Center Tap Voltage VCT | Write Mode | | 6.9 | | VDC |
| Head Current (per side) | Write Mode,<br>0 ≤ VCC ≤ 3.7V,<br>0 ≤ VDD1 ≤ 8.7V | -200 | | 200 | µA |
| Write Current Range | | 10 | | 60 | mA |
| Write Current Constant "K" | IW = 10 -60 mA | 2.375 | | 2.80 | V |
| Iwc to Head Current Gain | | | 0.99 | | mA/mA |
| Unselected Head Leakage Current | | | | 85 | µA |
| RDX, RDY Output Offset Voltage | Write/Idle Mode | -20 | | +20 | mV |
| RDX, RDY Common Mode Output Voltage | Write/Idle Mode | | 5.5 | | VDC |
| RDX, RDY Leakage | RDX, RDY = 6V<br>Write/Idle Mode | -100 | | 100 | µA |

**READ MODE**

| | | | | | |
|---|---|---|---|---|---|
| Center Tap Voltage | Read Mode | | 4.2 | | VDC |
| Head Current (per side) | Read or Idle Mode<br>0 ≤ VCC ≤ 5.5V<br>0 ≤ VDD1 ≤ 13.2V | -200 | | 200 | µA |
| Input Bias Current (per side) | | | | 45 | µA |
| Input Offset Voltage | Read Mode | -4 | | +4 | mV |
| Common Mode Output Voltage | Read Mode | 4.5 | 5.5 | 6.5 | VDC |

**DYNAMIC CHARACTERISTICS AND TIMING**

(Unless otherwise specified, recommended operating conditions apply and IW = 35 mA, Lh = 5 μH, f(WDI) = 5 MHz, CL(RDX, RDY) ≤ 35 pF.)

**WRITE MODE**

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|
| Differential Head Voltage Swing | | 7.0 | | | V(pk) |
| Unselected Head Transient Current | | | | 2 | mA(pk) |
| Differential Output Capacitance | | | | 15 | pF |
| Differential Output Resistance | | 430 | 650 | 870 | Ω |
| WDI Transition Frequency | WUS = low | 125 | | | kHz |

**READ MODE**

| | | | | | |
|---|---|---|---|---|---|
| Differential Voltage Gain | Vin = 1 mVpp @ 300 kHz, RL(RDX), RL(RDY) = 1 KΩ | 120 | 150 | 180 | V/V |
| Dynamic Range | AC Input Voltage, Vi, Where Gain Falls by 10%. V + f = 300 KHz | -3 | | | mVpp |
| Bandwidth (-3dB) | \|Zs\| < 5Ω, Vin = 1 mVpp | 30 | | | MHz |
| Input Noise Voltage | BW = 15 MHz, Lh = 0, Rh = 0 | | 1.0 | 1.3 | $nV/\sqrt{Hz}$ |
| Differential Input Capacitance | f = 5 MHz | | 14 | 18 | pF |
| Differential Input Resistance | 32R5161R, f = 5 MHz | 350 | | 800 | Ω |
| Common Mode Rejection Ratio | Vcm = VCT + 100 mVpp @ 5 MHz | 50 | | | dB |
| Power Supply Rejection Ratio | 100 mVpp @ 5 MHz on VDD1, VDD2 or VCC | 45 | | | dB |
| Channel Separation | Unselected Channels: Vin=100 mVpp @ 5 MHz; Selected Channel: Vin = 0 mVpp | 45 | | | dB |
| Single Ended Output Resistance | f = 5 MHz | | | 30 | Ω |
| Output Current | AC Coupled Load, RDX to RDY | ±2.1 | | | mA |

**DYNAMIC CHARACTERISTICS AND TIMING** (continued)

**SWITCHING CHARACTERISTICS**

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|
| R/$\overline{W}$ To Write | Delay to 90% of Write Current | | .15 | .7 | µs |
| R/$\overline{W}$ to Read | Delay to 90% of 100 mV, 10 MHz Read Signal Envelope or to 90% decay of Write Current | | .25 | .7 | µs |
| $\overline{CS}$ to Select | Delay to 90% of Write Current or to 90% of 100 mV, 10 MHz Read Signal Envelope | | .2 | 1.0 | µs |
| $\overline{CS}$ to Unselect | Delay to 90% Decay of Write Current | | .1 | 1.0 | µs |
| HS0 - HS2 to any head | Delay to 90% of 100 mV, 10 MHz Read Signal Envelope | | .25 | 1.0 | µs |
| WUS, Safe to Unsafe - TD1 | Iw = 35 mA | 1.6 | | 8.0 | µs |
| WUS, Unsafe to Safe - TD2 | Iw = 35 mA | | | 1.0 | µs |
| Head Current (Lh = 0 µH, Rh = 0Ω) | | | | | |
| Prop. Delay - TD3 | From 50% Points | | | 25 | ns |
| Asymmetry | WDI has 50% Duty Cycle and 1ns Rise/Fall Time | | | 1 | ns |
| Rise/Fall Time | 10% - 90% Points | | | 20 | ns |

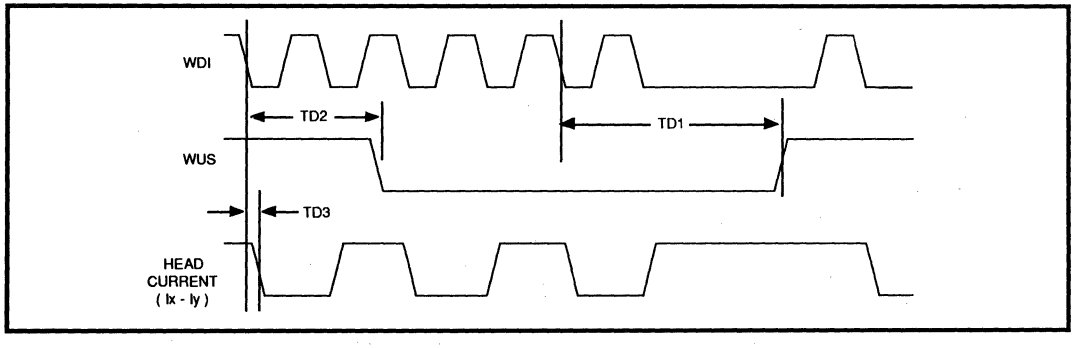
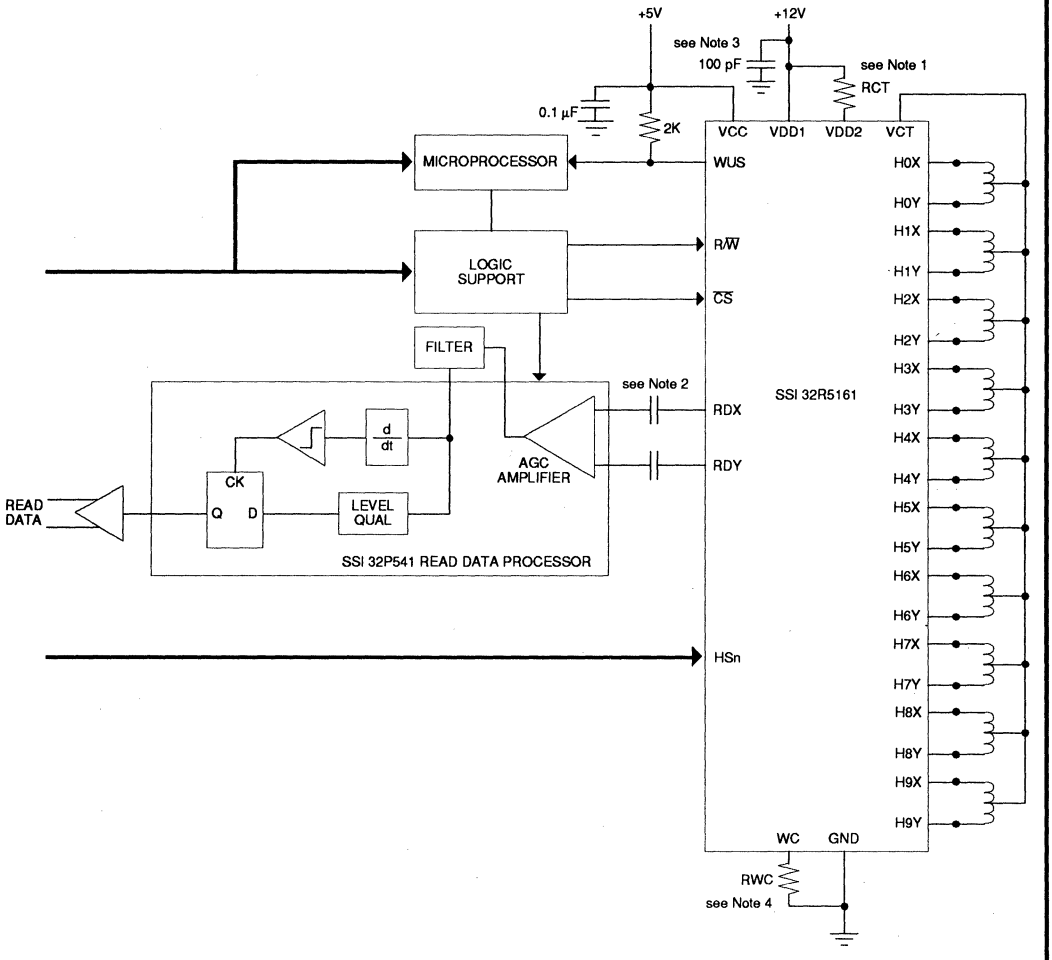



**FIGURE 1: Write Mode Timing Diagram**



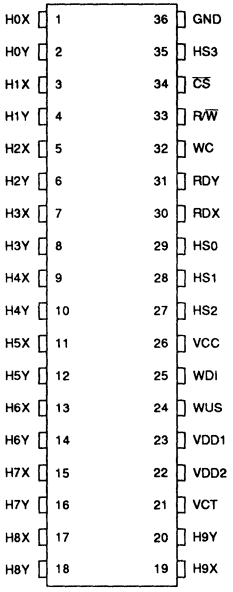

**NOTES**

1. An external resistor, RCT, given by; RCT = 82 (60/Iw) where Iw is the zero-peak write current in mA, can be used to limit internal power dissipation. Otherwise connect VDD2 to VDD1.
2. Limit DC current from RDX and RDY to 100 µA and load capacitance to 20 pF. In multi-chip application these outputs can be wire-OR'ed.
3. The power bypassing capacitor must be located close to the 32R5161R with its ground returned directly to device ground, with as short a path as possible.
4. To reduce ringing due to stray capacitance this resistor should be located close to the 32R5161R. Where this is not desirable a series resistor can be used to buffer a long WC line. In multi-chip applications a single resistor common to all chips may be used.

**FIGURE 2: Applications Information**

## PACKAGE PIN DESIGNATIONS

(Top View)




**36-Lead SOM**

**THERMAL CHARACTERISTICS:** θja

| | | |
|---|---|---|
| 36-lead | SOM | 50°C/W |

## ORDERING INFORMATION

| PART DESCRIPTION | ORDERING NO. | PKG. MARK |
|---|---|---|
| SSI 32R5161R Read/Write Device | | |
| 10-Channel SOM | 32R5161R-10CM | 32R5161R-10CM |



Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 573-6000, FAX (714) 573-6914

**Notes:**

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A TDK Group Company

# SSI 32R528R
## 9-Channel Thin Film Read/Write Device
## Preliminary Data

November 1991

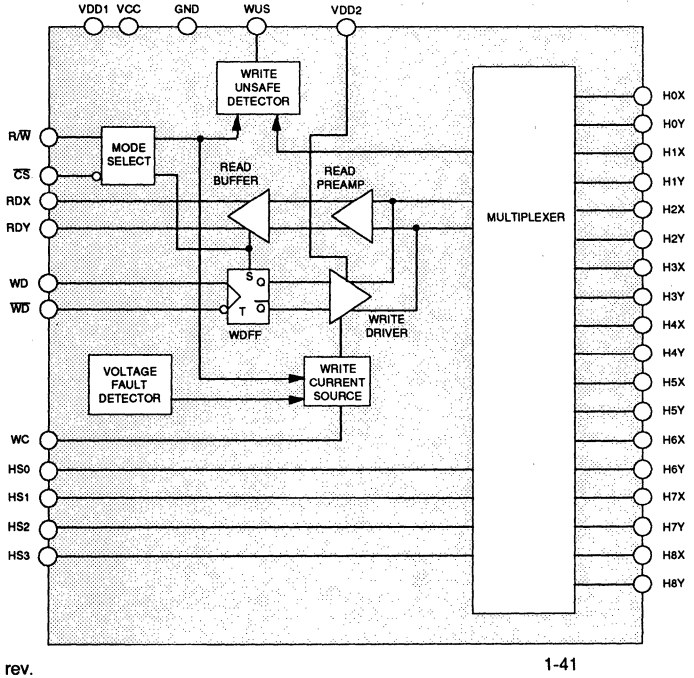
## DESCRIPTION

The SSI 32R528R Read/Write device is a bipolar monolithic integrated circuit designed for use with two terminal thin film recording heads. It provides a low noise read amplifier, write current control and data protection circuitry for eight or nine channels. Power supply fault protection is provided by disabling the write current generator during power sequencing. System write to read recovery time is significantly improved by controlling the read channel common mode output voltage shift in the write mode. It requires +5V and +12V power supplies and is available in a 36 SOM package. A mirror image pinout option is available to simplify flex circuit layout in multiple R/W device applications. The SSI 32R528R provides internal 700Ω damping resistors.

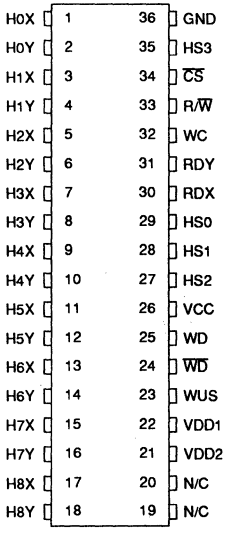
## FEATURES

- **High performance:**
  - **Read mode gain = 150 V/V**
  - **Input noise = 0.85 nV/√Hz max.**
  - **Input capacitance = 35 pF max.**
  - **Write current range = 10 mA to 40 mA**
  - **Head voltage swing = 7 Vpp**
  - **Write current rise time = 9 ns**
- **Enhanced system write to read recovery time**
- **Differential ECL-like Write Data input**
- **Power supply fault protection**
- **Compatible with two & three terminal TFH**
- **Write unsafe detection**
- **+5V, +12V power supplies**

## BLOCK DIAGRAM




## PIN DIAGRAM




**36-Lead SOM**

CAUTION: Use handling procedures necessary for a static sensitive component.

## CIRCUIT OPERATION

The SSI 32R528R addresses up to nine two-terminal thin film heads providing write drive or read amplification. Head selection and mode control is accomplished with pins HSn, $\overline{CS}$ and R/$\overline{W}$, as shown in Tables 1 & 2. Internal resistor pullups, provided on pins $\overline{CS}$ and R/$\overline{W}$ will force the device into a non-writing condition if either control line is opened accidentally.

### WRITE MODE

The write mode configures the SSI 32R528R as a current switch and activates the Write Unsafe (WUS) detection circuitry. Write current is toggled between the X and Y direction of the selected head on each low to high transition of the WD, Write Data Input.

A preceding read operation initializes the Write Data Flip Flop (WDFF) to pass write current in the X-direction of the head, i.e. into the X-port.

The magnitude of the write current (0-pk) given by:

$$Iw = \frac{Vwc}{RWC}$$

where Vwc (WC pin voltage) = 1.65V ± 5%, is programmed by an external resistor RWC, connected from pin WC to ground. In multiple device applications, a single RWC resistor may be made common to all devices. The actual head current Ix, y is given by:

$$Ix,y = \frac{Iw}{1 + Rh/Rd}$$

where:
Rh = head resistance + external wire resistance, and
Rd = damping resistance.

Power supply fault protection improves data security by disabling the write current generator during a voltage fault or power supply sequencing. Additionally, the write unsafe detection circuitry will flag any of the conditions listed below as a high level on the open collector output pin, WUS. Two negative transitions on the WD/$\overline{WD}$ lines, after the fault is corrected, are required to clear the WUS flag.

- WD frequency too low
- Device not selected
- Head open
- Device in read mode
- No write current

Power dissipation in Write Mode may be reduced by placing a resistor, Rw, between VDD1 and VDD2. The resistor value should be chosen such that Iw Rw ≤ 3.0V for an accompanying reduction of $(Iw)^2$ Rw in power dissipation. If a resistor is not used, VDD2 should be connected to VDD1. Note that Rw will also provide current limiting in the event of a head short.

### READ MODE

The read mode configures the SSI 32R528R as a low noise differential amplifier and deactivates the write current generator and write unsafe detection circuitry. The RDX and RDY outputs are emitter followers and are in phase with the "X" and "Y" head ports. These outputs should be AC coupled to the load. The RDX, RDY common mode voltage is maintained at the write mode value, minimizing the transient between write mode and read mode, substantially reducing the write to read recovery time in the subsequent Pulse Detection circuitry.

### IDLE MODE

The idle mode deactivates the internal write current generator, the write unsafe detector and switches the RDX, RDY outputs into a high impedance state. This facilitates multiple device applications by enabling the read outputs to be wire OR'ed and the write current programming resistor to be common to all devices.

**TABLE 1: Mode Select**

| $\overline{CS}$ | R/$\overline{W}$ | MODE |
|---|---|---|
| 0 | 0 | Write |
| 0 | 1 | Read |
| 1 | 0 | Idle |
| 1 | 1 | Idle |

**TABLE 2: Head Select**

| HS3 | HS2 | HS1 | HS0 | HEAD |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 2 |
| 0 | 0 | 1 | 1 | 3 |
| 0 | 1 | 0 | 0 | 4 |
| 0 | 1 | 0 | 1 | 5 |
| 0 | 1 | 1 | 0 | 6 |
| 0 | 1 | 1 | 1 | 7 |
| 1 | 0 | 0 | 0 | 8 |

0 = Low level  1 = High level

## PIN DESCRIPTIONS

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| HS0 - HS3 | I | Head Select: TTL level |
| $\overline{CS}$ | I | Chip Select: a low TTL level enables the device |
| R/$\overline{W}$ | I | Read/Write: a high TTL level selects Read mode |
| WUS | O* | Write Unsafe: Open collector output, a high level indicates an unsafe writing condition |
| WD, $\overline{WD}$ | I | Differential Write Data inputs: a positive transition on WD toggles the direction of the head current |
| H0X - H8X<br>H0Y - H8Y | I/O | X, Y Head Connections: Current in the X-direction flows into the X-port |
| RDX, RDY | O* | X, Y Read Data: differential read data output |
| WC | * | Write Current: used to set the magnitude of the write current |
| VCC | - | +5V Logic Circuit Supply |
| VDD1 | - | +12V |
| VDD2 | - | Positive Power Supply for Write current drivers |
| GND | - | Ground |

*When more than one R/W device is used, these signals can be wire OR'ed.

## ELECTRICAL SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS

Operation outside these rating limits may permanently damage the device.

| PARAMETER | | SYMBOL | VALUE | UNITS |
|---|---|---|---|---|
| DC Supply Voltage | | VDD1, 2 | -0.3 to +14 | VDC |
| | | VCC | -0.3 to +7 | VDC |
| Write Current | | Iw | 100 | mA |
| Digital Input Voltage | | Vin | -0.3 to VCC +0.3 | VDC |
| Head Port Voltage | | VH | -0.3 to VDD2 +0.3 | VDC |
| WUS Pin Voltage Range | | Vwus | -0.3 to +14 | VDC |
| Output Current | RDX, RDY | Io | -10 | mA |
| | WUS | Iwus | +12 | mA |
| Storage Temperature | | Tstg | -65 to +150 | °C |

**RECOMMENDED OPERATING CONDITIONS**

| PARAMETER | SYMBOL | VALUE | UNITS |
|---|---|---|---|
| DC Supply Voltage | VDD1 | 12 ± 10% | VDC |
| | VDD2 | VDD1 - 3.0 to VDD1 | VDC |
| | VCC | 5 ± 10% | VDC |
| Operating Temperature | Tj | 0 to +135 | °C |

**DC CHARACTERISTICS**
Unless otherwise specified, recommended operating conditions apply.

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|
| VDD1 Supply Current | Read Mode | - | - | 42 | mA |
| | Write Mode | - | - | 50 | mA |
| | Idle Mode | - | - | 22 | mA |
| VDD2 Supply Current | Read Mode | - | - | 200 | µA |
| | Write Mode | - | - | Iw + 0.4 | mA |
| | Idle Mode | - | - | 200 | µA |
| VCC Supply Current | Read Mode | - | - | 68 | mA |
| | Write Mode | - | - | 48 | mA |
| | Idle Mode | - | - | 55 | mA |
| Power Dissipation (Tj = +135°C) | Read Mode | - | - | 850 | mW |
| | Write Mode: Iw = 20 mA, VDD2 = VDD1 | - | - | 1100 | mW |
| | Write Mode: Iw = 40 mA, VDD1 - VDD2 = 3.0V | - | - | 1200 | mW |
| | Idle Mode | - | - | 550 | mW |
| WD, $\overline{WD}$ Input Low Current (IIL1) | VIL1 = VCC -1.625V | | | 80 | µA |
| WD, $\overline{WD}$ Input High Current (IIH1) | VIH1 = VCC -0.72V | | | 100 | µA |
| WD, $\overline{WD}$ Input Low Voltage (VIL1) | | VCC -1.870 | | VCC -1.625 | VDC |
| WD, $\overline{WD}$ Input High Voltage (VIH1) | | VCC -1.00 | | VCC -0.720 | VDC |
| R/$\overline{W}$, $\overline{CS}$, HS0-HS3 Input Low Current (IIL2) | VIL2 = 0.8V | -0.4 | | | mA |
| R/$\overline{W}$, $\overline{CS}$, HS0-HS3 Input High Current (IIH2) | VIH2 = 2.0V | | | 100 | µA |
| R/$\overline{W}$, $\overline{CS}$, HS0-HS3 Input Low Voltage (VIL2) | | | | 0.8 | VDC |
| R/$\overline{W}$, $\overline{CS}$, HS0-HS3 Input High Voltage (VIH2) | | 2.0 | | | VDC |

**DC CHARACTERISTICS** (Continued)

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|
| WUS Output Low Voltage (VOL) | ILUS = 8.0 mA | | | 0.5 | VDC |
| VDD Fault Voltage | | 8.5 | - | 10.0 | VDC |
| VCC Fault Voltage | | 3.5 | - | 4.2 | VDC |
| Head Current (HnX, HnY) | Write Mode, 0 ≤ VCC ≤ 3.5V<br>0 ≤ VDD1 ≤ 8.5V | -200 | - | +200 | µA |
| | Read/Idle Mode<br>0 ≤ VCC ≤ 5.5V<br>0 ≤ VDD1 ≤ 13.2V | -200 | - | +200 | µA |

**WRITE CHARACTERISTICS**

Unless otherwise specified, recommended operating conditions apply, Iw = 20 mA, Lh = 1.0 µH, Rh = 30Ω and $f$(WD) = 5 MHz.

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|
| WC Pin Voltage (Vwc) | | 1.57 | 1.65 | 1.73 | V |
| Differential Head Voltage Swing | | 7 | - | - | Vpp |
| Unselected Head Current | | - | - | 1 | mA(pk) |
| Differential Output Capacitance | | - | - | 25 | pF |
| Differential Output Resistance | 32R528R | 500 | 700 | 950 | Ω |
| WD Transition Frequency | WUS = low | 1.7 | - | - | MHz |
| Write Current Range | 0 - pk | 10 | - | 40 | mA |

**READ CHARACTERISTICS**

Unless otherwise specified, recommended operating conditions apply CL (RDX, RDY) < 20 pF and RL (RDX,RDY) = 1 kΩ.

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|---|
| Differential Voltage Gain | | Vin = 1 mVpp @ 1 MHz | 125 | - | 175 | V/V |
| Bandwidth | -1dB | \|Zs\| < 5Ω, Vin=1 mVpp | 25 | - | - | MHz |
| | -3dB | \|Zs\| < 5Ω, Vin=1 mVpp | 45 | - | - | MHz |
| Input Noise Voltage | | BW = 15 MHz, Lh = 0, Rh = 0 | - | 0.62 | 0.85 | nV/√Hz |
| Differential Input Capacitance | | Vin = 1 mVpp, $f$ = 5 MHz | - | - | 35 | pF |
| Differential Input Resistance | 32R528R | Vin = 1 mVpp, $f$ = 5 MHz | 300 | - | - | Ω |
| Dynamic Range | | Peak-to-peak ac input voltage where gain falls to 90% of its small signal value, $f$ = 5 MHz | 6 | - | - | mVpp |

**READ CHARACTERISTICS** (Continued)

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|
| Common Mode Rejection Ratio | Vin = 0 VDC+100 mVpp @ 5 MHz | 54 | - | - | dB |
| Power Supply Rejection Ratio | 100 mVpp @ 5 MHz on VDD1<br>100 mVpp @ 5 MHz on VCC | 54 | - | - | dB |
| Channel Separation | Unselected channels driven with 100 mVpp @ 5 MHz, Vin = 0 mVpp | 45 | - | - | dB |
| Output Offset Voltage | | -360 | - | +360 | mV |
| RDX, RDY Common Mode | Read Mode | 2.2 | 2.9 | 3.6 | VDC |
| Output Voltage | Write Mode | - | 2.9 | - | VDC |
| Single Ended Output Resistance | $f$ = 5 MHz | - | - | 40 | Ω |
| Output Current | AC Coupled Load, RDX to RDY | 3.2 | - | - | mA |

**SWITCHING CHARACTERISTICS** (See Figure 1)
Unless otherwise specified, recommended operating conditions apply, Iw = 20 mA, Lh = 1.0 µH, Rh = 30Ω and $f$(WD) = 5 MHz.

| PARAMETER | CONDITIONS | MIN | MAX | UNITS |
|---|---|---|---|---|
| R/$\overline{W}$ | | | | |
| R/$\overline{W}$ to Write Mode | Delay to 90% of write current | - | 0.6 | µs |
| R/$\overline{W}$ to Read Mode | Delay to 90% of 100 mV 10 MHz Read signal envelope or to 90% decay of write current | - | 0.6 | µs |
| $\overline{CS}$ | | | | |
| $\overline{CS}$ to Select | Delay to 90% of write current or to 90% of 100 mV 10 MHz Read signal envelope | - | 0.6 | µs |
| $\overline{CS}$ to Unselect | Delay to 10% of write current | - | 0.6 | µs |
| HSn | | | | |
| HS0, 1, 2, 3 to any Head | Delay to 90% of 100 mV 10 MHz Read signal envelope | - | 0.4 | µs |
| WUS | | | | |
| Safe to Unsafe - TD1 | | 0.6 | 3.6 | µs |
| Unsafe to Safe - TD2 | | - | 1 | µs |
| Head Current | | | | |
| Prop. Delay - TD3 | From 50% points, Lh=0µh, Rh=0Ω | - | 32 | ns |
| Asymmetry | WD has 50% duty cycle and 1ns rise/fall time, Lh=0µh, Rh=0Ω | - | 1 | ns |
| Rise/Fall Time | 10% - 90% points, Lh=0µh, Rh=0Ω | - | 9 | ns |

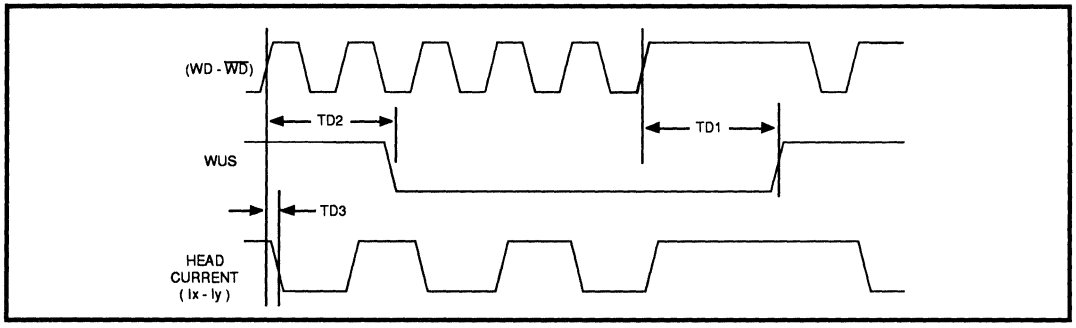



**FIGURE 1: Write Mode Timing Diagram**

## APPLICATIONS INFORMATION

The specifications, provided in the data section, account for the worst case values of each parameter taken individually. In actual operation, the effects of worst case conditions on many parameters correlate. Tables 3 & 4 demonstrate this for several key parameters. Notice that under the conditions of worst case input noise, the higher read back signal resulting from the higher input impedance can compensate for the higher input noise. Accounting for this correlation in your analysis will be more representative of actual performance.

**TABLE 3: Key Parameters Under Worst Case Input Noise Conditions**

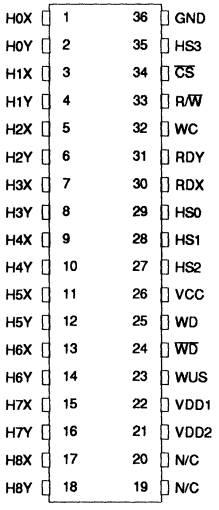
| PARAMETER | | Tj = 25°C | Tj = 135°C | UNITS |
|---|---|---|---|---|
| Input Noise Voltage (Max.) | | 0.70 | 0.85 | nV/$\sqrt{Hz}$ |
| Differential Input Resistance (Min.) | 32R528R | 390 | 420 | Ω |
| Differential Input Capacitance (Max.) | | 32 | 34 | pF |

**TABLE 4: Key Parameters Under Worst Case Input Impedance Conditions**

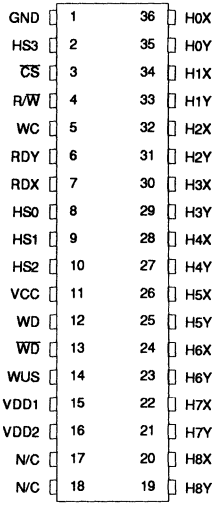
| PARAMETER | | Tj = 25°C | Tj = 135°C | UNITS |
|---|---|---|---|---|
| Input Noise Voltage (Max.) | | 0.58 | 0.71 | nV/$\sqrt{Hz}$ |
| Differential Input Resistance (Min.) | 32R528R | 310 | 350 | Ω |
| Differential Input Capacitance (Max.) | | 33 | 35 | pF |

# SSI 32R528R
# 9-Channel Thin Film
# Read/Write Device

## PACKAGE PIN DESIGNATIONS
(Top View)




36-Lead SOM




36-Lead SOM Mirror

**THERMAL CHARACTERISTICS: Ø ja**

| | |
|---|---|
| 36-Lead SOM | 50°C/W |

## ORDERING INFORMATION

| PART DESCRIPTION | ORDER NO. | PKG. MARK |
|---|---|---|
| SSI 32R528R with Internal Damping Resistor | | |
| 9-Channel SOM | 32R528R-9CM | 32R528R-9CM |
| SSI 32R528R Mirror Image with Damping Resistor | | |
| 9-Channel SOM | 32R528RM-9CL | 32R528RM-9CL |

**Preliminary Data:** Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.



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A TDK Group Company

# SSI 32R5281R
## 14-Channel Two-Terminal Read/Write Device
## Advance Information

November 1991

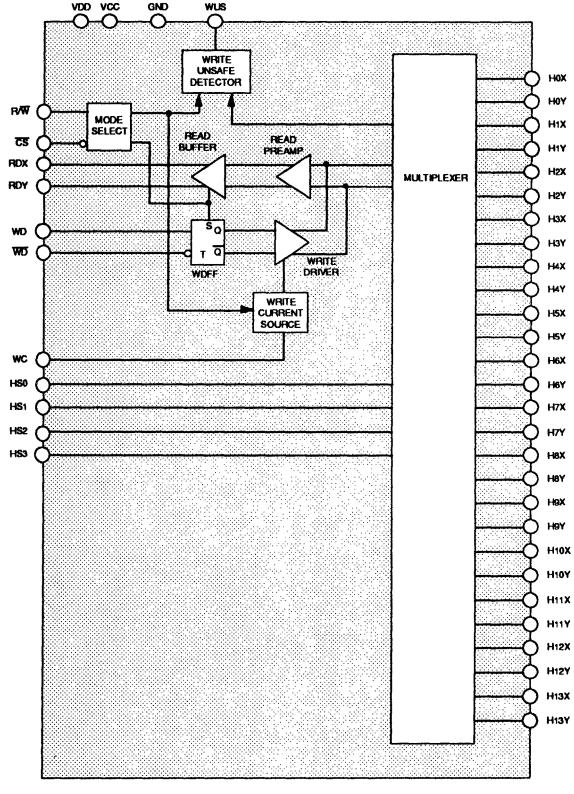
## DESCRIPTION

The SSI 32R5281R Read/Write device is a bipolar monolithic integrated circuit designed for use with two-terminal thin-film recording heads. It provides a low noise read amplifier, write current control and data protection circuitry for up to 14 channels. Power supply fault protection is provided by disabling the write current generator during power sequencing. System write to read recovery time is significantly improved by controlling the read channel common mode output voltage shift in the write mode. It requires +5V and +12V power supplies and provides internal 700Ω damping resistors.

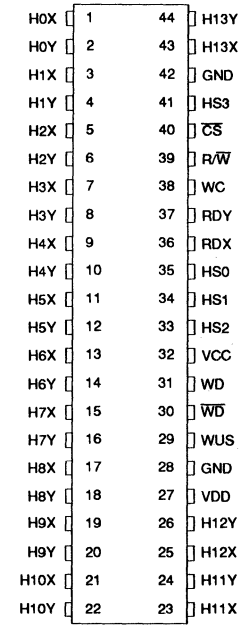
## FEATURES

- **High performance:**
  - **Read mode gain = 250 V/V**
  - **Input noise = 0.85 nV/√Hz max.**
  - **Input capacitance = 35 pF max.**
  - **Write current range = 10 mA to 40 mA**
  - **Head voltage swing = 7 Vpp**
  - **Write current rise time = 9 ns**
- **Enhanced system write to read recovery time**
- **Differential ECL-like Write Data input**
- **Power supply fault protection**
- **Write unsafe detection**
- **+5V, +12V power supplies**

## BLOCK DIAGRAM




## PIN DIAGRAM




**44-LEAD SOM**

CAUTION: Use handling procedures necessary for a static sensitive component.

## CIRCUIT OPERATION

The SSI 32R5281R addresses up to 14 two-terminal thin film heads providing write drive or read amplification. Head selection and mode control is accomplished with pins HSn, $\overline{CS}$ and R/$\overline{W}$, as shown in Tables 1 & 2. Internal resistor pullups, provided on pins $\overline{CS}$ and R/$\overline{W}$ will force the device into a non-writing condition if either control line is opened accidentally.

### WRITE MODE

The write mode configures the SSI 32R5281R as a current switch and activates the Write Unsafe (WUS) detection circuitry. Write current is toggled between the X and Y direction of the selected head on each low to high transition on the WD, Write Data input. (See figure 1.)

A preceding read operation initializes the Write Data Flip Flop (WDFF) to pass write current in the X-direction of the head, i.e., into the X-port.

The magnitude of the write current (0-pk) is given by:

$$Iw = \frac{Vwc}{Rwc}$$

where Vwc (WC pin voltage) = 1.65V ± 5%, is programmed by an external resistor Rwc, connected from pin WC to ground. In multiple device applications, a single Rwc resistor may be made common to all devices. The actual head current Ix, y is given by:

$$Ix,y = \frac{Iw}{1 + Rh/Rd}$$

where:
Rh = head resistance + external wire resistance, and
Rd = damping resistance.

Power supply fault protection improves data security by disabling the write current generator during a voltage fault or power supply sequencing. Additionally, the write unsafe detection circuitry will flag any of the conditions listed below as a high level on the open collector output pin, WUS. Two positive transitions on the WD, Write Data input line, after the fault is corrected, are required to clear the WUS flag.

- WD frequency too low
- Device not selected
- Open head
- Device in read mode
- No write current

### READ MODE

The read mode configures the SSI 32R5281R as a low noise differential amplifier and deactivates the write current generator and write unsafe detection circuitry. The RDX and RDY outputs are emitter followers and are in phase with the "X" and "Y" head ports. These outputs should be AC coupled to the load. The RDX, RDY common mode voltage is maintained at the write mode value, minimizing the transient between write mode and read mode, substantially reducing the write to read recovery time in the subsequent Pulse Detection circuitry.

### IDLE MODE

The idle mode deactivates the internal write current generator, the write unsafe detector and switches the RDX, RDY outputs into a high impedance state. This facilitates multiple device applications by enabling the read outputs to be wire-OR'ed and the write current programming resistor to be common to all devices.

**TABLE 1: Mode Select**

| $\overline{CS}$ | R/$\overline{W}$ | MODE |
|---|---|---|
| 0 | 0 | Write |
| 0 | 1 | Read |
| 1 | 0 | Idle |
| 1 | 1 | Idle |

**TABLE 2: Head Select**

| HS3 | HS2 | HS1 | HS0 | HEAD |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 2 |
| 0 | 0 | 1 | 1 | 3 |
| 0 | 1 | 0 | 0 | 4 |
| 0 | 1 | 0 | 1 | 5 |
| 0 | 1 | 1 | 0 | 6 |
| 0 | 1 | 1 | 1 | 7 |
| 1 | 0 | 0 | 0 | 8 |
| 1 | 0 | 0 | 1 | 9 |
| 1 | 0 | 1 | 0 | 10 |
| 1 | 0 | 1 | 1 | 11 |
| 1 | 1 | 0 | 0 | 12 |
| 1 | 1 | 0 | 1 | 13 |

0 = Low level  1 = High level

## PIN DESCRIPTION

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| HSO - HS3 | I | Head Select |
| $\overline{CS}$ | I | Chip Select: a low level enables the device |
| R/$\overline{W}$ | I | Read/Write: a high level selects Read mode |
| WUS | O* | Write Unsafe: Open collector output, a high level indicates an unsafe writing condition |
| WD, $\overline{WD}$ | I | Differential Write Data inputs: a positive transition on WD toggles the direction of the head current |
| H0X - H13X<br>H0Y - H13Y | I/O | X, Y Head Connections: Current in the X-direction flows into the X-port |
| RDX, RDY | O* | X, Y Read Data: differential read data output |
| WC | * | Write Current: used to set the magnitude of the write current |
| VCC | - | +5V Logic Circuit Supply |
| VDD | - | +12V |
| GND | - | Ground |

*When more than one R/W device is used, these signals can be wire OR'ed.

## ELECTRICAL SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS

Operation outside these rating limits may permanently damage the device.

| PARAMETER | | SYMBOL | VALUE | UNITS |
|---|---|---|---|---|
| DC Supply Voltage | | VDD | -0.3 to +14 | VDC |
| | | VCC | -0.3 to +7 | VDC |
| Write Current | | Iw | 100 | mA |
| Digital Input Voltage | | Vin | -0.3 to VCC +0.3 | VDC |
| Head Port Voltage | | VH | -0.3 to VDD2 +0.3 | VDC |
| WUS Pin Voltage Range | | Vwus | -0.3 to +14 | VDC |
| Output Current | RDX, RDY | Io | -10 | mA |
| | WUS | Iwus | +12 | mA |
| Storage Temperature | | Tstg | -65 to +150 | °C |

### RECOMMENDED OPERATING CONDITIONS

| PARAMETER | SYMBOL | VALUE | UNITS |
|---|---|---|---|
| DC Supply Voltage | VDD | 12 ± 10% | VDC |
| | VCC | 5 ± 10% | VDC |
| Operating Temperature | Tj | +25 to +135 | °C |

### DC CHARACTERISTICS

Unless otherwise specified, recommended operating conditions apply.

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|
| VDD Supply Current | Read Mode | - | 30 | TBD | mA |
| | Write Mode | - | 39 | TBD | mA |
| | Idle Mode | - | 12 | TBD | mA |
| VCC Supply Current | Read Mode | - | 50 | TBD | mA |
| | Write Mode | - | 32 | TBD | mA |
| | Idle Mode | - | 43 | TBD | mA |
| Power Dissipation (Tj = +135°C) | Read Mode | - | - | 800 | mW |
| | Write Mode: Iw = 20 mA, | - | - | 1000 | mW |
| | Idle Mode | - | 360 | 570 | mW |
| WD, $\overline{WD}$ Input Low Current (IIL1) | VIL1 = VCC -1.625V | | | 80 | µA |
| WD, $\overline{WD}$ Input High Current (IIH1) | VIH1 = VCC -0.72V | | | 100 | µA |
| WD, $\overline{WD}$ Input Low Voltage (VIL1) | | VCC -1.870 | | VCC -1.625 | VDC |
| WD, $\overline{WD}$ Input High Voltage (VIH1) | | VCC -1.00 | | VCC -0.720 | VDC |
| R/$\overline{W}$, $\overline{CS}$, HS0-HS3 Input Low Current (IIL2) | VIL2 = 0.8V | -0.4 | | | mA |
| R/$\overline{W}$, $\overline{CS}$, HS0-HS3 Input High Current (IIH2) | VIH2 = 2.0V | | | 100 | µA |
| R/$\overline{W}$, $\overline{CS}$, HS0-HS3 Input Low Voltage (VIL2) | | | | 0.8 | VDC |
| R/$\overline{W}$, $\overline{CS}$, HS0-HS3 Input High Voltage (VIH2) | | 2.0 | | | VDC |
| WUS Output Low Voltage (VOL) | Iol = 8 mA | - | - | 0.5 | VDC |
| VDD Fault Voltage | | 8.5 | - | 10.0 | VDC |
| VCC Fault Voltage | | 3.5 | - | 4.2 | VDC |

**DC CHARACTERISTICS** (continued)

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|
| Head Current (HnX, HnY) | Write Mode,<br>0 ≤ VCC ≤ 3.5V<br>0 ≤ VDD1 ≤ 8.5V | -200 | - | +200 | µA |
| | Read/Idle Mode,<br>0 ≤ VCC ≤ 5.5V<br>0 ≤ VDD1 ≤13.2V | -200 | - | +200 | µA |

**WRITE CHARACTERISTICS**

Unless otherwise specified, recommended operating conditions apply, Iw = 20 mA, Lh = 500 nH, Rh = 30Ω and f(WD) = 5 MHz.

| | | | | | |
|---|---|---|---|---|---|
| WC Pin Voltage (Vwc) | | - | 1.65 ±5% | - | V |
| Differential Head Voltage Swing | Iw = 40 mA | 7 | - | - | Vpp |
| Unselected Head Current | | - | - | 1 | mA(pk) |
| Differential Output Capacitance | | - | - | 25 | pF |
| Differential Output Resistance | | 500 | 700 | 950 | Ω |
| WDI Transition Frequency | WUS = low | 1.7 | - | - | MHz |
| | WUS = high | - | - | 500 | kHz |
| Write Current Range | | 10 | - | 40 | mA |

**READ CHARACTERISTICS**

Unless otherwise specified, recommended operating conditions apply CL (RDX, RDY) < 20pF and RL (RDX,RDY) = 1 kΩ.

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|---|
| Differential Voltage Gain | | Vin=1mVpp @ 300 kHz | 210 | 250 | 290 | V/V |
| Bandwidth | -1dB | \|Zs\|<5Ω, Vin=1 mVpp | 25 | 40 | - | MHz |
| | -3dB | \|Zs\|<5Ω, Vin=1 mVpp | 35 | 55 | - | MHz |
| Input Noise Voltage | | BW = 15 MHz, Lh = 0, Rh = 0 | - | 0.62 | 0.85 | nV/√Hz |
| Differential Input Capacitance | | Vin = 1 mVpp, f = 5 MHz | - | - | 35 | pF |
| Differential Input Resistance | | Vin = 1 mVpp, f = 5 MHz | 300 | - | - | Ω |
| Dynamic Range | | Peak-to-peak AC input voltage where gain falls to 90% of its small signal value, f = 5 MHz | 2.0 | - | - | mVpp |
| Common Mode Rejection Ratio | | Vin = 0 VDC+100 mVpp @ 5 MHz | 54 | - | - | dB |
| Power Supply Rejection Ratio | | 100 mVpp @ 5 MHz on VDD1<br>100 mVpp @ 5 MHz on VCC | 54 | - | - | dB |
| Channel Separation | | Unselected channels driven with 100 mVpp @ 5 MHz, Vin = 0 mVpp | 45 | - | - | dB |

**READ CHARACTERISTICS** (continued)

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|
| Output Offset Voltage | | -400 | - | +400 | mV |
| RDX, RDY Common Mode Output Voltage | Read Mode or Write Mode | Vcc -2.5 | Vcc - 2.1 | Vcc -1.7 | VDC |
| Single Ended Output Resistance | f = 5 MHz | - | - | 30 | Ω |
| Output Current | AC Coupled Load, RDX to RDY | 3.2 | - | - | mA |

**SWITCHING CHARACTERISTICS** (See Figure 1)
Unless otherwise specified, recommended operating conditions apply, Iw = 20 mA, Lh = 500 nH, Rh = 30Ω and f(WD) = 5 MHz.

| PARAMETER | CONDITIONS | MIN | MAX | UNITS |
|---|---|---|---|---|
| R/$\overline{W}$ | | | | |
| R/$\overline{W}$ to Write Mode | Delay to 90% of write current | - | 0.6 | µs |
| R/$\overline{W}$ to Read Mode | Delay to 90% of 100mV 10MHz Read signal envelope or to 90% decay of write current | - | 0.6 | µs |
| $\overline{CS}$ | | | | |
| $\overline{CS}$ to Select | Delay to 90% of write current or to 90% of 100mV 10MHz Read signal envelope | - | 0.6 | µs |
| $\overline{CS}$ to Unselect | Delay to 90% of write current | - | 0.6 | µs |
| HSn | | | | |
| HS0, 1, 2, 3 to any Head | Delay to 90 % of 100mV 10MHz Read signal envelope | - | 0.4 | µs |
| WUS | | | | |
| Safe to Unsafe - TD1 | | 0.6 | 3.0 | µs |
| Unsafe to Safe - TD2 | | - | 1 | µs |
| Head Current | | | | |
| Prop. Delay - TD3 | From 50 % points, Lh=0µh, Rh=0Ω | - | 32 | ns |
| Asymmetry | WD has 50 % duty cycle and 1ns rise/fall time, Lh=0µh, Rh=0Ω | - | 0.5 | ns |
| Rise/Fall Time | 10% - 90% points, Lh=0µh, Rh=0Ω | - | 9 | ns |

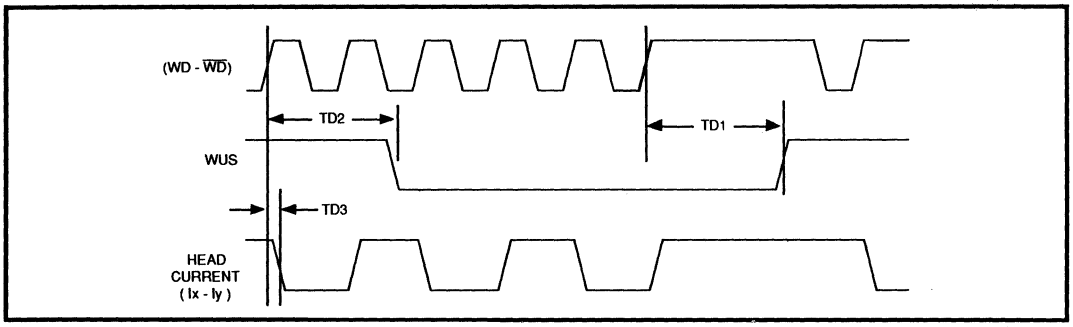



**FIGURE 1: Write Mode Timing Diagram**

## APPLICATIONS INFORMATION

The specifications, provided in the data section, account for the worst case values of each parameter taken individually. In actual operation, the effects of worst case conditions on many parameters correlate. Tables 3 & 4 demonstrate this for several key parameters. Notice that under the conditions of worst case input noise, the higher read back signal resulting from the higher input impedance can compensate for the higher input noise. Accounting for this correlation in your analysis will be more representative of actual performance.

**TABLE 3: Key Parameters Under Worst Case Input Noise Conditions**

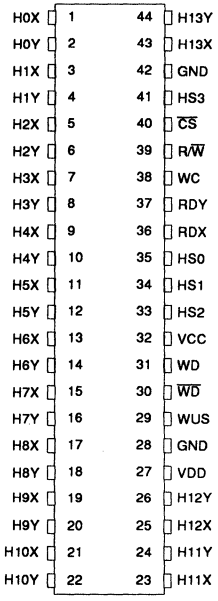
| PARAMETER | Tj = 25°C | Tj = 135°C | UNITS |
|---|---|---|---|
| Input Noise Voltage (Max.) | 0.70 | 0.85 | nV/$\sqrt{Hz}$ |
| Differential Input Resistance (Min.) | 390 | 420 | Ω |
| Differential Input Capacitance (Max.) | 32 | 34 | pF |

**TABLE 4: Key Parameters Under Worst Case Input Impedance Conditions**

| PARAMETER | Tj = 25°C | Tj = 135°C | UNITS |
|---|---|---|---|
| Input Noise Voltage (Max.) | 0.58 | 0.71 | nV/$\sqrt{Hz}$ |
| Differential Input Resistance (Min.) | 310 | 350 | Ω |
| Differential Input Capacitance (Max.) | 33 | 35 | pF |

# SSI 32R5281R
# 14-Channel Two-Terminal Read/Write Device

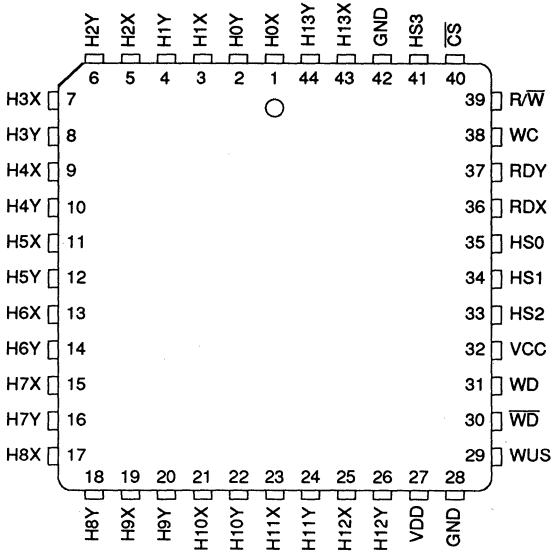
## PACKAGE PIN DESIGNATIONS
(Top View)




**44-Lead SOM**

**THERMAL CHARACTERISTICS: Øja**

| | |
|---|---|
| 44-Lead SOM | 50°C/W |
| 44-PLCC | 60°C/W |




**44-Pin PLCC**

**Advance Information:** Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.



Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 573-6000, FAX (714) 573-6914

silicon systems®
A TDK Group Company

# SSI 32R1200/1201
## +5V, 2, 4-Channel, 3-Terminal Read/Write Device

**Advance Information**

August 1992

## DESCRIPTION

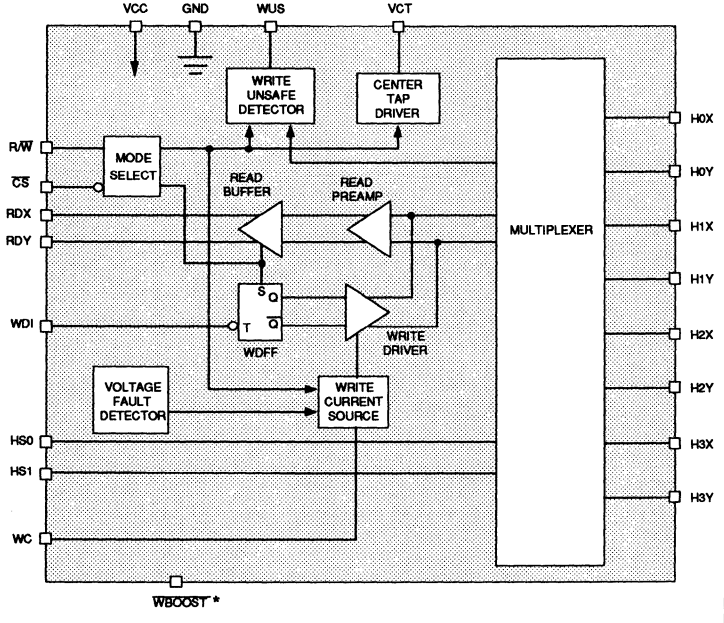
The SSI 32R1200/1201 are bipolar monolithic integrated circuits designed for use with center-tapped ferrite or MIG recording heads. They provide a low noise read path, write current control, and data protection circuitry for as many as 4 channels. Power supply fault protection is provided by disabling the write current generator during power supply switching. A power down mode (idle) is provided to reduce power consumption to less than 10 mW. The SSI 32R1201 option provides a write current boost feature which can be selected without using additional external resistors.

The SSI 32R1200R/1201R option provides internal 750Ω damping resistors. Both devices require only a +5V power supply and are available in surface mount packages.

## FEATURES

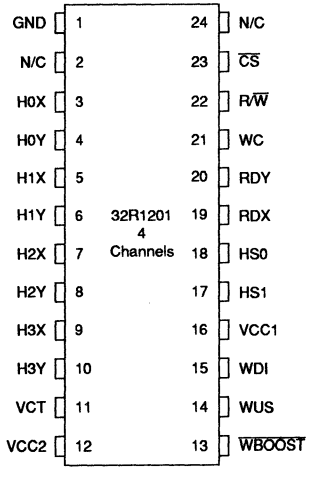
- **+5V only power supply**
- **Low power**
  - **Pd ≤ 200 mW read mode**
  - **Pd ≤ 10 mW idle mode**
- **High Performance**
  - **Read mode gain = 200 V/V**
  - **Input noise = 1.2 nV/√Hz max.**
  - **Input capacitance = 17 pF max.**
  - **Write current range = 15 - 50 mA**
  - **Head voltage swing = 6.0 Vpk**
- **Designed for center-tapped ferrite or MIG heads**
- **TTL selectable write current boost**
- **Power supply fault protection**
- **Includes write unsafe detection**
- **Enhanced Write to Read recovery**

## BLOCK DIAGRAM




* Not available in 20-pin SOL

## PIN DIAGRAM




**24-Pin SOL, VSOP**

CAUTION: Use handling procedures necessary for a static sensitive component.

# SSI 32R1200/1201
# +5V, 2, 4-Channel, 3-Terminal Read/Write Device

## DESCRIPTION

### WRITE MODE

A source of recording current is provided to the head center tap by an internal voltage reference, VCT. The current is conducted through the head alternately into an HnX terminal or an HnY terminal according to the state of an internal flip-flop. The flip-flop is triggered by the negative transition of the Write Data Input line (WDI). A proceeding read mode selection initializes the write data flip-flop, WDFF, to pass write current through the "X" side of the head. The write current magnitude is determined by the value of an external resistor Rwc connected between WC terminal and GND, and is given by:

Iw = K/Rwc, where K = Write Current Constant

In addition, this current can be given a 30% boost without switching in additional resistance values by pulling $\overline{\text{WBOOST}}$ low (32R1201/1201R only).

### WRITE MODE FAULT DETECT CIRCUIT

Several circuits are dedicated to detecting fault conditions associated with the write mode. A logical high level will be present at the Write Unsafe (WUS) terminal if any of the following write fault conditions are present:

- Head open
- Head center tap open
- Head shorted
- Head shorted to ground
- No write current
- WDI frequency too low
- Device in read or idle mode

The Write Unsafe output is open-collector and is usually terminated by an external resistor connected to VCC. Two negative transitions on WDI, after the fault is corrected, will clear the WUS flag.

A safe condition, WUS low, requires alternating voltage spikes on both HnX and HnY that exceed VCT + 1.5V at a rate equal to or higher than the Minimum Rate of WDI for Safe condition.

In addition, the power supply voltage level is monitored by a circuit that inhibits the write current if VCC is too low to permit valid data recording.

### READ MODE

In Read Mode, (R/$\overline{\text{W}}$ high and $\overline{\text{CS}}$ low), the circuit functions as a low noise differential amplifier. The read amplifier input terminals are determined by the Head Select inputs. The read amplifier outputs (RDX, RDY) are emitter follower sources, providing low impedance outputs. The amplifier gain polarity is non-inverting between HnX, HnY inputs and RDX, RDY outputs.

### IDLE MODE

Taking $\overline{\text{CS}}$ high selects the idle mode which switches the RDX and RDY outputs into a high impedance state and deactivates the device. Power consumption in this mode is held to a minimum.

### MODE SELECTION AND INDICATION CIRCUIT

Logical control inputs which select mode and head channel are TTL compatible. Their functions are described in Table1 and Table 2.

**TABLE 1: Head Select Table**

| Head Selected | HS1 | HS0 |
|---|---|---|
| 0 | 0 | 0 |
| 1 | 0 | 1 |
| 2 | 1 | 0 |
| 3 | 1 | 1 |

**TABLE 2: Mode Select Table**

| Mode Select | | Selected Mode | Indicating & Fault Outputs |
|---|---|---|---|
| $\overline{\text{CS}}$ | R/$\overline{\text{W}}$ | | WUS |
| 1 | X | Idle | off |
| 0 | 1 | Read | off |
| 0 | 0 | Write | on |

## PIN DESCRIPTION

| NAME | I/O | DESCRIPTION |
|---|---|---|
| HS0-HS1 | I | Head Select. Logical combinations select one of four Heads. See Table 1 |
| $\overline{CS}$ | I | Chip Select: a low level enables device. Has internal pull-up resistor. |
| R/$\overline{W}$ | I | Read/Write:a high level selects read mode. Has internal pull-up resistor. |
| WUS | O* | Write Unsafe: a high level indicates an unsafe writing condition |
| WDI | I | Write Data In: negative transition toggles direction of head current |
| H0X-H3X<br>H0Y-H3Y | I/O | X, Y head connections |
| RDX, RDY | O* | X, Y Read Data: differential read signal output |
| WC | - | Write Current: used to set the magnitude of the write current |
| $\overline{WBOOST}$** | I | A logic low signal on this pin increases the magnitude of write current by typically 30% |
| VCT | - | Voltage Center Tap: voltage source for head center tap |
| VCC | - | +5V |
| GND | - | Ground |

* When more than one R/W device is used, these signals can be wire OR'ed with unselected R/W devices.
** $\overline{WBOOST}$ available in 32R1201 only (16 and 24-pin options)

## ELECTRICAL SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND. Currents into device are positive.)

| PARAMETER | | RATING |
|---|---|---|
| DC Supply Voltage | VCC | -0.3 to +6 VDC |
| Digital Input Voltage Range<br>HS1, HS0, WDI, R/$\overline{W}$, $\overline{CS}$, $\overline{WBOOST}$ | | -0.3 to VCC + 0.3 VDC |
| Head Port Voltage Range | VH | -0.3 to VCC + 3.0 VDC |
| Write Current Pin Voltage | Vwc | -0.3 to VCC + 0.3 VDC |
| WUS Pin Voltage Range | Vwus | -0.3 to +6.0 VDC |
| Write Current Zero–Peak | IW | 60 mA |
| RDX, RDY Output Current | Io | -10 mA |
| RDX, RDY Pin Voltage | | VCC + 0.3 VDC |
| VCT Output Current Range | IVCT | -60 mA to +10 µA |
| WUS Output Current Range | Iwus | -0.1 to +10 mA |
| Storage Temperature Range | Tstg | -65 to 150 °C |
| Package Temperature (20 sec Reflow) | | 215 °C |
| WC Current Range | | 0 to -5 mA |

**RECOMMENDED OPERATION CONDITIONS**

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|---|
| DC Supply Voltage | VCC | | 4.75 | 5.0 | 5.25 | VDC |
| Head Inductance | Lh | | 1 | | 15 | µH |
| Damping Resistor | Rd | 32R1200/1201 only | 500 | | 2000 | Ω |
| Write Current Range | IW | | 15 | | 50 | mA |
| Junction Temperature Range | Tj | | +25 | | +135 | °C |

**DC CHARACTERISTICS**

(Unless otherwise specified, recommended operating conditions apply.)

**POWER SUPPLY**

| | | | | | |
|---|---|---|---|---|---|
| VCC Supply Current (ICC) | Read Mode | 28 | 38 | mA |
| | Idle Mode | 1.4 | 2.0 | mA |
| | Write Mode | 27 + Iw | 40 + Iw | mA |
| Power Dissipation | Read Mode | 140 | 200 | mW |
| | Idle Mode | 7 | 10.5 | mW |
| | Write Mode | | 210 +5.5 Iw | mW |

**DIGITAL I/O**

| | | | | | | |
|---|---|---|---|---|---|---|
| VIL | Input Low Voltage $\overline{CS}$, R/$\overline{W}$ WDI, HS0, HS1, $\overline{WBOOST}$ | | | | 0.8 | VDC |
| VIH | Input High Voltage $\overline{CS}$, R/$\overline{W}$ WDI, HS0, HS1, $\overline{WBOOST}$ | | 2.0 | | | VDC |
| IIL | Input Low Current $\overline{CS}$, R/$\overline{W}$ WDI, HS0, HS1, $\overline{WBOOST}$ | VIL = 0.4V | -0.4 | | | mA |
| IIH | Input High Current $\overline{CS}$, R/$\overline{W}$ WDI, HS0, HS1, $\overline{WBOOST}$ | VIH = 2.7V | | | 20 | µA |
| VOL | WUS Output Low Voltage | IOL = 4.0 mA | | | 0.5 | VDC |
| IOH | WUS Output High Current | VOH = 5.0V | | | 100 | µA |

**WRITE MODE**

| | | | | | | |
|---|---|---|---|---|---|---|
| Center Tap Voltage | VCT | Write Mode/Idle Mode | | Vcc - 0.9 | | VDC |
| Head Current (per side) | | Write Mode, 0 ≤ VCC ≤ 3.9V | -200 | | 200 | µA |
| Write Current Range | | 1.0 kΩ ≤ Rwc ≤ 3.3 kΩ | 15 | | 50 | mA |

**WRITE MODE** (continued)

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|
| Write Current Constant "K" | | 46 | 50 | 54 | mA-kΩ |
| Iwc to Head Current Gain | | | 20 | | mA/mA |
| $\overline{\text{WBOOST}}$ - Write Current Boost Factor* | $\overline{\text{WBOOST}}$ = Low | 1.25 | | 1.35 | mA/mA |
| Unselected Head Leakage Current | | | | 85 | µA |
| RDX, RDY Common Mode Output Voltage | | 2.0 | Vcc - 2.4 | 3.5 | VDC |
| RDX, RDY Leakage | RDX, RDY = 4V Idle Mode | -100 | | 100 | µA |
| WDI Minimum Pulse Width** | VIL ≥ 0.2VPWH | TBD | 11 | | ns |
| | VIN ≥ 2.4VPWL | TBD | 4 | | ns |
| * Not available in 20-pin SOL<br>** Refers to Figure 1 | | | | | |

**READ MODE**

| | | | | | |
|---|---|---|---|---|---|
| Center Tap Voltage | Read Mode | | Vcc - 1.5 | | VDC |
| Input Bias Current (per side) | | | 20 | 60 | µA |
| Output Offset Voltage | Read Mode | -200 | | +200 | mV |
| Common Mode Output Voltage | Read Mode | 2 | Vcc - 2.4 | 3.5 | VDC |
| Common Mode Output Voltage Change from Write to Read Mode | | -100 | | +100 | mV |

**FAULT DETECTION CHARACTERISTICS**

Unless otherwise specified recommended conditions apply, Iw = 30 mA, Lh = 5 µH, Rd = 750Ω. (SSI 32R1200/1201 only), F(WDI) = 10 MHz.

| | | | | | |
|---|---|---|---|---|---|
| Minimum Rate of WDI Input for Safe condition | | 500 | | | kHz |
| Maximum Rate of WDI Input for Unsafe condition | | | | 167 | kHz |
| Minimum voltage value for guaranteed write current turn-on | | 4.4 | | | VDC |
| Maximum voltage value for guaranteed write current turn-off | | | | 3.9 | VDC |

**DYNAMIC CHARACTERISTICS AND TIMING**

(Unless otherwise specified, recommended operating conditions apply and Iw = 30 mA, Lh = 5 µH, Rd = 750Ω (32R1200/1201) only, f(WDI) = 5 MHz, CL(RDX, RDY) ≤ 20 pF.)

**WRITE MODE**

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|
| Differential Head Voltage Swing | | 6.0 | 6.4 | | V(pk) |
| Unselected Head Transient Current | 1µH ≤ Lh ≤ 9.5µH | | | 2 | mA(pk) |
| Differential Output Capacitance | | | | 15 | pF |
| Differential Output Resistance | 32R1200/1201 | 10 | | | kΩ |
| | 32R1200R/1201R | 600 | | 960 | Ω |

**READ MODE**

| | | | | | |
|---|---|---|---|---|---|
| Differential Voltage Gain | Vin = 1 mV RMS @ 1 MHz | 160 | 200 | 240 | V/V |
| Bandwidth (-3dB) | \|Zs\| < 5Ω, Vin = 1 mVpp | 30 | 60 | | MHz |
| Input Noise Voltage | BW = 15 MHz, Lh = 0, Rh = 0 | | 0.85 | 1.2 | nV/√Hz |
| Differential Input Capacitance | Vin = mV RMS $f$ = 5MHz | | 14 | 17 | pF |
| Differential Input Resistance | 32R1200/1201 $f$ = 5 MHz | 2.0 | | | kΩ |
| | 32R1200R/1201R | 460 | | 860 | Ω |
| Dynamic Range | AC input voltage where gain falls to 90% of its small signal gain valve, $f$ = 5 MHz | 2 | | | mVpp |
| Common Mode Rejection Ratio | Vcm = 100 mVpp @1 MHz < $f$ < 10 MHz | 50 | 75 | | dB |
| Power Supply Rejection Ratio | ΔVcc =100 mVpp @1MHz < $f$ < 10 MHz | 45 | | | dB |
| Channel Separation | Unselected Channels: Vin = 20 mVpp 1 MHz < $f$ < 10 MHz | 45 | 54 | | dB |
| RDX,Y Single Ended Output Resistance | | | | 30 | Ω |
| Output Current | AC Coupled Load, RDX to RDY | ±1.5 | | | mA |

**SWITCHING CHARACTERISTICS**

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|---|
| R/$\overline{W}$ | Read to Write | R/$\overline{W}$ to 90% of write current | | 50 | 100 | ns |
| | Write to Read | R/$\overline{W}$ to 90% of 100 mV. 10 MHz Read signal envelope | | 0.15 | 1.0 | µs |
| $\overline{CS}$ | Unselect to Select | $\overline{CS}$ to 90% Ih or to 90% of 100 mV. 10 MHz Read signal envelope | | 1.0 | 2.0 | µs |
| | Select to Unselect | $\overline{CS}$ to 10% Ih | | 0.05 | 0.6 | µs |
| HS0, 1 to any Head | | To 90% of 100 mV. 10 MHz Read signal envelope | | | 0.6 | µs |
| WUS | Safe to Unsafe (TD1) | | 4 | 8 | 12 | µs |
| | R/$\overline{W}$ to Unsafe | | | | TBD | µs |
| | Unsafe to Safe (TD2) | Write mode, after fault cleared after 2nd transition | | | 150 | ns |
| | R/$\overline{W}$ to Safe | | | | * | µs |
| Head Current | | Rh = 0, Lh = 0 | | | | |
| | Prop. Delay (TD3) | From 50% points | | 25 | 30 | ns |
| | Asymmetry | WDI has 50% Duty Cycle and 1 ns Rise/Fall Time | | | 2 | ns |
| | Rise/Fall Time | 10% - 90% Points | | 4 | 20 | ns |
| Write to Read | | R/$\overline{W}$ to 90% | | 0.15 | 1.0 | µs |
| | | R/$\overline{W}$ to 10% Ih | | TBD | | ns |

* (Read to Write) + 2 Tw + TD2 where Tw = time between high to low WDI transitions

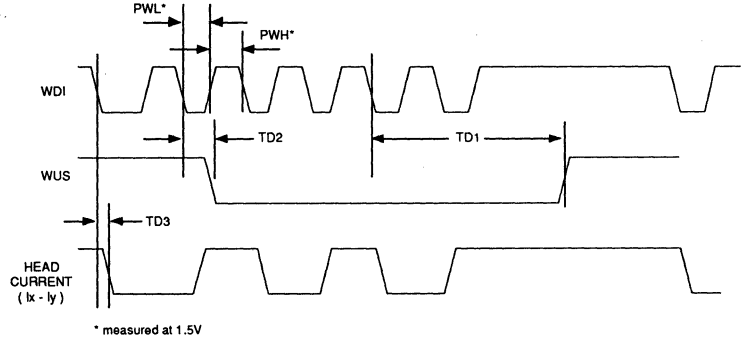
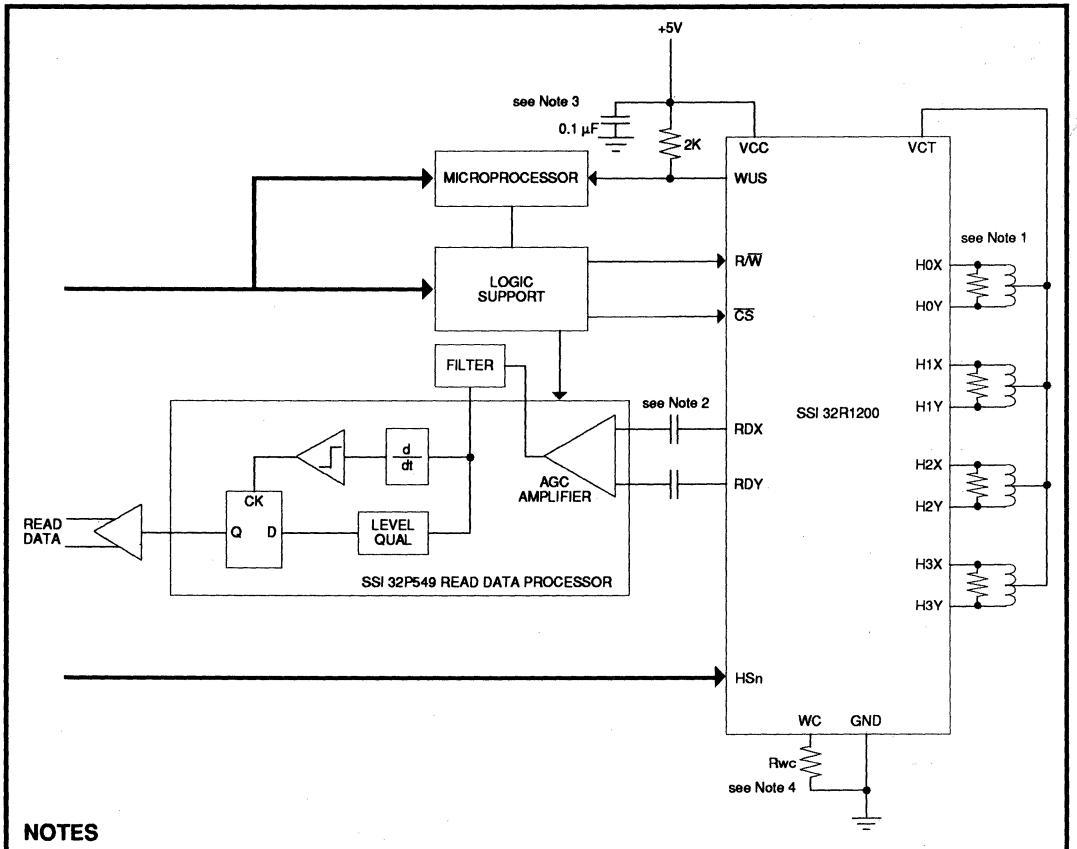



**FIGURE 1: Write Mode Timing Diagram**




**NOTES**

1. Damping resistors not required on 32R1200R versions.
2. Limit DC current from RDX and RDY to 100 µA and load capacitance to 20 pF. In multi-chip application these outputs can be wire-OR'ed.
3. The power bypassing capacitor must be located close to the 32R1200 with its ground returned directly to device ground, with as short a path as possible.
4. To reduce ringing due to stray capacitance this resistor should be located close to the 32R1200. Where this is not desirable a series resistor can be used to buffer a long WC line.

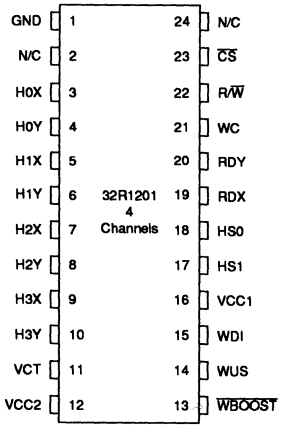
**FIGURE 2: Applications Information**

## PACKAGE PIN DESIGNATIONS

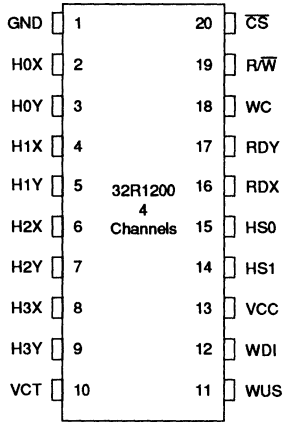
(Top View)

**THERMAL CHARACTERISTICS: θja**

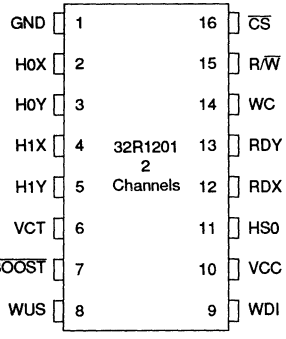
| | | |
|---|---|---|
| 24-lead | SOL | 80°C/W |
| 20-lead | SOL | 80°C/W |
| 16-lead | SOL | 105°C/W |
| 24-lead | VSOP | 110°C/W |
| 20-lead | VSOP | 125°C/W |




**24-Pin SOL, SOV**




**20-Pin SOL, SOV**




**16-Pin SOL**

**Advance Information:** Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.



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**Notes:**

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A TDK Group Company

# SSI 32R1203R
## +5V, 2, 4-Channel, 3-Terminal Read/Write Device
## Advance Information

December 1992

## DESCRIPTION

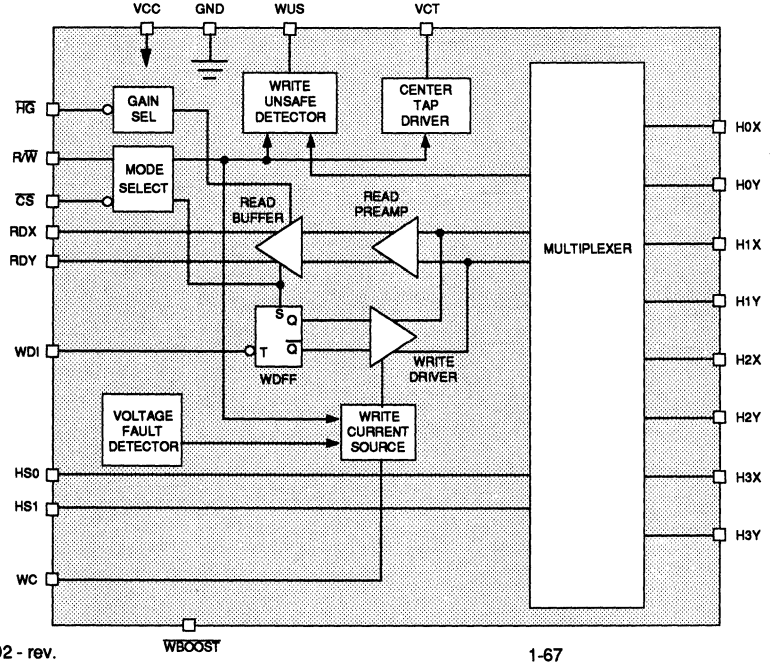
The SSI 32R1203R is a bipolar monolithic integrated circuit designed for use with center-tapped ferrite or MIG recording heads. It provides a low noise read path with selectable gains of 75 and 250 V/V, write current control, and data protection circuitry for as many as 4 channels. Power supply fault protection is provided by disabling the write current generator during power sequencing. A power down mode (idle) is provided to reduce power consumption to less than 10 mW. Included is a write current boost feature which can be selected without using additional external resistors.

Internal 750Ω damping resistors are provided. It requires only a +5V power supply and is available in a surface mount package.

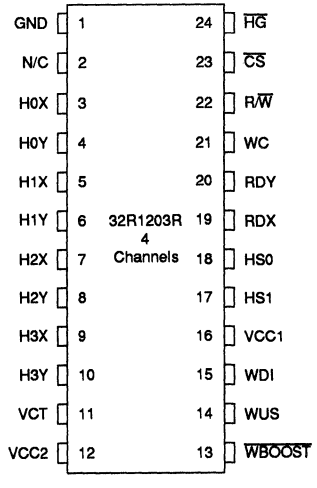
## FEATURES

- **Dual gain mode, 250 V/V and 75 V/V**
- **+5V only power supply**
- **Low power**
  - **Pd ≤ 220 mW read mode**
  - **Pd ≤ 10 mW idle mode**
- **High Performance**
  - **Dual gain mode, 250 V/V and 75 V/V**
  - **Input noise = 1.2 nV/√Hz max.**
  - **Input capacitance = 17 pF max.**
  - **Write current range = 15 - 50 mA**
  - **Head voltage swing = 6.0 Vpk**
- **Designed for center-tapped ferrite or MIG heads**
- **TTL selectable write current boost**
- **Power supply fault protection**
- **Includes write unsafe detection**
- **Enhanced Write to Read recovery**

## BLOCK DIAGRAM




## PIN DIAGRAM




**24-Pin SOV**

CAUTION: Use handling procedures necessary for a static sensitive component.

# SSI 32R1203R
# +5V, 2, 4-Channel, 3-Terminal Read/Write Device

## DESCRIPTION

### WRITE MODE

A source of recording current is provided to the head center tap by an internal voltage reference, VCT. The current is conducted through the head alternately into an HnX terminal or an HnY terminal according to the state of an internal flip-flop. The flip-flop is triggered by the negative transition of the Write Data Input line (WDI). A proceeding read mode selection initializes the write data flip-flop, WDFF, to pass write current through the "X" side of the head. The write current magnitude is determined by the value of an external resistor Rwc connected between WC terminal and GND, and is given by:

Iw = K/Rwc, where K = Write Current Constant

In addition, this current can be given a 30% boost without switching in additional resistance values by pulling $\overline{\text{WBOOST}}$ low .

### WRITE MODE FAULT DETECT CIRCUIT

Several circuits are dedicated to detecting fault conditions associated with the write mode. A logical high level will be present at the Write Unsafe (WUS) terminal if any of the following write fault conditions are present:

- Head open
- Head center tap open
- Head shorted
- Head shorted to ground
- No write current
- WDI frequency too low
- Device in read or idle mode

The Write Unsafe output is open-collector and is usually terminated by an external resistor connected to VCC. Two negative transitions on WDI, after the fault is corrected, will clear the WUS flag.

A safe condition, WUS low , requires alternating voltage spikes on both HnX and HnY that exceed VCT + 1.5V at a rate equal to or higher than the Minimum Rate of WDI for Safe condition.

In addition, the power supply voltage level is monitored by a circuit that inhibits the write current if VCC is too low to permit valid data recording.

### READ MODE

In Read Mode, (R/$\overline{\text{W}}$ high and $\overline{\text{CS}}$ low), the circuit functions as a low noise gain selectable differential amplifier. The read amplifier input terminals are determined by the Head Select inputs. The read amplifier outputs (RDX, RDY) are emitter follower sources, providing low impedance outputs. The amplifier gain polarity is non-inverting between HnX, HnY inputs and RDX, RDY outputs. Taking $\overline{\text{HG}}$ low selects high gain (250 V/V). Taking $\overline{\text{HG}}$ high or open selects low gain (75 V/V).

### IDLE MODE

Taking $\overline{\text{CS}}$ high selects the idle mode which switches the RDX and RDY outputs into a high impedance state and deactivates the device. Power consumption in this mode is held to a minimum.

### MODE SELECTION AND INDICATION CIRCUIT

Logical control inputs which select mode and head channel are TTL compatible. Their functions are described in Table1 and Table 2.

**TABLE 1: Head Select Table**

| Head Selected | HS1 | HS0 |
|---|---|---|
| 0 | 0 | 0 |
| 1 | 0 | 1 |
| 2 | 1 | 0 |
| 3 | 1 | 1 |

**TABLE 2: Mode Select Table**

| Mode Select | | Selected Mode | Indicating & Fault Outputs |
|---|---|---|---|
| $\overline{\text{CS}}$ | R/$\overline{\text{W}}$ | | WUS |
| 1 | X | Idle | off |
| 0 | 1 | Read | off |
| 0 | 0 | Write | on |

## PIN DESCRIPTIONS

| NAME | I/O | DESCRIPTION |
|---|---|---|
| HS0-HS1 | I | Head Select: Logical combinations select one of four Heads. See Table 1 |
| $\overline{CS}$ | I | Chip Select: a low level enables device. Has internal pull-up resistor. |
| R/$\overline{W}$ | I | Read/Write: a high level selects read mode. Has internal pull-up resistor. |
| WUS | O* | Write Unsafe: a high level indicates an unsafe writing condition |
| WDI | I | Write Data In: negative transition toggles direction of head current |
| H0X-H3X<br>H0Y-H3Y | I/O | X, Y head connections |
| RDX, RDY | O* | X, Y Read Data: differential read signal output |
| WC | - | Write Current: used to set the magnitude of the write current |
| $\overline{WBOOST}$ | I | A logic low signal on this pin increases the magnitude of write current by typically 30% |
| VCT | - | Voltage Center Tap: voltage source for head center tap |
| VCC1, VCC2 | - | +5V |
| GND | - | Ground |
| $\overline{HG}$ | I | Gain select: $\overline{HG}$ low selects 250 V/V. $\overline{HG}$ high or open selects 75 V/V. |
| * When more than one R/W device is used, these signals can be wire OR'ed with unselected R/W devices. | | |

## ELECTRICAL SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND. Currents into device are positive.)

| PARAMETER | | RATING |
|---|---|---|
| DC Supply Voltage | VCC | -0.3 to +6 VDC |
| Digital Input Voltage Range<br>HS1, HS0, WDI, R/$\overline{W}$, $\overline{CS}$, $\overline{WBOOST}$, $\overline{HG}$ | | -0.3 to VCC + 0.3 VDC |
| Head Port Voltage Range | VH | -0.3 to VCC + 3.0 VDC |
| Write Current Pin Voltage | Vwc | -0.3 to VCC + 0.3 VDC |
| WUS Pin Voltage Range | Vwus | -0.3 to +6.0 VDC |
| Write Current Zero–Peak | IW | 60 mA |
| RDX, RDY Output Current | Io | -10 mA |
| RDX, RDY Pin Voltage | | VCC + 0.3 VDC |
| VCT Output Current Range | IVCT | -60 mA to +10 mA |
| WUS Output Current Range | Iwus | -0.1 mA to +10 mA |
| Storage Temperature Range | Tstg | -65 to 150 °C |
| Package Temperature (20 sec Reflow) | | 215 °C |

### RECOMMENDED OPERATION CONDITIONS

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|---|
| DC Supply Voltage | VCC | | 4.75 | 5.0 | 5.25 | VDC |
| Head Inductance | Lh | | 1 | | 15 | µH |
| Write Current Range | IW | | 15 | | 50 | mA |
| Junction Temperature Range | Tj | | +25 | | +135 | °C |

### DC CHARACTERISTICS

(Unless otherwise specified, recommended operating conditions apply.)

### POWER SUPPLY

| | | | | |
|---|---|---|---|---|
| VCC Supply Current (ICC) | Read Mode | 32 | 42 | mA |
| | Idle Mode | 1.4 | 2.0 | mA |
| | Write Mode | 31 + Iw | 44 + Iw | mA |
| Power Dissipation | Read Mode | 160 | 220 | mW |
| | Idle Mode | 7 | 10.5 | mW |
| | Write Mode | 155 + 5 Iw | 230 + 5.5 Iw | mW |

### DIGITAL I/O

| | | | | | | |
|---|---|---|---|---|---|---|
| VIL | Input Low Voltage $\overline{CS}$, R/$\overline{W}$ WDI, HS0, HS1, $\overline{WBOOST}$, $\overline{HG}$ | | | | 0.8 | VDC |
| VIH | Input High Voltage $\overline{CS}$, R/$\overline{W}$ WDI, HS0, HS1, $\overline{WBOOST}$, $\overline{HG}$ | | 2.0 | | | VDC |
| IIL | Input Low Current $\overline{CS}$, R/$\overline{W}$ WDI, HS0, HS1, $\overline{WBOOST}$, $\overline{HG}$ | VIL = 0.4V | -0.4 | | | mA |
| IIH | Input High Current $\overline{CS}$, R/$\overline{W}$ WDI, HS0, HS1, $\overline{WBOOST}$, $\overline{HG}$ | VIH = 2.7V | | | 20 | µA |
| VOL | WUS Output Low Voltage | IOL = 4.0 mA | | | 0.5 | VDC |
| IOH | WUS Output High Current | VOH = 5.0V | | | 100 | µA |

### WRITE MODE

| | | | | | | |
|---|---|---|---|---|---|---|
| Center Tap Voltage | VCT | Write Mode/Idle Mode | | Vcc - 0.9 | | VDC |
| Head Current (per side) | | Write Mode, 0 ≤ VCC ≤ 3.9V | -200 | | 200 | µA |
| Write Current Range | | 1.0 kΩ ≤ Rwc ≤ 3.3 kΩ | 15 | | 50 | mA |

**WRITE MODE** (continued)

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|
| Write Current Constant "K" | | 46 | 50 | 54 | mA-kΩ |
| Iwc to Head Current Gain | | | 20 | | mA/mA |
| $\overline{\text{WBOOST}}$ - Write Current Boost Factor | $\overline{\text{WBOOST}}$ = Low | 1.25 | | 1.35 | mA/mA |
| Unselected Head Leakage Current | | | | 85 | µA |
| RDX, RDY Common Mode Output Voltage | | 2.0 | Vcc - 2.4 | 3.5 | VDC |
| RDX, RDY Leakage | RDX, RDY = 4V Idle Mode | -100 | | 100 | µA |
| WDI Minimum Pulse Width* | VIL ≥ 0.2VPWH | TBD | 11 | | ns |
| | VIN ≥ 2.4VPWL | TBD | 4 | | ns |
| * Refers to Figure 1. | | | | | |

**READ MODE**

| | | | | | |
|---|---|---|---|---|---|
| Center Tap Voltage | Read Mode | | Vcc - 1.5 | | VDC |
| Input Bias Current (per side) | | | 20 | 60 | µA |
| Output Offset Voltage | Read Mode | -200 | | +200 | mV |
| Common Mode Output Voltage | Read Mode | 2 | Vcc - 2.4 | 3.5 | VDC |
| Common Mode Output Voltage Change from Write to Read Mode | | -100 | | +100 | mV |

**FAULT DETECTION CHARACTERISTICS**

Unless otherwise specified recommended conditions apply, Iw = 30 mA, Lh = 5 µH, F(WDI) = 10 MHz.

| | | | | | |
|---|---|---|---|---|---|
| Minimum Rate of WDI Input for Safe condition | | 150 | | | kHz |
| Maximum Rate of WDI Input for Unsafe condition | | | | 50 | kHz |
| Minimum voltage value for guaranteed write current turn-on | | 4.4 | | | VDC |
| Maximum voltage value for guaranteed write current turn-off | | | | 3.9 | VDC |

**DYNAMIC CHARACTERISTICS AND TIMING**

(Unless otherwise specified, recommended operating conditions apply and Iw = 30 mA, Lh = 5 µH, f(WDI) = 5 MHz, CL(RDX, RDY) ≤ 20 pF.)

**WRITE MODE**

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|
| Differential Head Voltage Swing | | 6.0 | 6.4 | | V(pk) |
| Unselected Head Transient Current | 1µH ≤ Lh ≤ 9.5µH | | | 2 | mA(pk) |
| Differential Output Capacitance | | | | 15 | pF |
| Differential Output Resistance | | 600 | | 960 | Ω |
| Differential Voltage Gain | Vin ≥ 1 mVrms @ 1 MHz | | | | |
| | $\overline{HG}$ = 0 | | 250 | | V/V |
| | $\overline{HG}$ = 1 or open | | 75 | | V/V |

**READ MODE**

| | | | | | |
|---|---|---|---|---|---|
| Differential Voltage Gain | Vin = 1 mVrms @ 1 MHz | 160 | 200 | 240 | V/V |
| Bandwidth (-3dB) | \|Zs\| < 5Ω, Vin = 1 mVpp | 30 | 60 | | MHz |
| Input Noise Voltage | BW = 15 MHz, Lh = 0, Rh = 0 | | 0.85 | 1.2 | nV/√Hz |
| Differential Input Capacitance | Vin = mVrms $f$ = 5MHz | | 14 | 17 | pF |
| Differential Input Resistance | | 460 | | 860 | Ω |
| Dynamic Range | AC input voltage where gain falls to 90% of its small signal gain value, $f$ = 5 MHz | 2 | | | mVpp |
| Common Mode Rejection Ratio | Vcm = 100 mVpp @1 MHz < $f$ < 10 MHz | 50 | 75 | | dB |
| Power Supply Rejection Ratio | ΔVcc =100 mVpp @1MHz < $f$ < 10 MHz | 45 | | | dB |
| Channel Separation | Unselected Channels: Vin = 20 mVpp 1 MHz < $f$ < 10 MHz | 45 | 54 | | dB |
| RDX,Y Single Ended Output Resistance | | | | 30 | Ω |
| Output Current | AC Coupled Load, RDX to RDY | ±1.5 | | | mA |

**SWITCHING CHARACTERISTICS**

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|---|
| R/$\overline{W}$ | Read to Write | R/$\overline{W}$ to 90% of write current | | 50 | 100 | ns |
| | Write to Read | R/$\overline{W}$ to 90% of 100 mV. 10 MHz Read signal envelope | | 0.15 | 1.0 | µs |
| $\overline{CS}$ | Unselect to Select | $\overline{CS}$ to 90% Ih or to 90% of 100 mV. 10 MHz Read signal envelope | | 1.0 | 2.0 | µs |
| | Select to Unselect | $\overline{CS}$ to 10% Ih | | 0.05 | 0.6 | µs |
| HS0, 1 to any Head | | To 90% of 100 mV. 10 MHz Read signal envelope | | | 0.6 | µs |
| WUS | Safe to Unsafe (TD1) | | 13 | | 40 | µs |
| | R/$\overline{W}$ to Unsafe | | | | TBD | µs |
| | Unsafe to Safe (TD2) | Write mode, after fault cleared after 2nd transition | | | 150 | ns |
| | R/$\overline{W}$ to Safe | | | | * | µs |
| Head Current | | Rh = 0, Lh = 0 | | | | |
| | Prop. Delay (TD3) | From 50% points | | 25 | 30 | ns |
| | Asymmetry | WDI has 50% Duty Cycle and 1 ns Rise/Fall Time | | | 2 | ns |
| | Rise/Fall Time | 10% - 90% Points | | 4 | 20 | ns |
| Write to Read | | R/$\overline{W}$ to 90% | | 0.15 | 1.0 | µs |
| | | R/$\overline{W}$ to 10% Ih | | TBD | | ns |

* (Read to Write) + 2 Tw + TD2 where Tw = time between high to low WDI transitions

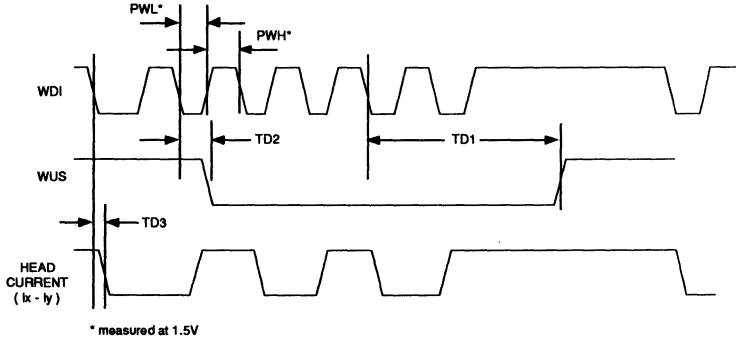
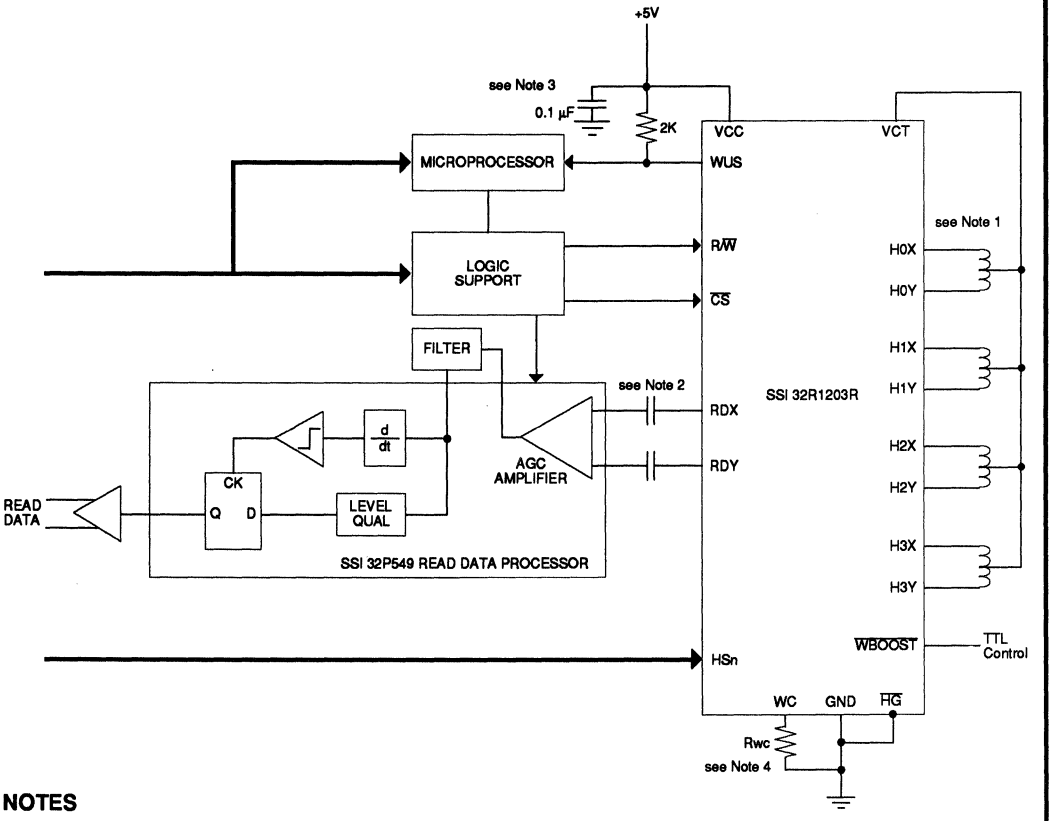



**FIGURE 1: Write Mode Timing Diagram**

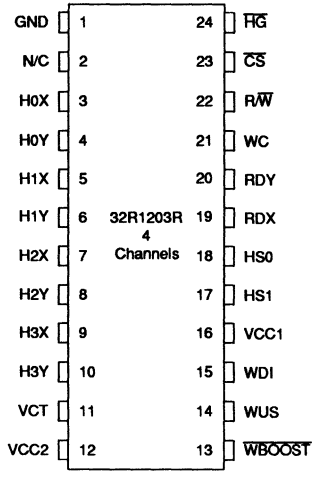



**NOTES**

1. Limit DC current from RDX and RDY to 100 µA and load capacitance to 20 pF. In multi-chip application these outputs can be wire-OR'ed.
2. The power bypassing capacitor must be located close to the 32R1203R with its ground returned directly to device ground, with as short a path as possible.
3. To reduce ringing due to stray capacitance this resistor should be located close to the 32R1203R. Where this is not desirable a series resistor can be used to buffer a long WC line.

**FIGURE 2: Applications Information**

## PACKAGE PIN DESIGNATIONS
(Top View)




**24-Lead SOV**

**THERMAL CHARACTERISTICS: θja**

| | | |
|---|---|---|
| 24-lead | VSOP | 110°C/W |

**Advance Information:** Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.



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**Notes:**

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# SSI 32R1220/1221/1222
## +5V, 2, 4-Channel Ferrite/MIG Read/Write Device

1

**Advance Information**

December 1992

## DESCRIPTION

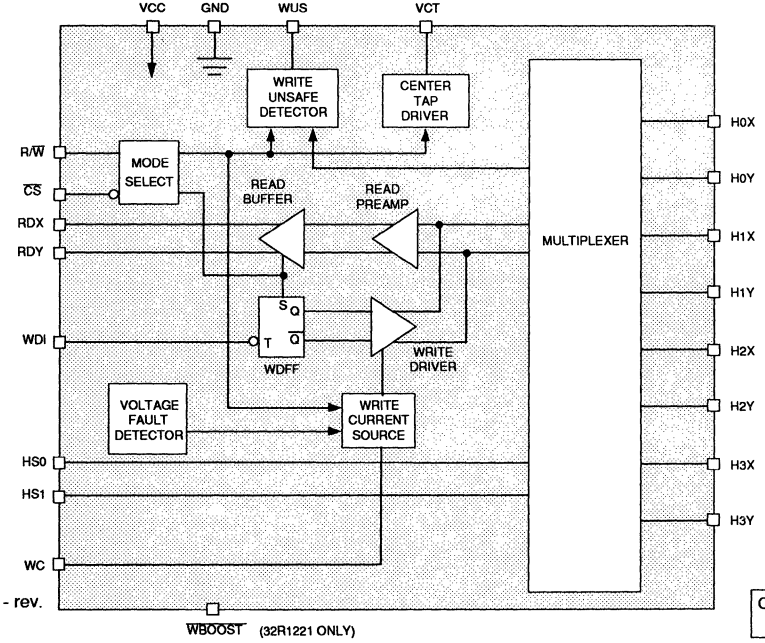
The SSI 32R1220/1221/1222 are bipolar monolithic integrated circuits designed for use with center-tapped ferrite or MIG recording heads. They provide a low noise read path, write current control, and data protection circuitry for as many as 4 channels. Power supply fault protection is provided by disabling the write current generator during power sequencing. A power down mode (idle) is provided to reduce power consumption to less than 10 mW. The SSI 32R1221 option provides write current boost feature which can be selected without using additional external resistors.

The SSI 32R1222 option provides a bond option compatible with other available three-terminal Read/Write devices.

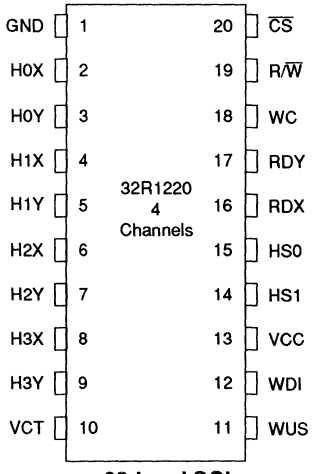
## FEATURES

- **+5V (± 10%) only power supply**
- **Low power**
  - **Pd =150 mW Read mode (NOM)**
  - **Pd ≤ 5 mW Idle mode (NOM)**
- **High Performance**
  - **Read mode gain = 250 V/V**
  - **Input noise = 0.9 nV/√Hz max.**
  - **Input capacitance = 19 pF max.**
  - **Write current range = 10 - 30 mA**
  - **Head voltage swing = 6.0 Vpk Nom**
- **Designed for center-tapped ferrite or MIG heads**
- **TTL selectable write current boost**
- **Pin compatible with 32R1200**
- **Power supply fault protection**
- **Write unsafe detection**
- **Enhanced Write to Read recovery**

## BLOCK DIAGRAM




## PIN DIAGRAM




**20-Lead SOL**

CAUTION: Use handling procedures necessary for a static sensitive component.

# SSI 32R1220/1221/1222
# +5V, 2, 4-Channel Ferrite/MIG Read/Write Device

## DESCRIPTION

### WRITE MODE

A source of recording current is provided to the head center tap by an internal voltage reference, VCT. The current is conducted through the head alternately into an HnX terminal or an HnY terminal according to the state of an internal flip-flop. The flip-flop is triggered by the negative transition of the Write Data Input line (WDI). A proceeding Read mode selection initializes the write data flip-flop, WDFF, to pass write current through the "X" side of the head. The write current magnitude is determined by the value of an external resistor Rwc connected between WC terminal and GND, and is given by:

Iw = K/Rwc, where K = Write Current Constant

In addition this current can be given a 33% boost, without switching in additional resistance values, by pulling $\overline{\text{WBOOST}}$ low (32R1221/1221R only).

### WRITE MODE FAULT DETECT CIRCUIT

Several circuits are dedicated to detecting fault conditions associated with the Write mode. A logical high level will be present at the Write Unsafe (WUS) terminal if any of the following write fault conditions are present:

- Head open
- Head center tap open
- Head shorted
- Head shorted to ground
- No write current
- WDI frequency too low
- Device in Read or Idle mode

The Write Unsafe output is open-collector and is usually terminated by an external resistor connected to VCC. Two negative transitions on WDI, after the fault is corrected, will clear the WUS flag.

Additionally, a power voltage monitoring circuit is used to detect VCC voltage level. If it is too low to permit valid data recording, write current is inhibited. With VCC voltage level above the inhibiting value, control of write current is provided by the mode selection inputs.

### READ MODE

In Read Mode, (R/$\overline{\text{W}}$ high and $\overline{\text{CS}}$ low), the circuit functions as a low noise differential amplifier. The read amplifier input terminals are determined by the Head Select inputs. The read amplifier outputs (RDX, RDY) are emitter follower sources, providing low impedance outputs. The amplifier gain polarity is non-inverting between HnX, HnY inputs and RDX, RDY outputs.

### IDLE MODE

Taking $\overline{\text{CS}}$ high selects the Idle mode which switches the RDX and RDY outputs into a high impedance state and deactivates the device. Power consumption in this mode is held to a minimum.

### MODE SELECTION AND INDICATION CIRCUIT

Logical control inputs which select mode and head channel are TTL compatible. Their functions are described in Table1 and Table 2.

**TABLE 1: Head Select Table**

| Head Selected | HS1 | HS0 |
|---|---|---|
| 0 | 0 | 0 |
| 1 | 0 | 1 |
| 2 | 1 | 0 |
| 3 | 1 | 1 |

**TABLE 2: Mode Select Table**

| Mode Select | | Selected Mode | Indicating & Fault Outputs |
|---|---|---|---|
| $\overline{\text{CS}}$ | R/$\overline{\text{W}}$ | | WUS |
| 1 | X | Idle | off |
| 0 | 1 | Read | off |
| 0 | 0 | Write | on* |

* Provided that no fault is detected.

## PIN DESCRIPTION

| NAME | I/O | DESCRIPTION |
|---|---|---|
| HS0-HS1 | I | Head Select. Logical combinations select one of four Heads. See Table 1. |
| $\overline{CS}$ | I | Chip Select: a low level enables device. Has internal pull-up resistor. |
| R/$\overline{W}$ | I | Read/Write:a high level selects Read mode. Has internal pull-up resistor. |
| WUS | O* | Write Unsafe: a high level indicates an unsafe writing condition. |
| WDI | I | Write Data In: negative transition toggles direction of head current. |
| H0X-H3X<br>H0Y-H3Y | I/O | X, Y head connections. |
| RDX, RDY | O* | X, Y Read Data: differential read signal output. |
| WC | - | Write Current: used to set the magnitude of the write current. |
| VCT | - | Voltage Center Tap: voltage source for head center tap. |
| VCC | - | +5V |
| GND | - | Ground |
| WBOOST** | I | A logic low signal on this pin increases the write current magnitude by typically 33%. |

* When more than one R/W device is used, these signals can be wire OR'ed.
** 32R1221 only.

## ELECTRICAL SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND. Currents into device are positive.)

| PARAMETER | | VALUE | UNITS |
|---|---|---|---|
| DC Supply Voltage | VCC | -0.3 to +6 | VDC |
| Digital Input Voltage Range<br>HS1, HS0, WDI, R/$\overline{W}$, $\overline{CS}$, $\overline{WBOOST}$ | | -0.3 to VCC + 0.3 | VDC |
| Head Port Voltage Range | VH | -0.3 to VCC + 0.3 | VDC |
| Write Current Pin Voltage | Vwc | -0.3 to VCC + 0.3 | VDC |
| WUS Pin Voltage Range | Vwus | -0.3 to +6.0 | VDC |
| Write Current Zero–Peak | IW | 60 | mA |
| RDX, RDY Output Current | Io | -10 | mA |
| RDX, RDY Pin Voltage | | VCC + 0.3 | VDC |
| VCT Output Current Range | IVCT | -60 | mA |
| WUS Output Current Range | Iwus | +12 | mA |
| Storage Temperature Range | Tstg | -65 to 150 | °C |
| Package Temperature (20 sec Reflow) | | 215 | °C |

### RECOMMENDED OPERATION CONDITIONS

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|---|
| DC Supply Voltage | VCC | | 4.5 | 5.0 | 5.5 | VDC |
| Head Inductance | Lh | | 1 | | 10 | µH |
| Damping Resistor | Rd | | 350 | | 2000 | Ω |
| Write Current Range | IW | | 10 | | 30 | mA |
| Iw • Lh Range | | | 20 | | 200 | mA • µH |
| Junction Temperature Range | Tj | | +25 | | +125 | °C |
| Operating Temperature Range | Ta | | 0 | | 70 | °C |

### DC CHARACTERISTICS

(Unless otherwise specified, recommended operating conditions apply.)

### POWER SUPPLY

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|
| VCC Supply Current (ICC) | Read Mode | | 30 | 40 | mA |
| | Idle Mode | | 1.0 | 1.8 | mA |
| | Write Mode | | 15 + Iw | 25 + Iw | mA |
| Power Dissipation | Read Mode | | 150 | 220 | mW |
| | Idle Mode | | 5 | 10 | mW |
| | Write Mode | | 75 + 5 Iw | 140 + 5 Iw | mW |

### DIGITAL I/O

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|---|
| VIL | Input Low Voltage $\overline{CS}$, R/$\overline{W}$ WDI, HS0, HS1 | | | | 0.8 | VDC |
| VIH | Input High Voltage $\overline{CS}$, R/$\overline{W}$ WDI, HS0, HS1 | | 2.0 | | | VDC |
| IIL | Input Low Current $\overline{CS}$, R/$\overline{W}$ WDI, HS0, HS1 | VIL = 0.4V | -0.1 | | | mA |
| IIH | Input High Current $\overline{CS}$, R/$\overline{W}$ WDI, HS0, HS1 | VIH = 2.7V | | | 20 | µA |
| VOL | WUS Output Low Voltage | IOL = 4.0 mA | | | 0.5 | VDC |
| IOH | WUS Output High Current | VOH = 5.0V | | | 100 | µA |

### WRITE MODE

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|
| Center Tap Voltage VCT | Write Mode | | Vcc - 0.9 | | VDC |
| Head Current (per side) | Write Mode, 0 ≤ VCC ≤ 3.75V | -200 | | 200 | µA |
| Write Current Range | 750 kΩ ≤ Rwc ≤ 3 kΩ | 10 | | 30 | mA |
| Write Current Constant "K" | | 27.6 | 30 | 32.4 | |
| Iwc to Head Current Gain | | | 20 | | mA/mA |
| Write Current Boost Factor * | $\overline{\text{WBOOST}}$ = Low | 1.28 | 1.33 | 1.38 | mA/mA |
| Unselected Head Leakage Current | DC Current | | | 85 | µA |
| RDX, RDY Leakage | RDX, RDY = 4V Idle Mode | -100 | | 100 | µA |
| WDI Pulse Width (see Figure 1) | Vil ≥ 0.2V PWH | 15 | | | ns |
| | PWL | 5 | | | ns |

* 32R1221 only

### READ MODE

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|
| Center Tap Voltage | Read Mode | | Vcc - 2.6 | | VDC |
| Input Bias Current (Differential) | | | 50 | 120 | µA |
| Output Offset Voltage | Read Mode | -400 | | +400 | mV |
| Common Mode Output Voltage | Read Mode | 2 | Vcc - 2.3 | 3.5 | VDC |

### FAULT DETECTION CHARACTERISTICS

Unless otherwise specified recommended conditions apply, Iw = 15 mA, Lh = 5 µH, Rd = 750Ω. F(WDI) = 10 MHz.

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|
| Minimum Rate of WDI Input for Safe condition | | 1.25 | | | MHz |
| Maximum Rate of WDI Input for Unsafe condition | | | | 250 | kHz |
| Minimum voltage value for guaranteed write current turn-on | | 4.25 | | | VDC |
| Maximum voltage value for guaranteed write current turn-off | | | | 3.75 | VDC |

## DYNAMIC CHARACTERISTICS AND TIMING

(Unless otherwise specified, recommended operating conditions apply and Iw = 15 mA, Lh = 5 µH, Rd = 750Ω, f(WDI) = 5 MHz, CL(RDX, RDY) ≤ 20 pF.)

### WRITE MODE

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|
| Differential Head Voltage Swing | | 5.0 | 6.0 | | V(pk) |
| Unselected Head Transient Current | 1µH ≤ Lh ≤ 9.5µH | | | 2 | mA(pk) |
| Differential Output Capacitance | | | | 15 | pF |
| Differential Output Resistance | 32R1220/1221/1222 | 10 | | | kΩ |
| | 32R1220R/1221R/1222R | 600 | | 960 | Ω |

### READ MODE

| | | | | | |
|---|---|---|---|---|---|
| Differential Voltage Gain | Vin = 1 mV RMS | 200 | 250 | 300 | V/V |
| Bandwidth (-3dB) | \|Zs\| < 5Ω, Vin = 1 mVpp | 30 | 50 | | MHz |
| Input Noise Voltage | BW = 15 MHz, Lh = 0, Rh = 0 | | 0.65 | 0.9 | nV/√Hz |
| Differential Input Capacitance | | | 15 | 19 | pF |
| Differential Input Resistance | | 1.2 | 2.5 | | kΩ |
| Common Mode Rejection Ratio | Vcm = 100 mVpp@1 MHz < $f$ < 10 MHz | 50 | | | dB |
| Power Supply Rejection Ratio | Vcs =100 mVpp@1 MHz < $f$ < 10 MHz | 45 | | | dB |
| Channel Separation | Unselected Channels: Vin = 20 mVpp 1 MHz < $f$ < 10 MHz | 50 | | | dB |
| Single Ended Output Resistance | | | 25 | 50 | Ω |
| Output Current | AC Coupled Load, RDX to RDY | 1.0 | 1.5 | | mA |

## DYNAMIC CHARACTERISTICS AND TIMING (continued)

### SWITCHING CHARACTERISTICS

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|---|
| R/$\overline{W}$ | Read to Write | R/W to 90% of write current | | | 1.0 | µs |
| | Write to Read | R/W to 90% of 100 mV. 10 MHz Read signal envelope | | | 1.0 | µs |
| $\overline{CS}$ | Unselect to Select | $\overline{CS}$ to 90% Iw or to 90% of 100 mV. 10 MHz Read signal envelope | | | 1.0 | µs |
| | Select to Unselect | | | | 0.6 | µs |
| HS0, 1 to any Head | | To 90% of 100 mV. 10 MHz Read signal envelope | | | 0.6 | µs |
| WUS: | Safe to Unsafe (TD1) | Write Mode, loss of WDI | 1.6 | 4 | 8 | µs |
| | Unsafe to Safe (TD2) | Write Mode, resumption of WDI | | | 1.0 | µs |
| Head Current | | From 50% Points, Lh = 0 | | | | |
| | Prop. Delay - TD3 | Rh = 0 | | 15 | 30 | ns |
| | Asymmetry | WDI has 50% Duty Cycle and 1 ns Rise/Fall Time | | | 2 | ns |
| | Rise/Fall Time | 10% - 90% Points | | | 20 | ns |

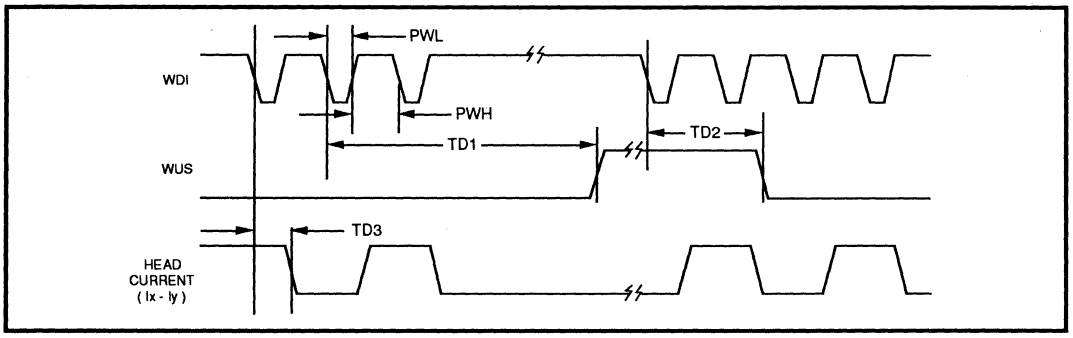
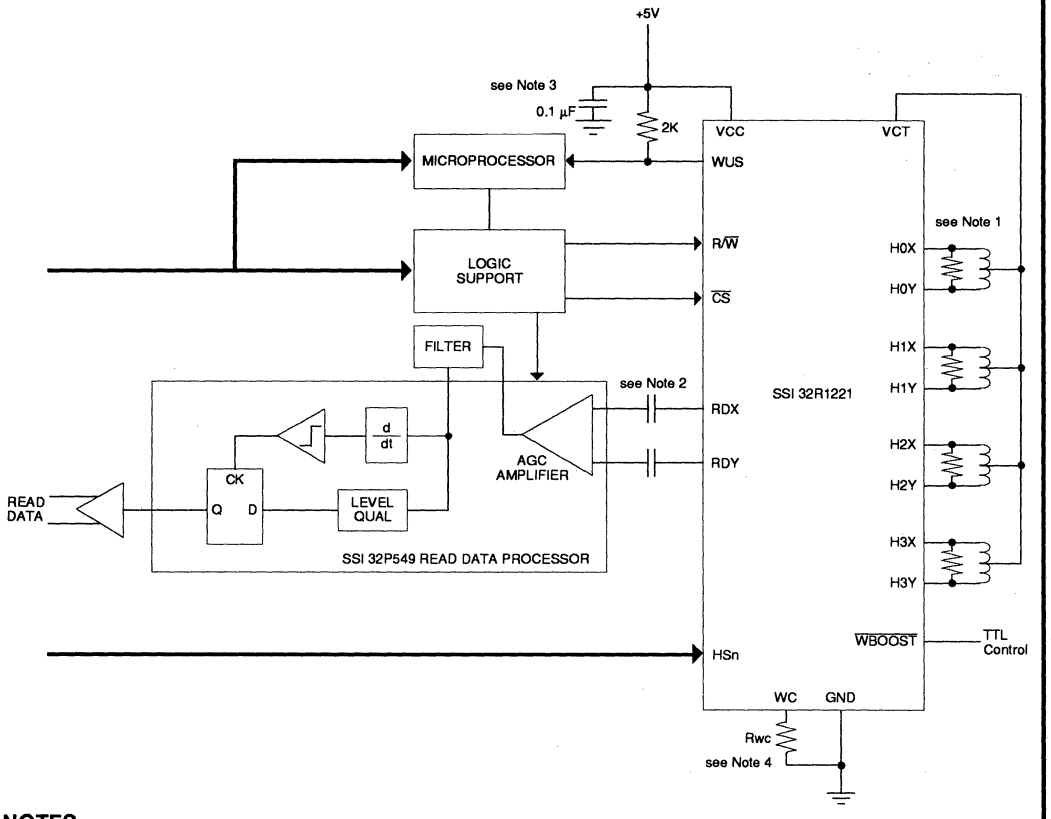



**FIGURE 1: Write Mode Timing Diagram**



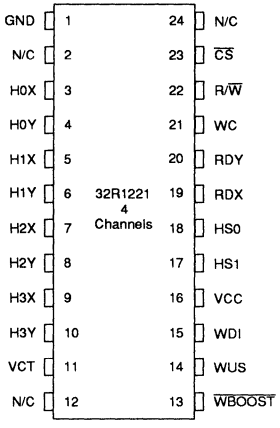

**NOTES**

1. Limit DC current from RDX and RDY to 100 µA and load capacitance to 20 pF. In multi-chip application these outputs can be wire-OR'ed.
2. The power bypassing capacitor must be located close to the device with its ground returned directly to device ground, with as short a path as possible.
3. To reduce ringing due to stray capacitance this resistor should be located close to the device. Where this is not desirable a series resistor can be used to buffer a long WC line.

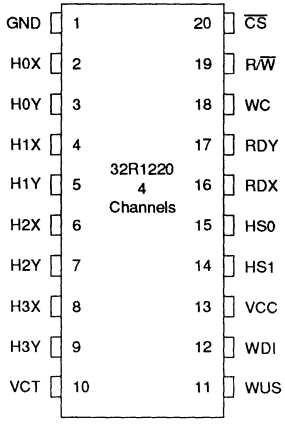
**FIGURE 2: Applications Information**

## PACKAGE PIN DESIGNATIONS

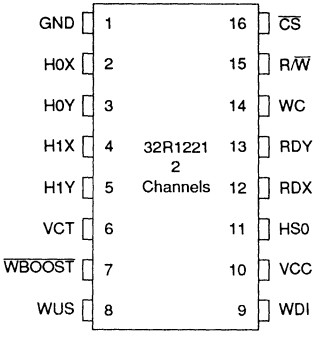
(Top View)



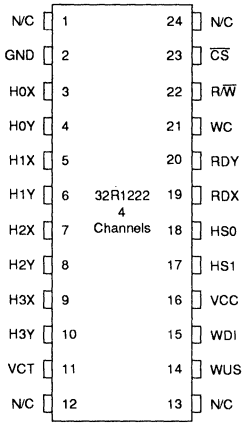

**24-Lead SOL, SOV**




**20-Lead SOL, SOV**




**16-Lead SOL, SON**




**24-Lead SOV**

**Advance Information:** Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.



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**Notes:**

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A TDK Group Company

# SSI 32R1510R
## MR Head Read/Write Device

**Advance Information**

January 1993

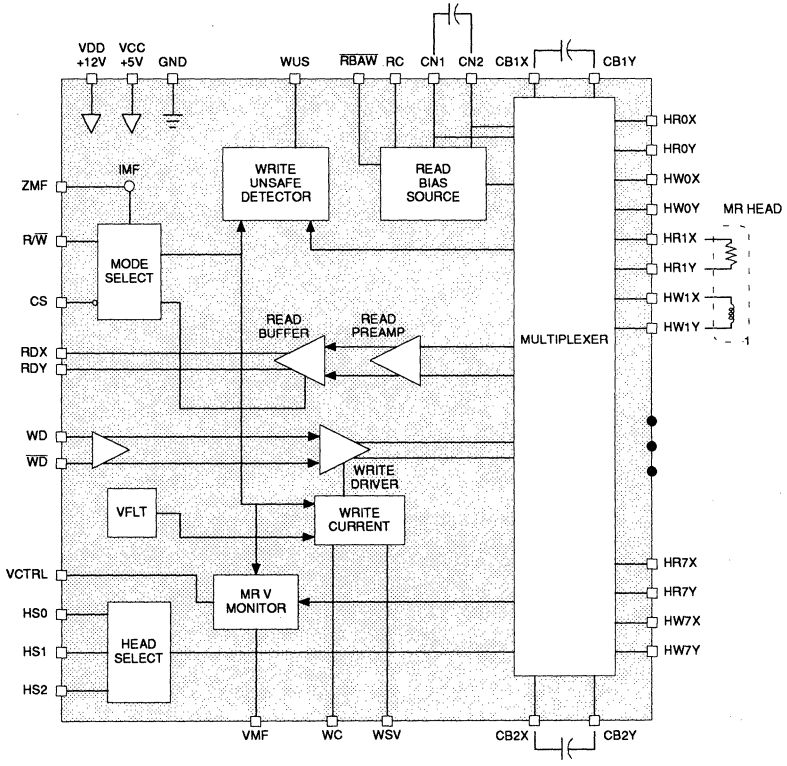
## DESCRIPTION

The SSI 32R1510R is an integrated circuit designed for use with Magneto-Resistive recording heads. It provides a write driver and a low noise read amplifier for up to 8 channels. The device requires +12V and +5 Volt power supplies and comes in a 68-pin PLCC package.

## FEATURES

- **Head Swing = 7.0 Vpp min**
- **Rise Time = 4 ns (Typ)**
- **Minimal external components**
- **Input Noise = 0.72 nV/ √ Hz**

## BLOCK DIAGRAM






CAUTION: Use handling procedures necessary for a static sensitive component.

## FUNCTIONAL DESCRIPTION

The SSI 32R1510R addresses up to 8 MR heads providing write drive or read amplification and MR current biasing. Head selection and mode control is accomplished with pins HSn, $\overline{CS}$ and R/$\overline{W}$ as shown in Tables 1 and 2.

### WRITE MODE

Taking both $\overline{CS}$ and R/$\overline{W}$ low selects Write mode which configures the 32R1510R as a current switch and activates the Write Unsafe (WUS) detect circuitry. Head current direction corresponds to the write data input level (WDX, WDY).

The magnitude of the write current is given by:

$$Iw = Vwc/Rwc$$

Rwc is connected from pin WC to GND. Note the actual head current Ihead is given by:

$$Ihead = Aw \cdot Iw/(1+Rh/Rd)$$

where Aw is the write current gain, Rh is the head resistance, and Rd is the damping resistance.

### WRITE MODE FAULT DETECT CIRCUIT (WUS)

Any of the following conditions will be indicated as a high level on the Write Unsafe, WUS open collector output:

- WDI frequency too low
- Device in Read or Idle mode
- Head open
- Head short to ground
- No Head current

In the case of a head short to ground, write current will be turned off to prevent excessive current dissipation. This will result in a pulsating WUS signal.

### LOW VOLTAGE FAULT PROTECT

The voltage fault detection circuit improves data security by disabling the write current generator during a low voltage fault or power startup regardless of mode. Note that WUS does not necessarily turn on to flag a power supply fault condition.

### READ BIAS ACTIVE IN WRITE ($\overline{RBAW}$)

The $\overline{RBAW}$ pin is a TTL control signal. A low level enables the MR bias current through the selected head in Write mode (Table 3). It can be used to speed up the write to read transition time. $\overline{RBAW}$ timing is shown in Figure 2.

### READ MODE

Taking $\overline{CS}$ low and R/$\overline{W}$ high selects Read mode which activates the bias current generator and the differential amplifier. The magnitude of the bias current is given by:

$$Ib = Ar \cdot Vrc/Rrc$$
$$= Kr/Rrc$$

where Ar is the bias current gain and Kr is the product of Ar and Vrc. Rrc is connected from pin RC to GND.

A voltage monitor, VMF, is provided for media biasing. In Read mode its output is set at the head bias voltage Vmr.

RDX and RDY are open collector outputs and should be terminated with 100Ω load resistors.

### IDLE MODE

Taking $\overline{CS}$ high selects Idle mode which switches the RDX and RDY outputs into a high impedance state and deactivates the internal write current source. This facilitates multi-device installations by allowing the read outputs to be wire OR'ed.

**TABLE 1: Mode Select/VMF Select**

| $\overline{CS}$ | R/$\overline{W}$ | VCTRL | MODE | VMF VALUE |
|---|---|---|---|---|
| 0 | 0 | X | Write | Dummy Head Center Voltage |
| 0 | 1 | X | Read | Selected Channel Center Voltage |
| 1 | X | 0 | Idle | High Impedance |
| 1 | X | 1 | Idle | Dummy Head Center Voltage |

**TABLE 2: Head Select**

| Head Selected | HS2 | HS1 | HS0 |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 |
| 2 | 0 | 1 | 0 |
| 3 | 0 | 1 | 1 |
| 4 | 1 | 0 | 0 |
| 5 | 1 | 0 | 1 |
| 6 | 1 | 1 | 0 |
| 7 | 1 | 1 | 1 |

**TABLE 3: Read Bias Active In Write**

| MODE | R/$\overline{W}$ | $\overline{RBAW}$ | MR Head Bias Current |
|---|---|---|---|
| Read | 1 | X | On |
| Write | 0 | 0 | On |
| | 0 | 1 or Open | Off |

## PIN DESCRIPTION

### CONTROL INPUT PINS

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| $\overline{CS}$ | I | Chip Select Input. A logical low level enables the circuit for a read or write operation. Has internal pull up. |
| R/$\overline{W}$ | I | Read/write select. A logical low level enables the write mode (when $\overline{CS}$ is low). Has internal pull up. |
| VCTRL | I | Voltage Control. In Idle mode, a high level selects VMF to supply a bias value. A low level selects high impedance. |
| $\overline{RBAW}$ | I | Read Bias Active In Write. A TTL low level enables the MR bias current through the selected head in both Read & Write modes. |
| HS0, HS1, HS2 | I | Head select inputs. Logical combinations select one of eight heads. See Table 2. Has internal pull down resistors. |

### HEAD TEMINAL PINS

| | | |
|---|---|---|
| HR0X - HR7X<br>HR0Y - HR7Y | I | MR read element X, Y connections. |
| HW0X - HR7X<br>HW0Y - HR7Y | O | MR write element X, Y, connections |

### DATA INPUT/OUTPUT PINS

| | | |
|---|---|---|
| WDX, WDY | I | Differential write data input. |
| RDX, RDY | O | Differential Read Data output. These open collector outputs are normally terminated in 100Ω resistors to VCC. |

### EXTERNAL COMPONENT CONNECTION PINS

| | | |
|---|---|---|
| WC | I/O | Resistor connected to GND to provide desired value of write current. |
| RC | | Resistor connected to GND to provide selected value of bias current. |
| CN1, CN2 | | Noise decoupling capacitor for MR bias source. |
| CB1X, CB1Y<br>CB2X, CB2Y | | DC blocking capacitors |

## PIN DESCRIPTION (continued)

### CIRCUIT MONITOR PINS

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| WUS | O | Write Unsafe is an open-collector output with the off-state indicating that conditions are not proper for a write operation. |
| WSV | O | Write Select Verify. Indicates that write current generator is active. |
| IMF | O | Current Monitor. Sinks 3 mA of current when device is actiive. |
| VMF | O | Voltage Monitor. Provides equivalent voltage to MR element bias midpoint [(V(HRnX) - V(HRnY))/2]. |

### POWER, GROUND PINS

| | | |
|---|---|---|
| VCC | I | +5V logic circuit supply. |
| VDD | I | +12V power supply. |
| GND | I | Power supply common. |

## ELECTRICAL SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS

Operation beyond the maximum ratings may damage the device.

| PARAMETER | RATING |
|---|---|
| Storage Temperature | -65 to 150°C |
| Junction Operating Temperature | +130°C |
| Positive Supply Voltage (VCC) | -0.3 to 6V |
| Positive Supply Voltage (VDD) | -0.3 to 14.0V |
| Voltage Applied to Logic Inputs | -0.3V to Vcc+0.3V |
| All other Pins | -0.3V to Vcc+0.3V |

## ELECTRICAL SPECIFICATIONS (continued)

### ELECTRICAL CHARACTERISTICS

Unless otherwise specified, 4.5V ≤ 5.5V, 10.8V ≤ VDD ≤ 13.2V, 0°C ≤ Ta ≤ 70°C.

Current maximums are currents with the highest absolute value.

#### POWER DISSIPATION

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| VCC Supply Current | Read Mode, Isense = 20 mA | | 12 | TBD | mA |
| | Write Mode Iw = 30 mA | | 18 | TBD | mA |
| | Idle Mode | | 7 | TBD | mA |
| VDD Supply Current | Read Mode, Isense = 20 mA | | 30+ Is • 1.2 | TBD | mA |
| | Write Mode Iw = 30 mA | | 34+Iw | TBD | mA |
| | Idle Mode | | 26 | TBD | mA |
| Power Dissipation | Read Mode Isense = 20 mA | | 480 + 1.2 • Is • VDD | | mW |
| | Write Mode Iw = 30 mA | | 500 + (VDD - 2) • Iw | | mW |
| | Idle Mode | | 340 | | mW |

#### DIGITAL INPUTS AND OUTPUTS

| | | | | | |
|---|---|---|---|---|---|
| WSV, WUS Output low Voltage | Iload = 4 mA | | | 0.5 | V |
| Input low voltage (VIL1) ($\overline{CS}$,R/$\overline{W}$,VCTRL,$\overline{RBAW}$,HS0-HS2) | | -0.3 | | 0.8 | V |
| Input high voltage (VIH1) ($\overline{CS}$,R/$\overline{W}$,VCTRL,$\overline{RBAW}$,HS0-HS2) | | 2.0 | | Vcc+0.3 | V |
| Input low current (IIL1) ($\overline{CS}$,R/$\overline{W}$,VCTRL,$\overline{RBAW}$,HS0-HS2) | VIL1=0.8V | -0.4 | | | mA |
| Input high current (IIH1) ($\overline{CS}$,R/$\overline{W}$,VCTRL,$\overline{RBAW}$,HS0-HS2) | VIH1 = 2.0V | | | 100 | µA |
| Input low Voltage (VIL3) (WDX, WDY) | | Vcc-2.2 | | VIH3-0.3 | V |
| Input high Voltage (VIH3) (WDX, WDY) | | VIL3 +0.3V | | Vcc-0.5 | V |
| Input low current (IIL3) (WDX, WDY) | VIL3=Vcc-1.4 | | | 50 | µA |
| Input high current (IIH3) (WDX, WDY) | VIH3 = Vcc-0.8 | | | 50 | µA |

## ELECTRICAL SPECIFICATIONS (continued)

### ANALOG OUTPUT

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| IMF Current | $\overline{CS}$ = 0 | 2.4 | 3 | 3.6 | mA |
| IMF Current | $\overline{CS}$ = 1 | | | 0.1 | mA |
| VMF Current | Sourcing | 4 | | | mA |
| | Sinking | 1 | | | mA |
| Voltage Monitor Output (VMF) | Read mode | Vmr-0.1 | Vmr | Vmr+0.1 | V |
| | Write in | | 5.5 | | |
| | Idle mode, VCTRL = 1 | | 5.5 | | |

### READ MODE

Test performed with 100Ω lead resistors from RDX & RDY to VCC

| | | | | | |
|---|---|---|---|---|---|
| Read Bias Current Gain (Ar) | Read Mode | | 20 | | mA/mA |
| | Idle Mode | | | 0.01 | mA/mA |
| Bias current setting Voltage (Vrc) | | | 2 | | V |
| "Kr" Factor | Kr=Ar • Vrc | 37.0 | 40 | 43.0 | V |
| Ih Bias Current (MR Element Bias Current) | Read Mode | 15 | | 25 | mA |
| Unselected bias Current | | | | 10 | uA |
| MR Head Bias Voltage (Vmr) | Selected Channel (Read) | | 5.5 | | V |
| | Unselected Channel (Read) | | 4.9 | | V |
| | Write, Idle Mode | | 4.9 | | V |
| MR Head Resistance (Rh) | | 10 | 15 | 25 | Ω |
| Differential Gain | | 100 | 150 | 180 | V/V |
| Differential Input Resistance | | | 210 | | Ω |
| Dynamic Range | Input Voltage where gain falls to 90% of its small signal gain value f = 5 MHz | 8 | | | mVpp |
| Input Referred Noise Voltage | | | 0.72 | 0.95 | nV/√ Hz |
| Differential Input Capacitance | | | 18 | | pF |
| Bandwidth | -3 dB, Vin = 1 mVpp Zs = 5Ω | 70 | 100 | | MHz |
| CMRR | Vin = 100 mVpp @ 5 MHZ | 55 | | | dB |
| PSRR | 100 mVpp @ 5 MHZ on VCC, VDD | 50 | | | dB |
| Channel Separation | | 45 | | | dB |

**READ MODE**(continued)

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Output Offset Voltage | | -300 | | 300 | mV |
| Output Voltage (common mode) | | | Vcc-0.6 | | VDC |
| Output Leakage Current | | | | 100 | 1µA |

**WRITE MODE**

| | | | | | |
|---|---|---|---|---|---|
| Write Current gain (Aw) | Rh = 0 | 0.96 | 0.99 | 1 | mA/mA |
| Write Current Voltage, Vwc | | 1.9 | 2.0 | 2.1 | V |
| Write Current range | | 10 | | 50 | mA |
| Differential Head Voltage Swing | | 7.0 | 8.0 | 9.0 | Vpp |
| Unselected Head current | DC | | | 0.2 | mA |
| | AC | | | 1 | mApp |
| Head differential load resistance | | 360 | 450 | 540 | Ω |
| VDD Fault Voltage | | 8.5 | | 10.0 | VDC |
| VCC Fault Voltage | | 3.5 | | 4.2 | VDC |
| Head Current (HnX, HnY) | Write Mode, 0 ≤ VCC ≤ 3.5V<br>0 ≤ VDD ≤ 8.5V | -200 | | +200 | µA |
| | Read/Idle Mode<br>0 ≤ VCC ≤ 5.5V<br>0 ≤ VDD ≤ 13.2V | -200 | | +200 | µA |

**SWITCHING CHARACTERISTICS**

Conditions: Head Variance Rh = ±10% max, CB1 = CB2 = 0.1 µF, Is = 20 mA, Iw = 30 mA

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Head Switching | to 90% of Read Envelope | | 1 | 2 | µs |
| Write-Read Mode | to 90% of Read Envelope | | 1 | 2 | µs |
| Read-Write Mode | to 90% of Write Current | | 0.2 | 0.5 | µs |
| Idle-Read/Write Mode | to 90% of Read Envelope | | 2 | 5 | µs |
| Read/Write - Idle Mode | | | 0.2 | 0.5 | µs |
| WUS Safe to Unsafe (TD1) | WDI Frequency too low | | 0.7 | 1.5 | µs |
| WUS Unsafe to Safe (TD2) | | | 0.1 | 0.3 | µs |
| WSV Delay Time | 50% R/W to 50% WSV | | | 0.5 | µs |
| IMF Delay Time | 50% CS/ to 50% IMF Current | | | 0.5 | µs |
| Write Current Rise/Fall time | Lh = 200 nH<br>Rh = 15 Ω<br>Iw = 30 mA | | 4 | 5 | ns |

**SWITCHING CHARACTERISTICS** (continued)

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Propagation delay | 50%(WDX-WDY) to 50%(Ix-Iy) | | 4 | | ns |
| Write current Asymmetry | Propagation delay difference | | | 0.5 | ns |

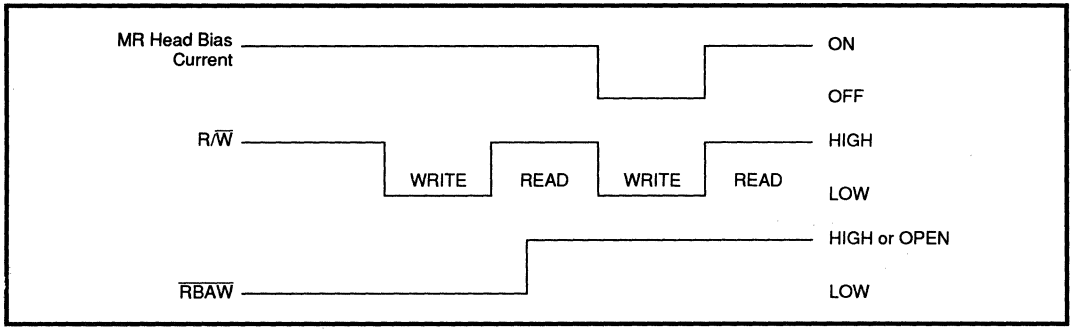



**FIGURE 2: Head Bias Current Timing**

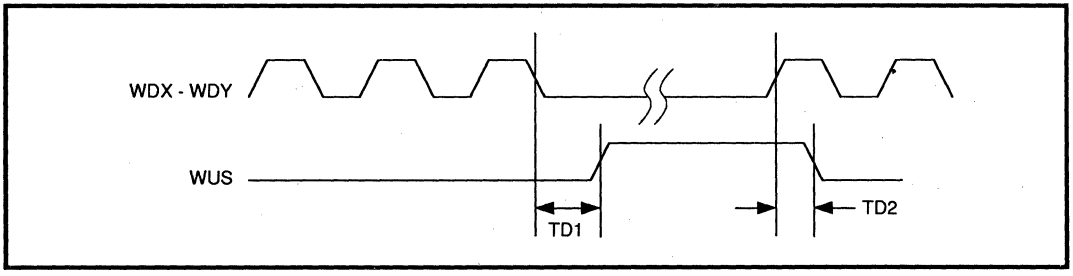
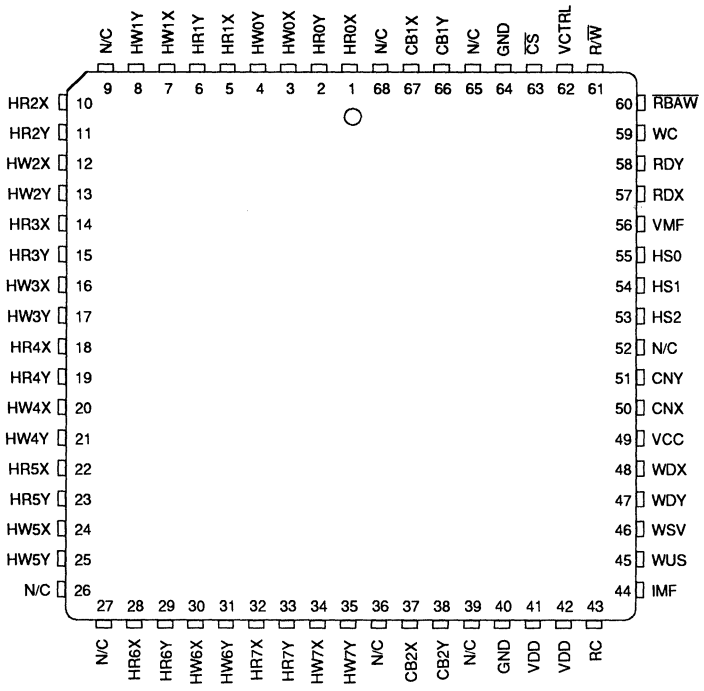



**FIGURE 3: WUS Timing**

## PACKAGE PIN DESIGNATIONS

(Top View)




**68-Pin PLCC**

**Advance Information:** Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.



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**Notes:**

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# SSI 32R2010R
## 10-Channel Thin Film Read/Write Device
## Preliminary Data

January 1993

## DESCRIPTION

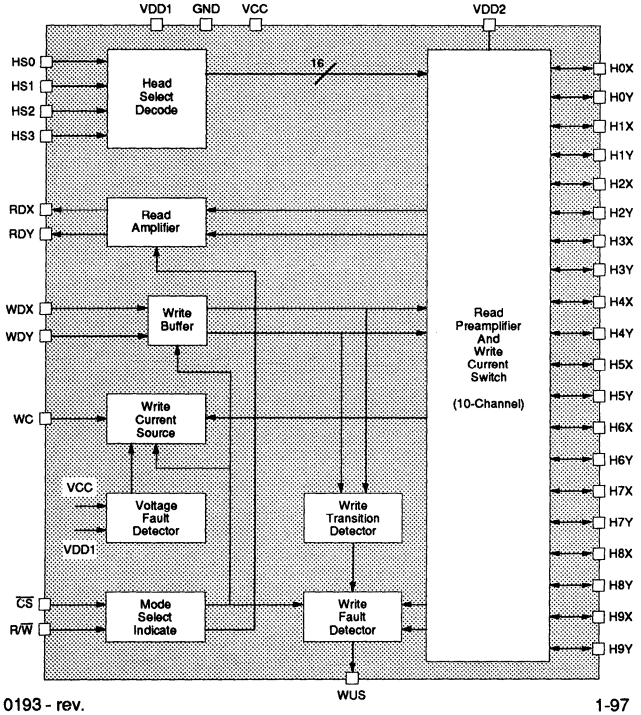
The SSI 32R2010R is an integrated read/write circuit designed for use with two terminal heads in disk drive systems. The device contains up to ten channels of read amplifiers and write drivers and also has an internal write current source. An internal 330Ω damping resistor is supplied in write mode, which is switched to 1 kΩ in read mode.

The circuit operates on +5V and +12V power supplies and is available in a 10 channel, 36 pin SO package.

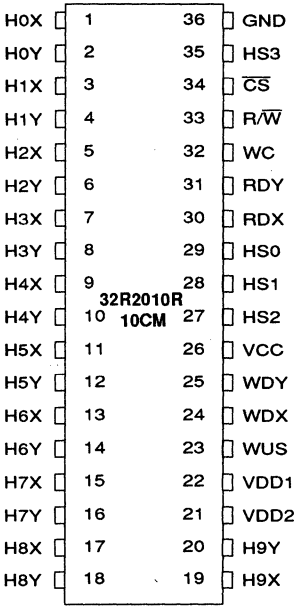
## FEATURES

- **High performance**
  - **Read Mode Gain = 150 Typ V/V**
  - **Input Noise = 0.58 nV/√Hz typ.**
  - **Input Capacitance = 15 pF typ.**
  - **Write Current Range = 10 mA to 25 mA**
  - **Write Current Rise Time = 4 ns**
  - **Head Voltage Swing = 7 Vpp min**
- **Write unsafe detection**
- **Differential, ECL-like write data input**
- **Open collector read data output**
- **Switch from 300Ω damping resistor to 1 kΩ read input resistance**
- **Power supply fault protection**
- **+5V, +12V power supplies ±10%**

## BLOCK DIAGRAM




## PIN DIAGRAM




36-Lead SOM

CAUTION: Use handling procedures necessary for a static sensitive component.

# SSI 32R2010R
# 10-Channel Thin Film Read/Write Device

## FUNCTIONAL DESCRIPTION

The SSI 32R2010R addresses up to 10 channels with logic control inputs which are TTL compatible. Head selection is accomplished as shown in Table 1. Mode selection is accomplished as shown in Table 2. The mode select inputs have internal pull up circuits so that if an input is open it will rise to the upper logic level and force the device into a non-writing condition.

### WRITE MODE

In Write Mode (R/$\overline{W}$ and $\overline{CS}$ low) the circuit functions as a current switch. The Head Select Inputs HS0, HS1, HS2 and HS3 determine the selected head. The write data inputs (WDX, WDY) determine the polarity of the head current. When WDX is high and WDY is low, write current is in the X direction. HNX is sinking current.

The write current magnitude is adjusted by an external resistor, Rwc, from WC to GND, and is given by:

$$Iw = Vwc/Rwc$$

Note that actual head current, Ihd, is:

$$Ihd = Iw/(1+\frac{Rh}{Rd}) + Ioffset$$

where Rh is head resistance, Rd is write damping resistance and Ioffset is a constant DC offset current.

### WRITE MODE FAULT DETECT CIRCUIT

Several circuits are dedicated to detecting fault conditions associated with the write mode. A logical high (off) level will be present at the Write Unsafe (WUS) terminal if any of the following write fault conditions are present:

- Open head circuit (Iw ≥ 20 mA)
- Head shorted to ground
- Write current transition frequency too low
- Write mode not logically selected

A head shorted to ground condition results in a pulsating WUS signal.

After the fault condition is removed, two transitions of the write data input lines are required to clear WUS. The Write Unsafe output is open-collector and is usually terminated by an external resistor connected to VCC.

Additionally, power voltage monitoring circuits are used to detect VCC and VDD1 voltage levels. If either is too low to permit valid data recording, write current is inhibited.

### READ MODE

In Read Mode, (R/$\overline{W}$ high and $\overline{CS}$ low), the circuit functions as a low noise differential amplifier. The read amplifier input terminals are determined by the Head Select inputs. The read amplifier outputs (RDX, RDY) are open collector, requiring external load resistors connected to VCC. The amplifier gain polarity is non-inverting between HnX, HnY inputs and RDX, RDY outputs.

The switch from write to read modes also changes the resistance across HnX and HnY from its write damping value of 300Ω to its read mode input value of 1 kΩ.

### IDLE MODE

Taking $\overline{CS}$ high selects the idle mode which switches the RDX and RDY outputs into a high impedance state and deactivates the internal write current source. This facilitates multi device installations by allowing the read outputs to be wired OR'ed and the write current programming resistor to be common to all devices.

**TABLE 1: Head Select**

| Head Selected | HS3 | HS2 | HS1 | HS0 |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 2 | 0 | 0 | 1 | 0 |
| 3 | 0 | 0 | 1 | 1 |
| 4 | 0 | 1 | 0 | 0 |
| 5 | 0 | 1 | 0 | 1 |
| 6 | 0 | 1 | 1 | 0 |
| 7 | 0 | 1 | 1 | 1 |
| 8 | 1 | 0 | 0 | 0 |
| 9 | 1 | 0 | 0 | 1 |

**TABLE 2: Mode Select**

| $\overline{CS}$ | R/$\overline{W}$ | Mode |
|---|---|---|
| 0 | 0 | Write |
| 0 | 1 | Read |
| 1 | 0 | Idle |
| 1 | 1 | Idle |

## PIN DESCRIPTION

### CONTROL INPUT PINS

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| $\overline{CS}$ | I | Chip Select Input. A logical low level enables the circuit for a read or write operation. Has internal pull up. |
| R/$\overline{W}$ | I | Read/write select. A logical low level enables the write mode (when $\overline{CS}$ is low). Has internal pull up. |
| HS0, HS1, HS2, HS3 | I | Head select inputs. Logical combinations select one of sixteen heads. See Table 1. Has internal pull down resistors. |
| **HEAD TERMINAL PINS** | | |
| H0X-H9X, H0Y-H9Y | I/O | X, Y Head connections: Current in the X-direction flows into the X-port. |
| **DATA INPUT/OUTPUT PINS** | | |
| WDX, WDY | I/O | Differential write data input. |
| RDX, RDY | I/O | Differential Read Data output. These open collector outputs are normally terminated in 100Ω resistors to VCC. |
| **EXTERNAL COMPONENT CONNECTION PINS** | | |
| WC | I/O | Resistor connected to GND to provide desired value of write current. |
| **CIRCUIT MONITOR PINS** | | |
| WUS | O | Write Unsafe is an open-collector output with the off-state indicating that conditions are not proper for a write operation. |
| **POWER, GROUND PINS** | | |
| VCC | I | +5V Logic circuit supply. |
| VDD1 | I | +12V power supply. |
| VDD2 | I | Positive power supply for write current drivers. |
| GND | I | Power supply common. |

## ELECTRICAL SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may permanently damage the device.

| PARAMETER | RATING | UNIT |
|---|---|---|
| Positive Supply Voltage, VCC | 6 | VDC |
| Supply Voltage, VDD1, 2 | 13.5 | VDC |
| Operating Junction Temperature | +130 | °C |
| Storage Temperature | -65 to +130 | °C |
| Package Temperature (20 sec. reflow) | 215 | °C |
| **Input Voltages** | | |
| HS0, HS1, HS2, HS3, $\overline{CS}$, R/$\overline{W}$ | -0.2 to VCC + 0.2 | VDC |
| **Outputs** | | |
| Read Data (RDX, RDY) | VCC -2.5 to VCC + 0.3 | VDC |
| Write Unsafe (WUS) | -0.2V to VCC + 0.2V | VDC |
| Current Reference (WC) | -80 mA to 1.0 mA | VDC |
| Head Outputs (Write Mode) | -80 mA to 1.0 mA | mA |

### POWER SUPPLY

Unless otherwise specified, 4.5V ≤ VCC ≤ 5.5V, 10.8V ≤ VDD1, 2 ≤ 13.2V, 0°C ≤ T (ambient) ≤ 70°C.

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Power Dissipation (Does not include power dissipation through RDX, RDY load resistors) | Idle mode | | 195 | 295 | mW |
| | Read mode | | 440 | 650 | mW |
| | Write mode | | 350 + 10 Iw | 530 + 11.2 Iw | mW |
| Positive Supply Current (ICC) (Includes RDX, RDY currents) | Idle Mode | | 13 | 20 | mA |
| | Read Mode | | 27 | 30 | mA |
| | Write Mode | | 22 | 26 | mA |
| Positive Supply Current (IDD1) | Idle Mode | | 10 | 12 | mA |
| | Read Mode | | 32 | 38 | mA |
| | Write Mode | | 23 | 28 | mA |
| Positive Supply Current (IDD2) | Idle Mode | | 0.5 | 2 | mA |
| | Read Mode | | 1 | 1.5 | mA |
| | Write Mode | | 1 + Iw | 2 + Iw | mA |

## DC CHARACTERISTICS

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| High-level Input Voltage VIH ($\overline{CS}$, R/$\overline{W}$, HS0, HS1, HS2, HS3) | | 2.0 | | - | V |
| Low-level Input Voltage VIL ($\overline{CS}$, R/$\overline{W}$, HS0, HS1, HS2, HS3) | | | | 0.8 | V |
| High-level Input Current IIH ($\overline{CS}$, R/$\overline{W}$, HS0, HS1, HS2, HS3) | VIH = 2.7V | | | 100 | µA |
| Low-level Input Current IIL ($\overline{CS}$, R/$\overline{W}$, HS0, HS1, HS2, HS3) | VIL = 0.4V | | | -400 | µA |
| High-level Output Voltage VIH (WDX, WDY) | | Vcc - 1.0 | | Vcc - 0.72 | V |
| Low-level Output Voltage VIL (WDX, WDY) | | Vcc - 1.87 | | Vcc - 1.625 | V |
| WUS, Low Level Voltage | ILUS = 4 mA (denotes safe condition) | | | 0.5 | V |
| WUS, High Level Current | VHUS = 5.0V (denotes unsafe condition) | | | 100 | µA |

**WRITE MODE**

Test Conditions (Unless otherwise specified). VCC = 4.5 to 5.5V, Ta = 0 to +70°C, VDD = 10.8 to 13.2V, Lh = 470 nH, Rh = 25Ω, WD Tr, Tf < 2 ns, Iw = 20 mA.

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Current Range, Iw | | 10 | | 25 | mA |
| Write Current Voltage, Vwc | | 1.95 | 2.05 | 2.15 | V |
| Differential Head voltage Swing | | 7.0 | 7.6 | | Vpp |
| Ioffset | | | 0.5 | | mA |
| Unselected Head Transient Current | Non adjacent heads tested to minimize external coupling effects | | | 1 | mA(pk) |
| Head Damping Resistance | | 240 | 300 | 360 | Ω |
| Differential Output Capacitance | | | | 20 | pF |

## FAULT DETECTION CHARACTERISTICS

Test conditions same as Write Mode above (unless otherwise specified.)

| CHARACTERISTIC | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| VCC Value for Write Current Turn off | Ih < 1 mA | 3.7 | 4.0 | 4.3 | V |
| VDD Value for Write Current Turn off | Ih < 1 mA | 9.5 | 10.0 | 10.5 | V |
| WDX, WDY Transition Frequency | WUS = Low (Guaranteed safe) | 1.0 | | | MHz |

### READ MODE

Tests performed with 100Ω load resistors from RDX and RDY to VCC. Test conditions same as Write mode (unless otherwise specified.)

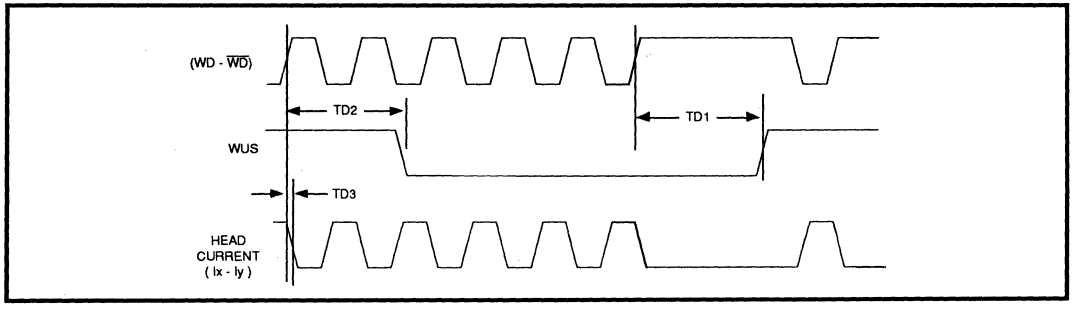
| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Differential Voltage Gain | Vin = 1 mVpp, $f$ = 300 kHz | 120 | 150 | 180 | V/V |
| Voltage Bandwidth (-3dB) | Zs < 5Ω, Vin = 1 mVpp | 75 | 100 | | MHz |
| (-1dB) | Zs < 5Ω, Vin = 1 mVpp | 20 | 35 | | MHz |
| Input Noise Voltage | Zs = 0Ω , Vin = 0V, Power Bandwidth = 20 MHz | | 0.58 | 0.75 | $nV\sqrt{Hz}$ |
| Differential Input Capacitance | Vin = 0V, $f$ = 5 MHz | | 15 | 20 | pF |
| Differential Input Resistance | Vin = 0V, $f$ = 5 MHz | 400 | | 1500 | Ω |
| Dynamic Range @ 5 MHz | Input voltage where AC gain falls to 90% of the gain | 4 | | | mVpp |
| Common Mode Rejection Ratio | Vin = 100 mVpp, 0V DC $f$ = 5 MHz | 60 | 90 | | dB |
| Power Supply Rejection Ratio | VCC or VDD = 100 mVpp $f$ = 5 MHz | 55 | 75 | | dB |
| Channel Separation | Unselected channels are driven with Vin = 20 mVpp @ 5MHz | 60 | 90 | | dB |
| Output Offset Voltage | Rh = 0, Lh = 0 | -250 | | 250 | mV |
| Output Leakage Current | Idle Mode | | | 20 | µA |
| Output Common Mode Voltage | Rh = 0, Lh = 0 | VCC - 0.9 | VCC - 0.5 | VCC - 0.3 | V |
| Output Voltage Compliance | Adjust RDX, Y load voltage source for <5% THD of either output. | VCC - 1.6 | | VCC | V |

**SWITCHING CHARACTERISTICS**

Test conditions same as Write Mode plus RDX, Y connected VCC through 100Ω resistors, WUS with 1kΩ to VCC.

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Idle to Read/Write Transition Time | Delay to 10 or 90% of Read Output or Write Current | | 75 | 150 | µs |
| Read/Write to Idle Transition Time | | | 85 | 150 | ns |
| Read to Write Transition Time | VLCS = 0.8V, Delay to 90% of Iw | | 85 | 150 | ns |
| Write to Read Transition Time | VLCS = 0.8V, Delay to 90% of 10 MHz Read Signal, 100 mV envelope | | 60 | 150 | ns |
| Head Select Switching Delay | Read or Write Mode | | | 500 | ns |
| Head Current Rise and Fall Times 10% to 90% | Iw = 25 mA, Lh = 0 nH Rh = 0Ω | | 2.5 | 4.0 | ns |
| | Iw = 15 mA, Lh = 1 µH Rh = 45Ω | | 6 | | ns |
| Head Current Rise and Fall Difference | | | | 0.5 | ns |
| Head Current Switching Delay Difference (Asymmetry) | WDX, WDY transitions 2 ns, switching time asymmetry 0.2 ns | | | 0.5 | ns |
| Head Current Propogation Delay (TD3) | 50% WD to 50% Iw | | 8 | 15 | ns |
| Unsafe to Safe Delay After Write Data Begins (WUS) (TD2) | $f$(data) = 5 MHz Write Mode (After 2 transitions of WD) | | | 200 | ns |
| Unsafe to Safe Delay After Write Mode Selected (WUS) | | | | 0.5 +Tw* | µs |
| Safe to Unsafe Delay (WUS) (TD1) | After Write Mode fault condition occurs | | | 1.5 | µs |
| Safe to Unsafe Delay (WUS) | After exiting Write Mode | | | 0.5 | µs |

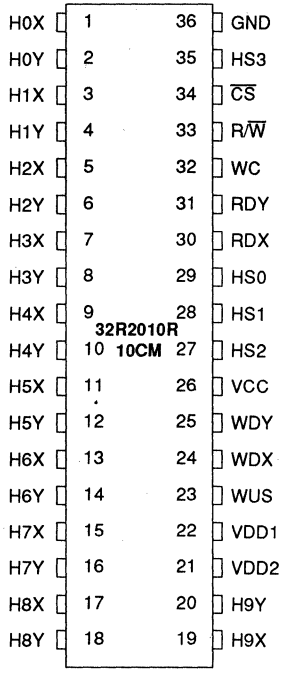
*Tw is the period of the write data input.



# SSI 32R2010R
# 10-Channel Thin Film Read/Write Device

## PACKAGE PIN DESIGNATIONS

(Top View)




**36-Lead SOM**

## THERMAL CHARACTERISTICS: θja

| | |
|---|---|
| **36-Lead SOM** | **75°C/W** |

## ORDERING INFORMATION

| PART DESCRIPTION | ORDER NO. | PKG. MARK |
|---|---|---|
| SSI 32R2010R<br>36-Lead SOM | 32R2010R-CM | 32R2010R-10CM |

**Preliminary Data:** Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.



Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680, (714) 573-6000, FAX: (714) 573-6914

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A TDK Group Company

# SSI 32R2015R
## 16-Channel Thin Film Read/Write Device

**Advance Information**

January 1993

## DESCRIPTION

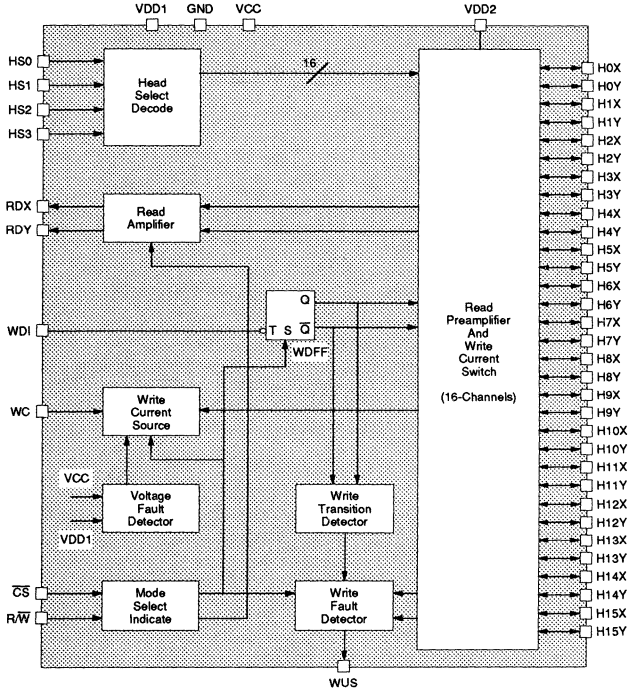
The SSI 32R2015R is an integrated read/write circuit designed for use with two terminal heads in disk drive systems. The device contains sixteen channels of read amplifiers and write drivers and also has an internal write current source. An internal 330Ω damping resistor is supplied in Write mode, which is switched to 1 kΩ in Read mode.

The circuit operates on +5V and +12V power supplies and is available in a 52-pin package.

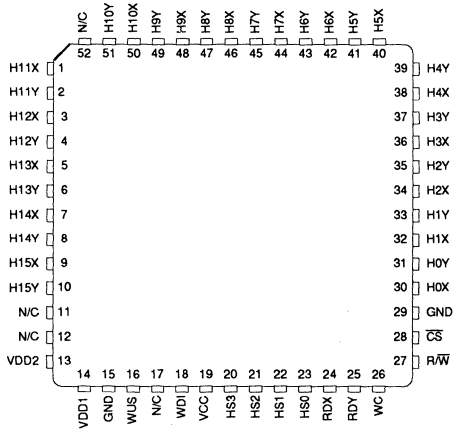
## FEATURES

- **High performance**
  - **Read Mode Gain = 150 Typ V/V**
  - **Input Noise = 0.58 nV/√Hz typ.**
  - **Input Capacitance = 15 pF typ.**
  - **Write Current Range = 10 mA to 25 mA**
  - **Write Current Rise Time = 4 ns**
  - **Head Voltage Swing = 7 Vpp min**
- **Write unsafe detection**
- **TTL write data input**
- **Open collector read data output**
- **Switch from 330Ω damping resistor to 1 kΩ read input resistance**
- **Power supply fault protection**
- **+5V, +12V power supplies ±10%**

## BLOCK DIAGRAM




## PIN DIAGRAM




**52-Pin Plastic QFP**

CAUTION: Use handling procedures necessary for a static sensitive component.

## FUNCTIONAL DESCRIPTION

The SSI 32R2015R addresses up to 16 channels with logic control inputs which are TTL compatible. Head selection is accomplished as shown in Table 1. Mode selection is accomplished as shown in Table 2. The mode select inputs have internal pull up circuits so that if an input is open it will rise to the upper logic level and force the device into a non-writing condition.

### WRITE MODE

In Write Mode (R/$\overline{W}$ and $\overline{CS}$ low) the circuit functions as a current switch. The Head Select Inputs HS0, HS1, HS2 and HS3 determine the selected head. Write current is toggled between the X and Y direction of the selected head on each high to low transition on pin WDI, Write Data Input.

A preceding read operation initializes the Write Data Flip-Flop (WDFF) to pass data in the X-direction of the head. The write current magnitude is adjusted by an external resistor, Rwc, from WC to GND, and is given by:

$$Iw = Vwc/Rwc$$

Note that actual head current, Ihd, is:

$$Ihd = Iw/(1+\frac{Rh}{Rd}) + Ioffset$$

where Rh is head resistance, Rd is write damping resistance and Ioffset is a constant DC offset current.

### WRITE MODE FAULT DETECT CIRCUIT

Several circuits are dedicated to detecting fault conditions associated with the Write mode. A logical high (off) level will be present at the Write Unsafe (WUS) terminal if any of the following write fault conditions are present:

- Open head circuit
- Head shorted to ground
- Write current transition frequency too low
- Write mode not logically selected

A head shorted to ground condition results in a pulsating WUS signal.

After the fault condition is removed, two negative transitions of WDI are required to clear WUS.

The Write Unsafe output is open-collector and is usually terminated by an external resistor connected to VCC.

Additionally, power voltage monitoring circuits are used to detect VCC and VDD1 voltage levels. If either is too low to permit valid data recording, write current is inhibited.

### READ MODE

In Read Mode, (R/$\overline{W}$ high and $\overline{CS}$ low), the circuit functions as a low noise differential amplifier. The read amplifier input terminals are determined by the Head Select inputs. The read amplifier outputs (RDX, RDY) are open collector, requiring external load resistors connected to VCC. The amplifier gain polarity is non-inverting between HnX, HnY inputs and RDX, RDY outputs.

The switch from Write to Read modes also changes the resistance across HnX and HnY from its write damping value of 300Ω to its Read mode input value of 1 kΩ.

### IDLE MODE

Taking $\overline{CS}$ high selects the Idle mode which switches the RDX and RDY outputs into a high impedance state and deactivates the internal write current source. This facilitates multi device installations by allowing the read outputs to be wired OR'ed and the write current programming resistor to be common to all devices.

**TABLE 1: Head Select**

| Head Selected | HS3 | HS2 | HS1 | HS0 |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 |
| 2 | 0 | 0 | 1 | 0 |
| 3 | 0 | 0 | 1 | 1 |
| 4 | 0 | 1 | 0 | 0 |
| 5 | 0 | 1 | 0 | 1 |
| 6 | 0 | 1 | 1 | 0 |
| 7 | 0 | 1 | 1 | 1 |
| 8 | 1 | 0 | 0 | 0 |
| 9 | 1 | 0 | 0 | 1 |
| 10 | 1 | 0 | 1 | 0 |
| 11 | 1 | 0 | 1 | 1 |
| 12 | 1 | 1 | 0 | 0 |
| 13 | 1 | 1 | 0 | 1 |
| 14 | 1 | 1 | 1 | 0 |
| 15 | 1 | 1 | 1 | 1 |

**TABLE 2: Mode Select**

| $\overline{CS}$ | R/$\overline{W}$ | Mode |
|---|---|---|
| 0 | 0 | Write |
| 0 | 1 | Read |
| 1 | 0 | Idle |
| 1 | 1 | Idle |

## PIN DESCRIPTION

### CONTROL INPUT PINS

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| $\overline{CS}$ | I | Chip Select Input. A logical low level enables the circuit for a read or write operation. Has internal pull up. |
| R/$\overline{W}$ | I | Read/write select. A logical low level enables the Write mode (when $\overline{CS}$ is low). Has internal pull up. |
| HS0, HS1, HS2, HS3 | I | Head select inputs. Logical combinations select one of ten heads. See Table 1. Has internal pull down resistors. |
| **HEAD TERMINAL PINS** | | |
| H0X-H15X, H0Y-H15Y | I/O | X, Y Head connections: Current in the X-direction flows into the X-port. |
| **DATA INPUT/OUTPUT PINS** | | |
| WDI | I/O | TTL Write Data Input: a negative transition toggles the direction of the head current. |
| RDX, RDY | I/O | Differential Read Data output. These open collector outputs are normally terminated in 100Ω resistors to VCC. |
| **EXTERNAL COMPONENT CONNECTION PINS** | | |
| WC | I/O | Resistor connected to GND to provide desired value of write current. |
| **CIRCUIT MONITOR PINS** | | |
| WUS | O | Write Unsafe is an open-collector output with the off-state indicating that conditions are not proper for a write operation. |
| **POWER, GROUND PINS** | | |
| VCC | I | +5V Logic circuit supply. |
| VDD1 | I | +12V power supply. |
| VDD2 | I | Positive power supply for write current drivers. |
| GND | I | Power supply common. |

## ELECTRICAL SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may permanently damage the device.

| PARAMETER | RATING | UNIT |
|---|---|---|
| Positive Supply Voltage, VCC | 6 | VDC |
| Supply Voltage, VDD1, 2 | 13.5 | VDC |
| Operating Junction Temperature | 130 | °C |
| Storage Temperature | -65 to +130 | °C |
| Package Temperature (20 sec. reflow) | 215 | °C |
| **Input Voltages** | | |
| HS0, HS1, HS2, HS3, $\overline{CS}$, R/$\overline{W}$, WDI | -0.2 to VCC + 0.2 | VDC |
| **Outputs** | | |
| Read Data ($\overline{RDX}$, RDY) | VCC -2.5 to VCC + 0.3 | VDC |
| Write Unsafe (WUS) | -0.2V to VCC + 0.2V | VDC |
| Current Reference (WC) | -80 mA to 1.0 mA | VDC |
| Head Outputs (Write Mode) | -80 mA to 1.0 mA | mA |

### POWER SUPPLY

Unless otherwise specified, 4.65V ≤ VCC ≤ 5.35V, 10.8V ≤ VDD1, 2 ≤ 13.2V, 0°C ≤ T (ambient) ≤ 70°C.

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Power Dissipation (Does not include power dissipation through RDX, RDY load resistors) | Idle mode | | 185 | 300 | mW |
| | Read mode | | 440 | 610 | mW |
| | Write mode | | 350 + 10 Iw | 530 + 11.2 Iw | mW |
| Positive Supply Current (ICC) (Includes RDX, RDY currents) | Idle Mode | | 13 | 20 | mA |
| | Read Mode | | 27 | 35 | mA |
| | Write Mode | | 18 | 26 | mA |
| Positive Supply Current (IDD1) | Idle Mode | | 9 | 12 | mA |
| | Read Mode | | 29 | 33 | mA |
| | Write Mode | | 20 | 33 | mA |
| Positive Supply Current (IDD2) | Idle Mode | | 1 | 2 | mA |
| | Read Mode | | 3 | 5 | mA |
| | Write Mode | | 2 + Iw | 3 + Iw | mA |

## DC CHARACTERISTICS

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| High-level Input Voltage VIH ($\overline{CS}$, R/$\overline{W}$, HS0, HS1, HS2, HS3, WDI) | | 2.0 | | - | V |
| Low-level Input Voltage VIL ($\overline{CS}$, R/$\overline{W}$, HS0, HS1, HS2, HS3, WDI) | | | | 0.8 | V |
| High-level Input Current IIH ($\overline{CS}$, R/$\overline{W}$, HS0, HS1, HS2, HS3, WDI) | VIH = 2.7V | | | 100 | µA |
| Low-level Input Current IIL ($\overline{CS}$, R/$\overline{W}$, HS0, HS1, HS2, HS3, WDI) | VIL = 0.4V | | | -400 | µA |
| WUS, Low Level Voltage | ILUS = 8 mA (denotes safe condition) | | | 0.5 | V |
| WUS, High Level Current | VHUS = 5.0V (denotes unsafe condition) | | | 100 | µA |

**WRITE MODE**

Test Conditions (Unless otherwise specified). VCC = 4.5 to 5.5V, Ta = 0 to +70°C, VDD = 10.8 to 13.2V, Lh = 470 nH, Rh = 25Ω, WDI Tr, Tf < 2 ns, Iw = 20 mA.

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Current Range, Iw | | 10 | | 25 | mA |
| Write Current Voltage, Vwc | | 1.95 | 2.05 | 2.15 | V |
| Differential Head voltage Swing | | 7.0 | | | Vpp |
| Ioffset | | | 0.5 | | mA |
| Unselected Head Transient Current | Non-adjacent heads tested to minimize external coupling effects | | | 1 | mA(pk) |
| Head Damping Resistance | | 230 | 330 | 430 | Ω |
| Differential Output Capacitance | | | | 20 | pF |

## FAULT DETECTION CHARACTERISTICS

Test conditions same as Write Mode above (unless otherwise specified).

| CHARACTERISTIC | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| VCC Value for Write Current Turn off | Ih < 1 mA | 3.7 | 4.0 | 4.3 | V |
| VDD Value for Write Current Turn off | Ih < 1 mA | 9.5 | 10.0 | 10.5 | V |
| WDI Transition Frequency | WUS = Low (Guaranteed safe) | 2.0 | | | MHz |

### READ MODE

Tests performed with 100Ω load resistors from RDX and RDY to VCC. Test conditions same as Write mode (unless otherwise specified).

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Differential Voltage Gain | Vin = 1 mVpp, $f$ = 300 kHz | 120 | 150 | 180 | V/V |
| Voltage Bandwidth (-3dB) | Zs < 5Ω, Vin = 1 mVpp | 50 | 84 | | MHz |
| (-1dB) | Zs < 5Ω, Vin = 1 mVpp | 20 | 45 | | MHz |
| Input Noise Voltage | Zs = 0Ω , Vin = 0V, Power Bandwidth = 20 MHz | | 0.58 | 0.7 | $nV\sqrt{Hz}$ |
| Differential Input Capacitance | Vin = 0V, $f$ = 5 MHz | | 15 | 26 | pF |
| Differential Input Resistance | Vin = 0V, $f$ = 5 MHz | 400 | | 1500 | Ω |
| Dynamic Range | Input voltage where AC gain falls to 90% of the gain with 0.5 mVpp input signal | 4 | | | mVpp |
| Common Mode Rejection Ratio | Vin = 100 mVpp, 0V DC $f$ = 5 MHz | 50 | | | dB |
| Power Supply Rejection Ratio | VCC or VDD = 100 mVpp $f$ = 5 MHz | 55 | | | dB |
| Channel Separation | Unselected channels are driven with Vin = 20 mVpp @ 5 MHz | 50 | | | dB |
| Output Offset Voltage | Rh = 0, Lh = 0 | -360 | | 360 | mV |
| Output Leakage Current | Idle Mode | | | 20 | µA |
| Output Common Mode Voltage | | VCC - 0.9 | VCC - 0.5 | VCC - 0.3 | V |
| Output Voltage Compliance | Adjust RDX, Y load voltage source for <5% THD of either output. | VCC - 1.5 | | VCC | V |

**SWITCHING CHARACTERISTICS**

Test conditions same as Write Mode plus RDX, Y connected to VCC through 100Ω resistors, WUS with 1 kΩ to VCC.

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Idle to Read/Write Transition Time | Delay to 10 or 90% of Read Output or Write Current | | | 0.4 | µs |
| Read/Write to Idle Transition Time | | | | 0.4 | µs |
| Read to Write Transition Time | VLCS = 0.8V, Delay to 90% of Iw | | | 0.4 | µs |
| Write to Read Transition Time | VLCS = 0.8V, Delay to 90% of 10 MHz Read Signal, 100 mV envelope | | | 0.6 | µs |
| Head Select Switching Delay | Read or Write Mode | | | 0.5 | µs |
| Head Current Rise and Fall Times 10% to 90% | Iw = 25 mA, LH = 0 nH Rh = 0Ω | | | 4 | ns |
| | Iw = 15 mA, LH = 1 µH Rh = 45Ω | | 6 | | ns |
| Head Current Rise and Fall Difference | | | | 0.5 | ns |
| Head Current Switching Delay (TD3) | 50% WDI to 50% Iw | | | 30 | ns |
| Head Current Switching Jitter (Asymmetry) | WDI transitions 2 ns, switching time symmetry 0.2 ns | | | 0.3 | ns |
| Unsafe to Safe Delay After Write Data Begins (WUS) (TD2) | $f$(data) = 5 MHz | | | 0.20 | µs |
| Unsafe to Safe Delay After Write Mode Selected (WUS) | | | | 0.5 +Tw* | µs |
| Safe to Unsafe Delay (WUS) (TD1) | After Write mode fault condition occurs | | | 1.50 | µs |
| Safe to Unsafe Delay (WUS) | After exiting Write mode | | | 0.5 | µs |

*Tw is the period of the write data input.

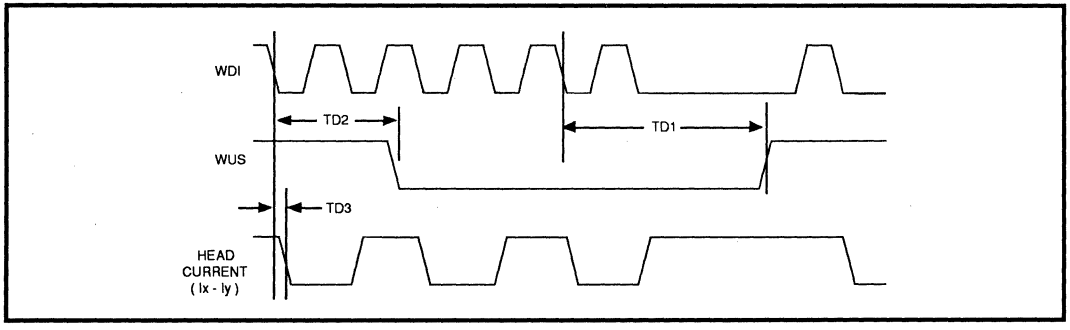
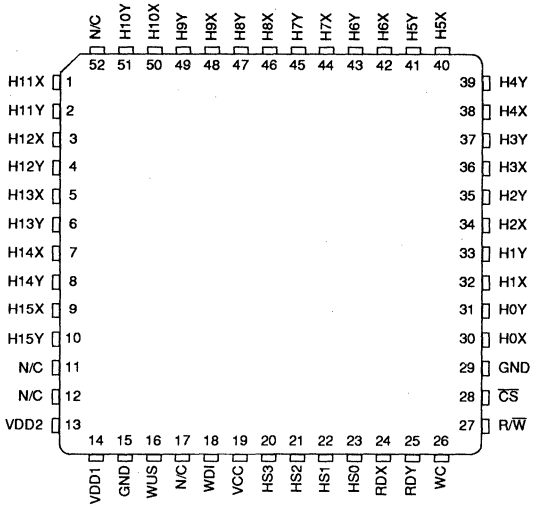



**FIGURE 1: Write Mode Timing Diagram**

# SSI 32R2015R
# 16-Channel Thin Film Read/Write Device

## PACKAGE PIN DESIGNATIONS
(Top View)




**52-Lead Plastic QFP**

### THERMAL CHARACTERISTICS: θja

| | |
|---|---|
| 52-Lead QFP | 50°C/W |

**Advance Information:** Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.



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# SSI 32R2020R/2021R
## 5V, 2, 4, 6, 10-Channel Thin-Film Read/Write Device

January 1993

## DESCRIPTION

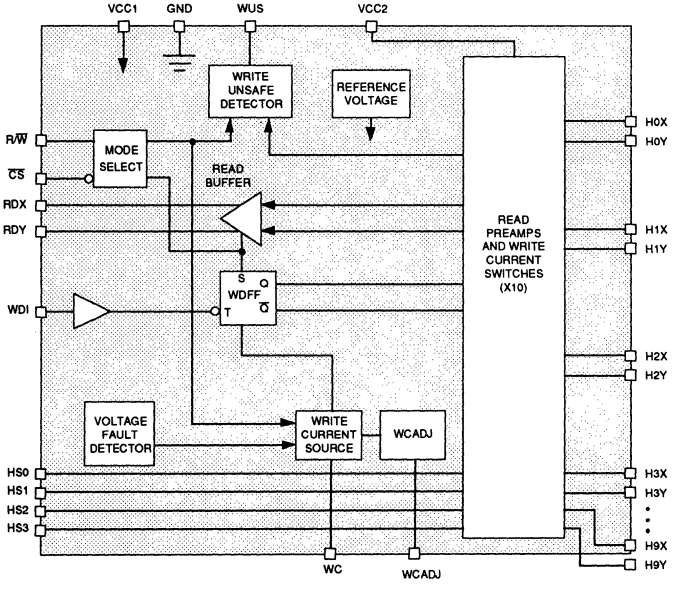
The SSI 32R2020R/2021R are bipolar monolithic integrated circuits designed for use with two-terminal recording heads. They provide a low noise read amplifier, write current control, and data protection circuitry for up to ten channels. The SSI 32R2020R/2021R provide internal 320Ω damping resistors. Damping resistors are switched in during write mode and switched out during read mode. Power supply fault protection is provided by disabling the write current generator during power sequencing. System write to read recovery time is significantly improved by controlling the read channel common mode output voltage shift in the write mode. The 32R2021R option provides the user with a controllable write current adjustment feature.

The SSI 32R2020R/2021R require only +5V power supplies and are available in a variety of packages. They are hardware compatible with the 32R4610A/4611A read/write devices.

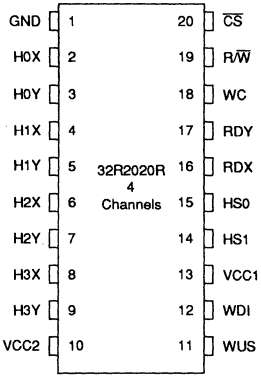
## FEATURES

- **+5V ±10% supply**
- **Low power**
  - **PD = 130 mW read mode (Nom)**
  - **PD = 3.3 mW idle (Nom)**
- **High Performance:**
  - **Read mode gain = 300 V/V**
  - **Input noise = 0.56 nV/√Hz (Nom)**
  - **Input capacitance = 16 pF (Nom)**
  - **Write current range = 5-35 mA**
- **Self switching damping resistance**
- **Designed for two-terminal thin-film or MIG heads with inductance up to 5.0 μH**
- **Pin compatible with the 32R4610AR/4611AR**
- **Write unsafe detection**
- **Power supply fault protection**
- **Head short to ground protection**

## BLOCK DIAGRAM




## PIN DIAGRAM




**20-PIN SOL**

CAUTION: Use handling procedures necessary for a static sensitive component.



WCADJ available on the 32R2021R-4 24-pin option only

# SSI 32R2020R/2021R
# 5V, 2, 4, 6, 10-Channel
# Thin-Film Read/Write Device

## CIRCUIT OPERATION

The SSI 32R2020R/2021R have the ability to address up to 10 two-terminal heads and provide write drive or read amplification. Mode control and head selection are described in Tables 1 and 2. The TTL inputs R/$\overline{W}$ and $\overline{CS}$ have internal pull-up resistors to prevent an accidental write condition. HS0, HS1, HS2 and HS3 have internal pulldown resistors. Internal clamp circuitry will protect the IC from a head short to ground condition in any mode.

**TABLE 1: Mode Select**

| $\overline{CS}$ | R/$\overline{W}$ | Mode |
|---|---|---|
| 0 | 0 | Write |
| 0 | 1 | Read |
| 1 | 0 | Idle |
| 1 | 1 | Idle |

**TABLE 2: Head Select**

| HS3 | HS2 | HS1 | HS0 | Head |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 2 |
| 0 | 0 | 1 | 1 | 3 |
| 0 | 1 | 0 | 0 | 4 |
| 0 | 1 | 0 | 1 | 5 |
| 0 | 1 | 1 | 0 | 6 |
| 0 | 1 | 1 | 1 | 7 |
| 1 | 0 | 0 | 0 | 8 |
| 1 | 0 | 0 | 1 | 9 |

## PIN DESCRIPTION

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| HS0, HS1, † HS2, HS3 | I | Head Select: selects one of ten heads |
| $\overline{CS}$ | I | Chip Select: a high inhibits the chip |
| R/$\overline{W}$ † | I | Read/Write : a high selects Read mode |
| WUS † | O | Write Unsafe: a high indicates an unsafe writing condition |
| WDI † | I | Write Data In: changes the direction of the current in the recording head |
| H0X - H9X; H0Y - H9Y | I/O | X, Y Head Connections |
| RDX, RDY † | O | X, Y Read Data: differential read data output |
| WC † | | Write Current: used to set the magnitude of the write current |
| WCADJ* † | | Write Current Adjust: Used to fine tune the write current |
| VCC1 | I | +5V Supply |
| VCC2 | I | +5V Supply for Write current drivers |
| GND | I | Ground |

* Available on 32R2021R-4 24-pin option only

† When more than one R/W device is used, signals can be wire OR'ed

### WRITE MODE

Taking both $\overline{CS}$ and R/$\overline{W}$ low selects Write mode which configures the SSI 32R2020R/2021R as a current switch and activates the Write Unsafe (WUS) detector circuitry. Head current is toggled between the X and Y side of the selected head on each high to low transition of the Write Data Input (WDI). Changing from Read or Idle mode to Write mode initializes the Write Data Flip-Flop to pass write current into the "X" pin. In this case, the Y side of the head will be higher potential than the X side. The magnitude of the write current (0-pk) is given by:

$$Iw = \frac{K \cdot Vwc}{Rwc}$$

Rwc is connected from pin WC to GND. Note the actual head current Ix, y is given by:

$$Ix, y = \frac{Iw}{1 + Rh/Rd}$$

Where:

Rh = Head resistance plus external wire resistance

Rd = Damping resistance

In write mode a 320Ω damping resistor is switched in across the Hx, Hy ports.

The 32R2021R adds a feature which allows the user to adjust the Iw current by a finite amount. The WCADJ pin is used to adjust write current for write operations on different zones of the disk. It is used by switching a separate write current adjust resistor in and out on the WCADJ pin or by connecting a DAC to that pin to sink a controllable amount of current. The WCADJ pin is nominally biased to VCC/2. Sinking current from this pin to ground will divert a proportional amount of current from the actual head current while maintaining a constant current through the WC resistor and VCC. Allowing WCADJ to float or pulling it high will cut off the circuit and it will have no effect. A TTL gate can be used as a switch with a small degradation in accuracy. The amount of write current decrease is shown below:

Iw head (decrease) (mA) = (29 • $V_{WCADJ}/R_{WCADJ}$)

where:

$V_{WCADJ}$ = VCC/2 (volts)

$R_{WCADJ}$ = write current adjust setting resistor (kΩ)

Example: For a 7.25 mA head current decrease, $R_{WCADJ}$ = (27 • 2.5) / 7.25 = 10 kΩ

### POWER SUPPLY FAULT PROTECTION

A voltage fault detection circuit improves data security by disabling the write current generator during a voltage fault or power startup regardless of mode. Note that WUS does not necessarily turn on to flag a power supply fault condition.

### HEAD SHORT TO GROUND PROTECTION

The 2020R/2021R provides a head short to ground protection circuit in any mode. In Idle or Read Mode, current out of the head port will not exceed 20 mA if any head is shorted to ground. In Write mode, if any head is shorted to ground (regardless if it is selected or not) the write current generator will turn off, the WUS flag will go high, and current will be limited to less than 1 mA out of the head port.

### WRITE UNSAFE

Any of the following conditions will be indicated as a high level on the Write Unsafe, WUS, open collector output.

- WDI frequency too low
- Device in Read mode
- Chip disabled
- No head current
- Head opened
- Head short to ground

To insure proper WUS operation, the product of write current, WDI frequency, and head inductance should be less than 500 mA•µH•MHz. To insure no false WUS trigger, the product of head current and head resistance (Ix,y•Rh) should be between 100 mV and 1.7V.

**WDI frequency too low** is detected if the WDI frequency falls below 500 kHz (typ). Consult the WUS Safe to Unsafe timing for range of frequency detection.

**Device in Read mode** and **Chip disabled** will flag WUS if R/$\overline{W}$ is high or $\overline{CS}$ is high.

**No head current** will flag WUS if Rwc = ∞ and the selected head is present.

**Head opened** will flag WUS if Rh = ∞ and under the condition that VCC/Iw < 0.25 V/mA.

**Head short to ground** is described in the preceding paragraph.

Upon entering write mode, WUS is valid after two high to low transitions of WDI following the required Read-Write transition time (0.6 µs max).

## CIRCUIT OPERATION (continued)

### READ MODE

The Read mode configures the SSI 32R2020R/2021R as a low noise differential amplifier and deactivates the write current generator. The damping resistor is switched out of the circuit allowing a high impedance input to the read amplifier. The RDX and RDY output are driven by emitter followers. They should be AC coupled to the load. The (X,Y) inputs are non-inverting to the (X,Y) outputs.

Note that in Idle or Write mode, the read amplifier is deactivated and RDX, RDY outputs become high impedance. This facilitates multiple R/W applications (wired-OR RDX, RDY) and minimizes voltage drifts when switching from Write to Read mode. Note also that the write current source is deactivated for both the Read and Idle mode.

### IDLE MODE

Taking $\overline{CS}$ high selects the idle mode which switches the RDX and RDY outputs into a high impedance state and deactivates the device. Power consumption in this mode is held to a minimum.

## ELECTRICAL SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may permanently damage the device.

| PARAMETER | | RATING |
|---|---|---|
| DC Supply Voltage | VCC1 | -0.3 to +6 VDC |
| | VCC2 | -0.3 to +6 VDC |
| Write Current | Iw | 60 mA |
| Digital Input Voltage | Vin | -0.3 to VCC1 +0.3 VDC |
| Head Port Voltage | VH | -0.3 to VCC2 +0.3 VDC |
| Output Current: RDX, RDY | I0 | -6 mA |
| $\overline{WUS}$ | | +8 mA |
| Storage Temperature | Tstg | -65 to +150 °C |

### RECOMMENDED OPERATING CONDITIONS

| | | | |
|---|---|---|---|
| DC Supply Voltage | VCC1 = VCC2 | 5 ±10% | VDC |
| Operating Junction Temperature | Tj | +25 to +135 | °C |
| Recommended Head Load Range | Lh | 0.3 - 5.0 | µH |

### DC CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified.

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| VCC1 Supply Current | Read Mode | | 18 | 25 | mA |
| | Write Mode | | 22 | 29 | mA |
| | Idle Mode | | 0.6 | 0.95 | mA |
| VCC2 Supply Current | Read Mode | | 8 | 11 | mA |
| | Write Mode | | 4 + Iw | 7 + Iw | mA |
| | Idle Mode | | 0 | 0.2 | mA |

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Power Dissipation | Read Mode | | 130 | 200 | mW |
| | Write Mode | | 130 + 4 Iw | 200 + 4.3 Iw | mW |
| | Idle Mode | | 3.3 | 6.5 | mW |
| VCC1 Fault Voltage | Iw < 0.2 mA | 3.5 | 3.9 | 4.2 | VDC |

**DIGITAL INPUTS**

| | | | | | |
|---|---|---|---|---|---|
| Input Low voltage (Vil) | | | | 0.8 | VDC |
| Input High Voltage (Vil) | | 2.0 | | | VDC |
| Input Low Current | Vil = 0.8V | -0.4 | | | mA |
| Input High Current | Vih = 2.0V | | | 100 | µA |
| WUS Output Low Voltage (Vol) | Iol = 2 mA max | | | 0.5 | VDC |

**WRITE CHARACTERISTICS**

Recommended operating conditions apply unless otherwise specified.

| | | | | | |
|---|---|---|---|---|---|
| Write Current Constant "K" | | | 0.99 | | |
| Write Current Voltage (Vwc) | | 1.15 | 1.25 | 1.35 | V |
| WCADJ Voltage<br>SSI 32R2021R | $I_{WCADJ}$ = 0 to .5 mA | 2.0 | VCC/2 | 3.0 | VDC |
| Ihead(Decrease)/$I_{WCADJ}$<br>SSI 32R2021R | | 23 | 27 | 31 | mA/mA |
| $I_{WCADJ}$ Range<br>SSI 32R2021R | | 0.0 | | 0.5 | mA |
| Differential Head Voltage Swing | | 4.2 | 5.6 | | Vpp |
| | Open Head Iw = 20 mA | 3.4 | 5.0 | | Vpp |
| Unselected Head Current | | | | 1 | mA (pk) |
| Head Differential Damping Resistance (Rd) | | | 320 | | Ω |
| WDI Pulse Width | Vil ≥ 0.2V PWH | 10 | | | ns |
| | PWL | 5 | | | ns |
| Write Current Range (Iw) | | 5 | | 35 | mA |
| Head Differential Load Capacitance | | | | 25 | pF |

**READ CHARACTERISTICS**

Recommended operating conditions apply unless otherwise specified. CL (RDX, RDY) < 20 pF, RL (RDX, RDY) = 1 kΩ.

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Differential Voltage Gain | Vin = 1 mVpp @1 MHz | 250 | 300 | 350 | V/V |
| Voltage BW -1dB | \|Zs\| < 5Ω, Vin = 1 mVpp | 20 | | | MHz |
| -3dB | \|Zs\| < 5Ω, Vin = 1 mVpp | 45 | | | MHz |
| Input Noise Voltage | BW = 15 MHz, Lh = 0, Rh = 0 | | 0.56 | 0.75 | nV/√Hz |
| Differential Input Capacitance | Vin = 1 mVpp, $f$ = 5 MHz | | 16 | 22 | pF |
| Differential Input Resistance | Vin = 1 mVpp, $f$ = 5 MHz | 720 | 1200 | | Ω |
| Dynamic Range | AC input voltage where gain falls to 90% of its small signal gain value, $f$ = 5 MHz | 2 | | | mVpp |
| Common Mode Rejection Ratio | Vin = 0 VDC + 100 mVpp @ 5 MHz | 55 | | | dB |
| Power Supply Rejection Ratio | 100 mVpp @ 5 MHz on VCC | 50 | | | dB |
| Channel Separation | Unselected channels driven with Vin = 0 VDC + 100 mVpp | 55 | | | dB |
| Output Offset Voltage | | | | ±300 | mV |
| Single Ended Output Resistance | $f$ = 5 MHz | | | 50 | Ω |
| Output Current | AC coupled load, RDX to RDY | 0.9 | | | mA |
| RDX, RDY Common Mode Output Voltage | | 0.4 VCC | VCC/2 | 0.6 VCC | VDC |

**SWITCHING CHARACTERISTICS**

Recommended operating conditions apply unless otherwise specified. IW = 20 mA, Lh = 1.0 µH, Rh = 30Ω $f$(Data) = 5 MHz.

| | | | | | | |
|---|---|---|---|---|---|---|
| R/$\overline{W}$ | Read to Write | R/W to 90% of write current | | 0.1 | 0.6 | µs |
| | Write to Read | R/W to 90% of 100 mV Read signal envelope | | 0.1 | 0.6 | µs |
| $\overline{CS}$ | Unselect to Select | $\overline{CS}$ to 90% of write current or to 90% of 100 mV 10 MHz | | 0.2 | 1 | µs |
| | Select to Unselect | $\overline{CS}$ to 10% of write current | | 0.11 | 0.6 | µs |
| HS0,1 to any Head | | To 90% of 100 mV 10 MHz Read signal envelope | | 0.11 | 0.6 | µs |
| WUS: | Safe to Unsafe (TD1) | Write mode, loss of WDI transitions. Defines maximum WDI period for WUS operation | 0.6 | 2.0 | 3.6 | µs |
| | Unsafe to Safe (TD2) | Fault cleared, from first neg WDI transition | | 0.1 | 0.6 | µs |

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Head Current: | | | | | |
| WDI to Ix - Iy (TD3) | from 50% points, Lh = 0, Rh = 0 | | 3 | 10 | ns |
| Asymmetry | WDI has 1 ns rise/fall time, Lh = 0, Rh = 0 | | | 1.0 | ns |
| Rise/fall Time | 10% to 90% points, Lh = 0, Rh = 0 | | 4 | 6 | ns |
| Rise/fall Time | Lh = 1 µH, Rh = 30Ω | | 15 | | ns |

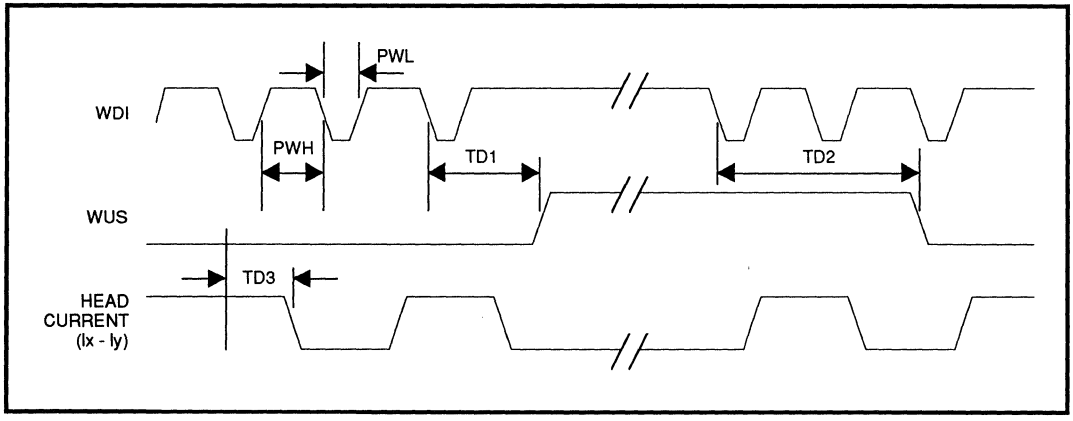
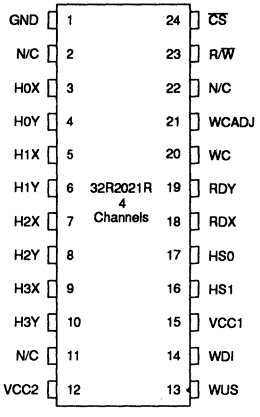


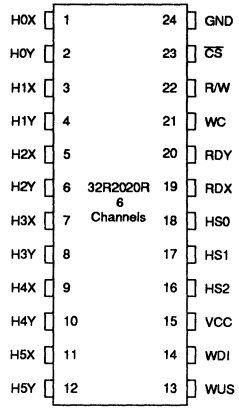

**FIGURE 1: Write Mode Timing Diagram**

# SSI 32R2020R/2021R
# 5V, 2, 4, 6, 10-Channel
# Thin-Film Read/Write Device

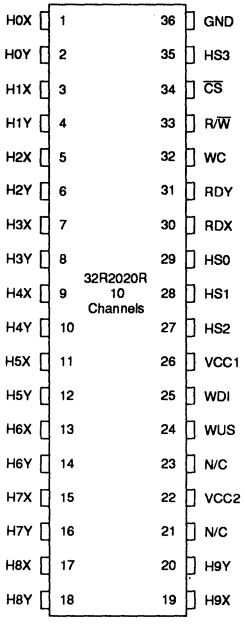
## PACKAGE PIN DESIGNATIONS
(Top View)



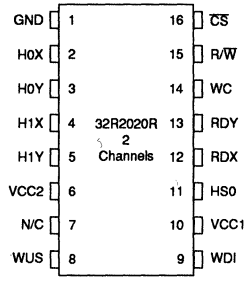

**24-Pin SOL, SOV**



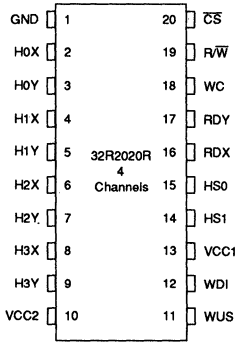

**24-Pin SOV**




**36-Pin SOM**




**16-Pin SOL**




**20-Pin SOL, SOV**



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# SSI 32R2024R
## 5V, 4-Channel Thin-Film Read/Write Device
## Advance Information

January 1993

## DESCRIPTION

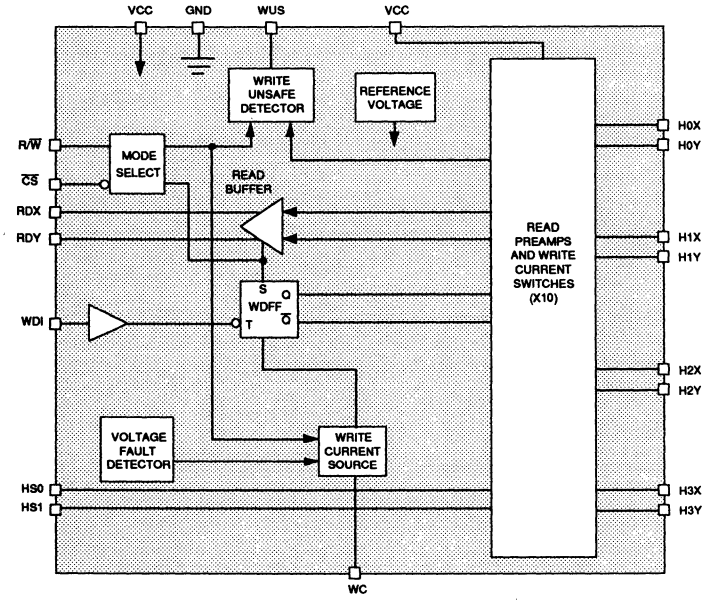
The SSI 32R2024R is a bipolar monolithic integrated circuit designed for use with two-terminal recording heads. It provides a low noise read amplifier, write current control, and data protection circuitry for up to four channels. The SSI 32R2024R provides internal 400Ω damping resistors that are switched in during write mode and switched out during read mode. Power supply fault protection is provided by disabling the write current generator during power sequencing. System write to read recovery time is significantly improved by controlling the read channel common mode output voltage shift in the write mode.

The SSI 32R2024R requires only +5V power supplies and is available in a variety of packages.

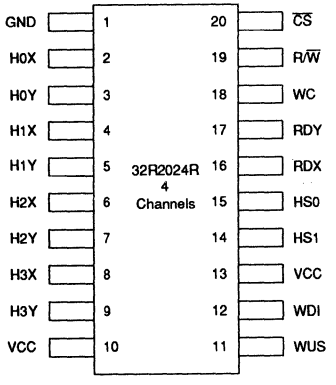
## FEATURES

- +5V ±10% supply
- Low power
  - PD = 160 mW read mode (Nom)
  - PD = 5 mW idle (Max)
- High Performance:
  - Read mode gain = 200 V/V
  - Input noise = 0.56 nV/√Hz (Nom)
  - Input capacitance = 16 pF (Nom)
  - Write current range = 5 - 40 mA
- Self switching damping resistance
- Designed for two-terminal thin-film or MIG heads with inductance up to 5.0 µH
- Write unsafe detection
- Power supply fault protection
- Head short to ground protection

## BLOCK DIAGRAM




## PIN DIAGRAM




20-PIN SOL

CAUTION: Use handling procedures necessary for a static sensitive component.

## CIRCUIT OPERATION

The SSI 32R2024R has the ability to address up to 4 two-terminal heads and provide write drive or read amplification. Mode control and head selection are described in Tables 1 and 2. The TTL inputs R/$\overline{W}$ and $\overline{CS}$ have internal pull-up resistors to prevent an accidental write condition. HS0 and HS1 have internal pulldown resistors. Internal clamp circuitry will protect the IC from a head short to ground condition in any mode.

**TABLE 1: Mode Select**

| $\overline{CS}$ | R/$\overline{W}$ | Mode |
|---|---|---|
| 0 | 0 | Write |
| 0 | 1 | Read |
| 1 | 0 | Idle |
| 1 | 1 | Idle |

**TABLE 2: Head Select**

| HS1 | HS0 | Head |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 2 |
| 1 | 1 | 3 |

## PIN DESCRIPTION

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| HS0, HS1 † | I | Head Select: selects one of four heads |
| $\overline{CS}$ | I | Chip Select: a high inhibits the chip |
| R/$\overline{W}$ † | I | Read/Write : a high selects Read mode |
| WUS † | O | Write Unsafe: a high indicates an unsafe writing condition |
| WDI † | I | Write Data In: changes the direction of the current in the recording head |
| H0X - H3X; H0Y - H3Y | I/O | X, Y Head Connections |
| RDX, RDY † | O | X, Y Read Data: differential read data output |
| WC † | | Write Current: used to set the magnitude of the write current |
| VCC | I | +5V Supply |
| GND | I | Ground |
| † When more than one R/W device is used, signals can be wire OR'ed | | |

### WRITE MODE

Taking both $\overline{CS}$ and R/$\overline{W}$ low selects Write mode which configures the SSI 32R2024R as a current switch and activates the Write Unsafe (WUS) detector circuitry. Head current is toggled between the X and Y side of the selected head on each high to low transition of the Write Data Input (WDI). Changing from Read or Idle mode to Write mode initializes the Write Data Flip-Flop to pass write current into the "X" pin. In this case, the Y side of the head will be higher potential than the X side. The magnitude of the write current (0-pk) is given by:

$$Iw = \frac{A_I \cdot Vwc}{RWC} = \frac{Kw}{RWC}$$

Rwc is connected from pin WC to GND. Note the actual head current Ix, y is given by:

$$Ix, y = \frac{Iw}{1 + Rh/Rd}$$

Where:

Rh = Head resistance plus external wire resistance

Rd = Damping resistance

In write mode a 400Ω damping resistor is across the Hx, Hy ports.

### POWER SUPPLY FAULT PROTECTION

A voltage fault detection circuit improves data security by disabling the write current generator during a voltage fault or power startup regardless of mode. Note that WUS does not necessarily turn on to flag a power supply fault condition.

### HEAD SHORT TO GROUND PROTECTION

The SSI 32R2024R provides a head short to ground protection circuit in any mode. In Idle or Read Mode, current out of the head port will not exceed 20 mA if any head is shorted to ground. In Write mode, if any head is shorted to ground (regardless if it is selected or not) the write current generator will turn off, the WUS flag will go high, and current will be limited to less than 1 mA out of the head port.

### WRITE UNSAFE

Any of the following conditions will be indicated as a high level on the Write Unsafe, WUS, open collector output.

- WDI frequency too low
- Device in Read mode
- Chip disabled
- No head current
- Head opened
- Head short to ground

To insure proper WUS operation, the product of write current, WDI frequency, and head inductance should be less than 500 mA•µH•MHz. To insure no false WUS trigger, the product of head current and head resistance (Ix,y•Rh) should be between 100 mV and 1.7V.

**WDI frequency too low** is detected if the WDI frequency falls below 500 kHz (typ). Consult the WUS Safe to Unsafe timing for range of frequency detection.

**Device in Read mode** and **Chip disabled** will flag WUS if R/$\overline{W}$ is high or $\overline{CS}$ is high.

**No head current** will flag WUS if Rwc = ∞ and the selected head is present.

**Head opened** will flag WUS if Rh = ∞ and under the condition that Iw • Rd > 3.9V.

**Head short to ground** is described in the preceding paragraph.

Upon entering write mode, WUS is valid after two high to low transitions of WDI following the required Read-Write transition time (0.6 µs max).

### READ MODE

The Read mode configures the SSI 32R2024R as a low noise differential amplifier and deactivates the write current generator. The damping resistor is switched out of the circuit allowing a high impedance input to the read amplifier. The RDX and RDY output are driven by emitter followers. They should be AC coupled to the load. The (X,Y) inputs are non-inverting to the (X,Y) outputs.

Note that in Idle or Write mode, the read amplifier is deactivated and RDX, RDY outputs become high impedance. This facilitates multiple R/W applications (wired-OR RDX, RDY) and minimizes voltage drifts when switching from Write to Read mode. Note also that the write current source is deactivated for both the Read and Idle mode.

### IDLE MODE

Taking $\overline{CS}$ high selects the idle mode which switches the RDX and RDY outputs into a high impedance state and deactivates the device. Power consumption in this mode is held to a minimum.

## ELECTRICAL SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may permanently damage the device.

| PARAMETER | | RATING |
|---|---|---|
| DC Supply Voltage | VCC | -0.3 to +6 VDC |
| Write Current | Iw | 60 mA |
| Digital Input Voltage | Vin | -0.3 to VCC +0.3 VDC |
| Head Port Voltage | VH | -0.3 to VCC +0.3 VDC |
| Output Current: RDX, RDY | I0 | -6 mA |
| WUS | | +8 mA |
| Storage Temperature | Tstg | -65 to +150°C |

### RECOMMENDED OPERATING CONDITIONS

| | | |
|---|---|---|
| DC Supply Voltage | | 5 ±10% VDC |
| Operating Junction Temperature | Tj | +25 to +135 °C |
| Recommended Head Load Range | Lh | 0.3 - 5.0 µH |
| Operating Ambient Temperature | Ta | 0 to 70°C |

### DC CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified.

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| VCC | Read Mode | | 32 | 41 | mA |
| | Write Mode | | 25 + Iw | 37 + Iw | mA |
| | Idle Mode | | 0.6 | 0.9 | mA |
| Power Dissipation | Read Mode | | 160 | 225 | mW |
| | Write Mode (Iw = 20 mA) | | 225 | 315 | mW |
| | Idle Mode | | 3 | 5 | mW |
| VCC Fault Voltage | Iw < 0.2 mA | 3.5 | 3.9 | 4.2 | VDC |

**DIGITAL INPUTS**

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Input Low voltage (Vil) | | | | 0.8 | VDC |
| Input High Voltage (Vih) | | 2.0 | | | VDC |
| Input Low Current | Vil = 0.8V | -0.4 | | | mA |
| Input High Current | Vih = 2.0V | | | 100 | µA |
| WUS Output Low Voltage (Vol) | Iol = 2 mA max | | | 0.5 | VDC |

**WRITE CHARACTERISTICS**

Recommended operating conditions apply unless otherwise specified.

| | | | | | | |
|---|---|---|---|---|---|---|
| Iwc to Head Current Gain (Ai) | Iw = Ai • VWC/RWC | | | 20 | | mA/mA |
| Write Current Constant (Kw) | Kw = Ai • VWC | | 47 | 51 | 55 | V |
| Write Current Voltage (Vwc) | | | | 2.55 | | V |
| Differential Head Voltage Swing | Open Head<br>Iw = 20 mA | | 4.2 | 5.6 | | Vpp |
| Unselected Head Current | | | | | 1 | mA (pk) |
| Head Differential Load Capacitance | | | | | 25 | pF |
| Head Differential Damping Resistance (Rd) | | | | 400 | | Ω |
| WDI Pulse Width | Vil ≥ 0.2V | PWH | 10 | | | ns |
| | | PWL | 5 | | | ns |
| Write Current Range (Iw) | | | 5 | | 40 | mA |
| RDX, RDY Common Mode Output Voltage | | | | VCC/2 | | V |

**READ CHARACTERISTICS**

Recommended operating conditions apply unless otherwise specified. CL (RDX, RDY) < 20 pF, RL (RDX, RDY) = 1 kΩ.

| | | | | | | |
|---|---|---|---|---|---|---|
| Differential Voltage Gain | | Vin = 1 mVpp @1 MHz | 166 | 200 | 234 | V/V |
| Voltage BW | -1 dB | \|Zs\| < 5Ω, Vin = 1 mVpp | 20 | | | MHz |
| | -3 dB | \|Zs\| < 5Ω, Vin = 1 mVpp | 45 | | | MHz |
| Input Noise Voltage | | BW = 15 MHz, Lh = 0, Rh = 0 | | 0.56 | 0.75 | nV/√Hz |
| Differential Input Capacitance | | Vin = 1 mVpp, $f$ = 5 MHz | | 16 | 22 | pF |
| Differential Input Resistance | | Vin = 1 mVpp, $f$ = 5 MHz | 720 | 1200 | | Ω |
| Dynamic Range | | AC input voltage where gain falls to 90% of its small signal gain value, $f$ = 5 MHz | 2 | | | mVpp |

**READ CHARACTERISTICS** (continued)

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Common Mode Rejection Ratio | Vin = 0 VDC + 100 mVpp @ 5 MHz | 55 | | | dB |
| Power Supply Rejection Ratio | 100 mVpp @ 5 MHz on VCC | 50 | | | dB |
| Channel Separation | Unselected channels driven with Vin = 0 VDC + 100 mVpp | 55 | | | dB |
| Output Offset Voltage | | | | ±300 | mV |
| Single Ended Output Resistance | $f$ = 5 MHz | | | 50 | Ω |
| Output Current | AC coupled load, RDX to RDY | 0.9 | | | mA |
| RDX, RDY Common Mode Output Voltage | | 0.4 VCC | VCC/2 | 0.6 VCC | VDC |

**SWITCHING CHARACTERISTICS**

Recommended operating conditions apply unless otherwise specified. IW = 20 mA, Lh = 1.0 µH, Rh = 30Ω $f$(Data) = 5 MHz.

| | | | | | | |
|---|---|---|---|---|---|---|
| R/$\overline{W}$ | Read to Write | R/W to 90% of write current | | 0.1 | 0.6 | µs |
| | Write to Read | R/W to 90% of 100 mV Read signal envelope | | 0.1 | 0.6 | µs |
| $\overline{CS}$ | Unselect to Select | $\overline{CS}$ to 90% of write current or to 90% of 100 mV 10 MHz | | 0.2 | 0.6 | µs |
| | Select to Unselect | $\overline{CS}$ to 10% of write current | | 0.11 | 0.6 | µs |
| HS0,1 to any Head | | To 90% of 100 mV 10 MHz Read signal envelope | | 0.11 | 0.6 | µs |
| WUS: | Safe to Unsafe (TD1) | Write mode, loss of WDI transitions. Defines maximum WDI period for WUS operation | 0.6 | 2.0 | 3.6 | µs |
| | Unsafe to Safe (TD2) | Fault cleared, from first neg WDI transition | | 0.1 | 0.6 | µs |
| Head Current: | | | | | | |
| | WDI to Ix - Iy (TD3) | from 50% points, Lh = 0, Rh = 0 | | 3 | 10 | ns |
| | Asymmetry | WDI has 1 ns rise/fall time, Lh = 0, Rh = 0 | | | 1.0 | ns |
| | Rise/fall Time | 10% to 90% points, Lh = 0, Rh = 0 | | 4 | 6 | ns |
| | Rise/fall Time | Lh = 1 µH, Rh = 30Ω | | 7 | | ns |

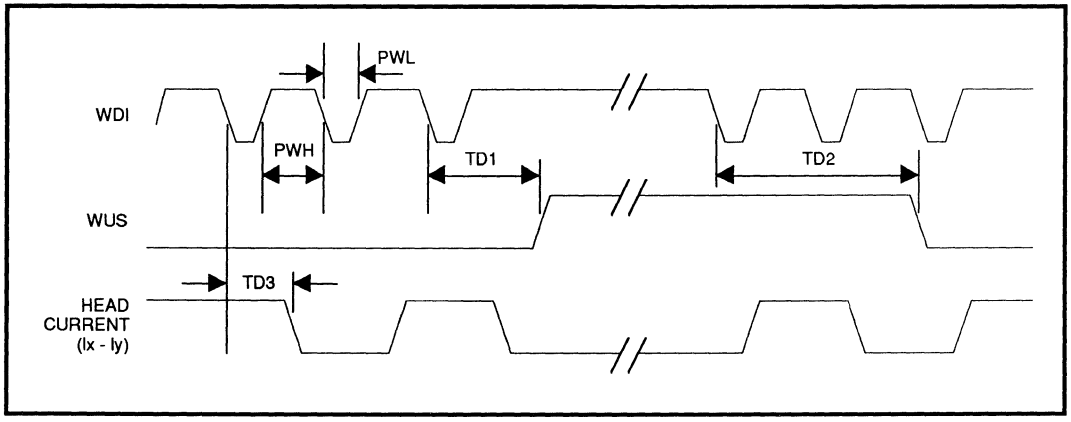
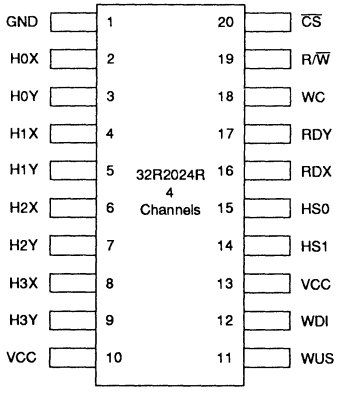



**FIGURE 1: Write Mode Timing Diagram**

## PACKAGE PIN DESIGNATIONS

(Top View)




**20-Lead SOL, SOV**

**Advance Information:** Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.



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**Notes:**

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A TDK Group Company

# SSI 32R2028R
## 5V, 10-Channel Thin-Film Read/Write Device

**Advance Information**

January 1993

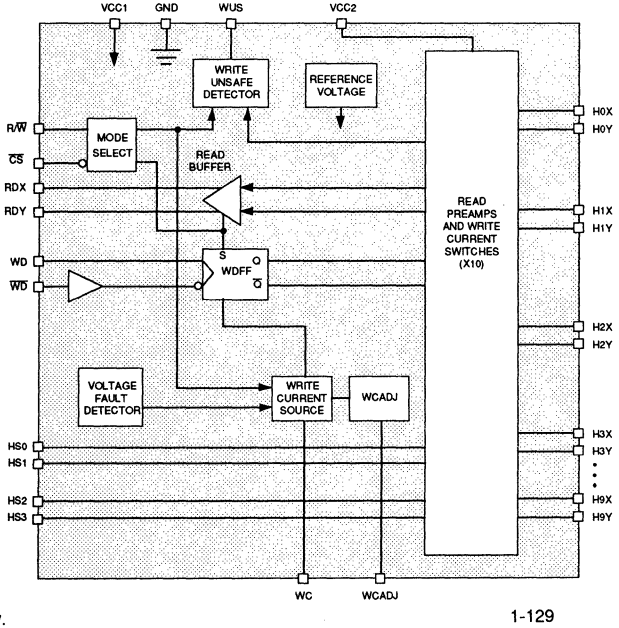
## DESCRIPTION

The SSI 32R2028R is a bipolar monolithic integrated circuits designed for use with two-terminal recording heads. It provides a low noise read amplifier, write current control, and data protection circuitry for up to ten channels. The device provides internal 320Ω damping resistors that are switched in during Write mode and switched out during Read mode. Power supply fault protection is provided by disabling the write current generator during power sequencing. System write to read recovery time is significantly improved by controlling the read channel common mode output voltage shift in the write mode. The device also provides the user with a controllable write current adjustment feature. The SSI 32R2028R requires only a +5V power supply.

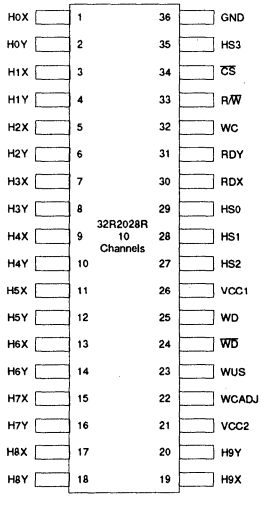
## FEATURES

- +5V ±10% supply
- Low power
  - PD = 130 mW read mode (Nom)
  - PD = 5 mW idle (Max)
- High Performance:
  - Read mode gain = 300 V/V
  - Input noise = 0.56 nV/√Hz (Nom)
  - Input capacitance = 16 pF (Nom)
  - Write current range = 5-35 mA
- Self switching damping resistance
- Designed for two-terminal thin-film or MIG heads with inductance up to 5.0 µH
- Differential ECL-like Write Data Input
- Write unsafe detection
- Power supply fault protection
- Head short to ground protection

## BLOCK DIAGRAM




## PIN DIAGRAM




**36-Lead SOM**

CAUTION: Use handling procedures necessary for a static sensitive component.

# SSI 32R2028R
# 5V, 10-Channel
# Thin-Film Read/Write Device

## CIRCUIT OPERATION

The SSI 32R2028R has the ability to address up to 10 two-terminal heads and provide write drive or read amplification. Mode control and head selection are described in Tables 1 and 2. The TTL inputs R/$\overline{W}$ and $\overline{CS}$ have internal pull-up resistors to prevent an accidental write condition. HS0, HS1, HS2 and HS3 have internal pulldown resistors. Internal clamp circuitry will protect the IC from a head short to ground condition in any mode.

**TABLE 1: Mode Select**

| $\overline{CS}$ | R/$\overline{W}$ | Mode |
|---|---|---|
| 0 | 0 | Write |
| 0 | 1 | Read |
| 1 | 0 | Idle |
| 1 | 1 | Idle |

**TABLE 2: Head Select**

| HS3 | HS2 | HS1 | HS0 | Head |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 2 |
| 0 | 0 | 1 | 1 | 3 |
| 0 | 1 | 0 | 0 | 4 |
| 0 | 1 | 0 | 1 | 5 |
| 0 | 1 | 1 | 0 | 6 |
| 0 | 1 | 1 | 1 | 7 |
| 1 | 0 | 0 | 0 | 8 |
| 1 | 0 | 0 | 1 | 9 |

## PIN DESCRIPTION

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| HS0, HS1, † HS2, HS3 | I | Head Select: selects one of ten heads |
| $\overline{CS}$ | I | Chip Select: a high inhibits the chip |
| R/$\overline{W}$ † | I | Read/Write : a high selects Read mode |
| WUS † | O | Write Unsafe: a high indicates an unsafe writing condition |
| WD, $\overline{WD}$ † | I | Differential Write Data Input: a negative transition of (WD - $\overline{WD}$) toggles the direction of the head current |
| H0X - H9X; H0Y - H9Y | I/O | X, Y Head Connections |
| RDX, RDY † | O | X, Y Read Data: differential read data output |
| WC † | | Write Current: used to set the magnitude of the write current |
| WCADJ † | | Write Current Adjust: Used to fine tune the write current |
| VCC1 | I | +5V Supply |
| VCC2 | I | +5V Supply for Write current drivers |
| GND | I | Ground |
| † When more than one R/W device is used, signals can be wire OR'ed | | |

### WRITE MODE

Taking both $\overline{CS}$ and R/$\overline{W}$ low selects Write mode which configures the SSI 32R2028R as a current switch and activates the Write Unsafe (WUS) detector circuitry. Head current is toggled between the X and Y side of the selected head on each high to low transition of the differential signal WD - $\overline{WD}$. Changing from Read or Idle mode to Write mode initializes the Write Data Flip-Flop to pass write current into the "X" pin. In this case, the Y side of the head will be higher potential than the X side. The magnitude of the write current (0-pk) is given by:

$$Iw = \frac{K \cdot Vwc}{Rwc}$$

Rwc is connected from pin WC to GND. Note the actual head current Ix, y is given by:

$$Ix, y = \frac{Iw}{1 + Rh/Rd}$$

Where:

Rh = Head resistance plus external wire resistance

Rd = Damping resistance

In write mode a 320Ω damping resistor is switched in across the Hx, Hy ports.

The SSI 32R2028R includes a feature which allows the user to adjust the Iw current by a finite amount. The WCADJ pin is used to adjust write current for write operations on different zones of the disk. It is used by switching a separate write current adjust resistor in and out on the WCADJ pin or by connecting a DAC to that pin to sink a controllable amount of current. The WCADJ pin is nominally biased to VCC/2. Sinking current from this pin to ground will divert a proportional amount of current from the actual head current while maintaining a constant current through the WC resistor and VCC. Allowing WCADJ to float or pulling it high will cut off the circuit and it will have no effect. A TTL gate can be used as a switch with a small degradation in accuracy. The amount of write current decrease is shown below:

Iw head (decrease) (mA) = (29 • $V_{WCADJ}/R_{WCADJ}$)

where:

$V_{WCADJ}$ = VCC/2 (volts)

$R_{WCADJ}$ = write current adjust setting resistor (kΩ)

Example: For a 7.25 mA head current decrease, $R_{WCADJ}$ = (27 • 2.5) / 7.25 = 10 kΩ

### POWER SUPPLY FAULT PROTECTION

A voltage fault detection circuit improves data security by disabling the write current generator during a voltage fault or power startup regardless of mode. Note that WUS does not necessarily turn on to flag a power supply fault condition.

### HEAD SHORT TO GROUND PROTECTION

The SSI 32R2028R provides a head short to ground protection circuit in any mode. In Idle or Read Mode, current out of the head port will not exceed 20 mA if any head is shorted to ground. In Write mode, if any head is shorted to ground (regardless if it is selected or not) the write current generator will turn off, the WUS flag will go high, and current will be limited to less than 1 mA out of the head port.

### WRITE UNSAFE

Any of the following conditions will be indicated as a high level on the Write Unsafe, WUS, open collector output.

- WD frequency too low
- Device in Read mode
- Chip disabled
- No head current
- Head opened
- Head short to ground

To insure proper WUS operation, the product of write current, WD frequency, and head inductance should be less than 500 mA•µH•MHz. To insure no false WUS trigger, the product of head current and head resistance (Ix,y•Rh) should be between 100 mV and 1.7V.

**WDI frequency too low** is detected if the WD frequency falls below 500 kHz (typ). Consult the WUS Safe to Unsafe timing for range of frequency detection.

**Device in Read mode** and **Chip disabled** will flag WUS if R/$\overline{W}$ is high or $\overline{CS}$ is high.

**No head current** will flag WUS if Rwc = ∞ and the selected head is present.

**Head opened** will flag WUS if Rh = ∞ and under the condition that VCC/Iw < 0.25 V/mA.

**Head short to ground** is described in the preceding paragraph.

Upon entering write mode, WUS is valid after two transitions of WD following the required Read-Write transition time (0.6 µs max).

## CIRCUIT OPERATION (continued)

### READ MODE

The Read mode configures the SSI 32R2028R as a low noise differential amplifier and deactivates the write current generator. The damping resistor is switched out of the circuit allowing a high impedance input to the read amplifier. The RDX and RDY output are driven by emitter followers. They should be AC coupled to the load. The (X,Y) inputs are non-inverting to the (X,Y) outputs.

Note that in Idle or Write mode, the read amplifier is deactivated and RDX, RDY outputs become high impedance. This facilitates multiple R/W applications (wired-OR RDX, RDY) and minimizes voltage drifts when switching from Write to Read mode. Note also that the write current source is deactivated for both the Read and Idle mode.

### IDLE MODE

Taking $\overline{CS}$ high selects the idle mode which switches the RDX and RDY outputs into a high impedance state and deactivates the device. Power consumption in this mode is held to a minimum.

## ELECTRICAL SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may permanently damage the device.

| PARAMETER | | RATING |
|---|---|---|
| DC Supply Voltage | VCC1 | -0.3 to +6 VDC |
| | VCC2 | -0.3 to +6 VDC |
| Write Current | Iw | 60 mA |
| Digital Input Voltage | Vin | -0.3 to VCC1 +0.3 VDC |
| Head Port Voltage | VH | -0.3 to VCC2 +0.3 VDC |
| Output Current: RDX, RDY | I0 | -6 mA |
| $\overline{WUS}$ | | +8 mA |
| Storage Temperature | Tstg | -65 to +150 °C |

### RECOMMENDED OPERATING CONDITIONS

| | | | |
|---|---|---|---|
| DC Supply Voltage | VCC1 = VCC2 | 5 ±10% | VDC |
| Operating Junction Temperature | Tj | +25 to +135 | °C |
| Recommended Head Load Range | Lh | 0.3 - 5.0 | µH |

### DC CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified.

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| VCC1 Supply Current | Read Mode | | 18 | 25 | mA |
| | Write Mode | | 22 | 29 | mA |
| | Idle Mode | | 0.6 | 0.9 | mA |
| VCC2 Supply Current | Read Mode | | 8 | 11 | mA |
| | Write Mode | | 4 + Iw | 7 + Iw | mA |
| | Idle Mode | | 0 | 0.2 | mA |

**DC CHARACTERISTICS** (continued)

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Power Dissipation | Read Mode | | 130 | 200 | mW |
| | Write Mode | | 130 + 4 Iw | 200 + 4.3 Iw | mW |
| | Idle Mode | | 3 | 5 | mW |
| VCC1 Fault Voltage | Iw < 0.2 mA | 3.5 | 3.9 | 4.2 | VDC |

**DIGITAL INPUTS**

| | | | | | |
|---|---|---|---|---|---|
| Input Low voltage (Vil) HSX, $\overline{CS}$, R/$\overline{W}$ | | | | 0.8 | VDC |
| Input High Voltage (Vil) HSX, $\overline{CS}$, R/$\overline{W}$ | | 2.0 | | | VDC |
| Input Low Current, HSX, $\overline{CS}$, R/$\overline{W}$ | Vil = 0.8V | -0.4 | | | mA |
| Input High Current, HSX, $\overline{CS}$, R/$\overline{W}$ | Vih = 2.0V | | | 100 | µA |
| WD, $\overline{WD}$ Input Low Current | Vil = VCC - 1.75V | | 70 | 100 | µA |
| WD, $\overline{WD}$ Input High Current | Vih = VCC - 0.75V | | 85 | 125 | µA |
| WD, $\overline{WD}$ Input Low Voltage Vil | | Vih - 1.5 | | Vih - 0.5 | VDC |
| WD, $\overline{WD}$ Input High Voltage Vih | | Vcc - 1.50 | | Vcc - 0.5 | VDC |
| Vih - Vil Input Voltage Difference | | 0.5 | 1.0 | 1.5 | V |
| WUS Output Low Voltage (Vol) | Iol = 2 mA max | | | 0.5 | VDC |

**WRITE CHARACTERISTICS**

Recommended operating conditions apply unless otherwise specified.

| | | | | | | |
|---|---|---|---|---|---|---|
| Write Current Constant "K" | | | | 0.99 | | |
| Write Current Voltage (Vwc) | | | 1.15 | 1.25 | 1.35 | V |
| WCADJ Voltage | $I_{WCADJ}$ = 0 to .5 mA | | 2.0 | VCC/2 | 3.0 | VDC |
| Ihead(Decrease)/$I_{WCADJ}$ | | | 23 | 27 | 31 | mA/mA |
| $I_{WCADJ}$ Range | | | 0.0 | | 0.5 | mA |
| Differential Head Voltage Swing | | | 4.2 | 5.6 | | Vpp |
| | Open Head, Iw = 20 mA | | 3.4 | 5.0 | | |
| Unselected Head Current | | | | | 1 | mA (pk) |
| Head Differential Damping Resistance (Rd) | | | | 320 | | Ω |
| WD Pulse Width | Vil ≥ 0.2V | PWH | 10 | | | ns |
| | | PWL | 5 | | | ns |
| Write Current Range (Iw) | | | 5 | | 35 | mA |
| Head Differential Load Capacitance | | | | | 25 | pF |

**READ CHARACTERISTICS**

Recommended operating conditions apply unless otherwise specified. CL (RDX, RDY) < 20 pF, RL (RDX, RDY) = 1 kΩ.

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Differential Voltage Gain | Vin = 1 mVpp @1 MHz | 250 | 300 | 350 | V/V |
| Voltage BW -1dB | \|Zs\| < 5Ω, Vin = 1 mVpp | 20 | | | MHz |
| -3dB | \|Zs\| < 5Ω, Vin = 1 mVpp | 40 | 45 | | MHz |
| Input Noise Voltage | BW = 15 MHz, Lh = 0, Rh = 0 | | 0.56 | 0.75 | nV/√Hz |
| Differential Input Capacitance | Vin = 1 mVpp, $f$ = 5 MHz | | 16 | 22 | pF |
| Differential Input Resistance | Vin = 1 mVpp, $f$ = 5 MHz | 720 | 1200 | | Ω |
| Dynamic Range | AC input voltage where gain falls to 90% of its small signal gain value, $f$ = 5 MHz | 2 | | | mVpp |
| Common Mode Rejection Ratio | Vin = 0 VDC + 100 mVpp @ 5 MHz | 55 | | | dB |
| Power Supply Rejection Ratio | 100 mVpp @ 5 MHz on VCC | 50 | | | dB |
| Channel Separation | Unselected channels driven with Vin = 0 VDC + 100 mVpp | 55 | | | dB |
| Output Offset Voltage | | | | ±300 | mV |
| Single Ended Output Resistance | $f$ = 5 MHz | | | 50 | Ω |
| Output Current | AC coupled load, RDX to RDY | 0.9 | | | mA |
| RDX, RDY Common Mode Output Voltage | | 0.4 VCC | VCC/2 | 0.6 VCC | VDC |

**SWITCHING CHARACTERISTICS**

Recommended operating conditions apply unless otherwise specified. IW = 20 mA, Lh = 1.0 µH, Rh = 30Ω $f$(Data) = 5 MHz.

| | | | | | | |
|---|---|---|---|---|---|---|
| R/$\overline{W}$ | Read to Write | R/W to 90% of write current | | 0.1 | 0.6 | µs |
| | Write to Read | R/W to 90% of 100 mV Read signal envelope | | 0.1 | 0.6 | µs |
| $\overline{CS}$ | Unselect to Select | $\overline{CS}$ to 90% of write current or to 90% of 100 mV 10 MHz | | 0.2 | 1 | µs |
| | Select to Unselect | $\overline{CS}$ to 10% of write current | | 0.11 | 0.6 | µs |
| HS0,1 to any Head | | To 90% of 100 mV 10 MHz Read signal envelope | | 0.11 | 0.6 | µs |
| WUS: | Safe to Unsafe (TD1) | Write mode, loss of WDI transitions. Defines maximum WDI period for WUS operation | 0.6 | 2.0 | 3.6 | µs |
| | Unsafe to Safe (TD2) | Fault cleared, from first neg WDI transition | | 0.1 | 0.6 | µs |

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Head Current: | | | | | |
| WD to Ix - Iy (TD3) | from 50% points, Lh = 0, Rh = 0 | | 8 | 12 | ns |
| Asymmetry | WDI has 1 ns rise/fall time, Lh = 0, Rh = 0 | | | 1.0 | ns |
| Rise/fall Time | 10% to 90% points, Lh = 0, Rh = 0 | | 4 | 6 | ns |
| Rise/fall Time | Lh = 1 µH, Rh = 30Ω | | 15 | | ns |

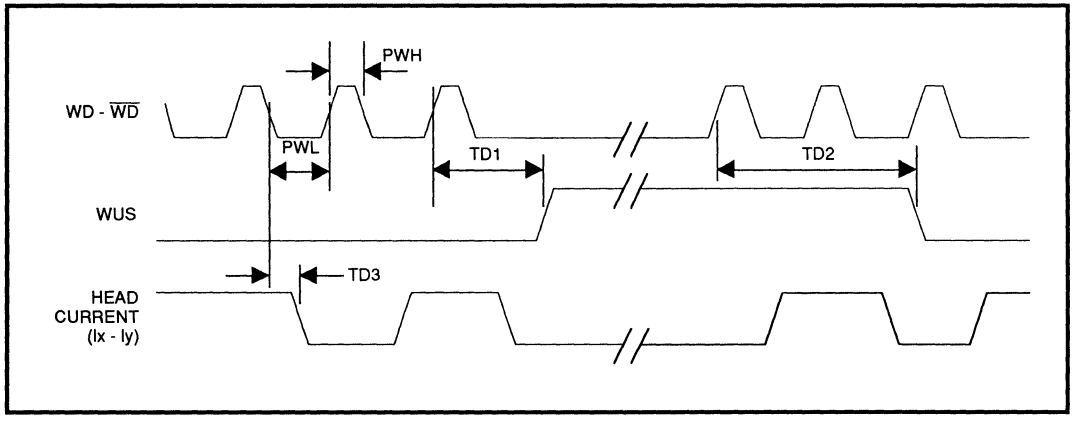
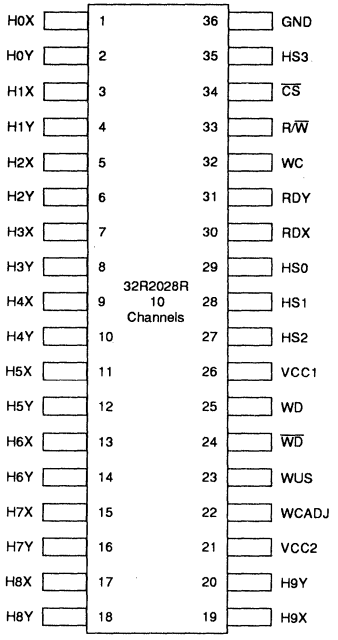



**FIGURE 1: Write Mode Timing Diagram**

# SSI 32R2028R
# 5V, 10-Channel
# Thin-Film Read/Write Device

## PACKAGE PIN DESIGNATIONS

(Top View)




**36-Lead SOM**

**Advance Information:** Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.



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# SSI 32R2030A/2031A
## 5V, 2, 4-Channel Thin-Film Read/Write Device

**Advance Information**

February 1992

## DESCRIPTION

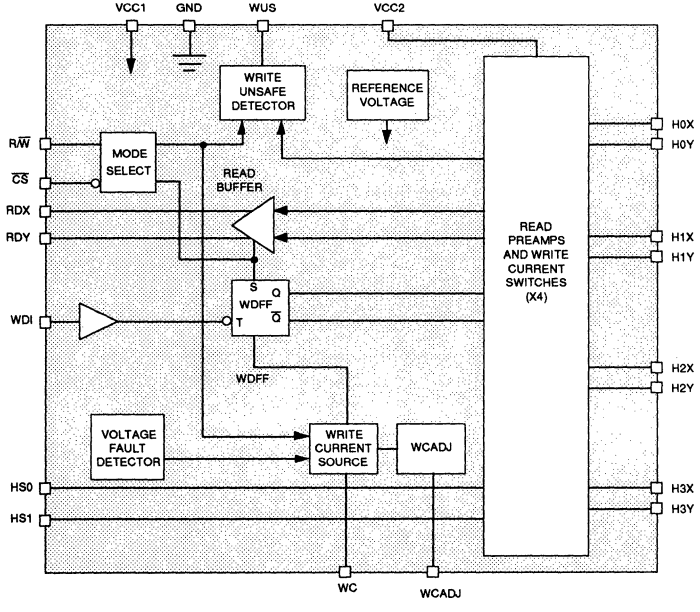
The SSI 32R2030A/2031A are bipolar monolithic integrated circuits designed for use with two-terminal thin-film recording heads. They provide a low noise read amplifier, write current control, and data protection circuitry for up to four channels. The SSI 32R2030AR/2031AR option provides internal 700Ω damping resistors. Power supply fault protection is provided by disabling the write current generator during power sequencing. System write to read recovery time is significantly improved by controlling the read channel common mode output voltage shift in the write mode. The 32R2031A option provides for an additional feature providing the user with a controllable write current adjustment feature.

The SSI 32R2030A/2031A require only +5V power supplies and are available in a variety of packages.

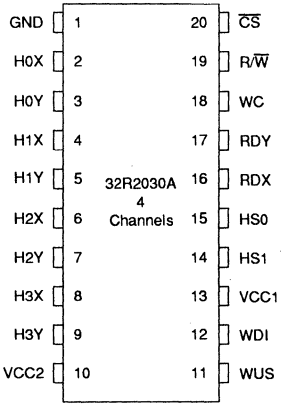
## FEATURES

- **5V ±10%**
- **Low power**
  - **PD = 175 mW read mode (Nom)**
- **High Performance:**
  - **Read mode gain = 250 V/V**
  - **Input noise = 0.85 nV/√Hz max**
  - **Input capacitance = 35 pF max**
  - **Write current range = 10-35 mA**
- **Designed for two-terminal thin-film heads or MIG heads up to 5 μH**
- **Programmable write current source**
- **Write unsafe detection**
- **Enhanced system write to read recovery time**
- **Power supply fault protection**
- **Head short to ground protection**

## BLOCK DIAGRAM




## PIN DIAGRAM




**20-PIN SOL**

CAUTION: Use handling procedures necessary for a static sensitive component.



WCADJ available on the 32R2031A 24-pin option only

# SSI 32R2030A/2031A
# 5V, 2, 4-Channel Thin-Film Read/Write Device

## CIRCUIT OPERATION

The SSI 32R2030A/2031A has the ability to address up to 4 two-terminal thin-film heads and provide write drive or read amplification. Head selection and mode control are described in Tables 2 and 3. The TTL inputs R/$\overline{W}$ and $\overline{CS}$ have internal pull-up resistors to prevent an accidental write condition. HS0, and HS1 have internal pulldowns. Internal clamp circuitry will protect the IC from a head short to ground condition in any mode.

**TABLE 1: Mode Select**

| $\overline{CS}$ | R/$\overline{W}$ | Mode |
|---|---|---|
| 0 | 0 | Write |
| 0 | 1 | Read |
| 1 | 0 | Idle |
| 1 | 1 | Idle |

**TABLE 2: Head Select**

| HS1 | HS0 | Head |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 2 |
| 1 | 1 | 3 |

## PIN DESCRIPTION

| NAME | | TYPE | DESCRIPTION |
|---|---|---|---|
| HS0, HS1 | | I | Head Select: selects one of four heads |
| $\overline{CS}$ | | I | Chip Select: a high inhibits the chip |
| R/$\overline{W}$ | † | I | Read/Write : a high selects Read mode |
| WUS | † | O | Write Unsafe: a high indicates an unsafe writing condition |
| WDI | † | I | Write Data In: changes the direction of the current in the recording head |
| H0X - H7X;<br>H0Y - H7Y | | I/O | X, Y Head Connections |
| RDX, RDY | † | O | X, Y Read Data: differential read data output |
| WC | † | | Write Current: used to set the magnitude of the write current |
| WCADJ* | † | | Write Current Adjust: Used to decrease the write current by a finite amount |
| VCC1 | | I | +5V Supply |
| VCC2 | | I | +5V Supply for Write current drivers |
| GND | | I | Ground |

*Available on 32R2031A 24-pin option only

† These signals can be wire OR'ed

### WRITE MODE

Taking both $\overline{CS}$ and R/$\overline{W}$ low selects write mode which configures the SSI 32R2030A/2031A as a current switch and activates the Write Unsafe (WUS) detector circuitry. Head current is toggled between the X and Y side of the selected head on each high to low transition of the Write Data Input (WDI). The WDI input pulse width requirement is amplitude dependent and pull ups are recommended at higher data rates, please refer to the WDI pulse width specifications. Note that a preceding read or idle mode select initializes the Write Data Flip-Flop to pass write current through the "X" side of the head. The magnitude of the write current (0-pk) is given by:

$$IW = \frac{K \cdot VWC}{RWC}$$

RWC is connected from pin WC to GND. Note the actual head current Ix, y is given by:

$$Ix, y = \frac{Iw}{1 + Rh/Rd}$$

Where:

Rh = Head resistance plus external wire resistance

Rd = Damping resistance

Any of the following conditions will be indicated as a high level on the Write Unsafe, WUS, open collector output.

- WDI frequency too low
- Device in Read mode
- Chip disabled
- No write current

After fault condition is removed, one negative transition on WDI is required to clear WUS.

The 32R2031A adds a feature which allows the user to adjust the Iw current by a finite amount. The WCADJ pin is used to adjust write current for write operations on different zones of the disk. It is used by switching a separate write current adjust resistor in and out on the WCADJ pin or by connecting a DAC to that pin to sink a controllable amount of current. The WCADJ pin is nominally biased to VCC/2. Sinking current from this pin to ground will divert a proportional amount of current from the actual head current while maintaining a constant current through the WC resistor and VCC. Allowing WCADJ to float or pulling it high will cut off the circuit and it will have no effect. For example, if the nominal head current is set to 30 mA through WC with WCADJ open, then for a 7.25 mA head current decrease, a 10 kΩ resistor would be connected from the WCADJ pin to ground. A TTL gate could be used as a switch with a small degradation in accuracy. To perform the same function, a DAC could be used, by programming it to sink 0.25 mA from the WCADJ pin.

Iw head (Decrease) = (29 • $V_{WCADJ}$ / $R_{WCADJ}$)

Where:

VWCADJ = Voltage on WCADJ pin = VCC/2

RWCADJ = Write current adjust setting resistor

### VOLTAGE FAULT

A voltage Fault detection circuit improves data security by disabling the write current generator during a voltage fault or power startup regardless of mode.

### READ MODE

The Read mode configures the SSI 32R2030A/2031A as a low noise differential amplifier and deactivates the write current generator. The RDX and RDY output are driven by emitter followers. They should be AC coupled to the load. The (X,Y) inputs are non-inverting to the (X,Y) outputs.

Note that in Idle or Write mode, the read amplifier is deactivated and RDX, RDY outputs become high impedance. This facilitates multiple R/W applications (wired-OR RDX, RDY) and minimizes voltage drifts when switching from Write to Read mode. Note also that the write current source is deactivated for both the Read and Idle mode.

### IDLE MODE

Taking $\overline{CS}$ high selects the idle mode which switches the RDX and RDY outputs into a high impedance state and deactivates the device. Power consumption in this mode is held to a minimum.

## ELECTRICAL SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may permanently damage the device.

| PARAMETER | | RATING | UNIT |
|---|---|---|---|
| DC Supply Voltage | VCC1 | -0.3 to +7 | VDC |
| | VCC2 | -0.3 to +7 | VDC |
| Write Current | IW | 80 | mA |
| Digital Input Voltage | Vin | -0.3 to VCC1 +0.3 | VDC |
| Head Port Voltage | VH | -0.3 to VCC2 +0.3 | VDC |
| Output Current: RDX, RDY | I0 | -10 | mA |
| WUS | | +12 | mA |
| Storage Temperature | Tstg | -65 to +150 | °C |

### RECOMMENDED OPERATING CONDITIONS

| PARAMETER | | RATING | UNIT |
|---|---|---|---|
| DC Supply Voltage | VCC1 | 5 ±10% | VDC |
| | VCC2 | 5 ±10% | VDC |
| Operating Junction Temperature | Tj | +25 to +110 | °C |

### DC CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified.

| PARAMETER | CONDITIONS | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| VCC1 Supply Current | Read Mode | (Vcc ±5%) | 23 | 28 | 33 | mA |
| | | (Vcc ±10%) | 19 | 28 | 37 | mA |
| | Write Mode | (Vcc ±5%) | 21 | 24 | 27 | mA |
| | | (Vcc ±10%) | 17 | 24 | 31 | mA |
| **Head Select Pins* | *Idle Mode | (Vcc ±5%) | 6 | 9 | 12 | mA |
| *(HS0, HS1) Floating* | | (Vcc ±10%) | 4 | 9 | 14 | mA |
| VCC2 Supply Current | Read Mode | (Vcc ±5%) | 5 | 8 | 11 | mA |
| | | (Vcc ±10%) | 4 | 8 | 12 | mA |
| | Write Mode | (Vcc ±5%) | 6 | 8 + Iw | 10 + Iw | mA |
| | | (Vcc ±10%) | 5 | 8 + Iw | 11 + Iw | mA |
| | Idle Mode | (Vcc ±5%) | 0.1 | 0.2 | 0.4 | mA |
| | | (Vcc ±10%) | 0.1 | 0.2 | 0.5 | mA |
| Power Dissipation | Read Mode | (Vcc ±5%) | | 175 | 230 | mW |
| | | (Vcc ±10%) | | | 270 | mW |

**DC CHARACTERISTICS** (Continued)

| PARAMETER | CONDITIONS | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| Power Dissipation (Continued) | Write Mode | (Vcc ±5%) | | 150 + 4Iw | 190 + 4Iw | mW |
| | | (Vcc ±10%) | | | 230 + 4.4Iw | mW |
| | Idle Mode | (Vcc ±5%) | | 50 | 65 | mW |
| | | (Vcc ±10%) | | | 80 | mW |
| VCC1 Fault Voltage | IW < 0.2 mA | | 3.8 | 4.0 | 4.2 | VDC |

**DIGITAL INPUTS**

| | | | | | |
|---|---|---|---|---|---|
| Input Low voltage (VIL) | | | | 0.8 | VDC |
| Input High Voltage (VIH) | | 2.0 | | | VDC |
| Input Low Current | VIL = 0.8V | -0.4 | | | mA |
| Input High Current | VIH = 2.0V | | | 100 | µA |
| WUS Output Low Voltage (VOL) | Iol = 2 mA max | | | 0.5 | VDC |

**WRITE CHARACTERISTICS**

Recommended operating conditions apply unless otherwise specified.

| | | | | | |
|---|---|---|---|---|---|
| Write Current Constant "K" | | .96 | .99 | | |
| Write Current Voltage (VWC) | | 1.15 | 1.25 | 1.35 | V |
| WCADJ Voltage<br>SSI 32R2031A/2031AR | $I_{WCADJ}$ = 0 to .5 mA | 2.0 | VCC/2 | 3.0 | VDC |
| Ihead(Decrease)/$I_{WCADJ}$<br>SSI 32R2031A/2031AR | | 26 | 29 | 32 | mA/mA |
| $I_{WCADJ}$ Range<br>SSI 32R2031A/2031AR | | 0.0 | | 0.5 | mA |
| Differential Head Voltage Swing | Ih (p-p) • Rh not to exceed 3.4V (Head Swing Min) | 3.4 | | | Vpp |
| Unselected Head Current | | | | 0.02 Iw | mApk |
| Head Differential Load Capacitance | | | | 25 | pF |
| Head Differential Load | SSI 32R2030A/32R2031A | 4K | | | Ω |
| Resistance (Rd) | SSI 32R2030AR/32R2031AR | 560 | 700 | 950 | Ω |
| WDI Pulse Width | Vil = 0.2V, Vih = 2.4V PWH | 37 | | | ns |
| (Ref: Figure 1) | PWL | 5 | | | ns |
| | Vil = 0.2V, Vih = VCC PWH | 20 | | | ns |
| | PWL | 5 | | | ns |
| Write Current Range (IW) | | 10 | | 35 | mA |

**READ CHARACTERISTICS**

Recommended operating conditions apply unless otherwise specified. CL (RDX, RDY) < 20 pF, RL (RDX, RDY) = 1 kΩ.

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| Differential Voltage Gain | | Vin = 1 mVpp @1 MHz | 200 | 250 | 300 | V/V |
| Voltage BW | -1dB | \|Zs\| < 5Ω, Vin = 1 mVpp | 20 | 60 | | MHz |
| | -3dB | | 35 | 70 | | MHz |
| Input Noise Voltage | | BW = 15 MHz, Lh = 0, Rh = 0 | | 0.6 | 0.85 | nV/√Hz |
| Differential Input Capacitance | | Vin = 1 mVpp, $f$ = 5 MHz | | 27 | 35 | pF |
| Differential Input Resistance | | Vin = 1 mVpp, $f$ = 5 MHz<br>SSI 32R2030A/2031A | 835 | 2600 | | Ω |
| | | SSI 32R2030AR/2031AR | 360 | 550 | | Ω |
| Dynamic Range | | AC input voltage where gain falls to 90% of its small signal gain value, $f$ = 5 MHz | 3 | 6 | | mVpp |
| Common Mode Rejection Ratio | | Vin = 0 VDC + 100 mVpp @ 5 MHz | 45 | 80 | | dB |
| Power Supply Rejection Ratio | | 100 mVpp @ 5 MHz on VCC | 40 | 70 | | dB |
| Channel Separation | | Unselected channels driven with Vin = 0 VDC + 100 mVpp | 45 | | | dB |
| Output Offset Voltage | | | -300 | | +300 | mV |
| Single Ended Output Resistance | | $f$ = 5 MHz | | | 40 | Ω |
| Output Current | | AC coupled load, RDX to RDY | 1.4 | | | mA |
| RDX, RDY Common Mode Output Voltage | | | 2.0 | VCC1/2 | 3.5 | VDC |

**SWITCHING CHARACTERISTICS**

Recommended operating conditions apply unless otherwise specified. IW = 20 mA, Lh = 1.0 µH, Rh = 30Ω $f$(Data) = 5 MHz.

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| R/$\overline{W}$ | Read to Write | R/W to 90% of write current | | 0.1 | 1.0 | µs |
| | Write to Read | R/W to 90% of 100 mV Read signal envelope | | 0.5 | 1.0 | µs |
| $\overline{CS}$ | Unselect to Select | $\overline{CS}$ to 90% of write current or to 90% of 100 mV 10 MHz | | 0.4 | 1.0 | µs |
| | Select to Unselect | $\overline{CS}$ to 10% of write current | | 0.4 | 1.0 | µs |
| HS0,1 to any Head | | To 90% of 100 mV 10 MHz Read signal envelope | | 0.2 | 1.0 | µs |
| WUS: | Safe to Unsafe (TD1) | Write mode, loss of WDI transitions. Defines maximum WDI period for WUS operation | 0.6 | 2.0 | 3.6 | µs |
| | Unsafe to Safe (TD2) | Fault cleared from first neg WDI transition | | 0.2 | 1.0 | µs |
| Head Current: | | Lh = 0, Rh = 0 | | | | |
| | WDI to Ix - Iy (TD3) | from 50% points | | 20 | 32 | ns |
| | Asymmetry | WDI has 1 ns rise/fall time | | | 1.0 | ns |
| | Rise/fall Time | 10% to 90% points | | 6 | 12 | ns |

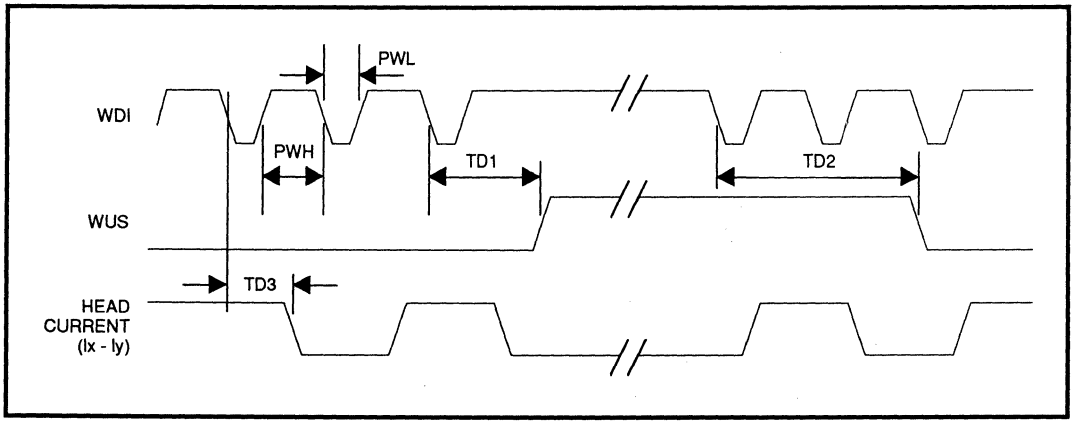



**FIGURE 1: Write Mode Timing Diagram**

## Worst Case Read Input Noise Voltage vs. Input Impedance for SSI 32R2030AR/2031AR

Case 1: IC Base sheet resistance = Maximum
Hence, IC bias Current = Minimum

| | Tj = 25°C | Tj = 110°C | Units |
|---|---|---|---|
| Vn (Max) | .7 | 0.85 | $nV/\sqrt{Hz}$ |
| Rin (Min) | 450 | 475 | Ω |
| Cin (Max) | 28 | 30 | pF |

Case 2: IC Base sheet resistance = Minimum
Hence, IC bias Current = Maximum

| | Tj = 25°C | Tj = 110°C | Units |
|---|---|---|---|
| Vn (Max) | .58 | .65 | $nV/\sqrt{Hz}$ |
| Rin (Min) | 360 | 400 | Ω |
| Cin (Max) | 33 | 35 | pF |

## Worst Case Read Input Noise Voltage vs. Input Impedance for SSI 32R2030A/2031A

Case 1: IC Base sheet resistance = Maximum
Hence, IC bias Current = Minimum

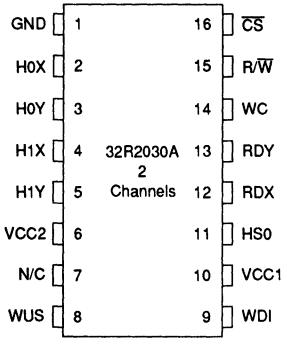
| | Tj = 25°C | Tj = 110°C | Units |
|---|---|---|---|
| Vn (Max) | .7 | 0.85 | $nV/\sqrt{Hz}$ |
| Rin (Min) | 1525 | 1895 | Ω |
| Cin (Max) | 28 | 30 | pF |

Case 2: IC Base sheet resistance = Minimum
Hence, IC bias Current = Maximum

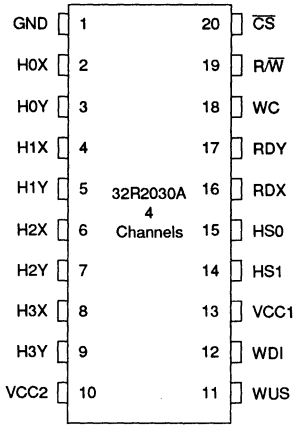
| | Tj = 25°C | Tj = 110°C | Units |
|---|---|---|---|
| Vn (Max) | .58 | .65 | $nV/\sqrt{Hz}$ |
| Rin (Min) | 835 | 1100 | Ω |
| Cin (Max) | 33 | 35 | pF |

## PACKAGE PIN DESIGNATIONS

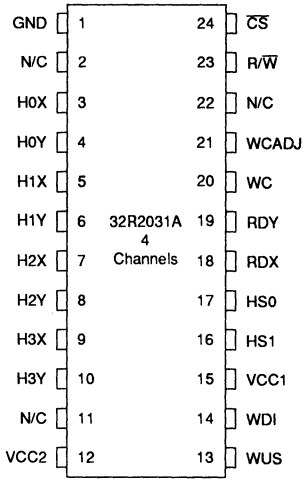
(Top View)




16-Pin SOL




20-Pin SOL, SOV




24-Pin SOL, SOV

### THERMAL CHARACTERISTICS: θja

| | |
|---|---|
| 16-Pin SOL | 105°C/W |
| 20-Pin SOL | 95°C/W |
| 20-Pin SOV | 125°C/W |
| 24-Pin SOL | 80°C/W |

**Advance Information:** Indicates a product still in the design cycle, and any specifications are based on design goals only. Do no use for final design.



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**Notes:**

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# SSI 32R2040
## 14-Channel Two-Terminal Read/Write Device

**Advance Information**

January 1993

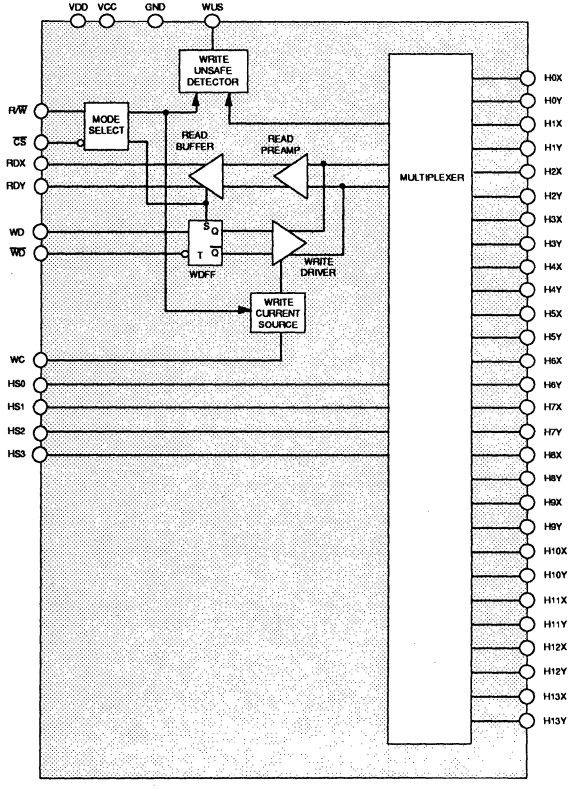
## DESCRIPTION

The SSI 32R2040 Read/Write device is a bipolar monolithic integrated circuit designed for use with two-terminal thin-film recording heads. It provides a low noise read amplifier, write current control and data protection circuitry for up to 14 channels. Power supply fault protection is provided by disabling the write current generator during power sequencing. System write to read recovery time is significantly improved by controlling the read channel common mode output voltage shift in the write mode. The SSI 32R2040 requires +5V and +12V power supplies, and it offers power and performance improvements over the SSI 32R5281R.

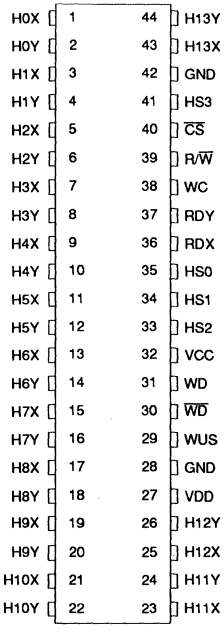
## FEATURES

- **High performance:**
  - **Read mode gain = 150 V/V**
  - **Input noise = 0.80 nV/√Hz max.**
  - **Input capacitance = 22 pF max.**
  - **Write current range = 10 mA to 40 mA**
  - **Head voltage swing = 7 Vpp**
  - **Write current rise time = 9 ns**
- **Enhanced system write to read recovery time**
- **Differential ECL-like Write Data input**
- **Power supply fault protection**
- **Write unsafe detection**
- **+5V, +12V power supplies**

## BLOCK DIAGRAM




## PIN DIAGRAM




**44-LEAD SOM**

CAUTION: Use handling procedures necessary for a static sensitive component.

# SSI 32R2040
# 14-Channel Two-Terminal Read/Write Device

## CIRCUIT OPERATION

The SSI 32R2040 addresses up to 14 two-terminal thin film heads providing write drive or read amplification. Head selection and mode control is accomplished with pins HSn, $\overline{CS}$ and R/$\overline{W}$, as shown in Tables 1 & 2. Internal resistor pullups, provided on pins $\overline{CS}$ and R/$\overline{W}$ will force the device into a non-writing condition if either control line is opened accidentally.

### WRITE MODE

The write mode configures the SSI 32R2040 as a current switch and activates the Write Unsafe (WUS) detection circuitry. Write current is toggled between the X and Y direction of the selected head on each low to high transition on the WD, Write Data input. (See figure 1.)

A preceding read operation initializes the Write Data Flip Flop (WDFF) to pass write current in the X-direction of the head, i.e., into the X-port of the head. HnX will be biased higher than HnY.

The magnitude of the write current (0-pk) is given by:

$$Iw = \frac{Vwc}{Rwc}$$

where Vwc (WC pin voltage) = 1.65V ± 5%, is programmed by an external resistor Rwc, connected from pin WC to ground. In multiple device applications, a single Rwc resistor may be made common to all devices. The actual head current Ix, y is given by:

$$Ix,y = \frac{Iw}{1 + Rh/Rd}$$

where:
Rh = head resistance + external wire resistance, and
Rd = damping resistance.

Power supply fault protection improves data security by disabling the write current generator during a voltage fault or power supply sequencing. Additionally, the write unsafe detection circuitry will flag any of the conditions listed below as a high level on the open collector output pin, WUS. Up to two positive transitions on the WD, Write Data input line, after the fault is corrected, are required to clear the WUS flag.

- WD frequency too low
- Device not selected
- Open head
- Device in read mode
- No write current

### READ MODE

The read mode configures the SSI 32R2040 as a low noise differential amplifier and deactivates the write current generator and write unsafe detection circuitry. The RDX and RDY outputs are emitter followers and are in phase with the "X" and "Y" head ports. These outputs should be AC coupled to the load. The RDX, RDY common mode voltage is maintained at the write mode value, minimizing the transient between write mode and read mode, substantially reducing the write to read recovery time in the subsequent Pulse Detection circuitry.

### IDLE MODE

The idle mode deactivates the internal write current generator, the write unsafe detector and switches the RDX, RDY outputs into a high impedance state. This facilitates multiple device applications by enabling the read outputs to be wire-OR'ed and the write current programming resistor to be common to all devices.

**TABLE 1: Mode Select**

| $\overline{CS}$ | R/$\overline{W}$ | MODE |
|---|---|---|
| 0 | 0 | Write |
| 0 | 1 | Read |
| 1 | 0 | Idle |
| 1 | 1 | Idle |

**TABLE 2: Head Select***

| HS3 | HS2 | HS1 | HS0 | HEAD |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 2 |
| 0 | 0 | 1 | 1 | 3 |
| 0 | 1 | 0 | 0 | 4 |
| 0 | 1 | 0 | 1 | 5 |
| 0 | 1 | 1 | 0 | 6 |
| 0 | 1 | 1 | 1 | 7 |
| 1 | 0 | 0 | 0 | 8 |
| 1 | 0 | 0 | 1 | 9 |
| 1 | 0 | 1 | 0 | 10 |
| 1 | 0 | 1 | 1 | 11 |
| 1 | 1 | 0 | 0 | 12 |
| 1 | 1 | 0 | 1 | 13 |

0 = Low level  1 = High level

*Unused heads should be left open.

## PIN DESCRIPTION

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| HSO - HS3 | I | Head Select |
| $\overline{CS}$ | I | Chip Select: a low level enables the device |
| R/$\overline{W}$ | I | Read/Write: a high level selects Read mode |
| WUS | O* | Write Unsafe: Open collector output, a high level indicates an unsafe writing condition |
| WD, $\overline{WD}$ | I | Differential Write Data inputs: a positive transition on WD toggles the direction of the head current |
| H0X - H13X<br>H0Y - H13Y | I/O | X, Y Head Connections: Current in the X-direction flows into the X-port |
| RDX, RDY | O* | X, Y Read Data: differential read data output |
| WC | * | Write Current: used to set the magnitude of the write current |
| VCC | - | +5V Logic Circuit Supply |
| VDD | - | +12V |
| GND | - | Ground |

*When more than one R/W device is used, these signals can be wire OR'ed.

## ELECTRICAL SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS

Operation outside these rating limits may permanently damage the device.

| PARAMETER | | SYMBOL | RATING |
|---|---|---|---|
| DC Supply Voltage | | VDD | -0.3 to +13.5 VDC |
| | | VCC | -0.3 to +6 VDC |
| Write Current | | Iw | 100 mA |
| Digital Input Voltage | | Vin | -0.3 to VCC +0.3 VDC |
| Head Port Voltage | | VH | -0.3 to +8 VDC |
| Differential Port Voltage | \|HnX - HnY\| | ΔVH | 6 VDC |
| WUS Pin Voltage Range | | Vwus | -0.3 to VCC VDC |
| Output Current | RDX, RDY | Io | -10 mA |
| | WUS | Iwus | +12 mA |
| Storage Temperature | | Tstg | -65 to +150°C |

**RECOMMENDED OPERATING CONDITIONS**

| PARAMETER | SYMBOL | RATING |
|---|---|---|
| DC Supply Voltage | VDD | 12 ± 10% VDC |
| | VCC | 5 ± 10% VDC |
| Operating Temperature | Tj | +25 to +135°C |

**DC CHARACTERISTICS**

Unless otherwise specified, recommended operating conditions apply.

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|
| VDD Supply Current | Read Mode | - | 36 | 44 | mA |
| | Write Mode | - | 25 + Iw | 29 + Iw | mA |
| | Idle Mode | - | 3.5 | 4 | mA |
| VCC Supply Current | Read Mode | - | 22 | 29 | mA |
| | Write Mode | - | 14 | 18 | mA |
| | Idle Mode | - | 9 | 11.5 | mA |
| Power Dissipation (Tj = +135°C) | Read Mode | - | 540 | 740 | mW |
| | Write Mode | - | 370+10.35•Iw | 490 +11.6•Iw | mW |
| | Idle Mode | - | 87 | 115 | mW |
| WD, $\overline{WD}$ Input Low Current (IIL1) | VIL1 = VCC -1.625V | | | 80 | µA |
| WD, $\overline{WD}$ Input High Current (IIH1) | VIH1 = VCC -0.72V | | | 100 | µA |
| WD, $\overline{WD}$ Input Low Voltage (VIL1) | | VCC -1.870 | | VCC -1.625 | VDC |
| WD, $\overline{WD}$ Input High Voltage (VIH1) | | VCC -1.00 | | VCC -0.720 | VDC |
| R/$\overline{W}$, $\overline{CS}$, HS0-HS3 Input Low Current (IIL2) | VIL2 = 0.8V | -0.4 | | | mA |
| R/$\overline{W}$, $\overline{CS}$, HS0-HS3 Input High Current (IIH2) | VIH2 = 2.0V | | | 100 | µA |
| R/$\overline{W}$, $\overline{CS}$, HS0-HS3 Input Low Voltage (VIL2) | | | | 0.8 | VDC |
| R/$\overline{W}$, $\overline{CS}$, HS0-HS3 Input High Voltage (VIH2) | | 2.0 | | | VDC |
| WUS Output Low Voltage (VOL) | Iol = 8 mA | - | - | 0.5 | VDC |
| VDD Fault Voltage | | 9.0 | - | 10.3 | VDC |
| VCC Fault Voltage | | 3.5 | - | 4.2 | VDC |

**DC CHARACTERISTICS** (continued)

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|
| Head Current (HnX, HnY) | Write Mode,<br>0 ≤ VCC ≤ 3.5V<br>0 ≤ VDD ≤ 9.0V | -200 | - | +200 | µA |
| | Read/Idle Mode,<br>0 ≤ VCC ≤ 5.5V<br>0 ≤ VDD ≤13.2V | -200 | - | +200 | µA |

**WRITE CHARACTERISTICS**

Unless otherwise specified, recommended operating conditions apply, Iw = 20 mA, Lh = 500 nH, Rh = 30Ω and f(WD) = 5 MHz.

| | | | | | |
|---|---|---|---|---|---|
| WC Pin Voltage (Vwc) | 10 ≤ Iw ≤ 40 mA | 1.57 | 1.65 | 1.73 | V |
| Differential Head Voltage Swing | | 7 | - | - | Vpp |
| Unselected Head Current | | - | - | 1 | mA(pk) |
| Differential Output Capacitance | | - | - | 25 | pF |
| Differential Output Resistance | | - | 2000 | - | Ω |
| WDI Transition Frequency | WUS = low | 1.7 | - | - | MHz |
| | WUS = high | - | - | 500 | kHz |
| Write Current Range | | 10 | - | 40 | mA |

**READ CHARACTERISTICS**

Unless otherwise specified, recommended operating conditions apply CL (RDX, RDY) < 20pF and RL (RDX,RDY) = 1 kΩ.

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|---|
| Differential Voltage Gain | | Vin=1mVpp @ 300 kHz | 120 | 150 | 180 | V/V |
| Bandwidth | -1dB | \|Zs\|<5Ω, Vin=1 mVpp | 25 | 40 | - | MHz |
| | -3dB | \|Zs\|<5Ω, Vin=1 mVpp | 35 | 55 | - | MHz |
| Input Noise Voltage | | BW = 15 MHz, Lh = 0, Rh = 0 | - | 0.57 | 0.80 | nV/√Hz |
| Differential Input Capacitance | | Vin = 1 mVpp, f = 5 MHz | - | 15 | 22 | pF |
| Differential Input Resistance | | Vin = 1 mVpp, f = 5 MHz | 750 | 1000 | - | Ω |
| Dynamic Range | | Peak-to-peak AC input voltage where gain falls to 90% of its small signal value, f = 5 MHz | 2.0 | - | - | mVpp |
| Common Mode Rejection Ratio | | Vcm = 100 mVpp AC Coupled @ 5 MHz | 54 | - | - | dB |
| Power Supply Rejection Ratio | | 100 mVpp @ 5 MHz on VDD<br>100 mVpp @ 5 MHz on VCC | 54 | - | - | dB |
| Channel Separation | | Unselected channels driven with 100 mVpp @ 5 MHz, Vin = 0 mVpp | 45 | - | - | dB |

**READ CHARACTERISTICS** (continued)

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|
| Output Offset Voltage | | -400 | - | +400 | mV |
| RDX, RDY Common Mode Output Voltage | Read Mode | 2.3 | 2.9 | 3.5 | VDC |
| Single Ended Output Resistance | f = 5 MHz | - | - | 30 | Ω |
| Output Current | AC Coupled Load, RDX to RDY | 3.2 | - | - | mA |

**SWITCHING CHARACTERISTICS** (See Figure 1)
Unless otherwise specified, recommended operating conditions apply, Iw = 20 mA, Lh = 500 nH, Rh = 30Ω and f(WD) = 5 MHz.

| | | | | | |
|---|---|---|---|---|---|
| R/$\overline{W}$ | | | | | |
| R/$\overline{W}$ to Write Mode | Delay to 90% of write current | - | - | 0.6 | µs |
| R/$\overline{W}$ to Read Mode | Delay to 90% of 100 mV 10 MHz Read signal envelope or to 90% decay of write current | - | - | 0.6 | µs |
| $\overline{CS}$ | | | | | |
| $\overline{CS}$ to Select | Delay to 90% of write current or to 90% of 100 mV 10 MHz Read signal envelope | - | - | 0.6 | µs |
| $\overline{CS}$ to Unselect | Delay to 90% of write current | - | - | 0.6 | µs |
| HSn | | | | | |
| HS0, 1, 2, 3 to any Head | Delay to 90% of 100 mV 10 MHz Read signal envelope | - | - | 0.4 | µs |
| WUS | | | | | |
| Safe to Unsafe - TD1 | | - | 0.6 | 2.0 | µs |
| Unsafe to Safe - TD2 | | - | - | 1 | µs |
| Head Current | | | | | |
| Prop. Delay - TD3 | From 50% points, Lh=0 µh, Rh=0Ω | - | - | 32 | ns |
| Asymmetry | WD has 50% duty cycle and 1ns rise/fall time, Lh=0 µh, Rh=0Ω | - | - | 0.5 | ns |
| Rise/Fall Time | 10% - 90% points, Lh=0 µh, Rh=0Ω | - | - | 5 | ns |
| Rise/Fall Time | 10% - 90% points, Lh=1 µh, Rh=35Ω | - | TBD | - | ns |

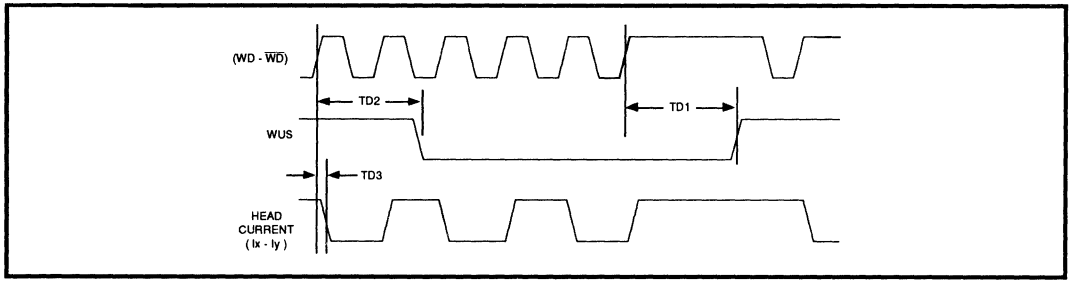


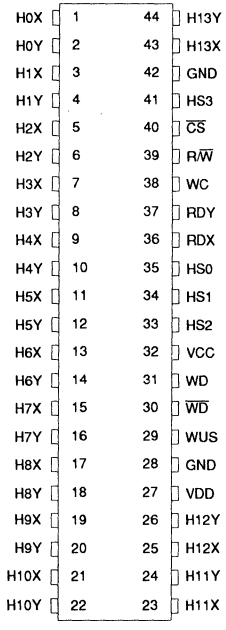

**FIGURE 1: Write Mode Timing Diagram**

## PACKAGE PIN DESIGNATIONS

(Top View)

### THERMAL CHARACTERISTICS: θja

| | |
|---|---|
| 44-Lead SOM | 40°C/W |




**44-Lead SOM**

**Advance Information:** Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.



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**Notes:**

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A TDK Group Company

# SSI 32R2060
## 5V, 8-Channel Thin-Film Read/Write Device
## Advance Information

December 1992

## DESCRIPTION

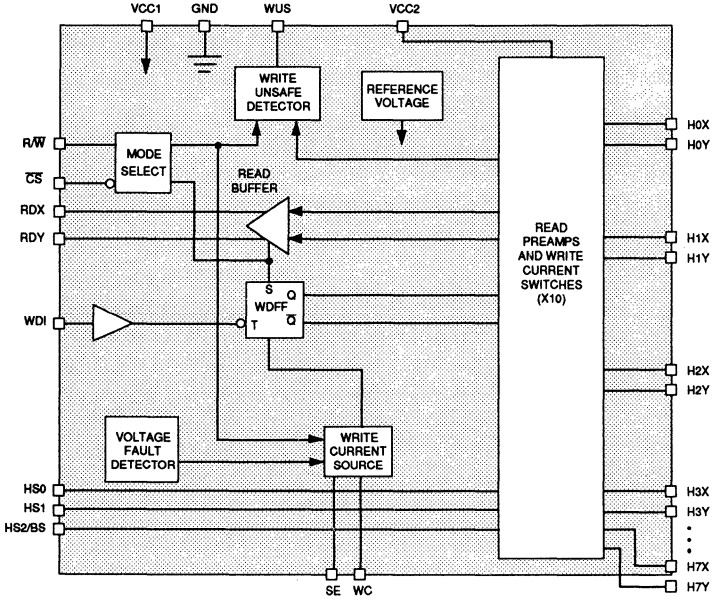
The SSI 32R2060 is a bipolar monolithic integrated circuit designed for use with two-terminal recording heads. It provides a low noise read amplifier, write current control, and data protection circuitry for up to eight channels. Power supply fault protection is provided by disabling the write current generator during power sequencing. System write to read recovery time is significantly improved by controlling the read channel common mode output voltage shift in the write mode.

The 32R2060 provides multiple channel write capability to assist in servo writing operations.

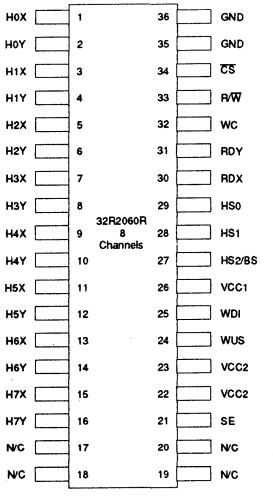
## FEATURES

- **+5V ±10% supply**
- **Low power**
  - **PD = 130 mW read mode (Nom)**
  - **PD = 5 mW idle (Max)**
- **High Performance:**
  - **Read mode gain = 250 V/V**
  - **Input noise = 0.56 nV/√Hz (Nom)**
  - **Input capacitance = 16 pF (Nom)**
  - **Write current range = 5-35 mA**
- **Designed for two-terminal thin-film or MIG heads with inductance up to 5.0 μH**
- **Multiple channel write capability**
- **Write unsafe detection**
- **Power supply fault protection**
- **Head short to ground protection**

## BLOCK DIAGRAM




## PIN DIAGRAM




**36-Lead SOM**

CAUTION: Use handling procedures necessary for a static sensitive component.

## CIRCUIT OPERATION

The SSI 32R2060 has the ability to address up to 8 two-terminal heads and provide write drive or read amplification. Mode control and head selection are described in Tables 1 and 2. The TTL inputs R/$\overline{W}$ and $\overline{CS}$ have internal pull-up resistors to prevent an accidental write condition. HS0, HS1, HS2/BS and SE have internal pulldown resistors. Internal clamp circuitry will protect the IC from a head short to ground condition in any mode.

**TABLE 1: Mode Select**

| $\overline{CS}$ | R/$\overline{W}$ | SE | HS2/BS* | Mode |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | Single Channel Write. See Table 2. |
| 0 | 0 | 0 | 1 | Single Channel Write. See Table 2. |
| 0 | 0 | 1 | 0 | Servo Write Channels 0, 1, 2, 3 |
| 0 | 0 | 1 | 1 | Servo Write Channels 4, 5, 6, 7 |
| 0 | 1 | X | X | Single Channel Read. See Table 2. |
| 1 | X | X | X | Idle. |

*HS2/BS is: HS2 in Read or Write mode (SE = 0)
BS in Servo Pack Write mode (SE = 1, R/$\overline{W}$ = 0)

**TABLE 2: Head Select**

| HS2/BS | HS1 | HS0 | Head |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 2 |
| 0 | 1 | 1 | 3 |
| 1 | 0 | 0 | 4 |
| 1 | 0 | 1 | 5 |
| 1 | 1 | 0 | 6 |
| 1 | 1 | 1 | 7 |

### WRITE MODE

Taking both $\overline{CS}$ and R/$\overline{W}$ low selects Write mode which configures the SSI 32R2060 as a current switch and activates the Write Unsafe (WUS) detector circuitry. Head current is toggled between the X and Y side of the selected head on each high to low transition of the Write Data Input (WDI). Changing from Read or Idle mode to Write mode initializes the Write Data Flip-Flop to pass write current into the "X" pin. In this case, the Y side of the head will be higher potential than the X side.

The magnitude of the write current (0-pk) is given by:

$$Iw = \frac{Aw \cdot Vwc}{Rwc}$$

Rwc is connected from pin WC to GND. Note the actual head current Ix, y is given by:

$$Ix, y = \frac{Iw}{1 + Rh/Rd}$$

Where:

Rh = Head resistance plus external wire resistance

Rd = Damping resistance

### SERVO WRITE MODE

Taking SE high and R/$\overline{W}$ low activates Servo Write mode. This mode allows for writing to multiple channels at once, which is useful during servo formatting. In this mode, selecting BS=0 will cause the write driver to drive channels 0, 1, 2, and 3 simultaneously. Selecting BS=1 will cause the write driver to drive channels 4, 5, 6, and 7 simultaneously.

### POWER SUPPLY FAULT PROTECTION

A voltage fault detection circuit improves data security by disabling the write current generator during a voltage fault or power startup regardless of mode. Note that WUS does not necessarily turn on to flag a power supply fault condition.

### HEAD SHORT TO GROUND PROTECTION

The 2060 provides a head short to ground protection circuit in any mode. In Idle or Read Mode, current out of the head port will not exceed 20 mA if any head is shorted to ground. In Write mode, if any head is shorted to ground (regardless if it is selected or not) the write current generator will turn off, the WUS flag will go high, and current will be limited to less than 1 mA out of the head port.

### WRITE UNSAFE

Any of the following conditions will be indicated as a high level on the Write Unsafe, WUS, open collector output.

- WDI frequency too low
- Device in Read mode
- Device in servo Write mode
- Chip disabled
- No head current
- Head opened
- Head short to ground

To insure proper WUS operation, the product of write current, WDI frequency, and head inductance should be less than 500 mA•µH•MHz. To insure no false WUS trigger, the product of head current and head resistance (Ix,y•Rh) should be between 100 mV and 1.7V.

**WDI frequency too low** is detected if the WDI frequency falls below 500 kHz (typ). Consult the WUS Safe to Unsafe timing for range of frequency detection.

**Device in Read mode, Device in servo Write mode** and **Chip disabled** will flag WUS if R/$\overline{W}$ is high, if SE is high, or $\overline{CS}$ is high.

**No head current** will flag WUS if Rwc = ∞ and the selected head is present.

**Head opened** will flag WUS if Rh = ∞ and under the condition that VCC/Iw < 0.25 V/mA.

**Head short to ground** is described in the preceding paragraph.

Upon entering write mode, WUS is valid after two high to low transitions of WDI following the required Read-Write transition time (0.6 µs max).

### READ MODE

The Read mode configures the SSI 32R2060 as a low noise differential amplifier and deactivates the write current generator. The damping resistor is switched out of the circuit allowing a high impedance input to the read amplifier. The RDX and RDY output are driven by emitter followers. They should be AC coupled to the load. The (X,Y) inputs are non-inverting to the (X,Y) outputs.

Note that in Idle, Write or Servo Write mode, the read amplifier is deactivated and RDX, RDY outputs become high impedance. This facilitates multiple R/W applications (wired-OR RDX, RDY) and minimizes voltage drifts when switching from Write to Read mode. Note also that the write current source is deactivated for both the Read and Idle mode.

### IDLE MODE

Taking $\overline{CS}$ high selects the idle mode which switches the RDX and RDY outputs into a high impedance state and deactivates the device. Power consumption in this mode is held to a minimum.

## PIN DESCRIPTION

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| HS0, HS1, † | I | Head Select: selects one of eight heads |
| HS2/BS | I | Head Select 2 in normal mode (SE = 0). Bank Select in Servo Write mode (SE = 1, R/$\overline{W}$ = 0) |
| $\overline{CS}$ | I | Chip Select: a high inhibits the chip |
| R/$\overline{W}$ † | I | Read/Write : a high selects Read mode |
| WUS † | O | Write Unsafe: a high indicates an unsafe writing condition |
| WDI † | I | Write Data In: changes the direction of the current in the recording head |
| H0X - H7X; H0Y - H7Y | I/O | X, Y Head Connections |
| RDX, RDY † | O | X, Y Read Data: differential read data output |
| WC † | | Write Current: used to set the magnitude of the write current |
| VCC1 | I | +5V Supply |
| VCC2 | I | +5V Supply for Write current drivers |
| GND | I | Ground |
| SE | I | When active, and R/$\overline{W}$ = 0, activates Servo Write mode. |

† When more than one R/W device is used, signals can be wire OR'ed

## ELECTRICAL SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may permanently damage the device.

| PARAMETER | | RATING |
|---|---|---|
| DC Supply Voltage | VCC1 | -0.3 to +6 VDC |
| | VCC2 | -0.3 to +6 VDC |
| Write Current | Iw | 60 mA |
| Digital Input Voltage | Vin | -0.3 to VCC1 +0.3 VDC |
| Head Port Voltage | VH | -0.3 to VCC2 +0.3 VDC |
| Output Current: RDX, RDY | I0 | -6 mA |
| WUS | | +8 mA |
| Storage Temperature | Tstg | -65 to +150 °C |

### RECOMMENDED OPERATING CONDITIONS

| | | | |
|---|---|---|---|
| DC Supply Voltage | VCC1 = VCC2 | 5 ±10% | VDC |
| Operating Junction Temperature | Tj | +25 to +135 | °C |
| Recommended Head Load Range | Lh | 0.3 - 5.0 | µH |

### DC CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified.

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| VCC1 Supply Current | Read Mode | | 18 | 25 | mA |
| | Write Mode | | 22 | 29 | mA |
| | Idle Mode | | 0.6 | 0.9 | mA |
| VCC2 Supply Current | Read Mode | | 8 | 11 | mA |
| | Write Mode | | 4 + Iw | 7 + Iw | mA |
| | Idle Mode | | 0 | 0.2 | mA |
| Power Dissipation | Read Mode | | 130 | 200 | mW |
| | Write Mode | | 130 + 4 Iw | 200 + 4.3 Iw | mW |
| | Idle Mode | | 3 | 5 | mW |
| VCC1 Fault Voltage | Iw < 0.2 mA | 3.5 | 3.9 | 4.2 | VDC |

## ELECTRICAL SPECIFICATIONS (continued)

### DIGITAL INPUTS

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Input Low voltage (Vil) | | | | 0.8 | VDC |
| Input High Voltage (Vil) | | 2.0 | | | VDC |
| Input Low Current | Vil = 0.8V | -0.4 | | | mA |
| Input High Current | Vih = 2.0V | | | 100 | µA |
| WUS Output Low Voltage (Vol) | Iol = 2 mA max | | | 0.5 | VDC |

### WRITE CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified.

| | | | | | | |
|---|---|---|---|---|---|---|
| Write Current Gain "Aw" | Iw = Aw • Vwc/Rwc | | | 20 | | mA/mA |
| Write Current Voltage (Vwc) | | | 2.375 | 2.5 | 2.625 | V |
| Differential Head Voltage Swing | Open Head<br>Iw = 20 mA | | 4.2 | 5.6 | | Vpp |
| Unselected Head Current | | | | | 1 | mA (pk) |
| Head Differential Damping Resistance (Rd) | | | 2200 | | | Ω |
| WDI Pulse Width | Vil ≥ 0.2V | PWH | 10 | | | ns |
| | | PWL | 5 | | | ns |
| Write Current Range (Iw) | | | 5 | | 35 | mA |
| Head Differential Load Capacitance | | | | | 25 | pF |

### SERVO WRITE CHARACTERISTICS

| | | | | | |
|---|---|---|---|---|---|
| Write Current Range | | 5 | | 25 | mA |
| Write Current Matching | Between channels | | +10% | | |

**READ CHARACTERISTICS**

Recommended operating conditions apply unless otherwise specified. CL (RDX, RDY) < 20 pF, RL (RDX, RDY) = 1 kΩ.

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Differential Voltage Gain | Vin = 1 mVpp @1 MHz | 250 | 300 | 350 | V/V |
| Voltage BW -1dB | \|Zs\| < 5Ω, Vin = 1 mVpp | 20 | | | MHz |
| -3dB | \|Zs\| < 5Ω, Vin = 1 mVpp | 45 | | | MHz |
| Input Noise Voltage | BW = 15 MHz, Lh = 0, Rh = 0 | | 0.56 | 0.75 | nV/√Hz |
| Differential Input Capacitance | Vin = 1 mVpp, $f$ = 5 MHz | | 16 | 22 | pF |
| Differential Input Resistance | Vin = 1 mVpp, $f$ = 5 MHz | 720 | 1200 | | Ω |
| Dynamic Range | AC input voltage where gain falls to 90% of its small signal gain value, $f$ = 5 MHz | 2 | | | mVpp |
| Common Mode Rejection Ratio | Vin = 0 VDC + 100 mVpp @ 5 MHz | 55 | | | dB |
| Power Supply Rejection Ratio | 100 mVpp @ 5 MHz on VCC | 50 | | | dB |
| Channel Separation | Unselected channels driven with Vin = 0 VDC + 100 mVpp | 55 | | | dB |
| Output Offset Voltage | | | | ±300 | mV |
| Single Ended Output Resistance | $f$ = 5 MHz | | | 50 | Ω |
| Output Current | AC coupled load, RDX to RDY | 0.9 | | | mA |
| RDX, RDY Common Mode Output Voltage | | 0.4 VCC | VCC/2 | 0.6 VCC | VDC |

**SWITCHING CHARACTERISTICS**

Recommended operating conditions apply unless otherwise specified. IW = 20 mA, Lh = 1.0 µH, Rh = 30Ω $f$(Data) = 5 MHz.

| | | | | | | |
|---|---|---|---|---|---|---|
| R/$\overline{W}$ | Read to Write | R/W to 90% of write current | | 0.1 | 0.6 | µs |
| | Write to Read | R/W to 90% of 100 mV Read signal envelope | | 0.1 | 0.6 | µs |
| $\overline{CS}$ | Unselect to Select | $\overline{CS}$ to 90% of write current or to 90% of 100 mV 10 MHz | | 0.2 | 1 | µs |
| | Select to Unselect | $\overline{CS}$ to 10% of write current | | 0.11 | 0.6 | µs |
| HS0,1 to any Head | | To 90% of 100 mV 10 MHz Read signal envelope | | 0.11 | 0.6 | µs |
| WUS: | Safe to Unsafe (TD1) | Write mode, loss of WDI transitions. Defines maximum WDI period for WUS operation | 0.6 | 2.0 | 3.6 | µs |
| | Unsafe to Safe (TD2) | Fault cleared, from first neg WDI transition | | 0.1 | 0.6 | µs |

## ELECTRICAL SPECIFICATIONS (continued)

### SWITCHING CHARACTERISTICS (continued)

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Head Current: | | | | | |
| WDI to Ix - Iy (TD3) | from 50% points, Lh = 0, Rh = 0 | | 3 | 10 | ns |
| Asymmetry | WDI has 1 ns rise/fall time, Lh = 0, Rh = 0 | | | 1.0 | ns |
| Rise/fall Time | 10% to 90% points, Lh = 0, Rh = 0 | | 4 | 6 | ns |
| Rise/fall Time | Lh = 1 µH, Rh = 30Ω | | 15 | | ns |

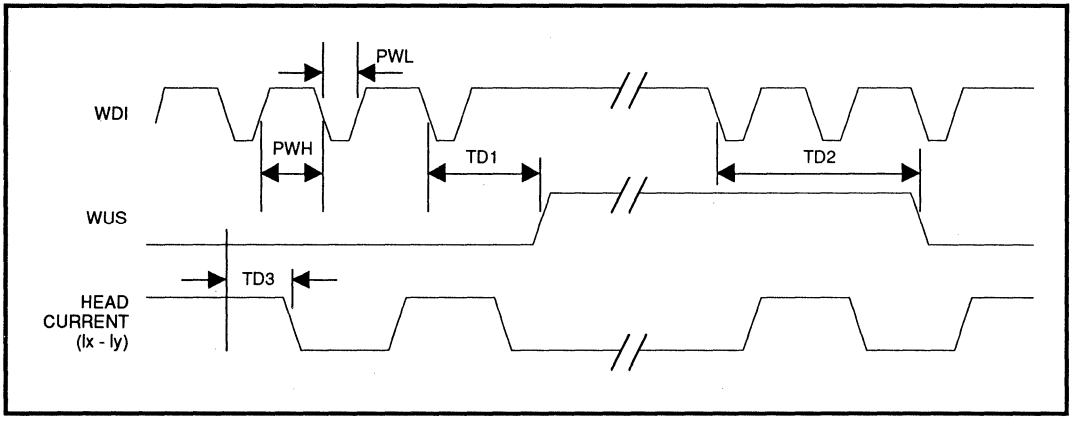
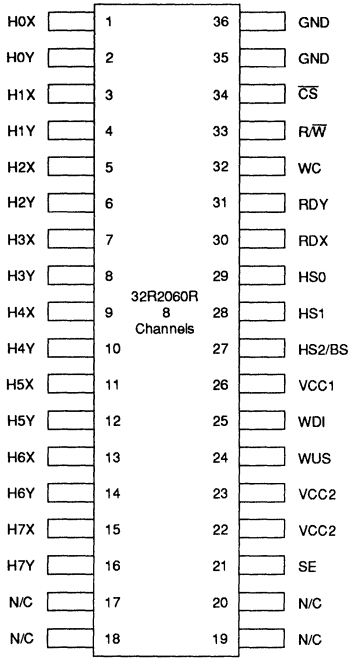



**FIGURE 1: Write Mode Timing Diagram**

## PACKAGE PIN DESIGNATIONS

(Top View)




**36-Lead SOM**

**Advance Information:** Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.



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**Notes:**

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# SSI 32R2063/2064/2065
## 5V, 4-Channel Thin-Film Read/Write Device
## Target Specification

January 1993

## DESCRIPTION

The SSI 32R2063/64/64 are a bipolar monolithic integrated circuits designed for use with two-terminal recording heads. They provide a low noise read amplifier, write current control, and data protection circuitry for up to four channels. Power supply fault protection is provided by disabling the write current generator during power sequencing. System write to read recovery time is significantly improved by controlling the read channel common mode output voltage shift in the write mode.

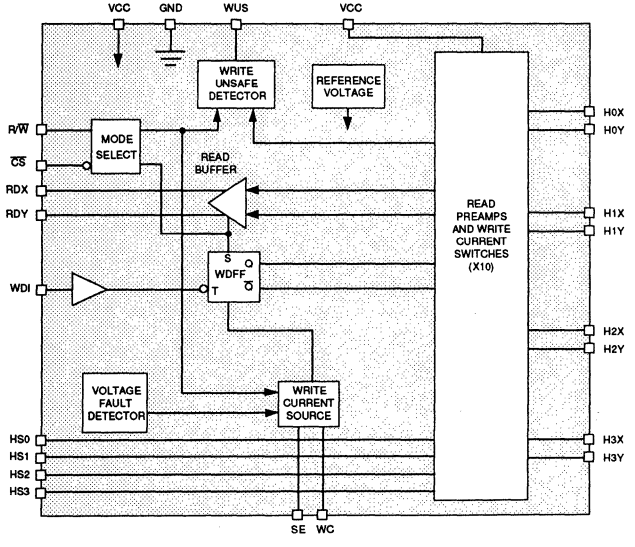
All versions provide multiple channel write capability to assist in servo writing operations. The 2063 device provides ECL write data input, with Servo Bank write selected by a TTL pin ($\overline{SE}$). The 2064 device provides TTL write data input, with servo write selected by a TTL pin ($\overline{SE}$). The 2065 device provides TTL write data input, with servo write selected by bringing the WUS/SE pin above VCC.

The SSI 32R2063/64/65 require only +5V power supplies and is available in a variety of packages.

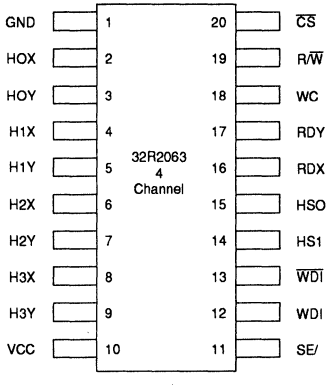
## FEATURES

- **+5V ±10% supply**
- **Low power**
  - **PD = 160 mW read mode (Nom)**
  - **PD = 5 mW idle (Max)**
- **High Performance:**
  - **Read mode gain = 200 V/V**
  - **Input noise = 0.56 nV/√Hz (Nom)**
  - **Input capacitance = 16 pF (Nom)**
  - **Write current range = 5 - 40 mA**
- **Multiple channel write capability**
- **Designed for two-terminal thin-film or MIG heads with inductance up to 5.0 µH**
- **Write unsafe detection**
- **Power supply fault protection**
- **Head short to ground protection**

## BLOCK DIAGRAM




## PIN DIAGRAM



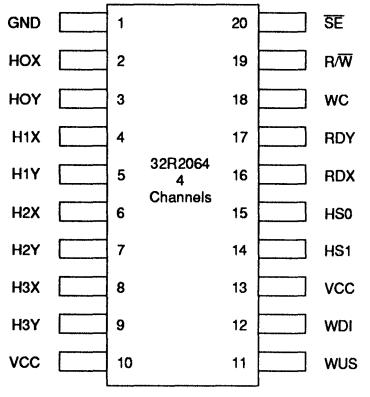

**20-LEAD SOL, VSOP**

CAUTION: Use handling procedures necessary for a static sensitive component.

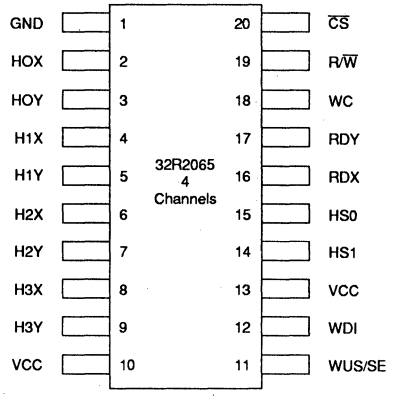
# SSI 32R2063/2064/2065
# 5V, 4-Channel
# Thin-Film Read/Write Device

## PACKAGE PIN DESIGNATIONS

(Top View)




**20-LEAD SOL, VSOP**




**20-LEAD SOL, VSOP**

**Target Specification:** The target specification is intended as an initial disclosure of specification goals for the product. The specifications are based on design goals, subject to change and are not guaranteed.



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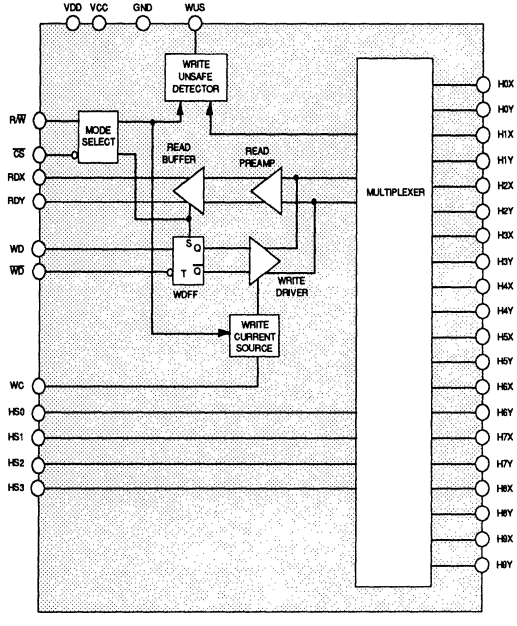
# SSI 32R2100R
## 10-Channel Two Terminal Thin-Film Read/Write Device
## Target Specification

January 1993

## DESCRIPTION

The SSI 32R2100R is a BiCMOS monolithic integrated circuit designed for use with two-terminal recording heads. It is intended for use in hard disk drive designs which require data rates exceeding 48 Mb/sec. It provides a low noise read amplifier, write current control, and data protection circuitry for 10 channels. The SSI 32R2100R provides internal 320Ω damping resistors that are switched in during Write mode and switched out during Read mode. Power supply fault protection is provided by disabling the write current during power sequencing. System write-to-read recovery time is significantly improved by controlling the read channel common mode output voltage shift in the Write mode. The device provides the user with a controllable write-current adjustment feature with a current gain of 20x. The device also provides a multiple channel "servo bank write" capability which is useful during servo writing.

## BLOCK DIAGRAM



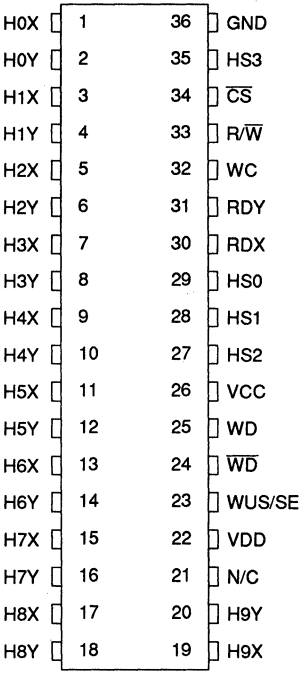

## FEATURES

- **+5V, +12V ±10% supply**
- **Low power**
  - **PD = 200 mW read mode (Nom)**
  - **PD = 1.0 mW idle (Max)**
- **High Performance:**
  - **Read mode gain = 250 V/V**
  - **Input noise = 0.45 nV/√Hz (Nom)**
  - **Input capacitance = 12 pF (Nom)**
  - **Write current range = 5-40 mA**
  - **Max write current rise/fall time = 7 nsec (typ. head)**
  - **Head voltage swing = 10Vpp (min)**
- **Servo bank-write capability**
- **Unselected heads are at GND potential**
- **Self-switching damping resistance**
- **Designed for two-terminal thin-film or MIG heads with inductance up to 1.0 μH**
- **Write unsafe detection**
- **Power supply fault protection**
- **Head short to ground protection**
- **Differential ECL-like write data input**
- **36-Lead SOM package**

# SSI 32R2100R
# 10 Channel Two Terminal Thin-Film Read/Write Device

## PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.




**36-Lead SOM**

**Target Specification:** The target specification is intended as an initial disclosure of specification goals for the product. The specifications are based on design goals, subject to change and are not guaranteed.



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# SSI 32R2200R/2201R
## 5V 4-Channel Thin-Film Read/Write Device
## Target Specification

January 1993

## DESCRIPTION

The SSI 32R2200R/2201R is a BiCMOS monolithic integrated circuit designed for use with two-terminal recording heads. It provides a low noise read amplifier, write current control, and data protection circuitry for 4 channels. The device provides internal 320 Ω damping resistors that are switched in during Write mode and switched out during Read mode. Power supply fault protection is provided by disabling the Write Current generator during power sequencing. System write-to-read recovery time is significantly improved by controlling the read channel common mode output voltage shift in the Write mode. The device provides the user with a controllable Write-Current adjustment feature with a current gain of 20x. The device also provides a multiple channel "servo bank write" capability which is useful during servo writing.

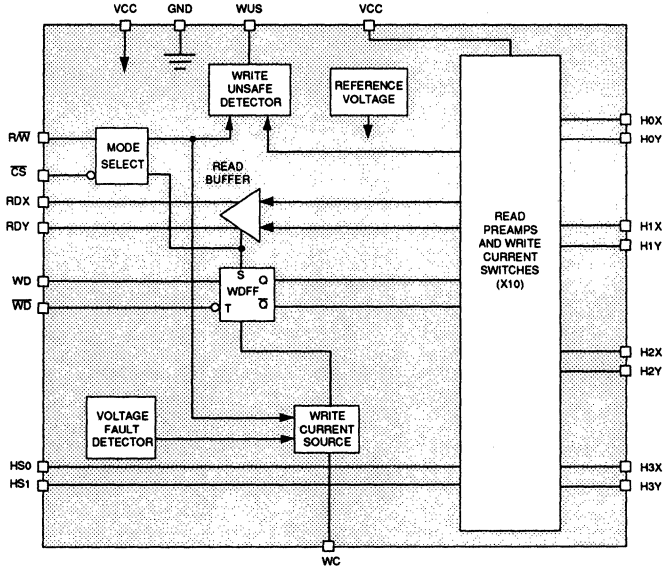
The SSI 32R2200R requires only +5V power supplies and is available in a variety of packages. It provides differential ECL - like write data input. The SSI 32R2201R provides TTL write data input. It is hardware compatible with the SSI 32R2020R Read/Write device.

## FEATURES

- **+5V ±10% supply**
- **Low power**
  - **PD = 150 mW Read mode (Nom)**
  - **PD = 0.5 mW Idle (Max)**
- **High Performance:**
  - **Read mode gain = 250 V/V**
  - **Input noise = 0.45 nV/√Hz (Nom)**
  - **Input capacitance = 12 pF (Nom)**
  - **Write current range = 3-35 mA**
  - **Max write current rise/fall time = 9 nsec (typical head)**
  - **Head voltage swing = 6 Vpp min**
- **Servo bank-write capability**
- **Unselected heads are at GND potential**
- **Self switching damping resistance**

(continued)

## BLOCK DIAGRAM



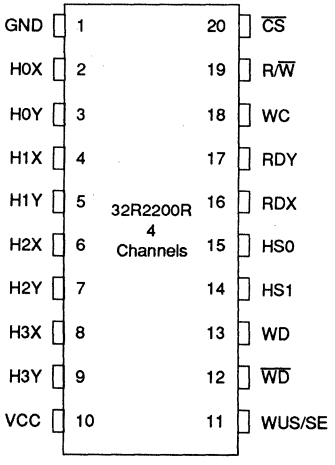
# SSI 32R2200R/2201R
# 5V 4-Channel
# Thin-Film Read/Write Device

## FEATURES (continued)

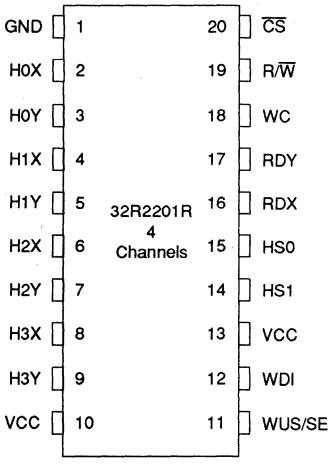
- Designed for two-terminal thin-film or MIG heads with inductance up to 1.5 μH
- Write unsafe detection
- Power supply fault protection
- Head short to ground protection
- Differential ECL-like (32R2200R) or TTL (32R2201R) write data inputs
- Available in 24-Lead SOL, SOV package

## PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.




20-Lead SOV, SOL




20-Lead SOV, SOL

**Target Specification:** The target specification is intended as an initial disclosure of specification goals for the product. The specifications are based on design goals, subject to change and are not guaranteed.



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# SSI 32R2300/2300R/2301/2301R
## +3.3V/5.0V, 2, 4-Channel 2-Terminal Read/Write Device

**Advance Information**

December 1992

## DESCRIPTION

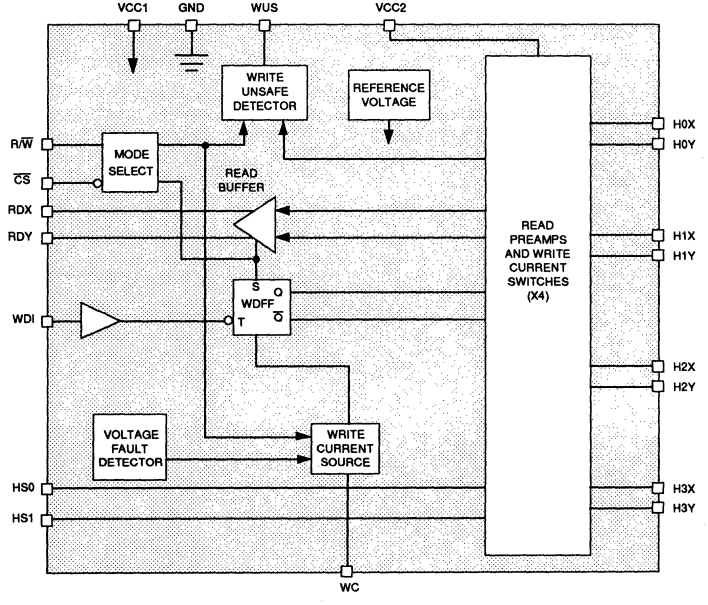
The SSI 32R2300/2300R are BiCMOS monolithic integrated circuits designed for use with two-terminal recording heads. They provide a low noise read amplifier, write current control, and data protection circuitry for up to four channels. The SSI 2300R option provides internal 350Ω damping resistors. Damping resistors are switched in during Write mode and switched out during Read mode. The SSI 32R2300 option does not provide a damping resistor. Power supply fault protection is provided by disabling the write current generator during power sequencing. System write to read recovery time is significantly improved by making the read channel outputs high impedance.

The SSI 32R2300/2300R require only a +3.3V power supply and are available in a variety of packages. They are hardware compatible with the SSI 32R4610A and SSI 32R2020R Read/Write devices. The SSI 32R2301/2301R is identical to the SSI 32R2300/2300R, but comes in 24-pin package.

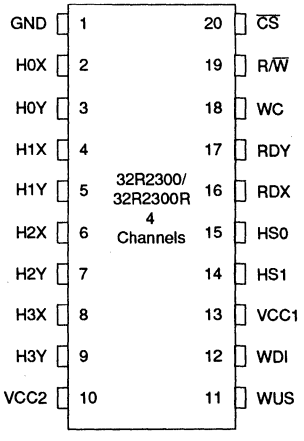
## FEATURES

- **+3.0V - 5.5V voltage supply**
- **Low power**
  - **PD = 63 mW read mode (Nom) (@3.3V supply)**
  - **PD = 1 mW idle (Max)**
- **High Performance:**
  - **Read mode gain = 200 V/V**
  - **Input noise = 0.50 nV/√Hz (Nom)**
  - **Input capacitance = 9 pF (Nom)**
  - **Write current range = 3-25 mA**
- **Self switching damping resistance**
- **Pin compatible with the SSI 32R4610AR and SSI 32R2020R**
- **Write unsafe detection**
- **Power supply fault protection**

## BLOCK DIAGRAM




## PIN DIAGRAM




**20-Lead SOL**

CAUTION: Use handling procedures necessary for a static sensitive component.

# SSI 32R2300/2300R/2301/2301R
# +3.3V/5.0V, 2, 4-Channel
# 2-Terminal Read/Write Device

## CIRCUIT OPERATION

The SSI 32R2300/2300R have the ability to address up to 4 two-terminal heads and provide write drive or read amplification. Mode control and head selection are described in Tables 1 and 2. The TTL inputs R/$\overline{W}$, $\overline{CS}$, HS0 and HS1 have internal pull-up resistors.

**TABLE 1: Mode Select**

| $\overline{CS}$ | R/$\overline{W}$ | Mode |
|---|---|---|
| 0 | 0 | Write |
| 0 | 1 | Read |
| 1 | 0 | Idle |
| 1 | 1 | Idle |

**TABLE 2: Head Select**

| HS1 | HS0 | Head |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 2 |
| 1 | 1 | 3 |

## PIN DESCRIPTIONS

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| HS0, HS1 † | I | Head Select: selects one of four heads |
| $\overline{CS}$ | I | Chip Select: a high inhibits the chip |
| R/$\overline{W}$ † | I | Read/Write : a high selects Read mode |
| WUS † | O | Write Unsafe: a high indicates an unsafe writing condition |
| WDI † | I | Write Data In: a negative transition on WDI changes the direction of the current in the recording head |
| H0X - H3X; H0Y - H3Y | I/O | X, Y Head Connections |
| RDX, RDY † | O | X, Y Read Data: differential read data output |
| WC | | Write Current: used to set the magnitude of the write current |
| VCC1 | I | Power Supply |
| VCC2 | I | Power Supply for Write current drivers |
| GND | I | Ground |

† When more that one R/W device is used, signals can be wire OR'ed

### WRITE MODE

Taking both $\overline{CS}$ and R/$\overline{W}$ low selects write mode which configures the SSI 32R2300/2300R as a current switch and activates the Write Unsafe (WUS) detector circuitry. Head current is toggled between the X and Y side of the selected head on each high to low transition of the Write Data Input (WDI). Note that a preceding Read to Write transition or Idle to Write transition initializes the Write Data Flip-Flop to pass write current into the "X" side of the device. In this case, the Y side is higher potential than the X side. The magnitude of the write current (0-pk) is given by:

$$Iw = Aw \cdot \frac{Vwc}{Rwc} = K/Rwc$$

where Aw is the write current gain.
RWC is connected from pin WC to GND. Note the actual head current Ix, y is given by:

$$Ix, y = \frac{Iw}{1 + Rh/Rd}$$

Where:

Rh = Head resistance plus external wire resistance
Rd = Damping resistance

In Write mode a 350 Ω damping resistor is switched in across the Hx, Hy ports (32R2300R only).

### VOLTAGE FAULT

A voltage Fault detection circuit improves data security by disabling the write current generator during a voltage fault or power startup in Read or Write mode.

### WRITE UNSAFE

Any of the following conditions will be indicated as a high level on the Write Unsafe, WUS, open collector output.

- WDI frequency too low
- Device in Read mode
- Device not selected
- No head current
- Open head
- Head short to ground

WUS is valid in the write current/head characteristic region defined by $5 < Ih \cdot Lh < 50$ mA • µH, and $1 < Rh < 1.25/Ih$. After the fault condition is removed, two negative transitions on WDI are required to clear WUS. Overcurrent protection during a head short to ground is accomplished by placing a series resistor between VCC1 and VCC2. The write current driver will shut down when VCC1 - VCC2 ≥ 0.3V. The resistor must be sized so that VCC1 - VCC2 ≤ 0.15V in normal operation.

### READ MODE

The Read mode configures the SSI 32R2300/2300R as a low noise differential amplifier and deactivates the write current generator. The damping resistor is switched out of the circuit allowing a high impedance input to the read amplifier. The RDX and RDY output are driven by emitter followers. They should be AC coupled to the load. The HnX, HnY inputs are non-inverting to the RDX, RDY outputs.

Note that in Idle or Write mode, the read amplifier is deactivated and RDX, RDY outputs become high impedance. This facilitates multiple R/W applications (wired-OR RDX, RDY) and minimizes voltage change when switching from Write to Read mode. Note also that the write current source is deactivated for both the Read and Idle mode.

### IDLE MODE

Taking $\overline{CS}$ high selects the Idle mode which switches the RDX and RDY outputs into a high impedance state and deactivates the device. Power consumption in this mode is held to a minimum.

## ELECTRICAL SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may permanently damage the device.

| PARAMETER | | RATING |
|---|---|---|
| DC Supply Voltage | VCC1 | -0.3 to +6 VDC |
| | VCC2 | -0.3 to +6 VDC |
| Write Current | Iw | 30 mA |
| Digital Input Voltage | Vin | -0.3 to VCC1 +0.3 VDC |
| Head Port Voltage | VH | -0.3 to VCC2 +0.3 VDC |
| Output Current: RDX, RDY | I0 | -10 mA |
| | WUS | +8 mA |
| Storage Temperature | Tstg | -55 to +150°C |

### RECOMMENDED OPERATING CONDITIONS

| PARAMETER | | RATING |
|---|---|---|
| DC Supply Voltage | VCC1 = VCC2 | 3.3 ±10%, 5.0 ±10% VDC |
| Recommended Head Load Range | Lh | 0.3 - 5.0 µH |
| WUS Operating Range | Iw • Lh | 5.0 - 50.0 mA • µH |
| Head Differential Load Capacitance | | 25 pF max |
| Ambient Operating Temperature | | 0 - 70 °C |

### DC CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified.

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| VCC1 Supply Current | Read Mode Vcc = 3.3V ±10% | | 19 | 29 | mA |
| | Write Mode Vcc = 3.3V ±10% | | 2 + 0.2 Iw | 3 + 0.3 Iw | mA |
| | Idle Mode Vcc = 3.3V ±10% | | 0.15 | 0.27 | mA |
| VCC2 Supply Current | Read Mode Vcc = 3.3V ±10% | | - | 0.1 | mA |
| | Write Mode Vcc = 3.3V ±10% | | 1.0 + Iw | 3.0 + Iw | mA |
| | Idle Mode Vcc = 3.3V ±10% | | - | 0.01 | mA |
| Power Dissipation | Read Mode Vcc = 3.3V ±10% | | 63 | 105 | mW |
| | Write Mode Vcc = 3.3V ±10% | | 10 + 4 • Iw | 20 + 5 • Iw | mW |
| | Idle Mode Vcc = 3.3V ±10% | | 0.5 | 1 | mW |
| VCC1 Supply Current | Read Mode Vcc = 5.0V ±10% | | 20 | 32 | mA |
| | Write Mode Vcc = 5.0V ±10% | | 3 + 0.2 Iw | 5 + 0.3 Iw | mA |
| | Idle Mode Vcc = 5.0V ±10% | | 0.25 | 0.45 | mA |
| VCC2 Supply Current | Read Mode Vcc = 5.0V ±10% | | | 0.1 | mA |
| | Write Mode Vcc = 5.0V ±10% | | 1.0 + Iw | 3.0 + Iw | mA |
| | Idle Mode Vcc = 5.0V ±10% | | | 0.01 | mA |
| Power Dissipation | Read Mode Vcc = 5.0V ±10% | | 100 | 180 | mW |
| | Write Mode Vcc = 5.0V ±10% | | 20 + 6 • Iw | 45 + 7.2 Iw | mW |
| | Idle Mode Vcc = 5.0V ±10% | | 1.25 | 2.5 | mW |

### DIGITAL INPUTS

| | | | | | | |
|---|---|---|---|---|---|---|
| Input Low voltage (VIL) | | | | | 0.8 | VDC |
| Input High Voltage (VIH) | | | 2.0 | | | VDC |
| Input Low Current | VIL = 0.4 | VCC = 3.6V | -0.4 | -.09 | | mA |
| | | VCC = 5.5V | -0.4 | -0.13 | | mA |
| Input High Current | VIH = 2.7V | | | 0 | 20 | µA |
| WUS Output Low Voltage (VOL) | Iol = 2 mA max | | | .35 | 0.5 | VDC |

**WRITE CHARACTERISTICS**

Recommended operating conditions apply unless otherwise specirfied.

| PARAMETER | CONDITIONS | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| VCC1 Fault Voltage | Iw < 0.2 mA | | | 2.5 | 2.75 | VDC |
| Write Current Gain (Aw) | Iw = 3 mA to 20 mA | | 18.4 | 20 | 21.6 | mA/mA |
| Write Current Gain (Aw) | Iw = 20 mA to 25 mA | | 17.0 | 20 | 23 | mA/mA |
| Write Current Voltage (VWC) | | | 1.2 | 1.3 | 1.4 | V |
| Differential Head Voltage Swing | Open head | | 4.0 | 4.8 | | Vpp |
| Unselected Head Current | Iw ≥ 10 mA | | | | 0.02 Iw | mA (pk) |
| | Iw < 10 mA | | | | 0.2 | mA (pk) |
| Head Differential Load | | 32R2300 | 2400 | 3000 | 3600 | Ω |
| Resistance (Rd) | | 32R2300R | 250 | 350 | 450 | Ω |
| WDI Pulse Width | Vil ≤ 0.8V, Vih ≥ 2.0V | PWH | 5 | | | ns |
| | $t_f = t_r$ = 1ns | PWL | 10 | | | ns |
| Write Current Range (Iw) | | | 3 | | 25 | mA |

**READ CHARACTERISTICS**

Recommended operating conditions apply unless otherwise specified. CL (RDX, RDY) < 20 pF, RL (RDX, RDY) = 1 kΩ.

| | | | | | | |
|---|---|---|---|---|---|---|
| Differential Voltage Gain | | Vin = 1 mVpp @1 MHz | 160 | 200 | 240 | V/V |
| Voltage BW | -1dB | \|Zs\| < 5Ω, Vin = 1 mVpp | 20 | 35 | | MHz |
| | -3dB | | 40 | 70 | | MHz |
| Input Noise Voltage | | BW = 15 MHz, Lh = 0, Rh = 0 | | 0.50 | 0.75 | nV/√Hz |
| Input Noise Current | | | | 3 | | pA/√Hz |
| Differential Input Capacitance | | Vin = 1 mVpp, f = 5 MHz | | 9 | 14 | pF |
| Differential Input Resistance | | Vin = 1 mVpp, f = 5 MHz | | | | |
| | | 32R2300 | 500 | 750 | 1800 | Ω |
| | | 32R2300R | 500 | 750 | 1800 | Ω |
| Dynamic Range | | AC input voltage where gain falls to 90% of its small signal gain value, f = 5 MHz | 2 | 5 | | mVpp |
| Common Mode Rejection Ratio | | Vin = 0 VDC + 100 mVpp @ 5 MHz | 45 | 60 | | dB |
| Power Supply Rejection Ratio | | 100 mVpp @ 5 MHz on VCC | 40 | 70 | | dB |
| Channel Separation | | Unselected channels driven with Vin = 0 VDC + 100 mVpp | 45 | 60 | | dB |
| Output Offset Voltage | | | -200 | | +200 | mV |
| Single Ended Output Resistance | | f = 5 MHz | | 60 | 100 | Ω |
| Output Current | | AC coupled load, RDX to RDY | 1.0 | 2.0 | | mA |
| RDX, RDY Common Mode Output Voltage | | | Vcc-1.0 | Vcc-1.35 | Vcc-1.70 | VDC |

**SWITCHING CHARACTERISTICS**

Recommended operating conditions apply unless otherwise specified. IW = 15 mA, Lh = 1.0 µH, Rh = 30Ω $f$(Data) = 5 MHz.

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| R/$\overline{W}$ | Read to Write | R/$\overline{W}$ to 90% of write current | | 0.3 | 1.0 | µs |
| | Write to Read | R/$\overline{W}$ to 90% of 100 mV Read signal envelope | | 0.4 | 1 | µs |
| $\overline{CS}$ | Unselect to Select | $\overline{CS}$ to 90% of 100 mV 10 MHz Read signal envelope | | 0.6 | 2 | µs |
| | Select to Unselect | $\overline{CS}$ to 10% of write current | | 0.1 | 1 | µs |
| HS0,1 to any Head | | To 90% of 100 mV 10 MHz Read signal envelope | | 0.2 | 1 | µs |
| WUS* | Safe to Unsafe (TD1) | Write mode, loss of WDI transitions; Defines max WDI period for WUS operation | 0.6 | 2.0 | 3.6 | µs |
| | Unsafe to Safe (TD2) | Fault cleared: from second negative WDI transition | | 0.2 | 1.0 | µs |
| WDI | Frequency Range | Valid WUS | 1.67 | | 25 | MHz |
| Head Current | | Lh = 0, Rh = 0 | | | | |
| | WDI to Ix - Iy (TD3) | from 50% points | | 25 | 40 | ns |
| | Asymmetry | WDI has 1 ns rise/fall time | | | 1.5 | ns |
| | Rise/fall Time | 10% to 90% points | | | | |
| | | Iw = 15 mA, Rh = 0, Lh = 0 | | 6 | 9 | ns |
| | | Iw = 15 mA, Rh = 30Ω, Lh = 1µH | | 14 | 18 | ns |
| * 5 < Iw • Lh < 50 mA • µH, 1 < Rh ≤ 1.25/Iw | | | | | | |

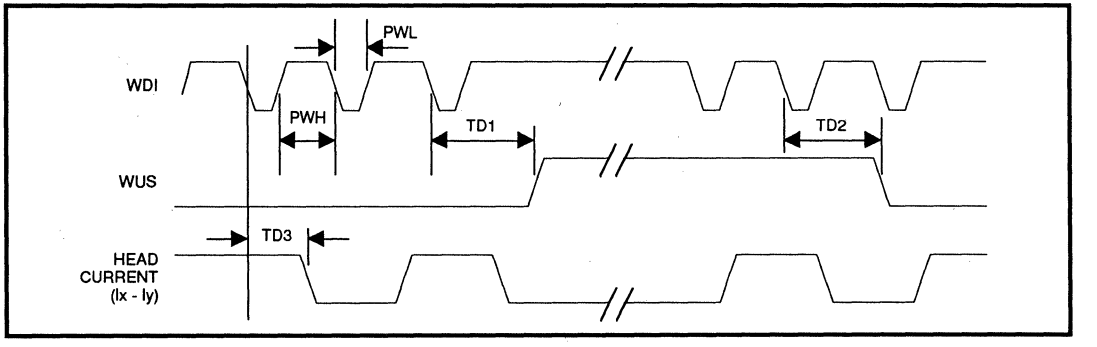



**FIGURE 1: Write Mode Timing Diagram**

Worst Case Read Input Noise Voltage vs. Input Impedance for SSI 32R2300R

Case 1: IC Base sheet resistance = Maximum
Hence, IC bias current = Minimum

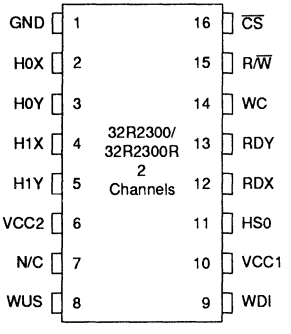
| | Tj = 25°C | Tj = 110°C | Units |
|---|---|---|---|
| Vn (Max) | TBD | TBD | $nV/\sqrt{Hz}$ |
| Rin (Min) | TBD | TBD | Ω |
| Cin (Max) | TBD | TBD | pF |

Case 2: IC Base sheet resistance = Minimum
Hence, IC bias current = Maximum

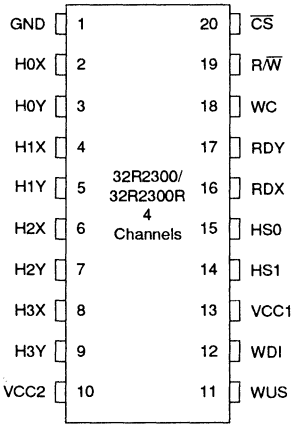
| | Tj = 25°C | Tj = 110°C | Units |
|---|---|---|---|
| Vn (Max) | TBD | TBD | $nV/\sqrt{Hz}$ |
| Rin (Min) | TBD | TBD | Ω |
| Cin (Max) | TBD | TBD | pF |

## PACKAGE PIN DESIGNATIONS

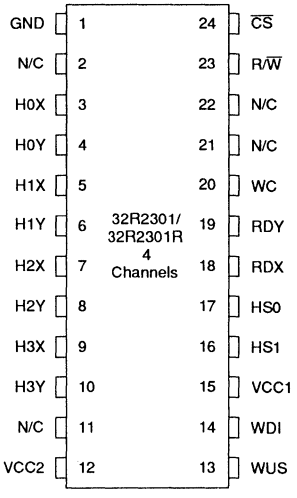
(Top View)




**16-Lead SOL, SON**




**20-Lead SOL, VSOP**




**24-Lead SOL, VSOP**

**Advance Information:** Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.



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**Notes:**

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# SSI 32R2310/2310R
## +3.3V/5.0V, 2, 4-Channel 2-Terminal Read/Write Device
## Target Specification

January 1993

## DESCRIPTION

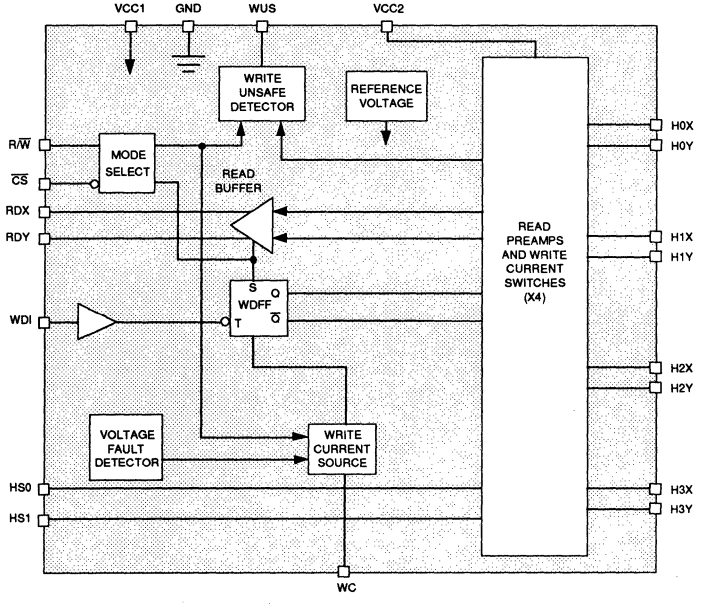
The SSI 32R2310/2310R are BiCMOS monolithic integrated circuits designed for use with two-terminal recording heads. They provide a low noise read amplifier, write current control, and data protection circuitry for up to four channels. The SSI 32R2310R option provides internal 350Ω damping resistors. Damping resistors are switched in during Write mode and switched out during Read mode. The SSI 32R2310 option does not provide a damping resistor. Power supply fault protection is provided by disabling the write current generator during power sequencing. System write to read recovery time is significantly improved by making the read channel outputs high impedance.

The SSI 32R2310/2310R require only a +3.3V power supply and are available in a variety of packages. They are identical to the SSI 32R2300/2300R devices, except that the $\overline{CS}$ input is CMOS. This allows for lower idle mode power dissipation.

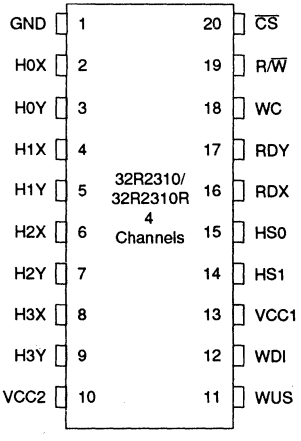
## FEATURES

- **+3.0V - 5.5V voltage supply**
- **Low power**
  - **PD = 63 mW read mode (Nom) (@3.3V supply)**
  - **PD = 200 μW (Max) Idle Mode**
- **High Performance:**
  - **Read mode gain = 200 V/V**
  - **Input noise = 0.50 nV/√Hz (Nom)**
  - **Input capacitance = 9 pF (Nom)**
  - **Write current range = 3-25 mA**
  - **Head voltage swing = 4.0 Vpp min**
- **Self switching damping resistance**
- **Pin compatible with the SSI 32R2300/2300R**
- **Write unsafe detection**
- **Power supply fault protection**

## BLOCK DIAGRAM




## PIN DIAGRAM




**20-Lead SOL**

CAUTION: Use handling procedures necessary for a static sensitive component.

# SSI 32R2310/2310R
# +3.3V/5.0V, 2, 4-Channel
# 2-Terminal Read/Write Device

**Target Specification:** The target specification is intended as an initial disclosure of specification goals for the product. The specifications are based on design goals, subject to change and are not guaranteed.



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# SSI 32R4610A/4611A
5V, 2, 4, 8-Channel Thin-Film
# SSI 32R4610B
5V, 8 Channel Thin-Film
Read/Write Device

December 1992

## DESCRIPTION

The SSI 32R4610A/4611A and SSI 32R4610B are bipolar monolithic integrated circuits designed for use with two-terminal thin- film recording heads. They provide a low noise read amplifier, write current control, and data protection circuitry for up to eight channels. The SSI 32R4610AR/4611AR option provides internal 700Ω damping resistors. Power supply fault protection is provided by disabling the write current generator during power sequencing. System write to read recovery time is significantly improved by controlling the read channel common mode output voltage shift in the Write mode. The 32R4611A option provides for an additional feature providing the user with a controllable write current adjustment feature.

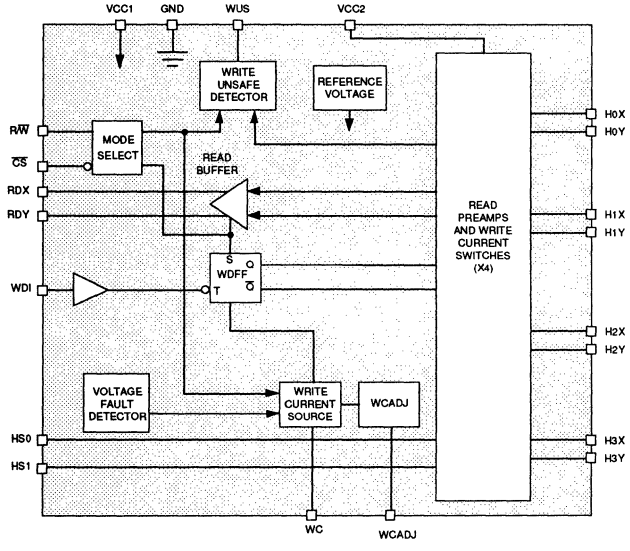
The SSI 32R4610B is an 8 channel device which improves the write unsafe performance over the SSI 32R4610A-8. In all other areas, performance is identical to the SSI 32R4610A-8.

The SSI 32R4610/4611 and SSI 32R4610B require only +5V power supplies and are available in a variety of packages.

## FEATURES

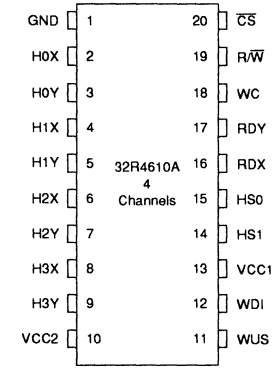
- **5V ±10%**
- **Low power**
  - **PD = 175 mW read mode (Nom)**
- **High Performance:**
  - **Read mode gain = 200 V/V**
  - **Input noise = 0.85 nV/√Hz max**
  - **Input capacitance = 35 pF max**
  - **Write current range = 10-35 mA**
- **Designed for two-terminal thin-film heads**
- **Programmable write current source**
- **Write unsafe detection**
- **Enhanced system write to read recovery time**
- **Power supply fault protection**
- **Head short to ground protection**

## BLOCK DIAGRAM




WCADJ available on the 32R4611A 24-pin option only

## PIN DIAGRAM




**20-PIN SOL**

CAUTION: Use handling procedures necessary for a static sensitive component.

## CIRCUIT OPERATION

The SSI 32R4610A/4611A and SSI 32R4610B have the ability to address up to 8 two-terminal thin-film heads and provide write drive or read amplification. Head selection and mode control are described in Tables 2 and 3. The TTL inputs R/$\overline{W}$ and $\overline{CS}$ have internal pull-up resistors to prevent an accidental write condition. HS0, HS1 and HS2 have internal pulldowns. Internal clamp circuitry will protect the IC from a head short to ground condition in any mode.

**TABLE 1: Mode Select**

| $\overline{CS}$ | R/$\overline{W}$ | Mode |
|---|---|---|
| 0 | 0 | Write |
| 0 | 1 | Read |
| 1 | 0 | Idle |
| 1 | 1 | Idle |

**TABLE 2: Head Select**

| HS2 | HS1 | HS0 | Head |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 2 |
| 0 | 1 | 1 | 3 |
| 1 | 0 | 0 | 4 |
| 1 | 0 | 1 | 5 |
| 1 | 1 | 0 | 6 |
| 1 | 1 | 1 | 7 |

## PIN DESCRIPTION

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| HS0, HS1, HS2 † | I | Head Select: selects one of four heads |
| $\overline{CS}$ | I | Chip Select: a high inhibits the chip |
| R/$\overline{W}$ † | I | Read/Write : a high selects Read mode |
| WUS † | O | Write Unsafe: a high indicates an unsafe writing condition |
| WDI † | I | Write Data In: changes the direction of the current in the recording head |
| H0X - H7X;<br>H0Y - H7Y | I/O | X, Y Head Connections |
| RDX, RDY † | O | X, Y Read Data: differential read data output |
| WC † | | Write Current: used to set the magnitude of the write current |
| WCADJ* † | | Write Current Adjust: Used to decrease the write current by a finite amount |
| VCC1 | I | +5V Supply |
| VCC2 | I | +5V Supply for Write current drivers |
| GND | I | Ground |
| *Available on 32R4611A 24-pin option only<br>† These signals can be wire OR'ed | | |

### WRITE MODE

Taking both $\overline{CS}$ and R/$\overline{W}$ low selects Write mode which configures the SSI 32R4610A/4611A and SSI 32R4610B as a current switch and activates the Write Unsafe (WUS) detector circuitry. Head current is toggled between the X and Y side of the selected head on each high to low transition of the Write Data Input (WDI). The WDI input pulse width requirement is amplitude dependent and pull ups are recommended at higher data rates, please refer to the WDI pulse width specifications. Note that a preceding Read or Idle mode select initializes the Write Data Flip-Flop to pass write current through the "X" side of the head. The magnitude of the write current (0-pk) is given by:

$$IW = \frac{K \cdot VWC}{RWC}$$

RWC is connected from pin WC to GND. Note the actual head current Ix, y is given by:

$$Ix, y = \frac{Iw}{1 + Rh/Rd}$$

Where:

Rh = Head resistance plus external wire resistance

Rd = Damping resistance

### WUS

Any of the following conditions will be indicated as a high level on the Write Unsafe, WUS, open collector output.

- WDI frequency too low
- Device in Read mode
- Chip disabled
- No write current
- Head opened*

After fault condition is removed, one negative transition on WDI is required to clear WUS.

*Open head detect is not always detected on the SSI 32R4610A-8. This circuit is improved in the SSI 32R4610B-8.

### WCADJ

The 32R4611A adds a feature which allows the user to adjust the Iw current by a finite amount. The WCADJ pin is used to adjust write current for write operations on different zones of the disk. It is used by switching a separate write current adjust resistor in and out on the WCADJ pin or by connecting a DAC to that pin to sink a controllable amount of current. The WCADJ pin is nominally biased to VCC/2. Sinking current from this pin to ground will divert a proportional amount of current from the actual head current while maintaining a constant current through the WC resistor and VCC. Allowing WCADJ to float or pulling it high will cut off the circuit and it will have no effect. For example, if the nominal head current is set to 30 mA through WC with WCADJ open, then for a 7.25 mA head current decrease, a 10 kΩ resistor would be connected from the WCADJ pin to ground. A TTL gate could be used as a switch with a small degradation in accuracy. To perform the same function, a DAC could be used, by programming it to sink 0.25 mA from the WCADJ pin.

Iw head (Decrease) = (29 • $V_{WCADJ}$ / $R_{WCADJ}$)

Where:

VWCADJ = Voltage on WCADJ pin = VCC/2

RWCADJ = Write current adjust setting resistor

### VOLTAGE FAULT

A voltage fault detection circuit improves data security by disabling the write current generator during a voltage fault or power startup regardless of mode.

### READ MODE

The Read mode configures the SSI 32R4610A/4611A and SSI 32R4610B as a low noise differential amplifier and deactivates the write current generator. The RDX and RDY output are driven by emitter followers. They should be AC coupled to the load. The (X,Y) inputs are non-inverting to the (X,Y) outputs.

Note that in Idle or Write mode, the read amplifier is deactivated and RDX, RDY outputs become high impedance. This facilitates multiple R/W applications (wired-OR RDX, RDY) and minimizes voltage drifts when switching from Write to Read mode. Note also that the write current source is deactivated for both the Read and Idle mode.

### IDLE MODE

Taking $\overline{CS}$ high selects the Idle mode which switches the RDX and RDY outputs into a high impedance state and deactivates the device. Power consumption in this mode is held to a minimum.

## ELECTRICAL SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may permanently damage the device.

| PARAMETER | | RATING | UNIT |
|---|---|---|---|
| DC Supply Voltage | VCC1 | -0.3 to +7 | VDC |
| | VCC2 | -0.3 to +7 | VDC |
| Write Current | IW | 80 | mA |
| Digital Input Voltage | Vin | -0.3 to VCC1 +0.3 | VDC |
| Head Port Voltage | VH | -0.3 to VCC2 +0.3 | VDC |
| Output Current: RDX, RDY | I0 | -10 | mA |
| WUS | | +12 | mA |
| Storage Temperature | Tstg | -65 to +150 | °C |

### RECOMMENDED OPERATING CONDITIONS

| | | | |
|---|---|---|---|
| DC Supply Voltage | VCC1 | 5 ±10% | VDC |
| | VCC2 | 5 ±10% | VDC |
| Operating Junction Temperature | Tj | +25 to +110 | °C |

### DC CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified.

| PARAMETER | CONDITIONS | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| VCC1 Supply Current | Read Mode | (Vcc ±5%) | 23 | 28 | 33 | mA |
| | | (Vcc ±10%) | 19 | 28 | 37 | mA |
| | Write Mode | (Vcc ±5%) | 21 | 24 | 27 | mA |
| | | (Vcc ±10%) | 17 | 24 | 31 | mA |
| **Head Select Pins* | *Idle Mode | (Vcc ±5%) | 6 | 9 | 12 | mA |
| *(HS0, HS1, HS2) Floating* | | (Vcc ±10%) | 4 | 9 | 14 | mA |
| VCC2 Supply Current | Read Mode | (Vcc ±5%) | 5 | 8 | 11 | mA |
| | | (Vcc ±10%) | 4 | 8 | 12 | mA |
| | Write Mode | (Vcc ±5%) | 6 | 8 + Iw | 10 + Iw | mA |
| | | (Vcc ±10%) | 5 | 8 + Iw | 11 + Iw | mA |
| | Idle Mode | (Vcc ±5%) | 0.1 | 0.2 | 0.4 | mA |
| | | (Vcc ±10%) | 0.1 | 0.2 | 0.5 | mA |
| Power Dissipation | Read Mode | (Vcc ±5%) | | 175 | 230 | mW |
| | | (Vcc ±10%) | | | 270 | mW |

**DC CHARACTERISTICS** (Continued)

| PARAMETER | CONDITIONS | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| | Write Mode | (Vcc ±5%) | | 150 + 4Iw | 190 + 4Iw | mW |
| | | (Vcc ±10%) | | | 230 + 4.4Iw | mW |
| | Idle Mode | (Vcc ±5%) | | 50 | 65 | mW |
| | | (Vcc ±10%) | | | 80 | mW |
| VCC1 Fault Voltage | IW < 0.2 mA | | 3.8 | 4.0 | 4.2 | VDC |

**DIGITAL INPUTS**

| | | | | | |
|---|---|---|---|---|---|
| Input Low voltage (VIL) | | | | 0.8 | VDC |
| Input High Voltage (VIH) | | 2.0 | | | VDC |
| Input Low Current | VIL = 0.8V | -0.4 | | | mA |
| Input High Current | VIH = 2.0V | | | 100 | µA |
| WUS Output Low Voltage (VOL) | Iol = 2 mA max | | | 0.5 | VDC |

**WRITE CHARACTERISTICS**

Recommended operating conditions apply unless otherwise specified.

| | | | | | |
|---|---|---|---|---|---|
| Write Current Constant "K" | | .96 | .99 | | |
| Write Current Voltage (VWC) | | 1.15 | 1.25 | 1.35 | V |
| WCADJ Voltage SSI 32R4611A/4611AR | $I_{WCADJ}$ = 0 to .5 mA | 2.0 | VCC/2 | 3.0 | VDC |
| Ihead(Decrease)/$I_{WCADJ}$ SSI 32R4611A/4611AR | | 26 | 29 | 32 | mA/mA |
| $I_{WCADJ}$ Range SSI 32R4611A/4611AR | | 0.0 | | 0.5 | mA |
| Differential Head Voltage Swing | Ih (p-p) • Rh not to exceed 3.4V (Head Swing Min) | 3.4 | | | Vpp |
| Unselected Head Current | | | | 0.02 Iw | mApk |
| Head Differential Load Capacitance | | | | 25 | pF |
| Head Differential Load | SSI 32R4610A/32R4611A | 4K | | | Ω |
| Resistance (Rd) | SSI 32R4610AR/32R4611AR | 560 | 700 | 950 | Ω |
| WDI Pulse Width | Vil = 0.2V, Vih = 2.4V PWH | 37 | | | ns |
| (Ref: Figure 1) | PWL | 5 | | | ns |
| | Vil = 0.2V, Vih = VCC PWH | 20 | | | ns |
| | PWL | 5 | | | ns |
| Write Current Range (IW) | | 10 | | 35 | mA |

**READ CHARACTERISTICS**

Recommended operating conditions apply unless otherwise specified. CL (RDX, RDY) < 20 pF, RL (RDX, RDY) = 1 kΩ.

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Differential Voltage Gain | Vin = 1 mVpp @1 MHz | 160 | 200 | 240 | V/V |
| Voltage BW -1dB | \|Zs\| < 5Ω, Vin = 1 mVpp | 20 | 81 | | MHz |
| -3dB | | 35 | 91 | | MHz |
| Input Noise Voltage | BW = 15 MHz, Lh = 0, Rh = 0 | | 0.6 | 0.85 | nV/√Hz |
| Differential Input Capacitance | Vin = 1 mVpp, $f$ = 5 MHz | | 27 | 35 | pF |
| Differential Input Resistance | Vin = 1 mVpp, $f$ = 5 MHz SSI 32R4610A/4611A | 835 | 2600 | | Ω |
| | SSI 32R4610AR/4611AR | 360 | 550 | | Ω |
| Dynamic Range | AC input voltage where gain falls to 90% of its small signal gain value, $f$ = 5 MHz | 3 | 6 | | mVpp |
| Common Mode Rejection Ratio | Vin = 0 VDC + 100 mVpp @ 5 MHz | 45 | 80 | | dB |
| Power Supply Rejection Ratio | 100 mVpp @ 5 MHz on VCC | 40 | 70 | | dB |
| Channel Separation | Unselected channels driven with Vin = 0 VDC + 100 mVpp | 45 | | | dB |
| Output Offset Voltage | | -300 | | +300 | mV |
| Single Ended Output Resistance | $f$ = 5 MHz | | | 40 | Ω |
| Output Current | AC coupled load, RDX to RDY | 1.4 | | | mA |
| RDX, RDY Common Mode Output Voltage | | 2.0 | VCC1/2 | 3.5 | VDC |

**SWITCHING CHARACTERISTICS**

Recommended operating conditions apply unless otherwise specified. IW = 20 mA, Lh = 1.0 µH, Rh = 30Ω $f$(Data) = 5 MHz.

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| R/$\overline{W}$ | Read to Write | R/W to 90% of write current | | 0.1 | 1.0 | µs |
| | Write to Read | R/W to 90% of 100 mV Read signal envelope | | 0.5 | 1.0 | µs |
| $\overline{CS}$ | Unselect to Select | $\overline{CS}$ to 90% of write current or to 90% of 100 mV 10 MHz | | 0.4 | 1.0 | µs |
| | Select to Unselect | $\overline{CS}$ to 10% of write current | | 0.4 | 1.0 | µs |
| HS0,1 to any Head | | To 90% of 100 mV 10 MHz Read signal envelope | | 0.2 | 1.0 | µs |
| WUS: | Safe to Unsafe (TD1) | Write mode, loss of WDI transitions. Defines maximum WDI period for WUS operation | 0.6 | 2.0 | 3.6 | µs |
| | Unsafe to Safe (TD2) | Fault cleared from first neg WDI transition | | 0.2 | 1.0 | µs |
| Head Current: | | Lh = 0, Rh = 0 | | | | |
| | WDI to Ix - Iy (TD3) | from 50% points | | 20 | 32 | ns |
| | Asymmetry | WDI has 1 ns rise/fall time | | | 1.0 | ns |
| | Rise/fall Time | 10% to 90% points | | 6 | 12 | ns |

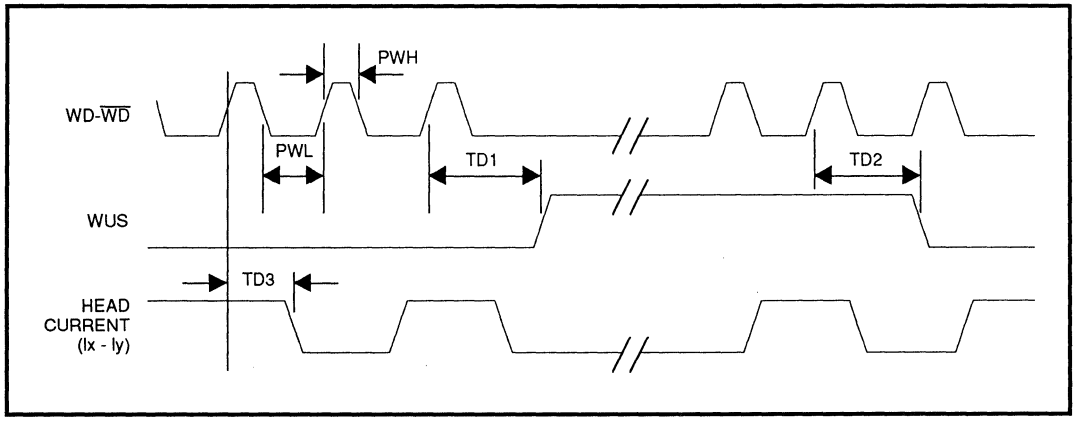



**FIGURE 1: Write Mode Timing Diagram**

Worst Case Read Input Noise Voltage vs. Input Impedance for SSI 32R4610AR/4611AR and SSI 32R4610B

Case 1: IC Base sheet resistance = Maximum
Hence, IC bias Current = Minimum

| | Tj = 25°C | Tj = 110°C | Units |
|---|---|---|---|
| Vn (Max) | .7 | 0.85 | $nV/\sqrt{Hz}$ |
| Rin (Min) | 450 | 475 | Ω |
| Cin (Max) | 28 | 30 | pF |

Case 2: IC Base sheet resistance = Minimum
Hence, IC bias Current = Maximum

| | Tj = 25°C | Tj = 110°C | Units |
|---|---|---|---|
| Vn (Max) | .58 | .65 | $nV/\sqrt{Hz}$ |
| Rin (Min) | 360 | 400 | Ω |
| Cin (Max) | 33 | 35 | pF |

Worst Case Read Input Noise Voltage vs. Input Impedance for SSI 32R4610A/4611A and SSI 32R4610B

Case 1: IC Base sheet resistance = Maximum
Hence, IC bias Current = Minimum

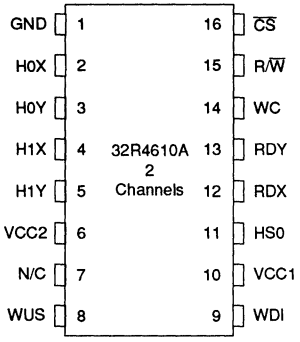
| | Tj = 25°C | Tj = 110°C | Units |
|---|---|---|---|
| Vn (Max) | .7 | 0.85 | $nV/\sqrt{Hz}$ |
| Rin (Min) | 1525 | 1895 | Ω |
| Cin (Max) | 28 | 30 | pF |

Case 2: IC Base sheet resistance = Minimum
Hence, IC bias Current = Maximum

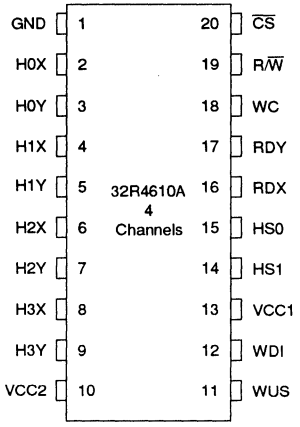
| | Tj = 25°C | Tj = 110°C | Units |
|---|---|---|---|
| Vn (Max) | .58 | .65 | $nV/\sqrt{Hz}$ |
| Rin (Min) | 835 | 1100 | Ω |
| Cin (Max) | 33 | 35 | pF |

## PACKAGE PIN DESIGNATIONS

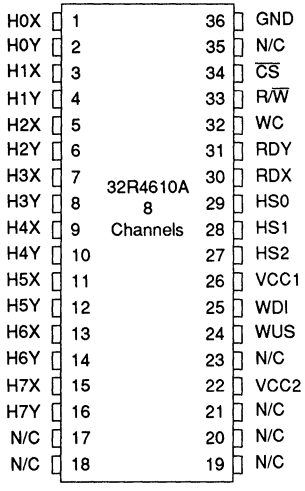
(Top View)



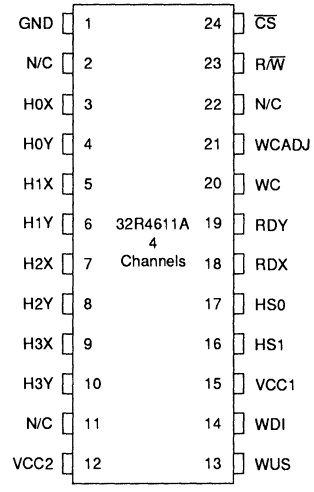

16-Pin SOL




20-Pin SOL, SOV




36-Pin SOM




24-Pin SOL, SOV

## ORDERING INFORMATION

| PART DESCRIPTION | | ORDER NUMBER | PACKAGE MARK |
|---|---|---|---|
| SSI 32R4610A | | | |
| 2-Channel | 16-lead SOL | 32R4610A-2CL | 32R4610A-2CL |
| 4-Channel | 20-lead SOL | 32R4610A-4CL | 32R4610A-4CL |
| 4-Channel | 20-lead SOV | 32R4610A-4CV | 32R4610A-4CV |
| 8-Channel | 36-lead SOM | 32R4610A-8CM | 32R4610A-8CM |
| SSI 32R4610B | Improves WUS from SSI 32R4610A-8 | | |
| 8-Channel | 36-lead SOM | 32R4610B-8CM | 32R4610B-8CM |
| SSI 32R4610AR | Includes 700Ω Resistor | | |
| 2-Channel | 16-lead SOL | 32R4610AR-2CL | 32R4610AR-2CL |
| 4-Channel | 20-lead SOL | 32R4610AR-4CL | 32R4610AR-4CL |
| 4-Channel | 20-lead SOV | 32R4610AR-4CV | 32R4610AR-4CV |
| 8-Channel | 36-lead SOM | 32R4610AR-8CM | 32R4610AR-8CM |
| SSI 32R4610BR | Improves WUS from SSI 32R4610AR-8 | | |
| 8-Channel | 36-lead SOM | 32R4610BR-8CM | 32R4610BR-8CM |
| SSI 32R4611A | Includes WCADJ Function | | |
| 4-Channel | 24-lead SOL | 32R4611A-4CL | 32R4611A-4CL |
| 4-Channel | 24-lead SOV | 32R4611A-4CV | 32R4611A-4CV |
| SSI 32R4611AR | Includes 700Ω Resistor | | |
| 4-Channel | 24-lead SOL | 32R4611AR-4CL | 32R4611AR-4CL |
| 4-Channel | 24-lead SOV | 32R4611AR-4CV | 32R4611AR-4CV |



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Section 2



# HDD PULSE DETECTION

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# SSI 32P541B
## Read Data Processor

2

November 1992

## DESCRIPTION

The SSI 32P541B is a bipolar integrated circuit that provides all data processing necessary for detection and qualification of MFM or RLL encoded read signals.

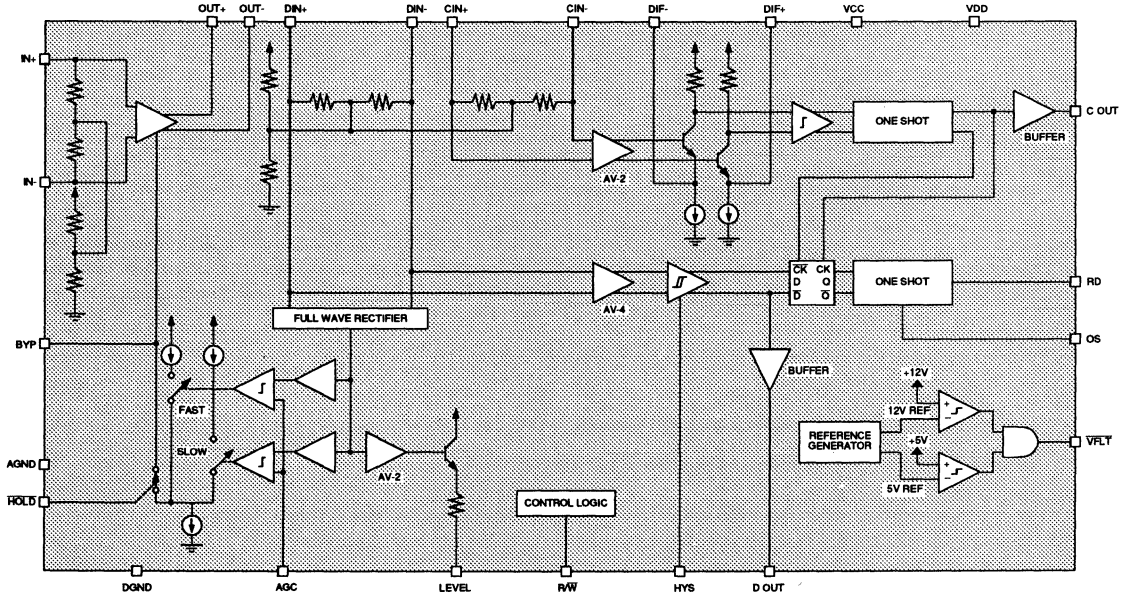
In read mode the SSI 32P541B provides amplification and qualification of head preamplifier outputs. Pulse qualification is accomplished using level qualification of differentiated input zero crossings. An AGC amplifier is used to compensate for variations in head preamp output levels, presenting a constant input level to the pulse qualification circuitry. The AGC loop can be disabled so that a constant gain can be used for embedded servo decoding or other processing needs.

In write mode the circuitry is disabled and the AGC gain stage input impedance is switched to a lower level to allow fast settling of the input coupling capacitors during a write to read transition. The SSI 32P541B requires a +5V or +12V power supply, and is available in 28-pin PLCC and 24-pin SOL.

## FEATURES

- **Level qualification supports high resolution MFM and RLL encoded data retrieval**
- **Wide bandwidth AGC input amplifier**
- **Standard 12V ± 10% and 5V ± 10% supplies**
- **Supports embedded servo pattern decoding**
- **Write to read transient suppression**
- **Fast and slow AGC attack regions for fast transient recovery**
- **Internal voltage fault indicator**
- **≤ ±1.0 ns pulse pairing**
- **24 Mb/s operation**

## BLOCK DIAGRAM



## CIRCUIT OPERATION

### READ MODE

In the read mode (R/$\overline{W}$ input high or open) the input read signal is amplified and qualified using an AGC amplifier and pulse level qualification of the detected signal peaks.

The amplified head signals are AC coupled to the IN + and IN - pins of the AGC amplifier that is gain controlled by full wave rectifying and amplifying the (DIN+ - DIN–) voltage level and comparing it to a reference level at the AGC pin. A fast attack mode, which supplies a 1.7 mA charging current for the capacitor at the BYP pin, is entered whenever the instantaneous DIN ± level is more than 125% of set level. Between 100% and 125% the slow attack mode is invoked, providing 0.18 mA of charging current. The two attack modes allow rapid AGC recovery from a write to read transition while reducing zero crossing distortion once the amplifier is in range.

The level at the AGC pin should be set such that the differential voltage level at the DIN+, DIN- pins is 1.00 Vpp. The voltage level can be up to 2.5 Vpp at the OUT+ and OUT- pins which allows for up to 6 dB loss in any external filter connected between the OUT+, OUT- outputs and the DIN+, DIN- inputs.

$$\frac{Av2}{Av1} = \exp - \left( \frac{V2 - V1}{5.8 + Vt} \right)$$

Gain of the AGC section is nominally
Where: Av1 and Av2 are initial and final amplifier gains. V1, V2 are initial and final voltages on the BYP pin.

Vt = (K x T)/q = 26 mV at room temperature.

One filter for both data (DIN+, DIN- input) and clock (CIN+, CIN- input) paths, or a separate filter for each path may be used. If two filters are used, care must be exercised to control time delays so that each path is timed properly. A multi-pole Bessell filter is typically used for its linear phase or constant group delay characteristics.

### HYSTERESIS LEVEL

In level qualification, hysteresis comparator eliminates errors due to low level additive noise, see Figure 4B.

The 32P541B allows two implementations of hysteresis: fixed hysteresis threshold or DIN tracking hysteresis threshold. Fixed hysteresis threshold can be simply done by a setting a DC voltage at HYS pin, such as from a resistor divider from VCC to GND. The hysteresis threshold at the comparator can be computed as: Hysteresis Gain x $V_{HYS}$. For high performance system application, however, fixed hysteresis threshold is not recommended.

DIN tracking hysteresis has the advantages of shorter write-to-read recovery time and lower probability of error with input amplitude drop out. The hysteresis threshold is designed as a percentage of the DIN peak voltage. This technique can be implemented by feeding the LEVEL output, through a resistor divider network, to the HYS pin (see Figure 4b). The LEVEL output, amplified peak capture of DIN voltage, can be computed as: Level Gain x V(DIN+ - DIN-). With the resistor divider, a fraction of the LEVEL output is presented at the HYS pin. The hysteresis threshold, as a function of DIN, can be summarized as: Level Gain x Resistor Dividing Ratio x Hysteresis Gain x V(DIN+ - DIN-). For a typical case of 1 Vpp differential at DIN± input, assume equal value resistors in the divider network, the hysteresis threshold is 1.95 x 0.50 x 0.19 x 1V = 0.185V. This represents 37% hysteresis on a 1 Vpp signal. While both the Level Gain and Hysteresis threshold vs. HYS bear a moderate tolerance due to typical process variations, they inversely track each other to yield a much tighter hysteresis threshold in a closed loop. In designing the hysteresis threshold, the nominal Level Gain and Hysteresis Gain values should be used. The tolerance on DIN tracking hysteresis threshold is specified as the Tracking Hysteresis Threshold Tolerance in the specification.

While the external resistor divider ratio determines the hysteresis threshold, the total resistance and the peak capture capacitor should be optimized for the system data rate. The RC time constant must be small enough to allow good response to changing DIN± peak-to-peak, but large enough to provide a constant hysteresis threshold in each level qualification.

The filtered clock path signal is differentiated to transform signal peaks to zero-crossings which clock an edge-trigger circuit to provide output pulses at each zero-crossing. The pulses are used to clock the D-type flip-flop. The COUT pin is a buffered test point for monitoring this function.

The differentiator function is set by an external network between the DIF+, DIF- pins. The transfer function is:

Where: C = external capacitor (20 pF to 150 pF)

$$AV = \frac{-2000Cs}{LCs^2 + (R+92)Cs + 1}$$

L = external inductor

R = external resistor

$s = j\omega = j2\pi f$

During normal operation the differentiator circuit clocks the D flip-flop on every positive and negative peak of the signal input to CIN+, CIN-. The D input to the flip–flop only changes state when the signal applied to the DIN+, DIN- inputs exceeds the hysteresis comparator threshold opposite in polarity to the previous peak that exceeded the threshold.

The clocking path, then, determines signal timing and the data path determines validity by blocking signal peaks that do not exceed the hysteresis comparator threshold.

The delays from CIN+, CIN- inputs to the flip-flop clock input and from the DIN+, DIN- inputs to the flip-flop D input are well matched.

### WRITE (DISABLED) MODE

In the write or disabled mode (R/$\overline{W}$ input low) the digital circuitry is disabled and the AGC amplifier input impedance is reduced. In addition the AGC amplifier, gain is set to maximum so that the loop is in its fast attack mode when changing back to Read Mode. The lowered input impedance facilitates more rapid settling of the write to read transient by reducing the time constant of the network between the SSI 32P541B and read/write preamplifier, such as the SSI 32R512.

Internal SSI 32P541B timing is such that this settling is accomplished before the AGC loop is activated when going to read mode. Coupling capacitors should be chosen with as low a value as possible, consistent with bandwidth requirements, to allow more rapid settling.

### LAYOUT CONSIDERATIONS

The SSI 32P541B is a high gain wide bandwidth device that requires care in layout. The designer should keep analog signal lines as short as possible and well balanced. Use of a ground plane is recommended along with supply bypassing and separation of the SSI 32P541B and associated circuitry grounds from other circuits on the disk drive PCB.

### LOW VOLTAGE FAULT DETECTION

A low voltage detection dircuit monitors both supplies and pulls an open collector TTL output low when either supply drops below their trip point. This option is available only in the 28-pin PLCC package.

**TABLE 1: Mode Control**

| R/$\overline{W}$ | $\overline{HOLD}$ | MODE |
|---|---|---|
| 1 | 1 | READ - Read amp on, AGC active, Digital section active |
| 1 | 0 | HOLD - Read amp on, AGC gain held constant Digital section active |
| 0 | X | WRITE - AGC gain switched to maximum, Digital section inactive, common mode input resistance reduced |

## PIN DESCRIPTION

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| VCC | | 5 volt power supply |
| VDD | | 12 volt power supply |
| AGND, DGND | | Analog and Digital ground pins |
| R/$\overline{W}$ | I | TTL compatible read/write control pin |
| IN+, IN- | I | Analog signal input pins |
| OUT+, OUT- | O | AGC Amplifier output pins |
| BYP | | The AGC timing capacitor is tied between this pin and AGND |
| $\overline{HOLD}$ | I | TTL compatible pin that holds the AGC gain when pulled low |
| AGC | I | Reference input voltage level for the AGC circuit |
| DIN+, DIN- | I | Analog input to the hysteresis comparator |
| HYS | I | Hysteresis level setting input to the hysteresis comparator |
| LEVEL | O | Provides rectified signal level for input to the hysteresis comparator |
| DOUT | O | Buffered test point for monitoring the flip-flop D input |
| CIN+, CIN- | I | Analog input to the differentiator |
| DIF+, DIF- | | Pins for external differentiating network |
| COUT | O | Buffered test point for monitoring the clock input to the flip-flop |
| OS | | Connection for read output pulse width setting capacitor |
| RD | O | TTL compatible read output |
| $\overline{VFLT}$* | O | Open collector output that goes low when a low power supply fault is detected. |

*$\overline{VFLT}$ output offered in 28-pin PLCC package only.

## ELECTRICAL SPECIFICATIONS

Unless otherwise specified 4.5 ≤ VCC ≤ 5.5V, 10.8V ≤ VDD ≤ 13.2V, 25 °C ≤ Tj ≤ 135 °C.

### ABSOLUTE MAXIMUM RATINGS

Operation above absolute maximum ratings may permanently damage the device.

| PARAMETER | RATING | UNIT |
|---|---|---|
| 5V Supply Voltage, VCC | 6 | V |
| 12V Supply Voltage, VDD | 14 | V |
| Storage Temperature | -65 to 150 | °C |
| Lead Temperature | 260 | °C |
| R/$\overline{W}$, IN+, IN-, $\overline{HOLD}$, $\overline{VFLT}$ | -0.3 to VCC + 0.3 | V |
| RD | -0.3V to VCC + 0.3V or +12 | mA |
| All others | -0.3 to VDD + 0.3 | V |

### POWER SUPPLY

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| ICC - VCC Supply Current | Outputs unloaded | | | 14 | mA |
| IDD - VDD Supply Current | Outputs unloaded | | | 70 | mA |
| Pd - Power Dissipation | Outputs unloaded, Tj = 135°C | | | 850 | mW |

### LOGIC SIGNALS

| | | | | | |
|---|---|---|---|---|---|
| VIL - Input Low Voltage | | -0.3 | | 0.8 | V |
| VIH - Input High Voltage | | 2.0 | | | V |
| IIL - Input Low Current | VIL = 0.4V | 0.0 | | -0.4 | mA |
| IIH - Input High Current | VIH = 2.4V | | | 100 | µA |
| VOL - Output Low Voltage | IOL = 4.0 mA | | | 0.4 | V |
| VOH - Output High Voltage | IOH = -400 µA | 2.4 | | | V |

### MODE CONTROL

| | | | | | |
|---|---|---|---|---|---|
| Read to Write Transition Time | | | | 1.0 | µs |
| Write to Read Transition Time | AGC settling not included, transition to high input resistance | 1.2 | | 3.0 | µs |
| Read to Hold Transition Time | | | | 1.0 | µs |

### WRITE MODE

| | | | | | |
|---|---|---|---|---|---|
| Common Mode Input Impedance (both sides) | R/$\overline{W}$ pin = low | | 250 | | Ω |

### READ MODE

Unless otherwise specified IN+ and IN- are AC coupled, OUT+, and OUT- are loaded differentially with > 600Ω and each side is loaded with < 10 pF to GND, a 2000 pF capacitor is connected between BYP and GND, OUT+ is AC coupled to DIN+, OUT- is AC coupled to DIN-, AGC pin voltage is 2.2 VDC.

### AGC AMPLIFIER

| | | | | | |
|---|---|---|---|---|---|
| Differential Input Resistance | V(IN+ – IN-) = 100 mVpp @ 2.5 MHz | | 5K | | Ω |
| Differential Input Capacitance | V(IN+ – IN-) = 100 mVpp @ 2.5 MHz | | | 10 | pF |
| Common Mode Input Impedance | R/$\overline{W}$ pin high | | 1.8 | | kΩ |
| (both sides) | R/$\overline{W}$ pin low | | 0.25 | | kΩ |
| Minimum Gain Range | 1.0 Vpp ≤ V(OUT+ – OUT-) ≤ 2.5 Vpp | 4.0 | | 83 | V/V |

**AGC AMPLIFIER** (Continued)

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Input Noise Voltage | Gain set to maximum, RS = 0<br>Bw = 15 MHz | | | 30 | nV/√Hz |
| Bandwidth | Gain set to maximum<br>-3 dB point | 30 | | | MHz |
| Maximum Output Voltage Swing | Set by AGC pin voltage | 3.0 | | | Vpp |
| OUT+ to OUT- Pin Current | No DC path to GND | ±3.2 | | | mA |
| Output Resistance | | 12 | | 32 | Ω |
| Output Capacitance | | | | 15 | pF |
| (DIN+ – DIN-) Input Voltage Swing VS AGC Input Level | 30 mVpp ≤ V(IN+ – IN-) @ 2.5 MHz | 0.33 | | 0.43 | Vpp/V |
| | ≤ 550 mVpp; @ 9 MHz | 0.44 | | 0.69 | Vpp/V |
| | 0.5 Vpp ≤ V(DIN+ – DIN-) ≤ 1.5 Vpp | | | | |
| (DIN+ – DIN-) Input Voltage Swing Variation | 30 mVpp V(IN+ – IN-) @ 2.5 MHz | | | 4 | % |
| | ≤ 550 mVpp AGC Fixed, @ 9 MHz | | | 12 | % |
| | over supply & temp. @ 9 MHz Cold | | | 14 | % |
| Gain Decay Time (Td) | Vin = 300 mVpp–> 150 mVpp at 2.5 MHz, Vout to 90% of final value Figure 1a | | 50 | | µs |
| Gain Attack time (Ta) | From Write to Read transition to Vout at 110% of final value Vin = 400 mVpp @ 2.5 MHz. Figure 1b | | 4 | | µs |
| Fast AGC Capacitor Charge Current | V(DIN+ - DIN-) = 1.6V<br>V(AGC) = 2.2V | 1.3 | | 2.0 | mA |
| Slow AGC Capacitor Charge Current | V(DIN+ – DIN-) = 1.6V Vary V(AGC) until slow discharge | 0.14 | | 0.22 | mA |
| Fast to Slow Attack Switchover Point | $\frac{V(DIN+-DIN-)}{V(DIN+-DIN-)\ Final}$ | | 1.25 | | |
| AGC Capacitor Discharge Current | V(DIN+ – DIN-) = 0.0V | | | | |
| | Read Mode | | 4.5 | | µA |
| | Hold Mode | -0.2 | | +0.2 | µA |
| CMRR (Input Referred) | V(IN+) = V(IN-) = 100 mVpp @ 5 MHz,gain at max. | 40 | | | dB |
| PSRR (Input Referred) | ΔVCC or ΔVDD = 100 mVpp @ 5 MHz, gain at max. | 30 | | | dB |
| Maximum AGC Amplifier Output Offset Variation | V(IN+ - IN-) = 0<br>Min to max gain | | | 200 | mV |

**HYSTERESIS COMPARATOR**

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Input Signal Range | | | | 1.5 | Vpp |
| Differential Input Resistance | V(DIN+ – DIN-) = 100 mVpp @ 2.5 MHz | 5 | | 11 | kΩ |
| Differential Input Capacitance | V(DIN+ – DIN-) = 100 mVpp @ 2.5 MHz | | | 6.0 | pF |
| Common Mode Input Impedance | (both sides) | | 2.0 | | kΩ |
| Comparator Offset Voltage | HYS pin at GND, ≤ 1.5 kΩ across DIN+, DIN- | | | 10 | mV |
| Hysteresis Gain (see figure 4c) | At DIN+, DIN- pins 1V < V (HYS) < 3V | 0.16 | 0.19 | 0.22 | V/V |
| HYS Pin Input Current | 1V < V (HYS) < 3V | 0.0 | | -20 | µA |
| Tracking Hysteresis Threshold Tolerance | V (Hys) = some % of *V (AGC) or V (LEVEL) 1V < V (Hys) < 3V; f = 0-9 MHz | -15 | | +15 | % Peak |
| Level Gain (see figure 4d) | 0.6 < \| V (DIN+ – DIN-) \| <1.3 Vpp, 10 kΩ from LEVEL pin to GND | 1.7 | 1.95 | 2.2 | V/Vpp |
| LEVEL Pin Max Output Current | | 3.0 | | | mA |
| LEVEL Pin Output Resistance | I(LEVEL) = 0.5 mA | | 180 | | Ω |
| DOUT Pin Output Low Voltage | 0.0 ≤ IOL ≤ 0.5 mA | VDD -4.0 | | VDD -2.8 | V |
| DOUT Pin Output High Voltage | 0.0 ≤ IOH ≤ 0.5 mA | VDD -2.5 | | VDD -1.8 | V |

*In an open loop configuration where reference is V(AGC) tolerance can be slightly higher

**ACTIVE DIFFERENTIATOR**

| | | | | | |
|---|---|---|---|---|---|
| Input Signal Range | | | | 1.5 | Vpp |
| Differential Input Resistance | V(CIN+ – CIN-) = 100 mVpp @ 2.5 MHz | 5.8 | | 11.0 | kΩ |
| Differential Input Capacitance | V(CIN+ – CIN-) = 100 mVpp @ 2.5 MHz | | | 6.0 | pF |
| Common mode Input Impedance | (both sides) | | 2.0 | | kΩ |
| Voltage Gain From CIN± to DIF± | R(DIF+ to DIF-) = 2 kΩ | 1.7 | | 2.2 | V/V |
| DIF+ to DIF- Pin Current | Differentiator Impedance must be set so as not to clip signal at this current level | ±1.3 | | | mA |
| Comparator Offset Voltage | DIF+, DIF- are AC Coupled | | | 10.0 | mV |
| COUT Pin Output Low Voltage | 0.0 ≤ IOH ≤ 0.5 mA | | VDD -3.0 | | V |
| COUT Pin Output Pulse voltage V(high) - V(low) | 0.0 ≤ IOH ≤ 0.5 mA | | +0.4 | | V |
| COUT Pin Output Pulse Width | 0.0 ≤ IOH ≤ 0.5 mA | | 30 | | ns |

**OUTPUT DATA CHARACTERISTICS** (See Figure 2)
Unless otherwise specified V(CIN+ – CIN-) = V(DIN+ – DIN-) = 1.0 Vpp AC coupled sine wave at 2.5 MHz differentiating network between DIF+ and DIF- is 100Ω in series with 65 pF, V (Hys) = 1.8 DC, a 33 pF capacitor is connected between OS and VCC, RD- is loaded with a 4 kΩ resistor to VCC and a 10 pF capacitor to GND.

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| D-Flip-Flop Set Up Time (Td1) | Min delay from V(DIN+ DIN-) exceeding threshold to V(DIF+ – DIF-) reaching a peak | 0 | | | ns |
| Propagation Delay (Td3) | | | | 110 | ns |
| Output Data Pulse Width<br><br>Variation | Td5 = 11.4 ns + 740 • Cos<br>50% - 50%<br>15 pF ≤ Cos ≤ 150 pF | | | ±15 | % |
| Pulse Pairing | \|Td3 - Td4\| | | | ±1.0 | ns |
| Output Rise Time | From 0.4V to 2.4V level | | | 15 | ns |
| Output Fall Time | From 0.4V to 2.4V level | | | 9 | ns |

**SUPPLY VOLTAGE FAULT DETECTION**

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| VDD Fault Threshold | | 9.1 | | 10.3 | V |
| VCC Fault Threshold | | 4.1 | | 4.4 | V |
| VOL Output Low Voltage | 4.5 < VCC < 5.5V,<br>IOL = 1.6 mA | | | 0.4 | V |
| | 1.0 < VCC < 4.5V,<br>IOL = 0.5 mA | | | 0.4 | V |
| IOH Output High Current | | | | 25 | µA |

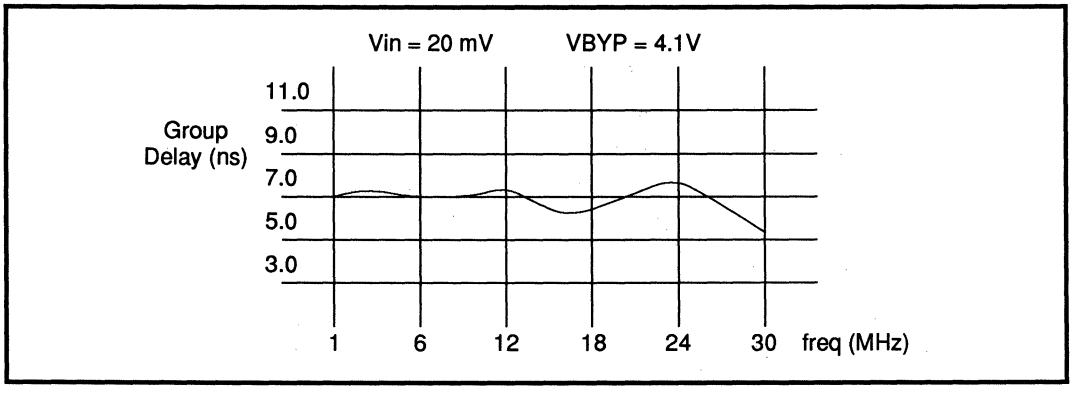



**FIGURE 1: AGC Amplifier - Typical Group Delay Variation**

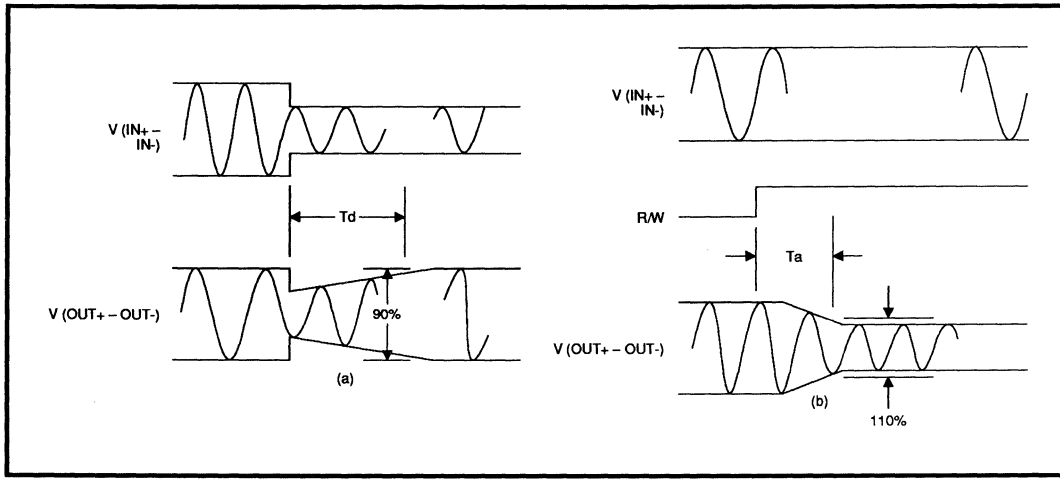



**FIGURE 1(a), (b): AGC Timing Diagrams**

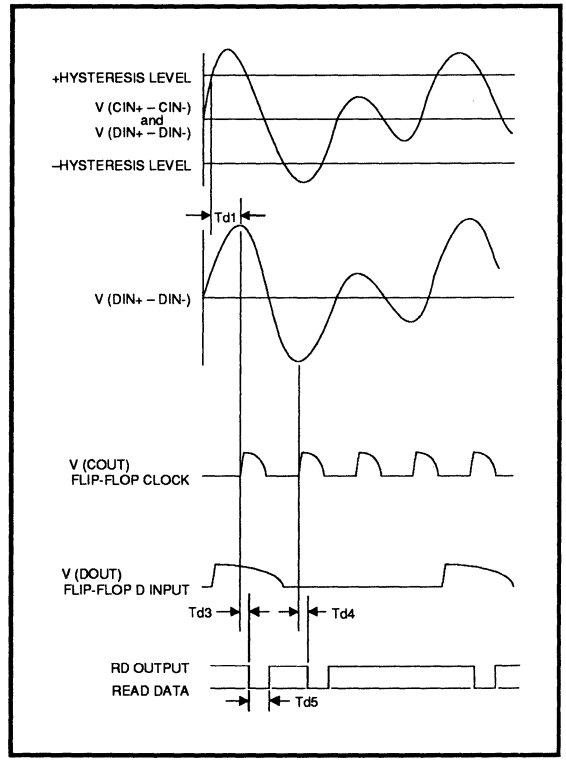
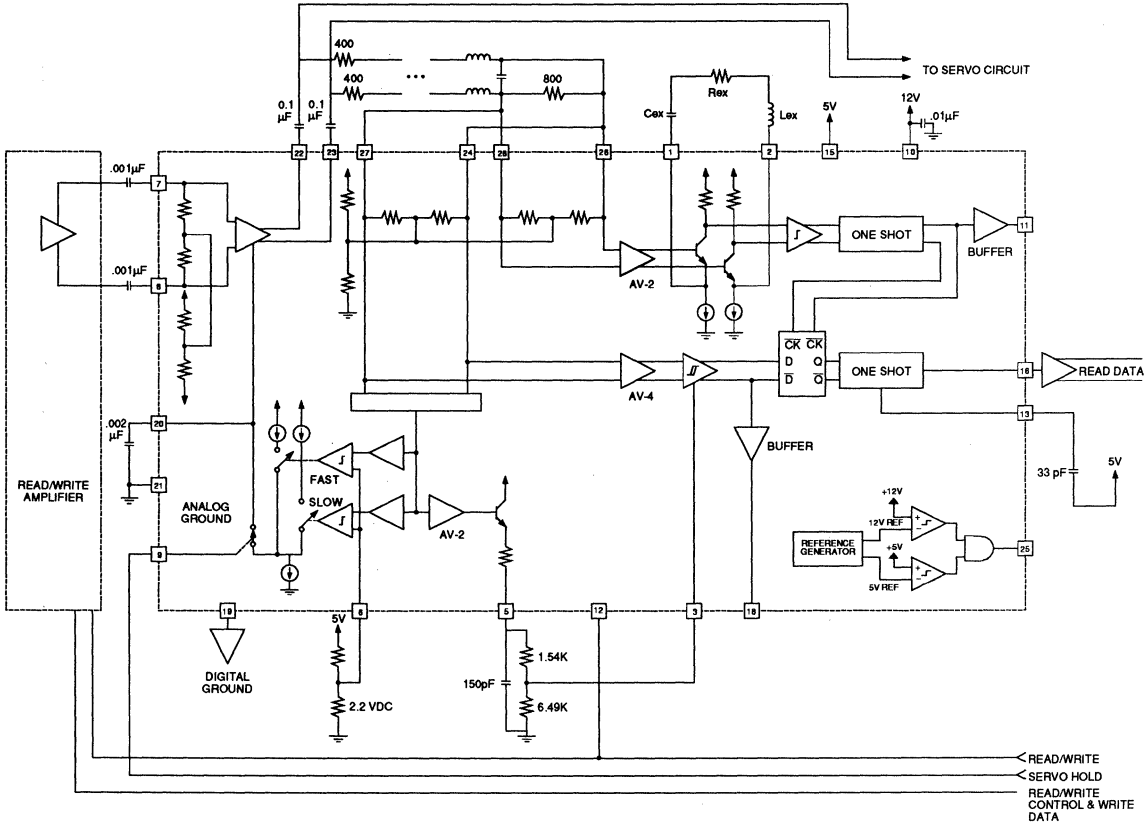



**FIGURE 2: Timing Diagram**




NOTE: Circuit traces for the 12V bypass capacitor and the AGC Hold Capacitor should be as short as possible with both capacitors returned to the Analog Ground Pin.
Component values, where given, are for a 24 Mbit/s System.
Above pin numbers are for the 28-pin PLCC package.

**FIGURE 3: Typical Read/Write Electronics Set Up**

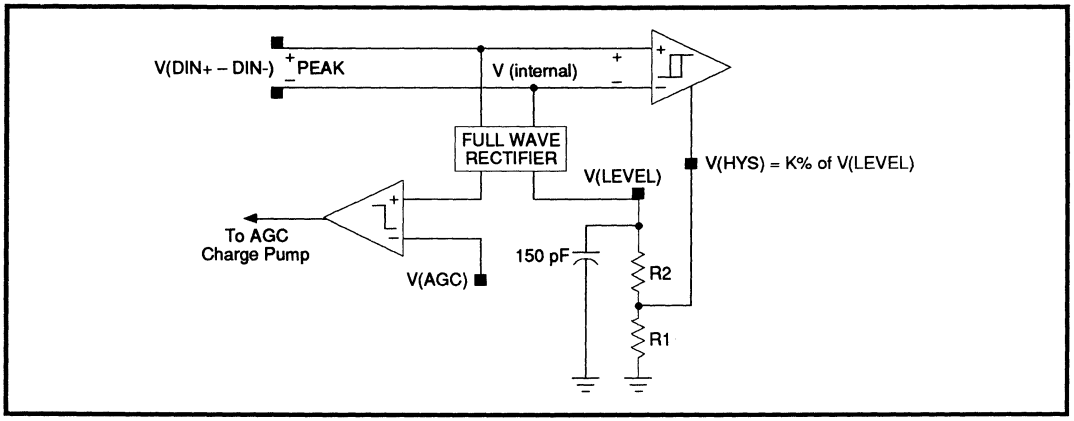



**FIGURE 4a: Feed Forward Mode**

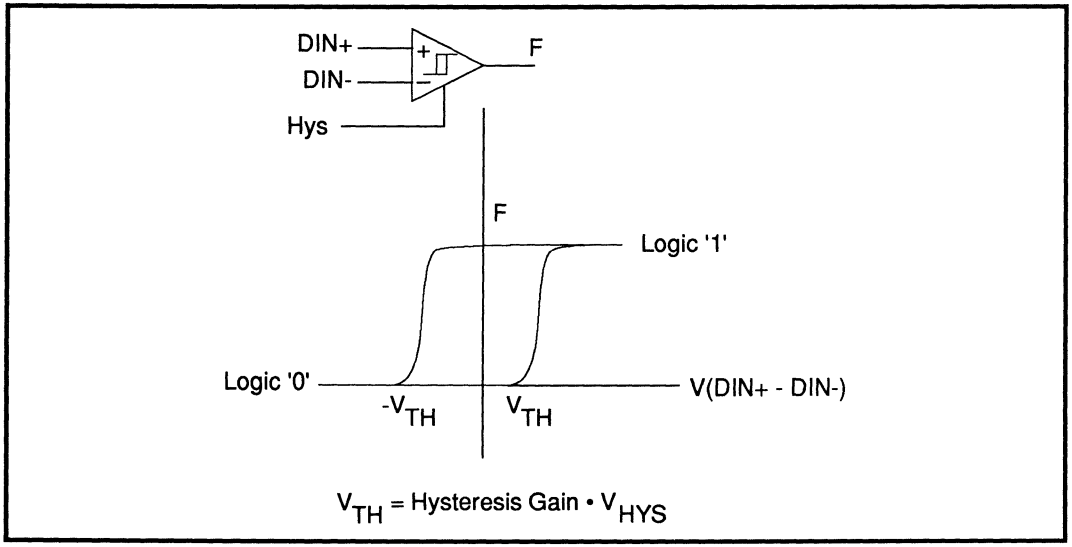



**FIGURE 4b: Hysteresis Comparator Transfer Function**

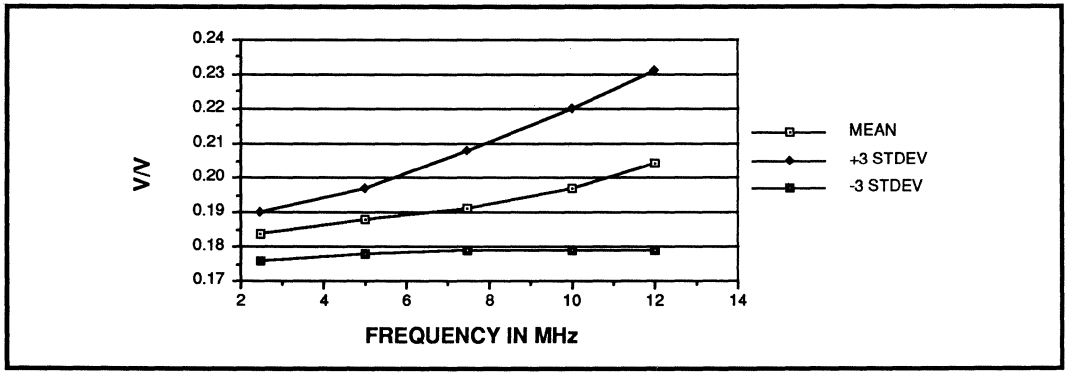



**FIGURE 4c: Hysteresis Gain**

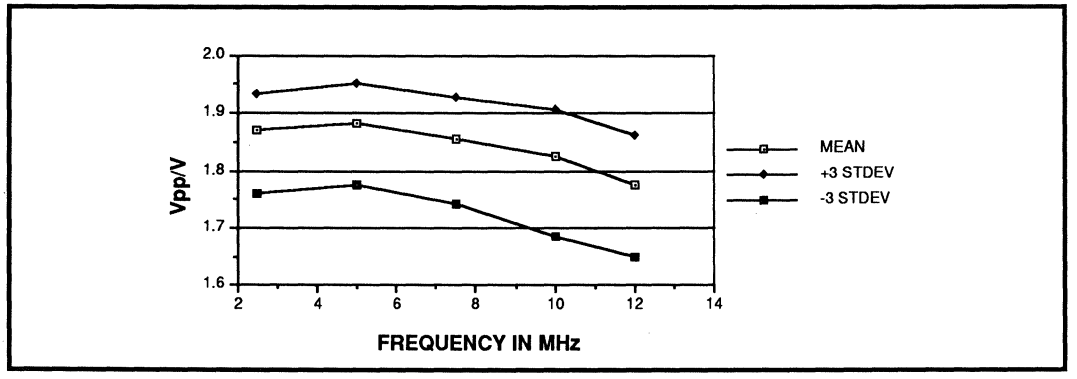



**FIGURE 4d: Level Gain**

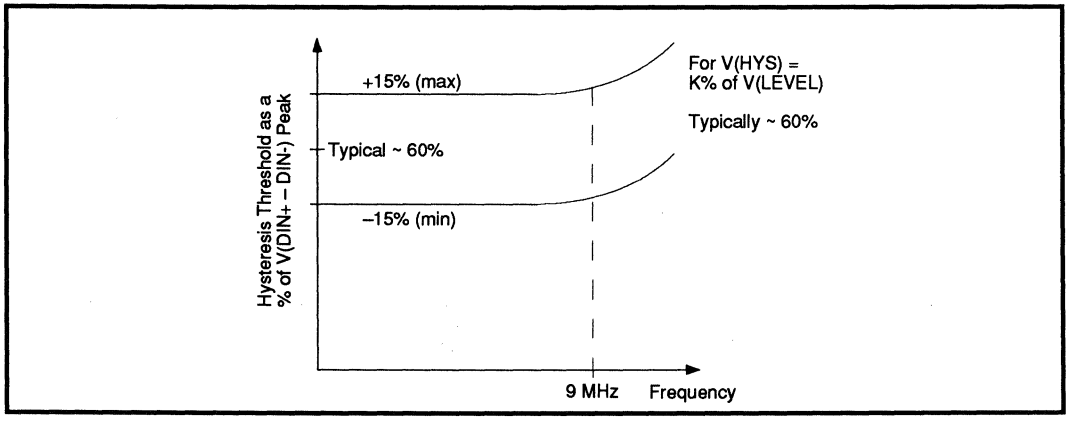
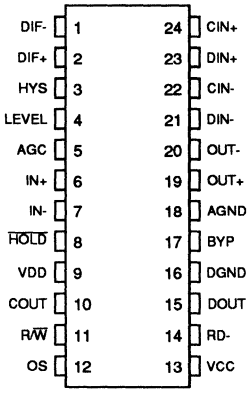


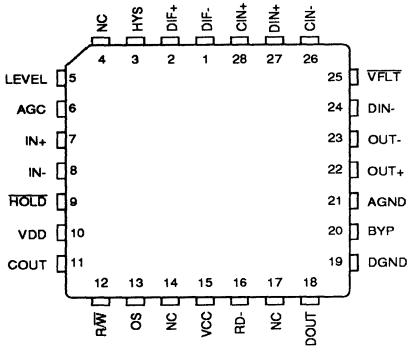

**FIGURE 5: Percentage Threshold Versus Frequency**

## PACKAGE PIN DESIGNATIONS

(Top View)




**24-Lead SOL**




**28-Lead PLCC**

**THERMAL CHARACTERISTICS: θja**

| | |
|---|---|
| 24-Lead SOL | 80°C/W |
| 28-Lead PLCC | 65°C/W |

CAUTION: Use handling procedures necessary for a static sensitive component.

## ORDERING INFORMATION

| PART DESCRIPTION | ORDERING NUMBER | PACKAGE MARK |
|---|---|---|
| SSI 32P541B Read Data Processor | | |
| 28-Lead PLCC | SSI 32P541B-CH | SSI 32P541B-CH |
| 24-Lead SOL | SSI 32P541B-CL | SSI 32P541B-CL |



Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 573-6000, FAX (714) 573-6914

**Notes:**

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A TDK Group Company

# SSI 32P544
## Read Data Processor and Servo Demodulator

2

December 1992

## DESCRIPTION

The SSI 32P544 Read Data Processor and Servo Demodulator has a fully integrated bipolar circuit that detects and validates amplitude peaks in the output from a disk drive read amplifier, as well as detecting embedded servo information to provide position error signals used for read head positioning.

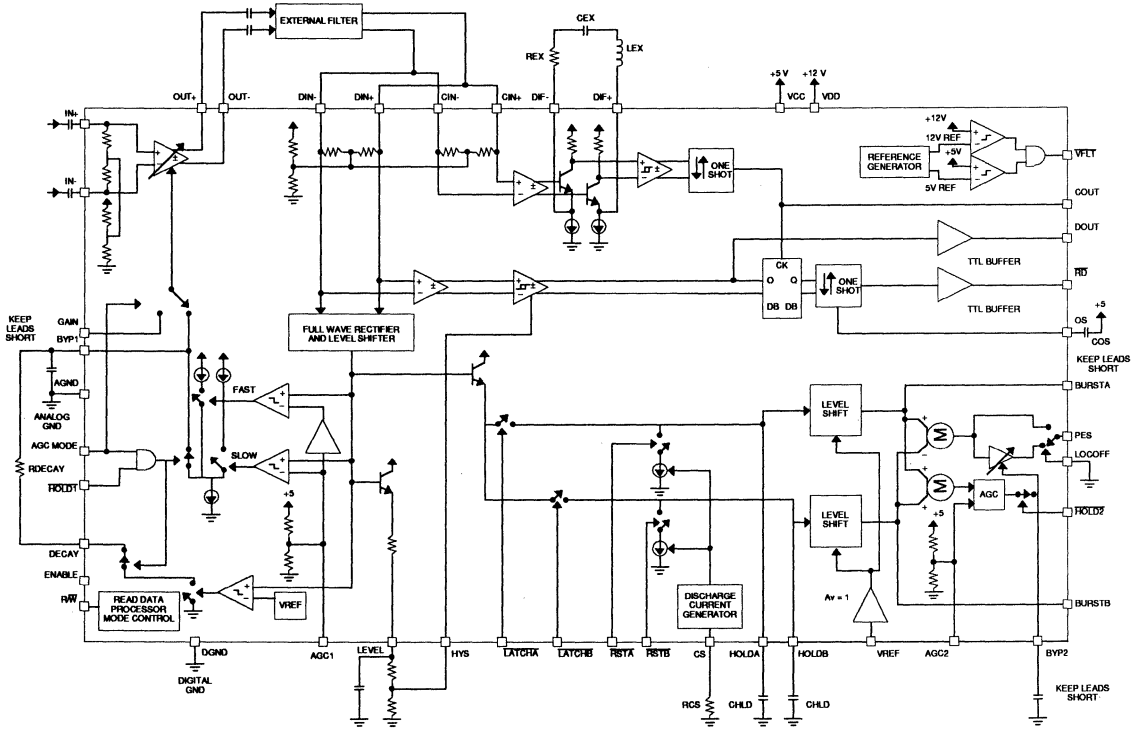
Time and amplitude qualification are used to provide a TTL compatible output that accurately duplicates the time position of input signal peaks. An AGC control loop, using a dual rate charge pump, provides a constant imput amplitude for the level qualifier. Level qualification can be implemented as a fixed threshold or a constant percentage that tracks signal amplitude that enhances qualification during AGC loop transients.

(Continued)

## FEATURES

- **Wide bandwidth AGC input amplifier**
- **Level qualification supports MFM and RLL encoded data retrieval**
- **Fast and slow AGC attack and decay regions for fast transient recovery**
- **Embedded servo channel provides servo burst capture and difference circuits**
- **Local servo AGC provided based on servo burst output amplitude sum**
- **Standard ±10%, 12V and 5V supplies**
- **Write to Read transient suppression**

## BLOCK DIAGRAM



## DESCRIPTION (Continued)

The Servo Demodulator consists of two peak detector channels that capture rectified servo data peaks. Buffered individual channel outputs are provided along with a difference output. Servo channel gain can be controlled by an AGC signal based on maintaining the amplitude of the sum of both channels.

The circuit also provides a voltage fault flag that indicates a low voltage condition on either supply.

The SSI 32P544 requires standard ±10% tolerance +5V and +12V supplies and is available in a 44-pin PLCC package.

## CIRCUIT OPERATION

### READ MODE

In Read Mode the SSI 32P544 is used to process either data or servo signals. In the Data Read Mode the input signal is amplified and qualified using an AGC amplifier and pulse level qualification of the detected signal peaks. In the Servo Read Mode the input signal is amplified and an error signal based on amplitude comparison is made available.

### DATA READ MODE

An amplified head output signal is AC coupled to the IN+ and IN- pins of the AGC amplifier. Gain control is accomplished by full wave rectifying and amplifying the [(DIN+) - (DIN-)] voltage level and comparing it to a reference voltage level at the AGC1 pin.

Two attack modes are entered depending on the instantaneous level at DIN±. For DIN± levels above 125% of desired level a fast attack mode is invoked that supplies 1.7 mA charging current to the network on the BYP1 pin. Between 125% and 100% of the desired level the circuit enters a slow attack mode and supplies 0.18 mA of charging current. This allows the AGC to rapidly recover during a write to read transition but reduces distortion once the AGC amplifier is in range.

Two decay modes are available that apply a discharge current to the BYP1 pin network when DIN± falls below the desired level. An internal decay current sink will supply 4.0 µA of discharge current. Also, if |(DIN+) - (DIN-)| is above 200 mV0-pk a decay current, controlled by a resistor from BYP1 to DECAY, is switched in to decrease decay time. The amount of charge pulled from the AGC timing capacitor on each data pulse is:

$$Q_{DECAY} = K_1(Ton + Ts)/R_{DECAY}$$

Where:

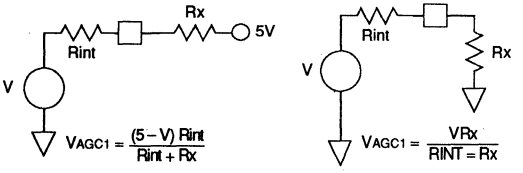
$K_1$ = 4.0V typ.

Ton = Time in seconds that the data pulse at DIN± is greater than 200 mVop

Ts = Switching time in seconds (<2 µs, max)

The AGC1 pin is internally biased so that the target differential voltage input at DIN± is 1.0 Vpp at nominal conditions. The AGC1 voltage can be modified by tying a resistor between AGC1 and ground or VCC. A resistor to ground decreases the voltage level while a resistor to VCC increases it. The resultant AGC1 voltage level is:

Where:




V = Voltage at AGC1 with pin open (2.2V, nom.)

Rint = AGC1 pin input impedance (6.7 kΩ, typ.)

Rx = External resistor.

The new DIN± input target level is nominally 0.48 Vpp/ $V_{AGC1}$

The AGC amplifier can swing 3.0 Vpp at OUT± which allows for up to 6 dB loss in any external filter between OUT± and DIN±.

Gain of the AGC amplifier is nominally:

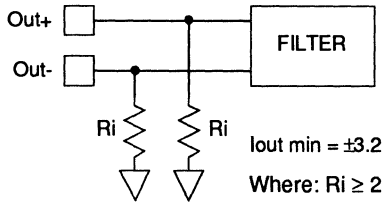
$$Av1/Av2 = e^{[6.9\,(V2 - V1)]}$$

Where:

Av1, Av2 are initial and final amplifier gains.

V1, V2 are initial and final voltages on the BYP1 pin.

The minimum output current from the AGC amplifier is ±3.2 mA. In cases where more current is required to drive a low impedance load the current can be increased by connecting load resistors Ri from OUT± to GND, as shown below.




One filter for both amplitude (DIN± input) and time (CIN± input) channels, or a separate filter for each may be used. If two filters are used, attention must be paid to time delays so that each channel is timed properly. A multi-pole Bessel filter is typically used for its linear phase or constant group delay characteristics.

In the amplitude channel the signal is sent to a hysteresis comparator. The hysteresis threshold level is set so that it will be tripped only by valid signal pulses and not by baseband noise. It can be fixed level or a fraction of the DIN± voltage level.

The latter approach is accomplished by using an external filter/network between the LEVEL and HYS pins. This allows setting the AGC slow attack and decay times slow enough to minimize time channel distortion and setting a shorter time constant for the hysteresis level. The LEVEL pin output is a rectified and amplified version of DIN±, 1.0 Vpp at DIN± results in 2.0 V0-pk nominally, at the LEVEL pin. A voltage divider is used from LEVEL to ground to set the Hysteresis threshold at a percentage of the peak DIN± voltage. For example, if DIN± is 1.0 Vpp, then using an equal valued resistor divider will result in 1.0 V0-pk at the HYS pin. This will result in a nominal ±0.210V threshold or a 42% threshold of a ±0.500V DIN± input. The capacitor is chosen to set an appropriate time constant. This "feed forward" technique speeds up transient recovery by allowing qualification of the input pulses while the AGC is still settling. This helps in the two critical areas of write to read and head change recovery. Some care in the selection of the hysteresis level time constant must be exercised so as to not miss pattern (resolution) induced lower amplitude signals. The output of the hysteresis comparator is the "D" input of a D-type flip-flop. The DOUT pin provides a buffered TTL compatible comparator output signal for testing purposes or for use in the servo circuit if required.

In the time channel the signal is differentiated to transform signal peaks to zero crossings which are detected and used to trigger a bi-directional one-shot. The one-shot output pulses are used as the clock input of the D flip-flop. The COUT pin provides the one-shot output for test purposes.

The differentiator function is accomplished by an external network between the DIF+ and DIF- pins. The transfer function from CIN± to the comparator input (not DIF±) is:

$$Av = \frac{-1000(Abuf)(Cs)}{2LCs^2 + C(R+92)s + 1}$$

Where: C, L, R are external passive components
20 pF < C < 150 pF
Abuf = Gain From CIN± to DIF±
$s = j\omega = j2\pi f$

During normal operation, the time channel clocks the D flip-flop on every positive and negative peak of the CIN± input. The D input to the flip-flop only changes state when the DIN± input exceeds the hysteresis comparator threshold opposite in polarity to the previous threshold exceeding peak.

The time channel, then, determines signal peak timing and the amplitude channel determines validity by blocking signal peaks that do not exceed the hysteresis comparator threshold. The delays in each of these channels to the D flip-flop inputs are well matched.

The D flip-flop output triggers a one-shot that sets the $\overline{RD}$ output pulse width. Width is controlled by an external capacitor from the OS pin to VCC.

### SERVO READ MODE

A position error signal (PES) is generated based on the relative amplitude of two servo signals, A and B. Several methods are made available for maintaining channel gain during servo signal processing.

**SERVO READ MODE** (Continued)

Rectified servo signal peaks are captured on hold capacitors at the HOLDA/B pins. This is accomplished by pulling $\overline{\text{LATCHA}}$ or $\overline{\text{LATCHB}}$ low for a sample period. Additionally, a hold capacitor discharge current of up to 1.0 mA can be turned on by pulling $\overline{\text{RSTA}}$ or $\overline{\text{RSTB}}$ low. The discharge current is determined by a resistor tied between CS and ground. Its magnitude is:

$$Ics = 2.6/(Rcs + 750)\ A, typ.$$

Where: Rcs = resistor from CS to ground

Outputs BURSTA/B & PES are referenced to an external reference applied to the VREF pin.

As noted, several methods are used to determine channel gain in Servo Read Mode. These methods make use of the data read mode AGC loop, the servo AGC loop and external or fixed AGC loop gain. Two methods are used that control the channel gain based on maintaining the sum of A & B channel amplitudes.

In one case (see Figure 1) the BYP2 pin is connected to the GAIN pin and the servo channel gain is determined by the read channel gain as controlled by the sum of the A and B amplitudes. In this case a current is sourced/sinked to/from the capacitor on the GAIN/BYP2 pin whenever the $\overline{\text{HOLD2}}$ pin is pulled high. The current magnitude and direction is determined by:

$$Ic = K_4[(K_5 \bullet V_{AGC2}) - Va(DIN)pp - Vb(DIN)pp]$$

Where:

$V_{AGC2}$ = AGC2 pin voltage

$K_4$ = 650 µA/Vpp

$K_5$ = 0.39 V/V

Va/b(DIN)pp = peak to peak A or B servo pattern Signal voltages at DIN±

The other case (see Figure 2) controls the channel by fixing the Read Data channel gain by taking $\overline{\text{HOLD1}}$ low and closing the loop about the Servo Channel AGC (LOCOFF is held low for this mode).

$\overline{\text{HOLD2}}$ is used to update the control voltage on the AGC capacitor at the BYP2 pin. This AGC function has a time constant defined by:

$$\text{Time Constant} = K_6 \bullet C_{BYP2}$$

Where: $K_6$ = 1.64 to 7.5 kΩ

$C_{BYP2}$ = BYP2 pin capacitor value in farads

Another method (see Figure 5) uses either a fixed voltage at the GAIN pin to determine channel gain or a gain based on preamble data amplitude. In this case no AGC methods are used that are based on servo signal amplitudes. Gain, as determined by an external voltage has been covered above. In the preamble method $\overline{\text{HOLD1}}$ is taken low during a preamble and the channel gain, determined by that necessary to maintain DIN± as programmed by the AGC1 voltage, is held during servo data processing.

**WRITE MODE**

In Write Mode the SSI 32P544 is disabled and preset for the following Read Mode. The digital circuitry is disabled, the input AGC amplifier gain is set to maximum and the AGC amplifier input impedance is reduced.

Resetting the AGC amplifier gain and input impedance shortens system Write to Read recovery times. With the AGC gain at maximum when returning to Read mode the AGC loop is in fast attack mode.

The lowered input impedance improves settling time by reducing the time constant of the network between the SSI 32P544 and a read preamplifier such as the SSI 32R510A. Write to read timing is controlled to maintain the reduced impedance for 1.2 to 3.0 µs before the AGC circuitry is activated. Coupling capacitors should be chosen with as low a value as possible consistent with adequate bandwidth to allow more rapid settling.

**POWER DOWN MODE**

A power down mode is provided to reduce power usage during the idle periods. Taking ENABLE pin low selects this mode. Recovery from this state can be slow due to the necessity of charging external capacitors.

**LOW VOLTAGE FAULT DETECTION**

A low voltage detection circuit monitors both supplies and pulls an open collector TTL output low whenever either supply drops below their trip point.

**MODE CONTROL**

The SSI 32P544 circuit mode is controlled by the ENABLE, R/$\overline{\text{W}}$, AGCMODE, $\overline{\text{HOLD1}}$, $\overline{\text{HOLD2}}$, and LOCOFF pins as shown in Table 1.

**Data Read Mode**

AGC active and controlled by data, Digital section active

**Data Read Mode, Hold**

AGC gain held constant, Digital section active. Gain will drift higher at rate determined by $C_{BYP1}$ and Hold mode discharge current.

**Servo Read Mode I** (See Figures 1 & 3)

The BYP2 and GAIN pins are tied together. Read amplifier AGC control voltage developed from sum of Servo signal levels. $\overline{HOLD2}$ is toggled to update the control voltage after each Servo frame.

**Servo Read Mode II** (See Figures 2 & 4)

Read amplifier AGC gain held fixed ($\overline{HOLD1}$ low). Servo AGC loop activated with $\overline{HOLD2}$ toggled to update or hold gain based on a constant servo signal sum.

**Servo Mode III** (See Figure 5)

Read channel gain determined by voltage on GAIN pin.

**Write**

Read amplifier input impedance reduced. BYP1 pin voltage pulled low to select maximum amplifier gain. Digital section deactivated.

**Power Down**

Circuit switched to a low current disabled mode.

Note: When AGCMODE is switched to a low state the voltage at the BYP1 pin will be held subject to Hold mode discharge current induced drift. So, when returning to Data Read Mode, the channel gain will be the same as it was prior to AGCMODE switching or slightly higher.

**TABLE 1: SSI 32P544 Circuit Mode Control**

| ENABLE | R/$\overline{W}$ | AGC MODE | $\overline{HOLD1}$ | $\overline{HOLD2}$ | LOCOFF | READ PATH MODES |
|---|---|---|---|---|---|---|
| 1 | 1 | 1 | 1 | - | - | Data Read Mode |
| 1 | 1 | 1 | 0 | - | - | Data Read Mode Hold |
| 1 | 1 | 0 | - | 1 | 1 | Servo Read Mode I |
| 1 | 1 | 0 | - | 0 | 1 | |
| 1 | 1 | 1 | 0 | 0 | 0 | Servo Read Mode II |
| 1 | 1 | 1 | 0 | 1 | 0 | |
| 1 | 1 | 0 | - | - | - | Servo Mode III |
| 1 | 0 | - | - | - | - | Write |
| 0 | - | - | - | - | - | Power Down |

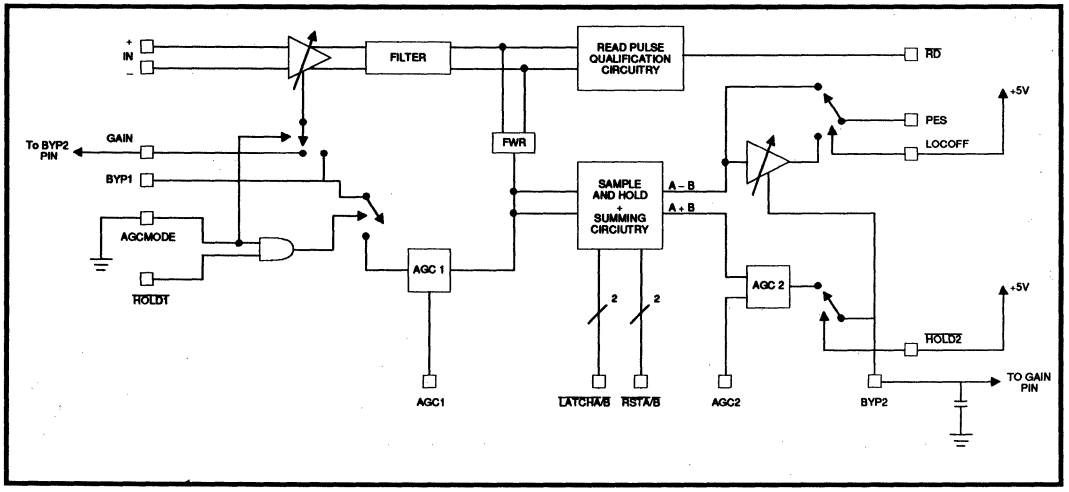



**FIGURE 1: Servo Read Mode I**

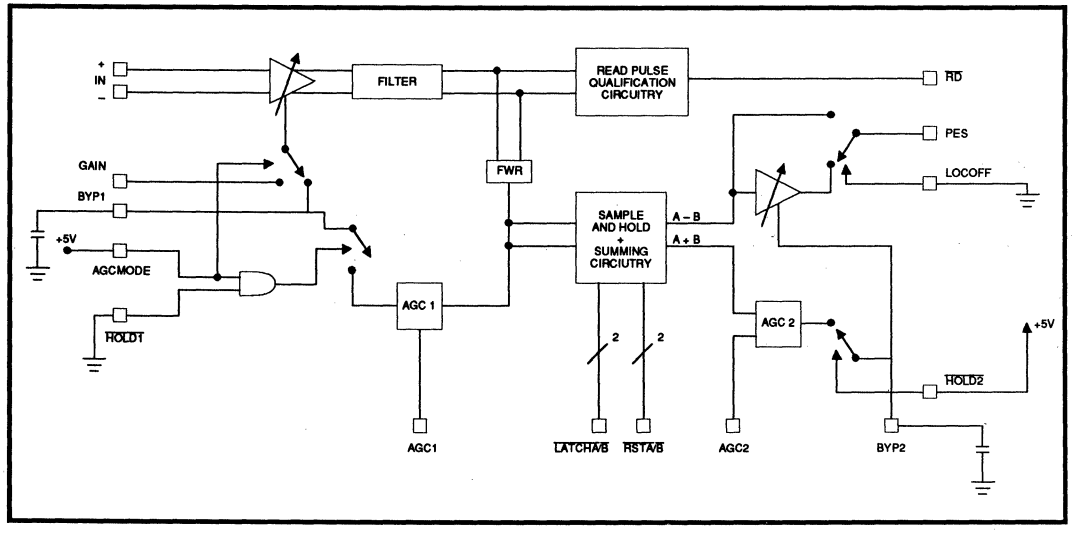



**FIGURE 2: Servo Read Mode II**

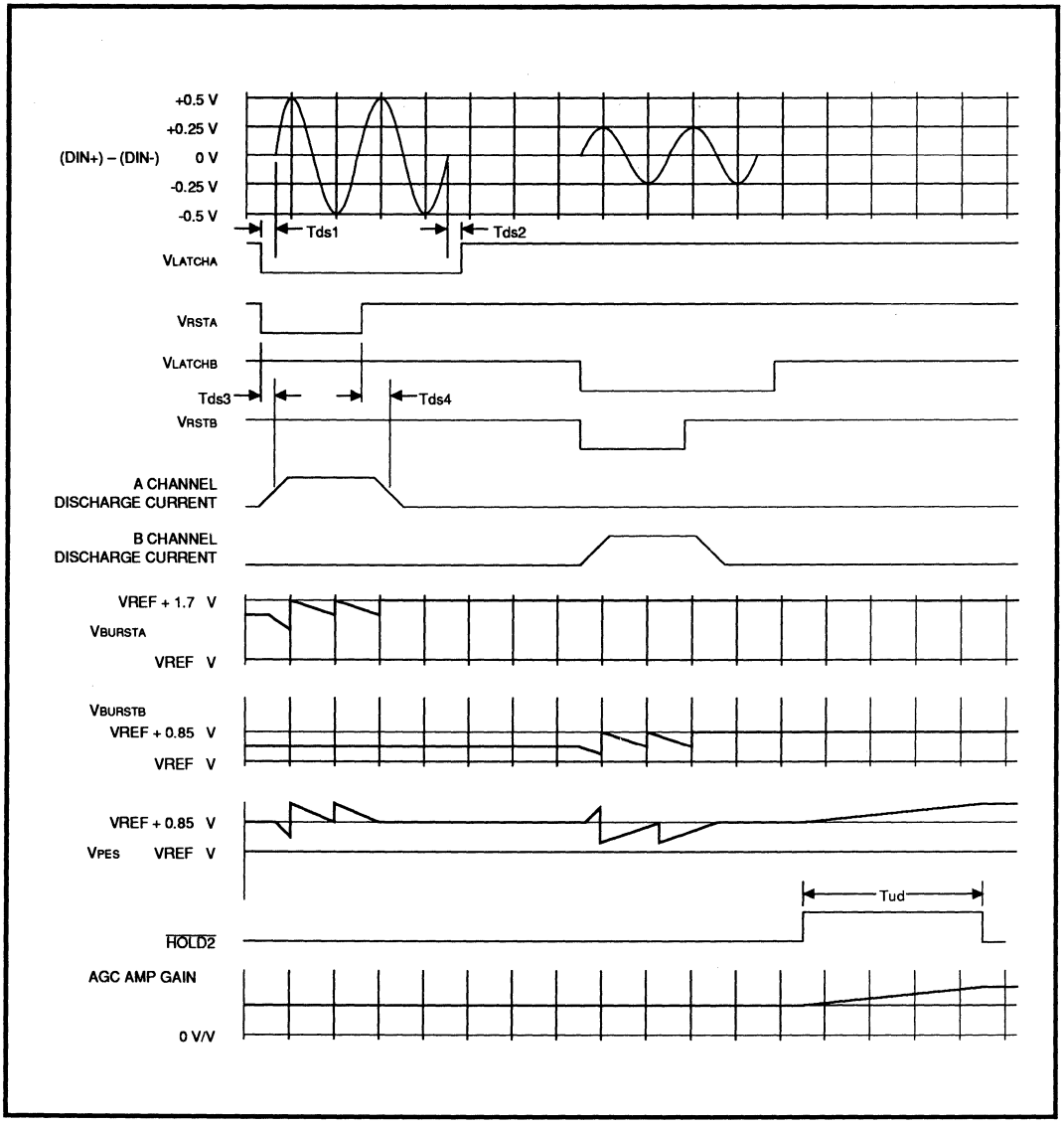



**FIGURE 3: Servo Read Mode I Timing Diagram**

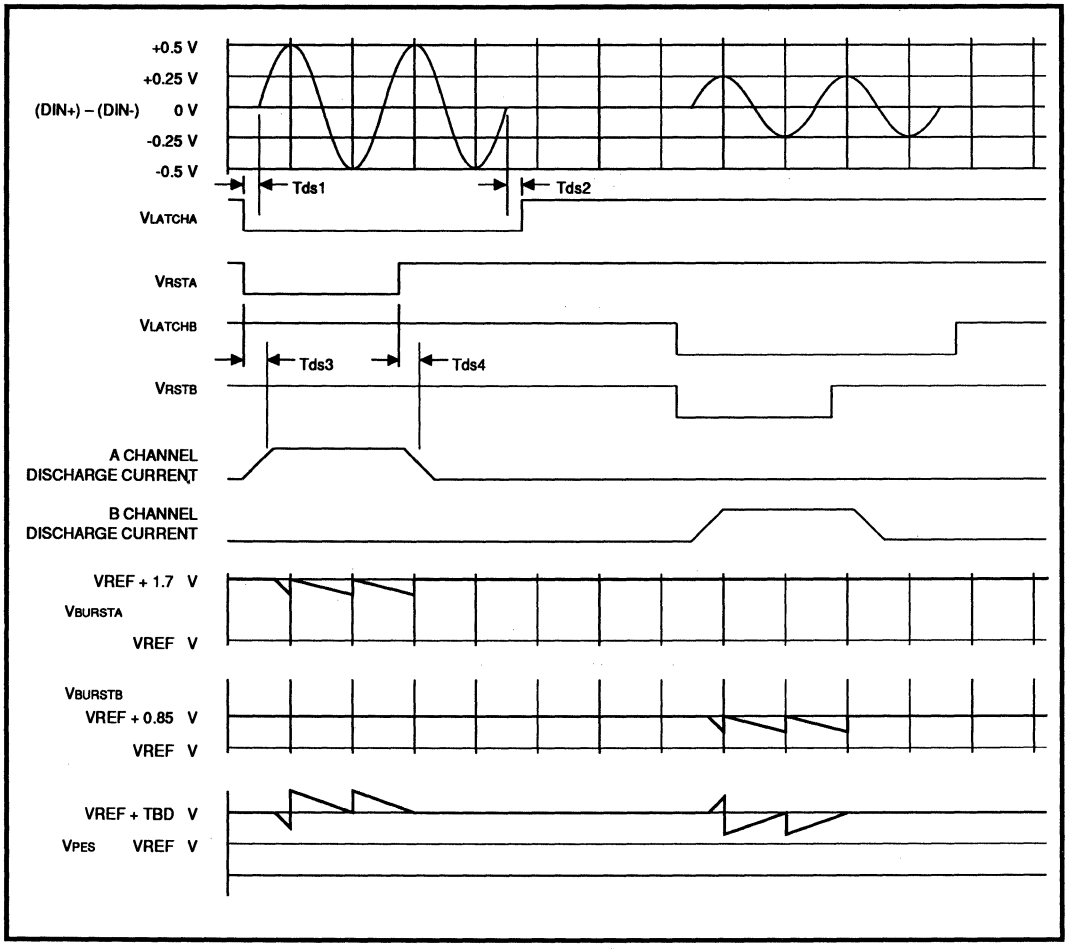



**FIGURE 4: Servo Read Mode II Timing Diagram**

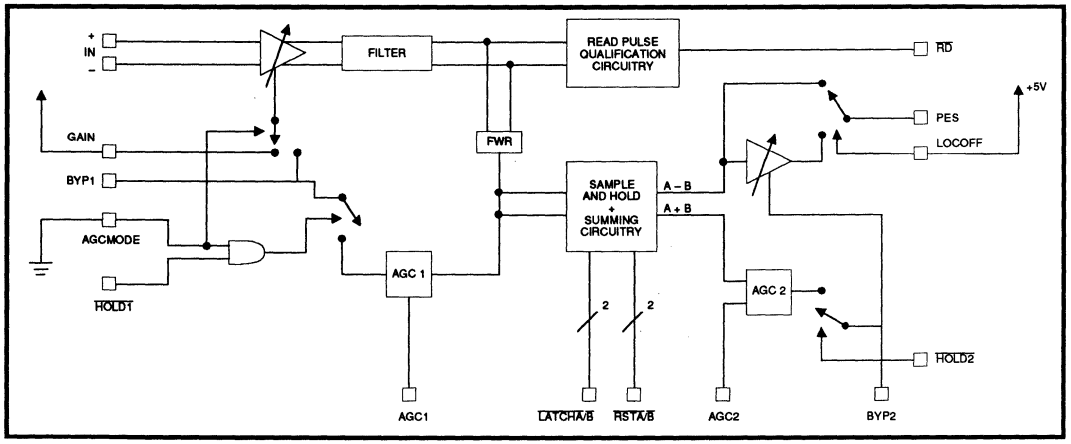



**FIGURE 5: Servo Read Mode III**

## PIN DESCRIPTION

### POWER SUPPLY AND CONTROL

| NAME | DESCRIPTION |
|---|---|
| VCC | 5 volt power supply. |
| VDD | 12 volt power supply. |
| AGND, DGND | Analog and digital ground pins. |
| R/$\overline{W}$* | TTL compatible read/write control pin |
| ENABLE* | TTL compatible power up control pin. A low input selects a low power state. |
| $\overline{VFLT}$ | Open collector output that goes low when a low power supply fault is detected. |

### AGC GAIN STAGE

| | |
|---|---|
| IN+, IN- | Analog signal input pins. |
| OUT+, OUT- | Read path AGC amplifier output pins. |
| AGC1 | Reference input voltage level for the read path AGC loop. |
| AGCMODE* | TTL compatible pin that selects the AGC loop control input. A high selects BYP1, a low GAIN. |
| BYP1 | An AGC timing capacitor or network is tied between this pin and AGND. |
| GAIN | A voltage at this pin may be used to control AGC gain. |
| DECAY | A resistor to control the AGC loop decay time constant may be tied between this pin and BYP1. |
| $\overline{HOLD1}$* | TTL compatible control pin that holds the read path AGC loop gain constant when low. |

* These inputs have internal pull-ups, so an open connection is the same as a high input.

## PIN DESCRIPTION (Continued)

### DIGITAL PROCESSING STAGE

| NAME | DESCRIPTION |
|---|---|
| DIN+, DIN- | Analog input to the hysteresis comparator. |
| CIN+, CIN | Analog input to the differentiator. |
| DIF+, DIF- | Pins for external differentiating network. |
| LEVEL | Output from full wave rectifier that may be used for input to the hysteresis-comparator. |
| HYS | Threshold setting input to the hysteresis-comparator. |
| DOUT | Buffered TTL output for monitoring the flip-flop D input. Provided for testing or servo use. |
| COUT | Test point for monitoring the flip-flop clock input. |
| OS | Connection for output pulse width setting capacitor. |
| $\overline{RD}$ | TTL compatible read output. |

### SERVO BURST CAPTURE STAGE

| | |
|---|---|
| $\overline{LATCHA}$, $\overline{LATCHB}$ | TTL compatible inputs that switch channels A or B into peak acquisition mode when low. |
| HOLDA, HOLDB | Peak holding capacitors are tied from each of these pins to AGND. |
| $\overline{RSTA}$, $\overline{RSTB}$ | TTL compatible inputs that enable discharge of Channel A or B hold capacitors when low. |
| CS | Hold capacitor discharge current magnitude is controlled by a resistor from this pin to ground. |
| VREF | Reference voltage input for servo outputs. |
| AGC2 | Reference input voltage level for the servo AGC loop. |
| BYP2 | An AGC timing capacitor or network is tied between this pin and AGND. |
| $\overline{HOLD2}$ | TTL compatible control pin that holds the servo AGC loop gain constant when low. |
| BURSTA, BURSTB | Buffered hold capacitor voltage outputs. |
| PES | Position error signal A minus B output. |
| LOCOFF* | TTL compatible input to select path for PES signal. (Local On/Off) Selects between AGC amp. output or A-B output. |

* These inputs have internal pull-ups, so an open connection is the same as a high input.

## ELECTRICAL SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS

Operation outside these rating limits may cause permanent damage to this device.

| PARAMETER | RATING | UNIT |
|---|---|---|
| 5V Supply Voltage, VCC | 6.0 | V |
| 12V Supply Voltage, VDD | 14.0 | V |
| Pin Voltage<br>GAIN, BYP1/2, AGC1/2 LEVEL, HYS, HOLDA/B, VREF<br>BURSTA/B, PES, COUT, DIF±, OUT± | -0.3 to VDD + 0.3 | V |
| Pin Voltage<br>IN±, AGCMODE, $\overline{\text{HOLD1/2}}$, ENABLE, R/$\overline{\text{W}}$, $\overline{\text{LATCHA/B}}$,<br>$\overline{\text{RSTA/B}}$, CS, LOCOFF, OS, CIN±, DIN± | -0.3 to VCC + 0.3 | V |
| Pin Voltage<br>RD, DOUT, DECAY, $\overline{\text{VFLT}}$ | -0.3 to VCC + 0.3<br>or +12 mA | V |
| Storage Temperature | 65 to 150 | °C |
| Lead Temperature (Soldering 10 sec.) | 260 | °C |

### RECOMMENDED OPERATING CONDITIONS

Currents flowing into the chip are positive.

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| VCC | Supply Voltage | | 4.5 | 5.0 | 5.5 | V |
| VDD | Supply Voltage | | 10.8 | 12.0 | 13.2 | V |
| Ta | Ambient Temperature | | 0 | | 70 | °C |

### ELECTRICAL CHARACTERISTICS

### POWER SUPPLY

Recommended conditions apply unless otherwise specified.

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|---|
| ICC | VCC Supply Current | Outputs unloaded,<br>ENABLE = high or open | | | 20 | mA |
| ICC | | ENABLE = low | | | 17 | mA |
| IDD | VDD Supply Current | Outputs unloaded,<br>ENABLE = high or open | | | 90 | mA |
| IDD | | ENABLE = low | | | 25 | mA |

**POWER SUPPLY** (Continued)

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|---|
| Pd | Power dissipation | Tj = 145°C, ENABLE = high, Outputs unloaded | | | 1.0 | W |
| | | ENABLE = low, Outputs unloaded | | | 0.35 | W |

**LOGIC SIGNALS**

| | | | | | | |
|---|---|---|---|---|---|---|
| VIL | Input Low Voltage | | -0.3 | | 0.8 | V |
| VIH | Input High Voltage | | 2.0 | | VCC+0.3 | V |
| IIL | Input Low Current | VIL = 0.4V | 0.0 | | -0.4 | mA |
| IIH | Input Low Current | VIH = 2.4V | | | 100 | µA |
| VOL | Output Low Voltage | IOL = 4.0 mA | | | 0.4 | V |
| VOH | Output High Voltage | IOH = 400 µA | 2.4 | | | V |
| | Output rise time | VOH = 2.4V* | | | 15.0 | ns |
| | Output full time | VOL = 0.4V* | | | 9.0 | ns |

*10 - 90%, 10 pF capacitor to DGND

**MODE CONTROL**

| | | | | | |
|---|---|---|---|---|---|
| Enable to/from Disable Transition Time | Settling time of external capacitors not included ENABLE pin high to/from low | | | 10 | µs |
| Read to Write Transition Time | R/$\overline{W}$ pin high to low | | | 1.0 | µs |
| Write to Read Transition Time | R/$\overline{W}$ pin low to high AGC setting not included | 1.2 | | 3.0 | µs |
| AGC On to/from AGC Off Transition Time | AGCMODE pin high to/from low | | | 2.0 | µs |
| $\overline{HOLD1}$ On to/from $\overline{HOLD2}$ Off Transition Time | $\overline{HOLD1}$ pin high to/from low | | | 1.0 | µs |
| $\overline{HOLD2}$ On to $\overline{HOLD2}$ Off Transition Time | $\overline{HOLD2}$ pin high to/from low | | | 1.0 | µs |

**WRITE MODE**

| PARAMETER | CONDITION | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Common Mode Input Impedance | R/$\overline{W}$ pin = low | | 250 | | Ω |

**READ MODE**

**READ PATH AGC AMPLIFIER**

Unless otherwise specified, recommended operating conditions apply. Input signals are AC coupled to IN±. OUT± are loaded differentially with >600Ω, and each side is loaded with < 10 pF to AGND, and AC coupled to DIN±. A 2000 pF capacitor is connected between BYP1 and AGND. AGC1 pin is open. R/$\overline{W}$ is high.

| PARAMETER | CONDITION | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Gain Range | 1.0 Vpp ≤ (OUT+) – (OUT-) ≤ 3.0 Vpp | 4 | | 83 | V/V |
| Output Offset Voltage | Over entire gain range | -400 | | +400 | mV |
| Maximum Output Voltage Swing | Set by BYP1 pin | 3.0 | | | Vpp |
| Differential Input Resistance | (IN+) – (IN-) = 100 mVpp @ 2.5 MHz | | 5.0 | | kΩ |
| Differential Input Capacitance | (IN+) – (IN-) = 100 mVpp @ 2.5 MHz | | | 10 | pF |
| Common Mode Input Impedance | R/$\overline{W}$ = high | | 1.8 | | kΩ |
| | R/$\overline{W}$ = Low | | 250 | | Ω |
| Input Noise Voltage | Gain set to maximum, RS = 0, BW = 15 MHz | | | 30 | nV/$\sqrt{Hz}$ |
| Bandwidth | -3 dB bandwidth at maximum gain | 28 | | | MHz |
| OUT+ to OUT- Pin Current | No DC path to AGND | ±3.0 | | | mA |
| Output Resistance | | 20 | | 50 | Ω |
| CMRR (Input Referred) | (IN+) = (IN-) = 100 mVpp @ 5 MHz, gain set to max | 40 | | | dB |

**READ PATH AGC AMPLIFIER** (Continued)

| PARAMETER | CONDITION | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| PSRR (Input Referred) | VDD or VCC = 100 mVpp @ 5 MHz, gain set to max | 30 | | | dB |
| Externally controlled Gain Constants<br>$AV = K_2 \cdot e^{(K_3 \cdot VGAIN)}$ V/V | $K_2$, AGCMODE = Low<br>$K_3$, AGCMODE = Low | .89<br>1.95 | | 2.3<br>2.64 | |
| Gain pin parasitic Input current | AGCMODE & $\overline{HOLD1}$ = low | 0.2 | | +0.2 | µA |
| (DIN+) – (DIN-) Input Swing vs. AGC1 Input | 30 mVpp ≤ (IN+) – (IN-) ≤ 550 mVpp<br>0.5 Vpp ≤ (DIN+) – (DIN-) ≤ 1.5 Vpp, AGCMODE & $\overline{HOLD1}$ = high | 0.36 | | 0.56 | Vpp/V |
| (DIN+) – (DIN-) Input Voltage Swing Variation | 30 mVpp ≤ (IN+) – (IN-) ≤ 550 mVpp | | | 8.0 | % |
| AGC1 Voltage | AGC1 open, $V_{(ACC1)}$ = 2.35V | -5 | | +5 | % |
| AGC1 Pin Input Impedance | | 5.0 | | 8.3 | kΩ |
| Fast Decay Threshold (DIN+) – (DIN-) | AGCMODE = high | | ±0.3 | | V |
| Slow AGC Capacitor Discharge Current | (DIN+) – (DIN-) = 0V<br>$V_{BYP}$ = 4.5V | | 4.0 | | µA |
| AGC Capacitor Leakage Current | AGCMODE = high, $\overline{HOLD1}$ = low, 2.5V < $V_{BYP}$ < 5.5V | -0.2 | | +0.2 | µA |
| Slow AGC Capacitor Charge Current | (DIN+) – (DIN-) = 0.75 VDC, vary AGC1 until slow charge begins | -0.14 | | -0.22 | mA |
| Fast AGC Capacitor Charge Current | (DIN+) – (DIN-) = 0.75 VDC, $V_{AGC1}$ = 3.0V | -1.3 | | -2.0 | mA |
| Fast to Slow Attack Switchover Point | [(DIN+) – (DIN-)] – [(DIN+) – (DIN-)]FINAL | | 0.2 | | Vpp |
| Gain Decay Time (Td) (See Figure 6a) | (IN+) – (IN-) = 300 mVpp to 150 mVpp @ 2.5 MHz DECAY pin open, (OUT+) – (OUT-) to 90% final value. | | 50 | | µs |

**READ PATH AGC AMPLIFIER** (Continued)

| PARAMETER | CONDITION | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Gain Attack Time (Ta)<br>(See Figure 6b) | R/$\overline{W}$ = low to high<br>(IN+) – (IN-) = 400 mVpp<br>@ 2.5 MHz, (OUT+) – (OUT-)<br>to 110% final value | | 4 | | µs |

**HYSTERESIS COMPARATOR**

Unless otherwise specified, recommended operating conditions apply. Input (DIN+) – (DIN-) is an AC coupled, 1.0 Vpp, 2.5 MHz sine wave. 1.8 VDC is applied to the HYS pin. ENABLE and R/$\overline{W}$ pins are high.

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Input Signal Range | | | | 1.5 | Vpp |
| Differential Input Resistance | (DIN+) – (DIN-) = 100 mVpp<br>@ 2.5 MHz | 10 | | 18.0 | kΩ |
| Differential Input Capacitance | (DIN+) – (DIN-) = 100 mVpp<br>@ 2.5 MHz | | | 4.0 | pF |
| Common Mode Input<br>Impedance (Both Sides) | | 2.25 | | 5.0 | kΩ |
| Level Pin Output Voltage<br>vs. (DIN+) – (DIN-) | 0.6 Vpp < (DIN+) – (DIN-)<br>< 1.5 Vpp, 10K between<br>LEVEL and AGND | 1.2 | | 2.2 | V/Vpp |
| Level Pin Output Impedance | $I_{LEVEL}$ = 0.5 mA | | 180 | | |
| Level pin Maximum<br>Output Current | | 3.0 | | | mA |
| Hysteresis Voltage at DIN±<br>vs. HYS Pin Voltage | 1 V < HYS < 3V | 0.16 | | 0.25 | V/V |
| Hysteresis threshold margin as<br>a % of V(DIN+) – (DIN-) peak | V(HYS) = some % of<br>*V(AGC) or V(LEVEL)<br>1V < V(HYS) < 3V<br>*see Figures 8 & 9 | -15 | | +15 | %Peak |
| HYS Pin Current | 1 V < HYS < 3V | 0.0 | | -20 | µA |
| Comparator Offset Voltage | HYS pin at AGND<br>≤ 1.5 kΩ across DIN± | | | 10.0 | mV |

* In an open loop configuration where reference is V(AGC) tolerance can be slightly higher.

**ACTIVE DIFFERENTIATOR**

Unless otherwise specified, recommended operating conditions apply. Input (CIN+) – (CIN-) is an AC-coupled, 1.0 Vpp, 2.5 MHz sine wave. 100Ω in series with 65 pF are tied from DIF+ to DIF-.

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Input Signal Range | | | | 1.5 | Vpp |
| Differential Input Resistance | (CIN+) – (CIN-) = 100 mVpp @ 2.5 MHz | 10 | | 18.0 | kΩ |
| Differential Input Capacitance | (CIN+) – (CIN-) = 100 mVpp @ 2.5 MHz | | | 4.0 | pF |
| Common Mode Input Impedance | Both sides | 2.25 | | 5.0 | kΩ |
| Voltage Gain From CIN± to DIF± | (DIF+ to DIF-) = 2 kΩ | 1.7 | | 2.2 | V/V |
| DIF+ to DIF- PIn Current | Differentiator impedance must be set so as to not clip the signal for this current level | ±1.2 | | | mA |
| Comparator Offset Voltage | DIF+, DIF- are AC-coupled | | | 10.0 | mV |
| COUT Pin Output Low Voltage | 0 ≤ IOL ≤ 0.5 mA | | VDD-3.0 | | V |
| COUT pin Output Pulse Voltage, $V_{HIGH}$ - $V_{LOW}$ | 0 ≤ IOL ≤ 0.5 mA | | 0.4 | | V |
| COUT pin Output Pulse Width | 0 ≤ IOH ≤ 0.5 mA | | 30 | | ns |

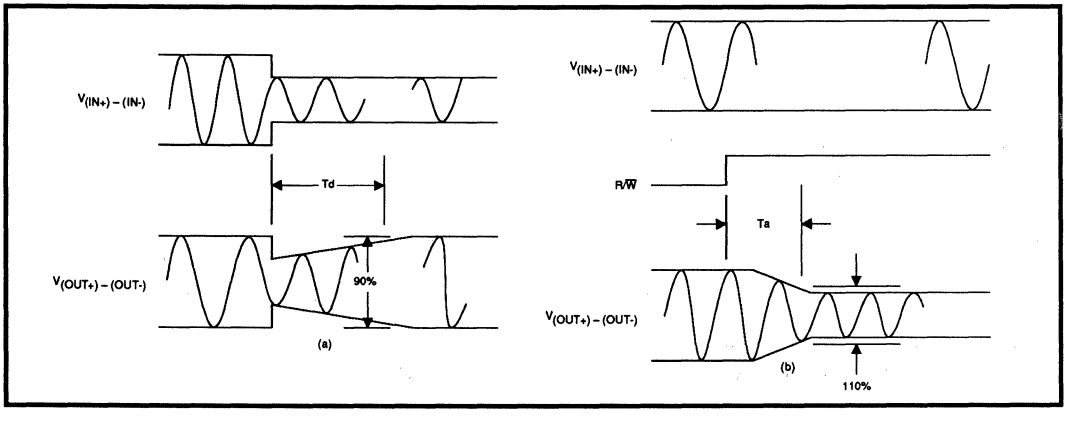



**FIGURE 6: AGC Timing Diagram**

**OUTPUT DATA CHARACTERISITICS** (See Figure 7)

Unless otherwise specified, recommended operating conditions apply. Inputs (CIN+) – (CIN-) and (DIN+) – (DIN-) are in-place as a coupled, 1.0 Vpp, 2.5 MHz sine wave. 100Ω in series with 65 pF are tied from DIF+ to DIF-. 1.8V is applied to the HYS pin. A 60 pF capacitor is tied between OS and VCC. $\overline{RD}$ is loaded with a 4 kΩ resistor to VCC and a 10 pF capacitor to DGND. ENABLE and R/$\overline{W}$ pins are high.

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| Td1 | D Flip-Flop Set Up Time | Minimum allowable time delay from (DIN+) – (DIN-) exceeding hysterisis point to (DIF+) – (DIF-) hitting a peak value. | 0 | | | ns |
| Td3 | Propagation Delay | | | | 110 | ns |
| Td5 | Output Pulse Width Variation | Td5 = 800(Cos) @ $V_{RD}$ = 1.4V<br>50 pF ≤ Cos ≤ 200 pF | | | ±15 | % |
| \|Td3-Td4\| | Pulse Pairing | | | | 1.5 | ns |

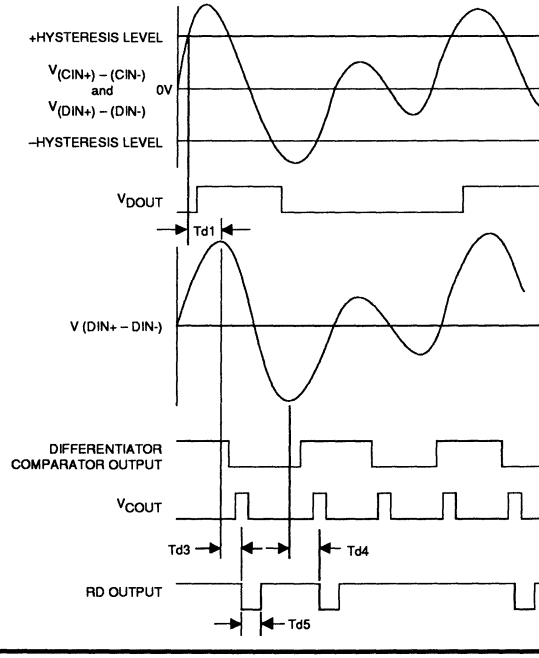



**FIGURE 7: Read Mode Digital Section Timing Diagram**

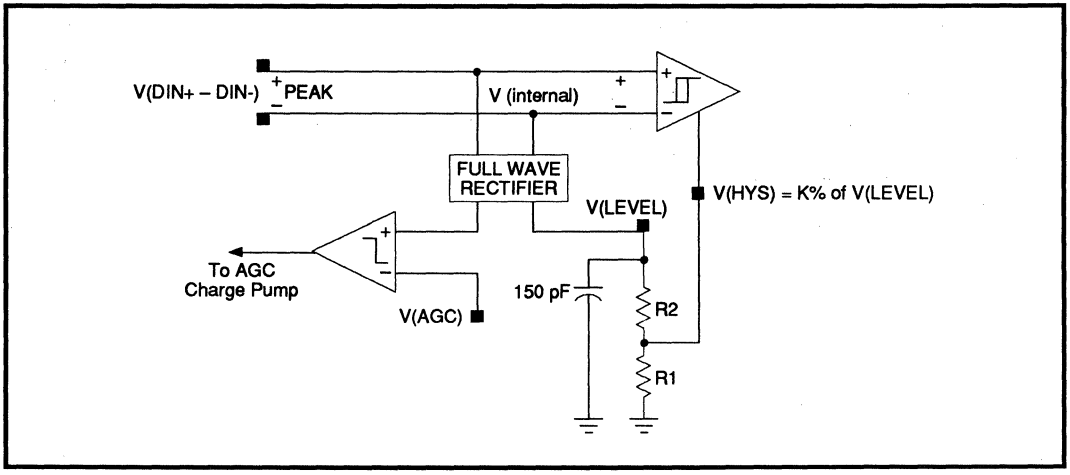



**FIGURE 8: Feed Forward Mode**

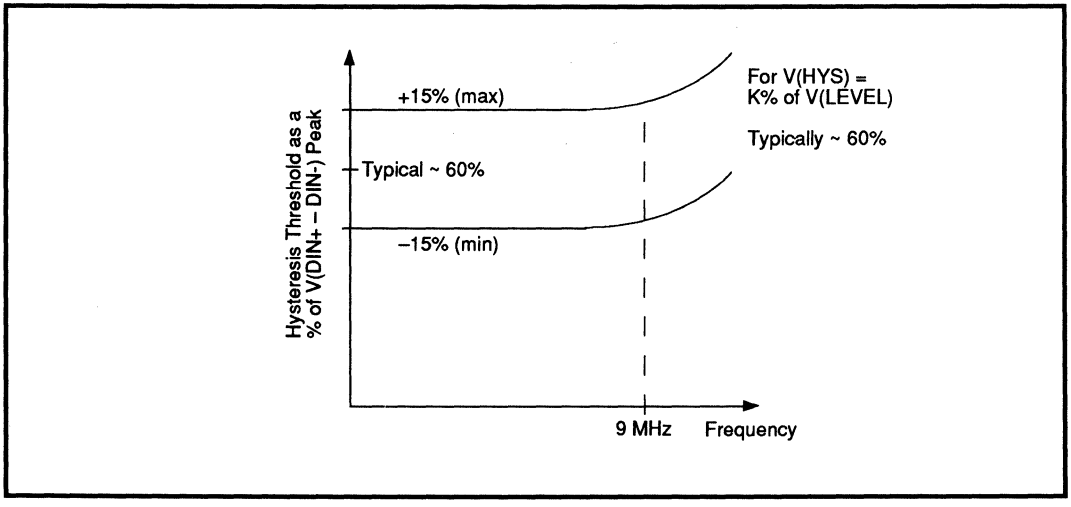



**FIGURE 9: Percentage Threshold vs. Frequency**

**SERVO SECTION** (Unless otherwise specified, recommended operating conditions apply.)

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| VREF Voltage Range | | 3.9 | | 6.0 | V |
| AGC2 Pin Voltage | AGC2 Pin Open, $V_{(AGC2)}$ = 3.4V | -5 | | +5 | % |
| AGC2 Pin Input Impedance | | 5.0 | | 9.1 | kΩ |
| BURSTA/B pin Output Voltage vs (DIN+) – (DIN-) | $\overline{LATCHA/B}$ = Low<br>$\frac{V_{BURSTA/B} - VREF}{(DIN+) - (DIN-)}$ = 1.7 V/Vp-p | -6.5 | | +6.5 | % |
| BURSTA/B Output Offset Voltage $V_{BURST}$ - VREF | $\overline{LATCHA/B}$ = Low, (DIN+) = (DIN-), RCS = 38.3 kΩ | -80 | | +80 | mV |
| BURSTA - BURSTB Output Offset Match | $\overline{LATCHA/B}$ = low (DIN+) = (DIN-) | -15 | | +15 | mV |
| Maximum PES Pin Output Voltage | Controlled by AGC2 | | | 5.0 | Vpp |
| PES Pin Output Offset Voltage | $V_{PES}$ - VREF, (DIN+) = (DIN-) $\overline{LATCHA/B}$ = Low After 30 sec. temp. stable | -50 | | +50 | mV |
| Output Resistance, BURSTA/B & PES pins | | | | 20 | Ω |
| Hold A/B Charge Current | $\overline{LATCHA/B}$ = Low | 25 | | | mA |
| HOLDA/B Discharge Current Tolerance | $\overline{RSTA/B}$ = Low, ICS = 2.6V/(RSC + 750Ω) | -15 | | +15 | % |
| | $\overline{RSTA/B}$ = High, $\overline{LATCHA/B}$ = High | -0.5 | | +0.5 | µA |
| Load Resistance BURSTA/B, PES pins | Resistors to VREF | 10.0 | | | kΩ |
| Load Capacitance BURSTA/B, PES pins | | | | 20 | pF |
| $\overline{LATCHA/B}$ pin set up time | (Tds1 in Figures 3 & 4) | 150 | | | ns |
| $\overline{LATCHA/B}$ pin Hold Time | (Tds2 in Figures 3 & 4) | 150 | | | ns |
| Channel A/B Discharge Current Turn On time | (Tds3 in Figures 3 & 4) | | | 150 | ns |
| Channel A/B discharge Current Turn Off time | (Tds4 in Figures 3 & 4) | | | 150 | ns |
| BYP2 Pin Parasitic Input Current | $\overline{HOLD2}$ = Low<br>LOCOFF = Low<br>LOCOFF = High | <br>-0.02<br>-9.0 | | <br>+0.02<br>+9.0 | <br>µA<br>µA |

**SERVO SECTION** (Continued)

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| BYP2 Pin Charge/Discharge Current<br>$I_C = K_4[(K_5 \cdot V_{AGC2}) - V_{A(DIN)pp} - V_{B(DIN)pp}]$ | $K_4$, $\overline{HOLD2}$ = High | 487 | 650 | 813 | µA/Vpp |
| | $K_5$, $\overline{HOLD2}$ = High | 0.35 | | 0.43 | V/V |
| *AGC Gain Range | LOCOFF=Low | 0.6 | | 6.0 | V/Vpp |
| $V_{PES}$ pp vs. $V_{AGC2}$ | $V_{PES}$ pp/$V_{AGC2}$<br>LOCOFF = Low | 1.24 | 1.38 | 1.52 | Vpp/V |
| | LOCOFF = High | 1.42 | 1.5 | 1.58 | |
| | $V_{PES}$ pp/$V_{AGC2}$<br>AGC2=Open<br>LOCOFF = Low | 5.03 | 5.3 | 5.56 | Vpp<br>Vpp/V |
| | LOCOFF = High | 5.32 | 5.6 | 5.88 | |
| BURSTA/B Pin Output vs. $V_{AGC2}$ | $(V_A + V_B - 2VREF)/V_{AGC2}$<br>LOCOFF = High | | 0.77 | | V/V |
| | $V_A + V_B$ - 2VREF,<br>AGC2=Open<br>LOCOFF = High | | 2.85 | | V |

*$A_V$ = (VPES - VREF)/($V_{A(DIN)pp}$ + $V_{B(DIN)pp}$)

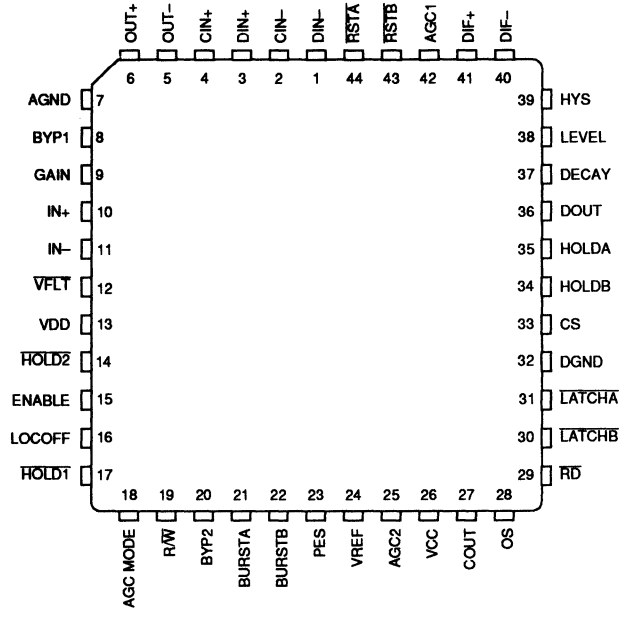
**Supply Voltage Fault Detection**

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| VDD Fault Threshold | | 9.1 | | 10.5 | V |
| VCC Fault Threshold | | 4.1 | | 4.4 | V |
| VOL Output Low | 4.5 < VCC < 5.5V,<br>IOL = 1.6 mA | | | 0.4 | V |
| | 1.0 < VCC < 4.5,<br>IOL = 0.5 mA | | | 0.4 | V |
| IOH Output High Current | | | | 25 | µA |

## PACKAGE PIN DESIGNATIONS
(Top View)

**Thermal Characteristics: θjA**

| | |
|---|---|
| 44-lead PLCC | 60° C/W |




**44-Lead PLCC**

CAUTION: Use handling procedures necessary for a static sensitive component.

## ORDERING INFORMATION

| PART DESCRIPTION | ORDER NO. | PKG. MARK |
|---|---|---|
| SSI 32P544 - 44-Lead PLCC | 32P544-CH | 32P544-CH |



Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 573-6000, FAX (714) 573-6914

**Notes:**

silicon systems®
A TDK Group Company

# SSI 32P547
## High Performance Pulse Detector

2

December 1992

## DESCRIPTION

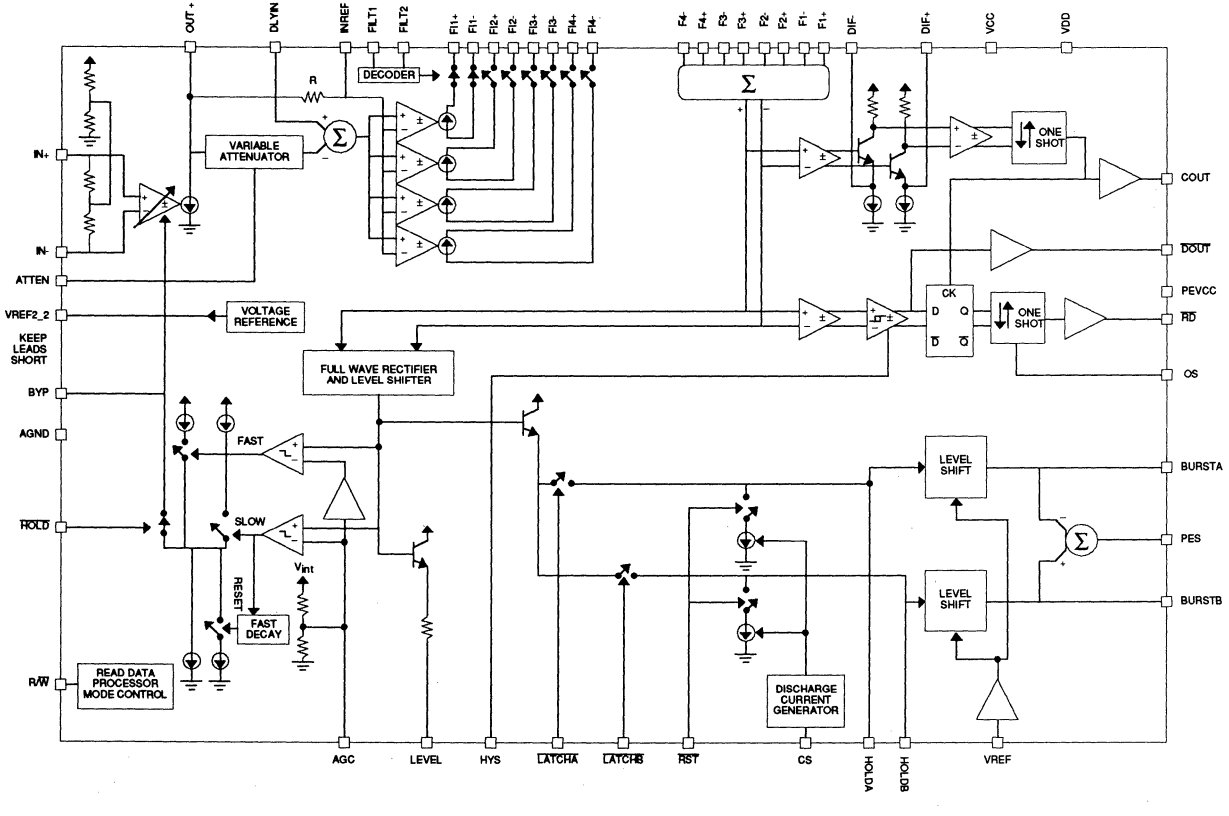
The SSI 32P547 Read Data Processor and Servo Demodulator with Variable Pulse Slimming and Zone Filter Mux is a fully integrated bipolar circuit that detects and validates amplitude peaks in the output from a disk drive read amplifier, as well as detecting embedded servo information to provide position error signals used for read head positioning.

Time and amplitude qualification are used to provide a PECL output that accurately duplicates the time position of input signal peaks. An AGC control loop, using a dual rate charge pump, provides a constant input amplitude for the level qualifier.

## FEATURES

- **Wide bandwidth AGC input amplifier**
- **Uses standard +12V and +5V ± 10% supplies**
- **Level qualification supports MFM or RLL codes**
- **Servo burst capture circuit for use in embedded servo**
- **Four input differential filter MUX**
- **Pulse Slimming with Variable Attenuation**

## BLOCK DIAGRAM



## CIRCUIT OPERATION

Level qualification can be implemented as fixed threshold or a constant percentage that tracks signal amplitude that enhances qualification during AGC loop transients.

The Servo Demodulator consists of two peak detector channels that capture rectified servo data peaks. Buffered individual channel outputs are provided along with a difference output.

The SSI 32P547 requires standard ±10% tolerance +5V and +12V supplies and is available in a 52-pin Quad PLCC package.

### MODE CONTROL

The circuit mode is controlled by the R/$\overline{W}$, and $\overline{HOLD}$ as shown in Table 1.

### READ MODE

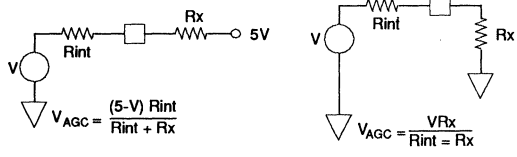
The circuit is placed in the read mode when the R/$\overline{W}$ pin is high or open and is disabled (write mode) when the R/$\overline{W}$ pin is low. In the write mode the digital circuitry is disabled, the AGC amplifier gain is set to maximum and the input impedance of the input analog stage is reduced to allow more rapid settling of the input coupling capacitors from the read/write circuit (such as the SSI 32R510A) upon transition to the read mode. Write to read transition timing is controlled to allow settling of the coupling capacitors between the read/write circuit and the SSI 32P547 before the AGC circuitry is activated when going to the read mode. Coupling capacitors should be chosen with as low a value as possible consistent with adequate bandwidth to allow for more rapid settling. When the R/$\overline{W}$, and $\overline{HOLD}$ pins are high or open the input amplifier is in the read data AGC mode and gain is controlled to keep a constant read data peak level. When the $\overline{HOLD}$ pin is pulled low the gain of the analog circuit is held at the level determined when the $\overline{HOLD}$ pin was high (the gain will slowly drift due to leakage).

### READ DATA AUTOMATIC GAIN CONTROL CIRCUIT

In this mode an amplified head output signal, such as the output of the SSI 32R117, 32R501, or 32R510A read/write circuits, is AC coupled to the IN+ and IN- inputs. In the read mode the level at the Fx +/- pins is controlled by full wave rectifying the level at the summer output and comparing it to a reference level supplied at the AGC pin. When the input level at the filter outputs is greater than 125% of the desired level as set by the AGC pin, the circuit is in a fast attack mode and will supply about 1.8 mA of charging current at the BYP pin. When the input level is between 125% and 100% of the desired level, the circuit enters a slower attack mode and will supply about 0.18 mA of charging current. This allows the AGC to rapidly recover when going from write to read but reduces zero crossing distortion once the AGC amplifier is in range.

To reduce the effect of gain attack overshoot on settling time (due to offsets) a fast decay mode is entered if slow decay mode exceeds 1.6 µsec (nom). Fast decay discharge current is 0.8 mA and slow decay discharge current is 4.5 µA.

The AGC pin is internally biased so that the level at the filter input pins is 0.83 Vpp. The level at the filter input pins can be increased by tying a resistor from the AGC pin to VCC or reduced by tying a resistor from the AGC pin to GND.




Where:

V = Voltage at AGC with pin open (2.4V, nom.)

Rint = AGC pin input impedance (6.7 KΩ, typ.)

Rx = External resistor.

The new DIN+/- input target level is nominally 0.43 Vp-p/$V_{AGC}$.

Gain of the AGC section in the AGC mode is approximately: $\left(\frac{Av1}{Av2}\right) = \exp\left[6.9 \times (V2 - V1)\right]$

Where:

Av1, Av2 are initial and final amplifier gains. V1, V2 are initial and final voltages on the BYP pin.

### READ DATA PULSE SLIMMING CIRCUIT

The Pulse Slimming Circuit uses an external delay line and an analog controllable Variable Attenuator to implement pulse slimming. Input biasing for this stage is accomplished by low pass filtering the signal at the

OUT+ pin with an on chip resistor and external capacitor tied to the INREF pin and using that signal as a reference to the single-ended-to-differential gain stage which follows.

$$\text{Freq}(-3\text{dB}) = \frac{1}{2\pi RC}$$

Where: R (lowpass) is the on-chip resistor = 6 kΩ nom
C (ext) is the external capacitor

The ratio between the gains of the attenuated and non-attenuated signal paths (K) is controlled by varying the gain of the on-chip attenuator:

K = Av (attenuated) / Av (non-attenuated)
= Ko - G x V (ATTEN) / VREF2_2

Where G is the gain factor, V (ATTEN) is the voltage applied to the ATTEN pin. VREF2_2 is the voltage on the VREF2_2 pin and Ko is the value for K when V(ATTEN) = 0.0V.

## SELECTABLE EXTERNAL FILTER DRIVER/RECEIVER

The on-chip circuitry allows four separate filters to be used for support of constant density recording. A filter is selected by using the two TTL input filter select pins; FILT1, and FILT2. Filter selection is as follows:

| Filter1 | Filter 2 | Channel |
|---|---|---|
| 0 | 0 | FI1 |
| 0 | 1 | FI2 |
| 1 | 0 | FI3 |
| 1 | 1 | FI4 |

## READ MODE DIGITIZING SECTION

In the data path the signal is sent to a hysteresis comparator. The comparator hysteresis level can be set at a fixed level or, with the addition of an external filter network, a fraction of the signal level.

The latter approach allows setting the AGC circuit decay and slow attack times slow enough to minimize distortion of the signal going into the clocking path and setting a short time constant for the hysteresis level. Thus when switching to a head with a different output level or when switching from write to read the circuit is properly decoding data before the AGC circuit gain has settled to its final steady state value. The output of the hysteresis comparator is the "D" input of a D flip-flop. The $\overline{\text{DOUT}}$ pin provides a PECL comparator output digital signal for testing purposes and, if required, for use in the servo circuit.

In the clocking path the signal is sent to a differentiator circuit whose characteristics are set by external components. The differentiator transfer expression from Fx+/- to the comparator input (which is not the DIF+/- output) is:

$$Av = \frac{-2C_{ex}R_i s}{2L_{ex}C_{ex}s^2 + C_{ex}(R_{ex} + 2R_e)s + 1}$$

Where: $R_i$= on chip resistors = 1.0 KΩ nominally; $R_e$= emitter resistance seen at DIF+ or DIF- = 46 Ω nominally; $C_{ex}$= external capacitor, allowable range is 20 pF to 150 pF; $R_{ex}$= external resistor; $L_{ex}$= external inductor.

The output of the differentiator circuit is sent to the edge trigger circuit which creates an output pulse on every zero crossing of the output of the differentiator. The output of the edge trigger is the clock input of the D flip-flop. During normal system operation the differentiator circuit clocks the D flip-flop once every positive and negative peak of the input signal.

The data path D input to the flip-flop only changes state when the signal applied to the filter inputs exceeds the hysteresis comparator threshold in a polarity opposite the polarity of the peak which last exceeded the threshold. Therefore, the clocking path determines signal timing and the data path blocks spurious peaks if they do not exceed the hysteresis comparator threshold. Figure 6 shows circuit operation of the digital section. The two digital signal path delays between the Fx+ and Fx- inputs to the flip-flop clock and data inputs are well matched.

## SERVO BURST CAPTURE SECTION

Rectified servo data peaks are latched into the A or B servo channels by pulling the TTL compatible inputs $\overline{\text{LATCHA}}$ or $\overline{\text{LATCHB}}$ low, respectively. A chip-generated discharge current is turned on for channels A or B by pulling the TTL compatible input $\overline{\text{RST}}$ low. The magnitude of this discharge current is set by a resistor tied to the CS pin.Outputs of the BURSTA, BURSTB, and PES are referenced to an externally generated reference applied at the VREF pin.

## PIN DESCRIPTIONS

### POWER SUPPLY AND CONTROL

| NAME | I/O | DESCRIPTION |
|---|---|---|
| VCC | | 5 Volt power supply. |
| PEVCC | | Collector of PECL emitter follower output which is to be connected to the 5 volt power supply. |
| VDD | | 12 volt power supply |
| AGND | | Analog ground pin |
| R/$\overline{W}$ | I | TTL compatible read/write control pin |

### AGC GAIN STAGE

| | | |
|---|---|---|
| IN+,IN- | | Analog signal input pins |
| OUT+ | | Transconductance output for the AGC amplifier and input to the variable attenuator |
| DLYIN | | Delayed input signal to the pulse slimming amplifier |
| INREF | | Reference DC voltage to the single ended to differential gain stage |
| VREF2_2 | | Internally generated voltage used as a reference by the external DAC used to control the attenuator gain |
| BYP | | The AGC timing capacitor is tied between this pin and AGND |
| $\overline{HOLD}$ | I | TTL compatible control pin which holds the input AGC amplifier AGC level when pulled low |
| ATTEN | | An Analog input which controls the attenuation value for the Variable Attenuator |
| AGC | | Reference input voltage for the AGC circuit |

### SERVO BURST CAPTURE STAGE

| | | |
|---|---|---|
| $\overline{LATCHA}$<br>$\overline{LATCHB}$ | I | TTL inputs which initiates capture of a servo burst<br>Peak on channel A or B when pulled low |
| HOLDA<br>HOLDB | | Peak holding capacitors are tied from each pin to GND |
| $\overline{RST}$ | I | TTL input which initiates discharge of channel A and B hold capacitors when pulled low |
| CS | | Pin to control magnitude of discharge current during active discharge of channel A and B hold capacitors |
| VREF | | Reference level for servo circuit |
| BURSTA<br>BURSTB | | Buffered burst peak outputs |
| PES | | BURST B minus BURST A output |

**DIGITAL PROCESSING STAGE**

| NAME | I/O | DESCRIPTION |
|---|---|---|
| FIx±<br>Fx± | | Differential filter I/O pins for the four external filters |
| FILT1<br>FILT2 | I | TTL compatible inputs to control multiplexer for selection of 1 of 4 filters |
| HYS | | Hysteresis level setting input to the hysteresis level detect comparator |
| LEVEL | | Provides rectified signal level for input into the hysteresis circuit |
| $\overline{DOUT}$ | O | A Pseudo ECL D input into D flip-flop provided for testing or servo use |
| DIF+,DIF- | | Pins for external differentiator components |
| COUT | O | Clock input into D flip-flop provided for testing |
| OS | | Pin for external capacitor in the one shot which determines read channel output one-shot pulse width |
| $\overline{RD}$ | O | A Pseudo ECL (PECL) read output |

**TABLE 1: Mode Control**

| MODE | R/$\overline{W}$ | $\overline{HOLD}$ | CONDITIONS |
|---|---|---|---|
| Read/AGC | 1 | 1 | Read amp on, AGC active and controlled by data, Digital section active |
| Read/Hold | 1 | 0 | Read amp on at fixed gain, AGC level held constant Digital section active |
| Write | 0 | - | Read amp on with reduced input impedance AGC level pulled low, Digital section deactivated, BYP pin set for maximum AGC gain |

## ELECTRICAL SPECIFICATIONS

**ABSOLUTE MAXIMUM RATING**

Operation above absolute maximum ratings may permanently damage the device.

| PARAMETER | RATING | UNITS |
|---|---|---|
| +5V Supply Voltage,VCC, PEVCC | 6.0 | V |
| +12V Supply Voltage,VDD | 14.0 | V |
| Pin Voltage<br>BYP, AGC, LEVEL, HYS, HOLD A/B,<br>VREF, BURST A/B, PES, DIF+/-, FIx± | -0.3 to VDD+0.3 | V |
| Pin Voltage<br>IN+/-, $\overline{HOLD}$, R/$\overline{W}$, $\overline{RST}$, ATTEN,<br>$\overline{LATCHA/B}$, CS, OS, FILT1-2,<br>Fx±, OUT+, DLYIN, INREF, VREF2_2 | -0.3 to VCC+0.3 | V |

**ABSOLUTE MAXIMUM RATING** (continued)

| PARAMETER | RATING | UNITS |
|---|---|---|
| $\overline{RD}$, $\overline{DOUT}$, COUT | -0.3 to VCC+0.3 or +12mA | V |
| Storage Temperature | -65 to +150 | °C |
| Lead temperature (soldering 10 sec) | 260 | °C |

**RECOMMENDED OPERATING CONDITIONS**

Currents flowing into the chip are positive.

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| VCC | Supply Voltage | | 4.5 | 5.0 | 5.5 | V |
| VDD | Supply Voltage | | 10.8 | 12.0 | 13.2 | V |
| Tj | Junction Temperature | | 25 | | 145 | C |
| Ta | Ambient Temperature | | 0 | | 70 | C |

**ELECTRICAL CHARACTERISTICS**

**POWER SUPPLY**

Recommended conditions apply unless otherwise specified.

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| ICC | VCC Supply Current | Outputs unloaded | | | 50.0 | mA |
| IDD | VDD Supply Current | Outputs unloaded | | | 80.0 | mA |
| Pd | Power dissipation | Ta=70° C<br>Outputs unloaded | | | 1.25 | W |

**MODE CONTROL**

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|
| Read-to-Write Transition time | R/$\overline{W}$ Pin High → Low | | | 1.0 | µs |
| Write to Read Transition time | R/$\overline{W}$ Pin Low → High<br>AGC settling not included | 1.2 | | 3.0 | µs |
| Hold On ↔ Hold off Transition time | $\overline{HOLD}$ Pin High ↔ Low<br>R/$\overline{W}$ Pin High | | | 1.0 | µs |

**LOGIC SIGNALS** ($\overline{HOLD}$, FILT1-2, R/$\overline{W}$, $\overline{LATCHA}$,$\overline{B}$, $\overline{RST}$ Pins)

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|---|
| VIL | Input Low Voltage | | -0.3 | | 0.8 | V |
| VIH | Input High Voltage | | 2.0 | | VCC+0.3 | V |
| IIL | Input Low Current | VIL = 0.4V | 0.0 | | * -0.4 | mA |
| IIH | Input High Current | VIH = 2.4V | | | 100 | µA |

*For $\overline{RST}$ only, limit is -0.8 mA

**PECL OUTPUT: $\overline{RD}$, $\overline{DOUT}$ PINS**

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|
| Output Low Voltage | | | | VCC-1.625 | V |
| Output High Voltage | | VCC-1.02 | | | V |
| Output Rise Time | 10 to 90 % | | | 5.0 | ns |
| Output Fall Time | 90 to 10 % | | | 5.0 | ns |

*Output load is a 2.5 kΩ resistor to GND, and a 5 pF capacitor to ground.

**AUTOMATIC GAIN CONTROL CIRCUIT**

All of the measurements in the AGC gain mode are made with the following conditions unless otherwise stated:

1. The circuit is in the read mode (R/$\overline{W}$, and $\overline{HOLD}$ pins high).
2. The circuit is connected as in Figure 5.
3. The amplifier inputs, IN+ and IN- , are AC coupled.
4. The OUT+ pin is loaded with 100 Ω to Vcc and Fx+, Fx- 200Ω each to VDD (through series capacitors).
5. A 1000 pF capacitor is tied between BYP and GND.
6. The AGC pin is left open.

**READ DATA MODE**

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Slow AGC Capacitor Discharge Current | V(Fx+ - Fx-)=0.0 Volts Vary V(AGC) until slow discharge begins | | 4.5 | | µA |
| Fast AGC Capacitor Discharge Current | V(Fx+ - Fx-)=0.0 Volts Vary V(AGC) until fast discharge begins | | 0.8 | | mA |
| Fast Decay Hold Off Time | Slow Attack Threshold Not Reached | 0.7 | 1.6 | 3.0 | µs |
| AGC Capacitor Leakage Current | R/$\overline{W}$ pin high, $\overline{HOLD}$ low | -0.2 | | 0.2 | µA |

**ELECTRICAL CHARACTERISTICS** (continued)

**READ DATA MODE** (continued)

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Slow AGC Capacitor Charge Current | V(Fx+ - Fx-)=0.41 Vdc, Vary V(AGC) until slow charge begins | -0.14 | | -0.22 | mA |
| Fast AGC Capacitor Charge Current | V(Fx+ - Fx-)=0.8 Vdc Vary AGC until fast charge begins | -1.3 | | -2.0 | mA |
| Fast → Slow Attack Switchover Point | Minimum V(Fx ±) in fast attack mode; Minimum V(Fx ±) in slow attack mode | | 0.15 | | V |
| Gain Attack Time (Ta) See Fig. 1 | R/$\overline{W}$ = low → high, changing Vin from 200 to 400 mVpp @ 2.5 MHz, V(Fx±) to 110% of final value | | 4 | | µs |
| Fx+ - Fx- Input Voltage Swing vs AGC Input Voltage | 15 mVpp < V(IN+ - IN-) < 250 mVpp, 0.4 Vpp < V(Fx+ - Fx-) < 1.25 Vpp, V(ATTEN) = V(VREF2_2) | 0.25 | | 0.48 | Vpp/V |
| Fx+ - Fx- Input Voltage Swing Variation | 15 mVpp < V(IN+ - IN-) < 250 mVpp 0.4 Vpp < V(Fx+ - Fx-) < 1.25 Vpp | | | 8.0 | % |
| AGC Pin Input Impedance | | 5.0 | | 8.3 | kΩ |
| AGC Pin Voltage | AGC pin open | 2.28 | 2.4 | 2.52 | V |

**AGC AMPLIFIER CHARACTERISTICS**

| | | | | | |
|---|---|---|---|---|---|
| Gain Range | Z Load = 100Ω | 0.3 | | 16.5 | V/V |
| Output DC Voltage Variation | V(IN+) = V(IN-); over actual gain range | | | ±150 | mV |
| Maximum Allowable Output Voltage Swing on OUT+ pin | | | | 360 | mVpp |
| Differential Input Resistance | V(IN+ - IN-)=100 mVpp @ 2.5 MHz | | 5.0 | | kΩ |
| Differential Input Capacitance | V(IN+ - IN-)=100 mVpp @ 2.5 MHz | | | 10.0 | pF |
| Common Mode Input Impedance | R/$\overline{W}$ pin = high | | 1.8 | | kΩ |
| (Both Sides) | R/$\overline{W}$ pin = low | | 250 | | Ω |
| Input Noise | Gain set to 16 V/V, RS = 0, BW = 15 MHz | | | 25 | $\frac{nV}{\sqrt{(Hz)}}$ |

**AGC AMPLIFIER CHARACTERISTICS** (continued)

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Bandwidth | Transconductance (Iout/Vin) ± 3 dB bandwidth, referenced to 2.5 MHz | 40 | | | MHz |
| Common Mode Rejection Ratio (Input Referred) | V(IN+) = V(IN-) = 100 mV, 5 MHz, gain set to 16 V/V | 40 | | | dB |
| Output DC Current on OUT+ Pin | IN+, IN- shorted together | | 4.5 | | mA |
| Output Impedance, OUT+ Pin | | | 50 | | kΩ |
| Output Capacitance OUT+ Pin | | | 5 | | pF |
| Allowable DC Load Resistance To VCC on OUT+ Pin | | 88 | | 112 | Ω |
| Allowable AC Load Impedance on OUT+ Pin | | 88 | | 112 | Ω |
| Power Supply Rejection Ratio (input referred) | ΔV(VDD) or ΔV(VCC) = 100 mVpp, 5 MHz, gain set at 16 V/V | 22 | | | dB |

**PULSE SLIMMER, EXTERNAL FILTER DRIVERS AND VARIABLE ATTENUATOR**

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Gain from OUT+ pin to (Flx+ - Flx-) | V (ATTEN) = VREF2_2 | | 9 | | V/V |
| Kmin, minimum attenuator gain | V(ATTEN) = VREF2_2 | | | 0.05 | |
| Kmax, maximum attenuator gain | V(ATTEN) = 0.0V | 0.81 | | | |
| Gain Factor G Tolerance | G(ideal) = 0.83, V(ATTEN) = VREF2_2 | -4 | | +4 | % |
| Ko Tolerance | Ko(ideal) = 0.84, V(ATTEN) = 0.0V | -4 | | +4 | % |
| Attenuator Gain K Ratio Linearity | 0.0 < V(ATTEN) < VREF2_2 end point method | -0.0 | | -4.5 | % |
| OUT+ to INREF pin resistance | | 5 | | 9 | kΩ |
| Output Voltage Ref VREF2_2 Pin | Iload = 0 to -1 mA | 1.95 | 2.28 | 2.45 | V |
| Output Voltage Resistance VREF2_2 Pin | Iload = -.7mA | | 4 | | Ω |
| Maximum Output Voltage Swing | Flx± | 1.25 | | | Vpp |

**ELECTRICAL CHARACTERISTICS** (continued)

**PULSE SLIMMER AND EXTERNAL FILTER DRIVERS**

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Input Resistance DLYIN Pin | | | 200 | | kΩ |
| Input Capacitance DLYIN Pin | | | 5 | | pF |
| Bandwidth referenced to 2.5 MHz | Transconductance I(FIx± /V(OUT+) | 40 | | | MHz |
| Allowable External DC Load Resistance | FIx± to VDD | 190 | | 210 | Ω |
| Power Supply Rejection Ratio (Input Referred) | ΔV (12) or ΔV (5) = 100 mVpp, 5 MHz delayline shorted | 45 | | | dB |
| Input Resistance ATTEN Pin | | | 200 | | kΩ |
| Input Bias Current ATTEN Pin | | | 8 | | μA |

**READ MODE DIGITIZING SECTION**

All of the measurements in the read mode digital section are made with the following conditions unless otherwise stated:

1. The circuit is in the read mode (R/$\overline{W}$ pin is high).
2. The summer input pins, (Fx+, Fx-) receive AC coupled 2.5 MHz, 0.83 Vpp sine wave input signal.
3. 100 Ω in series with 65 pF are tied between DIF+ and DIF-.
4. A 1.8 Vdc voltage is applied to the HYS pin.
5. OS is tied to the 5V supply with a 60 pF capacitor, Cos.
6. The $\overline{DOUT}$ pin is loaded with a 2.5 kΩ resistor to GND and a 5 pF capacitor to GND.
7. The $\overline{RD}$ pin is loaded with a 2.5 kΩ resistor to GND and a 5 pF capacitor to GND.

**SUMMER AND BUFFER**

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Allowable Input Signal Range | V(Fx+ - Fx-) | | | 1.25 | Vpp |
| Differential Input Resistance | V(Fx+ - Fx-) =100 mVpp DC | 10 | | 18 | kΩ |
| Differential Input Capacitance | V(Fx+ - Fx-) =100 mVpp @2.5 MHz | | 4.0 | | pF |
| Common Mode Input Impedance | On all Fx+ to Fx- Fx+/- tied together | 2.5 | | 4.5 | kΩ |
| Bandwidth referenced to 2.5 MHz | V(DIF±)/V(Fx±) | 35 | | | MHz |

**HYSTERESIS COMPARATOR CIRCUIT**

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| LEVEL Pin Output Voltage vs Fx+ - Fx- Input Voltage | 0.4 < V(Fx+ -Fx-) < 1.25 Vpp, 10 kΩ between LEVEL pin and GND | 1.8 | | 3.0 | V/Vpp |
| LEVEL Pin Output Impedance | I(LEVEL) = 0.5 mA | | 180 | | Ω |
| LEVEL Pin Maximum Output Current | V(Fx±) = 0.415V, ΔV(Level) ≤0.8 V | 3.0 | | | mA |
| Comparator and Summer Offset Voltage | HYS pin at GND, ≤1.5 kΩ across Fx+,Fx-. | | | 30 | mV |
| Input referred Hysteresis Voltage (at Fx+ - Fx- Pins) vs HYS Pin Voltage | 1 V < V(HYS) < 3 V | 0.16 | | 0.25 | V/V |
| Hysteresis threshold tolerance as a % of V(Fx+ - Fx-) peak | Set V(HYS) such that Hysteresis Threshold (Ideal) is 60% of V(Fx±), V(Fx±) = .415V (see Figures 2 & 3) | -15 | | +15 | % |
| HYS Pin Input Current | 1 V < V(HYS) < 3 V | 0.0 | | -20 | µA |

* In an open loop configuration where reference is V(AGC), tolerance can be slightly higher.

**DIFFERENTIATOR CIRCUIT**

| | | | | | |
|---|---|---|---|---|---|
| Voltage Gain from Fx+/- to DIF+/- | R(DIF+ to DIF-) = 2.0 kΩ | 2.0 | | 3.06 | V/V |
| DIF+ to DIF- Pin Current | Differentiator impedance must be set so as to not clip the signal for this current level | ±1.3 | | | mA |
| Comparator Offset Voltage | DIF+, DIF- AC coupled not directly measured | | | 10.0 | mV |
| COUT Pin Output Low Voltage | 0.0 ≤ Iol ≤ 0.5 mA | | VDD-3.0 | | V |
| COUT Pin Output Pulse Voltage Swing, V(high) - V(low) | 0.0 ≤ Ioh ≤ 0.5 mA | | +0.4 | | V |
| COUT Pin Output Pulse Width | 0.0 ≤ Ioh ≤ 0.5 mA | | 30 | | ns |
| Required DFF Set-up Time, Td1 in Fig. 6 | Minimum allowable time delay from V(Fx+,Fx-) exceeding hysteresis point to V(DIF+,DIF-) hitting peak value | 0 | | | ns |
| Propagation Delay, Td3 in Fig. 6 | | | | 110 | ns |
| Output Data Pulse Width at $\overline{RD}$ Pin, Td5 in Fig. 6 | Td5(ideal) = 900 x Cos @ V($\overline{RD}$) = 50% 30 ≤ Cos ≤ 200 pF | | | ±15 | % |

**ELECTRICAL CHARACTERISTICS** (continued)

**READ DIGITAL SECTION AS SYSTEM**

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Pulse Pairing<br>\|Td3 - Td4\| Fig. 6 | 0.83 Vpp into Fx+/- pins<br>at 2.5 MHz | | | 1.5 | ns |
| | 0.83 Vpp into Fx+/- pins<br>at 9.0 MHz | | | 1.0 | ns |

**SERVO BURST CAPTURE CIRCUIT**

All of the measurements are made with the following conditions unless otherwise stated:

1. The circuit is connected as in Figure 5.
2. A and B bursts are sampled onto $\overline{\text{BURSTA}}$ and $\overline{\text{BURSTB}}$ pins.

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Allowable VREF Voltage Range | | 3.9 | | 6.0 | V |
| BURSTA, BURSTB<br>Pin Output Voltage<br>vs (Fx+ - Fx-) Input Voltage | $AV=\frac{V(BURST)-VREF}{V(Fx+-Fx-)}=2.6V/Vpp$<br>$\overline{\text{LATCHA}}$ or $\overline{\text{LATCHB}}$ = Low | | | ±11 | % |
| BURSTA, BURSTB<br>Output Offset Voltage | V(BURST) - V(VREF),<br>$\overline{\text{LATCHA}}$, $\overline{\text{LATCHB}}$ Low,<br>V(Fx+) = V(Fx-), RCS =<br>38.3 kΩ, $\overline{\text{RST}}$ low | | | ±60 | mV |
| BURSTA - BURSTB<br>Output Offset<br>Voltage Match | V(BURSTA)-V(BURSTB),<br>$\overline{\text{LATCHA}}$, $\overline{\text{LATCHB}}$ Low,<br>V(Fx+) = V(Fx-) | | | ±15 | mV |
| PES Pin Output<br>Offset Voltage | V(PES) - V(VREF),<br>$\overline{\text{LATCHA}}$, $\overline{\text{LATCHB}}$ Low,<br>V(Fx+) = V(Fx-) | | | ±50 | mV |
| PES Pin Output Voltage<br>vs. Va(Fx)pp - Vb(Fx)pp | $AV=\frac{V(PES)-VREF}{Va(Fx)pp-Vb(Fx)pp}=2.6V/Vpp$ | | | ±15 | % |
| Output Resistance<br>BURSTA, BURSTB PES pins | | | | 20.0 | Ω |
| HOLDA/B Charge Current | | 25 | | | mA |
| HOLDA/B Discharge Current | $\overline{\text{RST}}$ = Low;<br>Idis = 2.6/(RCS + 750) | -15 | | +15 | % |
| | $\overline{\text{RST}}$ = High,<br>LATCH_A/B = High | | | ±0.5 | µA |
| Allowable Load Resistance;<br>BURSTA/B,PES pins | Resistor to VREF | 10.0 | | | kΩ |
| Allowable Load Capacitance;<br>BURSTA/B,PES pins | | | | 20.0 | pF |

**SERVO BURST CAPTURE CIRCUIT** (continued)

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $\overline{\text{LATCHA/B}}$ Pin Setup Time (Tds1 in Fig. 2) | | 150 | | | ns |
| $\overline{\text{LATCHA/B}}$ Pin Hold Time, (Tds2 in Fig. 2) | | 150 | | | ns |
| Channel A/B Discharge Current Turn On Time (Tds3 in Fig. 2) | | | | 150 | ns |
| Channel A/B Discharge Current Turn Off Time (Tds4 in Fig. 2) | | | | 150 | ns |

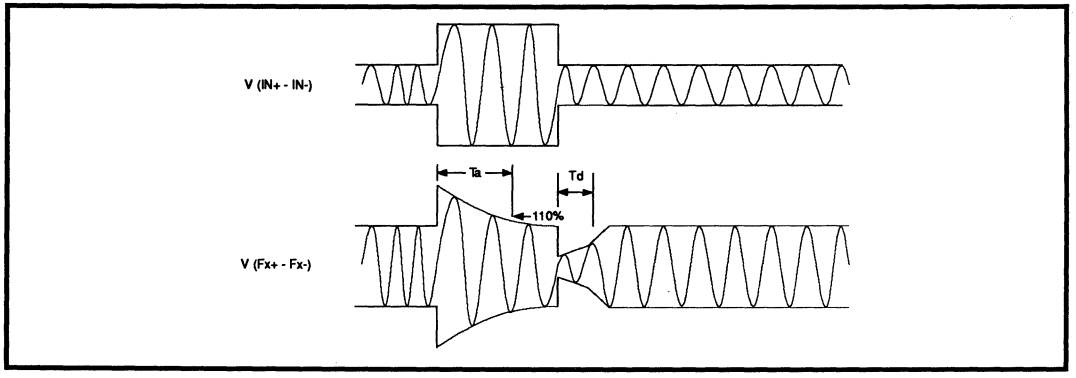



**FIGURE 1: AGC Timing Diagram**

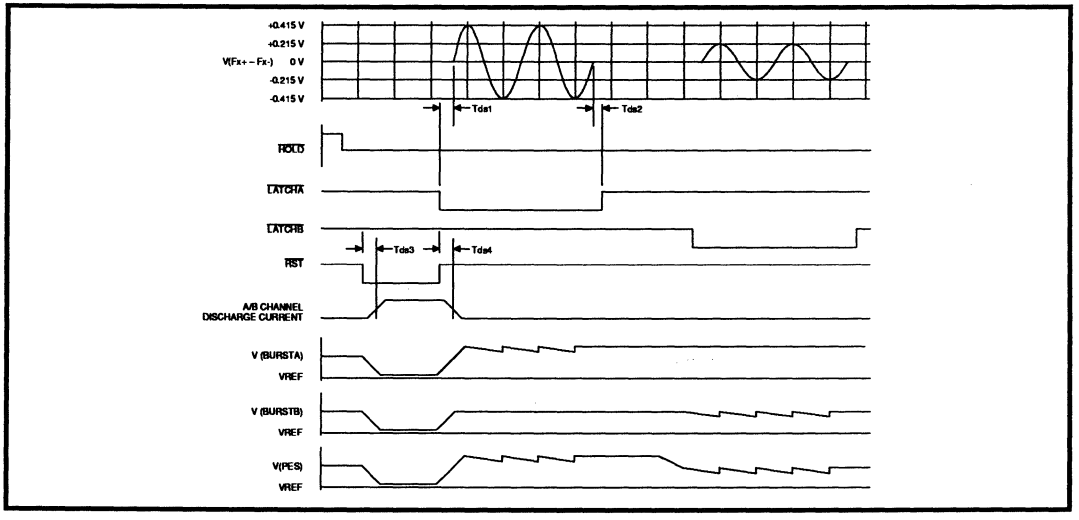



**FIGURE 2: Servo Timing Diagram**

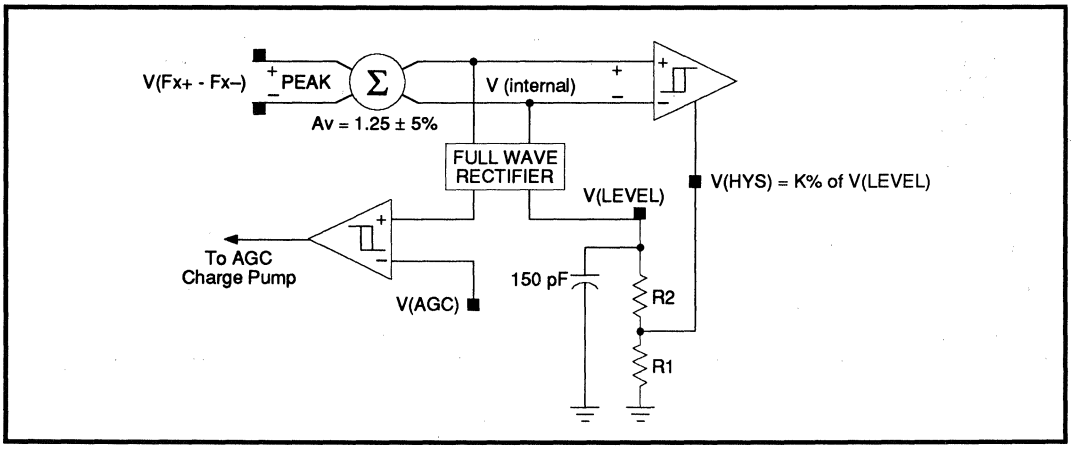



**FIGURE 3: Feed Forward Mode**

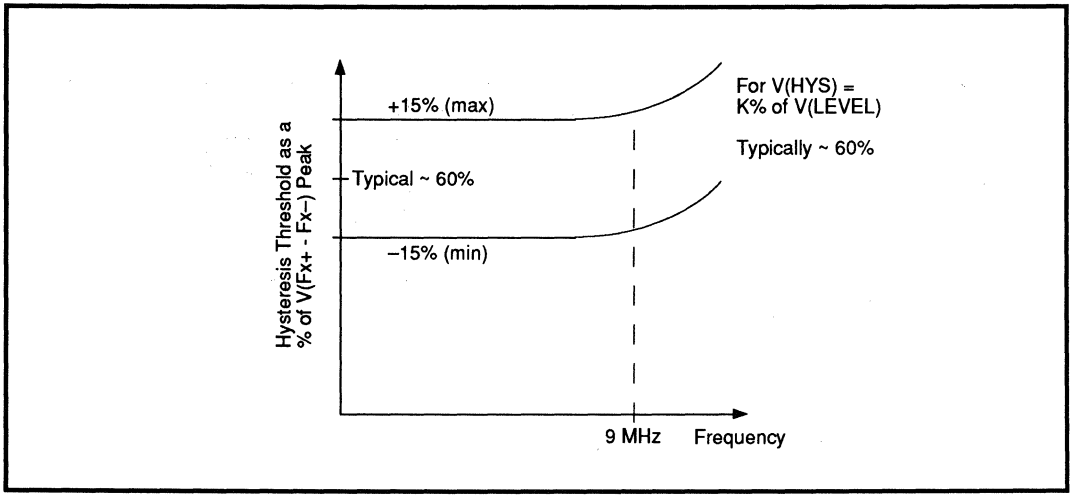



**FIGURE 4: Percentage Threshold vs. Frequency**

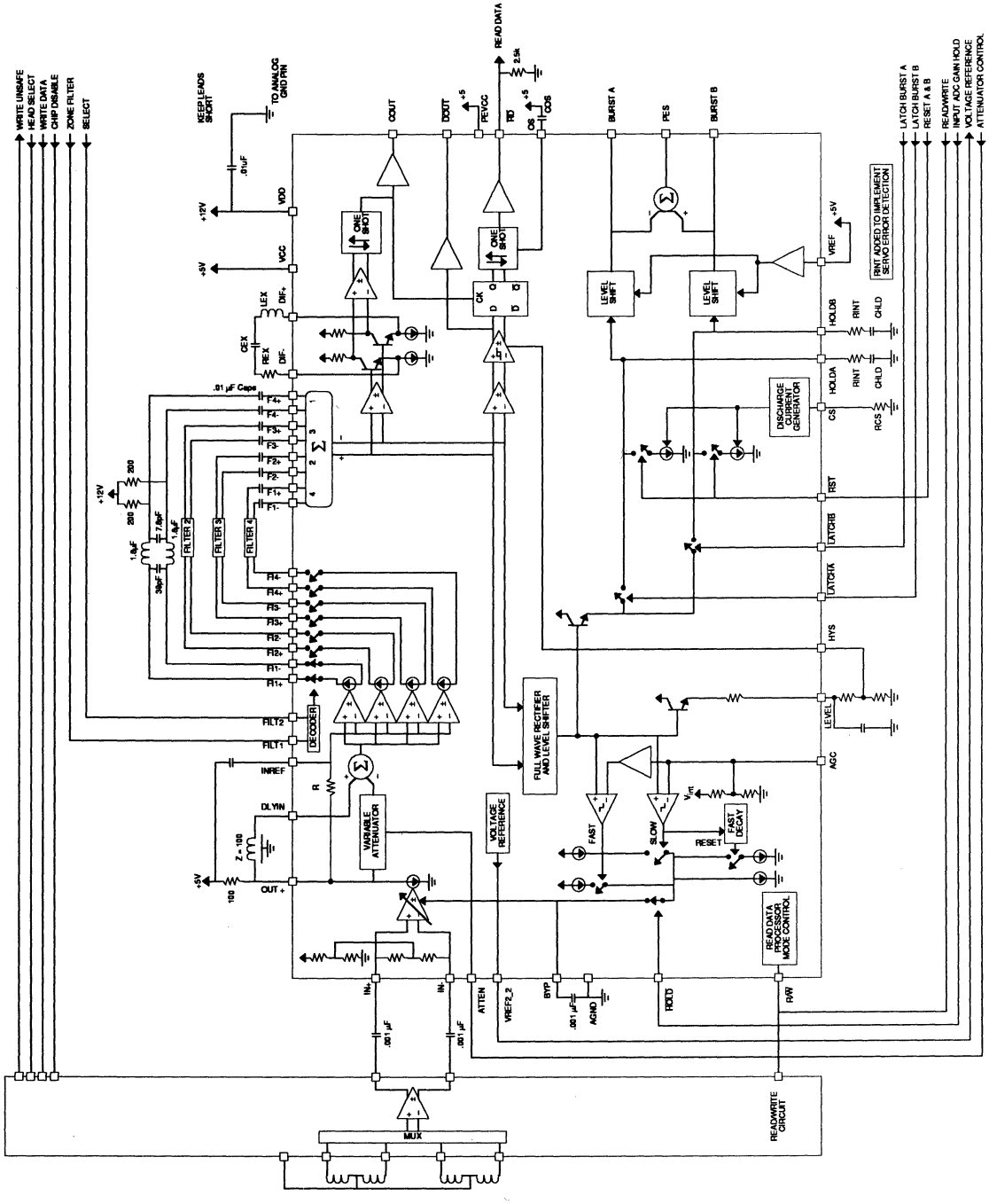



**FIGURE 5: Applications Circuit Diagram**

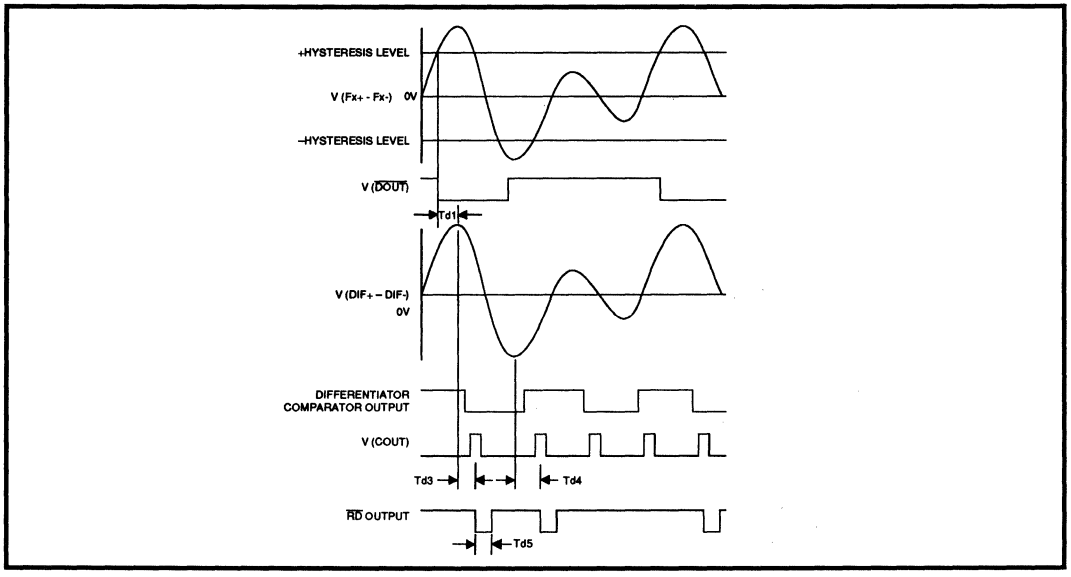



**FIGURE 6: Read Mode Digital Section Timing Diagram**

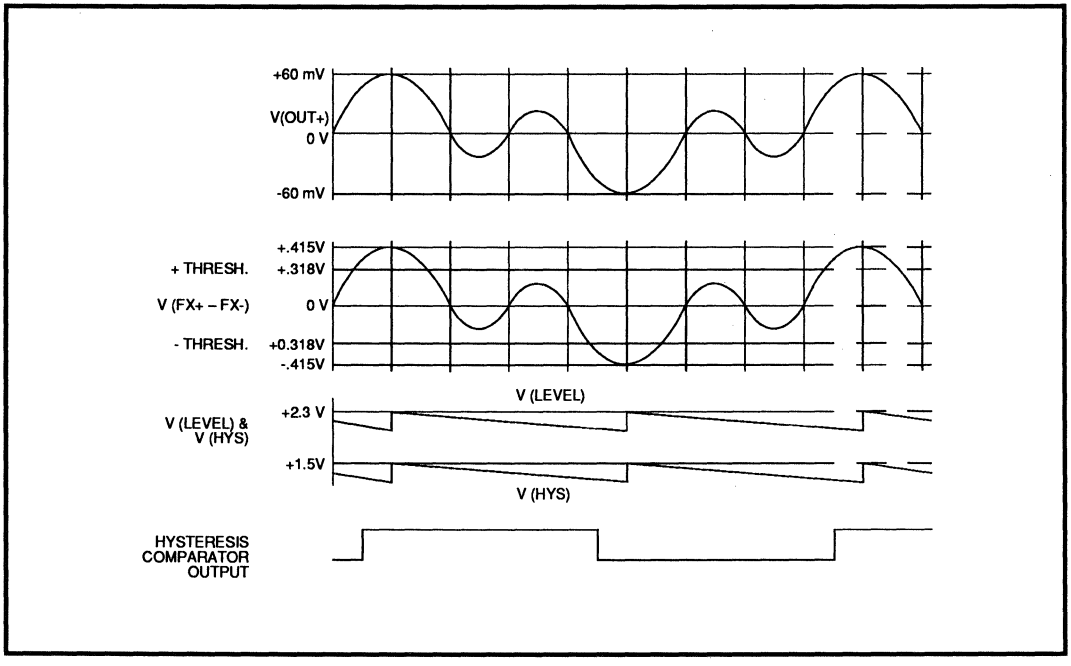


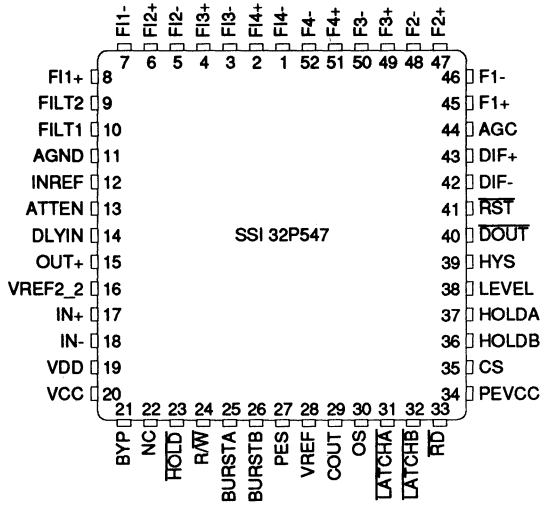

**FIGURE 7: Expected Nominal Voltage Levels**

## PACKAGE PIN DESIGNATIONS

(Top View)

**Thermal Characteristics: θjA**

| | |
|---|---|
| 52-lead PLCC | 55° C/W |




**52-Lead PLCC**

CAUTION: Use handling procedures necessary for a static sensitive component.

## ORDERING INFORMATION

| PART DESCRIPTION | ORDER NO. | PKG. MARK |
|---|---|---|
| SSI 32P547 52-Lead PLCC | 32P547-CH | 32P547-CH |



Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 573-6000, FAX (714) 573-6914

**Notes:**

# SSI 32P5491
## Pulse Detector

**Preliminary Data** 2

December 1992

## DESCRIPTION

The SSI 32P5491 is a bipolar integrated circuit that provides all data processing necessary for detection and qualification of MFM or RLL encoded read signals.

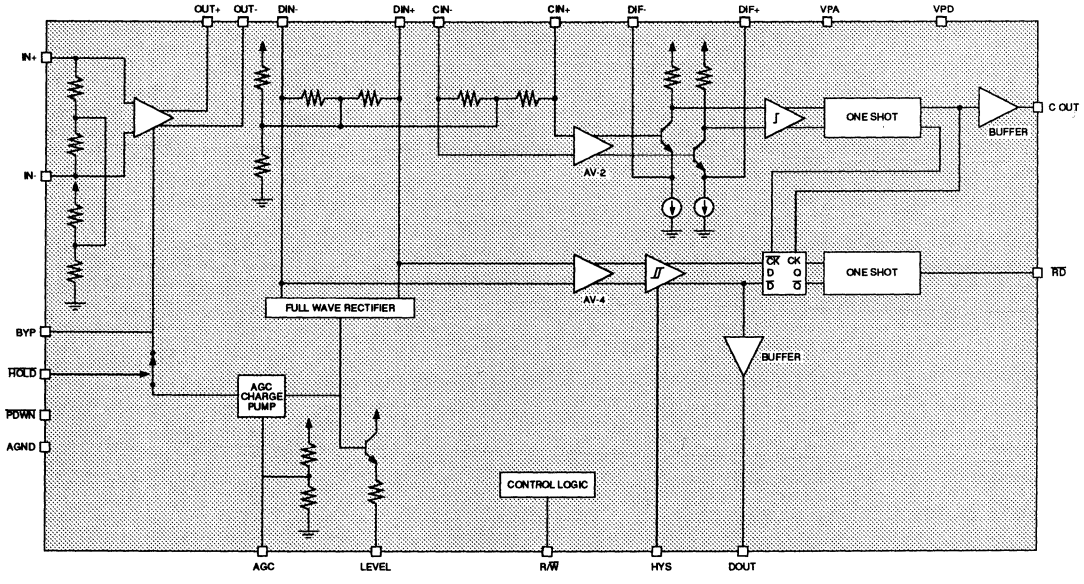
In read mode the SSI 32P5491 provides amplification and qualification of head preamplifier outputs. Pulse qualification is accomplished using level qualification of differentiated input zero crossings. An AGC amplifier is used to compensate for variations in head preamp output levels, presenting a constant input level to the pulse qualification circuitry. The AGC loop can be disabled so that a constant gain can be used for embedded servo decoding or other processing needs.

In write mode the circuitry is disabled and the AGC gain stage input impedance is switched to a lower level to allow fast settling of the input coupling capacitors during a write to read transition. The SSI 32P5491 requires a +5V power supply and is available in 28-pin PLCC and 24-pin SOL packages.

## FEATURES

- **Level qualification supports high resolution MFM and RLL encoded data retrieval**
- **Wide bandwidth AGC input amplifier**
- **Standard +5V ± 10% supplies**
- **Write to read transient suppression**
- **Fast and slow AGC attack regions for fast transient recovery**
- **≤ ±1.0 ns pulse pairing**
- **24 Mbit/s operation**
- **Power down mode (5 mW maximum)**
- **Low power**

## BLOCK DIAGRAM



## CIRCUIT OPERATION

### READ MODE

In read mode (R/$\overline{W}$ input high or open) the input signal is amplified and qualified using an AGC amplifier and pulse level qualification of the detected signal peaks.

An amplified head output signal is AC coupled to the IN+ and IN- pins of the AGC amplifier. Gain control is accomplished by full wave rectifying and amplifying the [(DIN+)-(DIN-)] voltage level and comparing it to a reference voltage level at the AGC pin.

The 32P5491 contains a dual rate attack charge pump. The value of the attack current is dependent on the instantaneous level at DIN±. For signal levels above 125% of the desired level a fast attack mode is invoked that supplies a 1.3 mA charge current to the network on the BYP pin. Between 125% and 100% of the desired level the circuit enters a slow attack mode and supplies 0.18 mA of charge current to the BYP pin.

Two decay modes are available and are automatically controlled within the device.

Upon a switch to write mode, the device will hold the gain at its previous value. When the device is then switched back to read mode the AGC holds the gain and stays in a low impedance state for 0.9 µs. It then switches into a fast/slow attack mode if the new gain required is less than the previously held gain or a fast decay mode if the gain required is more than its previous value. The fast decay current is 0.12 mA and stays on for 0.9 µs. After the 0.9 µs time period the device stays in a steady state slow attack, slow decay mode. The slow decay discharge current is 4.5 µA.

The AGC pin is internally biased so that the target differential voltage input at DIN± is 1.0 Vpp under nominal conditions. The voltage on this pin can be modified by tying a resistor between AGC and GND or VPA. A resistor to GND decreases the voltage level, while a resistor to VPA increases it. The resulting AGC voltage level is shown in Figure 1; where:

V = Voltage at AGC w/pin open (1V, nom)

Rint = AGC pin input impedance (4.0 kΩ, typ)

Rext = External resistor

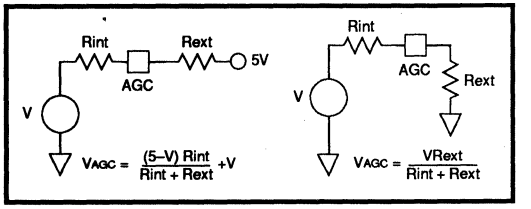



**FIGURE 1: AGC Voltage**

The new DIN ± input target level is nominally 1.0 Vpp/ VAGC.

The maximum AGC amplifier output swing is 3.0 Vpp at OUT±, which allows for up to 6dB loss in any external filter between OUT± and DIN±.

AGC gain is a linear function of the BYP-pin voltage (VBYP) as shown in Figure 2.

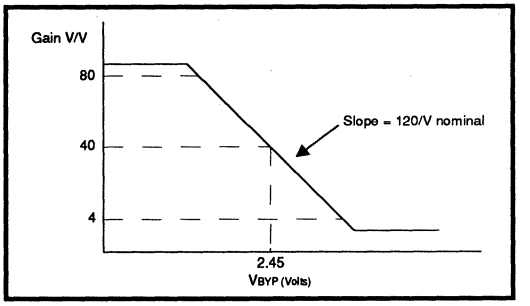



**FIGURE 2: AGC Gain**

In the amplitude channel the signal is sent to a hysteresis comparator. The hysteresis threshold level is set so that it will be tripped only by valid signal pulses and not by baseband noise. It can be a fixed level or a fraction of the DIN± voltage level.

The latter approach is accomplished by using an external filter/network between the LEVEL and HYS pins. This allows setting the AGC slow attack and decay times slow enough to minimize time channel distortion and setting a shorter time constant for the hysteresis level. The LEVEL pin output is a rectified and amplified version of DIN±, 1.0 Vpp at DIN± results in 1.0 VO-pk nominally, at the LEVEL pin. A voltage divider is used from LEVEL to ground to set the Hysteresis threshold at a percentage of the peak DIN± voltage. For example,

if DIN± is 1.0 Vpp, then using an equal valued resistor divider will result in 0.5 Vpk at the HYS pin. This will result in a nominal ±0.18V threshold or a 36% threshold of a ±0.500V DIN± input. The capacitor is chosen to set an appropriate time constant. This "feed forward" technique speeds up transient recovery by allowing qualification of the input pulses while the AGC is still settling. This helps in the two critical areas of write to read and head change recovery. Some care in the selection of the hysteresis level time constant must be exercised so as to not miss pattern (resolution) induced lower amplitude signals. The output of the hysteresis comparator is the "D" input of a D-type flip-flop. The DOUT pin is a comparator output signal for testing purposes only.

In the time channel the signal is differentiated to transform signal peaks to zero crossings which are detected and used to trigger a bi-directional one-shot. The one-shot output pulses are used as the clock input of the D flip-flop. The COUT pin provides the one-shot output for test purposes.

The differentiator function is accomplished by an external network between the DIF+ and DIF- pins. The transfer function from CIN± to the comparator input (not DIF±) is:

$$Av = \frac{-3536Cs}{LCs^2 + C(R+52)s + 1}$$

where: C, L, R are external passive components
$15\ pF < C < 125\ pF$
$s = j\omega = j2\pi f$

During normal operation, the time channel clocks the D flip-flop on every positive and negative peak of the CIN± input. The D input to the flip-flop only changes state when the DIN± input exceeds the hysteresis comparator threshold opposite in polarity to the previous threshold exceeding peak.

The time channel, then, determines signal peak timing and the amplitude channel determines validity by blocking signal peaks that do not exceed the hysteresis comparator threshold. The delays in each of these channels to the D flip-flop inputs are well matched.

### WRITE MODE

In Write Mode the SSI 32P5491 Pulse Detector section is disabled and preset for the following Read Mode. The digital circuitry is disabled, the input AGC amplifier gain is held at its previous value and the AGC amplifier input impedance is reduced.

Holding the AGC amplifier gain and reducing input impedance shortens system Write to Read recovery times.

The lowered input impedance improves settling time by reducing the time constant of the network between the SSI 32P5491 and a head preamplifier such as the SSI 32R2020R. Write to read timing is controlled to maintain the reduced impedance for 0.9 µs before the AGC circuitry is activated. Coupling capacitors should be chosen with as low a value as possible consistent with adequate bandwidth to allow more rapid settling.

### POWER DOWN MODE

A power down mode is provided to reduce power usage during the idle periods. Taking $\overline{PDWN}$ low causes the device to go into complete shutdown dissipating a maximum 5 mW of power. When $\overline{PDWN}$ returns high, the device executes the normal Write to Read recovery sequence.

### MODE CONTROL

The SSI 32P5491 circuit mode is controlled by the $\overline{PDWN}$, $\overline{HOLD}$, and R/$\overline{W}$ pins as shown in Table 1.

| R/$\overline{W}$ | $\overline{HOLD}$ | $\overline{PDWN}$ | |
|---|---|---|---|
| 1 | 1 | 1 | Read Mode, AGC Active |
| 1 | 0 | 1 | Read Mode AGC gain held constant* |
| 0 | X | 1 | Write Mode AGC gain held constant*<br>Input impedance reduced |
| X | X | 0 | Power Down - low current disabled mode |

* AGC gain will drift at a rate determined by BYP and Hold mode discharge current.

**TABLE 1: Mode Control**

## PIN DESCRIPTION

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| VPA | I | Analog (+5V) power supply for pulse detector |
| AGND | I | Analog ground pin for pulse detector block |
| VPD | I | Digital (+5V) power supply pin |
| DGND | I | Digital ground pin |
| IN+, IN– | I | Analog signal input pins |
| OUT+, OUT– | O | Read path AGC Amplifier output pins |
| DIN+, DIN– | I | Analog input to the hysteresis comparator |
| CIN+, CIN– | I | Analog input to the differentiator |
| DIF+, DIF– | I/O | Pins for external differentiating network |
| COUT | O | Test point for monitoring the flip-flop clock input |
| DOUT | O | Test point for monitoring the flip-flop D-input |
| $\overline{RD}$ | O | TTL compatible read output |
| BYP | I/O | An AGC timing capacitor or network is tied between this pin and AGND1 |
| AGC | I | Reference input voltage for the read data AGC loop |
| LEVEL | O | Output from fullwave rectifier that may be used for input to the hysteresis comparator |
| HYS | I | Hysteresis level setting input to the hysteresis comparator |
| $\overline{HOLD}$ | I | TTL compatible pin that holds the AGC gain when pulled low |
| $\overline{PDWN}$ | I | Low state on this pin puts the device in a low power "off" state |
| R/$\overline{W}$ | I | Selects Read or Write mode |

## ELECTRICAL SPECIFICATIONS

Recommended conditions apply unless otherwise specified.

### ABSOLUTE MAXIMUM RATINGS

Operation outside these rating limits may cause permanent damage to this device.

| PARAMETER | RATING |
|---|---|
| 5V Supply Voltage, VPA, VPD | 6.0V |
| Pin Voltage (Analog pins) | -0.3 to VPA, + 0.3V |
| Pin Voltage (All others) | -0.3 to VPD + 0.3V<br>or +12 mA |
| Storage Temperature | 65 to 150°C |
| Lead Temperature (Soldering 10 sec.) | 260°C |

### RECOMMENDED OPERATING CONDITIONS

Currents flowing into the chip are positive.

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Supply Voltage (VPA & VPD) | | 4.5 | 5.0 | 5.5 | V |
| Junction Temperature, Tj | | 25 | | 135 | °C |
| Ambient Temperature, Ta | | 0 | | 70 | °C |

### POWER SUPPLY

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| IVPA<br>IVPD | Supply Current | Outputs unloaded;<br>$\overline{PDWN}$ = high or open | | 34 | 42 | mA |
| Pd | Power dissipation | Ta = 25°C, outputs unloaded | | 170 | 230 | mW |
| | | $\overline{PDWN}$ = low,<br>Outputs unloaded | | 2 | 5 | mW |

### LOGIC SIGNALS

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| VIL | Input Low Voltage | | -0.3 | | 0.8 | V |
| VIH | Input High Voltage | | 2.0 | | VCC+0.3 | V |
| IIL | Input Low Current | VIL = 0.4V | 0.0 | | -0.4 | mA |
| IIH | Input High Current | VIH = 2.4V | | | 100 | µA |
| VOL | Output Low Voltage | IOL = 4.0 mA | | | 0.5 | V |
| VOH | Output High Voltage | IOH = -400 µA | 2.4 | | | V |

* Output load is a 4K resistor to 5V and a 10 pF capacitor to DGND.

**MODE CONTROL**

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Enable to/from $\overline{PDWN}$ Transition Time | Settling time of external capacitors not included, pin high to/from low | | 20 | | µs |
| Read to Write Transition Time | R/$\overline{W}$ pin high to low | | 0.2 | 1.0 | µs |
| Write to Read Transition Time | R/$\overline{W}$ pin low to high AGC settling not included | 0.5 | 0.9 | 1.3 | µs |
| $\overline{HOLD}$ On to/from $\overline{HOLD}$ Off Transition Time | $\overline{HOLD}$ pin high to/from low | | | 1.0 | µs |

**READ MODE** (R/$\overline{W}$ is high)

**AGC AMPLIFIER**

Unless otherwise specified, recommended operating conditions apply. Input signals are AC coupled to IN± and amplitude is between 25 mVpp & 250 mVpp differential. OUT± are loaded differentially with >600Ω, and each side is loaded with < 10 pF to AGND, and AC coupled to DIN±. A 2000 pF capacitor is connected between BYP and AGND. AGC pin is open.

| PARAMETER | CONDITION | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Gain Range | 1.0 Vpp ≤ (OUT+) - (OUT-) ≤ 3.0 Vpp | 4 | | 80 | V/V |
| Output Offset Voltage | Over entire gain range | -200 | 0 | +200 | mV |
| Maximum Output Voltage Swing | Set by BYP pin THD ≤ 5% | 3.0 | | | Vpp |
| Differential Input Resistance | (IN+) - (IN-) = 100 mVpp @ 2.5 MHz | | 5.0 | | kΩ |
| Differential Input Capacitance | (IN+) - (IN-) = 100 mVpp @ 2.5 MHz | | | 10 | pF |
| Common Mode Input | R/$\overline{W}$ = high | | 1.5 | | kΩ |
| Impedance | R/$\overline{W}$ = low | | 160 | | Ω |
| Input Noise Voltage | Gain set to maximum, RS = 0, BW = 15 MHz | | 6 | 15 | nV/$\sqrt{Hz}$ |
| Bandwidth | -3 dB bandwidth at maximum gain | 32 | | | MHz |
| OUT+ & OUT- Pin Current | No DC path to AGND | | 3 | | mA |
| CMRR (Input Referred) | (IN+) = (IN-) = 100 mVpp @ 2.5 MHz, gain set to max | 40 | | | dB |
| PSRR (Input Referred) | VPA1, 2 = 100 mVpp @ 2.5 MHz, gain set to max | 30 | | | dB |

**AGC AMPLIFIER** (Continued)

| PARAMETER | CONDITION | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| (DIN+) - (DIN-) Input Swing vs. AGC Input | 25 mVpp ≤ (IN+) - (IN-) ≤ 250 mVpp, $\overline{HOLD}$ = high, 0.5 Vpp ≤ (DIN+) - (DIN-) ≤ 1.5 Vpp | 0.9 | 1.0 | 1.1 | Vpp/V |
| (DIN+) - (DIN-) Input Voltage Swing Variation | 25 mVpp ≤ (IN+) - (IN-) ≤ 250 mVpp | | | 6.0 | % |
| AGC Voltage | AGC open | 0.8 | 1.0 | 1.2 | V |
| AGC Pin Input Impedance | | 3.5 | 4.0 | 5.5 | kΩ |
| Slow AGC Discharge Current | (DIN+) - (DIN-) = 0V | 4 | 4.5 | 6 | µA |
| Fast AGC Discharge Current | Starts at 0.9 µs after R/$\overline{W}$ goes high, stops at 1.8 µs after R/$\overline{W}$ goes high | 98 | 120 | 150 | µA |
| AGC Leakage Current | $\overline{HOLD}$ = low | -0.2 | 0 | +0.2 | µA |
| Slow AGC Charge Current | (DIN+) - (DIN-) = 0.8 VDC, vary AGC until slow charge begins | -0.12 | -0.18 | -0.24 | mA |
| Fast AGC Charge Current | (DIN+) - (DIN-) = 0.8 VDC, $V_{AGC}$ = 3.0V | -0.9 | -1.3 | -1.7 | mA |
| Fast to Slow Attack Switchover Point | $\frac{[(DIN+)-(DIN-)]}{[(DIN+)-(DIN-)]FINAL}$ | | 125 | | % |
| Gain Decay Time (Td) | (IN+) - (IN-) = 250 mVpp to 125 mVpp @ 2.5 MHz, (OUT+) - (OUT-) to 90% final value | | 20 | | µs |
| | (IN+) - (IN-) = 50 mVpp to 25 mVpp at 2.5 MHz (OUT+) - (OUT-) to 90% final value | | 70 | | µs |
| Gain Attack Time | R/$\overline{W}$ = low to high (IN+) - (IN-) = 250 mVpp @ 2.5 MHz, (OUT+) - (OUT-) to 110% final value | | 1.5 | | µs |

**WRITE MODE** (R/$\overline{W}$ is low)

| PARAMETER | CONDITION | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Common Mode Input Impedance | | | 160 | | Ω |

### HYSTERESIS COMPARATOR

Unless otherwise specified, recommended operating conditions apply. Input (DIN+) - (DIN-) is an AC coupled, 1.0 Vpp, 2.5 MHz sine wave. 0.5 VDC is applied to the HYS pin. R/$\overline{W}$ pin is high.

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Input Signal Range | | 0.6 | 1.0 | 1.5 | Vpp |
| Differential Input Resistance | (DIN+) - (DIN-) = 100 mVpp @ 2.5 MHz | 17.5 | 20 | 22.5 | kΩ |
| Differential Input Capacitance | (DIN+) - (DIN-) = 100 mVpp @ 2.5 MHz | | | 5.0 | pF |
| Common Mode Input Impedance (Both Sides) | | 3.5 | 4.5 | 5.5 | kΩ |
| Level Pin Output Voltage vs. (DIN+) - (DIN-) | 0.6 Vpp < (DIN+) - (DIN-) < 1.5 Vpp, 10K between LEVEL and AGND | | 1 | | V/Vpp |
| Level Pin Output Offset Voltage | 10 kΩ between level and AGND | | 170 | | mV |
| Level Pin Output Impedance | $I_{LEVEL}$ = 0.2 mA | | 330 | | Ω |
| Level pin Maximum Output Current | | 1.5 | | | mA |
| Hysteresis Voltage at DIN± vs. HYS Pin Voltage | 0.3 V < HYS < 1.0V | | 0.41 | | V/V |
| HYS Pin Input Current | 0.5 V < HYS < 1.5V | 0.0 | | -10 | µA |
| DOUT Pin Output Low Voltage | 5 kΩ from DOUT to GND | | VPA -2.8 | | V |
| DOUT Pin Output High Voltage | 5 kΩ from DOUT to GND | | VPA -2.4 | | V |

### ACTIVE DIFFERENTIATOR

Unless otherwise specified, recommended operating conditions apply. Input (CIN+) - (CIN-) is an AC-coupled, 1.0 Vpp, 2.5 MHz sine wave. 100Ω in series with 65 pF are tied from DIF+ to DIF-.

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Input Signal Range | | 0.6 | 1.0 | 1.5 | Vpp |
| Differential Input Resistance | (CIN+) - (CIN-) = 100 mVpp @ 2.5 MHz | 17.5 | 20 | 22.5 | kΩ |
| Differential Input Capacitance | (CIN+) - (CIN-) = 100 mVpp @ 2.5 MHz | | | 5.0 | pF |
| Common Mode Input Impedance | Both sides | 3.5 | 4.5 | 5.5 | kΩ |
| Voltage Gain From CIN± to DIF± | (DIF+ to DIF-) = 2 kΩ | | 1 | | V/V |
| DIF+ to DIF- PIn Current | Differentiator impedance must be set so as to not clip the signal for this current level | ±0.7 | | | mA |
| COUT Pin Output Low Voltage | 5 kΩ from COUT to GND | | VPA -2.8 | | V |
| COUT Pin Output High Voltage | 5 kΩ from COUT to GND | | VPA -2.4 | | V |
| COUT Pin Output Pulse Width | | | 47 | | ns |

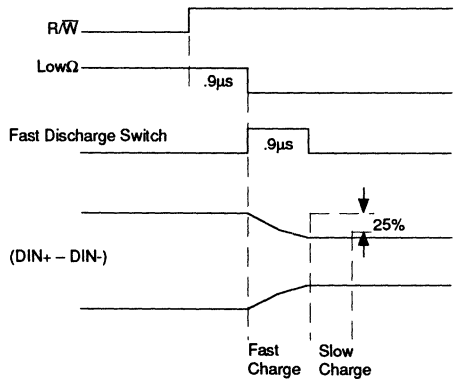



Figure A: AGC Attack Sequence

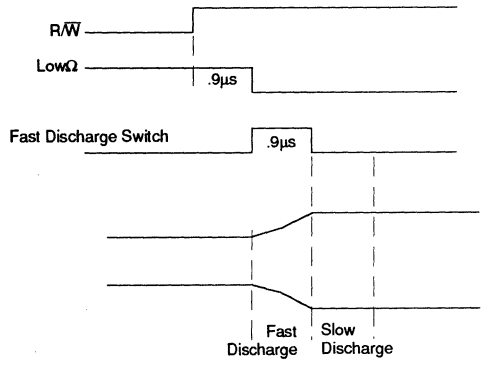



Figure B: AGC Decay Sequence

**FIGURE 7: AGC Timing Diagram**

### QUALIFIER TIMING

Unless otherwise specified, recommended operating conditions apply. Inputs (CIN+) - (CIN-) and (DIN+) - (DIN-) are in-place as a coupled, 1.0 Vpp, 2.5 MHz sine wave. 100Ω in series with 65 pF are tied from DIF+ to DIF-. 0.5V is applied to the HYS pin. COUT and DOUT each have a 5 kΩ pull-down resistor (for test purposes only.) R/$\overline{W}$ pin is high.

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| Td1 | D Flip-Flop Set Up Time | Minimum allowable time delay from (DIN+) - (DIN-) exceeding hysterisis point to (DIF+) - (DIF-) hitting a peak value. | 0 | 6.0 | | ns |
| Td3 | Propagation Delay | From positive peak to RD0* output pulse | | 30 | | ns |
| Td4 | Propagation Delay | From negative peak to RD0* output pulse | | 30 | | ns |
| Td3-Td4 | Pulse Pairing | | | 0.3 | 1.0 | ns |
| Td5 | $\overline{RD}$ Output Pulse Width | RDW pin open | 24 | 32 | 41 | ns |

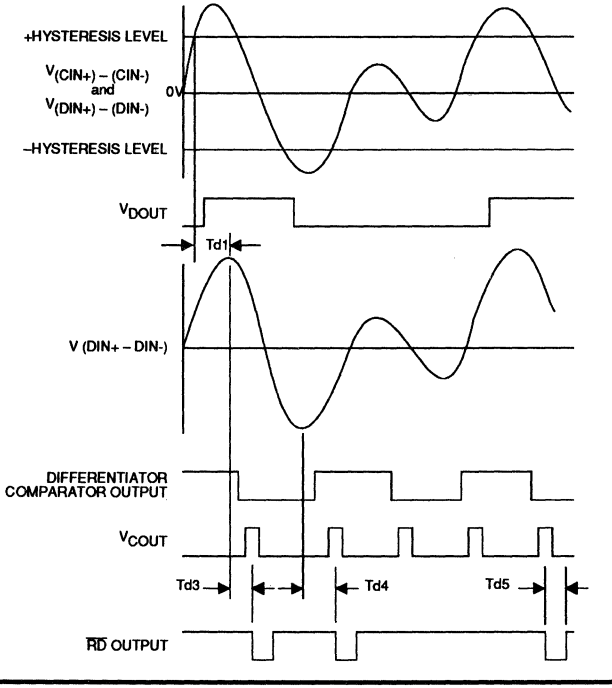
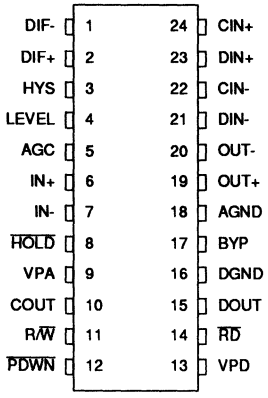



**FIGURE 8: Read Mode Digital Section Timing Diagram**

## PACKAGE PIN DESIGNATIONS

(Top View)

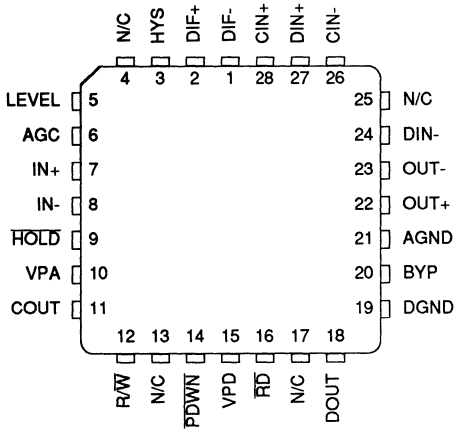



**24-Lead SOL**

CAUTION: Use handling procedures necessary for a static sensitive component.

**THERMAL CHARACTERISTICS: θja**

| | |
|---|---|
| 24-Lead SOL | 80°C/W |
| 28-Lead PLCC | 65°C/W |




**28-Pin PLCC**

## ORDERING INFORMATION

| PART DESCRIPTION | ORDER NO. | PKG. MARK |
|---|---|---|
| SSI 32P5491 Pulse Detector | | |
| 24-Lead SOL | 32P5491-CL | 32P5491-CL |
| 28-Pin PLCC | 32P5491-CH | 32P5491-CH |

**Preliminary Data:** Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.



Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680, (714) 573-6000, FAX: (714) 573-6914

**Notes:**

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# SSI 32P3000
## Pulse Detector with Programmable Filter

2

January 1993

## DESCRIPTION

The SSI 32P3000 is a bipolar integrated circuit that provides all the data processing for detection and qualification of encoded read signals from a head preamplifier. This device can handle a NRZ data rate of 64 Mbit/s.

The SSI 32P3000 includes an AGC amplifier with AGC charge pump, a programmable 7-pole Bessel low pass filter, and a pulse qualification circuit. The device features a complete differential circuit architecture in the signal path, for high immunity to noise and power supply ripples.

For fast write-to-read recovery, the SSI 32P3000 allows the user to control the low input state and AGC fast recovery mode independently. The AGC action can also be disabled for embedded servo decoding or other processing needs.

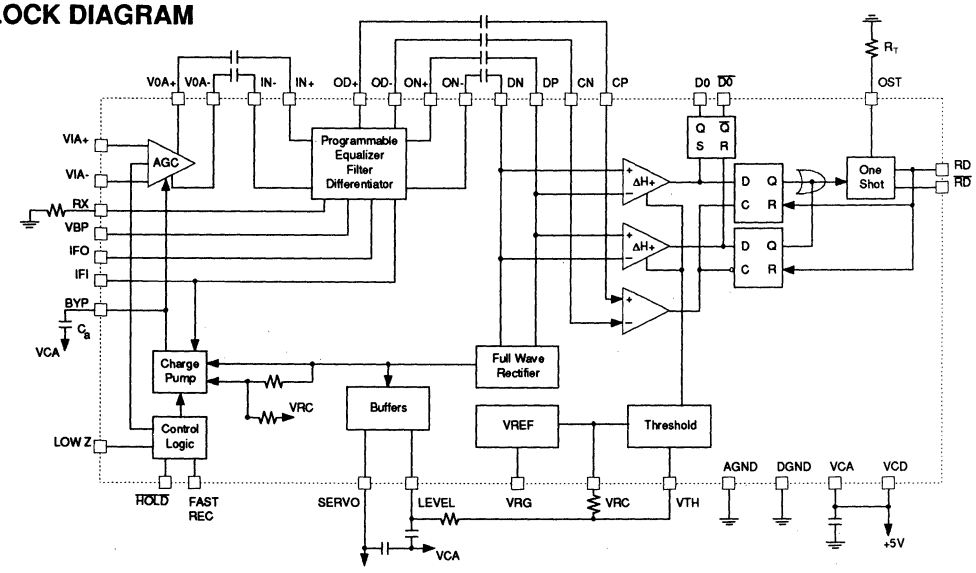
Ideal for constant density recording applications, the SSI 32P3000 low pass filter has a programmable 9 - 27 MHz bandwidth and 0 - 13 dB boost for pulse slimming. A time derivative of the read signal is also provided by the filter for time qualification in peak detection.

The SSI 32P3000 requires only a +5V power supply and is available in a 36-pin SOM package.

## FEATURES

- Compatible with 64 Mbit/s data rate operation
- Fast attack/decay modes for rapid AGC recovery
- Low Drift AGC hold, fast AGC recovery, and low AGC input impedance control signals
- Includes programmable pulse slimming equalization and programmable channel filter and differentiator with no external filter components
- ±0.5 ns filter group delay variation from 0.3 $fc$ to $fc$ = 27 MHz
- Independent positive and negative threshold qualification to suppress error propagation
- 0.5 ns max pulse pairing
- +5V only operation
- 36-pin SOM package

## BLOCK DIAGRAM



# SSI 32P3000
# Pulse Detector with Programmable Filter

## FUNCTIONAL DESCRIPTION

The SSI 32P3000 Pulse Detector is designed to support a 64 Mbit/s NRZ data rate. The signal processing circuits include a wide band variable gain amplifier, a dual-rate AGC charge pump, a programmable electronic filter, and a pulse qualifier.

### AGC Amplifier

The wide band AGC amplifier is to amplify the read signal from the read/write pre-amp to a signal level acceptable at the pulse qualifier. The AGC amplifier gain is an exponential function of the BYP voltage when referenced to VCA.

$$Av = Ao \exp[(\frac{V@BYP - Vr}{K})] \text{ (see note 1)}$$

### AGC Actions

The AGC loop is to maintain a constant DP/DN signal at the nominal level, ~1Vppd. The AGC actions are current charging and discharging the external BYP integrating capacitor. These AGC actions can be classified into the following categories:

#### Automatic

##### Slow Decay

When the DP/DN signal is below the nominal level, a slow decay current, Id, charges the BYP capacitor. The AGC amplifier gain is increased slowly. This slow decay current tracks with the bandwidth of the filter. Id = 0.008 x IFI. At T = 27°C, the maximum Id is 4.5 µA when the filter cutoff frequency is 27 MHz.

##### Slow Attack

When the DP/DN signal exceeds the nominal level but is below 125% of the nominal level, a slow attack current, Ich, discharges the BYP capacitor. The AGC amplifier gain is decreased. The slow attack current is 30 times that of the slow decay current. Thus, for a given BYP capacitor, the slow attack response time is quicker than the slow decay response.

Note 1: In a closed AGC loop, the sensitivity of Ao, Vr and K to typical process variations is irrelevant. The typical values of Ao, Vr and K are provided for references only, and not tested in production. Ao = 11, Vr = 3.6 and K = 0.22

##### Fast Attack

When the DP/DN signal exceeds 125% of the nominal level, the device enters a fast attack mode. A fast attack current, Ichf, discharges the BYP capacitor. The AGC amplifier gain is quickly lowered. The fast attack current is seven times that of the slow attack current.

#### User Control

##### FAST REC

When FAST REC = 1, the SSI 32P3000 enters the fast recovery mode. Independent of the DP/DN signal level, a fast recovery current, Idf, charges the BYP capacitor. This fast recovery current magnitude is 20 times that of the slow decay current. The AGC amplifier gain is quickly raised. Meanwhile, all the above automatic AGC actions remain active.

##### $\overline{\text{HOLD}}$

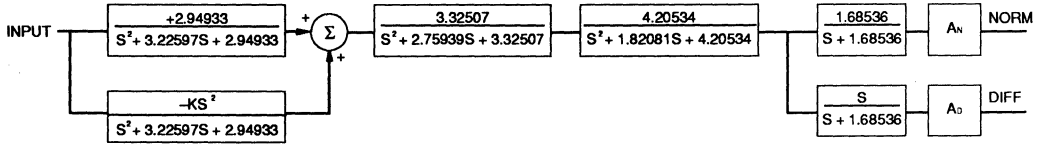
When HOLD = 0, all the automatic AGC actions and the fast recovery action are suspended. The BYP capacitor voltage remains constant, except for leakage effects.

### Programmable Filter

The SSI 32P3000 includes a programmable low pass filter following the AGC amplifier for (1) 2X voltage gain from filter input to filter outputs, (2) noise limiting, (3) pulse slimming, and (4) provision of a time differentiated signal. The low pass filter is of a 7-pole 2-zero Bessel type. The filter's un-boosted -3 dB bandwidth, defined as the cutoff frequency, is programmable from 9 - 27 MHz; the high frequency equalization is programmable from 0 - 13 dB at the cutoff frequency.

The filter input is ac-coupled from the AGC amplifier output. The filter's normal low pass output is ac-coupled to the data channel of the pulse qualifier. The differentiated low pass output is ac-coupled to the time channel of the pulse qualifier.

The normalized 7-pole 2-zero Bessel filter transfer function is given as:




The cutoff frequency, $fc$, is programmable with 3 pins: RX, IFO and IFI. At the RX pin, an external resistor to ground establishes a reference current, IFO = 0.75 / Rx, at T = 27°C. IFI should be made proportional to IFO for $fc$ temperature stability. The cutoff frequency is related to the RX resistor, IFO and IFI currents at the following:

$$fc(\text{MHz}) = 27 \cdot \frac{\text{IFI}}{\text{IFO}} \cdot \frac{1.25}{\text{RX}(k\Omega)}$$

For a fixed cutoff frequency setting, IFO and IFI can be tied together. The cutoff frequency equation then reduces to:

$$fc(\text{MHz}) = 27 \cdot \frac{1.25}{\text{RX}(k\Omega)}$$

For programmable cutoff frequency, an external current DAC can be used. IFO should be the reference current into the DAC. The DAC output current drives IFI, which is then proportional to IFO. The DACF in the SSI 32D4661 Time Base Generator is designed to control $fc$ of the Silicon Systems programmable filters. When the DACF, which has a 4X current gain from its reference to fullscale output, is used, 5 kΩ RX is used. The $fc$ is then given by:

$$fc(\text{MHz}) = 27 \cdot \frac{\text{F\_Code}}{127}$$

where F_Code is a decimal code equivalent to the 7-bit input into the DACF.

The high frequency equalization is programmable with two pins: VRG and VBP. The VRG is a bandgap reference voltage, 2.3 V typically. The voltage at the VBP pin determines the amount of high frequency boost at the cutoff frequency. The boost function is as the following:

$$\text{Boost(dB)} = 20\log_{10}\left[\text{Kb} \cdot \frac{\text{VBP}}{\text{VRG}}) + 1\right],$$

$$\text{Kb} = 3.041 + 0.0276 \cdot fci$$

Where $fci$ is the ideal cutoff frequency in MHz

For a fixed boost setting, a resistor divider between VRG and ground can be used with the divided voltage at the VBP pin. For programmable equalization, an external voltage DAC can be used. VRG should be the reference voltage to the DAC. The DAC output voltage is then proportional to VRG. The DACS in the SSI 32D4661 is designed to control the magnitude equalization of Silicon Systems' programmable filters. When DACS is used, the boost relation then reduces to:

$$\text{Boost(dB)} = 20\log_{10}\left[\left(\frac{\text{Kb} \cdot \text{S\_Code}}{127}\right) + 1\right]$$

### Pulse Qualification

The SSI 32P3000 validates each DP/DN peak by combination of level qualification and time qualification. In level qualification, a dual-comparator threshold detection eliminates errors due to low level additive noise. In time qualification, the filter's differentiated output is used to locate signal peaks.

### Level Qualification

The dual-comparator architecture allows independent detection for positive and negative peaks. One comparator detects a positive peak by comparing the data signal with a positive threshold. The other comparator detects a negative peak by comparing the data signal with a negative threshold. Each comparator has a small hysteresis, 20% of the set threshold, to avoid false triggering by noise around the set threshold.

The SSI 32P3000 allows two ways of setting the thresholds: fixed threshold or DP/DN tracking threshold. Fixed threshold can be simply set by a DC voltage at the VTH pin, such as from a resistor divider from VCA to VRC (see note 2). The threshold at each comparator can be computed as: Hysteresis Gain • (VTH - VRC). The thresholds at the two comparators are of the same

Note 2: VCA is the +5V supply. VRC is the bandgap voltage referenced from VCA, i.e., VRC = VCA - VRG.

magnitude, but of opposite polarity. For high performance system application, however, fixed threshold is not recommended.

DP/DN tracking threshold has the advantages of shorter write-to-read recovery time and lower probability of error with input amplitude drop out. The threshold is designed as a percentage of the DP/DN peak voltage. This technique can be implemented by feeding the LEVEL output, through a resistor divider network, to the VTH pin. The LEVEL output, amplified peak capture of DP/DN signal, can be computed as: Level Gain • DP/DN ppd + VRC. With the resistor divider, a fraction of the LEVEL output is presented at the VTH pin. The threshold, as a function of DP/DN, can be summarized as Level Gain • Resistor Dividing Ratio • Hysteresis Gain • DP/DN ppd. For a typical case of 1 Vppd DIN signal, assume equal value resistors in the divider network, the threshold is 0.75 • 0.5 • 0.455 • 1.0 = 0.17 V. This represents 34% threshold on a 1 Vppd signal. While both the Level Gain and Hysteresis Gain bear a moderate tolerance due to typical process variation, they inversely track each other to yield a much tighter threshold accuracy in a closed loop.

While the external resistor divider ratio determines the qualification setting, the total resistance and the peak capture capacitor should be optimized for the system data rate. The RC time constant must be small enough to allow good response to changing DP/DN peak, but large enough to provide a constant threshold after a long duration of input absence.

The Pulse Qualifier output is the pseudo-ECL differential output, RD and $\overline{RD}$. Corresponding to each validated peak of the DP/DN signal, a one-shot pulse occurs at the RD/$\overline{RD}$ output. The pulse width of the one-shot pulse is determined by an external resistor from the OST pin to ground.

$$\text{Pulse Width (sec)} = 0.157 \cdot (R_{OST} - 196) \cdot (22\ \text{pF} + C_S)$$

$$R_{OST} = 2\ \text{kW to}\ 8\ \text{kW}, C_S = \text{stray capacitance}$$

DO and $\overline{DO}$ form the differential output as test points to examine the output of the two comparators. Each is an open-emitter output requiring an 5 kΩ external resistor pull-down to ground.

## PIN DESCRIPTION

### INPUT PINS

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| VIA+, VIA- | I | AGC Amplifier input pins. |
| IN+, IN- | I | Equalizer/filter input pins. |
| DP, DN | I | Data inputs to data comparators and fullwave rectifier. |
| CP, CN | I | Differentiated data inputs to the clock comparator. |
| VTH | I | Threshold level setting input for the data comparators. |
| FAST REC | I | TTL compatible input when high puts the charge pump in the fast decay mode. |
| LOW Z | I | TTL compatible input when high reduces the AGC amplifier input resistance. |
| $\overline{HOLD}$ | I | TTL compatible input when low disables the AGC action by turning off the charge pump. |

## PIN DESCRIPTION (continued)

### OUTPUT PINS

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| VOA+, VOA- | O | AGC amplifier output pins. |
| ON+, ON- | O | Equalizer/filter normal output pins. |
| OD+, OD- | O | Equalizer/filter differentiated output pins. |
| DO+, DO- | O | ECL compatible data comparator latch output pins. |
| RD+, RD- | O | ECL compatible read data output pins. |
| LEVEL | O | Open NPN emitter output that provides a fullwave rectified signal for the VTH input. The signal is referenced to VRC. |
| SERVO | O | Open NPN emitter output that provides a fullwave rectified servo signal. The signal is referenced to VRC. |
| **ANALOG PINS** | | |
| OST | - | Pin for $R_T$ network to set RD output pulse width. An internal 22 pF capacitor has been included. |
| VRC | - | Reference voltage pin for SERVO and LEVEL. VRC is referenced to VCA. |
| VRG | - | Reference voltage pin for the programmable filter. VRG is referenced to ground. |
| VBP | - | The equalizer high frequency boost is set by an external voltage applied to this pin. VBP must be proportional to VRG. Programmable boost is implemented by using a DAC that uses VRG as its reference. A fixed amount of boost can be set by an external resistor divide network connected from VBP to VRG and GND. |
| RX | - | Pin to set filter reference current. External resistor Rx from this pin to ground sets the filter reference current IFO. |
| IFO | - | Reference current output pin. The reference current is normally supplied as the reference current to a current DAC which generates the programmable input current for the IFI pin. |
| IFI | - | Programmable filter input current pin. The filter cutoff frequency is proportional to the current into this pin. The current must be proportional to the reference current out of IFO. A fixed filter cutoff frequency is generated by connecting IFO to IFI and selecting Rx to set the desired frequency. |
| AGC | - | Optional reference voltage input for the AGC. The reference voltage is normally set by an internal resistor divider for VCC to VRC. (Not available in 36 pin SO package). |
| BYP | - | The AGC integrating capacitor $C_A$ is connected between BYP and VCA. |
| VCA, VCD | - | Analog and Digital +5V. |
| AGND1, DGND | - | Analog and Digital grounds. |

## ELECTRICAL SPECIFICATIONS

Unless otherwise specified, 4.5V < VCC < 5.5V, 0°C < Ta < 70°C

**ABSOLUTE MAXIMUM RATINGS** (Operation above maximum ratings may damage the device.)

| PARAMETER | VALUE |
|---|---|
| Storage Temperature | -65 to +150°C |
| Junction Operating Temperature,Tj | +130°C |
| Supply Voltage, VCA, VCD | -0.3 to 7V |
| Voltage Applied to Inputs | -0.7 to VCA, VCD + 0.7V |

**RECOMMENDED OPERATING CONDITIONS**

| PARAMETER | | RATING | UNIT |
|---|---|---|---|
| Supply Voltage | VCA = VCD = VCC | 4.5 < VCC < 5.5 | V |
| Ambient Temperature, Ta | | 0<Ta<70 | °C |

**POWER SUPPLY**

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| ISS | Supply Current | | | 82 | 105 | mA |
| PD | Power Dissipation | | | 410 | 580 | mW |

**LOGIC SIGNALS**

| | | | | | | |
|---|---|---|---|---|---|---|
| VIL | TTL Input Low Voltage | | -0.3 | | 0.8 | V |
| VIH | TTL Input High Voltage | | 2.0 | | VCC +0.3 | V |
| IIL | TTL Input Low Current | VIL = 0.4V | -0.4 | | | mA |
| IIH | TTL Input High Current | VIH = 2.7V | | | 0.1 | mA |
| VOHE | EECL Output High Voltage | | VCC -1.02 | VCC - 0.77 | VCC - 0.4 | V |
| VES | ECL Differential Output Swing \|VRD - $\overline{VRD}$\| | | 0.3 | 0.41 | 0.6 | V |
| TRF | ECL Output Rise and Fall Time | CL ≤ 10 pF | | | 3.5 | ns |
| TCS | Control Input Switching Times | | | | 0.1 | µs |

**AGC AMPLIFIER**

The input signals are AC coupled to VIA+ and VIA-. VOA+ and VOA- are AC coupled to IN+ and IN-. ON+ and ON- are AC coupled to DP and DN. Ca 1000 pF. Fin = 4 MHz. Unless otherwise specified, the output is measured differentially at VOA+ and VOA-.

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| VIR | Input Range | Filter boost at Fc = 0 dB | 24 | | 240 | mVppd |
| | | Filter boost at Fc = 11 dB | 20 | | 100 | mVppd |
| VD | DP-DN voltage | VIA± = 0.1 Vppd | 0.85 | | 1.05 | Vppd |
| VDV | DP-DN Voltage Variation | 24 mV < VIA± < 240 mV | | | 8.0 | % |
| AV | Gain Range | | 1.9 | | 22 | V/V |
| AVPV | Gain Sensitivity | | | 38 | | dB/V |
| DR | VOA± Dynamic Range | THD = 1% max | 0.75 | | | Vpp |
| RINDA | Differential Input Impedance | LOW Z = low | 3.7 | 5.8 | 7.4 | kΩ |
| RINSA | Single Ended Input Impedance | LOW Z = low | | 2.8 | | kΩ |
| | | LOW Z = high | | 100 | 150 | Ω |
| VOS | Output Offset Voltage Variation | from min gain to max gain | -200 | | +200 | mV |
| VIN | Input Referred Noise Voltage | gain = max, Rs = 0Ω filter not connected to VOA+, VOA-, BW = 15 MHz | | | 20 | $nV/\sqrt{Hz}$ |
| BW | Bandwidth | No AGC action | 55 | | | MHz |
| CMRR | Common Mode Rejection Ratio | gain = max, Vin = 0VDC + 100 mVpp @ 5 MHz | 40 | 65 | | dB |
| PSRR | Power Supply Rejection Ratio | gain = max, 100 mVpp on VCA, VCD @ 5 MHz | 45 | 67 | | dB |
| GDT | Gain Decay Time | VIA± = 240 mV to 120 mV VOA± <0.9 Final Value IFI = 600 µA | | 33 | | µs |
| GAT | Gain Attack Time | VIA± = 120 mV to 240 mV VOA± <1.1 Final Value IFI = 600 µA | | 1.2 | | µs |

## ELECTRICAL SPECIFICATIONS (continued)

Unless otherwise specified, 4.5<VCC<5.5, 0°C<Ta<70°C

### AGC CONTROL

The input signals are AC coupled to DP and DN. Ca = 1000 pF, LEVEL load = 50 µA, SERVO load = 100 µA, 110 µA < IFI < 600 µA.

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| VDI | DP-DN Signal Input Range | | | | 1.4 | Vpp |
| ID | Discharge Current, Id | FAST REC = low<br>DP - DN = 0 | | 0.008 x IFI | | mA |
| IDF | Fast Discharge Current, Idf | FAST REC = high | | 20 x Id | | mA |
| ICH | Charge Pump Attack Current, Ich | DP - DN = 0.55V | | 30 x Id | | mA |
| ICHF | Charge Pump Fast Attack Current, Ichf | DP-DN = 0.675V | | 7 x Ich | | mA |
| IK | BYP Pin Leakage Current | $\overline{HOLD}$ = low, VBYP = Vcc - 1.5V | -0.1 | | 0.1 | µA |
| VRG | Reference Voltage | I source = 0 to 1 mA | 2.2 | | 2.45 | V |
| VRC | Reference Voltage | | | VCC-VRG | | V |
| IVRC | VRC Output Drive | ΔVRC < 20 mV | -0.75 | | 0.75 | mA |

**EQUALIZER/FILTER** The input signals are AC coupled to IN+ and IN-.

| | | | | | | |
|---|---|---|---|---|---|---|
| FC | Filter Cutoff Frequency | RX = 5kΩ<br>$fc$ = 27 x IFI/(4 x IFO ) MHz<br>4 ≥ IFI/IFO ≥ 4/3 | 9 | | 27 | MHz |
| IFO | IFO Reference Current Range | IFO = 0.75/RX; Tj = 27°C<br>5kΩ > RX > 1.25 kΩ | 0.15 | | 0.6 | mA |
| IFI | IFI Program Current Range | Tj = 27°C, 27 MHz > $fc$ > 9 MHz | 0.2 | | 0.6 | mA |
| FCA | FCA Filter FC Accuracy | $fc$ nominal = 27 MHz | -13 | | 13 | % |
| RX | RX Range | | 1.25 | | 5 | kΩ |
| AO | Normal Low Pass Gain<br>AO = (ON ±) / (IN±) | Fin = 0.67$fc$ | 1.4 | | 2.2 | V/V |
| AD | Differentiated Low Pass Gain<br>AD = (OD ±) / (IN±) | Fin = 0.67$fc$ | 0.8AO | | 1.2AO | V/V |
| FBA | Frequency Boost | VRG/VBP = VRG | -1.5 | | +1.5 | dB |
| | Accuracy | VBP/VRG = 0.5 | -1.0 | | +1.0 | dB |
| TGD1 | Group Delay Variation | $fc$ = 27 MHz, VBP = 0 to VRG<br>$fc$ > Fin > 0.3$fc$ | -0.5 | | +0.5 | ns |

**EQUALIZER/FILTER** (continued)

The input signals are AC coupled to IN+ and IN-.

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| TGD2 | | *fc* = 9 to 27 MHz, VBP = 0 to VRG<br>*fc* > Fin > 0.3 *fc* | -2.5 | | +2.5 | % |
| VOSVF | Output Offset Voltage Variation | 200 µA < IFI < 600 µA | -200 | | 200 | mV |
| DRF | Filter Output Dynamic Range | THD = 1.5% max<br>Fin = 0.67 *fc* | 1.2 | | | Vpp |
| RINF | Filter Input Resistance | | 3.0 | | | kΩ |
| CINF | Filter Input Capacitance | | | | 7 | pF |
| ROF | Filter Output Resistance | IO+ = 1 mA | | | 60 | Ω |
| IOF | Filter Output Current | | -1.0 | | 1.0 | mA |
| VNN | Eout Output Noise Voltage; ON+, ON- | BW = 100 MHz, RS = 50Ω<br>VBP = 0, *fc* = 27 MHz | | 2.7 | 3.5 | mVRms |
| | | BW = 100 MHz, RS = 50Ω<br>VBP = VRG, *fc* = 27 MHz | | 5.7 | 8.0 | mVRms |
| VND | Eout Output Noise Voltage; OD+, OD- | BW = 100 MHz, RS = 50Ω<br>VBP = 0, *fc* = 27 MHz | | 5.7 | 7.5 | mVRms |
| | | BW = 100 MHz, RS = 50Ω<br>VBP = VRG, *fc* = 27 MHz | | 13.0 | 21.0 | mVRms |

**DATA COMPARATOR**

The input signals are AC coupled to DP and DN, I (LEVEL) = 50 µA, I (SERVO) = 100 µA, 0.01 µF caps tied from LEVEL and SERVO to VCA.

| | | | | | | |
|---|---|---|---|---|---|---|
| VID | DP-DN Signal Range | | | | 1.5 | Vpp |
| RIND | Differential Input Resistance | | 8 | | 14 | kΩ |
| CIND | Differential Input Capacitance | | | | 5 | pF |
| VOSD | Comparator Offset Voltage (Note 1) | | | | 4 | mV |
| LG | Level (Servo) Output Gain | DP-DN = 0.25 to 0.5 VDC | 0.712 | | 0.788 | V/V |
| LBW | Level (Servo) Output Bandwidth | ±1 dB referenced to 1 MHz | 20 | | | MHz |
| VLOS | Level Offset Voltage | Output-VRC, IL = 50 µA | -30 | | +30 | mV |
| VSOS | Servo Offset Voltage | Output - VRC, IL = 100 µA | -30 | | +30 | mV |
| GHYS | Threshold Voltage Gain | 0.3 < VTH-VRC < 0.9<br>0 | 0.42 | 0.455 | 0.49 | V/V |
| VSH | Threshold Voltage Hysteresis | | | 0.20 x GHYS x (VTH - VRC) | | V/V |

Note 1: Not directly measurable

**DATA COMPARATOR** (continued)

The input signals are AC coupled to DP and DN.

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| VHM | Minimum Threshold Voltage | VTH-VRC ≤ 0.11V | | 0.05 | | V |
| TPDD | Propagation Delay | From DP/DN to DO, $\overline{DO}$ | | 5 | | ns |
| IVTH | Input Bias Current | | | | 2 | µA |

**CLOCKING SECTION**

The input signals are AC coupled to CP and CN.

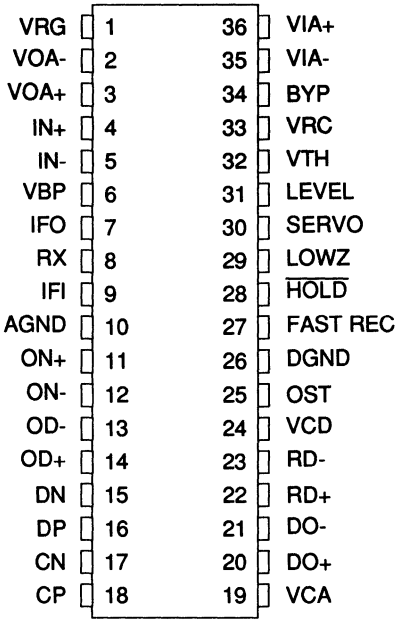
| | | | | | | |
|---|---|---|---|---|---|---|
| VC | CP-CN Signal Range | | | | 1.5 | Vpp |
| VOSC | Comparator Offset Voltage (Note 1) | | | | 4 | mV |
| RINC | Differential Input Resistance | | 8 | | 14 | kΩ |
| CINC | Differential Input Capacitance | | | | 5 | pF |
| TDS | D F/F Set Up Time | DP-DN threshold to CP-CN zero cross | | | 1 | ns |
| PP | Pulse Pairing | Vs = 1 Vpp, F = 18 MHz | | 0.15 | 0.5 | ns |
| TPDC | Propagation Delay to RD | Vs = 20 mVpp sq wave | | 7 | | ns |
| PWRD | RD Output Pulse Width | Tpd = 0.157 (Rt-196)(22pf + Cs)<br>Rt = 2K to 8 kΩ,<br>Cs = stray capacitance | 0.78 T pd | | 1.22 T pd | ns |
| RT | Resistor Range | | 3 | | 10 | kΩ |

Note 1: Not directly measurable

## PACKAGE PIN DESIGNATIONS
(Top View)

**Thermal Characteristics: θjA**

| | |
|---|---|
| 36-lead SOM | 75° C/W |




**36-Lead SOM**

## ORDERING INFORMATION

| PART DESCRIPTION | ORDER NO. | PKG. MARK |
|---|---|---|
| SSI 32P3000<br>36-Lead Small Outline (31.6 mil. pitch) | 32P3000-CM | 32P3000-CM |



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**Notes:**

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# SSI 32P3001
## Pulse Detector with Programmable Filter
## Preliminary Data

2

January 1993

## DESCRIPTION

The SSI 32P3001 is a bipolar integrated circuit that provides all the data processing for detection and qualification of encoded read signals from a head preamplifier. This device can handle a NRZ data rate of 64 Mbit/s.

The SSI 32P3001 includes an AGC amplifier with AGC charge pump, a programmable 7-pole Bessel low pass filter, and a pulse qualification circuit. The device features a complete differential circuit architecture in the signal path, for high immunity to noise and power supply ripples.

For fast write-to-read recovery, the SSI 32P3001 allows the user to control the low input state and AGC fast recovery mode independently. The AGC action can also be disabled for embedded servo decoding or other processing needs.

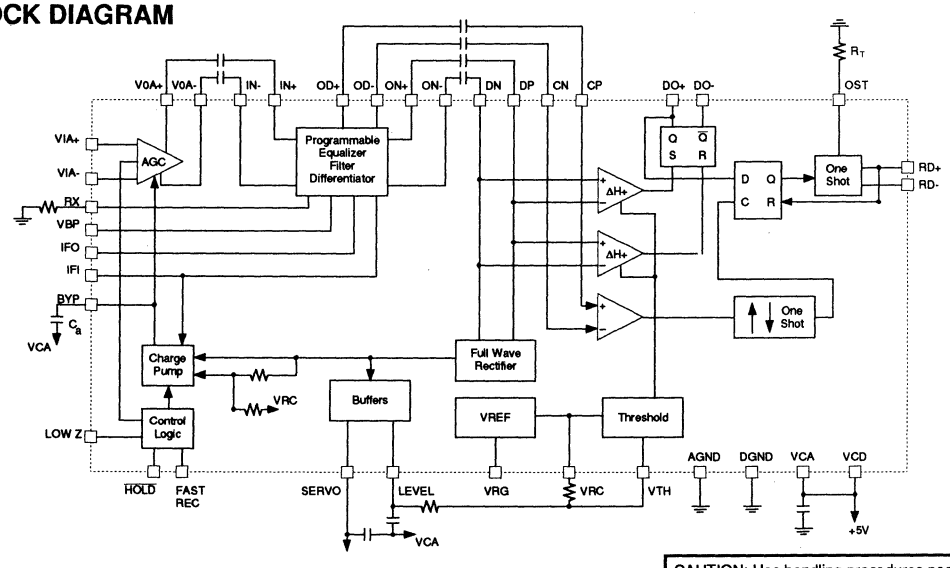
Ideal for constant density recording applications, the SSI 32P3001 low pass filter has a programmable 8-24 MHz bandwidth and 0 - 13 dB boost for pulse slimming. A time derivative of the read signal is also provided by the filter for time qualification in peak detection.

The SSI 32P3001 requires only a +5V power supply and is available in a 36-pin SOM package.

## FEATURES

- Compatible with 64 Mbit/s data rate operation
- Fast attack/decay modes for rapid AGC recovery
- Low Drift AGC hold, fast AGC recovery, and low AGC input impedance control signals
- Includes programmable pulse slimming equalization and programmable channel filter and differentiator with no external filter components
- ±0.5 ns filter group delay variation from 0.3 $fc$ to $fc$ = 24 MHz
- Independent positive and negative threshold qualification to suppress error propagation
- 0.5 ns max pulse pairing
- +5V only operation
- 36-pin SOM package

## BLOCK DIAGRAM




CAUTION: Use handling procedures necessary for a static sensitive component.

# SSI 32P3001
# Pulse Detector with Programmable Filter

## FUNCTIONAL DESCRIPTION

The SSI 32P3001 Pulse Detector is designed to support a 64 Mbit/s NRZ data rate. The signal processing circuits include a wide band variable gain amplifier, a dual-rate AGC charge pump, a programmable electronic filter, and a pulse qualifier.

### AGC Amplifier

The wide band AGC amplifier is to amplify the read signal from the read/write pre-amp to a signal level acceptable at the pulse qualifier. The AGC amplifier gain is an exponential function of the BYP voltage when referenced to VCA.

$$Av = Ao \exp[(\frac{V@BYP - Vr}{K})] \text{ (see note 1)}$$

### AGC Actions

The AGC loop is to maintain a constant DP/DN signal at the nominal level, ~1Vppd. The AGC actions are current charging and discharging the external BYP integrating capacitor. These AGC actions can be classified into the following categories:

#### Automatic

##### Slow Decay

When the DP/DN signal is below the nominal level, a slow decay current, Id, charges the BYP capacitor. The AGC amplifier gain is increased slowly. This slow decay current tracks with the bandwidth of the filter. Id = 0.008 x IFI. At T = 27°C, the maximum Id is 4.5 µA when the filter cutoff frequency is 24 MHz.

##### Slow Attack

When the DP/DN signal exceeds the nominal level but is below 125% of the nominal level, a slow attack current, Ich, discharges the BYP capacitor. The AGC amplifier gain is decreased. The slow attack current is 30 times that of the slow decay current. Thus, for a given BYP capacitor, the slow attack response time is quicker than the slow decay response.

Note 1: In a closed AGC loop, the sensitivity of Ao, Vr and K to typical process variations is irrelevant. The typical values of Ao, Vr and K are provided for references only, and not tested in production. Ao = 11, Vr = 3.6 and K = 0.22

##### Fast Attack

When the DP/DN signal exceeds 125% of the nominal level, the device enters a fast attack mode. A fast attack current, Ichf, discharges the BYP capacitor. The AGC amplifier gain is quickly lowered. The fast attack current is seven times that of the slow attack current.

#### User Control

##### FAST REC

When FAST REC = 1, the SSI 32P3001 enters the fast recovery mode. Independent of the DP/DN signal level, a fast recovery current, Idf, charges the BYP capacitor. This fast recovery current magnitude is 20 times that of the slow decay current. The AGC amplifier gain is quickly raised. Meanwhile, all the above automatic AGC actions remain active.

##### $\overline{\text{HOLD}}$

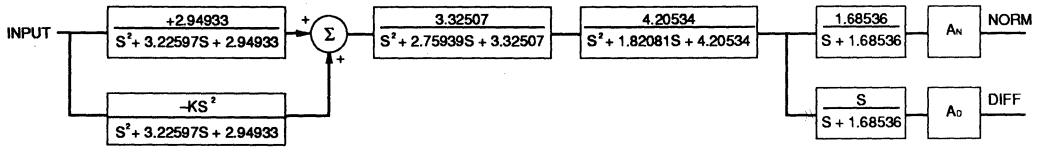
When HOLD = 0, all the automatic AGC actions and the fast recovery action are suspended. The BYP capacitor voltage remains constant, except for leakage effects.

### Programmable Filter

The SSI 32P3001 includes a programmable low pass filter following the AGC amplifier for (1) 2X voltage gain from filter input to filter outputs, (2) noise limiting, (3) pulse slimming, and (4) provision of a time differentiated signal. The low pass filter is of a 7-pole 2-zero Bessel type. The filter's un-boosted -3 dB bandwidth, defined as the cutoff frequency, is programmable from 8-24 MHz; the high frequency equalization is programmable from 0 - 13 dB at the cutoff frequency.

The filter input is ac-coupled from the AGC amplifier output. The filter's normal low pass output is ac-coupled to the data channel of the pulse qualifier. The differentiated low pass output is ac-coupled to the time channel of the pulse qualifier.

The normalized 7-pole 2-zero Bessel filter transfer function is given as:




The cutoff frequency, $fc$, is programmable with 3 pins: RX, IFO and IFI. At the RX pin, an external resistor to ground establishes a reference current, IFO = 0.75 / RX, at T = 27°C. IFI should be made proportional to IFO for $fc$ temperature stability. The cutoff frequency is related to the RX resistor, IFO and IFI currents by the following equation:

$$fc = 24 \cdot \frac{IFI}{IFO} \cdot \frac{1.25}{RX(k\Omega)} \cdot MHz$$

For a fixed cutoff frequency setting, IFO and IFI can be tied together. The cutoff frequency equation then reduces to:

$$fc = 24 \cdot \frac{1.25}{RX(k\Omega)} \cdot MHz$$

For programmable cutoff frequency, an external current DAC can be used. IFO should be the reference current into the DAC. The DAC output current drives IFI, which is then proportional to IFO. The DACF in the SSI 32D4661 Time Base Generator is designed to control $fc$ of the Silicon Systems programmable filters. When the DACF, which has a 4X current gain from its reference to fullscale output, is used, 5 kΩ RX is used. The $fc$ is then given by:

$$fc(MHz) = 24 \cdot \frac{F\_Code}{127}$$

where F_Code is a decimal code equivalent to the 7-bit input into the DACF.

The high frequency equalization is programmable with two pins: VRG and VBP. The VRG is a bandgap reference voltage, nominally equal to 2.33V. The voltage at the VBP pin determines the amount of high frequency boost at the cutoff frequency. The boost function is as the following:

$$Boost(dB) = 20\log_{10}[(Kb \cdot \frac{VBP}{VRG}) + 1]$$

$$Kb = 3.041 + 0.0276 \cdot fci$$

where fci is the ideal cutoff frequency in MHz.

For a fixed boost setting, a resistor divider between VRG and ground can be used with the divided voltage at the VBP pin. For programmable equalization, an external voltage DAC can be used. VRG should be the reference voltage to the DAC. The DAC output voltage is then proportional to VRG. The DACS in the SSI 32D4661 is designed to control the magnitude equalization of Silicon Systems' programmable filters. When DACS is used, the boost relation then reduces to:

$$Boost(dB) = 20\log_{10}[(\frac{Kb \cdot S\_Code}{127}) + 1]$$

### Pulse Qualification

The SSI 32P3001 validates each DP/DN peak by combination of level qualification and time qualification. In level qualification, a dual-comparator threshold detection eliminates errors due to low level additive noise. In time qualification, the filter's differentiated output is used to locate signal peaks.

### Level Qualification

The level qualification is performed by a dual comparator circuit. One comparator detects a positive peak by comparing the data signal with a positive threshold. The other comparator detects a negative peak by comparing the data signal with a negative threshold. Each comparator has a small hysteresis, 20% of the set threshold, to avoid false triggering by noise around the set threshold. Polarity check is added to ensure that the slope of two successive peaks is opposite in sign.

The SSI 32P3001 allows two ways of setting the thresholds: fixed threshold or DP/DN tracking threshold. Fixed threshold can be simply set by a DC voltage at the VTH pin, such as from a resistor divider from VCC to VRC (see note 2). The threshold at each comparator can be computed as: Hysteresis Gain • (VTH - VRC). The thresholds at the two comparators are of the same magnitude, but of opposite polarity. For high performance system applications, however, a fixed threshold is not recommended.

Note 2: VCC is the +5V supply. VRC is the bandgap voltage referenced from VCC, i.e., VRC = VCC - VRG.

DP/DN tracking threshold has the advantages of shorter write-to-read recovery time and lower probability of error with input amplitude drop out. The threshold is designed as a percentage of the DP/DN peak voltage. This technique can be implemented by feeding the LEVEL output, through a resistor divider network, to the VTH pin. For a given divider network attenuation $\alpha$, the equivalent input threshold, THR is:

$THR = V_{IN} \cdot LG \cdot \alpha \cdot GHYS\ Vpd$

For example if

$\alpha = 0.5$

$V_{IN} = 1\ Vppd = 500\ mVpd$

the equivalent input threshold is 290 mVpd or 58% of the input signal. While both the Level Gain and Hysteresis Gain bear a moderate tolerance due to typical process variation, they inversely track each other to yield a much tighter threshold accuracy in a closed loop.

While the external resistor divider ratio determines the qualification setting, the total resistance and the peak capture capacitor should be optimized for the system data rate. The RC time constant must be small enough to allow good response to changing DP/DN peak, but large enough to provide a constant threshold after a long duration of input absence.

The Pulse Qualifier output is the pseudo-ECL differential output, RD and $\overline{RD}$. Corresponding to each validated peak of the DP/DN signal, a one-shot pulse occurs at the RD/$\overline{RD}$ output. The pulse width of the one-shot pulse is determined by a external resistor from the OST pin to ground.

$$\text{Pulse Width(sec)} = 0.157 \cdot (R_{OST} - 196) \cdot (22pF + C_S)$$

$R_{OST} = 2k\Omega$ to $8k\Omega, C_S$ = stray capacitance

DO and $\overline{DO}$ form the differential output as test points to examine the data input of the qualifier D flip flop. These outputs should be left unconnected during normal operation.

## PIN DESCRIPTION

### INPUT PINS

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| VIA+, VIA- | I | AGC Amplifier input pins. |
| IN+, IN- | I | Equalizer/filter input pins. |
| DP, DN | I | Data inputs to data comparators and fullwave rectifier. |
| CP, CN | I | Differentiated data inputs to the clock comparator. |
| VTH | I | Threshold level setting input for the data comparators. |
| FAST REC | I | TTL compatible input when high puts the charge pump in the fast decay mode. |
| LOW Z | I | TTL compatible input when high reduces the AGC amplifier input resistance. |
| $\overline{HOLD}$ | I | TTL compatible input when low disables the AGC action by turning off the charge pump. |

## PIN DESCRIPTION (continued)

### OUTPUT PINS

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| VOA+, VOA- | O | AGC amplifier output pins. |
| ON+, ON- | O | Equalizer/filter normal output pins. |
| OD+, OD- | O | Equalizer/filter differentiated output pins. |
| DO+, DO- | O | PECL compatible data comparator latch output pins. |
| RD+, RD- | O | PECL compatible read data output pins. |
| LEVEL | O | Open NPN emitter output that provides a fullwave rectified signal for the VTH input. The signal is referenced to VRC. |
| SERVO | O | Open NPN emitter output that provides a fullwave rectified servo signal. The signal is referenced to VRC. |
| **ANALOG PINS** | | |
| OST | - | Pin for $R_T$ network to set RD output pulse width. An internal 22 pF capacitor has been included. |
| VRC | - | Reference voltage pin for SERVO and LEVEL. VRC is referenced to VCA. |
| VRG | - | Reference voltage pin for the programmable filter. VRG is referenced to ground. |
| VBP | - | The equalizer high frequency boost is set by an external voltage applied to this pin. VBP must be proportional to VRG. Programmable boost is implemented by using a DAC that uses VRG as its reference. A fixed amount of boost can be set by an external resistor divide network connected from VBP to VRG and GND. |
| RX | - | Pin to set filter reference current. External resistor Rx from this pin to ground sets the filter reference current IFO. |
| IFO | - | Reference current output pin. The reference current is normally supplied as the reference current to a current DAC which generates the programmable input current for the IFI pin. |
| IFI | - | Programmable filter input current pin. The filter cutoff frequency is proportional to the current into this pin. The current must be proportional to the reference current out of IFO. A fixed filter cutoff frequency is generated by connecting IFO to IFI and selecting Rx to set the desired frequency. |
| BYP | - | The AGC integrating capacitor $C_A$ is connected between BYP and VCA. |
| VCA, VCD | - | Analog and Digital +5V. |
| AGND, DGND | - | Pulse detector and filter ground. Must be tied together. |

## ELECTRICAL SPECIFICATIONS

Unless otherwise specified, 4.5V<VCC<5.5V, 0°C<Ta<70°C

**ABSOLUTE MAXIMUM RATINGS** (Operation above maximum ratings may damage the device.)

| PARAMETER | VALUE |
|---|---|
| Storage Temperature | -65 to +150°C |
| Junction Operating Temperature,Tj | +130°C |
| Supply Voltage, VCC, VCD | -0.3 to 7V |
| Voltage Applied to Inputs | -0.3 to VCC, VCD + 0.3V |

**RECOMMENDED OPERATING CONDITIONS**

| PARAMETER | | RATING | UNIT |
|---|---|---|---|
| Supply Voltage | VCD = VCC | 4.5 < VCC < 5.5 | V |
| Ambient Temperature, Ta | | 0<Ta<70 | °C |

**POWER SUPPLY**

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| ISS | Supply Current | | | 100 | | mA |
| PD | Power Dissipation | | | 550 | 660 | mW |

**LOGIC SIGNALS**

| | | | | | | |
|---|---|---|---|---|---|---|
| VIL | TTL Input Low Voltage | | -0.3 | | 0.8 | V |
| VIH | TTL Input High Voltage | | 2.0 | | VCC +0.3 | V |
| IIL | TTL Input Low Current | VIL = 0.4V | -0.4 | | | mA |
| IIH | TTL Input High Current | VIH = 2.7V | | | 0.1 | mA |
| VOHE | PECL Output High Voltage | | | | VCC -0.6 | V |
| VOLE | PECL Output Low Voltage | | VCC -1.9 | | | V |
| IOHE | PECL High Output Current | RD+, RD- only. The limit for DO+, DO- is 1 mA | 4 | | | mA |
| IOLE | PECL Low Output Current | RD+, RD- only. The limit for DO+, DO- is 1 mA | -4 | | | mA |
| VES | ECL Differential Output Swing \|VRD - $\overline{VRD}$\| | VCC = 5V | 0.75 | 0.85 | 0.95 | Vpd |
| TRF | ECL Output Rise and Fall Time | CL ≤ 10 pF, RD± only | | | 3.5 | ns |
| TCS | Control Input Switching Times | | | | 0.1 | µs |

**AGC AMPLIFIER**

The input signals are AC coupled to VIA+ and VIA-. VOA+ and VOA- are AC coupled to IN+ and IN-. ON+ and ON- are AC coupled to DP and DN. Ca 1000 pF. Fin = 4 MHz. Unless otherwise specified, the output is measured differentially at VOA+ and VOA-.

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| VIR | Input Range | Filter boost at $fc$ = 0 dB | 24 | | 240 | mVppd |
| | | Filter boost at $fc$ = 11 dB | 20 | | 100 | mVppd |
| VD | DP-DN voltage | VIA± = 0.1 Vppd * | 0.85 | | 1.05 | Vppd |
| VDV | DP-DN Voltage Variation | 24 mV < VIA± < 240 mV * | | | 8.0 | % |
| AVmin | AGC minimum gain | | | | 1.9 | V/V |
| AVmax | AGC maximum gain | | 22 | | | V/V |
| AVPV | Gain Sensitivity | | | 38 | | dB/V |
| DR | VOA± Dynamic Range | THD = 1% max | 0.75 | | | Vpp |
| RINDA | Differential Input Resistance | LOW Z = low | 3.7 | 5.8 | 7.4 | kΩ |
| RINSA | Single Ended Input Resistance | LOW Z = low | | 2.8 | | kΩ |
| | | LOW Z = high | | 100 | 150 | Ω |
| VOS | Output Offset Voltage Variation | from min gain to max gain | -200 | | +200 | mV |
| VIN | Input Referred Noise Voltage | gain = max, Rs = 0Ω filter not connected to VOA+, VOA-, BW = 15 MHz | | | 20 | nV/√Hz |
| BW | Bandwidth | No AGC action, 1.9<Av<22 | 55 | | | MHz |
| CMRR | Common Mode Rejection Ratio | gain = max, Vin = 0 VDC + 100 mVpp @ 5 MHz | 40 | 65 | | dB |
| PSRR | Power Supply Rejection Ratio | gain = max, 100 mVpp on VCA, VCD @ 5 MHz | 45 | 67 | | dB |
| GDT | Gain Decay Time | VIA± = 240 mV to 120 mV VOA± <0.9 Final Value | | 33 | | µs |
| GAT | Gain Attack Time | VIA± = 120 mV to 240 mV VOA± <1.1 Final Value | | 1.2 | | µs |

* AGC loop closed

## ELECTRICAL SPECIFICATIONS (continued)

Unless otherwise specified, 4.5<VCC<5.5, 0°C<Ta<70°C

### AGC CONTROL

The input signals are AC coupled to DP and DN. Ca = 1000 pF, LEVEL load = 50 µa, SERVO load = 100 µA, 100 µA < IFI < 600 µA.

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| VDI | DP-DN Signal Input Range | | 0.8 | | 1.2 | Vpp |
| ID | Discharge Current, Id | FAST REC = low<br>DP - DN = 0 | | 0.008 x IFI | | mA |
| IDF | Fast Discharge Current, Idf | FAST REC = high | | 20 x Id | | mA |
| ICH | Charge Pump Attack Current, Ich | DP - DN = 0.55V | | 30 x Id | | mA |
| ICHF | Charge Pump Fast Attack Current, Ichf | DP-DN = 0.675V | | 7 x Ich | | mA |
| IK | BYP Pin Leakage Current | $\overline{HOLD}$ = low,<br>VBYP = VCC -1.5V | -0.1 | | 0.1 | µA |
| VRG | Reference Voltage | Isource = 0 to 1 mA | 2.2 | | 2.45 | V |
| VRC | Reference Voltage | | | VCC-VRG | | V |
| IVRC | VRC Output Drive | ΔVRC < 20 mV | -0.75 | | 0.75 | mA |

**EQUALIZER/FILTER** The input signals are AC coupled to IN+ and IN-.

| | | | | | | |
|---|---|---|---|---|---|---|
| $fc$ | Filter Cutoff Frequency | RX = 5 kΩ<br>$fc$ = 24 x IFI/(4 x IFO ) MHz<br>4 ≥ IFI/IFO ≥ 4/3 | 8 | | 24 | MHz |
| IFO | IFO Reference Current Range | IFO = 0.75/RX; Tj = 27°C<br>5 kΩ > RX > 1.25 kΩ | 0.15 | | 0.6 | mA |
| IFI | IFI Program Current Range | Tj = 27°C, 24 MHz > $fc$ > 8 MHz | 0.2 | | 0.6 | mA |
| FCA | FCA Filter FC Accuracy | $fc$ nominal = 24 MHz | -13 | | 13 | % |
| RX | RX Range | | 1.25 | | 5 | kΩ |
| AO | Normal Low Pass Gain<br>AO = (ON ±) / (IN±) | Fin = 0.67$fc$ | 1.4 | | 2.2 | V/V |
| AD | Differentiated Low Pass Gain<br>AD = (ON ±) / (IN±) | Fin = 0.67$fc$ | 0.8AO | | 1.2AO | V/V |
| FBA | Frequency Boost | FB nominal VBP = VRG | -1.5 | | +1.5 | dB |
| | Accuracy | VBP/VRG = 0.5 | -1.0 | | +1.0 | dB |
| TGD1 | Group Delay Variation | $fc$ = 24 MHz, FB = 0 to 9 dB<br>$fc$ > Fin > 0.3$fc$,<br>VBP = 0 to VRG | -0.5 | | +0.5 | ns |

**EQUALIZER/FILTER** (continued)

The input signals are AC coupled to IN+ and IN-.

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| TGD2 | | $fc$ = 8 to 24 MHz, $fc$ > Fin > 0.3 $fc$, VBP = 0 to VRG | -2.5 | | +2.5 | % |
| VOSVF | Output Offset Voltage Variation | Normal and differentiated outputs, 200 µA < IFI < 600 µA | -200 | | +200 | mV |
| DRF | VOF Filter Output Dynamic Range | THD = 1.5% max Fin = 0.67 $fc$ | 1.2 | | | Vpp |
| RINF | Filter Input Resistance | | 3.0 | | | kΩ |
| CINF | Filter Input Capacitance | | | | 7 | pF |
| ROF | Filter Output Resistance | IO = 1 mA | | | 60 | Ω |
| IOF | Filter Output Current | | -1.0 | | 1.0 | mA |
| VNN | Eout Output Noise Voltage; ON+, ON- | NBW = 100 MHz, RS = 50Ω VBP = 0, $fc$ = 24 MHz | | 2.7 | 3.5 | mVRms |
| | | NBW = 100 MHz, RS = 50Ω VBP = VRG, $fc$ = 24 MHz | | 5.7 | 8.0 | mVRms |
| VND | Eout Output Noise Voltage; OD+, OD- | NBW = 100 MHz, RS = 50Ω VBP = 0, $fc$ = 24 MHz | | 5.7 | 7.5 | mVRms |
| | | NBW = 100 MHz, RS = 50Ω VBP = VRG, $fc$ = 24 MHz | | 13.0 | 21.0 | mVRms |

**DATA COMPARATOR**

The input signals are AC coupled to DP and DN. I (LEVEL) = 50 mA, I (SERVO) = 100 µA, 0.01 µF capacitors tied from LEVEL and SERVO to VCA

| | | | | | | |
|---|---|---|---|---|---|---|
| VID | DP-DN Signal Range | | | | 1.5 | Vpp |
| RIND | Differential Input Resistance | | 8 | | 14 | kΩ |
| CIND | Differential Input Capacitance | | | | 5 | pF |
| OSD | Comparator Offset Voltage (Note 1) | | | | 4 | mV |
| LG | Level (Servo) Output Gain | DP-DN = .5 to 1 Vppd | 0.712 | | 0.788 | V/Vppd |
| LBW | Level (Servo) Output Bandwidth | +1 dB referenced to 1 MHz | 20 | | | MHz |
| VLOS | Level Offset Voltage | Output-VRC, IL = 50 µA | -30 | | +30 | mV |
| VSOS | Servo Offset Voltage | Output - VRC, IL = 100 µA | -30 | | +30 | mV |
| GHYS | Threshold Voltage Gain | 0.3 < VTH-VRC < 0.9 @ 1 MHz | 0.77 | 0.8 | 0.83 | Vpd/V |
| VSH | Threshold Voltage Hysteresis (Note 1) | | | .20 x GHYS x (VTH - VRC) | | V/V |

Note 1: Not directly measurable

**DATA COMPARATOR** (continued)

The input signals are AC coupled to DP and DN.

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| VHM | Minimum Threshold Voltage | VTH-VRC ≤ 0.11V | | 0.05 | | Vpd |
| TPDD | Propagation Delay | From DP/DN to DO, $\overline{DO}$ | | 7 | | ns |
| IVTH | Input Bias Current | | | | 2 | µA |

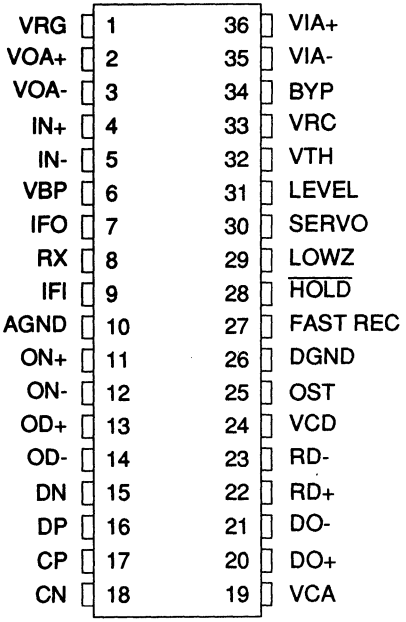
**CLOCKING**

The input signals are AC coupled to CP and CN.

| | | | | | | |
|---|---|---|---|---|---|---|
| VC | CP-CN Signal Range | | | | 1.5 | Vpp |
| VOSC | Comparator Offset Voltage (Note 1) | | | | 4 | mV |
| RINC | Differential Input Resistance | | 8 | | 14 | kΩ |
| CINC | Differential Input Capacitance | | | | 5 | pF |
| TDS | D F/F Set Up Time | DP-DN threshold to CP-CN zero cross | 0 | | | ns |
| PP | Pulse Pairing | Vs = 1Vpp, F = 11 MHz | | 0.15 | 0.5 | ns |
| TPDC | Propagation Delay to RD | Vs = 20 mVpp sq wave | | 10 | | ns |
| PWRD | RD Output Pulse Width | Tpd =0.157 (Rt-196)(22pf + Cs) Rt = 2K to 8K, Cs = stray capacitance | 0.78x Tpd | | 1.22x Tpd | ns |

Note 1: Not directly measurable

## PACKAGE PIN DESIGNATIONS
(Top View)




**36-Lead SOM**

### THERMAL CHARACTERISTICS : θja

| | |
|---|---|
| 36-Lead SOM | 75° C/W |

## ORDERING INFORMATION

| PART DESCRIPTION | ORDERING NUMBER | PACKAGE MARK |
|---|---|---|
| SSI 32P3001 | | |
| 36-Lead Small Outline (31.6 mil pitch) | 32P3001-CM | 32P3001-CM |

**Preliminary Data:** Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.



Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 573-6000, FAX (714) 573-6914

**Notes:**

silicon systems®
A TDK Group Company

# SSI 32P3011
## Pulse Detector with Programmable Filter
## Preliminary Data

2

January 1993

## DESCRIPTION

The SSI 32P3011 is a bipolar integrated circuit that provides all the data processing for pulse detection and four-burst servo capture from encoded read signals. This device can handle a NRZ data rate of 48 Mbit/s.

The SSI 32P3011 includes an AGC amplifier with AGC charge pump, a programmable 7-pole Bessel low pass filter, a pulse qualification circuit, and a 4-burst servo capture circuit. Automatic AGC control maintains a constant signal level into the pulse qualifier, and achieves fast write-to-read recovery. A time differentiator is included in the servo signal path, if so needed.

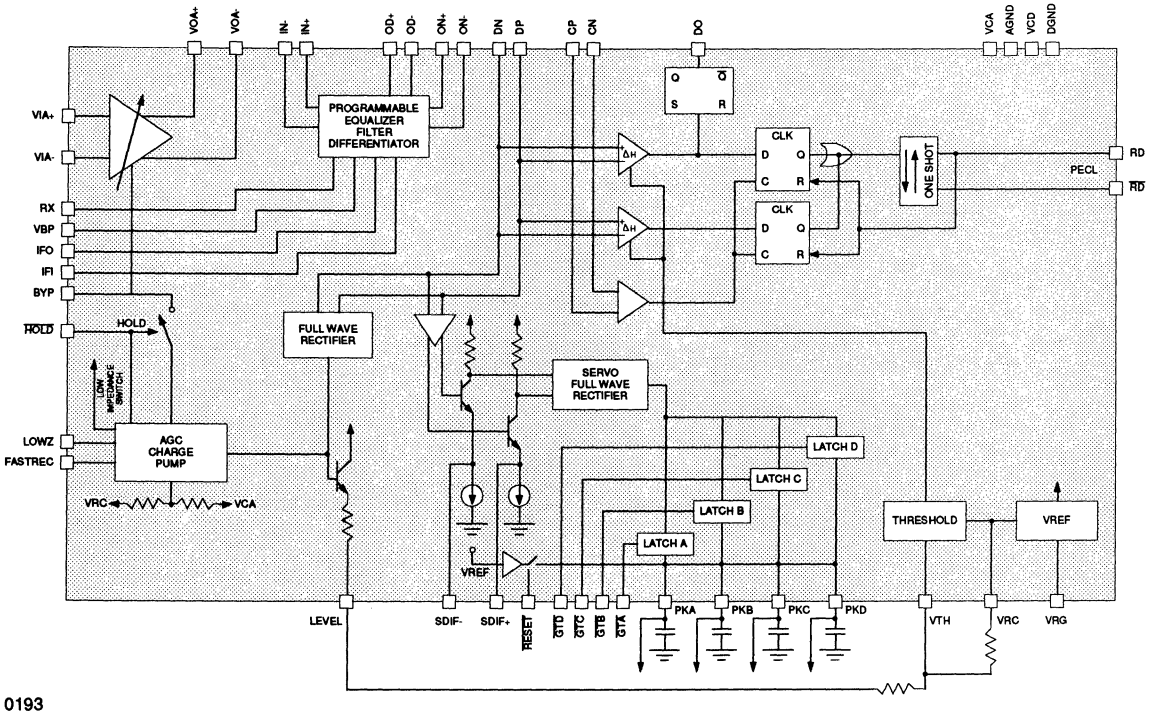
Ideal for constant density recording applications, the SSI 32P3011 low pass filter has a programmable 5-18 MHz bandwidth and 0-13 dB boost for pulse slimming. A time derivative of the read signal is also provided by the filter for time qualification in peak detection.

The SSI 32P3011 requires only a +5V power supply and is available in a 44-pin SOM package.

## FEATURES

- Compatible with 48 Mbit/s data rate operation
- Fast attack/decay modes for rapid AGC recovery
- Automatic AGC actions: Low Drift AGC hold, fast AGC recovery, and low AGC input impedance control signals
- Includes programmable pulse slimming equalization and programmable channel filter and differentiator with no external filter components
- ±0.75 ns filter group delay variation from $0.3fc$ to $fc$
  $fc$ = 18 MHz
- Independent positive and negative threshold qualification to suppress error propagation
- 0.5 ns max pulse pairing
- Servo differentiator and 4-burst servo capture
- +5V only operation
- 44-pin SOM package

## BLOCK DIAGRAM




0193

# SSI 32P3011
# Pulse Detector with Programmable Filter

## FUNCTIONAL DESCRIPTION

The SSI 32P3011 Pulse Detector/Filter with 4-Burst Servo Capture is designed to support a 48 Mbit/s NRZ data rate. The signal processing circuits include a wide band variable gain amplifier, a sophisticated dual-rate AGC charge pump, a programmable electronic filter, a pulse qualifier, a servo differentiator and a 4-burst servo capture circuit. The 4-Burst Servo Capture portion includes four gated servo peak detector/latches that can be reset.

### AGC Amplifier

The wide band AGC amplifier amplifies the read signal from the read/write pre-amp to a signal level acceptable at the pulse qualifier. The AGC amplifier gain is an exponential function of the BYP voltage when referenced to VR.

$$Av = Ao \exp[\frac{(V_{BYP} - VR)}{K}] \quad \text{(See note 1)}$$

### AGC Actions

The AGC loop maintains a constant DP/DN signal level at a nominal level, ~1 Vppd. The AGC actions are current charging and discharging to/from the external BYP integrating capacitor, and are classified into the following modes:

### AUTOMATIC

**Slow Decay**: When the DP/DN signal is below 1 Vppd, a slow decay current, Id, charges the BYP capacitor. The AGC amplifier gain is increased slowly. This slow decay current tracks with the bandwidth of the filter. Id = 0.008 x IFI. At T = 27°C, the maximum Id is 4.5 µA when the filter cutoff frequency is 18 MHz.

**Slow Attack**: When the DP/DN signal exceeds 1 Vppd, but is below 1.25 Vppd, a slow attack current, Ich, discharges the BYP capacitor. The AGC amplifier gain is decreased. The slow attack current is 20 times that of the slow decay current. Thus, for a given BYP capacitor, the slow attack response time is quicker than the slow decay response.

**Fast Attack**: When the DP/DN signal exceeds 1.25 Vppd, the device enters a fast attack mode. A fast attack current, Ichf, discharges the BYP capacitor. The AGC amplifier gain is quickly lowered. The fast attack current is seven times that of the slow attack current.

**Note:**

1. In a closed AGC loop, the sensitivity of Ao and K to typical process variations is irrelevant. The typical values of Ao and K are provided for reference only, and not tested in production. Ao = 11, K = 0.22, VR = 3.6.

### USER CONTROL

**Fast Recovery**: When FAST REC = 1, a fast decay current, IDF, continuously charges the BYP capacitor. This function raises the AGC amplifier gain rapidly. This fast decay current is 20 x ID. The automatic AGC actions remains active in the Fast Recovery mode. With the large Fast Attack current, the DP/DN signal level quickly reaches an equilibrium at ~ 125% of nominal level. Without the Fast Recovery function, the AGC amplifier gain can only be slowly increased with the slow decay current.

**Hold**: All the above AGC actions can be suspended with $\overline{HOLD}$ = 0. The AGC amplifier gain is held constant, except for any leakage effect at the BYP pin.

While the Fast Recovery function reduces the AGC amplifier gain recovery time, the input impedance control function speeds up the input settling. In a Write Mode, a large DC voltage could be stored at the external AC coupling capacitors. When switched back to the Read Mode, the DC voltage across these capacitors must settle to its normal level. With LOW_Z = 1, the input RC time constant is lower for fast input recovery.

### Programmable Filter

The SSI 32P3011 includes a programmable low pass filter following the AGC amplifier for (1) 2X voltage gain from the AGC amplifier output to the pulse qualifier input, (2) noise limiting, (3) pulse slimming, and (4) provision of a time differentiated signal. The low pass filter is of a 7-pole 2-zero Bessel type. The filter's unboosted -3 dB bandwidth, defined as the cutoff frequency, is programmable from 5-18 MHz; the high frequency equalization is programmable from 0-13 dB at the cutoff frequency.

The filter input is ac-coupled from the AGC amplifier output. The filter's normal low pass output is ac-coupled to the data channel of the pulse qualifier. The differentiated low pass output is ac-coupled to the time channel of the pulse qualifier.

The normalized 7-pole 2-zero Bessel filter transfer function is given in Figure 1.

The cutoff frequency, fc, is programmable with 3 pins: RX, IFO and IFI. At the RX pin, an external resistor to ground establishes a reference current:

$$IFO = \frac{0.75}{Rx}, \text{at } T = 27°C$$

IFI should be made proportional to IFO for $fc$ temperature stability. The cutoff frequency is related to the RX resistor, IFO and IFI currents as the following:

$$fc(MHz) = 22.5 \cdot \frac{IFI}{IFO} \cdot \frac{1}{Rx(k\Omega)}$$

For a fixed cutoff frequency setting, IFO and IFI can be tied together. The cutoff frequency equation then reduces to:

$$fc(MHz) = 22.5 \cdot \frac{1}{Rx(k\Omega)}$$

For programmable cutoff frequency, an external current DAC can be used. IFO should be the reference current into the DAC. The DAC output current drives IFI, which is then proportional to the IFO. The DACF in the SSI 32D4661 Time Base Generator is designed to control $fc$ of the Silicon Systems programmable filters. When the DACF, which has a 4X current gain from its reference to fullscale output, is used, 5 kΩ RX is used. The fc is then given by:

$$fc(MHz) = 18 \cdot \frac{F\_Code}{127}$$

where F_Code is the decimal code equivalent to the 7-bit input into the DACF.

The high frequency equalization is programmable with two pins: VRG and VBP. The VRG is a bandgap reference voltage, 2.3V typically. The voltage at the VBP pin determines the amount of high frequency boost at the cutoff frequency. The boost function is as follows:

$$Boost(dB) = 20\log_{10}\left[\left(\frac{Kb \cdot VBP}{VRG}\right) + 1\right]$$

$Kb = 0.03511\ fc + 3.556$

$fc$ is the ideal cutoff frequency in MHz.

For a fixed boost setting, a resistor divider between VRG to ground can be used with the divided voltage at the VBP pin. For programmable equalization, an external voltage DAC can be used. VRG should be the reference voltage to the DAC. The DAC output voltage is then proportional to the VRG. The DAC in the SSI 32D4661 is designed to control the magnitude equalization of Silicon Systems programmable filters.

When DACs are used, the boost relation then reduces to:

$$Boost(dB) = 20\log_{10}\left[\left(Kb \cdot \frac{S\_Code}{127}\right) + 1\right]$$

**Dual Hysteresis Comparator & Hysteresis Threshold Setting**

The SSI 32P3011 uses a dual comparator architecture to allow independent positive and negative threshold qualification. Each signal peak which exceeds the threshold is qualified regardless of the previous qualified peak's polarity. This has the advantage of suppressing error propagation, if one signal peak is weak in magnitude and missed.

The SSI 32P3011 allows two implementations of hysteresis: fixed by hysteresis threshold or DP/DN tracking hysteresis threshold. Fixed hysteresis threshold can be simply done by setting a DC voltage at the VTH pin, such as a resistor divider from VCC to VRC. The hysteresis threshold at the comparator can be computed as Hysteresis Gain x (VTH - VRC). For high performance system applications, however, the DP/DN tracking hysteresis threshold is recommended.

DP/DN tracking hysteresis has the advantages of shorter write-to-read recovery time and lower probability of error with input amplitude drop out. The hysteresis threshold is designed as a percentage of the DP/DN peak voltage. This technique can be implemented by feeding the LEVEL output, through a resistor divider network, to the VTH pin. The LEVEL output is an amplified and rectified replica of the DP/DN voltage. It can be computed as: Level Gain x (DP - DN) ppd + VRC. With the resistor divider, a fraction of the LEVEL output is presented at the VTH pin. The hysteresis threshold, as a function of (DP - DN)ppd, can be summarized as:

Level Gain x (DP - DN)ppd x Resistor Dividing Ratio x Hysteresis Gain.

For a typical case of 1Vppd at the DP/DN pins, assume equal value resistors in the divider network, the hysteresis threshold is 0.75 x 1 x 0.5 x 0.445 = 0.17 V. This represents 34% hysteresis on a 1Vppd signal.

While both the Level Gain and the Hysteresis Gain bear moderate tolerance due to typical process variations, they inversely track each other to yield a much tighter hysteresis threshold in a closed loop. In designing the hysteresis threshold, the nominal Level Gain and Hysteresis Gain values should be used. The tolerance on DP/DN tracking hysteresis threshold is specified as the Tracking Hysteresis Tolerance. With a 15% tolerance in the above example, the % hysteresis is expected between 34% x (1-0.15) = 29% to 34% x (1+0.15) = 39%.

While the external resistor divider ratio determines the hysteresis threshold, the total resistance and the peak capture capacitor should be optimized for the system data rate. The RC time constant must be small enough to allow good response to changing DP/DN peak-to-peak, but large enough to provide a constant hysteresis threshold in each level qualification.

The SSI 32P3011 provides a 4-Burst Servo Capture circuit. The signal at the DP/DN inputs is full wave rectified, level shifted and gated to servo peak detector / latches. A servo differentiator block is available if servo signal differentiation is necessary. The transfer function from DP/DN input to the differentiator output is given as:

$$\frac{\text{Vout@Differentiator}}{(\text{DP}-\text{DN})\text{ppd}} = \frac{2380Cs}{LCs^2+C(R+48.1)s+1}$$

where C, L and R are external passive components across SDIF+ and SDIF-

$15\ pF < C < 125\ pF$

$s = j\omega$

If servo signal differentiation is not needed, the servo differentiator can be turned into a ~1X gain block with a 2kΩ resistor across SDIF+ and SDIF-.

One master reset control, $\overline{RST}$, is used to initialize all four servo outputs, PKA-D, to a level below the offset bias of servo read data. Each servo burst is individually selected with its $\overline{GT}$- control. With GTA = 0, the DP/DN signal is full wave rectified and gated to PKA output. The PK- output is a peak captured 1Vp signal biased at 2.0V. The output signal can be between 2.0V to 3.0V. Figure 2 shows a typical servo timing sequence and the respective outputs.

## PIN DESCRIPTION

### INPUT PINS

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| VIA+, VIA- | I | AGC Amplifier input pins. |
| IN+, IN- | I | Equalizer/filter input pins. |
| DP, DN | I | Data inputs to data comparators and fullwave rectifier. |
| CP, CN | I | Differentiated data inputs to the clock comparator. |
| VTH | I | Threshold level setting input for the data comparators. |
| FAST REC | I | TTL compatible input. When high, the device is In Fast Decay Mode. |
| LOWZ | I | TTL compatible input. When high, the input impedance is lower for faster write-to-read recovery. |
| $\overline{GTA}$, $\overline{GTB}$, $\overline{GTC}$, $\overline{GTD}$ | I | TTL compatible input. When low the corresponding servo gate channel is enabled. |
| $\overline{HOLD}$ | I | TTL compatible input. When low the AGC action is suspended. |
| $\overline{RESET}$ | I | TTL input, when low, all four servo capture outputs are reset to a level below normal servo read bias. |

## PIN DESCRIPTION

### OUTPUT PINS

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| VOA+, VOA- | O | AGC amplifier output pins. |
| ON+, ON- | O | Equalizer/filter normal output pins. |
| OD+, OD- | O | Equalizer/filter differentiated output pins. |
| DO | O | ECL compatible data comparator latch output pin. |
| RD, $\overline{RD}$ | O | ECL compatible read data output pins. |
| SDIF+, SDIF- | - | Pins for external differentiating network for servo data. |
| PKA, PKB<br>PKC, PKD | O | Peak detector outputs. A 1000 pF hold capacitor must be connected between PKX and AGND. These outputs are high impedance when not enabled by $\overline{GTX}$ |
| **ANALOG PINS** | | |
| VRC | - | Reference voltage pin. VRC is referenced to VCA. |
| VRG | - | Reference voltage pin for the programmable filter. VRG is referenced to ground. |
| VBP | - | The equalizer high frequency boost is set by an external voltage applied to this pin. VBP must be proportional to VRG. Programmable boost is implemented by using a DAC that uses VRG as its reference. A fixed amount of boost can be set by an external resistor divide network connected from VBP to VRG and GND. |
| RX | - | Pin to set filter reference current. External resistor Rx from this pin to ground sets the filter reference current IFO. |
| IFO | - | Reference current output pin. The reference current is normally supplied as the reference current to a current DAC which generates the programmable input current for the IFI pin. |
| IFI | - | Programmable filter input current pin. The filter cutoff frequency is proportional to the current into this pin. The current must be proportional to the reference current out of IFO. A fixed filter cutoff frequency is generated by connecting IFO to IFI and selecting Rx to set the desired frequency. |
| BYP | - | The AGC integrating capacitor $C_A$ is connected between BYP and VCA. |
| VCA, VCD | - | Analog and Digital +5 volts. |
| AGND, DGND | - | Analog and Digital grounds. Must be tied together for proper operation. |

## ELECTRICAL SPECIFICATIONS

Unless otherwise specified, 4.5V < Vcc < 5.5V, 0°C<Ta<70°C

**ABSOLUTE MAXIMUM RATINGS** (Operation above maximum ratings may damage the device.)

| PARAMETER | VALUE |
|---|---|
| Storage Temperature | -65°C to +150°C |
| Junction Operating Temperature,Tj | +130°C |
| Supply Voltage, VCA, VCD | -0.7 to 7V |
| Voltage Applied to Inputs | -0.7 to VCA, VCD V |

**RECOMMENDED OPERATING CONDITIONS**

| PARAMETER | | RATING |
|---|---|---|
| Supply Voltage | VCA = VCD = VCC | 4.5V < VCC < 5.5V |
| Ambient Temperature, Ta | | 0°C<Ta<70°C |

**POWER SUPPLY**

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| PD | Power Dissipation | Outputs unloaded<br>4.5V < VCA, VCD < 5.5V | | 490 | 650 | mW |

**LOGIC SIGNALS**

| | | | | | | |
|---|---|---|---|---|---|---|
| VIL | TTL Input Low Voltage | | -0.3 | | 0.8 | V |
| VIH | TTL Input High Voltage | | 2.0 | | VCC +0.3 | V |
| IIL | TTL Input Low Current | VIL = 0.4V | -0.4 | | | mA |
| IIH | TTL Input High Current | VIH = 2.7V | | | 0.1 | mA |
| VOL | ECL Output High Voltage | VCC = 5V | VCC -1.2 | | | V |
| VOE | ECL Differential Output Swing | VCC = 5V | 0.3 | | | Vpp |
| TRF | EC1 Output Rise and Fall Time | CL ≤ 10 pF | | | 3.5 | ns |
| TS | Control Input Switching Times | | | | 0.1 | µs |
| VOLT | TTL Output Low Voltage | IOL = 4 mA | 0.5 | | | V |
| VOHT | TTL Output High Voltage | IOH = -400 mA | | | 2.7 | V |

**AGC AMPLIFIER**

The input signals are AC coupled to VIA+ and VIA-. VOA+ and VOA- are AC coupled to IN+ and IN-. ON+ and ON- are AC coupled to DP and DN. Ca 1000 pF. Fin = 4 MHz. Unless otherwise specified, the output is measured differentially at VOA+ and VOA-.

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| VIB | Input Range | Filter boost at $fc$ = 0 dB | 24 | | 240 | mVppd |
| | | Filter boost at $fc$ = 11 dB | 20 | | 100 | mVppd |
| VD | DP-DN Voltage | VIA± = 0.1 Vppd | 0.90 | | 1.10 | Vppd |
| VDV | DP-DN Voltage Variation | 24 mV < VIA± < 240 mV | | | 8.0 | % |
| AV | Gain Range | | 1.9 | | 22 | V/V |
| AVPV | Gain Sensitivity w.r.t. BYP Voltage | | | 28 | | dB/V |
| DR | VOA+ VOA- Dynamic Range | THD = 1% max | .75 | | | Vppd |
| RINDA | Differential Input Impedance | LOWZ = 0 | 4.7 | | 8.4 | kΩ |
| | | LOWZ = 1 | | 1 | | |
| RINSA | Single Ended Input Impedance | LOWZ = 0 | | 3 | | kΩ |
| | | LOWZ = 1 | | 0.5 | | kΩ |
| VOS | Differential Output Offset Variation | from min. gain to max. gain | -200 | | +200 | mV |
| VIN | Input Referred Noise Voltage | gain = max, Rs = 0Ω filter not connected to VOA+ and VOA-, Bw = 15 MHz | | | 15 | nV/√Hz |
| BW | Bandwidth | No AGC action, Gain = 22 | 55 | | | MHz |
| CMRR | Common Mode Rejection Ratio | gain = 22, Vin = 0 VDC + 100 mVpp @ 5 MHz | 40 | | | dB |
| PSRR | Power Supply Rejection Ratio | gain = 22, 100 mVpp on VCA, VCD @ 5 MHz | 45 | | | dB |
| TGD | Gain Decay Time | VIA± = 240 mV to 120 mV VOA± < 0.9 Final Value IFI = 600 µA | | 25 | | µs |
| TGA | Gain Attack Time | VIA± = 120 mV to 240 mV VOA± < 1.1 Final Value IFI = 600 µA | | 25 | | µs |

## ELECTRICAL SPECIFICATIONS (continued)

Unless otherwise specified, 4.5V<VCC<5.5V, 0°C<Ta<70°C

### AGC CONTROL

The input signals are AC coupled to DP and DN. Ca = 1000 pF.

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| VDI | DP-DN Signal Input Range | | | | 1.5 | Vpp |
| ID | Discharge Current | $\overline{WG}$ = 1, DP - DN = 0V | | 0.008 x IFI | | A |
| IDF | Fast Discharge Current | | | 20 x Id | | A |
| ICH | Charge Pump Attack Current | $\overline{WG}$ = 1, DP - DN = 0.55V | | 30 x Id | | A |
| ICHF | Charge Pump Fast Attack Current, Ichf | $\overline{WG}$ = 1, DP - DN = 0.675V | | 7 x Ich | | A |
| IK | BYP Pin Leakage Current | $\overline{HOLD}$ = 0 | -0.1 | | +0.1 | µA |
| VRC | VRC Reference Voltage | | | VCA -VRG | | V |
| IVRC | VRC Output Drive | | -0.75 | | +0.75 | mA |
| VRG | VRG Reference Voltage | Isource 0mA to 1mA | 2.2 | | 2.45 | V |

### EQUALIZER/FILTER

The input signals are AC coupled to IN+ and IN-.

| | | | | | | |
|---|---|---|---|---|---|---|
| *fc* | Filter Cutoff Frequency | $fc(MHz) = 22.5 \cdot \frac{IFI}{IFO} \cdot \frac{1}{Rx(k\Omega)}$ | 5 | | 18 | MHz |
| IFO | IFO Reference Current | IFO = 0.75/RX; Tj = 27°C<br>5kΩ > RX > 1.25 kΩ | 0.15 | | 0.6 | mA |
| RIFO | IFO Output Impedence | IFO = 0.6 mA @ Tj = 27°C | 25 | | | kΩ |
| VIFO | IFO Output Voltage Compliance | IFO = changes < 2.5% | 0 | | Vcc -1.5 | V |
| IFI | IFI Program Current Range | Tj = 27°C, 27 MHz > *fc* > 9 MHz | 0.167 | | 0.6 | mA |
| RIFI | IFI Input Impedence | IFI = 0.6 mA @ Tj = 27°C | | | 2.5 | kΩ |
| VIFI | IFI Input Bias Voltage | IFI = 0.6 mA @ Tj = 27°C | 0.75 | | 2.5 | V |
| FCA | FCA Filter FC Accuracy | *fc* = 18 MHz | -10 | | 10 | % |
| RX | RX Range | | 1.25 | | 5 | kΩ |
| AO | Normal Low Pass Gain<br>AO = (ON ±) / (IN±) | Fin = 0.67*fc* | 1.4 | | 2.2 | V/V |
| AD | Differentiated Low Pass Gain<br>AD = (OD ±) / (IN±) | Fin = 0.67*fc* | 0.9AO | | 1.3AO | V/V |

**EQUALIZER/FILTER** (continued)
The input signals are AC coupled to IN+ and IN-.

| PARAMETER | | CONDITIONS | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| FBA | Boost Accuracy | VBP = VRG | $fc$ = 5 MHz | 12 | 13.5 | 15 | dB |
| | | | $fc$ = 18 MHz | 12.8 | 14.3 | 15.8 | dB |
| | | VBP/VRG = 0.533 | $fc$ = 5 MHz | 8.5 | 9.5 | 10.5 | dB |
| | | | $fc$ = 18 MHz | 9.2 | 10.2 | 11.2 | dB |
| TGD1 | Group Delay Variation | $fc$ = 18 MHz, VBP = 0 to VRG<br>$fc$ > Fin > 0.3 $fc$ | | -0.75 | | +0.75 | ns |
| TGD2 | | $fc$ = 5 to 18 MHz, VBP = 0 to VRG<br>$fc$ > Fin > 0.3 $fc$ | | -2.5 | | +2.5 | % |
| VOSVF | Output Offset Voltage Variation | 150 µA < IFI < 600 µA | | -200 | | +200 | mV |
| DRF | VOF Filter Output Dynamic Range | THD = 1.5% max<br>Fin = 0.67 $fc$ | | 1.5 | | | Vpp |
| RINF | Filter Input Resistance | | | 3.0 | 4 | | kΩ |
| CINF | Filter Input Capacitance | | | | | 7 | pF |
| ROF | Filter Output Resistance | IO = 0.5 mA | | | | 60 | Ω |
| IOF | Filter Output Current | | | -1.0 | | 2.0 | mA |
| VNN | Eout Output Noise Voltage; ON+, ON- | BW = 100 MHz, RS = 50Ω<br>VBP = 0, $fc$ = 27 MHz | | | 2.7 | | mVRms |
| | | BW = 100 MHz, RS = 50Ω<br>VBP = VRG, $fc$ = 27 MHz | | | 5.7 | | mVRms |
| VND | Eout Output Noise Voltage; OD+, OD- | BW = 100 MHz, RS = 50Ω<br>VBP = 0, $fc$ = 27 MHz | | | 5.5 | | mVRms |
| | | BW = 100 MHz, RS = 50Ω<br>VBP = VRG, $fc$ = 27 MHz | | | 13.0 | | mVRms |

**DATA COMPARATOR**
The input signals are AC coupled to DP and DN.

| | | | | | | |
|---|---|---|---|---|---|---|
| VID | DP-DN Signal Range | | | | 1.5 | Vpp |
| RIND | Differential Input Resistance | | 8 | | 14 | kΩ |
| CIND | Differential Input Capacitance | | | | 5 | pF |
| VOSD | Comparator Offset Voltage (Note 1) | | | | 4 | mV |

**DATA COMPARATOR** (continued)
The input signals are AC coupled to DP and DN.

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| GLEV | Level Output Gain | DP-DN = 0.25 to 0.5 VDC | 0.712 | | 0.788 | V/V |
| RLEV | Level Output Resistance | | | 120 | | Ω |
| HYS | Threshold Voltage Gain | 0.2V < VTH-VRC < 1.1V | 0.41 | | 0.48 | V/V |
| VSH | Threshold Voltage Hysteresis (Note 1) | | | .20 x GHYS x (VTH -VRC) | | V/V |
| TPDD | Propagation Delay | From DP-DN to DO | | 6 | | ns |
| IVTH | VTH Input Bias Current | | | | 2 | µA |

**CLOCKING**
The input signals are AC coupled to CP and CN.

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| VIC | CP-CN Signal Range | | | | 1.5 | Vppd |
| VOSC | Comparator Offset Voltage | | | | 4 | mV |
| RINC | Differential Input Resistance | | 8 | | 14 | kΩ |
| CINC | Differential Input Capacitance | | | | 5 | pF |
| TDS | D Flip-Flop Set Up Time | DP-DN threshold to CP-CN zero cross, CP-CN = 1Vppd at 18 MHz | 0 | | | ns |
| PP | Pulse Pairing | | | | 0.5 | ns |
| TPDC | Propagation Delay from CP-CN zero crossing to RD | | | 9 | | ns |
| PWRD | RD Output Pulse Width Accuracy | PW = 9 X 18 / $fc$ (MHz) ns | -20 | | +20 | % |

**SERVO DIFFERENTIATOR/FULL-WAVE RECTIFIER**

An external series network is connected between SDIF and $\overline{SDIF}$ to determine the servo differentiator transfer function. The input signals are AC coupled to DP and DN. Fin = 6.7 MHz at 1.0 Vppd.

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| ISDIF | SDIF to $\overline{SDIF}$ pin current | Differentiator impedance must must be set so as not to dip the signal for this level | 0.7 | 1.0 | 1.3 | mA |
| RDIF | Internal differentiator pull-up resistors | Cannot be directly tested | 1.0 | 1.2 | 1.4 | kΩ |
| FWR | Input voltage range to maintain FWR voltage gain | Cannot be directly tested | 0.1 | | 1.2 | Vppd |
| RERR | Rectification Error | | | | 5 | % |
| AFWR | FWR Voltage Gain from FWR Input to PKA-D Outputs | | 0.72 | 0.9 | 1.08 | Vpp/Vppd |
| VCOS | PKA-D Channel to Channel Offset | 1Vppd input to servo FWR | -10 | | +10 | mV |
| PKOB | PKA-D Output Bias | | 1.8 | 2 | 2.2 | V |
| PK | PKA-D Output Levels | | PKOB | | PKOB+1 | V |
| PKRST | PKA-D Output Reset Level | $\overline{RESET}$ = Low | PKOB-1 | | PKOB-0.1 | V |
| IRST | PKA-D Peak Reset Discharge Current on each output | | 480 | 700 | 1000 | µA |
| PKLK | PKA-D Leakage Current | Channel Disabled: DP-DN = 1 Vpdd | | | 10 | µA |
| IPK | PKA-D Peak Charging Current | | 10 | 20 | | mA |
| TRON | Reset Current Turn On Delay from $\overline{RST}$ Fall | | | | 50 | ns |
| TROFF | Reset Current Turn Off Delay from $\overline{RST}$ Rise | | | | 100 | ns |
| TSUR | RST Rise Setup Time to GT-Falls | | 100 | | | ns |
| TSUG | GT-Rise Setup Time to Next GT-Fall | | 100 | | | ns |

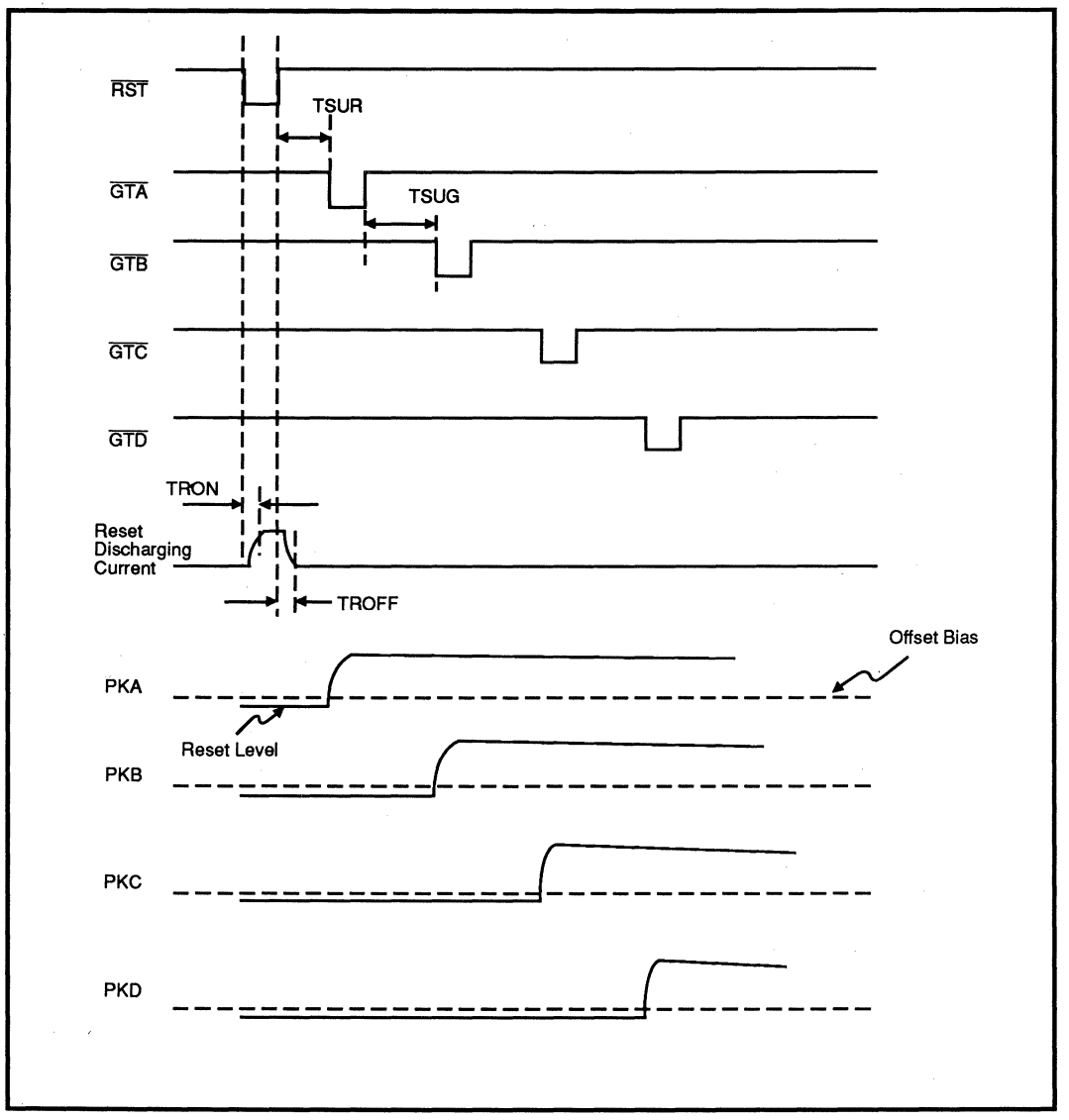
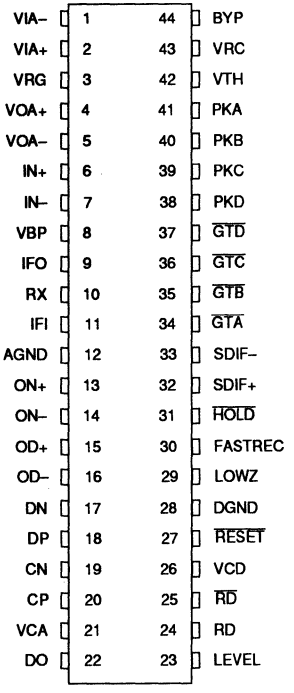



**FIGURE 2: Servo Capture Timing Sequence**

## PACKAGE PIN DESIGNATIONS
(Top View)

**THERMAL CHARACTERISTICS: θja**

| | |
|---|---|
| **44-Lead SOM** | **70°C/W** |




**32P3011**
**44-Lead SOM**

## ORDERING INFORMATION

| PART DESCRIPTION | ORDERING NUMBER | PACKAGE MARK |
|---|---|---|
| SSI 32P3011 | | |
| 36-Lead Small Outline (31.6 mil pitch) | 32P3011-CM | 32P3011-CM |

**Preliminary Data:** Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.



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**Notes:**

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# SSI 32P3013
## Pulse Detector with Programmable Filter
## Preliminary Data

2

January 1993

## DESCRIPTION

The SSI 32P3013 is a bipolar integrated circuit that provides all the data processing for pulse detection and four-burst servo capture from encoded read signals. This device can handle a NRZ data rate of 48 Mbit/s.

The SSI 32P3013 includes an AGC amplifier with AGC charge pump, a programmable 7-pole Bessel low pass filter, a pulse qualification circuit, and a 4-burst servo capture circuit. Automatic AGC control maintains a constant signal level into the pulse qualifier, and achieves fast write-to-read recovery. A time differentiator is included in the servo signal path, if so needed.

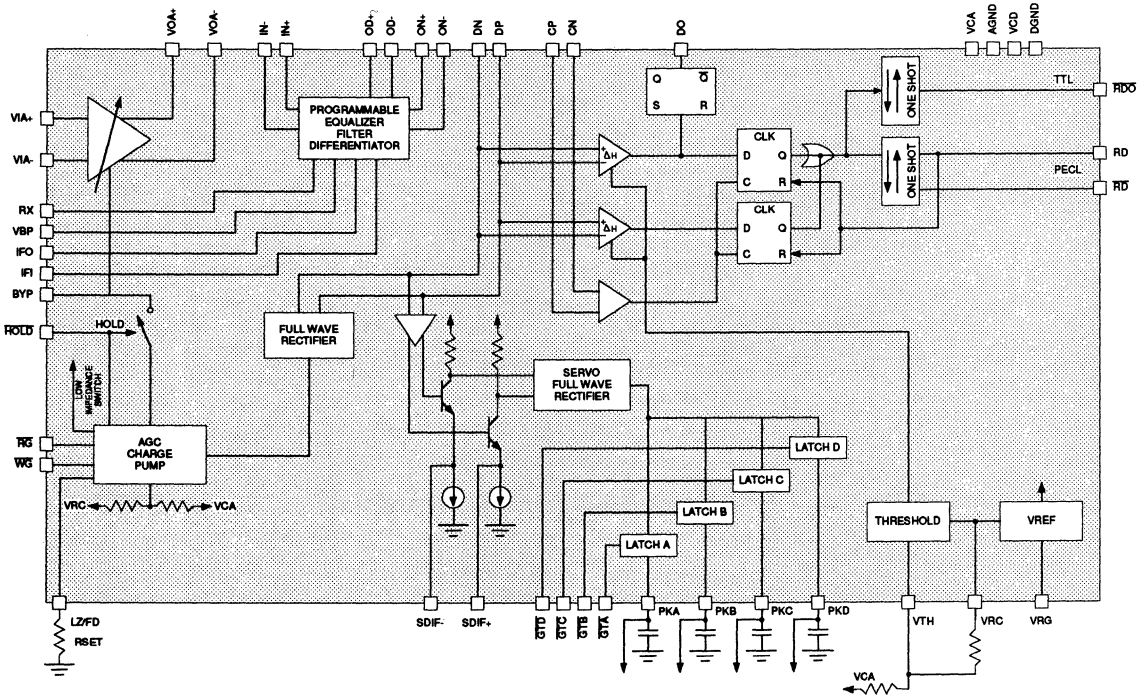
Ideal for constant density recording applications, the SSI 32P3013 low pass filter has a programmable 9-27 MHz bandwidth and 0-13 dB boost for pulse slimming. A time derivative of the read signal is also provided by the filter for time qualification in peak detection.

The SSI 32P3013 requires only a +5V power supply and is available in a 44-pin SOM package.

## FEATURES

- Compatible with 48 Mbit/s data rate operation
- Fast attack/decay modes for rapid AGC recovery
- Automatic AGC actions: Low Drift AGC hold, fast AGC recovery, and low AGC input impedance control signals
- Includes programmable pulse slimming equalization and programmable channel filter and differentiator with no external filter components
- ±0.5 ns filter group delay variation from 0.3FC to FC, FC = 27 MHz
- Independent positive and negative threshold qualification to suppress error propagation
- 0.5 ns max pulse pairing
- Servo differentiator and 4-burst servo capture
- +5V only operation
- 44-pin SOM package

## BLOCK DIAGRAM

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# SSI 32P3013
# Pulse Detector with Programmable Filter

## FUNCTIONAL DESCRIPTION

The SSI 32P3013 Pulse Detector/Filter with 4-Burst Servo Capture is designed to support a 48 Mbit/s NRZ data rate. The signal processing circuits include a wide band variable gain amplifier, a sophisticated dual-rate AGC charge pump, a programmable electronic filter, a pulse qualifier, a servo differentiator and a 4-burst servo capture circuit.

### Modes of Operation

The SSI 32P3013 can operate in one of three modes as controlled by $\overline{RG}$ and $\overline{WG}$.

**Normal Read Mode** $\overline{RG}$ = 0, $\overline{WG}$ = 1

In the normal Read Mode, the AGC actions are active. The AGC amplifier processes the input signal pulses; one-shot pulses are generated at the RD and $\overline{RD}$ outputs for each qualified signal peak. The $\overline{RDO}$ output buffer, which is a TTL buffer of the RD/$\overline{RD}$, is disabled and its output is pulled up high to reduce jitter and noise.

**Servo Read Mode** $\overline{RG}$ = 1, $\overline{WG}$ = 1

In the servo Read Mode, the AGC actions remain active (See note 1). The servo signal is amplified, fullwave rectified, differentiated and gated to the proper peak capture capacitor. The pulse qualifier remains active, and the $\overline{RDO}$ output is active to aid in servo decode.

**Write Mode** $\overline{RG}$ = X, $\overline{WG}$ = 0

In the Write Mode, the AGC actions are suspended. The AGC amplifier input impedance is clamped low to facilitate fast recovery. The $\overline{RDO}$ output is disabled and pulled up high to reduce jitter and noise.

### AGC Amplifier

The wide band AGC amplifier amplifies the read signal from the read/write pre-amp to a signal level acceptable at the pulse qualifier. The AGC amplifier gain is an exponential function of the BYP voltage when referenced to VR.

$$Av = Ao \exp[\frac{(V_{BYP} - VR)}{K}] \quad \text{(See note 2)}$$

### AGC Actions

The AGC loop maintains a constant DP/DN signal level at a nominal level, ~1 Vppd. The AGC actions are current charging and discharging to/from the external BYP integrating capacitor, and are classified into the following modes:

**Normal Read and Servo Read Mode ($\overline{RG}$ = X, $\overline{WG}$ = 1)**

**Slow Decay**: When the DP/DN signal is below 1 Vppd, a slow decay current, Id, charges the BYP capacitor. The AGC amplifier gain is increased slowly. This slow decay current tracks with the bandwidth of the filter. Id = 0.008 x IFI. At T = 27°C, the typical Id is 4.8 µA when the filter cutoff frequency is 27 MHz.

**Slow Attack**: When the DP/DN signal exceeds 1 Vppd, but is below 1.25 Vppd, a slow attack current, Ich, discharges the BYP capacitor. The AGC amplifier gain is decreased. The slow attack current is 20 times that of the slow decay current. Thus, for a given BYP capacitor, the slow attack response time is quicker than the slow decay response.

**Fast Attack**: When the DP/DN signal exceeds 1.25 Vppd, the device enters a fast attack mode. A fast attack current, Ichf, discharges the BYP capacitor. The AGC amplifier gain is quickly lowered. The fast attack current is seven times that of the slow attack current.

In servo Read Mode, constant AGC amplifier gain is generally desirable. Without an external AGC hold control, the servo data amplitude should be made lower than that of the data signal prior to the servo read mode. The SSI 32P3013 then enters the slow decay mode, which has a very slow effect on the AGC amplifier gain.

**Write Mode ($\overline{RG}$ = X, $\overline{WG}$ = 0)**

In the write mode, the AGC charge pump is disabled. This holds the AGC amplifier gain at its previous value.

Notes:

1. The servo signal should have a lower amplitude than the data signal prior to the servo read mode. Servo read should be completed before and significant change in AGC amplifier gain is resulted from the slow decay AGC mode.

2. In a closed AGC loop, the sensitivity of Ao and K to typical process variations is irrelevant. The typical values of Ao and K are provided for reference only, and not tested in production. Ao = 11, K = 0.22, VR = 3.6.

**Write-to-Read Transition**
**($\overline{RG}$ = X, $\overline{WG}$ = 0-to-1)**

When the SSI 32P3013 switches from the write to read mode, i.e., $\overline{WG}$ 0-to-1 transition, the device remains in the low input impedance state for a preset time period. For the next time period, the device then enters either the fast decay or attack mode depending on the signal level at the DP/DN pins. The time period, $\tau$, is determined by an external resistor, RT, from the LZ/FD pin to ground.

$$\tau(\mu s) = \frac{RT(k\Omega)}{28}$$

For example, with RT = 30 kΩ, each time period is 1.07 µs.

**Programmable Filter**

The SSI 32P3013 includes a programmable low pass filter following the AGC amplifier for (1) 2X voltage gain from the AGC amplifier output to the pulse qualifier input, (2) noise limiting, (3) pulse slimming, and (4) provision of a time differentiated signal. The low pass filter is of a 7-pole 2-zero Bessel type. The filter's unboosted -3 dB bandwidth, defined as the cutoff frequency, is programmable from 9-27 MHz; the high frequency equalization is programmable from 0-13 dB at the cutoff frequency.

The filter input is ac-coupled from the AGC amplifier output. The filter's normal low pass output is ac-coupled to the data channel of the pulse qualifier. The differentiated low pass output is ac-coupled to the time channel of the pulse qualifier.

The normalized 7-pole 2-zero Bessel filter transfer function is given in Figure 1.

The cutoff frequency, fc, is programmable with 3 pins: RX, IFO and IFI. At the RX pin, an external resistor to ground establishes a reference current:

$$IFO = \frac{0.75}{Rx}, \text{at } T = 27°C$$

IFI should be made proportional to IFO for $fc$ temperature stability. The cutoff frequency is related to the RX resistor, IFO and IFI currents as the following:

$$fc(MHz) = 27 \cdot \frac{IFI}{IFO} \cdot \frac{1.25}{Rx(k\Omega)}$$

For a fixed cutoff frequency setting, IFO and IFI can be tied together. The cutoff frequency equation then reduces to:

$$fc(MHz) = 27 \cdot \frac{1.25}{Rx(k\Omega)}$$

For programmable cutoff frequency, an external current DAC can be used. IFO should be the reference current into the DAC. The DAC output current drives IFI, which is then proportional to the IFO. The DACF in the SSI 32D4661 Time Base Generator is designed to control $fc$ of the Silicon Systems programmable filters. When the DACF, which has a 4X current gain from its reference to fullscale output, is used, 5 kΩ RX is used. The fc is then given by:

$$fc(MHz) = 27 \cdot \frac{F\_Code}{127}$$

where F_Code is the decimal code equivalent to the 7-bit input into the DACF.

The high frequency equalization is programmable with two pins: VRG and VBP. The VRG is a bandgap reference voltage, 2.3V typically. The voltage at the VBP pin determines the amount of high frequency boost at the cutoff frequency. The boost function is as follows:

$$Boost(dB) = 20\log_{10}\left[\left(\frac{Kb \cdot VBP}{VRG}\right) + 1\right]$$

$$Kb = 3.041 + 0.0276 \cdot fci$$

where fci is the ideal cutoff frequency in MHz.

For a fixed boost setting, a resistor divider between VRG to ground can be used with the divided voltage at the VBP pin. For programmable equalization, an external voltage DAC can be used. VRG should be the reference voltage to the DAC. The DAC output voltage is then proportional to the VRG. The DAC in the SSI 32D4661 is designed to control the magnitude equalization of Silicon Systems programmable filters.

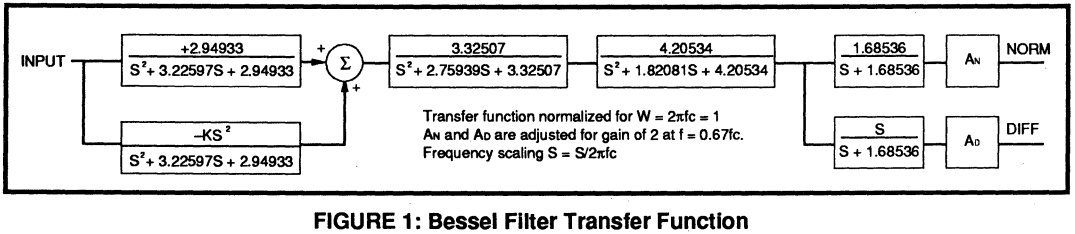



**FIGURE 1: Bessel Filter Transfer Function**

When DACs are used, the boost relation then reduces to:

$$Boost(dB) = 20\log_{10}[(Kb \bullet \frac{S\_Code}{127}) + 1]$$

**Pulse Qualification**

The SSI 32P3013 validates each DP/DN peak by a combination of level qualification and time qualification. In level qualification, a dual-comparator threshold detection eliminates errors due to low level additive noise. In time qualification, the filter's differentiated output is used to locate signal peaks.

**Level Qualification**

The dual-comparator architecture allows independent detection for positive and negative peaks. One comparator detects a positive peak by comparing the data signal with a positive threshold. The other comparator detects a negative peak by comparing the data signal with a negative threshold. Each comparator has a small hysteresis, 20% of the set threshold, to help qualify signals which just clear the set threshold.

The SSI 32P3013 comparator thresholds are set by a DC voltage at the VTH pin, such as from a resistor divider from VCA to VRC (see note 3). The threshold at each comparator can be computed as: Hysteresis Gain x (VTH - VRC). The thresholds at the two comparators are of the same magnitude, but of opposite polarity.

The SSI 32P3013 has three sets of pulse detector outputs: RD/$\overline{RD}$, $\overline{RDO}$, and DO/$\overline{DO}$. RD/$\overline{RD}$ output is the pseudo-ECL differential output. Corresponding to each validated peak of the DP/DN signal, a one-shot pulse occurs at the RD/$\overline{RD}$ output. The pulse width of the one-shot pulse is determined by an internal timing circuit, and specified in the electrical specification.

$\overline{RDO}$ is the TTL output of the pulse detector, logically equivalent to RD/$\overline{RD}$. Again, a one-shot pulse occurs at the $\overline{RDO}$ output for each validated peak of the DP/DN signal. The pulse width of this one-shot pulse is also specified in the electrical specification. DO/$\overline{DO}$ outputs are differential test points used to monitor the outputs of the internal comparators. Each is an open-emitter output requiring a 5 kΩ external resistor pull-down to ground.

**Four-Burst Servo Differentiator and Capture**

The SSI 32P3013 supports advanced embedded 4-burst servo technique. The signal at the DP/DN input can be time differentiated, fullwave rectified, and gated onto the selected peak capture output. A peak capture output is selected by pulling its corresponding $\overline{GT}$ x to logic '0.'

The transfer function from the DP/DN to the servo fullwave rectifier input is:

$$Av = \frac{2380Cs}{LCs^2 + (R + 48.1)Cs + 1}$$

where: R, L, and C are external passive components across SDIF±

$$15\ pF < C < 125\ pF$$
$$s = jw$$

When the time differentiation function is not desired, a 2 kΩ resistor should be used across the SDIF± pins.

The transfer function from the servo fullwave rectifier input to the peak capture output is set so that a 1 Vppd DP/DN signal produces 0.95 Vpeak output. With no signal input, the outputs are set close to ground, with a finite offset common to all four channels.

Note 3: VCA is the +5V supply. VRC is the bandgap voltage referenced from VCA, i.e., VRC = VCA - VRG.

## PIN DESCRIPTION

**INPUT PINS**

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| VIA+, VIA- | I | AGC Amplifier input pins. |
| IN+, IN- | I | Equalizer/filter input pins. |
| DP, DN | I | Data inputs to data comparators and fullwave rectifier. |
| CP, CN | I | Differentiated data inputs to the clock comparator. |
| VTH | I | Threshold level setting input for the data comparators. |
| $\overline{WG}$ | I | TTL compatible input. When low the device is in Write Mode. |

## PIN DESCRIPTION

**INPUT PINS** (continued)

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| $\overline{RG}$ | I | TTL compatible input. When low, the device is In normal Read Mode. |
| $\overline{WG}$ | I | TTL compatible input. When low, the device is in Write Mode. When both $\overline{RG}$ and $\overline{WG}$ are low, the device is in Servo Mode. |
| $\overline{GTA}$, $\overline{GTB}$, $\overline{GTC}$, $\overline{GTD}$ | I | TTL compatible input. When low the corresponding servo gate channel is enabled. |
| $\overline{HOLD}$ | I | TTL compatible input. When low the AGC action is suspended. |
| **OUTPUT PINS** | | |
| VOA+, VOA- | O | AGC amplifier output pins. |
| ON+, ON- | O | Equalizer/filter normal output pins. |
| OD+, OD- | O | Equalizer/filter differentiated output pins. |
| DO | O | ECL compatible data comparator latch output pin. |
| RD, $\overline{RD}$ | O | ECL compatible read data output pins. |
| $\overline{RDO}$ | O | TTL compatible read data output. |
| SDIF+, SDIF- | - | Pins for external differentiating network for servo data. |
| PKA, PKB PKC, PKD | O | Open npn emitter outputs that provide a fullwave rectified signal from the servo differentiator. These outputs are referenced to AGND. These outputs are high impedance when not enabled by $\overline{GTX}$ |
| **ANALOG PINS** | | |
| VRC | - | Reference voltage pin for SERVO and LEVEL. VRC is referenced to VCA. |
| VRG | - | Reference voltage pin for the programmable filter. VRG is referenced to ground. |
| VBP | - | The equalizer high frequency boost is set by an external voltage applied to this pin. VBP must be proportional to VRG. Programmable boost is implemented by using a DAC that uses VRG as its reference. A fixed amount of boost can be set by an external resistor divide network connected from VBP to VRG and GND. |
| RX | - | Pin to set filter reference current. External resistor Rx from this pin to ground sets the filter reference current IFO. |
| IFO | - | Reference current output pin. The reference current is normally supplied as the reference current to a current DAC which generates the programmable input current for the IFI pin. |
| IFI | - | Programmable filter input current pin. The filter cutoff frequency is proportional to the current into this pin. The current must be proportional to the reference current out of IFO. A fixed filter cutoff frequency is generated by connecting IFO to IFI and selecting Rx to set the desired frequency. |
| LZ/FD | - | Pin for external resistor to set timing for both Low-Z input and fast decay modes. |
| BYP | - | The AGC integrating capacitor $C_A$ is connected between BYP and VCA. |
| VCA, VCD | - | Analog and Digital +5 volts. |
| AGND, DGND | - | Analog and Digital grounds. |

## ELECTRICAL SPECIFICATIONS

Unless otherwise specified, 4.5V < VCC < 5.5V, 0°C<Ta<70°C

**ABSOLUTE MAXIMUM RATINGS** (Operation above maximum ratings may damage the device.)

| PARAMETER | VALUE |
|---|---|
| Storage Temperature | -65 to +150°C |
| Junction Operating Temperature,Tj | +130°C |
| Supply Voltage, VCA, VCD | -0.7 to 7V |
| Voltage Applied to Inputs | -0.7 to VCA + 0.7V, -0.7 to VCD + 0.7V |

**RECOMMENDED OPERATING CONDITIONS**

| PARAMETER | | RATING |
|---|---|---|
| Supply Voltage | VCA = VCD = VCC | 4.5V < VCC < 5.5V |
| Ambient Temperature, Ta | | 0°C<Ta<70°C |

**POWER SUPPLY**

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| PD | Power Dissipation | Outputs unloaded<br>4.5V < VCA, VCD < 5.5V | | 490 | 625 | mW |

**LOGIC SIGNALS**

| | | | | | | |
|---|---|---|---|---|---|---|
| VIL | TTL Input Low Voltage | | -0.3 | | 0.8 | V |
| VIH | TTL Input High Voltage | | 2.0 | | VCC +0.3 | V |
| IIL | TTL Input Low Current | VIL = 0.4V | -0.4 | | | mA |
| IIH | TTL Input High Current | VIH = 2.7V | | | 0.1 | mA |
| VOHE | ECL Output High Voltage | | VCC -1.02 | | VCC -0.4 | V |
| VES | ECL Differential Output Swing | | 0.3 | | 0.6 | V |
| TRF | EC1 Output Rise and Fall Time | CL ≤ 10 pF | | | 3.5 | ns |
| TS | Control Input Switching Times | | | | 0.1 | µs |
| VOLT | TTL Output Low Voltage | IOL = 4mA | 0.5 | | | V |
| VOHT | TTL Output High Voltage | IOH = -400 mA | | | 2.7 | V |

**AGC AMPLIFIER**

The input signals are AC coupled to VIA+ and VIA-. VOA+ and VOA- are AC coupled to IN+ and IN-. ON+ and ON- are AC coupled to DP and DN. Ca 1000 pF. Fin = 4 MHz. Unless otherwise specified, the output is measured differentially at VOA+ and VOA-.

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| VIB | Input Range | Filter boost at $fc$ = 0 dB | 24 | | 240 | mVppd |
| | | Filter boost at $fc$ = 11 dB | 20 | | 100 | mVppd |
| VD | DP-DN Voltage | VIA± = 0.1 Vppd | 0.90 | | 1.10 | Vppd |
| VDV | DP-DN Voltage Variation | 24 mV < VIAppd < 240 mV | | | 8.0 | % |
| AV | Gain Range | | 1.9 | | 22 | V/V |
| AVPV | Gain Sensitivity w.r.t. BYP Voltage | | | 28 | | dB/V |
| DR | VOA+ VOA- Dynamic Range | THD = 1% max | .75 | | | Vppd |
| RINDA | Differential Input Impedance | $\overline{WG}$ = 1 | 3.7 | | 7.4 | kΩ |
| | | $\overline{WG}$ =0 | | 300 | | Ω |
| RINSA | Single Ended Input Impedance | $\overline{WG}$ = 1 | | 3 | | kΩ |
| | | $\overline{WG}$ = 0 | | 150 | | Ω |
| VOS | Differential Output Offset Variation | from min. gain to max. gain | -200 | | +200 | mV |
| VIN | Input Referred Noise Voltage | gain = max, Rs = 0Ω filter not connected to VOA+ and VOA-, BW = 15 MHz | | | 20 | nV/√Hz |
| BW | Bandwidth | No AGC action, Gain = 22 | 55 | | | MHz |
| CMRR | Common Mode Rejection Ratio | gain = 22, Vin = 0 VDC + 100 mVpp @ 5 MHz | 40 | | | dB |
| PSRR | Power Supply Rejection Ratio | gain = 22, 100 mVpp @ 5 MHz on VCA, VCD | 45 | | | dB |
| TGD | Gain Decay Time | VIA± = 120 mV to 240 mV VOA± < 0.9 Final Value IFI = 600 µA | | 25 | | µs |
| TGA | Gain Attack Time | VIA± = 120 mV to 240 mV VOA± < 1.1 Final Value IFI = 600 µA | | 25 | | µs |

## ELECTRICAL SPECIFICATIONS (continued)

Unless otherwise specified, 4.5V<VCC<5.5V, 0°C<Ta<70°C

### AGC CONTROL

The input signals are AC coupled to DP and DN. Ca = 1000 pF, 110 µA<IFI<600 µA.

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| VDI | DP-DN Signal Input Range | | | | 1.5 | Vpp |
| ID | Discharge Current | $\overline{WG}$ = 1, DP - DN = 0V | | 0.008 x IFI | | A |
| IDF | Fast Discharge Current | | | 20 x Id | | A |
| ICH | Charge Pump Attack Current | $\overline{WG}$ = 1, DP - DN = 0.55V | | 40 x Id | | A |
| ICHF | Charge Pump Fast Attack Current, Ichf | $\overline{WG}$ = 1, DP - DN = 0.675V | | 7 x Ich | | A |
| IK | BYP Pin Leakage Current | $\overline{WG}$ or $\overline{HOLD}$ = 0, VBYP = VCC - 1.5V | -0.1 | | +0.1 | µA |
| VRC | VRC Reference Voltage | | | VCA -VRG | | V |
| IVRC | VRC Output Drive | | -0.75 | | +0.75 | mA |
| VRG | VRG Reference Voltage | Isource 0 mA to 1 mA | 2.2 | | 2.45 | V |
| TLZ | Low-Z and Fast Decay Timing Accuracy | T = RT/28 | -30 | | +30 | % |

### EQUALIZER/FILTER

The input signals are AC coupled to IN+ and IN-.

| | | | | | | |
|---|---|---|---|---|---|---|
| $fc$ | Filter Cutoff Frequency | RX = 5kΩ<br>$fc$ = 27 x IFI/(4 x IFO ) MHz<br>4 ≥ IFO/IFI ≥ 4/3 | 9 | | 27 | MHz |
| IFO | IFO Reference Current | IFO = 0.75/RX; Tj = 27°C<br>5kΩ > RX > 1.25 kΩ | 0.15 | | 0.6 | mA |
| IFI | IFI Program Current Range | Tj = 27°C, 27 MHz > $fc$ > 9 MHz | 0.2 | | 0.6 | mA |
| FCA | FCA Filter FC Accuracy | $fc$ = 27 MHz | -13 | | 13 | % |
| RX | RX Range | | 1.25 | | 5 | kΩ |
| AO | Normal Low Pass Gain<br>AO = (ON ±) / (IN±) | Fin = 0.67$fc$ | 1.4 | | 2.2 | V/V |
| AD | Differentiated Low Pass Gain<br>AD = (OD ±) / (IN±) | Fin = 0.67$fc$ | 0.8AO | | 1.2AO | V/V |
| FBA | Frequency Boost | VBP = VRG | -1.5 | | +1.5 | dB |
| | Accuracy | VBP/VRG = 0.5 | -1.0 | | +1.0 | dB |

**EQUALIZER/FILTER** (continued)

The input signals are AC coupled to IN+ and IN-.

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| TGD1 | Group Delay Variation | $fc$ = 27 MHz, VBP = 0 to VRG<br>$fc$ > Fin > 0.3 $fc$ | -0.5 | | +0.5 | ns |
| TGD2 | | $fc$ = 9 to 27 MHz, VBP = 0 to VRG<br>$fc$ > Fin > 0.3 $fc$ | -2.5 | | +2.5 | % |
| VOSVF | Output Offset Voltage Variation | 200 µA < IFI < 600 µA | | | 200 | mV |
| DRF | VOF Filter Output Dynamic Range | THD = 1.5% max<br>Fin = 0.67 $fc$ | 1.2 | | | Vpp |
| RINF | Filter Input Resistance | | 3.0 | | | kΩ |
| CINF | Filter Input Capacitance | | | | 7 | pF |
| ROF | Filter Output Resistance | IO+ = 1.0 mA | | | 60 | Ω |
| IOF | Filter Output Current | | -1.0 | | 1.0 | mA |
| VNN | Eout Output Noise Voltage; ON+, ON- | BW = 100 MHz, RS = 50Ω<br>VBP = 0, $fc$ = 27 MHz | | 2.7 | 3.5 | mVRms |
| | | BW = 100 MHz, RS = 50Ω<br>VBP = VRG, $fc$ = 27 MHz | | 5.7 | 8.0 | mVRms |
| VND | Eout Output Noise Voltage; OD+, OD- | BW = 100 MHz, RS = 50Ω<br>VBP = 0, $fc$ = 27 MHz | | 5.5 | 7.5 | mVRms |
| | | BW = 100 MHz, RS = 50Ω<br>VBP = VRG, $fc$ = 27 MHz | | 13.0 | 21.0 | mVRms |

**DATA COMPARATOR**

The input signals are AC coupled to DP and DN.

| | | | | | | |
|---|---|---|---|---|---|---|
| VID | DP-DN Signal Range | | | | 1.5 | Vpp |
| RIND | Differential Input Resistance | | 8 | | 14 | kΩ |
| CIND | Differential Input Capacitance | | | | 5 | pF |
| VOSD | Comparator Offset Voltage (Note 1) | | | | 4 | mV |
| HYS | Threshold Voltage Gain | 0.3 < VTH-VRC < 0.9 | 0.42 | | 0.49 | V/V |
| VSH | Threshold Voltage Hysteresis (Note 1) | | | .20 x GHYS x (VTH -VRC) | | V/V |
| TPDD | Propagation Delay | To DO, $\overline{DO}$ | | 6 | | ns |
| IVTH | VTH Input Bias Current | | | | 2 | µA |

Note 1: Not directly measureable

**CLOCKING**
The input signals are AC coupled to CP and CN.

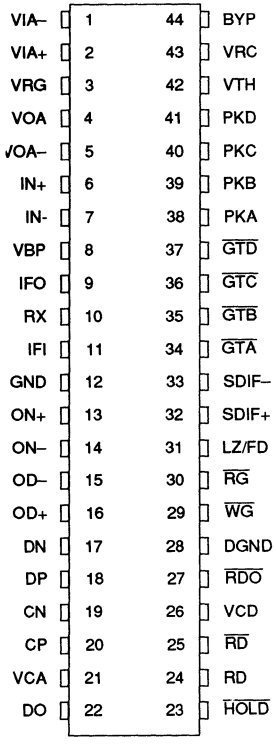
| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| VIC | CP-CN Signal Range | | | | 1.5 | Vppd |
| VOSC | Comparator Offset Voltage (Note 1) | | | | 4 | mV |
| RINC | Differential Input Resistance | | 8 | | 14 | kΩ |
| CINC | Differential Input Capacitance | | | | 5 | pF |
| TDS | D Flip-Flop Set Up Time | DP-DN threshold to CP-CN zero cross, CP-CN = 1Vppd at 18 MHz | | | 1 | ns |
| PP | Pulse Pairing | Vs = 1 Vpp, F = 18 MHz | | | 0.5 | ns |
| TPDC | Propagation Delay from CP-CN zero crossing to RD | Vs = 20 mVpp square wave | | 9 | | ns |
| PWRD | RD Output Pulse Width | | 8 | | 14 | ns |
| PWRT | $\overline{RDO}$, TTL Output Pulse Width | | 20 | | 40 | ns |

**SERVO DIFFERENTIATOR/FULL-WAVE RECTIFIER**
An external series network is connected between SDIF and $\overline{SDIF}$ to determine the servo differentiator transfer function. The input signals are AC coupled to DP and DN. Fin = 6.7 MHz at 1.0 Vppd.

| | | | | | | |
|---|---|---|---|---|---|---|
| ISDIF | SDIF+ to SDIF- pin current | Differentiator impedance must be set so as not to dip the signal for this level | 1.4 | 2.0 | 2.6 | mA |
| RDIF | Internal differentiator pull-up resistors | Cannot be directly tested | 0.4 | 0.6 | 0.8 | kΩ |
| FWR | Input voltage range to maintain FWR voltage gain | Cannot be directly tested | 0.1 | | 2.0 | Vppd |
| RERR | Rectification Error | | | | 5 | % |
| AFWR | FWR Voltage Gain from FWR Input to PKA-D Outputs (Note 1) | | TBD | 0.97 | TBD | Vpp/Vppd |
| ISL | Servo Output Leakage Current | Channel diabled | | | 10 | µA |
| VCOS | PKA-D Channel to Channel Offset | 1Vppd input to servo FWR | -5 | | 5 | mV |
| VAOS | PKA-D Absolute Offset | 1Vppd input to servo FWR | TBD | | TBD | mV |

Note 1: Not directly measureable

## PACKAGE PIN DESIGNATIONS
(Top View)




**44-Lead SOM**

### THERMAL CHARACTERISTICS: θja

| | |
|---|---|
| **44-Lead SOM** | **70°C/W** |

## ORDERING INFORMATION

| PART DESCRIPTION | ORDERING NUMBER | PACKAGE MARK |
|---|---|---|
| SSI 32P3013 | | |
| 44-Lead SOM | 32P3013-CM | 32P3013-CM |

**Preliminary Data:** Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.



Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 573-6000, FAX (714) 573-6914

**Notes:**

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# SSI 32P3015
## Pulse Detector with Programmable Filter
## Advance Information

2

January 1993

## DESCRIPTION

The SSI 32P3015 is a bipolar integrated circuit that provides all the data processing for pulse detection and four-burst servo capture from encoded read signals. This device can handle a NRZ data rate of 64 Mbit/s.

The SSI 32P3015 includes an AGC amplifier with AGC charge pump, a programmable 7-pole Bessel low pass filter, a pulse qualification circuit, and a 4-burst servo capture circuit. Automatic AGC control maintains a constant signal level into the pulse qualifier, and achieves fast write-to-read recovery. A time differentiator is included in the servo signal path, if so needed.

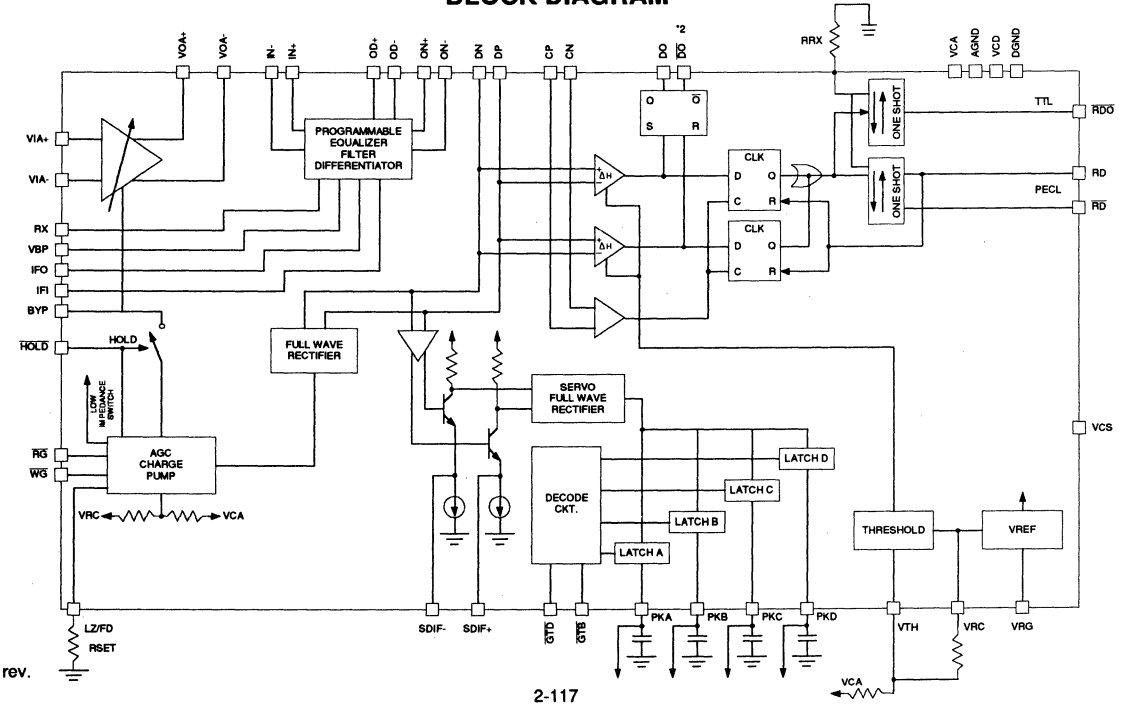
Ideal for constant density recording applications, the SSI 32P30105 low pass filter has a programmable 9-27 MHz bandwidth and 0-13 dB boost for pulse slimming. A time derivative of the read signal is also provided by the filter for time qualification in peak detection.

The SSI 32P3015 requires only a +5V power supply and is available in a 44-pin SOM package.

## FEATURES

- **Compatible with 64 Mbit/s data rate operation**
- **Fast attack/decay modes for rapid AGC recovery**
- **Automatic AGC actions: Low Drift AGC hold, fast AGC recovery, and low AGC input impedance control signals**
- **Includes programmable pulse slimming equalization and programmable channel filter and differentiator with no external filter components**
- **±0.5 ns filter group delay variation from 0.3FC to FC = 27 MHz**
- **Independent positive and negative threshold qualification to suppress error propagation**
- **0.5 ns max pulse pairing**
- **Servo differentiator and 4-burst servo capture**
- **+5V only operation**
- **44-pin SOM package**

## BLOCK DIAGRAM



## FUNCTIONAL DESCRIPTION

The SSI 32P3015 Pulse Detector/Filter with 4-Burst Servo Capture is designed to support a 64 Mbit/s NRZ data rate. The signal processing circuits include a wide band variable gain amplifier, a sophisticated dual-rate AGC charge pump, a programmable electronic filter, a pulse qualifier, a servo differentiator and a 4-burst servo capture circuit.

### Modes of Operation

The SSI 32P3015 can operate in one of three modes as controlled by $\overline{RG}$, $\overline{WG}$, and SG.

**Normal Read Mode** $\overline{RG}$ = 0, $\overline{WG}$ = 1, SG = X

In the normal Read Mode, the AGC actions are active. The AGC amplifier processes the input signal pulses; one-shot pulses are generated at the RD and $\overline{RD}$ outputs for each qualified signal peak. The $\overline{RDO}$ output buffer, which is a TTL buffer of the RD/$\overline{RD}$, is disabled and its output is pulled up high to reduce jitter and noise.

**Servo Read Mode** $\overline{RG}$ = 1, $\overline{WG}$ = 1, SG = 1

In the servo Read Mode, the AGC actions remain active (See note 1). The servo signal is amplified, fullwave rectified, differentiated and gated to the proper peak capture capacitor. The pulse qualifier remains active, and the $\overline{RDO}$ output is active to aid in servo decode.

**Write Mode** $\overline{RG}$ = X, $\overline{WG}$ = 0, SG =X

In the Write Mode, the AGC actions are suspended. The AGC amplifier input impedance is clamped low to facilitate fast recovery. The $\overline{RDO}$ output is disabled and pulled up high to reduce jitter and noise.

### AGC Amplifier

The wide band AGC amplifier amplifies the read signal from the read/write pre-amp to a signal level acceptable at the pulse qualifier. The AGC amplifier gain is an exponential function of the BYP voltage when referenced to VR.

$$Av = Ao \exp[\frac{(V_{BYP} - VR)}{K}] \quad \text{(See note 2)}$$

### AGC Actions

The AGC loop maintains a constant DP/DN signal level at a nominal level, ~1 Vppd. The AGC actions are current charging and discharging to/from the external BYP integrating capacitor, and are classified into the following modes:

Normal Read and Servo Read Mode
($\overline{RG}$ = X, $\overline{WG}$ = 1) SG = X

**Slow Decay:** When the DP/DN signal is below 1 Vppd, a slow decay current, Id, charges the BYP capacitor. The AGC amplifier gain is increased slowly. This slow decay current tracks with the bandwidth of the filter. Id = 0.008 x IFI. At T = 27°C, the maximum Id is 4.5 µA when the filter cutoff frequency is 27 MHz.

**Slow Attack:** When the DP/DN signal exceeds 1 Vppd, but is below 1.25 Vppd, a slow attack current, Ich, discharges the BYP capacitor. The AGC amplifier gain is decreased. The slow attack current is 20 times that of the slow decay current. Thus, for a given BYP capacitor, the slow attack response time is quicker than the slow decay response.

**Fast Attack:** When the DP/DN signal exceeds 1.25 Vppd, the device enters a fast attack mode. A fast attack current, Ichf, discharges the BYP capacitor. The AGC amplifier gain is quickly lowered. The fast attack current is seven times that of the slow attack current.

In servo Read Mode, constant AGC amplifier gain is generally desirable. Without an external AGC hold control, the servo data amplitude should be made lower than that of the data signal prior to the servo read mode. The SSI 32P3015 then enters the slow decay mode, which has a very slow effect on the AGC amplifier gain.

Write Mode ($\overline{RG}$ = X, $\overline{WG}$ = 0) SG = X

In the write mode, the AGC charge pump is disabled. This holds the AGC amplifier gain at its previous value.

Notes:

1. The servo signal should have a lower amplitude than the data signal prior to the servo read mode. Servo read should be completed before and significant change in AGC amplifier gain is resulted from the slow decay AGC mode.

2. In a closed loop, the sensitivity of Ao and K to typical process variations is irrelevant. The typical values of Ao and K are provided for reference only, and not tested in production. A0 = 11, K = 0.22, VR = 3.6.

**Write-to-Read Transition**
**($\overline{RG}$ = X, $\overline{WG}$ = 0-to-1) SG = X**

When the SSI 32P3015 switches from the write to read mode, i.e., $\overline{WG}$ 0-to-1 transition, the device remains in the low input impedance state for a preset time period. For the next time period, the device then enters either the fast decay or attack mode depending on the signal level at the DP/DN pins. The time period, t, is determined by an external resistor, RT, from the LZ/FD pin to ground.

$$\tau(\mu s) = \frac{RT(k\Omega)}{28}$$

For example, with RT = 38 kΩ, each time period is 1.36 µs.

**Programmable Filter**

The SSI 32P3015 includes a programmable low pass filter following the AGC amplifier for (1) 2X voltage gain from the AGC amplifier output to the pulse qualifier input, (2) noise limiting, (3) pulse slimming, and (4) provision of a time differentiated signal. The low pass filter is of a 7-pole 2-zero Bessel type. The filter's unboosted -3 dB bandwidth, defined as the cutoff frequency, is programmable from 9-27 MHz; the high frequency equalization is programmable from 0-13 dB at the cutoff frequency.

The filter input is ac-coupled from the AGC amplifier output. The filter's normal low pass output is ac-coupled to the data channel of the pulse qualifier. The differentiated low pass output is ac-coupled to the time channel of the pulse qualifier.

The normalized 7-pole 2-zero Bessel filter transfer function is given in Figure 1.

The cutoff frequency, fc, is programmable with 3 pins: RX, IFO and IFI. At the RX pin, an external resistor to ground establishes a reference current:

$$IFO = \frac{0.75}{Rx}, \text{at } T = 27°C$$

IFI should be made proportional to IFO for $fc$ temperature stability. The cutoff frequency is related to the RX resistor, IFO and IFI currents as the following:

$$fc(MHz) = 27 \cdot \frac{IFI}{IFO} \cdot \frac{1.25}{Rx(k\Omega)}$$

For a fixed cutoff frequency setting, IFO and IFI can be tied together. The cutoff frequency equation then reduces to:

$$fc(MHz) = 27 \cdot \frac{1.25}{Rx(k\Omega)}$$

For programmable cutoff frequency, an external current DAC can be used. IFO should be the reference current into the DAC. The DAC output current drives IFI, which is then proportional to the IFO. The DACF in the SSI 32D4661 Time Base Generator is designed to control $fc$ of the Silicon Systems programmable filters. When the DACF, which has a 4X current gain from its reference to fullscale output, is used, 5 kΩ RX is used. The fc is then given by:

$$fc(MHz) = 27 \cdot \frac{F\_Code}{127}$$

where F_Code is the decimal code equivalent to the 7-bit input into the DACF.

The high frequency equalization is programmable with two pins: VRG and VBP. The VRG is a bandgap reference voltage, 2.3V typically. The voltage at the VBP pin determines the amount of high frequency boost at the cutoff frequency. The boost function is as follows:

$$Boost(dB) = 20\log_{10}\left[\left(\frac{Kb \cdot VBP}{VRG}\right) + 1\right]$$

$$Kb = 3.041 + 0.0276 \cdot fci$$

where fci is the ideal cutoff frequency in MHz.

For a fixed boost setting, a resistor divider between VRG to ground can be used with the divided voltage at the VBP pin. For programmable equalization, an external voltage DAC can be used. VRG should be the reference voltage to the DAC. The DAC output voltage is then proportional to the VRG. The DAC in the SSI 32D4661 is designed to control the magnitude equalization of Silicon Systems programmable filters.

When DACs are used, the boost relation then reduces to:

$$Boost(dB) = 20\log_{10}\left[\left(Kb \cdot \frac{S\_Code}{127}\right) + 1\right]$$

**Pulse Qualification**

The SSI 32P3015 validates each DP/DN peak by a combination of level qualification and time qualification. In level qualification, a dual-comparator threshold detection eliminates errors due to low level additive noise. In time qualification, the filter's differentiated output is used to locate signal peaks.

**Level Qualification**

The dual-comparator architecture allows independent detection for positive and negative peaks. One comparator detects a positive peak by comparing the data signal with a positive threshold. The other comparator detects a negative peak by comparing the data signal with a negative threshold. Each comparator has a small hysteresis, 20% of the set threshold, to help qualify signals which just clear the set threshold.

The SSI 32P3015 comparator thresholds are set by a DC voltage at the VTH pin, such as from a resistor divider from VCA to VRC (see note 3). The threshold at each comparator can be computed as: Hysteresis Gain x (VTH - VRC). The thresholds at the two comparators are of the same magnitude, but of opposite polarity.

The SSI 32P3015 has three sets of pulse detector outputs: RD/$\overline{RD}$, $\overline{RDO}$, and DO. RD/$\overline{RD}$ output is the pseudo-ECL differential output. Corresponding to each validated peak of the DP/DN signal, a one-shot pulse occurs at the RD/$\overline{RD}$ output. The pulse width of the one-shot pulse is determined by an internal timing circuit, and specified in the electrical specification.

$\overline{RDO}$ is the TTL output of the pulse detector, logically equivalent to RD/$\overline{RD}$. Again, a one-shot pulse occurs at the $\overline{RDO}$ output for each validated peak of the DP/DN signal. The pulse width of this one-shot pulse is also specified in the electrical specification. DO output is a test point used to monitor the outputs of the internal comparators. It is an open-emitter output requiring a 5 kΩ external resistor pull-down to ground.

### Four-Burst Servo Differentiator and Capture

The SSI 32P3015 supports advanced embedded 4-burst servo technique. The signal at the DP/DN input can be time differentiated, fullwave rectified, and gated onto the selected peak capture output.

The transfer function from the DP/DN to the servo fullwave rectifier input is:

$$Av = \frac{2380Cs}{LCs^2 + (R + 48.1)Cs + 1}$$

where: R, L, and C are external passive components across SDIF±

$$15\ pF < C < 125\ pF$$

$$s = jw$$

When the time differentiation function is not desired, a 2 kΩ resistor should be used across the SDIF± pins.

The transfer function from the servo fullwave rectifier input to the peak capture output is set so that a 1 Vppd DP/DN signal produces 0.95 Vpeak output. With no signal input, the outputs are set close to ground, with little or no offset common to all four channels.

GTA, GTB, GTC, and GTD are now generated on-chip, using STROBE and SG as inputs. N.B.: There must be exactly 4 strobe pulses withing the TRUE time of SG.

A two-bit counter and 4 gates produce:

GTA from the first STROBE pulse,

GTB from the second STROBE pulse,

GTC from the third STROBE pulse,

GTD from the fourth STROBE pulse,.

Resetting of PKA, PKB, PKC, and PKD must still be done externally.

VCS Pin: This is a third +5V pin, intended not to be switched off by the customer in order to power down.

VCS is used as the high-voltage tie point for the ESD diodes from the 5 TTL-level input pins:

1) STROBE
2) SG
3) $\overline{RG}$
4) $\overline{WG}$
5) $\overline{HOLD}$

The purpose of this is to make it impossible for one or more of the TTL-level input drives to attempt to support the chip, via ESD diodes, when VCC and VCD are switched off.

VCS also supports the held servo voltages at pins PKA, PKB, PKC, and PKD. This is done by using VCN as the +5V supply for SSIN, PKCTRLN (via VPB), and LSERVO.

RRX Pin: This pin connects to an external precision, low T-C resistor, which is used to set the discharge currents of the one-shots, OSE_A and OSE_B, which in turn determine the pulse widths of the TTL ouput pulse, $\overline{RDT}$, and of the ECL ouput pulses, RD and $\overline{RD}$. This permits adjustment of the pulse widths for different applications and/or for variations in on-chip capacitances, and reduces the pulse-width changes caused by "corner" conditions.

Note 3: VCA is the +5V supply. VRC is the bandgap voltage referenced from VCA, i.e., VRC = VCA - VRG.

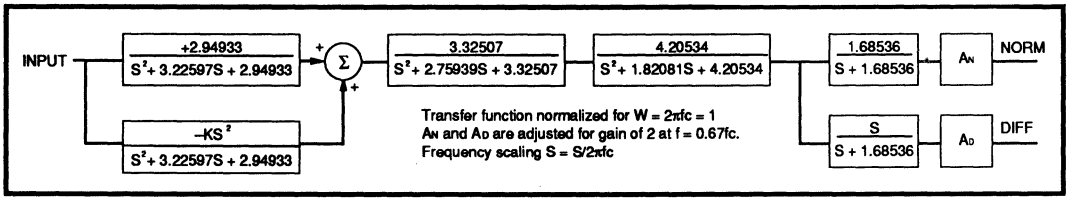



**FIGURE 1: Bessel Filter Transfer Function**

## PIN DESCRIPTION

### INPUT PINS

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| VIA+, VIA- | I | AGC Amplifier input pins. |
| IN+, IN- | I | Equalizer/filter input pins. |
| DP, DN | I | Data inputs to data comparators and fullwave rectifier. |
| CP, CN | I | Differentiated data inputs to the clock comparator. |
| VTH | I | Threshold level setting input for the data comparators. |
| STROBE | I | TTL input. Enables servo gate according to Figure 3. |
| $\overline{RG}$ | I | TTL compatible input. When low, the device is in normal Read Mode. |
| $\overline{WG}$ | I | TTL compatible input. When low, the device is in Write Mode. When both $\overline{RG}$ and $\overline{WG}$ are low, the device is in Servo Mode. |
| SG | I | TTL compatible input. When high the corresponding servo gate channel is enabled. |
| $\overline{HOLD}$ | I | TTL compatible input. When low the AGC action is suspended. |

### OUTPUT PINS

| | | |
|---|---|---|
| VOA+, VOA- | O | AGC amplifier output pins. |
| ON+, ON- | O | Equalizer/filter normal output pins. |
| OD+, OD- | O | Equalizer/filter differentiated output pins. |
| DO | O | ECL compatible data comparator latch output pin. |
| RD, $\overline{RD}$ | O | ECL compatible read data output pins. |
| $\overline{RDO}$ | O | TTL compatible read data output. |
| SDIF+, SDIF- | – | Pins for external differentiating network for servo data. |
| PKA, PKB<br>PKC, PKD | O | Open npn emitter outputs that provide a fullwave rectified signal from the servo differentiator. These outputs are referenced to AGND. These outputs are high impedance when not enabled by STROBE and SG. |

## PIN DESCRIPTION (continued)

### ANALOG PINS

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| RRX | – | Pin to set, via external R, output pulse widths. |
| VRC | – | Reference voltage pin for SERVO and LEVEL. VRC is referenced to VCA. |
| VRG | – | Reference voltage pin for the programmable filter. VRG is referenced to ground. |
| VBP | – | The equalizer high frequency boost is set by an external voltage applied to this pin. VBP must be proportional to VRG. Programmable boost is implemented by using a DAC that uses VRG as its reference. A fixed amount of boost can be set by an external resistor divide network connected from VBP to VRG and GND. |
| RX | – | Pin to set filter reference current. External resistor Rx from this pin to ground sets the filter reference current IFO. |
| IFO | – | Reference current output pin. The reference current is normally supplied as the reference current to a current DAC which generates the programmable input current for the IFI pin. |
| IFI | – | Programmable filter input current pin. The filter cutoff frequency is proportional to the current into this pin. The current must be proportional to the reference current out of IFO. A fixed filter cutoff frequency is generated by connecting IFO to IFI and selecting Rx to set the desired frequency. |
| LZ/FD | – | Pin for external resistor to set timing for both Low-Z input and fast decay modes. |
| BYP | – | The AGC integrating capacitor $C_A$ is connected between BYP and VCA. |
| VCA, VCD, VCS | – | Analog, Digital, and Servo +5V |
| AGND, DGND | – | Analog and Digital grounds. |

## ELECTRICAL SPECIFICATIONS

Unless otherwise specified, 4.5V<VCC<5.5V, 0°C<Ta<70°C

**ABSOLUTE MAXIMUM RATINGS** (Operation above maximum ratings may damage the device.)

| PARAMETER | RATING |
|---|---|
| Storage Temperature | -65 to +150°C |
| Junction Operating Temperature,Tj | +130°C |
| Supply Voltage, VCA, VCD | -0.7 to 7V |
| Voltage Applied to Inputs | -0.7 to VCA, VCD V and VCS |

**RECOMMENDED OPERATING CONDITIONS**

| | |
|---|---|
| Supply Voltage, VCS = VCA = VCD = VCC | 4.5V < VCC < 5.5V |
| Ambient Temperature, Ta | 0°C<Ta<70°C |

**POWER SUPPLY**

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| PD | Power Dissipation | Outputs unloaded<br>4.5V < VCA, VCD < 5.5V | | 490 | 540 | mW |

**LOGIC SIGNALS**

| | | | | | | |
|---|---|---|---|---|---|---|
| VIL | TTL Input Low Voltage | | -0.3 | | 0.8 | V |
| VIH | TTL Input High Voltage | | 2.0 | | VCC +0.3 | V |
| IIL | TTL Input Low Current | VIL = 0.4V | -0.4 | | | mA |
| IIH | TTL Input High Current | VIH = 2.7V | | | 0.1 | mA |
| VOL | ECL Output High Voltage | VCC = 5V | VCC -1.02 | | | V |
| VOE | ECL Differential Output Swing | VCC = 5V | 0.3 | | | V |
| TRF | EC Output Rise and Fall Time | CL ≤ 10 pF | | | 3.5 | ns |
| TS | Control Input Switching Times | | | | 0.1 | µs |
| VOLT | TTL Output Low Voltage | IOL = 4mA | 0.5 | | | V |
| VOHT | TTL Output High Voltage | IOH = -400 mA | | | 2.7 | V |

## ELECTRICAL SPECIFICATIONS (continued)

Unless otherwise specified, 4.5V<VCC<5.5V, 0°C<Ta<70°C

### AGC AMPLIFIER

The input signals are AC coupled to VIA+ and VIA-. VOA+ and VOA- are AC coupled to IN+ and IN-. ON+ and ON- are AC coupled to DP and DN. Ca 1000 pF. Fin = 4 MHz. Unless otherwise specified, the output is measured differentially at VOA+ and VOA-.

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| VIB | Input Range | Filter boost at $fc$ = 0 dB | 24 | | 240 | mVppd |
| | | Filter boost at $fc$ = 11 dB | 20 | | 100 | mVppd |
| VD | DP-DN Voltage | VIA± = 0.1 Vppd | 0.90 | | 1.10 | Vppd |
| VDV | DP-DN Voltage Variation | 24 mV < VIA± < 240 mV | | | 8.0 | % |
| AV | Gain Range | | 1.9 | | 22 | V/V |
| AVPV | Gain Sensitivity w.r.t. BYP Voltage | | | 28 | | dB/V |
| DR | VOA+ VOA- Dynamic Range | THD = 1% max | .75 | | | Vppd |
| RINDA | Differential Input Impedance | $\overline{WG}$ = 1 | 4.7 | | 8.4 | kΩ |
| | | $\overline{WG}$ = 0 | | 1 | | |
| RINSA | Single Ended Input Impedance | $\overline{WG}$ = 1 | | 3 | | kΩ |
| | | $\overline{WG}$ = 0 | | 0.5 | | kΩ |
| VOS | Differential Output Offset Variation | from min. gain to max. gain | -200 | | +200 | mV |
| VIN | Input Referred Noise Voltage | gain = max, Rs = 0Ω filter not connected to VOA+ and VOA-, BW = 15 MHz | | | 15 | nV/√Hz |
| BW | Bandwidth | No AGC action, Gain = 22 | 55 | | | MHz |
| CMRR | Common Mode Rejection Ratio | gain = 22, Vin = 0 VDC + 100 mVpp @ 5 MHz | 40 | | | dB |
| PSRR | Power Supply Rejection Ratio | gain = 22, 100 mVpp on VCA, VCD @ 5 MHz | 45 | | | dB |
| TGD | Gain Decay Time | VIA± = 240 mV to 120 mV VOA± < 0.9 Final Value IFI = 600 µA | | TBD | | µs |
| TGA | Gain Attack Time | VIA± = 120 mV to 240 mV VOA± < 1.1 Final Value IFI = 600 µA | | TBD | | µs |

**AGC CONTROL**

The input signals are AC coupled to DP and DN. Ca = 1000 pF, 110 µA<IFI<600 µA.

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| VDI | DP-DN Signal Input Range | | | | 1.5 | Vpp |
| ID | Discharge Current | $\overline{WG}$ = 1, DP - DN = 0V | | 0.008 x IFI | | A |
| IDF | Fast Discharge Current | | | 20 x Id | | A |
| ICH | Charge Pump Attack Current | $\overline{WG}$ = 1, DP - DN = 0.55V | | 40 x Id | | A |
| ICHF | Charge Pump Fast Attack Current, Ichf | $\overline{WG}$ = 1, DP - DN = 0.675V | | 7 x Ich | | A |
| IK | BYP Pin Leakage Current | $\overline{WG}$ or $\overline{HOLD}$ = 0 | -0.1 | | +0.1 | µA |
| VRC | VRC Reference Voltage | | | VCA -VRG | | V |
| IVRC | VRC Output Drive | | -0.75 | | +0.75 | mA |
| VRG | VRG Reference Voltage | Isource 0 to 1 mA | 2.2 | | 2.45 | V |
| TLZ | Low-Z and Fast Decay Timing Accuracy | T = RT/28 | -30 | | +30 | % |

**EQUALIZER/FILTER**

The input signals are AC coupled to IN+ and IN-.

| | | | | | | |
|---|---|---|---|---|---|---|
| *fc* | Filter Cutoff Frequency | RX = 5kΩ<br>*fc* = 27 x IFI/(4 x IFO ) MHz<br>4 ≥ IFO/IFI ≥ 4/3 | 9 | | 27 | MHz |
| IFO | IFO Reference Current | IFO = 0.75/RX; Tj = 27°C<br>5kΩ > RX > 1.25 kΩ | 0.15 | | 0.6 | mA |
| IFI | IFI Program Current Range | Tj = 27°C, 27 MHz > *fc* > 9 MHz | 0.2 | | 0.6 | mA |
| FCA | FCA Filter FC Accuracy | *fc* = 27 MHz | -13 | | 13 | % |
| RX | RX Range | | 1.25 | | 5 | kΩ |
| AO | Normal Low Pass Gain<br>AO = (ON ±) / (IN±) | Fin = 0.67*fc* | 1.4 | | 2.2 | V/V |
| AD | Differentiated Low Pass Gain<br>AD = (OD ±) / (IN±) | Fin = 0.67*fc* | 0.8AO | | 1.2AO | V/V |
| FBA | Frequency Boost Accuracy | VBP = VRG | -1.5 | | +1.5 | dB |
| | | VBP/VRG = 0.5 | -1.0 | | +1.0 | dB |

## ELECTRICAL SPECIFICATIONS (continued)

Unless otherwise specified, 4.5V<VCC<5.5V, 0°C<Ta<70°C

### EQUALIZER/FILTER (continued)

The input signals are AC coupled to IN+ and IN-.

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| TGD1 | Group Delay Variation | $fc$ = 27 MHz, FB = 0 to 9 dB<br>$fc$ > Fin > 0.3 $fc$ | -0.5 | | +0.5 | ns |
| TGD2 | | $fc$ = 9 to 27 MHz<br>$fc$ > Fin > 0.3 $fc$ | -2.5 | | +2.5 | % |
| VOSVF | Output Offset Voltage Variation | 200 µA,IFI<600 µA | -200 | | 200 | mV |
| DRF | VOF Filter Output Dynamic Range | THD = 1.5% max<br>Fin = 0.67 $fc$ | 1.2 | | | Vpp |
| RINF | Filter Input Resistance | | 3.0 | | | kΩ |
| CINF | Filter Input Capacitance | | | | 7 | pF |
| ROF | Filter Output Resistance | IO+ = 1.0 mA | | | 60 | Ω |
| IOF | Filter Output Current | | -1.0 | | 1.0 | mA |
| VNN | Eout Output Noise Voltage; ON+, ON- | BW = 100 MHz, RS = 50Ω<br>VBP = 0, $fc$ = 27 MHz | | 2.7 | | mVRms |
| | | BW = 100 MHz, RS = 50Ω<br>VBP = VRG, $fc$ = 27 MHz | | 5.7 | | mVRms |
| VND | Eout Output Noise Voltage; OD+, OD- | BW = 100 MHz, RS = 50Ω<br>VBP = 0, $fc$ = 27 MHz | | 5.5 | | mVRms |
| | | BW = 100 MHz, RS = 50Ω<br>VBP = VRG, $fc$ = 27 MHz | | 13.0 | | mVRms |

### DATA COMPARATOR

The input signals are AC coupled to DP and DN.

| | | | | | | |
|---|---|---|---|---|---|---|
| VID | DP-DN Signal Range | | | | 1.5 | Vpp |
| RIND | Differential Input Resistance | | 8 | | 14 | kΩ |
| CIND | Differential Input Capacitance | | | | 5 | pF |
| VOSD* | Comparator Offset Voltage | | | | 4 | mV |
| HYS | Threshold Voltage Gain | 0.3 < VTH-VRC < 0.9 | 0.42 | | 0.49 | V/V |
| VSH* | Threshold Voltage Hysteresis | | | .20 x GHYS x (VTH -VRC) | | V/V |
| TPDD | Propagation Delay | To DO, $\overline{DO}$ | | 6 | | ns |
| IVTH | VTH Input Bias Current | | | | 2 | µA |

* Not externally measurable

**CLOCKING**

The input signals are AC coupled to CP and CN.

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| VIC | CP-CN Signal Range | | | | 1.5 | Vppd |
| VOSC | Comparator Offset Voltage | | | | 4 | mV |
| RINC | Differential Input Resistance | | 8 | | 14 | kΩ |
| CINC | Differential Input Capacitance | | | | 5 | pF |
| TDS | D Flip-Flop Set Up Time | DP-DN threshold to CP-CN zero cross, CP-CN = 1Vppd at 18 MHz | | | 1 | ns |
| PP | Pulse Pairing | CP-CN = 20 mVppd square wave | | | 0.5 | ns |
| TPDC | Propagation Delay from CP-CN zero crossing to RD | | | 9 | | ns |
| PWRD | RD Output Pulse Width | RRX = 7.87 kΩ CL = 10 pF | 6 | | 10.5 | ns |
| PWRT | $\overline{\text{RDO}}$, TTL Output Pulse Width | RRX = 7.87 kΩ CL = 10 pF | 15 | | 30 | ns |

**SERVO DIFFERENTIATOR/FULL-WAVE RECTIFIER**

An external series network is connected between SDIF and SDIF to determine the servo differentiator transfer function. The input signals are AC coupled to DP and DN. Fin = 6.7 MHz at 1.0 Vppd.

| | | | | | | |
|---|---|---|---|---|---|---|
| ISDIF | SDIF+ to SDIF- pin current | Differentiator impedance must be set so as not to dip the signal for this level | 1.4 | 2.0 | 2.6 | mA |
| RDIF | Internal differentiator pull-up resistors | Cannot be directly tested | 0.4 | 0.6 | 0.8 | kΩ |
| FWR | Input voltage range to maintain FWR voltage gain | Cannot be directly tested | 0.1 | | 2.0 | Vppd |
| RERR | Rectification Error | | | | 5 | % |
| AFWR | FWR Voltage Gain from FWR Input to PKA-D Outputs | | TBD | 0.97 | TBD | Vpp/ Vppd |
| ISL | Servo Output Leakage Current | Channel disabled | | | 10 | µA |
| VCOS | PKA-D Channel to Channel Offset | 1Vppd input to servo FWR | TBD | | TBD | mV |
| VAOS | PKA-D Absolute Offset | 1Vppd input to servo FWR | TBD | | TBD | mV |

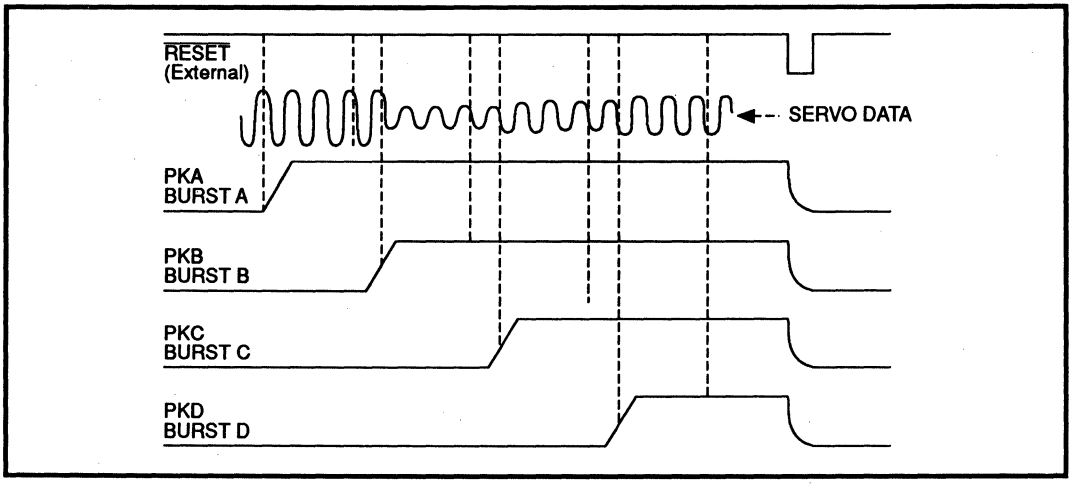



**FIGURE 2: Servo Gate Timing**

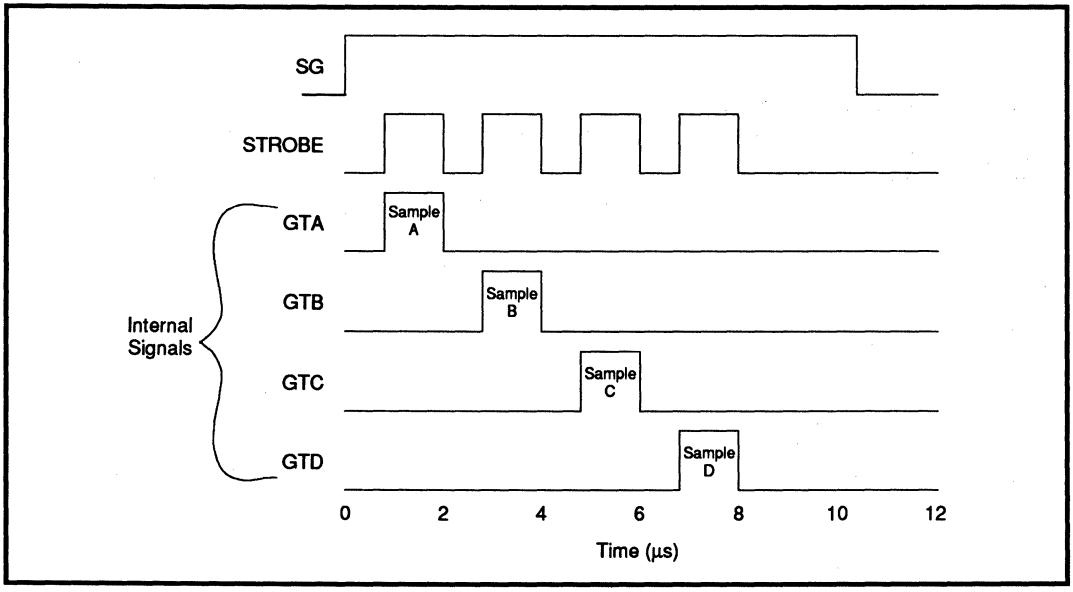
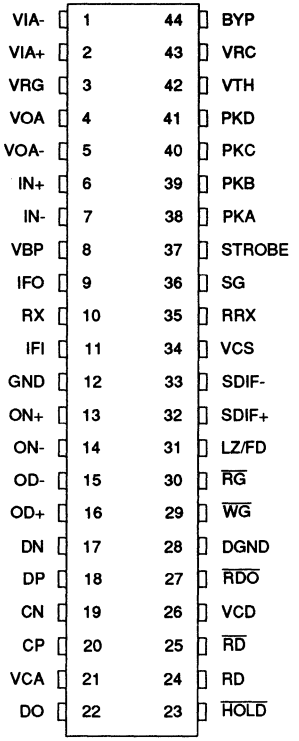



**FIGURE 3: Servo Capture Timing Diagram**

## PACKAGE PIN DESIGNATIONS
(Top View)

**THERMAL CHARACTERISTICS: θja**

| | |
|---|---|
| **44-Lead SOM** | **70°C/W** |




**44-Lead SOM**

**Advance Information:** Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.



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**Notes:**

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A TDK Group Company

# SSI 32P3030
## Pulse Detector and Servo Demodulator

2

December 1992

## DESCRIPTION

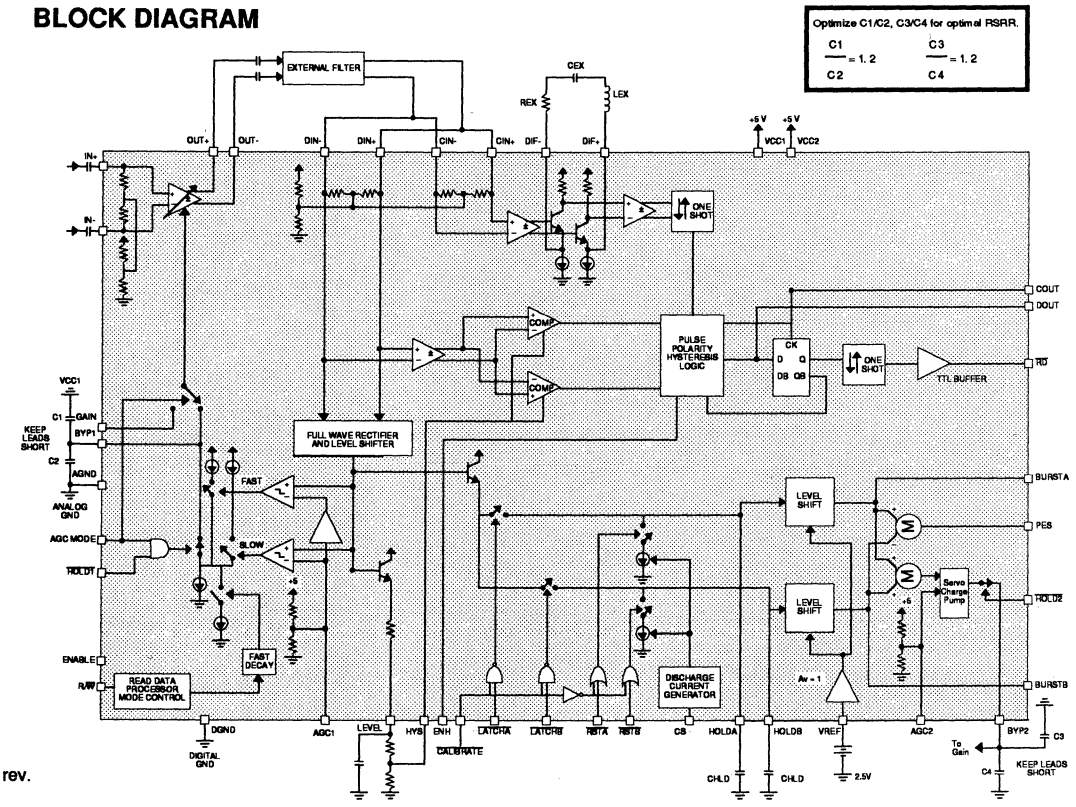
The SSI 32P3030 is a low power pulse detector and servo demodulator designed for use in low power applications requiring +5V only power supplies. This device has a fully integrated bipolar circuit that detects and validates amplitude peaks in the output from a disk drive read amplifier, as well as detecting embedded servo information to provide position error signals used for read head positioning.

Time and amplitude qualification are used to provide a TTL compatible output that accurately duplicates the time position of input signal peaks. An AGC control loop, using a dual rate charge pump, provides a constant input amplitude for the level qualifier. Level qualification with or without hysteresis can be implemented as a fixed threshold or a constant percentage that tracks signal amplitude that enhances qualification during AGC loop transients. (Continued)

## FEATURES

- **+5V only power supplies**
- **Wide bandwidth AGC input amplifier**
- **Fast and slow AGC attack and decay regions for fast transient recovery**
- **Embedded servo channel provides servo burst capture and difference circuits**
- **Local sampled servo AGC provided based on servo burst output amplitude sum**
- **Write to Read transient suppression**
- **Dual mode pulse qualification with/without pulse polarity hysteresis for read/servo data retrieval.**
- **24 Mbit/s operation**

## BLOCK DIAGRAM



## DESCRIPTION (Continued)

The Servo Demodulator consists of two peak detector channels that capture rectified servo data peaks. Buffered individual channel outputs are provided along with a difference output. Servo channel gain can be controlled by a sampled AGC signal based on maintaining the amplitude of the sum of both channels.

## CIRCUIT OPERATION

**READ MODE** (R/$\overline{W}$ pin high or open)

In Read Mode the SSI 32P3030 is used to process either data or servo signals. In the Data Read Mode the input signal is amplified and qualified using an AGC amplifier and pulse level qualification of the detected signal peaks. In the Servo Read Mode the input signal is amplified and rectified and an error signal based on amplitude comparison is made available. Two servo burst channels are available that provide A & B burst levels.

**DATA READ MODE** (AGCMODE pin high or open)

An amplified head output signal is AC coupled to the IN+ and IN- pins of the AGC amplifier. Gain control is accomplished by full wave rectifying and amplifying the [(DIN+) - (DIN-)] voltage level and comparing it to a reference voltage level at the AGC1 pin.

The SSI 32P3030 contains a dual rate attack charge pump. The value of the attack current is dependent on the instantaneous level at DIN±. For signal levels above 125% of the desired level a fast attack mode is invoked that supplies a 1.4 mA charge current to the network on the BYP1 pin. Between 125% and 100% of the desired level the circuit enters a slow attack mode and supplies 0.18 mA of charge current to the BYP1 pin. This allows the AGC to rapidly recover during a write to read transition but reduces distortion once the AGC amplifier is within range.

Two decay modes are available and are automatically controlled within the device.

Upon a switch to write mode (R/$\overline{W}$ pin low), the device will hold the gain at its previous value, and the AGC input stage is switched into a low impedance state. When the device is then switched back to read mode the AGC holds the gain and stays in the low impedance state for 0.9 µs. It then switches into a fast/slow attack mode if the new gain required is less than the previously held gain or a fast decay mode if the gain required is more than its previous value. The fast decay current is 0.12 mA and stays on 0.9 µs. After the 0.9 µs time period the device stays in a steady state slow attack, slow decay mode. The slow decay discharge current is 4.5 µA.

The AGC1 pin is internally biased so that the target differential voltage input at DIN± is 1.0 Vpp at nominal conditions. The voltage on this pin can be modified by tying a resistor between AGC and AGND or VCC1. A resistor to AGND decreases the voltage level, while a resistor to VCC1 increases it. The resulting AGC voltage level is shown in Figure 1;

Where:

V = Voltage at AGC1 with pin open (2.3V, nom.)

Rint = AGC1 pin input impedance (6.5 kΩ, typ.)

Rx = External resistor.

The new DIN± input target level is nominally
$(V_{AGC1} - 0.75) \cdot 0.64$ Vpp

The maximum AGC amplifier output swing is 2.6 Vpp at OUT± which allows for up to 6 dB loss in any external filter between OUT± and DIN±.

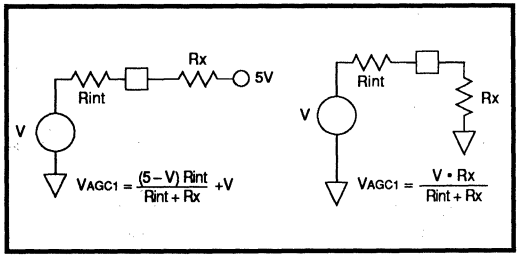



**FIGURE 1: AGC Voltage**

AGC gain is a linear function of the BYP1/Gain-pin voltage (VBYP1) as shown in Figure 2.

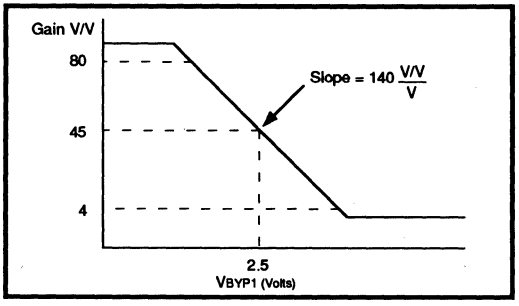



**FIGURE 2: AGC Gain**

The AGC amplifier has emitter follower outputs and can sink 4.0 mA.

One filter for both amplitude (DIN± input) and time (CIN± input) channels, or a separate filter for each may be used. If two filters are used, attention must be paid to time delays so that each channel is timed properly. A multi-pole Bessel filter is typically used for its linear phase or constant group delay characteristics.

In the amplitude channel the signal is sent to a hysteresis comparator. The hysteresis threshold level is set so that it will be tripped only by valid signal pulses and not by baseband noise. It can be a fixed level or a fraction of the DIN± voltage level.

The latter approach is accomplished by using an external filter/network between the LEVEL and HYS pins. This allows setting the AGC slow attack and decay times slow enough to minimize time channel distortion and setting a shorter time constant for the hysteresis level. The LEVEL pin output is a rectified and amplified version of DIN±, 1.0 Vpp at DIN± results in 1.0 Vop nominally, at the LEVEL pin. A voltage divider is used from LEVEL to ground to set the Hysteresis threshold at a percentage of the peak DIN± voltage. For example, if DIN± is 1.0 Vpp, then using an equal valued resistor divider will result in 0.5 Vop at the HYS pin. This will result in a nominal ±0.18V threshold or a 36% threshold of a ±0.5V DIN± input. The capacitor, from the LEVEL pin to GND, is chosen to set an appropriate time constant. This "feed forward" technique speeds up transient recovery by allowing qualification of the input pulses while the AGC is still settling. This helps in the two critical areas of write to read and head change recovery. Some care in the selection of the hysteresis level time constant must be exercised so as to not miss pattern (resolution) induced lower amplitude signals. Note that there is a built in 50mV threshold (ie., 10% of ± 0.5V DIN± input) for level qualification even when the HYS pin is grounded. This is to prevent false triggering by baseband noise during a DC erase gap, (e.g., address mark). The output of the hysteresis comparator is the "D" input of a D-type flip-flop. The DOUT pin is a comparator output signal for testing purposes only. When testing, it requires an external 3-6 kΩ pull-down resistor to ground. If no testing is necessary, the DOUT pin can be pulled up to Vcc (+5V) to save power.

In the time channel the signal is differentiated to transform signal peaks to zero crossings which are detected and used to trigger a bi-directional one-shot. The one-shot output pulses are used as the clock input of the D flip-flop. The COUT pin provides the one-shot output for test purposes. It also requires an external 3-6 kΩ pull down resistor for testing.

The differentiator function is accomplished by an external network between the DIF+ and DIF- pins. The transfer function from CIN± to the comparator input (not DIF±) is:

$$Av = \frac{-2000Cs}{LCs^2 + C(R+92)s + 1}$$

Where: C, L, R are external passive components

$20\ pF < C < 150\ pF$

$s = j\omega = j2\pi f$

During normal operation, the time channel clocks the D flip-flop on every positive and negative peak of the CIN± input. Two qualification modes exist to determine peaks. The first mode, qualification with pulse polarity hysteresis, (ENH = High), is exactly the same as the qualification on the SSI 32P541. In this mode, the D input to the flip-flop only changes state when the DIN± input exceeds the hysteresis comparator threshold opposite in polarity to the previous threshold exceeding peak. In the second mode, qualification without pulse polarity hysteresis, (ENH = Low), the polarity of the peaks is ignored. In this mode, the D input to the flip-flop changes state whenever the DIN± input exceeds the threshold regardless of polarity. This is accomplished, (see figure 3), by clocking the toggle flip-flop whenever the threshold is exceeded in either direction at the same time that the comparator detects a zero

crossing. It may be advantageous to use this mode of pulse qualification for retrieving certain kinds of servo patterns.

The time channel, then, determines signal peak timing and the amplitude channel determines validity by blocking signal peaks that do not exceed the hysteresis comparator threshold. The delays in each of these channels to the D flip-flop inputs are well matched. The D flip-flop output triggers a one-shot that sets the $\overline{RD}$ output pulse width.

### SERVO READ MODE

A position error signal (PES) is generated based on the relative amplitude of two servo signals, A and B. Rectified servo signal peaks are captured on hold capacitors at the HOLDA/B pins. This is accomplished by pulling $\overline{LATCHA}$ or $\overline{LATCHB}$ low for a sample period. Additionally, a default hold capacitor discharge current of 1.5 mA can be turned on by pulling $\overline{RSTA}$ or $\overline{RSTB}$ low. This default 1.5 mA discharge current can be modified by tying a resistor between CS and GND or VCC1. A resistor to GND increases the discharge current, while a resistor to VCC1 decreases it. The equation for increasing the discharge current is:

$$Ics = 22.5V \bullet \left(\frac{15k + Rcs}{15k \bullet Rcs}\right), \quad Rcs \geq 15\ k\Omega$$

For decreasing the discharge current, the equation is:

$$Ics = 22.5V \bullet \left(\frac{Rcs - 22.5k}{15k \bullet Rcs}\right), \quad Rcs \geq 22.5\ k\Omega$$

Outputs BURSTA/B & PES are referenced to an external reference applied to the VREF pin.

In servo read mode (see Figure 4) the BYP2 pin is connected to the GAIN pin and the servo channel gain is determined by the read channel gain as controlled by the sum of the A and B amplitudes. In this case a current is sourced/sinked to/from the capacitor on the GAIN/BYP2 pin whenever the $\overline{HOLD2}$ pin is pulled high. The current magnitude and direction is determined by:

$Ic = K_4[(K_5 \bullet V_{AGC2}) - Va(DIN)pp - Vb(DIN)pp]$

Where:

$V_{AGC2}$ = AGC2 pin voltage = 2.3V with pin open.

$K_4$ = 640 µA/Vpp

$K_5$ = 0.50 V/V

Va/b(DIN)pp = peak to peak A or B servo pattern signal voltages at DIN±

### WRITE MODE

In Write Mode the SSI 32P3030 Pulse Detector section is disabled and preset for the following Read Mode. The digital circuitry is disabled, the input AGC amplifier gain is held at its previous value and the AGC amplifier input impedance is reduced to about 250Ω.

Holding the AGC amplifier gain and reducing input impedance shortens system Write to Read recovery times.

The lowered input impedance improves settling time by reducing the time constant of the network between the SSI 32P3030 and a head preamplifier such as the SSI 32R4610AR. Write to read timing is controlled to maintain the reduced impedance for 0.9 µs before the AGC circuitry is activated. Coupling capacitors should be chosen with as low a value as possible consistent with adequate bandwidth to allow more rapid settling.

## MODE CONTROL

The device circuit mode is controlled by the ENABLE, R/$\overline{W}$, AGCMODE, $\overline{HOLD1}$ and $\overline{HOLD2}$ pins a shown in Table 1.

### DATA READ MODE

AGC active and controlled by data, Digital section active.

### DATA READ MODE, HOLD

AGC gain held constant, Digital section active. Gain will drift higher or lower at a rate determined by $C_{BYP1}$ and Hold mode leakage current.

### SERVO READ MODE I (See Figures 4 & 5)

The BYP2 and GAIN pins are tied together. Read amplifier AGC control voltage developed from sum of Servo signal levels. $\overline{HOLD2}$ is toggled to update the control voltage after each Servo frame.

### CALIBRATE MODE

A low level on $\overline{CALIBRATE}$ shall force $\overline{LATCHA}$ and $\overline{LATCHB}$ low and $\overline{RSTA}$ and $\overline{RSTB}$ high to measure the offset of the entire servo BURSTA, BURSTB, and PES channel.

### WRITE

Read amplifier input impedance reduced. AGC gain held constant, $\overline{RD}$ stays high.

### POWER DOWN

Circuit switched to a low current disabled mode.

Note: When AGCMODE is switched to a low state the voltage at the BYP1 pin will be held constant subject to Hold mode leakage current induced drift. So, when returning to Data Read Mode, the channel gain will be the same as it was prior to AGCMODE switching or slightly higher/lower.

**TABLE 1: SSI 32P3030 Circuit Mode Control**

| ENABLE | R/$\overline{W}$ | AGC MODE | $\overline{HOLD1}$ | $\overline{HOLD2}$ | READ PATH MODES |
|---|---|---|---|---|---|
| 1 | 1 | 1 | 1 | X | Data Read Mode |
| 1 | 1 | 1 | 0 | X | Data Read Mode Hold |
| 1 | 1 | 0 | X | 1 | Servo Read Mode - Sample |
| 1 | 1 | 0 | X | 0 | Servo Read Mode - Hold |
| 1 | 0 | X | X | X | Write |
| 0 | X | X | X | X | Power Down |

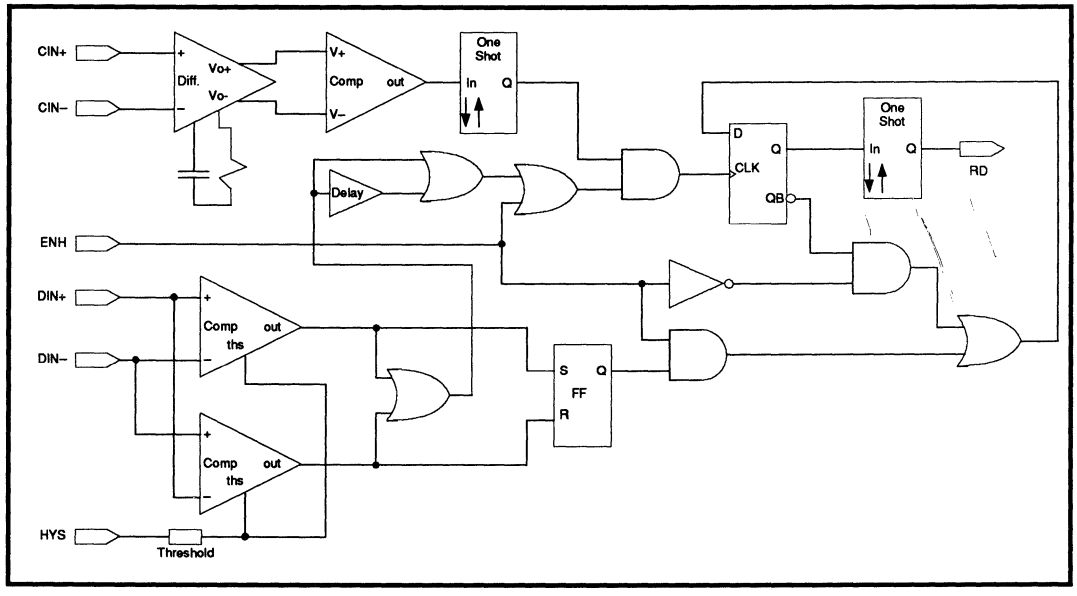



**FIGURE 3: ENH Provides Two Pulse Qualification Modes.**

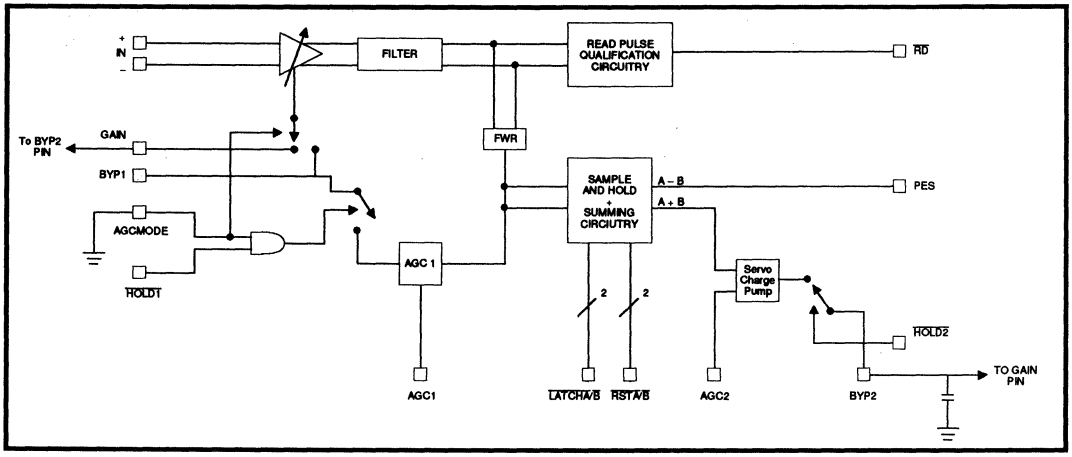



**FIGURE 4: Servo Read Mode**

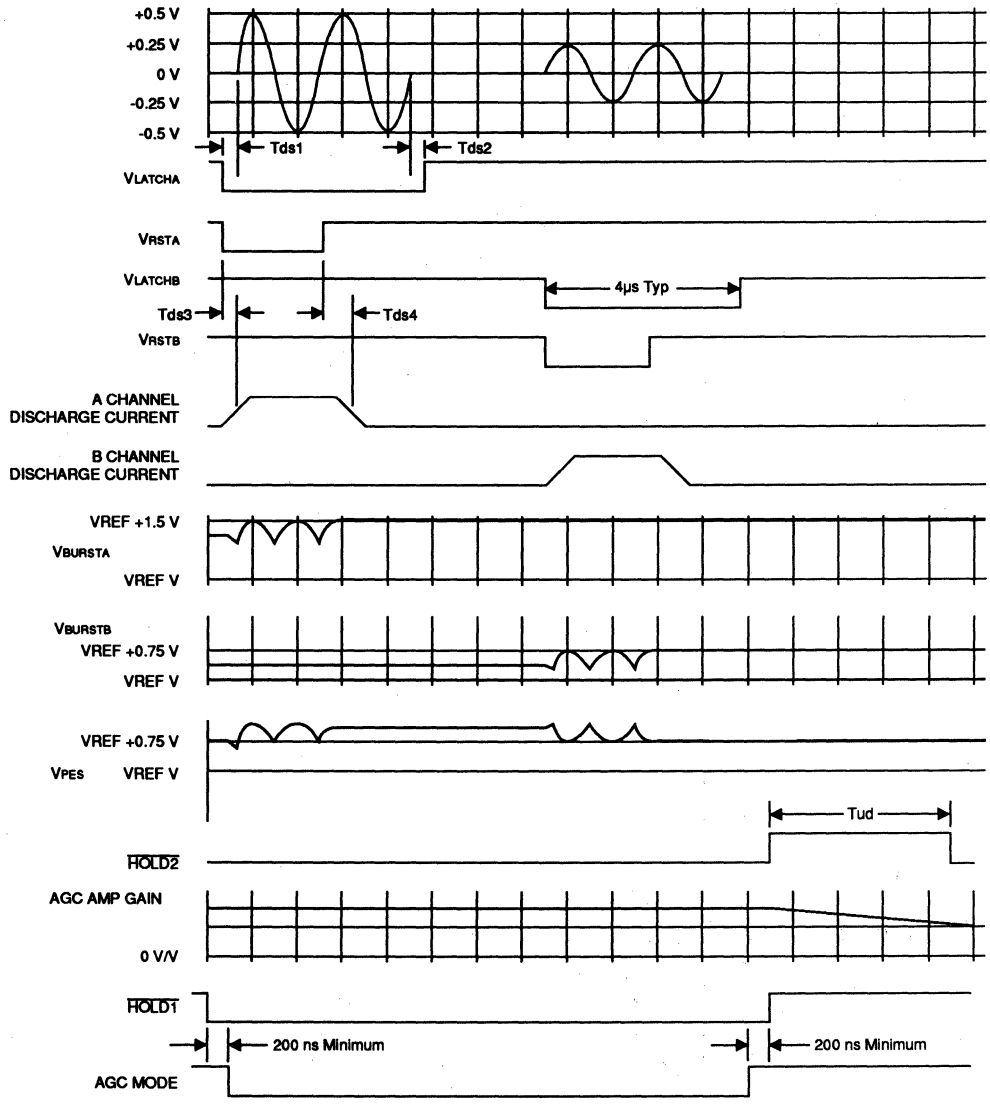



**FIGURE 5: Servo Read Mode 1**

## PIN DESCRIPTION

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| VCC1 | I | Analog (+5V) power supply for pulse detector. |
| AGND | I | Analog ground pin for pulse detector block. |
| VCC2 | I | Digital (+5V) supply pin for data synchronizer block. |
| DGND | I | Digital ground pin. |
| IN+, IN– | I | Analog signal input pins. |
| OUT+, OUT– | O | Read path AGC Amplifier output pins. |
| DIN+, DIN– | I | Analog input to the amplitude channel. |
| CIN+, CIN– | I | Analog input to the time channel. |
| DIF+, DIF– | I/O | Pins for external differentiating network. |
| COUT | O | Test point for monitoring the flip-flop clock input, pull-down resistor required. |
| DOUT | O | Test point for monitoring the flip-flop D-input, pull-down resistor required. |
| BYP1, BYP2 | I/O | An AGC timing capacitor or network is tied between each pin and GND. BYP1 is for read data. BYP2 is for servo data. |
| AGC1, AGC2 | I | Reference input voltage for the read data AGC loop. (AGC1) and sampled servo AGC loop (AGC2). |
| LEVEL | O | Output from fullwave rectifier that may be used for input to the hysteresis comparator. |
| HYS | I | Hysteresis level setting input to the hysteresis comparator. |
| $\overline{\text{HOLD1}}$, $\overline{\text{HOLD2}}$ | I | TTL compatible pin that holds the AGC gain when pulled low. |
| $\overline{\text{LATCHA}}$, $\overline{\text{LATCHB}}$ | I | TTL compatible inputs that switch channel A or B into peak acquisition mode when low. |
| $\overline{\text{RSTA}}$, $\overline{\text{RSTB}}$ | I | TTL compatible input that enables the discharge of channels A & B hold capacitors when held low. |
| CS | I | Hold capacitor discharge current magnitude is controlled by a resistor from this pin to GND or VCC1. If left open the default current is 1.5 mA. |
| HOLDA, HOLDB | I/O | Peak holding capacitors are tied from each of these pins to AGND. |
| VREF | O | Reference voltage for Servo outputs. |
| BURSTA, BURSTB | O | Buffered hold capacitor voltage outputs. |
| PES | O | Position error signal, A minus B output. |
| R/$\overline{\text{W}}$ | I | TTL compatible Read/Write control pin. A low input selects write mode. |
| Enable | I | TTL compatible power up control. A low input selects a low power state. |
| AGCMODE | I | TTL compatible pin that selects the AGC loop control input. A high selects BYP1, a low selects GAIN. |
| Gain | I | A voltage at the pin may be used to control AGC gain. |
| $\overline{\text{RD}}$ | O | TTL compatible read output, a falling edge corresponds to a detected peak. |
| $\overline{\text{CALIBRATE}}$ | I | Used to measure servo offset. |
| ENH | I | TTL compatible pulse qualification control pin. A low input selects modes which ignore polarity of peaks. |

## ELECTRICAL SPECIFICATIONS

Recommended conditions apply unless otherwise specified.

### ABSOLUTE MAXIMUM RATINGS

Operation outside these rating limits may cause permanent damage to this device.

| PARAMETER | RATING | UNIT |
|---|---|---|
| 5V Supply Voltage, VCC1, VCC2 | 6.5 | V |
| Pin Voltage (Analog pins) | .3 to VCC1 + .3 | V |
| Pin Voltage (Digital pins) | .3 to VCC2 + .3 or +12 mA | V |
| Storage Temperature | -65 to 150 | °C |
| Lead Temperature (Soldering 10 sec.) | 260 | °C |

### RECOMMENDED OPERATING CONDITIONS

Currents flowing into the chip are positive.

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Supply Voltage (VCC1, VCC2) | | 4.5 | 5.0 | 5.5 | V |
| Tj Junction Temperature | | - | | 135 | °C |
| Ambient Temperature | ENABLE = High or Low | 0 | | 80 | °C |

### POWER SUPPLY

| | | | | | |
|---|---|---|---|---|---|
| IVCC1,2 Supply Current | Outputs unloaded; ENABLE = high or open | | 76 | 110 | mA |
| Pd Power dissipation | Ta = 25°C, outputs unloaded | | 380 | 570 | mW |
| | ENABLE = Low | | 140 | 210 | mW |

### LOGIC SIGNALS

| | | | | | | |
|---|---|---|---|---|---|---|
| VIL | Input Low Voltage | | -0.3 | | 0.8 | V |
| VIH | Input High Voltage | | 2.0 | | VCC+0.3 | V |
| IIL | Input Low Current | VIL = 0.4V | 0.0 | | -0.4 | mA |
| IIH | Input High Current | VIH = 2.4V | | | 100 | µA |
| VOL | Output Low Voltage | IOL = 4.0 mA | | | 0.5 | V |
| VOH | Output High Voltage | IOH = -400 µA | 2.4 | | | V |

**MODE CONTROL**

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Enable to/from Disable Transition Time | Settling time of external capacitors not included, ENABLE pin high to/from low | | | 20 | µs |
| Read to Write Transition Time | R/$\overline{W}$ pin high to low | | | 1.0 | µs |
| Write to Read Transition Time | R/W pin low to high AGC setting not included | 0.4 | 0.9 | 1.6 | µs |
| AGC on to/from AGC off transition time | AGC mode pin high to/from low | | | 2.0 | µs |
| $\overline{HOLD1}$ ON to/from $\overline{HOLD1}$ OFF transition time | $\overline{HOLD1}$ pin high to/from low | | | 1.0 | µs |
| $\overline{HOLD2}$ ON to/from $\overline{HOLD2}$ OFF | $\overline{HOLD2}$ pin high to/from low | | | 1.0 | µs |

**READ MODE** (R/$\overline{W}$ is High)

**AGC AMPLIFIER**

Unless otherwise specified, recommended operating conditions apply. Input signals are AC coupled to IN±. OUT± are loaded differentially with 800Ω, and each side is loaded with < 10 pF to AGND, and AC coupled to DIN±. A 900 pF capacitor is connected between BYP1/BYP2 and AGND. An 1100 pF capacitor is connected between BYP1/BYP2 and VCC1. AGC1/AGC2 pin is open.

| PARAMETER | CONDITION | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Minimum Gain Range | 1.0 Vp-p ≤ (OUT+) - (OUT-) ≤ 2.6 Vp-p | 4 | | 80 | V/V |
| AGC Input Range | | 25 | | 250 | mVpp |
| Output Offset Voltage Variation | Over entire gain range | -500 | | +500 | mV |
| Maximum Output Voltage Swing | Set by BYP1 pin | 2.6 | | | Vpp |
| Differential Input Resistance | (IN+) - (IN-) = 100 mVp-p @ 2.5 MHz | 4 | 5.4 | 7.5 | kΩ |
| Differential Input Capacitance | (IN+) - (IN-) = 100 mVp-p @ 2.5 MHz | | 4 | 10 | pF |
| Single-Ended Input Impedance | R/$\overline{W}$ = high, IN+ or IN- | 2 | 2.7 | 3.8 | kΩ |
| | R/$\overline{W}$ = low, IN+ or IN- | | 160 | 250 | Ω |
| Input Noise Voltage | Gain set to maximum, RS = 0, BW = 15 MHz | | 5 | 15 | nV/$\sqrt{Hz}$ |
| Bandwidth | -3 dB bandwidth at maximum gain | 30 | | | MHz |
| OUT+ & OUT- Pin Current | No DC path to AGND | ±2.5 | ±4.0 | | mA |
| CMRR (Input Referred) | (IN+) = (IN-) = 100 mVp-p @ 5 MHz, gain set to max | 40 | | | dB |

**AGC AMPLIFIER (continued)**

| PARAMETER | CONDITION | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| PSRR (Input Referred) | VCC1, 2 = 100 mVp-p @ 5 MHz, gain set to max | 30 | | | dB |
| (DIN+) - (DIN-) Input Swing vs. AGC1 Input (DIN+) - (DIN-) = ($V_{AGC1}$-K1) • K2 K2 | 25 mVp-p ≤ (IN+) - (IN-) ≤ 250 mVp-p, $\overline{HOLD}$ = high, 0.5 Vp-p ≤ (DIN+) - (DIN-) ≤ 1.5 Vp-p | .54 | .64 | .74 | Vp-p/V |
| K1 | | 0.5 | 0.75 | 1.0 | V |
| (DIN+) - (DIN-) Input Voltage Swing Variation | 25 mVp-p ≤ (IN+) - (IN-) ≤ 250 mVp-p | | | 5.0 | % |
| AGC1 Voltage | AGC1 open | 1.8 | 2.2 | 2.7 | V |
| AGC1 Pin Input Impedance | | 4.8 | 6.5 | 9.5 | kΩ |
| Slow AGC Discharge Current | (DIN+) - (DIN-) = 0V | 2.8 | 4.5 | 6.5 | µA |
| Fast AGC Discharge Current | Starts at 0.9 µs after R/$\overline{W}$ goes high, stops at 1.8 µs | 0.07 | 0.12 | 0.18 | mA |
| BYP1 Leakage Current | $\overline{HOLD1}$ = low, 10 ≤ Gain ≤ 80 | -0.2 | | +0.2 | µA |
| Gain Pin Leakage Current | $\overline{HOLD2}$ = low, 10 ≤ Gain ≤ 80 | -0.2 | | +0.2 | µA |
| Slow AGC Charge Current | (DIN+) - (DIN-) = .563 VDC, $V_{AGC1}$ = 2.3 V | -0.11 | -0.18 | -0.27 | mA |
| Fast AGC Charge Current | (DIN+) - (DIN-) = 0.8 VDC, $V_{AGC1}$ = 2.3 V | -0.9 | -1.4 | -2.1 | mA |
| Fast to Slow Attack Switchover Point | $\frac{[(DIN+)-(DIN-)]}{[(DIN+)-(DIN-)]FINAL}$ | 110 | | 140 | % |
| Gain Decay Time (Td) | (IN+) - (IN-) = 250 mVp-p to 125 mVp-p @ 2.5 MHz, (OUT+) - (OUT-) to 90% final value | 12 | 20 | 36 | µs |
| | (IN+) - (IN-) = 50 mVp-p to 25 mVp-p at 2.5 MHz (OUT+) - (OUT-) to 90% final value | 38 | 60 | 110 | µs |
| Gain Attack Time | R/$\overline{W}$ low to high (IN+) - (IN-) = 250 mVp-p @ 2.5 MHz, (OUT+) - (OUT-) to 110% final value | .8 | 2 | 3.6 | µs |

**HYSTERESIS COMPARATOR**

Unless otherwise specified, recommended operating conditions apply. Input (DIN+) - (DIN-) is an AC coupled, 1.0 Vp-p, 2.5 MHz sine wave. 0.5 VDC is applied to the HYS pin. R/$\overline{W}$ pin is high.

| PARAMETER | CONDITION | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Input Signal Range | | | | 1.5 | Vp-p |
| Differential Input Resistance | (DIN+) - (DIN-) = 100 mVp-p @ 2.5 MHz | 8 | 10 | 14 | kΩ |
| Differential Input Capacitance | (DIN+) - (DIN-) = 100 mVp-p @ 2.5 MHz | | 3.0 | 5.0 | pF |
| Single-Ended Input Impedance | DIN+ or DIN- | 4 | 5 | 7 | kΩ |
| Slope of Level Gain | Calculated from 0.6 < DIN± < 1.5 Vppd | .85 | 1 | 1.2 | V/Vp-p |
| Intercept of Level Gain | DIN± = 0 Vppd | 0 | 0.13 | 0.26 | V |
| Level Gain | | Slope + (Intercept / DIN ppd) | | | |
| Level Pin Output Impedance | $I_{LEVEL}$ = 0.2 mA | 100 | 200 | 300 | Ω |
| Level pin Maximum Output Current | | 1.5 | | | mA |
| Slope of Hysteresis Gain | Calculated from 0.3V < HYS < 1.0V | 0.32 | 0.36 | 0.44 | V/V |
| Intercept of Hysteresis Gain | HYS = 0 | -0.04 | -0.025 | 0 | V |
| Hysteresis Gain | | Slope + (Intercept / HYS Voltage) | | | |
| HYS Pin Current | 0.3V < HYS < 1.0V | 0.0 | | -5 | µA |
| Tracking Hysteresis Threshold Tolerance | | -15 | | +15 | % |
| DOUT Pin Output Low Voltage | 5 kΩ from DOUT to GND | VCC -2.5 | VCC -2.0 | VCC -1.35 | V |
| DOUT Pin Output High Voltage | 5 kΩ from DOUT to GND | VCC -2.0 | VCC -1.6 | VCC -1.1 | V |

**ACTIVE DIFFERENTIATOR**

Unless otherwise specified, recommended operating conditions apply. Input (CIN+) - (CIN-) is an AC-coupled, 1.0 Vp-p, 2.5 MHz sine wave. 100Ω in series with 65 pF are tied from DIF+ to DIF-.

| | | | | | |
|---|---|---|---|---|---|
| Input Signal Range | | | | 1.5 | Vp-p |
| Differential Input Resistance | (CIN+) - (CIN-) = 100 mVp-p @ 2.5 MHz | 8 | 10 | 14 | kΩ |
| Differential Input Capacitance | (CIN+) - (CIN-) = 100 mVp-p @ 2.5 MHz | | 3.0 | 5.0 | pF |
| Single-Ended Input Impedance | CIN+ or CIN- | 4 | 5 | 7 | kΩ |
| Voltage Gain From CIN± to DIF± | (DIF+ to DIF-) = 2 kΩ | | 1 | | V/V |
| DIF+ to DIF- Pin Current | Differentiator impedance must be set so as to not clip the signal for this current level | ±0.7 | | | mA |

**ACTIVE DIFFERENTIATOR** (Continued)
Unless otherwise specified, recommended operating conditions apply. Input (CIN+) - (CIN-) is an AC-coupled, 1.0 Vp-p, 2.5 MHz sine wave. 100Ω in series with 65 pF are tied from DIF+ to DIF-.

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| COUT Pin Output Low Voltage | 5 kΩ from COUT to GND | VCC -2.5 | VCC -2.0 | VCC -1.35 | V |
| COUT Pin Output High Voltage | 5 kΩ from COUT to GND | VCC -2.0 | VCC -1.6 | VCC -1.1 | V |
| COUT Pin Output Pulse Width | | 22 | 35 | 52 | ns |

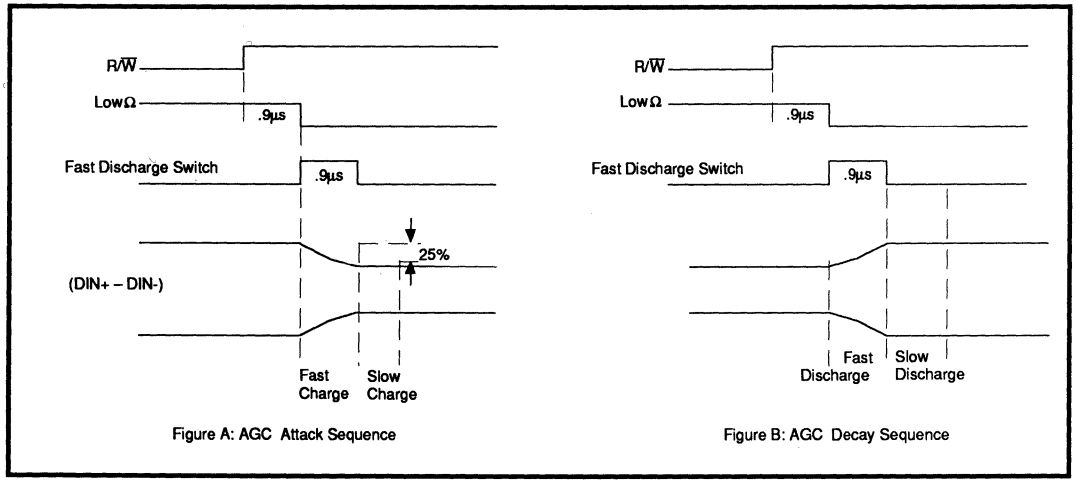



Figure A: AGC Attack Sequence

Figure B: AGC Decay Sequence

**FIGURE 6: AGC Timing Diagram**

**OUTPUT DATA CHARACTERISTICS** (See Figure 7)
Unless otherwise specified, recommended operating conditions apply. Inputs (CIN+) - (CIN-) and (DIN+) - (DIN-) are in-place as an AC coupled, 1.0 Vp-p, 2.5 MHz sine wave. 100Ω in series with 65 pF are tied from DIF+ to DIF-. 0.5V is applied to the HYS pin. $\overline{RD}$ is loaded with a 4 kΩ resistor to VCC and a 10 pF capacitor to DGND. ENABLE and R/$\overline{W}$ pins are high.

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| Td1 | D Flip-Flop Set Up Time | Minimum allowable time delay from (DIN+) - (DIN-) exceeding hysteresis point to (DIF+) - (DIF-) hitting a peak value. | 0 | | | ns |
| Td3 | Propagation Delay | | | 15 | 40 | ns |
| \|Td3-Td4\| | Pulse Pairing | 2.5 MHz sine wave input | | | 1.5 | ns |
| \|Td3-Td4\| | Pulse Pairing | 4 MHz sine wave input | | | 1.0 | ns |
| Td5 | Output Pulse Width | | 22 | 35 | 52 | ns |

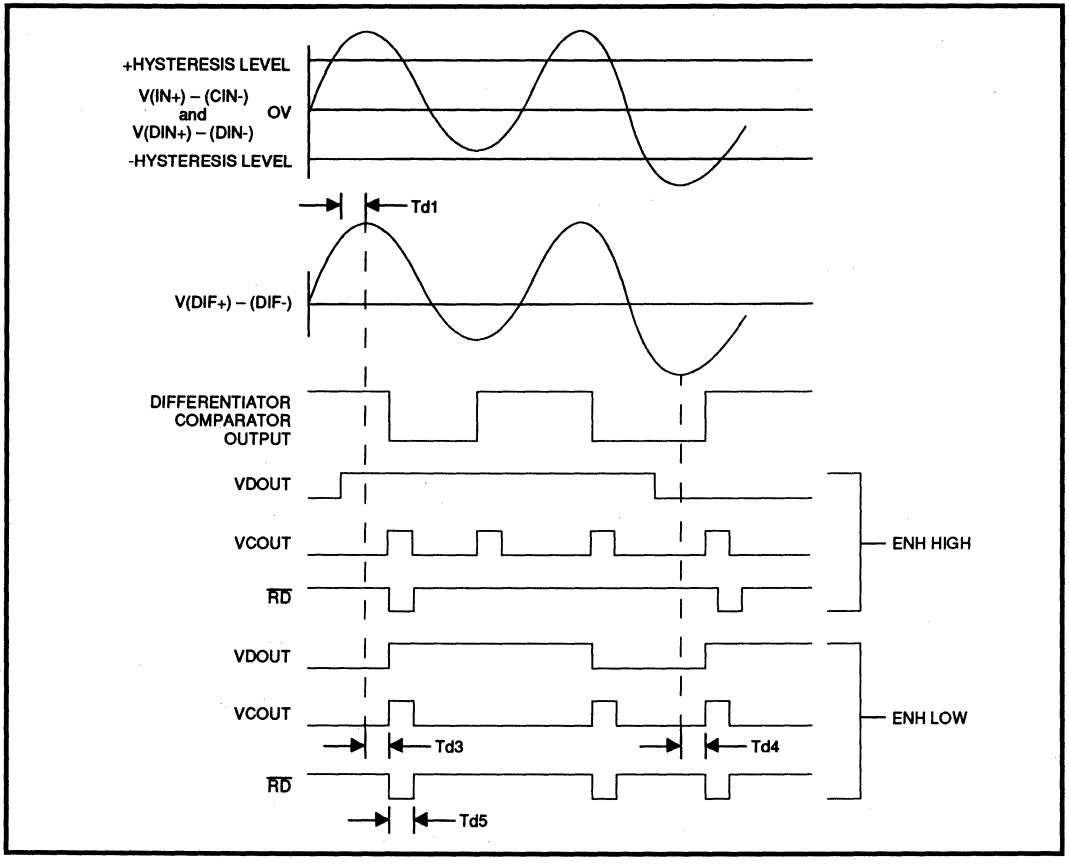



**FIGURE 7: Read Mode Digital Section Timing Diagram**

**SERVO SECTION** (Unless otherwise specified, recommended operating conditions apply.), LATCH A/B = Low, RST A/B = High, CS Pin Open

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| VREF Voltage Range | | 2.25 | 2.5 | 2.75 | V |
| VREF Pin Input Impedance | | 30 | | | kΩ |
| AGC2 Pin Voltage | AGC2 Pin Open, | 1.8 | 2.3 | 2.7 | V |
| AGC2 Pin Input Impedance | | 4.8 | 6.5 | 9.5 | kΩ |
| BURSTA/B pin Output Voltage vs (DIN+) – (DIN-) | $\overline{LATCHA/B}$ = Low<br>$\frac{V_{BURSTA/B} - VREF}{(DIN+) - (DIN-)} = 1.5\,V/Vp\text{-}p$ | -20 | | +10 | % |

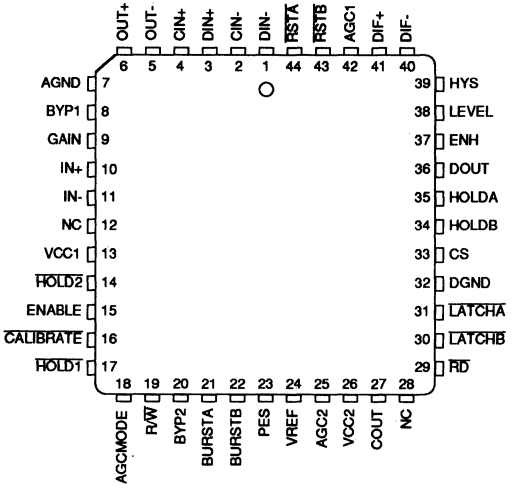
**SERVO SECTION** (Continued)

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| BURSTA/B Output<br><br>Offset Voltage<br>$V_{BURST}$ - VREF | I(HOLDA) = I(HOLDB) =-20 µA,<br>$\overline{LATCHA}$, $\overline{B}$ = Low<br>CS pin open<br>(DIN+) = (DIN-) | -150 | | +150 | mV |
| BURSTA - BURSTB Output Offset Match | $\overline{LATCHA/B}$ = low<br>(DIN+) = (DIN-) | -15 | | +15 | mV |
| Maximum PES Pin Output Voltage | Controlled by AGC2 | | | VCC1-1.5 | Vpp |
| PES Pin Output Offset Voltage | $V_{PES}$ - VREF, (DIN+) = (DIN-)<br>$\overline{LATCHA/B}$ = Low | -15 | | +15 | mV |
| Output Resistance, BURSTA/B & PES pins | $I_{LOAD}$ ± 500 µA | | | 50 | Ω |
| Hold A/B Charge Current | $\overline{LATCHA/B}$ = Low | 8 | | | mA |
| HOLDA/B Discharge Current Tolerance | $\overline{RSTA/B}$ = Low,<br>CS pin open | 0.8 | 1.5 | 2.2 | mA |
| | $\overline{RSTA/B}$ = High,<br>$\overline{LATCHA/B}$ = High | -0.2 | | +0.2 | µA |
| Load Resistance BURSTA/B, PES pins | Resistors to GND | 10.0 | | | kΩ |
| Load Capacitance BURSTA/B, PES pins | | | | 20 | pF |
| $\overline{LATCHA/B}$ pin set up time | (Tds1 in Figure 5) | 150 | | | ns |
| $\overline{LATCHA/B}$ pin Hold Time | (Tds2 in Figure 5) | 150 | | | ns |
| Channel A/B Discharge Current Turn On time | (Tds3 in Figure 5) | | | 150 | ns |
| Channel A/B discharge Current Turn Off time | (Tds4 in Figure 5) | | | 150 | ns |
| BYP2 Pin Leakage Current | $\overline{HOLD2}$ = Low | -0.2 | | +0.2 | µA |
| BYP2 Pin Charge/Discharge Current<br>$I_C = K_4[(K_5 \cdot V_{AGC2}) - V_{A(DIN)pp} - V_{B(DIN)pp}]$ | $K_4$, $\overline{HOLD2}$ = High | 400 | 640 | 880 | µA/Vpp |
| | $K_5$, $\overline{HOLD2}$ = High | 0.4 | 0.5 | 0.7 | V/V |
| Maximum BYP2 pin charge/discharge current | | 190 | 300 | 450 | µA |
| $V_{PES}$ pp vs. $V_{AGC2}$ | $V_{PES}$ pp/$V_{AGC2}$ | 1.18 | 1.33 | 1.5 | Vpp/V |
| | $V_{PES}$ pp Swing<br>AGC2 = Open | 2.4 | 3 | 3.6 | Vpp |

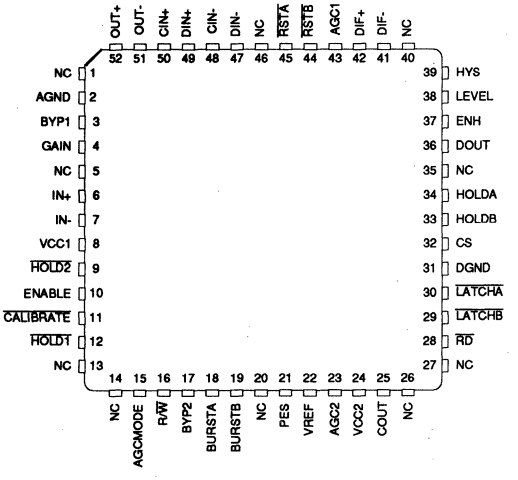
# SSI 32P3030
# Pulse Detector
# and Servo Demodulator

## PACKAGE PIN DESIGNATION
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.




**44-Pin PLCC**




**52-Pin QFP**

**THERMAL CHARACTERISTICS: θja**

| | |
|---|---|
| 44-Pin PLCC | 60° C/W |
| 52-Pin QFP | 75° C/W |

## ORDERING INFORMATION

| PART DESCRIPTION | ORDER NO. | PKG. MARK |
|---|---|---|
| SSI 32P3030 44-Pin PLCC | 32P3030-CH | 32P3030-CH |
| SSI 32P3030 52-Pin QFP | 32P3030-CG | 32P3030-CG |



Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714)573-6000, FAX (714) 573-6914

# SSI 32P3040
## Pulse Detector with Programmable Filter



December 1992

## DESCRIPTION

The SSI 32P3040 is a bipolar integrated circuit that provides all data processing necessary for detection and qualification of encoded read signals. The circuit will handle a data rate of 32 Mbit/s.

In read mode the SSI 32P3040 provides amplification and qualification of head preamplifier outputs. Pulse qualification is accomplished using level qualification of differentiated input zero crossings. An AGC amplifier is used to compensate for variations in head preamp output levels, presenting a constant input level to the pulse qualification circuitry. The AGC loop can be disabled so that a constant gain can be used for embedded servo decoding or other processing needs.

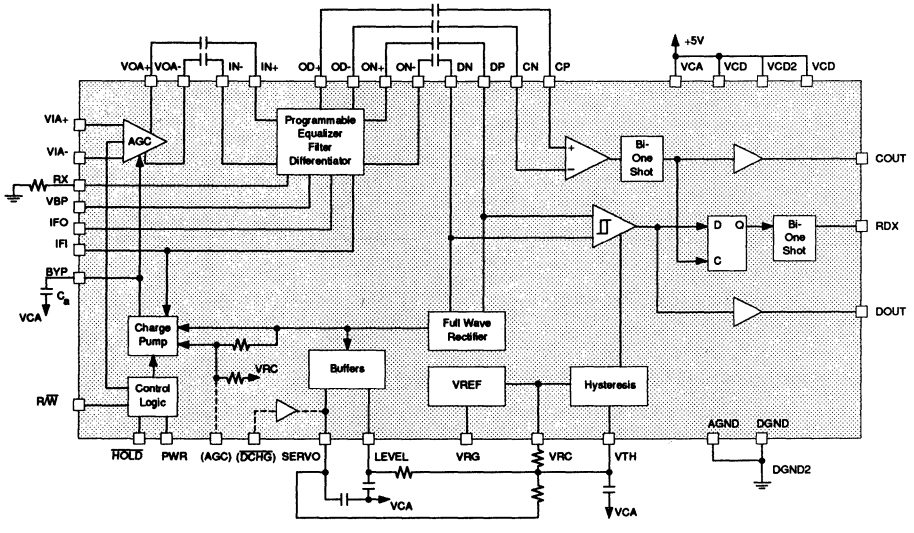
Write to read transient recovery is enhanced by providing AGC input impedance switching and a selectable Fast Recovery mode that provides a higher decay current.

Additionally, the SSI 32P3040 contains an integrated programmable electronic filter with cutoff frequencies between 2.5 and 13 MHz. High frequency boost (for pulse slimming) of up to +9db is also provided. The SSI 32P3040 requires only a +5V power supply and is available in 36-lead SOM and 32-lead TQFP packages.

## FEATURES

- **Compatible with 32 Mbit/s data rate operation**
- **Fast attack/decay modes for rapid AGC recovery**
- **Dual rate charge pump for fast transient recovery charge pump currents track programmable channel bandwidth**
- **Low drift AGC hold, fast AGC recovery, and low AGC input impedance control signals. Circuitry supports programmable gain non-AGC operation**
- **Temperature compensated, exponential control AGC**
- **Precision wide bandwidth fullwave rectifier**
- **Supports programmable pulse slimming equalization and programmable channel filter and differentiator with no external filter components**
- **±2% Filter group delay variation from 0.3FC to FC**
- **Servo burst output available**
- **Differential hysteresis qualifier comparator to ease clock channel timing**
- **Accurate feed forward or fixed threshold set**

## BLOCK DIAGRAM



# SSI 32P3040
# Pulse Detector with Programmable Filter

## FEATURES (continued)

- 1 ns max pulse pairing with sine wave input
- 5 mW low power idle mode
- TTL read data output
- +5V only operation
- 36-pin SOM and 32-pin TQFP packages

## FUNCTIONAL DESCRIPTION

The SSI 32P3040 Pulse Detector is designed to support a 32 Mbit/s data rate. The signal processing circuits include a wide band variable gain amplifier, a programmable electronic filter, differentiator and pulse slimming equalizer, a precision wide bandwidth fullwave rectifier, and a dual rate charge pump. A fully differential filter, differentiator, equalizer, and fullwave rectifier are provided to minimize external noise pick-up. To optimize recovery for constant density recording, the AGC charge pump current tracks the programmable filter current IFI. The differentiator zero tracks the programmable filter cutoff frequency. Thus in constant density recording applications, an approximately constant differentiated signal amplitude is maintained. The desired filter response and equalization are easily programmed with the SSI 32D4661, Time Base Generator DACs. A dual rate attack charge pump and a Fast Decay mode are included for fast transient recovery. At maximum IFI current, the normal AGC attack current is 0.28 mA. When the signal exceeds 125% of the nominal signal level, the attack current is increased by a factor of 5. The nominal decay current at max IFI is 5.6 µA. The decay current is increased 20 times when in the fast decay mode. In this mode, transients that produce low gain will recover more rapidly with the fast decay current, while transients that produce high gain will put the circuit in the fast attack recovery mode. The decay modes are automatically controlled within the device. When R/$\overline{W}$ is low, the AGC is in its hold mode and its input impedance is switched low. When R/$\overline{W}$ is switched high, the AGC remains in the hold and low input impedance state for 0.7 µs and then switches to the fast decay mode for 0.7 µs. The AGC amplifier input impedance is reduced to allow quick recovery of the AGC amplifier input AC coupling capacitors. When the $\overline{HOLD}$ input is low, the AGC action is stopped and the AGC amplifier gain is set by the voltage at the BYP pin. In most applications, the BYP pin voltage is stored on an external capacitor when $\overline{HOLD}$ goes low. In applications where AGC action is not desired, the BYP voltage can be set by a resistor divider network connected from VCC to VRC. If a programmable gain is desired, the resistor network could be driven by a current DAC. The precision fullwave rectifier produces an accurate Level and Servo output signal. These outputs are referenced to the reference voltage VRC. SERVO and LEVEL are buffered open emitter outputs with 100 ohm series current limiting resistors. These outputs could be further filtered with external capacitors.

LEVEL has an internal 50 µA discharge current source. An optional Servo output capacitor discharge circuit can be included. An external resistor connected to the RX pin sets the electronic filter reference current which is the source from pin IFO. If a programmable frequency response is desired, a portion of the current from IFO, which is proportional to absolute temperature, must be injected into pin IFI. This could be accomplished by a current DAC. Some frequency response programming may be accomplished by connecting IFO to IFI and switching different resistors to pin RX. Frequency boost is accomplished by varying the voltage at VBP. VBP has a nominal 100 mV built-in offset so that the circuit has 0 dB boost for VBP below 100 mV. The voltage at VBP should be proportional to the reference voltage at pin VRG.

A differential comparator with floating hysteresis threshold allows differential signal qualification for noise rejection. An accurate feed forward qualification level is generated by comparing the difference between LEVEL and VRC. VRC is referenced to VCA. Thus with the VTH resistor network connected from VCA to VRC, an accurate fixed threshold can be established. The threshold is clamped to a minimum value of 50 mV. Thus a qualified signal must exceed this minimum level even when the VTH-VRC voltage is zero. A qualified signal zero crossing triggers the output one shot. The one shot period is set internally. Low level differential outputs are provided for high speed operation and to minimize noise generation.

## PIN DESCRIPTION

### INPUT PINS

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| VIA+, VIA- | I | AGC Amplifier input pins. |
| IN+, IN- | I | Equalizer/filter input pins. |
| DP, DN | I | Data inputs to data comparators and fullwave rectifier. |
| CP, CN | I | Differentiated data inputs to the clock comparator. |
| VTH | I | Threshold level setting input for the data comparators. |
| R/$\overline{W}$ | I | TTL compatible input when high puts the charge pump in the normal mode. |
| PWR | I | TTL compatible input when high puts the circuit in its normal operating mode. |
| $\overline{HOLD}$ | I | TTL compatible input when low disables the AGC action by turning off the charge pump. |
| $\overline{DCHG}$ | I | Optional TTL compatible input pin when low produces a discharge current at the SERVO pin. Not available in 36 pin SO package. |
| **OUTPUT PINS** | | |
| VOA+, VOA- | O | AGC amplifier output pins. |
| ON+, ON- | O | Equalizer/filter normal output pins. |
| OD+, OD- | O | Equalizer/filter differentiated output pins. |
| DOUT | O | Test point for monitoring the data F/F D-input. Usage requires an external 2.4K resistor from DOUT to GND. (Not available in 32-pin TQFP package.) |
| COUT | O | Test points for monitoring the data F/F clock inputs. Usage requires an external 2.4K resistor from DOUT to GND. (Not available in 32-pin TQFP package.) |
| $\overline{RD}$ | O | TTL compatible read data output pins. |
| LEVEL | O | Open NPN emitter output that provides a fullwave rectified signal for the VTH input. The signal is referenced to VRC. |
| SERVO | O | Open NPN emitter output that provides a fullwave rectified servo signal. The signal is referenced to VRC. |
| **ANALOG PINS** | | |
| VRC | - | Reference voltage pin for SERVO and LEVEL. VRC is referenced to VCA. |
| VRG | - | Reference voltage pin for the programmable filter. VRG is referenced to ground. |
| VBP | - | The equalizer high frequency boost is set by an external voltage applied to this pin. VBP must be proportional to VRG. Programmable boost is implemented by using a DAC that uses VRG as its reference. A fixed amount of boost can be set by an external resistor divide network connected from VBP to VRG and GND. |
| RX | - | Pin to set filter reference current. External resistor Rx from this pin to ground sets the filter reference current IFO. |
| IFO | | Reference current output pin. The reference current is normally supplied as the reference current to a current DAC which generates the programmable input current for the IFI pin. |

## PIN DESCRIPTION (continued)

**ANALOG PINS** (continued)

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| IFI | | Programmable filter input current pin. The filter cutoff frequency is proportional to the current into this pin. The current must be proportional to the reference current out of IFO. A fixed filter cutoff frequency is generated by connecting IFO to IFI and selecting Rx to set the desired frequency. |
| AGC | | Optional reference voltage input for the AGC. The reference voltage is normally set by an internal resistor divider for VCC to VRC. (Not available in 36 pin SO package). |
| BYP | | The AGC integrating capacitor $C_A$ is connected between BYP and VCA. |
| VCA, VCD,VCD2 | | Analog and Digital +5 volts. |
| AGND, DGND, DGND2 | | Analog and Digital grounds. |

## ELECTRICAL SPECIFICATIONS

Unless otherwise specified, 4.5V<VCC<5.5V, 0°C<Ta<70°C

**ABSOLUTE MAXIMUM RATINGS** (Operation above maximum ratings may damage the device.)

| PARAMETER | RATING |
|---|---|
| Storage Temperature | -65 to +150°C |
| Junction Operating Temperature,Tj | +130°C |
| Supply Voltage, VCA, VCD | -0.7 to 7V |
| Voltage Applied to Inputs | -0.5 to VCA, VCD +0.5V |

**RECOMMENDED OPERATING CONDITIONS**

| PARAMETER | | RATING |
|---|---|---|
| Supply Voltage | VCA = VCD = VCC | 4.5V<VCC<5.5V |
| Ambient Temperature, Ta | | 0°C<Ta<70°C |

**POWER SUPPLY**

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| ISS | Supply Voltage Current | Active mode | | 75 | 90 | mA |
| | | Low-Power mode | | 1 | 1.5 | mA |
| PD | Power Dissipation | Active mode | | 400 | 500 | mW |
| | | Low-Power mode | | 5 | 8 | mW |

**LOGIC SIGNALS**

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| VIL | TTL Input Low Voltage | | -0.3 | | 0.8 | V |
| VIH | TTL Input High Voltage | | 2.0 | | VCC +0.3 | V |
| IIL | TTL Input Low Current | VIL = 0.4V | | | -0.4 | mA |
| IIH | TTL Input High Current | VIH = 2.7V | | | 0.1 | mA |
| VOH | TTL Output High Voltage | IOH = -400µA | 2.4 | | | V |
| VOL | TTL Output Low Voltage | IOL = 3 mA | | | 0.5 | Vpp |
| TRDRF | Output Rise and Fall Time | CL = 15 pF | | | 7 | ns |
| TH | Hold Input Switching Times | | | | 0.3 | µs |
| TWR | Write to Read Input Short Time | R/$\overline{W}$ pin low to high | 0.5 | | 1.4 | µs |

**AGC AMPLIFIER**

The input signals are AC coupled to VIA+ and VIA-, VOA+ and VOA- are AC coupled to IN+ and IN-, ON+ and ON- are AC coupled to DP and DN, Ca 1000 pF, Fin = 4 MHz. Unless otherwise specified, the output is measured differentially at VOA+ and VOA-, Fin = 4 MHz and filter boost at Fc = 0dB.

| | | | | | | |
|---|---|---|---|---|---|---|
| VIR | Input Range | Filter boost at FC = 0 dB | 24 | | 240 | mVppd |
| | | Filter boost at FC = 9 dB | 20 | | 120 | mVppd |
| VDPN | DP-DN voltage | (VIA+) - (VIA-) = 0.1 Vpp | 0.95 | | 1.05 | Vppd |
| VDPNV | DP-DN Voltage Variation | 24 mV < (VIA+) - ( VIA-) < 240 mV | | | 8.0 | % |
| AV | Gain Range | | 1.9 | | 22 | V/V |
| AVPV | Gain Sensitivity | | | 38 | | dB/V |
| VOADR | VOA+, VOA- Dynamic Range | THD = 1% max | 0.75 | | | Vpp |
| ZIN | Input Impedance | R/$\overline{W}$= high | 3.0 | | 7.5 | kΩ |
| ZCMIN | Common Mode | R/$\overline{W}$ = high | | 1.5 | | kΩ |
| | Input Impedance | R/$\overline{W}$ = low | | 200 | | Ω |
| VOS | Output Offset Voltage Variation | Over gain range | -200 | | +200 | mV |
| VINO | Input Noise Voltage | gain = max, filter not connected to VOA+, VOA-, Rs = 0Ω, Bw = 15 MHz | | 5 | 10 | nV/√Hz |
| BW | Bandwidth | No AGC action | 55 | 75 | | MHz |
| CMRR | Common-mode Rejection Ratio | gain = max, Vin = VDC + 100 mVpp @ 5 MHz | 40 | 65 | | dB |
| PSRR | Power Supply Rejection Ratio | gain = max, 100 mVpp @ 5 MHz on VCA, VCD, VCD2 | 45 | 67 | | dB |
| TGD | Gain Decay Time | VIA+ VIA- = 240 mV to 120 mV VOA+ VOA- >0.9 Final Value BYP ≤, 1000 pF, IFI = max | | 34 | 44 | µs |
| TGA | Gain Attack Time | VIA+ VIA- = 120 mV to 240 mV VOA+ VOA- <1.1 Final Value BYP ≤, 1000 pF, IFI = max | | 1.5 | 2 | µs |

## ELECTRICAL SPECIFICATIONS (continued)

Unless otherwise specified, 4.5V<VCC<5.5V, 0°C<Ta<70°C

### AGC CONTROL

The input signals are AC coupled to DP and DN. Ca = 1000 pF, LEVEL load = 50 µA, SERVO load = 100 µA.

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| VDI | DP-DN Signal Input Range | | | | 1.4 | Vpp |
| ALO | Level (Servo) Output Gain | DP-DN = .5 to 1 Vpp | 0.73 | | 0.81 | V/Vpp |
| BWL | Level (Servo) Output Bandwidth | 1 dB | 15 | | | MHz |
| VLO | Level Offset Voltage | Output-VRC, IL = 50 µA | | | 30 | mV |
| VSO | Servo Offset Voltage | Output - VRC, IL = 100 µA | | | 30 | mV |
| ZLS | Level (Servo) Output Impedance | IL = 100 µA | | 200 | 300 | Ω |
| ID | Discharge Current | | | 0.008 x IFI | | mA |
| IDF | Fast Discharge Current | 0.7 to 1.4 µs after R/$\overline{W}$ goes high | | 20 x Id | | mA |
| ICH | Charge Pump Attack Current | | | 50 x Id | | mA |
| ICHF | Charge Pump Fast Attack Current | DP-DN = 1.35 Vpp | | 5 x Ich | | mA |
| IBYP | Pin Leakage Current | $\overline{HOLD}$ = low | -0.1 | | 0.1 | µA |
| VRC | Reference Voltage | | VCC-2.52 | | VCC-2.15 | V |
| IVRC | Output Drive | | -0.75 | | 0.75 | mA |
| VRG | Reference | | 2.15 | | 2.5 | V |
| IVRG | Source Current | | 1 | | | mA |
| VAGC | Pin Voltage | | | VRC+1.0 | | V |

**EQUALIZER/FILTER** The input signals are AC coupled to IN+ and IN-.

| | | | | | | |
|---|---|---|---|---|---|---|
| *fc* | Filter Cutoff Frequency | *fc* = 19.14(IFI/IFO)(1/Rx) | 2.5 | | 13.5 | MHz |
| VRX | PTAT Reference Current Set Output Voltage | TA = 25°C<br>IRX = 0 - 0.7 mA<br>Rx > 1.21 kΩ | | 850 | | mV |
| IFOR | PTAT Reference Current Output Current Range | TA = 25°C<br>1.21 kΩ < Rx < 7.73 kΩ<br>IFO = VRX/Rx | 0.11 | | 0.7 | mA |

**EQUALIZER/FILTER** (continued)

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| IFIR | PTAT Programming Current Range | TA = 25°C, $V_{RX}$ = 850 mV | 0.11 | | 0.7 | mA |
| VBPR | Input Voltage Range | | 0 | | VRG | V |
| IBP | Input Bias Current | | | | 3 | µA |
| FCA | Filter FC Accuracy | FC = 5 to 13.5 MHz | -10 | | +10 | % |
| AO | [(ON+)-(ON-)]/[(IN+)-(IN-)] Normal Gain | F = 0.67 FC | 1.4 | | 2.2 | V/V |
| AD | [(OD+)-(OD-)]/[(IN+)-(IN-)] Diff Gain | F = 0.67 FC | 1.0AO | | 1.3AO | V/V |
| FB | Frequency Boost at FC | FB = 20 log [1.884(VBP-0.1) /VRG+1] VBP -0.1>0 | 0 | | 9.5 | dB |
| FBA | Frequency Boost Accuracy | FB = 9 dB | -1 | | +1 | dB |
| TGD | Group Delay Variation | 0.3 FC to FC = 13.5 MHz FB = 0 to 9 dB | -2 | | +2 | % |
| VOO | Output Offset Voltage | Variation over entire frequency range | -200 | | +200 | mV |
| VOF | Filter Output Dynamic Range | THD = 1.5% max | 1.0 | | | Vpp |
| | | THD = 3.0% max F = 0.67 FC | 1.5 | | | Vpp |
| RINF | Filter Input Resistance | | 4.0 | 6.0 | 8.0 | kΩ |
| CINF | Filter Input Capacitance | | | | 7 | pF |
| RO | Filter Output Resistance | IO = 0.5 mA | | 70 | 85 | Ω |
| IFOD | Filter Output Drive Current | | -1 | | +1 | mA |
| VNN | Eout Output Noise Voltage ON+ ON- | BW = 100 MHz, Rs = 50Ω IFI = 0.7 mA, VBP = 0 | | 2.2 | 3.0 | mVRMS |
| | | BW = 100 MHz, Rs = 50Ω IFI = 0.7 mA, VBP = VRG | | 3.0 | 4.5 | mVRMS |
| VND | Eout Output Noise Voltage OD+ OD- | BW = 100 MHz, Rs = 50Ω IFI = 0.7 mA, VBP = 0 | | 5.4 | 6.4 | mVRMS |
| | | BW = 100 MHz, Rs = 50Ω IFI = 0.7 mA, VBP = VRG | | 9.6 | 10.6 | mVRMS |

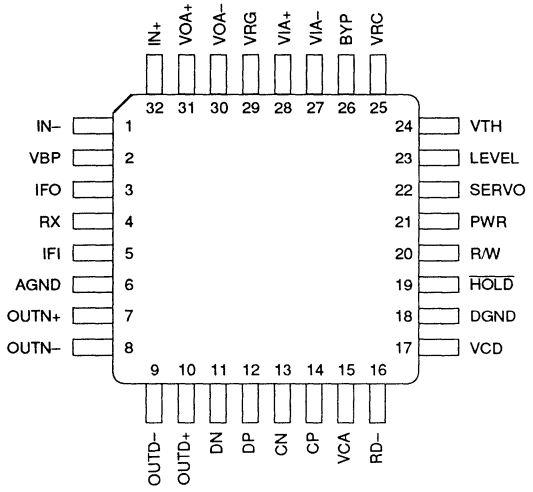
**DATA COMPARATOR**
The input signals are AC coupled to DP and DN.

| | | | | | |
|---|---|---|---|---|---|
| DR DP-DN Signal Range | | | | 1.5 | Vpp |
| RINDC Differential Input Resistnace | | 7 | | 14 | kΩ |
| CINDC Differential Input Capacitance | | | | 5 | pF |
| ATH Threshold Voltage Gain, Kth | 0.3 < VTH-VRC < 0.75 | 0.42 | | 0.49 | V/V |
| VIAMIN Minimum Threshold Voltage | VTH-VRC ≤ 0.11V | | .05 | | V |
| TPDDC Propagation Delay | To DO+, DO- | | 10 | | ns |
| ITH VTH Input Bias Current | | | | 2 | μA |
| DOUTSS DOUT Signal Swing | 2.4K from DOUT to GND | | 0.5 | | V |

**CLOCKING**
The input signals are AC coupled to CP and CN.

| | | | | | |
|---|---|---|---|---|---|
| CR CP-CN Signal Range | | | | 1.5 | Vpp |
| RINCL Differential Input Resistance | | 7 | | 14 | kΩ |
| CINCL Differential Input Capacitance | | | | 5 | pF |
| TDS D F/F Set Up Time | DP-DN threshold to CP-CN zero cross | 0 | | | ns |
| TPP Pulse Pairing | Vs = 1Vpp, F = 2.5 MHz | | | 1 | ns |
| TPDCL Propagation Delay to RD | Vs = 20 mVpp sq wave | | 14 | 20 | ns |
| RDPW Output Pulse Width | Measured at 1.4V level | 10 | | 27 | ns |
| COUTS Signal Swing | 2.4K from COUT to GND | | 0.5 | | V |

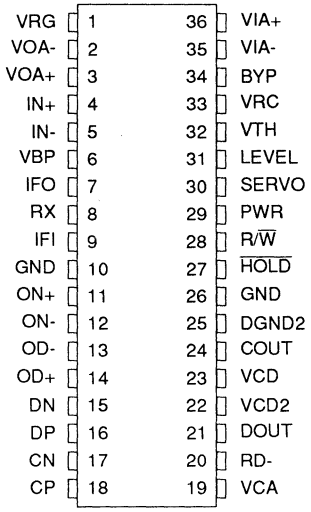
## PACKAGE PIN DESIGNATIONS
(Top View)




**32-Lead TQFP**

**THERMAL CHARACTERISTICS: θja**

| | |
|---|---|
| 32-Lead TQFP | 124° C/W |
| 36-Lead SOM | 75° C/W |




**36-Lead SOM**

CAUTION: Use handling procedures necessary for a static sensitive component.

## ORDERING INFORMATION

| PART DESCRIPTION | ORDER NO. | PKG. MARK |
|---|---|---|
| SSI 32P3040 | | |
| 32-Lead Thin Quad Flatpack | 32P3040-CGT | 32P3040-CGT |
| 36-Lead Small Outline | 32P3040-CM | 32P3040-CM |



Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 573-6000, FAX (714) 573-6914

**Notes:**

Section 3



# PROGRAMMABLE ELECTRONIC FILTERS

silicon systems®
A TDK Group Company

# SSI 32F8001/8002
## Low-Power Programmable Electronic Filter

**Advance Information**

December 1992

3

## DESCRIPTION

The SSI 32F8001/8002 Programmable Electronic Filters provide an electronically controlled low–pass filter with a separate differentiated low–pass output. A seven–pole, low–pass filter is provided along with a single-pole, single-zero differentiator. Both outputs have matched delays. The delay matching is unaffected by any amount of programmed equalization or bandwidth. This programability combined with low group delay variation make the SSI 32F8001/8002 ideal for use in constant density recording applications. Pulse slimming equalization is accomplished by a two–pole, low–pass with a two–pole, high–pass feed forward section to provide complimentary real axis zeros. A variable attenuator is used to program the zero locations.

The SSI 32F8001 programmable equalization and bandwidth characteristics can be controlled by external DACs. Fixed characteristics are easily accomplished with three external resistors, in addition equalization can be switched in or out by a logic signal.

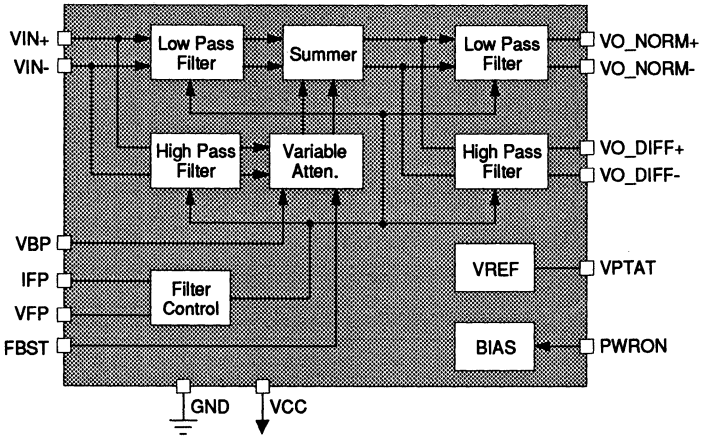
The SSI 32F8002 is identical to the SSI 32F8001, except for the cutoff frequency range, which is 6 to 18 MHz in the SSI 32F8002.

The SSI 32F8001/8002 require only a +5V supply and are available in 16-pin SON and SOL packages.

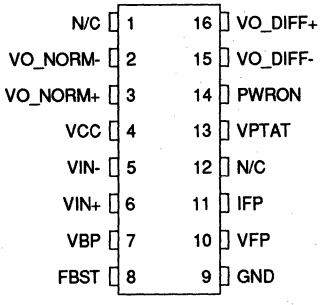
## FEATURES

- **Ideal for multi-rate systems applications**
- **Programmable filter cutoff frequency ($fc$ = 9 to 27 MHz, 32F8001; $fc$ = 6 to 18 MHz, 32F8002)**
- **Programmable pulse slimming equalization (0 to 13 dB boost at the filter cutoff frequency)**
- **Matched normal and differentiated low-pass outputs**
- **Differential filter input and outputs**
- **±10% cutoff frequency accuracy**
- **±2% maximum group delay variation from 0.2 $fc$ to $fc$ here,**
  - **9 MHz ≤ $fc$ ≤ 27 MHz SSI 32F8001**
  - **6 MHz ≤ $fc$ ≤ 18 MHz SSI 32F8002**
- **Total harmonic distortion less than 1.5%**
- **No external filter components required**
- **+5V only operation**
- **16-pin SON and SOL package**
- **Pin compatible with SSI 32F8011**

## BLOCK DIAGRAM




## PIN DIAGRAM




CAUTION: Use handling procedures necessary for a static sensitive component.

# SSI 32F8001/8002
# Low-Power Programmable Electronic Filter

## FUNCTIONAL DESCRIPTION

The SSI 32F8001/8002 are high performance programmable electronic filters. They feature a 7-pole 0.05° equiripple linear phase filter with matched normal and differentiated outputs.

### CUTOFF FREQUENCY PROGRAMMING

The SSI 32F8001 programmable electronic filter can be set to a filter cutoff frequency from 9 to 27 MHz with no boost (6 to 18 MHz for the SSI 32F8002).

Cutoff frequency programming can be established using either a current source fed into pin IFP whose output current is proportional to the SSI 32F8001/8002 output reference voltage VPTAT, or by means of an external resistor tied from the output voltage reference pin VPTAT to pin VFP. The former method is optimized using the SSI 32D4661 Time Base Generator, since the current source into pin IFP is available at the DAC F output of the SSI 32D4661. Furthermore, the voltage reference input is supplied to pin VR3 of the SSI 32D4661 by the reference voltage from the VPTAT pin of the SSI 32F8001/8002. This reference voltage is internally generated by a band-gap circuit in conjunction with a temperature varying reference to create a voltage which is proportional to absolute temperature.

The VPTAT voltage will compensate for internal temperature variation of the $fc$ and boost circuits.

The cutoff frequency, determined by the -3dB point relative to a very low frequency value (< 10 kHz), is related to the current IVFP injected into pin IFP by the following formulas.

$fc$ (ideal, in MHz)

(32F8001) = 45.0 • IFP = 45.0 • IVFP • 1.8/VPTAT

(32F8002) = 30.0 • IFP = 30.0 • IVFP • 1.8/VPTAT

where IFP and IVFP are in mA, 0.2 < IFP < 0.6 mA, and VPTAT is in volts. Ta = 25°C.

If a current source is used to inject current into pin IFP, pin VFP should be left open.

If the SSI 32F8001/8002 cutoff frequency is set using voltage VPTAT to bias up a resistor tied to pin VFP, the cutoff frequency is related to the resistor value by the following formulas.

$fc$ (ideal, in MHz)

(32F8001) = 45.0 • IFP = 45.0 • 1.8/(3 • Rx)

(32F8002) = 30.0 • IFP = 30.0 • 1.8/(3 • Rx)

Rx in kΩ

If pin VFP is used to program cutoff frequency, pin IFP should be left open.

### MAGNITUDE EQUALIZATION PROGRAMMING

The magnitude equalization, measured in dB, is the amount of high frequency peaking at the cutoff frequency relative to the original -3 dB point. For example, when 12 dB boost is applied, the magnitude response peaks up 9 dB above the DC gain.

The amplitude of the input signal at frequencies near the cutoff frequency can be increased using this feature. Applying an external voltage to pin VBP which is proportional to reference output voltage VPTAT (provided by the VPTAT pin) will set the amount of boost. A fixed amount of boost can be set by an external resistor divider network connected from pin VBP to pins VPTAT and GND. No boost is applied if pin FBST, frequency boost enable, is at a low logic level.

The amount of boost FB at the cutoff frequency Fc is related to the voltage VBP by the formula

FB (ideal, in dB) = 20 $\log_{10}$[3.46(VBP/VPTAT)+1], where 0 < VBP < VPTAT.

### POWER ON / OFF

The SSI 32F8001/8002 support a power down mode for minimal idle mode power dissipation. When PWRON is pulled up to logic 1, the device is in normal operation mode. When PWRON is pulled down to logic 0, or left open, the device is in the power down mode.

## PIN DESCRIPTION

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| VIN+, VIN- | I | Differential Signal Inputs. The input signals must be AC coupled to these pins. |
| VO_NORM+, VO_NORM- | O | Differential Normal Outputs. The output signals must be AC coupled. |
| VO_DIFF+, VO_DIFF- | O | Differential Differentiated Outputs. For minimum time skew, these outputs should be AC coupled. |
| IFP | I | Frequency Program Input. The filter cutoff frequency $fc$, is set by an external current IFP, injected into this pin. IFP must be proportional to voltage VPTAT. This current can be set with an external current generator such as a DAC. VFP should be left open when using this pin. |
| VFP | I | Frequency Program Input. The filter cutoff frequency can be set by programming a current through a resistor from VPTAT to this pin. IFP should be left open when using this pin. |
| VBP | I | Frequency Boost Program Input. The high frequency boost is set by an external voltage applied to this pin. VBP must be proportional to voltage VPTAT. A fixed amount of boost can be set by an external resistor divider network connected from VBP to VPTAT and GND. No boost is applied if the FBST pin is grounded, or at logic low. |
| FBST | I | Frequency Boost. A high logic level or open enables the frequency boost circuitry. A low input disables this function. |
| PWRON | I | Power On. A high logic level enables the chip. A low level or open pin puts the chip in a low power state. |
| VPTAT | O | PTAT Reference Voltage. This pin outputs a reference voltage which is proportional to absolute temperature (PTAT). VBP, VFP or IFP must be referenced to this pin for proper operation. |
| VCC | O | +5 Volt Supply. |
| GND | I | Ground |

## ELECTRICAL SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may damage the device.

| PARAMETER | RATINGS |
|---|---|
| Storage Temperature | -65 °C to +150 °C |
| Junction Operating Temperature, Tj | +130 °C |
| Supply Voltage, VCC | -0.5V to 7V |
| Voltage Applied to Inputs | -0.5V to VCC |

## ELECTRICAL SPECIFICATIONS (continued)

### RECOMMENDED OPERATING CONDITIONS

| PARAMETER | RATINGS |
|---|---|
| Supply voltage, VCC | 4.50V < VCC < 5.50V |
| Ambient Temperature | 0 °C < Ta < 70 °C |

### ELECTRICAL CHARACTERISTICS

Unless otherwise specified recommended operating conditions apply.

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| **Power Supply Characteristics** | | | | | | |
| Power Supply Current | ICC | PWRON ≤ 0.8V | | 0.1 | 0.5 | mA |
| Power Supply Current | ICC | PWRON ≥ 2.0V | | 46 | 60 | mA |
| Power Dissipation | PD | PWRON ≥ 2.0V, VCC = 5.0V | | 230 | 300 | mW |
| | | PWRON ≥ 2.0V, VCC = 5.5V | | 275 | 330 | mW |
| | | PWRON ≤ 0.8V | | 0.5 | 2.5 | mW |
| **DC Characteristics** | | | | | | |
| High Level Input Voltage | VIH | TTL input | 2.0 | | | V |
| Low Level Input Voltage | VIL | | | | 0.8 | V |
| High Level Input Current | IIH | VIH = 2.7V | | | 20 | µA |
| Low Level Input Current | IIL | VIL = 0.4V | | | −1.5 | mA |
| **Filter Characteristics** | | | | | | |
| Filter Cutoff Frequency *(*f* -3dB) | *fc | 32F8001 $fc = \frac{45\ MHz}{mA}(IVFP)$ | 9.0 | | 27.0 | MHz |
| | | IVFP = 0.2 to 0.6 µA, Ta = 25v °C | | | | |
| | | 32F8002 $fc\frac{30\ MHz}{mA}(IVFP)$ | 6 | | 18 | MHz |
| Filter *fc* Accuracy | FCA | *fc* = max. | −10 | | +10 | % |
| VO_NORM Diff Gain | AO | F = 0.67 *fc*, FB = 0 dB | 0.8 | | 1.20 | V/V |
| VO_DIFF Diff Gain | AD | F = 0.67 *fc*, FB = 0 dB | 0.85AO | | 1.15AO | V/V |
| Frequency Boost at *fc* | FB | VBP = VPTAT *fc* = max. | 11.5 | 13.0 | 14.5 | dB |
| | | *fc* = min. | 11.0 | 12.5 | 14.0 | dB |
| Frequency Boost Accuracy | FBA | VBP/VPTAT = 0.5255 *fc* = max. | −1 | | +1 | dB |
| | | VBP/VPTAT = 1.0 *fc* = max. | −1.5 | | +1.5 | dB |

**Filter Characteristics** (continued)

| PARAMETER | | CONDITIONS | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| Group Delay Variation Without Boost | TGDO | $fc$ = max., $\frac{VBP}{VPTAT}=0$ | 32F8001 | –500 | | +500 | ps |
| | | F = 0.2 $fc$ to $fc$ | 32F8002 | -750 | | +750 | ps |
| | | $fc$ = min., $\frac{VBP}{VPTAT}=0$ | 32F8001 | -1.5 | | +1.5 | ns |
| | | F = 0.2 $fc$ to $fc$ | 32F8002 | -2.25 | | +2.25 | ns |
| | | $fc$ = 9 MHz - 27 MHz (32F8001)<br>$fc$ = 6 MHz - 18 MHz (32F8002)<br>F = 0.2 $fc$ to $fc$ $\frac{VBP}{VPTAT}=0$ | | –2 | | +2 | % |
| | | $fc$ = 9 MHz - 27 MHz, $\frac{VBP}{VPTAT}=0$ | | -4 | | +4 | % |
| | | F = $fc$ to 1.75 $fc$ | 32F8001 | | | | |
| | | $fc$ = 6 MHz - 18 MHz, $\frac{VBP}{VPTAT}=0$ | | -3 | | +3 | % |
| | | F = $fc$ to 1.75 $fc$ | 32F8002 | | | | |
| | TGDB | $fc$ = max, VBP = VPTAT | 32F8001 | –500 | | +500 | ps |
| | | F = 0.2 $fc$ to $fc$ | 32F8002 | -750 | | +750 | |
| | | $fc$ = min., VBP = VPTAT | 32F8001 | -1.5 | | +1.5 | ns |
| | | F = 0.2 to $fc$ | 32F8002 | -2.25 | | +2.25 | ns |
| | | $fc$ = 9 MHz - 27 MHz (32F8001)<br>$fc$ = 6 MHz - 18 MHz (32F8002)<br>F = 0.2 $fc$ to $fc$, VBP = VPTAT | | –2 | | +2 | % |
| | | $fc$ = 9 MHz - 27 MHz, VBP = VPTAT | | -4 | | +4 | % |
| | | F = $fc$ to 1.75 $fc$ | 32F8001 | | | | |
| | | $fc$ = 6 MHz to 18 MHz, VBP = VPTAT | | -3 | | +3 | % |
| | | F = $fc$ to 1.75 $fc$ | 32F8002 | | | | |
| Filter Input Dynamic Range | VIF | THD = 1% max, F = 0.67 $fc$, VBP = 0V (1000 pF across Rx) | | 1.0 | | | Vpp |
| | | THD = 1.5% max, F = 0.67 $fc$, VBP = 0V, Normal output (1000 pF across Rx) | | 1.5 | | | Vpp |
| | | THD = 2.0% max, F = 0.67 $fc$, VBP = 0V, Differentiated output (1000 pF across Rx) | | 1.5 | | | Vpp |

## ELECTRICAL SPECIFICATIONS (continued)

**Filter Characteristics** (continued)

| PARAMETER | | CONDITIONS | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| Filter Output Dynamic Range | VOF | THD = 1% max, F = 0.67 *fc*<br>RLOAD ≥ 1kΩ (1000 pF across Rx) | | 1.0 | | | Vpp |
| Filter Diff Input Resistance | RIN | | | 3.0 | | | kΩ |
| Filter Input Capacitance | CIN | | | | | 7 | pF |
| Output Noise Voltage Differentiated Output | EOUT | BW = 100 MHz, Rs = 50Ω<br>*fc* = max, VBP = 0V | 32F8001 | | 3.6 | | mVRms |
| | | | 32F8002 | | 3.3 | | |
| Output Noise Voltage Normal Output | EOUT | BW = 100 MHz, Rs = 50Ω<br>*fc* = max, VBP = 0V | 32F8001 | | 2.3 | | mVRms |
| | | | 32F8002 | | 2.0 | | |
| Output Noise Voltage Differentiated Output | EOUT | BW = 100 MHz, Rs = 50Ω<br>*fc* = max, VBP = VPTAT | 32F8001 | | 5.8 | | mVRms |
| | | | 32F8002 | | 5.0 | | |
| Output Noise Voltage Normal Output | EOUT | BW = 100 MHz, Rs = 50Ω<br>*fc* = max, VBP = VPTAT | 32F8001 | | 2.9 | | mVRms |
| | | | 32F8002 | | 2.5 | | |
| Filter Output Sink Current | IO– | | | 1.0 | | | mA |
| Filter Output Source Current | IO+ | | | 2.0 | | | mA |
| Filter Output Resistance (Single ended) | RO | IO+ = 1.0 mA | | | | 60 | Ω |
| **Filter Control Characteristics** | | | | | | | |
| Reference Voltage | VPTAT | Tj = 25 °C | | | 1.8 | | V |
| PTAT Voltage Input | VFP | | | | 2/3 VPTAT | | V |
| Programming Current Range | IVFP | TA = 25 °C | | 0.2 | | 0.6 | mA |
| Programming Current Range | $V_{VBP}$ | | | 0 | | VPTAT | V |
| Voltage at pin IFP | $V_{IFP}$ | $I_{VFP}$ = 0 mA | | | 2/3 VPTAT | | V |

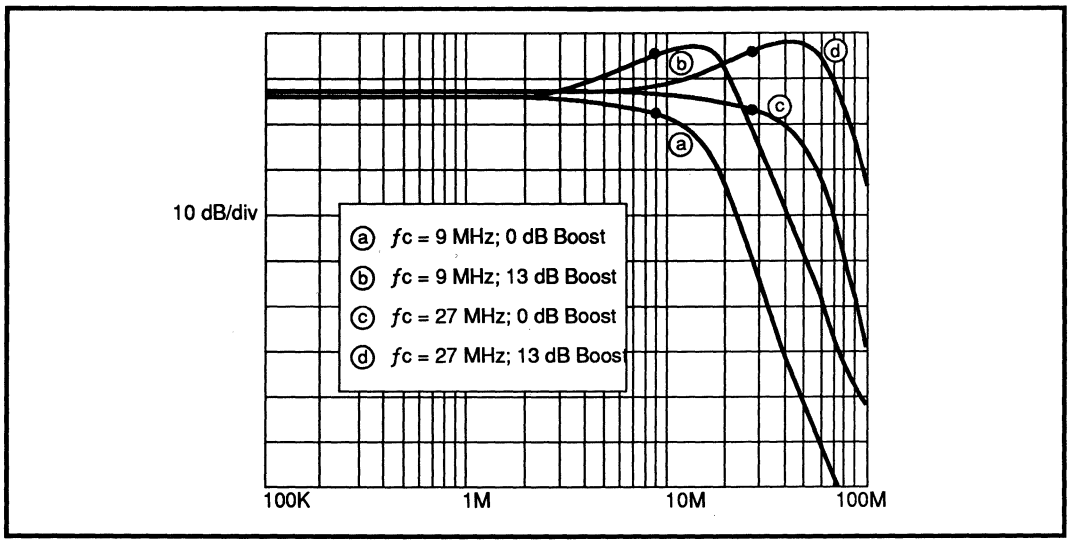



**FIGURE 1: 32F8001 Normal Low Pass Response**

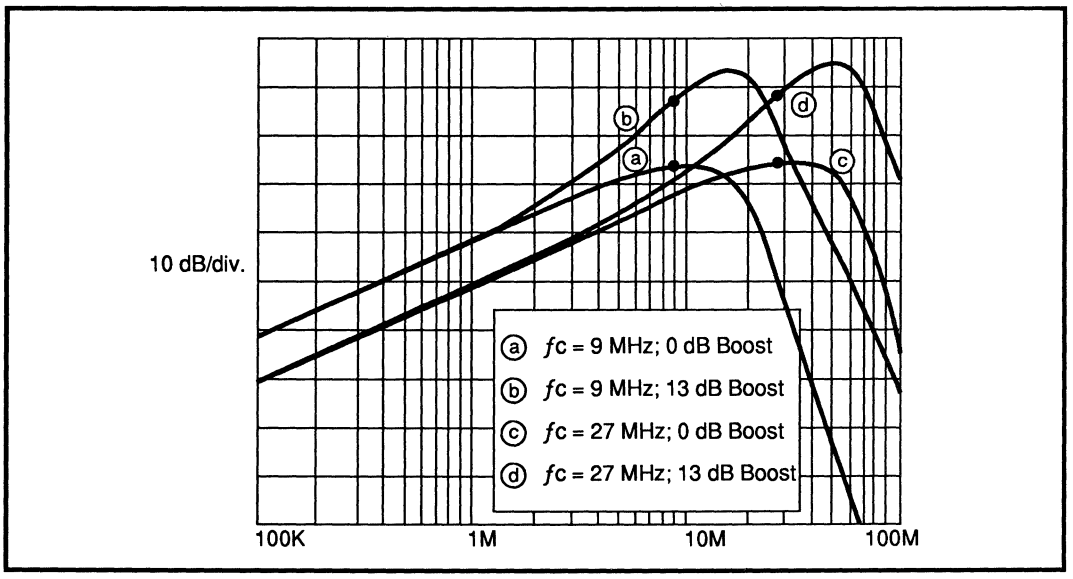



**FIGURE 2: 32F8001 Differentiated Low Pass Response**

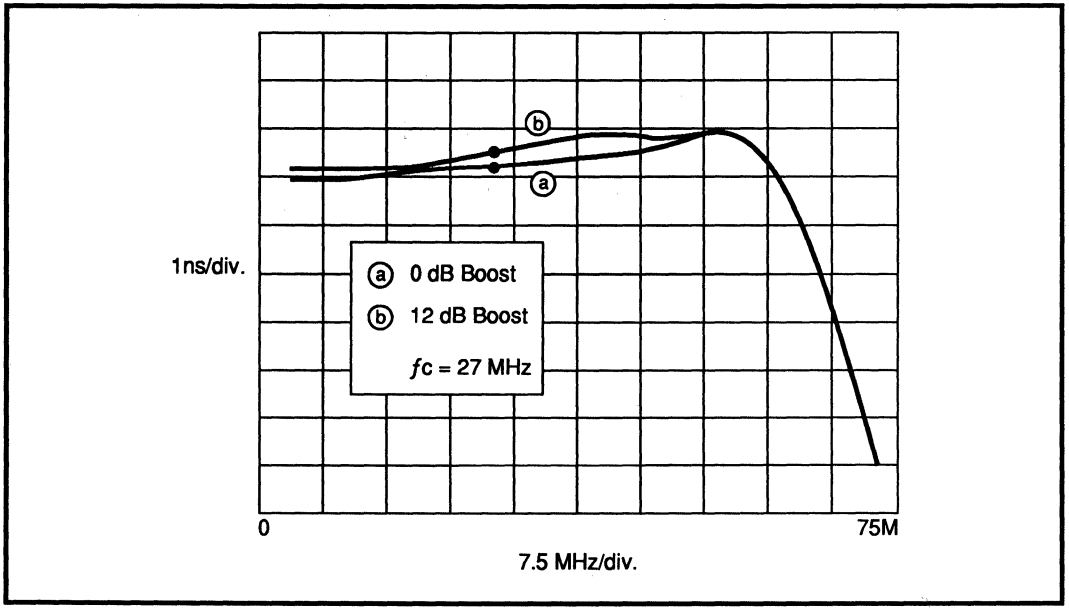
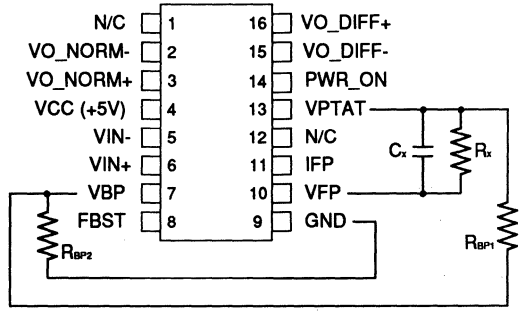



**FIGURE 3: 32F8001 Group Delay Response with *fc* = 27 MHz**




VPTAT = 1.8V (25 °C)

$V_{VFP}$ = 2/3 (VPTAT)

IVFP range: 0.2 mA to 0.6 mA @25°C

(9 to 27 MHz no boost 32F8001)

(6 to 18 MHz no boost 32F8002)

Fixed frequency programming is accomplished as shown in the drawing above.

In this case IVFP (programming current) is equivalent to $\frac{VPTAT}{3} \cdot \frac{1}{R_x}$

i.e., $fc$ = 27 MHz then

IVFP = 0.6 mA @25 °C Rx = 1 KΩ

Fixed boost programming is also accomplished as shown above. In this case $V_{VBP}$ is set by a voltage divider, where $V_{VBP}$ is a fraction of VPTAT.

i.e., boost = 9 dB then,

VBP/VPTAT = 0.5255 9 dB = 20 log [3.46 (0.5255) + 1]

$$\frac{R_{BP2}}{R_{BP1}} = \frac{1}{\left(\frac{VPTAT}{VBP} - 1\right)} = 1.107$$

Cx = 1000 pF - Cx is needed for lower THD at lower $fc$.

**FIGURE 4: 32F8001/8002 Applications Setup**

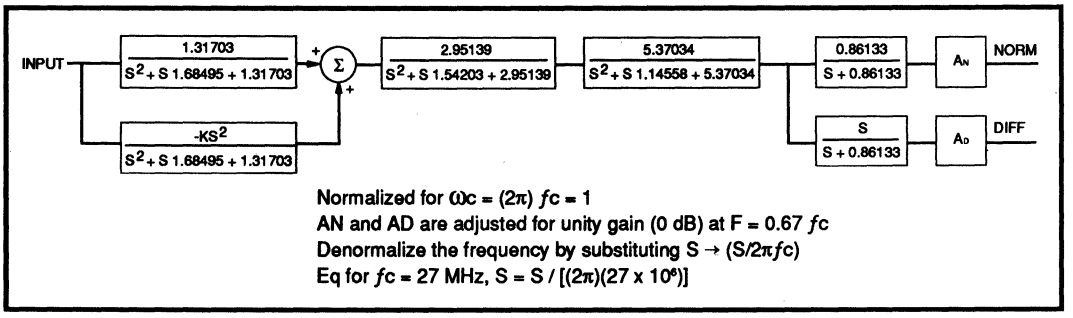



**FIGURE 5: 32F8001/8002 Normalized Block Diagram**

**TABLE 1: 32F8001/8002 Frequency Boost Calculations**

Assuming 13 dB boost for VBP = VPTAT

$$\frac{VBP}{VPTAT} \cong \frac{\left(10^{(FB/20)}\right)-1}{3.46}$$

| Boost | K | VBP/VPTAT | Boost | K | VBP/VPTAT |
|---|---|---|---|---|---|
| 1 dB | 0.16 | 0.035 | 6 dB | 1.31 | 0.288 |
| 2 dB | 0.34 | 0.075 | 7 dB | 1.63 | 0.358 |
| 3 dB | 0.54 | 0.119 | 8 dB | 1.99 | 0.437 |
| 4 dB | 0.77 | 0.169 | 9 dB | 2.40 | 0.526 |
| 5 dB | 1.03 | 0.225 | 10 dB | 2.85 | 0.625 |
| | | | 11 dB | 3.36 | 0.737 |
| | | | 12 dB | 3.43 | 0.862 |
| | | | 13 dB | 4.57 | 1.00 |

or,

$$\text{boost in dB} = 20\log\left[3.46\left(\frac{VBP}{VPTAT}\right)+1\right]$$

| VBP/VPTAT | Boost | VBP/VPTAT | Boost |
|---|---|---|---|
| 0.1 | 2.581 dB | 0.6 | 9.760 dB |
| 0.2 | 4.568 dB | 0.7 | 10.686 dB |
| 0.3 | 6.184 dB | 0.8 | 11.522 dB |
| 0.4 | 7.546 dB | 0.9 | 12.285 dB |
| 0.5 | 8.723 dB | 1.0 | 13 dB |

**TABLE 2: Calculations**

Typical change in $f$-3 dB point with boost

| Boost (dB) | Gain@$fc$ (dB) | Gain@ peak (dB) | $f$peak/$fc$ | $f$-3dB/$fc$ |
|---|---|---|---|---|
| 0 | -3 | 0.00 | no peak | 1.00 |
| 1 | -2 | 0.00 | no peak | 1.21 |
| 2 | -1 | 0.00 | no peak | 1.51 |
| 3 | 0 | 0.15 | 0.70 | 1.80 |
| 4 | 1 | 0.99 | 1.05 | 2.04 |
| 5 | 2 | 2.15 | 1.23 | 2.20 |
| 6 | 3 | 3.41 | 1.33 | 2.33 |
| 7 | 4 | 4.68 | 1.38 | 2.43 |
| 8 | 5 | 5.94 | 1.43 | 2.51 |
| 9 | 6 | 7.18 | 1.46 | 2.59 |
| 10 | 7 | 8.40 | 1.48 | 2.66 |
| 11 | 8 | 9.59 | 1.51 | 2.73 |
| 12 | 9 | 10.77 | 1.51 | 2.80 |
| 13 | 10 | 11.92 | 1.53 | 2.87 |

Notes:
1. $fc$ is the original programmed cutoff frequency with no boost
2. $f$-3 dB is the new -3 dB value with boost implemented
3. $f$peak is the frequency where the amplitude reaches its maximum value with boost implemented

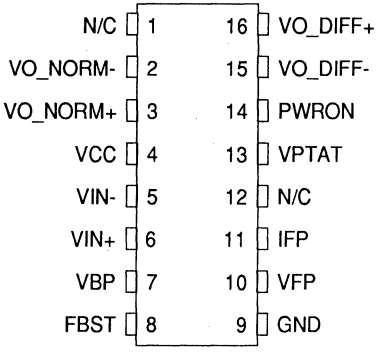
i.e., $fc$ = 9 MHz when boost = 0 dB

if boost is programmed to 5 dB then f-3 dB = 19.8 MHz

$f$peak = 11.07 MHz

## PACKAGE PIN DESIGNATIONS

(Top View)




**32F8001/8002**
**16-pin SON, SOL**

**THERMAL CHARACTERISTICS: θja**

| | |
|---|---|
| 16-lead SON (150 mil) | 105°C/W |
| 16-lead SOL (300 mil) | 100°C/W |

**Advance Information:** Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.



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A TDK Group Company

# SSI 32F8011/8012
## Programmable Electronic Filter

December 1992

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## DESCRIPTION

The SSI 32F8011/8012 Programmable Electronic Filter provides an electronically controlled low–pass filter with a separate differentiated low–pass output. A seven–pole, Bessel–type, low–pass filter is provided along with a single-pole, single-zero differentiator. Both outputs have matched delays. The delay matching is unaffected by any amount of programmed high frequency peaking (boost) or bandwidth. This programmability, combined with low group delay variation makes the SSI 32F8011/8012 ideal for use in many applications. Double differentiation high frequency boost is accomplished by a two–pole, low–pass with a two–pole, high–pass feed forward section to provide complementary real axis zeros. A variable attenuator is used to program the zero locations, which controls the amount of boost.

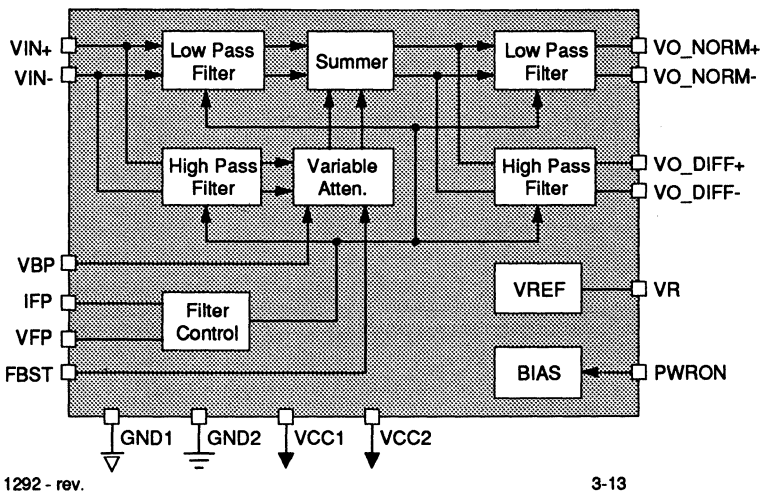
The SSI 32F8011/8012 programmable boost and bandwidth characteristics can be controlled by external DACs or DACs provided in the SSI 32D4661 Time Base Generator. Fixed characteristics are easily accomplished with three external resistors, in addition boost can be switched in or out by a logic signal.

The SSI 32F8011/8012 requires only a +5V supply and is available in 16-pin SON and SOL packages.

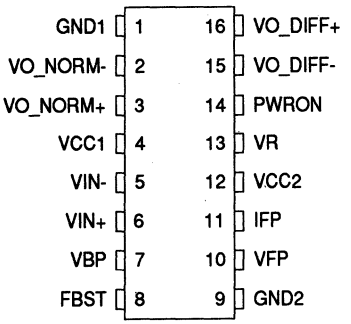
## FEATURES

- **Ideal for:**
  - **constant density recording applications**
  - **cellular telephone applications**
  - **radio**
  - **data acquisition**
  - **LAN**
- **Programmable filter cutoff frequency**
  **(SSI 32F8011 *fc* = 5 to 13 MHz)**
  **(SSI 32F8012 *fc* = 6 to 15 MHz)**
- **Programmable high frequency peaking**
  **(0 to 9 dB boost at the filter cutoff frequency)**
- **Matched normal and differentiated low-pass outputs**
- **Differential filter input and outputs**
- **±0.75 ns group delay variation from 0.2 *fc* to *fc* = 13 MHz**
- **Total harmonic distortion less than 1%**
- **+5V only operation**
- **16-pin SON, and SOL packages**

## BLOCK DIAGRAM




## PIN DIAGRAM




CAUTION: Use handling procedures necessary for a static sensitive component.

## FUNCTIONAL DESCRIPTION

The SSI 32F8011/8012, a high performance programmable electronic filter, provides a low pass Bessel-type seven pole filter with matched normal and differentiated outputs. The device has been optimized for usage with several Silicon Systems products, including the SSI 32D4661 Time Base Generator, the SSI 32P54x family of Pulse Detectors, and the SSI 32P4720 Combo chip (Data Separator and Pulse Detector).

### CUTOFF FREQUENCY PROGRAMMING

The programmable electronic filter can be set to a filter cutoff frequency from 5 to 13 MHz (with no boost) for SSI 32F8011 and 6 to 15 MHz for SSI 32F8012.

Cutoff frequency programming can be established using either a current source fed into pin IFP whose output current is proportional to the SSI 32F8011/8012 output reference voltage VR, or by means of an external resistor tied from the output voltage reference pin VR to pin VFP. The former method is optimized using the SSI 32D4661 Time Base Generator, since the current source into pin IFP is available at the DAC F output of the 32D4661. Furthermore, the voltage reference input is supplied to pin VR3 of the 32D4661 by the reference voltage VR from the VR pin of the 32F8011/8012. This reference voltage is an internally generated bandgap reference, which typically varies less than 1% over supply voltage and temperature variation.

The cutoff frequency, determined by the -3dB point relative to a very low frequency value (< 10 kHz), is related to the current IVFP injected into pin IFP by the following formulas.

SSI 32F8011
Fc (ideal, in MHz) = 16.25•IFP = 16.25•IVFP•2.2/VR

SSI 32F8012
Fc (ideal, in MHz) = 18.75•IFP = 18.75•IVFP•2.2/VR
where IFP and IVFP are in mA, 0.31<IFP<0.8 mA, and VR is in volts.

If a current source is used to inject current into pin IFP, pin VFP should be left open.

If the 32F8011/8012 cutoff frequency is set using voltage VR to bias up a resistor tied to pin VFP, the cutoff frequency is related to the resistor value by the following formulas.

SSI 32F8011
Fc (ideal, in MHz) = 16.25•IFP = 16.25•2.2/(3•Rx)

SSI 32F8012
Fc (ideal, in MHz) = 18.75•IFP = 18.75•2.2/(3•Rx)
where Rx is in kΩ, 0.917<Rx<2.366 kΩ.

If pin VFP is used to program cutoff frequency, pin IFP should be left open.

### SLIMMER HIGH FREQUENCY BOOST PROGRAMMING

The amplitude of the output signal at frequencies near the cutoff frequency can be increased using this feature. Applying an external voltage to pin VBP which is proportional to reference output voltage VR (provided by the VR pin) will set the amount of boost. A fixed amount of boost can be set by an external resistor divider network connected from pin VBP to pins VR and GND. No boost is applied if pin FBST, frequency boost enable, is at a low logic level.

The amount of boost FB at the cutoff frequency Fc is related to the voltage VBP by the formula

FB (ideal, in dB) = $20 \log_{10}[1.884(VBP/VR)+1]$, where 0<VBP<VR.

## PIN DESCRIPTION

| NAME | DESCRIPTION |
|---|---|
| VIN+, VIN- | DIFFERENTIAL SIGNAL INPUTS. The input signals must be AC coupled to these pins. |
| VO_NORM+, VO_NORM- | DIFFERENTIAL NORMAL OUTPUTS. The output signals must be AC coupled. |
| VO_DIFF+, VO_DIFF- | DIFFERENTIAL DIFFERENTIATED OUTPUTS. For minimum time skew, these outputs should be AC coupled to the pulse detector. |
| IFP | FREQUENCY PROGRAM INPUT. The filter cutoff frequency FC, is set by an external current IFP, injected into this pin. IFP must be proportional to voltage VR. This current can be set with an external current generator such as a DAC. VFP should be left open when using this pin. |
| VFP | FREQUENCY PROGRAM INPUT. The filter cutoff frequency can be set by programming a current through a resistor from VR to this pin. IFP should be left open when using this pin. |
| VBP | FREQUENCY BOOST PROGRAM INPUT. The high frequency boost is set by an external voltage applied to this pin. VBP must be proportional to voltage VR. A fixed amount of boost can be set by an external resistor divider network connected from VBP to VR and GND. No boost is applied if the FBST pin is grounded, or at logic low. |
| FBST | FREQUENCY BOOST. A high logic level or open input enables the frequency boost circuitry. |
| PWRON | POWER ON. A high logic level or open circuit enables the chip. A low level puts the chip in a low power state. |
| VR | REFERENCE VOLTAGE. Internally generated reference voltage. |
| VCC1, VCC2 | +5 VOLT SUPPLY. |
| GND1, GND2 | GROUND |

## ELECTRICAL SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may damage the device.

| PARAMETER | RATINGS | UNIT |
|---|---|---|
| Storage Temperature | -65 to +150 | °C |
| Junction Operating Temperature, Tj | +130 | °C |
| Supply Voltage, VCC1, VCC2 | -0.5 to 7 | V |
| Voltage Applied to Inputs | -0.5 to VCC + 0.5 | V |
| IFP, VFP Inputs Maximum Current* | ≤1.2 | mA |

* Exceeding this current may cause frequency programming lockup.

### RECOMMENDED OPERATING CONDITIONS

| PARAMETER | RATINGS | UNIT |
|---|---|---|
| Supply voltage, VCC1, VCC2 | 4.5 < VCC1,2 < 5.50 | V |
| Ambient Temperature | 0 < Ta < 70 | °C |

## ELECTRICAL CHARACTERISTICS

**Power Supply Characteristics** (Unless otherwise specified, recommended operating conditions apply.)

| PARAMETER | | CONDITIONS | | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| ICC | Power Supply Current | PWRON ≤ 0.8V | VBP = VR | | 14 | 17 | mA |
| | | | VBP = 0V | | 12 | 15 | mA |
| ICC | Power Supply Current | PWRON ≥ 2.0V | | | 67 | 80 | mA |

**DC Characteristics**

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|---|
| VIH | High Level Input Voltage | TTL input | 2.0 | | VCC+0.3 | V |
| VIL | Low Level Input Voltage | | -0.3 | | 0.8 | V |
| IIH | High Level Input Current | VIH = 2.7V | | | 20 | µA |
| IIL | Low Level Input Current | VIL = 0.4V | | | –1.5 | mA |

**Filter Characteristics**

| PARAMETER | | CONDITIONS | | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| FCA | Filter *fc* Accuracy | using VFP pin<br>Rx = 0.917 kΩ | 32F8011<br>32F8012 | 11.7<br>13.5 | | 14.3<br>16.5 | MHz<br>MHz |
| AO | VO_NORM Diff Gain | F = 0.67 *fc*, FB = 0 dB | | 0.8 | | 1.20 | V/V |
| AD | VO_DIFF Diff Gain | F = 0.67 *fc*, FB = 0 dB | | 0.8AO | | 1.0AO | V/V |
| FBA | Frequency Boost Accuracy | VBP = VR @ *fc* = 5 MHz | | 8.5 | 9.5 | 10.5 | dB |
| TGD0 | Group Delay Variation Without Boost* | *fc* = Max *fc*, VBP = 0V<br>F = 0.2 *fc* to *fc* | | –0.75 | | +0.75 | ns |
| TGDB | Group Delay Variation With Boost* | *fc* = Max *fc*, VBP = VR<br>F = 0.2 *fc* to *fc* | | –0.75 | | +0.75 | ns |
| VIF | Filter Input Dynamic Range | THD = 1% max, F = 0.67 *fc*<br>(no boost) | | 1.5 | | | Vpp |
| VOF | Filter Output Dynamic Range | THD = 1% max, F = 0.67 *fc* | | 1.5 | | | Vpp |
| RIN | Filter Diff Input Resistance | | | 3.0 | 3.8 | | kΩ |
| CIN | Filter Diff Input Capacitance* | | | | 2.5 | 7 | pF |
| EOUT | Output Noise Voltage* Differentiated Output | BW = 100 MHz, Rs = 50Ω,<br>I*fp* = 0.8 mA, VBP = 0.0V | | | 5.5 | 6.8 | mVRms |
| EOUT | Output Noise Voltage* Normal Output | BW = 100 MHz, Rs = 50Ω<br>I*fp* = 0.8 mA, VBP = 0.0V | | | 2.75 | 3.6 | mVRms |
| EOUT | Output Noise Voltage* Differentiated Output | BW = 100 MHz, Rs = 50Ω<br>I*fp* = 0.8 mA, VBP = VR | | | 6.0 | 8.1 | mVRms |
| EOUT | Output Noise Voltage* Normal Output | BW = 100 MHz, Rs = 50Ω<br>I*fp* = 0.8 mA, VBP = VR | | | 3.25 | 4.4 | mVRms |

* Not directly testable in production, design characteristic.

**ELECTRICAL CHARACTERISTICS** (continued)

**Filter Characteristics** (continued)

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|---|
| IO– | Filter Output Sink Current | | 1.0 | | | mA |
| IO+ | Filter Output Source Current | | 2.0 | | | mA |
| RO | Filter Output Resistance Single ended | Source Current (IO+) = 1 mA | | | 60 | Ω |

**Filter Control Characteristics**

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|---|
| VR | Reference Voltage Output | | 2.0 | | 2.40 | V |
| $I_{VR}$ | Reference Output Source Current | | | | 2.0 | mA |

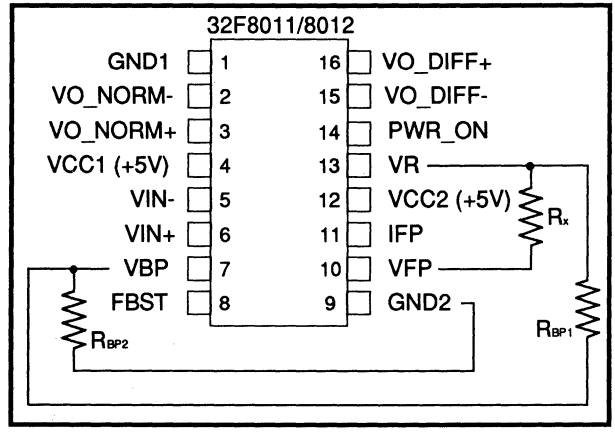



**FIGURE 1: 32F8011/8012 Applications Setup, 16-Pin SO or DIP**

VR = 2.2V

VFP = 0.667 VR

IVfp = 0.33VR/Rx

IVfp range: 0.31 mA to 0.8 mA
(5 MHz to 13 MHz for SSI 32F8011)
(6 MHz to 15 MHz for SSI 32F8012)

VFP is used when programming current is set with a resistor from VR. When VFP is used IFP must be left open.

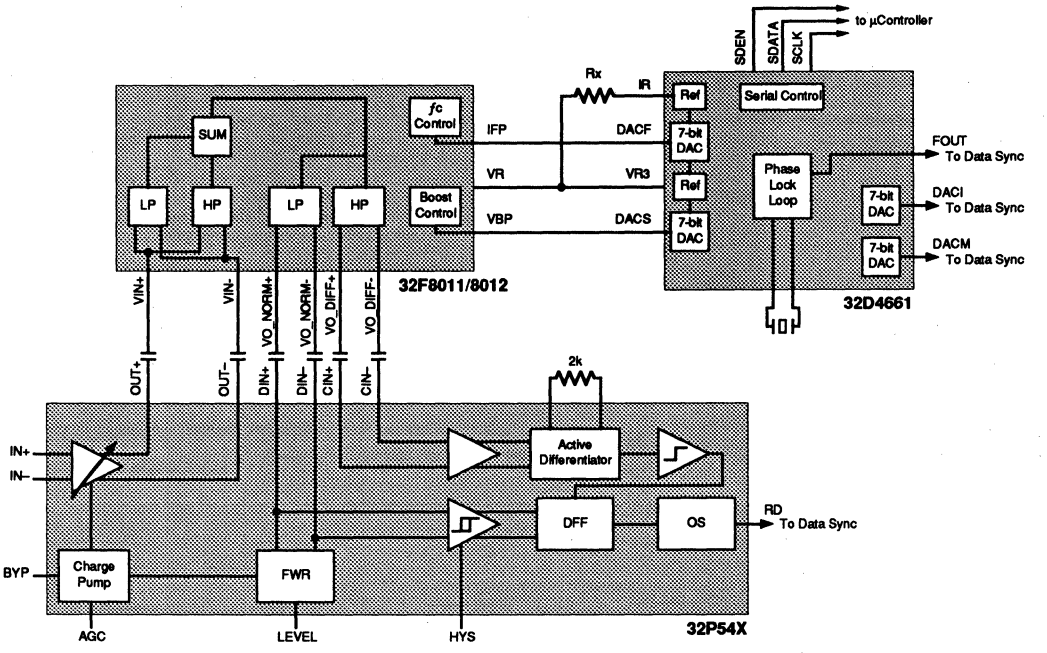



**FIGURE 2: Applications Setup, Constant Density Recording**
**32F8011/8012, 32P54X, 32D4661**

IOF = DACF output current

IOF = (0.98F•VR)/127Rx

Rx = (0.98F•VR)/127IOF

Rx = current reference setting resistor

VR = Voltage Reference = 2.2V

F = DAC setting: 0-127

Full scale, F = 127

For range of Max $f_c$ then IFP = 0.8 mA

Therefore, for Max programming current range to 0.8 mA:

Rx = (0.98)(2.2/0.8) = 2.7 kΩ

Please note that in setups such as this where IFP is used for cutoff frequency programming VFP must be left open.

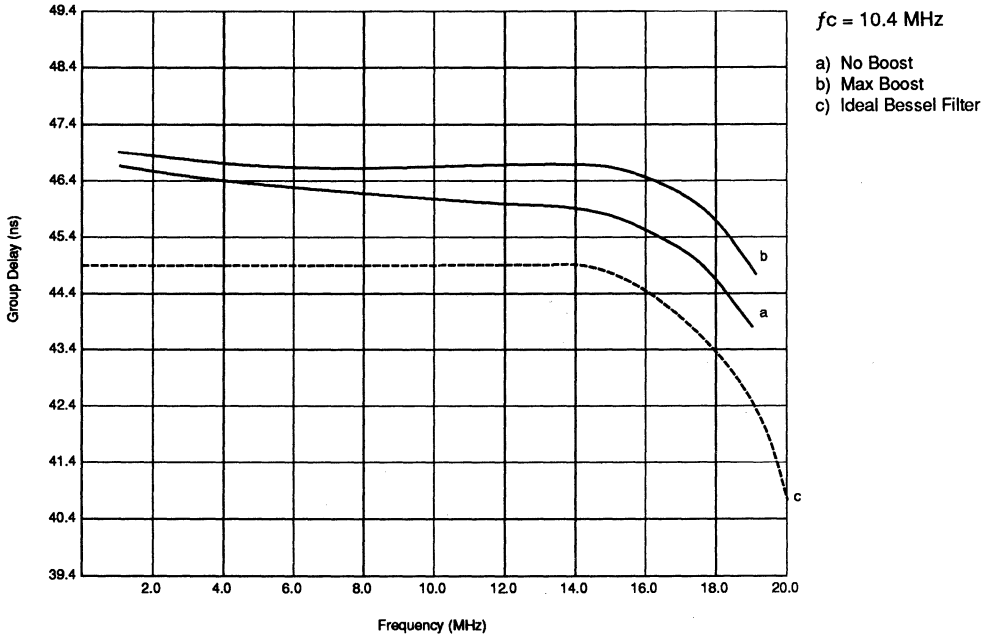



**FIGURE 3: 32F8011/8012 Typical Group Delay Variation (Differentiated Output)**

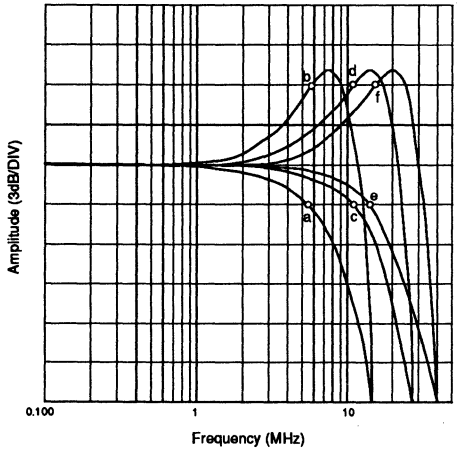



**FIGURE 4: 32F8011/8012 Normal Low Pass Output Response (VO_NORM)**

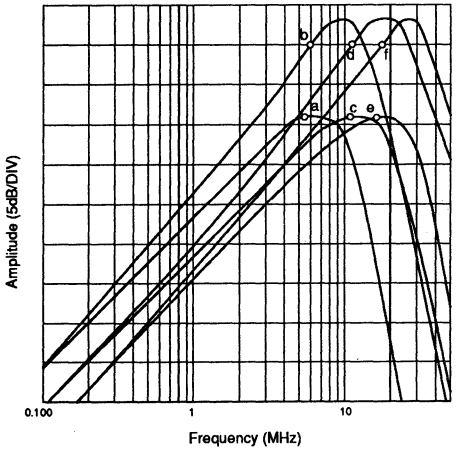
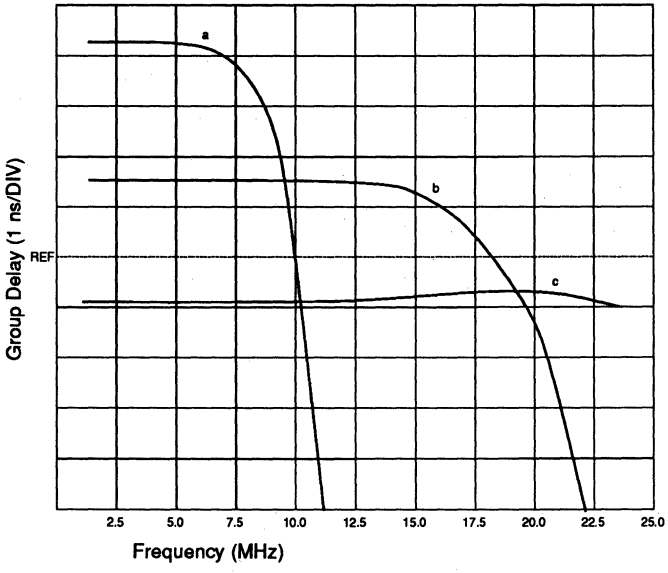


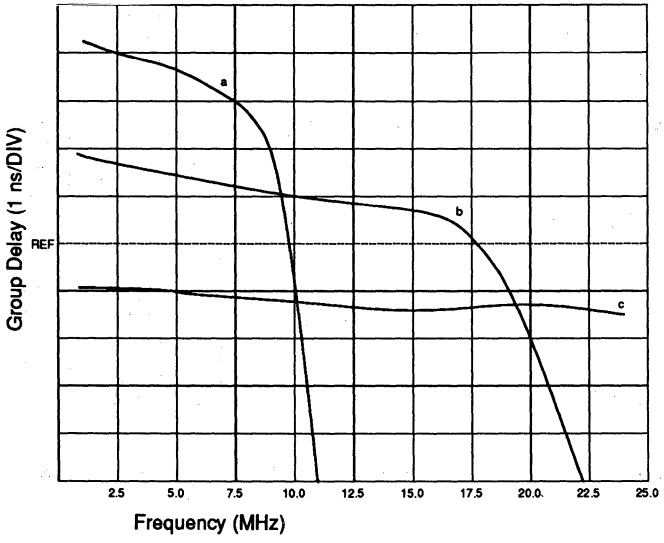

**FIGURE 5: 32F8011/8012 Differented Low Pass Output Response (VO_DIFF)**

a) $fc$ = 5 MHz No Boost
b) $fc$ = 5 MHz Max Boost
c) $fc$ = 10 MHz No Boost
d) $fc$ = 10 MHz Max Boost
e) $fc$ = 15 MHz No Boost
f) $fc$ = 15 MHz Max Boost



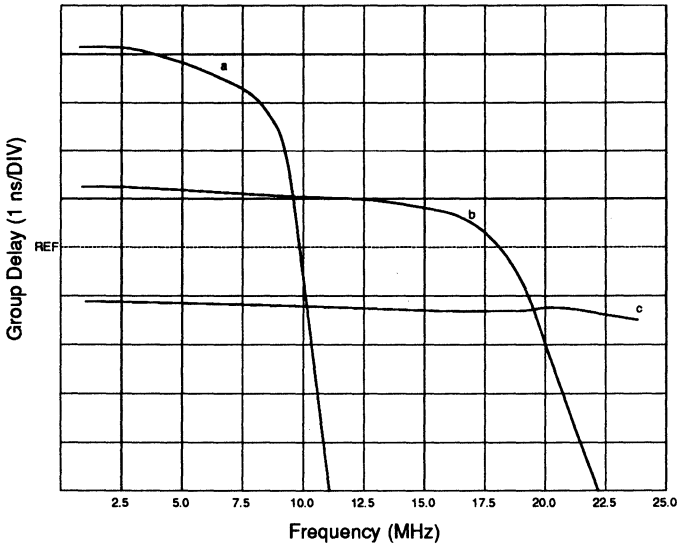

a) $fc$ = 5 MHz (Ref = 80 ns)
b) $fc$ = 10 MHz (Ref = 45 ns)
c) $fc$ = 15 MHz (Ref = 35 ns)

**FIGURE 6: 32F8011/8012 Typical Group Delay Variation (Differentiated Output) Maximum Boost**



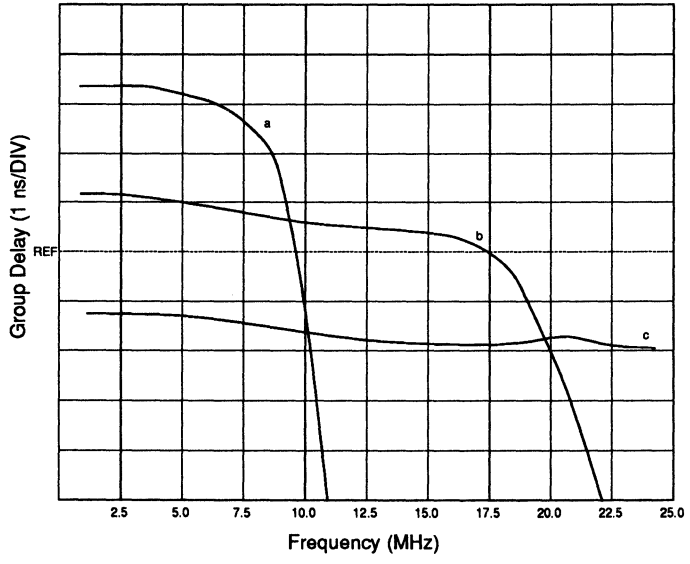

a) $fc$ = 5 MHz (Ref = 80 ns)
b) $fc$ = 10 MHz (Ref = 45 ns)
c) $fc$ = 15 MHz (Ref = 35 ns)

**FIGURE 7: 32F8011/8012 Typical Group Delay Variation (Differentiated Output) No Boost**



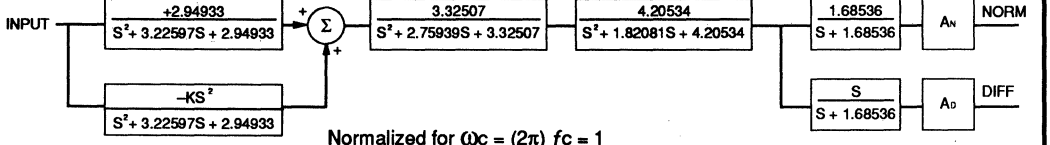

a) $fc$ = 5 MHz (Ref = 80 ns)
b) $fc$ = 10 MHz (Ref = 45 ns)
c) $fc$ = 15 MHz (Ref = 35 ns)

**FIGURE 8: 32F8011/8012 Typical Group Delay Variation (Normal Low Pass Output) Maximum Boost**




a) $fc$ = 5 MHz (Ref = 80 ns)
b) $fc$ = 10 MHz (Ref = 45 ns)
c) $fc$ = 15 MHz (Ref = 35 ns)

**FIGURE 9: 32F8011/8012 Typical Group Delay Variation (Normal Low Pass Output) No Boost**




Normalized for $\omega c = (2\pi)\ fc = 1$
AN and AD are adjusted for unity gain (0 dB) at $F = 0.67\ fc$
Denormalize the frequency by substituting $S \rightarrow (S/2\pi fc)$
Eq for $fc$ = 13 MHz, $S = S / [(2\pi)(13 \cdot 10^6)] = S / 8.16814^7$

**FIGURE 12: 32F8011/8012 Normalized Block Diagram**

**TABLE 1: 32F8011/8012 Frequency Boost Calculations**

Assuming 9.2 dB boost for VBP = VR

$$\frac{VBP}{VR} \cong \frac{\left(10^{(FB/20)}\right) - 1}{1.884}$$

| Boost | K | VBP/VR | Boost | K | VBP/VR |
|---|---|---|---|---|---|
| 1 dB | 0.36 | 0.065 | 6 dB | 2.94 | 0.528 |
| 2 dB | 0.76 | 0.137 | 7 dB | 3.65 | 0.658 |
| 3 dB | 1.22 | 0.219 | 8 dB | 4.46 | 0.802 |
| 4 dB | 1.73 | 0.310 | 9 dB | 5.36 | 0.965 |
| 5 dB | 2.30 | 0.413 | | | |

**or,**

$$\text{boost in dB} \cong 20 \log \left[1.884 \left(\frac{VBP}{VR}\right) + 1\right]$$

| VBP/VR | Boost | VBP/VR | Boost |
|---|---|---|---|
| 0.1 | 1.499 dB | 0.6 | 6.569 dB |
| 0.2 | 2.777 dB | 0.7 | 7.305 dB |
| 0.3 | 3.891 dB | 0.8 | 7.984 dB |
| 0.4 | 4.879 dB | 0.9 | 8.613 dB |
| 0.5 | 5.765 dB | 1.0 | 9.200 dB |

**TABLE 2: Calculations**

Typical change in $f$-3 dB point with boost

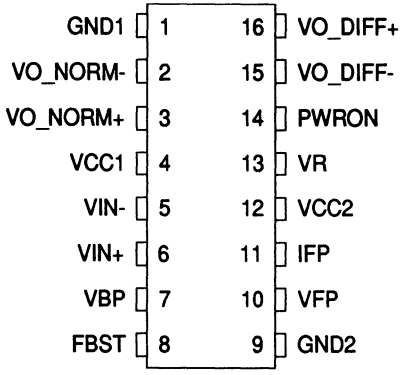
| Boost (dB) | Gain @ $fc$ (dB) | Gain @ peak (dB) | fpeak/$fc$ | f-3dB/$fc$ |
|---|---|---|---|---|
| 0 | -3 | 0.00 | no peak | 1.00 |
| 1 | -2 | 0.00 | no peak | 1.20 |
| 2 | -1 | 0.00 | no peak | 1.47 |
| 3 | 0 | 0.15 | 0.62 | 1.74 |
| 4 | 1 | 1.00 | 1.08 | 1.96 |
| 5 | 2 | 2.12 | 1.24 | 2.13 |
| 6 | 3 | 3.35 | 1.24 | 2.28 |
| 7 | 4 | 4.56 | 1.39 | 2.42 |
| 8 | 5 | 5.82 | 1.39 | 2.54 |
| 9 | 6 | 7.04 | 1.39 | 2.66 |

Notes: 1. $fc$ is the original programmed cutoff frequency with no boost
2. $f$-3 dB is the new -3 dB value with boost implemented
3. fpeak is the frequency where the magnitude peaks with boost implemented

i.e., $fc$ = 13 MHz when boost = 0 dB
if boost is programmed to 5 dB then f-3 dB = 27.69 MHz, fpeak = 16.12 MHz

## PIN DIAGRAM

(Top View)




**16-pin SON, SOL**

**Thermal Characteristics: θjA**

| | |
|---|---|
| 16-lead SON (150 mil) | 105° C/W |
| 16-lead SOL (300 mil) | 100° C/W |

## ORDERING INFORMATION

| PART DESCRIPTION | ORDER NO. | PKG. MARK |
|---|---|---|
| SSI 32F8011 | | |
| 16-lead SON (150 mil) | 32F8011-CN | 32F8011-CN |
| 16-lead SOL (300 mil) | 32F8011-CL | 32F8011-CL |
| SSI 32F8012 | | |
| 16-lead SON (150 mil) | 32F8012-CN | 32F8012-CN |
| 16-lead SOL (300 mil) | 32F8012-CL | 32F8012-CL |



Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 573-6000, FAX (714) 573-6914

**Notes:**

silicon systems®
A TDK Group Company

# SSI 32F8020A/8022A/8021/8023
## Low-Power Programmable Electronic Filter
## Preliminary Data

January 1993

3

## DESCRIPTION

The SSI 32F8020A/8022A Programmable Electronic Filter provides an electronically controlled low–pass filter with a separate differentiated low–pass output. A seven–pole, .05° Equiripple-type linear phase, low–pass filter is provided along with a single-pole, single-zero differentiator. Both outputs have matched delays. The delay matching is unaffected by any amount of programmed equalization or bandwidth. The SSI 32F8021/8023 does not have differentiated outputs. This programability combined with low group delay variation makes the SSI 32F8020A/8022A/8021/8023 ideal for use in constant density recording applications. Double differentiation pulse slimming equalization is accomplished by a two–pole, low–pass with a two–pole, high–pass feed forward section to provide complimentary real axis zeros. A variable attenuator is used to program the zero locations.

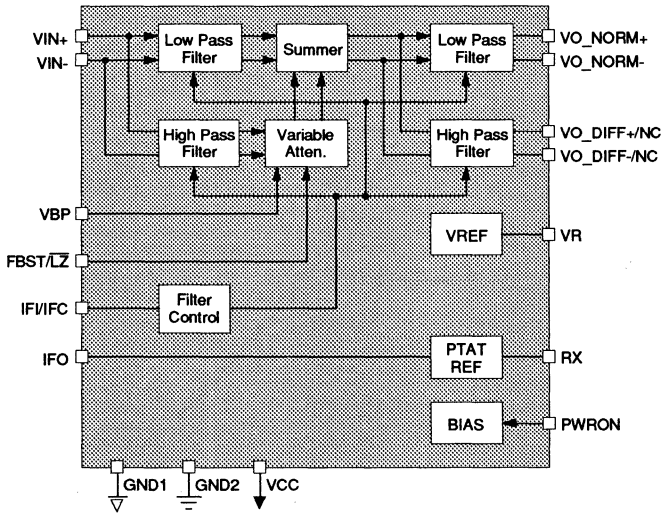
The SSI 32F8020A/8022A programmable equalization and bandwidth characteristics can be controlled by external DACs or DACs provided in the SSI 32D4661

(continued)

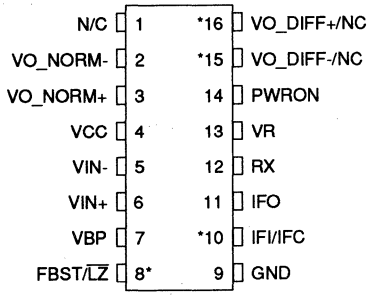
## FEATURES

- **Ideal for constant density recording applications**
- **Programmable filter cutoff frequency ($fc$ = 1.5 to 8 MHz)**
- **Programmable pulse slimming equalization (0 to 9 dB boost at the filter cutoff frequency)**
- **Matched normal and differentiated low-pass outputs (SSI 32F8020A/8022A)**
- **Differential filter input and outputs**
- **±10% cutoff frequency accuracy**
- **±2% maximum group delay variation from 1.5 - 8 MHz**
- **Total harmonic distortion less than 1%**
- **No external filter components required**
- **+5V only operation**
- **16-pin SON and SOL package**

## BLOCK DIAGRAM




## PIN DIAGRAM




* Pin 8 = FBST - SSI 32F8020A/8021
LZ - SSI 32F8022A/8023

* Pin 10 = IFI - SSI 32F8020A/8022A
IFC - SSI 32F8021/8023

* Pin 15 & 16 = VO_DIFF - SSI 32F8020A/8022A
N/C - SSI 32F8021/8023

## DESCRIPTION (continued)

SSI 32D4661 time base generator. Fixed characteristics are easily accomplished with three external resistors. External DACs are required for the SSI 32F8021/8023 to program the cutoff frequency. For the SSI 32F8020A/8021, equalization can be switched in or out by a logic signal. The input impedance of the SSI 32F8020A/8023 can be clamped low for fast recovery from input overload.

The SSI 32F8020A/8022A/8021/8023 require only a +5V supply and are available in 16-Lead SON and SOL packages.

## FUNCTIONAL DESCRIPTION

The SSI 32F8020A/8022A/8021/8023 is a high performance programmable electronic filter. It features a 7-pole 0.05° phase equiripple filter with matched normal and differentiated outputs. The device has been optimized for usage with several Silicon Systems products, including the SSI 32D4661 Time Base Generator, the SSI 32P54X family pulse detectors, and the SSI 32P4720 combo chip (Data Separator and Pulse Detector).

### CUTOFF FREQUENCY PROGRAMMING

The cutoff frequency, $fc$, of the SSI 32F8020A/8022A is defined as the -3dB filter bandwidth with no magnitude equalization applied, and is programmable from 1.5 MHz to 8 MHz.

The cutoff frequency is programmable with 3 pins: RX, IFO and IFI. At the RX pin, an external resistor to ground establishes a reference current:

$$IFO = \frac{0.75}{RX} \text{ at } T = 27°C$$

IFI should be made proportional to IFO for temperature stability. The cutoff frequency is related to the RX resistor, IFO and IFI currents as follows:

$$fc(MHz) = 8x\frac{IFI}{IFO}x\frac{1.25}{Rx(k\Omega)}$$

For a fixed cutoff frequency setting, IFO and IFI can be tied together. The cutoff frequency equation then reduces to:

$$fc(MHz) = 8x\frac{1.25}{Rx(k\Omega)}$$

For programmable cutoff frequency, an external current DAC can be used. The IFO should be the reference current into the DAC. The DAC output current drives IFI, which is then proportional to IFO. The DACF in the SSI 32D4661 Time Base Generator is designed to control $fc$ of the Silicon Systems programmable filters. When the DACF, which has a 4X current from its reference to full scale output is used, a 5-kΩ RX is used. The $fc$ is then given as follows:

$$fc(MHz) = 8x\frac{F\_Code}{127}$$

where F_Code is the decimal code equivalent to the 7-bit digital input for the DACF. The cutoff frequency programming for the SSI 32F8021/8023 is shown in Figure 3.

### MAGNITUDE EQUALIZATION PROGRAMMING

The magnitude equalization, measured in dB, is the amount of high frequency peaking at the cutoff frequency relative to the original -3 dB point. For example, when 9 dB boost is applied, the magnitude response peaks up 6 dB above the DC gain.

The magnitude equalization is programmable with two pins: VR and VBP. The VR is a bandgap reference voltage, 2.2V typically. The voltage at the VBP pin determines the amount of high frequency boost. The boost function is as follows:

$$Boost(dB) = 20\log_{10}[1.884(\frac{VBP}{VR}) + 1]$$

For a fixed boost setting, a resistor divider between VR to ground can be used with the divided voltage at the VBP pin. For programmable equalization, an external voltage DAC can be used. VR should be the reference voltage to the DAC. The DAC output voltage is then proportional to VR. The DACS in the SSI 32D4661 is designed to control the magnitude equalization of Silicon Systems programmable filters. When DACS is used, the boost relation then reduces to:

$$Boost(dB) = 20\log_{10}[1.884(\frac{S\_Code}{127}) + 1]$$

where S_Code is the decimal code equivalent to the 7-bit digital input for the DACS.

For the SSI 32F8020A/8021, the equalization function can be disabled when FBST is pulled to logic 0. For the SSI 32F8022A/8023, the VBP pin should be grounded to achieve 0 dB boost.

**LOW INPUT IMPEDANCE (SSI 32F8022A/8023 only)**

When the LZ is at logic 1 or left open, the SSI 32F8022A/8023 input is at high impedance state. When the LZ is pulled to logic 0, the SSI 32F8022A/8023 input is clamped to a low impedance state, 200 Ω typical.

**POWER ON/OFF**

The SSI 32F8020A/8022A/8021/8023 support a power down mode for minimal idle dissipation. When PWRON is pulled up to logic 1, the device is in normal operation mode. When PWRON is pulled down to logic 0, or left open, the device is in the power down mode.

## PIN DESCRIPTION

| NAME | DESCRIPTION |
|---|---|
| VIN+, VIN- | DIFFERENTIAL SIGNAL INPUTS. |
| VO_NORM+, VO_NORM- | DIFFERENTIAL NORMAL OUTPUTS. |
| VO_DIFF+ VO_DIFF- | DIFFERENTIAL DIFFERENTIATED OUTPUTS. |
| RX | PTAT REFERENCE CURRENT SET. PTAT (proportional to absolute temperature) reference current IFO is equivalent to the current set on this pin. |
| IFO | PTAT CURRENT REFERENCE OUTPUT. This pin ouputs a PTAT reference current which is externally scaled for control input into IFI. |
| IFI | FREQUENCY PROGRAM INPUT. The filter cutoff frequency $fc$, is set by an external current IFI, injected into this pin. IFI must be proportional to current IFO. This current can be set with an external current generator such as a DAC, referenced to IFO. |
| VBP | FREQUENCY BOOST PROGRAM INPUT. The slimmer high frequency boost is set by an external voltage applied to this pin. VBP must be proportional to voltage VR. A fixed amount of boost can be set by an external resistor divider network connected from VBP to VR and GND. No boost is applied if the FBST pin is grounded, or at logic low. |
| FBST (32F8020A/8021) | FREQUENCY BOOST. A high logic level or open input enables the frequency boost circuitry. No boost is applied if the FBST pin is grounded, or at logic low. |
| $\overline{LZ}$ (32F8022A /8023) | LOW IMPEDANCE MODE. With a low logic level, the analog input impedance is switched low for fast recovery from input overload. With a high logic level or left open, the input is at high impedance state. |
| PWRON | POWER ON. A high logic level circuit enables the chip. A low level puts the chip in a low power state. A low or open circuit disables the chip. |
| VR | REFERENCE VOLTAGE. Internally generated reference voltage. |
| VCC | +5 VOLT SUPPLY. |
| GND | GROUND |

## ELECTRICAL SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may damage the device.

| PARAMETER | RATING |
|---|---|
| Storage Temperature | -65 to +150 °C |
| Junction Operating Temperature, Tj | +130 °C |
| Supply Voltage, VCC | -0.5 to 7V |
| Voltage Applied to Inputs | -0.5 to VCCV |
| Maximum Power Dissipation, *fc* = 8 MHz, Vcc = 5.5V | 226 mW |

### RECOMMENDED OPERATING CONDITIONS

| | |
|---|---|
| Supply voltage, VCC | 4.50 < VCC < 5.50V |
| Ambient Temperature | 0 < Ta < 70 °C |

### Power Supply Characteristics

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| ICC | Power Supply Current | PWRON ≤ 0.8V | | | 0.5 | mA |
| | | PWRON ≥ 2.2V<br>SSI 32F8021/8023 | | 26 | 32 | mA |
| | | PWRON ≥ 2.2V<br>SSI 32F8020A/8022A | | 35 | 41 | mA |
| PD | Power Dissipation | PWRON ≤ 0.8V | | | 3 | mW |
| | | PWRON ≥ 2.2V, VCC = 5V<br>SSI 32F8021/8023 | | 130 | 160 | mW |
| | | PWRON ≥ 2.2V, VCC = 5.5V<br>SSI 32F8021/8023 | | 143 | 176 | mW |
| | | PWRON ≥ 2.2V, VCC = 5V<br>SSI 32F8020A/8022A | | 175 | 205 | mW |
| | | PWRON ≥ 2.2V, VCC = 5.5V<br>SSI 32F8020A/8022A | | 193 | 226 | mW |

**DC Characteristics**

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| VIH | High Level Input Voltage | TTL input | 2.0 | | | V |
| VIL | Low Level Input Voltage | | | | 0.8 | V |
| IIH | High Level Input Current | VIH = 2.7V | | | 20 | µA |
| IIL | Low Level Input Current | VIL = 0.4V | | | –1.5 | mA |
| VICM | VIN± Input Common Mode Voltage | | (VCC -1.6) -0.25 | | (VCC -1.6) +0.25 | V |
| VOCM | VO_NORM± Output Common Mode Voltage | | 1.8 | | 3.8 | V |
| VOFF | VO_NORM± Output Offset | VIN± open | -0.15 | | +0.25 | V |

**Filter Characteristics**

| | | | | | | |
|---|---|---|---|---|---|---|
| $fc$ | Filter Cutoff Frequency | Rx = 5kΩ<br>$fc\ (MHz) = 8 \cdot \frac{IFI}{4 \cdot IFO}$<br>(32F8020A/8022A)<br>$fc\ (MHz) = 8 \cdot \frac{IFC}{4 \cdot IFO}$<br>(32F8021/8023) | 1.5 | | 8.0 | MHz |
| FCA | Filter $fc$ Accuracy | $fc$ (nominal) = 8 MHz | –10 | | +10 | % |
| AO | VO_NORM Diff Gain | F = 0.67 $fc$, FB = 0 dB | 0.8 | 0.9 | 1.0 | V/V |
| AD | VO_DIFF Diff Gain (32F8020A/8022A) | F = 0.67 $fc$, FB = 0 dB | 0.8AO | | 1.2AO | V/V |
| FB | Frequency Boost at $fc$ | $FB(db)=20 \log\left[1.884\left(\frac{VBP}{VR}\right)+1\right]$<br>VBP = VR | | 9.2 | | dB |
| FBA | Frequency Boost Accuracy | FB (ideal) = 9.0 dB | –1 | | +1 | dB |
| TGD0 | Group Delay Variation Without Boost | $fc$ = 8 MHz, VBP = 0V<br>F = 0.2 $fc$ to 1.75 $fc$ | –1.3 | | +1.3 | ns |
| | | $fc$ = 1.5 MHz - 8 MHz<br>F = 0.2 $fc$ to 1.75 $fc$, VBP = 0V | –2 | | +2 | % |
| TGDB | Group Delay Variation With Boost | $fc$ = 8 MHz, VBP = VR<br>F = 0.2 $fc$ to 1.75 $fc$ | –1.3 | | +1.3 | ns |
| | | $fc$ = 1.5 MHz - 8 MHz<br>F = 0.2 $fc$ to 1.75 $fc$, VBP = VR | –2 | | +2 | % |
| VIF | Filter Input Dynamic Range | THD = 1% max, F = 0.67 $fc$ | 1.0 | | | Vpp |

## ELECTRICAL SPECIFICATIONS (continued)

### Filter Characteristics (continued)

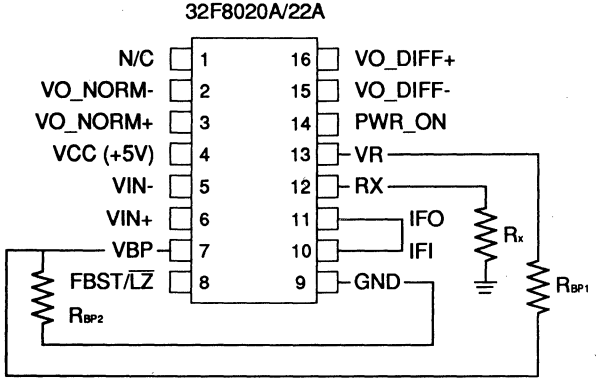
| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| VOF Filter Output Dynamic Range | THD = 1% max, F = 0.67 *fc* | 1.0 | | | Vpp |
| VIF Filter Input Dynamic Range | THD = 1.5%, F = 0.67 *fc* | 1.5 | | | Vpp |
| VOF Filter Output Dynamic Range | THD = 1.5%, F = 0.67 *fc* | 1.5 | | | Vpp |
| VIF Filter Input Dynamic Range | THD = 3% max, F = 0.67 *fc* | 2.0 | | | Vpp |
| VOF Filter Output Dynamic Range | THD = 3% max, F = 0.67 *fc* | 2.0 | | | Vpp |
| RIN Filter Diff Input Resistance | 32F8020A/8021<br>32F8022A/8023 LZ = 1 or open | 3.0 | 4.0 | | kΩ |
| | 32F8022A/8023 LZ = 0 | | 200 | 400 | Ω |
| CIN Filter Input Capacitance | | | | 7 | pF |
| EOUT Output Noise Voltage Differentiated Output | BW = 100 MHz, Rs = 50Ω<br>*fc* = 8 MHz, VBP = 0.0V<br>(32F8020A/8022A) | | 6.3 | 7.5 | mVRms |
| EOUT Output Noise Voltage Normal Output | BW = 100 MHz, Rs = 50Ω<br>*fc* = 8 MHz, VBP = 0.0V | | 2.7 | 4.0 | mVRms |
| EOUT Output Noise Voltage Differentiated Output | BW = 100 MHz, Rs = 50Ω<br>*fc* = 8 MHz, VBP = VR<br>(32F8020A/8020A) | | 9.4 | 11.0 | mVRms |
| EOUT Output Noise Voltage Normal Output | BW = 100 MHz, Rs = 50Ω<br>*fc* = 8 MHz, VBP = VR | | 3.7 | 4.5 | mVRms |
| IO– Filter Output Sink Current | | 1.0 | | | mA |
| IO+ Filter Output Source Current | | 2.0 | | | mA |
| RO Filter Output Resistance (Single ended) | IO+ = 1.0 mA | | | 60 | Ω |

### Filter Control Characteristics

| | | | | | |
|---|---|---|---|---|---|
| VR Reference Voltage | | 2.0 | | 2.40 | V |
| VBP Frequency Boost Control Voltage Range | VR = 2.2V<br>FBOOST = 0 to 9.2 dB | 0 | | 2.2 | V |
| VRX PTAT Reference Current Set Output Voltage | TA = 25°C<br>IRX = 0 - 0.6 mA<br>Rx > 1.25 kΩ | | 750 | | mV |
| IFO PTAT Reference Current, Output Current Range | TA = 25°C<br>1.25 kΩ < Rx < 6.8 kΩ<br>IFO = VRX/Rx<br>VRX = 750 mV | 0.11 | | 0.6 | mA |
| RIFO IFO Output Impedance | | 50 | | | kΩ |
| VIFO IFO Voltage Compliance | | 0 | | Vcc -1 | V |

**Filter Control Characteristics**

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| IFI | PTAT Programming Current Range | TA = 25°C, VRX = 750 mV 32F8020A/8022A | 0.11 | | 0.6 | mA |
| RIFI | IFI Input Impedance | 32F8020A/8022A | 1.0 | | 2.5 | kΩ |
| VIFI | IFI Voltage Compliance | 32F8020A/8022A | 0.5 | | 2.5 | V |
| IFC | PTAT Programming Current Range | TA = 25 °C, VRX = 750 mV 32F8021/8023 | 0.11 | | 0.6 | mA |
| TPWR | Power On Recovery Time | DC voltages within 20 mV of final values | | | 300 | ns |
| TBST | Boost Change Recovery | DC voltages within 20 mV of final values | | | 300 | ns |
| TFBW | Bandwidth Change Recovery | DC voltages within 20 mV of final values | | | 300 | ns |




VR = 2.2V

VRX = 750 mV @25°C

IFO = $V_{RX}/R_X$

IFI range: 0.11 mA to 0.60 mA @25°C

(1.5 to 8 MHz NO BOOST)

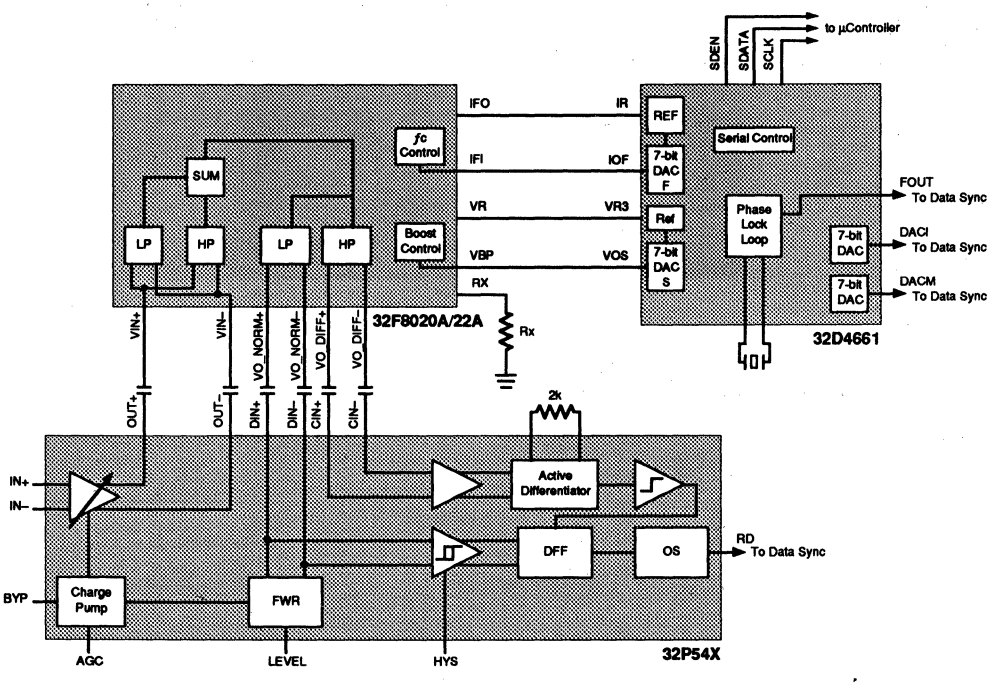
Fixed frequency programming is accomplished as shown in the drawing above. In this case IFI (programming current) is equivalent to IFO (reference current). Programming current is then set by $V_{RX}/R_X$.

where: $fc$ = 8.0 MHz then

IFI = IFO = 0.60 mA @25 °C

Rx = 750 mV/0.60 mA = 1.25 kΩ

**FIGURE 1: 32F8020A/8022A Applications Setup**




VR = 2.2V

VRX = 750 mV @25°C

IFO = VRX/Rx

IFI range: 0.11 mA to 0.60 mA @25°C

(1.5 to 8 MHz NO BOOST)

In this case the IFI (programming current) is scaled from IFO (reference current) through DACF on the 32D4661. DACF has a current gain of 4; therefore, the reference current should be set to 25% of the maximum desired IFI (programming current).

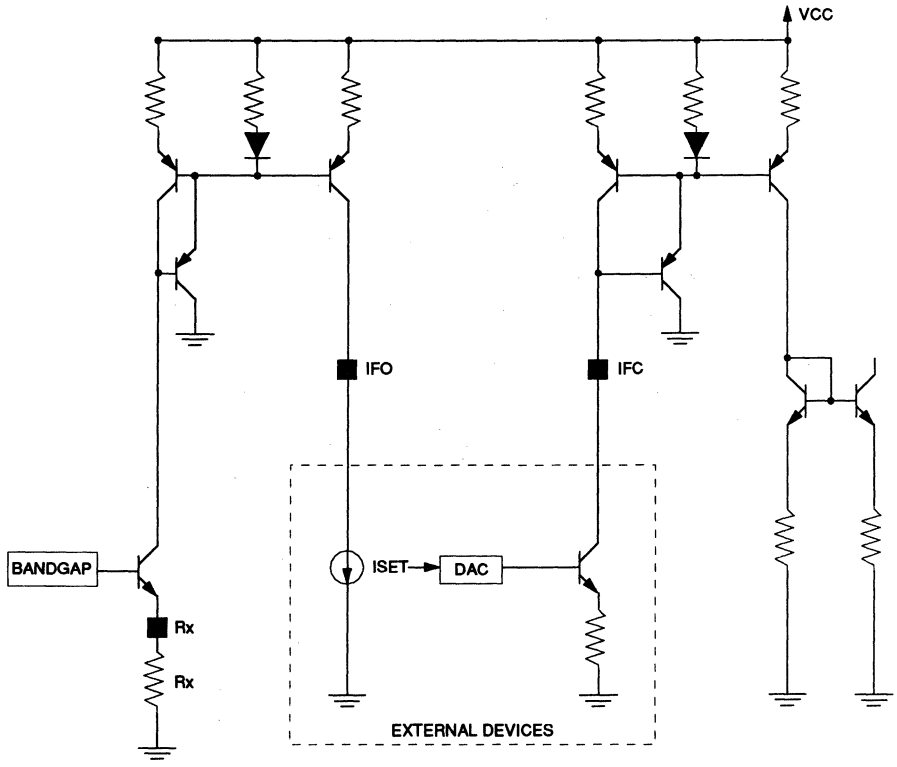
where: *fc* (max) = 8.0 MHZ then

IFI (max) = 0.60 mA @25°C

IFO (max) = 0.15 mA

therefore Rx = 750 mV/0.15 mA = 5 kΩ

**FIGURE 2: Applications Setup, Constant Density Recording 32F8020A/8022A, 32P54X, 32D4661**




VRX = 750 mV @25°C

IRX = IFO

IFC programming range: 0.11 mA to 0.60 mA @25°C
(1.5 to 8.0 MHz: No Boost)

The IFC (programming current) is scaled from IFO (reference current) by the set-up shown above. Assuming the DAC current gain = 4.0, then programming is accomplished as follows:

MAX programming current required: IFC = 0.6 mA ($fc$ = 8.0 MHz) @25°C

IFO = IFC/8 = 0.075 mA (MAX) @25°C

IRX = IFO

IRX = 750mV/Rx @25°C

Rx = 5 kΩ

**FIGURE 3: 32F8021/8023 Frequency Programming**

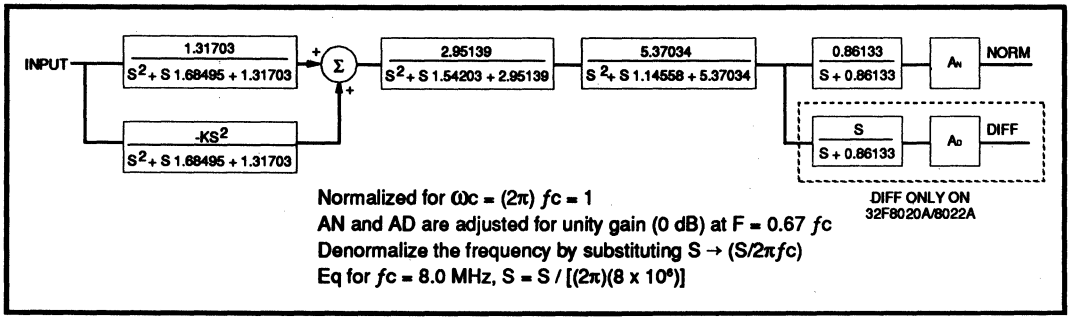



**FIGURE 4: 32F8020A/8022A/8021/8023 Normalized Block Diagram**

**TABLE 1: 32F8020A/8022A Frequency Boost Calculations**

Assuming 9.2 dB boost for **VBP = VR**

$$\frac{VBP}{VR} \cong \frac{\left(10^{(FB/20)}\right)-1}{1.884}$$

| Boost | VBP/VR | K |
|---|---|---|
| 1 dB | 0.065 | 0.16 |
| 2 dB | 0.137 | 0.34 |
| 3 dB | 0.219 | 0.54 |
| 4 dB | 0.310 | 0.77 |
| 5 dB | 0.413 | 1.03 |
| 6 dB | 0.528 | 1.31 |
| 7 dB | 0.658 | 1.63 |
| 8 dB | 0.802 | 1.99 |
| 9 dB | 0.965 | 2.40 |

**or,**

$$\text{boost in dB} \cong 20 \log\left[1.884\left(\frac{VBP}{VR}\right)+1\right]$$

| VBP/VR | Boost |
|---|---|
| 0.1 | 1.499 dB |
| 0.2 | 2.777 dB |
| 0.3 | 3.891 dB |
| 0.4 | 4.879 dB |
| 0.5 | 5.765 dB |
| 0.6 | 6.569 dB |
| 0.7 | 7.305 dB |
| 0.8 | 7.984 dB |
| 0.9 | 8.613 dB |
| 1.0 | 9.200 dB |

**TABLE 2: Calculations**
Typical change in $f$-3 dB point and frequency peak with boost.

| Boost (dB) | Gain@$fc$ (dB) | Gain@peak (dB) | $f$peak/$fc$ | $f$-3 dB/$fc$ |
|---|---|---|---|---|
| 0 | -3 | 0.00 | no peak | 1.00 |
| 1 | -2 | 0.00 | no peak | 1.21 |
| 2 | -1 | 0.00 | no peak | 1.51 |
| 3 | 0 | 0.15 | 0.70 | 1.80 |
| 4 | 1 | 0.99 | 1.05 | 2.04 |
| 5 | 2 | 2.15 | 1.23 | 2.20 |
| 6 | 3 | 3.41 | 1.33 | 2.33 |
| 7 | 4 | 4.68 | 1.38 | 2.43 |
| 8 | 5 | 5.94 | 1.43 | 2.51 |
| 9 | 6 | 7.18 | 1.46 | 2.59 |

**NOTES:** 1. $fc$ is the original programmed cutoff frequency with no boost.

2. $f$-3 dB is the new -3 dB value with boost implemented.

3. $f$peak is the frequency where the magnitude peaks when boost is implemented.

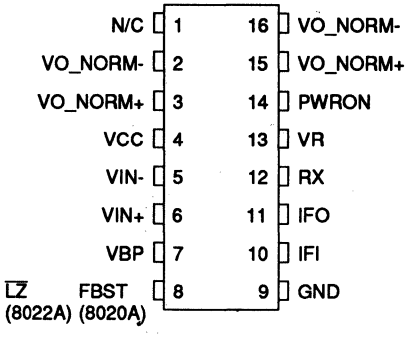
i.e., $fc$ = 8 MHz when boost = 0 dB if boost is programmed to 5 dB then

$f$-3 dB = 17.6 MHz

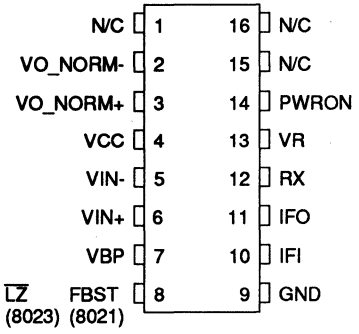
$f$peak = 9.84 MHz

# SSI 32F8020A/8022A/8021/8023
# Low-Power Programmable Electronic Filter

## PACKAGE PIN DESIGNATIONS
(Top View)




**32F8020A/8022A**
**16-Lead SON, SOL**




**32F8021/8023**
**16-Lead SON, SOL**

## THERMAL CHARACTERISTICS: θja

| | |
|---|---|
| 16-Lead SOL (150 mil) | 105° C/W |
| 20-Lead SOV (300 mil) | 100° C/W |

## ORDERING INFORMATION

| PART DESCRIPTION | | ORDER NUMBER | PACKAGE MARK |
|---|---|---|---|
| SSI 32F8020A | 16-Lead SON | 32F8020A-CN | 32F8020A-CN |
| | 16-Lead SOL | 32F8020A-CL | 32F8020A-CL |
| SSI 32F8022A | 16-Lead SON | 32F8022A-CN | 32F8022A-CN |
| | 16-Lead SOL | 32F8022A-CL | 32F8022A-CL |
| SSI 32F8021 | 16-Lead SON | 32F8021-CN | 32F8021-CN |
| | 16-Lead SOL | 32F8021-CL | 32F8021-CL |
| SSI 32F8023 | 16-Lead SON | 32F8023-CN | 32F8023-CN |
| | 16-Lead SOL | 32F8023-CL | 32F8023-CL |

**Preliminary Data:** Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.



Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 573-6000, FAX (714) 573-6914

silicon systems®
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# SSI 32F8030
## Programmable Electronic Filter

June 1992

3

## DESCRIPTION

The SSI 32F8030 Programmable Electronic Filter provides an electronically controlled low–pass filter with a separate differentiated low–pass output. A seven–pole, 0.05° Equiripple-type linear phase, low–pass filter is provided along with a single-pole, single-zero differentiator. Both outputs have matched delays. The delay matching is unaffected by any amount of programmed high frequency peaking (boost) or bandwidth. This programability, combined with low group delay variation makes the SSI 32F8030 ideal for use in many applications. Double differentiation high frequency boost is accomplished by a two–pole, low–pass with a two–pole, high–pass feed forward section to provide complementary real axis zeros. A variable attenuator is used to program the zero locations, which controls the amount of boost.

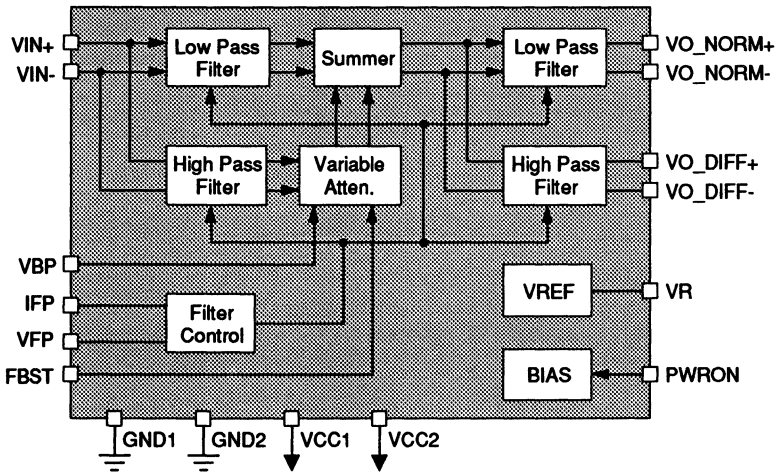
The SSI 32F8030 programmable boost and bandwidth characteristics can be controlled by external DACs or DACs provided in the SSI 32D4661 Time Base Generator. Fixed characteristics are easily accomplished with three external resistors. In addition, boost can be switched in or out by a logic signal.

The SSI 32F8030 requires only a +5V supply and is available in 16-Lead SON, and SOL packages.

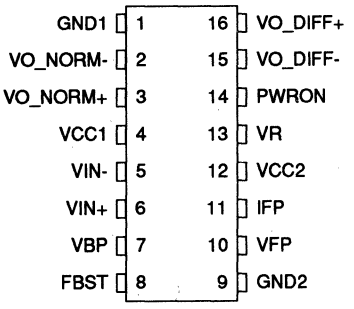
## FEATURES

- **Ideal for:**
  - **constant density recording applications**
  - **magnetic tape recording**
- **Programmable filter cutoff frequency ($fc$ = 250 kHz to 2.5 MHz)**
- **Programmable high frequency peaking (0 to 9 dB boost at the filter cutoff frequency)**
- **Matched normal and differentiated low-pass outputs**
- **Differential filter input and outputs**
- **±3.0% group delay variation from 0.2 $fc$ to 1.75 $fc$, 0.25 MHz ≤ $fc$ ≤ 2.5 MHz**
- **Total harmonic distortion less than 1%**
- **+5V only operation**
- **16-Lead SON, and SOL packages**
- **5 mW idle mode**

## BLOCK DIAGRAM




## PIN DIAGRAM




CAUTION: Use handling procedures necessary for a static sensitive component.

# SSI 32F8030
# Programmable
# Electronic Filter

## FUNCTIONAL DESCRIPTION

The SSI 32F8030, a high performance programmable electronic filter, provides a low pass 0.05° Equiripple-type linear phase seven pole filter with matched normal and differentiated outputs. The device has been optimized for usage with several Silicon Systems products, including the SSI 32D4661 Time Base Generator, the SSI 32P54x family of Pulse Detectors, and the SSI 32P4720 Combo device (Data Separator and Pulse Detector).

### CUTOFF FREQUENCY PROGRAMMING

The SSI 32F8030 programmable electronic filter can be set to a filter cutoff frequency from 250 kHz to 2.5 MHz (with no boost).

Cutoff frequency programming can be established using either a current source fed into the IFP pin, whose output current is proportional to the SSI 32F8030 output reference voltage VR, or by means of an external resistor tied from the output voltage reference pin VR to pin VFP. The former method is optimized using the SSI 32D4661 Time Base Generator, since the current source into pin IFP is available at the DAC F output of the 32D4661. Furthermore, the voltage reference input is supplied to pin VR3 of the 32D4661 by the reference voltage VR from the VR pin of the 32F8030. This reference voltage is an internally generated bandgap reference, which typically varies less than 1 % over voltage supply and temperature variation. (For the calculations below IVFP = current into IFP or VFP pins).

The cutoff frequency, determined by the -3dB point relative to a very low frequency value (< 10kHz), is related to the current IVFP injected into pin IFP by the formula

Fc (ideal, in MHz) = 3.125•IFP = 3.125•IVFP•2.2/VR, where IFP and IVFP are in mA, 0.08<IFP<0.8 mA, and VR is in volts.

If a current source is used to inject current into pin IFP, pin VFP should be left open.

If the 32F8030 cutoff frequency is set using voltage VR to bias up a resistor tied to pin VFP, the cutoff frequency is related to the resistor value by the formula

Fc (ideal, in MHz) = 3.125•IFP = 3.125•2.2/(3•Rx) where Rx is in kΩ, & 0.917 kΩ <Rx<9.17 kΩ.

If pin VFP is used to program cutoff frequency, pin IFP should be left open.

### SLIMMER HIGH FREQUENCY BOOST PROGRAMMING

The amplitude of the output signal at frequencies near the cutoff frequency can be increased using this feature. Applying an external voltage to pin VBP which is proportional to reference output voltage VR (provided by the VR pin) will set the amount of boost. A fixed amount of boost can be set by an external resistor divider network connected from pin VBP to pins VR and GND. No boost is applied if pin FBST, frequency boost enable, is at a low logic level.

The amount of boost FB at the cutoff frequency Fc is related to the voltage VBP by the formula

FB (ideal, in dB) = $20 \log_{10}[1.884(VBP/VR)+1]$, where 0<VBP<VR.

## PIN DESCRIPTION

| NAME | DESCRIPTION |
|---|---|
| VIN+, VIN- | DIFFERENTIAL SIGNAL INPUTS. The input signals must be AC coupled to these pins. |
| VO_NORM+, VO_NORM- | DIFFERENTIAL NORMAL OUTPUTS. The output signals must be AC coupled. |
| VO_DIFF+, VO_DIFF- | DIFFERENTIAL DIFFERENTIATED OUTPUTS. For minimum time skew, these outputs should be AC coupled to the pulse detector. |
| IFP | FREQUENCY PROGRAM INPUT. The filter cutoff frequency FC, is set by an external current IFP, injected into this pin. IFP must be proportional to voltage VR. This current can be set with an external current generator such as a DAC. VFP should be left open when using this pin. |
| VFP | FREQUENCY PROGRAM INPUT. The filter cutoff frequency can be set by programming a current through a resistor from VR to this pin. IFP should be left open when using this pin. |
| VBP | FREQUENCY BOOST PROGRAM INPUT. The high frequency boost is set by an external voltage applied to this pin. VBP must be proportional to voltage VR. A fixed amount of boost can be set by an external resistor divider network connected from VBP to VR and GND. No boost is applied if the FBST pin is grounded, or at logic low. |
| FBST | FREQUENCY BOOST. A high logic level or open input enables the frequency boost circuitry. |
| PWRON | POWER ON. A high logic level enables the chip. A low level puts the chip in a low power state. |
| VR | REFERENCE VOLTAGE. Internally generated reference voltage. |
| VCC1, VCC2 | +5 VOLT SUPPLY. |
| GND1, GND2 | GROUND |

## ELECTRICAL SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may damage the device.

| PARAMETER | RATING |
|---|---|
| Storage Temperature | -65 to +150°C |
| Junction Operating Temperature, Tj | +130°C |
| Supply Voltage, VCC1, VCC2 | -0.5 to 7V |
| Voltage Applied to Inputs | -0.5 to VCC + 0.5V |
| IFP, VFP Inputs Maximum Current | ≤1.2 mA |

### RECOMMENDED OPERATING CONDITIONS

| PARAMETER | RATING |
|---|---|
| Supply voltage, VCC1, VCC2 | 4.5 < VCC1,2 < 5.50V |
| Ambient Temperature | 0 < Ta < 70°C |

## ELECTRICAL SPECIFICATIONS

### Power Supply Characteristics

Unless otherwise specified, recommended operating conditions apply.

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| ICC | Power Supply Current | PWRON ≤ 0.8V | | | 0.5 | mA |
| ICC | Power Supply Current | PWRON ≥ 2.0V | | 28 | 42 | mA |
| PD | Power Dissipation | PWRON ≥ 2.0V | | 140 | 231 | mW |
| PD | Power Dissipation | PWRON ≤ 0.8V | | | 3 | mW |

### DC Characteristics

| | | | | | | |
|---|---|---|---|---|---|---|
| VIH | High Level Input Voltage | TTL input | 2.0 | | VCC+0.3 | V |
| VIL | Low Level Input Voltage | | -0.3 | | 0.8 | V |
| IIH | High Level Input Current | VIH = 2.7V | | | 20 | µA |
| IIL | Low Level Input Current | VIL = 0.4V | | | −1.5 | mA |

### Filter Characteristics

$fc$ = 1.25 MHz unless otherwise stated

| | | | | | | |
|---|---|---|---|---|---|---|
| FCA | Filter $fc$ Accuracy | using IFP pin: IFP = 0.4 mA or<br>using VFP pin: Rx = 1.84 kΩ | 1.125 | | 1.375 | MHz |
| AO | VO_NORM Diff Gain | F = 0.67 $fc$, FB = 0 dB | 0.8 | | 1.20 | V/V |
| AD | VO_DIFF Diff Gain | F = 0.67 $fc$, FB = 0 dB | 0.9AO | | 1.1AO | V/V |
| FBA | Frequency Boost Accuracy | VBP = VR | 8.0 | 9.2 | 10.4 | dB |
| TGD0 | Group Delay Variation Without Boost* | 0.25 MHz ≤ $fc$ ≤ 2.5 MHz<br>F = 0.2 $fc$ to 1.75 $fc$ | −3 | | +3 | % |
| TGDB | Group Delay Variation With Boost* | 0.25 MHz ≤ $fc$ ≤ 2.5 MHz<br>VBP = VR, F = 0.2 $fc$ to 1.75 $fc$ | −3 | | +3 | % |
| VIF | Filter Input Dynamic Range | THD = 1% max, F = 0.67 $fc$<br>(no boost, 1000 pF capacitor across Rx) | 1.0 | | | Vpp |
| VOF | Filter Normal Output Dynamic Range | THD = 1% max, F = 0.67 $fc$<br>VBP = 0 (1000 pF capacitor across Rx) | 1.0 | | | Vpp |
| VOF | Filter Normal Output Dynamic Range | THD = 1% max, F = 0.67 $fc$<br>VBP = VR (1000 pF capacitor across Rx) | 1.0 | | | Vpp |
| VOF | Filter Differentiated Output Dynamic Range | THD = 1% max, F = 0.67 $fc$<br>VBP = 0 (1000 pF capacitor across Rx) | 1.0 | | | Vpp |
| VOF | Filter Differentiated Output Dynamic Range | THD = 1% max, F = 0.67 $fc$<br>VBP = VR (1000 pF capacitor across Rx) | 1.0 | | | Vpp |

**Filter Characteristics** (continued)

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| RIN Filter Diff Input Resistance | | 3.0 | 4.0 | 5.0 | kΩ |
| CIN Filter Diff Input Capacitance* | | | 3.0 | | pF |
| EOUT Output Noise Voltage* Differentiated Output | BW = 100 MHz, Rs = 50Ω, Ifp = 0.8 mA, VBP = 0.0V | | 2.7 | 3.2 | mVRms |
| EOUT Output Noise Voltage* Normal Output | BW = 100 MHz, Rs = 50Ω Ifp = 0.8 mA, VBP = 0.0V | | 1.6 | 2.0 | mVRms |
| EOUT Output Noise Voltage* Differentiated Output | BW = 100 MHz, Rs = 50Ω Ifp = 0.8 mA, VBP = VR | | 3.1 | 3.8 | mVRms |
| EOUT Output Noise Voltage* Normal Output | BW = 100 MHz, Rs = 50Ω Ifp = 0.8 mA, VBP = VR | | 1.8 | 2.2 | mVRms |
| EOUT Output Noise Voltage* Differentiated Output | BW = 10 MHz, Rs = 50Ω, Ifp = 0.08 mA, VBP = 0.0V | | 1.8 | 2.1 | mVRms |
| EOUT Output Noise Voltage* Normal Output | BW = 10 MHz, Rs = 50Ω Ifp = 0.08 mA, VBP = 0.0V | | 1.0 | 1.2 | mVRms |
| EOUT Output Noise Voltage* Differentiated Output | BW = 10 MHz, Rs = 50Ω Ifp = 0.08 mA, VBP = VR | | 2.0 | 2.5 | mVRms |
| EOUT Output Noise Voltage* Normal Output | BW = 10 MHz, Rs = 50Ω Ifp = 0.08 mA, VBP = VR | | 1.1 | 1.5 | mVRms |
| IO- Filter Output Sink Current | | 1.0 | | | mA |
| IO+ Filter Output Source Current | | 2.0 | | | mA |
| RO Filter Output Resistance** | Sinking 1 mA from pin | | | 70 | Ω |

* Not directly testable in production, design characteristic.
** Single ended

**Filter Control Characteristics**

| | | | | | |
|---|---|---|---|---|---|
| VR Reference Voltage Output | | 2.0 | | 2.40 | V |
| $I_{VR}$ Reference Output Source Current | | | | 2.0 | mA |

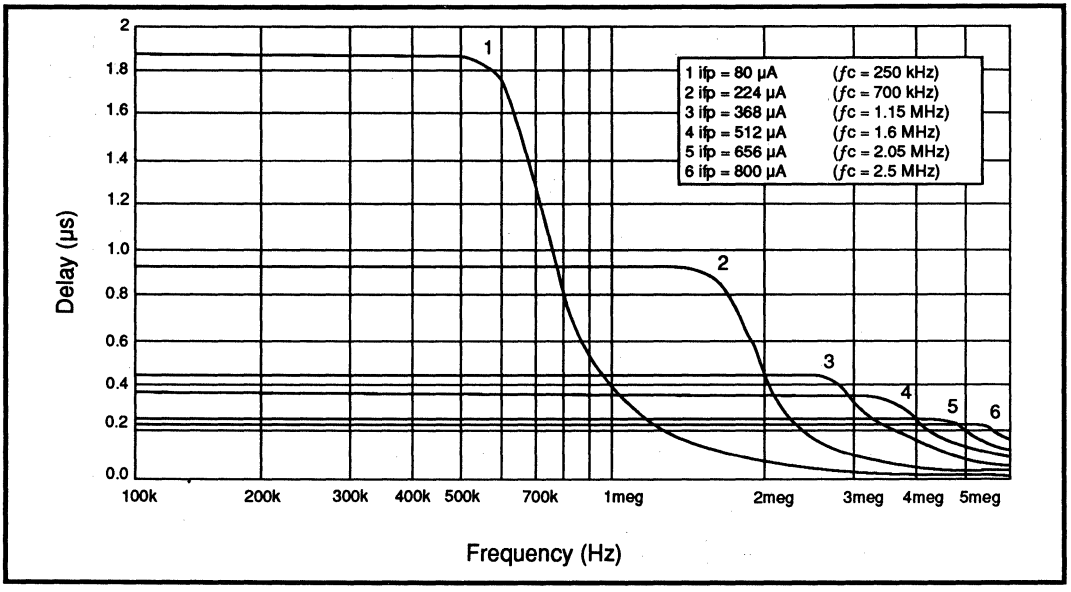



**FIGURE 1: Typical Normal/Differentiated Output Group Delay Response**

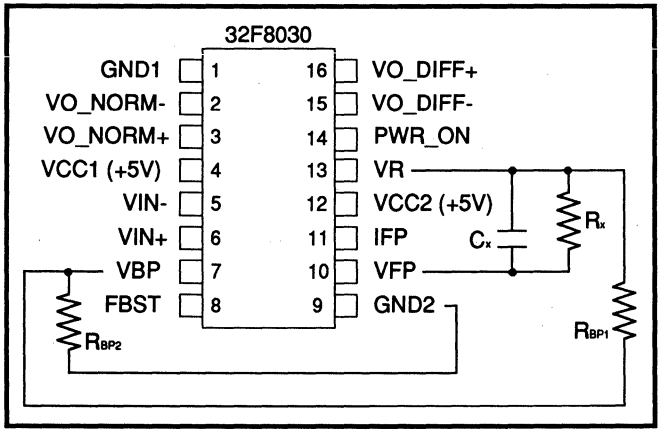



**FIGURE 1: 32F8030 Applications Setup 16-Pin SO**

VR = 2.2V

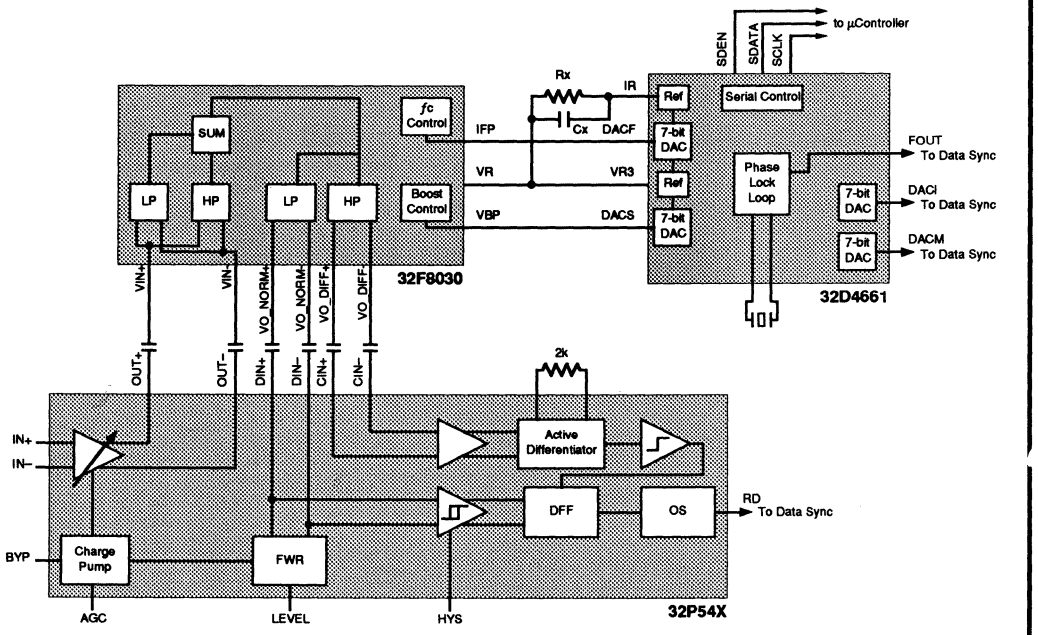
VFP = .667 VR

IVfp = .33VR/Rx

IVfp range: 0.08 mA to 0.8 mA
(0.25 MHz to 2.5 MHz)

Cx = 1000 pF needed for THD at low $fc$

VFP is used when programming current is set with a resistor from VR.
When VFP is used IFP must be left open.




IOF = DACF output current

IOF = (0.98F•VR)/127Rx

Rx = (0.98F•VR)/127IOF

Rx = current reference setting resistor

VR = Voltage Reference = 2.2V

F = DAC setting: 0-127

Full scale, F = 127

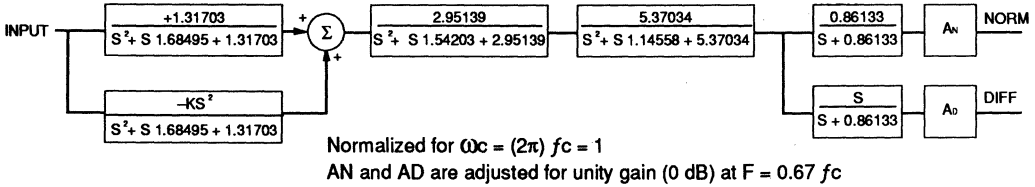
For range of Max $fc$ = 2.5 MHz then IFP = 0.8 mA

Therefore, for Max programming current range to 0.8 mA:

Rx = (0.98)(2.2/0.8) = 2.7 kΩ

Please note that in setups such as this where IFP is used for cutoff frequency programming VFP must be left open.

**FIGURE 2: Applications Setup, Constant Density Recording 32F8030, 32P54X, 32D4661**




Normalized for $\omega c = (2\pi)\ fc = 1$

AN and AD are adjusted for unity gain (0 dB) at F = 0.67 $fc$

Denormalize the frequency by substituting $S \rightarrow (S/2\pi fc)$

Eq for $fc$ = 2.5 MHz, $S = S / [(2\pi)(2.5 \cdot 10^6)] = S / (1.57080 \cdot 10^7)$

**FIGURE 3: 32F8030 Normalized Block Diagram**

**TABLE 1: 32F8030 Frequency Boost Calculations**

Assuming 9.2 dB boost for VBP = VR

$$\frac{VBP}{VR} \cong \frac{\left(10^{(FB/20)}\right)-1}{1.884}$$

| Boost | K | VBP/VR | Boost | K | VBP/VR |
|---|---|---|---|---|---|
| 1 dB | 0.16 | 0.065 | 6 dB | 1.31 | 0.288 |
| 2 dB | 0.34 | 0.137 | 7 dB | 1.63 | 0.358 |
| 3 dB | 0.54 | 0.219 | 8 dB | 1.99 | 0.437 |
| 4 dB | 0.77 | 0.310 | 9 dB | 2.40 | 0.526 |
| 5 dB | 1.03 | 0.413 | | | |

**or,**

$$\text{boost in dB} = 20\log\left[1.884\left(\frac{VBP}{VR}\right)+1\right]$$

| VBP/VR | Boost | VBP/VR | Boost |
|---|---|---|---|
| 0.1 | 1.499 dB | 0.6 | 6.569 dB |
| 0.2 | 2.777 dB | 0.7 | 7.305 dB |
| 0.3 | 3.891 dB | 0.8 | 7.984 dB |
| 0.4 | 4.879 dB | 0.9 | 8.613 dB |
| 0.5 | 5.765 dB | 1.0 | 9.200 dB |

**TABLE 2: Calculations**

Typical change in *f*-3 dB point with boost

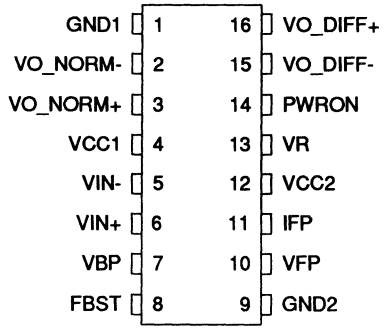
| Boost (dB) | Gain @ *f*c(dB) | Gain @ peak(dB) | *f*peak/*f*c | f-3 dB/*f*c |
|---|---|---|---|---|
| 0 | -3 | 0.00 | no peak | 1.00 |
| 1 | -2 | 0.00 | no peak | 1.21 |
| 2 | -1 | 0.00 | no peak | 1.51 |
| 3 | 0 | 0.15 | 0.70 | 1.80 |
| 4 | 1 | 0.99 | 1.05 | 2.04 |
| 5 | 2 | 2.15 | 1.23 | 2.20 |
| 6 | 3 | 3.41 | 1.33 | 2.33 |
| 7 | 4 | 4.68 | 1.38 | 2.43 |
| 8 | 5 | 5.94 | 1.43 | 2.51 |
| 9 | 6 | 7.18 | 1.46 | 2.59 |

Notes: 1. *f*c is the original programmed cutoff frequency with no boost
2. *f*-3 dB is the new -3 dB value with boost implemented
3. *f*peak is the frequency where the magnitude peaks with boost implemented

i.e., *f*c = 2.5 MHz when boost = 0 dB
if boost is programmed to 5 dB then f-3 dB = 5.5 MHz
*f*peak = 3.075 MHz

## PACKAGE PIN DESIGNATIONS

(Top View)




**16-Lead SON, SOL**

**Thermal Characteristics: θjA**

| | |
|---|---|
| 16-lead SON (150 mil) | 105° C/W |
| 16-lead SOL (300 mil) | 100° C/W |

## ORDERING INFORMATION

| PART DESCRIPTION | ORDER NUMBER | PACKAGE MARK |
|---|---|---|
| 16-lead SON (150 mil) | 32F8030-CN | 32F8030-CN |
| 16-lead SOL (300 mil) | 32F8030-CL | 32F8030-CN |



Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 573-6000, FAX (714) 573-6914

**Notes:**

silicon systems®
A TDK Group Company

# SSI 32F8101/8102/8103/8104
## Low-Power Programmable Filter

**Target Specification**

January 1993

3

## DESCRIPTION

The 32F810X is a high performance, low power, digitally programmable low-pass filter for applications requiring variable-frequency filtering. The device consists of three functional blocks: [1] a 7th-order 0.05° Equiripple Low-Pass filter, [2] two DACs for controlling the filter cutoff frequency and high-frequency peaking (boost), and [3] a Serial Port for programming the *fc* and Boost DACs. The device is offered in four frequency options: the 32F8101, 9-27 MHz; 32F8102, 6-18 MHz; 32F8103, 4-12 MHz; & 32F8104, 3-9 MHz.

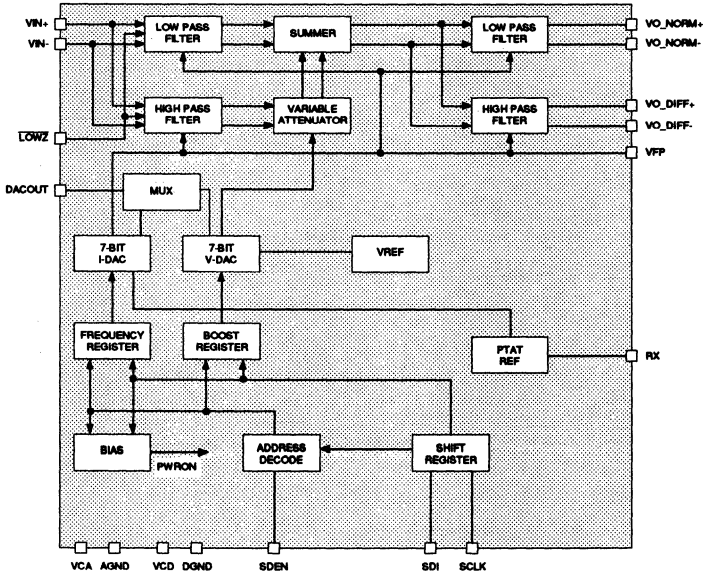
Cutoff frequency and boost are controlled by the two on-chip 7-bit DACs, which are programmed via the 3-line serial interface. Boost is programmable from 0 to 13 dB nominally, and is implemented using two symmetrical, real-axis zeroes. Both boost and *fc* control do not affect the flat group delay response.

The 32F81XX device is ideal for variable data rate and variable frequency shaping applications. It requires only a +5V supply and has an Idle mode for minimal power dissipation. The SSI 32F810X is available in 16-lead SON, and 20-Lead SOV packages.

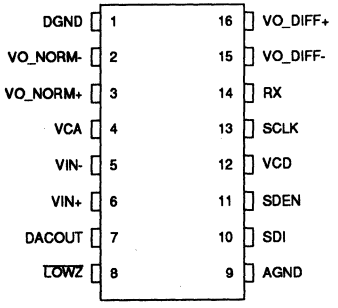
## FEATURES

- **Programmable cutoff frequency:**
  - **32F8101 - 9 to 27 MHz**
  - **32F8102 - 6 to 18 MHz**
  - **32F8103 - 4 to 12 MHz**
  - **32F8104 - 3 to 9 MHz**
- **Programmable boost/equalization of 0 to 13 dB**
- **Matched normal and differentiated outputs**
- **± 10% *fc* accuracy**
- **± 2% maximum group delay variation**
- **Less than 1% total harmonic distortion**
- **Low-Z input switch controlled by $\overline{\text{LOWZ}}$ pin**
- **No external filter components required**

## BLOCK DIAGRAM




## PIN DIAGRAM




**16-Lead SON**

CAUTION: Use handling procedures necessary for a static sensitive component.

## FUNCTIONAL DESCRIPTION

The SSI 32F810X programmable filter consists of an electronically controlled low-pass filter with a separate differentiated low-pass output. A seven-pole, low-pass filter is provided along with a single-pole, single-zero differentiator. Both outputs have matched delays. The delay matching is unaffected by any amount of programmed equalization or bandwidth. Programmable bandwidth and boost/equalization is provided by internal 7-bit control DACs. High-frequency boost equalization is accomplished by a two-pole, low-pass with a two-pole, high-pass feed forward section to provide complimentary real axis zeros. A variable attenuator is used to program the zero locations.

The filter implements a 0.05 degree equiripple linear phase response. The normalized transfer functions (i.e., $Wc = 2\pi fc = 1$) are:

$$Vnorm/Vi = [(-Ks2 + 17.98016)/D(s)] \times An$$

and

$$Vdiff/Vi = (Vnorm/Vi) \times (s/0.86133) \times Ad$$

Where D (s)=
$(S^2+1.68495s+1.31703)(S^2+1.54203\ s+2.95139)$
$(S^2+1\ .4558s+5.37034)(s+0.86133)$,

An and Ad are adjusted for a gain of 2 at $fs=(2/3)fc$.

### Filter Operation

Normally AC coupled differential signals are applied to the FIP/FIN inputs of the filter, although DC coupling can be implemented. To improve settling time of the coupling capacitors, the FIP/FIN inputs are placed into a Low-Z state when the $\overline{LOWZ}$ pin is brought high. The programmable bandwidth and boost/equalization features are controlled by internal DACs and the registers programmed through the serial port. The current reference for both DACs is set using a single 12.1 kΩ external resistor connected from pin RX to ground. The voltage at pin RX is proportional to absolute temperature (PTAT), hence the current for the DACs is a PTAT reference current.

Bandwidth Control: The programmable bandwidth is set by the filter cutoff DAC. This DAC has two separate 7-bit registers that can program the DAC value as follows:

***fc* = 0.2126 x DACF (MHz)** for the 32F8101
***fc* = 0.1417 x DACF (MHz)** for the 32F8102
***fc* = 0.09449 x DACF (MHz)** for the 32F8103
***fc* = 0.07087 x DACF (MHz)** for the 32F8104
where DACF = Cutoff Frequency Control Register value (decimal)

The filter cutoff set by the internal DAC is the unboosted 3 dB frequency. When boost/equalization is added, the actual 3 dB point will move out. Table 1 provides information on boost versus 3dB frequency.

**TABLE 1: 3dB Cutoff Frequency Versus Boost Magnitude**

| BOOST (dB) | *fc* (3 dB) | BOOST (dB) | *fc* (3 dB) |
|---|---|---|---|
| 0 | 1.00 | 7 | 2.41 |
| 1 | 1.22 | 8 | 2.53 |
| 2 | 1.47 | 9 | 2.65 |
| 3 | 1.74 | 10 | 2.73 |
| 4 | 1.95 | 11 | 2.81 |
| 5 | 2.13 | 12 | 2.88 |
| 6 | 2.28 | 13 | 2.96 |

### Boost/Equalization Control

The programmable equalization is also controlled by an internal DAC. The 7-bit Filter Boost Control Register (FBCR) determines the amount of equalization that will be added to the 3 dB cutoff frequency, as follows:

**Boost = 20 log [(0.0273 x FBCR) + 1] (dB)**

For example, with the DAC set for maximum output (FBCR = 7Fhex or 127) there will be 13 dB of boost added at the 3 dB frequency. This will result in +10 dB of signal boost above the 0 dB baseline.

### SERIAL INTERFACE OPERATION

The serial interface is a CMOS bi-directional port for reading and writing programming data from/to the internal registers of the 32F810X. For data transfers SDEN is brought high, serial data is presented at the SDATA pin, and a serial clock is applied to the SCLK pin.

After the SDEN goes high, the first 16 pulses applied to the SCLK pin will shift the data presented at the SDATA pin into an internal shift register on the rising edge of each clock. An internal counter prevents more than 16 bits from being shifted into the register. The data in the shift register is latched when SDEN goes low. If less than 16 clock pulses are provided before SDEN goes low, the data transfer is aborted.

All transfers are shifted into the serial port LSB first. The first byte of the transfer is address and instruction information. The LSB of this byte is the R/W bit which determines if the transfer is a read (1) or a write (0). The remaining seven bits determine the internal register to be accessed. The second byte contains the programming data. At initial power-up, the contents of the internal registers will be in an unknown state and they must be programmed prior to operation. During power down modes, the serial port remains active and register programming data is retained.

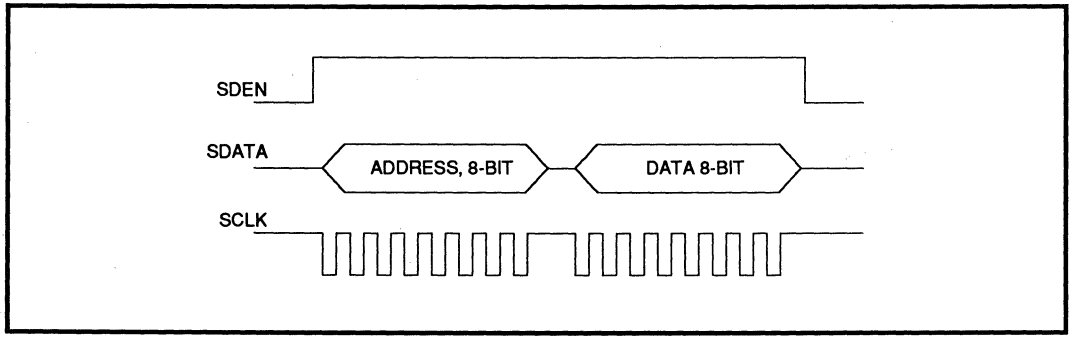



**FIGURE 1: Serial Port Data Transfer Format**

## PIN DESCRIPTION

### POWER SUPPLY PINS

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| VCA | - | Filter analog power supply pin |
| VCD | - | Serial port power supply pin |
| AGND | - | Filter analog ground pin |
| DGND | - | Serial port digital ground pin |

### INPUT PINS

| | | |
|---|---|---|
| VIN+, VIN- | I | FILTER SIGNAL INPUTS: The AGC output signals must be AC coupled into these pins. |

### OUTPUT PINS

| | | |
|---|---|---|
| VO_DIFF+, VO_DIFF- | O | DIFFERENTIAL DIFFERENTIATED OUTPUTS: Filter differentated outputs. These outputs are normally AC coupled. |
| VO_NORM+, VO_NORM- | O | DIFFERENTIAL NORMAL OUTPUTS: Filter normal low pass output signals. These outputs are normally AC coupled. |
| DACOUT | O | DAC VOLTAGE TEST POINT: This test point monitors the outputs of the internal DACs. The source DAC is selected by programming the two MSBs of the WSCR register. |
| RX | - | REFERENCE RESISTOR INPUT: An external 12.1 kΩ, 1% resistor is connected from this pin to ground to establish a precise PTAT (proportional to absolute temperature) reference current for the filter. |

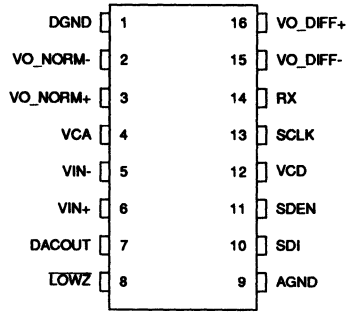
### SERIAL PORT PINS

| | | |
|---|---|---|
| SDEN | I/O | SERIAL DATA ENABLE: Serial enable CMOS compatible input. A high level TTL input enables the serial port. |
| SDI | I/O | SERIAL DATA: Serial data CMOS compatible input. NRZ programming data for the internal registers is applied to this input. |
| SCLK | I/O | SERIAL CLOCK: Serial clock CMOS compatible input. The clock applied to this pin is synchronized with the data applied to SDATA. |

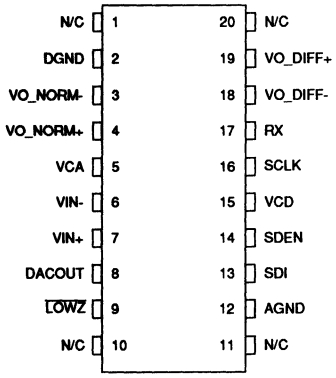
## PACKAGE PIN DESIGNATIONS
(Top View)

**THERMAL CHARACTERISTICS: θja**

| | |
|---|---|
| 16-lead SON | 100° C/W |
| 20-lead SOV | 125° C/W |




**16-Lead SON**




**20-Lead SOV**



Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 573-6000, FAX (714) 573-6914

**Notes:**

silicon systems®
A TDK Group Company

# SSI 32F8120
## Low-Power Programmable Electronic Filter
## Preliminary Data

December 1992

3

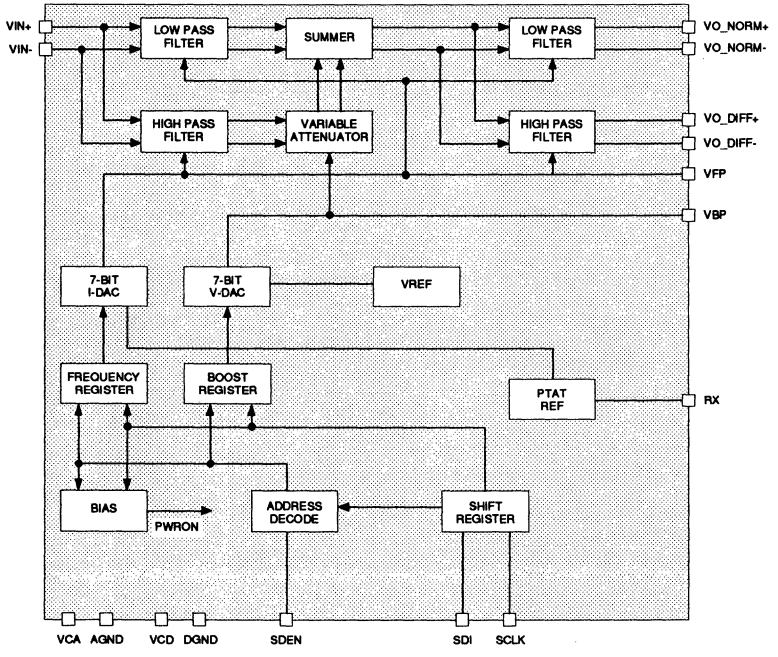
## DESCRIPTION

The SSI 32F8120 is a continuous time, low pass filter with programmable bandwidth and high frequency boost. The low pass filter is a 2 zero / 7 pole 0.05° phase equiripple type, featuring excellent group delay characteristics. It features 1.5 - 8 MHz programmable bandwidth and 0-10 dB programmable boost. Both functions are controlled by 7-bit command words, which are input via a 3-line serial interface.

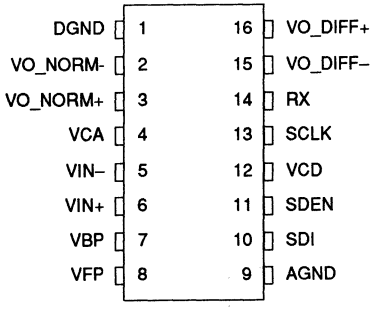
## FEATURES

- **Programmable filter cutoff frequency ($f_C$ =1.5 to 8 MHz) with no external components**
- **Programmable pulse slimming equalization (0 to 10 dB boost at the filter cutoff frequency)**
- **± 10% cutoff frequency accuracy**
- **Matched normal and differentiated low-pass outputs**
- **Differential filter inputs and outputs**
- **Device idle mode**
- **+5V only operation**
- **No external filter components required**
- **Supports constant density recording**

## BLOCK DIAGRAM




## PIN DIAGRAM




CAUTION: Use handling procedures necessary for a static sensitive component.

# SSI 32F8120
# Low-Power Programmable Electronic Filter

## FUNCTIONAL DESCRIPTION

### CUTOFF FREQUENCY PROGRAMMING

The SSI 32F8120 programmable electronic filter can be set to a filter cutoff frequency from 1.5 to 8 MHz. The cutoff frequency can be set by using the serial port through pins SDI, SDEN, and SCLK. SDI is the serial data input for an 8-bit control shift register, SDEN is the control register enable, and SCLK is the control register clock. The data packet is transmitted MSB (D7) first. The first four bits are the register address, the last four are the data bits. Registers larger than four bits must be loaded with two 8-bit data packets. See Table 1.

$fc$ is determined by the equation:

$fc$ (MHz) = 0.061321 (F_Code) + 0.212264

1.5 MHz ≤ $fc$ ≤ 8 MHz

21 ≤ F_ Code ≤ 127

### SLIMMER HIGH FREQUENCY BOOST PROGRAMMING

The amplitude of the input signal at frequencies near the cutoff frequency can be increased using this feature. By controlling the V-DAC output, the boost can be determined. The amount of boost at the cutoff frequency is related to the V-DAC output by the following formula:

$$[\text{Ouput of V-DAC} = VBP = VREF \times \frac{S\_Code}{127}]$$

BOOST (dB) = 20•log [0.01703 (S_Code) +1].

**TABLE 1**

| ADDRESS BITS | | | | USAGE | DATA BITS | | | |
|---|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | | D3 | D2 | D1 | D0 |
| X | 0 | 0 | 0 | S-MSB REGISTER | X | S6 | S5 | S4 |
| X | 0 | 0 | 1 | S-LSB REGISTER | S3 | S2 | S1 | S0 |
| X | 0 | 1 | 0 | F-MSB REGISTER | X | F6 | F5 | F4 |
| X | 0 | 1 | 1 | F-LSB REGISTER | F3 | F2 | F1 | F0 |
| X | 1 | 1 | 1 | P REGISTER | X | X | X | P0 |

X = Don't Care
S = 7-bit Boost (Slimming) Control
F = 7-bit Frequency (Bandwidth) Control
P = Power Down Control; PO = 1 for power up; PO = 0 for power down

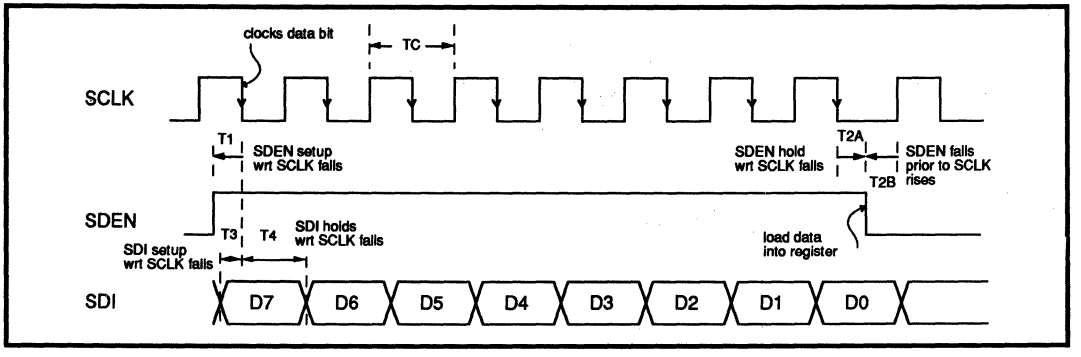



**FIGURE 1: Serial Port Timing Diagram**

## PIN DESCRIPTIONS

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| VIN+, VIN– | I | DIFFERENTIAL FILTER INPUTS. The input signals must be AC coupled to these pins. |
| VO_NORM+, VO_NORM– | O | DIFFERENTIAL NORMAL OUTPUTS. The output signals must be AC coupled to the pulse detector. |
| VO_DIFF+ VO_DIFF– | O | DIFFERENTIAL DIFFERENTIATED OUTPUTS. For minimum pulse pairing, these outputs should be AC coupled to the pulse detector. |
| SDEN | I | SERIAL DATA ENABLE. A logic HIGH level allows SERIAL CLOCK to clock data into the control register via the SERIAL DATA input. A logic LOW level latches the register data and issues the information to the appropriate circuitry. |
| SCLK | I | SERIAL CLOCK. Negative edge triggered clock input for serial register. |
| SDI | I | SERIAL DATA INPUT. |
| RX | – | REFERENCE CURRENT SET. With an external resistor (Rx = 5 kΩ ±1%) to ground, this pin gives a voltage proportional to the absolute temperature, setting the range for VFP. |
| VCA | I | ANALOG +5 VOLT SUPPLY. |
| VCD | I | DIGITAL +5 VOLT SUPPLY. |
| AGND | I | ANALOG GROUND. |
| DGND | I | DIGITAL GROUND. |
| VBP | O | BOOST PROGRAMMING VOLTAGE. Output of V-DAC which programs the boost. |
| VFP | O | CUTOFF FREQUENCY PROGRAMMING VOLTAGE. Output of I-DAC which programs the cutoff frequency.* |
| *A minimum load resistance of 150 kΩ should be used to avoid affecting the total minimum on-chip resistance of 1.35 kΩ. | | |

## ELECTRICAL SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may damage the device.

| PARAMETER | RATING |
|---|---|
| Storage Temperature | -65 to +150 °C |
| Junction Operating Temperature, Tj | +130 °C |
| Supply Voltage, VCC | -0.5 to 7V |
| Voltage Applied to Inputs* | -0.5 to VCC V |
| Maximum Power Dissipation, $fc$ = 8 MHz, Vcc = 5.5V | 0.5W |
| T1 Lead Temperature (1/16" from case for 10 seconds) | 260 °C |
| * Analog input signals of this magnitude shall not cause any change or degradation in filter performance after signal has returned to normal operating range. | |

### RECOMMENDED OPERATING CONDITIONS

| | |
|---|---|
| Supply voltage, VCC | 4.5V < VCC < 5.5V |
| Ambient Temperature | 0 °C < Ta < 70 °C |
| Tj Junction Temperature | 0 °C < Tj < 130 °C |

### ELECTRICAL CHARACTERISTICS

Unless otherwise specified recommended operating conditions apply.

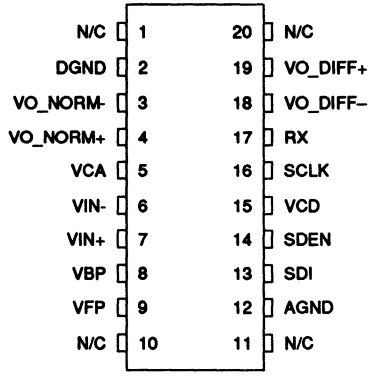
| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Isupply | VCC = 5.5V, outputs unloaded | | 55 | 75 | mA |
| Idle Mode Current | | | 9 | 13 | mA |
| Idle to Active Mode Recovery Time | | | | 50 | µs |
| Serial port program to output response time | | | | 50 | µs |
| **DC Characteristics** | | | | | |
| VIH High Level Input Voltage | TTL input | 2.0 | | | V |
| VIL Low Level Input Voltage | | | | 0.8 | V |
| IIH High Level Input Current | VIH = 2.7V | | | 20 | µA |
| IIL Low Level Input Current | VIL = 0.4V | –1.5 | | | mA |

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| **Filter Characteristics** | | | | | |
| *fc* Filter Cutoff Frequency | *fc* = VFP, 21 ≤ F_Code ≤ 127 | 1.5 | | 8 | MHz |
| FCA Filter *fc* Accuracy | *fc* = VFP, 8 MHz | -10 | | +10 | % |
| Cutoff Resolution | 1.5 to 8 MHz | 100 | | | kHz |
| AO VO_NORM Diff Gain | F = 0.67 *fc* | 0.7 | | 1.1 | V/V |
| AD VO_DIFF Diff Gain | F = 0.67 *fc* | 0.90 AO | | 1.2 AO | V/V |
| FB Frequency Boost at *fc* | FB(dB) = 20 log [0.01703 (S_Code) +1] | 0 | | 10 | dB |
| FBA Frequency Boost Accuracy | 0 to 10 dB, Ta < 22 °C | –1.5 | | +1.5 | dB |
| FBA Frequency Boost Accuracy | 0 to 10 dB, Ta > 22 °C | –1 | | +1 | dB |
| TGD0 Group Delay Variation Without Boost | 0.2 *fc* - *fc* | –2% gdm | | +2% gdm | ns |
| *fc* = 1.5 - 8 MHz gdm = group delay magnitude | *fc* - 1.75 *fc* | –3% gdm | | +3% gdm | ns |
| TGDB Group Delay Variation With Boost | 0.2 *fc* - *fc* | –2% gdm | | +2% gdm | ns |
| *fc* = 1.5 - 8 MHz | *fc* - 1.75 *fc* | –3% gdm | | +3% gdm | ns |
| Boost Resolution | 1.5 to 8 MHz | .25 | | | dB |
| VIF Filter Input Dynamic Range | THD = 1.5% max, VBP = 0, VO_NORM 0.1 µF capacitor across Rx | 1.5 | | | Vppd |
| VOF Filter Output Dynamic Range | THD = 1.5% max, VBP = 0, VO_NORM 0.1 µF capacitor across Rx | 1.5 | | | Vppd |
| VIF Filter Input Dynamic Range | THD = 3.5% max, VBP = 0, VO_DIFF 0.1 µF capacitor across Rx | 1.5 | | | Vppd |
| VOF Filter Output Dynamic Range | THD = 3.5% max, VBP = 0, VO_DIFF 0.1 µF capacitor across Rx | 1.5 | | | Vppd |
| VIF Filter Input Dynamic Range | THD = 1.5% max, VBP = 0, VO_NORM 0.1 µF capacitor across Rx | 1.0 | | | Vppd |
| VOF Filter Output Dynamic Range | THD = 1.5% max, VBP = 0, VO_NORM 0.1 µF capacitor across Rx | 1.0 | | | Vppd |
| VIF Filter Input Dynamic Range | THD = 2.0% max, VBP = 0, VO_DIFF 0.1 µF capacitor across Rx, Ta < 22 °C | 1.0 | | | Vppd |
| VOF Filter Output Dynamic Range | THD = 2.0% max, VBP = 0, VO_DIFF 0.1 µF capacitor across Rx, Ta < 22 °C | 1.0 | | | Vppd |
| VIF Filter Input Dynamic Range | THD = 1.5% max, VBP = 0, VO_DIFF 0.1 µF capacitor across Rx, Ta < 22 °C | 1.0 | | | Vppd |
| VOF Filter Output Dynamic Range | THD = 1.5% max, VBP = 0, VO_DIFF 0.1 µF capacitor across Rx, Ta < 22 °C | 1.0 | | | Vppd |

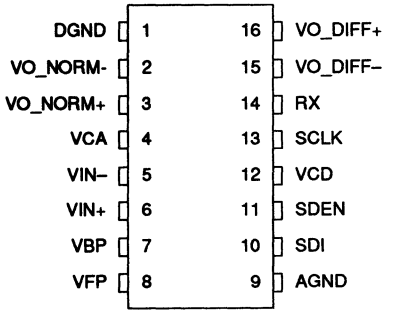
## ELECTRICAL SPECIFICATIONS (continued)

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| **Filter Characteristics** (continued) | | | | | |
| RIN Filter Diff Input Resistance | | 3.0 | | | kΩ |
| CIN Filter Input Capacitance | | | | 7 | pF |
| EOUT Output Noise Voltage (VO_NORM) | BW = 100 MHz, 0 dB Boost<br>50Ω input<br>$fc$ = 8 MHz 10 dB Boost | | 1.8<br><br>2.35 | 3<br><br>4 | mVRms<br><br>mVRms |
| EOUT Output Noise Voltage (VO_DIFF) | BW = 100 MHz, 0 dB Boost<br>50Ω input<br>$fc$ = 8 MHz 10 dB Boost | | 4.2<br><br>5.85 | 6<br><br>9 | mVRms<br><br>mVRms |
| IO- Filter Output Sink Current | | 1.0 | | | mA |
| IO+ Filter Output Source Current | | 3.0 | | | mA |
| RO Filter Output Resistance (Single ended) | Output source current, IO+ = 1 mA | | | 60 | Ω |
| TC Period, SCLK | | 100 | | | ns |
| T1 SDEN Setup to SCLK Falls | | 0 | | | ns |
| T2A SDEN Hold wrt SCLK Falls | | 0 | | | ns |
| T2B SDEN Falls prior to SCLK Rises | | 25 | | | ns |
| T3 SDI Setup to SCLK Falls | | 25 | | | ns |
| T4 SDI Hold to SCLK Falls | | 25 | | | ns |
| Power Supply Rejection Ratio | 100 mVpp @ 5 MHz on VCA, VCD | 40 | 70 | | dB |
| Common Mode Rejection Ratio | Vin = 0 VDC + 100 mVpp @5 MHz | 30 | 50 | | dB |
| Bias: Vin+, Vin- | VCC = 5V | 2.5 | 2.9 | 3.3 | V |
| VO_NORM+, VO_NORM– | VCC = 5V | 2.8 | 3.2 | 3.6 | V |
| VO_DIFF+, VO_DIFF- | VCC = 5V | 2.8 | 3.2 | 3.6 | V |
| Change in Normal Output Offset | FDAC switched from 21-127 | | 20 | | mV |
| Change in Differentiated Output Offset | FDAC switched from 21-127 | | 20 | | mV |

## PACKAGE PIN DESIGNATIONS
(Top View)




**20-Lead SOV**




**16-Lead SOL**

## THERMAL CHARACTERISTICS: θja

| | |
|---|---|
| 16-lead SOL | 100° C/W |
| 20-lead SOV | 125° C/W |

## ORDERING INFORMATION

| PART DESCRIPTION | | ORDER NUMBER | PACKAGE MARK |
|---|---|---|---|
| SSI 32F8120 | 16-Lead SOL | 32F8120-CL | 32F8120-CL |
| | 20-Lead SOV | 32F8120-CV | 32F8120-CV |

**Preliminary Data:** Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.



Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 573-6000, FAX (714) 573-6914

**Notes:**

silicon systems®
A TDK Group Company

# SSI 32F8130/8131
## Low-Power Programmable Electronic Filter

January 1993

3

## DESCRIPTION

The SSI 32F8130/8131 Programmable Electronic Filters are digitally controlled low pass filters with a normal low pass output and a time differentiated low pass output. The low pass filter is of a 7-pole / 2-zero 0.05° phase equiripple type, with flat group delay response beyond the passband.

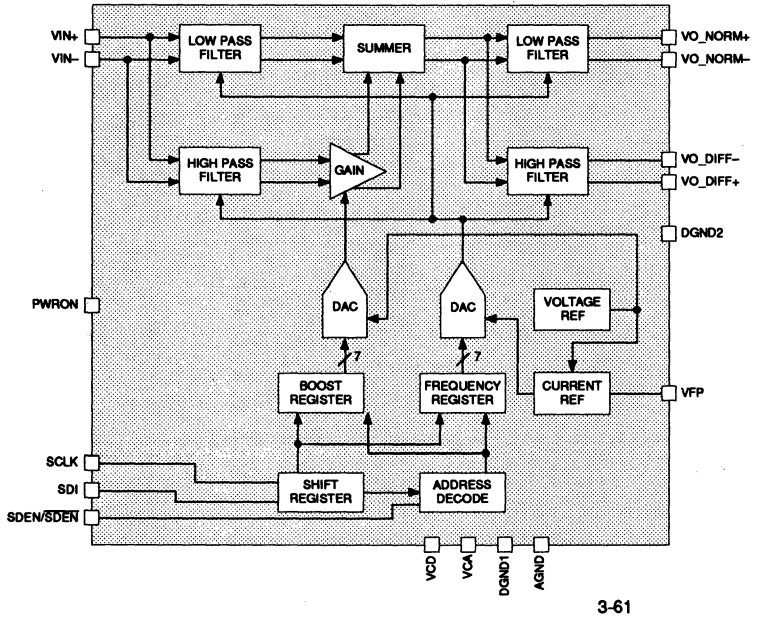
The SSI 32F8130/8131 bandwidth and boost are controlled by two on-chip 7-bit DACs, which are programmed via a 3-line serial interface. The SSI 32F8130 filter bandwidth is programmable from 250 kHz to 2.5 MHz. The SSI 32F8131 is programmable from 150 kHz to 1.4 MHz. The boost is programmable from 0 to 10 dB. Because the boost function is implemented as two zeros on the real axis with opposite sign, the flat group delay characteristic is not affected by the boost programming.

The SSI 32F8130/8131 are ideal for multi-rate, equalization applications. They require only a +5V supply and have a power down mode for minimal idle dissipation. The SSI 32F8130/8131 is available in a 16-lead SOL package.

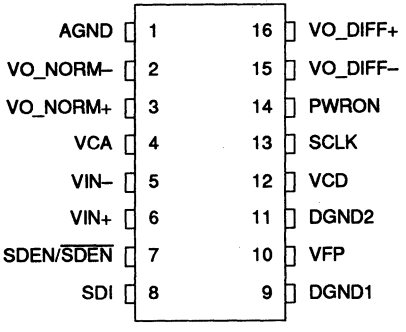
## FEATURES

- **Programmable filter cutoff frequency (SSI 32F8130 FC=0.25 to 2.5 MHz, SSI 32F8131: FC = 0.15 to 1.4 MHz) with no external components, serial data connections to minimze pin count**
- **Power down mode (<5 mW)**
- **Programmable pulse slimming equalization (0 to 10 dB boost at the filter cutoff frequency)**
- **Matched normal and differentiated low-pass outputs**
- **Differential filter inputs and outputs**
- **Programming via internal 7-bit DACs**
- **No external filter components required**
- **+5V only operation**
- **Supports constant density recording**

## BLOCK DIAGRAM




## PIN DIAGRAM




SSI 32F8130: Pin 7 = SDEN
SSI 32F8131: Pin 7 = $\overline{\text{SDEN}}$

CAUTION: Use handling procedures necessary for a static sensitive component.

# SSI 32F8130/8131
# Low-Power Programmable Electronic Filter

## FUNCTIONAL DESCRIPTION

The SSI 32F8130/8131, a high performance programmable electronic filter, provides a 7-pole / 2-zero 0.05° equiripple linear phase low pass function with matched normal and time differentiated outputs. The device includes multiple biquads and first-order sections to accomplish the filter function, two 7-bit DACs for bandwidth and boost controls, a 3-line serial interface, and complete bias reference circuits. Only one external precision 8.25 kΩ resistor should be connected from the VFP pin to ground for operation. See Figure 1.

### SERIAL INTERFACE

The SSI 32F8130/8131 allows easy digital controls of filter bandwidth and magnitude equalization via a 3-line serial interface. The three pins are SDI, SDEN and SCLK. SDI is the serial data input to an internal 8-bit shift register. SDEN is the shift register enable. SCLK is the shift register clock. Besides the 8-bit shift register which accepts data from the SDI input, there are four 4-bit registers which hold the filter bandwidth and boost controls. Two 4-bit registers are assigned to each control function, because a 7-bit binary control is required for each function.

The S-MSB register, whose address code is X000, holds the 3 MSBs of the boost control. The S-LSB register, whose address code is X001, holds the 4 LSBs of the boost control. The F-MSB register, whose address code is X010, holds the 4 MSBs of the cutoff frequency control. The F-LSB register, whose address code is X011, holds the 4 LSBs of the cutoff frequency control.

The serial interface consists of data packets, which are structured as 4-bit address decode followed by 4-bit data. Figure 2 shows the serial interface timing to successfully program the SSI 32F8130/8131.

### CUTOFF FREQUENCY PROGRAMMING

The cutoff frequency, $fc$, is defined as the -3dB bandwidth with no magnitude equalization applied, and is programmable from 250 kHz to 2.5 MHz for SSI 32F8130, and 150 kHz to 1.4 MHz for SSI 32F8131. While the $fc$ is controlled by an on-chip 7-bit DAC, the cutoff frequency resolution is better than 20-kHz step.

Let F_Code be the decimal equivalent of the 7-bit control. The cutoff frequency can be determined by the following equations:

SSI 32F8130 $fc$ (kHz) = 18.2 x F_Code +70

SSI 32F8131 $fc$ (kHz) = 10.81 x F_Code +37

where 12 < F_Code < 127.

### MAGNITUDE EQUALIZATION PROGRAMMING

The magnitude equalization, measured in dB, is the amount of high frequency peaking at the cutoff frequency relative to the original -3 dB point. For example, when 10 dB boost is applied, the magnitude response peaks up 7 dB above the DC gain. This equalization function is also controlled by an on-chip 7-bit DAC.

Let S_Code be the decimal equivalent of the 7-bit control. The magnitude equalization can be determined by the equation:

$$\text{Boost (dB)} = 20 \times \log_{10} [0.01703 \times \dot{S}\_\text{Code} + 1]$$

where 0 < S_Code < 127.

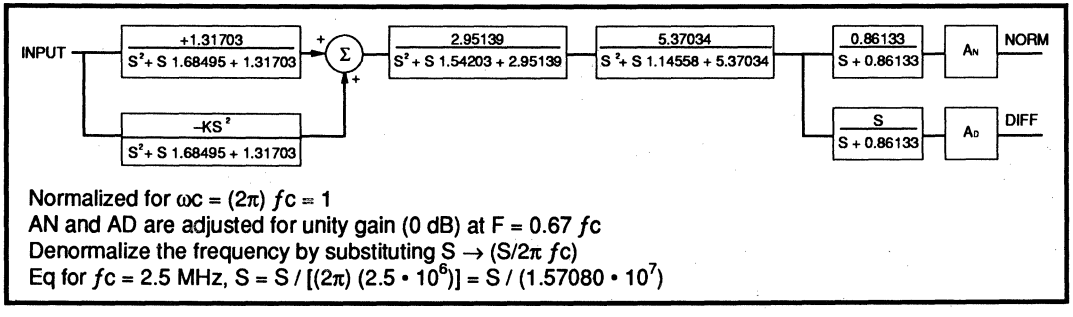



**FIGURE 1: Normalized Transfer Function of the SSI 32F8130/8131**

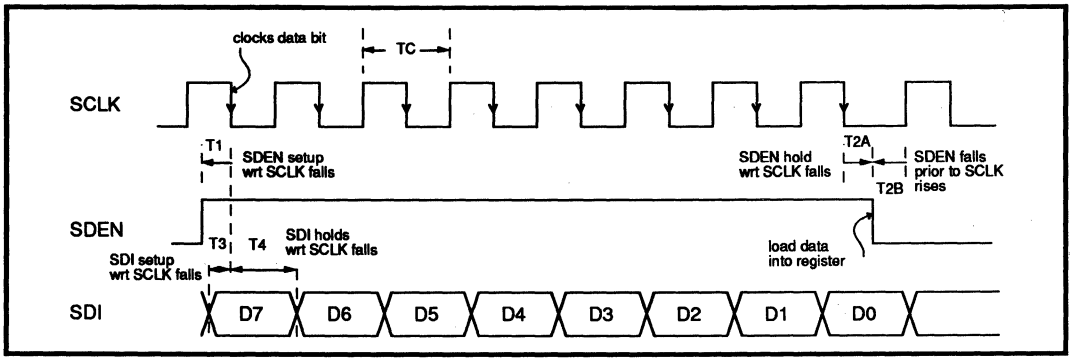



**FIGURE 2: Serial Port Timing Relationship**

Note:
The serial data enable function of the SSI 32F8130 and that of the SSI 32F8131 are of opposite polarity.

**TABLE 1: Data Packet Fields**

| | ADDRESS BITS | | | | USAGE | DATA BITS | | | |
|---|---|---|---|---|---|---|---|---|---|
| | D7 | D6 | D5 | D4 | | D3 | D2 | D1 | D0 |
| R0 | X | 0 | 0 | 0 | S - MSB REGISTER | X | S6 | S5 | S4 |
| R1 | X | 0 | 0 | 1 | S - LSB REGISTER | S3 | S2 | S1 | S0 |
| R2 | X | 0 | 1 | 0 | F - MSB REGISTER | X | F6 | F5 | F4 |
| R3 | X | 0 | 1 | 1 | F - LSB REGISTER | F3 | F2 | F1 | F0 |

X = Don't care bit.

## PIN DESCRIPTION

| NAME | DESCRIPTION |
|---|---|
| VIN+, VIN– | DIFFERENTIAL FILTER INPUTS. The input signals must be AC coupled to these pins. |
| VO_NORM+, VO_NORM– | DIFFERENTIAL NORMAL OUTPUTS. The output signals must be AC coupled to the load. |
| VO_DIFF+ VO_DIFF– | DIFFERENTIAL DIFFERENTIATED OUTPUTS. These outputs should be AC coupled to the load. |
| PWR_ON | POWER ON. A TTL high logic level enables the chip. A low level or open circuit puts the chip into a low power state. |
| SDEN (8130) $\overline{\text{SDEN}}$ (8131) | SERIAL DATA ENABLE. An active level allows SCLK to clock data into the shift register via the SDI input. An inactive level latches the register data and issues the information to the appropriate circuitry. Active level for SSI 32F8130 is HIGH, for SSI 32F8131 is LOW. |
| SCLK | SERIAL CLOCK. Negative edge triggered clock input for serial register. |
| SDI | SERIAL DATA INPUT. |
| VCA | ANALOG +5 VOLT SUPPLY. |
| VCD | DIGITAL +5 VOLT SUPPLY. |
| AGND | ANALOG GROUND. |
| DGND1 DGND2 | DIGITAL GROUND. |
| VFP | CUTOFF FREQUENCY PROGRAMMING REFERENCE. A resistor of 8.25 kΩ should be connected between this pin and AGND. |

## ELECTRICAL SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may permanently damage the device.

| PARAMETER | RATINGS | UNIT |
|---|---|---|
| Storage Temperature | -65 to +150 | °C |
| Junction Operating Temperature, Tj | +130 | °C |
| Supply Voltage, VCC | -0.5 to 7 | V |
| Voltage Applied to Inputs* | -0.5 to VCC | V |
| T1 Lead Temperature (1/16" from case for 10 seconds) | 260 | °C |

* Analog input signals of this magnitude shall not cause any change or degradation in filter performance after signal has returned to normal operating range.

### RECOMMENDED OPERATING CONDITIONS

| PARAMETER | RATINGS | UNIT |
|---|---|---|
| Supply voltage, VCC | 4.50 < VCC < 5.50 | V |
| Ambient Temperature | 0 < Ta < 70 | °C |
| Tj Junction Temperature | 0 < Tj < 130 | °C |

## ELECTRICAL SPECIFICATIONS (continued)

### ELECTRICAL CHARACTERISTICS

Unless otherwise specified recommended operating conditions apply. F_Code = 64, S_Code = 0.

| PARAMETER | | CONDITIONS | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| Idle Mode Current | | | | | | 1 | mA |
| Isupply | | | | | 60 | 70 | mA |
| Power Dissipation | | PWR_ON ≤ 0.8V | | | | 6 | mW |
| | | PWR_ON ≥ 2.0V | | | 303 | 385 | mW |
| Idle to Active Mode Recovery Time | | | | | | 50 | µs |
| Serial port program to output response time | | | | | | 50 | µs |
| *DC Characteristics* | | | | | | | |
| VIH | High Level Input Voltage | TTL input | | 2.0 | | | V |
| VIL | Low Level Input Voltage | | | | | 0.8 | V |
| IIH | High Level Input Current | VIH = 2.7V | | | | 20 | µA |
| IIL | Low Level Input Current | VIL = 0.4V | | | | –1.5 | mA |
| *Filter Characteristics* | | | | | | | |
| *fc* | Filter Cutoff Frequency | 12 < F_Code < 127 | | | | | |
| | | SSI 32F8130 | | 0.25 | | 2.5 | MHz |
| | | SSI 32F8131 | | 0.15 | | 1.4 | MHz |
| FCA | Filter *fc* Accuracy | over *fc* range | | -10 | | +10 | % |
| Cutoff Resolution | | $\text{Resolution} = \frac{\text{Max fc}}{127}$ | F8130 | | 20 | | kHz |
| | | | F8131 | | 12 | | kHz |
| AO | VO_NORM Diff Gain | F = 0.67 *fc* | | 0.8 | | 1.2 | V/V |
| AD | VO_DIFF Diff Gain | F = 0.67 *fc* | | 1.0 AO | | 1.2 AO | V/V |
| FB | Frequency Boost at *fc* | FB(dB) = 20 log [.01703 (S_Code) + 1] 0 ≤ S_Code ≤ 127 | | 0 | | 10 | dB |
| FBA | Frequency Boost Accuracy | 10 dB nominal | | -1.5 | | +1.5 | dB |
| TGD0 | Group Delay Variation Without Boost | 0.2 *fc* - *fc* | | -2% gdm | | +2% gdm | ns |
| | *fc* = 0.25 - 2.5 MHz | *fc* - 1.75 *fc* | | -3% gdm | | +3% gdm | ns |
| gdm = group delay magnitude | | | | | | | |
| TGDB | Group Delay Variation With Boost | 0.2 *fc* - *fc* | | -2% gdm | | +2% gdm | ns |
| | | *fc* - 1.75 *fc* | | -3% gdm | | +3% gdm | ns |
| Boost Resolution | | | | .25 | | | dB |
| VOF_N | Filter Output Dynamic Range | THD = 1% max, Normal Output | | 1 | | | Vpp |

**ELECTRICAL CHARACTERISTICS** (continued)
Unless otherwise specified recommended operating conditions apply. F_Code = 64, S_Code = 0.

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| *Filter Characteristics* (continued) | | | | | |
| VOF_D Filter Output Dynamic Range | THD = 1% max, Differentiated Output | 1 | | | Vpp |
| RIN Filter Diff Input Resistance | | 3.0 | 4.0 | 5.0 | kΩ |
| CIN Filter Input Capacitance | | | 3.0 | | pF |
| EOUT Output Noise Voltage (VO_NORM) | BW = 100 MHz, 50Ω input, 0 dB Boost | | 1.2 | 1.9 | mVRms |
| | $fc$ = Max $fc$, 10 dB Boost | | 1.4 | 2.0 | mVRms |
| EOUT Output Noise Voltage (VO_DIFF) | BW = 100 MHz, 50Ω input, 0 dB Boost | | 2.1 | 2.7 | mVRms |
| | $fc$ = Max $fc$, 10 dB Boost | | 2.5 | 3.4 | mVRms |
| IO– Filter Output Sink Current | | 1.0 | | | mA |
| IO+ Filter Output Source Current | | 3.0 | | | mA |
| RO Filter Output Resistance (Single ended) | Output source current, IO+ = 1 mA | | 50 | 70 | Ω |
| T1 SDEN Set-up WRT SCLK Falls | | 0 | | | ns |
| T2A SDEN Hold WRT SCLK Falls | | 0 | | | ns |
| T2B SDEN Falls (rises for 8131) prior to SCLK rises | | 25 | | | ns |
| T3 SDI Set-up WRT SCLK Falls | | 25 | | | ns |
| T4 SDI Hold WRT SCLK Falls | | 25 | | | ns |
| SCLK Period, TC | | 100 | | | ns |
| Power Supply Rejection Ratio VO_NORM | 100 mVpp from 10 kHz to 10 MHz on VCA, VCD | 30 | 40 | | dB |
| Power Supply Rejection Ratio VO_DIFF | | 20 | 30 | | dB |
| Common Mode Rejection Ratio VO_NORM | Vin = 0VDC + 10 mVpp from 10 kHz to 10 MHz | 30 | 40 | | dB |
| Common Mode Rejection Ratio VO_DIFF | | 20 | 30 | | dB |
| Bias: VO_NORM± | VCC = 5V | 2.40 | 2.75 | 3.10 | V |
| Vin± | | 2.20 | 2.35 | 2.80 | V |
| VO_DIFF± | | 2.40 | 2.75 | 3.10 | V |
| Normal Output Offset Variation | F_Code switched from 12-127 | -200 | | 200 | mV |
| Differentiated Output Offset Variation | F_Code switched from 12-127 | -200 | | 200 | mV |

**TABLE 1: Calculations**

Typical change in $f$-3 dB point with boost

| Boost (dB) | Gain@$fc$ (dB) | Gain@ peak (dB) | $f$peak/$fc$ | $f$-3dB/$fc$ | K |
|---|---|---|---|---|---|
| 0 | -3 | 0.00 | no peak | 1.00 | 0 |
| 1 | -2 | 0.00 | no peak | 1.21 | 0.16 |
| 2 | -1 | 0.00 | no peak | 1.51 | 0.34 |
| 3 | 0 | 0.15 | 0.70 | 1.80 | 0.54 |
| 4 | 1 | 0.99 | 1.05 | 2.04 | 0.77 |
| 5 | 2 | 2.15 | 1.23 | 2.20 | 1.03 |
| 6 | 3 | 3.41 | 1.33 | 2.33 | 1.31 |
| 7 | 4 | 4.68 | 1.38 | 2.43 | 1.63 |
| 8 | 5 | 5.94 | 1.43 | 2.51 | 1.97 |
| 9 | 6 | 7.18 | 1.46 | 2.59 | 2.40 |
| 10 | 7 | 8.40 | 1.48 | 2.66 | 2.85 |

Notes: 1. $fc$ is the original programmed cutoff frequency with no boost

2. $f$-3 dB is the new -3 dB value with boost implemented

3. $f$peak is the frequency where the amplitude reaches its maximum value with boost implemented

i.e., $fc$ = 1 MHz when boost = 0 dB

if boost is programmed to 5 dB then f-3 dB = 2.20 MHz

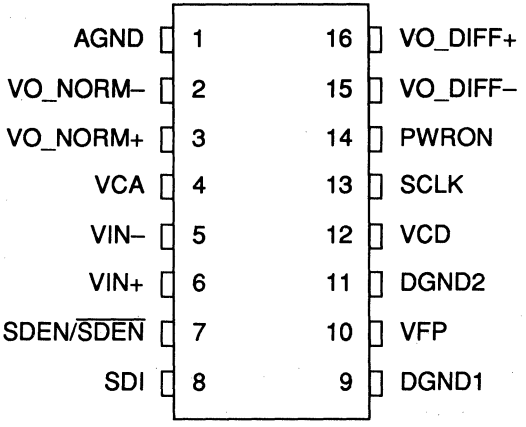
$f$peak = 1.23 MHz

# SSI 32F8130/8131
# Low-Power Programmable Electronic Filter

## PACKAGE PIN DESIGNATIONS
(Top View)

**THERMAL CHARACTERISTICS: θja**

| | |
|---|---|
| 16-Lead SOL | 100° C/W |




**16-Lead SOL**

SSI 32F8130: Pin 7 = SDEN
SSI 32F8131: Pin 7 = $\overline{\text{SDEN}}$

## ORDERING INFORMATION

| PART DESCRIPTION | ORDER NO. | PKG. MARK |
|---|---|---|
| SSI 32F8130 16-Lead SOL | 32F8130-CL | 32F8130-CL |
| SSI 32F8131 16-Lead SOL | 32F8131-CL | 32F8131-CL |



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Section 4

# HDD DATA RECOVERY

silicon systems®
A TDK Group Company

# SSI 32D5371/2/3/4

## Data Synchronization/1, 7 RLL ENDEC with Write Precompensation

**Preliminary Data**

February 1992

4

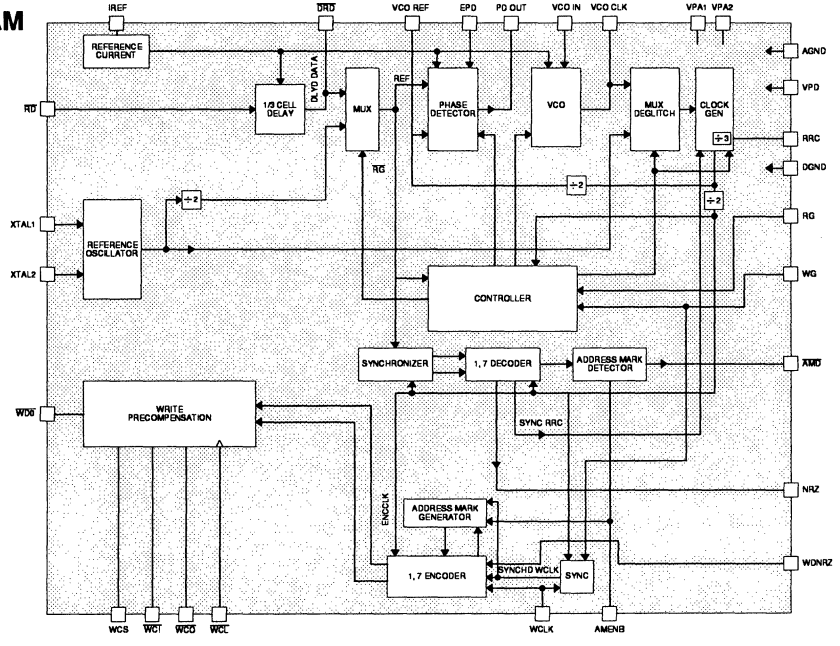
## DESCRIPTION

The SSI 32D537 Data Synchronizer/1, 7 RLL ENDEC family provides data recovery and data encoding for storage systems which employ a 1, 7 RLL encoding format. Data synchronization is performed with a fully integrated high performance PLL. A zero phase restart technique is used to minimize PLL acquisition time. The SSI 32D537 family has been optimized for operation as a companion device to the SSI 32C4650 controller. The VCO frequency setting elements are incorporated within the SSI 32D537 family for enhanced performance and reduced board space. Data rate is established with a single external programming resistor. The SSI 32D5371 family utilizes an advanced bipolar process technology which affords precise decode window control without the requirement of an accurate 1/3 cell delay or external devices. The SSI 32D537 family requires a single +5V supply.

## FEATURES

- **32D5371 – ECL RD Input Option, 10 to 24 Mbit/s**
- **32D5372 – TTL $\overline{RD}$ Input Option, 10 to 24 Mbit/s**
- **32D5373 – TTL $\overline{RD}$ Input Option, 15 to 32 Mbit/s**
- **32D5374 – ECL RD Input Option, 15 to 32 Mbit/s**
- **Data Synchronizer and 1, 7 RLL ENDEC**
- **Data Rate programmed with a single external resistor or current source**
- **Optimized for operation with the SSI 32C4650 controller.**
- **Fast acquisition phase lock loop**
  - **Zero phase restart technique**
- **Fully integrated data separator**
  - **No external delay lines or active devices required**
- **Programmable write precompensation**
- **Hard and soft sector operation**
- **Crystal controlled reference oscillator**
- **+5V operation**
- **28-Pin PLCC & 28-Pin SOL packages**
- **Test outputs - Allow drive margin testing**

## BLOCK DIAGRAM



## OPERATION

The SSI 32D5371, 32D5372, 32D5373, 32D5374 product family, hereafter designated as the 32D537X, are designed to perform data recovery and data encoding in rotating memory systems which utilize a 1,7 RLL encoding format. In the Read Mode the SSI 32D5367X performs Data Synchronization, Sync Field Search and Detect, Address Mark Detect, and Data Decoding. In the Write Mode, the SSI 32D537X converts NRZ data into the 1,7 RLL format described in Table 1, performs Write Precompensation, and inserts Address Marks as requested. The interface electronics and architecture of the SSI 32D537X have been optimized for use as a companion device to the SSI 32C9000 controller.

The SSI 32D537X can operate with data rates ranging from 10 to 32 Mbit/s. This data rate is established by a single 1% external resistor, RR, connected from pin IREF to VPA. This resistor establishes a reference current which sets the VCO center frequency, the phase detector gain, and the 1/3 cell delay. The value of this resistor is given by:

$$\text{32D5371/5372: } RR = \frac{92.6}{DR} - 1.7\,(k\Omega)$$

$$\text{32D5373/5374: } RR = \frac{139}{DR} - 1.7\,(k\Omega)$$

where: DR = Data Rate in Mbit/s.

An internal crystal reference oscillator, operating at three times the data rate, generates the standby reference for the PLL. A series resonant crystal between XTAL1 and XTAL2 should be selected at three times the Data Rate. If a crystal oscillator is not desired, then an AC coupled ECL source may be applied to XTAL1, leaving XTAL2 open. A TTL compatible reference may also be used if suitably attenuated and AC coupled.

The SSI 32D537X employs a Dual Mode Phase Detector; Harmonic in the Read Mode and Non Harmonic in Write and Idle Modes. In the Read Mode the Harmonic Phase Detector updates the PLL with each occurrence of a DYLD DATA pulse. In the Write and Idle modes the Non-Harmonic Phase Detector is continuously enabled, thus maintaining both phase and frequency lock. By acquiring both phase and frequency lock to the crystal reference oscillator and utilizing a zero phase restart technique, false lock to DLYD DATA is eliminated.

The phase detector incorporates a charge pump in order to drive the loop filter directly. The polarity and width of the output current pulses correspond to the direction and magnitude of the phase error.

The READ GATE (RG), and WRITE GATE (WG) inputs control the device mode.

RG is an asynchronous input and may be initiated or terminated at any position on the disk. WG is also an asynchronous input, but should not be terminated prior to the last output Write Data pulse.

### READ OPERATION

The Data Synchronizer utilizes a fully integrated fast acquisition PLL to accurately develop the decode window. Read Gate, RG, initiates the PLL locking sequence and selects the PLL reference input; a high level (Read Mode) selects the $\overline{RD}$ input and a low level selects the crystal reference oscillator.

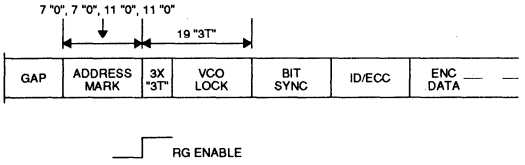
In the Read Mode the falling edge of $\overline{DRD}$ enables the Phase Detector while the rising edge is phase compared to the rising edge of the VCO/2. As depicted in Figure 1, $\overline{DRD}$ is a 1/3 cell wide (TVCO) pulse whose leading edge is defined by the leading edge of $\overline{RD}$. An accurate and symmetrical decode window is developed from the VCO/2 clock. By utilizing a fully integrated symmetrical VCO running at three times the data rate, the decode window is insured to be accurate and centered symmetrically about the rising edges of $\overline{DRD}$. The accuracy of the 1/3 cell delay only affects the retrace angle of the phase detector and does not influence the accuracy of the decode window.

In Non-Read Modes, the PLL is locked to the crystal reference oscillator. This forces the VCO to run at a frequency which is very close to that required for tracking actual data and thus minimizes the associated frequency step during acquisition. When the reference input to the PLL is switched, the VCO is stopped momentarily, then restarted in an accurate phase alignment with the next PLL reference input pulse, and the VCO clock divider is reset. By minimizing the phase alignment in this manner the acquisition time is substantially reduced.

After Read Mode is terminated (RG low), the VCO and RRC sources switch from $\overline{RD}$ and VCO/3, respectively, to the reference crystal. After a delay of one NRZ bit time (minimum) from when RG is low, write gate (WG) may be enabled (see figure 7 for timing diagram). NRZ is a tri-statable pin controlled by RG. NRZ will change states within one NRZ bit time. The NRZ pin can be connected to WDNRZ to form a bi-directional port.

### SOFT SECTOR OPERATION

Disk Operation Lock Sequence in Read Mode Soft Sector Operation




### ADDRESS MARK DETECT

In Soft Sector Read Operation the SSI 32D537X must first detect an address mark to be able to initiate the rest of the read lock sequence. An address mark for the SSI 32D537X consists of two (2) 7 "0" patterns followed by two 11 "0" patterns. To begin the read lock sequence the Address Mark Enable (AMENB) is asserted high by the controller. The SSI 32D537X Address Mark Detect ($\overline{AMD}$) circuitry then initiates a search of the read data ($\overline{RD}$) for an address mark. First the $\overline{AMD}$ looks for a set of 6 "0's" within the 7 "0" patterns. Having detected a 6 "0" the $\overline{AMD}$ then looks for a 9 "0" set within the 11 "0's." If $\overline{AMD}$ does not detect 9 "0's" within 5 $\overline{RD}$ bits after detecting 6 "0's" it will restart the Address Mark Detect sequence and look for 6 "0's." When the $\overline{AMD}$ has acquired a 6 "0," 9 "0" sequence the $\overline{AMD}$ transitions low disabling AMENB input. When AMENB is released, $\overline{AMD}$ will be released and reset by the SSI 32D537X. The AMENB should be released prior to entering Read Mode.

### PREAMBLE SEARCH

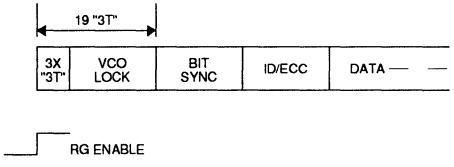
After the Address Mark (AM) has been detected, Read Gate (RG) can be asserted initiating the remainder of the read lock sequence. When RG is asserted an internal counter counts negative transitions of the incoming Read Data ($\overline{RD}$) looking for (3) consecutive negative transitions. Once the counter reaches count 3 (finds (3) consecutive negative transistors) the internal read gate switches the phase detector input from the reference oscillator to the Delayed Read Data ($\overline{DRD}$); at the same time a zero phase (internal) restart signal restarts the VCO in phase with the Delayed Read Data. This prepares the VCO to be synchronized to data when the bit sync circuitry is enabled after VCO lock is established.

### VCO LOCK & BIT SYNC ENABLE

When the internal counter counts 16 more negative transitions or a total of 19 "3T's" from RG enable, an internal VCO lock signal enables. The VCO lock signal activates the decoder bit synchronization circuitry to define the proper decode boundaries. Also, at the count of 19, the RRC source switches from the reference oscillator to VCO clock signal which is phase locked to $\overline{DRD}$. The VCO is assumed locked at this point. The bit sync circuitry searches for a '1001001' pattern to align the proper decode boundaries. During this time, an RRC pulse may be stretched a maximum of 2 RRC time periods during the alignment process to prevent any glitches.

### HARD SECTOR OPERATION

Disk Operation Lock Sequence in Read Mode Hard Sector Operation




In hard sector operation a low AMENB disables the SSI 32D537X's Address Mark Detection circuitry and $\overline{AMD}$ remains inactive. A hard sector read operation does not require an address mark search but starts with a preamble search as with soft sector and sequences identically. In all respects, with the exception of the address mark search sequence, hard sector read operation is the same as soft sector read.

### WRITE MODE

In the write mode the SSI 32D537X converts NRZ data from the controller into 1,7 RLL formatted data for storage on the disk. The SSI 32D537X can operate with a soft or hard sector hard drive.

Serial NRZ data is clocked into the SSI 32D537X and latched on defined cell boundaries. The NRZ input data must be synchronous with the rising edges of the WCLK input. The WCLK input is a feature provided for operation in an ESDI application to compensate for large cable delays. In SCSI or IDE operation, WCLK is connected directly to the RRC output.

Write precompensation circuitry is provided to compensate for intersymbol interference caused by media bit shift. The SSI 32D537X recognizes specific write data patterns and can add or subtract delays in the time position of write data bits to counteract the read back bit shift. The magnitude of the time shift, TPC, is determined by an external register on the WCS pin where the register is connected from WCS to VPA1.

When the write precompensation control latch, $\overline{WCL}$ is low, the SSI 32D537X performs write precompensation according to the algorithm outlined in Table 4.

### SOFT SECTOR

In soft sector operation, when Write Gate (WG) is asserted, the NRZ input (WDNRZ) must be kept low. To generate an Address Mark (consisting of 7 "0's", 7 "0's", 11 "0's", 11 "0's") the Address Mark Enable (AMENB) is toggled high for a minimum of 1 NRZ bit time. The toggling of AMENB must occur at least 1 NRZ bit time after WG is asserted. After the address mark is generated, WDNRZ must be kept low for an additional 44 NRZ bits to properly generate 19 x '3T' for the preamble plus three '3T' for the bit sync field. Data can then be written on the WDNRZ line with the encode data appearing on $\overline{WD}$ 5 NRZ bit times later. After writing is complete, WG should be held high for an additional 5 NRZ bit times to ensure that the encoder is flushed. See Figure 9 for timing diagram.

### HARD SECTOR

After WG is asserted, WDNRZ must be kept low for a minimum of 44 NRZ bit times to ensure a preamble field of at least 19 x "3T" plus 3 x "3T" for the bit sync field. Data can then be written as in the soft sector operation.

### TEST POINTS

The SSI 32D537X provides three (3) test points which can be utilized to evaluate window margin characteristics.

(a) $\overline{DRD}$, delayed read data – the positive edges represent the data bit position

(b) VCO REF, the VCO reference which represents the input to the Phase Detector, synchronizer, and 1,7 decoder

(c) VCO CLK, the VCO clock output which represents the output of the VCO

The following figure describes the relationship between the various test points:

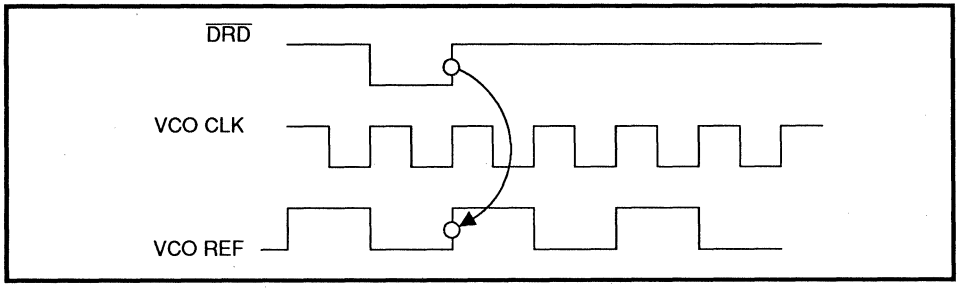



**FIGURE 1: Test Point Relationships**

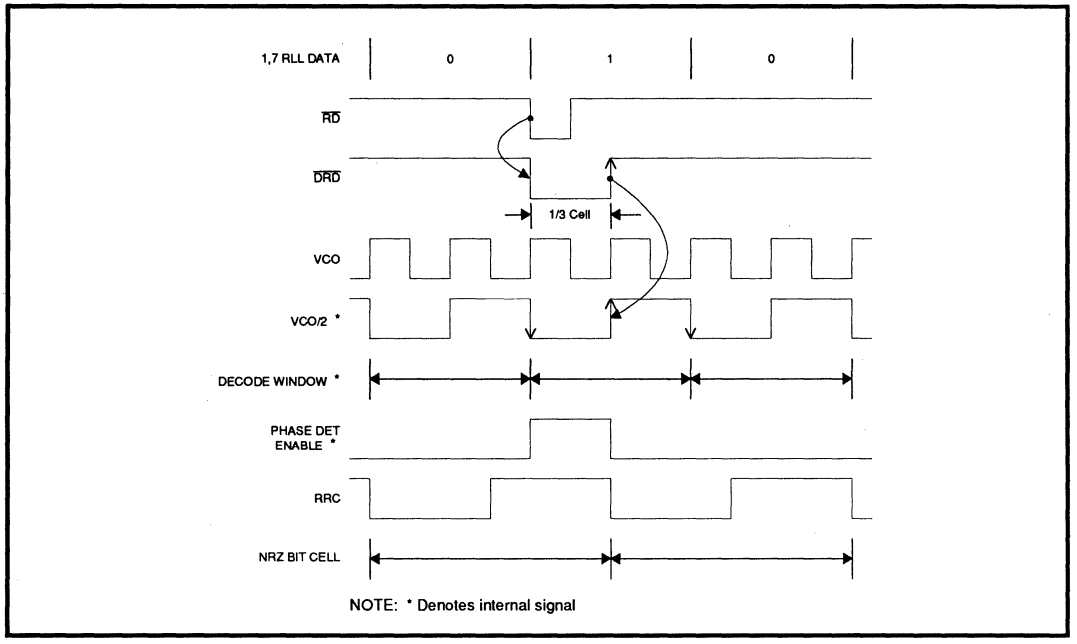



**FIGURE 2: Data Synchronization Waveform**

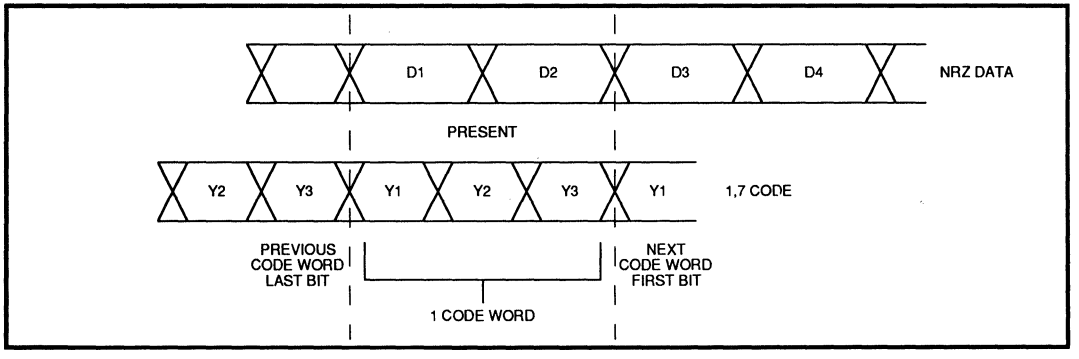



**FIGURE 3: NRZ Data Word Comparision to 1, 7 Code Word (See Tables 1, and 2 for Decode Scheme)**

**TABLE 1: Decode Table for (1, 7) RLL Code Set**

| ENCODED READ DATA | | | DECODED DATA | |
|---|---|---|---|---|
| Previous | Present | Next | | |
| Y Y | Y Y Y | Y Y | D D | |
| 2' 3' | 1 2 3 | 1 2 | 1 2 | |
| 0 0 | 0 0 0 | X X | 0 1 | |
| 1 0 | 0 0 0 | X X | 0 0 | |
| 0 1 | 0 0 0 | X X | 0 1 | |
| X X | 1 0 0 | X X | 1 1 | |
| X 0 | 0 1 0 | 0 0 | 1 1 | |
| X 0 | 0 1 0 | 1 0 | 1 0 | |
| X 0 | 0 1 0 | 0 1 | 1 0 | |
| X 1 | 0 1 0 | 0 0 | 0 1 | |
| X 1 | 0 1 0 | 1 0 | 0 0 | |
| X 1 | 0 1 0 | 0 1 | 0 0 | |
| 0 0 | 0 0 1 | X X | 0 1 | |
| 1 0 | 0 0 1 | X X | 0 0 | |
| 0 1 | 0 0 1 | X X | 0 0 | (Preamble) |
| X X | 1 0 1 | X X | 1 0 | |

**TABLE 2: Encode Table for (1, 7) RLL Code Set**

| NRZ DATA | | | | ENCODED WRITE DATA | | | |
|---|---|---|---|---|---|---|---|
| Present | | Next | | Previous | Present | | |
| D | D | D | D | Y | Y | Y | Y |
| 1 | 2 | 3 | 4 | 3 | 1 | 2 | 3 |
| 0 | 0 | 0 | X | X | 0 | 0 | 1 |
| 0 | 0 | 1 | X | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | X | 1 | 0 | 1 | 0 |
| 1 | 0 | 0 | X | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | X | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 |

NOTE: X = Don't Care

**TABLE 3: Clock Frequency**

| WG | RG | VCO REF | RRC | DECCLK | ENCCLK | MODE |
|---|---|---|---|---|---|---|
| 0 | 0 | XTAL/2 | XTAL/3 | XTAL/2 | XTAL/2 | IDLE |
| 0 | 1 | $\overline{RD}$ | VCO/3 | VCO/2 | XTAL/2 | READ |
| 1 | 0 | XTAL/2 | XTAL/3 | XTAL/2 | XTAL/2 | WRITE |
| 1 | 1 | XTAL/2 | XTAL/3 | XTAL/2 | XTAL/2 | IDLE |

Note 1: Until the VCO locks to the new source, the VCO/2 entries will be XTAL/2.

2: Until the VCO locks to the new source, the VCO/3 entries will be XTAL/3.

**TABLE 4: Write Precompensation Algorithm**

| BIT | BIT | BIT | BIT | BIT | COMPENSATION |
|---|---|---|---|---|---|
| n-2 | n-1 | n | n+1 | n+2 | BIT n |
| 1 | 0 | 1 | 0 | 1 | NONE |
| 0 | 0 | 1 | 0 | 0 | NONE |
| 1 | 0 | 1 | 0 | 0 | EARLY |
| 0 | 0 | 1 | 0 | 1 | LATE |

LATE: Bit n is time shifted (delayed) from its nominal time position towards the bit n+1 time position.

EARLY: Bit n is time shifted (advanced) from its nominal time position towards the bit n-1 time position.

**TABLE 5: Write Precompensation Magnitude**

| $\overline{WCI}$ | $\overline{WCO}$ | MAGNITUDE (WP) |
|---|---|---|
| 0 | 0 | 3 |
| 0 | 1 | 2 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

The nominal magnitude,
TPC = WP x TPC0 is externally set with resistors on pins WCS and IREF.

## PIN DESCRIPTION

### INPUT PINS

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| $\overline{RD}$ (TTL)<br>RD (ECL) | I | READ DATA: Encoded Read Data from the disk drive read channel. The TTL input version (5372/5373) is an active low signal. The ECL input version (5371/5374) is an active high signal. |
| RG | I | READ GATE: Selects the PLL reference input (REF), see Table 2. A change in state on RG initiates the PLL synchronization sequence. Pin RG has an internal resistor pullup. |
| WG | I | WRITE GATE: Enables the write mode, see Table 2. Pin WG has an internal resistor pullup. |
| WCLK | I | WRITE CLOCK: Write Clock input. Must be synchronous with the NRZ Write Data input. For small cable delays, WCLK may be connected directly to pin RRC. |
| EPD | I | ENABLE PHASE DETECTOR: A low level (Coast Mode) disables the phase detector and enables the test mode. This opens the PLL and the VCO will run at the frequency commanded by the voltage on pin VCO IN. In the test mode, functions normally driven by the VCO are switched to XTAL. Pin EPD has an internal resistor pull up. |
| AMENB | I | ADDRESS MARK ENABLE: Used to enable the address mark detection and address mark generation circuitry, active high. Pin AMENB has an internal resistor pullup. |
| $\overline{WC0}$, $\overline{WC1}$ | I | WRITE PRECOMPENSATION CONTROL BITS: Pins $\overline{WC1}$, and $\overline{WC0}$ control the magnitude of the write precompensation, see Table 4. Internal resistor pull ups are provided. If unused, leave pins open or tie high. |
| $\overline{WCL}$ | I | WRITE PRECOMPENSATION CONTROL LATCH: Used to latch the write precompensation control bits $\overline{WC1}$ and $\overline{WC0}$ into the internal DAC. An active low level latches the input bits. Pin $\overline{WCL}$ has an internal resistor pull up. If unused, leave pin open or tie high. |
| WDNRZ | I | NRZ WRITE DATA INPUT PIN: This pin can be connected to the NRZ pin to form a bidirectional data port. |

### OUTPUT PINS

| | | |
|---|---|---|
| $\overline{WD0}$ | O | WRITE DATA: Encoded write data output, active low. The data is automatically resynchronized (independent of the delay between RRC and WCLK) to one edge of the XTAL1 input clock. |
| RRC | O | READ/REFERENCE CLOCK: A multiplexed clock source used by the controller, see Table 2. During a mode change, no glitches are generated and no more than two lost clock pulses will occur. When RG goes high, RRC is synchronized to the NRZ Read Data after 19 read data pulses. |
| $\overline{AMD}$ | O | ADDRESS MARK DETECT: Tristate output pin that is in its high impedance state when WG is high or AMENB is low. A latched low level output indicates that an address mark has been detected. A low level on pin AMENB resets pin $\overline{AMD}$. |

**OUTPUT PINS** (Continued)

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| VCO REF | O | VCO REFERENCE: An open emitter ECL output test point. The VCO reference input to the phase detector, the positive edges are phase locked to DLYD DATA. The negative edges of this open emitter output signal indicate the edges of the decode window. Two external resistors are required to perform this test, they should be removed during normal operation for reduced power dissipation. |
| VCO CLK | O | VCO CLOCK: An open emitter ECL output test point. Two external resistors are required to perform this test. They should be removed during normal operation for reduced power dissipation. |
| $\overline{\text{DRD}}$ | O | DELAYED READ DATA: An open emitter ECL output test point. The positive edges of this open emitter output signal indicates the data bit position. The positive edges of the $\overline{\text{DRD}}$ and the VCO REF signals can be used to estimate window centering. The time jitter of DRD's positive edge is an indication of media bit shift. Two external resistors are required to perform this test. They should be removed during normal operation for reduced power dissipation. |
| NRZ | O | NRZ READ DATA OUTPUT: Tristate output pin that is enabled when read gate is high. This pin can be connected to the WDNRZ pin to form a bidirectional data port. |

**ANALOG PINS**

| | | |
|---|---|---|
| IREF | I | TIMING PROGRAM PIN: The VCO center frequency and the 1/3 cell delay are a function of the current sourced into pin IREF. The current is set by an external resistor, RR, connected between pin IREF and VPA2. |
| XTAL1, 2 | I | CRYSTAL OSCILLATOR CONNECTIONS: The pin frequency is at three times the data rate. If the crystal oscillator is used, an AC coupled parallel LC circuit must be connected from XTAL1 to ground. If the crystal oscillator is not desired, XTAL1 may be driven either by an AC coupled suitably attenuated TTL source or by an AC coupled ECL source, with XTAL2 open. The source duty cycle should be as close to 50% as possible, since its duty cycle will affect the RRC clock duty cycle when XTAL is its source. The additional RRC duty cycle error will be one third the source duty cycle error. |
| PD OUT | O | PHASE DETECTOR OUTPUT: Drives the loop filter input. |
| VCO IN | I | VCO CONTROL INPUT: Driven by the loop filter output. |
| WCS | I | WRITE PRECOMPENSATION SET: Pin for a resistor to program the write precompensation magnitude value. The resistor, RC, is connected between pin WCS and VPA2. If this pin is left open, write precompensation is disabled. |
| DGND, AGND | I | Digital and Analog Ground |
| VPA1, VPA2 | I | Analog +5V Supplies |
| VPD | I | Digital +5V Supply |

## ELECTRICAL SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may damage the device.

| PARAMETER | RATING | UNIT |
|---|---|---|
| Storage Temperature | -65 to + 150 | °C |
| Junction Operating Temperature, Tj | +150 | °C |
| Supply Voltage, VPA1, VPA2, VPD | -0.5 to 7 | V |
| Voltage Applied to Logic Inputs | -0.5 to VPD + 0.5 | V |
| Maximum Power Dissipation | 0.9 | W |

### RECOMMENDED OPERATING CONDITIONS

| | | |
|---|---|---|
| Supply Voltage, VPA1 = VPA2 = VPD = VCC | 4.75 < VCC < 5.25 | V |
| Junction Temperature, Tj | 0 < Tj < 135 | °C |
| Ambient Temperature, Ta | 0 < Ta < 70° | °C |

### ELECTRICAL CHARACTERISTICS

Unless otherwise specified, 4.75V < VCC < 5.25V, 10 MHz < 1/TORC < 24 MHz, 30 MHz < 1/TVCO < 72 MHz (32D5371/5372), 15 MHz < 1/TORC < 32 MHz, 45 MHz < 1/TVCO < 96 MHz (32D5373/5374), 0 °C < Ta < 70 °C.

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| VIH | High Level Input Voltage | | 2.0 | | | V |
| VIL | Low Level Input Voltage | | | | 0.8 | V |
| IIH | High Level Input Current | VIH = 2.7V | | | 20 | µA |
| IIL | Low Level Input Current | VIL = 0.4V | | | -0.36 | mA |
| VOH | High Level Output Voltage | IOH = 400 µA | 2.4 | | | V |
| VOL | Low Level Output Voltage | IOL = 4 mA | | | 0.5 | V |
| VIHP | Pseudo ECL High Level Input Voltage; RD | Ta = 25°C | VCC-1.0 | | | V |
| VILP | Pseudo ECL Low Level Input Voltage; RD | Ta = 25°C | | | VCC-1.5 | V |
| IIHP | Pseudo ECL High Level Input Current; RD | VIH = VCC -0.8V | | | 2.0 | mA |
| IILP | Pseudo ECL Low Level Input Current; RD | VIL = VCC -1.5V | | | 1.6 | mA |
| ICC | Power Supply Current | All outputs & test point pins open | | | 160 | mA |
| PWR | Power Dissipation | All outputs & test point pins open | | | 0.84 | W |

**ELECTRICAL CHARACTERISTICS** (Continued)

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| VOHT | Test Point Output High Level $\overline{DRD}$, VCO CLK, VCO REF | 262Ω to VPD<br>402Ω to DGND<br>VPD = 5.0V<br>VOHT - VPD | | -0.85 | | V |
| VOLT | Test Point Output Low Level $\overline{DRD}$, VCO CLK, VCO REF | 262Ω to VPD<br>402Ω to DGND<br>VPD = 5.0V<br>VOLT - VPD | | -1.75 | | V |

**DYNAMIC CHARACTERISTICS AND TIMING**

**READ MODE** (See Figure 3)

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| TRD | Read Data Pulse Width | | 12 | | 4/3TORC-20 | ns |
| TFRD | Read Data Fall Time | 2.0V to 0.8V, $C_L \leq 15$ pF | | | 9 | ns |
| TRRC | Read Clock Rise Time | 0.8V to 2.0V, $C_L \leq 15$ pF | | | 8 | ns |
| TFRC | Read Clock Fall Time | 2.0V to 0.8V, $C_L \leq 15$ pF | | | 5 | ns |
| RRC | Duty Cycle | 10 - 20 Mbit/s | 43 | 50 | 57 | % |
| | | >20 - 32 Mbit/s | 40.8 | 50 | 59.2 | % |
| TPNRZ | NRZ (out) Set Up/ Hold Time | 10 - 20 Mbit/s | 15.5 | | | ns |
| | | >20 - 24 Mbit/s | 13 | | | ns |
| | | >24 - 32 Mbit/s | 10 | | | ns |
| KD | Decode Window Centering Accuracy | | | ±1.5 | ns | |
| | Decode Window | | 2TORC/3) - 1.5 | | ns | |

**WRITE MODE** (See Figure 4)

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| TWD | Write Data Pulse Width | $C_L \leq 15$ pF | 2TOWC/3 -TPC -5 | | 2TOWC/3 +TPC +5 | ns |
| TFWD | Write Data Fall Time | 2.0V to 0.8V, $C_L \leq 15$ pF | | | 5 | ns |
| TRWC | Write Data Clock Rise Time | 0.8V to 2.0V | | | 10 | ns |
| TFWC | Write Data Clock Fall Time | 2.0V to 0.8V | | | 8 | ns |
| TSNRZ | WDNRZ Set up Time | | 5 | | | ns |
| THNRZ | WDNRZ Hold Time | | 5 | | | ns |

**WRITE MODE** (Continued)

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| TPC | Precompensation Time Shift Magnitude Accuracy | TPCO = 1.12T x A / (B + 3A)<br>T = XTAL Period<br>A = 0.19 / (Rc + 0.51) + 5.8E-3<br>B = 0.42 / (RR + 0.53) + 1.08E-2<br>$RC = \frac{0.19(1-2.7S)}{S[\frac{0.38}{RR+0.53)} + 0.025] - 0.006} - 0.51$<br>S = TPCO/T; RR, RC (kΩ)<br>(Rc tied between WCS and +5V) | | | | |
| | | $\overline{WC0}$ = 1, $\overline{WC1}$ = 1 | 0 | 0 | | ns |
| | | $\overline{WC0}$ = 0, $\overline{WC1}$ = 1 | | TPCO | | ns |
| | | $\overline{WC0}$ = 1, $\overline{WC1}$ = 0 | | 2TPCO | | ns |
| | | $\overline{WC0}$ = 0, $\overline{WC1}$ = 0 | | 3TPCO | | ns |

**DATA SYNCHRONIZATION** VCC = 5.0V; 32D5371/2: 2.15k ≤ RR ≤ 7.6k; 32D5373/4: 2.60k ≤ RR ≤ 7.6k

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| TVCO | VCO Center Frequency Period | VCO_IN = 2.7V<br>32D5371/5372 TO = 3.6 (RR + 1.7)<br>32D5373/5374 TO = 2.4 (RR + 1.7) | 0.8 TO | | 1.2 TO | ns |
| VCO | Frequency Dynamic Range | 1V ≤ VCO_IN ≤ VCC-0.6V | ±25 | | ±45 | % |
| KVCO | VCO Control Gain | ωo = 2π/TVCO<br>1V ≤ VCO_IN ≤ VCC 0.6V | 0.14 ωo | | 0.26 ωo | rad/s-V |
| KD | Phase Detector Gain* | KD= 0.66/(RR+530) Read Mode<br>= 0.33/(RR+530) Non-Read Mode<br>Indirectly tested | 0.83 KD | | 1.17 KD | μA/rad |
| | KVCO x KD Product Accuracy* | Indirectly tested | -28 | | -28 | % |
| | VCO Phase Restart Error* | Referred to RRC<br>Indirectly tested | -1 | | 1 | rad |
| TPAMD | $\overline{AMD}$ Propogation Delay | 10 - 24 Mbit/s<br>>24 - 32 Mbit/s | 13<br>10 | | | ns<br>ns |
| | 1/3 Cell Delay | TD = 3.6 (RR+1.7): 32D5371/2<br>TD = 2.4 (RR+1.7): 32D5373/4 | 0.8TD | | 1.2TD | ns |

**CONTROL CHARACTERISTICS** (See Figure 5)

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| TSWS | $\overline{WC0}$, $\overline{WC1}$ SET UP TIME | | 7 | | | ns |
| THWS | $\overline{WC0}$, $\overline{WC1}$ HOLD TIME | | 7 | | | ns |

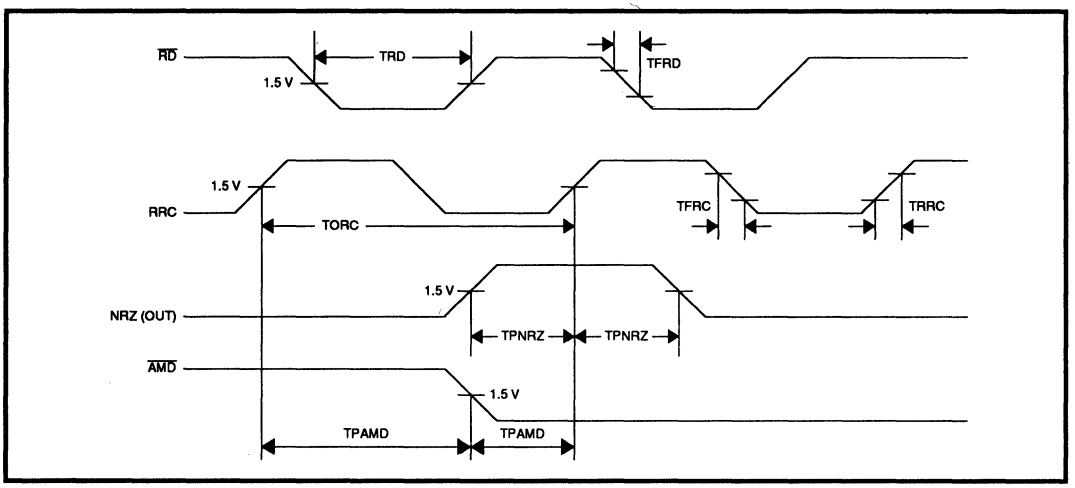



**FIGURE 3: Read Timing**

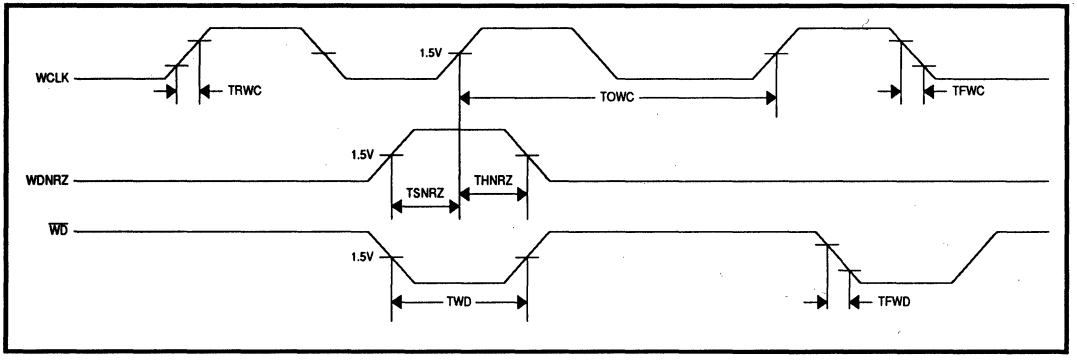



**FIGURE 4: Write Timing**

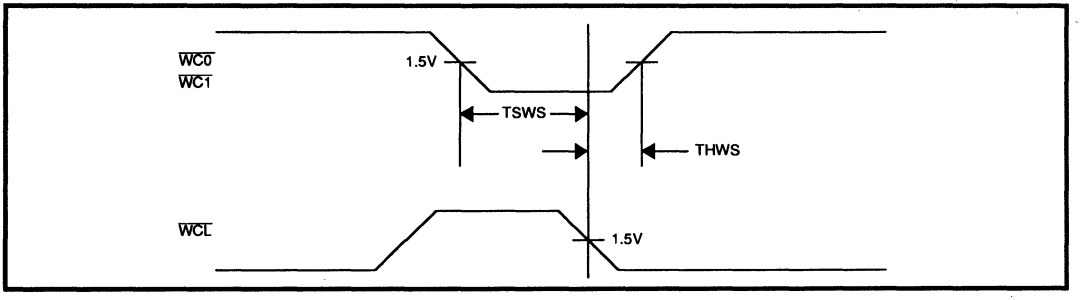



**FIGURE 5: Control Timing**

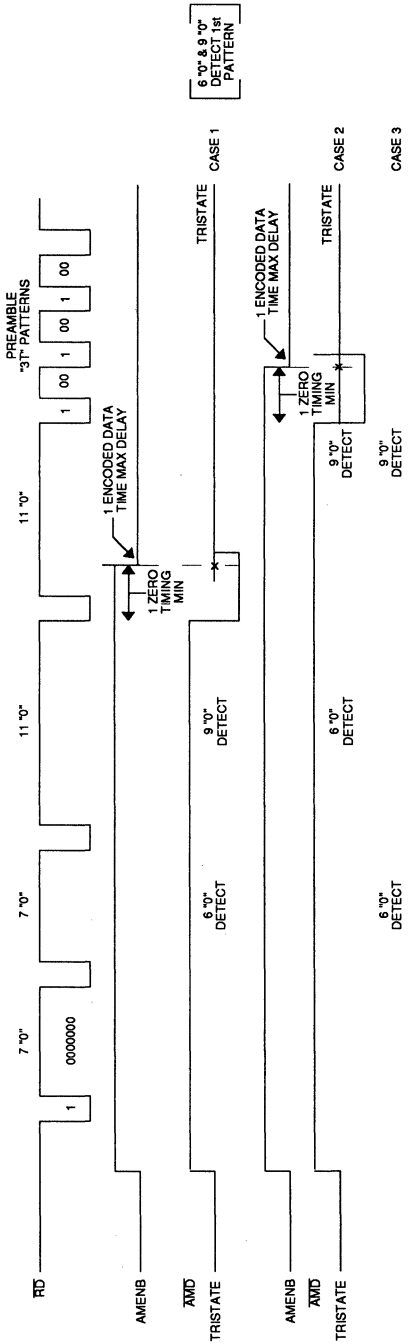



**FIGURE 6: Address Mark Search**

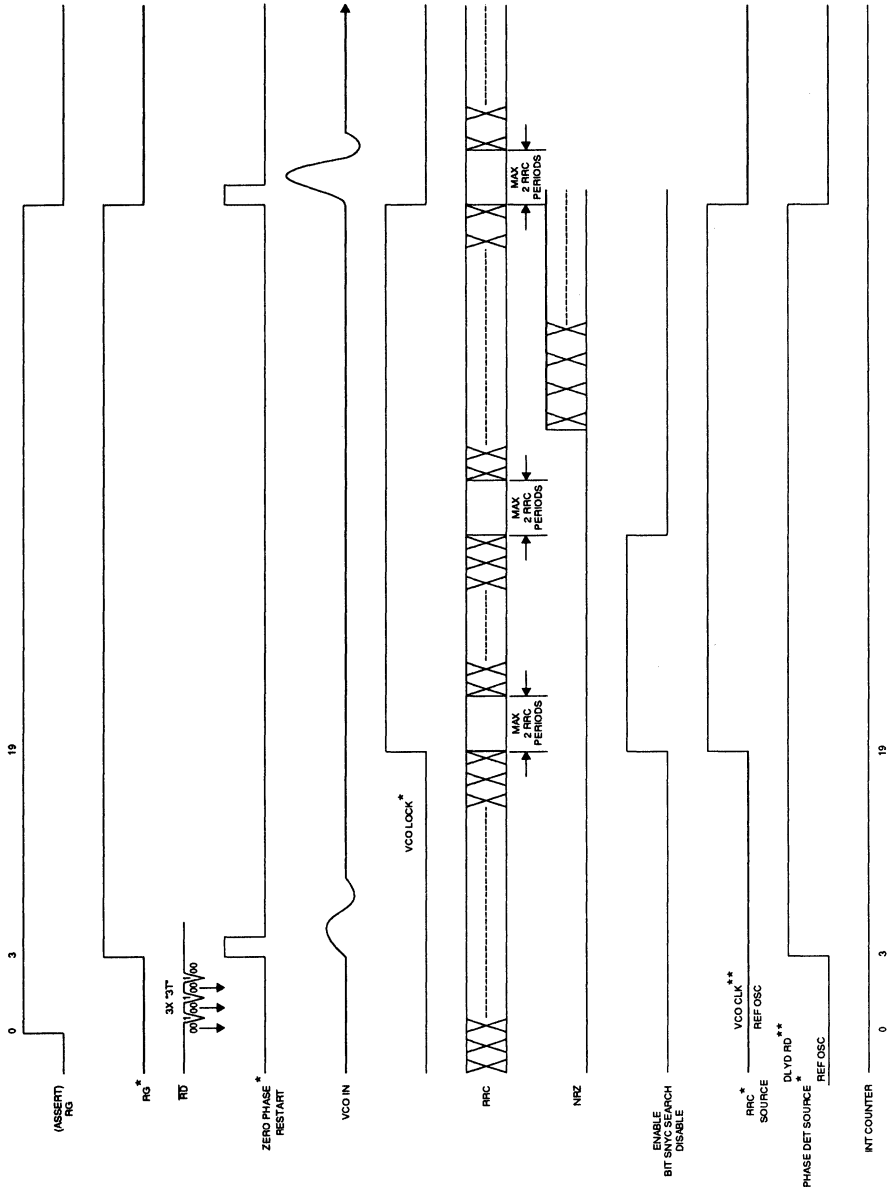



FIGURE 7: Read Mode Locking Sequence (Soft and Hard Sector)

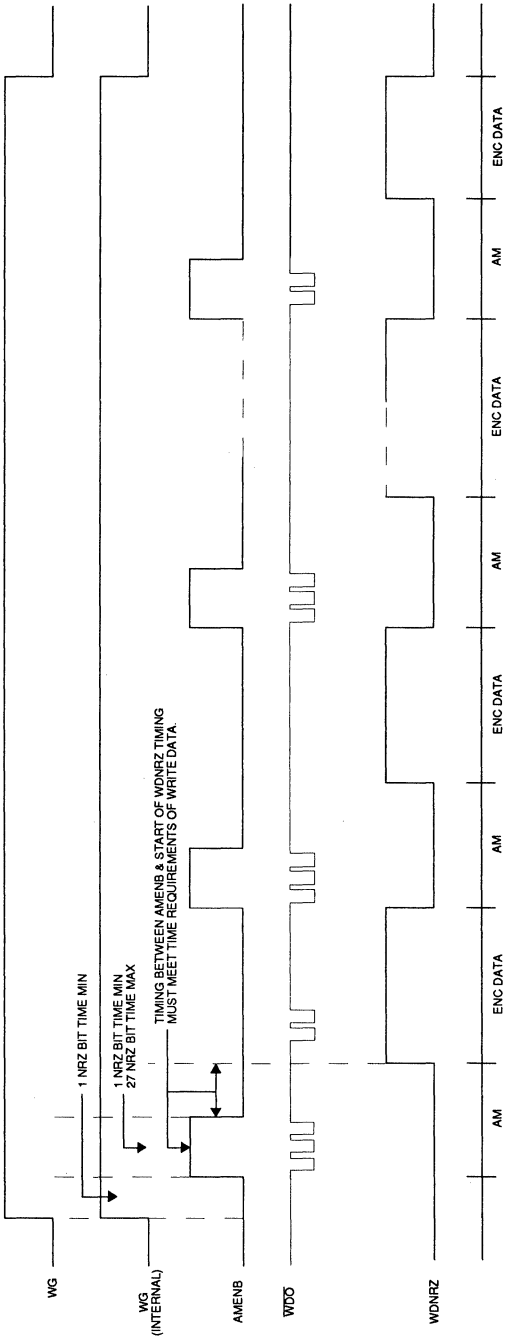



**FIGURE 8: Multiple Address Mark Write**

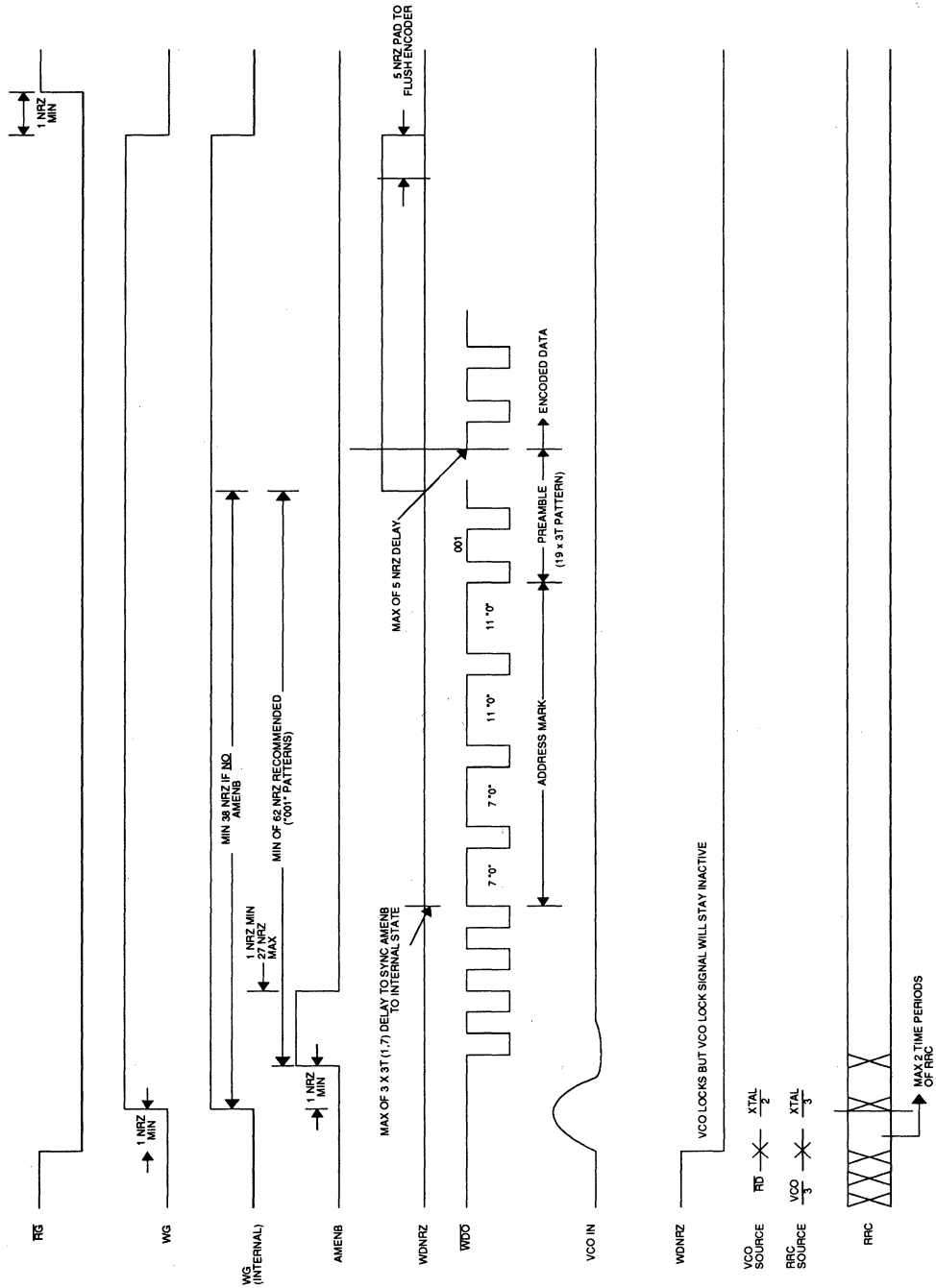
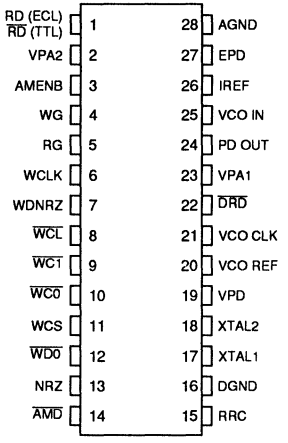



**FIGURE 9: Write Data**

# SSI 32D5371/2/3/4
# Data Synchronization/1, 7 RLL ENDEC with Write Precompensation

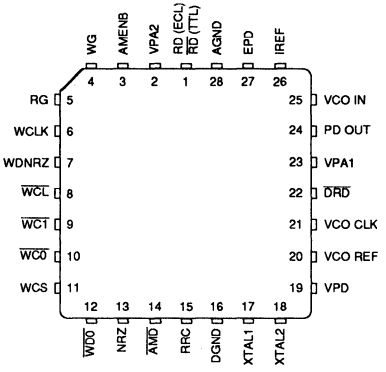
## PACKAGE PIN DESIGNATIONS

(Top View)




28-Pin SOL

CAUTION: Use handling procedures necessary for a static sensitive component.




28-Pin PLCC

## ORDERING INFORMATION

| PART DESCRIPTION | ORDERING NUMBER | PACKAGE MARK |
|---|---|---|
| SSI 32D5371 Data Synchronization/1, 7 RLL ENDEC with Write Precompensation | | |
| 28-Pin SOL | 32D5371-CL | 32D5371-CL |
| 28-PIN PLCC | 32D5371-CH | 32D5371-CH |
| SSI 32D5372 Data Synchronization/1, 7 RLL ENDEC with Write Precompensation | | |
| 28-Pin SOL | 32D5372-CL | 32D5372-CL |
| 28-PIN PLCC | 32D5372-CH | 32D5372-CH |
| SSI 32D5373 Data Synchronization/1, 7 RLL ENDEC with Write Precompensation | | |
| 28-Pin SOL | 32D5373-CL | 32D5373-CL |
| 28-PIN PLCC | 32D5373-CH | 32D5373-CH |
| SSI 32D5374 Data Synchronization/1, 7 RLL ENDEC with Write Precompensation | | |
| 28-Pin SOL | 32D5374-CL | 32D5374-CL |
| 28-PIN PLCC | 32D5374-CH | 32D5374-CH |

**Preliminary Data:** Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.



Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 573-6000, FAX (714) 573-6914

silicon systems®
A TDK Group Company

# SSI 32D539
## Data Synchronizer & 1, 7 RLL ENDEC
## Preliminary Data

December 1991

4

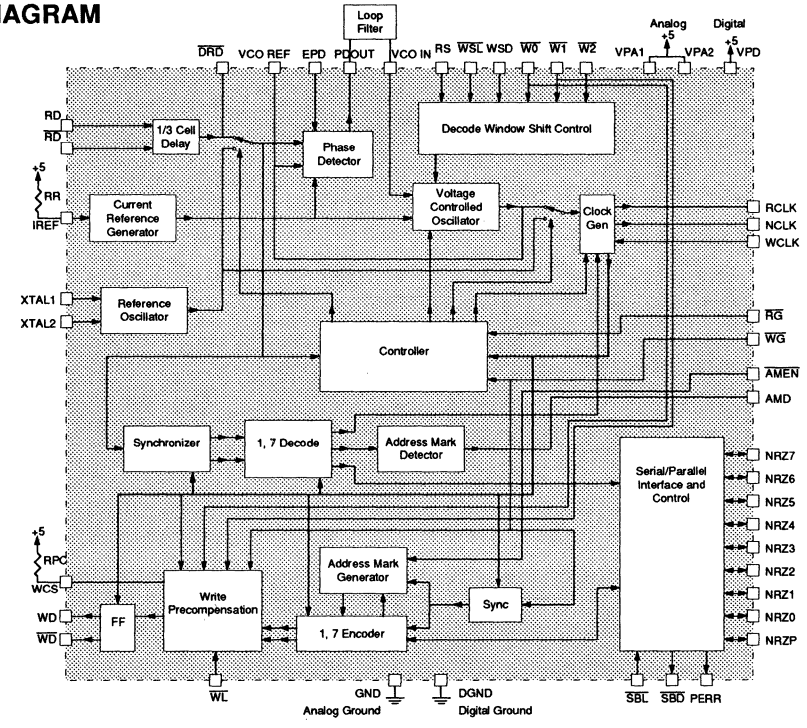
## DESCRIPTION

The circuit is intended to be used as a data/clock recovery circuit for 1, 7 RLL code in hard disk drive systems with a +5V supply.

## FEATURES

- **Data synchronizer and 1, 7 RLL ENDEC**
- **9-bit bi-directional data bus interface**
  - **8 data bits plus 1 parity bit**
  - **Parity generation during read operation**
  - **Parity checking during write operation**
- **Up to 48 Mbit/s operation**
  - **Data rate programmed with a single external resistor or current source**
- **Programmable Sync-Byte pattern detection**
- **Fast acquisition phase locked loop with zero phase restart technique**
- **Fully integrated data separator**
  - **No external delay lines or active devices required**
- **Programmable decode window symmetry control**
  - **Includes delayed read data and VCO clock monitor points**
- **Programmable write precompensation**
- **Hard and soft sector operation**
- **Uses standard 5V ± 5% supply**
- **44-pin PLCC package**

## BLOCK DIAGRAM



## OPERATION

### DATA/CLOCK RECOVERY CIRCUIT

The circuit is designed to perform data recovery and data encoding in rotating memory systems which utilize a 1, 7 RLL encoding format. In the read mode the circuit performs data synchronization, sync field search and detect, address mark detect, and data decoding. In the write mode, the circuit converts NRZ data into the 1, 7 RLL format described in Table 1, performs write precompensation, generates the preamble field and inserts address marks as requested.

This data rate is established by a single 1% external resistor, RR, connected from the IREF pin to VPA. This resistor establishes a reference current which sets the VCO center frequency, the phase detector gain, and the 1/3 cell delay. The value of this resistor is given by:

$$RR = \frac{185}{DR} - 1.7k\Omega$$

Where: DR = data rate in Mbit/s

Alternately, the IREF pin can be driven from the SSI 32D4660 in a constant density recording application.

The circuit employs a dual mode phase detector; harmonic in the read mode and non-harmonic in the write and idle modes. In the read mode, the harmonic phase detector updates the PLL with each occurrence of a DLYD DATA pulse. In the write and idle modes, the non-harmonic phase detector is continuously enabled, thus maintaining both phase and frequency lock. By acquiring both phase and frequency lock to the input reference frequency and utilizing a zero phase restart technique, false lock to DLYD DATA is eliminated.

The phase detector incorporates a charge pump in order to drive the loop filter directly. The polarity and width of the output current pulses correspond to the direction and magnitude of the phase error.

The READ GATE ($\overline{RG}$) and WRITE GATE ($\overline{WG}$) inputs control the mode of the data/clock recovery section of the chip.

$\overline{RG}$ is an asynchronous input and may be initiated or terminated at any position on the disk. $\overline{WG}$ is also an asynchronous input, but should not be terminated prior to the last output write data pulse.

### READ OPERATION

The data synchronizer utilizes a fully integrated fast acquisition PLL to accurately develop the decode window. Read gate, $\overline{RG}$, initiates the PLL locking sequence and selects the PLL reference input; a low level (read mode) selects the $\overline{RD}$ input and a high level selects the external reference clock.

In the read mode the falling edge of $\overline{DRD}$ enables the phase detector while the rising edge is phase compared to the rising edge of VCO. As depicted in Figure 1, $\overline{DRD}$ is a 1/3 cell wide (TVCO/2) pulse whose leading edge is defined by the leading edge of $\overline{RD}$. A decode window is developed from the VCO clock.

Shifting the symmetry of the VCO clock effectively shifts the relative position of the DRD pulse within the decode window. Decode window control is provided via the WS controls.

In the non-read modes, the PLL is locked to the external reference clock. When the reference input to the PLL is switched, the VCO is stopped momentarily, then restarted in an accurate phase alignment with the next PLL reference input pulse, and the VCO clock divider is reset.

### ADDRESS MARK DETECT

In soft sector read operation the circuit must first detect an address mark to be able to initiate the rest of the read lock sequence. An address mark consists of two sets

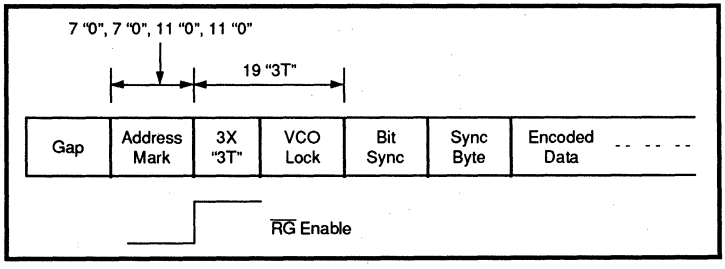



**FIGURE 1: Disk Operation Lock Sequence in Read Mode Soft Sector Operation**

of 7 "0" patterns followed by two sets of 11 "0" patterns. To begin the read lock sequence the Address Mark Enable ($\overline{AMEN}$) is asserted low by the controller. The address mark detect ($\overline{AMD}$) circuit then initiates a search of the read data ($\overline{RD}$) for an address mark. First the $\overline{AMD}$ looks for a set of 6 "0"s within the 7 "0" patterns. Having detected a 6 "0" the $\overline{AMD}$ then looks for a 9 "0" set within the 11 "0"s. If $\overline{AMD}$ does not detect 9 "0"s within 5 $\overline{RD}$ bits after detecting 6 "0"s it will restart the address mark detect sequence and look for 6 "0"s. When the $\overline{AMD}$ has acquired a 6 "0," 9 "0" sequence, the $\overline{AMD}$ transitions low.

### PREAMBLE SEARCH

After the Address Mark (AM) has been detected, a Read Gate ($\overline{RG}$) can be asserted low, initiating the remainder of the read lock sequence. When $\overline{RG}$ is asserted, an internal counter counts negative transitions of the incoming read data ($\overline{RD}$) looking for 3 consecutive 3T preambles. Once the counter reaches count 3 (finds 3 consecutive 3T preambles) the internal read gate enables, switching the phase detector from the external reference clock to the delayed read data input ($\overline{DRD}$); at the same time a zero phase (internal) restart signal restarts the VCO in phase with the read reference clock. This prepares the VCO to be synchronized to data when the bit sync circuitry is enabled after VCO lock is established.

### VCO LOCK AND BIT SYNC ENABLE

When the internal counter counts 16 more "3T" or a total of 19 negative transitions from RG enable, an internal VCO lock signal enables. The VCO lock signal activates the decoder bit synchronization circuitry to define the proper decode boundaries. Also, at count 19, the RRC source switches from the external reference clock to VCO clock signal which is phase locked to $\overline{DRD}$. The VCO is assumed locked at this point. A maximum of 2 RRC time periods may occur for the RRC transition, however, no short duration glitches will occur. After the bit sync circuitry sets the proper decode window (VCO in sync with RRC and RRC in sync with the data) NRZ is enabled and data is toggled in to be decoded for the duration of the read gate.

### BYTE SYNC AND NRZ OUT

As the data is decoded, it is compared to a Sync Byte that was loaded prior to the read operation. When a match is found, RCLK and NCLK are resynchronized to the correct byte boundary. NRZ data then appears at the byte output beginning with the sync byte. The $\overline{SBD}$ output is also set low at this time. It remains low until the end of the read operation. A parity bit (NRZP) is also generated for each output byte (even parity).

### HARD SECTOR OPERATION

In hard sector operation AMD remains inactive. A hard sector read operation does not require an address mark search but starts with a preamble search as with soft sector and sequences identically. In all respects, with exception to the address mark search sequence, hard sector read operation is the same as soft sector read.

### WRITE MODE

In the write mode the circuit converts NRZ data from the controller into 1, 7 RLL formatted data for storage on the disk. The circuit can operate with a soft or hard sector hard drive.

In soft sector operation the circuit generates a "7, 7, 11, 11" address mark and a preamble pattern. In hard sector operation the circuit generates a 19 x "3T" preamble pattern but no preceding address mark.

NRZ data is clocked into the circuit, serialized and latched on defined cell boundaries. The NRZ input data must be synchronous with the rising edges of the WCLK.

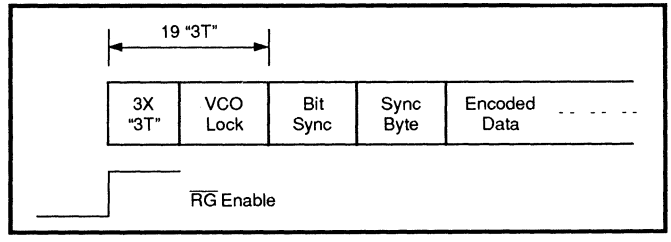



**FIGURE 2: Disk Operation Lock Sequence in Read Mode Hard Sector Operation**

**WRITE MODE** (Continued)

Write precompensation circuitry is provided to compensate for media bit shift caused by intersymbol interference. The circuit recognizes specific write data patterns and can add or subtract delays in the time position of write data bits to counteract the read back bit shift. The magnitude of the time shift, TPC, is determined by an external resistor on the WCS pin.

The circuit performs write precompensation according to the algorithm outlined in Table 3.

**SOFT SECTOR**

In soft sector operation, when read gate ($\overline{RG}$) transitions high, VCO source and RRC source switch from $\overline{RD}$ and 2VCO/3, respectively, to the external reference clock. At the same time the VCO (internal) lock goes inactive but the VCO is locked to the external reference clock. After delay of 1 NRZ time period (min) from $\overline{RG}$ high, the write gate ($\overline{WG}$) can be enabled low while NRZ is maintained (NRZ write data) low. The address mark enable ($\overline{AMEN}$) is made active (low) a minimum of 1 NRZ time period later. The address mark (consisting of 7 "0"s, 7 "0"s, 11 "0"s, 11 "0"s) and the 19 x "3T" preamble is then written by WD. While the preamble is being written, WCLK is clocking in an all "0" NRZ byte. The first non-zero NRZ byte input is assumed to be the sync byte. After a delay of 5 NRZ time periods, non-preamble data begins to toggle out WD. Finally, at the end of the write cycle, 2 bytes of blank NRZ time passes to insure the encoder is flushed of data; $\overline{WG}$ then goes high. WD stops toggling a maximum of 2 NRZ time periods after $\overline{WG}$ goes high.

As each NRZ byte is input for encoding, its parity is checked against the parity bit (NRZP). If a parity error is detected the PERR output flag is set high. It remains high until WG goes high.

**HARD SECTOR**

In hard sector operation, when read gate ($\overline{RG}$) transitions high, VCO source and RRC switch references and VCO lock (internal) goes inactive as with soft sector but the $\overline{AMEN}$ (address mark enable) is kept high.

The circuit then sequences from $\overline{RG}$ disable to $\overline{WG}$ enable and NRZ active as in soft sector operation.

## PIN DESCRIPTION

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| VPA1, VPA2 | I | 5 volt analog power supply pins |
| VPD | I | 5 volt digital power supply pin |
| AGND | O | Analog ground pin |
| DGND | O | Digital ground pin |
| $\overline{AMEN}$ | I | ADDRESS MARK ENABLE: Used to enable the address mark detection and address mark generation circuitry. Active low TTL input levels. |
| EPD | I | ENABLE PHASE DETECTOR: A low level (coast mode) disables the phase detector and enables the Test Mode. This opens the PLL and the VCO will run at the frequency commanded by the voltage on the VCO IN pin. (In the Test Mode, functions normally driven by the VCO are switched to XTAL.) Pin EPD has an internal pull-up resistor. TTL input levels. |
| RD, $\overline{RD}$ | I | READ DATA: Encoded Read Data from the disk drive read channel. Differential +5 volts offset ECL (PECL) input levels. |
| $\overline{RG}$ | I | READ GATE: Selects the PLL reference input and initiates the PLL synchronization sequence. A low level selects the RD input and enables the read mode/address detect sequences. A high level selects the XTAL input. See Table 2, TTL input levels. |
| $\overline{SBL}$ | I | SYNC BYTE LATCH CONTROL: Used to latch the Sync Byte reference value into the internal Sync Byte comparator. During idle mode, the Sync Byte latch is transparent while $\overline{SBL}$ is high. An active low level latches the input Sync Byte. The Sync Byte latch is kept in a hold state during non-idle modes, independent of the state of the $\overline{SBL}$ control. Pin $\overline{SBL}$ has an internal pull-up resistor. TTL input levels. |

**PIN DESCRIPTION** (Continued)

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| $\overline{W0}$, $\overline{W1}$, $\overline{W2}$ | I | WRITE/WINDOW CONTROL BITS: In Write Mode, pins $\overline{W0}$ and $\overline{W1}$ control the magnitude of the write precompensation (see Table 4). In Read Mode, pins $\overline{W0}$ and $\overline{W1}$, $\overline{W2}$ control the magnitude of the decode window shift. Each pin has an internal pull-up resistor. TTL input levels. |
| $\overline{WL}$ | I | WRITE PRECOMPENSATION LATCH CONTROL: Used to latch the write precompensation control bits $\overline{W0}$ and $\overline{W1}$ into the internal DAC. The latch is transparent while $\overline{WL}$ is high. An active low level latches the input control bits. Pin $\overline{WL}$ has an internal pull-up resistor. TTL input levels. |
| WCLK | I | WRITE CLOCK: Write mode byte clock. Must be synchronous with the Write Data NRZ input. For short cable delays, WCLK may be connected directly to pin RCLK. For long cable delays, WCLK should be connected to an RCLK return line matched to the NRZ data bus line delay. TTL input levels. |
| $\overline{WG}$ | I | WRITE GATE: Enables the write mode. See Table 2. Active low TTL input levels. |
| WSD | I | WINDOW SYMMETRY DIRECTION CONTROL: Controls the direction of the decode window shift. Each pin has an internal pull-up resistor. TTL input levels. |
| $\overline{WSL}$ | I | WINDOW SYMMETRY LATCH CONTROL: Used to latch the window symmetry control bits $\overline{W0}$, $\overline{W1}$, $\overline{W2}$ and WSD into the internal DAC. The latch is transparent while $\overline{WSL}$ is high. An active low level latches the input control bits. Pin $\overline{WSL}$ has an internal pull-up resistor. TTL input levels. |
| $\overline{AMD}$ | O | ADDRESS MARK DETECT: Tristate output pin that is in its high impedance state when WG is low or $\overline{AMEN}$ is high. When $\overline{AMEN}$ is low, this output indicates address mark search status. A latched low level output appears when an address mark has been detected. A high level on pin $\overline{AMEN}$ resets pin $\overline{AMD}$. TTL output levels. |
| $\overline{DRD}$ | O | DELAYED READ DATA: An open emitter ECL output test point. The positive edges of this signal indicate the data bit position. The positive edges of the $\overline{DRD}$ and VCO_REF outputs can be used to estimate window centering. The time jitter of $\overline{DRD}$'s positive edge is an indication of media bit jitter. Two external resistors are required to use this pin. They should be removed during normal operation to reduce power dissipation. |
| NCLK | O | NIBBLE CLOCK: A half-byte clock synchronized to RCLK. It runs at twice the RCLK frequency. TTL output levels. |
| PERR | O | PARITY ERROR FLAG: Active during write mode and during Sync Byte loading. When $\overline{WG}$ is low, the contents of the NRZ write data input register is examined and compared with the NRZP write data parity bit. Even parity is assumed. For example, PERR becomes active when NRZ7-0 and NRZP are all high. Parity checking is performed after each WCLK load operation. If the input data contains a parity error, or if the WCLK timing causes the input register to contain a parity error, an internal write parity error flag is set. If a parity error occurs during a write operation, the Write Data encoding will continue to function normally. This error flag is reset low when $\overline{WG}$ goes high.<br>Independent of $\overline{WG}$, a separate circuit monitors the Sync Byte. Each time $\overline{SBL}$ transitions from high to low, the contents of the Sync Byte latch is compared with the NRZP data parity bit. If a parity error exists, an internal Sync Byte parity error flag is set. This flag is reset low when $\overline{SBL}$ goes high. The PERR output displays the write parity flag condition when $\overline{WG}$ is low. When $\overline{WG}$ is high, PERR outputs the state of the Sync Byte parity error flag. TTL output levels. |

**PIN DESCRIPTION** (Continued)

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| RCLK | O | READ CLOCK: A multiplexed byte clock source used by the controller, see Table 2. During a mode change, no glitches are generated and no more than one lost clock pulse will occur. When $\overline{RG}$ goes low, RCLK initially remains synchronized to XTAL/12. When the Sync Byte is detected, RCLK is synchronized to the Read Data. When $\overline{RG}$ goes high, RCLK is synchronized back to the XTAL/12. TTL output levels. |
| $\overline{SBD}$ | O | SYNC BYTE DETECT: A TTL output that transitions low upon detecting a Sync Byte. This transition is synchronized to the first NRZ byte out following the sync byte. Once it transitions, $\overline{SBD}$ remains low until $\overline{RG}$ is raised, when it is returned to a high state. |
| VCO REF | O | VCO REFERENCE: An open emitter ECL output test point. This is the VCO reference input to the phase detector. The positive edges are phase locked to Delayed Read Data. The negative edges of this open emitter output signal indicate the edges of the decode window. Two external resistors are required to use this pin. They should be removed during normal operation to reduce power dissipation. |
| WD, $\overline{WD}$ | O | WRITE DATA: Encoded write data flip-flop output. The data is automatically resynchronized (independent of the delay between RCLK and WCLK) to the XTAL reference clock. Differential +5 volts offset ECL (PECL) output levels. |
| NRZ0-7 | I/O | NRZ DATA PORT: Read data output when $\overline{RG}$ is low, write data input when $\overline{WG}$ is low, and Sync Byte input when both $\overline{RG}$ and $\overline{WG}$ are high. TTL input and output levels. |
| NRZP | I/O | NRZ DATA PARITY BIT: Generated read data parity bit output when $\overline{RG}$ is low, write data parity bit input when $\overline{WG}$ is low, and Sync Byte parity bit input when both $\overline{RG}$ and $\overline{WG}$ are high. In read mode, even parity is generated. For example, when NRZ7-0 are all high, NRZP will be set low. TTL input and output levels. |

**ANALOG PINS**

| | | |
|---|---|---|
| IREF | I | CURRENT REFERENCE INPUT: The VCO center frequency, the 1/3 cell delay, and the phase detector gain are a function of the current sourced into this pin. |
| PD OUT | I/O | PHASE DETECTOR OUTPUT: Drives the loop filter input. |
| RS | I | WINDOW SYMMETRY ADJUST PIN: This pin allows analog adjustment of the decode window shift magnitude. Used in conjunction with the digital controls $\overline{W0}$ and $\overline{W1}$, $\overline{W2}$ this pin can be used to scale the magnitude of the preset window shift. Connect resistor to VPA. |
| VCO IN | I/O | VCO CONTROL INPUT: Driven by the loop filter output. |
| WCS | I | WRITE PRECOMPENSATION SET: Pin for the reference current to set the write precompensation magnitude value. |
| XTAL1, 2 | I | REFERENCE FREQUENCY INPUT: The pin frequency is at one and one-half times the data rate. If a crystal oscillator is used, an AC coupled parallel LC circuit must be connected from XTAL1 to ground. The crystal is connected between XTAL1 and XTAL2. If a crystal oscillator is not desired, XTAL1 may be driven either by a direct coupled TTL signal or by an AC coupled ECL signal, with XTAL2 open. |

## ELECTRICAL SPECIFICATIONS

Unless otherwise specified, 4.75V < VPA/VPD < 5.25V, 0 °C < T(ambient) < 70 °C, 25 °C < T(junction) < 135 °C. Currents flowing into the chip are positive. Current maximums are currents with the highest absolute value.

### ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may damage the device

| PARAMETER | RATING | UNIT |
|---|---|---|
| Supply Voltage, VPA1, VPA2, VPD | -0.3 to 6 | V |
| Storage Temperature | -65 to 150 | °C |
| Lead Temperature (Soldering 10 sec.) | 260 | °C |
| NRZ0 - NRZ7, RCLK, NCLK, WDT, $\overline{WDT}$, AMFND, SBFND, VCOREF, DRD Pins | -0.3 to (VPA/VPD+0.3), or +12 | V<br>mA |
| All other pins | -0.3 to (VPA/VPD+0.3) | V |

### POWER SUPPLY CURRENTS AND POWER

| PARAMETER | CONDITION | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| ICC (VPA, VPD)<br>Supply Current | Outputs and test point pins open,<br>Ta = 70 °C | | 200 | 230 | mA |
| PWR<br>Power Dissipation | Outputs and test point pins open,<br>Ta = 70 °C | | 1.0 | 1.2 | W |

### DIGITAL INPUTS AND OUTPUTS

**TTL Compatible Inputs:** $\overline{AMENB}$, EPD, NRZ0-NRZ7 (bid.), NRZP (bid.), $\overline{RG}$, $\overline{SBL}$, $\overline{W0}$, $\overline{W1}$, $\overline{W2}$, $\overline{WL}$, WCLK, $\overline{WG}$, WSD, $\overline{WSL}$ Pins

| PARAMETER | CONDITION | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| Input Low Voltage (VIL) | | -0.3 | | 0.8 | V |
| Input High Voltage (VIH) | | 2.0 | | VPD+0.3 | V |
| Input Low Current | VIL = 0.4 V | 0.0 | | -0.4 | mA |
| Input High Current | VIH = 2.4 V | | | 100 | µA |

Note: "bid." means bi-directional

**TTL Compatible Outputs** $\overline{AMD}$, NCLK, NRZ0-NRZ7 (bid.), NRZP (bid.), PERR, RCLK, $\overline{SBD}$ Pins

| PARAMETER | CONDITION | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| Output Low Voltage | Iol = 4.0 mA | | | 0.5 | V |
| Output High Voltage | Ioh = -400 µA | 2.4 | | | V |

**Digital Differential Inputs:** RD, $\overline{RD}$ Pins

| | | | | | |
|---|---|---|---|---|---|
| Input Low Voltage (VIL) | | VPA-2.2 | | VIH-0.5 | V |
| Input High Voltage (VIH) | | VIL+0.5 | | VPA-0.5 | V |
| Differential Voltage | $\lvert V_{RD} - V_{\overline{RD}} \rvert$ | 0.5 | | | V |
| Input Low Current | VIL = Min | -100 | | | µA |
| Input High Current | VIH = Max | | | +100 | µA |

**Digital Differential Outputs:** WD, $\overline{WD}$ Pins

| | | | | | |
|---|---|---|---|---|---|
| Output Low Voltage | Iol = TBD | VPD-2.1 | | | V |
| Output High Voltage | Ioh = TBD | | | VPD-0.7 | V |
| Differential Voltage | $\lvert V_{WD} - V_{\overline{WD}} \rvert$ | 0.5 | | | V |

**Test Point Output Levels**

| | | | | | |
|---|---|---|---|---|---|
| Test Point Output<br>High Level<br>$\overline{DRD}$, VCO REF | 262Ω to VPA,<br>402Ω to GND<br>VPA = 5V | | VPA<br>-0.85 | | V |
| Test Point Output<br>Low Level<br>$\overline{DRD}$, VCO REF | 262Ω to VPA,<br>402Ω to GND<br>VPA = 5V | | VPA<br>-1.75 | | V |

**DYNAMIC CHARACTERISTICS AND TIMING**

**READ MODE**

| PARAMETER | CONDITION | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| Read Data Pulse Width (TPRD) | | 10 | | (2)TVCO -10 | ns |
| Read Data Rise Time (TRRD) | 20% to 80%, CL ≤ 10 pF | | | 5 | ns |
| Read Data Fall Time (TFRD) | 80% to 20%, CL ≤ 10 pF | | | 5 | ns |
| Read Clock Rise Time (TRRC) | 0.8V to 2.0V, CL ≤ 15 pF | | | 10 | ns |
| Read Clock Fall Time (TFRC) | 2.0V to 0.8V, CL ≤ 15 pF | | | 8 | ns |
| NCLK Rise Time (TRNC) | 0.8V to 2.0V, CL ≤ 15 pF | | | 10 | ns |
| NCLK Fall Time (TFNC) | 2.0V to 0.8V, CL ≤ 15 pF | | | 8 | ns |
| NRZ (out) Set Up &<br>Hold Time (TDS, TDH) | | 30 | | | ns |
| $\overline{SBD}$ Set up & Hold Time<br>(TSBS, TSBH) | | 30 | | | ns |

**READ MODE** (Continued)

| PARAMETER | CONDITION | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| RCLK Pulse Width (TRD) | VCO re-sync | 0.4 TORC | | 1.25 TORC | ns |
| | BYTE re-sync | 0.4 TORC | | 1.6 TORC | ns |
| RCLK Duty Cycle | | 40 | | 60** | % |
| NCLK Pulse Width (TQD) | Except during re-sync | (TORC/4)-5 | | (TORC/4)+5 | ns |
| NCLK Pulse Width (TQD) | During re-sync | TORC/4-5 | | 3TORC/4+5 | ns |
| NCLK Skew (TQS) | | -20 | | 20 | ns |
| RCLK Resync Period (Tdc2) | | TORC | | (2)TORC | ns |
| NCLK Resync Period (Tdc1) | | TORC/2 | | TORC | ns |
| Decode Window Centering Accuracy | | | | ±0.75 | ns |
| Decode Window | | TVCO -0.75 | | | ns |

** Except during re-sync

**WRITE MODE**

| | | | | | |
|---|---|---|---|---|---|
| Write Data Rise Time (TRWD) | 20% to 80% Points<br>110Ωto VPD, 160Ωto DGND | | | 5 | ns |
| Write Data Fall Time (TFWD) | 80% to 20% Points<br>110Ωto VPD, 160Ωto DGND | | | 5 | ns |
| Write Data Clock Rise Time (TRWC) | 0.8V to 2.0V,<br>CL ≤ 15 pF | | | 10 | ns |
| Write Data Clock Fall Time (TFWC) | 2.0V to 0.8V,<br>CL ≤ 15 pF | | | 8 | ns |
| NRZ Set Up Time (TSNRZ) | | 20 | | | ns |
| NRZ Hold Time (THNRZ) | | 20 | | | ns |
| Precompensation Time Shift Magnitude Accuracy (TPC) | TPCO = 0.22 (Rc + 0.53)<br>Rc min=1 KΩ, Rc max=0.3TXTAL | | | | |
| | $\overline{W0}$=1 $\overline{W1}$=1 | -0.5 | | 0.5 | ns |
| | $\overline{W0}$=0 $\overline{W1}$=1 | 0.8 TPCO | | 1.2 TPCO | ns |
| | $\overline{W0}$=1 $\overline{W1}$=0 | 2 (0.8 TPCO) | | 2 (1.2 TPCO) | ns |
| | $\overline{W0}$=0 $\overline{W1}$=0 | 3 (0.8 TPCO) | | 3 (1.2 TPCO) | ns |

**DATA SYNCHRONIZATION**

| | | | | | |
|---|---|---|---|---|---|
| VCO Center Frequency Period (TVCO) | VCO IN=2.7V, VPA=VPD=5V<br>TO=3.6 (RR+1.7),<br>RR=(185/DR)-1.7K | 0.8TO | | 1.2TO | ns |
| VCO Frequency Dynamic Range | 1.0 V ≤ VCO IN<br>≤ VPA - 0.6V<br>VPA=VPD = 5 V | ± 25 | | ± 45 | % |
| VCO Control Gain (KVCO) | ωo = 2π/TVCO<br>1.0 V ≤ VCO IN<br>≤ VPA - 0.6V | 0.14 ωo | | 0.26 ωo | rad/s V |

**DATA SYNCHRONIZATION** (Continued)

| PARAMETER | CONDITION | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| Phase Detector Gain (KD) | VPA=VPD=5V<br>Read: KD=750/(RR + 0.53)<br>Non-Read: KD=375/(RR + 0.53) | 0.83KD | | 1.17KD | µA/rad |
| KVCO x KD Product Accuracy | | -28 | | +28 | % |
| VCO Phase Restart Error | Referred to RRC | -1 | | +1 | rad |
| 1/3 Cell Delay | VCC = 5.0V<br>TD=1.8 (RR + 1.7); RR = kΩ | 0.8TD | | 1.2TD | ns |

**CONTROL TIMING**

| | | | | | |
|---|---|---|---|---|---|
| $\overline{W0}$, $\overline{W1}$, WSD Set Up and Hold Time (TSWC, THWC) | | 20 | | | ns |
| $\overline{WL}$, $\overline{WSL}$ Pulse Width (TWL) | | 50 | | | ns |
| Sync Byte NRZ Set Up and Hold Time (TSSB, THSB) | | 20 | | | ns |
| $\overline{SBL}$ Pulse Width (TSB) | | 50 | | | ns |
| Sync Byte Parity Error Output Delay (TDSE) | | 0 | | 50 | ns |
| Sync Byte Parity Error Reset Delay (TSER) | | 0 | | 50 | ns |

**MODE CONTROL**

| $\overline{WG}$ | $\overline{RG}$ | $\overline{AMENB}$ | $\overline{SBL}$ | Modes | |
|---|---|---|---|---|---|
| 1 | 1 | 1 | 1 | Idle (SB Enable) | Idle mode. VCO locked to external XTAL reference. Byte clock and 4-bit clock synchronized to XTAL. NRZ0-NRZ7 tri-stated. $\overline{AMD}$ high. SB latch transparent. |
| 1 | 1 | 1 | 0 | SB Load | SB latch in a hold state. Other conditions same as idle mode. |
| 1 | 1 | 0 | X | AM Search | Read mode Address Mark search. VCO locked to external XTAL reference. Byte clock and 4-bit clock synchronized to XTAL. NRZ0-NRZ7 tri-stated. $\overline{AMD}$ active. |
| 1 | 0 | 1 | X | Read Data | Read mode preamble search and data acquisition. VCO switched from XTAL to RD after preamble lock. Byte clock and 4-bit clock synchronized to RD after Sync Byte found. NRZ0-NRZ7 active. $\overline{SBD}$ active. |
| 1 | 0 | 0 | X | Undefined | Illegal state. |
| 0 | 1 | 0 | X | Write AM | Write mode Address Mark insertion. VCO locked to external XTAL reference. Byte clock and 4-bit clock synchronized to XTAL. WD, $\overline{WD}$ active. NRZ0-NRZ7 tri-stated. $\overline{AMD}$ high. |
| 0 | 1 | 1 | X | Write Data | Write mode preamble insertion and data write. VCO locked to external XTAL reference. Byte clock and 4-bit clock synchronized to XTAL. WD, $\overline{WD}$ active. NRZ0-NRZ7 tri-stated. $\overline{AMD}$ high. |
| 0 | 0 | 1 | X | Undefined | Illegal state. |
| 0 | 0 | 0 | X | Undefined | Illegal state. |

### WRITE PRECOMP CONTROL

| $\overline{WL}$ - Write precomp latch control | $\overline{W1}$, $\overline{W0}$ - Write precomp magnitude control bits |
|---|---|
| 0 → Write precomp control latches in hold state<br>1 → Write precomp control latches in transparent state | 00 → 3x (maximum) shift<br>01 → 2x shift<br>10 → 1x shift<br>11 → No shift |

### WINDOW SHIFT CONTROL

$\overline{WSL}$ - Window shift latch control

0 → Window shift control latches in hold state

1 → Window shift control latches in transparent state

WSD - Window shift direction control

0 → Early window (+TS)

1 → Late window (-TS)

### WINDOW SHIFT MAGNITUDE CONTROL BITS

| $\overline{W2}$ | $\overline{W1}$ | $\overline{W0}$ | TS0 (decode window %) |
|---|---|---|---|
| 1 | 1 | 1 | No shift |
| 1 | 1 | 0 | 4% Minimum shift |
| 1 | 0 | 1 | 8% |
| 1 | 0 | 0 | 12% |
| 0 | 1 | 1 | 15% |
| 0 | 1 | 0 | 18% |
| 0 | 0 | 1 | 20% |
| 0 | 0 | 0 | 22% Maximum shift |

| Window shift with RRS used: | ($2K\Omega \leq RRS \leq 16\ K\Omega$) |
|---|---|
| $TS = TSO\left(\frac{RRS}{RRS+0.8}\right)$ | TSO = Window shift set by $\overline{W0}$ - $\overline{W1}$ with no RRS |

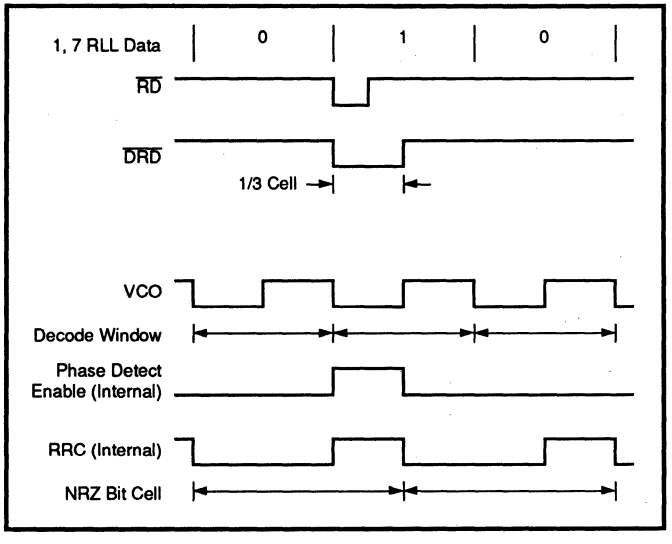



**FIGURE 3: Data Synchronization Waveforms**

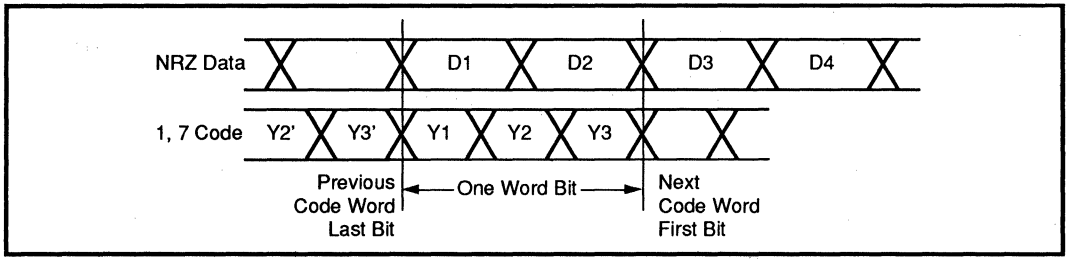



**FIGURE 4: NRZ Data Word Comparison to 1, 7 Code Word Bit**
(See Table 1 for Decode Scheme)

**TABLE 1: 1, 7 RLL Code Set**

| Previous Code Word Last Bits | | Data Bits Present | | Data Bits Next | | Code Bits | | |
|---|---|---|---|---|---|---|---|---|
| X | 0 | 1 | 0 | 0 | X | 1 | 0 | 1 |
| X | 0 | 1 | 0 | 1 | X | 0 | 1 | 0 |
| X | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 0 |
| X | 0 | 1 | 1 | ✶ | ✶ | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | X | 0 | 0 | 1 |
| 1 | 0 | 0 | 0 | 1 | X | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | X | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 1 | X | 0 | 0 | 0 |
| X | 1 | 0 | 0 | 0 | X | 0 | 0 | 1 |
| X | 1 | 0 | 0 | 1 | X | 0 | 1 | 0 |
| X | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| X | 1 | 0 | 1 | ✶ | ✶ | 0 | 0 | 0 |
| Y2' | Y3 | D1 | D2 | D3 | D4 | Y1 | Y2 | Y3 |

X = Don't Care;
✶ = Not All Zeros

**TABLE 2: Clock Frequency**

| $\overline{WG}$ | $\overline{RG}$ | VCO REF | RCLK | DECCLK | ENCCLK | MODE |
|---|---|---|---|---|---|---|
| 1 | 1 | XTAL | XTAL/12 | XTAL | XTAL | IDLE |
| 1 | 0 | RD | VCO/12 | VCO | XTAL | READ |
| 0 | 1 | XTAL | XTAL/12 | XTAL | XTAL | WRITE |

Notes 1: Until the VCO locks to the new source, the VCO entries will be XTAL.
2: Until the VCO locks to the new source, the VCO/12 entries will be XTAL/12.
3: $\overline{WG}$ = $\overline{RG}$ = 0 is undefined.

**TABLE 3: Write Precompensation Algorithm**

| Bit n-2 | Bit n-1 | Bit n | Bit n+1 | Bit n+2 | Compensation |
|---|---|---|---|---|---|
| 1 | 0 | 1 | 0 | 1 | None |
| 0 | 0 | 1 | 0 | 0 | None |
| 1 | 0 | 1 | 0 | 0 | Early |
| 0 | 0 | 1 | 0 | 1 | Late |

Notes Late: Bit n is time shifted (delayed) from its normal time position towards the Bit n+1 time position.
Early: Bit n is time shifted (advanced) from its normal time position towards the Bit n-1 time position.

**TABLE 4: Write Precompensation Magnitude**

| $\overline{WC1}$ | $\overline{WC0}$ | Magnitude, TPC |
|---|---|---|
| 0 | 0 | 3 (TPC0) |
| 0 | 1 | 2 (TPC0) |
| 1 | 0 | TPC0 |
| 1 | 1 | 0 |

The normal magnitude TPC0 is externally set with a resistor on pin WCS.

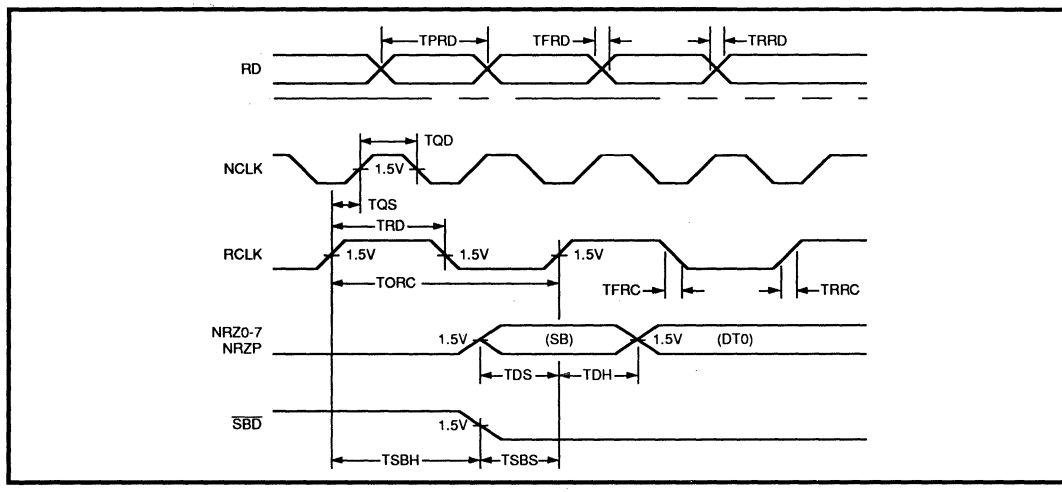



**FIGURE 5: Read Timing**

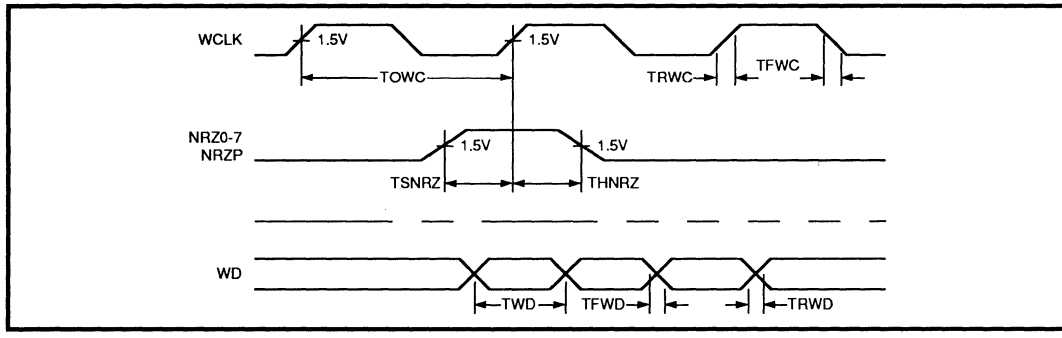



**FIGURE 6: Write Timing**

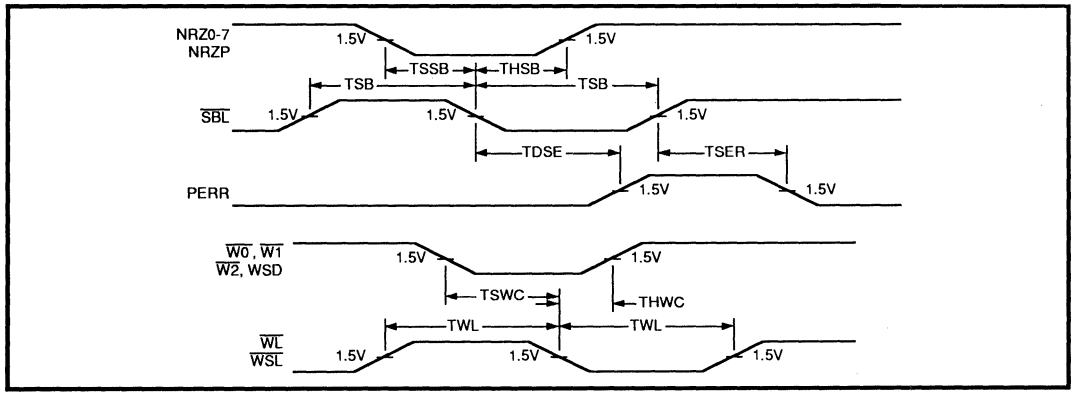



**FIGURE 7: Control Timing**

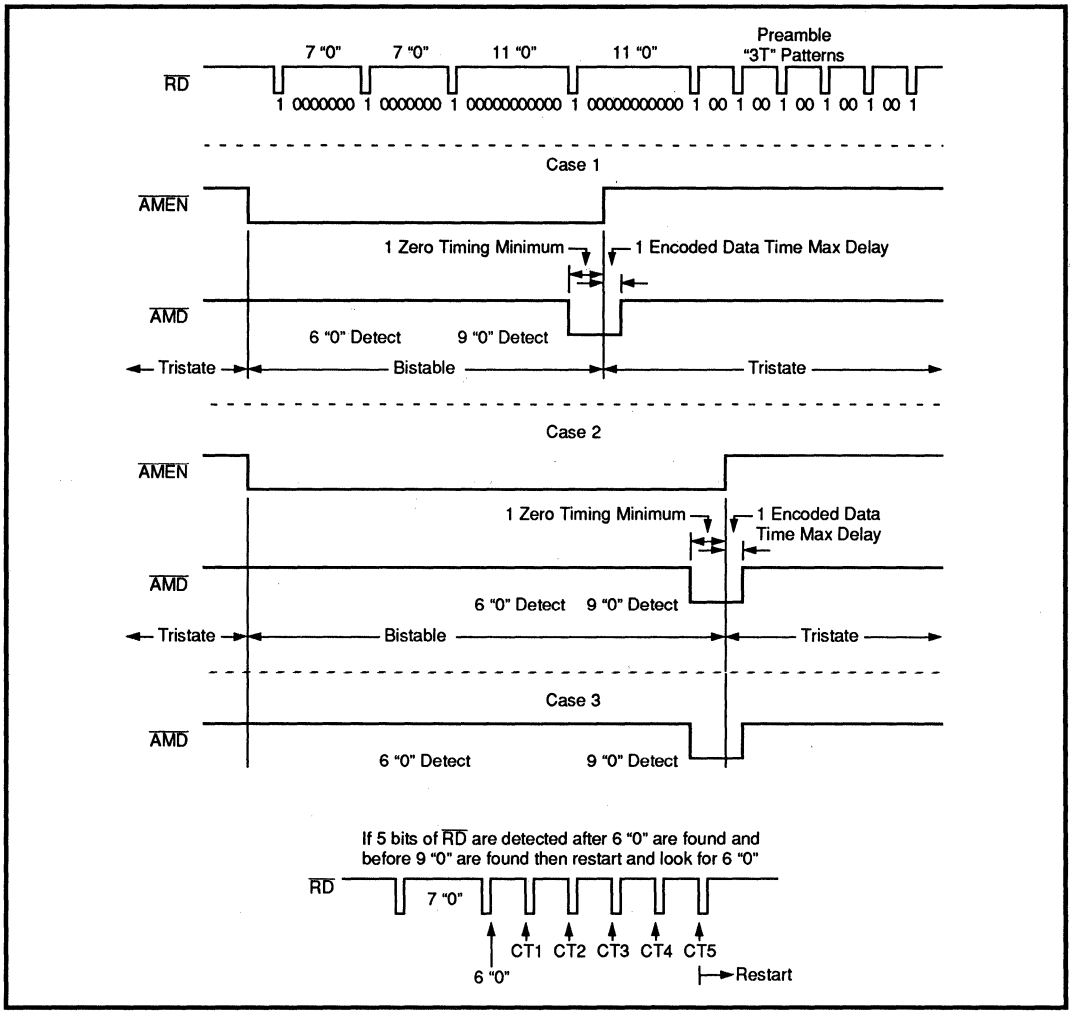



**FIGURE 8: Address Mark Search**

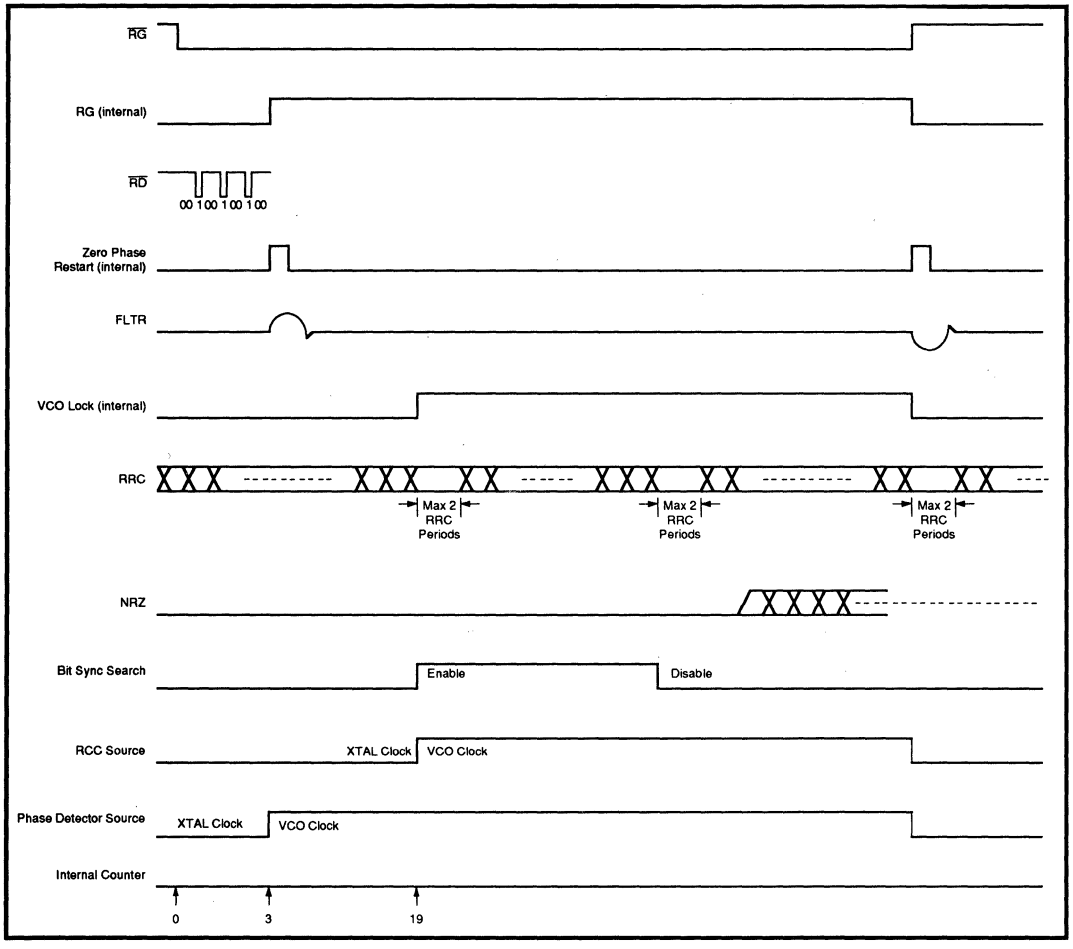



**FIGURE 9: Read Mode Locking Sequence (Soft and Hard Sector)**

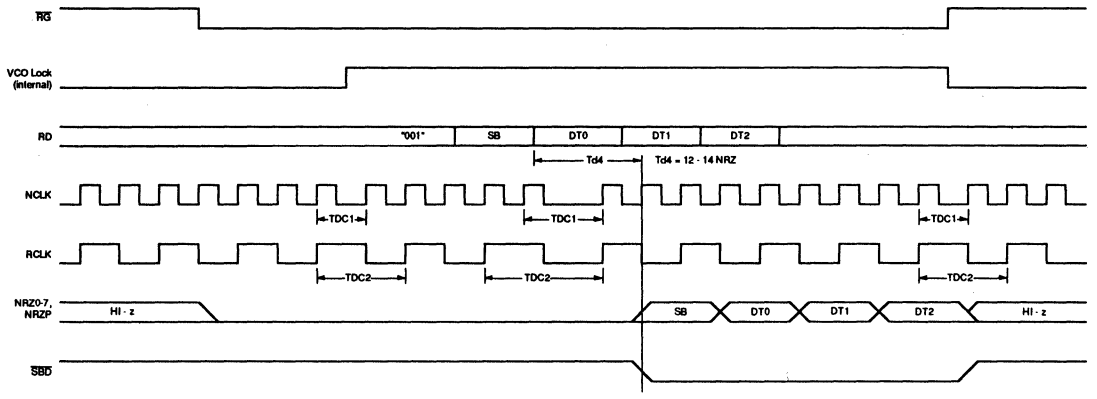



**FIGURE 10: Read Mode NRZ Data Timing**

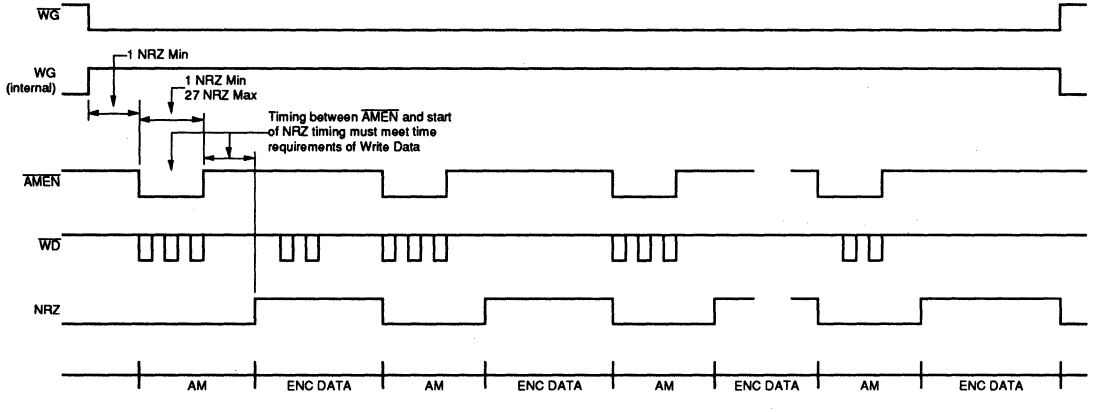



**FIGURE 11: Multiple Address Mark Write**

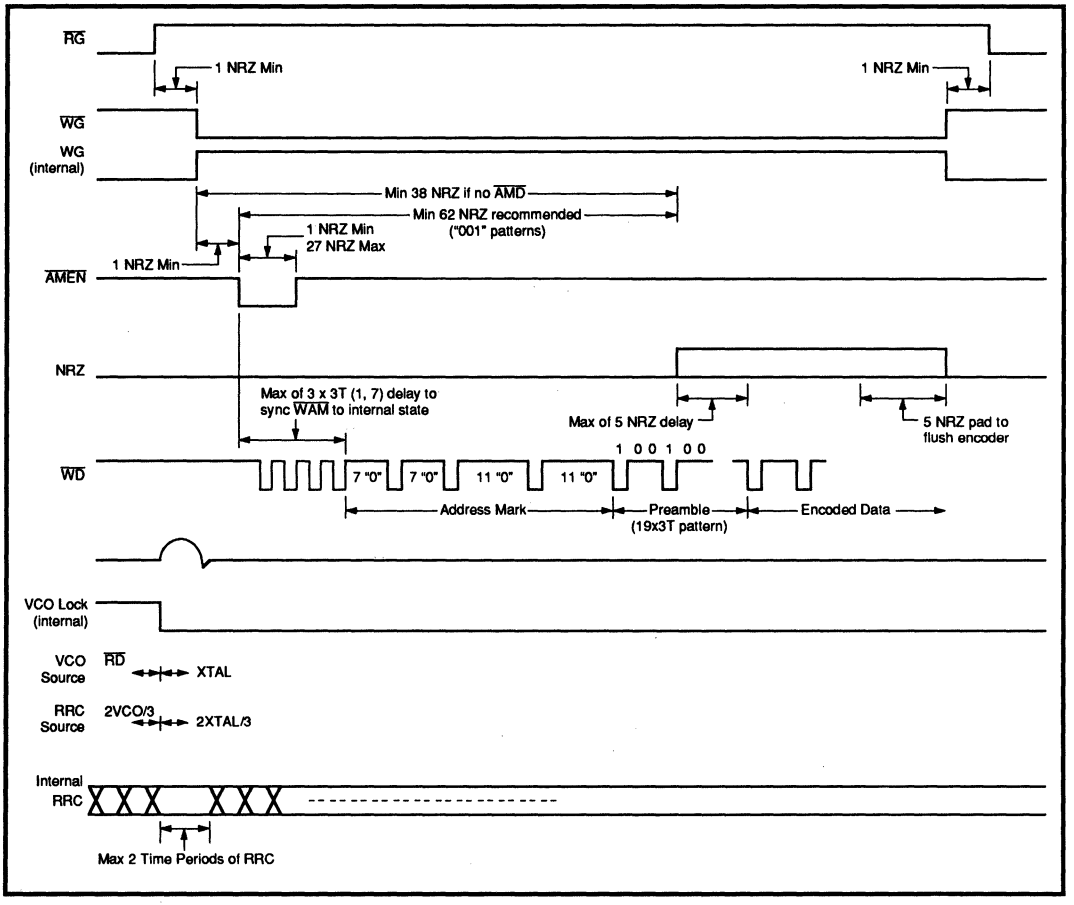



**FIGURE 12: Write Data**

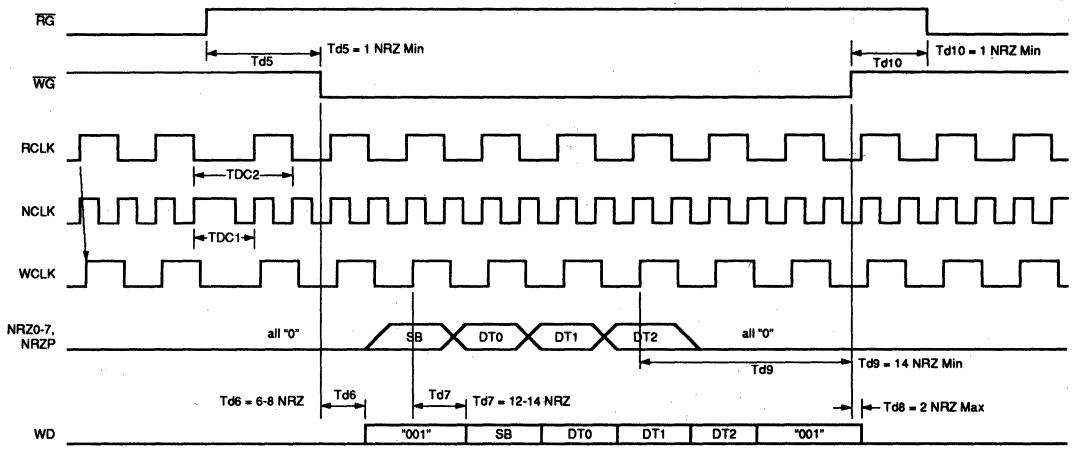



**FIGURE 13: Write Mode NRZ Timing**

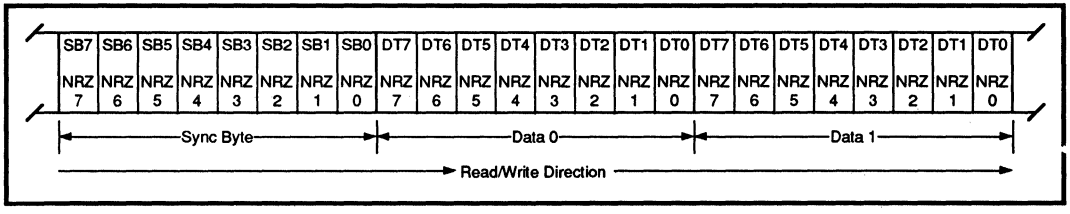
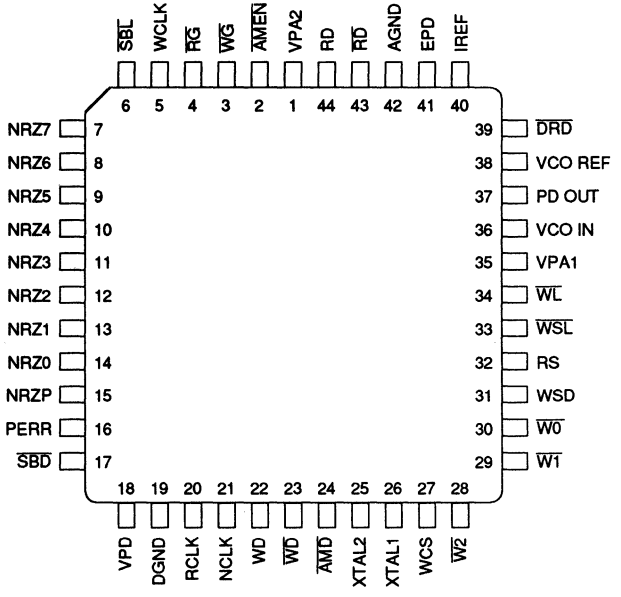



**FIGURE 14: Parallel/Serial Conversion Format**

## PACKAGE PIN DESIGNATIONS

(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.




4

## ORDERING INFORMATION

| PART DESCRIPTION | ORDER NO. | PKG. MARK |
|---|---|---|
| SSI 32D539 | | |
| 44-Pin PLCC | 32D539-CH | 32D539-CH |

**Preliminary Data:** Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.



Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680, (714) 573-6000, FAX: (714) 573-6914

**Notes:**

silicon systems®
A TDK Group Company

# SSI 32D5391
## Data Synchronizer & 1, 7 RLL ENDEC
## Advance Information

December 1992

4

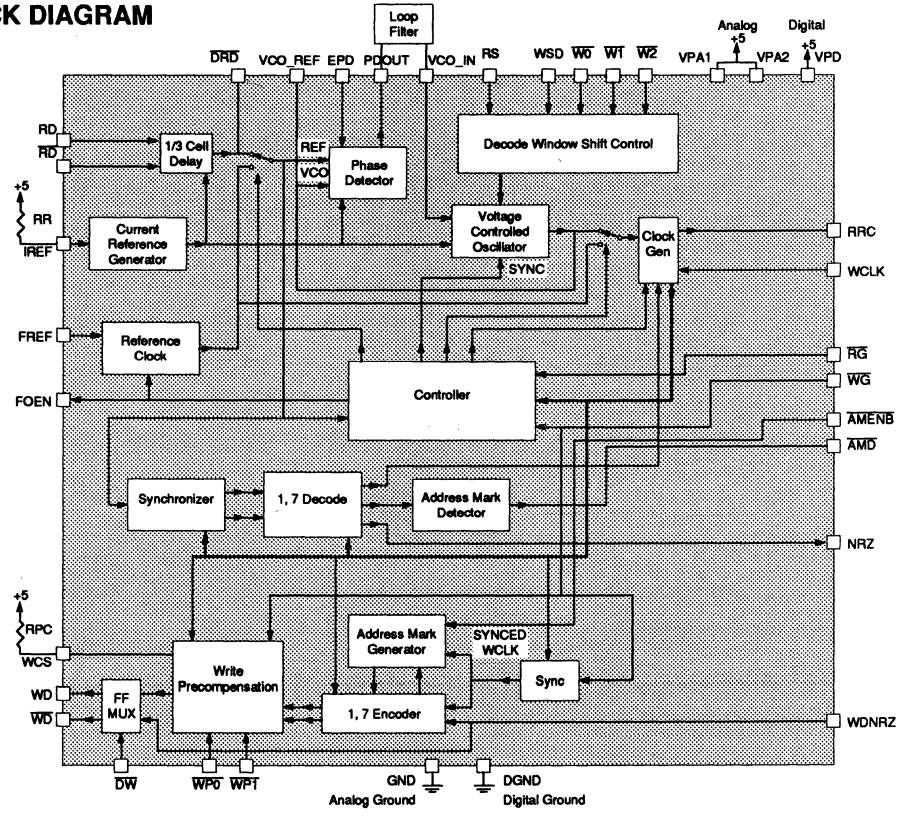
## DESCRIPTION

The SSI 32D5391 is intended to be used as a data/clock recovery circuit for 1, 7 RLL code in high performance hard disk drive systems with a +5V supply.

## FEATURES

- **Data synchronizer and 1, 7 RLL ENDEC**
- **Up to 40 Mbit/s operation**
  - **Data rate programmed with a single external resistor or current source**
- **Direct write capability**
- **Fast acquisition phase locked loop with zero phase restart technique**
- **Fully integrated data separator**
  - **No external delay lines or active devices required**
- **Programmable decode window symmetry control**
  - **Includes delayed read data and VCO clock monitor points**
- **Programmable write precompensation**
- **Hard and soft sector operation**
- **Uses standard 5V ± 5% supply**
- **44-pin PLCC package**

## BLOCK DIAGRAM



## PIN DEFINITION

### INPUT PINS

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| VPA1, VPA2 | I | 5 volt analog power supply pins. |
| VPD | I | 5 volt digital power supply pin. |
| $\overline{AMEN}$ | I | ADDRESS MARK ENABLE: Used to enable the address mark detection and address mark generation circuitry. Active low TTL input levels. |
| $\overline{DW}$ | I | DIRECT WRITE ENABLE: Use to enable the direct write mode. A high level allows normal write operation. A low level enables the encoder bypass mode. In this bypass mode, each falling edge of WDNRZ will directly clock the WD flip-flop when $\overline{WG}$ is low. Pin $\overline{DW}$ has an internal pull up resistor. TTL input levels. |
| EPD | I | ENABLE PHASE DETECTOR: A low level (coast mode) disables the phase detector and enables the Test Mode. This opens the PLL and the VCO will run at the frequency commanded by the voltage on the VCO_IN pin. (In the Test Mode, functions normally driven by the VCO are switched to XTAL.) Pin EPD has an internal pull-up resistor. TTL input levels. |
| FREF | I | REFERENCE FREQUENCY INPUT: The pin frequency is at one and one-half times the data rate. FREF may be driven either by an AC coupled suitably attenuated TTL signal or by an AC coupled ECL signal. |
| RD, $\overline{RD}$ | I | READ DATA: Encoded Read Data from the disk drive read channel. Differential pseudo ECL (PECL) input levels. |
| $\overline{RG}$ | I | READ GATE: Selects the PLL reference input and initiates the PLL synchronization sequence. A low level selects the RD input and enables the read mode/address detect sequences. A high level selects the XTAL input. See Table 2, TTL input levels. |
| $\overline{W0}$, $\overline{W1}$, $\overline{W2}$ | I | WINDOW SHIFT CONTROL BITS: In Read Mode, pins $\overline{W}$, $\overline{W1}$ and $\overline{W2}$ control the magnitude of the decode window shift. Each pin has an internal pull-up resistor. TTL input levels. |
| WSD | I | WINDOW SYMMETRY DIRECTION CONTROL: Controls the direction of the decode window shift. The pin has an internal pull-up resistor. TTL input levels. |
| WCLK | I | WRITE CLOCK: Write mode clock. Must be synchronous with the WDNRZ input. For short cable delays, WCLK may be connected directly to pin RRC. For long cable delays, WCLK should be connected to an RRC return line matched to the WDNRZ data line delay. TTL input levels. |
| WDNRZ | I | NRZ WRITE DATA INPUT PIN: This pin can be connected to the NRZ pin to form a bidirectional data port. Pin WDNRZ has an internal pull up resistor. TTL input levels. |
| $\overline{WP0}$, $\overline{WP1}$ | I | WRITE PRECOMPENSATION CONTROL BITS: In Write Mode, pins $\overline{WP0}$ and $\overline{WP1}$ control the magnitude of the write precompensation. Each pin has an internal pull up resistor. TTL input levels. |
| $\overline{WG}$ | I | WRITE GATE: Enables the write mode. Active low TTL input levels. |

## PIN DEFINITION (continued)

### OUTPUT PINS

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| AGND | O | Analog ground pin |
| DGND | O | Digital ground pin |
| $\overline{AMD}$ | O | ADDRESS MARK DETECT: Tristate output pin that is in its high impedance state when $\overline{WG}$ is low or $\overline{AMENB}$ is high. When $\overline{AMENB}$ is low, this output indicates address mark search status. A latched low level output appears when an address mark has been detected. A high level on pin $\overline{AMENB}$ resets pin $\overline{AMD}$. TTL output levels. |
| $\overline{DRD}$ | O | DELAYED READ DATA: An open emitter ECL output test point. The positive edges of this signal indicate the data bit position. The positive edges of the $\overline{DRD}$ and VCO_REF outputs can be used to estimate window centering. The time jitter of DRD's positive edge is an indication of media bit jitter. Two external resistors are required to use this pin. They should be removed during normal operation to reduce power dissipation. |
| FOEN | O | REFERENCE CLOCK ENABLE: When this output is high, the FREF clock is controlling the internal timing. When this output is low, the FREF clock is internally disabled. The output from pin FOEN can be used to disable the clock applied to the FREF pin to reduce VCO jitter during read modes. TTL output levels. |
| NRZ | O | NRZ READ DATA OUTPUT: Tristate output pin that is enabled when read gate is active. This pin can be connected to the WDNRZ pin to form a bidirectional data port. TTL output levels. |
| RRC | O | READ CLOCK: A multiplexed bit clock source used by the controller, see Table 2. During a mode change, no glitches are generated and no more than one lost clock pulse will occur. When $\overline{RG}$ goes low, RRC initially remains synchronized to 2FREF/3. After 19 read data pulses, RRC is synchronized to the Read Data. When $\overline{RG}$ goes high, RRC is synchronized back to 2FREF/3. TTL output levels. |
| VCO REF | O | VCO REFERENCE: An open emitter ECL output test point. This is the VCO reference input to the phase detector. The positive edges are phase locked to Delayed Read Data. The negative edges of this open emitter output signal indicate the edges of the decode window. Two external resistors are required to use this pin. They should be removed during normal operation to reduce power dissipation. |
| WD, $\overline{WD}$ | O | WRITE DATA: Encoded write data flip-flop output. The data is automatically resynchronized (independent of the delay between RRC and WCLK) to the FREF reference clock. Differential ECL output levels. |

## PIN DEFINITION (Continued)

### ANALOG PINS

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| IREF | I | CURRENT REFERENCE INPUT: The VCO center frequency, the 1/3 cell delay, and the phase detector gain are a function of the current sourced into this pin. |
| PD OUT | I/O | PHASE DETECTOR OUTPUT: Drives the loop filter input. |
| RS | I | WINDOW SYMMETRY ADJUST PIN: A resistor connected between this pin and VPA allows analog adjustment of the decode window shift magnitude. Used in conjunction with the digital controls $\overline{W0}$, $\overline{W1}$ and $\overline{W2}$, this pin can be used to scale the magnitude of the preset window shift. Connect resistor to VPA. |
| VCO IN | I/O | VCO CONTROL INPUT: Driven by the loop filter output. |
| WCS | I | WRITE PRECOMPENSATION SET: Pin for the reference current to set the write precompensation magnitude value. |

## ELECTRICAL SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS

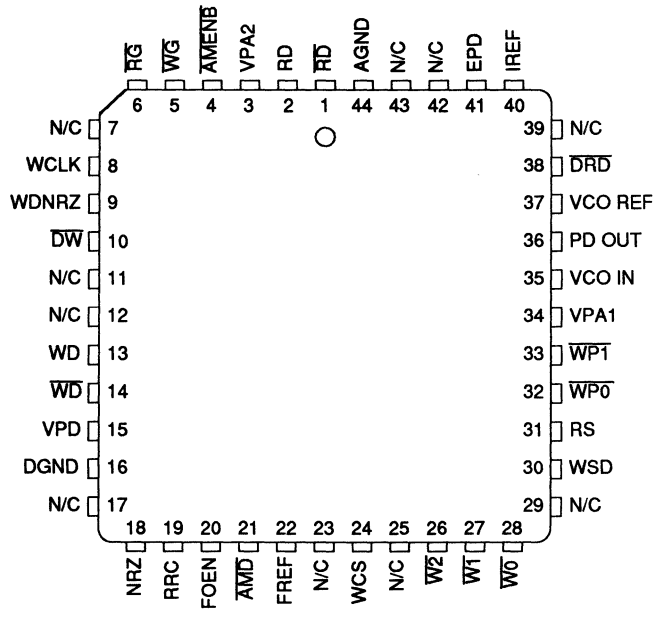
Operation above maximum ratings may damage the device

| PARAMETER | RATING |
|---|---|
| Positive 5.0V Supply Voltage, VPA1, VPA2, VPD | 6V |
| Storage Temperature | -65 to 150°C |
| Lead Temperature (Soldering 10 sec.) | 260°C |
| FOEN, NRZ, RRC, WD, $\overline{WD}$, $\overline{AMD}$, VCOREF, $\overline{DRD}$ Pins | 0.3V to VPA/VPD+0.3 or +12 mA |
| All other pins | -0.3V to VPA/VPD+0.3 |

## PACKAGE PIN DESIGNATIONS

(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.




**44-Pin PLCC**

**Advance Information:** Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.



Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680, (714) 573-6000, FAX: (714) 573-6914

**Notes:**

silicon systems®
A TDK Group Company

# SSI 32D5392

## Data Sync/1, 7 RLL ENDEC with Write Precomp. and Window Shift

**Advance Information**

February 1992

4

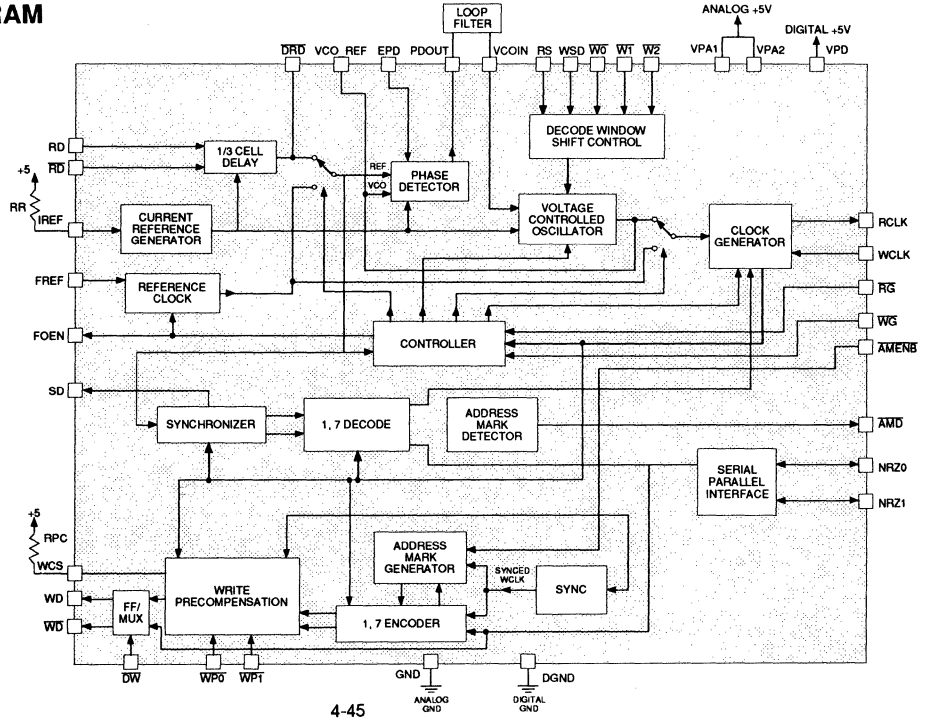
## DESCRIPTION

The SSI 32D5392 Data Synchronizer/1, 7 RLL ENDEC provides data recovery and data encoding for storage systems which employ a 1, 7 RLL encoding format. Data synchronization is performed with a fully integrated high performance PLL. A zero phase restart technique is used to minimize PLL acquisition time. The VCO frequency setting elements are incorporated within the SSI 32D5392 for enhanced performance and reduced board space. Data rate is established with a single external programming resistor. The SSI 32D5392 utilizes an advanced bipolar process technology which affords precise decode window control without the requirement of external devices. The SSI 32D5392 requires a single +5V supply.

## FEATURES

- **Data synchronizer and 1, 7 RLL ENDEC**
- **Dual bit NRZ bus**
- **24 to 48 Mbit/s operation**
  - **Data rate programmed with a single external resistor or current source**
- **Fast acquisition phase locked loop with improved zero phase restart technique**
- **Fully integrated data separator**
  - **No external delay lines or active devices required**
- **Programmable decode window symmetry control**
  - **Includes delayed read data and VCO clock monitor points**
- **Programmable write precompensation**
- **Hard and soft sector operation**
- **Uses standard 5V ± 5% supply**

## BLOCK DIAGRAM



## OPERATION

### DATA/CLOCK RECOVERY CIRCUIT

The circuit is designed to perform data recovery and data encoding in rotating memory systems which utilize a 1, 7 RLL encoding format. In the read mode the circuit performs data synchronization, sync field search and detect, address mark detect, and data decoding. In the write mode, the circuit converts NRZ data into the 1, 7 RLL format described in Table 1, performs write precompensation, generates the preamble field and inserts address marks as requested.

This data rate is established by a single 1% external resistor, RR, connected from the IREF pin to VPA. This resistor establishes a reference current which sets the VCO center frequency, the phase detector gain, and the 1/3 cell delay. The value of this resistor is given by:

$$RR = (185/DR) - 1.7\ k\Omega$$

Where: DR = data rate in Mbit/s

Alternately, the IREF pin can be driven from the SSI 32D4661 in a constant density recording application.

The circuit employs a dual mode phase detector; harmonic in the read mode and non-harmonic in the write and idle modes. In the read mode, the harmonic phase detector updates the PLL with each occurrence of a DLYD DATA pulse. In the write and idle modes, the non-harmonic phase detector is continuously enabled, thus maintaining both phase and frequency lock. By acquiring both phase and frequency lock to the input reference frequency and utilizing a zero phase restart technique, false lock to DLYD DATA is eliminated.

The phase detector incorporates a charge pump in order to drive the loop filter directly. The polarity and width of the output current pulses correspond to the direction and magnitude of the phase error.

The READ GATE ($\overline{RG}$) and WRITE GATE ($\overline{WG}$) inputs control the mode of the data/clock recovery section of the chip.

$\overline{RG}$ is an asynchronous input and may be initiated or terminated at any position on the disk. $\overline{WG}$ is also an asynchronous input, but should not be terminated prior to the last output write data pulse.

### READ OPERATION

The data synchronizer utilizes a fully integrated fast acquisition PLL to accurately develop the decode window. Read Gate, $\overline{RG}$, initiates the PLL locking sequence and selects the PLL reference input; a low level (Read Mode) selects the RD input and a high level selects the external reference clock.

In the read mode the falling edge of $\overline{DRD}$ enables the phase detector while the rising edge is phase compared to the rising edge of VCO. As depicted in Figure 1, $\overline{DRD}$ is a 1/3 cell wide (TVCO/2) pulse whose leading edge is defined by the leading edge of RD. A decode window is developed from the VCO clock.

Shifting the symmetry of the VCO clock effectively shifts the relative position of the $\overline{DRD}$ pulse within the decode window. Decode window control is provided via the WS controls.

In the non-read modes, the PLL is locked to the external reference clock. When the reference input to the PLL is switched, the VCO is stopped momentarily, then restarted in an accurate phase alignment with the next PLL reference input pulse, and the VCO clock divider is reset.

### ADDRESS MARK DETECT

In soft sector read operation the circuit must first detect an address mark to be able to initiate the rest of the read lock sequence. An address mark consists of two sets of 7 "0" patterns followed by two sets of 11 "0" patterns. To begin the read lock sequence the Address Mark Enable ($\overline{AMENB}$) is asserted low by the controller. The address mark detect ($\overline{AMD}$) circuit then initiates a search of the read data (RD) for an address mark. First the $\overline{AMD}$ looks for a set of 6 "0"s within the 7 "0" patterns. Having detected a 6 "0" the $\overline{AMD}$ then looks for a 9 "0" set within the 11 "0"s. If $\overline{AMD}$ does not detect 9 "0"s within 5 RD bits after detecting 6 "0"s it will restart the address mark detect sequence and look for 6 "0"s. When the $\overline{AMD}$ has acquired a 6 "0," 9 "0" sequence, the $\overline{AMD}$ transitions low. $\overline{AMD}$ will remain low for the duration of $\overline{AMENB}$. When $\overline{AMENB}$ is released, $\overline{AMD}$ will be released.

### PREAMBLE SEARCH

After the Address Mark (AM) has been detected, a Read Gate ($\overline{RG}$) can be asserted low, initiating the remainder of the read lock sequence. When $\overline{RG}$ is asserted, an internal counter counts positive transitions of the incoming read data (RD) looking for 3 consecutive "3T" preambles. Once the counter reaches count 3 (finds 3 consecutive 3T preambles) the internal read gate enables, switching the phase detector from the external reference clock to the delayed read data

input ($\overline{DRD}$); at the same time a zero phase (internal) restart signal restarts the VCO in phase with the $\overline{DRD}$. This prepares the VCO to be synchronized to data when the bit sync circuitry is enabled after VCO lock is established.

### VCO LOCK AND BIT SYNC ENABLE

When the internal counter counts 16 more "3T" or a total of 19 positive transitions from RG enable, an internal VCO lock signal enables. The VCO lock signal activates the decoder bit synchronization circuitry to define the proper decode boundaries. Also, at count 19, the internal RCLK source switches from the external reference clock to VCO clock signal which is phase locked to $\overline{DRD}$. The VCO is assumed locked at this point. A maximum of 2 RCLK time periods may occur for the RCLK transition, however, no short duration glitches will occur. After the bit sync circuitry sets the proper decode window (VCO in sync with RCLK and RCLK in sync with the data) NRZ is enabled and data is toggled in to be decoded for the duration of the read gate.

### HARD SECTOR OPERATION

In hard sector operation, a high $\overline{AMENB}$ disables the Address Mark Detection circuitry and $\overline{AMD}$ remains inactive. A hard sector read operation does not require an address mark search but starts with a preamble search as with soft sector and sequences identically. In all respects, with exception to the address mark search sequence, hard sector read operation is the same as soft sector read.

### WRITE MODE

In the write mode the circuit converts NRZ data from the controller into 1, 7 RLL formatted data for storage on the disk. The circuit can operate with a soft or hard sector hard drive.

In soft sector operation the circuit generates a "7, 7, 11, 11" address mark and a preamble pattern ("3T's"). In hard sector operation the circuit generates a 19 x "3T" preamble pattern but no preceding address mark.

NRZ data is clocked into the circuit and latched on defined cell boundaries. The NRZ input data must be synchronous with the rising edges of the WCLK.

Write precompensation circuitry is provided to compensate for media bit shift caused by intersymbol interference. The circuit recognizes specific write data patterns and can add or subtract delays in the time position of write data bits to counteract the read back bit shift. The magnitude of the time shift, TPC, is determined by an external resistor on the WCS pin.

The circuit performs write precompensation according to the algorithm outlined in Table 4.

### SOFT SECTOR

In soft sector operation, when read gate ($\overline{RG}$) transitions high, VCO source and RCLK source switch from RD and 2VCO/3, respectively, to the external reference clock. At the same time the VCO (internal) lock goes inactive but the VCO is locked to the external reference clock. After delay of 1 NRZ time period (min) from $\overline{RG}$ high, the write gate ($\overline{WG}$) can be enabled low while NRZ is maintained (NRZ write data) low. The address mark enable ($\overline{AMENB}$) is made active (low) a minimum of 1 NRZ time period later. The address mark (consisting of 7 "0"s, 7 "0"s, 11 "0"s, 11 "0"s) and the 19 x "3T" preamble is then written by WD. While the preamble is being written, WCLK is clocking in an all "0" NRZ bit pair. The first non-zero NRZ byte input is assumed to be the sync byte. At the end of the write cycle, 8 WCLK cycles of blank NRZ time passes to insure the encoder is flushed of data; $\overline{WG}$ then goes high. WD stops toggling a maximum of 1 NRZ time periods after $\overline{WG}$ goes high.

### HARD SECTOR

In hard sector operation, when read gate ($\overline{RG}$) transitions high, VCO source and RCLK switch references and VCO lock (internal) goes inactive as with soft sector but the $\overline{AMENB}$ (Address Mark Enable) is kept high.

The circuit then sequences from $\overline{RG}$ disable to $\overline{WG}$ enable and NRZ active as in soft sector operation.

### TEST POINTS

The SSI 32D5392 provides two (2) test points which can be utilized to evaluate window margin characteristics.

(a) $\overline{DRD}$, delayed read data – the positive edges represent the data bit position

(b) VCO REF, the VCO reference which represents the input to the Phase Detector, synchronizer, and 1,7 decoder

The following figure describes the relationship between the various test points:

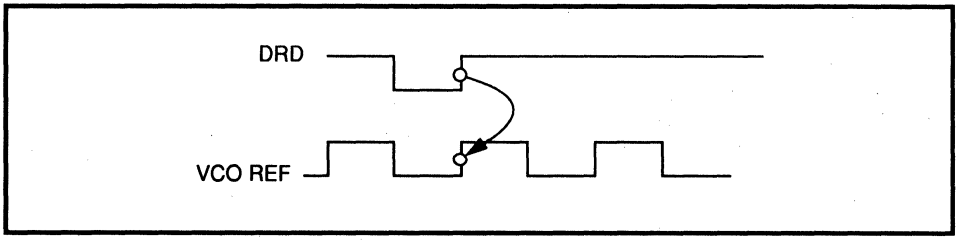



**FIGURE 1: Test Point Relationships**

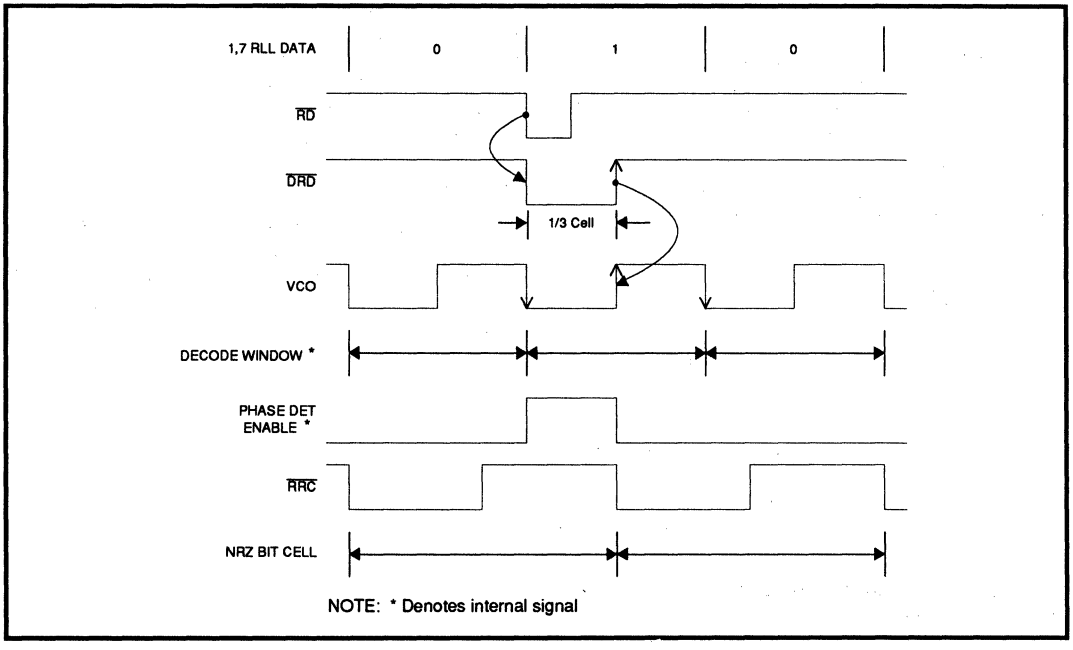



**FIGURE 2: Data Synchronization Waveform**

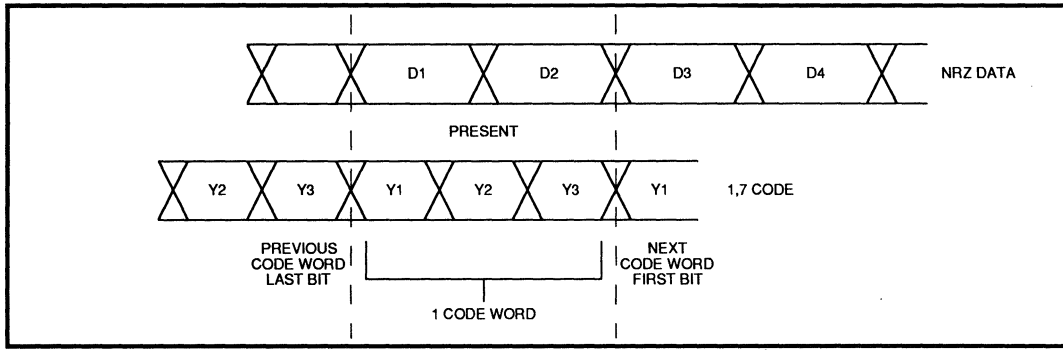



**FIGURE 3: NRZ Data Word Comparision to 1, 7 Code Word (See Tables 1, and 2 for Decode Scheme)**

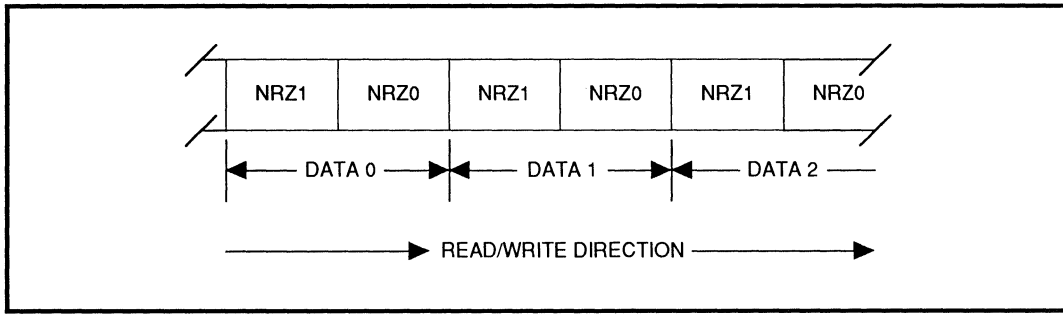



**FIGURE 4: Parallel/Serial Conversion Format**

**TABLE 1: Decode Table for (1, 7) RLL Code Set**

| ENCODED READ DATA | | | DECODED DATA | |
|---|---|---|---|---|
| Previous | Present | Next | | |
| Y Y | Y Y Y | Y Y | D D | |
| 2' 3' | 1 2 3 | 1 2 | 1 2 | |
| 0 0 | 0 0 0 | X X | 0 1 | |
| 1 0 | 0 0 0 | X X | 0 0 | |
| 0 1 | 0 0 0 | X X | 0 1 | |
| X X | 1 0 0 | X X | 1 1 | |
| X 0 | 0 1 0 | 0 0 | 1 1 | |
| X 0 | 0 1 0 | 1 0 | 1 0 | |
| X 0 | 0 1 0 | 0 1 | 1 0 | |
| X 1 | 0 1 0 | 0 0 | 0 1 | |
| X 1 | 0 1 0 | 1 0 | 0 0 | |
| X 1 | 0 1 0 | 0 1 | 0 0 | |
| 0 0 | 0 0 1 | X X | 0 1 | |
| 1 0 | 0 0 1 | X X | 0 0 | |
| 0 1 | 0 0 1 | X X | 0 0 | (Preamble) |
| X X | 1 0 1 | X X | 1 0 | |

**TABLE 2: Encode Table for (1, 7) RLL Code Set**

| NRZ DATA | | | | ENCODED WRITE DATA | | | |
|---|---|---|---|---|---|---|---|
| Present | | Next | | Previous | Present | | |
| D | D | D | D | Y | Y | Y | Y |
| 1 | 2 | 3 | 4 | 3 | 1 | 2 | 3 |
| 0 | 0 | 0 | X | X | 0 | 0 | 1 |
| 0 | 0 | 1 | X | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | X | 1 | 0 | 1 | 0 |
| 1 | 0 | 0 | X | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | X | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 |

NOTE: X = Don't Care

**TABLE 3: Clock Frequency**

| $\overline{WG}$ | $\overline{RG}$ | VCO REF | RCLK | DECCLK | ENCCLK | MODE |
|---|---|---|---|---|---|---|
| 1 | 1 | FREF | 2FREF/3 | N/A | N/A | IDLE |
| 1 | 0 | RD | 2VCO/3 | VCO | FREF | READ |
| 0 | 1 | FREF | 2FREF/3 | FREF | FREF | WRITE |
| 0 | 0 | Undefined | Undefined | Undefined | Undefined | Undefined |

Note 1: Until the VCO locks to the new source, the VCO entries will be FREF.

2: Until the VCO locks to the new source, the 2VCO/3 entries will be 2FREF/3.

**TABLE 4: Write Precompensation Algorithm**

| BIT | BIT | BIT | BIT | BIT | COMPENSATION |
|---|---|---|---|---|---|
| n-2 | n-1 | n | n+1 | n+2 | BIT n |
| 1 | 0 | 1 | 0 | 1 | NONE |
| 0 | 0 | 1 | 0 | 0 | NONE |
| 1 | 0 | 1 | 0 | 0 | EARLY |
| 0 | 0 | 1 | 0 | 1 | LATE |

LATE: Bit n is time shifted (delayed) from its nominal time position towards the bit n+1 time position.

EARLY: Bit n is time shifted (advanced) from its nominal time position towards the bit n-1 time position.

**TABLE 5: Write Precompensation Magnitude**

| $\overline{WP1}$ | $\overline{WP0}$ | MAGNITUDE (WP) |
|---|---|---|
| 0 | 0 | 3 |
| 0 | 1 | 2 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

The nominal magnitude,
TPC = WP x TPC0 is externally set with a resistor on pin WCS.

**TABLE 6: Window Shift Direction**

| WSD | DIRECTION |
|---|---|
| 0 | Early window (+TS) |
| 1 | Late window (-TS) |

**TABLE 7: Window Shift Magnitude**

| $\overline{W2}$ | $\overline{W1}$ | $\overline{W0}$ | MAGNITUDE (WP) |
|---|---|---|---|
| 1 | 1 | 1 | No shift |
| 1 | 1 | 0 | 4% Minimum shift |
| 1 | 0 | 1 | 8% |
| 1 | 0 | 0 | 12% |
| 0 | 1 | 1 | 15% |
| 0 | 1 | 0 | 18% |
| 0 | 0 | 1 | 20% |
| 0 | 0 | 0 | 22% Maximum shift |
| With resistor, RRS, connected between pins RS and VPA:<br>TS = TS0 [RRS/(RRS + 0.8)]<br>2kΩ < RRS | | | |

## PIN DESCRIPTION

### INPUT PINS

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| VPA1, VPA2 | I | 5 volt analog power supply pins |
| VPD | I | 5 volt digital power supply pin |
| AGND | - | Analog ground pin |
| DGND | - | Digital ground pin |
| $\overline{AMENB}$ | I | ADDRESS MARK ENABLE: Used to enable the address mark detection and address mark generation circuitry. Active low TTL input levels. |
| $\overline{DW}$ | I | DIRECT WRITE ENABLE : Used to enable the direct write mode. A high level allows normal write operation. A low level enables the encoder bypass path mode. In this bypass mode, NRZ0 will directly clock the WD Flip-Flop independent of the state of $\overline{WG}$. Pin $\overline{DW}$ has an internal pull up resistor. TTL input levels. |
| EPD | I | ENABLE PHASE DETECTOR: A low level (coast mode) disables the phase detector and enables the Test Mode. This opens the PLL and the VCO will run at the frequency commanded by the voltage on the VCO IN pin. (In the Test Mode, functions normally driven by the VCO are switched to FREF.) Pin EPD has an internal pull-up resistor. TTL input levels. |

**INPUT PINS** (continued)

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| FREF | I | REFERENCE FREQUENCY INPUT: The pin frequency is at one and one-half times the data rate. FREF may be driven either by a direct coupled TTL signal or by an AC coupled ECL signal. |
| RD, $\overline{RD}$ | I | READ DATA: Encoded Read Data from the disk drive read channel. Differential +5 volts offset ECL (PECL) input levels. |
| $\overline{RG}$ | I | READ GATE: Selects the PLL reference input and initiates the PLL synchronization sequence. A low level selects the RD input and enables the read mode/ address detect sequences. A high level selects the XTAL input. See Table 2. TTL input levels. |
| $\overline{W0}$, $\overline{W1}$, $\overline{W2}$ | I | WINDOW CONTROL BITS: In Read Mode, pins $\overline{W0}$ and $\overline{W1}$ and $\overline{W2}$ control the magnitude of the decode window shift. Each pin has an internal pull-up resistor. TTL input levels. |
| WCLK | I | WRITE CLOCK: Write mode dual-bit clock. Must be synchronous with the NRZ input. For short cable delays, WCLK may be connected directly to pin RCLK. For long cable delays, WCLK should be connected to an RCLK return line matched to the NRZ data bus line delay. TTL input levels. |
| $\overline{WP0}$,$\overline{WP1}$ | I | WRITE PRECOMPENSATION CONTROL BITS: In Write Mode, pins $\overline{WP0}$ and $\overline{WP1}$ control the magnitude of the write precompensation. Each pin has an internal pull-up resistor. TTL input levels. |
| $\overline{WG}$ | I | WRITE GATE: Enables the write mode. See Table 2. Active low TTL input levels. |
| WSD | I | WINDOW SYMMETRY DIRECTION CONTROL: Controls the direction of the decode window shift. Pin WSD has an internal pull-up resistor. TTL input levels. |
| **OUTPUT PINS** | | |
| $\overline{AMD}$ | O | ADDRESS MARK DETECT: Tristate output pin that is in its high impedance state when $\overline{WG}$ is low or $\overline{AMENB}$ is high. When $\overline{AMENB}$ is low, this output indicates address mark search status. A latched low level output appears when an address mark has been detected. A high level on pin $\overline{AMENB}$ resets pin $\overline{AMD}$. TTL output levels. |
| $\overline{DRD}$ | O | DELAYED READ DATA: An open emitter ECL output test point. The positive edges of this signal indicate the data bit position. The positive edges of the $\overline{DRD}$ and VCO_REF outputs can be used to estimate window centering. The time jitter of DRD's positive edge is an indication of media bit jitter. Two external resistors are required to use this pin. They should be removed during normal operation to reduce power dissipation. |
| FOEN | O | REFERENCE CLOCK ENABLE: When this output is high, the FREF clock is controlling the internal timing. When this output is low, the FREF clock is internally disabled. The output from pin FOEN can be used to disable the clock applied to the FREF pin to reduce VCO jitter during read modes. TTL output levels. |

**OUTPUT PINS** (continued)

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| RCLK | O | READ CLOCK: A multiplexed dual-bit clock source used by the controller, see Table 2. During a mode change, no glitches are generated and no more than one lost clock pulse will occur. When $\overline{RG}$ goes low, RCLK initially remains synchronized to 2FREF/3. After 19 read data pulses, RCLK is synchronized to the Read Data. When $\overline{RG}$ goes high, RCLK is synchronized back to the 2FREF/3. TTL output levels. |
| SD | O | SYNCHRONIZED DATA: An open emitter ECL output test point. Synchronized data before the decoder. Two external resistors are required to use this pin. They should be removed during normal operation to reduce power dissipation. |
| VCO REF | O | VCO REFERENCE: An open emitter ECL output test point. This is the VCO reference input to the phase detector. The positive edges are phase locked to Delayed Read Data. The negative edges of this open emitter output signal indicate the edges of the decode window. Two external resistors are required to use this pin. They should be removed during normal operation to reduce power dissipation. |
| WD, $\overline{WD}$ | O | WRITE DATA: Encoded write data output. The data is automatically resynchronized (independent of the delay between RRC and WCLK) to the FREF reference clock. Differential ECL output levels. Termination resistors are required. |
| **BIDIRECTIONAL PINS** | | |
| NRZ0, NRZ1 | B | NRZ READ DATA PORT: Dual-bit port. Read data output when $\overline{RG}$ is low, Write data input when $\overline{WG}$ is low. TTL input and output levels. |
| **ANALOG PINS** | | |
| IREF | I | CURRENT REFERENCE INPUT: The VCO center frequency, the 1/3 cell delay, and the phase detector gain are a function of the current sourced into this pin. |
| PD OUT | O | PHASE DETECTOR OUTPUT: Drives the loop filter input. |
| RS | I | WINDOW SYMMETRY ADJUST PIN: This pin allows analog adjustment of the decode window shift magnitude. Used in conjunction with the digital controls $\overline{W0}$ and $\overline{W1}$ and $\overline{W2}$ this pin can be used to scale the magnitude of the preset window shift. Connect resistor to VPA. |
| VCO IN | I | VCO CONTROL INPUT: Driven by the loop filter output. |
| WCS | I | WRITE PRECOMPENSATION SET: Pin for the reference current to set the write precompensation magnitude value. Connect resistor to VPA. |

## ELECTRICAL SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may damage the device.

| PARAMETER | RATING | UNIT |
|---|---|---|
| Supply Voltage, VPA1, VPA2, VPD | -0.3 to 6 | V |
| Storage Temperature | -65 to 150 | °C |
| Lead Temperature (Soldering 10 sec.)<br>FOEN,NRZ, WD, WD*, AMD*, DRD*, | 260 | °C |
| VCOREF pins | -0.3 to (VPA/VPD+0.3),<br>or +12 | V<br>mA |
| All other pins | -0.3 to (VPA/VPD+0.3) | V |

### RECOMMENDED OPERATING CONDITIONS

| | | |
|---|---|---|
| Supply Voltage, VPA1 = VPA2 = VPD = VCC | 4.75 < VCC < 5.25 | V |
| Junction Temperature, Tj | 0 < Tj < 135 | °C |
| Ambient Temperature, Ta | 0 < Ta < 70° | °C |

### ELECTRICAL CHARACTERISTICS

Unless otherwise specified, 4.75 < VPA/VPD < 5.25, 0°C < T(ambient) < 70 °C, 25 °C < T(junction) < 135 °C. Currents flowing into the chip are positive. Current maximums are currents with the highest absolute value.

### POWER SUPPLY CURRENTS AND POWER

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| ICC (VPA, VPD)<br>Supply Current | Outputs and test point pins open, Ta = 70 °C | | 150 | | mA |
| PWR<br>Power Dissipation | Outputs and test point pins open, Ta = 70 °C | | 0.75 | | W |

### DIGITAL INPUTS AND OUTPUTS

**TTL Compatible Inputs:** $\overline{\text{AMENB}}$, EPD, $\overline{\text{DW}}$, $\overline{\text{RG}}$, $\overline{\text{W0}}$, $\overline{\text{W1}}$, $\overline{\text{W2}}$, WCLK, $\overline{\text{WG}}$, $\overline{\text{WP0}}$, $\overline{\text{WP1}}$, NRZ0, NRZ1, FREF Pins

| | | | | | |
|---|---|---|---|---|---|
| Input Low Voltage (VIL) | | -0.3 | | 0.8 | V |
| Input High Voltage (VIH) | | 2.0 | | VPD+0.3 | V |
| Input Low Current | VIL = 0.4 V | 0.0 | | -0.4 | mA |
| Input High Current | VIH = 2.4 V | | | 100 | µA |
| Input Low Current (FREF) | VIL = 0.4 V | 0.0 | | TBD | mA |
| Input High Current (FREF) | VIH = 2.4 V | | | TBD | µA |

**ELECTRICAL CHARACTERISTICS (continued)**

**DIGITAL INPUTS AND OUTPUTS (continued)**

**TTL Compatible Outputs:** $\overline{AMD}$, FOEN, NRZ0, NRZ1, RCLK pins.

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Output Low Voltage | Iol = 4.0 mA | | | 0.5 | V |
| Output High Voltage | Ioh= -400µA | 2.4 | | | V |

**Digital Differential Inputs:** RD, $\overline{RD}$ Pins

| | | | | | |
|---|---|---|---|---|---|
| Input Low Voltage (VIL) | | VPA-2.2 | | VIH-0.5 | V |
| Input High Voltage (VIH) | | VIL+0.5 | | VPA-0.5 | V |
| Differential Voltage | $\lvert V_{RD} - \overline{V_{RD}} \rvert$ | 0.5 | | | V |
| Input Low Current | VIL = Min | -100 | | | µA |
| Input High Current | VIH = Max | | | +100 | µA |

**Digital Differential Outputs:** WD, $\overline{WD}$ Pins

| | | | | | |
|---|---|---|---|---|---|
| Output Low Voltage | Iol = TBD | VPD-2.1 | | | V |
| Output High Voltage | Ioh = TBD | | | VPD-0.7 | V |
| Differential Voltage | $\lvert V_{WD} - \overline{V_{WD}} \rvert$ | 0.5 | | | V |

**Test Point Output Levels**

| | | | | | |
|---|---|---|---|---|---|
| Test Point Output<br>High Level (DRD, VCOREF) | 262Ω to VPA,<br>402Ω to GND, VPA = 5V | | VPA<br>-1.02 | | V |
| Test Point Output<br>Low Level (DRD,VCOREF) | 262Ω to VPA,<br>402Ω to GND, VPA = 5V | | | VPA<br>-1.625 | V |

## DYNAMIC CHARACTERISTICS AND TIMING

### READ MODE

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Read Data Pulse Width (TPRD) | | 8 | | (2)TVCO -8 | ns |
| Read Data Rise Time (TRRD) | 20% to 80%, CL ≤ 10 pF | | | 5 | ns |
| Read Data Fall Time (TFRD) | 80% to 20%, CL ≤ 10 pF | | | 5 | ns |
| Read Clock Rise Time (TRRC) | 0.8V to 2.0V, CL ≤ 15 pF | | | 5 | ns |
| Read Clock Fall Time (TFRC) | 2.0V to 0.8V, CL ≤ 15 pF | | | 5 | ns |
| NRZ (out) Set Up & Hold Time (TDS, TDH) | | 13 | | | ns |
| RCLK Low Time (TLRC) | 0.8V, CL ≤ 15 pF | 13 | | | ns |
| RCLK High Time (THRC) | 2.0V, CL ≤ 15 pF | 15 | | | ns |
| $\overline{AMD}$ Set Up & Hold Time (TAS, TAH) | | 13 | | | ns |
| RRC re-sync period (Tdc2) | | TORC | | (2)TORC | ns |
| Decode Window Centering Accuracy | | | | ±0.75 | ns |
| Decode Window | | TVCO -0.75 | | | ns |

### WRITE MODE

| | | | | | |
|---|---|---|---|---|---|
| Write Data Rise Time (TRWD) | 20% to 80% Points 110Ω to VPD, 160Ω to DGND | | | 5 | ns |
| Write Data Fall Time (TFWD) | 80% to 20% Points 110Ω to VPD, 160Ω to DGND | | | 5 | ns |
| Write Data Clock Rise Time (TRWC) CL ≤ 15 pF | 0.8V to 2.0V, | | | 10 | ns |
| Write Data Clock Fall Time (TFWC) CL ≤ 15 pF | 2.0V to 0.8V, | | | 8 | ns |
| NRZ Set Up Time (TSNRZ) | | 5 | | | ns |
| NRZ Hold Time (THNRZ) | | 5 | | | ns |
| Precompensation Time Shift Magnitude Accuracy (TPC) | TPCO = 0.22 (Rc + 0.53) Rc min=1 kΩ, Rc max=0.3TXTAL | | | | |
| | $\overline{W0}$ = 1, $\overline{W1}$ =1 | -0.5 | | 0.5 | ns |
| | $\overline{W0}$ = 0, $\overline{W1}$ =1 | | TPCO | | ns |
| | $\overline{W0}$ = 1, $\overline{W1}$ =0 | | 2TPCO | | ns |
| | $\overline{W0}$ = 0, $\overline{W1}$ =0 | | 3TPCO | | ns |

**DATA SYNCHRONIZATION**

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| VCO Center Frequency Period (TVCO) | VCO IN=2.7V, VPA=VPD=5V TO=3.6 (RR+1.7), RR=(185/DR)-1.7K | 0.8TO | | 1.2TO | ns |
| VCO Frequency Dynamic Range | 1.0 V ≤ VCO IN ≤ VPA - 0.6V VPA=VPD = 5 V | ± 25 | | ± 45 | % |
| VCO Control Gain (KVCO) | wo = 2π/TVCO 1.0 V ≤ VCO IN ≤ VPA - 0.6V | 0.14 wo | | 0.26 wo | rad/s V |
| Phase Detector Gain (KD) | VPA = VPD = 5V Read: KD = 660/(RR+0.53) PLL REF = $\overline{RD}$, 1T Pattern Non-Read: KD = 330/(RR+0.53) | 0.83KD | | 1.17KD | μA/rad |
| KVCO x KD Product Accuracy | | -28 | | +28 | % |
| VCO Phase Restart Error | Referred to RRC | -1 | | +1 | rad |
| 1/3 Cell Delay | TD=1.8 (RR + 1.7); RR = kΩ | 0.8TD | | 1.2TD | ns |

**MODE CONTROL**

| $\overline{WG}$ | $\overline{RG}$ | $\overline{AMENB}$ | MODES | DESCRIPTION |
|---|---|---|---|---|
| 1 | 1 | 1 | Idle | Idle mode. VCO locked to external FREF reference. RCLK synchronized to FREF. $\overline{AMD}$ tri-state. |
| 1 | 1 | 0 | AM Search | Read mode Address Mark search. VCO locked to external FREF reference. RCLK synchronized to FREF. $\overline{AMD}$ active. |
| 1 | 0 | 1 | Read Data | Read mode preamble search and data acquisition. VCO switched from FREF to RD after preamble lock. RCLK synchronized to RD after 19 "3T" patterns. |
| 1 | 0 | 0 | Undefined | Illegal state. |
| 0 | 1 | 0 | Write AM | Write mode Address Mark insertion. VCO locked to external FREF reference. WD, $\overline{WD}$ active. $\overline{AMD}$ tri-state. |
| 0 | 1 | 1 | Write Data | Write mode preamble insertion and data write. VCO locked to external FREF reference. RCLK synchronized to FREF. WD, $\overline{WD}$ active. $\overline{AMD}$ tri-state. |
| 0 | 0 | 1 | Undefined | Illegal state. |
| 0 | 0 | 0 | Undefined | Illegal state. |

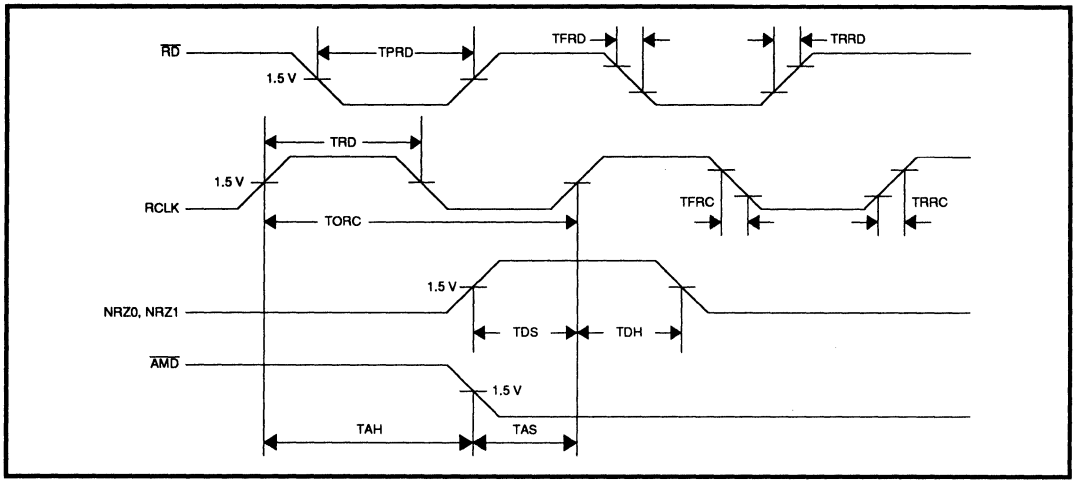



FIGURE 5: Read Timing

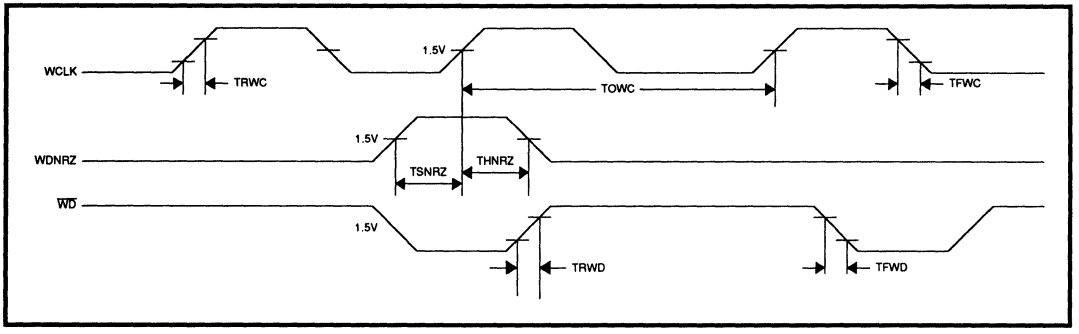



FIGURE 6: Write Timing

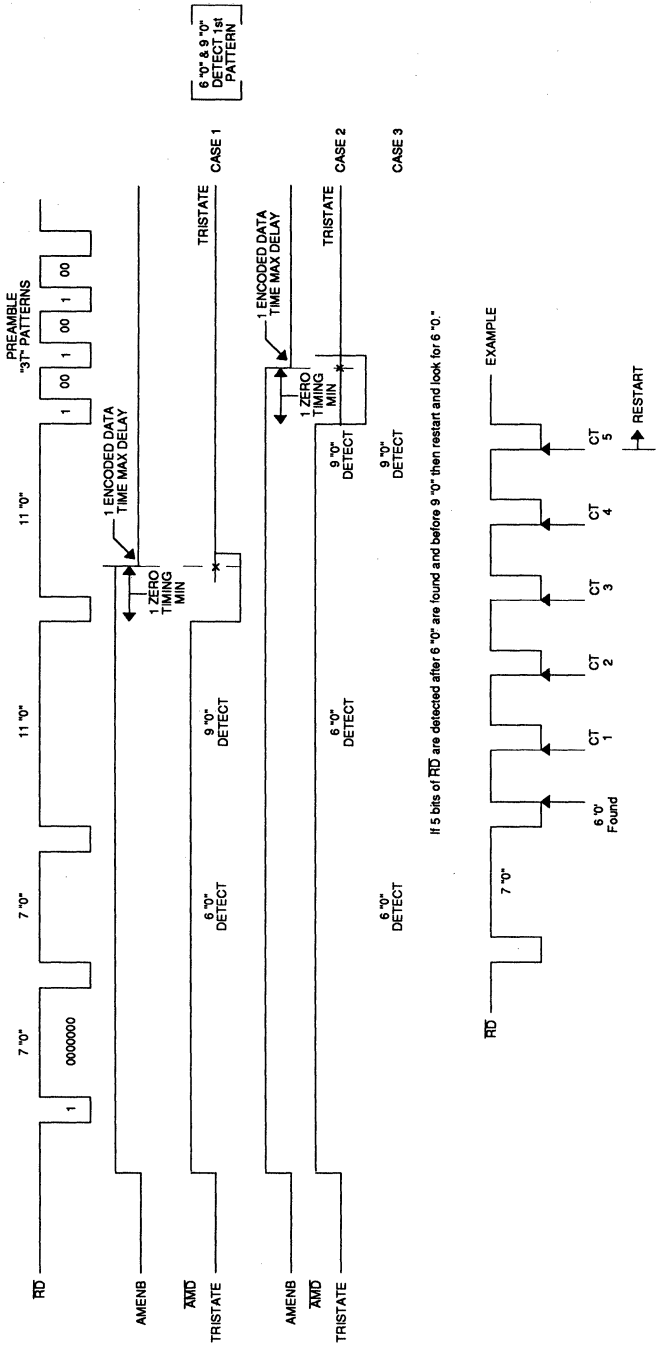



**FIGURE 7: Address Mark Search**

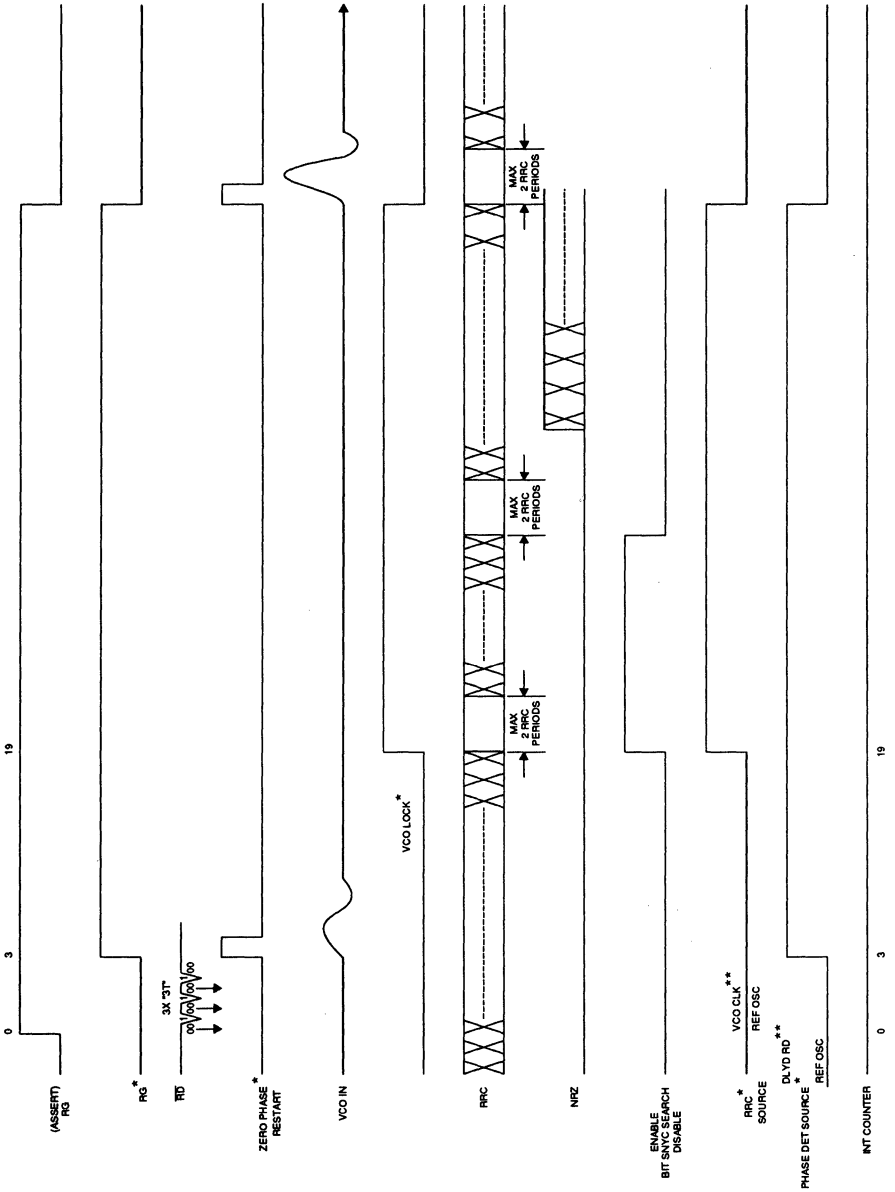



FIGURE 8: Read Mode Locking Sequence (Soft and Hard Sector)

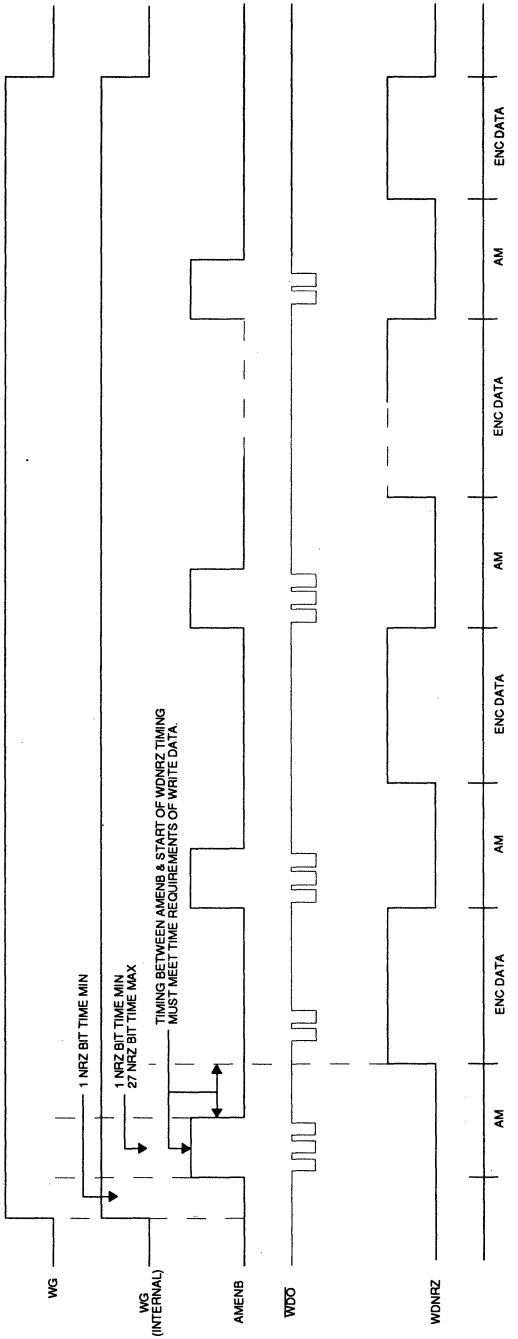



**FIGURE 9: Multiple Address Mark Write**

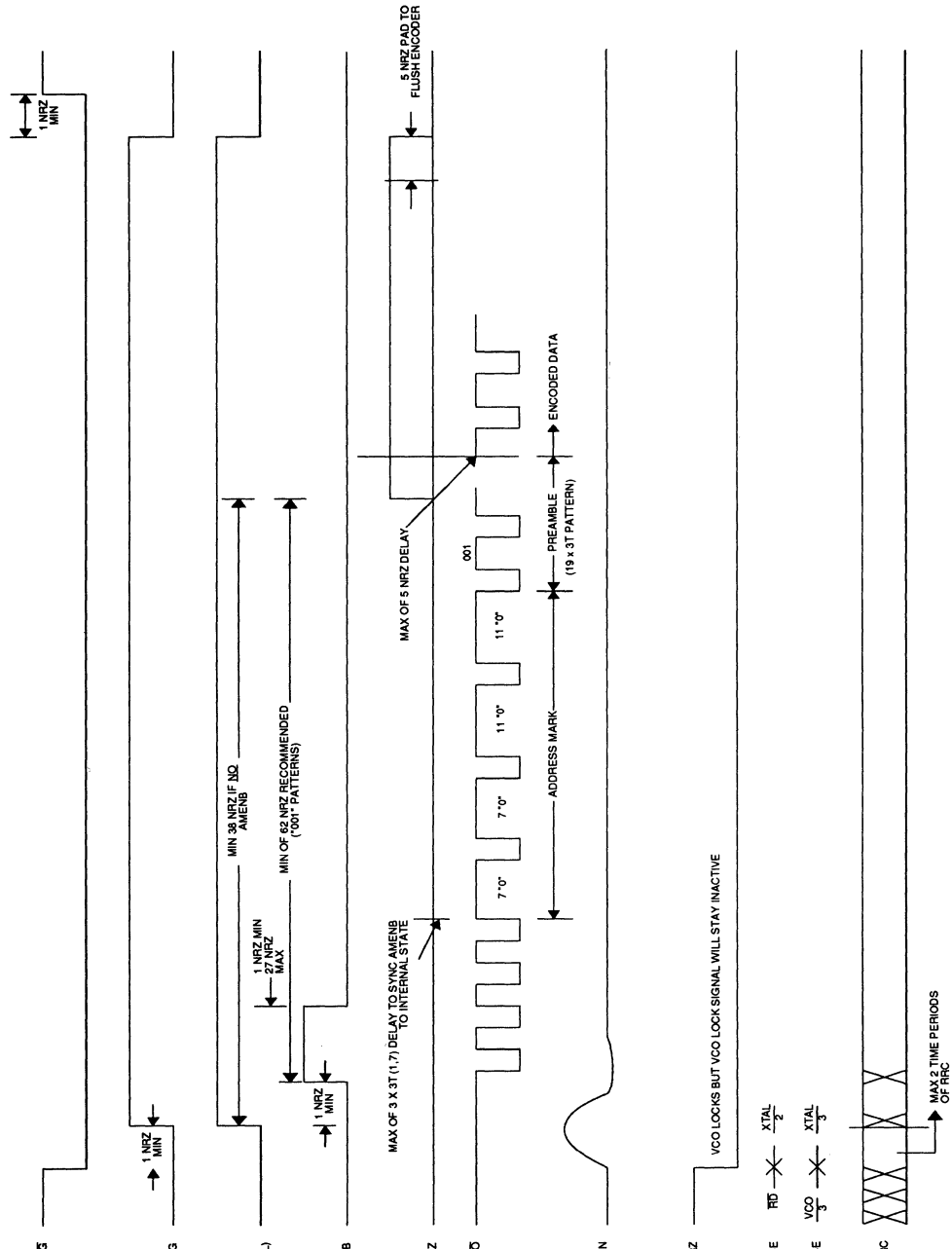
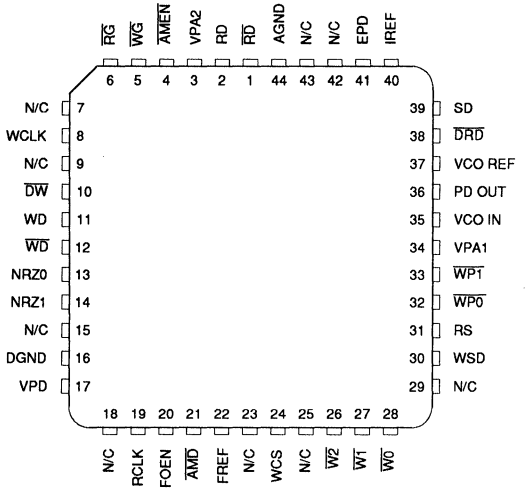



**FIGURE 10: Write Data**

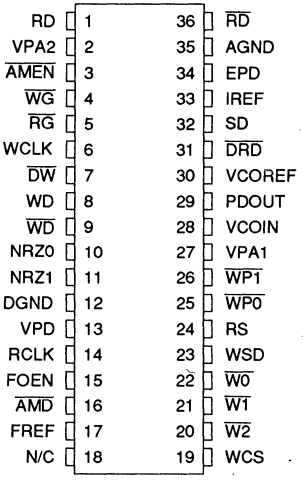
# SSI 32D5392
# Data Sync/1, 7 RLL ENDEC
# with Write Precomp. and Window Shift

## PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.




**44-Pin PLCC**




**36-Pin SOM**

**Advance Information:** Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.



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# SSI 32D5393

## Data Sync/1, 7 RLL ENDEC with Write Precomp. and Window Shift

October 1992

4

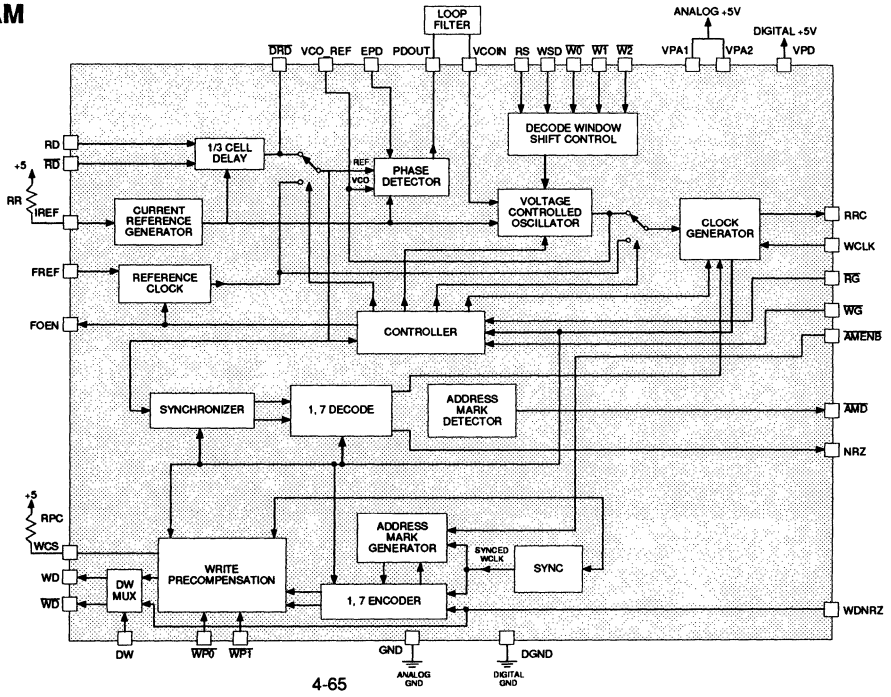
## DESCRIPTION

The SSI 32D5393 Data Synchronizer/1, 7 RLL ENDEC provides data recovery and data encoding for storage systems which employ a 1, 7 RLL encoding format. Data synchronization is performed with a fully integrated high performance PLL. A zero phase restart technique is used to minimize PLL acquisition time. The VCO frequency setting elements are incorporated within the SSI 32D5393 for enhanced performance and reduced board space. Data rate is established with a single external programming resistor. The SSI 32D5393 utilizes an advanced bipolar process technology which affords precise decode window control without the requirement of external devices. The SSI 32D5393 requires a single +5V supply.

## FEATURES

- Data synchronizer and 1, 7 RLL ENDEC
- 24 to 40 Mbit/s operation
  - Data rate programmed with a single external resistor or current source
- Fast acquisition phase locked loop with improved zero phase restart technique
- Fully integrated data separator
  - No external delay lines or active devices required
- Programmable decode window symmetry control
  - Includes delayed read data and VCO clock monitor points
- Programmable write precompensation
- Hard and soft sector operation (hard sector only in 28 pin PLCC)
- Uses standard 5V ± 5% supply
- 28-pin PLCC and 52-lead QFP packages

## BLOCK DIAGRAM



## OPERATION

### DATA/CLOCK RECOVERY CIRCUIT

The circuit is designed to perform data recovery and data encoding in rotating memory systems which utilize a 1, 7 RLL encoding format. In the read mode the circuit performs data synchronization, sync field search and detect, address mark detect, and data decoding. In the write mode, the circuit converts NRZ data into the 1, 7 RLL format described in Table 1, performs write precompensation, generates the preamble field and inserts address marks as requested.

This data rate is established by a single 1% external resistor, RR, connected from the IREF pin to VPA. This resistor establishes a reference current which sets the VCO center frequency, the phase detector gain, and the 1/3 cell delay. The value of this resistor is given by:

$$RR = (185/DR) - 1.7\ k\Omega$$

Where: DR = data rate in Mbit/s

Alternately, the IREF pin can be driven from the SSI 32D4661 in a constant density recording application.

The circuit employs a dual mode phase detector; harmonic in the read mode and non-harmonic in the write and idle modes. In the read mode, the harmonic phase detector updates the PLL with each occurrence of a DLYD DATA pulse. In the write and idle modes, the non-harmonic phase detector is continuously enabled, thus maintaining both phase and frequency lock. By acquiring both phase and frequency lock to the input reference frequency and utilizing a zero phase restart technique, false lock to DLYD DATA is eliminated.

The phase detector incorporates a charge pump in order to drive the loop filter directly. The polarity and width of the output current pulses correspond to the direction and magnitude of the phase error.

The READ GATE ($\overline{RG}$) and WRITE GATE ($\overline{WG}$) inputs control the mode of the data/clock recovery section of the chip.

$\overline{RG}$ is an asynchronous input and may be initiated or terminated at any position on the disk. $\overline{WG}$ is also an asynchronous input, but should not be terminated prior to the last output write data pulse.

### READ OPERATION

The data synchronizer utilizes a fully integrated fast acquisition PLL to accurately develop the decode window. Read Gate, $\overline{RG}$, initiates the PLL locking sequence and selects the PLL reference input; a low level (Read Mode) selects the RD input and a high level selects the external reference clock.

In the read mode the falling edge of $\overline{DRD}$ enables the phase detector while the rising edge is phase compared to the rising edge of VCO. As depicted in Figure X, $\overline{DRD}$ is a 1/3 cell wide (TVCO/2) pulse whose leading edge is defined by the leading edge of RD. A decode window is developed from the VCO clock.

Shifting the symmetry of the VCO clock effectively shifts the relative position of the $\overline{DRD}$ pulse within the decode window. Decode window control is provided via the WS controls.

In the non-read modes, the PLL is locked to the external reference clock. When the reference input to the PLL is switched, the VCO is stopped momentarily, then restarted in an accurate phase alignment with the next PLL reference input pulse, and the VCO clock divider is reset.

### ADDRESS MARK DETECT

In soft sector read operation the circuit must first detect an address mark to be able to initiate the rest of the read lock sequence. An address mark consists of two sets of 7 "0" patterns followed by two sets of 11 "0" patterns. To begin the read lock sequence the Address Mark Enable ($\overline{AMENB}$) is asserted low by the controller. The address mark detect ($\overline{AMD}$) circuit then initiates a search of the read data (RD) for an address mark. First the $\overline{AMD}$ looks for a set of 6 "0"s within the 7 "0" patterns. Having detected a 6 "0" the $\overline{AMD}$ then looks for a 9 "0" set within the 11 "0"s. If $\overline{AMD}$ does not detect 9 "0"s within 5 RD bits after detecting 6 "0"s it will restart the address mark detect sequence and look for 6 "0"s. When the $\overline{AMD}$ has acquired a 6 "0," 9 "0" sequence, the $\overline{AMD}$ transitions low. $\overline{AMD}$ will remain low for the duration of $\overline{AMENB}$. When $\overline{AMENB}$ is released, $\overline{AMD}$ will be released.

### PREAMBLE SEARCH

After the Address Mark (AM) has been detected, a Read Gate ($\overline{RG}$) can be asserted low, initiating the remainder of the read lock sequence. When $\overline{RG}$ is asserted, an internal counter counts positive transitions of the incoming read data (RD) looking for 3 consecutive "3T" preambles. Once the counter reaches count 3 (finds 3 consecutive 3T preambles) the internal read gate enables, switching the phase detector from the external reference clock to the delayed read data

input ($\overline{DRD}$); at the same time a zero phase (internal) restart signal restarts the VCO in phase with the $\overline{DRD}$. This prepares the VCO to be synchronized to data when the bit sync circuitry is enabled after VCO lock is established.

### VCO LOCK AND BIT SYNC ENABLE

When the internal counter counts 16 more "3T" or a total of 19 positive transitions from RG enable, an internal VCO lock signal enables. The VCO lock signal activates the decoder bit synchronization circuitry to define the proper decode boundaries. Also, at count 19, the internal RRC source switches from the external reference clock to VCO clock signal which is phase locked to $\overline{DRD}$. The VCO is assumed locked at this point. A maximum of 2 RRC time periods may occur for the RRC transition, however, no short duration glitches will occur. After the bit sync circuitry sets the proper decode window (VCO in sync with RRC and RRC in sync with the data) NRZ is enabled and data is toggled in to be decoded for the duration of the read gate.

### HARD SECTOR OPERATION

In hard sector operation, a high $\overline{AMENB}$ disables the Address Mark Detection circuitry and $\overline{AMD}$ remains inactive. A hard sector read operation does not require an address mark search but starts with a preamble search as with soft sector and sequences identically. In all respects, with exception to the address mark search sequence, hard sector read operation is the same as soft sector read.

### WRITE MODE

In the write mode the circuit converts NRZ data from the controller into 1, 7 RLL formatted data for storage on the disk. The circuit can operate with a soft or hard sector hard drive.

In soft sector operation the circuit generates a "7, 7, 11, 11" address mark and a preamble pattern ("3T's"). In hard sector operation the circuit generates a 19 x "3T" preamble pattern but no preceding address mark.

WDNRZ data is clocked into the circuit and latched on defined cell boundaries. The NRZ input data must be synchronous with the rising edges of the WCLK.

Write precompensation circuitry is provided to compensate for media bit shift caused by intersymbol interference. The circuit recognizes specific write data patterns and can add or subtract delays in the time position of write data bits to counteract the read back bit shift. The magnitude of the time shift, TPC, is determined by an external resistor on the WCS pin.

The circuit performs write precompensation according to the algorithm outlined in Table 3.

### SOFT SECTOR

In soft sector operation, when read gate ($\overline{RG}$) transitions high, VCO source and RRC source switch from RD and 2VCO/3, respectively, to the external reference clock. At the same time the VCO (internal) lock goes inactive but the VCO is locked to the external reference clock. After delay of 1 NRZ time period (min) from $\overline{RG}$ high, the write gate ($\overline{WG}$) can be enabled low while NRZ is maintained (NRZ write data) low. The address mark enable ($\overline{AMENB}$) is made active (low) a minimum of 1 NRZ time period later. The address mark (consisting of 7 "0"s, 7 "0"s, 11 "0"s, 11 "0"s) and the 19 x "3T" preamble is then written by WD. While the preamble is being written, WCLK is clocking in an all "0" NRZ bit pair. The first non-zero NRZ byte input is assumed to be the sync byte. At the end of the write cycle, 8 WCLK cycles of blank NRZ time passes to insure the encoder is flushed of data; $\overline{WG}$ then goes high. WD stops toggling a maximum of 1 NRZ time periods after $\overline{WG}$ goes high.

### HARD SECTOR

In hard sector operation, when read gate ($\overline{RG}$) transitions high, VCO source and RRC switch references and VCO lock (internal) goes inactive as with soft sector but the $\overline{AMENB}$ (Address Mark Enable) is kept high.

The circuit then sequences from $\overline{RG}$ disable to $\overline{WG}$ enable and NRZ active as in soft sector operation.

### TEST POINTS

The SSI 32D5393 provides two (2) test points which can be utilized to evaluate window margin characteristics.

(a) $\overline{DRD}$, delayed read data – the positive edges represent the data bit position

(b) VCO REF, the VCO reference which represents the input to the Phase Detector, synchronizer, and 1,7 decoder

The following figure describes the relationship between the various test points:

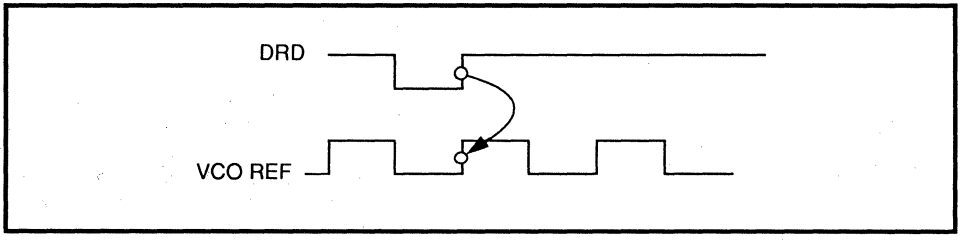



**FIGURE 1: Test Point Relationships**

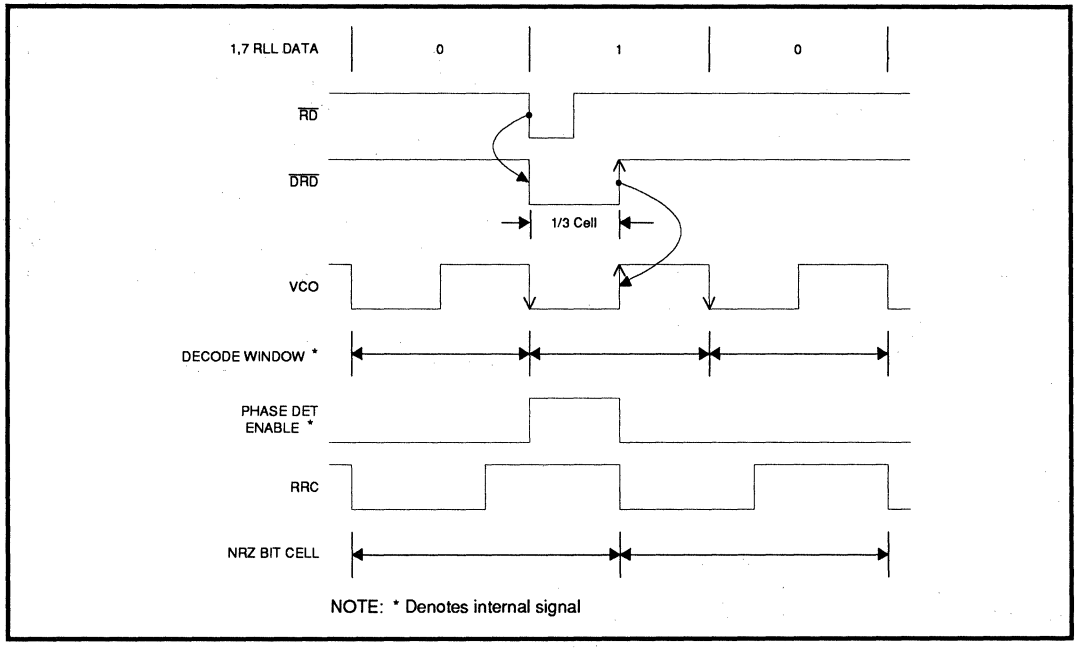



**FIGURE 2: Data Synchronization Waveform**

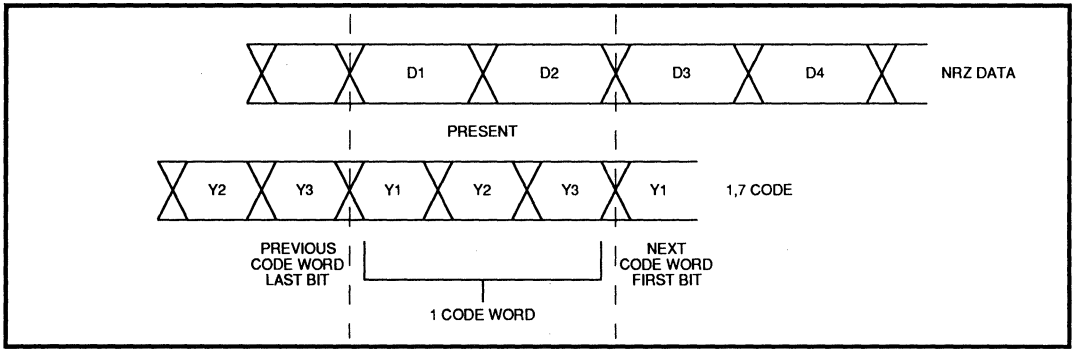



**FIGURE 3: NRZ Data Word Comparision to 1, 7 Code Word (See Tables 1, and 2 for Decode Scheme)**

**TABLE 1: Decode Table for (1, 7) RLL Code Set**

| ENCODED READ DATA | | | DECODED DATA | |
|---|---|---|---|---|
| Previous | Present | Next | | |
| Y Y | Y Y Y | Y Y | D D | |
| 2' 3' | 1 2 3 | 1 2 | 1 2 | |
| 0 0 | 0 0 0 | X X | 0 1 | |
| 1 0 | 0 0 0 | X X | 0 0 | |
| 0 1 | 0 0 0 | X X | 0 1 | |
| X X | 1 0 0 | X X | 1 1 | |
| X 0 | 0 1 0 | 0 0 | 1 1 | |
| X 0 | 0 1 0 | 1 0 | 1 0 | |
| X 0 | 0 1 0 | 0 1 | 1 0 | |
| X 1 | 0 1 0 | 0 0 | 0 1 | |
| X 1 | 0 1 0 | 1 0 | 0 0 | |
| X 1 | 0 1 0 | 0 1 | 0 0 | |
| 0 0 | 0 0 1 | X X | 0 1 | |
| 1 0 | 0 0 1 | X X | 0 0 | |
| 0 1 | 0 0 1 | X X | 0 0 | (Preamble) |
| X X | 1 0 1 | X X | 1 0 | |

**TABLE 2: Encode Table for (1, 7) RLL Code Set**

| NRZ DATA | | | | ENCODED WRITE DATA | | | |
|---|---|---|---|---|---|---|---|
| Present | | Next | | Previous | Present | | |
| D | D | D | D | Y | Y | Y | Y |
| 1 | 2 | 3 | 4 | 3 | 1 | 2 | 3 |
| 0 | 0 | 0 | X | X | 0 | 0 | 1 |
| 0 | 0 | 1 | X | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | X | 1 | 0 | 1 | 0 |
| 1 | 0 | 0 | X | 0 | 1 | 0 | 1 |
| 1 | 0 | 1 | X | 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 |

NOTE: X = Don't Care

**TABLE 3: Clock Frequency**

| $\overline{WG}$ | $\overline{RG}$ | VCO REF | RRC | DECCLK | ENCCLK | MODE |
|---|---|---|---|---|---|---|
| 1 | 1 | FREF | 2FREF/3 | N/A | N/A | IDLE |
| 1 | 0 | RD | 2VCO/3 | VCO | FREF | READ |
| 0 | 1 | FREF | 2FREF/3 | FREF | FREF | WRITE |
| 0 | 0 | Undefined | Undefined | Undefined | Undefined | Undefined |

Note 1: Until the VCO locks to the new source, the VCO entries will be FREF.

2: Until the VCO locks to the new source, the 2VCO/3 entries will be 2FREF/3.

**TABLE 4: Write Precompensation Algorithm**

| BIT | BIT | BIT | BIT | BIT | COMPENSATION |
|---|---|---|---|---|---|
| n-2 | n-1 | n | n+1 | n+2 | BIT n |
| 1 | 0 | 1 | 0 | 1 | NONE |
| 0 | 0 | 1 | 0 | 0 | NONE |
| 1 | 0 | 1 | 0 | 0 | EARLY |
| 0 | 0 | 1 | 0 | 1 | LATE |

LATE: Bit n is time shifted (delayed) from its nominal time position towards the bit n+1 time position.

EARLY: Bit n is time shifted (advanced) from its nominal time position towards the bit n-1 time position.

**TABLE 5: Write Precompensation Magnitude**

| $\overline{WP1}$ | $\overline{WP0}$ | MAGNITUDE (WP) |
|---|---|---|
| 0 | 0 | 3 |
| 0 | 1 | 2 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

The nominal magnitude,
TPC = WP x TPC0 is externally set with a resistor on pin WCS.

**TABLE 6: Window Shift Direction**

| WSD | DIRECTION |
|---|---|
| 0 | Early window (+TS) |
| 1 | Late window (-TS) |

**TABLE 7: Window Shift Magnitude**

| $\overline{W2}$ | $\overline{W1}$ | $\overline{W0}$ | MAGNITUDE (WP) |
|---|---|---|---|
| 1 | 1 | 1 | No shift |
| 1 | 1 | 0 | 4% Minimum shift |
| 1 | 0 | 1 | 8% |
| 1 | 0 | 0 | 12% |
| 0 | 1 | 1 | 15% |
| 0 | 1 | 0 | 18% |
| 0 | 0 | 1 | 20% |
| 0 | 0 | 0 | 22% Maximum shift |
| With resistor, RRS, connected between pins RS and VPA:<br>TS = TS0 [RRS/(RRS + 0.8)]<br>2kΩ < RRS < 16 kΩ | | | |

## PIN DESCRIPTION

### INPUT PINS

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| VPA1, VPA2 | I | 5 volt analog power supply pins |
| VPD | I | 5 volt digital power supply pin |
| AGND | - | Analog ground pin |
| DGND | - | Digital ground pin |
| $\overline{\text{AMENB}}$ | I | ADDRESS MARK ENABLE: Used to enable the address mark detection and address mark generation circuitry. Active low TTL input levels. |
| DW | I | DIRECT WRITE ENABLE : Used to enable the direct write mode. A low level allows normal write operation. A high level enables the encoder bypass path mode. In this bypass mode, WDNRZ will directly drive the WD output independent of the state of WG. Pin DW has an internal pull up resistor. TTL input levels. |
| EPD | I | ENABLE PHASE DETECTOR: A low level (coast mode) disables the phase detector and enables the Test Mode. This opens the PLL and the VCO will run at the frequency commanded by the voltage on the VCO IN pin. (In the Test Mode, functions normally driven by the VCO are switched to FREF.) Pin EPD has an internal pull-up resistor. TTL input levels. |
| FREF | I | REFERENCE FREQUENCY INPUT: The pin frequency is at one and one-half time the data rate. FREF may be driven either by a direct coupled TTL signal or by an AC coupled ECL signal. |
| RD, $\overline{\text{RD}}$ | I | READ DATA: Encoded Read Data from the disk drive read channel. Differential +5 volts offset ECL (PECL) input levels. |
| $\overline{\text{RG}}$ | I | READ GATE: Selects the PLL reference input and initiates the PLL synchronization sequence. A low level selects the RD input and enables the read mode/address detect sequences. A high level selects the XTAL input. See Table 2, TTL input levels. |
| $\overline{\text{W0}}$, $\overline{\text{W1}}$, $\overline{\text{W2}}$ | I | WINDOW CONTROL BITS: In Read Mode, pins $\overline{\text{W0}}$ and $\overline{\text{W1}}$ and $\overline{\text{W2}}$ control the magnitude of the decode window shift. Each pin has an internal pull-up resistor. TTL input levels. |
| WCLK | I | WRITE CLOCK: Write mode bit clock. Must be synchronous with the WDNRZ input. For short cable delays, WCLK may be connected directly to pin RRC. For long cable delays, WCLK should be connected to an RRC return line matched to the WDNRZ data bus line delay. TTL input levels. |
| WDNRZ | I | NRZ WRITE DATA INPUT PIN: This pin can be connected to the NRZ to form a bidirectional data port. Pin WDNRZ has an internal pull-up resistor. TTL input levels. |
| $\overline{\text{WP0}}$,$\overline{\text{WP1}}$ | I | WRITE PRECOMPENSATION CONTROL BITS: In Write Mode, pins $\overline{\text{WP0}}$ and $\overline{\text{WP1}}$ control the magnitude of the write precompensation. Each pin has an internal pull-up resistor. TTL input levels. |
| $\overline{\text{WG}}$ | I | WRITE GATE: Enables the write mode. See Table 2. Active low TTL input levels. |
| WSD | I | WINDOW SYMMETRY DIRECTION CONTROL: Controls the direction of the decode window shift. Pin WSD has an internal pull-up resistor. TTL input levels. |

**OUTPUT PINS**

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| $\overline{AMD}$ | O | ADDRESS MARK DETECT: Tristate output pin that is in its high impedance state when $\overline{WG}$ is low or $\overline{AMENB}$ is high. When $\overline{AMENB}$ is low, this output indicates address mark search status. A latched low level output appears when an address mark has been detected. A high level on pin $\overline{AMENB}$ resets pin $\overline{AMD}$. TTL output levels. |
| $\overline{DRD}$ | O | DELAYED READ DATA: An open emitter ECL output test point. The positive edges of this signal indicate the data bit position. The positive edges of the $\overline{DRD}$ and VCO_REF outputs can be used to estimate window centering. The time jitter of DRD's positive edge is an indication of media bit jitter. Two external resistors are required to use this pin. They should be removed during normal operation to reduce power dissipation. |
| FOEN | O | REFERENCE CLOCK ENABLE: When this output is high, the FREF clock is controlling the internal timing. When this output is low, the FREF clock is internally disabled. The output from pin FOEN can be used to disable the clock applied to the FREF pin to reduce VCO jitter during read modes. TTL output levels. |
| NRZ | O | NRZ READ DATA OUTPUT: Tristate output pin that is enabled when read gate is active. This pin can be connected to the WDNRZ pin to form a bidirectional data port. TTL input levels. |
| RRC | O | READ CLOCK: A multiplexed bit clock source used by the controller, see Table 2. During a mode change, no glitches are generated and no more than one lost clock pulse will occur. When $\overline{RG}$ goes low, RRC initially remains synchronized to 2FREF/3. After 19 read data pulses, RRC is synchronized to the Read Data. When $\overline{RG}$ goes high, RRC is synchronized back to the 2FREF/3. TTL output levels. |
| VCO REF | O | VCO REFERENCE: An open emitter ECL output test point. This is the VCO reference input to the phase detector. The positive edges are phase locked to Delayed Read Data. The negative edges of this open emitter output signal indicate the edges of the decode window. Two external resistors are required to use this pin. They should be removed during normal operation to reduce power dissipation. |
| WD, $\overline{WD}$ | O | WRITE DATA: Encoded write data output. The data is automatically resynchronized (independent of the delay between RRC and WCLK) to the FREF reference clock. Differential ECL output levels. Termination resistors are required. |
| **ANALOG PINS** | | |
| IREF | I | CURRENT REFERENCE INPUT: The VCO center frequency, the 1/3 cell delay, and the phase detector gain are a function of the current sourced into this pin. |
| PD OUT | I/O | PHASE DETECTOR OUTPUT: Drives the loop filter input. |
| RS | I | WINDOW SYMMETRY ADJUST PIN: This pin allows analog adjustment of the decode window shift magnitude. Used in conjunction with the digital controls $\overline{W0}$ and $\overline{W1}$ and $\overline{W2}$ this pin can be used to scale the magnitude of the preset window shift. Connect resistor to VPA. |
| VCO IN | I/O | VCO CONTROL INPUT: Driven by the loop filter output. |
| WCS | I | WRITE PRECOMPENSATION SET: Pin for the reference current to set the write precompensation magnitude value. Connect resistor to VPA. |

## ELECTRICAL SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may damage the device.

| PARAMETER | RATING | UNIT |
|---|---|---|
| Supply Voltage, VPA1, VPA2, VPD | -0.3 to 6 | V |
| Storage Temperature | -65 to 150 | °C |
| Lead Temperature (Soldering 10 sec.)<br>FOEN,NRZ, WD, WD*, AMD*, DRD*, | 260 | °C |
| VCOREF pins | -0.3 to (VPA/VPD+0.3),<br>or +12 | V<br>mA |
| All other pins | -0.3 to (VPA/VPD+0.3) | V |

### RECOMMENDED OPERATING CONDITIONS

| | | |
|---|---|---|
| Supply Voltage, VPA1 = VPA2 = VPD = VCC | 4.75 < VCC < 5.25 | V |
| Junction Temperature, Tj | 0 < Tj < 135 | °C |
| Ambient Temperature, Ta | 0 < Ta < 70° | °C |

### ELECTRICAL CHARACTERISTICS

Unless otherwise specified, 4.75 < VPA/VPD < 5.25, 0°C < T(ambient) < 70 °C, 25 °C < T(junction) < 135 °C. Currents flowing into the chip are positive. Current maximums are currents with the highest absolute value.

### POWER SUPPLY CURRENTS AND POWER

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| ICC (VPA, VPD)<br>Supply Current | Outputs and test point pins<br>open, Ta = 70 °C | | 150 | 195 | mA |
| PWR<br>Power Dissipation | Outputs and test point pins<br>open, Ta = 70 °C | | 0.75 | 1.03 | W |

### DIGITAL INPUTS AND OUTPUTS

**TTL Compatible Inputs:** $\overline{\text{AMENB}}$, EPD, WDNRZ, DW, RG, $\overline{\text{W0}}$, $\overline{\text{W1}}$, $\overline{\text{W2}}$, WCLK, WG, $\overline{\text{WP0}}$, $\overline{\text{WP1}}$, FREF Pins

| | | | | | |
|---|---|---|---|---|---|
| Input Low Voltage (VIL) | | -0.3 | | 0.8 | V |
| Input High Voltage (VIH) | | 2.0 | | VPD+0.3 | V |
| Input Low Current | VIL = 0.4 V | 0.0 | | -0.4 | mA |
| Input High Current | VIH = 2.4 V | | | 100 | µA |
| Input Low Current<br>(FREF) | VIL = 0.4 V | 0.0 | | -0.4 | mA |
| Input High Current<br>(FREF) | VIH = 2.4 V | | | 350 | µA |

**ELECTRICAL CHARACTERISTICS (continued)**

**DIGITAL INPUTS AND OUTPUTS (continued)**

**TTL Compatible Outputs:** $\overline{AMD}$, FOEN, NRZ, RRC pins.

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Output Low Voltage | Iol = 4.0 mA | | | 0.5 | V |
| Output High Voltage | Ioh= -400µA | 2.4 | | | V |

**Digital Differential Inputs:** RD, $\overline{RD}$ Pins

| | | | | | |
|---|---|---|---|---|---|
| Input Low Voltage (VIL) | | VPA-2.2 | | VIH-0.5 | V |
| Input High Voltage (VIH) | | VIL+0.5 | | VPA-0.5 | V |
| Differential Voltage | $\lvert V_{RD} - \overline{V}_{\overline{RD}}\rvert$ | 0.5 | | | V |
| Input Low Current | VIL = Min | -100 | | | µA |
| Input High Current | VIH = Max | | | +100 | µA |

**Digital Differential Outputs:** WD, $\overline{WD}$ Pins

| | | | | | |
|---|---|---|---|---|---|
| Output Low Voltage | Iol = TBD | VPD-2.1 | | | V |
| Output High Voltage | Ioh = TBD | | | VPD-0.7 | V |
| Differential Voltage | $\lvert V_{WD} - \overline{V}_{\overline{WD}}\rvert$ | 0.5 | | | V |

**Test Point Output Levels**

| | | | | | |
|---|---|---|---|---|---|
| Test Point Output<br>High Level (DRD, VCOREF) | 262Ω to VPA,<br>402Ω to GND, VPA = 5V | | VPA<br>-1.02 | | V |
| Test Point Output<br>Low Level (DRD,VCOREF) | 262Ω to VPA,<br>402Ω to GND, VPA = 5V | | | VPA<br>-1.625 | V |

**DYNAMIC CHARACTERISTICS AND TIMING**

**READ MODE**

| | | | | | |
|---|---|---|---|---|---|
| Read Data Pulse Width (TPRD) | | 8 | | (2)TVCO<br>-8 | ns |
| Read Data Rise Time (TRRD) | 20% to 80%, CL ≤ 10 pF | | | 5 | ns |
| Read Data Fall Time (TFRD) | 80% to 20%, CL ≤ 10 pF | | | 5 | ns |
| Read Clock Rise Time (TRRC) | 0.8V to 2.0V, CL ≤ 15 pF | | | 10 | ns |
| Read Clock Fall Time (TFRC) | 2.0V to 0.8V, CL ≤ 15 pF | | | 8 | ns |
| NRZ (out) Set Up &<br>Hold Time (TDS, TDH) | | 10 | | | ns |
| RRC duty cycle | except during re-sync | 40 | | 60 | % |
| (TRD) | during re-sync | 40 | | | % |
| $\overline{AMB}$ Set Up &<br>Hold Time (TAS, TAH) | | 10 | | | ns |
| RRC re-sync period (Tdc2) | | TORC | | (2)TORC | ns |
| 1/3 Cell Delay | TD=1.8 (RR + 1.7); RR = kΩ | 0.8TD | | 1.2TD | ns |

**WRITE MODE**

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Write Data Pulse Width(TWD) | CL ≤ 15 pF, @1.5V<br>TC=1.8(Rc+0.53) | TFREF<br>-TC-1 | | TFREF | ns |
| Write Data Rise Time (TRWD) | 20% to 80% Points<br>110Ωto VPD, 160Ωto DGND | | | 5 | ns |
| Write Data Fall Time (TFWD) | 80% to 20% Points<br>110Ωto VPD, 160Ωto DGND | | | 5 | ns |
| Write Data Clock Rise Time (TRWC) CL ≤ 15 pF | 0.8V to 2.0V, | | | 10 | ns |
| Write Data Clock Fall Time (TFWC) CL ≤ 15 pF | 2.0V to 0.8V, | | | 8 | ns |
| NRZ Set Up Time (TSNRZ) | | 5 | | | ns |
| NRZ Hold Time (THNRZ) | | 5 | | | ns |
| Precompensation Time Shift Magnitude Accuracy (TPC) | TPCO = 0.22 (Rc + 0.53)<br>Rc min=1 KΩ, Rc max=0.3TXTAL | | | | |
| | $\overline{W0}$ = 1, $\overline{W1}$ =1 | -0.5 | | 0.5 | ns |
| | $\overline{W0}$ = 0, $\overline{W1}$ =1 | | TPCO | | ns |
| | $\overline{W0}$ = 1, $\overline{W1}$ =0 | | 2TPCO | | ns |
| | $\overline{W0}$ = 0, $\overline{W1}$ =0 | | 3TPCO | | ns |

**DATA SYNCHRONIZATION**

| | | | | | |
|---|---|---|---|---|---|
| VCO Center Frequency Period (TVCO) | VCO IN=2.7V, VPA=VPD=5V<br>TO=3.6 (RR+1.7),<br>RR=(185/DR)-1.7K | 0.8TO | | 1.2TO | ns |
| VCO Frequency Dynamic Range | 1.0 V ≤ VCO IN<br>≤ VPA - 0.6V<br>VPA=VPD = 5 V | ± 25 | | ± 45 | % |
| VCO Control Gain (KVCO) | wo = 2π/TO<br>1.0 V ≤ VCO IN<br>≤ VPA - 0.6V | 0.14 wo | | 0.26 wo | rad/s V |
| Phase Detector Gain (KD) | VPA = VPD = 5V<br>Read: KD = 660/(RR+0.53)<br>PLL REF = $\overline{RD}$, 1T Pattern<br>Non-Read: KD = 330/(RR+0.53) | 0.83KD | | 1.17KD | µA/rad |
| KVCO x KD Product Accuracy | | -28 | | +28 | % |
| VCO Phase Restart Error | Referred to RRC | -1 | | +1 | rad |
| Decode Window Centering Accuracy | | | | ±0.75 | ns |
| Decode Window | | TVCO -0.75 | | | ns |

**MODE CONTROL**

| RG | WG | $\overline{\text{AMENB}}$ | MODES | DESCRIPTION |
|---|---|---|---|---|
| 1 | 1 | 1 | Idle | Idle mode. VCO locked to external FREF reference. RRC synchronized to FREF NRZ tri-stated. $\overline{\text{AMD}}$ high. |
| 1 | 1 | 0 | AM Search | Read mode Address Mark search. VCO locked to external FREF reference. RRC synchronized to FREF. NRZ tri-stated. $\overline{\text{AMD}}$ active. |
| 1 | 0 | 1 | Read Data | Read mode preamble search and data acquisition. VCO switched from FREF to RD after preamble lock.RRC synchronized to RD after 19 "3T" patterns. NRZ active. |
| 1 | 0 | 0 | Undefined | Illegal state. |
| 0 | 1 | 0 | Write AM | Write mode Address Mark insertion. VCO locked to external FREF reference. Byte clock and 4-bit clock synchronized to FREF. WD, $\overline{\text{WD}}$ active. NRZ0-NRZ7 tri-stated. $\overline{\text{AMD}}$ high. |
| 0 | 1 | 1 | Write Data | Write mode preamble insertion and data write. VCO locked to external FREF reference. RRC synchronized to FREF. WD, $\overline{\text{WD}}$ active. NRZ0 tri-stated. $\overline{\text{AMD}}$ high. |
| 0 | 0 | 1 | Undefined | Illegal state. |
| 0 | 0 | 0 | Undefined | Illegal state. |

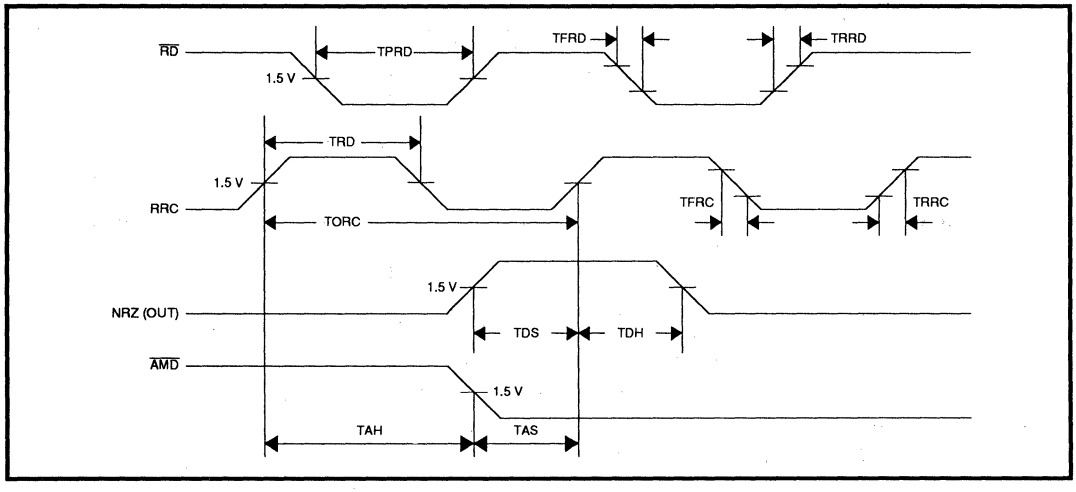



**FIGURE 3: Read Timing**

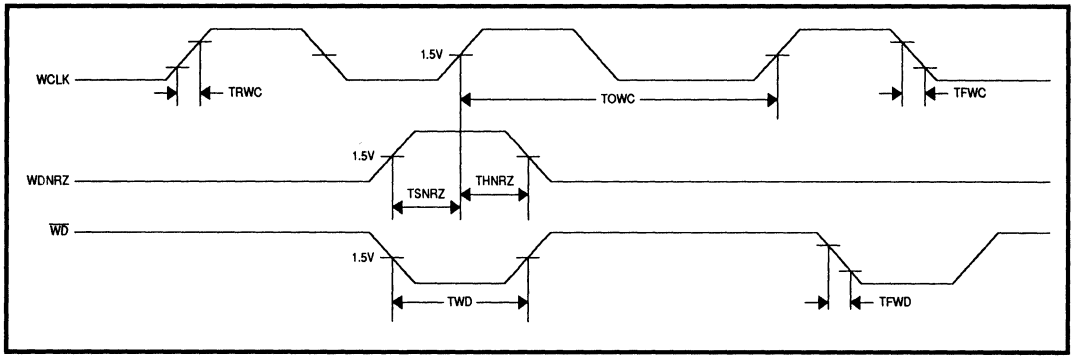



FIGURE 4: Write Timing

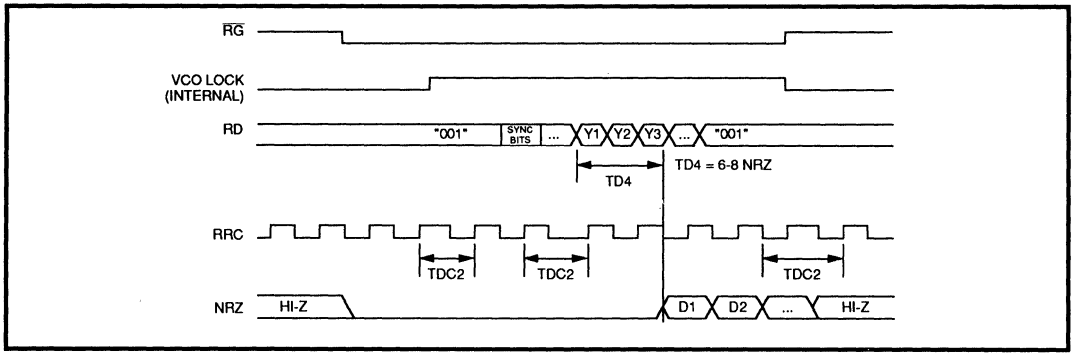



FIGURE 5: Read Mode NRZ Data Timing

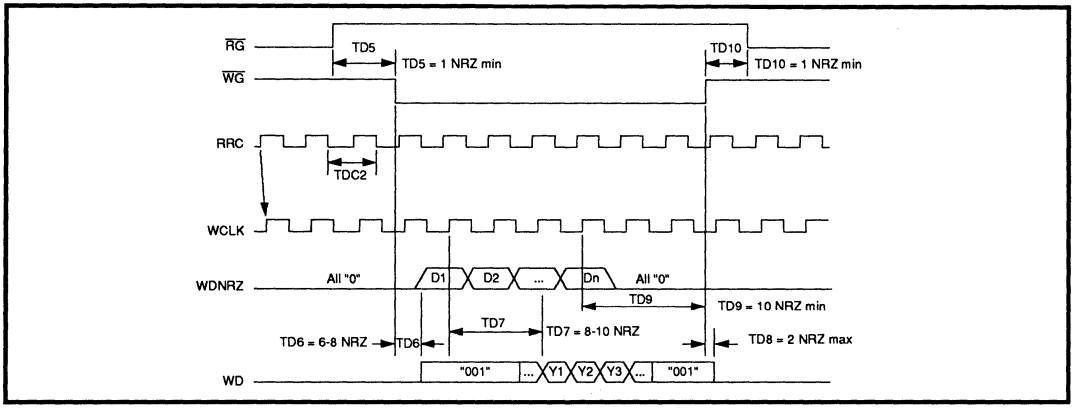



FIGURE 6: Write Mode NRZ Data Timing

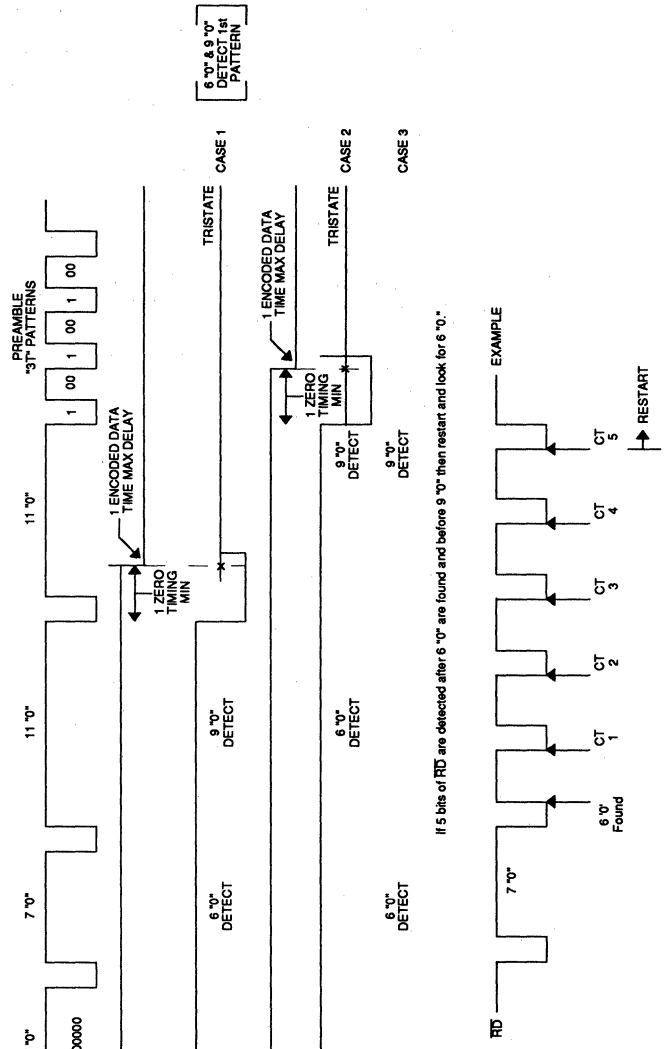



**FIGURE 6: Address Mark Search**

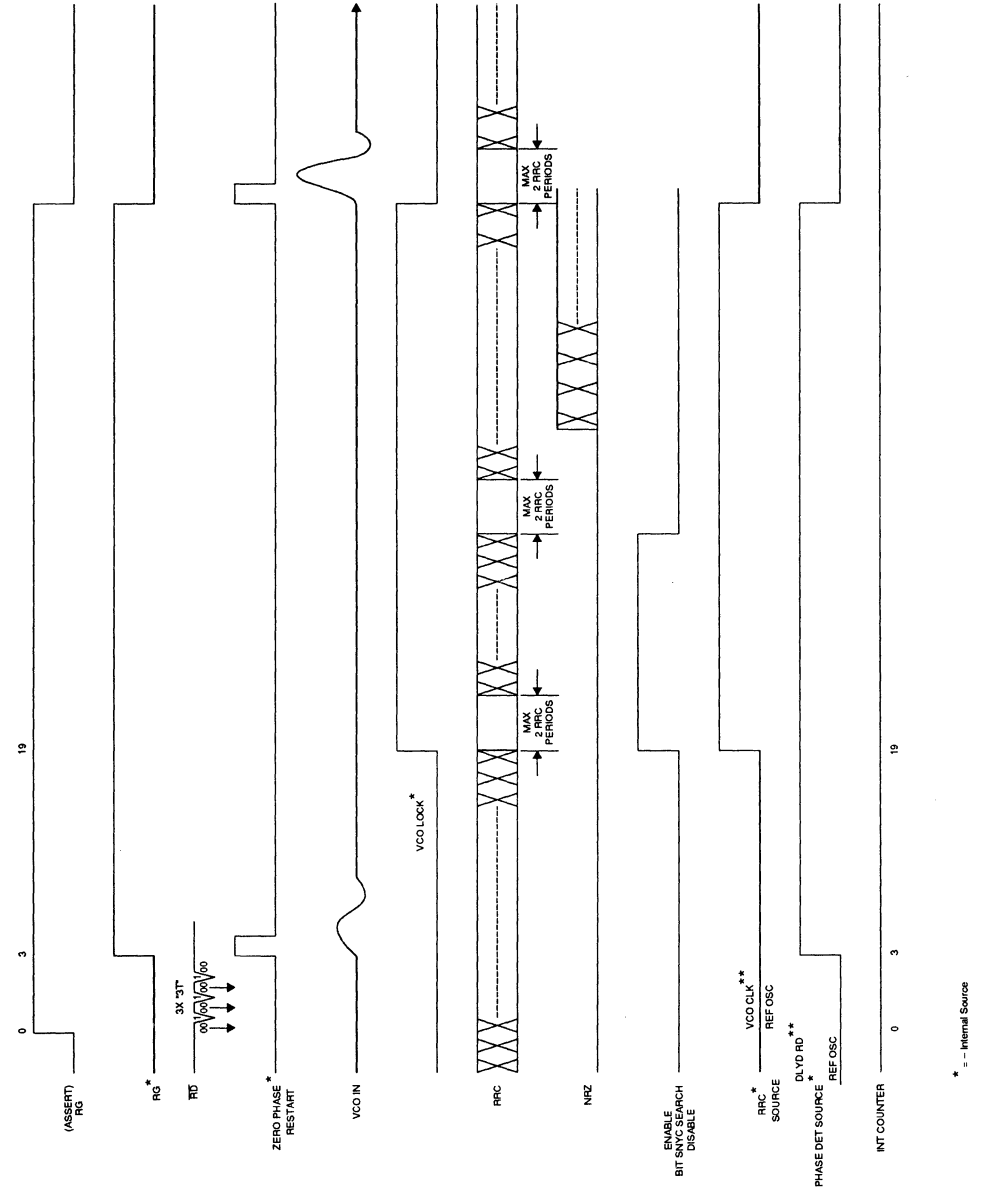



FIGURE 7: Read Mode Locking Sequence (Soft and Hard Sector)

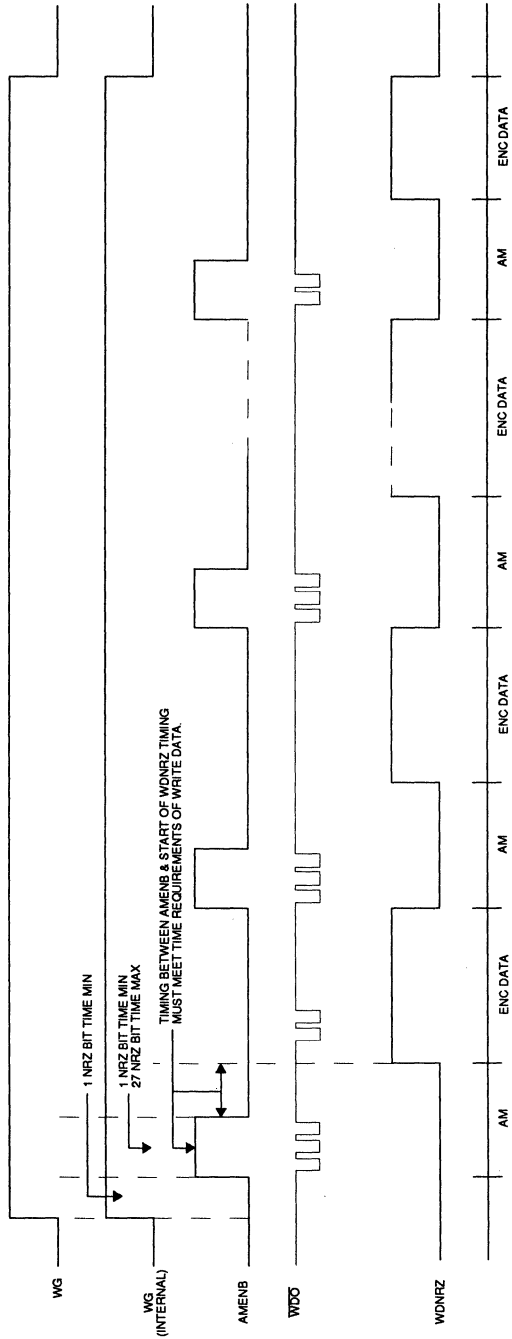



**FIGURE 8: Multiple Address Mark Write**

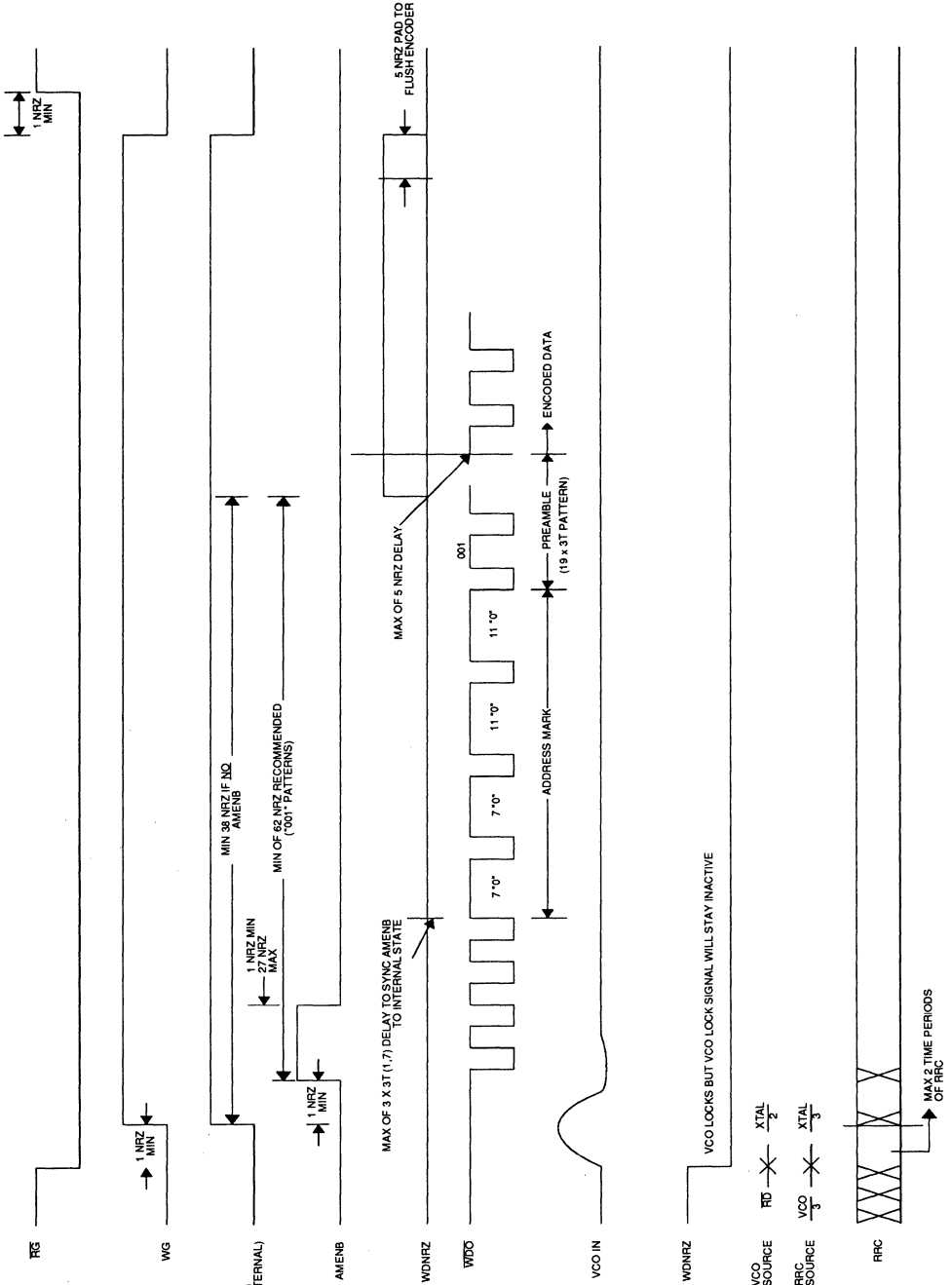
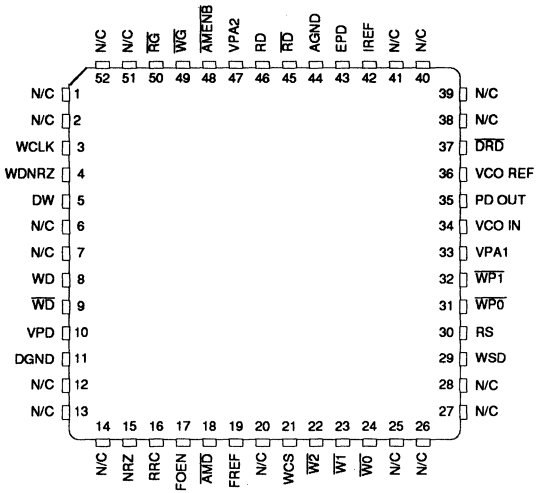



FIGURE 9: Write Data

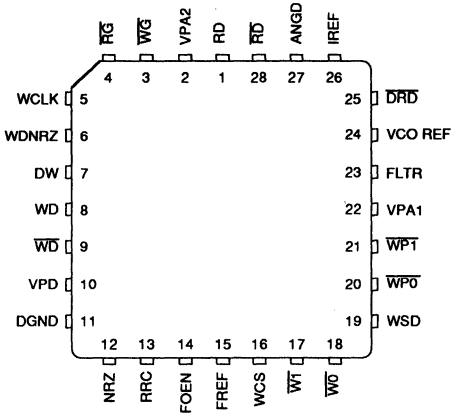
# SSI 32D5393
# Data Sync/1, 7 RLL ENDEC
# with Write Precomp. and Window Shift

## PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.




52-Lead QFP




28-Pin PLCC

## ORDERING INFORMATION

| PART DESCRIPTION | ORDERING NUMBER | PACKAGE MARK |
|---|---|---|
| SSI 32D5393 | | |
| 52-Lead QFP | 32D5393-CG | 32D5393-CG |
| 28-Pin PLCC | 32D5393-CH | 32D5393-CH |



Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 573-6000, FAX (714) 573-6914

silicon systems®
A TDK Group Company

# SSI 32D4040
## Data Sync/1,7 RLL ENDEC

**Advance Information**

January 1993

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## DESCRIPTION

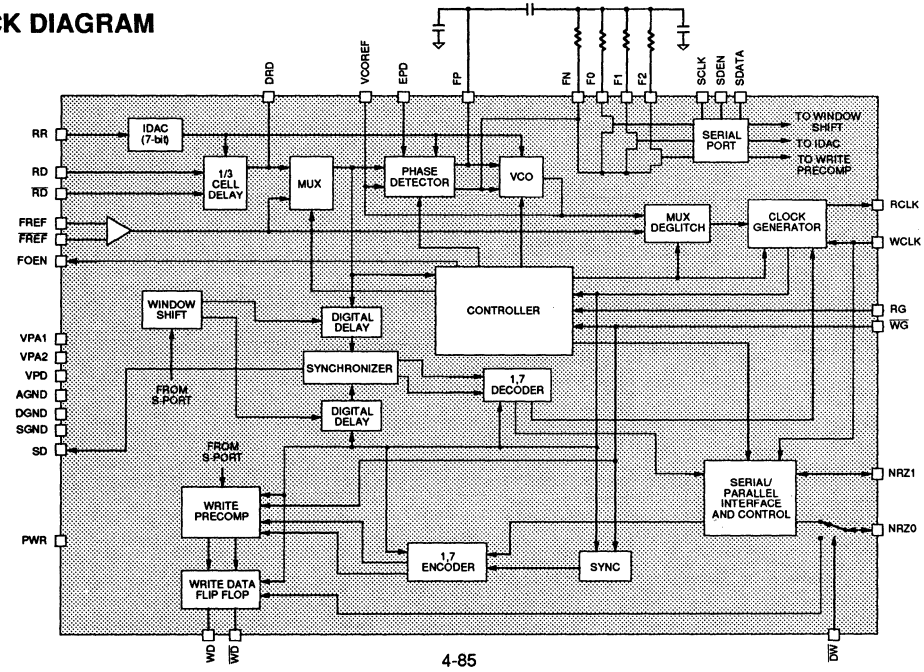
The 32D4040 is a high performance BiCMOS device that provides data encoding, decoding, and synchronization for data storage systems that use RLL 1,7 encoding formats. Data rates from 20 to 64 Mbit/sec can be programmed using an internal DAC whose reference current is set by a single external resistor. Data synchronization is performed by a fully integrated PLL with an advanced zero-phase restart technique that minimizes PLL acquisition time. The PLL is fully differential for maximum performance and noise rejection. For increased system flexibility, the 32D4040 includes inputs for four loop filter damping resistors. These resistors can be switched (using the serial port interface) to change the loop filter characteristics in a zoned recording application.

The 32D4040 utilizes an advanced BiCMOS process technology along with advanced circuit design techniques which result in a high performance device with low power consumption.

## FEATURES

- **Programmable data rates from 20 to 64 Mbit/s**
- **High performance dual-bit NRZ interface**
- **Integrated 1,7 RLL Encoder/Decoder**
- **Fast acquisition phase lock loop with zero phase restart technique**
- **Fully integrated data separator**
  - **No external delay lines or active devices required**
  - **No external active PLL components required**
- **Programmable decode window symmetry control via serial port**
  - **Window shift control ± 30% (4-bit)**
  - **Includes delayed read data and VCO clock monitor points**
- **Programmable write precompensation (3-bit)**
- **Low power operation (550 mW max., < 400 mW nom., < 50 mW sleep mode)**
- **Power supply range (4.3 to 5.5V)**
- **Small footprint 36-lead SOM-FP package**

## BLOCK DIAGRAM



## FUNCTIONAL DESCRIPTION

The 32D4040 circuit provides complete encoding, decoding, and synchronization for RLL 1,7 format data. In the read mode, the circuit performs sync field search and detect, data synchronization, and data decoding. In the write mode, the circuit provides data encoding and write precompensation for NRZ data applied to the NRZ0/1 pins. Data rate is established by the external reference frequency applied to FREF/$\overline{\text{FREF}}$ and an internal DAC (IDAC). The DAC generates a reference current which sets the VCO center frequency, the phase detector gain, and the 1/3 cell delay. The VCO center frequency is determined by the following equation:

$$\text{FVCO} = 1/\text{TVCO}$$

Where TVCO = 1.64 + (0.163RR/DACI); TVCO in nanoseconds, RR is the external RR value, and DACI is the value in programmed through the serial part for DACI.

The circuit employs a dual mode phase detector; harmonic in the read mode and non-harmonic in the write and idle modes. In the read mode the harmonic phase detector updates the PLL with each occurrence of a $\overline{\text{DRD}}$ pulse. In the write and idle modes the non-harmonic phase detector is continuously enabled, thus maintaining both phase and frequency lock onto the reference frequency of the internal time base generator. By acquiring both phase and frequency lock to the input reference frequency and utilizing a zero phase restart technique, the VCO transient is minimized and false lock to DLYD DATA is eliminated. The phase detector incorporates a charge pump in order to drive the loop filter directly. The polarity and width of the output current pulses correspond to the direction and magnitude of the phase error. The data synchronizer requires an external passive loop filter to control its PLL locking characteristics. The filter is fully-differential and balanced in order to suppress common mode noise which may be generated from the time base generator's PLL.

The read gate (RG) and write gate ($\overline{\text{WG}}$) inputs control the device operating mode. RG is an asynchronous input that should be initiated at the start of the preamble pattern. It may be terminated at any position on the disk. $\overline{\text{WG}}$ is also an asynchronous input that can be initiated at any position on the disk. $\overline{\text{WG}}$ should not be terminated prior to the last output write data pulse.

### READ MODE

The data synchronizer utilizes a fully integrated fast acquisition PLL to accurately develop the decode window. Read gate (RG) initiates the PLL locking sequence and selects the PLL reference input; a high level (read mode) selects the internal RD input and a low level selects the reference clock. In the read mode the falling edge of DRD* enables the phase detector while the rising edge is phase compared to the rising edge of the VCO reference (VCOR.) As depicted in Figure 3, $\overline{\text{DRD}}$ is a 1/3 cell wide (TVCO) pulse whose leading edge is defined by the falling edge of $\overline{\text{RD}}$. A decode window is developed from the VCOR clock.

#### Preamble Search

RG is asserted to initiate the preamble search. When RG is asserted, an internal counter is triggered to count positive transitions of the incoming read data, RD/$\overline{\text{RD}}$ (looking for 3 consecutive 3T preambles). Once the counter reaches count 3 (3 consecutive transitions detected) the internal read gate is enabled. This switches the phase detector reference from the FREF/$\overline{\text{FREF}}$ input to the delayed read data ($\overline{\text{DRD}}$) signal. At the same time an internal zero phase restart signal restarts the VCO in phase with the $\overline{\text{DRD}}$. This prepares the VCO to be synchronized to data when the bit sync circuitry is enabled after VCO lock is established. Refer to Figure 5 for a detailed timing diagram.

#### VCO Lock and Bit Sync Enable

While the counter counts an additional sixteen (16) $\overline{\text{DRD}}$ transitions (a total of 19 x 3T from assertion of RG) an internal VCO lock signal is asserted. The VCO lock signal activates the decoder bit synchronization circuitry to define the proper decode boundries. The following 3T patterns are used to set the proper decode window until it has been acquired so that VCO is in sync with RCLK and RCLK is in sync with the data. After the additional 16 transitions, the NRZ0/1 output is enabled and the data is toggled through the decoder for the duration of the RG.

When the decode window is determined, the internal RCLK source is also switched from the FREF/$\overline{\text{FREF}}$ input to the VCO clock signal that is phase locked to $\overline{\text{DRD}}$. During the internal RCLK swicthing period the external RCLK signal may be held for a maximum of 2 NRZ clock periods, however no short duration glitches will occur.

### Window Shift

Shifting the phase of the VCO clock effectively shifts the relative position of the $\overline{DRD}$ pulse within the decode window. Decode window control is provided via the WS control bits of the Window Shift (WS) register. Further description of the WS register is provided in section 5.5.

### NON-READ MODE

In the Non-Read modes, the PLL is locked to the reference clock. This forces the VCO to run at a frequency which is very close to that required for tracking actual data When the reference input to the PLL is switched, the VCO is stopped momentarily, then restarted in an accurate phase alignment with the next PLL reference input pulse. By minimizing the phase alignment error in this manner, the acquisition time is substantially reduced.

### WRITE MODE

In the Write mode the circuit converts NRZ data from the controller into 1,7 RLL formatted data for storage on the disk. Write mode is entered by asserting the write gate ($\overline{WG}$) low while the RG is held low. During write mode the VCO and the RCLK are referenced to the external FREF/$\overline{FREF}$ input signal.

When $\overline{WG}$ is asserted, the NRZ0/1 pins should be held low while the 32D4040 generates the 3T preamble pattern. 3T patterns will be generated as long as the NRZ0/1 pins are both held low. While the preamble is being written the encoder is active. Therefore, WCLK must be toggling and NRZ0/1 must be held low ("0".) The first non zero NRZ0/1 input bit indicates the end of the preamble pattern. After a delay of 5-6 WCLK time periods, non-preamble data begins to toggle out WD/$\overline{WD}$. At the end of the write cycle, 3 WCLK periods of blank NRZ data are required to insure the encoder is flushed of data before the $\overline{WG}$ can be transitioned low. WD/$\overline{WD}$ stops toggling a maximum of 1 WCLK time period after $\overline{WG}$ goes low. Reference Figure 6 for detailed timing information.

**Direct Write Function:** The 32D4040 includes a Direct Write ($\overline{DW}$) function that allows the NRZ0 data to bypass the encoder and write precomp circuitry. When the $\overline{DW}$ bit is driven low, the data applied to NRZ0 will bypass the encoder and write precomp and directly control the write data flip-flop. This allows the user to perform DC erase and media tests.

**TABLE 1: Mode Control**

| $\overline{WG}$ | RG | MODE |
|---|---|---|
| 1 | 0 | IDLE - VCO locked to FREF/$\overline{FREF}$ input. RCLK synchronized to FREF/$\overline{FREF}$. NRZ0 and NRZ1 are tri-stated. |
| 1 | 1 | READ MODE - Preamble search and PLL acquisition on data applied to RD/$\overline{RD}$. VCO switched to $\overline{DRD}$ after first 3 transitions on RD/$\overline{RD}$. After 19 transitions on RD/$\overline{RD}$, RCLK switched to VCO and NRZ0/NRZ1 are active. |
| 0 | 0 | WRITE MODE - Preamble generated and write data encoded. VCO is locked to FREF/$\overline{FREF}$. RCLK is driven by FREF/$\overline{FREF}$. WD/$\overline{WD}$ are active. |
| 0 | 1 | UNDEFINED - Illegal state. |

## FUNCTIONAL DESCRIPTION (continued)

### LOOP FILTER

The 32D4040 employs a differential loop filter for maximum noise supression. The charge pump sinks current from one side of the filter while sourcing current to the other side of the filter depending on the sign of the phase error. A common mode feedback circuit is employed to keep the output levels of the filter centered about VPA/2. The damping characteristics of the loop filter are determined by resistors connected to F0, F1, and F2. The internal FET switches between F0, F1, and F2 are enabled by bits in the Filter Control (FC) register. The external resistors can be switched-in to change the damping characteristics of the loop filter.

### POWER CONTROL

For power management, the PWR pin can be pulled low to disable power to the device. Register information is retained during the sleep mode so it is not necessary to reprogram the serial port registers after returning to an active mode.

### SERIAL INTERFACE OPERATION

The serial interface is a write only port for programming the internal registers of the 32D4040. For data transfers SDEN is brought high, serial data is presented at the SDATA pin, and a serial clock is applied to the SCLK pin. After the SDEN goes high, pulses applied to the SCLK pin will shift the data presented at the SDATA pin into an internal shift register on the falling edge of each clock. The internal shift register will continue to shift data through as long as SDEN is high and SCLK is toggling. The last 8 data bits in the shift register are latched on the falling edge of SDEN.

All transfers are shifted into the serial port MSB first. The first 4-bits of the transfer are the address information. Table 1 provides register mapping information. The second 4-bits contain the programming data. At initial power-up, the contents of the internal registers will be in an unknown state and they must be programmed prior to operation. During power down modes, the serial port remains active and register programming data is retained.

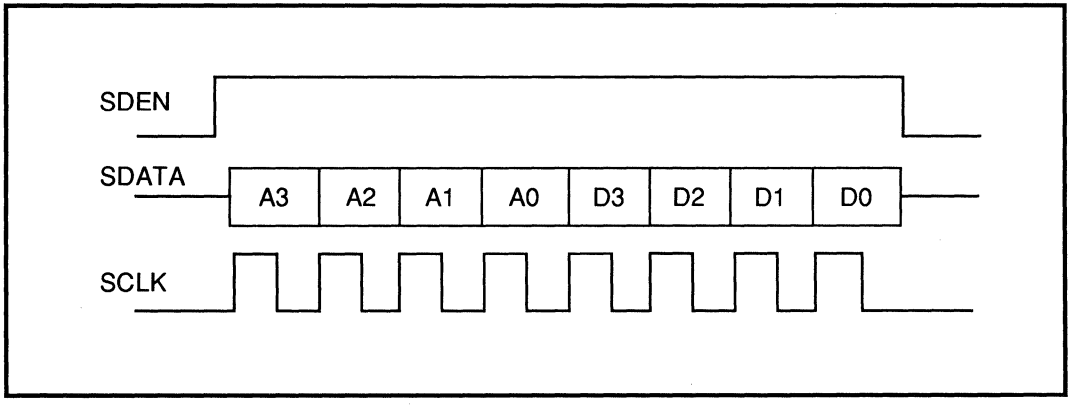



**FIGURE 1: Serial Port Data Transfer Format**

**TABLE 2: Serial Port Register Map**

| A3 | A2 | A1 | A0 | D3 | D2 | D1 | D0 | REGISTER |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | WSD | FS2 | FS1 | FS0 | Filter Control |
| 0 | 0 | 1 | 0 | TM | WP2 | WP1 | WP0 | Write Precomp |
| 0 | 0 | 1 | 1 | W3 | W2 | W1 | W0 | Window Shift |
| 0 | 1 | 1 | 0 | BYP | I6 | I5 | I4 | IDAC upper bits |
| 0 | 1 | 1 | 1 | I3 | I2 | I1 | I0 | IDAC lower bits |

During normal operation TM should be set to logic value "0." AC performance may be somewhat compromised if TM is set to "1." This bit is used during wafer probe to help measure key voltage levels inside the circuit. Also when the TM bit is set to "1" the write flip-flop is bypassed.

When BYP is set to "1," the write precomp circuit is bypassed, except for the write flip-flop, which is controlled by TM. In addition the window shift function is controlled by the BYP bit. In order to minimize jitter in the synchronization, the window shift circuit should be bypassed when the magnitude of window shift is set to 0. This is what occurs when BYP is set to "0." To allow more accurate testing of the jitter and timing offsets introduced by the window shift circuitry, the window shift circuitry is not bypassed when BYP is set to "1."

## PIN DESCRIPTION

### POWER SUPPLY PINS

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| VPA1 | | +5V analog power supply pin |
| VPA2 | | +5 V analog power supply pin |
| VPD | | TTL buffer I/O digital power supply pin |
| AGND | | Analog ground pin |
| DGND | | Digital ground pin |
| SGND | | Substrate ground pin |

### INPUT PINS

| | | |
|---|---|---|
| $\overline{DW}$ | I | DIRECTWRITE: TTL compatible. A low level on this input will allow the data provided on NRZ0 to directly clock the write data flip-flop. This pin has an internal pull-up. |
| EPD | I | ENABLE PHASE DETECTOR: TTL compatible. A low level disables the phase detector and places the VCO in a coast mode. The VCO will run at the frequency determined by the voltage across FP and FN. In this mode, FREF/$\overline{FREF}$ is used as the internal clock for all other functions. |
| FREF/$\overline{FREF}$ | I | REFERENCE FREQUENCY: Pseudo-ECL. A differential reference frequency of 1.5x the data rate should be dc-coupled into these pins. |
| RR | I | REFERENCE RESISTOR INPUT: An external 1% resistor is connected from this pin to AGND to establish a precise internal reference current for the IDAC. The value of this external resistor should be 4.75k. The voltage at this pin should be both temperature and supply compensated at 1.5 volts. |
| PWR | I | POWER: TTL compatible. A low level places all circuitry (except serial port) in a low power sleep mode. |
| RD/$\overline{RD}$ | I | READ DATA: Differential pseudo-ECL. Encoded read data input from the pulse detector device. |
| RG | I | READ GATE: TTL compatible read gate input. A high level TTL input selects the RD input as the phase detector source and enables the read mode. A low level selects the FREF input as the phase detector source. See Table 1. |
| WCLK | I | WRITE CLOCK: TTL compatible. Must be synchronous with the Write Data NRZ input. For short cable delays, WCLK may be connected directly to pin RCLK. For long cable delays, WCLK should be connected to an RCLK return line matched to the NRZ data bus line delay. |
| $\overline{WG}$ | I | WRITE GATE: TTL compatible. A low level TTL input enables the write mode. See Table 1. |

**OUTPUT PINS**

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| $\overline{DRD}$ | O | DELAYED READ DATA TEST POINT: Open emitter ECL test point. This signal represents that output of the 1/3 cell delay element. In read mode, the phase detector compares the positive edge of this signal to the positive edge of the VCO reference. Two external resistors are required to use this pin. They should be removed during normal operation to reduce power dissipation. |
| FOEN | O | FREQUENCY REFERENCE ENABLE: TTL compatible. When this pin is high, the FREF/$\overline{FREF}$ clock is enabled internally. This pin goes low (internally disabling the FREF/$\overline{FREF}$ clock) when RG is active, 19 x 3T patterns have been detected, and the VCO output is switched over as the source for RCLK. This signal can be used to disable the external reference source for improved jitter performance. |
| RCLK | O | READ REFERENCE CLOCK: TTL compatible. During a mode change, no glitches are generated and no more than one lost clock pulse will occur. When RG goes high, RCLK initially remains synchronized to FOUT/3. When the Sync Bits are detected, RCLK is synchronized to the Read Data. When RG goes low, RCLK is synchronized back to the FOUT/3. |
| SD | O | SYCHRONIZED DATA TEST POINT: Open emitter ECL test point. The positive edges of this signal represent the data out of the synchronizer. Two external resistors are required to use this pin. They should be removed during normal operation to reduce power dissipation. |
| VCO_REF | O | VCO REFERENCE TEST POINT: Open emitter ECL test point. This signal represents that VCO reference intput to the phase detector. Two external resistors are required to use this pin. They should be removed during normal operation to reduce power dissipation. |
| WD/$\overline{WD}$ | O | WRITE DATA: Differential pseudo-ECL. Output of the write data flip-flop that is synchronized to the FREF/FREF reference clock. When direct write is active WD/WD is directly controlled by the data on NRZ0. |

**BIDIRECTIONAL PINS**

| | | |
|---|---|---|
| F0, 1, 2 | I/O | LOOP FILTER RESISTORS: Loop filter damping resistors are connected to these pins to establish the loop characteristics. Internal FETs can be enabled to connect the resistors to the FN side of the VCO. The filter control register is programmed to select the desired resistor(s). |
| FP/FN | I/O | PLL LOOP FILTER: These pins are the connection points for the loop filter. FP is the positive output of the phase detector, FN is the negative output of the phase detector. The effective VCO voltage is FP - FN. |
| NRZ0/1 | I/O | NRZ DATA PORT: TTL compatible. Read data outputs when RG is high. Write data inputs when WG is high. |

## PIN DESCRIPTION (continued)

### SERIAL PORT PINS

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| SDEN | I | SERIAL DATA ENABLE: Serial enable TTL compatible input. A high level input enables the serial port. |
| SDATA | I | SERIAL DATA: Serial data TTL compatible input. NRZ programming data for the internal registers is applied to this input. |
| SCLK | I | SERIAL CLOCK: Serial clock TTL compatible input. The clock applied to this pin is synchronized with the data applied to SDATA. |

## ELECTRICAL SPECIFICATIONS

Unless otherwise specified, the recommended operating conditions are as follows: 4.5V < POSITIVE SUPPLY VOLTAGE < 5.5V, 0°C < T (ambient) < 70°C, and 25°C < T(junction) < 135°C. Currents flowing into the chip are positive. Current maximums are currents with the highest absolute value.

### ABSOLUTE MAXIMUM RATINGS

Operation beyond the maximum ratings may damage the device.

| PARAMETER | RATING |
|---|---|
| Storage Temperature | -65 to 150°C |
| Junction Operating Temperature | +135°C |
| Positive Supply Voltage (Vp) | -0.5V to 7V |
| Voltage Applied to Logic Inputs | -0.5V to Vp+0.5V |
| All other Pins | -0.5V to Vp+0.5V |

### POWER SUPPLY CURRENT AND POWER DISSIPATION

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| ICC (VPn) | Outputs and test point pins open<br>Ta = 27 °C, VP = 5.5 V, 64 Mbit/s<br>PWR = 1 | | | 100 | mA |
| PWR<br>Power Dissipation | Outputs and test point pins open,<br>Ta = 27°C, VP = 5.5 V, 64 Mbit/s<br>PWR = 1 | | | 550 | mW |
| Sleep Mode Power | PWR = 0 | | | 10<br>55 | mA<br>mW |

## DIGITAL INPUTS AND OUTPUTS

### TTL Compatible Inputs

Inputs will float high "1" if left open.

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| Input low voltage | VIL | | -0.3 | | 0.8 | V |
| Input high voltage | VIH | | 2.0 | | VPD+0.3 | V |
| Input low current | IIL | VIL=0.4V | | | -0.4 | mA |
| Input high current | IIH | VIH = 2.4V | | | 100 | µA |

### TTL Compatible Outputs

| | | | | | | |
|---|---|---|---|---|---|---|
| Output low voltage | VOL | IOL = 4.0 mA | | | 0.5 | V |
| Output high voltage | VOH | IOH = -400 µA | 2.4 | | | V |

### PECL Input Levels

(FREF/$\overline{\text{FREF}}$ and RD/$\overline{\text{RD}}$)

| | | | | | | |
|---|---|---|---|---|---|---|
| Input high voltage | VIH | | VIL+0.5 | | VPA-0.5 | V |
| Input low voltage | VIL | | VPA-2.2 | | VIH-0.5 | V |
| Input low current | | VIL = min | -100 | | | µA |
| Input high current | | VIH = max | | | 100 | µA |
| Differential input voltage | | \|RD - $\overline{\text{RD}}$\| or \|FREF - $\overline{\text{FREF}}$\| | 0.5 | | | Vpp |

### PECL output levels

(WD/$\overline{\text{WD}}$)

| | | | | | |
|---|---|---|---|---|---|
| Output high level | 511Ω to AGND, VPA = 5.0V | | | VPD-0.7 | V |
| Output low level | 511Ω to AGND, VPA = 5.0V | VPD-2.1 | | | V |
| Differential output voltage | \|WD - $\overline{\text{WD}}$\| | 1.6 | | 2.4 | Vpp |

### Test point output levels

($\overline{\text{DRD}}$, SD, VCO_REF)

| | | | | | |
|---|---|---|---|---|---|
| Output high level | 261Ω to VPA, 402Ω to AGND<br>VPA = 5.0V | VPA-1.02 | | | V |
| Output low level | 261Ω to VPA, 402Ω to AGND<br>VPA = 5.0V | | | VPA-1.62 | V |

## ELECTRICAL SPECIFICATIONS (continued)

### SERIAL PORT
(Refer to Figure 2)

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| SCLK period | | | 100 | | | ns |
| SCLK low time | TCKL | | 40 | | | ns |
| SCLK high time | TCKH | | 40 | | | ns |
| Enable to SCLK | TSENS | | -25 | | 25 | ns |
| SCLK to disable | TSENH | | -25 | | 25 | ns |
| Data set-up time | TDS | | 25 | | | ns |
| Data hold time | TDH | | 25 | | | ns |

### DATA SEPARATOR CHARACTERISTICS

**Read Mode**

| | | | | | | |
|---|---|---|---|---|---|---|
| Read data pulse width | TPRD | | 6 | | TVCO-6 | ns |
| Read data rise time | TRRD | 20 to 80%, CL ≤ 10 pF | | | 3 | ns |
| Read data fall time | TFRD | 80 to 20%, CL ≤ 10 pF | | | 3 | ns |
| Read clock rise time | TRRC | 0.8 to 2.0V, CL ≤ 15 pF | | | 5 | ns |
| Read clock fall time | TFRC | 2.0 to 0.8V, CL ≤ 15 pF | | | 5 | ns |
| RCLK high time | THRC | 2.0V, CL ≤ 15 pF | 13 | | | ns |
| RCLK low time | TLRC | 0.8V, CL ≤ 15 pF | 13 | | | ns |
| RCLK re-sync time | | | TORC | | 2TORC | ns |
| NRZ out set-up and hold time | TNS, TNH | | 10.0 | | | ns |
| 1/3 cell delay | | TD=0.5*TVCO | 0.9TD | | 1.1TD | ns |

Note: TVCO = 1.64 + (0.163•RR/DACI)
RR = 4.75 kΩ

**Write Mode**

| | | | | | | |
|---|---|---|---|---|---|---|
| Write data rise time | TRWD | 20 to 80%, 110Ω to VPD<br>160Ω to AGND | | | 3 | ns |
| Write data fall time | TFWD | 80 to 20%, 110Ω to VPD<br>160Ω to AGND | | | 3 | ns |
| Write data clock rise time | TRWC | 0.8 to 2.0 V, CL ≤ 15 pF | | | 10 | ns |
| Write data clock fall time | TFWC | 2.0 to 0.8 V, CL ≤ 15 pF | | | 8 | ns |
| NRZ set-up time | TSNRZ | | 5 | | | ns |
| NRZ hold time | THNRZ | | 5 | | | ns |

**Data Synchronization**

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| VCO center frequency period | TVCO | TVCO = 1.64 + (0.163•RR/DACI)<br>RR = 4.75 kΩ, FP = FM = 2.5V | 0.9TVC0 | | 1.1TVC0 | ns |
| VCO dynamic range | | -2.0V ≤ FP-FM ≤ +2.0V | ±28 | | ±45 | % |
| VCO control gain | KVCO | ωi =2π/TVCO<br>-2.0V ≤ FP-FN ≤ +2.0V | 0.12 ωi | | 0.18 ωi | rad/(V-S) |
| Phase detector gain | KD | RD = 3T pattern<br>KD = 0.106•DACI/(6πRR);<br>Non-Read:<br>KD = 0.106•DACI/(4π•RR) | 0.83 KD | | 1.17 KD | A/rad |
| KVCO x KD product accuracy | | | -26 | | +26 | % |
| VCO phase restart error | | | -0.05•TVCO | | +0.05•TVCO | ns |
| Decode window center accuaracy | | | -0.03•TVCO | | +0.03•TVCO | ns |
| Decode window width | | | 0.97•TVCO | | | ns |
| On resistance from FN to Fn | RSON | FSn = 1<br>n = 0, 1, or 2 | | | 20 | Ω |
| Off resistance from FN to Fn | RSON | FSn = 0<br>n = 0, 1, or 2 | 10M | | | Ω |

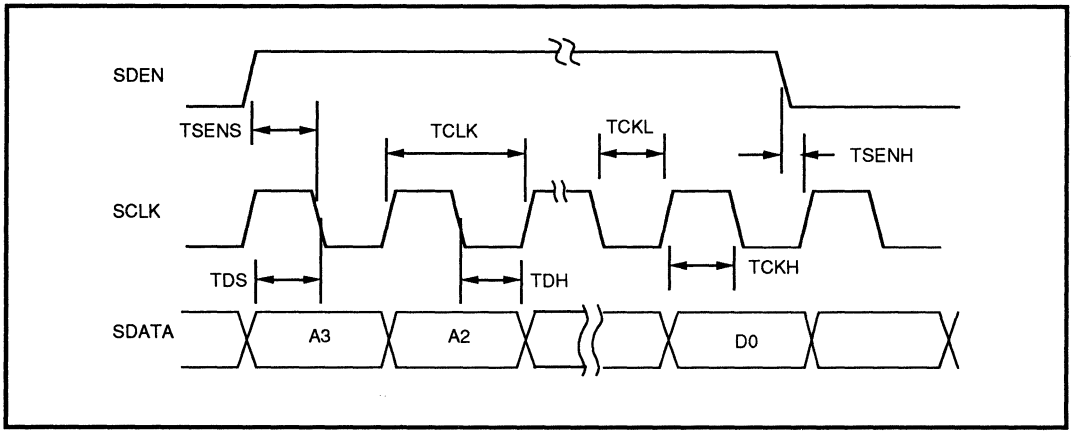



**FIGURE 2: Serial Port Timing**

## ELECTRICAL SPECIFICATIONS (continued)

### WINDOW SHIFT CONTROL

Window shift magnitude is set by the value in the Window Shift (WS) register which is at address 0011. The WS register bits are as follows:

| BIT | NAME | FUNCTION |
|---|---|---|
| 0 | WSO | |
| 1 | WS1 | |
| 2 | WS2 | |
| 3 | WS3 | |

The window shift magnitude is set as a percentage of the decode window, in 2% steps. The tolerance of the window shift magnitude is ±15%. Window shift should be set during idle mode or write mode.

| WS3 | WS2 | WS1 | WS0 | Shift Magnitude |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | No shift |
| 0 | 0 | 0 | 1 | 2% (minimum shift) |
| 0 | 0 | 1 | 0 | 4% |
| 0 | 0 | 1 | 1 | 6% |
| 0 | 1 | 0 | 0 | 8% |
| 0 | 1 | 0 | 1 | 10% |
| 0 | 1 | 1 | 0 | 12% |
| 0 | 1 | 1 | 1 | 14% |
| 1 | 0 | 0 | 0 | 16% |
| 1 | 0 | 0 | 1 | 18% |
| 1 | 0 | 1 | 0 | 20% |
| 1 | 0 | 1 | 1 | 22% |
| 1 | 1 | 0 | 0 | 24% |
| 1 | 1 | 0 | 1 | 26% |
| 1 | 1 | 1 | 0 | 28% |
| 1 | 1 | 1 | 1 | 30% (maximum shift) |

The window shift direction is set by bit 3 (WSD) in the WP register at address 0010. A "1" sets a positive shift, a "0" sets a negative shift. For normal operation, the "BYP" bit in the serial port should be set to "0." This allows the window shift circuit to detect the No shift condition and bypass the window shift circuit. This will tend to minimize window loss and shift in the normal operating mode. When "BYP" is set to "1," the window shift circuit does not detect the no shift condition and uses the window shift circuitry. This is useful when testing the device.

### WRITE PRECOMP CONTROL

Write precomp magnitude is set by the value in the Write Precomp (WP) register at address 0010. The WP register bits are as follows:

| BIT | NAME | FUNCTION |
|---|---|---|
| 0 | WO | |
| 1 | W1 | |
| 2 | W2 | |
| 3 | TM | Test Mode |

The write precomp magnitude is calculated as:

$$TPC = n \times 0.04 \times TREF$$

where n = precomp magnitude scaling factor as shown below. TREF is the period of the reference frequency of the input signal provided at FREF/FREF.

| W2 | W1 | W0 | Precomp Magnitude Scaling Factor |
|---|---|---|---|
| 0 | 0 | 0 | No precomp |
| 0 | 0 | 1 | 1X |
| 0 | 1 | 0 | 2X |
| 0 | 1 | 1 | 3X |
| 1 | 0 | 0 | 4X |
| 1 | 0 | 1 | 5X |
| 1 | 1 | 0 | 6X |
| 1 | 1 | 1 | 7X (maximum) |

| BIT N-2 | BIT N-1 | BIT N | BIT N+1 | BIT N+2 | BIT N COMPENSATION |
|---|---|---|---|---|---|
| 1 | 0 | 1 | 0 | 1 | None |
| 0 | 0 | 1 | 0 | 0 | None |
| 1 | 0 | 1 | 0 | 0 | Early |
| 0 | 0 | 1 | 0 | 1 | Late |

Late = Bit N is time shifted toward the N+1 bit by the programmed magnitude
Early = Bit N is time shifted toward the N-1 bit by the programmed magnitude

When the "BYP" bit in the serial port is set to "1," the precompensation circuitry is bypassed. For the precompensation circuit to function the "BYP" bit must be set to "0."

TABLE 2: 1,7 RLL Encode

| NRZ DATA | | | | ENCODED WRITE DATA | | | |
|---|---|---|---|---|---|---|---|
| PRESENT BITS | | NEXT BITS | | CODE BITS | | | |
| 0 | 0 | 0 | | | 0 | 0 | 1 |
| 0 | 0 | 1 | | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | | 1 | 0 | 1 | 0 |
| 1 | 0 | 0 | | | 1 | 0 | 1 |
| 1 | 0 | 1 | | | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 |

TABLE 3: 1,7 RLL Decode

| ENCODED READ DATA | | | | | | | DECODED DATA | |
|---|---|---|---|---|---|---|---|---|
| Previous | | Present | | | Next | | | |
| Y 2' | Y 3' | Y 1 | Y 2 | Y 3 | Y 1 | Y 2 | D 1 | D 2 |
| 0 | 0 | 0 | 0 | 0 | | | 0 | 1 |
| 1 | 0 | 0 | 0 | 0 | | | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | | | 0 | 1 |
| | | 1 | 0 | 0 | | | 1 | 1 |
| | 0 | 1 | 0 | 0 | 0 | 1 | 1 | |
| | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 |
| | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 0 | 0 | 0 | 0 | 1 | | | 0 | 1 |
| 1 | 0 | 0 | 0 | 1 | | | 0 | 0 |
| 0 | 1 | 0 | 0 | 1 | | | 0 | 0 |
| | | 1 | 0 | 1 | | | 1 | 0 |

**TABLE 4: Clock Source and Frequency vs. Mode**

| $\overline{WG}$ | RG | VCO REF | RCLK | DECODE CLOCK | ENCODE CLOCK | MODE |
|---|---|---|---|---|---|---|
| 1 | 0 | FREF | 2FREF/3 | FREF | FREF | IDLE |
| 1 | 1 | $\overline{DRD}$ | 2VCO/3 | VCO | FREF | READ |
| 0 | 0 | FREF | 2FREF/3 | FREF | FREF | WRITE |

NOTE 1: Until the VCO locks to the new source, the VCO entries will be FOUT.
NOTE 2: Until the VCO locks to the new source, the 2VCO/3 entries will be FOUT/3.
NOTE 3: $\overline{WG}$ =0; RG = 1 is an indeterminate state.
NOTE 4: FREF = External reference applied to FREF/$\overline{FREF}$.

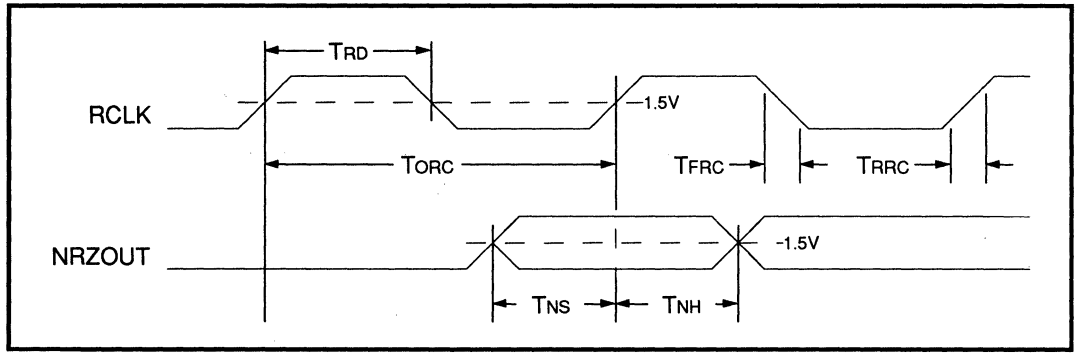



**FIGURE 3: NRZ Read Timing**

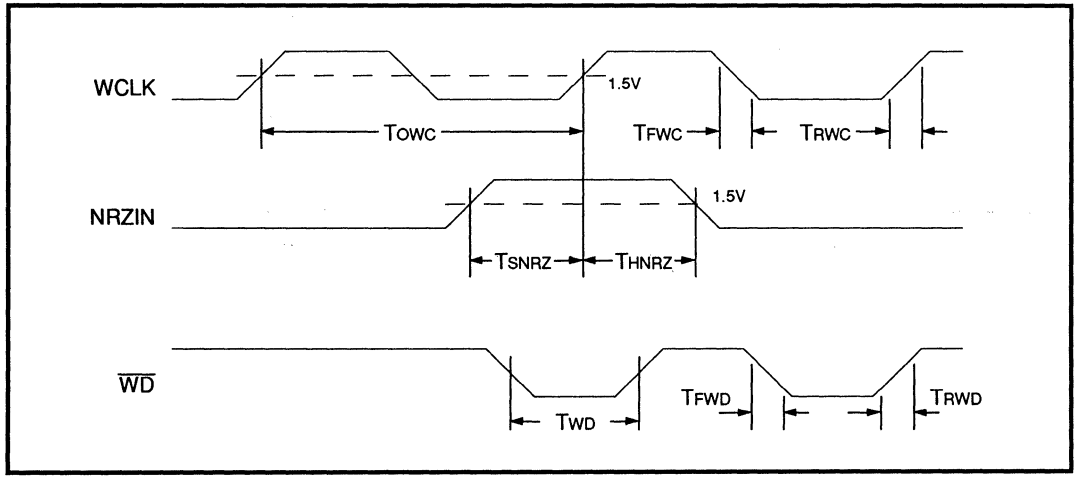



**FIGURE 4: $\overline{WD}$ and NRZ Write Timing**

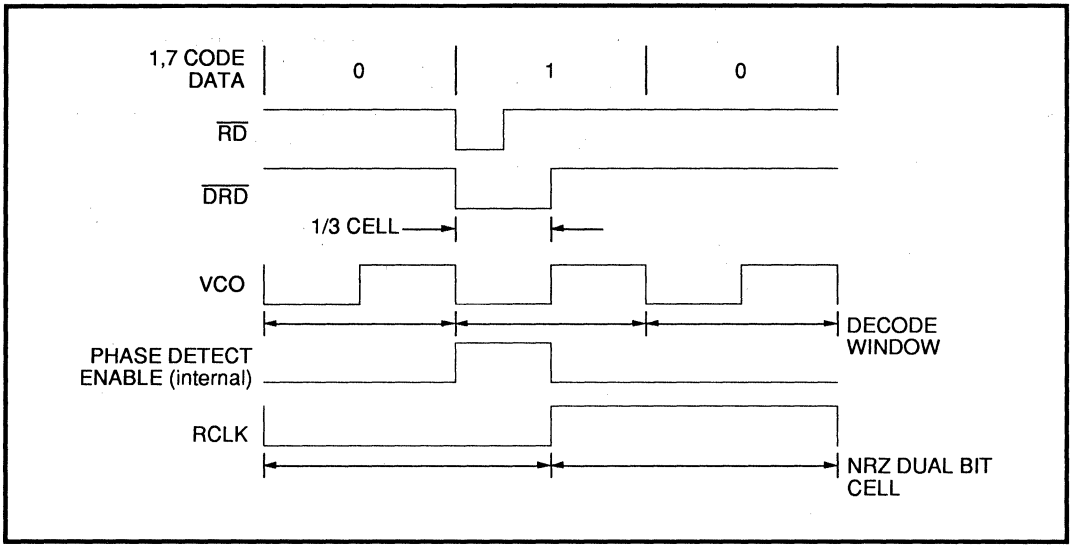



**FIGURE 5: Data Synchronization Waveform**

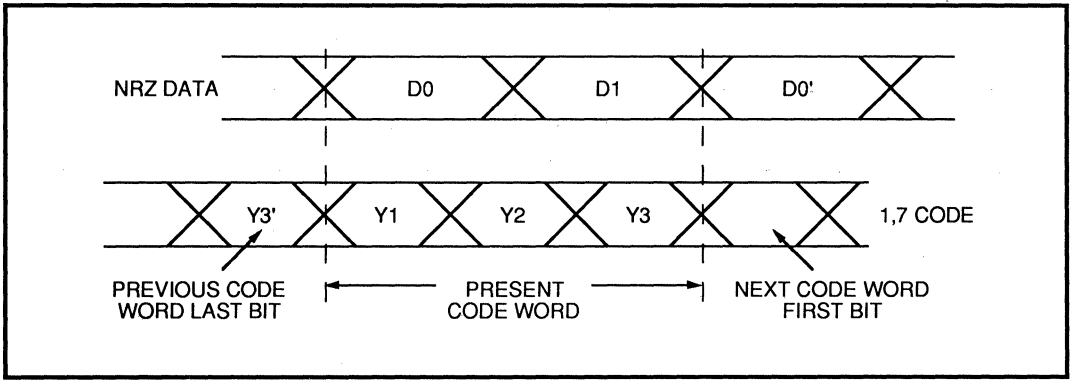



**FIGURE 6: NRZ Data Word to 1,7 Code Word Bit Comparison**
(Reference Tables 2 & 3 for encode/decode scheme)

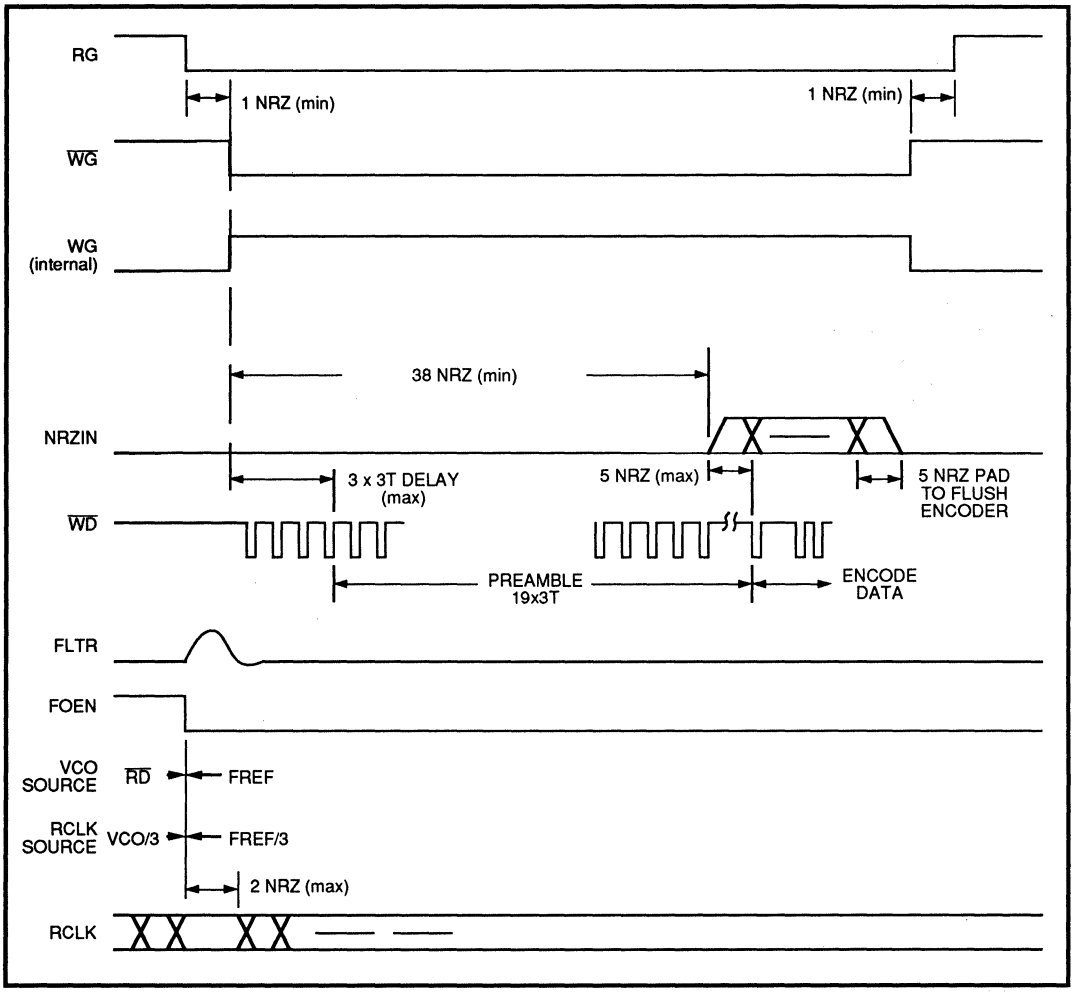



**FIGURE 7: Write Data Operation**

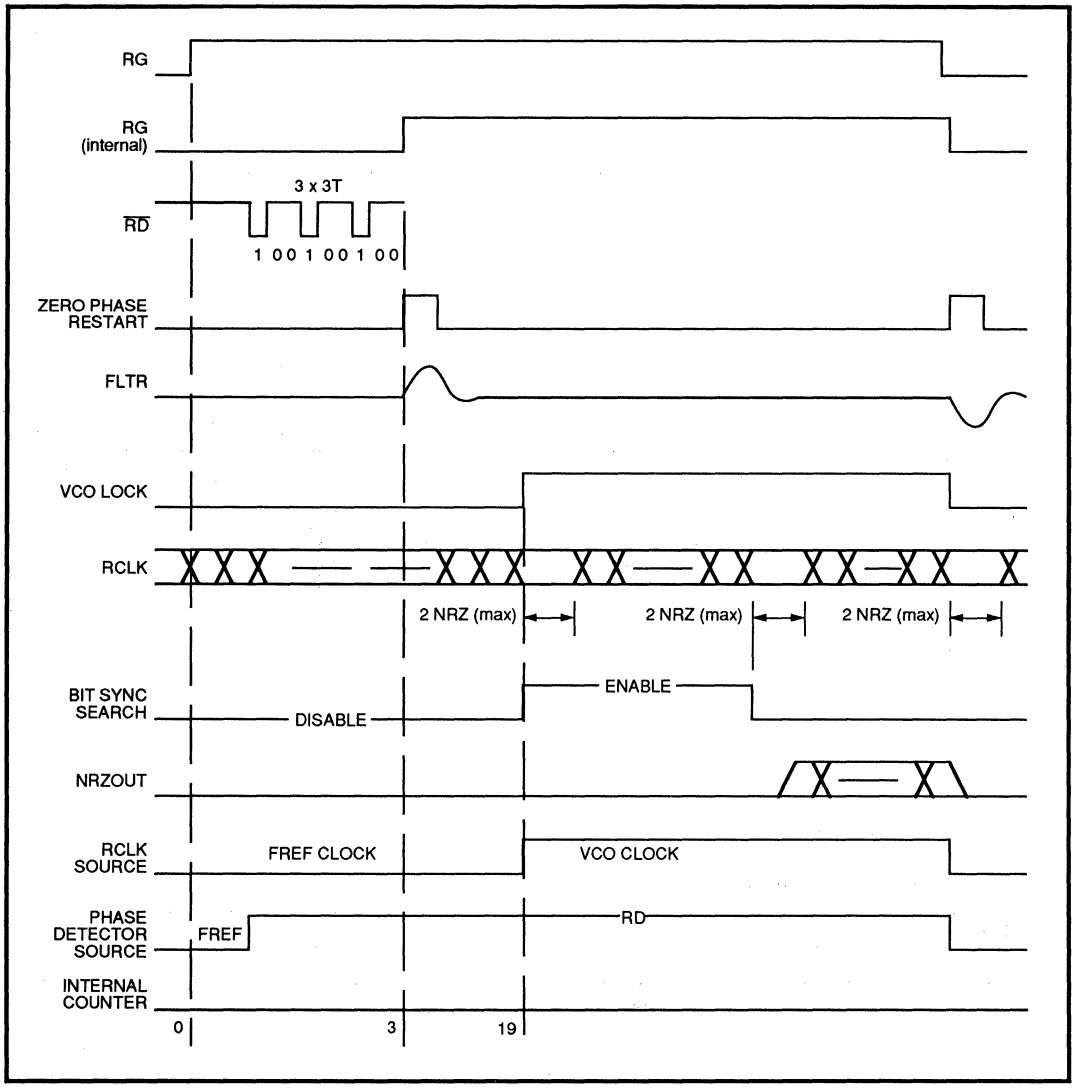



**FIGURE 8: Read Mode Locking Sequence**

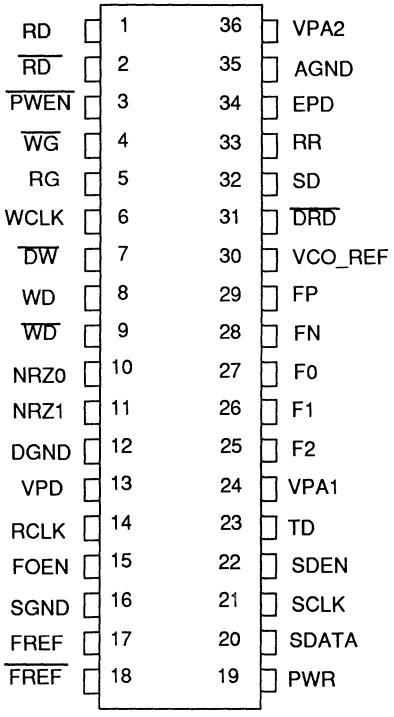
## PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.

**THERMAL CHARACTERISTICS: θja**

| | |
|---|---|
| 36-Lead SOM | 75°C/W |

4




**36-Lead SOM**

**Advance Information:** Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.



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**Notes:**

silicon systems®
A TDK Group Company

# SSI 32D4661/4662
## Time Base Generator

December 1992

4

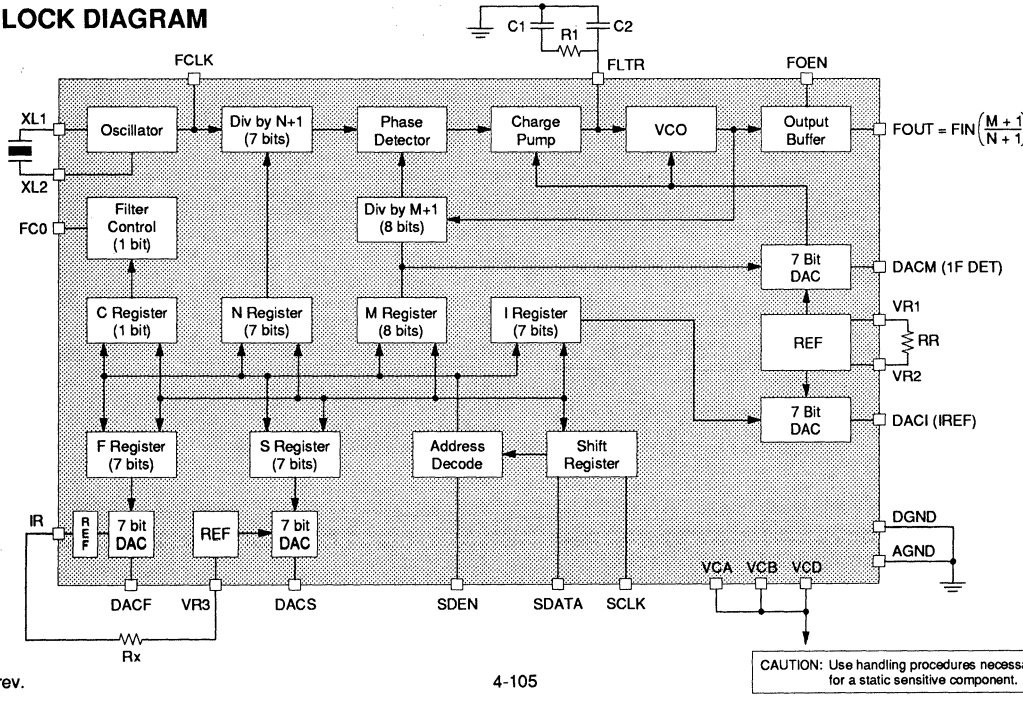
## DESCRIPTION

The SSI 32D4661/4662 Time Base Generator provides a programmable reference generator, channel filter control and data rate control for constant density recording applications. It is optimized to operate with the 32D53xx series data separators and contains a high performance programmable PLL for 1% reference frequency control. A 7–bit DAC, DACI is provided to program the IREF current which sets the data separator PLL operating center frequency. A 7–bit DAC, DACM is provided to program the 1FDET current which sets the timing for the data separator synch field detect. Two additional 7–bit DACs are provided for programmable electronic filter (slimmer) control. DACS controls the boost while DACF controls the cutoff frequency of the electronic filter. A latched TTL output is provided to control filter multiplexer. A serial microprocessor interface reduces pin count and provides convenient access to the internal program storage registers. The 32D4661/4662 only requires a +5V supply and is available in 24-lead SO packages.

## FEATURES

- **Not plug compatible with SSI 32D4660**
- **For constant density recording applications**
- **Reference frequency control**
- **Channel filter control**
- **Internal DAC available to program data separator data rate**
- **Internal DAC available to program data separator sync field detect timing**
- **Up to 72 MHz operation for the 32D4661**
- **Up to 108 MHz operation for the 32D4662**
- **1% frequency resolution**
- **No external active components required**
- **+5V only operation**
- **Low power mode**
- **24-lead SOL/VSOP package**

## BLOCK DIAGRAM




CAUTION: Use handling procedures necessary for a static sensitive component.

## PIN DESCRIPTION

### INPUT PINS

| NAME | DESCRIPTION |
|---|---|
| SDATA | Serial Data. Data input for an 8-bit control shift register. The data packet is transmitted MSB (D7) first. The first four bits are the register address and the last four are its data bits. Registers larger than 4-bits must be loaded with two 8-bit data packets. These packets should be loaded sequentially in less than 10 µs since the loading operation will cause output transients. With proper loop filter design, the output transients will recover within 1 ms. The data packet fields are given in Table 1. |
| SCLK | Serial Data Clock. Negative edge triggered clock input for the serial data. |
| SDEN | Serial Data Enable. A high level input enables data loading. The data is latched when the input is low. |
| FOEN | Frequency Output Enable. A high level input enables the FOUT output. A low level disables the output and minimizes the driven data separator jitter. |

### OUTPUT PINS

| | |
|---|---|
| FOUT | Frequency Output. An ECL output with internal current source. The low voltage swing which minimizes data separator jitter must be AC coupled to the data separator XTL1 input. FOUT = [(M +1)/(N +1)]FIN where M = M Register number and N must be set to approximately 32D4661: [(FIN) (256) / 72 MHz] - 1; 32D4662: [(FIN) (256) / 108 MHz] - 1 |
| DACM | DAC Output. 7-bit DAC current sink output used to program timing current to the data separator sync field detect SDS pin. The current magnitude is controlled by the 7 MSB's of the M Register and is compensated to minimize the sensitivity to power supply and temperature variations. If this output isn't required, the pin must be connected to VCC. |
| DACI | DAC Output. 7-bit DAC current source output used to program timing current for the data separator VCO center frequency. The current magnitude is controlled by the I Register and is compensated to minimize the sensitivity to power supply and temperature variations. |
| DACF | DAC Output. 7-bit DAC current output used for electronic filter control. The output current is set by the voltage at VR3, and the F Register number and an external resistor Rx. |
| DACS | DAC Output. 7-bit DAC voltage output used for electronic filter control. The output voltage is set by the voltage at VR3 and the S Register number. |
| FC0 | Filter Control 0. TTL output used to control an external filter multiplexer. C0 = H sets FC0 = H. |

**OUTPUT PINS** (Continued)

| NAME | DESCRIPTION |
|---|---|
| FCLK | Clock Output. Optional TTL output that may be used for a system clock. The output frequency is the same as the oscillator output frequency. For minimum FOUT jitter, this pin should be a no connect. |

**ANALOG PINS**

| | |
|---|---|
| XTL1, XTL2 | Crystal Oscillator Connections. The circuit is designed to be used with an 8 MHz to 20 MHz crystal. If a crystal is not desired, XTL1 may be driven by a TTL source with XTL2 left open. |
| VR1, VR2 | Current Setting Resistor Connections. An external resistor RR connected between VR1 and VR2 sets the DACM and DACI currents. |
| VR3 | Reference Voltage Input. An external 2.2V supply sets the reference for the DACS voltage. |
| IR | Reference Current Input. An external resistor Rx, connected from IR to VR3 reference voltage sets the reference current for the DACF current. |
| FLTR | PLL Loop Filter Connection. Connection for loop filter components R1, C1 and C2. |
| DGND, AGND | Digital and Analog Ground |
| VCA, VCB | Analog +5V Supplies |
| VCD | Digital +5V Supply |

**TABLE 1: Data Packet Fields**

| ADDRESS BITS | | | | USAGE | DATA BITS | | | |
|---|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | | D3 | D2 | D1 | D0 |
| 0 | 1 | 1 | 0 | I REGISTER | X | I6 | I5 | I4 |
| 0 | 1 | 1 | 1 | I REGISTER | I3 | I2 | I1 | I0 |
| 1 | 0 | 0 | 0 | S REGISTER | X | S6 | S5 | S4 |
| 1 | 0 | 0 | 1 | S REGISTER | S3 | S2 | S1 | S0 |
| 1 | 0 | 1 | 0 | F, C REGISTER | C0 | F6 | F5 | F4 |
| 1 | 0 | 1 | 1 | F REGISTER | F3 | F2 | F1 | F0 |
| 1 | 1 | 0 | 0 | M REGISTER | M7 | M6 | M5 | M4 |
| 1 | 1 | 0 | 1 | M REGISTER | M3 | M2 | M1 | M0 |
| 1 | 1 | 1 | 0 | N REGISTER | X | N6 | N5 | N4 |
| 1 | 1 | 1 | 1 | N REGISTER | N3 | N2 | N1 | N0 |

X = Don't care bit.

## ELECTRICAL SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may damage the device.

| PARAMETER | RATING |
|---|---|
| Storage Temperature | –65 to +150°C |
| Junction Operating Temperature, Tj | +150°C |
| Supply Voltage, VCA, VCB, VCD | –0.5 to 7V |
| Voltage Applied to Logic Inputs | –0.5 to 5.5V |
| Maximum Power Dissipation | 540 mW |

### RECOMMENDED OPERATING CONDITIONS

| PARAMETER | RATING | UNITS |
|---|---|---|
| Supply voltage, VCA = VCB = VCD | 4.65 to 5.35 | V |
| Junction Temperature, Tj | 0<Tj<135 | °C |
| Ambient Temperature, Ta | 0<Ta<70 | °C |

### ELECTRICAL CHARACTERISTICS

Unless Otherwise Specified: Recommended operating conditions apply

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| VIH | High Level Input Voltage | | 2.0 | | | V |
| VIL | Low Level Input Voltage | | | | 0.8 | V |
| IIH | High Level Input Current | VIH = 2.7V | | | 20 | µA |
| IIL | Low Level Input Current | VIL = 0.4V | | | -1.5 | mA |
| VOH | High Level Output Voltage | IOH = -400 µA | 2.4 | | | V |
| VOL | Low Level Output Voltage | IOL = 2 mA | | | 0.5 | V |
| VOH | FOUT ECL High Level | VCD = 5V, VOH-VCD | -1.02 | | | V |
| VOL | FOUT ECL Low Level | VCD = 5V, VOL-VCD | | | -1.45 | V |
| ICC | Power Supply Current | | | 77 | 103 | mA |
| IO | FOUT Output Current | | | ±4 | | mA |
| VO | FOUT Output Swing | | 0.6 | | | V |

**INPUT/OUTPUT CHARACTERISTICS**

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|---|
| FIN | FIN Frequency | | 8 | | 20 | MHz |
| FO | FOUT Frequency | 32D4661 | | | 72 | MHz |
| | | 32D4662 | | | 108 | MHz |
| JFO | FOUT Jitter | TO = 1/FO; FCLK active | | | ±400 | ps(pk) |
| DFO | FOUT Duty Cycle | 50% Amplitude<br>32D4661: FOUT = 72 MHz<br>32D4662: FOUT = 108 MHz | 42 | | 58 | % |
| F | F Register Number | | 0 | | 127 | - |
| S | S Register Number | | 0 | | 127 | - |
| M | M Divide Number | | 80 | | 255 | - |
| N | N Divide Number | 32D4661 | 25 | | 127 | - |
| | | 32D4662 | 18 | | 127 | - |
| I | I Register Number | | 30 | | 127 | - |
| RR | External Resistor | | 4.50 | | 5.25 | kΩ |
| TVCO | VCO Center Frequency Period | 32D4661: TO=(6.17)(RR/M)+2.4 ns<br>32D4662: TO=(4.08)(RR/M)+2.4 ns<br>VCC = 5V, RR = 4.75 kΩ<br>FLTR = 2.7V<br>M = 100 | 0.77TO | TVCO | 1.23TO | ns |
| | VCO Frequency Dynamic Range | 1V < FLTR < VCC – 0.5V,<br>VCC = 5V, M = 100 | ±25 | | ±45 | % |
| KVCO | VCO Control Gain | ωi = 2π/TVCO | 0.14ωi | | 0.26ωi | rad/s V |
| KD | Phase Detector | KD = (4.39E-3)M/RR | | KD | | A/rad |
| IOM | DACM Current | IO = (1.641E-2)M/RR<br>VCC = 5V, TA = 25°C,<br>RR = 4.75kΩ | 0.95IO<br>–1LSB | | 1.05IO<br>+1LSB | A |
| IOI | DACI Current | IO = (7.57E-2)I/RR<br>VCC = 5V, TA = 25°C,<br>RR = 4.75kΩ | 0.97IO<br>–3/4LSB | | 1.05IO<br>+3/4LSB | A |
| IOF | DACF Current | IOF = 0.98 F*4/127 • IR<br>VCC = 5V, Rx = 2.74 kΩ<br>Where IR = VR3/(4*Rx) or an external current source | 0.97IOF<br>–3/4LSB | | 1.03IOF<br>+3/4LSB | V |
| VOS | DACS Voltage | VOS = 0.98 S*VR3/127<br>VCC = 5V | 0.97VOS<br>–3/4LSB<br>+15 mV | | 1.03VOS<br>+3/4LSB<br>+60 mV | V |
| VR3 | DAC Reference | | 2.0 | | 2.4 | V |
| IVR3 | VR3 Input Current | VR3 = 2.2V | | | 1.0 | mA |

**INPUT/OUTPUT CHARACTERISTICS** (Continued)

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|---|
| Rx | | | 2.5 | | 3.0 | kΩ |
| I, M | DAC Current Tolerance | RR = 4.75 kΩ<br>0°C < Ta < 70°C<br>4.65V < Vcc < 5.35V | 0.75 IO | | 1.25 IO | A |
| I, F, M, S | Differential Linearity (Monotonicity) | 0°C<Ta<70°C<br>4.65V < Vcc < 5.35V | -1LSB | | | - |
| VODH | DACM Output Voltage | | 2.5 | | VCC | V |
| VODL | DACI Output Voltage | | | | 2 | V |
| VOFL | DACF, DACS Output Voltage | | 0.1 | | 2.4 | V |
| ROUT | DACF, DACS Output Resistance | | | | 3.7 | kΩ |
| SCLK | Data Clock Period, TC | | 100 | | | ns |
| TDD | Data Set Up/Hold Time WRT to SCLK Falls | | 25 | | | ns |
| SDEN | Rises Setup to SCLK Falls | | 0 | | | ns |
| | High Holds from SCLK Falls | | 0 | | | ns |
| | Falls Setup to SCLK Rises | | 25 | | | ns |

## APPLICATIONS INFORMATION

The serial port allows the user to program the internal registers of the 32D4661/4662 device. This port has been designed to operate with the serial port on most microcontrollers such as the 8051. Silicon Systems also provides a serial port board that can be used to operate the serial interface. The serial port consists of three lines: enable (SDEN or SERMODE), data (SDATA), and clock (SCLK). During a serial data transfer, eight bits of data should be transferred to the selected device. The first four bits of data contain register address information while the last four bits contain the programming data. The timing considerations for the serial port are fairly straight forward (see Figure 1). The enable line is driven high to initiate the data transfer. While the enable line is high, the transmitting device should output eight clock pulses along with eight bits of synchronous programming data, four address bits followed by four data bits. The data is shifted internally on the falling edge of the clock pulses. To prevent false data from being latched in, only eight (8) clock pulses should be provided while the enable line is active. The falling edge of the enable input will latch the data into the internal registers and initiate the selected function.

Note: it takes two transfers to load a single register.

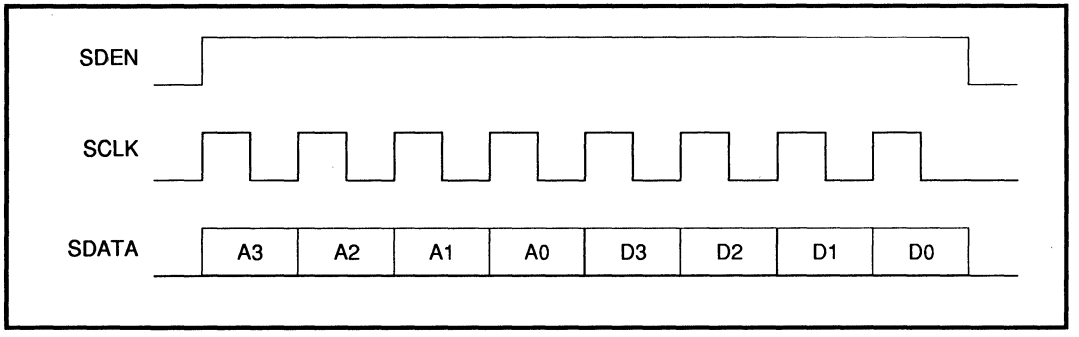



**FIGURE 1: Serial Port Timing**

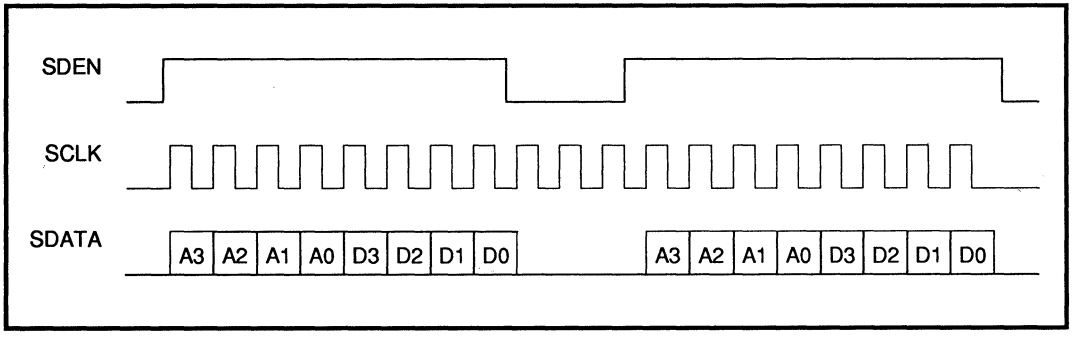



**FIGURE 2: Serial Port Timing, Multiple Transfers**

## APPLICATIONS INFORMATION (continued)

### REFERENCE FREQUENCY OUTPUT:

The 32D4661/4662 provides the reference frequency for the phase-locked loop (PLL) of a data separator. The required frequency is programmed using the **M** and **N** registers of the 4661/4662.

**32D4661:**
The value of the **N** register is determined by the oscillator that drives the 32D4661 according to the following equation:

$$N=\frac{(Fin \bullet 256)}{(72\ MHz)}-1$$

For this application, using a 12 MHz oscillator (Fin) would yield an **N** integer value of 42. Although the value of **N** should be fixed according to the equation shown above, there is a tolerance of ± 1 integer so **N** can be set from 41 to 43. (This is necessary as the phase detector frequency is fixed by Fin & **N**) Substituting **N** into the following equation and knowing the reference frequency required for each data rate allows for the determination of the **M** register value:

$$Fout=\frac{(M+1)}{(N+1)} \bullet Fin$$

Since **M** must be an integer value, it may be necessary to change **N** values for each data rate to obtain the required output frequency. For example (for 3x reference clock), at 12 Mbit/s the required reference frequency is 36 MHz and using a value of **N** = 41, yields an **M** value of 125. At 13 Mbit/s using the **N** value of 41 would require an **M** value of 135.5 to produce an output frequency of 39 MHz. Using **M** = 135 would give an output frequency of 38.86 MHz while using an **M** value of 136 the output frequency would be 39.14 MHz. If **N** is changed to 43 then a value of 143 for **M** would produce the required output frequency of 39 MHz. The required **M** and **N** values for some sample data rates are provided in the table that follows.

**TABLE 1: M and N Register Programming Example**

| DR (Mbit/s) | Fout | M | N |
|---|---|---|---|
| 12 Mb/s | 36 MHz | 125 | 41 |
| 13 Mb/s | 39 MHz | 142 | 43 |
| 14 Mb/s | 42 MHz | 146 | 41 |
| 15 Mb/s | 45 MHz | 164 | 43 |

The **N** register is at address "1110" for the MSBs and address "1111" for the LSBs. The table that follows gives the required register programming information for the values of **N**.

**TABLE 2: Frequency Programming Information, N Register**

| ADDRESS BITS | | | | DATA BITS | | | | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 1 | 1 | 1 | 0 | X | 0 | 1 | 0 | N Register MSBs for N = 41 |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | N Register LSBs for N = 41 |
| 1 | 1 | 1 | 0 | X | 0 | 1 | 0 | N Register MSBs for N = 43 |
| 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | N Resgister LSBs for N = 43 |

## APPLICATIONS INFORMATION (continued)

The **M** register is at address "1100" for the MSB's and at address "1101" for the LSB's. The table that follows gives the required register programming information for the values of **M** based on the equation given above for Fout.

**TABLE 3: Frequency Programming Information, M Register**

| ADDRESS BITS | | | | DATA BITS | | | | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | M Register = 125, |
| 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | Fout = 36 MHz |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | M Register = 142, |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | Fout = 39 MHz |
| 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | M Register = 146, |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | Fout = 42 MHz |
| 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | M Register = 164, |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | Fout = 45 MHz |

**32D4662:**
The value of the **N** register is determined by the oscillator that drives the 32D4662 according to the following equation:

$$N=\frac{(Fin \cdot 256)}{(108\ MHz)}-1$$

For this application, using a 20 MHz oscillator (Fin) would yield an **N** value of 46.4. Although the value of **N** should be fixed according to the equation shown above, there is a tolerance of ± 1 integer so **N** can be set from 45 to 47. (This is necessary as the phase detector frequency is fixed by Fin & **N**) Substituting **N** into the following equation and knowing the reference frequency required for each data rate allows for the determination of the **M** register value:

$$Fout=\frac{(M+1)}{(N+1)} \cdot Fin$$

Since **M** must be an integer value, it may be necessary to change **N** values for each data rate to obtain the required output frequency. For example (for 3x reference clock), at 26 Mbit/s the required reference frequency is 78 MHz and using a value of **N** = 47, yields an **M** value of 186. At 28 Mbit/s using the **N** value of 49 would require an **M** value of 209 to produce an output frequency of 84MHz. **M** and **N** values for some sample data rates are provided in the table that follows. Note: the values for Fout are approximate.

**TABLE 4: M and N Register Programming Example**

| DR (Mbit/s) | Fout | M | N |
|---|---|---|---|
| 26 Mb/s | 78 MHz | 186 | 47 |
| 28 Mb/s | 84 MHz | 192 | 45 |
| 30 Mb/s | 90 MHz | 206 | 45 |
| 32 Mb/s | 96 MHz | 220 | 45 |

## APPLICATIONS INFORMATION (continued)

### REFERENCE FREQUENCY OUTPUT (32D4662) (continued):

The **N** register is at address "1110" for the MSBs and address "1111" for the LSBs. The table that follows gives the required register programming information for the values of **N**.

**TABLE 5: Frequency Programming Information, N Register**

| ADDRESS BITS | | | | DATA BITS | | | | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 1 | 1 | 1 | 0 | X | 0 | 1 | 0 | N Register MSBs for N = 47 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | N Register LSBs for N = 47 |

The **M** register is at address "1100" for the MSBs and at address "1101" for the LSBs. The table that follows gives the required register programming information for the values of **M** based on the equation given above for Fout.

**TABLE 6: Frequency Programming Information, M Register**

| ADDRESS BITS | | | | DATA BITS | | | | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | M Register = 186, |
| 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | Fout = 78 MHz |
| 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | M Register = 192, |
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | Fout = 84 MHz |
| 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | M Register = 206, |
| 1 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | Fout = 90 MHz |
| 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | M Register = 220, |
| 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | Fout = 96 MHz |

### LOOP FILTER FOR THE 32D4661/32D4662:

The 32D4661/4662 requires a loop filter to control the PLL locking characteristics. While there are several types of filters that can be used to perform this function, a simple integrating filter has proven to be very effective (see Figure 3). To select the components for the loop filter, two considerations should be made. First, the acquisition time of the loop must be less than the minimum track-to-track seek time and second, the capacitor C1 should be low leakage (C1 < 1.0 μF). The acquisition time of the loop is set-up to accommodate a zero phase restart and allow for 1% maximum phase error after phase acquisition. This yields a settling time of: $t_s = 5/\omega_n$ .

**32D4661:**

Suppose FREF = 12 MHz, FOUT = 72 MHz, M = 251

KVCO = (0.21)(2π)($F_{out}$) rad/s V (typ.), at 72 MHz  KVCO' = KVCO/(M+1) = $\underline{3.8 \times 10^5}$

KD = (4.39 E-3) M/RR A/rad  @ RR = 4.75 KΩ, $\underline{KD = 2.32 \times 10^{-4}}$

For a second order system,

R1 = (2 x ζ x $\omega_n$)/(KVCO' x KD) where ζ is the damping factor.

C1 = (KVCO' x KD)/($\omega_n^2$) and C1/10 > C2 > C1/20

A damping factor of 0.7 to 1.0 is suggested to prevent locking to harmonics while maintaining an acceptable lock time. At the maximum frequency selected, the damping factor of 1.0 should be considered thereby allowing the damping factor to drop as the frequency drops.

If we start with $\omega_n$ = 2 x $10^4$, C1 can be calculated as 0.21 µF and C2 can be calculated as 0.01 to 0.02 µF. As mentioned above, the damping factor at the maximum frequency of 72 MHz should be 1.0, so R1 is calculated as:

R1 = (2 x 1.0 x 2E4 )/(3.8E5 x 2.32E-4) = 454 Ω

These values will produce a loop settling time $t_s$ of 5/2 x $10^4$ = 250 µs.

The values calculated here are sample values that have been used in the lab and should be considered starting values. The values of R1, C1, and C2 can be further optimized to meet specific needs.

**32D4662:**

Suppose FREF = 12 MHz, FOUT = 100 MHz, M = 232

KVCO = (0.21)(2π)($F_{out}$) rad/s V (typ.), at 100 MHz KVCO' = 5-7 x $10^5$

KD = (4.39 E-3)M/RR A/rad @ RR = 4.75 KΩ, KD = 2.14 x $10^{-4}$

For a second order system,

R1 = (2 x ζ x $\omega_n$)/(KVCO' x KD) where ζ is the damping factor.

C1 = (KVCO' x KD)/($\omega_n^2$ ) and C1/10 > C2 > C1/20

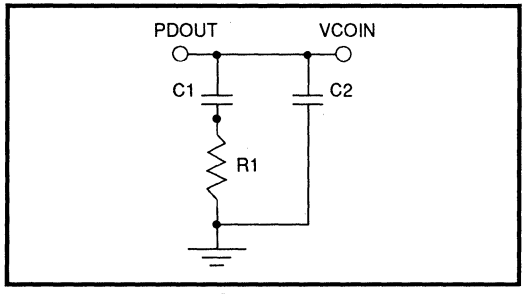
A damping factor of 0.7 to 1.0 is suggested to prevent locking to harmonics while maintaining an acceptable lock time. At the maximum frequency selected, the damping factor of 1.0 should be considered thereby allowing the damping factor to drop as the frequency drops.

If we start with $\omega_n$ = 2 x $10^4$, C1 can be calculated as 0.21 µF and C2 can be calculated as 0.01 to 0.02 µF. As mentioned above, the damping factor at the maximum frequency of 100 MHz should be 1.0, so R1 is calculated as:

R1 = (2 x 1.0 x 2E4 )/(5.7E5 x 2.14E-4) = 328Ω

These values will produce a loop settling time $t_s$ of 5/2 x $10^4$ = 250 µs.

The values calculated here are sample values that have been used in the lab and should be considered starting values. The values of R1, C1, and C2 can be further optimized to meet specific needs.




2 Single Rate

**FIGURE 3: Integrating Filter for the Phase Locked Loop**

NOTE: For further information on the loop filter, consult the Data Synchronizer Family Application Notes in Section 4 of the Silicon Systems Storage Products data book.

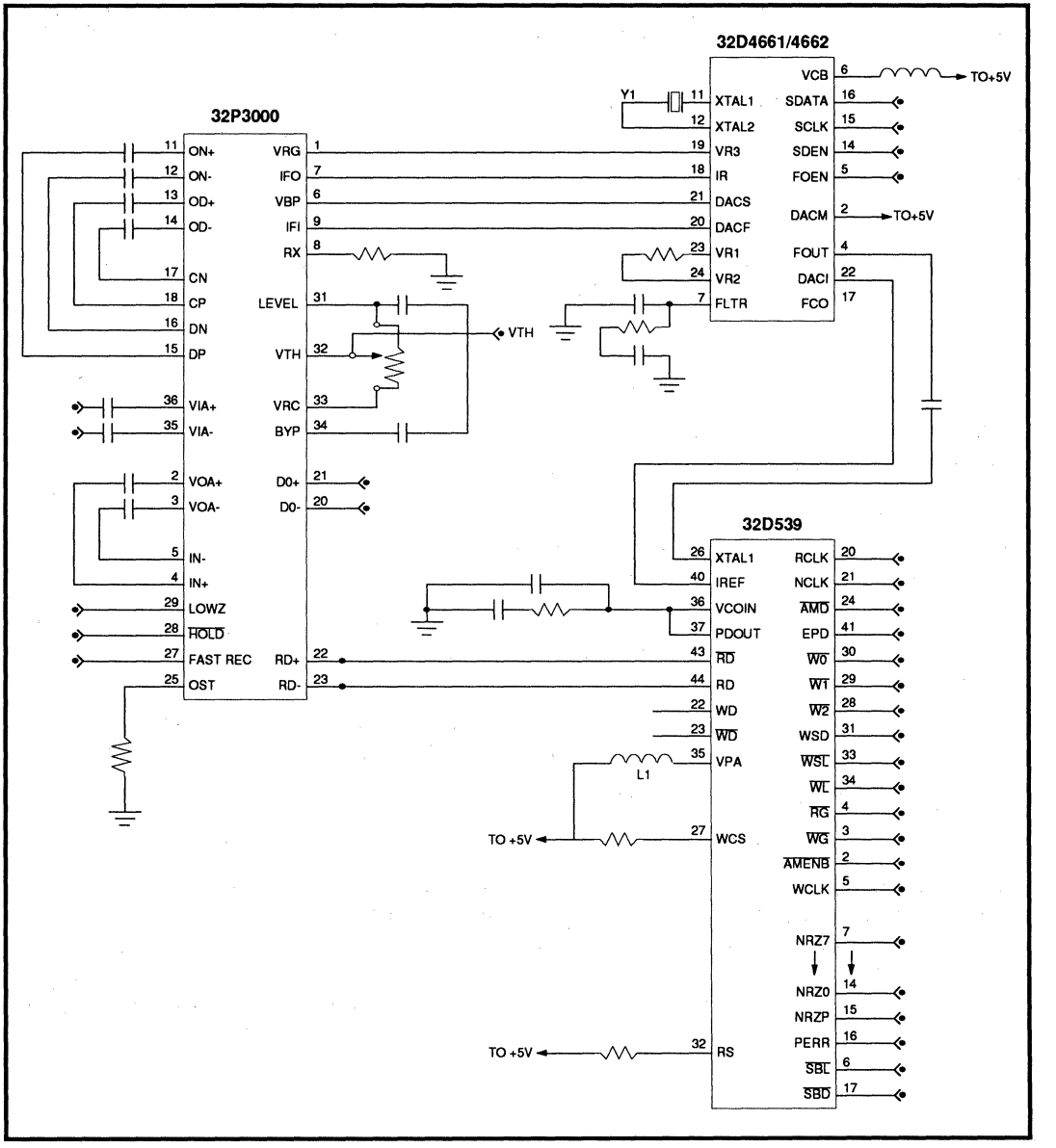
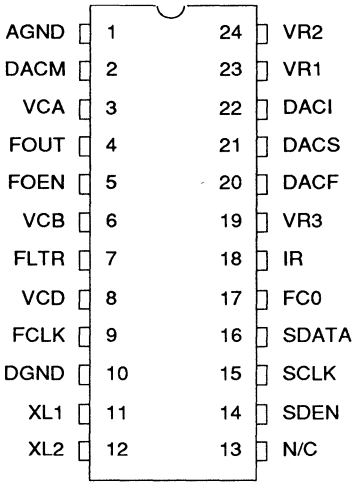



**FIGURE 4: Typical 32D4661/4662 Application**

## PIN DIAGRAM
(Top View)




**24 Lead SOL/VSOP**

## ORDERING INFORMATION

| PART DESCRIPTION | ORDERING NUMBER | PACKAGE MARK |
|---|---|---|
| SSI 32D4661 Time Base Generator | | |
| 24-Lead SOL | 32D4661-CL | 32D4661-CL |
| 24-Lead VSOP | 32D4661-CV | 32D4661-CV |
| SSI 32D4662 Time Base Generator | | |
| 24-Lead SOL | 32D4662-CL | 32D4662-CL |
| 24-Lead VSOP | 32D4662-CV | 32D4662-CV |



Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 573-6000, FAX (714) 573-6914

**Notes:**

silicon systems®
A TDK Group Company

# SSI 32D4664
## Time Base Generator

**Advance Information**

January 1993

4

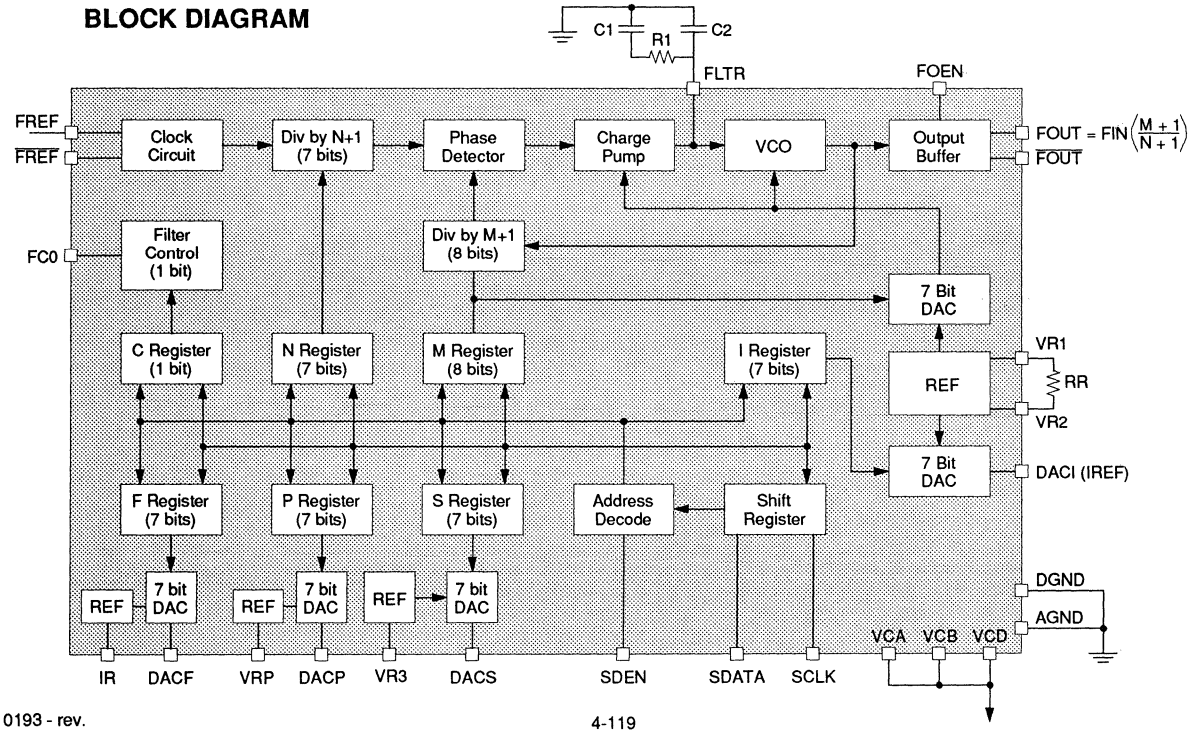
## DESCRIPTION

The SSI 32P4664 is a high performance bipolar device that provides a programmable frequency reference and four internal control DACs to support hard disk drive applications that use zoned recording techniques. It is optimized for use with the 32P3000 family of pulse detector/filter devices and the 32P53X family of data separators. The frequency reference can be programmed up to 72 MHz with better than 1% resolution. The 7-bit DACs provide control of the 3 dB cutoff frequency and pulse slimming of the electronic filter, the hysteresis level of the pulse qualifier, and the center frequency of the data separator. A single latched TTL output is also provided to control switching of external loop filter components on the data separator. A serial microprocessor interface reduces the pin count and provides convenient access to the internal program storage registers. The 32P4664 requires a +5 VDC supply and is available in a 24-lead SO and VSOP package.

## FEATURES

- **Programmable frequency output up to 72 MHz**
- **1% frequency resolution**
- **Differential PECL reference clock input (FREF)**
- **Differential PECL frequency reference output (FOUT)**
- **7-bit DAC for data separator center frequency control (DACI)**
- **7-bit DAC for filter Fc control (DACF)**
- **7-bit DAC for filter boost/equalization control (DACS)**
- **7-bit DAC for hysteresis level control (DACP)**
- **+5 VDC operation**
- **Available in small footprint 24-lead SO and VSOP packages**

## BLOCK DIAGRAM



## FUNCTIONAL DESCRIPTION

### FREQUENCY REFERENCE OPERATION

The 32P4664 programmable frequency reference accepts a differential PECL compatible clock source and generates a differential PECL compatible reference output (FOUT). The output frequency of FOUT is controlled by programming internal M and N counters to set up internal divide-by ratios. The 7-bit N register sets the divide-by factor for the input clock source. This will determine the update frequency for the phase detector. The value of this register is set based upon the frequency of the input clock according to the following equation:

$$N = [(FIN \times 256)/72] - 1$$

where FIN is in MHz

The 8-bit M register sets the divide-by term for the VCO reference clock feeding back into the phase detector and determines the center frequency of the VCO. The value set in the M register is independent of the input clock frequency. The value of the M register is determined by the following equation:

$$FOUT = [(M+1)/(N+1)] \times FIN$$

### DAC OPERATION

The output of each of the four 7-bit DACs is controlled by programming the associated register. In addition, each DAC has a reference input that determines the maximum DAC output. The following equations are used to calculate the DAC outputs:

$$I_{DACF} = (FREG \times 4)/(127 \times IR)\ mA$$

$$I_{DACI} = (7.41E\text{-}2 \times IREG)/RR\ mA, \text{ where RR is in } k\Omega$$

$$V_{DACP} = [2 \times PREG \times (VRP - (VCA - VR3))]/127\ V$$

$$V_{DACS} = (SREG \times VR3)/127\ V$$

### SERIAL PORT OPERATION

The 32P4664 provides a simple serial port interface that allows programming of the device's internal registers. The write-only serial port is a three-line interface that requires an enable signal (SDEN) along with clock (SCLK) and data (SDATA) signals to program the internal registers of the 32P4664. Data is shifted into the registers in 8-bit bytes that are divided into four bits of address and four bits of data. To load data into the device, the enable pin (SDEN) is asserted for eight clock cycles during which data can be presented on the SDATA input pin. Data on the SDATA pin is clocked into the device on the falling edges of the clock signal provided on the SCLK pin. The falling edge of SDEN latches the data internally and initiates the function selected. To save power the serial port circuitry is powered down when the SDEN line is low. Because of this, there is a minimum set-up and hold time for the SDEN signal (refer to specifications.) Table 1 provides the address-to-function mapping for the internal registers.

**TABLE 1: Data Packet Fields**

| ADDRESS BITS | | | | REGISTER | DATA BITS | | | |
|---|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | | D3 | D2 | D1 | D0 |
| 0 | 1 | 0 | 0 | P Register | X | P6 | P5 | P4 |
| 0 | 1 | 0 | 1 | P Register | P3 | P2 | P1 | P0 |
| 0 | 1 | 1 | 0 | I Register | X | I6 | I5 | I4 |
| 0 | 1 | 1 | 1 | I Register | I3 | I2 | I1 | I0 |
| 1 | 0 | 0 | 0 | S Register | X | S6 | S5 | S4 |
| 1 | 0 | 0 | 1 | S Register | S3 | S2 | S1 | S0 |
| 1 | 0 | 1 | 0 | F,C Register | C0 | F6 | F5 | F4 |
| 1 | 0 | 1 | 1 | F Register | F3 | F2 | F1 | F0 |
| 1 | 1 | 0 | 0 | M Register | M7 | M6 | M5 | M4 |
| 1 | 1 | 0 | 1 | M Register | M3 | M2 | M1 | M0 |
| 1 | 1 | 1 | 0 | N Register | X | N6 | N5 | N4 |
| 1 | 1 | 1 | 1 | N Register | N3 | N2 | N1 | N0 |

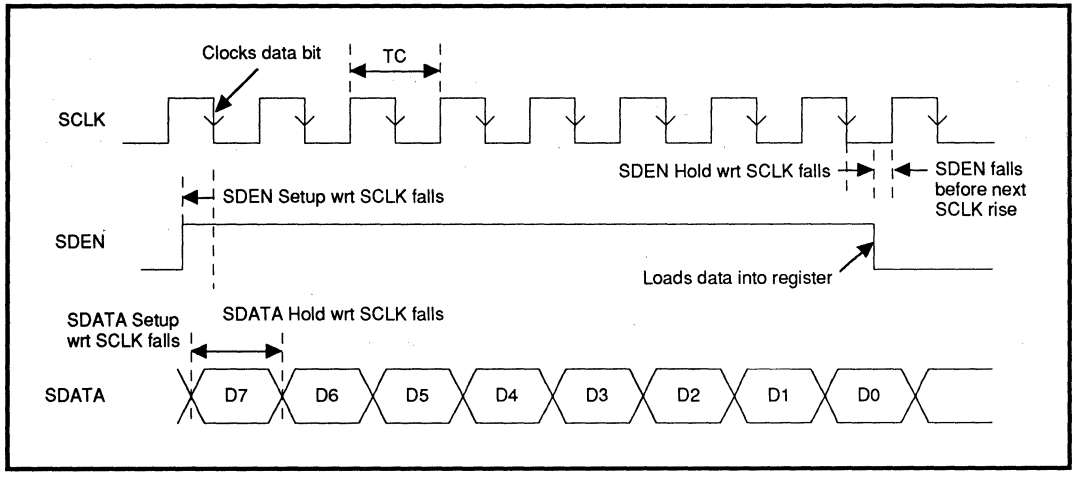



**FIGURE 1: Serial Port Timing Relationship**

## PIN DESCRIPTION

### INPUT PINS

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| AGND | I | Analog ground pin. |
| DGND | I | Digital ground pin. |
| VCA, B | I | +5V analog power supply pins. |
| VCD | I | +5V digital power supply pin. |
| FOEN | I | This is a TTL compatible input that disables the output buffer of the FOUT pin. This function is used to reduce jitter when the reference output is not required. |
| FREF/$\overline{\text{FREF}}$ | I | Reference clock inputs. An 8 to 20 MHz differential PECL reference clock is applied to these input pins. This serves as the reference for the internal PLL. |
| IR | I | Reference Current Input. The current applied to this pin provides the reference for DACF. |
| SDATA | I | Serial port input data. Data input for an 8-bit internal shift register. The data packet is transmitted MSB (D7) first. The first four bits are the register address and the last four bits are the data value. For loading data into both registers of a DAC or the M and N counters, it is suggested that the registers be loaded with a minimum delay between packets to reduce the output transients. |
| SCLK | I | Serial Data Clock. Serial data is clocked into the internal shift register on the falling edge of this input. |
| SDEN | I | Serial Data Enable. A high level TTL input on this pin will enable the clocking of the internal shift register. The data in the shift register is latched on the falling edge of SDEN. |
| VRP | I | Reference Input Voltage. The voltage applied to this pin establishes the reference for DACS. |
| VR3 | I | Reference Input Voltage. The voltage applied to this pin establishes the reference for DACP. |

**OUTPUT PINS**

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| DACF | O | Current DAC output. The output of this 7-bit current DAC is determined by the contents of the F register and the current applied to the IR pin. |
| DACI | O | Current DAC output. The output of this 7-bit current DAC is determined by the contents of the I register and the resistor across the VR1/VR2 pins. |
| DACP | O | Voltage DAC output. The output of this 7-bit voltage DAC is determined by the contents of the P register. |
| DACS | O | Voltage DAC output. The output of this 7-bit voltage DAC is determined by the contents of the S register. |
| FCO | O | Filter Control Output. This is a latched TTL output that can be used to switch an external FET for changing the components of the data separator loop filter. When C0 is set high ("1") in the F register, the FCO output will be high. |
| FOUT/$\overline{\text{FOUT}}$ | O | Frequency Output. A differential PECL frequency reference output that is determined by the M and N registers and the FREF/$\overline{\text{FREF}}$ input frequency. This output should be AC coupled into the reference input of the data separator device. |

**ANALOG PINS**

| | | |
|---|---|---|
| FLTR | – | PLL loop filter. An RC filter is connected to this pin to control the VCO voltage. |
| VR1/VR2 | – | Current setting resistor. A resistor is connected between these pins to set the current reference for DACI. |

## ELECTRICAL SPECIFICATIONS

Unless otherwise specified, the recommended operating conditions are as follows: 4.65V < POSITIVE SUPPLY VOLTAGE < 5.25V, 0 °C < T (ambient) < 70 °C, and 25 °C < T(junction) < 135 °C. Currents flowing into the chip are positive. Current maximums are currents with the highest absolute value.

### ABSOLUTE MAXIMUM RATINGS

Operation beyond the maximum ratings may damage the device.

| PARAMETER | RATING |
|---|---|
| Storage Temperature | -65 to 150 °C |
| Junction Operating Temperature, Tj | +150 °C |
| Positive Supply Voltage (VCA, VCB, VCD) | -0.5V to 7V |
| Voltage Applied to Logic Inputs | -0.5V to Vp+0.5V |
| Maximum Power Dissipation | 540 mW |

### RECOMMENDED OPERATING CONDITIONS

| | |
|---|---|
| Positive Supply Voltage (VCA, VCB, VCD) | 4.65V to 5.25V |
| Junction Operating Temperature, Tj | 0 ≤ Tj ≤ 130 °C |
| Ambient Temperature, Ta | 0 ≤ Ta ≤ 70 °C |

### POWER SUPPLY CURRENT AND POWER DISSIPATION

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| ICC (VCA, B, D) | Outputs and test point pins open | | 77 | 103 | mA |

### TTL COMPATIBLE INPUTS

| | | | | | | |
|---|---|---|---|---|---|---|
| Input low voltage | VIL | | | | 0.8 | V |
| Input high voltage | VIH | | 2.0 | | | V |
| Input low current | IIL | VIL=0.4V | | | -1.5 | mA |
| Input high current | IIH | VIH = 2.7V | | | 20 | µA |

### TTL COMPATIBLE OUTPUTS

| | | | | | | |
|---|---|---|---|---|---|---|
| Output low voltage | VOL | IOL = 2.0 mA | | | 0.5 | V |
| Output high voltage | VOH | IOH = -400 µA | 2.4 | | | V |

### PECL OUTPUT LEVELS (FOUT/$\overline{\text{FOUT}}$)

| | | | | | | |
|---|---|---|---|---|---|---|
| Output high level | | VCA = 5.0 V | VCA-1.02 | | | V |
| Output low level | | VCA = 5.0 V | | | VCA-1.45 | V |
| Single-ended output voltage swing | | VCA = 5.0 V | 0.75 | | 0.95 | V |
| Output current | IFOUT | | -4.0 | | +4.0 | mA |

## ELECTRICAL SPECIFICATIONS (continued)

### PECL INPUT LEVELS (FREF/$\overline{FREF}$)

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| Input high level | VFIH | VCA = 5.0 V | VFIL-0.5 | | VCA-0.5 | V |
| Input high current | IFIH | | | | 100 | µA |
| Input low level | VFIL | VCA = 5.0 V | VCA-2.2 | | VFIH-0.5 | V |
| Input low current | IFIL | | -100 | | | µA |
| Differential input voltage swing | | VCA = 5.0 V | 0.5 | | | V |

### FREQUENCY REFERENCE OUTPUT

Unless otherwise specified, FOUT = 30 MHz; loop filter components are C1 = 3300 pF, C2 = 270 pF, R1 = 4.12 kΩ; 4.65V ≤ VCn ≤ 5.25V; 0 ≤ Ta ≤ 70 °C.

| | | | | | | |
|---|---|---|---|---|---|---|
| Reference frequency | FIN | | 8 | | 20 | MHz |
| Output frequency | FOUT | | | | 72 | MHz |
| Output jitter | JFO | | -300 | | +300 | ps(RMS) |
| Output duty cycle | | 50% amplitude, FOUT = 72 MHz | 42 | | 58 | % |
| M counter value | | | 80 | | 255 | |
| N counter value | | | 25 | | 127 | |
| RR resistor value | | | 4.5 | | 5.25 | kΩ |
| VCO center frequency | TVCO | To=(4.01E-2)(RR/M) + 2.4 nsec; VCA = 5.0V, RR = 4.75 kΩ, FLTR = 2.7V, M = 100, FIN = 20 MHz | 0.77 TVCO | TVCO | 1.23 TVCO | ns |
| VCO dynamic range | | 1V < FLTR < VCA-0.5 FOUT = 72 MHz, VCA = 5.0V | ±25 | | ±45 | % |
| VCO control gain | KVCO | ωi = 2π/TVCO | 0.14ωi | | 0.26ωi | rad/s V |
| Phase detector gain | KD | KD = (4.39E-3) x M/RR | | KD | | A/rad |

### CONTROL DACs

| | | | | | |
|---|---|---|---|---|---|
| Differential linearity (monotonicity) | DACF, I, P, S<br>0 ≤ Ta ≤ 70 °C<br>4.75V ≤ VCA ≤ 5.25V | -1LSB | | | |
| DACF output accuracy | VCA = 5.0V<br>IF = (0.98 • F • 4 • IR)/128<br>Rx = 2.74 kΩ<br>IR = VR3/(4 x Rx) | 0.97 • IF<br><br>-3/4 LSB | | 1.03 • IF<br><br>+3/4 LSB | A |
| Rx resistor value | | 2.5 | | 3.0 | kΩ |
| DACF output resistance | | | | 3.7 | kΩ |

**CONTROL DACs** (continued)

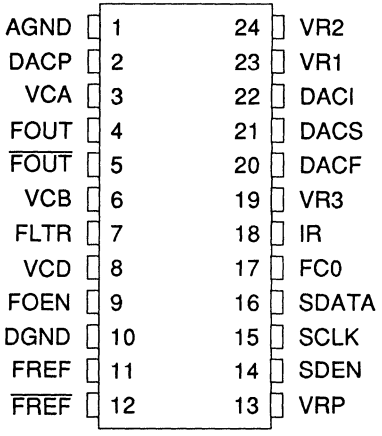
| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| DACI output accuracy | VCA = 5.0V<br>$I_I$ = (7.41E - 2) • I/RR<br>RR = 4.75 kΩ | 0.95 • $I_I$<br><br>-3/4 LSB | | 1.05 • $I_I$<br><br>+3/4 LSB | A |
| DACI/F output voltage | | | | 2 | V |
| DACP output accuracy | VCA = 5.0V<br>$V_P$ = 2 • P • [VRP - (VCC -VR3)]/128<br>RR = 4.75 kΩ<br>VR3 = 2.2V<br>VRP = 3.6V | 0.97 • $V_P$<br><br>-3/4LSB<br>-25 mV | | 1.04 • $V_P$<br><br>+3/4LSB<br>+25 mV | V |
| DACP output range | | VCA-VR3 | | VCA-0.9 | V |
| DACP output resistance | | 50 | | 200 | Ω |
| VRP input voltage | | (VCA -VR3) + 0.2 | | VCA -1.0 | V |
| VRP input current | 2.0V ≤ VRP ≤ VCA | | | 20 | μA |
| DACS output accuracy | VCn = 5.0V<br>$V_S$ = (0.98 • S • VR3)/128 | 0.97 • $V_S$<br><br>-3/4LSB<br>-15 mV | | 1.03 • $V_S$<br><br>+3/4LSB<br>+15 mV | V |
| DACS output range | | 0.1 | | 2.4 | V |
| DACS output resistance | | | | 3.7 | kΩ |
| VR3 input voltage | | 2.0 | | 2.4 | V |
| VR3 input current | VR3 = 2.2V | | | 1.0 | mA |

**SERIAL PORT TIMING**

| | | | | | |
|---|---|---|---|---|---|
| SCLK period | | 100 | | | ns |
| SDEN Setup wrt first SCLK falls | | 25 | | | ns |
| SDEN Hold wrt last SCLK falls | | 25 | | | ns |
| SDEN falls wrt next SCLK rise | | 25 | | | ns |
| SDATA Setup/Hold wrt SCLK falls | | 25 | | | ns |

## PACKAGE PIN DESIGNATIONS

(Top View)




**24-Lead SO/VSOP**

CAUTION: Use handling procedures necessary for a static sensitive component.



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**Notes:**

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A TDK Group Company

# SSI 32D4665
## Time Base Generator

**Advance Information**

December 1992

4

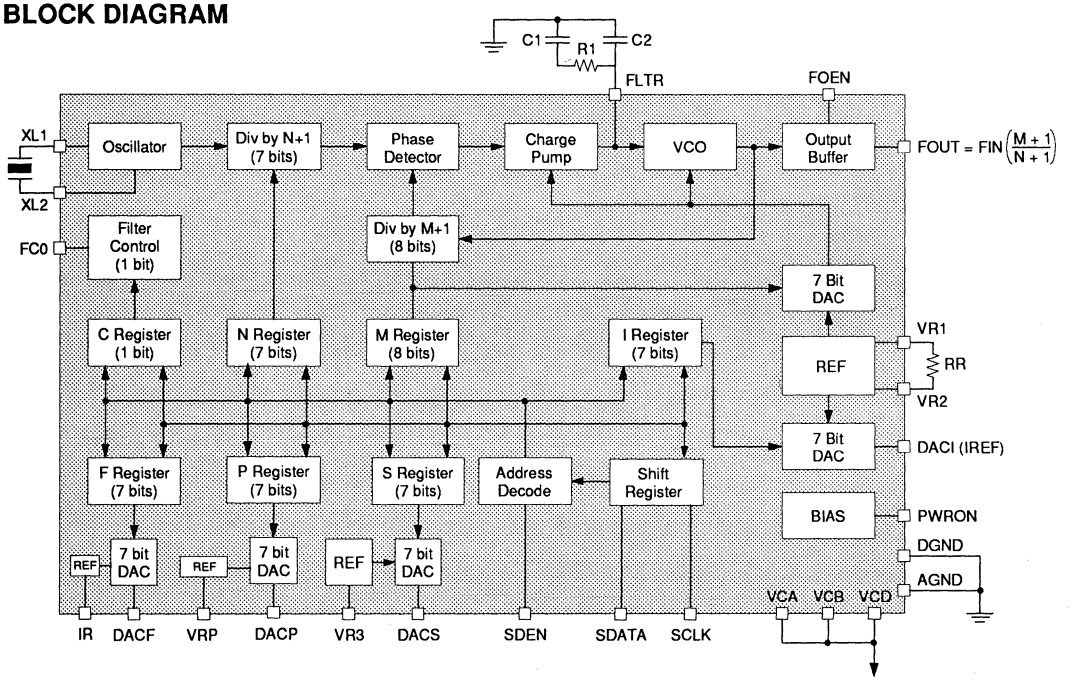
## DESCRIPTION

The SSI 32D4665 Time Base Generator provides a programmable reference generator, channel filter control and data rate control for constant density recording applications. It is optimized to operate with the 32D53xx series data separators and contains a high performance programmable PLL for 1% reference frequency control. A 7–bit DAC is provided to program the IREF current which sets the data separator PLL operating center frequency. A 7–bit DAC is provided to program the hysteresis level in the SSI 32P3000 series pulse detectors. Two additional 7–bit DACs are provided for programmable electronic filter (slimmer) control. A single latched TTL output is provided to control filter multiplexers. A serial microprocessor interface reduces pin count and provides convenient access to the internal program storage registers. The 32D4665 only requires a +5V supply and will be available in 24-lead SO packages.

## FEATURES

- **For constant density recording applications**
- **Reference frequency control**
- **Channel filter control**
- **Internal DAC available to program data separator data rate**
- **Internal DAC available to program pulse detector hysteresis (DACP)**
- **Up to 75 MHz operation**
- **1% frequency resolution**
- **No external active components required**
- **+5V only operation**
- **Low power mode**
- **24-lead SOL package**

## BLOCK DIAGRAM




CAUTION: Use handling procedures necessary for a static sensitive component.

## PIN DESCRIPTION

### INPUT PINS

| NAME | DESCRIPTION |
|---|---|
| SDATA | Serial Data. Data input for an 8-bit control shift register. The data packet is transmitted MSB (D7) first. The first four bits are the register address and the last four are its data bits. Registers larger than 4-bits must be loaded with two 8-bit data packets. These packets should be loaded sequentially in less than 10 µs since the loading operation will cause output transients. With proper loop filter design, the output transients will recover within 1 ms. The data packet fields are given in Table 1. |
| SCLK | Serial Data Clock. Negative edge triggered clock input for the serial data. |
| SDEN | Serial Data Enable. A high level input enables data loading. The data is latched when the input is low. |
| PWRON | Power On. A high level input enables the chip. A low level puts the chip in a low power idle state. |
| FOEN | Frequency Output Enable. A high level input enables the FOUT output. A low level disables the output and minimizes the driven data separator jitter. |

### OUTPUT PINS

| | |
|---|---|
| FOUT | Frequency Output. An ECL output with internal current source. The low voltage swing which minimizes data separator jitter must be AC coupled to the data separator XTL1 input. FOUT = [(M +1)/(N +1)]FIN where M = M Register number and N must be set to approximately [(FIN) (256) / 72 MHz] - 1. |
| DACI | DAC Output. 7-bit DAC current source output used to program timing current for the data separator VCO center frequency. The current magnitude is controlled by the I Register and is compensated to minimize the sensitivity to power supply and temperature variations. |
| DACP | DAC Output. 7-bit DAC voltage output used to program hysterysis levels to the pulse detector. The output voltage is set by tyhe difference between the VRP input voltage and the value of (Vcc - VR3). The voltage at the output is: (Vcc - VR3) + (2.0 • P/127) • (VRP - (Vcc - VR3). |
| DACF | DAC Output. 7-bit DAC current source output used for electronic filter control. The output current is set by the F Register number and the current entering the IR pin. This can be generated by an external resistor (Rx) between VR3 and IR or an external current source. |
| DACS | DAC Output. 7-bit DAC voltage output used for electronic filter control. The output voltage is set by the voltage at VR3 and the S Register number. |
| FC0 | Filter Control 1. TTL output used to control an external filter multiplexer. C0 = H sets FC0 = H. |

**ANALOG PINS**

| | |
|---|---|
| XTL1, XTL2 | Crystal Oscillator Connections. The circuit is designed to be used with an 8 MHz to 20 MHz crystal. If a crystal is not desired, XTL1 may be driven by a TTL source with XTL2 left open. |
| VR1, VR2 | Current Setting Resistor Connections. An external resistor RR connected between VR1 and VR2 sets the voltage controlled oscillator center frequency and the DACI currents. |
| VR3 | Reference Voltage Input. An external 2.2V supply sets the reference for the DACS voltage. |
| FLTR | PLL Loop Filter Connection. Connection for loop filter components R1, C1 and C2. |
| DGND, AGND | Digital and Analog Ground |
| VCA, VCB | Analog +5V Supplies |
| VCD | Digital +5V Supply |
| IR | Reference Current Input. An external resistor Rx, connected from IR to VR3 reference voltage or an external current source sets the reference current for the DACF current. |
| VRP | Reference Voltage Input. The output level for DACP is set by the difference between (Vcc - VR3) and VRP. |

**TABLE 1: Data Packet Fields**

| ADDRESS BITS | | | | USAGE | DATA BITS | | | |
|---|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | | D3 | D2 | D1 | D0 |
| 0 | 1 | 0 | 0 | P REGISTER | X | P6 | P5 | P4 |
| 0 | 1 | 0 | 1 | P REGISTER | P3 | P2 | P1 | P0 |
| 0 | 1 | 1 | 0 | I REGISTER | X | I6 | I5 | I4 |
| 0 | 1 | 1 | 1 | I REGISTER | I3 | I2 | I1 | I0 |
| 1 | 0 | 0 | 0 | S REGISTER | X | S6 | S5 | S4 |
| 1 | 0 | 0 | 1 | S REGISTER | S3 | S2 | S1 | S0 |
| 1 | 0 | 1 | 0 | F, C REGISTER | C0 | F6 | F5 | F4 |
| 1 | 0 | 1 | 1 | F REGISTER | F3 | F2 | F1 | F0 |
| 1 | 1 | 0 | 0 | M REGISTER | M7 | M6 | M5 | M4 |
| 1 | 1 | 0 | 1 | M REGISTER | M3 | M2 | M1 | M0 |
| 1 | 1 | 1 | 0 | N REGISTER | X | N6 | N5 | N4 |
| 1 | 1 | 1 | 1 | N REGISTER | N1 | N2 | N1 | N0 |

X = Don't care bit.

## ELECTRICAL SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may damage the device.

| PARAMETER | RATING | UNITS |
|---|---|---|
| Storage Temperature | –65 to +150 | °C |
| Junction Operating Temperature, Tj | +150 | °C |
| Supply Voltage, VCA, VCB, VCD | –0.5 to 7 | V |
| Voltage Applied to Logic Inputs | –0.5 to 5.5 | V |
| Maximum Power Dissipation | 540 | mW |

### RECOMMENDED OPERATING CONDITIONS

| PARAMETER | RATING | UNITS |
|---|---|---|
| Supply voltage, VCA = VCB = VCD | 4.65 to 5.25 | V |
| Junction Temperature, Tj | 0<Tj<135 | °C |
| Ambient Temperature, Ta | 0<Ta<70 | °C |

### ELECTRICAL CHARACTERISTICS

Unless otherwise specified: recommended operating conditions apply.

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| VIH | High Level Input Voltage | | 2.0 | | | V |
| VIL | Low Level Input Voltage | | | | 0.8 | V |
| IIH | High Level Input Current | VIH = 2.7V | | | 20 | µA |
| IIL | Low Level Input Current | VIL = 0.4V | | | -1.5 | mA |
| VOH | High Level Output Voltage | IOH = -400 µA | 2.4 | | | V |
| VOL | Low Level Output Voltage | IOL = 2 mA | | | 0.5 | V |
| VOH | FOUT ECL High Level | VCD = 5V, VOH-VCD | -1.02 | | | V |
| VOL | FOUT ECL Low Level | VCD = 5V, VOL-VCD | | | -1.45 | V |
| ICC | Power Supply Current | PWRON = 2.0V | | 77 | 103 | mA |
| | | PWRON = 0.8V | | 25 | | mA |
| IO | FOUT Output Current | | | ±4 | | mA |
| VO | FOUT Output Swing | | 0.6 | | | V |

## INPUT/OUTPUT CHARACTERISTICS

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|---|
| FIN | FIN Frequency | | 8 | | 20 | MHz |
| FO | FOUT Frequency | | | | 72 | MHz |
| JFO | FOUT Jitter | TO = 1/FO; FCLK active | | | ±400 | ps(pk) |
| DFO | FOUT Duty Cycle | 50% Amplitude<br>FOUT = 72 MHz | 42 | | 58 | % |
| M | M Divide Number | | 80 | | 255 | - |
| N, F | N, F Divide Number | | 25 | | 127 | - |
| P | P Register Number | | 10 | | 127 | - |
| I | I Register Number | | 30 | | 127 | - |
| RR | External Resistor | | 4.50 | | 5.25 | kΩ |
| TVCO | VCO Center Frequency Period | TO=(6.17 E-10)(RR/M)+2.4 ns<br>VCC = 5V, RR = 4.75 kΩ<br>FLTR = 2.7V<br>FIN = 20 MHZ, M = 100 | 0.77TO | TVCO | 1.23TO | ns |
| | VCO Frequency Dynamic Range | 1V < FLTR < VCC – 0.5V,<br>VCC = 5V, FOUT = 31.5 MHz | ±25 | | ±45 | % |
| KVCO | VCO Control Gain | ωi = 2π/TVCO | 0.14ωi | | 0.26ωi | rad/s V |
| KD | Phase Detector | KD = (4.39 E – 3)/RR | | KD | | A/rad |
| IOI | DACI Current | IO = (7.41 E-2)I/RR<br>VCC = 5V, TA = 25°C,<br>RR = 4.75 kΩ | 0.95IO<br>–3/4LSB | | 1.05IO<br>+3/4LSB | A |
| IOF | DACF Current | IOF = F • 4/128 • IR<br>VCC = 5V, Rx = 2.74 kΩ<br>Where IR = VR3/(4 • R) or an external current source | 0.97IOF<br>–3/4LSB | | 1.03IOF<br>+3/4LSB | V |
| VOP | DACP Voltage | VOP = 2.0 • P • (VRP-(Vcc-VR3))/128<br>VCC = 5V, VR3 = 2.2V,<br>VRP = 3.6V | 0.97VOP<br>+(Vcc-VR3)<br>-3/4LSB<br>-25mV | | 1.04VOP<br>+(Vcc-VR3)<br>+3/4LSB<br>+25mV | A |
| VOS | DACS Voltage | VOS = S • VR3/128<br>VCC = 5V | 0.97VOS<br>–3/4LSB<br>+15 mV | | 1.03VOS<br>+3/4LSB<br>+60 mV | V |
| VR3 | DAC Reference | | 2.0 | | 2.4 | V |
| IVR3 | VR3 Input Current | VR3 = 2.2V | | | 1.0 | mA |

**INPUT/OUTPUT CHARACTERISTICS** (Continued)

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|---|
| Rx | | | 2.5 | | 3.0 | kΩ |
| VRP | DAC P Reference | | (Vcc-VR3) +0.2 | | Vcc-1.0 | V |
| IVRP | VRP Input Current | 2.0V ≤ VRP ≤ Vcc | | | 20 | µA |
| I | DAC Current Tolerance | RR = 4.75 kΩ<br>0°C < Ta < 70°C<br>4.75V < Vcc < 5.25V | .81 IO | | 1.17 IO | A |
| I, F, P, S | Differential Linearity (Monotonicity) | 0°C < Ta < 70°C<br>4.75V < Vcc < 5.25V | -1LSB | | | - |
| VODL | DACI, DACF Output Voltage | | | | 2 | V |
| VOSL | DACS Output Voltage | | 0.1 | | 2.4 | V |
| VOPL | DACP Output Voltage | | Vcc-VR3 | | Vcc-0.9 | V |
| ROUT | DACF, DACS Output Resistance | | | | 3.7 | kΩ |
| SCLK | Data Clock Period, TC | | 100 | | | ns |
| TDD | Data Set Up/Hold Time | | 25 | | | ns |
| TDE | Data Enable Delay Time | Delay from data clock rising edge | -TC | | TC/4 | ns |
| ROUTP | DACP Output Resistance | | 50 | | 200 | Ω |

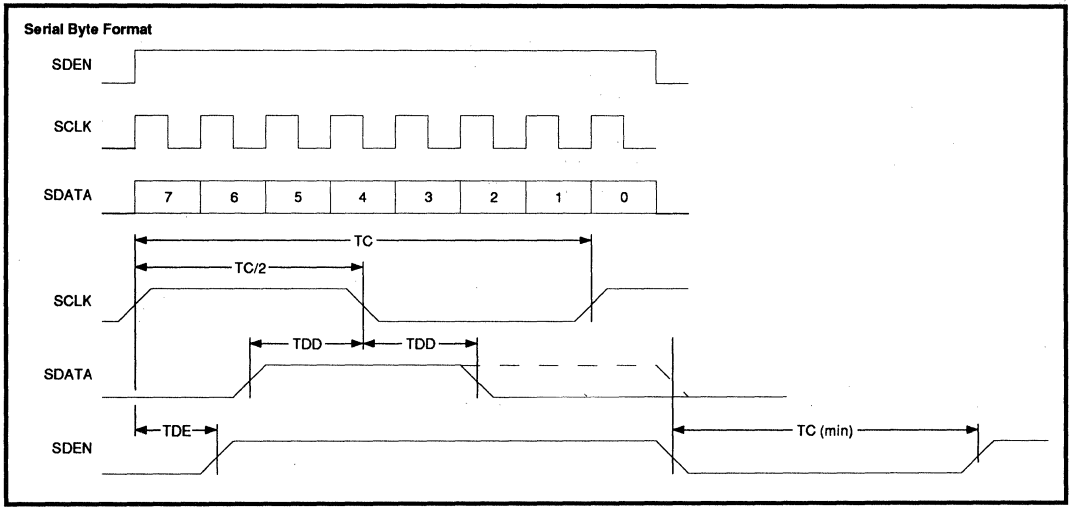



**FIGURE 1: Serial Port Timing**

## APPLICATIONS INFORMATION

### REFERENCE FREQUENCY OUTPUT:

The 32D4665 provides the reference frequency for the phase-locked loop (PLL) of a data separator. The required frequency is programmed using the **M** and **N** registers of the 4661. The value of the **N** register is determined by the oscillator that drives the 32D4665 according to the following equation:

$$N=\frac{(Fin \cdot 256)}{(72\ MHz)}-1$$

For this application, using a 12 MHz oscillator (Fin) would yield an **N** value of 41.7. Although the value of **N** should be fixed according to the equation shown above, there is a tolerance of ± 1 integer so **N** can be set from 41 to 43. (This is necessary as the phase detector frequency is fixed by Fin & **N**) Substituting **N** into the following equation and knowing the reference frequency required for each data rate allows for the determination of the **M** register value:

$$Fout=\frac{(M+1)}{(N+1)} \cdot Fin$$

Since **M** must be an integer value, it may be necessary to change **N** values for each data rate to obtain the required output frequency. For example (for 1.5x reference clock), at 24 Mbit/s the required reference frequency is 36 MHz and using a value of **N** = 41, yields an **M** value of 125. At 30 Mbit/s using the **N** value of 41 would require an **M** value of 156.5 to produce an output frequency of 45 MHz. Using **M** = 156 would give an output frequency of 44.86 MHz while using an **M** value of 157 the output frequency would be 45.14 MHz. If **N** is changed to 43 then a value of 146 for **M** would produce the required output frequency of 45 MHz. The required **M** and **N** values for some sample data rates are provided in the table that follows.

**TABLE 2: M and N Register Programming Example**

| DR (Mbit/s) | Fout | M | N |
|---|---|---|---|
| 24 Mbit/s | 36 MHz | 125 | 41 |
| 30 Mbit/s | 45 MHz | 164 | 43 |
| 36 Mbit/s | 54 MHz | 188 | 41 |
| 40 Mbit/s | 60 MHz | 209 | 41 |

The **N** register is at address "1110" for the MSBs and address "1111" for the LSBs. The table that follows gives the required register programming information for the values of **N**.

**TABLE 3: Frequency Programming Information, N Register**

| ADDRESS BITS | | | | DATA BITS | | | | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 1 | 1 | 1 | 0 | X | 0 | 1 | 0 | N Register MSBs for N = 41 |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | N Register LSBs for N = 41 |
| 1 | 1 | 1 | 0 | X | 0 | 1 | 0 | N Register MSBs for N = 43 |
| 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | N Register LSBs for N = 43 |

The **M** register is at address "1100" for the MSBs and at address "1101" for the LSBs. The table that follows gives the required register programming information for the values of **M** based on the equation given above for Fout.

## APPLICATIONS INFORMATION (continued)

**TABLE 4: Frequency Programming Information, M Register**

| ADDRESS BITS | | | | DATA BITS | | | | FUNCTION |
|---|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | M Register = 125, |
| 1 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | Fout = 36 MHz |
| 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | M Register = 164, |
| 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | Fout = 45 MHz |
| 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | M Register = 188, |
| 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | Fout = 54 MHz |
| 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | M Register = 209, |
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | Fout = 60 MHz |

**Loop Filter for the SSI 32D4665**

The SSI 32D4665 requires a loop filter to control the PLL locking characteristics. While there are several types of filters that can be used to perform this function, a simple integrating filter has proven to be very effective (see Figure 2). To select the components for the loop filter, two considerations should be made. First, the acquisition time of the loop must be less than the minimum track-to-track seek time and second, the capacitor C1 should be low leakage (C1 < 1.0 µF). The acquisition time of the loop is set-up to accommodate a zero phase restart and allow for 1% maximum phase error after phase acquisition. This yields a settling time of: $t_s = 5/\omega_n$.

From the data sheet,

KVCO = (0.21)(2π)($F_{out}$) rad/s V (typ.), at 72 MHz  KVCO = $9.5 \times 10^7$

KD = (4.14 E-3)/RR A/rad  @ RR = 4.75 kΩ, KD = $8.76 \times 10^{-7}$

For a second order system,

R1 = (2 x ζ x $\omega_n$)/(KVCO x KD) where ζ is the damping factor.

C1 = (KVCO x KD)/($\omega_n^2$) and C1/10 > C2 > C1/20

A damping factor of 0.7 to 1.0 is suggested to prevent locking to harmonics while maintaining an acceptable lock time. At the maximum frequency selected, the damping factor of 1.0 should be considered thereby allowing the damping factor to drop as the frequency drops.

If we start with $\omega_n = 2 \times 10^4$, C1 can be calculated as 0.21 µF and C2 can be calculated as 0.01 to 0.02 µF. As mentioned above, the damping factor at the maximum frequency of 72 MHz should be 1.0, so R1 is calculated as:

R1 = (2 x 1.0 x 2E4 )/(9.5E7 x 8.76E-7) = 480 Ω

These values will produce a loop settling time $t_s$ of $5/2 \times 10^4$ = 250 µsecs.

The values calculated here are sample values that have been used in the lab and should be considered starting values. The values of R1, C1, and C2 can be further optimized to meet specific needs.

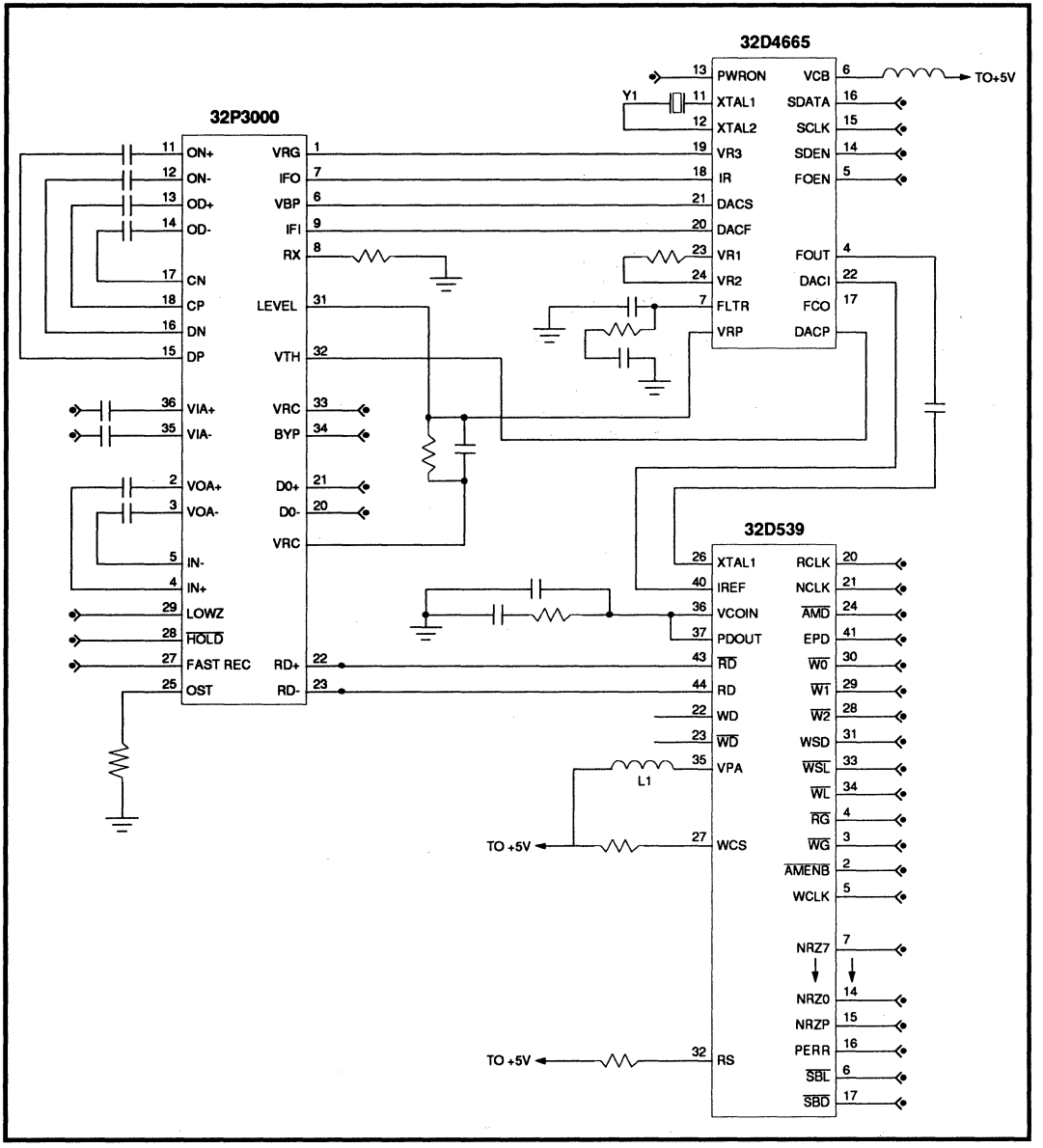
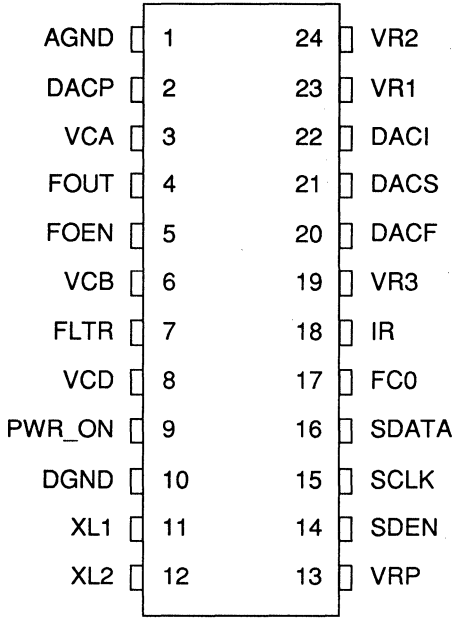



**FIGURE 2: Typical 32D4665 Application**

# SSI 32D4665
# Time Base Generator

## PACKAGE PIN DESIGNATIONS
(Top View)




**24-Lead SOL**

**Advance Information:** Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.



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silicon systems®
A TDK Group Company

# SSI 32D4666
## Time Base Generator

**Advance Information**

August 1992

4

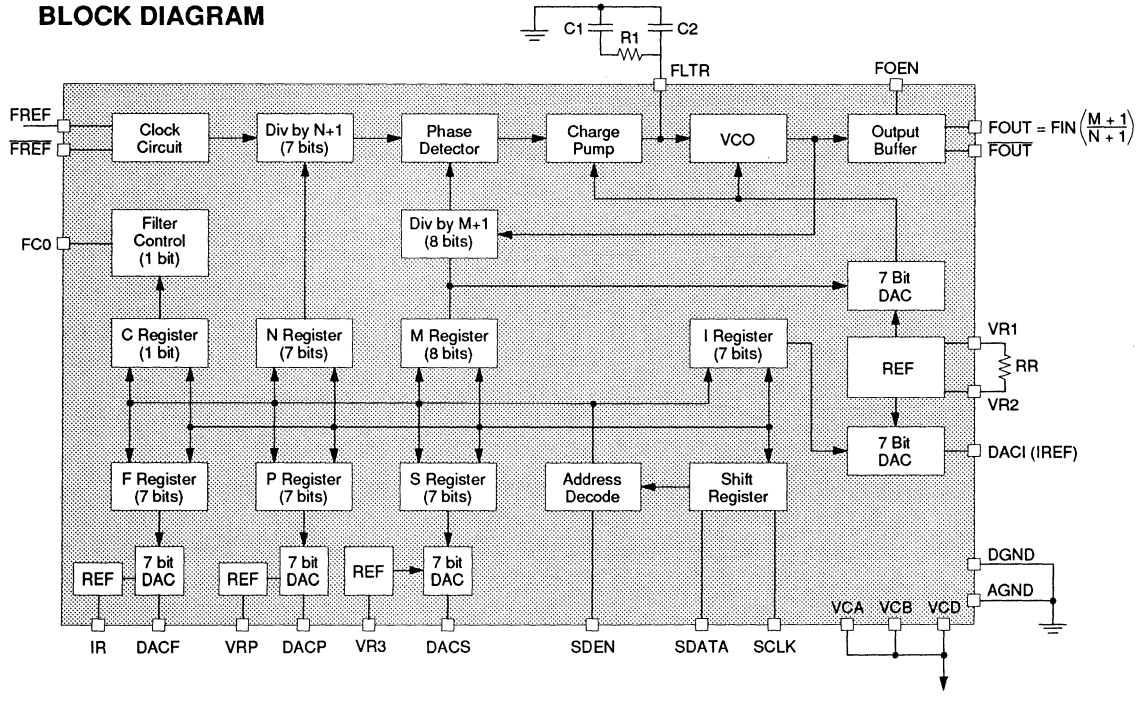
## DESCRIPTION

The SSI 32D4666 is a high performance bipolar device that provides a programmable frequency reference and four internal control DACs to support hard disk drive applications that use zoned recording techniques. It is optimized for use with the 32P3000 family of pulse detector/filter devices and the 32P53X family of data separators. The frequency reference can be programmed up to 108 MHz with better than 1% resolution. The 7-bit DACs provide control of the 3 dB cutoff frequency and pulse slimming of the electronic filter, the hysteresis level of the pulse qualifier, and the center frequency of the data separator. A single latched TTL output is also provided to control switching of external loop filter components on the data separator. A serial microprocessor interface reduces the pin count and provides convenient access to the internal program storage registers. The 32D4666 requires a +5 VDC supply and is available in a 24-pin SO and VSOP package.

## FEATURES

- **Programmable frequency output up to 108 MHz**
- **1% frequency resolution**
- **Differential PECL reference clock input (FREF)**
- **Differential PECL frequency reference output (FOUT)**
- **7-bit DAC for data separator center frequency control (DACI)**
- **7-bit DAC for filter Fc control (DACF)**
- **7-bit DAC for filter boost/equalization control (DACS)**
- **7-bit DAC for hysteresis level control (DACP)**
- **+5 VDC operation**
- **Available in small footprint 24-pin SO and VSOP packages**

## BLOCK DIAGRAM



## FUNCTIONAL DESCRIPTION

### FREQUENCY REFERENCE OPERATION

The 32D4666 programmable frequency reference accepts a differential PECL compatible clock source and generates a differential PECL compatible reference output (FOUT). The output frequency of FOUT is controlled by programming internal M and N counters to set up internal divide-by ratios. The 7-bit N register sets the divide-by factor for the input clock source. This will determine the update frequency for the phase detector. The value of this register is set based upon the frequency of the input clock according to the following equation:

$$N = [(FIN \times 256)/108] - 1$$

where FIN is in MHz

The 8-bit M register sets the divide-by term for the VCO reference clock feeding back into the phase detector and determines the center frequency of the VCO. The value set in the M register is independent of the input clock frequency. The value of the M register is determined by the following equation:

$$FOUT = [(M+1)/(N+1)] \times FIN$$

### DAC OPERATION

The output of each of the four 7-bit DACs is controlled by programming the associated register. In addition, each DAC has a reference input that determines the maximum DAC output. The following equations are used to calculate the DAC outputs:

$$I_{DACF} = (FREG \times 4)/(128 \times IR)\ mA$$

$$I_{DACI} = (7.41E\text{-}2 \times IREG)/RR\ mA, \text{ where RR is in } k\Omega$$

$$V_{DACP} = [2 \times PREG \times (VRP - (VCA - VR3))]/128\ V$$

$$V_{DACS} = (SREG \times VR3)/128\ V$$

### SERIAL PORT OPERATION

The 32D4666 provides a simple serial port interface that allows programming of the device's internal registers. The write-only serial port is a three-line interface that requires an enable signal (SDEN) along with clock (SCLK) and data (SDATA) signals to program the internal registers of the 32D4666. Data is shifted into the registers in 8-bit bytes that are divided into four bits of address and four bits of data. To load data into the device, the enable pin (SDEN) is asserted for eight clock cycles during which data can be presented on the SDATA input pin. Data on the SDATA pin is clocked into the device on the falling edges of the clock signal provided on the SCLK pin. The falling edge of SDEN latches the data internally and initiates the function selected. To save power the serial port circuitry is powered down when the SDEN line is low. Because of this, there is a minimum set-up and hold time for the SDEN signal (refer to specifications.) Table 1 provides the address-to-function mapping for the internal registers.

**TABLE 1: Data Packet Fields**

| ADDRESS BITS | | | | REGISTER | DATA BITS | | | |
|---|---|---|---|---|---|---|---|---|
| D7 | D6 | D5 | D4 | | D3 | D2 | D1 | D0 |
| 0 | 1 | 0 | 0 | P Register | X | P6 | P5 | P4 |
| 0 | 1 | 0 | 1 | P Register | P3 | P2 | P1 | P0 |
| 0 | 1 | 1 | 0 | I Register | X | I6 | I5 | I4 |
| 0 | 1 | 1 | 1 | I Register | I3 | I2 | I1 | I0 |
| 1 | 0 | 0 | 0 | S Register | X | S6 | S5 | S4 |
| 1 | 0 | 0 | 1 | S Register | S3 | S2 | S1 | S0 |
| 1 | 0 | 1 | 0 | F,C Register | C0 | F6 | F5 | F4 |
| 1 | 0 | 1 | 1 | F Register | F3 | F2 | F1 | F0 |
| 1 | 1 | 0 | 0 | M Register | M7 | M6 | M5 | M4 |
| 1 | 1 | 0 | 1 | M Register | M3 | M2 | M1 | M0 |
| 1 | 1 | 1 | 0 | N Register | X | N6 | N5 | N4 |
| 1 | 1 | 1 | 1 | N Register | N3 | N2 | N1 | N0 |

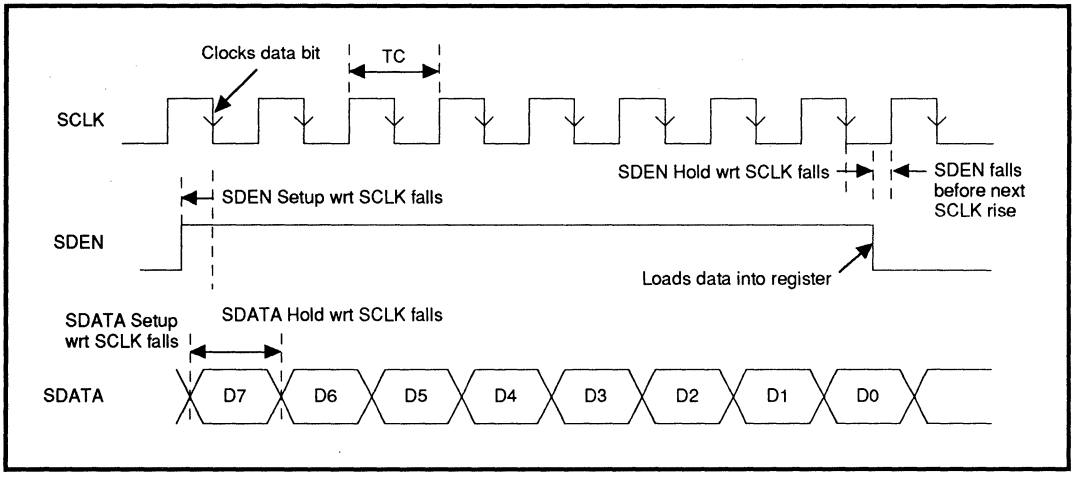



**FIGURE 1: Serial Port Timing Relationship**

## PIN DESCRIPTION

### INPUT PINS

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| AGND | I | Analog ground pin. |
| DGND | I | Digital ground pin. |
| VCA, B | I | +5V analog power supply pins. |
| VCD | I | +5V digital power supply pin. |
| FOEN | I | This is a TTL compatible input that disables the output buffer of the FOUT pin. This function is used to reduce jitter when the reference output is not required. |
| FREF/$\overline{\text{FREF}}$ | I | Reference clock inputs. An 8 to 20 MHz differential PECL reference clock is applied to these input pins. This serves as the reference for the internal PLL. |
| IR | I | Reference Current Input. The current applied to this pin provides the reference for DACF. |
| SDATA | I | Serial port input data. Data input for an 8-bit internal shift register. The data packet is transmitted MSB (D7) first. The first four bits are the register address and the last four bits are the data value. For loading data into both registers of a DAC or the M and N counters, it is suggested that the registers be loaded with a minimum delay between packets to reduce the output transients. |
| SCLK | I | Serial Data Clock. Serial data is clocked into the internal shift register on the falling edge of this input. |
| SDEN | I | Serial Data Enable. A high level TTL input on this pin will enable the clocking of the internal shift register. The data in the shift register is latched on the falling edge of SDEN. |
| VRP | I | Reference Input Voltage. The voltage applied to this pin establishes the reference for DACS. |
| VR3 | I | Reference Input Voltage. The voltage applied to this pin establishes the reference for DACP. |

**OUTPUT PINS**

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| DACF | O | Current DAC output. The output of this 7-bit current DAC is determined by the contents of the F register and the current applied to the IR pin. |
| DACI | O | Current DAC output. The output of this 7-bit current DAC is determined by the contents of the I register and the resistor across the VR1/VR2 pins. |
| DACP | O | Voltage DAC output. The output of this 7-bit voltage DAC is determined by the contents of the P register. |
| DACS | O | Voltage DAC output. The output of this 7-bit voltage DAC is determined by the contents of the S register. |
| FCO | O | Filter Control Output. This is a latched TTL output that can be used to switch an external FET for changing the components of the data separator loop filter. When C0 is set high ("1") in the F register, the FCO output will be high. |
| FOUT/$\overline{\text{FOUT}}$ | O | Frequency Output. A differential PECL frequency reference output that is determined by the M and N registers and the FREF/$\overline{\text{FREF}}$ input frequency. This output should be AC coupled into the reference input of the data separator device. |

**ANALOG PINS**

| | | |
|---|---|---|
| FLTR | – | PLL loop filter. An RC filter is connected to this pin to control the VCO voltage. |
| VR1/VR2 | – | Current setting resistor. A resistor is connected between these pins to set the current reference for DACI. |

## ELECTRICAL SPECIFICATIONS

Unless otherwise specified, the recommended operating conditions are as follows: 4.65V < POSITIVE SUPPLY VOLTAGE < 5.25V, 0 °C < T (ambient) < 70 °C, and 25 °C < T(junction) < 135 °C. Currents flowing into the chip are positive. Current maximums are currents with the highest absolute value.

### ABSOLUTE MAXIMUM RATINGS

Operation beyond the maximum ratings may damage the device.

| PARAMETER | RATING |
|---|---|
| Storage Temperature | -65 to 150 °C |
| Junction Operating Temperature, Tj | +150 °C |
| Positive Supply Voltage (VCA, VCB, VCD) | -0.5V to 7V |
| Voltage Applied to Logic Inputs | -0.5V to Vp+0.5V |
| Maximum Power Dissipation | 540 mW |

### RECOMMENDED OPERATING CONDITIONS

| | |
|---|---|
| Positive Supply Voltage (VCA, VCB, VCD) | 4.65V to 5.25V |
| Junction Operating Temperature, Tj | 0 ≤ Tj ≤ 130 °C |
| Ambient Temperature, Ta | 0 ≤ Ta ≤ 70 °C |

### POWER SUPPLY CURRENT AND POWER DISSIPATION

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| ICC (VCA, B, D) | Outputs and test point pins open | | 77 | 103 | mA |

### TTL COMPATIBLE INPUTS

| | | | | | | |
|---|---|---|---|---|---|---|
| Input low voltage | VIL | | | | 0.8 | V |
| Input high voltage | VIH | | 2.0 | | | V |
| Input low current | IIL | VIL=0.4V | | | -1.5 | mA |
| Input high current | IIH | VIH = 2.7V | | | 20 | µA |

### TTL COMPATIBLE OUTPUTS

| | | | | | | |
|---|---|---|---|---|---|---|
| Output low voltage | VOL | IOL = 2.0 mA | | | 0.5 | V |
| Output high voltage | VOH | IOH = -400 µA | 2.4 | | | V |

### PECL OUTPUT LEVELS (FOUT/$\overline{\text{FOUT}}$)

| | | | | | |
|---|---|---|---|---|---|
| Output high level | VCA = 5.0 V | VCA-1.02 | | | V |
| Output low level | VCA = 5.0 V | | | VCA-1.45 | V |
| Single-ended output voltage swing | VCA = 5.0 V | 0.75 | | 0.95 | V |
| Output current IFOUT | | -4.0 | | +4.0 | mA |

## ELECTRICAL SPECIFICATIONS (continued)

### PECL INPUT LEVELS (FREF/$\overline{FREF}$)

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| Input high level | VFIH | VCA = 5.0 V | VFIL-0.5 | | VCA-0.5 | V |
| Input high current | IFIH | | | | 100 | µA |
| Input low level | VFIL | VCA = 5.0 V | VCA-2.2 | | VFIH-0.5 | V |
| Input low current | IFIL | | -100 | | | µA |
| Differential input | | VCA = 5.0 V | 0.5 | | | V |

### FREQUENCY REFERENCE OUTPUT

Unless otherwise specified, FOUT = 30 MHz; loop filter components are C1 = 3300 pF, C2 = 270 pF, R1 = 4.12 kΩ; 4.65V ≤ VCn ≤ 5.25V; 0 ≤ Ta ≤ 70 °C.

| | | | | | | |
|---|---|---|---|---|---|---|
| Reference frequency | FIN | | 8 | | 20 | MHz |
| Output frequency | FOUT | | | | 108 | MHz |
| Output jitter | JFO | | -300 | | +300 | ps(RMS) |
| Output duty cycle | | 50% amplitude, FOUT = 108 MHz | 42 | | 58 | % |
| M counter value | | | 80 | | 255 | |
| N counter value | | | 18 | | 127 | |
| RR resistor value | | | 4.5 | | 5.25 | kΩ |
| VCO center frequency | TVCO | To = (4.01 E-10) (RR/M) + 2.4 nsec; VCA = 5.0V, RR = 4.75 kΩ, FLTR = 2.7V, M = 100, FIN = 20 MHz | 0.77 TVCO | TVCO | 1.23 TVCO | ns |
| VCO dynamic range | | 1V < FLTR < VCA-0.5 FOUT = 108 MHz, VCn = 5.0V | ±25 | | ±45 | % |
| VCO control gain | KVCO | $\omega i = 2\pi/TVCO$ | 0.14ωi | | 0.26ωi | rad/s V |
| Phase detector gain | KD | $K_D$ = (4.39E-3) x M/RR | | $K_D$ | | A/rad |

### CONTROL DACs

| | | | | | |
|---|---|---|---|---|---|
| Differential linearity (monotonicity) | DACF, I, P, S 0 ≤ Ta ≤ 70 °C 4.75V ≤ VCA ≤ 5.25V | -1LSB | | | |
| DACF output accuracy | VCA = 5.0V | 0.97I DACF | | 1.03I DACF | A |
| | Rx = 2.74 kΩ | -3/4LSB | | +3/4LSB | |
| | IR = VR3/(4 x Rx) | | | | |
| Rx resistor value | 2.5 | | | 3.0 | kΩ |
| DACF output resistance | | | | 3.7 | kΩ |

**CONTROL DACs** (continued)

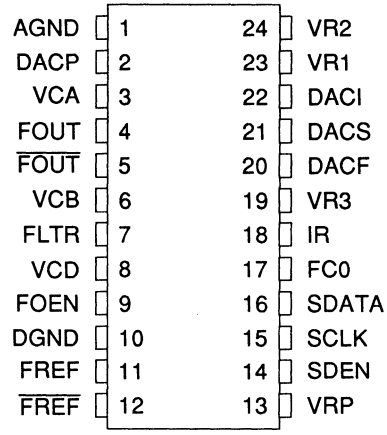
| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| DACI output accuracy | VCA = 5.0V | 0.95I DACI | | 1.05I DACI | A |
| | RR = 4.75 kΩ | -3/4LSB | | +3/4LSB | |
| DACI/F output voltage | | | | 2 | V |
| DACP output accuracy | VCA = 5.0V | 0.97V DACP | | 1.04V DACP | V |
| | RR = 4.75 kΩ | -3/4LSB | | +3/4LSB | |
| | VR3 = 2.2V | -25 mV | | +25 mV | |
| | VRP = 3.6V | | | | |
| DACP output range | | VCA-VR3 | | VCA-0.9 | V |
| DACP output resistance | | 50 | | 200 | Ω |
| VRP input voltage | | (VCA -VR3) + 0.2 | | VCA -1.0 | V |
| VRP input current | 2.0V ≤ VRP ≤ VCA | | | 20 | μA |
| DACS output accuracy | VCA = 5.0V | 0.97I DACS | | 1.03I DACS | V |
| | | -3/4LSB | | +3/4LSB | |
| | | -15 mV | | +15 mV | |
| DACP output range | | 0.1 | | 2.4 | V |
| DACS output resistance | | | | 3.7 | kΩ |
| VR3 input voltage | | 2.0 | | 2.4 | V |
| VR3 input current | VR3 = 2.2V | | | 1.0 | mA |

**SERIAL PORT TIMING**

| | | | | | |
|---|---|---|---|---|---|
| SCLK period | | 100 | | | ns |
| SDEN Setup wrt first SCLK falls | | 25 | | | ns |
| SDEN Hold wrt last SCLK falls | | 25 | | | ns |
| SDEN falls wrt next SCLK rise | | 25 | | | ns |
| SDATA Setup/Hold wrt SCLK falls | | 25 | | | ns |

## PACKAGE PIN DESIGNATIONS

(Top View)




**24-Pin SO/VSOP**

CAUTION: Use handling procedures necessary for a static sensitive component.

**Advance Information:** Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.



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**Notes:**

Section 5

# READ CHANNEL COMBINATION DEVICES

# STORAGE PRODUCTS REFERENCE

| Device Number | Data Rate | Power Supply | Compatibility | Device Functions | | | Process | Package | Power (typical) |
|---|---|---|---|---|---|---|---|---|---|
| | | | | ENDEC | Servo | Filter Fc | | | |
| **READ CHANNEL COMBINATION DEVICES** | | | | | | | | | |
| 32P548* | 12 Mbit/s | 5V | 32P5482 | No | "A, B, PES" | None | Bipolar | 52 QFP | 750 mW |
| 32P5482* | 16 Mbit/s | 5V | 32P548 | No | "A, B, PES" | None | Bipolar | 52 QFP | 350 mW |
| 32P4720A* | 18 Mbit/s | 5V | None | "1,7" | Rectified | None | Bipolar | 52 QFP | 700 mW |
| 32P4730 | 24 Mbit/s | 5V | 32P4744 and 32P4330 | "1,7" | "A-B, C-D" | 3 - 9 MHz | BiCMOS | 64 TQFP | 450 mW |
| 32P4731 | 24 Mbit/s | 5V | 32P4741 and 32P4331 | "1,7" | "A,B,C,D" | 3 - 9 MHz | BiCMOS | 64 TQFP | 450 mW |
| 32P4733 | 24 Mbit/s | 5V | 32P4743 and 32P4333 | No | "A,B" | 3 - 9 MHz | BiCMOS | 64 TQFP | 400 mW |
| 32P4741 | 40 Mbit/s | 5V | 32P4731 and 32P4331 | "1,7" | "A,B,C,D" | 6 - 18 MHz | BiCMOS | 64 TQFP | 500 mW |
| 32P4742 | 48 Mbit/s | 5V | 32P4731/41** | "1,7" | "A,B,C,D" | 8 - 24 MHz | BiCMOS | 64 TQFP | 500 mW |
| 32P4743 | 48 Mbit/s | 5V | 32P4733 and 32P4333 | No | "A,B" | 8 - 24 MHz | BiCMOS | 64 TQFP | 450 mW |
| 32P4744 | 40 Mbit/s | 5V | 32P4730 and 32P4330 | "1,7" | "A-B, C-D" | 6 - 18 MHz | BiCMOS | 64 TQFP | 500 mW |
| 32P4330 | 24 Mbit/s | 3 to 5.5V | 32P4730 and 32P4744 | "1,7" | "A-B, C-D" | 3 - 10 MHz | BiCMOS | 64 TQFP | 330 mW |
| 32P4331 | 24 Mbit/s | 3 to 5.5V | 32P4731 and 32P4741 | "1,7" | "A,B,C,D" | 3 - 10 MHz | BiCMOS | 64 TQFP | 330 mW |
| 32P4333 | 24 Mbit/s | 3 to 5.5V | 32P4733 and 32P4743 | No | "A,B" | 3 - 10 MHz | BiCMOS | 64 TQFP | 300 mW |

Unless otherwise noted, all devices include AGC, filter, pulse qualifiers, servo capture, data synchronizer, and time base generator.

*Does not include filter, time base generator, or control DACs.

**Not pin-to-pin compatible.

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# SSI 32P4731/41
## Read Channel with 1,7 ENDEC, 4-burst Servo

**Advance Information**

January 1993

## DESCRIPTION

The SSI 32P4731/41 devices are high performance BiCMOS single chip read channel ICs that contain all the functions needed to implement a complete zoned recording read channel for hard disk drive systems. Functional blocks include the pulse detector, programmable filter, 4-burst servo capture, time base generator, and data separator with 1,7 RLL ENDEC. Data rates can be programmed using an internal DAC whose reference current is set by a single external resistor.

Programmable functions of the SSI 32P4731/41 devices are controlled through a bi-directional serial port and banks of internal registers. This allows zoned recording applications to be supported without changing external component values from zone to zone.

The SSI 32P4731/41 utilize an advanced BiCMOS process technology along with advanced circuit design techniques which result in high performance devices with low power consumption.

## FEATURES

GENERAL:
- DAC controlled programmable data rates
  - 32P4731 - 8 to 24 Mbit/s
  - 32P4741 - 14 to 40 Mbit/s
- Complete zoned recording application support
- Low power operation -
  - 32P4731 - 400 mW typical @ 5V
  - 32P4741 - 500 mW typical @ 5V
- Bi-directional serial port for register access
- Register programmable power management (Sleep mode <1 mW)
- Power supply range (4.5 to 5.5 volts)
- Small footprint 64-pin TQFP package

PULSE DETECTOR:
- Fast attack/decay modes for rapid AGC recovery
- Dual rate charge pump for fast transient recovery
- Low Drift AGC hold circuitry
- Temperature compensated, exponential control AGC
- Wide bandwidth, high precision full-wave rectifier
- Dual mode pulse qualification circuitry (user selectable)
- TTL $\overline{\text{RDIO}}$ signal output for servo timing support
- Internal LOW-Z and fast decay timing
- 0.5 ns max. pulse pairing

SERVO CAPTURE:
- 4-burst servo capture with A, B, C, D outputs
- Internal hold capacitors
- Programmable charge current (4-Bit DAC)
- Separate registers for FC and VTH during servo mode
- 4-bit DAC for AGC level control (0.75 to 1.0 Vpp)

PROGRAMMABLE FILTER:
- Programmable cutoff frequency
  - 32P4731 - 3 to 9 MHz
  - 32P4741 - 5 to 18 MHz
- Programmable boost/equalization of 0 to 13 dB
- Matched normal and differentiated outputs
- ± 10% *fc* accuracy
- ± 2% maximum group delay variation
- Less than 1% total harmonic distortion
- Low-Z input switch
- No external filter components required

TIME BASE GENERATOR:
- Better than 1% frequency resolution
- Up to 75 MHz frequency output
- Independent M and N divide-by registers
- VCO center frequency matched to data synchronizer VCO

DATA SEPARATOR:
- Fast acquisition phase lock loop with zero phase restart technique
  - 32P4731 - 3 x VCO
  - 32P4741 - 1.5 x VCO
- Integrated 1,7 RLL Encoder/Decoder
- Fully integrated data separator
  - No external delay lines or active devices required
  - No external active PLL components required
- Programmable decode window symmetry control via serial port
  - Window shift control ± 30% (4-bit)
  - Includes delayed read data and VCO clock monitor points
- Programmable early/late write precomp (3-Bits each)

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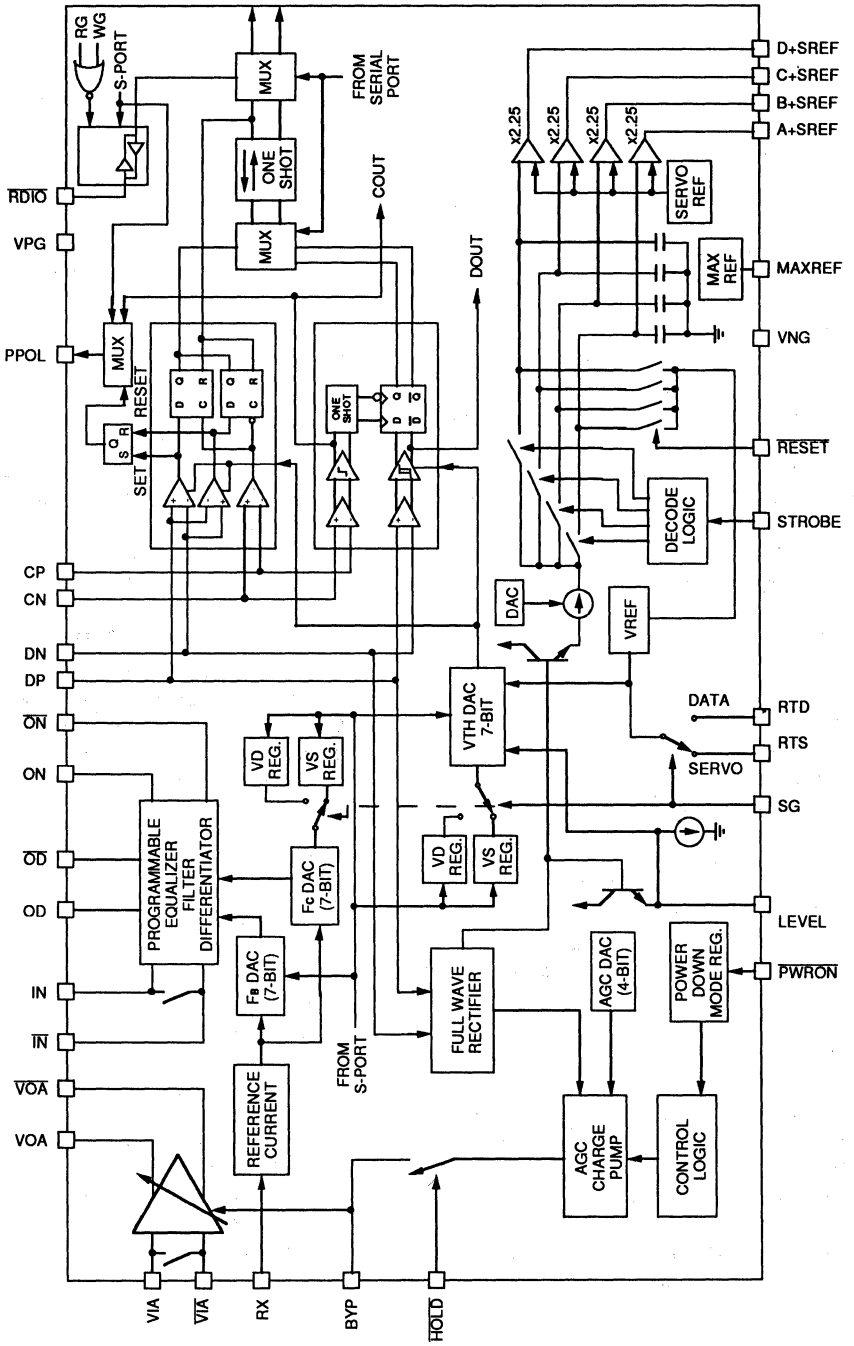


**FIGURE 1(a): 32P4731/41 Block Diagram**

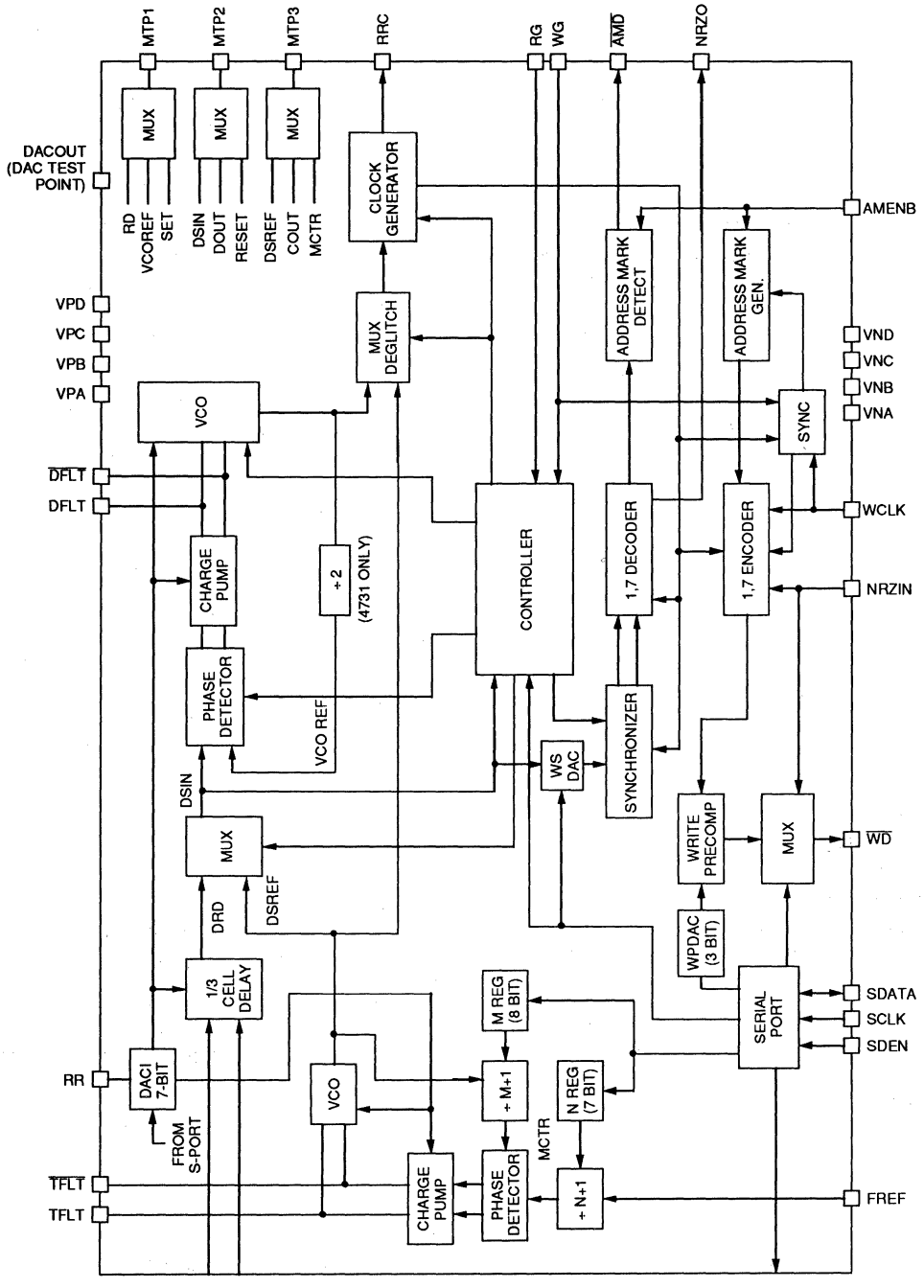


FIGURE 1(b): 32P4731/41 Block Diagram

## FUNCTIONAL DESCRIPTION

The SSI 32P4731/41 implement a high performance complete read channel, including pulse detector, 4-burst servo capture, programmable active filter, time base generator, and data separator with 1,7 RLL ENDEC, at data rates up to 40 Mbit/s (32P4741). A circuit block diagram is shown in Figure 1.

### Pulse Detector Circuit Description

The pulse detector, in conjunction with the programmable filter, provides all the data processing functions necessary for detection and qualification of encoded read signals. The signal processing circuits include a wide band variable gain amplifier; a wide bandwidth, high precision fullwave rectifier; and a dual rate charge pump. The entire signal path is fully-differential to minimize external noise pick up.

### AGC Circuit

The gain of the AGC amplifier is controlled by the voltage ($V_{BYP}$) stored on the BYP hold capacitor ($C_{BYP}$). A dual rate charge pump drives $C_{BYP}$ with currents that depend on the instantaneous differential voltage at the DP/DN pins. Attack currents lower $V_{BYP}$ which reduces the amplifier gain, while decay currents increase $V_{BYP}$ which increases the amplifier gain. When the signal at DP/DN is greater than 100% of the programmed AGC level, the nominal attack current of 0.18 mA is used to reduce the amplifier gain. If the signal is greater than 125% of the programmed AGC level, a fast attack current of eight (8) times nominal is used to reduce the gain. This dual rate approach allows AGC gain to be quickly decreased when it is too high yet minimizes distortion when the proper AGC level has been acquired.

A constant decay current of 4 µA increases the amplifier gain when the signal at DP/DN is less than the programmed AGC level. The large ratio (0.18 mA:4 µA) of the nominal attack and nominal decay currents enables the AGC loop to respond to the peak amplitudes of the incoming read signal rather than the average value. A fast decay current mode is provided to allow the AGC gain to be rapidly increased to reduce the recovery time between mode switches.

### AGC Mode Control

When write gate (WG) is driven high, the dual rate charge pump is disabled causing the AGC amplifier gain to be held constant. The input impedance of both the AGC amplifier and the programmable filter is reduced. When the WG pin transitions from high to low, the Low-Z mode is activated. In this mode, the input impedance at both the AGC amplifier and the programmable filter remain low to allow for quick recovery of the AC coupling capacitors. Directly following the Low-Z mode is the fast decay mode which allows rapid acquisition of the proper AGC level. In fast decay mode, an internal FET is switched on to drive a high current into the BYP pin. The current remains active until the signal at DP/DN is above 125% of the nominal amplitude, or until an internal timer expires. The duration of both the Low-Z and fast decay modes is internally set at a nominal 1 µs. Fast decay mode is also triggered by a transition of the servo gate (SG) pin in either direction. When the pulse detector is powered-down, $V_{BYP}$ will be held constant subject to leakage currents only. Upon power-up, the Low-Z/fast decay sequence is executed to rapidly recover from any transients or drift which may have occurred on the BYP hold capacitor.

External control for enabling the dual rate charge pump is also provided. Driving the $\overline{HOLD}$ pin low forces the dual rate charge pump output current to zero. In this mode, $V_{BYP}$ will be held constant subject only to leakage currents.

### $\overline{RDIO}$ Output Pin

A CMOS compatible inverted Read Data I/O ($\overline{RDIO}$) is provided to monitor the pulse detector output. This pin will be held high when SG is low and either RG or WG are high to reduce noise and accompanying jitter during read or write modes. Its falling edge indicates the occurrence of valid data pulse.

### Qualifier Selection

The 32P4731/41 provide both hysteresis and dual comparator pulse qualification circuits that may be independently selected for read mode and servo mode operation. For read mode operation the pulse qualifier method is selected by setting the MSB in the data threshold control register (DTCR). The lower 7 bits of the DTCR also set the hysteresis level of the comparators for read mode. For servo mode operation the pulse qualifier method is selected by setting the MSB in the servo threshold control register (STCR). The lower 7 bits of the STCR set the hysteresis level of the comparators for servo mode.

### Dual Comparator Qualification

When in dual comparator mode, independent positive and negative threshold qualification comparators are

used to suppress the error propagation of a positive and negative threshold hysteresis comparator. However a slight amount of hysteresis is included to increase the comparator output time when a signal that just exceeds the threshold level is detected. This eases the timing with respect to the zero crossing clock comparator. A differential comparator with programmable hysteresis threshold allows differential signal qualification for noise rejection. The programmable hysteresis threshold, $V_{TH}$, is driven by a multiplying DAC which is driven by the LEVEL voltage and referenced to VRC. Hysteresis thresholds from 10 to 80% may be set with a resolution of better than 1%. A parallel R-C network of RTD and CT sets the hysteresis threshold time constant when not in the Servo mode. A qualified signal zero crossing at the CP-CN inputs triggers the output one shot, Figure 2(a).

### Hysteresis Comparator Qualification

When the hysteresis qualification mode is selected, the same threshold qualification comparators and clock comparators are used to implement a polarity checking rule. In this mode, a positive peak that clears the established threshold level will set the hysteresis comparator and trigger the bidirectional one-shot that creates the read data pulses. In order to get another pulse clocked out, a peak of the opposite polarity must clear the negative threshold level to reset the hysteresis comparator and trigger the bidirectional one-shot. Figure 2(b).

### Servo Demodulator Circuit Description

The 32P4731/41 servo sections capture four separate servo bursts and provide A, B, C, and D burst outputs. Internal burst hold capacitors are provided to support low leakage burst capture and reduce external component count. To support embedded servo applications, the 32P4731/41 provides additional programming registers that set the filter cutoff frequency ($fc$) and the hysteresis threshold level (VTH) for servo mode. When SG is activated or deactivated there is a maximum 1.5 µs settling time for the internal DACs to recover from the register switching.

### Servo Mode Operation

When the servo gate (SG) is asserted, the control DACs for $fc$ and $V_{TH}$ switch from the data mode registers to the servo mode registers and the AGC goes into the fast decay mode. In addition, filter boost is disabled (as determined by the boost control bit), the AGC level is adjusted according to the AGC Level DAC and the RTS servo time constant setting resistor is connected to VRC (VRC is the internal bandgap reference.) By disabling the boost and providing the

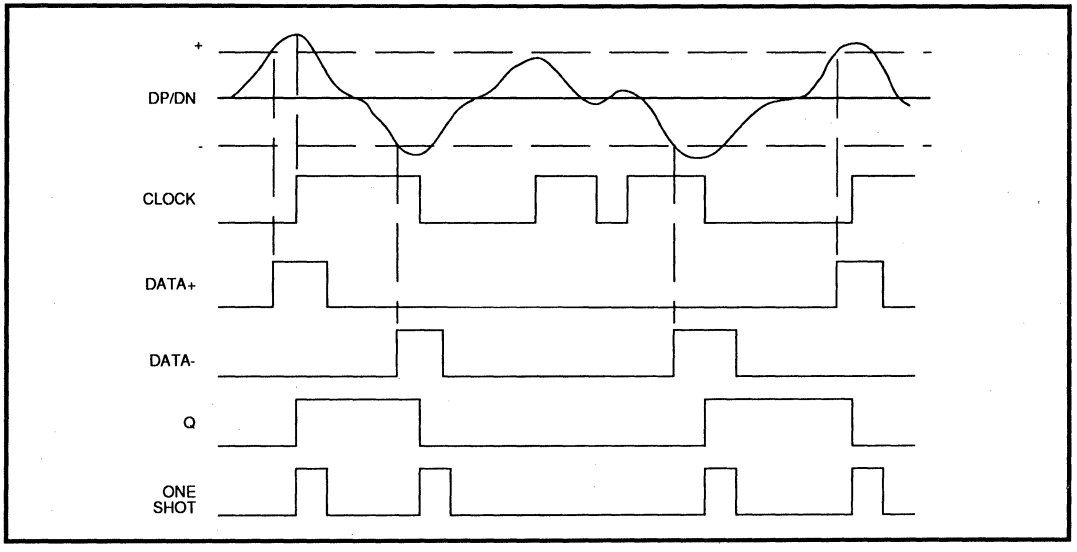


**FIGURE 2(a): Dual Comparator Timing Diagram**

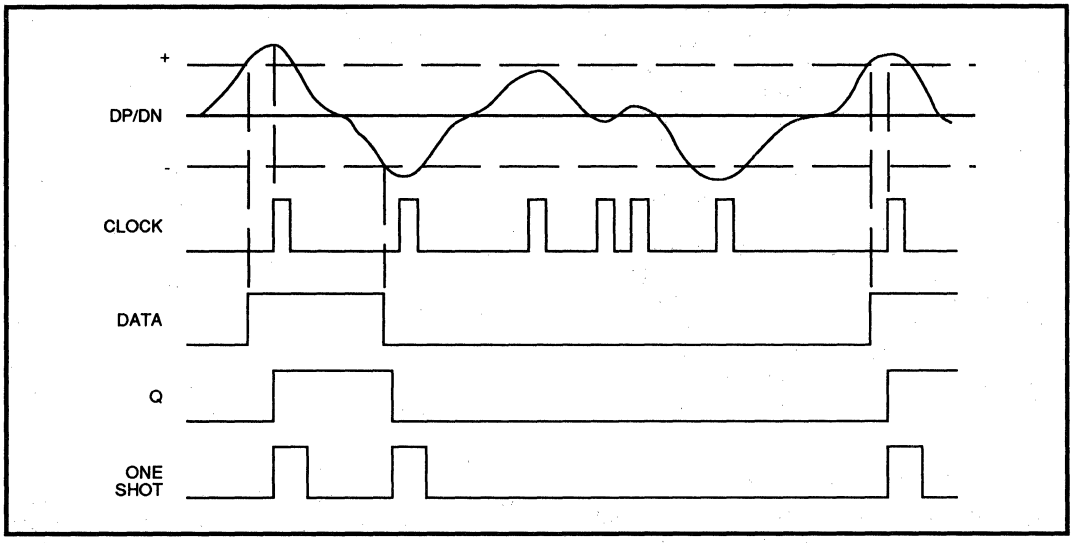


**FIGURE 2(b): Hysteresis Comparator Timing Diagram**

## FUNCTIONAL DESCRIPTION (continued)

servo control register for *fc* the servo signal to noise ratio can be greatly improved. When SG is activated or deactivated there is a maximum 1.5 µs settling time for the internal DACs to recover from the register switching. During servo mode, the AGC circuit remains active. A 4-bit DAC (DACA) is used to set the AGC level over a range of 0.75 to 1.00 Vpp as follows:

VAGC = 1.00 - (DACA x 0.01667) Vpp
where DACA is the value of the AGC Level register

Typically, a servo preamble is used to achieve the desired AGC level and then the $\overline{\text{HOLD}}$ pin is asserted to hold the AGC gain. When SG goes low to terminate the servo mode, the AGC goes into the Fast Decay mode for 1.0 µs to allow for fast transition into the read mode.

### Burst Capture

Burst capture is controlled by a single external pin designated STROBE and an internal counter. When SG is active, the first pulse on the STROBE pin gates the output of the servo peak detector to the A burst hold capacitor. The capacitor charges for as long as the STROBE pulse is high. On the falling edge of the STROBE signal, the internal counter is incremented. The next STROBE pulse will then gate the servo peak detector output to the B burst hold capacitor. Again, the capacitor charges for as long as the STROBE pulse is high. On the falling edge of STROBE, the counter is incremented again and the C burst is captured on the next STROBE pulse. On the next falling edge of STROBE, the counter is incremented again and the D burst is captured on the next STROBE pulse. After the falling edge of the fourth STROBE pulse, the counter is reset to zero and the burst capture process can be repeated. The internal counter is also reset when the SG pin is deactivated. The voltage level on the hold capacitors are buffered and amplified to generate the servo output signals. A 1.0 Vp-p differential voltage at the DP/DN pins will result in a 2.25V peak burst amplitude. The servo output signals (A, B, C, D) are referenced above an internal baseline of 0.5 volts. The output voltage at the MAXREF pin is a nominal 3.0V, and represents the maximum voltage to which the servo signal outputs will swing. It is typically used as the reference voltage for an external A/D converter. MAXREF is internally reduced to a 0.5 volt level, and establishes the servo zero-signal baseline. All four internal burst hold capacitors are discharged when the $\overline{\text{RESET}}$ pin is driven low. When the PKRESET bit is set high, the capacitors are reset below the 0.5 volt baseline. When PKRESET bit is low, the capacitors are reset to the 0.5 volt baseline.

The drive current of the servo peak detector charge pump is set by a 4-bit word (DACP) addressed through the serial port. The LSB value is 6 µA, and the offset is 1 LSB such that "0000" corresponds to 6 µA and "1111"results in 96 µA. Maximum noise immunity is obtained in the servo peak detector by choosing the smallest value of charge current to charge the internal 10 pF hold capacitor during the burst acquisition time.

### Timing Outputs

To support servo timing recovery, the pulse detector section provides a CMOS output of the servo information via the $\overline{\text{RDIO}}$ pin. A negative pulse is generated for each servo peak that is qualified through the pulse detector circuitry. Additional servo timing information is supported by the PPOL output. The PPOL pin provides pulse polarity information for the qualified peaks, where a high level TTL output indicates a positive pulse. To reduce noise progagation, $\overline{\text{RDIO}}$ and PPOL will not toggle when either RG or WG are active.

### PROGRAMMABLE FILTER CIRCUIT DESCRIPTION

The SSI 32P4731/41 programmable filter consist of an electronically controlled low-pass filter with a separate differentiated low-pass output. A seven-pole, low-pass filter is provided along with a single-pole, single-zero differentiator. Both outputs have matched group delays (< 1 ns typical.) A fixed delay of 1.25 ns (typ.) is added to the differentiated outputs to guarantee set-up timing in the data qualifier circuit. The delay matching is unaffected by any amount of programmed equalization or bandwidth. Programmable bandwidth and boost/ equalization is provided by internal 7-bit control DACs. Differentiation pulse slimming equalization is accomplished by a two-pole, low-pass with a two-pole, high-pass feed forward section to provide complimentary real axis zeros. A variable attenuator is used to program the zero locations. The filter implements a 0.05 degree equiripple linear phase response.

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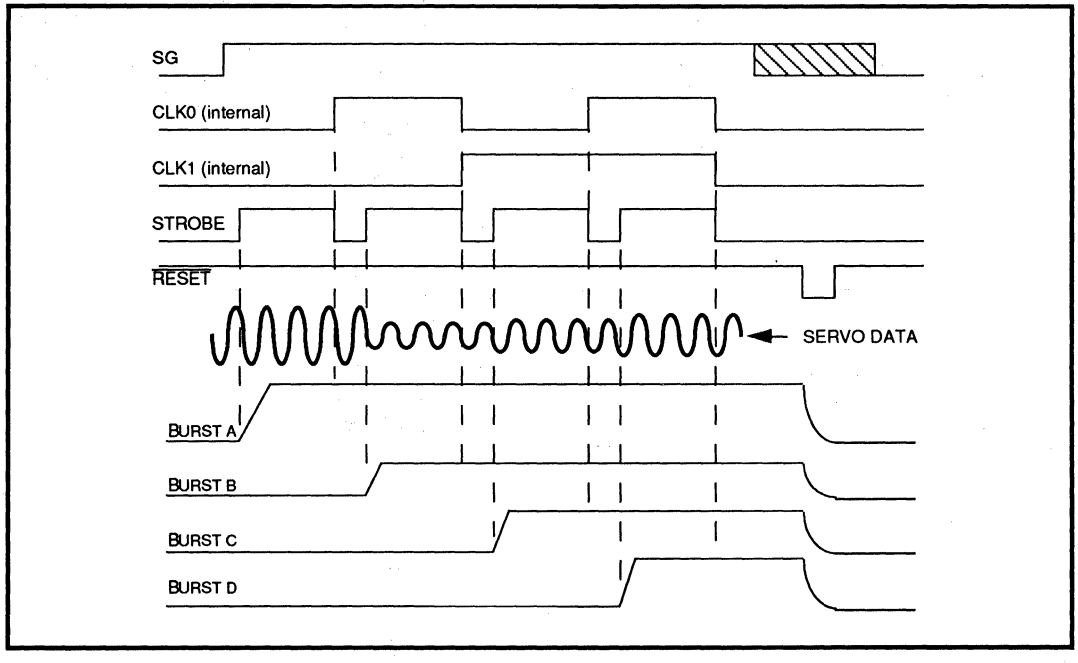


**FIGURE 3: Servo Capture Timing**

## FUNCTIONAL DESCRIPTION (continued)

The normalized transfer functions (i.e., $\omega c = 2\pi fc = 1$) are:

$$Vnorm/Vi = [(-Ks^2 + 17.98016)/D(s)] \times An$$

and

$$Vdiff/Vi = (Vnorm/Vi) \times (s/0.86133) \times Ad$$

Where D (s)=

$(s^2+1.68495s+1.31703)(s^2+1.54203\ s+2.95139)(s^2+1.14558s+5.37034)(s+0.86133)$,

An and Ad are adjusted for a gain of 2 at fs=(2/3)$fc$.

### Filter Operation

AC coupled differential signals from the AGC amplifier are applied to the IN/$\overline{IN}$ inputs of the filter. To improve settling time of the coupling capacitors, the IN/$\overline{IN}$ inputs are placed into a Low-Z state for 1.0 µs when WG goes inactive or when the $\overline{PWRON}$ pin is brought low. The programmable bandwidth and boost/equalization features are controlled by internal DACs and the registers programmed through the serial port. The current reference for both DACs is set using a single external resistor connected from pin RX to ground. The voltage at pin RX is proportional to absolute temperature (PTAT), hence the current for the DACs is a PTAT reference current.

### Bandwidth Control

The programmable bandwidth is set by the filter cutoff DAC. This DAC has two separate 7-bit registers that can program the DAC value as follows:

$fc$ = 0.0708 x DACF (MHz), for the 32P4731

$fc$ = 0.1417 x DACF (MHz), for the 32P4741

where DACF = DMCR or SMCR value

In the data mode, the Data Mode Cutoff Register (DMCR) is used to determine the filter's 3 dB cutoff frequency. In the servo mode, the Servo Mode Cutoff Register (SMCR) is used. Switching of the registers is controlled by the servo gate (SG) pin. The filter cutoff set by the internal DAC is the unboosted 3 dB frequency. When boost/equalization is added, the actual 3 dB point will move out. Table 1 provides information on boost verses 3 dB frequency.

### Boost/Equalization Control

The programmable equalization is also controlled by an internal DAC. The 7-bit Filter Boost Control Register (FBCR) determines the amount of equalization that will be added to the 3 dB cutoff frequency, as follows:

Boost = 20 log [(0.0273 x FBCR) + 1] (dB)

For example, with the DAC set for maximum output (FBCR = 7F or 127) there will be 13 dB of boost added at the 3 dB frequency. This will result in +10 dB of signal boost above the 0 dB baseline. When SG is active the boost can be disabled by setting bit 7 in FBCR. When bit 7 is "0" and SG is active the boost will automatically be set to 0 dB. If bit 7 is "1" the boost will remain at its programmed value regardless of the state of SG.

### Time Base Generator Circuit Description

The time base generator, which is a PLL based circuit, provides programmable reference frequency FOUT. The frequency can be programmed with an accuracy

**TABLE 1: 3 dB Cutoff Frequency versus Boost Magnitude**

| BOOST (dB) | $fc$ Multiplier | BOOST (dB) | $fc$ Multiplier |
|---|---|---|---|
| 0 | 1.00 | 7 | 2.42 |
| 1 | 1.21 | 8 | 2.51 |
| 2 | 1.50 | 9 | 2.59 |
| 3 | 1.80 | 10 | 2.66 |
| 4 | 2.04 | 11 | 2.73 |
| 5 | 2.20 | 12 | 2.80 |
| 6 | 2.32 | 13 | 2.88 |

better than 1%. An external passive loop filter is required to control the PLL locking characteristics. The filter is fully-differential and balanced in order to suppress common mode noise.

In Read, Write and Idle modes, the time base generator is programmed to provide a stable reference frequency (FOUT) for the data synchronizer. In Write and Idle modes, FOUT is the output of the time base generator. In Read mode FOUT is disabled after the data synchronizer has achieved lock and switched over to read data as the source for the RRC. This minimizes jitter in the data synchronizer PLL. The reference frequency is programmed using the M and N registers of the time base generator via the serial port, and is related to the external reference clock input, FREF, as follows:

$$FOUT = ((M+1)/(N+1))FREF$$

The VCO center frequency and the phase detector gain of the time base generator are controlled by an internal DAC addressed through the data recovery control register (DRCR). This DAC also sets the 1/3 cell delay, VCO center frequency, and phase detector gain for the data synchronizer circuitry.

$$Fvco = [12.5/(RR+0.4)] \times [(0.622 \times IDAC) + 4.27] \text{ MHz}$$

where IDAC is the value in the DRCR and RR is the value (kΩ) of the external RR resistor.

## DATA SEPARATOR CIRCUIT DESCRIPTION

The data separator circuit provides complete encoding, decoding, and synchronization for RLL 1,7 format data. In the Read mode, the circuit performs sync field search and detect, data synchronization, address mark detection, and data decoding. In the Write mode, the circuit provides address mark generation, data encoding, and write precompensation for NRZ data applied to the NRZIN pin. Data rate is established by the time base generator and DACI. The DAC generates a reference current which sets the VCO center frequency, the phase detector gain, and the 1/3 cell delay.

### Phase Locked Loop

The circuit employs a dual mode phase detector; harmonic in the Read mode and non-harmonic in the Write and Idle modes. In the read mode the harmonic phase detector updates the PLL with each occurrence of a $\overline{DRD}$ pulse. In the Write and Idle modes the non-harmonic phase detector is continuously enabled, thus maintaining both phase and frequency lock onto the reference frequency of the internal time base generator. By acquiring both phase and frequency lock to the input reference frequency and utilizing a zero phase restart technique, the VCO transient is minimized and false lock to DLYD DATA is eliminated. The phase detector incorporates a charge pump in order to drive the loop filter directly. The polarity and width of the output current pulses correspond to the direction and magnitude of the phase error.

The data synchronizer also requires an external passive loop filter to control its PLL locking characteristics. This filter is also fully-differential and balanced in order to suppress common mode noise.

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### READ/WRITE MODE CONTROL

The read gate (RG) and write gate (WG) inputs control the device operating mode. RG is an asynchronous input and may be initiated or terminated at any position on the disk. WG is also an asynchronous input, but should not be terminated prior to the last output write data pulse.

### Read Mode

The data synchronizer utilizes a fully integrated fast acquisition PLL to accurately develop the decode window. Read gate (RG) initiates the PLL locking sequence and selects the PLL reference input; a high level (read mode) selects the internal $\overline{DRD}$ signal and a low level selects the reference clock. In the read mode the falling edge of $\overline{DRD}$ enables the phase detector while the rising edge is phase compared to the rising edge of the VCO reference (VCOR.) As depicted in Figure 5, $\overline{DRD}$ is a 1/3 cell wide (TVCO) pulse whose leading edge is defined by the falling edge of $\overline{RD}$. A decode window is developed from the VCOR clock.

### Read Mode Soft Sector Operation

In soft sector operation the address mark must be detected before RG can be asserted to continue read mode operation. Soft sector operation is entered by driving the AMENB pin high to initiate an address mark search function. An address mark pattern consists of two 8T patterns followed by two 12T patterns. The address mark detect circuit searches the internal read data ($\overline{RD}$) for the address mark pattern. First the address mark detect circuit looks for a 6 "0's" within the 8T patterns. Having detected a 6 "0's" the address mark detect circuit then looks for a 9 "0's" within the 12T

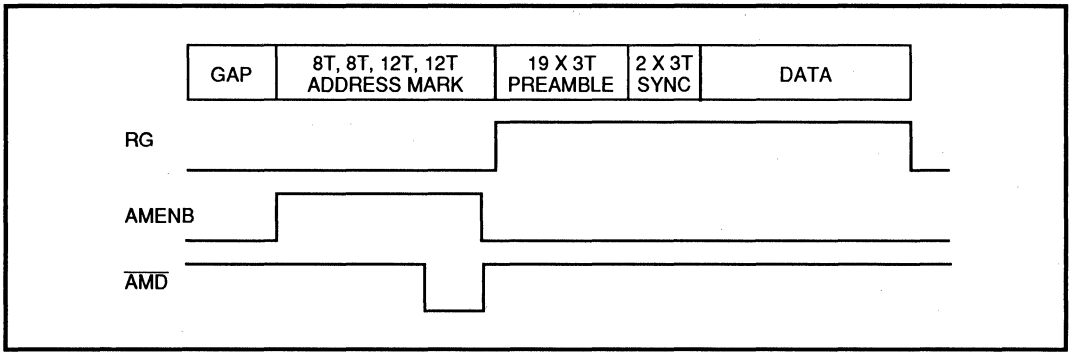



**FIGURE 4: Read Mode Soft Sector Operation**

## FUNCTIONAL DESCRIPTION (continued)

patterns. If the 9 "0's" pattern is not detected within 5 $\overline{RD}$ bits after detecting the 6 "0's" pattern, the address mark detect sequence will reset and look for a 6 "0's" pattern again. When the address mark detect circuit has acquired a 6 "0's", 9 "0's" sequence the $\overline{AMD}$ output transitions low. $\overline{AMD}$ will remain low until the AMENB input is driven low. Reference Figure 4.

### Preamble Search

After the address mark (AM) has been detected, RG can be asserted to initiate the preamble search. When RG is asserted, an internal counter is triggered to count positive transitions of the internal read data, RD. Once the counter reaches count 3 (3 consecutive 3T patterns detected) the internal read gate is enabled. This switches the phase detector reference from the internal time base to the delayed read data ($\overline{DRD}$) signal. At the same time an internal zero phase restart signal restarts the VCO in phase with the $\overline{DRD}$. This prepares the VCO to be synchronized to data when the bit sync circuitry is enabled after VCO lock is established.

### VCO Lock and Bit Sync Enable

One of two VCO locking modes will be entered depending on the state of the gain shift (GS) bit, or bit 1, in the Control B register. If GS = "1", the phase detector will enter a gain shift mode of operation. The phase detector starts out in a high gain mode of operation to support fast phase acquisition. After an internal counter counts the first 14 transitions of the internal $\overline{DRD}$ signal, the gain is reduced by a factor of 3. This reduces the bandwidth and damping factor of the loop by $\sqrt{3}$ which provides improved jitter performance in the data follow mode. The counter continues to count the next 4 $\overline{DRD}$ transitions (a total of 19 x 3T from assertion of RG) and then asserts an internal VCO lock signal. The VCO lock signal activates the decoder bit synchronization circuitry to define the proper decode boundaries. The next 2 x 3T patterns are used to set the proper decode window so that VCO is in sync with RRC and RRC is in sync with the data. Following this, the NRZ output is enabled and the data is toggled through the decoder for the duration of the RG.

When the VCO lock signal is asserted, the internal RRC source is also switched from the time base generator to the VCO clock signal that is phase locked to $\overline{DRD}$. During the internal RRC switching period the external RRC signal may be held for a maximum of 2 NRZ clock periods, however no short duration glitches will occur.

When the GS bit is set to "0" the phase detector gain shift function is disabled. The VCO lock sequence is identical to that of the gain shift mode explained above, except that no gain shift is made after the first 15 transitions.

### Split Field Servo Operation

The data separator circuit supports split field servo operation. For soft sector operation, the AMENB pin is asserted only at the beginning of the data sector (see Figure 7.) Within the data sector and following the servo burst, it is not necessary to provide another address mark pattern.

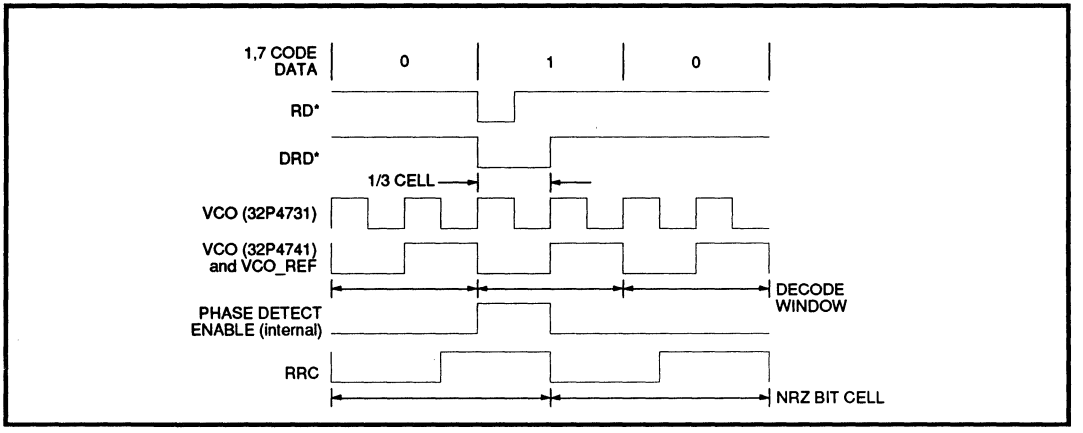



**FIGURE 5: Data Synchronization Waveform**

When SG goes low after the servo burst, the hard sector VCO lock sequence is automatically initiated. This reduces the overhead required.

### READ MODE HARD SECTOR OPERATION

The hard sector operation is entered by holding the AMENB pin low. In hard sector operation, $\overline{AMD}$ remains inactive and the address mark search sequence is not entered. The hard sector read operation starts with assertion of the RG. Once read gate is asserted the VCO lock sequence is identical to the soft sector operation.

### Window Shift

Shifting the phase of the VCO clock effectively shifts the relative position of the $\overline{DRD}$ pulse within the decode window. Decode window control is provided via the WS control bits of the Window Shift Control Register (WSCR). Further description of the WSCR will follow.

### Non-Read Mode

In the non-Read modes, the PLL is locked to the reference clock. This forces the VCO to run at a frequency which is very close to that required for tracking actual data. When the reference input to the PLL is switched, the VCO is stopped momentarily, then restarted in an accurate phase alignment with the next PLL reference input pulse. By minimizing the phase alignment error in this manner, the acquisition time is substantially reduced.

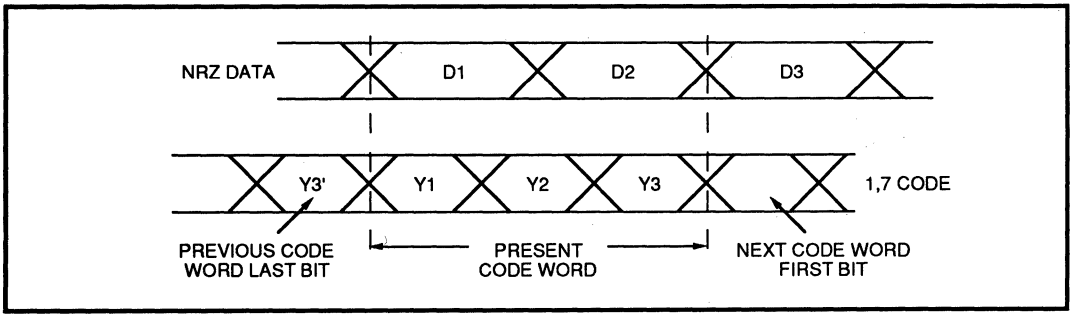



**FIGURE 6: NRZ Data Word to 1, 7 Code Word Bit Comparision**
(Reference Table 4 for decode scheme)

## FUNCTIONAL DESCRIPTION (continued)

### Write Mode

In the Write mode the circuit converts NRZIN data from the controller into 1,7 RLL formatted data for storage on the disk. In soft sector operation the circuit generates an address mark and a preamble pattern. In hard sector operation the circuit generates the preamble pattern but no preceding address mark. Write mode is entered by asserting WG while the RG is held low. During Write mode the VCO and the RRC are referenced to the internal time base generator signal, FOUT.

### Write Mode Soft Sector Operation

In soft sector operation an address mark pattern is written prior to the preamble and encoded data. To initiate the soft sector mode the AMENB is asserted 1 NRZ period after WG is asserted. Once AMENB is asserted, the address mark pattern of two 8T patterns followed by two 12T patterns is automatically generated. Following the address mark pattern, 3T patterns will be generated as long as the NRZIN data is held low. While the address mark and preamble are being written the encoder is active. Therefore, WCLK must be toggling and NRZIN must be held low ("0".) The first non zero NRZIN input bit indicates the end of the preamble pattern. After a delay of 5 NRZIN bit time periods, non-preamble data begins to toggle out of $\overline{WD}$. At the end of the write cycle, 5 bits of blank NRZ time passes to insure the encoder is flushed of data before the WG can be transitioned low. $\overline{WD}$ stops toggling a maximum of 2 NRZ (RRC) time periods after WG goes low. Reference Figures 9 and 12 for detailed timing information.

### Write Mode Hard Sector Operation

In hard sector operation AMENB is held low and no address mark pattern is generated. The preamble pattern is generated in the same sequence as the soft sector operation. During preamble generation the WCLK is toggled and NRZIN data is held low ("0".) Termination of a hard sector write operation follows the same sequence as soft sector mode.

### Direct Write Function

The 32P4731/41 includes a Direct Write (DW) function that allows the NRZIN data to bypass the encoder and write precomp circuitry. When the DW bit is set in the CBR, the data applied to NRZIN will bypass the encoder and write precomp and directly control the WD output buffer. This allows the user to perform DC erase and media tests.

### Operating Modes and Control

The 32P4731/41 has several operating modes that support read, write, servo, and power management functions. Mode selection is accomplished by controlling the read gate (RG), write gate (WG), servo gate (SG), and $\overline{PWRON}$ pins. Additional modes are also controlled by programming the Power Down Control Register (PDCR), the Control A (CAR) register, and the Control B (CBR) register via the serial port.

### External Mode Control

For normal operation the $\overline{PWRON}$ pin is driven low. During normal operation the 32P4731/41 is controlled by the read gate (RG), write gate (WG), and servo gate (SG) pins. (Reference Table 2.)

### Control Registers

Control registers CAR and CBR allow the user to configure the 32P4731/41 test points for evaluation of different internal signals and also control other device functions. CAR controls functions of the pulse detector, filter, and time base generator. CBR controls test points and functions of the data separator.

### Power Down Control

For power management, the $\overline{PWRON}$ pin can be used in conjunction with the Power Down Control Register (PDCR) to set the operating mode of the device. The PDCR provides a control bit for each of the functional blocks. When the $\overline{PWRON}$ pin is brought high ("1") the device is placed into Sleep mode (<5 mW) and all circuits are powered down except the serial port. This allows the user to program the serial port registers while still conserving power. Register information is retained during the Sleep mode so it is not necessary to reprogram the serial port registers after returning to an Active mode. When the $\overline{PWRON}$ pin is driven low ("0"), the contents of the PDCR determine which blocks will be active. Register mapping for the PDCR is shown in Table 3. To improve recovery time from the Sleep mode, the inputs to the AGC, Filter and DP/DN are placed into a Low-Z mode for 1 µs.

Following the Low-Z mode the AGC is placed into the fast decay mode.

### Serial Interface Operation

The serial interface is a bi-directional port for reading and writing programming data from/to the internal registers of the 32P4731/41. For data transfers SDEN is brought high, serial data is presented at the SDATA pin, and a serial clock is applied to the SCLK pin. After the SDEN goes high, the first 16 pulses applied to the SCLK pin will shift the data presented at the SDATA pin into an internal shift register on the rising edge of each clock. An internal counter prevents more than 16 bits from being shifted into the register. The data in the shift register is latched when SDEN goes low. If less than 16 clock pulses are provided before SDEN goes low, the data transfer is aborted.

All transfers are shifted into the serial port LSB first. The first byte of the transfer is address and instruction information. The LSB of this byte is the R/W bit which determines if the transfer is a read (1) or a write (0). The remaining 7-bits determine the internal register to be accessed. Table 3 provides register mapping information. The second byte contains the programming data. In read mode (R/W = 1) the 32P4731/41 will output the register contents of the selected address. In write mode the device will load the selected register with data presented on the SDATA pin. At initial power-up, the contents of the internal registers will be in an unknown state and they must be programmed prior to operation. During power down modes, the serial port remains active and register programming data is retained. Detailed timing information is provided in Figure 13(b) and in the electrical specifications.

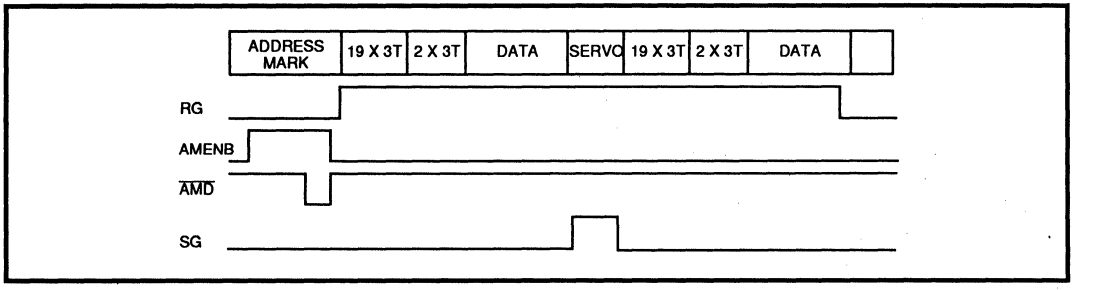



**FIGURE 7: Split Field Servo Operation**

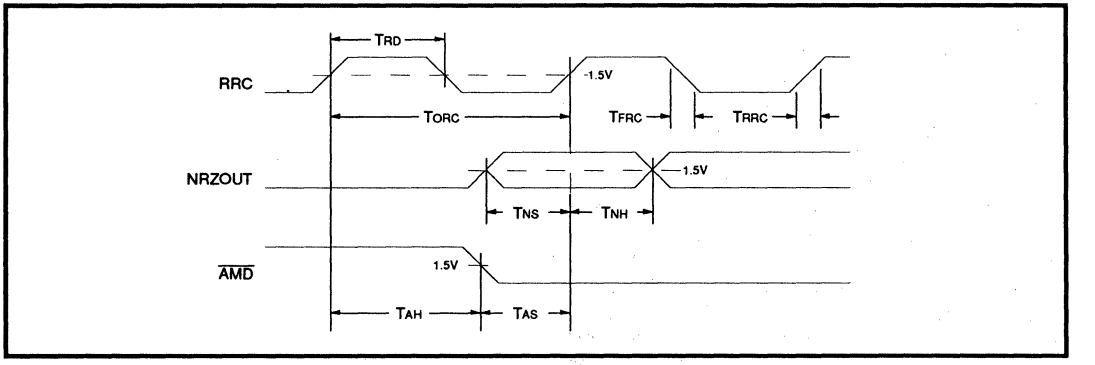



**FIGURE 8: NRZ Read Timing**

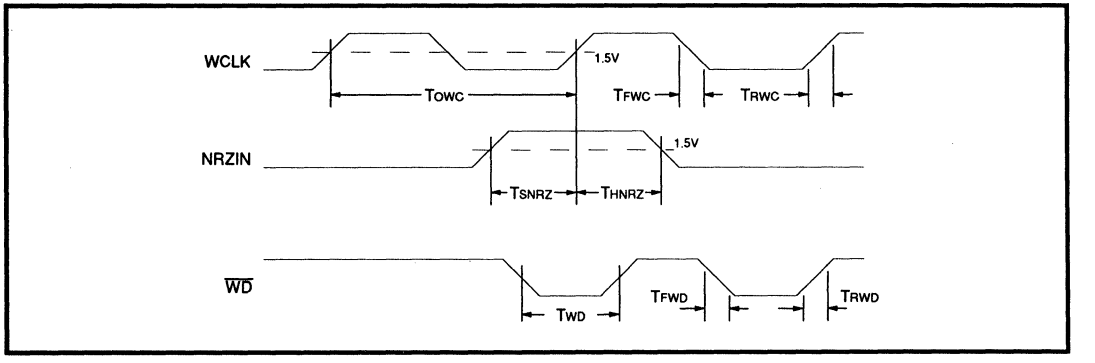



**FIGURE 9: $\overline{WD}$ and NRZ Write Timing**

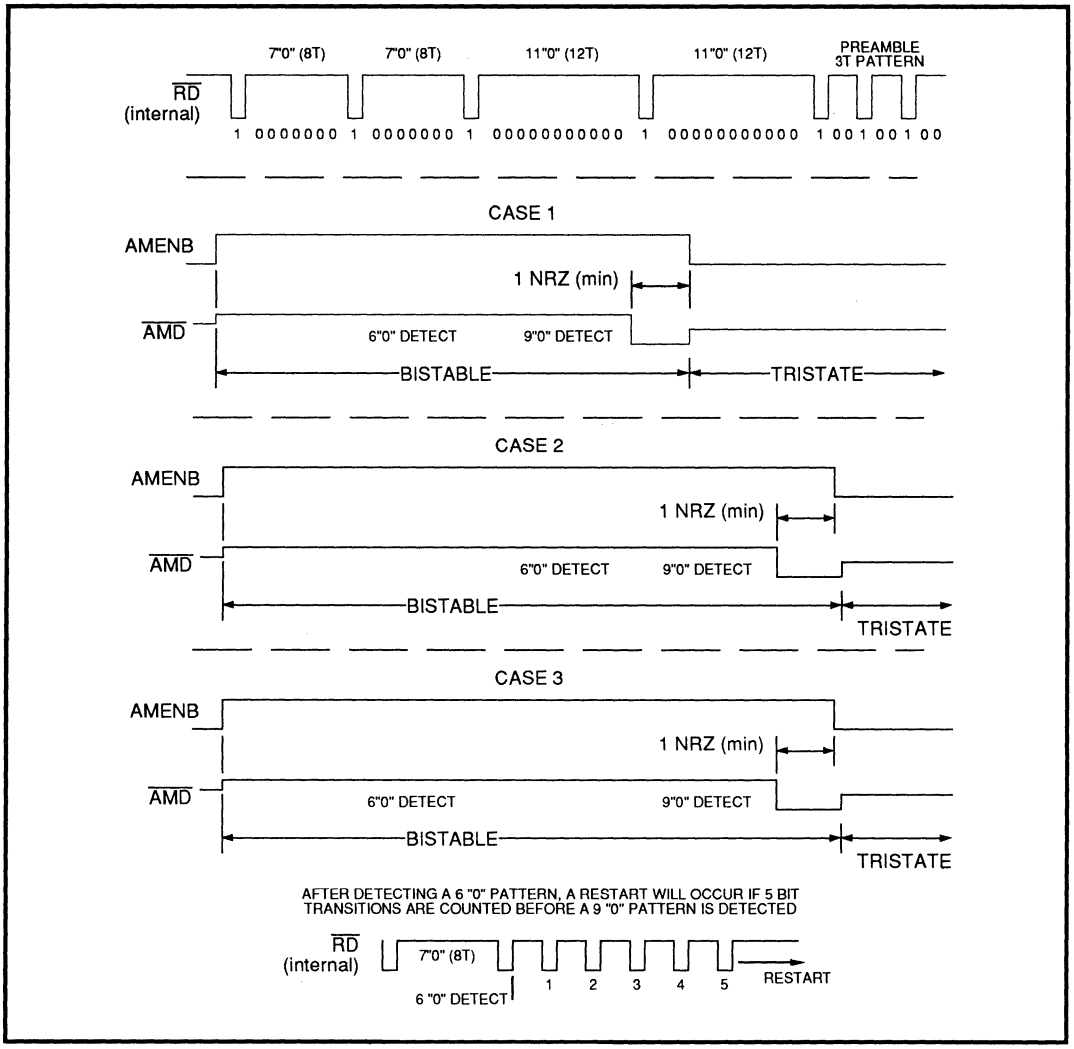



**FIGURE 10: Address Mark Search (Soft Sector)**

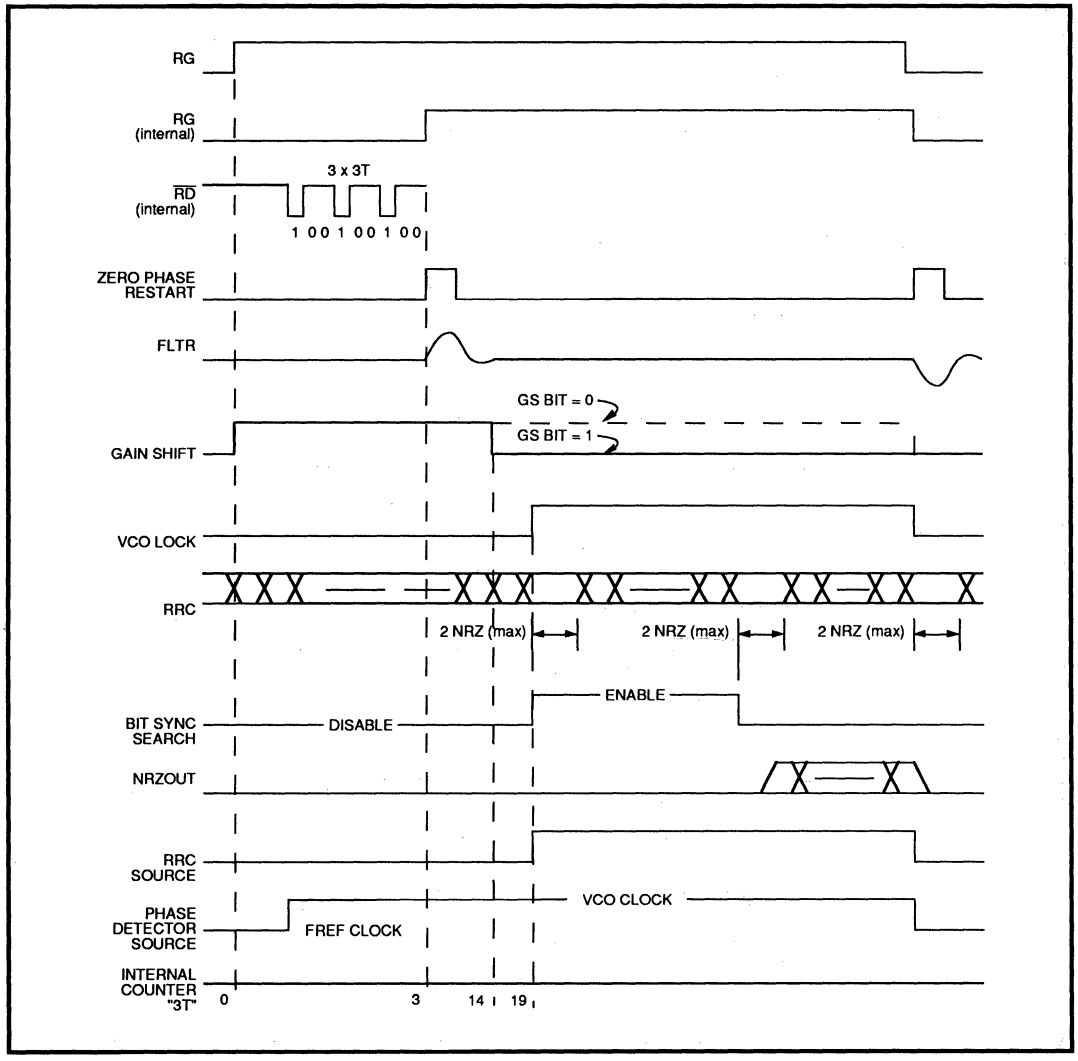



**FIGURE 11: Read Mode Locking Sequence (Hard and Soft Sector)**

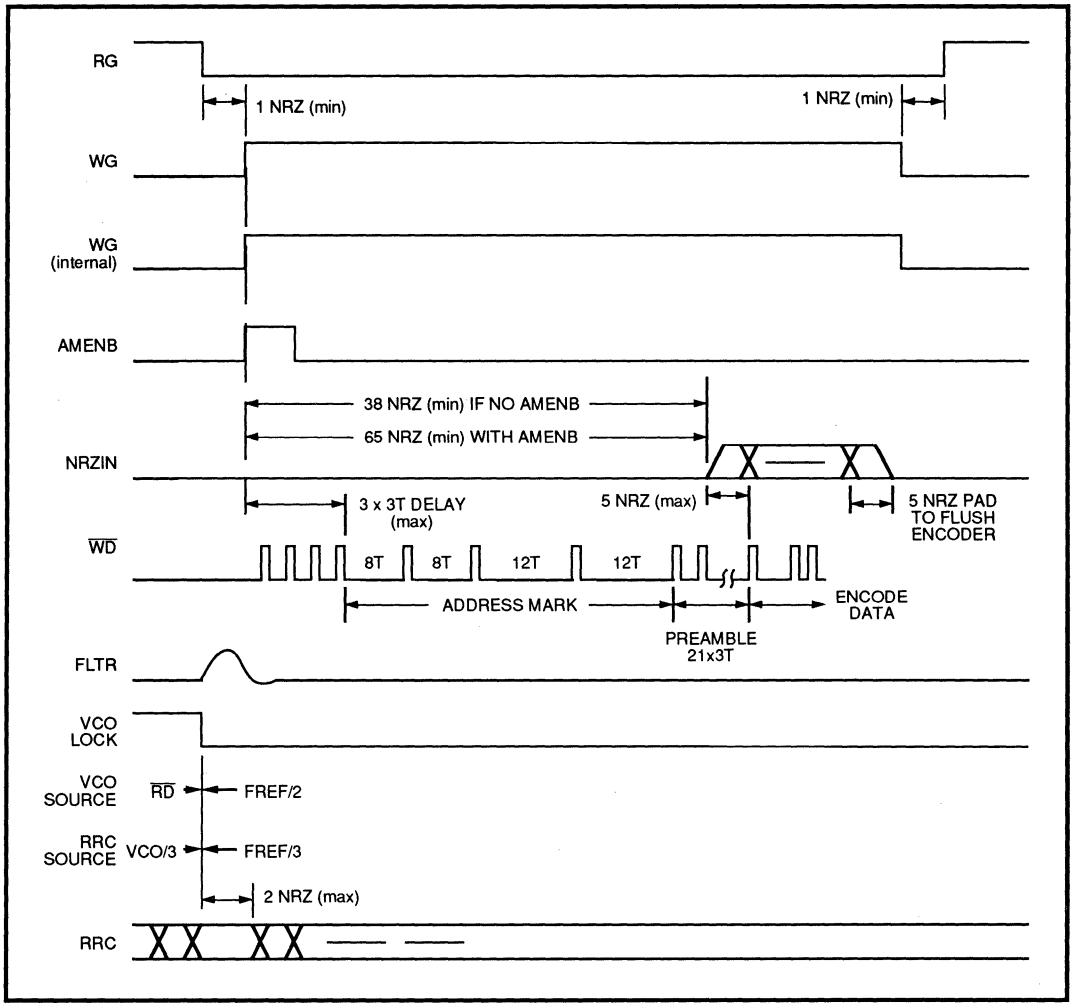



**FIGURE 12: Write Data Operation (Hard and Soft Sector)**

**TABLE 2: Mode Control Table**

| CONTROL LINES | | | | DEVICE MODE: | DAC CONTROL | | | |
|---|---|---|---|---|---|---|---|---|
| $\overline{PWRON}$ | RG | SG | WG | | VTH | FC | BOOST | AGC LEVEL |
| 1 | X | X | X | **SLEEP MODE:** All functions are powered down. The serial port registers remain active and register programming data is saved. | off | off | off | off |
| 0 | 0 | 0 | 1 | **WRITE MODE:** The pulse detector is inactive. The data synchronizer VCO is locked to the internal time base generator. Write precomp circuit is clocked by internal time base. $\overline{RDIO}$ and PPOL are inactive. | DR | DR | DR | DR |
| 0 | 1 | 0 | X | **READ MODE:** The pulse detector is active. The data synchronizer begins the preamble lock sequence. $\overline{RDIO}$ and PPOL are inactive. | DR | DR | DR | DR |
| 0 | X | 1 | X | **SERVO MODE:** The pulse detector is active and the servo control registers are enabled for the Fc DAC and the VTH DAC. $\overline{RDIO}$ and PPOL are active. The data synchronizer and time base generator can be disabled using the PDCR. | SR | SR | off | SR |
| 0 | 0 | 0 | 0 | **IDLE MODE:** The contents of the PDCR determine which blocks are powered-up. In normal operation with all blocks powered-up, the pulse detector is active, the data synchronizer VCO is locked to the time base generator, and the data control registers are used for VTH and FC. | DR | DR | DR | DR |
| | | | | If multiple control signals are active, the priority order will be PWRON, SG, RG, and WG. For example, if SG and RG are both "1", the servo mode will be active. | | | | |

DAC CONTROL Key: DR = data register, SR = servo register, off = disabled

| REGISTER NAME | A6 | | | ADDRESS | | | A0 | R/W | D7 | | | DATA BIT MAP | | | | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| POWER DOWN CONTROL | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | -- | -- | -- | TBG 1=DISABLE 0=ENABLE | DATA SEP 1=DISABLE 0=ENABLE | FILTER 1=DISABLE 0=ENABLE | -- | PD/SERVO 1=DISABLE 0=ENABLE |
| DATA MODE CUTOFF | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | * | DAC BIT 6 | DAC BIT 5 | DAC BIT 4 | DAC BIT 3 | DAC BIT 2 | DAC BIT 1 | DAC BIT 0 |
| SERVO MODE CUTOFF | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | * | DAC BIT 6 | DAC BIT 5 | DAC BIT 4 | DAC BIT 3 | DAC BIT 2 | DAC BIT 1 | DAC BIT 0 |
| FILTER BOOST | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | SRVO BST 1=ENABLE 0=DISABLE | DAC BIT 6 | DAC BIT 5 | DAC BIT 4 | DAC BIT 3 | DAC BIT 2 | DAC BIT 1 | DAC BIT 0 |
| DATA THRESHOLD | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1=DUAL 0=HYS | DAC BIT 6 | DAC BIT 5 | DAC BIT 4 | DAC BIT 3 | DAC BIT 2 | DAC BIT 1 | DAC BIT 0 |
| SERVO THRESHOLD | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1=DUAL 0=HYS | DAC BIT 6 | DAC BIT 5 | DAC BIT 4 | DAC BIT 3 | DAC BIT 2 | DAC BIT 1 | DAC BIT 0 |
| CONTROL A | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | Fast Decay test mode 0=ENABLE | TMS1 | TMS0 | TBG 1=BYPASS 0=NORMAL | TBG TEST POINT ENABLE | PUMP DWN 1=TP ON 0=TP OFF | PUMP UP 1=TP ON 0=TP OFF | PHASE DET 1=ENABLE 0=DISABLE |
| CONTROL B | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | * | MTPE 1=ENABLE 0=DISABLE | PUMP DWN 1=TP ON 0=TP OFF | PUMP UP 1=TP ON 0=TP OFF | PHASE DET 1=ENABLE 0=DISABLE | RDI 1 = INPUT 0 = OUTPUT | GAIN SHFT 1 = ON 0 = OFF | DIR WRITE 1 = ON 0 = OFF |
| N COUNTER | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | * | N COUNT BIT 6 | N COUNT BIT 5 | N COUNT BIT 4 | N COUNT BIT 3 | N COUNT BIT 2 | N COUNT BIT 1 | N COUNT BIT 0 |
| M COUNTER | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | M COUNT BIT 7 | M COUNT BIT 6 | M COUNT BIT 5 | M COUNT BIT 4 | M COUNT BIT 3 | M COUNT BIT 2 | M COUNT BIT 1 | M COUNT BIT 0 |
| DATA RECOVERY | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | * | IDAC BIT 6 | IDAC BIT 5 | IDAC BIT 4 | IDAC BIT 3 | IDAC BIT 2 | IDAC BIT 1 | IDAC BIT 0 |
| WINDOW SHIFT | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | TDAC 1 | TDAC 0 | WIN SHFT 1=ENABLE 0=DISABLE | WS DIR 1=LATE 0=EARLY | WS3* | WS2* | WS1* | WS0* |
| WRITE PRECOMP | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | PK RESET 1=HI RES 0=NORMAL | WL2* | WL1* | WL0* | WR PRCMP 1=ENABLE 0=DISABLE | WE2* | WE1* | WE0* |
| AGC LEVEL | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | DACP BIT 3 | DACP BIT 2 | DACP BIT 1 | DACP BIT 0 | DAC BIT 3 | DAC BIT 2 | DAC BIT 1 | DAC BIT 0 |

***These bits are used only for testing. They should be programmed to 0 in actual operation.**

**TABLE 3: Serial Port Register Mapping**

**Control Register CA:**

| BIT | NAME | FUNCTION |
|---|---|---|
| 0 | EPDT | Enable Phase Detector (Time Base Generator): This bit disables the output of the phase detector to the VCO. An external voltage applied across the TFLT pins drives the VCO to a fixed frequency.<br>1 = Phase detector active<br>0 = Phase detector charge pump disabled |
| 1 | UT | Enable Pump Up Current (Time Base Generator): This bit enables a test mode for checking the charge pump output current. The charge pump will source a fixed DC current from TFLT and sink the current at $\overline{\text{TFLT}}$.<br>0 = No current<br>1 = Maximum charge pump current |
| 2 | DT | Enable Pump Down Current (Time Base Generator): This bit enables a test mode for checking the charge pump output current. The charge pump will source a fixed DC current from $\overline{\text{TFLT}}$ and sink the current at TFLT.<br>0 = No current<br>1 = Maximum charge pump current |
| 3 | ET | This bit enables the MTP3 test point output buffer.<br>0 = Test point disabled<br>1 = Test point enabled |
| 4 | BYPT | This bit enables a time base generator bypasses mode where the FREF input is connected to the phase detector input.<br>0 = Time base enabled<br>1 = Time base bypassed |
| 5/6 | TMS0/1 | These bits select the test point signal sources (refer to Table 7). |
| 7 | FDTM | This bit continuously enables the AGC fast decay current.<br>0 = Fast decay current always on<br>1 = Normal fast decay operation |

**Control Register CB:**

| | | |
|---|---|---|
| 0 | DW | This bit enables the direct write (Bypass ENDEC) function.<br>0 = Normal operation<br>1 = Bypass encoder, NRZ0 directly to WD/$\overline{\text{WD}}$ |
| 1 | GS | This bit enables the phase detector gain switching in read mode.<br>0 = Normal operation<br>1 = Gain shift after 14 x 3T (read mode only) |
| 2 | RDI | This bit enables the $\overline{\text{RDIO}}$ pin as an input<br>0 = $\overline{\text{RDIO}}$ is an output<br>1 = $\overline{\text{RDIO}}$ is an input |
| 3 | EPDD | Enable Phase Detector (Data Separator): This bit disables the output of the phase detector to the VCO. An external voltage applied across the DFLT pins drives the VCO to a fixed frequency.<br>1 = Phase detector active<br>0 = Phase detector charge pump disabled |

**Control Register CB:** (continued)

| BIT | NAME | FUNCTION |
|---|---|---|
| 4 | UD | Enable Pump Up Current (Data Separator): This bit enables a test mode for checking the charge pump output current. The charge pump will source a fixed DC current from DFLT and sink the current at $\overline{DFLT}$.<br>0 = No current<br>1 = Maximum charge pump current |
| 5 | DD | Enable Pump Down Current (Data Separator): This bit enables a test mode for checking the charge pump output current. The charge pump will source a fixed DC current from $\overline{DFLT}$ and sink the current at DFLT.<br>0 = No current<br>1 = Maximum charge pump current |
| 6 | MTPE | This bit enables the multiplexed test points (MTP1, 2, 4)<br>0 = Test points disabled<br>1 = Test points enabled |
| 7 | – | Not used, must be programmed to 0. |

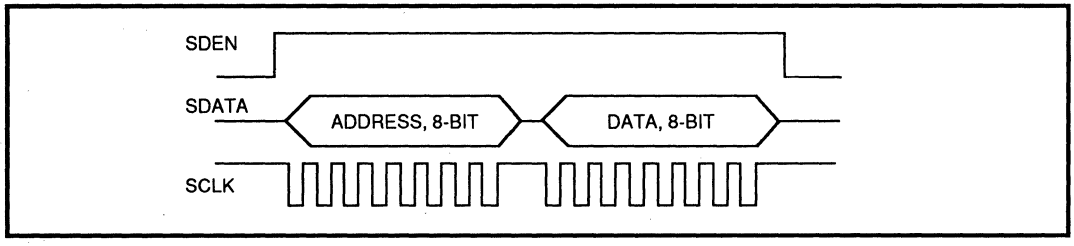



**FIGURE 13(a): Serial Port Data Transfer Format**

## PIN DESCRIPTION

### POWER SUPPLY PINS

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| VPA | - | Data separator PLL analog power supply pin. |
| VPB | - | Time base generator PLL analog power supply pin. |
| VPC | - | Internal ECL, CMOS logic power supply pin. |
| VPD | - | TTL buffer I/O digital power supply pin. |
| VPG | - | Pulse detector, filter, servo analog power supply pin. |
| VNA | - | Data separator PLL analog ground pin. |
| VNB | - | Time base generator PLL analog ground pin. |
| VNC | - | Internal ECL, CMOS logic ground pin. |
| VND | - | TTL buffer I/O digital ground pin. |
| VNG | - | Pulse detector, filter, servo analog ground pin. |

### INPUT PINS

| | | |
|---|---|---|
| VIA, $\overline{\text{VIA}}$ | I | AGC AMPLIFIER INPUTS: Differential AGC amplifier input pins. |
| DP, DN | I | ANALOG INPUTS FOR DATA PATH: Differential analog inputs to data comparators, full-wave rectifier. |
| CP, CN | I | ANALOG INPUTS FOR CLOCK PATH: Differential analog inputs to the clock comparator. |
| $\overline{\text{PWRON}}$ | I | Power Enable: CMOS compatible power control input. A low level CMOS input enables power to circuitry according to the contents of the PDCR. A high level CMOS input shuts down all circuitry. |
| $\overline{\text{HOLD}}$ | I | HOLD CONTROL: TTL compatible control pin which, when pulled low, disables the AGC charge pump and holds the AGC amplifier gain at its present value. |
| STROBE | I | BURST STROBE: TTL compatible burst strobe input. A high level TTL input will enable the servo peak detector to charge one of the burst capacitors. The falling edge of STROBE increments an internal counter that determines which burst capacitor will charge on the next STROBE pulse (reference Figure 3 for timing.) |
| $\overline{\text{RESET}}$ | I | RESET CONTROL INPUT: TTL compatible reset input. A low level TTL input will discharge the internal servo burst hold capacitors on channels A-D. |
| IN, $\overline{\text{IN}}$ | I | FILTER SIGNAL INPUTS: The AGC output signals must be AC coupled into these pins. |
| FREF | I | REFERENCE FREQUENCY INPUT: Frequency reference input for the time base generator. FREF may be driven either by a direct coupled TTL signal or by an ac coupled ECL signal. Pin FREF has an internal pull down resistor. |

**INPUT PINS** (continued)

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| AMENB | I | ADDRESS MARK ENABLE: TTL compatible input. A high level TTL input will enable the address mark generation circuitry in write mode and the address mark detect circuitry in read mode. |
| NRZIN | I | NRZ INPUT: TTL compatible write data NRZ input. This pin can be connected to the NRZO pin to form a bidirectional data port. Pin NRZIN has an internal pull up resistor. |
| RG | I | READ GATE: TTL compatible read gate input. A high level TTL input selects the RD input and enables the read mode/address mark detect sequences. A low level selects the FREF input. See Table 5. |
| SG | I | SERVO GATE: TTL compatible servo gate input. A high level TTL input activates the servo mode by selecting the servo control registers, the RDIO pin, and the RTS resistor. |
| WCLK | I | WRITE CLOCK: TTL compatible write clock input. Must be synchronous with the Write Data NRZ input. For short cable delays, WCLK may be connected directly to pin RRC. For long cable delays, WCLK should be connected to an RRC return line matched to the NRZ data bus line delay. |
| WG | I | WRITE GATE: TTL compatible write gate input. A high level TTL input enables the write mode. See Table 5. |

**OUTPUT PINS**

| | | |
|---|---|---|
| $\overline{\text{AMD}}$ | O | ADDRESS MARK DETECT: Address mark detect CMOS compatible output. Tristate output pin that is high impedance state when RG is low. When AMENB is high, this output indicates address mark search status. A low level output appears when an address mark has been detected. A low level on the AMENB pin resets $\overline{\text{AMD}}$. |
| MTP1,2,3 | O | MULTIPLEXED TEST POINTS: Open emitter ECL output test points. Internal test signals are routed to these test points as determined by the CAR and CBR. Two external resistors are required to use this pin. They should be removed during normal operation to reduce power dissipation. See Table 7. |
| NRZO | O | NRZ OUTPUT DATA: NRZ data CMOS compatible output. Tristate output pin that is in its high impedance state when RG is low. Read data output when RG is high. |
| OD, $\overline{\text{OD}}$ | O | DIFFERENTIAL DIFFERENTIATED OUTPUTS: Filter differentiated outputs. These outputs are AC coupled into the CP/CN inputs. |
| ON, $\overline{\text{ON}}$ | O | DIFFERENTIAL NORMAL OUTPUTS: Filter normal low pass output signals. These outputs are AC coupled into the DP/DN inputs. |
| PPOL | O | PULSE POLARITY: Pulse polarity CMOS compatible output. The output is high when the pulse being qualified is positive and it is low when the pulse being qualified is negative. |

## PIN DESCRIPTION (continued)

### INPUT PINS (continued)

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| $\overline{\text{RDIO}}$ | O | READ DATA I/O: Bi-directional CMOS pin. $\overline{\text{RDIO}}$ is an output when the SG is active or the RDI bit is low in the CBR. $\overline{\text{RDIO}}$ is an input when the RDIO bit is high in the CBR. The SG overrides the bit in the CBR. $\overline{\text{RDIO}}$ is high impedance when SG is low and RG or WG is high. |
| RRC | O | READ REFERENCE CLOCK: Read clock CMOS compatible output. During a mode change, no glitches are generated and no more than one lost clock pulse will occur. When RG goes high, RRC initially remains synchronized to FOUT. When the Sync Bits are detected, RRC is synchronized to the $\overline{\text{DRD}}$. When RG goes low, RCC is synchronized back to the FOUT. |
| VOA, $\overline{\text{VOA}}$ | O | AGC AMPLIFIER OUTPUT: Differential AGC amplifier output pins. These outputs are ac coupled into the filter inputs (IN/$\overline{\text{IN}}$). |
| $\overline{\text{WD}}$ | O | WRITE DATA: Encoded write data CMOS compatible output. The data is automatically resynchronized (independent of the delay between RRC and WCLK) to the FREF reference clock. When direct write is active $\overline{\text{WD}}$ is NRZIN data. |

### ANALOG PINS

| | | |
|---|---|---|
| A, B, C, D | - | SERVO OUTPUTS: These outputs are processed versions of the voltages captured on the servo hold capacitors. They are referenced to SREF. |
| BYP | - | The AGC integrating capacitor CBYP, is connected between BYP and VPG. |
| TFLT/$\overline{\text{TFLT}}$ | - | PLL LOOP FILTER: These pins are the connection points for the time base generator loop filter. |
| DACOUT | - | DAC VOLTAGE TEST POINT: This test point monitors the outputs of the internal DACs. The source DAC is selected by programming the two MSBs of the WSCR register:<br>TDAC1 TDAC0 DAC MONITORED<br>0 0 Filter $fc$ DAC<br>0 1 Qualifier threshold DAC (VTH)<br>1 0 Window shift DAC<br>1 1 Write precomp DAC |
| DFLT/$\overline{\text{DFLT}}$ | - | PLL LOOP FILTER: These pins are the connection points for the data separator loop filter. |
| LEVEL | - | An NPN emitter output that provides a full-wave rectified signal from the DP, DN inputs. An external capacitor should be connected from LEVEL to VPG to set the hysteresis threshold time constant in conjunction with RTS and RTD. An internal current source provides 50 µA of pull-down current at this pin. |
| RR | - | REFERENCE RESISTOR INPUT: An external 1% resistor is connected from this pin to ground to establish a precise internal reference current for the data separator and time base generator. |

**INPUT PINS** (continued)

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| RTS | - | SERVO TIME CONSTANT RESISTOR INPUT: An external resistor is connected from this pin to LEVEL to establish the hysteresis threshold time constant when in Servo mode. |
| RTD | - | DATA TIME CONSTANT RESISTOR INPUT: An external resistor is connected from this pin to LEVEL to establish the hysteresis threshold time constant when not in Servo mode. |
| RX | - | REFERENCE RESISTOR INPUT: An external 1% resistor is connected from this pin to VNG to establish a precise PTAT (proportional to absolute temperature) reference current for the filter. |
| MAXREF | - | SERVO REFERENCE: An external voltage output that can be used as the reference for an external A/D converter This represents the maximum output voltage for the A, B, C, and D outputs. |

**SERIAL PORT PINS**

| | | |
|---|---|---|
| SDEN | - | SERIAL DATA ENABLE: Serial enable CMOS compatible input. A high level input enables the serial port. |
| SDATA | - | SERIAL DATA: Serial data CMOS compatible input. NRZ programming data for the internal registers is applied to this input. |
| SCLK | - | SERIAL CLOCK: Serial clock CMOS compatible input. The clock applied to this pin is synchronized with the data applied to SDATA. |

## ELECTRICAL SPECIFICATIONS

Unless otherwise specified, the recommended operating conditions are as follows: 4.5V < POSITIVE SUPPLY VOLTAGE < 5.5V, 0°C < T (ambient) < 70°C, and 25°C < T(junction) < 135°C. Currents flowing into the chip are positive. Current maximums are currents with the highest absolute value.

### ABSOLUTE MAXIMUM RATINGS

Operation beyond the maximum ratings may damage the device

| PARAMETER | RATING |
|---|---|
| Storage Temperature | -65 to 150°C |
| Junction Operating Temperature | +135°C |
| Positive Supply Voltage (Vp) | -0.5 to 7V |
| Voltage Applied to any pin | -0.5V to Vp + 0.5V |

### POWER SUPPLY CURRENT AND POWER DISSIPATION

| PARAMETER | CONDITIONS | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| ICC (VPA, VPB, VPC, VPD, VPG) | Outputs and test point pins open | (32P4731) @ 24 Mb/s) | | 80 | | mA |
| | Ta = 27°C Vpn = 5.0 V | (32P4741) @ 40 Mb/s | | 100 | | mA |
| PWR Power Dissipation | Outputs and test point pins open, | (32P4731) @ 24 Mb/s | | 400 | | mW |
| | Ta = 27°C Vpn = 5.0 V | (32P4731) @ 40 Mb/s | | 500 | | mW |
| Sleep Mode Power | $\overline{\text{PWRON}}$ = 1 | | | | 1 | mW |
| Servo Mode Power | $\overline{\text{PWRON}}$ = 0 TBG Disabled Data Separator Disabled | | | 200 | | mW |

### DIGITAL INPUTS AND OUTPUTS

**TTL Compatible Inputs**

| | | | | | | |
|---|---|---|---|---|---|---|
| Input low voltage | VIL | | -0.3 | | 0.8 | V |
| Input high voltage | VIH | | 2.0 | | VPD+0.3 | V |
| Input low current | IIL | VIL=0.4V | | | -100 | µA |
| Input high current | IIH | VIH = 2.4V | | | 50 | µA |

**CMOS Compatible Inputs** - Schmitt trigger type, do not leave open. Nominal 1.0 V hysteresis around VPD/2.

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Input low voltage | | -0.3 | | 1.5 | V |
| Input high voltage | | 3.5 | | VPD+0.3 | |

**CMOS Compatible Outputs**

| | | | | | |
|---|---|---|---|---|---|
| Output low voltage | 5.0 V, 25 °C<br>IOL = 4.07 mA | | | 0.5 | V |
| Output high voltage | 5.0 V, 25 °C<br>IOH = -4.83 mA | 4.5 | | | V |
| Rise time | 4.5V, 70 °C, C =15 pF, 0.8 to 2.0V | | | 3.0 | ns |
| Fall time | 4.5V, 70 °C, C = 15 pF, 0.8 to 2.0V | | | 4.0 | ns |

**Test Point Output Levels (MTP1, MTP2, MTP3)**

| | | | | | |
|---|---|---|---|---|---|
| Output high level | 261Ω to VPA<br>402Ω to AGND<br>VPA = 5.0V | VPA-1.02 | | | V |
| Output low level | 261Ω to VPA<br>402Ω to AGND<br>VPA = 5.0V | | | VPA-1.62 | V |

**Serial Port**

| | | | | | | |
|---|---|---|---|---|---|---|
| SCLK period | $T_{CKL}$ | R/W Bit = 0 (Write) | 100 | | | ns |
| | | R/W Bit = 1 (Read) | 140 | | | ns |
| SCLK low time, | $T_{CKL}$ | R/W Bit = 0 (Write) | 40 | | | ns |
| | | R/W Bit = 1 (Read) | 60 | | | ns |
| SCLK high time, | $T_{CKH}$ | R/W Bit = 0 (Write) | 40 | | | ns |
| | | R/W Bit = 1 (Read) | 60 | | | ns |
| Enable to SCLK | $T_{SENS}$ | | 35 | | | ns |
| SCLK to disable | $T_{SENH}$ | | 100 | | | ns |
| Data set-up time | $T_{DS}$ | | 15 | | | ns |
| Data hold time | $T_{DH}$ | | 15 | | | ns |
| SDATA tri-state delay | $T_{SENDL}$ | | | | 50 | ns |
| SDATA turnaround time | $T_{TRN}$ | R/W Bit = 1 (Read) | 70 | | | ns |
| SDEN low time | $T_{SL}$ | | 200 | | | ns |
| SCLK to Valid Data | $T_{SKEW}$ | R/W Bit = 1 (Read) | | | 50 | ns |

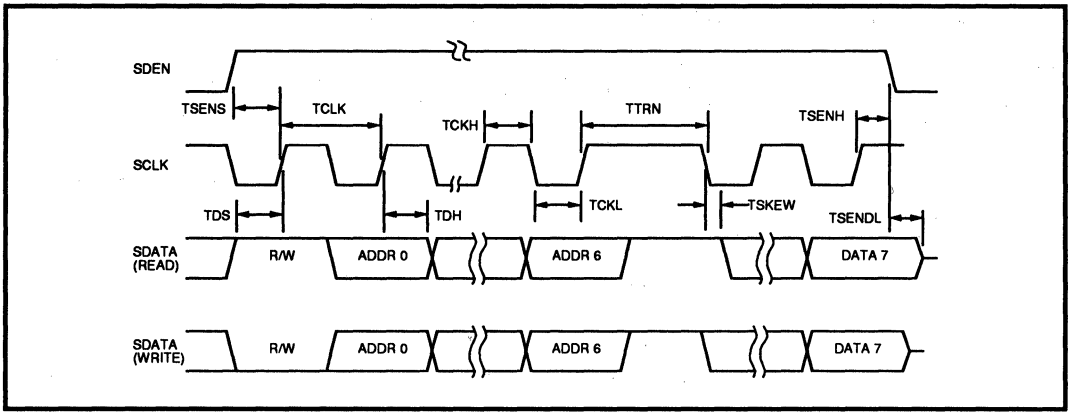



**FIGURE 13(b): Serial Port Timing Information**

## ELECTRICAL SPECIFICATIONS (continued)

### PULSE DETECTOR CHARACTERISTICS

**AGC Amplifier**

Input signals are AC coupled to VIA/$\overline{\text{VIA}}$, VOA/$\overline{\text{VOA}}$ outputs are AC coupled toIN/$\overline{\text{IN}}$, and ON/$\overline{\text{ON}}$ are AC coupled to DP/DN. A 1000 pF capacitor (CBYP) is connected from BYP to VPG. Unless otherwise specified, outputs are measured differentially at VOA/$\overline{\text{VOA}}$, FIN = 4 MHz, and filter boost = 0 dB.

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Input range | Filter boost = 0 dB | 22 | | 240 | mVpp |
| | Filter boost = 11 dB | 20 | | 100 | mVpp |
| DP-DN voltage | VIA-$\overline{\text{VIA}}$ = 0.1 Vpp | 0.90 | | 1.10 | Vpp |
| DP-DN voltage variation | 22 mV < VIA-$\overline{\text{VIA}}$ < 240 mV | | | 5 | % |
| Gain range | | 1.9 | | 22 | V/V |
| Gain sensitivity | BYP voltage change | | 28 | | dB/V |
| VOA-$\overline{\text{VOA}}$ dynamic range | THD = 1% max | 0.75 | | | Vpp |
| Differential input impedance | WG = low | 4.7 | 6.0 | 8.4 | kΩ |
| | WG = high; or Low-Z | | 350 | | Ω |
| Single-ended input impedance | WG = low | | 3.5 | | kΩ |
| | WG = high; or Low-Z | | 250 | | Ω |
| Output offset voltage variation | Gain = 1.9 to 22 | | | +200 | mV |
| Input noise voltage | Gain = 22, VIA/$\overline{\text{VIA}}$ shorted | | 10 | 15 | nV/√Hz |
| Bandwidth | Gain = 22 | 50 | | | MHz |
| CMRR | Gain = 22, $fc$ = 5MHz | 40 | | | dB |

**AGC Amplifier** (continued)

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| PSRR | Gain = 22, $fc$ = 5MHz | 45 | | | dB |
| Single-ended output resistance | | 150 | | Ω | |
| Gain decay time | VIA-$\overline{\text{VIA}}$ = 240 to 120 mV<br>VOA-$\overline{\text{VOA}}$ > 0.9 Final Value | | 50 | | µs |
| Gain attack time | VIA-$\overline{\text{VIA}}$ = 120 to 240 mV<br>VOA-$\overline{\text{VOA}}$ < 1.1 Final Value | | 1 | | µs |

**AGC Control**
The input signals are AC coupled into DN/DP, CBYP = 1000 pF to VPG. CT = 10000 pF, RTS = RTD = Open.

| | | | | | |
|---|---|---|---|---|---|
| DP-DN input range | For test only | | 1.0 | 1.5 | Vpp |
| Decay current | Normal decay ($I_D$) | | 4.0 | | µA |
| | Fast decay mode ($I_{DF}$) | | 1 | | mA |
| Attack current | Normal attack ($I_{CH}$) | | 0.18 | | mA |
| | Fast attack mode ($I_{CHF}$) | | 8 x ICH | | mA |
| BYP leakage current | WG = high | -10 | | 10 | nA |
| Low-Z duration | | | 1.0 | | µs |
| Fast decay duration | | | 1.0 | | µs |
| LEVEL output gain | \|DP-DN\| = 0.5 to 1.5V | 0.65 | 0.70 | 0.75 | V/Vpp |
| LEVEL output bandwidth | -1dB | 10 | | | MHz |
| LEVEL offset voltage | Output - $V_{RTS}$ or $V_{RTD}$, $I_L$ = 50 µA | | | 30 | mV |
| Internal LEVEL pull-down current | | 40 | 50 | 60 | µA |

**Data Comparator**
The input signals are AC coupled into DP/DN.

| | | | | | |
|---|---|---|---|---|---|
| DP-DN input range | | 0.5 | 1.0 | 1.5 | Vpp |
| Differential input resistance | WG = low | 7.0 | | 13.0 | kΩ |
| Single ended input resistance | WG = high | | 500 | | Ω |
| Threshold voltage hysteresis | | | .2XT% | | % |
| Threshold (T%) accuracy | 30% ≤ T% ≤ 80%<br>0.3 < Level - $V_{RTH}$ < 0.75<br>T% = $V_{THDAC}$ • 0.93/127 | T%-5 | T% | T%+5 | % |
| Minimum threshold voltage | LEVEL-VRC < 0.1V<br>$V_{THMIN}$ = $V_{\overline{THDAC}}$ 97.6%/127 | | $V_{THMIN}$ | | V |

## ELECTRICAL SPECIFICATIONS (continued)

**Clock Section**
The input signals are AC coupled into CP/CN.

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Comparator offset voltage | | -4.0 | | 4.0 | mV |
| Differential input resistance | | 7.0 | | 13.0 | kΩ |
| Pulse pairing | Sine wave into DP/DN<br>Phase shift 90° into CP/CN<br>$V_{SINE}$ = 1 Vpp, $F_{SINE}$ = 4 MHz | | | 0.5 | ns |

**SERVO CAPTURE CHARACTERISTICS**

| | | | | | |
|---|---|---|---|---|---|
| MAXREF output voltage | $I_{SOURCE}$ = 0 mA | 2.85 | 3.00 | 3.15 | V |
| MAXREF load regulation | $I_{SOURCE}$ = 0 to 4.5 mA | | | 20 | mV |
| A, B, C, D output low voltage | $I_{SINK}$ = 0.2 mA<br>$\overline{RESET}$ = 0V (low) | 0.47 | 0.50 | 0.53 | V |
| A, B, C, D output clip level | $I_{SOURCE}$ = 0.2 mA | VPG-1.2 | | | V |
| MAXREF-A,B,C,D high voltage | 22 mVpp ≤ VIA-$\overline{VIA}$<br>≤ 240 mVpp<br>AGC loop closed | 0 | | | V |
| A, B, C, D output impedance | $I_{SOURCE/SINK}$ = 0.2 mA | | | 50 | Ω |
| A, B, C, D gain | From DP/DN pins | 2.20 | 2.25 | 2.30 | V/V |
| Peak detector hold droop | STROBE = 0 V | -1 | 0 | +1 | mV/µs |
| Channel to channel amplitude mismatch | DP-DN = 1.0 Vpp<br>Sinewave at 4 MHz | -15 | | 15 | mV |
| Peak detector acquisition to 99% | DP-DN = 1.0 Vpp sinewave<br>Fs ≤ 6.7 MHz, DACP = 1000 | | | 800 | ns |
| Peak detector reset time to 1% | $\overline{RESET}$ = 0<br>DACP = 1000 | | | 300 | ns |
| $\overline{RESET}$ turn-on delay | From $\overline{RESET}$ fall @ 1.2V | | | 50 | ns |
| $\overline{RESET}$ turn-off delay | From $\overline{RESET}$ rise @ 1.2V | | | 50 | ns |
| $\overline{RDIO}$ pulse width | $C_L$ = 15 pF 32P4741 | 10 | | 15 | ns |
| | 32P4731 | 23 | | 47 | ns |
| $\overline{RDIO}$ turn-on delay | From WG or RG↓ | | | 150 | ns |
| $\overline{RDIO}$ turn-off delay | From WG or RG↑ | | | 150 | ns |

**PROGRAMMABLE FILTER CHARACTERISTICS**

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Filter cutoff range 32P4731 | $fc$ @ 3 dB point<br>$fc$ = (0.0708 MHz)<br>x DACF, Boost = 0 dB | 3 | | 9 | MHz |
| 32P4741 | $fc$ = (0.1417 MHz)<br>x DACF, Boost = 0 dB<br>32 ≤ DACF ≤ 127 | 6 | | 18 | MHz |
| Filter cutoff accuracy | DACF = 127 | -10 | | 10 | % |
| ON differential gain (AN) | F = 0.67 x $fc$, boost = 0 dB | 1.6 | 2.0 | 2.4 | V/V |
| OD differential gain (AD) | F = 0.67 x $fc$, boost = 0 dB | 0.9AN | | 1.1AN | V/V |
| Frequency boost @ $fc$ | DACS = 127 | | 13 | | dB |
| Boost accuracy | @ 6 dB, DACS = 37 | -0.75 | | +0.75 | dB |
| | @ 9 dB, DACS = 67 | -1.0 | | +1.0 | dB |
| | @ 13 db, DACS = 127 | -1.5 | | +1.5 | dB |
| Group delay variation<br>Boost = 0 dB to 13 dB | $fc$ = 9 MHz<br>FIN = 0.2 $fc$ to $fc$ | -1.25 | | 1.25 | ns |
| 32P4731 | 3 ≤ Fc < 9 MHz<br>FIN = 0.2 $fc$ to $fc$ | -2 | | +2 | % |
| | 3 ≤ $fc$ < 9 MHz<br>FIN = $fc$ to 1.75 $fc$ | -3 | | +3 | % |
| Group delay variation<br>Boost = 0 dB to 13 dB | $fc$ = 18 MHz<br>FIN = 0.2 $fc$ to $fc$ | -750 | | 750 | ps |
| 32P4741 | 6 ≤ Fc < 18 MHz<br>FIN = 0.2 $fc$ to $fc$ | -2 | | +2 | % |
| | 6 ≤ $fc$ < 18 MHz<br>FIN = $fc$ to 1.75 $fc$ | -3 | | +3 | % |
| Filter differential input dynamic range | THD = 1%, F = 0.67 $fc$<br>boost = 0 dB | 0.5 | | | Vpp |
| Filter differential output dynamic range | THD = 1%, F = 0.67 $fc$<br>boost = 0 dB | 1.0 | | | Vpp |
| Filter differential input resistance | Normal | 5.0 | | | kΩ |
| | Low-Z | | 300 | | Ω |
| Filter differential input capacitance | | | | 7.0 | pF |
| Output noise voltage | BW = 100 MHz, Rs = 50Ω | | | | |

## ELECTRICAL SPECIFICATIONS (continued)

### PROGRAMMABLE FILTER CHARACTERISTICS (continued)

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| 32P4731: differentiated output | $fc$ = 9 MHz, boost = 0 dB | | 2.6 | | mVRms |
| differentiated output | $fc$ = 9 MHz, boost = 13 dB | | 5.6 | | mVRms |
| normal output | $fc$ = 9 MHz, boost = 0 dB | | 2.0 | | mVRms |
| normal output | $fc$ = 9 MHz, boost = 13 dB | | 3.6 | | mVRms |
| 32P4741: differentiated output | $fc$ =18 MHz, boost = 0 dB | | 3.8 | | mVRms |
| differentiated output | $fc$ =18 MHz, boost = 13 dB | | 6.9 | | mVRms |
| normal output | $fc$ =18 MHz, boost = 0 dB | | 2.1 | | mVRms |
| normal output | $fc$ =18 MHz, boost = 13 dB | | 4.2 | | mVRms |
| Filter output sink current | | | 0.5 | | mA |
| Filter output source current | | 2.0 | | | mA |
| Filter output resistance | single ended | | | 200 | Ω |
| Rx pin voltage | Ta = 27°C | | 600 | | mV |
| | Tj = 127°C | | 800 | | mV |
| Rx resistance | 1% fixed value | | 12.1 | | kΩ |

### TIME BASE GENERATOR CHARACTERISTICS

| | | | | | |
|---|---|---|---|---|---|
| FREF input range | | 8 | | 20 | MHz |
| FOUT frequency range | | | | 75 | MHz |
| FOUT jitter | TOUT = 1/FOUT | -200 | | +200 | psRMS |
| | FOUT ≤ 75 MHz | | | | |
| M counter range | | 2 | | 255 | |
| N counter range | | 2 | | 127 | |
| VCO center frequency period (TVCO) | FVCO=[12.5/(RR+0.4)] x [(0.622 x IDAC) + 4.27] (MHz) -1.5V ≤ TFLT-$\overline{\text{TFLT}}$ ≤ +1.5V | 0.90T0 | | 1.10T0 | ns |
| VCO dynamic range | -1.5V ≤ TFLT-$\overline{\text{TFLT}}$ ≤ +1.5V FOUT = 54 MHz | ±25 | | ±45 | % |
| VCO control gain KVCO | ωi = 2π/TVCO -1.5V ≤ TFLT-$\overline{\text{TFLT}}$ ≤ + 1.5V | 0.14 ωi | 0.175 ωi | 0.26 ωi | rad/ (V-S) |
| Phase detector gain KD | KD = [12.5/(RR + 0.4)] x (0.6768 x IDAC + 3.4789) x $10^{-6}$ | 0.83KD | | 1.17KD | A/rad |

**TIME BASE GENERATOR CHARACTERISTICS** (continued)

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| KVCO x KD product accuracy | | -28 | | +28 | % |
| FREF input low time | | 20 | | | ns |
| FREF input high time | | 20 | | | ns |

**DATA SEPARATOR CHARACTERISTICS: Unless otherwise noted, RR = 12.1 kΩ**

**Read Mode**

| | | | | | |
|---|---|---|---|---|---|
| Read clock rise time TRRC | 0.8 to 2.0V CL ≤ 15 pF | | | 5 | ns |
| Read clock fall time TFRC | 2.0 to 0.8V CL ≤ 15 pF | | | 5 | ns |
| RRC duty cycle | | 40 | | 60 | % |
| NRZ out set-up and hold time (TNS, TNH) | | 8 | | | ns |
| NRZ out propagation delay (TPNRZ) | | | | ±15 | ns |
| $\overline{AMD}$ set-up and hold time (TAS, TAH) | | 13.0 | | | ns |
| $\overline{AMD}$ propagation delay (TPAMD) | | | | ±15 | ns |
| 1/3 cell delay | TVCO = 1/[0.622 x IDAC) + 4.27] | 0.8TD | | 1.2TD | ns |

**Write Mode**

| | | | | | |
|---|---|---|---|---|---|
| Write data pulse width (TWD) 32P4731 | 1.5V, CL ≤ 5 pF | 2TVCO/3 -0-5 | | 2TVCO/3 +0-5 | ns |
| 32P4741 | | TVCO+ 0.5 | | TVCO+ 0.5 | ns |
| Write data rise time (TRWD) | 0.8 to 2.0 V CL ≤ 15 pF | | | 5 | ns |
| Write data fall time (TFWD) | 2.0 to 0.8 V CL ≤ 15 pF | | | 5 | ns |
| Write data clock rise time (TRWC) | 0.8 to 2.0 V CL ≤ 15 pF | | | 10 | ns |
| Write data clock fall time (TFWC) | 2.0 to 0.8 V CL ≤ 15 pF | | | 8 | ns |
| NRZ set-up time (TSNRZ) | | 5 | | | ns |
| NRZ hold time (THNRZ) | | 5 | | | ns |

## ELECTRICAL SPECIFICATIONS (continued)

**Data Synchronization**

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Loop filter = TBD | | | | | |
| VCO center frequency period (TVCO) | FVCO=(0.622 x IDAC) + 4.27 (MHz)<br>-1.5V≤ DFLT-$\overline{\text{DFLT}}$ ≤ +1.5V | 0.90T0 | | 1.10T0 | ns |
| VCO dynamic range | -1.5V ≤ DFLT-$\overline{\text{DFLT}}$ ≤ +1.5V | ±25 | | ±45 | % |
| VCO control gain KVCO | ωi = 2π/TVCO (32P4741)<br>ωi = π/TVCO (32P4731) -1.5V ≤ DFLT-$\overline{\text{DFLT}}$ ≤ +1.5V | 0.14 ωi | 0.175 ωi | 0.26 ωi | rad/(V-S) |
| Phase detector gain, KD | PLL ref = FOUT | 0.83KD | | 1.17KD | µA/rad |
| | Idle mode = 1 x KD<br>Read mode = 3 x KD<br>Read mode after gain shift = 1 x KD<br>KD = [12.5/(RR + 0.4)] x (0.6768 x IDAC + 3.4789) x $10^{-6}$ | 0.83KD | | 1.17KD | A/rad |
| KVCO x KD product accuracy | | -28 | | +28 | % |
| VCO phase restart error | | -2 | | +2 | ns |
| Decode window center accuracy | 32P4731 | -1.5 | | +1.5 | ns |
| | 32P4741 | -0.75 | | +0.75 | ns |
| Decode window width | 32P4731 | (2TVCO/3)-1.5 | | | ns |
| | 32P4741 | TVCO-0.75 | | | ns |

**Window Shift Control**

Window shift magnitude is set by the value in the Window Shift (WS) register. The WS register bits are as follows:

| BIT | NAME | FUNCTION |
|---|---|---|
| 0 | $\overline{WS0}$ | |
| 1 | $\overline{WS1}$ | |
| 2 | $\overline{WS2}$ | |
| 3 | $\overline{WS3}$ | |
| 4 | WSD | Window shift direction. 0=early, 1=late |
| 5 | WSE | Window shift enable |
| 6 | TDAC0 | Used to route signals to DAC test point |
| 7 | TDAC1 | Used to route signals to DAC test point |

The window shift magnitude is set as a percentage of the decode window, in 2% steps. The tolerance of the window shift magnitude is ±15%. Window shift should be set during idle mode or write mode.

| $\overline{WS3}$ | $\overline{WS2}$ | $\overline{WS1}$ | $\overline{WS0}$ | Shift Magnitude |
|---|---|---|---|---|
| 1 | 1 | 1 | 1 | No shift |
| 1 | 1 | 1 | 0 | 2% (minimum shift) |
| 1 | 1 | 0 | 1 | 4% |
| 1 | 1 | 0 | 0 | 6% |
| 1 | 0 | 1 | 1 | 8% |
| 1 | 0 | 1 | 0 | 10% |
| 1 | 0 | 0 | 1 | 12% |
| 1 | 0 | 0 | 0 | 14% |
| 0 | 1 | 1 | 1 | 16% |
| 0 | 1 | 1 | 0 | 18% |
| 0 | 1 | 0 | 1 | 20% |
| 0 | 1 | 0 | 0 | 22% |
| 0 | 0 | 1 | 1 | 24% |
| 0 | 0 | 1 | 0 | 26% |
| 0 | 0 | 0 | 1 | 28% |
| 0 | 0 | 0 | 0 | 30% (maximum shift) |

## ELECTRICAL SPECIFICATIONS (continued)

### WRITE PRECOMP CONTROL

Write precomp magnitude is set by the value in the Write precomp (WP) register. The WP register bits are as follows:

| BIT | NAME | FUNCTION |
|---|---|---|
| 0 | $\overline{WE0}$ | Early Precomp Magnitude |
| 1 | $\overline{WE1}$ | Early Precomp Magnitude |
| 2 | $\overline{WE2}$ | Early Precomp Magnitude |
| 3 | WPE | Write Precomp enable, 0 = Disable 1 = Enable |
| 4 | $\overline{WL0}$ | Late Precomp Magnitude |
| 5 | $\overline{WL1}$ | Late Precomp Magnitude |
| 6 | $\overline{WL2}$ | Late Precomp Magnitude |
| 7 | – | Not used |

The write precomp magnitude is calculated as:

$$TPC = a \times 0.04 \times Tvco \text{ (32P4731)}$$
$$TPC = a \times 0.02 \times Tvco \text{ (32P4741)}$$

where a = precomp magnitude scaling factor as shown below. TREF is the period of the reference frequency provided by the internal time base generator.

| $\overline{Wn2}$ | $\overline{Wn1}$ | $\overline{Wn0}$ | Precomp Magnitude Scaling Factor |
|---|---|---|---|
| 1 | 1 | 1 | No precomp |
| 1 | 1 | 0 | 1X |
| 1 | 0 | 1 | 2X |
| 1 | 0 | 0 | 3X |
| 0 | 1 | 1 | 4X |
| 0 | 1 | 0 | 5X |
| 0 | 0 | 1 | 6X |
| 0 | 0 | 0 | 7X (maximum) |

| BIT N-2 | BIT N-1 | BIT N | BIT N+1 | BIT N+2 | BIT N COMPENSATION |
|---|---|---|---|---|---|
| 1 | 0 | 1 | 0 | 1 | None |
| 0 | 0 | 1 | 0 | 0 | None |
| 1 | 0 | 1 | 0 | 0 | Early |
| 0 | 0 | 1 | 0 | 1 | Late |

Late = Bit N is time shifted toward the N+1 bit by the programmed magnitude
Early = Bit N is time shifted toward the N-1 bit by the programmed magnitude

**TABLE 4: 1,7 RLL Encode Table**

| NRZ DATA | | | ENCODED WRITE DATA | | | | |
|---|---|---|---|---|---|---|---|
| Present | | Next | Previous | Present | | | |
| $D_1$ | $D_2$ | $D_1^* D_2^*$ | $Y_3'$ | $Y_1$ | $Y_2^*$ | $Y_3^*$ | |
| 0 | 0 | 0 | 1 | 0 | 0 | 1 | |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | |
| 0 | 0 | 1 | 1 | 0 | 1 | 0 | |
| 1 | 0 | 0 | | 1 | 0 | 1 | |
| 1 | 0 | 1 | | 0 | 1 | 0 | |
| 0 | 1 | 0 0 | 0 | 0 | 0 | 1 | |
| 0 | 1 | 0 0 | 1 | 0 | 1 | 0 | |
| 0 | 1 | 1 0 | | 0 | 0 | 0 | |
| 0 | 1 | 0 1 | 0 | 0 | 0 | 1 | |
| 0 | 1 | 0 1 | 1 | 0 | 0 | 0 | |
| 0 | 1 | 1 1 | | 0 | 0 | 0 | |
| 1 | 1 | 0 0 | 0 | 0 | 1 | 0 | |
| 1 | 1 | 1 0 | 0 | 1 | 0 | 0 | |
| 1 | 1 | 0 1 | 0 | 1 | 0 | 0 | |
| 1 | 1 | 1 1 | 0 | 1 | 0 | 0 | |

**TABLE 5: 1,7 RLL Decode Table**

| ENCODED READ DATA | | | | | | DECODED DATA | |
|---|---|---|---|---|---|---|---|
| Previous | | Present | | | Next | | |
| $Y_2'$ | $Y_3'$ | $Y_1$ | $Y_2$ | $Y_3$ | $Y_2^* Y_3^*$ | $D_1$ | $D_2$ |
| 0 | 0 | 0 | 0 | 0 | | 0 | 1 |
| 1 | 0 | 0 | 0 | 0 | | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | | 0 | 1 |
| | | 1 | 0 | 0 | | 1 | 1 |
| | 0 | 0 | 1 | 0 | 0 0 | 1 | 1 |
| | 0 | 0 | 1 | 0 | 1 0 | 1 | 0 |
| | 0 | 0 | 1 | 0 | 0 1 | 1 | 0 |
| | 1 | 0 | 1 | 0 | 0 0 | 0 | 1 |
| | 1 | 0 | 1 | 0 | 1 0 | 0 | 0 |
| | 1 | 0 | 1 | 0 | 0 1 | 0 | 0 |
| 0 | 0 | 0 | 0 | 1 | | 0 | 1 |
| 1 | 0 | 0 | 0 | 1 | | 0 | 0 |
| 0 | 1 | 0 | 0 | 1 | | 0 | 0 |
| | | 1 | 0 | 1 | | 1 | 0 |

## ELECTRICAL SPECIFICATIONS (continued)

**TABLE 6A: 32P4731 Clock Source and Frequency vs. Mode**

| WG | VCO RG | REF | DECODE RCLK | ENCODE CLOCK | CLOCK | MODE |
|---|---|---|---|---|---|---|
| 0 | 0 | FOUT/2 | FOUT/3 | FOUT/2 | FOUT/2 | IDLE |
| 0 | 1 | $\overline{DRD}$ | VCO/3 | VCO/2 | FOUT/2 | READ |
| 1 | 0 | FOUT/2 | FOUT/3 | FOUT/2 | FOUT/2 | WRITE |

NOTE 1: Until the VCO locks to the new source, the VCO/2 entries will be FOUT/2.

NOTE 2: Until the VCO locks to the new source, the VCO/3 entries will be FOUT/3.

NOTE 3: WG = RG = 1 is an indeterminate state.

**TABLE 6B: 32P4741 Clock Source and Frequency vs. Mode**

| WG | RG | VCO REF | RCLK | DECODE CLOCK | ENCODE CLOCK | MODE |
|---|---|---|---|---|---|---|
| 0 | 0 | FOUT | 2FOUT/3 | FOUT | FOUT | IDLE |
| 0 | 1 | $\overline{DRD}$ | 2VCO/3 | VCO | FOUT | READ |
| 1 | 0 | FOUT | 2FOUT/3 | FOUT | FOUT | WRITE |

NOTE 1: Until the VCO locks to the new source, the VCO/2 entries will be FOUT.

NOTE 2: Until the VCO locks to the new source, the 2VCO/3 entries will be 2FOUT/3.

NOTE 3: WG = RG = 1 is an indeterminate state.

**TABLE 7: Multiplexed Test Point Signal Selection**

| MTPE | TMS1 | TMS0 | MTP1 | MTP2 | MTP3 |
|---|---|---|---|---|---|
| 0 | X | X | OFF | OFF | OFF |
| 1 | 0 | 0 | VCOREF | DS-IN | DSREF |
| 1 | 0 | 1 | RD | DOUT | COUT |
| 1 | 1 | 0 | VCOREF | DS-IN | MCTR |
| 1 | 1 | 1 | SET | RESET | COUT |

COUT = Output of the pulse qualifier clock circuit

DOUT = Output of the pulse qualifier data comparators

DS-IN = Delayed read data output (read mode), Fout/2 (in non-read mode)

DSREF = Output of the time base generator

MCTR = M counter output of the time base generator

RD = Read data output from the pulse qualifier

RESET = Output of the negative threshold comparator

SET = Output of the positive threshold comparator

VCOREF = Data separator VCO reference clock

NOTES:
1) When the PWRON pin is LOW ("0") the Power Down Control Register is active. All blocks that have their control bit set to "1" will be powered down. When the PWRON pin is HIGH ("1") the device goes into a sleep mode with all blocks powered down except the serial port.

2) When the threshold DAC reference is switched, there is a maximum settling time of 1.5µsec for the DAC.

**FIGURE 14: Power Control Timing**

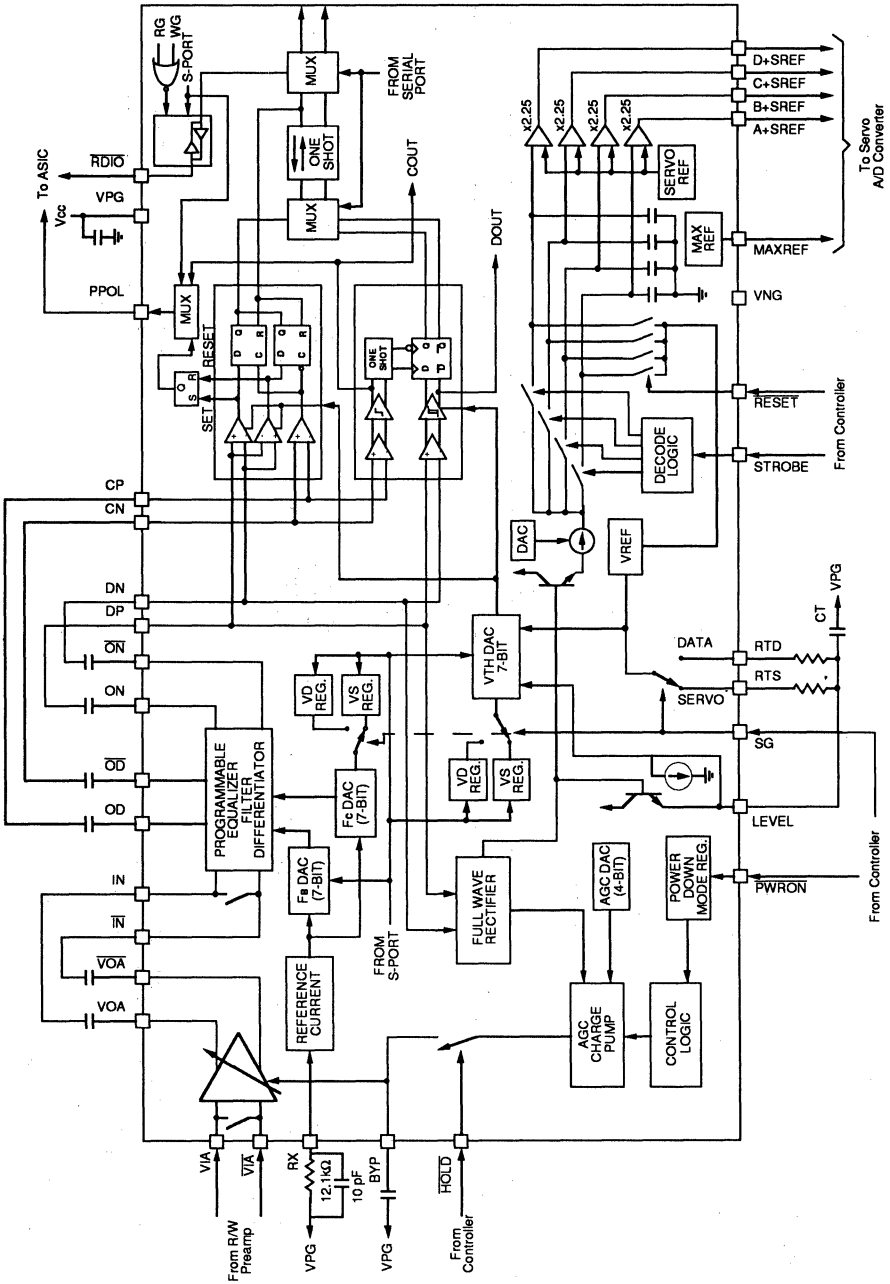



**FIGURE 15A: 32P4731/41 Application Diagram**

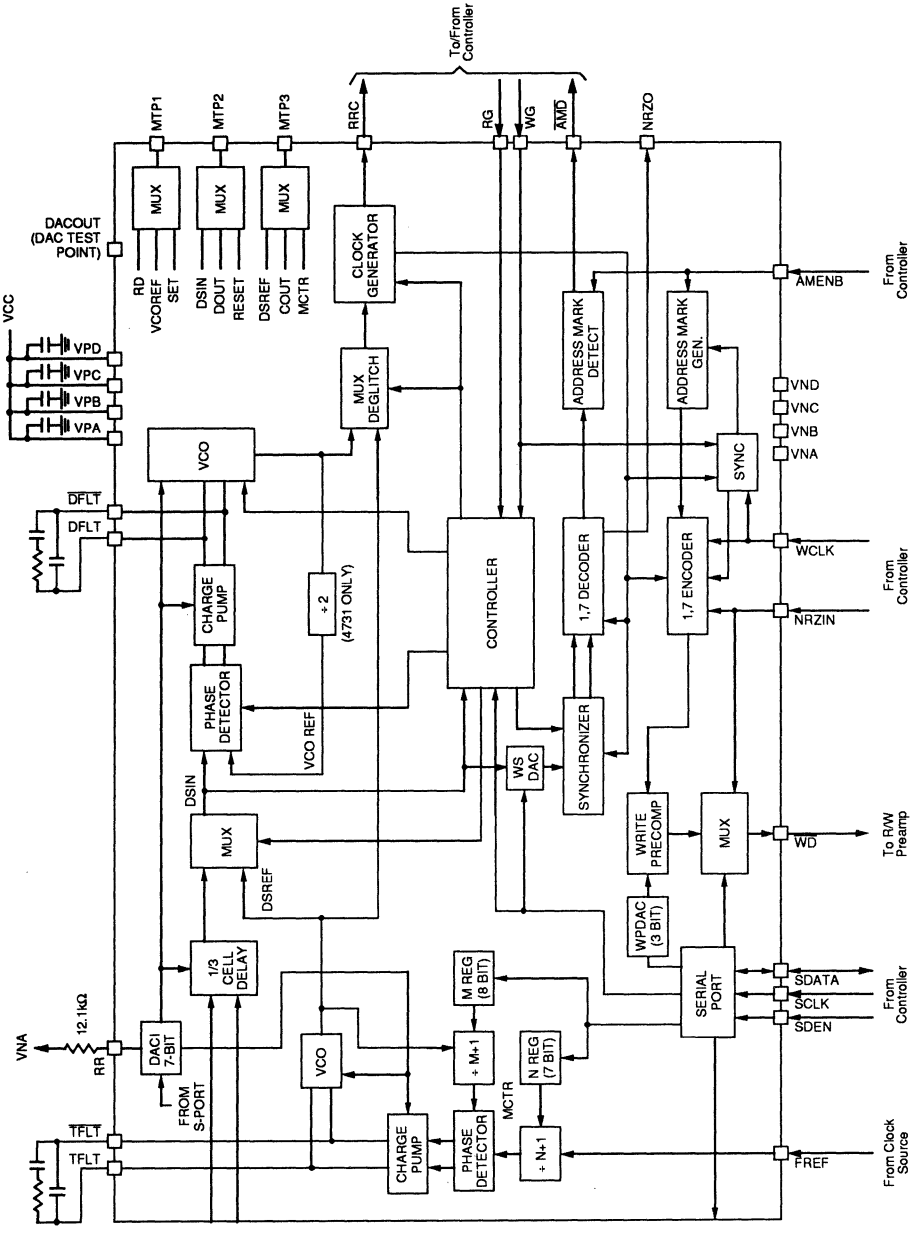
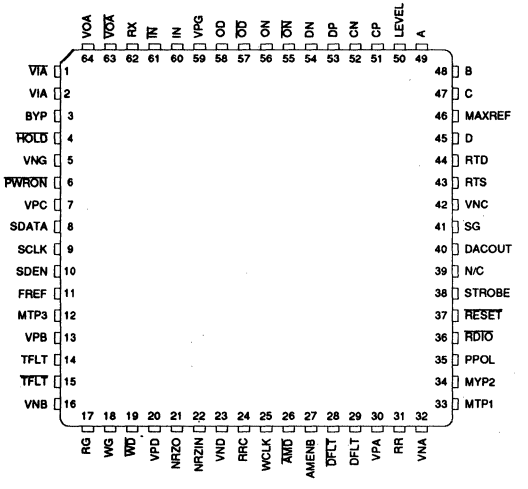



FIGURE 15B: 32P4731/41 Application Diagram

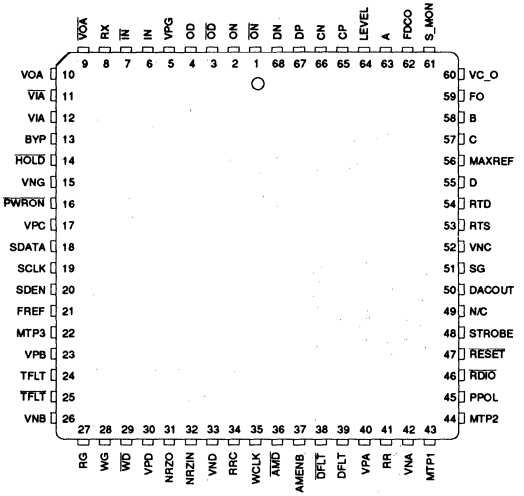
# SSI 32P4731/41
# Read Channel with
# 1,7 ENDEC, 4-burst Servo

## PACKAGE PIN DESIGNATIONS

(Top View)




**64-Pin TQFP**




**68-Pin PLCC**

**Advance Information:** Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.



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Section 6

# HDD HEAD POSITIONING

silicon systems®
A TDK Group Company

# SSI 32H569
## Servo Motor Driver

January 1993

## DESCRIPTION

The SSI 32H569 Servo Motor Driver is a bipolar device intended for use in Winchester disk drive head positioning systems employing linear or rotary voice coil motors. When used in conjunction with a position controller, such as the SSI 32H6220 Servo Controller, and a position reference, such as the SSI 32H6210 Servo Demodulator, the device allows the construction of a high performance, dedicated surface head positioning system.

The SSI 32H569 serves as a transconductance amplifier by driving 4 MOSFETs in an H-bridge configuration, performs motor current sensing and limits motor current and velocity. In its linear tracking mode, class B operation is guaranteed by crossover protection circuitry, which ensures that only one MOSFET in each leg of the H-bridge is active. The MOSFET drivers are disabled when motor velocity or current exceed externally programmable limits. In addition, automatic head retraction and spindle braking may be initiated by a low voltage condition or upon external command.

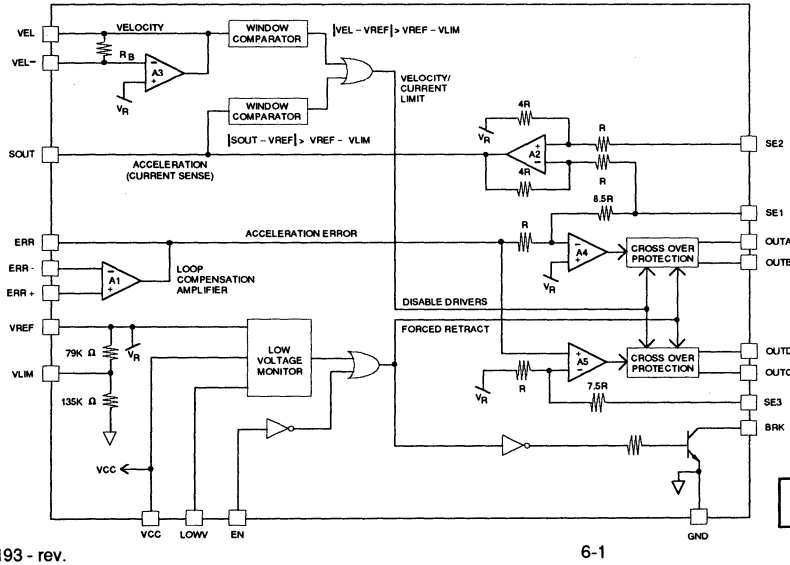
(continued)

## FEATURES

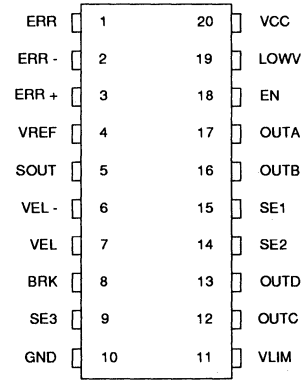
- **Predriver for linear and rotary voice coil motors**
- **Interfaces directly to MOSFET H-Bridge motor driver**
- **Class B linear mode and constant velocity retract mode**
- **Precision differential amplifier for motor current sensing**
- **Motor current and velocity limiting circuitry**
- **Automatic head retract and spindle braking signal on power failure**
- **External digital enable**
- **Servo loop parameters programmed with external components**
- **Advanced bipolar IC requires under 240 mW from 12V supply**
- **Available in 20-pin DIP or SO packaging**

6

## BLOCK DIAGRAM




## PIN DIAGRAM




20-Pin SO, DIP

CAUTION: Use handling procedures necessary for a static sensitive component.

## DESCRIPTION (continued)

The SSI 32H569 is implemented in an advanced bipolar process and dissipates less than 240 mW from a 12V supply. The IC is available in 20-pin DIP and 20-pin SO packaging.

## FUNCTIONAL DESCRIPTION

(Refer to block diagram and typical application Fig.2)

The SSI 32H569 has two modes of operation, linear and retract. The retract mode is activated by a power supply failure or when the control signal EN is false. Otherwise the device operates in linear mode.

During linear operation, an acceleration signal from the servo controller is applied through amplifier A1, whose three connections are all available externally. RC components may be used to provide loop compensation at this stage. The ERR signal drives two precision amplifiers, each with a gain of 8.5. The first of these amplifiers is inverting, and is formed from opamp A4, an on-chip resistor divider and an off-chip complementary MOSFET pair. The second is non-inverting, and is formed in a similar manner from opamp A5. Feedback from the MOSFET drains, on sense inputs SE1 and SE3, allows the amplifiers gains to be established precisely. The voice coil motor and a series current sense resistor are connected between SE1 and SE3.

Crossover protection circuitry between the outputs of A4 and A5, and the external MOSFETs, ensures class B operation by allowing only one MOSFET in each leg of the H-bridge to be in conduction. The crossover separation threshold, illustrated in Figure 5, is the maximum drive on any MOSFET gate when the motor voltage changes sign. The crossover circuitry can also disable all MOSFETS simultaneously (to limit motor current or velocity) or apply a constant voltage across the motor (to retract the heads at a constant velocity).

Motor current is sensed by a small resistor placed in series with the motor. The voltage drop across this resistor is amplified by a differential amplifier with a gain of 4 (A2 and associated resistors), whose inputs are SE1 and SE2. The resulting voltage, SOUT, is proportional to motor current, and hence acceleration. This signal is externally fed back to A1, so that the signal ERR represents the difference between the desired acceleration (from the servo controller) and the actual motor acceleration. If SOUT is integrated, using opamp A3 and an external RC network, the resulting signal, VEL, is proportional to the motor velocity.

Both SOUT and VEL are connected to window comparators, which are used to detect excessive motor current or velocity. The comparator outputs disable the MOSFET drivers until the motor comes within limits again. The VLIM pin may be used to program the voltage limits for the window comparators. The maximum voltage excursion allowed about VREF is (VREF-VLIM). An on-chip resistor divider sets a default value for VLIM and if VLIM is connected to ground, the windowing is effectively disabled.

The SSI 32H569 has low voltage monitor circuitry that will detect a loss of voltage on the VREF, VCC or LOWV pins. The power supply pin, VCC, should be connected to the disk drive's spindle motor so that its stored rotational energy may be used to hold up VCC briefly during a power failure. LOWV is used to detect a system power supply failure. When a low voltage condition is detected, the MOSFET drivers switch from linear operation to retract mode. In this mode a constant voltage is applied across the motor which will cause the heads to move at a constant speed. A mechanical stop must be provided for the heads when they reach a safe location. The current limiting circuitry will disable the MOSFET drivers when motor current increases due to loss of the velocity-induced back EMF. An open collector output, BRK, which is active while the device is in retract mode, is provided for spindle motor braking. An external RC delay may be used to defer braking until the heads are retracted. For proper operation of the SSI 32H569, a pullup resistor on BRK is required even if the BRK output is not used.

An example of an entire servo path implemented with the SSI 32H569 and its companion devices, the SSI 32H6210 and 32H6220, is shown in Figure10.

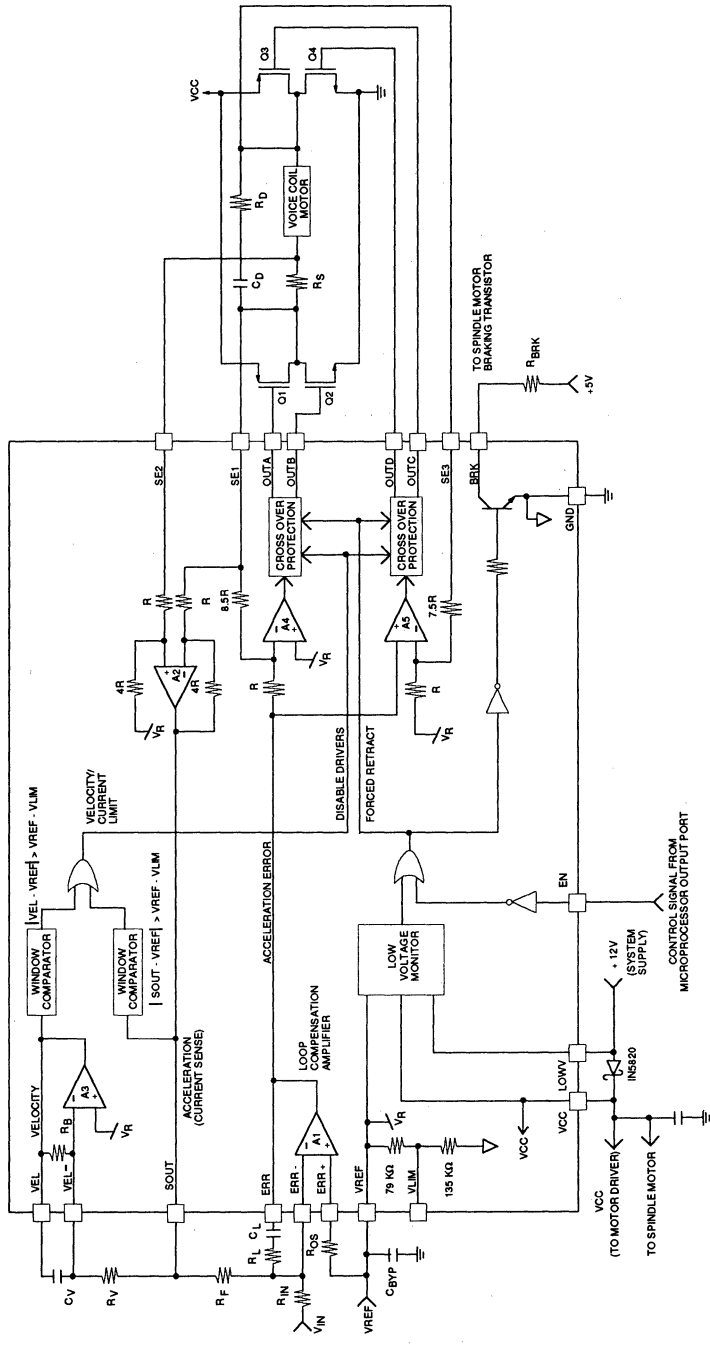



**FIGURE 2: Typical Application**

## PIN DESCRIPTION

### POWER

| NAME | PIN | TYPE | DESCRIPTION |
|---|---|---|---|
| VCC | 20 | | POSITIVE SUPPLY - 12V power supply. Usually taken from spindle motor supply. Spindle motor stored energy permits head retraction during power failure. If VCC falls below 9V, a forced head retraction occurs. |
| LOWV | 19 | I | LOW VOLTAGE - System 12V supply. If this input falls below 9V, a forced head retraction occurs. |
| VREF | 4 | I | REFERENCE VOLTAGE - 5.4V input. All analog signals are referenced to this voltage. If VREF falls below 4.3V, a forced head retraction occurs. |
| GND | 10 | | GROUND |

### CONTROL

| NAME | PIN | TYPE | DESCRIPTION |
|---|---|---|---|
| ERR | 1 | O | POSITION ERROR- Loop compensation amplifier output. This signal is amplified by the MOSFET drivers and applied to the motor by an external MOSFET H-bridge, as follows: SE3-SE1 = 17(ERR-VREF) |
| ERR- | 2 | I | POSITION ERROR INVERTING INPUT - Inverting input to the loop compensation amplifier. |
| ERR+ | 3 | I | POSITION ERROR NON-INVERTING INPUT - Non-inverting input to the loop compensation amplifier. |
| SOUT | 5 | O | MOTOR CURRENT SENSE OUTPUT - This output provides a voltage proportional to the voltage drop across the external current sense resistor, as follows: SOUT-VREF=4(SE2-SE1) |
| VEL- | 6 | I | VELOCITY INVERTING INPUT - Inverting input to the velocity integrating amplifier. The non-inverting input is connected internally to VREF. |
| VEL | 7 | O | VELOCITY OUTPUT - Output of the velocity integration amplifier. This signal is internally applied to a window comparator whose output limits motor drive current when the voltage at VEL exceeds a set limit. |
| BRK | 8 | O | BRAKE OUTPUT - Active high, open collector output which may be used to enable an external spindle motor braking transistor upon power failure or deassertion of EN. |
| VLIM | 11 | I | LIMITING VOLTAGE - The voltage at this pin sets motor current and velocity limits. Limiting occurs when: \|SOUT-VREF\|>VREF-VLIM or \|VEL-VREF\|>VREF-VLIM. An internal resistor divider establishes a default value that may be externally adjusted. |

**CONTROL** (Continued)

| NAME | PIN | TYPE | DESCRIPTION |
|---|---|---|---|
| SE2 | 14 | I | MOTOR CURRENT SENSE INPUT - Non-inverting input to the current sense differential amplifier. It should be connected to one side of an external current sensing resistor in series with the motor. The inverting input of the differential amplifier is connected internally to SE1. |
| EN | 18 | I | ENABLE - Active high TTL compatible input enables linear tracking mode. A low level will initiate a forced head retract. |

**FET DRIVE**

| NAME | PIN | TYPE | DESCRIPTION |
|---|---|---|---|
| SE3 | 9 | I | MOTOR VOLTAGE SENSE INPUT - This input provides feedback to the non-inverting MOSFET driver amplifier. It is connected to one side of the motor. The gain to this point is: SE3-VREF = 8.5(ERR-VREF) |
| OUTC | 12 | O | P-FET DRIVE (NON-INVERTING) - Drive signal for a P channel MOSFET connected between one side of the motor and VCC. This MOSFET drain is connected to SE3. |
| OUTD | 13 | O | N-FET DRIVE (NON-INVERTING) - Drive signal for an N channel MOSFET connected between one side of the motor and GND. This MOSFET drain is connected to SE3. Crossover protection circuitry ensures that the P and N channel devices driven by OUTC and OUTD are never enabled simultaneously. |
| SE1 | 15 | I | MOTOR VOLTAGE SENSE INPUT - This input provides feedback to the inverting MOSFET driver amplifier. It is connected to the current sensing resistor which is in series with the motor. The gain to this point is: SE1-VREF = -8.5(ERR-VREF) This input is internally connected to the current sense differential amplifier inverting input. |
| OUTB | 16 | O | N-FET DRIVE (INVERTING) - Drive signal for an N channel MOSFET connected between the current sense resistor and GND. This MOSFET drain is also connected to SE1. |
| OUTA | 17 | O | P-FET DRIVE (INVERTING) - Drive signal for a P channel MOSFET connected between the current sense resistor and VCC. This MOSFET drain is also connected to SE1. Crossover protection circuitry ensures that the P and N channel devices driven by OUTC and OUTD are never enabled simultaneously. |

## ELECTRICAL SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS

(Maximum limits indicates where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC operating characteristics.)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| VCC | | 0 | | 16 | V |
| VREF | | 0 | | 10 | V |
| SE1, SE2, SE3 | | -1.5 | | 15 | V |
| All other pins | | 0 | | 14 | V |
| Storage temperature | | -45 | | 165 | °C |
| Solder temperature | 10 sec duration | | | 260 | °C |

**RECOMMENDED OPERATION CONDITIONS** (Unless otherwise noted, the following conditions are valid throughout this document.)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| VCC | Normal Mode | 9 | 12 | 13.2 | V |
| | Retract Mode | 3.5V | | 14 | V |
| VREF | | 5 | | 7 | V |
| Operating temperature | | 0 | | 70 | °C |

### DC CHARACTERISTICS

| | | | | | |
|---|---|---|---|---|---|
| ICC, VCC current | | | | 20 | mA |
| IREF, VREF current | | | | 2 | mA |

### A1, LOOP COMPENSATION AMPLIFIER

| | | | | | |
|---|---|---|---|---|---|
| Input bias current | | | | 500 | nA |
| Input offset voltage | | | | 3 | mV |
| Voltage swing | About VREF | 2 | | | V |
| Common mode range | About VREF | ±1 | | | V |
| Load resistance | To VREF | 4 | | | KΩ |
| Load capacitance | | | | 100 | pF |
| Gain | | 80 | | | dB |
| Unity gain bandwidth | | 1 | | | MHz |
| CMRR | f<20 kHz | 60 | | | dB |
| PSRR | f<20 kHz | 60 | | | dB |

### A2, CURRENT SENSE AMPLIFIER

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| Input impedance | SE1 to SE2 | 3.5 | 5 | | KΩ |
| Input offset voltage | | | | 2 | mV |
| Output voltage swing | | VREF-4 | | VCC-1.2 | V |
| Common mode range | | 0 | | VCC-0.2 | V |
| Load Resistance | To VREF | 4 | | | KΩ |
| Load Capacitance | | | | 100 | pF |
| Output impedance | f<40 KHz | | | 20 | Ω |
| Gain (SOUT-VREF)/(SE1-SE2) | $V_{SE2} = V_{REF}$ | 3.9 | 4 | 4.1 | V/V |
| Unity gain bandwidth | | 1 | | | MHz |
| CMRR | f<20 KHz | 52 | | | dB |
| PSRR | f<20 KHz | 60 | | | dB |

### A3, VELOCITY INTEGRATING AMPLIFIER

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| Input bias current | | | | 250 | nA |
| Input offset voltage | | | | 2 | mV |
| Voltage swing | | VREF-4 | | VCC-1.2 | V |
| Common mode range | | 4.5 | | 6 | V |
| Load resistance | To VREF | 10 | | | KΩ |
| Load capacitance | | | | 100 | pF |
| RB, internal feedback resistor | | 80 | | 150 | KΩ |

### WINDOW COMPARATORS AND LIMITING

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| Window comparator threshold (SOUT-VREF or VEL-VREF) | | VREF-VLIM | | | V |
| Threshold hysteresis | | 35 | 50 | 65 | % |
| VLIM voltage | No external parts | VREF-1.8 | | VREF-2.2 | V |
| VLIM input resistance | | 50 | | | KΩ |

6

**POWER SUPPLY MONITOR**

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| VCC fail threshold | | 8.5 | 9 | 9.8 | V |
| LOWV fail threshold | \|ILowv\| < 0.5 mA | 8.5 | 9 | 9.8 | V |
| VREF fail threshold | | 3.9 | 4.3 | 4.8 | V |
| Hysteresis (LOWV, VCC) | | | 250 | | mV |
| Hysteresis (VREF) | | | 110 | | mV |
| EN input low voltage | \|IIL\| < 0.5 mA | 0.8 | | | V |
| EN input high voltage | \|IIH\| < 40 uA | | | 2 | V |
| BRK voltage | normal mode, \|IOL\| < 1 mA | | | 0.4 | V |
| BRK leakage current | retract mode | | | 10 | µA |
| BRK delay (from power fail or EN false to BRK floating) | | | | 1 | ms |

**MOSFET DRIVERS**

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| SE3 Input impedance | To VREF | 10 | 25 | | KΩ |
| OUTA, OUTC voltage swing \|Io\|<1 mA | | 0.7 | | VCC-1 | V |
| OUTB, OUTD voltage swing \|Io\|<1 mA | | 1 | | VCC-1 | V |
| VTH, Crossover separation threshold | | | | 2 | V |
| Slew rate (OUTA, OUTB, OUTC, OUTD) | Cl<1000 pF | 1.4 | | | V/µs |
| Crossover time | 300 mV step at ERR | | | 5 | µs |
| Output impedance (OUTA,B,C,D) | | | 50 | | KΩ |
| Transconductance I(OUTA,B,C,D)/(ERR-VREF) | | | 8 | | mA/V |
| Gain (-(SE1-VREF)/(ERR-VREF) or (SE3-VREF)/(ERR-VREF) ) | | 8 | 8.5 | 9 | V/V |
| Offset current | $R_S$ = 0.2Ω, $R_F$ = $R_{IN}$, $V_{IN}$=VREF | | | 20 | mA |
| Retract motor voltage (SE1-SE3) | | 0.7 | 1 | 1.3 | V |

## APPLICATIONS INFORMATION

A typical SSI 32H569 application is shown in Figure 2. The selection criteria for the external components shown are discussed below. Figure 3 shows the equivalent circuit and equations for the DC motor used in the following derivations. While the nomenclature chosen is for a rotating motor, the results are equally applicable to linear motors.

### MOTOR CURRENT SENSE AND LIMITING

The series resistor which senses motor current, Rs, is chosen to be small compared to the resistance of the motor, $R_m$. A value of Rs = 0.2Ω is typical in disk drive applications. The window comparator threshold, programmed by VLIM, must be chosen to cause limiting when the motor current reaches its maximum permissible value. If iMAX is the maximum motor current in Amps, then this value may be chosen as follows:

$$VLIM = VREF - 4 \cdot R_s \cdot iMAX \ (V)$$

VLIM may be set with a resistor divider whose thevenin resistance is substantially less than the output resistance of the VLIM pin (50 KΩ). The window comparators have hysteresis (typically 50% of their threshold, VREF-VLIM) to prevent multiple triggerings of the driver disable signal.

### VELOCITY LIMITING

The values of Rv and Cv in the velocity integrator are chosen to produce a voltage excursion of VREF-VLIM, when the motor speed is at its maximum permissible value. Rv must be large enough to prevent overloading of opamp A2. The following equation ignores the effect of RB, the internal resistor between VEL and VEL- which prevents saturation of A3 due to offsets. For the motor in Figure 3, with maximum velocity ωMAX (rad/s) these components may be chosen as follows:

$R_V // R_F > 4K\Omega$ (A2 output loading restriction)

$$C_V = \frac{4 R_s \cdot J\theta \cdot \omega MAX}{(VREF - VLIM) \cdot R_V \cdot K_m} \ (F)$$

### LOOP COMPENSATION

The transfer function of the SSI 32H569 in the application of Figure 2 is shown in figure 4(a). If the zero due to RL and CL in the loop compensation circuit is chosen to cancel the pole due to the motor inductance, Lm, then the transfer function can be simplified as shown in figure 4(b), under the assumption that this pole and the pole due to the motor mechanical response are widely separated. CL may then be chosen to set the desired open loop unity gain bandwidth.

$$C_L = \frac{68 \cdot R_s}{2 \cdot \pi \cdot R_F \cdot (R_m + R_s) \cdot BW}$$

where BW is the unity gain open loop bandwidth

$$R_L = \frac{L_m}{C_L \cdot (R_m + R_s)}$$

The closed loop response of the servo driver and motor combination, using the component values and simplifying assumptions given above, is given by:

$$\frac{i_m}{V_{in}}(s) = -\frac{1}{R_{in}} \cdot \frac{R_F}{4 \cdot R_s} \cdot \frac{1}{\left(1 + \frac{s}{2 \cdot \pi \cdot BW}\right)}$$

(This analysis neglects the pole due to the output impedance of the MOSFET drivers and the MOSFET gate capacitance, an effect that may be significant in some systems).

RF is chosen to be sufficiently large to avoid overloading A2 ($R_F // R_V > 4K\Omega$). The input resistor, RIN, sets the conversion factor from servo controller output voltage to servo motor current. RIN is chosen such that the servo controller internal voltages are scaled conveniently. The resistor ROS is optional and cancels out the effect of the input bias current of A1.

$$R_{os} = R_{in} // R_F$$

The external components RD and CD have no effect on the motor dynamics, but may be used to improve the stability of the MOSFET drivers. The load represented by the motor, ZM, is given by:

At frequencies above $(R_S + R_m)/(2 \cdot \pi \cdot L_m)$ Hz, this load

$$ZM = (R_s + R_m)\left(1 + s\frac{L_m}{R_s + R_m}\right)\left(1 + \frac{K_m^2}{s \cdot J\theta \cdot (R_s + R_m)}\right)(\Omega)$$

becomes entirely inductive, which is undesireable. RD and CD may be used to add some parallel resistive loading at these frequencies.

### H-BRIDGE MOSFETS

The MOSFETs chosen for the H-bridge should have gate capacitances in the range of 500-1000 pF. The MOSFET input capacitance forms part of the compensation for the MOSFET drivers, so values below 500 pF may cause some driver instability. Excessive input capacitance will degrade the slew mode performance of the drivers.

When the motor voltage is changing polarity, the crossover protection circuits at outputs OUTA-OUTD ensure that the maximum MOSFET gate drive is less than 2V (the crossover separation threshold), as illustrated in Figure 5. The thresholds of the MOSFET devices chosen should be as large as possible to minimize conduction in this region. If the device thresholds are significantly less than the crossover separation threshold, the N and P channel devices in each leg of the H-bridge will conduct simultaneously, causing unnecessary power dissipation.

### POWER FAILURE OPERATION

The power supply for the SSI 32H569, VCC, should be taken from the system 12V supply through a schottky diode (maximum 0.5V drop at If = 3A) and connected to the disk drive spindle motor. If the system power fails, the IC will continue to operate as the spindle motor becomes a generator. The SSI 32H569 will detect the power failure and cause a forced head retract, continuing to operate with VCC as low as 3.5V. The power fail mode will commence if either VCC or LOWV falls below 9V, or VREF falls below 4.3V, or EN is false. Hysteresis on the low voltage thresholds prevents the device from oscillating between operating modes when the power supply is marginal.

The BRK output, which is pulled low during normal operation, floats during a power failure. This allows an external transistor to be enabled for spindle motor braking. An external RC delay may be added to defer braking until head retraction is complete, since the spindle motor is required to generate the supply voltage during retraction.

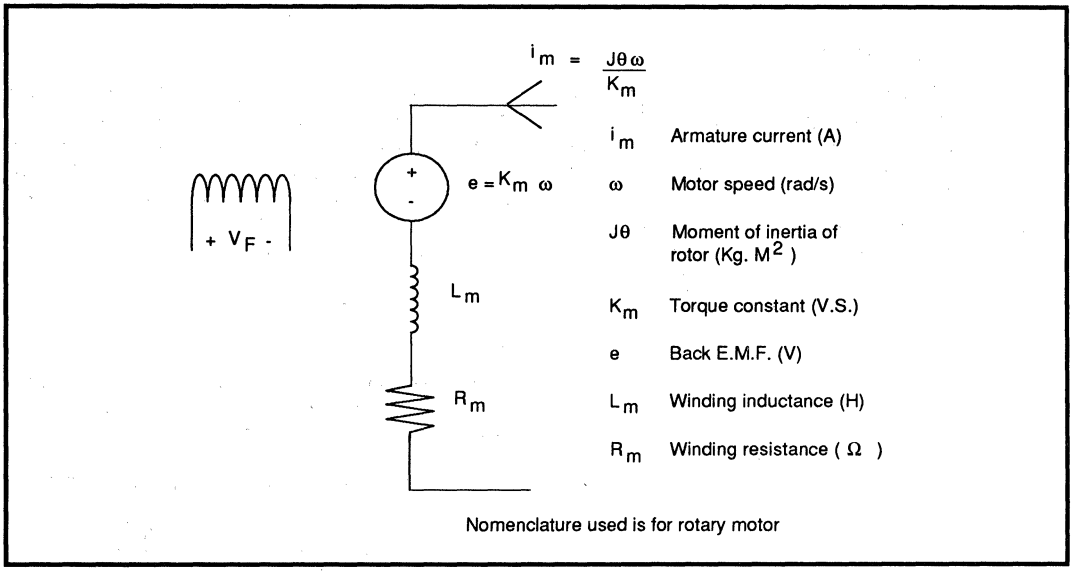



**FIGURE 3: Equivelant Circuit For Fixed Field DC Motor**

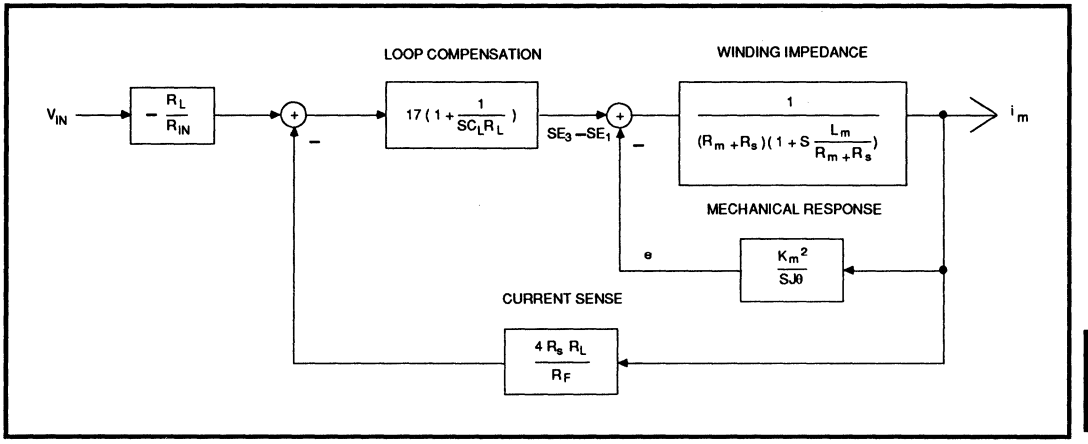



**FIGURE 4(A): Transfer Function Of SSI 32H569 In Typical Application With Fixed Field DC Motor**

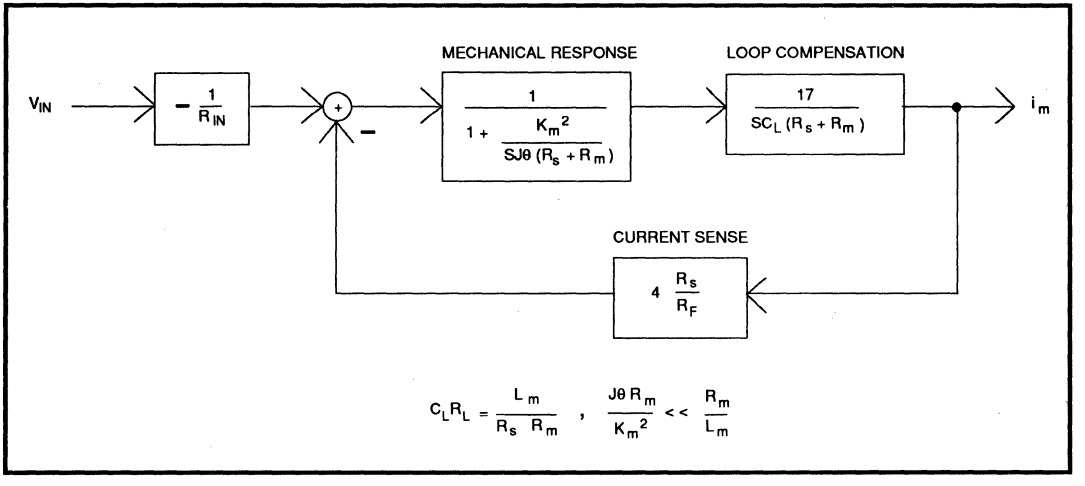



**FIGURE 4(B): Simplified Transfer Function Of SSI 32H569 In DC Motor Application**

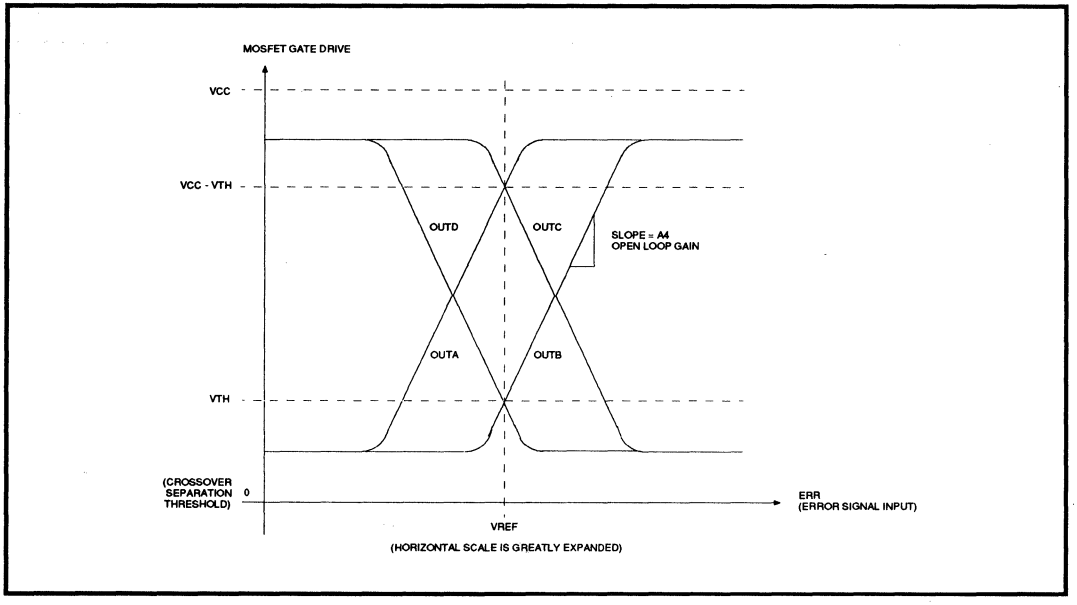



**FIGURE 4(B): Simplified Transfer Function Of SSI 32H569 In DC Motor Application**

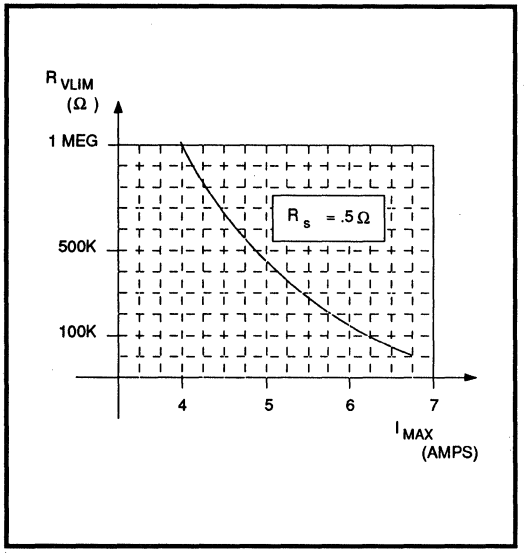



**FIGURE 6: RVLIM To Ground Typical Motor Current Limit**

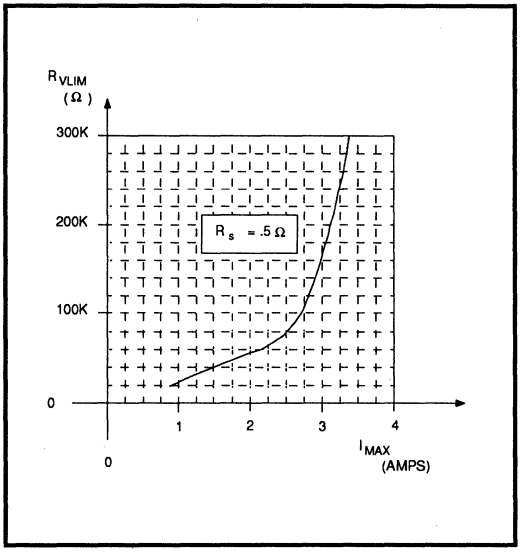



**FIGURE 7: RVLIM To VREF Typical Motor Current Limit**

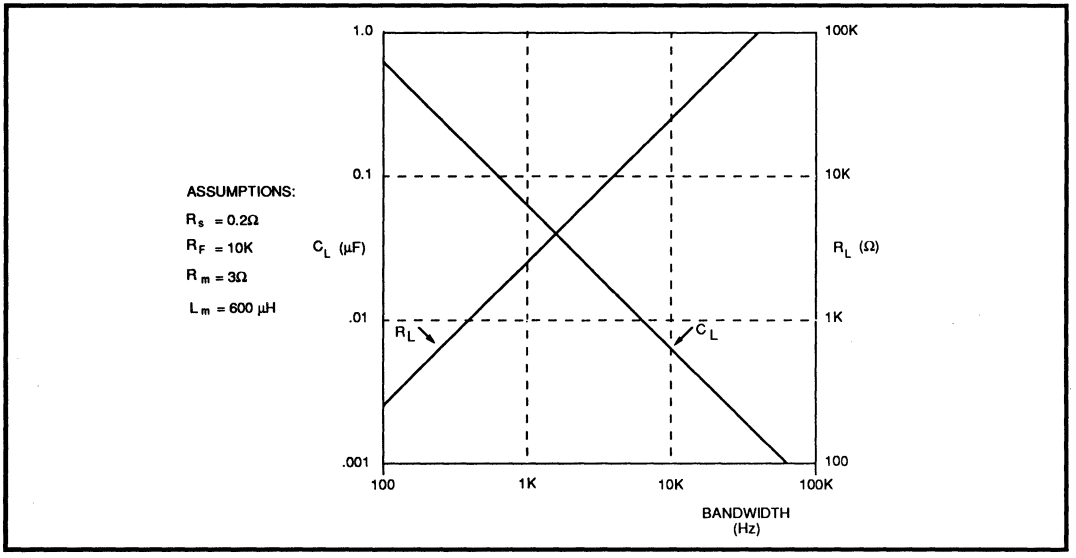



**FIGURE 8: Typical Motor Driver Compensation**

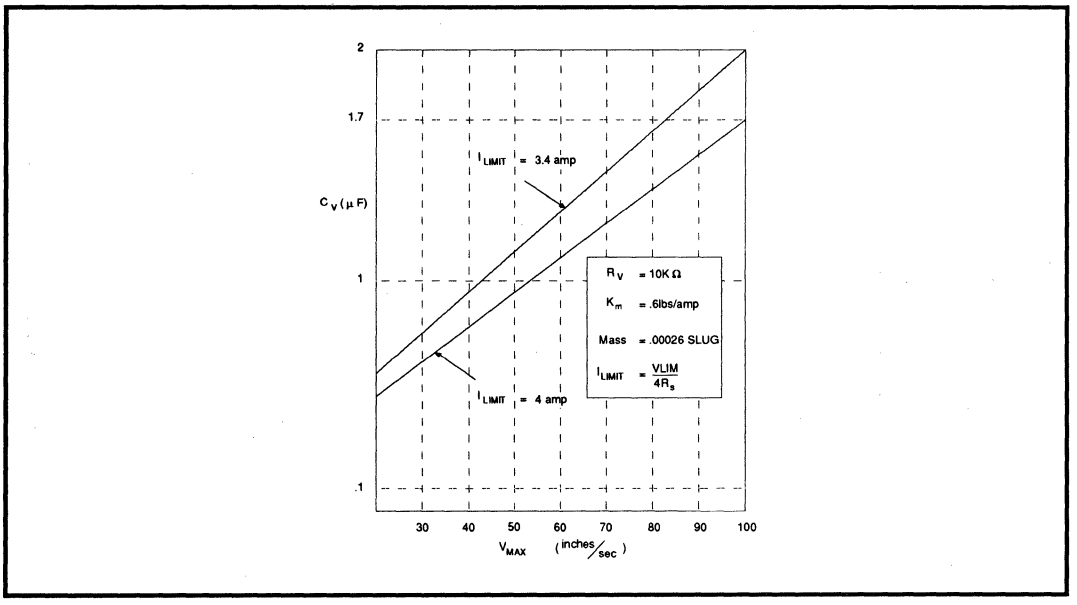



**FIGURE 9: Typical Motor Velocity Limit**

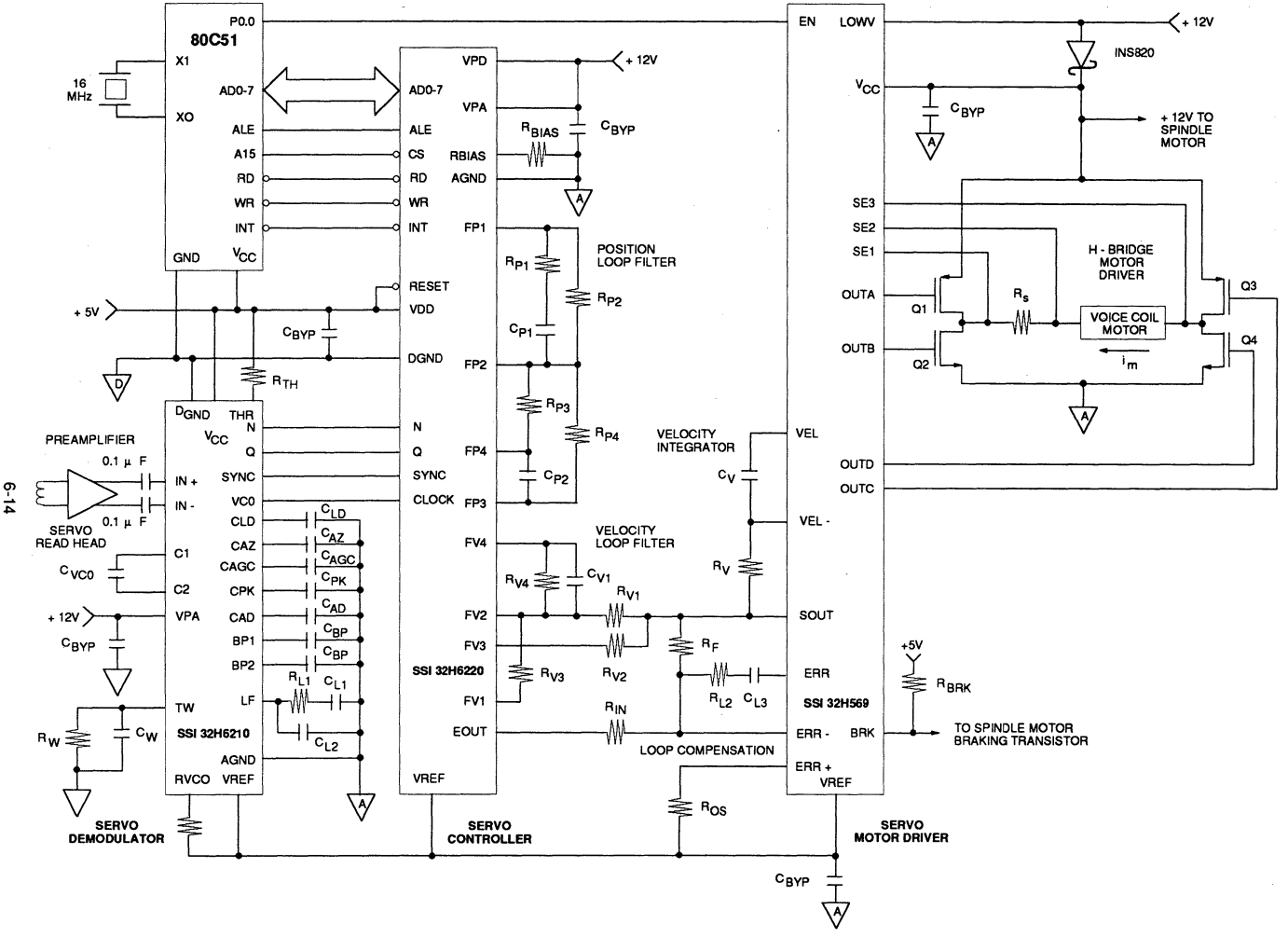
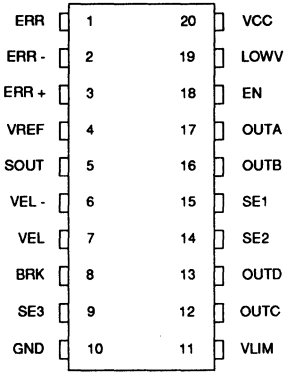



**FIGURE 10: Complete Example of Servo Path Electronics Using the SSI 32H6210/ 6220/ 569**

## PACKAGE PIN DESIGNATIONS

(Top View)




**20-Pin SO, DIP**

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## ORDERING INFORMATION

| PART DESCRIPTION | ORDER NO. | PKG. MARK |
|---|---|---|
| SSI 32H569, Servo Motor Driver | | |
| 20-Pin DIP | 32H569-CP | 32H569-CP |
| 20-Pin SOL | 32H569-CL | 32H569-CL |



Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 573-6000, FAX (714) 573-6914

 

**Notes:**

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A TDK Group Company

# SSI 32H4633
## Hybrid Servo & Spindle Controller
## Preliminary Data

December 1992

## DESCRIPTION

The SSI 32H4633 is a CMOS monolithic integrated circuit housed in a 100-pin QFP and operates on a single +5V supply. In addition to supporting Winchester disk drives with embedded servo sectors and dedicated servo surface, it contains all timing and control functions necessary to start, drive, and brake a 3-phase, 4/8/12 pole brushless DC spindle motor without sensors. It also provides an 8-bit A/D converter at a conversion rate up to 250 kHz and a Motorola/Intel compatible bus interface (Motel) to popular microcontrollers such as the 8051 and 68HC11. The features for each functionally different section are summarized in the following:

## FEATURES

### Servo Head Positioning Control

- Servo control for Winchester disk drives with hybrid servo head positioning systems
- For use in microprocessor-based digital servo applications
- Accepts quadrature position signals N, Q from a dedicated servo demodulator
- 12-bit double-buffered cylinder crossing counter for dedicated seek algorithms
- Timing controller for embedded servo position burst sampling
- Peak detect and sample/hold circuits for up to four embedded servo bursts
- H-bridge MOSFET predriver for linear and rotary voice coil motor
- Class B linear mode and constant voltage retract mode
- Active head retract on power failure

### Spindle Motor Speed Control

- 3-phase 4/8/12 pole bipolar/unipolar operation without need for sensors
- Precision speed regulation at 5400 RPM, with ± 0.018% speed resolution
- "At speed" indication
- Motor peak current limiting function
- Pulse amplitude modulation (PAM) for bridge MOSFET drivers
- Dynamic braking function on power failure

### Data Acquisition and Microprocessor Bus Interface

- Motel bus interface compatible with 8051 and 68HC11
- Ten internal registers and address decoding
- Internal 250 kHz 8-bit A/D and D/A converters

### General Functions

- Voltage fault detection for up to two supply voltages
- Write gate guarding
- Low power CMOS design
- 100 pin QFP package

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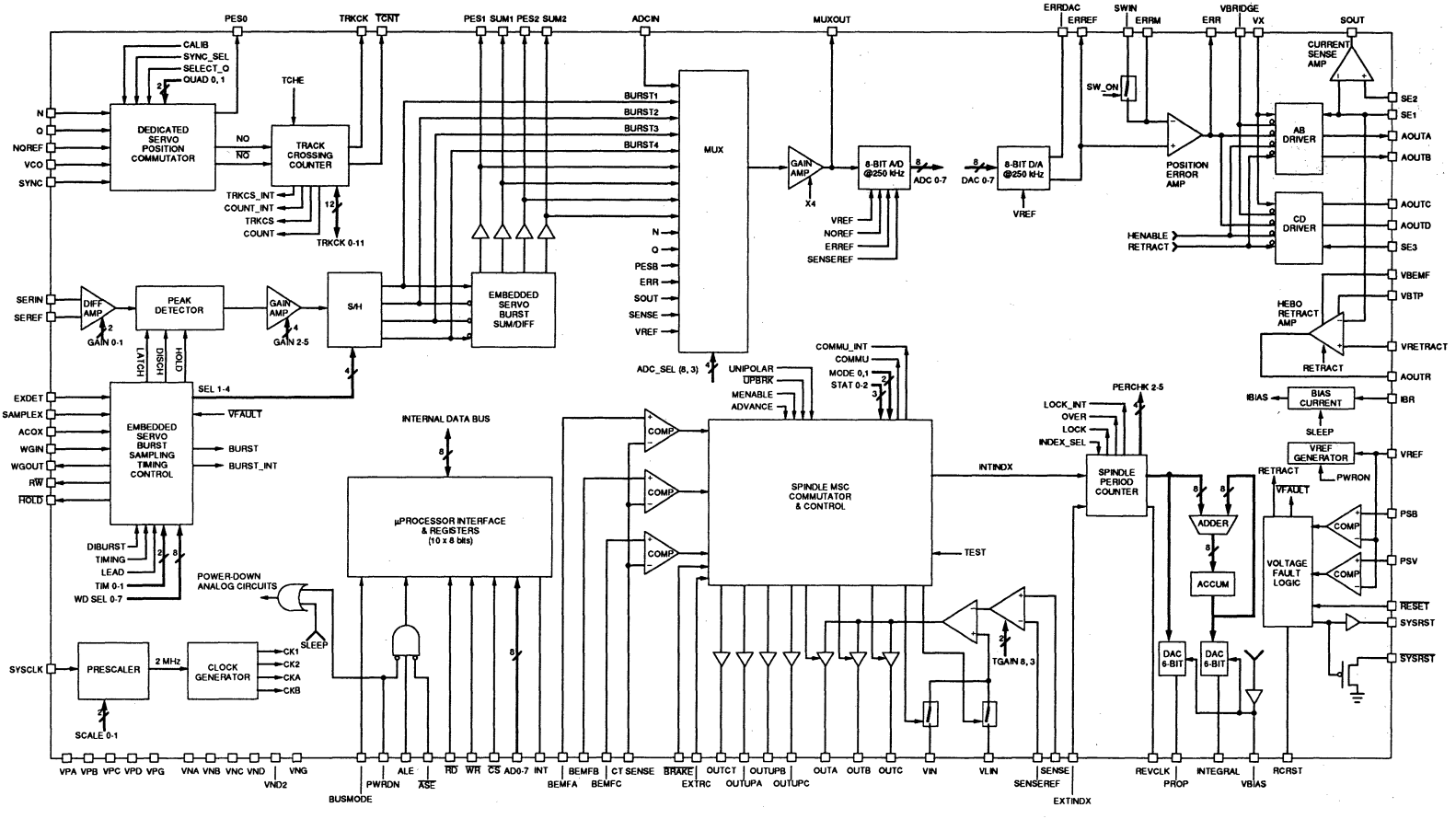


**FIGURE 1: SSI 32H4633 Block Diagram**

## FUNCTIONAL DESCRIPTION

As shown in Figure 1, the SSI 32H4633 can be divided into three major sections: servo head positioning control, spindle motor speed control, data acquisition and microprocessor bus interface.

### SERVO HEAD POSITIONING CONTROL

The SSI 32H4633 is intended for a servo head positioner for Winchester disk drives with both embedded servo sectors and a dedicated servo surface. The servo head positioning control section contains the following functions:

1. Dedicated servo position processor
2. Embedded servo burst amplitude processor
3. Embedded servo burst timing controller
4. Servo position error amplifier
5. H-bridge MOSFET predriver
6. Actuator current sense
7. Voltage fault detection and servo head retract

Figure 2 shows dedicated servo position processor. Figure 3 shows embedded servo burst amplitude processor with embedded servo burst timing controller. Figure 4 shows servo position error amplifier, H-bridge MOSFET predriver, actuator current sense. Figure 5 shows voltage fault and servo head retract logic.

### DEDICATED SERVO POSITION PROCESSOR

The dedicated servo position processor receives quadrature position information from a servo demodulator, such as SSI 32H6210, through analog inputs N, Q and NQREF. The NQREF is applied to establish a DC reference level for N and Q samples. N and Q are sampled at the falling edge of SYNC. The SYNC frequency, which is the servo frame rate on the dedicated servo surface, is generated from the servo demodulator and is no more than 500 kHz. The VCO provides the necessary clock signal to sample N and Q signals. The timing relationship among VCO, SYNC and N, Q is indicated in Figure 2. If it is not necessary to synchronize to N, Q samples, the SYNC input must be grounded and the SYNC SEL bit in the SERVO CONTROL register set HIGH. In this case, the SYSCLK input will be divided down internally to generate the frame rate to sample N and Q signals. The position processor compares N with both Q and -Q to generate digital signals NQ (N>Q) and $N\overline{Q}$ (N>-Q). Since N and Q signals span four tracks per period, NQ and $N\overline{Q}$ provide additional information on which track the head is positioned. In order to produce the position error signal PES0, the position processor selects N, Q, -N or -Q, based upon either the values of bits QUAD0 and QUAD1 when SELECT Q is enable; or the values of the digital signals NQ and $N\overline{Q}$ when SELECT Q is disabled. Note that the analog inputs N and Q to the position processor will switch to the DC reference level, NQREF, when the CALIB bit in the HYBRID SERVO CONTROL register is enabled. This allows calibrating the internal offset of the position error signal, PES0. For digital servo applications, N, Q and PES0 are provided to the internal multiplexed 8-bit A/D converter under µP control.

The SSI 32H4633 supports both hardware and software track counting techniques. The software track counting technique interfaces with bits NQ, $N\overline{Q}$ and TRKCS in the SERVO STATUS register. On each track crossing, either NQ or $N\overline{Q}$ changes state.

An internal timing hysteresis can be provided to prevent multiple state changes on NQ, $N\overline{Q}$ and TRKCS at low head velocities by setting the bit TCHE in the EMBEDDED SERVO GAIN CONTROL register. The TRKCS bit will be reset LOW when the SERVO STATUS REGISTER is read by the µP. The hardware track technique interfaces with TRKCK, an output clock intended to drive a hardware counter such as is available in the Intel 8051 family. TRKCK is normally LOW and pulses HIGH once whenever a track boundary is crossed. A 12-bit double-buffered down counter with programmable loading capability is implemented to aid seek algorithms. The counter is decremented at the LOW-TO-HIGH transition of TRKCK and the register is updated at the HIGH-TO-LOW transition of TRKCK. The 12-bit counter register stops updating after the LSB is read. This ensures consecutive reads provide information that corresponds to a single track. Therefore, one should read the LSB and then the MSB without exception. The counter will produce a LOW level on $\overline{TCNT}$ when the terminal count is reached. $\overline{TCNT}$ remains LOW until the counter is loaded with a new initial value.

## EMBEDDED SERVO BURST AMPLITUDE PROCESSOR

The embedded servo burst amplitude processor extracts the fine head position error information from the embedded servo bursts. The circuit acquires up to 4 burst amplitudes BURST1, BURST2, BURST3, and BURST4 from a read data channel, such as the SSI 32P4620, through analog inputs SERIN and SEREF. The SEREF is applied to establish a DC reference level for the full wave-rectified analog signal SERIN.
To accommodate a wide range of servo burst amplitudes, the differential signal between SERIN and SEREF is scaled by a 2-bit programmable gain amplifier under µP control. The gain of the differential amplifier ranges from -6 dB to 3 dB as defined in the EMBEDDED SERVO GAIN CONTROL register. The output of the differential amplifier is then provided to a peak detector which captures the peak voltage within a time interval derived from the internal timing controller or an external timing source through SAMPLEX. The peak voltage is further scaled by a 4-bit programmable gain amplifier under µP control. Thus the gain error introduced by the peak detector can be accurately corrected with this programmable gain amplifier. The gain adjustment ranges from 0 dB to 3 dB in 0.2 dB steps, as defined in the EMBEDDED SERVO GAIN CONTROL register. Each of the following four S/H circuits transfers and holds the scaled peak voltages onto their respective holding capacitors during a time interval defined by the internal timing controller or an external timing source through ACQX. The outputs of S/H circuits, BURST1, BURST2, BURST3, and BURST4, are provided to the 8-bit A/D converter under µP control. Note that the timing windows to acquire the scaled peak voltages can be configurated in any order, as defined in the EMBEDDED SERVO TIMING WINDOW CONTROL register. Therefore, the µP can mix and commutate servo bursts to accommodate for a variety of servo burst formats and maintain the position error signal in a proper polarity. The timing controller also issues a timing signal to discharge the captive voltage for each servo burst.

The captive signals are provided to two difference circuits to extract the differential signals between BURST1, BURST2 and BURST 3, BURST4, respectively. Typically, these differential signals define the distance between the read head and the center of a data track and one of them should be zero while the read head is at the center of a data track. These outputs, available externally on PES1 and PES2, are provided to the 8-bit A/D converter under µP control. Also, two summers add BURST1, BURST2 and BURST3, BURST4, respectively, and their outputs at SUM1 and SUM2 are provided to the 8-bit A/D converter as well.

## EMBEDDED SERVO BURST TIMING CONTROLLER

The embedded servo burst timing controller generates all the timing signals to sample the position bursts, as shown in Figures 3 and 4. These timing signals control the discharge, sample, and hold of the peak detector and the four S/H circuits. The EMBEDDED SERVO TIMING WINDOW CONTROL register can be programmed by the µP to select and sample the servo burst pairs in any order. The number of servo position bursts supported are either two or four. The DIBURST bit in the SERVO CONTROL register, when set HIGH, configures the internal timing controller to sample only two servo position bursts. When reset, four servo position bursts are sampled. During position burst sampling, $\overline{\text{HOLD}}$ and $\overline{\text{RW}}$ will be asserted and WGOUT held LOW.

An external timing controller may be used to provide all the timing signals for the discharge, sample, and hold of the peak detector and the four S/H circuits by setting the TIMING bit HIGH in the SERVO CONTROL register. Usually, in this mode, an external timing controller ASIC will be required to provide the timing signals at SAMPLEX and ACQX for servo position burst sampling while the internal servo timing controller is disabled.

## SERVO POSITION ERROR AMPLIFIER

The servo driver has two modes of operation, linear and retract. The retract mode is activated by a power supply failure or when the control signal $\overline{\text{RESET}}$ is LOW. Otherwise the driver operates in linear mode. During linear operation, the microcontroller acquires servo burst amplitudes and analyzes them to establish a position error signal. This signal travels through an 8-bit D/A converter and is applied to an amplifier whose three connections, ERRM, ERREF and ERR, are available externally. External RC components may be used to establish the gain and bandwidth of this amplifier. Additional analog input via SWIN may be provided to this amplifier by setting the SW ON bit in the SERVO CONTROL register.

## FUNCTIONAL DESCRIPTION (continued)

### H-BRIDGE MOSFET PREDRIVER

The error signal ERR generated from the position error amplifier drives two precision differential amplifiers, each with a gain of 15. The differential amplifier outputs, AOUTA, AOUTB, AOUTC and AOUTD drive an external MOSFET bridge powered by VBRIDGE. Feedback from the MOSFET drain terminals via sense inputs SE1 and SE3 allow the differential amplifier gains to be established precisely. The voice coil actuator and a current sense resistor are connected in series between SE1 and SE3. Included in the output control circuitry is a crossover protection function which ensures class B operation by permitting only one MOSFET in each leg of the bridge to be in conduction. The crossover circuit can be adjusted for different MOSFET threshold voltages with a resistor connected to VX. The crossover circuitry can be commanded by the µP to shut down the MOSFET drivers and thus remove current to the external bridge.

### MOTOR CURRENT SENSE

Motor current is sensed by a small resistor placed in series with the actuator. The voltage drop across the resistor is level-shifted and amplified by a differential amplifier with a gain of 4. The resulting signal, SOUT, is proportional to actuator current. This signal is externally fed back to the position error amplifier so that the error signal ERR represents the difference between the desired and actual actuator currents.

### VOLTAGE FAULT DETECTION AND SERVO HEAD RETRACT

A voltage fault detector which can monitor up to two voltage supplies is included to prevent the actuator from responding to a false error signal during a power failure. Retract mode is started when a power supply failure is sensed by the PSB or PSV comparators or when $\overline{\text{RESET}}$ is pulled LOW externally. During retract, a constant voltage is applied across the actuator in order to cause a constant velocity head retraction. This is accomplished by applying the voltage stored on VBYP to AOUTD and by driving AOUTR with an amplifier that monitors SE1. The amplifier is powered by VBEMF. During retract, VRETRACT is biased by an internal voltage reference and determines the retract voltage. At other times, power is saved by disconnecting VRETRACT from the voltage reference and letting it be pulled to VBEMF by a high value resistor. External components (a diode, for instance) can be connected between VRETRACT and ground to modify the retract voltage.

An open-drain output, $\overline{\text{SYSRST}}$, which is active LOW while the servo driver is in retract mode, is provided for spindle motor braking. An external RC delay may be used to defer braking until the head is retracted. The amount of $\overline{\text{SYSRST}}$ delay is determined by the external capacitor which is connected to the pin, RCRST.

### SPINDLE MOTOR SPEED CONTROL

A functional block diagram for the spindle motor control is shown in Figure 1. In conjunction with several external components, the spindle motor speed control provides the starting, accelerating, and precise rotational speed regulation functions. The circuit will control 4, 8, or 12 pole brushless DC motors without the need for Hall sensors. It will operate in either bipolar or unipolar drive mode. Control, configuration, and status monitoring are handled by the µP. The complete speed control loop is contained in the circuit and the µP is only required during start and to monitor status.

### SPINDLE MOTOR START-UP

Motor starting is accomplished with the µP utilizing various features contained in the motor speed control circuitry. The µP can write to the commutation counter and set it to a predetermined value with STATE0, STATE1, STATE2 bits. The counter can then be incremented with the ADVANCE bit which also excludes internal commutations when set HIGH. Bits COMMU, PERCHK 2, 3, 4, 5 provide feedback to the µP on motor activity. The µP can enable the drivers with MENABLE and UNIPOLAR bits as required, as well as cause a "soft" brake with $\overline{\text{UPBRK}}$.

Under µP control, initial open-loop commutation sequence is provided to the commutation logic which thereby advances and accelerates the spindle motor. The start-up process settles the motor initially by selecting the bits STATE0, STATE1, STATE2 in the SPINDLE CONTROL register to energize a proper motor winding. Motor current is enabled by setting the MEANABLE bit in the SPINDLE CONTROL register. The commutation state is advanced by providing ADVANCE pulses in the SPINDLE CONTROL register. The period of the ADVANCE pulses will be based upon the motor and load characteristics and decreased

gradually during the acceleration of the motor. The µP may look at the COMMU bit in the SPINDLE STATUS register for feedback indicating whether the motor has achieved a sufficient speed. Once the motor has achieved a sufficient speed, the µP will cease generating ADVANCE pulses and motor starting is thus completed.

### SPINDLE MOTOR SPEED REGULATION

Motor speed regulation is accomplished with mixed analog and digital techniques, converting a motor speed error derived from a reference clock and a period counter into a voltage. The voltage translates into a motor current across the current sense resistor regulating the motor speed. The speed regulation loop consists of a period counter, proportional and integral channels, two 6-bit D/A converters and a linear transconductance amplifier.

In operation, the motor speed error is determined by measuring the period of each revolution with a 500 kHz clock signal. Period resolution is therefore 2 microseconds with the desired period being 5555 counts (11.11 milliseconds or 5400.54 RPM). Motor rotor position is determined by monitoring the coil voltage of the winding that is not presently being driven by the drivers. The back-emf at the coil in conjunction with the state of the output drivers indicates rotor position. The back-emf is compared to a reference at CTSENSE and initiates "commutation events" when the appropriate comparison is made. The commutation is the sequential switching of the drive current to the motor windings. Since the back-emf comparison event occurs prior to the time when optimum commutation should occur, it is thus required to delay actual commutation by a predetermined time after the comparison. The commutation delay is provided by a non-retriggerable one-shot circuit wherein the time delay is a function of external RC timing components connected at EXTRC. Because commutation of the motor windings typically results in large transient voltages which could falsely indicate "commutation events," the one-shot circuit also provides a "noise filter" function which holds off retriggering further and blanks the back-emf comparison events for a period of time (approximately one half the commutation delay) after commutation. The commutation states are defined in the SPINDLE CONTROL register.

The period counter is loaded with a count of 5555 initially, and period measurement results in residual counts (ideally zero) in the period counter as it counts down during the index-to-index time interval. The residual count is fed to the proportional D/A converter (5 bit plus sign) whose output is provided at PROP. No period error will output half of VBIAS at PROP, too short a period will output a value less than half of VBIAS, and too long a period will output a value greater than half of VBIAS depending on the amount of error.

When the residual count is within ± 15 counts of zero, the motor is indicated as "in lock." The lower eight bits of the period counter are fed to an accumulator which adds the present period residue to the previous accumulation thus accomplishing an integrating effect to force the speed error to zero over time. The upper six bits of the accumulator are fed to the integral DAC whose output is INTEGRAL. Gross period errors will cause PROP and INTEGRAL to saturate at the appropriate extreme to achieve the maximum corrective control voltage.

The outputs at PROP and INTERGRAL are connected to VIN with an external resistor network. The resistor values should be selected to set the required loop response based upon motor requirements. The input VIN is the non-inverting input of the linear transconductance amplifier which uses the lower driver transistor that is presently active per the commutation state. An external resistor is used to sense the current flowing through the drive transistor drain (and hence the motor coil current). The voltage across the sense resistor, the difference between SENSE and SENSEREF, is amplified by a programmable gain stage and fed to the inverting input of the transconductance amplifier. The gain of the programmable amplifier is determined by TGAIN0 and TGAIN1 bits.

Motor speed control includes a speed range check circuit, which provides in the SPINDLE STATUS register a LOCK status bit, when the motor is at the target speed within ±0.27%, along with OVER status bit, when the motor is over or under the target speed. The LOCK and OVER status bits are available to the µP for diagnostics and spindle fault conditions.

Additional low-speed period measurement data is available to the µP as the PERCHK2,3,4,5 bits in the SPINDLE STATUS register.

## FUNCTIONAL DESCRIPTION (continued)

### MOTOR PEAK CURRENT LIMITING

When the period error exceeds 256 counts too slow, the voltage at VLIM is selected as the control voltage in lieu of VIN. VLIM is to be used to set the motor peak current during start-up and acceleration.

### MOTOR BRAKING

Fault conditions on power supplies and internal voltage reference generator will trigger an internal retract condition. The internal retract condition will cause all predriver outputs to the states which will turn the driver transistors off, allowing the motor to coast. $\overline{\text{BRAKE}}$ typically has a capacitor to ground attached and is connected to pin $\overline{\text{SYSRST}}$ via a resistor. $\overline{\text{SYSRST}}$ goes LOW in the retract condition, and thus $\overline{\text{BRAKE}}$ will go LOW after the RC delay. When $\overline{\text{BRAKE}}$ goes LOW, all lower drivers are activated to achieve dynamic braking of the motor. The circuitry for these operations is powered by the back-emf of the spindle motor and will operate without either 5 or 12 volt supply.

Dynamic braking can also be activated under µP control by setting $\overline{\text{UPBRK}}$ to LOW in the SPINDLE CONTROL register. During dynamic braking, the control loop is opened.

Two other motor speed control functions related to other circuit functions in the SSI 32H4633 are SLEEP mode and internal bias current. Two modes of SLEEP are provided for the SSI 32H4633, but the effect on the motor speed control is the same for both modes, i.e., all analog circuitry is de-biased, the clock is disabled, the upper driver outputs become logic HIGH (to turn off all upper drivers including the center tap if used), and the lower driver outputs become logic HIGH. The internal bias currents for analog functions are set by an external resistor connected between IBR and ground. A 22.6 KΩ, ±1% resistor should be used for proper operations.

### EXTERNAL INDEX APPLICATION

Normal operation is performed with an internal index signal derived from the commutation counter (scaled via the MODE0 and MODE1 bits based upon the number of motor poles). The period of the index signals is measured and controlled by the circuit to result in a rotational rate of 5400 RPM. Within the range from 5384.9 to 5415.1 RPM, the spindle will be "in lock."

After the motor is started and accelerated to speed (LOCK bit HIGH), an external index signal may be selected. Applying external index pulses at a rate within the lock range and setting INDEX SEL bit to HIGH will start the following sequence:

The circuit will complete the period measurement of the latest internal index period and then begin to measure the time between the last internal index and the next external index pulse. This will most likely be shorter than the nominal assuming the two events are asynchronous. If the period measured is not within 4.6% of the expected value, 11.11 milliseconds, the proportional and integral D/A converters will not be updated with a new correction value but will continue to output the previous value. The LOCK bit will be set to LOW indicating "out of lock." The next period measured will be between the first and second external index pulses and will presumably be within the lock range so that LOCK will be set to HIGH. If the period is within 4.5% of the desired value, the proportional and integral D/A converters will be updated. Similarly, during operation with external index, a missing index pulse would look like a gross speed error and no update on proportional and integral D/A converters will take place. The µP must perform the corrective actions in such cases, by examining LOCK bit, the PERCHK2,3,4,5 bits, and the source of the (missing) index pulses. A single missing index should require no action other than checking that LOCK returns to HIGH (in lock) in the next interval.

### DATA ACQUISITION AND MICROPROCESSOR BUS INTERFACE

Figure 1 shows data acquisition circuits along with the microprocessor bus interface. To facilitate microprocessor-based servo applications, the SSI 32H4633 contains a high-speed 8-bit A/D converter at a conversion rate up to 250 kHz, an 8-bit D/A converter, and Motel bus interface compatible with commonly used 12 MHz 8051 and 8 MHz 68HC11. The A/D converter can be multiplexed to sixteen different analog inputs by programming the ADC_SEL0, ADC_SEL1, ADC_SEL2 and ADC_SEL3 bits in the ADC ADDRESS register by the µP. The analog inputs can be scaled by a gain of 4 by setting the X4 bit HIGH. The output of the gain stage is available externally at MUXOUT for diagnostics. The A/D converter runs synchronously with the internal 500 kHz clock which is used for various circuits on the SSI 32H4633. Therefore, there would be a maximum of 2

microseconds of latency between a conversion request and the actual start of the conversion. Conversion is started by reading the A/D output register. The output is coded in 2's complement. Note that different voltage references corresponding to one half of the A/D full scale are used for different analog inputs as defined in the ADC ADDRESS register.

Similarly, the D/A converter runs synchronously with the internal 500 kHz clock and conversion is started by writing to the D/A input register. The output at ERRDAC is referenced to ERREF and is held constant between conversions.

The "Motel" interface to both Motorola and Intel µP's is provided for a direct connection to the SSI 32H4633. Three bus control signals are interpreted differently based upon the type of µP being used. The pin BUSMODE should be tied to HIGH for an Intel bus interface. The table below illustrates how both µPs connect to the SSI 32H4633. The $\overline{ASE}$ pin gates the AL/ASE input and can be used to shut off the ALE/AS to minimize noise on chip when the µP interface is not active. The $\overline{CS}$ pin performs a similar function on the rest of the µP bus inputs. The timing diagrams for Intel and Motorola µP interface are shown in Figures 5 and 6, respectively.

| Intel | Motorola | 32H4633 |
|---|---|---|
| ALE | AS | ALE |
| $\overline{RD}$ | DS;E; or Clock Phase 2 | $\overline{RD}$ |
| $\overline{WR}$ | R/$\overline{W}$ | $\overline{WR}$ |

## REGISTER DESCRIPTIONS

The SSI 32H4633 contains ten 8-bit internal registers which provide control, option select and status monitoring. The registers are addressed with a 4-bit register address which is latched from inputs at AD0, AD1, AD2, and AD3 on the falling edge of ALE. The registers from 0 to 5 are read/write memory, the registers from 6 to 9 are write only. The registers are summarized in Table 1.

**TABLE 1: SSI 32H4633 Internal Registers**

| ADDRESS | TYPE | REGISTER NAME |
|---|---|---|
| 0 | R/W | Interrupt Control/Status |
| 1 | R/W | Spindle Control/Status |
| 2 | R/W | Servo Control/Status |
| 3 | R/W | ADC Address/Data |
| 4 | R/W | Track Count LSB |
| 5 | R/W | Track Count MSB & Hybrid Servo Control |
| 6 | W | Error DAC Data |
| 7 | W | Embedded Servo Gain Control |
| 8 | W | Transconductance, Prescaler and Mode Control |
| 9 | W | Embedded Servo Timing Window Control |

### INTERRUPT CONTROL/STATUS REGISTER

Address: 0 Access: Read/Write Reset: 00
Register contents when Written to enable or disable interrupt events:

| BIT | NAME | DESCRIPTION |
|---|---|---|
| 0 | COMMU INT | When set HIGH, interrupt is enabled on a state change of the back-emf commutation clock COMMU. |
| 1 | LOCK INT | When set HIGH, interrupt is enabled on a state change of the spindle speed lock. |
| 2 | BURST INT | When set HIGH, interrupt is enabled on the embedded servo position bursts ready. |
| 3 | TRKCS INT | When set HIGH, interrupt is enabled on each track crossing. |
| 4 | COUNT INT | When set HIGH, interrupt is enabled on the terminal count ($000_H$) of the track crossing counter. |
| 5,6 | - | Undefined. |
| 7 | MST INT | When set HIGH, the microprocessor signal $\overline{INT}$ is enabled. |

Register contents when Read

| BIT | NAME | DESCRIPTION |
|---|---|---|
| 0 | COMMU INT | Active high indicates a state change of the back-emf commutation clock COMMU. |
| 1 | LOCK INT | Active high indicates a state change of the spindle speed lock. |
| 2 | BURST INT | Active high indicates that the embedded servo position bursts are ready. |
| 3 | TRKCS INT | TRKCS INT is asserted when NQ or $N\overline{Q}$ changes state, i.e., on each track crossing. |
| 4 | COUNT INT | COUNT INT is asserted when the terminal count ($000_H$) of the track crossing counter is reached. |
| 5,6 | - | Undefined. |
| 7 | MST INT | Active high indicates that one or more interrupts are pending. |

Each interrupt event status is reset when the µP reads the corresponding status register. Specifically, interrupt events COMMU INT and LOCK INT are reset whenever the SPINDLE STATUS register (ADDRESS=1) is read. Interrupt events TRKCS INT, COUNT INT and BURST INT are reset whenever the SERVO STATUS register (ADDRESS=2) is read. All interrupt events may be read as interrupt status regardless of their corresponding interrupt mask settings. The interrupt control register determines which event will actually cause a latched assertion of the µP signal $\overline{INT}$. Note that the MST INT is a master enable which disables all interrupt events from asserting $\overline{INT}$ when active low. Also, when read, MST INT indicates if any mask enabled interrupt events are still pending for service and reflects the internal state of the µP signal $\overline{INT}$.

### SPINDLE CONTROL/STATUS REGISTER

Address: 1 Access: Read/Write Reset: 00
Register contents when Written:

| BIT | NAME | DESCRIPTION |
|---|---|---|
| 0 | $\overline{\text{UPBRK}}$ | When set LOW, dynamic braking will be initiated where upper drivers are disabled and lower drivers are activated. |
| 1 | UNIPOLAR | This bit is set HIGH when unipolar motor is used. For unipolar motors, all upper drivers are disabled and OUTCT is activated. |
| 2 | INDEX SEL | When set HIGH, the input signal at EXTINDX, one pulse per revolution, is selected as the spindle speed indicator. Otherwise, the internal revolution clock developed from the back-emf sensing circuit is selected. |
| 3 | MENABLE | Driver Enable Control. When set LOW, both upper and lower drivers are turned off to deny power to the motor. This overrides all other output conditions. When set HIGH, drive outputs are activated per the state of the commutation state counter. |

Register contents when Written:

| BIT | NAME | DESCRIPTION |
|---|---|---|
| 4 | ADVANCE | Each LOW-TO-HIGH transition advances the edge-trigged commutation state counter by one. When set HIGH, the internal clock (derived from the back-emf events) to the commutation state counter is inhibited. When set LOW, normal operation is resumed. |
| 5<br>6<br>7 | STAT0<br>STAT1<br>STAT2 | Preset Commutation State. During start-up, the commutation state counter will be preset to the state decoded by these 3 bits per table 2: |

**TABLE 2:**

| STAT2 | STAT1 | STAT0 | OUTA | OUTB | OUTC | OUTUPA | OUTUPB | OUTUPC |
|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | OFF | ON | OFF | ON | OFF | OFF |
| 0 | 0 | 1 | OFF | OFF | ON | ON | OFF | OFF |
| 0 | 1 | 0 | OFF | OFF | ON | OFF | ON | OFF |
| 0 | 1 | 1 | ON | OFF | OFF | OFF | ON | OFF |
| 1 | 0 | 0 | ON | OFF | OFF | OFF | OFF | ON |
| 1 | 0 | 1 | OFF | ON | OFF | OFF | OFF | ON |
| 1 | 1 | 0 | Normal Operation | | | | | |
| 1 | 1 | 1 | Normal Operation | | | | | |

**SPINDLE CONTROL/STATUS REGISTER** (continued)

Register contents when Read:

| BIT | NAME | DESCRIPTION |
|---|---|---|
| 0 | LOCK | Active high indicates that the spindle motor is within ±15 counts of the nominal value (5555 counts with the counter clocked at 500 kHz) or ±0.27%. The corresponding interrupt event LOCK INT will be reset whenever this register is read by the µP. |
| 1 | OVER | Active high indicates that the spindle speed is faster than the nominal value; active low indicates that the spindle speed is slower than the nominal value. |
| 2 | COMMU | Back-emf commutation clock divided by 2. Each state change of COMMU indicates that the commutation state counter has advanced by one. The corresponding interrupt event COMMU INT will be reset whenever this register is read by the µP. |
| 3<br>4<br>5<br>6 | PERCHK5<br>PERCHK4<br>PERCHK3<br>PERCHK2 | Spindle Speed Check Bits. These bits are used to estimate the spindle speed if it is slower than the nominal value.<br>**P2 P3 P4 P5 SPEED,rps**<br>0 0 0 0 SPEED ≥65<br>1 0 0 0 51≤ SPEED ≥65<br>1 1 0 0 36≤ SPEED ≥51<br>1 1 1 0 22≤ SPEED ≥36<br>1 1 1 1 SPEED ≥22 |
| 7 | Undefined | |

6

### SERVO CONTROL/STATUS REGISTER

Address: 2 Access: Read/Write Reset: 00
Register contents when Written:

| BIT | NAME | DESCRIPTION |
|---|---|---|
| 0 | HENABLE | H-bridge Driver Enable. When set HIGH, H-bridge MOSFET drivers are enabled. |
| 1 | SW ON | When set HIGH, the analog switch between the ERRM and SWIN pins is turned on. |
| 2 | - | Undefined |
| 3 | TIMING | Timing Controller Disable. When set HIGH, the timing signals required to sample/hold embedded servo position bursts are derived from an external timing source via SAMPLEX and ACQX. Otherwise, the internal timing controller is used. |
| 4 | DIBURST | When HIGH, only two servo bursts, BURST1 and BURST2 are sampled. Otherwise, four servo burst amplitudes are sampled. |
| 5 | LEAD | Write Gate Guard Lead Enable. When set HIGH, the write gate guard is enabled one burst period prior to the sampling of the first position burst field. Otherwise, the write gate guard is enabled essentially at the same time as the sampling of the first position burst field. |
| 6<br>7 | TIM0<br>TIM1 | Burst Field Length Select. These two bits define the time duration of each embedded servo position burst field per table below:<br>**TIM1 TIM0 Burst Duration, μsec**<br>0 0 5<br>0 1 6<br>1 0 8<br>1 1 10 |

Register contents when Read:

| | | |
|---|---|---|
| 0 | - | Undefined |
| 1 | - | Undefined |
| 2 | BURST | Active HIGH indicates that the embedded servo position bursts are ready. |
| 3 | TRKCS | Active HIGH indicates a track crossing, i.e., NQ or $N\overline{Q}$ changes state. |
| 4 | COUNT | Active HIGH indicates that the terminal count ($000_H$) of the track crossing counter is reached. |
| 5 | - | Undefined |
| 6 | NQ | Active HIGH when N>Q and reset otherwise. |
| 7 | $N\overline{Q}$ | Active HIGH when N>-Q and reset otherwise. |

The corresponding interrupt events TRKCS INT, COUNT INT and BURST INT will be reset when this register is read by the μP. Also, the TRKCS, COUNT and BURST bits in this register are reset after being read.

### ADC ADDRESS/DATA REGISTER

Address: 3 Access: Read/Write Reset: Undefined

Description: When Written, the least significant 4 bits of the register define the analog input to the 8-bit A/D converter. After conversion, the 8-bit digital word of the analog input is stored into the register.

Register contents when Written:

| BIT | NAME | DESCRIPTION |
|---|---|---|
| 0<br>1<br>2<br>3 | ADC SEL0<br>ADC SEL1<br>ADC SEL2<br>ADC SEC3 | A/D Converter Input Select. These 4 bits define the analog input to the A/D converter per table below: |
| 4 | X4 | X4 Enable. When set HIGH, the analog input to the A/D converter will be multiplied by 4 before converted into a digital value. |
| 5,6,7 | - | Undefined |

| BIT3 | BIT2 | BIT1 | BIT0 | ADC INPUT | ADC Vref |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | BURST1 | VREF |
| 0 | 0 | 0 | 1 | BURST2 | VREF |
| 0 | 0 | 1 | 0 | BURST3 | VREF |
| 0 | 0 | 1 | 1 | BURST4 | VREF |
| 0 | 1 | 0 | 0 | PES1 | VREF |
| 0 | 1 | 0 | 1 | PES2 | VREF |
| 0 | 1 | 1 | 0 | PES0 | VREF |
| 0 | 1 | 1 | 1 | N | NQREF |
| 1 | 0 | 0 | 0 | Q | NQREF |
| 1 | 0 | 0 | 1 | ERR | VREF |
| 1 | 0 | 1 | 0 | SOUT | VREF |
| 1 | 0 | 1 | 1 | SENSE | SENSEREF |
| 1 | 1 | 0 | 0 | ADCIN | VREF |
| 1 | 1 | 0 | 1 | VREF | VREF |
| 1 | 1 | 1 | 0 | SUM1 | VREF |
| 1 | 1 | 1 | 1 | SUM2 | VREF |

Register contents when Read:

| BIT | NAME | DESCRIPTION |
|---|---|---|
| 0..7 | ADC0..7 | Digital output of the A/D converter in 2's complement format. ADC7 corresponds to the sign bit. |

### TRACK COUNT AND HYBRID SERVO CONTROL REGISTER

Address: 4 and 5 Access: Read/Write Reset: 00

Description: In a hybrid servo application, the dedicated servo channel is supported by a 12-bit track crossing counter with a 4-bit hybrid control register. The counter is preset by the µP and counts down by one whenever the head crosses a track boundary. The LSB 8 bits of the counter are defined at register 4 as follows:

| BIT | NAME | DESCRIPTION |
|---|---|---|
| 0..7 | TRACK0..7 | LSB of the track crossing counter 0..7. When written, these bits preset the track counter. When read, they reflect the counter state. |

The MSB 4 bits of the counter along with the hybrid control bits are latched when the LSB 8 bits are read. The hybrid control bits, QUAD0, QUAD1, SELECT Q and CALIB are "write only." They are defined at register 5 as follows:

| BIT | NAME | DESCRIPTION |
|---|---|---|
| 0..3 | TRACK8..11 | MSB of track crossing counter 8..11. When written, these bits preset the track counter. When read, they reflect the counter state. |
| 4<br>5 | QUAD0<br>QUAD1 | Quadrant Select. These 2 bits select the quadrant per table below:<br><br>QUAD1 QUAD0 Quadrant Selected<br>0 0 -Q<br>0 1 N<br>1 0 -N<br>1 1 Q |
| 6 | SELECT Q | Quadrant Select Enable. Select quadrant with QUAD0 and QUAD1 when set HIGH. |
| 7 | CALIB | Calibration Enable. When set HIGH, the device is in the calibration mode in which analog inputs N and Q are tied to a DC reference level, NQREF; the analog input SERIN is tied to the DC reference level, SEREF. |

### ERROR DAC DATA REGISTER

Address: 6 Access: Write Reset: 00

| BIT | NAME | DESCRIPTION |
|---|---|---|
| 0..7 | DAC0..7 | Digital input to the D/A converter in 2's complement format. DAC7 corresponds to the sign bit. |

**EMBEDDED SERVO GAIN CONTROL REGISTER**

Address: 7 Access: Write Reset: 00

| BIT | NAME | DESCRIPTION |
|---|---|---|
| 0 | GAIN0 | Embedded Servo Burst Amplitude Gain Select. |
| 1 | GAIN1 | These two bits define the gain setting for the embedded servo differential amplifier per table below:<br>**GAIN1 GAIN0 Gain, dB**<br>0 0 -6<br>0 1 -3<br>1 0 0<br>1 1 3 |
| 2<br>3<br>4<br>5 | GAIN2<br>GAIN3<br>GAIN4<br>GAIN5 | Embedded Servo Burst Amplitude Gain Select.<br>These four bits define the gain setting for the sample/hold amplifier per table below:<br>**GAIN5 GAIN4 GAIN3 GAIN2 Gain, dB**<br>0 0 0 0 0.0<br>0 0 0 1 0.2<br>0 0 1 0 0.4<br>0 0 1 1 0.6<br>0 1 0 0 0.8<br>0 1 0 1 1.0<br>0 1 1 0 1.2<br>0 1 1 1 1.4<br>1 0 0 0 1.6<br>1 0 0 1 1.8<br>1 0 1 0 2.0<br>1 0 1 1 2.2<br>1 1 0 0 2.4<br>1 1 0 1 2.6<br>1 1 1 0 2.8<br>1 1 1 1 3.0 |
| 6 | SYNC SEL | Sync Input Select. When set HIGH, the frame rate to sample dedicated quadrature position signals N and Q is derived internally from SYSCLK. Otherwise, it is provided externally from the servo demodulator through SYNC and VCO inputs. |
| 7 | TCHE | Track Clock Hysteresis Enable. When set HIGH, an internal timing hysteresis is added for deriving the TRKCK output. |

### TRANSCONDUCTANCE, PRESCALER & MODE CONTROL REGISTER

Address: 8 Access: Write Reset: Bit 4 and 5 only

| Bit | Name | Description |
|---|---|---|
| 0 | TEST | Test Mode Enable. When set HIGH, the device is in the test mode where the testing time for the spindle motor speed control function is shortened. |
| 1 | SLEEP | Power-down Mode Enable. When set HIGH, the device is in the power-down mode where all analog circuitry is de-biased, the clock is disabled and the output drivers are pulled to logical HIGH. |
| 2<br>3 | TGAIN0<br>TGAIN1 | Transconductance Select. The transconductance gain of spindle motor lower drivers is defined per table below:<br>**TGAIN1 TGAIN0 Gain**<br>0 0 2<br>0 1 4<br>1 0 8<br>1 1 16 |
| 4<br>5 | SCALE0<br>SCALE1 | SYSCLK Prescaler. To accommodate different system clocks which may be used, the prescaler selects a proper divider to generate a fixed clock at 500 kHz per table below:<br>**SCALE1 SCALE0 SYSCLK(MHz) Divider**<br>0 0 10 20<br>0 1 8 16<br>1 0 6 12<br>1 1 4 8 |
| 6<br>7 | MODE0<br>MODE1 | Spindle Mode Control. These two bits define the number of motor poles per table below:<br>**MODE1 MODE0 POLES COMMU/INDEX**<br>0 0 4 12<br>0 1 8 24<br>1 0 12 36<br>1 1 N/A N/A |

### EMBEDDED SERVO TIMING WINDOW CONTROL REGISTER

Address: 9 Access: Write Reset: 00

Description: The embedded servo position burst timing controller generates four timing windows. The sample control register matches these timing windows with four SAMPLE/HOLD circuits. The µP writes into the register a control pattern which will provide a necessary sampling to compare the required bursts in a proper polarity and sequence. In this manner, the µP can mix and commutate the bursts so that the position error signal is always in the same direction.

| BIT | NAME | DESCRIPTION |
|---|---|---|
| 0,1 | WD SH1 | Define timing window for SAMPLE/HOLD 1. Bit 0 is LSB. |
| 2,3 | WD SH2 | Define timing window for SAMPLE/HOLD 2. Bit 2 is LSB. |
| 4,5 | WD SH3 | Define timing window for SAMPLE/HOLD 3. Bit 4 is LSB. |
| 6,7 | WD SH4 | Define timing window for SAMPLE/HOLD 4. Bit 6 is LSB. |



The timing window is selected per table below:

| MSB | LSB | S/H Timing Window |
|---|---|---|
| 0 | 0 | Timing window 1 |
| 0 | 1 | Timing window 2 |
| 1 | 0 | Timing window 3 |
| 1 | 1 | Timing window 4 |

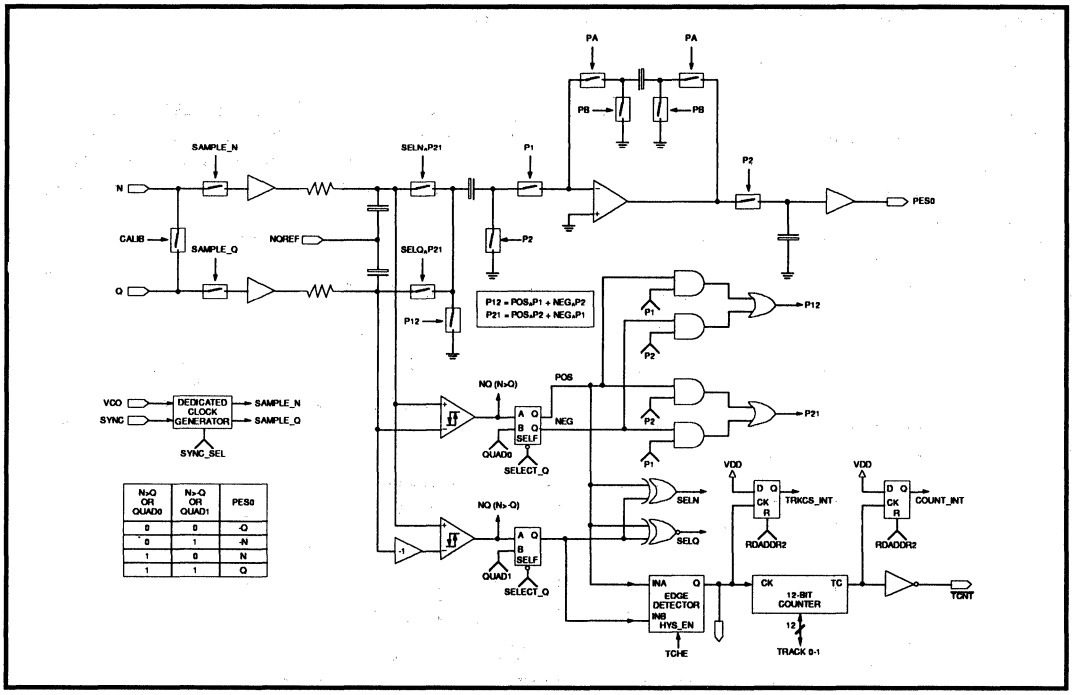


**FIGURE 2: Dedicated Servo Position Processor**

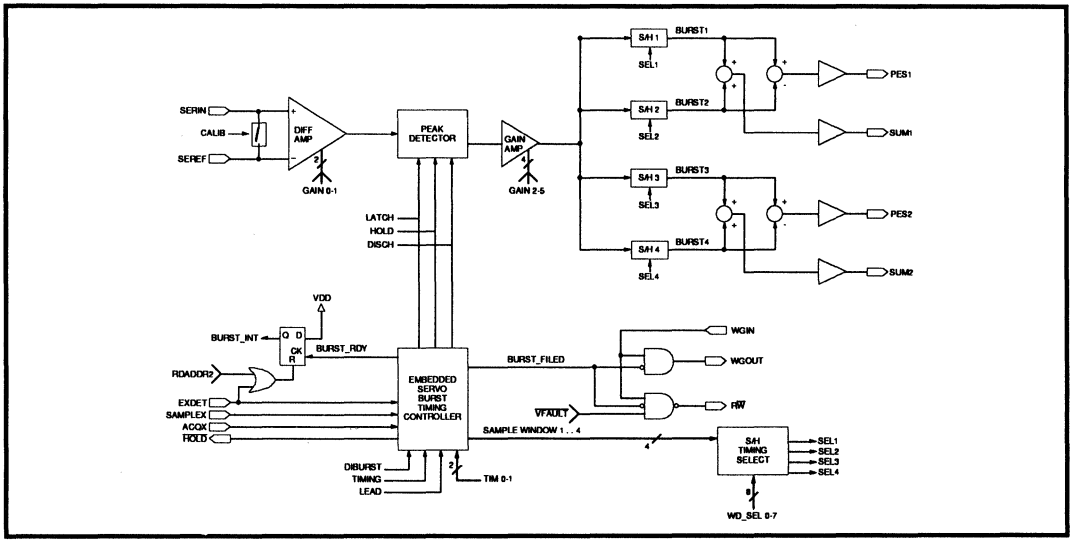


**FIGURE 3: Embedded Servo Burst Amplitude Processor & Timing Controller**

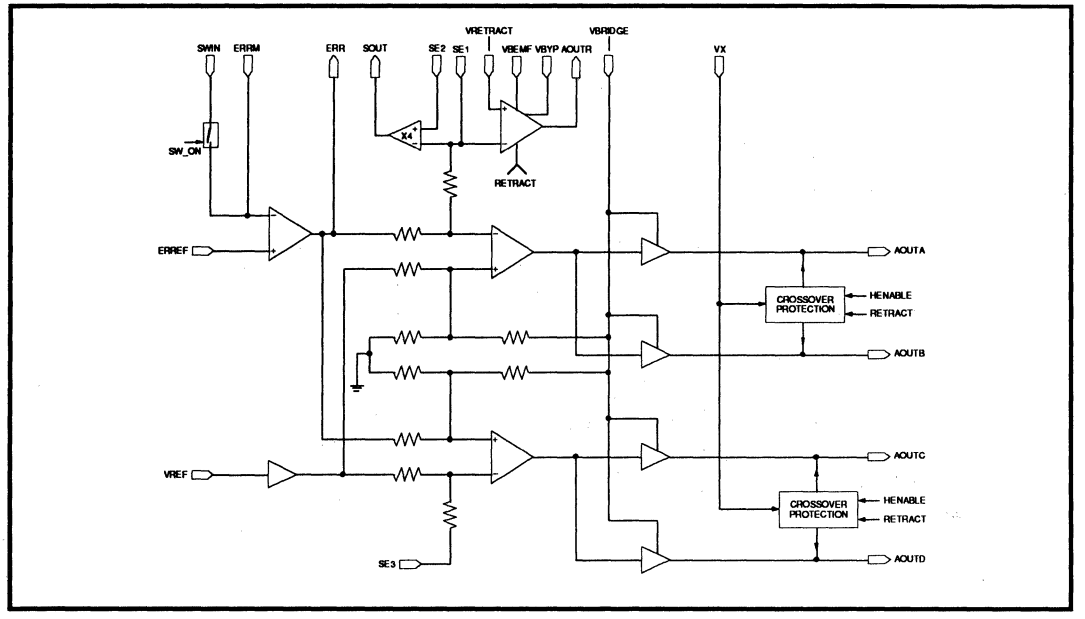


**FIGURE 4: Servo Position Error Amplifier**

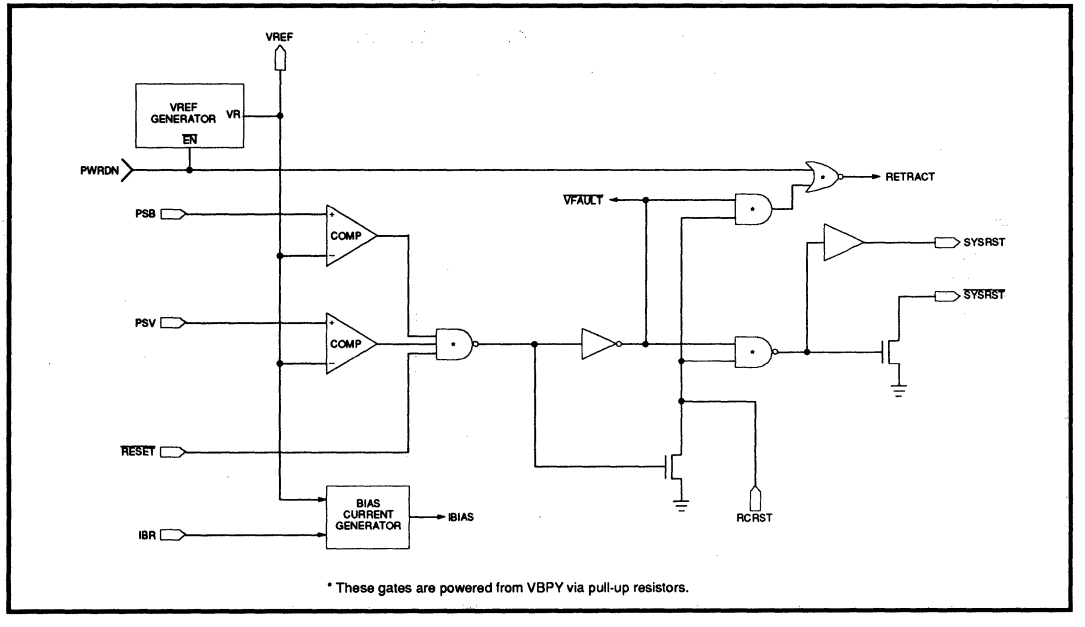


**FIGURE 5: Voltage Fault & Servo Head Retract Logic**

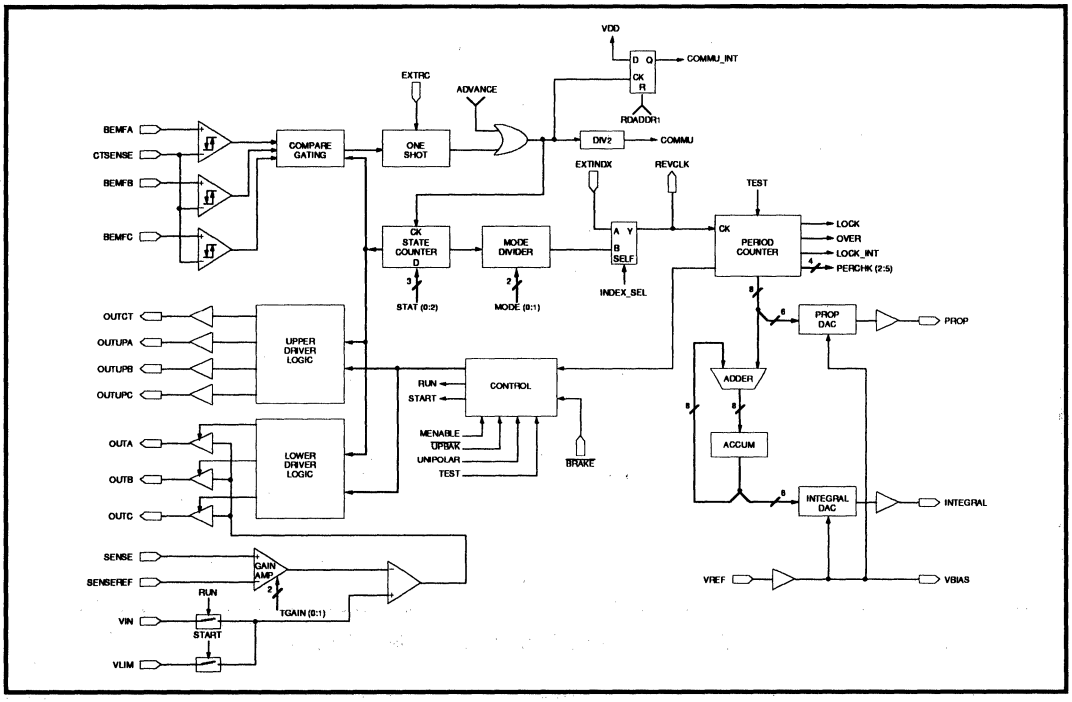


**FIGURE 6: Spindle Motor Speed Control**

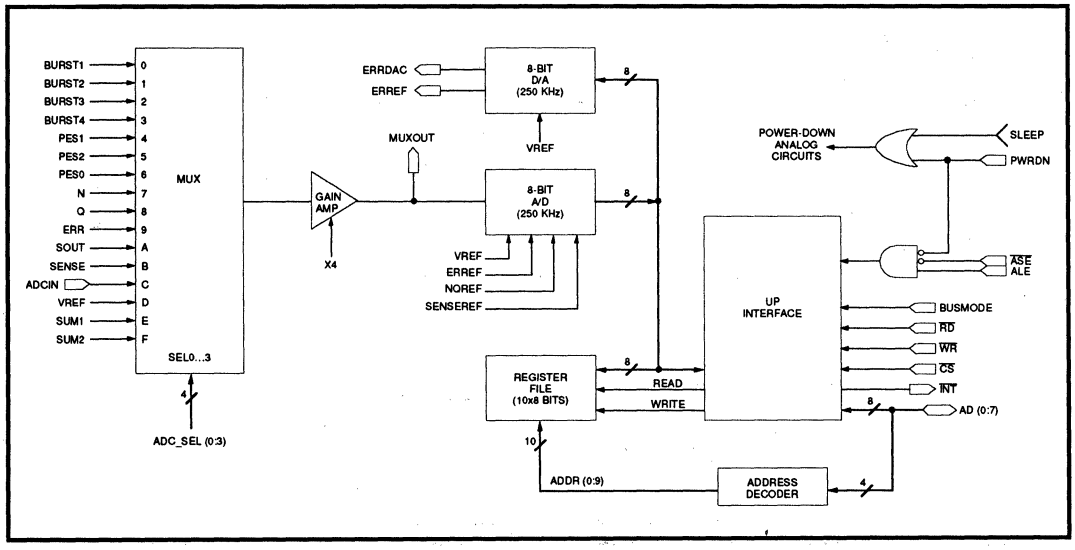


**FIGURE 7: Data Acquisition & Microprocessor Bus Interface**

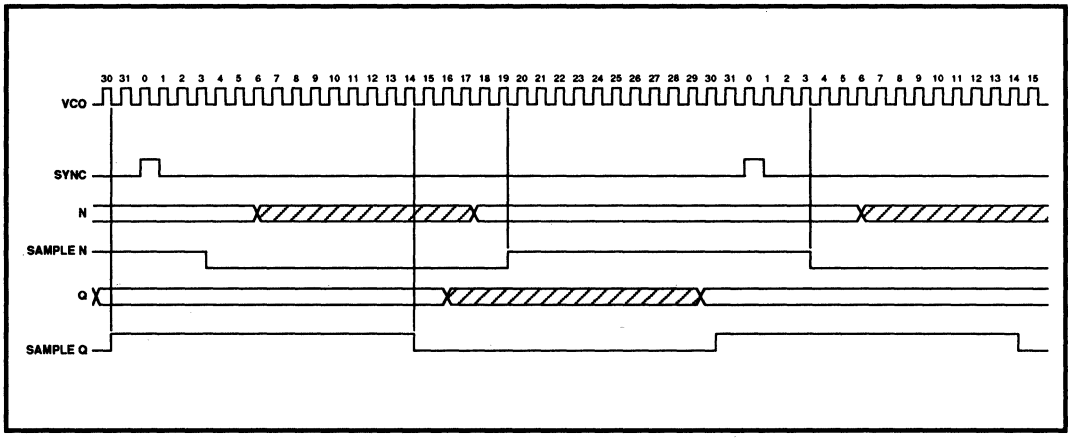


**FIGURE 8: Dedicated Servo Timing Diagram**

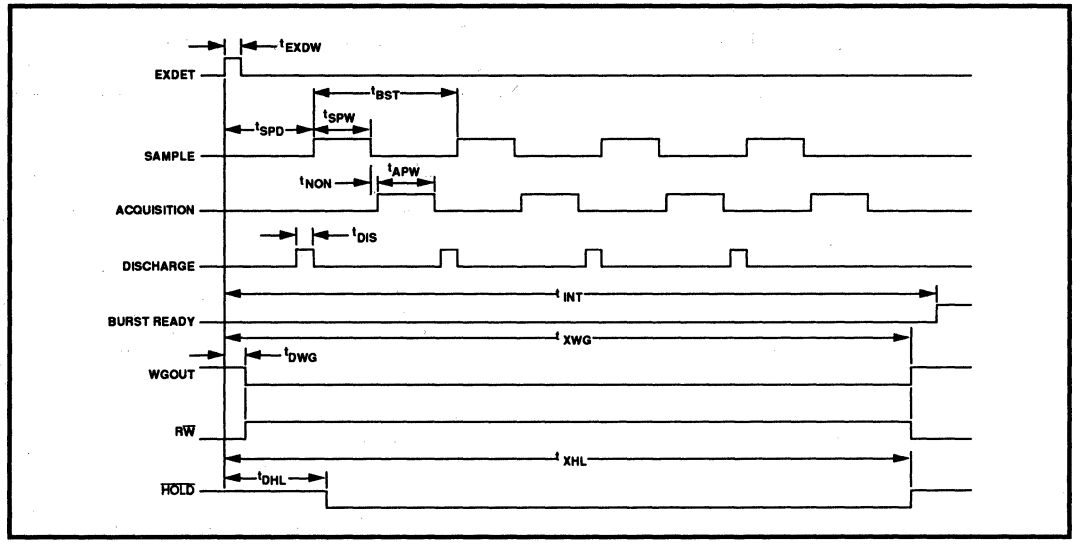


**FIGURE 9: Embedded Servo Timing Diagram with Internal Timing Source**

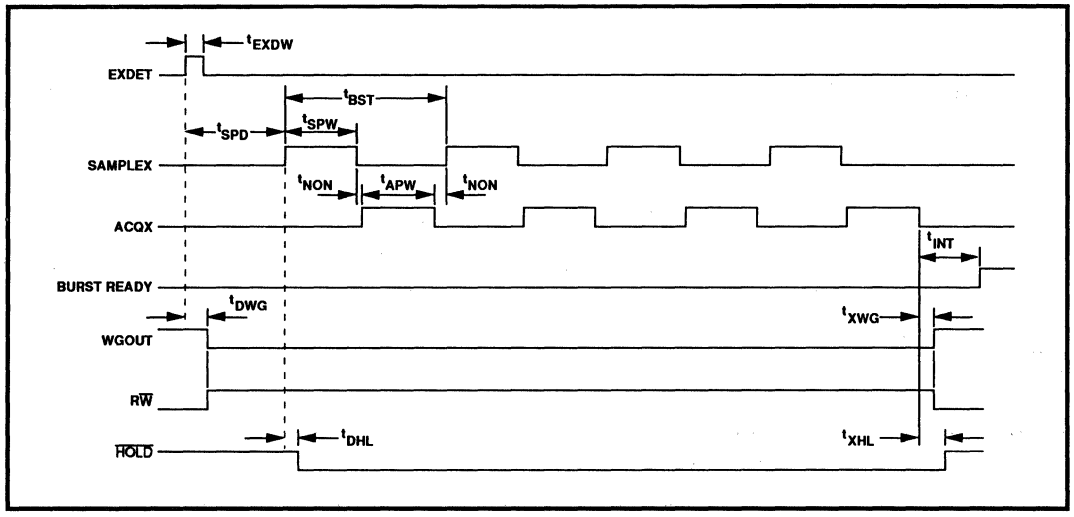


FIGURE 10: Embedded Servo Timing Diagram with External Timing Source

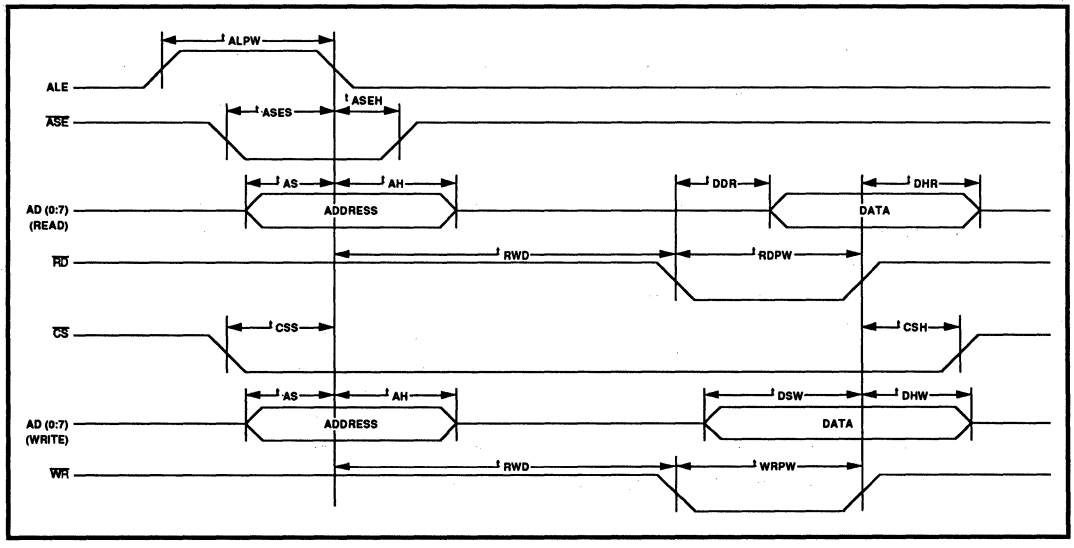


FIGURE 11: Intel Microprocessor Bus Interface Timing Diagram

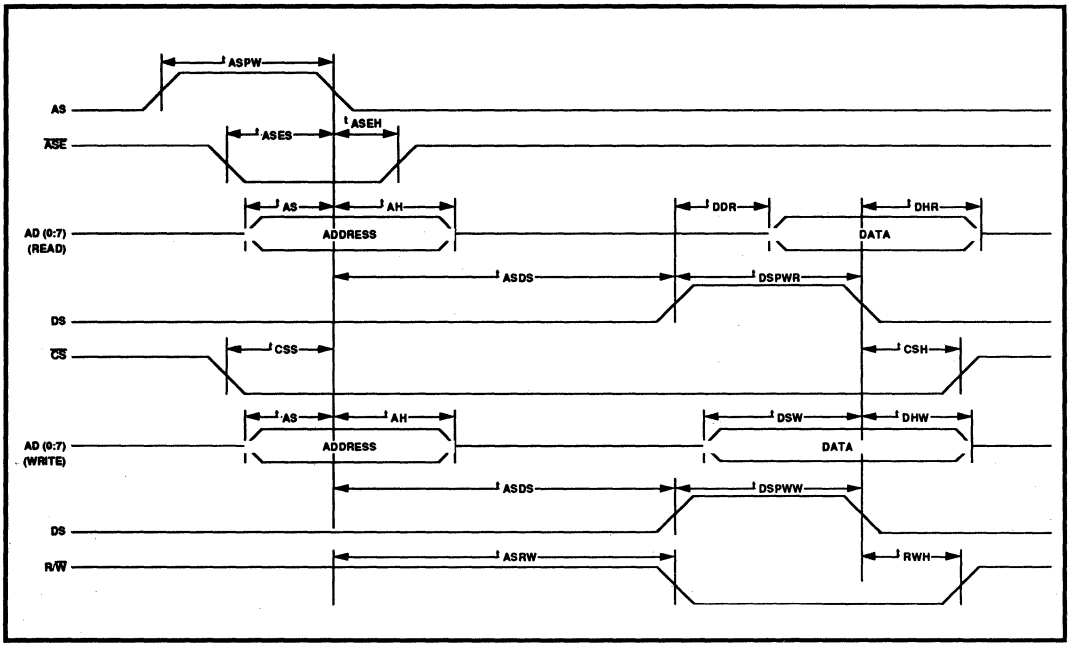


**FIGURE 12: Motorola Microprocessor Bus Interface Timing Diagram**

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| 0: INTERRUPT CONTROL/STATUS | | | 1: SPINDLE CONTROL/STATUS | | | 2: SERVO CONTROL/STATUS | | | 3: ADC CONTROL/STATUS | | | 4:TRACK COUNT LSB | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| # | WRITE | READ | # | WRITE | READ | # | WRITE | READ | # | WRITE | READ | # | WRITE | READ |
| 0 | COMMU INT | COMMU INT | 0 | $\overline{\text{UPBRK}}$ | LOCK | 0 | HENABLE | | 0 | ADC SEL0 | ADC0 | 0 | TRACK0 | TRACK0 |
| 1 | LOCK INT | LOCK INT | 1 | UNIPOLAR | OV ER | 1 | SW ON | | 1 | ADC SEL1 | ADC1 | 1 | TRACK1 | TRACK1 |
| 2 | BURST INT | BURST INT | 2 | INDEX SEL | COMMU | 2 | | BURST | 2 | ADC SEL2 | ADC2 | 2 | TRACK2 | TRACK2 |
| 3 | TRKS INT | TRKS INT | 3 | MENABLE | PERCHK5 | 3 | TIMING | TRKS | 3 | ADC SEL3 | ADC3 | 3 | TRACK3 | TRACK3 |
| 4 | COUNT INT | COUNT INT | 4 | ADVANCE | PERCHK4 | 4 | DIBURST | COUNT | 4 | X4 | ADC4 | 4 | TRACK4 | TRACK4 |
| 5 | | | 5 | STAT0 | PERCHK3 | 5 | LEAD | | 5 | | ADC5 | 5 | TRACK5 | TRACK5 |
| 6 | | | 6 | STAT1 | PERCHK2 | 6 | TIM0 | NQ | 6 | | ADC6 | 6 | TRACK6 | TRACK6 |
| 7 | MST INT | MST INT | 7 | STAT2 | | 7 | TIM1 | $\overline{\text{NQ}}$ | 7 | | ADC7 | 7 | TRACK7 | TRACK7 |

| 5: TRACK COUNT MSB & HYBRID SERVO CONTROL | | | 6: ERROR DAC DATA | | | 7: EMBEDDED SERVO GAIN CONTROL | | | 8: TRANSCONDUCTANCE PRESCALER & MODE CONTROL | | | 9: EMBEDDED SERVO TIMING WINDOW CONTROL | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| # | WRITE | READ | # | WRITE | READ | # | WRITE | READ | # | WRITE | READ | # | WRITE | READ |
| 0 | TRACK8 | TRACK8 | 0 | DAC0 | | 0 | GAIN0 | | 0 | TEST | | 0 | WD SEL0 | |
| 1 | TRACK9 | TRACK9 | 1 | DAC1 | | 1 | GAIN1 | | 1 | SLEEP | | 1 | WD SEL1 | |
| 2 | TRACK10 | TRACK10 | 2 | DAC2 | | 2 | GAIN2 | | 2 | TGAIN0 | | 2 | WD SEL2 | |
| 3 | TRACK11 | TRACK11 | 3 | DAC3 | | 3 | GAIN3 | | 3 | TGAIN1 | | 3 | WD SEL3 | |
| 4 | QUAD0 | | 4 | DAC4 | | 4 | GAIN4 | | 4 | SCALE0 | | 4 | WD SEL4 | |
| 5 | QUAD1 | | 5 | DAC5 | | 5 | GAIN5 | | 5 | SCALE1 | | 5 | WD SEL5 | |
| 6 | SELECT Q | | 6 | DAC6 | | 6 | SYNC SEL | | 6 | MODE0 | | 6 | WD SEL6 | |
| 7 | CALIB | | 7 | DAC7 | | 7 | TCHE | | 7 | MODE1 | | 7 | WD SEL7 | |

**FIGURE 13: SSI 32H4633 Register Map**

## PIN DESCRIPTION

This section describes the names of the pins, their symbols, their functions and their active states. The pins are grouped together into function for clarity.

### POWER SUPPLIES

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| VPA, B, C, G | - | Analog +5V supplies. They must be shorted externally. |
| VPD | - | Digital +5V supply. It must be shorted to analog +5V supplies externally. |
| VNA, B, C, G | - | Analog grounds. They must be shorted externally. |
| VND, VND2 | - | Digital grounds. They must be shorted to analog grounds externally. |



### SERVO HEAD POSITION PROCESSOR

| | | |
|---|---|---|
| N | I | Normal Input - Analog position signal from a dedicated servo demodulator. This input along with quadrature input is used to extract the position information from a dedicated servo surface. |
| Q | I | Quadrature Input - Analog position signal from a dedicated servo demodulator. |
| NQREF | I | Dedicated Position Error Reference - DC reference voltage for both normal and quadrature analog inputs. |
| SYNC | I | Sync Input - A clock signal generated from a dedicated servo demodulator. The falling edge of this clock causes the analog signals N and Q to be sampled. |
| VCO | I | VCO Input - A clock signal generated from a dedicated servo demodulator. The VCO should be synchronous with N and Q inputs. |
| TRKCK | O | Track Crossing Clock - This digital output drives external hardware track counter and is compatible with the counter function available in the Intel 8051 family of microcontrollers. It is normally LOW and pulses HIGH once per track crossing. |
| $\overline{\text{TCNT}}$ | O | Terminal Count - The terminal count output is normally HIGH and goes LOW when the 12-bit counter reaches zero. |
| PES0 | O | Position Error Output - Test point for the analog output of the position processor. This signal is proportional to the radial displacement of the head from the center of the current track, based upon the values of bits QUAD0, QUAD1 and SELECT Q. |
| SERIN | I | Embedded Servo Input - Full-wave rectified analog signal generated from a read data channel. This input is to extract the position information from embedded servo bursts. |
| SEREF | I | Embedded Servo Burst Reference - A DC reference level for the full-wave rectified analog signal SERIN. |
| SAMPLEX | I | Servo Burst Sample - This TTL compatible input, when HIGH, activates the peak detector. This input is used only when the TIMING bit in the SERVO CONTROL register is set HIGH for an external timing source. |

**SERVO HEAD POSITION PROCESSOR** (continued)

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| ACQX | I | Servo Burst Acquisition - This TTL compatible input, when HIGH, activates the transfer of the voltage captured by the peak detector onto holding capacitors. This input is used only when the TIMING bit in the SERVO CONTROL register is set HIGH for an external timing source. |
| PES1<br>PES2 | O | Position Error Signal - Test point for differential signals which are defined as:<br>PES1 = BURST1-BURST2<br>PES2 = BURST3-BURST4 |
| SUM1<br>SUM2 | O | Position Sum Signal - Test point for summed signals which are defined as:<br>SUM1 = BURST1+BURST2<br>SUM2 = BURST3+BURST4 |

**HEAD POSITIONER MOSFET DRIVER AND VOLTAGE FAULT DETECTION**

| | | |
|---|---|---|
| ERRM | I | Actuator Inverting Input - Inverting input to the position error amplifier of the MOSFET predriver. |
| SWIN | I | This input is shorted to ERRM when the bit SW ON is set HIGH. SWIN floats otherwise. |
| ERR | O | Acceleration Error - Position error amplifier output. This signal is amplified by the MOSFET drivers and applied to the actuator through an external MOSFET H-bridge as follows:<br>SE3-SE1 = 30 (ERR-VREF) |
| AOUTA<br>AOUTC | O | PFET Driver - Drive signals for P channel MOSFETs connected between VBRIDGE and the voice coil actuator. Crossover protection circuitry ensures that the P and N channel devices driven by OUTC and OUTD are never enabled simultaneously. |
| AOUTB<br>AOUTD | O | NFET Driver - Drive signals for N channel MOSFETs connected between the current sense resistor and the voice coil actuator. |
| VBRIDGE | I | Bridge Voltage Supply - Pin for connection to the voltage supply provided to external power transistors. |
| VRETRACT | I | Retract Voltage - In head retract mode this voltage is applied across the actuator to force the heads to move at a constant speed. |
| AOUTR | O | Head Retract Amplifier Output - Voltage output to drive an external head retract circuit. |
| SE1<br>SE3 | I | Motor Voltage Sense Input - These inputs provide feedback to the internal MOSFET drive amplifier. |
| SE2 | I | Motor Current Sense Input - Non-inverting input to the current sense differential amplifier. It should be connected to an external current sense resistor. The inverting input of the differential amplifier is SE1. |
| SOUT | O | Motor Current Sense Output - This output provides a voltage proportional to the voltage drop across the external current sense resistor as follows:<br>SOUT-ERREF = 4 (SE2-SE1) |

**HEAD POSITIONER MOSFET DRIVER AND VOLTAGE FAULT DETECTION** (continued)

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| VX | O | Crossover Protection Voltage - The current source output at VX is converted to a voltage with an external resistor. The value of the resistor should be adjusted so that VX is less than the specified minimum threshold voltage of the MOSFET bridge. |
| VBYP | I | Bypass Voltage Supply - The VBRIDGE voltage is stored on this node for use during retract. |
| PSB<br>PSV | I | Fault Voltage Comparator Inputs - Voltage inputs for the low voltage comparators. These two inputs should be connected to separate external resistor dividers. Each resistor divider divides its corresponding supply voltage to a proper value which is comparable with the internal voltage reference at 2.35 volts. |
| VREF | O | Internal Voltage Reference - A voltage reference at 2.35 volts is generated internally for the DC reference level throughout the device. Due to limited drive capability provided with on-chip voltage reference, this pin shall be used only for connecting an external bypass capacitor of 10 µF. |
| IBR | O | Bias Current Reference - Pin for connection to an external resistor (from GND) to establish a reference current for bias currents used in analog circuits. |
| $\overline{\text{RESET}}$ | I | Reset Input - When set LOW, all the internal registers are reset and a forced head retraction is activated. |
| $\overline{\text{SYSRST}}$ | O | Reset Output - Active LOW output signal, which is generated by a supply voltage fault or $\overline{\text{RESET}}$ being pulled LOW externally. |
| SYSRST | O | Reset Output - Active HIGH output signal which is inverted version of $\overline{\text{SYSRST}}$. |
| RCRST | I | Pin for connection to an external capacitor to extend the active low duration of $\overline{\text{SYSRST}}$. |

**SPINDLE MOTOR SPEED CONTROL**

| | | |
|---|---|---|
| EXTINDX | I | External Index Input - This TTL compatible input, when selected via the INDEX SEL bit, is used to provide a once-per-revolution indication of angular position and speed to the device. The falling edge of EXTINDX is the reference. |
| SYSCLK | I | System Clock Input - A TTL compatible input is provided to derive internal timing signals. |
| EXTRC | I | Pin for connection to a resistor (from VDD) and a capacitor (from GND) to provide the commutation delay. The commutation delay is 0.56 RC. After the commutation delay, the timing block provides a noise rejection interval to reject transients on the motor coils due to commutations. This noise rejection is an additional 0.29 RC. The total time (commutation delay and noise rejection internal) must be less than a commutation cycle time. |

**SPINDLE MOTOR SPEED CONTROL** (continued)

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| $\overline{\text{BRAKE}}$ | I | Spindle Braking Enable - This input, when active LOW, dynamically brakes the spindle motor. A resistor (from $\overline{\text{SYSRST}}$) and a capacitor (from GND) are connected to this pin to provide a delay between the initiation of fault-induced head retraction and motor braking. RC are selected such that 1.2 RC is equal to the maximum time required for head retraction. |
| VBIAS | O | Buffered Bias Voltage - VBIAS is buffered VREF to be used for VLIM and motor speed setting bias. (In some applications, it is necessary to create an "offset" to the speed control loop to obtain proper speed regulation.) |
| PROP | O | Proportional Channel D/A Output - The proportional channel output is the least significant 5 bits plus sign of the period measuring counter. The LSB signifies a 2 microsecond period variation. |
| INTEGRAL | O | Integral Channel D/A Output - The integral channel output is the most significant 6 bits of an 8-bit accumulator. The accumulator adds the least 8 bits of the period measurement counter to the previous value obtained from prior period measurements and accumulations. |
| VIN | I | Speed Control Voltage Input - The combination of external driver transistors and internal predriver circuits forms a transconductance amplifier which will define the motor current in relation to VIN. In conjunction with the SENSE input and the gain setting for the sense amplifier, the transconductance gain is given by: $g_m=I_m/VIN=1/(R_S \cdot A_V)$ where $I_m$ is the current flowing through the spindle motor coils, $R_S$ the current sense resistor and $A_V$ the transconductance gain defined by TGAIN0 and TGAIN1 bits. |
| VLIM | I | Current Limit Setting Voltage - The spindle motor current will be limited to a value determined by $R_S$, VLIM and Av such that Imax=VLIM/($R_S \cdot A_V$). VLIM is used whenever the spindle speed is measured less than 5151 RPM. |
| SENSE | I | Current Sense Amplifier Noninverting Input - The external driver transistor sources are connected to a current sense resistor $R_S$ to monitor motor current. The device will control the voltage across the sense resistor to match either VIN (during normal operation) and VLIM (during acceleration). |
| SENSEREF | I | Current Sense Amplifier Reference Input - Pin for a Kelvin connection to the ground side of the sense resistor. |
| OUTA<br>OUTB<br>OUTC | O | Predriver Outputs - These predriver outputs drive the gates of external power NFETs. They are configured as open-drain outputs with internal 10 KΩ pull-up resistors to VBEMF. |
| OUTUPA<br>OUTUPB<br>OUTUPC | O | Upper Pull-up Outputs - These predriver outputs drive the gates of external power PFETs. They are configured as open-drain outputs with internal 10 KΩ pull-up resistors to VBEMF. |
| OUTCT | O | Center Tap Predriver - This output drives an external PFET driver which connects the motor center tap to the positive power supply for unipolar drive applications. OUTCT has the same characteristics as OUTUPA,B,C and is enabled via the UNIPOLAR bit. |

**SPINDLE MOTOR SPEED CONTROL** (continued)

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| VBEMF | I | Back-emf Voltage - A power diode voltage drop from the motor power supply is defined as VBEMF. The external PFET sources are connected to VBEMF as is this pin. During power failure, this voltage is used to provide power for head retraction and motor braking. |
| BEMFA<br>BEMFB<br>BEMFC<br>CTSENSE | I | Back-emf Inputs - Inputs to be connected to their respective motor coils and the center tap for sensing generated back-emf voltages. The device uses the back-emf voltages to determine the rotor position and effect commutation. |
| REVCLK | O | Revolution Clock Output - This output generates a once-per-revolution indication of motor activity derived from back-emf events. |



**DATA ACQUISITION AND MICROPROCESSOR BUS INTERFACE**

| | | |
|---|---|---|
| ALE | I | Address Latch Enable - Falling edge latches the register address from the AD0..AD7 address/data bus. |
| $\overline{ASE}$ | I | Address Strobe Enable - When set LOW, this input enables ALE input to the device. |
| $\overline{CS}$ | I | Chip Select - Active LOW signal enables the device to respond to µP read or write. |
| $\overline{WR}$ | I | Write Strobe - In Intel µP applications, active LOW signal causes the data on the address/data bus to be written to the addressed register if $\overline{CS}$ is also active. |
| $\overline{RD}$ | I | Read Strobe - In Intel µP applications, active LOW signal causes the contents of the addressed register to be placed on the address/data bus if $\overline{CS}$ is also active. |
| AD0..AD7 | I/O | Address/Data Bus - 8-bit bus which carries register address information and bidirectional data. These pins are in the high impedance state when not used. |
| BUSMODE | I | Mode Select - When active HIGH, Intel bus interface is selected. Otherwise, Motorola bus interface is selected. |
| $\overline{INT}$ | O | Interrupt Strobe - Active LOW output signals the µP to respond to the device. It is released when all the pending interrupts have been serviced by the µP. |
| PWRDN | I | Power-down Mode Enable - When set HIGH, the device is in the power-down mode where all analog circuitry is de-biased, the clock is disabled and the output drivers are pulled to logical HIGH. |
| ERRDAC | O | Error DAC Output - An 8-bit D/A output which converts a digital word from the µP into an analog signal. This signal is fed back to the position error amplifier through external RC components. |
| ERREF | O | Reference voltage for D/A output ERRDAC. |
| ADCIN | I | External A/D input. |
| MUXOUT | O | Test point for the X4 amplifier output which is the input to the A/D converter. |

### EMBEDDED SERVO TIMING CONTROLLER

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| EXDET | I | Bit Synchronization Input - The internal servo timing controller is synchronized with this TTL compatible input. |
| $\overline{HOLD}$ | O | AGC Gain Hold - TTL compatible control signal holds the input AGC amplifier gain of a pulse detector, such as 32P4620, when pulled LOW. |
| WGIN | I | Write Gate Input - TTL compatible input from the storage controller. |
| WGOUT | O | Write Gate Output - TTL compatible control signal derived from WGIN. This output will be pulled LOW during embedded servo position burst sampling. |
| $R\overline{W}$ | O | Read/Write Control Output - TTL compatible control signal derived from WGIN. This output will be pulled HIGH during embedded servo position burst sampling or when a low voltage fault occurs. |

## ELECTRICAL SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS

Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device or affect reliability.

| PARAMETER | SYMBOL | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|---|
| Supply voltage applied at VPA, VPB, VPC, VPD, VPG | VDD | | 0.1 | | 7.0 | V |
| Signal ground applied at VNA, VNB, VNC, VND, VND2, VNG | GND | | 0.0 | | 0.0 | V |
| Bridge voltage applied at VBRIDGE | VBRIDGE | | 0.1 | | 14.0 | V |
| Bypass voltage applied at VBYP | VBYP | | 0.1 | | 14.0 | V |
| Back-emf voltage applied at VBEMF | VBEMF | | 0.1 | | 20.0 | V |
| VBEMF current if VBEMF>18V | IBEMF | | - | | 5.0 | mA |
| Digital input voltages | VIND | | -0.3 | | VDD+0.3 | V |
| Analog input voltages | VINA | | -0.3 | | VDD+0.3 | V |
| Storage temperature | Tstg | | -65 | | 150 | °C |
| Lead temperature | TI | | - | | 300 | °C |

## OPERATING ENVIRONMENT LIMITATIONS

The recommended operating conditions for the device are indicated in the table below. Performance specifications do not apply where the device is operating outside these limits.

| PARAMETER | SYMBOL | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| Supply voltage applied at VPA,VPB,VPC,VPD,VPG | VDD | | 4.75 | - | 5.25 | V |
| Signal ground applied at VNA,VNB,VNC,VND, VND2,VNG | GND | | 0.0 | - | 0.0 | V |
| Bridge voltage applied at VBRIDGE | VBRIDGE | | 4.75 | - | 13.2 | V |
| Bypass voltage applied at VBYP | VBRIDGE -VBYP | | 0.0 | - | 0.8 | V |
| Back-emf voltage applied at VBEMF | VBRIDGE -VBEMF | | -5.0 | - | 0.8 | V |
| Ambient temperature | TA | | 0.0 | - | 70.0 | °C |
| System clock (10 MHz, Max) | Fc | | - | - | ±0.01 | % |
| Capacitive load on digital outputs | CL | | - | - | 100 | pF |
| Analog input impedance | Rin | | 100 | - | - | kΩ |
| | Cin | | - | - | 20 | pF |
| Load on analog outputs | Rout | | 10 | - | - | kΩ |
| | Cout | | - | - | 40 | pF |
| Bias resistor (22.6 kΩ, Typ) | RBIAS | | - | - | ±1 | % |

## DC CHARACTERISTICS

The following electrical specifications apply to the digital input and output signals over the recommended operating range unless otherwise noted. Positive current is defined as entering the device. Minimum and maximum are based upon the magnitude of the number.

| | | | | | | |
|---|---|---|---|---|---|---|
| Supply current<br>Normal mode | IDD | VDD=5.25V | - | - | 50 | mA |
| Power-down mode | - | | - | - | 5 | mA |
| Output logic "1" voltage | Voh | Ioh=-0.4 mA<br>VDD=4.75V | 2.4 | - | - | V |
| Output logic "0" voltage | Vol | Iol=1.6 mA<br>VDD=4.75V | - | - | 0.4 | V |
| Input logic "1" voltage | Vih | VDD=4.75V | 2.0 | - | - | V |
| Input logic "0" voltage | Vil | VDD=4.75V | - | - | 0.8 | V |

## ELECTRICAL SPECIFICATIONS (continued)

### DC CHARACTERISTICS (continued)

| PARAMETER | SYMBOL | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| Input logic "1" current | Iih | Vih=5.25V<br>VDD=5.25V | - | - | 10 | µA |
| Input logic "0" current | Iil | Vil=0.0<br>VDD=5.25V | - | - | -10 | µA |
| Input capacitance | Cin | | - | - | 10 | pF |

### FUNCTIONAL CHARACTERISTICS

#### Dedicated Servo Position Processor

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| N,Q comparator hysteresis | | 5 | - | 30 | mV |
| Commutator comparator offset | | - | - | ±30 | mV |
| N,Q input voltage w.r.t GND | | 0.5 | - | 3.7 | V |
| NQREF w.r.t. GND | | 1.9 | - | 2.9 | V |
| N,Q input voltage w.r.t NQREF | | - | - | ±1.1 | V |
| Channel gain from N,Q to PES0 | | 0.96 | 1.0 | 1.04 | V/V |
| PES0 offset | | - | - | ±50 | mV |
| PES0 output corner frequency | | 60 | 85 | 120 | kHz |

#### Embedded Servo Burst Amplitude Processor

| | | | | | |
|---|---|---|---|---|---|
| SERIN w.r.t. GND | | 2.0 | - | VDD | V |
| SEREF w.r.t. GND | | 2.0 | - | 3.0 | V |
| SERIN input voltage | Channel gain=-6 dB | 0.0 | - | 2.0 | Vp |
| swing w.r.t. SEREF | Channel gain=0 dB | 0.0 | - | 1.0 | Vp |
| Servo burst frequency | | 0.5 | - | 2.0 | MHz |
| Input impedance at | | 20 | - | - | kΩ |
| SERIN, SEREF | | - | - | 10 | pF |
| DC offset at PES1,PES2 | BURST1=BURST2=0.5V<br>BURST3=BURST4=0.5V | -30 | - | 20 | mV |
| DC offset at SUM1,SUM2 | BURST1=BURST2=0.5V<br>BURST3=BURST4=0.5V | 0 | - | -250 | mV |

**Embedded Servo Burst Amplitude Processor** (continued)

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Differential gain error at PES1,PES2,SUM1,SUM2 | | - | - | ±0.1 | dB |
| Integral gain error at PES1,PES2,SUM1,SUM2 | | - | - | ±1.0 | dB |
| PES1,PES2 output swing w.r.t. VREF | | - | - | ±1.1 | V |
| SUM1,SUM2 output swing w.r.t. VREF | | - | - | 1.1 | V |
| Allowable load at PES1, PES2, | | 10 | - | - | kΩ |
| SUM1,SUM2 to VREF | | - | - | 40 | pF |

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**Embedded Servo Timing**

The following timing specifications are applied when the internal servo timing block is selected by pulling the TIMING bit to logical LOW. Timing measurements are defined in Figure 3 and made at 50% VDD with 50 pF load capacitances for all pins, unless otherwise noted.

| PARAMETER | SYMBOL | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Burst cell time | $t_{BST}$ | | | | |
| TIM0='0' TIM1='0' | | - | 5.0 | - | µs |
| TIM0='1' TIM1='0' | | - | 6.0 | - | µs |
| TIM0='0' TIM1='1' | | - | 8.0 | - | µs |
| TIM0='1' TIM1='1' | | - | 10.0 | - | µs |
| EXDET pulse width | $t_{EXDW}$ | 0.5 | - | $t_{BST}$ | µs |
| Internal first sampling time from EXDET rise | $t_{SPD}$ | | | | |
| LEAD='0' | | 1.0 | - | 1.7 | µs |
| LEAD='1' | | ($t_{BST}$+1.0) | - | ($t_{BST}$+1.7) | µs |
| Sampling pulse width | $t_{SPW}$ | | | | |
| TIM0='0' TIM1='0' | | - | 2.0 | - | µs |
| TIM0='1' TIM1='0' | | - | 3.0 | - | µs |
| TIM0='0' TIM1='1' | | - | 5.0 | - | µs |
| TIM0='1' TIM1='1' | | - | 7.0 | - | µs |
| Acquisition pulse width | $t_{APW}$ | - | 2.0 | - | µs |
| Discharge pulse width | $t_{DIS}$ | - | 0.75 | - | µs |
| Nonoverlapping time between sampling & acquisition pulses | $t_{NON}$ | - | 0.25 | - | µs |

**Embedded Servo Timing** (continued)

| PARAMETER | SYMBOL | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Burst ready interrupt from EXDET rise | $t_{INT}$ | | | | |
| DIBURST='0' LEAD='0' | | $(4t_{BST}+5.2)$ | - | $(4t_{BST}+5.9)$ | µs |
| DIBURST='1' LEAD='0' | | $(2t_{BST}+5.2)$ | - | $(2t_{BST}+5.9)$ | µs |
| DIBURST='0' LEAD='1' | | $(5t_{BST}+5.2)$ | - | $(5t_{BST}+5.9)$ | µs |
| DIBURST='1' LEAD='1' | | $(3t_{BST}+5.2)$ | - | $(3t_{BST}+5.9)$ | µs |
| WGOUT & $R\overline{W}$ delay time from EXDET rise | $t_{DWG}$ | 0.0 | - | 0.1 | µs |
| WGOUT & $R\overline{W}$ hold time from EXDET rise | $t_{XWG}$ | | | | |
| DIBURST='0' LEAD='0' | | $(4t_{BST}+1.0)$ | - | $(4t_{BST}+1.7)$ | µs |
| DIBURST='1' LEAD='0' | | $(2t_{BST}+1.0)$ | - | $(2t_{BST}+1.7)$ | µs |
| DIBURST='0' LEAD='1' | | $(5t_{BST}+1.0)$ | - | $(5t_{BST}+1.7)$ | µs |
| DIBURST='1' LEAD='1' | | $(3t_{BST}+1.0)$ | - | $(3t_{BST}+1.7)$ | µs |
| $\overline{HOLD}$ delay time from EXDET rise | $t_{DHL}$ | | | | |
| LEAD='0' | | 0.2 | - | 0.7 | µs |
| LEAD='1' | | $(t_{BST}+0.2)$ | | $(t_{BST}+0.7)$ | µs |
| $\overline{HOLD}$ hold time from EXDET rise | $t_{XHL}$ | | | | |
| DIBURST='0' LEAD='0' | | $(4t_{BST}+1.0)$ | - | $(4t_{BST}+1.7)$ | µs |
| DIBURST='1' LEAD='0' | | $(2t_{BST}+1.0)$ | - | $(2t_{BST}+1.7)$ | µs |
| DIBURST='0' LEAD='1' | | $(5t_{BST}+1.0)$ | - | $(5t_{BST}+1.7)$ | µs |
| DIBURST='1' LEAD='1' | | $(3t_{BST}+1.0)$ | - | $(3t_{BST}+1.7)$ | µs |

The following timing specifications are applied when the internal servo timing block is selected by pulling the TIMING bit to logical HIGH. Timing measurements are defined in Figure 4 and made at 50% VDD with 50 pF load capacitances for all pins, unless otherwise noted.

| | | | | | |
|---|---|---|---|---|---|
| EXDET pulse width | $t_{EXDW}$ | 0.5 | - | 5.0 | µs |
| SAMPLEX delay time from EXDET rise | $t_{SPD}$ | 0.2 | - | - | µs |
| SAMPLEX pulse width | $t_{SPW}$ | 3 | - | - | µs |
| ACQX pulse width | $t_{APW}$ | 2 | - | - | µs |
| Nonoverlapping time between SAMPLEX & ACQX pulses | $t_{NON}$ | 0.0 | - | - | µs |
| Burst ready interrupt from last ACQX fall | $t_{INT}$ | 5.2 | - | 5.9 | µs |
| WGOUT & $R\overline{W}$ delay time from EXDET rise | $t_{DWG}$ | 0.0 | - | 0.1 | µs |

**Embedded Servo Timing** (continued)

| PARAMETER | SYMBOL | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| WGOUT & $R\overline{W}$ hold time from last ACQX fall | $t_{XWG}$ | 1.0 | - | 1.7 | µs |
| $\overline{HOLD}$ delay time from first SAMPLEX rise | $t_{DHL}$ | 0.2 | - | 0.7 | µs |
| $\overline{HOLD}$ hold time from last ACQX fall | $t_{XHL}$ | 1.0 | - | 1.7 | µs |

**Head Positioner MOSFET Driver**

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| VRETRACT voltage | VBEMF = 3V | 0.3 | - | 0.9 | V |
| | VBEMF = 12V | 0.4 | - | 1.2 | V |
| Retract offset | | | | | |
| VBEMF = 3V | VRETRACT = 0.5V | -70 | - | 50 | mV |
| VBEMF = 6V | VBYP = 4V to 13V | -70 | - | 70 | mV |
| VBEMF = 12V | $I_{AOUTR}$<1mA | -150 | - | 150 | mV |
| Voh at AOUTR | Ioh = -1mA | | | | |
| VBEMF = 4V VBYP = 4V | | 1.5 | - | - | V |
| VBEMF = 3V VBYP = 4V | | 1.3 | - | - | V |
| Leakage current at AOUTR | RETRACT = LOW AOUTR = 0V to 14V | - | - | 1 | µA |
| Voh at AOUTA, AOUTC | Ioh = -1 mA | VBRIDGE-1.5 | - | - | V |
| | Ioh = -1 µA | VBRIDGE-0.1 | - | - | V |
| Vol at AOUTA, AOUTC | Iol = 10 µA | - | - | 1 | V |
| Voh at AOUTB | Ioh = -10 µA | VBRIDGE-0.5 | - | - | V |
| Voh at AOUTD | Ioh = -10 µA | VBYP-0.5 | - | - | V |
| Vol at AOUTB, AOUTD | Iol = 1 mA | - | - | 1 | V |
| | Iol = 10 µA | - | - | 0.2 | V |
| Input offset at SOUT | | - | - | ±3 | mV |
| SOUT/(SE1-SE2) | | 3.9 | - | 4.1 | V/V |
| SE1/ERR, SE3/ERR | | 14.0 | - | 15.4 | V/V |
| ERRAMP input offset | | - | - | ±10 | mV |
| ERRAMP gain | | 1000 | - | - | V/V |
| Output crossover time CL = 600 pF at AOUTA,C CL = 150 pF at AOUTB,D | PFET VTH = -2V NFET VTH = 2V $R_X$ = 50 kΩ | - | - | 45 | µs |
| Input impedance at SE1, SE2,SE3 | | 20 | - | - | kΩ |

**Head Positioner MOSFET Driver** (continued)

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Output resistance at SOUT | | - | - | 350 | Ω |
| Analog switch on-resistance at SWIN | | - | - | 600 | Ω |
| Output resistance at ERR | | - | - | 100 | Ω |
| Output voltage at VX | | 1.0 | - | 1.4 | V |

**Voltage Reference and Voltage Fault Circuit**

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| VPB voltage for $\overline{SYSRST}$ & RCRST in operation | | 2.0 | - | - | V |
| On resistance at RCRST | | | | | |
| VPB>3.5V VBYP>4V | | - | - | 800 | Ω |
| VPB>3.5V VBYP>10V | | - | - | 550 | Ω |
| RCRST input threshold | VBYP=4V | 0.2 | - | 1.2 | V |
| IBR voltage w.r.t. VREF | | -80 | - | 20 | mV |
| Output voltage at VREF | \|II\|<10μA | 2.27 | 2.34 | 2.41 | V |
| PSB,PSV comparator offset | | - | - | ±15 | mV |

**Spindle Motor Speed Control**

| | | | | | |
|---|---|---|---|---|---|
| SYSCLK duty cycle | | 40 | - | 60 | % |
| EXTINDX pulse width | | 200 | - | - | ns |
| Advance pulse width | | 3 | - | - | μs |
| Timing resistor at EXTRC | | 0.01 | - | 10 | MΩ |
| Timing capacitor at EXTRC | | 100 | - | - | pF |
| Delay time variation relative to T0* | | - | - | ±5 | % |
| Vil at $\overline{BRAKE}$ | VBEMF = 5V | 0 | - | 0.3 | V |
| Vih at $\overline{BRAKE}$ | VBEMF = 5V | 1.5 | - | - | V |
| Output voltage swing at PROP & INTEGRAL | $I_{out}$<0.1mA | 0 | - | VBIAS±5% | V |
| DAC step size at PROP & INTEGRAL | | 32 | - | 39 | mV |
| Output impedance at PROP & INTEGRAL | 0.5V<$V_{out}$<2.0V<br>$I_{out}$=0.1mA | - | - | 300 | Ω |

**Spindle Motor Speed Control** (continued)

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Kp,proportional gain** | | 0.31 | - | 0.38 | V/rad/s |
| Ki,integral gain | | 7.00 | - | 8.55 | V/rad |
| VBIAS output w.r.t. VREF | | -50 | - | 25 | mV |
| Input voltage at VIN & VLIM | | 0 | - | 2.35 | V |
| Input leakage current at VIN & VLIM | | - | - | ±1 | µA |
| Output resistance at OUTUPA,B,C & OUTCT | Output in HIGH state, pulled to VBEMF | 5 | - | 20 | kΩ |
| Vol at OUTUPA,B,C & OUTCT | $I_{out}$<3mA VBEMF=13.2V | - | - | 1.0 | V |
| Output resistance at OUTA,B,C | Output in HIGH state, pulled to VBEMF | 5 | - | 20 | kΩ |
| Vol at OUTA,B,C | $I_{out}$<5mA | - | - | 1.0 | V |
| Input voltage at SENSE | $A_V$=2 | 0.0 | - | 1.0 | V |
| Input voltage at SENSEREF | | 0.0 | - | 0.05 | V |
| Input leakage current at SENSE | 0.0V<$V_{in}$<1.0V | - | - | ±10 | µA |
| Input leakage current at SENSEREF | 0.0V<$V_{in}$<0.05V | -200 | - | 10 | µA |
| Input capacitance at SENSE & SENSEREF | | - | - | 20 | pF |
| Gain variation*** | $A_V$=2,4,8,16 | - | - | ±10 | % |
| Input impedance at BEMFA,B,C | -0.3V<$V_{in}$<15V | 100<br>- | -<br>- | -<br>10 | kΩ<br>pF |
| Input impedance at CTSENSE | | 30<br>- | -<br>- | -<br>10 | kΩ<br>pF |
| LOCK indication range | | 5384.9 | - | 5415.1 | RPM |
| Speed resolution | | - | - | ±0.018 | % |

*T0 is the commutation delay and is given by the relationship T0 = 0.56RC. Suggested value for C would be 470 to 1000 pF. An external R and C must be provided such that T0 is greater than 10 µs (R=22 kΩ, C=470 pF).

**The motor speed control loop can be described as: $H(s)=K_p+K_i/s$

***The transconductance gain from VIN or VLIM to the steady-state current flowing through the motor is given by $G = 1/(R_{SENSE} \cdot A_V)$

## DATA ACQUISITION

### A/D Converter

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| ADCIN full-scale | X4=LOW | - | ±(VREF/2) | - | V |
| swing w.r.t. VREF | X4-HIGH | - | ±(VREF/8) | - | V |
| Resolution | | - | 8 | - | Bits |
| Conversion time* | | - | 4.0 | - | µs |
| LSB voltage | X4=LOW | - | VREF/256 | - | mV |
| | X4=HIGH | - | VREF/1024 | - | mV |
| Differential linearity error | | - | - | ±0.75 | LSB |
| Relative accuracy** | | - | - | ±1.0 | LSB |
| Power supply sensitivity | | - | - | ±0.5 | LSB |

*A maximum of 2 µs of latency between a conversion request and the actual start of conversion must be added to this conversion time of 4 µs to calculate the total delay time from a conversion request to the completion of conversion.

**Relative accuracy is the deviation of the analog value at any code (relative to the full analog range of the A/D transfer characteristic) from its theoretical value (relative to the same range), after the full-scale range has been calibrated.

### Error D/A Converter

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| ERRDAC full-scale voltage swing w.r.t ERREF | | - | ±(VREF/2) | - | V |
| Resolution | | - | 8 | - | Bits |
| Conversion time* | | - | 4.0 | | µs |
| LSB voltage | | - | VREF/256 | - | mV |
| Output voltage at ERREF | | 1.56 | 1.61 | 1.66 | V |
| ERRDAC offset w.r.t. ERREF | | - | - | ±5 | mV |
| Differential linearity error | | - | - | ±0.5 | LSB |
| Relative accuracy** | | - | - | ±1.0 | LSB |
| Power supply sensitivity | | - | - | ±0.5 | LSB |

*A maximum of 2 µs of latency between a conversion request and the actual start of conversion must be added to this conversion time of 4 µs to calculate the total delay time from a conversion request to the completion of conversion.

**Relative accuracy is the deviation of the analog value at any code (relative to the full analog range of the D/A transfer characteristic) from its theoretical value (relative to the same range), after the full-scale range has been calibrated.

### Intel Microprocessor Interface Timing

The following timing specifications are applied when an Intel bus interface is selected by pulling the BUSMODE pin to logical HIGH. Timing measurements are defined in Figure 5 and made at 50% VDD with 50 pF load capacitances for all pins, unless otherwise noted.

| PARAMETER | SYMBOL | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Pulse width, ALE HIGH | $t_{ALPW}$ | 45 | - | - | ns |
| Muxed address valid time to ALE fall | $t_{AS}$ | 7.5 | - | - | ns |
| Muxed address hold time from ALE fall | $t_{AH}$ | 20 | - | - | ns |
| Read data delay time from $\overline{RD}$ fall | $t_{DDR}$ | - | - | 149 | ns |
| Read data hold time from $\overline{RD}$ rise | $t_{DHR}$ | 0 | - | 55 | ns |
| Pulse width, $\overline{RD}$ LOW | $t_{RDPW}$ | 200 | - | - | ns |
| Write data set up time to $\overline{WR}$ rise | $t_{DSW}$ | 70 | - | - | ns |
| Write data hold time from $\overline{WR}$ rise | $t_{DHW}$ | 10 | - | - | ns |
| Pulse width, $\overline{WR}$ LOW | $t_{WRPW}$ | 100 | - | - | ns |
| $\overline{RD}$ or $\overline{WR}$ delay time from ALE fall | $t_{RWD}$ | 25 | - | - | ns |
| $\overline{CS}$ valid time to ALE fall | $t_{CSS}$ | 0 | - | - | ns |
| $\overline{CS}$ hold time from $\overline{RD}$ or $\overline{WR}$ rise | $t_{CSH}$ | 0 | - | - | ns |
| $\overline{ASE}$ valid time to ALE fall | $t_{ASES}$ | 45 | - | - | ns |
| $\overline{ASE}$ hold time from ALE fall | $t_{ASEH}$ | 0 | - | - | ns |

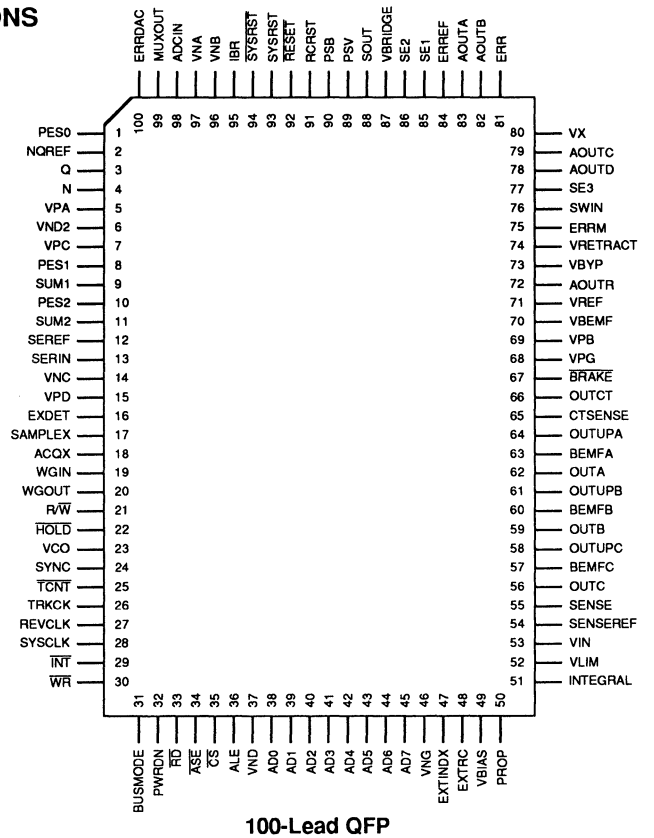
**Motorola Microprocessor Interface Timing**

The following timing specifications are applied when a Motorola bus interface is selected by pulling the BUSMODE pin to logical LOW. Timing measurements are defined in Figure 6 and made at 50% VDD with 50 pF load capacitances for all pins, unless otherwise noted.

| PARAMETER | SYMBOL | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Pulse width, AS HIGH | $t_{ASPW}$ | 45 | - | - | ns |
| Muxed address valid time to AS fall | $t_{AS}$ | 10 | - | - | ns |
| Muxed address hold time from AS fall | $t_{AH}$ | 20 | - | - | ns |
| Read data delay time from DS rise | $t_{DDR}$ | - | - | 180 | ns |
| Read data hold time from DS fall | $t_{DHR}$ | 0 | - | 80 | ns |
| Pulse width, DS HIGH during READ | $t_{DSPWR}$ | 200 | - | - | ns |
| Write data setup time to DS fall | $t_{DSW}$ | 70 | - | - | ns |
| Write data hold time from DS fall | $t_{DHW}$ | 10 | - | - | ns |
| Pulse width, DS HIGH during WRITE | $t_{DSPWW}$ | 100 | - | - | ns |
| DS delay time from AS fall | $t_{ASDS}$ | 25 | - | - | ns |
| R/$\overline{W}$ delay time from AS fall during WRITE | $t_{ASRW}$ | 25 | - | - | ns |
| R/$\overline{W}$ hold time from DS fall during WRITE | $t_{RWH}$ | 0 | - | - | ns |
| $\overline{CS}$ valid time to AS fall | $t_{CSS}$ | 0 | - | - | ns |
| $\overline{CS}$ hold time from DS fall | $t_{CSH}$ | 0 | - | - | ns |
| $\overline{ASE}$ valid time to AS fall | $t_{ASES}$ | 45 | - | - | ns |
| $\overline{ASE}$ hold time from AS fall | $t_{ASEH}$ | 0 | - | - | ns |

## PACKAGE PIN DESIGNATIONS

(Top View)




100-Lead QFP

CAUTION: Use handling procedures necessary for a static sensitive component.

6

## ORDERING INFORMATION

| PART DESCRIPTION | ORDER NUMBER | PACKAGE MARK |
|---|---|---|
| SSI 32H4633 100-Lead QFP | 32H4633-CG | 32H4633-CG |

**Preliminary Data:** Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.



Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 573-6000, FAX (714) 573-6914

**Notes:**

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# SSI 32H6110
## Differential Amplifier

December 1992

## DESCRIPTION

The SSI 32H6110 is a high performance, differential amplifier used as a preamplifier for the magnetic servo thin-film head in Winchester disk drives. The SSI 32H6110 is offered in an 8-pin SON package.

## FEATURES

- **High gain (Av=300)**
- **Low noise, 0.85 nV/$\sqrt{Hz}$ maximum**
- **Operates with a +5V power supply**

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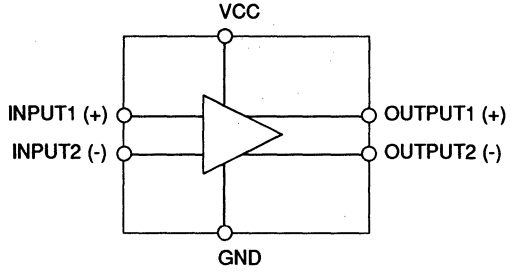
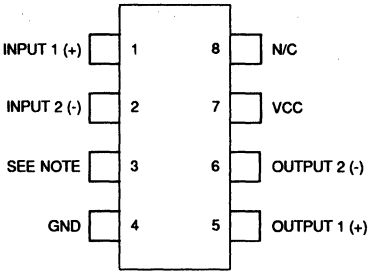
## BLOCK DIAGRAM




## PIN DIAGRAM




**8-Pin SON**

CAUTION: Use handling procedures necessary for a static sensitive component.

# SSI 32H6110
# Differential Amplifier

## ELECTRICAL SPECIFICATIONS

**ABSOLUTE MAXIMUM RATINGS** – operating above maximum ratings may damage the device

| PARAMETER | RATING | UNIT |
|---|---|---|
| Power Supply Voltage (VCC) | 7 | V |
| Differential Input Voltage | ±1 | V |
| Storage Temperature Range | -65 to 150 | °C |
| Operating Ambient Temperature, Ta | 10 to 100 | °C |
| Operating Junction Temperature, Tj | 10 to 135 | °C |

**RECOMMENDED OPERATING CONDITIONS**

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Supply Voltage (VCC) | | 4.50 | 5.0 | 5.50 | V |
| Input Signal (Vin) | | | 1.0 | | mVpp |
| Ambient Temperature | | 0 | | +100 | °C |
| Operating Junction Temperature | | 0 | | +135 | °C |

**ELECTRICAL CHARACTERISTICS**
Unless otherwise specified, recommended operating conditions apply.

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| Gain (Differential) | $R_L$ = 120Ω | Vin = 1mVpp, $R_L$ = 120Ω<br>Ta = 25°C, f = 1 MHz | 225 | 300 | 375 | mV/mV |
| | $R_L$ = 100Ω | Vin = 1mVpp, $R_L$ = 100Ω<br>Ta = 25°C, f = 1 MHz | 200 | 250 | 300 | mV/mV |
| Bandwidth (3 dB) | | Vin = 1mVpp, $C_L$ = 15 pF<br>$R_L$ = 120Ω | 10 | 30 | | MHz |
| Gain Sensitivity (Supply) | | Ta = 25°C | | | 4.0 | %/V |
| Gain Sensitivity (Temp.) | | 15°C < Ta < 55°C | | | –0.16 | %/°C |
| Input Noise Voltage | | Input Referred, Rs = 0 | | 0.6 | 0.85 | $nV/\sqrt{Hz}$ |
| Input Capacitance (Differential) | | Vin = 1 mVpp, f = 5 MHz | | | 35 | pF |
| Input Resistance (Differential) | | | | 200 | | Ω |
| Common Mode Rejection Ratio (Input Referred) | | Vin = 100 mVpp, f = 1 MHz | 60 | | | dB |
| Power Supply Rejection Ratio (Input Referred) | | Vin = 100 mVpp, f = 1 MHz | 54 | | | dB |

**ELECTRICAL CHARACTERISTICS,** (Continued)
Unless otherwise specified, recommended operating conditions apply.

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Input Dynamic Range (Differential) | AC input voltage where gain falls to 90% of its small signal value, f = 5MHz, $R_L$ = 120Ω | 5.0 | | | mVpp |
| Output Offset Voltage (Differential) | Inputs shorted | -400 | ±50 | +400 | mV |
| Output Voltage (Common Mode) | Inputs shorted together and Outputs shorted, $R_L$ = 120Ω | VCC-0.56 | VCC-0.88 | VCC-1.2 | V |
| Single Ended Output Capacitance | | | | 10 | pF |
| Power Supply Current | VCC = 5V | | 23 | 34 | mA |
| Input DC Voltage | Common Mode | | 2.0 | | V |

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## APPLICATION INFORMATION

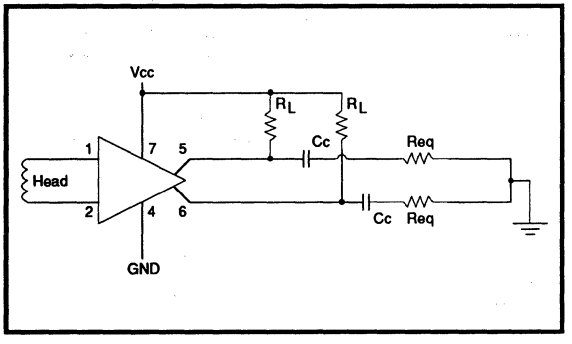


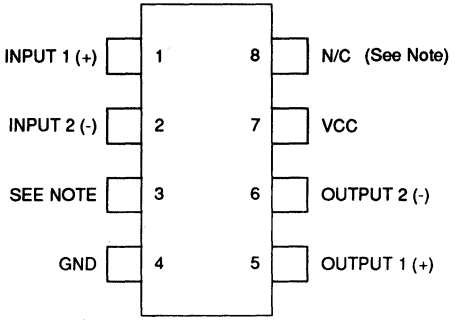

**FIGURE 1: Connection Diagram**

### RECOMMENDED LOAD CONDITIONS

1. Input is directly coupled to the head.
2. Cc's are AC coupling capacitors.
3. RL's are DC bias and termination resistors, 120Ω recommended.
4. REQ. represents equivalent load resistance.
5. Ceramic capacitors (0.1 µF) are recommended for good power supply noise filtering.

# SSI 32H6110
# Differential Amplifier

## PACKAGE PIN DESIGNATIONS
(Top View)




**8-Pin SON**

NOTE : N/C pin must be left open and not connected to any circuit etch.

## ORDERING INFORMATION

| PART DESCRIPTION | ORDERING NUMBER | PACKAGE MARK |
|---|---|---|
| SSI 32H6110 Differential Amplifier | | |
| 8-Pin SON | 32H6110-CN | H6110 |



Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 573-6000, FAX (714) 573-6914

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# SSI 32H6210
## Servo Demodulator

**Preliminary Data**

February 1992

## DESCRIPTION

The SSI 32H6210 Servo Demodulator is a bipolar device intended for use in Winchester disk drives with dedicated surface head positioning systems. It processes a di-bit quadrature pattern read from the servo surface by a preamplifier, such as the SSI 32H101 or SSI 32H116, and generates normal and quadrature (N and Q) position reference signals. These signals provide the servo controller with position error feedback. A complete position control system can be realized with the SSI 32H6210 and its companion devices, the SSI 32H6220 Servo Controller and SSI 32H6230 Servo Motor Driver.

The SSI 32H6210 incorporates an input amplifier with automatic gain control and offset cancellation, a phase locked loop and sync separator to recover timing information, and pulse area detectors to recover the position information. External components are used to set the operating characteristics of the SSI 32H6210, such as AGC response, VCO center frequency, PLL response and sync separator threshold. Its high performance analog/digital circuitry is capable of supporting servo frame rates of up to 400 kHz.

## FEATURES

- **Servo signal demodulation for dedicated surface head positioning systems**
- **Supports industry standard di-bit quadrature servo pattern with frame rates up to 400 kHz**
- **N, Q outputs convey track crossing and position error information**
- **PLL for timing recovery and synchronization**
- **Adjustable sync separator threshold**
- **Auto-zeroing AGC input amplifier**
- **AGC reference level adjustment**
- **Precision bandgap voltage reference output**
- **Advanced bipolar process dissipates less than 900 mW (5V, 12V)**
- **Available in 28-pin PLCC, DIP, SO packages**

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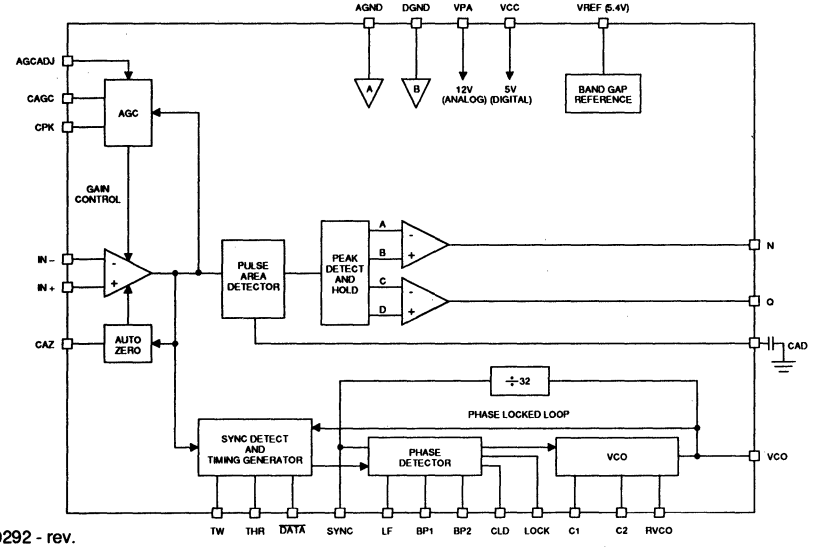
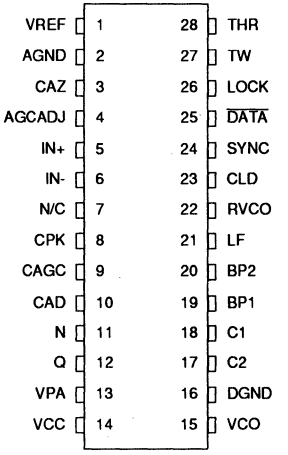
## BLOCK DIAGRAM




## PIN DIAGRAM




**28-PIN**
**DIP, SO**

## FUNCTIONAL DESCRIPTION

(Refer to block diagram, and typical application, Fig.2)

The SSI 32H6210 processes servo position information which is read from a dedicated surface by a pre-amplifier. The servo information must conform to the 'di-bit quadrature' pattern which is illustrated in Figure 4. Servo frames, consisting of data and sync pulses followed by four information pulses (A, B, C, D) are prerecorded along each track of the servo surface. All the servo frames on an individual track are identical, but in the radial direction four different frame types are encountered, with every fourth track being identical. The N signal generated by the SSI 32H6210 is proportional to the difference in sizes of pulses A and B, while the Q signal is proportional to the difference between pulses C and D. When the read head is off track, the read signal is effectively a linear interpolation between the prerecorded information of two adjacent tracks, making it possible to sense the head displacement exactly.

The SSI 32H6210 has a differential input amplifier which incorporates offset voltage cancellation and automatic gain control. An external read preamplifier must provide a differential input signal of 23 to 400 mV peak to peak from the servo read head. This signal is applied to a pulse detector whose output is proportional to the area under the input pulse.

An AGC circuit adjusts the input gain so that the maximum pulse detector output is 2V peak. The AGC circuit incorporates a peak detector which stores the maximum pulse area signal on the external capacitor $C_{PK}$. This signal is compared to an internal amplitude reference and the input amplifier gain is adjusted until they are equal. The capacitor $C_{AGC}$ determines the response time of the gain control circuit. An offset cancellation circuit , whose response is set with the external capacitor $C_{AZ}$, ensures that the average level at the differential amplifier output is zero.

An AGC adjust (AGCADJ) pin allows the user to adjust the AGC reference level. AGCADJ can be driven with a potentiometer or a D/A ( a simple Pulse Width Modulated signal is usually sufficient.) This pin is left open if no AGC adjustment is required.

All internal analog signals are referenced to a 5.4V bandgap reference voltage. This level is available at the VREF output, which is capable of supplying 10 mA to the rest of the servo path electronics.

In a standard servo frame, the data and sync pulses are more closely spaced than the information pulses (A-D). This allows the sync detect circuit to recover the SYNC pulses. A threshold, which is defined as percentage of the peak signal at the output of the AGC amplifier, is set externally with $R_{TH}$. Pulses which exceed this threshold are defined as valid pulses. As illustrated in Figure 6, at the end of the positive going half of a valid pulse, a window, whose width is set by Rw and Cw, is opened. If a second valid pulse occurs within this window, it is recognized as a SYNC pulse. This pulse becomes the input signal to a phase locked loop whose VCO clock frequency is 32 times the SYNC frequency (servo frame rate). The $\overline{DATA}$ output rises after a missing data pulse. The example illustrated in Figure 6 includes the case of a missing DATA pulse. The SYNC clock output, which marks the start of a new servo frame, is derived from the VCO output so that the clock continues to run when a data pulse is missing. Absolute positioning information such as track 0 and guardband flags may be encoded on the servo surface by the omission of data pulses.

To generate the servo pattern shown in the timing diagram, Figure 5, the DATA and SYNC pulses must be written to overlap as shown in Figure 7.

The phase detector compares the detected sync pulses with the SYNC output. A current pulse proportional to the phase error is applied to an external loop filter network connected to the LF pin, to generate the VCO control voltage. If improved power supply rejection is required, bypassing may be provided at pins BP1 and BP2. The VCO center frequency is determined by the external components $R_{VCO}$ and $C_{VCO}$.

A lock detect circuit measures the phase difference between the detected sync pulses and the sync output. When this difference exceeds half of a VCO clock cycle, a pulse of discharge current is applied to CLD. Otherwise a pulse of charging current is applied to CLD.

A clamp circuit limits the swing of the CLD pin and also insures that a small amount of hysteresis is present. When the voltage on CLD falls below the upper clamp level by more than the "lock margin," the open collector LOCK output transistor is turned on. Likewise, when the voltage on CLD rises above the lower clamp level by more than the "unlock margin," the LOCK output transistor is turned off.

## FUNCTIONAL DESCRIPTION (Continued)

Internal timing windows are generated from the recovered SYNC pulse and VCO clock. These windows, WA, WB, WC, and WD, in Figure 5, enable the four peak detectors to capture the A, B, C and D information pulses. The N and Q analog outputs are formed by differencing adjacent pulses. These outputs change during a servo frame and only become valid after the D pulse has been detected. N and Q should be sampled by the servo controller on the next falling edge of the SYNC output clock.

An example of an entire servo path implemented with the SSI 32H6210 and its companion devices, the SSI 32H6220 and SSI 32H6230, is shown in Figure 9.

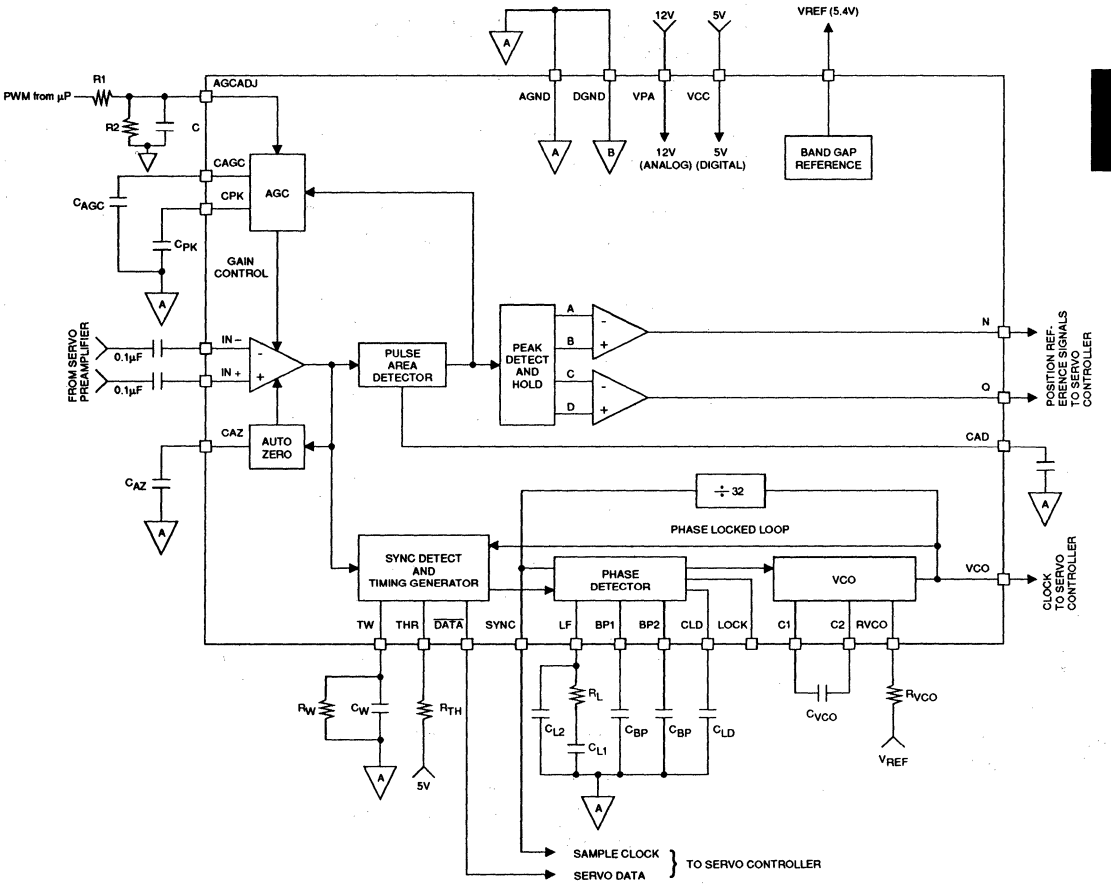



**FIGURE 2: Typical Application**

## PIN DESCRIPTION

### POWER

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| VREF | O | REFERENCE VOLTAGE - 5.4V output. All analog signals are referenced to this voltage. |
| AGND | - | ANALOG GROUND |
| VPA | - | ANALOG SUPPLY - 12V power supply. |
| VCC | - | DIGITAL SUPPLY - 5V power supply. |
| DGND | - | DIGITAL GROUND |

### INPUT AMPLIFIER

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| CAZ | - | AUTOZERO CAPACITOR - A capacitor which sets the response of the input amplifier offset cancellation circuit should be connected between this pin and analog ground. |
| IN + | I | NON-INVERTING INPUT - AGC input amplifier connection. The non-inverting output of the differential servo pre-amplifier should be AC coupled to this pin. |
| IN - | I | INVERTING INPUT - AGC input amplifier connection. The inverting output of the differential servo pre-amplifier should be AC coupled to this pin. |
| CPK | - | PEAK HOLD CAPACITOR - A capacitor which is used by the peak detector of the AGC circuitry must be connected between this pin and analog ground. |
| CAGC | - | AGC CAPACITOR - A capacitor which sets the AGC attack and decay times must be connected between this pin and analog ground. |
| AGCADJ | I | AGC Adjust - This pin allows for AGC reference level adjustment. It is driven by a potentiometer or D/A. Normally this pin is left open. |

### TIMING RECOVERY

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| VCO | O | VCO OUTPUT - TTL compatible digital clock which is 32 times the sync frequency (servo frame rate). |
| C2,C1 | - | VCO CAPACITOR - Connection points for a capacitor which sets the VCO center frequency in conjunction with an external resistor connected to RVCO. |
| BP1,BP2 | - | PLL BYPASS - Bypass capacitors may be connected between these pins and analog ground to provide additional power supply rejection in the phase locked loop. |

**TIMING RECOVERY** (Continued)

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| LF | - | PHASE LOCKED LOOP FILTER - An external RC network which sets the PLL loop characteristics must be connected between this pin and analog ground. |
| RVCO | - | VCO RESISTOR - Connection for a resistor which sets the VCO center frequency, in conjunction with the capacitor between pins C1 and C2. The resistor must be connected between this pin and the VREF output. |
| SYNC | O | SYNC OUTPUT - TTL compatible digital clock whose falling edge indicates the presence of valid analog signals on the N and Q outputs. There is one SYNC cycle per servo frame. |
| $\overline{\text{DATA}}$ | O | DATA OUTPUT - Active low TTL compatible digital output that indicates the presence of a data pulse in the servo frame. This signal is updated on the falling edge of the SYNC output. |
| TW | - | TIMING WINDOW - A resistor and capacitor must be connected in parallel between this pin and analog ground to set a timing window which is used in detecting SYNC pulses. |
| THR | - | PULSE THRESHOLD - A resistor which sets a threshold for SYNC and $\overline{\text{DATA}}$ pulse detection must be connected between this pin and VCC (digital 5V supply). |
| CLD | - | LOCK DETECT CAPACITOR - The value of this capacitor determines how quickly the LOCK output responds (1000 pF). |
| LOCK | O | LOCK OUTPUT - An open collector output that indicates the lock status of the PLL. |

**POSITION INFORMATION**

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| CAD | - | AREA DETECTOR CAPACITOR - A capacitor, which forms an integrator to sense the pulse area of the servo position signals, must be connected between this point and analog ground. |
| N | O | N OUTPUT - This sampled analog signal is the normal position reference output. N is referenced to VREF and is periodic in radial displacement, with a period of 4 tracks. |
| Q | O | Q OUTPUT - This sampled analog signal is the quadrature position reference output. Q is referenced to VREF and is periodic in radial displacement, with a period of 4 tracks. It is 90 degrees out of phase with N. |

## ELECTRICAL SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS

(Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC operating characteristics.)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| VCC voltage | | 0 | | 8 | V |
| VPA voltage | | 0 | | 16 | V |
| Voltage on PLL inputs | | -0.5 | | VCC+0.5 | V |
| Voltage on other inputs | | 0 | | 14 | V |
| Storage Temp. | | -45 | | 160 | °C |
| Solder Temp. | 10 sec. duration | | | 260 | °C |

**RECOMMENDED OPERATION CONDITIONS** (Unless otherwise noted, the following conditions are valid throughout this document.)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| VPA, analog supply | | 10.8 | 12 | 13.2 | V |
| Supply noise | F<1 MHz | | | 0.1 | Vpp |
| VCC, digital supply | | 4.75 | 5 | 5.25 | V |
| Ta, ambient temperature | | 0 | | 70 | °C |
| VCO operating range | | | | 12.8 | MHz |
| Load resistance | To VREF | 10 | | | kΩ |
| Load capacitance | | | | 50 | pF |

### DC CHARACTERISTICS

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| IPA, VPA current | | | | 50 | mA |
| ICC, VCC current | | | | 60 | mA |
| VOH, digital output high | \|IOH\|<40 µA | 2.4 | | | V |
| VOL, digital output low | \|IOL\|<1.6 mA | | | 0.5 | V |
| IREF, VREF output current capacity | | 10 | | | mA |
| VREF output voltage | \|IREF\|<10 mA | 5.1 | 5.4 | 5.7 | V |

## ELECTRICAL SPECIFICATIONS (Continued)

### AC CHARACTERISTICS

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| VREF output impedance | IOUT = 0-10 mA<br>1 µF bypass to AGND<br>Frequency<15MHz | | | 12 | Ω |
| **N, Q outputs** | | | | | |
| Output impedance | F = 1 MHz | | | 100 | Ω |
| Voltage per track | Referenced to VREF<br>23-400 mVpp differential<br>AGCADJ open | 1.8 | 2 | 2.2 | V |
| Offset voltage | | | | 20 | mV |
| Output noise | 10 Hz<F<1 kHz | | -55 | | dBV |
| **Input amplifier** | | | | | |
| Input resistance | | 5 | | | kΩ |
| Input resistance mismatch | | | | 1 | % |
| Input capacitance | | | | 20 | pF |
| PSRR | F<0.5MHz | 35 | | | dB |
| AGC headroom | | 2 | | | dB |
| AGC bandwidth | Open loop unity gain<br>$C_{AGC}$=0.04 µF<br>$C_{PK}$=1500 pF | 5 | | 15 | kHz |
| Autozero pole | $C_{AZ}$ in µF | | 220/$C_{AZ}$ | | Hz |
| **AGCADJ** | | | | | |
| Open circuit voltage | | 0.7 | 0.76 | 0.82 | V |
| Gain | | -1.6 | -1.4 | -1.2 | V/V |
| Volts per track adj range | | 1.0 | | 2.6 | V |
| Input impedance, $R_{AGC}$ | Ta = 25°C | 4 | 5.5 | 7 | kΩ |
| | Temp. coefficient | | 2600 | | ppm/°C |
| **SYNC detector** | | | | | |
| Timing window | Rw in Ω, Cw in pF | $0.4(Rw \cdot Cw) + 43 \cdot 10^{-9}$ | | | s |
| Valid pulse threshold | $R_{TH}$ in kΩ (% of full scale) | | 0.37/$R_{TH}$ | | % |

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## ELECTRICAL SPECIFICATIONS (Continued)

### AC CHARACTERISTICS (Continued)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| **LOCK Detector** | | | | | |
| CLD up current | RVCO = 11K ± 1% | 0.7 | | 3 | µA |
| CLD down current | RVCO = 11K ± 1% | 3 | | 10 | µA |
| CLD lock margin | | 0.5 | | 1.3 | V |
| CLD unlock margin | | 0.5 | | 1.3 | V |
| CLD hysteresis | | 75 | | 400 | mV |
| **Phase locked loop** | | | | | |
| Capture range | Centered on selected $f_{NOM}$ | ±5 | | | % |
| VCO phase shift | Missing DATA pulse | | | 0.005 | rad/frame |
| VCO phase delay | Relative to sync pulse zero crossing | | | 70 | ns |
| VCO gain | $f_{VCO}$ in Hz | | 10.47 $f_{VCO}$ | | rad/s/V |
| Phase detector gain | | | 32 | | uA/rad |

### TIMING CHARACTERISTICS

(Digital output load capacitance Cl<15 pF, VCO frequency $f_{VCO}$ <12.8 MHz, timing measurements for digital signals are measured at 1.3V, unless otherwise noted.)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| TDD, data delay | | | | 30 | ns |
| TW, sync pulse width | | 40 | | | ns |
| TSKW, SYNC to VCO skew | | 0 | | 40 | ns |
| SYNC fall time | | | | 20 | ns |
| TADS, N or Q output settling time | | | | 260 | ns |
| TADH, N or Q output hold time | | 0 | | | ns |

## APPLICATIONS INFORMATION

A typical SSI 32H6210 application is shown in Figure 2. The selection criteria for the external components shown are discussed below.

### INPUT AMPLIFIER

The autozero circuit is effectively a high pass filter, whose pole frequency is given by:

$$f_{AZ} = \frac{220}{C_{AZ}(\mu F)} Hz$$

With a value of 10 µF for $C_{AZ}$, the autozero circuit's corner frequency will be 22 Hz. This is sufficient for DC offset rejection and it will not interfere with the servo signal.

The AGC response may be characterized in terms of the open loop unity gain bandwidth of its control loop. The nominal value for this loop is set by $C_{AGC}$ as follows:

$$f_{BW} = \frac{390}{C_{AGC}(\mu F)} Hz$$

For a nominal bandwidth of 10 kHz, $C_{AGC}$ should be 0.039 µF. With a 1% capacitor, the variation in actual bandwidth will be +/- 50% due to the tolerance of internal components. The AGC peak detector capacitor should always be set to 1500 pF. This represents a reasonable tradeoff between leakage current tolerance and storage aperture time.

The pulse area detector storage capacitor must be chosen to keep the AGC circuit operating within its linear range. Its value is related to the VCO frequency as follows:

$C_{AD} = \frac{620}{f_{VCO}(MHz)}$ pF, where $f_{VCO}$ is the VCO freq.

Larger values for CAD are required with lower VCO frequencies in order to maintain constant signal levels within the device, since the integration time is increased.

$$K = 2\frac{V_{AGCADJ}(typ)}{VCC(min)} \qquad dv = \frac{\Delta V}{AGCADJGain(max)}$$

$$R1 = \frac{R_{AGC}(min)}{K}\left(\frac{V_{AGCADJ}(min)}{dv} - 1\right)$$

$$R2 = \frac{K}{1-K}(R1)$$

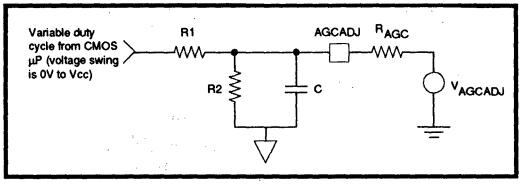


**FIGURE 3: AGCADJ Input**

for example if: $\Delta V = 0.4V$, $VCC = 5V \pm 5\%$, $Ta = 0\text{-}70°C$
$VREF = 5.4V \pm 6\%$

then: $K = .318$, $dv = 0.26V$, $R1 = 20.4k$,
$R2 = 9.5k$

The amplitude of N & Q signals can be adjusted using the AGCADJ input. If it is desired to adjust the N & Q amplitude by $\pm \Delta V$ volts, the values of R1 and R2 can be calculated from K and dv as shown in figure 3.

When R1 & R2 are calculated, a filter capacitor C is calculated from the replication rate of the µP duty cycle output. The parallel combination of R1, R2, $R_{AGC}$ minimizes the ripple of $V_{AGC}$, and yet still provides sufficient response time to changes in duty cycle.

### SYNC DETECTOR

Two sync detector parameters may be adjusted with external components. The first is the valid pulse threshold. The threshold is expressed as a percentage of a full scale pulse (since the sync detector follows the AGC and input amplitude variations are removed). The threshold is determined with resistor $R_{TH}$ as follows:

$$Threshold = \frac{0.44}{R_{TH}(k\Omega)} \cdot 100(\%)$$

For example, a value of $R_{TH}$ = 1.0 kΩ sets the valid pulse threshold at 44% of full scale. This prevents false triggering on noisy signals, but does not unduly shorten the sync pulse.

A timing window is used to detect sync pulses, since the sync and data pulses are more closely spaced than any other pulses in a valid servo signal. The delay from the zero crossing of the data pulse to the leading edge of the sync pulse is 1.5 cycles of the VCO clock. The next most closely spaced pulses (which must be rejected by the sync detect circuit) are separated by 3

## APPLICATIONS INFORMATION (Continued)

### SYNC DETECTOR (Continued)

VCO cycles. Thus the timing window should be set for 2 cycles of the VCO clock, to allow reliable detection of the sync pulse while suppressing false syncs. The timing window is determined as follows:

$$0.4\,(R_W \cdot C_W) + 43 \cdot 10^{-9}$$

The resistor Rw should always be set to 5.6 kΩ, which means that for a 2 cycle window, Cw is given by:

$$Cw = \frac{900}{fvco(MHz)} - 19pF$$

For a 12.8 MHz clock, Cw should be chosen as 51 pF.

### LOCK DETECTOR

The LOCK detector behavior is controlled by the value of $C_{LD}$. A value too small will be prone to unlock prematurely and give false warnings to the system. A typical value for $C_{LD}$ is 0.001µF.

### PHASE LOCKED LOOP

The VCO center frequency is determined by Rvco and Cvco. Rvco should always be set to 11 kΩ ± 1%. Cvco may then be chosen by:

$$Cvco = \frac{830}{fvco} - 10.6pF,$$

where fvco is the desired center frequency in MHz.

For fvco = 12.8 MHz, Cvco = 54 pF and for fvco = 4 MHz, Cvco = 200 pF. If 1% tolerance external components are used, the VCO absolute frequency accuracy will be 15%. The VCO output frequency is related to the control voltage at the loop filter pin, $V_{LF}$, as follows:

$$fo/fvco = 1 + 1.667(V_{LF} - V_{BPI})$$

This means that the VCO gain, $K_0$, is given by:

$$K_0 = 2 \cdot \pi \cdot fvco(Hz) \cdot 1.667\ rads/s/V$$

The phase detector is a digitally controlled charge pump, which injects a current into the loop filter whose average value is proportional to the phase error. The detector gain, Kd, is fixed at 32 µA/rad. If a loop filter consisting of a series resistor and capacitor is used, as shown in Figure 2, the phase locked loop becomes a second order system with the following transfer function:

$$\frac{\text{phase error}}{\text{input phase}}(s) = \frac{(s/\omega n)^2}{1 + 2 \cdot \zeta \cdot s/\omega n + (s/\omega n)^2}$$

where:

$$\omega n\,(\text{natural freq.}) = \sqrt{((K_d \cdot K_0/(32 \cdot C_{L1}))}\ rad/s$$

$$\zeta(\text{damping factor}) = 0.5 \cdot R_L \cdot C_{L1} \cdot \omega n$$

As an example, the values for Cvco, $R_L$ and $C_L$ are

$$fvco = 12.8\,MHz,\ \omega n/(2 \cdot \pi) = 4600\,Hz,\ \zeta = 0.68$$

$$Cvco = \frac{830}{fvco} - 10.6 = 54pF$$

$$C_{L1} = \frac{K_d K_0}{32 \cdot \omega n^2} = \frac{(32 \cdot 10e-6)(10.47 \cdot f_{VCO})}{32(2 \cdot \pi \cdot 4600)^2} = .2\mu F$$

$$R_L = \frac{2 \cdot z}{C_{L1} \cdot \omega n} = 470\,\Omega$$

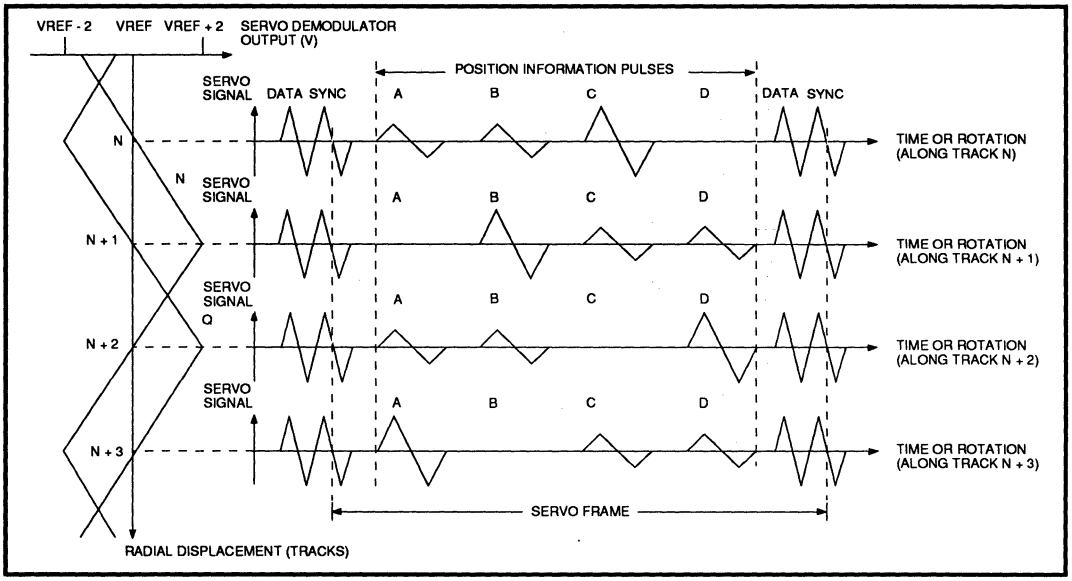


**FIGURE 4: Pre-recorded Servo Signal and Servo Demodulator Output vs. Radial Displacement**

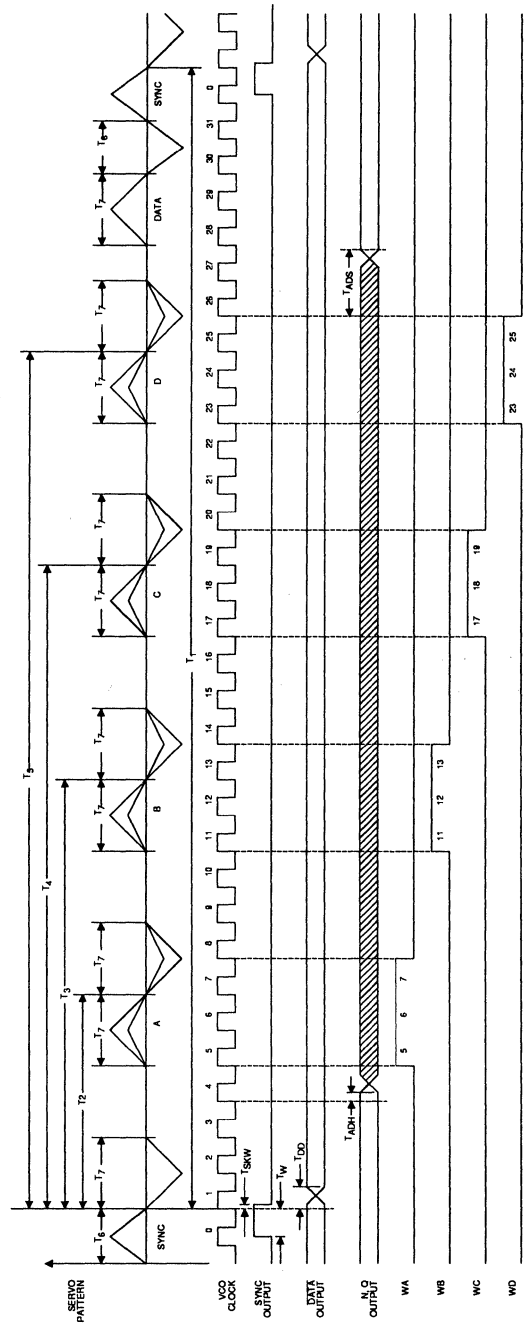


FIGURE 5: Timing Diagram

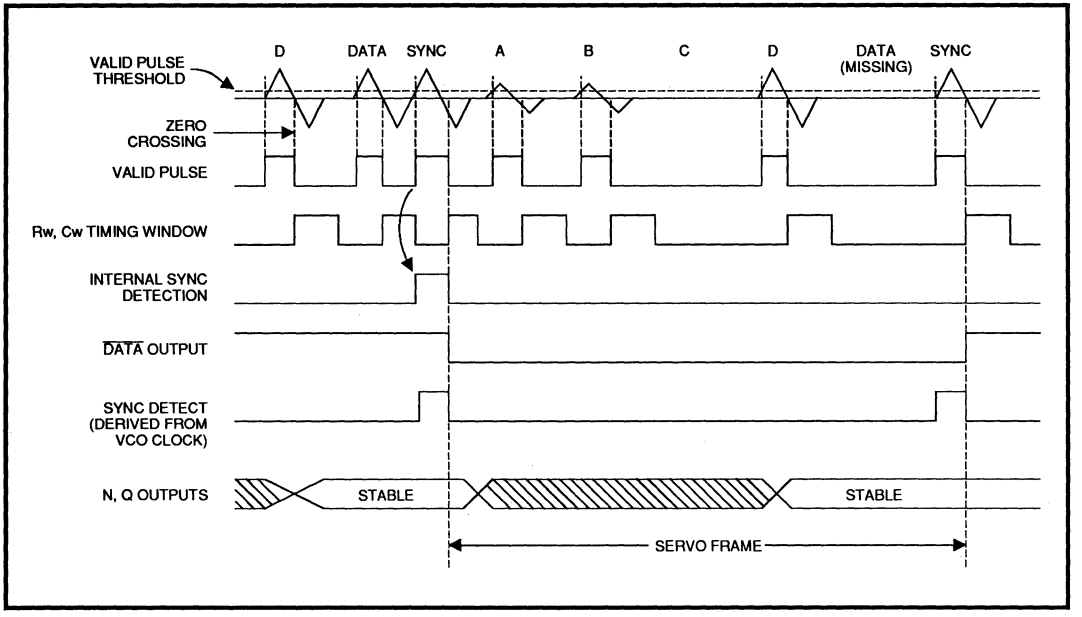


**FIGURE 6 : Sync and $\overline{DATA}$ Pulse Detection**

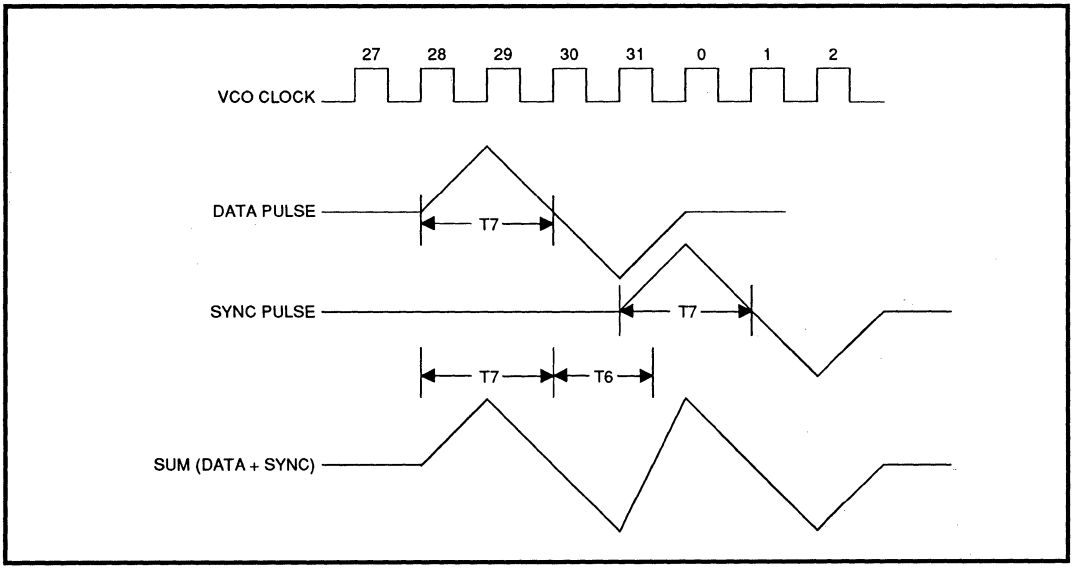


**FIGURE 7 : Servo Writer Data-Sync Pulse Generation**

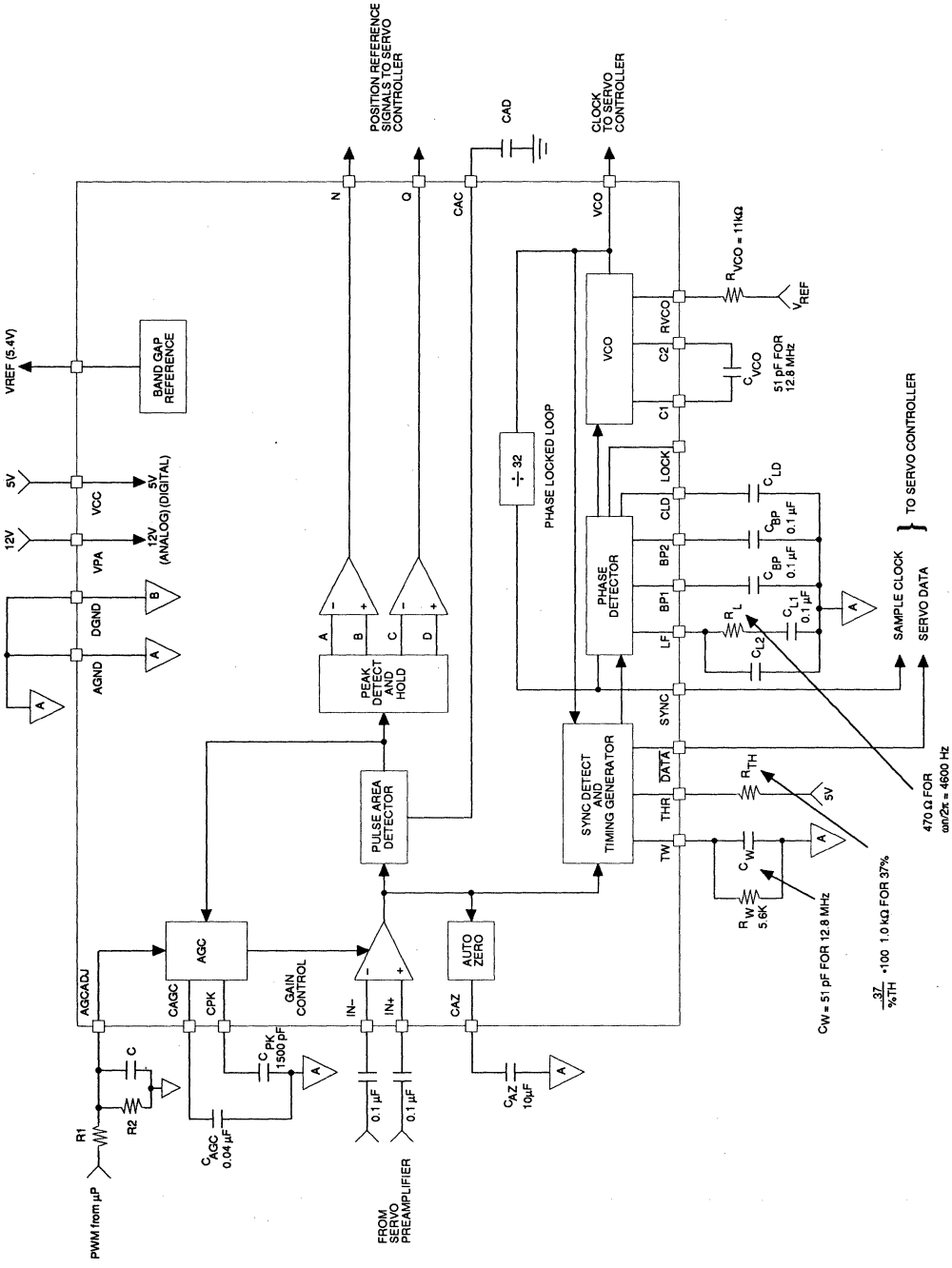


**FIGURE 8: Design Example for 400 kHz Frame Rate**

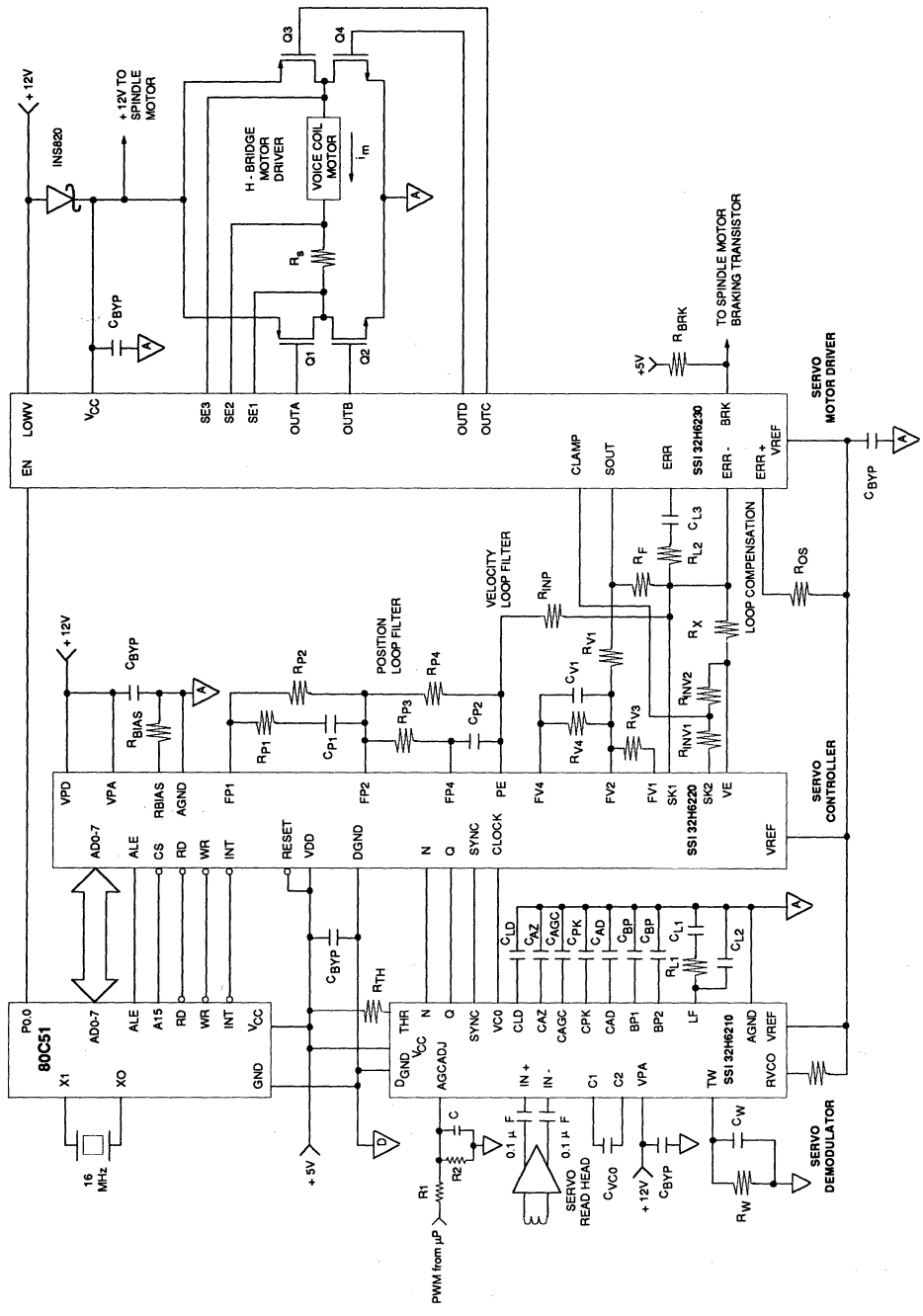


**FIGURE 9: Complete Example of Servo Path Electronics Using SSI 32H6210/6220/6230 Chip Set**

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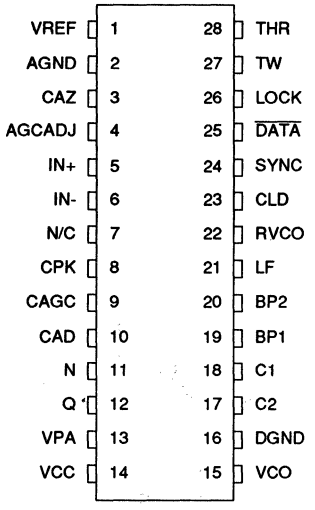
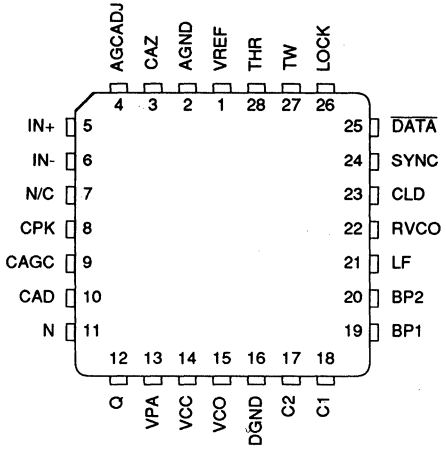
# SSI 32H6210
# Servo Demodulator

## PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.




**28-Pin DIP,SOL**




**28-Pin PLCC**

## ORDERING INFORMATION

| PART DESCRIPTION | ORDER NO. | PKG. MARK |
|---|---|---|
| SSI 32H6210 | | |
| 28-Pin DIP | 32H6210-CP | 32H6210-CP |
| 28-Lead SOL | 32H6210-CL | 32H6210-CL |
| 28-Lead PLCC | 32H6210-CH | 32H6210-CH |

**Preliminary Data:** Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.



Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 573-6000, FAX (714) 573-6914

# SSI 32H6215
## Servo Demodulator

**Advance Information**

January 1993

## DESCRIPTION

The SSI 32H6215 Servo Demodulator is a BiCMOS device intended for use in Winchester disk drives with dedicated surface head positioning systems. It processes a di-bit quadrature pattern read from the servo surface by a preamplifier, such as the SSI 32H6110, and generates normal and quadrature (N and Q) position reference signals. These signals provide the servo controller with position error feedback. A complete position control system can be realized with the SSI 32H6215 and its companion device, the SSI 32H4633 Servo Controller and Servo Motor Pre-Driver.

The SSI 32H6215 incorporates an input amplifier with automatic gain control and offset cancellation, a phase locked loop and sync separator to recover timing information, and pulse peak detectors to recover the position information. External components are used to set the operating characteristics of the SSI 32H6215, such as AGC response, VCO center frequency, PLL response and sync separator threshold. Its high performance analog/digital circuitry is capable of supporting servo frame rates of up to 500 kHz.

## FEATURES

- **Servo signal demodulation for dedicated surface head positioning systems**
- **Supports industry standard di-bit quadrature servo pattern with frame rates up to 500 kHz**
- **N, Q outputs convey track crossing and position error information**
- **PLL for timing recovery and synchronization**
- **Adjustable sync separator threshold**
- **AGC reference level adjustment**
- **Precision bandgap voltage reference output**
- **Advanced BiCMOS process dissipates less than 200 mW (5V)**
- **Available in 32-lead TQFP package**

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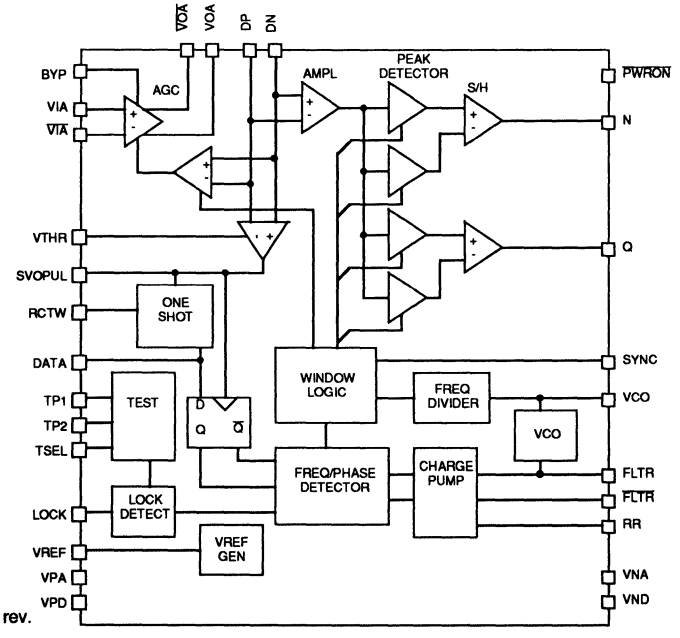
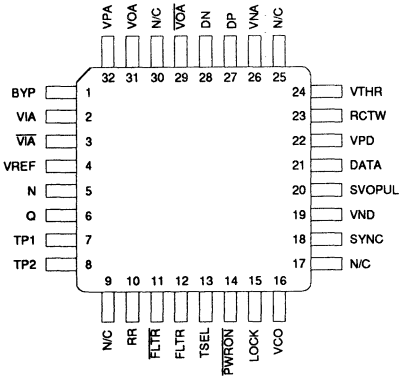
## BLOCK DIAGRAM




0193 - rev.

## PIN DIAGRAM




**32-Lead TQFP**

## FUNCTIONAL DESCRIPTION

The SSI 32H6215 processes servo position information which is read from a dedicated surface by a pre-amplifier. The servo information must conform to the 'di-bit quadrature' pattern. Servo frames, consisting of data and sync pulses followed by four information pulses (A, B, C, D) are prerecorded along each track of the servo surface. All the servo frames on an individual track are identical, but in the radial direction four different frame types are encountered, with every fourth track being identical. The N signal generated by the SSI 32H6215 is proportional to the difference in sizes of pulses A and B, while the Q signal is proportional to the difference between pulses C and D. When the read head is off track, the read signal is effectively a linear interpolation between the prerecorded information of two adjacent tracks, making it possible to sense the head displacement exactly.

The SSI 32H6215 has a differential input amplifier which incorporates offset voltage cancellation and automatic gain control. An external read preamplifier must provide a differential input signal of 23 to 400 mV peak to peak from the servo read head. This signal is applied to a pulse detector whose output is proportional to the area under the input pulse.

All internal analog signals are referenced to a 2.3V bandgap reference voltage. This level is available at the VREF output, which is capable of supplying 10 mA to the rest of the servo path electronics.

In a standard servo frame, the data and sync pulses are more closely spaced than the information pulses (A-D). This allows the sync detect circuit to recover the SYNC pulses. A threshold, which is defined as percentage of the peak signal at the output of the AGC amplifier, is set externally with $V_{THR}$. Pulses which exceed this threshold are defined as valid pulses. At the end of the positive going half of a valid pulse, a window, whose width is set by Rw and Cw, is opened. If a second valid pulse occurs within this window, it is recognized as a SYNC pulse. This pulse becomes the input signal to a phase locked loop whose VCO clock frequency is 32 times the SYNC frequency (servo frame rate). The SYNC clock output, which marks the start of a new servo frame, is derived from the VCO output so that the clock continues to run when a data pulse is missing. Absolute positioning information such as track 0 and guardband flags may be encoded on the servo surface by the omission of data pulses.

The phase detector compares the detected sync pulses with the SYNC output. A current pulse proportional to the phase error is applied to an external loop filter network connected to the FLTR/$\overline{\text{FLTR}}$ pin, to generate the VCO control voltage. If improved power supply rejection is required, bypassing may be provided at pins BP1 and BP2. The VCO center frequency is determined by the external component RR.

## PIN DESCRIPTION

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| VPA | - | Analog Supply: 5V power supply. |
| VPD | - | Digital Supply: 5V power supply. |
| BYP | - | AGC Bypass: AGC bypass capacitor. |
| VOA | O | AGC Output: AGC analog output |
| $\overline{\text{VOA}}$ | O | AGC Output: AGC analog output. |
| DP | O | Differential Positive Input: Positive input of peak detect circuit. |
| DN | O | Differential Negative Input: Negative input of peak detect circuit. |
| VNA | - | Analog Ground. |
| VND | - | Digital Ground. |
| VTHR | - | Pulse Threshold: A resistor which sets a threshold for SYNC and DATA pulse detection must be connected between this pin and VCC (digital 5V supply). |
| SVOPUL | O | Servo Output Level. |
| RCTW | - | RC Timing Window: A resistor and capacitor must be connected in parallel between this pin and analog ground to set a timing window which is used in detecting SYNC pulses. |
| DATA | O | Data Output: Active high TTL compatible digital output that indicates the presence of a data pulse in the servo frame. This signal is updated on the falling edge of the sync pulses. |
| TP1 | I/O | Test Point 1. |
| TP2 | I/O | Test Point 2. |
| TSEL | I | Test Select. |
| $\overline{\text{PWRON}}$ | I | Power On: Active low power on input. |
| LOCK | O | Lock Output: An open collector output that indicates the lock status of the PLL. |
| SYNC | O | Sync Output: TTL compatible digital clock whose falling edge indicates the presence of valid analog signal on the N and Q outputs. There is one SYNC cycle per servo frame. |
| VCO | O | VCO Output: TTL compatible digital clock which is 32 times the sync frequency (servo frame). |
| FLTR | - | Phase Lock Loop Filter: An external RC network which sets the PLL loop characteristics must be connected between this pin and analog ground. |
| $\overline{\text{FLTR}}$ | - | Phase Lock Loop Filter: An external RC network which sets the PLL loop characteristics must be connected between this pin and analog ground. |
| VREF | O | Reference Voltage: All analog voltages are referenced to this voltage. |

## PIN DESCRIPTION (contiued)

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| N | O | N Output: This sampled and held analog output is the normal position reference output. N is referenced to VREF and is periodic in radial displacement with a period of 4 tracks. |
| Q | O | Q Output: This sampled and held analog output is the quadrature position reference output. Q is referenced to VREF and is periodic in radial displacement with a period of 4 tracks. |

## ELECTRICAL SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS

Operation beyond the maximum ratings may damage the device.

| PARAMETER | RATING |
|---|---|
| VCC voltage | 0 to 8V |
| VPA voltage | 0 to 8V |
| Voltage on PLL inputs | -0.5 to VCC + 0.5V |
| Voltage on other inputs | 0 to 8V |
| Storage Temp. | -45 to 160°C |
| Solder Temp. 10 sec. duration | 260°C |

### RECOMMENDED OPERATING CONDITIONS

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| VPA, analog voltage | | 4.5 | | 5.5 | V |
| Supply noise | | | | 0.1 | Vpp |
| VCC, digital supply | | 4.5 | | 5.5 | V |
| Ta, ambient temperature | | 0 | | 70 | °C |
| VCO operating range | | | | 16 | MHz |
| Load resistance | | 10 | | | kΩ |
| Load capacitance | | | | 50 | pF |

### DC CHARACTERISTICS

| | | | | | |
|---|---|---|---|---|---|
| IPA, VPA current | | | | 30 | mA |
| ICC, VCC current | | | | 20 | mA |
| Sleep current | IPA + ICC | | | 0.5 | mA |
| VOH, digital output high | | 2.4 | | | V |
| VOL, digital output low | | | | 0.5 | V |
| IREF, VREF output current capacity | | 10 | | | mA |
| VREF output voltage | | | | | V |

### AGC AMPLIFIER

Input signals are AC coupled to VIA/$\overline{\text{VIA}}$, VOA/$\overline{\text{VOA}}$ outputs are AC coupled to DP/DN. A 1000 pF capacitor (CBYP) is connected from BYP to VCA. Unless otherwise specified outputs are measured differentially at VOA/$\overline{\text{VOA}}$, FIN = 4 MHz.

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Input Range | | 25 | | 375 | mVpp |
| DP-DN Voltage | VIA-$\overline{\text{VIA}}$ = 0.1Vpp | 0.9 | | 1.1 | Vpp |
| DP-DN Voltage variation | 25mV < VIA-$\overline{\text{VIA}}$ < 375mV | | | 8 | % |
| Gain Range | | 2.5 | | 40 | V/V |
| Differential input impedance | | 4.7 | 6 | 8.4 | kΩ |
| Single ended input impedance | | | 3.3 | | kΩ |
| Output offset voltage | Gain = 22 | -200 | | 200 | mV |
| Input noise voltage | Gain = 22, VIA/$\overline{\text{VIA}}$ short | | 10 | | nV/√Hz |
| CMRR | Gain = 22, $fc$ = 5MHz | 40 | | | dB |
| PSRR | Gain = 22, $fc$ = 5MHz | 45 | | | dB |
| Single ended output resistance | | | 150 | | Ω |

### AGC CONTROL

The input signals are AC coupled into DP/DN, CBYP = 1000 pF to VPA.

| | | | | | |
|---|---|---|---|---|---|
| Decay current | Normal delay (ID) | | 4 | | µA |
| Attack current | Normal attack (ICH) | | 0.18 | | mA |
| BYP Leakage current | | -10 | | 10 | nA |

### VOLTAGE REFERENCE

| | | | | | |
|---|---|---|---|---|---|
| Voltage | | 1.9 | 2 | 2.1 | V |
| Output Impedance | | | | 20 | Ω |
| Output current capability | | -0.5 | | 5 | mA |

### N,Q OUTPUTS

| | | | | | |
|---|---|---|---|---|---|
| Output impedance | | | | 250 | Ω |
| Volts per track | | 0.9 | 1 | 1.1 | V/track |
| Offset voltage | | | | 20 | mV |

## ELECTRICAL SPECIFICATIONS (continued)

### VCO

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| VCO center frequency | $fc$ | | TBD | | TBD | MHz |
| Frequency dynamic range | VCO | | ±25 | | ±45 | % |
| VCO control gain | KVCO | | 0.14 ωi | | 0.26 ωi | Rad/(V-s) |
| Phase detector gain constant | KD | | 0.83 KD | | 1.17 KD | A/rad |
| KVCO x KD product accuracy | | | -28 | | 28 | % |
| VCO output frequency | f VCO | | | | 16 | MHz |
| Precision external resistor | RR | | | 12.5 | | kΩ |

### VALID PULSE DETECTOR

| | | | | | | |
|---|---|---|---|---|---|---|
| Input voltage range | Vsd | At,DP, DN | 0.9 | 1 | 1.1 | Vpp |
| Threshold voltage | Vthr | Resistor divider from VPA to Vref | Vref | | | V |
| Threshold input current | Ithr | DP, DN shorted, Vth r= Vref + 0.5V | | | TBD | µA |
| Detector zero crossing | Tdp | Vsd=1.1Vpp Measured at SVOPUL T.P. | | | TBD | nsec |

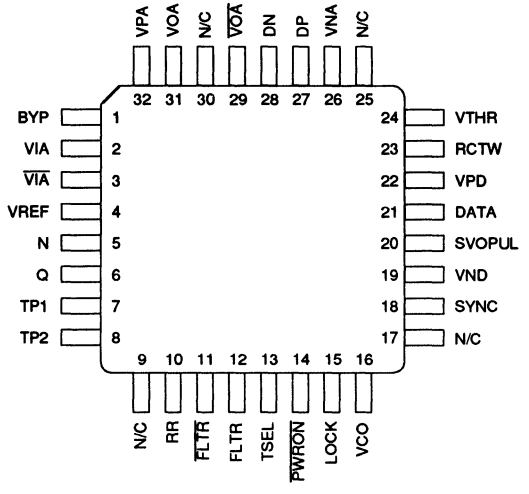
### SYNC SEPARATOR

| | | | | | | |
|---|---|---|---|---|---|---|
| Timing window | Tw | Rw(Ω), Cw(F) | | 0.92 RwCw | | Sec |
| Window resistance | Rw | | 10 | | | kΩ |
| RCTW output low voltage | Vol | | | | 0.1 | V |

## PACKAGE PIN DESIGNATIONS

(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.




**32-Lead TQFP**

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**Advance Information:** Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.



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**Notes:**

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A TDK Group Company

# SSI 32H6230
## Servo Motor Driver

**Preliminary Data**

December 1992

## DESCRIPTION

The SSI 32H6230 Servo Motor Driver is a bipolar device intended for use in Winchester disk drive head positioning systems employing linear or rotary voice coil motors. When used in conjunction with a position controller, such as the SSI 32H6220 Servo Controllers, and a position reference, such as the SSI 32H6210 Servo Demodulator, the device allows the construction of a high performance, dedicated surface head positioning system.

The SSI 32H6230 serves as a transconductance amplifier by driving 4 MOSFETs in an H-bridge configuration, performs motor current sensing and limits motor current. In its linear tracking mode, class B operation is guaranteed by crossover protection circuitry, which ensures that only one MOSFET in each leg of the H-bridge is active. The MOSFET drivers are disabled when motor velocity or current exceed externally programmable limits. In addition, automatic head retraction and spindle braking may be initiated by a low voltage condition or upon external command.

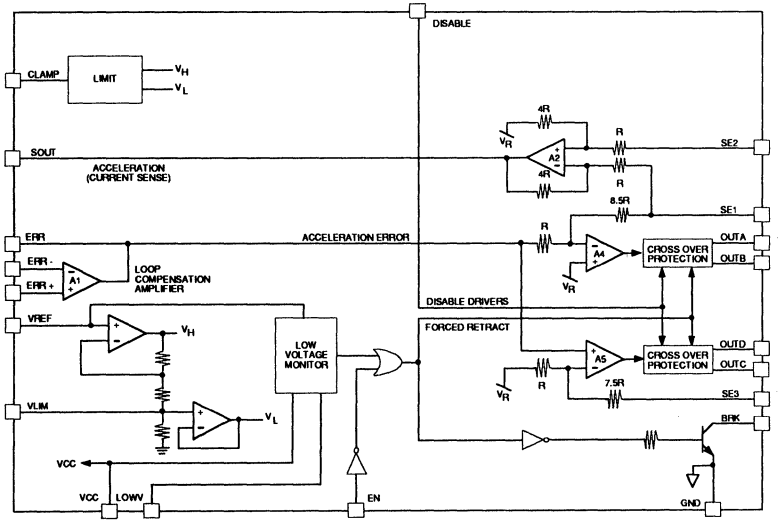
(Continued)

## FEATURES

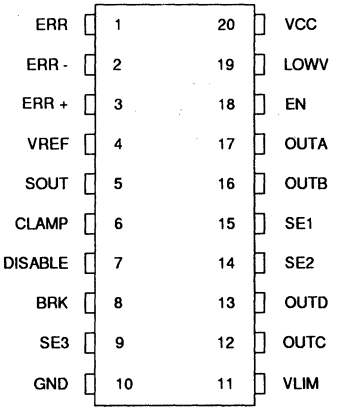
- **Predriver for linear and rotary voice coil motors**
- **Interfaces directly to MOSFET H-Bridge motor driver**
- **Class B linear mode and constant velocity retract mode**
- **FET disable function**
- **Precision differential amplifier for motor current sensing**
- **Clamp for motor current limiting**
- **Automatic head retract and spindle braking signal on power failure**
- **External digital enable**
- **Servo loop parameters programmed with external components**
- **Advanced bipolar IC requires under 240 mW from 12V supply**
- **Available in 20-pin DIP or SO packaging**

6

## BLOCK DIAGRAM




## PIN DIAGRAM



## DESCRIPTION (Continued)

The SSI 32H6230 is implemented in an advanced bipolar process and dissipates less than 240 mW from a 12V supply. The IC is available in 20-pin DIP and 20-pin SO packaging.

## FUNCTIONAL DESCRIPTION

(Refer to block diagram and typical application Fig.2)

The SSI 32H6230 has two modes of operation, linear and retract. The retract mode is activated by a power supply failure or when the control signal EN is false. Otherwise the device operates in linear mode.

During linear operation, an acceleration signal from the servo controller is applied through amplifier A1, whose three connections are all available externally. RC components may be used to provide loop compensation at this stage. The ERR signal drives two precision amplifiers, each with a gain of 8.5. The first of these amplifiers is inverting, and is formed from opamp A4, an on-chip resistor divider and an off-chip complementary MOSFET pair. The second is non-inverting, and is formed in a similar manner from opamp A5. Feedback from the MOSFET drains, on sense inputs SE1 and SE3, allows the amplifiers gains to be established precisely. The voice coil motor and a series current sense resistor are connected between SE1 and SE3.

Crossover protection circuitry between the outputs of A4 and A5, and the external MOSFETs, ensures class B operation by allowing only one MOSFET in each leg of the H-bridge to be in conduction. The crossover separation threshold, illustrated in Figure 5, is the maximum drive on any MOSFET gate when the motor voltage changes sign. The crossover circuitry can also disable all MOSFETS simultaneously (to limit motor current or velocity) or apply a constant voltage across the motor (to retract the heads at a constant velocity).

Motor current is sensed by a small resistor placed in series with the motor. The voltage drop across this resistor is amplified by a differential amplifier with a gain of 4 (A2 and associated resistors), whose inputs are SE1 and SE2. The resulting voltage, SOUT, is proportional to motor current, and hence acceleration. This signal is externally fed back to A1, so that the signal ERR represents the difference between the desired acceleration (from the servo controller) and the actual motor acceleration.

An adjustable voltage clamp is provided to prevent over current to the motor. It accomplishes the current limiting by clamping the voltage excursion at the input of A1. The voltage clamp values are programmed by VREF and VLIM. VLIM is the lower clamp value and the upper clamp limit is 2 • VREF - VLIM.

Disable function will cause all 4 bridge FETs to turn off. Note that this function does not override the retract function.

The SSI 32H6230 has low voltage monitor circuitry that will detect a loss of voltage on the VREF, VCC or LOWV pins. The power supply pin, VCC, should be connected to the disk drive's spindle motor so that its stored rotational energy may be used to hold up VCC briefly during a power failure. LOWV is used to detect a system power supply failure. When a low voltage condition is detected, the MOSFET drivers switch from linear operation to retract mode. In this mode a constant voltage is applied across the motor which will cause the heads to move at a constant speed. A mechanical stop must be provided for the heads when they reach a safe location. The current limiting circuitry will disable the MOSFET drivers when motor current increases due to loss of the velocity-induced back EMF. An open collector output, BRK, which is active while the device is in retract mode, is provided for spindle motor braking. An external RC delay may be used to defer braking until the heads are retracted.

Two examples of an entire servo path implemented with the SSI 32H6230 and its companion devices, the SSI 32H567, 32H568, and the SSI 32H6210, 32H6220 are shown in Figure 7.

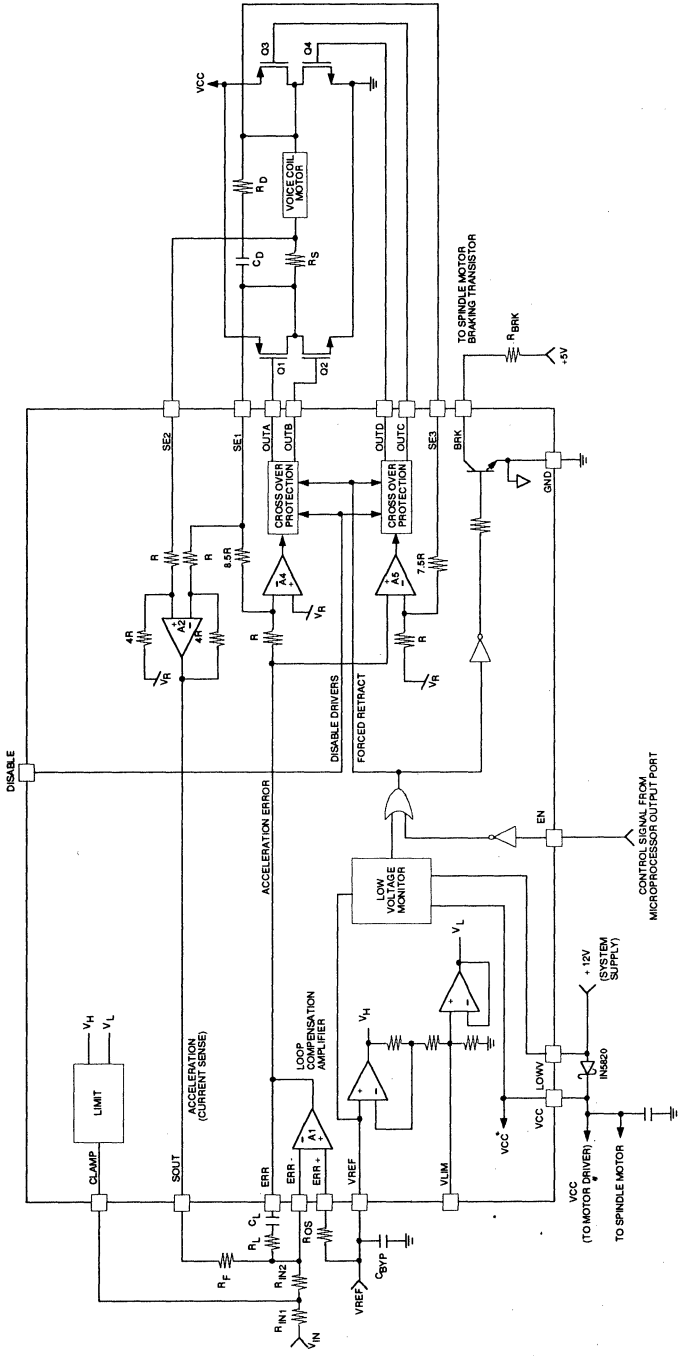



FIGURE 2: Typical Application

## PIN DESCRIPTION

### POWER

| NAME | PIN | TYPE | DESCRIPTION |
|---|---|---|---|
| VCC | 20 | | POSITIVE SUPPLY - 12V power supply. Usually taken from spindle motor supply. Spindle motor stored energy permits head retraction during power failure. If VCC falls below 9V, a forced head retraction occurs. |
| LOWV | 19 | I | LOW VOLTAGE - System 12V supply. If this input falls below 9V, a forced head retraction occurs. |
| VREF | 4 | I | REFERENCE VOLTAGE - 5.4V input. All analog signals are referenced to this voltage. If VREF falls below 4.3V, a forced head retraction occurs. |
| GND | 10 | | GROUND |

### CONTROL

| NAME | PIN | TYPE | DESCRIPTION |
|---|---|---|---|
| ERR | 1 | O | POSITION ERROR- Loop compensation amplifier output. This signal is amplified by the MOSFET drivers and applied to the motor by an external MOSFET H-bridge, as follows: SE3-SE1 = 17(ERR-VREF) |
| ERR- | 2 | I | POSITION ERROR INVERTING INPUT - Inverting input to the loop compensation amplifier. |
| ERR+ | 3 | I | POSITION ERROR NON-INVERTING INPUT - Non-inverting input to the loop compensation amplifier. |
| SOUT | 5 | O | MOTOR CURRENT SENSE OUTPUT - This output provides a voltage proportional to the voltage drop across the external current sense resistor, as follows: SOUT-VREF=4(SE2-SE1) |
| DISABLE | 7 | I | DISABLE INPUT – Active High TTL input will cause all 4 bridge FETs to turn off. DISABLE does not override the retract function. |
| CLAMP | 6 | I | CLAMP – A clamp pin to limit the input error voltage. The voltage swing at this pin is limited to VREF +- (VREF - VLIM). |
| BRK | 8 | O | BRAKE OUTPUT – Active high, open collector output which may be used to enable an external spindle motor braking transistor upon power failure or deassertion of EN. |
| VLIM | 11 | I | VOLTAGE LIMIT – The voltage at this pin sets the upper and lower clamp voltage limits in conjunction with the voltage at VREF.<br>Upper Clamp Limit = 2 • VREF - VLIM<br>Lower Clamp Limit = VLIM. |
| SE2 | 14 | I | MOTOR CURRENT SENSE INPUT - Non-inverting input to the current sense differential amplifier. It should be connected to one side of an external current sensing resistor in series with the motor. The inverting input of the differential amplifier is connected internally to SE1. |
| EN | 18 | I | ENABLE - Active high TTL compatible input enables linear tracking mode. A low level will initiate a forced head retract. |

**FET DRIVE**

| NAME | PIN | TYPE | DESCRIPTION |
|---|---|---|---|
| SE3 | 9 | I | MOTOR VOLTAGE SENSE INPUT - This input provides feedback to the non-inverting MOSFET driver amplifier. It is connected to one side of the motor. The gain to this point is:<br>SE3-VREF = 8.5(ERR-VREF) |
| OUTC | 12 | O | P-FET DRIVE (NON-INVERTING) - Drive signal for a P channel MOSFET connected between one side of the motor and VCC. This MOSFET drain is connected to SE3. |
| OUTD | 13 | O | N-FET DRIVE (NON-INVERTING) - Drive signal for an N channel MOSFET connected between one side of the motor and GND. This MOSFET drain is connected to SE3. Crossover protection circuitry ensures that the P and N channel devices driven by OUTC and OUTD are never enabled simultaneously. |
| SE1 | 15 | I | MOTOR VOLTAGE SENSE INPUT - This input provides feedback to the inverting MOSFET driver amplifier. It is connected to the current sensing resistor which is in series with the motor. The gain to this point is:<br>SE1-VREF = -8.5(ERR-VREF)<br>This input is internally connected to the current sense differential amplifier inverting input. |
| OUTB | 16 | O | N-FET DRIVE (INVERTING) - Drive signal for an N channel MOSFET connected between the current sense resistor and GND. This MOSFET drain is also connected to SE1. |
| OUTA | 17 | O | P-FET DRIVE (INVERTING) - Drive signal for a P channel MOSFET connected between the current sense resistor and VCC. This MOSFET drain is also connected to SE1. Crossover protection circuitry ensures that the P and N channel devices driven by OUTC and OUTD are never enabled simultaneously. |

## ELECTRICAL SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS

(Maximum limits indicates where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC operating characteristics.)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| VCC | | 0 | | 16 | V |
| VREF | | 0 | | 10 | V |
| SE1, SE2, SE3, OUT D | | -1.5 | | 15 | V |
| All other pins | | -.3 | | VCC + .3 | V |
| Storage temperature | | -45 | | 165 | °C |
| Solder temperature | 10 sec duration | | | 260 | °C |

**RECOMMENDED OPERATION CONDITIONS** (Unless otherwise noted, the following conditions are valid throughout this document.)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| VCC | Normal Mode | 9 | 12 | 13.2 | V |
| | Retract Mode | 3.5V | | 14 | V |
| VREF | | 5 | | 7 | V |
| Operating temperature | | 0 | | 70 | °C |

### DC CHARACTERISTICS

| | | | | | |
|---|---|---|---|---|---|
| ICC, VCC current | | | | 20 | mA |
| IREF, VREF current | | | | 2 | mA |

### A1, LOOP COMPENSATION AMPLIFIER

| | | | | | |
|---|---|---|---|---|---|
| Input bias current | | | | 500 | nA |
| Input offset voltage | | | | 3 | mV |
| Voltage swing | About VREF | 2 | | | V |
| Common mode range | About VREF | ±1 | | | V |
| Load resistance | To VREF | 4 | | | kΩ |
| Load capacitance | | | | 100 | pF |
| Gain | | 80 | | | dB |
| Unity gain bandwidth | | 1 | | | MHz |
| CMRR | $f$ <20 kHz | 60 | | | dB |
| PSRR | $f$ <20 kHz | 60 | | | dB |

### A2, CURRENT SENSE AMPLIFIER

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| Input impedance | SE1 to SE2 | 3.5 | 5 | | kΩ |
| Input offset voltage | | | | 2 | mV |
| Output voltage swing | | VREF-4 | | VCC-1.2 | V |
| Common mode range | | 0 | | VCC-0.2 | V |
| Load Resistance | To VREF | 4 | | | kΩ |
| Load Capacitance | | | | 100 | pF |
| Output impedance | $f$ < 40 kHz | | | 20 | Ω |
| Gain (SOUT-VREF)/(SE1-SE2) | VSE2 = VREF | 3.9 | 4 | 4.1 | V/V |
| Unity gain bandwidth | | 1 | | | MHz |
| CMRR | $f$ < 20 kHz | 52 | | | dB |
| PSRR | $f$ < 20 kHz | 60 | | | dB |



### VOLTAGE CLAMP

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| CLAMP bias current | CLAMP = VREF | | | 0.1 | µA |
| Upper CLAMP limit (VREF + 1/3 VREF) | ICLAMP = 10 µA VLIM open | | $\frac{4}{3}$ VREF | | V |
| Lower CLAMP limit (VREF - 1/3 VREF) | ICLAMP = -10 µA VLIM open | | $\frac{2}{3}$ VREF | | V |
| CLAMP accuracy | \| ICLAMP \| = 10 µA | -3 | | 3 | % |
| CLAMP Impedance | 1.0 mA> \| ICLAMP \| >10 µA | | | 20 | Ω |
| VLIM Voltage | | | $\frac{2\,VREF}{3}$ | | V |
| VLIM Accuracy | | -1 | | +1 | % |

### POWER SUPPLY MONITOR

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| VCC fail threshold | | 8.5 | 9 | 9.8 | V |
| LOWV fail threshold | \|ILowv\| < 0.5 mA | 8.5 | 9 | 9.8 | V |
| VREF fail threshold | | 3.9 | 4.3 | 4.8 | V |
| Hysteresis (LOWV, VCC) | | | 250 | | mV |
| Hysteresis (VREF) | | | 110 | | mV |
| EN input low voltage | \|IIL\| < 0.5 mA | 0.8 | | | V |

**POWER SUPPLY MONITOR** (Continued)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| EN input high voltage | \|IIH\| < 40 uA | | | 2 | V |
| BRK voltage | normal mode, \|IOL\| < 1 mA | | | 0.4 | V |
| BRK leakage current | retract mode | | | 10 | µA |
| BRK delay (from power fail or EN false to BRK floating) | | | | 1 | ms |

**MOSFET DRIVERS**

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| SE3 Input impedance | To VREF | 10 | 25 | | kΩ |
| OUTA, OUTC voltage swing \|Io\|<1 mA | | 0.7 | | VCC-1 | V |
| OUTB, OUTD voltage swing \|Io\|<1 mA | | 1 | | VCC-1 | V |
| VTH, Crossover separation threshold | | | | 2 | V |
| Slew rate (OUTA, OUTB, OUTC, OUTD) | Cl<1000 pF | 1.4 | | | V/µs |
| Crossover time | 300 mV step at ERR | | | .5 | µs |
| Output impedance (OUTA,B,C,D) | | | 50 | | kΩ |
| Transconductance I(OUTA,B,C,D)/(ERR-VREF) | | | 8 | | mA/V |
| Gain (-(SE1-VREF)/(ERR-VREF) or (SE3-VREF)/(ERR-VREF) ) | | 8 | 8.5 | 9 | V/V |
| Offset current | $R_S$ = 0.2Ω, $R_F$ = $R_{IN}$, $V_{IN}$=VREF | | | 20 | mA |
| Retract motor voltage (SE1-SE3) | | 0.7 | 1 | 1.3 | V |

## APPLICATIONS INFORMATION

A typical SSI 32H6230 application is shown in Figure 2. The selection criteria for the external components shown are discussed below. Figure 3 shows the equivalent circuit and equations for the DC motor used in the following derivations. While the nomenclature chosen is for a rotating motor, the results are equally applicable to linear motors.

### MOTOR CURRENT SENSE AND LIMITING

The series resistor which senses motor current, Rs, is chosen to be small compared to the resistance of the motor, Rm. A value of Rs = 0.2Ω is typical in disk drive applications.

VLIM, RIN1, and RIN2 must be chosen to keep the motor current below Imax. The voltage clamp values programmed by VREF and VLIM must be chosen to cause limiting when the motor current reaches its maximum permissible current in amps, this value may be chosen as follows:

$$|Imax| = \frac{CLAMP}{RIN2} \cdot \frac{RF}{4 \cdot Rs}$$

Where the upper clamp limit is 2 • VREF - VLIM and the lower clamp limit is VLIM. If VLIM is left open, a value of 0.667 • VREF will appear. The upper clamp limit is then 1.33 • VREF and the lower clamp limit is 0.667 • VREF. The values of RIN1, RIN2 must be chosen to satisfy the maximum swing of Vin before limiting occurs,

$$Vin(max) = CLAMP\left(1 + \frac{RIN1}{RIN2}\right) - \frac{RIN1}{RIN2}(VREF) + VREF$$

and they should also satisfy the maximum current VCLAMP can source or sink

$$\frac{Vin\ (max)\ [Actual] - CLAMP}{RIN1} \leq 1mA$$

### LOOP COMPENSATION

The transfer function of the SSI 32H6230 in the application of Figure 2 is shown in Figure 4(a). If the zero due to RL and CL in the loop compensation circuit is chosen to cancel the pole due to the motor inductance, Lm, then the transfer function can be simplified as shown in Figure 4(b), under the assumption that this pole and the pole due to the motor mechanical response are widely separated. CL may then be chosen to set the desired open loop unity gain bandwidth.

$$C_L = \frac{68 \cdot R_s}{2 \cdot \pi \cdot R_F \cdot (R_m + R_s) \cdot BW}$$

where BW is the unity gain open loop bandwidth

$$R_L = \frac{L_m}{C_L \cdot (R_m + R_s)}$$

The closed loop response of the servo driver and motor combination, using the component values and simplifying assumptions given above, is given by:

$$\frac{i_m}{V_{in}}(s) = -\frac{1}{R_{in}} \cdot \frac{R_F}{4 \cdot R_s} \cdot \frac{1}{\left(1 + \frac{s}{2 \cdot \pi \cdot BW}\right)}$$

Where: Rin = RIN1 + RIN2

(This analysis neglects the pole due to the output impedance of the MOSFET drivers and the MOSFET gate capacitance, an effect that may be significant in some systems.)

RF is chosen to be sufficiently large to avoid overloading A2 ($R_F > 4\ k\Omega$). The input resistor, RIN, sets the conversion factor from servo controller output voltage to servo motor current. RIN is chosen such that the servo controller internal voltages are scaled conveniently. The resistor ROS is optional and cancels out the effect of the input bias current of A1.

$$R_{os} = R_{in} // R_F$$

The external components RD and CD have no effect on the motor dynamics, but may be used to improve the stability of the MOSFET drivers. The load represented by the motor, ZM, is given by:

$$ZM = (R_s + R_m)\left(1 + s\frac{L_m}{R_s + R_m}\right)\left(1 + \frac{K_m^2}{s \cdot J\theta \cdot (R_s + R_m)}\right)(\Omega)$$

At frequencies above $(Rs+Rm)/(2\pi \cdot Lm)$ Hz, this load becomes entirely inductive, which is undesireable. RD and CD may be used to add some parallel resistive loading at these frequencies.

### H-BRIDGE MOSFETS

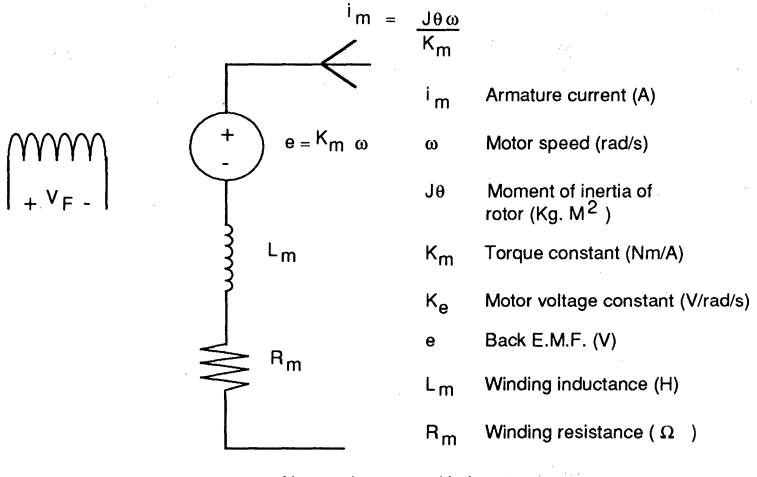
The MOSFETs chosen for the H-bridge should have gate capacitances in the range of 500-1000 pF. The MOSFET input capacitance forms part of the compensation for the MOSFET drivers, so values below 500 pF may cause some driver instability. Excessive input capacitance will degrade the slew mode performance of the drivers.

When the motor voltage is changing polarity, the crossover protection circuits at outputs OUTA-OUTD ensure that the maximum MOSFET gate drive is less than 2V (the crossover separation threshold), as illustrated in Figure 5. The thresholds of the MOSFET devices chosen should be as large as possible to minimize conduction in this region. If the device thresholds are significantly less than the crossover separation threshold, the N and P channel devices in each leg of the H-bridge will conduct simultaneously, causing unnecessary power dissipation.

### POWER FAILURE OPERATION

The power supply for the SSI 32H6230, VCC, should be taken from the system 12V supply through a schottky diode (maximum 0.5V drop at If = 3A) and connected to the disk drive spindle motor. If the system power fails, the IC will continue to operate as the spindle motor becomes a generator. The SSI 32H6230 will detect the power failure and cause a forced head retract, continuing to operate with VCC as low as 3.5V. The power fail mode will commence if either VCC or LOWV falls below 9V, or VREF falls below 4.3V, or EN is false. Hysteresis on the low voltage thresholds prevents the device from oscillating between operating modes when the power supply is marginal.

The BRK output, which is pulled low during normal operation, floats during a power failure. This allows an external transistor to be enabled for spindle motor braking. An external RC delay may be added to defer braking until head retraction is complete, since the spindle motor is required to generate the supply voltage during retraction.




Nomenclature used is for rotary motor

**FIGURE 3: Equivalent Circuit for Fixed Field DC Motor**

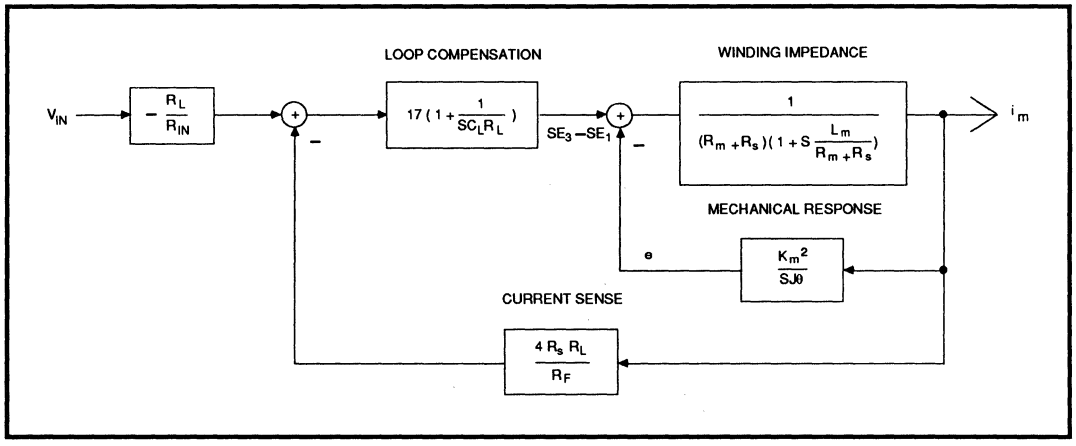



**FIGURE 4(A): Transfer Function of SSI 32H6230 in Typical Application with Fixed Field DC Motor**

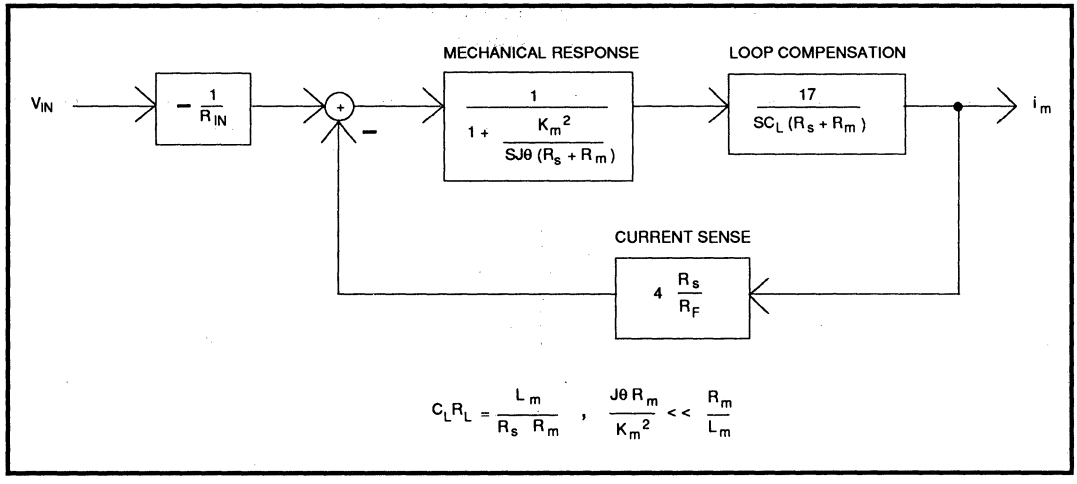



**FIGURE 4(B): Simplified Transfer Function of SSI 32H6230 in DC Motor Application**

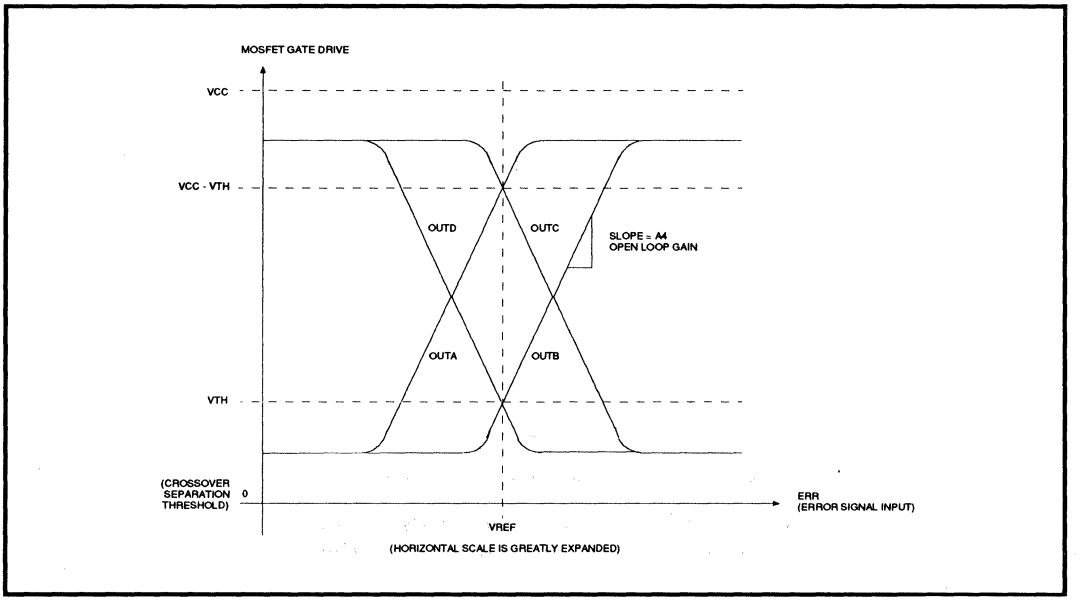



**FIGURE 5: Simplified Transfer Function of SSI 32H6230 in DC Motor Application**

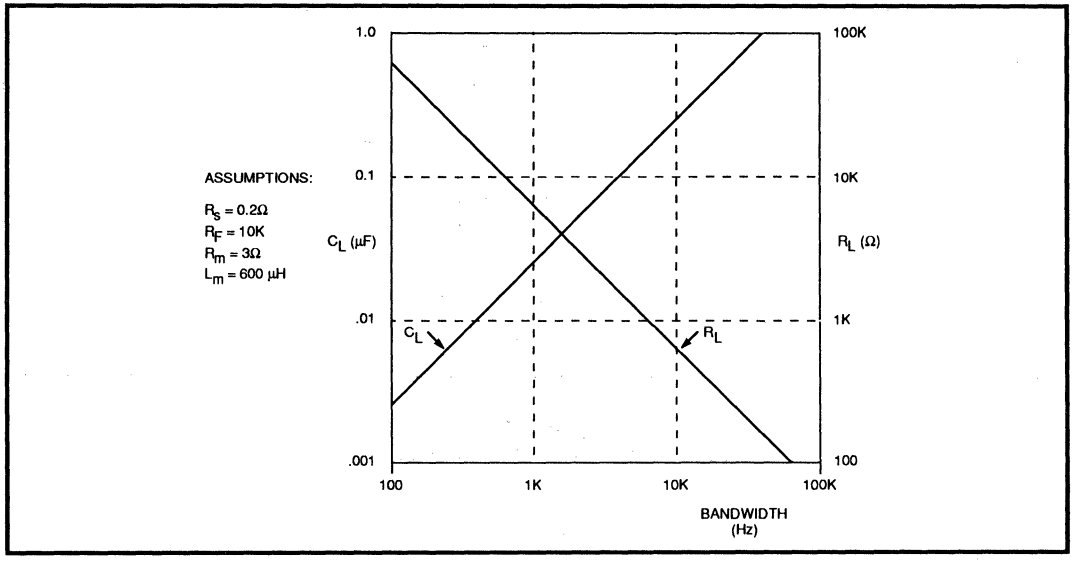



**FIGURE 6: Typical Motor Driver Compensation**

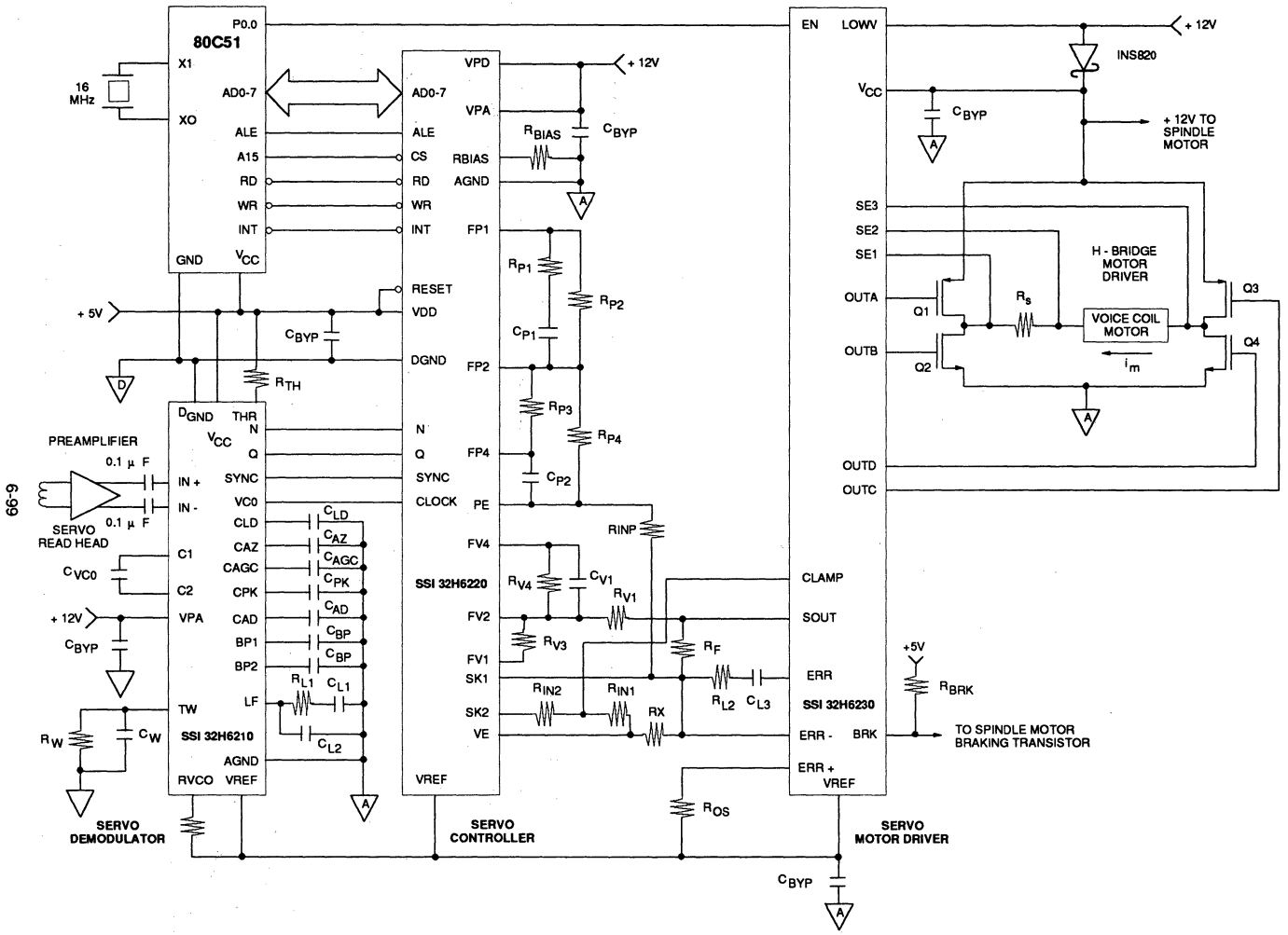
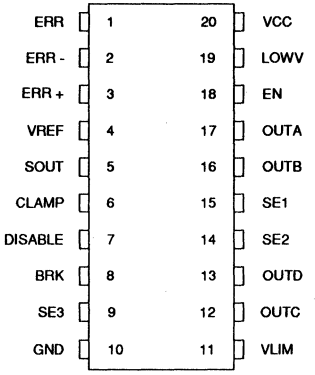



**FIGURE 7: Complete Example of Servo Path Electronics Using the SSI 32H6210/6220/6230 Chip Set**

# SSI 32H6230
# Servo Motor Driver

## PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.




**20-Pin DIP, SO**

## ORDERING INFORMATION

| PART DESCRIPTION | ORDER NO. | PKG. MARK |
|---|---|---|
| SSI 32H6230, Servo Motor Driver | | |
| 20-Pin DIP | 32H6230-CP | 32H6230-CP |
| 20-Lead SOL | 32H6230-CL | 32H6230-CL |

**Preliminary Data:** Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.



Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 573-6000, FAX (714) 573-6914

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A TDK Group Company

# SSI 32H6240
## Servo Motor Driver

**Advance Information**

December 1992

## DESCRIPTION

The SSI 32H6240 Servo Motor Driver is a bipolar device intended for use in Winchester disk drive head positioning systems employing linear or rotary voice coil motors. When used in conjunction with a position controller, such as the SSI 32H6220 Servo Controllers, and a position reference, such as the SSI 32H567 Servo Demodulator, the device allows the construction of a high performance, dedicated surface head positioning system.

The SSI 32H6240 serves as a transconductance amplifier by driving 4 bipolar power transistors in an H–bridge configuration and performs motor current sensing by using an on-chip differential amplifier. In its linear tracking mode, class B operation is guaranteed by crossover protection circuitry, which ensures that only one transistor in each leg of the H-bridge is active. Automatic head retraction and spindle braking may be initiated by a low voltage condition or upon external command.

The SSI 32H6240 is implemented in an advanced bipolar process and dissipates less than (240 mW) from a 12V supply. The SSI 32H6240 is available in a 28-pin PLCC.

## FEATURES

- **Predriver for linear and rotary voice coil motors**
- **Interfaces directly to Bipolar H-Bridge motor driver**
- **Class B linear mode and constant velocity retract mode**
- **Power transistor disable function**
- **Precision differential amplifier for motor current sensing**
- **On-chip precision power fail detect**
- **Automatic head retract and spindle braking signal on power failure**
- **External digital enable**
- **Servo loop parameters programmed with external components**
- **Advanced bipolar IC requires under (240 mW) from 12V supply**
- **Available in 28-pin PLCC packaging**
- **+5V, +12V operation**

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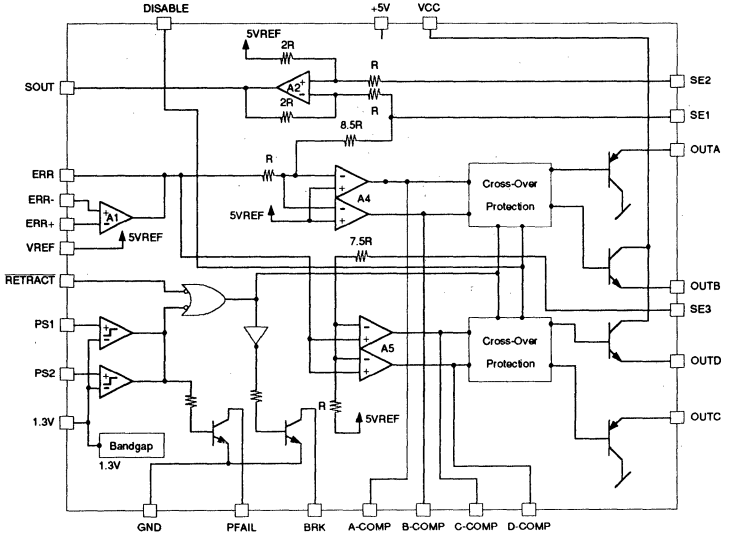
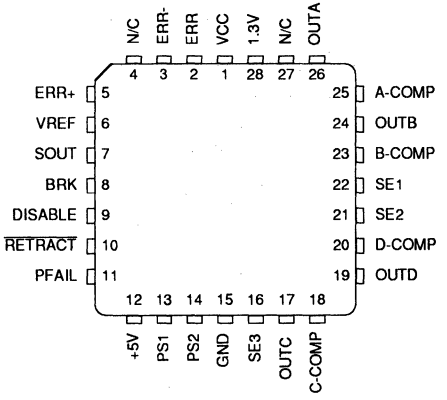
## BLOCK DIAGRAM




## PIN DIAGRAM




CAUTION: Use handling procedures necessary for a static sensitive component.

## FUNCTIONAL DESCRIPTION

(Refer to block diagram and typical application Fig.2)

There are three modes of operation of the SSI 32H6240: Disable, Retract, and Linear. The circuit mode is controlled by the DISABLE , $\overline{\text{RETRACT}}$, PS1, and PS2 pins.

DISABLE mode turns off the output drivers. OUTA and OUTC are pulled to VCC through internal 1.5 kΩ resistors. OUTB and OUTD are pulled to GND through internal 1.5 kΩ resistors. Disable mode does not override Retract mode.

RETRACT mode turns off OUTB and OUTC. OUTD is turned on. OUTA is turned on in a special manner to force 1V at SE1. Retract mode does override Disable mode.

POWER FAIL mode occurs when either PS1 or PS2 fall below 1.3V. Power fail overrides Retract and Disable inputs and forces the chip into RETRACT mode.

When the $\overline{\text{RETRACT}}$ pin is pulled low the SSI 32H6240 will go into retract mode. The BRK pin will go high. When the DISABLE pin is pulled high it will cause all 4 bridge power transistors to turn off. PFAIL and BRK will remain low if PS1, PS2, and $\overline{\text{RETRACT}}$ pins do not change.

During linear mode operation an acceleration signal from the servo controller is applied through amplifier A1. Amplifier A1's three connections are available for connection to external loop compensation components. The ERR signal drives two precision amplifiers, each with a gain of 8.5. The first of these amplifiers is inverting, and is formed from opamp A4, an on-chip resistor divider, and an off-chip complementary Bipolar Power Transistor pair. The second amplifier is non-inverting and is formed in a similar manner from opamp A5. Feedback from external transistor's collectors on sense inputs SE1 and SE3 allows the amplifier's gains to be precisely set. The voice coil motor and a series current sense resistor are connected between SE1 and SE3. The output of the amplifiers will provide the base current for the external H-Bridge Bipolar Power Transistors. The chip is designed to work with external transistors with a minimum Beta of 40 and minimum $f_T$ of 40 MHz. The base bias resistors for the external bridge transistors are internal to the IC.

Cross over protection circuitry between the outputs of A4 and A5 and the external power transistors ensure Class B operation by allowing only one transistor in each leg of the H-bridge to be in conduction. The crossover circuitry can also disable all Power Transistors simultaneously (to limit motor current or velocity) or apply a constant voltage across the motor (to retract the heads at a constant velocity.)

Motor current is sensed by a small resistor placed in series with the motor. The voltage drop across this resistor is amplified by a differential amplifier with a gain of 2 (A2 and associated resistors), whose inputs are SE1 and SE2. The resulting output voltage, SOUT, is proportional to motor current, and hence acceleration. This signal is externally fed back to A1 so that the signal ERR represents the difference between the desired acceleration (from the servo controller) and the actual motor acceleration. The total output offset current (Vin = Vref, Rsense = 0.5 Ω) is less than 5.5 mA.

The SSI 32H6240 has low voltage monitor circuitry that will detect a decrease in the voltage at PS1 and PS2 pins. The +5V and +12V power supplies are divided down by external resistors and then compared to an internal 1.25V ±5% reference. The power supply pin, VCC, should be connected to the disk drive's spindle motor so that its stored rotational energy may be used to hold up VCC briefly during a power failure. When a low voltage condition is detected on either the PS1 or PS2 pins the BIPOLAR drivers switch from linear operation to retract mode. In this mode a constant voltage is applied across the motor which will cause the heads to move at a constant speed. A mechanical stop must be provided for the heads when they reach a safe location. External current limiting circuitry is required for both the linear and retract modes of operation. An open collector output, PFAIL, which is low in the linear mode, will go high to indicate a power failure. This signal is gated with the $\overline{\text{RETRACT}}$ input signal to force the chip into the Retract mode during power failure and to signal a BRK spindle. A BRK spindle is signaled by forcing a High level on the BRK open collector output which is normally low in the Linear mode. The BRK pin is provided for spindle motor braking. An external RC delay may be used to defer braking until the heads are retracted.

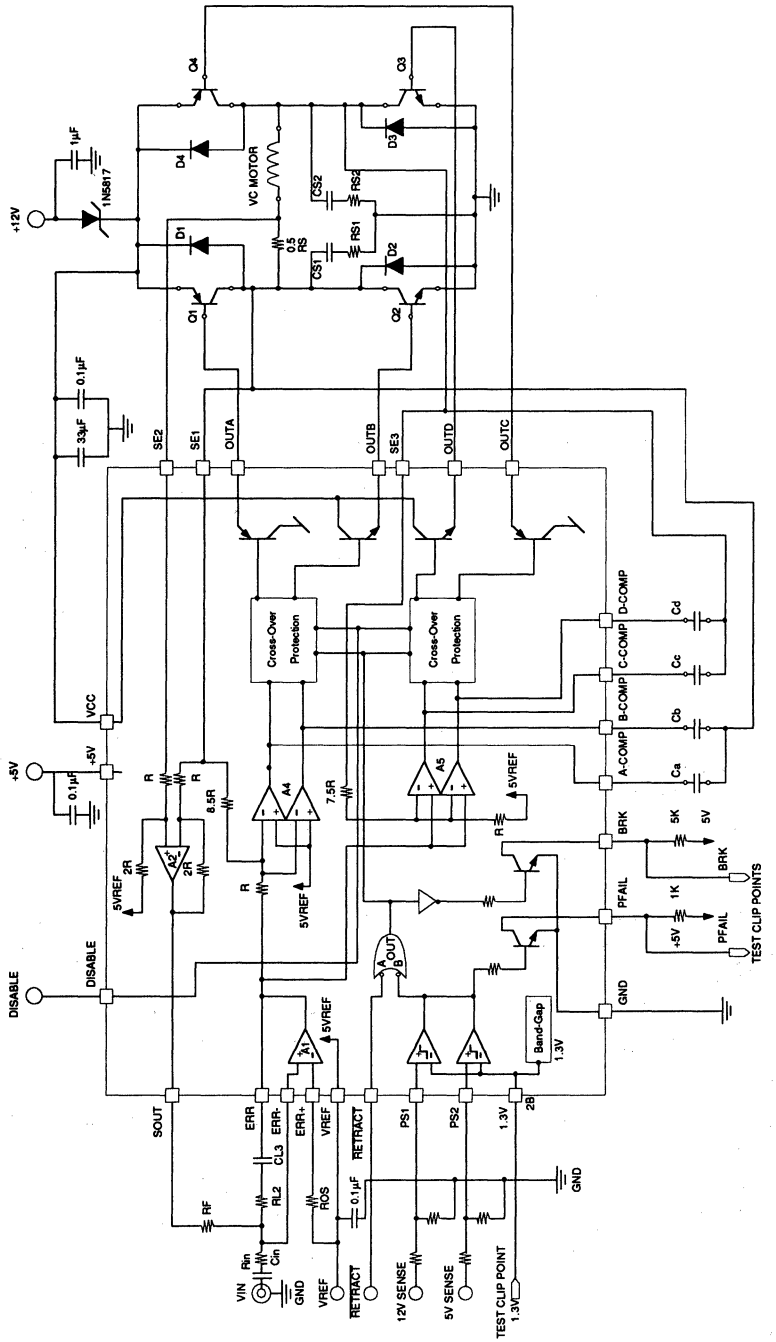



FIGURE 2: SSI 32H6240 Typical Application

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## PIN DESCRIPTION

### POWER

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| VCC | - | POSITIVE SUPPLY - Usually taken from spindle motor supply. Spindle motor stored energy permits head retraction during power failure. If either a "Power Failure" or a "Retract" is asserted a forced head retraction occurs. Usually supplied through a power Schottky diode from Spindle Motor Supply. |
| +5V | I | 5-volt power supply |
| VREF | I | REFERENCE VOLTAGE - 5.0V input. All analog signals are referenced to this input. |
| GND | - | GROUND |

### CONTROL

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| ERR | O | POSITION ERROR- Loop compensation amplifier output. This signal is amplified by the BIPOLAR drivers and applied to the motor by an external BIPOLAR H-bridge, as follows: SE3-SE1 = 17 (ERR-VREF) |
| ERR- | I | POSITION ERROR INVERTING INPUT - Inverting input to the loop compensation amplifier. |
| ERR+ | I | POSITION ERROR NON-INVERTING INPUT - Non-inverting input to the loop compensation amplifier. |
| SOUT | O | MOTOR CURRENT SENSE OUTPUT - This output provides a voltage proportional to the voltage drop across the external current sense resistor, as follows: SOUT-VREF=4 (SE2-SE1) |
| BRK | O | BRAKE OUTPUT - Active high, open collector output which may be used to enable an external spindle motor braking transistor upon power failure. External resistor may be tied to +5 or +12V. |
| DISABLE | I | DISABLE DRIVERS INPUT – Logic level input. An input high level will cause all 4 bridge BIPOLAR Power Devices to turn off. DISABLE does not override retract. |
| $\overline{\text{RETRACT}}$ | I | $\overline{\text{RETRACT}}$ INPUT – Logic level low will assert a forced head retraction. RETRACT will override DISABLE. $\overline{\text{RETRACT}}$ will continue to work at VCC=3.5V. |
| PS1 | I | POWER SENSE 1 – 12V sense input to power fail comparator. |
| PS2 | I | POWER SENSE 2 – 5V sense input to power fail comparator. |
| PFAIL | O | POWER FAIL – Power fail indicator open collector output. Floats if either supply goes below threshold. |
| 1.3V | O | INTERNAL REFERENCE MONITOR - Used for testing purposes only. |
| A-COMP | O | AMPLIFIER A COMPENSATION - Compensation capacitor pin |
| B-COMP | O | AMPLIFIER B COMPENSATION - Compensation capacitor pin |
| C-COMP | O | AMPLIFIER C COMPENSATION - Compensation capacitor pin |
| D-COMP | O | AMPLIFER D COMPENSATION - Compensation capacitor pin |

**CONTROL (Continued)**

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| SE2 | I | MOTOR CURRENT SENSE INPUT - Non-inverting input to the current sense differential amplifier. It should be connected to one side of an external current sensing resistor in series with the motor. The inverting input of the differential amplifier is connected internally to SE1. |

**BIPOLAR DRIVE**

| | | |
|---|---|---|
| SE3 | I | MOTOR VOLTAGE SENSE INPUT - This input provides feedback to the non-inverting BIPOLAR driver amplifier. It is connected to one side of the motor. The gain to this point is: SE3-VREF = 8.5 (ERR-VREF) |
| SE1 | I | MOTOR VOLTAGE SENSE INPUT - This input provides feedback to the inverting BIPOLAR driver amplifier. It is connected to the current sensing resistor which is in series with the motor. The gain to this point is: SE1 - VREF = -8.5 (ERR-VREF) |
| OUTA | O | PNP DRIVE (INVERTING) - Drive signal for a PNP power transistor connected between the current sense resistor and VCC. The PNP collector is also connected to SE1. Crossover protection circuitry ensures that the PNP and NPN devices driven by OUTA and OUTB are never simultaneously enabled. |
| OUTB | O | NPN DRIVE (INVERTING) - Drive signal for an NPN power transistor connected between the current sense resistor and GND. This NPN collector is also connected to SE1. |
| OUTC | O | PNP DRIVE (NON-INVERTING) - Drive signal for a PNP power transistor connected between one side of the motor and VCC. This PNP collector is connected to SE3. Crossover protection circuitry ensures that the PNP and NPN devices driven by OUTC and OUTD are never simultaneously enabled. |
| OUTD | O | NPN DRIVE (NON-INVERTING) - Drive signal for an NPN power transistor connected between one side of the motor and GND. This NPN collector is connected to SE3. Crossover protection circuitry ensures that the PNP and NPN devices driven by OUTC and OUTD are never simultaneously enabled. |

## ELECTRICAL SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS

(Maximum limits indicates where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC operating characteristics.)

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| VCC | | 0 | | 16 | V |
| VREF | | 0 | | 10 | V |
| +5V | | 0 | | 7 | V |
| SE1, SE2, SE3 | | -1.5 | | 15 | V |
| DISABLE, $\overline{\text{RETRACT}}$ | | -.3 | | +5V + .3 | V |
| All other pins | | -.3 | | VCC + .3 | V |
| Storage temperature | | -45 | | 165 | °C |
| Solder temperature | 10 sec duration | | | 260 | °C |

**RECOMMENDED OPERATION CONDITIONS** (Unless otherwise noted, the following conditions are valid throughout this document.)

| | | | | | |
|---|---|---|---|---|---|
| VCC | Normal Mode | 9 | 12 | 13.2 | V |
| | Retract Mode | 3.5V | | 13.2 | V |
| +5V | | 4.5 | 5 | 5.5 | V |
| VREF | | 4.5 | 5 | 5.5 | V |
| Operating temperature | | 0 | | 70 | °C |

### DC CHARACTERISTICS

| | | | | | |
|---|---|---|---|---|---|
| ICC, VCC current | | | 13 | 20 | mA |
| I5V, +5V Current | | | 0.6 | 1 | mA |
| IREF, VREF current | | | 300 | | µA |

### A1, LOOP COMPENSATION AMPLIFIER

| | | | | | |
|---|---|---|---|---|---|
| Input bias current | | | | 500 | nA |
| Input offset voltage | | | | 3 | mV |
| Voltage swing | About VREF | | 2 | | V |
| Common mode range | About VREF | ±1 | | | V |
| Load resistance | To VREF | 4 | | | kΩ |
| Gain | | | 80 | | dB |
| Unity gain bandwidth | | | 1 | | MHz |
| CMRR | f<20 kHz | | 60 | | dB |
| PSRR | f<20 kHz | | 60 | | dB |

### A2, CURRENT SENSE AMPLIFIER

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| Input impedance | SE1 to SE2 | 7.0 | 10 | | kΩ |
| Input offset voltage | SE1 = SE2 = VREF | | | 2 | mV |
| Output voltage swing | | VREF-4 | | VCC-1.2 | V |
| Common mode range | | 0 | | VCC-0.2 | V |
| Load Resistance | To VREF | 4 | | | kΩ |
| Output impedance | f<40 kHz | | | 20 | Ω |
| Gain (SOUT-VREF)/(SE1-SE2) | VSE2 = VREF | 1.95 | 2 | 2.05 | V/V |
| Unity gain bandwidth | | | 1 | | MHz |
| CMRR | f<20 kHz | | 52 | | dB |
| PSRR | f<20 kHz | | 60 | | dB |

### POWER SUPPLY MONITOR

| | | | | | |
|---|---|---|---|---|---|
| 1.3V pin voltage | 1.3V pin open | 1.18 | 1.25 | 1.31 | V |
| PS1 threshold | | | 1.25 | | V |
| PS2 threshold | | | 1.25 | | V |
| PS1, PS2 Hysteresis | | | 20 | | mV |
| PS1, PS2 Input Bias Current | PS1, PS2 = 1.3V | | 1 | | µA |
| PFAIL VOL | Linear mode IOC = 1mA | | | 0.4 | V |
| BRK VOL | Linear mode IOC = 1mA | | | 0.4 | V |
| PFAIL IOH | Retract mode VOH = 12V | | | 10 | µA |
| BRK IOH | Retract mode VOH = 12V | | | 10 | µA |
| DISABLE IIL | VIL = 0.8V | | 2 | 20 | µA |
| $\overline{\text{RETRACT}}$ IIL | VIL = 0.8V | | 2 | 10 | µA |
| DISABLE IIH | VIH = 2.4 | | 1 | 10 | µA |
| $\overline{\text{RETRACT}}$ IIH | VIH = 2.4 | | 1 | 10 | µA |
| DISABLE and $\overline{\text{RETRACT}}$ Threshold Voltage | | | 1.4 | | V |

**BIPOLAR DRIVERS**

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| SE3 Input Impedance | To VREF | 10 | 25 | | kΩ |
| A Comp, C Comp Voltage Swing | w/ External Trans. | VCC - 1.4 | | VCC - .7 | V |
| B comp, D Comp Voltage Swing | w/ External Trans. | 0.7 | | 1.4 | V |
| Output Impedance<br>A, B, C, D Comp | Output Off, No External Trans. | | 75 | | kΩ |
| Transconductance<br>I (A, B, C, D Comp)/(ERR-VREF) | | | 6 | | mA/V |
| Gain<br>-(SE1-VREF)/(ERR-VREF) or<br>(SE3-VREF)/(ERR-VREF) | Includes External Trans. | 8 | 8.5 | 9 | V/V |
| Offset Current<br>(A2 Vos) | Rs = 0.5Ω Rf = Rin<br>Vin = Vref | | 3.5 | | mA |
| Retract Motor Voltage<br>(SE1-SE3) | | 0.7 | 1.3 | 1.7 | V |
| Out B, Out D<br>Source Current | Vout = 0.8V | 20 | | | mA |
| Out B, Out D<br>Current Limit | Vcc = 10.8V, Out B, D = 0.8V<br>Vcc = 12.0V, Out B, D = 0.8V | 20<br>23 | 25<br>27 | 30<br>33 | mA<br>mA |
| Out A, Out C<br>Sink Current | Vout = 11.2V | 20 | | | mA |
| B and D Output<br>NPN Output Transistor Beta | Ic = 20mA Vce = 10V | | 20 | | V/V |
| A and C Output<br>PNP Output Transistor Beta | Ic = 20mA Vce = 10V | | 10 | | V/V |

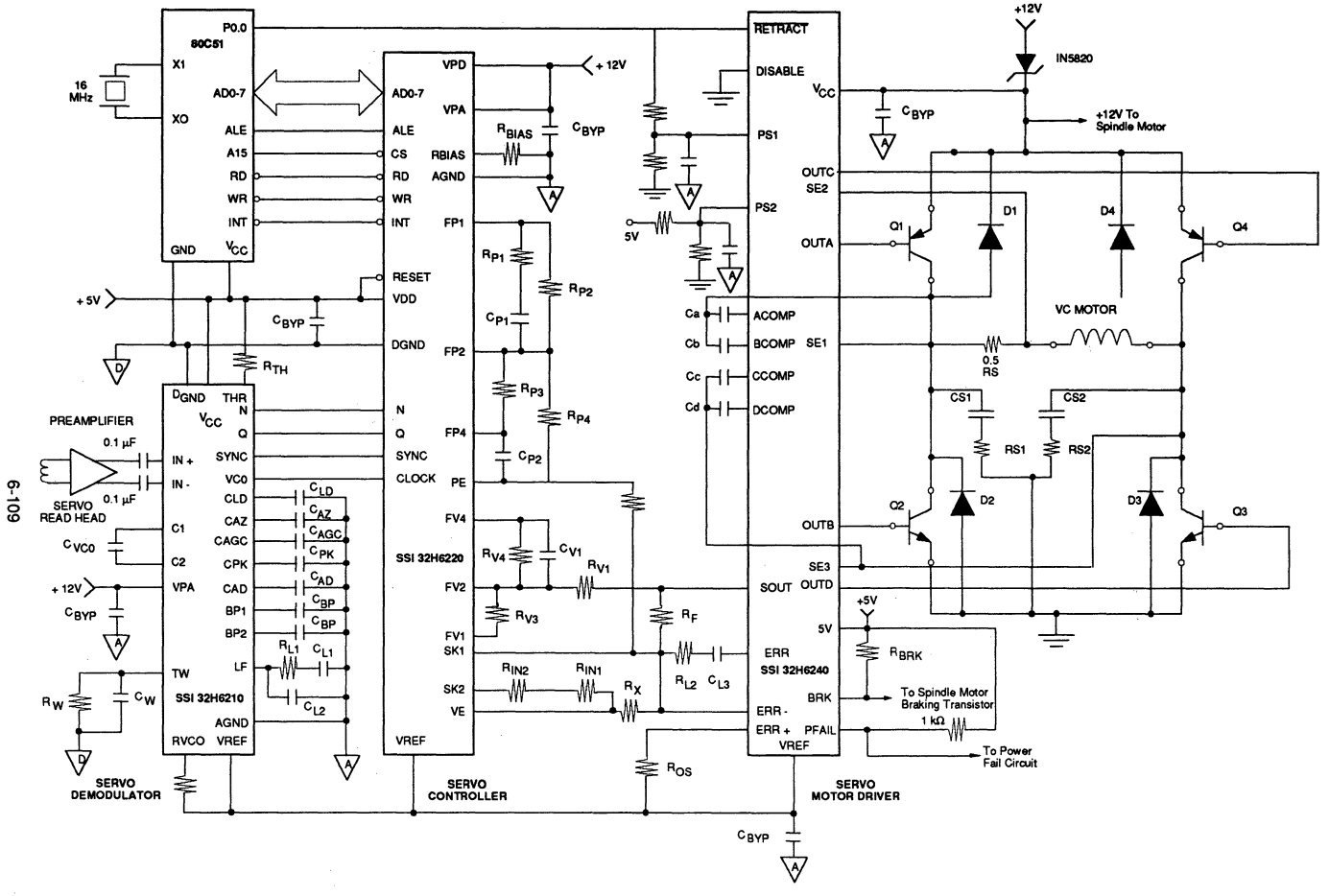
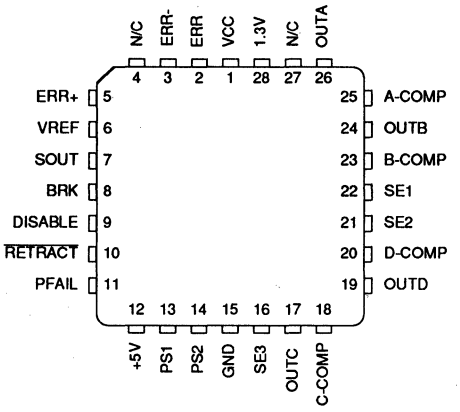



**FIGURE 3: Complete Example of Servo Path Electronics using the SSI 32H6210/6220/6240 Chip Set**

# SSI 32H6240
# Servo Motor Driver

## PACKAGE PIN DESIGNATIONS
(TOP VIEW)

CAUTION: Use handling procedures necessary for a static sensitive component.




**28-Pin PLCC**

**Advance Information:** Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.



Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680, (714) 573-6000, FAX: (714) 573-6914

# SSI 32H6510
## 5V Servo Driver

**Preliminary Data**

December 1992

## DESCRIPTION

The SSI 32H6510 is a fully integrated power amplifier for use in disk drive head positioning systems employing linear or rotary voice coil motors. It is intended for use in 5V systems and is capable of generating ±1 Amp motor currents. The part is internally thermal overload protected.

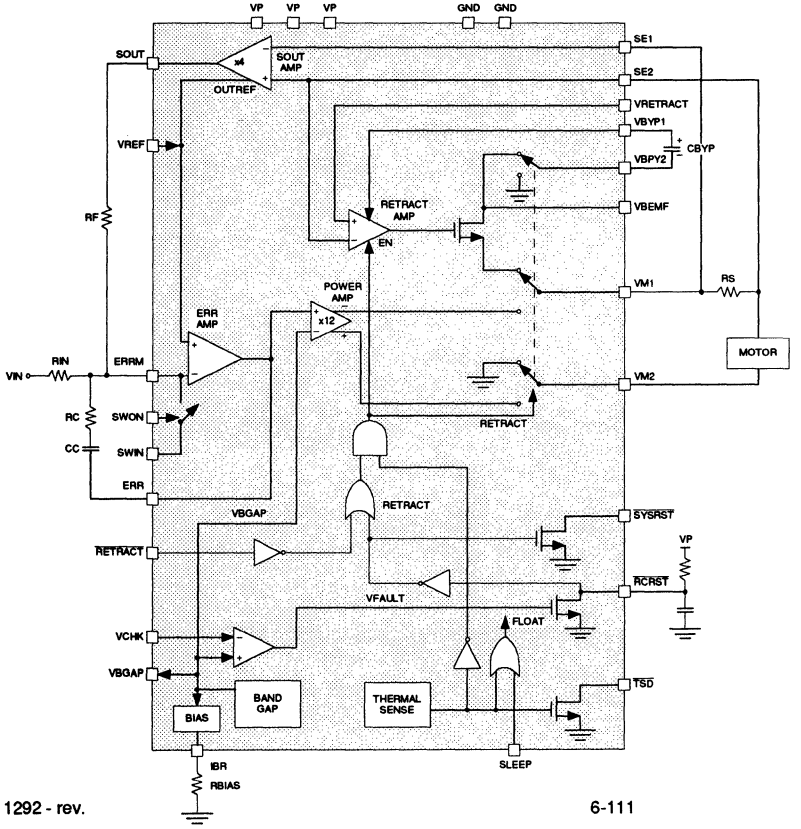
The SSI 32H6510 is a power transconductance amplifier for use in driving voice coil type servo motors (VCMs). The SSI 32H6510 has two primary modes of operation, normal (or linear) and retract. The retract mode is activated by a power supply failure or when $\overline{\text{RETRACT}}$ is asserted. Otherwise the device operates in linear mode.

## FEATURES

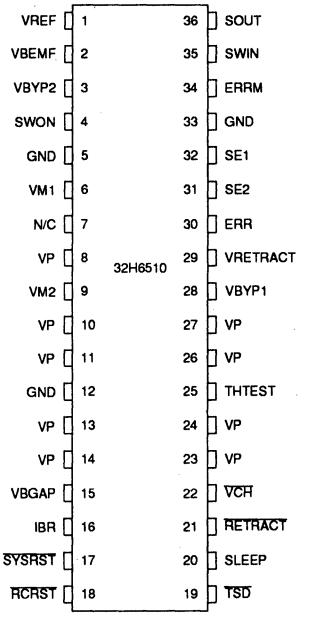
- **36-pin SO package**
- **Internal 1A power devices**
- **NMOS output stage**
- **Total on resistance less than 1.3Ω at 500 mA**
- **Thermal overload protection**
- **No deadband, low distortion, class B output**
- **Low power sleep mode**
- **Gain select switch optimizes performance with 8-bit DACs**
- **Built in retract circuitry**
- **Power fault detection**

6

## BLOCK DIAGRAM




## PIN DIAGRAM




CAUTION: Use handling procedures necessary for a static sensitive component.

## DESCRIPTION (continued)

The SSI 32H6510 consists of five major blocks: SOUT amplifier, ERR amplifier, retract amplifier, power amplifier, and control circuitry. These parts are each described in this section. External components needed for proper operation of the SSI 32H6510 are also described.

### SOUT AMPLIFIER

This amplifier generates a voltage at SOUT that is proportional to positioner current. It does this by sensing the voltage across Rs, amplifying it, and referencing the result to VREF. Since the common mode voltage on Rs can range over the full power supply, while the differential voltage is a few millivolts, the SOUT amplifier is designed to have very high input common mode rejection, and very low input offset.

### ERR AMPLIFIER

The ERR amplifier is a high gain op amp. Due to the fixed gain of the power amp, ERR is proportional to the VCM voltage. The negative input of this amplifier is the system summing junction--currents proportional to the desired VCM current, the measured VCM current, and the VCM voltage are summed here.

### POWER AMPLIFIER

The power amplifier is a fixed gain voltage amplifier with differential inputs and outputs. Its input is the differential voltage between ERR and VBGAP. Its output drives the VCM directly.

### RETRACT AMPLIFIER

When a voltage fault is sensed, or when $\overline{\text{RETRACT}}$ is asserted, the SSI 32H6510 enters retract mode. In this mode, it is assumed that no current is available from VP (VP may actually be at GND potential). Thus power for this mode comes from VBEMF, the rectified spindle back EMF voltage, and from VBYP1, a voltage generated from the external storage capacitor CBYP. The retract amplifier is powered by VBYP1. It senses the voltage at VRETRACT and raises VM1 to be equal to VRETRACT. The drain of the source follower is VBEMF.

### CONTROL CIRCUITRY

The control circuitry consists of voltage monitoring circuitry, a thermal overload circuit, and control logic. The inputs to the control circuitry are the external signals $\overline{\text{RETRACT}}$, VCHK, and SLEEP, along with internal signal from the thermal overload detector (visible externally on TSD). Table 1 describes the behavior of the part in response to these inputs.

**TABLE 1: IC Mode Selection**

| INPUT | | | | CHIP FUNCTION | | |
|---|---|---|---|---|---|---|
| SLEEP | $\overline{\text{RETRACT}}$ | VCHK>VBGAP | $\overline{\text{TSD}}$ | BRIDGE | RETRACT | $\overline{\text{SYSRST}}$ |
| X | X | 0 | 0 | Off | Off | 0 |
| X | X | 0 | 1 | Off | On | 0 |
| X | X | 1 | 0 | Off | Off | 1 |
| X | 0 | 1 | 1 | Off | On | 1 |
| 0 | 1 | 1 | 1 | On | Off | 1 |
| 1 | 1 | 1 | 1 | Off | Off | 1 |

## PIN DESCRIPTION

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| VP | Power | The positive power supply. The VP pins are thermally connected to the die and provide a low thermal resistance path to the circuit board. All VP pins should be shorted together. |
| GND | Power | The negative power supply. All GND pins should be shorted together. |
| SWON | Dig In | Turns on the switch between ERRM and SWIN. |
| SWIN | An In | One side of an analog switch connected to ERRM. |
| SOUT | An Out | The current sense amplifier output. SOUT is referenced to VREF. |
| ERR | An Out | The error amplifier output. ERR is used to provide compensation to the transconductance loop. ERR is referenced to VBGAP. |
| ERRM | An In | The error amplifier negative input. |
| VREF | An In | The reference voltage for the error amplifier and the current sense amplifier. |
| $\overline{\text{RETRACT}}$ | Dig In | When low, forces a retract. |
| THTEST | Dig In | Test input. |
| VCHK | An In | Comparator input for power supply monitoring. When VCHK is below VBGAP, an internal voltage fault is generated. |
| VBGAP | An Out | An internal voltage reference for use with the power supply monitor comparator. |
| IBR | An Out | A resistor is tied from this pin to ground to establish the bias current for internal circuitry. |
| SLEEP | Dig In | Turns off the output drivers. Does not override the retract function when a voltage fault occurs. Powers down all but the voltage monitor and retract circuitry. |
| $\overline{\text{TSD}}$ | O/C Out | Thermal Shut Down. When low, this open collector output indicates that the junction temperature has exceeded the recommended operating range and that the part is in thermal shutdown. |
| $\overline{\text{RCRST}}$ | O/C Out | This pin serves the dual purpose of providing power-on-reset and stretching short VFAULT pulses to a width suitable for the host microcontroller. An external RC network sets the minimum width of any $\overline{\text{SYSRST}}$ pulse. |
| $\overline{\text{SYSRST}}$ | O/C Out | When low, this open collector output indicates that an internal voltage fault has occurred. |
| VRETRACT | An In | The retract voltage. Supplied externally by a diode reference. |
| VBYP1 | An In | The bypassed power supply. An external capacitor is connected to this node to store charge for use by the retract circuitry. |
| VBYP2 | An In | The other side of the bypass capacitor is connected here. |
| VBEMF | An In | Rectified spindle back emf voltage. This input provides current to the internal retract power FET. |

## PIN DESCRIPTION (continued)

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| VM2 | An Out | One side of the voice coil motor. |
| VM1 | An Out | The other side of the voice coil motor and sense resistor combination. |
| SE1, SE2 | An In | The sense voltages around the sense resistor. |

## ELECTRICAL SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS

Operation of the part outside these limits may result in degradation or failure of the device.

| PARAMETER | RATING | UNITS |
|---|---|---|
| Power Supply, VP | 7 | V |
| Voltage on any pin | | |
| VBEMF, VBYP1, VBYP2, $\overline{\text{SYSRST}}$, $\overline{\text{RCRST}}$ | -0.3 to 16 | V |
| VM1, VM2, SE1, SE2 | -0.3 to 12 | V |
| All others | -0.3 to VP+.3 | V |
| Storage Temperature | -45 to 165 | °C |
| Solder Temperature (10 sec duration) | 260 | °C |
| Output Current - I(VM1), I(VM2) | 2 | Amp |
| Junction Temperature | 150 | °C |

### RECOMMENDED OPERATING CONDITIONS

The performance specifications for this part apply only when the operating environment is within this specified range.

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Power Supply, VP | | 4.75 | | 5.25 | V |
| Junction Temperature | | 0 | | 125 | °C |
| Output Current - I(VM1), I(VM2) | | | | 1.0 | Amp |
| VBEMF | | 1.0 | | 14 | V |
| VREF | | 0.5 | | VP-2 | V |
| RF | | 10 | | | kΩ |
| RC | | 10 | | | kΩ |
| RBIAS | | 21.5 | | 22.5 | kΩ |
| VBYP1 - Retract Mode | | 3 | | 14 | V |

**PERFORMANCE SPECIFICATIONS**

| DESCRIPTION | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|
| VP Supply Current: | | | | | |
| Normal operation, Imotor = 0 | | | | 15 | mA |
| Sleep mode | | | | 2 | mA |
| SOUT gain | | 3.9 | | 4.1 | V/V |
| SOUT input offset (SOUT = VREF) | | -3 | | 3 | mV |
| SOUT output swing | | 0.15 | | VP-1 | V |
| ERRM input offset (ERR = ERRM) | | -10 | | 10 | mV |
| ERR output swing | | 1.6 | | 3.25 | V |
| GAIN (VM1-VM2)/(ERR-VBGAP) | | 11 | | 13 | V/V |
| VBGAP | | 2.13 | | 2.37 | V |
| VCHK offset | | -15 | | 15 | mV |
| Retract offset | | | | | |
| VRETRACT = 0.5V | | -50 | | 50 | mV |
| VRETRACT input impedance | | 500 | | | kΩ |
| Output voltage drop: VP-\|VM1-VM2\| | | | | | |
| Imotor = ± 0.5A, Tj = 25°C | | | | 0.65 | V |
| Imotor = ± 0.1A, Tj = 25°C | | | | 0.15 | V |
| Thermal shutdown temperature | | 120 | | 140 | °C |
| Thermal shutdown hysteresis | | 3 | | 7 | °C |
| Crossover time | | | | | |
| Imotor = 10mA p 1000 Hz | | | | 45 | µs |
| Crossover distortion | | | | | |
| Imotor = 10mA p 1000 Hz | | | | 2 | %THD |
| Digital open collector output, sink current: | | | | | |
| $\overline{SYSRST}$, $\overline{RC\_RST}$, $\overline{TSD}$ | | | | | |
| Vol = 0.4V | | 1.6 | | | mA |
| SWIN on resistance | | | | 250 | Ω |

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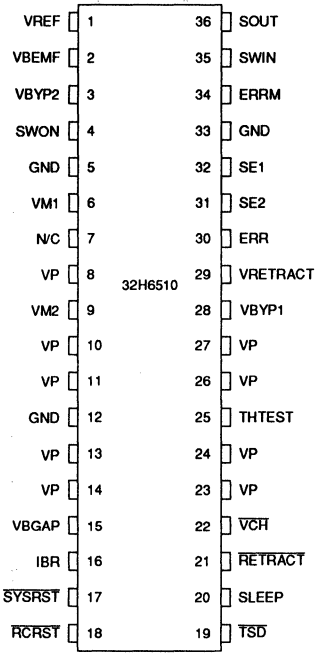
# SSI 32H6510
# 5V Servo Driver

## PACKAGE PIN DESIGNATIONS
(Top View)




**36-Lead SOM**

**Preliminary Data:** Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.



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# SSI 32H6520
## Embedded Servo Controller

**Preliminary Data**

December 1992

## DESCRIPTION

The 32H6520 Embedded Servo Controller is a CMOS monolithic integrated circuit housed in a 48-pin TQFP and operates on a single +5.0 volt supply. It provides one 10-bit A/D converter with 2.5 µs conversion time, and two 10-bit D/A converters with 2.5 µs digital delay as well as Motorola/Intel compatible bus interface (Motel) to commonly used microcontrollers such as 80C196 and 68HC11. In addition, it includes bus interface logic to support DSP-based, such as TMS320XX, digital servo applications.

## FEATURES

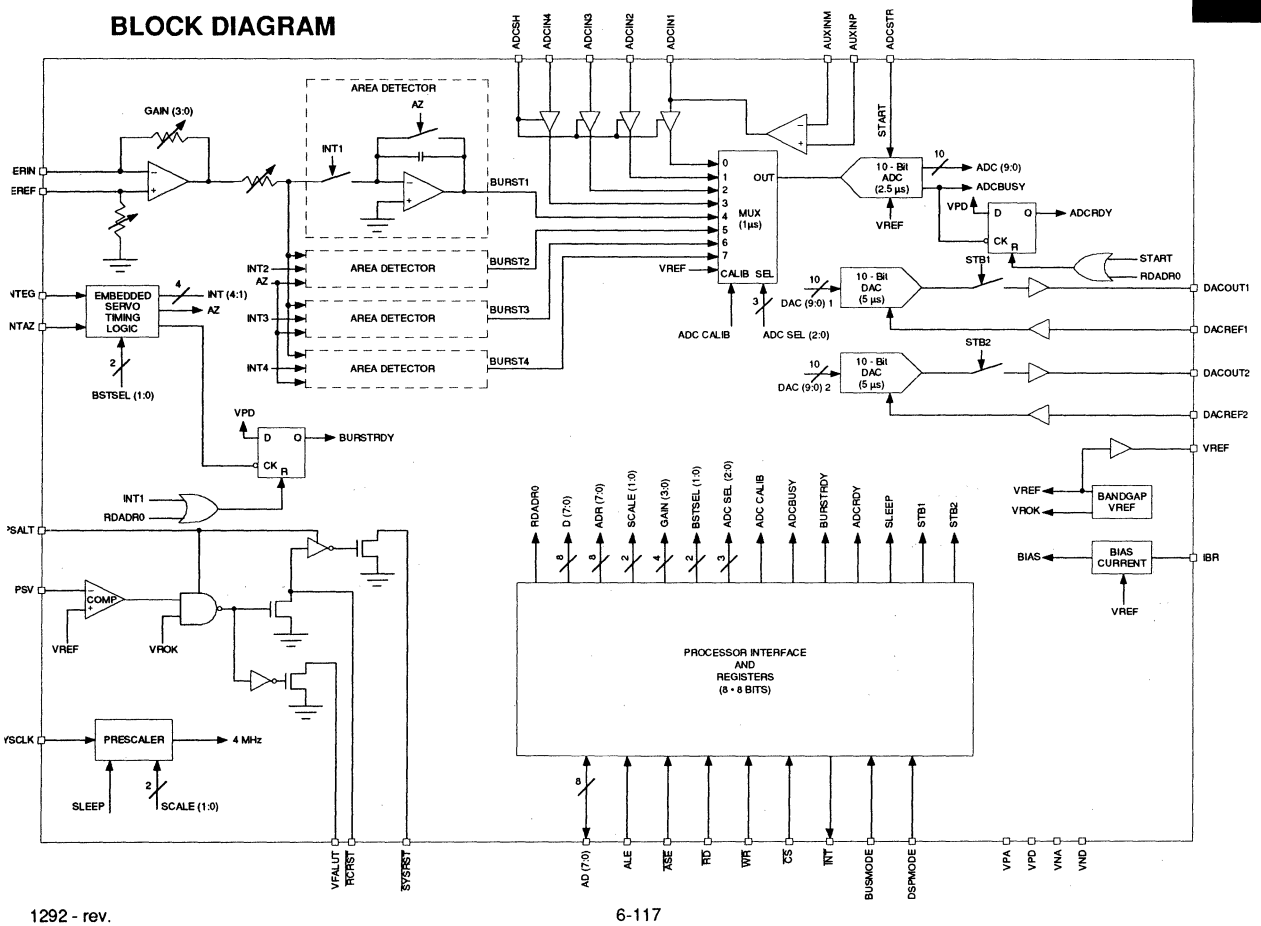
**Embedded Servo Burst Processor**

- Servo control for Winchester disk drives with embedded servo sectors
- For use in µP/DSP-based digital servo applications
- Pulse area detects and S/H circuits for up to four embedded servo bursts
- Programmable gain adjustment from -2.8 dB to 3.2 dB

(continued)



## BLOCK DIAGRAM



## FEATURES (continued)

**Data Acquisition and Microprocessor/DSP Bus Interface**

- Motel bus interface compatible with 80C196 and 68HC11
- Bus interface logic to support DSP-based digital servo applications
- Eight internal registers and address decoding
- Two 10-bit D/A converters with 2.5 µs digital delay
- One 8-channel 10-bit A/D converter with 2.5 µs conversion time

**General Functions**

- Voltage fault detection
- Low power CMOS design
- 48-pin TQFP

## FUNCTIONAL DESCRIPTION

The 32H6520 can be divided into four major sections: embedded servo burst processor, voltage fault detector/logic, data acquisition and microprocessor/DSP bus interface.

### EMBEDDED SERVO BURST PROCESSOR

The embedded servo burst processor extracts the head position error information from the embedded servo bursts using an area detection technique. The area detection technique provides improved noise immunity over peak detector. The embedded servo burst processor contains a differential/gain amplifier, four pulse area detectors and required timing logic. First, a full wave-rectified analog signal from a read data channel, such as SSI 32P4620, is provided at SERIN through an external resistor equal to Rint and a DC reference level for the full wave-rectified analog signal at SEREF through another external resistor equal to Rint. To accommodate a wide dynamic range of servo burst amplitudes and process variations of the integration capacitor Cint, the differential signal between SERIN and SEREF is scaled under µP control. The gain of the differential amplifier ranges from -2.8 dB to 3.2 dB in a step of 0.4 dB, as defined in the SERVO GAIN CONTROL register. The output of the differential/gain amplifier is then provided to four pulse area detectors whose output are proportional to the area above the DC reference level during time intervals defined by an external timing source through INTEG. Each area detector applies an on-chip capacitor Cint equal to 10 pF to integrate the incoming pulses during the integration interval and then hold the integrated voltage outputs thereafter. Note that the max ±20% tolerance of on-chip capacitors can be calibrated out by adjusting the gain of the preceding amplifier. Finally, the integrated voltage outputs at BURST1, BURST2, BURST3 and BURST4 are provided to a 10–bit A/D converter under µP control and will be discharged during a time interval defined by an external timing source through INTAZ. For proper operatons, the time interval defined by the INTAZ must be no less than 0.5 µs and be applied only once per servo frame preceding the integration pulses defined by the INTEG.

Limited timing logic is included to generate all the timing signals required for the embedded servo burst processor, per figure 1. These timing signals control the integration, sample/hold of the pulse area detectors. The number of embedded servo bursts supported by this circuit are two, three or four. The BSTSEL0 and BSTSEL1 bits in the SERVO CONTROL register configure the internal timing logic to generate a servo burst ready interrupt after the last servo burst is captured.

### VOLTAGE FAULT DETECTOR/LOGIC

The voltage fault detector is to monitor the power supply applied at PSV through an external resistor divider, which defines the trigger level for power supply failure. An open-drain output VFAULT is pulled HIGH by an external resistor when a power supply failure is sensed by the PSV comparator. The user-defined trigger level for voltage failure is applied at PSV. Another open-drain output, opposite logic polarity as the pin VFAULT and with an additional RC delay, is provided at $\overline{\text{SYSRST}}$. The amount of $\overline{\text{SYSRST}}$ delay is determined by an external RC connected to the pin, $\overline{\text{RCRST}}$.

### DATA ACQUISITION

The A/D converter is multiplexed to eight different analog inputs by programming the ADC SEL0, ADC SEL1, and ADC SEL2 bits in the ADC ADDRESS register by the µP. The eight analog inputs multiplexed to the A/D converter are four embedded servo processor outputs at BURST1, BURST2, BURST3 and BURST4 and four external analog inputs through four T/H amplifiers. These T/H amplifiers sample external

**DATA ACQUISITION** (continued)

analog inputs during the time interval defined by an external timing source applied at ADCSH. If the sampling of four external analog inputs is not necessarily synchronized, ADCSH must be tied to HIGH. The A/D conversions on these external analog inputs are always referenced to the internal voltage reference at 2.23 volts. An operational amplifier with uncommitted inputs is provided to implement a level shifting function for the external analog input applied to AUXINP. The output of the operational amplifier is tied to ADCIN1.

The A/D converter starts to acquire a new analog input whenever the conversion is completed. A minimum of 1 µs is required to acquire an analog input to the A/D converter. Actual conversion is started by reading the A/D MSB register or by an external timing source applied to ADCSTR. The A/D address lines ADC SEL0, ADC SEL1, and ADC SEL2 will be incremented by one after the A/D conversion is started. The automatic increment of the address lines is employed to eliminate repetitive write operations by the µP to the ADC ADDRESS register required for converting the consecutive analog inputs.

The A/D converter runs synchronously with the internal 4 MHz clock which is used for various circuits on the 32H6520 and divided down from the system clock SYSCLK by a prescaler. Therefore there would be a maximum of 0.25 µs of latency between a conversion request and the actual start of the conversion. The output is coded in 2's complement.

Similarly, the D/A converters run synchronously with the internal 2 MHz clock and the conversion is started by writing to the corresponding D/A input register. The output of the first D/A converter is referenced to an external analog input, DACREF1 and the output of the second D/A converter is referenced to an external analog input, DACREF2. In the "normal" mode when STBEN1 (STBEN2) bit in the ADC ADDRESS register is reset, the D/A output will be automatically applied to DACOUT1 (DACOUT2) during the conversion. In the "strobe" mode, the D/A output will be applied to DACOUT1 (DACOUT2) at the falling edge of $\overline{RD}$ for a read to the corresponding D/A MSB DATA register.

**MICROPROCESSOR/DSP BUS INTERFACE**

The 32H6520 is provided with Motorola/Intel compatible bus interface for a direct connection to popular microcontrollers such as 80C196 and 68HC11. It also contains logic to interface with TMS320XX for DSP-based servo applications. Bus control signals ALE, $\overline{RD}$, $\overline{WR}$ and BUSMODE are interpreted differently, as described in table 1, based upon the type of processors being used. When the 32H6520 is interfaced with TMS320XX, the pin DSPMODE must be tied to HIGH and the pin BUSMODE is redefined as XFER/$\overline{SEL}$. The pin BUSMODE must be tied to HIGH for an Intel bus interface and LOW for a Motorola bus interface. The $\overline{ASE}$ pin gates the ALE/AS input and can be used to shut off the ALE/AS to minimize noise on the chip when the µP interface is not active. The $\overline{CS}$ pin performs a similar function on the rest of the µP bus inputs. The timing diagrams for different processors are depicted in Figures 2, 3 and 4.

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**TABLE 1: Microprocessor/DSP Bus Interface**

| 32H6520 | Intel | Motorola | TMS320XX |
|---|---|---|---|
| DSPMODE | LOW | LOW | HIGH |
| BUSMODE | HIGH | LOW | XFER/$\overline{SEL}$ (PA0) |
| $\overline{CS}$ | $\overline{CS}$ | $\overline{CS}$ | $\overline{CS}$ (PA1) |
| ALE | ALE | AS | N/C |
| $\overline{RD}$ | $\overline{RD}$ | DS;E; or Clock Phase 2 | $\overline{REN}$ |
| $\overline{WR}$ | $\overline{WR}$ | R/$\overline{W}$ | $\overline{WE}$ |

## REGISTER DESCRIPTIONS

The 32H6520 contains eight 8-bit internal registers which provide control, option select and status monitoring. The registers are addressed with a 3-bit register address which is latched from inputs at AD0(LSB), AD1, and AD2(MSB) at the falling edge of ALE. The registers 0, 2, and 3 are read/write memory, and the registers 1, 4, 5, 6, and 7 are write only memory. The registers are summarized in Table 2.

**TABLE 2: Register Descriptions**

| ADDRESS | TYPE | REGISTER NAME |
|---|---|---|
| 0 | R/W | INTERRUPT MASK/STATUS |
| 1 | W | SERVO GAIN CONTROL & PRESCALER |
| 2 | R/W | ADC LSB DATA |
| 3 | R/W | ADC ADDRESS & MSB DATA |
| 4 | W | DAC1 LSB DATA |
| 5 | W | DAC1 MSB DATA |
| 6 | W | DAC2 LSB DATA |
| 7 | W | DAC2 MSB DATA |

### INTERRUPT MASK/STATUS REGISTER

Address: 0
Access: Read/Write
Reset: Bit 0, 1 only

Register contents when Written:

| BIT | NAME | DESCRIPTION |
|---|---|---|
| 0 | BURST INT | When set HIGH, interrupt is enabled on the embedded servo position bursts ready. |
| 1 | ADC INT | When set HIGH, interrupt is enabled on the completion of the A/D conversion. |
| 2 - 7 | | Unused. |

Register contents when Read:

| BIT | NAME | DESCRIPTION |
|---|---|---|
| 0 | BURSTRDY | Active high indicates that the embedded servo bursts are ready. |
| 1 | ADCRDY | Active high indicates that the A/D conversion is completed. |

Each interrupt event status will be reset after the µP reads this register. The interrupt control register determines if the event will actually cause a latched assertion of the µP signal $\overline{INT}$.

**SERVO GAIN CONTROL & PRESCALER REGISTER**

Address: 1
Access: Write
Reset: 00

| BIT | NAME | DESCRIPTION |
|---|---|---|
| 0<br>1 | SCALE0<br>SCALE1 | SYSCLK Prescaler. To accommodate different system clocks, the prescaler selects a proper divider to generate a fixed clock at 4 MHz per table below: |

| SCALE1 | SCALE0 | SYSCLK(MHz) | Divider |
|---|---|---|---|
| 0 | 0 | 16 | 4 |
| 0 | 1 | 12 | 3 |
| 1 | 0 | 8 | 2 |
| 1 | 1 | 4 | 1 |

| BIT | NAME | DESCRIPTION |
|---|---|---|
| 2<br>3<br>4<br>5 | GAIN0<br>GAIN1<br>GAIN2<br>GAIN3 | Servo Burst Amplitude Gain Select. These four bits define the gain setting for the differential/gain amplifier per table below: |

| GAIN3 | GAIN4 | GAIN3 | GAIN0 | Gain, dB |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | -2.8 |
| 0 | 0 | 0 | 1 | -2.4 |
| 0 | 0 | 1 | 0 | -2.0 |
| 0 | 0 | 1 | 1 | -1.6 |
| 0 | 1 | 0 | 0 | -1.2 |
| 0 | 1 | 0 | 1 | -0.8 |
| 0 | 1 | 1 | 0 | -0.4 |
| 0 | 1 | 1 | 1 | +0.0 |
| 1 | 0 | 0 | 0 | +0.4 |
| 1 | 0 | 0 | 1 | +0.8 |
| 1 | 0 | 1 | 0 | +1.2 |
| 1 | 0 | 1 | 1 | +1.6 |
| 1 | 1 | 0 | 0 | +2.0 |
| 1 | 1 | 0 | 1 | +2.4 |
| 1 | 1 | 1 | 0 | +2.8 |
| 1 | 1 | 1 | 1 | +3.2 |

| BIT | NAME | DESCRIPTION |
|---|---|---|
| 6<br>7 | BSTSEL0<br>BSTSEL1 | Burst Number Select. These two bits define the number of embedded servo bursts per sector. |

| BSTSEL1 | BSTSEL0 | # of Bursts |
|---|---|---|
| 0 | 0 | 2 |
| 0 | 1 | 3 |
| 1 | 0 | 4 |

### ADC LSB DATA REGISTER

Address: 2
Access: Read/Write
Reset: Bit 5, 6, 7 only

Register contents when Written:

| BIT | NAME | DESCRIPTION |
|---|---|---|
| 0 - 4 | | Unused. |
| 5 | SLEEP | Power-down Mode Enable. When set HIGH, the device is in the sleep mode where all analog circuitry are de-biased, the clock is disabled, and the bandgap voltage, reference voltage fault logic and processor interface stay active. |
| 6 | STBEN1 | When set HIGH, the analog output of the DAC1 is transferred and held onto DACOUT1. |
| 7 | STBEN2 | When set HIGH, the analog output of the DAC2 is transferred and held onto DACOUT2. |

Register contents when Read:

Description: After A/D conversion, the least significant 2 bits of the 10-bit digital word is stored into the register.

| | | |
|---|---|---|
| 0 - 5 | | Unused. Logic LOW is provided to these bits. |
| 6,7 | ADC0, ADC1 | The LSB 2 bits of the A/D converter output in 2's complement format. |

### ADC ADDRESS & MSB DATA REGISTER

Address: 3
Access: Read/Write
Reset: Bits 0, 1, 2, and 3 only

Description: When Written, the least significant 3 bits of the register define the analog input to the 10-bit A/D converter. After conversion, the most significant 8 bits of the 10-bit digital word is stored into the register.

Register contents when Written:

0 ADC SEL0
1 ADC SEL1
2 ADC SEL2

A/D Converter Input Select. These 3 bits define the analog input to the A/D converter per table below:

| BIT2 | BIT1 | BIT0 | ADC INPUT |
|---|---|---|---|
| 0 | 0 | 0 | ADCIN1 |
| 0 | 0 | 1 | ADCIN2 |
| 0 | 1 | 0 | ADCIN3 |
| 0 | 1 | 1 | ADCIN4 |
| 1 | 0 | 0 | BURST1 |
| 1 | 0 | 1 | BURST2 |
| 1 | 1 | 0 | BURST3 |
| 1 | 1 | 1 | BURST4 |

**ADC ADDRESS & MSB DATA REGISTER** (continued)

| BIT | NAME | DESCRIPTION |
|---|---|---|
| 3 | ADC CALIB | When set HIGH, VREF (2.23 volts) is applied to the A/D converter input. |
| 4 - 7 | | Unused. |

Register contents when Read:

| | | |
|---|---|---|
| 0 - 7 | ADC2 - 9 | The MSB 8 bits of the A/D converter output in 2's complement. ADC9 is the sign bit. |

**DAC1 LSB DATA REGISTER**

Address: 4
Access: Write
Reset: 00

| | | |
|---|---|---|
| 0 - 5 | | Unused. |
| 6, 7 | DAC0,<br>DAC1 | The LSB 2 bits to the DAC1 in 2's complement. |

**DAC1 MSB DATA REGISTER**

Address: 5
Access: Write
Reset: 00

| | | |
|---|---|---|
| 0 - 7 | DAC2 - 9 | The MSB 8 bits to the DAC1 in 2's complement, DAC9 is the sign bit. |

**DAC2 LSB DATA REGISTER**

Address: 6
Access: Write
Reset: 00

| | | |
|---|---|---|
| 0 - 5 | | Unused. |
| 6<br>7 | DAC0,<br>DAC1 | The LSB 2 bits to the DAC2 in 2's complement. |

**DAC2 MSB DATA REGISTER**

Address: 7
Access: Write
Reset: 00

| | | |
|---|---|---|
| 0 - 7 | DAC2 - 9 | The MSB 8 bits to the DAC2 in 2's complement. DAC9 is the sign bit. |

## PIN DESCRIPTION

### POWER SUPPLIES

| NAME | DESCRIPTION |
|---|---|
| VPA | Analog +5V supply. |
| VPD | Digital +5V supply. It must be shorted to analog +5V supply externally. |
| VNA | Analog ground. |
| VND | Digital ground. It must be shorted to analog ground externally. |
| PSALT | Alternate Voltage Supply to power the voltage fault logic during a voltage fault. This power supply should be taken from the system +5V supply through a Schottky diode and be connected to a capacitor, which is used to hold up PSALT briefly during a voltage fault. |

### EMBEDDED SERVO BURST PROCESSOR

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| SERIN | I | Servo Burst Input - Full-wave rectified analog signal generated from a read data channel. This input is to extract the position information from embedded servo bursts. |
| SEREF | I | Servo Burst Reference - A DC reference level for the full-wave rectified analog signal SERIN. |
| INTEG | I | Pulse Area Detector Enable - This TTL compatible input, when HIGH, activates the pulse area detectors. |
| INTAZ | I | Integrator Capacitor Reset - This TTL compatible input, when HIGH, discharges the holding capacitors, Cint. |

### VOLTAGE FAULT DETECTION

| | | |
|---|---|---|
| PSV | I | Fault Voltage Comparator Input - A voltage input for the low voltage comparator. This input should be connected to an external resistor divider. The resistor divider divides its corresponding supply voltage to a proper value which is comparable with the internal voltage reference at 2.23 volts. |
| VREF | O | VREF Output - A buffered voltage reference at 2.23 volts. |
| IBR | O | Pin for connection to an external resistor (from GND) to establish a reference current for bias currents required for analog circuits. |
| VFAULT | O | Voltage Fault Indication - An open-drain output which is pulled HIGH when a supply voltage fault is detected. |
| $\overline{\text{SYSRST}}$ | O | Reset Output - An open-drain output which is pulled LOW with an amount of delay determined by an external RC connected to the pin RCRST when a supply voltage fault is detected. |
| $\overline{\text{RCRST}}$ | O | Pin for connection to an external RC to implement the delay of active LOW $\overline{\text{SYSRST}}$. |

**MICROPROCESSOR/DSP BUS INTERFACE**

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| ALE | I | Address Latch Enable - Falling edge latches the register address from the AD0 - AD7 address/data bus. |
| $\overline{ASE}$ | I | Address Strobe Enable - When set LOW, this input enables ALE input to the device. |
| $\overline{CS}$ | I | Chip Select - Active LOW signal enables the device to respond to µP read or write. |
| $\overline{WR}$ | I | Write Strobe - In Intel µP applications, active LOW signal causes the data on the address/data bus to be written to the addressed register if $\overline{CS}$ is also active. |
| $\overline{RD}$ | I | Read Strobe - In Intel µP applications, active LOW signal causes the contents of the addressed register to be placed on the address/data bus if $\overline{CS}$ is also active. |
| AD0 - AD7 | I/O | Address/Data Bus - 8-bit bus which carries register address information and bidirectional data. These pins are in the high impedance state when not used. |
| BUSMODE | I | Mode Select - When active HIGH, Intel bus interface is selected. Otherwise, Motorola bus interface is selected. For DSP interface, when DSPMODE set HIGH, this input is redefined as XFER/$\overline{SEL}$. |
| $\overline{INT}$ | O | Interrupt Strobe - An open-drain output which signals the µP to respond to the device. It is released when all pending interrupts have been serviced by the µP. |
| DSPMODE | I | DSP Mode Select - When active HIGH, DSP bus interface is selected. |
| SYSCLK | I | System Clock Input - A TTL compatible input for the system clock which is divided down with a prescaler to generate internal timing signals. |

**DATA ACQUISITION**

| | | |
|---|---|---|
| DACOUT1 | O | DAC1 Output - A 10-bit D/A output which converts a digital word from the µP into an analog signal. |
| DACREF1 | I | DAC1 Output Reference - An external analog input to be provided to DAC1 as a reference voltage for DACOUT1. |
| DACOUT2 | O | DAC2 Output - A 10-bit D/A output which converts a digital word from the µP into an analog signal. |
| DACREF2 | I | DAC2 Output Reference - An external analog input to be provided to DAC2 as a reference voltage for DACOUT2. |
| ADCIN1<br>ADCIN2<br>ADCIN3<br>ADCIN4 | I | External A/D inputs. |
| ADCSH | I | A/D Analog Sampling Input Strobe - A TTL compatible control signal. During active HIGH, four track/hold amplifiers prior to the A/D converter will sample external A/D analog inputs. |

**DATA ACQUISITION** (continued)

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| ADCSTR | I | A/D Conversion Start Strobe - A TTL compatible control signal whose rising edge triggers the start of the A/D conversion. |
| AUXINP | I | Level Shifter Noninverting Input - Noninverting input to the level-shifting amplifier. |
| AUXINM | I | Level Shifter Inverting Input - Inverting input to the level-shifting amplifier. |

## ELECTRICAL SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS

Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device or affect device reliability.

| SYMBOL | PARAMETER | RATING |
|---|---|---|
| VDD | Supply voltage applied at VPA, VPD | -0.3 to 7.0V |
| GND | Signal ground applied at VNA, VND | 0.0V |
| PSALT | Supply voltage applied at PSALT | -0.3 to 7.0V |
| VIND | Digital input voltages | -0.3 to VDD+0.3V |
| VINA | Analog input voltages | -0.3 to VDD+0.3V |
| Tstg | Storage temperature | -65 to 150 °C |
| TI | Lead temperature (10 seconds) | 300 °C |

### RECOMMENDED OPERATING CONDITIONS

The recommended operating conditions for the device are indicated in the table below. Performance specifications do not apply where the device is operating outside these limits.

| SYMBOL | PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| VDD | Supply voltage applied at VPA, VPD | | 4.5 | | 5.25 | V |
| GND | Signal ground applied at VNA, VND | | 0.0 | | 0.0 | V |
| PSALT | Supply voltage applied at PSALT | | 3.0 | | 6.0 | V |
| TA | Ambient temperature | | 0.0 | | 70.0 | °C |
| Fc | System clock (16MHz, Max) | | | | ±0.1 | % |
| Tc | System clock duty cycle | | 40 | | 60 | % |

**RECOMMENDED OPERATING CONDITIONS** (continued)

| SYMBOL | PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| CLOAD | Capacitive load on digital outputs | | - | | 100 | pF |
| RBIAS | Bias resistor (22.6 kΩ) | | | | ±1 | % |

**DC CHARACTERISTICS**

The following electrical specifications apply to the digital input and output signals over the recommended operating range unless otherwise noted. Positive current is defined as entering the device. Minimum and maximum are based upon the magnitude of the number.

| | | | | | | |
|---|---|---|---|---|---|---|
| IDD | Supply current<br>Normal mode<br>Sleep mode | VDD = 5.25V | <br>-<br>- | | <br>25<br>2 | <br>mA<br>mA |
| Voh | Output logic "1" voltage | Ioh = -0.4mA, VDD = 4.5V | 2.4 | | - | V |
| Vol | Output logic "0" voltage | Iol = 1.6mA, VDD = 4.5V | - | | 0.4 | V |
| Vih | Input logic "1" voltage | VDD = 4.5V | 2.0 | | - | V |
| Vil | Input logic "0" voltage | VDD = 4.5V | - | | 0.8 | V |
| Iih | Input logic "1" current | Vih = 5.25V, VDD = 5.25V | - | | 1 | µA |
| Iil | Input logic "0" voltage | Vil = 0.0, VDD = 5.25V | - | | -1 | µA |
| Cin | Input capacitance | | - | | 10 | pF |

## FUNCTIONAL CHARACTERISTICS

**EMBEDDED SERVO BURST AMPLITUDE PROCESSOR**

| | | | | | |
|---|---|---|---|---|---|
| SERIN with respect to GND | | 1.0 | - | VDD | V |
| SEREF with respect to GND | | 1.0 | | 3.0 | V |
| SERIN input voltage | Servo gain = -2.8 dB | 0.0 | - | 1.5 | Vp |
| swing with respect to SEREF | Servo gain = 0 dB | 0.0 | - | 1.0 | Vp |
| Servo burst frequency | | 1.0 | - | 5.0 | MHz |
| Input impedance at | Servo gain = -2.8 dB | 15 | 20 | 25 | kΩ |
| SERIN, SEREF | Servo gain = 0 dB | 18 | 24 | 30 | kΩ |
| Cin = 2 pF nominal | Servo gain = 3.2 dB | 21 | 28 | 35 | kΩ |
| $C_{int}$ integration time, $t_{INT}$ | Integrates to within 1% of | 1.0 | | | µs |
| $C_{int}$ discharge time, $t_{DISCH}$ | | 0.5 | | | µs |
| Burst integration timing window separation, $t_{NON}$ | | 0.5 | | | µs |
| Servo burst ready, $t_{RDY}$ | | 0.1 | | | µs |

**EMBEDDED SERVO BURST AMPLITUDE PROCESSOR** (continued)

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Servo channel ouput when SERIN shorted with SEREF | SEREF = 2V<br>$R_{int}$ = 63 kΩ | 1.40 | - | 1.75 | V |
| Servo channel gain step size | Guaranteed Monotonic | 1.0 | 1.05 | 1.1 | V/V |
| Servo channel slope deviation | SERIN from 0.2 $V_p$ to 0.8 $V_p$<br>$R_{int}$ = 63 kΩ | - | - | ±6 | % |

**VOLTAGE REFERENCE AND VOLTAGE FAULT CIRCUIT**

| | | | | | |
|---|---|---|---|---|---|
| VPA voltage for $\overline{SYSRST}$ & RCRST in operation | | 2 | - | 5.25 | V |
| On resistance at RCRST | | - | - | 100 | Ω |
| RCRST input threshold | PSALT = 3V | 0.8 | - | 1.6 | V |
| IBR voltage with respect to VREF | | | - | ±40 | mV |
| VREF voltage | No load | 2.16 | 2.23 | 2.30 | V |
| Allowable load at VREF | | 10 | | - | kΩ |
| | | - | | 100 | pF |
| PSV comparator offset | | | - | ±15 | mV |

**A/D INPUT UNCOMMITTED OPERATIONAL AMPLIFIER**

| | | | | | |
|---|---|---|---|---|---|
| AUXINP Input Voltage | With respect to GND | 1.25 | - | 2.5 | V |
| Unit-gain bandwidth | | 2 | - | - | MHz |
| Input-referred D.C. offset | | - | - | ±10 | mV |
| Allowable load at ADCIN | | 5.0 | - | - | kΩ |
| | | | | 40 | pF |

**DATA ACQUISITION**

**A/D Converter**

| | | | | | |
|---|---|---|---|---|---|
| ADCIN full-scale voltage with respect to VREF | | - | ± (VREF/2) | - | V |
| Resolution | | - | 10 | - | Bits |
| Acquisition time | | - | 1.0 | | µs |
| Conversion time | | - | 2.5 | | µs |
| LSB voltage | | - | VREF/ 1024 | - | V |
| Differential nonlinearity | Guaranteed Monotonic | - | - | ±1.0 | LSB |

### D/A Converter

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| DAC full-scale voltage with respect to DACREF | | - | ±(VREF/2) | - | V |
| Resolution | | - | 10 | - | Bits |
| Digital delay | | - | 2.5 | - | µs |
| Output settling time | To within ±0.5 LSB | - | 5.0 | - | µs |
| LSB voltage | | - | VREF/ 1024 | - | V |
| Differential nonlinearity | Guaranteed Monotonic | - | - | ±1.0 | LSB |
| DACREF1, DACREF2 | | 1.5 | | 2.3 | V |
| DACOUT1, DACOUT2 | | 0.3 | | 3.5 | V |



### Intel Microprocessor Interface Timing

The following timing specifications are applied when an Intel bus interface is selected by pulling the BUSMODE pin to logical HIGH and the DSPMODE pin to logical LOW. Timing measurements are made at 50% VDD with 100 pF load capacitances for all pins, unless otherwise noted.

| SYMBOL | PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{ALPW}$ | Pulse width, ALE HIGH | | 45 | | - | ns |
| $t_{AS}$ | Muxed address valid time to ALE fall | | 7.5 | | - | ns |
| $t_{AH}$ | Muxed address hold time after ALE fall | | 20 | | - | ns |
| $t_{DDR}$ | Read data delay time from $\overline{RD}$ fall | | - | | 60 | ns |
| $t_{DHR}$ | Read data hold time after $\overline{RD}$ rise | | 0 | | 50 | ns |
| $t_{RDPW}$ | Pulse width, $\overline{RD}$ LOW | | 75 | | - | ns |
| $t_{DSW}$ | Write data setup time to $\overline{WR}$ rise | | 40 | | | ns |
| $t_{DHW}$ | Write data hold time after $\overline{WR}$ rise | | 10 | | - | ns |
| $t_{WRPW}$ | Pulse width, $\overline{WR}$ LOW | | 50 | | - | ns |
| $t_{RWD}$ | $\overline{RD}$ or $\overline{WR}$ delay time from ALE fall | | 25 | | - | ns |
| $t_{CSS}$ | $\overline{CS}$ setup time prior to ALE fall | | 0 | | - | ns |
| $t_{CSH}$ | $\overline{CS}$ hold time after $\overline{RD}$ or $\overline{WR}$ rise | | 0 | | - | ns |
| $t_{ASES}$ | $\overline{ASE}$ setup time prior to ALE fall | | 45 | | - | ns |
| $t_{ASEH}$ | $\overline{ASE}$ hold time to ALE fall | | 0 | | - | ns |

### Motorola Microprocessor Interface Timing

The following timing specifications are applied when a Motorola bus interface is selected by pulling the BUSMODE pin to logical LOW and the DSPMODE pin to logical LOW. Timing measurements are made at 50% VDD with 100 pF load capacitances for all pins, unless otherwise noted.

| SYMBOL | PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{ASPW}$ | Pulse width, AS HIGH | | 45 | | - | ns |
| $t_{AS}$ | Muxed address valid time to AS fall | | 7.5 | | - | ns |
| $t_{AH}$ | Muxed address hold time after AS fall | | 20 | | - | ns |
| $t_{DDR}$ | Read data delay time from DS rise | | - | | 100 | ns |
| $t_{DHR}$ | Read data hold time after DS fall | | 0 | | 50 | ns |
| $t_{DSPWR}$ | Pulse width, DS HIGH during READ | | 100 | | - | ns |
| $t_{DSW}$ | Write data setup time prior to DS fall | | 60 | | - | ns |
| $t_{DHW}$ | Write data hold time after DS fall | | 10 | | - | ns |
| $t_{DSPWW}$ | Pulse width, DS HIGH during WRITE | | 100 | | - | ns |
| $t_{ASDS}$ | DS delay time from AS fall | | 25 | | - | ns |
| $t_{ASRW}$ | R/$\overline{W}$ delay time from AS fall during WRITE | | 25 | | - | ns |
| $t_{RWH}$ | R/$\overline{W}$ hold time after DS fall during WRITE | | 0 | | - | ns |
| $t_{CSS}$ | $\overline{CS}$ setup time prior to AS fall | | 0 | | - | ns |
| $t_{CSH}$ | $\overline{CS}$ hold time after DS fall | | 0 | | - | ns |
| $t_{ASES}$ | $\overline{ASE}$ setup time prior to AS fall | | 45 | | - | ns |
| $t_{ASEH}$ | $\overline{ASE}$ hold time after AS fall | | 0 | | - | ns |

### DSP Interface Timing

The following timing specifications are applied when a DSP bus interface is selected by pulling the DSPMODE pin to logical HIGH. Timing measurements are made at 50% VDD with 100 pF load capacitances for all pins, unless otherwise noted.

| SYMBOL | PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{ALPW}$ | Pulse width, XFER/$\overline{SEL}$ LOW | | 75 | | - | ns |
| $t_{ALHW}$ | XFER/$\overline{SEL}$ hold time after $\overline{WR}$ rise | | 0 | | - | ns |
| $t_{DDR}$ | Read data delay time from $\overline{REN}$ fall | | - | | 60 | ns |
| $t_{DHR}$ | Read data hold time after $\overline{REN}$ rise | | 0 | | 50 | ns |
| $t_{RDPW}$ | Pulse width $\overline{REN}$ LOW | | 50 | | - | ns |
| $t_{DSW}$ | Write data setup time prior to $\overline{WR}$ rise | | 40 | | - | ns |
| $t_{DHW}$ | Write data hold time after $\overline{WR}$ rise | | 10 | | - | ns |
| $t_{WRPW}$ | Pulse width, $\overline{WR}$ LOW | | 50 | | - | ns |
| $t_{CSSW}$ | $\overline{CS}$ setup time prior to $\overline{WR}$ | | 25 | | - | ns |
| $t_{CSSR}$ | $\overline{CS}$ setup time prior to $\overline{REN}$ | | 25 | | - | ns |
| $t_{CSH}$ | $\overline{CS}$ hold time after $\overline{REN}$ or $\overline{WR}$ rise | | 0 | | - | ns |

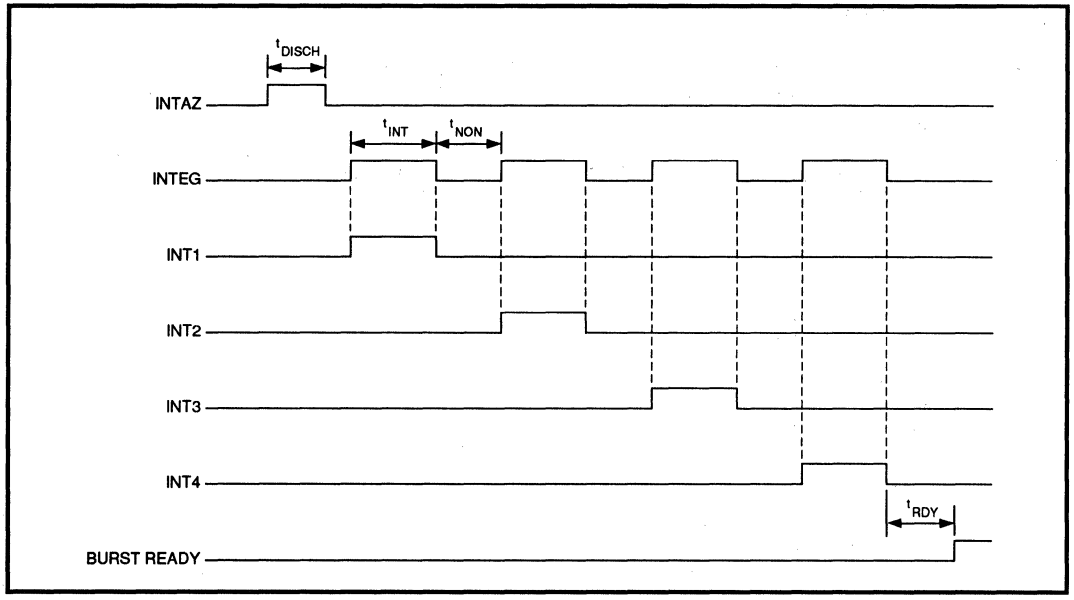



**FIGURE 1: Embedded Servo Burst Processor Timing Diagram**

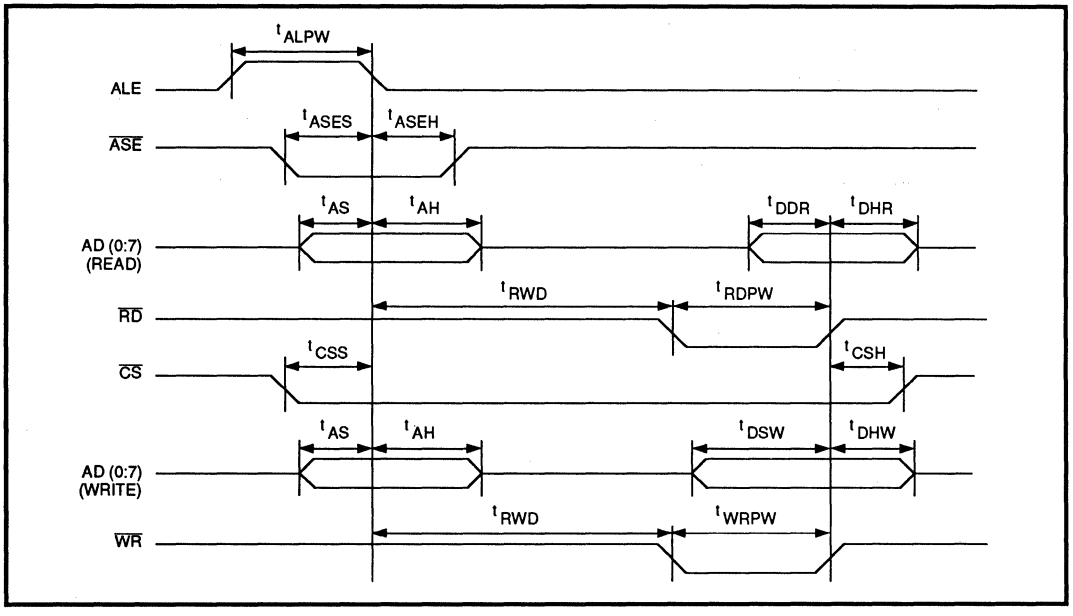



**FIGURE 2: Intel Microprocessor Bus Interface Timing Diagram**

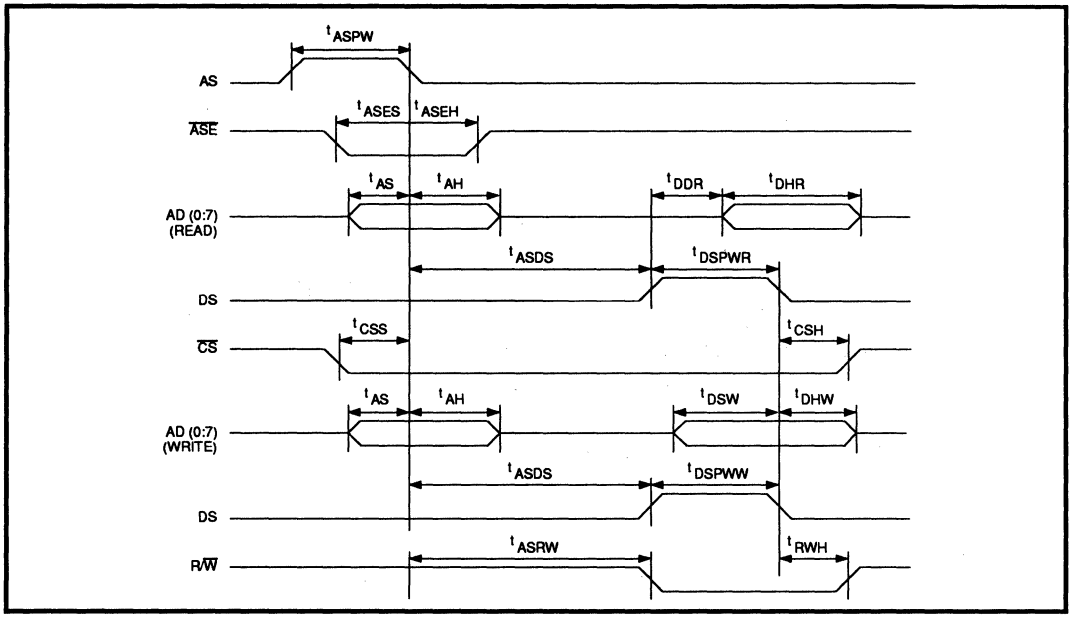



**FIGURE 3: Motorola Microprocessor Bus Interface Timing Diagram**

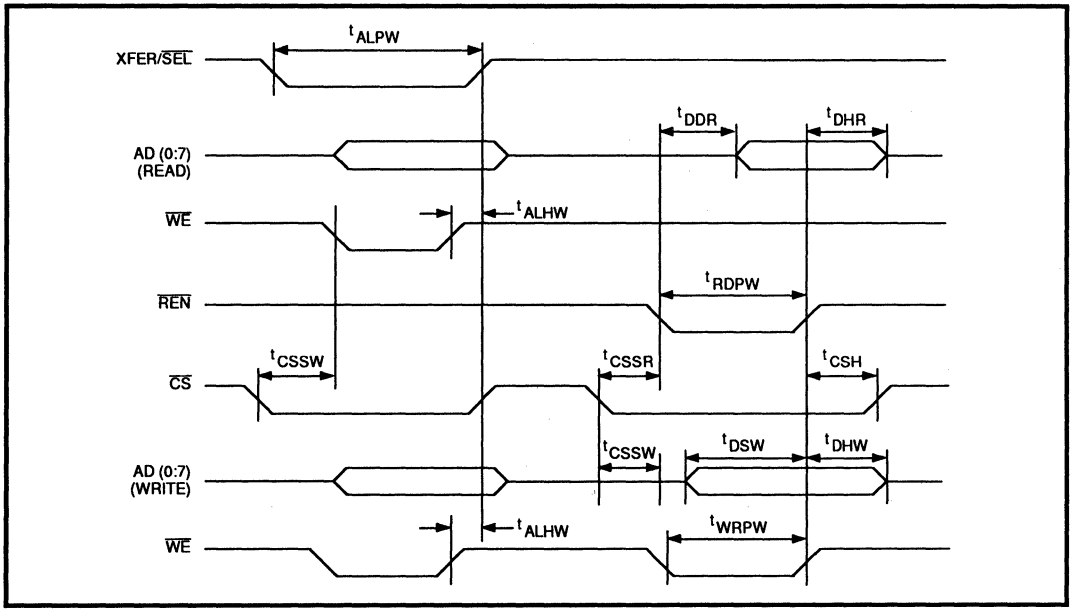


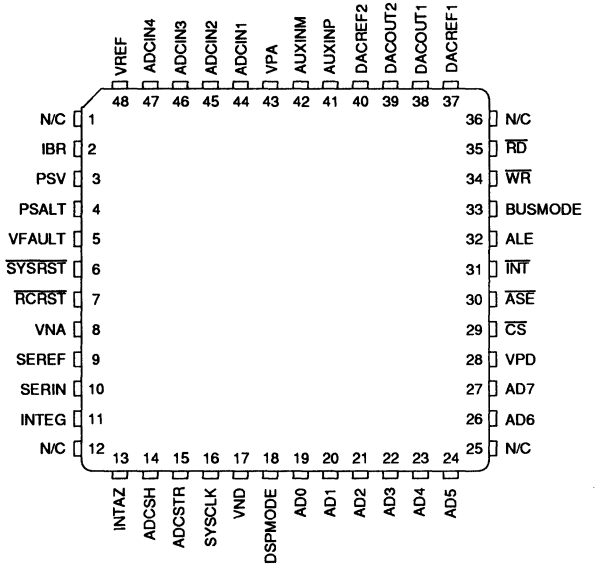

**FIGURE 4: TMS320XX Bus Interface Timing Diagram**

| 0: INTERRUPT MASK/STATUS | | | 1: SERVO GAIN CONTROL & PRESCALER | | | 2: ADC LSB DATA | | | 3: ADC ADDRESS & MSB DATA | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| # | WRITE | READ | # | WRITE | READ | # | WRITE | READ | # | WRITE | READ |
| 0 | BURST INT | BURSTRDY | 0 | SCALE0 | | 0 | | '0' | 0 | ADC SEL0 | ADC2 |
| 1 | ADC INT | ADCRDY | 1 | SCALE1 | | 1 | | '0' | 1 | ADC SEL1 | ADC3 |
| 2 | | | 2 | GAIN0 | | 2 | | '0' | 2 | ADC SEL2 | ADC4 |
| 3 | | | 3 | GAIN1 | | 3 | | '0' | 3 | ADC CALIB | ADC5 |
| 4 | | | 4 | GAIN2 | | 4 | | '0' | 4 | | ADC6 |
| 5 | | | 5 | GAIN3 | | 5 | SLEEP | '0' | 5 | | ADC7 |
| 6 | | | 6 | BSTSEL0 | | 6 | STBEN1 | ADC0 | 6 | | ADC8 |
| 7 | | | 7 | BSTSEL1 | | 7 | STBEN2 | ADC1 | 7 | | ADC9 |
| 4: DAC1 LSB DATA | | | 5: DAC1 MSB DATA | | | 6: DAC2 LSB DATA | | | 7: DAC2 MSB DATA | | |
| # | WRITE | READ | # | WRITE | READ | # | WRITE | READ | # | WRITE | READ |
| 0 | | | 0 | DAC2 1 | | 0 | | | 0 | DAC2 2 | |
| 1 | | | 1 | DAC3 1 | | 1 | | | 1 | DAC3 2 | |
| 2 | | | 2 | DAC4 1 | | 2 | | | 2 | DAC4 2 | |
| 3 | | | 3 | DAC5 1 | | 3 | | | 3 | DAC5 2 | |
| 4 | | | 4 | DAC6 1 | | 4 | | | 4 | DAC6 2 | |
| 5 | | | 5 | DAC7 1 | | 5 | | | 5 | DAC7 2 | |
| 6 | DAC0 1 | | 6 | DAC8 1 | | 6 | DAC0 2 | | 6 | DAC8 2 | |
| 7 | DAC1 1 | | 7 | DAC9 1 | | 7 | DAC1 2 | | 7 | DAC9 2 | |

**FIGURE 5: SSI 32H6520 Embedded Servo Processor Register Map**

## PACKAGE PIN DESIGNATIONS

(Top View)




**48-pin TQFP**

CAUTION: Use handling procedures necessary for a static sensitive component.

## ORDERING INFORMATION

| PART DESCRIPTION | ORDER NUMBER | PACKAGE MARK |
|---|---|---|
| SSI 32H6520 48-pin TQFP | 32H6520-CGT | 32H6520-CGT |

**Preliminary Data:** Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.



Silicon Systems, Inc. 14351 Myford Road, Tustin, CA 92680, (714) 573-6000, FAX (714) 573-6914

**Notes:**

silicon systems®
A TDK Group Company

# SSI 32H6810/6810A
# 5V Servo & Motor Speed Drivers

**Advance Information**

January 1993

## DESCRIPTION

The 32H6810/6810A combines the head positioning and spindle motor electronics with internal power FETs. It also provides voltage fault logic and over-temperature protection.

The positioner section serves as a transconductance amplifier by driving 4 internal FETs in an H-bridge configuration and performs motor current sensing. Class B operation is guaranteed by crossover protection circuitry, which ensures that only one FET in each leg of the H-bridge is active. It also offers over-temperature protection by disabling the output FETs. In addition, automatic head retraction may be initiated by a low voltage condition or upon external command.

(continued)

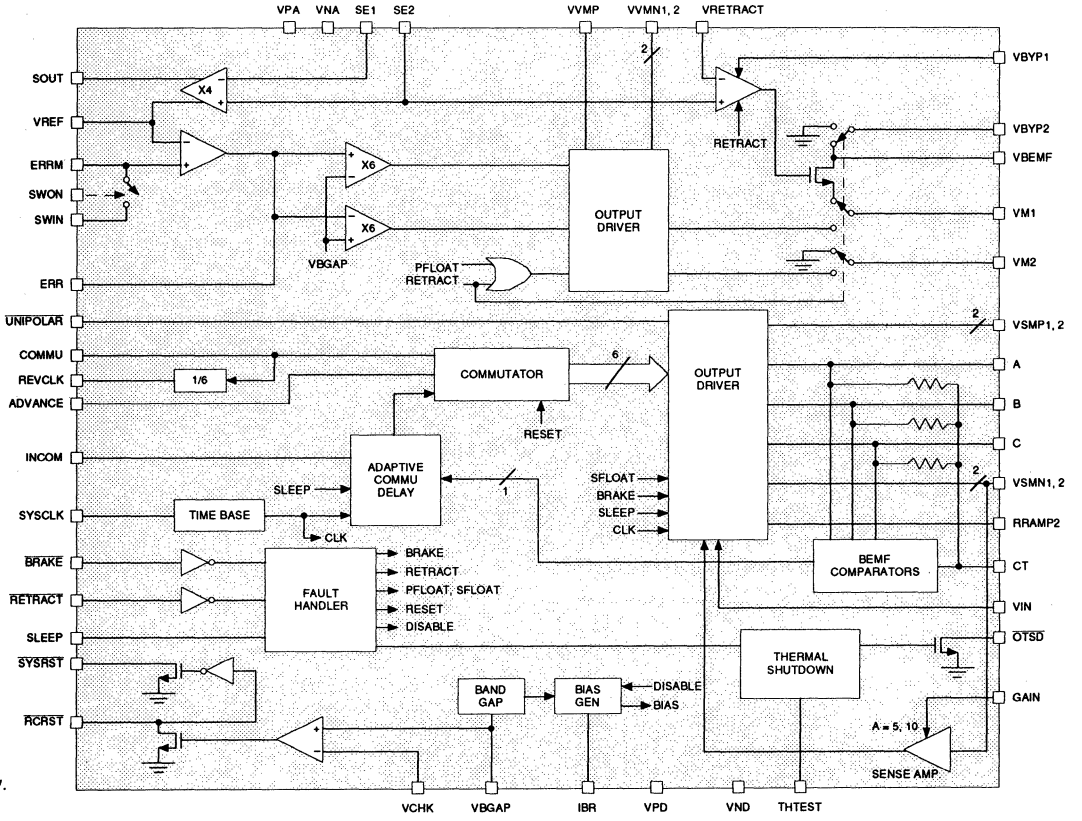
## FEATURES

- **48-lead TQFP package**
- **NMOS output stage, no blocking diode required**
- **Internal 1.0A power devices**
- **Total spindle on resistance less than**
  **2.5Ω: 32H6810**
  **1.7Ω: 32H6810A**
- **No deadband, low distortion, class B servo driver output**
- **Thermal overload protection**

(continued)

6

## BLOCK DIAGRAM



# SSI 32H6810/6810A
# 5V Servo & Motor Speed Drivers

## FEATURES (continued)

- **Builit-in retract circuitry**
- **Multiple Brake/Coast/Retract modes**
- **Power fault detect & retract circuitry**
- **Optimum commutation without external components or Hall sensors**
- **Reduced DV/DT on commutation – no snubber networks required**
- **Both Unipolar and Bipolar operating modes**

## DESCRIPTION (continued)

The (Spindle) Motor Commutator in conjunction with external components, provides the motor driving capability for starting, accelerating, and rotational speed regulation for brushless DC motors without the need for Hall sensors. Control is accomplished via five pins (plus 2 optional pins INCOM & $\overline{\text{UNIPOLAR}}$) and operation is monitored via three pins (plus optional pin REVCLK). The speed regulation control loop is completed with a microprocessor or signal processor external to the SSI 32H6810/6810A.

Motor speed control may be accomplished by measuring the period of the output signal COMMU. Motor armature position is determined by monitoring the coil voltage of the winding that is not presently being driven by the drivers. The back-emf from the coil in conjunction with the state of the output drivers, indicates armature position.

The back emf is compared to a reference (CT) and initiates commutation "events" when the appropriate comparison is made. (Commutation is the sequential switching of drive current to the motor windings.) Because the back-emf comparison event occurs prior to the time when optimum commutation should occur, it is preferred to delay commutation by a predetermined time after the comparison. The commutation delay is provided by circuitry which measures the interval between comparison events and delays commutation by a time equal to 3/7 of the prior measured interval. The circuit is adaptive and will provide the optimum delay for a wide range of motor speeds (-80% to +50% of nominal). Since the commutation of motor coils typically causes transients, the commutation delay circuit also provides a noise blanking function which prevents response to back-emf comparison events for a period of time equal to 4/7 of the interval (between events) after the comparison event. The commutation states are given in Table 1.

Input pin VIN is the non-inverting input of a linear transconductance amplifier which uses the lower driver transistor that is presently active per the commutation state as the power driver element. An external resistor Rsense is used to sense the current in the drive transistor source VSMN (and hence the motor coil current). The voltage across the sense resistor is amplified by a gain stage (Av = 5) and fed to the inverting input of the transconductance output stage.

The output pins A, B, and C are intended to drive motor coils directly. The output drivers operate to reduce switching noise transients by limiting dv/dt during commutation. Each output consists of two n-channel MOSFET drivers, one for pull-up to VSMP and one for pull-down to VSMN. The pull-up looks like a switch (1.5 Ω maximum) with voltage rise and fall times of about 25 microseconds. The pull-down transistor is part of the transconductance amplifier which converts VIN into motor current (Imotor = VIN/(Rsense • 5) ). When the pull-down output is commutating to the "off" state, dv/dt is controlled such that dv/dt is approximately 1.5E10/Rramp volts per second.

Motor starting is accomplished by a companion microprocessor utilizing ADVANCE, SLEEP, $\overline{\text{BRAKE}}$ and COMMU. The microprocessor can control SLEEP and $\overline{\text{BRAKE}}$ to initialize the commutation counter and then increment the counter with ADVANCE. Reset with SLEEP = low and $\overline{\text{BRAKE}}$ = low then enable with $\overline{\text{BRAKE}}$ = high (power-up condition and preparation to begin a starting sequence), the commutation state will be state 0 per Table 1, but lower driver output B remains inactive to prevent current flow through the motor (out of A which is "high"). On the first ADVANCE set high, commutation state 1 is selected and the drivers are per Table 1. ADVANCE at logic high excludes internal commutations. COMMU provides feedback to the microprocessor on motor activity.

Seven operating conditions are selected via $\overline{\text{BRAKE}}$, SLEEP and $\overline{\text{RETRACT}}$ (when VPA is present) as indicated by Table 2. If VPA is not present (VCHK < VBGAP), power for the braking circuitry during retract and spin-down is provided by the charge stored on an external capacitor on pin VBYP1, power for the retract circuitry is provided by the back emf voltage and the retract circuitry itself is driven by charge stored on the capacitor between VBYP1 and VBYP2.

| STATE | COMMU | Pull-Downs A | B | C | Pull-Ups A | B | C |
|---|---|---|---|---|---|---|---|
| 0, (Reset state) | 0 | off | on (1) | off | on | off | off |
| 1 | 1 | off | off | on | on | off | off |
| 2 | 0 | off | off | on | off | on | off |
| 3 | 1 | on | off | off | off | on | off |
| 4 | 0 | on | off | off | off | off | on |
| 5 | 1 | off | on | off | off | off | on |
| (1) B is off in reset state, see text. | | | | | | | |

**TABLE 1: Commutation States**

| VCHK>VBGAP | SLEEP | $\overline{\text{BRAKE}}$ | $\overline{\text{RETRACT}}$ | CONDITION | ANALOG | POSITIONER | A, B, C |
|---|---|---|---|---|---|---|---|
| 0 | X | 1 | X | Power Fault | On | Retract | Float |
| 0 | X | 0 | X | Power Fault | On | Retract | Low Z to GND |
| 1 | 1 | 1 | 1 | Sleep | Off | Float | Float |
| 1 | 1 | 0 | 1 | Sleep/Brake | Off | Float | Low Z to GND |
| 1 | 1 | 0 | 0 | Sleep/Retract | Off | Retract | Low Z to GND |
| 1 | 1 | 1 | 0 | Sleep/Retract | Off | Retract | Float |
| 1 | 0 | 0 | X | Brake/Retract | On | Retract | Low Z to GND |
| 1 | 0 | 1 | 0 | Retract (Spindle Run) | On | Retract | Active |
| 1 | 0 | 1 | 1 | Run | On | Active | Active |
| X | X | X | X | Thermal Shutdown | On | Float | Float |

**TABLE 2: Operating Mode Control**

NOTES:
1. $\overline{\text{BRAKE}}$ internally linked to force retract.
2. Voltage fault circuit is never turned off.
3. Counter is reset when sleep input is high.

The circuit also provides an over temperature detection function. If the die temperature exceeds 135°C (approximately), $\overline{\text{OTSD}}$ is asserted low and all output drivers are turned off. The drivers will become operative after the temperature is reduced and ADVANCE is asserted high.

## PIN DESCRIPTION

### POWER SUPPLIES

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| VPA | I | Supply: Analog positive power supply. |
| VNA | I | Ground: Analog ground. |
| VPD | I | Supply: Digital positive power supply. |
| VND | I | Ground: Digital ground. VND is circuitry ground and also the low side input to the current SENSE amplifier and thus care should be taken to see that VND and the low side of the external Rsense resistor are at the same potential. |
| VVMP | I | Supply: Positve supply for voice coil motor. |
| VVMN1, VVMN2 | I | Supply: Negative supply for voice coil motor. |

### POSITIONER

| | | |
|---|---|---|
| SWON | I | Turns on the switch between ERRM and SWIN. |
| SWIN | I | Analog switch, the other side of the switch is connected to ERRM. |
| SOUT | O | The current sense amplifier output. SOUT is referenced to VREF. |
| ERR | O | The error amplifier output. ERR is used to provide compensation to the transconductance loop. ERR is referenced to VBGAP. |
| ERRM | I | The error amplifier negative input. |
| VREF | I | The reference voltage for the error amplifier and the current sense amplifier. |
| VRETRACT | I | The retract voltage. If left open, the retract voltage will be the default setting. This value can be over-ridden by biasing VRETRACT externally. |
| VM1 | O | Connection for voice coil motor and sense resistor. |
| VM2 | O | Connection for the other side of voice coil motor. |
| SE1, SE2 | I | Sense voltage on the sense resistor. |

### MOTOR SPEED CONTROL

| | | |
|---|---|---|
| SYSCLK | I | System clock (input) pin. SYSCLK is 2.00 MHz nominal and is used to generate internal timing signals assuming a nominal 3600 RPM, 8-pole motor environment. |
| COMMU | O | Commutation count pin. COMMU is the LSB of the commutation counter. |
| REVCLK | O | REVCLK is COMMU divided by six. |
| $\overline{\text{UNIPOLAR}}$ | I | Unipolar mode (inverse) select pin. This pin will turn all upper drivers off when low. Pulled high internally to provide the default bipolar mode. |

**MOTOR SPEED CONTROL** (continued)

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| ADVANCE | I | Advance pin. ADVANCE is controlled by microprocessor during start mode to increment the commutation counter. The rising edge of ADVANCE will increment the counter. ADVANCE held high will inhibit internal incrementing of the counter, ADVANCE held low permits the normal operation of commutation from back-emf events. |
| INCOM | I | Commutation delay control pin. Adaptive commutation delay may be adjusted from its nominal value of one half the commutation interval by inserting or withdrawing current ot this pin. This should only be done via an external control loop which can compensate for the range of internal circuit parameter variations. |
| VIN | I | Control Voltage input pin. The internal driver transistors and internal predriver circuits form a transconductance amplifier which will set motor current in relation to VIN. In conjunction with Rsense at VSMN input and the gain of the Sense amplifier, transconductance (Gm) will be Gm = Im/VIN = 1/ (Rsense • 5). |
| A, B, C | O | Motor Drive Outputs. These pins provide drive to the motor coils. |
| CT | I | Back EMF input from motor coil center tap. Input connected to the center tap for sensing generated back emf voltages. It is also derived internally from A, B, C through a resistor network (y-connection). The circuit uses the back-emf voltages to determine rotor position and effect commutation. |
| RRAMP | I | Lower driver turn-off dv/dt setting resistor. External resistor from VPD to this pin sets the dv/dt slope of the motor coil voltage when the lower drivers are commutating to the off state. The dv/dt is given approximately by the relationship dv/dt (volts/second) = 1.5 • 10E10/Rramp. Typical value: RRAMP = 200K. |
| GAIN | I | Sense amplifier gain control pin. In normal operation, this pin is tied to high to set sense amplifier gain = 5. In low motor current operation, amplifier gain = 10 can be set by tying this input to low. |
| VSMP | I | Supply: Positive supply for spindle motor. |
| VSMN1, VSMN2 | I | Supply: Negative for spindle motor. Current monitoring sense amplifier (high side) input pin and motor current returns to ground. **All pins must be connected with low resistance circuit board traces.** The lower driver transistor current (hence motor current) comes out of these pins to Rsense resistor to monitor motor current. During normal (at speed) operation, the circuit will control the voltage across this resistor (multiplied by the gain of 5 in the sense amplifier) to match VIN. |
| | | **VVMP, VVMN, VSMP and VSMN conductors must be sized in accordance with anticipated motor current. The analog and digital supplies should be bypassed separately. VPA and VPD should be shorted externally, VNA and VND should be shorted externally.** |

## PIN DESCRIPTION

### MISCELLANEOUS

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| VBYP1 | I | The bypassed power supply. An external voltage for BRAKE and RETRACT circuitry. An external capacitor is attached to this pin and an internal circuit will charge this pin to VCC. The charge on this capacitor is used by the brake and retract function when VCC is removed (power-off). The capacitor must hold sufficient charge during the period when VCC is lost while retract is taking place (20 to 50 ms) so it will have enough voltage to drive the outputs during braking. Very little current is used during power-off braking so that C can be chosen from the retract conditions:<br>C ≥ Tretract • Ivbyp (float mode) / .5 volt<br>or approximately:<br>C ≥ 500E-6 • Tretract<br>This pin is normally a diode drop below VPA, rising by VBEMF during retract. |
| VBYP2 | I | The other side of the bypass capacitor connection. This pin is normally at VNA, rising to VBEMF during retract. |
| VBEMF | I | Rectified spindle back emf voltage. This voltage drives the internal retract FET. |
| SLEEP | I | Sleep pin. When asserted high, internal counters and registers are cleared. Refer to Table 2. Also forces an internal voltage fault which causes a head retract. Disables all output drivers, powers down all other circuitry except the over-temperature and voltage fault circuitry. |
| $\overline{\text{RETRACT}}$ | I | Retract (inverse) pin. When asserted low, forces a retract. Refer to Table 2. |
| $\overline{\text{BRAKE}}$ | I | Brake (inverse) pin. $\overline{\text{BRAKE}}$ is used to provide a delay between the initiation of fault-induced head retract and motor braking. A capacitor to ground and a resistor to $\overline{\text{SYSRST}}$ are selected such that 1.2 • R • C is equal to the maximum time required for retract. Refer to Table 2. |
| $\overline{\text{OTSD}}$ | O | Over-Temperature Sense Detect. Excessive die temperature will bring this open drain output low. Spindle motor and positioner drivers are disabled whenever $\overline{\text{OTSD}}$ is asserted. |
| VCHK | I | Comparator input for power supply monitoring. |
| VBGAP | O | An internal voltage reference for use with the power supply monitor comparator. |
| IBR | O | A resistor is tied from this pin to ground to establish the bias current for internal circuitry. |
| $\overline{\text{RCRST}}$ | I/O | This pin serves the dual purpose of providing power on reset and stretching short VFAULT pulses to a width suitable for the host microcontroller. An external RC network sets the minimum width of any $\overline{\text{SYSRST}}$ pulse. |
| $\overline{\text{SYSRST}}$ | O | When low, this open drain output indicates that an internal voltage fault has occured or that $\overline{\text{RCRST}}$ has been pulled low. |

## ELECTRICAL SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS

Operation above absolute maximum ratings may permanently damage the device.

| PARAMETER | SYMBOL | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply Voltage | VPA, VPD,<br>VVMP, VSMP (1, 2) | -0.3<br>-0.3 | 7.0<br>7.0 | V<br>V |
| Output Current | Imax (in or out of<br>A, B, C, VM1, VM2) | -1.0 | 1.0 | Amp |
| Analog I/O | VIN, RRAMP, | -0.3 | VPD + 0.3 | V |
| Voltage on pins | CT, A, B, C, VBEMF,<br>VBYP1, VBYP2 | -0.3 | 12.0 | V |
| | VM1, VM2, SE1, SE2 | -0.3 | 7.0 | V |
| | All other pins | -0.3 | VPD + 0.3 | V |
| Storage Temperature | Tstg | -65 | 150 | °C |
| Lead Temperature<br>(10 sec duration) | Tlead | 0 | 300 | °C |

### OPERATING CONDITIONS

| PARAMETER | SYMBOL | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply Voltage | VPA, VPD<br>VVMP, VSMP | 4.5<br>4.5 | 5.5<br>5.5 | V<br>V |
| Supply Current | I (VPA + VPD) | | 20 | mA |
| | I (VPA + VPD +<br>VVMP + VSMP)<br>Sleep mode | | 20 | mA |
| | IVVMP | | 0.4 | A |
| | IVSMP | | 0.5 | A |
| VBEMF | | 1.0 | 10.0 | V |
| VREF | | 0.5 | VPA-2 | V |
| VIN | | 0 | 2.5 | V |
| Vin, VSMN1, VSMN2 * | Normal operation | 0.0 | 0.50 | V |
| RF | | 10 | | kΩ |
| RC | | 10 | | kΩ |
| RBIAS | | 112 | 114 | kΩ |
| Ambient Temperature | Ta | 0 | 70 | °C |
| Capacitive Load Digital I/O | Cl | 0 | 100 | pF |

**OPERATING CONDITIONS** (continued)

| PARAMETER | SYMBOL | MIN | MAX | UNIT |
|---|---|---|---|---|
| Analog Outputs | CI | 0 | 50 | pF |
| Resistive Load Analog Outputs | RI | 10 | | kΩ |
| Power Dissipation | Pd | | 500 | mW |
| * Transconductance gain from VIN to motor current (steady-state) will be given by: G = Imotor/VIN = 1/(Rsense • 5) | | | | |

**PARAMETRIC REQUIREMENTS**

**Digital Input/Output**

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Fclk, SYSCLK | | 1.5 | | 2.5 | MHz |
| Twh, Twl, SYSCLK width high or low | | 40 | | | ns |
| Input Leakage ($\overline{\text{UNIPOLAR}}$) | | -50 | | 10 | µA |
| Input Leakage (all other pins) | | | | 10 | µA |
| Vil ($\overline{\text{BRAKE}}$) | | | | 1.2 | V |
| Vih ($\overline{\text{BRAKE}}$) | | 2.0 | | | V |
| Vil (all other digital inputs) | | | | 0.8 | V |
| Vih (all other digital inputs) | | 2.0 | | | V |
| Output Sink current | Vo = 0.4V | 1.6 | | | mA |
| $\overline{\text{RCRST}}$, $\overline{\text{OTSD}}$ | | | | | |
| $\overline{\text{SYSRST}}$ | Vo = 0.4V | 4.0 | | | mA |

**Digital Output COMMU, REVCLK**

| | | | | | |
|---|---|---|---|---|---|
| Voh | Iout = -100 µA | 2.4 | | | V |
| Vol | Iout = 2.0 mA | | | 0.4 | V |

**VIN**

| | | | | | |
|---|---|---|---|---|---|
| Input Current | 0 ≤ Vin < 2.5V | -1 | | +1 | µA |

**Outputs A, B, C**

| | | | | | |
|---|---|---|---|---|---|
| Total voltage drop | 32H6810 | Imotor = 200 mA, $V_{PD}$ = 4.5V | | 0.5 | V |
| across power FETs | 32H6810A | Imotor = 500 mA, $V_{PD}$ = 4.5V | | 0.85V | V |

**CT, And A, B, C, When Not Driving**

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Rin | -0.3V ≤ Vin < 7V | 5K | 9K | | Ω |
| Cin @ CT | | | | 20 | pF |
| Cin @ A, B, C | | | | 200 | pF |

**VBYP1**

| | | | | | |
|---|---|---|---|---|---|
| IVBYP1 (run) | VDD = 4.5V | | | 100 | µA |
| IVBYP1 (retract) | VDD = 0.5V, VBYP1 = 3V | | | 20 | µA |
| IVBYP1 (brake) | VDD ≤ 0.5V, VBYP1 = 3V | | | 10 | µA |

**BEMF**

| | | | | | |
|---|---|---|---|---|---|
| IBEMF | VBEMF = 4V | | | 300 | µA |
| IBEMF (retract) | I (VM1) = I (VM2) = 0,<br>I (VBYP2) = 0 | | | 20 | µA |

**SOUT**

| | | | | | |
|---|---|---|---|---|---|
| Gain | | 3.9 | | 4.1 | V/V |
| Input Offset | SOUT = VREF | -3 | | 3 | mV |
| Output Swing | $R_L$ = 10 kΩ to VREF | 0.15 | | VP-1 | V |

**ERR**

| | | | | | |
|---|---|---|---|---|---|
| ERRM Input Offset | ERR = ERRM | -15 | | 15 | mV |
| ERR Output Swing | | 1.55 | | VP -1.25 | V |

**POSITIONER**

| | | | | | |
|---|---|---|---|---|---|
| (VM1 - VM2) / (ERR - VBGAP) | | 11 | | 13 | V |
| Crossover Time | Imotor = 10 mA, PP @ 1 KHz,<br>RL= 16Ω, RSENSE = 0.5Ω | | 10 | 25 | µs |
| Output Distortion | Imotor = 100 mA, PP @ 100 Hz<br>RL= 16Ω, RSENSE = 0.5Ω | | | 2 | %THD |

**VBGAP**

| | | | | | |
|---|---|---|---|---|---|
| Bandgap Voltage | Iout < ±0.2 mA | 2.13 | | 2.37 | V |

**VCHK**

| | | | | | |
|---|---|---|---|---|---|
| Offset | | -15 | | 15 | mV |

**OUTPUT VM1, VM2**

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Total voltage drop across power FETs | I = 400 mA | | | 1.0 | V |

**SWIN**

| | | | | | |
|---|---|---|---|---|---|
| On Resistance | | | | 250 | Ω |

**RETRACT**

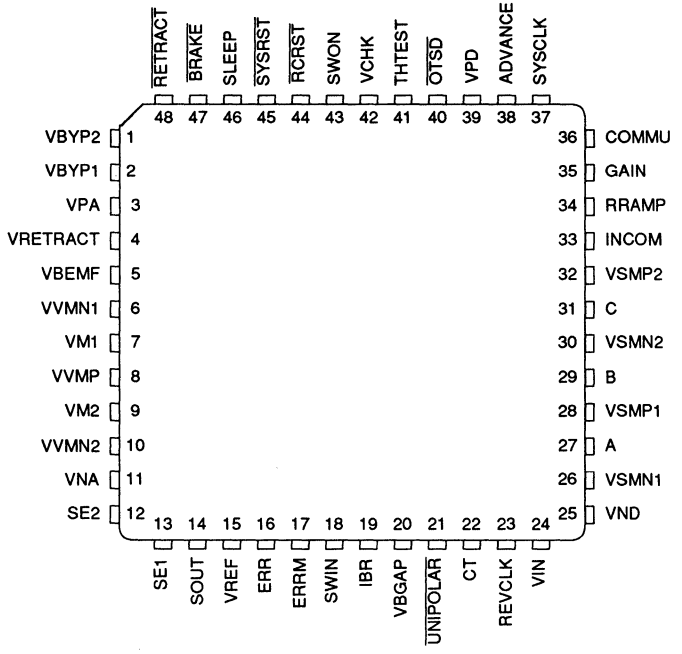
| | | | | | |
|---|---|---|---|---|---|
| VRETRACT Offset | VRETRACT = 0.1V<br>VBEMF ≥ 1V<br>RL = 16Ω | -100 | | 0 | mV |
| Short Circuit Current | VRETRACT = 0.5V<br>VBEMF = 1V<br>VBYP1 = 4.5V<br>VM1 = VM2 | 60 | | | mA |
| | VRETRACT = 0.5V<br>VBEMF = 1.5V<br>VBYP1 = 4.5V<br>VM1 = VM2 | 100 | | | mA |

$\overline{\text{OTSD}}$ (Thermal Shutdown)

| | | | | | |
|---|---|---|---|---|---|
| Die temperature | | 125 | | 145 | °C |

## PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.




**48-Lead TQFP**

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**Advance Information:** Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.



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**Notes:**

silicon systems®
A TDK Group Company

# SSI 32H6811
## Servo Motor Speed 5V Driver/DACs

**Advance Information**

January 1993

## DESCRIPTION

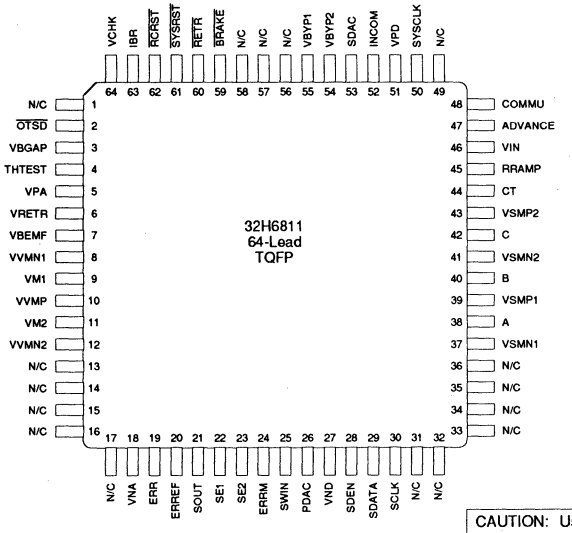
The SSI 32H6811 Servo and MSC Drivers, a CMOS monolithic integrated circuit housed in a 64-lead TQFP package, operates from a single 5V supply. It provides a fully integrated servo driver and a spindle motor commutator with internal power FETs. The servo driver is intended for use in disk drive head positioning systems employing linear or rotary voice coil motors. The commutator in conjunction with a microprocessor (μP) or digital signal processor (DSP), provides a complete spindle motor speed control system. It also includes two 10-bit D/A converters, with a serial interface to commonly used μP or DSP, for commanding the servo positioner and the spindle motor respectively. The device is ideal for use in 5V small-form disk driver applications.

## FEATURES

- **Internal 1.0A servo driver with no deadband, class-B output**
- **Thermal overload protection**
- **Power fault detection with built-in retract circuitry**
- **10-bit VCM D/A converter with 4 μs digital delay**
- **Gain select switch for a wide dynamic range of servo inputs**
- **Internal precision voltage reference**
- **Programmable commutation delay for optimal motor efficiency**
- **10-bit MSC D/A converter with 4μs digital delay**
- **Internal 1.0A spindle driver**
- **Switch-mode current limiting for spindle motor start-up**
- **Serial interface compatible with 80C196 and 68HC16**
- **Low power CMOS design with sleep mode**
- **64-lead TQPF package**

6

## PIN DIAGRAM




**64-LEAD TQFP**

CAUTION: Use handling procedures necessary for a static sensitive component.

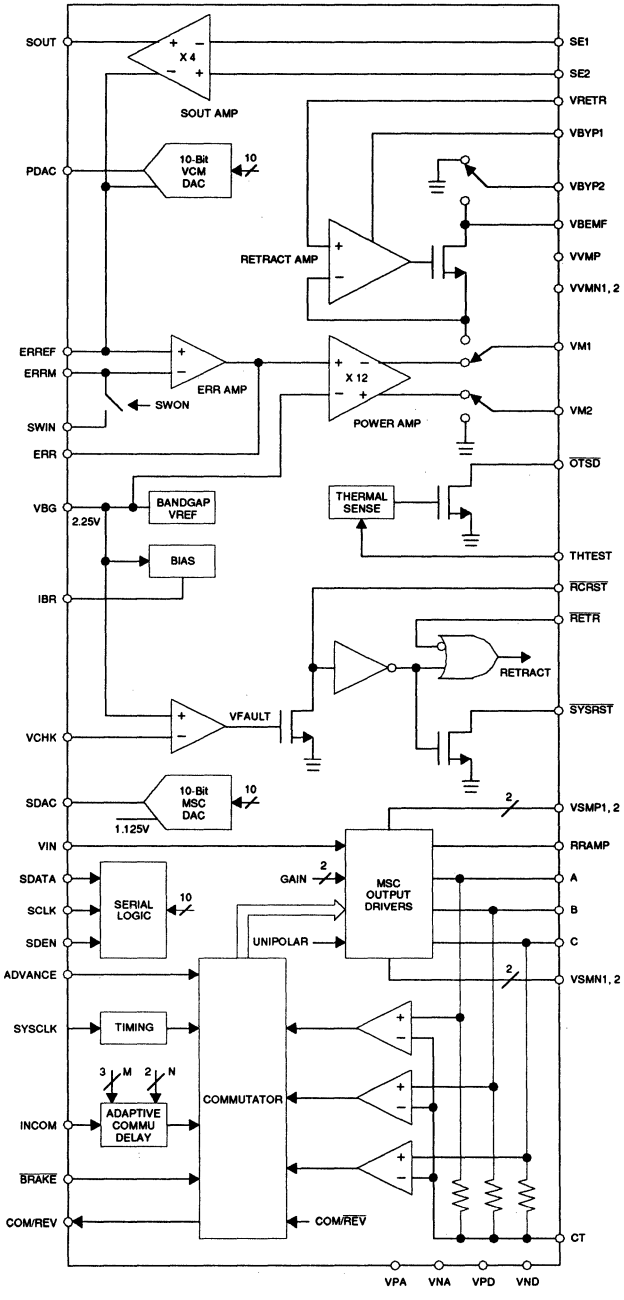



**FIGURE 1: SSI 32H6811 Functional Block Diagram**

## FUNCTIONAL DESCRIPTION

As shown in Figure 1, the SSI 32H6811 can be divided into four major sections: Servo positioner, Spindle motor commutator/driver, Control circuitry and Serial interface port.

### Servo Positioner

The servo positioner is a power transconductance amplifier for use in driving a voice coil servo motor (VCM). It has two primary modes of operation, normal (or linear) and retract. The retract mode is activated by a power supply failure or when $\overline{\text{RETR}}$ is asserted low while $\overline{\text{BRAKE}}$ being high. Otherwise the device operates in linear mode. The servo positioner consists of SOUT amplifier, ERR amplifier, retract amplifier, power amplifier and 10-bit VCM D/A converter.

### SOUT Amplifier

The SOUT amplifier generates a voltage at SOUT, proportional to positioner current, by sensing the voltage across Rs, amplifying and referencing to ERREF. Since the common mode voltage on Rs can range over the full power supply, while the differential voltage is in the order of millivolts, the SOUT amplifier is realized with a high input common mode rejection and low input offset.

### ERR Amplifier

The ERR amplifier is a high gain op amp. Due to the fixed gain of the power amp, ERR is proportional to the VCM voltage. The negative input of this amplifier is the system summing junction for the currents which are proportional to the desired VCM current, the measured VCM current, and the VCM voltage.

### Power Amplifier

The power amplifier is a fixed gain voltage amplifier with differential inputs and outputs. Its input is the differential voltage between ERR and VBG. Its output drives the VCM directly through an internal NMOS bridge. An internal charge pump generates gate voltages higher than VVMP so the upper NMOS devices can drive VM1 and VM2 up to VVMP.

### Retract Amplifier

When a voltage fault is sensed, or when $\overline{\text{RETR}}$ is asserted low while $\overline{\text{BRAKE}}$ being high, the servo positioner enters into retract mode. In this mode, it is assumed that no current is available for VVMP. Thus power for this mode comes from VBEMF, the rectified spindle back emf voltage, and from VBYP1, a voltage generated from an external storage capacitor CBYP. The retract amplifier is powered by VBYP1. It senses the voltage at VRETR and, through a power NMOS source follower, raises VM1 to VRETR. The drain of the source follower is VBEMF.

### VCM D/A Converter

Switched-capacitor circuit technique is employed to implement the VCM D/A converter with two non-overlapped clock phases, one phase for auto-zeroing and another one for evaluation. These two phases run synchronously with an internal 250 kHz clock, which is derived directly from the system clock at SYSCLK.

The request of the VCM D/A converter is initiated by writing to the VCM D/A register (00) through the serial interface port. The input data word must be coded in two's complement form. Note that there would be a maximum of 2 µsec of latency between a conversion request and the actual start of conversion. The conversion delay from the actual start of conversion to when the analog output begins to slew to a new value is 2 µsec. Therefore a maximum of 4 µsec is required for a conversion in addition to the time needed for completion of a serial data transfer, which is equal to 16/SCLK.

The VCM D/A converter provided at PDAC is referenced to ERREF, which also serves as a reference voltage for the error amplifier and the current sense amplifier.

### Spindle Motor Commutator/Driver

The spindle motor commutator in conjunction with external components provides the motor driving capability for starting, accelerating and rotational speed regulation for brushless DC motors without the need for Hall sensors. The speed regulation control loop is completed with a µP or DSP external to this device.

### Commutator

Motor speed control may be accomplished by measuring the period of the output signal at COM/REV. COM/REV may be defined as either the LSB of the commutation counter (COMMU) or the revolution clock of the motor (REVCLK), selected via the bit COM/$\overline{\text{REV}}$ in the mode register (10). Motor armature position is deter-

mined by monitoring the coil voltage of the winding that is not presently being driven by the drivers. The back emf from the coil, in conjunction with the state of the output drivers, indicates the armature position. The back emf is compared with a reference CT and initiates commutation "events" when the appropriate comparison is made. Commutation is the sequential switching of drive current to the motor windings. Because the back emf comparison event occurs prior to the time when optimum commutation should occur, it is preferred to delay commutation by a predetermined time after the comparison. The commutation delay is provided by a circuitry which measures the interval between comparison events and delays commutation by a time equal to 3/7 of the prior measured interval. The circuit is adaptive and will provide the optimum delay for a wide range of motor speeds (-80% to 50% of the nominal value). Since the commutation of motor coils typically causes transients, the commutation delay circuit also provides a noise blanking function which prevents the circuit from responding to back emf comparison events for a period of time equal to 4/7 of the interval between events after the comparison event. The commutation table is described in Table 1.

### Transconductance Amplifier

Input pin VIN is the non-inverting input of a transconductance amplifier which uses the lower driver transistor, that is presently active per the commutation state, as the power driver element. An external resistor is used to sense the current flowing through the drive transistor source (and hence the motor coil current). The voltage across the sense resistor is amplified by a gain stage (Av = 5, 10, 20 or 30 selected by the GAIN bits in the MODE register) and fed to the inverting input of the transconductance output stage.

The 10-bit MSC D/A converter, referenced to VBG/2, is provided at SDAC for converting the commanding signal in digital format into an analog voltage. Its operation is similar to the VCM D/A converter, but is initiated by writing to the MSC D/A register (01) in two's complement form.

### Power Amplifier

The output pins A, B and C are intended to drive motor coils directly. The output drivers operate to reduce switching noise transients by limiting dv/dt during commutation. Each output consists of two N-channel MOSFET drivers, one for pullup to VSMP1 or VSMP2 and one for pulldown to VSMN1 or VSMN2. The pullup FET functions as a switch (1.5Ω maximum) with voltage rise and fall times of about 25 microseconds. The pulldown FET is a part of the transconductance amplifier which converts the voltage VIN into motor current (Imotor = VIN/(Rsense • Av), where Av is either 5, 10, 20 or 30). When the pulldown output is commutating to the off state, dv/dt on the respective pin is controlled such that dv/dt is approximately 15/RRAMP volts per microseconds, where RRAMP is measured in kohms.

### Motor Start-Up

Motor starting is accomplished by a companion µP or DSP via ADVANCE, $\overline{\text{RETR}}$, $\overline{\text{BRAKE}}$ and COM/REV. The µP can assert $\overline{\text{RETR}}$ and $\overline{\text{BRAKE}}$ low to initialize the commutation counter and then increment the counter with ADVANCE. After $\overline{\text{RETR}}$ and $\overline{\text{BRAKE}}$ are asserted low and de-asserted (the power-up condition for preparation to begin a starting sequence), the commutation state will be state 0 per TABLE 1, but the lower driver output B remains inactive to prevent current flowing through the motor (out of A which is high). On the first ADVANCE set high, the commutation state 1 is selected and the drivers are per TABLE 1. ADVANCE at logic high excludes internal commutations. COMMU provides feedback to the µP on motor activity.

### Switch-Mode Operation

Switch-mode operation is provided for limiting the motor current during motor start-up. Two values M and N, loaded into the mode register (10) through the serial interface, determines the basic switching parameters for the operation. The M (3 bits) sets the minimum "on" time of the lower drivers and sample delay time. The N (2 bits) sets the switching period. The timing is given by:

Minimum "on" time = (M+1) • 4 µs

Sample delay time = M • 4 µs

Switching period = (N+2) • (M+1) • 4 µs

Hence, Minimum duty cycle = 1/(N+2)

Sample delay time, defined as the time from turning the lower drivers "on" until switching transients have settled, is a function of the particular application and will be determined by the user.

The value of M=0 is defined as linear mode, no switching except normal commutation will occur.

For a proper switch-mode operation, three flyback diodes from outputs A, B, and C, and a blocking diode from the system power supply VCC to the VSMP1 and VSMP2 pins are required. The flyback diodes will provide power for retract (during power failure) at pins VSMP1 and VSMP2.

### Control Circuitry

The control circuitry consists of a power fault detector, a thermal overload circuit, and control logic. The inputs to the control circuitry are VCHK, $\overline{\text{RETR}}$, and $\overline{\text{BRAKE}}$, along with the internal signals from the thermal overload detector. The voltage fault detector monitors the system power supply VCC to prevent the VCM driver from responding to a false command during a power failure. The system power supply is applied at VCHK through an external resistor divider and compared with an internal voltage reference at VBG.

Four operating modes are selected via $\overline{\text{RETR}}$ and $\overline{\text{BRAKE}}$ (when the system power supply is present) per Table 2. With $\overline{\text{RETR}}$ and $\overline{\text{BRAKE}}$ asserted low, the VCM drivers are in a high impedance state, the MSC driver outputs A, B, and C are low impedance to ground (without current limiting), and analog circuits are de-biased. This is the "sleep" mode. It also provides dynamic braking to the spindle motor. With $\overline{\text{RETR}}$ asserted, $\overline{\text{BRAKE}}$ de-asserted, both VCM and MSC drivers are in a high impedance state, and the retract amplifier is activated and powered by the back emf of a spinning motor for retracting heads. For $\overline{\text{BRAKE}}$ asserted, and $\overline{\text{RETR}}$ de-asserted, the VCM drivers are in a high impedance state, the MSC driver outputs are low impedance to ground (without current limiting), and analog circuits are biased. Normal mode is given for $\overline{\text{RETR}}$ and $\overline{\text{BRAKE}}$ de-asserted.

When a power failure is sensed, the $\overline{\text{SYSRST}}$ is asserted low and the retract mode is activated. If the die temperature exceeds approximately 135 °C, the $\overline{\text{OTSD}}$ is asserted low and all output drivers (both VCM and MSC) are turned off. The drivers will become operative after the temperature is reduced and the ADVANCE is asserted high.



| STATE | COMMU | Pullups A | Pullups B | Pullups C | Pulldowns A | Pulldowns B | Pulldowns C |
|---|---|---|---|---|---|---|---|
| 0 | 0 | OFF | ON | OFF | ON | OFF | OFF |
| 1 | 1 | OFF | OFF | ON | ON | OFF | OFF |
| 2 | 0 | OFF | OFF | ON | OFF | ON | OFF |
| 3 | 1 | ON | OFF | OFF | OFF | ON | OFF |
| 4 | 0 | ON | OFF | OFF | OFF | OFF | ON |
| 5 | 1 | OFF | ON | OFF | OFF | OFF | ON |

**TABLE 1: Commutation States**

| $\overline{\text{OTSD}}$ | VCHK > VBG | $\overline{\text{RETR}}$ | $\overline{\text{BRAKE}}$ | Mode | Analog | Counter | VCM Driver | MSC Driver |
|---|---|---|---|---|---|---|---|---|
| 0 | x | x | x | Shutdown | ON | Active | Float | Float |
| 1 | 0 | x | 0 | Fault/Break | OFF | Active | Retract | Low Z |
| 1 | 0 | x | 1 | Fault/Retract | OFF | Active | Retract | Float |
| 1 | 1 | 0 | 0 | Sleep | OFF | Reset | Float | Float |
| 1 | 1 | 0 | 1 | Retract | ON | Active | Retract | Float |
| 1 | 1 | 1 | 0 | Brake | ON | Active | Float | Low Z |
| 1 | 1 | 1 | 1 | Run | ON | Active | Active | Active |

**TABLE 2: Mode of Operations**

**Serial Interface Port**

A synchronous serial port, compatible with the commonly used µP such as 80C196 and 68HC16, is used to input digital words for D/A converters and mode registers. It is shift register based I/O interface and consists of three pins SDEN, SCLK and SDATA. Data from uP is transferred 8 bits (one byte) at a time with the LSB first. A complete transfer requires two bytes which are formatted into an instruction and a data field.

Data received through SDATA is clocked into an internal 16-bit shift register at the rising edge of SCLK while SDEN is active high. At the end of each transfer, SDEN must return low. If SDEN remains high after the last bit (which is the MSB of the second byte) is received, any additional data on SDATA will be ignored. Data must be two bytes for each transfer. If, for any reasons, SDEN is brought low prior to the completion of the second byte, the write operation of the data will be aborted.

The instruction field includes the first six bits of the first byte and is defined per the table below. The data field is 10-bit wide and includes the last two bits of the first byte and the second byte.

| BIT | NAME | DESCRIPTION |
|---|---|---|
| 0 (LSB) | R/W | Read/Write control. It must be '0' for this device since all of its registers are write only. |
| 1, 2, 3 | DID0..2 | Device ID. These three bits define the SSI device for which the serial communication is to be established. '111' is designated for this device. |
| 4, 5 | ADDR0..1 | Register address. These two bits define the internal register to which data is transferred.<br>ADDR1 / ADDR0 / Register<br>0 / 0 / VCM D/A<br>0 / 1 / MSC D/A<br>1 / 0 / Mode<br>1 / 1 / Reserved |
| The mode register (10) is defined as: | | |
| 0 | SWON | Analog switch enable |
| 1, 2 | GAIN0, 1 | Sense amplifier gain select, default 0,0<br>GAIN1 / GAIN0 / Gain<br>0 / 0 / 30<br>0 / 1 / 20<br>1 / 0 / 10<br>1 / 1 / 5 |
| 3 | UNIPOLAR | Unipolar mode enable |
| 4 | N0 | LSB of N value - minimum duty cycle |
| 5 | N1 | MSB of N value |
| 6 | M0 | LSB of M value - sample delay time |
| 7 | M1 | M value |
| 8 | M2 | MSB of M value. |
| 9 | COM/$\overline{\text{REV}}$ | Select COMMU (=0) or REVCLK (=1) |

## PIN DESCRIPTION

### POWER SUPPLIES

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| VPA | | Analog positive supply. |
| VNA | | Analog ground. |
| VPD | | Digital positive supply. It should be shorted externally with VPA. |
| VND | | Digital ground. It should be shorted externally with VNA. VND is also the low side input to the current sense amplifier of the spindle motor and thus care should be taken to keep VND and the low side of the external resistor Rsense at the same potential. |
| VVMP * | | Positive supply used for voice coil motor. |
| VVMP1, 2 | | Negative supply used for voice coil motor. |
| VSMP1, 2 | | Positive supply used for spindle motor. |
| VSMN1, 2 | | Negative supply used for spindle motor. They are also the high side inputs to the current sense amplifier of the spindle motor. |
| * The circuit board contacts for VVMP, VVMN1, VVMN2, VSMP1, VSMP2, VSMN1, and VSMN2 must be sized in accordance with anticipated motor currents. All pins must be connected with low resistance circuit board traces. | | |

### SERVO POSITIONER

| | | |
|---|---|---|
| SWIN | I | The analog switch input. The other side of the switch is connected to ERRM. |
| ERRM | I | The inverting input of the error amplifier. |
| ERREF | I | The reference voltage for the error amplifier, the VCM D/A converter and the current sense amplifier. |
| ERR | O | The error amplifier output. ERR is to provide compensation to the transconductance loop and is reference to VBG. |
| SOUT | O | The current sense amplifier output. SOUT is referenced to ERREF. |
| VRETR | I | The retract voltage. If left open, the retract voltage will be the default setting. Otherwise, it can be over-ridden by biasing VRETR externally. |
| VBYP1 | I | The bypassed power supply. An external capacitor is connected to this node to store charge for use by the retract circuitry. This pin is normally a diode drop below VCC, rising by VBEMF during retract. |
| VBYP2 | I | The other side of the bypass capacitor is connected to this pin. It is normally at ground, rising to VBEMF during retract. |
| VBEMF | I | Rectified spindle back emf voltage. This input provides current to the internal retract power amplifier. |

**SERVO POSITIONER** (continued)

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| VM1 | O | One side of the voice coil motor. |
| VM2 | O | The other side of the voice coil motor and sense resistor combination. |
| SE1,SE2 | I | The voltage across the sense resistor for the voice motor current. |
| $\overline{\text{RETR}}$ | I | When asserted low, it forces a retract. Refer to Table 2. |
| PDAC | O | The 10-bit VCM D/A converter output. It is referenced to ERREF. |

**SPINDLE MOTOR COMMUTATOR/DRIVER**

| | | |
|---|---|---|
| SYSCLK | I | System clock input. SYSCLK is internally divided by a divider to generate an internal clock at 2 MHz. |
| COM/REV | O | When the COM/$\overline{\text{REV}}$ bit in the mode regsiter is low, this pin is defined as the LSB of the commutation counter. Otherwise, it is defined as the revolution clock of the spindle motor. |
| ADVANCE | I | ADVANCE is used to increment the commutation counter externally. The rising edge of ADVANCE will increment the counter by 1. When held high, it inhibits the counter from internal incrementing. When held low, it permits the normal operation of commutation from back emf events. |
| INCOM | I | Commutation delay control. Adaptive commutation delay may be adjusted from its nominal value of one half the commutation interval by sinking or sourcing current from this pin. This should be done via an external control loop which can compensate for the range of internal circuit parameter variations. |
| SDAC | O | The 10-bit MSC D/A converter output. It is referenced to VBG/2. |
| VIN | I | Control voltage input. The combination of the MOSFET drivers and the predriver circuit forms a transconductance amplifier which sets the motor current in relation to VIN. In conjunction with Rsense connected at VSMN and the gain of the sense amplifier, the transconductance is defined by:<br>Gm = Im/VIN = 1/($\overline{\text{Rsense}}$ • 4) |
| A, B, C | O | Spindle motor driver outputs. |
| CT | I | Back emf input from spindle motor coil center tap. Internal circuit uses the back emf voltages to determine the rotor position and effect commutation. |
| RRAMP | I | Lower driver turn-off dv/dt setting resistor. External resistor from VPA to this pin sets the dv/dt slope of the motor coil voltage when the lower drivers are commutating to the off state. The dv/dt is approximately given by the relationship: dv/dt=15/RRAMP, where dv/dt is expressed in volts/µs and RRAMP in kΩ. |
| $\overline{\text{BRAKE}}$ | I | $\overline{\text{BRAKE}}$ is used to provide a delay between the initiation of fault-induced head retract and spindle motor braking. A capacitor to ground and a resistor to $\overline{\text{SYSRST}}$ are selected such that 1.2RC is equal to the maximum time required for retract. |

**CONTROL CIRCUITRY**

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| VCHK | I | Comparator input for power supply monitoring. When VCHK is below VBG, an internal voltage fault is generated. |
| VBG | O | Voltage reference, generated from the internal bandgap voltage, for use with the power supply monitor comparator. |
| IBR | O | A resistor is tied from this pin to ground to establish a bias current for internal circuitry. |
| $\overline{\text{RCRST}}$ | O/C | This pin serves the dual purpose of providing power-on-reset and stretching short internal VFAULT pulses to a width suitable for the host micro controller. An external RC network sets the minimum width of any $\overline{\text{SYSRST}}$ pulse. If $\overline{\text{RCRST}}$ is pulled low by external circuitry, this device will enter into the retract mode and pull $\overline{\text{SYSRST}}$ low. |
| $\overline{\text{SYSRST}}$ | O/C | When low, this open-collector output indicates that an internal voltage fault has occurred. |
| $\overline{\text{OTSD}}$ | O/C | Thermal shut-down. When low, this open- collector output indicates that the junction temperature has exceeded the recommended operating range and the device is in thermal shut-down. In thermal shut-down, all output drivers are turned off and analog circuit de-biased. |
| THTEST | I | Biased low with an internal pull-down. When asserted high, $\overline{\text{RETR}}$ will be connected to the thermal overload test circuitry for use as a test input. |

**SERIAL INTERFACE PORT**

| | | |
|---|---|---|
| SDATA | I | Serial data input passing digital words for internal registers. |
| SCLK | I | Serial data timing reference. The rising edge of the SCLK is to strobe SDATA while SDEN is asserted high. |
| SDEN | I | Serial data transfer enable. When active high, the serial data transfer is enabled. |

## ELECTRICAL SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS

Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device or affect device reliability.

| PARAMETER | SYMBOL | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Supply voltage @ VPA, VPD, VVMP, VSMP1, VSMP2 | Vdd | -0.3 | | 7.0 | V |
| Motor current @ A, B, C, VM1, VM2 | Imax | | | ±1.0 | A |
| Input voltage @ VIN, RRAMP | Vin | -0.3 | | VDD+0.3 | V |
| Input voltage @ | | | | | |
| CT, A, B, C, VBEMF, VBYP1, VBYP2 | | -0.3 | | 12.0 | V |
| VM1, VM2, SE1, SE2 | | -0.3 | | 7.0 | V |
| Other pins | | -0.3 | | Vdd | V |
| Storage temperature | Tstg | -65 | | 150 | °C |
| Lead temperature (10 sec duration) | Tlead | 0 | | 300 | °C |

### RECOMMENDED OPERATING CONDITIONS

The recommended operating conditions for the device are indicated in the table below. Performance specifications do not apply when the device is operated outside the recommended conditions.

| PARAMETER | SYMBOL | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Supply voltage | Vdd | 4.5 | | 5.5 | V |
| Supply current | | | | | |
| VPA,VPD | Idd | | | 25 | mA |
| VVMP | Ivmp | | | 0.4 | A |
| VSMP | Ismp | | | 0.5 | A |
| Sleep mode | Isleep | | | 1.0 | mA |
| VBYP1,braking | Ibrk | | | 10 | µA |
| VBYP1,retract | Iret | | | 20 | µA |
| Input voltage @ VBEMF | | 1.0 | | 10 | V |
| Input voltage @ ERREF | | VBG/2 | VBG | VDD-2.0 | V |
| Input voltage @ VIN | | 0 | | 2.5 | V |
| Ambient temperature | Ta | 0 | | 70 | °C |
| Capacitive load on digital outputs | Cl | | | 100 | pF |

**RECOMMENDED OPERATING CONDITIONS** (continued)

| PARAMETER | SYMBOL | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Analog output load | Cl | | | 40 | pF |
| | Rl | 10 | | | kΩ |
| System clock fc = 8 MHz | | | | | |
| Frequency tolerance | fc | | | ±0.1 | % |
| Pulse width | Twh, Twl | 40 | | | ns |
| Biasing resistor Rbias = 22.6 kΩ | Rbias | | | ±5 | % |
| External resistors | Rf,Rc | 10 | | | kΩ |
| Power dissipation | Pd | | | 500 | mW |

## PERFORMANCE SPECIFICATIONS

**DIGITAL I/O**

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Digital input @ SDATA, SCLK, SDEN, ADVANCE, SYSCLK, $\overline{\text{RETR}}$ | | | | | |
| Vil | | 0.8 | | | V |
| Vih | | | | 2.0 | V |
| Iil, Iih | | | | ±10 | µA |
| Digital input @ $\overline{\text{BRAKE}}$ | | | | | |
| Vil | | 1.2 | | | V |
| Vih | | | | 2.0 | V |
| Iil, Iih | | | | ±10 | µA |
| Digital O/C output @ $\overline{\text{RCRST}}$, $\overline{\text{SYSRST}}$, $\overline{\text{OTSD}}$ | | | | | |
| Ioh | Voh = Vdd | | | 10 | µA |
| Iol | Vol = 0.4 | 4 | | | mA |
| Digital Output @ COM/REV | | | | | |
| Vol | Iol = 2.0 mA | | | 0.4 | V |
| Voh | Ioh = -100 µA | 2.4 | | | V |

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**SERVO POSITIONER**

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| BEMF current | | | | | |
| Normal mode | VBEMF = 4V | | | 300 | µA |
| Retract mode | VBEMF = 3V, Imotor = 0<br>IVBYP2 = 0 | | | 20 | µA |
| SOUT amplifier | | | | | |
| Gain | | 3.9 | | 4.1 | V/V |
| Input offset | SOUT = VBG | -3 | | 3 | mV |
| Output swing | $R_L$ = 10 kΩ to ERREF | 0.15 | | VDD-1 | V |
| ERRAMP amplifier | | | | | |
| Input offset | ERR = ERRM | | | ±15 | mV |
| Output swing | | 1.55 | | VDD-1.25 | V |
| Power amplifier (VCM Driver) | | | | | |
| Gain (VM1-VM2)/(ERR-VBG) | | 11 | | 13 | V/V |
| Output voltage drop | $R_L$ = 16Ω Tj = 25°C,<br>Imotor = 0.4A | | | 1.0 | V |
| Bridge crossover time | | | | | |
| Ivcm = 10 mA, pp @ 1 kHz | $R_L$ = 16Ω | | | 45 | µs |
| VCM output THD | | | | | |
| Ivcm=100 mA, pp @ 100 Hz | $R_L$ = 16Ω | | | 2 | % |
| SWIN on resistance | | | | 250 | Ω |
| Retract amplifier (retract), VRETR = 0.5V, VBEMF > 1V, $R_L$ = 16Ω | | | | | |
| offset | | -100 | | | mV |
| Maximum output current, VRETR = 0.5V, VBYP1 = 4.5V | | | | | |
| VBEMF = 1V, VM1 = VM2 | | 60 | | | mA |
| VBEMF = 1.5V, VM1 = VM2 | | 100 | | | mA |
| Retract Amplifier (normal)<br>VRETR leakage | | | | ±10 | µA |

### SPINDLE MOTOR COMMUTATOR/DRIVER

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Tshift, Shift Range in commu delay | INCOM = 0 to 0.8V<br>8-pole Motor @ 3600 rpm | | | ±15 | % |
| Input current @ VIN | 0 < VIN < 2.5V | | | ±1 | µA |
| Total FETs voltage drop | Imotor = 0.5A | | | 0.85 | V |
| Outputs @ CT, A, B, C while not driving | | | | | |
| Rin | -0.3V < Vin < 7V | 5 | | | kΩ |
| Cin | CT | | | 20 | pF |
| Cin | A, B, C | | | 200 | pF |

### CONTROL CIRCUITRY

| | | | | | |
|---|---|---|---|---|---|
| Vdd voltage for $\overline{\text{SYSRST}}$ & $\overline{\text{RCRST}}$ in operation | | 2 | | 5.5 | V |
| VBG | Iout < +0.2 mA | 2.18 | | 2.32 | V |
| VCHK comparator offset | | | | ±15 | mV |
| Thermal shutdown | | | | | |
| Temperature threshold | | 125 | | 145 | °C |
| Hysteresis | | | 5 | | °C |

### D/A CONVERTER

| | | | | | |
|---|---|---|---|---|---|
| Full-scale voltage | | | VBG | | V |
| Resolution | | | 10 | | bits |
| Digital Delay | | | | 4 | µs |
| LSB volatge | | | VBG/1024 | | V |
| Differential nonlinearity | | | | ±1 | LSB |
| ERREF | | | VBG/2 | VBG | V |

### SERIAL INTERFACE PORT

| | | | | | |
|---|---|---|---|---|---|
| SDEN setup time prior to SCLK | Tsens | 35 | | | ns |
| SDEN hold time after SCLK | Tsenh | 50 | | | ns |
| SDATA setup time prior to SCLK rise | Tds | 15 | | | ns |
| SDATA hold time after SCLK fall | Tdh | 15 | | | ns |
| SCLK pulse width | Tpw | 100 | | | ns |

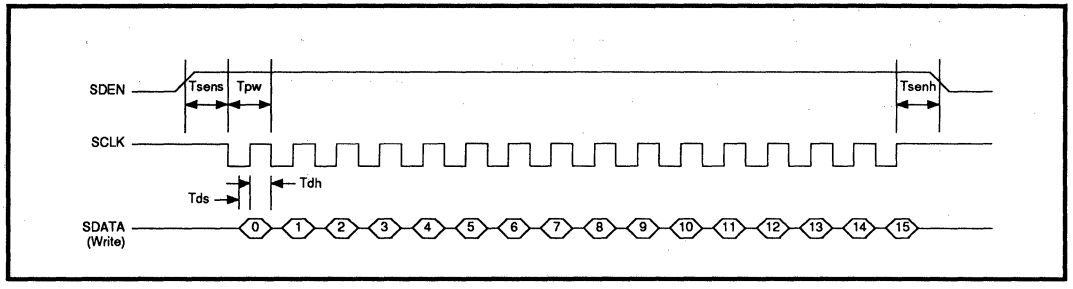
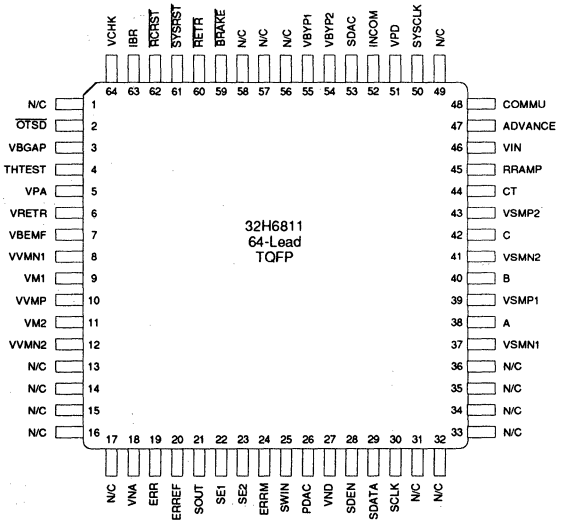



**FIGURE 2: SSI 32H6811 Serial Interface Timing Diagram**

## PACKAGE PIN DESIGNATIONS

(Top View)




**64-LEAD TQFP**

**Advance Information:** Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

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A TDK Group Company

# SSI 32H6830
## Servo DSP

**Advance Information**

December 1992

## DESCRIPTION

The SSI 32H6830, designated as the "Seeker™," contains a DSP, a 10-bit ADC, two 10-bit DACs, and sufficient I/O pins to perform the servo and MSC functions of a hard disk drive with no overhead to the master microprocessor. When fully programmed, the Seeker performs self-contained seek, track, and spindle control functions. When the device is given a track destination, it will seek to the desired track, generate an interrupt when it arrives on track, and then servo on the track. As a spindle controller, the Seeker will start the motor, spin it up to a speed indicated by the microprocessor, and generate an interrupt when proper speed has been achieved. The spindle controller is also capable of phase locking to a master spindle index and maintaining a specified phase with respect to the master index. The DSP will allow more sophisticated algorithms with better phase margin than those implemented with a microprocessor. The program and constants for the DSP are stored in the microprocessor ROM and are uploaded to the DSP. The part is optimized for use with the SSI 32H6810 motor speed commutator and servo amplifier device.

The Seeker offloads all sector rate processing from the microprocessor and allows it to spend nearly 100% of its time dealing with the controller chip; an essential feature as data rates approach 48Mbit/s. It also allows better algorithms to be implemented with less phase delay. This results in faster, quieter seek times and higher track bandwidths.

## FEATURES

- **Self contained seek, track, spindle start, spindle run, and spindle sync capability**
- **Can operate at a multiple of the sector rate to reduce latency time between seek command and start of seek**
- **DSP with 16 x 16 multiply in 200 ns**
- **10-bit 2 µs ADC with 6 input MUX**
- **Two 10 bit DACs**
- **Serial µP port for uploading program memory from system µP**
- **Interfaces with pulse detectors containing on board peak detectors such as SSI 32P548 and SSI 32P4730**

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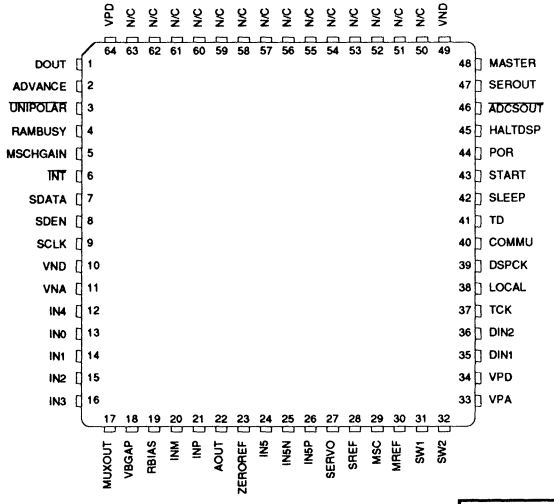
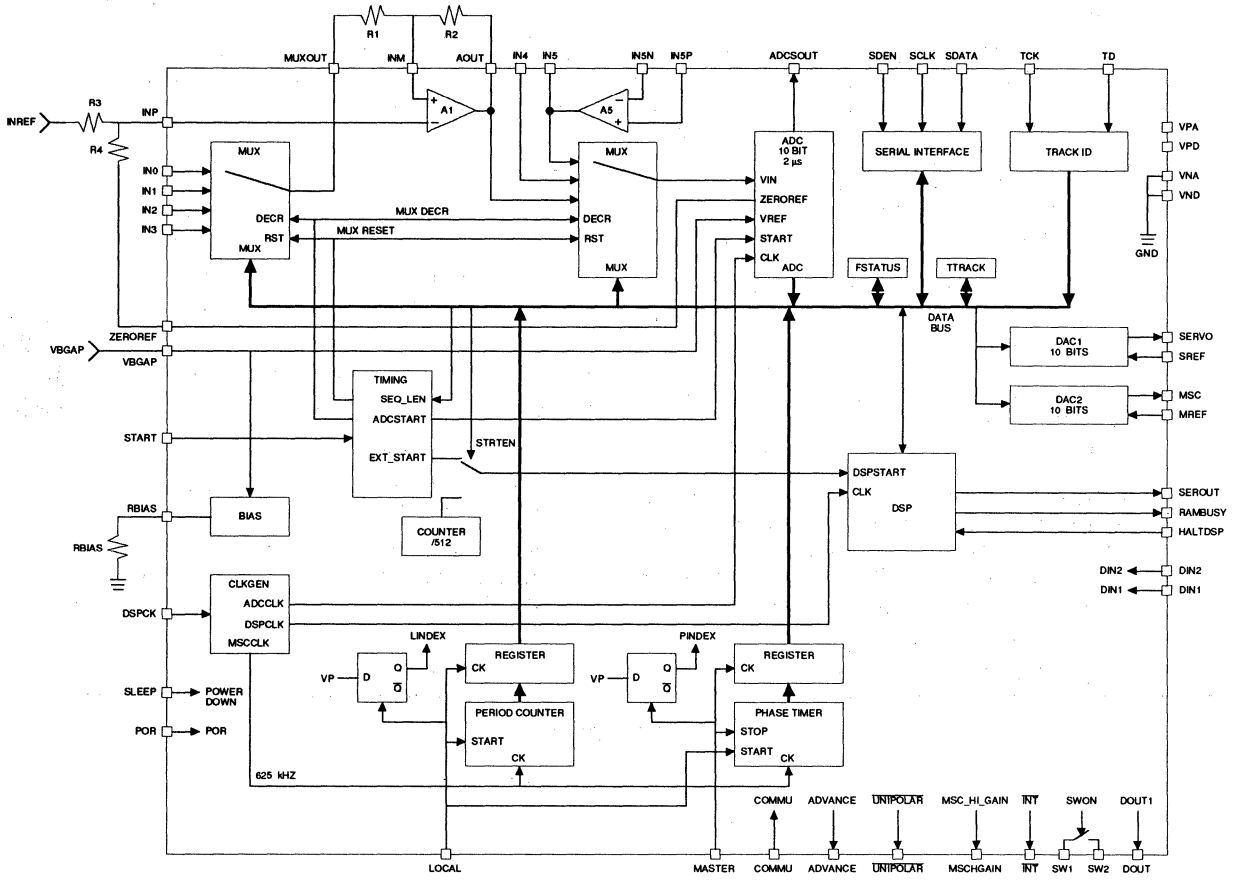
## PIN DIAGRAM




**64-Lead TQFP**

CAUTION: Use handling procedures necessary for a static sensitive component.

## BLOCK DIAGRAM



## FUNCTIONAL DESCRIPTION

### HARDWARE FUNCTIONAL BLOCKS

#### Front End

The Seeker front end consists of a 10-bit two's complement ADC, a 6-input MUX and some amplifiers whose gain can be set with external components. The front end is intended to be driven by pulse detectors like the SSI 32P548 that have internal peak detectors or integrators. External resistors perform gain and offset correction.

#### Front End Timing

A start pulse sets the MUX address to five, raises RAMBUSY, and initiates a sequence of consecutive ADC conversions. The result of each conversion is stored in the data RAM (DRAM) address 0 through 5, respectively. The MUX inputs are converted in reverse numerical order for IN0 through IN3. When the conversions are complete, other status words such as the state of the period and phase timers, the target track, and the current track are inserted in the DSP DRAM and a DSP code pass is started.

The start pulse can be generated by hardware (the START pin or an internal counter) or software (STARTBIT in FSTATUS.) If STRTEN (in FSTATUS) is high, the start signal is taken from the START pin. If it is low, the internal counter generates a start signal every 512 DSP clocks. STARTBIT generates a start regardless of any other pin or bit.

#### DSP Timing

When the DSP is started, the ADC values, DSPIN, TTRACK, PHTIME, PTIME, and TRACK have already been loaded in DRAM. These values will not be updated again until the next start pulse occurs. When the DSP reaches a STOP instruction, it halts, lowers RAMBUSY and waits for another start signal.

#### Track ID

The current track ID is demodulated and converted to binary by external circuitry. It is then supplied to the Seeker through a dedicated serial port. The track ID is transferred to DRAM address 10 when a DSP start pulse is received. Depending on the TRKMSB bit in the FSTATUS word, track ID is received either LSB or MSB first. Since the track ID register can handle up to 16 bits, the unused bits can be utilized as flag bits from the demodulator. Some possible uses for the flag bits are: warning the DSP that certain sector data as bad, and in oversampling applications, indicating to the DSP which start pulses are at the beginning of a sector.

#### Spindle Control Hardware

The MSC portion of the seeker will support start, run, and synchronized spindle modes. The MSC hardware consists of a period timer and a phase timer. The period counter starts on the rising edge of LOCAL and transfers its count to a latch when the next rising edge occurs. A status bit, LINDEX, is set whenever new data is available at the latch. The status bit will be high for one DSP code pass. The phase timer is also started on every LOCAL rising edge. It is stopped when MASTER rises. A status bit, MINDEX, indicates when new data from the phase timer is available. By comparing the value of the period timer and the phase timer, the actual phase error between local and master can be determined. The DSP controls spindle start by monitoring COMMU and asserting ADVANCE. See the SSI 32H6810 or equivalent data sheet for more details.

#### µP Serial Port

Through the serial port, the µP can read FSTATUS and any DRAM or IRAM memory word. It can write the FSTATUS and TTRACK registers as well as any DRAM or IRAM word. The registers are internally double buffered and can be accessed by the µP at any time. Access to RAM must be limited to when the DSP is idle. The format of the serial port data string is consistent with other Silicon Systems serial interfaces.

#### DAC1 and DAC2

These DACs are 10 bits wide. They are memory mapped to DRAM address 2 and 3 for DAC 1 and 2, respectively. Each DAC has its own zero-reference input. The full scale swing of each DAC is ±VBGAP/2. These DACs are intended to drive the servo and spindle buffers.

#### TTRACK Memory

This 16 bit word is accessed by the µP serial port. It is double buffered so the µP does not need to synchronize to RAMBUSY. When TTRACK is programmed to a new target track, the next DSPSTART pulse will transfer it to DRAM and cause a seek to begin.

## FUNCTIONAL DESCRIPTION (continued)

### FSTATUS Memory

This 16-bit word can be read and written by the µP. It is double buffered so the µP does not need to synchronize to RAMBUSY.

### Interrupt

The $\overline{INT}$ output is controlled by the DSP. It is typically used to indicate an event of interest to the µP such as spindle control achieving lock, or the head arriving at its target, or at other times, spindle control losing lock or the head falling off track. Upon receiving the interrupt, the µP should read FSTATUS to determine the interrupt type. Reading FSTATUS clears the $\overline{INT}$ output.

### SEROUT

This is an output serial port used for diagnostic purposes. Whenever the DSP writes to this port, the bits are shifted out at the DSP clock rate. SEROUT normally sits high. A leading zero prefixes all outputs as a marker. This pin is useful for monitoring internal data words while the DSP is operating in real time.

### Software Interface to µP

The µP is able to read or write any word in the IRAM or DRAM. In addition, it is able to read and write the FSTATUS register, and to write the TTRACK register.

### FSTATUS Register—Read

The first 4 bits are interrupt status bits. They are written by the DSP and cause an interrupt to be initiated whenever they change state. The second four bits are information bits and do not affect $\overline{INT}$. The third group of 4 bits are interrupt flags, indicating which of the interrupt status bits caused an interrupt. The last 4 bits are for version control and future reserved functions. Note that whenever FSTATUS is read, $\overline{INT}$ is deasserted and the interrupt flags are cleared.

| Bit | Name | Description |
|---|---|---|
| 0 | Spare_INT | When this bit changes state, $\overline{INT}$ is asserted. |
| 1 | Ontrack | Indicates that the head is on track. When this bit changes state, $\overline{INT}$ is asserted. |
| 2 | At_speed | Indicates that the spindle is at speed. When this bit changes state, $\overline{INT}$ is asserted. |
| 3 | Phase_lock | Indicates that the local index is phase locked to the master index. When this bit changes state, $\overline{INT}$ is asserted. |
| 4 | Track/Seek | Indicates if the DSP is in track mode. |
| 5 | RAMBUSY | Indicates the DSP RAM is servicing the DSP and is "locked out" of the µP serial interface. |
| 6 | DSTAT11 | Bit 11 of DSPSTATUS |
| 7 | DSTAT12 | Bit 12 of DSPSTATUS |
| 8 | INTF0 | Is set when bit 0 changes state. Is cleared when FSTATUS is read. |
| 9 | INTF1 | Is set when bit 1 changes state. Is cleared when FSTATUS is read. |
| 10 | INTF2 | Is set when bit 2 changes state. Is cleared when FSTATUS is read. |
| 11 | INTF3 | Is set when bit 3 changes state. Is cleared when FSTATUS is read. |

**FSTATUS Register—Read** (continued)

| Bit | Name | Description |
|---|---|---|
| 12 | REV0 | LSB of revision number. |
| 13 | REV1 | MSB of revision number. |
| 14 | RESERVED | |
| 15 | RESERVED | |

**FSTATUS Register—Write**

| | | |
|---|---|---|
| 0 | STRTEN | Selects DSPSTART from the timing block instead of the divide-by-512 counter. |
| 1 | TRKMSB | Sets the TRACK ID serial to parallel converter to "MSB first" mode. |
| 2 | HALTBIT | Serves the same purpose as the HALTDSP pin. When asserted, the DSP will continue executing its current code pass and then will remain idle, ignoring both external and internal hardware start pulses. This bit should be set by the µP during initialization of the Seeker. |
| 3 | STARTBIT | Is a third way of creating a "start." When HALTBIT is asserted, this is the only way to create a "start." If this bit is programmed to 1, the usual sequence of ADC conversions and data transfers to DRAM is initiated. The DSP code pass will not be initiated, however. Instead the DSP will wait for SS pulses. STARTBIT is automatically cleared after it is written. |
| 4 | SS | This bit is ignored except if HALTBIT is asserted. In that case, every "one" written to SS causes the DSP to advance one clock cycle. SS is automatically cleared after it is written. |
| 5 | RESETBIT | Resets the Seeker to the state where the µP serial interface has complete access. This bit should be set by the µP before initializing the Seeker. |
| 6 | RESUMEBIT | Terminates the single step mode by resuming DSP execution at full speed. |
| 7 | FS7 | A spare bit for communication from µP to DSP. |

## FUNCTIONAL DESCRIPTION (continued)

### Serial Port

The serial port is designed to be shared by other devices. For this reason, a device ID is included in the preamble. The device ID conforms to the Silicon Systems standard: 1-R/W, 2-Pulse Det, 3-Filter, 4-Data Sep, 5-ENDEC, 6-Time Base, 7-Servo/MSC. Bit 0 of the serial port is received first. Each bit string received by the serial port can be unlimited in length but consists of the following initial fields:

| Bit # | Field | Description |
|---|---|---|
| 0 | R/W | Indicates whether data is to be read or written. |
| 1..3 | Device ID | Identifies the device being programmed (LSB is bit 1). Must be '7' to communicate with this part. |
| 4..5 | Type | Indicates which memory is addressed (LSB is bit 4):<br>0 FSTATUS<br>1 TTRACK (write only)<br>2 DRAM or ACCUMULATOR<br>3 IRAM or PROGRAM COUNTER |
| 6..7 | Address bank | The bank address for memories with more than 256 words. These bits are ignored if FSTATUS or TTRACK is being accessed. Note that if bank is 11, type 2 and 3 become ACCUMULATOR and PROGRAM COUNTER respectively. |
| 8.115 | Address | The RAM address (LSB is bit 8). This field must always be sent except when accessing FSTATUS or TTRACK. |
| 16.. or 8.. | Data | The data (LSB first). If RAM data is being read or written, consecutive data words can be concatenated. The address will automatically increment after each 16 (DRAM) or 20 (IRAM) bits. The address bank is automatically incremented when necessary. |

### DSP Memory Map

The DSP communicates with the Seeker chip through memory mapped regions of DRAM. The first 10 words are mapped to various hardware resources as defined below. Note that the first four words are "write protected." The remaining words are initialized at the beginning of each DSP code pass and may then be modified or overwritten by the DSP.

| DRAM Address | Read by DSP | Written by DSP |
|---|---|---|
| 0 | ADC5 (write protected) | DSPSTATUS |
| 1 | ADC4 (write protected) | SEROUT |
| 2 | ADC3 (write protected) | DAC1 |
| 3 | ADC2 (write protected) | DAC2 |
| 4 | ADC1 | |
| 5 | ADC0 | |
| 6 | DSPIN | |
| 7 | TTRACK | |
| 8 | PTIME (period time) | |
| 9 | PHTIME (phase time) | |
| 10 | TRACK | |



### DSPSTATUS and DSPIN

DSPIN is the word the DSP uses to communicate with bits set by the µP or by Seeker input pins. DSPSTATUS is the word the DSP uses to control bits read by the µP and external pins controlled by the DSP. Whenever the first 4 bits of DSPSTATUS are changed by the DSP, $\overline{INT}$ is asserted. The bits in DSPIN and DSPSTATUS are defined below.

| BIT | DSPIN (Read by DSP) | DSPSTATUS (Written by DSP) |
|---|---|---|
| 0 | COMMU (from COMMU pin) | SPARE_INT (to FSTATUS) |
| 1 | LINDEX (from period timer) | ONTRACK (to FSTATUS) |
| 2 | MINDEX (from phase timer) | ATSPEED (to FSTATUS) |
| 3 | DIN1 (from DIN1 pin) | PHLOCK (to FSTATUS) |
| 4 | DIN2 (from DIN2 pin) | TRACK/SEEK (to FSTATUS) |
| 5 | LOCAL (from LOCAL pin) | $\overline{UNIPOLAR}$ (to pin) |
| 6 | MASTER (from MASTER pin) | MSCHGAIN (to pin) |
| 7 | FS7 (from FSTATUS) | ADVANCE (to pin) |
| 8 | | DOUT (to pin) |

## FUNCTIONAL DESCRIPTION (continued)

**DSPSTATUS and DSPIN** (continued)

| BIT | DSPIN (Read by DSP) | DSPSTATUS (Written by DSP) |
|---|---|---|
| 9 | | SWON (to SW1, SW2 switch) |
| 10 | | DSTAT11 (to FSTATUS) |
| 11 | | DSTAT12 (to FSTATUS) |
| 12 | | not used |
| 13 | | not used |
| 14 | | not used |
| 15 | | not used |

## PIN DESCRIPTION

The following description lists each pin, associates a pin type to it, and provides a brief description of the pin's function.

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| VPA, VPD | VCC | Analog and digital power supplies. |
| VNA, VND | GND | Analog and digital grounds. |
| IN0, IN1, IN2, IN3 | Ana In | The four primary inputs automatically converted by the A/D. These inputs drive a low resistance analog switch. |
| MUXOUT | Ana Out | The output of the IN0..IN3 mux. |
| INM | Ana In | The inverting input to amplifier A1. |
| AOUT | Ana Out | The output of amplifier A1. |
| INP | Ana In | The non-inverting input to A1. |
| VBGAP | Ana In | The voltage reference input. This will determine the full scale swing of the ADC and the two DACs. |
| ZEROREF | Ana Out | The ADC zero reference output. Can be used by the A1 resistor network to level shift IN0 through IN3. |
| IN4 | Ana In | A direct input to the ADC mux. |
| IN5 | Ana Out | The output of amplifier A5. |
| IN5N, IN5P | Ana In | The inputs to amplifier A5. |
| RBIAS | Ana Out | A resistor to ground from this pin sets the bias current for the analog circuitry. |
| SERVO | Ana Out | The output of the servo DAC. |
| SREF | Ana In | The servo DAC reference. The DAC output swing will be SREF-0.5•VBGAP to SREF+0.5•VBGAP. |
| MSC | Ana Out | The output of the MSC DAC. |
| MREF | Ana In | The MSC DAC reference. The DAC output swing will be MREF-0.5•VBGAP to MREF+0.5•VBGAP. |

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| SW1, SW2 | Ana In | The two terminals of an uncommitted analog switch. The switch is controlled by the SWON bit in the DSP STATUS word. |
| ADCSOUT | Dig Out | A test point from the ADC. This test point is connected to the output of the ADC comparator. |
| START | Dig In | A rising edge on START initiates consecutive ADC conversions and causes a pass through the DSP code to begin. |
| DSPCK | Dig In | The master clock (20 MHz) for the chip. |
| SLEEP | Dig In | Reduces the supply current of the chip. All analog circuitry is deactivated, with outputs becoming high impedence. The chip clock is deactivated. No data will be lost in RAM due to the use of static RAM. |
| POR | Dig In | Chip reset. This pin is for diagnostic purposes and should be grounded in normal operation. |
| SDEN | Dig In | The µP serial interface enable. SCLK and SDATA are ignored and the interface reset when SDEN is low. |
| SCLK | Dig In | The µP serial interface clock. |
| SDATA | Dig I/O | The µP serial interface data. This pin is an input except for the data cycles of a serial read request. |
| TCK | Dig In | The clock for the current track serial input. |
| TD | Dig In | The data for the current track serial input. |
| SEROUT | Dig Out | The serial output from the SEROUT word memory mapped into DRAM. This output can be used to monitor the DSP during real time applications. |
| RAMBUSY | Dig Out | When high, the DSP is executing code. When low, it is waiting for a START pulse. |
| HALTDSP | Dig In | When high, halts the DSP. Similar in function to HALTBIT in FSTATUS. This pin or HALTBIT should be asserted during µP access of DRAM and IRAM. |
| LOCAL | Dig In | The local index pulse. The period counter measures the time between LINDEX pulses. |
| MASTER | Dig In | The master index pulse. The phase timer measures the time from LINDEX to MINDEX. |
| COMMU | Dig In | The input from the BEMF comparator on the MSC chip. |
| ADVANCE | Dig Out | The output to the MSC chip. |
| $\overline{\text{UNIPOLAR}}$ | Dig Out | An uncommitted DSP output bit that can be used to command the external MSC commutator to switch to unipolar mode. |
| MSCHGAIN | Dig Out | An uncommitted DSP output bit that can be used to command the external MSC commutator to switch gains. |
| $\overline{\text{INT}}$ | Dig O/D | The interrupt output for the DSP. |
| DOUT | Dig Out | An uncommitted output bit that can be programmed by the DSP. |
| DIN1, DIN2 | Dig In | Uncommitted input bit that can be read by the DSP. |

## ELECTRICAL SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS

Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device or affect device reliability.

| PARAMETER | | | RATING |
|---|---|---|---|
| Supply voltage VPA, VPD | | Vdd | -0.3 to 7.0V |
| Pin voltage | Ana In | Vinai | -0.3 to VDD+0.3V |
| | Ana Out | Vinao | -0.3 to VDD+0.3V |
| | Dig In | Vindi | -0.3 to VDD+0.3V |
| | Dig Out | Vindo | -0.3 to VDD+0.3V |
| Storage temperature | | Tstg | -65 to 150°C |
| Lead temperature (10 sec duration) | | Tlead | 0 to 300°C |

### RECOMMENDED OPERATING CONDITIONS

The recommended operating conditions for the device are indicated in the table below. Performance specifications do not apply when the device is operated outside the recommended conditions.

| PARAMETER | | | RATING |
|---|---|---|---|
| Supply voltage | | Vdd | 4.5 to 5.5V |
| Ambient temperature | | Ta | 0 to 70°C |
| Capacitive load on digital outputs | | Cl | 50 pF |
| Analog output load | | | |
| | Cl | | 50 pF |
| | Rl | | 20 kΩ |
| System clock $fc$ = 20 MHz | | | |
| | Freq. tolerance | $fc$ | -0.01 to 0.01% |
| | Pulse width | Twh,Twl | 20 to 30 ns |
| Biasing resistor, Rbias = 56.3 kΩ | | Rbias | -5 to 5% |
| VBGAP tolerance, VBGAP = 2.25V | | VBGAP | -5 to 5% |

## PERFORMANCE SPECIFICATIONS

**SUPPLY CURRENT** (FSTART = 5 kHz, DSP ACTIVE TIME = 25 µs)

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| VPA | Idda | | | | 24 | mA |
| VPD | Idd | | | | 13 | mA |
| VPA, Sleep mode | Iddas | | | | TBD | mA |
| VPD, Sleep mode | Idds | | | | TBD | mA |

**DIGITAL I/O**

| | | | | | |
|---|---|---|---|---|---|
| Digital input | | | | | |
| Vil | | 0.8 | | | V |
| Vih | | | | 2.0 | V |
| Iil,Iih | | | | 1 | µA |
| Digital Output (except $\overline{INT}$) | | | | | |
| Vol | Iol = 2.0 mA | | | 0.4 | V |
| Voh | Ioh = -100 µA | Vdd-.4 | | | V |
| Digital Output ($\overline{INT}$) | | | | | |
| Vol | Iol = 4.0 mA | | | 0.4 | V |

**SERVO D/A CONVERTER**

| | | | | | |
|---|---|---|---|---|---|
| Positive Full-scale voltage Digital=0x1FF | | | SREF+ VBGAP/2 | | V |
| Negative Full-scale voltage Digital=0x200 | | | SREF- VBGAP/2 | | V |
| Resolution | | | 10 | | bits |
| Digital Delay | | | | 4 | µs |
| LSB voltage | | | VBGAP/ 1024 | | V |
| Differential nonlinearity | | | | 1 | LSB |
| Offset | | | | TBD | mV |

## ELECTRICAL SPECIFICATIONS (continued)

### MSC D/A CONVERTER

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Positive Full-scale voltage Digital = 0x1FF | | | MREF+ VBGAP/2 | | V |
| Negative Full-scale voltage Digital = 0x200 | | | MREF- VBGAP/2 | | V |
| Resolution | | | 10 | | bits |
| Digital Delay | | | | 4 | µs |
| LSB voltage | | | | VBGAP/ 1024 | V |
| Differential nonlinearity | | | | 1 | LSB |
| Offset | | | | TBD | mV |

### ADC CONVERTER

| | | | | | |
|---|---|---|---|---|---|
| Positive full-scale input Digital Output = 0x1 FF | | | VBGAP | | V |
| Negative full scale input Digital Output = 0x200 | | | VBGAP/9 | | V |
| Resolution | | | 10 | | bits |
| Conversion time (includes MUX delay) | | | | 2 | µs |
| LSB voltage | | | VBGAP/ 1152 | | V |
| Differential nonlinearity | | | | 1 | LSB |

### AMPLIFIERS

| | | | | | |
|---|---|---|---|---|---|
| Gain | | 50 | | | dB |
| Unit gain bandwidth | | 1 | | | MHz |
| Input offset | | -20 | | 20 | mV |
| Output swing | | .2 | | 3.5 | V |
| Input common mode Range | | 0 | | Vdd | V |
| Settling time to 0.1%full scale step, inverting unity gain | | | | 1.8 | µs |

### MUX

| | | | | | |
|---|---|---|---|---|---|
| On Resistance | | | | 100 | Ω |

**SW1, SW2 SWITCH**

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| On Resistance | | | | 100 | Ω |

**µP SERIAL INTERFACE PORT TIMING**

| | | | | | | |
|---|---|---|---|---|---|---|
| SCLK | | | | | | |
| | Period | TCLK | | 50 | | ns |
| | Low Time | TCKL | | 15 | | ns |
| | High Time | TCKH | | 25 | | ns |
| SDEN | | | | | | |
| | Setup Time | TSENS | | 20 | | ns |
| | Hold Time | TSENH | | 60 | | ns |
| SDATA | | | | | | |
| | Setup Time | TDS | | 5 | | ns |
| | Hold Time | TDH | | 2 | | ns |
| | Read Delay | TPD | CL = 0 to 50 pF | 4 | 60 | ns |
| | Disable Delay | TSENDL | | | 25 | ns |

**µP TRACK ID PORT TIMING**

| | | | | | | |
|---|---|---|---|---|---|---|
| TCK | | | | | | |
| | Period | TCLK | | 20 | | ns |
| | Low Time | TCKL | | 10 | | ns |
| | High Time | TCKH | | 10 | | ns |
| TD | | | | | | |
| | Setup Time | TDS | | 3 | | ns |
| | Hold Time | TDH | | 2 | | ns |

6

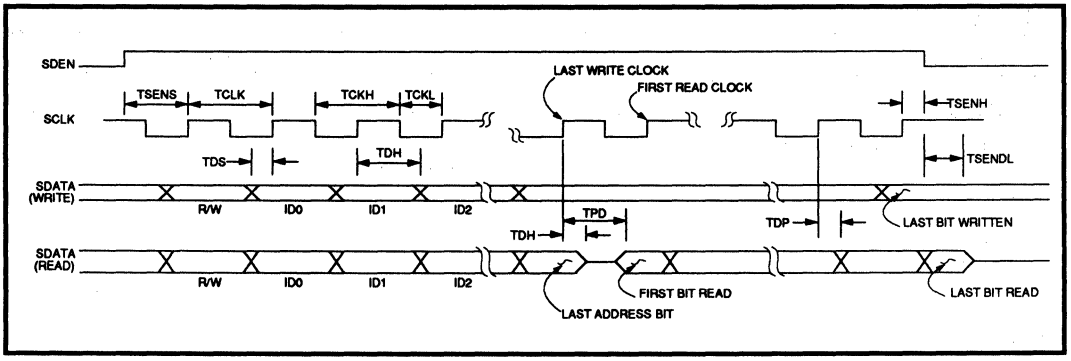



**FIGURE 1: Serial Port Data Transfer Format**

## PROGRAMMER'S DESCRIPTION

This programmer's description of the SEEKER DSP contains a register level description of the DSP that is detailed enough to illustrate each opcode. It also contains a description of each opcode.

### REGISTER LEVEL DESCRIPTION

The DSP consists of an arithmetic unit and an instruction unit. The arithmetic unit consists of a data RAM (DRAM), a shifter, an ALU, and an accumulator. The instruction unit consists of instruction RAM (IRAM) and a program counter. Figure 2 shows the contents of the DSP.

In a one-clock cycle, the DSP is capable of shifting a data word up to ±15 bits and adding it to the accumulator. A 4-cycle multiply is implemented in the multiply and accumulate functions.

### DRAM

The DRAM stores data and coefficients for use by the DSP. The first 11 addresses of the DRAM are memory mapped to on-chip resources. In addition, a lookup command allows the DSP to use portions of DRAM as lookup tables.

### DATA REG AND MULT REG

These registers store the data from the DRAM. This permits the DRAM to perform other operations during a multiply. A STORE or the setup cycle of an MLD or MADD instruction will be executed while a previous MLD or MADD instruction is completing.

### SEQUENCER

This logic block controls the execution of instructions by monitoring the state of the accumulator, the DRAM, and the IRAM. When the resources required by the next instruction are available, the sequencer permits that instruction to execute.

### FLAGS

Certain instructions cause one of the three flags to be updated with the sign bit of the accumulator. The flags are used by the instruction unit during conditional jumps.

### SHIFTER

The shifter shifts the DATA REG word up to ±15 bits in one clock cycle. Unused left hand bits are sign extended and unused right hand bits are zero filled. The shifter has a 24-bit input and output width. The 16-bit word from DATA REG is sign extended 4 bits and padded with 4 zero bits below the LSB before entering the shifter.

### ALU

The ALU is capable of performing an add, subtract, absolute value, XOR, AND, OR, and NEG function. The list of opcodes details the choices.

### ACCUMULATOR

The accumulator is 16 bits with 4 extra LSB bits and 4 extra sign bits. The extra LSB bits minimize the rounding error when partial products are summed during a multiply. The top 4 sign bits are used as an aid in identifying overflow. They also are used in extended precision calculations where they are shifted to the least significant bits of the 16-bit accumulator.

### MULTIPLIER DESCRIPTION

The multiplier returns the top 16 bits of a 16x16 product. An additional 4 LSBs are calculated to improve the truncation accuracy of the product. A RADIX register shifts the multiplicand (pointed to by DR) a certain number of bits to the left.

This multiplier facilitates the use of the two's complement fractional representation. For instance if RADIX is set to zero, each 16 bit number should be thought of as a signed fraction whose full scale value approaches ±1.0. The value of the fraction is calculated by the following equation:

$$\text{value} = -2^{0}b_{15} + 2^{-1}b_{14} + 2^{-2}b_{13} + \ldots + 2^{-15}b_{0}$$

Two such numbers multiplied together will yield an answer in the same format. For instance 0x4000 (0.5) multiplied by 0x4000 (0.5) results in 0x2000 (0.25).

Alternatively, if it is desired to represent numbers whose integer value can approach ±16, set RADIX to 4 and use the following formula:

$$\text{value} = -2^{4}b_{15} + 2^{3}b_{14} + 2^{2}b_{13} + \ldots + 2^{-11}b_{0}$$

With this format, 0x0400 (0.5) multiplied by 0x1800 (3.0) results in 0x0C00 (1.5).

### OPCODE LIST

The following opcodes are implemented in the SEEKER DSP. Parameters in [square] brackets are optional. Parameters enclosed in {curly} brackets form a list from which only one parameter may be chosen. Parameters may be placed in any order within all instructions except MLD and MADD. Opcodes, symbols and all options are case insensitive.

### SHORT/LONG FORM DESCRIPTION

There is instruction memory capacity for 1K by 10-bit short form commands or 500 bytes by 20-bit long form commands. Short form is a 10-bit command which uses relative addressing, whereas long form is a 20-bit command with direct addressing.

DR, MR, and SR are three different pointers to DRAM which are updated with each reference. The assembler will insert short forms of each command if the pointer reference is close enough to its previous reference that relative addressing can be used. Every instruction has a short form except AND, OR, XOR, store commands that use /RET, and jump instructions conditional on F2 or F3. The relative address distance is listed in each opcode description.

If it is desired to force a long or short version of a particular command, an .L or .S suffix can be appended to the command. Alternatively, a short instruction can be forced by specifying a relative address such as '+1' or '+2'.

### ALU INSTRUCTIONS WITH MULTIPLY

MLD *DramDR DramMR* [/F1]

Loads the data register with *DramDR* and the multiplier register with *DramMR* and initiates a multiply and load. The value in *DramDR* is shifted left by RADIX before being multiplied. The MLD instruction requires either 4 or 5 cycles to execute. The 5th cycle is not needed if the previous ALU instruction was an MLD or MADD and was followed by fewer than 4 non-ALU instructions. If F1 is specified, the F1 flag will be updated with the sign bit of the accumulator result. Relative address distance for both DR and MR addresses is +2, -1.

MADD *DramDR DramMR* [/F1]

Loads the data register with *DramDR* and the multiplier register with *DramMR* and initiates a multiply and add. The value in *DramDR* is shifted left by RADIX before being multiplied. The MADD instruction requires either 4 or 5 cycles to execute. The 5th cycle is not needed if the previous ALU instruction was an MLD or MADD and was followed by fewer than 4 non-ALU instructions. If F1 is specified, the F1 flag will be updated with the sign bit of the accumulator result. Relative address distance for both DR and MR addresses is +2, -1.

### MULTIPLIER CONTROL INSTRUCTIONS

RADIX n [/RET]

Sets the amount of left shift "bias" to be performed on DR during MLD and MADD instructions. This command is effectively defining the location of the radix point in the MR word. The RET option will cause a subroutine return. The RADIX command is always short form and is the only short form instruction with a RET option.

### ALU INSTRUCTIONS WITH SHIFT

LDS *DramDR* {/SHL=n, /SHR=n} [/F1] [/ABS]

Loads the contents of *DramDR* in the accumulator after being shifted as specified. Relative address distance is +2, -1. F1 indicates that the F1 flag is to be updated with the sign of the result. ABS indicates that the absolute value of *DramDR* is to be used. If F1 or ABS is specified, the long form of the instruction is used.

LDNS *DramDR* {/SHL=n, /SHR=n} [/F1]

Loads the negative contents of *DramDR* in the accumulator after being shifted as specified. Relative address distance is +2, -1. F1 indicates that the F1 flag is to be updated with the sign of the result. If F1 is specified, the long form of the instruction is used.

ADDS *DramDR* {/SHL=n, /SHR=n} [/ABS] [/F1]

Adds the contents of *DramDR* to the accumulator after being shifted as specified. F1 indicates that the F1 flag is to be updated with the sign of the result. ABS indicates that the absolute value of *DramDR* is to be used. If F1 or ABS is specified, the long form of the instruction is used. Relative address distance is +2, -1.

SUBS *DramDR* {/SHL=n, /SHR=n} [/ABS] [/F1]

Subtracts the contents of *DramDR* to the accumulator after being shifted as specified. F1 indicates that the F1 flag is to be updated with the sign of the result. ABS indicates that the absolute value of *DramDR* is to be used. If F1 or ABS is specified, the long form of the instruction is used. Relative address distance is +2, -1.

XSIGN *DramDR* {/SHL=n, /SHR=n} [/F1]

Multiplies the accumulator by the sign of *DramDR*—if *DramDR* is negative, the accumulator will be inverted. If F1 is specified, the F1 flag is updated with the sign of the accumulator at the end of the command's execution. Relative address distance is +4, -3.

AND *DramDR* [/INV] {/SHL=n, /SHR=n}

ANDs the contents of *DramDR* to the accumulator after being inverted and shifted as specified. There is no short form of this instruction.

OR *DramDR* {/SHL=n, /SHR=n}

ORs the contents of *DramDR* to the accumulator after being shifted as specified. There is no short form of this instruction.

XOR *DramDR* {/SHL=n, /SHR=n}

XORs the contents of *DramDR* to the accumulator after being shifted as specified. There is no short form of this instruction.

### ALU INSTRUCTIONS

LD *DramDR* [/ABS] [/F1]

Loads the contents of *DramDR* in the accumulator. If [ABS] is specified, the absolute value of *DramDR* is loaded. If F1 is specified, the F1 flag is updated with the sign of the accumulator at the end of the command's execution. Relative address distance is +4, -3.

LDN *DramDR* [/F1]

Loads the negative contents of *DramDR* in the accumulator. If F1 is specified, the F1 flag is updated with the sign of the accumulator at the end of the command's execution. Relative address distance is +4, -3.

ADD *DramDR* [/ABS] [/F1]

Adds the contents of *DramDR* to the accumulator. If [ABS] is specified, the absolute value of *DramDR* is added. If F1 is specified, the F1 flag is updated with the sign of the accumulator at the end of the command's execution. Relative address distance is +4, -3.

SUB *DramDR* [/ABS] [/F1]

Subtracts the contents of *DramDR* from the accumulator. If [ABS] is specified, the absolute value of *DramDR* is subtracted. If F1 is specified, the F1 flag is updated with the sign of the accumulator at the end of the command's execution. Relative address distance is +4, -3.

XSIGN *DramDR* [/F1]

Multiplies the accumulator by the sign of *DramDR*—if *DramDR* is negative, the accumulator will be inverted. If F1 is specified, the F1 flag is updated with the sign of the accumulator at the end of the command's execution. Relative address distance is +4, -3.

NOP

An arithmetic command that does nothing.It is sometimes useful before STO and conditional JMP commands. This command is always short.

LKUP

Loads the accumulator with the left justified DRAM value pointed to by the accumulator. The upper 8 bits of the accumulator are used as the DRAM address. The SAT module is always activated during LKUP. This command is always short.

### STORE COMMANDS

STO *DramSR* [/RET] [{/F2, /F3}]

Store the accumulator in *DramSR*. If F2 or F3 is specified, the appropriate flag will be updated with the sign of the value being stored. Relative address distance is +2, -1. If RET is specified, the long form of this instruction is used.

STOSAT *DramSR* [/RET] [{/F2, /F3}]

Store the accumulator in *DramSR* with saturation logic enabled. If F2 or F3 is specified, the appropriate flag will be updated with the sign of the value being stored. Relative address distance is +2, -1. If RET is specified, the long form of this instruction is used.

STOLSW *DramSR* [/RET] [{/F2, /F3}]

Store the least significant word. This command stores the accumulator in *DramSR* and then shifts the sign bits right by 16 bits. The extra LSB bits are cleared. If F2 or F3 is specified, the appropriate flag will be updated with the sign of the value being stored. Relative address distance is +2, -1. If RET is specified, the long form of this instruction is used.

STODR *DramSR* [/RET] [{/F2, /F3}]

Stores the DATA REG contents in *DramSR*. This command permits fast data moves since the data does not have to flow through the accumulator pipeline. If F2 or F3 is specified, the appropriate flag will be updated with the sign of the value being stored. Relative address distance is +2, -1. If RET is specified, the long form of this instruction is used.

### PROGRAM CONTROL

JMP *label:*
An unconditional jump. Relative address distance is +8, -7.

JSUB *label:*
An unconditional subroutine call. This is always a long instruction.

JF *label:* {/F1, /F2, /F3}
Jump if flag is one. Relative address distance is +8, -7. If F2 or F3 is specified, the long form is used.

JFB *label:* {/F1, /F2, /F3}
Jump if flag is zero. Relative address distance is +8, -7. If F2 or F3 is specified, the long form is used.

JALU
A computed jump. The jump address is taken from the bottom 9 bits of the accumulator. This is a short instruction.

STOP
Stops execution of the program. The program restarts on a rising edge of DSPSTART pulse.

### COMMAND SEQUENCING

Although the SEEKER DSP is a pipeline architecture, instruction sequencing is unaffected except in one case.

Commands that depend on accumulator results such as STORE and conditional jump must allow one cycle to occur after the accumulator instruction completes. If the accumulator instruction requires more than one cycle to complete (MLD or MADD), the STORE or conditional jump must be placed one ALU instruction after the accumulator command. This allows the result to propagate into the accumulator before it is stored.

Example 1: Calculate C=A•B and E=A•B+D.

```
MLD   A B    ;load accumulator with A•B
ADD   D      ;add D to accumulator
STO   C      ;store A•B in C
STO   E      ;store A•B+D in E
```

Example 2: Calculate C=A•B and E=A•B+D•F.

```
MLD   A B    ;load accumulator with A•B
MADD  D F    ;add D•F to accumulator
STO   C      ;store A•B in C
NOP          ;NOP is an ALU instruction
STO   E      ;store A•B+D•F in E
```

### CYCLE COUNTING

All instructions execute in one cycle except MLD and MADD instructions which require a setup cycle and 4 ALU cycles. During a multiply, the sequencer will execute up to 4 non-ALU instructions until it encounters another ALU command. Non-ALU commands include JUMP, STORE, and the setup cycle of MLD and MADD instructions. Thus it is often possible to store results and setup the next multiply without consuming clock cycles.

Example 3: Calculate a 2 pole Chebyshev low pass:

$$v_{out} = z^{-1}(v_x + K_3 v_{out})$$

$$v_x = v_x z^{-1} + v_{in} K_1 - v_{out} K_2$$

```
LD    VX        ;(1 clock) load vx
MADD  VIN K1    ;(5 clock) OLDVX + K1•VIN
MADD  VOUTNK2   ;(4 clock) the setup for this
                instruction occurs during the
                previous instruction.
MADD  VOUT K3   ;(4 clock) the setup for this
                instruction occurs during the
                previous instruction.
STO   VX        ;(0 clock) VX=OLDVX +
                K1•VIN + K2•VOUT
LD    VX        ;(1 clock) begin new
                calculation
STO   VOUT      ;(1 clock) VOUT=VX +
                K3•VOUT
```

Thus this biquad requires 16 cycles to execute. Note that NK2 = -K2.

**ASSEMBLER INPUT FILE**

The assembler input file contains both DRAM initialization information and IRAM instructions. A typical structure for the file is:

```
;*******************************sample input file*********************
;sample.asm
;comments extend from ; to end of line
;
.dorg 0                 ;indicates the beginning of a DRAM section which will specify addresses
                        ;beginning with 0. If no value is specified, the addressing will start where the last
                        ;.dorg section ended.

zero:     data 0        ;values can be expressed in decimal
qrtr:     data 0x2000   ;or hex
x2:       data 256
          data
          data          ;DRAM labels are optional
prod:     data 0
adc1:
dac1:     data 0        ;more than one label can refer to the same address
temp:     data jump1    ;a DRAM value can be another DRAM or IRAM label.

.org            ;indicates the beginning of an IRAM section. As in the .dorg case, a value can be
                ;specified to indicate where in the IRAM the code is to be inserted.

lds       qrtr /shl=1   ;load qrtr into accumulator after being shifted by 1 bit to the left
radix     1             ;indicate that multipliers have the radix point 1 bit from left
sto       x2            ;store 0x4000 into x2
madd      adc1 qrtr  /f1 ;multiply adc1 times qrtr times two (due to RADIX), update f1
nop                     ;wait one arith cycle before result is valid for sto or jmp
jf /f1    jump1         ;jump if f1 is one
sto       prod          ;sto prod if positive
jmp       end
jump1:                  ;labels can be on a line by themselves
sto       dac1          ;if neg, send prod to dac1
end:      stop
;*******************************end of sample file*******************
```

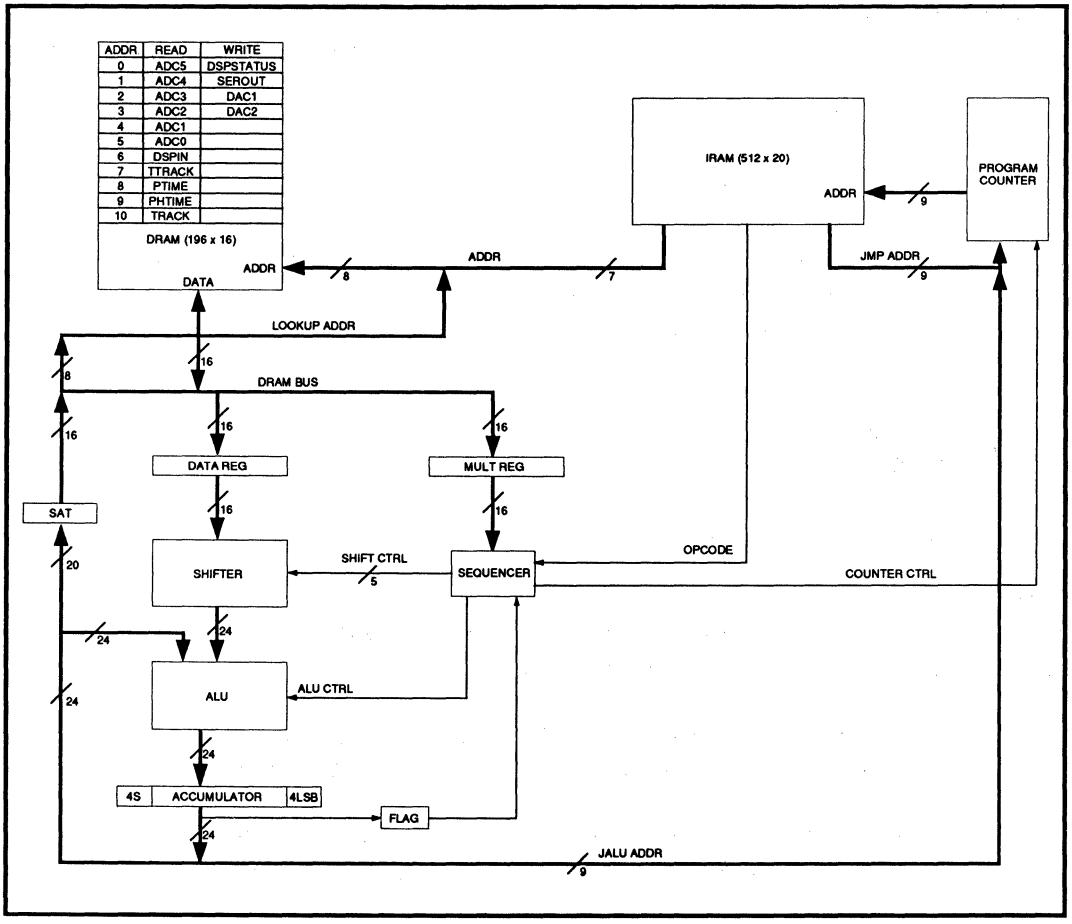
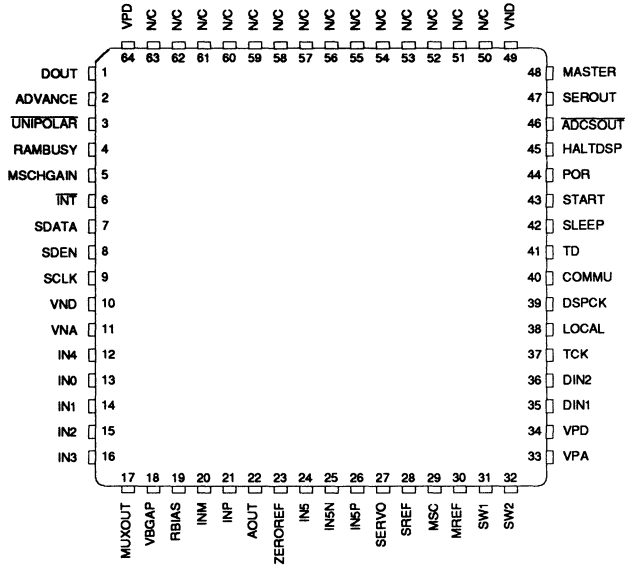



**FIGURE 2: Programmer's Model**

## PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.




**64-Lead TQFP**

6

**Advance Information:** Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.



Silicon Systems, Inc. 14351 Myford Road, Tustin, CA 92680, (714) 573-6000, FAX (714) 573-6914

**Notes:**

Section 7

# HDD SPINDLE MOTOR CONTROL

silicon systems®
A TDK Group Company

# SSI 32M7010
## Hall-Sensorless Motor Speed Control
## Preliminary Data

February 1992

## DESCRIPTION

The (Spindle) Motor Speed Control in conjunction with several external components, provides starting, accelerating, and precise rotational speed regulation functions. Different circuit versions are provided to control 4-, 8-, or 12-pole brushless DC motors without the need for Hall sensors. Control is accomplished via five pins and operation is monitored via two pins. The complete speed regulation control loop is contained in the circuit and the companion microprocessor is only required during start and to monitor status.

Motor speed control is accomplished by measuring the period of each revolution with a 500 kHz clock signal (SYSCLK divided by four). Period resolution is therefore 2 microseconds with the desired period being 8333 counts (16.66 milliseconds, or 3600.144 RPM).

Motor armature position is determined by monitoring the coil voltage of the winding that is not presently being driven by the drivers. The back-emf at the coil in conjunction with the state of the output drivers, indicates armature position. The back emf is compared to a reference (CT) and initiates commutation when the

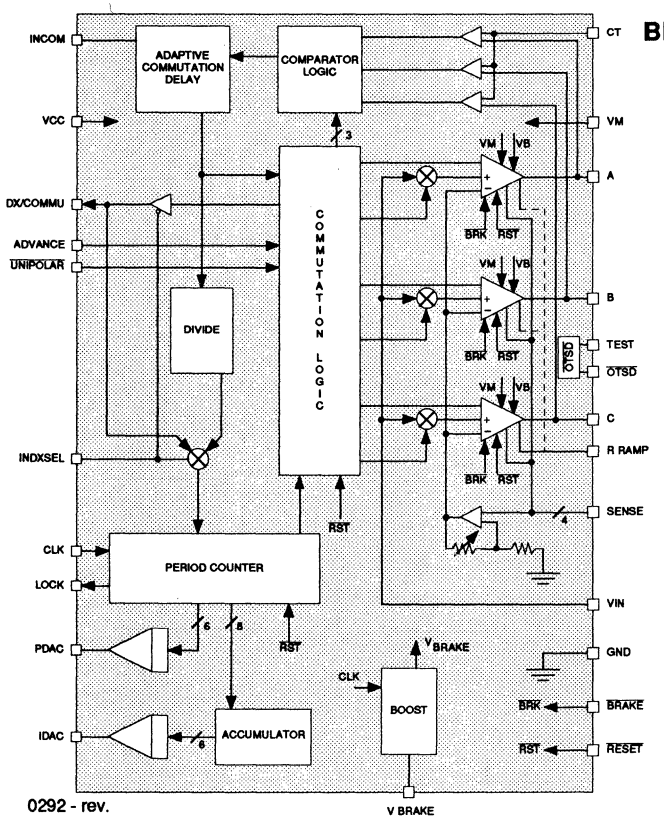
(continued)

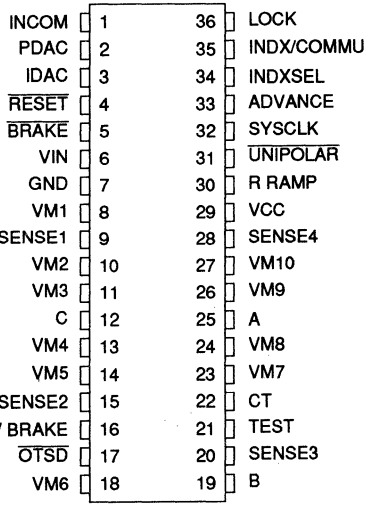
## FEATURES

- **Precise speed control**
- **1 amp peak drivers**
- **No blocking diode**
- **Adaptive commutation delay**
- **Commutation transient suppression**
- **Convenient Retract / Brake Control**

7

## BLOCK DIAGRAM




**36-Pin SOM**
**PIN DIAGRAM**

CAUTION: Use handling procedures necessary for a static sensitive component.

**TABLE 1: Output Driver States**

| STATE | COMMU | PULL DOWNS A | B | C | PULL UP UPA | UPB | UPC |
|---|---|---|---|---|---|---|---|
| 0, (Reset State) | 1 | off | on, (off) | off | on | off | off |
| 1 | 0 | off | off | on | on | off | off |
| 2 | 1 | off | off | on | off | on | off |
| 3 | 0 | on | off | off | off | on | off |
| 4 | 1 | on | off | off | off | off | on |
| 5 | 0 | off | on | off | off | off | on |

## DESCRIPTION (Continued)

appropriate comparison is made. Because the back-emf comparison event occurs prior to the time when optimum commutation should occur, commutation is delayed by a predetermined time after the comparison. The commutation delay is provided by a circuit which measures the interval between comparison events and delays commutation by a time equal to 0.43 of the prior interval. (The delay is set at 0.43 not 0.50 in order to compensate for commutation delays and motor current build-up time.) The circuit is adaptive and will provide the optimum delay for a wide range of motor speeds. Since the commutation of motor coils typically causes transients, the circuit also provides a noise blanking function which prevents response to back-emf comparison events for a period of time equal to 5/7 of the interval (between events) after the comparison event. The commutation delay can be externally modified by ±15% with the INCOM pin. The commutation states are shown in Table 1.

The period counter is loaded with a count of 8333 initially, and the period measurement results in residual counts (ideally zero) in the period counter as it counts down during the index to index time. The residual count is fed to the proportional DAC (5 bits plus sign). When there is no period error the PDAC will output 1/2 full scale (2.25/2 volts) from PDAC, too short a period will output a lower voltage, and too long a period will output a higher voltage, each depending on the amount of period error. When the residual count is within ± 15 counts of zero, the motor status is indicated as "in lock." The lower eight bits of the period counter are fed to an accumulator which adds the present period residue to the previous accumulation thus accomplishing an integrating effect which forces the speed error to zero over time. The upper six bits of the accumulator are fed to the integral DAC whose output is IDAC. Gross period errors will cause PDAC and IDAC to saturate at the appropriate extremes to achieve the maximum corrective control voltage.

The outputs PDAC and IDAC are connected to VIN with an external resistor network. The resistor values are selected to set the required loop response based on motor and system requirements. Input pin VIN is the non-inverting input of a linear transconductance amplifier which uses the lower driver transistor that is presently active per the commutation state as the power driver element. An external resistor is used to sense the current in the drive transistor source (and hence the motor coil current). The voltage across the sense resistor is amplified by a gain stage (Av=8) and fed to the inverting input of the transconductance output stage.

When the speed error is more than 3% slow, 2.25 volts is selected as the control voltage in lieu of VIN. Maximum motor current is limited to a value such that Imotor ≤ 2.25V/ (4 • $R_{SENSE}$).

Four operating conditions are selected via $\overline{BRAKE}$ and $\overline{RESET}$. With $\overline{BRAKE}$ and $\overline{RESET}$ asserted (low), outputs A, B, and C are low impedance to ground, (without current limiting function) and analog circuits are de-biased. This is the "sleep" condition. It also provides dynamic braking to the motor. With $\overline{BRAKE}$ asserted, and $\overline{RESET}$ de-asserted, drivers are low impedance to ground (without current limit function) and the analog circuitry is biased. For $\overline{RESET}$ asserted, $\overline{BRAKE}$ de-asserted, the output drivers are in a high impedance state. This will allow the user to take energy from the back-emf of a spinning motor for retracting heads. Normal operation is given for $\overline{BRAKE}$ and $\overline{RESET}$ de-asserted.

## DESCRIPTION (Continued)

**TABLE 2: Rout Low to SENSE**

| $\overline{\text{BRAKE}}$ | $\overline{\text{RESET}}$ | CONDITION | ANALOG | COUNTERS | A, B, C |
|---|---|---|---|---|---|
| 0 | 0 | SLEEP/BRAKE | OFF | RESET | Rout low to SENSE |
| 0 | 1 | BRAKE | ON | ACTIVE | Rout low to SENSE |
| 1 | 0 | RETRACT | ON | ACTIVE | FLOAT |
| 1 | 1 | RUN | ON | ACTIVE | ACTIVE |

Motor starting is accomplished with a companion microprocessor utilizing ADVANCE, $\overline{\text{RESET}}$ and COMMU. The microprocessor can assert $\overline{\text{RESET}}$ to initialize the commutation counter and then increment the counter with ADVANCE. ADVANCE at logic high excludes internal commutations. COMMU provides feedback to the microprocessor on motor activity.

## PIN DESCRIPTION

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| $\overline{\text{RESET}}$ | I | When asserted low, internal counters and registers are cleared. Refer to Table 2. |
| $\overline{\text{BRAKE}}$ | I | $\overline{\text{BRAKE}}$ is used to provide a delay between the initiation of Fault-induced head retract and motor braking. A capacitor to ground and a resistor to $\overline{\text{RESET}}$ are selected such that 1.2•R•C is equal to the maximum time required for retract. |
| SYSCLK | I | Reference frequency for motor speed measurement. A 2.000 MHz SYSCLK will result in 3600 RPM motor speed for 8-pole motors. SYSCLK can be set to other frequencies to obtain a different rotational speed or operate with motors other than 8-pole configurations (use of an external index signal is only valid for 8-pole motors). |
| INDX/COMMU | I/O | When selected with INDXSEL set high, this pin is used to provide a once-per-revolution indication of rotational position and speed to the circuit. With INDXSEL low, COMMU (the LSB of the commutation counter) is presented as an output. |
| INDXSEL | I | See above. |
| LOCK | O | When the motor period is within ±15 counts of nominal, the motor is indicated as "in lock" with LOCK high. |
| ADVANCE | I | ADVANCE is used to increment the commutation counter. The rising edge of ADVANCE will increment the counter. ADVANCE held high will inhibit internal incrementing of the counter, ADVANCE held low permits the normal operation of commutation from back-emf events. |
| VM 1 - 10 | - | Motor Power Supply. |

## PIN DESCRIPTION (continued)

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| INCOM | I | Adaptive commutator delay test point. |
| PDAC | O | Proportional DAC output pin. The proportional channel output is the lowest 5 bits plus sign of the period measuring counter. The LSB signifies a 2 microsecond period variation for SYSCLK = 2.00 MHz. |
| IDAC | O | Integral DAC output pin. The integral channel output comes from the upper six bits of an eight bit accumulator. The accumulator adds the lower eight bits of the period measurement to the previous value obtained from prior period measurements and accumulations. |
| VIN | I | Control Voltage input pin. The internal driver transistors and internal predriver circuits form a transconductance amplifier which will set motor current in relation to VIN. In conjunction with the SENSE input and the gain of the sense amplifier, transconductance (Gm) will be: Gm = Im/VIN = 1/ (Rs • 8). |
| SENSE1<br>SENSE2<br>SENSE3<br>SENSE4 | I | Current monitoring sense amplifier (high side) input pin. The lower driver transistor current (hence motor current) is sent through a current sensing resistor to monitor motor current. The circuit will control the voltage across this resistor (multiplied by the gain of 8 in the sense amplifier) to match either VIN (during normal operation) or internal 2.25V (during low-speed operation with Av = 4). |
| A, B, C | O | Motor Drive Outputs. These pins provide drive to the motor coils. |
| CT | I | Back-EMF input from motor coil center tap. Input connected to the center tap for sensing generated back-emf voltages. The circuit uses the back-emf voltages to determie rotor position and effect commutation. |
| VCC | - | 5V power pin. |
| V BRAKE | O | External capacitor to store charge for driver circuitry. The stored charge is used by the lower drivers in fault conditions to achieve dynamic braking. |
| GND | - | Ground connection. GND is the low side input to the current SENSE amplifier and care should be taken to see that GND and the low side of the sense resistor are at the same potential. |
| $\overline{\text{OTSD}}$ | O | Indicates over temperature condition. |
| R RAMP | I | External resistor. Sets DV/DT for lower driver turn-off. DV/DT is approximately 4E 10 • R RAMP. |
| $\overline{\text{UNIPOLAR}}$ | I | Select line for Unipolar or Bipolar mode. |

## ELECTRICAL SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS

(Exposure to conditions in excess of the conditions given below may result in permanent damage or affect device reliability.)

| PARAMETER | | RATING |
|---|---|---|
| Supply Voltage | VCC | -0.3 to 7V |
| | VM | -0.3 to 15V |
| Digital Inputs/Outputs | SYSCLK, ADVANCE INDXSEL, INDX/COMMU, LOCK | -0.3 to VCC +0.3V |
| Analog I/O | PDAC, IDAC, VIN | -0.3 to VCC +0.3V |
| Motor Interface Voltage | CT, A, B, C, $\overline{\text{BRAKE}}$, SENSE, $\overline{\text{RESET}}$ | -0.3 to 20V |
| Motor Interface Current | A, B, C, VM, SENSE | -1.0 to +1.0A |
| Storage Temperature, Tstg | | -65 to 150°C |
| Lead Temperature, Tlead | | 300°C |

### RECOMMENDED OPERATING CONDITIONS

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Supply Voltage | VCC | | 4.75 | | 5.25 | V |
| | VM | | 4.75 | | 5.25 | V |
| Supply Current | ICC | | 1.0 | | 10.0 | mA |
| | ICC, Sleep Mode | | 0.05 | | 1.0 | mA |
| | IVM | | 0 | | 0.75 | A |
| | IVM, Sleep Mode | | 0.1 | | 1.5 | mA |
| Ambient Temperature | Ta | | 0 | | 70 | °C |
| Capacitive Load Digital I/O | Cl | | 0 | | 100 | pF |
| Resistive Load PROP, INTEGRAL | Rla | | 5000 | | | Ω |
| Capacitive Load PROP, INTEGRAL | Cla | | 0 | | 40 | pF |

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## ELECTRICAL SPECIFICATIONS (Continued)

### DIGITAL INPUTS

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| Fmax, SYSCLK | | | | 4.5 | MHz |
| Twh, Twl, SYSCLK width high or low | | 40 | | | ns |
| External Index, INDX/COMMU (as input) Pulse Width | | 200 | | | ns |
| Input Leakage, INDX/COMMU | | | | 10 | µA |
| Input Leakage, others | | | | 1 | µA |
| Vil (EXTINDX, SYSCLK, ADVANCE, INDXSEL) | | | | 0.8 | V |
| Vih (inputs above) | | 2.0 | | | V |
| Vil ($\overline{\text{RESET}}$, $\overline{\text{BRAKE}}$) | VBRAKE ≥ 4.5V | | | 0.8 | V |
| Vih ($\overline{\text{RESET}}$, $\overline{\text{BRAKE}}$) | VBRAKE ≥ 4.5V | 2.0 | | | V |

### PROPORTIONAL (PDAC), INTEGRAL (IDAC) OUTPUTS

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| Output Voltage | Iout ≤ 0.1 mA<br>VCC = 5.0 V | 0 | | 2.25V ±5% | V |
| DAC Step Size | VCC = 5.0V | 0.32 | | 0.39 | V |
| Output Impedance | 0.5V ≤V out <2.0V<br>Iout = 0.10 mA | | | 200 | Ω |
| Kp, Porportional Gain | | 0.70 | | 0.85 | V/rad/s |
| Ki, Integral Gain | | 10.48 | | 12.75 | V/rad |

### DIGITAL OUTPUTS, LOCK, INDX/COMMU

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| Voh | Iout = -100 µA | 2.4 | | | V |
| Vol | Iout = 2.0 mA | | | 0.4 | V |
| Tdts, Time delay to tri-state output | INDXSEL high to high impedance on INDX/COMMU | 10 | | 100 | ns |
| Tdoe, Time delay to enable as output pin | INDXSEL low to drive state | 10 | | 100 | ns |

## ELECTRICAL SPECIFICATIONS (Continued)

**VIN**

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| Input Voltage | | 0 | | 2.25 | V |
| Input Current | 0 ≤ Vin < 2.5V | -1 | | +1 | µA |

**OUTPUTS A, B, C**

| | | | | | |
|---|---|---|---|---|---|
| Routup | Output in high state VM = 4.75V | 0.05 | | 1.0 | Ω |
| Routlow | Output driving low, VM = 4.75V | 0.05 | | 1.0 | Ω |

**SENSE**

| | | | | | |
|---|---|---|---|---|---|
| Vin, SENSE | Normal operation | 0.0 | | 0.4 | V |
| | Low speed operation | 0.0 | | 0.8 | V |
| Iin, SENSE | 0.0 ≤ Vin < 1.0V | -10 | | +10 | µA |
| Cin | | | | 20 | pF |
| Transconductance gain from VIN to motor current (steady-state) will be given by: G = Imotor/VIN = 1/Rsense • 8, for rotational speeds greater than 3490 RPM. | | | | | |

**CT**

| | | | | | |
|---|---|---|---|---|---|
| Rin | -0.3V ≤Vin < 15V | 30K | | | Ω |
| Cin | | | | 10 | pF |

**V BRAKE**

| | | | | | |
|---|---|---|---|---|---|
| Ibst (run) | VCC = 4.75V | | | 100 | µA |
| Ibst (float) | VCC ≤ 0.5V | | | 10 | µA |
| Ibst (brake) | VCC ≤ 0.5V | | | 10 | µA |

**OPERATING REQUIREMENTS**

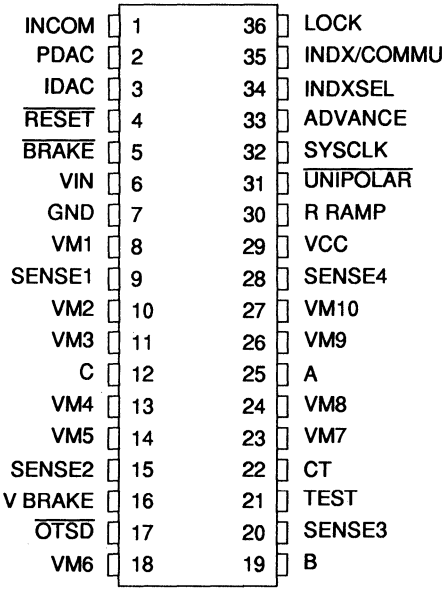
| | | | | | |
|---|---|---|---|---|---|
| LOCK Indication Range | SYSCLK = 2.000 MHz, 8-pole | 3593.5 | | 3606.5 | RPM |
| Speed Resolution | | -.012 | | +0.012 | % |

7

# SSI 32M7010
# Hall-Sensorless
# Motor Speed Control

## PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.




**36-Pin SOM**

## ORDERING INFORMATION

| PART DESCRIPTION | ORDER NO. | PKG. MARK |
|---|---|---|
| SSI 32M7010, Hall-Sensorless Motor Speed Control | | |
| 36-Pin SOM | 32M7010-CM | 32M7010 |

**Preliminary Data:** Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.



Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 573-6000, FAX (714) 573-6914

silicon systems®
A TDK Group Company

# SSI 32M7011
## Hall-Sensorless Motor Speed Commutator
## Advance Information

December 1991

## DESCRIPTION

The (Spindle) Motor Commutator in conjunction with a companion microcontroller, provides starting, accelerating, precise rotational speed regulation functions, coasting (for retract), and dynamic brake. The circuit can be used with 4-, 8-, or 12-pole, 3 phase, brushless DC motors without the need for Hall sensors.

The commutator determines motor armature position by monitoring the coil voltage of the winding that is not presently being driven by the drivers. The back-emf at the coil in conjunction with the state of the output drivers, indicates armature position. The back emf is compared to a reference (CT) and initiates commutation when the appropriate comparison is made.

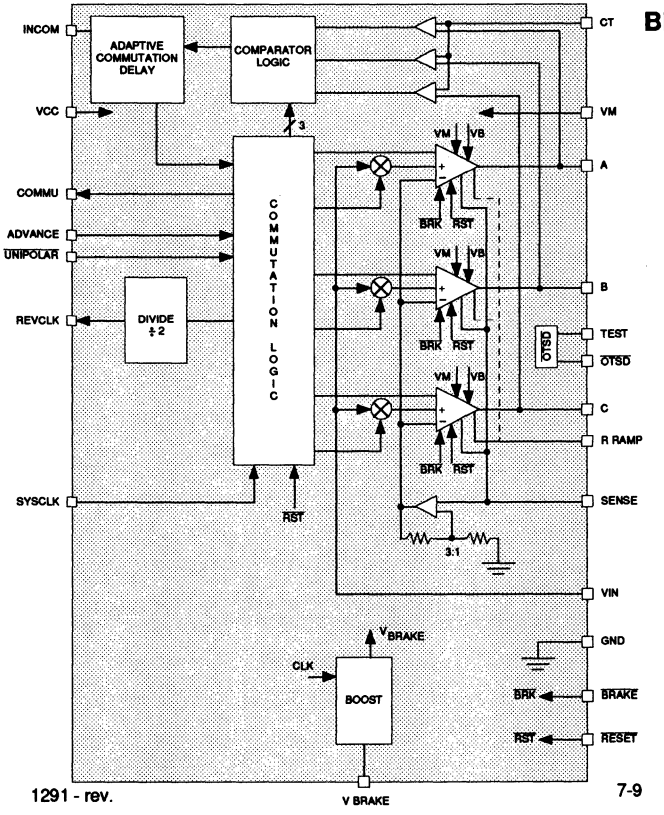
(continued)

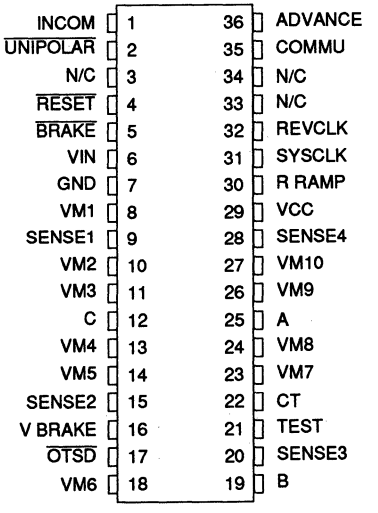
## FEATURES

- **Optimum commutation without external components**
- **Retract coast and brake modes supported**
- **1Ω FET drivers**
- **Commutation without Hall sensors**
- **Reduced DV/DT on commutation - no snubber networks required**
- **No blocking diode required**
- **Immune to brown outs and load transients**

7

## BLOCK DIAGRAM




**36-Pin SOM**

**PIN DIAGRAM**

CAUTION: Use handling procedures necessary for a static sensitive component.

## DESCRIPTION (Continued)

Because the back-emf comparison event occurs prior to the time when optimum commutation should occur, commutation is delayed by a predetermined time after the comparison. The commutation delay is provided by a circuit which measures the interval between prior comparison events and delays commutation by a time equal to 0.43 of the prior interval. (The delay is set at 0.43 not 0.50 in order to compensate for commutation delays and motor current build-up time.) The circuit is adaptive and will provide the optimum delay for a wide range of motor speeds. Since the commutation of motor current typically causes transients, the circuit also provides a noise blanking function which prevents response to back-emf comparison events for a period of time equal to 0.71 of the interval (between events) after the comparison event. The commutation delay can be externally modified by ±15% with the INCOM pin. The commutation states are shown in Table 1.

Input pin VIN is the non-inverting input of a linear transconductance amplifier which uses the lower driver transistor that is presently active per the commutation state as the power driver element. An external resistor is used to sense the current in the drive transistor source (and hence the motor coil current). The voltage across the sense resistor is amplified by a gain stage (Av=4) and fed to the inverting input of the transconductance output stage. Input voltage VIN must be generated from external means that use either REVCLK or other external rotational index indicators to measure rotational speed.

Four operating conditions are selected via $\overline{\text{BRAKE}}$ and $\overline{\text{RESET}}$. With $\overline{\text{BRAKE}}$ and $\overline{\text{RESET}}$ asserted (low), outputs A, B, and C are low impedance to ground, (without current limiting function) and analog circuits are de-biased. This is the "sleep" condition. It also provides dynamic braking to the motor. With $\overline{\text{BRAKE}}$ asserted, and $\overline{\text{RESET}}$ de-asserted, drivers are low impedance to ground (without current limit function) and the analog circuitry is biased. For $\overline{\text{RESET}}$ asserted, $\overline{\text{BRAKE}}$ de-asserted, the output drivers are in a high impedance state. This will allow the user to take energy from the back-emf of a spinning motor for retracting heads. Normal operation is given for $\overline{\text{BRAKE}}$ and $\overline{\text{RESET}}$ de-asserted.

Note that circuit utilizes NMOS driver transistors and does not require a Schottky blocking diode to prevent current flow from the spinning motor to the power supply. During RETRACT conditions, the motor is isolated from VM.

**TABLE 1: Output Driver States**

| STATE | COMMU | PULL DOWNS A | B | C | PULL UP UPA | UPB | UPC |
|---|---|---|---|---|---|---|---|
| 0, (Reset State) | 1 | off | on, (off) | off | on | off | off |
| 1 | 0 | off | off | on | on | off | off |
| 2 | 1 | off | off | on | off | on | off |
| 3 | 0 | on | off | off | off | on | off |
| 4 | 1 | on | off | off | off | off | on |
| 5 | 0 | off | on | off | off | off | on |

**TABLE 2: Rout Low to SENSE**

| $\overline{\text{BRAKE}}$ | $\overline{\text{RESET}}$ | CONDITION | ANALOG | COUNTERS | A, B, C |
|---|---|---|---|---|---|
| 0 | 0 | SLEEP/BRAKE | OFF | RESET | Rout low to SENSE |
| 0 | 1 | BRAKE | ON | ACTIVE | Rout low to SENSE |
| 1 | 0 | RETRACT | ON | ACTIVE | FLOAT |
| 1 | 1 | RUN | ON | ACTIVE | ACTIVE |

Motor starting is accomplished with a companion microprocessor utilizing ADVANCE, $\overline{\text{RESET}}$ and COMMU. The microprocessor can assert $\overline{\text{RESET}}$ to initialize the commutation counter and then increment the counter with ADVANCE. ADVANCE at logic high excludes internal commutations. COMMU provides feedback to the microprocessor on motor activity.

## PIN DESCRIPTION

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| $\overline{\text{RESET}}$ | I | Refer to Table 2. |
| $\overline{\text{BRAKE}}$ | I | $\overline{\text{BRAKE}}$ is used to provide a delay between the initiation of Fault-induced head retract and motor braking. A capacitor to ground and a resistor to $\overline{\text{RESET}}$ are selected such that 1.2•R•C is equal to the maximum time required for retract. |
| SYSCLK | I | 2.0 MHz clock input signal. |
| COMMU | O | COMMU is the LSB of the commutation counter. |
| REVCLK | O | Indicates 1 revolution of 4-pole motor, 1/2 revolution of 8-pole, and 1/3 revolution of 12-pole motor. |
| ADVANCE | I | ADVANCE is used to increment the commutation counter. The rising edge of ADVANCE will increment the counter. ADVANCE held high will inhibit internal incrementing of the counter, ADVANCE held low permits the normal commutation due to back-emf events. |
| VM 1 - 10 | Power | Motor Power Supply. |
| INCOM | I | Adaptive commutator delay trim. Generally a no-connect. |
| VIN | I | Control Voltage input pin. The internal driver transistors and internal predriver circuits form a transconductance amplifier which will set motor current in relation to VIN. In conjunction with the SENSE input and the gain of the sense amplifier, transconductance (Gm) will be Gm = Im/VIN = 1/ (Rs•4). The voltage at VIN must be controlled by external circuitry to accomplish speed control. |
| SENSE1<br>SENSE2<br>SENSE3<br>SENSE4 | Power | Current monitoring sense amplifier (high side) input pin. The lower driver transistor current (hence motor current) is sent through a current sensing resistor to monitor motor current. The circuit will control the voltage across this resistor (multiplied by the gain of 4 in the sense amplifier) to match VIN. |
| A, B, C | O | Motor Drive Outputs. These pins provide drive to the motor coils. |
| CT | I | Back-EMF input from motor coil center tap. Input connected to the center tap for sensing generated back-emf voltages. The circuit uses the back-emf voltages to determine rotor position and effect commutation. 3 equal value resistors from A, B, and C attached to CT will suffice to synthesize a center-tap potential on three terminal motors. 4 terminal motors should use this terminal. |
| VCC | Power | 5-volt power pin. |

## PIN DESCRIPTION (continued)

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| V BRAKE | O | External capacitor to store charge for driver circuitry. The stored charge is used by the lower drivers in fault conditions to achieve dynamic braking. |
| GND | - | Ground connection. GND is the low side input to the current SENSE amplifier and care should be taken to see that GND and the low side of the sense resistor are at the same potential. |
| $\overline{\text{OTSD}}$ | O | Indicates over temperature condition and forces drivers off. Operation after cool down is restored by asserting ADVANCE. |
| R RAMP | I | External resistor. Sets DV/DT for lower driver turn-off. DV/DT is approximately $25 \cdot \frac{10^9}{\text{RRAMP}}$ (Volts / Second) |
| $\overline{\text{UNIPOLAR}}$ | I | Select line for Unipolar or Bipolar mode. $\overline{\text{UNIPOLAR}}$ = low will de-activate upper drivers. Note: for BRAKE and SLEEP modes user must guarantee that external Unipolar driver transistor(s) do not conflict with lower driver transistors on circuit. |
| TEST | I/O | No connect, leave open circuited. |

## ELECTRICAL SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS

(Exposure to conditions in excess of the conditions given below may result in permanent damage or affect device reliability.)

| PARAMETER | SYMBOL | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply Voltage | VCC | -0.3 | 7 | V |
| | VM | -0.3 | 7 | V |
| Digital Inputs/Outputs | SYSCLK, ADVANCE COMMU, REVCLK | -0.3 | VCC +0.3 | V |
| Analog I/O | VIN, RRAMP, INCOM, TEST | -0.3 | VCC +0.3 | V |
| Motor Interface Voltage | CT, A, B, C, $\overline{\text{BRAKE}}$, SENSE, $\overline{\text{RESET}}$ | -0.3 | 20 | V |
| Motor Interface Current | A, B, C, VM, SENSE | -1.0 | +1.0 | A |
| Storage Temperature, Tstg | | -65 | 150 | °C |
| Lead Temperature, Tlead | | - | 300 | °C |

## ELECTRICAL SPECIFICATIONS

### RECOMMENDED OPERATING CONDITIONS

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Supply Voltage | VCC | | 4.75 | | 5.25 | V |
| | VM | | 4.75 | | 5.25 | V |
| Supply Current | ICC | | 1.0 | | 10.0 | mA |
| | ICC, Sleep Mode | | 0.05 | | 1.0 | mA |
| | IVM | | 0 | | 0.75 | A |
| | IVM, Sleep Mode | | 0 | | 1.5 | mA |
| Ambient Temperature | Ta | | 0 | | 70 | °C |
| Capacitive Load Digital I/O | Cl | | 0 | | 100 | pF |

### DIGITAL INPUTS

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| Fmax, SYSCLK | | 1.0 | 2.0 | 4.5 | MHz |
| Twh, Twl, SYSCLK width high or low | | 40 | | | ns |
| Advance Pulse Width | | 200 | | | ns |
| Input Leakage, others | | | | 1 | µA |
| Vil (SYSCLK, ADVANCE) | | | | 0.8 | V |
| Vih (inputs above) | | 2.0 | | | V |
| Vil ($\overline{\text{RESET}}$, $\overline{\text{BRAKE}}$) | VBRAKE ≥ 4.5V | | | 0.8 | V |
| Vih ($\overline{\text{RESET}}$, $\overline{\text{BRAKE}}$) | VBRAKE ≥ 4.5V | 2.0 | | | V |

### DIGITAL OUTPUTS, COMMU, REVCLK

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| Voh | Iout = -100 µA | 2.4 | | | V |
| Vol | Iout = 2.0 mA | | | 0.4 | V |

### VIN

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| Input Voltage | | 0 | | 2.25 | V |
| Input Current | 0 ≤ Vin < 2.5V | -1 | | +1 | µA |

## ELECTRICAL SPECIFICATIONS (Continued)

### OUTPUTS A, B, C

| PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|
| Routup | Output in high state<br>VM = 4.75V | 0.05 | | 1.0 | Ω |
| Routlow | Output driving low,<br>VM = 4.75V | 0.05 | | 1.0 | Ω |

### SENSE

| | | | | | |
|---|---|---|---|---|---|
| Vin, SENSE | Normal operation | 0.0 | | 0.5 | V |
| Iin, SENSE | 0.0 ≤ Vin < 1.0V | -10 | | +10 | µA |
| Cin | | | | 20 | pF |
| Transconductance gain from VIN to motor current (steady-state) will be given by:<br>G = Imotor/VIN = 1/Rsense • 4. | | | | | |

### CT

| | | | | | |
|---|---|---|---|---|---|
| Rin | -0.3V ≤Vin < 15V | 30K | | | Ω |
| Cin | | | | 10 | pF |

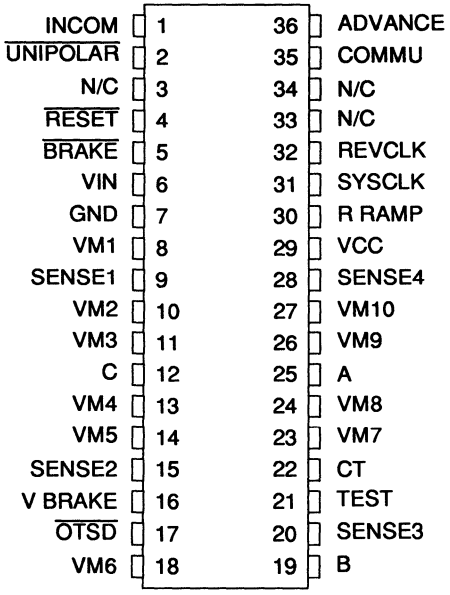
### V BRAKE

| | | | | | |
|---|---|---|---|---|---|
| Ibst (run) | VCC = 4.75V | | | 100 | µA |
| Ibst (float) | VCC ≤ 0.5V | | 25 | 100 | µA |
| Ibst (brake) | VCC ≤ 0.5V | | 3 | 10 | µA |

## PACKAGE PIN DESIGNATIONS

(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.




**36-Pin SOM**

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**Advance Information:** Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.



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**Notes:**

Section 8

# HDD CONTROLLER/ INTERFACE

silicon systems®
A TDK Group Company

# SSI 32C9001
## PC-AT Combo Controller With Reed Solomon, 48 Mbit/s

**Advance Information**

January 1993

## DESCRIPTION

The SSI 32C9001 is an advanced CMOS VLSI device which integrates major portions of the hardware needed to build an ATA disk drive. The circuitry of the SSI 32C9001 includes a complete ATA interface, an advanced buffer manager, a high performance disk formatter and an 88 bit Reed-Solomon ECC with fast "on-the-fly" hardware correction. The SSI 32C9001 provides maximum performance while minimizing micro controller intervention.

The SSI 32C9001 is capable of concurrent transfers of up to 48 megabits per second on the disk interface and 6 megawords (16 bit transfers) per second across the ATA bus. In addition, on-the-fly error corrections and micro controller accesses to the buffer memory will not degrade the throughput during transfers.

The high level of integration within the SSI 32C9001 represents a major reduction in parts count. When the SSI 32C9001 ATA Controller is combined with the

(continued)

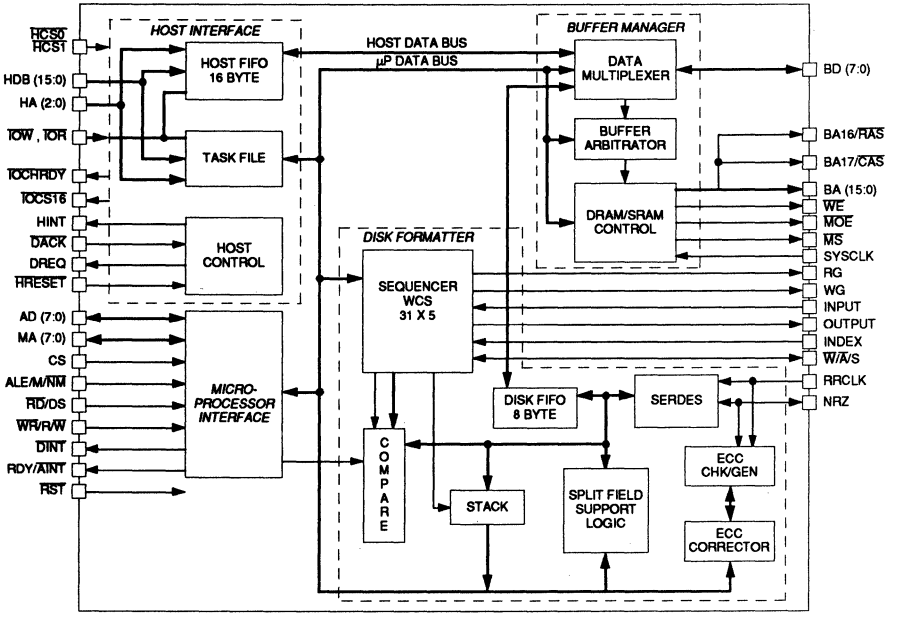
## FEATURES

- **ATA Interface**
  - **Single Chip PC AT Controller**
  - **Full ANSI ATA Compliance**
  - **Direct PC Bus connection with on board 24 mA drivers**
  - **PC transfers to 6 megawords/second**
  - **Supports PIO, DMA and EISA Class B Demand DMA**
  - **Logic for daisy chaining 2 drives**
  - **Automatic command decoding of write, write buffer and format commands.**
  - **Automatic updates of the host task file registers in both Cyl/Hd/Sec and LBA modes**
  - **Hardware added to provide Multi-Sector data transfers without microprocessor intervention**

(continued)

8

## BLOCK DIAGRAM



# SSI 32C9001
# PC-AT Combo Controller
# With Reed Solomon, 48 Mbit/s

## DESCRIPTION (continued)

SSI 32R2010 Read/Write device, the SSI 32P3000 Pulse Detector, the SSI 32D5391 Data Synchronizer with 1,7 ENDEC, the 32H4631 Servo and Motor Speed Controller, an appropriate micro controller and memory, a complete, cost efficient, high performance intelligent drive solution is created.

## FEATURES (continued)

- Automatic Host Interrupt and Busy for multiple sector transfers
- 16 byte FIFO to improve performance
- Power Down I/O pins

- **Buffer Manager**
  - Direct support of DRAM or SRAM
  - SRAM: up to 256k bytes of memory with throughput to 20 megabytes per second
  - DRAM: up to 1 megabyte of memory with throughput to 17.78 megabytes per second
  - Programmable memory timing
  - Supports page mode DRAM access
  - Programmable page mode burst length
  - Programmable DRAM refresh period
  - Buffer RAM segmentation with flexible segment sizes from 256 bytes to 1 megabyte
  - Dedicated host, disk and microprocessor address pointers
  - Buffer Streaming with internal buffer protection circuit providing buffer integrity
  - Multiple sector host transfers
- **Disk Formatter**
  - NRZ Data Rates to 48 megabits per second
  - Automatic multi-sector transfer
  - Header or microprocessor based split data field support
  - Advanced sequencer organized in 31 x 5 bytes
  - Advanced branch and interrupt logic
  - 88-bit Reed Solomon ECC with "on-the-fly" fast hardware correction circuitry
  - Capable of correcting up to four 10-bit symbols in error
  - Guaranteed to correct one 31-bit burst or two 11-bit bursts
  - Hardware on-the-fly correction of either an 11- or 31-bit single burst error within a quarter sector time
  - Detects up to one 51-bit burst or three 11-bit bursts
- **Microprocessor Interface**
  - Supports both multiplexed or non-multiplexed microprocessors

Separate host and disk interrupts

- **Other Features**
  - Internal power down mode
  - Available in 100-pin QFP or TQFP

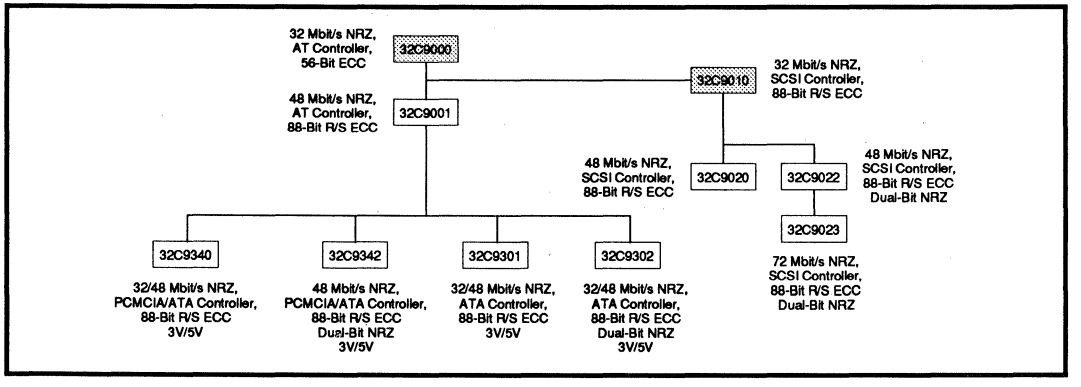



**FIGURE 1: Silicon Systems' Disk Controller Chip Hierarchy**

## FUNCTIONAL DESCRIPTION

The SSI 32C9001 contains the following four major functional blocks:

- Microprocessor Interface
- ATA Interface
- Disk Formatter
- Buffer Manager

The Microprocessor Interface allows the local microprocessor access to all of the SSI 32C9001 internal control registers and any location within the buffer memory. The microprocessor, by writing and reading the internal registers, can control all activities of the SSI 32C9001. The microprocessor can elect to perform host and/or disk operations directly, or it can enable the advanced features of the SSI 32C9001 which can perform these operations automatically.

The ATA Interface block handles all PC AT bus activities. The ATA interface includes 24 mA drivers allowing for direct connection of the SSI 32C9001 to the PC AT bus. The ATA interface block is highly automated, capable of performing multiple block transfers without micro controller involvement. The ATA block interfaces directly with the Buffer Manager via an internal speed matching FIFO. This FIFO, the bandwidth capabilities of the Buffer Manager, plus the advanced features of the ATA Interface guarantee sustained full speed transfers across the PC AT bus.

The Disk Formatter performs the serialization and deserialization of data. It provides all of the necessary functions to control track formatting, header search, and the reading and writing of data. The heart of the Disk Formatter is an advanced programmable sequencer. The sequencer can contain 31 instructions, each of which is 5 bytes (40 bits) in width. The width of the instructions allows for sophisticated branching techniques which increase the flexibility and power of the sequencer. The disk interface can be configured through a wide range of capabilities, allowing the SSI 32C9001 to interface with nearly any read/write channel. This allows the user of the SSI 32C9001 to select the read/write channel best suited to the device. Of course, by selecting the SSI 32C9001 controller and the SSI 32D5391 Data Synchronizer with 1,7 ENDEC, you are guaranteed a problem free interface.

Within the Disk Formatter are the ECC generator/checker and ECC corrector. The generator/checker provides the ability to generate or check a 32 bit ECC for headers and an 88 bit Reed Solomon code for data. If the checker detects an error using the 88 bit Reed Solomon code, the syndrome information is transferred into the corrector. The corrector then performs the necessary operations to determine if the error was correctable and, if it was correctable, the corrector interfaces directly with the buffer controller and performs the correction automatically. The corrector performs its correction within one quarter of a sector. This guarantees that the corrector will always be available to correct the next sector if necessary.

As its name implies, the Buffer Manager manages the data buffer of the controller. The Buffer Manager can support either SRAM or DRAM. When configured to operate with DRAM, the Buffer Manager automatically performs necessary refresh cycles. The buffer manager creates all of the necessary timing and control signals for a wide range of memory types and speeds. Besides interfacing with the buffer memory, the Buffer Manager interfaces with the ATA Interface block, the Disk Formatter block, the ECC corrector and the microprocessor. If more than one of these devices requires access to the buffer memory, the Buffer Manager arbitrates the requests automatically. The Buffer Manager of the SSI 32C9001 can sustain ATA operations at the rate of 6 megawords per second, Disk Formatter operations at 48 megabits per second (6 megabytes per second) and still has sufficient band width left to handle on-the-fly ECC corrections and microprocessor accesses without degrading performance on any of the interfaces.

## PIN DESCRIPTION

The following convention is used in the pin description:

- (I) denotes an input
- (O) denotes an output
- (I/O) denotes a bidirectional signal
- (Z) denotes a tri-state output
- (OD) denotes an open drain output

Active low signals are denoted by a bar on top of the signal name and dual function pins are denoted with a slash between the two signals — A9/$\overline{HCS1}$.

### GENERAL

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| VDD | | POWER SUPPLY PIN, VCC |
| GND | | GROUND |

### HOST INTERFACE

| | | |
|---|---|---|
| A(2:0) | I | HOST ADDRESS LINES. The Host Address lines A(2:0) are used to access the various PC/AT control/status, and data registers. |
| A9/$\overline{HCS1}$ | I | HOST ADDRESS LINE 9/HOST CHIP SELECT 1. This is a multiplexed input pin. When Register 48H-bit 3 is reset this input is HOST ADDRESS LINE 9; when the bit is set this input is HOST CHIP SELECT 1. |
| $\overline{HCS0}$ | I | HOST CHIP SELECT 0. This pin selects access to the control, status and data registers. |
| $\overline{IOCS16}$ | OD | 16 BIT DATA TRANSFER. An open drain active low output that indicates that a 16-bit transfer is active. |
| HINT | O, Z | HOST INTERRUPT. Asserted active high to indicate to the Host that the controller needs attention. |
| $\overline{IOCHRDY}$ | O, Z | I/O CHANNEL READY. Active low, this signal is asserted to extend the host's I/O cycle. |
| DREQ | O, Z | DMA REQUEST. The active high DMA Request signal is used during DMA transfer between the Host and the controller to initiate DMA Transfers. |
| $\overline{DACK}$ | I | DMA ACKNOWLEDGE. This active low signal is used during DMA to complete the DMA handshake for data transfer between the host and the controller. |
| $\overline{IOR}$ | I | INPUT READ SELECT. This active low pin is asserted by the Host during a Host read operation. When asserted with $\overline{HCS0}$, $\overline{HCS1}$, or DACK, data from the device is enabled onto the host data bus. |
| $\overline{IOW}$ | I | INPUT WRITE SELECT. Asserted active low by the Host during a Host write operation. When asserted with $\overline{HCS0}$, $\overline{HCS1}$, or DACK, data from the host data bus is strobed into the device. |

**HOST INTERFACE** (continued)

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| $\overline{\text{HRESET}}$ | I | HOST RESET. This active low signal stops all commands in progress and initializes the control/status registers — see Design Guide for Register Reset conditions. This signal can also "wake up" the device while it is in power down mode. |
| HDB (15:0) | I/O | HOST DATA BUS. These bits are used for word transfers between the Buffer Memory and the Host; note that for transferring commands, status or ECC only bits (7:0) are used. |

**DISK INTERFACE**

| | | |
|---|---|---|
| INDEX | I | INDEX. This input is a pulse that occurs once per revolution and defines the start of a physical track. |
| INPUT | I | DISK SEQUENCER INPUT. A general purpose input pin used to synchronize the disk sequence to an external event. |
| OUTPUT | O | DISK SEQUENCER OUTPUT. This pin is controlled by bit 2 of the Control Field of the disk sequencer. |
| $\overline{\text{WAM}}$/<br>$\overline{\text{AMD}}$/<br>SEC | I/O | WRITE ADDRESS MARK/ADDRESS MARK DETECT/SECTOR. This pin is configured to operate in Hard or Soft Sector mode by initializing the Disk Formatter Mode Control Register: 4FH, bit 1. In the hard sector mode it is used as the sector input — a pulse on this pin indicates the beginning of a sector.<br>In the soft sector mode, an active low output is asserted when formatting to allow writing of an address mark. When reading, an active low input indicates an address mark was detected. The device powers up in soft sector mode. |
| RG | O | READ GATE. This active high output enables the reading of the disk. It is asserted by the sequencer Control Field bits 5 and 6. It is automatically deasserted at the end of the CRC or ECC. |
| WG | O | WRITE GATE. This active high output enables writing onto the disk. It is asserted and deasserted by the sequencer Control Field bits 5 and 6. |
| RRCLK | I | READ/REFERENCE CLOCK. This pin is used in conjunction with the NRZ pin to clock data in and out of the SSI 32C9001 device. This input must be glitch-free to ensure correct operation of the chip. |
| NRZ | I/O | NON RETURN TO ZERO. This signal is the serial read data input from the disk drive when the read gate signal is asserted; it is the write data output to the disk drive when the write gate signal is asserted. |

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## PIN DESCRIPTION (continued)

### MICROPROCESSOR INTERFACE

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| $\overline{RST}$ | I | RESET. An asserted active low input generates a component reset that holds the internal registers of the SSI 32C9001 at reset, stops all operations within the chip, and deasserts all output signals. All input/output signals and Host outputs are set to the high-Z state. |
| ALE/$\overline{M}$/NM | I | ADDRESS LATCH ENABLE/MULTIPLEXED/NON-MULTIPLEXED ADDRESS SELECT. When tied high, the microprocessor interface is configured as non-multiplexed. When driven low, the microprocessor interface is configured as multiplexed. In this case this pin functions as the address latch enable, and the MA(7:0) pins are the demultiplexed address outputs. |
| CS | I | CHIP SELECT. This signal must be asserted high for all microprocessor accesses to the registers of this chip. |
| $\overline{WR}$/R/$\overline{W}$ | I | WRITE STROBE/READ/WRITE. In the Multiplexed address/data bus mode, when an active low signal is present with CS signal asserted high, the data on the AD0:7 is written to the internal registers.<br><br>In the Non-Multiplexed address/data bus mode, this signal acts as the R/$\overline{W}$ signal. A high on this input along with the $\overline{RD}$/DS signal asserted and the CS signal asserted high indicates a read operation. A low on this input along with the $\overline{RD}$/DS signal asserted and the CS signal asserted high indicates a write operation. See table below. |

| CS | $\overline{WR}$/R/$\overline{W}$ | $\overline{RD}$/DS | Mux/Non-Mux | Action |
|---|---|---|---|---|
| High | Low | High | Intel Multiplexed | Write to internal registers. |
| High | High | Low | Intel Multiplexed | Read from internal registers. |
| High | Low | High | Motorola Multiplexed | Write to internal registers. |
| High | Low | Low | Non-Multiplexed | Write to internal registers. |
| High | High | High | Motorola Multiplexed | Read from internal registers. |
| High | High | Low | Non-Multiplexed | Read from internal registers. |
| Low | X | X | M or N | No action. |

Note: X denotes don't care.

| | | |
|---|---|---|
| $\overline{RD}$/DS | I | READ STROBE/DATA STROBE. In the Multiplexed address data bus mode, when an active low signal is present with CS signal high, internal registers will be accessed.<br><br>In the Non-Multiplexed address data mode, this signal acts as the DS signal. A high on R/$\overline{W}$, with the CS and DS signals asserted, indicates a read operation. A low on the R/$\overline{W}$ signal, with the DS and the CS symbols asserted, indicates a write operation to the internal registers. Note: DS is active high in multiplexed mode, active low in non-multiplexed. |

**MICROPROCESSOR INTERFACE** (continued)

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| $\overline{DINT}$ | O, OD | INTERRUPT. This signal is an interrupt line to the microprocesor. It is the combined interrupt line of the disk side and host side interrupts when pin RDY/$\overline{AINT}$ is programmed as ready; otherwise, it only signals the occurrence of disk side interrupt events. This signal is programmable for either a push-pull or open-drain output circuit. This signal powers up as an open drain output. May be programmed as active high or low; reset state is active low. |
| AD(7:0) | I/O | ADDRESS/DATA BUS. When configured in the Multiplexed address data mode, these lines are multiplexed, bidirectional data path to the microprocessor. During the beginning of the memory cycle the bus captures the low order byte of the microprocessor address. These lines provide communication with the controller device's internal registers and the buffer memory.<br>When configured in the Non-Multiplexed Microprocessors mode, these lines are bidirectional data lines only. |
| MA(7:0) | I/O | MICROPROCESSOR ADDRESS BUS. This 8-bit output bus is the AD(7:0) bus latched by the ALE pin during the address phase of a Multiplexed address data type microprocessor cycle. These signals are the address input when used with a non-multiplexed bus microprocessor. |
| READY/$\overline{AINT}$ | O | READY. When this signal is deasserted low, the microprocessor inserts wait states to allow time for the chip to respond to the access. Wait states are programmed by Buffer Mode Control Register — 53H: bits 7-6. |
| | O, OD | $\overline{AINT}$: AT BUS INTERRUPT. This signal is asserted when the controller is requesting microprocessor service from the AT host bus side. This signal is programmable for either a push-pull or open-drain output circuit. This signal powers up as the READY signal. $\overline{AINT}$ may be programmed as active high or low; reset state is active low. |

**BUFFER MANAGER INTERFACE**

| | | |
|---|---|---|
| BA(15:0) | O | BUFFER MEMORY ADDRESS LINES 0:15. These sixteen outputs provide address lines for the dynamic memory or static memory chips used to implement the buffer memory. |
| BA16/RAS | O | BUFFER MEMORY ADDRESS 16. In SRAM mode, this pin generates the address A16 for direct connection to a Static RAM address line 16.<br>ROW ADDRESS STROBE. This active low output signal is generated to strobe the row — high order — address into the dynamic RAMs. It is intended to be directly tied to the RAMs input control pin. |
| BA17/CAS | O | BUFFER MEMORY ADDRESS 17. In SRAM mode, this pin generates the address A17 for direct connection to a Static RAM address line 17.<br>COLUMN ADDRESS STROBE: This output signal is generated to strobe the column — low order address — into the dynamic RAM devices. |

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## PIN DESCRIPTION (continued)

### MICROPROCESSOR INTERFACE (continued)

| | | |
|---|---|---|
| BD(7:0) | I/O | BUFFER MEMORY DATA BUS. These eight signals are bits 7-0 of the 8-bit parallel data lines to/from the buffer memory. Note that BD6 is used to select between the Intel- and Motorola-style microprocessor interfaces. If BD6 is externally pulled up when $\overline{RST}$ is asserted, Intel mode is used; if BD6 is externally pulled down when $\overline{RST}$ is asserted, Motorola mode is used. |
| $\overline{MOE}$ | O | MEMORY OUTPUT ENABLE. This active low output controls the enabling of data onto the data bus by the dynamic RAMs or to indicate when a buffer memory read is active in SRAM mode. |
| $\overline{WE}$ | O | WRITE ENABLE. This active low output signal is used to strobe the data into the RAMs from the Data bus. For both buffer memory applications, this line is tied directly to the SRAM or DRAM control pin. |
| SYSCLK | I | SYSTEM CLOCK. This signal is used to synchronize the buffer RAM access, including the generation of memory address lines, write enable WE, and memory output enable MOE. In power down mode, this signal is shut off from the internal logic and hence buffer memory access is inhibited. |
| $\overline{MS}$ | O | MEMORY SELECT. This signal is asserted low when there is a read or write access to the buffer RAM. The timing of the $\overline{MS}$ pin follows that of the address pins. This signal is used to deselect the buffer RAM when not in use so that power can be saved. |

## ELECTRICAL SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS

Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC operating characteristics.

| PARAMETER | RATING |
|---|---|
| Power Supply Voltage, VCC | 7V |
| Ambient Temperature | 0 to 70 °C |
| Storage Temperature | -65 to 150 °C |
| Power Dissipation | 750 mW |
| Input, Output pins | -0.5 to VCC+0.5V |

### ELECTRICAL CHARACTERISTICS

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| VCC Power Supply Voltage | | 4.5 | | 5.5 | V |
| ICC Supply Current | | | | 50 | mA |
| ICCS Supply Current | Note 1 | | | 250 | µA |
| VIL Input Low Voltage | except RESET pin | -0.5 | | 0.8 | V |
| VIH Input High Voltage | except RESET pin | 2.0 | | VCC+0.5 | V |

**ELECTRICAL CHARACTERISTICS** (continued)

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| VIL Input Low Voltage | Reset Pin | -0.5 | | 1.7 | V |
| VIH Input High Voltage | Reset Pin | 2.5 | | VCC+0.5 | V |
| VOL Output Low Voltage IOL = 2 mA | Note 2 | | | 0.4 | V |
| VOL Output Low Voltage IOL = 24 mA | Note 3 | | | 0.5 | V |
| VOH Output High Voltage IOH = -400 µA | | 2.4 | | | V |
| IL Input Leakage Current 0 < VIN < VCC | | -10 | | 10 | µA |
| CIN Input Capacitance | | | | 10 | pF |
| COUT Output Capacitance | | | | 10 | pF |

Note: (1) Synchronization and Clock Control Register, 7FH: bits 3 and 4 set. RRCLK and SYSCLK internally inhibited.

(2) All interface pins except Host Interface pins.

(3) Host Interface pins.

**MULTIPLEXED BUS MICROPROCESSOR INTERFACE TIMING PARAMETERS (Figures 2 through 5)**

| | | | | | | |
|---|---|---|---|---|---|---|
| Ta | Ale Width | | 20 | | | ns |
| Tma | Address valid to MA0:7 valid | | | | 30 | ns |
| Tr | $\overline{RD}$ Width | | 80 | | | ns |
| As | Address Valid to ALE ↓ | | 5 | | | ns |
| Ah | ALE ↓ to Address Invalid | | 10 | | | ns |
| Cs | CS Valid to RD ↓ or DS ↑ | | 20 | | | ns |
| Ch | $\overline{RD}$ ↑ or DS ↓ to CS ↓ | | 0 | | | ns |
| Tda | $\overline{RD}$ ↓ or DS ↑ to Read Data Valid | | | | 60 | ns |
| Tds | DS width | | 80 | | | ns |
| Tdh | $\overline{RD}$ ↑ to Read Data Invalid | | 0 | | 25 | ns |
| Tsrw | R/$\overline{W}$ valid to DS ↑ | | 20 | | | ns |
| Thrw | DS ↓ to R/W Invalid | | 20 | | | ns |
| Tdrdy | $\overline{RD}$ ↓ to READY ↓ (Intel) or DS ↑ to READY ↓ (Motorola) | | | | 30 | ns |
| Wds | Write data valid to $\overline{WR}$ ↑ or DS ↓ | | 40 | | | ns |
| Wdh | $\overline{WR}$ ↑ or DS ↓ to write data invalid | | 10 | | | ns |
| Note: | ↑ indicates rising edge | ↓ indicates falling edge | | | | |

8

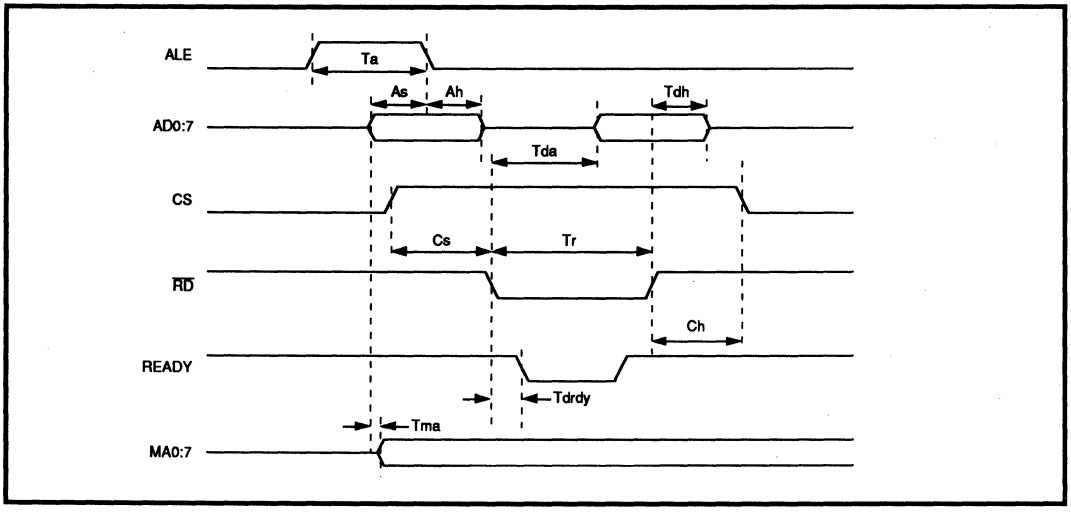


**FIGURE 2: Intel Register Read Timing**

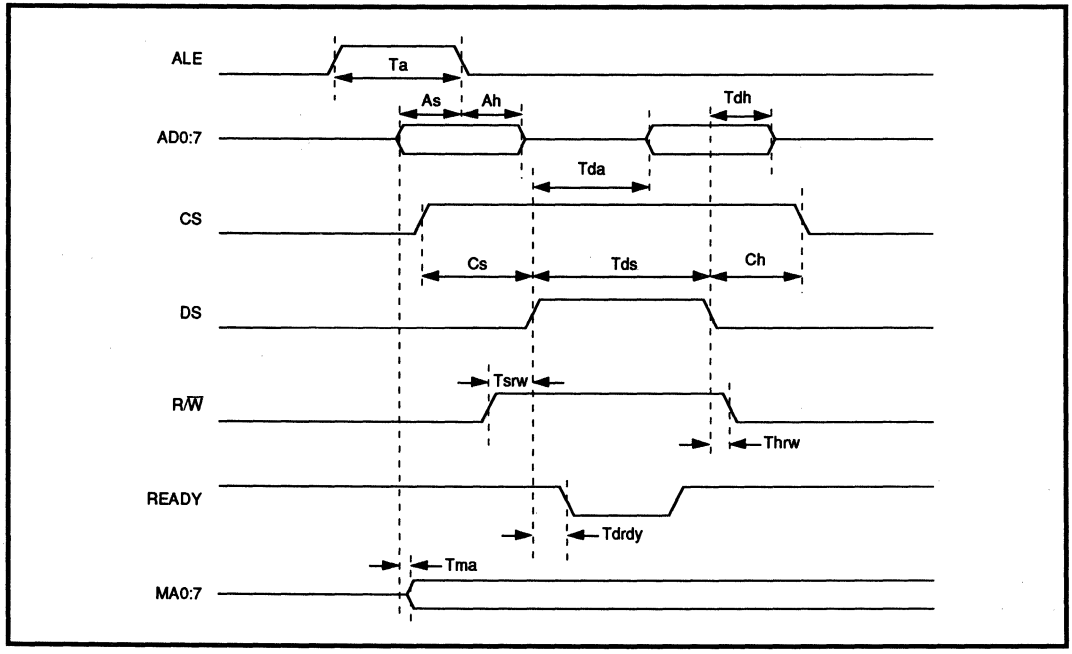


**FIGURE 3: Motorola Register Multiplexed Read Timing**

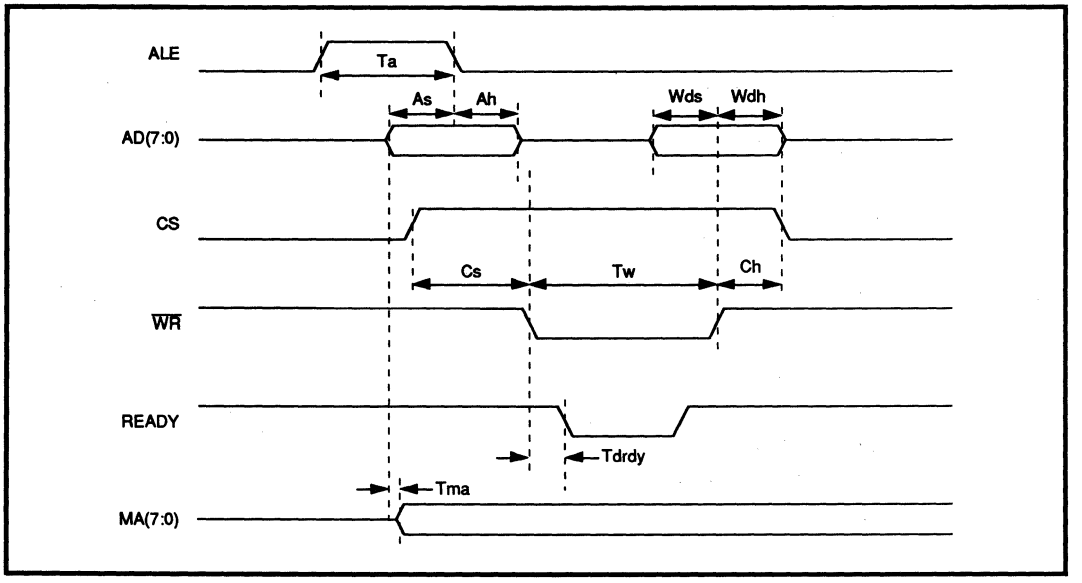


**FIGURE 4: Intel Register Multiplexed Write Timing**



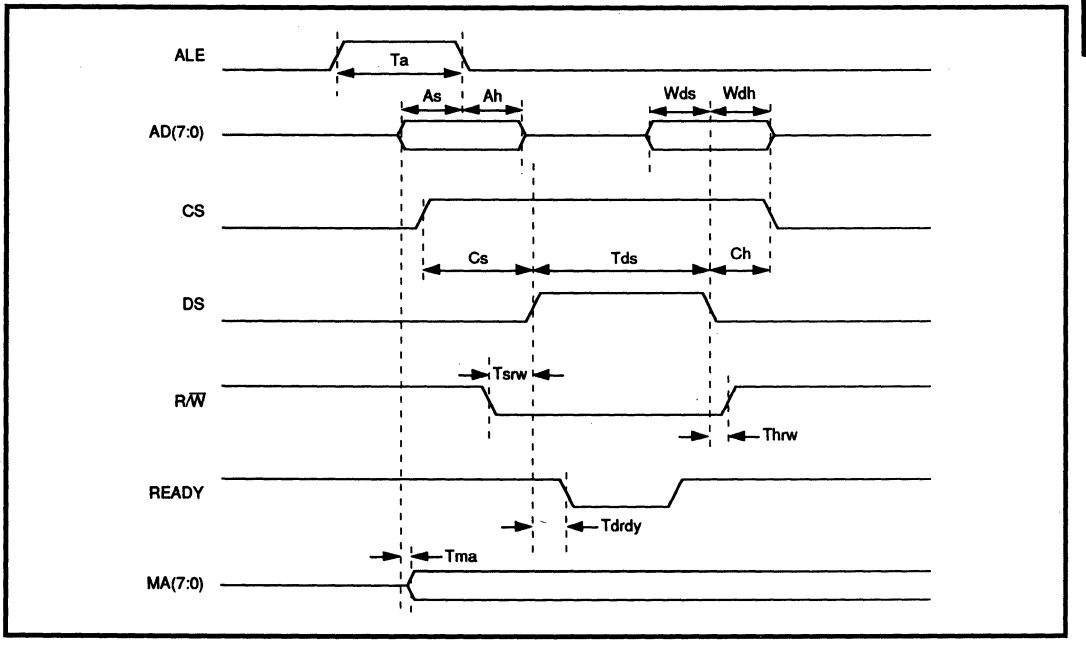


**FIGURE 5: Motorola Register Multiplexed Write Timing**

## ELECTRICAL SPECIFICATIONS (continued)

### NON-MULTIPLEXED BUS MICROPROCESSOR INTERFACE TIMINGS (Figure 6)

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| Tmas | MA(7:0) valid to DS ↓ | | 5 | | | ns |
| Tmah | DS ↑ to MA(7:0) invalid | | 5 | | | ns |
| Cs | CS valid to DS ↓ | | 20 | | | ns |
| Ch | DS ↑ to CS ↓ | | 0 | | | ns |
| Tda | DS ↓ to read data valid | | | | 60 | ns |
| Tds | DS width | | 80 | | | ns |
| Tdh | DS ↑ to read data invalid | | 0 | | 25 | ns |
| Tsrw | R/$\overline{W}$ valid to DS ↓ | | 20 | | | ns |
| Thrw | DS ↑ to R/$\overline{W}$ invalid | | 20 | | | ns |
| Tdrdy | DS ↓ to READY ↓ (Motorola) Note 3 | | | | 30 | ns |
| Wds | Write data valid to R/$\overline{W}$ ↑ or DS ↑ | | 40 | | | ns |
| Wdh | R/$\overline{W}$ ↑ or DS ↑ to write data invalid | | 10 | | | ns |

Note 1: ↑ indicates rising edge ↓ indicates falling edge

Note 2: Loading capacitor = 30pF

Note 3: Ready is not shown and is not used by Motorola processors. Timing provided for information only.

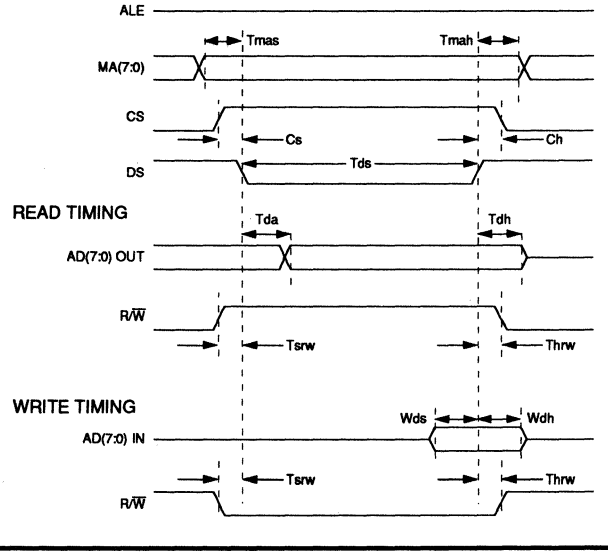


**FIGURE 6: Non-Multiplexed Bus Timing Diagrams**

**DISK READ/WRITE TIMING (Figures 7 and 8)**

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| T | RRCLK | | 20.8 | | | ns |
| T/2 | RRCLK high/low time | | 8.3 | | | ns |
| Tr = Tf | RRCLK rise and fall time | | 0 | | 2 | ns |
| Ds | NRZ in valid to RRCLK ↑ | | 3 | | | ns |
| Dh | RRCLK ↑ to NRZ in invalid | | 3 | | | ns |
| As* | AMD valid to RRCLK ↑ | | 3 | | | ns |
| Dv | RRCLK ↑ to NRZ out | | 3 | | 15 | ns |
| Wv* | RRCLK ↑ to WAM out | | 3 | | 15 | ns |
| Note: | ↑ indicates rising edge | ↓ indicates falling edge | | | | |
| | * These specifications are only applicable in the Soft Sector mode. | | | | | |

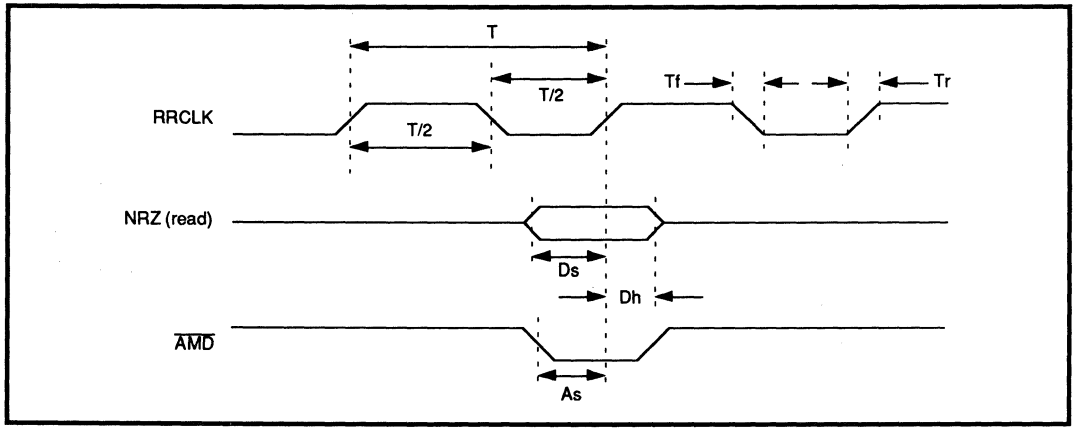


**FIGURE 7: Disk Read Timing**

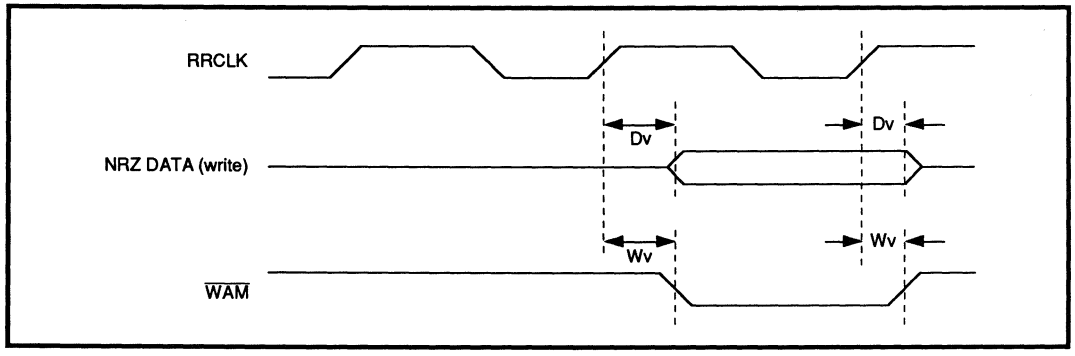


**FIGURE 8: Disk Write Timing**

## ELECTRICAL SPECIFICATIONS (continued)

**BUFFER MEMORY READ/WRITE TIMING PARAMETERS (Figures 9 through 13)**

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| T | SYSCLK period | | 25 | | | ns |
| T/2 | SYSCLK high/low time | | 10 | | | ns |
| Tav | SYSCLK / to address valid | Note 1 | | | 18 | ns |
| Tmsv | SYSCLK / to $\overline{MS}$\ | Notes 1, 6 | | | 18 | ns |
| Tmsh | SYSCLK / to $\overline{MS}$/ | Note 1 | | | 18 | ns |
| Tmv | SYSCLK / to $\overline{MOE}$\ | Note 1 | | | 18 | ns |
| Tmh | SYSCLK / to $\overline{MOE}$/ | Note 1 | | | 18 | ns |
| Twv | SYSCLK / to $\overline{WE}$\ | Note 1 | | | 18 | ns |
| Twh | SYSCLK / to $\overline{WE}$/ | Note 1 | | | 18 | ns |
| Tdov | SYSCLK to data out valid | Note 1 | | | 18 | ns |
| Tdoh | SYSCLK to data out invalid | Note 1 | | | 18 | ns |
| Tdis | Data in valid to $\overline{MOE}$ / (SRAM) | | 5 | | | ns |
| | Data in valid to $\overline{CAS}$ / (DRAM) | | 5 | | | ns |
| Tdih | $\overline{MOE}$ ↑ to data in valid (SRAM) | | 0 | | | ns |
| | $\overline{CAS}$ ↑ to data in valid (DRAM) | | 0 | | | ns |
| Trv | SYSCLK / to $\overline{RAS}$\ | Note 1 | | | 18 | ns |
| Trh | SYSCLK / to $\overline{RAS}$/ | Note 1 | | | 18 | ns |
| Trav | SYSCLK to row address valid | Note 1 | | | 18 | ns |
| Trah | SYSCLK / to row address invalid | Note 1 | | | 18 | ns |
| Tcv | SYSCLK / to $\overline{CAS}$\ | Note 1 | | | 18 | ns |
| Tch | SYSCLK / to $\overline{CAS}$/ | Note 1 | | | 18 | ns |
| Tcav | SYSCLK / to column address valid | Note 1 | | | 18 | ns |
| Tcah | SYSCLK / to column address invalid | | 0 | | | ns |

**BUFFER MEMORY READ/WRITE TIMING PARAMETERS (Figures 9 through 13)** (continued)

| PARAMETER | | CONDITIONS | MIN | UNIT |
|---|---|---|---|---|
| Trwl | $\overline{RAS}$\ to $\overline{RAS}$/ | Notes 2, 3 | ((RWL + 3)•T)-2 | ns |
| Trwh | $\overline{RAS}$/ to $\overline{RAS}$\ | Notes 2, 4 | ((RWH + 1)•T)-2 | ns |
| Tcwl | $\overline{CAS}$\ to $\overline{CAS}$/ | Note 2 | ((CWL + 1)•T)-2 | ns |
| Tcwl | $\overline{CAS}$/ to $\overline{CAS}$\ | Notes 2, 5 | ((CWL + 1)•T)-2 | ns |

Note: Loading capacitance = 30 pF

Note 1: The measured delay for any of the signal indicated by this note will not vary from the measured delay of any other signal indicated by this note by more than ±1 ns.

Note 2: RWL, RWH, CWL and CWH are fields in the Buffer Manager Timing Control Register (54H). Each is a two bit field which can contain a value of 0, 1, 2, or 3. These values determine the minimum number of SYSCLK periods (T) for the associated signal width.

Note 3: The minimum width value of Trwl will be generated for refresh cycles and for any buffer memeory access cycle except when multiple page mode accesses are performed. When multiple page mdoe accesses are performed, the width of the $\overline{RAS}$ low pulse is extended until the end of the last $\overline{CAS}$ low cycle.

Note 4: The minumum value of Trwh will be generated whenever the Buffer Manager determines that a buffer request is pending at the ocmpletion of the current memory cycle and a page mode access can not be used either because page mode operation is not enabled or the needed location is not within the current page.

Note 5: The minumum value of Tcwh will be generated only between consecutive page mode accesses.

Note 6: $\overline{MS}$ will rise only if the Buffer Manager determines that no additional requests for buffer access are pending. If the Buffer Manager determines that another access is to be Made, $\overline{MS}$ is kept low between the accesses for improved speed.

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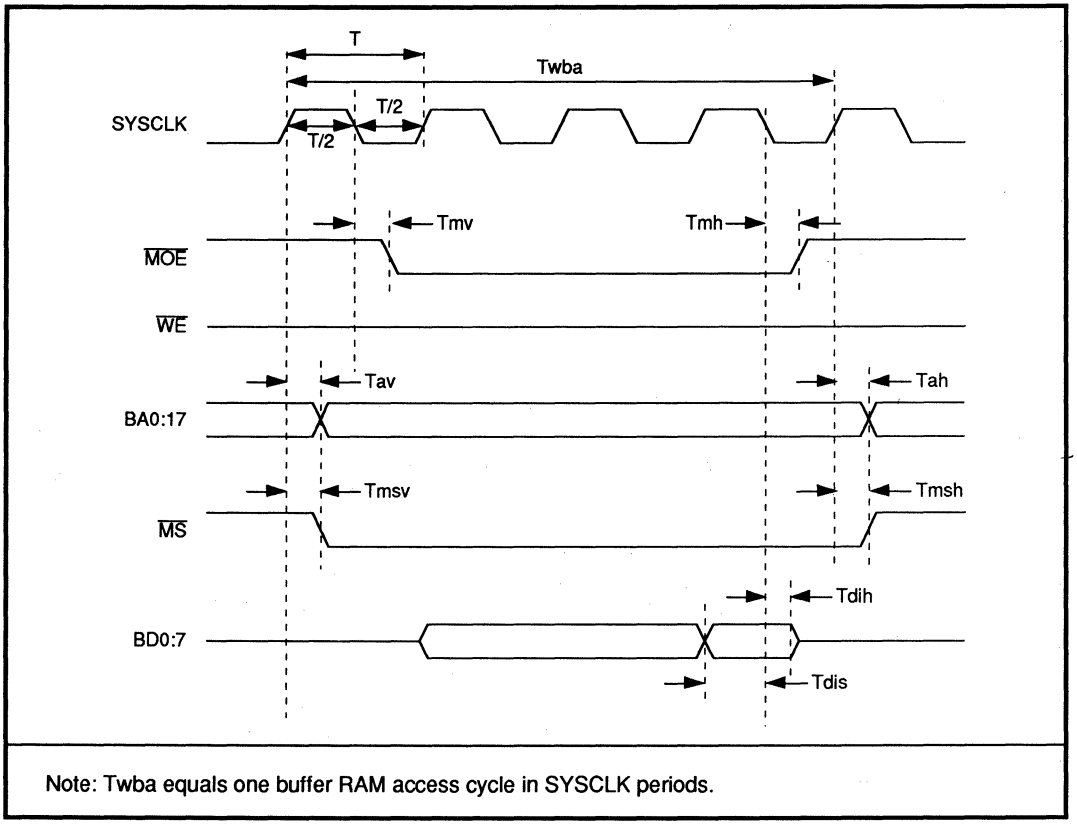
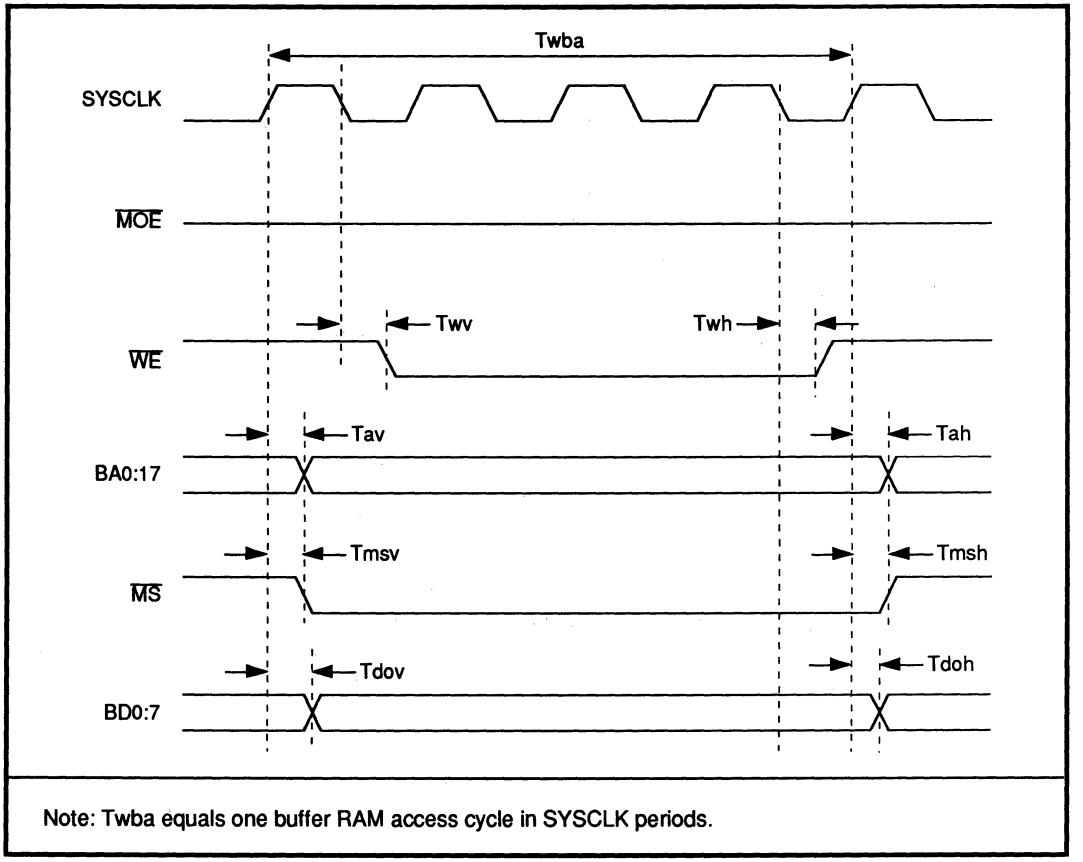



Note: Twba equals one buffer RAM access cycle in SYSCLK periods.

**FIGURE 9: SRAM Read Timing**




Note: Twba equals one buffer RAM access cycle in SYSCLK periods.

**FIGURE 10: SRAM Write Timing**

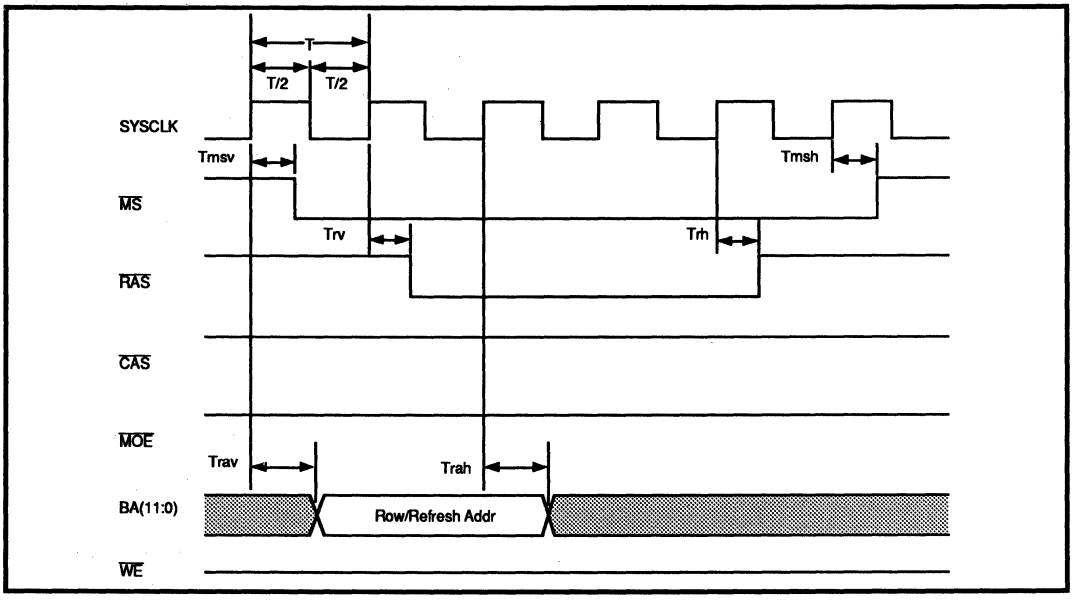



**FIGURE 11: DRAM Timing, Refresh Cycle (Shown with WRL = 0)**

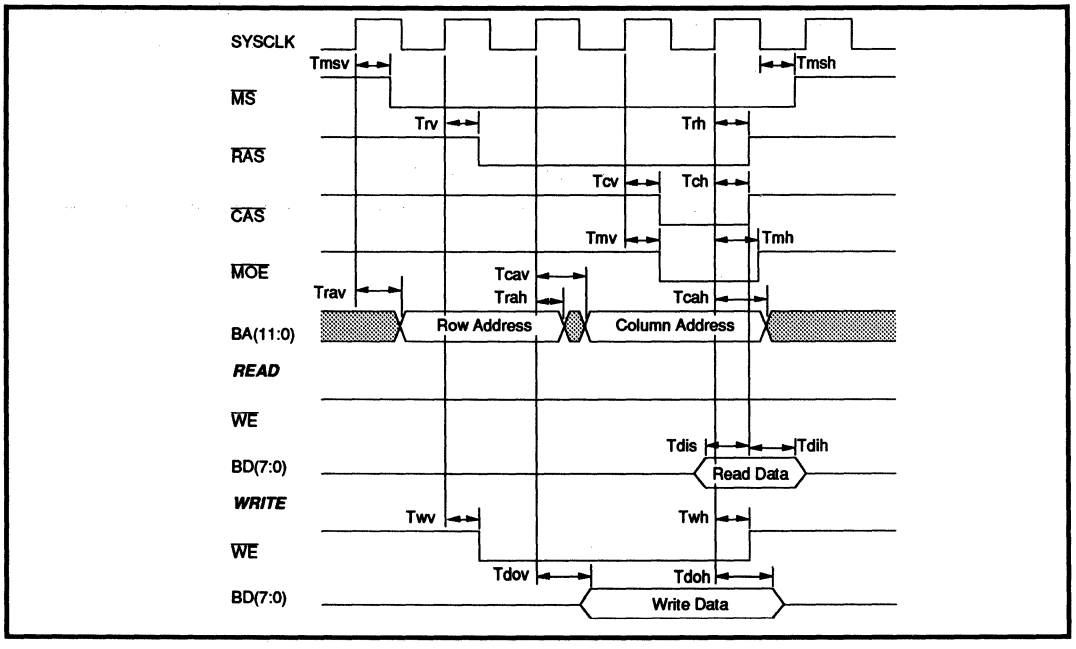



**FIGURE 12: DRAM Timing, Standard Cycle (Shown with RWL = 0 and CWL = 0)**

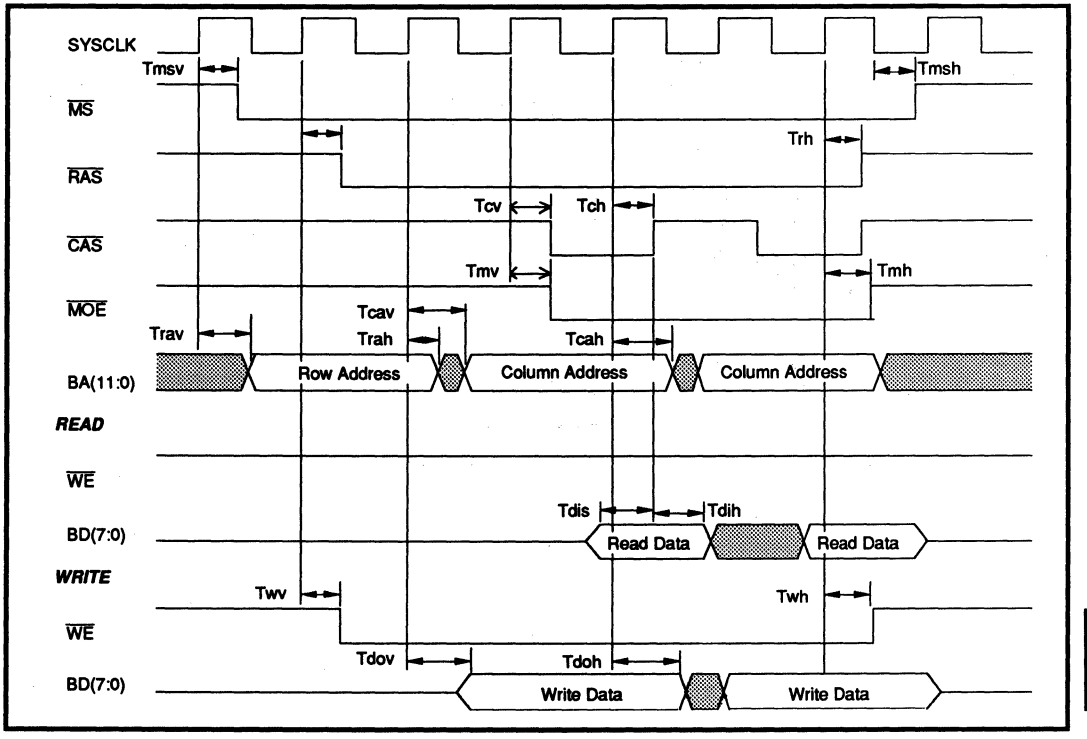



**FIGURE 13: DRAM Timing, Fast Page Cycles (Shown with RWL = 0, RWH = 0, CWL = 0 and CWH = 0)**

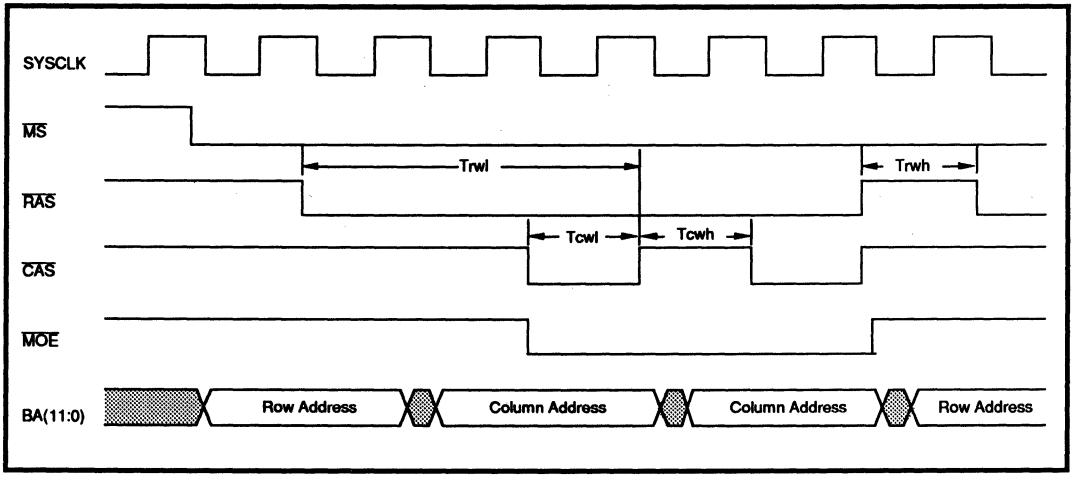



**FIGURE 14: DRAM Timing (Showing the Relationship of RWL, RWH, CWL and CWH to overall timing)**

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## ELECTRICAL SPECIFICATIONS (continued)

### HOST DMA 8/16-BIT INTERFACE TIMING PARAMETERS (Figure 15)

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| DREQL | DREQ ↓ from $\overline{DACK}$ ↓ | | | | 40 | ns |
| RDTA | $\overline{IOR}$ ↓ to HD[0:15] valid | | | | 50 | ns |
| RDHLD | $\overline{IOR}$ ↑ to HD[0:15] tri-state | | 2 | | 20 | ns |
| WDS | HD[0:15] setup to $\overline{IOW}$ ↑ | | 30 | | | ns |
| WDHLD | HD[0:15] hold from $\overline{IOW}$ ↑ | | 10 | | | ns |
| RWPULSE | $\overline{IOR}$/$\overline{IOW}$ pulse width | | 80 | | | ns |
| DMASET | $\overline{DACK}$ ↓ to $\overline{IOR}$/$\overline{IOW}$ ↓ | | 10 | | | ns |
| DMAHLD | $\overline{DACK}$ hold from $\overline{IOR}$/$\overline{IOW}$ ↑ | | 10 | | | ns |

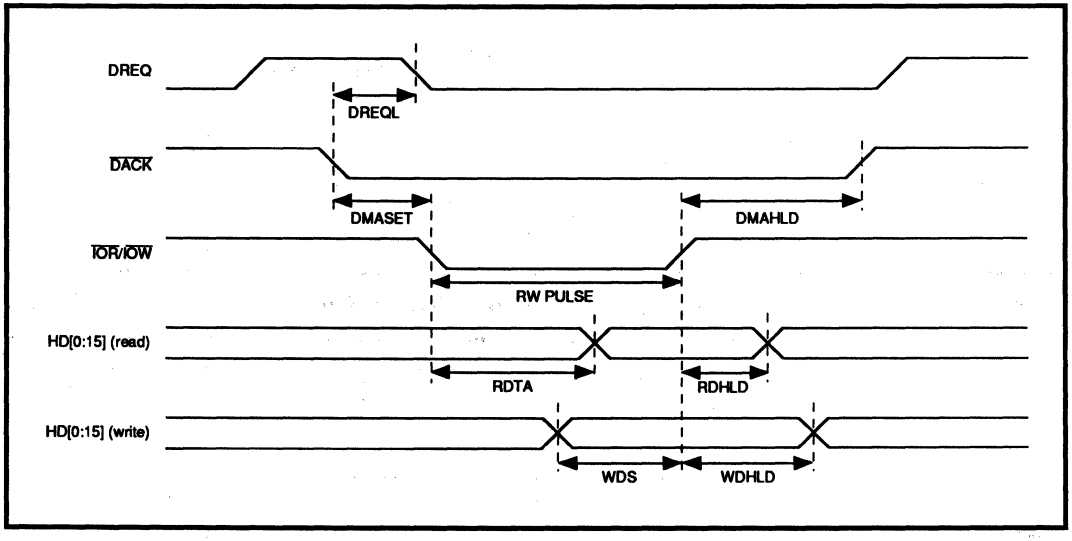


**FIGURE 15: Host DMA 8/16-Bit Interface Timing**

**HOST DMA 8/16-BIT INTERFACE TIMING PARAMETERS (DEMAND MODE) (Figure 16)**

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| DMASET | $\overline{DACK}$ ↓ to $\overline{IOR}$/$\overline{IOW}$ ↓ | | 10 | | | ns |
| RDTA | $\overline{IOR}$ ↓ to HD [0:15} valid | | | | 50 | ns |
| RDHLD | $\overline{IOR}$ ↑ to HD [0:15] tristate | | 2 | | 20 | ns |
| WDS | HD [0:15] setup to $\overline{IOW}$ ↑ | | 30 | | | ns |
| WDHLD | HD [0:15] hold from $\overline{IOW}$ ↑ | | 10 | | | ns |
| RWPULSE | $\overline{IOR}$/$\overline{IOW}$ low | | 80 | | | ns |
| RWPAUSE | $\overline{IOR}$/$\overline{IOW}$ high | | 40 | | | ns |
| DREQL | DREQ ↓ from $\overline{IOR}$/$\overline{IOW}$ ↓ | | 5 | | 40 | ns |
| DMAHLD | $\overline{DACK}$ hold from $\overline{IOR}$/$\overline{IOW}$ ↑ | | 10 | | | ns |

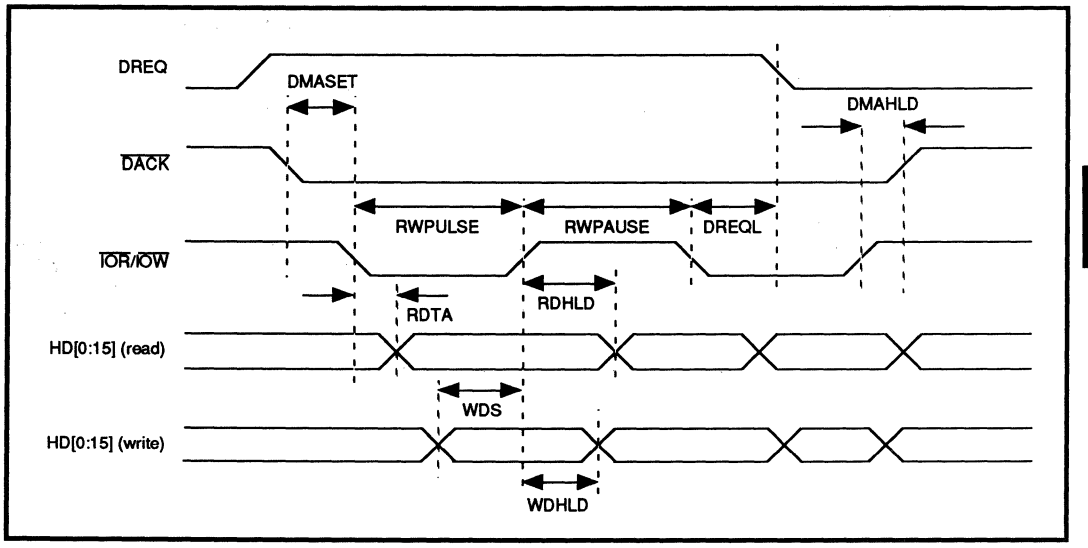


**FIGURE 16: Host DMA 8/16-Bit Interface Timing (Demand Mode)**

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## ELECTRICAL SPECIFICATIONS (continued)

### HOST PROGRAMMED I/O TIMING PARAMETERS (Figure 16)

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| CS16L | $\overline{HCS0}$ ↓, A0:2, A9 ↓, or $\overline{HSC1}$ ↑ to $\overline{IOCS16}$ ↓ | | | | 20 | ns |
| IOCHL | $\overline{IOR}$/$\overline{IOW}$ ↓ to $\overline{IOCHRDY}$ ↓ | | | | 25 | ns |
| IOCHTW * | IOCHRDY pulse width | | 0 | | 5 x BCLK | ns |
| RDTA | $\overline{IOR}$ ↓ to HD[0:15] valid | | | | 50 | ns |
| RDHLD | $\overline{IOR}$ ↑ to HD[0:15] tri-state | | 2 | | 20 | ns |
| WDS | HD[0:15] setup to $\overline{IOW}$ ↑ | | 30 | | | ns |
| WDHLD | HD[0:15] hold from $\overline{IOW}$ ↑ | | 10 | | | ns |
| RWPULSE | $\overline{IOR}$/$\overline{IOW}$ pulse width | | 80 | | | ns |
| ADRSET | $\overline{HCS0}$, A0:2, A9/$\overline{HCS1}$ setup to $\overline{IOR}$/$\overline{IOW}$ ↓ | | 25 | | | ns |
| ADRHLD | $\overline{HCS0}$, A0:2, A9,$\overline{HCS1}$ hold, from $\overline{IOR}$/$\overline{IOW}$ ↑ | | 0 | | | ns |
| * Maximum specification applies when Auto Wait State Generation is disabled (Register 40H, Bit 2 is reset) | | | | | | |

### RESET ASSERTION TIMING PARAMETERS (Figure 17)

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| Trpwl | $\overline{RST}$ pulse width low | Not power on reset | 500 | | | ns |
| | | Power on reset | 7.5 | | | µs |

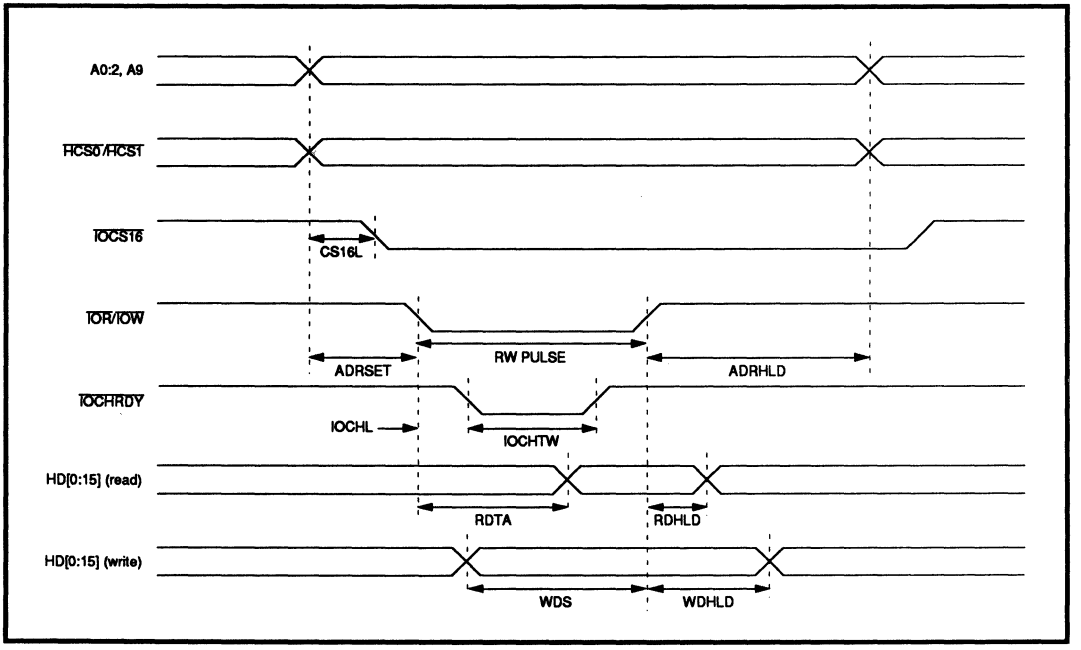
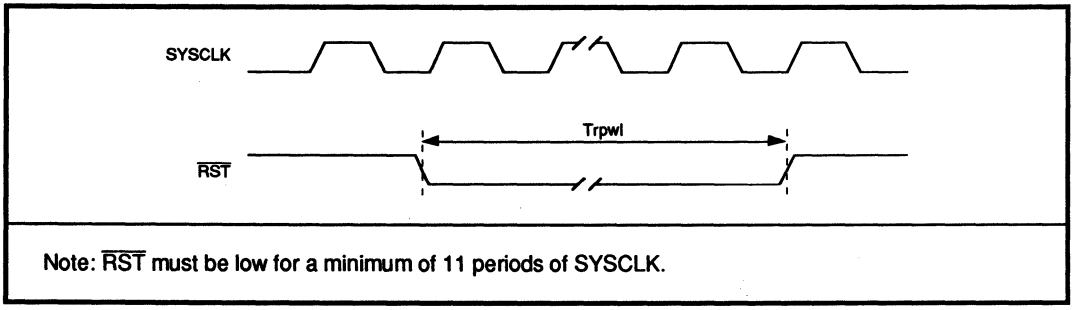



**FIGURE 16: Host Programmed I/O 8/16-Bit Timing**



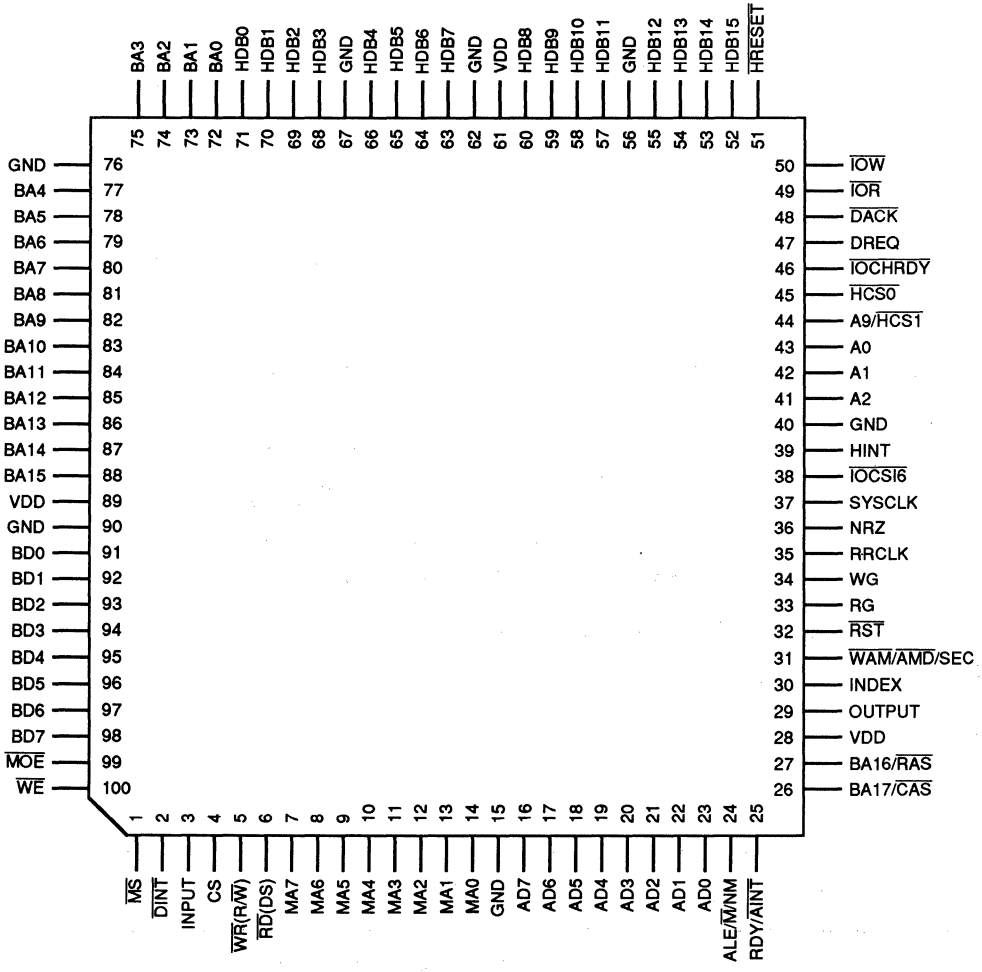

Note: $\overline{RST}$ must be low for a minimum of 11 periods of SYSCLK.

**FIGURE 17: RESET Assertion Timing**

## PACKAGE PIN DESIGNATIONS

(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.

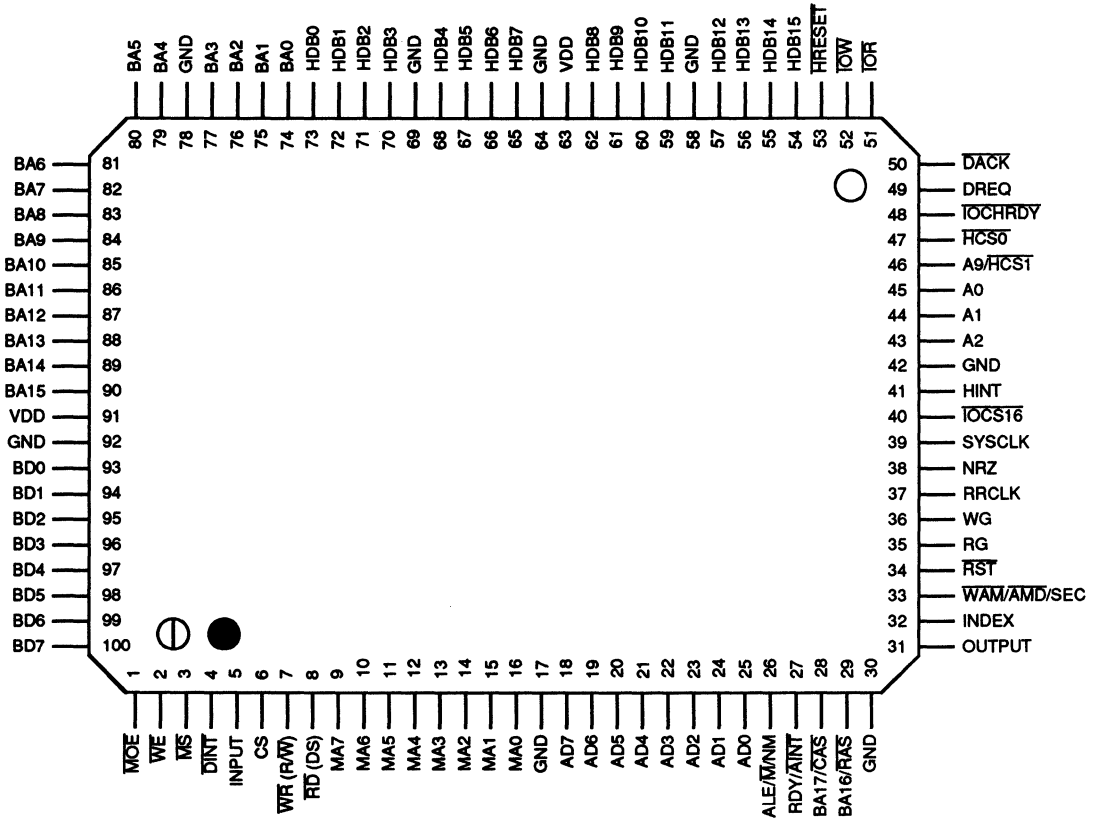



**100-Lead TQFP**

## PACKAGE PIN DESIGNATIONS

(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.




**100-Lead QFP**

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**Advance Information:** Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.



Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680, (714) 573-6000, FAX: (714) 573-6914

**Notes:**

silicon systems®
A TDK Group Company

# SSI 32C9020
## SCSI Combo Controller
## 48 Mbit/s; single bit NRZ interface

**Advance Information**

January 1993

## DESCRIPTION

The SSI 32C9020 is an advanced CMOS VLSI device which integrates major portions of the hardware needed to build an SCSI disk drive. The circuitry of the SSI 32C9020 includes a complete SCSI target interface, an advanced buffer manager, a high performance disk formatter and an 88 bit Reed-Solomon ECC with fast "on-the-fly" hardware correction. The SSI 32C9020 provides maximum performance while minimizing micro controller intervention.

The SSI 32C9020 is capable of concurrent transfers of up to 48 megabits per second on the disk interface and 10 megabytes per second across the SCSI bus. In addition, on-the-fly error corrections and micro controller accesses to the buffer memory will not degrade the throughput during transfers.

The SSI 32C9020 is one of a family of Silicon Systems' single chip disk controllers which support a wide range of device interfaces. The SSI 32C9022 provides the same basic capabilities as the SSI 32C9020 but has

(continued)

## FEATURES

- **SCSI Bus Interface**
  - **Full SCSI-2 Compatibility**
  - **Direct bus interface logic with on-chip 48 mA drivers**
  - **Synchronous transfer rates up to 10 megabytes per second**
  - **Asynchronous transfer rates up to 5 megabytes per second**
  - **Parity generation and checking**
  - **Auto Command Mode (ACM) SCSI state machine performs high level SCSI sequences without microprocessor intervention**
  - **Four level ACM command FIFO supports automatic execution of multiple ACM commands**
  - **Hardware support for automatic handling of SCSI-2 command queuing**

(continued)

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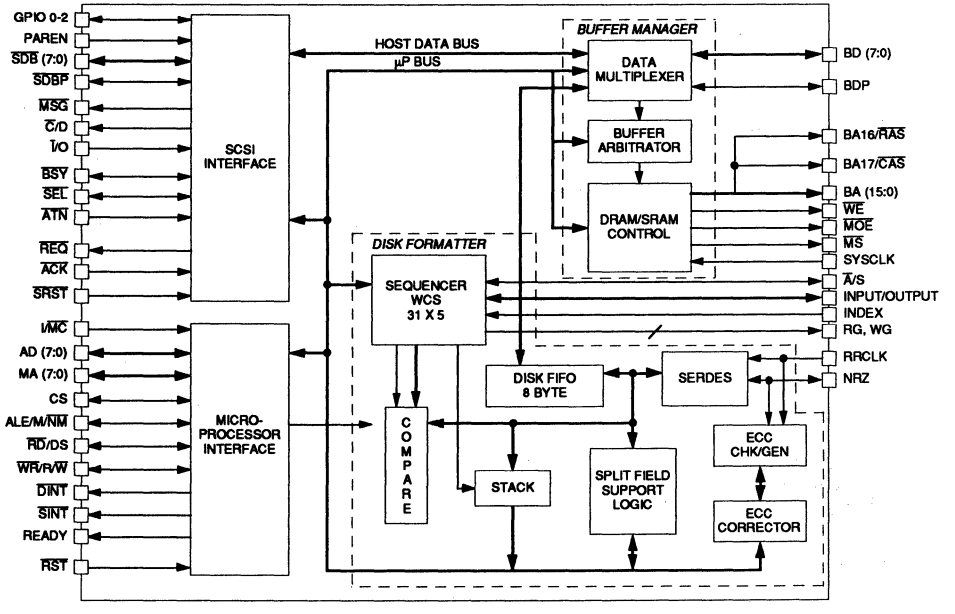
## BLOCK DIAGRAM



**DESCRIPTION** (continued)

a dual NRZ disk interface. Other family members support AT and PCMCIA interfaces. All members are based on a common architecture allowing major portions of firmware to be reused. The Silicon Systems' chip family is illustrated in the hierarchy chart shown in Figure 1.

The high level of integration within the SSI 32C9020 represents a major reduction in parts count. When the SSI 32C9020 SCSI Controller is combined with the SSI 32R2010 Read/Write device, the SSI 32P3000 Pulse Detector, the SSI 32D5391 Data Synchronizer with 1,7 ENDEC, the 32H4631 Servo and Motor Speed Controller, an appropriate micro controller and memory, a complete, cost efficient, high performance intelligent drive solution is created.

## FEATURES (continued)

- Automatic SCSI CDB size determination
- Automatic SCSI Disconnect and Reconnect
- Sixteen byte data FIFO between SCSI channel and Buffer Manager

- **Buffer Manager**
  - Direct support of DRAM or SRAM
  - SRAM throughput to 20 megabytes per second
  - SRAM size up to 256k bytes
  - DRAM throughput to 17.78 megabytes per second
  - DRAM size up to 1 megabyte
  - Programmable memory timing
  - Buffer RAM segmentation with flexible segment sizes from 256 bytes to 1 megabyte
  - Dedicated host, disk and microprocessor address pointers
  - Internal buffer protection circuit provides buffer integrity
- **Disk Formatter**
  - NRZ Data Rates to 48 megabits/s
  - Automatic multi-sector transfer
  - Header or microprocessor based split data field support
  - Advanced sequencer organized in 31 x 5 bytes
  - 88-bit Reed Solomon ECC with "on-the-fly" fast hardware correction circuitry
  - Capable of correcting up to four 10-bit symbols in error
  - Guaranteed to correct one 31-bit burst or two 11-bit bursts
  - Hardware on-the-fly correction of either an 11- or 31-bit single burst error within a half sector time
  - Detects up to one 51-bit burst or three 11-bit bursts
- **Microprocessor Interface**
  - Supports both multiplexed or non-multiplexed microprocessors
  - Separate or combined host and disk interrupts
  - Programmable wait state insertion
- **Other Features**
  - Internal power down mode
  - Available in 100-pin QFP

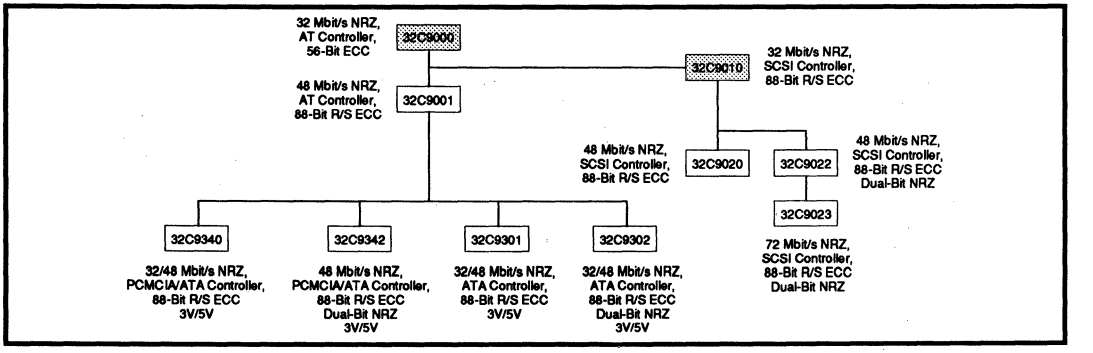



**FIGURE 1: Silicon Systems' Disk Controller Chip Hierarchy**

## FUNCTIONAL DESCRIPTION

The SSI 32C9020 contains the following four major functional blocks:

Microprocessor Interface

SCSI Interface

Disk Formatter

Buffer Manager

The Microprocessor Interface allows the local microprocessor access to all of the SSI 32C9020 internal control registers and any location within the buffer memory. The microprocessor, by writing and reading the internal registers can control all activities of the SSI 32C9020. The microprocessor can elect to perform SCSI and/or disk operations directly, or it can enable the advanced features of the SSI 32C9020 which can perform all typical operations automatically.

The SCSI Interface block handles all SCSI activities. The SCSI interface includes 48 mA drivers allowing for direct connection of the SSI 32C9020 to the SCSI bus. The SCSI interface logic includes Auto Command Mode (ACM) logic, an advanced state machine capable of handling a variety of complex SCSI sequences without microprocessor intervention. The microprocessor can queue up to four ACM commands into the ACM Command FIFO to create even more sophisticated command sequences. The SCSI block interfaces directly with the Buffer Manager via an internal speed matching FIFO. This FIFO, plus the bandwidth capabilities of the Buffer Manager guarantee sustained full speed transfers across the SCSI bus. The high level of automation of the ACM minimizes SCSI bus overhead. The net result is maximized performance with minimum SCSI bus band width utilization.

The Disk Formatter performs the serialization and deserialization of data. It provides all of the necessary functions to control track formatting, header search, and the reading and writing of data. The heart of the Disk Formatter is an advanced programmable sequencer which is flexible enough to interface to a wide variety of read/write channels. The sequencer can contain 31 instructions, each of which is 5 bytes (40 bits) in width. The width of the instructions allows for sophisticated branching techniques which increase the flexibility and power of the sequencer. The flexible disk interface can be configured through a wide range of capabilities. This allows the SSI 32C9020 to interface with nearly any read/write channel and allows the user of the SSI 32C9020 to select the read/write channel best suited to the device. Of course, by selecting the SSI 32C9020 controller and the SSI 32D5391 Data Synchronizer with 1,7 ENDEC, you are guaranteed a problem free interface.

Within the Disk Formatter are the ECC generator/checker and ECC corrector. The generator/checker provides the ability to generate or check a 32 bit ECC for headers and an 88 bit Reed Solomon code for data. If the checker detects an error in an 88 bit Reed Solomon data field, the syndrome information is transferred into the corrector. The corrector performs the necessary operations to determine if the error was correctable and interfaces directly with the buffer controller to perform the correction automatically. The corrector performs its correction within one half of a sector time. This guarantees that the corrector will always be available to correct the next sector if necessary.

As its name implies, the Buffer Manager manages the data buffer of the controller. The Buffer Manager can support either SRAM or DRAM. When configured to operate with DRAM, the Buffer Manager automatically performs necessary refresh cycles. The buffer manager creates all of the necessary timing and control signals for a wide range of memory types and speeds. The Buffer Manager interfaces with the buffer memory, the SCSI Interface block, the data path of the Disk Formatter block, the ECC corrector and the microprocessor. If more than one of these devices requires access to the buffer memory, the Buffer Manager arbitrates the requests automatically. The Buffer Manager of the SSI 32C9020 can sustain SCSI operations at the rate of 10 megabytes per second, Disk Formatter operations at 48 megabits per second (6 megabytes per second) and still have sufficient band width left to handle on-the-fly ECC corrections and microprocessor accesses without degrading performance on any of the interfaces.

## PIN DESCRIPTION

The following convention is used in the pin description:

(I) denotes an input

(O) denotes an output

(Z) denotes a tri-state output

(OD) denotes an open drain output

**GENERAL**

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| VDD | | POWER SUPPLY PIN, VCC |
| GND | | GROUND |

**HOST INTERFACE**

| | | |
|---|---|---|
| $\overline{SDBP}$ | I/O | SCSI DATA BUS PARITY. Odd parity bit for the SCSI data bus. |
| $\overline{SDB(7:0)}$ | I/O | SCSI DATA BUS BITS 7-0. |
| $\overline{ATN}$ | I | ATTENTION. This active low signal is used by the initiator to request a message out phase. |
| $\overline{BSY}$ | I/O | BUSY. This active low signal is used to indicate when the bus is active. |
| $\overline{ACK}$ | I | ACKNOWLEDGE. This active low signal is used in the handshake protocol to indicate the completion of a data byte transfer. |
| $\overline{SRST}$ | I | SCSI RESET. This active low signal is used to reset the SCSI controller. |
| $\overline{MSG}$ | O | MESSAGE. This active low signal is used to indicate a message phase. |
| $\overline{SEL}$ | I/O | SELECT. This active low signal is used to indicate either a selection or reselection phase. |
| $\overline{C}$/D | O | COMMAND/DATA. This signal is used to indicate either a command or data phase. |
| $\overline{REQ}$ | I | REQUEST. This active low signal is used in the handshake protocol to initiate a data byte transfer. |
| $\overline{I}$/O | I | INPUT/OUTPUT. This signal is used to indicate the direction of data transfer. |
| PAREN | I | SCSI PARITY ENABLE. This active high signal is used to enable parity checking of the SCSI data bus. Parity checking is disabled when this pin is held low. |

**DISK INTERFACE**

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| GPIO(2:0) | I/O | INPUT/OUTPUT. These pins are used to indicate the SCSI ID of the target device. The pins can be programmed as outputs for test purposes only. |
| INDEX | I | INDEX. Input for index pulse received from the drive. |
| INPUT/ | I/O | DISK SEQUENCER INPUT/OUTPUT. A general purpose control (output) and status (input) pin configured by the Output Enable Bit of Register 71H, bit 7.<br>At power-on, this pin is an input. As an input, it can be used to synchronize the disk sequencer to an external event. As an output, it is controlled by bit 2 of the Control Field of the disk sequencer. |
| $\overline{\text{AMD}}$/SECTOR | I/O | ADDRESS MARK DETECT/SECTOR. This pin is used in the hard sector mode as the sector input. A pulse on this pin indicates a sector mark is found.<br>In the soft sector mode a low-level input indicates an address mark was detected. The device powers up in soft sector default mode. |
| RG | O | READ GATE. During disk data read, this pin is asserted. Active high. |
| WG | O | WRITE GATE. During disk data write, this pin is asserted. Active high. |
| RRCLK | I | READ/REFERENCE CLOCK. This pin is used to clock data on the NRZ pin into and out of the device. |
| NRZ | I/O | NON RETURN TO ZERO. This signal is the read data input from the disk drive when the read gate signal is asserted; it is the write data output to the disk drive when the write gate signal is asserted. |

**MICROPROCESSOR INTERFACE**

| | | |
|---|---|---|
| $\overline{\text{RST}}$ | I | RESET. An asserted low input generates a component reset that holds the internal registers at reset, stops all operations within the chip, and deasserts all output signals. All input/output signals are set to the high-Z state during the assertion of this signal. |
| ALE/M/$\overline{\text{NM}}$ | I | ADDRESS LATCH ENABLE/MULTIPLEXED/NON-MULTIPLEXED ADDRESS SELECT. When tied high or left floating after reset, the microprocessor interface is configured as non-multiplexed. When driven low, then the microprocessor interface is configured as multiplexed. In this case this pin functions as the address latch enable, and the MA(7:0) pins are the demultiplexed address outputs. |
| CS | I | CHIP SELECT. Active high signal, when asserted, the internal registers of the SSI 32C9020 can be accessed. |
| $\overline{\text{WR}}$/R/$\overline{\text{W}}$ | I | WRITE STROBE/READ/WRITE. In the Intel bus mode, when an active low signal is present with CS signal high, the data is written to the internal registers.<br>In the Motorola bus mode, this signal acts as the R/$\overline{\text{W}}$ signal. |
| $\overline{\text{RD}}$/DS | I | READ STROBE/DATA STROBE. In the Intel bus mode, when an active low signal is present with CS signal high, internal register data is read.<br>In the Motorola mode, this signal acts as the DS signal. DS when active high is data strobe. |

## PIN DESCRIPTION (continued)

### MICROPROCESSOR INTERFACE (continued)

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| DINT | O, OD,Z | DISK INTERRUPT. An active low signal indicates the controller is requesting microprocessor service from the disk side. This signal is programmable for either a push-pull or open-drain output circuit. This signal powers up in the high-Z state. Register 4F bit 3 enables the pull-up. |
| $\overline{SINT}$ | O, OD,Z | SCSI INTERRUPT. This signal is generated by the SCSI controller and is an interrupt line to the microprocessor. It is programmable for either a push-pull or open drain output circuit. This signal powers up in the high-Z state. The interrupt is sourced from the SCSI Interrupt Register. Register 4F bit 3 enables the pull-up. This signal is also programmable to be either an active high or low interrupt. |
| AD(7:0) | I/O | ADDRESS/DATA BUS. When configured in the Intel mode, these lines are multiplexed, bidirectional microprocessor register address and data lines.<br>When configured in the Motorola mode, these lines are bidirectional data lines. |
| MA(7:0) | I/O | MICROPROCESSOR ADDRESS BUS: These signals are nonmultiplexed address input or latched address output lines. |
| READY | O | READY: When this signal is deasserted low, the microprocessor shall insert wait states to allow time for the chip to respond. |
| I/$\overline{MC}$ | I | INTEL/MOTOROLA: This signal selects the microprocessor interface to be used. When this signal is asserted high, it selects the Intel bus control interface. When this signal is deasserted low, it selects the Motorola bus control interface. This signal has an internal pull-up to allow the default selection of the Intel bus control interface. |

### BUFFER MANAGER INTERFACE

| | | |
|---|---|---|
| BA(15:0) | O | BUFFER MEMORY ADDRESS LINES 0:15. Active high, for direct connection to a Static or Dynamic RAM address lines 0:15. |
| BA16/$\overline{RAS}$ | O | BUFFER MEMORY ADDRESS 16: In SRAM mode, for direct connection to a Static RAM address line 16.<br>ROW ADDRESS STROBE: In DRAM mode, for direct connection to a Dynamic RAM Row Address Strobe signal. |
| BA17/$\overline{CAS}$ | O | BUFFER MEMORY ADDRESS 17: In SRAM mode, for direct connection to a Static RAM address line 17.<br>ROW ADDRESS STROBE: In DRAM mode, active low, for direct connection to a Dynamic RAM Column Address Strobe signal. |
| BD(7:0) | I/O | BUFFER MEMORY DATA BUS. 7 through 0. Active high, buffer data bus that connects directly to the buffer RAM data lines. |

**BUFFER MANAGER INTERFACE**

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| BDP | I/O | BUFFER MEMORY DATA PARITY. This signal provides odd parity for the buffer memory data bus during transfers to/from the buffer memory to the buffer RAM. |
| $\overline{MOE}$ | O | MEMORY OUTPUT ENABLE. This signal is asserted low only for buffer memory read operations. |
| $\overline{WE}$ | O | WRITE ENABLE. Active low, write enable for the buffer RAM. |
| SYSCLK | I | SYSTEM CLOCK. This signal is used to synchronize the buffer RAM access, including the generation of memory address bits, write enable $\overline{WE}$, and memory output enable $\overline{MOE}$. |

## ELECTRICAL SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS

Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC operating characteristics.

| PARAMETER | RATING |
|---|---|
| Power Supply Voltage, VCC | 7V |
| Ambient Temperature | 0 to 70 °C |
| Storage Temperature | -65 to 150 °C |
| Power Dissipation | 750 mW |
| Input, Output pins | -0.5 to VCC+0.5V |

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**ELECTRICAL CHARACTERISTICS**

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|
| VCC Power Supply Voltage | | 4.50 | | 5.50 | V |
| ICC Supply Current | Ta = 25°C Outputs Unloaded | | | 50 | mA |
| ICCS Supply Current | | | | 250 | µA |
| VIL Input Low Voltage | | -0.5 | | 0.8 | V |
| V0IH Input High Voltage | | 2.0 | | VCC+0.5 | V |
| VOL Output Low Voltage | All pins except SCSI interface, IOL = 2 mA | | | 0.4 | |
| VOL Output Low Voltage | SCSI interface pins, IOL = 48 mA | | | 0.5 | V |
| VOH Output High Voltage | IOH = -400 µA | | | 2.4 | V |
| IL Input Leakage Current | 0 < VIN < VCC | -10 | | 10 | µA |
| CIN Input Capacitance | | | | 10 | pF |
| COUT Output Capacitance | | | | 10 | pF |

## ELECTRICAL SPECIFICATIONS (continued)

### Microprocessor Interface Timing Parameters

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|---|
| Ta | Ale width | | 20 | | | ns |
| Tma | Address valid to MA0:7 valid | | | | 30 | ns |
| Tr | $\overline{RD}$ Width | | 80 | | | ns |
| As | Address valid to ALE ↓ | | 5 | | | ns |
| Ah | ALE ↓ to address invalid | | 10 | | | ns |
| Cs | CS Valid to $\overline{RD}$ ↓ or DS ↑ | | 20 | | | ns |
| Ch | $\overline{RD}$ ↑ or DS ↓ to CS ↓ | | 0 | | | ns |
| Tda | $\overline{RD}$ ↓ or DS ↑ to read data valid | | | | 60 | ns |
| Tds | DS width | | 80 | | | ns |
| Tdh | $\overline{RD}$ ↑ or DS ↓ to read data invalid | | 0 | | 25 | ns |
| Tsrw | R/$\overline{W}$ valid to DS ↑ | | 20 | | | ns |
| Thrw | DS ↓ to R/$\overline{W}$ invalid | | 20 | | | ns |
| Tdrdy | $\overline{RD}$ ↓ to READY ↓ (Intel) or DS ↑ to READY ↓ (Motorola) | | | | 30 | ns |
| Wds | Write data valid to $\overline{WR}$ ↑ or DS ↓ to write data invalid | | 40 | | | ns |
| Wdh | $\overline{WR}$ ↑ or DS ↓ to write data invalid | | 10 | | | ns |
| Note: | ↑ indicates rising edge | ↓ indicates falling edge | | | | |

### Non-Multiplexed Bus Interface Timings

| | | | | | | |
|---|---|---|---|---|---|---|
| Tmas | MA(7:0) valid to DS ↓ | | 5 | | | ns |
| Tmah | DS ↑ to MA(7:0) invalid | | 5 | | | ns |
| Cs | CS valid to DS ↓ | | 20 | | | ns |
| Ch | DS ↑ to CS ↓ | | 0 | | | ns |
| Tda | DS ↑ to read data valid | | | | 60 | ns |
| Tds | DS width | | 80 | | | ns |
| Tdh | DS ↑ to read data invalid | | 0 | | 25 | ns |
| Tsrw | R/$\overline{W}$ valid to DS ↓ | | 20 | | | ns |
| Thrw | DS ↑ to R/$\overline{W}$ invalid | | 20 | | | ns |
| Tdrdy | DS ↑ to READY ↓ (Motorola) | | | | 30 | ns |
| WDS | Write data valid to $\overline{WR}$ ↑ or DS ↓ | | 40 | | | ns |
| Wdh | $\overline{WR}$ ↑ or DS ↓ to write data invalid | | 10 | | | ns |
| Note 1: | ↑ indicates rising edge | ↓ indicates falling edge | | | | |
| Note 2: | Loading capacitor = 30pF | | | | | |

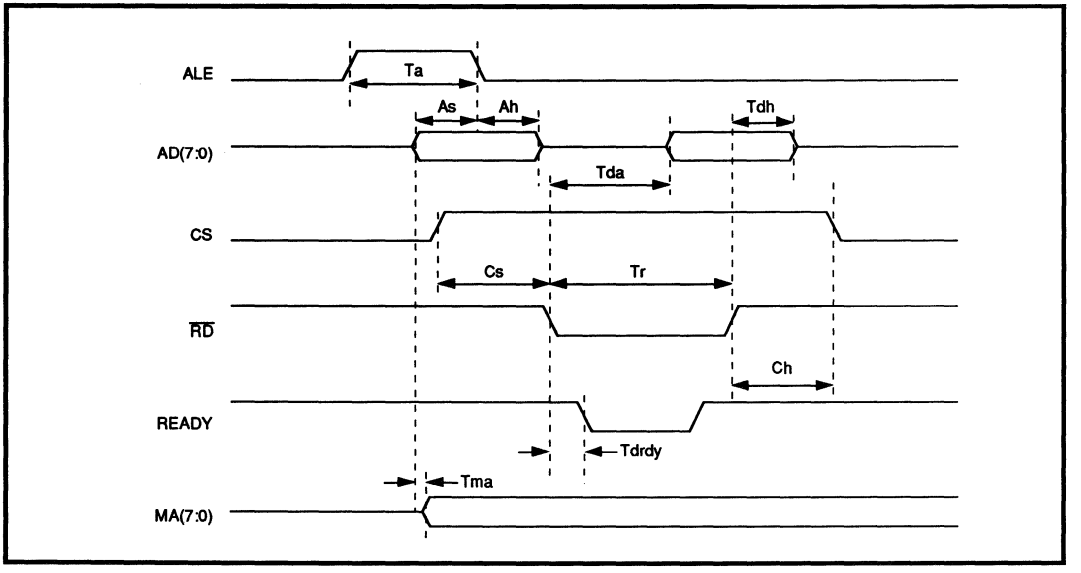


**FIGURE 2: Intel Register Multiplexed Read Timing**



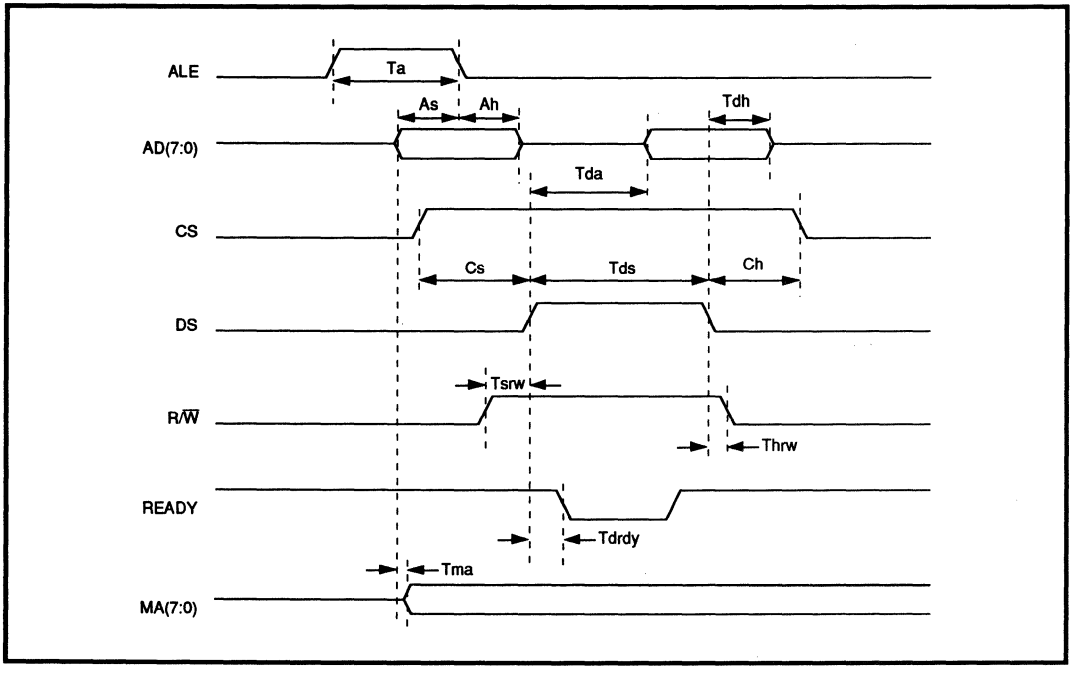


**FIGURE 3: Motorola Register Multiplexed Read Timing**

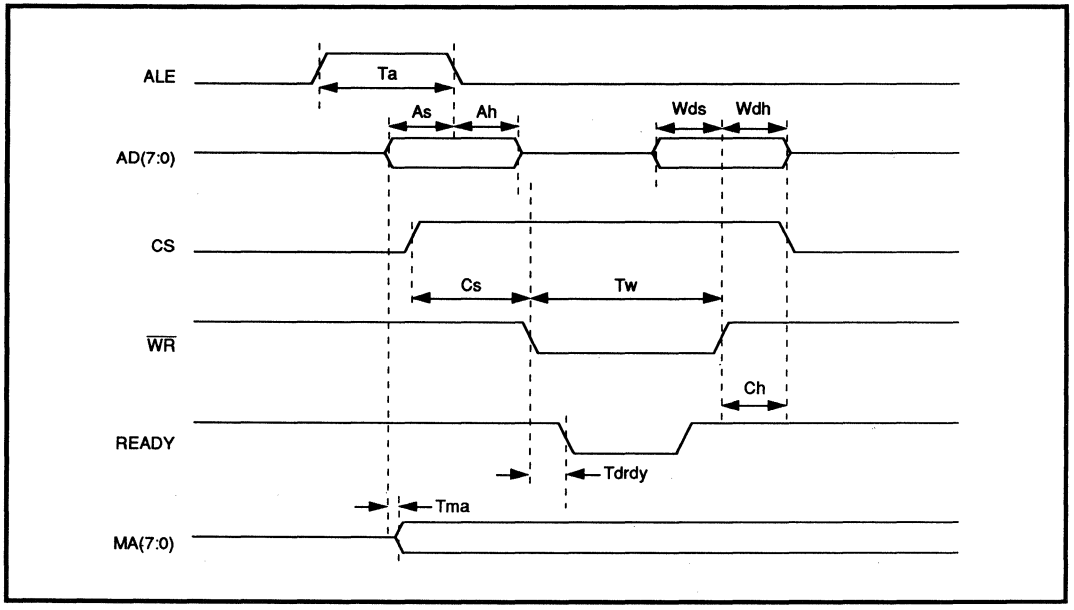


**FIGURE 4: Intel Register Multiplexed Write Timing**

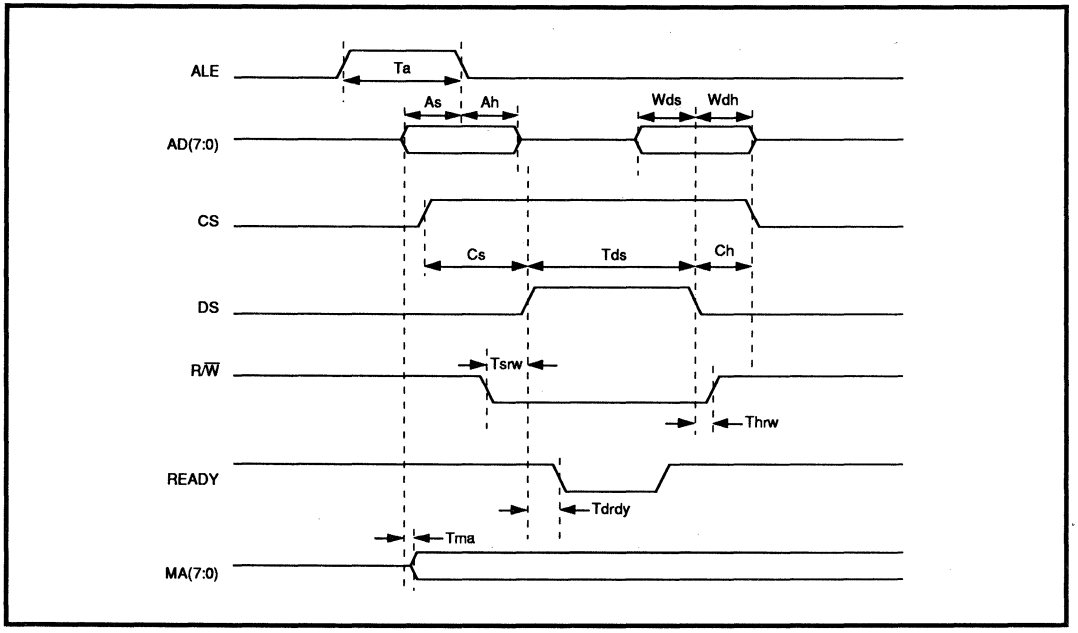


**FIGURE 5: Motorola Register Multiplexed Write Timing**

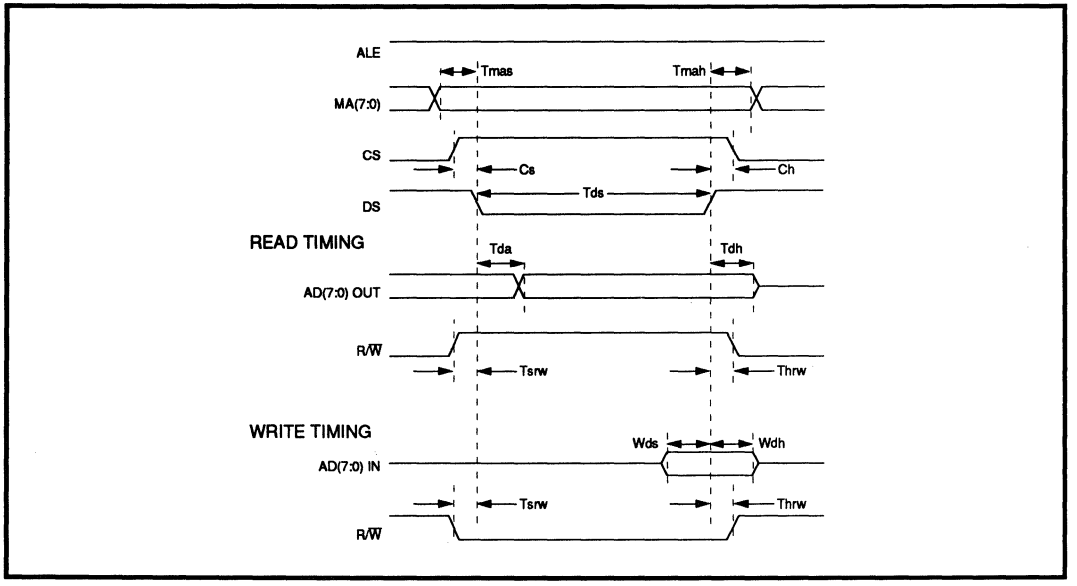


**FIGURE 6: Non-Multiplexed Bus Timing Diagrams**

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## ELECTRICAL SPECIFICATIONS (continued)

### Disk Interface Timing

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|---|
| T | RRCLK | | 20.8 | | | ns |
| T/2 | RRCLK high/low time | | 8.5 | | | ns |
| Tr, Tf | RRCLK rise and fall time | | 0 | | 2 | ns |
| Ds | NRZ in valid to RRCLK ↑ | | 3 | | | ns |
| Dh | RRCLK ↑ to NRZ in invalid | | 3 | | | ns |
| As | $\overline{AME}$ valid to RRCLK ↑ | | 3 | | | ns |
| Dv | RRCLK ↑ to NRZ out | | 3 | | 15 | ns |
| Note: | ↑ indicates rising edge | | | | | |
| Loading capacitor = 10pF | | | | | | |

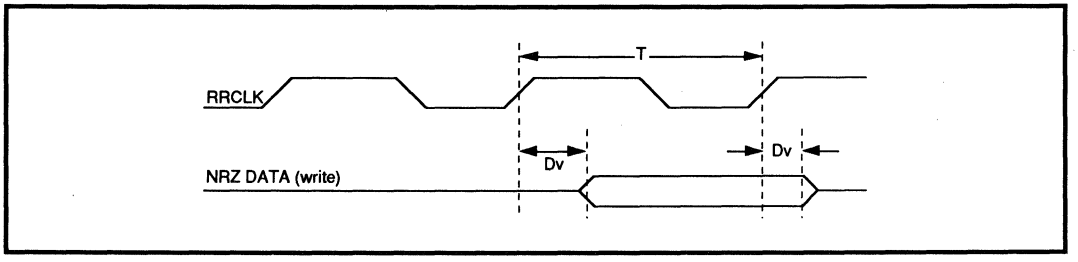



**FIGURE 7: Disk Write Timing**

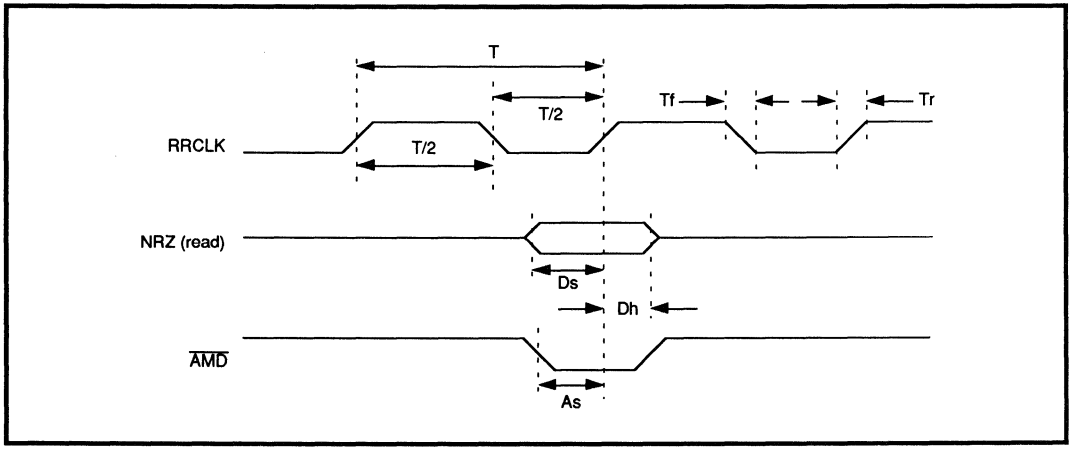



**FIGURE 8: Disk Read Timing**

**BUFFER MEMORY READ/WRITE TIMING PARAMETERS (Figures 9 through 13)**

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| T | SYSCLK period | | 25 | | | ns |
| T/2 | SYSCLK high/low time | | 10 | | | ns |
| Tav | SYSCLK / to address valid | Note 1 | | | 18 | ns |
| Tmsv | SYSCLK / to $\overline{MS}$\ | Notes 1, 6 | | | 18 | ns |
| Tmsh | SYSCLK / to $\overline{MS}$/ | Note 1 | | | 18 | ns |
| Tmv | SYSCLK / to $\overline{MOE}$\ | Note 1 | | | 18 | ns |
| Tmh | SYSCLK / to $\overline{MOE}$/ | Note 1 | | | 18 | ns |
| Twv | SYSCLK / to $\overline{WE}$\ | Note 1 | | | 18 | ns |
| Twh | SYSCLK / to $\overline{WE}$/ | Note 1 | | | 18 | ns |
| Tdov | SYSCLK to data out valid | Note 1 | | | 18 | ns |
| Tdoh | SYSCLK to data out invalid | Note 1 | | | 18 | ns |
| Tdis | Data in valid to $\overline{MOE}$ / (SRAM)<br>Data in valid to $\overline{CAS}$ / (DRAM) | | 5 | | | ns |
| Tdih | $\overline{MOE}$ to data in valid (SRAM)<br>$\overline{CAS}$ to data in valid (DRAM) | | 0 | | | ns |
| Trv | SYSCLK / to $\overline{RAS}$\ | Note 1 | | | 18 | ns |
| Trh | SYSCLK / to $\overline{RAS}$/ | Note 1 | | | 18 | ns |
| Trav | SYSCLK to row address valid | Note 1 | | | 18 | ns |
| Trah | SYSCLK / to row address invalid | Note 1 | | | 18 | ns |
| Tcv | SYSCLK / to $\overline{CAS}$\ | Note 1 | | | 18 | ns |
| Tch | SYSCLK / to $\overline{CAS}$/ | Note 1 | | | 18 | ns |
| Tcav | SYSCLK / to column address valid | Note 1 | | | 18 | ns |
| Tcah | SYSCLK / to column address invalid | | 0 | | | ns |

## ELECTRICAL SPECIFICATIONS (continued)

### BUFFER MEMORY READ/WRITE TIMING PARAMETERS (Figures 9 through 13) (continued)

| PARAMETER | | CONDITIONS | MIN | UNIT |
|---|---|---|---|---|
| Trwl | $\overline{RAS}$\ to $\overline{RAS}$/ | Notes 2, 3 | ((RWL + 3)•T)-2 | ns |
| Trwh | $\overline{RAS}$/ to $\overline{RAS}$\ | Notes 2, 4 | ((RWH + 1)•T)-2 | ns |
| Tcwl | $\overline{CAS}$\ to $\overline{CAS}$/ | Note 2 | ((CWL + 1)•T)-2 | ns |
| Tcwl | $\overline{CAS}$/ to $\overline{CAS}$\ | Notes 2, 5 | ((CWL + 1)•T)-2 | ns |

Note: Loading capacitance = 30 pF

Note 1: The measured delay for any of the signal indicated by this note will not vary from the measured delay of any other signal indicated by this note by more than ±1 ns.

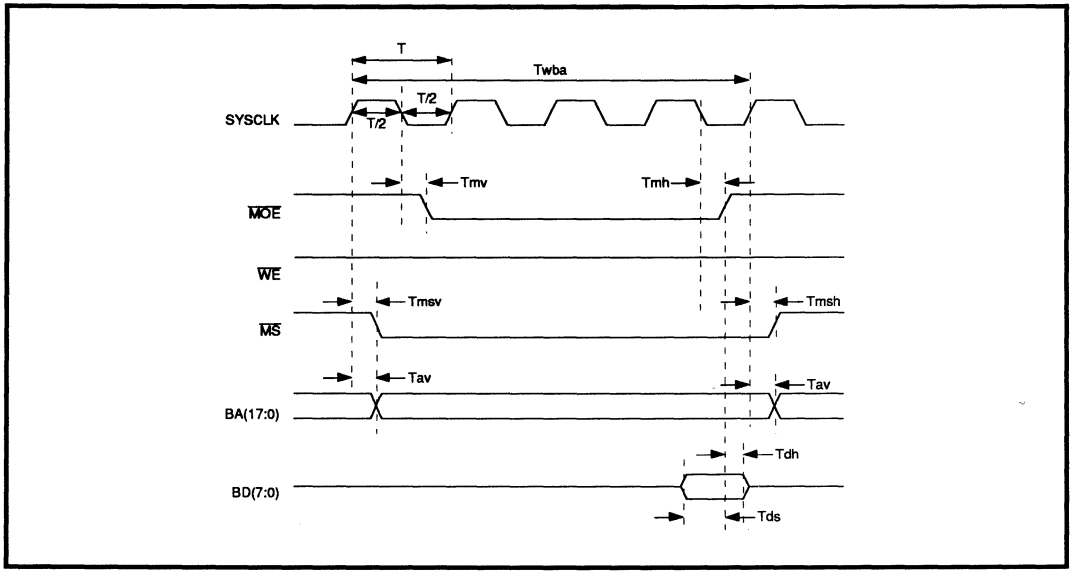
Note 2: RWL, RWH, CWL and CWH are fields in the Buffer Manager Timing Control Register (54H). Each is a two bit field which can contain a value of 0, 1, 2, or 3. These values determine the minimum number of SYSCLK periods (T) for the associated signal width.

Note 3: The minimum width value of Trwl will be generated for refresh cycles and for any buffer memory access cycle except when multiple page mode accesses are performed. When multiple page mode accesses are performed, the width of the $\overline{RAS}$ low pulse is extended until the end of the last $\overline{CAS}$ low cycle.

Note 4: The minumum value of Trwh will be generated whenever the Buffer Manager determines that a buffer request is pending at the ocmpletion of the current memory cycle and a page mode access can not be used either because page mode operation is not enabled or the needed location is not within the current page.

Note 5: The minumum value of Tcwh will be generated only between consecutive page mode accesses.

Note 6: $\overline{MS}$ will rise only if the Buffer Manager determines that no additional requests for buffer access are pending. If the Buffer Manager determines that another access is to be Made, $\overline{MS}$ is kept low between the accesses for improved speed.




Note: Twba is a functional parameter that gives the duration of one RAM data buffer access cycle in SYSCLK periods. The value is programmed in bits 1-0 of register 54H. These examples show Twba = 4T.

**FIGURE 9: SRAM Read Timing**



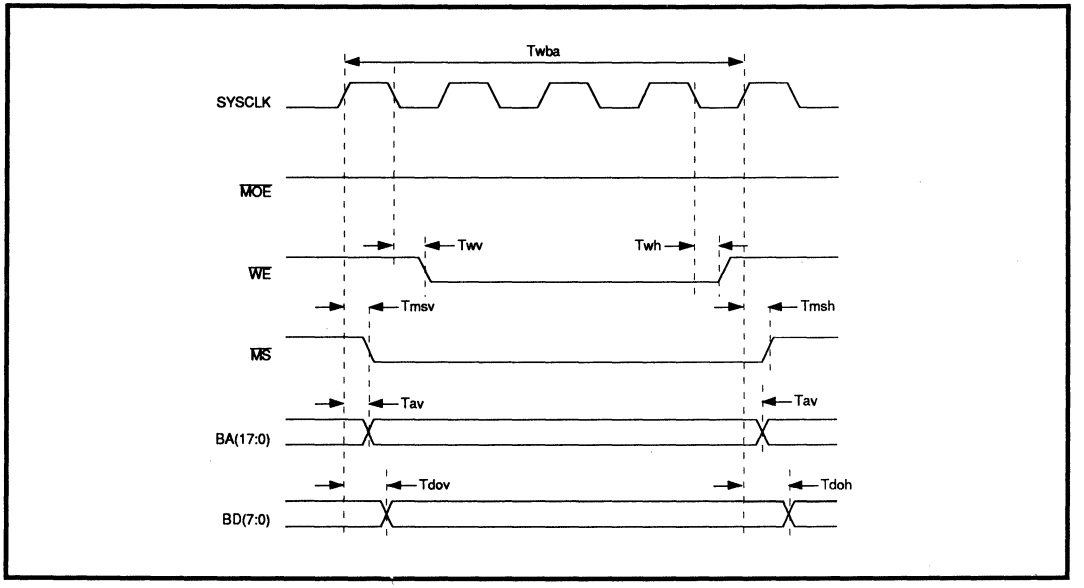



**FIGURE 10: SRAM Write Timing**

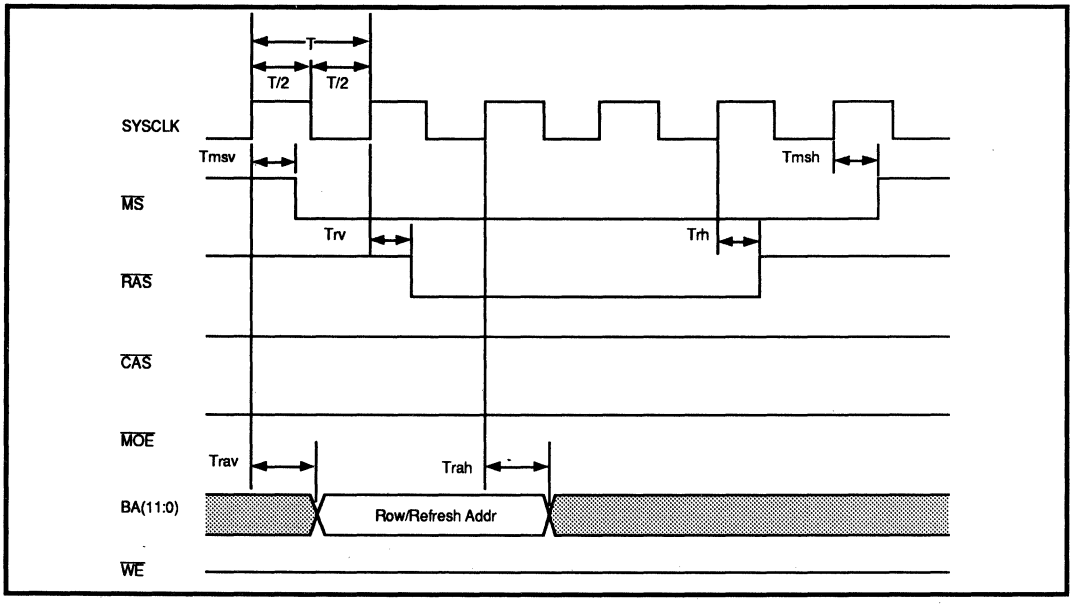



**FIGURE 11: DRAM Timing, Refresh Cycle (Shown with WRL = 0)**

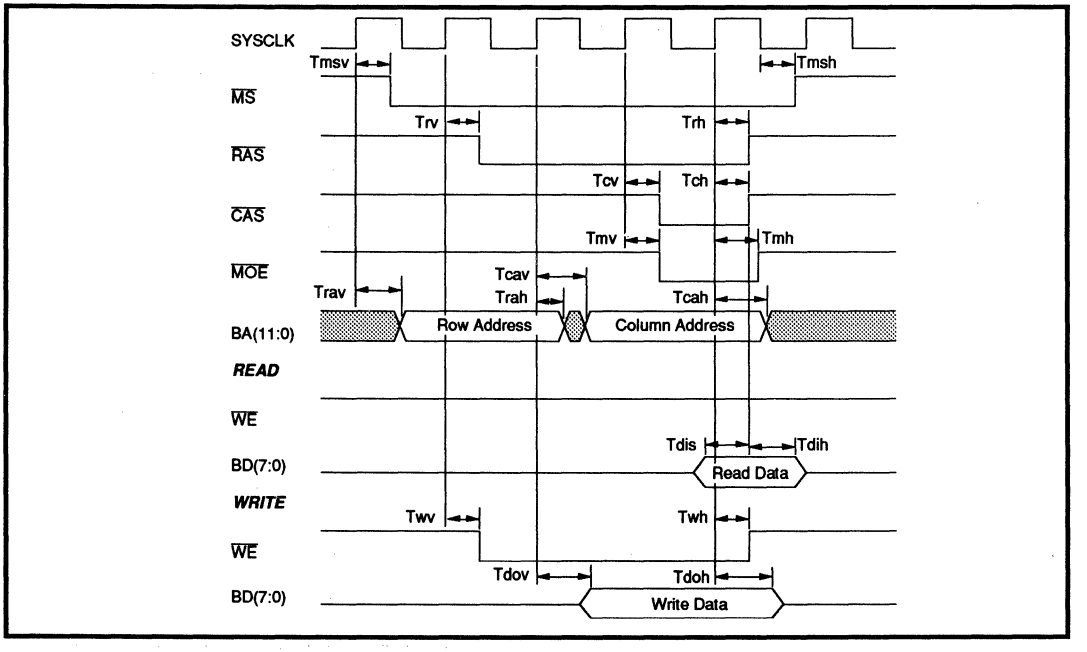



**FIGURE 12: DRAM Timing, Standard Cycle (Shown with RWL = 0 and CWL = 0)**

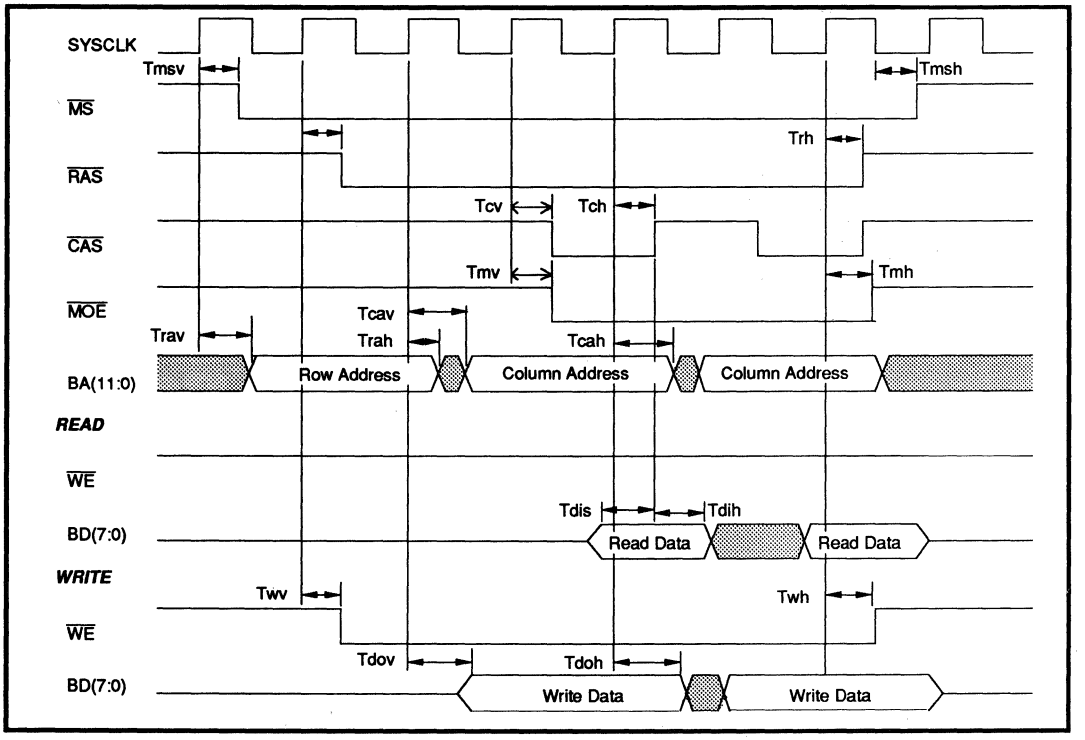



**FIGURE 13: DRAM Timing, Fast Page Cycles (Shown with RWL = 0, RWH = 0, CWL = 0 and CWH = 0)**

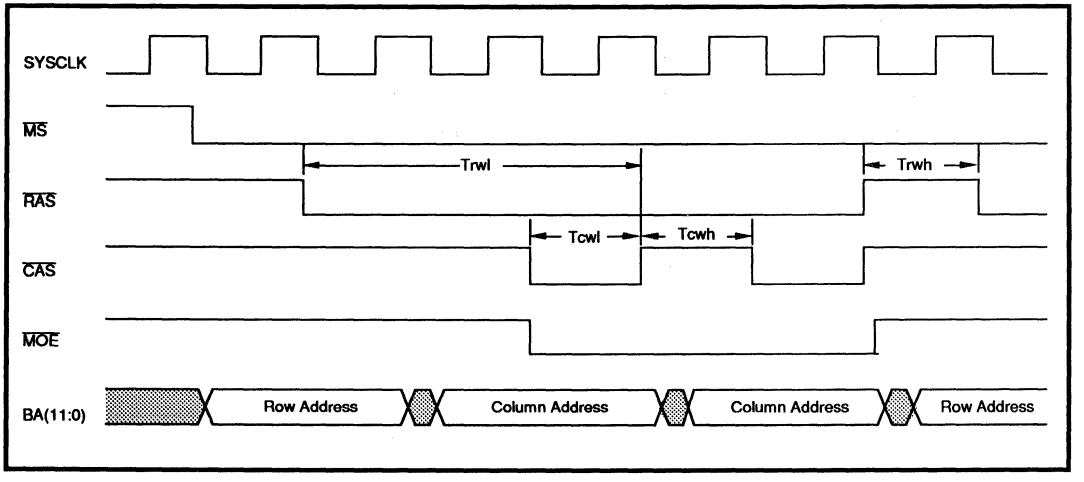



**FIGURE 14: DRAM Timing (Showing the Relationship of RWL, RWH, CWL and CWH to overall timing)**

## ELECTRICAL SPECIFICATIONS (continued)

| PARAMETER | | MIN (Fast) | MAX (Fast) | MIN (Slow) | MAX (Slow) | UNIT |
|---|---|---|---|---|---|---|
| Trh | $\overline{REQ}$ Assertion Time | 37 | 48 | | | ns |
| Trl | $\overline{REQ}$ Deassertion Time | 63 | 52 | | | ns |
| Tids | Setup time SCSI Data to $\overline{REQ}$\ (write to SCSI bus) | 43 | | | | ns |
| Tidh | Hold time $\overline{REQ}$\ to SCSI Data invalid (write to bus) | 43 | | | | ns |
| Tal | Minimum $\overline{ACK}$ Assertion Width Required | 10 | | | | ns |
| Tods | Data Hold from $\overline{ACK}$\ (Read from the SCSI bus) | 5 | | | | ns |
| Todh | Data Hold from $\overline{ACK}$\ (Read from the SCSI bus) | 12 | | | | ns |
| Note: All timing parameters are measured with 200 pF load, two SCSI terminator loads, $\overline{ACK}$ filter turned off. | | | | | | |

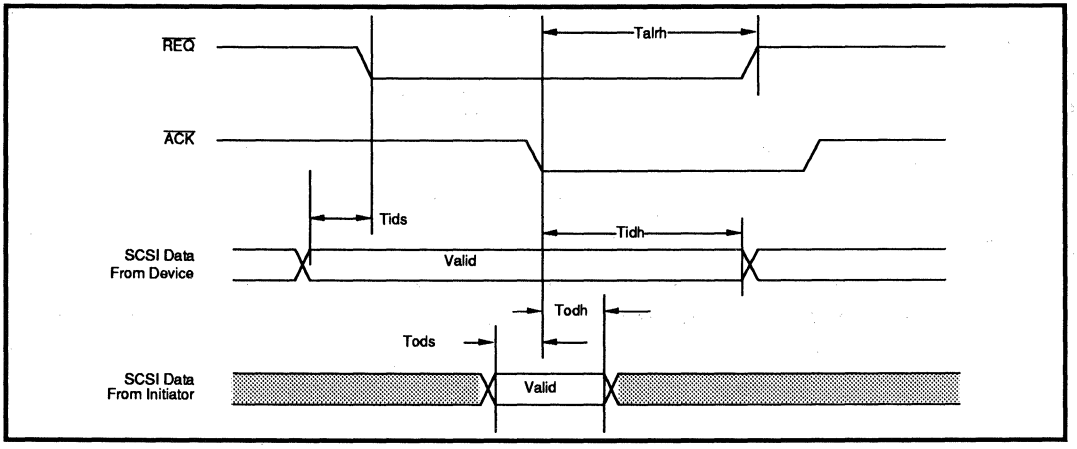



**FIGURE 15: SCSI Synchronous Timing**

## ELECTRICAL SPECIFICATIONS (continued)

| PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Tods | Data Setup to $\overline{ACK}$\ (SCSI Output phase) | 5 | | ns |
| Todh | Data Hold form $\overline{ACK}$\ (SCSI Output phase) | 12 | | ns |
| Talrh | $\overline{ACK}$\ to $\overline{REQ}$/ | | 49 | ns |
| Tids | Data Setup to $\overline{REQ}$\ (SCSI Input phase) | 80 | | ns |
| Tidh | Data Hold from $\overline{ACK}$\ (SCSI Input phase) | 29 | | ns |
| Note: All timing parameters are measured with 200 pF load, two SCSI terminator loads, $\overline{ACK}$ filter turned off. | | | | |

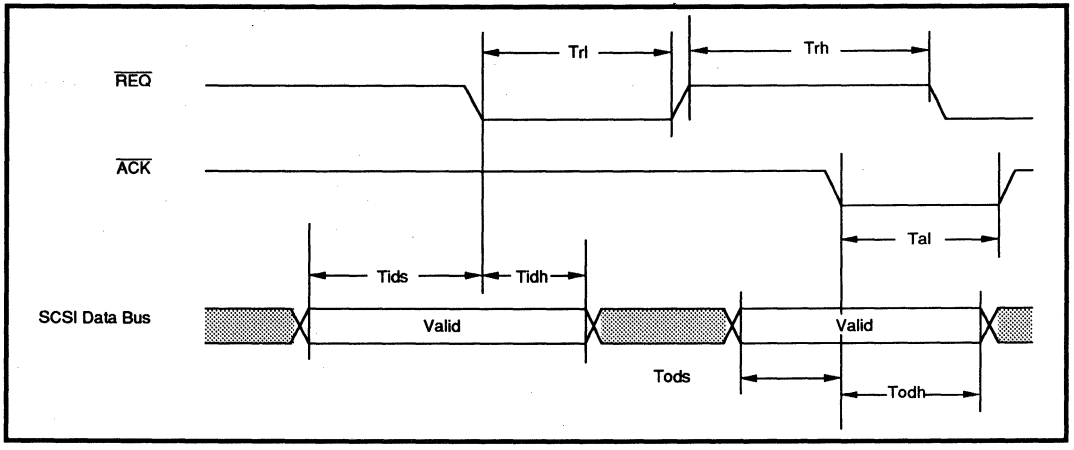



FIGURE 16: SCSI Asynchronous Timing

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**Synchronous Data In/Out Phase**

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|---|
| Txtrp* | Synchronous Transfer Period | (see note) | | | | ns |
| Tsrl | SYSFREQ high to $\overline{REQ}$ low | | | | 50 | |
| Tsrh | SYSFREQ high to $\overline{REQ}$ high | | | | 60 | ns |
| Tdov | SYSFREQ high to data out valid | | | | 40 | ns |
| Tdsu | Data setup to $\overline{ACK}$ low | | 55 | | | ns |
| Tdh | Data hold from $\overline{ACK}$ low | | 40 | | | ns |

Note: Txtrp is the Synchronous Transfer Period as defined by the Synchronous Control Register (Reg: 43H). SYSFREQ is a function of the BUFCLK and is determined by the prescale value as defined by the Clock Control Register (Reg: 49H).

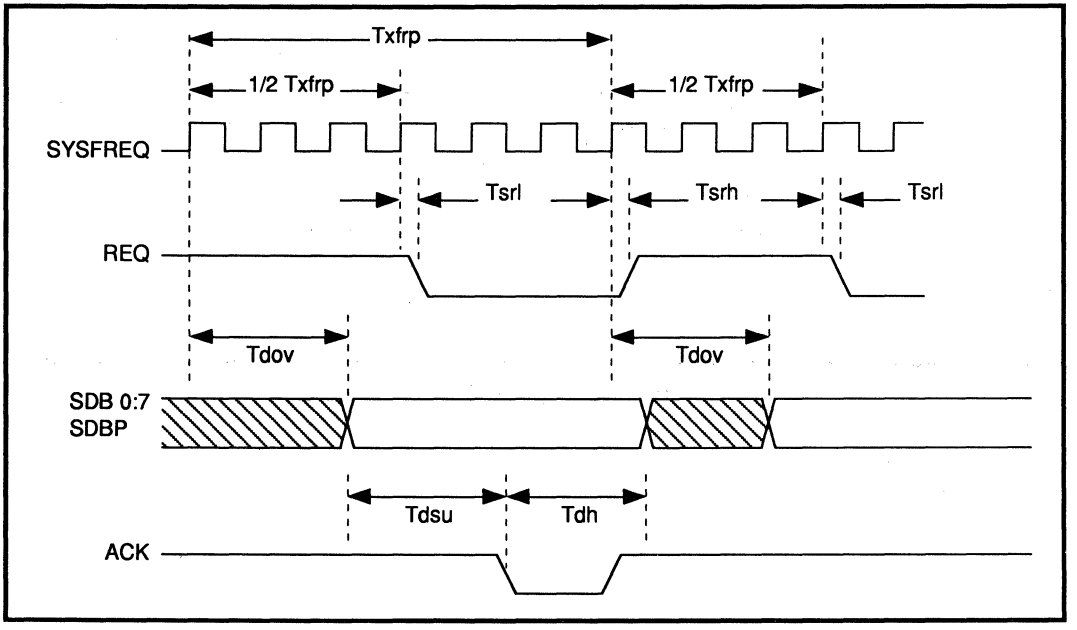



**FIGURE 17: Even Number of SYSFREQ Cycles/SCSI Transfer Period**

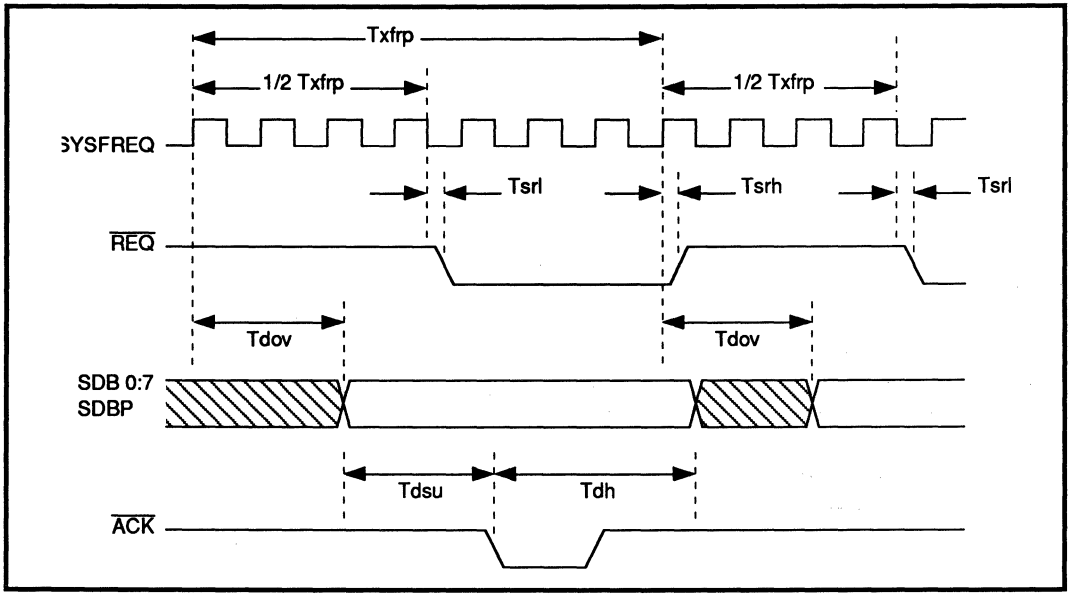



**FIGURE 18: Odd Number of SYSFREQ Cycles/SCSI Transfer Period**

8

**Wait for Selection**

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|---|
| Tbsd | Bus Settle Delay (400 ns) to the assertion of $\overline{BSY}$ | | 3T + 90 | | 4T + 90 | ns |
| Note: T is the SCSI Clock Period (SCP) as defined in Register 49H (CLKCTL). | | | | | | |

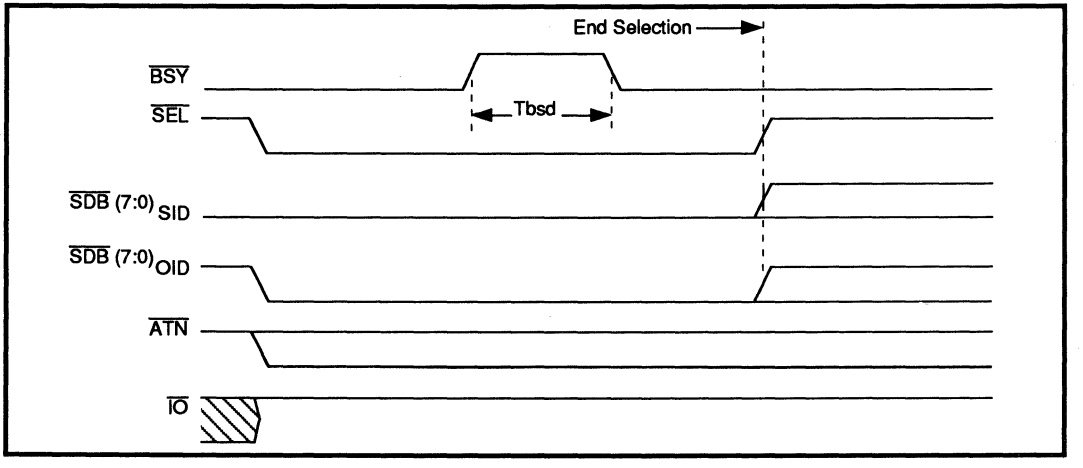



**FIGURE 19: Wait for Selection**

**Arbitration**

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|---|
| Tbfsd | Bus Settle Delay (400 ns) + Bus Free Delay (800 ns) to the assertion of BSY and $\overline{SDB}_{OID}$ | | 6T + 110 | | 7T + 110 | ns |
| Tad | Arbitration Delay (2.4 µsec) to the assertion of $\overline{SEL}$ (win) or deassertion of $\overline{BSY}$ and $\overline{SDB}_{OID}$ (lost) | | - | | 13T + 100 | ns |
| Tbcsd | Bus Clear Delay (800 ns)+ Bus Settle Delay (400 ns) to end of Arbitration Phase | | - | | 6T + 100 | ns |
| Note: T is the SCSI Clock Period (SCP) as defined in Register 61H (CLKCTL). | | | | | | |

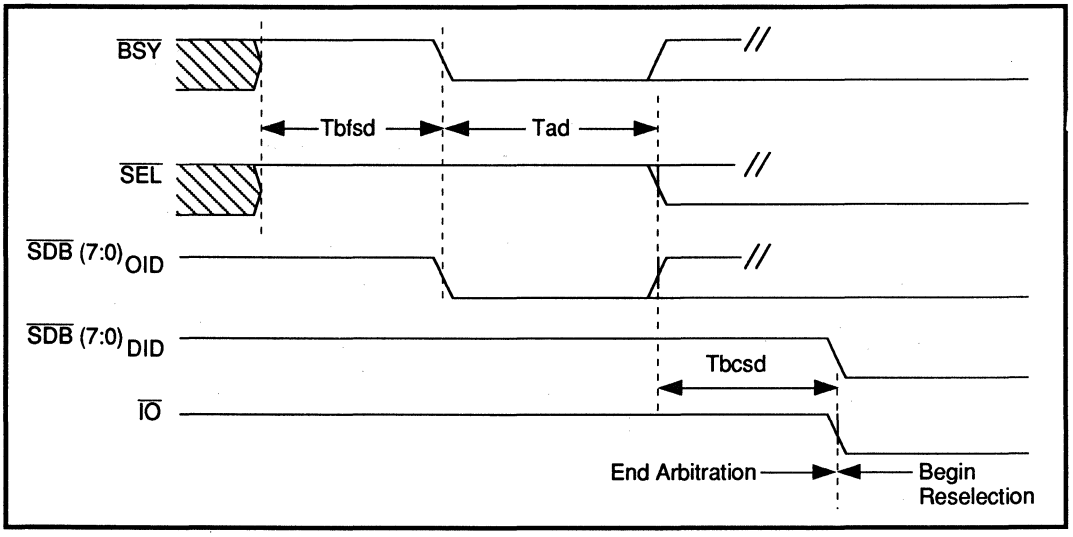



**FIGURE 20: Arbitration**

**Reselection**

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|---|
| Tbcsd | Bus Clear Delay (800 ns) + Bus Settle Delay (400 ns) to end of Arbitration Phase | | - | | 6T + 100 | ns |
| Tdskd1 | Two Deskew Delays (90 ns) to the deassertion of $\overline{BSY}$ | | - | | 160 | ns |
| Tbsd | Bus Settle Delay (400 ns) to the assertion of $\overline{BSY}$ | | - | | 2T + 40 | ns |
| Tdskd2 | Two Deskew Delays (90 ns) to the deassertion of SEL, $\overline{SDB}_{OID}$, and $\overline{SDB}_{DID}$ | | 1T +70 | | 2T + 70 | ns |
| Note: T is the SCSI Clock Period (SCP) as defined in Register 61H (CLKCTL). | | | | | | |

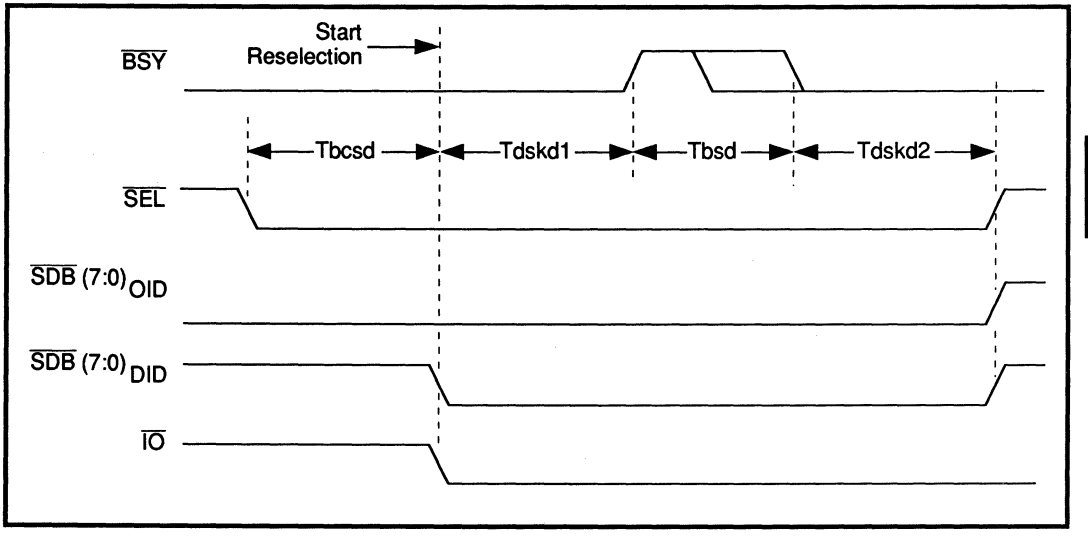
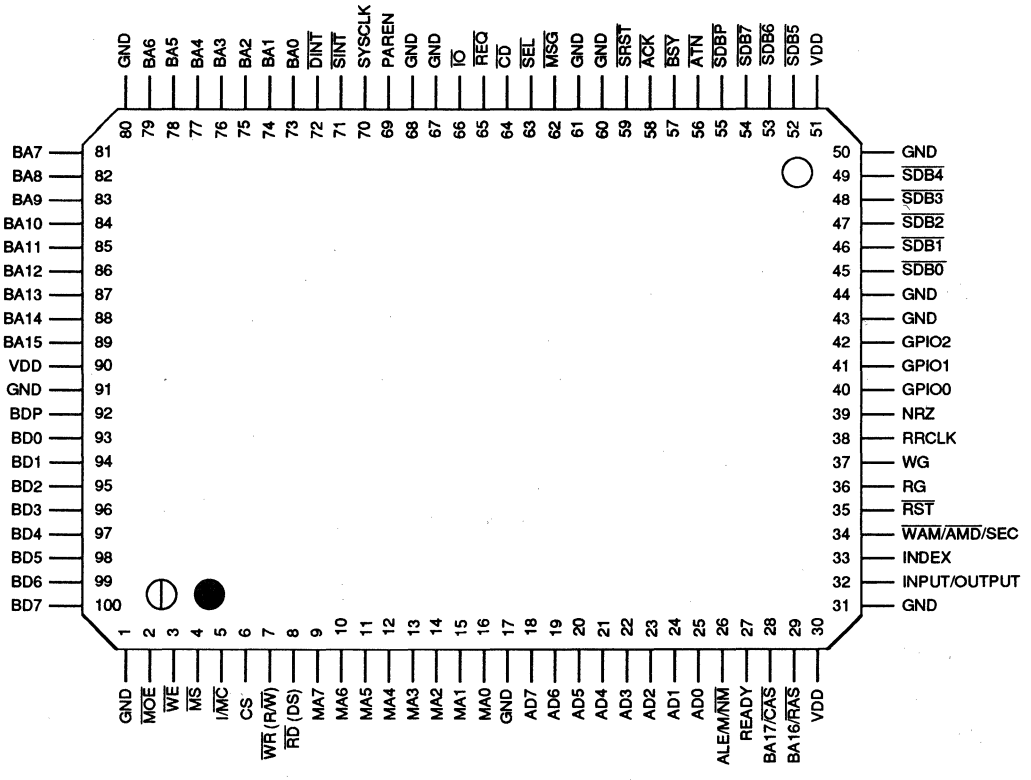



**FIGURE 21: Reselection**

# SSI 32C9020
# SCSI Combo Controller
# 48 Mbit/s; single bit NRZ interface

## PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.




**100-pin QFP**

**Advance Information:** Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.



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A TDK Group Company

# SSI 32C9022
## SCSI Combo Controller
## 48 Mbit/s; dual bit NRZ interface
## Advance Information

January 1993

## DESCRIPTION

The SSI 32C9022 is an advanced CMOS VLSI device which integrates major portions of the hardware needed to build an SCSI disk drive. The circuitry of the SSI 32C9022 includes a complete SCSI target interface, an advanced buffer manager, a high performance disk formatter and an 88 bit Reed-Solomon ECC with fast "on-the-fly" hardware correction. The SSI 32C9022 provides maximum performance while minimizing micro controller intervention.

The SSI 32C9022 provides a Dual Bit Interface to the ENDEC. The Dual Bit Interface allows an effective transfer rate of up to 48 megabits per second on the disk interface by utilizing two parallel NRZ data signals and a clock rate of 24 MHz. The reduction of overall clock rates between the SSI 32C9022 and the ENDEC can be of great benefit to the designer.

The SSI 32C9022 can sustain concurrent transfers of up to 48 megabits per second transfer rate to the disk and 10 megabytes per second across the SCSI bus. In addition, on-the-fly error corrections and micro controller accesses to the buffer memory will not degrade the throughput during transfers.

(continued)

## FEATURES

- **SCSI Bus Interface**
  - **Full SCSI-2 Compatibility**
  - **Direct bus interface logic with on-chip 48 mA drivers**
  - **Synchronous transfer rates up to 10 megabytes per second**
  - **Asynchronous transfer rates up to 5 megabytes per second**
  - **Parity generation and checking**
  - **Auto Command Mode (ACM) SCSI state machine performs high level SCSI sequences without microprocessor intervention**
  - **Four level ACM command FIFO supports automatic execution of multiple ACM commands**
  - **Hardware support for automatic handling of SCSI-2 command queuing**
  - **Automatic SCSI CDB size determination**
  - **Automatic SCSI Disconnect and Reconnect**
  - **Sixteen byte data FIFO between SCSI channel and Buffer Manager**

(continued)

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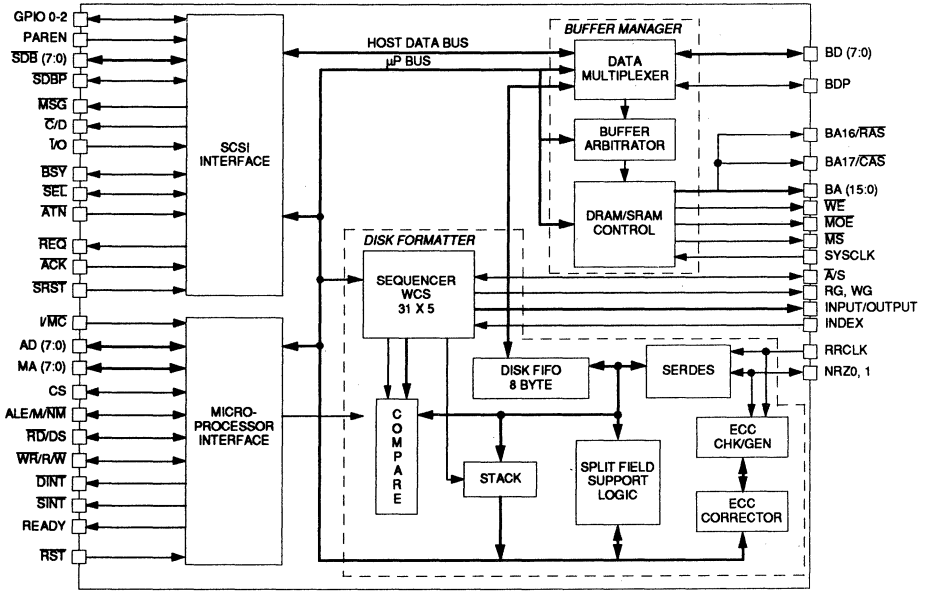
## BLOCK DIAGRAM



# SSI 32C9022
# SCSI Combo Controller
# 48 Mbit/s; dual bit NRZ interface

## DESCRIPTION (continued)

The SSI 32C9022 is one of a family of Silicon Systems' single chip disk controllers which support a wide range of device interfaces. The SSI 32C9020 is similar to the SSI 32C9022, but supports a Single Bit or Serial NRZ interface for applications which require this feature. Other family members support AT and PCMCIA interfaces. All members are based on a common architecture allowing major portions of firmware to be reused. The Silicon Systems' chip family is illustrated in the hierarchy chart shown in Figure 1.

The high level of integration within the SSI 32C9022 represents a major reduction in parts count. When the SSI 32C9022 SCSI Controller is combined with the SSI 32R2010 Read/Write device, the SSI 32P3000 Pulse Detector, the SSI 32D5392 Dual Bit Data Synchronizer with 1,7 ENDEC, the 32H4631 Servo and Motor Speed Controller, an appropriate micro controller and memory, a complete, cost efficient, high performance intelligent drive solution is created.

## FEATURES (continued)

- **Buffer Manager**
  - **Direct support of DRAM or SRAM**
    - **SRAM throughput to 20 megabytes per second**
    - **SRAM size up to 256k bytes**
    - **DRAM throughput to 17.78 megabytes per second**
    - **DRAM size up to 1 megabyte**
  - **Programmable memory timing**
  - **Buffer RAM segmentation with flexible segment sizes from 256 bytes to 1 megabyte**
  - **Dedicated host, disk and microprocessor address pointers**
  - **Internal buffer protection circuit provides buffer integrity**
- **Disk Formatter**
  - **Dual Bit NRZ Interface**
  - **Effective Data Rates to 48 megabits/s (24 MHz Dual Bit Transfers)**
  - **Automatic multi-sector transfer**
  - **Header or microprocessor based split data field support**
  - **Advanced sequencer organized in 31 x 5 bytes**
  - **88-bit Reed Solomon ECC with "on-the-fly" fast hardware correction circuitry**
  - **Capable of correcting up to four 10-bit symbols in error**
  - **Guaranteed to correct one 31-bit burst or two 11-bit bursts**
  - **Hardware on-the-fly correction of either an 11- or 31-bit single burst error within a half sector time**
  - **Detects up to one 51-bit burst or three 11-bit bursts**
- **Microprocessor Interface**
  - **Supports both multiplexed or non-multiplexed microprocessors**
  - **Separate or combined host and disk interrupts**
  - **Programmable wait state insertion**
- **Other Features**
  - **Internal power down mode**
  - **Available in 128-pin QFP**

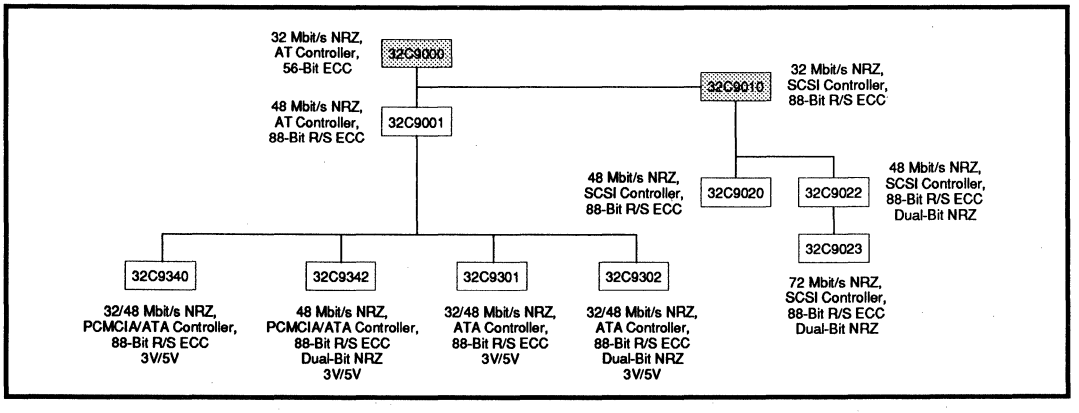



**FIGURE 1: Silicon Systems' Single Chip Controller Hierarchy**

## FUNCTIONAL DESCRIPTION

The SSI 32C9022 contains the following four major functional blocks:

Microcontroller Interface
SCSI Interface
Disk Formatter
Buffer Manager

The Microprocessor Interface allows the local microprocessor access to all of the SSI 32C9022 internal control registers and any location within the buffer memory. The microprocessor, by writing and reading the internal registers can control all activities of the SSI 32C9022. The microprocessor can elect to perform SCSI and/or disk operations directly, or it can enable the advanced features of the SSI 32C9022 which can perform all typical operations automatically.

The SCSI Interface block handles all SCSI activities. The SCSI interface includes 48 mA drivers allowing for direct connection of the SSI 32C9022 to the SCSI bus. The SCSI interface logic includes Auto Command Mode (ACM) logic, an advanced state machine capable of handling a variety of complex SCSI sequences without microprocessor intervention. The microprocessor can queue up to four ACM commands into the ACM Command FIFO to create even more sophisticated command sequences. The SCSI block interfaces directly with the Buffer Manager via an internal speed matching FIFO. This FIFO, plus the bandwidth capabilities of the Buffer Manager guarantee sustained full speed transfers across the SCSI bus. The high level of automation of the ACM minimizes SCSI bus overhead. The net result is maximized performance with minimum SCSI bus band width utilization.

The Disk Formatter performs the serialization and deserialization of data. It provides all of the necessary functions to control track formatting, header search, and the reading and writing of data. The heart of the Disk Formatter is an advanced programmable sequencer which is flexible enough to interface to a wide variety of read/write channels. The sequencer can contain 31 instructions, each of which is 5 bytes (40 bits) in width. The width of the instructions allows for sophisticated branching techniques which increase the flexibility and power of the sequencer. The flexible disk interface can be configured through a wide range of capabilities. This allows the SSI 32C9022 to interface with nearly any read/write channel and allows the user of the SSI 32C9022 to select the read/write channel best suited to the device. Of course, by selecting the SSI 32C9022 controller and the SSI 32D5392 Data Synchronizer with 1,7 ENDEC, you are guaranteed a problem free interface.

Within the Disk Formatter are the ECC generator/checker and ECC corrector. The generator/checker provides the ability to generate or check a 32 bit ECC for headers and an 88 bit Reed Solomon code for data. If the checker detects an error in an 88 bit Reed Solomon data field, the syndrome information is transferred into the corrector. The corrector performs the necessary operations to determine if the error was correctable and interfaces directly with the buffer controller to perform the correction automatically. The corrector performs its correction within one half of a sector time. This guarantees that the corrector will always be available to correct the next sector if necessary.

As its name implies, the Buffer Manager manages the data buffer of the controller. The Buffer Manager can support either SRAM or DRAM. When configured to operate with DRAM, the Buffer Manager automatically performs necessary refresh cycles. The Buffer Manager creates all of the necessary timing and control signals for a wide range of memory types and speeds. The Buffer Manager interfaces with the buffer memory, the SCSI Interface block, the data path of the Disk Formatter block, the ECC corrector and the microprocessor. If more than one of these devices requires access to the buffer memory, the Buffer Manager arbitrates the requests automatically. The Buffer Manager of the SSI 32C9022 can sustain SCSI operations at the rate of 10 megabytes per second, Disk Formatter operations at 48 megabits per second (6 megabytes per second) and still have sufficient band width left to handle on-the-fly ECC corrections and microprocessor accesses without degrading performance on any of the interfaces.

## PIN DESCRIPTION

The following convention is used in the pin description:

(I) denotes an input
(O) denotes an output
(Z) denotes a tri-state output
(OD) denotes an open drain output

### GENERAL

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| VDD | | POWER SUPPLY PIN, VCC |
| GND | | GROUND |

### HOST INTERFACE

| | | |
|---|---|---|
| $\overline{SDBP}$ | I/O | SCSI DATA BUS PARITY. Odd parity bit for the SCSI data bus. |
| $\overline{SDB(7:0)}$ | I/O | SCSI DATA BUS BITS 7-0. |
| $\overline{ATN}$ | I | ATTENTION. This active low signal is used by the initiator to request a message out phase. |
| $\overline{BSY}$ | I/O | BUSY. This active low signal is used to indicate when the bus is active. |
| $\overline{ACK}$ | I | ACKNOWLEDGE. This active low signal is used in the handshake protocol to indicate the completion of a data byte transfer. |
| $\overline{SRST}$ | I | SCSI RESET. This active low signal is used to reset the SCSI controller. |
| $\overline{MSG}$ | O | MESSAGE. This active low signal is used to indicate a message phase. |
| $\overline{SEL}$ | I/O | SELECT. This active low signal is used to indicate either a selection or reselection phase. |
| $\overline{C}$/D | O | COMMAND/DATA. This signal is used to indicate either a command or data phase. |
| $\overline{REQ}$ | I | REQUEST. This active low signal is used in the handshake protocol to initiate a data byte transfer. |
| $\overline{I}$/O | I | INPUT/OUTPUT. This signal is used to indicate the direction of data transfer. |
| PAREN | I | SCSI PARITY ENABLE. This active high signal is used to enable parity checking of the SCSI data bus. Parity checking is disabled when this pin is held low. |
| GPIO(2:0) | I/O | INPUT/OUTPUT. These pins are used to indicate the SCSI ID of the target device. The pins can be programmed as outputs for test purposes only. |

### DISK INTERFACE

| | | |
|---|---|---|
| INDEX | I | INDEX. Input for index pulse received from the drive. |
| INPUT/ OUTPUT | I/O | DISK SEQUENCER INPUT/OUTPUT. A general purpose control (output) and status (input) pin configured by the Output Enable Bit of Register 71H, bit 7.<br>At power-on, this pin is an input. As an input, it can be used to synchronize the disk sequencer to an external event. As an output, it is controlled by bit 2 of the Control Field of the disk sequencer. |
| $\overline{AMD}$/ SECTOR | I/O | ADDRESS MARK DETECT/SECTOR. This pin is used in the hard sector mode as the sector input. A pulse on this pin indicates a sector mark is found.<br>In the soft sector mode, a low-level input indicates an address mark was detected. The device powers up in soft sector default mode. |

**DISK INTERFACE** (continued)

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| RG | O | READ GATE. During disk data read, this pin is asserted. Active high. |
| WG | O | WRITE GATE. During disk data write, this pin is asserted. Active high. |
| RRCLK | I | READ/REFERENCE CLOCK. This is a clock signal generated from an external data synchronizer. This clock is used to synchronize the input NRZ data and clock the disk formatter of the chip. |
| WCLK | O | WRITE CLOCK. This signal clocks the NRZ data out in the dual NRZ interface mode. |
| NRZ1 | I/O | NON RETURN TO ZERO 1. In dual NRZ mode, this signal is the most significant bit read data input from the disk drive when the read gate signal is asserted; it is the most significant bit write data output to the disk drive when the write gate signal is asserted. In single NRZ mode, this signal is not used and should be grounded. NRZ1 is the leading bit of the bit pair. In Write mode, the MSB of the data bytes always appears on NRZ1. |
| NRZ | I/O | NON RETURN TO ZERO. In dual NRZ mode, this signal is the least significant bit read data input from the disk drive when the read gate signal is asserted; it is the least significant bit write data output to the disk drive when the write gate signal is asserted. In single NRZ mode, this signal is used to transfer NRZ data to/from the read channel chip. |

**MICROPROCESSOR INTERFACE**

| | | |
|---|---|---|
| $\overline{RST}$ | I | RESET. An asserted low input generates a component reset that holds the internal registers at reset, stops all operations within the chip, and deasserts all output signals. All input/output signals are set to the high-Z state during the assertion of this signal. |
| ALE/M/$\overline{NM}$ | I | ADDRESS LATCH ENABLE/MULTIPLEXED/NON-MULTIPLEXED ADDRESS SELECT. When tied high or left floating after reset, the microprocessor interface is configured as non-multiplexed. When driven low, then the microprocessor interface is configured as multiplexed. In this case this pin functions as the address latch enable, and the MA(7:0) pins are the demultiplexed address outputs. |
| CS | I | CHIP SELECT. Active high signal, when asserted, the internal registers of the SSI 32C9022 can be accessed. |
| $\overline{WR}$/R/$\overline{W}$ | I | WRITE STROBE/READ/WRITE. In the Intel bus mode, when an active low signal is present with CS signal high, the data is written to the internal registers.<br>In the Motorola bus mode, this signal acts as the R/$\overline{W}$ signal. |
| $\overline{RD}$/DS | I | READ STROBE/DATA STROBE. In the Intel bus mode, when an active low signal is present with CS signal high, internal register data is read.<br>In the Motorola mode, this signal acts as the DS signal. DS when active high is data strobe. |
| $\overline{DINT}$ | O, OD,Z | DISK INTERRUPT. An active low signal indicates the controller is requesting microprocessor service from the disk side. This signal is programmable for either a push-pull or open-drain output circuit. This signal powers up in the high-Z state. Register 4F bit 3 enables the pull-up. |

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**MICROPROCESSOR INTERFACE** (continued)

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| $\overline{SINT}$ | O, OD,Z | SCSI INTERRUPT. This signal is generated by the SCSI controller and is an interrupt line to the microprocessor. It is programmable for either a push-pull or open drain output circuit. This signal powers up in the high-Z state. The interrupt is sourced from the SCSI Interrupt Register. Register 4F bit 3 enables the pull-up. This signal is also programmable to be either an active high or low interrupt. |
| AD(7:0) | I/O | ADDRESS/DATA BUS. When configured in the Intel mode, these lines are multiplexed, bidirectional microprocessor register address and data lines.<br>When configured in the Motorola mode, these lines are bidirectional data lines. |
| MA(7:0) | I/O | MICROPROCESSOR ADDRESS BUS: These signals are nonmultiplexed address input or latched address output lines. |
| READY | O | READY: When this signal is deasserted low, the microprocessor shall insert wait states to allow time for the chip to respond. |
| I/$\overline{MC}$ | I | INTEL/MOTOROLA: This signal selects the microprocessor interface to be used. When this signal is asserted high, it selects the Intel bus control interface. When this signal is deasserted low, it selects the Motorola bus control interface. This signal has an internal pull-up to allow the default selection of the Intel bus control interface. |

**BUFFER MANAGER INTERFACE**

| | | |
|---|---|---|
| BA(15:0) | O | BUFFER MEMORY ADDRESS LINES 15 through 0. Active high, for direct connection to a Static or Dynamic RAM address lines. |
| BA16/$\overline{RAS}$ | O | BUFFER MEMORY ADDRESS 16: In SRAM mode, for direct connection to a Static RAM address line 16.<br>ROW ADDRESS STROBE: In DRAM mode, for direct connection to a Dynamic RAM Row Address Strobe signal. |
| BA17/$\overline{CAS}$ | O | BUFFER MEMORY ADDRESS 17: In SRAM mode, for direct connection to a Static RAM address line 17.<br>ROW ADDRESS STROBE: In DRAM mode, active low, for direct connection to a Dynamic RAM Column Address Strobe signal. |
| BD(7:0) | I/O | BUFFER MEMORY DATA BUS. 7 through 0. Active high, buffer data bus that connects directly to the buffer RAM data lines. |
| BDP | I/O | BUFFER MEMORY DATA PARITY. This signal provides odd parity for the buffer memory data bus during transfers to/from the buffer memory to the buffer RAM. |
| $\overline{MOE}$ | O | MEMORY OUTPUT ENABLE. In SRAM mode this signal is asserted low when every buffer memory access is active. In DRAM mode this signal is asserted low only for buffer memory read operation. |
| $\overline{MS}$ | O | MEMORY SELECT. An active low signal indicates external memory is selected. |
| $\overline{WE}$ | O | WRITE ENABLE. Active low, write enable for the buffer RAM. |
| SYSCLK | I | SYSTEM CLOCK. This signal is used to synchronize the buffer RAM access, including the generation of memory address bits, write enable $\overline{WE}$, and memory output enable $\overline{MOE}$. |

## ELECTRICAL SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS

Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC operating characteristics.

| PARAMETER | RATING |
|---|---|
| Power Supply Voltage, VCC | 7V |
| Ambient Temperature | 0 to 70°C |
| Storage Temperature | -65 to 150°C |
| Power Dissipation | 750 mW |
| Input, Output pins | -0.5 to VCC+0.5V |

### ELECTRICAL CHARACTERISTICS

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|
| VCC Power Supply Voltage | | 4.50 | | 5.50 | V |
| ICC Supply Current | Ta = 25°C Outputs Unloaded | | | 50 | mA |
| ICCS Supply Current | | | | 500 | µA |
| VIL Input Low Voltage | | -0.5 | | 0.8 | V |
| V0IH Input High Voltage | | 2.0 | | VCC+0.5 | V |
| VOL Output Low Voltage | All pins except SCSI interface, IOL = 2 mA | | | 0.4 | V |
| VOL Output Low Voltage | SCSI interface pins, IOL = 48 mA | | | 0.5 | V |
| VOH Output High Voltage | IOH = -400 µA | | | 2.4 | V |
| IL Input Leakage Current | 0 < VIN < VCC | -10 | | 10 | µA |
| CIN Input Capacitance | | | | 10 | pF |
| COUT Output Capacitance | | | | 10 | pF |

8

**MICROPROCESSOR INTERFACE TIMING**

**Multiplexed Interface Timing Parameters (Figures 2-5)**

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|---|
| Ta | ALE width | | 20 | | | ns |
| Tma | Address valid to MA(7:0) valid | | | | 30 | ns |
| Tr | $\overline{RD}$ width | | 80 | | | ns |
| As | Address valid to ALE ↓ | | 5 | | | ns |
| Ah | ALE ↓ to address invalid | | 10 | | | ns |
| Cs | CS valid to $\overline{RD}$ ↓ or DS ↑ | | 20 | | | ns |
| Ch | $\overline{RD}$ ↑ or DS ↓ to CS ↓ | | 0 | | | ns |
| Tda | $\overline{RD}$ ↓ or DS ↑ to read data valid | | | | 60 | ns |
| Tds | DS width | | 80 | | | ns |
| Tdh | $\overline{RD}$ ↑ or DS ↓ to read data invalid | | 0 | | 25 | ns |
| Tsrw | R/$\overline{W}$ valid to DS ↑ | | 20 | | | ns |
| Thrw | DS ↓ to R/$\overline{W}$ invalid | | 20 | | | ns |
| Tdrdy | $\overline{RD}$ ↓ to READY ↓ (Intel) or DS ↑ to READY ↓ (Motorola) | | | | 30 | ns |
| Wds | Write data valid to $\overline{WR}$ ↑ or DS ↓ | | 40 | | | ns |
| Wdh | $\overline{WR}$ ↑ or DS ↓ to write data invalid | | 10 | | | ns |

Note: ↑ indicates rising edge ↓ indicates falling edge

**Non-Multiplexed Bus Interface Timings (Figure 6)**

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|---|
| Tmas | MA(7:0) valid to DS ↓ | | 5 | | | ns |
| Tmah | DS ↑ to MA(7:0) invalid | | 5 | | | ns |
| Cs | CS valid to DS ↓ | | 20 | | | ns |
| Ch | DS ↑ to CS ↓ | | 0 | | | ns |
| Tda | DS ↑ to read data valid | | | | 60 | ns |
| Tds | DS width | | 80 | | | ns |
| Tdh | DS ↑ to read data invalid | | 0 | | 25 | ns |
| Tsrw | R/$\overline{W}$ valid to DS ↓ | | 20 | | | ns |
| Thrw | DS ↑ to R/$\overline{W}$ invalid | | 20 | | | ns |
| Tdrdy | DS ↑ to READY ↓ (Motorola) | | | | 30 | ns |
| Wds | Write data valid to $\overline{WR}$ ↑ or DS ↓ | | 40 | | | ns |
| Wdh | $\overline{WR}$ ↑ or DS ↓ to write data invalid | | 10 | | | ns |

Note 1: ↑ indicates rising edge ↓ indicates falling edge

Note 2: Loading capacitor = 30 pF

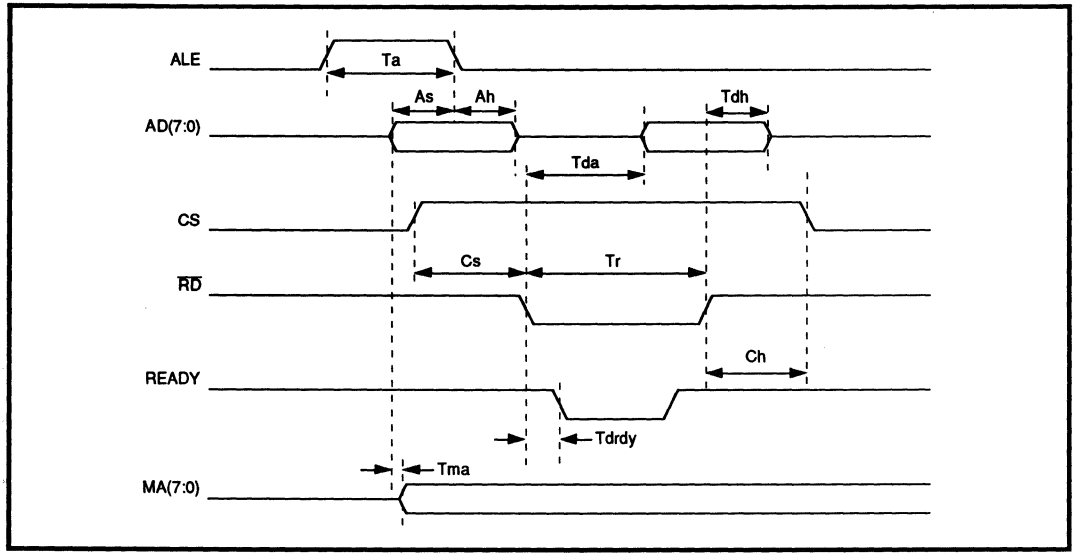


**FIGURE 2: Intel Register Multiplexed Read Timing**

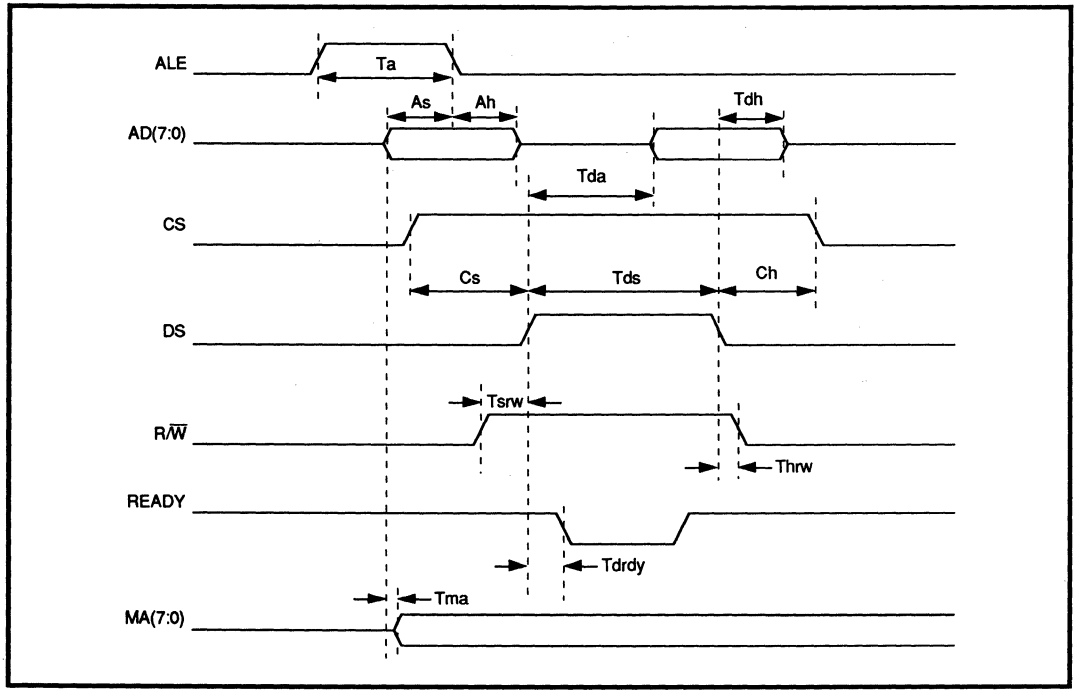


**FIGURE 3: Motorola Register Multiplexed Read Timing**

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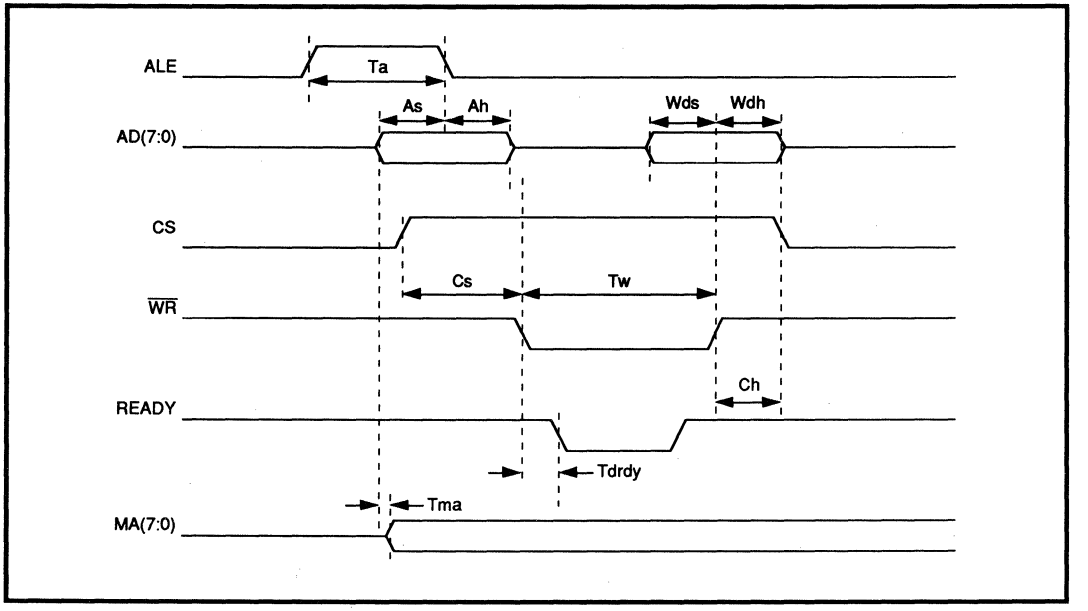


**FIGURE 4: Intel Register Multiplexed Write Timing**

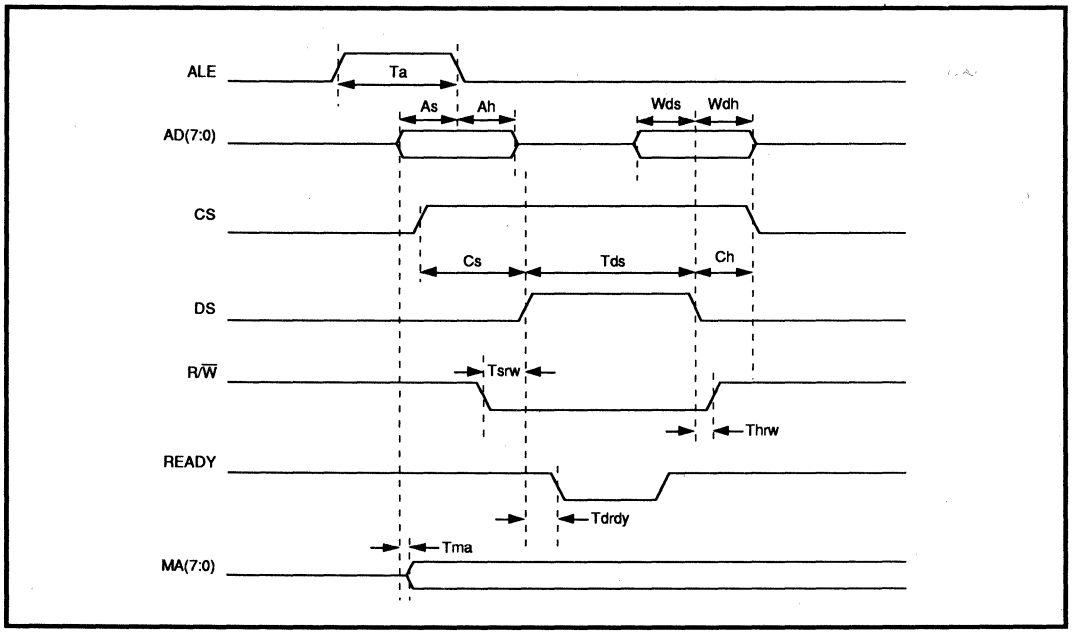


**FIGURE 5: Motorola Register Multiplexed Write Timing**

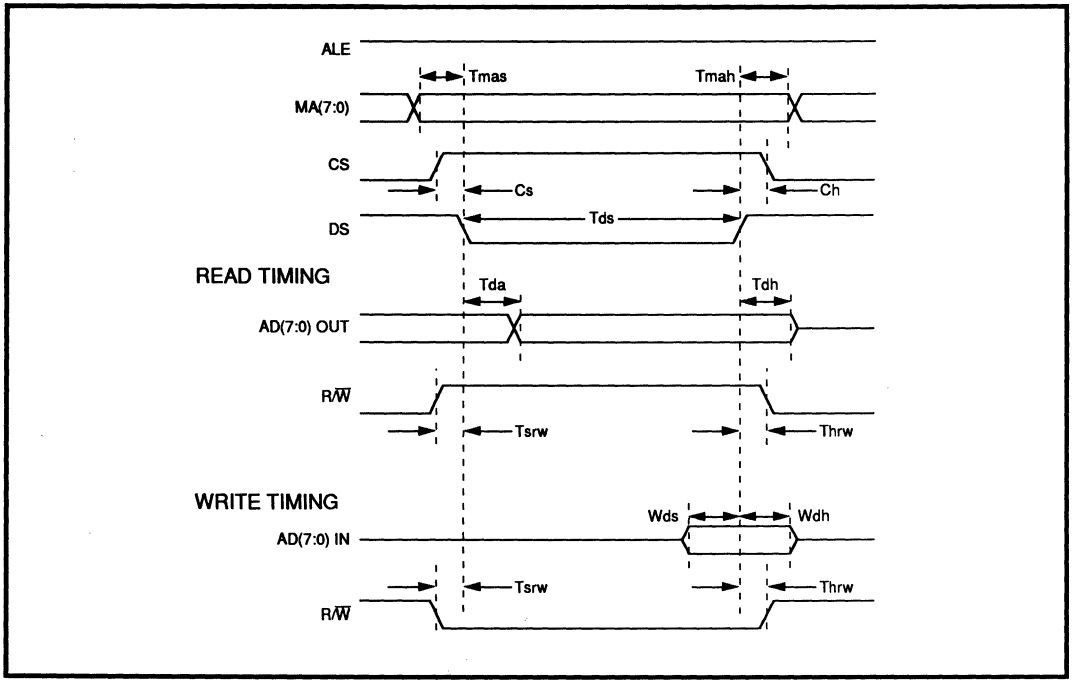


**FIGURE 6: Non-Multiplexed Bus Timing Diagrams**

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## ELECTRICAL SPECIFICATIONS (continued)

### Disk Interface Timing

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|---|
| T | RRCLK period | | 41 | | | ns |
| T/2 | RRCLK high/low time | | 18 | | | ns |
| Tr, Tf | RRCLK rise/fall time | | | | 3 | ns |
| Dis | NRZ in valid to RRCLK ↑ | | 3 | | | ns |
| Dih | RRCLK ↑ to NRZ in invalid | | 3 | | | ns |
| As | $\overline{AMD}$ valid to RRCLK ↑ | | 3 | | | ns |
| Tckd | RRCLK ↓ to WCLK ↓ or RRCLK ↑ to WCLK ↑ | | | | 8 | ns |
| Dv | WCLK ↓ to NRZ out valid | | | | ±1 | ns |

Note: ↑ indicates rising edge ↓ indicates falling edge

Loading capacitor = 10 pF

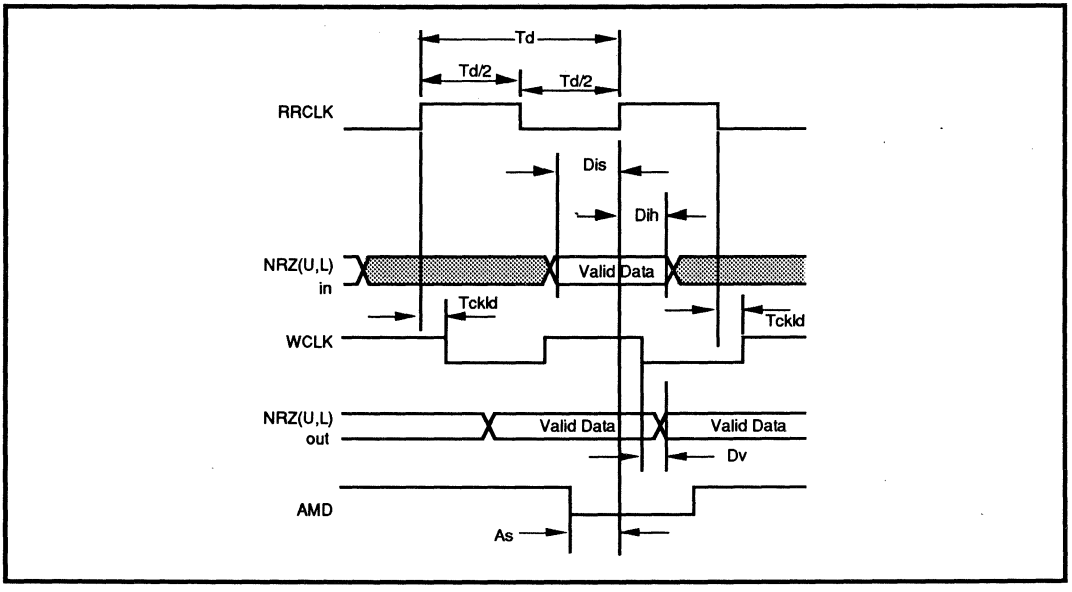



**FIGURE 7: Disk Interface Timing**

**BUFFER MEMORY READ/WRITE TIMING PARAMETERS**

| PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|
| T | SYSCLK period | 25 | | ns |
| T/2 | SYSCLK high/low time | 10 | | ns |
| Tav | SYSCLK / to address valid (Note 1) | | 18 | ns |
| Tmsv | SYSCLK / to $\overline{MS}$\ (Notes 1, 6) | | 18 | ns |
| Tmsh | SYSCLK / to $\overline{MS}$/ (Note 1) | | 18 | ns |
| Tmv | SYSCLK / to $\overline{MOE}$\ (Note 1) | | 18 | ns |
| Tmh | SYSCLK / to $\overline{MOE}$/ (Note 1) | | 18 | ns |
| Twv | SYSCLK / to $\overline{WE}$\ (Note 1) | | 18 | ns |
| Twh | SYSCLK / to $\overline{WE}$/ (Note 1) | | 18 | ns |
| Tdov | SYSCLK to data out valid (Note 1) | | 18 | ns |
| Tdoh | SYSCLK to data out invalid (Note 1) | | 18 | ns |
| Tdis | Data in valid to $\overline{MOE}$ / (SRAM)<br>Data in valid to $\overline{CAS}$ / (DRAM) | 5 | | ns |
| Tdih | $\overline{MOE}$ / to data in valid (SRAM)<br>$\overline{CAS}$ / to data in valid (DRAM) | 0 | | ns |
| Trv | SYSCLK / to $\overline{RAS}$\ (Note 1) | | 18 | ns |
| Trh | SYSCLK / to $\overline{RAS}$/ (Note 1) | | 18 | ns |
| Trav | SYSCLK to row address valid (Note 1) | | 18 | ns |
| Trah | SYSCLK / to row address invalid (Note 1) | | 18 | ns |
| Tcv | SYSCLK / to $\overline{CAS}$\ (Note 1) | | 18 | ns |
| Tch | SYSCLK / to $\overline{CAS}$/ (Note 1) | | 18 | ns |
| Tcav | SYSCLK / to column address valid (Note 1) | | 18 | ns |
| Tcah | SYSCLK / to column address invalid | 0 | | ns |

## ELECTRICAL SPECIFICATIONS (continued)

### BUFFER MEMORY READ/WRITE TIMING PARAMETERS (continued)

| PARAMETER | | CONDITIONS | MIN | UNIT |
|---|---|---|---|---|
| Trwl | $\overline{RAS}$\ to $\overline{RAS}$/ | Notes 2, 3 | (RWL + 3)•T)-2 | ns |
| Trwh | $\overline{RAS}$/ to $\overline{RAS}$\ | Notes 2, 4 | (RWH + 1)•T)-2 | ns |
| Tcwl | $\overline{CAS}$\ to $\overline{CAS}$/ | Note 2 | (CWL + 1)•T)-2 | ns |
| Tcwl | $\overline{CAS}$/ to $\overline{CAS}$\ | Notes 2, 5 | (CWL + 1)•T)-2 | ns |

Note: Loading capacitance = 30 pF

Note 1: The measured delay for any of the signal indicated by this note will not vary from the measured delay of any other signal indicated by this note by more than ±1 ns.

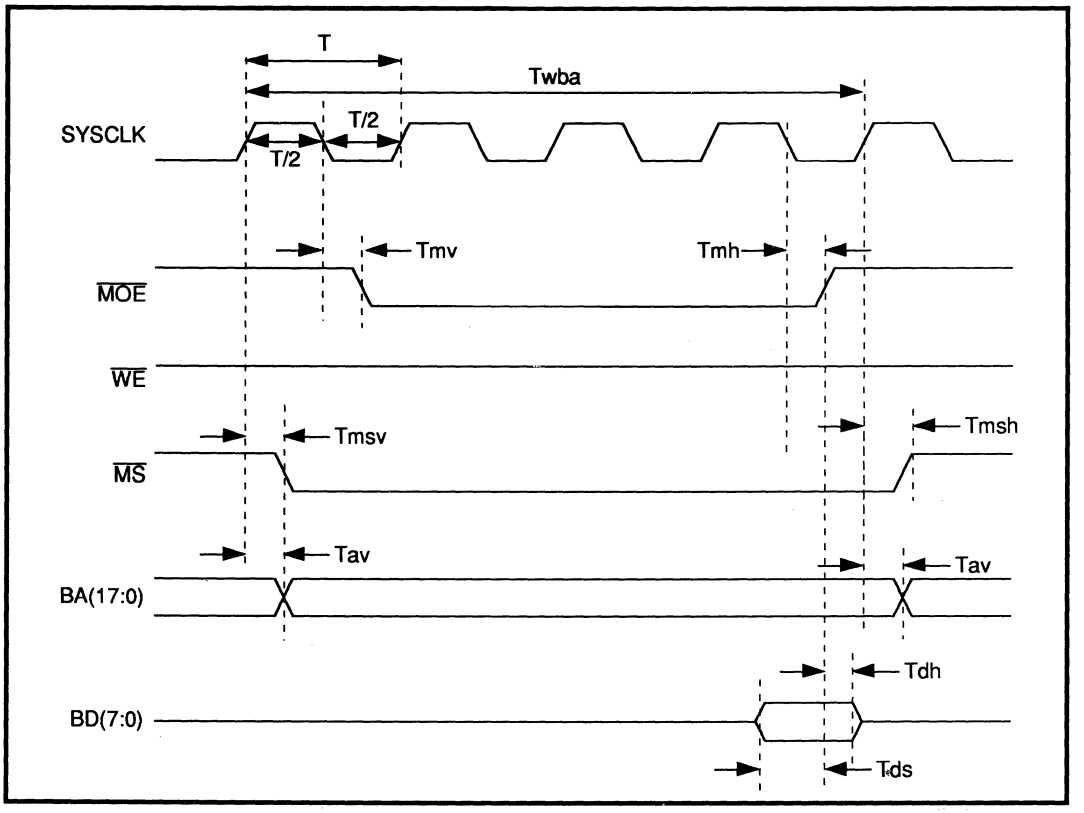
Note 2: RWL, RWH, CWL and CWH are fields in the Buffer Manager Timing Control Register (54H). Each is a two bit field which can contain a value of 0, 1, 2, or 3. These values determine the minimum number of SYSCLK periods (T) for the associated signal width.

Note 3: The minimum width value of Trwl will be generated for refresh cycles and for any buffer memory access cycle except when multiple page mode accesses are performed. When multiple page mode accesses are performed, the width of the $\overline{RAS}$ low pulse is extended until the end of the last $\overline{CAS}$ low cycle.

Note 4: The minumum value of Trwh will be generated whenever the Buffer Manager determines that a buffer request is pending at the completion of the current memory cycle and a page mode access can not be used either because page mode operation is not enabled or the needed location is not within the current page.

Note 5: The minumum value of Tcwh will be generated only between consecutive page mode accesses.

Note 6: $\overline{MS}$ will rise only if the Buffer Manager determines that no additional requests for buffer access are pending. If the Buffer Manager determines that another access is to be Made, $\overline{MS}$ is kept low between the accesses for improved speed.




Note: Twba is a functional parameter that gives the duration of one RAM data buffer access cycle in SYSCLK periods. The value is programmed in bits 1-0 of register 54H. These examples show Twba = 4T.

**FIGURE 8: SRAM Read Timing**

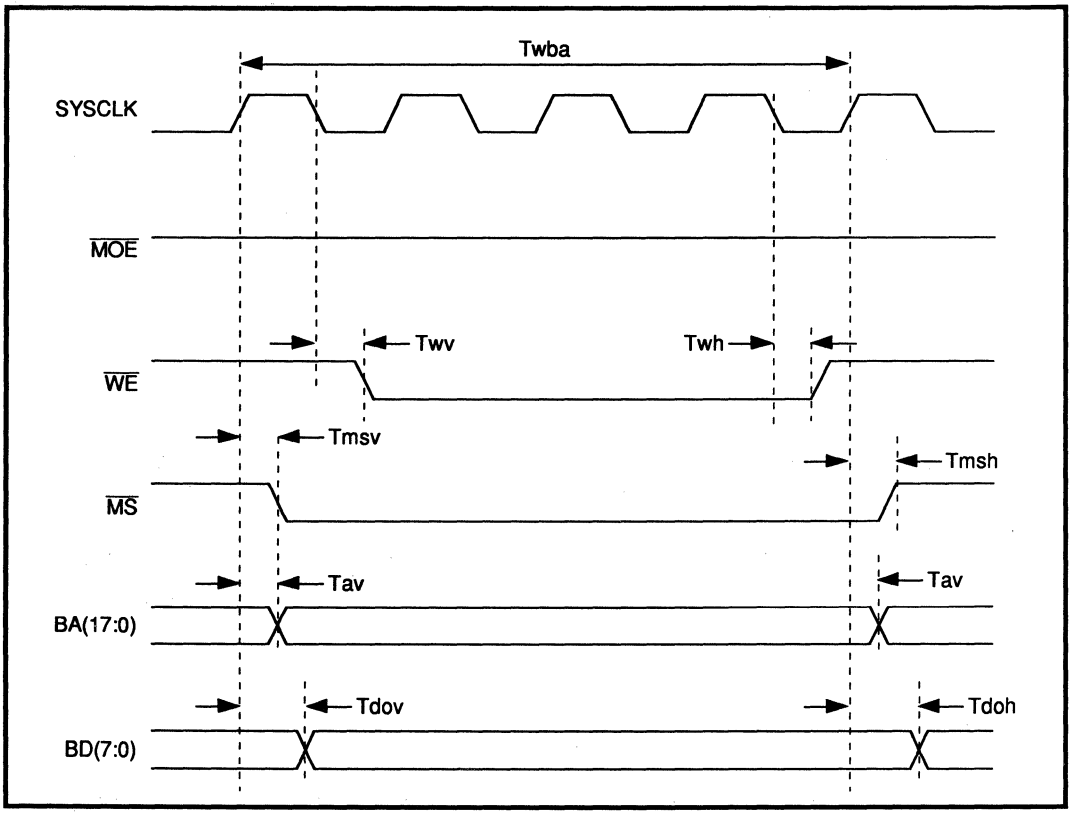



**FIGURE 9: SRAM Write Timing**

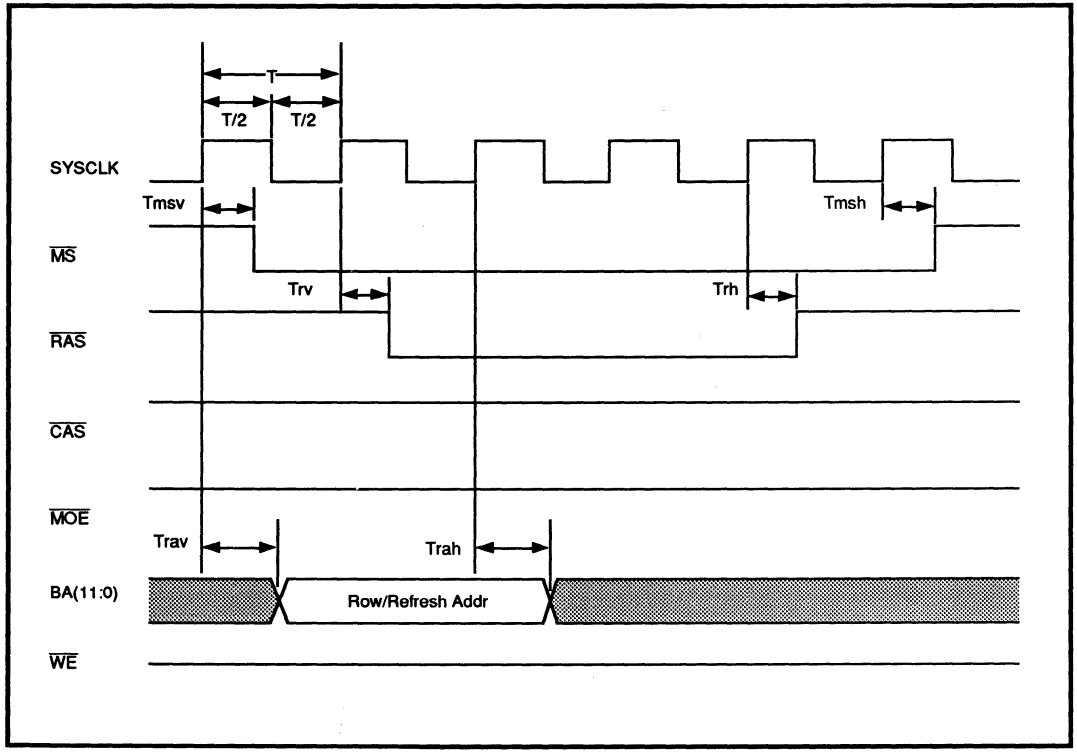



FIGURE 10: DRAM Timing, Refresh Cycle (Shown with WRL = 0)

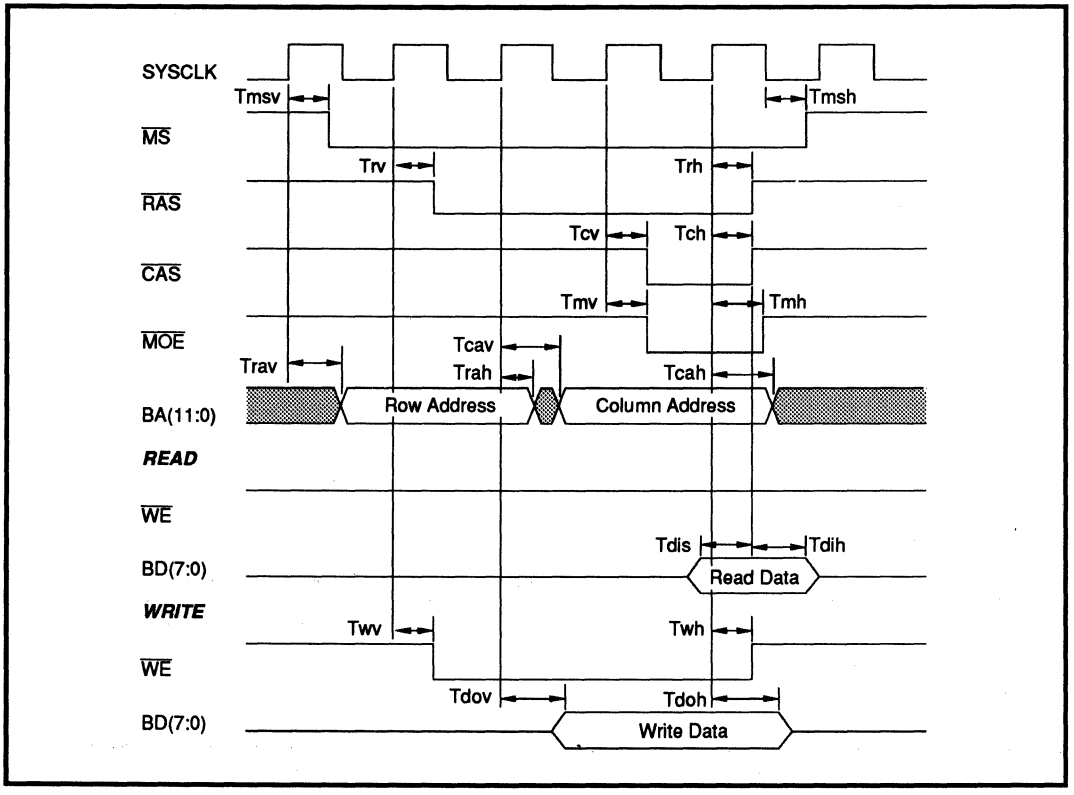



**FIGURE 11: DRAM Timing, Standard Cycle (Shown with RWL = 0 and CWL = 0)**

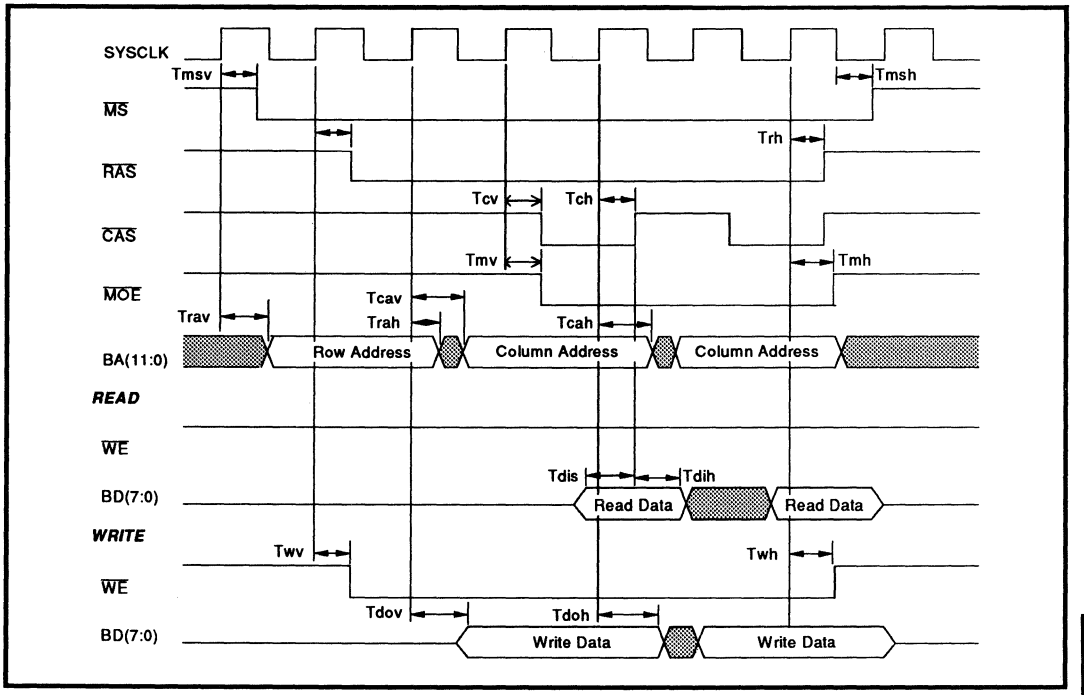



**FIGURE 12: DRAM Timing, Fast Page Cycles (Shown with RWL = 0, RWH = 0, CWL = 0 and CWH = 0)**

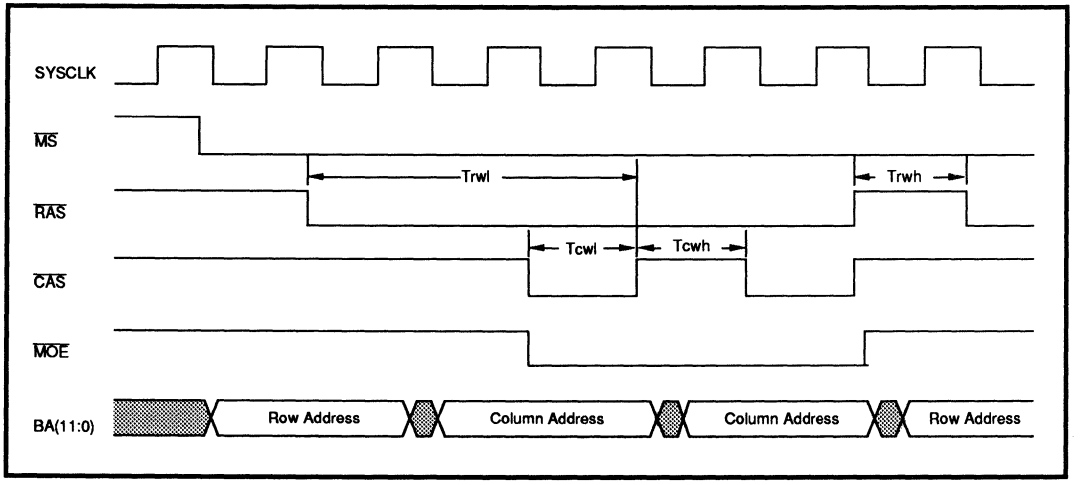



**FIGURE 13: DRAM Timing (Showing the Relationship of RWL, RWH, CWL and CWH to overall timing)**

**SCSI Asynchronous Timing Paraemeters**

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|---|
| Tods | Data Setup to $\overline{ACK}$\ | SCSI Output Phase | 5 | | | ns |
| Todh | Data Hold from $\overline{ACK}$\ | SCSI Output Phase | 12 | | | ns |
| Talrh | $\overline{ACK}$\ to $\overline{REQ}$/ | | | | 49 | ns |
| Tids | Data Setup to $\overline{REQ}$ \ | SCSI Input Phase | 80 | | | ns |
| Tidh | Data Hold from $\overline{ACK}$\ | SCSI Input Phase | 29 | | | ns |

Note: All timing parameters are measured with 200 pf load, two SCSI terminator loads with $\overline{ACK}$ Filter turned off.

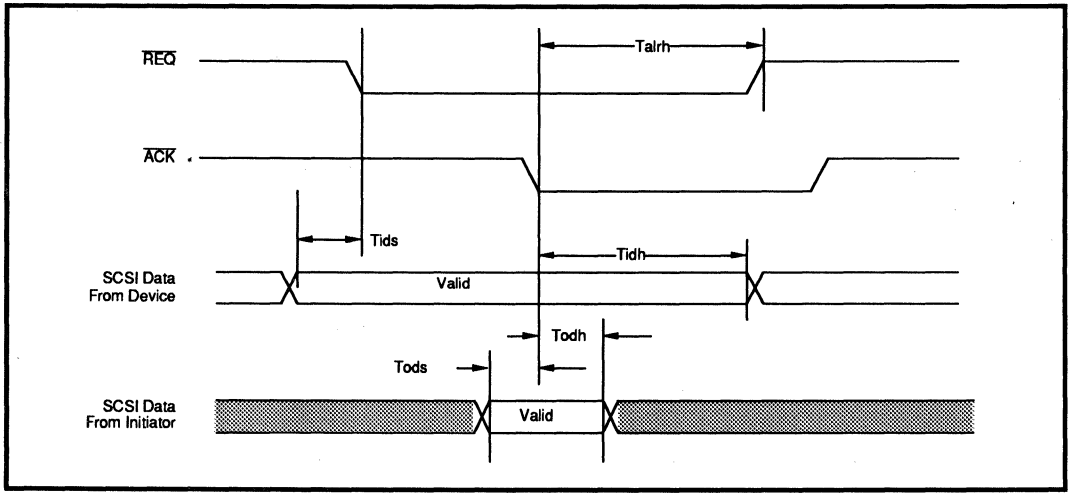



**FIGURE 14: SCSI Asynchronous Timing**

**SCSI Synchronous Timing Paramenters**

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|---|
| Trh | $\overline{REQ}$ Assertion Time | | 37 | | 48 | ns |
| Trl | $\overline{REQ}$ Deassertion Time | | 63 | | 52 | ns |
| Tids | Setup time SCSI Data to $\overline{REQ}$\ | Write to SCSI bus | 43 | | | ns |
| Tidh | Hold time $\overline{REQ}$\ to SCSI Data invalid | Write to bus | 43 | | | ns |
| Tal | Minimum $\overline{ACK}$ Assertion Width Required | | 10 | | | ns |
| Tods | Data Setup to $\overline{ACK}$\ | Read from the SCSI bus | 5 | | | ns |
| Todh | Data Hold from $\overline{ACK}$\ | Read from the SCSI bus | 12 | | | ns |

Note: All timing parameters are measured with 200 pf load, two SCSI terminator loads, $\overline{ACK}$ filter turned off.

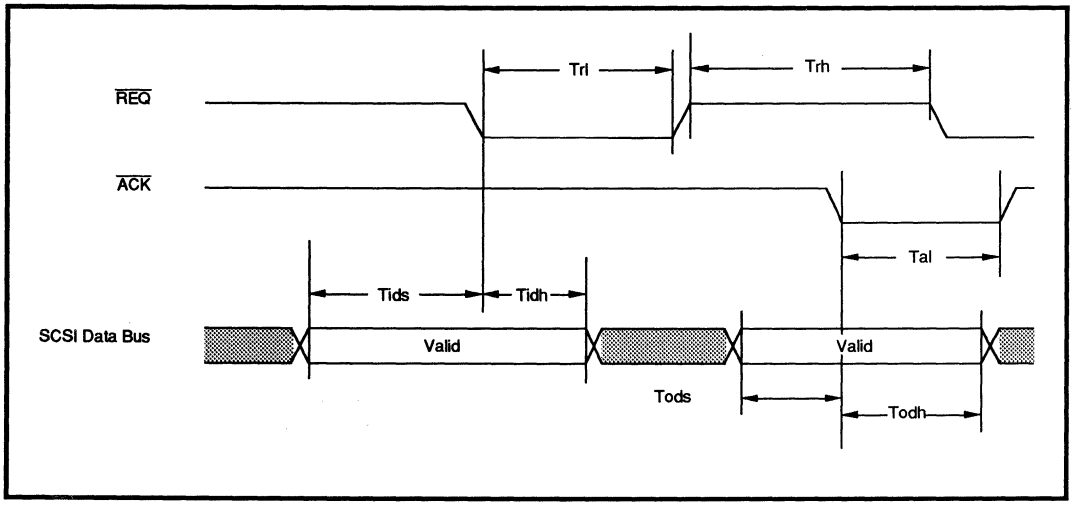



**FIGURE 15: SCSI Synchronous Timing**

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**Synchronous Data In/Out Phase**

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|---|
| Txtrp* | Synchronous Transfer Period | (see note) | | | | ns |
| Tsrl | SYSFREQ high to $\overline{REQ}$ low | | | | 50 | ns |
| Tsrh | SYSFREQ high to $\overline{REQ}$ high | | | | 60 | ns |
| Tdov | SYSFREQ high to data out valid | | | | 40 | ns |
| Tdsu | Data setup to $\overline{ACK}$ low | | 55 | | | ns |
| Tdh | Data hold from $\overline{ACK}$ low | | 40 | | | ns |

Note: Txtrp is the Synchronous Transfer Period as defined by the Synchronous Control Register (Reg: 43H). SYSFREQ is a function of the BUFCLK and is determined by the prescale value as defined by the Clock Control Register (Reg: 49H).

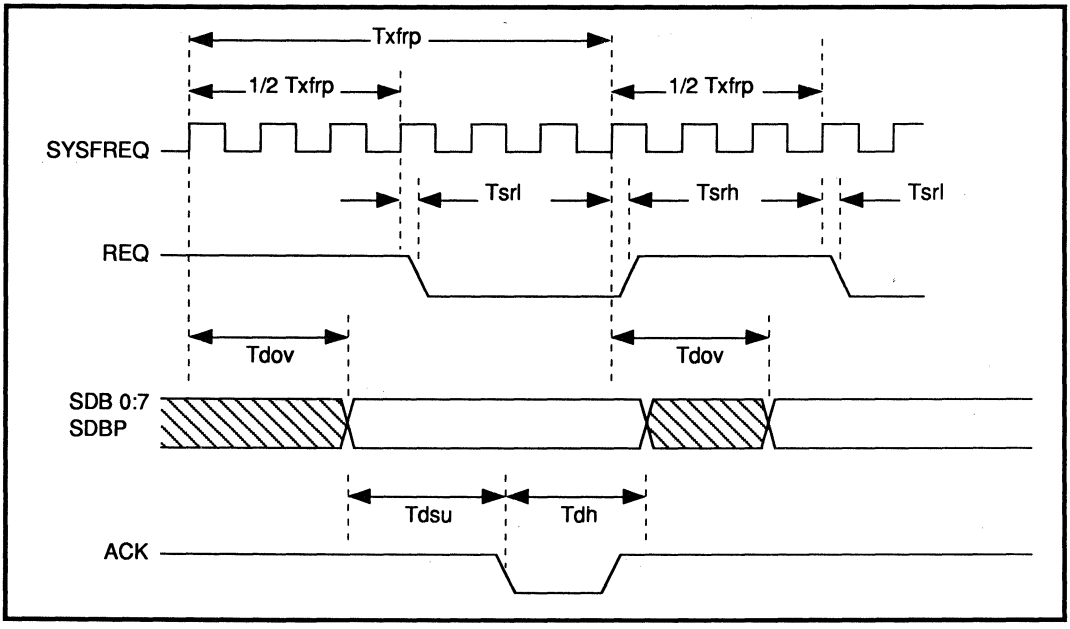


**FIGURE 16: Even Number of SYSFREQ Cycles/SCSI Transfer Period**

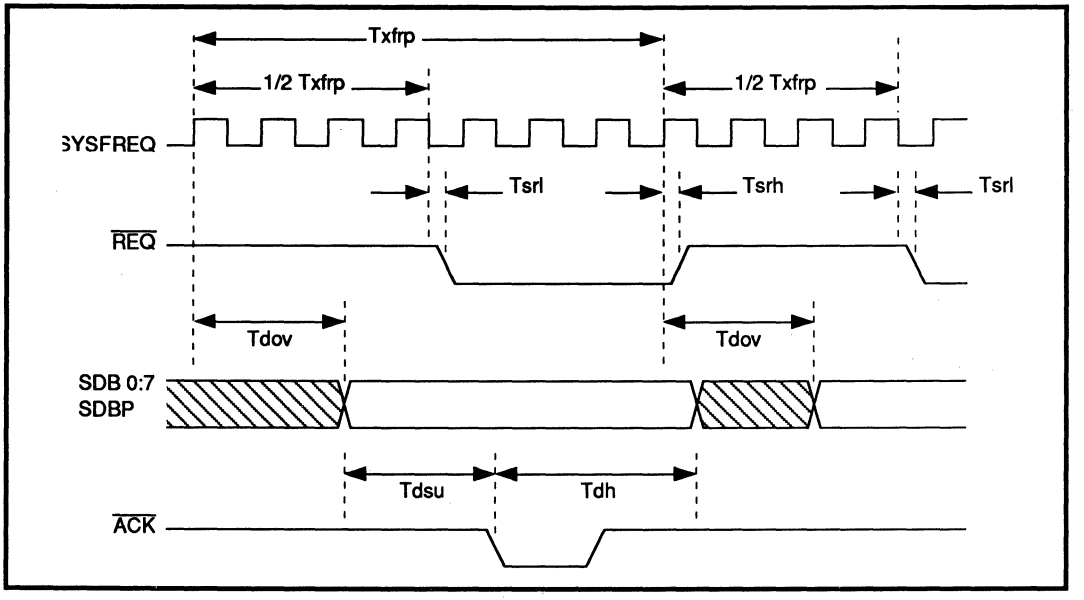


**FIGURE 17: Odd Number of SYSFREQ Cycles/SCSI Transfer Period**

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**Wait for Selection**

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|---|
| Tbsd | Bus Settle Delay (400 ns) to the assertion of $\overline{BSY}$ | | 3T + 90 | | 4T + 90 | ns |

Note: T is the SCSI Clock Period (SCP) as defined in Register 49H (CLKCTL).

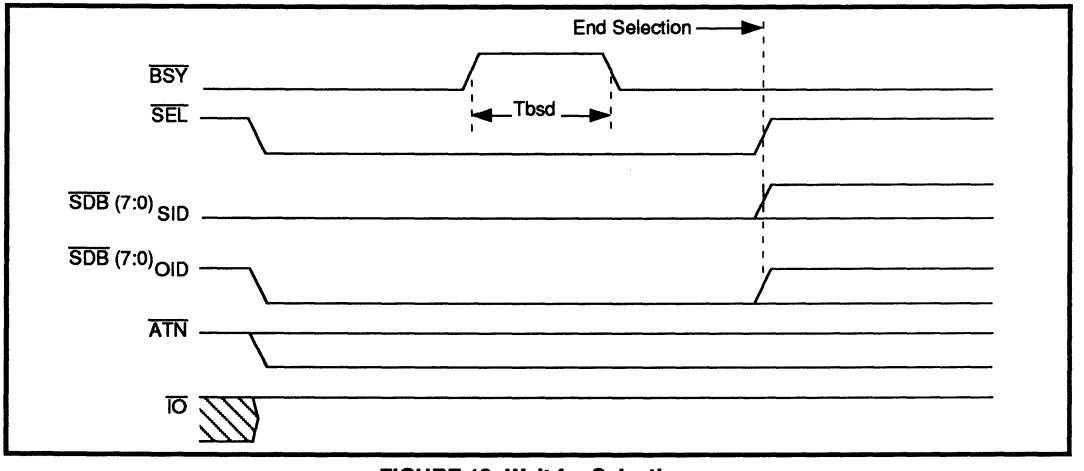



**FIGURE 18: Wait for Selection**

**Arbitration**

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|---|
| Tbfsd | Bus Settle Delay (400 ns) + Bus Free Delay (800 ns) to the assertion of BSY and $\overline{SDB}_{OID}$ | | 6T + 110 | | 7T + 110 | ns |
| Tad | Arbitration Delay (2.4 µsec) to the assertion of $\overline{SEL}$ (win) or deassertion of $\overline{BSY}$ and $\overline{SDB}_{OID}$ (lost) | | - | | 13T + 100 | ns |
| Tbcsd | Bus Clear Delay (800 ns)+ Bus Settle Delay (400 ns) to end of Arbitration Phase | | - | | 6T + 100 | ns |

Note: T is the SCSI Clock Period (SCP) as defined in Register 61H (CLKCTL).

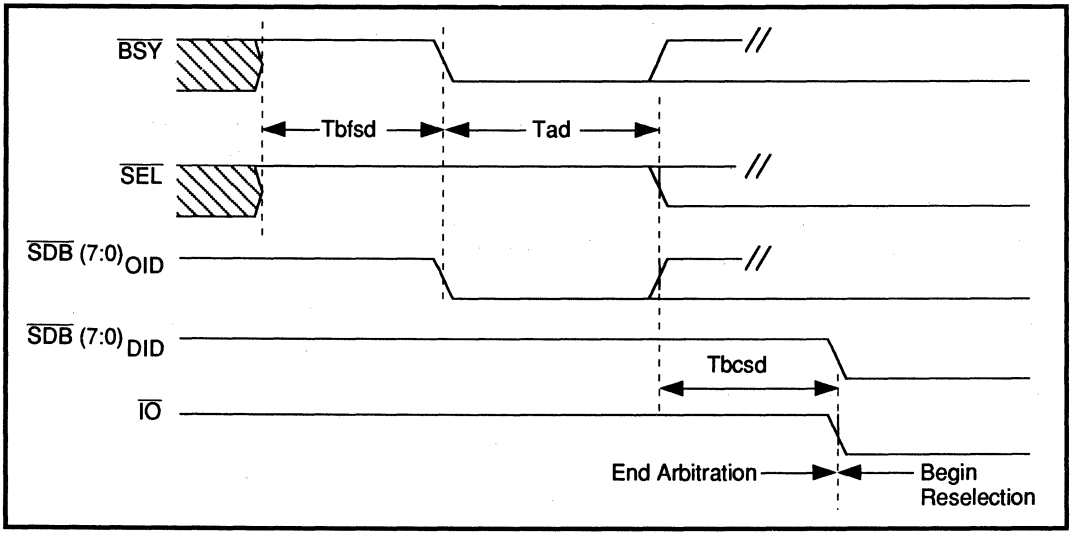



**FIGURE 19: Arbitration**

**Reselection**

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|---|
| Tbcsd | Bus Clear Delay (800 ns) + Bus Settle Delay (400 ns) to end of Arbitration Phase | | - | | 6T + 100 | ns |
| Tdskd1 | Two Deskew Delays (90 ns) to the deassertion of $\overline{BSY}$ | | - | | 160 | ns |
| Tbsd | Bus Settle Delay (400 ns) to the assertion of $\overline{BSY}$ | | - | | 2T + 40 | ns |
| Tdskd2 | Two Deskew Delays (90 ns) to the deassertion of SEL, $\overline{SDB}_{OID}$, and $\overline{SDB}_{DID}$ | | 1T +70 | | 2T + 70 | ns |

Note: T is the SCSI Clock Period (SCP) as defined in Register 61H (CLKCTL).

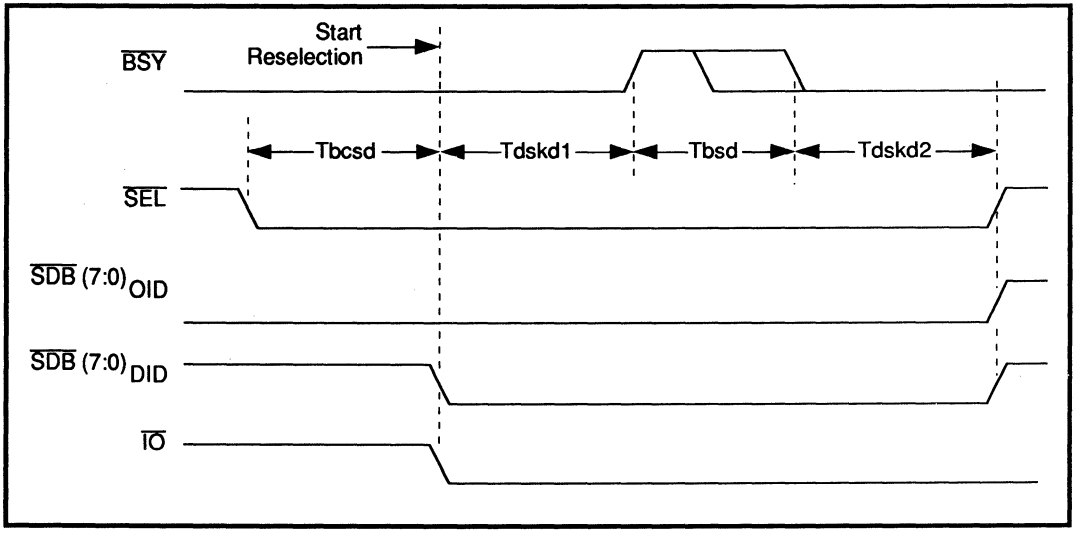
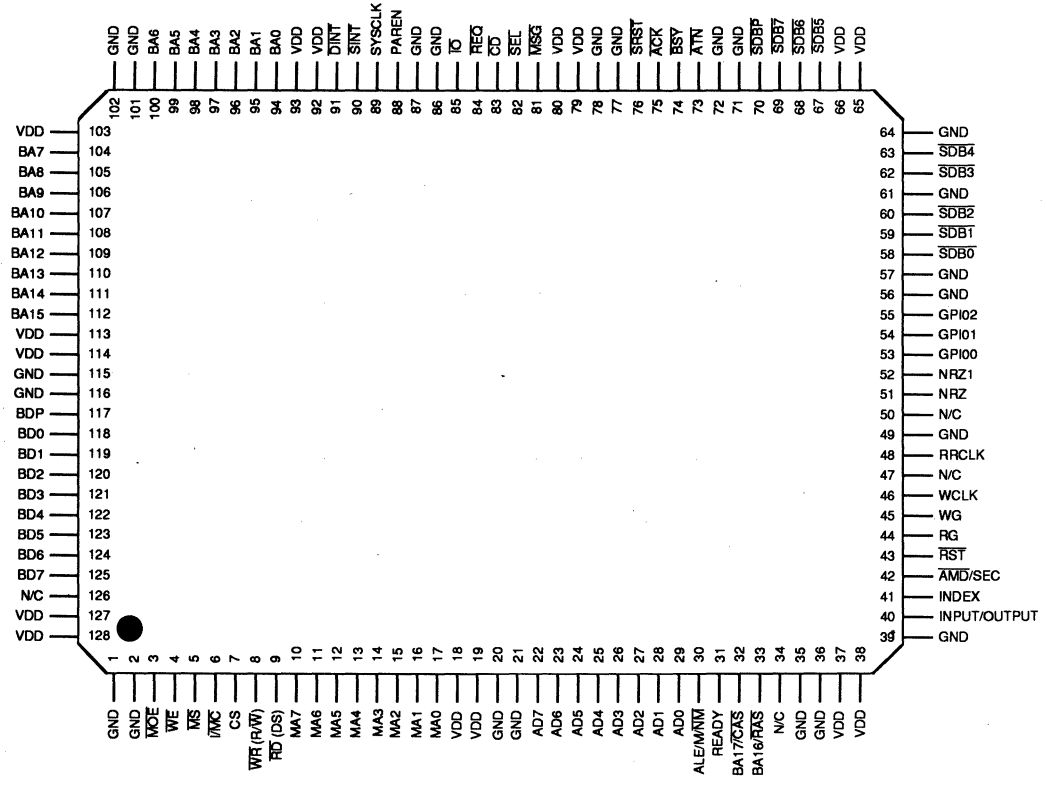



**FIGURE 20: Reselection**

# SSI 32C9022
# SCSI Combo Controller
# 48 Mbit/s; dual bit NRZ interface

## PACKAGE PIN DESIGNATIONS

(Top View)




**128-Lead QFP**

**Advance Information:** Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.



Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680, (714) 573-6000, FAX: (714) 669-8814

silicon systems®
A TDK Group Company

# SSI 32C9023
## SCSI Combo Controller
## 72 Mbit/s; dual bit NRZ interface
## Advance Information

January 1993

## DESCRIPTION

The SSI 32C9023 is an advanced CMOS VLSI device which integrates major portions of the hardware needed to build an SCSI disk drive. The circuitry of the SSI 32C9023 includes a complete SCSI target interface, an advanced buffer manager, a high performance disk formatter and an 88 bit Reed-Solomon ECC with fast "on-the-fly" hardware correction. The SSI 32C9023 provides maximum performance while minimizing micro controller intervention.

The SSI 32C9023 provides a Dual Bit Interface to the ENDEC. The Dual Bit Interface allows an effective transfer rate of up to 72 megabits per second on the disk interface by utilizing two parallel NRZ data signals and a clock rate of 36 MHz. The reduction of overall clock rates between the SSI 32C9023 and the ENDEC can be of great benefit to the designer.

The SSI 32C9023 can sustain concurrent transfers of up to 72 megabits per second transfer rate to the disk and 10 megabytes per second across the SCSI bus. In addition, on-the-fly error corrections and micro controller accesses to the buffer memory will not degrade the throughput during transfers.

(continued)

## FEATURES

- **SCSI Bus Interface**
  - **Full SCSI-2 Compatibility**
  - **Direct bus interface logic with on-chip 48 mA drivers**
  - **Synchronous transfer rates up to 10 megabytes per second**
  - **Asynchronous transfer rates up to 5 megabytes per second**
  - **Parity generation and checking**
  - **Auto Command Mode (ACM) SCSI state machine performs high level SCSI sequences without microprocessor intervention**
  - **Four level ACM command FIFO supports automatic execution of multiple ACM commands**
  - **Hardware support for automatic handling of SCSI-2 command queuing**
  - **Automatic SCSI CDB size determination**
  - **Automatic SCSI Disconnect and Reconnect**
  - **Sixteen byte data FIFO between SCSI channel and Buffer Manager**

(continued)

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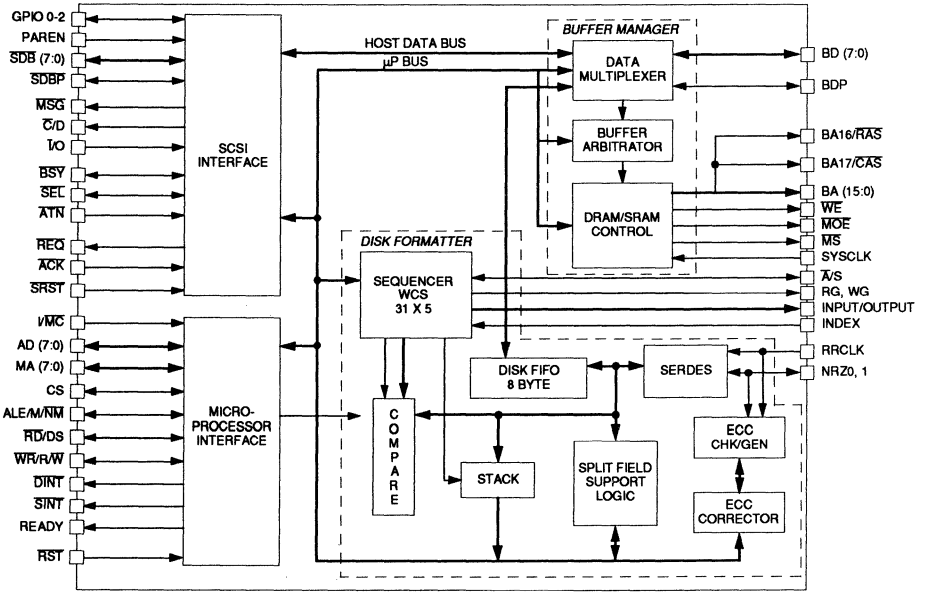
## BLOCK DIAGRAM



# SSI 32C9023
# SCSI Combo Controller
# 72 Mbit/s; dual bit NRZ interface

## DESCRIPTION (continued)

The SSI 32C9023 is one of a family of Silicon Systems' single chip disk controllers which support a wide range of device interfaces. The SSI 32C9020 is similar to the SSI 32C9023, but supports a Single Bit or Serial NRZ interface for applications which require this feature. The SSI 32C9022 is pin compatible with the SSI 32C9023 but supports disk data transfers rate up to only 48 megabits per second. Other family members support AT and PCMCIA interfaces. The Silicon Systems' chip family is illustrated in the hierarchy chart shown in Figure 1. All members are based on a common architecture allowing major portions of firmware to be reused.

The high level of integration within the SSI 32C9023 represents a major reduction in parts count. When the SSI 32C9023 SCSI Controller is combined with the SSI 32R2010Read/Write device, the SSI 32P3000 Pulse Detector, the SSI 32D4040 Dual Bit Data Synchronizer with 1,7 ENDEC, the 32H4631 Servo and Motor Speed Controller, an appropriate micro controller and memory, a complete, cost efficient, high performance intelligent drive solution is created.

## FEATURES (continued)

- **Buffer Manager**
  - **Direct support of DRAM or SRAM**
    - **SRAM throughput to 20 megabytes per second**
    - **SRAM size up to 256k bytes**
    - **DRAM throughput to 17.78 megabytes per second**
    - **DRAM size up to 1 megabyte**
  - **Programmable memory timing**
  - **Buffer RAM segmentation with flexible segment sizes from 256 bytes to 1 megabyte**
  - **Dedicated host, disk and microprocessor address pointers**
  - **Internal buffer protection circuit provides buffer integrity**
- **Disk Formatter**
  - **Dual Bit NRZ Interface**
  - **Effective Data Rates to 72 megabits/s (36 MHz Dual Bit Transfers)**
  - **Automatic multi-sector transfer**
  - **Header or microprocessor based split data field support**
  - **Advanced sequencer organized in 31 x 5 bytes**
  - **88-bit Reed Solomon ECC with "on-the-fly" fast hardware correction circuitry**
  - **Capable of correcting up to four 10-bit symbols in error**
  - **Guaranteed to correct one 31-bit burst or two 11-bit bursts**
  - **Hardware on-the-fly correction of either an 11- or 31-bit single burst error within a half sector time**
  - **Detects up to one 51-bit burst or three 11-bit bursts**
- **Microprocessor Interface**
  - **Supports both multiplexed or non-multiplexed microprocessors**
  - **Separate or combined host and disk interrupts**
  - **Programmable wait state insertion**
- **Other Features**
  - **Internal power down mode**
  - **Available in 128-pin QFP**

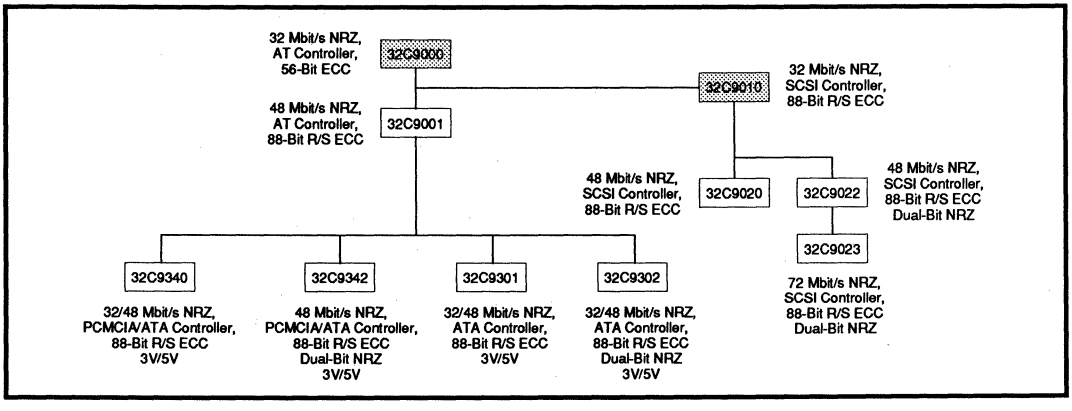



**FIGURE 1: Silicon Systems' Single Chip Controller Hierarchy**

## FUNCTIONAL DESCRIPTION

The SSI 32C9023 contains the following four major functional blocks:

Microcontroller Interface
SCSI Interface
Disk Formatter
Buffer Manager

The Microprocessor Interface allows the local microprocessor access to all of the SSI 32C9023 internal control registers and any location within the buffer memory. The microprocessor, by writing and reading the internal registers can control all activities of the SSI 32C9023. The microprocessor can elect to perform SCSI and/or disk operations directly, or it can enable the advanced features of the SSI 32C9023 which can perform all typical operations automatically.

The SCSI Interface block handles all SCSI activities. The SCSI interface includes 48 mA drivers allowing for direct connection of the SSI 32C9023 to the SCSI bus. The SCSI interface logic includes Auto Command Mode (ACM) logic, an advanced state machine capable of handling a variety of complex SCSI sequences without microprocessor intervention. The microprocessor can queue up to four ACM commands into the ACM Command FIFO to create even more sophisticated command sequences. The SCSI block interfaces directly with the Buffer Manager via an internal speed matching FIFO. This FIFO, plus the bandwidth capabilities of the Buffer Manager guarantee sustained full speed transfers across the SCSI bus. The high level of automation of the ACM minimizes SCSI bus overhead. The net result is maximized performance with minimum SCSI bus band width utilization.

The Disk Formatter performs the serialization and deserialization of data. If provides all of the necessary functions to control track formatting, header search, and the reading and writing of data. The heart of the Disk Formatter is an advanced programmable sequencer which is flexible enough to interface to a wide variety of read/write channels. The sequencer can contain 31 instructions, each of which is 5 bytes (40 bits) in width. The width of the instructions allows for sophisticated branching techniques which increase the flexibility and power of the sequencer. The flexible disk interface can be configured through a wide range of capabilities. This allows the SSI 32C9023 to interface with nearly any read/write channel and allows the user of the SSI 32C9023 to select the read/write channel best suited to the device. Of course, by selecting the SSI 32C9023 controller and the SSI 32D4040 Data Synchronizer with 1,7 ENDEC, you are guaranteed a problem free interface.

Within the Disk Formatter are the ECC generator/checker and ECC corrector. The generator/checker provides the ability to generate or check a 32 bit ECC for headers and an 88 bit Reed Solomon code for data. If the checker detects an error in an 88 bit Reed Solomon data field, the syndrome information is transferred into the corrector. The corrector performs the necessary operations to determine if the error was correctable and interfaces directly with the buffer controller to perform the correction automatically. The corrector performs its correction within one half of a sector time. This gaurantees that the corrector will always be available to correct the next sector if necessary.

As its name implies, the Buffer Manager manages the data buffer of the controller. The Buffer Manager can support either SRAM or DRAM. When configured to operate with DRAM, the Buffer Manager automatically performs necessary refresh cycles. The Buffer Manager creates all of the necessary timing and control signals for a wide range of memory types and speeds. The Buffer Manager interfaces with the buffer memory, the SCSI Interface block, the data path of the Disk Formatter block, the ECC corrector and the microprocessor. If more than one of these devices requires access to the buffer memory, the Buffer Manager arbitrates the requests automatically. The Buffer Manager of the SSI 32C9023 can sustain SCSI operations at the rate of 10 megabytes per second, Disk Formatter operations at 72 megabits per second (9 megabytes per second) and still have sufficient band width left to handle on-the-fly ECC corrections and microprocessor accesses without degrading performance on any of the interfaces.

## PIN DESCRIPTION

The following convention is used in the pin description:

(I) denotes an input
(O) denotes an output
(Z) denotes a tri-state output
(OD) denotes an open drain output

### GENERAL

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| VDD | | POWER SUPPLY PIN, VCC |
| GND | | GROUND |

### HOST INTERFACE

| | | |
|---|---|---|
| $\overline{SDBP}$ | I/O | SCSI DATA BUS PARITY. Odd parity bit for the SCSI data bus. |
| $\overline{SDB(7:0)}$ | I/O | SCSI DATA BUS BITS 7-0. |
| $\overline{ATN}$ | I | ATTENTION. This active low signal is used by the initiator to request a message out phase. |
| $\overline{BSY}$ | I/O | BUSY. This active low signal is used to indicate when the bus is active. |
| $\overline{ACK}$ | I | ACKNOWLEDGE. This active low signal is used in the handshake protocol to indicate the completion of a data byte transfer. |
| $\overline{SRST}$ | I | SCSI RESET. This active low signal is used to reset the SCSI controller. |
| $\overline{MSG}$ | O | MESSAGE. This active low signal is used to indicate a message phase. |
| $\overline{SEL}$ | I/O | SELECT. This active low signal is used to indicate either a selection or reselection phase. |
| $\overline{C}$/D | O | COMMAND/DATA. This signal is used to indicate either a command or data phase. |
| $\overline{REQ}$ | I | REQUEST. This active low signal is used in the handshake protocol to initiate a data byte transfer. |
| $\overline{I}$/O | I | INPUT/OUTPUT. This signal is used to indicate the direction of data transfer. |
| PAREN | I | SCSI PARITY ENABLE. This active high signal is used to enable parity checking of the SCSI data bus. Parity checking is disabled when this pin is held low. |
| GPIO(2:0) | I/O | INPUT/OUTPUT. These pins are used to indicate the SCSI ID of the target device. The pins can be programmed as outputs for test purposes only. |

### DISK INTERFACE

| | | |
|---|---|---|
| INDEX | I | INDEX. Input for index pulse received from the drive. |
| INPUT/ OUTPUT | I/O | DISK SEQUENCER INPUT/OUTPUT. A general purpose control (output) and status (input) pin configured by the Output Enable Bit of Register 71H, bit 7.<br>At power-on, this pin is an input. As an input, it can be used to synchronize the disk sequencer to an external event. As an output, it is controlled by bit 2 of the Control Field of the disk sequencer. |
| $\overline{AMD}$/ SECTOR | I/O | ADDRESS MARK DETECT/SECTOR. This pin is used in the hard sector mode as the sector input. A pulse on this pin indicates a sector mark is found.<br>In the soft sector mode, a low-level input indicates an address mark was detected. The device powers up in soft sector default mode. |

**DISK INTERFACE** (continued)

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| RG | O | READ GATE. During disk data read, this pin is asserted. Active high. |
| WG | O | WRITE GATE. During disk data write, this pin is asserted. Active high. |
| RRCLK | I | READ/REFERENCE CLOCK. This is a clock signal generated from an external data synchronizer. This clock is used to synchronize the input NRZ data and clock the disk formatter of the chip. |
| WCLK | O | WRITE CLOCK. This signal clocks the NRZ data out in the dual NRZ interface mode. |
| NRZ1 | I/O | NON RETURN TO ZERO 1. In dual NRZ mode, this signal is the most significant bit read data input from the disk drive when the read gate signal is asserted; it is the most significant bit write data output to the disk drive when the write gate signal is asserted. In single NRZ mode, this signal is not used and should be grounded. NRZ1 is the leading bit of the bit pair. In Write mode, the MSB of the data bytes always appears on NRZ1. |
| NRZ | I/O | NON RETURN TO ZERO. In dual NRZ mode, this signal is the least significant bit read data input from the disk drive when the read gate signal is asserted; it is the least significant bit write data output to the disk drive when the write gate signal is asserted. In single NRZ mode, this signal is used to transfer NRZ data to/from the read channel chip. |

**MICROPROCESSOR INTERFACE**

| | | |
|---|---|---|
| $\overline{RST}$ | I | RESET. An asserted low input generates a component reset that holds the internal registers at reset, stops all operations within the chip, and deasserts all output signals. All input/output signals are set to the high-Z state during the assertion of this signal. |
| ALE/M/$\overline{NM}$ | I | ADDRESS LATCH ENABLE/MULTIPLEXED/NON-MULTIPLEXED ADDRESS SELECT. When tied high or left floating after reset, the microprocessor interface is configured as non-multiplexed. When driven low, then the microprocessor interface is configured as multiplexed. In this case this pin functions as the address latch enable, and the MA(7:0) pins are the demultiplexed address outputs. |
| CS | I | CHIP SELECT. Active high signal, when asserted, the internal registers of the SSI 32C9022 can be accessed. |
| $\overline{WR}$/R/$\overline{W}$ | I | WRITE STROBE/READ/WRITE. In the Intel bus mode, when an active low signal is present with CS signal high, the data is written to the internal registers.<br>In the Motorola bus mode, this signal acts as the R/$\overline{W}$ signal. |
| $\overline{RD}$/DS | I | READ STROBE/DATA STROBE. In the Intel bus mode, when an active low signal is present with CS signal high, internal register data is read.<br>In the Motorola mode, this signal acts as the DS signal. DS when active high is data strobe. |
| $\overline{DINT}$ | O, OD,Z | DISK INTERRUPT. An active low signal indicates the controller is requesting microprocessor service from the disk side. This signal is programmable for either a push-pull or open-drain output circuit. This signal powers up in the high-Z state. Register 4F bit 3 enables the pull-up. |

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**MICROPROCESSOR INTERFACE** (continued)

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| $\overline{SINT}$ | O, OD,Z | SCSI INTERRUPT. This signal is generated by the SCSI controller and is an interrupt line to the microprocessor. It is programmable for either a push-pull or open drain output circuit. This signal powers up in the high-Z state. The interrupt is sourced from the SCSI Interrupt Register. Register 4F bit 3 enables the pull-up. This signal is also programmable to be either an active high or low interrupt. |
| AD(7:0) | I/O | ADDRESS/DATA BUS. When configured in the Intel mode, these lines are multiplexed, bidirectional microprocessor register address and data lines.<br>When configured in the Motorola mode, these lines are bidirectional data lines. |
| MA(7:0) | I/O | MICROPROCESSOR ADDRESS BUS: These signals are nonmultiplexed address input or latched address output lines. |
| READY | O | READY: When this signal is deasserted low, the microprocessor shall insert wait states to allow time for the chip to respond. |
| I/$\overline{MC}$ | I | INTEL/MOTOROLA: This signal selects the microprocessor interface to be used. When this signal is asserted high, it selects the Intel bus control interface. When this signal is deasserted low, it selects the Motorola bus control interface. This signal has an internal pull-up to allow the default selection of the Intel bus control interface. |

**BUFFER MANAGER INTERFACE**

| | | |
|---|---|---|
| BA(15:0) | O | BUFFER MEMORY ADDRESS LINES 15 through 0. Active high, for direct connection to a Static or Dynamic RAM address lines. |
| BA16/$\overline{RAS}$ | O | BUFFER MEMORY ADDRESS 16: In SRAM mode, for direct connection to a Static RAM address line 16.<br>ROW ADDRESS STROBE: In DRAM mode, for direct connection to a Dynamic RAM Row Address Strobe signal. |
| BA17/$\overline{CAS}$ | O | BUFFER MEMORY ADDRESS 17: In SRAM mode, for direct connection to a Static RAM address line 17.<br>ROW ADDRESS STROBE: In DRAM mode, active low, for direct connection to a Dynamic RAM Column Address Strobe signal. |
| BD(7:0) | I/O | BUFFER MEMORY DATA BUS. 7 through 0. Active high, buffer data bus that connects directly to the buffer RAM data lines. |
| BDP | I/O | BUFFER MEMORY DATA PARITY. This signal provides odd parity for the buffer memory data bus during transfers to/from the buffer memory to the buffer RAM. |
| $\overline{MOE}$ | O | MEMORY OUTPUT ENABLE. In SRAM mode this signal is asserted low when every buffer memory access is active. In DRAM mode this signal is asserted low only for buffer memory read operation. |
| $\overline{MS}$ | O | MEMORY SELECT. An active low signal indicates external memory is selected. |
| $\overline{WE}$ | O | WRITE ENABLE. Active low, write enable for the buffer RAM. |
| SYSCLK | I | SYSTEM CLOCK. This signal is used to synchronize the buffer RAM access, including the generation of memory address bits, write enable $\overline{WE}$, and memory output enable $\overline{MOE}$. |

## ELECTRICAL SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS

Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC operating characteristics.

| PARAMETER | RATING |
|---|---|
| Power Supply Voltage, VCC | 7V |
| Ambient Temperature | 0 to 70°C |
| Storage Temperature | -65 to 150°C |
| Power Dissipation | 750 mW |
| Input, Output pins | -0.5 to VCC+0.5V |

### ELECTRICAL CHARACTERISTICS

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|
| VCC Power Supply Voltage | | 4.50 | | 5.50 | V |
| ICC Supply Current | Ta = 25°C Outputs Unloaded | | | 50 | mA |
| ICCS Supply Current | | | | 500 | µA |
| VIL Input Low Voltage | | -0.5 | | 0.8 | V |
| V0IH Input High Voltage | | 2.0 | | VCC+0.5 | V |
| VOL Output Low Voltage | All pins except SCSI interface, IOL = 2 mA | | | 0.4 | V |
| VOL Output Low Voltage | SCSI interface pins, IOL = 48 mA | | | 0.5 | V |
| VOH Output High Voltage | IOH = -400 µA | | | 2.4 | V |
| IL Input Leakage Current | 0 < VIN < VCC | -10 | | 10 | µA |
| CIN Input Capacitance | | | | 10 | pF |
| COUT Output Capacitance | | | | 10 | pF |

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## MICROPROCESSOR INTERFACE TIMING

### Multiplexed Interface Timing Parameters (Figures 2-5)

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|---|
| Ta | ALE width | | 20 | | | ns |
| Tma | Address valid to MA(7:0) valid | | | | 30 | ns |
| Tr | $\overline{RD}$ width | | 80 | | | ns |
| As | Address valid to ALE ↓ | | 5 | | | ns |
| Ah | ALE ↓ to address invalid | | 10 | | | ns |
| Cs | CS valid to $\overline{RD}$ ↓ or DS ↑ | | 20 | | | ns |
| Ch | $\overline{RD}$ ↑ or DS ↓ to CS ↓ | | 0 | | | ns |
| Tda | $\overline{RD}$ ↓ or DS ↑ to read data valid | | | | 60 | ns |
| Tds | DS width | | 80 | | | ns |
| Tdh | $\overline{RD}$ ↑ or DS ↓ to read data invalid | | 0 | | 25 | ns |
| Tsrw | R/$\overline{W}$ valid to DS ↑ | | 20 | | | ns |
| Thrw | DS ↓ to R/$\overline{W}$ invalid | | 20 | | | ns |
| Tdrdy | $\overline{RD}$ ↓ to READY ↓ (Intel) or DS ↑ to READY ↓ (Motorola) | | | | 30 | ns |
| Wds | Write data valid to $\overline{WR}$ ↑ or DS ↓ | | 40 | | | ns |
| Wdh | $\overline{WR}$ ↑ or DS ↓ to write data invalid | | 10 | | | ns |

Note: ↑ indicates rising edge ↓ indicates falling edge

### Non-Multiplexed Bus Interface Timings (Figure 6)

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|---|
| Tmas | MA(7:0) valid to DS ↓ | | 5 | | | ns |
| Tmah | DS ↑ to MA(7:0) invalid | | 5 | | | ns |
| Cs | CS valid to DS ↓ | | 20 | | | ns |
| Ch | DS ↑ to CS ↓ | | 0 | | | ns |
| Tda | DS ↑ to read data valid | | | | 60 | ns |
| Tds | DS width | | 80 | | | ns |
| Tdh | DS ↑ to read data invalid | | 0 | | 25 | ns |
| Tsrw | R/$\overline{W}$ valid to DS ↓ | | 20 | | | ns |
| Thrw | DS ↑ to R/$\overline{W}$ invalid | | 20 | | | ns |
| Tdrdy | DS ↑ to READY ↓ (Motorola) | | | | 30 | ns |
| Wds | Write data valid to $\overline{WR}$ ↑ or DS ↓ | | 40 | | | ns |
| Wdh | $\overline{WR}$ ↑ or DS ↓ to write data invalid | | 10 | | | ns |

Note 1: ↑ indicates rising edge ↓ indicates falling edge

Note 2: Loading capacitor = 30 pF

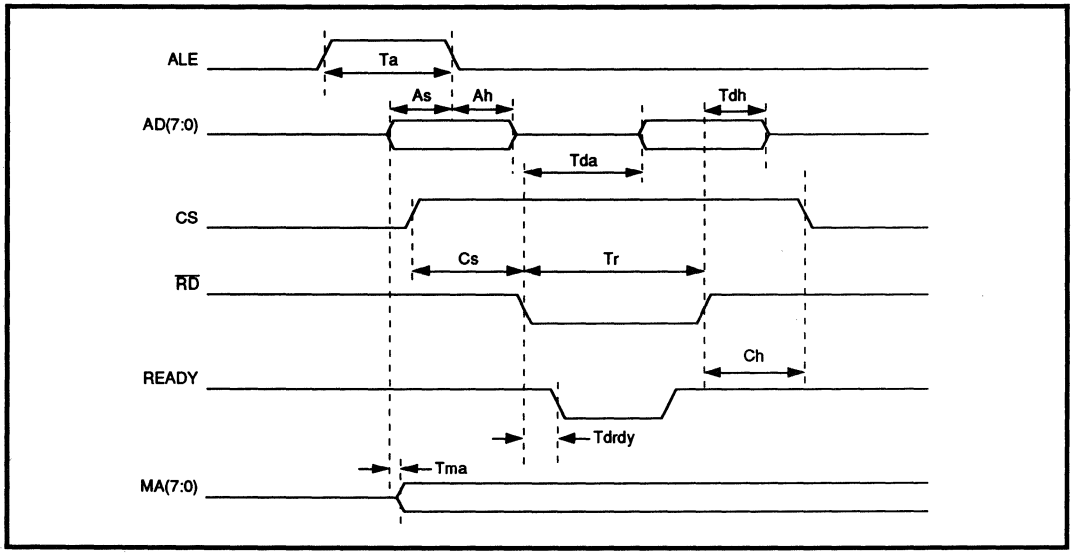


**FIGURE 2: Intel Register Multiplexed Read Timing**

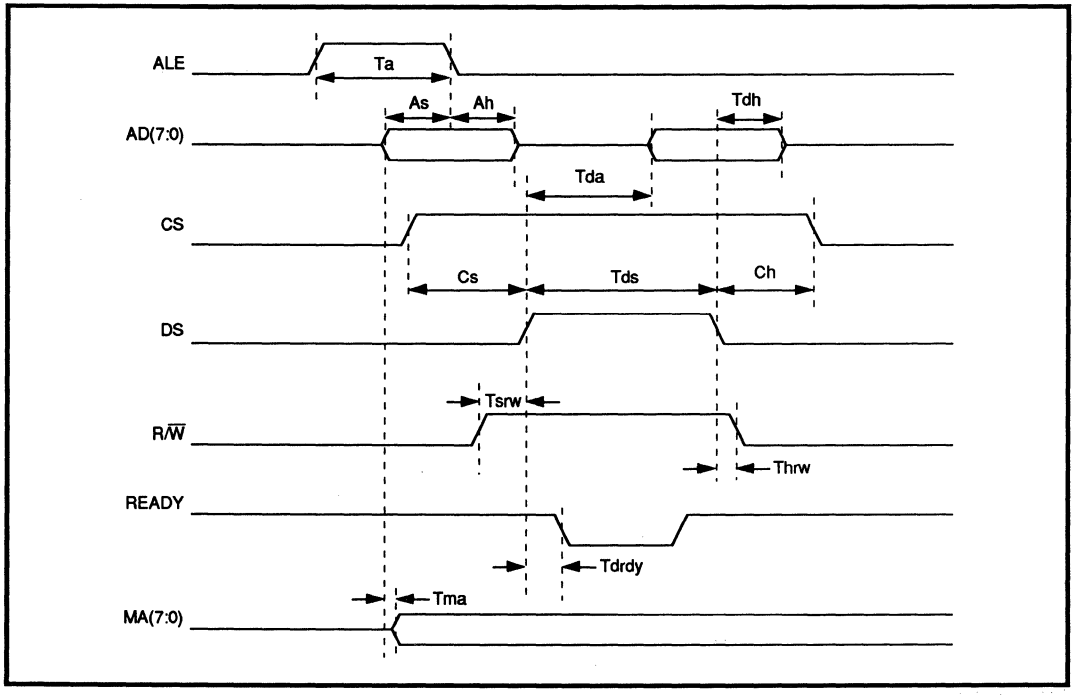


**FIGURE 3: Motorola Register Multiplexed Read Timing**

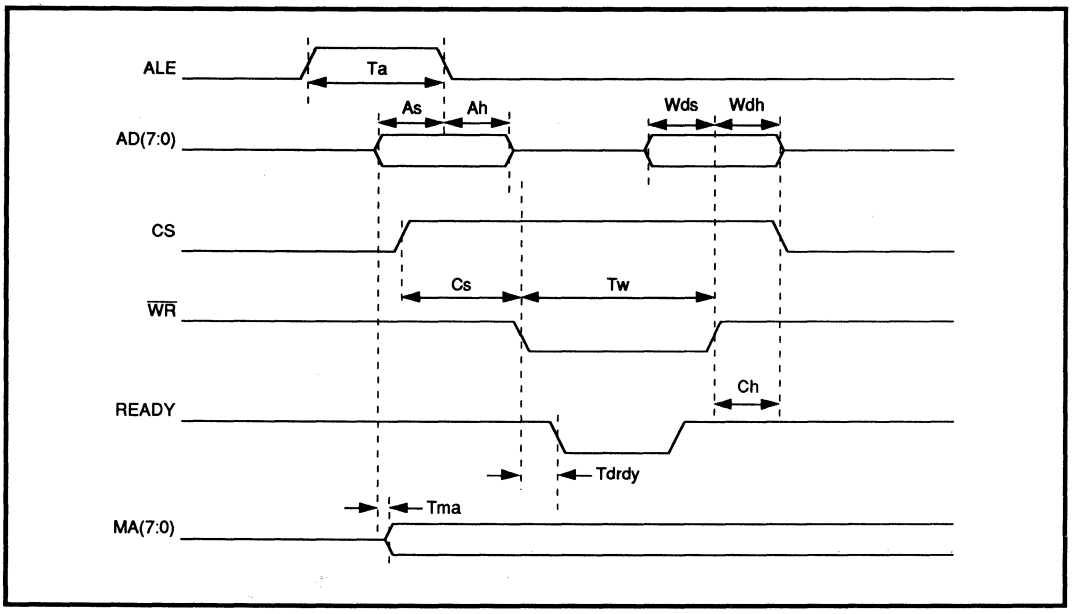


**FIGURE 4: Intel Register Multiplexed Write Timing**

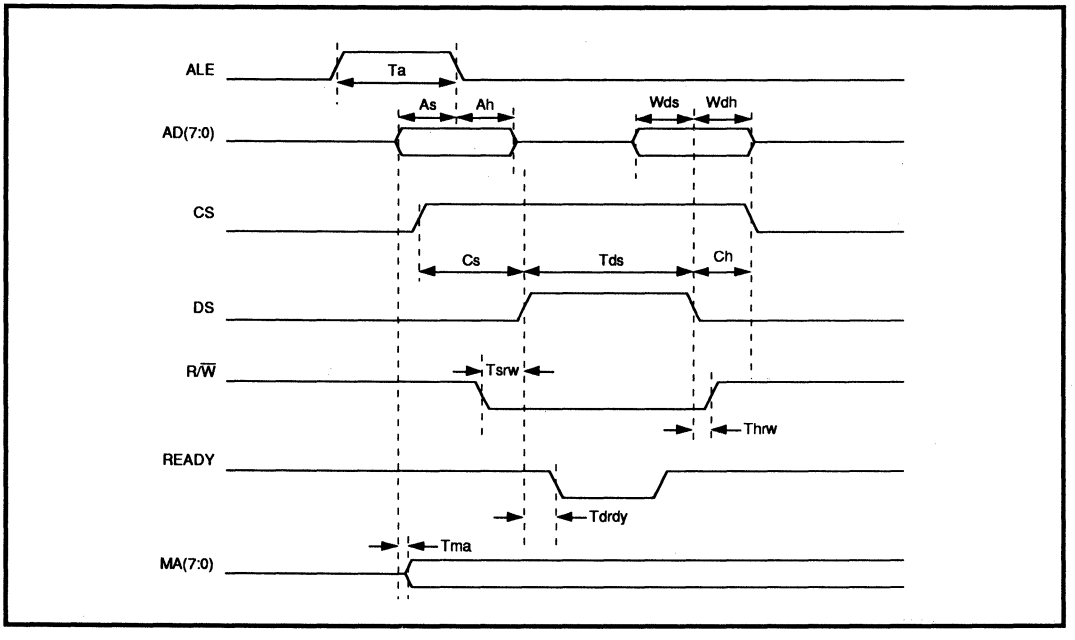


**FIGURE 5: Motorola Register Multiplexed Write Timing**

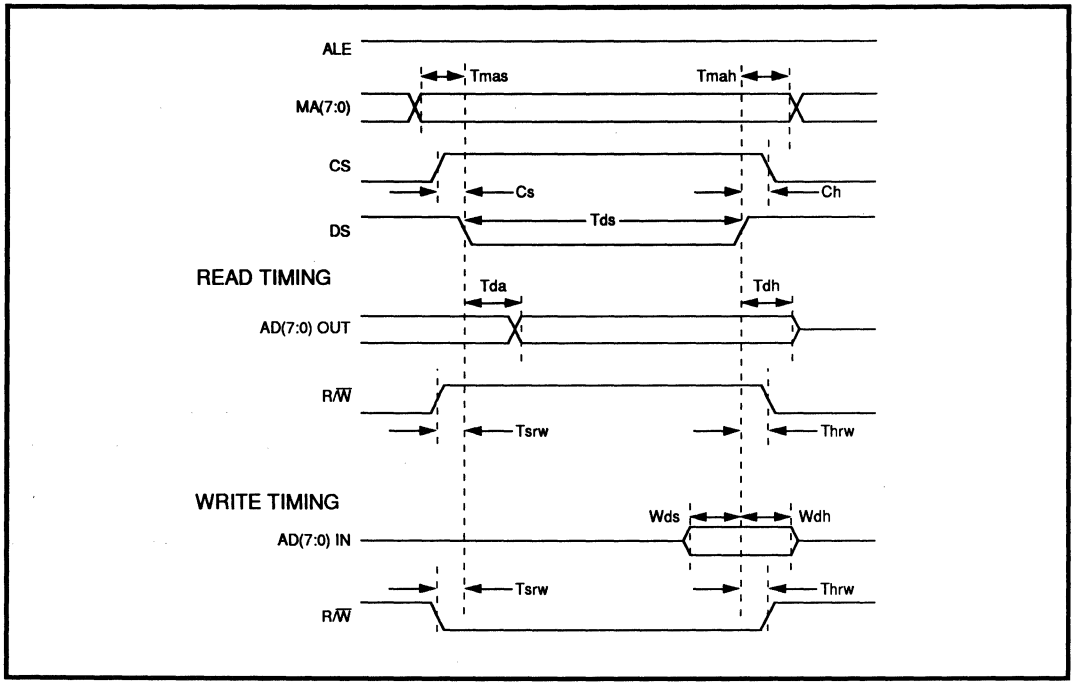


**FIGURE 6: Non-Multiplexed Bus Timing Diagrams**

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## ELECTRICAL SPECIFICATIONS (continued)

### Disk Interface Timing

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|---|
| T | RRCLK period | | 20.8 | | | ns |
| T/2 | RRCLK high/low time | | 8.5 | | | ns |
| Tr, Tf | RRCLK rise/fall time | | | | 3 | ns |
| Dis | NRZ in valid to RRCLK ↑ | | 3 | | | ns |
| Dih | RRCLK ↑ to NRZ in invalid | | 3 | | | ns |
| As | $\overline{AMD}$ valid to RRCLK ↑ | | 3 | | | ns |
| Tckd | RRCLK ↓ to WCLK ↓ or RRCLK ↑ to WCLK ↑ | | | | 8 | ns |
| Dv | WCLK ↓ to NRZ out valid | | | | ±1 | ns |

Note: ↑ indicates rising edge ↓ indicates falling edge

Loading capacitor = 10 pF

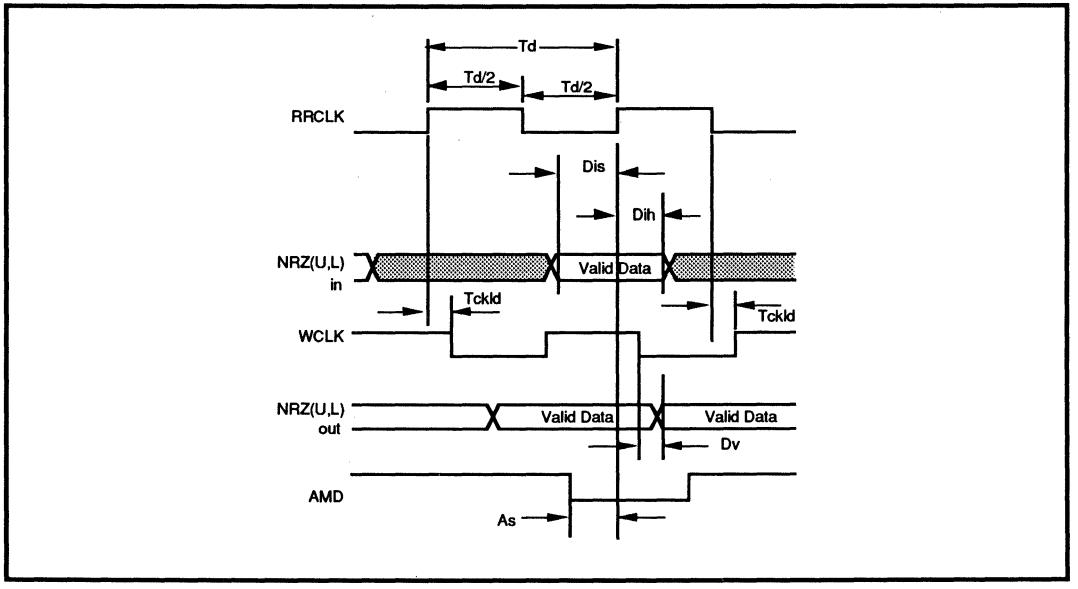



**FIGURE 7: Disk Interface Timing**

**BUFFER MEMORY READ/WRITE TIMING PARAMETERS**

| PARAMETER | | MIN | MAX | UNIT |
|---|---|---|---|---|
| T | SYSCLK period | 25 | | ns |
| T/2 | SYSCLK high/low time | 10 | | ns |
| Tav | SYSCLK / to address valid (Note 1) | | 18 | ns |
| Tmsv | SYSCLK / to $\overline{MS}$\ (Notes 1, 6) | | 18 | ns |
| Tmsh | SYSCLK / to $\overline{MS}$/ (Note 1) | | 18 | ns |
| Tmv | SYSCLK / to $\overline{MOE}$\ (Note 1) | | 18 | ns |
| Tmh | SYSCLK / to $\overline{MOE}$/ (Note 1) | | 18 | ns |
| Twv | SYSCLK / to $\overline{WE}$\ (Note 1) | | 18 | ns |
| Twh | SYSCLK / to $\overline{WE}$/ (Note 1) | | 18 | ns |
| Tdov | SYSCLK to data out valid (Note 1) | | 18 | ns |
| Tdoh | SYSCLK to data out invalid (Note 1) | | 18 | ns |
| Tdis | Data in valid to $\overline{MOE}$ / (SRAM)<br>Data in valid to $\overline{CAS}$ / (DRAM) | 5 | | ns |
| Tdih | $\overline{MOE}$ / to data in valid (SRAM)<br>$\overline{CAS}$ / to data in valid (DRAM) | 0 | | ns |
| Trv | SYSCLK / to $\overline{RAS}$\ (Note 1) | | 18 | ns |
| Trh | SYSCLK / to $\overline{RAS}$/ (Note 1) | | 18 | ns |
| Trav | SYSCLK / to row address valid (Note 1) | | 18 | ns |
| Trah | SYSCLK / to row address invalid (Note 1) | | 18 | ns |
| Tcv | SYSCLK / to $\overline{CAS}$\ (Note 1) | | 18 | ns |
| Tch | SYSCLK / to $\overline{CAS}$/ (Note 1) | | 18 | ns |
| Tcav | SYSCLK / to column address valid (Note 1) | | 18 | ns |
| Tcah | SYSCLK / to column address invalid | 0 | | ns |

## ELECTRICAL SPECIFICATIONS (continued)

### BUFFER MEMORY READ/WRITE TIMING PARAMETERS (continued)

| PARAMETER | | CONDITIONS | MIN | UNIT |
|---|---|---|---|---|
| Trwl | $\overline{RAS}$\ to $\overline{RAS}$/ | Notes 2, 3 | (RWL + 3)•T)-2 | ns |
| Trwh | $\overline{RAS}$/ to $\overline{RAS}$\ | Notes 2, 4 | (RWH + 1)•T)-2 | ns |
| Tcwl | $\overline{CAS}$\ to $\overline{CAS}$/ | Note 2 | (CWL + 1)•T)-2 | ns |
| Tcwl | $\overline{CAS}$/ to $\overline{CAS}$\ | Notes 2, 5 | (CWL + 1)•T)-2 | ns |

Note: Loading capacitance = 30 pF

Note 1: The measured delay for any of the signal indicated by this note will not vary from the measured delay of any other signal indicated by this note by more than ±1 ns.

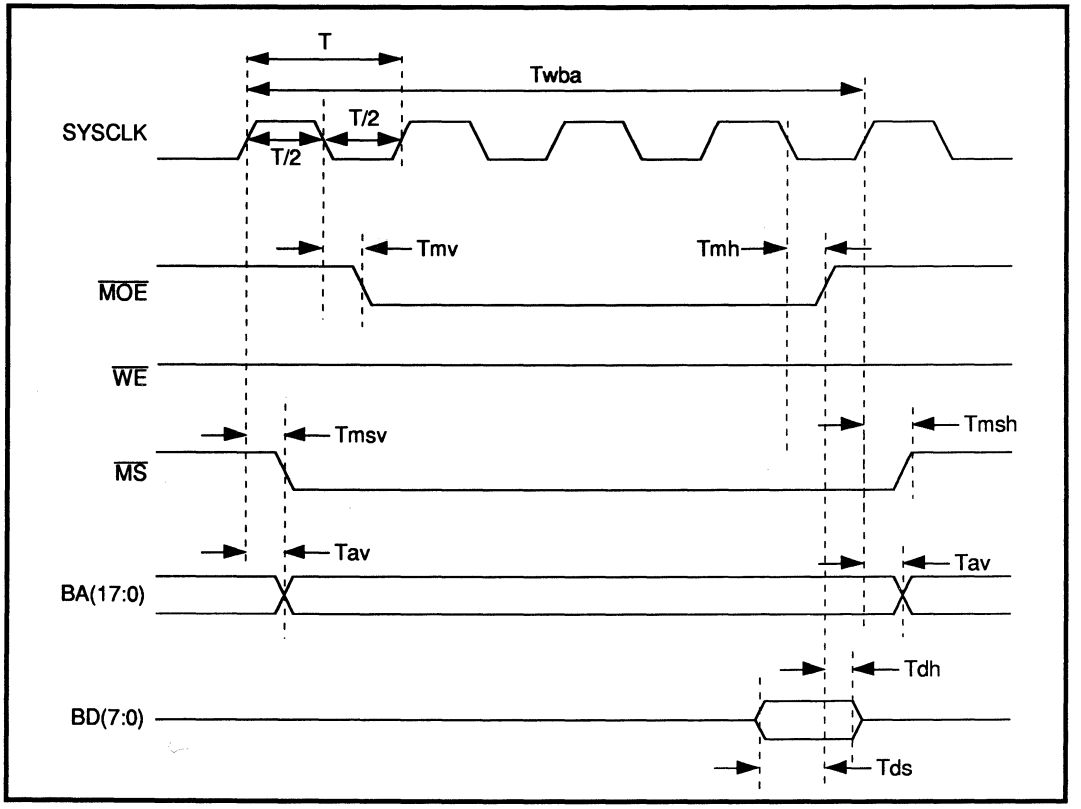
Note 2: RWL, RWH, CWL and CWH are fields in the Buffer Manager Timing Control Register (54H). Each is a two bit field which can contain a value of 0, 1, 2, or 3. These values determine the minimum number of SYSCLK periods (T) for the associated signal width.

Note 3: The minimum width value of Trwl will be generated for refresh cycles and for any buffer memory access cycle except when multiple page mode accesses are performed. When multiple page mode accesses are performed, the width of the $\overline{RAS}$ low pulse is extended until the end of the last $\overline{CAS}$ low cycle.

Note 4: The minumum value of Trwh will be generated whenever the Buffer Manager determines that a buffer request is pending at the completion of the current memory cycle and a page mode access can not be used either because page mode operation is not enabled or the needed location is not within the current page.

Note 5: The minumum value of Tcwh will be generated only between consecutive page mode accesses.

Note 6: $\overline{MS}$ will rise only if the Buffer Manager determines that no additional requests for buffer access are pending. If the Buffer Manager determines that another access is to be Made, $\overline{MS}$ is kept low between the accesses for improved speed.




Note: Twba is a functional parameter that gives the duration of one RAM data buffer access cycle in SYSCLK periods. The value is programmed in bits 1-0 of register 54H. These examples show Twba = 4T.

**FIGURE 8: SRAM Read Timing**

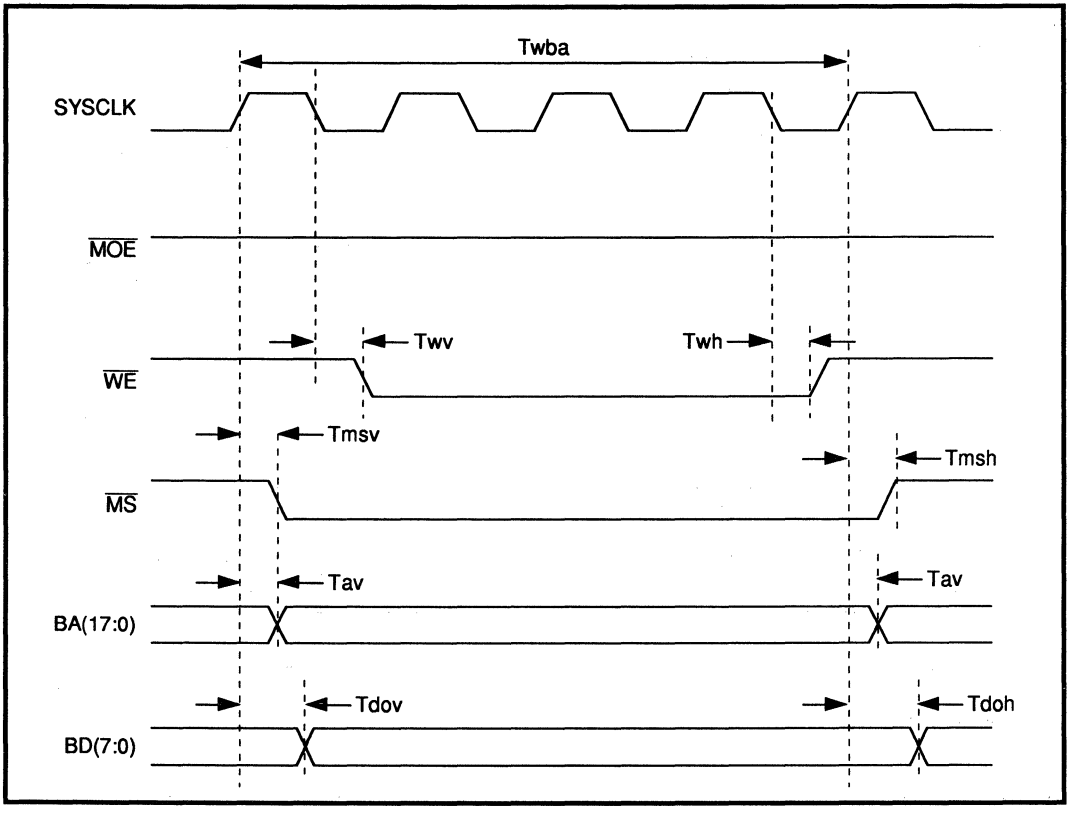



**FIGURE 9: SRAM Write Timing**

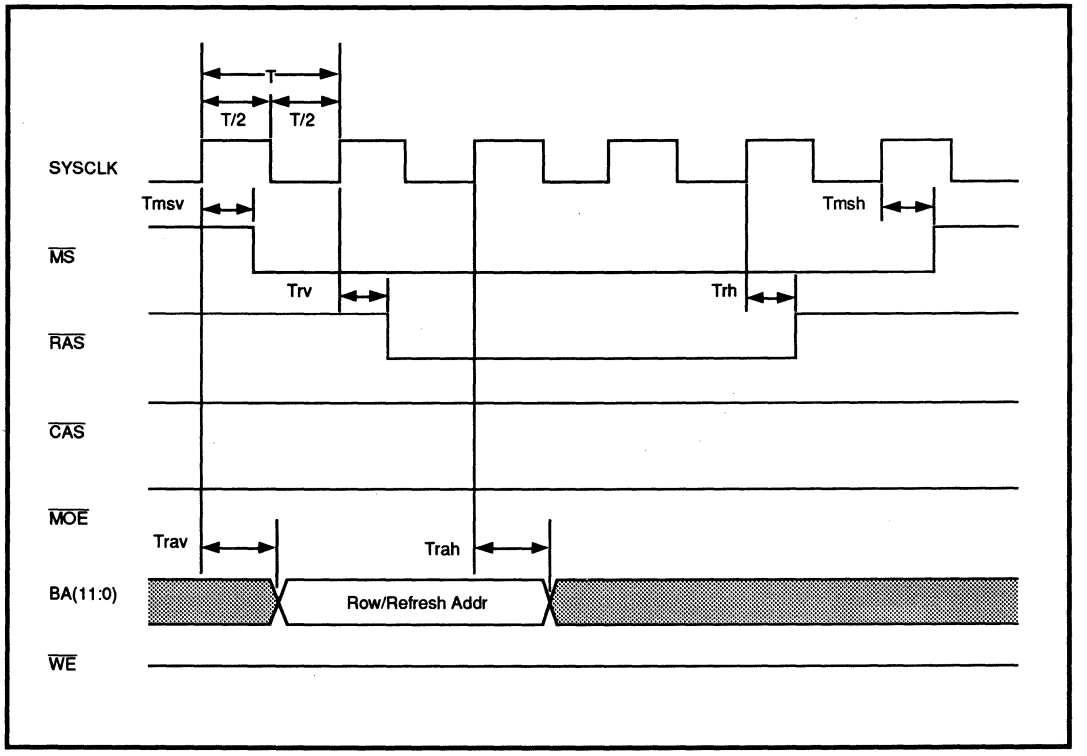



**FIGURE 10: DRAM Timing, Refresh Cycle (Shown with WRL = 0)**

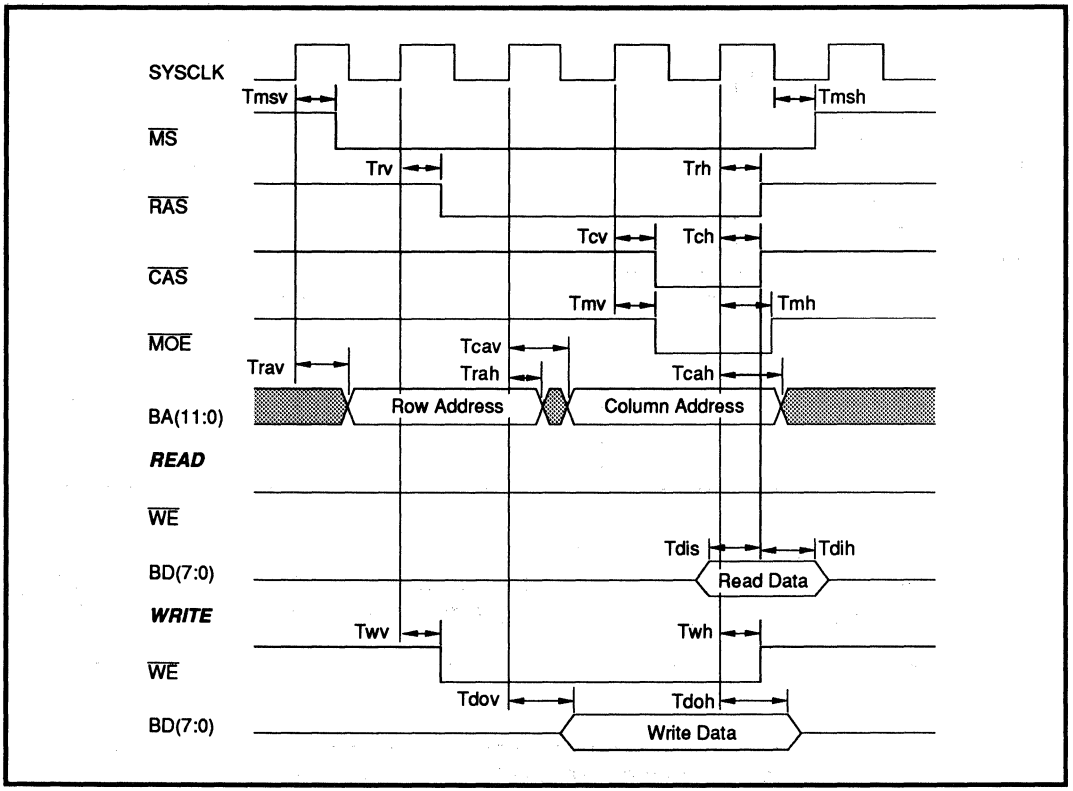



**FIGURE 11: DRAM Timing, Standard Cycle (Shown with RWL = 0 and CWL = 0)**

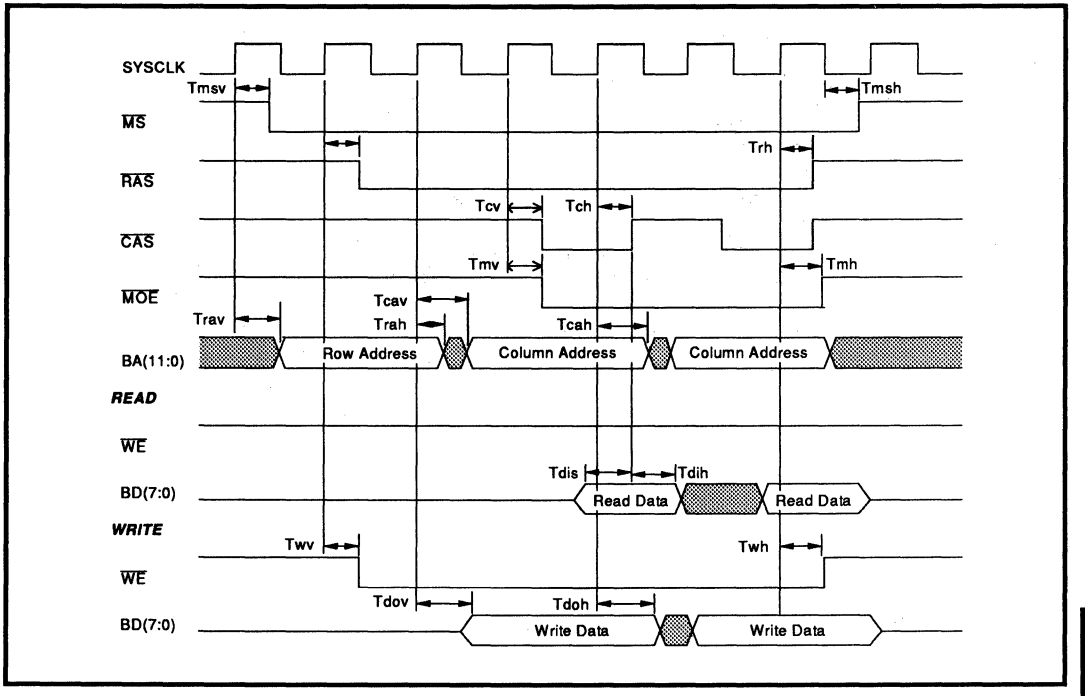



**FIGURE 12: DRAM Timing, Fast Page Cycles (Shown with RWL = 0, RWH = 0, CWL = 0 and CWH = 0)**

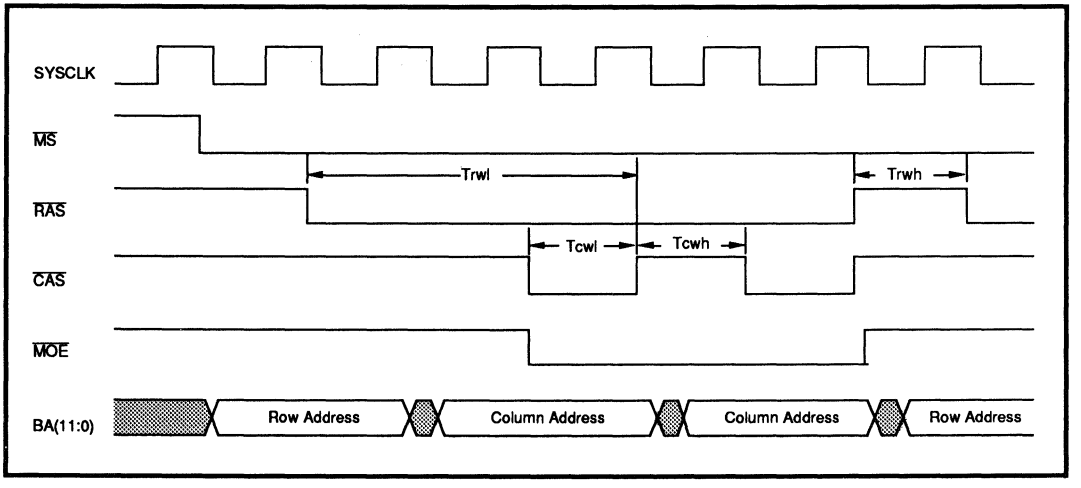



**FIGURE 13: DRAM Timing (Showing the Relationship of RWL, RWH, CWL and CWH to overall timing)**

**SCSI Asynchronous Timing Paraemeters**

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|---|
| Tods | Data Setup to $\overline{ACK}$\ | SCSI Output Phase | 5 | | | ns |
| Todh | Data Hold from $\overline{ACK}$\ | SCSI Output Phase | 12 | | | ns |
| Talrh | $\overline{ACK}$\ to $\overline{REQ}$/ | | | | 49 | ns |
| Tids | Data Setup to $\overline{REQ}$ \ | SCSI Input Phase | 80 | | | ns |
| Tidh | Data Hold from $\overline{ACK}$\ | SCSI Input Phase | 29 | | | ns |

Note: All timing parameters are measured with 200 pf load, two SCSI terminator loads with $\overline{ACK}$ Filter turned off.

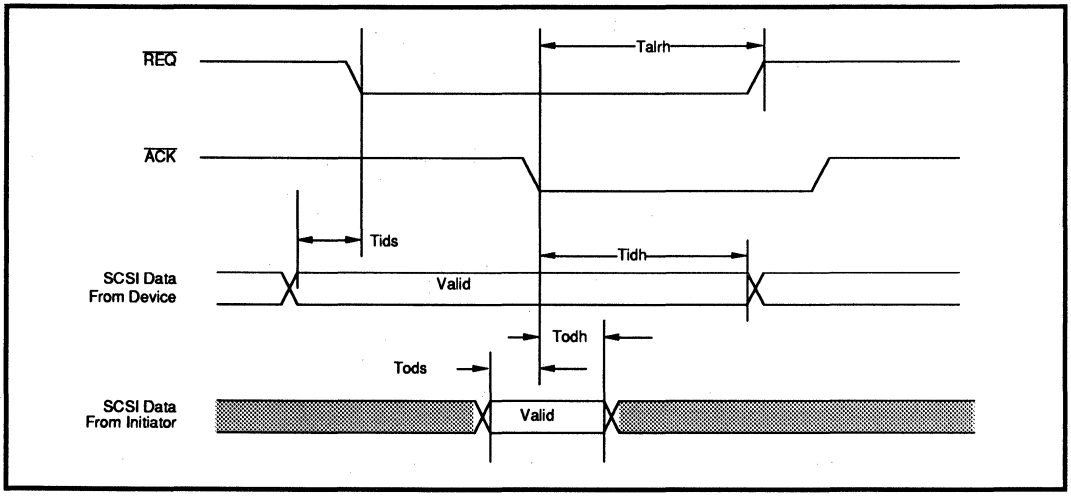



**FIGURE 14: SCSI Asynchronous Timing**

**SCSI Synchronous Timing Paramenters**

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|---|
| Trh | $\overline{REQ}$ Assertion Time | | 37 | | 48 | ns |
| Trl | $\overline{REQ}$ Deassertion Time | | 63 | | 52 | ns |
| Tids | Setup time SCSI Data to $\overline{REQ}$\ | Write to SCSI bus | 43 | | | ns |
| Tidh | Hold time $\overline{REQ}$\ to SCSI Data invalid | Write to bus | 43 | | | ns |
| Tal | Minimum $\overline{ACK}$ Assertion Width Required | | 10 | | | ns |
| Tods | Data Setup to $\overline{ACK}$\ | Read from the SCSI bus | 5 | | | ns |
| Todh | Data Hold from $\overline{ACK}$\ | Read from the SCSI bus | 12 | | | ns |

Note: All timing parameters are measured with 200 pf load, two SCSI terminator loads, $\overline{ACK}$ filter turned off.

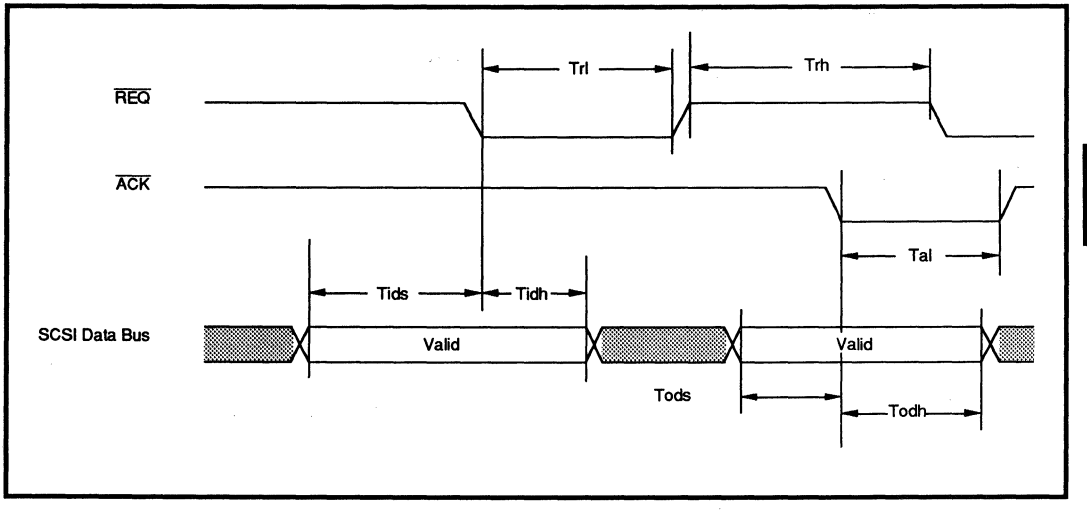



**FIGURE 15: SCSI Synchronous Timing**

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**Synchronous Data In/Out Phase**

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|---|
| Txtrp* | Synchronous Transfer Period | (see note) | | | | ns |
| Tsrl | SYSFREQ high to $\overline{REQ}$ low | | | | 50 | ns |
| Tsrh | SYSFREQ high to $\overline{REQ}$ high | | | | 60 | ns |
| Tdov | SYSFREQ high to data out valid | | | | 40 | ns |
| Tdsu | Data setup to $\overline{ACK}$ low | | 55 | | | ns |
| Tdh | Data hold from $\overline{ACK}$ low | | 40 | | | ns |

Note: Txtrp is the Synchronous Transfer Period as defined by the Synchronous Control Register (Reg: 43H). SYSFREQ is a function of the BUFCLK and is determined by the prescale value as defined by the Clock Control Register (Reg: 49H).

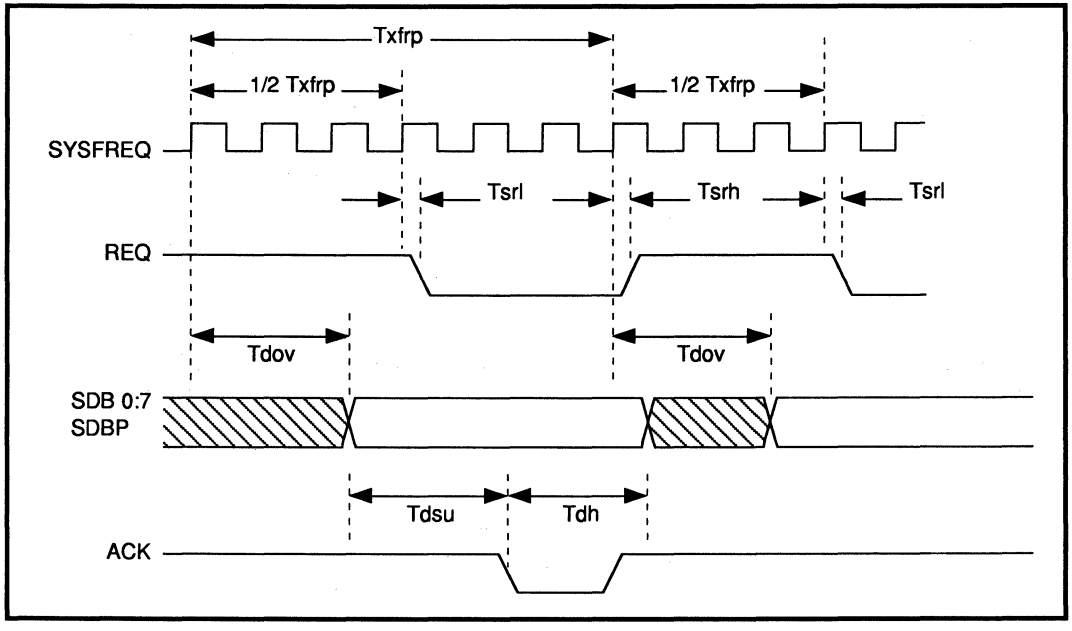


**FIGURE 16: Even Number of SYSFREQ Cycles/SCSI Transfer Period**

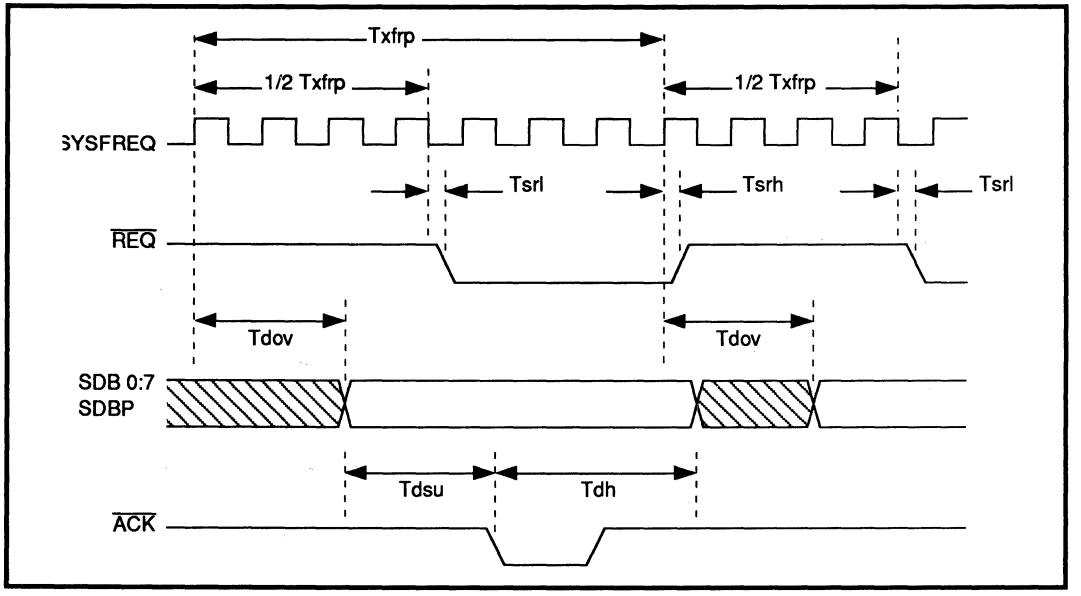


**FIGURE 17: Odd Number of SYSFREQ Cycles/SCSI Transfer Period**

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**Wait for Selection**

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|---|
| Tbsd | Bus Settle Delay (400 ns) to the assertion of $\overline{BSY}$ | | 3T + 90 | | 4T + 90 | ns |

Note: T is the SCSI Clock Period (SCP) as defined in Register 49H (CLKCTL).

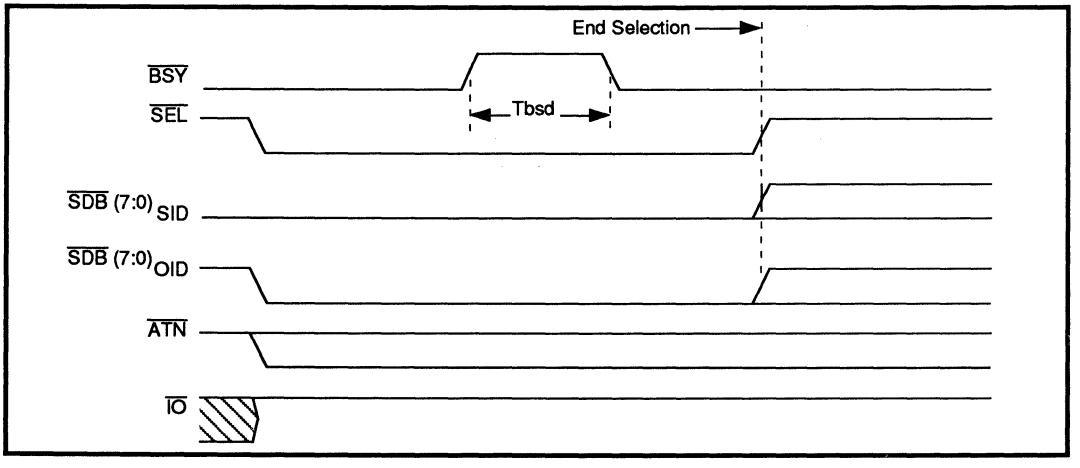



**FIGURE 18: Wait for Selection**

**Arbitration**

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|---|
| Tbfsd | Bus Settle Delay (400 ns) + Bus Free Delay (800 ns) to the assertion of BSY and $\overline{SDB}_{OID}$ | | 6T + 110 | | 7T + 110 | ns |
| Tad | Arbitration Delay (2.4 µsec) to the assertion of $\overline{SEL}$ (win) or deassertion of $\overline{BSY}$ and $\overline{SDB}_{OID}$ (lost) | | - | | 13T + 100 | ns |
| Tbcsd | Bus Clear Delay (800 ns)+ Bus Settle Delay (400 ns) to end of Arbitration Phase | | - | | 6T + 100 | ns |

Note: T is the SCSI Clock Period (SCP) as defined in Register 61H (CLKCTL).

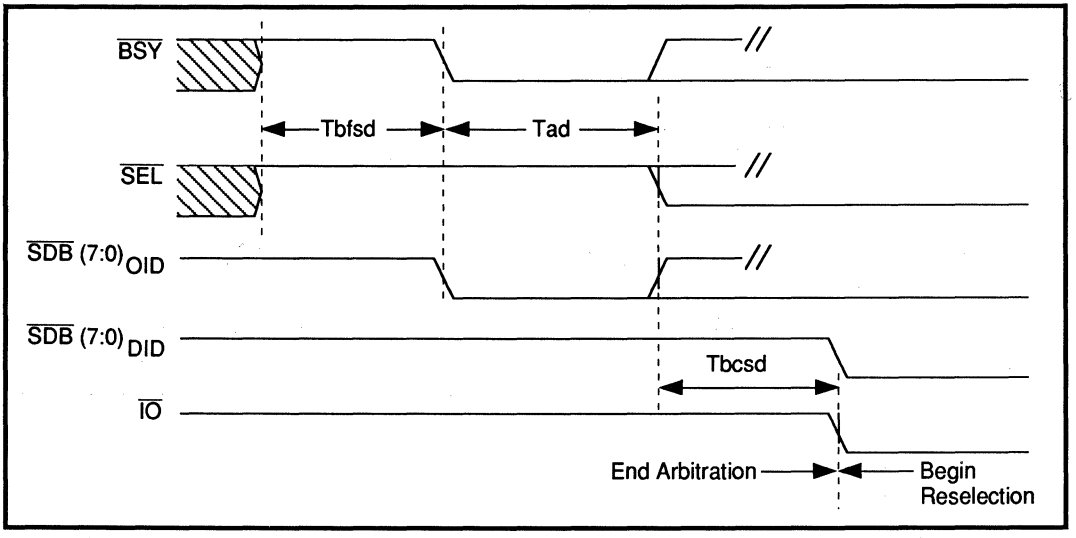



**FIGURE 19: Arbitration**

**Reselection**

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|---|
| Tbcsd | Bus Clear Delay (800 ns) + Bus Settle Delay (400 ns) to end of Arbitration Phase | | - | | 6T + 100 | ns |
| Tdskd1 | Two Deskew Delays (90 ns) to the deassertion of $\overline{BSY}$ | | - | | 160 | ns |
| Tbsd | Bus Settle Delay (400 ns) to the assertion of $\overline{BSY}$ | | - | | 2T + 40 | ns |
| Tdskd2 | Two Deskew Delays (90 ns) to the deassertion of SEL, $\overline{SDB}_{OID}$, and $\overline{SDB}_{DID}$ | | 1T +70 | | 2T + 70 | ns |

Note: T is the SCSI Clock Period (SCP) as defined in Register 61H (CLKCTL).

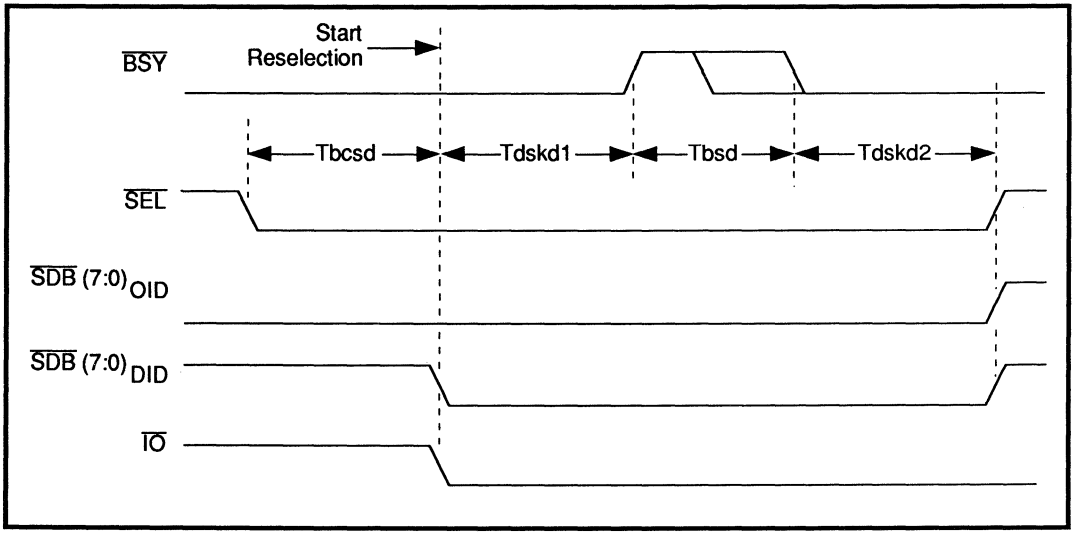
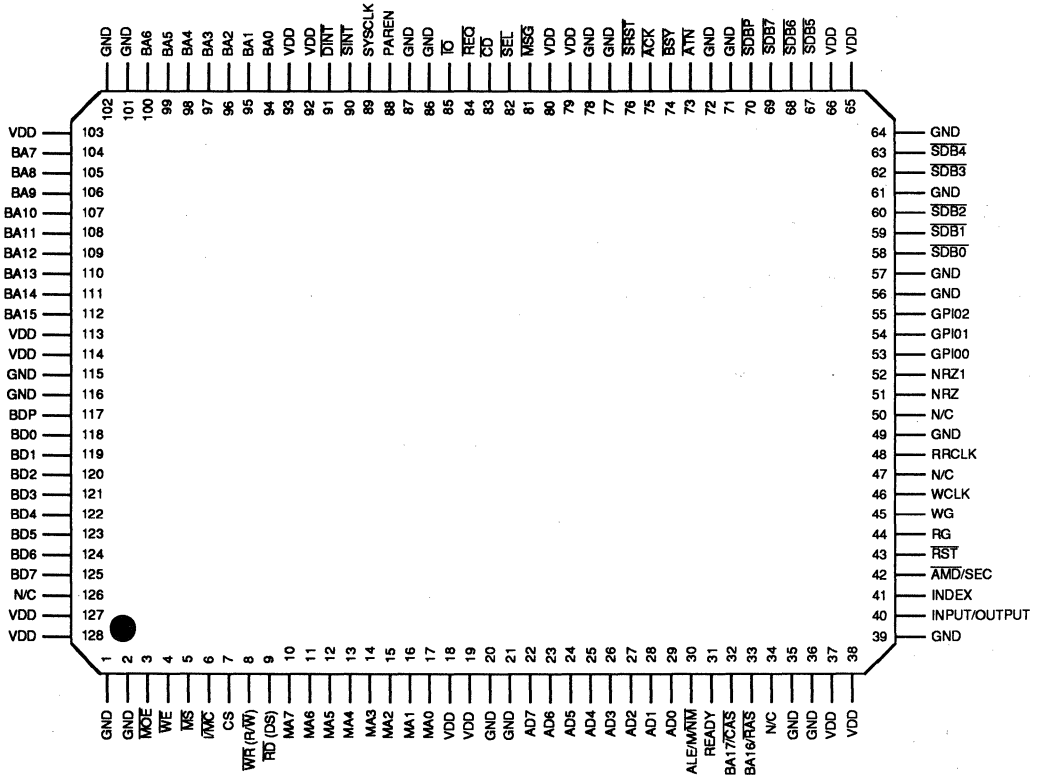



**FIGURE 20: Reselection**

# SSI 32C9023
# SCSI Combo Controller
# 72 Mbit/s; dual bit NRZ interface

## PACKAGE PIN DESIGNATIONS
(Top View)




**128-Lead QFP**

**Advance Information:** Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.



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silicon systems®
A TDK Group Company

# SSI 32C9301
## PC-AT Combo Controller With Reed Solomon, 3V Operation
## Advance Information

January 1993

## DESCRIPTION

The SSI 32C9301 is an advanced CMOS VLSI device which integrates major portions of the hardware needed to build an ATA disk drive. The SSI 32C9301 can operate on 3.3 volts or 5 volts allowing use in 3.3 volt or 5 disk drives. In addition, the 32C9301 can operate in a 3.3 volt drive and interface with a 5 volt host system. The circuitry of the SSI 32C9301 includes a complete ATA interface, an advanced buffer manager, a high performance disk formatter and an 88 bit Reed-Solomon ECC with fast "on-the-fly" hardware correction. The SSI 32C9301 provides maximum performance while minimizing micro controller intervention.

When operating in a 3.3 volt environment, the SSI 32C9301 is capable of concurrent transfers of up to 32 megabits per second on the disk interface and 3 megawords (16 bit transfers) per second across the

(continued)

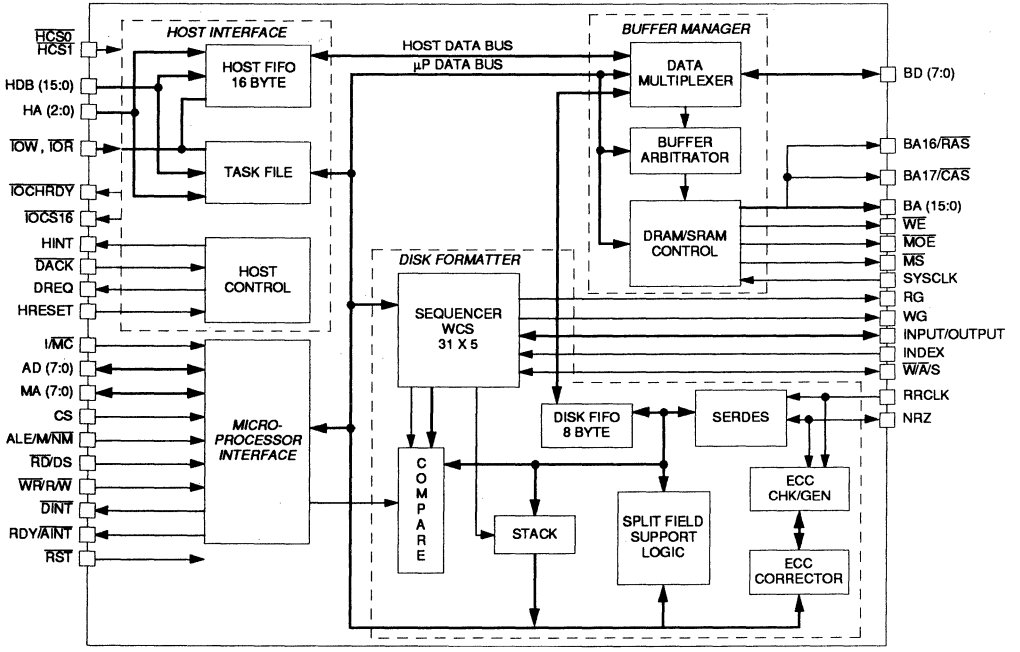
## FEATURES

- **ATA Interface**
  - **Single Chip PC AT Controller**
  - **Full ANSI ATA Compliance**
  - **Direct PC Bus connection with on board 16 mA (24 mA @5v) drivers**
  - **PC transfers to 3 (6 @5v) megawords per second**
  - **Supports PIO, DMA and EISA Class B Demand DMA**
  - **Logic for daisy chaining 2 drives**
  - **Automatic command decoding of write, write buffer and format commands**
  - **Automatic updates of the host task file registers in both Cyl/Hd/Sec and LBA modes**

(continued)

8

## BLOCK DIAGRAM



# SSI 32C9301
# PC-AT Combo Controller
# With Reed Solomon, 3V Operation

## DESCRIPTION (continued)

ATA bus. In a 5 volt environment, the SSI 32C9301 is capable of concurrent transfers of up to 48 megabits per second on the disk interface and 6 megawords per second across the ATA bus. The SSI 32C9301 is capable of performing concurrent disk data transfers, host data transfers, on-the-fly error corrections and micro controller accesses of the buffer memory without any degradation of performance on any interface.

The SSI 32C9301 is one of a family of Silicon Systems' single chip disk controllers which support a wide range of device interfaces. The SSI 32C9001 is a 5 volt only version of the 32C9301 which is 100% firmware and pin out compatible. The 32C9302 is another 3.3/5 volt ATA controller which supports a dual NRZ disk formatter interface. The SSI 32C9020, 32C9022 and 32C9023 family members are SCSI disk controllers providing many of the same features as the SSI 32C9301. The SSI 32C9340 and 32C9342 disk controllers complete the family by providing PCMCIA/ ATA compliant interfaces. All members are based on a common architecture allowing major portions of firmware to be reused. The Silicon Systems' chip family is illustrated in hierarchy chart shown in Figure 1.

The high level of integration within the SSI 32C9301 represents a major reduction in parts count. When the SSI 32C9301 ATA Controller is combined with the SSI 32R2300 Read/Write device, the SSI 32P4330 Pulse Detector with 1,7 ENDEC, the 32H6300 Servo and Motor Speed Controller, an appropriate micro controller and memory, a complete, cost efficient, high performance intelligent drive solution is created.

## FEATURES (continued)

- Hardware added to provide Multi-Sector data transfers without microprocessor intervention
- Automatic Host Interrupt and Busy for multiple sector transfers
- 16 byte FIFO to improve performance
- Separate host interface VDD to allow 3.3 volt drives to plug into 5 volt systems
- Power Down I/O pins

- Buffer Manager
  - Direct support of DRAM or SRAM
  - SRAM: up to 256k bytes of memory with throughput to 10 (20 @5v) megabytes per second
  - DRAM: up to 1 megabyte of memory with throughput to 8 (17.78 @5v) megabytes per second
  - Programmable memory timing
  - Supports page mode DRAM access
  - Programmable page mode burst length
  - Programmable DRAM refresh period
  - Buffer RAM segmentation with flexible segment sizes from 256 bytes to 1 megabyte
  - Dedicated host, disk and microprocessor address pointers
  - Buffer Streaming with internal buffer protection circuit providing buffer integrity
  - Multiple sector host transfers
- Disk Formatter
  - NRZ Data Rates to 32 (48 @5v) megabits per second
  - Automatic multi-sector transfer
  - Header or microprocessor based split data field support
  - Advanced sequencer organized in 31 x 5 bytes
  - Advanced branch and interrupt logic
  - 88-bit Reed Solomon ECC with "on-the-fly" fast hardware correction circuitry
  - Capable of correcting up to four 10-bit symbols in error
  - Guaranteed to correct one 31-bit burst or two 11-bit bursts
  - Hardware on-the-fly correction of either an 11- or 31-bit single burst error within one half of a sector time
  - Detects up to one 51-bit burst or three 11-bit bursts
- Microprocessor Interface
  - Supports both Intel and Motorola microprocessors
  - Separate host and disk interrupts
- Other Features
  - Internal power down mode
  - Available in 100-pin QFP or TQFP
  - Automatic power supply level detection
  - Conforms to JEDEC 3.3 volt specifications
  - TTL compatible input receivers at 3.3V or 5V

## FUNCTIONAL DESCRIPTION

The SSI 32C9301 contains the following four major functional blocks:

Microprocessor Interface

ATA Interface

Disk Formatter

Buffer Manager

The Microprocessor Interface allows the local microprocessor access to all of the SSI 32C9301 internal control registers and any location within the buffer memory. The microprocessor, by writing and reading the internal registers, can control all activities of the SSI 32C9301. The microprocessor can elect to perform host and/or disk operations directly, or it can enable the advanced features of the SSI 32C9301 which can perform these operations automatically.

The ATA Interface block handles all PC AT bus activities. The ATA interface includes 16 mA (24 mA @5v) drivers allowing for direct connection of the SSI 32C9301 to the PC AT bus. The ATA interface block is highly automated, capable of performing multiple block transfers without micro controller involvement. The ATA block interfaces directly with the Buffer Manager via an internal speed matching FIFO. This FIFO, the bandwidth capabilities of the Buffer Manager, plus the advanced features of the ATA Interface guarantee sustained full speed transfers across the PC AT bus.

The Disk Formatter performs the serialization and deserialization of data. It provides all of the necessary functions to control track formatting, header search, and the reading and writing of data. The heart of the Disk Formatter is an advanced programmable sequencer. The sequencer can contain 31 instructions, each of which is 5 bytes (40 bits) in width. The width of the instructions allows for sophisticated branching techniques which increase the flexibility and power of the sequencer. The disk interface can be configured through a wide range of capabilities, allowing the SSI 32C9301 to interface with nearly any read/write channel. This allows the user of the SSI 32C9301 to select the read/write channel best suited to the device. Of course, by selecting the SSI 32C9301 controller and the SSI 32P4330 Read Channel with 1,7 ENDEC, you are guaranteed a problem free interface.

Within the Disk Formatter are the ECC generator/checker and ECC corrector. The generator/checker provides the ability to generate or check a 32 bit ECC for headers and an 88 bit Reed Solomon code for data. If the checker detects an error using the 88 bit Reed Solomon code, the syndrome information is transferred into the corrector. The corrector then performs the necessary operations to determine if the error was correctable and, if it was correctable, the corrector interfaces directly with the buffer controller and performs the correction automatically. The corrector performs its correction within one quarter of a sector. This guarantees that the corrector will always be available to correct the next sector if necessary.

As its name implies, the Buffer Manager manages the data buffer of the controller. The Buffer Manager can support either SRAM or DRAM. When configured to operate with DRAM, the Buffer Manager automatically

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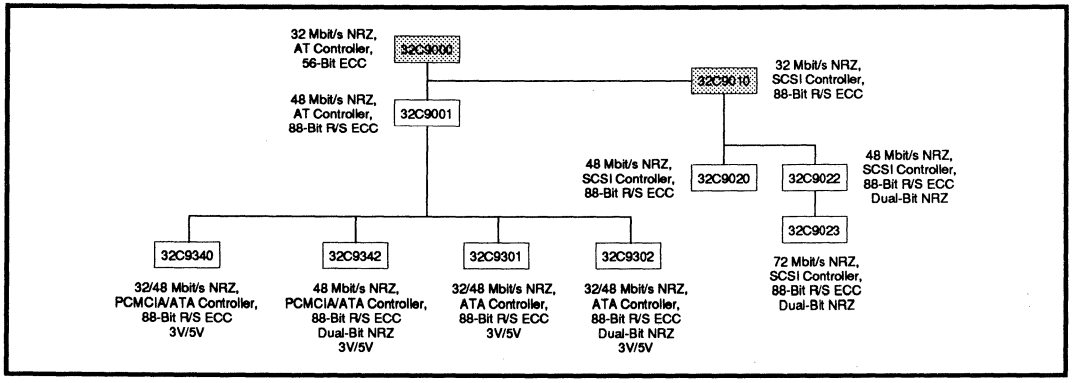


**FIGURE 1: Silicon Systems' Disk Controller Chip Hierarchy**

## FUNCTIONAL DESCRIPTION (continued)

performs necessary refresh cycles. The buffer manager creates all of the necessary timing and control signals for a wide range of memory types and speeds. Besides interfacing with the buffer memory, the Buffer Manager interfaces with the ATA Interface block, the Disk Formatter block, the ECC corrector of the Disk Formatter block and the microprocessor. If more than one of these devices requires access to the buffer memory, the Buffer Manager arbitrates the requests automatically. The Buffer Manager of the SSI 32C9301 can sustain ATA operations at the rate of 3 (6 @5v) megawords per second, Disk Formatter operations at 32 (48 @ 5v) megabits per second and still has sufficient band width left to handle on-the-fly ECC corrections and microprocessor accesses without degrading performance on any of the interfaces.

## PIN DESCRIPTION

The following convention is used in the pin description:

- (I) denotes an input
- (I/S) denotes a Schmitt trigger input
- (O) denotes an output
- (I/O) denotes a bidirectional signal
- (Z) denotes a tri-state output
- (OD) denotes an open drain output

Active low signals are denoted by a bar on top of the signal name and dual function pins are denoted with a slash between the two signals — A9/$\overline{\text{HCS1}}$.

**GENERAL**

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| VDD | | POWER SUPPLY PIN, VCC |
| GND | | GROUND |

**HOST INTERFACE**

| | | |
|---|---|---|
| A(2:0) | I | HOST ADDRESS LINES. The Host Address lines A(2:0) and A9 are used to access the various PC/AT control/status, and data registers. |
| A9/$\overline{\text{HCS1}}$ | I | HOST ADDRESS LINE 9/HOST CHIP SELECT 1. This is a multiplexed input pin. When Register 48H-bit 3 is reset this input is HOST ADDRESS LINE 9, when the bit is set this input is HOST CHIP SELECT 1. |
| $\overline{\text{HCS0}}$ | I | HOST CHIP SELECT 0. This pin selects access to the control, status and data registers. |
| $\overline{\text{IOCS16}}$ | OD | 16 BIT DATA TRANSFER. An open drain active low output that indicates that a 16-bit buffer transfer is active. |
| HINT | O | HOST INTERRUPT. Asserted active high to indicate to the Host that the controller needs attention. |

**HOST INTERFACE** (continued)

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| $\overline{\text{IOCHRDY}}$ | O,Z | I/O CHANNEL READY. Active low, this signal is asserted whenever the internal host FIFO is not ready to transfer data. |
| DREQ | O,Z | DMA REQUEST. The active high DMA Request signal is used during DMA transfer between the Host and the SSI 32C9301. |
| $\overline{\text{DACK}}$ | I | DMA ACKNOWLEDGE. This active low signal is used during DMA to complete the DMA handshake for data transfer between the host and the controller. |
| $\overline{\text{IOR}}$ | I | INPUT READ SELECT. This active low pin is asserted by the Host during a Host read operation. When asserted with $\overline{\text{HCS0}}$, $\overline{\text{HCS1}}$, or $\overline{\text{DACK}}$, data from the device is enabled onto the host data bus. |
| $\overline{\text{IOW}}$ | I | INPUT WRITE SELECT. Asserted active low by the HOST during a HOST write operation. When asserted with $\overline{\text{HCS0}}$, $\overline{\text{HCS1}}$, or $\overline{\text{DACK}}$, data from the host data bus is strobed into the device. |
| $\overline{\text{HRESET}}$ | I | HOST RESET. This active low signal stops all commands in progress and initializes the control/status registers. This signal can also "wake up" the device while it is in power down mode. |
| HDB(15:0) | I/O | HOST DATA BUS. These bits are used for word transfers between the Buffer Memory and the Host; bits (7:0) are used for status, commands, or ECC byte transfers. |

**DISK INTERFACE**

| | | |
|---|---|---|
| INDEX | I | INDEX. This input is a pulse that occurs once per revolution and defines the start of first sector. |
| OUTPUT | O | DISK SEQUENCER OUTPUT. This pin is controlled by bit 2 of the control field of the disk sequencer. |
| INPUT | I | INPUT. This signal is used to synchronize the disk sequencer to an external event. |
| $\overline{\text{WAM}}$/$\overline{\text{AMD}}$/ SECTOR | I/O | WRITE ADDRESS MARK/SECTOR/ADDRESS MARK DETECT. This pin is configured to operate in Hard or Soft Sector mode by initializing the Disk Formatter Mode Control Register: 4FH, bit 1. In the hard sector mode it is used as the sector input — a pulse on this pin indicates a sector mark is found.<br>In the soft sector mode, an active low output is asserted when formatting to allow writing of address mark. When reading, an active low input indicates an address mark was detected. The device powers up in soft sector mode. |
| RG | O | READ GATE. This active high output enables the reading of the disk. It is asserted at the beginning of the PLO for header and data field by the sequencer — sequencer Control Field bits 5 and 6. It is automatically deasserted at the end of the CRC or ECC. |
| WG | O | WRITE GATE. This active high output enables writing onto the disk. It is asserted and deasserted by the sequencer Control Field bits 5 and 6. |

8

## PIN DESCRIPTION (continued)

### DISK INTERFACE (continued)

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| RRCLK | I | READ/REFERENCE CLOCK. This pin is used in conjunction with the NRZ pin to clock data in and out of the SSI 32C9001 device. This input must be glitch-free to ensure correct operation of the chip. |
| NRZ | I/O | NON RETURN TO ZERO. This signal is the serial read data input from the disk drive when the read gate signal is asserted; it is the write data output to the disk drive when the write gate signal is asserted. |

### MICROPROCESSOR INTERFACE

| | | |
|---|---|---|
| $\overline{RST}$ | I/S | RESET. An asserted active low input generates a component reset that holds the internal registers of the SSI 32C9301 at reset, stops all operations within the chip, and deasserts all output signals. All input/output signals and Host outputs are set to the high-Z state. |
| ALE/M/$\overline{NM}$ | I | ADDRESS LATCH ENABLE/MULTIPLEXED/NON-MULTIPLEXED ADDRESS SELECT. When tied high or left floating after reset, the microprocessor interface is configured as non-multiplexed. When driven low, then the microprocessor interface is configured as multiplexed. In this case this pin functions as the address latch enable, and the MA(7:0) pins are the demultiplexed address outputs. |
| CS | I | CHIP SELECT. This signal must be asserted high for all microprocessor accesses to the registers of this chip. |
| $\overline{WR}$/R/$\overline{W}$ | I | WRITE STROBE/READ/WRITE. In the Multiplexed Microprocessors bus mode, when an active low signal is present with CS signal asserted high, the data on the AD0:7 is written to the internal registers.<br><br>In the Non-Multiplexed Microprocessors bus mode, this signal acts as the R/$\overline{W}$ signal. A high on this input along with the $\overline{RD}$/DS signal high and the CS signal asserted high indicates a read operation. A low on this input along with the $\overline{RD}$/DS signal asserted and the CS signal asserted high indicates a write operation. See table below. |

| I/$\overline{MC}$ | CS | $\overline{WR}$/R/$\overline{W}$ | $\overline{RD}$/DS | Action | Mux/Non-Mux |
|---|---|---|---|---|---|
| High | High | Low | High | Write to internal registers. | M |
| High | High | High | Low | Read from internal registers. | M |
| Low | High | Low | High | Write to internal registers. | N |
| Low | High | High | High | Read from internal registers. | N |
| X | Low | X | X | No action. | M or N |

Note: X denotes don't care.

| | | |
|---|---|---|
| $\overline{RD}$/DS | I | READ STROBE/DATA STROBE. In the Multiplexed Microprocessors bus mode, when an active low signal is present with CS signal high, internal registers will be accessed.<br><br>In the Non-Multiplexed Microprocessors mode, this signal acts as the DS signal. A high on the DS, R/$\overline{W}$, and the CS signals, indicates a read operation. A low on the R/$\overline{W}$ signal, highs on both the DS and the CS, indicates a write operation to the internal registers. |

**MICROPROCESSOR INTERFACE** (continued)

| | | |
|---|---|---|
| $\overline{DINT}$ | O, OD, Z | INTERRUPT. An active low signal indicates the controller is requesting microprocessor service from the disk side. This signal is programmable for either a push-pull with an internal pull up resistor or open-drain output circuit. This signal powers up in the high-Z state. Disk Formatter Mode Control Register, 4FH: bit 3 set high, programs this pin as a push-pull, and when set low programs it as an open drain output signal. |
| AD(7:0) | I/O | ADDRESS/DATA BUS. When configured in the Multiplexed Microprocessors mode, these lines are multiplexed, bidirectional data path to the microprocessor. During the beginning of the memory cycle the bus captures the low order byte of the microprocessor address. These lines provide communication with the controller device's internal registers and the buffer memory.<br>When configured in the Non-Multiplexed Microprocessors mode, these lines are bidirectional data lines. |
| MA(7:0) | I/O | MICROPROCESSOR ADDRESS BUS: This 8-bit output bus is the AD(7:0) bus latched by the ALE pin during the low order address phase of an Multiplexed Microprocessors type microprocessor cycle. These signals are nonmultiplexed address input when used with a non-multiplexed bus microprocessor — Non-Multiplexed Microprocessors interface. |
| READY/$\overline{AINT}$ | O | READY: When this signal is deasserted low, the microprocessor inserts wait states to allow time for the chip to respond to the access. Wait states are programmed by Buffer Mode Control Register — 53H: bits 7-6. |
| | O, OD, Z | $\overline{AINT}$: AT BUS INTERRUPT. An active low signal indicates the controller is requesting microprocessor service from the AT host bus side. This signal is programmable for either a push-pull with an internal pull up resistor or open-drain output circuit. This signal powers up in the high-Z state. Disk Formatter Mode Control Register, 4FH: bit 3 set high, programs this pin as a push-pull, and when set low programs it as an open drain output signal. |

**BUFFER MANAGER INTERFACE**

| | | |
|---|---|---|
| BA(15:0) | O | BUFFER MEMORY ADDRESS LINES 15 through 0. These sixteen outputs provide address lines for the dynamic memory or static memory chips used to implement the buffer memory. |
| BA16/$\overline{RAS}$ | O | BUFFER MEMORY ADDRESS 16: In SRAM mode, this pin generates the address: A16 for direct connection to a Static RAM address line 16.<br>BUFFER ROW ADDRESS STROBE: This active low output signal is generated to strobe the row — high order — address into the dynamic RAMs. It is intended to be directly tied to the RAMs input control pin. |
| BA17/$\overline{CAS}$ | O | BUFFER MEMORY ADDRESS 17: In SRAM mode, this pin generates the address: A17 for direct connection to a Static RAM address line 17.<br>COLUMN ADDRESS STROBE: This output signal is generated to strobe the column — low order address — into the dynamic RAM devices. |
| BD(7:0) | I/O | BUFFER MEMORY DATA BUS. 7 through 0. The bidirectional Data Bus connects directly to the buffer memory. This bus is designed for high speed data transfer. |

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## PIN DESCRIPTION (continued)

### BUFFER MANAGER INTERFACE (continued)

| | | |
|---|---|---|
| $\overline{MOE}$ | O | MEMORY OUTPUT ENABLE. This active low output controls the enabling of data onto the data bus by the dynamic RAMs or to indicate when every buffer memory access is active in SRAM mode. |
| $\overline{WE}$ | O | WRITE ENABLE. This active low output signal is used to strobe the data into the RAMs from the Data bus. For both buffer memory applications, this line is tied directly to the SRAM or DRAM control pin. |
| SYSCLK | I | SYSTEM CLOCK. This signal is used to synchronize the buffer RAM access, including the generation of memory address lines, write enable WE, and memory output enable MOE. In power down mode, this signal is shut off from the internal logic and hence buffer memory access is inhibited. |
| $\overline{MS}$ | O | Memory selected, asserted active low. |

## ELECTRICAL SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS

Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC operating characteristics.

| PARAMETER | RATING |
|---|---|
| Power Supply Voltage, VCC | 7V |
| Ambient Temperature | 0 to 70°C |
| Storage Temperature | -65 to 150°C |
| Power Dissipation | 750 mW |
| Input, Output pins | -0.5 to VCC+0.5V |

### ELECTRICAL CHARACTERISTICS

| PARAMETER | CONDITIONS | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| VCC Power Supply Voltage | | 3V | 3.0 | | 3.6 | V |
| | | 5V | 4.5 | | 5.5 | V |
| ICC Supply Current | | 3V | | | 30 | mA |
| | | 5V | | | 50 | mA |
| ICCS Standby Current | Note 1 | | | | 250 | µA |
| VIL Input Low Voltage | Except $\overline{RST}$ pin | | -0.5 | | 0.8 | V |
| VIH Input High Voltage | Except $\overline{RST}$ pin | | 2.0 | | VCC+0.5 | V |
| VIL Input Low Voltage | $\overline{RST}$ pin | 3V | -0.5 | | 0.8 | V |
| | $\overline{RST}$ pin | 5V | -0.5 | | 1.7 | V |
| VIH Input High Voltage | $\overline{RST}$ pin | 3V | 2.0 | | VCC+0.5 | V |
| | $\overline{RST}$ pin | 5V | 2.5 | | VCC+0.5 | V |

**ELECTRICAL CHARACTERISTICS** (continued)

| PARAMETER | CONDITIONS | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| VOL Output Low Voltage | Note 2 | | | | 0.4 | V |
| VOL Output Low Voltage | Note 3 | | | | 0.4 | V |
| VOH Output High Voltage IOH = -400 µA | | 3V | 2.15 | | | V |
| | | 5V | 2.4 | | | V |
| IL Input Leakage Current 0 < VIN < VCC | | | -10 | | 10 | µA |
| CIN Input Capacitance | | | | | 10 | pF |
| COUT Output Capacitance | | | | | 10 | pF |

Note: (1) Synchronization and Clock Control Register, 7FH: bits 3 and 4 set. RRCLK and SYSCLK internally inhibited.

(2) All interface pins except Host Interface pins. IOL= 2 mA.

(3) Host Interface pins, IOL=24 mA.

**MICROPROCESSOR INTERFACE TIMING PARAMETERS**

**Multiplexed Bus Interface Timings (Figures 2, 3, 4, 5)**

| | | | | | | |
|---|---|---|---|---|---|---|
| Ta | ALE Width | | 20 | | | ns |
| Tma | Address valid to MA (7:0) valid | 3V | | | 45 | ns |
| | | 5V | | | 30 | ns |
| Tr | $\overline{RD}$ Width | | 80 | | | ns |
| As | Address valid to ALE ↓ | | 5 | | | ns |
| Ah | ALE ↓ to address invalid | | 10 | | | ns |
| Cs | CS valid to $\overline{RD}$ ↓ or DS ↑ | | 20 | | | ns |
| Ch | $\overline{RD}$ ↑ or DS ↓ to CS ↓ | | 0 | | | ns |
| Tda | $\overline{RD}$ ↓ or DS ↑ to read data valid | 3V | | | 80 | ns |
| | | 5V | | | 60 | ns |
| Tds | DS width | | 80 | | | ns |
| Tdh | RD ↑ to or DS ↓ read data invalid | | 0 | | 25 | ns |
| Tsrw | R/$\overline{W}$ valid to DS ↑ | | 20 | | | ns |
| Thrw | DS ↓ to R/W invalid | | 20 | | | ns |
| Tdrdy | $\overline{RD}$ ↓ to READY ↓ (Intel) or | 3V | | | 45 | ns |
| | DS ↑ to READY ↓ (Motorola) | 5V | | | 30 | ns |
| Wds | Write data valid to $\overline{WR}$ ↑ or DS ↓ | | 40 | | | ns |
| Wdh | $\overline{WR}$ ↑ or DS ↓ to write data invalid | | 10 | | | ns |

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## ELECTRICAL SPECIFICATIONS (continued)

**Non-Multiplexed Bus Interface Timings (Figure 6)**

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| Tmas | MA (7:0) valid to DS ↓ | | 5 | | | ns |
| Tmah | DS ↑ to MA (7:0) invalid | | 5 | | | ns |
| Cs | CS valid to DS ↓ | | 20 | | | ns |
| Ch | DS ↑ to CS ↓ | | 0 | | | ns |
| Tda | DS ↑ to read data valid | 3V | | | 80 | ns |
| | | 5V | | | 60 | ns |
| Tds | DS width | | 80 | | | ns |
| Tdh | DS ↑ to read data invalid | | 0 | | 25 | ns |
| Tsrw | $\overline{R/W}$ valid to DS ↓ | | 20 | | | ns |
| Thrw | DS ↑ to $\overline{R/W}$ invalid | | 20 | | | ns |
| Tdrdy | DS ↑ to READY ↓ (Motorola) | 3V | | | 45 | ns |
| | | 5V | | | 30 | ns |
| Wds | Write data valid to $\overline{WR}$ ↑ or DS ↓ | | 40 | | | ns |
| Wdh | $\overline{WR}$ ↑ or DS ↓ to write data invalid | | 10 | | | ns |

Note: (1) Loading capacitor = 30 pF
(2) ↑ indicates rising edge ↓ indicates falling edge

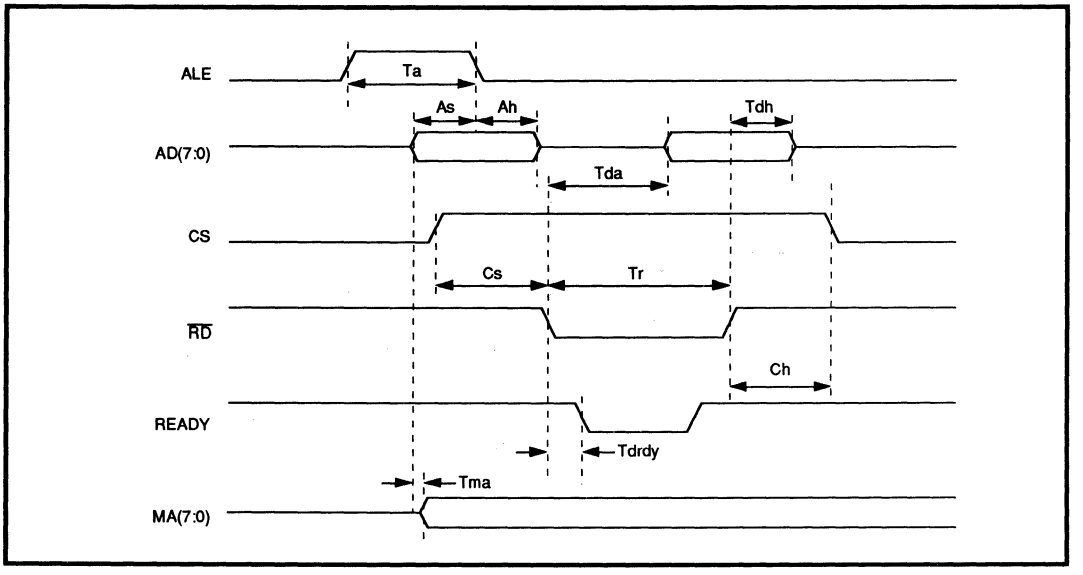


**FIGURE 2: Intel Register Multiplexed Read Timing**



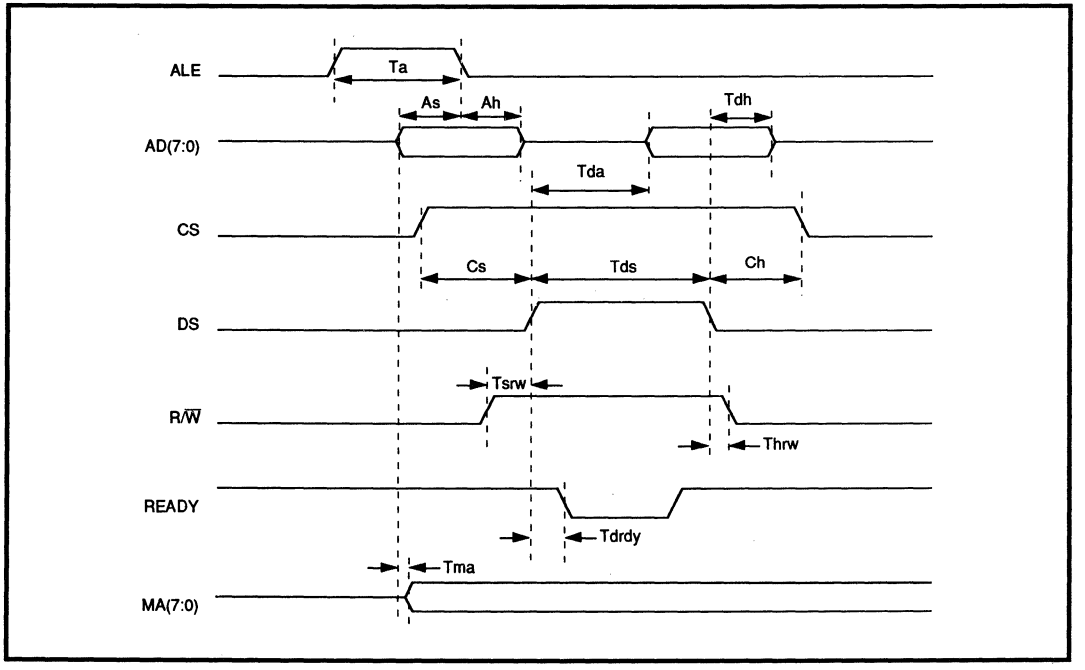


**FIGURE 3: Motorola Register Multiplexed Read Timing**

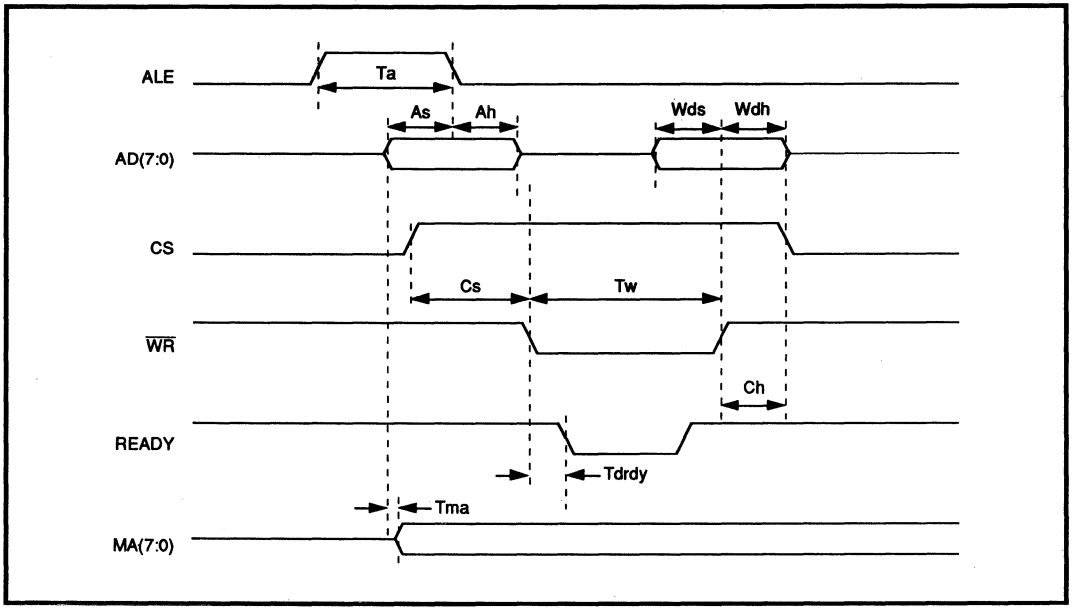


**FIGURE 4: Intel Register Multiplexed Write Timing**

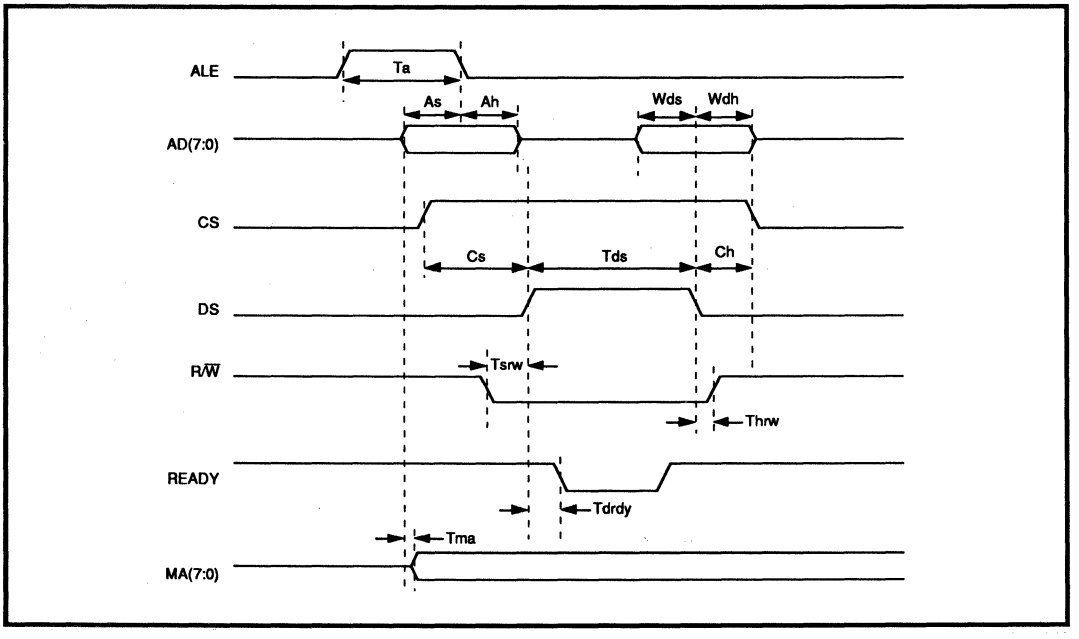


**FIGURE 5: Motorola Register Multiplexed Write Timing**

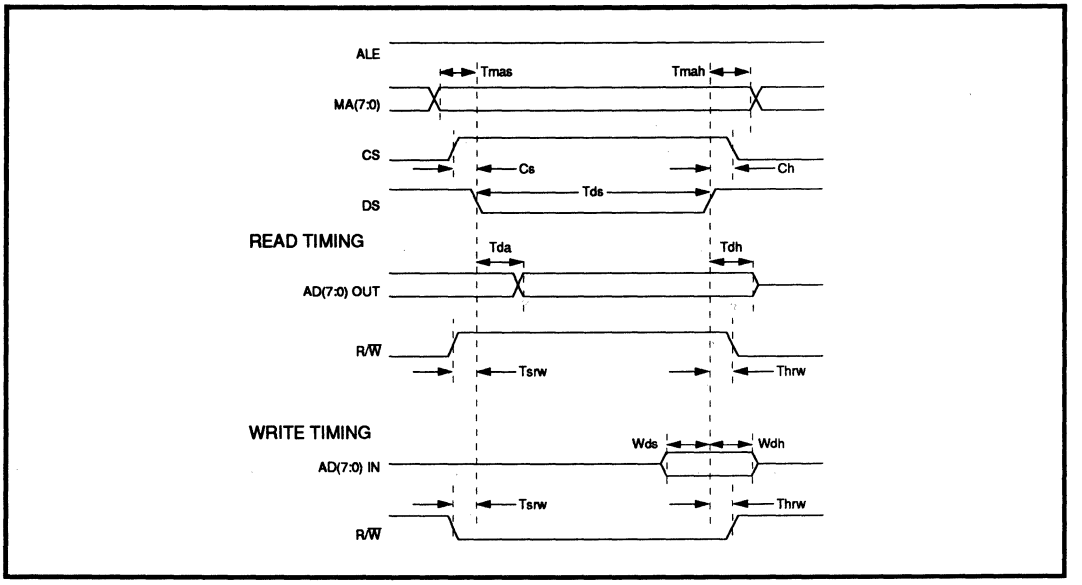


**FIGURE 6: Non-Multiplexed Bus Timing Diagrams**

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**Disk Read/Write Timing (Figures 7 and 8)**

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|---|
| T | RRCLK | 3V | 31 | | | ns |
| | | 5V | 20.8 | | | ns |
| T/2 | RRCLK high/low time | 3V | 12 | | | ns |
| | | 5V | 8.5 | | | ns |
| Tr = Tf | RRCLK rise and fall time | 3V | | | 3 | ns |
| | | 5V | | | 2 | ns |
| Ds | NRZ in valid to RRCLK ↑ | 3V | 5 | | | ns |
| | | 5V | 3 | | | ns |
| Dh | RRCLK ↑ to NRZ in invalid | 3V | 5 | | | ns |
| | | 5V | 3 | | | ns |
| As* | $\overline{AMD}$ valid to RRCLK ↑ | 3V | 5 | | | ns |
| | | 5V | 3 | | | ns |
| Dv | RRCLK ↑ to NRZ out | 3V | 5 | | 27 | ns |
| | | 5V | 3 | | 15 | ns |
| Wv* | RRCLK ↑ to $\overline{WAM}$ out | 3V | 5 | | 27 | ns |
| | | 5V | 3 | | 15 | ns |
| Note: | ↑ indicates rising edge ↓ indicates falling edge | | | | | |
| | * These specifications are only applicable in the Soft Sector mode. | | | | | |

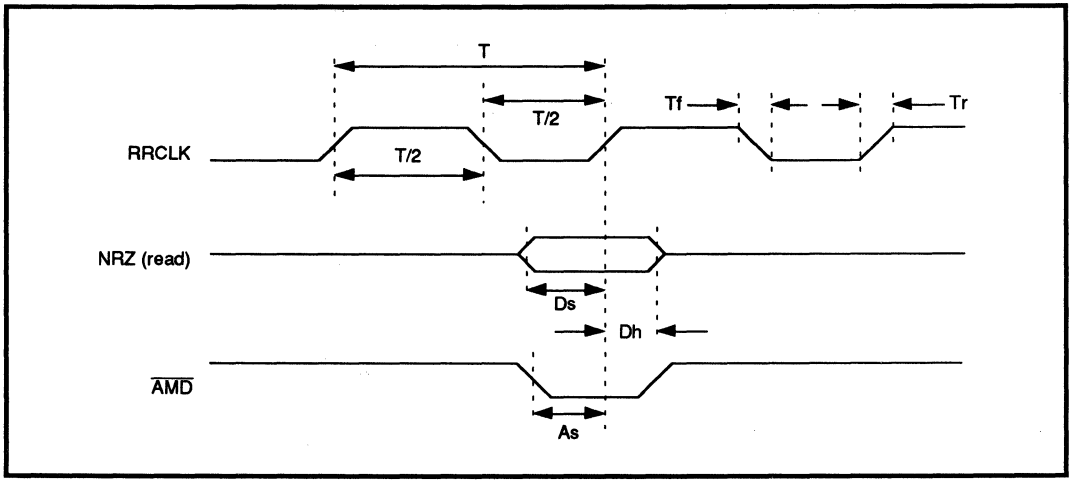



**FIGURE 7: Disk Read Timing**

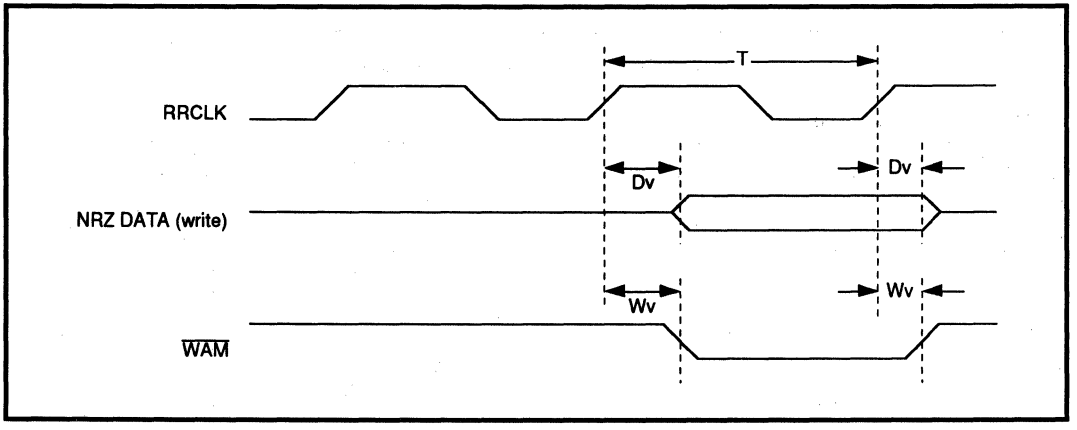



**FIGURE 8: Disk Write Timing**

## ELECTRICAL SPECIFICATIONS (continued)

### BUFFER MEMORY READ/WRITE TIMING PARAMETERS (Figures 9 through 12)

| PARAMETER | | MIN 5V | MAX 5V | MIN 3.3V | MAX 3.3V | UNIT |
|---|---|---|---|---|---|---|
| T | SYSCLK period | 25 | | 28 | | ns |
| T/2 | SYSCLK high/low time | 10 | | 12 | | ns |
| Tav | SYSCLK / to address valid (Note 1) | | 18 | | 35 | ns |
| Tmsv | SYSCLK / to $\overline{MS}$\ (Notes 1, 6) | | 18 | | 35 | ns |
| Tmsh | SYSCLK / to $\overline{MS}$/ (Note 1) | | 18 | | 35 | ns |
| Tmv | SYSCLK / to $\overline{MOE}$\ (Note 1) | | 18 | | 35 | ns |
| Tmh | SYSCLK / to $\overline{MOE}$/ (Note 1) | | 18 | | 35 | ns |
| Twv | SYSCLK / to $\overline{WE}$\ (Note 1) | | 18 | | 35 | ns |
| Twh | SYSCLK / to $\overline{WE}$/ (Note 1) | | 18 | | 35 | ns |
| Tdov | SYSCLK to data out valid (Note 1) | | 18 | | 35 | ns |
| Tdoh | SYSCLK to data out invalid (Note 1) | | 18 | | 35 | ns |
| Tdis | Data in valid to $\overline{MOE}$ / (SRAM)<br>Data in valid to $\overline{CAS}$ / (DRAM) | 5 | | 5 | | ns |
| Tdih | $\overline{MOE}$ / to data in valid (SRAM)<br>$\overline{CAS}$ / to data in valid (DRAM) | 0 | | 0 | | ns |
| Trv | SYSCLK / to $\overline{RAS}$\ (Note 1) | | 18 | | 35 | ns |
| Trh | SYSCLK / to $\overline{RAS}$/ (Note 1) | | 18 | | 35 | ns |
| Trav | SYSCLK to row address valid (Note 1) | | 18 | | 35 | ns |
| Trah | SYSCLK / to row address invalid (Note 1) | | 18 | | 35 | ns |
| Tcv | SYSCLK / to $\overline{CAS}$\ (Note 1) | | 18 | | 35 | ns |
| Tch | SYSCLK / to $\overline{CAS}$/ (Note 1) | | 18 | | 35 | ns |
| Tcav | SYSCLK / to column address valid (Note 1) | | 18 | | 35 | ns |
| Tcah | SYSCLK / to column address invalid | 0 | | 0 | | ns |

## ELECTRICAL SPECIFICATIONS (continued)

**BUFFER MEMORY READ/WRITE TIMING PARAMETERS (Figures 9 through 12)** (continued)

| PARAMETER | | CONDITIONS | MIN | UNIT |
|---|---|---|---|---|
| Trwl | $\overline{RAS}$\ to $\overline{RAS}$/ | Notes 2, 3 | (RWL + 3)•T-2 | ns |
| Trwh | $\overline{RAS}$/ to $\overline{RAS}$\ | Notes 2, 4 | (RWH + 1)•T-2 | ns |
| Tcwl | $\overline{CAS}$\ to $\overline{CAS}$/ | Note 2 | (CWL + 1)•T-2 | ns |
| Tcwl | $\overline{CAS}$/ to $\overline{CAS}$\ | Notes 2, 5 | (CWL + 1)•T-2 | ns |

Note: Loading capacitance = 30 pF

Note 1: The measured delay for any of the signal indicated by this note will not vary from the measured delay of any other signal indicated by this note by more than TBD (3V), ±1 ns (5V).

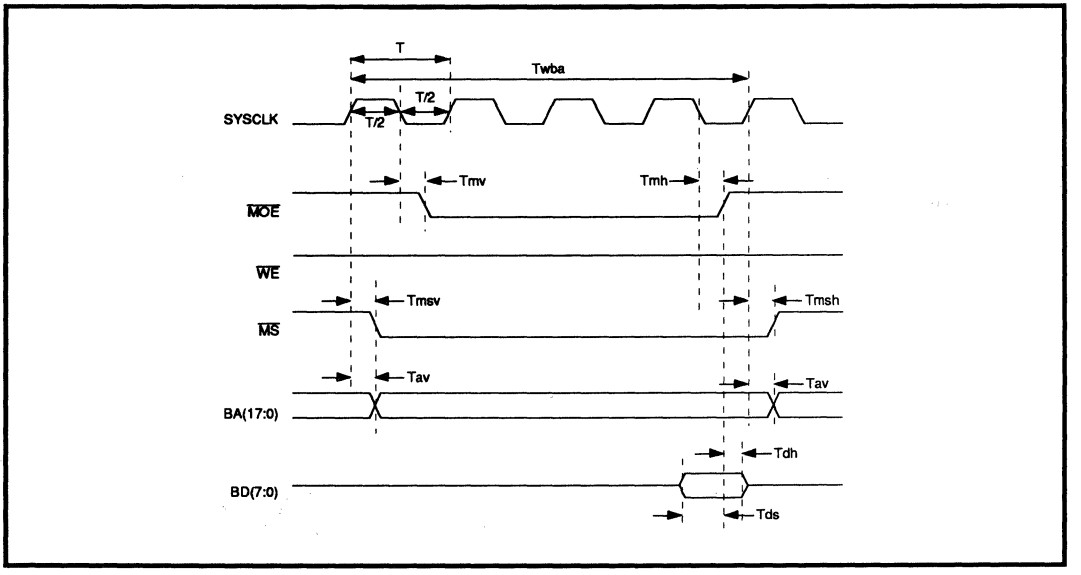
Note 2: RWL, RWH, CWL and CWH are fields in the Buffer Manager Timing Control Register (54H). Each is a two bit field which can contain a value of 0, 1, 2, or 3. These values determine the minimum number of SYSCLK periods (T) for the associated signal width.

Note 3: The minimum width value of Trwl will be generated for refresh cycles and for any buffer memory access cycle except when multiple page mode accesses are performed. When multiple page mode accesses are performed, the width of the $\overline{RAS}$ low pulse is extended until the end of the last $\overline{CAS}$ low cycle.

Note 4: The minumum value of Trwh will be generated whenever the Buffer Manager determines that a buffer request is pending at the completion of the current memory cycle and a page mode access can not be used either because page mode operation is not enabled or the needed location is not within the current page.

Note 5: The minumum value of Tcwh will be generated only between consecutive page mode accesses.

Note 6: $\overline{MS}$ will rise only if the Buffer Manager determines that no additional requests for buffer access are pending. If the Buffer Manager determines that another access is to be made, $\overline{MS}$ is kept low between the accesses for improved speed.




Note: Twba is a functional parameter that gives the duration of one RAM data buffer access cycle in SYSCLK periods. The value is programmed in bits 1-0 of register 54H. These examples show Twba = 4T.

**FIGURE 9: SRAM Read Timing**

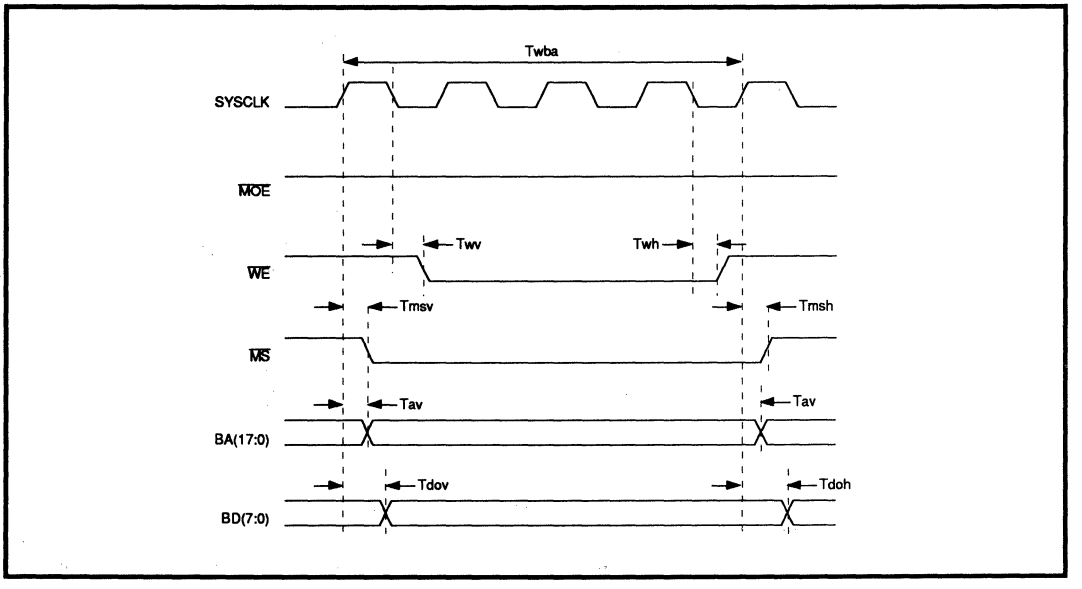



**FIGURE 10: SRAM Write Timing**

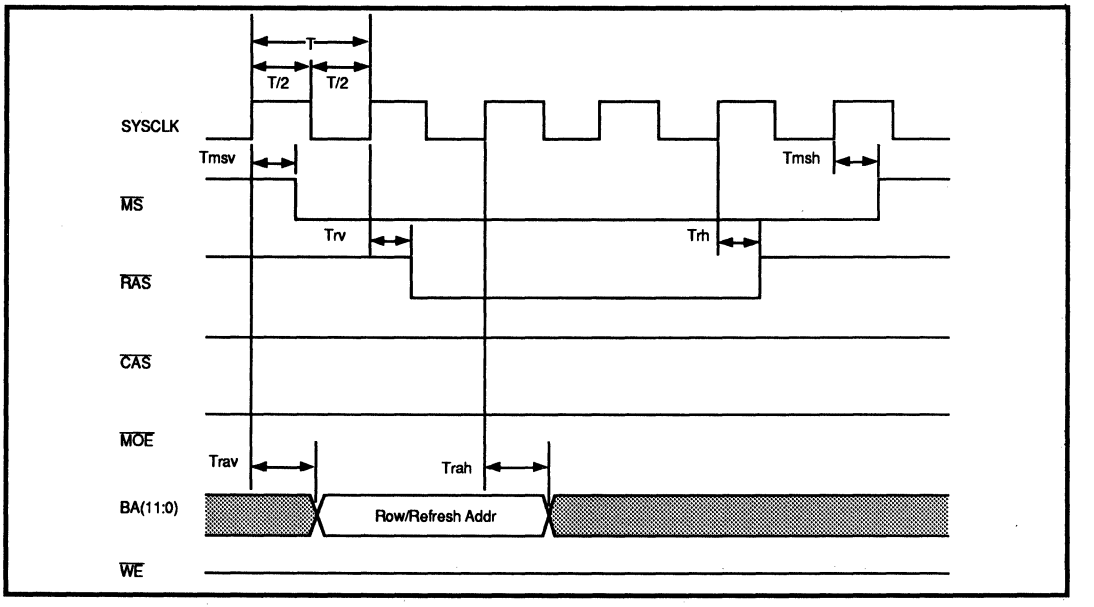



**FIGURE 11: DRAM Timing, Refresh Cycle (shown with WRL = 0)**

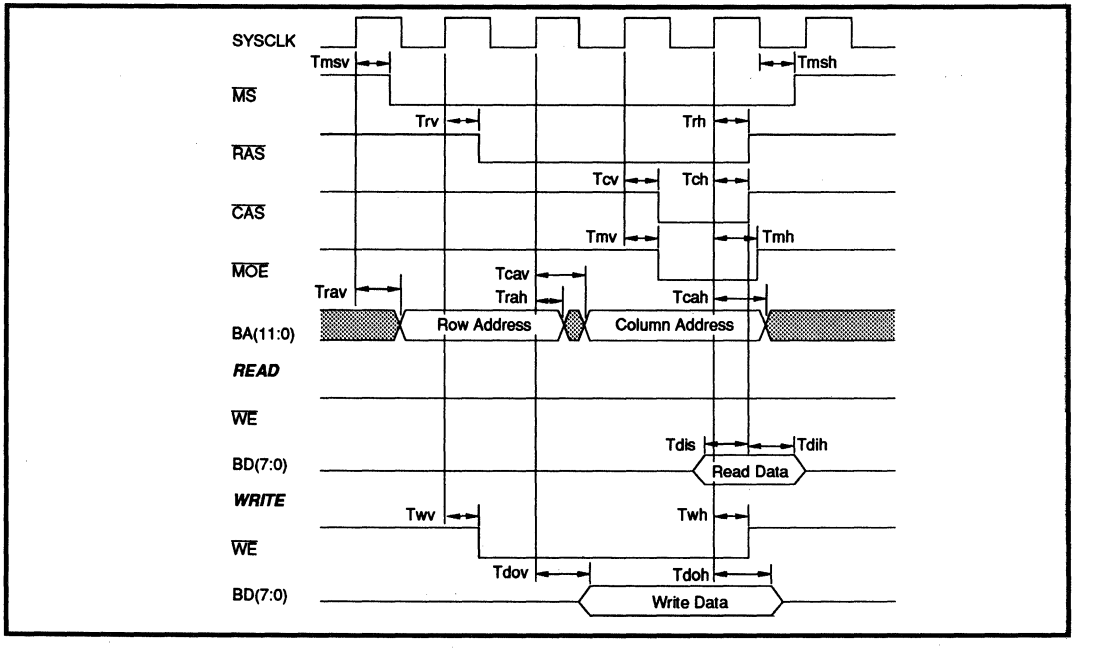



**FIGURE 12: DRAM Timing, Standard Cycle (shown with RWL = 0 and CWL = 0)**

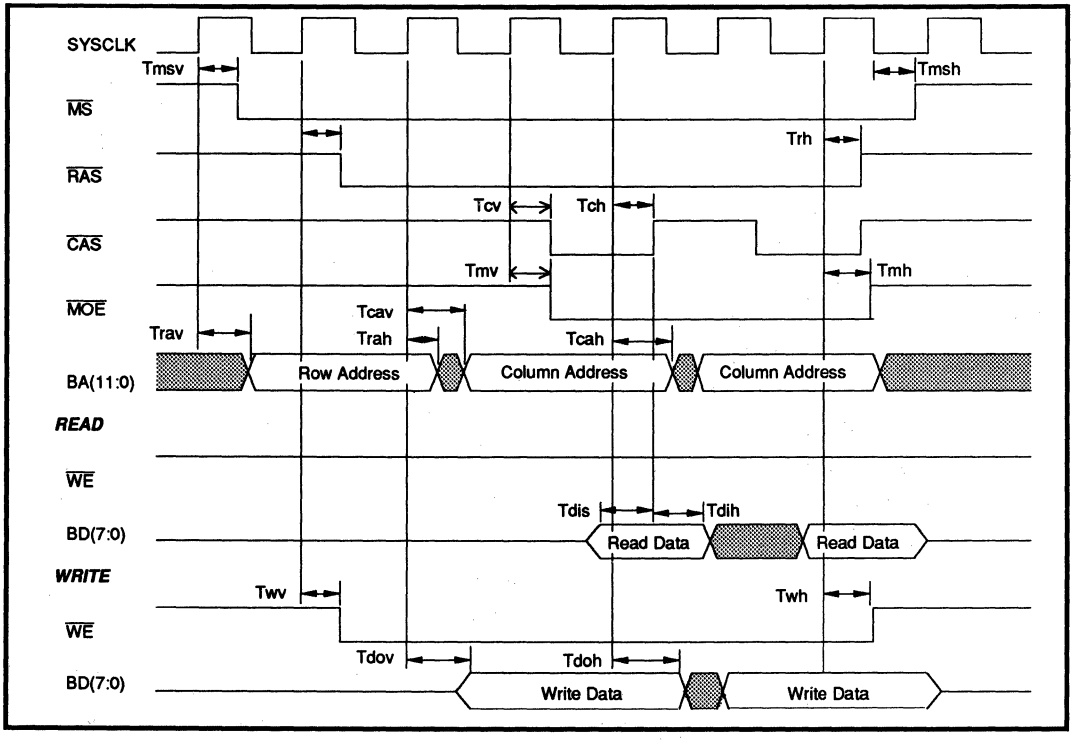



**FIGURE 13: DRAM Timing, Fast Page Cycles (shown with RWL = 0, RWH = 0, CWL = 0 and CWH = 0)**

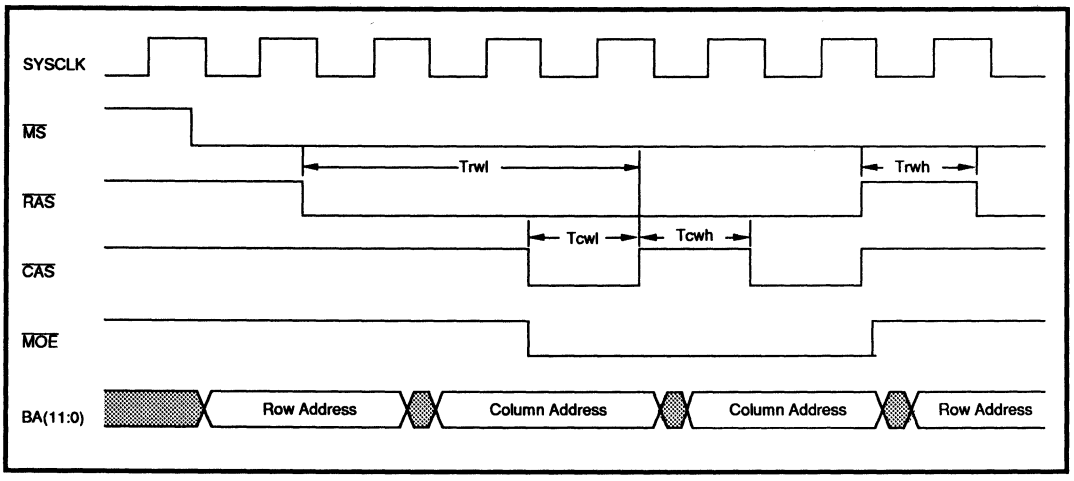



**FIGURE 14: DRAM Timing (showing the relationship of RWL, RWH, CWL and CWH to overall timing)**

## ELECTRICAL SPECIFICATIONS (continued)

### AT Host Interface Timing Parameters

| PARAMETER | | MIN 3.3V | MAX 3.3V | MIN 5V | MAX 5V | UNIT |
|---|---|---|---|---|---|---|
| DREQL | $\overline{DACK}$ ↓ to DREQ ↓ | | 50 | | 40 | ns |
| RDTA | $\overline{IOR}$ ↓ to HD(15:0) valid | | 70 | | 50 | ns |
| DMASET | $\overline{DACK}$ ↓ to $\overline{IOW}$ ↓ or $\overline{IOR}$ ↓ | 10 | | 10 | | ns |
| DMAHLD | $\overline{IOR}$ ↑ or $\overline{IOW}$ ↑ to $\overline{DACK}$ ↑ | 10 | | 10 | | ns |
| RDHLD | $\overline{IOR}$ ↑ to HD (15:0) hi-Z | 0 | 20 | 0 | 20 | ns |
| WDS | HD(15:0) setup to $\overline{IOW}$ ↑ | 40 | | 30 | | ns |
| WDHLD | HD(15:0) hold from $\overline{IOW}$ ↑ | 10 | | 10 | | ns |
| RWPULSE | $\overline{IOR}$ or $\overline{IOW}$ low pulse width | 80 | | 80 | | ns |
| RWH | $\overline{IOR}$ or $\overline{IOW}$ high pulse width | 50 | | 50 | | ns |
| CS16L | $\overline{HCS0}$ ↓, A(2:0) ↓, A9 ↓ or $\overline{HCS1}$ ↑ to $\overline{IOCS16}$ ↓ | | 30 | | 20 | ns |
| IOCHL | $\overline{IOR}$ or $\overline{IOW}$ ↓ to $\overline{IOCHRDY}$ ↓ | | 35 | | 25 | ns |
| ADRSET | $\overline{HCS0}$, A(2:0), A9/$\overline{HCS1}$ setup to $\overline{IOR}$ ↓ or $\overline{IOW}$ ↓ | 25 | | 25 | | ns |
| ADRHLD | $\overline{HCS0}$, A(2:0), A9/$\overline{HCS1}$ hold from $\overline{IOR}$ ↑ or $\overline{IOW}$ ↑ | 10 | | 0 | | ns |
| Note: Loading capacitance = 30 pF | | | | | | |

### Functional Specification

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| IOCHTW | $\overline{IOCHRDY}$ pulse width | | 0 | | 5xBCLK | ns |

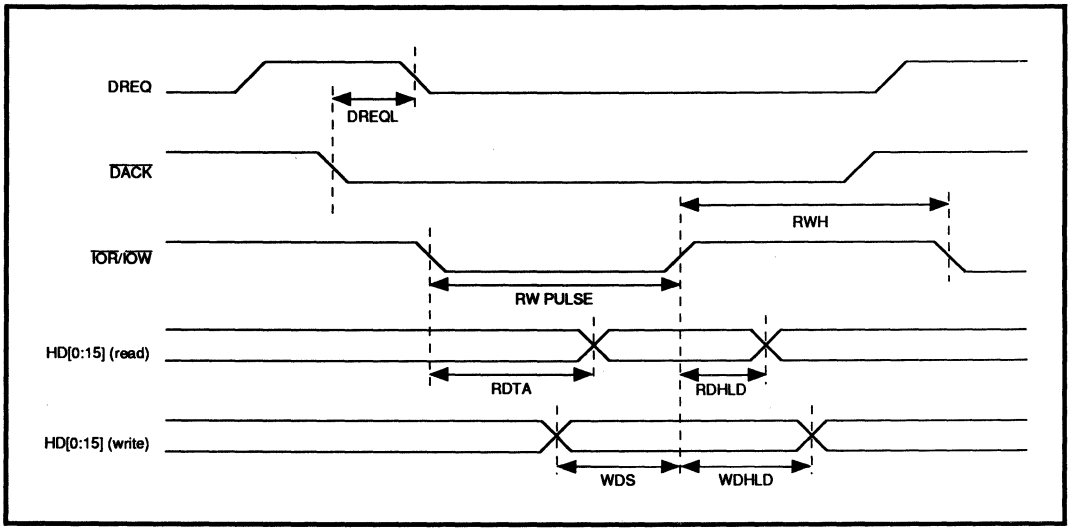



**FIGURE 15: Host Programmed I/O 8-16 Bit Timing**

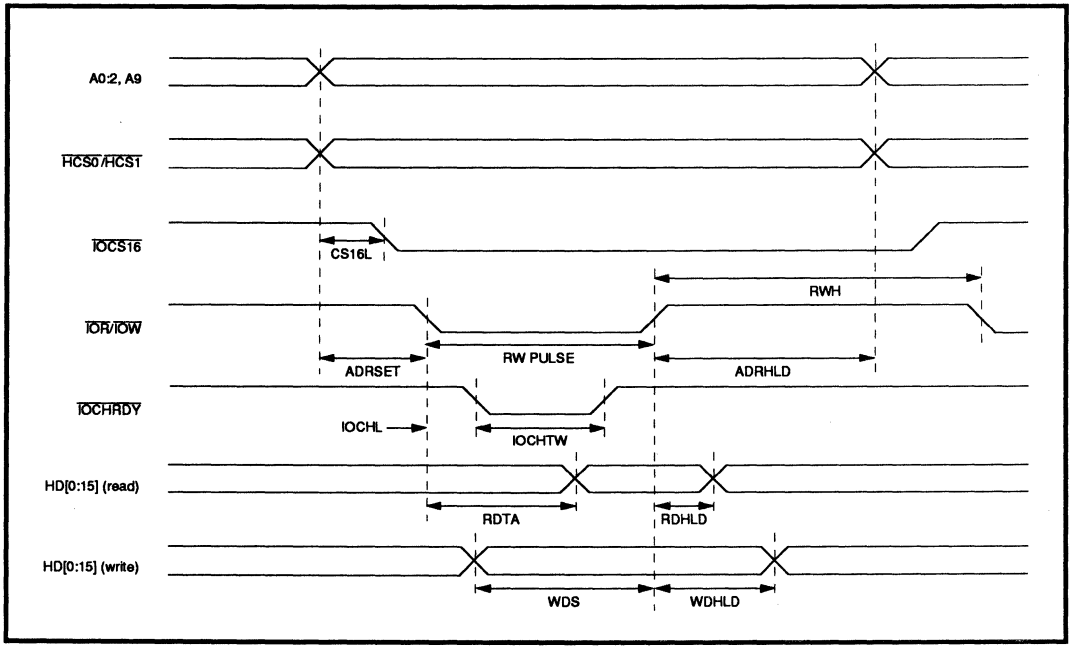



**FIGURE 16: Host DMA 8-16 Bit Interface Timing (Non-demand mode)**

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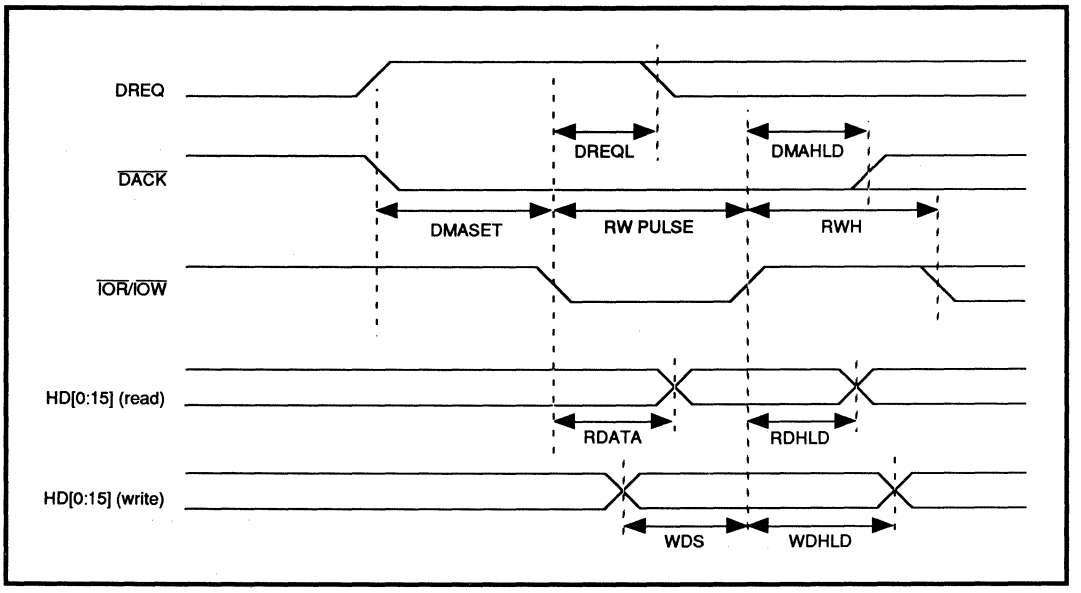



**FIGURE 17: Host DMA 8/16-Bit Interface Timing (Demand Mode)**

**RESET Assertion Timing Parameters (Figure 18)**

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| Trpwl | $\overline{RST}$ pulse width low | NOT Power On Reset | 500 | | | ns |
| | | Power On Reset | 7.5 | | | µs |

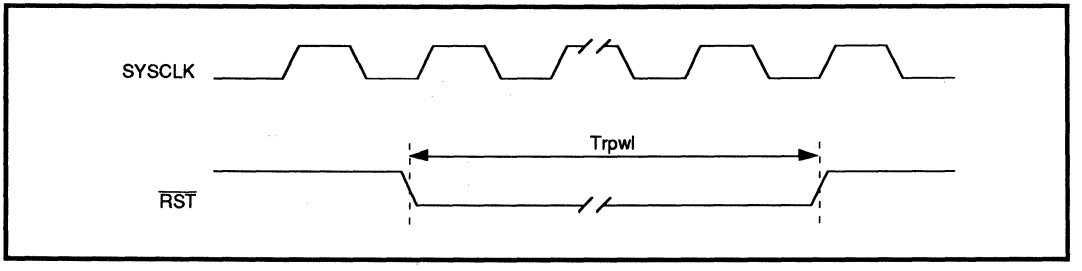
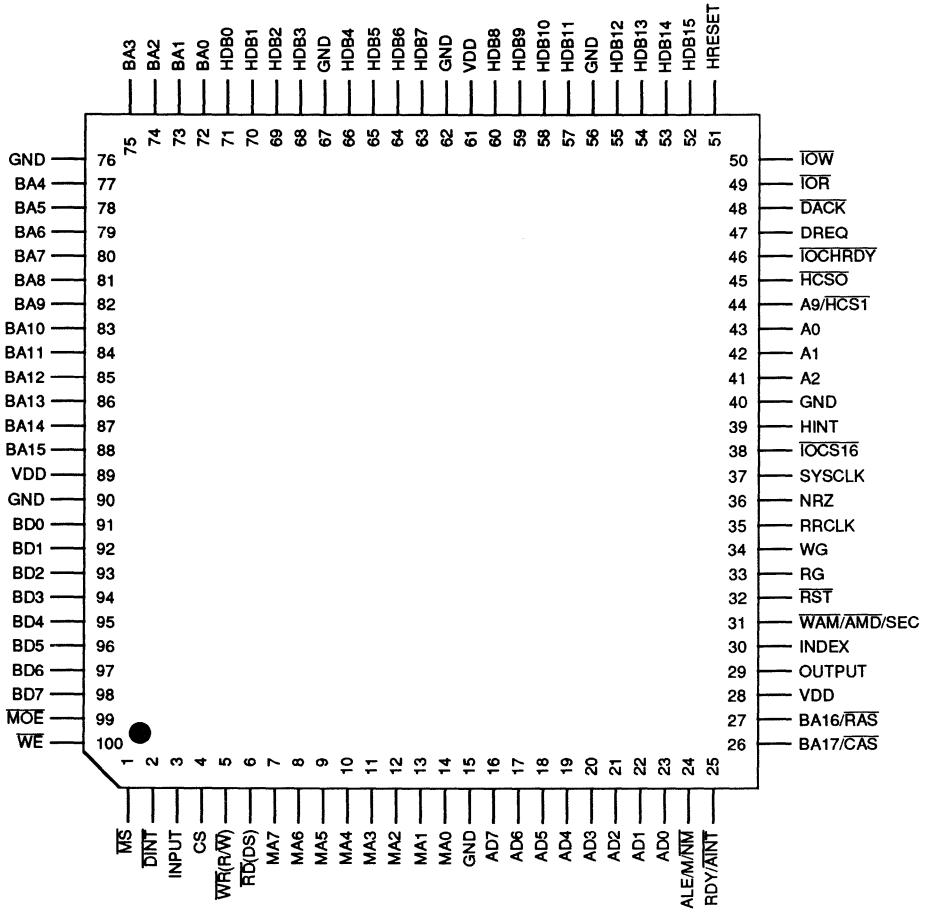



**FIGURE 18: RESET Assertion Timing**

## PACKAGE PIN DESIGNATIONS

(Top View)




**100-Lead TQFP**

8

**Advance Information:** Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.



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**Notes:**

silicon systems®
A TDK Group Company

# SSI 32C9302
## PC-AT Combo Controller With Reed Solomon, 3V Operation

**Advance Information**

January 1993

## DESCRIPTION

The SSI 32C9302 is an advanced CMOS VLSI device which integrates major portions of the hardware needed to build an ATA disk drive. The SSI 32C9302 can operate on 3.3 volts or 5 volts allowing use in 3.3 volt, 5 volt, or dual voltage disk drives. The 32C9302 has a dual bit NRZ interface to allow interfacing with channel IC's supporting this interface. The circuitry of the SSI 32C9302 includes a complete ATA interface, an advanced buffer manager, a high performance disk formatter and an 88 bit Reed-Solomon ECC with fast "on-the-fly" hardware correction. The SSI 32C9302 provides maximum performance while minimizing micro controller intervention.

When operating in a 3.3 volt environment, the SSI 32C9302 is capable of concurrent transfers of up to 32 megabits per second on the disk interface and 3

(continued)

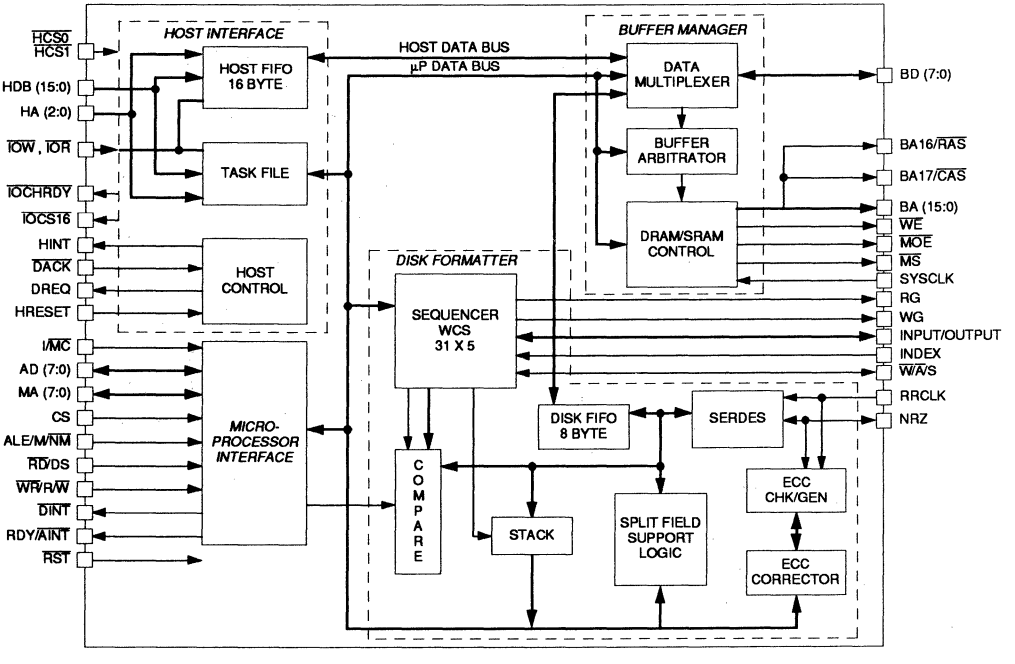
## FEATURES

- **ATA Interface**
  - **Single Chip PC AT Controller**
  - **Full ANSI ATA Compliance**
  - **Direct PC Bus connection with on board 16 mA (24 mA @5V) drivers**
  - **PC transfers to 3 (6 @5V) megawords per second**
  - **Supports PIO, DMA and EISA Class B Demand DMA**
  - **Logic for daisy chaining 2 drives**
  - **Automatic command decoding of write, write buffer and format commands**
  - **Automatic updates of the host task file registers in both Cyl/Hd/Sec and LBA modes**

(continued)

8

## BLOCK DIAGRAM



# SSI 32C9302
# PC-AT Combo Controller
# With Reed Solomon, 3V Operation

## DESCRIPTION (continued)

megawords (16 bit transfers) per second across the ATA bus. In a 5 volt environment, the SSI 32C9302 is capable of concurrent transfers of up to 48 megabits per second on the disk interface and 6 megawords per second across the ATA bus. In addition, on-the-fly error corrections and micro controller accesses to the buffer memory will not degrade the throughput during transfers.

The SSI 32C9302 is one of a family of Silicon Systems' single chip disk controllers which support a wide range of device interfaces. The 32C9301 is another 3.3/5 volt ATA controller, but supports a single NRZ disk formatter interface. The SSI 32C9001 is a 5 volt only version of the 32C9301 which is 100% firmware and pinout compatible. The SSI 32C9020, 32C9022 and 32C9023 family members are SCSI disk controllers providing many of the same features as the SSI 32C9302. The SSI 32C9340 and 32C9342 disk controllers complete the family providing PCMCIA/ ATA compliant interfaces. All members are based on a common architecture allowing major portions of firmware to be reused. The Silicon Systems' chip family is illustrated in the hierarchy chart shown in Figure 1.

The high level of integration within the SSI 32C9302 represents a major reduction in parts count. When the SSI 32C9302 ATA Controller is combined with the SSI 32R2300 Read/Write device, the SSI 32P4342 Pulse Detector with 1,7 ENDEC, the 32H6300 Servo and Motor Speed Controller, an appropriate micro controller and memory a complete, cost efficient, high performance intelligent drive solution is created.

## FEATURES (continued)

- **Hardware added to provide Multi-Sector data transfers without microprocessor intervention**
- **Automatic Host Interrupt and Busy for multiple sector transfers**
- **16 byte FIFO to improve performance**
- **Separate host interface VDD to allow 3.3 volt drives to plug into 5 volt systems**
- **Power Down I/O pins**

- **Buffer Manager**
  - **Direct support of DRAM or SRAM**
  - **SRAM: up to 256k bytes of memory with throughput to 10 (20 @5V) megabytes per second**
  - **DRAM: up to 1 megabyte of memory with throughput to 8 (17.78 @5V) megabytes per second**
  - **Programmable memory timing**
  - **Buffer RAM segmentation with flexible segment sizes from 256 bytes to 1 megabyte**
  - **Dedicated host, disk and microprocessor address pointers**
  - **Buffer Streaming with internal buffer protection circuit providing buffer integrity**
- **Disk Formatter**
  - **Dual Bit NRZ interface supporting data rates to 32 (48 @5V) megabits per second**
  - **Automatic multi-sector transfer**
  - **Header or microprocessor based split data field support**
  - **Advanced sequencer organized in 31 x 5 bytes**
  - **88-bit Reed Solomon ECC with "on-the-fly" fast hardware correction circuitry**
  - **Capable of correcting up to four 10-bit symbols in error**
  - **Guaranteed to correct one 31-bit burst or two 11-bit bursts**
  - **Hardware on-the-fly correction of either an 11- or 31-bit single burst error within a quarter sector time**
  - **Detects up to one 51-bit burst or three 11-bit bursts**
- **Microprocessor Interface**
  - **Supports both multiplexed or non-multiplexed microprocessors**
  - **Separate host and disk interrupts**
- **Other Features**
  - **Internal power down mode**
  - **Automatic power supply level detection**
  - **Conforms to JEDEC 3.3 volt specifications**
  - **TTL compatible input receivers at 3.3V or 5V**
  - **Available in 120-pin TQFP**

## FUNCTIONAL DESCRIPTION

Microprocessor Interface

ATA Interface

Disk Formatter

Buffer Manager

The Microprocessor Interface allows the local microprocessor access to all of the SSI 32C9302 internal control registers and any location within the buffer memory. The microprocessor, by writing and reading the internal registers, can control all activities of the SSI 32C9302. The microprocessor can elect to perform host and/or disk operations directly, or it can enable the advanced features of the SSI 32C9302 which can perform these operations automatically.

The ATA Interface block handles all PC AT bus activities. The ATA interface includes 12 mA (24 mA @ 5v) drivers allowing for direct connection of the SSI 32C9302 to the PC AT bus. The ATA interface block is highly automated, capable of performing multiple block transfers without micro controller involvement. The ATA block interfaces directly with the Buffer Manager via an internal speed matching FIFO. This FIFO, the bandwidth capabilities of the Buffer Manager, plus the advanced features of the ATA Interface guarantee sustained full speed transfers across the PC AT bus.

The Disk Formatter performs the serialization and deserialization of data. It provides all of the necessary functions to control track formatting, header search, and the reading and writing of data. The heart of the Disk Formatter is an advanced programmable sequencer. The sequencer can contain 31 instructions, each of which is 5 bytes (40 bits) in width. The width of the instructions allows for sophisticated branching techniques which increase the flexibility and power of the sequencer. The flexible disk interface can be configured through a wide range of capabilities. This allows the SSI 32C9302 to interface with nearly any read/write channel and allows the user of the SSI 32C9302 to select the read/write channel best suited to the device. Of course, by selecting the SSI 32C9302 controller and the SSI 32P4342 Read Channel with 1,7 ENDEC, you are guaranteed a problem free interface.

Within the Disk Formatter are the ECC generator/checker and ECC corrector. The generator/checker provides the ability to generate or check a 32 bit ECC for headers and an 88 bit Reed Solomon code for data. If the checker detects an error using the 88 bit Reed Solomon code, the syndrome information is transferred into the corrector. The corrector then performs the necessary operations to determine if the error was correctable and, if it was correctable, the corrector interfaces directly with the buffer controller and performs the correction automatically. The corrector performs its correction within one quarter of a sector. This guarantees that the corrector will always be available to correct the next sector if necessary.

As its name implies, the Buffer Manager manages the data buffer of the controller. The Buffer Manager can support either SRAM or DRAM. When configured to operate with DRAM, the Buffer Manager automatically performs necessary refresh cycles. The Buffer Manager creates all of the necessary timing and control signals for a wide range of memory types and

(continued)

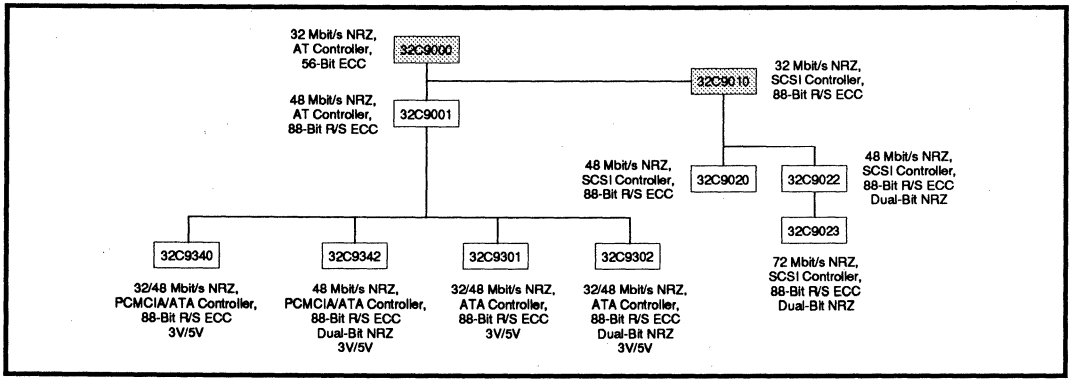



**FIGURE 1: Silicon Systems' Disk Controller Chip Hierarchy**

## FUNCTIONAL DESCRIPTION (continued)

speeds. Besides interfacing with the buffer memory, the Buffer Manager interfaces with the ATA Interface block, the Disk Formatter block, the ECC corrector and the microprocessor. If more than one of these devices requires access to the buffer memory, the Buffer Manager arbitrates the requests automatically. The Buffer Manager of the SSI 32C9302 can sustain ATA operations at the rate of 3 (6 @ 5v) megawords per second, Disk Formatter operations at 32 (48 @ 5v) megabits per second and still has sufficient band width left to handle on-the-fly ECC corrections and microprocessor accesses without degrading performance on any of the interfaces.

## PIN DESCRIPTION

The following convention is used in the pin description:

- (I) denotes an input
- (I/S) denotes a Schmitt trigger input
- (O) denotes an output
- (I/O) denotes a bidirectional signal
- (Z) denotes a tri-state output
- (OD) denotes an open drain output

Active low signals are denoted by a bar on top of the signal name and dual function pins are denoted with a slash between the two signals — A9/$\overline{\text{HCS1}}$.

**GENERAL**

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| VDD | | POWER SUPPLY PIN, VCC |
| GND | | GROUND |

**HOST INTERFACE**

| | | |
|---|---|---|
| A(2:0) | I | HOST ADDRESS LINES. The Host Address lines A(2:0) and A9 are used to access the various PC/AT control/status, and data registers. |
| A9/$\overline{\text{HCS1}}$ | I | HOST ADDRESS LINE 9/HOST CHIP SELECT 1. This is a multiplexed input pin. When Register 48H-bit 3 is reset this input is HOST ADDRESS LINE 9, when the bit is set this input is HOST CHIP SELECT 1. |
| $\overline{\text{HCS0}}$ | I | HOST CHIP SELECT 0. This pin selects access to the control, status and data registers. |
| $\overline{\text{IOCS16}}$ | OD | 16 BIT DATA TRANSFER. An open drain active low output that indicates that a 16-bit buffer transfer is active. |
| HINT | O | HOST INTERRUPT. Asserted active high to indicate to the Host that the controller needs attention. |

## PIN DESCRIPTION (continued)

### HOST INTERFACE (continued)

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| $\overline{\text{IOCHRDY}}$ | O,Z | I/O CHANNEL READY. Active low, this signal is asserted whenever the internal host FIFO is not ready to transfer data. |
| DREQ | O,Z | DMA REQUEST. The active high DMA Request signal is used during DMA transfer between the Host and the SSI 32C9301. |
| $\overline{\text{DACK}}$ | I | DMA ACKNOWLEDGE. This active low signal is used during DMA to complete the DMA handshake for data transfer between the host and the controller. |
| $\overline{\text{IOR}}$ | I | INPUT READ SELECT. This active low pin is asserted by the Host during a Host read operation. When asserted with $\overline{\text{HCS0}}$, $\overline{\text{HCS1}}$, or $\overline{\text{DACK}}$, data from the device is enabled onto the host data bus. |
| $\overline{\text{IOW}}$ | I | INPUT WRITE SELECT. Asserted active low by the HOST during a HOST write operation. When asserted with $\overline{\text{HCS0}}$, $\overline{\text{HCS1}}$, or $\overline{\text{DACK}}$, data from the host data bus is strobed into the device. |
| $\overline{\text{HRESET}}$ | I | HOST RESET. This active low signal stops all commands in progress and initializes the control/status registers — This signal can also "wake up" the device while it is in power down mode. |
| HDB(15:0) | I/O | HOST DATA BUS. These bits are used for word transfers between the Buffer Memory and the Host; bits (7:0) are used for status, commands, or ECC byte transfers. |
| $\overline{\text{DASP}}$ | O | DRIVE ACTIVE/DRIVE 1 PRESENT. This is a time-multiplexed signal which indicates that a drive is active, or that Drive 1 is present. |
| $\overline{\text{PDIAG}}$ | I/O | PASSED DIAGNOSTICS. This signal is an output for when configured as Drive 1 and an input when configured as Drive 0. |

### DISK INTERFACE

| | | |
|---|---|---|
| INDEX | I | INDEX. This input is a pulse that occurs once per revolution and defines the start of first sector. |
| OUTPUT | O | DISK SEQUENCER OUTPUT. This pin is controlled by bit 2 of the control field of the disk sequencer. |
| INPUT | I | INPUT. This signal is used to synchronize the disk sequencer to an external event. |
| $\overline{\text{AMD}}$/ SECTOR | I/O | SECTOR/ADDRESS MARK DETECT. This pin is configured to operate in Hard or Soft Sector mode by initializing the Disk Formatter Mode Control Register: 4FH, bit 1. In the hard sector mode it is used as the sector input — a pulse on this pin indicates a sector mark is found.<br>In the soft sector mode, an active low input indicates an address mark was detected. The device powers up in soft sector mode. |

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## PIN DESCRIPTION (continued)

### DISK INTERFACE (continued)

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| RG | O | READ GATE. This active high output enables the reading of the disk. It is asserted at the beginning of the PLO for header and data field by the sequencer — sequencer Control Field bits 5 and 6. It is automatically deasserted at the end of the CRC or ECC. |
| WG | O | WRITE GATE. This active high output enables writing onto the disk. It is asserted and deasserted by the sequencer Control Field bits 5 and 6. |
| RRCLK | I | READ/REFERENCE CLOCK. This pin is used in conjunction with the NRZ pin to clock data in and out of the SSI 32C9001 device. This input must be glitch-free to ensure correct operation of the chip. |
| WCLK | O | WRITECLOCK. This signal clocks the NRZ data out in the dual NRZ interface mode. |
| NRZ0, 1 | I/O | NON RETURN TO ZERO. These signals are the read data input 0 and 1 from the disk drive when the read gate signal is asserted; it is the write data output to the disk drive when the write gate signal is asserted. |

### MICROPROCESSOR INTERFACE

| | | |
|---|---|---|
| $\overline{RST}$ | I/S | RESET. An asserted active low input generates a component reset that holds the internal registers of the SSI 32C9301 at reset, stops all operations within the chip, and deasserts all output signals. All input/output signals and Host outputs are set to the high-Z state. |
| ALE/M/$\overline{NM}$ | I | ADDRESS LATCH ENABLE/MULTIPLEXED/NON-MULTIPLEXED ADDRESS SELECT. When tied high or left floating after reset, the microprocessor interface is configured as non-multiplexed. When driven low, then the microprocessor interface is configured as multiplexed. In this case this pin functions as the address latch enable, and the MA(7:0) pins are the demultiplexed address outputs. |
| CS | I | CHIP SELECT. This signal must be asserted high for all microprocessor accesses to the registers of this chip. |

## PIN DESCRIPTION (continued)

### MICROPROCESSOR INTERFACE (continued)

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| $\overline{WR}$/R/$\overline{W}$ | I | WRITE STROBE/READ/WRITE. In the Multiplexed Microprocessors bus mode, when an active low signal is present with CS signal asserted high, the data on the AD0:7 is written to the internal registers.<br><br>In the Non-Multiplexed Microprocessors bus mode, this signal acts as the R$\overline{W}$ signal. A high on this input along with the $\overline{RD}$/DS signal high and the CS signal asserted high indicates a read operation. A low on this input along with the $\overline{RD}$/DS signal asserted and the CS signal asserted high indicates a write operation. See table below.<br><br>I/MC CS WR/R/W RD/DS Action Mux/Non-Mux<br>High High Low High Write to internal registers. M<br>High High High Low Read from internal registers. M<br>Low High Low High Write to internal registers. N<br>Low High High High Read from internal registers. N<br>X Low X X No action. M or N<br><br>Note: X denotes don't care. |
| $\overline{RD}$/DS | I | READ STROBE/DATA STROBE. In the Multiplexed Microprocessors bus mode, when an active low signal is present with CS signal high, internal registers will be accessed.<br><br>In the Non-Multiplexed Microprocessors mode, this signal acts as the DS signal. A high on the DS, R/$\overline{W}$, and the CS signals, indicates a read operation. A low on the R/$\overline{W}$ signal, highs on both the DS and the CS, indicates a write operation to the internal registers. |
| $\overline{DINT}$ | O, OD, Z | INTERRUPT. An active low signal indicates the controller is requesting microprocessor service from the disk side. This signal is programmable for either a push-pull with an internal pull up resistor or open-drain output circuit. This signal powers up in the high-Z state. Disk Formatter Mode Control Register, 4FH: bit 3 set high, programs this pin as a push-pull, and when set low programs it as an open drain output signal. |
| AD(7:0) | I/O | ADDRESS/DATA BUS. When configured in the Multiplexed Microprocessors mode, these lines are multiplexed, bidirectional data path to the microprocessor. During the beginning of the memory cycle the bus captures the low order byte of the microprocessor address. These lines provide communication with the controller device's internal registers and the buffer memory.<br><br>When configured in the Non-Multiplexed Microprocessors mode, these lines are bidirectional data lines. |
| MA(7:0) | I/O | MICROPROCESSOR ADDRESS BUS: This 8-bit output bus is the AD(7:0) bus latched by the ALE pin during the low order address phase of an Multiplexed Microprocessors type microprocessor cycle. These signals are nonmultiplexed address input when used with a non-multiplexed bus microprocessor — Non-Multiplexed Microprocessors interface. |

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## PIN DESCRIPTION (continued)

### MICROPROCESSOR INTERFACE (continued)

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| READY/$\overline{AINT}$ | O | READY: When this signal is deasserted low, the microprocessor inserts wait states to allow time for the chip to respond to the access. Wait states are programmed by Buffer Mode Control Register — 53H: bits 7-6. |
| | O, OD, Z | $\overline{AINT}$: AT BUS INTERRUPT. An active low signal indicates the controller is requesting microprocessor service from the AT host bus side. This signal is programmable for either a push-pull with an internal pull up resistor or open-drain output circuit. This signal powers up in the high-Z state. Disk Formatter Mode Control Register, 4FH: bit 3 set high, programs this pin as a push-pull, and when set low programs it as an open drain output signal. |

### BUFFER MANAGER INTERFACE

| | | |
|---|---|---|
| BA(15:0) | O | BUFFER MEMORY ADDRESS LINES 15 through 0. These sixteen outputs provide address lines for the dynamic memory or static memory chips used to implement the buffer memory. |
| BA16/$\overline{RAS}$ | O | BUFFER MEMORY ADDRESS 16: In SRAM mode, this pin generates the address: A16 for direct connection to a Static RAM address line 16. |
| | | BUFFER ROW ADDRESS STROBE: This active low output signal is generated to strobe the row — high order — address into the dynamic RAMs. It is intended to be directly tied to the RAMs input control pin. |
| BA17/$\overline{CAS}$ | O | BUFFER MEMORY ADDRESS 17: In SRAM mode, this pin generates the address: A17 for direct connection to a Static RAM address line 17.<br>COLUMN ADDRESS STROBE: This output signal is generated to strobe the column — low order address — into the dynamic RAM devices. |
| BD(7:0) | I/O | BUFFER MEMORY DATA BUS. 7 through 0. The bidirectional Data Bus connects directly to the buffer memory. This bus is designed for high speed data transfer. |
| $\overline{MOE}$ | O | MEMORY OUTPUT ENABLE. This active low output controls the enabling of data onto the data bus by the dynamic RAMs or to indicate when every buffer memory access is active in SRAM mode. |
| $\overline{WE}$ | O | WRITE ENABLE. This active low output signal is used to strobe the data into the RAMs from the Data bus. For both buffer memory applications, this line is tied directly to the SRAM or DRAM control pin. |
| SYSCLK | I | SYSTEM CLOCK. This signal is used to synchronize the buffer RAM access, including the generation of memory address lines, write enable WE, and memory output enable MOE. In power down mode, this signal is shut off from the internal logic and hence buffer memory access is inhibited. |
| $\overline{MS}$ | O | Memory selected, asserted active low. |

## ELECTRICAL SPECIFICATIONS

### ABSOLUTE MAXIMUM RATINGS

Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC operating characteristics.

| PARAMETER | RATING |
|---|---|
| Power Supply Voltage, VCC | 7V |
| Ambient Temperature | 0 to 70°C |
| Storage Temperature | -65 to 150°C |
| Power Dissipation | 750 mW |
| Input, Output pins | -0.5 to VCC+0.5V |

### ELECTRICAL CHARACTERISTICS

| PARAMETER | CONDITIONS | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| VCC Power Supply Voltage | | 3V | 3.0 | | 3.6 | V |
| | | 5V | 4.5 | | 5.5 | V |
| ICC Supply Current | | 3V | | | 30 | mA |
| | | 5V | | | 50 | mA |
| ICCS Standby Current | Note 1 | | | | 250 | µA |
| VIL Input Low Voltage | Except $\overline{RST}$ pin | | -0.5 | | 0.8 | V |
| VIH Input High Voltage | Except $\overline{RST}$ pin | | 2.0 | | VCC+0.5 | V |
| VIL Input Low Voltage | $\overline{RST}$ pin | 3V | -0.5 | | 0.8 | V |
| | $\overline{RST}$ pin | 5V | -0.5 | | 1.7 | V |
| VIH Input High Voltage | $\overline{RST}$ pin | 3V | 2.0 | | VCC+0.5 | V |
| | $\overline{RST}$ pin | 5V | 2.5 | | VCC+0.5 | V |
| VOL Output Low Voltage | Note 2 | | | | 0.4 | V |
| VOL Output Low Voltage | Note 3 | | | | 0.5 | V |
| VOH Output High Voltage IOH = -400 µA | | 3V | 2.15 | | | V |
| IL Input Leakage Current 0 < VIN < VCC | | | -10 | | 10 | µA |
| CIN Input Capacitance | | | | | 10 | pF |
| COUT Output Capacitance | | | | | 10 | pF |

Note: (1) Synchronization and Clock Control Register, 7FH: bits 3 and 4 set. RRCLK and SYSCLK internally inhibited.

(2) All interface pins except Host Interface pins. IOL= 2 mA.

(3) Host Interface pins, IOL=24 mA.

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## MICROPROCESSOR INTERFACE TIMING PARAMETERS

### Multiplexed Bus Interface Timings (Figures 2, 3, 4, 5)

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| Ta | ALE Width | | 20 | | | ns |
| Tma | Address valid to MA (7:0) valid | 3V | | | 45 | ns |
| | | 5V | | | 30 | ns |
| Tr | $\overline{RD}$ Width | | 80 | | | ns |
| As | Address valid to ALE ↓ | | 5 | | | ns |
| Ah | ALE ↓ to address invalid | | 10 | | | ns |
| Cs | CS valid to $\overline{RD}$ ↓ or DS ↑ | | 20 | | | ns |
| Ch | $\overline{RD}$ ↑ or DS ↓ to CS ↓ | | 0 | | | ns |
| Tda | $\overline{RD}$ ↓ or DS ↑ to read data valid | 3V | | | 80 | ns |
| | | 5V | | | 60 | ns |
| Tds | DS width | | 80 | | | ns |
| Tdh | RD ↑ to or DS ↓ read data invalid | | 0 | | 25 | ns |
| Tsrw | R/$\overline{W}$ valid to DS ↑ | | 20 | | | ns |
| Thrw | DS ↓ to R/W invalid | | 20 | | | ns |
| Tdrdy | $\overline{RD}$ ↓ to READY ↓ (Intel) or | 3V | | | 45 | ns |
| | DS ↑ to READY ↓ (Motorola) | 5V | | | 30 | ns |
| Wds | Write data valid to $\overline{WR}$ ↑ or DS ↓ | | 40 | | | ns |
| Wdh | $\overline{WR}$ ↑ or DS ↓ to write data invalid | | 10 | | | ns |

### Non-Multiplexed Bus Interface Timings (Figure 6)

| | | | | | | |
|---|---|---|---|---|---|---|
| Tmas | MA (7:0) valid to DS ↓ | | 5 | | | ns |
| Tmah | DS ↑ to MA (7:0) invalid | | 5 | | | ns |
| Cs | CS valid to DS ↓ | | 20 | | | ns |
| Ch | DS ↑ to CS ↓ | | 0 | | | ns |
| Tda | DS ↑ to read data valid | 3V | | | 80 | ns |
| | | 5V | | | 60 | ns |
| Tds | DS width | | 80 | | | ns |
| Tdh | DS ↑ to read data invalid | | 0 | | 25 | ns |
| Tsrw | $\overline{R/W}$ valid to DS ↓ | | 20 | | | ns |
| Thrw | DS ↑ to $\overline{R/W}$ invalid | | 20 | | | ns |
| Tdrdy | DS ↑ to READY ↓ (Motorola) | 3V | | | 45 | ns |
| | | 5V | | | 30 | ns |
| Wds | Write data valid to $\overline{WR}$ ↑ or DS ↓ | | 40 | | | ns |
| Wdh | $\overline{WR}$ ↑ or DS ↓ to write data invalid | | 10 | | | ns |

Note: (1) Loading capacitor = 30 pF
(2) ↑ indicates rising edge ↓ indicates falling edge

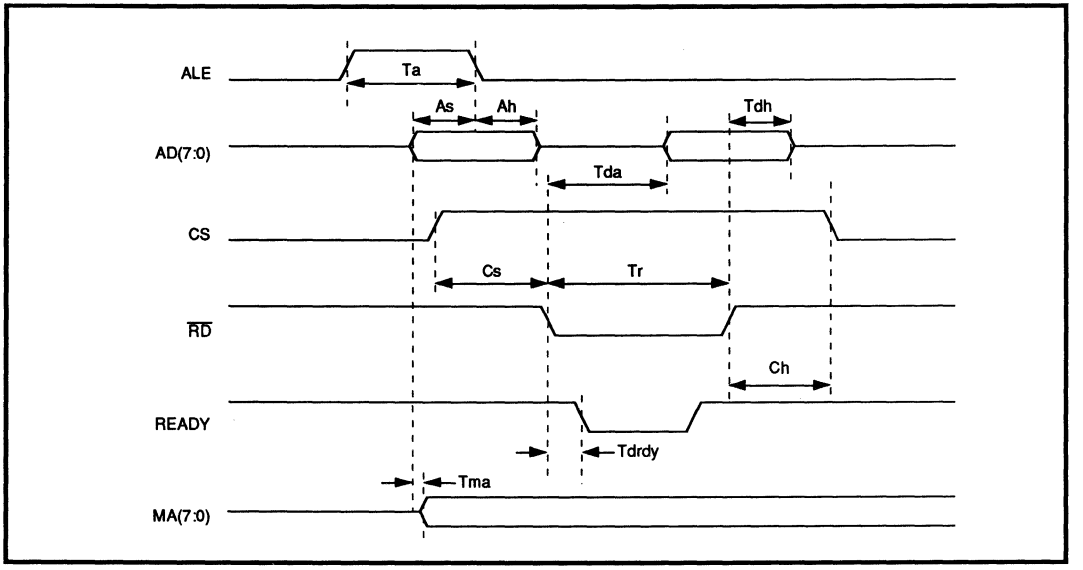



**FIGURE 2: Intel Register Multiplexed Read Timing**



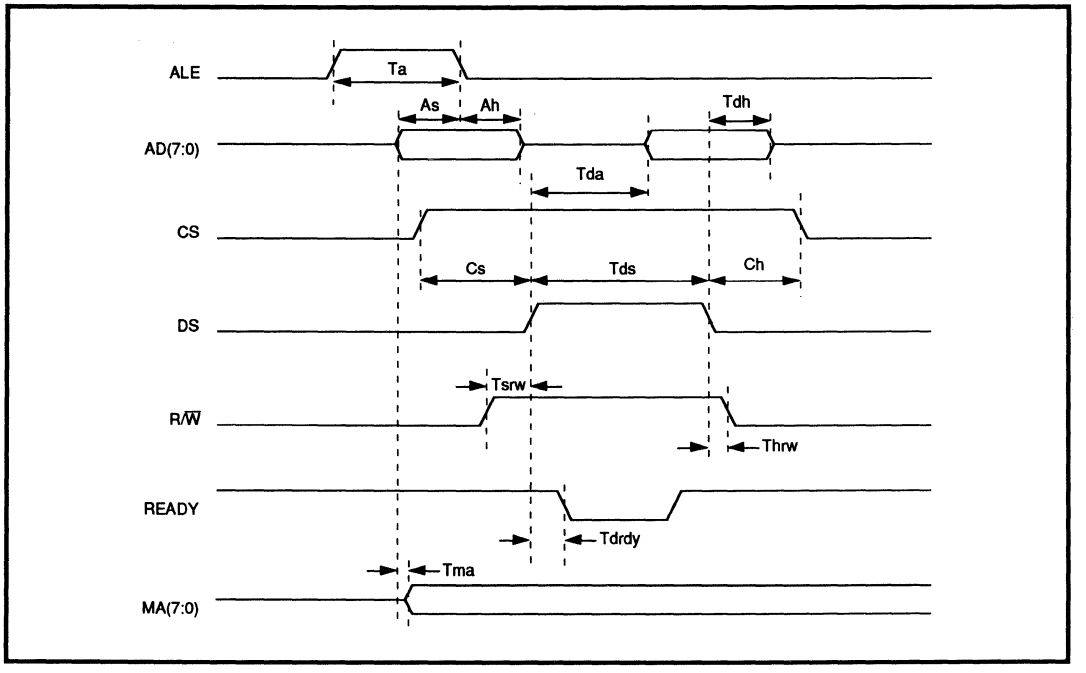



**FIGURE 3: Motorola Register Multiplexed Read Timing**

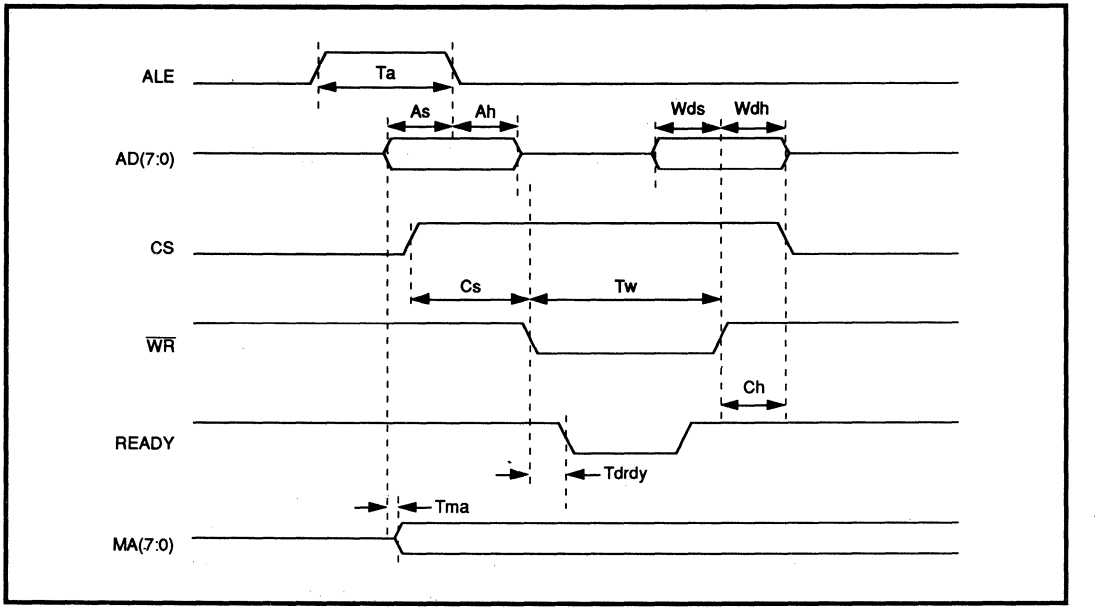



**FIGURE 4: Intel Register Multiplexed Write Timing**

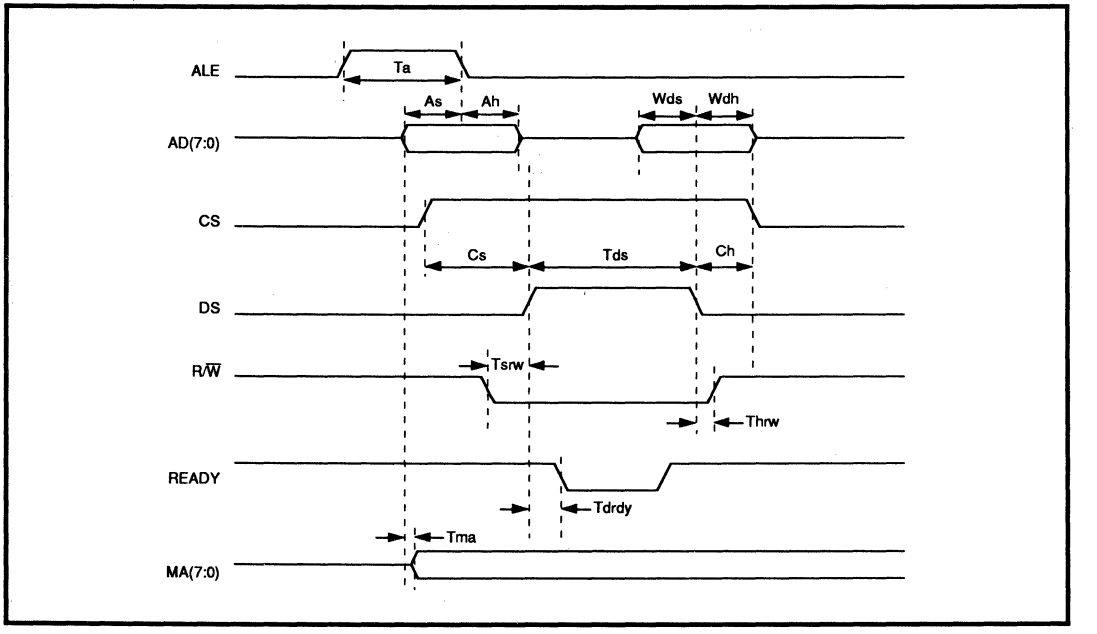



**FIGURE 5: Motorola Register Multiplexed Write Timing**

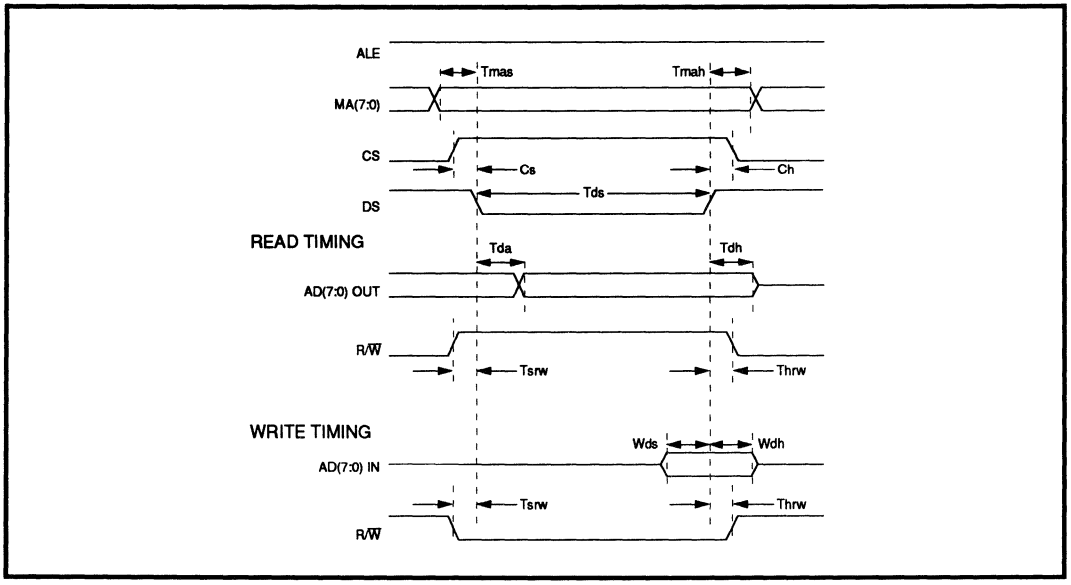



**FIGURE 6: Non-Multiplexed Bus Timing Diagrams**

**Disk Read/Write Timing (Figures 7 and 8)**

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|---|
| T | RRCLK | 3V | 62.5 | | | ns |
| | | 5V | 41 | | | ns |
| T/2 | RRCLK high/low time | 3V | 12 | | | ns |
| | | 5V | 8.5 | | | ns |
| Tr = Tf | RRCLK rise and fall time | 3V | | | 3 | ns |
| | | 5V | | | 2 | ns |
| Dis | NRZ in valid to RRCLK ↑ | 3V | 5 | | | ns |
| | | 5V | 3 | | | ns |
| Dih | RRCLK ↑ to NRZ in invalid | 3V | 5 | | | ns |
| | | 5V | 3 | | | ns |
| As* | $\overline{AMD}$ valid to RRCLK ↑ | 3V | 5 | | | ns |
| | | 5V | 3 | | | ns |
| Dv | RRCLK ↑ to NRZ out | 3V | 5 | | 27 | ns |
| | | 5V | 3 | | 15 | ns |
| Wv* | RRCLK ↑ to $\overline{WAM}$ out | 3V | 5 | | 27 | ns |
| | | 5V | 3 | | 15 | ns |
| Tckd | RRCLK↑ to WCLK ↑ or | 3V | | | 12 | ns |
| | RRCLK ↑ to WCLK ↑ | 5V | | | 8 | ns |
| Note: | ↑ indicates rising edge ↓ indicates falling edge | | | | | |
| | * These specifications are only applicable in the Soft Sector mode. | | | | | |

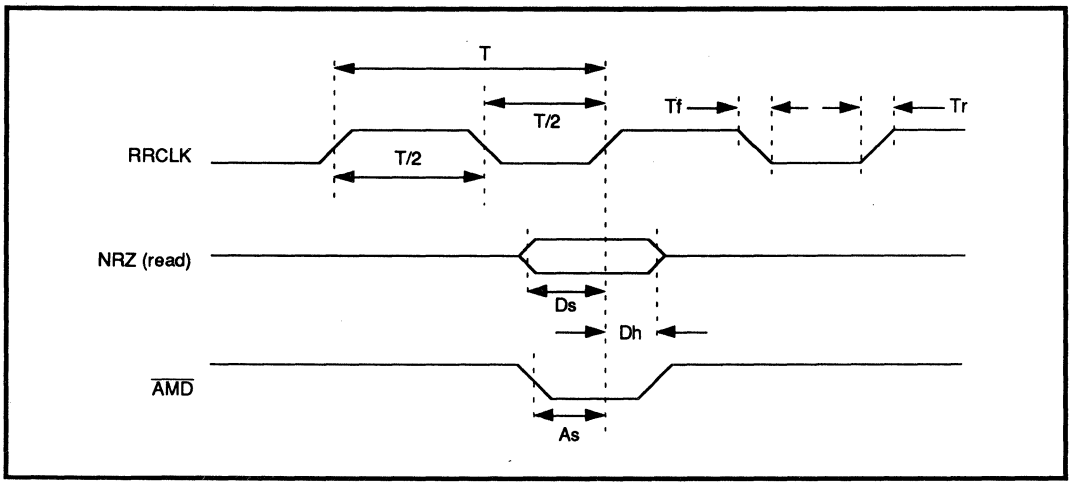



**FIGURE 7: Disk Read Timing**

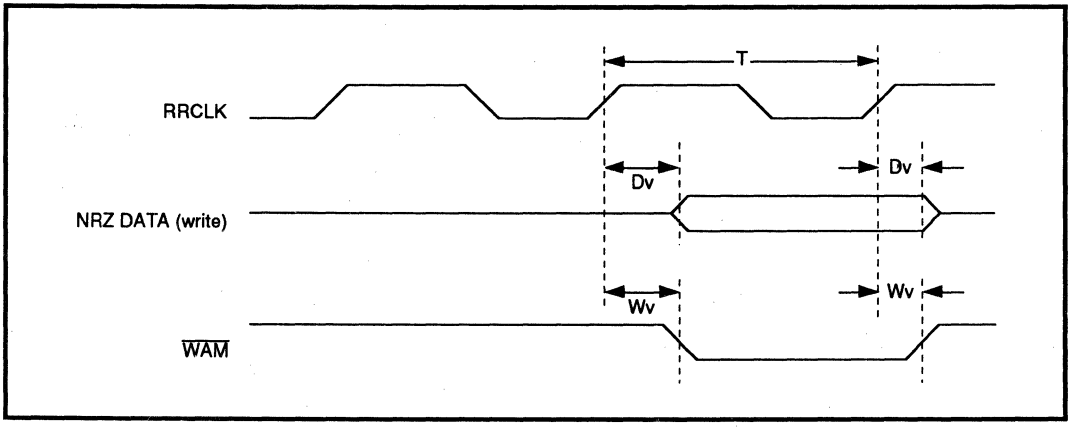



**FIGURE 8: Disk Write Timing**

## ELECTRICAL SPECIFICATIONS (continued)

**BUFFER MEMORY READ/WRITE TIMING PARAMETERS (Figures 9 through 14)**

| PARAMETER | | MIN 5V | MAX 5V | MIN 3.3V | MAX 3.3V | UNIT |
|---|---|---|---|---|---|---|
| T | SYSCLK period | 25 | | 28 | | ns |
| T/2 | SYSCLK high/low time | 10 | | 12 | | ns |
| Tav | SYSCLK / to address valid (Note 1) | | 18 | | 55 | ns |
| Tmsv | SYSCLK / to $\overline{MS}$\ (Notes 1, 6) | | 18 | | 55 | ns |
| Tmsh | SYSCLK / to $\overline{MS}$/ (Note 1) | | 18 | | 55 | ns |
| Tmv | SYSCLK / to $\overline{MOE}$\ (Note 1) | | 18 | | 55 | ns |
| Tmh | SYSCLK / to $\overline{MOE}$/ (Note 1) | | 18 | | 55 | ns |
| Twv | SYSCLK / to $\overline{WE}$\ (Note 1) | | 18 | | 55 | ns |
| Twh | SYSCLK / to $\overline{WE}$/ (Note 1) | | 18 | | 55 | ns |
| Tdov | SYSCLK to data out valid (Note 1) | | 18 | | 40 | ns |
| Tdoh | SYSCLK to data out invalid (Note 1) | | 18 | | 40 | ns |
| Tdis | Data in valid to $\overline{MOE}$ / (SRAM)<br>Data in valid to $\overline{CAS}$ / (DRAM) | 5 | | 5 | | ns |
| Tdih | $\overline{MOE}$ / to data in valid (SRAM)<br>$\overline{CAS}$ / to data in valid (DRAM) | 0 | | 0 | | ns |
| Trv | SYSCLK / to $\overline{RAS}$\ (Note 1) | | 18 | | 40 | ns |
| Trh | SYSCLK / to $\overline{RAS}$/ (Note 1) | | 18 | | 40 | ns |
| Trav | SYSCLK to row address valid (Note 1) | | 18 | | 40 | ns |
| Trah | SYSCLK / to row address invalid (Note 1) | | 18 | | 40 | ns |
| Tcv | SYSCLK / to $\overline{CAS}$\ (Note 1) | | 18 | | 40 | ns |
| Tch | SYSCLK / to $\overline{CAS}$/ (Note 1) | | 18 | | 40 | ns |
| Tcav | SYSCLK / to column address valid (Note 1) | | 18 | | 40 | ns |
| Tcah | SYSCLK / to column address invalid | 0 | | 0 | | ns |

## ELECTRICAL SPECIFICATIONS (continued)

**BUFFER MEMORY READ/WRITE TIMING PARAMETERS (Figures 9 through 14)** (continued)

| PARAMETER | | CONDITIONS | MIN | UNIT |
|---|---|---|---|---|
| Trwl | $\overline{RAS}$\ to $\overline{RAS}$/ | Notes 2, 3 | (RWL + 3)•T-2 | ns |
| Trwh | $\overline{RAS}$/ to $\overline{RAS}$\ | Notes 2, 4 | (RWH + 1)•T-2 | ns |
| Tcwl | $\overline{CAS}$\ to $\overline{CAS}$/ | Note 2 | (CWL + 1)•T-2 | ns |
| Tcwl | $\overline{CAS}$/ to $\overline{CAS}$\ | Notes 2, 5 | (CWL + 1)•T-2 | ns |

Note: Loading capacitance = 30 pF

Note 1: The measured delay for any of the signal indicated by this note will not vary from the measured delay of any other signal indicated by this note by more than TBD (3V), ±1 ns (5V).

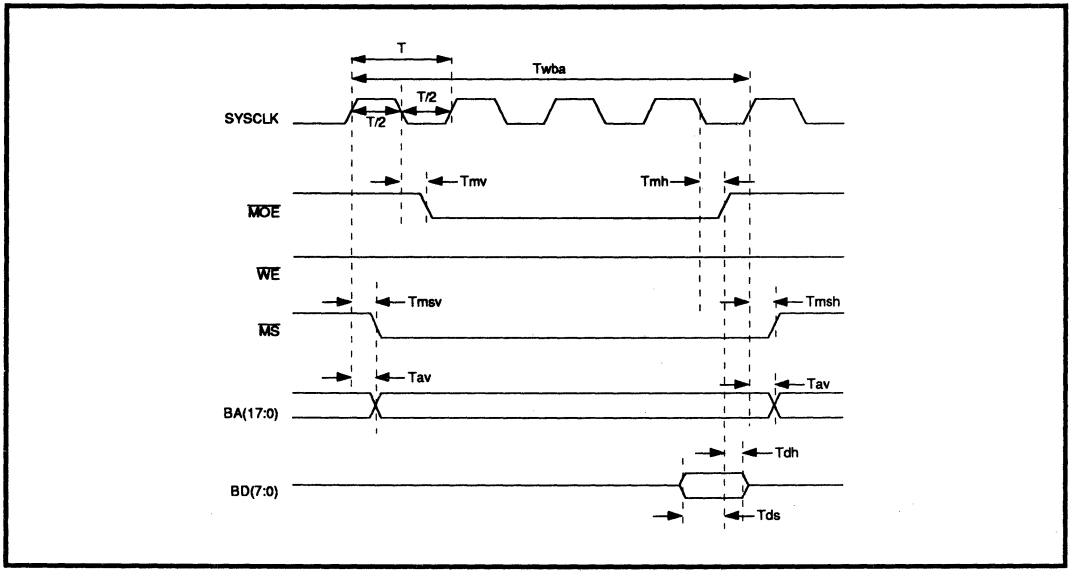
Note 2: RWL, RWH, CWL and CWH are fields in the Buffer Manager Timing Control Register (54H). Each is a two bit field which can contain a value of 0, 1, 2, or 3. These values determine the minimum number of SYSCLK periods (T) for the associated signal width.

Note 3: The minimum width value of Trwl will be generated for refresh cycles and for any buffer memory access cycle except when multiple page mode accesses are performed. When multiple page mode accesses are performed, the width of the $\overline{RAS}$ low pulse is extended until the end of the last $\overline{CAS}$ low cycle.

Note 4: The minumum value of Trwh will be generated whenever the Buffer Manager determines that a buffer request is pending at the completion of the current memory cycle and a page mode access can not be used either because page mode operation is not enabled or the needed location is not within the current page.

Note 5: The minumum value of Tcwh will be generated only between consecutive page mode accesses.

Note 6: $\overline{MS}$ will rise only if the Buffer Manager determines that no additional requests for buffer access are pending. If the Buffer Manager determines that another access is to be made, $\overline{MS}$ is kept low between the accesses for improved speed.




Note: Twba is a functional parameter that gives the duration of one RAM data buffer access cycle in SYSCLK periods. The value is programmed in bits 1-0 of register 54H. These examples show Twba = 4T.

**FIGURE 9: SRAM Read Timing**

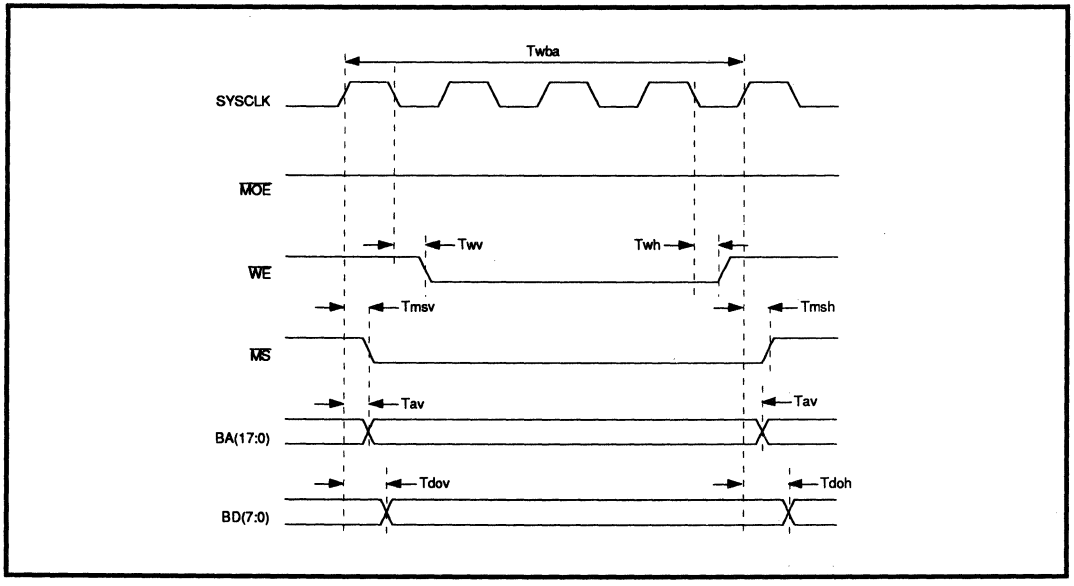



**FIGURE 10: SRAM Write Timing**

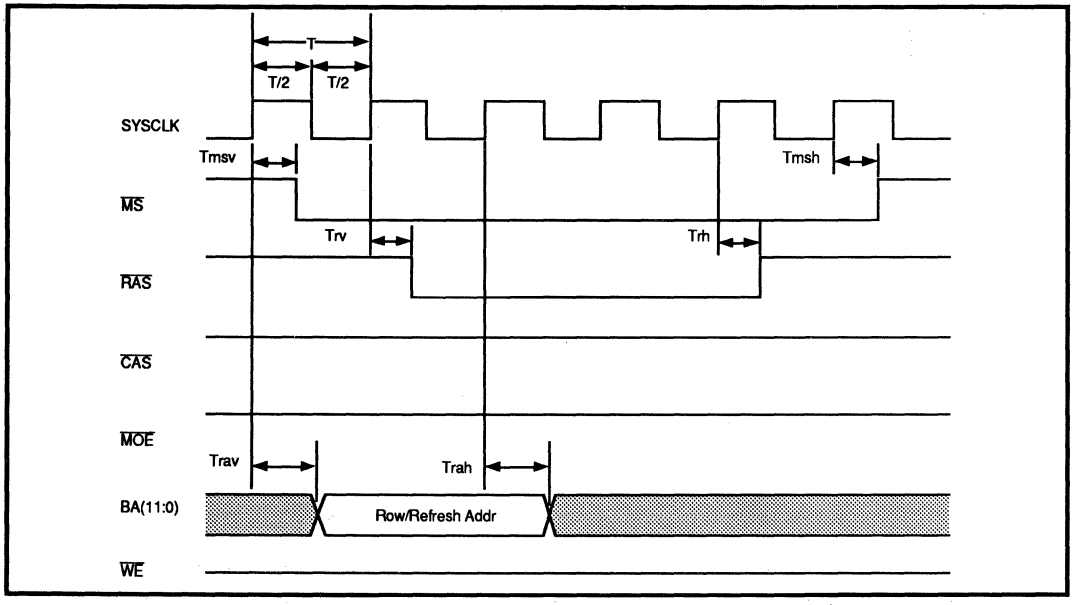



**FIGURE 11: DRAM Timing, Refresh Cycle (Shown with WRL = 0)**

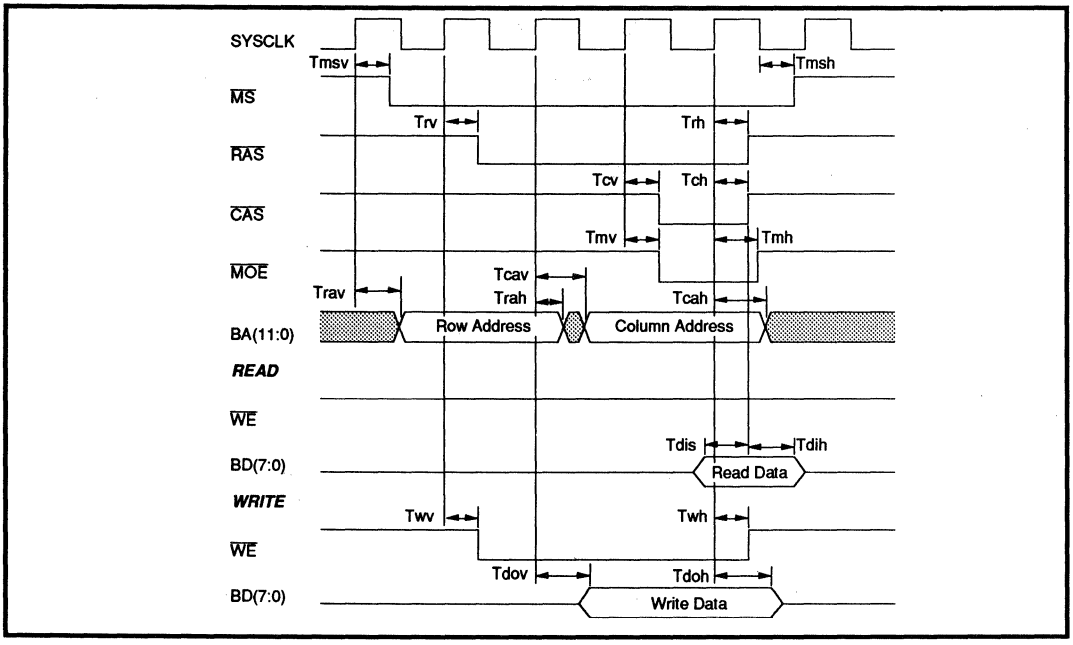



**FIGURE 12: DRAM Timing, Standard Cycle (Shown with RWL = 0 and CWL = 0)**

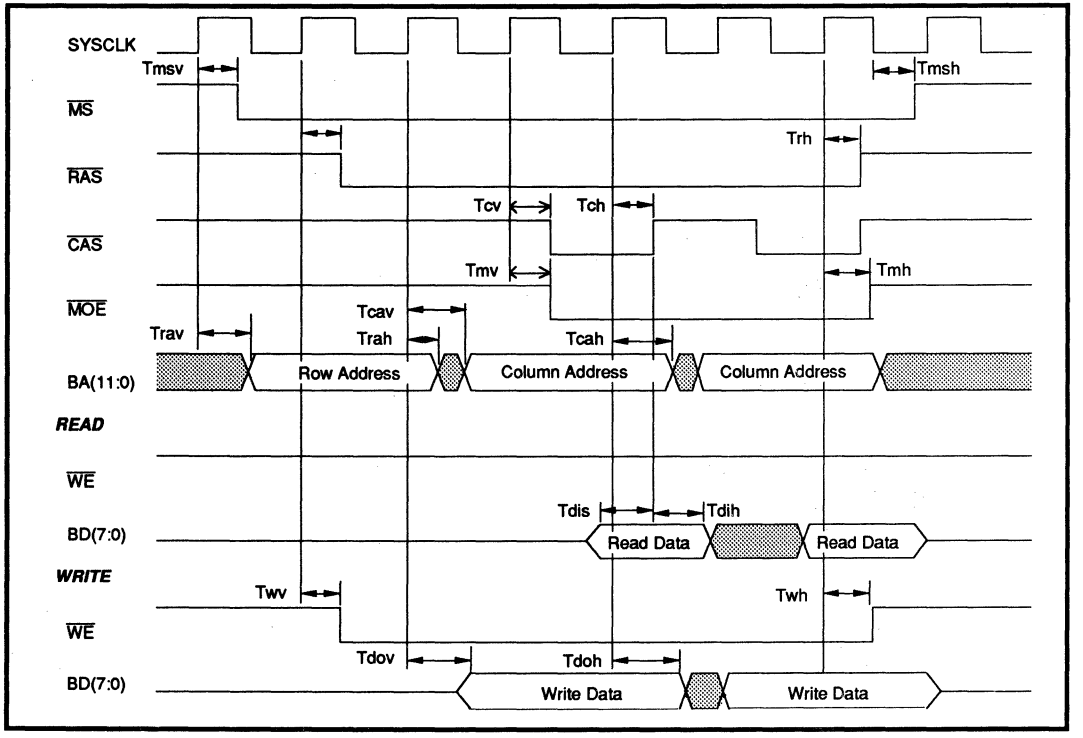



**FIGURE 13: DRAM Timing, Fast Page Cycles (Shown with RWL = 0, RWH = 0, CWL = 0 and CWH = 0)**

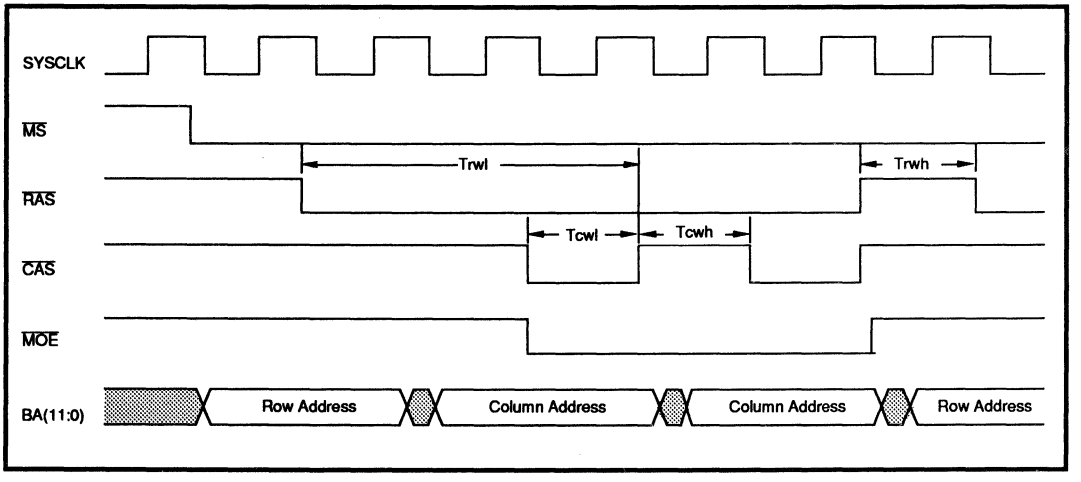



**FIGURE 14: DRAM Timing (Showing the Relationship of RWL, RWH, CWL and CWH to overall timing)**

## ELECTRICAL SPECIFICATIONS (continued)

### AT Host Interface Timing Parameters

| PARAMETER | | MIN 3.3V | MAX 3.3V | MIN 5V | MAX 5V | UNIT |
|---|---|---|---|---|---|---|
| DREQL | $\overline{DACK}$ ↓ to DREQ ↓ | | 50 | | 40 | ns |
| RDTA | $\overline{IOR}$ ↓ to HD(15:0) valid | | 70 | | 50 | ns |
| DMASET | $\overline{DACK}$ ↓ to $\overline{IOW}$ ↓ or $\overline{IOR}$ ↓ | 10 | | 10 | | ns |
| DMAHLD | $\overline{IOR}$ ↑ or $\overline{IOW}$ ↑ to $\overline{DACK}$ ↑ | 10 | | 10 | | ns |
| RDHLD | $\overline{IOR}$ ↑ to HD (15:0) hi-Z | 0 | 20 | 0 | 20 | ns |
| WDS | HD(15:0) setup to $\overline{IOW}$ ↑ | 40 | | 30 | | ns |
| WDHLD | HD(15:0) hold from $\overline{IOW}$ ↑ | 10 | | 10 | | ns |
| RWPULSE | $\overline{IOR}$ or $\overline{IOW}$ low pulse width | 80 | | 80 | | ns |
| RWH | $\overline{IOR}$ or $\overline{IOW}$ high pulse width | 50 | | 50 | | ns |
| CS16L | $\overline{HCS0}$ ↓, A(2:0) ↓, A9 ↓ or $\overline{HCS1}$ ↑ to $\overline{IOCS16}$ ↓ | | 30 | | 20 | ns |
| IOCHL | $\overline{IOR}$ or $\overline{IOW}$ ↓ to $\overline{IOCHRDY}$ ↓ | 25 | 35 | | 25 | ns |
| ADRSET | $\overline{HCS0}$, A(2:0), A9/$\overline{HCS1}$ setup to $\overline{IOR}$ ↓ or $\overline{IOW}$ ↓ | 25 | | 25 | | ns |
| ADRHLD | $\overline{HCS0}$, A(2:0), A9/$\overline{HCS1}$ hold from $\overline{IOR}$ ↑ or $\overline{IOW}$ ↑ | 10 | | 0 | | ns |
| Note: Loading capacitance = 30 pF | | | | | | |

### Functional Specification

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| IOCHTW | $\overline{IOCHRDY}$ pulse width | | 0 | | 5xBCLK | ns |

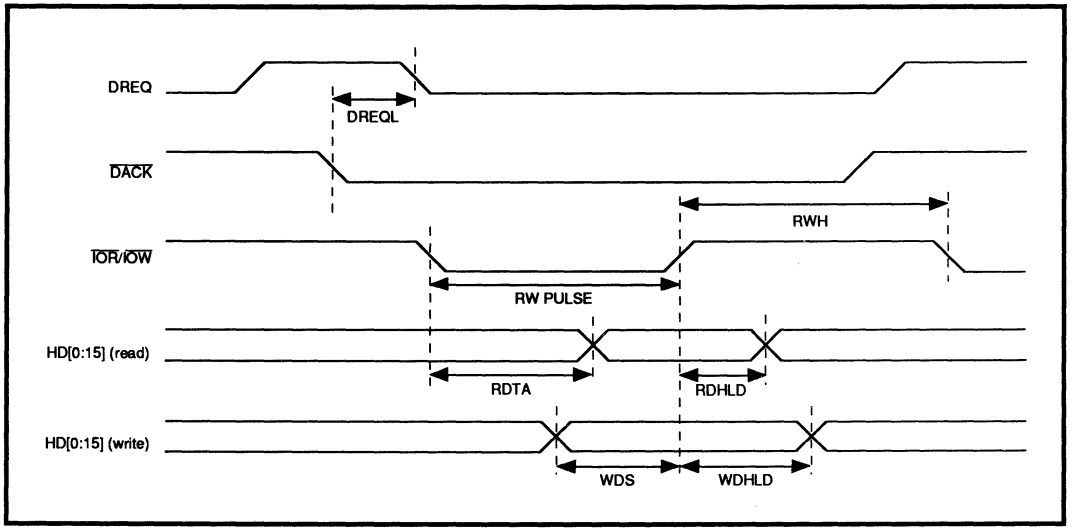



**FIGURE 15: Host DMA 8-16 Bit Interface Timing (Non-demand mode)**

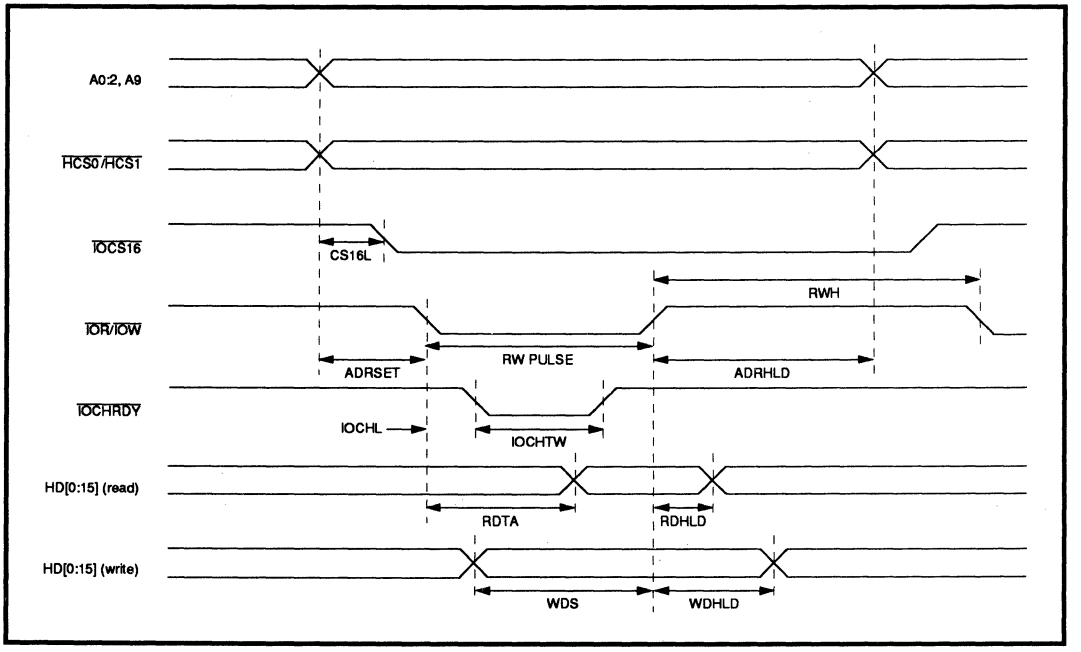



**FIGURE 16: Host Programmed I/O 8-16 Bit Timing**

8

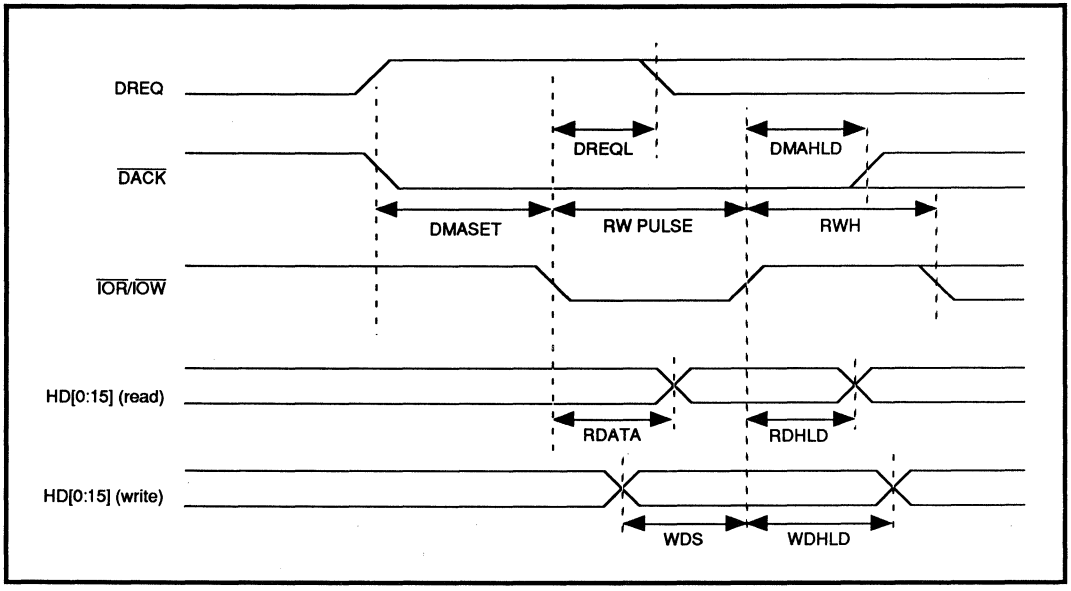



**FIGURE 17: Host DMA 8/16-Bit Interface Timing (Demand Mode)**

**RESET Assertion Timing Parameters (Figure 18)**

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| Trpwl | $\overline{RST}$ pulse width low | NOT Power On Reset | 500 | | | ns |
| | | Power On Reset | 7.5 | | | µs |

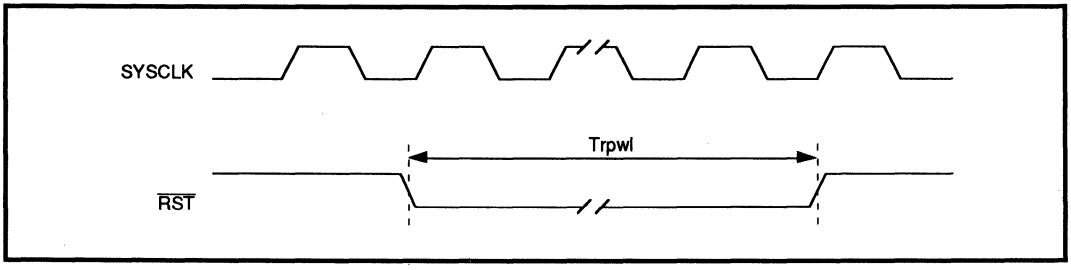
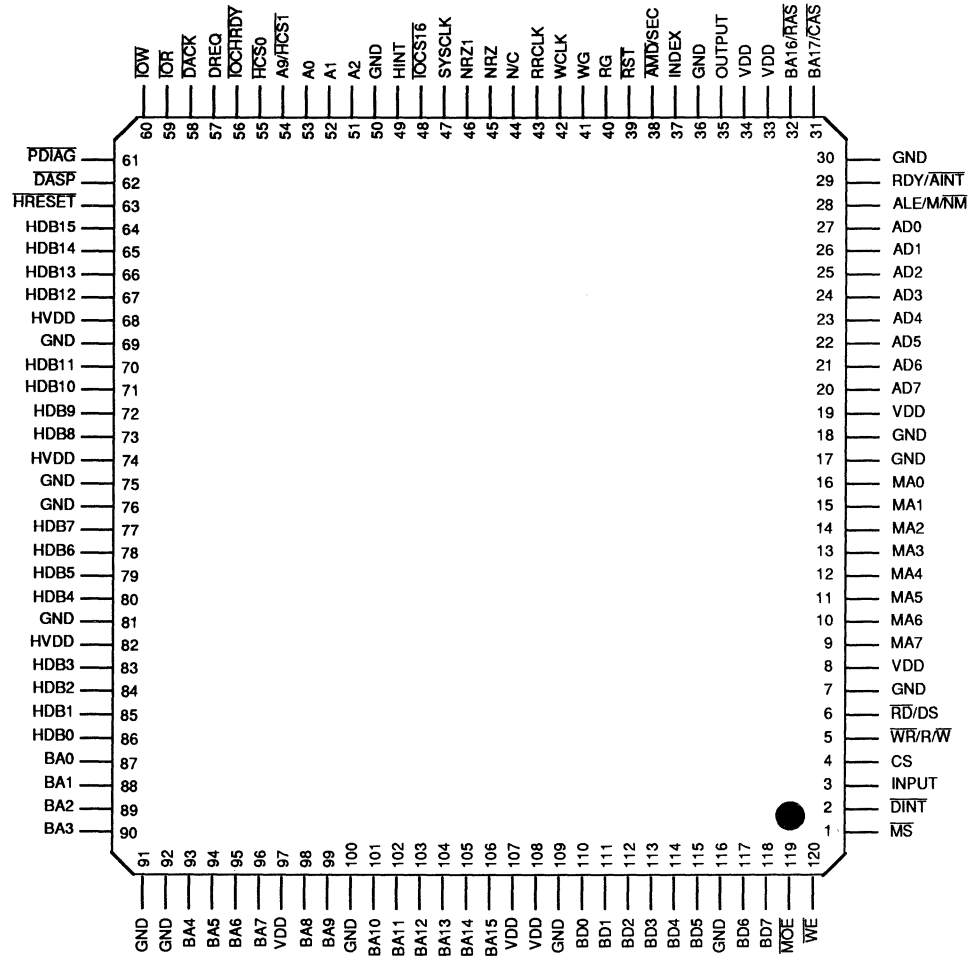



**FIGURE 18: RESET Assertion Timing**




**120-Lead TQFP**

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**Advance Information:** Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.



Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680, (714) 573-6000, FAX: (714) 573-6914

**Notes:**

silicon systems®
A TDK Group Company

# SSI 32C9340
## PCMCIA Combo Controller with Reed Solomon, 32/48 Mbit/s
## Target Specification

January 1993

## DESCRIPTION

The SSI 32C9340 is a CMOS VLSI device which integrates major portions of the hardware needed to build a PCMCIA and/or ATA drive hard disk controller. The SSI 32C9340's place in the Silicon Systems' chip family is illustrated in the hierarchy chart in Figure 1. It provides most of the functional circuitry necessary to build a PCMCIA intelligent disk.

The SSI 32C9340 is capable of supporting interleaved host and disk transfers while maintaining a disk data transfer rate of up to 32 Mbit/s while operating in a 3.3V environment. This part also operates in a 5 volt environment supporting disk transfer rates of up to 48 Mbit/s.

The SSI 32C9340 includes a multi-port Buffer Manager, a storage controller and a high performance PCMCIA host interface block that incorporates extensive hardware support — including direct connection to a PCMCIA or ATA bus.

The SSI 32C9340 performs all the controller functions for the peripheral device including: Serialization and deserialization of data; and, ECC generation, checking and on-the-fly data correction.

## FEATURES

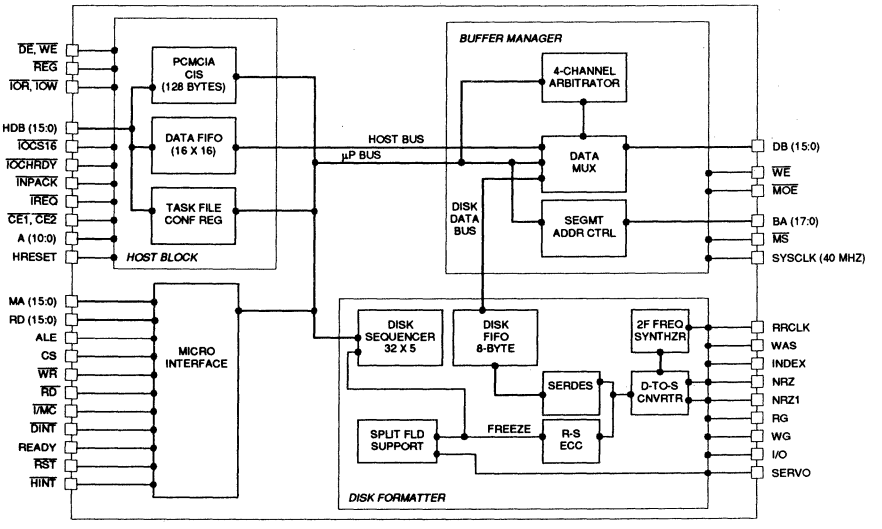
**HOST INTERFACE:**

- **PCMCIA/ATA and ATA compatible host interface**
- **Hardware and software compatible with PCMCIA bus standard, revision 2.0**
- **Separate host interface VDD to allow 3.3V drive to plug into 5V systems**
- **Programmable 256-byte PCMCIA CIS provided**
- **High Current drivers for direct connection to the PCMCIA or AT bus**
- **Both memory and I/O interfaces supported for PCMCIA**
- **Includes IBM AT compatible Task File registers**
- **Hardware added to provide Multi-Sector data transfers without microprocessor intervention**
- **Automatic BUSY, INTRQ**
- **16 byte FIFO to improve throughput**
- **Automatic command decoding of write, write buffer and format commands**
- **Automatic update of the host task file registers in both LBA mode and Cyl/Hd/Sec mode**
- **Power-down IO pins**

(continued)

8

## BLOCK DIAGRAM



# SSI 32C9340
# PCMCIA Combo Controller with Reed Solomon, 32/48 Mbit/s

## FEATURES (continued)

BUFFER MANAGER:

- Supports Buffer RAM throughput up to:
  - 5V: 20 MByte/sec for SRAM and 17.2 MByte/sec for DRAM (with 40MHz SYSCLK)
  - 3.3V: 15 MByte/sec for SRAM and 12MByte/sec for DRAM (with 30 MHz SYSCLK)
- Programmable microprocesssor scratch pad area
- Auto data streaming capability
- Supports Multiple sector host data transfer
- Supports up to 1M byte DRAM and up to 256K SRAM
- Supports variable DRAM and SRAM timings and sizes
- Reload transfer counter and host address pointers
- Supports page mode DRAM access
- Programmable DRAM page mode burst length
- Programmable DRAM refresh period
- Separate host, disk, and microprocessor buffer RAM address pointers
- Provides protection logic for buffer data allowing simultaneous host and disk accesses to the same buffer segment.

DISK FORMATTER:

- Advanced sequencer organized in 31 x 5 bytes
- Advanced branch and interrupt logic
- Defect management support
- Supports multiple-sector data transfers
- NRZ byte synchronization time out timer
- Three-index counter providing limit of search and retry
- 8-byte stack for header information storage
- 16-byte disk data FIFO
- Sector header or microprocessor-based split data field processing logic supporting embedded servo and zone-bit recording
- Supports variable data field length
- Disk transfer rate up to:
  - 3.3V: 32 Mbit/s second NRZ
  - 5V: 48 Mbit/s second NRZ
- Power Down Mode

MICROPROCESSOR INTERFACE:

- High speed internal register access
- Programmable wait state insertion
- Supports both Intel and Motorola type microprocessers

ERROR CORRECTION LOGIC:

- Enhanced 16-bit CRC polynomial with one order of magnitude better burst error detection than CCITT-CRC16
- Non-interleaved 88-bit Reed Solomon Code of degree 8 operation on 10-bit symbols
- Automatic on-the-fly in-buffer error correction
- Selectable on-the-fly error correction span of 11 or 31 bits signal burst
- Calculation of buffer offsets and masks for on-the-fly ECC within one half of a sector time
- On the fly in-buffer correction accomplished in no more than 5 buffer reads and writes through an independent channel
- Capable of correcting by software four 10-bit symbols in error
- Guaranteed to correct by software one 31-bit burst or two 11-bit bursts
- Detects up to one 51-bit burst or three 11-bit bursts

OTHERS:

- Automatic power supply level detection circuit
- JEDEC conformant 3.3V specification
- TTL-Level compatible input receivers at 3.3V or 5V
- Avaiable in 120-pin surface mount TQFP

## FUNCTIONAL DESCRIPTION

The SSI 32C9340 is capable of operating in either a 3.3 volt or 5 volt environment. In addition, the SSI 32C9340 can operate in a mixed voltage environment with the host interface operating in a 5 volt environment and the remainder of its interfaces operating in a 3.3 environment. This allows a drive designed to operate on 3.3 volts to interface with a host which is operating on 5 volts.

The SSI 32C9340 contains the following four major functional blocks:

Microprocessor Interface

PCMCIA/ATA Interface

Disk Formatter

Buffer Manager

The Microprocessor Interface allows the local microprocessor access to all of the SSI 32C9340 internal control registers and any location within the buffer memory. The microprocessor, by writing and reading the internal registers, can control all activities of the SSI 32C9340. The microprocessor can elect to perform host and/or disk operations directly, or it can enable the advanced features of the SSI 32C9340 which can perform these operations automatically.

The PCMCIA/ATA Interface block can interface with PCMCIA interface as a PCMCIA/ATA device or with a PC AT bus. The SSI 32C9340 has on-board sensing logic to help determine whether it is operating in either the PCMCIA or ATA mode. The interface includes 16 mA (24 mA @5V) drivers allowing for direct connection of the SSI 32C9340 to either the PCMCIA or PC AT bus. The interface is highly automated, capable of performing multiple block transfers without micro-controller involvement. The PCMCIA/ATA block interfaces directly with the Buffer Manager via an internal speed matching FIFO. This FIFO, the bandwidth capabilities of the Buffer Manager, plus the advanced features of the PCMCIA/ATA Interface guarantee sustained full speed transfers.

The Disk Formatter performs the serialization and deserialization of data. It provides all of the necessary functions to control track formatting, header search, and the reading and writing of data. The heart of the Disk Formatter is an advanced programmable sequencer. The sequencer can contain 31 instructions, each of which is 5 bytes (40 bits) in width. The width of the instructions allows for sophisticated branching techniques which increase the flexibility and power of the sequencer. The disk interface can be configured through a wide range of capabilities. This allows the SSI 32C9340 to interface with nearly any read/write channel. This allows the user of the SSI 32C9340 to select the read/write channel best suited to the device. Of course, by selecting the SSI 32C9340 controller and the SSI 32P4330 Read Channel with 1,7 ENDEC, you are guaranteed a problem free interface.

Within the Disk Formatter are the ECC generator/checker and ECC corrector. The generator/checker provides the ability to generate or check a 32 bit ECC for headers and an 88 bit Reed Solomon code for data. If the checker detects an error in an 88 bit Reed Solomon data field, the syndrome information is transferred into the corrector. The corrector then performs the necessary operations to determine if the error was correctable and, if it was correctable, the corrector interfaces directly with the buffer controller and performs the correction automatically. The corrector performs its correction within one half of a sector. This guarantees that the corrector will always be available to correct the next sector if necessary.

As its name implies, the Buffer Manager manages the data buffer of the controller. The Buffer Manager can support either SRAM or DRAM. When configured to operate with DRAM, the Buffer Manager automatically performs necessary refresh cycles. The buffer manager creates all of the necessary timing and control signals for a wide range of memory types and speeds. Besides interfacing with the buffer memory, the Buffer Manager interfaces with the ATA Interface block, the Disk Formatter block, the ECC corrector and the microprocessor. If more than one of these devices requires access to the buffer memory, the Buffer Manager arbitrates the requests automatically. The Buffer Manager of the SSI 32C9340 can sustain ATA operations at the rate of 3 (6 @ 5V) megawords per second, Disk Formatter operations at 32 (48 @ 5V) megabits per second and still has sufficient bandwidth left to handle on-the-fly ECC corrections and microprocessor accesses without degrading performance on any of the interfaces.

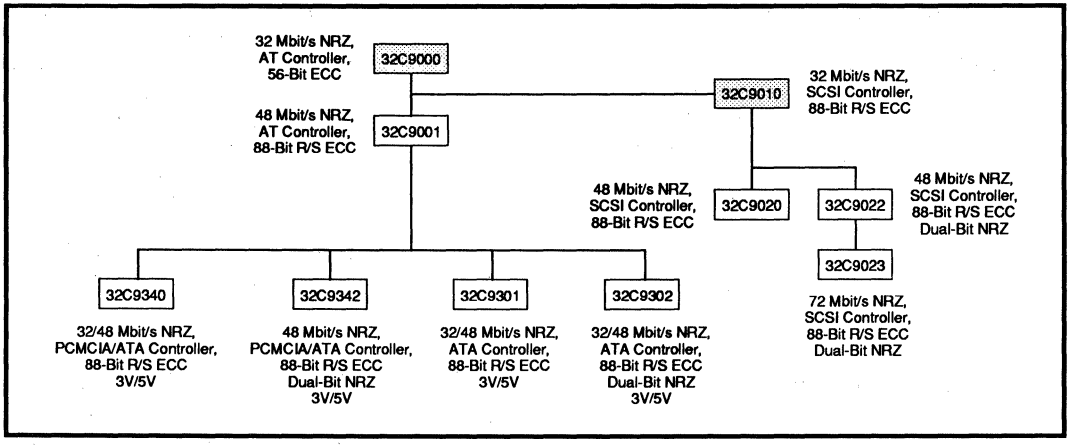



**FIGURE 1: Silicon Systems's Disk Controller Chip Hierarchy**

## PIN DESCRIPTION

I = input, O = output; Z = tri-state output, OD = open drain output. All unused inputs must be tied to the inactive state to VCC or GND, respectively.

**BUFFER MANAGER INTERFACE**

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| BA17/$\overline{CAS}$ | O | Buffer Memory Address 17/Column Address Strobe: This signal is used for addressing the buffer memory in SRAM mode or as the column address strobe in DRAM mode. |
| BA16/$\overline{RAS}$ | O | Buffer Memory Address 16/Row Address Strobe: This signal is used for addressing the buffer memory in SRAM mode or as the row address strobe in DRAM mode. |
| $\overline{MOE}$/$\overline{MS}$ | O | Memory Output Enable/Memory Select: When configured as $\overline{MOE}$, this signal is active during buffer memory reads. When configured as $\overline{MS}$ this signal is active during both buffer memory reads and buffer memory writes. This timing of the $\overline{MS}$ signal follows that of the address pins. |
| $\overline{WE}$ | O | Write Enable: This signal is asserted low when a buffer memory write operation is active in both SRAM and DRAM modes. |
| SYSCLK | I | System Clock: This is the clock input that is used to generate buffer memory access cycles. |
| BD (7:0) | I/O | Buffer Memory Data Bus: These eight signals are bits 7-0 of the 8-bit parallel data lines to/from the buffer memory. Note that BD6 is used to select between the Intel and Motorola-style microprocessor interfaces. IF BD6 is externally pulled up when $\overline{RST}$ is asserted, Intel mode is used; if BD6 is externally pulled down when $\overline{RST}$ is asserted, Motorola mode is used. |
| BA (15.0) | | Buffer Memory Address Lines: These are signals 15-0 for addressing the buffer memory. |

**MICROPROCESSOR INTERFACE**

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| $\overline{DINT}$ | O, OD, Z | Interrupt: This signal is an interrupt line to the microprocessor. It is the combined interrupt line of the disk side and host side interrupts when pin RDY/$\overline{HINT}$ is programmed as Ready; otherwise it only signals the occurrence of disk side interrupt events. This signal is programmable for either a push-pull or open-drain output circuit. This signal powers up in the high-Z state. |
| CS | I | Chip Select: This signal must be asserted high for all microprocessor accesses to the registers of this chip. |
| $\overline{WR}$/R/$\overline{W}$ | I | Write Strobe/Read/Write: When the Intel bus control interface is selected, this signal acts as the $\overline{WR}$ signal. When the write strobe signal is asserted low and the CS signal is asserted high, the data on the AD bus will be written to the register.<br>When the Motorola bus control interface is selected, this signal acts as the DS signal. A high on the R/$\overline{W}$ signal along with the signal asserted and the CS signal asserted high indicates a read operation. A low on the R/$\overline{W}$ signal along with the signal asserted and the CS signal asserted high indicates a write operation. Note that when non-multiplexed address and data busses are sued, this pin configured as $\overline{DS}$ (active low). |
| $\overline{RD}$/DS | I | Read Strobe/Data Strobe: When the Intel bus control interface is selected, this signal acts as the $\overline{RD}$ signal. When the read strobe signal is asserted low and the CS signal is asserted high, the data from the specified register will be driven onto the AD bus.<br>When Motorola bus control interface is selected the signal acts as the DS signal. A high on the R/$\overline{W}$ signal along with this signal asserted and the CS signal asserted high indicates a read operation. A low on the R/$\overline{W}$ signal along with this signal asserted and the CS signal asserted high indicates a write operation. Note that when non-multiplexed address and data buses are used, this pin configured as $\overline{DS}$ (active low). |
| RDY/$\overline{HINT}$ | O | Ready/Host Side Interrupt: When programmed as the ready function, this signal is deasserted low for the microprocessor to insert wait states to allow time for the chip to respond to the access.<br>When programmed as host side interrupt, this pin interrupts the microprocessor when there is an AT host related interrupt event. The interrupt signal is programmable for either a push-pull or open-drain output circuit. This signal powers up as the "ready" function. |
| AD (7:0) | I/O | Microprocessor Address/Data Bus: These signals are bidirectional multiplexed microprocessor address/data lines when the chip is configured in the multiplexed bus mode. Otherwise these signals are the bidirectional data lines. |
| MA (7:0) | I/O | Microprocessor Address/Bus: These signals are nonmultiplexed address input or demultiplexed address output lines. |

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## PIN DESCRIPTION (continued)

### MICROPROCESSOR INTERFACE (continued)

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| ALE | I | Address Latch Enable/Intel or Motorola Mode Select: If this input is tied high after reset (i.e., after $\overline{RST}$ has been asserted and released), the microprocessor interface is configured for Motorola mode with DS active high. If this input is tied low after reset, the microprocessor interface is configured for Motorola mode with $\overline{DS}$ active low. If this input makes a low to high transition after reset, then the microprocessor interface is configured for Intel mode. In this case, this pin functions as the address latch enable, and the latched address is output on the MA(7:0) pins. |
| $\overline{RST}$ | I | Reset: An asserted low input generates a component reset that stops all operations within the chip and deasserts all output signals. All input/output signals are set to the high-Z state. |

### DISK FORMATTER INTERFACE

| | | |
|---|---|---|
| INPUT/OUTPUT | I/O | Disk Sequencer Input/Output: When configured as Input, this signal may be used to synchronize the disk sequencer to an external event. When configured as Output, this pin is controlled by bit 2 of the disk sequencer's control field. When $\overline{RST}$ is asserted, this pin as configured as Input. |
| INDEX | I | Index: This is the input for the Index pulse received from the disk drive. |
| $\overline{AMD}$/SECTOR | I/O | Address Mark Detect/Sector: In hard sector mode, this is the input for the sector pulse from the disk drive. In soft sector mode, a low-level input during a read indicates an address mark was detected. |
| RG | O | Read Gate: This signal is asserted when a disk read operation is in progress and the NRZ data is input to the chip. |
| WG | O | Write Gate: This signal is used to enable the writing of NRZ data out to the storage device during a write operation. |
| RRCLK | I | Read Reference Clock: This signal input clocks the NRZ data. |
| NRZ | I/O | Non Return to Zero: This signal is the read data input from this disk drive when the read gate signal is asserted; it is the write data output to the disk drive when the write gate signal is asserted. |

**HOST INTERFACE PINS**

| | | |
|---|---|---|
| $\overline{IOCS16}$ | O, OD | 16-Bit Data Select: This signal indicates that a 16-bit sector buffer transfer is active on the host data bus. This pin is open-drain in ATA mode, but push-pull in PCMCIA mode. This pin is not driven while $\overline{RST}$ is asserted, and remains so until the interface mode (PCMCIA or ATA) is determined. |
| R/$\overline{BUSY}$/IRQ | O, Z | Ready/$\overline{BUSY}$/Host Interrupt Request: In PCMCIA mode, this pin is the Ready/$\overline{BUSY}$ signal when configured with a memory interface. In ATA mode, or in PCMCIA mode when configured with an I/O interface, this pin is the host interrupt request, and is asserted to indicate to the host that the controller needs attention. As an interrupt request, this pin is active high in ATA mode, but active low in PCMCIA mode. This pin is always driven in PCMCIA mode, but will be tri-stated when the drive is not selected or interrupts are not enabled in ATA mode. This pin is driven low while $\overline{RST}$ is asserted, and remains so until the interface mode (PCMCIA or ATA) is determined. If PCMCIA mode is selected after reset, the chip is configured with a memory interface, and this pin will reflect the status of the BUSY bit in the Drive Status Register. |
| A(8:0), A10 | I | Host Address Lines: The host address lines A(8:0) and A10 are used to access the various PC/AT control, status, and data registers. |
| A9/$\overline{HCS1}$ | I | A9/$\overline{HCS1}$: This is a multiplexed input pin. When in PCMCIA mode, or when register 4CH, bit 3 is reset, this is host address line A9. When register 4CH, bit 3 is set in ATA mode, this is Host chip select 1 (active low). |
| $\overline{CE0}$/$\overline{HCS0}$ | I | Host Chip Select 0/Card Enable 1: This signal when low, selects access to the control, status, and data registers. It is configured as $\overline{HCS0}$ in ATA mode, and as $\overline{CE1}$ in PCMCIA mode. |
| $\overline{WAIT}$/IOCHRDY | O, Z | Wait/I/O Channel Ready: This signal is asserted low to extend host transfer cycles when the controller is not ready to respond. This pin is always driven in PCMCIA mode, but will be tri-stated when a read or write is not in progress in ATA mode. This pin is tri-state while $\overline{RST}$ is asserted, and remains so until the interface mode (PCMCIA or ATA) is determined. |
| $\overline{INPACK}$/DREQ | O, Z | Input Acknowledge/DMA Request: In PCMCIA mode, this pin is configured as $\overline{INPACK}$, and is asserted when a valid address and chip select are present. In ATA mode, this pin is configured as the DMA request signal, and is used during DMA transfer between the host and the controller. In ATA mode, this pin is tri-stated when DMA transfers are not enabled. This pin is tri-state while $\overline{RST}$ is asserted, and remains so until the interface mode (PCMCIA or ATA) is determined. |
| $\overline{REG}$/$\overline{DACK}$ | I | Register Select and I/O $\overline{ENABLE}$/DMA $\overline{ACKNOWLEDGE}$: In PCMCIA mode, this pin is configured as $\overline{REG}$, and selects the attribute memory space or I/O space when asserted. In ATA mode, this pin is configured as $\overline{DACK}$, and is used as the DMA acknowledge signal during DMA data transfers. |
| $\overline{IOR}$ | I | I/O Read: Asserted by the host during a host I/O read operation. When asserted with a valid address and chip selects, status or data is enabled onto the host data bus. |
| $\overline{IOW}$ | I | I/O Write: Asserted by the host during a host I/O write operation. When asserted with a valid address and chip selects, data from the host data bus is strobed into the controller. |

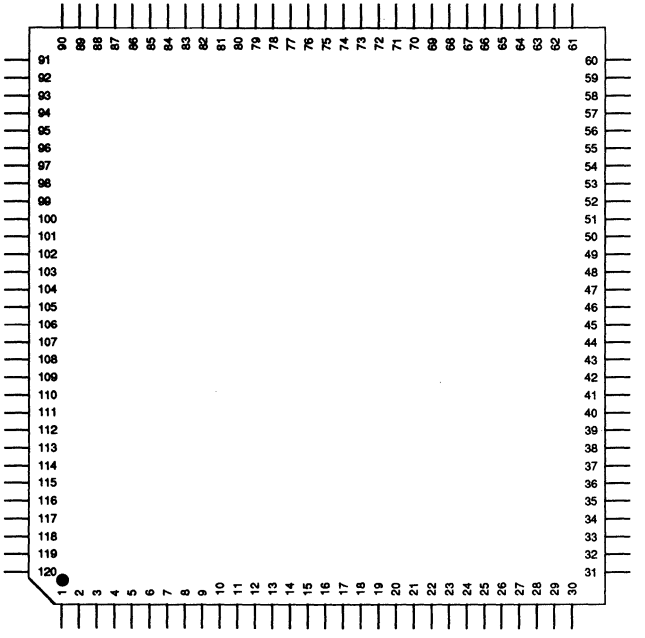
## PIN DESCRIPTION (continued)

### HOST INTERFACE PINS (continued)

| | | |
|---|---|---|
| HRESET/$\overline{\text{HRESET}}$ | I | Host Reset: This signal, when active, initializes the control/status registers and stops any command in process. It is active low in ATA mode, but active high in PCMCIA mode. |
| HDB(15:0) | I/O | Host Data Bus: This bus is used to transfer data and status between the host and the controller. These pins are not driven while $\overline{\text{RST}}$ is asserted, and remain so until the interface mode (PCMCIA or ATA) is determined. |
| $\overline{\text{CE2}}$ | I | Card Enable 2: This signal, when low, selects access to the control, status, and data registers and may enable use of the upper half of the data bus. It is used only in PCMCIA mode. |
| $\overline{\text{HOE}}$/SELATA | I | Output Enable/Select ATA Mode: To determine which host interface to use, this pin is sampled starting at least 8 µs after $\overline{\text{RST}}$ is deasserted, and continuing until at least 25 µs after $\overline{\text{RST}}$ is deasserted. If this pin is high at any time during this sampling period, the interface will immediately be configured for PCMCIA mode, and the sampling will end. If the pin remains low throughout the sampling period, the interface will be configured for ATA mode. Once in PCMCIA mode, this pin is configured as output enable ($\overline{\text{HOE}}$), and is asserted by the host during a common memory or attribute memory read. When asserted with a valid address and chip select, data is enabled onto the host data bus. In ATA mode, this signal is ignored. |
| $\overline{\text{HWE}}$ | I | Write Enable: In PCMCIA mode, this signal is asserted by the host during a common memory or attribute memory write. When asserted with a valid address and chip select, data from the host data bus is strobed into the controller. In ATA mode, this signal is ignored. |
| $\overline{\text{STSCHG}}$/PDIAG | I, O, | Status Changed/Passed Diagnostics: In PCMCIA mode, this pin is used as the Status Changed output. In ATA mode, this pin is used as the Passed Diagnostics signal and may be an input or an open-drain output. This pin is tri-state while $\overline{\text{RST}}$ is asserted, and remains so until the interface mode (PCMCIA or ATA) is determined. |
| $\overline{\text{SPKR}}$/$\overline{\text{DASP}}$ | I/OD | Speaker/Drive Active-Slave Present: In PCMCIA mode, this pin is used as the Speaker pin, and is a push-pull output. In ATA mode, this pin is used as the Drive Active/Slave Present signal, and is an input or an open-drain output. In ATA mode, this pin is used for Master/Slave drive communications and/or for driving an LED. This pin is tri-state while $\overline{\text{RST}}$ is asserted, and remains so until the interface mode (PCMCIA or ATA) is determined. |

## PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.




**120-Lead TQFP**

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**Target Specification:** The target specification is intended as an initial disclosure of specification goals for the product. The specifications are based on design goals, subject to change and are not guaranteed.



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**Notes:**

silicon systems®
A TDK Group Company

# SSI 32C9342
## PCMCIA Combo Controller with Reed Solomon, 48 Mbit/s
## Target Specification

January 1993

## DESCRIPTION

The SSI 32C9342 is a CMOS VLSI device which integrates major portions of the hardware needed to build a PCMCIA and/or ATA drive hard disk controller. The SSI 32C9342's place in the Silicon Systems' chip family is illustrated in the hierarchy chart in Figure 1. It provides most of the functional circuitry necessary to build a PCMCIA intelligent disk.

The SSI 32C9342 is capable of supporting interleaved host and disk transfers while maintaining a disk data transfer rate of up to 48 Mbit/s while operating in either a 3.3 volt or 5 volt environment.

The SSI 32C9342 includes a multi-port Buffer Manager, a storage controller and a high performance PCMCIA host interface block that incorporates extensive hardware support — including direct connection to a PCMCIA or ATA bus.

The SSI 32C9342 performs all the controller functions for the peripheral device including: Serialization and deserialization of data; and, ECC generation, checking and on-the-fly data correction.

## FEATURES

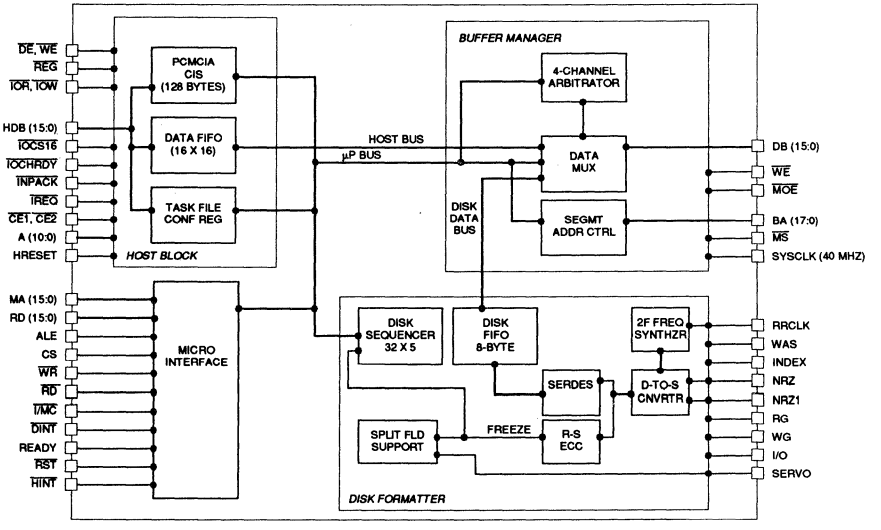
**HOST INTERFACE:**

- **PCMCIA/ATA compatible host interface**
- **Hardware and software compatible with PCMCIA bus standard, revision 2.0**
- **Separate host interface VDD to allow 3.3V drive to plug into 5V systems**
- **Programmable 256-byte PCMCIA CIS provided**
- **High Current drivers for direct connection to the PCMCIA or AT bus**
- **Both memory and I/O interfaces supported for PCMCIA**
- **Includes IBM AT compatible Task File registers**
- **Hardware added to provide Multi-Sector data transfers without microprocessor intervention**
- **Automatic BUSY, INTRQ**
- **16 byte FIFO to improve throughput**
- **Automatic command decoding of write, write buffer and format commands**
- **Automatic update of the host task file registers in both LBA mode and Cyl/Hd/Sec mode**
- **Power-down IO pins**

(continued)

8

## BLOCK DIAGRAM



# SSI 32C9342
# PCMCIA Combo Controller with Reed Solomon, 48 Mbit/s

## FEATURES (continued)

BUFFER MANAGER:

- Supports Buffer RAM throughput up to:
  5V: 20 MByte/sec for SRAM and 17.2 MByte/sec for DRAM (with 40MHz SYSCLK)
  3.3V: 15 MByte/sec for SRAM and 12MByte/sec for DRAM (with 30 MHz SYSCLK)
- Programmable microprocesssor scratch pad area
- Auto data streaming capability
- Supports Multiple sector host data transfer
- Supports up to 1M byte DRAM and up to 256K SRAM
- Supports variable DRAM and SRAM timings and sizes
- Reload transfer counter and host address pointers
- Supports page mode DRAM access
- Programmable DRAM page mode burst length
- Programmable DRAM refresh period
- Separate host, disk, and microprocessor buffer RAM address pointers
- Provides protection logic for buffer data allowing simultaneous host and disk accesses to the same buffer segment.

DISK FORMATTER:

- Advanced sequencer organized in 31 x 5 bytes
- Advanced branch and interrupt logic
- Defect management support
- Supports multiple-sector data transfers
- NRZ byte synchronization time out timer
- Three-index counter providing limit of search and retry
- 8-byte stack for header information storage
- 16-byte disk data FIFO
- Sector header or microprocessor-based split data field processing logic supporting embedded servo and zone-bit recording
- Supports variable data field length
- Disk transfer rate up to 48 Mbit/s second NRZ
- Power Down Mode

MICROPROCESSOR INTERFACE:

- High speed internal register access
- Programmable wait state insertion
- Supports both Intel and Motorola type microprocessers

ERROR CORRECTION LOGIC:

- Enhanced 16-bit CRC polynomial with one order of magnitude better burst error detection than CCITT-CRC16
- Non-interleaved 88-bit Reed Solomon Code of degree 8 operation on 10-bit symbols
- Automatic on-the-fly in-buffer error correction
- Selectable on-the-fly error correction span of 11 or 31 bits signal burst
- Calculation of buffer offsets and masks for on-the-fly ECC within one half of a sector time
- On the fly in-buffer correction accomplished in no more than 5 buffer reads and writes through an independent channel
- Capable of correcting by software four 10-bit symbols in error
- Guaranteed to correct by software one 31-bit burst or two 11-bit bursts
- Detects up to one 51-bit burst or three 11-bit bursts

OTHERS:

- Automatic power supply level detection circuit
- JEDEC conformant 3.3V specification
- TTL-Level compatible input receivers at 3.3V or 5V
- Avalable in 120-pin surface mount TQFP

## FUNCTIONAL DESCRIPTION

The SSI 32C9342 is capable of operating in either a 3.3 volt or 5 volt environment. In addition, the SSI 32C9342 can operate in a mixed voltage environment with the host interface operating in a 5 volt environment and the remainder of its interfaces operating in a 3.3 environment. This allows a drive designed to operate on 3.3 volts to interface with a host which is operating on 5 volts.

The SSI 32C9342 contains the following four major functional blocks:

Microprocessor Interface

PCMCIA/ATA Interface

Disk Formatter

Buffer Manager

The Microprocessor Interface allows the local microprocessor access to all of the SSI 32C9342 internal control registers and any location within the buffer memory. The microprocessor, by writing and reading the internal registers, can control all activities of the SSI 32C9342. The microprocessor can elect to perform host and/or disk operations directly, or it can enable the advanced features of the SSI 32C9342 which can perform these operations automatically.

The PCMCIA/ATA Interface block can interface with PCMCIA interface as a PCMCIA/ATA device or with a PC AT bus. The SSI 32C9342 has on-board sensing logic to help determine whether it is operating in either the PCMCIA or ATA mode. The interface includes 16 mA (24 mA @5V) drivers allowing for direct connection of the SSI 32C9342 to either the PCMCIA or PC AT bus. The interface is highly automated, capable of performing multiple block transfers without micro-controller involvement. The PCMCIA/ATA block interfaces directly with the Buffer Manager via an internal speed matching FIFO. This FIFO, the bandwidth capabilities of the Buffer Manager, plus the advanced features of the PCMCIA/ATA Interface guarantee sustained full speed transfers.

The Disk Formatter performs the serialization and deserialization of data. It provides all of the necessary functions to control track formatting, header search, and the reading and writing of data. The heart of the Disk Formatter is an advanced programmable sequencer. The sequencer can contain 31 instructions, each of which is 5 bytes (40 bits) in width. The width of the instructions allows for sophisticated branching techniques which increase the flexibility and power of the sequencer. The flexible disk interface can be configured through a wide range of capabilities. This allows the SSI 32C9342 to interface with nearly any read/write channel and allows the user of the SSI 32C9342 to select the read/write channel best suited to the device. Of course, by selecting the SSI 32C9342 controller and the SSI 32P4342 Read Channel with 1,7 ENDEC, you are guaranteed a problem free interface.

Within the Disk Formatter are the ECC generator/checker and ECC corrector. The generator/checker provides the ability to generate or check a 32 bit ECC for headers and an 88 bit Reed Solomon code for data. If the checker detects an error in an 88 bit Reed Solomon data field, the syndrome information is transferred into the corrector. The corrector then performs the necessary operations to determine if the error was correctable and, if it was correctable, the corrector interfaces directly with the buffer controller and performs the correction automatically. The corrector performs its correction within one half of a sector. This guarantees that the corrector will always be available to correct the next sector if necessary.

As its name implies, the Buffer Manager manages the data buffer of the controller. The Buffer Manager can support either SRAM or DRAM. When configured to operate with DRAM, the Buffer Manager automatically performs necessary refresh cycles. The buffer manager creates all of the necessary timing and control signals for a wide range of memory types and speeds. Besides interfacing with the buffer memory, the Buffer Manager interfaces with the ATA Interface block, the Disk Formatter block, the ECC corrector and the microprocessor. If more than one of these devices requires access to the buffer memory, the Buffer Manager arbitrates the requests automatically. The Buffer Manager of the SSI 32C9342 can sustain ATA operations at the rate of 3 (6 @ 5V) megawords per second, Disk Formatter operations at 48 megabits per second and still has sufficient bandwidth left to handle on-the-fly ECC corrections and microprocessor accesses without degrading performance on any of the interfaces.

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# PCMCIA Combo Controller with Reed Solomon, 48 Mbit/s

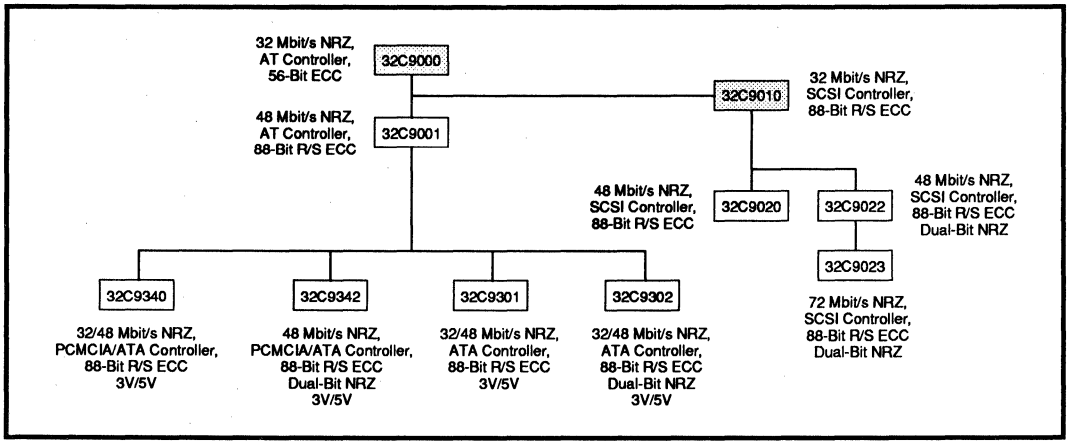


**FIGURE 1: Silicon Systems's Disk Controller Chip Hierarchy**

## PIN DESCRIPTION

I = input, O = output; Z = tri-state output, OD = open drain output. All unused inputs must be tied to the inactive state to VCC or GND, respectively.

### BUFFER MANAGER INTERFACE

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| BA17/$\overline{CAS}$ | O | Buffer Memory Address 17/ Column Address Strobe: This signal is used for addressing the buffer memory in SRAM mode or as the column address strobe in DRAM mode. |
| BA16/$\overline{RAS}$ | O | Buffer Memory Address 16/Row Address Strobe: This signal is used for addressing the buffer memory in SRAM mode or as the row address strobe in DRAM mode. |
| $\overline{MOE}$/$\overline{MS}$ | O | Memory Output Enable/Memory Select: When configured as $\overline{MOE}$, this signal is active during buffer memory reads. When configured as $\overline{MS}$ this signal is active during both buffer memory reads and buffer memory writes. This timing of the $\overline{MS}$ signal follows that of the address pins. |
| $\overline{WE}$ | O | Write Enable: This signal is asserted low when a buffer memory write operation is active in both SRAM and DRAM modes. |
| SYSCLK | I | System Clock: This is the clock input that is used to generate buffer memory access cycles. |
| BD (7:0) | I/O | Buffer Memory Data Bus: These eight signals are bits 7-0 of the 8-bit parallel data lines to/from the buffer memory. Note that BD6 is used to select between the Intel and Motorola-style microprocessor interfaces. IF BD6 is externally pulled up when $\overline{RST}$ is asserted, Intel mode is used; if BD6 is externally pulled down when $\overline{RST}$ is asserted, Motorola mode is used. |
| BA (15.0) | | Buffer Memory Address Lines: These are signals 15-0 for addressing the buffer memory. |

**MICROPROCESSOR INTERFACE**

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| $\overline{DINT}$ | O, OD, Z | Interrupt: This signal is an interrupt line to the microprocessor. It is the combined interrupt line of the disk side and host side interrupts when pin RDY/$\overline{HINT}$ is programmed as Ready; otherwise it only signals the occurrence of disk side interrupt events. This signal is programmable for either a push-pull or open-drain output circuit. This signal powers up in the high-Z state. |
| CS | I | Chip Select: This signal must be asserted high for all microprocessor accesses to the registers of this chip. |
| $\overline{WR}$/R/$\overline{W}$ | I | Write Strobe/Read/Write: When the Intel bus control interface is selected, this signal acts as the $\overline{WR}$ signal. When the write strobe signal is asserted low and the CS signal is asserted high, the data on the AD bus will be written to the register.<br>When the Motorola bus control interface is selected, this signal acts as the R/$\overline{W}$ signal. A high on this input along with the $\overline{RD}$/DS signal asserted and the CS signal asserted high indicates a read operation. A low on this input along with the $\overline{RD}$/DS signal asserted and the CS signal asserted high indicates a write operation. |
| $\overline{RD}$/DS | I | Read Strobe/Data Strobe: When the Intel bus control interface is selected, this signal acts as the $\overline{RD}$ signal. When the read strobe signal is asserted low and the CS signal is asserted high, the data from the specified register will be driven onto the AD bus.<br>When Motorola bus control interface is selected the signal acts as the DS signal. A high on the R/$\overline{W}$ signal along with this signal asserted and the CS signal asserted high indicates a read operation. A low on the R/$\overline{W}$ signal along with this signal asserted and the CS signal asserted high indicates a write operation. Note that when non-multiplexed address and data buses are used, this pin configured as $\overline{DS}$ (active low). |
| RDY/$\overline{HINT}$ | O | Ready/Host Side Interrupt: When programmed as the ready function, this signal is deasserted low for the microprocessor to insert wait states to allow time for the chip to respond to the access.<br>When programmed as host side interrupt, this pin interrupts the microprocessor when there is an AT host related interrupt event. The interrupt signal is programmable for either a push-pull or open-drain output circuit. This signal powers up as the "ready" function. |
| AD (7:0) | I/O | Microprocessor Address/Data Bus: These signals are bidirectional multiplexed microprocessor address/data lines when the chip is configured in the multiplexed bus mode. Otherwise these signals are the bidirectional data lines. |
| MA (7:0) | I/O | Microprocessor Address/Bus: These signals are nonmultiplexed address input or demultiplexed address output lines. |

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## PIN DESCRIPTION (continued)

### MICROPROCESSOR INTERFACE (continued)

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| ALE | I | Address Latch Enable/Intel or Motorola Mode Select: If this input is tied high after reset (i.e., after $\overline{RST}$ has been asserted and released), the microprocessor interface is configured for Motorola mode with DS active high. If this input is tied low after reset, the microprocessor interface is configured for Motorola mode with $\overline{DS}$ active low. If this input makes a low to high transition after reset, then the microprocessor interface is configured for Intel mode. In this case, this pin functions as the address latch enable, and the latched address is output on the MA(7:0) pins. |
| $\overline{RST}$ | I | Reset: An asserted low input generates a component reset that stops all operations within the chip and deasserts all output signals. All input/output signals are set to the high-Z state. |

### DISK FORMATTER INTERFACE

| | | |
|---|---|---|
| INPUT/OUTPUT | I/O | Disk Sequencer Input/Output: When configured as Input, this signal may be used to synchronize the disk sequencer to an external event. When configured as Output, this pin is controlled by bit 2 of the disk sequencer's control field. When $\overline{RST}$ is asserted, this pin as configured as Input. |
| INDEX | I | Index: This is the input for the Index pulse received from the disk drive. |
| $\overline{AMD}$/SECTOR | I/O | Address Mark Detect/Sector: In hard sector mode, this is the input for the sector pulse from the disk drive. In soft sector mode, a low-level input during a read indicates an address mark was detected. |
| RG | O | Read Gate: This signal is asserted when a disk read operation is in progress and the NRZ data is input to the chip. |
| WG | O | Write Gate: This signal is used to enable the writing of NRZ data out to the storage device during a write operation. |
| RRCLK | I | Read Reference Clock: This signal input clocks the NRZ data. |
| NRZ0 | I/O | NRZ Bit 0: This signal is the read data input from this disk drive when the read gate signal is asserted; it is the write data output to the disk drive when the write gate signal is asserted. This pin is used for the least significant bit in dual bit NRZ mode; it is used for the serial data stream in signal bit NRZ mode. |
| NRZ1 | I/O | NRZ Bit 1: This signal is the read data input from the disk drive when the read gate signal is asserted; it is the write data output to the disk drive when the write gate signal is asserted. This pin is used for the most significant bit in dual bit NRZ mode; it is not used in single bit NRZ mode. |
| WCLK | O | Write Clock: This signal clocks the NRZ data out of the chip during a write. |

**HOST INTERFACE PINS**

| | | |
|---|---|---|
| $\overline{IOCS16}$ | O, OD | 16-Bit Data Select: This signal indicates that a 16-bit sector buffer transfer is active on the host data bus. This pin is open-drain in ATA mode, but push-pull in PCMCIA mode. This pin is not driven while $\overline{RST}$ is asserted, and remains so until the interface mode (PCMCIA or ATA) is determined. |
| R/$\overline{BUSY}$/IRQ | O, Z | Ready/$\overline{BUSY}$/Host Interrupt Request: In PCMCIA mode, this pin is the Ready/$\overline{BUSY}$ signal when configured with a memory interface. In ATA mode, or in PCMCIA mode when configured with an I/O interface, this pin is the host interrupt request, and is asserted to indicate to the host that the controller needs attention. As an interrupt request, this pin is active high in ATA mode, but active low in PCMCIA mode. This pin is always driven in PCMCIA mode, but will be tri-stated when the drive is not selected or interrupts are not enabled in ATA mode. This pin is driven low while $\overline{RST}$ is asserted, and remains so until the interface mode (PCMCIA or ATA) is determined. If PCMCIA mode is selected after reset, the chip is configured with a memory interface, and this pin will reflect the status of the BUSY bit in the Drive Status Register. |
| A(8:0), A10 | I | Host Address Lines: The host address lines A(8:0) and A10 are used to access the various PC/AT control, status, and data registers. |
| A9/$\overline{HCS1}$ | I | A9/$\overline{HCS1}$: This is a multiplexed input pin. When in PCMCIA mode, or when register 4CH, bit 3 is reset, this is host address line A9. When register 4CH, bit 3 is set in ATA mode, this is Host chip select 1 (active low). |
| $\overline{CE0}$/$\overline{HCS0}$ | I | Host Chip Select 0/Card Enable 1: This signal when low, selects access to the control, status, and data registers. It is configured as $\overline{HCS0}$ in ATA mode, and as $\overline{CE1}$ in PCMCIA mode. |
| $\overline{WAIT}$/IOCHRDY | O, Z | Wait/I/O Channel Ready: This signal is asserted low to extend host transfer cycles when the controller is not ready to respond. This pin is always driven in PCMCIA mode, but will be tri-stated when a read or write is not in progress in ATA mode. This pin is tri-state while $\overline{RST}$ is asserted, and remains so until the interface mode (PCMCIA or ATA) is determined. |
| $\overline{INPACK}$/DREQ | O, Z | Input Acknowledge/DMA Request: In PCMCIA mode, this pin is configured as $\overline{INPACK}$, and is asserted when a valid address and chip select are present. In ATA mode, this pin is configured as the DMA request signal, and is used during DMA transfer between the host and the controller. In ATA mode, this pin is tri-stated when DMA transfers are not enabled. This pin is tri-state while $\overline{RST}$ is asserted, and remains so until the interface mode (PCMCIA or ATA) is determined. |
| $\overline{REG}$/$\overline{DACK}$ | I | Register Select and I/O $\overline{ENABLE}$/DMA $\overline{ACKNOWLEDGE}$: In PCMCIA mode, this pin is configured as $\overline{REG}$, and selects the attribute memory space or I/O space when asserted. In ATA mode, this pin is configured as $\overline{DACK}$, and is used as the DMA acknowledge signal during DMA data transfers. |
| $\overline{IOR}$ | I | I/O Read: Asserted by the host during a host I/O read operation. When asserted with a valid address and chip selects, status or data is enabled onto the host data bus. |
| $\overline{IOW}$ | I | I/O Write: Asserted by the host during a host I/O write operation. When asserted with a valid address and chip selects, data from the host data bus is strobed into the controller. |

## PIN DESCRIPTION (continued)

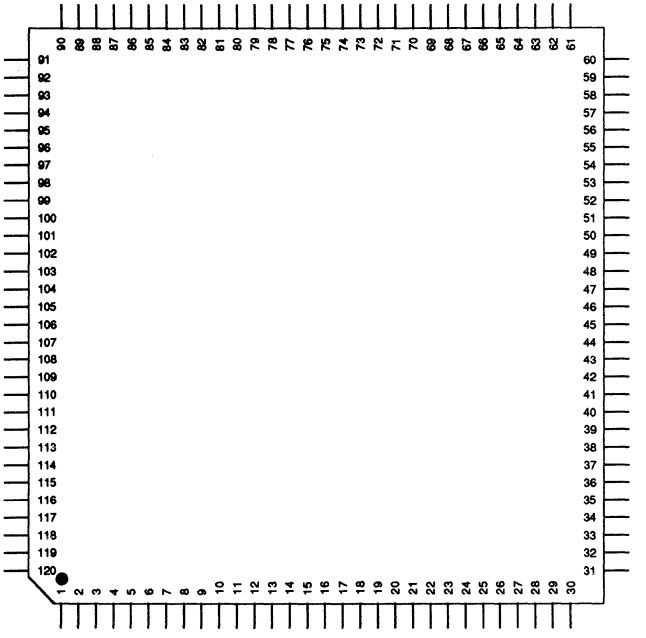
### HOST INTERFACE PINS (continued)

| | | |
|---|---|---|
| HRESET/$\overline{\text{HRESET}}$ | I | Host Reset: This signal, when active, initializes the control/status registers and stops any command in process. It is active low in ATA mode, but active high in PCMCIA mode. |
| HDB(15:0) | I/O | Host Data Bus: This bus is used to transfer data and status between the host and the controller. These pins are not driven while $\overline{\text{RST}}$ is asserted, and remain so until the interface mode (PCMCIA or ATA) is determined. |
| $\overline{\text{CE2}}$ | I | Card Enable 2: This signal, when low, selects access to the control, status, and data registers and may enable use of the upper half of the data bus. It is used only in PCMCIA mode. |
| $\overline{\text{HOE}}$/$\overline{\text{SELATA}}$ | I | Output Enable/Select ATA Mode: To determine which host interface to use, this pin is sampled starting at least 8 µs after $\overline{\text{RST}}$ is deasserted, and continuing until at least 25 µs after $\overline{\text{RST}}$ is deasserted. If this pin is high at any time during this sampling period, the interface will immediately be configured for PCMCIA mode, and the sampling will end. If the pin remains low throughout the sampling period, the interface will be configured for ATA mode. Once in PCMCIA mode, this pin is configured as output enable ($\overline{\text{HOE}}$), and is asserted by the host during a common memory or attribute memory read. When asserted with a valid address and chip select, data is enabled onto the host data bus. In ATA mode, this signal is ignored. |
| $\overline{\text{HWE}}$ | I | Write Enable: In PCMCIA mode, this signal is asserted by the host during a common memory or attribute memory write. When asserted with a valid address and chip select, data from the host data bus is strobed into the controller. In ATA mode, this signal is ignored. |
| $\overline{\text{STSCHG}}$/$\overline{\text{PDIAG}}$ | I, O, | Status Changed/Passed Diagnostics: In PCMCIA mode, this pin is used as the Status Changed output. In ATA mode, this pin is used as the Passed Diagnostics signal and may be an input or an open-drain output. This pin is tri-state while $\overline{\text{RST}}$ is asserted, and remains so until the interface mode (PCMCIA or ATA) is determined. |
| $\overline{\text{SPKR}}$/$\overline{\text{DASP}}$ | I/OD | Speaker/Drive Active-Slave Present: In PCMCIA mode, this pin is used as the Speaker pin, and is a push-pull output. In ATA mode, this pin is used as the Drive Active/Slave Present signal, and is an input or an open-drain output. In ATA mode, this pin is used for Master/Slave drive communications and/or for driving an LED. This pin is tri-state while $\overline{\text{RST}}$ is asserted, and remains so until the interface mode (PCMCIA or ATA) is determined. |

## PACKAGE PIN DESIGNATIONS

(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.




**120-Lead TQFP**

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**Target Specification:** The target specification is intended as an initial disclosure of specification goals for the product. The specifications are based on design goals, subject to change and are not guaranteed.



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**Notes:**

Section 9

# FLOPPY DISK DRIVE CIRCUITS

silicon systems®
A TDK Group Company

# SSI 34P553/5531
## Pulse Detector & Data Synchronizer

December 1992

## DESCRIPTION

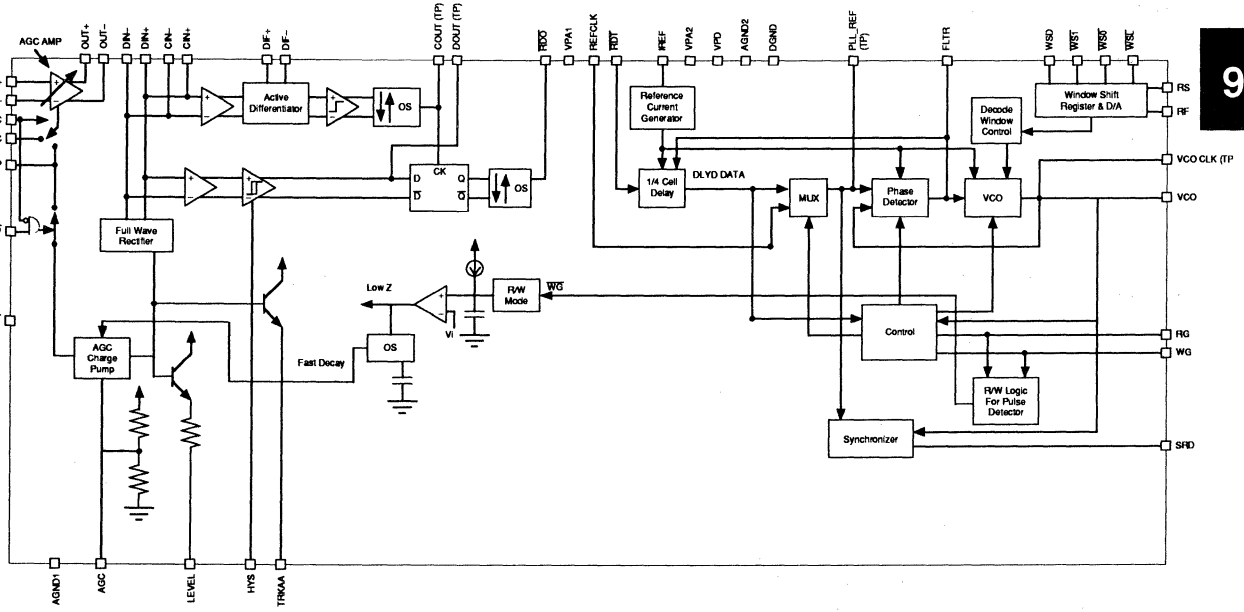
The SSI 34P553/5531 is a low power, high performance Pulse Detection, Data Synchronization combination device. This device is designed for use in low power applications requiring +5V only power supplies. The pulse detection portion of this device detects and validates amplitude peaks in the output from a disk drive read amplifier. The data synchronization portion is an MFM and 1, 7 data synchronizer with window shift capability. The SSI 34P553/5531 achieves low system operating power two ways, with a low operating power (+5V only design) and with a power down mode. The power down mode is a complete shutdown or sleep mode. The SSI 34P553/5531 is available in a 52-lead fine pitch QFP package.

The 34P5531 is the same device, but with separate CIN+, DIN+ inputs, for use with active filters such as the SSI 32F8030.

## FEATURES

- **Highly Integrated Pulse Detector and Data Synchronizer**
- **+5V only Power Supplies**
- **790 mW max. power**
- **Low Pulse Pairing**
- **0.6-1.6 Mbit/s operation**

## BLOCK DIAGRAM






CAUTION: Use handling procedures necessary for a static sensitive component.

## CIRCUIT OPERATION

### PULSE DETECTOR SECTION

#### READ MODE

The SSI 34P553/5531 enters into the read mode when the WG pin is pulled low. In the read mode, the SSI 34P553/5531 provides amplification and pulse level qualification of the signal applied to the input pins of the AGC amplifier.

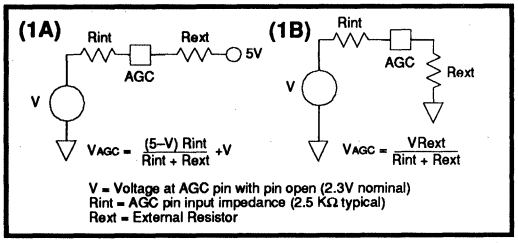
#### AGC AMPLIFIER

An amplified head output signal is AC coupled to the IN+ and IN- pins of the AGC amplifier. To control the gain of the AGC amplifier, the signal at the DIN± pins is full-wave rectified and amplified. The resulting voltage is compared to the voltage level present at the AGC pin. If the voltage level is higher than the AGC pin reference level, the SSI 34P553/5531 will enter into an attack mode. If it is lower than the AGC pin voltage the device will enter into a decay mode.

**Attack Mode.** The SSI 34P553/5531 contains a dual rate attack charge pump that is controlled by the instantaneous level at DIN±. When the voltage from the full wave rectifier exceeds the AGC pin voltage by greater than 125%, a fast attack mode is entered. During fast attack, 1.4 mA of current is supplied to the network on the BYP pin. When the full wave rectifier voltage exceeds the AGC pin voltage by 100 to 125%, the slow attack mode is entered. During slow attack the charge current supplied to the BYP pin is 0.18 mA. This dual rate charge pump allows the AGC to recover rapidly during write to read transitions while minimizing distortion once the AGC amplitude is within range.

**Decay Mode.** Two internally controlled decay modes are provided by the SSI 34P553/5531. Upon a switch to write mode, the device holds the gain at its last value and the AGC inputs are switched to low impedance. When the device is switched back from write to read, the gain remains held and the AGC inputs remain in a low impedance state for 0.9 µs. At this time, if the new gain required is more than the held value the device enters into the decay mode. A fast decay current of 0.12 mA is automatically switched on for a period of 0.9 µs. After 0.9 µs the device will sink a steady state slow decay current of 4.5 µA (reference Figure 7.)

**AGC Level Control.** The AGC level is controlled by the voltage presented on the AGC pin. The AGC pin is internally biased at approximately 2.3V which sets the signal at the DIN± pins to 1.0 Vpp under nominal conditions. The voltage at the AGC pin can be externally controlled by connecting a resistor between the AGC pin and either VPA1 or AGND1. When a resistor is connected from AGC to VPA1 the voltage on the AGC pin can be increased (Figure 1a). When a resistor is connected from AGC to AGND1 the voltage on the AGC pin can be decreased (Figure 1b). The new DIN± input target level is nominally (VAGC -0.75)•0.64 Vpp. The output of the AGC amplifier has a maximum swing of 3.0 Vpp that can be controlled using the AGC pin. The 3.0 Vpp swing supports the use of external filters that have up to 6 dB of loss. A multi-pole Bessel filter is typically used for its linear phase or constant group delay characteristics.




**FIGURES 1A & 1B: AGC Voltage**

The gain of the AGC amplifier is directly controlled by the voltage at the BYP pin (VBYP) or the VEGC pin as shown in Figure 2. The AGC amplifier has open collector outputs that can sink up to 4.0 mA of current. For correct operation over the gain range each output should be pulled up to VPAI through a 340 Ω resistor as shown in Figure 3.

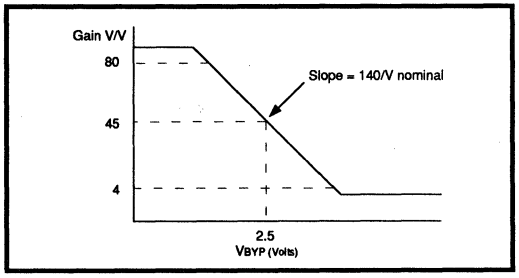



**FIGURE 2: AGC Gain**

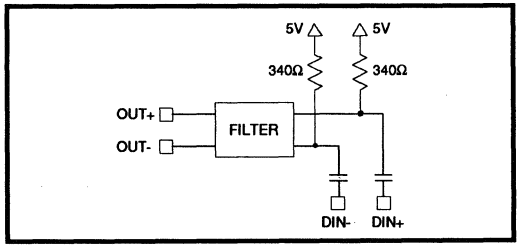



**FIGURE 3: AGC Filter**

## PULSE QUALIFICATION

The SSI 34P553/5531 uses both amplitude and time qualification to digitize the incoming data pulses. In the amplitude channel the signal is sent to a hysteresis comparator. A hysteresis trip level is externally set such that only pulses that exceed the required signal level will trip the comparator. This prevents false qualification of baseband noise. The hysteresis trip level can be either a fixed level or a fraction of the DIN +/- voltage level.

**Hysteresis Level.** A fixed hysteresis level can be set by applying a DC voltage to the HYS pin. This is a simple method for hysteresis control but it does not compensate well for internal variances from device to device. A more effective approach is to feed forward a percentage of the voltage level at the DIN± pins. This approach is accomplished by using a filter/divider network between the LEVEL and HYS pins. The LEVEL pin output voltage is a rectified and amplified version of the voltage level applied to the DIN± pins. The gain in this circuit is set so that a 1 Vpp signal applied to DIN+/- will result in a 1 Vpk (typical) output signal at the LEVEL pin. An external capacitor to AGND1 should be used on the LEVEL pin to maintain a DC level. An external voltage divider can be connected between the LEVEL pin and AGND1 to provide the hysteresis programming voltage to the HYS pin. The HYS pin voltage determines the percentage of the DIN+/- input signal that will trip the hysteresis comparator of the SSI 34P553/5531. The transfer function of the HYS pin for setting the threshold percentage is:

$$\text{Hysteresis Threshold} = 0.41 \times \text{VHYS}$$

where VHYS is the voltage applied to the HYS pin. For example, with a 1.0 Vpp signal at DIN+/- the LEVEL pin output will be 1.0 Vpk. Using a 50% resistor divider between LEVEL and AGND1 would result in a HYS pin voltage of 0.5V and that would produce a hysteresis threshold of 0.20V in both the positive and negative direction. This translates to a hysteresis threshold percentage of 40% of DIN+/-.

Because the SSI 34P553/5531 circuits are internally biased to the same levels, the technique of feeding forward the LEVEL pin voltage helps to offset process related internal tolerance variations. In addition, the feed forward technique speeds up transient recovery by allowing qualification of input pulses while the AGC is still settling, such as during write to read recovery or head change recovery. Care should be taken in selecting the hysteresis level time constant so that pattern induced low amplitude signals are not missed. The SSI 34P553/5531 has a built in minimum of ±50 mV threshold for level qualification even when the HYS pin is grounded. This prevents false triggering due to baseband noise during a DC erase gap.

The outputs of the hysteresis comparator are the "D" inputs of the D-type flip-flop. One side of the hysteresis comparator outputs is provided as the DOUT pin test point. The DOUT pin can be monitored by connecting a 3 to 6 kΩ resistor to AGND2. When the DOUT pin is not used, it can be pulled up to VPA2 to save power.

In the time channel the signal is differentiated to transform signal peaks to zero crossings which are detected and used to trigger a bi-directional one-shot. The one-shot output pulses are used as the clock input of the D flip-flop. The COUT pin provides the one-shot output for test purposes. It also requires an external 3 to 6 KΩ pull-down resistor for testing.

The differentiator function is accomplished by an external network between the DIF+ and DIF- pins. The transfer function from DIN± to the comparator input (not DIF±) is:

$$Av = \frac{-2000Cs}{LCs^2 + C(R+92)s + 1}$$

where: C, L, R are external passive components
$20\ pF < C < 500\ pF$
$s = j\omega = j2\pi f$

During normal operation, the time channel clocks the D flip-flop on every positive and negative peak of the DIN± input. The D input to the flip-flop only changes state when the DIN± input exceeds the hysteresis comparator threshold opposite in polarity to the previous threshold exceeding peak.

The time channel, then, determines signal peak timing and the amplitude channel determines validity by blocking signal peaks that do not exceed the hysteresis comparator threshold. The delays in each of these channels to the D flip-flop inputs are well matched. The D flip-flop output triggers a one-shot that sets the $\overline{RDO}$ output pulse width.

### WRITE MODE

In Write Mode the SSI 34P553/5531 Pulse Detector section is disabled and preset for the following Read Mode. The digital circuitry is disabled, ($\overline{RDO}$ pin held high), the input AGC amplifier gain is held at its previous value and the AGC amplifier input impedance is reduced.

Holding the AGC amplifier gain and reducing input impedance shortens system Write to Read recovery times.

The lowered input impedance improves settling time by reducing the time constant of the network between the SSI 34P553/5531 and a head preamplifier such as the SSI 32R1200R. Write to read timing is controlled to maintain the reduced impedance for 0.9 µs before the AGC circuitry is activated. Coupling capacitors should be chosen with as low a value as possible consistent with adequate bandwidth to allow more rapid settling.

### DATA SYNCHRONIZER SECTION

The SSI 34P553/5531 is designed to perform data synchronization in rotating memory systems which utilize a 1, 7 RLL and MFM encoding format. In the Read Mode the SSI 34P553/5531 performs Data Synchronization. The interface electronics and architecture of the SSI 34P553/5531 have been optimized for use as a companion device to the WD 42C22 controllers.

The SSI 34P553/5531 can operate with data rates ranging from .6 to 1.6 Mbit/s. This data rate is established by a single 1% external resistor, RR, connected from pin IREF to VPA2. This resistor establishes a reference current which sets the VCO center frequency, the phase detector gain, and the 1/4 cell delay. The value of this resistor is given by:

$$RR = \frac{5.97}{DR} - 1.78(k\Omega) \text{ MFM}$$

$$RR = \frac{7.96}{DR} - 1.78(k\Omega) \text{ 1,7}$$

Where: DR = Data Rate in Mbit/s

An external TTL compatible reference may be applied to REFCLK

The SSI 34P553/5531 employs a Dual Mode Phase Detector: Harmonic in the Read Mode and Non-Harmonic in Write and Idle Modes. In the Read Mode the Harmonic Phase Detector updates the PLL with each occurrence of a DLYD DATA pulse. In the Write and Idle Modes the Non-Harmonic Phase Detector is continuously enabled, thus maintaining both phase and frequency lock. By acquiring both phase and frequency lock to the crystal reference oscillator and utilizing a zero phase restart technique, false lock to DLYD DATA is eliminated.

The phase detector incorporates a charge pump in order to drive the loop filter directly. The polarity and width of the output current pulses correspond to the direction and magnitude of the phase error. Figure 4 depicts the average output current as function of the input phase error (relative to the VCO period.)

The READ GATE (RG), and WRITE GATE (WG), inputs control the device mode as described in Table 1. RG is an asynchrouous input and may be initiated or terminated at any position on the disk. WG is also an asynchronous input, but should not be terminated prior to the last output Write Data pulse.

### READ OPERATION

The Data Synchronizer utilizes a fully integrated fast acquisition PLL to accurately develp the decode window. Read Gate, RG, initiates the PLL locking sequence and selects the PLL reference input; a high level (Read Mode) selects the Read Data input and low level selects the crystal reference oscillator.

In the Read Mode the rising edge of DLYD DATA enables the Phase Detector while the falling edge is phase compared to the rising edge of the VCO. As depicted in Figure 5, DLYD DATA is a 1/4 cell wide (TVCO/2) pulse whose leading edge is defined by the leading edge of Read Data. VCO is generated from the rising edges of the VCO clock. By utilizing a fully integrated symmetrical VCO running at the code rate, VCO is insured to be accurate and centered symmetrically about the falling edges of DLYD DATA. The accuracy of the 1/4 cell delay only affects the retrace angle of the phase detector and does not influence the accuracy of VCO.

Shifting the symmetry of the VCO clock effectively shifts the relative position of the DLYD DATA pulse within the decode window. This powerful capability easily facilitates defect mappings, automatic calibration, window margin testing, error recovery, and systematic error cancellation. For enhanced disk drive testability and error recovery, decode window control is provided via a µP port ($\overline{WSL}$, WSD, $\overline{WS0}$, $\overline{WS1}$) as described in Table 2. In application not utilizing this feature, $\overline{WSL}$ should be left open or connected to VPA2, while WSD, $\overline{WS0}$, and $\overline{WS1}$ can be left open.

Window shifts in the range of ±5% to ±20% of TVCO are easily programmed by latching the appropriate control word into the Window Shift Register with the WSL pin. Shifts in the positive or negative directions result in early or late decode windows respectively, as depicted in Figure 6. Additionally, for small systematic error cancellation, a resistor, R, connected from either RS (Early) or RF (Late) to ground will provide analog control over the decode window. The magnitude of this shift, TSA is determined by:

$$TSA = 0.25\,TVCO\left(1 - \frac{3260+R}{5950+R}\right)$$

Where: R is in Ω

Pins RF and RS are intended to be used as a trim and should be restricted to ±3% window shifts. They can be used in conjunction with the digital control port.

In Non-Read Modes, the PLL is locked to REFCLK. This forces the VCO to run at a frequency which is very close to that required for tracking actual data and thus minimizes the associated frequency step during acquisition. When RG transitions, the VCO is stopped momentarily, then restarted in an accurate phase alignment with the next PLL reference input pulse. By minimizing the phase alignment in this manner, the acquisition time is substantially reduced.

### POWER DOWN MODE

A power down mode is provided to reduce power usage during the idle periods. Taking $\overline{\text{PDWN1}}$ low causes the device to go into complete shutdown.

### MODE CONTROL

The SSI 34P553/5531 circuit mode is controlled by the $\overline{\text{PDWN1}}$, $\overline{\text{HOLD}}$, RG, and WG pins as shown in Table 1.

**TABLE 1: Mode Control**

| WG | RG | $\overline{\text{HOLD}}$ | $\overline{\text{PDWN1}}$ | |
|---|---|---|---|---|
| 0 | 0 | 1 | 1 | Read Mode VCO Locked to XTAL |
| 0 | 1 | 1 | 1 | Read Mode VCO Locked to Read Data |
| 0 | X | 0 | 1 | Read Mode AGC gain held constant* |
| 1 | 0 | X | 1 | Write Mode AGC gain held constant*<br>Input impedance reduced |
| X | X | X | 0 | Power shutdown mode |

* AGC gain will drift at a rate determined by BYP capacitor and Hold mode leakage current.

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**TABLE 2: Decode Window Symmetry Control**

| Ts, NOMINAL WINDOW SHIFT | WSD | $\overline{WS1}$ | $\overline{WS0}$ |
|---|---|---|---|
| +TS3 | 0 | 0 | 0 |
| +TS2 | 0 | 0 | 1 |
| +TS1 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 |
| -TS3 | 1 | 0 | 0 |
| -TS2 | 1 | 0 | 1 |
| -TS1 | 1 | 1 | 0 |
| 0 | 1 | 1 | 1 |

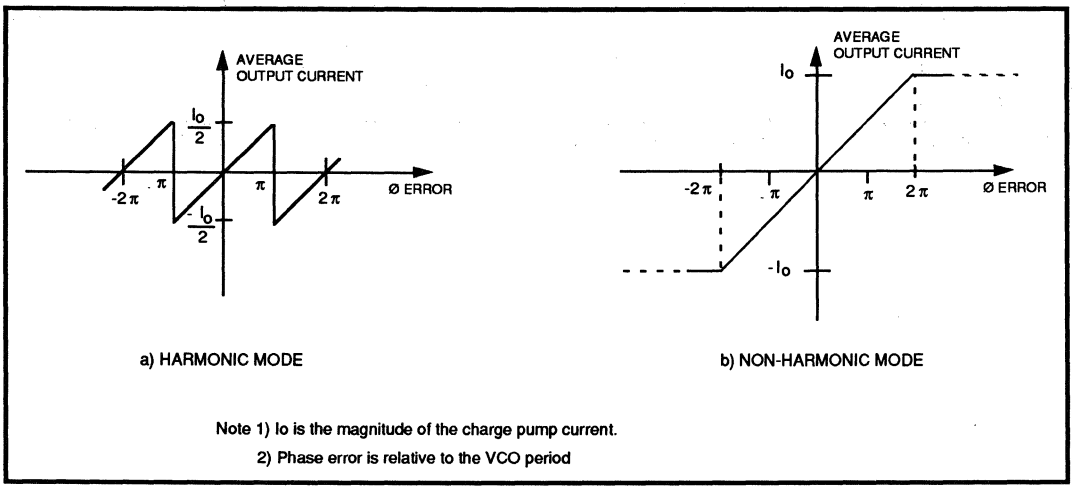


**FIGURE 4: Phase Detector Transfer Function**

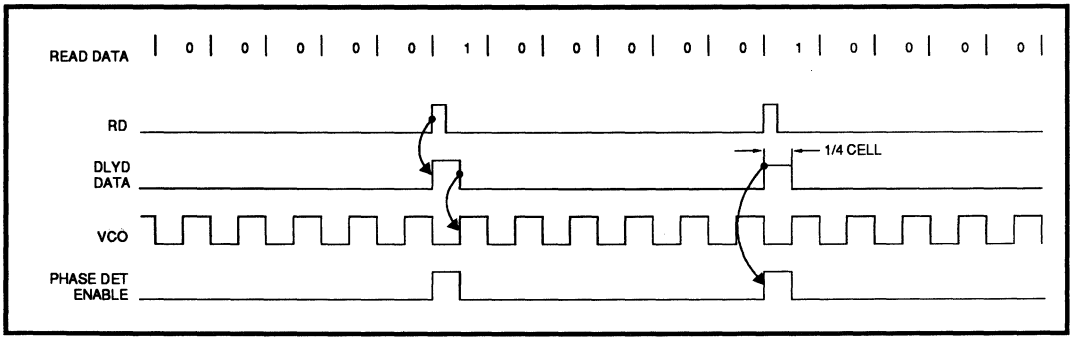


**FIGURE 5: Data Synchronization Waveform Diagram**



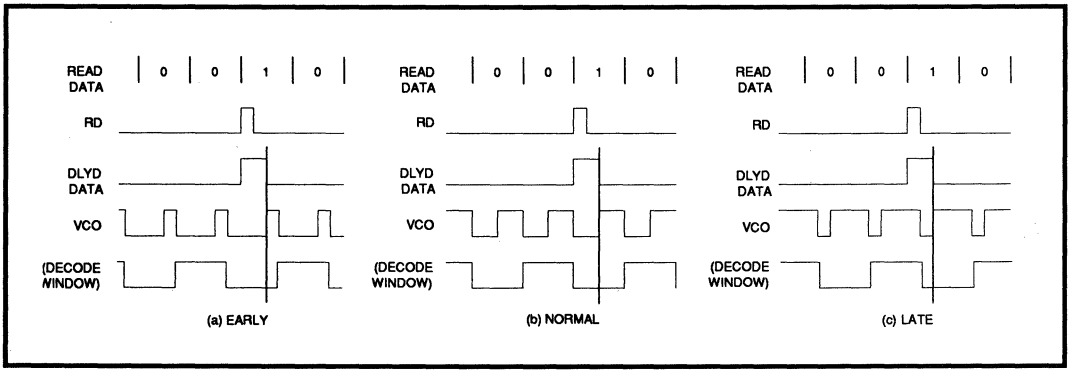


**FIGURE 6: Decode Window**

## PIN DESCRIPTION

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| VPA1 | I | Analog (+5V) power supply for pulse detector. |
| AGND1 | I | Analog ground pin for pulse detector block. |
| VPA2 | I | Analog (+5V) supply pin for data synchronizer block. |
| AGND2 | I | Analog ground pin for data synchronizer block. |
| VPD | I | Digital (+5V) power supply pin. |
| DGND | I | Digital ground pin. |
| IN+, IN– | I | Analog signal input pins. |
| OUT+, OUT– | O | Read path AGC Amplifier output pins. |
| DIN+, DIN– | I | Analog input to the hysteresis comparator, and differentiator. |
| CIN+, CIN– | I | Analog input to the clock comparator, differentiator. In the 34P553/5531, CIN+ is connected to DIN+, CIN– is connected to DIN–. |
| DIF+, DIF– | I/O | Pins for external differentiating network. |
| COUT | O | Test point for monitoring the flip-flop clock input. Pull down resistor required. |
| DOUT | O | Test point for monitoring the flip-flop D-input. Pull down resistor required. |
| BYP | I/O | An AGC timing capacitor or network is tied between this pin and AGND1. |
| AGC | I | Reference input voltage for the read data AGC loop. |
| LEVEL | O | Output from fullwave rectifier that may be used for input to the hysteresis comparator. |
| HYS | I | Hysteresis level setting input to the hysteresis comparator. |
| TRKAA | O | Full wave rectifier output. This output has the same DC level as the LEVEL pin, i.e., $\leq 0.3V$ with no AC signal and $\approx 1V_{OP}$ with a $1V_{PP}$ AC signal at DIN+/DIN-. |
| $\overline{\text{HOLD}}$ | I | TTL compatible pin that holds the AGC gain when pulled low. |
| EGC | I | External Gain Control. This is a TTL input pin that allows the AGC gain to be controlled by either BYP or the VEGC pin voltage. When AGE is high, the AGC gain is controlled by VEGC and the internal charge pump to BYP is disabled. |
| VEGC | I | The voltage at this pin is used to control the AGC gain when the EGC pin is held high. |
| $\overline{\text{RDO}}$ | O | Read Data Output. This is the TTL output from the pulse detector. This signal may be fed directly into the $\overline{\text{RDT}}$ input. |
| IREF | I | Timing program pin: the VCO center frequency, Phase Detector Gain and the 1/4 cell delay are a function of the current source into pin IREF. The current is set by an external resistor, RR connected from IREF to VPA2. |
| FLTR | I/O | Filter pin: the phase detector output and VCO input node. The loop filter is connected to this pin. |

## PIN DESCRIPTION (Continued)

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| SRD | O | Synchronized Read Data: read data that has been re-synchronized to VCO clock. |
| WSD | I | Window Symmetry Direction: controls the directions of the optional window symmetry shift. Pin WSD has an internal resistor pull-up. |
| $\overline{WS0}$ | I | Window symmetry control bit: a low level introduces a window shift of 5% TORC (read reference clock period) in the direction established by WSD pin. $\overline{WS0}$ has an internal resistor pull-up. |
| $\overline{WS1}$ | I | Window Symmetry Control bit: a low level introduces a window shift of 15% TORC (read reference clock period) in the direction established by WSD. A low level at both $\overline{WS0}$ and $\overline{WS1}$ will produce the sum of the two window shifts. Pin $\overline{WS1}$ has an internal resistor pull-up. |
| $\overline{WSL}$ | I | Window Symmetry Latch: used to latch the input window symmetry control bits WSD, $\overline{WS0}$, $\overline{WS1}$ into the internal DAC. An active low level latches the input bits. |
| RF, RS | I | WINDOW SYMMETRY ADJUST PINS: Provides analog control over the decode window symmetry; typically used to null out any window symmetry offset. A resistor connected from either RF or RS to AGND will provide magnitude and direction control. They can be used in conjunction with the digital control port WSD, $\overline{WS0}$, $\overline{WS1}$. |
| RG | I | Read gate: selects the PLL reference input and initiates the PLL synchronization sequence. A high level selects the internal RD± inputs. A low level selects the crystal reference oscillator, Pin RG has an internal resistor pullup. |
| WG | I | Write Gate: enables the write mode. Pin WG has an internal resistor pullup. |
| VCO CLK | O | VCO CLK: An open emitter ECL output test point. Two external resistors are required to perform this test. They should be removed during normal operation for reduced power dissipation. |
| $\overline{RDT}$ | I | Read Data input. This TTL input comes from the $\overline{RDO}$ output of the pulse detector. This signal is active low. |
| $\overline{PDWN1}$ | I | Power Down input. When this input is low, the chip enters low power mode. This pin has an internal pullup resistor, and may be left open or tied high if not used. |
| REF CLK | I | Reference Clock. This is a TTL input at the code rate that is used as the reference for the VCO in idle mode. |
| VCO | O | VCO output. This is the VCO signal converted to a TTL level. |
| PLL_REF | O | PLL Reference Test Point. In write and idle modes, this is the reference oscillator signal. In read mode, it is the delayed read data (DRD) signal. This is an ECL level output. PLL_REF can be compared to VCOCLK to see the window centering accuracy. |

## ELECTRICAL SPECIFICATIONS

Unless otherwise specified, 4.5V ≤ VPA 2 ≤ 5.5V, 25°C ≤ Tj ≤ 135°C, 1.2 MHz ≤ 1/TVCO ≤ 2.4 MHz.

### ABSOLUTE MAXIMUM RATINGS

Operation outside these rating limits may cause permanent damage to this device.

| PARAMETER | RATING |
|---|---|
| 5V Supply Voltage, VPA1, VPA2, VPD | 6.0 V |
| Pin Voltage (Analog pins) | -0.3 to VPA1, 2 + 0.3 V |
| Pin Voltage (All others) | -0.3 to VPD + 0.3 V or +12 mA |
| Storage Temperature | -65 to 150 °C |
| Lead Temperature (Soldering 10 sec.) | 260 °C |

### RECOMMENDED OPERATING CONDITIONS

Currents flowing into the chip are positive.

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Supply Voltage (VPA1, 2 & VPD) | | 4.5 | 5.0 | 5.5 | V |
| Tj Junction Temperature | | 25 | | 135 | °C |

### POWER SUPPLY

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| IVPA1, 2 Supply Current<br>IVPD | Outputs unloaded<br>$\overline{PDWN1}$= high or open | | 110 | 143 | mA |
| | $\overline{PDWN1}$ = low<br>Outputs unloaded | | 44 | 57 | mA |
| Pd Power dissipation | Ta = 25°C, outputs unloaded<br>$\overline{PDWN1}$= high or open | | 550 | 790 | mW |
| | $\overline{PDWN1}$ = low<br>Outputs unloaded | | 220 | 315 | mW |

**LOGIC SIGNALS**

| PARAMETER | CONDITION | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| VIL Input Low Voltage | | -0.3 | | 0.8 | V |
| VIH Input High Voltage | | 2.0 | | VCC+0.3 | V |
| IIL Input Low Current | VIL = 0.4V | 0.0 | | -0.4 | mA |
| IIL WG Input Low Current | VIL = 0.4V | 0.0 | | -0.8 | mA |
| IIH Input High Current | VIH = 2.4V | | | 100 | µA |
| VOL Output Low Voltage | IOL = 4.0 mA | | | 0.5 | V |
| VOH Output High Voltage | IOH = -400 µA | 2.4 | | | V |
| VOHT Test Point<br>Output High Level<br>PLL_ REF, VCOCLK | 262Ω to VPD<br>402Ω to GND<br>VPD = 5.0V<br>VOHT - VPD | | -.85 | | V |
| VOLT Test Point<br>Output Low Level<br>PLL_REF, VCOCLK | 262Ω to VPD<br>402Ω to GND<br>VPD = 5.0V, VOHT - VPD | | -1.75 | | V |

* Output load is a 4K resistor to 5V and a 10 pF capacitor to DGND.

**MODE CONTROL**

| | | | | | |
|---|---|---|---|---|---|
| Enable to/from $\overline{\text{PDWN1}}$ Transition Time | Settling time of external capacitors not included, $\overline{\text{PDWN}}$ pin high to/from low | | | 20 | µs |
| Read to Write Transition Time | WG pin low to high | | | 1.0 | µs |
| Write to Read Transition Time | WG pin high to low<br>AGC setting not included | 0.4 | 0.9 | 1.6 | µs |
| $\overline{\text{HOLD}}$ On to/from $\overline{\text{HOLD}}$ Off Transition Time | $\overline{\text{HOLD}}$ pin high to/from low | | | 1.0 | µs |
| RG Time Delay | | | | 100 | ns |

**READ MODE** (WG is low)

**AGC AMPLIFIER**

Unless otherwise specified, recommended operating conditions apply. Input signals are AC coupled to IN±. OUT± are loaded differentially with 340Ω x 2 to VPA1, and each side is loaded with < 10 pF to AGND1, and AC coupled to DIN±. A 0.1 µF capacitor is connected between BYP and AGND1. AGC pin is open.

| | | | | | |
|---|---|---|---|---|---|
| Gain Range | 1.0 Vpp ≤ (OUT+) - (OUT-) ≤ 3.0 Vpp | 4 | | 80 | V/V |
| AGC Input Range | AGC output = 1Vpp differential | 25 | | 250 | mVpp |
| Output Offset Voltage Variation | Over entire gain range | -500 | | +500 | mV |
| Maximum Output Voltage Swing | Set by BYP or VEGC pin | 3.0 | | | Vpp |
| Differential Input Resistance | (IN+) - (IN-) = 100 mVpp @ 2.5 MHz | 4 | 5.4 | 7.5 | kΩ |

**AGC AMPLIFIER** (Continued)

| PARAMETER | CONDITION | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Differential Input Capacitance | (IN+) - (IN-) = 100 mVpp @ 2.5 MHz | | 5 | 10 | pF |
| Single Ended Input | WG = low, IN+ or IN- | 2 | 2.7 | 4 | kΩ |
| Impedance | WG = high, IN+ or IN- | | 160 | 250 | Ω |
| Input Noise Voltage | Gain set to maximum, Rs = 0 Bw = 15 MHz | | 5 | 15 | $nV/\sqrt{Hz}$ |
| Bandwidth | -3 dB bandwidth at maximum gain | 12 | | | MHz |
| OUT+ & OUT- Pin Current | No DC path to AGND1 | 2.5 | 4.0 | | mA |
| CMRR (Input Referred) | (IN+) = (IN-) = 100 mVpp @ 5 MHz, gain set to max | 40 | | | dB |
| PSRR (Input Referred) | VPA1, 2 = 100 mVpp @ 5 MHz, gain set to max | 30 | | | dB |
| (DIN+) - (DIN-) Input Swing vs. AGC Input (DIN+) - (DIN-) = ($V_{AGC}$ - K1) • K2 | 25 mVpp ≤ (IN+) - (IN-) ≤ 250 mVpp, $\overline{HOLD}$ = high, 0.5 Vpp ≤ (DIN+) - (DIN-) ≤ 1.5 Vpp | | | | |
| | K1 | 0.5 | 0.8 | 0.95 | V |
| | K2 | 0.54 | 0.64 | 0.74 | Vpp/V |
| (DIN+) - (DIN-) Input Voltage Swing Variation | 25 mVpp ≤ (IN+) - (IN-) ≤ 250 mVpp | | | 5.0 | % |
| AGC Voltage | AGC open | 2.0 | 2.3 | 2.6 | V |
| AGC Pin Input Impedance | | 1.8 | 2.5 | 3.8 | kΩ |
| Slow AGC Discharge Current | (DIN+) - (DIN-) = 0V, AGC pin open | 2.8 | 4.5 | 6 | µA |
| Fast AGC Discharge Current | Starts at 0.9 µs after WG goes low, stops at 1.8 µs after WG goes low | | 0.12 | | mA |
| BYP Leakage Current | $\overline{HOLD}$ = low | -0.2 | | +0.2 | µA |
| Slow AGC Charge Current | (DIN+) - (DIN-) = 0.563 VDC, AGC pin open | -0.11 | -0.18 | -0.25 | mA |
| Fast AGC Charge Current | (DIN+) - (DIN-) = 0.8 VDC, AGC pin open | -0.9 | -1.4 | -1.9 | mA |
| Fast to Slow Attack Switchover Point | $\frac{[(DIN+)-(DIN-)]}{[(DIN+)-(DIN-)]FINAL}$ | | 125 | | % |

**AGC AMPLIFIER** (Continued)

| PARAMETER | CONDITION | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Gain Decay Time (Td) | (IN+) - (IN-) = 250 mVpp to 125 mVpp @ 0.6 MHz, (OUT+) - (OUT-) to 90% final value | | 100 | 180 | µs |
| | (IN+) - (IN-) = 50 mVpp to 25 mVpp at 0.6 MHz (OUT+) - (OUT-) to 90% final value | 190 | 300 | 550 | µs |
| Gain Attack Time | WG = high to low (IN+) - (IN-) = 250 mVpp @ 0.6 MHz, (OUT+) - (OUT-) to 110% final value | | 8 | 15 | µs |

**WRITE MODE** (WG is high)

| PARAMETER | CONDITION | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Single Ended Input Impedance (Each Side) | IN+ or IN- | | 160 | 250 | Ω |

**HYSTERESIS COMPARATOR**

Unless otherwise specified, recommended operating conditions apply. Input (DIN+) - (DIN-) is an AC coupled, 1.0 Vpp, 0.6 MHz sine wave. 0.5 VDC is applied to the HYS pin. WG pin is low.

| | | | | | |
|---|---|---|---|---|---|
| Input Signal Range | | | | 1.5 | Vpp |
| Differential Input Resistance | (DIN+) - (DIN-) = 100 mVpp @ 0.6 MHz | 3 | 5.5 | 8 | kΩ |
| Differential Input Capacitance | (DIN+) - (DIN-) = 100 mVpp @ 0.6 MHz | | 4 | 8 | pF |
| Single Ended Input Impedance (Each Side) | DIN+ or DIN- | 1.5 | 2.75 | 4 | kΩ |
| Level Gain | 0.6 Vpp < (DIN+) - (DIN-) < 1.5 Vpp, 10K between LEVEL and AGND | 0.80 | 1.00 | 1.25 | V/Vpp |
| Slope of Level Gain | Calculated from 0.6 Vpp < (DIN+) - (DIN-) < 1.5 Vpp | 0.75 | 0.87 | 1.00 | V/Vpp |
| Intercept of Level Gain | DIN± = 0 Vpp | -0.6 | -0.4 | -0.2 | V |
| Level Gain | | Slope + (Intercept/DIN) | | | |
| Level Pin Output Impedance | $I_{LEVEL}$ = 0.2 mA | 100 | 200 | 300 | Ω |
| Level pin Maximum Output Current | | 1.5 | | | mA |

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**HYSTERESIS COMPARATOR** (Continued)

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| Hysteresis Gain | 0.3V < HYS < 1.0V | 0.30 | 0.41 | 0.50 | V/V |
| Slope of Hysteresis Gain | Calculated from 0.3V < HYS < 1.0V | 0.34 | 0.42 | 0.46 | V/Vpp |
| Intercept of Hysteresis Gain | HYS = 0V | -0.05 | 0.00 | 0.05 | V |
| Hysteresis Gain | | Slope + (Intercept/HYS V) | | | |
| HYS Pin Current | 0.3 V < HYS < 1.0V | 0.0 | | -5 | µA |
| DOUT Pin Output Low Voltage | 5 kΩ from DOUT to AGND2 | VPA2 -2.5 | VPA2 -2 | VPA2 -1.35 | V |
| DOUT Pin Output High Voltage | 5 kΩ from DOUT to AGND2 | VPA2 -2.0 | VPA2 -1.6 | VPA2 -1.1 | V |

**ACTIVE DIFFERENTIATOR**

Unless otherwise specified, recommended operating conditions apply. Input (DIN+) - (DIN-) is an AC-coupled, 1.0 Vpp, 0.6 MHz sine wave. 100Ω in series with 265 pF are tied from DIF+ to DIF-.

| | | | | | |
|---|---|---|---|---|---|
| Input Signal Range | | | | 1.5 | Vp-p |
| Differential Input Resistance | (CIN+) - (CIN-) = 100 mVp-p @ 2.5 MHz | 8 | 10 | 14 | kΩ |
| Differential Input Capacitance | (CIN+) - (CIN-) = 100 mVp-p @ 2.5 MHz | | | 5.0 | pF |
| Common Mode Input Impedance | Both sides | 2.0 | 2.5 | 3.5 | kΩ |
| Voltage Gain From CIN± to DIF± | (DIF+ to DIF-) = 2 kΩ | | 1 | | V/V |
| DIF+ to DIF- Pin Current | Differentiator impedance must be set so as to not clip the signal for this current level | ±0.7 | | | mA |
| COUT Pin Output Low Voltage | 5 kΩ from COUT to GND | VPA2 -2.5 | VPA2 -2 | VPA2 -1.35 | V |
| COUT Pin Output High Voltage | 5 kΩ from COUT to GND | VPA2 -2 | VPA2 -1.6 | VPA2 -1.1 | V |
| COUT Pin Output Pulse Width | | | 36 | | ns |

**QUALIFIER TIMING** (See Figure 8)

Unless otherwise specified, recommended operating conditions apply. Inputs (DIN+) - (DIN-) are an AC coupled, 1.0 Vpp, 0.6 MHz sine wave. 100Ω in series with 265 pF are tied from DIF+ to DIF-. 0.5V is applied to the HYS pin. COUT and DOUT have a 5 kΩ pull-down resistor (for test purposes only.) WG pin is low. $\overline{RDO}$ is loaded with a 4 kΩ resistor to VPD and a 10 pF capacitor to DGND.

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| Td1 | D Flip-Flop Set Up Time | Minimum allowable time delay from (DIN+) - (DIN-) exceeding hysteresis point to (DIF+) - (DIF-) hitting a peak value. | 0 | | | ns |
| Td3 | Propagation Delay | | | 60 | 110 | ns |
| Td3-Td4 | Pulse Pairing | | | | 6 | ns |
| Td5 | Output Pulse Width | | 25 | 36 | 55 | ns |

## SYNCHRONIZER SECTION

**READ MODE**

| | | | | | |
|---|---|---|---|---|---|
| TRVCO, VCO Output Rise Time | 0.8V to 2.0V, CL ≤ 15 pF | | | 8 | ns |
| TFVCO, VCO Output Fall Time | 2.0V to 0.8V, CL ≤ 15 pF | | | 5 | ns |
| TSRD, SRD Output Pulse Width | | (TVCO) -12 | | (TVCO) +12 | ns |
| TRSRD, Read Data Rise Time | 0.8V to 2.0V, CL ≤ 15 pF | | | 10 | ns |
| TFSRD, Read Data Fall Time | 2.0V to 0.8V, CL ≤ 15 pF | | | 8 | ns |
| TPSRD, SRD Output Setup/HoldTime | Falling edge of VCO to either edge of SRD | -15 | | 15 | ns |
| TRD, $\overline{RDT}$ Input Pulse Width | | 20 | | (TVCO) -20 | ns |
| TFRD, $\overline{RDT}$ Input Fall Time | | | | 15 | ns |
| TWVCO, VCO Output | | .26TVCO | | .74TVCO | ns |
| Pulse Width (Includes Effects of Window Shift) | | -10 | | +10 | |

**WINDOW SYMMETRY CONTROL CHARACTERISTICS**

| | | | | | |
|---|---|---|---|---|---|
| TWSS $\overline{WS0}$, $\overline{WS1}$, WSD Set Up Time | | 50 | | | ns |
| TWSH $\overline{WS0}$, $\overline{WS1}$, WSD Hold Time | | 0 | | | ns |

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**DATA SYNCHRONIZATION**

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| TVCO | VCO Center Frequency Period | VCO IN = 2.7V<br>TO = 83.8 (RR + 1.78),<br>RR = 3k to 9k<br>VPA2 = 5.0V | 0.8TO | | 1.2TO | ns |
| | VCO Frequency Dynamic Range | 1.0V ≤ VCO IN ≤ VPA2-0.6V<br>VPA2 = 5.0V | ±22 | | ±45 | % |
| KVCO | VCO Control Gain | $\omega o = 2\pi / TO$<br>1.0V ≤ VCO IN ≤ VPA2-0.6V | 0.16 ωo | | 0.25 ωo | rad/s V |
| KD | Phase Detector Gain | KD = 0.538 / (RR+500)<br>VPA2 = 5.0V | 0.83 KD | | 1.17 KD | A/rad |
| * | KVCO x KD Product Accuracy | | -28 | | +28 | % |
| * | VCO Phase Restart Error | | | 12 | | ns |
| | Decode Window Centering Accuracy | | -.02 TVCO | | .02 TVCO | ns |
| | Decode Window | | 0.9 TVCO | | | ns |
| TS1 | Decode Window Time Shift | TWS1 = .05 TVCO<br>$\overline{WSO}$ = 0; $\overline{WSI}$ = 1 | | TWS1 | | ns |
| TS2 | Decode Window Time Shift | TWS2 = .15 TVCO<br>$\overline{WSO}$ = 1; $\overline{WSI}$ = 0 | | TWS2 | | ns |
| TS3 | Decode Window Time Shift | TWS3 = .2 TVCO<br>$\overline{WSO}$ = 0; $\overline{WSI}$ = 0 | | TWS3 | | ns |
| TSA | Decode Window Time Shift | $TWSA = 0.29\,TVCO\left(1-\frac{3260+R}{5950+R}\right)$<br>$\overline{WSO}$ = 1; $\overline{WSI}$ = 1 | | TWSA | | ns |
| * | Not directly testable; design characteristics | | | | | |

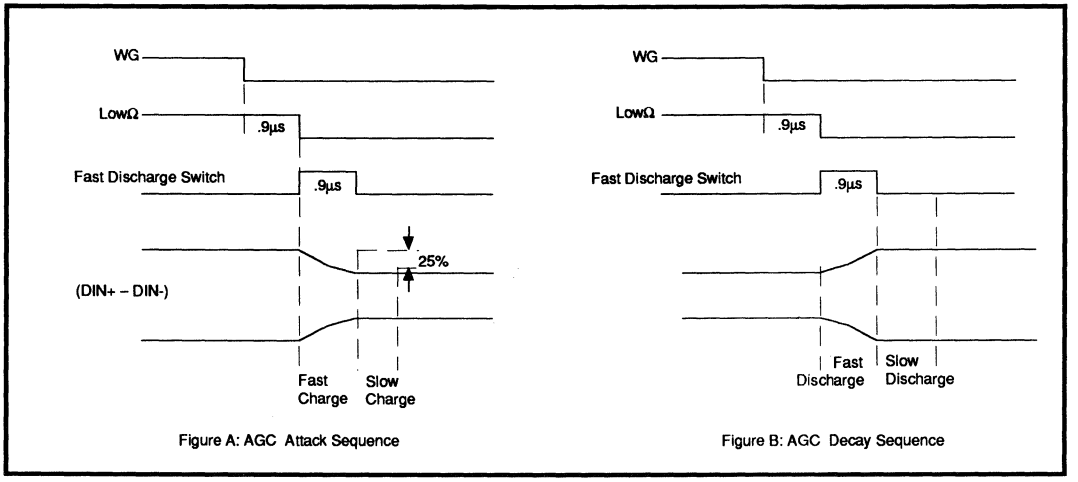


Figure A: AGC Attack Sequence

Figure B: AGC Decay Sequence

**FIGURE 7: AGC Timing Diagram**

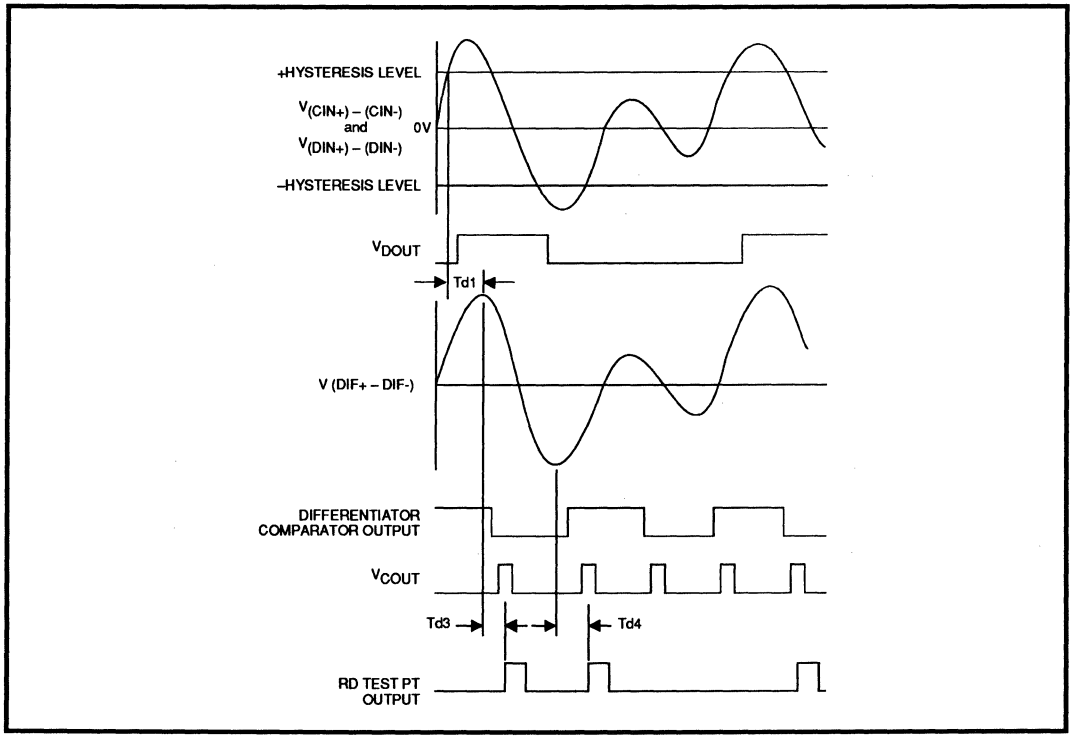


**FIGURE 8: Read Mode Digital Section Timing Diagram**

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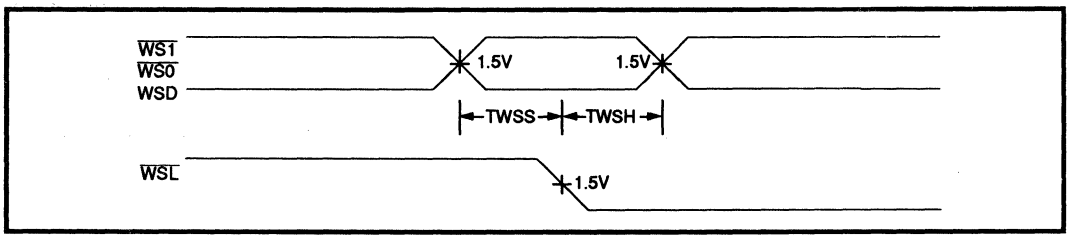


**FIGURE 9: Window Symmetry Control Timing**

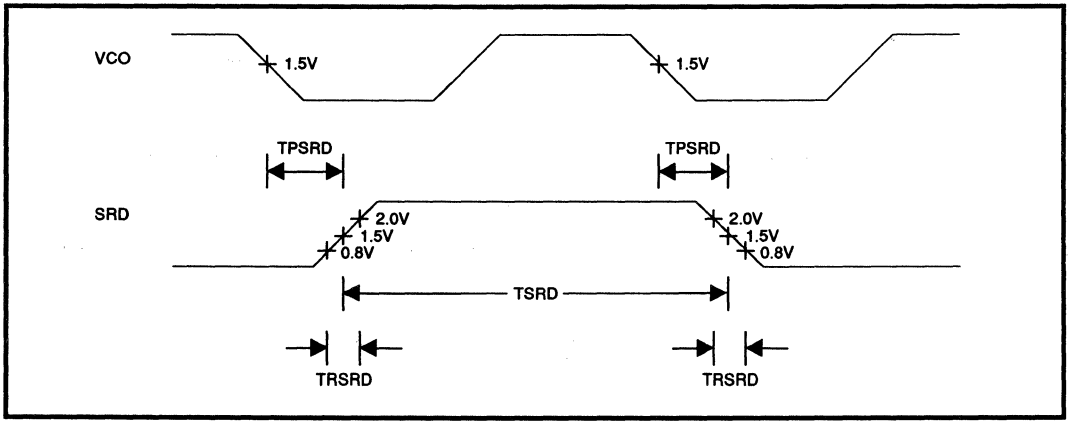


**FIGURE 10: Read Mode Timing**

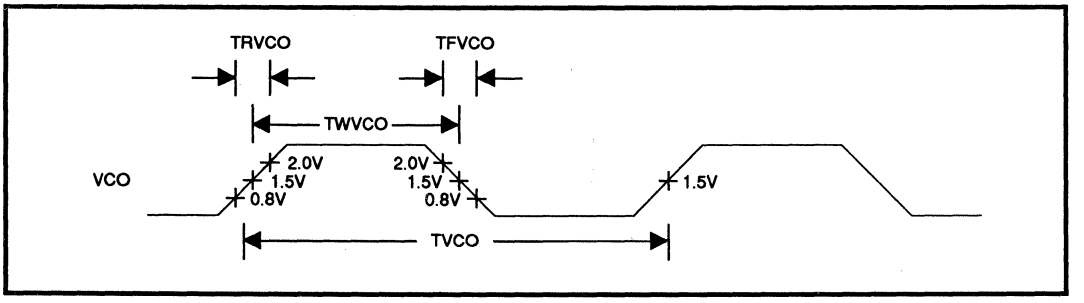


**FIGURE 11: VCO Timing**

## APPLICATIONS INFORMATION

The SSI 34P553/5531 PLL uses a new architecture which incorporates an accurate quarter cell delay circuit. The standard architecture of a data synchronizer PLL is shown in Figure14A. In read mode, the rising edge of the quarter cell delay enables the phase detector, and the falling edge is locked to the VCO. Ideally, the quarter cell delay enables the phase detector one half of an encoded bit cell time before the phase comparison takes place. A data bit could then shift early or late by one half of an encoded bit cell time before a phase detector output error would occur. If the quarter cell delay is not exactly one half of an encoded bit cell time, a phase detector error will occur when the read data shifts by an amount that is smaller than one half of an encoded bit cell time when shifting in one direction and an amount larger than one half of an encoded bit cell time in the other direction. In addition, when an error occurs, the resulting charge pump output goes from maximum output one way to maximum output the other way. This can cause loss of lock to occur. The timing is shown in Figure 15.

The SSI 34P553/5531 achieves an accurate quarter cell delay time by using the VCO control voltage to compensate the quarter cell delay one-shot circuit for process, temperature and power supply induced timing variations. The modified architecture of the SSI 34P553/5531 data synchronizer is shown in Figure 16B. Because the quarter cell delay timing is adjusted by the VCO control voltage, there is an effect on the PLL transfer function due to the new quarter cell delay circuit.

The quarter cell delay circuit produces a time delay output in response to a voltage input. In order to include this function in a phase-locked loop, the time delay function must be converted into a phase function. This is straightforward, since a time delay is equivalent to a phase angle. The equivalent phase representation of the quarter cell delay is derived below.

For the VCO: $K_o = \frac{d\omega_o}{dV}$ (1a)

$$\frac{dT_o}{dV} = \frac{d}{dV}\left(\frac{1}{f_o}\right) = -\frac{1}{f_o^2}\frac{df_o}{dV} = -T_o^2\frac{df_o}{dV} = -\frac{T_o^2}{2\pi}\frac{dw_o}{dV} \quad (1b)$$

where:

$K_o$ = VCO gain
$\omega_0$ = VCO center frequency (rad/s)
$f_0$ = VCO center frequency (Hz)
$T_0$ = VCO center frequency (sec)

For the quarter cell delay,

$$K_T = \frac{dq_o}{dV} = \frac{2\pi}{T_o}a\frac{dT_0}{dV} = -\alpha T_o\frac{dw_o}{dV} = -\alpha T_o K_o$$

where:

$\theta_0$ = Phase due to quarter cell delay circuit
$T_0$ = VCO center frequency period
$T_Q$ = Quarter cell delay time
$\alpha = T_Q/T_0 = 0.5$ for the 32P548

The gain of the quarter cell delay block is constant in the SSI 34P553/5531, regardless of the values of other components.

For the SSI 34P553/5531, the nominal value of $K_T$ is $0.17\pi$.

### PLL TRANSFER FUNCTION

There are two modes of operation of the PLL, and two transfer functions. In write and idle modes, the PLL is locked to the reference oscillator, and the quarter cell delay does not enter into the transfer function. In read, mode, the PLL is locked to read data, and the quarter cell delay is included in the transfer function. In addition, the effective loop gain of the PLL increases in idle mode due to the phase detector. This will be explained later in more detail.

The transfer functions for read and idle modes are given in (3) and (4), respectively.

$$\frac{\theta_O(s)}{\theta_r(s)} = \frac{\frac{nK_OK_dF(s)}{S}}{1+nK_TK_dF(s)+\frac{nK_OK_dF(s)}{S}} \quad (3)$$

$$\frac{\theta_O(s)}{\theta_r(s)} = \frac{\frac{nK_OK_dF(s)}{S}}{1+\frac{nK_OK_dF(s)}{S}} \quad (4)$$

where:

$K_T$ = Quarter cell delay one-shot gain
$K_O$ = VCO gain
$K_d$ = Phase detector gain
F(s) = Loop filter transfer function
n = Ratio of input freq. to reference freq.

In (3) the K term in the denominator is a result of the quarter cell delay. Substituting $K_T = \alpha K_O T_O$ into (3),

$$\frac{\theta_O(s)}{\theta_r(s)} = \frac{\frac{nK_OK_dF(s)}{S}}{1+(1-s\alpha T_O)\frac{nK_OK_dF(s)}{S}}$$

The additional $-s\alpha T_O$ term in the denominator due to the quarter cell delay introduces positive feedback. However, the gain of the positive feedback is always less than one, so there is no instability. The additional term is not always negligible, and must be taken into account in the loop analysis and design.

Two loop filter configurations, shown in Figure 12, will be considered. Both filters result in a second order type 2 loop transfer function, with only minor differences in the loop equation.

The transfer function of the loop filter for a charge-pump PLL is the transimpedance, $V_o/I_i$ (s), where $V_o$ (s) is the output voltage, and $I_i$ (s) is the input current. The transfer functions of (a) and (b) are given by:

$$F_a(s) = \frac{sR_1C_1+1}{s(C_1+C_2)\left(sR_1\frac{C_1C_2}{C_1+C_2}+1\right)} \quad (6)$$

$$F_b(s) = \frac{sR_1(C_1+C_2)+1}{sC(sR_1C_2+1)} \quad (7)$$

For loop filter (a), $C_2$ is normally chosen to be much smaller than $C_1$ so that it does not affect the loop transfer function significantly. Assuming that $C_1 \gg C_2$ and $sR_1C_1 \ll 1$ at the frequencies of interest, (6) reduces to:

$$F_a(s) = \frac{sR_1C_1+1}{sC_1} \quad (8)$$

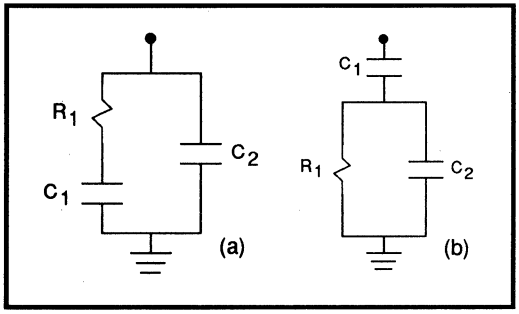


**FIGURE 12: Loop Filter**

For loop filter (b), $C_2$ is normallly chosen to be much smaller than $C_1$ so that it does not affect the loop transfer function significantly. Assuming that $C_1 \gg C_2$ and that $sR_1C_2 \ll 1$ at the frequencies of interest, (7) reduces to:

$$F_b(s) = \frac{sR_1C_1+1}{sC_1} \quad (9)$$

Equations (8) and (9) are the same, and either loop filter may be used. Substituting (8) into (3) gives:

(10)

$$\frac{\theta_O(s)}{\theta_r(s)} = \frac{\frac{nK_OK_d}{C_1(1-\alpha T_O nK_OK_dR_1)}(sR_1C_1+1)}{s^2+s\frac{nK_OK_d}{1-\alpha T_O nK_OK_dR_1}\left(R_1-\frac{\alpha T_O}{C_1}\right)+\frac{nK_OK_d}{C_1(1-\alpha T_O nK_OK_dR_1}}$$

This is in the form of a standard second order transfer fucntion. The denominator has the form:

$$D(s) = s^2 + 2\zeta\omega_n s + \omega_n^2 \quad (11)$$

where: $\zeta$ = damping factor
$\omega_n$ = natural frequency

The damping factor and natural frequency of (10) can be extracted:

$$\omega_n = \sqrt{\frac{nK_OK_d}{C_1(1-\alpha T_O nK_OK_dR_1)}} \quad (12)$$

$$\zeta = \frac{R_1-\frac{\alpha T_O}{C_1}}{2}\sqrt{\frac{nK_OK_dC_1}{1-\alpha T_O nK_OK_dR_1}} \quad (13)$$

Substituting (8) into (4) gives the transfer function for idle mode:

$$\frac{\theta_O(s)}{\theta_r(s)} = \frac{\frac{nK_OK_d}{C_1}(sR_1C_1+1)}{s^2+s(nK_OK_dR_1)+\frac{nK_OK_d}{C_1}} \quad (14)$$

Again, this is in the form of a second order transfer function. The damping factor and natural frequency are found to be:

$$\omega_n = \sqrt{\frac{nK_OK_d}{C_1}} \quad (15)$$

$$\zeta = \frac{R_1}{2}\sqrt{nK_OK_dC_1} \quad (16)$$

To design the loop for proper read mode operation using (12) and (13), R, and C, must be found in terms of the damping factor and natural frequency.

To do this, first find $\zeta/\omega_n$, then solve for $R_1C_1$.

$$R_1C_1 = \frac{2\zeta}{\omega_n} + \alpha T_O \quad (17)$$

Substitute this value for $R_1C_1$ into the equation for $\omega_n$ and solve for $C_1$.

$$C_1 = \frac{nK_OK_d}{\omega_n^2} + \alpha T_O nK_OK_d\left(\frac{2\zeta}{\omega_n} + \alpha T_O\right) \quad (18)$$

Now that $C_1$ is known, $R_1$ can be found by dividing (17) through by $C_1$.

$$R_1 = \left(\frac{2\zeta}{\omega_n} + \alpha T_O\right)\frac{1}{C_1} \quad (19)$$

**EXAMPLE 1**

Assume that the data rate is 0.6 Mbit/s, $\zeta = 0.7$, a length of 20 2T patterns for the loop to lock is used, and $\omega_n t = 5.7$ for error < 1%.

n = 0.5 due to the 2T pattern.

$$T_O = \frac{1}{f_O} = \frac{1}{1.2\cdot10^6} = 833\text{ns}$$

$\omega_0 = 2\pi f_0 = 2\pi\ (1.2 \cdot 10^6) = 7.54 \cdot 10^6$ rad/s

$\alpha_0 = 0.5$

For the SSI 34P553: $RR = \frac{5.97}{DR} - 1.79(k\Omega) = 8.17k\Omega$

where DR = Data Rate in Mbit/s

$$K_0 = 0.17\omega_0 = 1.28\cdot10^6\ \frac{\text{rad/sec}}{\text{Volt}}$$

$$K_d = \frac{0.62}{RR+500} = 71.51\cdot10^{-6}\ \text{A/rad}$$

$K_T = 0.17\pi = 0.534$

Assuming a length of 20 2T patterns, then:
t = (20) (2) (833) ns = 33.3 µs

$$\omega n = \frac{5.7}{33.3\mu s} = 1.71\cdot10^5\ \text{rad/s}$$

$C_1$ = 1565 pF + 165.6 pF = 1.73 nF

$R_1$ = 5.02 kΩ

The resulting loop filter is shown in Figure 13.

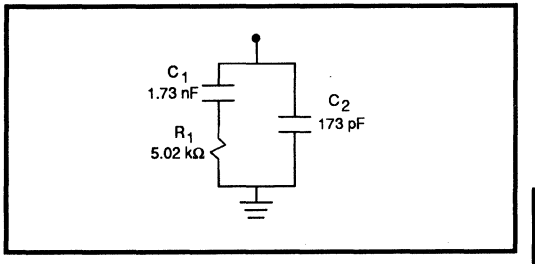


**FIGURE 13**

The value of $C_2 = C_1/10$ is chosen to damp out transients on the FILT pin and meet the requirement $C_2 \ll C_1$.

When the loop locks to the reference oscillator in idle mode, the loop transfer function is given by (14), and $\omega_n$ and $\zeta$ are given by (15) and (16). $R_1$ and $C_1$ from Example 1 can be substituted into these equations to find the resulting natural frequency and damping factor in idle mode.

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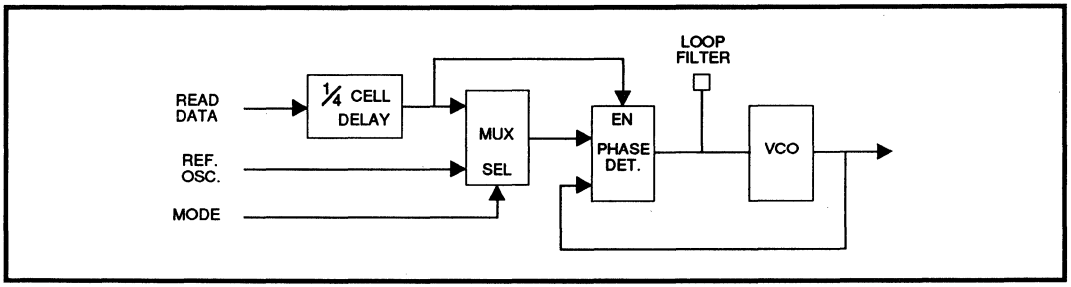



**FIGURE 14A: Standard Configuration of a Data Synchronizer Phase-Locked Loop**

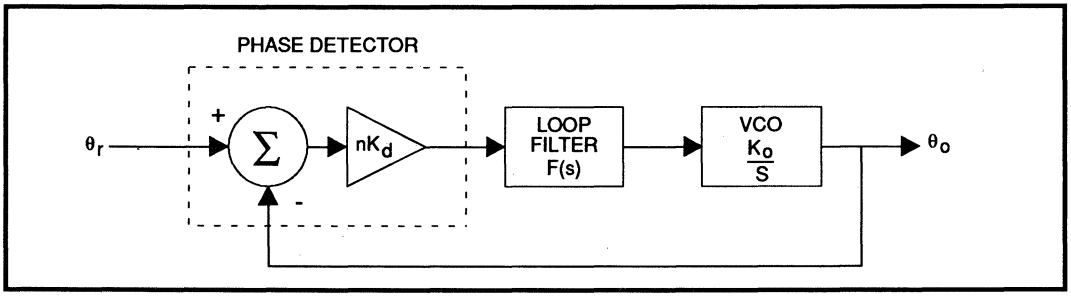



**FIGURE 14B: Phase-Lock Loop System Representation**

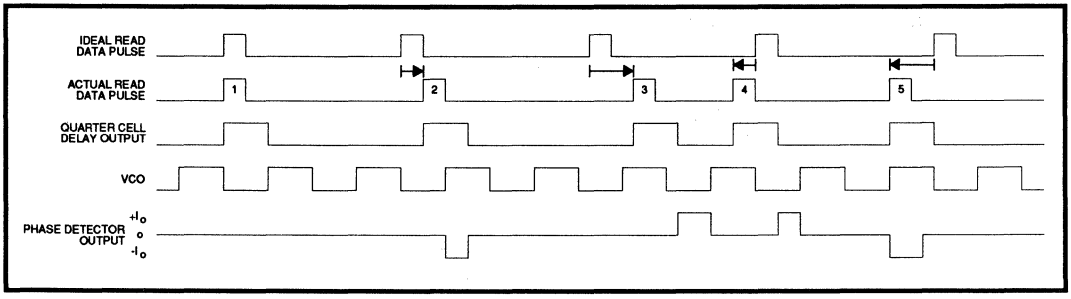



**FIGURE 15A: Phase Detector Timing with Ideal Quarter Cell Delay.** For an ideal pulse (1), there is no phase detector output. When a pulse is shifted late (2) or early (4) by less than the quarter cell delay time, the phase detector output is negative or positive, respectively. When the read data is shifted late (3) or early (5) by more than the quarter cell delay time, a phase detector output polarity error occurs. In this case, the output polarity becomes positive for a late shifted pulse and negative for an early shifted pulse.

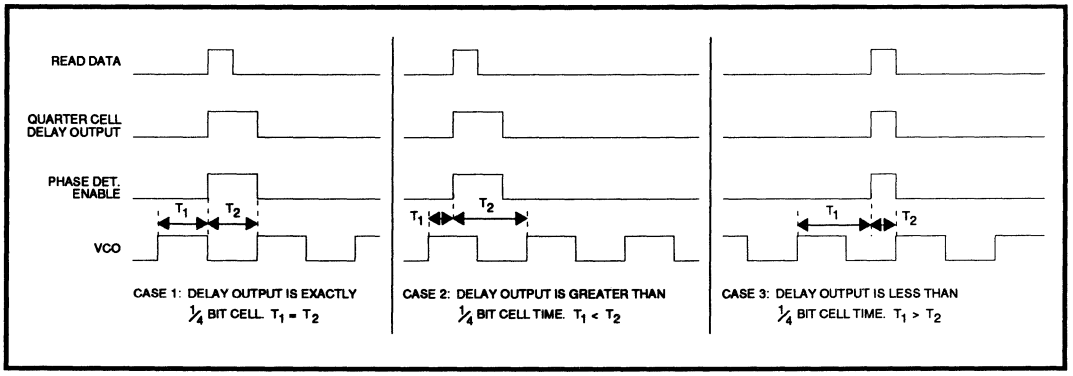



**FIGURE 15B: Timing of Phase Detector Enable Logic.** The read data input pulse can shift to the left by T1 and to the right by T2 before an error occurs in the phase detector output polarity, If the quarter cell delay output is not exactly 1/4 bit cell wide, then T1 ≠ T2, as shown in cases 2 and 3.

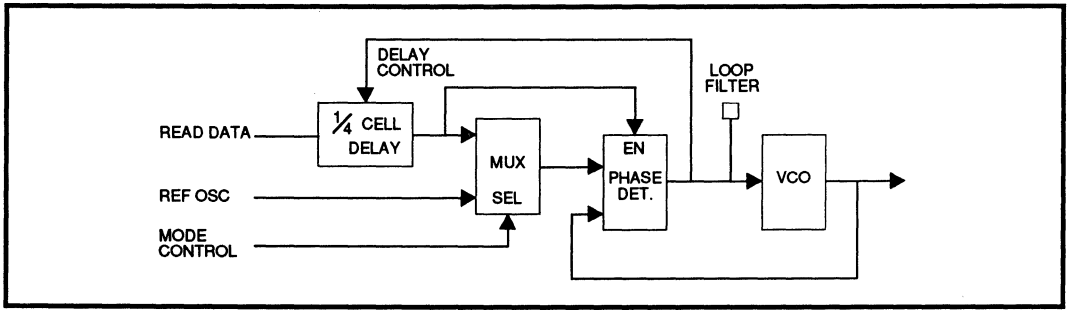



**FIGURE 16A: Modified Data Synchronizer Phase-Locked-Loop with Quarter Cell Delay Control**

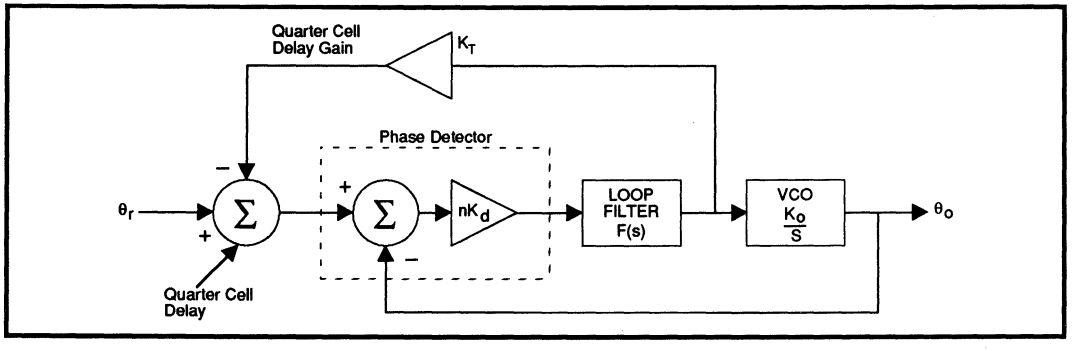


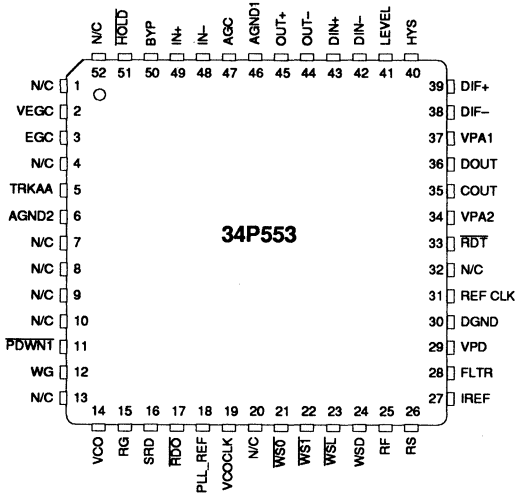

**FIGURE 16B: Modified Data Synchronizer System Representation**

# SSI 34P553/5531
# Pulse Detector & Data Synchronizer

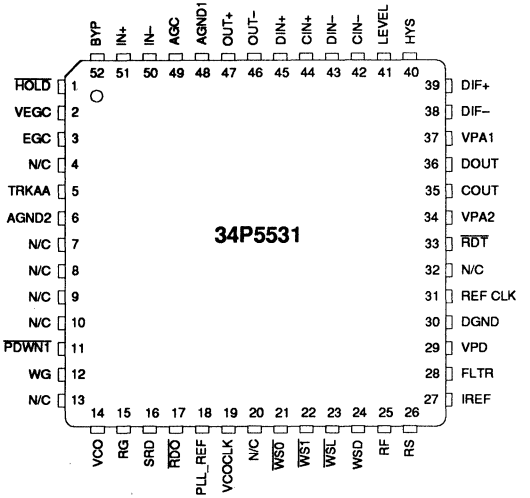
## PACKAGE PIN DESIGNATIONS
(Top View)

**THERMAL CHARACTERISTICS: θja**

| | |
|---|---|
| 52-Lead QFP | 75° C/W |




**52-Lead QFP**




**52-Lead QFP**

## ORDERING INFORMATION

| PART DESCRIPTION | ORDERING NUMBER | PACKAGE MARK |
|---|---|---|
| SSI 32P553 Pulse Detector & Data Synchronizer | | |
| 52-Lead QFP | 32P553-CG | 32P553-CG |
| SSI 32P5531 Pulse Detector & Data Synchronizer | | |
| 52-Lead QFP | 32P5531-CG | 32P5531-CG |



Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 573-6000, FAX (714) 573-6914

silicon systems®
A TDK Group Company

# SSI 34P3200
## Pulse Detector & Data Synchronizer for High Density Floppy Storage

**Advance Information**

January 1993

## DESCRIPTION

The SSI 34P3200 is a high performance pulse detector and data synchronizer integrated circuit. This device is designed for use in high density floppy storage applications conforming to the JEIDA standard. The pulse detection portion of this device detects and validates amplitude peaks in the output from a disk drive read amplifier. The data synchronization portion is a 2,7 RLL or MFM data synchronizer with window shift and write pre-compensation capability. The SSI 34P3200 supports a sleep mode for minimal power dissipation in non-operational periods.

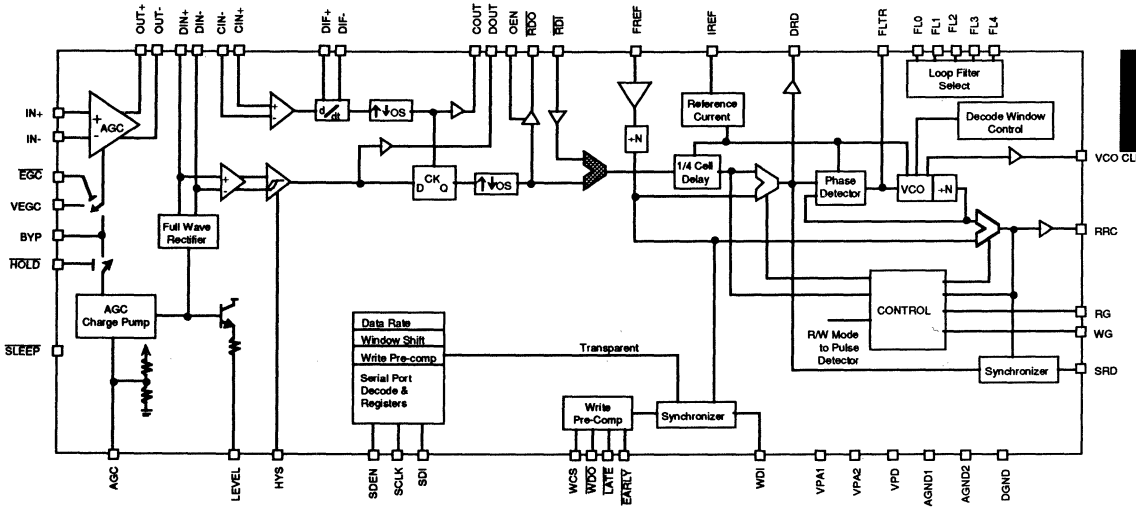
The SSI 34P3200 features a 3-pin serial port for easy selection of data rate and operating configurations

The SSI 34P3200 is available in a 52-lead QFP package.

## FEATURES

- **Highly Integrated Pulse Detector & Data Synchronizer**
- **Ideal for High Density Floppy Storage Application in JEIDA Standard**
- **Operating Data Rate: 250K/500K/1M/2M/3M/ 4.5M/6M NRZ bits per second**
- **Supports 2,7 RLL or MFM Encoding Format**
- **3-Pin Serial Port Programming: Data Rate Selection, Window Symmetry Control & Test Mode**
- **Fast Acquisition Phase Lock Loop & Zero Phase Restart Technique**
- **5V Operation only**
- **Low Operating Power**
- **5 mW Sleep Mode**

## BLOCK DIAGRAM

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## FUNCTIONAL DESCRIPTION

The SSI 34P3200 is a pulse detector and data synchronizer circuit. Its three main functions are:

- Validate and time-position preserve the analog pulses (VIN±) from a read-write pre-amplifier.
- Extract the encoded data bit and its corresponding clock signal.
- Provide write precompensation function for write data signal.

The SSI 34P3200 major functional blocks are:

- AGC amplifier & AGC control
- Pulse qualifier
- Data synchronizer
- Window shift
- Write precompensation
- Serial port decode & registers

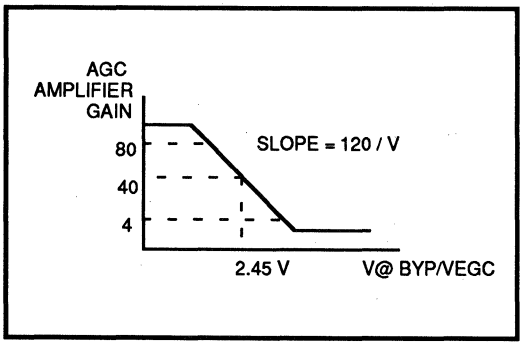



**FIGURE 1: AGC Amplifier Gain vs BYP/VEGC Voltage**

### AGC AMPLIFIER & AGC CONTROL

The AGC amplifier provides signal amplification prior to pulse qualification. The amplifier gain is a linear function of a gain control voltage, Figure 1. The gain control voltage is either the BYP voltage when $\overline{EGC} = 1$, or the VEGC voltage when $\overline{EGC} = 0$.

In the normal read mode, i.e., with the AGC active, the DIN± input signal is regulated to a nominal level which is set by the voltage at the AGC pin. With the AGC pin open, the nominal DIN± level is 1 $V_{PPD}$ (peak-to-peak differential). This nominal DIN± level can be adjusted with an external resistor tied from the AGC pin to either VPA1 or AGND1, as shown in Figure 2.

The AGC actions are current charging and discharging the external BYP integrating capacitor. They are described as follows:

#### Slow Decay

When the instantaneous DIN± signal is below the nominal level, a slow decay current, 4.5 µA, discharges the BYP capacitor. The AGC amplifier gain is increased slowly.

#### Slow Attack

When the instantaneous DIN± signal exceeds the nominal level but is below 125% of the nominal level, a slow attack current, 0.18 mA, charges the BYP capacitor. The AGC amplifier gain is decreased.

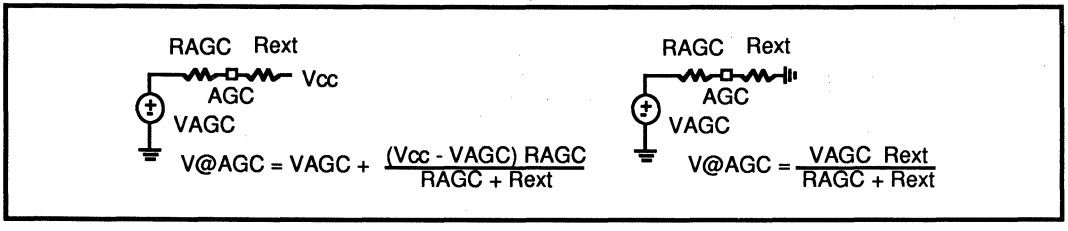



**FIGURE 2: AGC Loop Reference Adjustment**

### Fast Attack

When the instantaneous DIN± signal exceeds 125% of the nominal level, the device enters a fast attack mode. A fast attack current, 1.3 mA, charges the BYP capacitor. The AGC amplifier gain is quickly lowered.

### Write-to-Read Recovery

With a 1-to-0 transition of the WG, the SSI 34P3200 enters the write-to-read recovery mode. The input impedance remains in low impedance state for 0.9 µs for fast input DC coupling recovery. Then, the device restores to high input impedance state, and enters into a fast decay mode for 0.9 µs. In the fast decay mode, a continuous 0.12 mA current discharges the BYP capacitor. The AGC amplifier gain is increased very quickly. (Otherwise only the slow decay mode is available to increase the AGC amplifier gain.) Figure 3 shows the write-to-read AGC action timing.

The following AGC actions, except that of write-to-read recovery, can be suspended with the $\overline{HOLD}$ = 0. The AGC amplifier gain is then held constant, except for leakage effect.

With $\overline{EGC}$ = 0, the AGC amplifier gain is determined by the VEGC voltage. With a fixed external DC voltage, or a second AGC control loop at the VEGC pin, the AGC amplifier gain is set independent of the on-chip AGC control loop, such as when read signal is over a servo demodulation field.

The AGC amplifier outputs are emitter follower outputs.

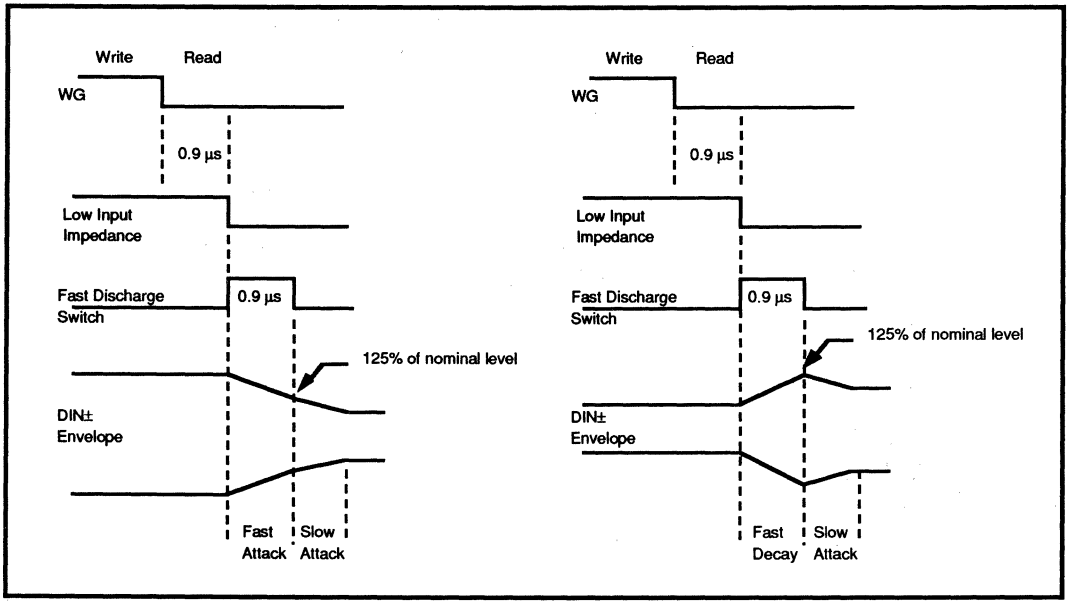



**FIGURE 3: AGC Action Timing in Write-to-Read Recovery**

## FUNCTIONAL DESCRIPTION (continued)

### PULSE QUALIFIER

The pulse qualifier validates each DIN± peak by a combination of level qualification and time qualification. In level qualification, a hysteresis comparator eliminates errors due to low level additive noise. In time qualification, the AGC amplifier output is time differentiated to locate the signal peaks in time.

#### Level Qualification

The level qualification is accomplished by comparing the DIN± signal with a set threshold. The SSI 34P3200 allows two ways of setting the thresholds: fixed threshold or DIN± tracking threshold. Fixed threshold can be simply set by a DC voltage at the HYS pin, such as a resistor from VPA1 to ground. The threshold at the comparator can be computed as:

Hysteresis Gain x V@HYS.

For high performance system application, however, DIN± tracking threshold is recommended.

DIN± tracking threshold has the advantage of shorter write-to-read recovery time and lower probability of error with input amplitude drop out. The threshold is designed as a percentage of the DIN± peak voltage. This technique can be implemented by feeding the LEVEL output, through a resistor divider, to the HYS pin. The LEVEL output, amplified peak capture of DIN± signal, can be computed as: Level Gain x DIN± ppd. With the resistor divider, a fraction of the LEVEL output is presented at the HYS pin. The threshold, as a function of DIN±, can be summarized as: Level Gain x Resistor Dividing Ratio x Hysteresis Gain x DIN± ppd. For a typical case of 1 Vppd DIN± signal, assume equal value resistors in the divider network, the threshold is 1 x 0.5 x 0.36 x 1 =0.18V. This represents 36% threshold on a 1 Vppd signal. While both the Level Gain and the Hysteresis Gain bear a moderate tolerance due to typical process variation, they inversely track each other to yield a much tighter threshold accuracy in a closed loop.

While the external resistor divider ratio determines the qualification setting, the total resistance and the peak capture capacitor should be optimized for the system data rate. The RC time constant must be small enough to allow good response to changing DIN± peak, but large enough to provide a constant threshold after a long duration of input absence.

#### Time Qualification

Time qualification is to locate DIN± peaks. With time differentiation, each DIN± peak is translated into a zero crossing, which clocks a on-chip flip-flop in the pulse qualifier. The SSI 34P3200 supports on-chip or off-chip differentiation.

On-Chip Differentiation

The on-chip differentiation is accomplished by connecting an external RLC network across the DIF± pins. The DIN+ and CIN+ pins should be tied together, as well as the DIN- and CIN- pins. The differentiator transfer function from the CIN± input to the flip-flop clock input is given as:

$$Av = \frac{TBD\ Cs}{LC\ s^2 + C(R + TBD)s + 1}$$

where R, L and C are external passive components

$$TBD\ pF < C < TBD\ pF$$
$$s = j\omega = j\ 2\pi f$$

Off-Chip Differentiation

For constant density recording applications, a differentiation function with a low pass bandwidth tracking data rate can maximize the signal-to-noise ratio performance. A time differentiated input can be applied at the CIN± pins, separated from the DIN± pins.

This function can best be supported by the Silicon Systems programmable filters, such as the SSI 32F8030, F8130/8131. The filters feature both a normal low pass output and a differentiated low pass output. The low pass bandwidth is programmable by the user to track the data rate. The signal delays of the two signal paths are well matched.

#### Qualified Read Data

Upon level and time qualification, a one-shot data pulse is generated for every validated peak of the DIN± signal. This read data pulse can be monitored at the $\overline{RDO}$ pin, when OEN = Logic 1. In high speed normal read mode, it is recommended that the $\overline{RDO}$ output be disabled for lower noise performance with OEN = Logic 0. The pulse detector read data can be used as input to the data synchronizer. Alternately, external input at the $\overline{RDI}$ pin can be used as input to the data synchronizer.

Figure 4 summarizes the pulse detector function.

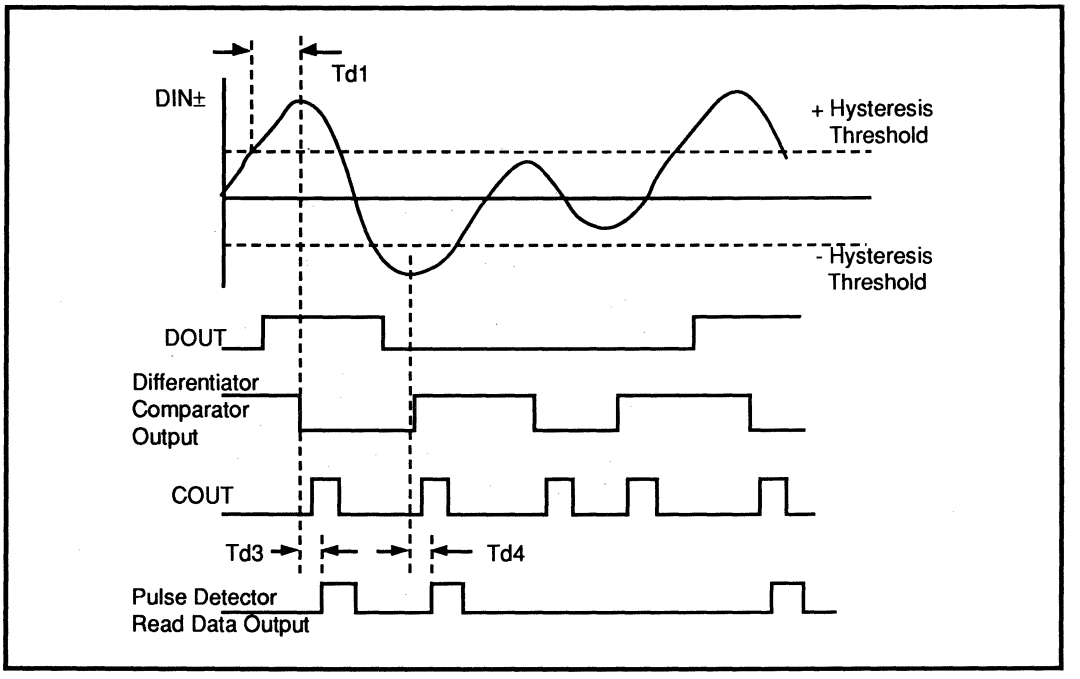



**FIGURE 4: Read Mode Pulse Detector Timing**



### DATA SYNCHRONIZER

The data synchronizer is used to extract the clock and the encoded data signals from the read data signal. The input source to the data synchronizer can be from the pulse qualifier or from an external source via the $\overline{RDI}$ pin.

The SSI 34P3200 is designed to perform data synchronization for the following operating data rates, which are selected through a serial port register R0:

| Rate | NRZ Data Rate | Encoding Format |
|---|---|---|
| 1 | 6 Mbit/s | 2,7 RLL |
| 2 | 4.5 Mbit/s | 2,7 RLL |
| 3 | 3 Mbit/s | 2,7 RLL |
| 4 | 2 Mbit/s | MFM |
| 5 | 1 Mbit/s | MFM |
| 6 | 500 Kbit/s | MFM |
| 7 | 250 Kbit/s | MFM |

For both the 2,7 RLL and MFM encoding formats, the encoded bit rate, as well as the data synchronizer clock, is at twice the NRZ data rate. Thus, the required data synchronizer clock rate is from 500 KHz to 12 MHz.

To accommodate the wide data rate dynamic range, the SSI 34P3200 employs a novel data synchronizer phase locked loop (PLL) architecture (see block diagram). While the voltage controlled oscillator (VCO) operates only between 6 MHz to 12 MHz, a divide-down function is used to generate the lower frequency clock. For Rates 1-3, the VCO operates at 12 MHz, 9 MHz and 6 MHz, respectively. For Rates 4-7, the VCO operates at 8 MHz and the divide-down factor, N, is from 2 to 16.

## FUNCTIONAL DESCRIPTION (continued)

### DATA SYNCHRONIZER (continued)

With the serial register R0 programmed for a specific data rate, the SSI 34P3200 would properly decode the proper VCO frequency and the divide-down factor. Furthermore, the 1/4 cell delay duration, i.e., one half of the encoded bit period, is also set properly for each operating mode.

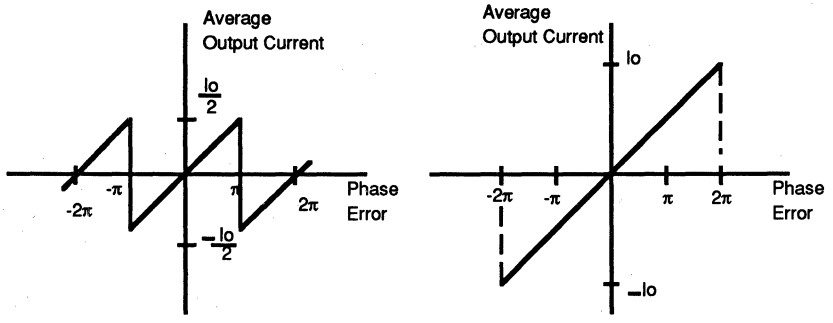
When the SSI 34P3200 is in the idle mode, the VCO should lock to an external reference clock, FREF. For Rates 1-3, the FREF should be 12 MHz, 9 MHz and 6 MHz, respectively. For Rates 4-7, the FREF should be 8 MHz.

The SSI 34P3200 employs a dual mode phase detector: harmonic in the read mode and non-harmonic in the write and idle modes. In the read mode, the harmonic phase detector updates the PLL with each occurrence of a read data pulse from the pulse qualifier. In the write and idle modes, the non-harmonic phase detector is continuously enabled, thus maintaining both phase and frequency lock. Figure 5 shows the phase detector transfer function. By acquiring both phase and frequency lock to the FREF and utilizing a zero phase restart technique, false lock to the pulse detector read data is eliminated.

The phase detector incorporates a charge pump in order to drive the loop filter directly. The polarity and width of the output current pulses correspond to the direction and magnitude of the phase error.

Because of the wide data rate dynamic range, the SSI 34P3200 provides four high impedance/low impedance switchable nodes, FL1-4, for external loop filter component switching. When the node is in high impedance state, the external component connected to this node is switched out. When the node is in low impedance state, the external component is included in the loop filter network.

The various operating modes of the data synchronizer are discussed in the following section.




Note 1) Io is the magnitude of the charge pump current
2) Phase error is relative to the ÷N counter output period

**FIGURE 5: Phase Detector Transfer Function**

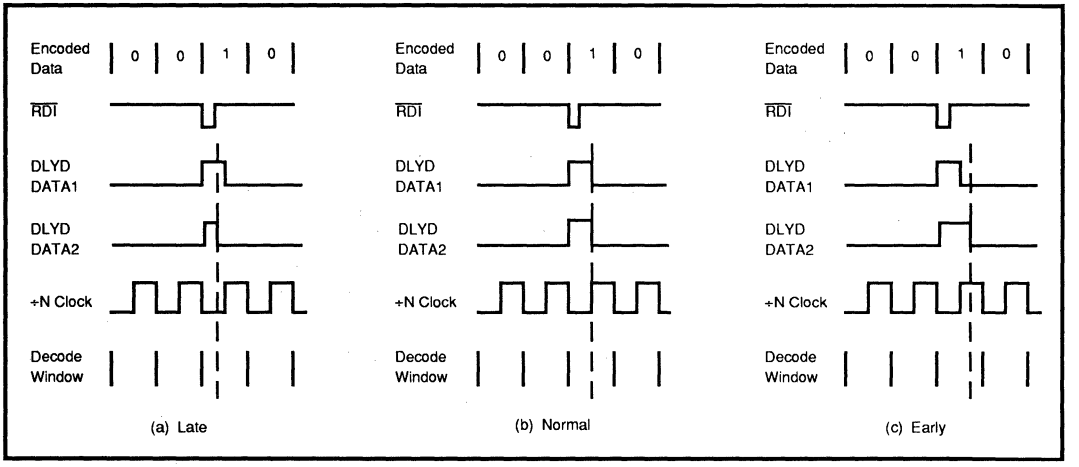



**FIGURE 6: Decode Window & Window Shift Directions**

## WINDOW SHIFT

To enhance the data decode function, the SSI 34P3200 supports a window shift function for the highest three data rate operations. Shifting the symmetry of the VCO clock effectively shifts the relative position of the DLYD DATA pulse within the decode window. This powerful capability, supported through serial register R1, easily facilitates defect mappings, automatic calibration, window margin testing, error recovery, and systematic error cancellation.

The window shift can be set to ±10%, ±15% or ±20% of the decode window. Figure 6 defines the direction of the window shift. Refer to the Serial Port Decode & Registers section for serial port register assignment.

## WRITE PRECOMPENSATION

Write precompensation circuitry is provided to compensate for media bit shift caused by intersymbol interference. The magnitude of the time shift, TC, is determined by an external resistor on the WCS pin, with Rp from WCS to VPA2. TC is given as:

$$TC = 16 \times 10^{-3} R_p$$

## SERIAL PORT DECODE & REGISTERS

The SSI 34P3200 provides a 3-pin serial port to facilitate the following digital controls:

- Data rate (Register 0: Bits 2-0)
- Window shift (Register 1: Bits 3-0)
- Write pre-comp (Register 2: Bit 0)
- Data synchronizer input source (Register 2: Bit 2)

The 3 serial port pins are SDEN, SDI and SCLK. Figure 7 shows a timing diagram of the serial data transmission. Each data transmission consists of a 8-bit packet. Bit 7 being the most significant bit (MSB). The 8-bit packet is divided into two fields: Bit7-4 address field, Bit 3-0 data field. These registers are reset to Q when the power-on function is used.

## FUNCTIONAL DESCRIPTION (continued)

### SERIAL PORT DECODE & REGISTERS (continued)

The register assignment is as follows:

**Register 0** Address 0000

| Bit 3 | Not used | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit 2-0 | NRZ Data Rate | VCOFrequency | Divide Down | FL0 | FL1 | FL2 | FL3 | FL4 |
| 000 | 6 Mbit/s | 12 MHz | 1 | LowZ | Hi-Z | Hi-Z | Hi-Z | Hi-Z |
| 001 | 4.5 Mbit/s | 9 MHz | 1 | LowZ | Hi-Z | Hi-Z | Hi-Z | Hi-Z |
| 010 | 3 Mbit/s | 6 MHz | 1 | LowZ | Hi-Z | Hi-Z | Hi-Z | Hi-Z |
| 011 | 2 Mbit/s | 8 MHz | 2 | Hi-Z | LowZ | Hi-Z | Hi-Z | Hi-Z |
| 100 | 1 Mbit/s | 8 MHz | 4 | Hi-Z | LowZ | LowZ | Hi-Z | Hi-Z |
| 101 | 500 Kbit/s | 8 MHz | 8 | Hi-Z | LowZ | LowZ | LowZ | Hi-Z |
| 110 | 250 Kbit/s | 8 MHz | 16 | Hi-Z | LowZ | LowZ | LowZ | LowZ |

**Register 1** Address 0001

The window shift function is available for the 6 Mbit/s, 4.5 Mbit/s and 3 Mbit/s data rates.

| Bit 3 | Window shift Enable |
|---|---|
| 0 | Disabled |
| 1 | Enabled |
| Bit 2 | Window shift direction |
| 0 | Early |
| 1 | Late |
| Bits 1-0 | Window shift magnitude |
| 00 | 20 % of RRC period |
| 01 | 15 % |
| 10 | 10 % |
| 11 | 0 % |

**Register 2** Address 0010

| Bits 3, 1 | Not used |
|---|---|
| Bit 2 | Data Synchronizer Input Source |
| 0 | From internal pulse qualifier output |
| 1 | From the $\overline{RDI}$ pin |
| Bit 0 | Write Pass Through |
| 1 | Write synchronizer is a simple buffer |
| 0 | Write synchronizer & pre-comp is active |

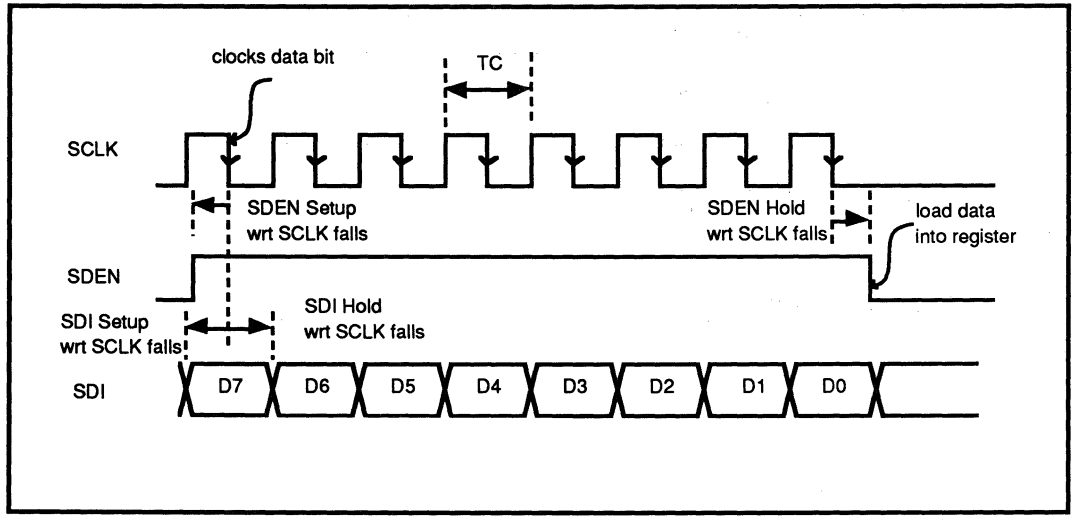



**FIGURE 7: Serial Port Timing**

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## OPERATION MODES

The SSI 32P3200 can support the following operating modes:

| Mode | WG | RG | $\overline{\text{HOLD}}$ | $\overline{\text{EGC}}$ | $\overline{\text{SLEEP}}$ |
|---|---|---|---|---|---|
| Idle<br>VCO locked to FREF<br>AGC active | 0 | 0 | 1 | 1 | 1 |
| Idle<br>VCO locked to FREF<br>AGC gain held constant by BYP | 0 | 0 | 0 | 1 | 1 |
| Idle<br>VCO locked to FREF<br>AGC gain held constant by VEGC | 0 | 0 | X | 0 | 1 |
| Read<br>VCO locked to Pulse Qualifier DLYD DATA<br>AGC active | 0 | 1 | 1 | 1 | 1 |
| Read<br>VCO locked to Pulse Qualifier DLYD DATA<br>AGC gain held constant by BYP | 0 | 1 | 0 | 1 | 1 |
| Read<br>VCO locked to Pulse Qualifier DLYD DATA<br>AGC gain held constant by VEGC | 0 | 1 | X | 0 | 1 |
| Write<br>AGC gain held constant by BYP<br>Input impedance lowered<br>VCO locked to FREF | 1 | X | X | 1 | 1 |
| Write<br>AGC gain held constant by VEGC<br>Input impedance lowered<br>VCO locked to FREF | 1 | X | X | 0 | 1 |
| Power Shutdown | X | X | X | X | 0 |

## READ MODE

In the Read mode, the rising edge of DLYD DATA enables the phase detector while the falling edge is phase compared to the rising edge of the ÷N counter. As depicted in Figure 8, DLYD DATA is 1/4 cell wide (TVCO / 2 / N) pulse whose leading edge is defined by the leading edge of Read Data. RRC is generated from the rising edge of the ÷N counter output. The accuracy of the 1/4 cell delay only affects the retrace angle of the phase detector and does not influence the accuracy of RRC.

In the non-Read modes, the PLL is locked to FREF. This forces the VCO to run at a frequency which is very close to that required for tracking actual data and thus minimizes the associated frequency step during acquisition. When RG transitions, the VCO is stopped momentarily, then restarted in an accurate phase alignment with the next PLL reference input pulse. By minimizing the phase alignment in this manner (phase error $\leq 0.5$ rads), the acquisition time is substantially reduced.

With the PLL in lock, the encoded data bit is re-synchronized before output to the SRD pin. Figure 9 shows the Read mode timing.

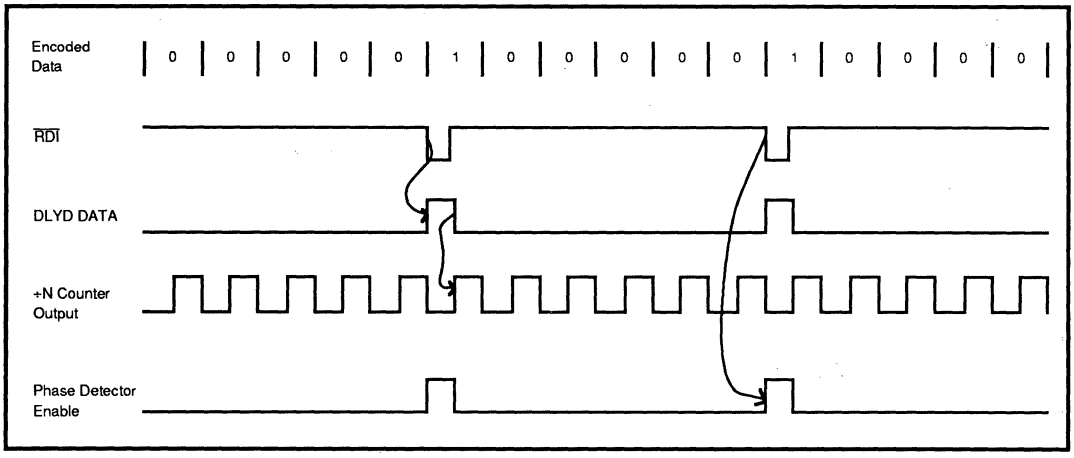


FIGURE 8: Data Sychronizer Timing

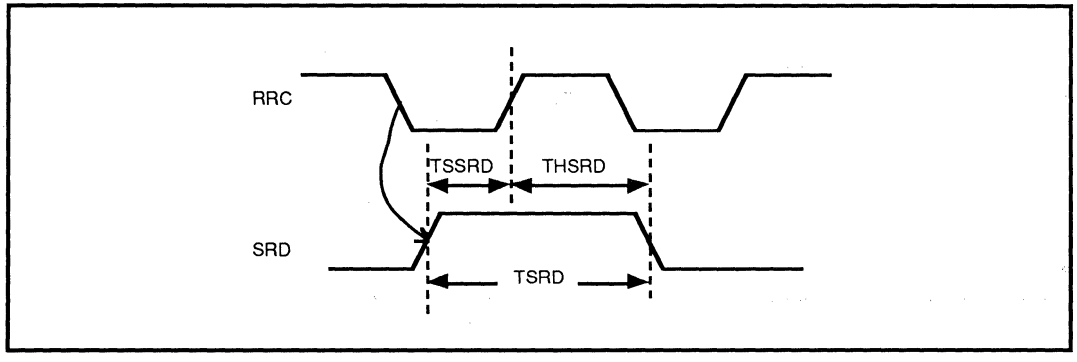


FIGURE 9: Read Mode Timing

## OPERATION MODES (continued)

### WRITE MODE

In the Write mode, the SSI 34P3200 pulse detector is disabled and preset for the subsequent Read mode. The digital circuitry is disabled, the input AGC amplifier gain is held at its previous value and the AGC amplifier input impedance is reduced.

Holding the AGC amplifier gain and reducing input impedance shortens system write-to-read recovery times.

The lowered input impedance improves settling time by reducing the time constant of the network between the SSI 34P3200 and a head preamplifier such as the SSI 32R1200R. Write-to-read timing is controlled to maintain the reduced impedance for TBD µs before the AGC circuitry is activated. Coupling capacitors should be chosen with as low a value as possible consistent with adequate bandwidth to allow more rapid settling.

Write Data Input can be re-synchronized to the Read Reference Clock before feeding to a write driver. Figure 10 shows the Write mode timing.

By a serial register bit control, the SSI 34P3200 can be placed in the write pass through mode. The synchronizer and the pre-comp function are disabled and act as a buffer only.

### POWER SHUTDOWN

For reduced power dissipation during non-operational periods, the SSI 34P3200 can be switched into a Sleep mode. The serial port registers must be reprogrammed immediately following 0-to-1 SLEEP transition.

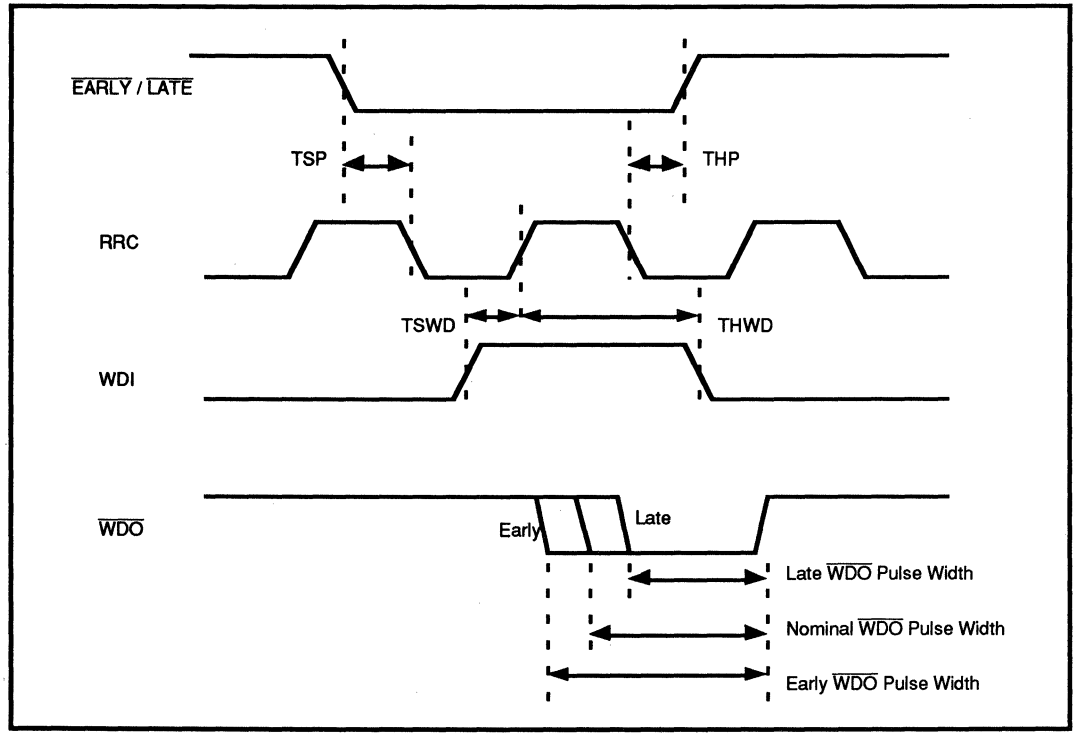


**FIGURE 10: Write Mode Timing**

## PIN DESCRIPTION

### ANALOG INPUT PINS

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| IN+, IN- | I | AGC amplifier inputs. |
| DIN+, DIN- | I | Data inputs to hysteresis comparator and full-wave rectifier. |
| CIN+, CIN- | I | Data inputs to time-channel qualification. |
| HYS | I | Hysteresis input to establish the hysteresis threshold of the data comparator. |
| AGC | I | The voltage at the AGC pin determines the nominal level at the DIN± pins. |
| BYP | I | The voltage at the BYP pin controls the AGC amplifier gain when $\overline{EGC}$ = 1. |
| VEGC | I | The voltage at the VEGC pin controls the AGC amplifier gain when $\overline{EGC}$ = 0. |

### DIGITAL INPUT PINS:

| | | |
|---|---|---|
| FREF | I | TTL reference clock input to data synchronizer. |
| OEN | I | TTL RDO Output Enable input: RDO enabled with OEN=1, RDO forced to 0 with OEN=0. |
| $\overline{RDI}$ | I | TTL external input source to the data synchronizer. |
| RG | | TTL Read Gate input. |
| WG | I | TTL Write Gate input. |
| WDI | I | TTL Write Data Input. |
| $\overline{EARLY}$ | I | TTL write precompensation control input to shift write data pulse early. |
| $\overline{LATE}$ | I | TTL write precompensation control input to shift write data pulse late. |
| $\overline{SLEEP}$ | I | TTL power shutdown control. The device is in power shutdown mode when $\overline{SLEEP}$ = 0. The device is in normal operational state when $\overline{SLEEP}$ = 1, or left open. |
| $\overline{HOLD}$ | I | TTL input that holds the AGC gain constant when pulled to 0. When left open, this input is at logic 1. |
| $\overline{EGC}$ | I | TTL input. When $\overline{EGC}$ = 0, the AGC amplifier gain is controlled by the voltage at VEGC.When $\overline{EGC}$ = 1, or left open, the AGC amplifier gain is controlled by the voltage at BYP. |
| SDI | I | TTL Serial Data Input. |
| SCLK | I | TTL Serial Clock. |
| SDEN | I | TTL Serial Data Enable. |

## PIN DESCRIPTION (continued)

### ANALOG OUTPUT PINS:

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| OUT+, OUT- | O | AGC amplifier emitter follower output pins. |
| LEVEL | O | Open emitter output from fullwave rectifier that may be used for input to the HYS pin. |
| FL0-4 | O | Loop filter connection pins. Either high impedance or low impedance state. |

### ANALOG CONTROL PINS:

| | | |
|---|---|---|
| DIF+, DIF- | - | Pins for external differentiating network. When off-chip differentiator is used, a TBDΩ resistor should be tied across DIF+ and DIF-. |
| IREF | - | Input reference current for VCO bias. A 7.5 kΩ resistor should be tied between IREF and VPA2. |
| FLTR | - | Loop filter pin. |
| WCS | - | Write precomp set: used to set the magnitude of the write pre-compensation time via an external capacitor Cp to VPA2 and an external resistor, Rp to AGND2. |

### DIGITAL OUTPUT PINS:

| | | |
|---|---|---|
| $\overline{\text{RDO}}$ | O | TTL output of the pulse detector read data. This output is enabled with OEN=1. It is forced to 0 with OEN=0. |
| RRC | O | Read Reference Clock: a multiplexed TTL clock source used by the controller. In the read mode, this clock is the encoded bit rate. In the write mode, it is the FREF divided down by the N factor. No short clock pulses are generated during a mode change. |
| SRD | O | Synchronized Read Data: a TTL read data that has been re-synchronized to read clock. |
| $\overline{\text{WDO}}$ | O | Write Data Output: a TTL output. |
| COUT | O | Time qualification one-shot test point: open emitter output which requires an external pull down resistor when used. |
| DOUT | O | Data comparator test point: open emitter output which requires an external pull down resistor when used. |
| DRD | O | Delay Read Data test point: open emitter output which requires an external pull down resistor when used. |
| VCO CLK | O | VCO test point: open emitter output which requires an external pull down resistor when used. |

**POWER & GROUND**

| NAME | TYPE | DESCRIPTION |
|---|---|---|
| VPA1 | - | Analog supply to the pulse detector section. |
| VPA2 | - | Analog supply to the data synchronizer section. |
| VPD | - | Digital supply. |
| AGND1 | - | Analog ground to the pulse detector section. |
| AGND2 | - | Analog ground to the data synchronizer section. |
| DGND | - | Digital ground. |

## ELECTRICAL SPECIFICATIONS

Unless otherwise specified, the recommended operating conditions apply.

**ABSOLUTE MAXIMUM RATINGS**

Operation beyond the maximum ratings may damage the device.

| PARAMETER | RATING |
|---|---|
| Storage Temperature | -65 to +150°C |
| Junction Operating Temperature | +130°C |
| Supply Voltage, VPA1-2, VPD | -0.7 to +7V |
| Voltage Applied to Inputs | -0.3 to Supply + 0.3V |

**RECOMMENDED OPERATING CONDITIONS**

| | |
|---|---|
| Supply Voltage | 4.5V < VPA1, VPA2, VPD < 5.5V |
| Ambient Temperature, Ta | 0°C < Ta < 70 °C |

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**POWER SUPPLY**

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| Power Dissipation Active | PD | Outputs unloaded<br>4.5V < VPA1, VPA2, VPD < 5.5V | | 500 | 800 | mW |
| Power Down Dissipation | PDS | Output unloaded; SLEEP- = 0 | | 3.5 | 7 | mW |

## ELECTRICAL SPECIFICATIONS (continued)

### LOGIC SIGNALS

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| TTL Input Low Voltage | VIL | | -0.3 | | 0.8 | V |
| TTL Input High Voltage | VIH | | 2 | | VCC + 0.3 | V |
| TTL Input Low Current | IIL | VIL = 0.4V | | | -0.4 | mA |
| TTL Input High Current | IIH | VIH = 2.7V | | | 0.1 | mA |
| TTL Input Switching Time | TS | 0.8V - 2.0V transition | | | 0.1 | µs |
| TTL Output Low Voltage | VOL | IOL = 4.0 mA | | | 0.5 | V |
| TTL Output High Voltage | VOH | IOH = -400 µA | 2.7 | | | V |
| Test Point Output High Voltage | VOHT | 261Ω to VPD, 420Ω to DGND | | VPA - 2.4 | | V |
| Test Point Output Low Voltage | VOLT | 261Ω to VPD, 420Ω to DGND | | VPA - 2.8 | | |

### MODE CONTROL

| | | | | | | |
|---|---|---|---|---|---|---|
| Read-to-Write Transition | TDRW | WG pin 0-to-1 | | | 1 | µs |
| Write-to-Read Transition | TDWR | WG pin 1-to-0; AGC settling not included | 0.5 | 0.9 | 1.3 | µs |
| HOLD- On to Off/Off to On Transition | TDH | HOLD- pin 1 to/from 0 transition | | | 1 | µs |
| Power shutdown mode to Read/Write Delay | TDSL | Settling time of external capacitor not included | | 0.1 | | µs |
| Read/Write Mode to power shutdown Delay | TDOFF | Settling time of external capacitor not included | | 10 | | µs |
| Low Input Impedance Pulse Width | PWIMS | WG pin 1-to-0. Not directly testable | | 0.9 | | µs |
| Fast Discharge Pulse Width | PWFDC | WG pin 1-to-0 following PWIMS. Not directly testable | | 0.9 | | µs |

### AGC AMPLIFIER

Unless otherwise specified, recommended operating conditions apply. Input signals, 100 mVppd at 1.0 MHz, are AC coupled to IN±. OUT± are AC coupled to DIN±.

A 2000 pF capacitor is connected between BYP and AGND1. AGC pin is open.

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| Minimum Gain Range | MIGR | 1.0Vppd ≤ OUT± ≤ 3.0Vppd | | | 4 | V/V |
| Maximum Gain Range | MAGR | | 80 | | | V/V |
| Output Offset Voltage Variation | VOS | Over entire gain range | -200 | 0 | 200 | mV |
| Maximum Output Voltage Swing | VOMX | Set by BYP pin | 3 | | | Vppd |
| Differential Input Impedance | RIN | IN± = 100 mVppd @ 1.0 MHz | | 5 | | kΩ |
| Differential Input Impedance | CIN | IN± = 100 mVppd @ 1.0 MHz | | | 10 | pF |
| Single Ended Input Impedance | ZCMH | WG = 0 IN+ = IN- | | 1.5 | | kΩ |
| | | WG = 1 IN+ = IN- | | | 250 | Ω |
| Input Noise Voltage | VIN | Gain set to maximum, BW = 15 MHz, short IN+ to IN- | | | 40 | nV/√Hz |
| Bandwidth | BW | Gain set to maximum referenced to 1.0 MHz | 15 | | | MHz |
| Single Ended Output Impedance on OUT± | ROUT | | | | 100 | Ω |
| Input Referred Common Mode Rejection | CMRR | IN+ = IN- = 100 mVpp @ 1.0 MHz gain set to maximum | 40 | | | dB |
| Input Referred Power Supply Rejection | PSRR | 1.0 mVpp @ 1.0 MHz on VPA1 gain set to maximum | 30 | | | dB |
| DIN± Input Swing vs AGC Input | KAGC | 25 mVppd ≤ IN± ≤ 250 mVppd ; HOLD- = 1Vppd/V 0.5 Vppd ≤ DIN± ≤ 1.5 Vppd | 0.7 | 1 | 1.3 | Vppd/V |
| DIN± Input Swing Variation with IN± | ΔDIN | 25 mVppd ≤ IN± ≤ 250 mVppd | | | 6 | % |
| AGC Open Voltage | VAGC | AGC open | 0.8 | 1 | 1.2 | V |
| AGC Pin Input Impedance | RAGC | | 2.5 | 3.8 | 6.0 | kΩ |
| Slow AGC Discharge Current | ISD | DIN± = 0V | 4 | 4.5 | 6 | μA |
| Fast AGC Discharge Current | IFD | Starts at 0.9 μs after WG 1-to-0 transition Stops at 1.8 μs after WG 1-to-0 transition | 0.08 | 0.12 | 0.16 | mA |
| AGC Leakage Current | ILK | HOLD- = 0 | -0.2 | 0 | 0.2 | μA |
| Slow AGC Charge Current | ISC | DIN± = 0.8 VDC vary AGC until slow charge begins | -0.12 | -0.18 | -0.24 | mA |
| Fast AGC Charge Current | IFC | DIN± = 0.8 VDC V @ AGC = 3.0V | -0.9 | -1.3 | -1.7 | mA |

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## ELECTRICAL SPECIFICATIONS (continued)

### AGC AMPLIFIER (continued)

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| Fast to Slow Attack Switchover Point | FSSP | DIN±(fast) / DIN±(slow) | | 125 | | % |
| Gain Decay Time | TGD | IN± = 250 mVppd to 125 mVppd @ 1.0MHz OUT± to 90% final value | | 12 | | µs |
| | | IN± = 50 mVppd to 25 mVppd @ 1.0 MHz OUT± to 90% final value | | 60 | | µs |
| Gain Attack Time | TGA | WG = 1 to 0 IN± = 250 mVppd @ 1.0 MHz OUT± to 110% final value | | 2 | | µs |

### HYSTERESIS COMPARATOR

Unless otherwise specified, recommended operating conditions apply. Input DIN± is AC coupled, 1.0 Vppd @ 1.0 MHz sinewave. 0.5 VDC is applied to the HYS pin. WG = 0

| | | | | | | |
|---|---|---|---|---|---|---|
| Input Signal Range | IRHC | | | | 1.5 | Vppd |
| Differential Input Resistance | RHCD | DIN± = 100 mVppd @ ≤ 2.0 MHz | 15 | 20 | 25 | kΩ |
| Differential Input Capacitance | CHCD | DIN± = 100 mVppd @ 2.0 MHz | | | 5 | pF |
| Single Ended Input Impedance | RHCC | DIN+ = DIN- | 4 | 5 | 6 | kΩ |
| Level Gain from DIN± to LEVEL | KLD | 0.6 Vppd ≤ DIN± ≤ 1.5 Vppd 10 kΩ from LEVEL to AGND1 | 0.75 | 1 | 1.25 | V/Vppd |
| Level Pin Output Offset Voltage | VLOS | DIN± = 0 Vppd; 10 kΩ from LEVEL to AGND1 | | 100 | | mV |
| Level Pin Output Impedance | ZLV | I @ LEVEL = -0.2 mA | | 700 | | Ω |
| Level Pin Maximum Output Current | ILMX | | 1.5 | | | mA |
| Hysteresis Gain | KHYS | 0.3V < HYS < 1.0 V | | 0.36 | | V/V |
| HYS Pin Current | IHYS | 0.5V < HYS < 1.5 V | 0 | | -10 | µA |
| Comparator Offset Voltage | VHCOS | HYS pin at AGND; < 1.5 kΩ across DIN+ to DIN- 0.5 kΩ from DOUT to DGND | | 5 | 15 | mV |

### ACTIVE DIFFERENTIATOR

Unless otherwise specified, recommended operating conditions apply. Input CIN± is AC coupled, 1.0 Vppd, 1.0 MHz sinewave.

100Ω resistor in series with 65 pF capacitor are tied across DIF+ to DIF-.

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| Input Signal Range | IRAD | | | | 1.5 | V |
| Differential Input Resistance | RADD | CIN± = 100 mVppd @ 2.0 MHz | 15 | 20 | 25 | kΩ |
| Differential Input Capcitance | CADD | CIN± = 100 mVppd @ 2.0 MHz | | | 5 | pF |
| Single Ended Input Impedance | RADC | CIN+ = CIN- | 4 | 5 | 6 | kΩ |
| Voltage Gain from CIN± to DIF± | KAD | 3.5 kΩ from DIF+ to DIF- | | 1 | | V/V |
| DIF+ to DIF- Pin Current | IDIF | Differentiator impedance must be set so as not to clip the signal for this current level | | 1.0 | | mA |
| Comparator Offset Voltage | VADOS | DIF± AC coupled | | 0 | 5 | mV |
| COUT Pin Output High Voltage | PWC | 5 kΩ from COUT to DGND | | 30 | | ns |

### QUALIFIER TIMING

Unless otherwise specified, recommended operating conditions apply. Inputs CIN± and DIN± are in-place as AC coupled, 1.0 Vppd, 1.0 MHz sinewave. 100Ω resistor in series with 65 pF capacitor are tied from DIF+ to DIF-. 0.5V is applied to the HYS pin.

$\overline{RDO}$ is enabled as output. OEN = 1. WG = 0

| | | | | | | |
|---|---|---|---|---|---|---|
| D Flip Flop Set Up Time | TD1 | Minimum allowable time delay from DIN± exceeding hysteresis point to DIF± hitting a peak value. | 0 | | | ns |
| Propagation Delay from Positive Peak to RDIO Pulse | TD3 | | | 20 | | ns |
| Propagation Delay from Negative Peak to RDIO Pulse | TD4 | | | 20 | | ns |
| Pulse Pairing Abs (TD3 - TD4) | PP | | | | 3 | ns |
| $\overline{RDO}$ Pulse Width | TRD | | 20 | 25 | 30 | ns |

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## ELECTRICAL SPECIFICATIONS (continued)

### SYNCHRONIZER SECTION

#### WRITE MODE

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| Write Data Input Setup Time to RRC | TSWD | Rising edge of WDI to rising edge of RRC | 15 | | | ns |
| Write Data Input Hold Time after RRC | THWD | Falling edge of WDI to rising edge of RRC | 3 | | | ns |
| EARLY-/LATE- Input Setup Time to RRC | TSP | Falling edge of EARLY- / LATE- to falling edge of RRC | 15 | | | ns |
| EARLY-/LATE- Input Hold Time after RRC | THP | Rising edge of EARLY- / LATE- to falling edge of RRC | 10 | | | ns |
| Precomp Time Shift Magnitude | TPC | TPC0 = 16 x $10^{-3}$ Rp | 0.8 x TPC0 | TPC0 | 1.2 TPC0 | ns |
| Write Data Output Pulse Width | TWD | CL ≤ 15 pF<br>To = Read Reference Clock Period | T0 -2TPC -12 | T0 -TPC | T0 + 12 | ns |
| Write Pass Through Delay from WDI to WDO | TPD | | | | 1 | µs |

#### READ MODE

| | | | | | | |
|---|---|---|---|---|---|---|
| Read Reference Clock Rise Time | TRRC | 0.8V to 2.0V; CL ≤ 15 pF | | | 8 | ns |
| Read Reference Clock Fall Time | TFRC | 2.0V to 0.8V; CL ≤ 15 pF | | | 5 | ns |
| Read Reference Clock Pulse Width | TWRC | To = Read Reference Clock Period | 0.5•To-10 | | 0.5•To+10 | ns |
| Read Data Pulse Width | TSRD | To = Read Reference Clock Period | To -2 | To | To+2 | ns |
| Read Data Rise Time | TRSRD | 0.8V to 2.0V ; CL ≤ 15 pF | | | 10 | ns |
| Read Data Fall Time | TFSRD | 2.0V to 0.8V ; CL ≤ 15 pF | | | 8 | ns |
| SRD Output Setup wrt RRC Rise | TSSRD | | 15 | | | ns |
| SRD Output Hold wrt RRC Rise | THSRD | | 15 | | | ns |

**DATA SYNCHRONIZATION**

| PARAMETER | | CONDITIONS | MIN | NOM | MAX | UNITS |
|---|---|---|---|---|---|---|
| VCO Center Frequency Period | TVCO | V@FLTR = 2.7V<br>Serial Reg 0 = X000 T1= 83 ns<br>Serial Reg 0 = X001 T1 = 111 ns<br>Serial Reg 0 = X010 T1 = 167 ns<br>Serial Reg 0 = Other T1 = 125 ns | 0.8 T1 | T1 | 1.2 T1 | ns |
| VCO Frequency Dynamic Range | VDR | 1.0V ≤ V @ FLTR ≤ VPA2 - 0.6V<br>VPA2 = 5V | ±24 | ±34 | ±45 | % |
| VCO Control Gain | KVCO | V @ FLTR = 2.7V; ωo = 2π/TVCO | 0.14 ωo | 0.20 ωo | 0.26 ωo | rad/s-V |
| Phase Detector Gain | KD | KD = 0.62/(RR + 527)<br>VPA2 = 5V (RR = 7.5K) | 0.83 KD | KD | 1.17 KD | A/rad |
| FL1-4 High Impedance | FLZH | | 2 | | | kΩ |
| FL1-4 Low Impedance | FLZL | | | | 100 | Ω |
| KVCO x KD Product Accuracy | KPA | | -28 | 0 | 28 | % |
| VCO Phase Restart Error | PRE | | | 4 | | ns |
| Decode Window | DW | To = Read Clock Period | To - 2 | To | | ns |
| Decode Window Center Accuracy | DWCA | | -5% To | | +5% To | ns |
| Decode Window Shift Magnitude | TS1 | Serial Register 1 = XX00 | | ±20% To | | ns |
| | TS2 | Serial Register 1 = XX01 | | ±15% To | | ns |
| | TS3 | Serial Register 1 = XX10 | | ±10% To | | ns |

**MISCELLANEOUS TIMING**

| | | | | | | |
|---|---|---|---|---|---|---|
| RG, WG Time Delay | RWTD | | | | 100 | ns |

**SERIAL PORT SECTION**

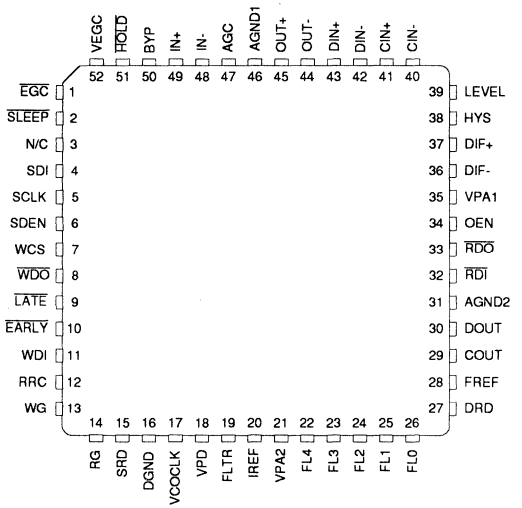
| | | | | | | |
|---|---|---|---|---|---|---|
| SCLK Period | TC | | 10 | | | µs |
| SDEN Setup to SCLK | TSP1 | | 1.5 | | TC/4 | µs |
| SDEN Hold after SCLK | TSP2 | | 1 | | TC/4 | µs |
| SDI Setup to SCLK | TSP3 | | 45 | | | ns |
| SDI Hold after SCLK | TSP4 | | 45 | | | ns |

9

# SSI 34P3200
# Pulse Detector & Data Synchronizer for High Density Floppy Storage

## PACKAGE PIN DESIGNATIONS

(Top View)




**52-Lead QFP**

CAUTION: Use handling procedures necessary for a static sensitive component.

**Advance Information:** Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.



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Section 10

# CUSTOM SOLUTIONS

## *SILICON SYSTEMS LEADS THE WAY DEVELOPING MIXED-SIGNAL CUSTOM PRODUCTS.*

This is a story about leadership. Silicon Systems is dedicated to taking the point in the creation of high-performance, application-specific custom, mixed-signal integrated circuits (MSICs®).

Such dedication means we bring a lot to the party. Including truly innovative analog, digital, and mixed analog/digital ICs. A full complement of mixed-signal CMOS, BiCMOS and Bipolar wafer fabrication processes, state-of-the-art automated design tools, production, assembly, test, and QA capability.

### No one's more experienced

Our nearly 20 years of successful IC design work makes us the most experienced engineering team in the MSICs field. Add it all up and you get a company that saves you time and money while delivering you the most sophisticated mixed-signal custom ICs you can get.

### Faster to market for mixed-signal applications

Whatever your mixed-signal design application, Silicon Systems gives you a competitive advantage. In communications, disk drives, other storage products, automotive control systems, or other analog/digital signal processing applications, you can depend on our technical know-how to do the job right and turn your design around faster.

### CMOS. Bipolar. Analog. Digital. We've done it

Our designers are an experienced bunch. They're uniquely able to take a look at your specific application problem and move quickly to the right IC solution.

Our team is particularly adept at identifying key issues such as power, cost and performance trade-offs. So we can gear our efforts toward delivering you an optimized solution, manufactured with the appropriate fab process.

| Technique | Application | Silicon Systems Designed Examples |
|---|---|---|
| CMOS Signal Processing | For analog continuous time and sampled data (switched-capacitor implementation) and digital signal processing (DSP) applications. Low-power capability also allows inclusion of ROMs, RAMs, and other analog/digital subsystems. | • 73K224 complete single-chip 2400 bit/s modem<br>• C301 single-chip telephone headset amplifier<br>• 14.4 kbit modem<br>• Direct-broadcast satellite descrambler<br>• Motor controllers<br>• High-resolution analog data acquisition |
| Bipolar Signal Processing | For high-performance, low noise, wideband signal acquisition and processing applications. Offers TTL and/or ECL logic interfaces with high current drive. | • Sub 1 nV/√Hz HDD R/W amplifiers<br>• AGC, pulse detection amplifiers<br>• High-speed data separators<br>• Wideband transceivers<br>• PLLs (phase locked loops)<br>• Optical signal processing |
| Digital CMOS | For ASIC controllers, sequencers and data path applications with on-board ROM, RAM, and PLA sub-systems. Offers standard TTL and/or CMOS logic interfaces. | • Hard disk drive controllers<br>• SCSI interface controllers<br>• UARTs<br>• Protocol controllers<br>• Digital signal processors |
| Digital Bipolar | High-speed logic and interface circuitry. Offers standard logic or custom interfaces. | • Encoders and decoders<br>• High-speed digital transceivers |

### The right mix of analog and digital

Providing total analog/digital systems on a chip allows you to meet your cost and performance objectives whether you're designing the next generation of communications devices, or perhaps an I/O multiplexer to control electronics in 21st century automobiles.

We've turned to CMOS to effectively implement low-power, highly integrated systems solutions for everything from modems and CATV satellite descramblers to hard disk drive controllers and digital signal processors.

We've gone the Bipolar route to meet the high-performance needs of products like wideband transceivers, R/W amplifiers, low-noise amplifiers, pulse detectors, high-speed data separators and high-performance, low-power combo devices.

Our BiCMOS technology promises to open up new horizons of product capability for applications demanding optimum performance at the lowest power.

## SOPHISTICATED TOOLS FOR A CUSTOM DESIGN

At each of five design centers capable of worldwide service — Tustin, Santa Clara and Nevada City, California; Tokyo and Singapore — Silicon Systems employs PEGASYS™, an internal design automation system developed from carefully selected vendor tools and our own proprietary software. Using Mentor Graphics workstations for both electrical and physical design, PEGASYS helps create complex designs while significantly reducing schedules, costs and errors.

By integrating such helpful third-party tools and custom software, we're better able to design and analyze mixed-signal integrated circuits in all CMOS, Bipolar and BiCMOS technologies. It's an approach that has given us the edge in mixed-signal design and helped put Silicon Systems' customers in a favorable position in the marketplace.

Specifically, PEGASYS brings the following to each design:

- Fully integrated design environment
- Methodology for precision circuit design
- Integrated physical design
- Automatic place and route
- Complete layout verification

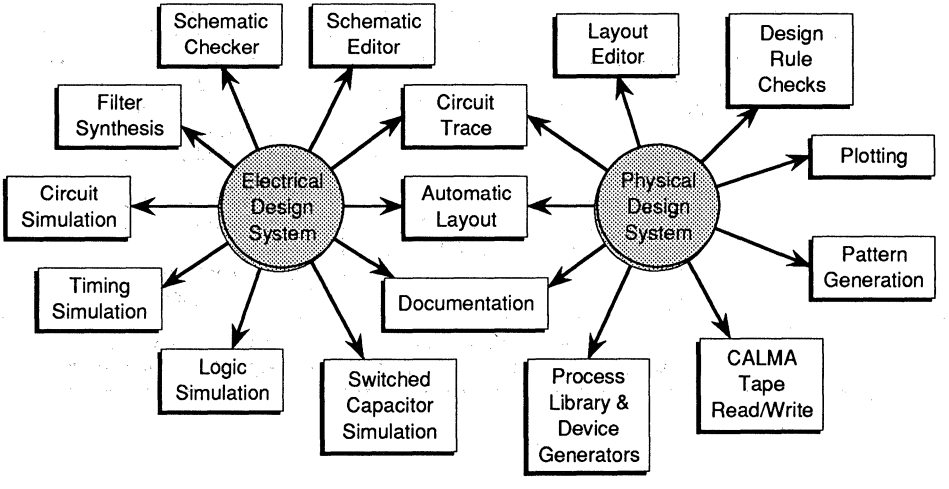
Our design automation staff integrates the third-party tools and optimizes their use on the Mentor platform. This framework can easily accommodate new tools when needed, and it enables us to support a combination of analog and digital design techniques in all CMOS, Bipolar and BiCMOS chip designs. By mixing design methodologies, we can achieve optimum systems performance, even when schedules are tight.

### Electrical design

A single CAE (computer aided engineering) environment provides for schematic capture, simulation, synthesis and documentation. We support this software with extensive libraries of pre-designed cells and components. Highly specialized cells or components can be designed and enhanced where required. We simulate each circuit to meet precise performance specifications using:

- Analog circuit simulation
- Digital logic simulation
- Timing simulation
- Mixed-mode simulation
- Switched-capacitor filter simulation
- Behavioral simulation

Admittedly, simulation alone is not the key to perfecting performance. That's why we work aggressively to refine our understanding of models to make them work with simulation. Inside our progressive device modeling and characterization



(DMC) laboratory, we develop accurate circuit simulation models and parameters. The DMC lab provides complete device model data for our processes using capabilities such as AC measurement, statistical analysis and worst-case modeling. Accurate models are a cornerstone of our design-for-quality approach.

### Physical design

Our PEGASYS layout system aids the mask designer through all physical design phases, ensuring consistency throughout the design cycle. This fully integrated environment provides for both full-custom design and automatic place-and-route design including these capabilities:

- Graphic editing
- On-line point-to-point routing
- Compaction
- On-line design rule checking
- Layout-to-schematic verification
- Parasitic extraction/back annotation
- Output in industry standard GDS format

The same physical design environment supports all processes and design methodologies.

### Automatic place & route software

The automatic place-and-route capability speeds through physical design far more rapidly than a full-custom, hand-drawn approach. We have combined Cadence Design Systems' TANCELL™, the most area-efficient router on the market, with our proprietary tools. This flexible environment allows for floor planning and automatic routing, and it supports the combination of custom cells, standard cells and compiled blocks.

### Layout-to-schematic trace and verification software

Our circuit-trace capability compares the completed IC layout to the schematic data base, using proprietary techniques and tools to guarantee quality. We help to eliminate layout errors through verification checks of both connectivity and component values. The resulting layout is an exact match of the schematic design. Further possible layout problems are identified during post-layout simulations using true parasitic modeling of capacitance and resistance interconnect. In short, all potential problems are fixed or addressed before first silicon fabrication.

### KADS. A mutual drive for custom design

The Silicon Systems Key Account Design Service (KADS) program is our way of designing and developing custom IC solutions in a high-level cooperative partnership with our customers.

The KADS approach introduces the best minds in your company to Silicon Systems' mixed-signal specialists. Together we work closely, freely exchanging each other's ideas and experience in order to inspire breakthrough technical achievements and raise quality and creativity to a new level.

## *WHERE PROCESS MEETS NEED: CMOS*

Silicon Systems offers two proven CMOS process technologies for creating low-power, highly integrated systems solutions. We use CH for 5V and12V applications and CG for 5V only needs. Both offer excellent analog performance. For a summary, see Table 1.

Our CH process achieves its higher (to 12V) operation via a DDD (double diffused drain) source/drain structure. This increases the S/D junction grading and breakdown voltage while lowering the associated junction capacitance.

The CH process also provides high quality, low voltage coefficient, precision poly-poly capacitors that support high performance switched-capacitor filtering and data conversion (A/D and D/A) circuits. Another important CH process feature for analog applications is found with our high Ω/▫ poly resistors. Their low voltage coefficient is important for low distortion, continuous time filters such as in anti-aliasing applications. Typical CMOS processes use unacceptable high-value well resistors, and do not provide poly-poly capacitors.

### Improved CMOS reliability

Silicon Systems boosts your system's reliability by incorporating a well ring into the CH process. This improves well tie-down and increases latchup immunity. For harsher environments such as motor drivers or the automobile, we use an epitaxial (epi) substrate to provide latchup immunity of more than 200 mA.

### CMOS CG. Low-power & high performance

Our CG CMOS process is specifically designed to support your 5V mixed-signal applications. Its smaller feature size (1.5μ, shrinkable to 1.2μ) allows for much higher levels of system integration, higher speed and lower power.

CG supports high performance analog circuitry with precision poly-poly capacitors as well as complex digital circuitry including DSPs, microcontrollers, data paths and memory.

For a cross-section view of the Silicon Systems CG CMOS process, see Figure 1.

## *BIPOLAR & BICMOS PROCESS TECHNOLOGIES*

Our bipolar MSICs take advantage of two high-performance Bipolar processes: BK (for 12V applications) and BN (for 5V applications). The BK analog/digital process achieves its higher voltage operation and improves lateral PNP transistor performance by using a lightly-doped epi layer.

In BK we provide deep N+ and P+ enhancement layers to reduce both collector series and base resistance. Our use of up-junction isolation gives us a major reduction in device area, when compared with that of typical junction isolated processes. Metal-poly capacitors with a nitride dielectric are used for improving capacitor reliability.

### BN. Low-power/ 8 Ghz Bipolar at 5 volts

A noteworthy feature of a minimum size BN process transistor is that it's only about 1/5th the size of a minimum size BK transistor. Because we employ full oxide isolation in BN, we can fabricate very fast, very small transistors and reduce sidewall capacitances. This supports not only high speed, but low power.

The BN process features high-performance NPN transistors to support mixing high-performance emitter coupled logic (ECL) with analog circuitry. To provide for strict TTL I/O compatibility, we use superior PtSi Schottky diodes.

The resulting speed and packing density allows you to effectively implement dense high-performance, low-power Bipolar analog/digital capability into your system designs.

For a feature-by-feature comparison of Silicon Systems' BK and BN Bipolar processes, see Table 3.

### BiCMOS process technologies

High performance NPNs and CMOS transistors highlight our BiCMOS process. They support mixing high performance analog circuitry with high density digital logic.

We greatly improve response speed through the use of silicided base components and S/D regions that decrease extrinsic resistances in both types of active components while reducing the emitter-base and gate-source (drain) space.

BiCMOS is virtually immune to CMOS latch-up due to retro-grade wells. The high drive capability of Bipolar and the low-power/high-density capability of CMOS combine to enhance design potential considerably. Full-featured, 3-volt designs are one such example.

| Process | Type | Application Voltage | BVDSS | Drawn Gate Length | Interconnect Pitches Poly 1 | Metal 1 | Metal 2 | Features |
|---|---|---|---|---|---|---|---|---|
| CH | Si-Gate, single metal, dual poly, PWell | 12V | 18V | 3.6μ | 5.8μ | 6.4μ | n/a | • DDD S/D structure<br>• Poly-poly capacitors<br>• Low-voltage coefficient<br>• High Ω /□ poly resistors<br>• Epi substrate option<br>• Buried well-ring |
| CG | Si-Gate, dual metal, dual poly, PWell | 5V | 7V | 1.5μ | 3.0μ | 4.5μ | 6.0μ | • DDD S/D structure<br>• Poly-poly capacitors<br>• Shrinkable to 1.2μ |

**TABLE 1: CMOS Process Chart**

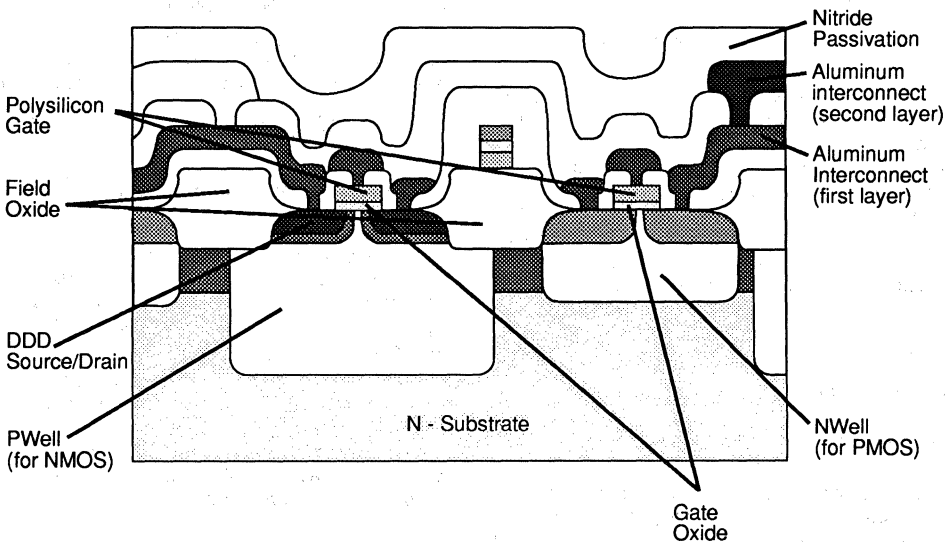



**FIGURE 1: CG CMOS Process Transistor**

| Type | Appl. Voltage | BVDSS | Drawn Gate Length | Interconnect Pitches Poly | M0 | M1 | M2 | $BV_{CEO}$ | NPN Ft | Emitter | Features |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Bipolar:**<br><br>Oxide isolated<br><br>**CMOS:**<br><br>Si-Gate, single poly, triple metal, PWell | 5V | 10V | 1.0μ | 2.6μ | 3.2μ | 3.8μ | 5.0μ | 8V | 13 GHz | 1.0μ | **Bipolar:**<br><br>•High Perf. NPNs<br>•PtSi Schottky Diodes<br>•Gate Oxide Capacitors<br>•Poly Capacitors<br>•Sidewall Oxide Isolation<br>•Fuses<br><br>**CMOS:**<br>•Lightly Doped Drains |

**TABLE 2: BiCMOS Process Chart**

| Process | Type | $BV_{CEO}$ | NPN Ft | Emitter Size | M1 Pitch | M2 Pitch | Features |
|---|---|---|---|---|---|---|---|
| BK | Junction-isolated | 12V | 2 GHz | 2.5μ | 9.0μ | 14.0μ | • Polysilicon emitters<br>• Al Schottky diodes<br>• Nitride capacitors<br>• Ion implanted resistors<br>• Up/down junction isolation<br>• Collector/base plugs |
| BN | Oxide-isolated | 6V | 8 GHz | 2.0μ | 4.5μ | 8.0μ | • High performance NPNs<br>• PtSi Schotty diodes<br>• Nitride capacitors<br>• Ion implanted resistors<br>• Sidewall oxide isolation<br>• Collector/base plugs |

**TABLE 3: Bipolar Process Chart**

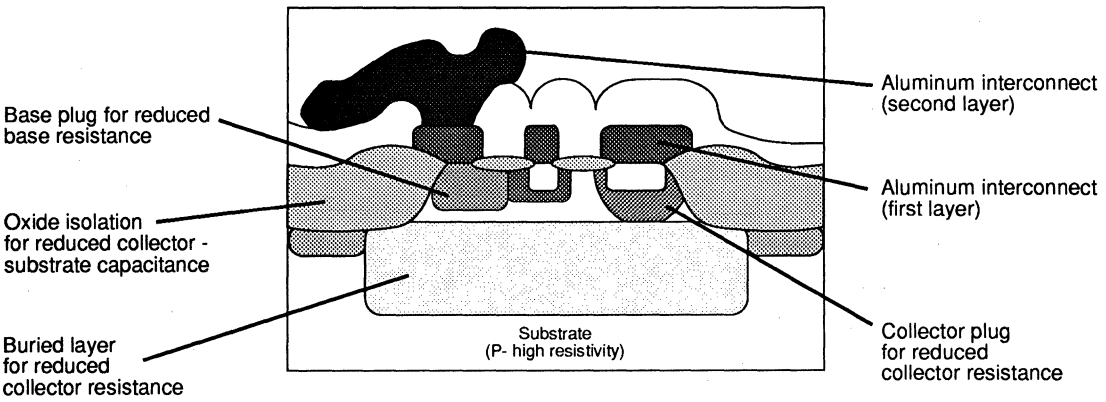



**FIGURE 2: BN Bipolar Process NPN Transistor**

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## A SUPERIOR FINISH FOR CMOS, BIPOLAR AND BICMOS

You might say this is the payoff window. The benefits of our process technologies, design tools and our unique custom approach all come together during wafer fabrication, test and assembly.

Our two manufacturing centers, located in Tustin and Santa Cruz, California, can offer specialized capabilities to match your particular fabrication requirements. Both facilities provide you with high resolution stepper photolithography technology, positive resist, dry plasma etch systems, high current ion implantation and automatic sputtering.

Fabrication sites in both Tustin and Santa Cruz accommodate 4- and 6-inch wafer fabrication and Bipolar, CMOS and BiCMOS processes.

### The right package

Silicon Systems offers a wide range of packages to meet the small footprint requirements of advanced storage and communication products. We continue to be innovative in surface mount technology by providing PLCC, SO, VSOP, SSOP, QFP, TQFP and VTQFP packages. At our Singapore assembly & test facility we have the full capability to support high quality automated packaging while also maintaining rapid cycle times.

### Promis. Quality through CAM

Process and Management Information System (PROMIS) underscores our commitment to computer-aided manufacturing (CAM). And to delivering you a superior quality product on time.

We use PROMIS to facilitate the data required in our manufacturing, monitoring and statistical process control (SPC) systems.

With PROMIS we more effectively manage our inventory, accurately track wafers in process, and closely monitor the clean room environment.

PROMIS also assists our SPC efforts, as does our commitment to fully train all of our manufacturing personnel in SPC basics.

### We design for quality

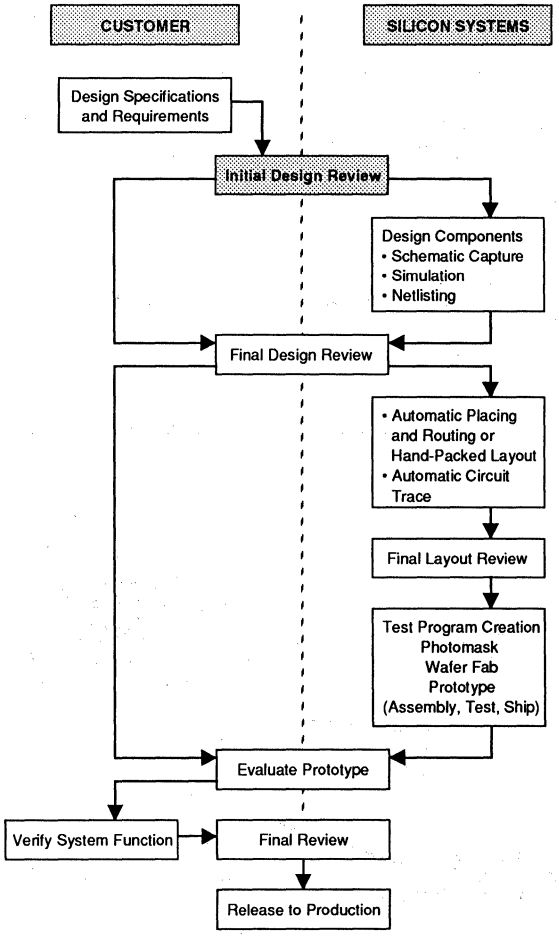
It's our view that quality is nothing less than absolute customer satisfaction. To achieve it, we begin far "upstream" in the product development process. Our design-for-quality approach scrutinizes the design itself with statistically based models, comprehensive simulation tools and vigorous design reviews.

The results of such an effort are IC products that boast lower defect rates, higher parametric performance and far fewer redesigns. Moreover, our persistence in improving quality keeps us focused on finding better and faster ways to satisfy future customer demands.

### Quality that delivers

With effective systems such as PROMIS and our design-for-quality approach in place, Silicon Systems is prepared to deliver you finished products you can really depend on. On time. And within budget.

For details on how you can take best advantage of Silicon Systems' custom mixed-signal IC solutions, see your nearest Silicon Systems representative, or contact us. Silicon Systems, Inc. 14351 Myford Road, Tustin, CA 92680. 714-573-6000. FAX: (714) 573-6914.




**CUSTOMER INTERFACE FOR FULL-CUSTOM AND CELL-BASED DESIGNS**

Section 11

# RELIABILITY & QUALITY ASSURANCE

# CONTINUOUS IMPROVEMENT MISSION & OBJECTIVE STATEMENT

## Mission

Be the supplier of choice by exceeding customer expectations through continuous improvements in our products, systems and services.

## Objectives

Provide world class quality in our products and services through focus on:

Customer Partnering
Cycle Time Improvement
Process and System Improvements

Develop a culture that ensures the consistent use of continuous improvement tools and fact based decision methodology by:

Senior Management Leadership
Employee Empowerment
Aggressive Goal Setting and Performance Measurement
Communication and Celebration of Successes

Alan V. King
President, CEO

Cheryl A. Stock
Vice President, Corporate R&QA

Silicon Systems®
A TDK Group Company

## SECTION 1

### 1.1 INTRODUCTION

Silicon Systems is committed to the goal of customer satisfaction through the on-time delivery of defect free products that meet the customer's expectations and requirements. This section outlines Silicon Systems' ongoing activities for the control and continual improvement of quality in every aspect of our organization.

Silicon Systems is diligently working to maintain and improve its position as a world-class provider of mixed-signal integrated circuits (MSICs®).

We realize and practice the concept that quality and reliability must be designed and built into our products. In addition, Silicon Systems utilizes rigid inspections and data analysis to evaluate the acceptability and variation existing in incoming materials and performs stringent outgoing quality verification. The manufacturing process flow is encompassed by an effective system of test/inspection checks and in-line monitors which focus on the control and reduction of process variation. These gates and monitors ensure precise adherence to prescribed standards and procedures.

Silicon Systems also incorporates the use of statistical process control techniques into company operations. The control and reduction of the process variation by the use of statistical problem solving techniques, analytical controls and other quantitative methods ensures that Silicon Systems' products maintain the highest levels of quality and reliability.

Our Reliability and Quality Assurance organizations are committed to working closely with our customers to provide assistance and a continually improving level of product quality.

### 1.2 SILICON SYSTEMS' QUALITY MANDATE: CONTINUOUS IMPROVEMENT

Continuous improvement is Silicon System's strategic thrust for the 1990's. In order to ensure that all aspects of our business are encompassed by this mandate, Corporate Reliability & Quality Assurance has been chartered with the responsibility for developing, educating and overseeing the worldwide continuous improvement process. The continuous improvement initiative will lead to developing a new organizational culture, changing attitudes and stronger ownership and accountability for total customer satisfaction.

### 1.3 CHARACTERISTICS OF SILICON SYSTEMS' CONTINUOUS IMPROVEMENT PROCESS

- Executive Steering Committee leadership and direction - defines the right things to do and provides guidance - the right way to do them.
- Continuous improvement is measured everywhere and by everyone. Metrics that reflect pride in accomplishment are celebrated.
- Benchmarking is employed as a method to shorten learning curves and ensure successful ventures.
- Quality management and employee empowerment are encouraged at all levels.

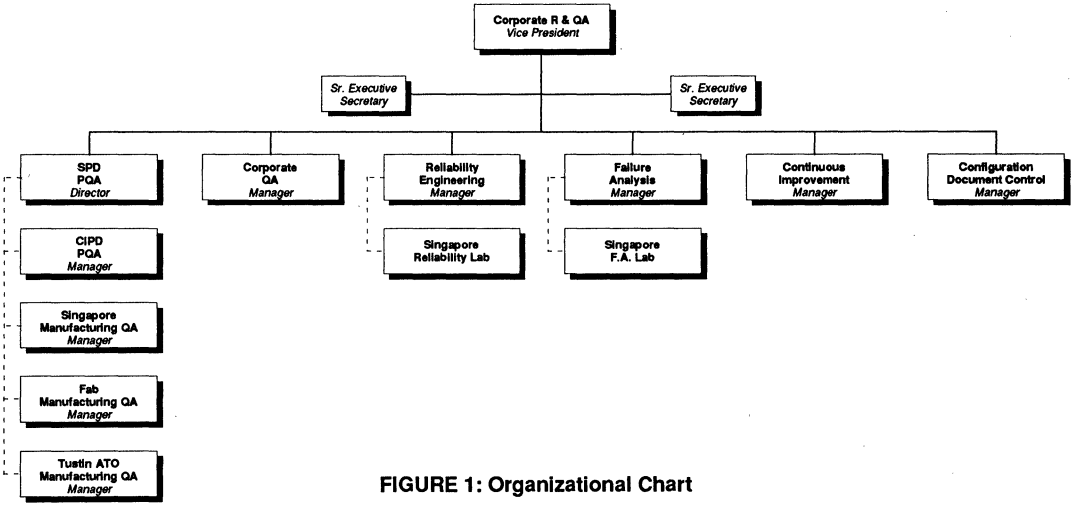



**FIGURE 1: Organizational Chart**

- Supplier partnership is a critical element of our quality strategy.

This is the essence of Silicon Systems - a total quality involved company - forward looking and immersed in the goal of customer satisfaction and best-in-class business pursuits.

### 1.4 CORPORATE RELIABILITY AND QUALITY ASSURANCE

It is the objective of the Corporate Reliability and Quality Assurance organization to ensure that proactive quality systems are in place to ensure that Silicon Systems' products will meet or exceed customer requirements and expectations. In addition, the Reliability and Quality Assurance organization works to facilitate the timely implementation of solutions and monitors the effectiveness of corrective actions. These organizational strategies support the continuing enhancement of quality consciousness throughout Silicon Systems.

## SECTION 2: QUALITY ASSURANCE

### 2.1 QUALITY OBJECTIVES

While all Silicon Systems employees have direct responsibility for quality in their functions, the Quality Assurance Organizations have the ultimate responsibility for the reliable performance of our products. This is accomplished through the development, administration and assessment of formal quality systems which assure Silicon Systems' management, as well as our customers, that products will fulfill the requirements of customer purchase orders and all other specifications related to design, raw material and in process through completion of the finished product.

Corporate Quality Assurance supports, coordinates and actively participates in the formal qualification of suppliers, material, processes, and products, and the administration of quality systems and production monitors to assure that our products meet Silicon Systems quality standards. Product Quality Assurance provides the liaison between Silicon Systems and the customer for all product quality related concerns.

It is the practice of Silicon Systems to have corporate quality and reliability objectives encompass all of its activities. This starts with a strong commitment of support from the corporate level and continues with exceptional customer support long after the product has been shipped.

Silicon Systems emphasizes the belief that quality and reliability must be built into all of its products by ensuring that all employees are educated in the quality philosophy of the company. Some of the features built into Silicon Systems quality culture include:

1. Structured training programs directed at wafer fabrication, test, process control personnel and supporting organizations.
   - Team based problem solving methodologies.
   - Corporate-wide training of quality philosophy and statistical methods.
2. Stringent in-process inspection, gates, and monitors.
3. Rigorous evaluation of designs, materials, and processing procedures.
4. Stringent electrical testing (100% and QC AQL/Sample testing).
5. Ongoing reliability monitors and process verifications.
6. Real-time use of statistical process control methodology.
7. Corporate level audits of manufacturing, subcontractors, and suppliers.
8. Timely corrective action system.
9. Control of non-conforming material.

These focused quality methods result in products which deliver superior performance and reliability in the field.

#### 2.2.1 INCOMING INSPECTIONS

Incoming inspection plays a key role in Silicon Systems' quality efforts. Small variations in incoming material can traverse the entire production cycle before being detected much later in the process. By paying strict attention to the monitoring of materials at the earliest possible stage, variation can be reduced, resulting in a stable uniform process.

#### 2.2.2 IN-PROCESS INSPECTIONS

Silicon Systems has established key inspection monitors in such strategic areas as wafer fabrication, wafer probe, assembly, and final test. These quality monitoring tests are performed in addition to the intermediate and final inspections found in the manufacturing process.

Quality control monitors have been integrated throughout the manufacturing flow, so that data may be collected and analyzed to verify the results of intermediary manufacturing steps. This data is used to document quality trends or long term improvements in the quality of specific operations. Abnormality control is being used to enhance the effectiveness of this process. In process monitors such as oxide integrity, electromigration immunity and other parameters monitor long term reliability as well as circuit performance.

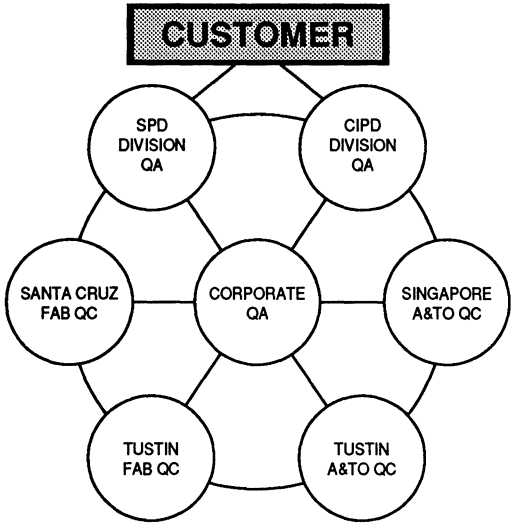



**FIGURE 2**
**Quality Assurance Relationships**
**Quality Steering Committee**

### 2.3 QUALITY STEERING COMMITTEE

The Corporate, Product and Manufacturing Quality Assurance organizations work closely together to provide leadership in the development, integration and assessment of Silicon Systems' worldwide quality systems and procedures.

This team approach ensures that policies and procedures are standardized and facilitates rapid improvement in products, processes and services.

### 2.4 DESIGN FOR QUALITY

Since the foundation of a reliable product is rooted in the design process, the Reliability and Quality Assurance organizations actively participate in comprehensive cross-functional reviews of design stages prior to the product's transition to production status. These review stages assure a predictable and effective development cycle. Other important design-related functions include ensuring that process specification revisions are translated into updated design parameters and the translation of manufacturing process capability into design guidelines. This is accomplished through the identification and monitoring of critical process and device parameters. Wafer level test at the early stages of process development also plays a critical role. These elements, included in Silicon Systems design for quality effort, support the development of robust design rules which are as insensitive as possible to inherent manufacturing variation. The result is a product that delivers predictable and reliable long term performance.

### 2.5 PPM REDUCTION PROGRAM

The primary purpose of a PPM reduction program is to provide a formalized feedback system in which data from nonconforming products can be used to improve future product consistency and reliability. The action portion of this program is accomplished in three stages:

1. Identification of defects by failure mode.
2. Identification of defect causes and initiation of corrective action.
3. Measurement of results and setting of improved goals.

The data summarized from the established PPM program is compiled as a ratio of units rejected/tested. This ratio is then expressed in terms of defective parts per million (PPM). Founded on a statistically valid database of PPM data and an established five-year strategic plan identifying PPM improvement goals, Silicon Systems has consistently achieved excellent quality standards and will continue to progressively improve PPM standards.

### 2.6 COMPUTER AIDED MANUFACTURING CONTROL

Computer Aided Manufacturing (CAM) is used throughout Silicon Systems for the identification, control, collection and dissemination of timely information for logistics control. Silicon Systems also uses this type of computerized system for statistical process control and manufacturing monitoring. PROMIS, (PROcess Management and Information System), displays approved/controlled recipes, processes, and procedures; tracks work-in-process; reports accurate inventory information; allows continuous recording of facilities data; contains statistical analysis capabilities; and much more. PROMIS allows for a paperless facility, a major element in minimizing contamination of clean room areas.

| TEST | CONDITIONS | PURPOSE OF EVALUATION |
|---|---|---|
| Biased temperature/humidity | 85°C/85% RH | Resistance to high humidity with bias |
| Highly accelerated stress test (HAST) | JDEC A110 | Evaluates package integrity |
| High temperature operating life (HTOL) | Mil 883D, Method 1005 | Resistance to electrical and thermal stress |
| Early Failure Rate | Mil 883D, Method 1005 | Detect infant mortality |
| Steam pressure | 121°C/15PSI | Resistance to high humidity |
| Temperature cycling | Mil 883D, Method 1010 | Resistance to thermal excursion (air) |
| Thermal shock | Mil 883D, Method 1011 | Resistance to thermal excursion (liquid) |
| Salt atmosphere | Mil 883D, Method 1009 | Resistance to corrosive environment |
| Constant acceleration | Mil 883D, Method 2001 | Resistance to constant acceleration |
| Mechanical shock | Mil 883D, Method 2002 | Resistance to mechanical shocks |
| Solderability | Mil 883D, Method 2003 | Evaluates solderability of leads |
| Lead integrity | Mil 883D, Method 2004 | Evaluates lead integrity before board assembly |
| Vibration, variable frequency | Mil 883D, Method 2007 | Resistance to vibration |
| Thermal resistance | Silicon Systems Method | Evaluates thermal dissipation |
| Electrostatic damage | Mil 883D, Method 3015 | Evaluates ESD susceptability |
| Latch-up | Silicon Systems Method | Evaluates latch-up susceptibility |
| Seal fine and gross leak | Mil Std 883D, Method 1014 | Evaluates hermeticity of sealed packages |

**TABLE 1: Reliability Stress Tests**

## SECTION 3: RELIABILITY

### 3.1 RELIABILITY PROGRAM

Silicon Systems has defined various programs that will characterize product reliability levels on a continuous basis. These programs can be categorically described by:

1. Qualifications
2. Production monitors
3. Evaluations
4. Failure analysis
5. Wafer level reliability
6. Data collection and presentation for improvement projects

### 3.2 QUALIFICATIONS

Extensive qualification testing and data collection ensures that all new product designs, processes, and packaging configurations meet the absolute maximum ratings of design and the worst case performance criteria for end users. A large database generated by means of accelerated stress testing results in a high degree of confidence in predicting final use performance. The qualification criteria used are periodically reviewed to be consistent with Silicon Systems' increasing quality and reliability goals in support of our customers.

### 3.3 PRODUCTION MONITORS

This program has been established to randomly select a statistically significant sample of production products for subjection to maximum stress test levels in order to evaluate the useful life of the product in a field use environment.

Table 1 lists reliability test methods that are in use at Silicon Systems. This analysis of production monitor at Silicon Systems provides valuable information on possible design/process changes which assure continued improved reliability. The monitors are periodically reviewed for effectiveness and improvements.

### 3.4 EVALUATIONS

The evaluation program at Silicon Systems is an ongoing effort that will continue defining standards which address the reliability assessment of the circuit design, process parameters, and package of a new product. This program continuously analyzes updated performance characteristics of product as they undergo improvement efforts at Silicon Systems.

### 3.5 FAILURE ANALYSIS

The failure analysis function is an integral part of the Quality and Reliability department at Silicon Systems. Silicon Systems has assembled a highly technical and sophisticated failure analysis laboratory and staff. This laboratory provides visual analysis, electrical reject mode analysis, and both

destructive and non-destructive data to aid the engineers in developing corrective action for improvement. These test analyses may include metallurgical, optical, chemical, electrical, SEM with X-ray dispersive analysis, and E-Beam non-contact analysis as needed.

These conclusive in-house testing and analysis techniques, are complemented by outside support, such as scanning acoustic microscopy, focused ion beam, and complete surface and material analysis. This allows Silicon Systems to monitor all aspects of product manufacturing to ensure that the product of highest quality is shipped to our customers.

### 3.6 WAFER LEVEL RELIABILITY PROGRAM

A primary objective at Silicon Systems is to improve the reliability of our products through characterization of our manufacturing operations. The identification of specific failure mechanisms occuring in the wafer fabrication and assembly processes is a prerequisite to effective corrective action aimed at reducing defects and improving quality and reliability.

The primary advantage of wafer level reliability testing is the speed at which results can be derived, thereby providing additional response time and an early warning of process changes. This tool provides Silicon Systems with a very rapid analysis tool which allows for the early identification of possible problems and a determination of their origin.

The continuous improvement approach taken at Silicon Systems uses the wafer level reliability tests as tools to improve the process, identify potential problems, determine the sources of any process weakness and eliminate problems upstream in the process. This results in a focus on reliability improvement that goes well beyond merely determining the projected lifetime of a product to a detailed characterization, measurement and control of the specific parameters which actuallly determine product lifetime.

### 3.7 DATA COLLECTION AND PRESENTATION FOR IMPROVEMENT PROJECTS

Data collected from each element of the Reliability program is summarized for scope and impact and distributed among all engineering disciplines in the company. This data facilitates improvement and provides our customers an opportunity to review the performance of our product.

### 3.8 RELIABILITY METHODS

The Reliability Program utilizes a number of stress tests that are presently being used to define performance levels of our products. Many of these stress tests are per MIL-STD-883D as shown in Table 1.

### 3.9 RELIABILITY PREDICTION METHODOLOGY

At Silicon Systems, the Arrhenius model is used to relate a failure rate at an accelerated temperature test condition to a normal use temperature condition.

The model basically states $FR = A \exp(-Ea/KT)$

Where:

- FR = Failure rate
- A = Constant
- Ea = Activation Energy (eV)
- K = Boltzmann's constant $8.62 \times 10^{-5}$ eV/ degree K
- T = Absolute temperature (degree K)

## SECTION 4: ELECTROSTATIC DISCHARGE PROGRAM

### 4.1 ESD PREVENTION

Silicon Systems recognizes that the protection of Electrostatic Discharge (ESD) sensitive devices from damage by electrical transients and static electricity is vital. ESD safe procedures are incorporated throughout all operations which come in contact with these devices. Continuous improvement in the ESD protection levels is being accomplished through the incorporation of increasingly robust protection devices during the circuit design process as well as work area improvements.

Silicon Systems' quality activity incorporates several protection measures for the control of ESD. Some of the preventive measures include handling of parts at static safe-guarded workstations, the wearing of wrist straps during all handling operations, the use of conductive lab coats in all test areas and all areas which handle parts and the packaging of components in conductive or anti-static containers.

**NOTES**

Section 12

# PACKAGING/ORDERING INFORMATION

# Silicon Systems
## Packaging Index



SON is a 150 mil width package.

SOL is a 300 mil width package.

SOW is a 400 mil width package.

SOM is a 300 mil width package, fine pitch (0.8mm).

SOV is a 220 mil width package, fine pitch (0.65mm).

Ordering Information
Optional
SSI NNA NNNN A AA - N A AA A
SHIPPING OPTIONS
R Tape and Reel
PRODUCT CATEGORY
32B HDD Interface
32C HDD Controller
32D HDD Data Recovery
32F Electronic Filter
32H HDD Head Positioning
32M HDD Motor Speed Controller
32P HDD Pulse Detection
32R HDD Read/Write Amp
34B FDD Interface
34D FDD Data Recovery
34P FDD Pulse Detection
34R FDD Read/Write Amp
35P Tape Drive Pulse Detection
66F Standard Automotive Products
67F Standard Automotive Products
73D Modem Device Set
73K K-Series Modem
73M Modem/Modem Support
75T Tone Signalling
78A Analog Telecom
78P Digital Telecom
78Q LAN Products
DEVICE TYPE 3 or 4 Digits
RELEASE LEVEL (Revision) A through E
NUMBER OF CHANNELS
PACKAGE TYPE
C Side-Brazed Ceramic
F Flatpack
G QFP, Quad Flatpack (2.5 mm height)
GT TQFP, Thin Quad Flatpack (1.4 mm height)
GV Very Thin Quad Flatpack (1.0 mm height)
H PLCC
P Plastic Dip
T Metal Can
S Plastic, Skinny Dip
N Small Outline, Narrow (150 mil.)
L Small Outline, Large (300 mil.)
W Small Outline, Wide (400 mil.)
M Small Outline, (300 mil.), Fine Pitch (0.8 mm)
V Very Small Outline (220 mil.) Fine Pitch (0.65 mm)
VT Very Thin Small Outline (1.0 mm height)
MODIFIERS
F FAX Capability
J Burn-In (168 Hours)
K Burn-In (48 Hours)
L Low Power
LP AT Commands, MNP5
LT AT Commands
LV AT Commands, MNP5, V.42
LZ AT Commands, MNP5, V.42, V.42bis
M Mirror Image
S Serial Version
SL Low Power Serial
R Damping Resistor
RM Resistor, Mirror Image
T 100 V/V Read Mode Gain (R/W)
U 150 V/V Read Mode Gain (R/W)
V 200 V/V Read Mode Gain (R/W)
W 250 V/V Read Mode Gain (R/W)
X 300 V/V Read Mode Gain (R/W)
Y 350 V/V Read Mode Gain (R/W)
Z 400 V/V Read Mode Gain (R/W)
Cannot use A-E in left position
TEMPERATURE RANGE
C Commercial (0 °C to +70 °C)
I Industrial (-40 °C to +85 °C)

# Package Information
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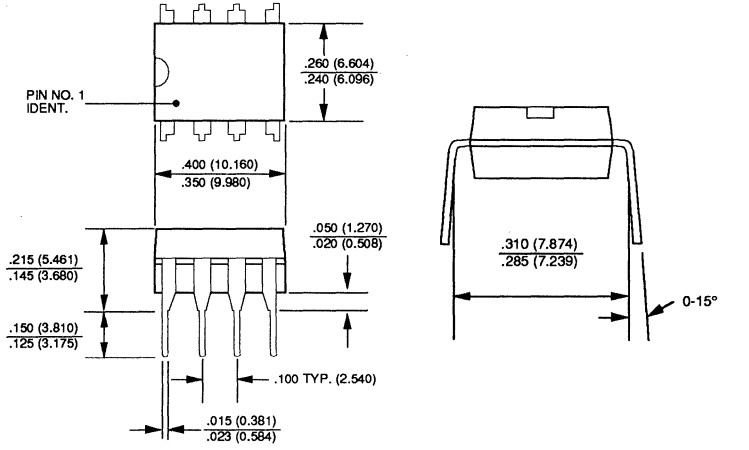
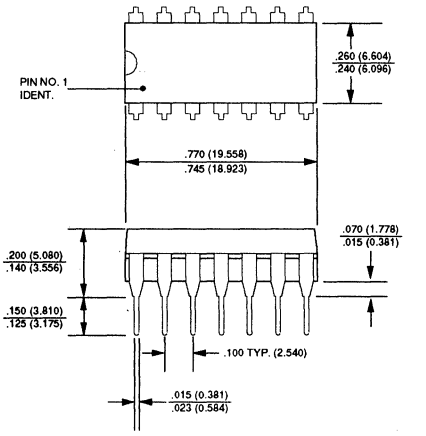
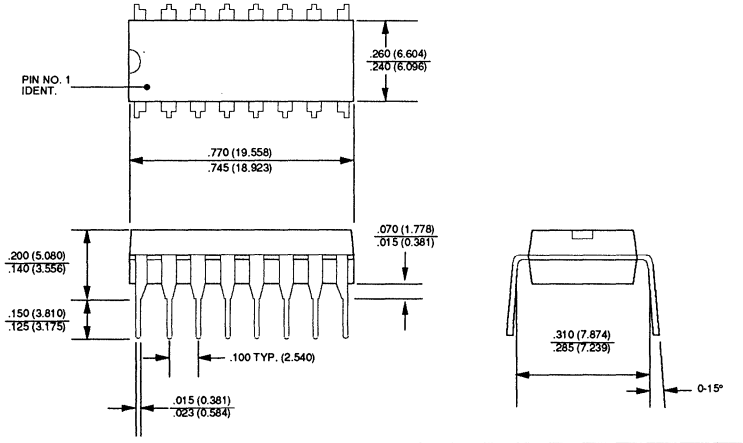


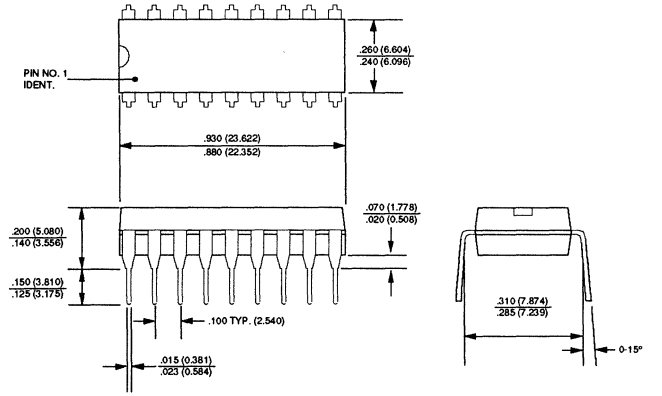

**8-Pin Plastic**




**14-Pin Plastic**

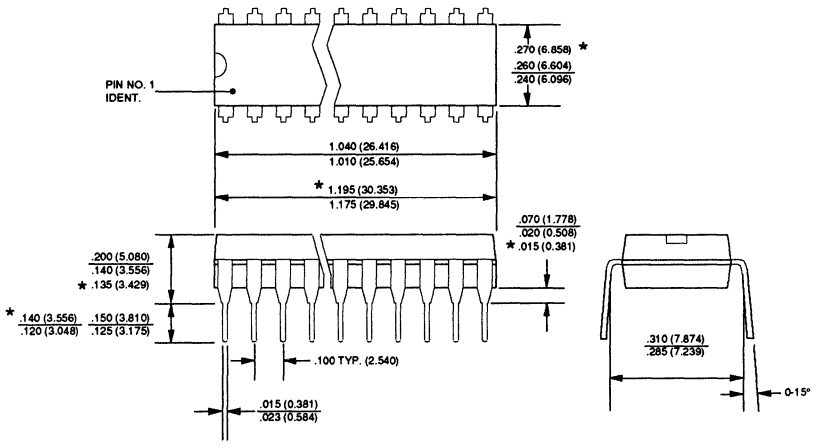



**16-Pin Plastic**

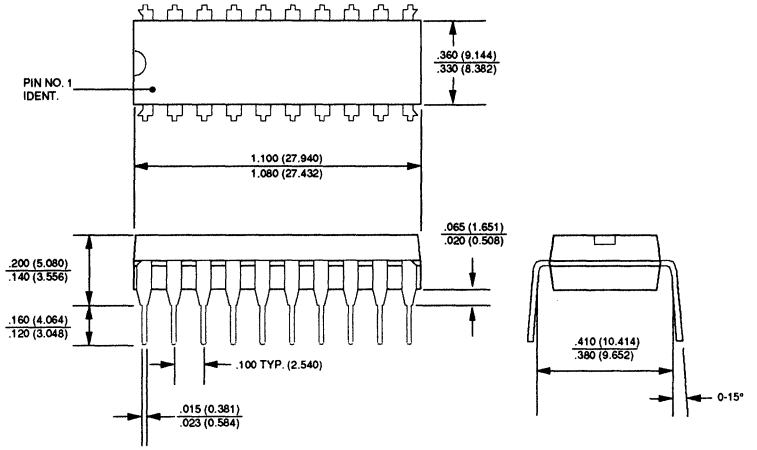



**18-Pin Plastic**

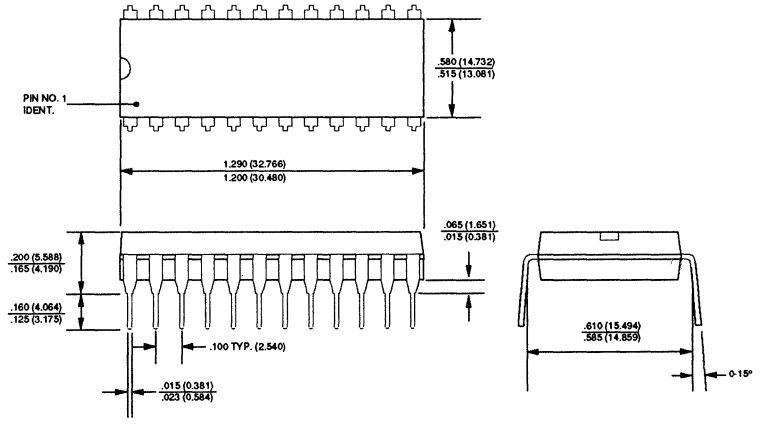
# Package Information




**20 Pin Plastic**
***24S Pin Plastic**



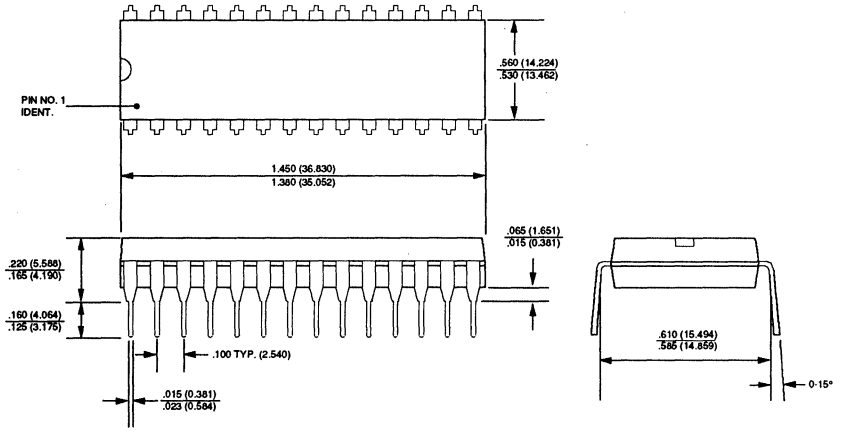

**22-Pin Plastic**



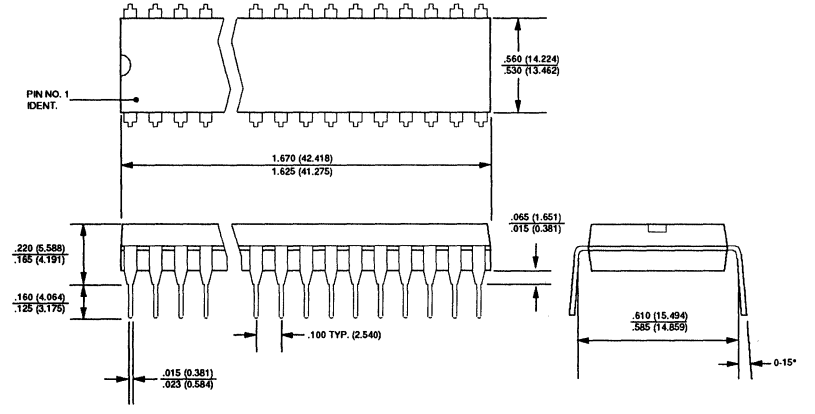

**24-Pin Plastic**

12

# Package Information




**28-Pin Plastic**

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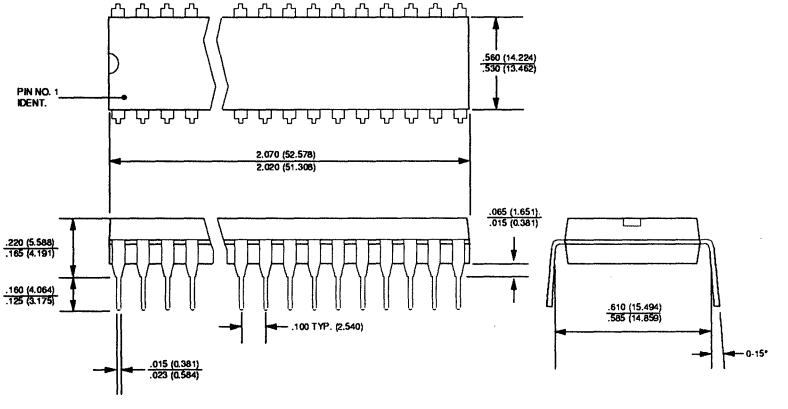
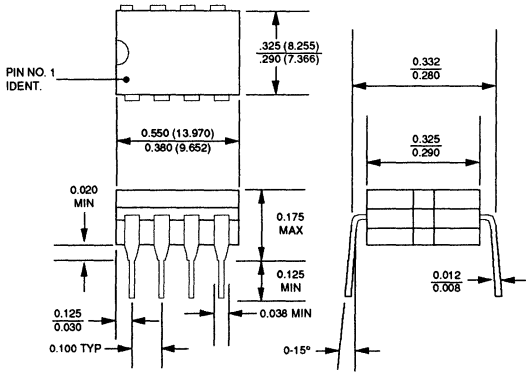
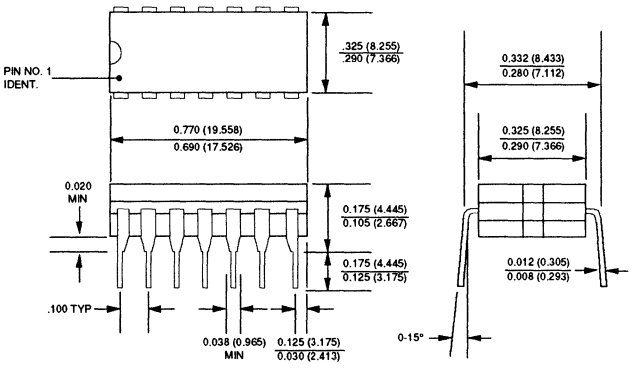



**40-Pin Plastic**

# Package Information
# Cerdip




**8-Pin Cerdip**

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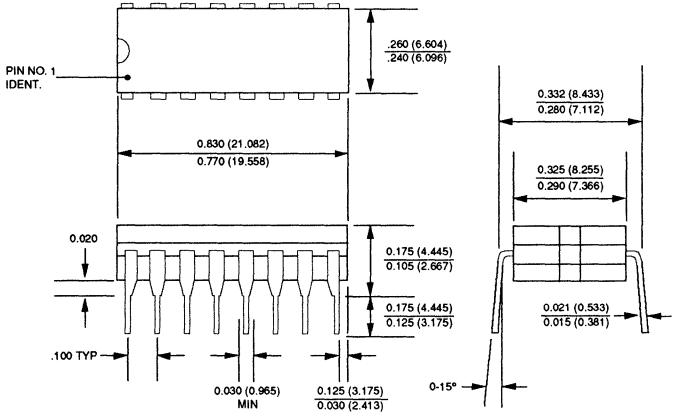
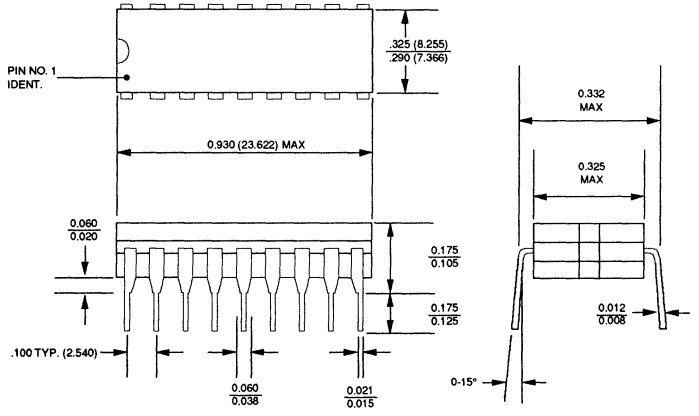


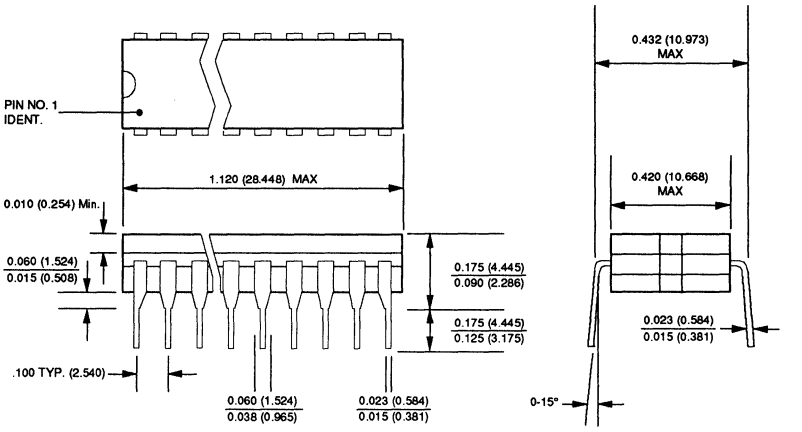

**16-Pin Cerdip**



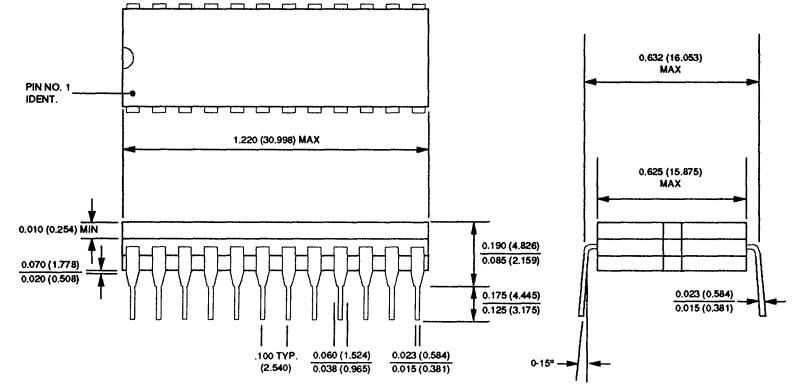

**18-Pin Cerdip**

12

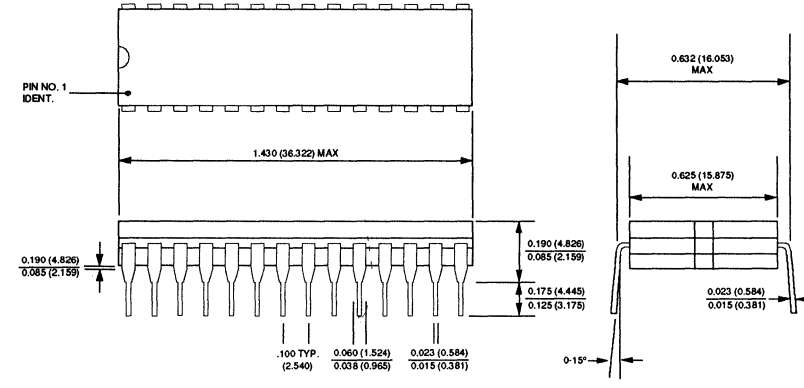
# Package Information




**22-Pin Cerdip**

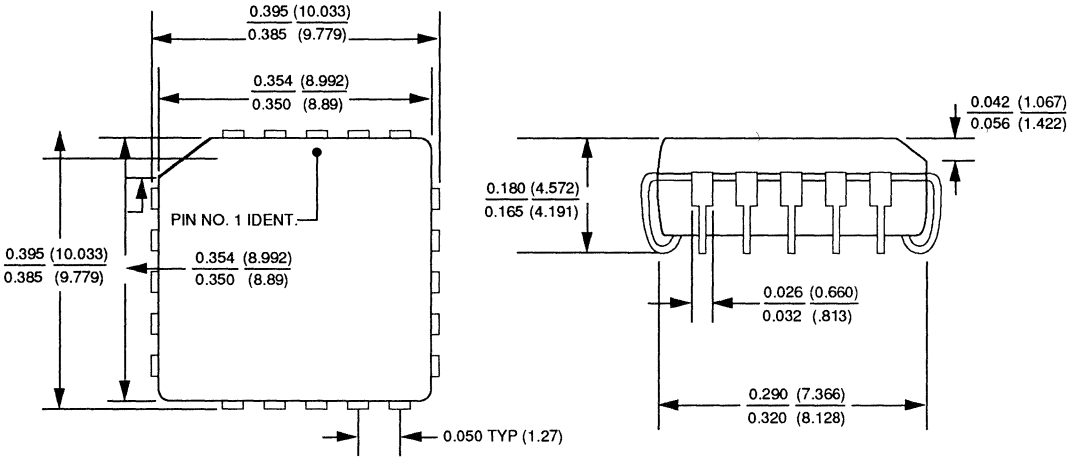



**24-Pin Cerdip**




**28-Pin Cerdip**

# Package Information
# Quad (PLCC)

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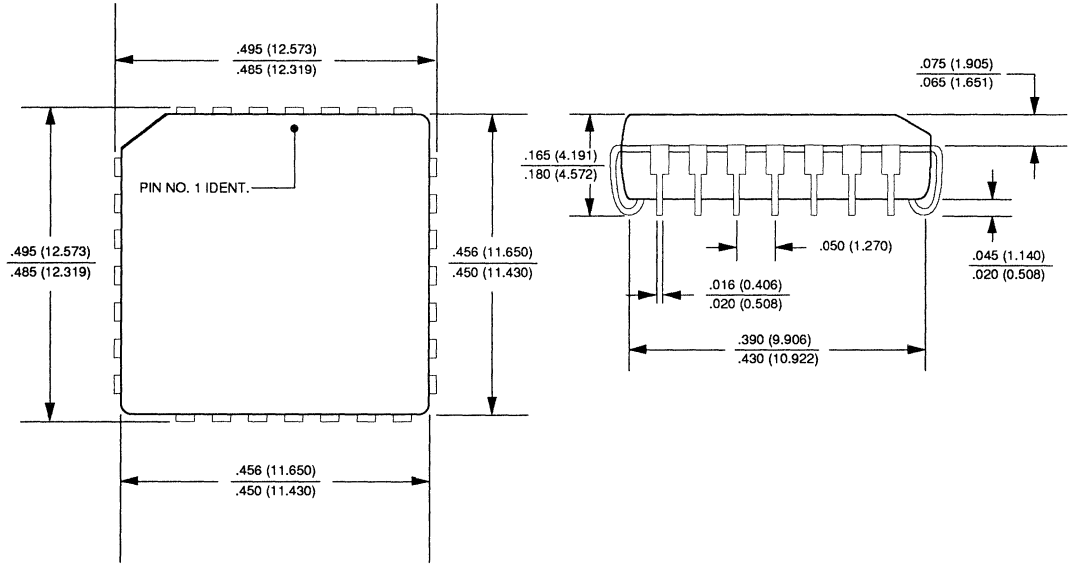
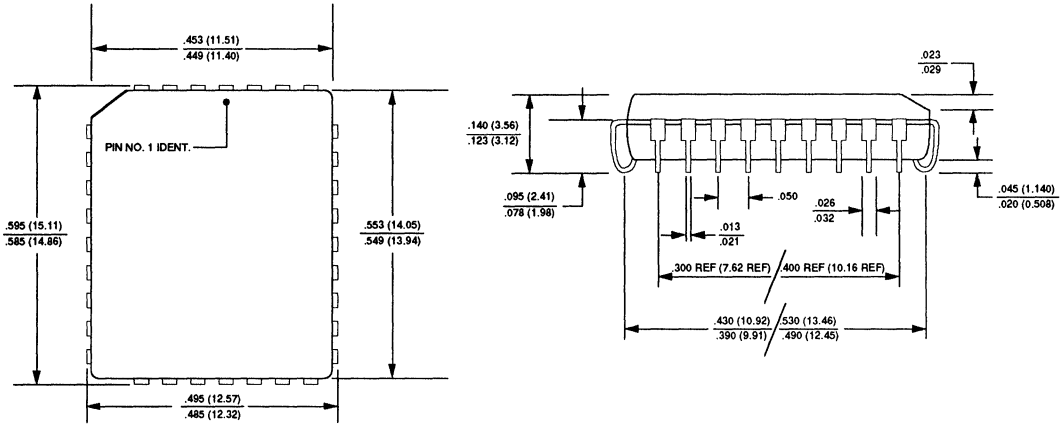


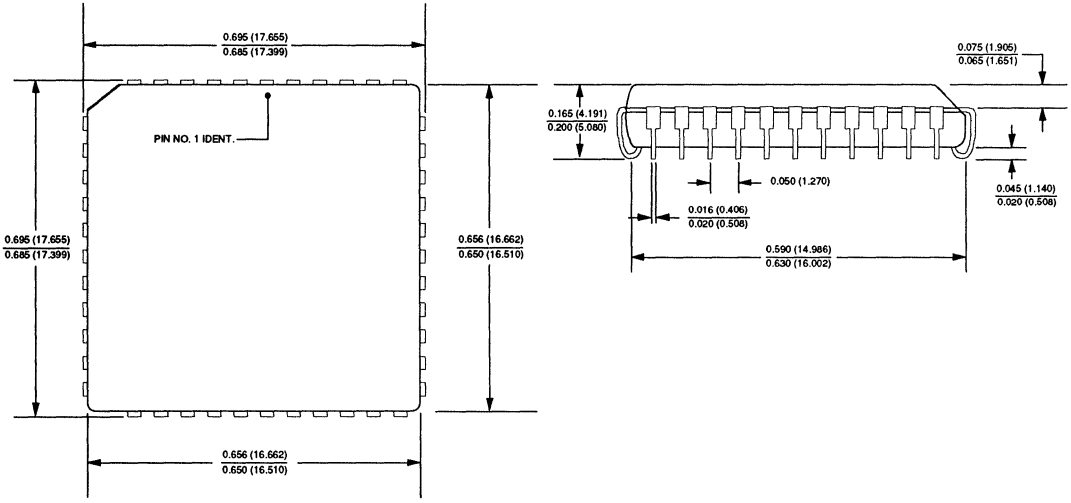

**28-Pin Quad PLCC**

12

# Package Information

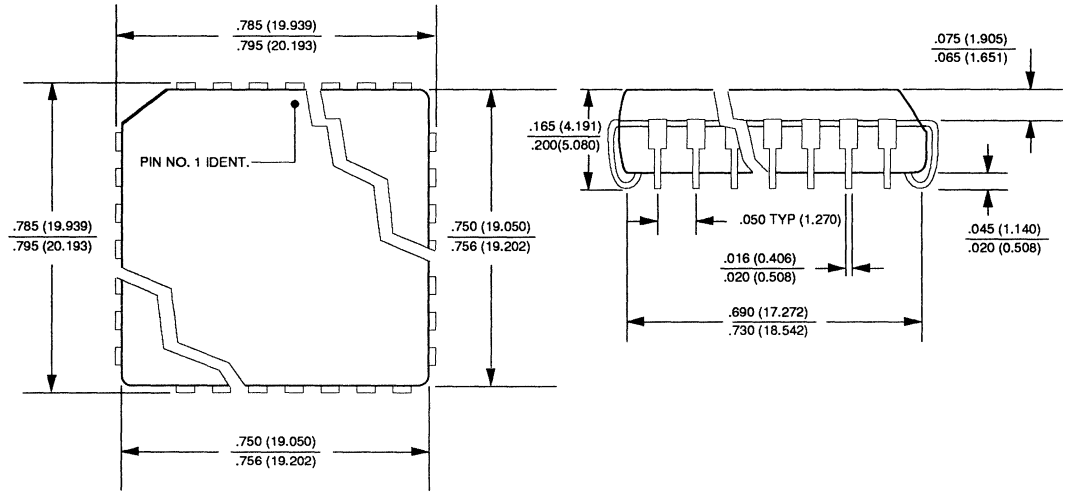



## 32-Pin Quad PLCC

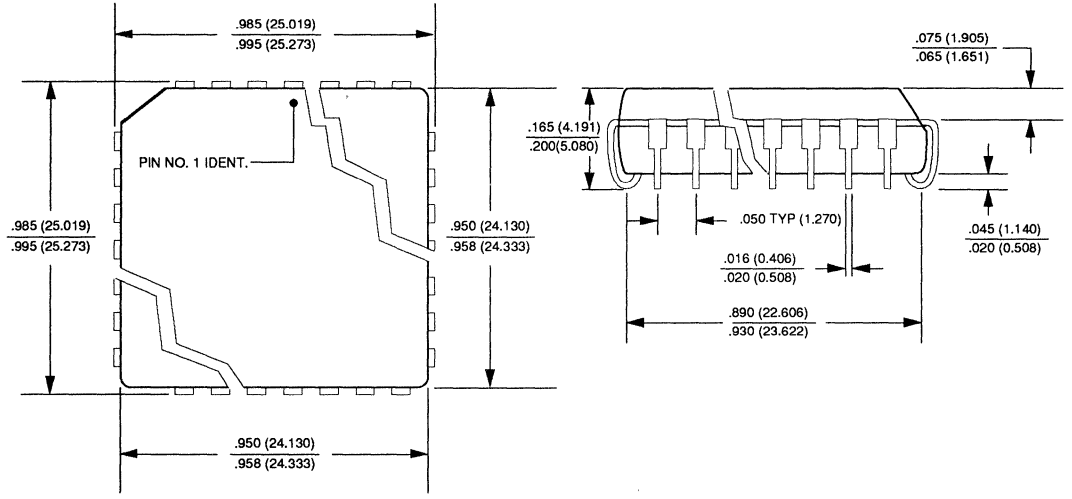



## 44-Pin Quad PLCC

# Package Information



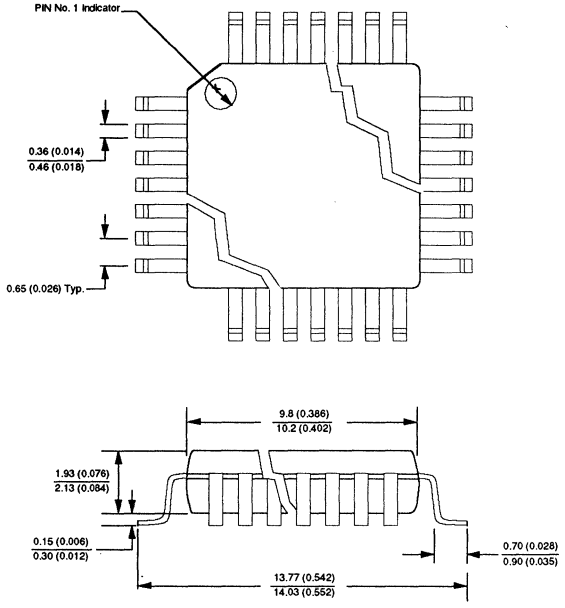

**52-Pin Quad PLCC**




**68-Pin Quad PLCC**

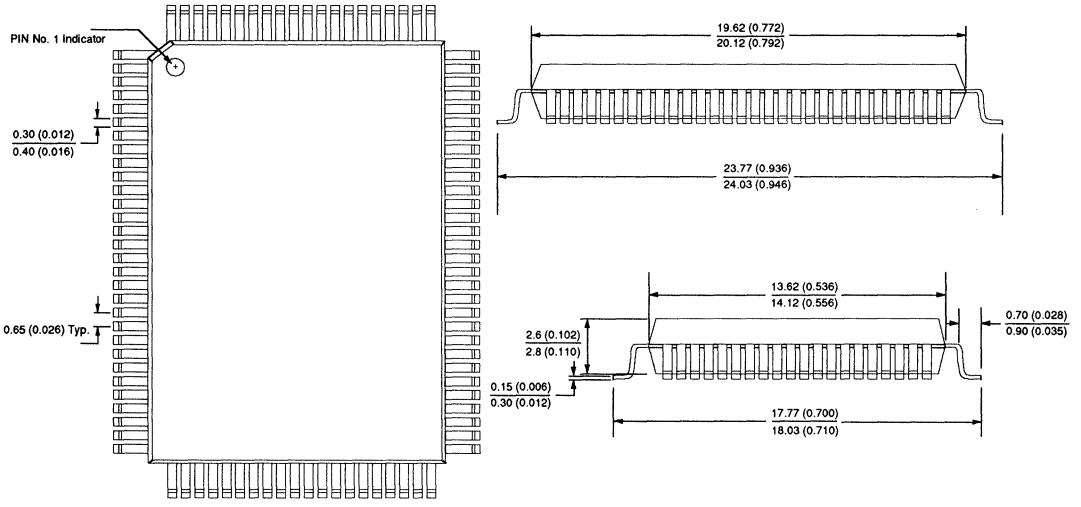
12

# Package Information
# Quad Flatpack (QFP)




## 52-Lead Quad Flatpack

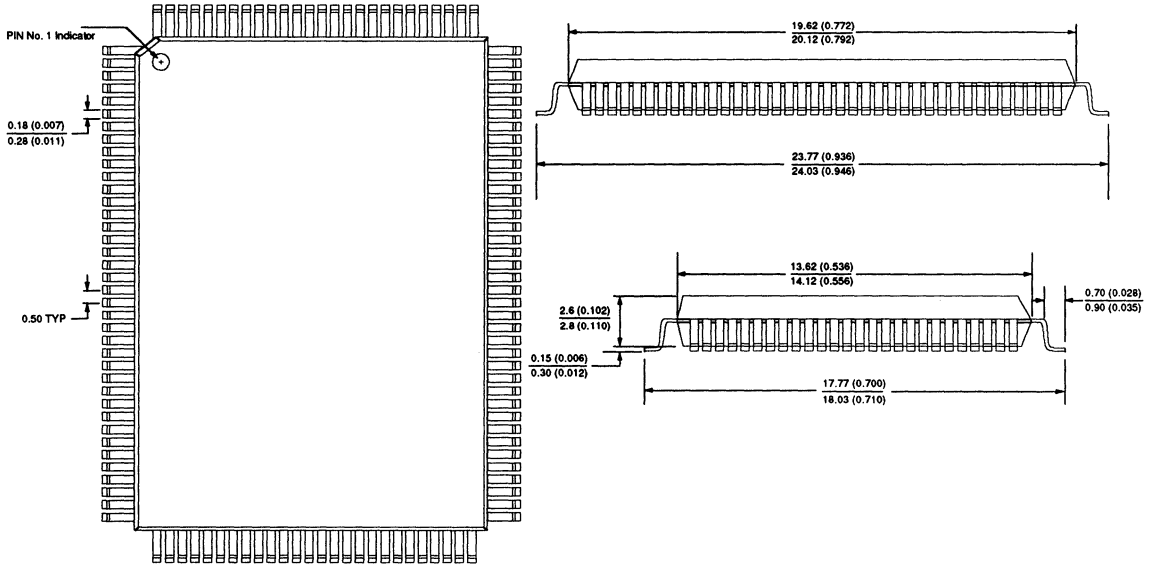
NOTE: Dimensions are in mm




## 100-Lead Quad Flatpack

NOTE: Dimensions are in mm

# Package Information

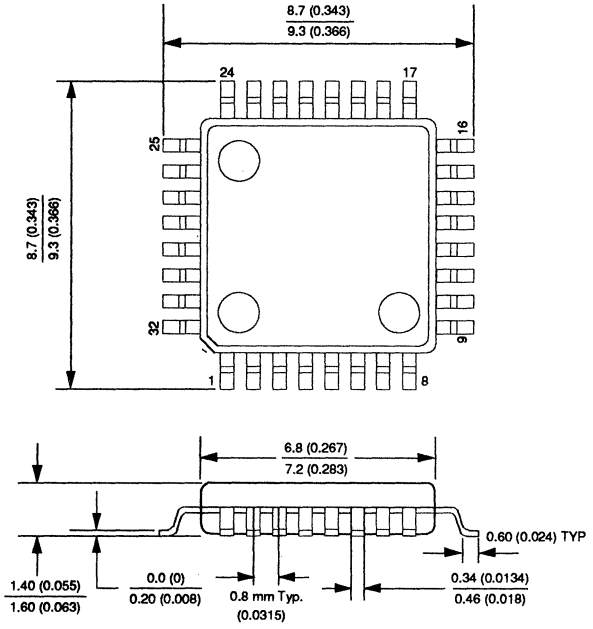



**128-Lead Quad Flatpack**

NOTE: Dimensions are in mm

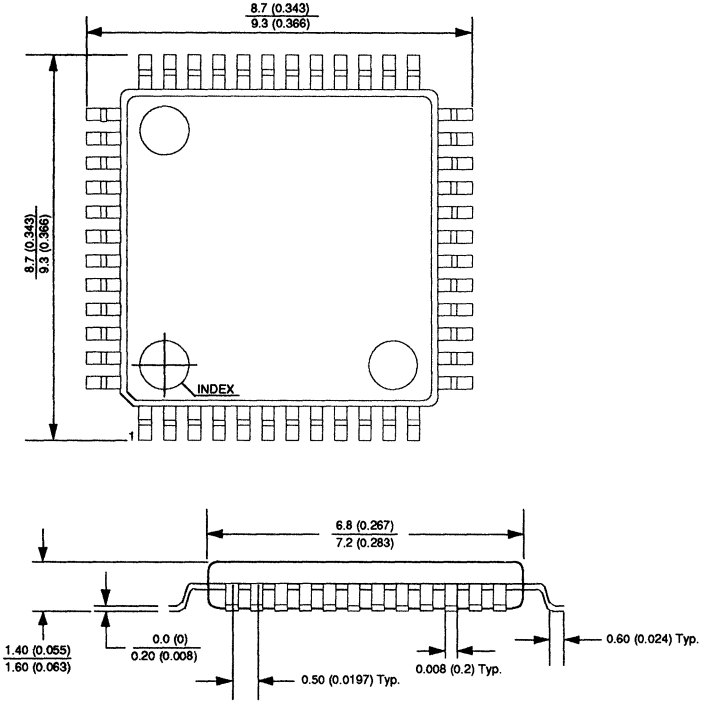
12

# Package Information
# Thin Quad Flatpack (TQFP)



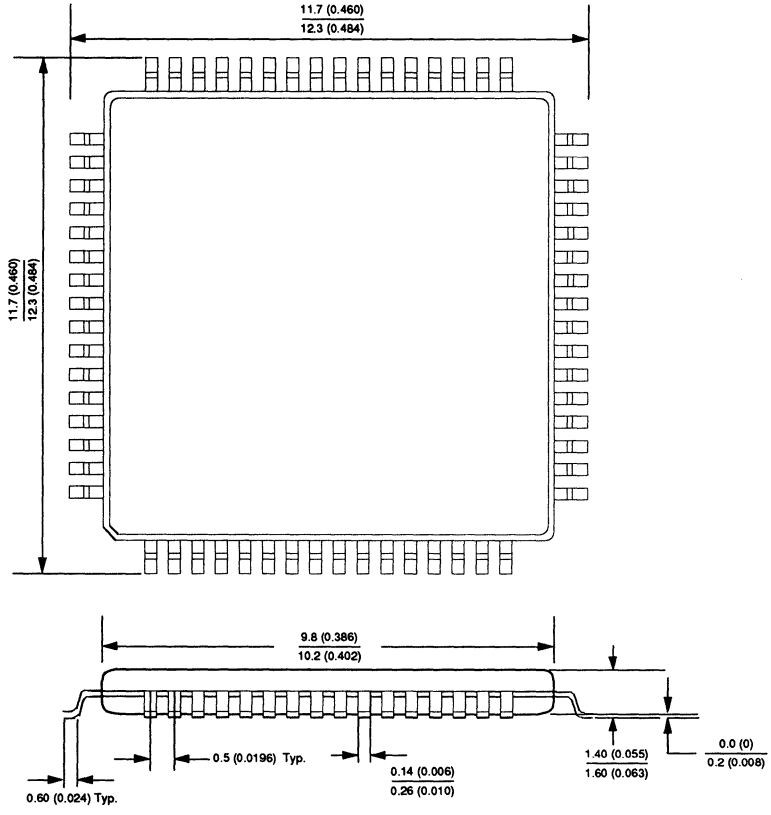

### 32-Lead Thin Quad Flatpack

NOTE: Dimensions are in mm




### 48-Lead Thin Quad Flatpack

NOTE: Dimensions are in mm

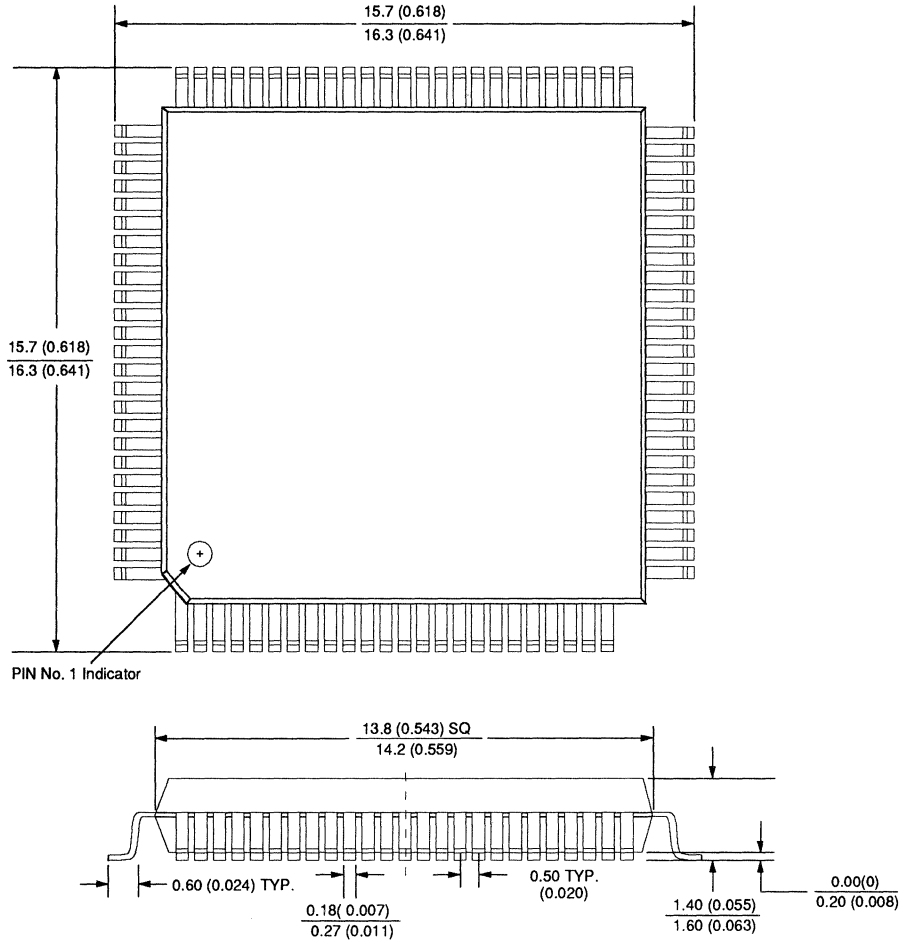



**64-Lead Thin Quad Flatpack**

NOTE: Dimensions are in mm

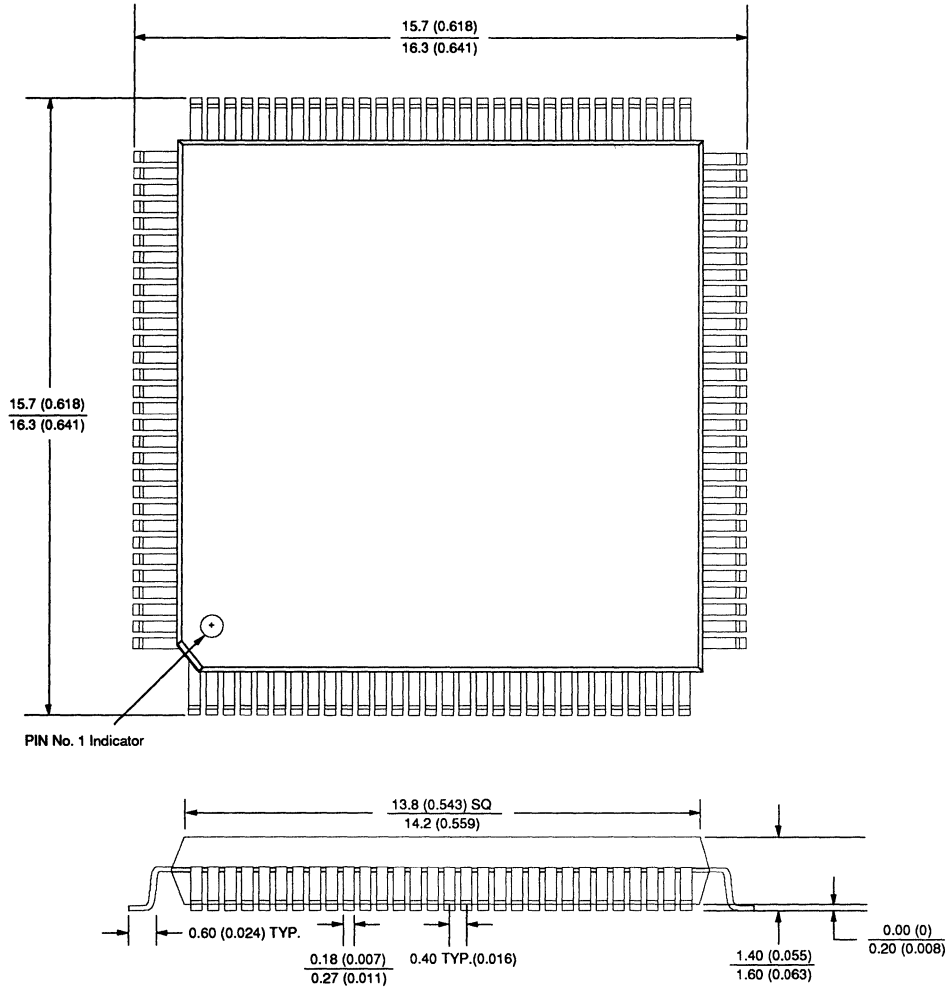
12

# Package Information




## 100-Lead Thin Quad Flatpack

NOTE: Dimensions are in mm




## 120-Lead Thin Quad Flatpack

NOTE: Dimensions are in mm

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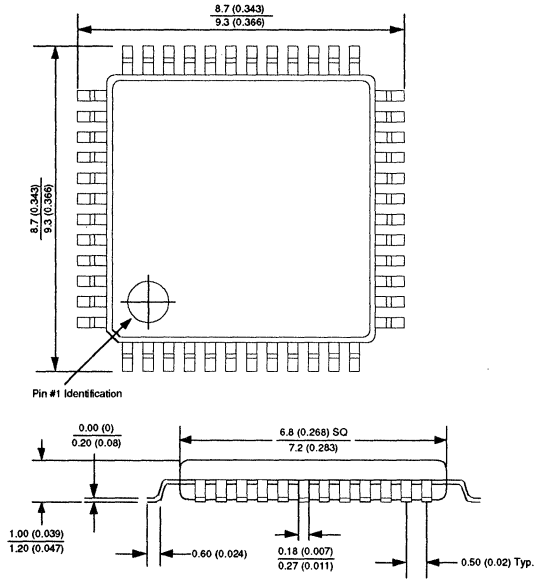
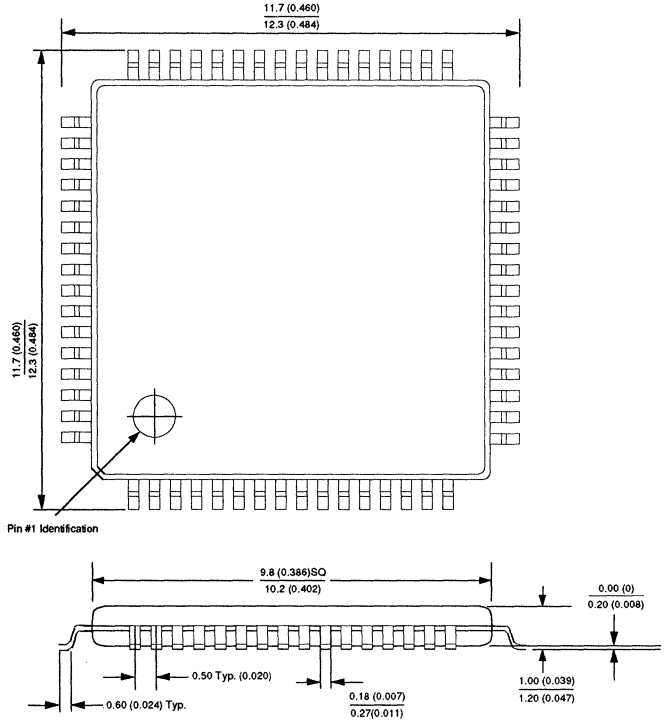
# Package Information
# Very Thin Quad Flatpack (VTQFP)



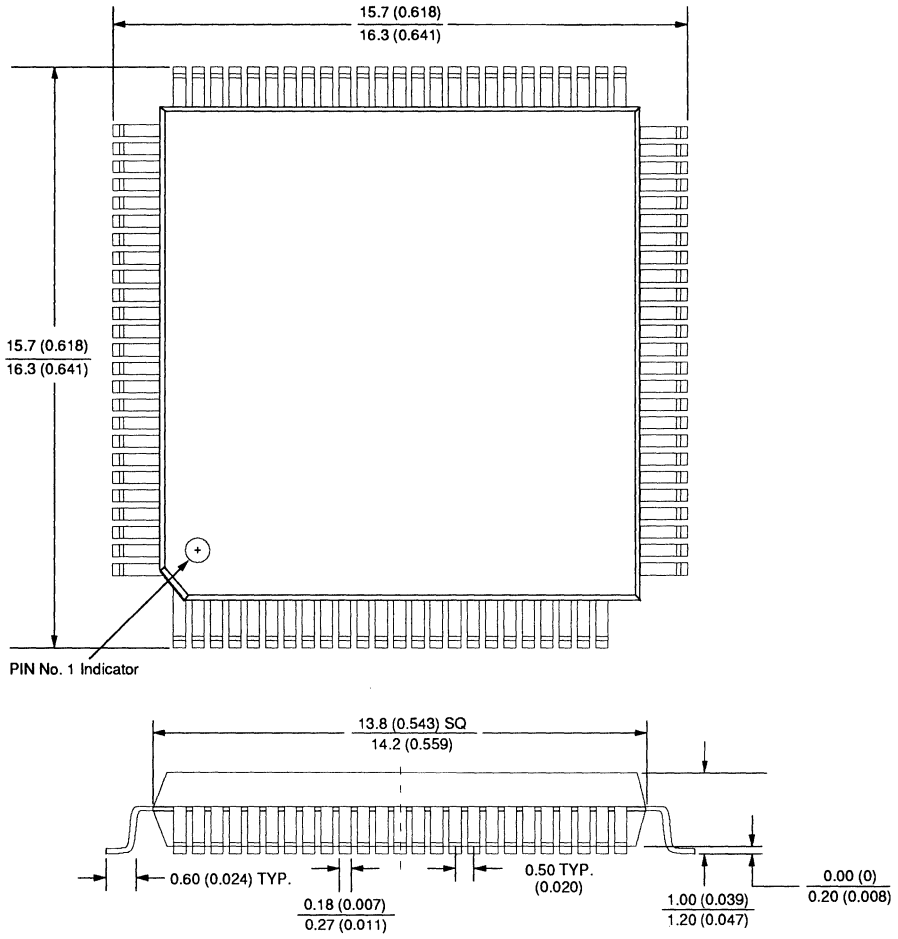

**48-Lead VTQFP**

NOTE: Dimensions are in mm




**64-Lead VTQFP**

NOTE: Dimensions are in mm

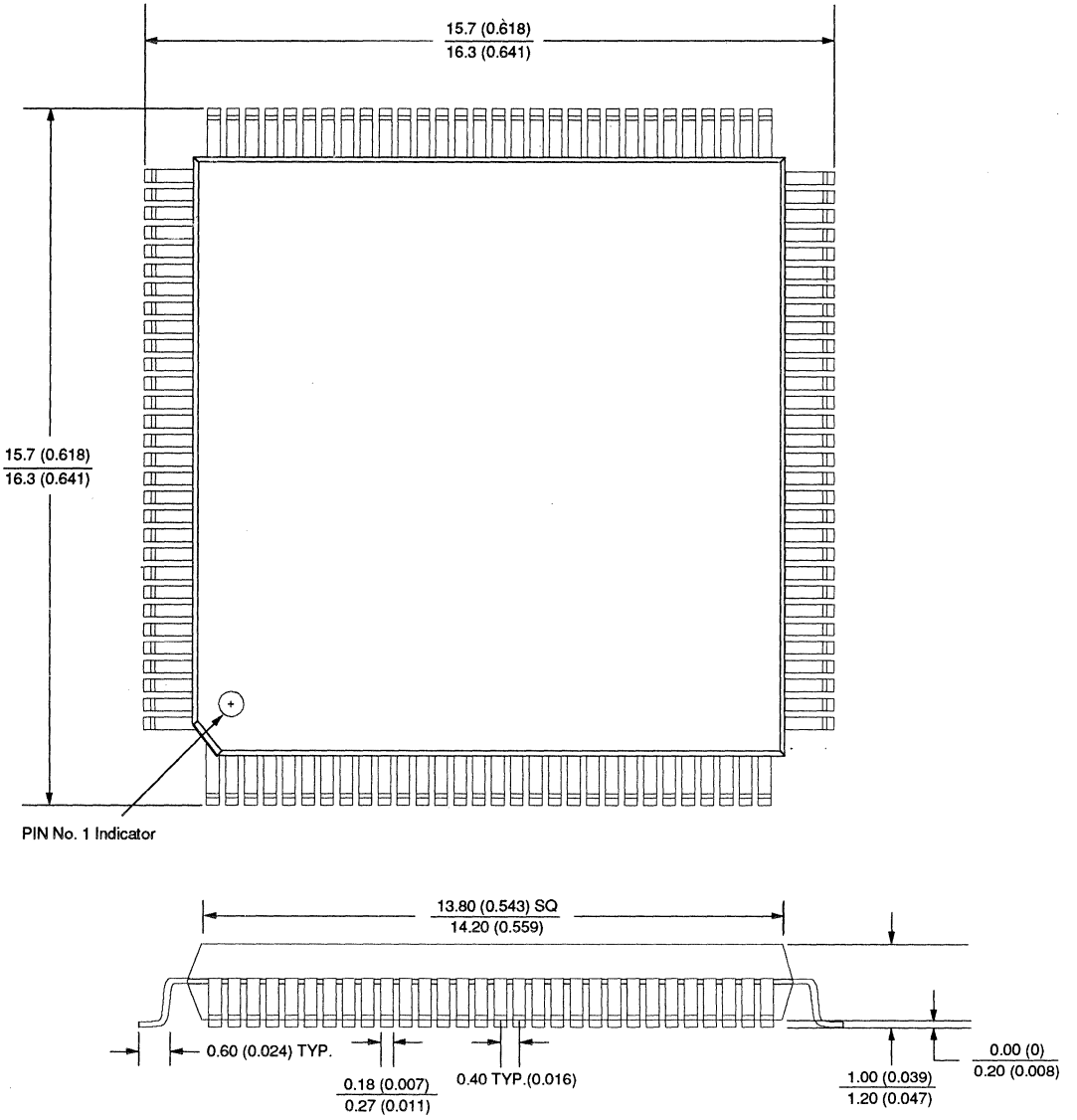



**100-Lead VTQFP**

NOTE: Dimensions are in mm

12

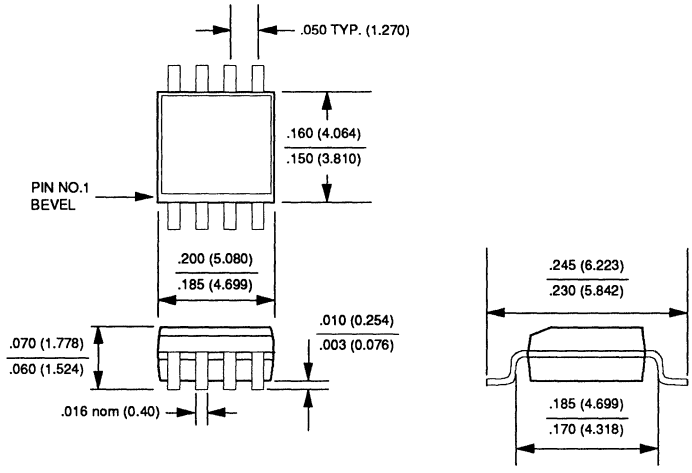
# Package Information



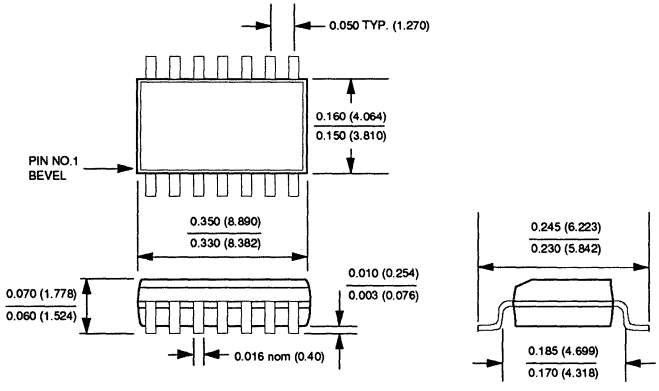

**120-Lead VTQFP**

NOTE: Dimensions are in mm

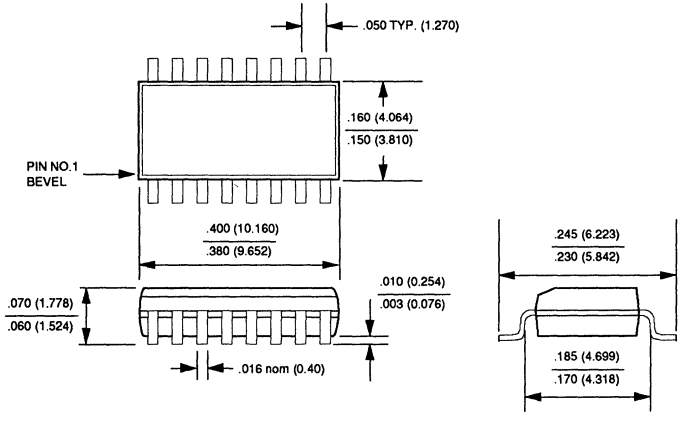
# Package Information
# SON




**8-Lead SON**




**14-Lead SON**




**16-Lead SON**

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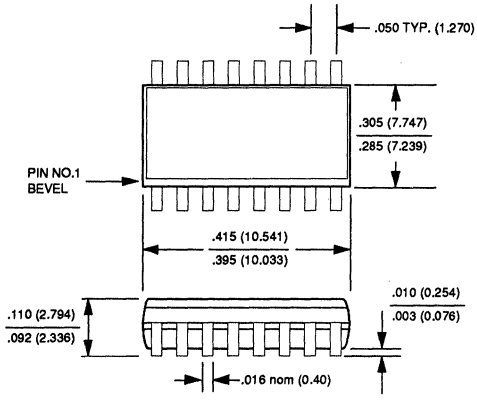
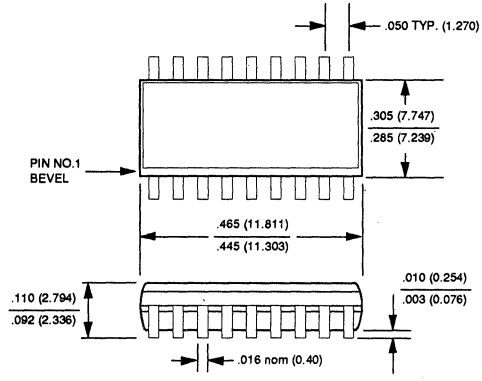
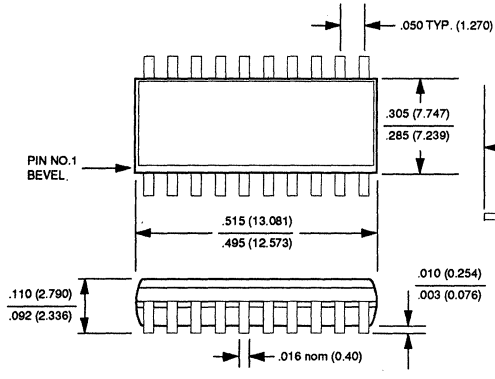
# Package Information
# SOL



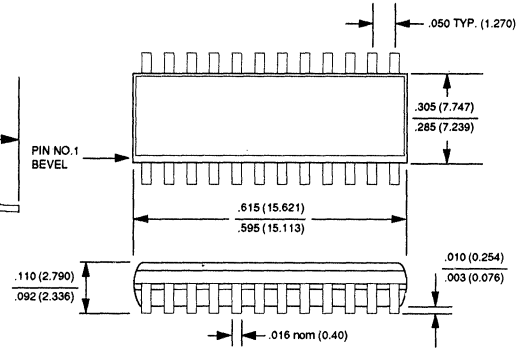

**16-Lead SOL**



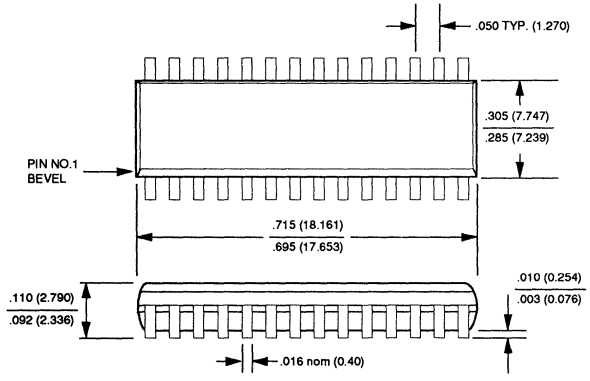

**18-Lead SOL**




**20-Lead SOL**

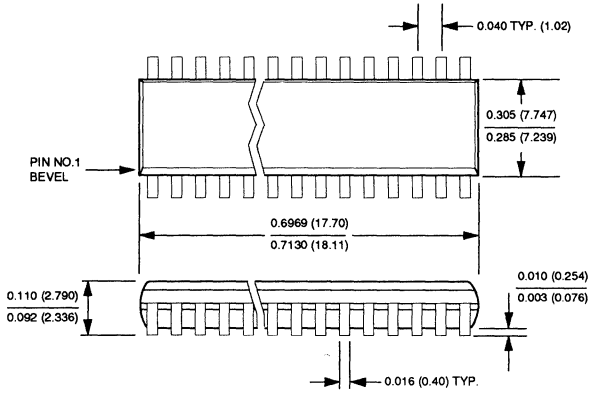


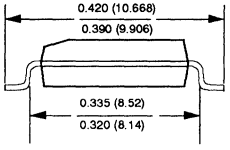

**24-Lead SOL**



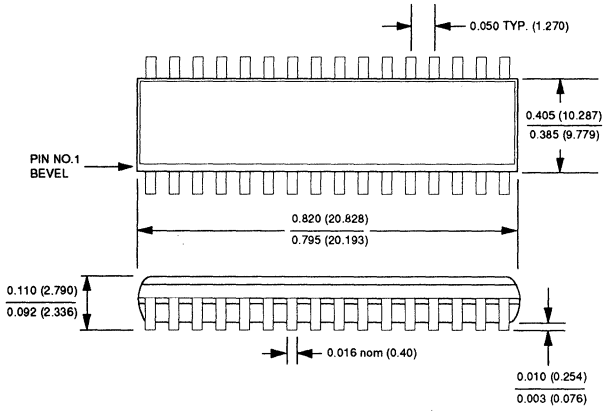

**28-Lead SOL**

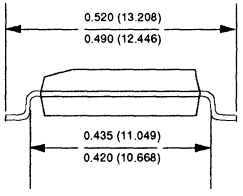
# Package Information
# SOL/SOM/SOW



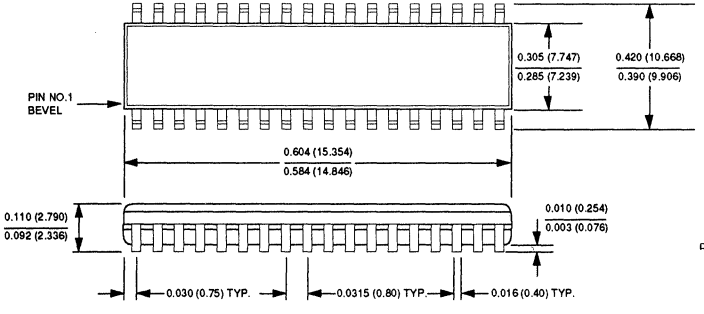



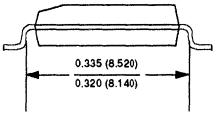

**34-Lead SOL**




**32-Lead SOW**




**36-Lead SOM (Fine Pitch)**

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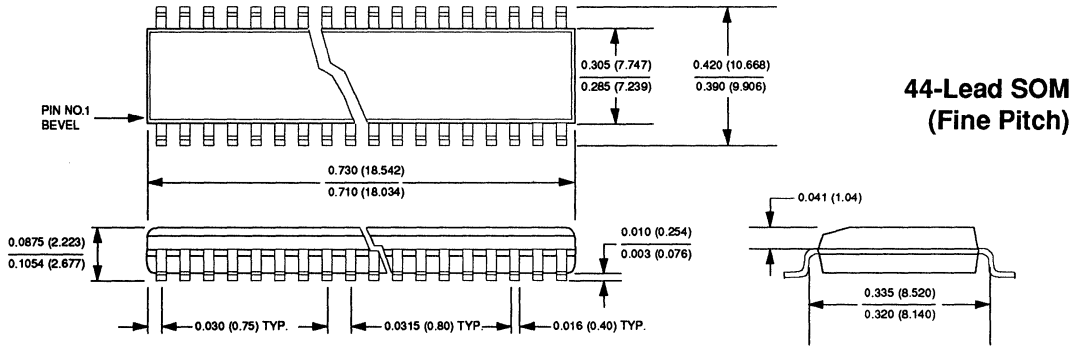
# Package Information

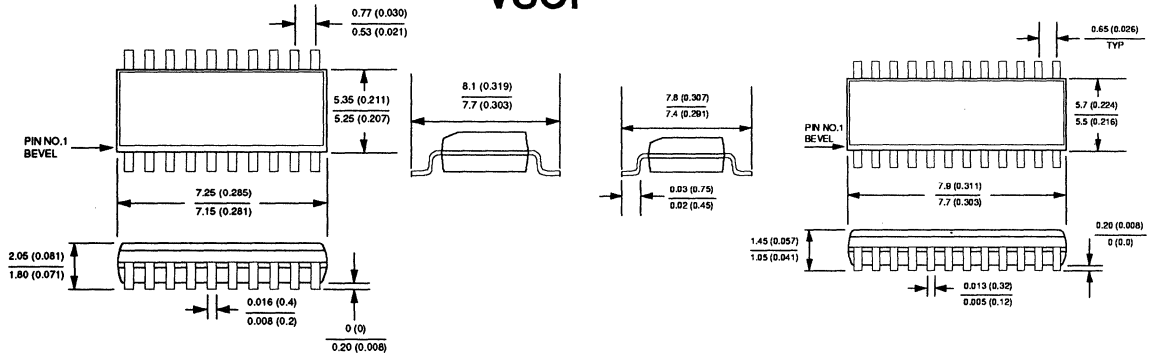



**44-Lead SOM (Fine Pitch)**

# Package Information

NOTE: Dimensions are in mm

## VSOP

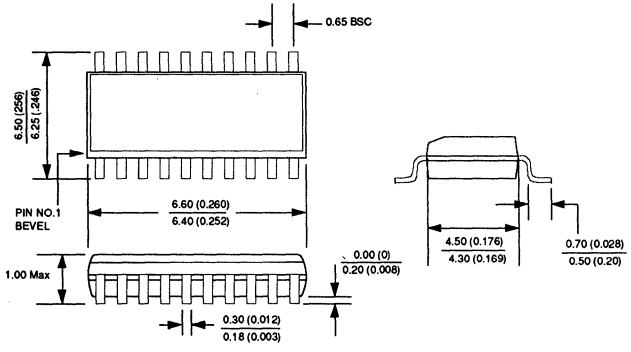



**20-Lead VSOP** **24-Lead VSOP**

# Package Information

NOTE: Dimensions are in mm

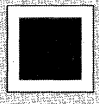
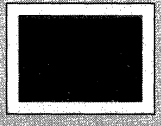
## VTSOP




**20-Lead VTSOP**

# Small Form Factor Package Selector Guide

## Quad Flatpack Packages

| PACKAGE TYPE | ACTUAL SIZE (AREA) | BODY SIZE (PITCH) mm | LAYOUT AREA mm² | ACTUAL SIZE (HEIGHT) | HEIGHT mm |
|---|---|---|---|---|---|
| 32G (QFP) |  | 7.0 x 7.0 (0.8) | 9.0 x 9.0 = 81 |  | 1.45 |
| 48 TQFP |  | 7.0 x 7.0 (0.5) | 9.0 x 9.0 = 81 |  | 1.4 |
| 52G (QFP) |  | 10.0 x 10.0 (0.65) | 14.0 x 14.0 = 196 |  | 2.2 |
| 64 TQFP |  | 10.0 x 10.0 (0.5) | 12.0 x 12.0 = 144 |  | 1.4 |
| 100G (QFP) |  | 20.0 x 14.0 (0.65) | 24.0 x 18.0 = 432 |  | 2.9 |
| 100 TQFP |  | 14.0 x 14.0 (0.5) | 17.2 x 17.2 = 296 |  | 1.4 |
| 128 QFP |  | 20.0 x 14.0 (0.5) | 24.0 x 18.0 = 432 |  | 2.54 |

 = Actual Body Size  = Full Layout Area All dimensions are nominal values.

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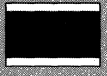
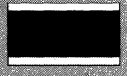
# Small Form Factor Package Selector Guide

## Small Outline Packages

| PACKAGE TYPE | ACTUAL SIZE (AREA) | BODY SIZE (PITCH) mm | LAYOUT AREA $mm^2$ | ACTUAL SIZE (HEIGHT) | HEIGHT mm |
|---|---|---|---|---|---|
| 16 SON |  | 9.8 x 3.9 (1.27) | 9.8 x 6.0 = 58.8 |  | 1.65 |
| 16 SOL |  | 10.2 x 7.5 (1.27) | 10.2 x 10.2 = 104 |  | 2.54 |
| 20 SOL |  | 12.8 x 7.5 (1.27) | 12.8 x 10.2 = 130.6 |  | 2.54 |
| 24 SOL |  | 15.4 x 7.5 (1.27) | 15.4 x 10.2 = 157 |  | 2.54 |
| 20 SOV (VSOP) |  | 7.2 x 5.4 (0.65) | 7.2 x 7.9 = 56.9 |  | 1.9 |
| 24 SOV (VSOP) |  | 7.8 x 5.6 (0.65) | 7.8 x 7.9 = 59.3 |  | 1.25 |
| 36 SOM (SSOP) |  | 15.1 x 7.5 (0.8) | 15.1 x 10.2 = 154 |  | 2.54 |
| 44 SOM (SSOP) |  | 18.3 x 7.5 (0.8) | 18.3 x 10.2 = 186.7 |  | 2.54 |

 = Actual Body Size:  = Full Layout Area All dimensions are nominal values.

Section 13

# SALES OFFICES/ DISTRIBUTORS

# North American
## Regional Offices & Sales Representatives

### NORTHWEST

**HEADQUARTERS**
Jon Tammel, Area Manager
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2001 Gateway Place
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FAX: (408) 453-5988

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Santa Clara
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FAX: (408) 727-8573

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*OHMS Technology, Inc.*
Minneapolis
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FAX: (612) 932-2918

**OREGON**
*Western Technical Sales*
Beaverton
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FAX: (503) 644-8200

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*Western Technical Sales*
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FAX: (206) 641-5829

Spokane
Ph: (509) 922-7600
FAX: (509) 922-7603

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**HEADQUARTERS**
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FAX: (714) 832-5247

Colorado Sales Office
Howard Barlow
3445 Penrose Place, Suite 140
Boulder, CO 80301
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FAX: (303) 440-9783

**ARIZONA**
*Western High Tech Marketing, Inc.*
Scottsdale
Ph: (602) 860-2702
FAX: (602) 860-2712

**CALIFORNIA**
*Hadden Associates*
San Diego
Ph: (619) 565-9444
FAX: (619) 565-1802

*SC Cubed*
Thousand Oaks
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FAX: (805) 495-3601

Tustin
Ph: (714) 731-9206
FAX: (714) 731-7801

**COLORADO**
*Lange Sales*
Littleton
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FAX: (303) 795-0373

Colorado Springs
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FAX: (719) 632-8419

**MONTANA**
*Lange Sales*
Boise, ID
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FAX: (208) 323-0834

**NEW MEXICO**
*Western High Tech Marketing, Inc.*
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FAX: (505) 884-2258

**TEXAS**
*OM Associates, Inc.*
Austin
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FAX: (512) 794-9987

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FAX: (214) 690-8721

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FAX: (713) 789-4825

**UTAH**
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Salt Lake City
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FAX: (801) 484-5408

### EASTERN

**HEADQUARTERS**
Wayne Taylor, Area Manager
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Dan Kilcourse
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FAX: (404) 368-1060

Automotive Sales (Detroit):
Fabian Battaglia
108 E. Grand River, Suite 6
Brighton, MI 48116
Ph: (313) 229-2811
FAX: (313) 229-3266

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*Technology Mktg. Assoc. (TMA)*
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FAX: (203) 628-0494

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FAX: (407) 671-4117

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FAX: (813) 535-9044

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FAX: (708) 773-2721

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Kokomo
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FAX: (317) 454-6987

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FAX: (319) 377-0958

**KANSAS**
*B.C. Electronics*
Kansas City
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FAX: (913) 342-0207

**KENTUCKY**
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FAX: (317) 888-8416

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Woburn
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FAX: (617) 932-0511

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FAX: (313) 338-6720

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*Technical Marketing Group*
West Caldwell
Ph: (201) 226-3300
FAX: (201) 226-9518

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*Omni Sales*
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FAX: (215) 233-4702

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FAX: (716) 427-0614

East Syracuse
Ph: (315) 463-1248
FAX: (315) 463-1717

*Technical Marketing Group*
Melville
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FAX: (516) 351-8667

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*Makin Associates*
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FAX: (513) 871-2524

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Solon
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**PENNSYLVANIA**
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Burgin-Kreh, Maryland

**WISCONSIN**
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Downsview
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FAX: (416) 660-5102

Nepean
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FAX: (613) 726-8834

**QUEBEC**
*Har-Tech*
Pointe Claire
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FAX: (32) 3-458-3126

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Massy Cedex
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**Notes:**

**Notes:**

Section 14

# APPLICATION NOTES

# Application Notes Index

# FILTER PRODUCTS SELECTOR GUIDE

| Device Number | Cutoff Frequency Range (MHz) | Power Dissipation (mW) | | Max Boost (dB) | NOISE VOLTAGE (mV Rms) | | | | THD | Supply Voltage | Group Delay Variation | Filter Type | Packages Available |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Normal (max) | Idle (max) | (nom) | Norm Out No Boost (max) | Norm Out Max Boost (max) | Diff Out No Boost (max) | Diff Out Max Boost (max) | 1 mVpp Input (%) | (V) | (%) * | (LPF) | |
| SSI 32F8001 | 9 to 27 | 330 | 3 | 13 | 3.5 | 4 | 4.7 | 6.5 | 1 | 5 | 4 | equiripple | 16L, 16N |
| SSI 32F8002 | 6 to 18 | 330 | 3 | 13 | 3.5 | 4 | 4.7 | 6.5 | 1 | 5 | 3 | equiripple | 16L, 16N |
| SSI 32F8003 | 5 to 13 | 330 | 3 | 13 | 3.5 | 4 | 4.7 | 6.5 | 1 | 5 | 3 | equiripple | 16L, 16N |
| SSI 32F8011 | 5 to 13 | 440 | 95 | 9 | 3.6 | 4.4 | 6.8 | 8.1 | 1 | 5 | 2 | Bessel | 16L, 16N |
| SSI 32F8012 | 6 to 15 | 440 | 95 | 9 | 3.6 | 4.4 | 6.8 | 8.1 | 1 | 5 | 2 | Bessel | 16L, 16N |
| SSI 32F8020A | 1.5 to 8 | 226 | 3 | 9 | 4 | 4.5 | 7.5 | 11 | 1 | 5 | 3 | equiripple | 16L, 16N |
| SSI 32F8021 | 1.5 to 8 | 226 | 3 | 9 | 4 | 4.5 | N/A | N/A | 1 | 5 | 3 | equiripple | 16L, 16N |
| SSI 32F8022A | 1.5 to 8 | 226 | 3 | 9 | 4 | 4.5 | 7.5 | 11 | 1 | 5 | 3 | equiripple | 16L, 16N |
| SSI 32F8023 | 1.5 to 8 | 226 | 3 | 9 | 4 | 4.5 | N/A | N/A | 1 | 5 | 3 | equiripple | 16L, 16N |
| SSI 32F8030 | 0.25 to 2.5 | 230 | 3 | 9 | 2 | 2.2 | 3.2 | 3.8 | 1 | 5 | 3 | equiripple | 16L, 16N |

* Valid from 0.2 *fc* to 1.75 *fc* for equiripple filters, 0.2 *fc* to *fc* for Bessel filters

(continued)

# FILTER PRODUCTS SELECTOR GUIDE (continued)
## Filters with Serial Port and DACs

| Device Number | Cutoff Frequency Range (MHz) | Power Dissipation (mW) Normal (max) | Power Dissipation (mW) Idle (max) | Max Boost (dB) (nom) | NOISE VOLTAGE (mV Rms) Norm Out No Boost (max) | NOISE VOLTAGE (mV Rms) Norm Out Max Boost (max) | NOISE VOLTAGE (mV Rms) Diff Out No Boost (max) | NOISE VOLTAGE (mV Rms) Diff Out Max Boost (max) | THD 1 mVpp Input (%) | Supply Voltage (V) | Group Delay Variation (%) * | Filter Type (LPF) | Packages Available |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SSI 32F8101 | 9 to 27 | 150 | 5 | 13 | 3.5 | 4.5 | 5 | 8.4 | 1 | 5 | 3 | equiripple | 16N, 20V |
| SSI 32F8102 | 6 to 18 | 150 | 5 | 13 | 3.5 | 4.5 | 5 | 8.4 | 1 | 5 | 3 | equiripple | 16N, 20V |
| SSI 32F8103 | 4 to 12 | 150 | 5 | 13 | 3 | 5 | 3.4 | 6.7 | 1 | 5 | 3 | equiripple | 16N, 20V |
| SSI 32F8104 | 3 to 9 | 150 | 5 | 13 | 3 | 5 | 3.4 | 6.7 | 1 | 5 | 3 | equiripple | 16N, 20V |
| SSI 32F8120 | 1.5 to 8 | 410 | 70 | 10 | 3 | 4 | 6 | 9 | 1.5 | 5 | 3 | equiripple | 16L, 20V |
| SSI 32F8130 | 0.25 to 2.5 | 385 | 6 | 10 | 1.9 | 2 | 2.7 | 3.4 | 1 | 5 | 3 | equiripple | 16L |
| SSI 32F8131 | 0.15 to 1.4 | 385 | 6 | 10 | 1.9 | 2 | 2.7 | 3.4 | 1 | 5 | 3 | equiripple | 16L |
| SSI 32F8144** | 7 to 27 | 550 | 66 | 9 | 4 | 6 | 6 | 9 | 1 | 5 | 3 | equiripple | 20V, 20L |

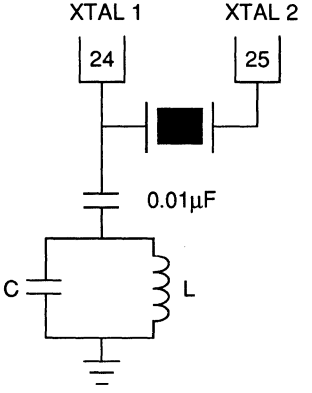
* Valid from 0.2 $fc$ to 1.75 $fc$ for equiripple filters, 0.2 $fc$ to $fc$ for Bessel filters
** The F8144 has a programmable gain from 10 to 100 V/V

January 1993

## REFERENCE OSCILLATOR

An internal reference oscillator generates the standby reference for the PLL. A series resonant crystal should be used between XTAL1 and XTAL2. If a crystal oscillator is not desired, then an external AC coupled ECL source may be applied to XTAL1, leaving XTAL2 open. A TTL compatible reference may also be used if suitably attenuated.

If it is desired to operate a crystal at a non-fundamental or harmonic frequency, then the following network is suggested:



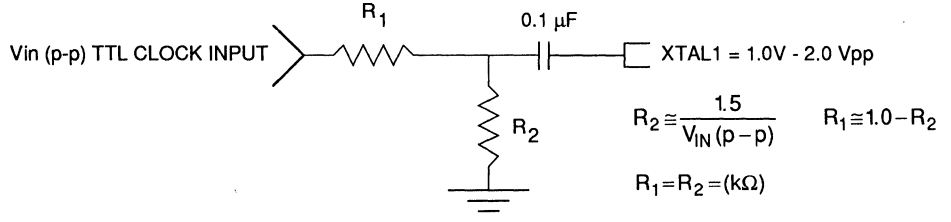

$$\omega_o = 2\Pi F_o = \frac{1}{\sqrt{LC}}$$

$$Q_o = \omega_o C \, Rin$$

The typical input impedance looking into XTAL1 is approximately Rin = 250Ω. It is recommended to design the value of Qo at approximately 10 to 15. Therefore, a resonant frequency of Fo = 20 MHz would result in L ≅ 0.16 μH and C ≅ 380 pF.

## ATTENUATOR CIRCUIT

If a crystal oscillator is not desired, then an external TTL Compatible reference may be applied to XTAL1 leaving XTAL2 open. It is required, however that the TTL signal be attenuated then A.C. coupled into XTAL1 using the following network:




The signal amplitude into XTAL1 should be attenuated to approximately 1.0 to 2.0 Vp-p; this will insure that the transients associated with TTL switching characteristics won't couple into the data synchronizer and degrade performance.

## LOOP FILTER

The performance of the data synchronizer is directly related to the selection of the loop filter. The loop filter characteristics should be optimized for:

**(A) Fast Acquisition**

The ability of the loop to quickly obtain lock when the input signal to the Phase Detector is switched between the reference oscillator (crystal) and the Read Data ($\overline{RD}$). Fast acquisition implies a large loop bandwidth so that it can quickly respond to changes at the input.

**(B) Data Margin**

The ability of the loop to ignore bit shifts (jitter) and maintain a well centered window about the data pulse train. In general, it is not desirable to allow the loop to respond to a single shifted bit as this would cause the subsequent bit to be poorly centered within its window and possibly cause an error. This requirement implies a small loop bandwidth reducing the sensitivity to high frequency jitter.

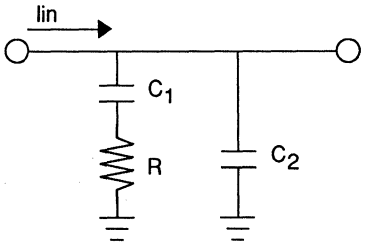
**(C) Data Tracking**

The ability to respond to instantaneous changes in phase and frequency of the data. This can be a result of such phenomena as disk rotational speed variations which cause changes in the characteristics of the incoming data stream. In general, this requirement is consistent with that of fast acquisition, however, this depends upon the application.

Although the loop performance characteristics place conflicting requirements on the loop bandwidth, the architecture of the Silicon Systems data synchbronizer family significantly simplifies the design by minimizing the "step in phase" and "step in frequency" encountered when switching the Phase Detector input reference signal. A zero phase restart technique is employed to minimize the initial phase error while the standby reference oscillator keeps the VCO at the center frequency during non-read modes.

One approach in determining the initial loop filter selection is to consider the requirements imposed during acquisition. This includes both acquiring lock to the crystal reference in non-read modes, as well as locking to the preamble field prior to decoding data. The format of the sector will dictate which of these two criteria imposes the tightest restriction on acquisition.

The requirements for acquiring lock to the crystal oscillator are application specific and usually depend upon the length of the Write Splice gap. Therefore, the design approach employed in this analysis will be based upon the requirements during acquisition to the preamble field. The length (in time) of the preamble field is set by the data synchronizer's locking sequence. Knowing this length in time, and that our initial phase error is less than 0.5 radians, we can determine an acceptable loop bandwidth ($\omega_n$) and damping factor ($\zeta$).
One possible loop filter configuration is as follows:



The role of C1 is as an integrating element. The larger this capacitance, the longer the acquisition time; the smaller the capacitance, the greater the ability to track high frequency jitter. The resistor R reduces the phase shift induced by C1. The capacitor C2 will suppress high frequency transients and will have minimal effect on the loop response if it is small relative to C1 (typically C2 = C1/10)

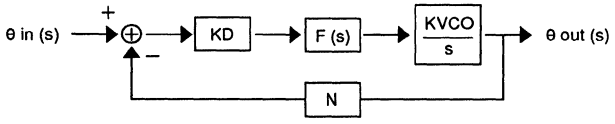
The loop filter transfer function is:

$$F(s) = \frac{Vout}{Iin} = \frac{1 + sRC_1}{sC_1\left(1 + sC_2R + C_2/C_1\right)}$$

If C2 << C1, then:

$$F(s) = \frac{Vout}{Iin} = \frac{1 + sRC_1}{sC_1}$$

The overall block diagram for the phaselock loop can be described as:




Where:

KD = Phase Detector gain [A/rad]

F(s) = Loop filter impedance [V/A]

KVCO/s = VCO control gain [rad/s V]

N = The ratio of the reference input frequency to the VCO output frequency

The closed loop transfer function is:

$$T(s) = \frac{\theta out(s)}{\theta in(s)} = \frac{G(s)}{1 + GH(s)} = \frac{KD \cdot KVCO[(1 + sRC_1)/C_1]}{s^2 + s[N \cdot KD \cdot KVCO \cdot R] + \frac{N \cdot KD \cdot KVCO}{C_1}}$$

by putting the characteristic equation (denominator) in the form of:

$$s^2 + 2s\zeta\omega n + \omega n^2$$

we can solve for $\omega n$ and $\zeta$ to get:

$$\omega n^2 = \frac{N \cdot KD \cdot KVCO}{C1} \qquad \zeta = \frac{N \cdot KD \cdot KVCO \cdot R}{2\omega n}$$

Now we can solve for R, C1 and C2:

$$C1 = \frac{N \cdot KD \cdot KVCO}{\omega n^2} \qquad R = \frac{2\zeta\omega n}{N \cdot KD \cdot KVCO} \qquad C_2 = \frac{C_1}{10}$$

where: $\omega n$ = loop bandwidth and, $\zeta$ = loop damping factor

Because of the nature of Run Length Limited (RLL) codes, the Phase Detector will only be enabled during a data pulse. This technique allows the VCO to run at a center frequency with period, TVCO, equal to one encoded data bit cell time.

Figure 1 represents the relationship between the VCO output when locked to various Phase Detector input signals.

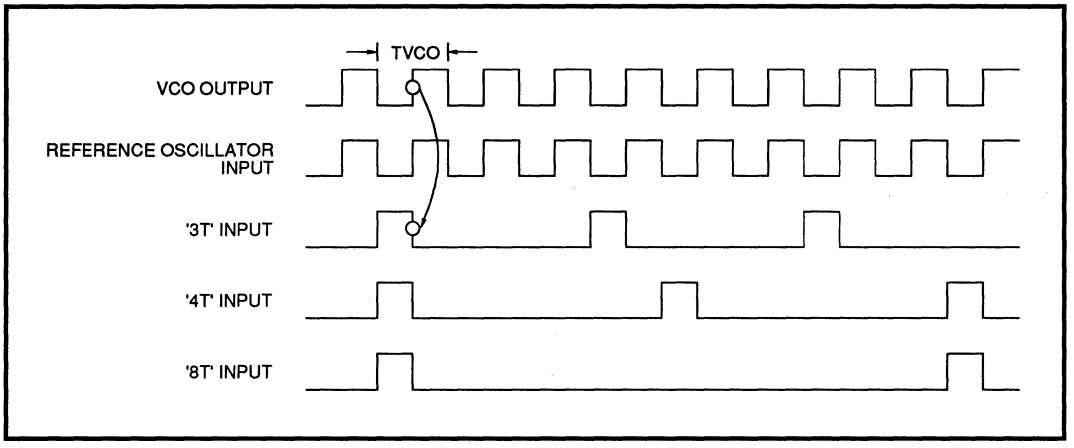



**FIGURE 1: Relationship of VCO Output to Phase Detector Input**

The average amplitude of the Phase Detector gain depends upon the Phase Detector input signal. When the PLL is locked to the reference oscillator, the Phase Detector is continuously enabled and the gain is at its maximum. When the PLL is tracking data and the input is an "8T" pattern, then the Phase Detector gain is at its minimum. The following indicates the value of "N" for various input conditions:

N = 1.0 for θin = reference oscillator

N = 0.33 for θin = 3T (100) preamble field

N = 0.25 for θin = 4T (1000)

N = 0.125 for θin = 8T

Throughout this analysis the PLL has been considered as a continuous time system. In actuality the characteristics of the Phase Detector result in a sampled data system. By utilizing an integrating loop filter to average and smooth the Phase Detector charge pump output pulses, this analogy should be reasonable.

Determining an acceptable amount of phase error after locking to the preamble field depends upon the system requirements. In addition, it may be necessary to consider the effects of frequency steps in applications where motor speed control tolerances are significant. Generally, an acceptable amount of error is defined to be that amount which when added to all other timing error contributors, results in the data being within its timing window by the required margin.

In general, it is desirable to have the loop damping factor "ζ" between 0.5 and 1.0 during acquisition. For a high gain, second-order loop this results in minimal noise bandwidth.

Figure 2 represents the phase error's response in time to a transient step in phase as a function of the loop bandwidth and damping factor. Figure 3 indicates the response of the VCO control voltage to compensate for this step in phase.

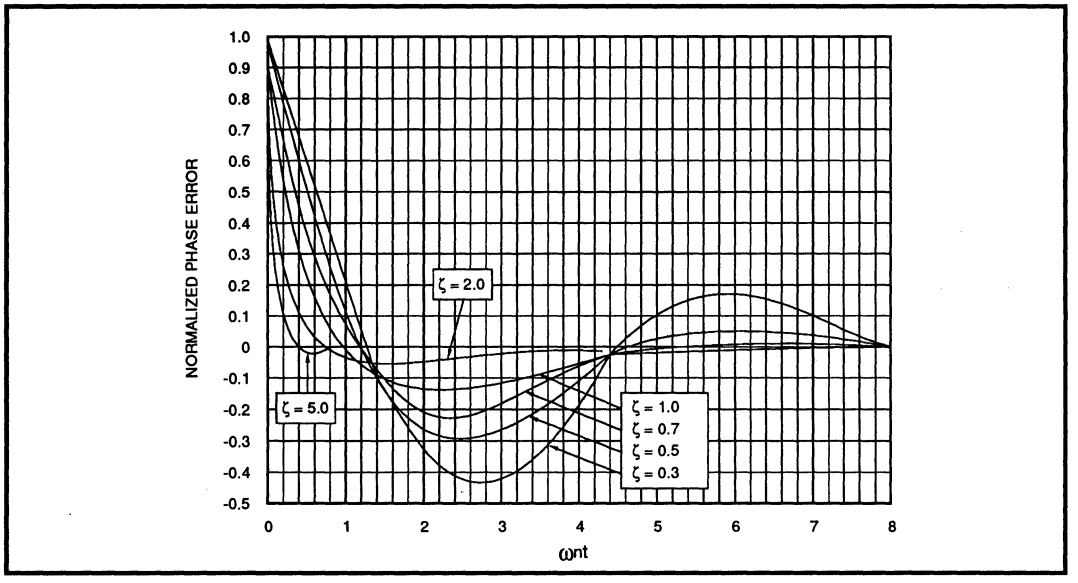



**FIGURE 2: Transient Phase Error θe(t) Due To a Step In Phase Δθ**

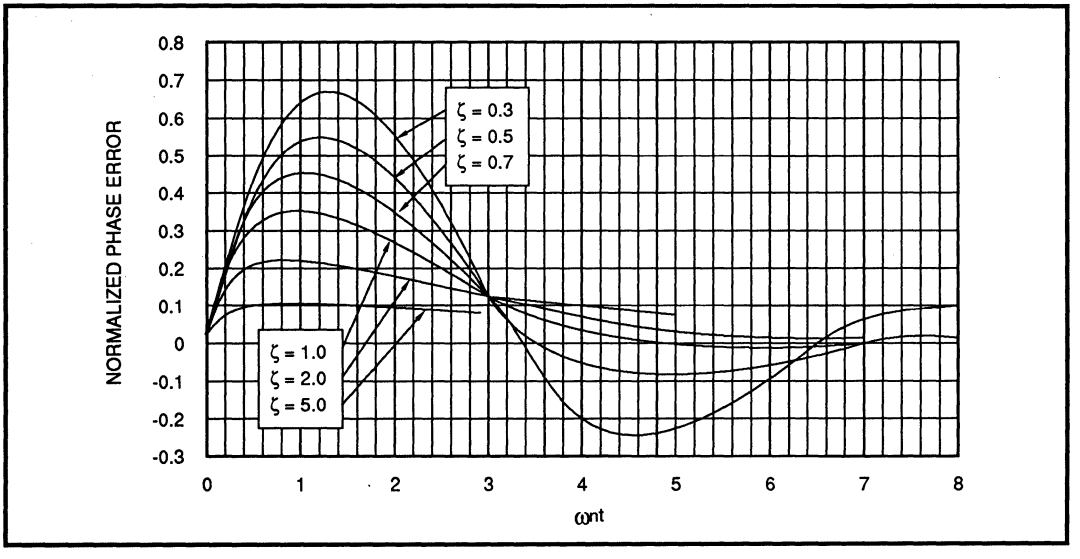



**FIGURE 3: Transient Phase Error θe(t) Due to a Step In Frequency Δω**

## DATA RECOVERY APPLICATIONS

### DETERMINING LOOP FILTER COMPONENTS

What follows is a method to calculate loop filter components based on the acceptable phase error when the VCO switches from the reference frequency to read data.

To determine the maximum time the VCO has to lock from the reference frequency to read data, the equation is: Tmax = Ln • 'xT'/(DR•M)

DR is the data rate and Tmax is the amount of time the Phase Lock Loop (PLL) has to settle to within an acceptable amount of error before tracking and decoding data. Ln, 'xT' and M are variables that are device dependent and are defined tin Table 'A'. It is important to note it follows from the above equation that the locking time from the reference frequency (crystal oscillator) to read data is fixed and is not dependent on the length of the preamble field. Although, any additional preamble field will allow more time for the PLL to settle out before starting to decode data.

**Table A**

| DEVICE | MODE | PREAMBLE ('xT') | Ln | M |
|---|---|---|---|---|
| 537X | -- | 3 | 16 | 1.5 |
| 539X | -- | 3 | 16 | 1.5 |

DEVICE: An 'X' implies a family of devices, for instance 537X includes the 5371, 5372, 5373 and 5374

MODE: This is 'SS' for soft sector and 'HS' for hard sector application. '--' implies that there is no difference between hard sector or soft sector applications.

PREAMBLE ('xT'): Depending on the mode, the preamble could be a '3T' (xT = 3) or '4T' (xT = 4).

Ln: This is the number of read data transitions that the device counts within the preamble to allow for VCO lock. The transitions are assumed to be part of a uniform preamble field.

M: This factor times the Data Rate determines the frequency of read data. It is also the code rate. For instance, for the 537X, if the data rate is 20Mbit/s then the read data frequency would be 20 • M = 20 • 1.5 = 30 Mbit/s.

Example;

Assuming a SSI 32D5372 running at a data rate of 20Mbit/s,

tmax = 16 • 3/(20E6 • 1.5) = 1.6 µs

Therefore, the PLL has 1.6 µs to settle within an acceptable amount of error before tracking and decoding data.

To determine the components of the loop filter, the next step is to calculate the typical phase detector gain (Kd) and VCO control gain (KVCO) of the specific data synchronizer device.

In Table B is the typical Kd and KVCO equations of the current data synchronizer family, check the latest product data sheet to ensure that the equations have not changed during the product characterization cycle.

**Table B**

| DEVICE | Kd (μA/rad) | KVCO |
|---|---|---|
| 5371/2 | 660/(RR + 0.53)* | 0.20 • 2 • π/(2To)** |
| 5373/4 | 660/(RR + 0.53)* | 0.20 • 2 • π/(2To) |
| 539 | 750/(RR + 0.42)* | 0.20 • 2 • π/To |
| 5392 | 220/(RR + 0.53)* | 0.20 • 2 • π/To |
| 5393 | 660/(RR + 0.53)* | 0.20 • 2 • π/To |

Where: To: is the VCO Center frequency period
RR: is the reference resistor connected to the IR pin
KD: is normalized for a 1F read data pattern

*Note: This device switches the phase detector gain between read and non-read modes to optimize locking between the reference frequency and read data (and back again.) The equation given in the table is for read mode.

**Note: The VCO frequency in this device is divided by two before entering the phase detector. The additional '2' in the denominator normalizes KVCO for the following loop filter equations.

***Note: A reference current, Iref, may be used instead of RR. These two are associated by the following equation RR = (Vcc - 0.7)/Iref - r. "r" is the constant added to RR in the equation for KD.

In general, it is desirable to have the loop damping factor "ζ" between 0.5 and 1.0 during acquisition. For a high gain, second-order loop this results in minimal noise bandwidth.

To determine the bandwidth $\omega_n$, one must decide what the acceptable phase error will be when the PLL switches from the reference frequency to read data after the locking time, Tmax, is complete. As shown in figure 2, with $\zeta = 0.7$, choosing $\omega_n T = 2.3$ the phase error will be at most 22% of the initial phase error, 7.5% at $\omega_n T = 4.0$, etc. The bandwidth is then $\omega_n = (\omega_n T)/Tmax$; where Tmax is the settling time of the PLL calculated above.

We now have enough information to calculate the loop filter components:

$C1 = N \cdot Kd \cdot KVCO/(\omega_n)^2$ $\quad R = 2 \cdot$ "ζ" $\cdot \omega_n/(N \cdot KD \cdot KVCO)$ $C2 = C1/10$

where:

Kd = Phase Detector gain (μA/rad)
KVCO = VCO control gain (rad/s V)
N = The ratio of the reference input frequency to the VCO output frequency.
(For a '3T' preamble N = 0.33, '4T' preamble N = 0.25)
$\omega_n$ = Acceptable loop bandwidth
"ζ" = Acceptable loop damping factor

Example:

SSI 32D5393 running at 40 Mbit/s.

From Table A

xT = 3; Ln = 16; M = 1.5

Tmax = Ln • 'xT'/(DR • M) = 16 • 3(40E6 • 1.5) = 0.8 μs

For this example, we want the acceptable phase error when the VCO is switched from the reference frequency to read data to be less than 15% of the initial phase error. This results, from figure 2 and "ζ" = 0.7, in a wn(Tmax) between 3 and 4. To simplify the results let $\omega_n$(Tmax) = 3.2. Since the data synchronizer family employs a zero phase restart technique to reduce the initial phase error (a design goal of ± one rad is typical for the family.) The initial phase error has been characterized to be typically 6ns for the SSI 32D5362A. Thus the acceptable phase error will be 0.15 • 6 = 0.9 ns when the VCO is switched.

$\omega_n$(Tmax) = 3.2 $\omega_n$ = 3.2/.8E-6 = 4 µrad/s

RR = (185/DR) - 1.7 kΩ = 2.925 kΩ

From Table B

KD = 6600/(RR + 0.53) = 191 µrad/s

KVCO = 0.2 • 2 • π/To = 0.2 • 2 • π/(1.67E - 9) = 75.4 µrad/s (s • V)

C1 = N • KVCO • KD/($\omega_n$)2 = 0.33 • 75.4 • 191/(4E6)2 = 297pF

C2 = C1/10 = 29.7 pF

R1 = 2 • "ζ" • $\omega_n$/(N • KD • KVCO) = 2 • 0.7 • 4E6/(0.33 • 191 • 75.4) = 1178Ω

## LAYOUT CONSIDERATIONS

As with other high frequency analog devices the SSI 32D5371/72 requires care in layout. The designer should keep analog signal lines as short as possible and well balanced. Use of a ground plane is recommended, along with supply bypassing to separate the SSI 32D5371/72, and associated circuitry, from other circuits on the PCB.

The following is a list of recommended component values based on the above calculations. It is important to note that these values should be considered a starting point in designing a loop filter for a specific drive application, the optimal bandwidth and requirements for re-locking back to the reference frequency after read mode has been terminated have not been considered.

**32D5371/5372**

| DATA RATE (Mbit/s) | DAMPING FACTOR,ζ | LOCK TIME $t_{max}$ (µs) | $\omega_n t$ | BANDWIDTH $\omega_n \left(\frac{rad}{sec}\right)$ | KD $\left(\frac{\mu A}{rad}\right)$ | KVCO $\left(\frac{\mu A}{s\text{-}V}\right)$ | EXTERNAL COMPONENT VALUES | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | RR(kΩ) | R(kΩ) | $C_1$ (pF) | $C_2$ (pF) |
| 10 | 0.7 | 3.2 | 3.2 | $1.0 \times 10^6$ | 81.58 | 18.84 | 7.56 | 2.76 | 507 | 50.7 |
| 20 | 0.7 | 1.6 | 3.2 | $2 \times 10^6$ | 190.75 | 37.68 | 2.93 | 1.18 | 593 | 59.3 |

**32D5373/5374**

| DATA RATE (Mbit/s) | DAMPING FACTOR,ζ | LOCK TIME $t_{max}$ (µs) | $\omega_n t$ | BANDWIDTH $\omega_n \left(\frac{rad}{sec}\right)$ | KD $\left(\frac{\mu A}{rad}\right)$ | KVCO $\left(\frac{\mu A}{s\text{-}V}\right)$ | EXTERNAL COMPONENT VALUES | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | RR(kΩ) | R(kΩ) | $C_1$ (pF) | $C_2$ (pF) |
| 15 | 0.7 | 2.1 | 3.2 | $1.5 \times 10^6$ | 81.58 | 28.26 | 7.56 | 2.76 | 338 | 33.8 |
| 32 | 0.7 | 1.0 | 3.2 | $3.2 \times 10^6$ | 207.96 | 60.28 | 2.64 | 108 | 404 | 40.4 |

**32D539**

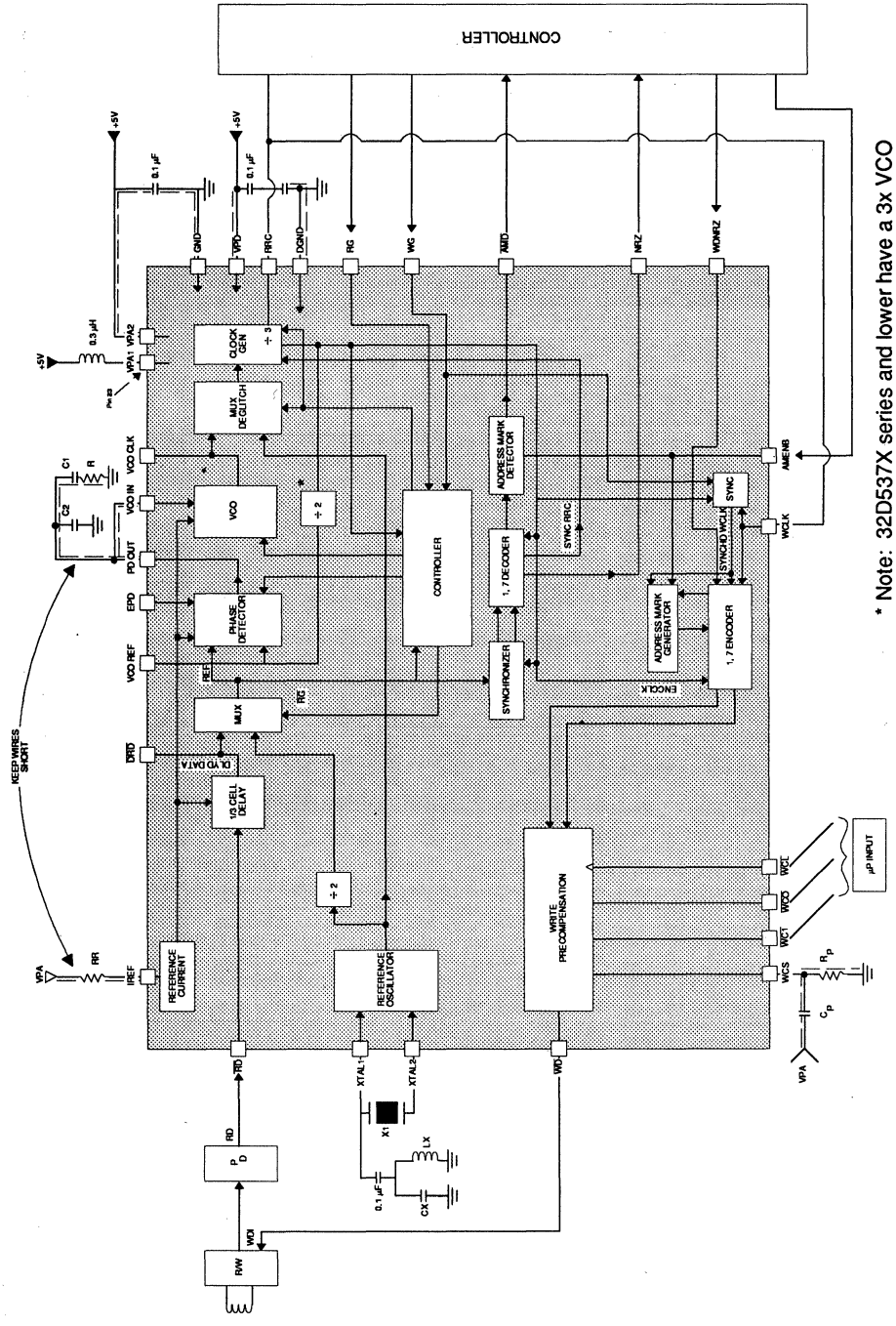
| DATA RATE (Mbit/s) | DAMPING FACTOR,ζ | LOCK TIME $t_{max}$ (μs) | $\omega_n t$ | BANDWIDTH $\omega_n\left(\frac{rad}{sec}\right)$ | KD $\left(\frac{\mu A}{rad}\right)$ | KVCO $\left(\frac{\mu A}{s\text{-}V}\right)$ | EXTERNAL COMPONENT VALUES | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | RR(kΩ) | R(kΩ) | $C_1$ (pF) | $C_2$ (pF) |
| 36 | 0.7 | 0.89 | 3.2 | $3.6 \times 10^6$ | 194.35 | 67.82 | 3.44 | 1.16 | 336 | 33.6 |
| 48 | 0.7 | 0.67 | 3.2 | $4.8 \times 10^6$ | 291.35 | 90.43 | 2.15 | 0.77 | 377 | 37.7 |

**32D5392**

| DATA RATE (Mbit/s) | DAMPING FACTOR,ζ | LOCK TIME $t_{max}$ (μs) | $\omega_n t$ | BANDWIDTH $\omega_n\left(\frac{rad}{sec}\right)$ | KD $\left(\frac{\mu A}{rad}\right)$ | KVCO $\left(\frac{\mu A}{s\text{-}V}\right)$ | EXTERNAL COMPONENT VALUES | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | RR(kΩ) | R(kΩ) | $C_1$ (pF) | $C_2$ (pF) |
| 36 | 0.7 | 0.89 | 3.2 | $3.6 \times 10^6$ | 55.41 | 67.82 | 3.44 | 4.05 | 99 | 9.9 |
| 40 | 0.7 | 0.80 | 3.2 | $4 \times 10^6$ | 63.68 | 75.36 | 2.92 | 3.54 | 96 | 9.6 |

**32D5393**

| DATA RATE (Mbit/s) | DAMPING FACTOR,ζ | LOCK TIME $t_{max}$ (μs) | $\omega_n t$ | BANDWIDTH $\omega_n\left(\frac{rad}{sec}\right)$ | KD $\left(\frac{\mu A}{rad}\right)$ | KVCO $\left(\frac{\mu A}{s\text{-}V}\right)$ | EXTERNAL COMPONENT VALUES | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | RR(kΩ) | R(kΩ) | $C_1$ (pF) | $C_2$ (pF) |
| 36 | 0.7 | 0.89 | 3.2 | $3.6 \times 10^6$ | 166.29 | 67.82 | 3.44 | 1.35 | 297 | 29.7 |
| 40 | 0.7 | 0.80 | 3.2 | $4 \times 10^6$ | 191.03 | 75.36 | 2.92 | 1.18 | 287 | 28.7 |




* Note: 32D537X series and lower have a 3x VCO
32D539X series has a 1.5X VCO (no need for ÷ 2)

**FIGURE 5: Typical Application**

## LAYOUT CONSIDERATIONS

As with other high frequency devices the data synchronizer family requires care in layout. The designer should keep analog signal lines as short as possible and well balanced. Use of a ground plane is recommended, along with supply bypassing, to separate the data synchronizer device and associated circuitry from other circuits on the PCB. It is also recommended that an inductor (~0.3µH) be placed in series with the analog supply which supports the VCO circuitry on the higher data rate (1,7) RLL products. This is generally VPA1, but check the application diagram in the specific product data sheet for more information. This additional filtering has been shown to be effective in reducing VCO jitter, which can degrade window margin performance.

## TEST POINTS

The SSI 32D5362A, 5371/5372/5373/5374, 539 provide three (3) test points which can be utilized to evaluate window margin characteristics.

(a) $\overline{DRD}$, delayed read data – the positive edges represent the data bit position
(b) VCO REF, the VCO reference which represents the input to the Phase Detector, synchronizer, and 1,7 decoder
(c) VCO CLK, the VCO clock output which represents the output of the VCO

The following figure describes the relationship between the various test points:

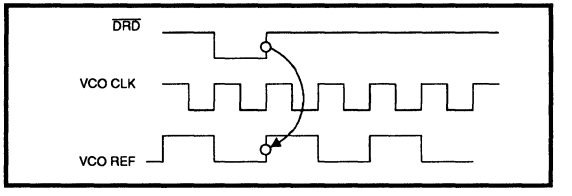



**FIGURE 6: Test Point Relationships**



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**Notes:**

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# SSI 32F8001
## Programmable Electronic Filter

**Application Note**

December 1992

## INTRODUCTION

Analog filtering is a universal requirement in any signal processing system. Filter design is now made easy with the programmable filters from Silicon Systems Inc. Whether the requirement is a fixed filtering characteristic or a programmable response, this family of programmable filters offers distinct advantages of design simplicity, accuracy, versatility and board space saving. Additional features, such as high frequency boost, differentiated outputs, are also available. This application note focuses on the SSI 32F8001, cutoff frequency programmable from 9-27 MHz.

The objectives of this application note are:

- To present a description of the SSI 32F8001
- To discuss its applications
- To present a typical fixed response design
- To present a programmable response application

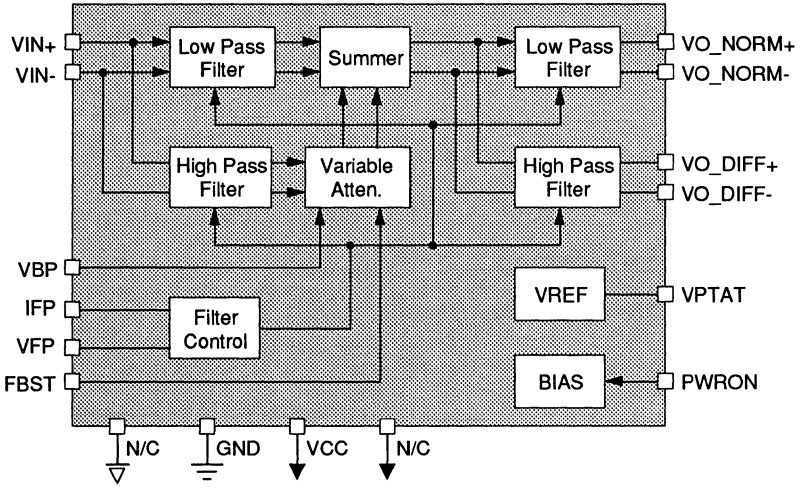


**FIGURE 1: Block Diagram**

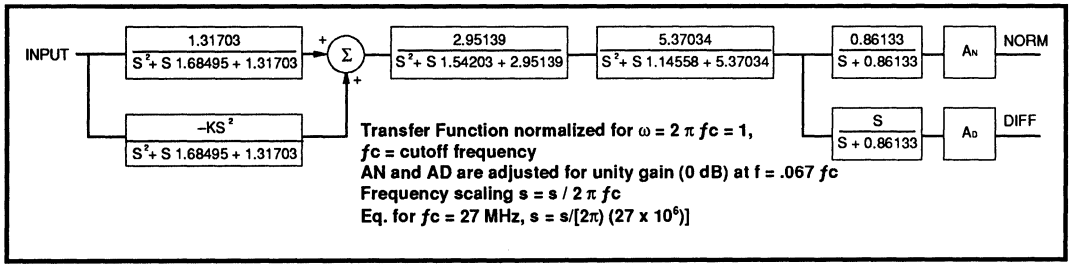


**FIGURE 2: The SSI 32F8001 Transfer Function**



CAUTION: Use handling procedures necessary for a static sensitive component.

## 1.0 DESCRIPTION

The SSI 32F8001 is a programmable 7-pole 0.05° equiripple linear phase low pass filter in a silicon bipolar integrated circuit. Figures 1 and 2 show the block diagram and the filter transfer function.

The SSI 32F8001 cutoff frequency and high frequency boost can be independently controlled by two control signals. Two sets of filter outputs are available: normal low pass output and differentiated low pass output. As an equiripple linear phase type filter, the filter outputs exhibit constant group delay in the pass band and out to 1.75 $fc$. Furthermore, the delays through the normal output and the differentiated output are well matched.

The input and outputs of the SSI 32F8001 are differential signals, requiring external AC coupling capacitors. The given transfer function shows the relationship between the input and the two sets of outputs. Typical differential input resistance is 4 kΩ.

### 1.1 CUTOFF FREQUENCY PROGRAMMING

The cutoff frequency, defined to be the -3dB corner frequency with no boost, can be programmed between 9 - 27 MHz. It can be set by one of three methods:

- A resistor can be inserted between the VPTAT and the VFP pins. This setting is only used for a fixed response design. The IFP pin should be left open. The design equation for this resistor value is:

  Rx (kΩ) = 27 / $fc$ (MHz)

  A design example is given in Section 4.

- A current source input can be fed into the IFP pin. The VFP pin should be left open. A current source digital-to-analog converter (DAC), such as the DACF in the SSI 32D4661 Time Base Generator, allows a microcontroller to change the filter response dynamically. To achieve the highest accuracy the current source DAC should be referenced to the reference voltage at the VPTAT pin. The design equation for this current source value is:

  IFP (mA) = 0.0222 x $fc$ (MHz)

  A design example is given in Section 4.

- A current sink input can be fed into the IFP pin. A 1 kΩ resistor should be placed across the VPTAT and the VFP pins. With a current sink DAC, this design also allows a microcontroller to change the filter response dynamically. To achieve the highest accuracy and temperature stability, the current sink DAC should be referenced to the reference voltage at the VPTAT pin. The design equation for this current sink value is:

  IFP (mA) = 0.0222 x (27 - $fc$) (MHz)

  A design example is given in Section 4.

### 1.2 HIGH FREQUENCY BOOST CONTROL

The high frequency boost function is especially desirable for pulse slimming and magnitude equalization applications. This function can be enabled or disabled by a TTL logic input at the FBST pin. With FBST = '1' or open, the amount of high frequency boost, measured at the cutoff frequency, can be programmed from 0 to 13 dB at $fc$ by a voltage input at the VBP pin. External resistors can be designed in for a fixed filter response. For a programmable high frequency boost, a voltage DAC, such as the DACS in the SSI 32D4661 Time Base Generator, can be used to control the VBP pin. This input voltage should be made proportional to the reference voltage at the VPTAT pin for accuracy. The design equation for this control voltage is:

VBP = VPTAT x (10^(FB/20) - 1) / 3.46 where FB is in dB.

Design example is given in Section 3.

With a finite boost, the magnitude response peaks at a frequency slightly higher than the original cutoff frequency. The effective pass band bandwidth is wider.

### 1.3 OTHER FEATURES OF THE SSI 32F8001

The SSI 32F8001 features excellent constant group delay. At $fc$ = 27 MHz, the group delay variation from 0.2 $fc$ to $fc$ is less than 0.5 ns. Furthermore, the high frequency boost function does not affect the group delay variation. Group delay variation is within ±3% out to 1.75 $fc$.

In addition to the normal low pass output, the SSI 32F8001 also provides a differentiated low pass output of the input signal. The signal delay is well matched to the normal output.

The SSI 32F8001 provides a reference voltage VPTAT for the DAC references. Because the internal filter control circuitry is referenced to VPTAT, the control current for filter cutoff frequency and control voltage for high frequency boost should be referenced to VPTAT.

The SSI 32F8001 can be switched into a sleep mode, dissipating less than 3 mW, by a TTL input at PWRON.

Two package options are available for the SSI 32F8001: 16-lead SOL and 16-lead SON. The small feature size of the 16-lead SON package offers significant board space saving.

## 2.0 APPLICATIONS

A programmable filter is a versatile component in any signal processing system. Some areas of applications include fixed response filtering, variable data rate processing and adaptive equalization.

For fixed response filtering applications, the SSI 32F8001 offers a simple-to-use solution. The once complex design of cutoff frequency or magnitude equalization is now rendered to simple resistance calculation. The narrow 16-pin small outline package offers significant board space economy.

In variable data rate processing, a programmable filter can be used to optimize bandwidth and signal-to-noise tradeoff. One application is constant density recording for high capacity storage products. As the data rate increases from the inner tracks to the outer tracks, the filter cutoff frequency can be scaled accordingly to maximize the signal-to-noise performance. The high frequency boost function provides pulse slimming for accurate pulse detection.

A programmable filter offers a revolutionary approach to adaptive equalization. In signal transmission applications, an equalization filter is used to combat channel distortion. The magnitude of channel distortion is often not known a priori. Adaptive equalization can dynamically shape the equalization function. With an appropriate external adaptive sensing function, the cutoff frequency and the high frequency boost of the SSI 32F8001 can be dynamically programmed through microprocessor control.

## 3.0 FIXED RESPONSE DESIGN PROCEDURE

This section suggests some design guidelines to apply the SSI 32F8001 as a fixed response filter. Figure 3 shows the design schematic. Rx determines the filter's cutoff frequency, defined as the -3 dB frequency with no boost. The ratio of RB1 and RB2 determines the amount of high frequency boost.

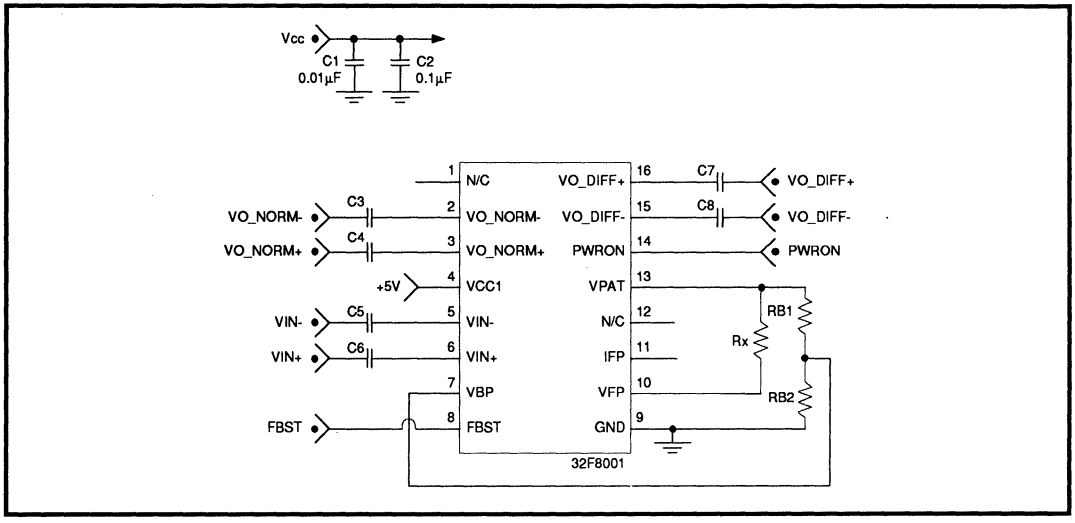


**FIGURE 3: The 32F8001 Setup as a Fixed Response Filter**

## 3.0 FIXED RESPONSE DESIGN PROCEDURE (continued)

Given $fc$, cutoff frequency in MHz, and FB, high frequency boost in dB:

- Rx can be calculated, as given in Section 1.
  Rx (kΩ) = 27 / $fc$ (MHz)
  Voltage across Rx is 0.33 VPTAT. The current through Rx is 0.33 (VPTAT / Rx).
  Rx should be between 1 kΩ to 3 kΩ, i.e., $fc$ between 9 MHz to 27 MHz.
- RB1/RB2 sets FB, and can be determined as follows:
  RB1 / RB2 = 3.46 / (10^( FB / 20 ) - 1) - 1
- Total current drawn out of the VPTAT pin should be limited to 2 mA max. Thus, RB1 and RB2 should be designed accordingly.
- The IFP pin should be left open.

## 4.0 PROGRAMMABLE RESPONSE DESIGN PROCEDURE

This section suggests some design guidelines to apply the SSI 32F8001 as a programmable filter. The high frequency boost can be controlled by a voltage DAC driving the VBP pin. The VBP voltage should be between 0 and VPTAT. The cutoff frequency can be controlled by a current DAC. The application setup for using a current source DAC is different from the one using a current sink DAC. Both are presented below.

### 4.1 PROGRAMMABLE FILTER USING A CURRENT SOURCE DAC

Figure 4 shows the setup schematic of the SSI 32F8001 using an external current source DAC to control the filter's cutoff frequency.

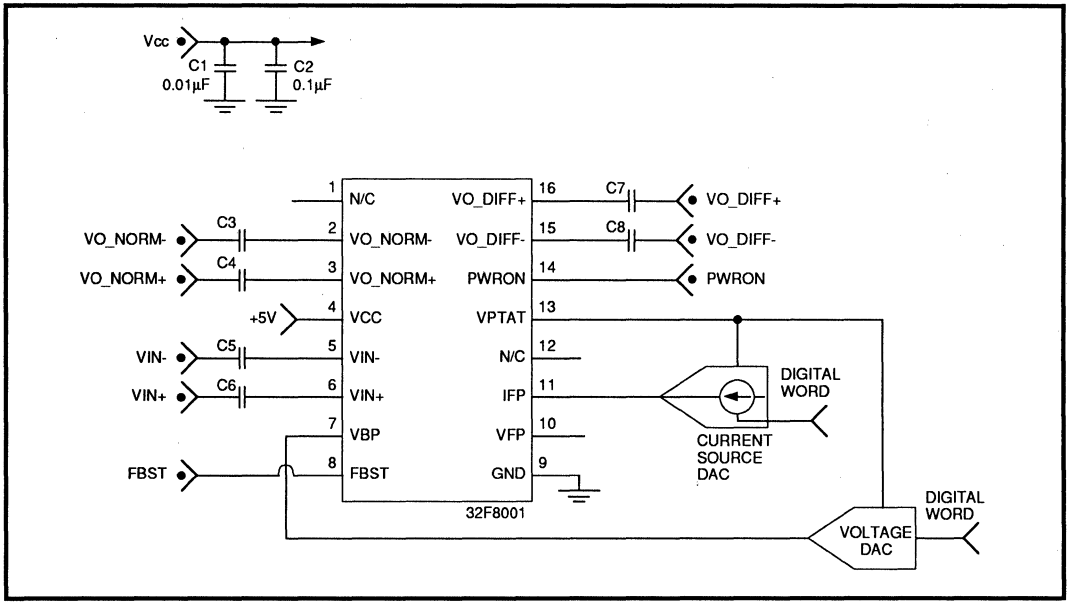


**FIGURE 4: The SSI 32F8001 Setup Schematic Using a Current Source DAC for Cutoff Frequency Control**

Design guidelines for the SSI 32F8001:

- The VFP pin should be left open.
- Both the current source DAC and the voltage DAC should reference to VPTAT for accuracy.
- The reference bias current drawn from VR should be less than 2 mA.
- The current source output voltage compliance should be between 1.1V to 1.8V.
- The IFP current and the filter cutoff frequency are related as follows:

  $fc\ (MHz) = 45 \times IFP\ (mA) \times \frac{1.8}{VPTAT}$

  IFP should be between 0.2 mA to 0.6 mA with VPTAT = 1.8V (at room temperature).
- The VBP voltage and the high frequency boost are related as follows:

  FB = 20 x log (3.46 x VBP / VPTAT + 1) dB

### 4.2 PROGRAMMABLE FILTER USING CURRENT SINK DAC

Figure 5 shows the setup schematic of the SSI 32F8001 using an external current sink DAC to control the filter's cutoff frequency. The high frequency boost control is the same as in Section 4.1.

Some design guidelines:

- Rx should be set to 1 kΩ between VPTAT and VFP.
- Both the current source DAC and the voltage DAC should reference to VPTAT for accuracy and temperature stability.
- The total current drawn from VPTAT should be less than 2mA. This includes the 0.6mA through Rx. Thus, the current sink DAC and the voltage DAC reference should not draw more than 1.4 mA.
- The current sink DAC output voltage compliance should be between 0.8V to 1.4V.
- The IFP current and the cutoff frequency are related as follows:

  $fc\ (MHz) = 27 - 45 \times IFP\ (mA) \times \frac{VPTAT}{1.8}$

  IFP should be between 0 mA to 0.4 mA.

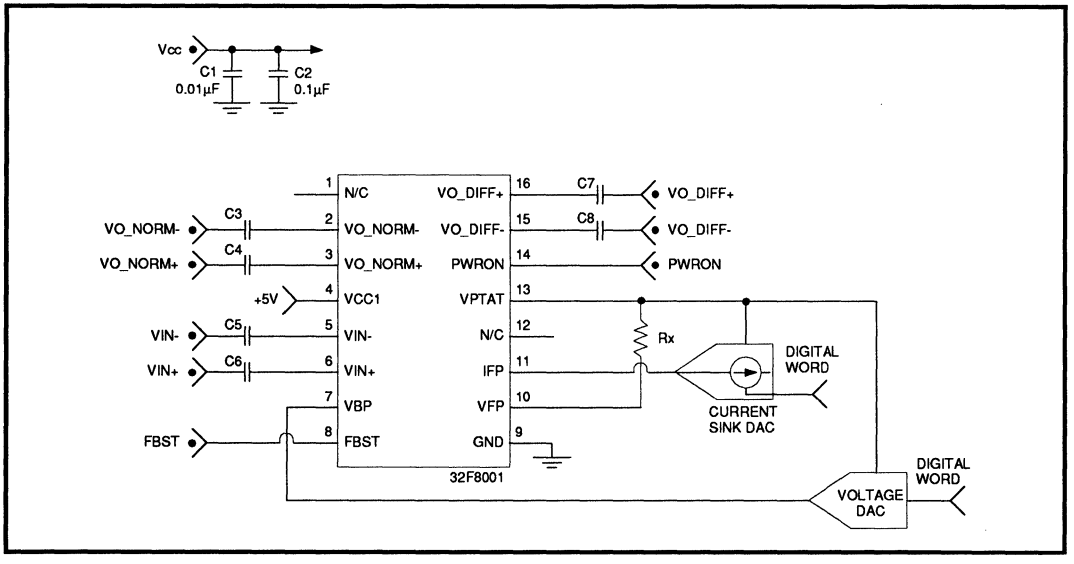


**FIGURE 5: The SSI 32F8001 Setup Schematic Using a Current Sink DAC for Cutoff Frequency Control**

**Notes:**

# SSI 32F8011
## Programmable Electronic Filter

**Application Note**

December 1992

## INTRODUCTION

Analog filtering is a universal requirement in any signal processing system. Filter design is now made easy with the programmable filters from Silicon Systems Inc. Whether the requirement is a fixed filtering characteristic or a programmable response, this family of programmable filters offers distinct advantages of design simplicity, accuracy, versatility and board space saving. Additional features, such as high frequency boost, differentiated outputs, are also available. This application note focuses on the SSI 32F8011, cutoff frequency programmable from 5 - 13 MHz.

The objectives of this application note are:

- To present a description of the SSI 32F8011
- To discuss its applications
- To present a typical fixed response design
- To present a programmable response application

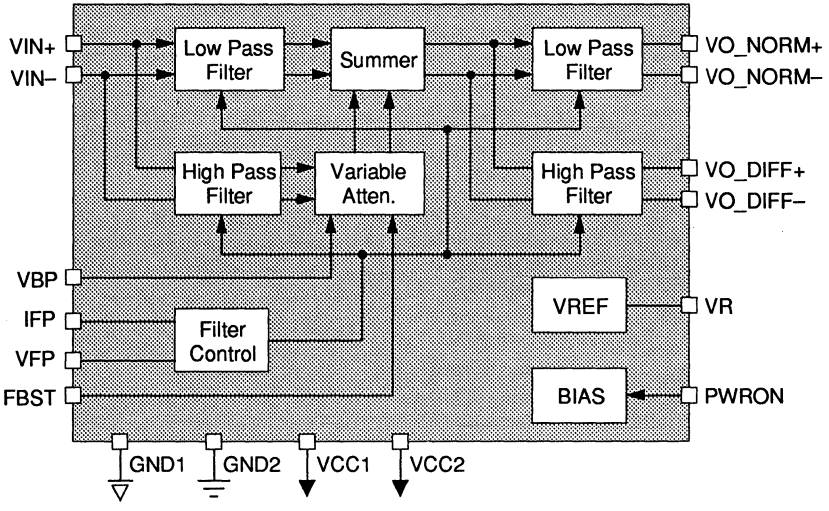


**FIGURE 1: Block Diagram**

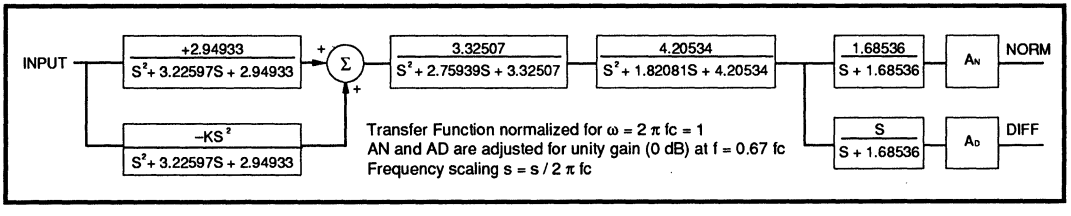


**FIGURE 2: The SSI 32F8011 Transfer Function**

# SSI 32F8011
# Programmable Electronic Filter

## Application Note

## 1.0 DESCRIPTION

The SSI 32F8011 is a programmable 7-pole Bessel low pass filter in a silicon bipolar integrated circuit. Figures 1 and 2 show the block diagram and the filter transfer function.

The SSI 32F8011 cutoff frequency and high frequency boost can be independently controlled by two control signals. Two sets of filter outputs are available: normal low pass output and differentiated low pass output. As a Bessel type filter, the filter outputs exhibit constant group delay in the pass band. Furthermore, the delays through the normal output and the differentiated output are well matched.

The input and outputs of the SSI 32F8011 are differential signals, requiring external AC coupling capacitors. The given transfer function shows the relationship between the input and the two sets of outputs. The maximum input signal is 1.5 Vpp differential, with differential input resistance 4 kΩ typical. The minimum recommended output load is 1 kΩ differential, AC coupled.

### 1.1 CUTOFF FREQUENCY PROGRAMMING

The cutoff frequency, defined to be the -3dB corner frequency with no boost, can be programmed between 5 - 13 MHz. It can be set by one of three methods:

- A resistor can be inserted between the VR and the VFP pins. This setting is only used for a fixed response design. The IFP pin should be left open. The design equation for this resistor value is:

  Rx (kΩ) = 11.92 / fc (MHz)

  A design example is given in Section 4.

- A current source input can be fed into the IFP pin. The VFP pin should be left open. With a current source digital-to-analog converter (DAC), such as the DACF in the SSI 32D4661, this design allows a microcontroller to change the filter response dynamically. To achieve the highest accuracy and temperature stability, the current source DAC should be referenced to the temperature compensated reference voltage at the VR pin. The design equation for this current source value is:

  IFP (mA) = 0.0615 x fc (MHz)

  A design example is given in Section 4.

- A current sink input can be fed into the IFP pin. A 917Ω resistor should be placed across the VR and the VFP pins. With a current sink DAC, this design also allows a microcontroller to change the filter response dynamically. To achieve the highest accuracy and temperature stability, the current sink DAC should be referenced to the temperature compensated reference voltage at the VR pin. The design equation for this current sink value is:

  IFP (mA) = 0.0615 x (13 - fc) (MHz)

  A design example is given in Section 4.

### 1.2 HIGH FREQUENCY BOOST CONTROL

The high frequency boost function is especially desirable for pulse slimming and magnitude equalization applications. This function can be enabled or disabled by a TTL logic input at the FBST pin. With FBST = '1' or open, the amount of high frequency boost, measured at the cutoff frequency, can be programmed from 0 to 9 dB at $fc$ by a voltage input at the VBP pin. External resistors can be designed in for a fixed filter response. For a programmable high frequency boost, a voltage DAC, such as the DACS in the SSI 32D4661 Time Base Generator, can be used to control the VBP pin. This input voltage should be made proportional to the reference voltage at the VR pin for accuracy and temperature stability. The design equation for this control voltage is:

VBP = VR x (10^(FB/20) - 1) / 1.884 where FB is in dB.

Design example is given in Section 3.

With a finite boost, the magnitude response peaks at a frequency slightly higher than the original cutoff frequency. The effective pass band bandwidth is wider.

### 1.3 OTHER FEATURES OF THE SSI 32F8011

The SSI 32F8011 is a 7-pole Bessel type filter. It features excellent constant group delay. At $fc$ = 13 MHz, the group delay variation from 0.2 fc to fc is less than 1ns. Furthermore, the high frequency boost function does not affect the group delay variation.

In addition to the normal low pass output, the SSI 32F8011 also provides a differentiated low pass output of the input signal. The signal delay is well matched to the normal output.

### 1.3 OTHER FEATURES OF THE SSI 32F8011 (continued)

The SSI 32F8011 provides a temperature compensated reference voltage, VR, for the DAC references. Because the internal filter control circuitry is referenced to VR, the control current for filter cutoff frequency and control voltage for high frequency boost should be referenced to VR.

The SSI 32F8011 can be switched into a sleep mode, dissipating only 60 mW, by a TTL input at PWRON.

Two package options are available for the SSI 32F8011: 16-lead SOL and 16-lead SON. The small feature size of the 16-pin SON package offers significant board space saving.

## 2.0 APPLICATIONS

A programmable filter is a versatile component in any signal processing system. Some areas of applications include fixed response filtering, variable data rate processing and adaptive equalization.

For fixed response filtering applications, the SSI 32F8011 offers a simple-to-use solution. The once complex design of cutoff frequency or magnitude equalization is now rendered to simple resistance calculation. The narrow 16-pin small outline package offers significant board space economy.

In variable data rate processing, a programmable filter can be used to optimize bandwidth and signal-to-noise tradeoff. One application is constant density recording for high capacity storage products. As the data rate increases from the inner tracks to the outer tracks, the filter cutoff frequency can be scaled accordingly to maximize signal-to-noise performance. The high frequency boost function provides pulse slimming for accurate pulse detection.

Programmable filter offers a revolutionary approach to adaptive equalization. In signal transmission applications, an equalization filter is used to combat channel distortion. The magnitude of channel distortion is often not known a priori. Adaptive equalization can dynamically shape the equalization function. With an appropriate external adaptive sensing function, the cutoff frequency and the high frequency boost of the SSI 32F8011 can be dynamically programmed through microprocessor control.

## 3.0 FIXED RESPONSE DESIGN PROCEDURE

This section suggests some design guidelines to apply the SSI 32F8011 as a fixed response filter. Figure 3 shows the design schematic. Rx determines the filter's cutoff frequency, defined as the -3 dB frequency with no boost. The ratio of RB1 and RB2 determines the amount of high frequency boost.

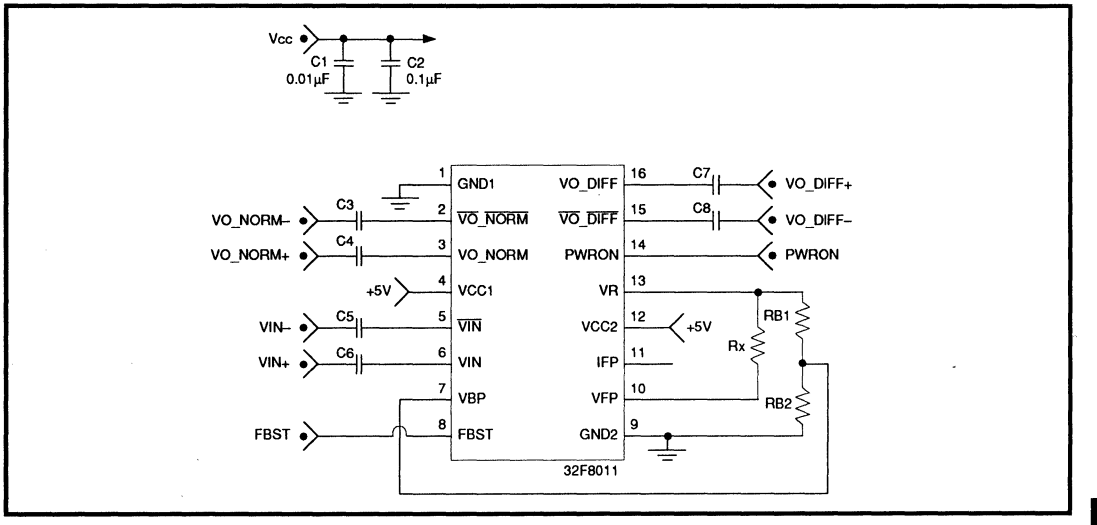


**FIGURE 3: The 32F8011 Setup as a Fixed Response Filter**

## 3.0 FIXED RESPONSE DESIGN PROCEDURE (continued)

Given fc, cutoff frequency in MHz, and FB, high frequency boost in dB:

- Rx can be calculated, as given in Section 1.
  Rx (kΩ) = 11.92 / fc (MHz)
  Voltage across Rx is 0.33 VR. The current through Rx is 0.33 (VR / Rx).
  Rx should be between 917 Ω to 2.38 kΩ, i.e., fc between 5 MHz to 13 MHz.
- RB1/RB2 sets FB, and can be determined as follows:
  RB1 / RB2 = 1.884 / (10^( FB / 20 ) - 1) - 1
- Total current drawn out of the VR pin should be limited to 2 mA max. Thus, RB1 and RB2 should be designed accordingly.
- The IFP pin should be left open.

## 4.0 PROGRAMMABLE RESPONSE DESIGN PROCEDURE

This section suggests some design guidelines to apply the SSI 32F8011 as a programmable filter. The high frequency boost can be controlled by a voltage DAC driving the VBP pin. The VBP voltage should be between 0 and VR. The cutoff frequency can be controlled by a current DAC. The application setup for using a current source DAC is different from the one using a current sink DAC. Both are presented below.

### 4.1 PROGRAMMABLE FILTER USING A CURRENT SOURCE DAC

Figure 4 shows the setup schematic of the SSI 32F8011 using an external current source DAC to control the filter's cutoff frequency.

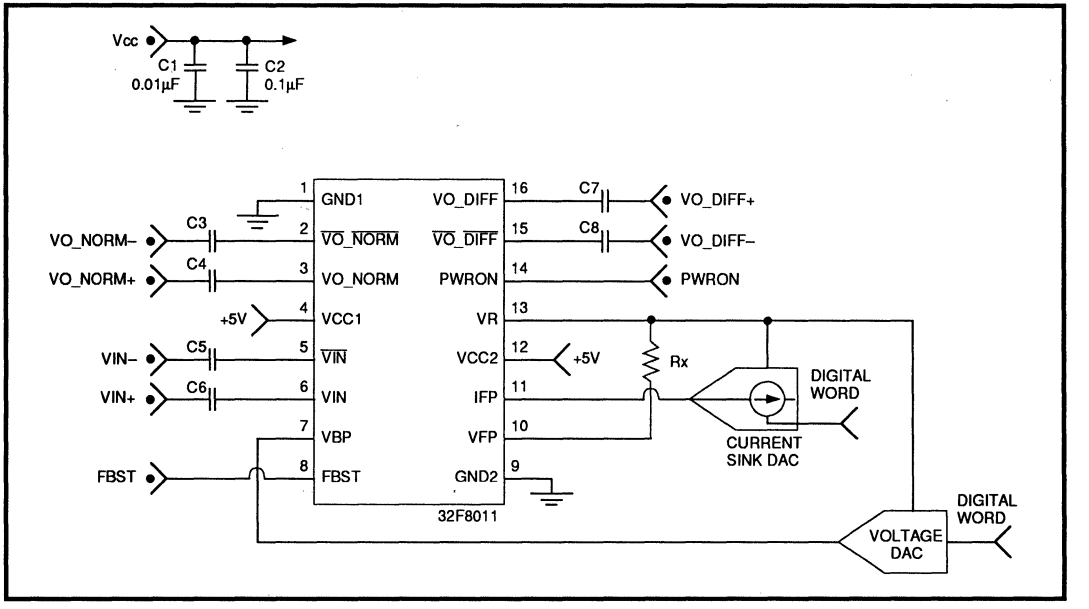


**FIGURE 4: The SSI 32F8011 Setup Schematic Using a Current Source DAC for Cutoff Frequency Control**

### 4.1 PROGRAMMABLE FILTER USING A CURRENT SOURCE DAC (continued)

Some design guidelines:

- The VFP pin should be left open.
- Both the current source DAC and the voltage DAC should reference to VR for accuracy and temperature stability.
- The reference bias current drawn from VR should be less than 2 mA.
- The current source output voltage compliance should be > 2.0 V.
- The IFP current and the filter cutoff frequency are related as follows:

  $fc\ (MHz) = 16.25 \times IFP\ (mA) \times \frac{VR}{2.2}$

  IFP should be between 0.31 mA to 0.8 mA with VR = 2.2V.
- The VBP voltage and the high frequency boost are related as follows:

  $FB = 20 \times \log (1.884 \times VBP / VR + 1)\ dB$

### 4.2 PROGRAMMABLE FILTER USING CURRENT SINK DAC

Figure 5 shows the setup schematic of the SSI 32F8011 using an external current sink DAC to control the filter's cutoff frequency. The high frequency boost control is the same as in Section 4.1.

Some design guidelines:

- Rx should be set to 917Ω between VR and VFP.
- Both the current source DAC and the voltage DAC should reference to VR for accuracy and temperature stability.
- The total current drawn from VR should be less than 2mA. This includes the 0.8mA through Rx. Thus, the current sink DAC and the voltage DAC reference should not draw more than 1.2 mA.
- The current sink DAC output voltage compliance should be between 0.75V to 1.2V.
- The IFP current and the cutoff frequency are related as follows:

  $fc\ (MHz) = 13 - 16.25 \times IFP\ (mA) \times \frac{VR}{2.2}$

  IFP should be between 0 mA to 0.49 mA.

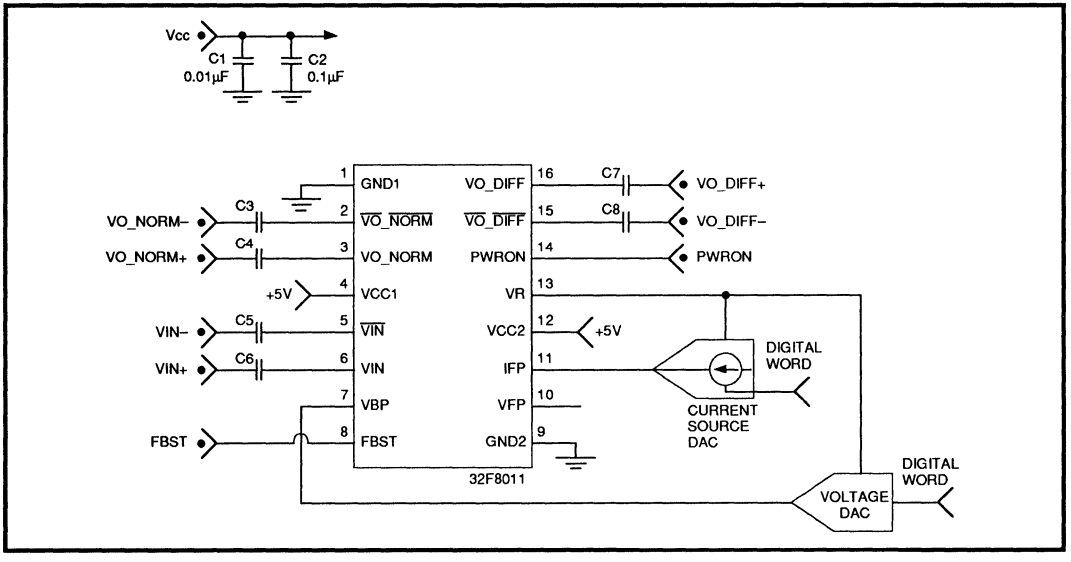


**FIGURE 5: The SSI 32F8011 Setup Schematic Using a Current Sink DAC for Cutoff Frequency Control**

**Notes:**

# SSI 32F8020A
## Programmable Electronic Filter

**Application Note**

October 1992

## INTRODUCTION

Analog filtering is a universal requirement in any signal processing system. Filter design is now made easy with the programmable filters from Silicon Systems Inc. Whether the requirement is a fixed filtering characteristic or a programmable response, this family of programmable filters offers distinct advantages of design simplicity, accuracy, versatility and board space savings. Additional features, such as high frequency boost, differentiated outputs, are also available. This application note focuses on the SSI 32F8020A, cutoff frequency programmable from 1.5 - 8 MHz.

The objectives of this application note are:

- To present a description of the SSI 32F8020A
- To discuss its applications
- To present a typical fixed response design
- To present a programmable response application

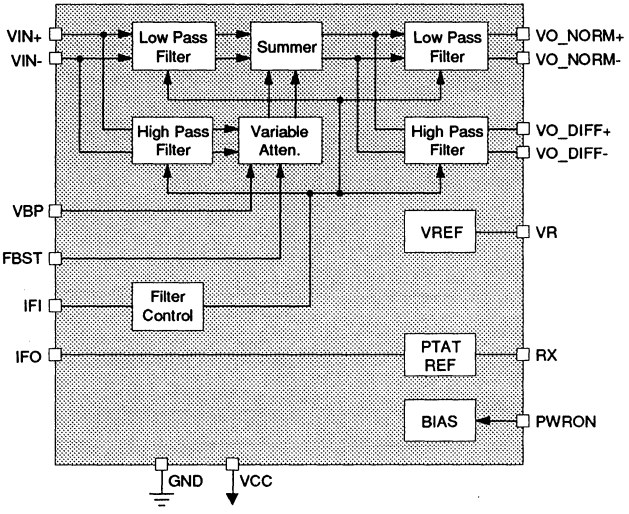


**FIGURE 1: Block Diagram**

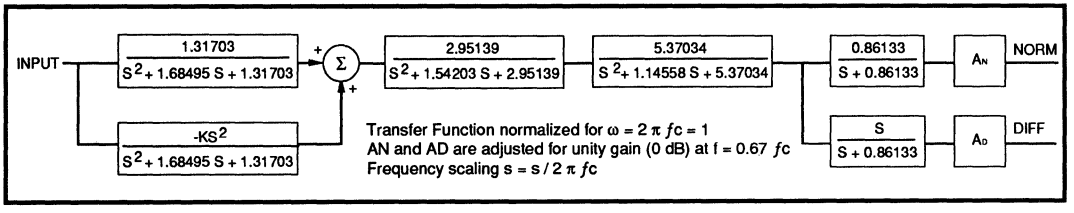


**FIGURE 2: The SSI 32F8020A Transfer Function**



CAUTION: Use handling procedures necessary for a static sensitive component.

# SSI 32F8020A
# Programmable Electronic Filter

## Application Note

## 1.0 DESCRIPTION

The SSI 32F8020A is a programmable 7-pole 0.05° equiripple low pass filter in a silicon bipolar integrated circuit. Figures 1 and 2 show the block diagram and the filter transfer function.

The SSI 32F8020A cutoff frequency and high frequency boost can be independently controlled by two control signals. Two sets of filter outputs are available: normal low pass output and differentiated low pass output. As a 0.05° equiripple type filter, the filter outputs exhibit constant group delay beyond its cutoff frequency. Furthermore, the delays through the normal output and the differentiated output are well matched.

The input and outputs of the SSI 32F8020A are differential signals, requiring external ac coupling capacitors. The given transfer function shows the relationship between the input and the two sets of outputs. The maximum input signal is 2.0 Vpp differential. The differential input resistance is 4 kΩ (typ.).

### 1.1 CUTOFF FREQUENCY CONTROL

The cutoff frequency, defined to be the -3dB corner frequency with no boost, is programmable from 1.5 - 8 MHz. It can be set by one of three methods:

1) A resistor is connected between Rx and Ground. The IFO and IFI pins are shorted. This setting is only used for a fixed response design. The design equation for this resistor value is:

   Rx (kΩ) = 10.00 / $f$c (MHz)

   A design example is given in Section 3.

2) A current source input can be fed into the IFI pin. With a current source digital-to-analog converter (DAC), such as the DACF in the SSI 32D4661 Time Base Generator, this design allows a microcontroller to change the filter response dynamically. A resistor from Rx to Ground is needed to establish a bias current on the IFO pin. To achieve the highest accuracy and temperature stability, this bias current on the IFO pin is used to reference the current source DAC. This bias current should be set such that the maximum DAC output current is 0.6 mA at room temperature. The design equations for Rx and the current source value are:

   Rx (kΩ) = 0.75 / IFO (mA) at T = 27°C

   IFI (mA) = 0.075 x $f$c (MHz)

   A design example is given in Section 4.

3) A current sink input can be fed into the IFI pin. With a current sink DAC, this design also allows a microcontroller to change the filter response dynamically. To achieve the highest accuracy and temperature stability, the current sink DAC should be referenced to the proportional to absolute temperature voltage at the Rx pin, nominally at 750 mV. The DAC maximum sinking current should be at least 0.49 mA. A resistor from Rx to Ground is needed. The total current drawn from the Rx pin needs to be 0.6 mA at room temperature. The IFO and IFI pins are shorted. The design equations for Rx and this current sink value are:

   Rx (kΩ) = 0.75 / ( 0.6 - $I_{DAC\ Bias}$ ) (mA)

   IFI (mA) = 0.60 - 0.075 x $f$c (MHz)

   A design example is given in Section 4.

### 1.2 HIGH FREQUENCY BOOST CONTROL

The high frequency boost function is especially desirable for pulse slimming and magnitude equalization applications. This function can be enabled or disabled by a TTL logic input at the FBST pin. With FBST = '1' or open, the amount of high frequency boost, measured at the cutoff frequency, can be programmed from 0 to 9 dB by a voltage input at the VBP pin. External resistors can be used in for a fixed filter response. For a programmable high frequency boost, a voltage DAC, such as the DACS in the SSI 32D4661, can be used to control the VBP pin. This input voltage should be made proportional to the reference voltage at the VR pin for accuracy and temperature stability. The design equation for this control voltage is:

VBP = VR x (10^(FB/20) - 1) / 1.884

where FB is in dB.

Design example is given in Section 3.

With a finite boost, the magnitude response peaks at a frequency slightly higher than the original cutoff frequency. The effective pass band bandwidth is also wider.

### 1.3 OTHER FEATURES OF THE SSI 32F8020A

The SSI 32F8020A is a 7-pole 0.05° equiripple type filter. It features excellent constant group delay. The group delay variation from 0.2 $f$c to 1.75 $f$c is less than ± 2% of the total filter delay. Furthermore, the high frequency boost function does not affect the group delay variation.

In addition to the normal low pass output, the SSI 32F8020A also provides a differentiated low pass output of the input signal. The signal delay is well matched to the normal output.

The SSI 32F8020A provides a temperature compensated reference voltage, VR, and a proportional to absolute temperature voltage, Rx, for the DAC references. The filter cutoff frequency should be referenced to the current at the Rx pin. The high frequency boost control should be referenced to the voltage at the VR pin.

The SSI 32F8020A can be switched into a sleep mode, dissipating less than 2.5 mW, by a TTL low level input at the PWRON pin.

Three package options are available for the SSI 32F8020A: 16-pin DIP, 16-pin SOL and 16-pin SON. The small feature size of the 16-pin SON package offers significant board space saving.

## 2.0 APPLICATIONS

A programmable filter is a versatile component in any signal processing system. Some areas of applications include fixed response filtering, variable data rate processing and adaptive equalization.

For fixed response filtering applications, the SSI 32F8020A offers a simple-to-use solution. The once complex design of cutoff frequency or magnitude equalization is now rendered to simple resistance calculations. The narrow 16-pin small outline package offers significant board space economy.

In variable data rate processing, a programmable filter can be used to optimize bandwidth and signal-to-noise tradeoff. One application is constant density recording for high capacity storage products. As the data rate increases from the inner tracks to the outer tracks, the filter cutoff frequency can be scaled accordingly to maximize signal-to-noise performance. The high frequency boost function provides pulse slimming for accurate pulse detection.

A programmable filter offers a revolutionary approach to adaptive equalization. In signal transmission applications, an equalization filter is used to combat channel distortion. The magnitude of channel distortion is often not known a priori. Adaptive equalization can dynamically shape the equalization function. With an appropriate external adaptive sensing function, the cutoff frequency and the high frequency boost of the SSI 32F8020A can be dynamically programmed through microprocessor control.

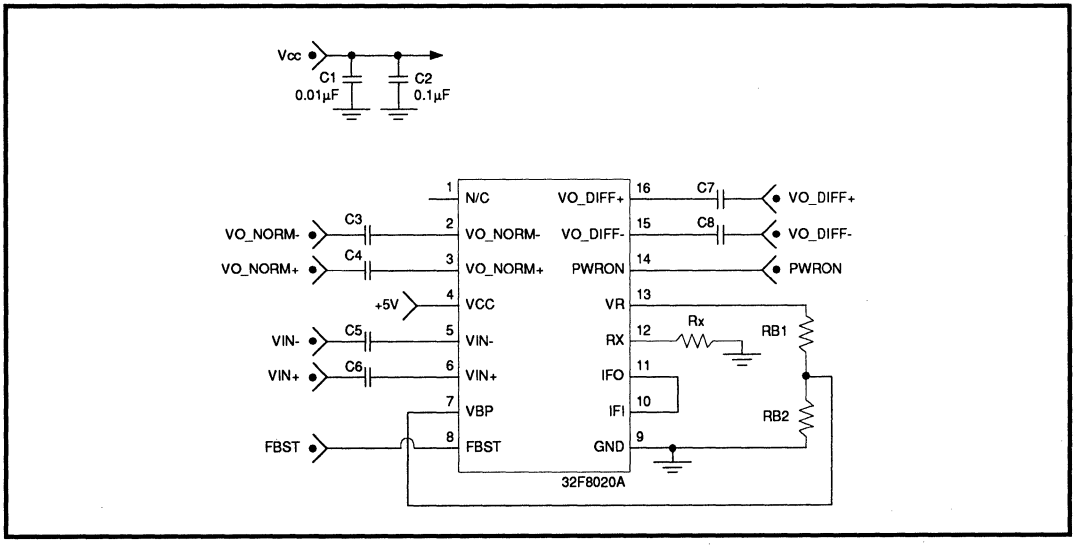


**FIGURE 3: The 32F8020A Setup as a Fixed Response Filter**

## 3.0 FIXED RESPONSE DESIGN PROCEDURE

This section suggests some design guidelines to apply the SSI 32F8020A as a fixed response filter. Figure 3 shows the design schematic. Rx determines the filter's cutoff frequency, defined as the -3 dB frequency with no boost. The ratio of RB1 and RB2 determines the amount of high frequency boost.

Given $fc$, cutoff frequency in MHz, and FB, high frequency boost in dB:

- Rx can be calculated, as given in Section 1.

  Rx (kΩ) = 10.00 / $fc$ (MHz)

  Voltage across Rx is 0.75V, and is proportional to the absolute temperature.

  Rx should be between 1.25 kΩ to 6.67 kΩ, i.e., $fc$ between 1.5 MHz to 8 MHz.

- RB1/RB2 sets FB, and can be determined as follows:

  RB1 / RB2 = 1.884 / (10^( FB / 20 ) - 1) - 1

- Total current drawn out of the VR pin should be limited to 2 mA max. Thus, RB1 and RB2 should be designed accordingly.
- The IFO and IFI pins are shorted together.

## 4.0 PROGRAMMABLE RESPONSE DESIGN PROCEDURE

This section suggests some design guidelines to apply the SSI 32F8020A as a programmable filter. The high frequency boost can be controlled by a voltage DAC driving the VBP pin. The VBP voltage should be between 0 and VR. The cutoff frequency can be controlled by a current DAC. The application setup for using a current source DAC is different from the one using a current sink DAC. Both are presented below.

### 4.1 PROGRAMMABLE FILTER USING A CURRENT SOURCE DAC

Figure 4 shows the setup schematic of the SSI 32F8020 using an external current source DAC to control the filter's cutoff frequency.

Some design guidelines:

- The current source DAC should be referenced to the IFO current. The voltage DAC should reference to VR.
- The reference bias current drawn from VR should be less than 2 mA.
- The IFO current biases the current source DAC for 0.6 mA maximum output at room temperature.

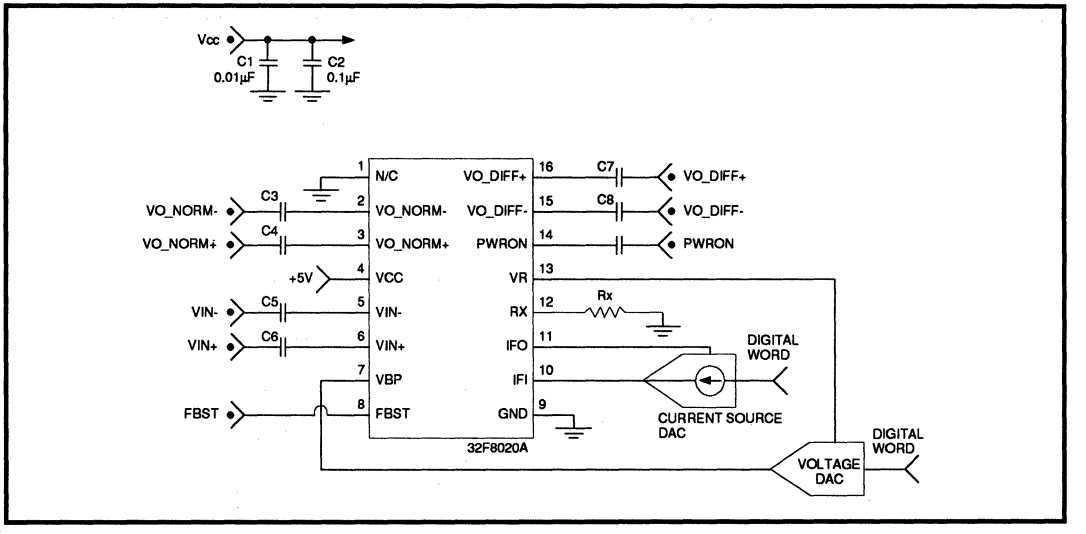


**FIGURE 4: The SSI 32F8020A Setup Schematic Using a Current Source DAC for Cutoff Frequency Control**

### 4.1 PROGRAMMABLE FILTER USING A CURRENT SOURCE DAC (continued)

- The Rx resistor determines the IFO current.

  Rx (kΩ) = 0.75 / $I_{DAC\ Bias}$ (mA)

- The current source output voltage compliance should be between 0 to 2.5V.
- The IFI current and the filter cutoff frequency are related as follows:

  $f_c$ (MHz) = 13.33 x IFI (mA)

  IFI should be between 0.11 mA to 0.6 mA at room temperature.
- The VBP voltage and the high frequency boost are related as follows:

  FB = 20 x log (1.884 x VBP / VR + 1) dB

### 4.2 PROGRAMMABLE FILTER USING CURRENT SINK DAC

Figure 5 shows the setup schematic of the SSI 32F8020 using an external current sink DAC to control the filter's cutoff frequency. The high frequency boost control is the same as in Section 4.1.

Some design guidelines:

- The current sink DAC should reference to the voltage at the Rx pin.

  The voltage DAC should reference to VR.
- The IFO and IFI pins are shorted.
- The total current drawn from VR should be less than 2 mA.

  The total current drawn from the Rx pin should be 0.6 mA.

  Rx (kΩ) = 0.75 / ( 0.6 - $I_{DAC\ Bias}$ ) (mA)
- The current sink DAC output voltage compliance should be between 0 to 2.5V.
- The IFI current and the cutoff frequency are related as follows:

  $f_c$ (MHz) = 8 - 13.33 x IFI (mA)

  IFI should be between 0 mA to 0.49 mA.

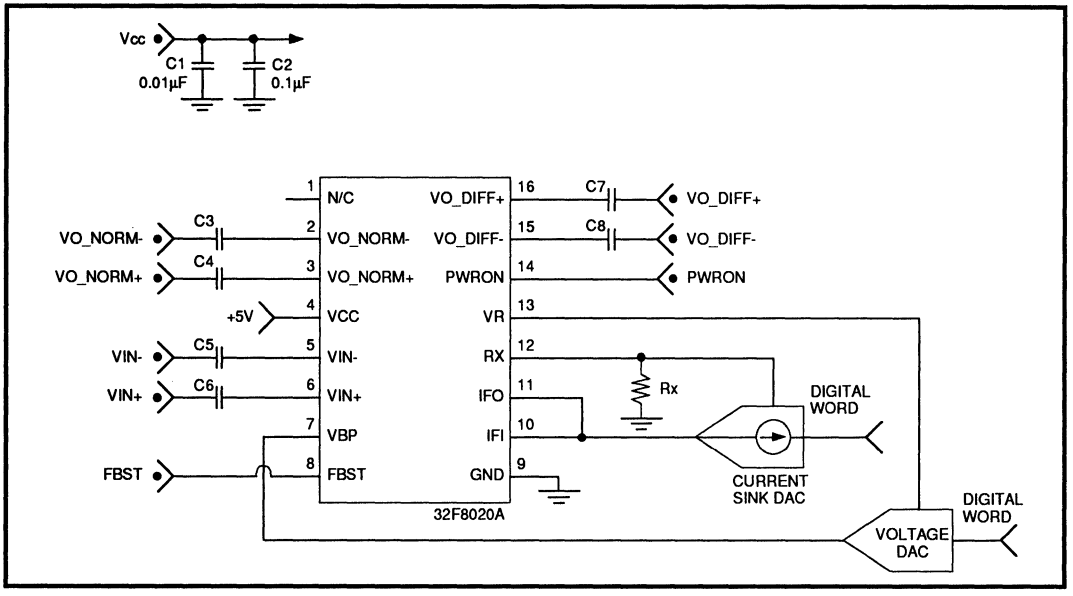


**FIGURE 5: The SSI 32F8020A Setup Schematic Using a Current Sink DAC for Cutoff Frequency Control**

**Notes:**

# SSI 32F8030
## Programmable Electronic Filter

**Application Note**

December 1992

## INTRODUCTION

Analog filtering is a universal requirement in any signal processing system. Filter design is now made easy with the programmable filters from Silicon Systems Inc. Whether the requirement is a fixed filtering characteristic or a programmable response, this family of programmable filters offers distinct advantages of design simplicity, accuracy, versatility and board space savings. Additional features, such as high frequency boost, differentiated outputs, are also available. This application note focuses on the SSI 32F8030, cutoff frequency programmable from 250 kHz - 2.5 MHz.

The objectives of this application note are:

- To present a description of the SSI 32F8030
- To discuss its applications
- To present a typical fixed response design
- To present a programmable response application

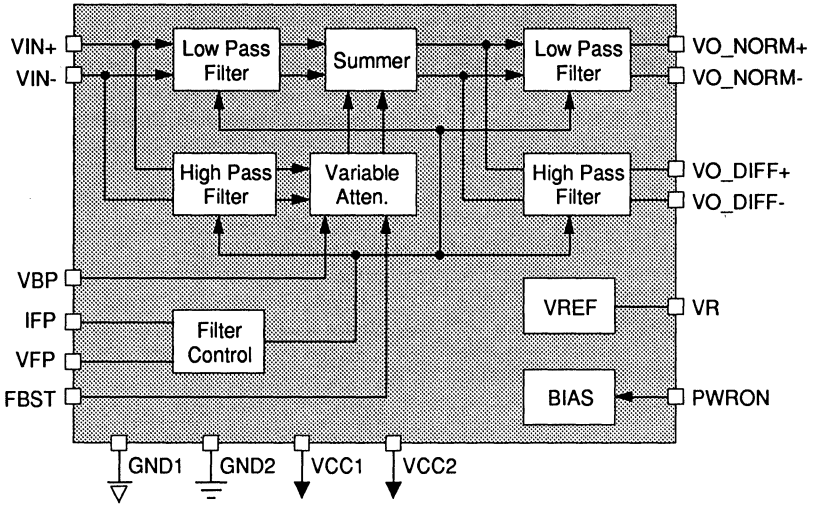


**FIGURE 1: Block Diagram**

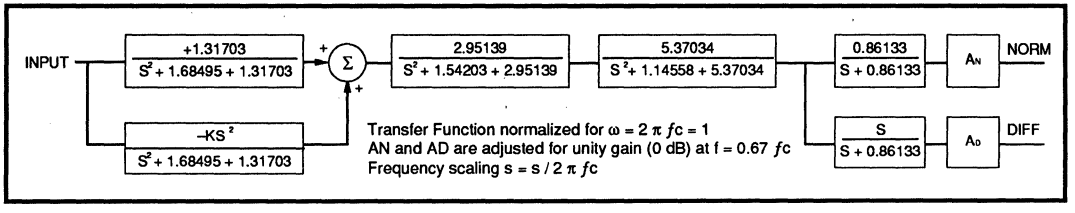


**FIGURE 2: The SSI 32F8030 Transfer Function**



CAUTION: Use handling procedures necessary for a static sensitive component.

# SSI 32F8030
# Programmable Electronic Filter

## 1.0 DESCRIPTION

The SSI 32F8030 is a programmable 7-pole 0.05° Equiripple low pass filter in a silicon bipolar integrated circuit. Figures 1 and 2 show the block diagram and the filter transfer function.

The SSI 32F8030 cutoff frequency and high frequency boost can be independently controlled by two control signals. Two sets of filter outputs are available: normal low pass output and differentiated low pass output. As a 0.05° Equiripple type filter, the filter outputs exhibit constant group delay beyond the pass band. Furthermore, the delays through the normal output and the differentiated output are well matched.

The input and outputs of the SSI 32F8030 are differential signals, requiring external AC coupling capacitors. The given transfer function shows the relationship between the input and the two sets of outputs. The maximum input signal is at least 1.0 Vpp differential, with differential input resistance 4 kΩ typical.

### 1.1 CUTOFF FREQUENCY PROGRAMMING

The cutoff frequency, defined to be the -3 dB corner frequency with no boost, can be programmed between 250 kHz - 2.5 MHz. It can be set by one of three methods:

- A resistor can be inserted between the VR and the VFP pins. This setting is only used for a fixed response design. The IFP pin should be left open. The design equation for this resistor value is:

  Rx (kΩ) = 2.292 / $f$c (MHz)

  A design example is given in Section 4.

- A current source input can be fed into the IFP pin. The VFP pin should be left open. A current source digital-to-analog converter (DAC), such as the DACF in the SSI 32D4661 Time Base Generator, allows a microcontroller to change the filter response dynamically. To achieve the highest accuracy and temperature stability, the current source DAC should be referenced to the temperature compensated reference voltage at the VR pin. The design equation for this current source value is:

  IFP (mA) = 0.320 x $f$c (MHz)

  A design example is given in Section 4.

- A current sink input can be fed into the IFP pin. A 917Ω resistor should be placed across the VR and the VFP pins. With a current sink DAC, this design also allows a microcontroller to change the filter response dynamically. To achieve the highest accuracy and temperature stability, the current sink DAC should be referenced to the temperature compensated reference voltage at the VR pin. The design equation for this current sink value is:

  IFP (mA) = 0.320 x (2.5 - $f$c) (MHz)

  A design example is given in Section 4.

### 1.2 HIGH FREQUENCY BOOST CONTROL

The high frequency boost function is especially desirable for pulse slimming and magnitude equalization applications. This function can be enabled or disabled by a TTL logic input at the FBST pin. With FBST = '1' or open, the amount of high frequency boost measured at the cutoff frequency can be programmed from 0 to 9 dB by a voltage input at the VBP pin. External resistors can be designed in for a fixed filter response. For a programmable high frequency boost, a voltage DAC, such as the DACS in the SSI 32D4661 Time Base Generator, can be used to control the VBP pin. This input voltage should be made proportional to the reference voltage at the VR pin for accuracy and temperature stability. The design equation for this control voltage is:

VBP = VR x (10^(FB/20) - 1) / 1.884 where FB is in dB.

Design example is given in Section 3.

With a finite boost, the magnitude response peaks at a frequency slightly higher than the original cutoff frequency. The effective pass band bandwidth is wider.

### 1.3 OTHER FEATURES OF THE SSI 32F8030

The SSI 32F8030 is a 7-pole 0.05° Equiripple filter. It features excellent constant group delay. The group delay variation from 0.2 $f$c to $f$c is less than 2% of mean group delay. Furthermore, the high frequency boost function does not affect the group delay variation.

In addition to the normal low pass output, the SSI 32F8030 also provides a differentiated low pass output of the input signal. The signal delay is well matched to the normal output.

The SSI 32F8030 provides a temperature compensated reference voltage, VR, for the DAC references. Because the internal filter control circuitry is referenced to VR, the control current for filter cutoff frequency and control voltage for high frequency boost should be referenced to VR.

The SSI 32F8030 can be switched into a sleep mode, dissipating < 5 mW, by a TTL input at PWRON.

Three package options are available for the SSI 32F8030: 16-pin DIP, 16-pin SOL and 16-pin SON. The small feature size of the 16-pin SON package offers significant board space saving.

## 2.0 APPLICATIONS

A programmable filter is a versatile component in any signal processing system. Some areas of applications include fixed response filtering, variable data rate processing and adaptive equalization.

For fixed response filtering applications, the SSI 32F8030 offers a simple-to-use solution. The once complex design of cutoff frequency or magnitude equalization is now rendered to simple resistance calculation. The narrow 16-pin small outline package offers significant board space economy.

In variable data rate processing, a programmable filter can be used to optimize bandwidth and signal-to-noise tradeoff. One application is constant density recording for high capacity storage products. As the data rate increases from the inner tracks to the outer tracks, the filter cutoff frequency can be scaled accordingly to maximize the signal-to-noise performance. The high frequency boost function provides pulse slimming for accurate pulse detection.

Programmable filter offers a revolutionary approach to adaptive equalization. In signal transmission applications, an equalization filter is used to combat channel distortion. The magnitude of channel distortion is often not known a priori. Adaptive equalization can dynamically shape the equalization function. With an appropriate external adaptive sensing function, the cutoff frequency and the high frequency boost of the SSI 32F8030 can be dynamically programmed through a microprocessor control.

## 3.0 FIXED RESPONSE DESIGN PROCEDURE

This section suggests some design guidelines to apply the SSI 32F8030 as a fixed response filter. Figure 3 shows the design schematic. Rx determines the filter's cutoff frequency, defined as the -3 dB frequency with no boost. The ratio of RB1 and RB2 determines the amount of high frequency boost.

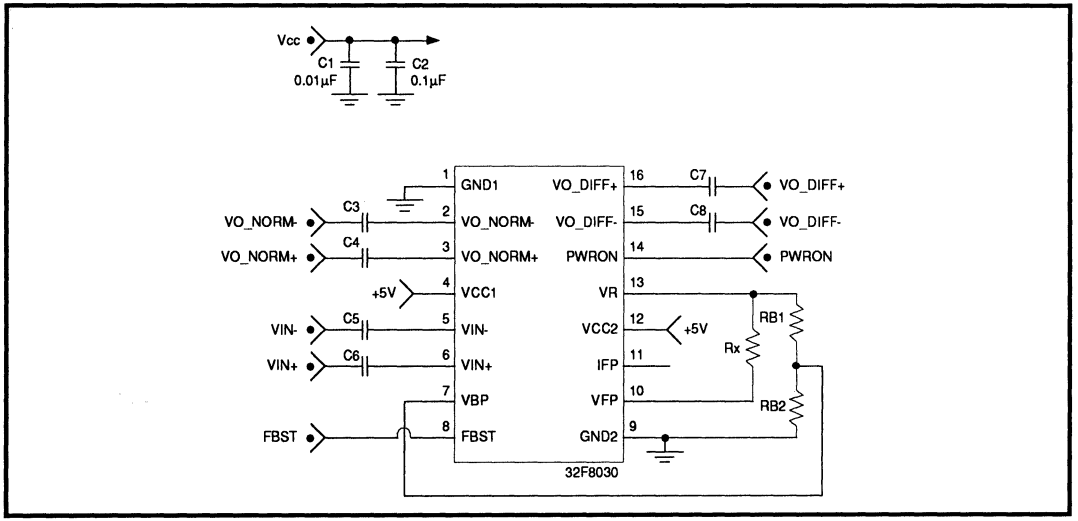


**FIGURE 3: The 32F8030 Setup as a Fixed Response Filter**

## 3.0 FIXED RESPONSE DESIGN PROCEDURE (continued)

Given $fc$, cutoff frequency in MHz, and FB, high frequency boost in dB:

- Rx can be calculated, as given in Section 1.
  Rx (kΩ) = 2.292 / $fc$ (MHz)
  Voltage across Rx is 0.33 VR. The current through Rx is 0.33 (VR / Rx).
  Rx should be between 917Ω to 9.17 kΩ, i.e., $fc$ between 250 kHz to 2.5 MHz.
- RB1/RB2 sets FB, and can be determined as follows:
  RB1 / RB2 = 1.884 / (10^( FB / 20 ) - 1) - 1
- Total current drawn out of the VR pin should be limited to 2 mA max. Thus, RB1 and RB2 should be designed accordingly.
- The IFP pin should be left open.

## 4.0 PROGRAMMABLE RESPONSE DESIGN PROCEDURE

This section suggests some design guidelines to apply the SSI 32F8030 as a programmable filter. The high frequency boost can be controlled by a voltage DAC driving the VBP pin. The VBP voltage should be between 0 and VR. The cutoff frequency can be controlled by a current DAC. The application setup for using a current source DAC is different from the one using a current sink DAC. Both are presented below.

### 4.1 PROGRAMMABLE FILTER USING A CURRENT SOURCE DAC

Figure 4 shows the setup schematic of the SSI 32F8030 using an external current source DAC to control the filter's cutoff frequency.

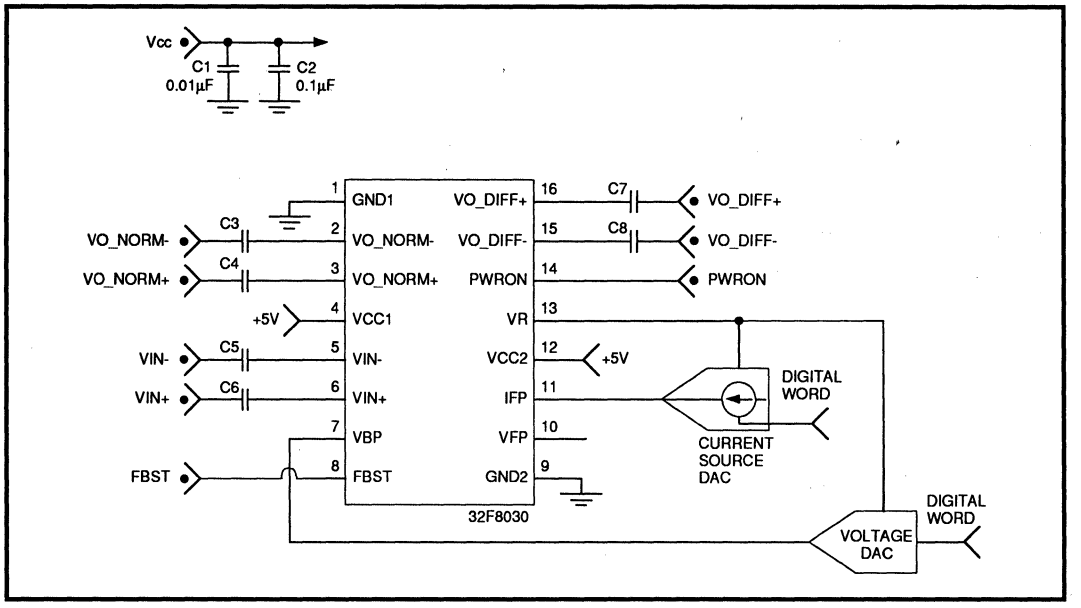


**FIGURE 4: The SSI 32F8030 Setup Schematic Using a Current Source DAC for Cutoff Frequency Control**

Design guidelines for the SSI 32F8030:

- The VFP pin should be left open.
- Both the current source DAC and the voltage DAC should reference to VR for accuracy and temperature stability.
- The reference bias current drawn from VR should be less than 2 mA.
- The current source output voltage compliance should be between 1.3V to 2.1 V.
- The IFP current and the filter cutoff frequency are related as follows:

  $fc$ (MHz) = 3.125 x IFP (mA)

  IFP should be between 0.08 mA to 0.8 mA.
- The VBP voltage and the high frequency boost are related as follows:

  FB = 20 x log (1.884 x VBP / VR + 1) dB

### 4.2 PROGRAMMABLE FILTER USING CURRENT SINK DAC

Figure 5 shows the setup schematic of the SSI 32F8030 using an external current sink DAC to control the filter's cutoff frequency. The high frequency boost control is the same as in Section 4.1.

Some design guidelines:

- Rx should be set to 917Ω between VR and VFP.
- Both the current source DAC and the voltage DAC should reference to VR for accuracy and temperature stability.
- The total current drawn from VR should be less than 2 mA. This includes the 0.8 mA through Rx. Thus, the current sink DAC and the voltage DAC reference should not draw more than 1.2 mA.
- The current sink DAC output voltage compliance should be between 0.85V to 1.6V.
- The IFP current and the cutoff frequency are related as follows:

  $fc$ (MHz) = 2.5 - 3.125 x IFP (mA)

  IFP should be between 0 mA to 0.72 mA.

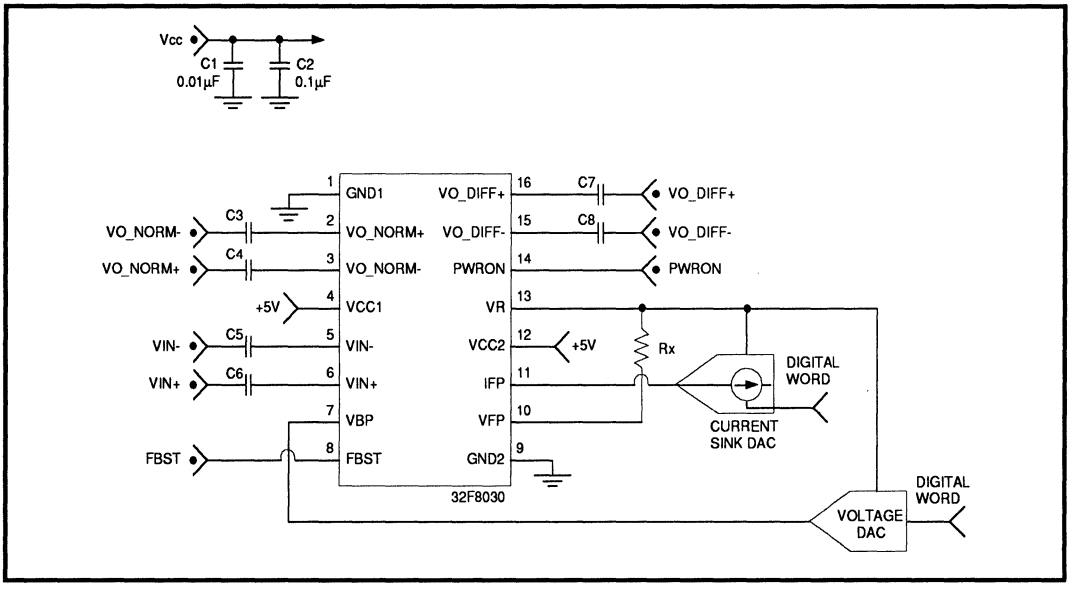


**FIGURE 5: The SSI 32F8030 Setup Schematic Using a Current Sink DAC for Cutoff Frequency Control**

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**Notes:**

December 1992

## SERVO DESIGN EXAMPLE

The application of the SSI 32H6220 dedicated servo controller, SSI 32H569/32H6230 H-bridge predriver, and SSI 32H6210 servo demodulator chips require both discrete component determination and microprocessor programmed register values. This section provides as a design example, a systematic method of determining both the discrete components and programmable values required in implementing a fully functional track and seek head positioning servo. This example makes use of an available Silicon Systems' program named SERVO CALC which runs on the PC/XT or PC/AT compatible personal computer. The program provides an interactive enviroment for entering target specifications, systematically proceeding through the design, and automating the calculation of components and programmable values. The program provides various tools for system performance review such as velocity profile plots, open and closed loop Bode plots, step response plot, mechanical resonances and notch filter effects.

## SPECIFY SEEK PERFORMANCE REQUIREMENTS

Specifying the average seek time, total number of tracks for a full length seek, and profile characteristics will provide the basis for determining a precise head velocity profile. Profile characteristics specify the relationship between acceleration and deceleration under different conditions. The ratio of deceleration time plus settling time all divided by the acceleration time provides the profile characteristic "R." The number of tracks traveled in "triangular mode" divided by the total number of tracks for a full length seek provides the profile characteristic "BETA." These two profile characteristics may be used along with a modified square root law to determine a velocity profile which will result in satisfying the specified average seek time.

As an example, specify as design goals:

Linear actuator
1400 TPI for a G2 of 55,860 Tracks/Meter
1000 total cylinders
Average access time of 15 ms
30 gram actuator mass
R = 1.2 and BETA = 0.4

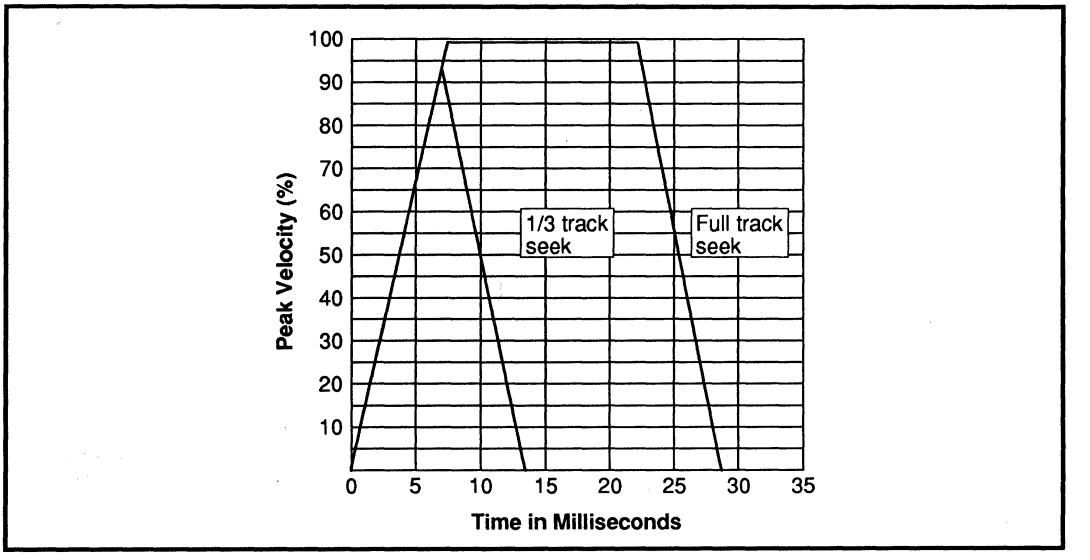


**FIGURE 1: Track Seek Profile**

### REVIEW VELOCITY PROFILES

The deceleration profile may be reviewed and adjusted by modifying the square root law which relates profile head velocity to the number of tracks left to travel. Step-wise increasing the exponent of tracks to go from 1/2 (square root starting point) will "soften" the deceleration approach curve. As the curve softens, the settling time available decreases. The "R" value may be adjusted to match a suitable deceleration curve with the required settling time.

From the profile chosen, the following parameters may be determined for our example design:

Head acceleration of 6,175,115 tracks/sec$^2$

Peak head velocity of 49,699.5 tracks/sec

200 deceleration tracks required

8.05 ms of acceleration, 12.08 ms coasting, and 9.66ms decelerating full seek

Full seek time 29.8 ms

Both the average and full length seek profiles are shown in Figure 1.

### SPECIFY MOTOR AND LOAD PARAMETERS

The motor and load parameters must be estimated and specified so that the power required to meet the velocity profile chosen may be computed and compared against design goals. G1 is preamplifier gain and is not dependent upon motor or load parameters. G1 is fixed at 6 VOLTS/TRACK when using the SSI 32H6210. The motor resistance will introduce both a power loss and a voltage drop which must be considered. The two motor systems, namely linear and rotary, require different units of specification.

#### Linear Motor Specifications

G2 transport constant in Tracks/Meter

J mass in KG (kilograms)

Km motor constant in N/A (newton/amps)

#### Rotary Motor Specifications

G2 transport constant in Tracks/Rad

J inertia in KG m$^2$ (kilograms meter squared)

Km motor constant in (N • m/A)

Optionally, Km may be computed from the head velocity profile based on a specified maximum motor current IPEAK. The two specifications of IPEAK and Km are interrelated.

For our example,

IPEAK is 1 Amp and Km is calculated

Rm = 3.8Ω

Rs = 0.2Ω

### REVIEW MOTOR VOLTAGE, POWER AND Km

From the motor and load specifications, the required peak current needed to satisfy the chosen head velocity profile may be calculated. Using the transport constant G2, the back EMF of the motor may be calculated at peak head velocity and added to the the voltage drop across the motor resistance Rm and sense resistor Rs. The total voltage required by the motor may be compared to the available driver voltage. Peak motor power may be computed and compared to design goals. If Km was calculated from a specification of IPEAK, the resulting value of Km may be compared against that actually attainable in the motor design. Adjustment of Km and IPEAK may be made to both satisfy the average seek time specification and general design goals.

For this example:

Km was calculated to be 3.316 N/A

Peak drive voltage required is 6.95V including the voltage across Rs

Peak coil input power is 6.75 Watt

Coil dissipation 3.8 Watt

### SPECIFY POWER AMPLIFIER COMPONENTS

The power amplifier is shared by both the track following and seek servo control loops. The determination of DC gain for the power amplifier for seek will also determine some components shared with the track following servo. Referring to the example schematic of the SSI 32H6210/6220/6230, RS, RF and the sum resistance of RINV1 and RINV2 (RINV) may be determined. Choosing RF to be an initial nominal value such as 10,000Ω and choosing RS as some small resistance such as 0.2Ω provides good starting points.

The DC power amplifier gain for the seek servo is calculated from the peak current required to satisfy the peak velociyy of the velocity profile and the full scale target DAC output voltage. A motor current limit may be implemented when using the SSI 32H6230 by connecting the CLAMP pin to ERR- through the RINV1 and RINV2 network as shown on the schematic. The limit voltage is programmable by setting the voltage at the 6230 VLIM pin. It is necessary to choose the limit current higher with tolerance margin above that current required to meet the maximum head velocity from the velocity profile.

In the example,

RINV total should be 5062.5Ω

RF is specified as 10,000Ω

## CHOOSE DIFFERENTIATOR AND VELOCITY LOOP GAINS

The differentiator within the SSI 32H568 or 32H6220 provides a programmable corner frequency determined by servo frame rate and the two bit register ND. Having determined the maximum head velocity from the velocity profile and knowing the transport constant and servo frame rate, the maximum output voltage from the differentiator may be calculated.

The output of the differentiator is amplified by the velocity amplifier A3 and the programmable gain stage set by NVG. The velocity loop gain from the output of the differentiator to the feed back summing junction of the target DAC must be set so that the peak differentiator output voltage will result in zero VE voltage (relative to VREF) when the target DAC is at its full range of 255. Choosing a nominal NVG setting of 10 and selecting an ND which does not exceed the amplitude limit of the differentiator itself, will result in the calculation of the necessary gain in A3. The seek velocity feedback may be fine tuned by adjusting the gain of NVG as indicated in drive self-calibration.

For the example, the programmable registers are:

NVG is 10 decimal

ND will be 2 for a frame rate of 250 kHz

Gain of A3 will be 1.96 so that (RV4/RV3) = 1.96; If RV4 = 19.6K, then RV3 = 10K

RV1 and CV1 will not be used in this example

## GENERATE TARGET PROFILES

The seek servo velocity loop is closed within the SSI 32H6220. The implementation of the velocity profile is commanded by the supporting microprocessor. The microprocessor commands target velocities by writing to the target DAC. The necessary DAC values may be derived from the velocity profile. The acceleration DAC value is determined from the peak head velocity in the velocity profile. The microprocessor writes the acceleration target velocity to the target DAC and monitors track crossings determining when to begin deceleration. Once the head has moved past the deceleration corner, the microprocessor will write the deceleration target velocities to the target DAC usually track by track thereby following the head velocity down to the transition point into track following. The number of table entries making up the deceleration table can be found from the profile data discussed in the earlier section, Review Velocity Profiles.

A fill table may be generated corresponding to the target velocity table. The fill table is usually only a few entries long. The fill table values are computed from the position error voltage available at FP1 and the step in target DAC voltage for the last few deceleration velocity targets. The fill value programs the gain of the fill amplifier which subtracts from the velocity error a portion of the position error signal. This subtraction of position error from the velocity error has the effect of smoothing the velocity error voltage at VE when the head is moving slowly and tends to insure that the head will move towards the center of the target track prior to switching on track following.

The 20 element fill value table resulting for the example is shown below in Table 1. "t" is the target track.

| Target Track Lineup | |
|---|---|
| t-0: 12 | t-10: 2 |
| t-1: 5 | t-11: 1 |
| t-2: 4 | t-12: 2 |
| t-3: 3 | t-13: 1 |
| t-4: 3 | t-14: 2 |
| t-5: 3 | t-15: 1 |
| t-6: 3 | t-16: 1 |
| t-7: 2 | t-17: 1 |
| t-8: 2 | t-18: 2 |
| t-9: 2 | t-19: 1 |

**TABLE 1**

The velocity target DAC values for the example are listed below in Table 2, ordered as the number of tracks remaining to go, ie: "t-n":

| t-0 | t-20 | t-40 | t-60 | t-80 | t-100 | t-120 | t-140 | t-160 | t-180 |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 81 | 114 | 140 | 161 | 180 | 198 | 213 | 229 | 243 |
| 18 | 83 | 115 | 141 | 162 | 181 | 198 | 214 | 229 | 243 |
| 25 | 85 | 117 | 142 | 163 | 182 | 199 | 215 | 230 | 244 |
| 31 | 86 | 118 | 143 | 164 | 183 | 200 | 216 | 231 | 245 |
| 36 | 88 | 120 | 144 | 165 | 184 | 201 | 217 | 232 | 245 |
| 40 | 90 | 121 | 145 | 166 | 185 | 202 | 218 | 232 | 246 |
| 44 | 92 | 122 | 146 | 167 | 186 | 202 | 219 | 233 | 247 |
| 48 | 94 | 124 | 148 | 168 | 187 | 203 | 219 | 234 | 247 |
| 51 | 95 | 125 | 149 | 169 | 187 | 204 | 220 | 234 | 248 |
| 54 | 97 | 126 | 150 | 170 | 188 | 205 | 221 | 235 | 249 |
| 57 | 99 | 127 | 151 | 171 | 189 | 206 | 222 | 236 | 249 |
| 60 | 100 | 129 | 152 | 172 | 190 | 206 | 222 | 236 | 250 |
| 62 | 102 | 130 | 153 | 173 | 191 | 207 | 223 | 237 | 250 |
| 65 | 104 | 131 | 154 | 174 | 192 | 208 | 224 | 238 | 251 |
| 67 | 105 | 132 | 155 | 175 | 193 | 209 | 224 | 239 | 252 |
| 70 | 107 | 134 | 156 | 176 | 193 | 209 | 225 | 239 | 252 |
| 72 | 108 | 135 | 157 | 177 | 194 | 210 | 226 | 240 | 253 |
| 74 | 110 | 136 | 158 | 178 | 195 | 211 | 227 | 241 | 254 |
| 76 | 111 | 137 | 159 | 178 | 196 | 212 | 227 | 241 | 254 |
| 79 | 113 | 138 | 160 | 179 | 197 | 213 | 228 | 242 | 255 |

**TABLE 2**

### POWER AMPLIFIER COMPENSATION

Components RL2 and CL3 set the bandwidth of the power amplifier. Specifying motor inductance Lm and power amplifier bandwidth BW while having determined RF, Rm, and Rs from seek requirements provides the means for calculating CL3 and RL2.

For the example,

Power amplifier bandwidth is specified as 10 kHz

Lm is specified as 1 mH

CL3 is calculated to be 0.005 μF

RL2 is calcuated to be 47 kΩ

### TRACK FOLLOWING GAIN

Both the track following and seek loops share many of the power amplifier gain setting components. Having determined RINV, RF and Rs from velocity profile requirements, the track following power amplifier gain KP is determined entirely by RINP. The track following power amplifer gain KP is interactively set with the position loop filter gain KF. An initial KP may be chosen as 1 AMP/VOLT and the value of KF may be adjusted as needed to stabilize the track following loop. The value of RINP may be computed from RF, Rs, and KP.

In the example,

Specify KP = 1 Amp/Volt

Calculate RINP = 12.5 kΩ

### POSITION LOOP FILTER

The implemented filter will take the form of a LAG-LEAD-LEAD-LAG in ascending frequency breakpoints. Due to the double integration in the motor-load mechanics going from acceleration to position, there is an initial 180 degree position phase lag which must be compensated to prevent instability and oscillation. Phase lag introduced by a pole will add additional phase lag exceeding 180 degrees while phase lead introduced by a zero will reduce phase lag. The objective of the position loop filter is to ensure that there

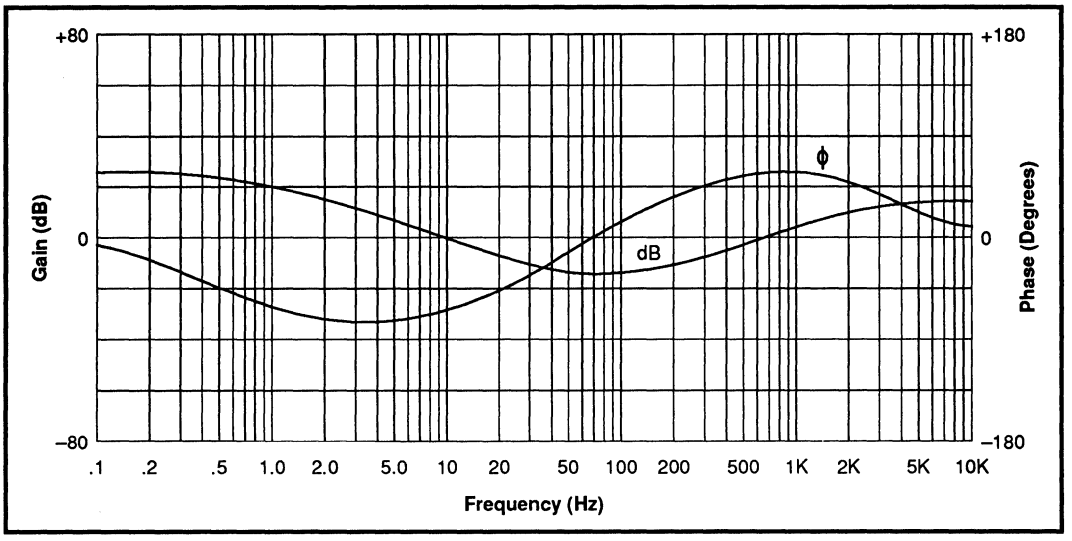


**FIGURE 2: Position Loop Filter Bode Plot**

is phase margin at the system unity gain crossover frequency while at the same time providing stiffness and long term tracking error cancelation.

The initial position loop filter gain KF may be estimated through a specification for DC stiffness. Specifying a stiffness in units of force per track and knowing G1, Km, and KP will provide a way to solve for KF.

DC stiffness per track is calcuated as:

STIFFNESS = G1 KF KP Km

Specifying 100 N/TRACK stiffness, KF is determined in the example to be 5.

The lowest frequency LAG time constant is referred to as bT2 and is the product CP2(RP3+RP4). This low frequency LAG serves effectively as an integrator with limited DC gain intended to minimize long term tracking error and allowing an increased DC gain improving stiffness which otherwise would not be possible due to mechanical higher frequency resonances. Time constant bT2 generally should be made as large as practically possible. Choosing a value for CP2 such as .47 μF and a pole frequency between 0.1 and 1 HZ will provide a good starting point.

The track following servo is stabilized by providing phase margin at the unity gain crossover frequency. Phase margin is obtained through the use of the two LEAD networks. The first lead breakpoint compensates for the integrator phase lag and the second lead breakpoint provides the required phase margin. Time constant T2 made up of RP3 and CP2 provides the phase lead needed to bring the phase back towards 180 degrees of phase lag. Lead time constant aT1 provides additional phase lead by reducing the phase lag less than 180 degrees at the unity gain crossover frequency. Choosing the time constant aT1 such that its break point frequency is equal to the unity gain crossover bandwidth for the system will provide approximately 45 degrees of phase margin. Time constant T2 needs to be chosen to be at least five times aT1 thereby minimizing the interactive effects of the two leads together. T2 should not be chosen so low in frequency as to cancel out the effects of the integrator lag and the low frequency gain enhancement.

Finally, the high frequency pole T1 determined by RP1 and CP1 provides a high frequency gain limit. The breakpoint frequency associated with the time constant T1 should be placed several times higher than the breakpoint frequency set by aT1. Mechanical resonances may require further adjustment of the T1 breakpoint frequency. Some systems may require additional

**POSITION LOOP FILTER** (Continued)

notch filters to minimize high frequency mechanical effects.

Having chosen the break point frequencies, the position filter components may all be computed having specified CP2 and KF.

For the example, the break points were initially specified as:

bT2 frequency = 0.6 Hz

T2 frequency = 60 Hz

aT1 frequency = 600 Hz (target system unity gain bandwidth)

T1 frequency = 2000 Hz

**TRACK FOLLOWING SYSTEM RESPONSE REVIEW**

Bode plots of the open loop response for the LAG-LEAD-LEAD-LAG position loop filter are useful in evaluating the break point frequencies chosen. More useful is the system open loop Bode plot which provides the necessary information needed to properly adjust KF to meet the desired system unity gain bandwidth. Adjusting KF will move the overall response vertically such that unity gain occurs at the desired system bandwidth frequency. The amount of vertical movement indicates how KF should change relative to its intial current value. The phase margin peak may be adjusted horizontally by changing the time constants aT1 and T2. Moving the peak phase lead to correspond to the unity gain frequency is desireable. The system unity bandwidth indicates the stability of the servo system by the amount of phase margin at the unity gain crossover point. Figure 2 shows the open loop position filter Bode plot. Notice the peaking of phase near the target system unity bandwidth frequency of 600 Hz. Figure 3 shows the overall open loop system Bode plot.

After review and adjustment, the final components were standardized as:

RP1 = 8,250Ω

RP2 = 91 kΩ

RP3 = 13 kΩ

RP4 = 680 kΩ

CP1 = 0.0075 µF

CP2 = 0.47 µF

Which resulted in actual break points of:

bT2 frequency = 0.49 Hz

T2 frequency = 26 Hz

aT1 frequency = 213 Hz

T1 frequency = 2572 Hz

And KF = 7.47 for a DC stiffness of 148 N/Track. The resulting phase margin is 51.60 degrees at 630 Hz. The gain margin is 25.2 dB at 4800 Hz.

The closed loop system step response may be obtained and examined to evaluate the overshoot and settling time. The integrator time constant bT2 will tend to control the settling time or "tail." The time constants aT1 and T2 effect the amount of ringing and overshoot. Figure 4 shows the response of the system to a position step.

For the example,

Overshoot is 30%

First zero crossing at 0.4 ms

Settling within 2 ms

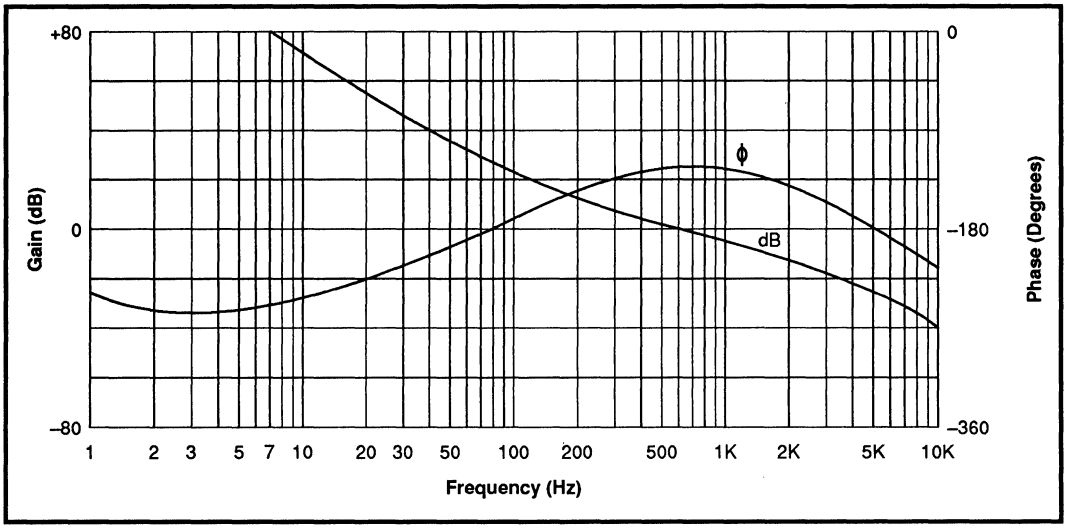


FIGURE 3: Overall Position Open Loop Bode Plot

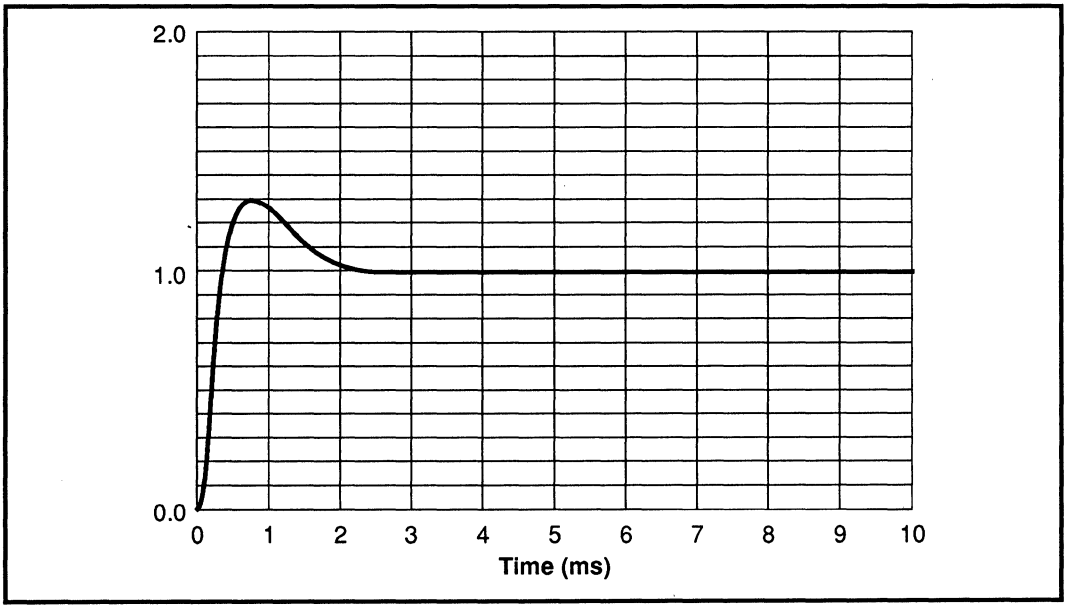


FIGURE 4: Position Closed Loop Step Response

## SERVO CALC SOFTWARE

### HEAD POSITIONING APPLICATIONS TOOL

### DESCRIPTION

This software is an aid to disk drive head position servo design using SSI 32H 6210, 32H6220, 32H569, 32H6230 servo controller and servo motor driver chips. It uses block diagram algebra and transfer function analytical techniques to arrive at first order approximations for the servo design values and parameters. This software offers visual representations of block diagrams, transfer functions, schematics, as well as Bode, seek profile and step response plots. It includes design aids for the design of velocity profiles and tables for evaluation of gain and characteristics settings. It uses simple menus to choose the design screens for power amplifier and position loop filter design and design modules for seek profile/loop parameters and their components. It also has a user definable polynomial transfer function for Bode plot and step response evaluations. The effects of parameter and component changes are specially flagged and quickly displayed.

### SERVO CALC PROGRAM FEATURES

- Mathematical modeling
- Polynomial transfer functions displayed/described
- Block diagrams displayed
- Individual design screens displaying design progress
- Stability analysis
- Bode and step response plots
- Mechanical resonance and notch filter effects
- Motor current and power dissipation analysis
- Velocity profile and fill table generation
- Develops design for power amplifier components
- Tabulates and displays design choices in velocity loop
- User-controllable plot and print settings

### MINIMUM SYSTEM REQUIREMENTS TO RUN SERVO CALC

An IBM PC/XT/AT or compatible computer with at least 512 Kb of RAM, EGA or EGA-compatible video adapter and monitor, one 5 1/4 inch floppy disk drive. A dot matrix printer for plots and screen printings is optional. A math co-processor and a hard disk is recommended but not required.

For your copy of the SERVO CALC software and other helpful servo tools, please contact your local representative or Silicon Systems, Inc. at (714) 573-6000.



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# Snubbing Network Design for Spindle Motors

## Silicon Systems 32M595, 32H4631

## Application Note

The use of an RC snubber network placed across each winding of a three-phase brushless motor may be beneficial in reducing the switching EMF and acoustic noise of the motor. Further, use of the snubber is generally required when applying the SSI 32M595 or 32H4631 in systems using 12 volt unipolar (HALF-WAVE) drive modes. Use of snubbers in the unipolar drive mode reduces the amplitude of the switching transients which can be as large as 20 volts. When the individual motor phase and snubber circuit is considered as a simple L-R-C circuit, the following design approach may be taken to compute the necessary snubber R and C values.

1. **Determine the necessary time constant for the network.**
   The motor circuit and the snubbing network to be added will be designed so as to create a second order exponentially decaying step response. The remaining amplitude should be a small value at the time the next commutation zero crossing is expected to occur. Since the zero crossing occurs roughly 1/2 of a commutation cell period after commutation occurs (due to the chip intentional commutation delay), one can calculate the allowable time for the decay and specify the snubbing network by following through this example:
   a. Peak amplitude of transient is 12 volts (12 volt UNIPOLAR)
   b. Die down to 1/1000 of initial transient in 1/2 commutation cell period. This will result in 12 mV remaining. The remaining transient voltage can alter the commutation angle. In a typical unipolar application with a $K_t$ (torque constant) of 3.5 oz-in/Amp the magnitude of the BEMF signal used for commutation when at speed (assumes 3600 RPM) is 9.3 volts peak. The amount of commutation shift, or jitter due to residual transient voltage in degrees of electrical angle is:

      $$Angle_{shift} = \pm [SIN^{-1} (.012/9.3)] = .074°$$

      Which is, of course, negligible.
   c. Decay period (1/2 the commutation cell time) is 694 µsec for a 4-pole motor at 3600 RPM.
   d. Motor inductance is 3.5 mH, resistance is 7Ω, and torque constant, $K_t$, is 3.5 oz-in/Amp. Knowing that the transient dies down exponentially as:

      $$v = e^{(-t/\tau)}$$

      Where $\tau$ denotes the time constant of the motor and snubber circuit and t is the time allowed for this decay to occur. We can solve for the necessary $-(t/\tau)$ by:

      $$Log_e(1/1000) = -6.908$$

      and since $t/\tau = 6.908$, and t=694 µsec, then $\tau$ = 694e-6 ÷ 6.908, which equals 100.5 µsec.

2. **Computing the required snubbing capacitor.**
   The motor and snubber circuit equivalent circuit is shown in Figure 1.
   Solving for the transient response at

   $$v = \frac{RCS + 1}{L_m C S^2 + (R_m + R)C S + 1}$$

   Where: $L_m C = 1/w_\eta^2$, and $w_\eta$ is the natural frequency in radians, and $(R_m + R)C = 2\zeta/w_\eta$, and $\zeta$ is the damping constant of the second order characteristic equation which defines the time constant,

   $$\tau = 1/(\zeta w_\eta).$$

   When critical damping is desired, as it is now, $\tau$ reduces to $1/w_\eta$.
   In our example $\tau$ is 100.5e-6 sec, and in the calculation $L_m \times C = 1/w_\eta^2$, therefore to calculate C when $L_m$ is known:

   $$C = \tau^2 / L_m .$$

   In the example $L_m$ is 3.5 mH, therefore $C = (100.5e-6)^2 / 3.5e-3$

   $$C = 2.89\ \mu Fd$$

# Snubbing Network Design for Spindle Motors

## Silicon Systems 32M595, 32H4631

3. **Computing the resistor.**
   The total resistance in the circuit determines the damping factor. The characteristic equation has $(R_m + R) \times C$ equaling 2 times the damping factor divided by the natural frequency, $w_\eta$. The total resistance for a damping factor of 1 (critical damping is desired) is: $R_{(total)} = (2 \times \tau)/C$

   $$R_{(total)} = (2 \times 100.5e\text{-}6)/2.89e\text{-}6$$

   $$R_{(total)} = 69.7\Omega.$$

   To find R (the snubbing resistor) the motor resistance is subtracted from the total resistance just calculated:

   $69.7 - R_m$( which is $7\Omega$), therefore:

   $$R = 62.7\Omega.$$

**Summary**

This approach can be iterated to result in a more common snubbing capacitor value by changing the target time constant. Too much snubbing will cause a shift in the zero crossing time resulting in poorer motor performance. Further, the snubber may result in some noticeable power and torque loss, but using this approach generally will yield good working values.

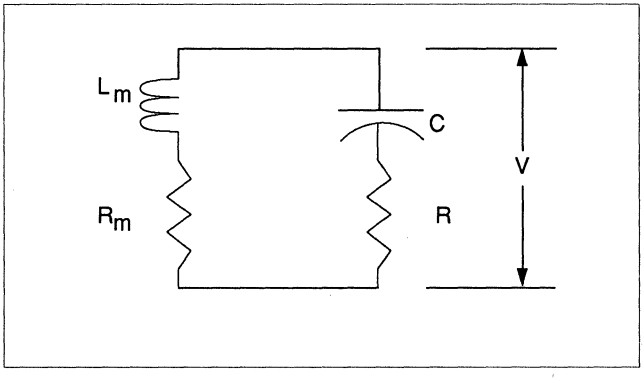



Figure 1: Motor and Snubber Circuit Equivalent Circuit

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 573-6000, FAX (714) 573-6914

# Setting Speed Control Loop Compensation Gains for SSI 32M595, 32H4631, 32M7010

## Application Note

The speed control compensation is controlled by two gain terms $K_p$ and $K_i$, the proportional and integral gains. These gains are set by the selection of two resistors. This document presents a method of determining those two gains and then the resistor values. The derivation of the gains will be shown by using the linearized block diagram and the transfer function obtained from that simplification. The amount of error that this will introduce due to the speed control being a sampled system is within tolerable limits at most bandwidths necessary for disk drive spindle applications. Of course the presentation of this method does not try to indicate this is the only way these gains may be determined, or even the best way. It is one method only and the user may elect another method that will best suit his needs.

The simplified, linearized block diagram is seen in Figure 1; the derivation of the open loop transfer function is shown.

This is where:

$K_A$ is the transconductance gain of the driver circuit which is a function of $R_{sense}$ ( see the respective part data sheet).

$K_T$ is the motor torque constant. Use units that are compatible with J such as oz-in/Amp and oz-in-sec$^2$, or newton-meters/Amp & Kilogram-meters$^2$.

J is the load rotating inertia. Use units that are compatible with $K_T$.

S is the Laplace operator.

$K_p$ is the proportional gain calculated.

$K_i$ is the integral gain calculated.

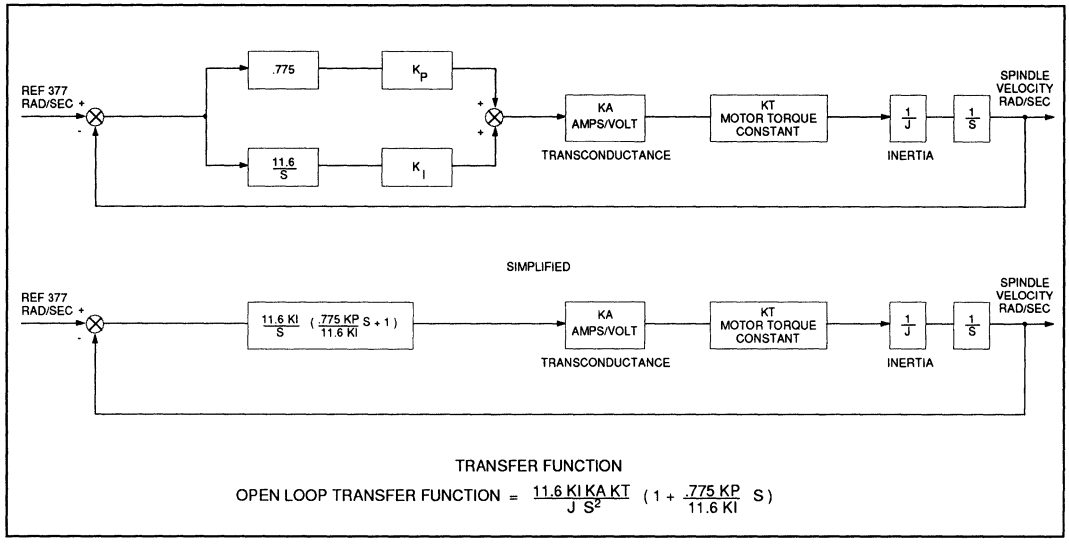



**FIGURE 1: Motor Speed Control Linearized Block Diagram**

# Setting Speed Control Loop Compensation Gains

## For SSI 32M595, 32H4631, 32M7010

From the open loop transfer function the loop gain is:

$$LG = \frac{11.6\ K_i K_A K_T}{J\ S^2}\ (1 + \frac{.775\ K_P}{11.6\ K_i}\ S)$$

This can be expanded to:

$$LG = \frac{11.6\ K_i K_A K_T}{J\ S^2} + \frac{K_A K_T\ .775\ K_P}{J\ S}$$

The problem is to select values for $K_p$ and $K_i$ that will allow the loop gain to come to 1.0 (0 dB) at the desired bandwidth frequency; and with a phase margin of the desired amount considering stability and performance (usually 45 to 60 degrees).

Evaluate the loop gain at the bandwidth frequency and calculate the unknown gains.

Where: LG = 1.0 at an angle of -135 degrees
(45 degrees phase margin)
S = jw
BW = desired bandwidth frequency in Hertz
w = 2 πBW

$$1 \angle -135° = \frac{11.6\ K_i K_A K_T}{J\ j^2\ w^2} + \frac{K_A K_T\ .775\ K_P}{J\ jw}$$

Separate both sides of the equation into their real and imaginary parts:

$$-.707, -j\ .707 = \frac{-11.6\ K_i K_A K_T}{J\ w^2},\ -j\ \frac{K_A K_T\ .775\ K_P}{J\ w}$$

The real part can be solved directly for $K_i$ and the imaginary part for $K_p$:

$$-.707 = \frac{-11.6\ K_i K_A K_T}{J\ (2\pi BW)^2} \text{ solving: } K_i = \frac{.707\ J\ (2\pi BW)^2}{11.6\ K_A K_T}$$

$$-j\ .707 = -j\ \frac{K_A K_T\ .775\ K_P}{J\ (2\pi BW)} \text{ solving: } K_P = \frac{.707\ J\ (2\pi BW)}{.775\ K_A K_T}$$

Let some values be assumed as an example and solve for the gains:
Let:

$K_A$ = 1.0 Amp/volt
$K_T$ = 3.5 oz-in/Amp
J = .0098 oz-in-sec$^2$
BW = 1 Hz.

$K_i = (.707 \times .0098 \times (2\pi 1)^2)/(11.6 \times 1.0 \times 3.5) = .00674$

$K_p = (.707 \times .0098 \times (2\pi 1))/(.775 \times 1.0 \times 3.5) = .016$

These gains and assumed values can be put into the loop gain equation and as a design verification a bode plot can be made with SERVOCALC®, see Figure 2.

$$LG = \frac{11.6\ (.00674)\ (1.0)\ (3.5)}{(.0098)\ S^2}\ (1 + \frac{.775\ (.016)}{11.6\ (.00674)}\ S)$$

In polynomial form:

$$LG(s) = \frac{4.429\ S + 27.923}{S^2}$$

This polynomial is entered into the USER POLYNOMIAL module of SERVOCALC® and a Bode plot made.

As can be seen in the figure the 0 dB crossover is at 1 Hz and the phase margin is 45°.

Now that the gains have been calculated they need to be set in to the circuit with resistors $R_p$ and $R_i$ as in the data sheet. Let the summing resistor be $R_o$ from the $V_{in}$ pin to ground as on the data sheet; a suggested value is 10 KΩ. Solving for the resistors in the general case:

$$R_P = R_O\ (\frac{1 - K_i}{K_P} - 1)$$

$$R_i = R_O\ (\frac{1 - K_P}{K_i} - 1)$$

And solving for our example case:

$R_p$ = 610 KΩ
$R_i$ = 1.45 MΩ

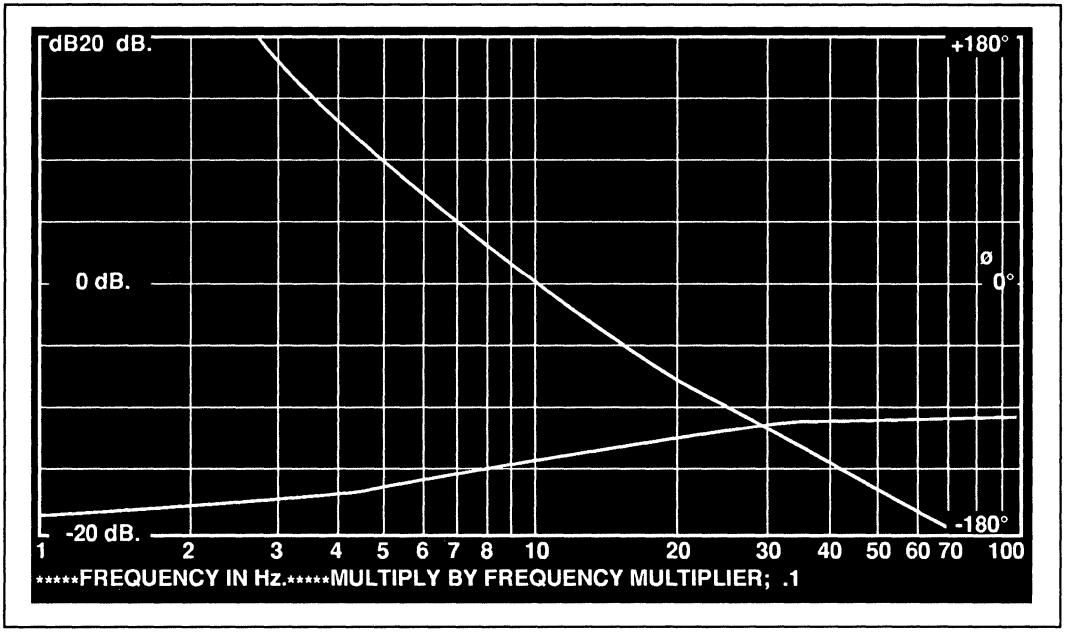



**FIGURE 2: Open Loop Bode Plot**

**Notes:**

December 1992

## INTRODUCTION

The SSI 32P3000 is a high performance pulse detector for 48 Mbits/sec storage system applications. It provides the complete solution for detection and qualification of encoded read signals. The AGC function, noise limiting filtering, pulse slimming, level and time qualifications are all integrated into one chip. Additional features include input impedance control, fast AGC recovery from write-to-read transition, and independent positive and negative threshold qualifications.

The objectives of this application note are to:

- Present a brief description of the SSI 32P3000
- Present a description of the evaluation board of the SSI 32P3000
- Explain in detail key features of the SSI 32P3000

While the evaluation board design does not suggest optimized component values, which vary with system requirements, it presents a means to evaluate the performance of the SSI 32P3000. Test setups in evaluation of pulse pairing, exercise of fast recovery function and others are suggested in this application note.

## 1.0 DESCRIPTION OF THE SSI 32P3000

The AGC amplifier compensates for variations in head preamp output levels, and presents a constant input level to the pulse qualification circuitry. The AGC action can be suspended to hold at a constant gain in embedded servo decode or other processing needs.

A programmable 7-pole Bessel low pass filter is included. Two sets of filter outputs are available: normal low pass output and differentiated low pass output. The signal delays of the two outputs are well matched, ideal in pulse qualification. The filter cutoff frequency can be

(continued)

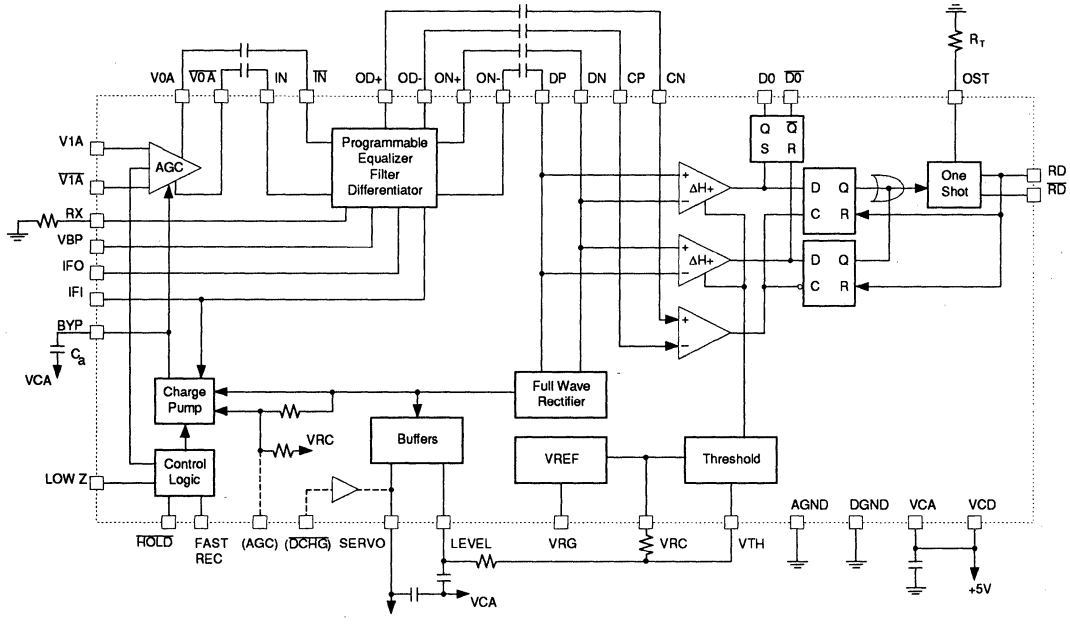



**Figure 1: The SSI 32P3000 Block Diagram**

## 1.0 DESCRIPTION OF THE SSI 32P3000 (continued)

programmed from 9 to 27 MHz, via a current input. Up to 12dB high frequency boost (for pulse slimming) can also be independently programmed. The SSI 32P3000 is ideal for constant density recording.

Both level qualification and time qualification are used in the SSI 32P3000 pulse qualification. For level qualification, the filter output peak can be fed forward to establish the comparator hysteresis threshold. This allows the threshold to track the comparator input amplitude, and to qualify data while AGC amplifier settling is still in transition. The 32P3000 employs a dual-comparator qualification scheme, which allows independent positive and negative threshold detection. This has the advantage of reducing error propagation. For time qualification, the differentiated filter output translates each input peak into a zero crossing, and is used in clocking the comparator outputs.

For each peak of the VIA+/-, there is a one-shot pulse at the differential RD output. The pulse width of the one-shot pulse is determined by a user selected resistor at the OST pin.

The SSI 32P3000 is available in a 36-pin SOM package.

## 2.0 DESCRIPTION OF THE EVALUATION BOARD

The SSI 32P3000 can be evaluated with the 48 Mbit/s Demo Board from Silicon Systems. This board is designed with the Silicon Systems 48 Mbit/s chip set: 32P3000 (36-pin SOM) as the pulse detector, 32D4661 (24-pin DIP) as the time base generator; and 32D539 (44-pin PLCC) as the data synchronizer with 1,7 RLL ENDEC. The SSI 32D4661 provides two digital-to-analog converters (DAC) to program the filter cutoff frequency and the high frequency boost function of the SSI 32P3000 filter. In evaluating the SSI 32P3000, the SSI 32D539 is not needed.

This evaluation board requires the Silicon Systems Serial Communication Board to interface between a RS232 serial port and the SSI 32P4661. This reduces the filter programming to simple inputs through an IBM PC. Details in programming steps are discussed in a later section.

The analog inputs, VIA+/-, mode control inputs, LOWZ, HOLD- and FAST REC, and read data outputs, RD+/- of the SSI 32P3000 are accessible through pin terminals. The filter inputs and outputs are not brought out to pin terminals, but accessible at the pads of their respective coupling capacitors.

## 3.0 EQUIPMENT AND SOFTWARE REQUIREMENTS

To facilitate the following demonstrations of the SSI 32P3000 with the Silicon Systems 48MB Demo Board, the following equipment and software are needed:

- IBM PC with serial port on COM1
- Crosstalk communication software
- Silicon Systems Serial Communication Board
- Serial port setup file, provided with evaluation board
- +5V, +12V and -12V power supplies to the Serial Communication Board
- +5V power supply to Silicon Systems 48MB Demo Board
- TTL pattern generator
- Signal generator, with amplitude modulation input
- Oscilloscope
- Spectrum analyzer, with a tracking output, for filter characteristics measurements
- Time interval analyzer, for pulse pairing measurement

## 4.0 DEMONSTRATIONS

Four demonstration setups are presented in this section for:

- general functionality
- pulse pairing
- filter characteristic
- fast recovery exercise

### 4.1 SOFTWARE SETUP & COMMANDS

To facilitate filter cutoff frequency and high frequency boost control, an RS232 serial port is used to command the two 7-bit DACs in the SSI 32D4661.

Two files can be found on the Silicon Systems Serial Port Setup Disk: "SERIAL.XTS" and "SERIAL.XTK". Both files should be copied to the Crosstalk directory. At prompt, type **xtalk serial**. Now, the Silicon Systems Serial Comm Board and the 32D4661 are ready to accept control commands from the keyboard.

### 4.1 SOFTWARE SETUP & COMMANDS (continued)

In evaluating the SSI 32P3000, only two functions are controlled from the keyboard: the filter cutoff frequency and the high frequency boost. Because each DAC in the SSI 32D4661 is a 7-bit DAC and the Silicon Systems Serial Comm Board data is 4-bit wide, two registers are needed for each function control. Registers 8 and 9 are for high frequency boost control; Registers 10 and 11 are for filter cutoff frequency control. Other registers are used to control the SSI 32D539 functions which are not covered in this application note.

Upon power up of the evaluation board and the communication board, these registers must be initialized by the user. For now, type **R8=0 R9=0 R10=7 R11=15**, followed by a carriage return. Details are given in Section 5.4 filter characteristics discussion. The above command sets the filter at 27 MHz cutoff frequency with no boost.

### 4.2 GENERAL FUNCTIONALITY

Figure 2 shows a general setup to evaluate the SSI 32P3000. In normal read operation, the following conditions should be set: LOWZ=0, HOLD-=1 and FAST REC=0. With an 18 MHz, 200 mVpp sinusoidal input, the RD+/- shows a pulse corresponding to each positive peak and each negative peak, as shown in Figure 3. The pulse width has been preset to be ~ 10ns, with RT = 3kΩ. The user may change the pulse width by replacing RT.

RT = 302Ω + Pulse Width / [ 0.159 ( 22 pF + Cstray ) ]
RT should be between 3 kΩ to 10 kΩ.

### 4.3 PULSE PAIRING MEASUREMENT

The SSI32P3000 has demonstrated excellent pulse pairing performance, less than 500ps. Pulse pairing is one of the most critical parameters of any pulse detector. It is defined to be the systematic time error from ideal, caused by comparator threshold offset, in pulse detection of an input signal peak.

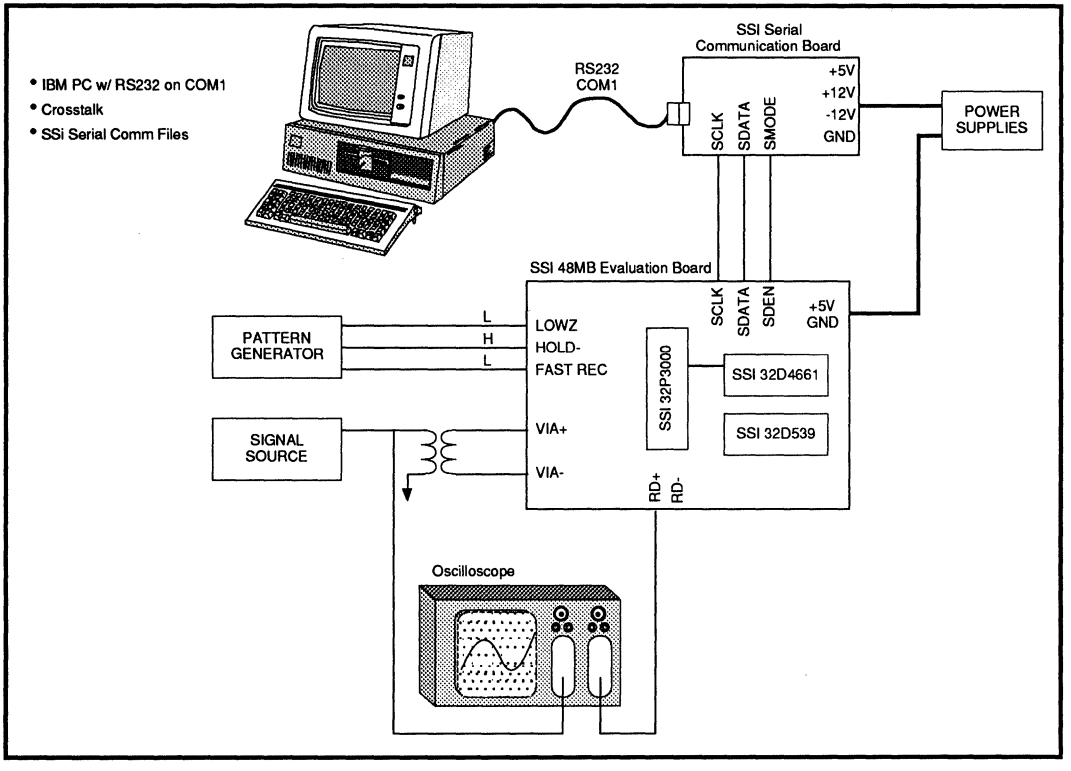



**Figure 2: SSI 32P3000 Evaluation Board General Setup**

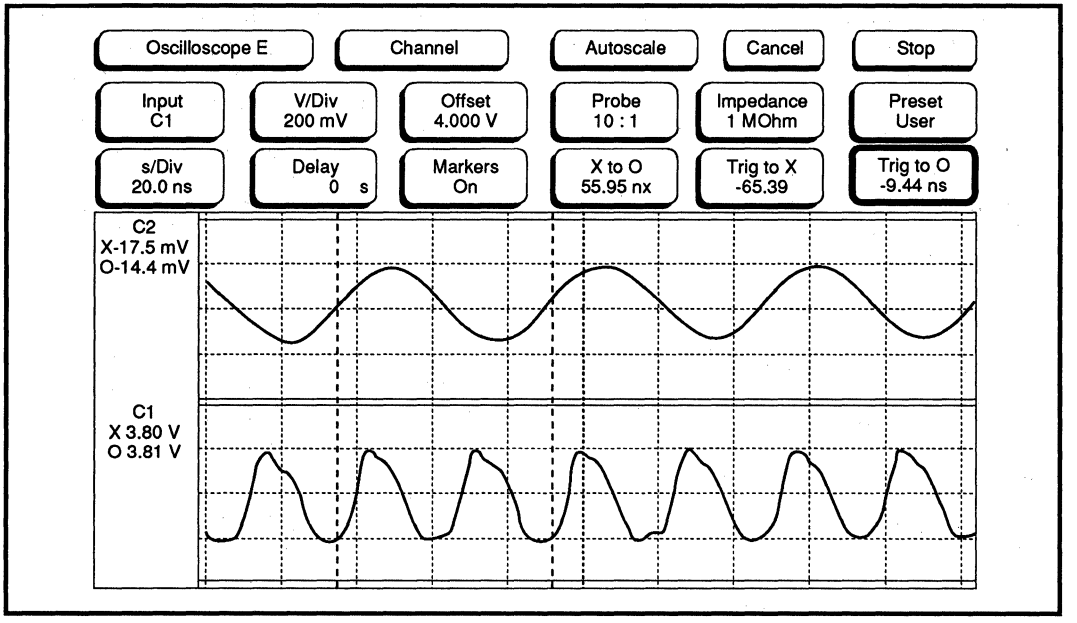



**Figure 3: Normal Read Function: 18 MHz Sinusoidal Input (top) and RD Pulses (bottom)**

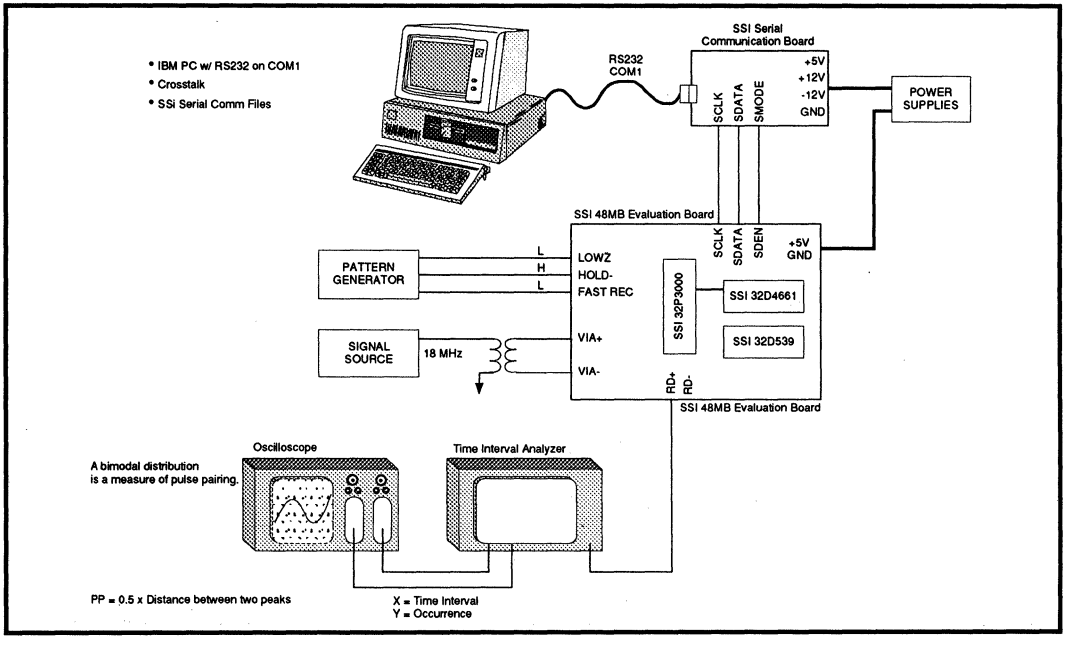



**Figure 4: SSI 32P3000 Evaluation Board Pulse Pairing Setup**

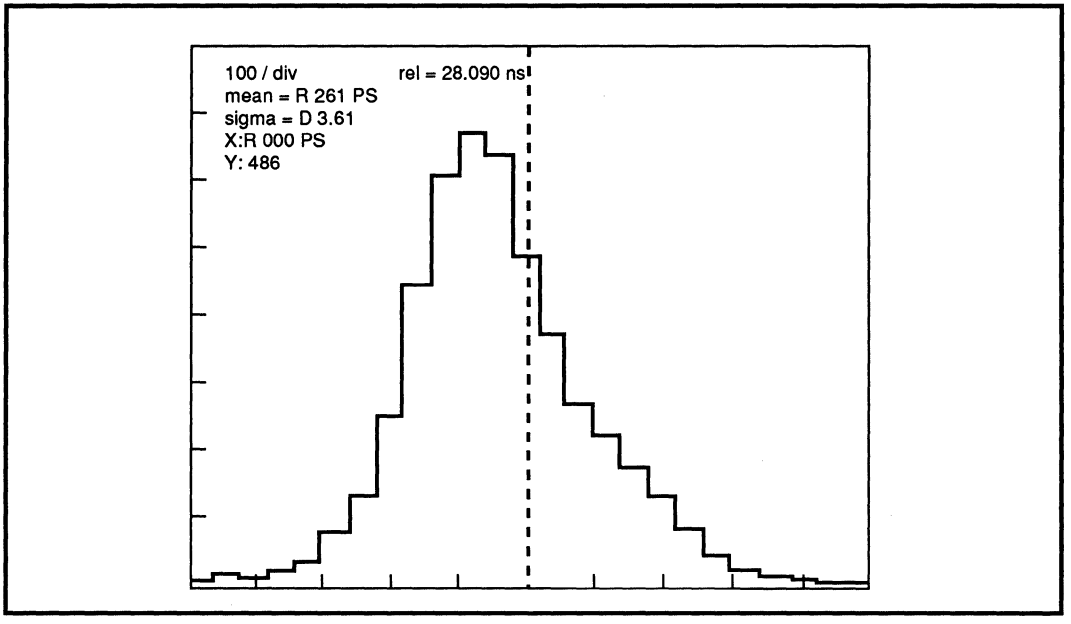



**Figure 5: Histogram of RD Periods with 18 MHz Sinusoidal Input**
**No Bimodal Distribution => Pulse Pairing less than 500 ps**

### 4.3 PULSE PAIRING MEASUREMENT (continued)

The test procedure is as follows:

- Feed a low jitter sinusoidal input
- Measure the time distance between RD pulses, corresponding to one positive peak detection and one negative peak detection
- Histogram plot measurements
- Significant pulse pairing will appear as a bimodal distribution of time period measurements
- Pulse pairing can be calculated as half of the time distance between two peaks in the histogram plot

Figure 4 shows a setup for the pulse pairing measurement. The SSI 32P3000 has demonstrated less than 500 ps pulse pairing, as shown in Figure 5.

### 4.4 FILTER CHARACTERISTIC

The SSI 32P3000 is ideal for constant density recording application with its programmable filter. The filter is a 7-pole Bessel low pass filter with normal output, as well as differentiated output. The normal output is for level qualification; the differentiated output is for time qualification. Their signal delays are well matched. The group delay is maintained within ±300 ps from 0.3 $fc$ to $fc$. The filter cutoff frequency can be programmed from 9 MHz to 27 MHz through a current input at the IFI pin. The high frequency boost can be programmed from 0 to 12 dB through a voltage input at the VBP pin.

$fc$ = 45 x IFI MHz; IFI in mA (at room temp.)

Boost = 20 x log [ Kb (VBP / VRG) + 1 ] dB;
VRG is reference voltage at Pin 1.

Kb = 3.041 + 0.0276 x fci, where fci is the ideal cutoff frequency.

Figure 6 shows a test setup to evaluate the frequency response of the SSI 32P3000 filter. The SSI 32D4661 provides two 7-bit DACs for ease of programming.

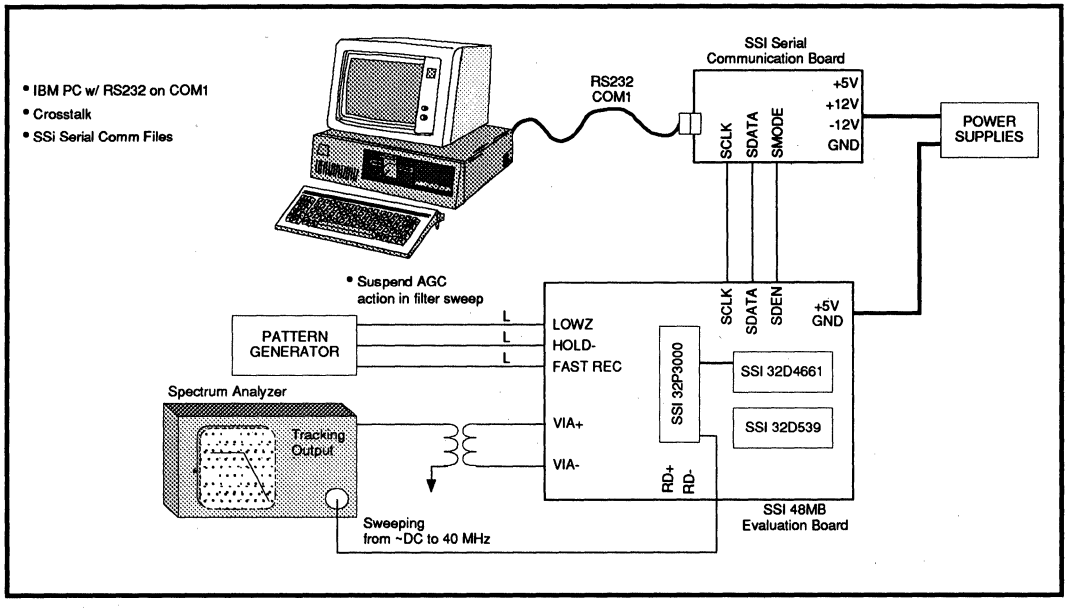



**Figure 6: SSI 32P3000 Evaluation Board Filter Characteristic Setup**

The full scale DAC value, i.e., Code 127, corresponds to maximum cutoff frequency, 27MHz, or maximum boost, 12dB. In decimal code, the cutoff frequency and high frequency boost can be calculated as follows:

$fc$ = 27 MHz x ( DACF Code ) / 127;
42 ≤ DACF Code ≤ 127

Boost = 20 x log [ Kb x ( DACS Code ) / 127 + 1 ] dB;
0 ≤ DACS Code ≤ 127

Because the Silicon Systems Serial Communication Board works with 4-bit nibbles, each 7-bit code is divided into two registers. For cutoff frequency control, R10 and R11 represents the 3 most significant bits (MSB) and the 4 least significant bits (LSB), respectively. Only the lower 3 bits of R10 4-bit nibble is used. For high frequency boost control, R8 and R9 represents the 3 MSBs and the 4 LSBs, respectively.

For example, the user wants to program the filter to 14 MHz cutoff with 3 dB boost. The DAC codes are calculated as the following:

DACF Code = 127 x 14 / 27 = 66, R10=4 R11=2;

DACS Code = 127 x [ 10^( 3 / 20 ) -1 ] / 3.467 = 15,

R8=0 R9=15.

At the keyboard, the user enters **R8=0 R9=15 R10=4 R11=2**, followed by a carriage return.

To evaluate the frequency response of the filter, the AGC amplifier gain must be held constant, HOLD-=0. The tracking output of the spectrum analyzer sweeps the signal over a frequency spectrum. The filter output can be examined at the pad of C5 on the board. Figure 7 shows the filter responses at 9MHz and at 27MHz. Figure 8 shows the filter response with no boost and that with maximum boost.

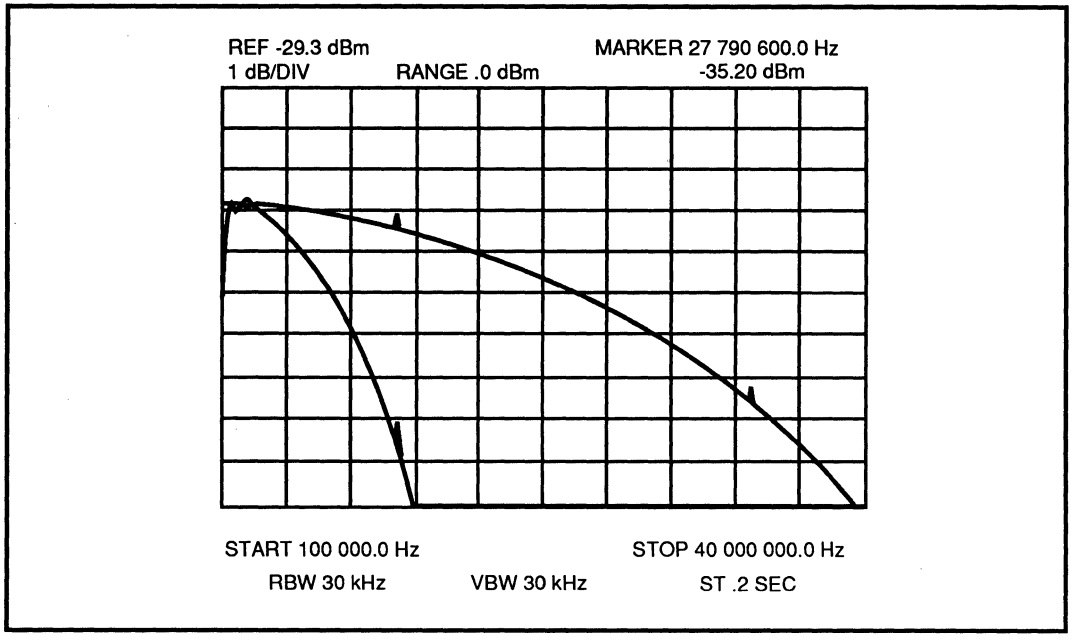



**Figure 7: SSI 32P3000 Filter Magnitude Responses at 9 MHz (left) and 27 MHz (right) Cutoff**

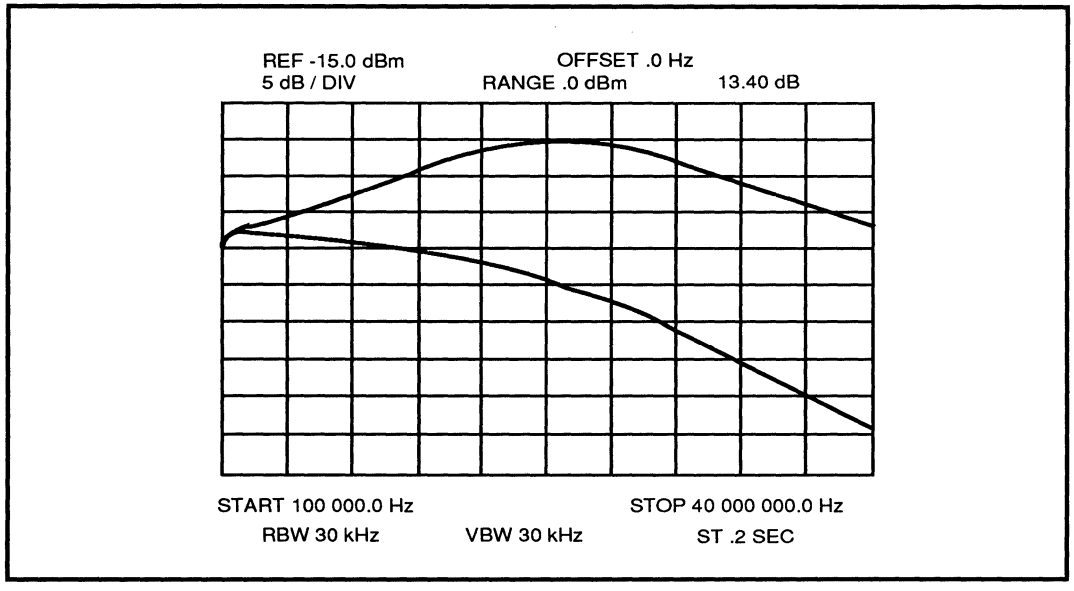



**Figure 8: Cutoff Frequency = 14 MHz. The SSI 32P3000 Filter Response with no boost (bottom) and with maximum boost (top)**

### 4.5 AGC ACTIONS & RECOVERY

The SSI 32P3000 has the following AGC control features:

- Automatic

  Fast Attack: When the DIN+/- input exceeds the preset nominal level (1Vpp) by 25%, a fast attack current, 2.24 x IFI, quickly discharges CBYP and lowers the AGC amplifier gain.

  Slow Attack: When DIN+/- input exceeds the preset nominal level by less than 25%, a slow attack current, 0.32 x IFI, discharges CBYP and lowers the AGC amplifier gain until DIN+/- returns to nominal level.

  Slow Decay: When the DIN+/- input falls below the preset nominal level, a small decay current, 0.008 x IFI, charges CBYP and increases the AGC amplifier gain until DIN+/- returns to nominal. Because Fast Attack and Slow Attack currents are much larger than that of Slow Decay, it is obvious that AGC amplifier gain can be lowered quickly, but can only be increased very slowly. The purpose of the large ratio between attack/decay current is to ensure that the AGC settles to the peak-to-peak voltage amplitude.

- User Control

  Fast Recovery: To recover the AGC amplifier gain from a low gain condition rapidly, the FAST REC can be asserted. With FAST REC = 1, a fast decay current, 0.16 x IFI, charges CBYP continuously, independent of signal level. While the Fast and Slow Attacks are still active, the AGC amplifier gain settles quickly to ~125% of nominal. When the FAST REC returns to 0, the Fast Attack and Slow Attack actions restore the AGC amplifier gain to 100% level.

  Hold: When HOLD- = 0, all the above AGC actions are suspended. The AGC amplifier gain is held constant, except for leakage effects.

The setup in Figure 9 is used to demonstrate the advantage of the FAST REC function. Figures 10a & 10b show the AGC amplifier gain recovery time without and with the FAST REC function, respectively. Without the FAST REC function, the AGC amplifier gain slowly recovers to the 100% nominal level, due to the small decay current. With the FAST REC function, the AGC amplifier gain quickly reaches 125%+. When the FAST REC returns to 0, the attack time is very short. One application of the FAST REC function is immediately after a long hold period during which the gain could have drifted low.

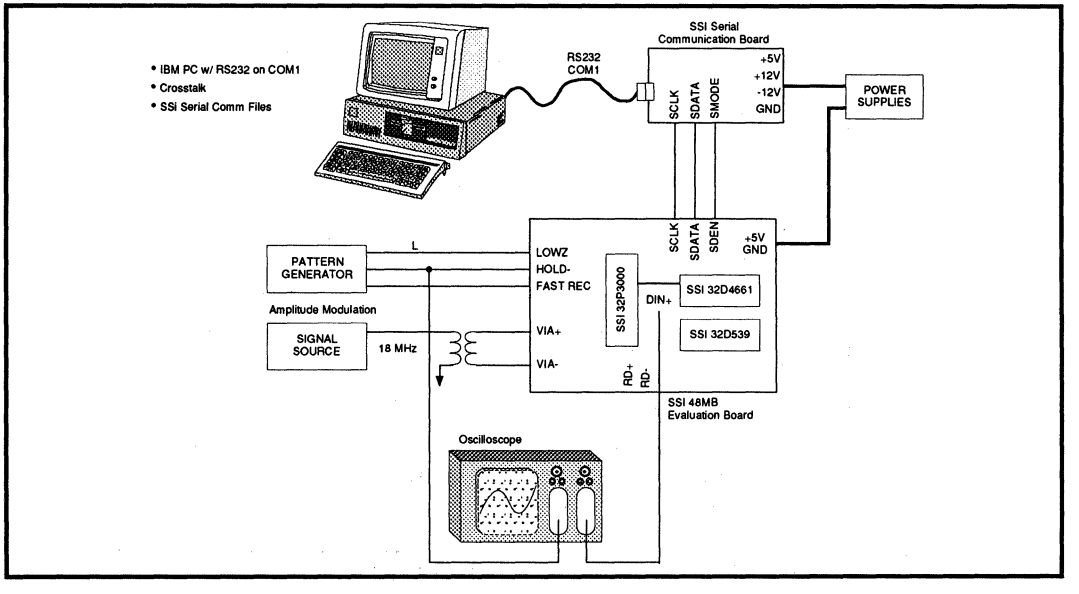



**Figure 9: SSI 32P3000 Evaluation Board AGC Recovery Setup**

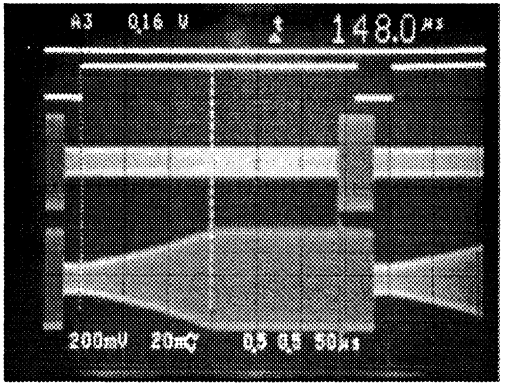



Figure 10: AGC Recovery Without Using FAST REC
FAST REC = 0
HOLD-
Analog Input: Amplitude Modulated to Simulate Gain Change
DIN±

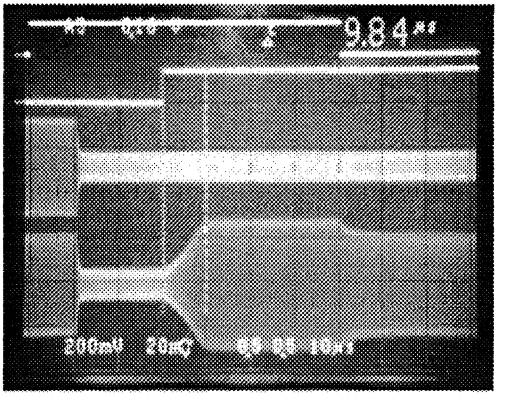



Figure 11: AGC Recovery With FAST REC
FAST REC
HOLD-
Analog Input
DIN±: Note fast recovery settling to above 100% and attacking at the end of fast recovery

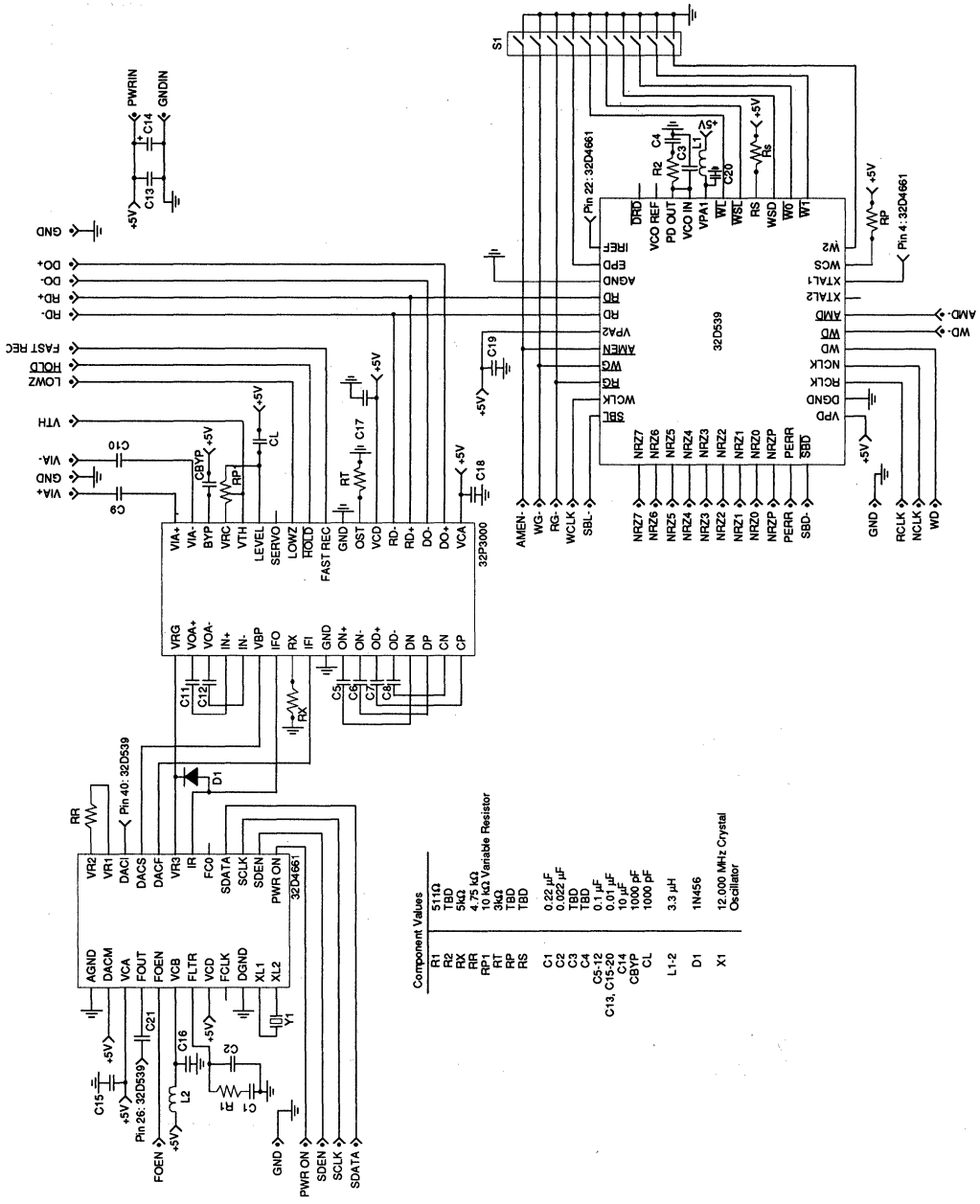



FIGURE 12: 32P3000 / 32D539 / 32D4661 Evaluation Board Schematic

silicon systems®
A TDK Group Company

# SSI 32P4730/4731
## Single-Chip Read Channel Device
## Application Note

January 1993

## 1.0 INTRODUCTION

Silicon Systems Inc. is pleased to introduce the SSI 32P4730 /4731, the highest performance single-chip read channel device available. This device contains all the functions needed to implement a complete zoned recording read channel for hard disk drive systems. The functional blocks include a pulse detector, programmable filter, 4-burst servo circuit, time base generator, and a data separator with a 1,7 RLL ENDEC. The data sheet shows the device block diagram of the SSI 32P4730 and 32P4731, respectively. The operating NRZ data rate is programmable from 8 to 24 Mbit/s.

*While both the SSI 32P4730 and 32P4731 provide a 4-burst servo capture circuitry, the distinction is in the servo output form. The SSI 32P4730 features A+B, A-B and C-D outputs. The SSI 32P4731 features individual Burst A, B, C and D outupts.*

This application note details the operation of all functional blocks of the SSI 32P4730/4731. This is an abridged applications note for the SSI 32P473014231, a more detailed note is available upon request. Design notes and evaluation techniques are suggested when applicable. This note is intended to supplement the device specification. For updated device parameter limits, the user is recommended to refer to the specification.

### GENERAL FEATURES

- Programmable data rate 8 - 24 Mbit/s
- Low power dissipation 450 mW typ @ 24 Mbit/s and 5V supply
- Bi-directional serial port programming
- Flexible power management less than 5 mW in complete power down
- Wide power supply range 4.5 to 5.5 V
- Small footprint 64-lead TQFP package

### Pulse Detector

- Fast attack / decay mode for rapid AGC recovery
- Dual rate charge pump for fast transient recovery
- Programmable qualification threshold
- Low drift AGC hold circuitry
- Temperature compensated, exponential control AGC
- Wide bandwidth, high precision full-wave rectifier
- Dual mode pulse qualification circuitry (user selectable)
- TTL $\overline{\text{RDIO}}$ signal output for servo timing support
- Internal Low-Z and fast decay timing for rapid transient recovery and AGC acquisition
- 0.5 ns max pulse pairing

### Servo Capture

- 4-burst servo capture
- Internal hold capacitors
- Separate registers for filter cutoff and qualification threshold in servo mode
- Servo AGC level programmable via 4-bit DAC
- P4730: A+B, A-B and C-D outputs
  P4731: Burst A, B, C and D outputs

### Programmable Filter

- Cutoff frequency programmable from 3 to 9 MHz, within ±10% accuracy
- Boost programmable from 0 to 13 dB
- Matched normal and differentiated outputs
- Constant group delay, within ±2% variation
- Low Z for rapid transient recovery
- No external filter components needed

### Time Base Generator

- Better than 1% frequency resolution
- Up to 75 MHz frequency output
- Independent M and N divide-by counters
- VCO center frequency matched to data synchronizer VCO

### Data Separator

- Fast acquistion phase lock loop with zero phase restart technique
- Programmable high phase detector gain switch for fast acquisition
- Integrated 1,7 RLL encoder/decoder
- Programmable decode window symmetry control via serial port
- Programmable write precompensation
- Hard and soft sector operation

## 2.0 CONTROL REGISTER MAPPING & SERIAL INTERFACE DESCRIPTION

For flexible system applications, the SSI 32P4730/31 features 14 control registers for device configuration. The control words can be loaded to or read back from these registers via the 3-pin serial interface. This section defines the register mapping and the serial interface timing.

Upon power up from no supply voltage state, the control registers are at random state, and should be programmed before system operation. The control register contents are retained when the device is powered down to idle mode, i.e. with $\overline{PWRON}$ = 1.

### 2.1 COMMAND REGISTER MAPPING

**Power Down Control Register**

Address (A6..A0) = 0 0 0 0 0 1 0 = $02_{HEX}$

| | | |
|---|---|---|
| D7 (MSB) - D5 | | Internal hardwired for factory use only |
| D4 | = 1 | Time Base Generator is disabled, reducing power dissipation by 100 mW. |
| | = 0 | Time Base Generator is active. |
| D3 | = 1 | Data Separator is disabled, reducing power dissipation by 120 mW. |
| | = 0 | Data Separator is active. |
| D2 | = 1 | Programmable Filter is disabled, reducing power dissipation by 100 mW. |
| | = 0 | Programmable Filter is active. |
| D1 | = X | Not used, don't care |
| D0 | = 1 | Pulse Detector/Servo is disabled, reducing power dissipation by 75 mW. |
| (LSB) | = 0 | Pulse Detector/Servo is active. |

**Data Mode Cutoff Register**

Address (A6..A0) = 0 0 0 0 0 1 1 = $03_{HEX}$

D7 (MSB)= X Not used, don't care

D6..D0 Filter cutoff frequency control in the data read mode.

$fc$ (MHz) = 9 • Code / 127

Maximum code, 1111111 or 127 decimal, represents the maximum 9 MHz cutoff frequency.

Minimum code is 42, for 3 MHz cutoff frequency.

**Servo Mode Cutoff Register**

Address (A6..A0) = 0 0 1 0 0 1 1 = $13_{HEX}$

D7 (MSB)= X Not used, don't care

D6..D0 Filter cutoff frequency control in the Servo mode.

**Filter Boost Register**

Address (A6..A0) = 0 0 0 1 0 1 1 = $0B_{HEX}$

| | | |
|---|---|---|
| D7 | =1 | Filter boost remains active in the Servo mode. |
| (MSB) | =0 | Filter boost is disabled in the Servo mode. |
| D6..D0 | | Filter boost control setting<br>Boost (dB) =<br>20 log [(0.0273 • Code) + 1] |
| | | Maximum boost, 13 dB, is set with Code = 127 decimal. |
| | | Minimum code, 0, represents no boost. |

**Data Threshold Register**

Address (A6..A0) = 0 0 0 1 0 1 0 = $0A_{HEX}$

| | | |
|---|---|---|
| D7 | = 1 | Window Threshold Qualification in Data Read Mode |
| (MSB) | = 0 | Hysteresis Threshold Qualification in Data Read Mode |
| D6..D0 | | Qualification threshold percentage setting in Data Read Mode |
| | | Qual % = 97.6% • Code / 127 |
| | | Qual % should be limited between 10% to 80%. Thus, this code should be restricted from 13 to 104. |

**Servo Threshold Register**

Address (A6..A0) = 0 0 1 0 0 1 0 = $12_{HEX}$

| | | |
|---|---|---|
| D7 | = 1 | Window Threshold Qualification in Servo Mode |
| (MSB) | = 0 | Hysteresis Threshold Qualification in Servo Mode |
| D6..D0 | | Qualification threshold percentage setting in Servo Mode |

**Control A Register**

Address (A6..A0) = 0 0 1 1 0 1 0 = $1A_{HEX}$

D7 (MSB) = 1 Not in fast decay current test mode

= 0 Fast decay current is always turned on, for test use only. Other AGC actions, such as $\overline{HOLD}$, attack, ... remain active.

D6-5 Test point source select bits, work in combination with *Control B Register :* D6. See Section 4.5.

D4 = 1 Frequency synthesizer is bypassed. TBG output = FREF

= 0 Frequency synthesizer is active. TBG output = FREF • [(M+1) / (N+1)].

D3 = 1 Enables test point MTP3

= 0 Test point MTP3 forced to Logic 1

D2 = 1 TBG phase detector pump down state, for test use only.

= 0 Not in TBG phase detector Pump Down Test mode

D1 = 1 TBG phase detector pump up state, for test use only

= 0 Not in TBG phase detector Pump Up Test mode

D0 = 1 TBG phase detector active

= 0 TBG phase detector disabled, allowing pump up/down test modes

**Only one bit of {D0, D1, D2} can be set to 1 at any one time. Violation causes indeterminate state.**

**Control B Register**

Address (A6..A0) = 0 0 0 1 1 0 0 = $0C_{HEX}$

D7 (MSB)= X Not used, don't care

D6 = 1 Enables test points MTP1 and MTP2

= 0 Test points MTP1 and MTP2 forced to Logic 1

D5 = 1 Data Separator phase detector pump down state, for test use only

= 0 Not in Data Separator phase detector Pump Down Test mode

D4 = 1 Data Separator phase detector pump up state, for test use only

= 0 Not in Data Separator phase detector Pump Up Test mode

D3 = 1 Data Separator phase detector active

= 0 Data Separator phase detector disabled, allowing pump up/down test modes

**Only one bit of {D3, D4, D5} can be set to 1 at any one time. Violation causes indeterminate state.**

D2 = 1 The $\overline{RDIO}$ pin is an input pin.

= 0 The $\overline{RDIO}$ pin is an output pin.

D1 = 1 Data Separator phase detector gain shift is enabled.

= 0 Data Separator phase detector gain shift is disabled. See Section 4.8.

D0 = 1 Direct write enabled, i.e. write data bypasses the ENDEC.

= 0 Direct write disabled, i.e. write data is encoded before appearing at write data output.

**N Counter Register**

Address (A6..A0) = 0 0 0 0 1 1 0 = $06_{HEX}$

D7 (MSB)= X Not used, don't care

D6..D0 7-bit N counter code in Time Base Generator frequency synthesizer

See Section 4.3 for N selection.

N Counter can be programmed anytime, but becomes effective only after a subsequent Date Rate Register programming.

**M Counter Register**

Address (A6..A0) = 0 0 0 1 1 1 0 = $0E_{HEX}$

D7..D0 8-bit M counter code in Time Base Generator frequency synthesizer

Fout = [(M + 1) / (N + 1) ] • Fref,

Fout = TBG output frequency

Fref = Reference frequency @ FREF pin

M Counter can be programmed anytime, but becomes effective only after a subsequent Date Rate Register programming.

## 2.0 CONTROL REGISTER MAPPING & SERIAL INTERFACE DESCRIPTION (continued)

### 2.1 COMMAND REGISTER MAPPING (continued)

**Data Rate Register**

Address (A6..A0) = 0 0 0 0 1 0 0 = $04_{HEX}$

D7 (MSB) = X Not used, don't care

D6..D0 Per data rate, code sets the VCO center biasing

Code = $(3 \cdot DR_{MHz} - 4.27) / 0.622$, (use 1.5 • DR for 1.5X VCO's)

For 20 Mbit/s operation, Code = 90, i.e. 1011010

**Window Shift Register**

Address (A6..A0) = 0 0 0 0 1 0 1 = $05_{HEX}$

D7..D6 = 00 Fc DAC output, i.e. filter cutoff, @ DACOUT

= 01 Vth DAC output, i.e. qualification threshold, @ DACOUT

= 10 Ws DAC output, i.e. window shift, @ DACOUT

= 11 Wp DAC output, i.e. write precomp, @ DACOUT

D5 = 1 Window shift function enabled

= 0 Window shift function disabled

D4 = 1 Window shift direction : Late

= 0 Window shift direction : Early

D3-0 4-bit code to set the window shift magnitude

Window Shift % of Data Separator VCO Period = 30% - Code • 2%

For 20% shift, Code = 5 i.e. 0101

**Write Precomp Register**

Address (A6..A0) = 0 0 0 1 1 0 1 = $0D_{HEX}$

D7 = 1 Servo burst reset in High Resolution mode

= 0 Servo burst reset in Normal mode

D6..D4 Not used, don't care

D3 = 1 Write Precomp function enabled

= 0 Write Precomp function disabled

D2..D0 3-bit code to set the write precomp magnitude

The need and direction of write precomp is determined by data pattern. But precomp magnitude is programmable via this register as the following:

= 000 7 x TSTS = 0.04 • Data Separator PLL reference clock period, i.e. the TBG output

= 001 6 x

= 010 5 x

= 011 4 x

= 100 3 x

= 101 2 x

= 110 1 x

= 111 No Precomp

**Servo AGC Level / Peak Detector Current Register**

Address (A6..A0) = 0 1 0 0 0 1 0 = $22_{HEX}$

D7..D4 4-bit code to set the output current of the servo peak detector charge pump. The current is programmable from 6µA to 96µa. Maximum noise immunity is obtained in the servo peak detector by choosing the smallest value of charge current.

PDCurrent = ( code • 6 µA) + 6 µA

D3..D0 4-bit code to set the AGC nominal level at the DP/DN in the servo mode only.

Nominal level at DP/DN = 1 - Code • 0.0153 Vppd

For 0.8 Vppd at DP/DN, code = 13, i.e. 1101

## 3.0 MODES OF OPERATION & POWER MANAGEMENT

The SSI 32P4730/4731 has several operating modes that support read, write, servo and power management functions. Mode selection is accomplished by controlling the read gate (RG), write gate (WG), servo gate (SG) and $\overline{\text{PWRON}}$ pins. Additional modes are controlled by programming the *Power Down Control Register* (PDCR), the *Control A Register* (CAR), and the Control B Register (CBR). This section discusses the controls of each mode. The detailed operating functions are presented in Section 4.

### 3.1 POWER MANAGEMENT

For optimal overall system power saving, the SSI 32P4730/4731 allows flexible power down options. With $\overline{\text{PWRON}}$ = 1, the entire device is powered down, except the serial interface and the control register. With $\overline{\text{PWRON}}$ = 0, the device is in normal operation mode. Each individual function can be powered down by programming the *Power Down Control Register.* An important consideration in exercising the power down functions is the recovery time.

The recovery time from a power down mode is application dependent. While most of the internal nodes within the device can recover very quickly, the I/O DC bias settling times depend on the external ac-coupling and bypass capacitors. All TTL logic inputs are not affected by any power down state. However, for low power dissipation, these logic inputs are recommended to be at a logic '1' state. All TTL logic outputs are in high impedance states. These logic outputs return to active state in less than 1 µs after power up. The following are some notes on the other I/Os power down recovery behavior.

| Pin | Power Down Voltage | Typical Recovery Time |
|---|---|---|
| VIA± | 4.0 V | 2 µs |
| DP, DN | 5.0 V | 6 µs |
| CP, CN | 5.0 V | 12 µs |
| IN± | 3.8 V | 5 µs |
| MTP1,2,3 | Pseudo-ECL logic '1' | 350 µs |
| OD± | 4.5 V | 0.5 µs |
| ON± | 4.5 V | 2.8 µs |
| VOA± | 4.4 V | 3 µs |
| DACOUT | 5.0 V | 1 µs |
| TFLT± | 0 V | 13 µs, loop filter dependent |
| DFLT± | 0 V | 13 µs, loop filter dependent |
| LEVEL | 3.9 V | 2 µs |
| RR | 0 V | 0.5 µs |
| RTS | 3.9 V | 20 µs in Non-Servo mode, 0.8 µs in Servo mode |
| RTD | 3.9 V | 20 µs in Non-Data mode, 0.8 µs in Data mode |
| RX | 0 V | 1.5 µs |
| SREF | 0V | 100µs |
| A-B | 5V | |
| C-D | 5V | |
| A+B | 5V | |
| BYP | Leakage effect only | |

## 3.0 MODES OF OPERATION & POWER MANAGEMENT (continued)

### 3.2 READ MODE

When $\overline{PWRON}$ = 0, SG=0 and RG = 1, the SSI 32P4730/4731 is in Data Read mode. All the control bits in the *Power Down Control Register* must be reset to 0.

In the data read mode, all functions of the SSI 32P4730/31, except the servo, are active. The AGC amplifier amplifies the read signal. The low pass filter bandlimits the high frequency noise and applies pulse slimming. The pulse qualifier validates each valid signal peaks. The time base generator provides an internal frequency reference to the data separator at 3X the NRZ data rate. The data separator phase locked loop is locked onto the read data pulses from the pulse qualifier. The clock is extracted from the data bits. The data is re-synchronized and decoded into NRZ data.

The servo outputs remain to be valid and are held constant from the previous servo sampling.

### 3.3 WRITE MODE

When $\overline{PWRON}$ = 0, SG=0, RG = 0, and WG = 1, the SSI 32P4730/31 is in write mode. At the least, the data separator and the time base generator control bits in the *Power Down Control Register* must be reset to 0.

In the write mode, the SSI 32P4730/31 accepts the NRZIN input at each rising edge of the WCLK. The data is encoded into 1,7 RLL codes, unless the ENDEC bypass is chosen for direct write. Write precompensation, if enabled, is applied to selected data pattern. The coded data is re-synchronized at the $\overline{WD}$ output by the internal data separator reference clock.

The pulse detector and programmable filter are not used in the write mode. The AGC amplifier gain is held constant at prior to entering the write mode. The servo outputs remain to be valid and are held constant from the previous servo sampling.

| $\overline{PWRON}$ | SG | RG | WG | MODE |
|---|---|---|---|---|
| 1 | X | X | X | SLEEP |
| 0 | 0 | 0 | 0 | IDLE |
| 0 | 1 | X | X | SERVO |
| 0 | 0 | 1 | X | READ |
| 0 | 0 | 0 | 1 | WRITE |

**Mode Control**

### 3.4 SERVO MODE

When $\overline{PWRON}$ = 0 and SG = 1, the SSI 32P4730/4731 is in Servo mode. At the least, the pulse detector/servo and the programmable filter control bits in the *Power Down Control Register* must be reset to 0.

While the SSI 32P4730 and the SSI 32P4731 feature different servo outputs, both share the same servo sampling sequence in operation. In the servo mode, the AGC amplifier remains active. A servo AGC pattern should be provided for servo AGC with the $\overline{HOLD}$ input at '1'. With the $\overline{HOLD}$ input at '0', the AGC amplifier gain is held constant. The servo A, B, C and D bursts are sampled and captured.

The servo operation, with the distinctions between the SSI 32P4730 and the SSI 32P4731, is detailed in Section 5.0.

## 4.0 READ MODE EVALUATION

As a single-chip read channel IC, the SSI 32P47304731 supports many functions in read mode alone. This section discusses the functions of the various blocks. Where appropriate, lab experiments are suggested in evaluation.

### 4.1 PULSE DETECTOR FUNCTION

The pulse detector is the first block of the SSI 32P4730/4731. It amplifies, validates and time-preserves the read signal from a read/write pre-amp, such as the SSI 32R2020. The pulse detector block includes the wideband AGC amplifier, the AGC control circuitry, the 7-pole programmable low pass filter, and the pulse qualifier.

#### 4.1.1 AGC Amplifier & Control

The wideband AGC amplifier accepts a low amplitude read signal, typically <200 mVppd, and amplifies it to a larger amplitude prior to pulse qualification. Because of varying head-to-media conditions, the amplifier gain is automatic-gain controlled to provide a 1Vppd signal at the DP/DN pins. The amplifier gain is an exponential function of the voltage at the BYP pin. For reference use only, the gain function is Av = 12 exp {2.5 ( V@BYP + 2.15 - VPG)}. Internal clamp circuitry clamps the BYP pin voltage between ~2.0V and ~3.5V. The clamp resistance is <10 Ω. It is advised not to sink or source more than 3 mA at the BYP pin.

The AGC actions are current charging and discharging the external BYP integrating capacitor to maintain a 1Vppd at the DP/DN pins. They are described as follows:

- Slow Decay
  When the instantaneous DP/DN signal is below 1Vppd, a slow decay current, 4.0 µA, charges the BYP capacitor. The AGC amplifier gain is increased slowly.
- Slow Attack
  When the instantaneous DP/DN signal exceeds 1Vppd, but is below 1.25 Vppd, a slow attack current, 0.18 mA, discharges the BYP capacitor. The AGC amplifier gain is decreased.
- Fast Attack
  When the instantaneous DP/DN signal exceeds 1.25Vppd, the device enters a fast attack mode. A fast attack current, 1.26 mA, discharges the BYP capacitor. The AGC amplifier gain is quickly lowered.
- Write-to-Read Recovery
  With a 1-to-0 transition of the WG, the SSI 32P4730 enters the write-to-read recovery mode. The input impedance remains in low impedance state for 1 µs for fast input DC coupling recovery. Then, the device restores to high input impedance state, and enters into a fast decay mode. In the fast decay mode, a high current quickly charges the BYP capacitor until the signal at DP/DN exceeds 125% of nominal. After reaching 125%, the high current is disabled and the slow attack sequence commences. (Otherwise only the slow decay mode is available to increase the AGC amplifier gain.) Figure 4.1.1 shows the write-to-read AGC action timing. This same sequence is executed when the device switches from power down to power up mode.

All the AGC actions are suspended in any one of the following conditions:

- $\overline{\text{HOLD}}$ = 0, or
- Write mode.

The AGC amplifier gain is then held constant, except for leakage effect.

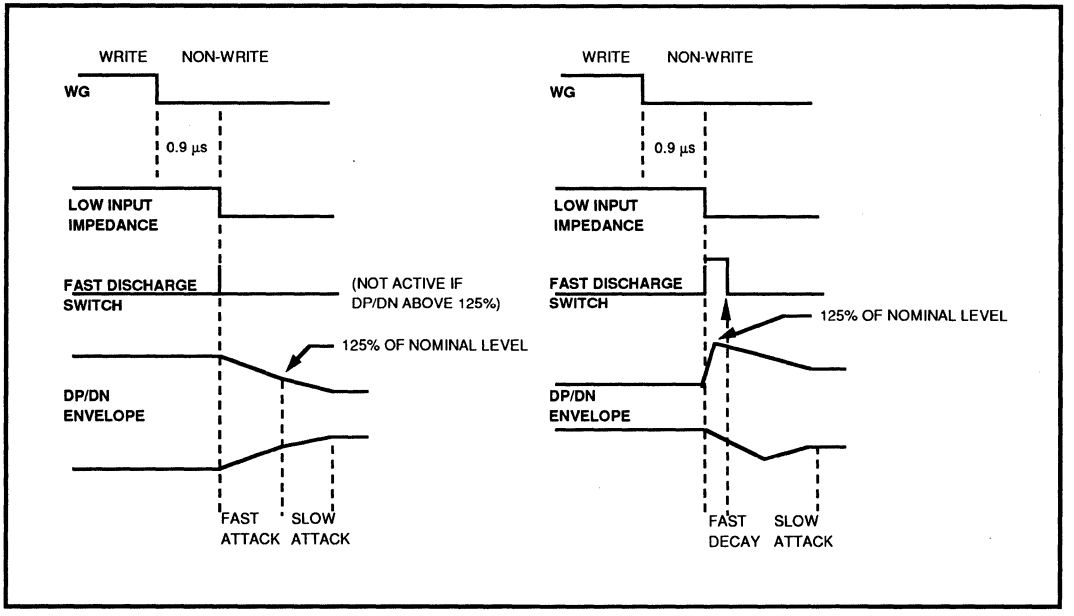



**FIGURE 4.1.1: AGC Action Timing in Write-to-Read Recovery**

## 4.0 READ MODE EVALUATION (continued)

### 4.1 PULSE DETECTOR FUNCTION (continued)

#### 4.1.2 Low Pass Filter Function

From the head/media point to the AGC amplifier output, the signal path should have very wide bandwidth, and is therefore noisy. To reduce false pulse qualification, the SSI 32P4730 includes a 7-pole 0.05° phase equiripple programmable low pass filter to reject noise beyond the signal frequency of interest. In addition, this filter provides pulse slimming equalization for improved pulse pairing performance. Ideal for zoned bit recording applications, the filter bandwidth and the pulse slimming equalization are both programmable through the serial port. The filter's normal low pass output, ON±, is the input to the pulse qualifier.

An additional function of the filter is to provide a time differentiated signal of the read data, i.e. 90° phase lead. Each read data peak is translated into a zero-crossing at the OD±. This time differentiated output is used in time qualification as described in the next topic.

The control and the dynamics of the filter are discussed in Section 4.5.

#### 4.1.3 Pulse Qualifier Function

The pulse qualifier transforms each valid analog read data pulse into a digital pulse, while preserving the relative time position of each valid pulse peak. Each DP/DN pulse is validated by a combination of level qualification and time qualification. The SSI 32P4730/4731 supports two methods of level qualification: window threshold qualification and hysteresis qualification. In time qualification, the time differentiated filter output is used to locate the signal peaks in time.

**Level Qualification**

The two options in level qualification are: window threshold qualification and hysteresis qualification.

*Window Threshold Qualification*: When in window threshold qualification mode, independent positive and negative threshold qualification comparators are used. A slight amount of local hysteresis is included to increase the comparator output time when a signal that just exceeds the threshold level is detected. This eases the timing with respect to the zero crossing clock comparator. Any peak, regardless of polarity, which exceeds the programmed threshold level triggers the read data one-shot. Qualification thresholds from 10% to 80% may be set with a resolution of 1%. A parallel R-C network of RTD and CT set the hysteresis threshold time constant when not in the Servo mode.

*Hysteresis Qualification*: When the hysteresis qualification mode is selected, the same threshold qualification mode is selected, the same threshold qualification comparators and clock comparators are used to implement a polarity checking rule. In this mode, a positive peak that clears the established threshold level will set the hysteresis comparator and trigger the bidirectional one-shot that creates the read data pulses. In order to get another pulse clocked out, a peak of the opposite polarity must clear negative threshold level to reset the hysteresis comparator and trigger the bidirectional one-shot.

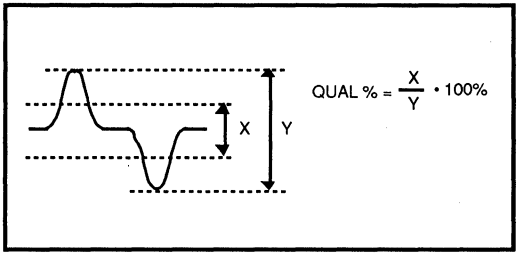



**FIGURE 4.1.2: Qualification Percentage Definition**

Qualification threshold in percentage is defined to be the distance between the positive threshold and the negative threshold as a percentage of the DP/DN peak-to-peak. The SSI 32P4730 has a 7-bit DAC to allow flexibility in qualification % setting through serial port programming, with better than 1% resolution.

Qualification Percentage = 97.6% • DAC Code / 127.

Because the qualification percentage should be between 10% to 80%, the DAC Code must be limited between 13 and 104, in decimal. Operation outside of this range may result in qualification percentage setting inaccuracy.

The qualification threshold DAC can accept its 7-bit input code from one of two registers, *Data Threshold Register or Servo Threshold Register*, depending on the operation mode. Thus, the qualification percentage can be set separately for the normal data read mode and the servo mode. The MSB bit (D7) of each register selects the level qualification method, either window threshold or hysteresis.

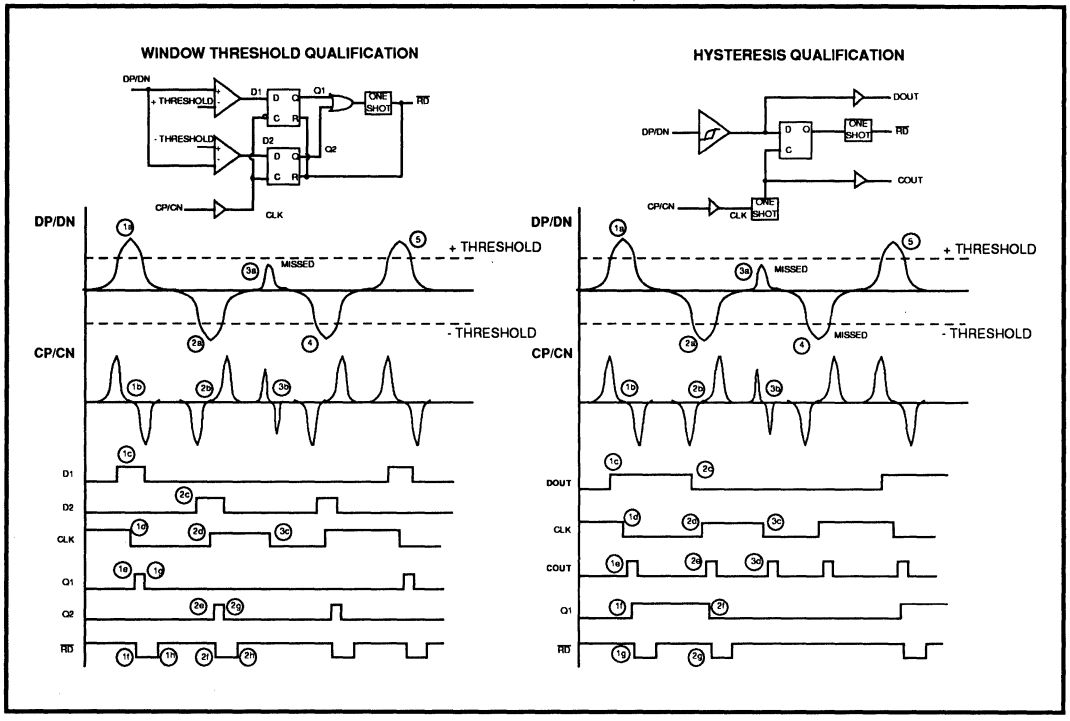



**FIGURE 4.1.3: Window Threshold Qualification & Hysteresis Qualification**

### Qualification Threshold Time Constant

Because the qualification threshold is set as a percentage of the pulse qualifier input's peak-to-peak swing, this threshold can track with any long term signal amplitude variation at the DP/DN input. An external R-C network, with an internal 50 µA pull down current source, from the LEVEL output to the RTD pin (or the RTS pin for servo mode) determines the tracking time constant.

There are two constraints in determining this R-C time constant:

- This time constant should not be too small such that the threshold may track the noise.
- This time constant should not be too large such that reasonably lower amplitude pulses are not qualified.

Both constraints are system dependent, specifically the head/media combination. The user must determine these limits. However, it is accurate to say that the time constant should be smaller than that of the AGC loop. Otherwise, the AGC loop will restore 1Vppd at the DP/DN input, and this defeats the purpose of the tracking threshold.

## 4.0 READ MODE EVALUATION (continued)

### 4.1 PULSE DETECTOR FUNCTION (continued)

#### 4.1.3 Pulse Qualifier Function (continued)

***Lab Experiment 4.1*: Pulse Detector Qualification Threshold Time Constant**

The SSI 32P4730 supports a tracking qualification threshold in pulse detection. Given a change in input signal amplitude, at a rate faster than the AGC loop can respond, the qualification threshold can remain as a fixed percentage of the signal level, if its time constant is set properly. This qual threshold time constant is determined by an external R-C network between the LEVEL pin and the RTD (or RTS) pin, with an internal 50 µA pull down current at the LEVEL pin. Because the LEVEL voltage 70 is the reference voltage for the internal 7-bit threshold setting DAC, the percentage change in (V@LEVEL - VRC) is the same as the qualification threshold voltage. The key point is then to allow the LEVEL 70 voltage to track with any change in signal amplitude with the two constraints discussed above.

For this experiment, the AGC time constant is made artificially large with a 0.01µF BYP capacitor. This is to suppress the AGC action to emphasis the qualification threshold time constant effects.

*What would happen if the qualification threshold time constant is too large?*

A 0.033µF capacitor is connected between the LEVEL pin and the VPA pin. The resistor is omitted, but the internal pull down current provides a discharge path. With 50 µA discharge current, the maximum decay rate at the LEVEL pin is 50 µA /0.033 µF = 1.52 mV/µs. Nominally, the LEVEL voltage is at 0.65V above the VRC voltage. Thus, the percentage change rate of the qualification threshold voltage is 1.52 / 650 x 100% per µs = 0.24%/µs. The actual qualification percentage change is then 0.24%/µs x Set Qual Level. If the qualification level is set at 50%, for example, the qualification percentage change rate is 0.12%/µs. If the DP/DN signal changes faster than this rate, the qualification threshold may not stay at 50% level.

Photo 4.1.1 shows the dynamic input signal, the LEVEL voltage and the $\overline{\text{RDIO}}$. The input signal changes gradually from 100 mVppd to 40 mVppd, and remains at 40 mVppd for 10 µs. The qualification level is set at 50%. Because of the large time constant, the LEVEL voltage does not track with the input amplitude. The qualification threshold remains at 50% of the larger input signal. As a result, the pulses of 40 mVppd are not qualified and missed. Photo 4.1.2 shows the same signal dynamics with a 330 pF capacitor from the LEVEL pin to the RTD pin.

*What would happen if the qualification threshold time constant is too small?*

To exaggerate the effects, no external capacitor, except parasitics from scope probe, is placed between the LEVEL pin and the VPA pin. The input signal has a sequence of 100 mVppd pulses, followed by a '0' period for 500 ns and two weak pulses of 20 mVppd. The qualification level is set at 50%. Should the threshold stay rigid, the two weak pulses would not be qualified. Because of the small time constant, the LEVEL voltage varies very rapidly with the instantaneous input signal. The qualification threshold drops very quickly. As a result, any weak pulses are qualified.

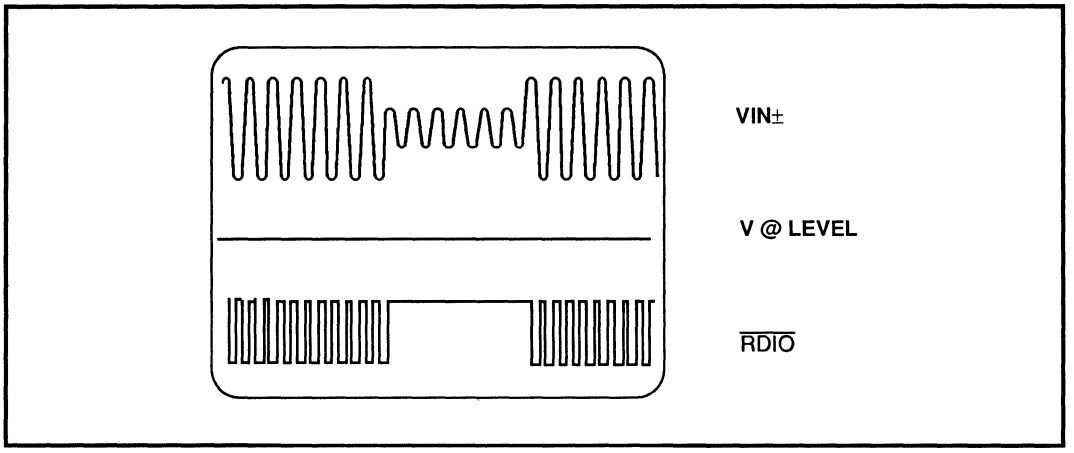



PHOTO 4.1.1: Qualification threshold at 50%; 0.033 μF from LEVEL to VPA. Input changes from 100 mVppd to 40 mVppd. Large qual threshold time constant >> Missing RDIO pulses.

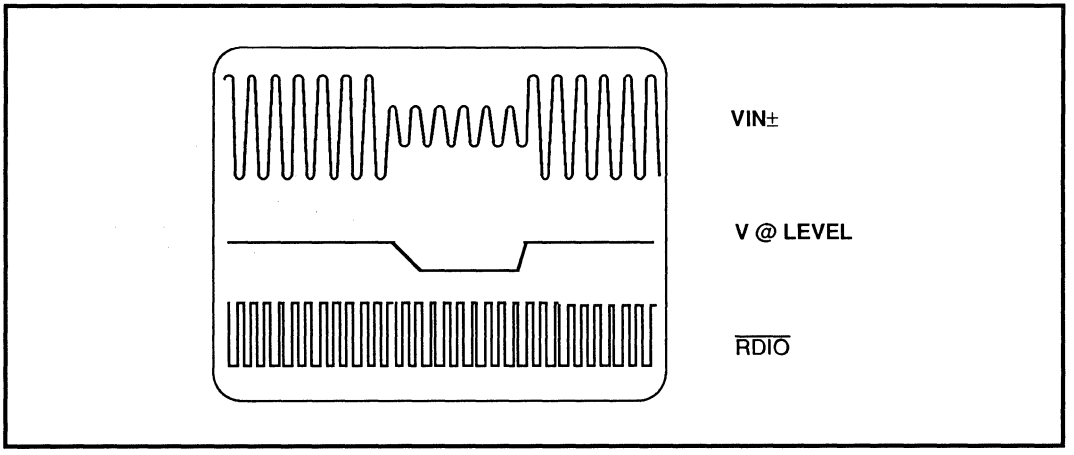



PHOTO 4.1.2: Qualification threshold at 50%; 330 pF from LEVEL to VPA. Input changes from 100 mVppd to 40 mVppd. Proper qual threshold time constant >> All RDIO pulses present.

## 4.0 READ MODE EVALUATION (continued)

### 4.1 PULSE DETECTOR FUNCTION (continued)

#### 4.1.4 Pulse Detector I/O & Test Points

An excellent troubleshooting aid is to know the inputs, the outputs and the available test points. For the pulse detector portion, this is a list of the related pins:

- VIA±
  Differential analog input to the AGC amplifier: The input should be ac-coupled from the source. The input amplitude should be limited to between 20 mVppd to 240 mVppd when no boost is applied at the filter. When boost is applied, the input amplitude should be lowered, as not to exceed the dynamic range of the AGC amplifier and the filter. The DC bias voltage is approximately 3.5V.
- VOA±
  Differential analog output of the AGC amplifier: The output should be ac-coupled to the the filter input. In a closed AGC loop, its amplitude depends on the filter cutoff and boost setting. The DC bias voltage is approximately 3.5V.
- BYP
  AGC amplifier gain control pin: The input voltage controls the AGC amplifier gain. An integrating capacitor should be connected from the BYP pin to VPG. This voltage should be between 2V to 3.5V.
- $\overline{\text{HOLD}}$
  TTL logic input: When $\overline{\text{HOLD}}$ = 0, the AGC amplifier gain is held constant. When $\overline{\text{HOLD}}$ = 1, or left open, the AGC loop is active.
- IN±
  Differential analog input of the filter: The DC bias voltage is approximately 3.5V. The VOA± should be ac-coupled to this input.
- ON±
  Differential normal low pass filter output: This output should be ac-coupled to the DP/DN input. It is simply the filtered version of the IN±. In a closed AGC loop, it should be ~ 1Vppd. The filter has a nominal gain of 2.0V/V in the passband. However, the gain can be higher at frequency where boost is applied. The DC bias voltage is approximately 2.3V.
- OD±
  Differential differentiated low pass filter output: This output should be ac-coupled to the CP/CN input. It is the bandlimited time differentiated version of the IN±. Every peak (positive or negative) is translated into a zero crossing. Its amplitude is frequency dependent. The DC bias voltage is approximately 2.3V.
- DP/DN
  Differential input to the pulse qualifier: The ON± should b e ac-coupled to this input. The DC bias voltage is approximately 3.6V.
- CP/CN
  Differential input to the time qualifier: The OD± should be ac-coupled to this input. The DC bias voltage is approximately 3.6V.
- PPOL
  Pulse polarity indicator: This is an optional TTL output indicating the polarity of the input pulse. A positive qualified pulse puts a logic '1' at the PPOL output. A negative qualified pulse puts a logic '0' at the PPOL output. This output is enabled when RG = WG = 0.
- MTP1-3
  Open emitter output test points: These test points are governed by the following logic control.

| Control B Reg D6 | Control A Reg D5 | D6 | MTP1 | MTP2 | MTP3 |
|---|---|---|---|---|---|
| 0 | 0 | X | 1 | 1 | 1 |
| 0 | 1 | X | 1* | 1* | 1* |
| 1 | 0 | 0 | VCO REF | DS-IN | DS REF |
| 1 | 0 | 1 | VCO REF | DS-IN | M CTR |
| 1 | 1 | 0 | RD | DOUT | COUT |
| 1 | 1 | 1 | SET | RESET | COUT |

VCO REF = reference input to the data synchronizer phase detector, VCO REF = VCO ÷ 2
DS-IN = input to data synchronizer
in read mode, this is the delayed read data
in non-read mode, this is the output of the time base generator ÷ 2
DS REF = reference frequency to the data separator, i.e. time base generator output (Active only in idle mode)
M CTR = time base VCO divided down signal, an input to the time base phase detector
RD = read data output of the pulse detector, i.e. input to the 1/3 cell delay
DOUT = output of the data comparator in hysteresis qualification
COUT = output of the clock comparator in hysteresis qualification
SET = output of the positive threshold comparator in window threshold qualification
RESET = output of the negative threshold comparator in window threshold qualification
1 = logic 1
1* = logic 1, but with slightly higher power dissipation

- $\overline{\text{RDIO}}$

  Read data I/O pin: This is a bi-directional TTL compatible pin. When *Control B Register* D2 = 1, the $\overline{\text{RDIO}}$ is an input pin for the data separator. When the *Control B Register* D2 = 0, the $\overline{\text{RDIO}}$ is an output pin. When this pin is configured as an output pin and both RG = WG = 0, the $\overline{\text{RDIO}}$ represents the pulse detector read data output. A pulse is generated for every qualified peak. With either RG or WG being 1, the $\overline{\text{RDIO}}$ is held at static 1.

- DACOUT

  Multiplexed DAC output: When *Window Shift Register* : D7-6 = 01, DACOUT represents the qualification threshold setting DAC output. The qualification threshold voltage can be estimated to be about TBD.

## 4.0 READ MODE EVALUATION (continued)

### 4.2 PROGRAMMABLE FILTER CHARACTERISTICS

The SSI 32P4730/31 features a on-chip programmable 7-pole 0.05° phase equiripple low pass filter / equalizer. This filter serves three functions: (1) noise limiting low pass filter of the read data signal, (2) time differentiating the read data signal for signal peak location, and (3) high frequency boost for pulse slimming equalization. The cutoff frequency, to be defined below, is programmable from 3 MHz to 9 MHz. The boost function can be programmed up to 13 dB. Both functions are controlled by command registers programmable via the serial interface.

The cutoff frequency, $fc$, is defined to be the -3dB bandwidth with no boost. When finite boost is applied, the effective -3 dB bandwidth is higher than the cutoff frequency. Table 4.2.1 lists the bandwidth increase vs the applied boost.

The high frequency boost is defined to be the amount of magnitude rise at the cutoff frequency, relative to the original -3 dB point. A 13 dB boost would mean a 10 dB peaking above the passband.

Figure 4.2.1 shows the normalized transfer function of the programmable filter. As a 0.05° phase equiripple filter, the group delay variation is minimal within the passband and up to ~ 2 x $fc$. One fact not denoted in the transfer function diagram is that the DIFF± output is delayed by 1.2 ns relative to the NORM±. This is to ensure sufficient data setup time for a flip-flop in the pulse qualifier.

An 1% 12.1 kΩ resistor and a 0.01 µF are needed from the RX pin to ground for filter biasing.

**TABLE 4.2.1: Filter Bandwidth Increase vs Boost**

| Boost (dB) | New -3dB Bandwidth / Cutoff Frequency | Boost (dB) | New -3dB Bandwidth / Cutoff Frequency |
|---|---|---|---|
| 0 | 1.00 | 7 | 2.42 |
| 1 | 1.21 | 8 | 2.51 |
| 2 | 1.50 | 9 | 2.59 |
| 3 | 1.80 | 10 | 2.66 |
| 4 | 2.04 | 11 | 2.73 |
| 5 | 2.20 | 12 | 2.80 |
| 6 | 2.32 | 13 | 2.86 |

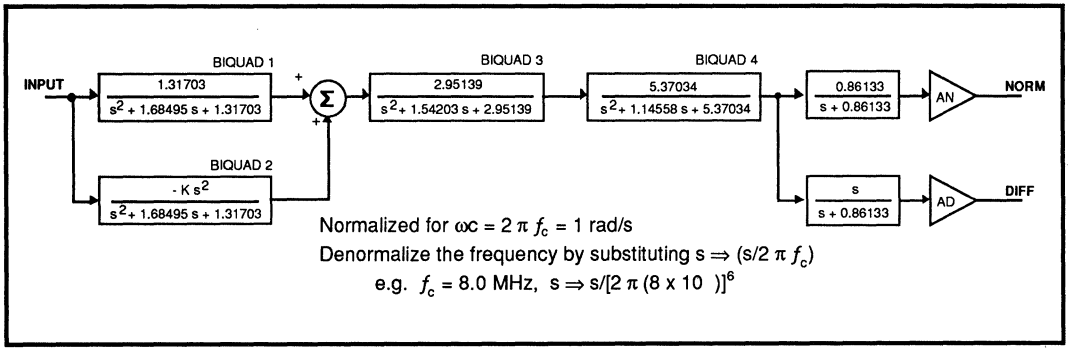



**FIGURE 4.2.1: Programmable Filter Normalized Transfer Function**
AN = 1.17 and AD = 1.51 for unity gain (0 dB) at 0.67 $fc$
K varies from 0 to 4.57 for boost up to 13 dB

### 4.2.1 Cutoff Control

For optimized signal-to-noise performance in a zoned recording application, the SSI 32P4730/3471 provides a programmable low pass filter. The filter cutoff frequency is programmable from 3 MHz to 9 MHz by the Fc DAC, an on-chip 7-bit DAC. In any non-servo mode, i.e. SG = 0, the Fc DAC is controlled by the *Data Mode Cutoff Register.* In the Servo mode, i.e. SG = 1, the Fc DAC is controlled by the *Servo Mode Cutoff Register.* This allows immediate bandwidth adjustment switching between data Read and Servo modes.

The filter cutoff frequency is determined as:
$fc$ (MHz) = 9 • Code / 127. In general, the cutoff frequency should be set to about the maximum signal frequency at the given data rate. However, the user should optimize the filter cutoff setting for a given head/media system combination.

### 4.2.2 Boost Control

For pulse slimming application, the programmable filter allows high frequency boost equalization. The filter boost is programmable from 0 to 13 dB by the Fb DAC, an on-chip 7-bit DAC. The Fb DAC is controlled by the lower 7 bits of the *Filter Boost Register.* In the Servo mode, i.e. SG = 1, the boost can be enabled / disabled by the MSB of this control register.

The filter boost is set as:
Boost (dB) = 20 log [(0.0273 • Code) + 1]. This boost setting should be optimized for lowest bit error rate for a given head/media system combination.

### 4.2.3 Programmable Filter I/O & Test Points

In troubleshooting the programmable filter, the following I/O and test points should be examined:

- IN±
  Differential analog input of the filter: The DC bias voltage is approximately 3.5V. The AGC amplifier output, VOA±, should be ac-coupled to this input.
- ON±
  Differential normal low pass filter output: This output should be ac-coupled to the DP/DN input. It is simply the filtered version of the IN±. In a closed AGC loop, it should be ~ 1 Vppd. The filter has a nominal gain of 2.0V/V in the passband. However, the gain can be higher at frequency where boost is applied. The DC bias voltage is approximately 2.3V.
- OD±
  Differential differentiated low pass filter output: This output should be ac-coupled to the CP/CN input. It is the bandlimited time differentiated version of the IN±. Every peak (positive or negative) is translated into a zero crossing. Its amplitude is frequency dependent. The DC bias voltage is approximately 2.3V.
- RX
  Reference resistor pin: An external 1% 12.1 kΩ resistor should be connected from this pin to ground. The voltage at this pin is proportional to absolute temperature. At room temperature ambient, this voltage is typically measured to be 700 mV.
- DACOUT
  Multiplexed DAC output: When *Window Shift Register* : D7-6 = 00, DACOUT = Fc DAC.

## 4.0 READ MODE EVALUATION (continued)

### 4.3 TIME BASE GENERATOR FUNCTIONALITY

The SSI 32P4730/4731 includes the time base generator to support the variable data rate in a zoned recording application. The data separator VCO requires a 3X data rate reference frequency (not to confuse with FREF, which is reference to the time base generator). Thus, for 24 Mbit/s operation, a 72 MHz reference is needed to the data separator. The time base generator provides such a stable reference frequency.

The SSI 32P4730/4731 time base generator is a phase locked loop based frequency synthesizer, Figure 4.3.1. If *Control A Register*: D4 = 0, the time base generator output, Fout, is made programmable by loading two divide-down factors achieving better than 1% resolution up to 75 MHz. If the *Control B Register*: D4 = 1, the frequency synthesizer is bypassed. The time base generator output is at the same frequency as FREF. FREF should be limited between 8 MHz to 20 MHz.

In the frequency synthesizer active mode, Fout = FREF • [(M + 1) / (N + 1)]. The N factor is a 7-bit code in the *N Counter Register*. The M factor is a 8-bit code in the *M Counter Register*. How do you determine the optimal N and M codes? The principle is to meet the frequency resolution requirement and to achieve the highest update rate for the phase detector. Figure 4.3.2 illustrates a flow chart to determine the M and N codes.

The M and N counters can be programmed anytime. However, they only become effective after a Data Rate Register programming. This is to reduce any transient condition for the phase locked loop in new data rate programming.

An external differential passive loop filter is need in the phase locked loop. This loop filter design allows design trade off between PLL settling time vs noise jitter performance. The differential architecture minimizes external noise pickup. The loop filter design details are presented in the next section.

#### 4.3.2 Time Base Generator Loop Filter Design

The SSI 32P4730/4731 requires a loop filter to control the PLL locking characterisitcs. While there are several types of filters that can be used to perform this function, a simple differential integrating filter, Figure 4.3.1, has proven to be very effective.

In designing the loop filter for the TBG PLL, two key considerations should be noted:

- PLL settling time
  In zoned recording application, the TBG output frequency must vary with data rate changes from one zone to another. When the *M Counter Register* is updated, the PLL would acquire and settle to the correct output frequency. This settling time should be less than the minimum track-to-track seek time.
- C1 capacitor must have low leakage.
  Typically, C1 should be selected to be less than 1.0 µF.

The loop filter bandwidth must be large enough for the PLL to settle fast. Yet, the time jitter performance is improved by a lower filter bandwidth. Thus, the bandwidth should only be large enough to meet the PLL settling time requirement.

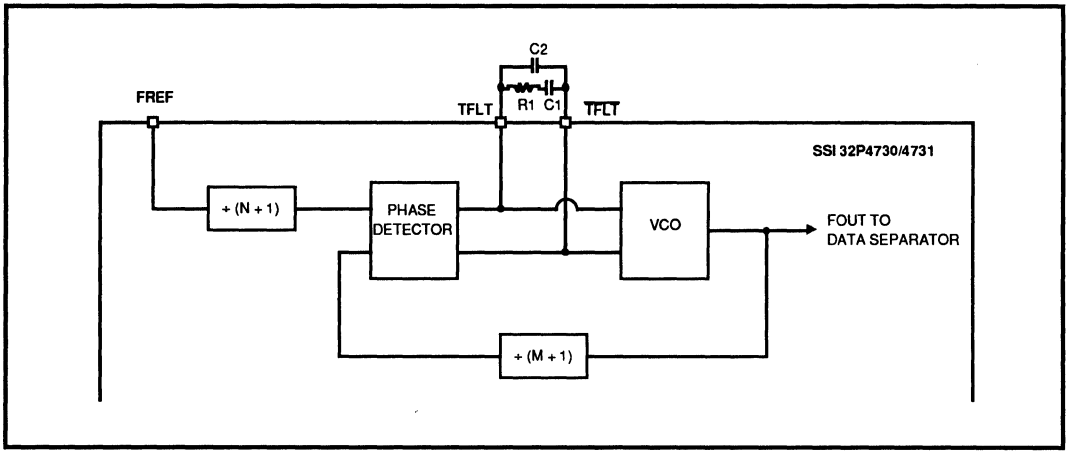



FIGURE 4.3.1: Time Base Generator Functional Model

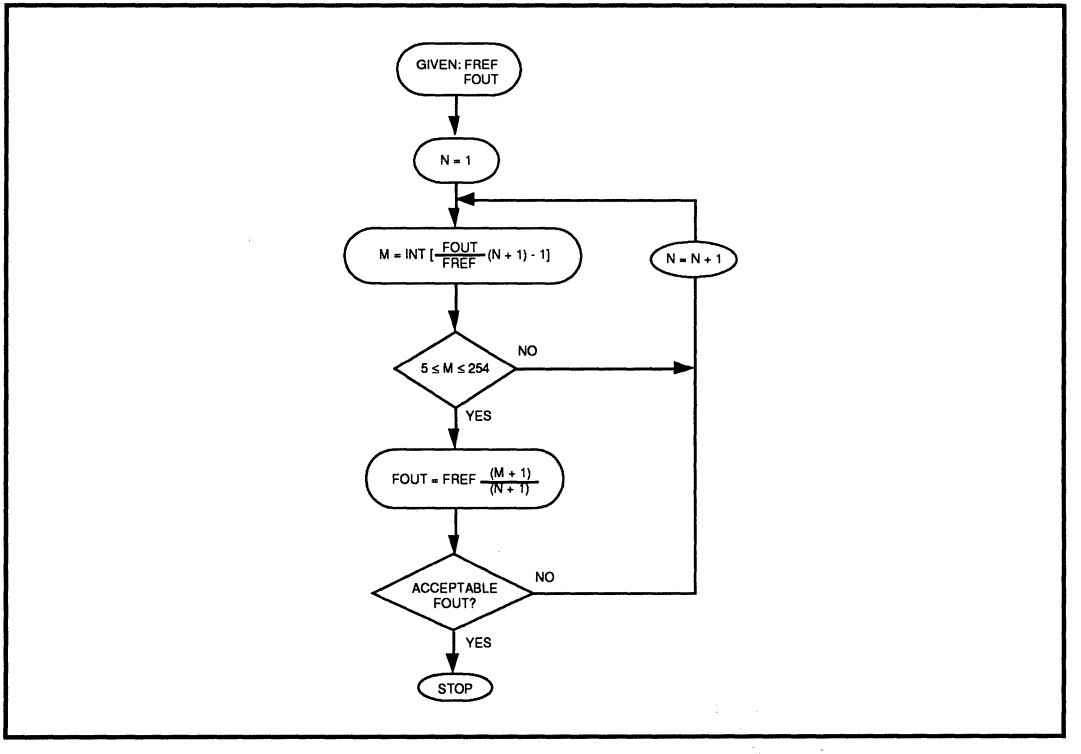



FIGURE 4.3.2: M & N Codes for Time Base Generator

## 4.0 READ MODE EVALUATION (continued)

### 4.3 TIME BASE GENERATOR FUNCTIONALITY (continued)

Figure 4.3.1 shows the functional model diagram. C2 is typically designed to be only one-tenth of C1, for high frequency noise shunt purpose. It may be neglected in the R1 and C1 design consideration. From second-order linear analysis, the loop response can be shown to be:

$I_{out} = KD \cdot (\theta_i - \theta_o)$ KD = Phase Detector Gain, $\theta_i$ = Reference input phase, $\theta_o$ = VCO output phase

$V_{VCO} = I_{OUT} \cdot F(s)$ F(s) = Loop Filter Transfer Function

$$\theta_o = \frac{KVCO \cdot V_{VCO}}{(M+1)} \frac{1}{s}$$ KVCO = VCO Gain

$$\frac{\theta_o}{\theta_i} = \frac{KVCO \cdot KD \cdot F(s)}{s + KVCO \cdot KD \cdot F(s)/(M+1)} \qquad F(s) = R_1 + \frac{1}{sC_1}$$

$$= \frac{KVCO \cdot KD \cdot (1 + s\,R_1C_1)/[C_1(M+1)]}{s^2 + s\,KVCO \cdot KD \cdot \frac{R_1}{(M+1)} + \frac{KVCO \cdot KD}{C_1(M+1)}}$$

Let the characteristic equation be written as:

$$\chi(s) = s^2 + 2s\,\zeta\,\omega_n + \omega_n^2 \qquad \omega_n^2 = \frac{KVCO \cdot KD}{C_1(M+1)} \qquad \zeta = \frac{KVCO \cdot KD \cdot R_1}{2(M+1)\omega_n}$$

The damping factor of 1.0 is employed thereby allowing the damping factor to drop as the frequency drops.

The acquisition time of the loop is set-up to accommodate a zero phase restart and allow for 1% maximum phase error after acquisition.

Refer to Figure 3 in Data Synchronizer Family Applications Notes in 1992 Data Book.

$\omega_n T = 5.2$

where T = settling time

From data sheet, KVCO = 0.17 $\omega_{vco}$rad/(V-sec), $\omega_{VCO} = 2 \times \pi \times$ Fout

KD = (0.6768 • DR-code + 3.4798) µA/rad; see latest specifications for accurate values

Design Example:

Assume a Data Rate of 24 MHz with a TBG reference FREF = 12 MHz

Choose N = 14 and M - 89 for an FOUT of 72 MHz

NOTE: The choice of N will decide the size of Capacitor $C_1$

KVCO = 76.9 Mrad / (V-sec)

KD = 76.5 µA / rad

Max settling time = 0.5 ms >> $\omega_v$ = 10.4 Krad / sec

| | |
|---|---|
| $C_1$ = 0.91 µF ; | $R_1$ = 212Ω |
| $C_2$ = 0.091 µF | |

In the following table, R C1 and C2 were chosen based on the maximum data rate. Wn and Psi are then re-calculated based on other data rate requirements and calculated loop filter component values.

| Zone | Data Rate | N | M | KD | KVCO | T | Wn | Psi |
|---|---|---|---|---|---|---|---|---|
| 0 | 24 | 14 | 59 | 76.5 | 76.5 | 0.5 | 10.4 | 1.0 |
| 1 | 20 | 14 | 49 | 63.0 | 64.1 | 0.55 | 9.4 | 0.90 |
| 2 | 16 | 14 | 39 | 50.2 | 51.2 | 0.62 | 8.4 | 0.81 |

#### 4.3.2 Time Base Generator Jitter Performance

Jitter performance is an important figure of merit for a time base generator. For a single-chip read channel device, jitter can degrade a drive system in two areas: (1) noisy reference clock to the data separator, and (2) write data clock instability. Because the data separator is re-trained and re-locked to the read data pattern, the former is not as critical as the latter.

One method to minimize the TBG output jitter is by limiting the TBG PLL loop filter bandwidth. However, the loop bandwidth must be wide enough to allow fast acquisition time.

The SSI 32P4730/4731 features very low output jitter. With the proper loop filter design, the SSI 32P4730/4731 rms jitter is specified as <130 ps. For design purposes, the time jitter six sigma would be + or - 400 ps.

#### 4.3.3 Time Base Generator I/O & Test Points

The SSI 32P4730/4731 Time Base Generator has only one input and one test point.

- FREF
  TTL frequency reference input: This input provides a reference input to the TBG PLL. It should be limited to between 8 MHz to 20 MHz. When the TBG is bypassed, as commanded by *Control A Register*: D4, the data separator PLL reference is that at the FREF input.
- MTP3
  This test point can be configured to monitor the data separator PLL reference clock.

### 4.4 DATA SEPARATOR FUNCTIONALITY

The SSI 32P4730/4731 Data Separator performs the following functions:

- Synchronization
- RLL 1,7 encode & decode
- Address mark generation & detection (for soft sector application)
- Preamble generation & detection
- Write pre-compensation
- Window shift adjustment

#### 4.4.1 Synchronization

For synchronization, the data separator has two objectives:

- Clock regeneration
- Encoded data syncrhonization

##### 4.4.1.1 Clock Regeneration

Because the data is coded with the clock signal, the clock must be regenerated for precise timing. For the SSI 32P4730/4731, the clock regeneration is accomplished with a phase locked loop comprised of a phase detector, a loop filter and a voltage controlled oscillator (VCO). The VCO runs at 3X the NRZ data rate. For 24 Mbit/s operation, the VCO should run at 72 MHz.

In the Idle mode, i.e. RG = WG = SG = 0, the VCO is phase & frequency locked to the time base generator output, Fout, which can be either a frequency synthesized signal or FREF (see Section 4.3). With the TBG output at 3X the NRZ data rate, the VCO is centered for a subsequent read / write cycle. The RRC is at the NRZ data rate, which is Fout ÷ 3.

## 4.0 READ MODE EVALUATION (continued)

### 4.4 DATA SEPARATOR FUNCTIONALITY (continued)

#### 4.4.1.1 Clock Regeneration (continued)

Entering into the Read mode, i.e. RG 0-to-1 transition, the phase detector reference input switches from the TBG output to the delayed read data, $\overline{DRD}$. A preamble pattern of 19 '3T' is used for training the VCO to phase-lock to the $\overline{DRD}$.

To reduce the initial phase error, the SSI 32P4730/4731 employs a zero-phase restart technique which, after 3 $\overline{DRD}$ transitions, halts the VCO momentarily until the 4th $\overline{DRD}$ transition is detected. The initial phase error is limited to below 2 ns of the decode window. For 24 Mbit/s operation, this represents ~ 7% error, or 0.45 radian.

In addition to the zero-phase restart, the SSI 32P4730/4731 also features phase detector gain shift, enabled by *Control B Register* : D1, to support fast phase acquisition. When phase detector gain shift is enabled, immediately following the read gate transition, the phase detector gain is 3X the nominal Idle mode phase detector gain. The PLL bandwidth is effectively increased by a factor of √3. The gain shift remains active until after the first 14'3T' patterns are detected. After the 14th '3T', the phase detector gain returns to the nominal value for improved jitter performance. The VCO continues to be trained by the remaining preamble pattern. After the first 19 '3T' patterns are detected, an internal VCO lock signal is asserted.

With the internal VCO lock asserted, the following two events are initiated:

- The RRC is now switched from Fout ÷ 3 to VCO ÷3. During this switching, the RRC may be held static for a maximum of 2 NRZ clock periods. However, the SSI 32P4730/4731 guarantees no glitch on the RRC.
- The data syncrhonizer decode window, to be defined in Section 4.4.1.2, boundaries are by the next two '3T' pattern.

When the phase detector gain shift is disabled, immediately following the read gate transition, the phase detector gain is 3X the nominal Idle mode phase detector gain. The PLL bandwidth is effectively increased by a factor of √3. The gain boost remains active throughout the read cycle.

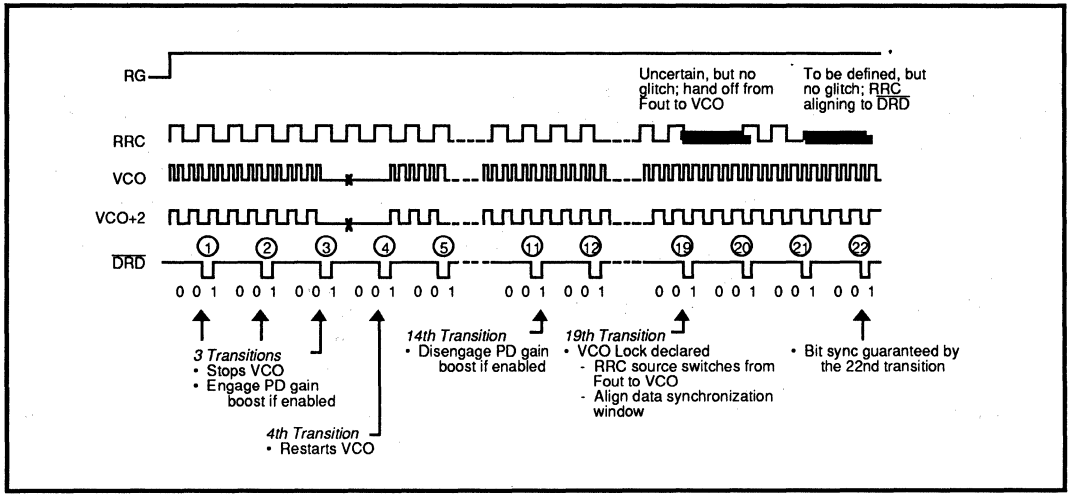



**FIGURE 4.4.1: SSI 32P4730/4731 Regeneration Process**

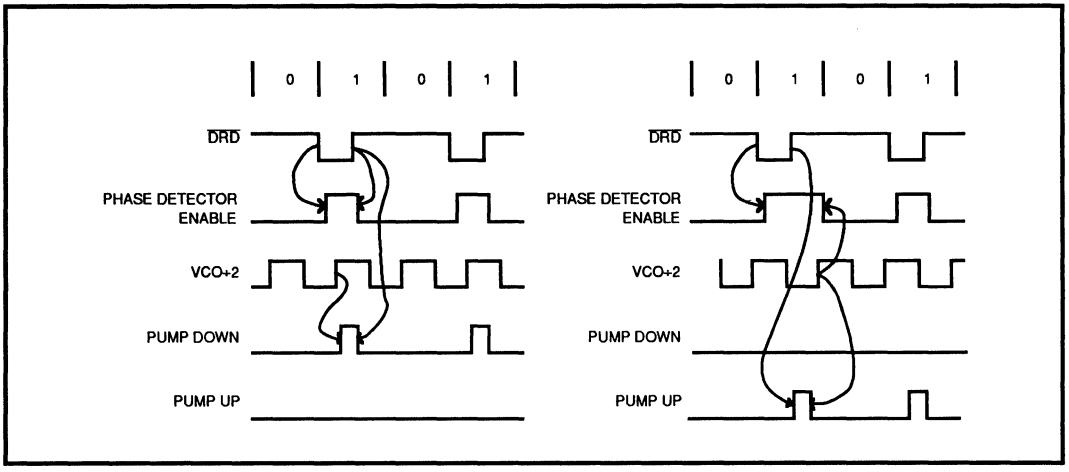



**FIGURE 4.4.2: SSI 32P4730/4731 Data Separator Phase Detector Data Locking Mechanism**

Figure 4.4.1 illustrates the clock regeneration process.

#### 4.4.1.2 Data Separator PLL & Phase Decode Window

In the Data Read mode, the VCO is locked to the $\overline{DRD}$ by phase comparing the VCO÷2 and $\overline{DRD}$. Each $\overline{DRD}$ pulse corresponds to a read data '1'. Its width is one-half of the encoded bit period. Its leading edge enables the phase detector. Its trailing edge is phase compared to the rising edge of VCO÷2. The VCO is then steered in the direction to correct the phase difference. After a phase comparison, the phase detector is disabled until the next leading edge of the $\overline{DRD}$.

An important concept in the working of data separator is the phase decode window. The phase decode window is the time span between two consecutive falling edges of the VCO÷2. In a locked condition, when the phase detector is enabled at the beginning of a phase decode window, the phase decode window is said to be perfectly centered. Should a $\overline{DRD}$ bit shift by up to half of VCO÷2 period in either direction, this $\overline{DRD}$ bit would still be phase compared with the proper VCO÷2 rising edge, Figure 4.4.3a. If the $\overline{DRD}$ pulse width is not matched to half of VCO÷2 period, the tolerance on bit shift is reduced. The $\overline{DRD}$ bit would be phase compared to the wrong VCO÷2 rising edge. Thus, a phase decode error would occur. It should be noted that a phase decode error would cause a transient disturbance on the VCO control voltage.

The SSI 32P4730/4731 features excellent matching between the $\overline{DRD}$ pulse width and the VCO period. Figure 4.4.4 shows some test data taken on this device.

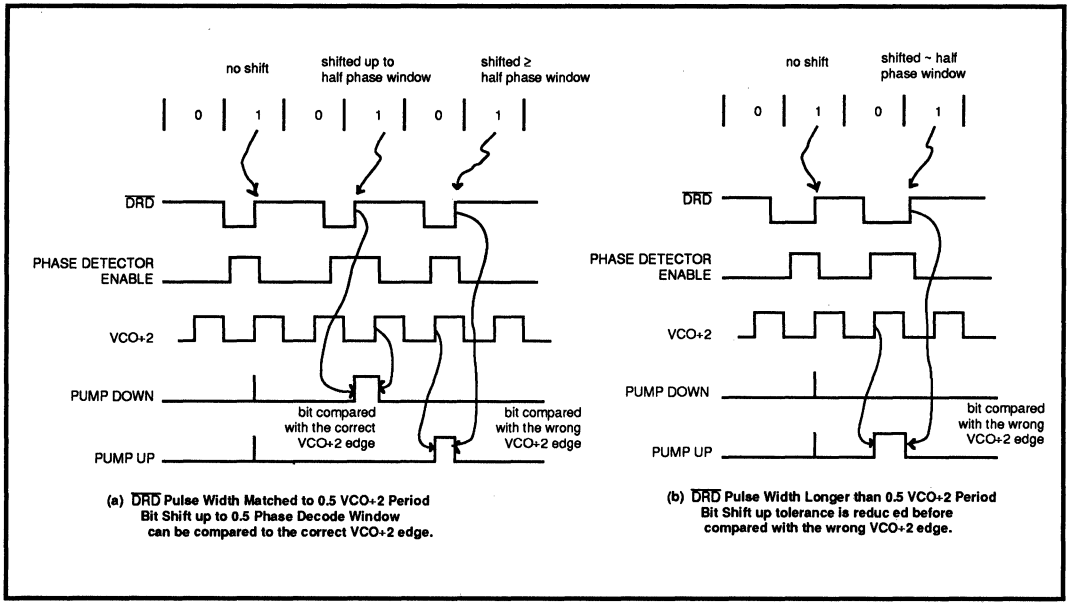



**FIGURE 4.4.3: SSI 32P4730/4731 Data Separator Phase Decode Window**
Asymmetry causes bit shift tolerance reduction.

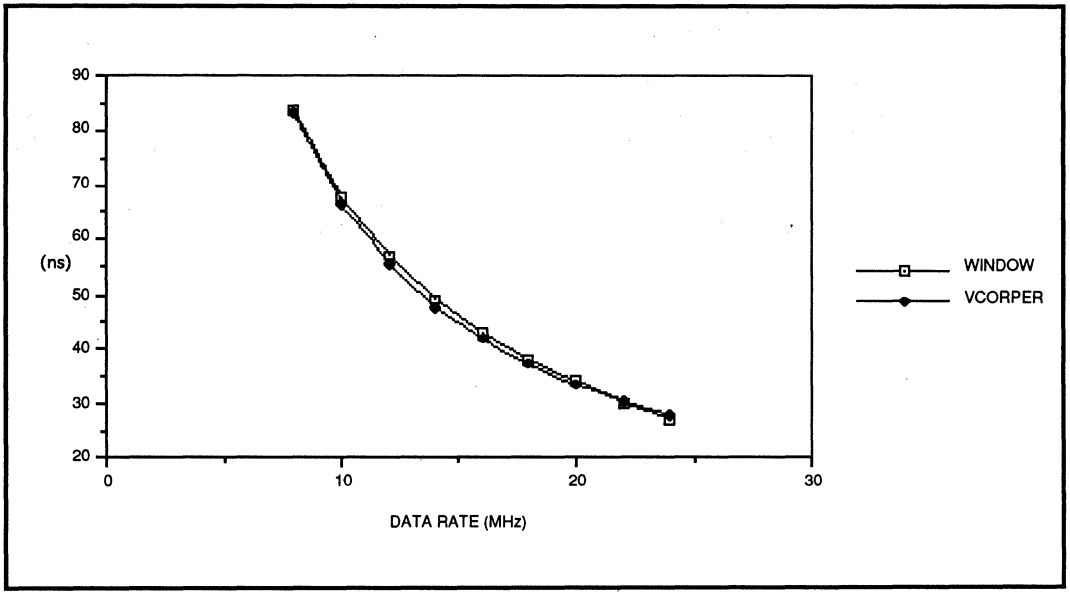



**FIGURE 4.4.4: SSI 32P4730/4731 1/3 Delay Cell & VCO Period Matching**

## 4.0 READ MODE EVALUATION (continued)

### 4.4 DATA SEPARATOR FUNCTIONALITY ( continued)

#### 4.4.1.3 Encoded Data Synchronization

With the clock extracted from the read data, the SSI 32P4730/4731 re-synchronizes the encoded data prior to the 1,7 Decoder. Figure 4.4.5 illustrates the timing function of the synchronization.

#### 4.4.1.4 Data Separator PLL I/O & Test Points

The following I/O & test points are helpful in trouble-shooting the data separator PLL:

- MTP1
  Open emitter output test point: it can be configured to monitor the VCO÷2 reference to the phase detector. See Section 4.1.4.
- MTP2
  Open emitter output test point: it can be configured to monitor the DRD input to the phase detector. See Section 4.1.4.
- MTP3
  Open emitter output test point: it can be configured to monitor the reference frequency to the data separator PLL in the idle mode. See Section 4.1.4.
- DFLT & $\overline{\text{DFLT}}$
  Differential VCO control pins: a differential loop filter is connected across these two pins. The common mode voltage at these two pins should be near 2.0V.
- RRC
  TTL read reference clock output: the RRC frequency should be at the NRZ data rate.

### 4.5 DATA SEPARATOR LOOP FILTER DESIGN

The SSI 32P4730/4731 data separator PLL requires a differential external loop filter. Again, the same integrating loop filter topology as for the Time Base Generator can be used. The loop filter bandwidth must be sufficient large for minimal phase error at the end of the VCO training pattern. However, the narrow bandwidth is desirable for noise & jitter rejection.

The SSI 32P4730/4731 features a high phase detector gain boost for fast phase acquisition, and yet narrower bandwidth in normal data read operation. While entering the read mode, the data separator PLL utilizes a zero-phase restart technique to minimize the initial phase error between the VCO & the $\overline{\text{DRD}}$ pulses. The initial phase error is 2 ns. For 24 Mbit/s operation, this corresponds to 0.45 rad phase error. The data separator PLL has 16 '3T' pattern period to lock onto the $\overline{\text{DRD}}$ pulses. Depending on system parameters, such as jitter expectation from the head / media combination, the user must decide the maximum acceptable final phase error at the end of the training sequence. The following presents a design example, with the phase detector gain shift disabled.

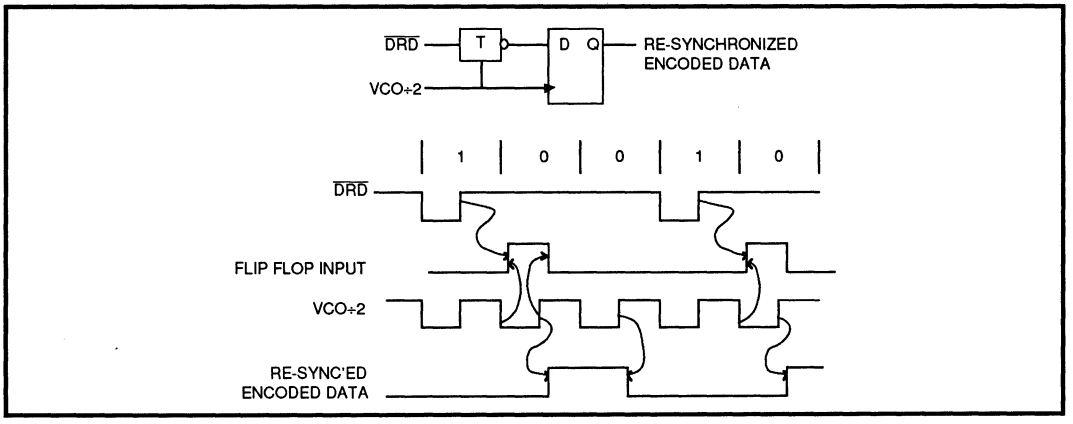



**FIGURE 4.4.5: Data Resychrnoziation Timing**

## 4.0 READ MODE EVALUATION (continued)

### 4.5 DATA SEPARATOR LOOP FILTER DESIGN (continued)

#### 4.5.1 Phase Detector Gain Shift Disabled

Assume max DR = 24 Mbit/s  Encode Bit Period = $\frac{1}{1.5 \times 24\ \text{MHz}} = 27.78$ ns

Sixteen '3T' pattern implies training time T= 16 • 3 • 27.78 ns = 1.33 µs

Let Z be the damping factor. It is set to 1.0 to allow a drop as the data rate increases.
Let the final phase error be less than 1% of maximum phase error.

From SSi 1992 Storage Data Book, page 4-211, Figure 2, $\omega_n T = 2.6$

Thus, $\omega_n = 3.91$ Mrad/s

It was shown in Section 6.6.1

$$\omega_n^2 = \frac{KVCO \cdot KD}{3\,C_1} \qquad Z = \frac{KVCO \cdot KD \cdot R_1}{2 \cdot 3 \cdot \omega_n}$$

From data sheet, KVCO = $0.17\ \omega_{vco}/2 = 0.17 \cdot \pi \cdot 72 = 38.5$ Mrad/(V-sec)
KD = (2.0304 • DR-code + 10.4394 = 229.7 µA/rad; see latest specifications for accurate values
DR Code = 108 for 24 Mbit/s

| | |
|---|---|
| $C_1$ = 192 pF ; | $R_1 = 2675\Omega$ |
| $C_2$ = 19 pF | |

In the following table, R C1 and C2 were chosen based on the maximum data rate. Wn and Psi are then re-calculated based on other data rate requirements and calculated loop filter component values.

| Zone | Data Rate | KD | KVCO | T | Wn | Psi |
|---|---|---|---|---|---|---|
| 0 | 24 | 229.7 | 38.5 | 1.33 | 3.9 | 1.0 |
| 1 | 20 | 189.1 | 32 | 1.61 | 3.23 | 0.828 |
| 2 | 16 | 150.5 | 25.6 | 202 | 2.58 | 0.66 |

### 4.6 1,7 RLL DECODE FUNCTION

The SSI 32P4730/4731 supports the 1,7 RLL encode & decode function. In the read mode, the encoded data from the read/write preamplifier is AGC amplified, pulse qualified, clock extracted and re-synchronized. The encoded data is then decoded back into the NRZ domain.

Because every three encoded bits are decoded into two NRZ bits, the leading bit of the three-bit frame must be defined. This is the bit synchronization. When the RG is asserted, nineteen 3T patterns must be detected prior to the internal VCO lock is asserted. After the internal VCO lock is asserted, the SSI 32P4730/4731 searches for three consecutive 3T patterns for bit synchronization. The bit immediately following the last '1' bit of the three 3T patterns is defined as the leading bit of a three-bit frame. The decode function follows Table 4.6.1.

The decoded NRZ data appears at the NRZOUT pin. A valid NRZ data bit is clocked out by a RRC falling edge. The controller should receive the NRZ data bit by RRC rising edge. The NRZOUT bit is guranteed to be present at least 13 ns before the RRC rising edge, and at least 13 ns after the same RRC rising edge.

In non-read mode, i.e. RG = 0, the NRZOUT is a tri-state high impedance pin. With the RG asserted, the NRZOUT is an output pin. Refer to the electrical specification for the delay time limits.

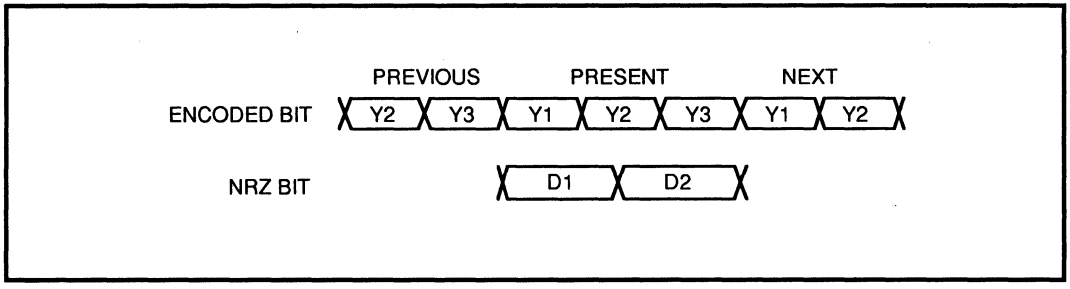



**FIGURE 14: Definition of Y1-3 & D1-2 for Decode Table**

## 4.0 READ MODE EVALUATION (continued)

### 4.7 ADDRESS MARK DETECT FUNCTION

The SSI 32P4730/4731 can support both hard sector and soft sector operations.

In hard sector operation, the AMENB pin is held to logic '0' and the $\overline{AMD}$ output is in tri-state high impedance mode. The read cylce is initiated with the RG assertion. No address mark detection is necessary.

In soft sector operation, the address mark must be detected before the RG is asserted to continue a read cycle. With the AMENB asserted to logic '1', the SSI 32P4730/4731 initiates the address mark search. An address mark pattern should consist of two 8T patterns followed by two 12T patterns. The address mark detect circuitry searches for six consecutive 0's followed by nine consecutive 0's. After the six consecutive 0's are detected, the nine-0 pattern must be detected within five encoded '1' bits are detected. If no nine consecutive 0 pattern is detected before the fifth encoded '1' bit is detected, the address mark search resets and looks for the six consecutive 0's again. If the nine consecutive 0's are detected, the $\overline{AMD}$ output is pulled to logic '0' until the AMENB is released. The RG should be asserted after $\overline{AMD}$ is pulled low. Figure 4.7.1 illustrates a timing example in the soft sector read mode.

### 4.8 WINDOW SHIFT FUNCTION

The SSI 32P4730/4731 allows the user to perform window margin testing with the window shift function. If the synchronization window is well centered without loss, the window can be theorectically shifted up to 50% in each direction. The window shift function is accomplished via a digital delay circuit which can delay the $\overline{DRD}$ with respect to the VCO÷2, or vice versa. Figure 4.8.1 illustrates the window shift function.

By programming the *Window Shift Register*, the synchronization window can be shifted up to 15% in either direction. The lower 4 bits, D3..D0, sets the amount of window shift. D4 determines the window shift direction. D5 enables the window shift function.

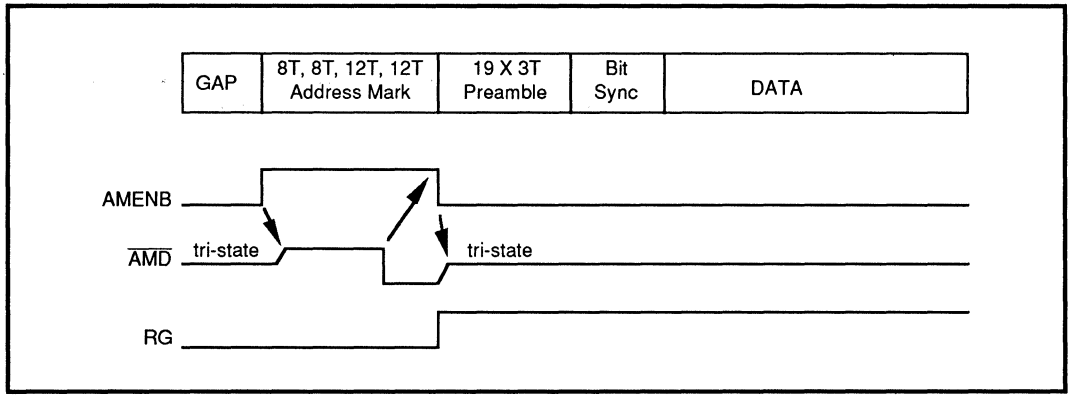
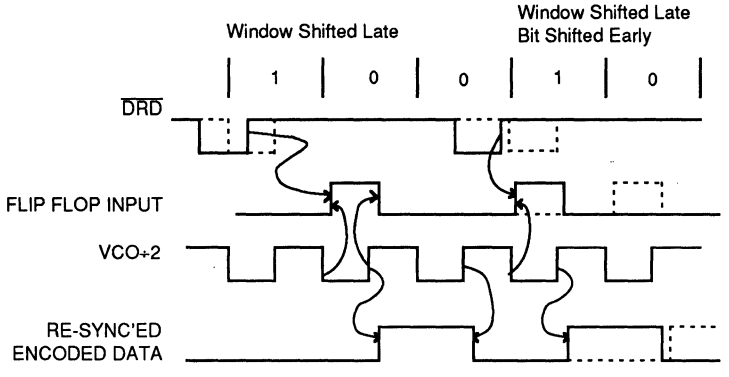
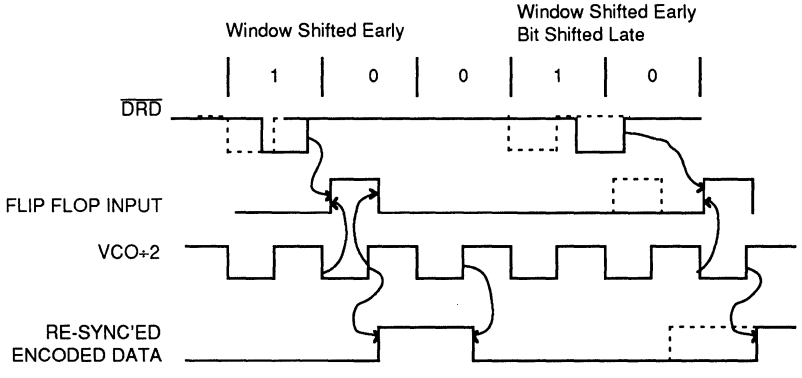



**FIGURE 4.7.1: Read Mode Soft Sector Timing**




(a) WINDOW SHIFTED LATE




(b) WINDOW SHIFTED EARLY

**FIGURE 4.8.1: Window Shift Function Illustration**

## 5.0 SERVO MODE EVALUATION

The SSI 32P4730 and 32P4731 both support 4 burst servo capture function. Four internal peak capture 10 pF capacitors are used to sample the 4 servo bursts. While all other functions are identical between the two devices, the two devices offer different servo capture schemes.

For both the P4730 and the P4731, the servo mode is initiated by asserting the servo gate. With a 0-to-1 SG transition, the following events occur:

- the AGC control enters the fast decay (gain increase) for 1.0 µs,
- the programmable filter cutoff freqeuncy is set according to the *Servo Mode Cutoff Register*,
- the programmable filter boost is enabled / disabled according to the MSB of the *Filter Boost Register*,
- the pulse qualification method and percentage are set according to the *Servo Threshold Register*,
- the qualification threshold time constant is switched to the RTS pin, and
- the AGC functions will regulate the DP/DN signal to the prescribed level according to the *Servo AGC Level Register*.

Because the servo signal and the data rate signal are typically of different frequency, the filter bandwidth can be set independent from the data mode. Likewise, the boost function can be enabled or disabled. The pulse qualification percentage, method and time constant are also set independent from the Data mode.

Immediately following the SG 0-to-1 transition, the device enters the fast decay mode for 1.0 µs. A servo preamble pattern is expected to allow the AGC to regulate the DP/DN signal level, which is programmable from 0.77 Vppd to 1.0 Vppd via the *Servo AGC Level Register*. The $\overline{\text{HOLD}}$ should be pulled to logic '0' after the servo AGC preamble.

The control sequence after the servo preamble pattern differs between the 32P4730 and 32P4731.

### 5.1 SSI 32P4730 SERVO

The SSI 32P4730 features A+B, A-B and C-D servo outputs. Other input controls for the Servo mode include $\overline{\text{RESET}}$, LATCH0, LATCH1, STROBE and reference input (SREF).

The $\overline{\text{RESET}}$ input, when pulled to logic '0', the four internal peak capture capacitors are discharged and reset. All outputs are expected to be at the voltage as the SREF, which should be between 1.0V to 3.0V. The $\overline{\text{RESET}}$ input can be active without SG activated.

Each burst channel is designated by LATCH1 and LATCH0 as following:

- LATCH1, LATCH0 = 0, 0 Burst Channel A
- LATCH1, LATCH0 = 0, 1 Burst Channel B
- LATCH1, LATCH0 = 1, 0 Burst Channel C
- LATCH1, LATCH0 = 1, 1 Burst Channel D

The amplified, filtered and full-wave rectified servo signal is peak captured onto an internal hold capacitor, designated by LATCH1 and LATCH0, when STROBE = '1'. When STROBE = '0', the full-wave rectified output is disconnected from all internal hold capacitors. It is recommended that STROBE returns to '0' before LATCH1/0 change state for next burst channel.

The voltage gain from the DP/DN to the internal hold capacitors is 1.0 Vop/Vppd. For example, a 0.4 Vppd DP/DN signal yields 0.4V (relative to a given reference bias). The P4730 outputs are defined as:

- A + B = DP/DN @ Burst A + DP/DN @ Burst B + SREF
- A - B = DP/DN @ Burst A - DP/DN @ Burst B + SREF
- C - D = DP/DN @ Burst C - DP/DN @ Burst D + SREF

All DP/DN voltages are peak-to-peak differential.

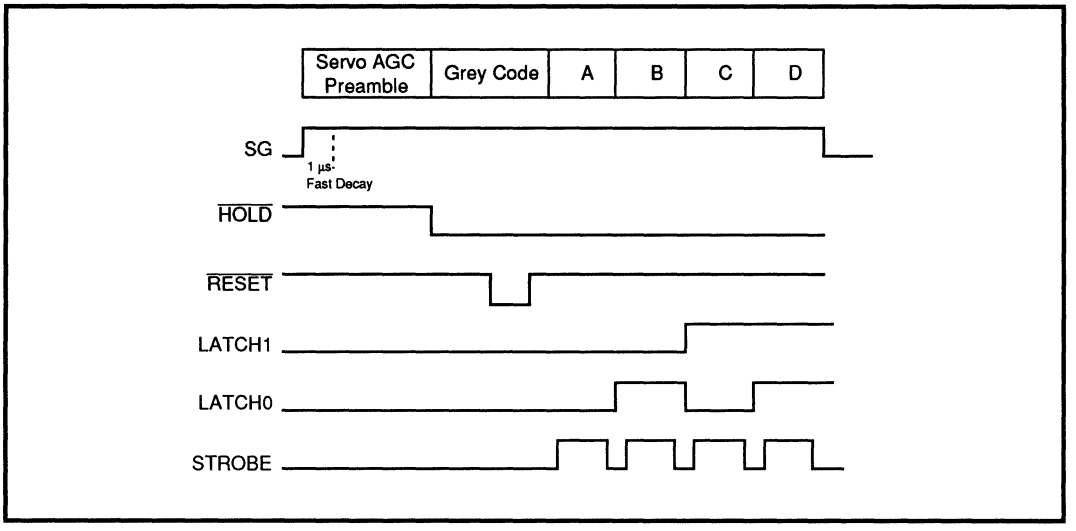



**FIGURE 5.1.1: SSI 32P4730 Servo Control Sequence**

### 5.2 SSI 32P4731 SERVO

The SSI 32P4731 features individual servo burst outputs: Bursts A, B, C and D. Other input controls for the servo mode include $\overline{\text{RESET}}$, STROBE. A reference output voltage is available, MAXREF, which should be always higher than the maximum possible Bursts A, B, C and D voltage when DP/DN = 1Vppd.

The $\overline{\text{RESET}}$ input, when pulled to logic '0', the four internal peak capture capacitors are discharged and reset. All outputs are expected to be at 0.5V. The $\overline{\text{RESET}}$ input can be active without SG activated.

There is no burst channel address bit needed for P4731. With the $\overline{\text{RESET}}$ pulled to logic 0, the internal counter is pre-set for Burst Channel A. With the first falling edge on the STROBE input, the counter is advanced to Burst Channel B. Another falling edge advances the counter to Burst Channel C. Another falling edge advances the counter to Burst Channel D.

The amplified, filtered and full-wave rectified servo signal is peak captured onto an internal hold capacitor when STROBE = '1'. When STROBE = '0', the full-wave rectified output is disconnected from all internal hold capacitors.

The voltage gain from the DP/DN to the Bursts A, B, C and D outputs is 2.25 Vop/Vppd. For example, a 0.4 Vppd DP/DN signal yields 0.9V (relative to a given reference bias). The 32P4731 burst output is:

- Burst X = DP/DN @ Burst X • 2.25 + 0.5 V

The DP/DN voltage is peak-to-peak differential.

### 5.3 SERVO DIGITAL OUTPUTS

To support the servo timing, the SSI 32P4730/31 have two TTL digital outputs: $\overline{\text{RDIO}}$ and PPOL.

$\overline{\text{RDIO}}$

This pin must be configured as an output for this utility. In the servo mode, a 10 ns pulse is generated for each qualified peak. This output is disabled, pulled to static '1', when either RG or WG is at logic 1.

PPOL

When RG and WG are both logic 0, this output represents the polarity of the peak being qualified. A logic 1 indicates a positive peak. A logic 0 indicates a negative peak.

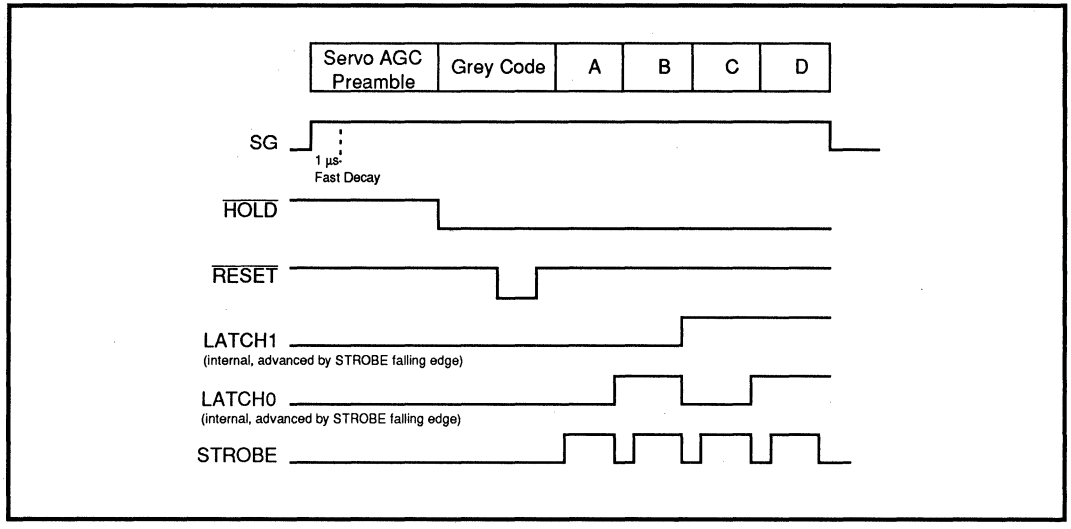



**FIGURE 5.2.1: SSI 32P4731 Servo Control Sequence**

## 6.0 WRITE MODE EVALUATION

In the write mode, the SSI 32P4730/4731 converts the NRZIN data into 1,7 RLL encoded data. Write mode is entered by asserting the write gate, WG, while the read gate, RG, is held to logic 0. In soft sector operation, the circuit generates an address mark and a preamble pattern. In hard sector operation, the circuit generates the preamble pattern without preceding address mark. The NRZIN data is clocked into the encoder at each WCLK rising edge. The encoded data appears at the $\overline{WD}$ output pin which feeds a write driver. The data separator PLL and the RRC are locked onto the time base generator output.

The $\overline{WD}$ is an active low signal. When an encoded '1' bit is to be written, a low pulse of 0.67 encoded bit period occurs at the $\overline{WD}$ output.

### 6.1 ADDRESS MARK GENERATION

The address mark generation is only applicable to soft sector operation. One NRZ period after the WG 0-to-1 transition, the AMENB is asserted for at least 1 NRZ period and at most 27 NRZ period. The address mark pattern of two 8T's followed by two 12T's is automatically generated. With the NRZIN input kept at logic '0', 3T patterns are generated to follow the address mark pattern. From the WG 0-to-1 transition, the NRZIN input should be kept at logic '0' for at least 65 (for hard sector, at least 38) NRZ periods to ensure the complete preamble & bit sync pattern is written.

At the end of the NRZ data stream, at least five additional NRZ bits are recommended before the WG returns to logic 0.

### 6.2 WRITE PRECOMPENSATION FUNCTION

The SSI 32P4730/31 supports a programmable write precompensation function, which can be enabled by *Write Precomp Register*: D3 = 1. The device examines the bit pattern to determine the write precomp direction as governed in Table 6.2.1.

The 3 LSBs of the *Write Precomp Register* programs the amount of write precompensation as integral multiple (up to 7X) of 4% of encoded bit period. For example, a precomp magnitude of 16% of the encoded bit period is given by setting *Write Precomp Register*: D2-0 = 011.

The write precomp function is bypassed in the direct write mode, see Section 6.4.

**TABLE 6.2.1: Write Precompensation Direction**

| Bit N-2 | Bit N-1 | Bit N | Bit N+1 | Bit N+2 | Bit N Precomp Direction |
|---|---|---|---|---|---|
| 1 | 0 | 1 | 0 | 1 | None |
| 0 | 0 | 1 | 0 | 0 | None |
| 1 | 0 | 1 | 0 | 0 | Early |
| 0 | 0 | 1 | 0 | 1 | Late |

Late = Bit N is shifted toward Bit N+1; Early = Bit N is shifted toward Bit N-1

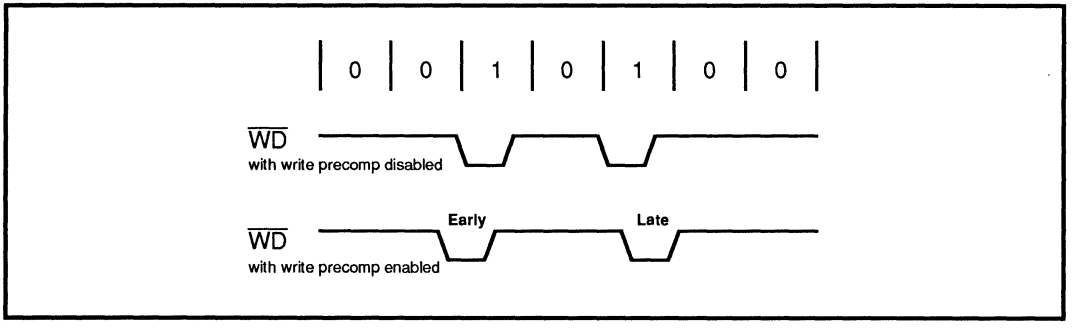



**FIGURE 6.2.1: Write Precomp Effect on $\overline{WD}$**

## 6.0 WRITE MODE EVALUATION (continued)

### 6.3 1,7 RLL ENCODE FUNCTION

The SSI 32P4730/31 converts the NRZIN data into 1,7 RLL encoded bits as given in the data sheet endode table.

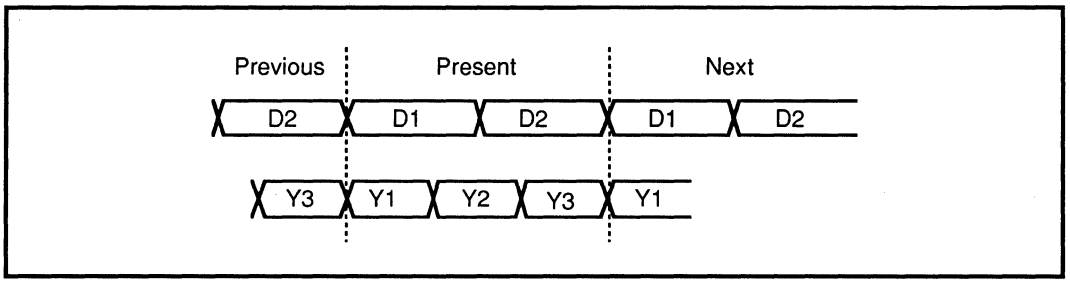



**FIGURE 8.3.1: Definition of Y1-3 & D1-2 in Encode Table**

The write data output, WD, is synchronized to the internal synthesized clock which can be asynchronous relative to the WCLK input. In the bit stream of the NRZ input, every two NRZ bits are paired together and encoded into three 1,7 RLL code bits. The pairing of the NRZ bits can be one of two combinations which, for discussion purposes, are termed as odd-even pair and even-odd pair. The odd-even pair and the even-odd pair will be encoded into different 1,7 RLL code bits. However, in the decode process, both pairings will result in the same NRZ pattern with a possible extra leading '0' bit. While a controller will re-frame the NRZ data, this does not create any problem in a system application.

Consider the following NRZ bit pattern: $0AD340_{HEX}$ = 00101011010011010000

The two possible NRZ pairings are:

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| odd-even pair - | 00 | 10 | 10 | 11 | 01 | 00 | 11 | 01 | 00 |
| even-odd pair - | 01 | 01 | 01 | 10 | 10 | 01 | 10 | 10 | 00 |

The encoded bits are:

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| odd-even pair - | 010 | 010 | 010 | 100 | 001 | 010 | 100 | 001 | 001 |
| even-odd pair - | 000 | 001 | 000 | 010 | 101 | 000 | 010 | 101 | 001 |

### 6.4 DIRECT WRITE FUNCTION

The SSI 32P4730/4731 supports the direct write function by setting *Control B Register*: D0 = 1. In the direct write mode, the 1,7 RLL encoder and the write precompensation are bypassed in the write mode. The NRZIN data is buffered and appears at the $\overline{WD}$.

This is an abridged applications note for the SSI 32P473014231, a more detailed note is available upon request. Design notes and evaluation techniques are suggested when applicable. This note is intended to supplement the device specification. For updated device parameter limits, the user is recommended to refer to the specification.

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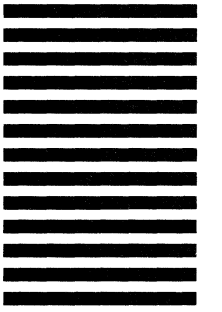

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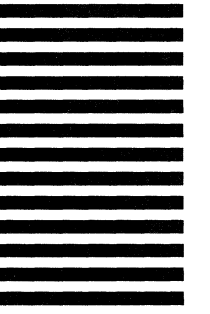

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