FIRST CLASS
CAR-RT SORT

INTEGRATED CIRCUITS FOR

STORAGE PRODUCTS

1994 DATA BOOK

silicon systems®
A TDK Group Company

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1994 Data Book

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Contents

Target, Advanced and Preliminary Information
In this data book the following conventions are used in designating a data sheet "Target," "Advanced" or "Preliminary":

Target Specification–
The target specification is intended as an initial disclosure of specification goals for the product. Product is in first stages of design cycle.

Advance Information–
Indicates a product still in the design cycle, undergoing testing processes, and any specifications are based on design goals only. Do not use for final design.

Preliminary Data–
Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

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Discontinued Parts List

The following parts are no longer supplied or supported by Silicon Systems.

32C4650
32C4651
32C9342
32D4010
32D4420
32F8000
32H101
32H116A
32H523AR
32H566R
32H4631/4632
32P3010
32P4620/4622
32P4731
32P5411B
32P546
32P548
32P549
32P5481
32R1200R
32R1220/21/22
32R2015R
34B580
34D441
34R575

STORAGE PRODUCTS REFERENCE

Device Number	Head Type	Number of Channels	Max Input Noise (nV/√Hz)	Max Input Capacitance (pF)	Read Gain (typ)	Write Current Range (mA)	Power Supplies (V)	Write Data Ports	Min. Head Swing (V)
READ/WRITE AMPLIFIERS									
SSI 32R117/117R	3 Terminal	2, 4, 6	2.1	20	100	10 to 50	+5, +12	TTL	8.0 (0-pk)
SSI 32R501/501R	3 Terminal	4, 6, 8	1.5	23	100	10 to 50	+5, +12	TTL	7.5 (0-pk)
SSI 32R510A/510AR	3 Terminal	2, 4, 6	1.5	20	100	10 to 40	+5, +12	TTL	7.0 (0-pk)
SSI 32R511/511R	3 Terminal	4, 6, 8	1.5	20	100	10 to 40	+5, +12	TTL	7.0 (0-pk)
SSI 32R516	3 Terminal	4, 6, 8	1.3	18	120	10 to 60	+5, +12	TTL	7.0 (0-pk)
SSI 32R5161R	3 Terminal	10	1.3	18	150	10 to 60	+5, +12	TTL	7.0 (0-pk)
SSI 32R512/512R	2 Terminal	8, 9	0.85	35	150	10 to 40	+5, +12	TTL	7.0 (pk-pk)
SSI 32R5121/5121R	2 Terminal	14	0.85	35	250	10 to 40	+5, +12	TTL	7.0 (pk-pk)
SSI 32R524R	2 Terminal	8	0.75	60	100	20 to 60	+5, +12	TTL	7.0 (pk-pk)
SSI 32R528R	2 Terminal	8, 9	0.85	35	150	10 to 40	+5, +12	Differential	7.0 (pk-pk)
SSI 32R5281	2 Terminal	14	0.85	35	250	10 to 40	+5, +12	Differential	7.0 (pk-pk)
SSI 32R1510BR	MR	8	0.95	18	150	20 to 50	+5, +12	Differential	8.0 (pk-pk)
SSI 32R1530	MR	10					+5, -1		
SSI 32R1540	MR	4,6					+5, -4.5		
SSI 32R1560	MR	8					+5, -3		
SSI 32R2010R/2011R	2 Terminal	10	0.84	26	150	10 to 25	+5, +12	Differential	7.0 (pk-pk)
SSI 32R2020R/2021R	2 Terminal	2, 4, 10	0.8	20	300	5 to 35	+5	TTL	4.2 (pk-pk)
SSI 32R2024	2 Terminal	4	0.75	22	150, 200, 300	5 to 40	+5	TTL	4.2 (pk-pk)
SSI 32R2025	2 Terminal	4	0.75	22	300	5 to 35	+5	TTL	4.2 (pk-pk)
SSI 32R2026	2 Terminal	4	0.75	22	300	5 to 35	+5	TTL	4.2 (pk-pk)
SSI 32R2030A/2031A	2 Terminal	2, 4	0.85	35	250	10 to 35	+5	TTL	3.4 (pk-pk)
SSI 32R2041	2 Terminal	4, 6	0.8	22	250	10 to 40	5, 12	ECL	7.0 (pk-pk)
SSI 32R2060	2 Terminal	8	0.75	22	150	5 to 35	+5	TTL	4.2 (pk-pk)
SSI 32R2063/64/65	2 Terminal	4	0.75	22	150, 200	3 to 40	+5	TTL/ECL	4.2 (pk-pk)
SSI 32R2100	2 Terminal	10	0.70	18	250	5 to 40	+5, +12	ECL	10.0 (pk-pk)
SSI 32R2110	2 Terminal	24	0.70	18	250	5 to 40	+5, +12	ECL	10.0 (pk-pk)
SSI 32R2112	2 Terminal	20	0.70	18	150	5 to 40	+5, +12	ECL/TTL	10.0 (pk-pk)
SSI 32R2200/2201	2 Terminal	4, 6	0.70	18	250	3 to 35	+5	ECL/TTL	6.0 (pk-pk)
SSI 32R2300/2300R/2310	2 Terminal	4	0.75	20	200	3 to 25	+3.3/+5	TTL	3.4 (pk-pk)
SSI 32R2320R/2420R	2 Termianl	2,4	0.75	20	200	3 to 35	+3.3/+5	ECL/TTL	3.4 (pk-pk)
SSI 32R4610A/4611A	2 Terminal	2, 4, 8	0.85	35	200	10 to 35	+5	TTL	3.4 (pk-pk)

STORAGE PRODUCTS REFERENCE

Device Number	Circuit Function	Features
DISCRETE CHANNEL		
SSI 32D5321	Data Separator	Data Synchronizer / 2, 7 RLL ENDEC 7.5 to 10 Mbit/s
SSI 32D5322	Data Separator	Data Synchronizer / 2, 7 RLL ENDEC 7.5 to 13 Mbit/s
SSI 32D534A	Data Separator	Data Synchronizer / MFM ENDEC / Write Precompensation
SSI 32D5351A	Data Separator	Data Synchronizer / 2, 7 RLL ENDEC / Write Precompensation 8 to 18 Mbit/s
SSI 32D5362A	Data Separator	Data Synchronizer / 1, 7 RLL ENDEC / Write Precompensation 10 to 20 Mbit/s
SSI 32D5371/2	Data Separator	Data Synchronizer / 1, 7 RLL ENDEC / Write Precompensation 12 to 24 Mbit/s
SSI 32D5373/4	Data Separator	Data Synchronizer / 1, 7 RLL ENDEC / Write Precompensation 15 to 32 Mbit/s
SSI 32D539	Data Separator	Data Synchronizer / 1, 7 RLL ENDEC / 8-bit parallel NRZ 24 to 48 Mbit/s
SSI 32D5391/2/3	Data Separator	Data Synchronizer / 1, 7 RLL ENDEC / Serial NRZ 24 to 40 Mbit/s
SSI 32D4660/1/2/3/4/5/6	Time Base Generator	Up to 100 MHz Reference Frequency PLC for Constant Density Recording
SSI 32D4680	Time Base Generator	Up to 120 MHz, 1% Frequency Resolution
SSI 32P541	Read Data Processor	AGC, Amplitude & Time Pulse Qualification, RLL Compatible
SSI 32P541B	Read Data Processor	32P541 pin compatible, 32P541A w/ Increased Data Rate to 24 Mbit/s
SSI 32P541C	Read Data Processor	32P541 pin compatible, 32P541A w/ Increased Data Rate to 24 Mbit/s
SSI 32P544	Pulse Detector	32P541-type Pulse Detector w/ Embedded Servo Electronics
SSI 32P547	Pulse Detector	32P544-type Pulse Detector w/ Filter Multiplexer, Pulse Slimming Support
SSI 32P5491	Read Data Processor	32P549 pin compatible, 5 mW Idle Mode power, Pd = 170 mW
SSI 32P3000/3001	Pulse Detector / Programmable Filter	64 Mbit/s Pulse Detector w/9-27 MHz Bessel filter (3000), 8-24 MHz filter (3001), +5V only
SSI 32P3013	Pulse Detector / Programmable Filter	48 Mbit/s Pulse Detector w/9-27 MHz Bessel filter, 4-burst servo capture
SSI 32P3015/3016	Pulse Detector / Programmable Filter	64 Mbit/s Pulse Detector w/9-27 MHz Bessel filter, 4-burst servo capture, adjustable RD pulse width
SSI 32P3030/31	Pulse Detector / Servo Demodulator	Pulse Detector w/2-burst servo demodulator, +5V only
SSI 32P3040/41	Pulse Detector / Programmable Filter	24-32 Mbit/s Pulse Detector w/2.5-13 MHz Bessel filter, +5V only
READ CHANNEL COMBINATION DEVICES		
SSI 32P548	Pulse Detector / Data Synchronizer	32P544-type w/ 2, 7 Synchronizer, Low Power, +5V only, <700 mW
SSI 32P5482	Pulse Detector / Data Synchronizer	Low power 32P548-type device (350 mW), no Write Precompensation
SSI 32P4740/41	Complete Read Channel	4730 with 14 to 40 Mbit/s operation, A-B/C-D Servo
SSI 32P4742/42A	Complete Read Channel	4731 with 16 to 48 Mbit/s, Dual-bit NRZ, A-B/C-D Servo
SSI 32P4746/46A	Complete Read Channel	4730 with 16 to 48 Mbit/s, Dual-bit NRZ
SSI 32P4901	PR4, ML Read Channel	Parital Response, Maximum Likelihood channel, 24 to 72 Mbit/s, Dual-bit NRZ
PROGRAMMABLE FILTERS		
SSI 32F8001/8002	Low Power Programmable Electronic Filter	7-Pole Equiripple Active Filter, Programmable Cutoff Frequency / Pulse Slimming, 9 - 27 MHz (8001), 6-18 MHz (8002)
SSI 32F8003	Programmable Electronic Filter	7-Pole Equiripple Active Filter, Programmable Cutoff Frequency / Pulse Slimming, 5 - 13 MHz
SSI 32F8011/8012	Programmable Electronic Filter	7-Pole Bessel Active Filter, Programmable Cutoff Frequency / Pulse Slimming, (5 - 13 MHz, 8011) (6-15 MHz, 8012)
SSI 32F8020/8022	Low Power Programmable Electronic Filter	7-Pole Equiripple Active Filter, Programmable Cutoff Frequency / Pulse Slimming, 1.5 - 8 MHz
SSI 32F8030	Programmable Electronic Filter	7-Pole Equiripple Active Filter, Programmable Cutoff Frequency / Pulse Slimming, 250 kHz - 2.5 MHz
SSI 32F8101	Low Power Digitally Programmable Filter	8001 w/Serial Port & DACs, 95 mW
SSI 32F8102	Low Power Digitally Programmable Filter	8002 w/Serial Port & DACs, 95 mW
SSI 32F8103	Low Power Digitally Programmable Filter	8003 w/Serial Port & DACs, 95 mW
SSI 32F8104	Low Power Digitally Programmable Filter	Similar to 8103, Fc range 3-9 MHz

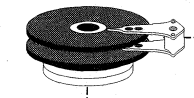
STORAGE PRODUCTS REFERENCE

Device Number	Circuit Function	Features
PROGRAMMABLE FILTERS (continued)		
SSI 32F8120	Low Power Digitally Programmable Filter	32F8020 with serial port and DACs
SSI 32F8130/31	Low Power Digitally Programmable Filter	32F8030 with serial port and DACs / 32F8131 = 150 kHz < fc < 1.5 MHz
SSI 32F8144	Low Power Digitally Programmable Filter	2 zero/7-pole linear phase filter, 7-bit serial shift register, 7-27 MHz
HEAD POSITIONING		
SSI 32H569	Servo Motor Driver	Head parking, spindle motor braking
SSI 32H4633	Combo Servo & Motor Speed Control	Embedded & hybrid servo, Hall sensorless motor speed control, 5400 RPM
SSI 32H6110	Preamplifier -Thin Film head	AV = 250 or 300, BW = 20 MHz, e_n = 0.85 nV/√Hz
SSI 32H6210	Servo Demodulator	Di-bit quadrature servo pattern; PLL synchronization AGC adjustment
SSI 32H6215	Servo 5V Demodulator	5V, 500 kHz frame rate dedicated servo demodulator
SSI 32H6220	Servo Controller	Track & seek mode operation; microprocessor interface
SSI 32H6230/31	Servo Motor Driver	Head parking, spindle motor braking, voltage clamp
SSI 32H6240	Servo Motor Driver	Predriver for bipolar H-bridge
SSI 32H6510	Servo 5V Driver	Low voltage retract, 1Ω drivers
SSI 32H6520	Servo Acquisition and D/A	10-bit A/D D/A circuits, DSP interface
SSI 32H6521	Embedded Servo Controller	10-bit A/D converter, 2.5 µs digital delay, DSP interface
SSI 32H6810/6810A/B	Servo/Spindle 5V Driver	Combo driver supports 5V @ 1.0A, voltage IN
SSI 32H6811/11B	Servo/Spindle 5V Driver	Combo driver supports 5V @ 1.0A, voltage IN, serial port with DACs
SSI 32H6812	Servo/Spindle 5V Driver	10-bit D/A converter, serial DSP interface
SSI 32H6814	Servo/Spindle 5V Driver	10-bit D/A converter, serial DSP interface
SSI 32H6820	Servo/Spindle 12V Driver	Servo head positioning and motor speed control
SSI 32H6825	Servo/Spindle 12V Driver	Window comparator, uncommitted opamp, reduced power dissipation
SSI 32H6830	Servo/Spindle DSP Controller	DSP with 10-bit A/D & dual D/A converters
SPINDLE MOTOR CONTROL		
SSI 32M593A	3-Phase Motor Speed Control	±0.037% speed accuracy; bipolar operation, 5 1/4" drives
SSI 32M594	3-Phase Motor Speed Control	±0.037% speed accuracy; bipolar operation, 3 1/2" & 5 1/4" drives
SSI 32M595	3-Phase Sensor-less MSC	Hall sensorless; motor speed control
SSI 32M7010	Motor Speed Control 5V Driver	Hall sensorless; commutator digital speed control, 5V 1Ω driver
SSI 32M7011	Motor Speed Control 5V Commutator	Hall sensorless; commutator, 5V 1Ω driver

STORAGE PRODUCTS REFERENCE

Device Number	Circuit Function	Features
CONTROLLER/INTERFACE		
SSI 32C9001	ATA Combo Controller	48 Mbit/s; High Performance ATA Disk Controller
SSI 32C9003	High Perf. ATA Combo Controller	72 Mbit/s; LBA mode; Automated multi commands
SSI 32C9020	High Perf. SCSI Combo Controller	48 Mbit/s; SCSI-2 compatible; Fast SCSI; single ended
SSI 32C9022	Dual-bit High Perf. SCSI Combo Controller	Dual-bit NRZ, 48 Mbit/s; SCSI-2 compatible; Fast SCSI
SSI 32C9023	Dual-bit High Perf. SCSI Combo Controller	Dual-bit NRZ, 72 Mbit/s; SCSI-2 compatible; Fast SCSI
SSI 32C9024	Dual-bit High Perf. SCSI Combo Controller	Dual-bit NRZ, 72 Mbit/s; SCSI-2 compatible; Fast SCSI; Differential
SSI 32C9301	High Perf. ATA Combo Controller (3V, 5V)	32 Mbit/s (3V), 48 Mbit/s (5V); LBA mode support
SSI 32C9302	Dual-bit High Perf. ATA Combo Cont. (3V, 5V)	Dual-bit NRZ, 48 Mbit/s; LBA mode support
SSI 32C9340	Dual-bit PCMCIA/ATA Combo Controller (3V, 5V)	Dual-bit NRZ, 48 Mbit/s (3V/5V); 256 byte CIS
SSI32C9600	ATA-2 Controller	Dual-/8-bit NRZ; 160 Mbit/s; ATA/ATA-2 Compatible; Wide Buffer; Advanced Reed-Solomon ECC
SSI 32C9800	SCSI-3 Controller	Dual-/8-bit NRZ; 160 Mbit/s; SCSI -2/SCSI -3 Compatible; Fast and wide; Advanced Reed-Solomon ECC
FLOPPY DISK DRIVES		
SSI 34P553/5531	Pulse Detector/Data Synchronizer	0.6 - 1.6 Mbit/s data rate, MFM or 2, 7 RLL code
SSI 34P3200	Pulse Detector/Data Synchronizer	250K - 6 Mbit/s
SSI 34P3201	Pulse Detector/Data Synchronizer	250K - 8 Mbit/s
SSI 34R1203R	5V, 2-, 4-Channel, 3-Terminal R/W	Selectable gain, 250 V/V and 85 V/V
OPTICAL DISK DRIVES		
SSI 33P3700	Magneto Optical Read Channel	Pulse detector/filter/time base generator/data synchronizer, 8-48 Mbit/s
SSI 33P3733/3734	Read Channel, No ENDEC	Pulse detector/filter/time base generator/data separator, 8 - 26.5 Mbit/s
SSI 33P3733A	Read Channel, No ENDEC	33P3733 with MO pit qualifier
TAPE DRIVES		
SSI 34P553/5531	Pulse Detector/Data Synchronizer	0.6 - 1.6 Mbit/s data rate, MFM or 2, 7 RLL code
SSI 34P3200	Pulse Detector/Data Synchronizer	250K - 6 Mbit/s
SSI 34P3201	Pulse Detector/Data Synchronizer	250K - 8 Mbit/s

WINCHESTER DISK DRIVE IC PRODUCT FAMILY



MOTOR SPEED CONTROL (MSC) & HEAD POSITIONING

MSC

SSI 32M593A
SSI 32M594
SSI 32M595
SSI 32M7010
SSI 32M7011

HEAD POSITIONING

SSI 32H569
SSI 32H4631
SSI 32H4633*
SSI 32H6210
SSI 32H6215
SSI 32H6220
SSI 32H6230
SSI 32H6240
SSI 32H6510
SSI 32H6520
SSI 32H6521

MSC & HEAD POSITIONING

SSI 32H6810A/B
SSI 32H6811/B
SSI 32H6812
SSI 32H6814*
SSI 32H6815*
SSI 32H6820*
SSI 32H6825*
SSI 32H6826*
SSI 32H6830

READ/WRITE

3-TERMINAL
SSI 32R117
SSI 32R117A
SSI 32R1200
SSI 32R501
SSI 32R510A
SSI 32R511A
SSI 32R516
SSI 32R5161
SSI 32R1220

MR HEAD PREAMP
SSI 32R1510BR

2-TERMINAL
SSI 32R512
SSI 32R5121
SSI 32R524
SSI 32R528
SSI 32R2010
SSI 32R2020/21
SSI 32R2024
SSI 32R2025
SSI 32R2026
SSI 32R2030/31A
SSI 32R2041
SSI 32R2060
SSI 32R2063/64/65
SSI 32R2100*
SSI 32R2110*
SSI 32R2200/2201*
SSI 32R2300/10/20
SSI 32R5281A

SERVO PREAMP

SSI 32H6110

PULSE DETECTOR

SSI 32P3000
SSI 32P3001
SSI 32P3013
SSI 32P3015
SSI 32P3030
SSI 32P3040/41
SSI 32P4720/1*
SSI 32P541
SSI 32P541B
SSI 32P544
SSI 32P547
Combo - SSI 32P548
SSI 32P5482
Combo - SSI 32P549/5491
Combo - SSI 32P4730
Combo - SSI 32P4741
Combo - SSI 32P4742
Combo - SSI 32P4744
Combo - SSI 32P4745
Combo - SSI 32P4746*
Combo - SSI 32P4750*
Combo - SSI 32P4752*
Combo - SSI 34P553/5531

ACTIVE FILTER

SSI 32F8001
SSI 32F8002
SSI 32F8011/12
SSI 32F8020/20A
SSI 32F8030
SSI 32F8101/2/3/4
SSI 32F8120
SSI 32F8130/31
SSI 32F8144*

DATA RECOVERY

SSI 32D4040/41*
SSI 32D4660
SSI 32D4661
SSI 32D4662
SSI 32D4664
SSI 32D4665
SSI 32D4666
SSI 32D5321
SSI 32D5322
SSI 32D534A
SSI 32D535
SSI 32D5351
SSI 32D5362A
SSI 32D5371
SSI 32D5372
SSI 32D5373
SSI 32D5374
SSI 32D539
SSI 32D5391
SSI 32D5392
SSI 32D5393
SSI 32D5396/96A

CONTROLLER

SSI 32C9001
SSI 32C9003
SSI 32C9020
SSI 32C9022
SSI 32C9023
SSI 32C9024
SSI 32C9301
SSI 32C9302
SSI 32C9340*
SSI 32C9600*
SSI 32C9800*

µP

RAM

** New or In Development*

Section 1

CUSTOM SOLUTIONS

SILICON SYSTEMS LEADS THE WAY DEVELOPING MIXED-SIGNAL CUSTOM PRODUCTS.

This is a story about leadership. Silicon Systems is dedicated to taking the point in the creation of high-performance, application-specific custom, mixed-signal integrated circuits (MSICs®).

Such dedication means we bring a lot to the party. Including truly innovative analog, digital, and mixed analog/digital ICs. A full complement of mixed-signal CMOS, BiCMOS and Bipolar wafer fabrication processes, state-of-the-art automated design tools, production, assembly, test, and QA capability.

No one's more experienced

More than 20 years of successful IC design work makes us the most experienced engineering team in the MSICs field. Add it all up and you get a company that saves you time and money while delivering you the most sophisticated mixed-signal custom ICs you can get.

Faster to market for mixed-signal applications

Whatever your mixed-signal design application, Silicon Systems gives you a competitive advantage. In communications, disk drives, other storage products, automotive control systems, or other analog/digital signal processing applications, you can depend on our technical know-how to do the job right and turn your design around faster.

CMOS. Bipolar. BiCMOS. Analog. Digital. We've done it

Our designers are an experienced bunch. They're uniquely able to take a look at your specific application problem and move quickly to the right IC solution.

Our team is particularly adept at identifying key issues such as power, cost and performance trade-offs. So we can gear our efforts toward delivering you an optimized solution, manufactured with the appropriate fab process.

Technique	Application	Silicon Systems Designed Examples
CMOS Analog Processing	For analog continuous time, samples data (switched-capacitor implementation), and high-current power transistor applications. Low power, high density capability also allows inclusion of ROMs, RAMs, and other analog/digital subsystems.	• Complete single-chip 2400 bit/s modem • 14.4 kbps modem chip set • Direct-broadcast satellite descrambler • Servo and spindle motor controllers with 1.0 Amp motor interfaces • High-resolution analog data acquisition • Cellular baseband processor
BiCMOS Signal Processing	For high-performance, low noise, wideband signal acquisition and processing applications. Offers TTL and/or ECL logic interfaces with high current drive.	• Sub 1 nV/√Hz HDD R/W amplifiers • AGC, pulse detection amplifiers • High-speed data separators • Wideband transceivers • PLLs (phase locked loops) • Optical signal processing • Digital cellular, PCS IF circuits
Digital CMOS	For ASIC controllers, digital signal processors, sequencers and data path applications with on-board ROM, RAM, and PLA sub-systems. Offers standard TTL and/or CMOS logic interfaces.	• Digital communications LAN devices • Hard disk drive controllers • SCSI interface controllers • UARTs • Digital signal processors for hard disk servo and telecommunications

The right mix of analog and digital

Providing total analog/digital systems on a chip allows you to meet your cost and performance objectives whether you're designing the next generation of communication, computer peripheral, or industrial control systems.

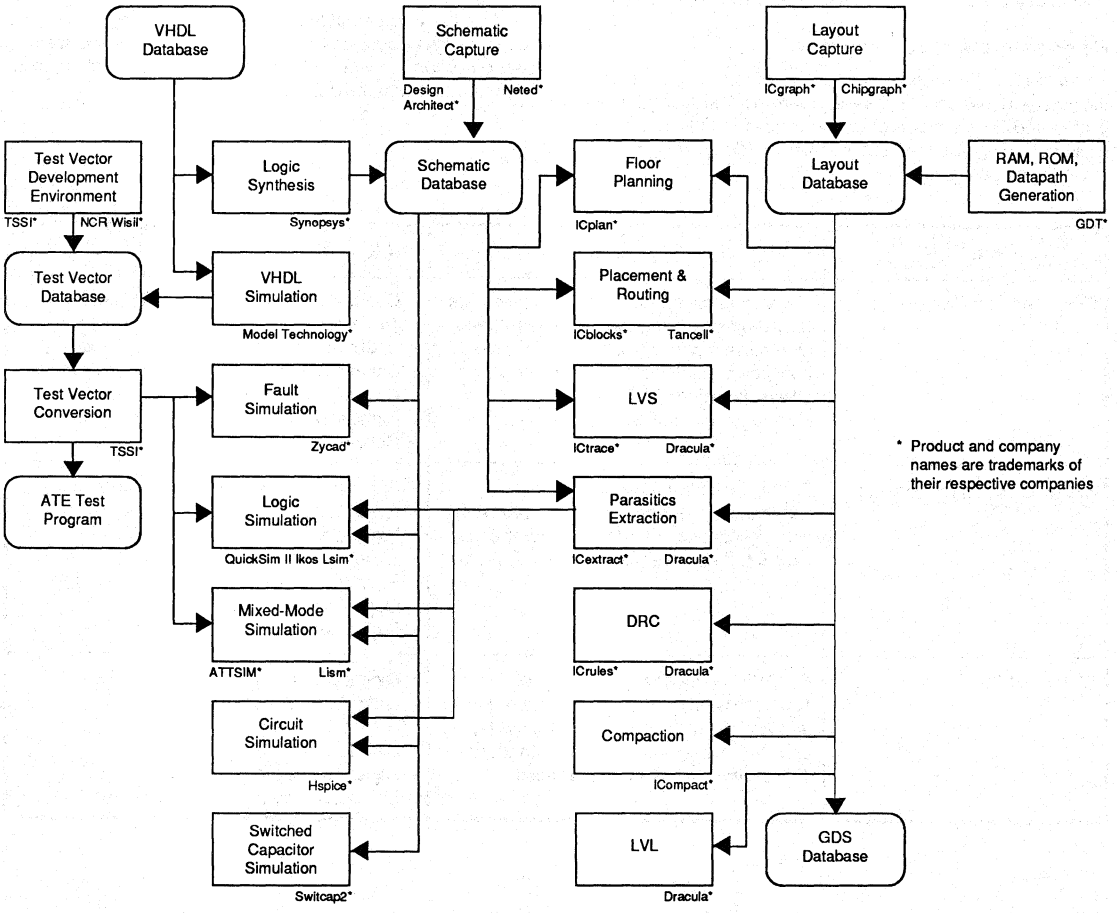
We've turned to CMOS to effectively implement low-power, highly integrated systems solutions for everything from modems and cellular phones to hard disk drive controllers and digital signal processors.

We've gone the BiCMOS route to meet the high-performance needs of products like wideband transceivers, wireless IF modems, R/W amplifiers, low-noise amplifiers, pulse detectors, high-speed data separators and high-performance, low-power combo devices.

SOPHISTICATED TOOLS FOR STRUCTURED CUSTOM DESIGN

At each of five design centers capable of worldwide service — Tustin, San Jose and Nevada City, California; Tokyo and Singapore — Silicon Systems employs PEGASYS, an internal design automation system developed from carefully selected vendor tools and our own proprietary software. Using Mentor Graphics workstations for both electrical and physical design, PEGASYS helps create complex designs while significantly reducing schedules, costs and errors.

By integrating third-party tools and custom software, we're better able to design and analyze mixed-signal integrated circuits in all CMOS, Bipolar and BiCMOS technologies. It's an approach that has given us the edge in mixed-signal design and helped put Silicon Systems' customers in a favorable position in the marketplace.



PEGASYS Design System

Specifically, PEGASYS brings the following to each design:

- Fully integrated design environment
- Methodology for precision circuit design
- Integrated electrical and physical design
- Unique blend of full-custom and automated layout techniques
- Complete layout verification
- Full mixed-signal parasitic extraction

Our design automation staff integrates the third-party tools and optimizes their use on the Mentor platform. This framework can easily accommodate new tools when needed, and it enables us to support a combination of analog and digital design techniques in all CMOS, Bipolar and BiCMOS chip designs. By mixing design methodologies, we can achieve optimum systems performance, even when schedules are tight.

Electrical design

A single CAE (computer aided engineering) environment provides for schematic capture, synthesis, simulation, and fault grading. We support this software with extensive libraries of pre-designed cells and components. Highly specialized cells or components can be designed and enhanced where required. We simulate each circuit to meet precise performance specifications using:

- Analog circuit simulation
- Digital logic simulation
- VHDL simulation
- Mixed-mode simulation
- Switched-capacitor filter simulation
- Analog and mixed-mode behavioral simulation

Admittedly, simulation alone is not the key to perfecting performance. That's why we work aggressively to refine our understanding of models to make them work with simulation. Inside our progressive device modeling and characterization (DMC) laboratory, we develop accurate circuit simulation models and parameters. The DMC lab provides complete device model data for our processes using capabilities such as AC measurement, statistical analysis and worst-case modeling. Accurate models are a cornerstone of our design-for-quality approach.

To ensure high quality test vectors, production test vectors are derived from simulation vectors using the TSSI tools early in the design process. The industry-standard Zycad fault simulator is then used to determine fault coverage.

Physical design

Our PEGASYS layout system aids the mask designer through all physical design phases, ensuring consistency throughout the design cycle. This flexible, fully integrated environment supports a broad range of layout techniques, from full-custom to full-automation. Capabilities include:

- Chip floor planning
- Analog device generators
- Schematic driven layout
- On-line point-to-point routing
- Compaction
- Automatic place and route
- Support of custom cells, standard cells, and compiled blocks in any combination
- Design rule checking (drc)
- Layout-versus-schematic verification (lvs)
- Parasitic extraction/back annotation
- Output in industry standard GDS format

In the first generation Pegasys system, Silicon Systems pioneered a device-generator based approach to precision analog layout. In partnership with Mentor Graphics, we have enhanced this technique for our current system, based on Mentor Graphics V8 ICstation® tools. ICstation® provides tremendous flexibility, combined with ease of customization, to fully support analog and mixed-signal designs. A variety of layout styles and techniques are combined to meet each chip's specific requirements. Rigorous verification checks ensure the quality and accuracy of the layout, for both physical and electrical properties. Post-layout simulation uses true parasitic modeling to handle remaining problems before first silicon fabrication.

STATE OF THE ART CMOS DIGITAL AND ANALOG PROCESSES

Silicon Systems offers four proven CMOS process technologies for creating cost effective, highly integrated systems solutions. These processes combine small geometry digital circuit capability with high performance analog capability. Table 1 summarizes Silicon Systems' CMOS process capabilities.

Our newest CK process is designed to support high breakdown, high current power FETs, bipolar structure for specialized analog needs, poly capacitors and resistors, low noise differential amplifiers and high performance A/D and D/A converters. It also includes highly optimized and silicon area efficient digital cells including DSPs, microcontrollers, sequencers, memory managers and data paths.

The CJ process provides high performance analog and digital cells and includes the same analog and digital complex devices in our CK process.

Our CG process supports high-performance analog circuitry with precision poly-poly capacitors. Complex analog circuitry includes 1.25 Amp power FETs, 12-bit switched capacitor analog to digital converters and low distortion operational amplifiers and filters. Complex digital circuitry includes DSPs, microcontrollers, sequencers, memory mangers and data paths.

The CH process also provides high quality, low voltage coefficient, precision poly-poly capacitors that support high performance switched-capacitor filtering and data conversion (A/D and D/A) circuits.

BIPOLAR & BICMOS PROCESS TECHNOLOGIES

Our bipolar MSICs take advantage of two high-performance Bipolar processes: BK (for 12V applications) and BN (for 5V applications). The BK analog/digital process achieves its higher voltage operation and improves lateral PNP transistor performance by using a lightly-doped epi layer.

In BK we provide deep N+ and P+ enhancement layers to reduce both collector series and base resistance. Our use of up-junction isolation gives us a major reduction in device area, when compared with that of typical junction isolated processes. Metal-poly capacitors with a nitride dielectric are used for improving capacitor reliability.

BN. Low-power/ 8 GHz Bipolar at 5 volts

A noteworthy feature of a minimum size BN process transistor is that it's only about 1/5th the size of a minimum size BK transistor. Because we employ full oxide isolation in BN, we can fabricate very fast, very small transistors and reduce sidewall capacitances. This supports not only high speed, but low power.

The BN process features high-performance NPN transistors to support mixing high-performance emitter coupled logic (ECL) with analog circuitry. To provide for strict TTL I/O compatibility, we use superior PtSi Schottky diodes.

The resulting speed and packing density allows you to effectively implement dense high-performance, low-power Bipolar analog/digital capability into your system designs.

For a feature-by-feature comparison of Silicon Systems' BK and BN Bipolar processes, see Table 3.

BiCMOS process technologies

Our BiCMOS process portfolio is expanding to support the evolving demands of the mixed-signal IC market. Now in production is our BCA process which combines 13 GHz NPNs with 1.0μ CMOS features to support the design of efficient, high performance, mixed-signal circuits. High bandwidth analog circuits can be combined with dense digital logic to support the development of 5V data channels with transfer rates into the 120+ Mbit/s range, while maintaining low power consumption. The BCA technology has also allowed our designers to develop 3V only circuits to address very low power applications.

Our second generation BiCMOS process, BCB, will provide the next step in performance with a parallel improvement in circuit density. BCB advances our BiCMOS with 0.8μ CMOS feature sizes and improved interconnect capability resulting in a significant performance step for CMOS logic. This will allow implementation of mixed-signal circuits that support data transfer rates well beyond 200 Mbit/s, while maintaining very low power dissipation. The dense digital advantages of BCB will also expand the possibilities for cost effective customization and programmability in both 5V and 3V environments.

For a summary of our BiCMOS processes see Table 2.

Process	Type	Application Voltage	BVDSS	Drawn Gate Length	Interconnect Pitches Poly 1	Metal 1	Metal 2	Features
CH	Si-Gate, single metal, dual poly, PWell	12V	18V	3.6µ	5.8µ	6.4µ	n/a	• DDD S/D structure • Poly-poly capacitors • Low-voltage coefficient • High Ω/□poly resistors • Epi substrate option • Buried well-ring
CG	Si-Gate, dual metal, dual poly, PWell	5V	7V	1.5µ	3.0µ	4.5µ	6.0µ	• DDD S/D structure • Poly-poly capacitors • Shrinkable to 1.2µ
CJ	Si-Gate, dual metal, dual poly, NWell	5V	7V	1.0µ	2.0µ	3.0µ	3.3µ	• Ldd S/D structure • Poly-poly capacitors • Shrinkable to 0.8µ
CK	Si-Gate, dual metal, dual poly, NWell	5V	7V	0.8µ	1.6µ	2.0µ	2.4µ	• Ldd S/D structure • Poly-poly capacitors • Shrinkable to 0.5µ

TABLE 1: CMOS Process Chart

Process	Appl. Voltage	BVDSS	Drawn Gate Length	Interconnect Pitches Poly	M0	M1	M2	BV_{CEO}	NPN Ft	Emitter	Features
BCA:	5V	10V	1.0µ	2.6µ	3.2µ	3.8µ	5.0µ	8V	13 GHz	1.0µ	**Bipolar:** • High Performance NPNs • Polysilicon emitters • PtSi Schottky Diodes • Poly resisters • Gate Oxide Capacitors • Poly Capacitors • Sidewall Oxide Isolation • Fuses **CMOS:** • Lightly Doped Drains
BCB:	5V	8V	0.8µ	1.6µ	2.0µ	2.0µ	2.4µ	8V	15 GHz	0.8µ	

TABLE 2: BiCMOS Process Chart

Process	Type	BV_{CEO}	NPN Ft	Emitter Size	M1 Pitch	M2 Pitch	Features
BK	Junction-isolated	12V	2 GHz	2.5µ	9.0µ	14.0µ	• Polysilicon emitters • Al Schottky diodes • Nitride capacitors • Ion implanted resistors • Up/down junction isolation • Collector/base plugs
BN	Oxide-isolated	6V	8 GHz	2.0µ	4.5µ	8.0µ	• High performance NPNs • PtSi Schottky diodes • Nitride capacitors • Ion implanted resistors • Sidewall oxide isolation • Collector/base plugs

TABLE 3: Bipolar Process Chart

A SUPERIOR FINISH FOR CMOS, BIPOLAR AND BICMOS

You might say this is the payoff window. The benefits of our process technologies, design tools and our unique custom approach all come together during wafer fabrication, test and assembly.

Our two manufacturing centers, located in Tustin and Santa Cruz, California, can offer specialized capabilities to match your particular fabrication requirements. Both facilities provide you with high resolution stepper photolithography technology, positive resist, dry plasma etch systems, high current ion implantation and automatic sputtering.

Fabrication sites in both Tustin and Santa Cruz accommodate 4- and 6-inch wafer fabrication and Bipolar, CMOS and BiCMOS processes.

The right package

Silicon Systems offers a wide range of packages to meet the small footprint requirements of advanced storage and communication products. We continue to be innovative in surface mount technology by providing PLCC, SO, VSOP, VTSOP, QFP, TQFP, VTQFP and UTQFP packages. At our ISO 9002-certified Singapore assembly & test facility we have the full capability to support high quality automated packaging while also maintaining rapid cycle times.

Promis. Quality through CAM

Process and Management Information System (PROMIS) underscores our commitment to computer-aided manufacturing (CAM). And to delivering you a superior quality product on time.

We use PROMIS to facilitate the data required in our manufacturing, monitoring and statistical process control (SPC) systems.

With PROMIS we more effectively manage our inventory, accurately track wafers in process, and closely monitor the clean room environment.

PROMIS also assists our SPC efforts, as does our commitment to fully train all of our manufacturing personnel in SPC basics.

We design for quality

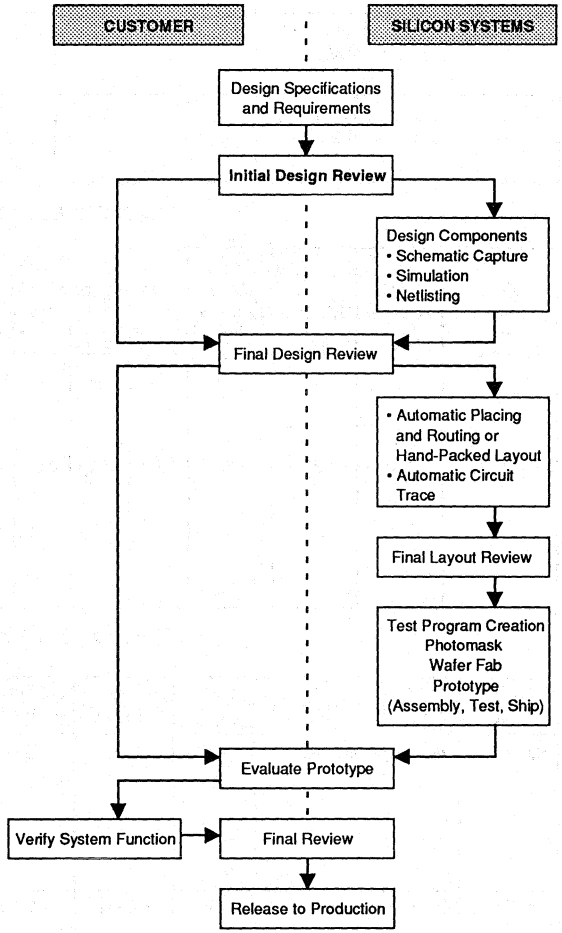
It's our view that quality is nothing less than absolute customer satisfaction. To achieve it, we begin far "upstream" in the product development process. Our design-for-quality approach scrutinizes the design itself with statistically based models, comprehensive simulation tools and vigorous design reviews.

The results of such an effort are IC products that boast lower defect rates, higher parametric performance and far fewer redesigns. Moreover, our persistence in improving quality keeps us focused on finding better and faster ways to satisfy future customer demands.

Quality that delivers

With effective systems such as PROMIS and our design-for-quality approach in place, Silicon Systems is prepared to deliver you finished products you can really depend on. On time. And within budget.

For details on how you can take best advantage of Silicon Systems' custom mixed-signal IC solutions, see your nearest Silicon Systems representative, or contact us. Silicon Systems, Inc. 14351 Myford Road, Tustin, CA 92680-7022. 714-573-6000. FAX: (714) 573-6914.



Customer Interface for Full-Custom and Cell-Based Designs

Section 2

RELIABILITY & QUALITY ASSURANCE

CONTINUOUS IMPROVEMENT MISSION & OBJECTIVE STATEMENT

Mission

Be the supplier of choice by exceeding customer expectations through continuous improvements in our products, systems and services.

Objectives

Provide world class quality in our products and services through focus on:

Customer Partnering
Cycle Time Improvement
Process and System Improvements

Develop a culture that ensures the consistent use of continuous improvement tools and fact based decision methodology by:

Senior Management Leadership
Employee Empowerment
Aggressive Goal Setting and Performance Measurement
Communication and Celebration of Successes

Alan V. King
President, CEO

Cheryl A. Stock
Vice President, Corporate R&QA

Silicon Systems®
A TDK Group Company

SECTION 1

1.1 INTRODUCTION

Silicon Systems is committed to the goal of customer satisfaction through the on-time delivery of defect free products that meet the customer's expectations and requirements. This section outlines Silicon Systems' ongoing activities for the control and continual improvement of quality in every aspect of our organization.

Silicon Systems is diligently working to maintain and improve its position as a world-class provider of mixed-signal integrated circuits (MSICs®).

We realize and practice the concept that quality and reliability must be designed and built into our products. In addition, Silicon Systems utilizes rigid inspections and data analysis to evaluate the acceptability and variation existing in incoming materials and performs stringent outgoing quality verification. The manufacturing process flow is encompassed by an effective system of test/inspection checks and in-line monitors which focus on the control and reduction of process variation. These gates and monitors ensure precise adherence to prescribed standards and procedures.

Silicon Systems also incorporates the use of statistical process control techniques into company operations. The control and reduction of the process variation by the use of statistical problem solving techniques, analytical controls and other quantitative methods ensures that Silicon Systems' products maintain the highest levels of quality and reliability.

Our Reliability and Quality Assurance organizations are committed to working closely with our customers to provide assistance and a continually improving level of product quality.

1.2 SILICON SYSTEMS' QUALITY MANDATE: CONTINUOUS IMPROVEMENT

Continuous improvement is Silicon System's strategic thrust for the 1990's. In order to ensure that all aspects of our business are encompassed by this mandate, Corporate Reliability & Quality Assurance has been chartered with the responsibility for developing, educating and overseeing the worldwide continuous improvement process. The continuous improvement initiative will lead to developing a new organizational culture, changing attitudes and stronger ownership and accountability for total customer satisfaction.

1.3 CHARACTERISTICS OF SILICON SYSTEMS' CONTINUOUS IMPROVEMENT PROCESS

- Executive Steering Committee leadership and direction - defines the right things to do and provides guidance - the right way to do them.
- Continuous improvement is measured everywhere and by everyone. Metrics that reflect pride in accomplishment are celebrated.
- Benchmarking is employed as a method to shorten learning curves and ensure successful ventures.
- Quality management and employee empowerment are encouraged at all levels.

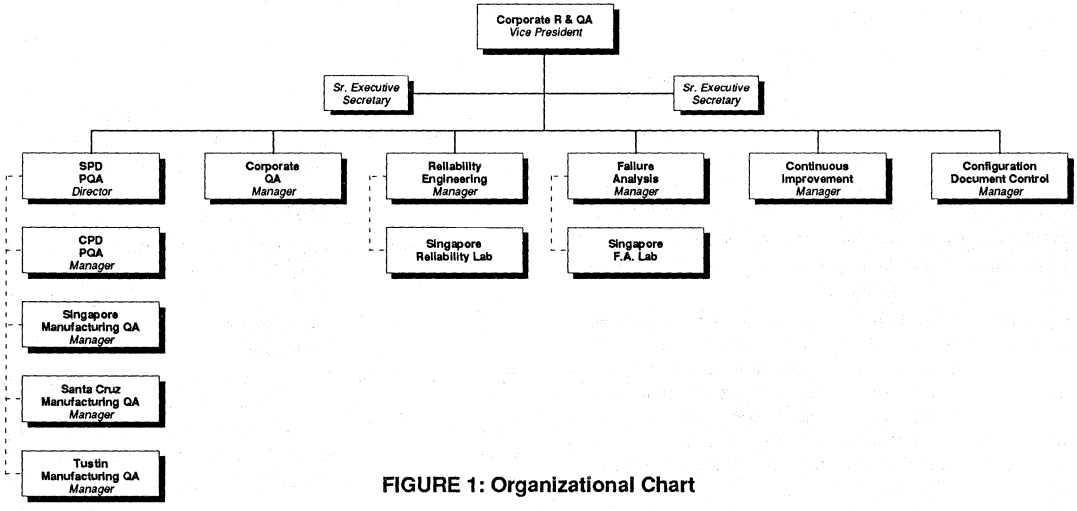


FIGURE 1: Organizational Chart

- Supplier partnership is a critical element of our quality strategy.

This is the essence of Silicon Systems - a total quality involved company - forward looking and immersed in the goal of customer satisfaction and best-in-class business pursuits.

1.4 CORPORATE RELIABILITY AND QUALITY ASSURANCE

It is the objective of the Corporate Reliability and Quality Assurance organization to ensure that proactive quality systems are in place to ensure that Silicon Systems' products will meet or exceed customer requirements and expectations. In addition, the Reliability and Quality Assurance organization works to facilitate the timely implementation of solutions and monitors the effectiveness of corrective actions. These organizational strategies support the continuing enhancement of quality consciousness throughout Silicon Systems.

1.5 ISO 9000 CERTIFICATION

Silicon Systems has determined that ISO 9000 certification is an important strategy for achieving total customer satisfaction. Our Singapore assembly and test operations facility has been ISO 9002 certified through SISIR and our domestic facilities are currently in pursuit of this important industry standard. We believe strongly that ISO 9000 certification proves that Silicon Systems is doing the right things to do things right.

SECTION 2: QUALITY ASSURANCE

2.1 QUALITY OBJECTIVES

While all Silicon Systems employees have direct responsibility for quality in their functions, the Quality Assurance Organizations have the ultimate responsibility for the reliable performance of our products. This is accomplished through the development, administration and assessment of formal quality systems which assure Silicon Systems' management, as well as our customers, that products will fulfill the requirements of customer purchase orders and all other specifications related to design, raw material and in process through completion of the finished product.

Corporate Quality Assurance supports, coordinates and actively participates in the formal qualification of suppliers, material, processes, and products, and the administration of quality systems and production monitors to assure that our products meet Silicon Systems quality standards. Product Quality Assurance provides the liaison between Silicon Systems and the customer for all product quality related concerns.

It is the practice of Silicon Systems to have corporate quality and reliability objectives encompass all of its activities. This starts with a strong commitment of support from the corporate level and continues with exceptional customer support long after the product has been shipped.

Silicon Systems emphasizes the belief that quality and reliability must be built into all of its products by ensuring that all employees are educated in the quality philosophy of the company. Some of the features built into Silicon Systems quality culture include:

1. Structured training programs directed at wafer fabrication, test, process control personnel and supporting organizations.
   - Team-based problem solving methodologies.
   - Corporate-wide training of quality philosophy and statistical methods.
2. Stringent in-process inspection, gates, and monitors.
3. Rigorous evaluation of designs, materials, and processing procedures.
4. Stringent electrical testing (100% and QC AQL/Sample testing).
5. Ongoing reliability monitors and process verifications.
6. Real-time use of statistical process control methodology.
7. Corporate level audits of manufacturing, subcontractors, and suppliers.
8. Timely corrective action system.
9. Control of non-conforming material.

These focused quality methods result in products which deliver superior performance and reliability in the field.

2.2.1 INCOMING INSPECTIONS

Incoming inspection plays a key role in Silicon Systems' quality efforts. Small variations in incoming material can traverse the entire production cycle before being detected much later in the process. By paying strict attention to the monitoring of materials at the earliest possible stage, variation can be reduced, resulting in a stable uniform process.

2.2.2 IN-PROCESS INSPECTIONS

Silicon Systems has established key inspection monitors in such strategic areas as wafer fabrication, wafer probe, assembly, and final test. These quality monitoring tests are performed in addition to the intermediate and final inspections found in the manufacturing process.

Quality control monitors have been integrated throughout the manufacturing flow, so that data may be collected and analyzed to verify the results of intermediary manufacturing steps. This data is used to document quality trends or long term improvements in the quality of specific operations.

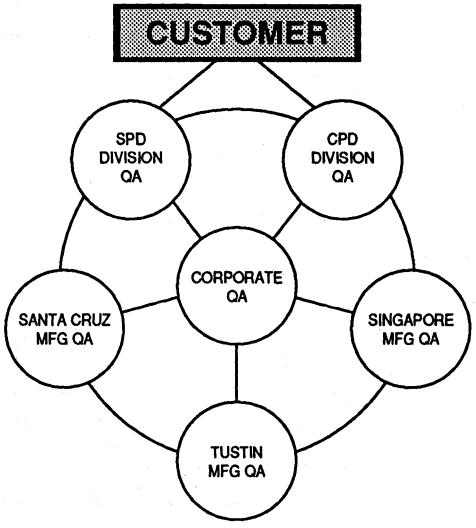


FIGURE 2
Quality Assurance Relationships
Quality Steering Committee

Abnormality control is being used to enhance the effectiveness of this process. In process monitors such as oxide integrity, electromigration immunity and other parameters monitor long term reliability as well as circuit performance.

2.3 QUALITY STEERING COMMITTEE

The Corporate, Product and Manufacturing Quality Assurance organizations work closely together to provide leadership in the development, integration and assessment of Silicon Systems' worldwide quality systems and procedures.

This team approach ensures that policies and procedures are standardized and facilitates rapid improvement in products, processes and services.

2.4 DESIGN FOR QUALITY

Since the foundation of a reliable product is rooted in the design process, the Reliability and Quality Assurance organizations actively participate in comprehensive cross-functional reviews of design stages prior to the product's transition to production status. These review stages assure a predictable and effective development cycle. Other important design-related functions include ensuring that process specification revisions are translated into updated design parameters and the translation of manufacturing process capability into design guidelines. This is accomplished through the identification and monitoring of critical process and device parameters. Wafer level test at the early stages of process development also plays a critical role. These elements, included in Silicon Systems design for quality effort, support the development of robust design rules which are as insensitive as possible to inherent manufacturing variation. The result is a product that delivers predictable and reliable long term performance.

2.5 PPM REDUCTION PROGRAM

The primary purpose of a PPM reduction program is to provide a formalized feedback system in which data from nonconforming products can be used to improve future product consistency and reliability. The action portion of this program is accomplished in three stages:

1. Identification of defects by failure mode.
2. Identification of defect causes and initiation of corrective action.
3. Measurement of results and setting of improved goals.

The data summarized from the established PPM program is compiled as a ratio of units rejected/tested. This ratio is then expressed in terms of defective parts per million (PPM). Founded on a statistically valid database of PPM data and an established five-year strategic plan identifying PPM improvement goals, Silicon Systems has consistently achieved excellent quality standards and will continue to progressively improve PPM standards.

2.6 COMPUTER AIDED MANUFACTURING CONTROL

Computer Aided Manufacturing (CAM) is used throughout Silicon Systems for the identification, control, collection and dissemination of timely information for logistics control. Silicon Systems also uses this type of computerized system for statistical process control and manufacturing monitoring. PROMIS, (PROcess Management and Information System), displays approved/controlled recipes, processes, and procedures; tracks work-in-process; reports accurate inventory information; allows continuous recording of facilities data; contains statistical analysis capabilities; and much more. PROMIS allows for a paperless facility, a major element in minimizing contamination of clean room areas.

TEST	CONDITIONS	PURPOSE OF EVALUATION
Biased temperature/humidity	85°C/85° %RH	Resistance to high humidity with bias
Highly accelerated stress test (HAST)	JDEC A110	Evaluates package integrity
High temperature operating life (HTOL)	Mil 883D, Method 1005	Resistance to electrical and thermal stress
Early Failure Rate	Mil 883D, Method 1005	Detect infant mortality
Steam pressure	121°C/15PSI	Resistance to high humidity
Temperature cycling	Mil 883D, Method 1010	Resistance to thermal excursion (air)
Thermal shock	Mil 883D, Method 1011	Resistance to thermal excursion (liquid)
Salt atmosphere	Mil 883D, Method 1009	Resistance to corrosive environment
Constant acceleration	Mil 883D, Method 2001	Resistance to constant acceleration
Mechanical shock	Mil 883D, Method 2002	Resistance to mechanical shocks
Solderability	Mil 883D, Method 2003	Evaluates solderability of leads
Lead integrity	Mil 883D, Method 2004	Evaluates lead integrity before board assembly
Vibration, variable frequency	Mil 883D, Method 2007	Resistance to vibration
Thermal resistance	Silicon Systems Method	Evaluates thermal dissipation
Electrostatic damage	Mil 883D, Method 3015	Evaluates ESD susceptability
Latch-up	Silicon Systems Method	Evaluates latch-up susceptibility
Seal fine and gross leak	Mil Std 883D, Method 1014	Evaluates hermeticity of sealed packages

TABLE 1: Reliability Stress Tests

SECTION 3: RELIABILITY

3.1 RELIABILITY PROGRAM

Silicon Systems has defined various programs that will characterize product reliability levels on a continuous basis. These programs can be categorically described by:

1. Qualifications
2. Production monitors
3. Evaluations
4. Failure analysis
5. Wafer level reliability
6. Data collection and presentation for improvement projects

3.2 QUALIFICATIONS

Extensive qualification testing and data collection ensures that all new product designs, processes, and packaging configurations meet the absolute maximum ratings of design and the worst case performance criteria for end users. A large database generated by means of accelerated stress testing results in a high degree of confidence in predicting final use performance. The qualification criteria used are periodically reviewed to be consistent with Silicon Systems' increasing quality and reliability goals in support of our customers.

3.3 PRODUCTION MONITORS

This program has been established to randomly select a statistically significant sample of production products for subjection to maximum stress test levels in order to evaluate the useful life of the product in a field use environment.

Table 1 lists reliability test methods that are in use at Silicon Systems. This analysis of production monitor at Silicon Systems provides valuable information on possible design/process changes which assure continued improved reliability. The monitors are periodically reviewed for effectiveness and improvements.

3.4 EVALUATIONS

The evaluation program at Silicon Systems is an ongoing effort that will continue defining standards which address the reliability assessment of the circuit design, process parameters, and package of a new product. This program continuously analyzes updated performance characteristics of product as they undergo improvement efforts at Silicon Systems.

3.5 FAILURE ANALYSIS

The failure analysis function is an integral part of the Quality and Reliability department at Silicon Systems. Silicon Systems has assembled a highly technical and sophisticated failure analysis laboratory and staff. This laboratory provides visual analysis, electrical reject mode analysis, and both

destructive and non-destructive data to aid the engineers in developing corrective action for improvement. These test analyses may include metallurgical, optical, chemical, electrical, SEM with X-ray dispersive analysis, and E-Beam non-contact analysis as needed.

These conclusive in-house testing and analysis techniques, are complemented by outside support, such as scanning acoustic microscopy, focused ion beam, and complete surface and material analysis. This allows Silicon Systems to monitor all aspects of product manufacturing to ensure that the product of highest quality is shipped to our customers.

3.6 WAFER LEVEL RELIABILITY PROGRAM

A primary objective at Silicon Systems is to improve the reliability of our products through characterization of our manufacturing operations. The identification of specific failure mechanisms occuring in the wafer fabrication and assembly processes is a prerequisite to effective corrective action aimed at reducing defects and improving quality and reliability.

The primary advantage of wafer level reliability testing is the speed at which results can be derived, thereby providing additional response time and an early warning of process changes. This tool provides Silicon Systems with a very rapid analysis tool which allows for the early identification of possible problems and a determination of their origin.

The continuous improvement approach taken at Silicon Systems uses the wafer level reliability tests as tools to improve the process, identify potential problems, determine the sources of any process weakness and eliminate problems upstream in the process. This results in a focus on reliability improvement that goes well beyond merely determining the projected lifetime of a product to a detailed characterization, measurement and control of the specific parameters which actuallly determine product lifetime.

3.7 DATA COLLECTION AND PRESENTATION FOR IMPROVEMENT PROJECTS

Data collected from each element of the Reliability program is summarized for scope and impact and distributed among all engineering disciplines in the company. This data facilitates improvement and provides our customers an opportunity to review the performance of our product.

3.8 RELIABILITY METHODS

The Reliability Program utilizes a number of stress tests that are presently being used to define performance levels of our products. Many of these stress tests are per MIL-STD-883D as shown in Table 1.

3.9 RELIABILITY PREDICTION METHODOLOGY

At Silicon Systems, the Arrhenius model is used to relate a failure rate at an accelerated temperature test condition to a normal use temperature condition.

The model basically states $FR = A \exp(-Ea/KT)$

Where:

- FR = Failure rate
- A = Constant
- Ea = Activation Energy (eV)
- K = Boltzmann's constant 8.62×10^{-5} eV/ degree K
- T = Absolute temperature (degree K)

SECTION 4: ELECTROSTATIC DISCHARGE PROGRAM

4.1 ESD PREVENTION

Silicon Systems recognizes that the protection of Electrostatic Discharge (ESD) sensitive devices from damage by electrical transients and static electricity is vital. ESD safe procedures are incorporated throughout all operations which come in contact with these devices. Continuous improvement in the ESD protection levels is being accomplished through the incorporation of increasingly robust protection devices during the circuit design process as well as work area improvements.

Silicon Systems' quality activity incorporates several protection measures for the control of ESD. Some of the preventive measures include handling of parts at static safe-guarded workstations, the wearing of wrist straps during all handling operations, the use of conductive lab coats in all test areas and all areas which handle parts and the packaging of components in conductive or anti-static containers.

NOTES

Section 3

HDD READ/WRITE AMPLIFIERS

silicon systems®
A TDK Group Company

SSI 32R5281AR
14-Channel Two-Terminal Read/Write Device

Advance Information

July 1992

DESCRIPTION

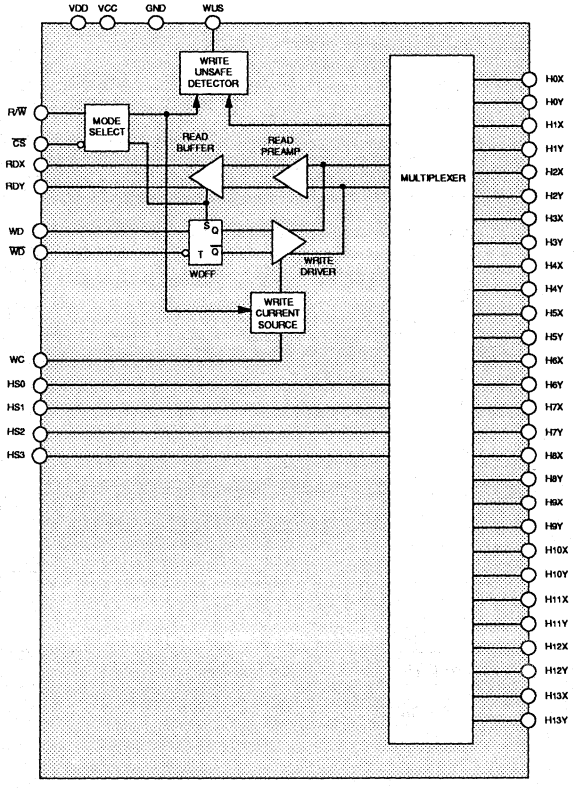
The SSI 32R5281AR Read/Write device is a bipolar monolithic integrated circuit designed for use with two-terminal thin-film recording heads. It provides a low noise read amplifier, write current control and data protection circuitry for up to 14 channels. Power supply fault protection is provided by disabling the write current generator during power sequencing. System write to read recovery time is significantly improved by controlling the read channel common mode output voltage shift in the write mode. It requires +5V and +12V power supplies and provides internal 700Ω damping resistors. The 32R5281AR offers power and performance improvement over 32R5281R.

FEATURES

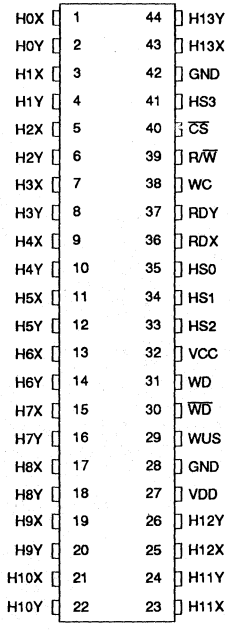
- **High performance:**
  - **Read mode gain = 250 V/V**
  - **Input noise = 0.80 nV/√Hz max.**
  - **Input capacitance = 22 pF max.**
  - **Write current range = 10 mA to 40 mA**
  - **Head voltage swing = 7 Vpp**
  - **Write current rise time = 9 ns**
- **Enhanced system write to read recovery time**
- **Differential ECL-like Write Data input**
- **Power supply fault protection**
- **Write unsafe detection**
- **+5V, +12V power supplies**

3

BLOCK DIAGRAM



PIN DIAGRAM



44-LEAD SOM

CAUTION: Use handling procedures necessary for a static sensitive component.

CIRCUIT OPERATION

The SSI 32R5281AR addresses up to 14 two-terminal thin film heads providing write drive or read amplification. Head selection and mode control is accomplished with pins HSn, $\overline{CS}$ and R/$\overline{W}$, as shown in Tables 1 & 2. Internal resistor pullups, provided on pins $\overline{CS}$ and R/$\overline{W}$ will force the device into a non-writing condition if either control line is opened accidentally.

WRITE MODE

The write mode configures the SSI 32R5281AR as a current switch and activates the Write Unsafe (WUS) detection circuitry. Write current is toggled between the X and Y direction of the selected head on each low to high transition on the WD, Write Data input. (See figure 1.)

A preceding read operation initializes the Write Data Flip Flop (WDFF) to pass write current in the X-direction of the head, i.e., into the X-port of the head. HnX will be biased higher than HnY.

The magnitude of the write current (0-pk) is given by:

$$Iw = \frac{Vwc}{Rwc}$$

where Vwc (WC pin voltage) = 1.65V ± 5%, is programmed by an external resistor Rwc, connected from pin WC to ground. In multiple device applications, a single Rwc resistor may be made common to all devices. The actual head current Ix, y is given by:

$$Ix,y = \frac{Iw}{1 + Rh/Rd}$$

where:
Rh = head resistance + external wire resistance, and
Rd = damping resistance.

Power supply fault protection improves data security by disabling the write current generator during a voltage fault or power supply sequencing. Additionally, the write unsafe detection circuitry will flag any of the conditions listed below as a high level on the open collector output pin, WUS. Up to two positive transitions on the WD, Write Data input line, after the fault is corrected, are required to clear the WUS flag.

- WD frequency too low
- Device not selected
- Open head
- Device in read mode
- No write current

READ MODE

The read mode configures the SSI 32R5281R as a low noise differential amplifier and deactivates the write current generator and write unsafe detection circuitry. The RDX and RDY outputs are emitter followers and are in phase with the "X" and "Y" head ports. These outputs should be AC coupled to the load. The RDX, RDY common mode voltage is maintained at the write mode value, minimizing the transient between write mode and read mode, substantially reducing the write to read recovery time in the subsequent Pulse Detection circuitry.

IDLE MODE

The idle mode deactivates the internal write current generator, the write unsafe detector and switches the RDX, RDY outputs into a high impedance state. This facilitates multiple device applications by enabling the read outputs to be wire-OR'ed and the write current programming resistor to be common to all devices.

TABLE 1: Mode Select

$\overline{CS}$	R/$\overline{W}$	MODE
0	0	Write
0	1	Read
1	0	Idle
1	1	Idle

TABLE 2: Head Select*

HS3	HS2	HS1	HS0	HEAD
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13

0 = Low level 1 = High level

*Unused heads should be left open.

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
HSO - HS3	I	Head Select
$\overline{CS}$	I	Chip Select: a low level enables the device
R/$\overline{W}$	I	Read/Write: a high level selects Read mode
WUS	O*	Write Unsafe: Open collector output, a high level indicates an unsafe writing condition
WD, $\overline{WD}$	I	Differential Write Data inputs: a positive transition on WD toggles the direction of the head current
H0X - H13X H0Y - H13Y	I/O	X, Y Head Connections: Current in the X-direction flows into the X-port
RDX, RDY	O*	X, Y Read Data: differential read data output
WC	*	Write Current: used to set the magnitude of the write current
VCC	-	+5V Logic Circuit Supply
VDD	-	+12V
GND	-	Ground

*When more than one R/W device is used, these signals can be wire OR'ed.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation outside these rating limits may permanently damage the device.

PARAMETER		SYMBOL	RATING
DC Supply Voltage		VDD	-0.3 to +13.5 VDC
		VCC	-0.3 to +6 VDC
Write Current		Iw	100 mA
Digital Input Voltage		Vin	-0.3 to VCC +0.3 VDC
Head Port Voltage		VH	-0.3 to +8 VDC
Differential Port Voltage	|HnX - HnY|	ΔVH	6 VDC
WUS Pin Voltage Range		Vwus	-0.3 to VCC VDC
Output Current	RDX, RDY	Io	-10 mA
	WUS	Iwus	+12 mA
Storage Temperature		Tstg	-65 to +150°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATING
DC Supply Voltage	VDD	12 ± 10% VDC
	VCC	5 ± 10% VDC
Operating Temperature	Tj	+25 to +135°C

DC CHARACTERISTICS
Unless otherwise specified, recommended operating conditions apply.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
VDD Supply Current	Read Mode	-	36	TBD	mA
	Write Mode	-	25 + Iw	TBD	mA
	Idle Mode	-	3	TBD	mA
VCC Supply Current	Read Mode	-	22	TBD	mA
	Write Mode	-	14	TBD	mA
	Idle Mode	-	10	TBD	mA
Power Dissipation (Tj = +135°C)	Read Mode	-	540	700	mW
	Write Mode	-	375+10.35•Iw	490 +11.6•Iw	mW
	Idle Mode	-	85	110	mW
WD, $\overline{WD}$ Input Low Current (IIL1)	VIL1 = VCC -1.625V			80	µA
WD, $\overline{WD}$ Input High Current (IIH1)	VIH1 = VCC -0.72V			100	µA
WD, $\overline{WD}$ Input Low Voltage (VIL1)		VCC -1.870		VCC -1.625	VDC
WD, $\overline{WD}$ Input High Voltage (VIH1)		VCC -1.00		VCC -0.720	VDC
R/$\overline{W}$, $\overline{CS}$, HS0-HS3 Input Low Current (IIL2)	VIL2 = 0.8V	-0.4			mA
R/$\overline{W}$, $\overline{CS}$, HS0-HS3 Input High Current (IIH2)	VIH2 = 2.0V			100	µA
R/$\overline{W}$, $\overline{CS}$, HS0-HS3 Input Low Voltage (VIL2)				0.8	VDC
R/$\overline{W}$, $\overline{CS}$, HS0-HS3 Input High Voltage (VIH2)		2.0			VDC
WUS Output Low Voltage (VOL)	Iol = 8 mA	-	-	0.5	VDC
VDD Fault Voltage		9.0	-	10.3	VDC
VCC Fault Voltage		3.5	-	4.2	VDC

DC CHARACTERISTICS (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Head Current (HnX, HnY)	Write Mode, 0 ≤ VCC ≤ 3.5V 0 ≤ VDD ≤ 9.0V	-200	-	+200	µA
	Read/Idle Mode, 0 ≤ VCC ≤ 5.5V 0 ≤ VDD ≤13.2V	-200	-	+200	µA

3

WRITE CHARACTERISTICS

Unless otherwise specified, recommended operating conditions apply, Iw = 20 mA, Lh = 500 nH, Rh = 30Ω and f(WD) = 5 MHz.

WC Pin Voltage (Vwc)	10 ≤ Iw ≤ 40 mA	1.57	1.65	1.73	V
Differential Head Voltage Swing		7	-	-	Vpp
Unselected Head Current		-	-	1	mA(pk)
Differential Output Capacitance		-	-	25	pF
Differential Output Resistance		500	700	950	Ω
WDI Transition Frequency	WUS = low	1.7	-	-	MHz
	WUS = high	-	-	500	kHz
Write Current Range		10	-	40	mA

READ CHARACTERISTICS

Unless otherwise specified, recommended operating conditions apply CL (RDX, RDY) < 20pF and RL (RDX,RDY) = 1 kΩ.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
Differential Voltage Gain		Vin=1mVpp @ 300 kHz	210	250	290	V/V
Bandwidth	-1dB	|Zs|<5Ω, Vin=1 mVpp	25	40	-	MHz
	-3dB	|Zs|<5Ω, Vin=1 mVpp	35	55	-	MHz
Input Noise Voltage		BW = 15 MHz, Lh = 0, Rh = 0	-	0.57	0.80	nV/√Hz
Differential Input Capacitance		Vin = 1 mVpp, f = 5 MHz	-	15	22	pF
Differential Input Resistance		Vin = 1 mVpp, f = 5 MHz	300	565	-	Ω
Dynamic Range		Peak-to-peak AC input voltage where gain falls to 90% of its small signal value, f = 5 MHz	2.0	-	-	mVpp
Common Mode Rejection Ratio		Vcm = 100 mVpp AC Coupled @ 5 MHz	54	-	-	dB
Power Supply Rejection Ratio		100 mVpp @ 5 MHz on VDD 100 mVpp @ 5 MHz on VCC	54	-	-	dB
Channel Separation		Unselected channels driven with 100 mVpp @ 5 MHz, Vin = 0 mVpp	45	-	-	dB

READ CHARACTERISTICS (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Output Offset Voltage		-400	-	+400	mV
RDX, RDY Common Mode Output Voltage	Read Mode or Write Mode	Vcc -2.5	Vcc - 2.1	Vcc -1.7	VDC
Single Ended Output Resistance	f = 5 MHz	-	-	30	Ω
Output Current	AC Coupled Load, RDX to RDY	3.2	-	-	mA

SWITCHING CHARACTERISTICS (See Figure 1)
Unless otherwise specified, recommended operating conditions apply, Iw = 20 mA, Lh = 500 nH, Rh = 30Ω and f(WD) = 5 MHz.

PARAMETER	CONDITIONS	MIN	MAX	UNITS
R/$\overline{W}$				
R/$\overline{W}$ to Write Mode	Delay to 90% of write current	-	0.6	µs
R/$\overline{W}$ to Read Mode	Delay to 90% of 100mV 10MHz Read signal envelope or to 90% decay of write current	-	0.6	µs
$\overline{CS}$				
$\overline{CS}$ to Select	Delay to 90% of write current or to 90% of 100mV 10MHz Read signal envelope	-	0.6	µs
$\overline{CS}$ to Unselect	Delay to 90% of write current	-	0.6	µs
HSn				
HS0, 1, 2, 3 to any Head	Delay to 90 % of 100mV 10MHz Read signal envelope	-	0.4	µs
WUS				
Safe to Unsafe - TD1		0.6	2.0	µs
Unsafe to Safe - TD2		-	1	µs
Head Current				
Prop. Delay - TD3	From 50 % points, Lh=0µh, Rh=0Ω	-	32	ns
Asymmetry	WD has 50 % duty cycle and 1ns rise/fall time, Lh=0µh, Rh=0Ω	-	0.5	ns
Rise/Fall Time	10% - 90% points, Lh=0µh, Rh=0Ω	-	9	ns

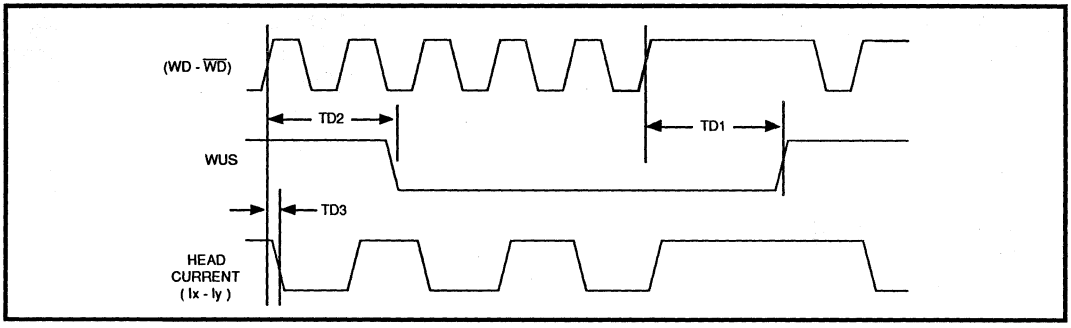


FIGURE 1: Write Mode Timing Diagram

APPLICATIONS INFORMATION

The specifications, provided in the data section, account for the worst case values of each parameter taken individually. In actual operation, the effects of worst case conditions on many parameters correlate. Tables 3 & 4 demonstrate this for several key parameters. Notice that under the conditions of worst case input noise, the higher read back signal resulting from the higher input impedance can compensate for the higher input noise. Accounting for this correlation in your analysis will be more representative of actual performance.

TABLE 3: Key Parameters Under Worst Case Input Noise Conditions

PARAMETER	Tj = 25°C	Tj = 135°C	UNITS
Input Noise Voltage (Max.)	TBD	0.80	nV/$\sqrt{Hz}$
Differential Input Resistance (Min.)	TBD	TBD	Ω
Differential Input Capacitance (Max.)	TBD	TBD	pF

TABLE 4: Key Parameters Under Worst Case Input Impedance Conditions

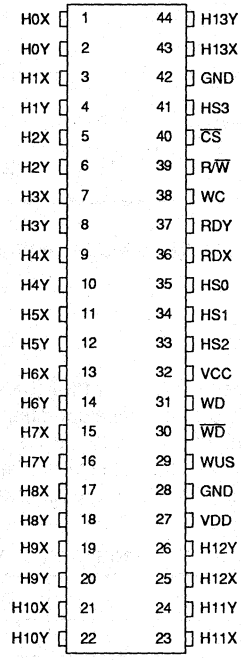
PARAMETER	Tj = 25°C	Tj = 135°C	UNITS
Input Noise Voltage (Max.)	TBD	TBD	nV/$\sqrt{Hz}$
Differential Input Resistance (Min.)	TBD	TBD	Ω
Differential Input Capacitance (Max.)	TBD	TBD	pF

SSI 32R5281AR
14-Channel Two-Terminal Read/Write Device

PACKAGE PIN DESIGNATIONS
(Top View)

THERMAL CHARACTERISTICS: θja

44-Lead SOM	40°C/W



44-Pin SOM

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914

SSI 32R1203A/1203AR
+5V, 4-Channel, 3-Terminal Read/Write Device

January 1994

DESCRIPTION

The SSI 32R1203A is a bipolar monolithic integrated circuit designed for use with center-tapped ferrite or MIG recording heads. It provides a low noise read path with a gain of 250 V/V, write current control, and data protection circuitry for as many as 4 channels. Power supply fault protection is provided by disabling the write current generator during power sequencing. A Power Down mode (Idle) is provided to reduce power consumption to less than 10 mW.

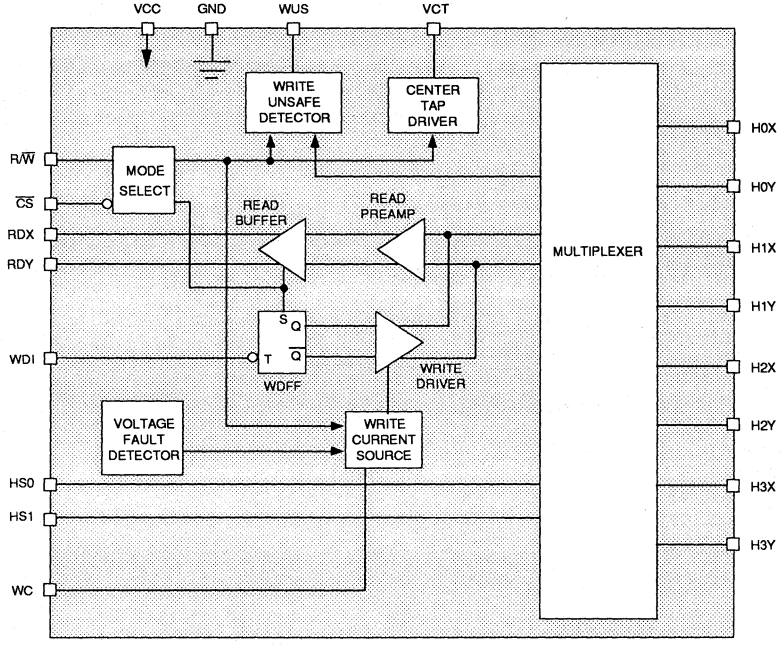
The SSI 32R1203A requires only a +5V power supply and is available in a surface mount package.

FEATURES

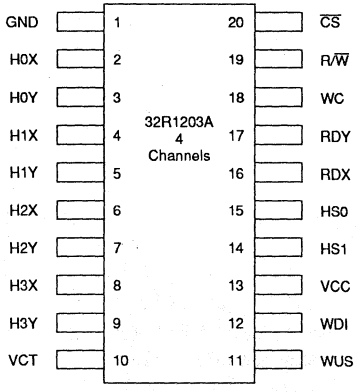
- **+5V only power supply**
- **Low power**
  - **Pd ≤ 225 mW Read mode**
  - **Pd ≤ 10 mW Idle mode**
- **High Performance**
  - **Input noise = 1.2 nV/√Hz max.**
  - **Input capacitance = 19 pF max.**
  - **Write current range = 15 - 50 mA**
  - **Head voltage swing = 6.0 Vpk**
- **250 V/V read gain**
- **Designed for center-tapped ferrite or MIG heads**
- **Power supply fault protection**
- **Includes write unsafe detection**
- **Enhanced Write to Read recovery**

3

BLOCK DIAGRAM



PIN DIAGRAM



20-Lead SOL, SOV

CAUTION: Use handling procedures necessary for a static sensitive component.

FUNCTIONAL DESCRIPTION

WRITE MODE

A source of recording current is provided to the head center tap by an internal voltage reference, VCT. The current is conducted through the head alternately into an HnX terminal or an HnY terminal according to the state of an internal flip-flop. The flip-flop is triggered by the negative transition of the Write Data Input line (WDI). A preceding Read mode selection initializes the write data flip-flop, WDFF, to pass write current through the "X" side of the head. The write current magnitude is determined by the value of an external resistor Rwc connected between WC terminal and GND, and is given by:

Iw = K/Rwc, where K = Write Current Constant

WRITE MODE FAULT DETECT CIRCUIT

Several circuits are dedicated to detecting fault conditions associated with the Write mode. A logical high level will be present at the Write Unsafe (WUS) terminal if any of the following write fault conditions are present:

- Head open
- Head center tap open
- Head shorted
- Head shorted to ground
- No write current
- WDI frequency too low
- Device in Read or Idle mode

The Write Unsafe output is open-collector and is usually terminated by an external resistor connected to VCC. Two negative transitions on WDI, after the fault is corrected, will clear the WUS flag.

A safe condition, WUS low, requires alternating voltage spikes on both HnX and HnY that exceed VCT + 1.5V at a rate equal to or higher than the Minimum Rate of WDI for Safe condition.

In addition, the power supply voltage level is monitored by a circuit that inhibits the write current if VCC is too low to permit valid data recording.

READ MODE

In Read Mode, (R/$\overline{W}$ high and $\overline{CS}$ low), the circuit functions as a low noise gain selectable differential amplifier. The read amplifier input terminals are determined by the Head Select inputs. The read amplifier outputs (RDX, RDY) are emitter follower sources, providing low impedance outputs. The amplifier polarity is non-inverting between HnX, HnY inputs and RDX, RDY outputs.

IDLE MODE

Taking $\overline{CS}$ high selects the Idle mode which switches the RDX and RDY outputs into a high impedance state and deactivates the device. Power consumption in this mode is held to a minimum.

MODE SELECTION AND INDICATION CIRCUIT

Logical control inputs which select mode and head channel are TTL compatible. Their functions are described in Table 1 and Table 2.

TABLE 1: Head Select Table

Head Selected	HS1	HS0
0	0	0
1	0	1
2	1	0
3	1	1

TABLE 2: Mode Select Table

Mode Select		Selected Mode	Indicating & Fault Outputs
$\overline{CS}$	R/$\overline{W}$		WUS
1	X	Idle	high
0	1	Read	high
0	0	Write	active

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
HS0, HS1	I*	Head Select: Logical combinations select one of four Heads. See Table 1
$\overline{CS}$	I	Chip Select: a low level enables device. Has internal pull-up resistor.
R/$\overline{W}$	I*	Read/Write: a high level selects Read mode. Has internal pull-up resistor.
WUS	O*	Write Unsafe: a high level indicates an unsafe writing condition.
WDI	I*	Write Data In: negative transition toggles direction of head current.
H0X-H3X H0Y-H3Y	I/O	X, Y head connections
RDX, RDY	O*	X, Y Read Data: differential read signal output.
WC	-	Write Current: used to set the magnitude of the write current.
VCT	-	Voltage Center Tap: voltage source for head center tap.
VCC	-	+5V
GND	-	Ground
* When more than one R/W device is used, these signals can be wire OR'ed with unselected R/W devices.		

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

All voltages referenced to GND. Currents into device are positive.

PARAMETER		RATING
DC Supply Voltage	VCC	-0.3 to +6 VDC
Digital Input Voltage Range HS1, HS0, WDI, R/$\overline{W}$, $\overline{CS}$		-0.3 to (VCC + 0.3 VDC)
Head Port Voltage Range	VH	-0.3 to (VCC + 3.0 VDC)
Write Current Pin Voltage	Vwc	-0.3 to (VCC + 0.3 VDC)
WUS Pin Voltage Range	Vwus	-0.3 to +6.0 VDC
Write Current Zero–Peak	IW	60 mA
RDX, RDY Output Current	Io	-10 mA
RDX, RDY Pin Voltage		VCC + 0.3 VDC
VCT Output Current Range	IVCT	-60 mA to +10 mA
WUS Output Current Range	Iwus	-0.1 mA to +10 mA
Storage Temperature Range	Tstg	-65 to 150°C
Package Temperature (20 sec Reflow)		215°C

ELECTRICAL SPECIFICATIONS (continued)

RECOMMENDED OPERATION CONDITIONS

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
DC Supply Voltage	VCC		4.75	5.0	5.25	VDC
Head Inductance	Lh		1		15	µH
Write Current Range	IW		15		50	mA
Junction Temperature Range	Tj		+25		+135	°C

DC CHARACTERISTICS

Unless otherwise specified, recommended operating conditions apply.

POWER SUPPLY

VCC Supply Current (ICC)	Read Mode		33	44	mA
	Idle Mode		1.4	2.0	mA
	Write Mode		31 + Iw	44 + Iw	mA
Power Dissipation	Read Mode		165	227	mW
	Idle Mode		7	10.5	mW
	Write Mode		155 + 5 Iw	230 + 5.5 Iw	mW

DIGITAL I/O

Input Low Voltage $\overline{CS}$, R/$\overline{W}$ WDI, HS0, HS1	VIL				0.8	VDC
Input High Voltage $\overline{CS}$, R/$\overline{W}$ WDI, HS0, HS1	VIH		2.0			VDC
Input Low Current $\overline{CS}$, R/$\overline{W}$ WDI, HS0, HS1	IIL	VIL = 0.4V	-0.4			mA
Input High Current $\overline{CS}$, R/$\overline{W}$ WDI, HS0, HS1	IIH	VIH = 2.7V			20	µA
WUS Output Low Voltage	VOL	IOL = 4.0 mA			0.5	VDC
WUS Output High Current	IOH	VOH = 5.0V			100	µA

WRITE MODE

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Center Tap Voltage VCT	Write Mode/Idle Mode		Vcc - 0.9		VDC
Head Current (per side)	Write Mode, Voltage Fault $0 \leq VCC \leq 3.9V$	-200		200	µA
Write Current Range	$1.0\ k\Omega \leq Rwc \leq 3.3\ k\Omega$	15		50	mA
Write Current Constant "K"		46	50	54	mA-kΩ
Iwc to Head Current Gain			20		mA/mA
Unselected Head Leakage Current				85	µA
RDX, RDY Common Mode Output Voltage		Vcc - 3	Vcc - 2.4	Vcc - 2	VDC
WDI Minimum Pulse Width	PWH VIL ≥ 0.2V		11		ns
See Figure 1	PWL VIN ≥ 2.4V		4		ns

READ MODE

Center Tap Voltage VCT			Vcc - 1.5		VDC
Input Bias Current (per side)	From VCT to HnX or HnY		20	60	µA
Output Offset Voltage	RDX - RDY	-200		+200	mV
Common Mode Output Voltage	$\frac{RDX + RDY}{2}$	2	Vcc - 2.4	3.5	VDC
Common Mode Output Voltage Change from Write to Read Mode		-100		+100	mV

FAULT DETECTION CHARACTERISTICS
Unless otherwise specified recommended conditions apply, Iw = 30 mA, Lh = 5 µH, F(WDI) = 10 MHz.

Minimum Rate of WDI Input for Safe condition		150			kHz
Maximum Rate of WDI Input for Unsafe condition				50	kHz
Minimum voltage value for guaranteed write current turn-on		4.4			VDC
Maximum voltage value for guaranteed write current turn-off				3.9	VDC

ELECTRICAL SPECIFICATIONS (continued)

DYNAMIC CHARACTERISTICS AND TIMING

Unless otherwise specified, recommended operating conditions apply and Iw = 30 mA, Lh = 5 µH, f(WDI) = 5 MHz, CL(RDX, RDY) ≤ 20 pF.

WRITE MODE

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Differential Head Voltage Swing		6.0	6.4		V(pk)
Unselected Head Transient Current	1 µH ≤ Lh ≤ 9.5 µH			2	mA(pk)
Differential Output Capacitance				15	pF
Differential Output Resistance	(1203AR only)	600		960	Ω

READ MODE

Differential Voltage Gain	Vin = 1 mVrms @ 1 MHz	200	250	300	V/V
Bandwidth (-3dB)	|Zs| < 5Ω, Vin = 1 mVpp	30	60		MHz
Input Noise Voltage	BW = 15 MHz, Lh = 0, Rh = 0		0.85	1.2	nV/√Hz
Differential Input Capacitance	Vin = 1 mVrms, f = 5MHz		16	19	pF
Differential Input Resistance			2		kΩ
Dynamic Range	AC input voltage where gain falls to 90% of its small signal gain value, f = 5 MHz	2			mVpp
Common Mode Rejection Ratio	Vcm = 100 mVpp @ 1 MHz < f < 10 MHz	50	75		dB
Power Supply Rejection Ratio	ΔVcc =100 mVpp @ 1 MHz < f < 10 MHz	45			dB
Channel Separation	Unselected Channels: Vin = 20 mVpp 1 MHz < f < 10 MHz	45	54		dB
RDX, RDY Single Ended Output Resistance				30	Ω
Output Current	AC Coupled Load, RDX to RDY	±1.5			mA

SWITCHING CHARACTERISTICS

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
R/W	Read to Write	R/W to 90% of write current		50	400	ns
	Write to Read	R/W to 90% of 100 mV 10 MHz read signal envelope or to 10% IW		0.15	1.0	µs
CS	Unselect to Select	$\overline{CS}$ to 90% of 100 mV 10 MHz read signal envelope		1.0	2.0	µs
	Select to Unselect	$\overline{CS}$ to 10% Ih		0.05	0.6	µs
HS0, 1 to any Head		To 90% of 100 mV 10 MHz read signal envelope			0.6	µs
WUS	Safe to Unsafe (TD1)	(1203A only)	3.5		20	µs
		(1203AR only)	7.0		30	µs
	Unsafe to Safe (TD2)	Write mode, after fault cleared after 2nd transition			350	ns
Head Current		Rh = 0, Lh = 0				
	Prop. Delay (TD3)	From 50% points		25	40	ns
	Asymmetry	WDI has 50% Duty Cycle and 1 ns Rise/Fall Time			2	ns
	Rise/Fall Time	10% - 90% Points		4	20	ns

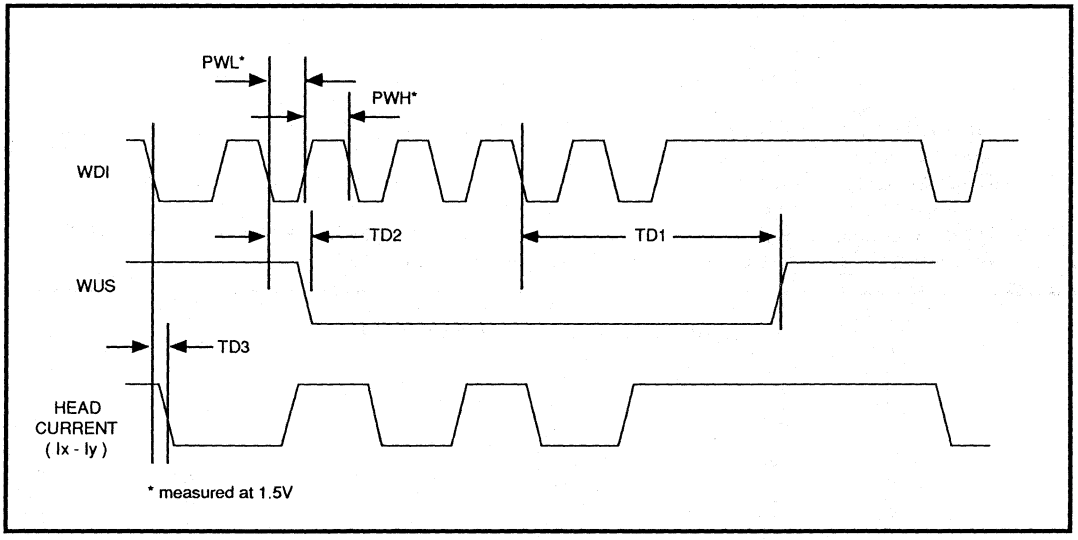
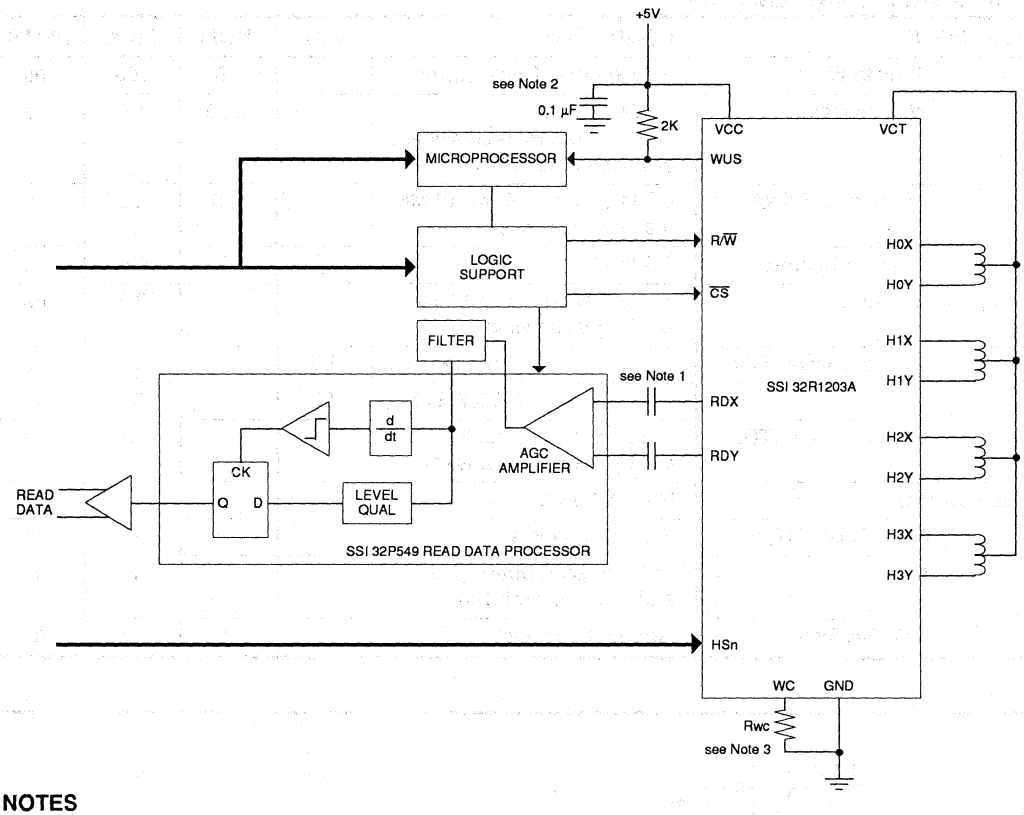


FIGURE 1: Write Mode Timing Diagram



NOTES

1. Limit DC current from RDX and RDY to 100 µA and load capacitance to 20 pF. In multi-chip application these outputs can be wire-OR'ed.
2. The power bypassing capacitor must be located close to the 32R1203A with its ground returned directly to device ground, with as short a path as possible.
3. To reduce ringing due to stray capacitance this resistor should be located close to the 32R1203A. Where this is not desirable a series resistor can be used to buffer a long WC line.

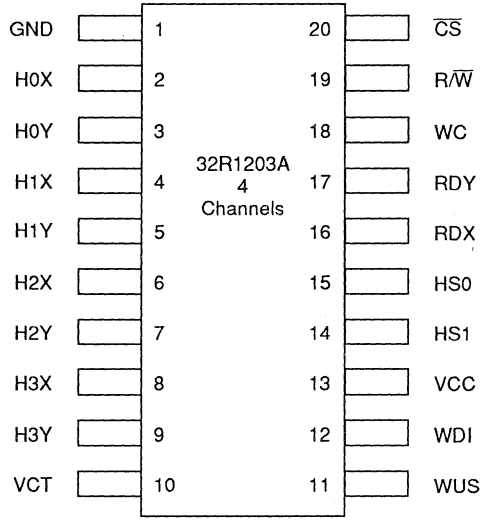
FIGURE 2: Applications Information

PACKAGE PIN DESIGNATIONS

(Top View)

THERMAL CHARACTERISTICS: θjA

20-Lead SOL, SOV	96° C/W



20-Lead SOL, SOV

CAUTION: Use handling procedures necessary for a static sensitive component.

ORDERING INFORMATION

PART DESCRIPTION	ORDERING NUMBER	PACKAGE MARK
SSI 32R1203A		
20-Lead SOL	SSI 32R1203A-CL	SSI 32R1203A-CL
20-Lead SOV	SSI 32R1203A-CV	SSI 32R1203A-CV
SSI 32R1203AR		
20-Lead SOL	SSI 32R1203AR-CL	SSI 32R1203AR-CL
20-Lead SOV	SSI 32R1203AR-CV	SSI 32R1203AR-CV

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Notes:

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SSI 32R1510BR
MR Head Read/Write Device

Advance Information

December 1993

DESCRIPTION

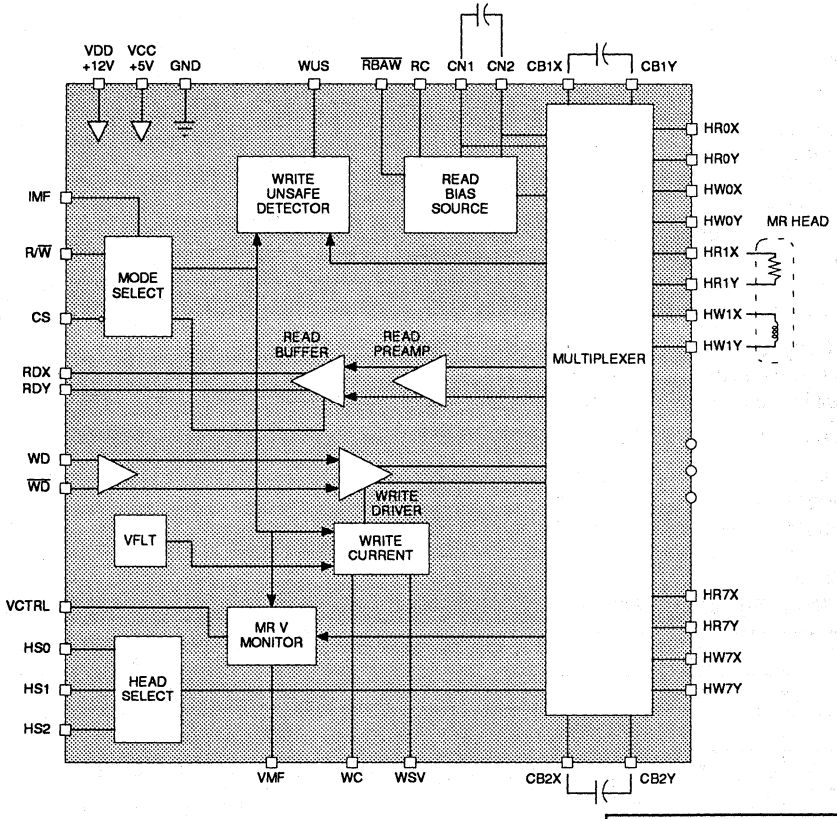
The SSI 32R1510BR is an integrated circuit designed for use with Magneto-Resistive recording heads. It provides a write driver and a low noise read amplifier for up to 8 channels. The device requires +12V and +5V power supplies and comes in a 68-pin PLCC package.

FEATURES

- **Head Swing = 7.0 Vpp min**
- **Rise Time = 4 ns (Typ)**
- **Minimal external components**
- **Input Noise = 0.72 nV/ √ Hz**

3

BLOCK DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

FUNCTIONAL DESCRIPTION

The SSI 32R1510BR addresses up to 8 MR heads providing write drive or read amplification and MR current biasing. Head selection and mode control is accomplished with pins HSn, $\overline{CS}$ and R/$\overline{W}$ as shown in Tables 1 and 2.

WRITE MODE

Taking both $\overline{CS}$ and R/$\overline{W}$ low selects Write mode which configures the 32R1510BR as a current switch and activates the Write Unsafe (WUS) detect circuitry. Head current direction corresponds to the write data input level (WDX, WDY).

The magnitude of the write current is given by:

$$Iw = Vwc/Rwc$$

Rwc is connected from pin WC to GND. Note the actual head current Ihead is given by:

$$Ihead = Aw \cdot Iw/(1+Rh/Rd)$$

where Aw is the write current gain, Rh is the head resistance, and Rd is the damping resistance.

WRITE MODE FAULT DETECT CIRCUIT (WUS)

Any of the following conditions will be indicated as a high level on the Write Unsafe, WUS open collector output:

- WDI frequency too low
- Device in Read or Idle mode
- Head open
- Head short to ground
- No Head current

In the case of a head short to ground, write current will be turned off to prevent excessive current dissipation. This will result in a pulsating WUS signal.

LOW VOLTAGE FAULT PROTECT

The voltage fault detection circuit improves data security by disabling the write current generator during a low voltage fault or power startup regardless of mode. Note that WUS does not necessarily turn on to flag a power supply fault condition.

READ BIAS ACTIVE IN WRITE ($\overline{RBAW}$)

The $\overline{RBAW}$ pin is a TTL control signal. A low level enables the MR bias current through the selected head in Write mode (Table 3). It can be used to speed up the write to read transition time. $\overline{RBAW}$ timing is shown in Figure 2.

READ MODE

Taking $\overline{CS}$ low and R/$\overline{W}$ high selects Read mode which activates the bias current generator and the differential amplifier. The magnitude of the bias current is given by:

$$Ib = Ar \cdot Vrc/Rrc$$
$$= Kr/Rrc$$

where Ar is the bias current gain and Kr is the product of Ar and Vrc. Rrc is connected from pin RC to GND.

A voltage monitor, VMF, is provided for media biasing. In Read mode its output is set at the head bias voltage Vmr. When VMF sources over 7.5 mA, the chip assumes the media is not biased correctly, then the device turns off Read mode, and WUS flags low to indicate incorrect media biasing.

RDX and RDY are open collector outputs and should be terminated with 100Ω load resistors.

IDLE MODE

Taking $\overline{CS}$ high selects Idle mode which switches the RDX and RDY outputs into a high impedance state and deactivates the internal write current source. This facilitates multi-device installations by allowing the read outputs to be wire OR'ed.

APPLICATION CAUTION

Care should be used when powering up the 32R1510R. An ESD protection diode is connected between VCC and VDD on the chip. If VCC is powered up before VDD, the ESD diode can suffer irreversible breakdown and damage the device permanently.

TABLE 1: Mode Select/VMF Select

$\overline{CS}$	R/$\overline{W}$	VCTRL	MODE	VMF VALUE
0	0	X	Write	Dummy Head Center Voltage
0	1	X	Read	Selected Channel Center Voltage
1	X	0	Idle	High Impedance
1	X	1	Idle	Dummy Head Center Voltage

TABLE 2: Head Select

Head Selected	HS2	HS1	HS0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

TABLE 3: Read Bias Active in Write

MODE	R/$\overline{W}$	$\overline{RBAW}$	MR Head Bias Current
Read	1	X	On
Write	0	0	On
	0	1 or Open	Off

PIN DESCRIPTION

CONTROL INPUT PINS

NAME	TYPE	DESCRIPTION
$\overline{CS}$	I	Chip Select Input. A logical low level enables the circuit for a read or write operation. Has internal pull up.
R/$\overline{W}$	I	Read/write select. A logical low level enables the Write mode (when $\overline{CS}$ is low). Has internal pull up.
VCTRL	I	Voltage Control. In Idle mode, a high level selects VMF to supply a bias value. A low level selects high impedance.
$\overline{RBAW}$	I	Read Bias Active In Write. A TTL low level enables the MR bias current through the selected head in both Read & Write modes.
HS0, HS1, HS2	I	Head select inputs. Logical combinations select one of eight heads. See Table 2. Has internal pull down resistors.

HEAD TEMINAL PINS

HR0X - HR7X HR0Y - HR7Y	I	MR read element X, Y connections.
HW0X - HR7X HW0Y - HR7Y	O	MR write element X, Y, connections

DATA INPUT/OUTPUT PINS

WDX, WDY	I	Differential write data input.
RDX, RDY	O	Differential Read Data output. These open collector outputs are normally terminated in 100Ω resistors to VCC.

EXTERNAL COMPONENT CONNECTION PINS

WC	I/O	Resistor connected to GND to provide desired value of write current.
RC		Resistor connected to GND to provide selected value of bias current.
CN1, CN2		Noise decoupling capacitor for MR bias source.
CB1X, CB1Y CB2X, CB2Y		DC blocking capacitors.

PIN DESCRIPTION (continued)

CIRCUIT MONITOR PINS

NAME	TYPE	DESCRIPTION
WUS	O	Write Unsafe is an open-collector output with the off-state indicating that conditions are not proper for a write operation.
WSV	O	Write Select Verify. Indicates that write current generator is active.
IMF	O	Current Monitor. Sinks 3 mA of current when device is actiive.
VMF	O	Voltage Monitor. Provides equivalent voltage to MR element bias midpoint [(V(HRnX) - V(HRnY))/2].

POWER, GROUND PINS

VCC	I	+5V logic circuit supply.
VDD	I	+12V power supply.
GND	I	Power supply common.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation beyond the maximum ratings may damage the device.

PARAMETER	RATING
Storage Temperature	-65 to 150°C
Junction Operating Temperature	+130°C
Positive Supply Voltage (VCC)	-0.3 to 6V
Positive Supply Voltage (VDD)	-0.3 to 14.0V
Voltage Applied to Logic Inputs	-0.3V to Vcc+0.3V
All other Pins	-0.3V to Vcc+0.3V

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, 4.5V ≤ 5.5V, 10.8V ≤ VDD ≤ 13.2V, 0°C ≤ Ta ≤ 70°C.

Current maximums are currents with the highest absolute value.

POWER DISSIPATION

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VCC Supply Current	Read Mode, Isense = 8.5 mA		12	17	mA
	Write Mode Iw = 30 mA		18	25	mA
	Idle Mode		7	10	mA
VDD Supply Current	Read Mode, Isense = 8.5 mA		34+ Is • 1.25	44+ Is • 1.25	mA
	Write Mode Iw = 30 mA $\overline{RBAW}$ = High		34+Iw	46+Iw	mA
	Idle Mode		26	36	mA
Power Dissipation	Read Mode Isense = 8.5 mA		520 + 1.25 • Is • VDD		mW
	Write Mode Iw = 30 mA $\overline{RBAW}$ = High		570 + (VDD - 2) • Iw		mW
	Idle Mode		340		mW

DIGITAL INPUTS AND OUTPUTS

WSV, WUS Output low Voltage	Iload = 4 mA			0.5	V
Input low voltage (VIL1) ($\overline{CS}$,R/$\overline{W}$,VCTRL,$\overline{RBAW}$,HS0-HS2)		-0.3		0.8	V
Input high voltage (VIH1) ($\overline{CS}$,R/$\overline{W}$,VCTRL,$\overline{RBAW}$,HS0-HS2)		2.0		Vcc+0.3	V
Input low current (IIL1) ($\overline{CS}$,R/$\overline{W}$,VCTRL,$\overline{RBAW}$,HS0-HS2)	VIL1 = 0.8V	-0.4			mA
Input high current (IIH1) ($\overline{CS}$,R/$\overline{W}$,VCTRL,$\overline{RBAW}$,HS0-HS2)	VIH1 = 2.0V			100	µA
Input low Voltage (VIL3) (WDX, WDY)		Vcc-2.2		VIH3-0.3	V
Input high Voltage (VIH3) (WDX, WDY)		VIL3 +0.3V		Vcc-0.5	V
Input low current (IIL3) (WDX, WDY)	VIL3=Vcc-1.4			50	µA
Input high current (IIH3) (WDX, WDY)	VIH3 = Vcc-0.8			50	µA

ELECTRICAL SPECIFICATIONS (continued)

ANALOG OUTPUT

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
IMF Current	$\overline{CS}$ = 0	2.4	3	3.6	mA
IMF Current	$\overline{CS}$ = 1			0.1	mA
VMF Current	Sourcing	2.5			mA
	Sinking	0.8			mA
VMF Over Current Protection		7.5			mA
Voltage Monitor Output (VMF)	Read mode	Vmr-0.1	Vmr	Vmr+0.1	V
	Write in	4.5	5.5	6.5	V
	Idle mode, VCTRL = 1	4.5	5.5	6.5	V
VMF Voltage Difference	VMF_{READ} - VMF_{WRITE}	-0.3		0.3	V

READ MODE

Test performed with 100Ω lead resistors from RDX & RDY to VCC

Read Bias Current Gain (Ar)	Read Mode		12		mA/mA
	Idle Mode			0.01	mA/mA
Bias current setting Voltage (Vrc)		1.9	2.0	2.1	V
"Kr" Factor	Kr=Ar • Vrc	22	24	26	V
Ih Bias Current (MR Element Bias Current)	Read Mode	6		12	mA
Unselected bias Current				10	uA
MR Head Bias Voltage (Vmr)	Selected Channel (Read)	4.3	5.5	6.7	V
	Unselected Channel (Read)		4.9		V
	Write, Idle Mode		4.9		V
MR Head Resistance (Rh)		20	36	55	Ω
Differential Gain		110	150	190	V/V
Differential Input Resistance		200	400	800	Ω
Dynamic Range	Input Voltage where gain falls to 90% of its small signal gain value f = 5 MHz	8			mVpp
Input Referred Noise Voltage			0.72	0.95	nV/√ Hz
Differential Input Capacitance			18		pF
Bandwidth	-3 dB, Vin = 1 mVpp Zs = 5Ω	70	100		MHz
CMRR	Vin = 100 mVpp @ 5 MHZ	55			dB
PSRR	100 mVpp @ 5 MHZ on VCC, VDD	50			dB
Channel Separation		45			dB

READ MODE (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Output Offset Voltage		-300		300	mV
Output Voltage (Common mode)			Vcc-0.6		VDC
Output Leakage Current	$\overline{CS}$ = 1			100	µA

WRITE MODE

Write Current gain (Aw)	Rh = 0	0.92	0.99	1	mA/mA
Write Current Voltage, Vwc		1.9	2.0	2.1	V
Write Current range		10		50	mA
Differential Head Voltage Swing		7.0	8.0	9.0	Vpp
Unselected Head current	DC			0.2	mA
	AC			1	mApp
Head differential load resistance		360	450	540	Ω
VDD Fault Voltage		8.5	9.2	10.0	VDC
VCC Fault Voltage		3.5	3.9	4.2	VDC
Head Current (HnX, HnY)	Write Mode, 0 ≤ VCC ≤ 3.5V 0 ≤ VDD ≤ 8.5V	-200		+200	µA
	Read/Idle Mode 0 ≤ VCC ≤ 5.5V 0 ≤ VDD ≤ 13.2V	-200		+200	µA

SWITCHING CHARACTERISTICS

Conditions: Rh = 36Ω, CB1 = CB2 = 0.047 µF, CN = 0.47 µF, Is = 8.5 mA, Iw = 30 mA, T mode = 1 ms

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Head Switching	to ± 0.1V of Read DC and 90% of Read Envelope		1.5	3	µs
Write-Read Mode RBAW = 1	to ± 0.1V of Read DC and 90% of Read Envelope		1.5	2.5	µs
Write-Read Mode RBAW = 0	to ± 0.1V of Read DC and 90% of Read Envelope		0.5	1.5	µs
Read-Write Mode	to 90% of Write Current		0.2	0.5	µs
Idle-Read/Write Mode	to ± 0.1V of Read DC and 90% of Read Envelope		5	10	µs
Read/Write - Idle Mode			0.2	0.5	µs
WUS Safe to Unsafe (TD1)	WDI Frequency too low	0.3	0.7	1.5	µs
WUS Unsafe to Safe (TD2)			0.1	0.3	µs
WSV Delay Time	50% R/W to 50% WSV			0.5	µs
IMF Delay Time	50% CS/ to 50% IMF Current			0.5	µs

ELECTRICAL SPECIFICATIONS (continued)

SWITCHING CHARACTERISTICS (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Write Current Rise/Fall time	Lh = 200 nH Rh = 15 Ω Iw = 30 mA		4	5	ns
Propagation delay	50%(WDX-WDY) to 50%(Ix-Iy)		4		ns
Write current Asymmetry	Propagation delay difference			0.5	ns

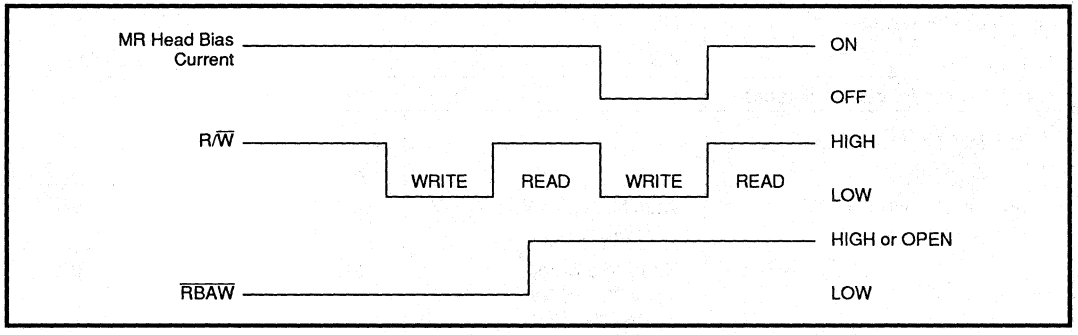


FIGURE 2: Head Bias Current Timing

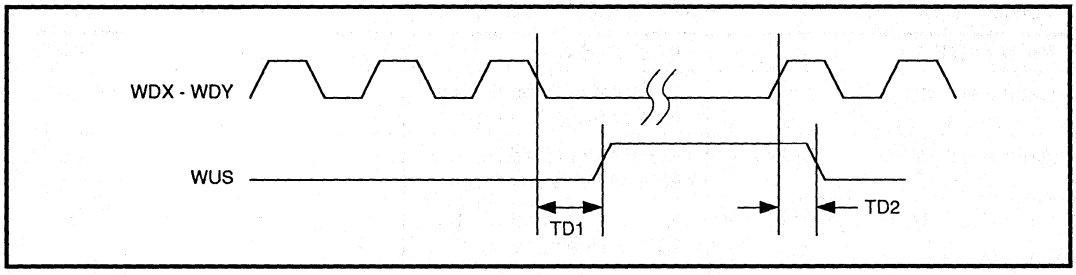
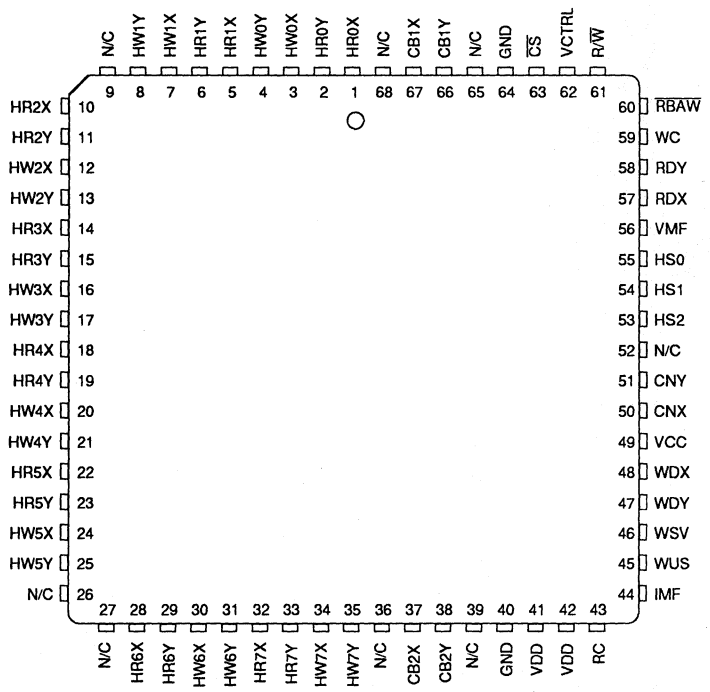


FIGURE 3: WUS Timing

PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



68-Pin PLCC

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Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

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Notes:

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SSI 32R1540R
6-Channel MR Read/Write Amplifier
Target Specification

January 1994

3

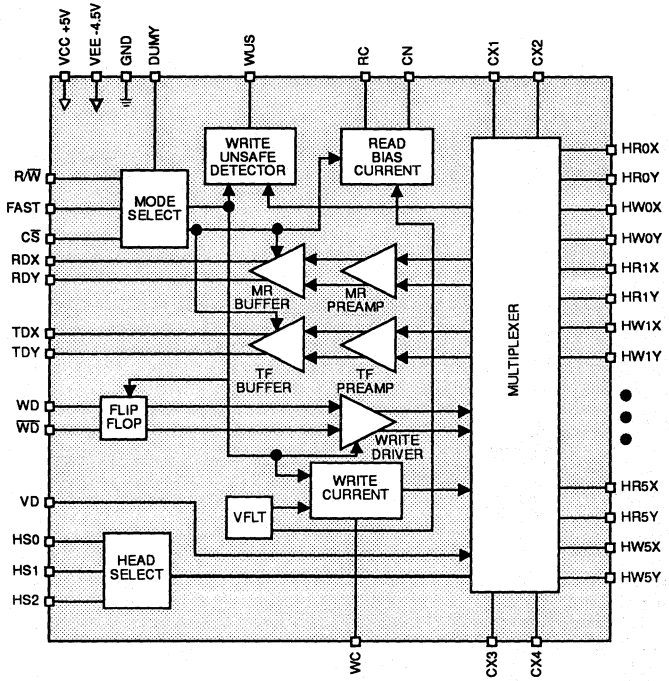
DESCRIPTION

The SSI 32R1540R is a BiCMOS monolithic integrated circuit designed for use with four-terminal, Magneto-Resistive recording heads. It provides a write driver, MR read bias current, low noise read amplifiers for both the MR and inductive thin-film heads, and fault detection circuitry for up to six channels. The device requires +5V and -4.5V power supplies and comes in a 64-Lead TQFP package.

FEATURES

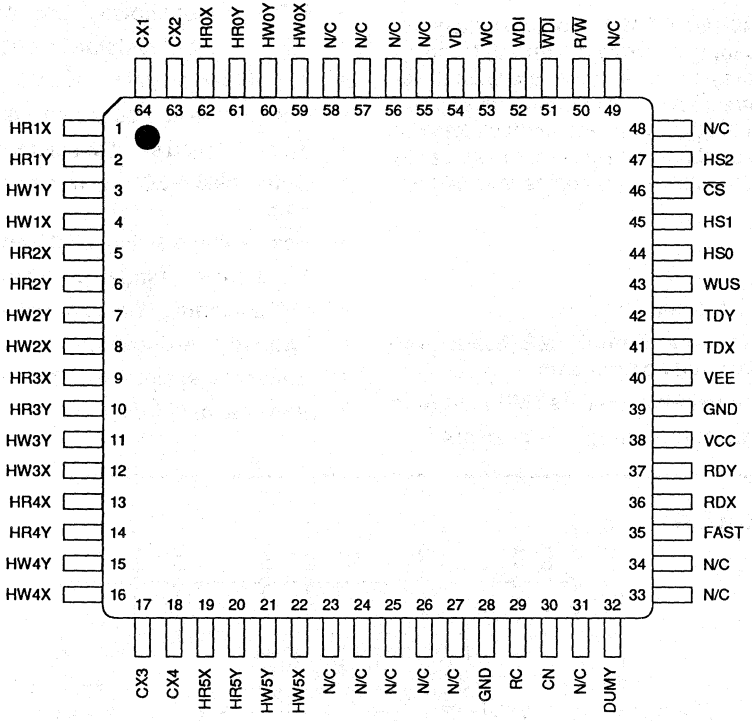
- +5V, -4.5V ±10% supply
- Designed for four-terminal MR heads with minimum external components
- Truly differential I-bias/V-sense MR read Amp
- MR head bias current range = 10 - 26 mA
- MR read gain = 250 V/V
- MR read input noise = 0.65 nV√Hz (Nom)
- MR read input resistance = 900Ω (Nom)
- Thin-film read gain = 300 V/V
- Thin-film read input noise = 0.48 nV√Hz (Nom)
- Thin-film read input capacitance = 12 pF (Nom)
- Differential PECL write data input with Flip-Flop
- Head voltage swing = 7.0 Vpp (Nom)
- Write current range = 5 - 30 mA
- Self-switching damping resistance
- Write unsafe detection
- Enhanced system write to read recovery time
- Power supply fault protection

BLOCK DIAGRAM



SSI 32R1540R
6-Channel MR
Read/Write Amplifier

PACKAGE PIN DESIGNATIONS
(Top View)



64-Lead TQFP

CAUTION: Use handling procedures necessary for a static sensitive component.

Target Specification: The target specification is intended as an initial disclosure of specification goals for the product. The specifications are based on design goals, subject to change and are not guaranteed. Silicon Systems assumes no obligation regarding future manufacture unless agreed to in writing.

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SSI 32R2010R
10-Channel Thin Film Read/Write Device

December 1993

3

DESCRIPTION

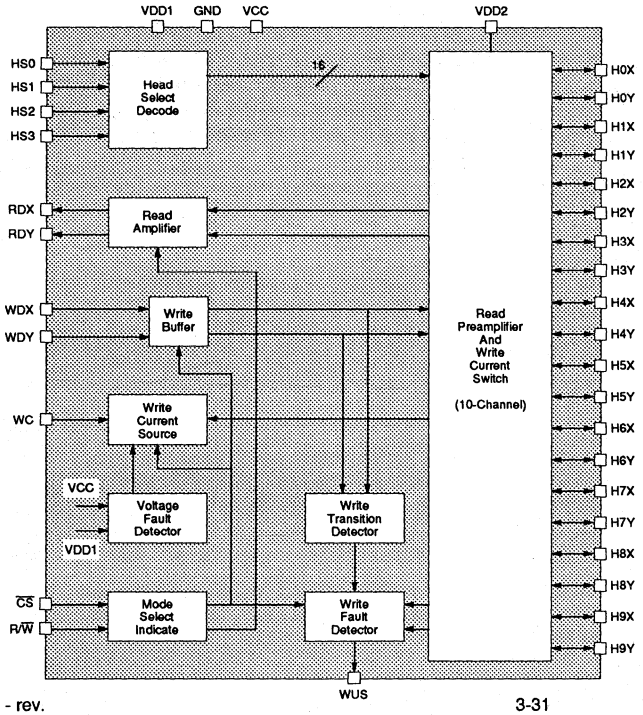
The SSI 32R2010R is an integrated read/write circuit designed for use with two terminal heads in disk drive systems. The device contains up to ten channels of read amplifiers and write drivers and also has an internal write current source. An internal 300Ω damping resistor is supplied in Write mode, which is switched to 1 kΩ in Read mode.

The circuit operates on +5V and +12V power supplies and is available in a 10-channel, 36-pin SO package.

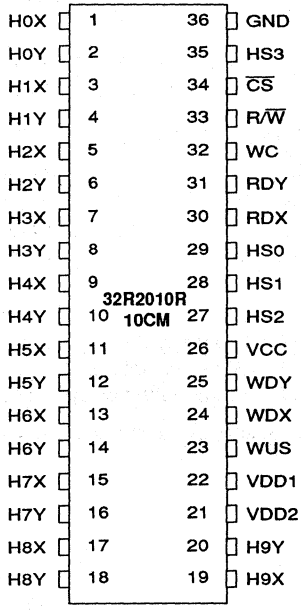
FEATURES

- **High performance**
  - **Read Mode Gain = 150 Typ V/V**
  - **Input Noise = 0.58 nV/√Hz typ.**
  - **Input Capacitance = 15 pF typ.**
  - **Write Current Range = 10 mA to 25 mA**
  - **Write Current Rise Time = 4 ns**
  - **Head Voltage Swing = 7 Vpp min**
- **Write unsafe detection**
- **Differential, ECL-like write data input**
- **Open collector read data output**
- **Switch from 300Ω damping resistor to 1 kΩ read input resistance**
- **Power supply fault protection**
- **+5V, +12V power supplies ±10%**

BLOCK DIAGRAM



PIN DIAGRAM



36-Lead SOM

CAUTION: Use handling procedures necessary for a static sensitive component.

FUNCTIONAL DESCRIPTION

The SSI 32R2010R addresses up to 10 channels with logic control inputs which are TTL compatible. Head selection is accomplished as shown in Table 1. Mode selection is accomplished as shown in Table 2. The mode select inputs have internal pull up circuits so that if an input is open it will rise to the upper logic level and force the device into a non-writing condition.

WRITE MODE

In Write Mode (R/$\overline{W}$ and $\overline{CS}$ low) the circuit functions as a current switch. The Head Select Inputs HS0, HS1, HS2 and HS3 determine the selected head. The write data inputs (WDX, WDY) determine the polarity of the head current. When WDX is high and WDY is low, write current is in the X direction. HNX is sinking current.

The write current magnitude is adjusted by an external resistor, Rwc, from WC to GND, and is given by:

$$Iw = Vwc/Rwc$$

Note that actual head current, Ihd, is:

$$Ihd = Iw/(1+\frac{Rh}{Rd}) + Ioffset$$

where Rh is head resistance, Rd is write damping resistance and Ioffset is a constant DC offset current.

WRITE MODE FAULT DETECT CIRCUIT

Several circuits are dedicated to detecting fault conditions associated with the write mode. A logical high (off) level will be present at the Write Unsafe (WUS) terminal if any of the following write fault conditions are present:

- Open head circuit (Iw ≥ 20 mA)
- Head shorted to ground
- Write current transition frequency too low
- Write mode not logically selected

A head shorted to ground condition results in a pulsating WUS signal.

After the fault condition is removed, two transitions of the write data input lines are required to clear WUS. The Write Unsafe output is open-collector and is usually terminated by an external resistor connected to VCC.

Additionally, power voltage monitoring circuits are used to detect VCC and VDD1 voltage levels. If either is too low to permit valid data recording, write current is inhibited.

READ MODE

In Read Mode, (R/$\overline{W}$ high and $\overline{CS}$ low), the circuit functions as a low noise differential amplifier. The read amplifier input terminals are determined by the Head Select inputs. The read amplifier outputs (RDX, RDY) are open collector, requiring external load resistors connected to VCC. The amplifier gain polarity is non-inverting between HnX, HnY inputs and RDX, RDY outputs.

The switch from write to read modes also changes the resistance across HnX and HnY from its write damping value of 300Ω to its read mode input value of 1 kΩ.

IDLE MODE

Taking $\overline{CS}$ high selects the idle mode which switches the RDX and RDY outputs into a high impedance state and deactivates the internal write current source. This facilitates multi device installations by allowing the read outputs to be wired OR'ed and the write current programming resistor to be common to all devices.

TABLE 1: Head Select

Head Selected	HS3	HS2	HS1	HS0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

TABLE 2: Mode Select

$\overline{CS}$	R/$\overline{W}$	Mode
0	0	Write
0	1	Read
1	0	Idle
1	1	Idle

PIN DESCRIPTION

CONTROL INPUT PINS

NAME	TYPE	DESCRIPTION
$\overline{CS}$	I	Chip Select Input. A logical low level enables the circuit for a read or write operation. Has internal pull up.
R/$\overline{W}$	I	Read/write select. A logical low level enables the write mode (when $\overline{CS}$ is low). Has internal pull up.
HS0, HS1, HS2, HS3	I	Head select inputs. Logical combinations select one of sixteen heads. See Table 1. Has internal pull down resistors.
HEAD TERMINAL PINS		
H0X-H9X, H0Y-H9Y	I/O	X, Y Head connections: Current in the X-direction flows into the X-port.
DATA INPUT/OUTPUT PINS		
WDX, WDY	I/O	Differential write data input.
RDX, RDY	I/O	Differential Read Data output. These open collector outputs are normally terminated in 100Ω resistors to VCC.
EXTERNAL COMPONENT CONNECTION PINS		
WC	I/O	Resistor connected to GND to provide desired value of write current.
CIRCUIT MONITOR PINS		
WUS	O	Write Unsafe is an open-collector output with the off-state indicating that conditions are not proper for a write operation.
POWER, GROUND PINS		
VCC	I	+5V Logic circuit supply.
VDD1	I	+12V power supply.
VDD2	I	Positive power supply for write current drivers.
GND	I	Power supply common.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may permanently damage the device.

PARAMETER	RATING
Positive Supply Voltage, VCC	6 VDC
Supply Voltage, VDD1, 2	13.5 VDC
Operating Junction Temperature	+130°C
Storage Temperature	-65 to +130°C
Package Temperature (20 sec. reflow)	215°C
Input Voltages	
HS0, HS1, HS2, HS3, $\overline{CS}$, R/$\overline{W}$	-0.2 to VCC + 0.2 VDC
Outputs	
Read Data (RDX, RDY)	VCC -2.5 to VCC + 0.3 VDC
Write Unsafe (WUS)	-0.2V to VCC + 0.2V VDC
Current Reference (WC)	-80 mA to 1.0 mA VDC
Head Outputs (Write Mode)	-80 mA to 1.0 mA mA

POWER SUPPLY

Unless otherwise specified, 4.5V ≤ VCC ≤ 5.5V, 10.8V ≤ VDD1, 2 ≤ 13.2V, 0°C ≤ T (ambient) ≤ 70°C.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Power Dissipation (Does not include power dissipation through RDX, RDY load resistors)	Idle mode		195	295	mW
	Read mode		440	775	mW
	Write mode		350 + 10 Iw	530 + 11.2 Iw	mW
Positive Supply Current ICC (Includes RDX, RDY currents)	Idle Mode		13	20	mA
	Read Mode		27	35	mA
	Write Mode		22	26	mA
Positive Supply Current IDD1	Idle Mode		10	12	mA
	Read Mode		32	42	mA
	Write Mode		23	28	mA
Positive Supply Current IDD2	Idle Mode		0.5	2	mA
	Read Mode		1	1.5	mA
	Write Mode		1 + Iw	2 + Iw	mA

DC CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
High-level Input Voltage VIH ($\overline{CS}$, R/$\overline{W}$, HS0, HS1, HS2, HS3)		2.0		-	V
Low-level Input Voltage VIL ($\overline{CS}$, R/$\overline{W}$, HS0, HS1, HS2, HS3)				0.8	V
High-level Input Current IIH ($\overline{CS}$, R/$\overline{W}$, HS0, HS1, HS2, HS3)	VIH = 2.7V			100	µA
Low-level Input Current IIL ($\overline{CS}$, R/$\overline{W}$, HS0, HS1, HS2, HS3)	VIL = 0.4V			-400	µA
High-level Output Voltage VIH (WDX, WDY)		Vcc - 1.0		Vcc - 0.72	V
Low-level Output Voltage VIL (WDX, WDY)		Vcc - 1.87		Vcc - 1.625	V
WUS, Low Level Voltage	ILUS = 4 mA (denotes safe condition)			0.5	V
WUS, High Level Current	VHUS = 5.0V (denotes unsafe condition)			100	µA

WRITE MODE

Test Conditions (Unless otherwise specified). VCC = 4.5 to 5.5V, Ta = 0 to +70°C, VDD = 10.8 to 13.2V, Lh = 470 nH, Rh = 25Ω, WD Tr, Tf < 2 ns, Iw = 20 mA.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Current Range, Iw		10		25	mA
Write Current Voltage, Vwc		1.95	2.05	2.15	V
Differential Head voltage Swing		7.0	7.6		Vpp
Ioffset			0.5		mA
Unselected Head Transient Current	Non adjacent heads tested to minimize external coupling effects			1	mA(pk)
Head Damping Resistance		240	300	360	Ω
Differential Output Capacitance				20	pF

ELECTRICAL SPECIFICATIONS (continued)

FAULT DETECTION CHARACTERISTICS

Test conditions same as Write Mode above (unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VCC Value for Write Current Turn off	Ih < 1 mA	3.7	4.0	4.3	V
VDD Value for Write Current Turn off	Ih < 1 mA	8.8	9.5	10.2	V
WDX, WDY Transition Frequency	WUS = Low (Guaranteed safe)	1.0			MHz

READ MODE

Tests performed with 100Ω load resistors from RDX and RDY to VCC. Test conditions same as Write mode (unless otherwise specified.)

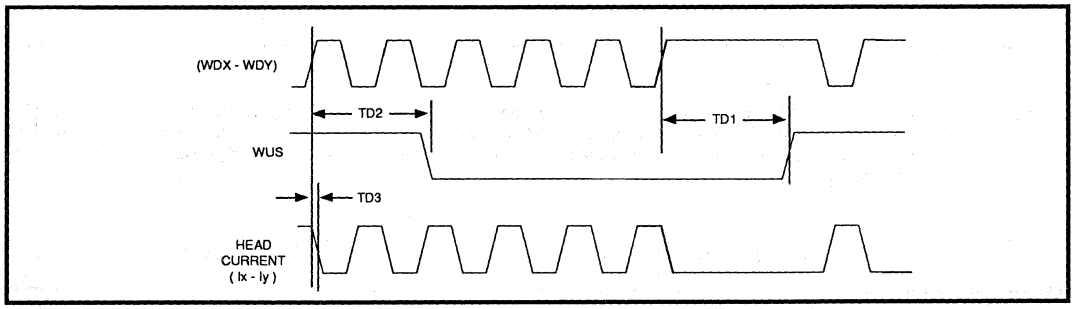
PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Differential Voltage Gain		Vin = 1 mVpp, f = 300 kHz	120	150	180	V/V
Voltage Bandwidth	-3 dB	Zs < 5Ω, Vin = 1 mVpp	50	65		MHz
	-1 dB	Zs < 5Ω, Vin = 1 mVpp	20	35		MHz
Input Noise Voltage		Zs = 0Ω , Vin = 0V, Power Bandwidth = 20 MHz		0.58	0.75	nV/√Hz
Differential Input Capacitance		Vin = 0V, f = 5 MHz		15	20	pF
Differential Input Resistance		Vin = 0V, f = 5 MHz	400		1500	Ω
Dynamic Range @ 5 MHz		Input voltage where AC gain falls to 90% of the gain	4			mVpp
Common Mode Rejection Ratio		Vin = 100 mVpp, 0V DC f = 5 MHz	60	90		dB
Power Supply Rejection Ratio		VCC or VDD = 100 mVpp f = 5 MHz	55	75		dB
Channel Separation		Unselected channels are driven with Vin = 20 mVpp @ 5 MHz	60	90		dB
Output Offset Voltage		Rh = 0, Lh = 0	-250		250	mV
Output Leakage Current		Idle Mode			20	µA
Output Common Mode Voltage		Rh = 0, Lh = 0	VCC - 0.9	VCC - 0.5	VCC - 0.3	V
Output Voltage Compliance		Adjust RDX, Y load voltage source for <5% THD of either output.	VCC - 1.6		VCC	V

SWITCHING CHARACTERISTICS

Test conditions same as Write Mode plus RDX, Y connected VCC through 100Ω resistors, WUS with 1 kΩ to VCC.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Idle to Read/Write Transition Time	Delay to 10 or 90% of Read Output or Write Current		75	150	ns
Read/Write to Idle Transition Time			85	150	ns
Read to Write Transition Time	VLCS = 0.8V, Delay to 90% of Iw		85	150	ns
Write to Read Transition Time	VLCS = 0.8V, Delay to 90% of 10 MHz Read Signal, 100 mV envelope		350	600	ns
Head Select Switching Delay	Read or Write Mode			500	ns
Head Current Rise and Fall Times 10% to 90%	Iw = 25 mA, Lh = 0 nH Rh = 0Ω		2.5	4.0	ns
	Iw = 15 mA, Lh = 1 µH Rh = 45Ω		6		ns
Head Current Rise and Fall Difference				0.5	ns
Head Current Switching Delay Difference (Asymmetry)	WDX, WDY transitions 2 ns, switching time asymmetry 0.2 ns			0.5	ns
Head Current Propogation Delay TD3	50% WD to 50% Iw		8	15	ns
Unsafe to Safe Delay After Write Data Begins WUS TD2	f(data) = 5 MHz Write Mode (After 2 transitions of WD)			200	ns
Unsafe to Safe Delay After Write Mode Selected WUS				0.5 +Tw*	µs
Safe to Unsafe Delay WUS TD1	After Write Mode fault condition occurs			1.5	µs
Safe to Unsafe Delay WUS	After exiting Write Mode			0.5	µs

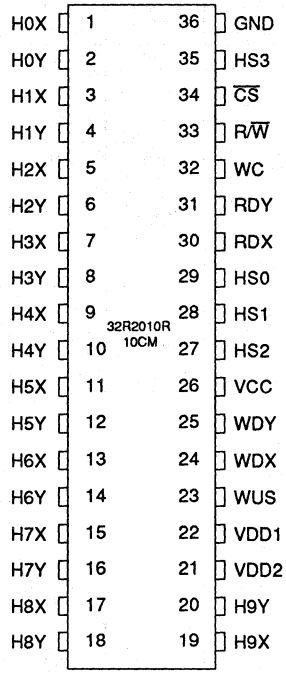
*Tw is the period of the write data input.



SSI 32R2010R
10-Channel Thin Film
Read/Write Device

PACKAGE PIN DESIGNATIONS

(Top View)



36-Lead SOM

THERMAL CHARACTERISTICS: θja

36-Lead SOM	75°C/W

CAUTION: Use handling procedures necessary for a static sensitive component.

ORDERING INFORMATION

PART DESCRIPTION	ORDER NUMBER	PACKAGE MARK
SSI 32R2010R 36-lead SOM	32R2010R-CM	32R2010R-10CM

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022, (714) 573-6000, FAX: (714) 573-6914

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SSI 32R2011R
10-Channel Thin Film Read/Write Device
Advance Information

December 1993

3

DESCRIPTION

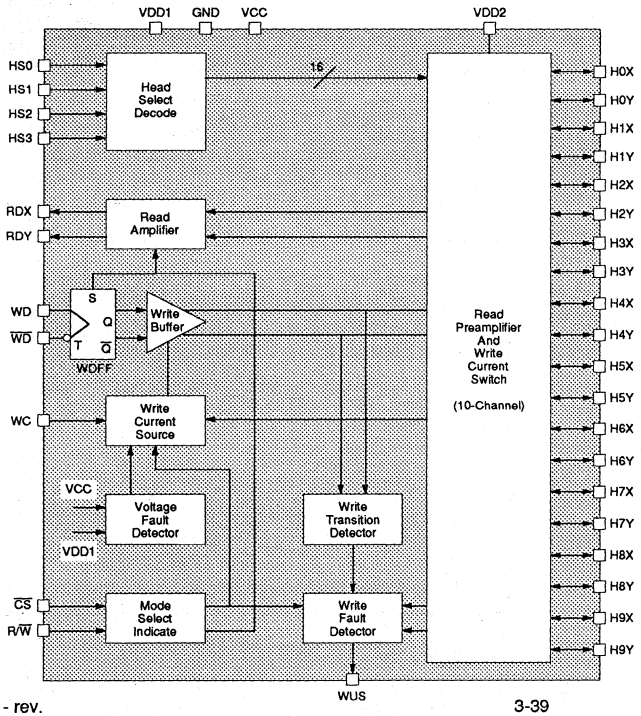
The SSI 32R2011R is an integrated read/write circuit designed for use with two terminal heads in disk drive systems. The device contains up to ten channels of read amplifiers and write drivers and also has an internal write current source. An internal 300Ω damping resistor is supplied in Write mode, which is switched to 1 kΩ in Read mode.

The circuit operates on +5V and +12V power supplies and is available in a 10-channel, 36-pin SO package.

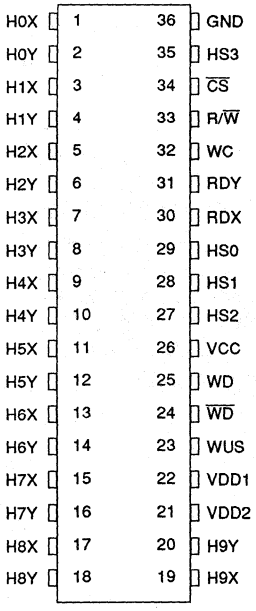
FEATURES

- **High performance**
  - **Read Mode Gain = 150 Typ V/V**
  - **Input Noise = 0.58 nV/$\sqrt{Hz}$ typ.**
  - **Input Capacitance = 15 pF typ.**
  - **Write Current Range = 10 mA to 25 mA**
  - **Write Current Rise Time = 4 ns**
  - **Head Voltage Swing = 7 Vpp min**
- **Write unsafe detection**
- **Differential, ECL-like write data input**
- **Open collector read data output**
- **Switch from 300Ω damping resistor to 1 kΩ read input resistance**
- **Power supply fault protection**
- **+5V, +12V power supplies ±10%**

BLOCK DIAGRAM



PIN DIAGRAM



36-Lead SOM

CAUTION: Use handling procedures necessary for a static sensitive component.

FUNCTIONAL DESCRIPTION

The SSI 32R2011R addresses up to 10 channels with logic control inputs which are TTL compatible. Head selection is accomplished as shown in Table 1. Mode selection is accomplished as shown in Table 2. The mode select inputs have internal pull up circuits so that if an input is open it will rise to the upper logic level and force the device into a non-writing condition.

WRITE MODE

In Write Mode (R/$\overline{W}$ and $\overline{CS}$ low) the circuit functions as a current switch. The Head Select Inputs HS0, HS1, HS2 and HS3 determine the selected head. The write data inputs (WD, $\overline{WD}$) determine the polarity of the head current. Write current is toggled between the X and Y direction of the selected head on each low to high transition of WD (see Figure 1). A preceding read operation initializes the Write Data Flip Flop (WDFF) to pass write current in the X-direction of the head (i.e., into the X-port).

The write current magnitude is adjusted by an external resistor, Rwc, from WC to GND, and is given by:

$$Iw = Vwc/Rwc$$

Note that actual head current, Ihd, is:

$$Ihd = Iw/(1+\frac{Rh}{Rd}) + Ioffset$$

where Rh is head resistance, Rd is write damping resistance and Ioffset is a constant DC offset current.

WRITE MODE FAULT DETECT CIRCUIT

Several circuits are dedicated to detecting fault conditions associated with the Write mode. A logical high (off) level will be present at the Write Unsafe (WUS) terminal if any of the following write fault conditions are present:

- Open head circuit (Iw ≥ 20 mA)
- Head shorted to ground
- Write current transition frequency too low
- Write mode not logically selected

After the fault condition is removed, two transitions of the write data input lines are required to clear WUS. The Write Unsafe output is open-collector and is usually terminated by an external resistor connected to VCC.

Additionally, power voltage monitoring circuits are used to detect VCC and VDD1 voltage levels. If either is too low to permit valid data recording, write current is inhibited.

READ MODE

In Read Mode, (R/$\overline{W}$ high and $\overline{CS}$ low), the circuit functions as a low noise differential amplifier. The read amplifier input terminals are determined by the Head Select inputs. The read amplifier outputs (RDX, RDY) are open collector, requiring external load resistors (100Ω) connected to VCC. The amplifier gain polarity is non-inverting between HnX, HnY inputs and RDX, RDY outputs.

The switch from Write to Read modes also changes the resistance across HnX and HnY from its write damping value of 300Ω to its read mode input value of 1 kΩ.

IDLE MODE

Taking $\overline{CS}$ high selects the Idle mode which switches the RDX and RDY outputs into a high impedance state and deactivates the internal write current source. This facilitates multi device installations by allowing the read outputs to be wired OR'ed and the write current programming resistor to be common to all devices.

TABLE 1: Head Select

Head Selected	HS3	HS2	HS1	HS0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

TABLE 2: Mode Select

$\overline{CS}$	R/$\overline{W}$	Mode
0	0	Write
0	1	Read
1	0	Idle
1	1	Idle

PIN DESCRIPTION

CONTROL INPUT PINS

NAME	TYPE	DESCRIPTION
$\overline{CS}$	I	Chip Select Input. A logical low level enables the circuit for a read or write operation. Has internal pull up.
R/$\overline{W}$	I	Read/write select. A logical low level enables the write mode (when $\overline{CS}$ is low). Has internal pull up.
HS0, HS1, HS2, HS3	I	Head select inputs. Logical combinations select one of sixteen heads. See Table 1. Has internal pull down resistors.

HEAD TERMINAL PINS

H0X-H9X, H0Y-H9Y	I/O	X, Y Head connections: Current in the X-direction flows into the X-port.

DATA INPUT/OUTPUT PINS

WD, $\overline{WD}$	I	Differential write data input.
RDX, RDY	O	Differential Read Data output. These open collector outputs are normally terminated in 100Ω resistors to VCC.

EXTERNAL COMPONENT CONNECTION PINS

WC	I/O	Resistor connected to GND to provide desired value of write current.

CIRCUIT MONITOR PINS

WUS	O	Write Unsafe is an open-collector output with the off-state indicating that conditions are not proper for a write operation.

POWER, GROUND PINS

VCC	I	+5V Logic circuit supply.
VDD1	I	+12V power supply.
VDD2	I	+12V power supply for write current drivers.
GND	I	Power supply common.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may permanently damage the device.

PARAMETER	RATING
Positive Supply Voltage, VCC	6 VDC
Supply Voltage, VDD1, 2	13.5 VDC
Operating Junction Temperature	+130°C
Storage Temperature	-65 to +130°C
Package Temperature (20 sec. reflow)	215°C

INPUT VOLTAGES

HS0, HS1, HS2, HS3, $\overline{CS}$, R/$\overline{W}$	-0.2 to VCC + 0.2 VDC

OUTPUTS

Read Data (RDX, RDY)	VCC -2.5 to VCC + 0.3 VDC
Write Unsafe (WUS)	-0.2V to VCC + 0.2V
Current Reference (WC)	-80 mA to 1.0 mA
Head Outputs (Write Mode)	-80 mA to 1.0 mA

POWER SUPPLY

Unless otherwise specified, 4.5V ≤ VCC ≤ 5.5V, 10.8V ≤ VDD1, 2 ≤ 13.2V, 0°C ≤ T (ambient) ≤ 70°C.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Power Dissipation (Does not include power dissipation through RDX, RDY load resistors)	Idle mode		195	295	mW
	Read mode		440	775	mW
	Write mode		350 + 10 Iw	530 + 11.2 Iw	mW
Positive Supply Current ICC (Includes RDX, RDY currents)	Idle Mode		13	20	mA
	Read Mode		27	35	mA
	Write Mode		22	26	mA
Positive Supply Current IDD1	Idle Mode		10	14	mA
	Read Mode		32	49	mA
	Write Mode		23	28	mA
Positive Supply Current IDD2	Idle Mode		0.5	2	mA
	Read Mode		1	1.5	mA
	Write Mode		1 + Iw	2 + Iw	mA

DC CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
High-level Input Voltage VIH ($\overline{CS}$, R/$\overline{W}$, HS0, HS1, HS2, HS3)		2.0		-	V
Low-level Input Voltage VIL ($\overline{CS}$, R/$\overline{W}$, HS0, HS1, HS2, HS3)				0.8	V
High-level Input Current IIH ($\overline{CS}$, R/$\overline{W}$, HS0, HS1, HS2, HS3)	VIH = 2.7V			100	µA
Low-level Input Current IIL ($\overline{CS}$, R/$\overline{W}$, HS0, HS1, HS2, HS3)	VIL = 0.4V			-400	µA
High-level Input Voltage VIHI (WD, $\overline{WD}$)		Vcc - 1.0		Vcc - 0.72	V
Low-level Input Voltage VILI (WD, $\overline{WD}$)		Vcc - 1.87		Vcc - 1.625	V
WUS, Low Level Voltage	ILUS = 4 mA (denotes safe condition)			0.5	V
WUS, High Level Current	VHUS = 5.0V (denotes unsafe condition)			100	µA

WRITE MODE

Test Conditions (Unless otherwise specified). VCC = 4.5 to 5.5V, Ta = 0 to +70°C, VDD = 10.8 to 13.2V, Lh = 470 nH, Rh = 25Ω, WD Tr, Tf < 2 ns, Iw = 20 mA.

Current Range, Iw		10		25	mA
Write Current Voltage, Vwc		1.95	2.05	2.15	V
Differential Head voltage Swing		7.0	7.6		Vpp
Ioffset			0.5		mA
Unselected Head Transient Current	Non adjacent heads tested to minimize external coupling effects			1	mA(pk)
Head Damping Resistance		240	300	360	Ω
Differential Output Capacitance				20	pF

ELECTRICAL SPECIFICATIONS (continued)

FAULT DETECTION CHARACTERISTICS

Test conditions same as Write Mode above (unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VCC Value for Write Current Turn off	Ih < 1 mA	3.7	4.0	4.3	V
VDD Value for Write Current Turn off	Ih < 1 mA	8.8	9.5	10.2	V
WD, $\overline{WD}$ Transition Frequency	WUS = Low (Guaranteed safe)	2.0			MHz

READ MODE

Tests performed with 100Ω load resistors from RDX and RDY to VCC. Test conditions same as Write mode (unless otherwise specified.)

Differential Voltage Gain		Vin = 1 mVpp, f = 300 kHz	120	150	180	V/V
Voltage Bandwidth	-3 dB	Zs < 5Ω, Vin = 1 mVpp	50	65		MHz
	-1 dB	Zs < 5Ω, Vin = 1 mVpp	20	35		MHz
Input Noise Voltage		Zs = 0Ω , Vin = 0V, Power Bandwidth = 20 MHz		0.58	0.75	nV/√Hz
Differential Input Capacitance		Vin = 0V, f = 5 MHz		15	20	pF
Differential Input Resistance		Vin = 0V, f = 5 MHz	400		1500	Ω
Dynamic Range @ 5 MHz		Input voltage where AC gain falls to 90% of the gain	4			mVpp
Common Mode Rejection Ratio		Vin = 100 mVpp, 0V DC f = 5 MHz	60	90		dB
Power Supply Rejection Ratio		VCC or VDD = 100 mVpp f = 5 MHz	55	75		dB
Channel Separation		Unselected channels are driven with Vin = 20 mVpp @ 5 MHz	60	90		dB
Output Offset Voltage		Rh = 0, Lh = 0	-250		250	mV
Output Leakage Current		Idle Mode			20	µA
Output Common Mode Voltage		Rh = 0, Lh = 0	VCC - 0.9	VCC - 0.5	VCC - 0.3	V
Output Voltage Compliance		Adjust RDX, Y load voltage source for <5% THD of either output.	VCC - 1.6		VCC	V

SWITCHING CHARACTERISTICS

Test conditions same as Write Mode plus RDX, Y connected VCC through 100Ω resistors, WUS with 1 kΩ to VCC.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Idle to Read/Write Transition Time	Delay to 90% of Read Output or Write Current		75	150	ns
Read/Write to Idle Transition Time	Delay to 10% of Read Output or Write Current		85	150	ns
Read to Write Transition Time	VL$\overline{CS}$ = 0.8V, Delay to 90% of Iw		85	150	ns
Write to Read Transition Time	VL$\overline{CS}$ = 0.8V, Delay to 90% of 10 MHz Read Signal, 100 mV envelope		350	600	ns
Head Select Switching Delay	Read or Write Mode			500	ns
Head Current Rise and Fall Times 10% to 90%	Iw = 25 mA, Lh = 0 nH Rh = 0Ω		2.5	4.0	ns
	Iw = 15 mA, Lh = 1 µH Rh = 45Ω		6		ns
Head Current Rise and Fall Difference				0.5	ns
Head Current Switching Delay Difference (Asymmetry)	WD, $\overline{WD}$ transitions 2 ns, switching time asymmetry 0.2 ns			0.5	ns
Head Current Propogation Delay TD3	50% WD to 50% Iw		8	15	ns
Unsafe to Safe Delay After Write Data Begins WUS TD2	f(data) = 5 MHz Write Mode (After 2 transitions of WD)			200	ns
Unsafe to Safe Delay After Write Mode Selected WUS				0.5 +Tw*	µs
Safe to Unsafe Delay WUS TD1	After Write Mode fault condition occurs			1.5	µs
Safe to Unsafe Delay WUS	After exiting Write Mode			0.5	µs

*Tw is the period of the write data input.

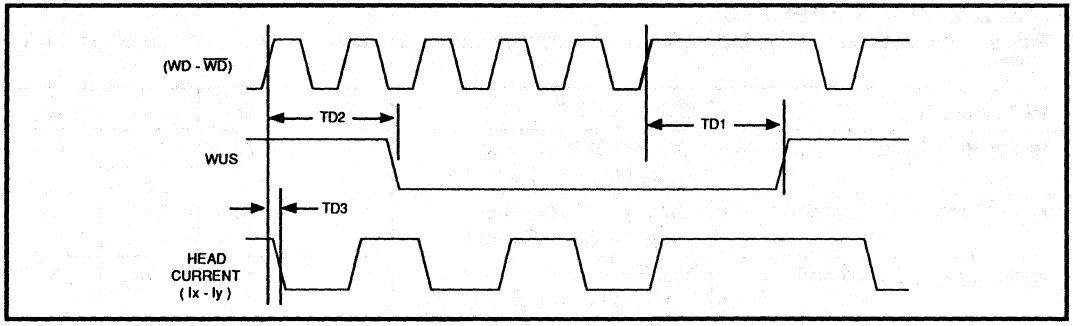
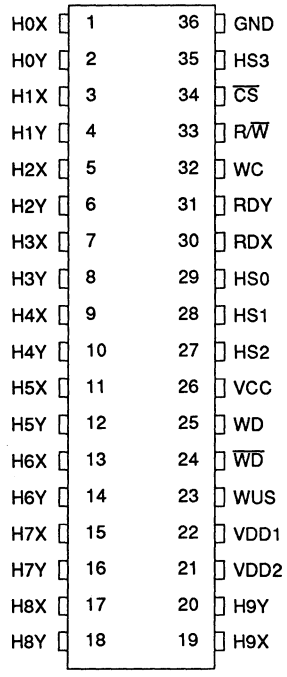


FIGURE 1: Write Mode Timing Diagram

PACKAGE PIN DESIGNATIONS

(Top View)



36-Lead SOM

THERMAL CHARACTERISTICS: θja

36-Lead SOM	75°C/W

CAUTION: Use handling procedures necessary for a static sensitive component.

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022, (714) 573-6000, FAX: (714) 573-6914

Notes:

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SSI 32R2020R/2021R
5V, 2, 4, 6, 10-Channel Thin-Film Read/Write Device

January 1993

DESCRIPTION

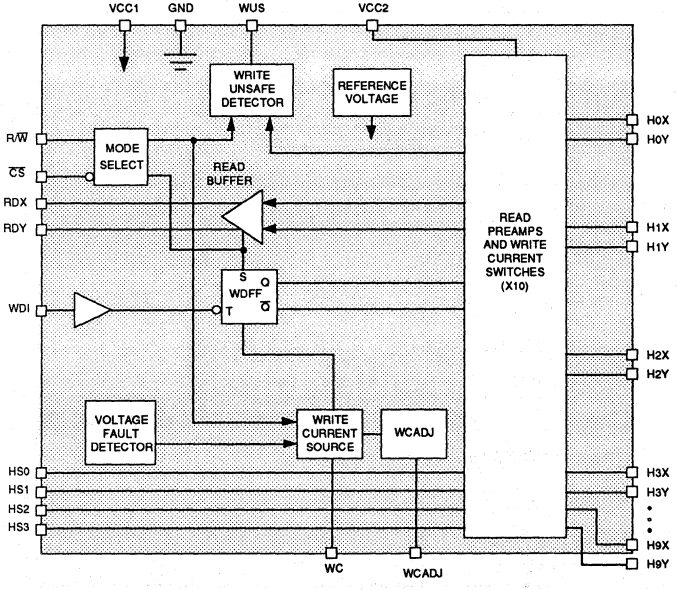
The SSI 32R2020R/2021R are bipolar monolithic integrated circuits designed for use with two-terminal recording heads. They provide a low noise read amplifier, write current control, and data protection circuitry for up to ten channels. The SSI 32R2020R/2021R provide internal 320Ω damping resistors. Damping resistors are switched in during write mode and switched out during read mode. Power supply fault protection is provided by disabling the write current generator during power sequencing. System write to read recovery time is significantly improved by controlling the read channel common mode output voltage shift in the write mode. The 32R2021R option provides the user with a controllable write current adjustment feature.

The SSI 32R2020R/2021R require only +5V power supplies and are available in a variety of packages. They are hardware compatible with the 32R4610A/4611A read/write devices.

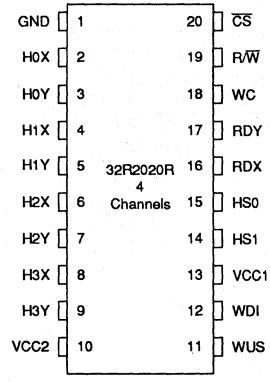
FEATURES

- **+5V ±10% supply**
- **Low power**
  - **PD = 130 mW read mode (Nom)**
  - **PD = 3.3 mW idle (Nom)**
- **High Performance:**
  - **Read mode gain = 300 V/V**
  - **Input noise = 0.56 nV/√Hz (Nom)**
  - **Input capacitance = 16 pF (Nom)**
  - **Write current range = 5-35 mA**
- **Self switching damping resistance**
- **Designed for two-terminal thin-film or MIG heads with inductance up to 5.0 μH**
- **Pin compatible with the 32R4610AR/4611AR**
- **Write unsafe detection**
- **Power supply fault protection**
- **Head short to ground protection**

BLOCK DIAGRAM



PIN DIAGRAM



20-PIN SOL

CAUTION: Use handling procedures necessary for a static sensitive component.

WCADJ available on the 32R2021R-4 24-pin option only

CIRCUIT OPERATION

The SSI 32R2020R/2021R have the ability to address up to 10 two-terminal heads and provide write drive or read amplification. Mode control and head selection are described in Tables 1 and 2. The TTL inputs R/$\overline{W}$ and $\overline{CS}$ have internal pull-up resistors to prevent an accidental write condition. HS0, HS1, HS2 and HS3 have internal pulldown resistors. Internal clamp circuitry will protect the IC from a head short to ground condition in any mode.

TABLE 1: Mode Select

$\overline{CS}$	R/$\overline{W}$	Mode
0	0	Write
0	1	Read
1	0	Idle
1	1	Idle

TABLE 2: Head Select

HS3	HS2	HS1	HS0	Head
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
HS0, HS1, † HS2, HS3	I	Head Select: selects one of ten heads
$\overline{CS}$	I	Chip Select: a high inhibits the chip
R/$\overline{W}$ †	I	Read/Write : a high selects Read mode
WUS †	O	Write Unsafe: a high indicates an unsafe writing condition
WDI †	I	Write Data In: changes the direction of the current in the recording head
H0X - H9X; H0Y - H9Y	I/O	X, Y Head Connections
RDX, RDY †	O	X, Y Read Data: differential read data output
WC †		Write Current: used to set the magnitude of the write current
WCADJ* †		Write Current Adjust: Used to fine tune the write current
VCC1	I	+5V Supply
VCC2	I	+5V Supply for Write current drivers
GND	I	Ground

* Available on 32R2021R-4 24-pin option only

† When more than one R/W device is used, signals can be wire OR'ed

WRITE MODE

Taking both $\overline{CS}$ and R/$\overline{W}$ low selects Write mode which configures the SSI 32R2020R/2021R as a current switch and activates the Write Unsafe (WUS) detector circuitry. Head current is toggled between the X and Y side of the selected head on each high to low transition of the Write Data Input (WDI). Changing from Read or Idle mode to Write mode initializes the Write Data Flip-Flop to pass write current into the "X" pin. In this case, the Y side of the head will be higher potential than the X side. The magnitude of the write current (0-pk) is given by:

$$Iw = \frac{K \cdot Vwc}{Rwc}$$

Rwc is connected from pin WC to GND. Note the actual head current Ix, y is given by:

$$Ix, y = \frac{Iw}{1 + Rh/Rd}$$

Where:

Rh = Head resistance plus external wire resistance

Rd = Damping resistance

In write mode a 320Ω damping resistor is switched in across the Hx, Hy ports.

The 32R2021R adds a feature which allows the user to adjust the Iw current by a finite amount. The WCADJ pin is used to adjust write current for write operations on different zones of the disk. It is used by switching a separate write current adjust resistor in and out on the WCADJ pin or by connecting a DAC to that pin to sink a controllable amount of current. The WCADJ pin is nominally biased to VCC/2. Sinking current from this pin to ground will divert a proportional amount of current from the actual head current while maintaining a constant current through the WC resistor and VCC. Allowing WCADJ to float or pulling it high will cut off the circuit and it will have no effect. A TTL gate can be used as a switch with a small degradation in accuracy. The amount of write current decrease is shown below:

Iw head (decrease) (mA) = (29 • V_{WCADJ}/R_{WCADJ})

where:

V_{WCADJ} = VCC/2 (volts)

R_{WCADJ} = write current adjust setting resistor (kΩ)

Example: For a 7.25 mA head current decrease, R_{WCADJ} = (27 • 2.5) / 7.25 = 10 kΩ

POWER SUPPLY FAULT PROTECTION

A voltage fault detection circuit improves data security by disabling the write current generator during a voltage fault or power startup regardless of mode. Note that WUS does not necessarily turn on to flag a power supply fault condition.

HEAD SHORT TO GROUND PROTECTION

The 2020R/2021R provides a head short to ground protection circuit in any mode. In Idle or Read Mode, current out of the head port will not exceed 20 mA if any head is shorted to ground. In Write mode, if any head is shorted to ground (regardless if it is selected or not) the write current generator will turn off, the WUS flag will go high, and current will be limited to less than 1 mA out of the head port.

WRITE UNSAFE

Any of the following conditions will be indicated as a high level on the Write Unsafe, WUS, open collector output.

- WDI frequency too low
- Device in Read mode
- Chip disabled
- No head current
- Head opened
- Head short to ground

To insure proper WUS operation, the product of write current, WDI frequency, and head inductance should be less than 500 mA•µH•MHz. To insure no false WUS trigger, the product of head current and head resistance (Ix,y•Rh) should be between 100 mV and 1.7V.

WDI frequency too low is detected if the WDI frequency falls below 500 kHz (typ). Consult the WUS Safe to Unsafe timing for range of frequency detection.

Device in Read mode and **Chip disabled** will flag WUS if R/$\overline{W}$ is high or $\overline{CS}$ is high.

No head current will flag WUS if Rwc = ∞ and the selected head is present.

Head opened will flag WUS if Rh = ∞ and under the condition that VCC/Iw < 0.25 V/mA.

Head short to ground is described in the preceding paragraph.

Upon entering write mode, WUS is valid after two high to low transitions of WDI following the required Read-Write transition time (0.6 µs max).

CIRCUIT OPERATION (continued)

READ MODE

The Read mode configures the SSI 32R2020R/2021R as a low noise differential amplifier and deactivates the write current generator. The damping resistor is switched out of the circuit allowing a high impedance input to the read amplifier. The RDX and RDY output are driven by emitter followers. They should be AC coupled to the load. The (X,Y) inputs are non-inverting to the (X,Y) outputs.

Note that in Idle or Write mode, the read amplifier is deactivated and RDX, RDY outputs become high impedance. This facilitates multiple R/W applications (wired-OR RDX, RDY) and minimizes voltage drifts when switching from Write to Read mode. Note also that the write current source is deactivated for both the Read and Idle mode.

IDLE MODE

Taking $\overline{CS}$ high selects the idle mode which switches the RDX and RDY outputs into a high impedance state and deactivates the device. Power consumption in this mode is held to a minimum.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may permanently damage the device.

PARAMETER		RATING
DC Supply Voltage	VCC1	-0.3 to +6 VDC
	VCC2	-0.3 to +6 VDC
Write Current	Iw	60 mA
Digital Input Voltage	Vin	-0.3 to VCC1 +0.3 VDC
Head Port Voltage	VH	-0.3 to VCC2 +0.3 VDC
Output Current: RDX, RDY	I0	-6 mA
WUS		+8 mA
Storage Temperature	Tstg	-65 to +150 °C

RECOMMENDED OPERATING CONDITIONS

DC Supply Voltage	VCC1 = VCC2	5 ±10%	VDC
Operating Junction Temperature	Tj	+25 to +135	°C
Recommended Head Load Range	Lh	0.3 - 5.0	µH

DC CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VCC1 Supply Current	Read Mode		18	25	mA
	Write Mode		22	29	mA
	Idle Mode		0.6	0.95	mA
VCC2 Supply Current	Read Mode		8	11	mA
	Write Mode		4 + Iw	7 + Iw	mA
	Idle Mode		0	0.2	mA

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Power Dissipation	Read Mode		130	200	mW
	Write Mode		130 + 4 Iw	200 + 4.3 Iw	mW
	Idle Mode		3.3	6.5	mW
VCC1 Fault Voltage	Iw < 0.2 mA	3.5	3.9	4.2	VDC

DIGITAL INPUTS

Input Low voltage (Vil)				0.8	VDC
Input High Voltage (Vil)		2.0			VDC
Input Low Current	Vil = 0.8V	-0.4			mA
Input High Current	Vih = 2.0V			100	µA
WUS Output Low Voltage (Vol)	Iol = 2 mA max			0.5	VDC

WRITE CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified.

Write Current Constant "K"			0.99		
Write Current Voltage (Vwc)		1.15	1.25	1.35	V
WCADJ Voltage SSI 32R2021R	I_{WCADJ} = 0 to .5 mA	2.0	VCC/2	3.0	VDC
Ihead(Decrease)/I_{WCADJ} SSI 32R2021R		23	27	31	mA/mA
I_{WCADJ} Range SSI 32R2021R		0.0		0.5	mA
Differential Head Voltage Swing		4.2	5.6		Vpp
	Open Head Iw = 20 mA	3.4	5.0		Vpp
Unselected Head Current				1	mA (pk)
Head Differential Damping Resistance (Rd)			320		Ω
WDI Pulse Width	Vil ≥ 0.2V PWH	10			ns
	PWL	5			ns
Write Current Range (Iw)		5		35	mA
Head Differential Load Capacitance				25	pF

READ CHARACTERISTICS
Recommended operating conditions apply unless otherwise specified. CL (RDX, RDY) < 20 pF, RL (RDX, RDY) = 1 kΩ.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Differential Voltage Gain	Vin = 1 mVpp @1 MHz	250	300	350	V/V
Voltage BW -1dB	|Zs| < 5Ω, Vin = 1 mVpp	20			MHz
-3dB	|Zs| < 5Ω, Vin = 1 mVpp	45			MHz
Input Noise Voltage	BW = 15 MHz, Lh = 0, Rh = 0		0.56	0.75	nV/√Hz
Differential Input Capacitance	Vin = 1 mVpp, f = 5 MHz		16	22	pF
Differential Input Resistance	Vin = 1 mVpp, f = 5 MHz	720	1200		Ω
Dynamic Range	AC input voltage where gain falls to 90% of its small signal gain value, f = 5 MHz	2			mVpp
Common Mode Rejection Ratio	Vin = 0 VDC + 100 mVpp @ 5 MHz	55			dB
Power Supply Rejection Ratio	100 mVpp @ 5 MHz on VCC	50			dB
Channel Separation	Unselected channels driven with Vin = 0 VDC + 100 mVpp	55			dB
Output Offset Voltage				±300	mV
Single Ended Output Resistance	f = 5 MHz			50	Ω
Output Current	AC coupled load, RDX to RDY	0.9			mA
RDX, RDY Common Mode Output Voltage		0.4 VCC	VCC/2	0.6 VCC	VDC

SWITCHING CHARACTERISTICS
Recommended operating conditions apply unless otherwise specified. IW = 20 mA, Lh = 1.0 µH, Rh = 30Ω f(Data) = 5 MHz.

R/$\overline{W}$	Read to Write	R/W to 90% of write current		0.1	0.6	µs
	Write to Read	R/W to 90% of 100 mV Read signal envelope		0.1	0.6	µs
$\overline{CS}$	Unselect to Select	$\overline{CS}$ to 90% of write current or to 90% of 100 mV 10 MHz		0.2	1	µs
	Select to Unselect	$\overline{CS}$ to 10% of write current		0.11	0.6	µs
HS0,1 to any Head		To 90% of 100 mV 10 MHz Read signal envelope		0.11	0.6	µs
WUS:	Safe to Unsafe (TD1)	Write mode, loss of WDI transitions. Defines maximum WDI period for WUS operation	0.6	2.0	3.6	µs
	Unsafe to Safe (TD2)	Fault cleared, from first neg WDI transition		0.1	0.6	µs

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Head Current:					
WDI to Ix - Iy (TD3)	from 50% points, Lh = 0, Rh = 0		3	10	ns
Asymmetry	WDI has 1 ns rise/fall time, Lh = 0, Rh = 0			1.0	ns
Rise/fall Time	10% to 90% points, Lh = 0, Rh = 0		4	6	ns
Rise/fall Time	Lh = 1 µH, Rh = 30Ω		15		ns

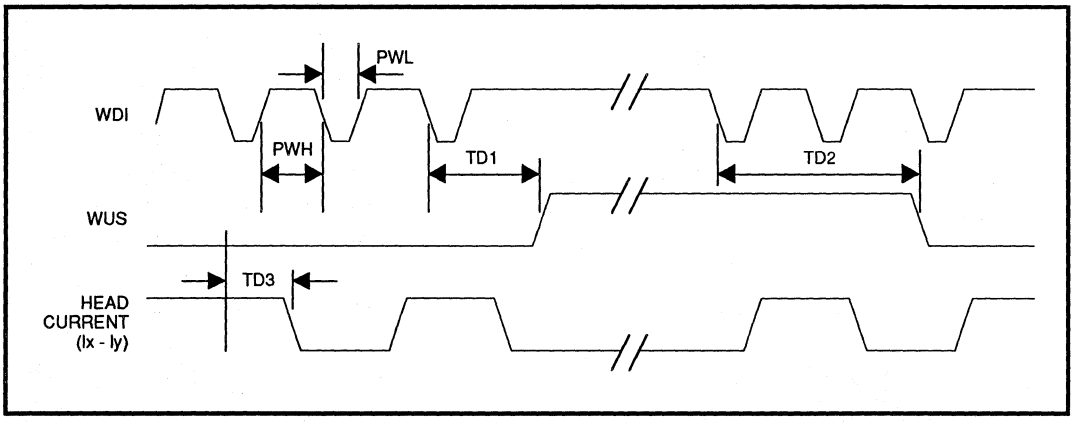
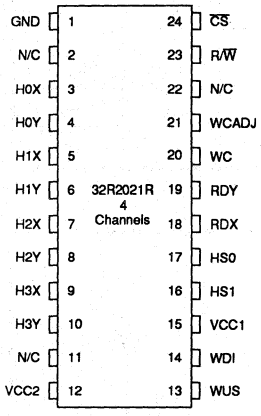


FIGURE 1: Write Mode Timing Diagram

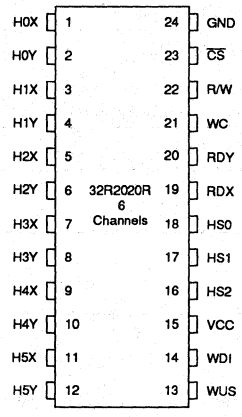
SSI 32R2020R/2021R
5V, 2, 4, 6, 10-Channel
Thin-Film Read/Write Device

PACKAGE PIN DESIGNATIONS

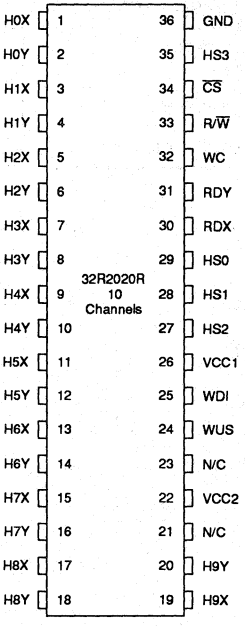
(Top View)



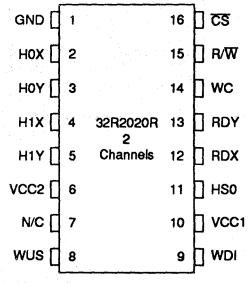
24-Pin SOL, SOV



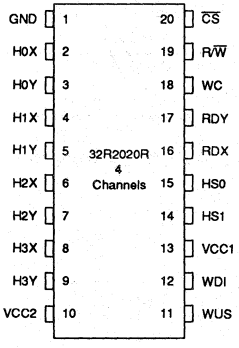
24-Pin SOV



36-Pin SOM



16-Pin SOL



20-Pin SOL, SOV

ORDERING INFORMATION

PART DESCRIPTION		ORDER NUMBER	PACKAGE MARK
2-Channel			
SSI 32R202R	16-Lead SOL	32R2020R-2CL	32R2020R-2CL
	20-Lead SON	32R2020R-2CN	32R2020R-2CN
4-Channel			
SSI 32R202R	20-Lead SOL	32R2020R-4CL	32R2020R-4CL
	20-Lead SOV	32R2020R-4CV	32R2020R-4V
32R2021R	24-Lead SOV	32R2021R-4CV	32R2021R-4CV
6-Channel			
32R2020R	24-Lead SOV	32R2020R-6CV	32R2020R-6CV
10-Channel	36-Lead SOM	32R2020R-10CM	32R2020R-10CM

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 573-6000, FAX (714) 573-6914

0193 - rev.

Notes:

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SSI 32R2025R
5V, 4-Channel Thin-Film Read/Write Device
Advance Information

December 1993

3

DESCRIPTION

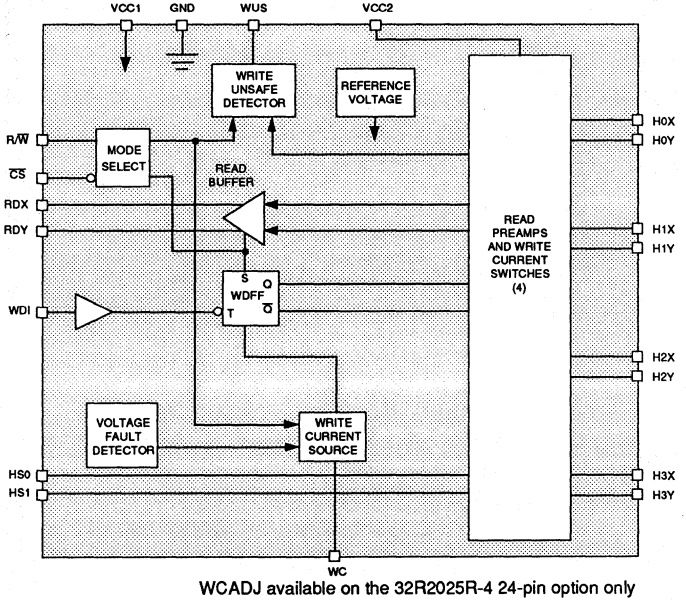
The SSI 32R2025R is a bipolar monolithic integrated circuit designed for use with two-terminal recording heads. It provides a low noise read amplifier, write current control, and data protection circuitry for up to four channels. The SSI 32R2025R provides internal 620Ω damping resistors. Damping resistors are switched in during Write mode and switched out during Read mode. Power supply fault protection is provided by disabling the write current generator during power sequencing. System write to read recovery time is significantly improved by controlling the read channel common mode output voltage shift in the Write mode. The 32R2025R option provides the user with a controllable write current adjustment feature.

The SSI 32R2025R requires only +5V power supplies and is available in 20-lead SO packages. It is hardware compatible with the SSI 32R2020R Read/Write device.

FEATURES

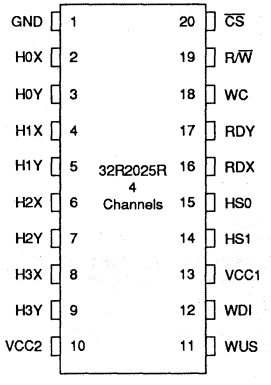
- **+5V ±10% supply**
- **Low power**
  - **PD = 130 mW Read mode (Nom)**
  - **PD = 3.3 mW Idle (Nom)**
- **High Performance:**
  - **Read mode gain = 300 V/V**
  - **Input noise = 0.56 nV/√Hz (Nom)**
  - **Input capacitance = 16 pF (Nom)**
  - **Write current range = 5-35 mA**
- **Self switching damping resistance**
- **Designed for two-terminal, thin-film or MIG heads with inductance up to 5.0 μH**
- **Pin compatible with the 32R2020R**
- **Write unsafe detection**
- **Power supply fault protection**
- **Head short to ground protection**

BLOCK DIAGRAM



WCADJ available on the 32R2025R-4 24-pin option only

PIN DIAGRAM



20-LEAD SOL, SOV

CAUTION: Use handling procedures necessary for a static sensitive component.

SSI 32R2025R
5V, 4-Channel
Thin-Film Read/Write Device

CIRCUIT OPERATION

The SSI 32R2025R has the ability to address up to 4 two-terminal heads and provide write drive or read amplification. Mode control and head selection are described in Tables 1 and 2. The TTL inputs R/$\overline{W}$ and $\overline{CS}$ have internal pull-up resistors to prevent an accidental write condition. HS0 and HS1 have internal pulldown resistors. Internal clamp circuitry will protect the IC from a head short to ground condition in any mode.

TABLE 1: Mode Select

$\overline{CS}$	R/$\overline{W}$	Mode
0	0	Write
0	1	Read
1	0	Idle
1	1	Idle

TABLE 2: Head Select

HS1	HS0	Head
0	0	0
0	1	1
1	0	2
1	1	3

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
HS0, HS1 †	I	Head Select: selects one of four heads
$\overline{CS}$	I	Chip Select: a high inhibits the chip
R/$\overline{W}$ †	I	Read/Write : a high selects Read mode
WUS †	O	Write Unsafe: a high indicates an unsafe writing condition
WDI †	I	Write Data In: changes the direction of the current in the recording head
H0X - H3X; H0Y - H3Y	I/O	X, Y Head Connections
RDX, RDY †	O	X, Y Read Data: differential read data output
WC †		Write Current: used to set the magnitude of the write current
VCC1	I	+5V Supply
VCC2	I	+5V Supply for write current drivers
GND	I	Ground
† When more than one R/W device is used, signals can be wire OR'ed.		

WRITE MODE

Taking both $\overline{CS}$ and R/$\overline{W}$ low selects Write mode which configures the SSI 32R2025R as a current switch and activates the Write Unsafe (WUS) detector circuitry. Head current is toggled between the X and Y side of the selected head on each high to low transition of the Write Data Input (WDI). Changing from Read or Idle mode to Write mode initializes the Write Data Flip-Flop to pass write current into the "X" pin. In this case, the Y side of the head will be higher potential than the X side. The magnitude of the write current (0-pk) is given by:

$$Iw = \frac{K \cdot Vwc}{Rwc}$$

Rwc is connected from pin WC to GND. Note the actual head current Ix, y is given by:

$$Ix, y = \frac{Iw}{1 + Rh/Rd}$$

Where:

Rh = Head resistance plus external wire resistance

Rd = Damping resistance

In Write mode a 620Ω damping resistor is switched in across the Hx, Hy ports.

POWER SUPPLY FAULT PROTECTION

A voltage fault detection circuit improves data security by disabling the write current generator during a voltage fault or power startup regardless of mode. Note that WUS does not necessarily turn on to flag a power supply fault condition.

HEAD SHORT TO GROUND PROTECTION

The 32R2025R provides a head short to ground protection circuit in any mode. In Idle or Read mode, current out of the head port will not exceed 20 mA if any head is shorted to ground. In Write mode, if any head is shorted to ground (regardless if it is selected or not) the write current generator will turn off, the WUS flag will go high, and current will be limited to less than 2 mA out of the head port.

WRITE UNSAFE

Any of the following conditions will be indicated as a high level on the Write Unsafe, WUS, open collector output.

- WDI frequency too low
- Device in Read mode
- Chip disabled
- No head current
- Head opened
- Head short to ground

To insure proper WUS operation, the product of write current, WDI frequency, and head inductance should be less than 400 mA•µH•MHz. To insure no false WUS trigger, the product of head current and head resistance (Ix,y•Rh) should be between 100 mV and 1.7V.

WDI frequency too low is detected if the WDI frequency falls below 500 kHz (typ). Consult the WUS Safe to Unsafe timing for range of frequency detection.

Device in Read mode and **Chip disabled** will flag WUS if R/$\overline{W}$ is high or $\overline{CS}$ is high.

No head current will flag WUS if Rwc = ∞ and the selected head is present.

Head opened will flag WUS if Rh = ∞ and under the condition that Vcc/Iw < 0.25 V/mA.

Head short to ground is described in the preceding paragraph.

Upon entering Write mode, WUS is valid after two high to low transitions of WDI following the required Read-Write transition time (0.6 µs max).

READ MODE

The Read mode configures the SSI 32R2025R as a low noise differential amplifier and deactivates the write current generator. The damping resistor is switched out of the circuit allowing a high impedance input to the read amplifier. The RDX and RDY output are driven by emitter followers. They should be AC coupled to the load. The (X,Y) inputs are non-inverting to the (X,Y) outputs.

Note that in Idle or Write mode, the read amplifier is deactivated and RDX, RDY outputs become high impedance. This facilitates multiple R/W applications (wired-OR RDX, RDY) and minimizes voltage drifts when switching from Write to Read mode. Note also that the write current source is deactivated for both the Read and Idle mode.

IDLE MODE

Taking $\overline{CS}$ high selects the idle mode which switches the RDX and RDY outputs into a high impedance state and deactivates the device. Power consumption in this mode is held to a minimum.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may permanently damage the device.

PARAMETER		RATING
DC Supply Voltage	VCC1	-0.3 to +6 VDC
	VCC2	-0.3 to +6 VDC
Write Current	Iw	60 mA
Digital Input Voltage	Vin	-0.3 to VCC1 +0.3 VDC
Head Port Voltage	VH	-0.3 to VCC2 +0.3 VDC
Output Current: RDX, RDY	I0	-6 mA
$\overline{\text{WUS}}$		+8 mA
Storage Temperature	Tstg	-65 to +150 °C

RECOMMENDED OPERATING CONDITIONS

DC Supply Voltage	VCC1 = VCC2	5 ±10%	VDC
Operating Junction Temperature	Tj	+25 to +135	°C
Recommended Head Load Range	Lh	0.3 - 5.0	µH

DC CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VCC1 Supply Current	Read mode		18	25	mA
	Write mode		22	29	mA
	Idle Mode		0.6	0.95	mA
VCC2 Supply Current	Read mode		8	11	mA
	Write mode		4 + Iw	7 + Iw	mA
	Idle Mode		0	0.2	mA
Power Dissipation	Read mode		130	200	mW
	Write mode		130 + 4 Iw	200 + 4.3 Iw	mW
	Idle Mode		3.3	6.5	mW
VCC1 Fault Voltage	Iw < 0.2 mA	3.5	3.9	4.2	VDC

DIGITAL INPUTS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Input Low voltage (Vil)				0.8	VDC
Input High Voltage (Vil)		2.0			VDC
Input Low Current	Vil = 0.8V	-0.4			mA
Input High Current	Vih = 2.0V			100	µA
WUS Output Low Voltage (Vol)	Iol = 2 mA max			0.5	VDC

WRITE CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified.

Write Current Constant "K"				0.99		
Write Current Voltage (Vwc)			1.15	1.25	1.35	V
Differential Head Voltage Swing			4.2	5.6		Vpp
	Open Head, Iw = 20 mA		3.4	5.0		Vpp
Unselected Head Current					1	mA (pk)
Unselected Head Voltage				4.5		V
Head Differential Damping Resistance (Rd)				620		Ω
WDI Pulse Width	Vil ≥ 0.2V	PWH	10			ns
		PWL	5			ns
Write Current Range (Iw)			5		35	mA
Head Differential Load Capacitance					25	pF

READ CHARACTERISTICS
Recommended operating conditions apply unless otherwise specified. CL (RDX, RDY) < 20 pF, RL (RDX, RDY) = 1 kΩ.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Differential Voltage Gain	Vin = 1 mVpp @1 MHz	250	300	350	V/V
Voltage BW -1dB	|Zs| < 5Ω, Vin = 1 mVpp	20			MHz
-3dB	|Zs| < 5Ω, Vin = 1 mVpp	45			MHz
Input Noise Voltage	BW = 15 MHz, Lh = 0, Rh = 0		0.56	0.75	nV/√Hz
Differential Input Capacitance	Vin = 1 mVpp, f = 5 MHz		16	22	pF
Differential Input Resistance	Vin = 1 mVpp, f = 5 MHz	720	1200		Ω
Dynamic Range	AC input voltage where gain falls to 90% of its small signal gain value, f = 5 MHz	2			mVpp
Common Mode Rejection Ratio	Vin = 0 VDC + 100 mVpp @ 5 MHz	55			dB
Power Supply Rejection Ratio	100 mVpp @ 5 MHz on VCC	50			dB
Channel Separation	Unselected channels driven with Vin = 0 VDC + 100 mVpp	55			dB
Output Offset Voltage				±300	mV
Single Ended Output Resistance	f = 5 MHz			50	Ω
Output Current	AC coupled load, RDX to RDY	0.9			mA
RDX, RDY Common Mode Output Voltage		0.4 VCC	VCC/2	0.6 VCC	VDC

SWITCHING CHARACTERISTICS
Recommended operating conditions apply unless otherwise specified. IW = 20 mA, Lh = 1.0 µH, Rh = 30Ω f(Data) = 5 MHz.

R/$\overline{W}$	Read to Write	R/W to 90% of write current		0.1	0.6	µs
	Write to Read	R/W to 90% of 100 mV Read signal envelope		0.1	0.6	µs
$\overline{CS}$	Unselect to Select	$\overline{CS}$ to 90% of write current or to 90% of 100 mV 10 MHz		0.2	1	µs
	Select to Unselect	$\overline{CS}$ to 10% of write current		0.11	0.6	µs
HS0,1 to any Head		To 90% of 100 mV 10 MHz Read signal envelope		0.11	0.6	µs
WUS:	Safe to Unsafe (TD1)	Write mode, loss of WDI transitions. Defines maximum WDI period for WUS operation	0.6	2.0	3.6	µs
	Unsafe to Safe (TD2)	Fault cleared, from first neg WDI transition		0.1	0.6	µs

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Head Current:					
WDI to Ix - Iy (TD3)	from 50% points, Lh = 0, Rh = 0		3	10	ns
Asymmetry	WDI has 1 ns rise/fall time, Lh = 0, Rh = 0			1.0	ns
Rise/fall Time	10% to 90% points, Lh = 0, Rh = 0		4	6	ns
Rise/fall Time	Lh = 1 µH, Rh = 30Ω		15		ns

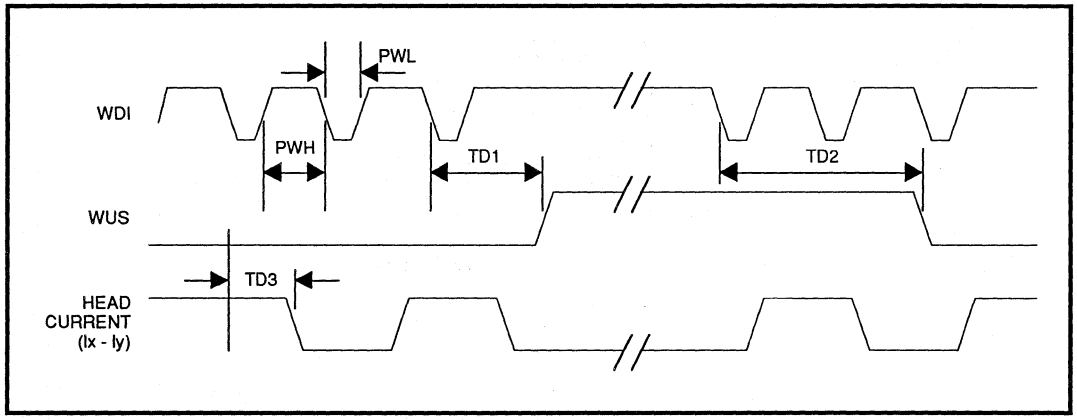
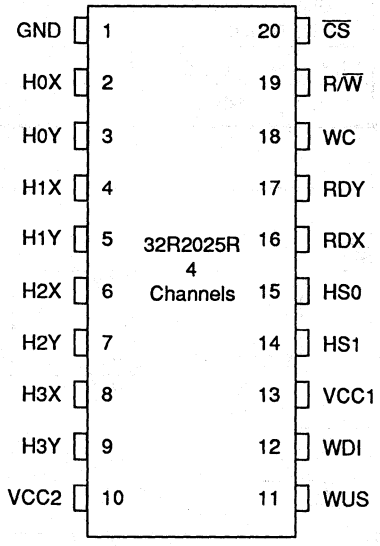


FIGURE 1: Write mode Timing Diagram

SSI 32R2025R
5V, 4-Channel
Thin-Film Read/Write Device

PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



20-Pin SOL, SOV

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914

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SSI 32R2026R
5V, 4-Channel Thin-Film Read/Write Device
Preliminary Data

April 1993

DESCRIPTION

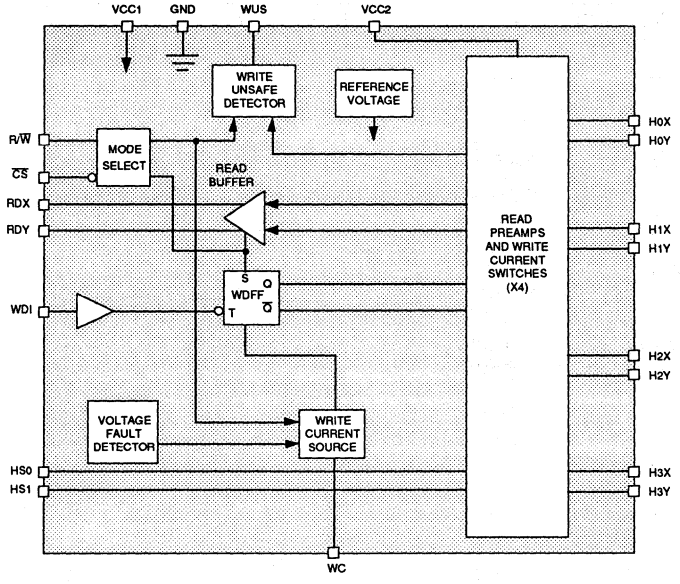
The SSI 32R2026R are bipolar monolithic integrated circuits designed for use with two-terminal recording heads. They provide a low noise read amplifier, write current control, and data protection circuitry for up to four channels. The SSI 32R2026R provide internal 320Ω damping resistors. Damping resistors are switched in during write mode and switched out during read mode. Power supply fault protection is provided by disabling the write current generator during power sequencing. System write to read recovery time is significantly improved by controlling the read channel common mode output voltage shift in the write mode.

The SSI 32R2026R requires only +5V power supplies and is available in a variety of packages. It is hardware compatible with the 32R2020R read/write devices.

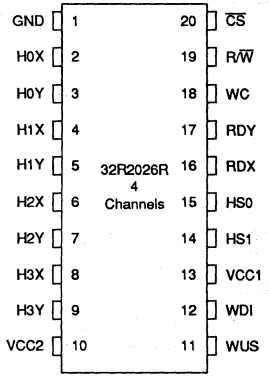
FEATURES

- **+5V ±10% supply**
- **Low power**
  - **PD = 130 mW read mode (Nom)**
  - **PD = 3.3 mW idle (Nom)**
- **High Performance:**
  - **Read mode gain = 300 V/V**
  - **Input noise = 0.56 nV/√Hz (Nom)**
  - **Input capacitance = 16 pF (Nom)**
  - **Write current range = 5-35 mA**
- **Self switching damping resistance**
- **Designed for two-terminal thin-film or MIG heads with inductance up to 5.0 μH**
- **Pin compatible with the 32R2020R**
- **Write unsafe detection**
- **Power supply fault protection**
- **Unselected head at ground potential**

BLOCK DIAGRAM



PIN DIAGRAM



20-LEAD SOL

CAUTION: Use handling procedures necessary for a static sensitive component.

CIRCUIT OPERATION

The SSI 32R2026R have the ability to address up to 4 two-terminal heads and provide write drive or read amplification. Mode control and head selection are described in Tables 1 and 2. The TTL inputs R/$\overline{W}$ and $\overline{CS}$ have internal pull-up resistors to prevent an accidental write condition. HS0 and HS1 have internal pulldown resistors. Internal clamp circuitry will protect the IC from a head short to ground condition in any mode.

TABLE 1: Mode Select

$\overline{CS}$	R/$\overline{W}$	Mode
0	0	Write
0	1	Read
1	0	Idle
1	1	Idle

TABLE 2: Head Select

HS1	HS0	Head
0	0	0
0	1	1
1	0	2
1	1	3

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
HS0, HS1, †	I	Head Select: selects one of four heads
$\overline{CS}$	I	Chip Select: a high inhibits the chip
R/$\overline{W}$ †	I	Read/Write : a high selects Read mode
WUS †	O	Write Unsafe: a high indicates an unsafe writing condition
WDI †	I	Write Data In: changes the direction of the current in the recording head
H0X - H3X; H0Y - H3Y	I/O	X, Y Head Connections
RDX, RDY †	O	X, Y Read Data: differential read data output
WC †		Write Current: used to set the magnitude of the write current
VCC1	I	+5V Supply
VCC2	I	+5V Supply for Write current drivers
GND	I	Ground
† When more than one R/W device is used, signals can be wire OR'ed		

WRITE MODE

Taking both $\overline{CS}$ and R/$\overline{W}$ low selects Write mode which configures the SSI 32R2026R as a current switch and activates the Write Unsafe (WUS) detector circuitry. Head current is toggled between the X and Y side of the selected head on each high to low transition of the Write Data Input (WDI). Changing from Read or Idle mode to Write mode initializes the Write Data Flip-Flop to pass write current into the "X" pin. In this case, the Y side of the head will be higher potential than the X side. The magnitude of the write current (0-pk) is given by:

$$Iw = \frac{K \cdot Vwc}{Rwc}$$

Rwc is connected from pin WC to GND. Note the actual head current Ix, y is given by:

$$Ix, y = \frac{Iw}{1 + Rh/Rd}$$

Where:

Rh = Head resistance plus external wire resistance

Rd = Damping resistance

In write mode a 320Ω damping resistor is switched in across the Hx, Hy ports. The unselected head potential is kept at ground.

POWER SUPPLY FAULT PROTECTION

A voltage fault detection circuit improves data security by disabling the write current generator during a voltage fault or power startup regardless of mode. Note that WUS does not necessarily turn on to flag a power supply fault condition.

HEAD SHORT TO GROUND PROTECTION

The 32R2026R provides a head short to ground protection circuit in any mode. In Idle or Read Mode, current out of the head port will not exceed 20 mA if any head is shorted to ground. In Write mode, if any head is shorted to ground (regardless if it is selected or not) the write current generator will turn off, the WUS flag will go high, and current will be limited to less than 1 mA out of the head port.

WRITE UNSAFE

Any of the following conditions will be indicated as a high level on the Write Unsafe, WUS, open collector output.

- WDI frequency too low
- Device in Read mode
- Chip disabled
- No head current
- Head opened
- Head short to ground

To insure proper WUS operation, the product of write current, WDI frequency, and head inductance should be less than 500 mA•μH•MHz. To insure no false WUS trigger, the product of head current and head resistance (Ix,y•Rh) should be between 100 mV and 1.7V.

WDI frequency too low is detected if the WDI frequency falls below 500 kHz (typ). Consult the WUS Safe to Unsafe timing for range of frequency detection.

Device in Read mode and **Chip disabled** will flag WUS if R/$\overline{W}$ is high or $\overline{CS}$ is high.

No head current will flag WUS if Rwc = ∞ and the selected head is present.

Head opened will flag WUS if Rh = ∞ and under the condition that VCC/Iw < 0.25 V/mA.

Head short to ground is described in the preceding paragraph.

Upon entering write mode, WUS is valid after two high to low transitions of WDI following the required Read-Write transition time (0.6 μs max).

READ MODE

The Read mode configures the SSI 32R2026R as a low noise differential amplifier and deactivates the write current generator. The damping resistor is switched out of the circuit allowing a high impedance input to the read amplifier. The RDX and RDY output are driven by emitter followers. They should be AC coupled to the load. The (X,Y) inputs are non-inverting to the (X,Y) outputs. Unselected head potential is kept at ground.

Note that in Idle or Write mode, the read amplifier is deactivated and RDX, RDY outputs become high impedance. This facilitates multiple R/W applications (wired-OR RDX, RDY) and minimizes voltage drifts when switching from Write to Read mode. Note also that the write current source is deactivated for both the Read and Idle mode.

IDLE MODE

Taking $\overline{CS}$ high selects the idle mode which switches the RDX and RDY outputs into a high impedance state and deactivates the device. Power consumption in this mode is held to a minimum. Head potential is kept at ground.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may permanently damage the device.

PARAMETER		RATING
DC Supply Voltage	VCC1	-0.3 to +6 VDC
	VCC2	-0.3 to +6 VDC
Write Current	Iw	60 mA
Digital Input Voltage	Vin	-0.3 to VCC1 +0.3 VDC
Head Port Voltage	VH	-0.3 to VCC2 +0.3 VDC
Output Current: RDX, RDY	I0	-6 mA
WUS		+8 mA
Storage Temperature	Tstg	-65 to +150 °C

RECOMMENDED OPERATING CONDITIONS

DC Supply Voltage	VCC1 = VCC2	5 ±10%	VDC
Operating Junction Temperature	Tj	+25 to +135	°C
Recommended Head Load Range	Lh	0.3 - 5.0	µH

DC CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VCC1 Supply Current	Read Mode		18	25	mA
	Write Mode		22	29	mA
	Idle Mode		0.6	0.95	mA
VCC2 Supply Current	Read Mode		0	0.2	mA
	Write Mode		4 + Iw	7 + Iw	mA
	Idle Mode		0	0.2	mA
Power Dissipation	Read Mode		100	170	mW
	Write Mode		130 + 4 Iw	200 + 4.3 Iw	mW
	Idle Mode		3.3	6.5	mW
VCC1 Fault Voltage	Iw < 0.2 mA	3.5	3.9	4.2	VDC

DIGITAL INPUTS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Input Low voltage (Vil)				0.8	VDC
Input High Voltage (Vil)		2.0			VDC
Input Low Current	Vil = 0.8V	-0.4			mA
Input High Current	Vih = 2.0V			100	µA
WUS Output Low Voltage (Vol)	Iol = 2 mA max			0.5	VDC

WRITE CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified.

Write Current Constant "K"				0.99		
Write Current Voltage (Vwc)			1.15	1.25	1.35	V
Differential Head Voltage Swing			4.2	5.6		Vpp
	Open Head Iw = 20 mA		3.4	5.0		Vpp
Unselected Head Current					1	mA (pk)
Unselected Head Voltage				0	0.3	V
Head Differential Damping Resistance (Rd)				320		Ω
WDI Pulse Width	Vil ≥ 0.2V	PWH	10			ns
		PWL	5			ns
Write Current Range (Iw)			5		35	mA
Head Differential Load Capacitance					25	pF

READ CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified. CL (RDX, RDY) < 20 pF, RL (RDX, RDY) = 1 kΩ.

Differential Voltage Gain	Vin = 1 mVpp @1 MHz	250	300	350	V/V
Voltage BW -1dB	|Zs| < 5Ω, Vin = 1 mVpp	20			MHz
-3dB	|Zs| < 5Ω, Vin = 1 mVpp	45			MHz
Input Noise Voltage	BW = 15 MHz, Lh = 0, Rh = 0		0.56	0.75	nV/√Hz
Differential Input Capacitance	Vin = 1 mVpp, f = 5 MHz		16	22	pF
Differential Input Resistance	Vin = 1 mVpp, f = 5 MHz	720	1200		Ω
Dynamic Range	AC input voltage where gain falls to 90% of its small signal gain value, f = 5 MHz	2			mVpp
Common Mode Rejection Ratio	Vin = 0 VDC + 100 mVpp @ 5 MHz	55			dB

READ CHARACTERISTICS (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Power Supply Rejection Ratio	100 mVpp @ 5 MHz on VCC	50			dB
Channel Separation	Unselected channels driven with Vin = 0 VDC + 100 mVpp	55			dB
Output Offset Voltage				±300	mV
Single Ended Output Resistance	f = 5 MHz			50	Ω
Output Current	AC coupled load, RDX to RDY	0.9			mA
RDX, RDY Common Mode Output Voltage		0.4 VCC	VCC/2	0.6 VCC	VDC

SWITCHING CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified. IW = 20 mA, Lh = 1.0 µH, Rh = 30Ω f(Data) = 5 MHz.

R/$\overline{W}$	Read to Write	R/W to 90% of write current		0.1	0.6	µs
	Write to Read	R/W to 90% of 100 mV Read signal envelope		0.3	1	µs
$\overline{CS}$	Unselect to Select	$\overline{CS}$ to 90% of write current or to 90% of 100 mV 10 MHz		0.2	1	µs
	Select to Unselect	$\overline{CS}$ to 10% of write current		0.11	0.6	µs
HS0,1 to any Head		To 90% of 100 mV 10 MHz Read signal envelope		0.11	0.6	µs
WUS:	Safe to Unsafe (TD1)	Write mode, loss of WDI transitions. Defines maximum WDI period for WUS operation	0.6	2.0	3.6	µs
	Unsafe to Safe (TD2)	Fault cleared, from first neg WDI transition		0.1	0.6	µs
Head Current:						
	WDI to Ix - Iy (TD3)	from 50% points, Lh = 0, Rh = 0		3	10	ns
	Asymmetry	WDI has 1 ns rise/fall time, Lh = 0, Rh = 0			1.0	ns
	Rise/fall Time	10% to 90% points, Lh = 0, Rh = 0		4	6	ns
	Rise/fall Time	Lh = 1 µH, Rh = 30Ω		15		ns

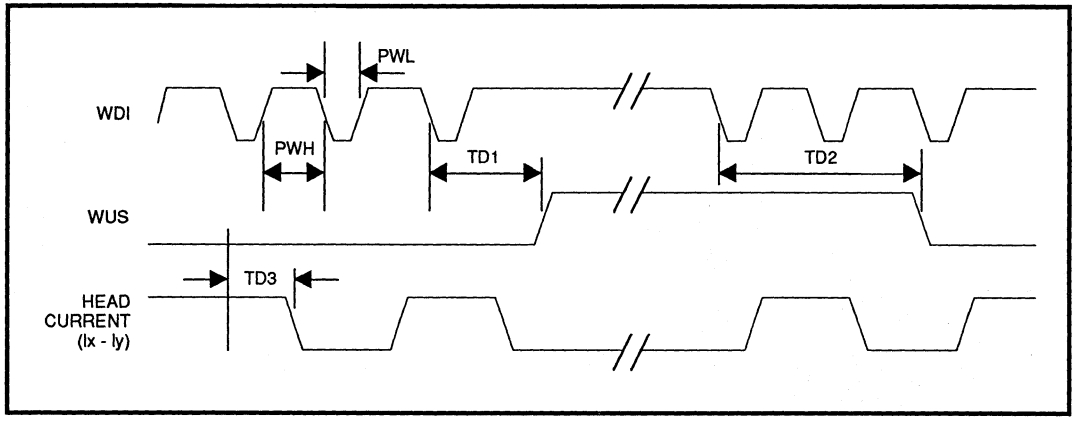
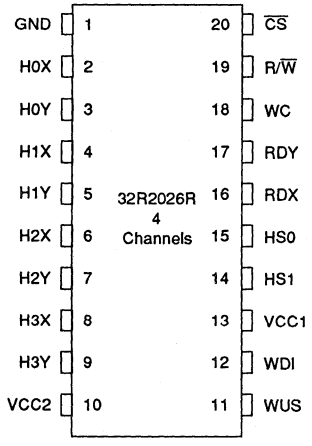


FIGURE 1: Write Mode Timing Diagram

PACKAGE PIN DESIGNATIONS

(Top View)



20-Lead SOL, SOV

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

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Notes:

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SSI 32R2028R
5V, 10-Channel
Thin-Film Read/Write Device

Advance Information

December 1993

3

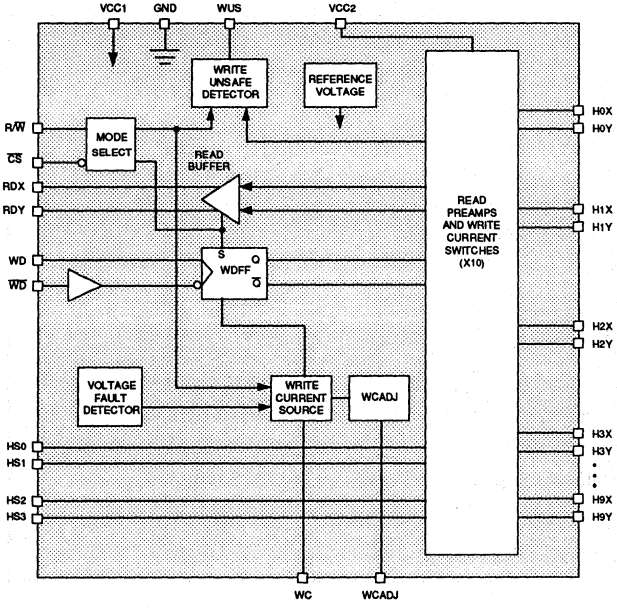
DESCRIPTION

The SSI 32R2028R is a bipolar monolithic integrated circuit designed for use with two-terminal recording heads. It provides a low noise read amplifier, write current control, and data protection circuitry for up to ten channels. The device provides internal 320Ω damping resistors that are switched in during Write mode and switched out during Read mode. Power supply fault protection is provided by disabling the write current generator during power sequencing. System write to read recovery time is significantly improved by controlling the read channel Common mode output voltage shift in the Write mode. The device also provides the user with a controllable write current adjustment feature. The SSI 32R2028R requires only a +5V power supply.

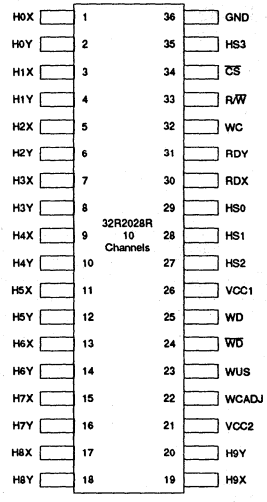
FEATURES

- +5V ±10% supply
- Low power
  - PD = 130 mW Read mode (Nom)
  - PD = 5 mW idle (Max)
- High Performance:
  - Read mode gain = 300 V/V
  - Input noise = 0.56 nV/√Hz (Nom)
  - Input capacitance = 16 pF (Nom)
  - Write current range = 5-35 mA
- Self switching damping resistance
- Designed for two-terminal thin-film or MIG heads with inductance up to 5.0 μH
- Differential ECL-like Write Data Input
- Write unsafe detection
- Power supply fault protection
- Head short to ground protection

BLOCK DIAGRAM



PIN DIAGRAM



36-Lead SOM

CAUTION: Use handling procedures necessary for a static sensitive component.

CIRCUIT OPERATION

The SSI 32R2028R has the ability to address up to 10 two-terminal heads and provide write drive or read amplification. Mode control and head selection are described in Tables 1 and 2. The TTL inputs R/$\overline{W}$ and $\overline{CS}$ have internal pull-up resistors to prevent an accidental write condition. HS0, HS1, HS2 and HS3 have internal pulldown resistors. Internal clamp circuitry will protect the IC from a head short to ground condition in any mode.

TABLE 1: Mode Select

$\overline{CS}$	R/$\overline{W}$	Mode
0	0	Write
0	1	Read
1	0	Idle
1	1	Idle

TABLE 2: Head Select

HS3	HS2	HS1	HS0	Head
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
HS0, HS1, † HS2, HS3	I	Head Select: selects one of ten heads
$\overline{CS}$	I	Chip Select: a high inhibits the chip
R/$\overline{W}$ †	I	Read/Write: a high selects Read mode
WUS †	O	Write Unsafe: a high indicates an unsafe writing condition
WD, $\overline{WD}$ †	I	Differential Write Data Input: a negative transition of (WD - $\overline{WD}$) toggles the direction of the head current
H0X - H9X; H0Y - H9Y	I/O	X, Y Head Connections
RDX, RDY †	O	X, Y Read Data: differential read data output
WC †		Write Current: used to set the magnitude of the write current
WCADJ †		Write Current Adjust: Used to fine tune the write current
VCC1	I	+5V Supply
VCC2	I	+5V Supply for Write current drivers
GND	I	Ground
†When more than one R/W device is used, signals can be wire OR'ed		

WRITE MODE

Taking both $\overline{CS}$ and R/$\overline{W}$ low selects Write mode which configures the SSI 32R2028R as a current switch and activates the Write Unsafe (WUS) detector circuitry. Head current is toggled between the X and Y side of the selected head on each high to low transition of the differential signal WD - $\overline{WD}$. Changing from Read or Idle mode to Write mode initializes the Write Data Flip-Flop to pass write current into the "X" pin. In this case, the Y side of the head will be higher potential than the X side. The magnitude of the write current (0-pk) is given by:

$$Iw = \frac{K \cdot Vwc}{Rwc}$$

Rwc is connected from pin WC to GND. Note the actual head current Ix, y is given by:

$$Ix, y = \frac{Iw}{1 + Rh/Rd}$$

Where:

Rh = Head resistance plus external wire resistance

Rd = Damping resistance

In Write mode a 320Ω damping resistor is switched in across the Hx, Hy ports.

The SSI 32R2028R includes a feature which allows the user to adjust the Iw current by a finite amount. The WCADJ pin is used to adjust write current for write operations on different zones of the disk. It is used by switching a separate write current adjust resistor in and out on the WCADJ pin or by connecting a DAC to that pin to sink a controllable amount of current. The WCADJ pin is nominally biased to VCC/2. Sinking current from this pin to ground will divert a proportional amount of current from the actual head current while maintaining a constant current through the WC resistor and VCC. Allowing WCADJ to float or pulling it high will cut off the circuit and it will have no effect. A TTL gate can be used as a switch with a small degradation in accuracy. The amount of write current decrease is shown below:

Iw head (decrease) (mA) = (29 • V_{WCADJ}/R_{WCADJ})

where:

V_{WCADJ} = VCC/2 (volts)

R_{WCADJ} = write current adjust setting resistor (kΩ)

Example: For a 7.25 mA head current decrease, R_{WCADJ} = (27 • 2.5) / 7.25 = 10 kΩ

POWER SUPPLY FAULT PROTECTION

A voltage fault detection circuit improves data security by disabling the write current generator during a voltage fault or power startup regardless of mode. Note that WUS does not necessarily turn on to flag a power supply fault condition.

HEAD SHORT TO GROUND PROTECTION

The SSI 32R2028R provides a head short to ground protection circuit in any mode. In Idle or Read Mode, current out of the head port will not exceed 20 mA if any head is shorted to ground. In Write mode, if any head is shorted to ground (regardless if it is selected or not) the write current generator will turn off, the WUS flag will go high, and current will be limited to less than 1 mA out of the head port.

WRITE UNSAFE

Any of the following conditions will be indicated as a high level on the Write Unsafe, WUS, open collector output.

- WD frequency too low
- Device in Read mode
- Chip disabled
- No head current
- Head opened
- Head short to ground

To insure proper WUS operation, the product of write current, WD frequency, and head inductance should be less than 500 mA•μH•MHz. To insure no false WUS trigger, the product of head current and head resistance (Ix,y•Rh) should be between 100 mV and 1.7V.

WD frequency too low is detected if the WD frequency falls below 500 kHz (typ). Consult the WUS Safe to Unsafe timing for range of frequency detection.

Device in Read mode and **Chip disabled** will flag WUS if R/$\overline{W}$ is high or $\overline{CS}$ is high.

No head current will flag WUS if Rwc = ∞ and the selected head is present.

Head opened will flag WUS if Rh = ∞ and under the condition that VCC/Iw < 0.25 V/mA.

Head short to ground is described in the preceding paragraph.

Upon entering Write mode, WUS is valid after two transitions of WD following the required Read-Write transition time (0.6 μs max).

CIRCUIT OPERATION (continued)

READ MODE

The Read mode configures the SSI 32R2028R as a low noise differential amplifier and deactivates the write current generator. The damping resistor is switched out of the circuit allowing a high impedance input to the read amplifier. The RDX and RDY output are driven by emitter followers. They should be AC coupled to the load. The (X,Y) inputs are non-inverting to the (X,Y) outputs.

Note that in Idle or Write mode, the read amplifier is deactivated and RDX, RDY outputs become high impedance. This facilitates multiple R/W applications (wired-OR RDX, RDY) and minimizes voltage drifts when switching from Write to Read mode. Note also that the write current source is deactivated for both the Read and Idle mode.

IDLE MODE

Taking $\overline{CS}$ high selects the Idle mode which switches the RDX and RDY outputs into a high impedance state and deactivates the device. Power consumption in this mode is held to a minimum.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may permanently damage the device.

PARAMETER		RATING
DC Supply Voltage	VCC1	-0.3 to +6 VDC
	VCC2	-0.3 to +6 VDC
Write Current	Iw	60 mA
Digital Input Voltage	Vin	-0.3 to VCC1 +0.3 VDC
Head Port Voltage	VH	-0.3 to VCC2 +0.3 VDC
Output Current: RDX, RDY WUS	I0	-6 mA +8 mA
Storage Temperature	Tstg	-65 to +150 °C

RECOMMENDED OPERATING CONDITIONS

DC Supply Voltage	VCC1 = VCC2	5 ±10%	VDC
Operating Junction Temperature	Tj	+25 to +135	°C
Recommended Head Load Range	Lh	0.3 - 5.0	µH

DC CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VCC1 Supply Current	Read Mode		18	25	mA
	Write Mode		22	29	mA
	Idle Mode		0.6	0.9	mA
VCC2 Supply Current	Read Mode		8	11	mA
	Write Mode		4 + Iw	7 + Iw	mA
	Idle Mode		0	0.2	mA

DC CHARACTERISTICS (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Power Dissipation	Read Mode		130	200	mW
	Write Mode		130 + 4 Iw	200 + 4.3 Iw	mW
	Idle Mode		3	5	mW
VCC1 Fault Voltage	Iw < 0.2 mA	3.5	3.9	4.2	VDC

DIGITAL INPUTS

Input Low voltage (Vil) HSX, $\overline{CS}$, R/$\overline{W}$				0.8	VDC
Input High Voltage (Vil) HSX, $\overline{CS}$, R/$\overline{W}$		2.0			VDC
Input Low Current, HSX, $\overline{CS}$, R/$\overline{W}$	Vil = 0.8V	-0.4			mA
Input High Current, HSX, $\overline{CS}$, R/$\overline{W}$	Vih = 2.0V			100	µA
WD, $\overline{WD}$ Input Low Current	Vil = VCC - 1.75V		70	100	µA
WD, $\overline{WD}$ Input High Current	Vih = VCC - 0.75V		85	125	µA
WD, $\overline{WD}$ Input Low Voltage Vil		Vcc -1.870		Vcc - 1.625	VDC
WD, $\overline{WD}$ Input High Voltage Vih		Vcc - 1.50		Vcc - 0.5	VDC
WUS Output Low Voltage (Vol)	Iol = 2 mA max			0.5	VDC

WRITE CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified.

Write Current Constant "K"				0.99		
Write Current Voltage (Vwc)			1.15	1.25	1.35	V
WCADJ Voltage	I_{WCADJ} = 0 to .5 mA		2.0	VCC/2	3.0	VDC
Ihead(Decrease)/I_{WCADJ}			23	27	31	mA/mA
I_{WCADJ} Range			0.0		0.5	mA
Differential Head Voltage Swing			4.2	5.6		Vpp
	Open Head, Iw = 20 mA		3.4	5.0		
Unselected Head Current					1	mA (pk)
Head Differential Damping Resistance (Rd)				320		Ω
WD Pulse Width	Vil ≥ 0.2V	PWH	10		ns	
		PWL	5			ns
Write Current Range (Iw)			5		35	mA
Head Differential Load Capacitance					25	pF

READ CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified. CL (RDX, RDY) < 20 pF, RL (RDX, RDY) = 1 kΩ.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Differential Voltage Gain	Vin = 1 mVpp @1 MHz	250	300	350	V/V
Voltage BW -1dB	|Zs| < 5Ω, Vin = 1 mVpp	20			MHz
-3dB	|Zs| < 5Ω, Vin = 1 mVpp	40	45		MHz
Input Noise Voltage	BW = 15 MHz, Lh = 0, Rh = 0		0.56	0.75	nV/√Hz
Differential Input Capacitance	Vin = 1 mVpp, f = 5 MHz		16	22	pF
Differential Input Resistance	Vin = 1 mVpp, f = 5 MHz	720	1200		Ω
Dynamic Range	AC input voltage where gain falls to 90% of its small signal gain value, f = 5 MHz	2			mVpp
Common Mode Rejection Ratio	Vin = 0 VDC + 100 mVpp @ 5 MHz	55			dB
Power Supply Rejection Ratio	100 mVpp @ 5 MHz on VCC	50			dB
Channel Separation	Unselected channels driven with Vin = 0 VDC + 100 mVpp	55			dB
Output Offset Voltage				±300	mV
Single Ended Output Resistance	f = 5 MHz			50	Ω
Output Current	AC coupled load, RDX to RDY	0.9			mA
RDX, RDY Common Mode Output Voltage		0.4 VCC	VCC/2	0.6 VCC	VDC

SWITCHING CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified. IW = 20 mA, Lh = 1.0 µH, Rh = 30Ω f(Data) = 5 MHz.

R/$\overline{W}$	Read to Write	R/W to 90% of write current		0.1	0.6	µs
	Write to Read	R/W to 90% of 100 mV Read signal envelope		0.1	0.6	µs
$\overline{CS}$	Unselect to Select	$\overline{CS}$ to 90% of write current or to 90% of 100 mV 10 MHz		0.2	1	µs
	Select to Unselect	$\overline{CS}$ to 10% of write current		0.11	0.6	µs
HS0,1 to any Head		To 90% of 100 mV 10 MHz Read signal envelope		0.11	0.6	µs
WUS:	Safe to Unsafe (TD1)	Write mode, loss of WDI 0.6 transitions. Defines maximum WDI period for WUS operation	2.0	3.6	µs	
	Unsafe to Safe (TD2)	Fault cleared, from first neg WDI transition		0.1	0.6	µs

SWITCHING CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified. IW = 20 mA, Lh = 1.0 µH, Rh = 30Ω

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Head Current:					
WD to Ix - Iy (TD3)	from 50% points, Lh = 0, Rh = 0		8	12	ns
Asymmetry	WDI has 1 ns rise/fall time,				
	Lh = 0, Rh = 0			1.0	ns
Rise/fall Time	10% to 90% points, Lh = 0, Rh = 0		4	6	ns
Rise/fall Time	Lh = 1 µH, Rh = 30Ω		15		ns

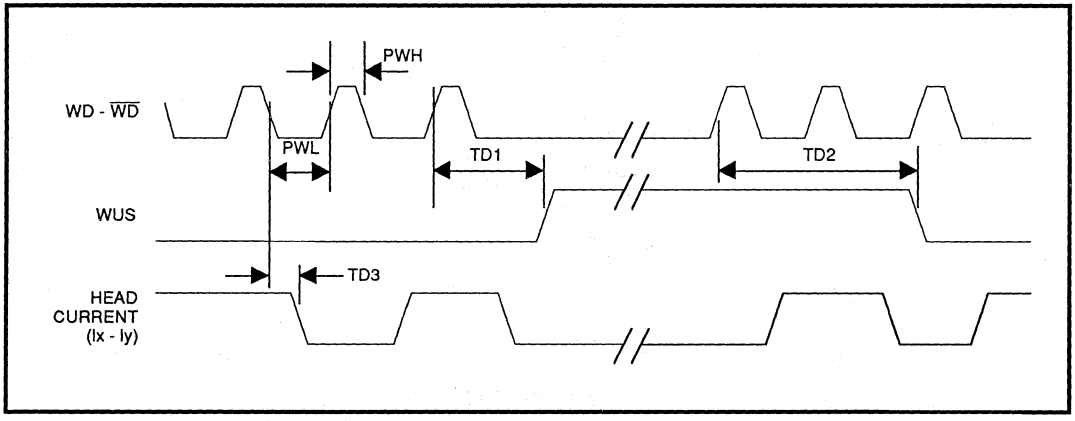
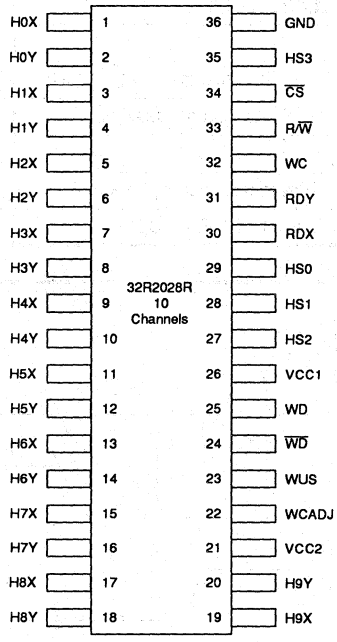


FIGURE 1: Write Mode Timing Diagram

SSI 32R2028R
5V, 10-Channel
Thin-Film Read/Write Device

PACKAGE PIN DESIGNATIONS

(Top View)



36-Lead SOM

CAUTION: Use handling procedures necessary for a static sensitive component.

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914

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SSI 32R2030A/2031A
5V, 2, 4-Channel Thin-Film Read/Write Device

January 1994

3

DESCRIPTION

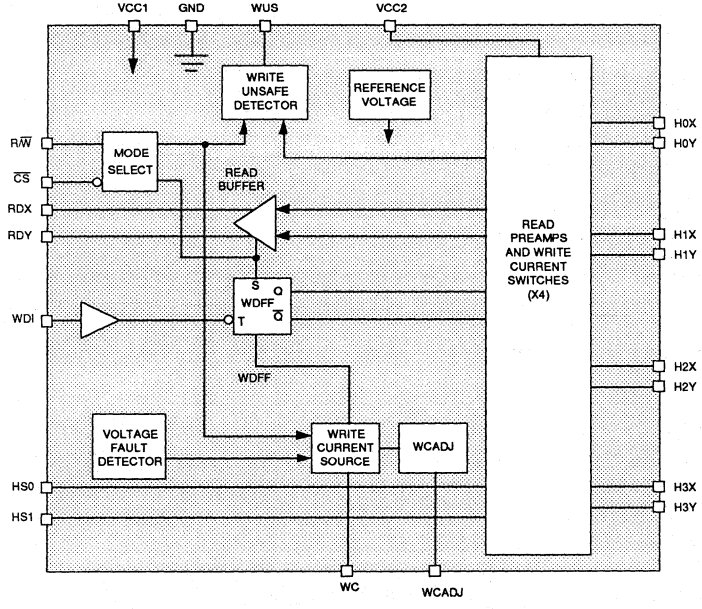
The SSI 32R2030A/2031A are bipolar monolithic integrated circuits designed for use with two-terminal thin-film recording heads. They provide a low noise read amplifier, write current control, and data protection circuitry for up to four channels. The SSI 32R2030AR/2031AR option provides internal 700Ω damping resistors. Power supply fault protection is provided by disabling the write current generator during power sequencing. System write to read recovery time is significantly improved by controlling the read channel common mode output voltage shift in the write mode. The 32R2031A option provides for an additional feature providing the user with a controllable write current adjustment feature.

The SSI 32R2030A/2031A require only +5V power supplies and are available in a variety of packages.

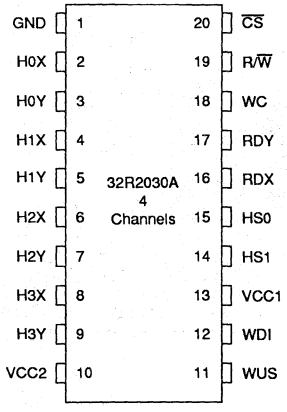
FEATURES

- **5V ±10%**
- **Low power**
  - **PD = 175 mW read mode (Nom)**
- **High Performance:**
  - **Read mode gain = 250 V/V**
  - **Input noise = 0.85 nV/√Hz max**
  - **Input capacitance = 35 pF max**
  - **Write current range = 10-35 mA**
- **Designed for two-terminal thin-film heads or MIG heads up to 5 μH**
- **Programmable write current source**
- **Write unsafe detection**
- **Enhanced system write to read recovery time**
- **Power supply fault protection**
- **Head short to ground protection**

BLOCK DIAGRAM



PIN DIAGRAM



20-PIN SOL

CAUTION: Use handling procedures necessary for a static sensitive component.

WCADJ available on the 32R2031A 24-pin option only

SSI 32R2030A/2031A
5V, 2, 4-Channel Thin-Film Read/Write Device

CIRCUIT OPERATION

The SSI 32R2030A/2031A has the ability to address up to 4 two-terminal thin-film heads and provide write drive or read amplification. Head selection and mode control are described in Tables 2 and 3. The TTL inputs R/$\overline{W}$ and $\overline{CS}$ have internal pull-up resistors to prevent an accidental write condition. HS0, and HS1 have internal pulldowns. Internal clamp circuitry will protect the IC from a head short to ground condition in any mode.

TABLE 1: Mode Select

$\overline{CS}$	R/$\overline{W}$	Mode
0	0	Write
0	1	Read
1	0	Idle
1	1	Idle

TABLE 2: Head Select

HS1	HS0	Head
0	0	0
0	1	1
1	0	2
1	1	3

PIN DESCRIPTION

NAME		TYPE	DESCRIPTION
HS0, HS1		I	Head Select: selects one of four heads
$\overline{CS}$		I	Chip Select: a high inhibits the chip
R/$\overline{W}$	†	I	Read/Write : a high selects Read mode
WUS	†	O	Write Unsafe: a high indicates an unsafe writing condition
WDI	†	I	Write Data In: changes the direction of the current in the recording head
H0X - H7X; H0Y - H7Y		I/O	X, Y Head Connections
RDX, RDY	†	O	X, Y Read Data: differential read data output
WC	†		Write Current: used to set the magnitude of the write current
WCADJ*	†		Write Current Adjust: Used to decrease the write current by a finite amount
VCC1		I	+5V Supply
VCC2		I	+5V Supply for Write current drivers
GND		I	Ground

*Available on 32R2031A 24-pin option only

† These signals can be wire OR'ed

WRITE MODE

Taking both $\overline{CS}$ and R/$\overline{W}$ low selects write mode which configures the SSI 32R2030A/2031A as a current switch and activates the Write Unsafe (WUS) detector circuitry. Head current is toggled between the X and Y side of the selected head on each high to low transition of the Write Data Input (WDI). The WDI input pulse width requirement is amplitude dependent and pull ups are recommended at higher data rates, please refer to the WDI pulse width specifications. Note that a preceding read or idle mode select initializes the Write Data Flip-Flop to pass write current through the "X" side of the head. The magnitude of the write current (0-pk) is given by:

$$IW = \frac{K \cdot VWC}{RWC}$$

RWC is connected from pin WC to GND. Note the actual head current Ix, y is given by:

$$Ix, y = \frac{Iw}{1 + Rh/Rd}$$

Where:

Rh = Head resistance plus external wire resistance

Rd = Damping resistance

Any of the following conditions will be indicated as a high level on the Write Unsafe, WUS, open collector output.

- WDI frequency too low
- Device in Read mode
- Chip disabled
- No write current

After fault condition is removed, one negative transition on WDI is required to clear WUS.

The 32R2031A adds a feature which allows the user to adjust the Iw current by a finite amount. The WCADJ pin is used to adjust write current for write operations on different zones of the disk. It is used by switching a separate write current adjust resistor in and out on the WCADJ pin or by connecting a DAC to that pin to sink a controllable amount of current. The WCADJ pin is nominally biased to VCC/2. Sinking current from this pin to ground will divert a proportional amount of current from the actual head current while maintaining a constant current through the WC resistor and VCC. Allowing WCADJ to float or pulling it high will cut off the circuit and it will have no effect. For example, if the nominal head current is set to 30 mA through WC with WCADJ open, then for a 7.25 mA head current decrease, a 10 kΩ resistor would be connected from the WCADJ pin to ground. A TTL gate could be used as a switch with a small degradation in accuracy. To perform the same function, a DAC could be used, by programming it to sink 0.25 mA from the WCADJ pin.

Iw head (Decrease) = (29 • V_{WCADJ} / R_{WCADJ})

Where:

VWCADJ = Voltage on WCADJ pin = VCC/2

RWCADJ = Write current adjust setting resistor

VOLTAGE FAULT

A voltage Fault detection circuit improves data security by disabling the write current generator during a voltage fault or power startup regardless of mode.

READ MODE

The Read mode configures the SSI 32R2030A/2031A as a low noise differential amplifier and deactivates the write current generator. The RDX and RDY output are driven by emitter followers. They should be AC coupled to the load. The (X,Y) inputs are non-inverting to the (X,Y) outputs.

Note that in Idle or Write mode, the read amplifier is deactivated and RDX, RDY outputs become high impedance. This facilitates multiple R/W applications (wired-OR RDX, RDY) and minimizes voltage drifts when switching from Write to Read mode. Note also that the write current source is deactivated for both the Read and Idle mode.

IDLE MODE

Taking $\overline{CS}$ high selects the idle mode which switches the RDX and RDY outputs into a high impedance state and deactivates the device. Power consumption in this mode is held to a minimum.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may permanently damage the device.

PARAMETER		RATING
DC Supply Voltage	VCC1	-0.3 to +7 VDC
	VCC2	-0.3 to +7 VDC
Write Current	IW	80 mA
Digital Input Voltage	Vin	-0.3 to VCC1 +0.3 VDC
Head Port Voltage	VH	-0.3 to VCC2 +0.3 VDC
Output Current: RDX, RDY	I0	-10 mA
	WUS	+12 mA
Storage Temperature	Tstg	-65 to +150°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		RATING
DC Supply Voltage	VCC1	5 ±10% VDC
	VCC2	5 ±10% VDC
Operating Junction Temperature	Tj	+25 to +110°C

DC CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified.

PARAMETER	CONDITIONS		MIN	NOM	MAX	UNIT
VCC1 Supply Current	Read Mode	(Vcc ±5%)	23	28	33	mA
		(Vcc ±10%)	19	28	37	mA
	Write Mode	(Vcc ±5%)	21	24	27	mA
		(Vcc ±10%)	17	24	31	mA
*Head Select Pins	*Idle Mode	(Vcc ±5%)	6	9	12	mA
(HS0, HS1) Floating		(Vcc ±10%)	4	9	14	mA
VCC2 Supply Current	Read Mode	(Vcc ±5%)	5	8	11	mA
		(Vcc ±10%)	4	8	12	mA
	Write Mode	(Vcc ±5%)	6	8 + Iw	10 + Iw	mA
		(Vcc ±10%)	5	8 + Iw	11 + Iw	mA
	Idle Mode	(Vcc ±5%)	0.1	0.2	0.4	mA
		(Vcc ±10%)	0.1	0.2	0.5	mA
Power Dissipation	Read Mode	(Vcc ±5%)		175	230	mW
		(Vcc ±10%)			270	mW

DC CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS		MIN	NOM	MAX	UNIT
Power Dissipation (Continued)	Write Mode	(Vcc ±5%)		150 + 4Iw	190 + 4Iw	mW
		(Vcc ±10%)			230 + 4.4Iw	mW
	Idle Mode	(Vcc ±5%)		50	65	mW
		(Vcc ±10%)			80	mW
VCC1 Fault Voltage	IW < 0.2 mA		3.8	4.0	4.2	VDC

DIGITAL INPUTS

Input Low voltage (VIL)				0.8	VDC
Input High Voltage (VIH)		2.0			VDC
Input Low Current	VIL = 0.8V	-0.4			mA
Input High Current	VIH = 2.0V			100	µA
WUS Output Low Voltage (VOL)	Iol = 2 mA max			0.5	VDC

WRITE CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified.

Write Current Constant "K"		0.96	0.99		
Write Current Voltage (VWC)		1.15	1.25	1.35	V
WCADJ Voltage SSI 32R2031A/2031AR	I_{WCADJ} = 0 to .5 mA	2.0	VCC/2	3.0	VDC
Ihead(Decrease)/I_{WCADJ} SSI 32R2031A/2031AR		26	29	32	mA/mA
I_{WCADJ} Range SSI 32R2031A/2031AR		0.0		0.5	mA
Differential Head Voltage Swing	Ih (p-p) • Rh not to exceed 3.4V (Head Swing Min)	3.4			Vpp
Unselected Head Current				0.02 Iw	mApk
Head Differential Load Capacitance				25	pF
Head Differential Load	SSI 32R2030A/32R2031A	4K			Ω
Resistance (Rd)	SSI 32R2030AR/32R2031AR	560	700	950	Ω
WDI Pulse Width	Vil = 0.2V, Vih = 2.4V PWH	37			ns
(Ref: Figure 1)	PWL	5			ns
	Vil = 0.2V, Vih = VCC PWH	20			ns
	PWL	5			ns
Write Current Range (IW)		10		35	mA

READ CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified. CL (RDX, RDY) < 20 pF, RL (RDX, RDY) = 1 kΩ.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Differential Voltage Gain		Vin = 1 mVpp @1 MHz	200	250	300	V/V
Voltage BW	-1dB	|Zs| < 5Ω, Vin = 1 mVpp	20	60		MHz
	-3dB		35	70		MHz
Input Noise Voltage		BW = 15 MHz, Lh = 0, Rh = 0		0.6	0.85	nV/√Hz
Differential Input Capacitance		Vin = 1 mVpp, f = 5 MHz		27	35	pF
Differential Input Resistance		Vin = 1 mVpp, f = 5 MHz SSI 32R2030A/2031A	835	2600		Ω
		SSI 32R2030AR/2031AR	360	550		Ω
Dynamic Range		AC input voltage where gain falls to 90% of its small signal gain value, f = 5 MHz	3	6		mVpp
Common Mode Rejection Ratio		Vin = 0 VDC + 100 mVpp @ 5 MHz	45	80		dB
Power Supply Rejection Ratio		100 mVpp @ 5 MHz on VCC	40	70		dB
Channel Separation		Unselected channels driven with Vin = 0 VDC + 100 mVpp	45			dB
Output Offset Voltage			-300		+300	mV
Single Ended Output Resistance		f = 5 MHz			40	Ω
Output Current		AC coupled load, RDX to RDY	1.4			mA
RDX, RDY Common Mode Output Voltage			2.0	VCC1/2	3.5	VDC

SWITCHING CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified. IW = 20 mA, Lh = 1.0 µH, Rh = 30Ω f(Data) = 5 MHz.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
R/$\overline{W}$	Read to Write	R/W to 90% of write current		0.1	1.0	µs
	Write to Read	R/W to 90% of 100 mV Read signal envelope		0.5	1.0	µs
$\overline{CS}$	Unselect to Select	$\overline{CS}$ to 90% of write current or to 90% of 100 mV 10 MHz		0.4	1.0	µs
	Select to Unselect	$\overline{CS}$ to 10% of write current		0.4	1.0	µs
HS0,1 to any Head		To 90% of 100 mV 10 MHz Read signal envelope		0.2	1.0	µs
WUS:	Safe to Unsafe (TD1)	Write mode, loss of WDI transitions. Defines maximum WDI period for WUS operation	0.6	2.0	3.6	µs
	Unsafe to Safe (TD2)	Fault cleared from first neg WDI transition		0.2	1.0	µs
Head Current:		Lh = 0, Rh = 0				
	WDI to Ix - Iy (TD3)	from 50% points		20	32	ns
	Asymmetry	WDI has 1 ns rise/fall time			1.0	ns
	Rise/fall Time	10% to 90% points		6	12	ns

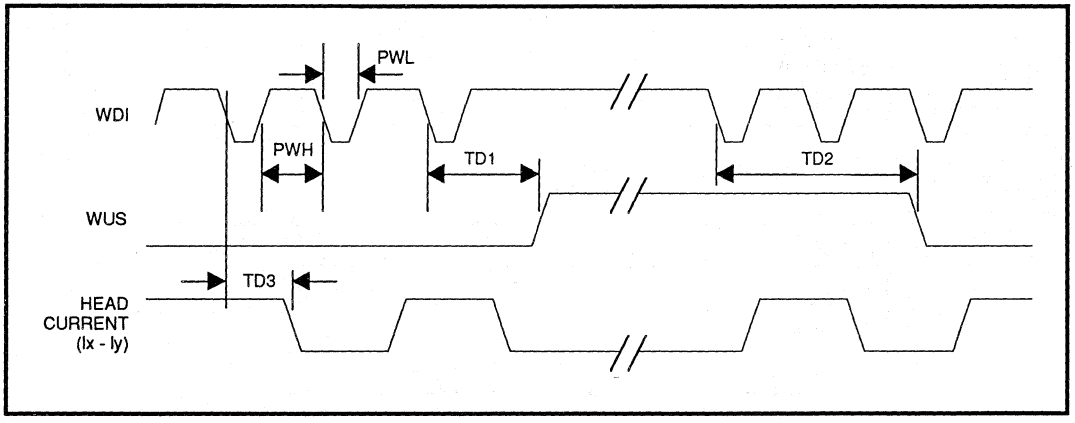


FIGURE 1: Write Mode Timing Diagram

Worst Case Read Input Noise Voltage vs. Input Impedance for SSI 32R2030AR/2031AR

Case 1: IC Base sheet resistance = Maximum
Hence, IC bias Current = Minimum

	Tj = 25°C	Tj = 110°C	Units
Vn (Max)	.7	0.85	$nV/\sqrt{Hz}$
Rin (Min)	450	475	Ω
Cin (Max)	28	30	pF

Case 2: IC Base sheet resistance = Minimum
Hence, IC bias Current = Maximum

	Tj = 25°C	Tj = 110°C	Units
Vn (Max)	.58	.65	$nV/\sqrt{Hz}$
Rin (Min)	360	400	Ω
Cin (Max)	33	35	pF

Worst Case Read Input Noise Voltage vs. Input Impedance for SSI 32R2030A/2031A

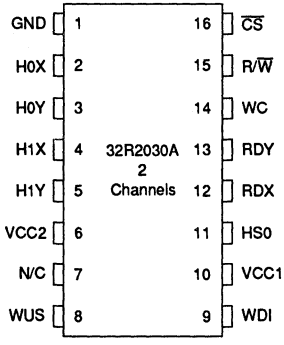
Case 1: IC Base sheet resistance = Maximum
Hence, IC bias Current = Minimum

	Tj = 25°C	Tj = 110°C	Units
Vn (Max)	.7	0.85	$nV/\sqrt{Hz}$
Rin (Min)	1525	1895	Ω
Cin (Max)	28	30	pF

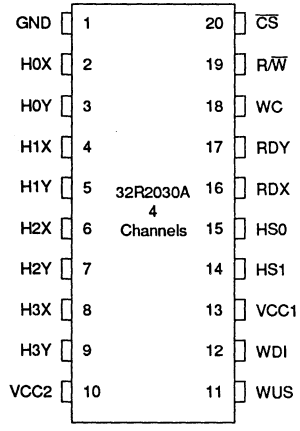
Case 2: IC Base sheet resistance = Minimum
Hence, IC bias Current = Maximum

	Tj = 25°C	Tj = 110°C	Units
Vn (Max)	.58	.65	$nV/\sqrt{Hz}$
Rin (Min)	835	1100	Ω
Cin (Max)	33	35	pF

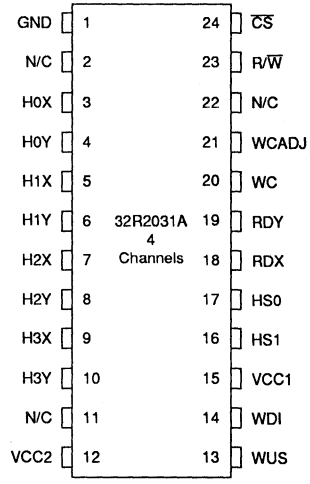
PACKAGE PIN DESIGNATIONS
(Top View)



16-Pin SOL



20-Pin SOL, SOV



24-Pin SOL, SOV

THERMAL CHARACTERISTICS: θja

16-Pin SOL	105°C/W
20-Pin SOL	95°C/W
20-Pin SOV	125°C/W
24-Pin SOL	80°C/W

ORDERING INFORMATION

PART DESCRIPTION	ORDER NUMBER	PACKAGE MARK
SSI 32R2030A		
16-Pin SOL	32R2030A-2CL	32R2030A-2CL
20-Pin SOL	32R2030A-4CL	32R2030A-4CL
20-Pin SOV	32R2030A-4CV	32R2030A-4CV
SSI 32R2031A		
24-Pin SOL	32R2031A-4CL	32R2031A-4CL
24-Pin SOV	32R2031A-4CV	32R2031A-4CV

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914

Notes:

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SSI 32R2041RW
4, 6-Channel, Two-Terminal Read/Write Device
Advance Information

December 1993

3

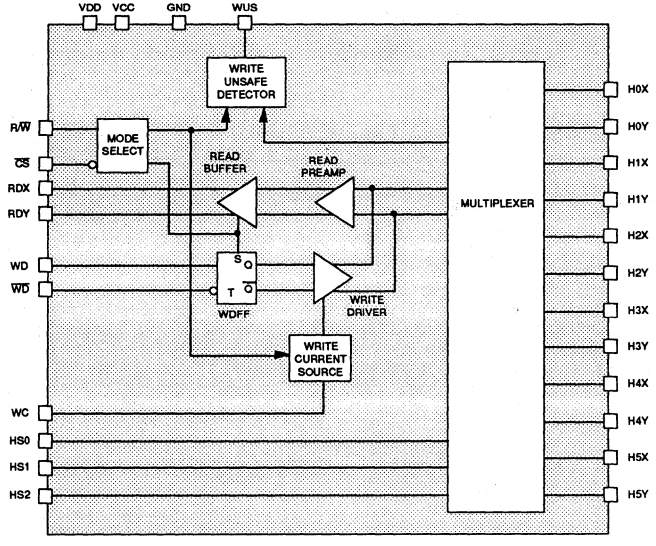
DESCRIPTION

The SSI 32R2041RW Read/Write device is a bipolar monolithic integrated circuit designed for use with two-terminal thin-film recording heads. It provides a low noise read amplifier, write current control and data protection circuitry for up to 6 channels. Power supply fault protection is provided by disabling the write current generator during power sequencing. System write to read recovery time is significantly improved by controlling the read channel common mode output voltage shift in the write mode. The SSI 32R2041RW requires +5V and +12V power supplies, and provides internal 700Ω damping resitors.

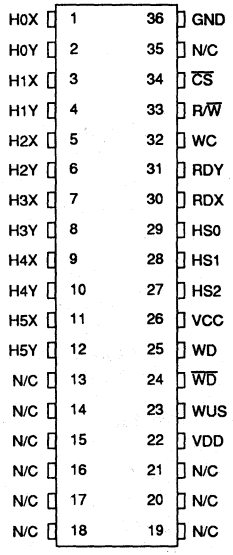
FEATURES

- **High performance:**
  - **Read mode gain = 250 V/V**
  - **Input noise = 0.80 nV/√Hz max.**
  - **Input capacitance = 22 pF max.**
  - **Write current range = 10 mA to 40 mA**
  - **Head voltage swing = 7 Vpp**
  - **Write current rise time = 9 ns**
- **Enhanced system write to read recovery time**
- **Differential ECL-like Write Data input**
- **Power supply fault protection**
- **Write unsafe detection**
- **+5V, +12V power supplies**

BLOCK DIAGRAM



PIN DIAGRAM



36-LEAD SOM
6-Channel

CAUTION: Use handling procedures necessary for a static sensitive component.

SSI 32R2041RW
4, 6-Channel, Two-Terminal Read/Write Device

CIRCUIT OPERATION

The SSI 32R2041RW addresses up to 6 two-terminal thin film heads providing write drive or read amplification. Head selection and mode control is accomplished with pins HSn, $\overline{CS}$ and R/$\overline{W}$, as shown in Tables 1 & 2. Internal resistor pullups, provided on pins $\overline{CS}$ and R/$\overline{W}$ will force the device into a non-writing condition if either control line is opened accidentally.

WRITE MODE

The write mode configures the SSI 32R2041RW as a current switch and activates the Write Unsafe (WUS) detection circuitry. Write current is toggled between the X and Y direction of the selected head on each low to high transition on the WD, Write Data input. (See figure 1.)

A preceding read operation initializes the Write Data Flip Flop (WDFF) to pass write current in the X-direction of the head, i.e., into the X-port of the head. HnX will be biased higher than HnY.

The magnitude of the write current (0-pk) is given by:

$$Iw = \frac{Vwc}{Rwc}$$

where Vwc (WC pin voltage) = 1.65V ± 5%, is programmed by an external resistor Rwc, connected from pin WC to ground. In multiple device applications, a single Rwc resistor may be made common to all devices. The actual head current Ix, y is given by:

$$Ix,y = \frac{Iw}{1+Rh/Rd}$$

where:
Rh = head resistance + external wire resistance, and
Rd = damping resistance.

Power supply fault protection improves data security by disabling the write current generator during a voltage fault or power supply sequencing. Additionally, the write unsafe detection circuitry will flag any of the conditions listed below as a high level on the open collector output pin, WUS. Up to two positive transitions on the WD, Write Data input line, after the fault is corrected, are required to clear the WUS flag.

- WD frequency too low
- Device not selected
- Open head
- Device in read mode
- No write current

READ MODE

The read mode configures the SSI 32R2041RW as a low noise differential amplifier and deactivates the write current generator and write unsafe detection circuitry. The RDX and RDY outputs are emitter followers and are in phase with the "X" and "Y" head ports. These outputs should be AC coupled to the load. The RDX, RDY common mode voltage is maintained at the write mode value, minimizing the transient between write mode and read mode, substantially reducing the write to read recovery time in the subsequent Pulse Detection circuitry.

IDLE MODE

The idle mode deactivates the internal write current generator, the write unsafe detector and switches the RDX, RDY outputs into a high impedance state. This facilitates multiple device applications by enabling the read outputs to be wire-OR'ed and the write current programming resistor to be common to all devices.

TABLE 1: Mode Select

$\overline{CS}$	R/$\overline{W}$	MODE
0	0	Write
0	1	Read
1	0	Idle
1	1	Idle

TABLE 2: Head Select*

HS2	HS1	HS0	HEAD
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5

0 = Low level 1 = High level

*Unused heads should be left open.

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
HS0 - HS2	I	Head Select
$\overline{CS}$	I	Chip Select: a low level enables the device
R/$\overline{W}$	I	Read/Write: a high level selects Read mode
WUS	O*	Write Unsafe: Open collector output, a high level indicates an unsafe writing condition
WD, $\overline{WD}$	I	Differential Write Data inputs: a positive transition on WD toggles the direction of the head current
H0X - H5X H0Y - H5Y	I/O	X, Y Head Connections: Current in the X-direction flows into the X-port
RDX, RDY	O*	X, Y Read Data: differential read data output
WC	*	Write Current: used to set the magnitude of the write current
VCC	-	+5V Logic Circuit Supply
VDD	-	+12V
GND	-	Ground

*When more than one R/W device is used, these signals can be wire OR'ed.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation outside these rating limits may permanently damage the device.

PARAMETER		SYMBOL	RATING
DC Supply Voltage		VDD	-0.3 to +13.5 VDC
		VCC	-0.3 to +6 VDC
Write Current		Iw	100 mA
Digital Input Voltage		Vin	-0.3 to VCC +0.3 VDC
Head Port Voltage		VH	-0.3 to +8 VDC
Differential Port Voltage	|HnX - HnY|	ΔVH	6 VDC
WUS Pin Voltage Range		Vwus	-0.3 to VCC VDC
Output Current	RDX, RDY	Io	-10 mA
	WUS	Iwus	+12 mA
Storage Temperature		Tstg	-65 to +150°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATING
DC Supply Voltage	VDD	12 ± 10% VDC
	VCC	5 ± 10% VDC
Operating Temperature	Tj	+25 to +135°C

DC CHARACTERISTICS

Unless otherwise specified, recommended operating conditions apply.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
VDD Supply Current	Read Mode	-	36	44	mA
	Write Mode	-	25 + Iw	29 + Iw	mA
	Idle Mode	-	3.5	4	mA
VCC Supply Current	Read Mode	-	22	29	mA
	Write Mode	-	14	18	mA
	Idle Mode	-	9	11.5	mA
Power Dissipation (Tj = +135°C)	Read Mode	-	540	740	mW
	Write Mode	-	370+10.35•Iw	490 +11.6•Iw	mW
	Idle Mode	-	87	115	mW
WD, $\overline{WD}$ Input Low Current (IIL1)	VIL1 = VCC -1.625V			80	µA
WD, $\overline{WD}$ Input High Current (IIH1)	VIH1 = VCC -0.72V			100	µA
WD, $\overline{WD}$ Input Low Voltage (VIL1)		VCC -1.870		VCC -1.625	VDC
WD, $\overline{WD}$ Input High Voltage (VIH1)		VCC -1.00		VCC -0.720	VDC
R/$\overline{W}$, $\overline{CS}$, HS0-HS2 Input Low Current (IIL2)	VIL2 = 0.8V	-0.4			mA
R/$\overline{W}$, $\overline{CS}$, HS0-HS2 Input High Current (IIH2)	VIH2 = 2.0V			100	µA
R/$\overline{W}$, $\overline{CS}$, HS0-HS2 Input Low Voltage (VIL2)				0.8	VDC
R/$\overline{W}$, $\overline{CS}$, HS0-HS2 Input High Voltage (VIH2)		2.0			VDC
WUS Output Low Voltage (VOL)	Iol = 4 mA	-	-	0.5	VDC
VDD Fault Voltage		9.0	-	10.3	VDC
VCC Fault Voltage		3.5	-	4.2	VDC

DC CHARACTERISTICS (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Head Current (HnX, HnY)	Write Mode, 0 ≤ VCC ≤ 3.5V 0 ≤ VDD ≤ 9.0V	-200	-	+200	µA
	Read/Idle Mode, 0 ≤ VCC ≤ 5.5V 0 ≤ VDD ≤13.2V	-200	-	+200	µA

WRITE CHARACTERISTICS

Unless otherwise specified, recommended operating conditions apply, Iw = 20 mA, Lh = 500 nH, Rh = 30Ω and f(WD) = 5 MHz.

WC Pin Voltage (Vwc)		1.57	1.65	1.73	V
Differential Head Voltage Swing		7	-	-	Vpp
Unselected Head Current		-	-	1	mA(pk)
Differential Output Capacitance		-	-	25	pF
Differential Output Resistance		500	700	950	Ω
WDI Transition Frequency	WUS = low	1.7	-	-	MHz
	WUS = high	-	-	500	kHz
Write Current Range		10	-	40	mA

READ CHARACTERISTICS

Unless otherwise specified, recommended operating conditions apply CL (RDX, RDY) < 20pF and RL (RDX,RDY) = 1 kΩ.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
Differential Voltage Gain		Vin=1mVpp @ 300 kHz	210	250	290	V/V
Bandwidth	-1dB	|Zs|<5Ω, Vin=1 mVpp	35	45	-	MHz
	-3dB	|Zs|<5Ω, Vin=1 mVpp	50	65	-	MHz
Input Noise Voltage		BW = 15 MHz, Lh = 0, Rh = 0	-	0.57	0.80	nV/√Hz
Differential Input Capacitance		Vin = 1 mVpp, f = 5 MHz	-	15	22	pF
Differential Input Resistance		Vin = 1 mVpp, f = 5 MHz	300	565	-	Ω
Dynamic Range		Peak-to-peak AC input voltage where gain falls to 90% of its small signal value, f = 5 MHz	2.0	-	-	mVpp
Common Mode Rejection Ratio		Vcm = 100 mVpp AC Coupled @ 5 MHz	54	-	-	dB
Power Supply Rejection Ratio		100 mVpp @ 5 MHz on VDD 100 mVpp @ 5 MHz on VCC	54	-	-	dB
Channel Separation		Unselected channels driven with 100 mVpp @ 5 MHz, Vin = 0 mVpp	45	-	-	dB

READ CHARACTERISTICS (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Output Offset Voltage		-400	-	+400	mV
RDX, RDY Common Mode Output Voltage	Read Mode	2.3	2.9	3.5	VDC
Single Ended Output Resistance	f = 5 MHz	-	-	50	Ω
Output Current	AC Coupled Load, RDX to RDY	3.2	-	-	mA

SWITCHING CHARACTERISTICS (See Figure 1)
Unless otherwise specified, recommended operating conditions apply, Iw = 20 mA, Lh = 500 nH, Rh = 30Ω and f(WD) = 5 MHz.

R/$\overline{W}$					
R/$\overline{W}$ to Write Mode	Delay to 90% of write current	-	0.2	0.6	µs
R/$\overline{W}$ to Read Mode	Delay to 90% of 100 mV 10 MHz Read signal envelope or to 90% decay of write current	-	0.3	0.6	µs
$\overline{CS}$					
$\overline{CS}$ to Select	Delay to 90% of write current or to 90% of 100 mV 10 MHz Read signal envelope	-	0.3	0.6	µs
$\overline{CS}$ to Unselect	Delay to 10% of write current	-	0.2	0.6	µs
HSn					
HS0, 1, 2 to any Head	Delay to 90% of 100 mV 10 MHz Read signal envelope	-	0.1	0.4	µs
WUS					
Safe to Unsafe - TD1		-	0.6	2.0	µs
Unsafe to Safe - TD2		-	-	1	µs
Head Current					
Prop. Delay - TD3	From 50% points, Lh=0 µH, Rh=0Ω	-	-	32	ns
Asymmetry	WD has 50% duty cycle and 1ns rise/fall time, Lh=0 µh, Rh=0Ω	-	-	0.5	ns
Rise/Fall Time	10% - 90% points, Lh=0 µH, Rh=0Ω	-	-	5	ns
Rise/Fall Time	10% - 90% points, Lh=1 µH, Rh=35Ω	-	9	-	ns

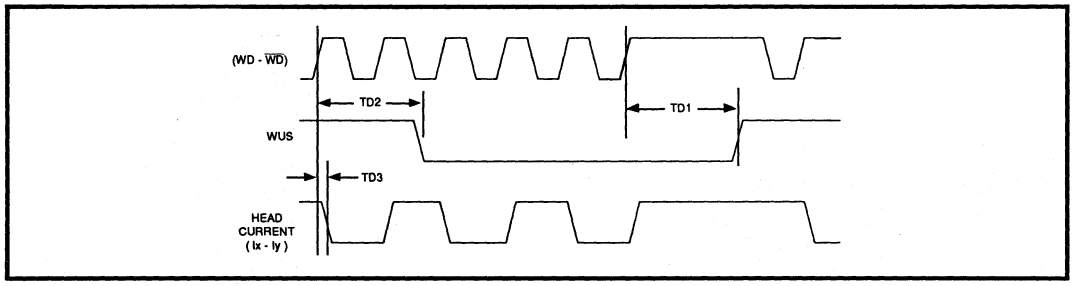


FIGURE 1: Write Mode Timing Diagram

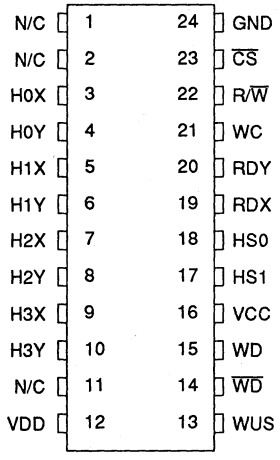
PACKAGE PIN DESIGNATIONS

(Top View)

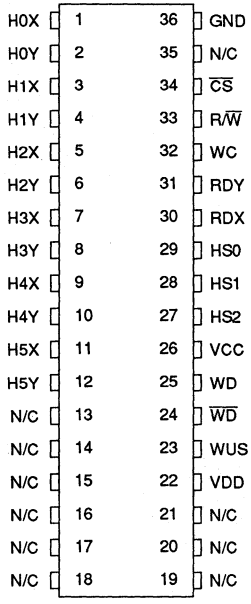
THERMAL CHARACTERISTICS*: θja

24-Lead VSOP	110°C/W
24-Lead SOL	80°C/W
36-Lead SOM	70°C/W

*Care should be taken not to exceed the maximum junction temperature. For example, on the 24-Lead VSOP, at a write current of 25 mA, the maximum ambient temperature should not exceed 50°C.



24-Lead SOL, VSOP



36-Lead SOM 6-Channel

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914

Notes:

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SSI 32R2063R/64R/65R
5V, 4-Channel Thin Film Read/Write Device
Advance Information

October 1993

3

DESCRIPTION

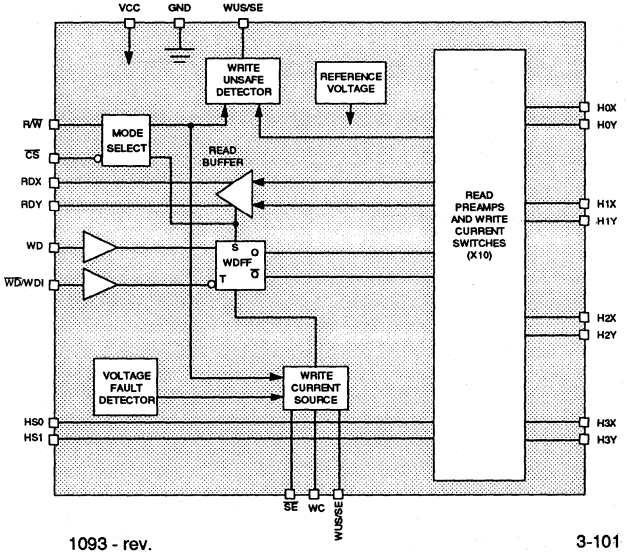
The SSI 32R2063R/64R/65R are Bipolar monolithic integrated circuits designed for use with two-terminal recording heads. They provide a low noise read amplifier, write current control, and data protection circuitry for up to four channels. The SSI 32R2063R option provides internal 350Ω damping resistors. Damping resistors are switched in during Write mode and switched out during Read mode. The SSI 32R2063/64/65 option does not provide a damping resistor. Power supply fault protection is provided by disabling the write current generator during power sequencing. System write to read recovery time is significantly improved by making the read channel outputs high impedance. The device also offers multiple channel "servo bank write" capability to assist in servo writing operations. Servo write is selected either with a TTL input (32R2063R/32R2064R) or with the WUS/SE pin (32R2065R).

The SSI 32R2063R/64R/65R require only a +5.0V power supply and are available in a variety of packages and gain options.

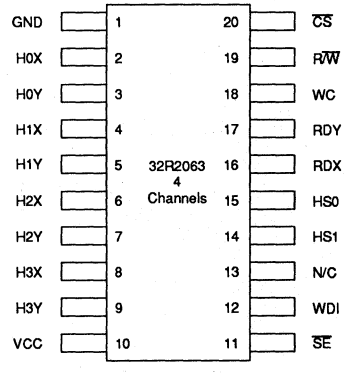
FEATURES

- +5V ±10% supply
- Low power
  - PD = 120 mW Read mode (Nom)
  - PD = 7 mW Idle (Max)
- High Performance:
  - Read mode gain = (U) 150, (W) 250 V/V
  - Input noise = 0.56 nV/√Hz (Nom)
  - Input capacitance = 16 pF (Nom)
  - Write current range = 1-35 mA
  - Max write current rise/fall time = 15 nsec (typical head)
  - Head voltage swing = 3.4 Vpp min
- Servo bank-write capability
- Self switching damping resistance
- Write unsafe detection
- Power supply fault protection
- Head short to ground protection
- Differential ECL-like (32R2063R) or TTL (32R2064R, 32R2065R) write data inputs

BLOCK DIAGRAM



PIN DIAGRAM



20-Lead SOL, VSOP

CAUTION: Use handling procedures necessary for a static sensitive component.

CIRCUIT OPERATION

The SSI 32R2063R/64R/65R has the ability to address up to 4 two-terminal heads and provide write drive or read amplification. Mode control and head selection are described in Tables 1 and 2. The TTL inputs R/$\overline{W}$, $\overline{CS}$ and $\overline{SE}$ have internal pull-up resistors to prevent an accidental write condition. HS0 and HS1 have internal pulldown(W)/Internal pull up (U) resistors. Internal clamp circuitry will protect the IC from a head short to ground condition in any mode.

TABLE 1a: Mode Select (32R2063R, 32R2064R)

$\overline{CS}$	R/$\overline{W}$	$\overline{SE}$	Mode
0	0	1	Single Channel Write. See Table 2.
0	0	0	Servo Write Channels 0, 1, 2, 3
0	1	X	Single Channel Read. See Table 2.
1	X	X	Idle.

TABLE 1b: Mode Select (32R2065R)

$\overline{CS}$	R/$\overline{W}$	WUS/SE	Mode
0	0	*	Single Channel Write. See Table 2.
0	0	Vcc+1.5*	Servo Write Channels 0, 1, 2, 3
0	1	X	Single Channel Read. See Table 2.
1	X	X	Idle.

*WUS/SE functions as WUS in Write Mode unless it is pulled above Vcc.

TABLE 2: Head Select

HS1	HS0	Head
0	0	0
0	1	1
1	0	2
1	1	3

WRITE MODE

Taking both $\overline{CS}$ and R/$\overline{W}$ low selects Write mode which configures the SSI 32R2063R/64R/65R as a current switch and activates the Write Unsafe (WUS) detector circuitry. On the 32R2063R, head current is toggled between the X and Y side of the selected head on each low to high transition of WD-$\overline{WD}$. On the 32R2064R/65R, head current is toggled between the X and Y side of the selected head on each high to low transition of the Write Data Input (WDI). Note that a preceding Read to Write transition or Idle to Write transition initializes the Write Data Flip-Flop to pass write current into the "X" side of the device. In this case, the Y side is higher potential than the X side. The magnitude of the write current (0-pk) is given by:

$$Iw = Aw \cdot \frac{Vwc}{Rwc} = K/Rwc$$

where Aw is the write current gain.

RWC is connected from pin WC to GND. Note the actual head current Ix, y is given by:

$$Ix, y = \frac{Iw}{1 + Rh/Rd}$$

Where:

Rh = Head resistance plus external wire resistance

Rd = Damping resistance

In Write mode a 350Ω damping resistor is switched in across the Hx, Hy ports (32R2063R/64R/65R). The unselected head potential is kept at ground.

SERVO WRITE MODE

Taking $\overline{SE}$ low and R/$\overline{W}$ low (32R2063R/64R) or taking WUS/SE to Vcc+1.5 (32R2065R) activates Servo Write mode. This mode allows for writing to multiple channels at once, which is useful during servo formatting. In this mode, the write driver will drive channels 0, 1, 2, and 3 simultaneously.

POWER SUPPLY FAULT PROTECTION

A voltage fault detection circuit improves data security by disabling the write current generator during a voltage fault or power startup regardless of mode. Note that WUS does not necessarily turn on to flag a power supply fault condition.

HEAD SHORT TO GROUND PROTECTION

The SSI 32R2063R/64R/65R provides a head short to ground protection circuit in any mode. In Idle or Read Mode, current out of the head port will not exceed 20 mA if any head is shorted to ground. In Write mode, if any head is shorted to ground (regardless if it is selected or not) the write current generator will turn off, the WUS flag will go high, and current will be limited to less than 1 mA out of the head port.

WRITE UNSAFE

Any of the following conditions will be indicated as a high level on the Write Unsafe, WUS, open collector output.

- WDI frequency too low
- Device in Read mode
- Device not selected
- Device in Servo Write mode
- No head current
- Open head
- Head short to ground

WDI frequency too low is detected if the WDI frequency falls below 1.67 MHz (typ). Consult the WUS Safe to Unsafe timing for range of frequency detection.

Device in Read mode, Device in servo Write mode and **Chip disabled** will flag WUS if R/$\overline{W}$ is high, if SE is high, or $\overline{CS}$ is high.

No head current will flag WUS if Rwc = ∞ and the selected head is present.

Head opened will flag WUS if Rh = ∞

Head short to ground is described in the preceding paragraph.

Upon entering Write mode, WUS is valid after two low to high transitions of WD-$\overline{WD}$ (32R2063R), or two high to low transitions of WDI (32R2064R/65R) following the required Read-Write transition time (0.6 µs max).

After the fault condition is removed, two positive transitions of WD-$\overline{WD}$ (32R2063R), or two negative transitions of WDI (32R2064R/65R) are required to clear WUS.

READ MODE

The Read mode configures the devices as a low noise differential amplifier and deactivates the write current generator. The damping resistor is switched out of the circuit allowing a high impedance input to the read amplifier. The RDX and RDY output are driven by emitter followers. They should be AC coupled to the load. The HnX, HnY inputs are non-inverting to the RDX, RDY outputs.

Note that in Idle or Write mode, the read amplifier is deactivated and RDX, RDY outputs become high impedance. This facilitates multiple R/W applications (wired-OR RDX, RDY) and minimizes voltage change when switching from Write to Read mode. Note also that the write current source is deactivated for both the Read and Idle mode. The unselected head potential is kept at ground.

IDLE MODE

Taking $\overline{CS}$ high selects the Idle mode which switches the RDX and RDY outputs into a high impedance state and deactivates the device. Power consumption in this mode is held to a minimum. The head potential is kept at ground.

PIN DESCRIPTION

CONTROL/STATUS

NAME	TYPE	DESCRIPTION
$\overline{CS}$	I	Chip Select Input. A logical low level enables the device.
R/$\overline{W}$†	I	Read/Write. A logical high level enables Read mode. A logical low level enables Write mode.
$\overline{SE}$	I	Servo Enable. A low level enables servo bank Write mode. See Servo Enable section (32R2063R, 32R2064R).
HS0,HS1	I	Head Select. Decoded address selects one of 4 channels. See Table 2.
WUS†	O	Write Unsafe. A high level indicates an unsafe writing condition. See WUS section (32R2064R).
WUS/SE†	I/O	Write Unsafe/Servo Enable. When in Servo Bank Write mode, pulling this pin above Vcc enables servo bank write. See Servo Enable section. Otherwise, a high level indicates an unsafe writing condition. See WUS section (32R2065R).
WC	I	Write Current. Sets the write current through the recording head.

HEAD TERMINAL CONNECTIONS

H0X-H3X H0Y-H3Y	I	X,Y Head Connections

DATA INPUT/OUTPUT

WDI†	I	Write Data In. A negative transition of WDI changes the direction of current in the recording head (32R2064R, 32R2065R).
WD,$\overline{WD}$†	I	Differential Write Data In. A positive transition of WD-$\overline{WD}$ changes the direction of current in the recording head (32R2063R).
RDX,RDY†	O	Differential Read Data Out. Emitter follower output.

POWER

VCC	I	+5 V power supply
GND	I	Ground

† When more than one Read/Write device is used, signals can be wire OR'ed.

ELECTRICAL SPECIFICATIONS

Current maximums are currents with the highest absolute value.

ABSOLUTE MAXIMUM RATINGS

Operation beyond the maximum ratings may damage the device.

PARAMETER			RATING
DC Supply Voltage		VCC	-0.3 to 7V
Write Current*		Iw	60 mA
Digital Input Voltage		Vin	-0.3 to VCC+0.3V
Head Port Voltage		VH	-0.3 to VCC+0.3V
WUS Pin Voltage		Vwus	VCC+0.3V
Output Current	RDX,RDY	Io	-6 mA
	WUS	Iwus	+8 mA
Junction Operating Temperature			+135°C
Storage Temperature			-65 to +150°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER		CONDITIONS
DC Supply Voltage	VCC	5 ± 10%V
Ambient Operating Temperature		0° < Ta < 75°C

TEST CONDITIONS

Recommended operating conditions apply.

PARAMETER	CONDITIONS
Write Current, Iw	1-35 mA
Head Inductance, Lh	1 µH
Head Resistance, Rh	30Ω
WD Frequency	5 MHz
WD,$\overline{WD}$ rise/fall time (32R2063R)	1ns
WDI rise/fall time (32R2064R/2065R)	1 ns

*Maximum servo write current or ambient temperature needs to be regulated to prevent the junction temperature from exceeding 135°C.

POWER DISSIPATION

Recommended operating conditions apply.

PARAMETER	CONDITIONS		MIN	NOM	MAX	UNIT
VCC Supply Current	Read Mode	(U)		24	32	mA
		(W)		28	38.2	mA
	Write Mode	Single Channel		(28+Iw)	(39+Iw)	mA
		Servo Write		(61+ 4Iw)	(83+ 4Iw)	mA
	Idle Mode			0.7	1.1	mA
Power Dissipation	Read Mode			140	209	mW
	Write Mode	Single Channel		(140+ 5.3 Iw)	(210+ 6 Iw)	mW
		Servo Write		(305+ 20 Iw)	(450+ 22.5 Iw)	mW
	Idle Mode			4	7	mW

DIGITAL INPUTS

Input High Voltage Vih HSX, CS/, R/$\overline{W}$, $\overline{SE}$, WDI		2.0			VDC
Input Low Voltage Vil HSX, CS/, R/$\overline{W}$, $\overline{SE}$, WDI				0.8	VDC
Input High Current Iih HSX, CS/, R/$\overline{W}$, $\overline{SE}$, WDI	Vih = 2.0V			100	µA
Input Low Current Iil HSX, CS/, R/$\overline{W}$, $\overline{SE}$, WDI	Vil = 0.8V	-0.4			mA
WD, WD/ Input High Voltage Vih		Vcc-1.0		Vcc-0.5	VDC
WD, WD/ Input Low Voltage Vil		Vih-2.5		Vih-1.0	VDC
WD-WD/ Input Voltage Difference	0.5	0.5	1.0	1.5	V
WD,WD/ Input High Current	Vih = Vcc-0.75V		85	120	µA
WD,WD/ Input Low Current	Vih = Vcc-1.75V		65	100	µA
WUS Output Low Voltage Vol	Iol = 2 mA max		0.35	0.5	VDC

ELECTRICAL SPECIFICATIONS (continued)

WRITE CHARACTERISTICS

Test conditions apply unless otherwise specified.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Write Current Voltage Vwc		2.4	2.5	2.6	V
Write Current Gain Aw	Iw = Aw•Vwc/Rwc		20		V
Write Current Constant "K"	Iw = K/Rwc	48.5	50	51.5	V
Differential Head Voltage Swing	Iw = 20 mA	4.2	3.6		Vpp
	Open Head, Iw = 20 mA	3.4	5.0		Vpp
Head Differential Rd	32R2063R/64R/65R	310	350	390	Ω
Load Resistance	32R2063	2400	3000	3600	Ω
WD Pulse Width	PWH	5			ns
(Write mode)	PWL	10			ns
WD Pulse Width	PWH	5			ns
(Servo Write)	PWL	20			ns
WD, $\overline{WD}$ Pulse Width	PWH	5			ns
(Write, Servo Write) 32R2063R	PWL	5			ns
Head Current HnX,HnY		-200		200	µA
Unselected Head Voltage				0.3	VDC
Unselected Head Current	DC			100	µA
VCC Fault Voltage	Iw ≤ 0.2 mA	3.5	4.0	4.2	V

SERVO WRITE CHARACTERISTICS

Write Current Range		5		25	mA
Write Current Matching	Between channels		±10%		
WUS/SE Input Voltage	Servo bank write enabled (32R2065R)	Vcc + 1.5			V

READ CHARACTERISTICS

Test conditions apply unless otherwise specified. CL (RDX, RDY) < 20 pF, RL (RDX, RDY) = 1 kΩ.

PARAMETER		CONDITIONS		MIN	NOM	MAX	UNIT
Differential Voltage Gain		Vin = 1 mVpp	(U)	110	150	190	V/V
		@1 MHz	(W)	200	250	300	V/V
Voltage BW	-1dB	|Zs| < 5Ω, Vin = 1 mVpp		20	35		MHz
	-3dB			45	70		MHz
Input Noise Voltage		BW = 15 MHz, Lh = 0, Rh = 0			0.56	0.75	nV/√Hz
Input Noise Current					3		pA/√Hz
Differential Input Capacitance		Vin = 1 mVpp, f = 5 MHz			16	22	pF
Differential Input Resistance		Vin = 1 mVpp, f = 5 MHz 32R2063/64/65		720	1200		Ω
Dynamic Range		AC input voltage where gain falls to 90% of its small signal gain value, f = 5 MHz		2	5		mVpp
Common Mode Rejection Ratio		Vin = 0 VDC + 100 mVpp @ 5 MHz		55			dB
Power Supply Rejection Ratio		100 mVpp @ 5 MHz on VCC		50			dB
Channel Separation		Unselected channels driven with Vin = 0 VDC + 100 mVpp		50			dB
Output Offset Voltage		Shorted head	(U) 150 Av	-200		+200	mV
			(W) 250 Av	-300		+300	mV
Single Ended Output Resistance		f = 5 MHz			25	50	Ω
Output Current		AC coupled load, RDX to RDY		0.9	1.4		mA
RDX, RDY Common Mode Output Voltage				0.4 • Vcc	0.5 • Vcc	0.6 • Vcc	VDC

ELECTRICAL SPECIFICATIONS (continued)

SWITCHING CHARACTERISTICS

Test conditions apply unless otherwise specified.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
R/$\overline{W}$	Read to Write	R/$\overline{W}$ to 90% of write current U		0.1	0.3	µs
		W		0.2	0.6	µs
	Read to Write	Rh = 10Ω, Lh = 1.5 µH Iw = 10 mA		0.07	0.15	µs
	Write to Read	R/$\overline{W}$ to 90% of 100 mV Read signal envelope		0.1	0.6	µs
$\overline{CS}$	Unselect to Select	CS to 90% of 100 mV 10 MHz Read signal envelope		0.4	1	µs
	Select to Unselect	CS to 10% of write current		0.4	1	µs
HS0,1 to any Head		To 90% of 100 mV 10 MHz Read signal envelope		0.2	0.6	µs
WUS	Safe to Unsafe (TD1)	Write mode, loss of WD transitions; Defines max WD period for WUS operation	0.6	2.0	3.6	µs
	Unsafe to Safe (TD2)	Fault cleared: from second WD transition		0.2	1.0	µs
WDI	Frequency Range	Valid WUS	1.67		25	MHz
Head Current		Lh = 0, Rh = 0				
	WDI to Ix - Iy (TD3)	from 50% points		3	10	ns
	Asymmetry	WDI has 1 ns rise/fall time			1.0	ns
	Rise/fall Time	10% to 90% points Iw = 15 mA, Rh = 0, Lh = 0		4	6	ns
		Iw = 15 mA, Rh = 30Ω, Lh = 1 µH			15	ns

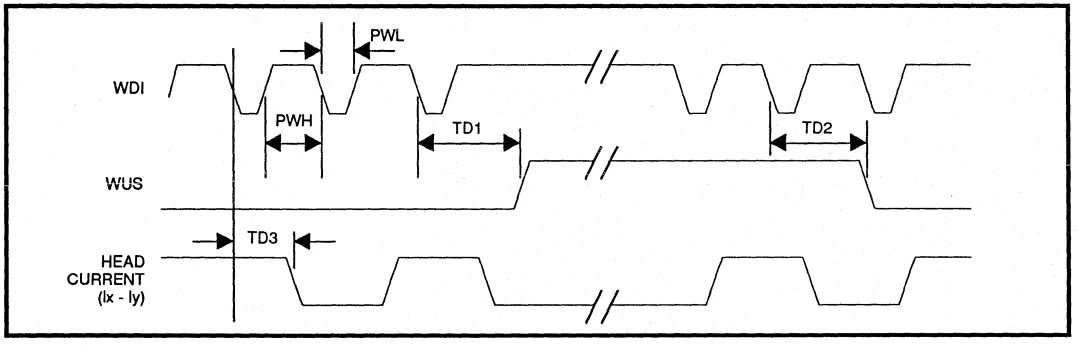


FIGURE 1a: Write Mode Timing Diagram 32R2064R, 32R2065R

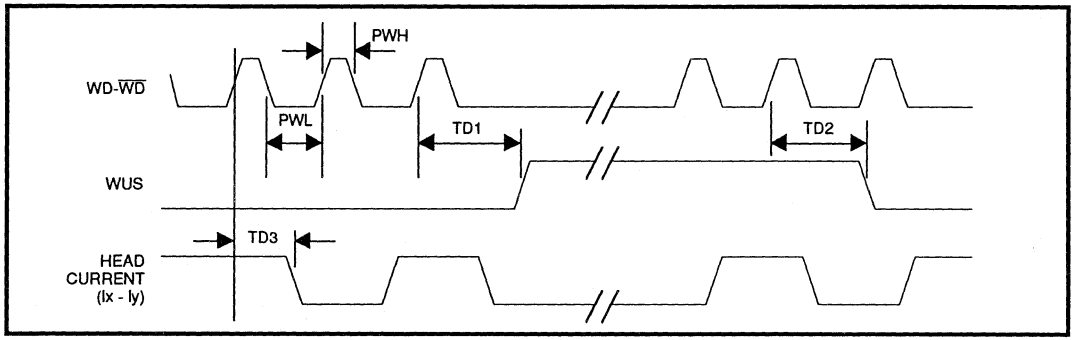
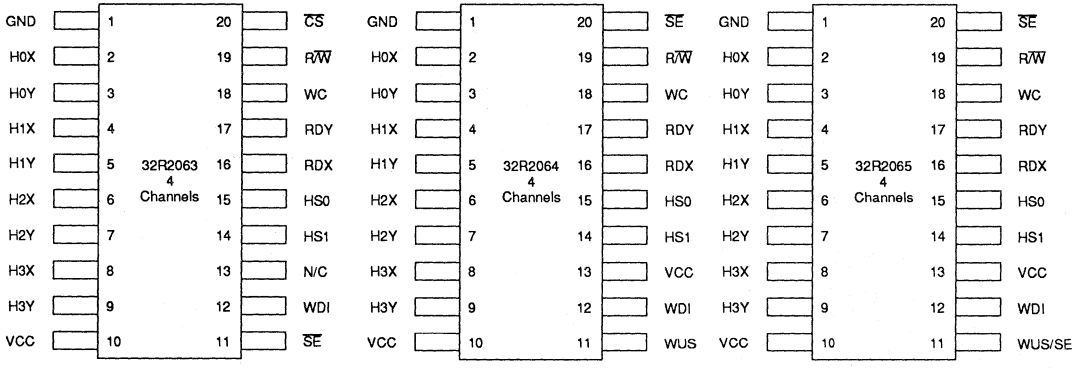


FIGURE 1b: Write Mode Timing Diagram 32R2063R

PACKAGE LEAD DESIGNATION

(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



20-Lead SOL, VSOP **20-Lead SOL, VSOP** **20-Lead SOL, VSOP**

Advanced Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Don not use for final design.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914

Notes:

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SSI 32R2110R/2111R
10-Channel Two Terminal Thin-Film Read/Write Device
Advance Information

January 1994

3

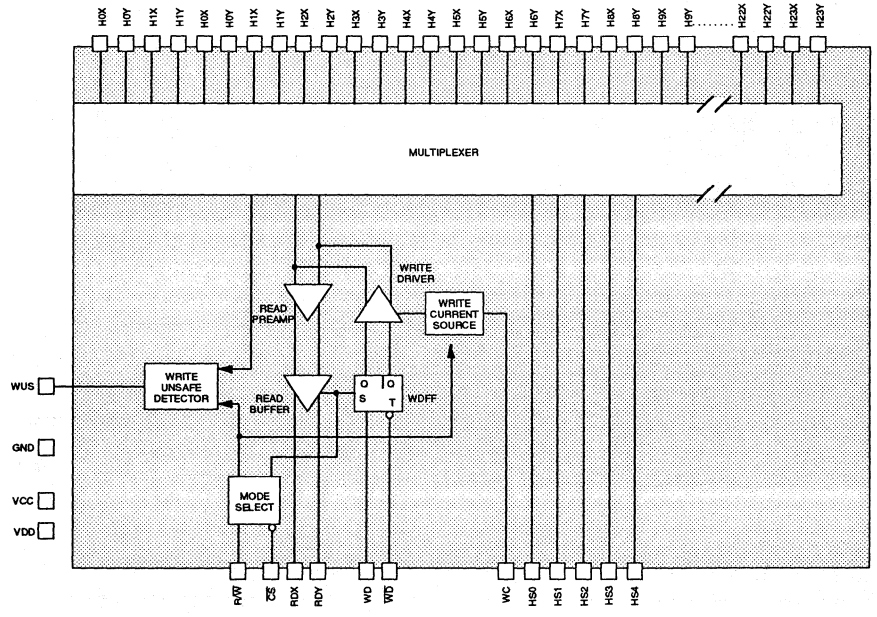
DESCRIPTION

The SSI 32R2110R/2111R is a BiCMOS monolithic integrated circuit designed for use with two-terminal recording heads. It is intended for use in hard disk drive designs which require data rates exceeding 48 Mbit/s. It provides a low noise read amplifier, write current control, and data protection circuitry for 24 channels. The SSI 32R2110R/2111R provides internal 320Ω damping resistors that are switched in during Write mode and switched out during Read mode. Power supply fault protection is provided by disabling the write current during power sequencing. System write-to-read recovery time is significantly improved by controlling the read channel common mode output voltage shift in the Write mode. The device provides the user with a controllable write-current adjustment feature with a current gain of 25x. The device also provides a multiple channel "servo bank write" capability which is useful during servo writing. The 32R2110R has a differential PECL write-data input, whereas the 32R2111R uses a single-ended TTL pin.

FEATURES

- **+5V, +12V ±10% supply**
- **Low power**
  - **PD = 235 mW read mode (Nom)**
  - **PD = 12 mW idle (Max)**
- **High Performance:**
  - **Read mode gain = 250 V/V**
  - **Input noise = 0.45 nV/√Hz (Nom)**
  - **Input capacitance = 12 pF (Nom)**
  - **Write current range = 10-40 mA**
  - **Max write current rise/fall time = 7 nsec (typ. head)**
  - **Head voltage swing = 10Vpp (min), 12V typ.**
- **Servo bank-write capability**
- **Unselected heads are at GND potential**
- **Self-switching damping resistance**

BLOCK DIAGRAM



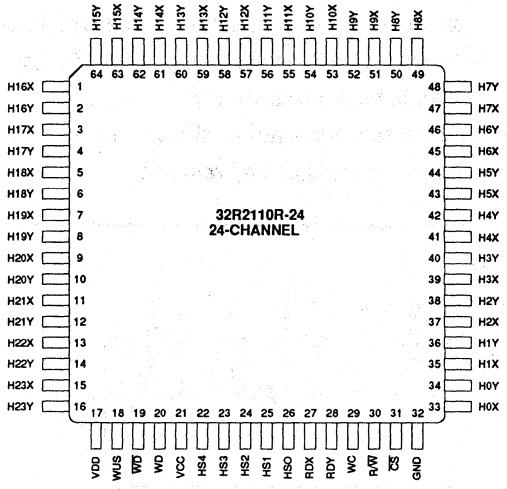
SSI 32R2110R/2111R
10-Channel Two Terminal Thin-Film Read/Write Device

FEATURES (continued)

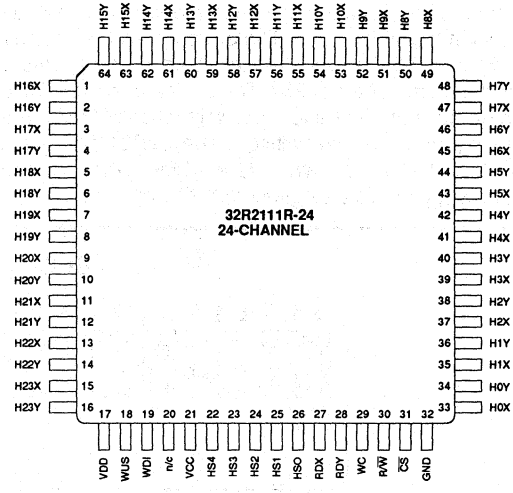
- **Designed for two-terminal thin-film or MIG heads with inductance up to 1.0 µH**
- **Write unsafe detection**
- **Power supply fault protection**
- **Head short to ground protection**
- **Differential ECL-like write data input**
- **64-Lead TQFP package**

PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



24-Channel
64-Lead TQFP (PECL input)



24-Channel
64-Lead TQFP (TTL input)

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

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SSI 32R2200R/2201R
+5V, 4-, 6-Channel Thin Film Read/Write Device
Target Specification

October 1993

3

DESCRIPTION

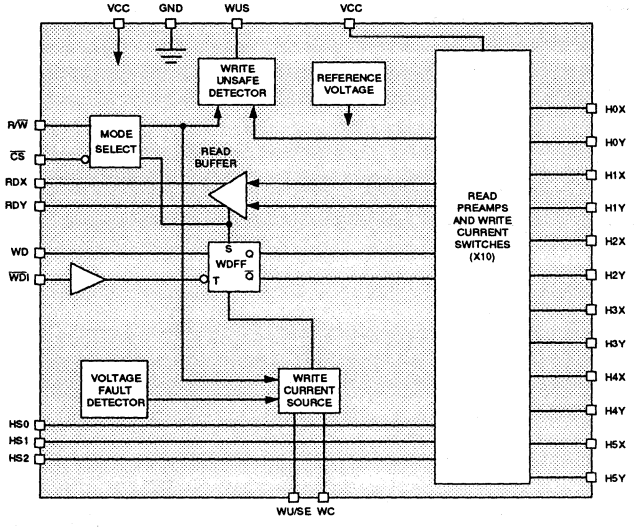
The SSI 32R2200R/2201R are BiCMOS monolithic integrated circuits designed for use with two-terminal recording heads. They provide a low noise read amplifier, write current control, and data protection circuitry for up to six channels. The SSI 2200R/2201R option provides internal 350Ω damping resistors. Damping resistors are switched in during Write mode and switched out during Read mode. The SSI 32R2200/2201 option does not provide damping resistors. Power supply fault protection is provided by disabling the write current generator during power sequencing. System write to read recovery time is significantly improved by making the read channel outputs high impedance. The device also offers multiple channel "servo bank write" capability to assist in servo writing operations.

The SSI 32R2200R/2201R require only a +5V power supply and are available in a variety of packages. The 32R2201R is hardware compatible with the SSI 32R4610AR and SSI 32R2020R Read/Write devices.

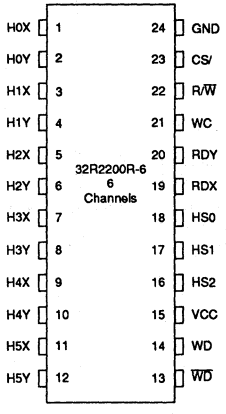
FEATURES

- **+5V ±10% supply**
- **Low power**
  - **PD = 150 mW Read mode (Nom)**
  - **PD = 1.0 mW Idle (Max)**
- **High Performance:**
  - **Read mode gain = 300 V/V**
  - **Input noise = 0.45 nV/√Hz (Nom)**
  - **Input capacitance = 12 pF (Nom)**
  - **Write current range = 3-35 mA**
  - **Max write current rise/fall time = 9 nsec (typical head)**
  - **Head voltage swing = 6 Vpp min**
- **Servo bank-write capability**
- **Self switching damping resistance**
- **Write unsafe detection** (continued)

BLOCK DIAGRAM



PIN DIAGRAM



20-Lead SOV, SOL

CAUTION: Use handling procedures necessary for a static sensitive component.

The target specification is intended as an initial disclosure of specification goals for the product. The specifications are based on design goals, subject to change and are not guaranteed. Silicon Systems assumes no obligation regarding future manufacture unless agreed to in writing.

FEATURES (continued)

- Power supply fault protection
- Head short to ground protection
- Differential ECL-like (32R2200R) or TTL (32R2201R) write data inputs

FUNCTIONAL DESCRIPTION

The SSI 32R2200R/2201R has the ability to address up to 6 two-terminal heads and provide write drive or read amplification. Mode control and head selection are described in Tables 1 and 2. The TTL inputs R/$\overline{W}$ and $\overline{CS}$ have internal pull-up resistors to prevent an accidental write condition. HS0, HS1 and HS2 have internal pulldown resistors. Internal clamp circuitry will protect the IC from a head short to ground condition in any mode.

TABLE 1: Mode Select

$\overline{CS}$	R/$\overline{W}$	WUS/SE	Mode
0	0	*	Single Channel Write. See Table 2.
0	0	Vcc + 1.9V	Servo Write.
0	1	X	Single Channel Read. See Table 2.
1	X	X	Idle.

*WUS/SE is a WUS output unless pulled above VCC, sourcing at least 4 mA of current.

TABLE 2: Head Select

HS2	HS1	HS0	Head
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5

WRITE MODE

Taking both $\overline{CS}$ and R/$\overline{W}$ low selects Write mode which configures the SSI 32R2200R/2201R as a current switch and activates the Write Unsafe (WUS) detector circuitry. On the 32R2200R, head current is toggled between the X and Y side of the selected head on each low to high transition of WD-$\overline{WD}$. On the 32R2201R, head current is toggled between the X and Y side of the selected head on each high to low transition of the Write Data Input (WDI). Note that a preceding Read to Write transition or Idle to Write transition initializes the Write Data Flip-Flop to pass write current into the "X" side of the device. In this case, the Y side is higher potential than the X side. The magnitude of the write current (0-pk) is given by:

$$Iw = Aw \cdot \frac{Vwc}{Rwc} = K/Rwc$$

where Aw is the write current gain.

RWC is connected from pin WC to GND. Note the actual head current Ix, y is given by:

$$Ix, y = \frac{Iw}{1 + Rh/Rd}$$

Where:

Rh = Head resistance plus external wire resistance

Rd = Damping resistance

In Write mode a 350Ω damping resistor is switched in across the Hx, Hy ports (32R2200R/2201R only).

SERVO WRITE MODE

Pulling WUS/SE above VCC and R/$\overline{W}$ low activates Servo Write mode. This mode allows for writing to multiple channels at once, which is useful during servo formatting. In this mode the write driver will drive all channels simultaneously.

Servo Write mode is initialized by pulling the WUS/SE pin 1.9V above Vcc while the R/$\overline{W}$ pin is high (Read mode) and is then activated by driving the R/$\overline{W}$ pin low.

POWER SUPPLY FAULT PROTECTION

A voltage fault detection circuit improves data security by disabling the write current generator during a voltage fault or power startup regardless of mode. Note that WUS does not necessarily turn on to flag a power supply fault condition.

HEAD SHORT TO GROUND PROTECTION

The SSI 32R2200R/2201R provides a head short to ground protection circuit in Write mode. If the selected head is shorted to ground the write current generator will turn off, the WUS flag will go high, and current will be limited to less than 1 mA out of the head port. Note that any unselected head is pulled to ground through internal circuitry. In the Idle mode, all heads are similarly pulled to ground.

In Read mode, current out of the selected head port will not exceed 20 mA if the head is shorted to ground.

WRITE UNSAFE

Any of the following conditions will be indicated as a high level on the Write Unsafe, WUS, open collector output.

- WDI frequency too low
- Device in Read mode
- Device not selected
- No head current
- Open head
- Head short to ground

WDI frequency too low is detected if the WDI frequency falls below 1 MHz. Consult the WUS Safe to Unsafe timing for range of frequency detection.

Device in Read mode, Device in servo Write mode and **Chip disabled** will flag WUS if R/$\overline{W}$ is high, if SE is high, or $\overline{CS}$ is high.

No head current will flag WUS if Rwc = ∞ and the selected head is present.

Head opened will flag WUS if Rh = ∞.

Head short to ground is described in the preceding paragraph.

FUNCTIONAL DESCRIPTION (continued)

Upon entering Write mode, WUS is valid after one low to high transition of WD-$\overline{WD}$ (32R2200R), or one high to low transition of WDI (32R2201R) following the required Read-Write transition time (0.6 µs max).

After the fault condition is removed, one positive transition of WD-$\overline{WD}$ (32R2200R), or one negative transition on WDI (32R2201R) are required to clear WUS.

READ MODE

The Read mode configures the SSI 32R2200R/2201R as a low noise differential amplifier and deactivates the write current generator. The damping resistor is switched out of the circuit allowing a high impedance input to the read amplifier. The RDX and RDY output are driven by emitter followers. They should be AC coupled to the load. The HnX, HnY inputs are non-inverting to the RDX, RDY outputs.

Note that in Idle or Write mode, the read amplifier is deactivated and RDX, RDY outputs become high impedance. This facilitates multiple R/W applications (wired-OR RDX, RDY) and minimizes voltage change when switching from Write to Read mode. Note also that the write current source is deactivated for both the Read and Idle mode.

IDLE MODE

Taking $\overline{CS}$ high selects the Idle mode which switches the RDX and RDY outputs into a high impedance state and deactivates the device. Power consumption in this mode is held to a minimum.

PIN DESCRIPTION

CONTROL/STATUS

NAME	TYPE	DESCRIPTION
$\overline{CS}$	I	Chip Select Input. A logical low level enables the device.
R/$\overline{W}$†	I	Read/Write. A logical high level enables Read mode. A logical low level enables Write mode.
HS0,HS1, HS2	I	Head Select. Decoded address selects one of 6 channels. See Table 2.
WUS/SE†	I/O	Write Unsafe/Servo Enable. When in Servo Bank Write mode, pulling this pin above Vcc enables servo bank write. See Servo Enable section. Otherwise, a high level indicates an unsafe writing condition. See WUS section.
WC†	I	Write Current. Sets the write current through the recording head.

HEAD TERMINAL CONNECTIONS

H0X-H5X H0Y-H5Y	I	X,Y Head Connections

DATA INPUT/OUTPUT

WDI† (32R2201R)	I	Write Data In. A negative transition of WDI changes the direction of current in the recording head.
WD,$\overline{WD}$† (32R2200R)	I	Differential Write Data In. A positive transition of WD-$\overline{WD}$ changes the direction of current in the recording head.
RDX,RDY†	O	Differential Read Data Out. Emitter follower output.

POWER

VCC	I	+5V power supply
GND	I	Ground

† When more than one Read/Write device is used, signals can be wire OR'ed.

ELECTRICAL SPECIFICATIONS

Current maximums are currents with the highest absolute value.

ABSOLUTE MAXIMUM RATINGS

Operation beyond the maximum ratings may damage the device.

PARAMETER			RATING
DC Supply Voltage		VCC	-0.3 to 6Vdc
Write Current		Iw	65 mA
Digital Input Voltage		Vin	-0.3 to VCC+0.3Vdc
Head Port Voltage		VH	-0.3 to VCC+0.3Vdc
WUS Pin Voltage		Vwus	VCC+0.3Vdc
Output Current	RDX,RDY	Io	-10 mA
	WUS	Iwus	+12 mA
Junction Operating Temperature			+125°C
Storage Temperature			-65 to +150°

RECOMMENDED OPERATING CONDITIONS

PARAMETER		CONDITIONS
DC Supply Voltage	VCC	5 ± 10%V
Ambient Operating Temperature		0° < Ta < 75°

TEST CONDITIONS

Recommended operating conditions apply.

PARAMETER		CONDITIONS
Write Current, Iw		20 mA
Head Inductance, Lh		1 µH
Head Resistance, Rh		30Ω
WD Frequency		5 MHz
WD,$\overline{WD}$ rise/fall time	32R2200R	1ns
WDI rise/fall time	32R2201R	1 ns

POWER DISSIPATION

Recommended operating conditions apply.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VCC Supply Current	Read Mode		21	31	mA
	Write Mode		20 + 1.2 Iw	TBD	mA
	Idle Mode		0.07	0.2	mA
Power Dissipation	Read Mode		107	170	mW
	Write Mode		100 + 6 Iw	TBD	mW
	Idle Mode		0.37	1.0	mW

DIGITAL INPUTS

Input High Voltage Vih HSX, CS/, R/$\overline{W}$, WDI		2.0			VDC
Input Low Voltage Vil HSX, CS/, R/$\overline{W}$, WDI				0.8	VDC
Input High Current Iih HSX, CS/, R/$\overline{W}$, WDI	Vih = 2.0V			100	µA
Input Low Current Iil HSX, CS/, R/$\overline{W}$, WDI	Vil = 0.8V	-0.4			mA
WD, $\overline{WD}$ Input High Voltage Vih	32R2200R	Vcc-1.50		Vcc-0.5	VDC
WD, $\overline{WD}$ Input Low Voltage Vil	32R2200R	Vih-1.50		Vih-0.5	VDC
WD-$\overline{WD}$ Input Voltage Difference	32R2200R	0.5		1.5	V
WD,$\overline{WD}$ Input High Current	Vih = Vcc-0.75V (32R2200R)		85	125	µA
WD,$\overline{WD}$ Input Low Current	Vih = Vcc-1.75V (32R2200R)		70	100	µA
WUS Output Low Voltage Vol	Iol = 2 mA max			0.5	VDC

ELECTRICAL SPECIFICATIONS (continued)

WRITE CHARACTERISTICS

Test conditions apply unless otherwise specified.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Write Current Voltage Vwc			2.0		V
Write Current Gain Aw	Iw = Aw•Vwc/Rwc		25		mA/mA
Write Current Constant "K"	Iw = K/Rwc	48	50	52	V
Differential Head Voltage Swing	Iw = 15 mA	6.5	8.0		Vpp
	Open Head, Iw = 15 mA	6.5	7.5		Vpp
Head Differential Rd	32R2200/2201	4			kΩ
Load Resistance	32R2200R/2201R		350		Ω
WD Pulse Width*	PWH	5			ns
	PWL	5			ns
Unselected Head Voltage				0.1	VDC
Unselected Head Current	DC			0.2	mA
VCC Fault Voltage	Iw ≤ 0.2 mA	3.9	4.1	4.3	V
Head Current HnX,HnY	VCC fault condition	-200		200	µA

SERVO WRITE CHARACTERISTICS

Write Current Range		5		25	mA
Write Current Matching	Between channels		±10%		
WUS/SE Voltage	Servo Bank Write Enabled	Vcc + 1.9			V

* See Figure 1.

The target specification is intended as an initial disclosure of specification goals for the product. The specifications are based on design goals, subject to change and are not guaranteed. Silicon Systems assumes no obligation regarding future manufacture unless agreed to in writing.

READ CHARACTERISTICS

Test conditions apply unless otherwise specified. CL (RDX, RDY) < 20 pF, RL (RDX, RDY) = 1 kΩ.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Differential Voltage Gain		Vin = 1 mVpp @1 MHz		320		V/V
Voltage BW	-1dB	|Zs| < 5Ω, Vin = 1 mVpp	35			MHz
	-3dB		65			MHz
Input Noise Voltage		BW = 15 MHz, Lh = 0, Rh = 0		0.45		nV/√Hz
Input Noise Current				3		pA/√Hz
Differential Input Capacitance		Vin = 1 mVpp, f = 5 MHz		12		pF
Differential Input Resistance		Vin = 1 mVpp, f = 5 MHz		1000		Ω
Dynamic Range		AC input voltage where gain falls to 90% of its small signal gain value, f = 5 MHz	2	5		mVpp
Common Mode Rejection Ratio		Vin = 0 VDC + 100 mVpp @ 5 MHz	50	60		dB
Power Supply Rejection Ratio		100 mVpp @ 5 MHz on VCC	50	70		dB
Channel Separation		Unselected channels driven with Vin = 0 VDC + 100 mVpp	50	60		dB
Output Offset Voltage		Lh = 0, Rh = 0	-250		+250	mV
Single Ended Output Resistance		f = 5 MHz		20	50	Ω
Output Current		AC coupled load, RDX to RDY	1.0	2.0		mA
RDX, RDY Common Mode Output Voltage				Vcc-2.6		VDC

ELECTRICAL SPECIFICATIONS (continued)

SWITCHING CHARACTERISTICS

Test conditions apply unless otherwise specified.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
R/$\overline{W}$	Read to Write	R/$\overline{W}$ to 90% of write current		0.1	0.6	µs
	Write to Read	R/$\overline{W}$ to 90% of 100 mV Read signal envelope		0.1	0.6	µs
$\overline{CS}$	Unselect to Select	CS to 90% of 100 mV 10 MHz Read signal envelope		0.6	2	µs
	Select to Unselect	CS to 10% of write current		0.1	1	µs
HS0,1 to any Head		To 90% of 100 mV 10 MHz Read signal envelope		0.2	1	µs
WUS	Safe to Unsafe (TD1)	Write mode, loss of WDI transitions; Defines max WDI period for WUS operation	0.6	2.0	3.6	µs
	Unsafe to Safe (TD2)	Fault cleared: from first negative WDI transition		0.2	1.0	µs
WDI	Frequency Range	Valid WUS	1.0		50	MHz
Head Current		Lh = 0, Rh = 0				
	WD to Ix - Iy (TD3)	from 50% points		2.5	4.0	ns
	Asymmetry	WDI has 1 ns rise/fall time			0.5	ns
	Rise/fall Time	10% to 90% points Iw = 15 mA, Rh = 0, Lh = 0		1	3	ns
		Iw = 15 mA, Rh = 30Ω, Lh = 1 µH		6	9	ns

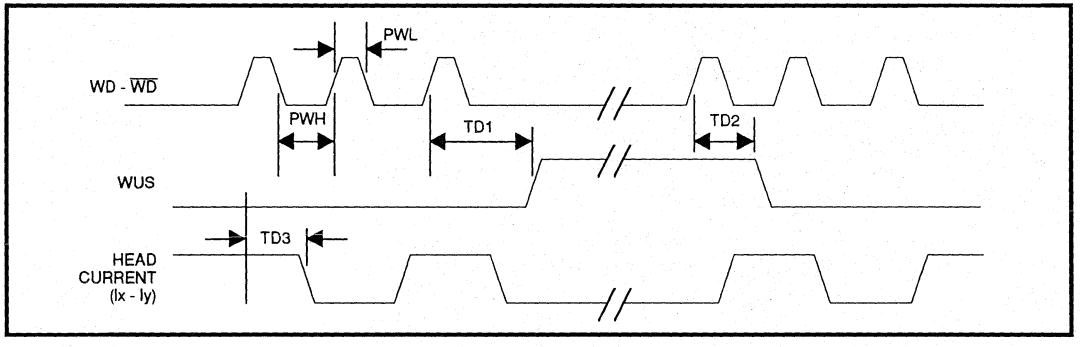


FIGURE 1: 32R2200R Write Mode Timing Diagram

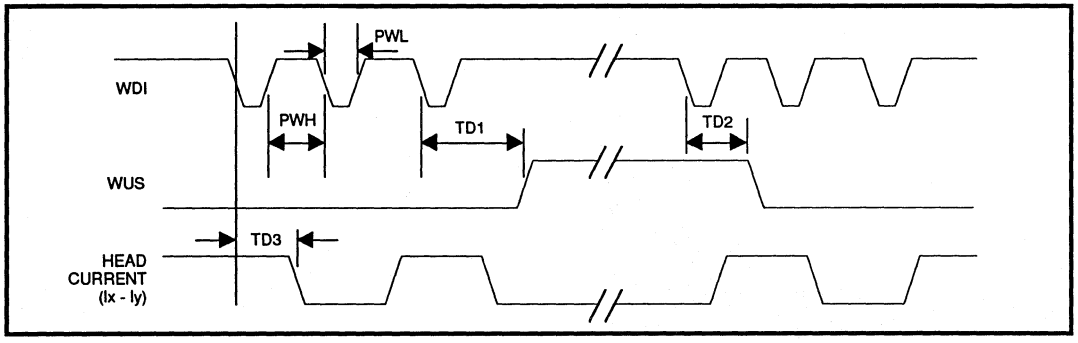
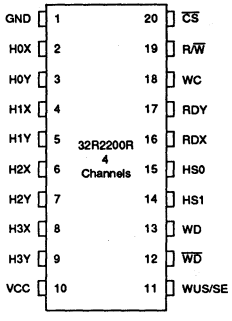


FIGURE 2: 32R2201R Write Mode Timing Diagram

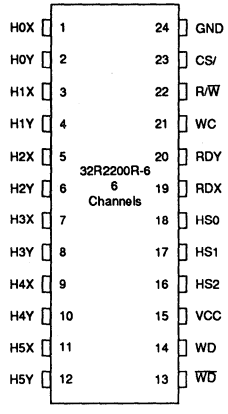
PACKAGE PIN DESIGNATIONS

(Top View)

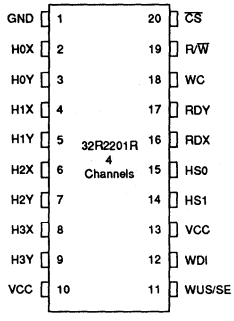
CAUTION: Use handling procedures necessary for a static sensitive component.



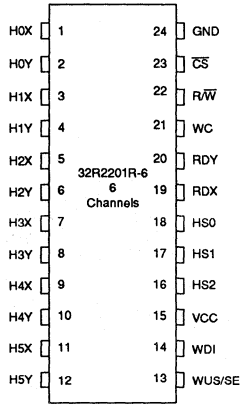
20-Lead SOV, SOL



24-Lead SOV, SOL



20-Lead SOV, SOL



24-Lead SOV, SOL

Target Specification: The target specification is intended as an initial disclosure of specification goals for the product. The specifications are based on design goals, subject to change and are not guaranteed.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914

Notes:

SSI 32R2300/2300R/2301/2301R
3.3V, 5V, 2, 4-Channel 2-Terminal Read/Write Device

December 1993

DESCRIPTION

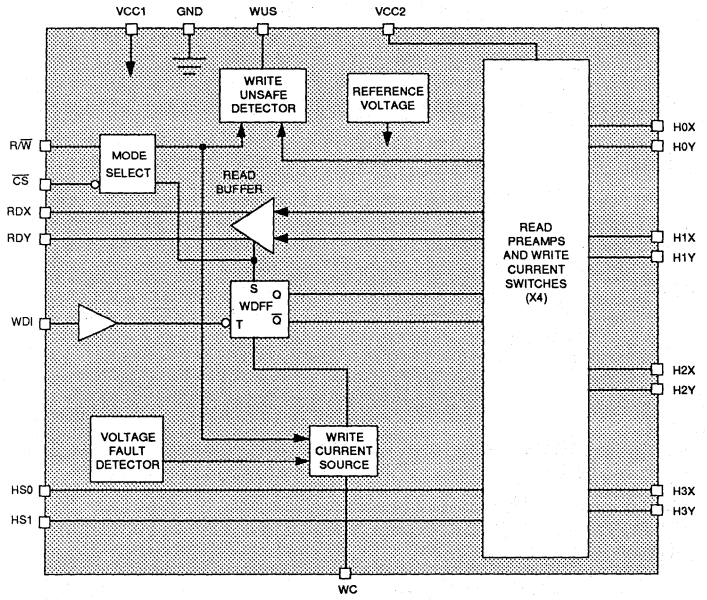
The SSI 32R2300/2300R are BiCMOS monolithic integrated circuits designed for use with two-terminal recording heads. They provide a low noise read amplifier, write current control, and data protection circuitry for up to four channels. The SSI 2300R option provides internal 350Ω damping resistors. Damping resistors are switched in during Write mode and switched out during Read mode. The SSI 32R2300 option does not provide a damping resistor. Power supply fault protection is provided by disabling the write current generator during power sequencing. System write to read recovery time is significantly improved by making the read channel outputs high impedance.

The SSI 32R2300/2300R require only a +3.3V power supply and are available in a variety of packages. They are hardware compatible with the SSI 32R4610A and SSI 32R2020R Read/Write devices. The SSI 32R2301/2301R is identical to the SSI 32R2300/2300R, but comes in 24-pin package.

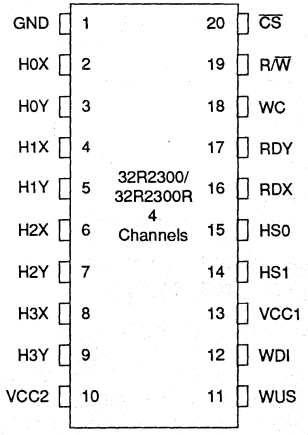
FEATURES

- **+3.0V to +5.5V voltage supply**
- **Low power**
  - **PD = 63 mW Read mode (Nom) (@3.3V supply)**
  - **PD = 1 mW idle (Max) (@3.3V)**
- **High Performance:**
  - **Read mode gain = 200 V/V**
  - **Input noise = 0.50 nV/√Hz (Nom)**
  - **Input capacitance = 9 pF (Nom)**
  - **Write current range = 2-30 mA**
- **Self switching damping resistance**
- **Pin compatible with the SSI 32R4610AR and SSI 32R2020R**
- **Write unsafe detection**
- **Power supply fault protection**

BLOCK DIAGRAM



PIN DIAGRAM



20-Lead SOL, VSOP

CAUTION: Use handling procedures necessary for a static sensitive component.

CIRCUIT OPERATION

The SSI 32R2300/2300R have the ability to address up to 4 two-terminal heads and provide write drive or read amplification. Mode control and head selection are described in Tables 1 and 2. The TTL inputs R/$\overline{W}$, $\overline{CS}$, HS0 and HS1 have internal pull-up resistors.

TABLE 1: Mode Select

$\overline{CS}$	R/$\overline{W}$	Mode
0	0	Write
0	1	Read
1	0	Idle
1	1	Idle

TABLE 2: Head Select

HS1	HS0	Head
0	0	0
0	1	1
1	0	2
1	1	3

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
HS0, HS1 †	I	Head Select: selects one of four heads
$\overline{CS}$	I	Chip Select: a high inhibits the chip
R/$\overline{W}$ †	I	Read/Write : a high selects Read mode
WUS †	O	Write Unsafe: a high indicates an unsafe writing condition
WDI †	I	Write Data In: a negative transition on WDI changes the direction of the current in the recording head
H0X - H3X; H0Y - H3Y	I/O	X, Y Head Connections
RDX, RDY †	O	X, Y Read Data: differential read data output
WC		Write Current: used to set the magnitude of the write current
VCC1	I	Power Supply
VCC2	I	Power Supply for Write current drivers
GND	I	Ground

† When more that one R/W device is used, signals can be wire OR'ed

WRITE MODE

Taking both $\overline{CS}$ and R/$\overline{W}$ low selects Write mode which configures the SSI 32R2300/2300R as a current switch and activates the Write Unsafe (WUS) detector circuitry. Head current is toggled between the X and Y side of the selected head on each high to low transition of the Write Data Input (WDI). Note that a preceding Read to Write transition or Idle to Write transition initializes the Write Data Flip-Flop to pass write current into the "X" side of the device. In this case, the Y side is higher potential than the X side. The magnitude of the write current (0-pk) is given by:

$$Iw = Aw \cdot \frac{Vwc}{Rwc} = K/Rwc$$

where Aw is the write current gain.
RWC is connected from pin WC to GND. Note the actual head current Ix, y is given by:

$$Ix, y = \frac{Iw}{1 + Rh/Rd}$$

Where:

Rh = Head resistance plus external wire resistance
Rd = Damping resistance

In Write mode a 350 Ω damping resistor is switched in across the Hx, Hy ports (32R2300R only).

VOLTAGE FAULT

A voltage Fault detection circuit improves data security by disabling the write current generator during a voltage fault or power startup in Read or Write mode.

WRITE UNSAFE

Any of the following conditions will be indicated as a high level on the Write Unsafe, WUS, open collector output.

- WDI frequency too low
- Device in Read mode
- Device not selected
- Open head
- Head short to ground

WUS is valid in the write current/head characteristic region defined by $5 < Ih \cdot Lh < 50$ mA • μH, and $1 < Rh < 1.25/Ih$. After the fault condition is removed, one negative transition on WDI is required to clear WUS. Overcurrent protection during a head short to ground is accomplished by placing a series resistor between VCC1 and VCC2. The write current driver will shut down when VCC1 - VCC2 ≥ 0.3V. The resistor must be sized so that VCC1 - VCC2 ≤ 0.15V in normal operation.

READ MODE

The Read mode configures the SSI 32R2300/2300R as a low noise differential amplifier and deactivates the write current generator. The damping resistor is switched out of the circuit allowing a high impedance input to the read amplifier. The RDX and RDY output are driven by emitter followers. They should be AC coupled to the load. The HnX, HnY inputs are non-inverting to the RDX, RDY outputs.

Note that in Idle or Write mode, the read amplifier is deactivated and RDX, RDY outputs become high impedance. This facilitates multiple R/W applications (wired-OR RDX, RDY) and minimizes voltage change when switching from Write to Read mode. Note also that the write current source is deactivated for both the Read and Idle mode.

IDLE MODE

Taking $\overline{CS}$ high selects the Idle mode which switches the RDX and RDY outputs into a high impedance state and deactivates the device. Power consumption in this mode is held to a minimum.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may permanently damage the device.

PARAMETER		RATING
DC Supply Voltage	VCC1	-0.3 to +7 VDC
	VCC2	-0.3 to +7 VDC
Write Current	Iw	30 mA
Digital Input Voltage	Vin	-0.3 to VCC1 +0.3 VDC
Head Port Voltage	VH	-0.3 to VCC2 +0.3 VDC
Output Current: RDX, RDY	I0	-10 mA
	WUS	+8 mA
Storage Temperature	Tstg	-55 to +150°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	RATING
DC Supply Voltage VCC1 = VCC2	3.3 ±10%, 5.0 ±10% VDC
Recommended Head Load Range Lh	0.3 - 5.0 µH
WUS Operating Range Iw • Lh	5.0 - 50.0 mA • µH
Head Differential Load Capacitance	15 pF max
Ambient Operating Temperature	0 - 70 °C

DC CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VCC1 Supply Current	Read Mode Vcc = 3.3V ±10%		19	29	mA
	Write Mode Vcc = 3.3V ±10%		2 + 0.2 Iw	3 + 0.3 Iw	mA
	Idle Mode Vcc = 3.3V ±10%		0.15	0.27	mA
VCC2 Supply Current	Read Mode Vcc = 3.3V ±10%		-	0.1	mA
	Write Mode Vcc = 3.3V ±10%		1.0 + Iw	3.0 + Iw	mA
	Idle Mode Vcc = 3.3V ±10%		-	0.01	mA
Power Dissipation	Read Mode Vcc = 3.3V ±10%		63	105	mW
	Write Mode Vcc = 3.3V ±10%		10 + 4 • Iw	20 + 5 • Iw	mW
	Idle Mode Vcc = 3.3V ±10%		0.5	1	mW
VCC1 Supply Current	Read Mode Vcc = 5.0V ±10%		20	32	mA
	Write Mode Vcc = 5.0V ±10%		3 + 0.2 Iw	5 + 0.3 Iw	mA
	Idle Mode Vcc = 5.0V ±10%		0.25	0.45	mA
VCC2 Supply Current	Read Mode Vcc = 5.0V ±10%			0.1	mA
	Write Mode Vcc = 5.0V ±10%		2.0 + Iw	4.0 + Iw	mA
	Idle Mode Vcc = 5.0V ±10%			0.01	mA
Power Dissipation	Read Mode Vcc = 5.0V ±10%		100	180	mW
	Write Mode Vcc = 5.0V ±10%		20 + 6 • Iw	45 + 7.2 Iw	mW
	Idle Mode Vcc = 5.0V ±10%		1.25	2.5	mW

DIGITAL INPUTS

Input Low voltage (VIL)					0.8	VDC
Input High Voltage (VIH)			2.0			VDC
Input Low Current	VIL = 0.4	Vcc = 3.6V	-0.4	-.09		mA
		Vcc = 5.5V	-0.4	-0.13		mA
Input High Current	VIH = 2.7V		0	20		µA
WUS Output Low Voltage (VOL)	Iol = 2 mA max		.35	0.5		VDC
Input Low Current	2 channel version	Vcc = 3.6V	-0.4	-0.22		
	for HSO	Vcc = 5.5V	-0.6	-0.35		

WRITE CHARACTERISTICS
Recommended operating conditions apply unless otherwise specirfied.

PARAMETER	CONDITIONS		MIN	NOM	MAX	UNIT
VCC1 Fault Voltage	Iw < 0.2 mA			2.5	2.75	VDC
Write Current Gain	Iw = 2-5 mA Vcc = 3.3V±10%		18.0	22.0	24.9	mA/mA
	Iw = 5-30 mA Vcc = 3.3V±10%		18.3	20.5	23.0	mA/mA
	Iw = 2-5 mA Vcc = 5.0V±10%		18.6	23.1	26.0	mA/mA
	Iw = 5-30 mA Vcc = 5.0V±10%		18.9	21.7	24.1	mA/mA
Write Current Voltage (VWC)			1.2	1.3	1.4	V
Differential Head Voltage Swing	Open head		4.0	4.8		Vpp
Unselected Head Current	AC				0.1 Iw	mA (pk)
	DC				0.1	mA
Head Differential Load		32R2300	2400	3000	3600	Ω
Resistance (Rd)		32R2300R	250	350	450	Ω
WDI Pulse Width	Vil ≤ 0.8V, Vih ≥ 2.0V	PWH	5			ns
	$t_f = t_r$ = 1ns	PWL	10			ns
Write Current Range (Iw)			2		30	mA

READ CHARACTERISTICS
Recommended operating conditions apply unless otherwise specified. CL (RDX, RDY) < 20 pF, RL (RDX, RDY) = 1 kΩ.

Differential Voltage Gain		Vin = 1 mVpp @1 MHz	160	200	240	V/V
Voltage BW	-1dB	|Zs| < 5Ω, Vin = 1 mVpp	20	35		MHz
	-3dB		40	70		MHz
Input Noise Voltage		BW = 15 MHz, Lh = 0, Rh = 0		0.50	0.75	nV/√Hz
Input Noise Current				3		pA/√Hz
Differential Input Capacitance		Vin = 1 mVpp, f = 5 MHz		9	14	pF
Differential Input Resistance		Vin = 1 mVpp, f = 5 MHz				
		32R2300	500	750	1800	Ω
		32R2300R	500	750	1800	Ω
Dynamic Range		AC input voltage where gain falls to 90% of its small signal gain value, f = 5 MHz	2	5		mVpp
Common Mode Rejection Ratio		Vin = 0 VDC + 100 mVpp @ 5 MHz	45	60		dB
Power Supply Rejection Ratio		100 mVpp @ 5 MHz on VCC	40	70		dB
Channel Separation		Unselected channels driven with Vin = 0 VDC + 100 mVpp	45	60		dB

READ CHARACTERISTICS (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Output Offset Voltage	Head shorted	-200		+200	mV
	Head opened	-250		+250	mV
Single Ended Output Resistance	f = 5 MHz		60	100	Ω
Output Current	AC coupled load, RDX to RDY	1.0	2.0		mA
RDX, RDY Common Mode Output Voltage		Vcc-1.0	Vcc-1.35	Vcc-1.70	VDC

SWITCHING CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified. IW = 15 mA, Lh = 1.0 µH, Rh = 30Ω f(Data) = 5 MHz.

R/$\overline{W}$	Read to Write	R/$\overline{W}$ to 90% of write current; WUS valid		0.3	1.0	µs
	Write to Read	R/$\overline{W}$ to 90% of 100 mV Read signal envelope		0.4	1	µs
$\overline{CS}$	Unselect to Select	$\overline{CS}$ to 90% of 100 mV 10 MHz Read signal envelope		0.6	2	µs
	Select to Unselect	$\overline{CS}$ to 10% of write current		0.1	1	µs
HS0,1 to any Head		To 90% of 100 mV 10 MHz Read signal envelope		0.2	1	µs
WUS*	Safe to Unsafe (TD1)	Write mode, loss of WDI transitions; Defines max WDI period for WUS operation	0.6	2.0	3.6	µs
	Unsafe to Safe (TD2)	Fault cleared: from first negative WDI transition		0.2	1.0	µs
WDI	Frequency Range	Valid WUS	1.67		25	MHz
Head Current		Lh = 0, Rh = 0				
	WDI to Ix - Iy (TD3)	from 50% points		25	40	ns
	Asymmetry	WDI has 1 ns rise/fall time			1.5	ns
	Rise/fall Time	10% to 90% points				
		Iw = 15 mA, Rh = 0, Lh = 0		6	9	ns
		Iw = 15 mA, Rh = 30Ω, Lh = 1µH		14	18	ns

* $5 < Iw \cdot Lh < 50$ mA • µH, $1 < Rh \leq 1.25/Iw$

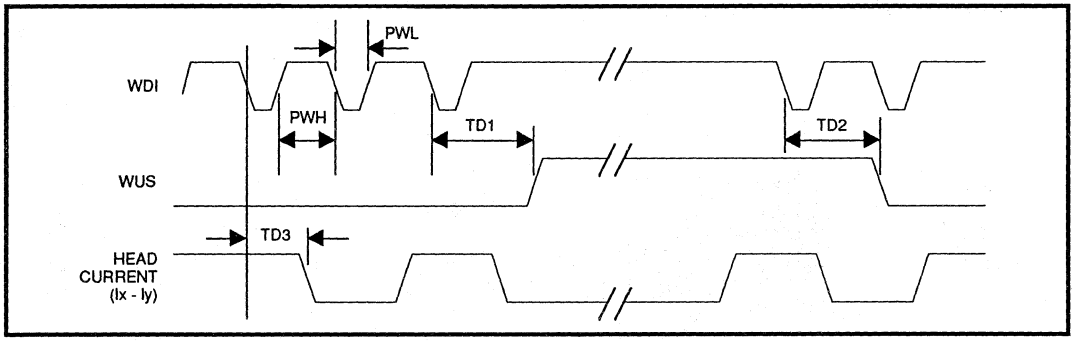
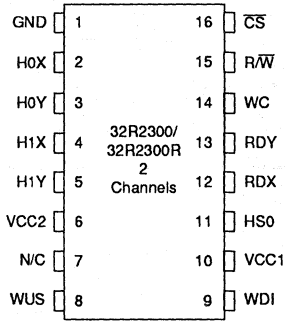


FIGURE 1: Write Mode Timing Diagram

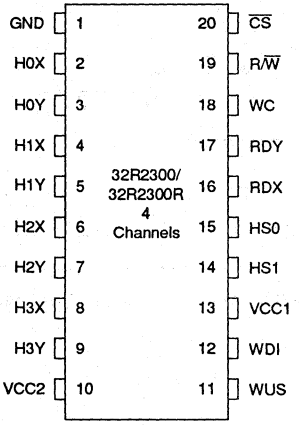
SSI 32R2300/2300R/2301/2301R
3.3V, 5V, 2, 4-Channel
2-Terminal Read/Write Device

PACKAGE PIN DESIGNATIONS

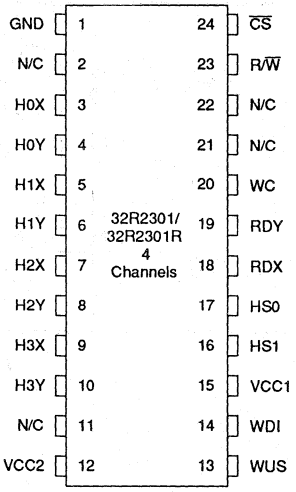
(Top View)



16-Lead SOL



20-Lead SOL, VSOP



24-Lead VSOP

CAUTION: Use handling procedures necessary for a static sensitive component.

ORDERING INFORMATION

PART DESCRIPTION	ORDERING NUMBER	PACKAGE MARK
SSI 32R2300R/2301R R Version		
2-Channel 16-Lead SOL	32R2300R-2CL	32R2300R-2CL
4-Channel 20-Lead SOL	32R2300R-4CL	32R2300R-4CL
4-Channel 20-Lead SOV	32R2300R-4CV	32R2300R-4CV
4-Channel 24-Lead SOV	32R2301R-4CV	32R2301R-4CV
SSI 32R2300/2301 Non-R Version		
2-Channel 16-Lead SOL	32R2300-2CL	32R2300-2CL
4-Channel 20-Lead SOL	32R2300-4CL	32R2300-4CL
4-Channel 20-Lead SOV	32R2300-4CV	32R2300-4CV
4-Channel 24-Lead SOV	32R2301-4CV	32R2301-4CV

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914

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SSI 32R2320/21/22/23/24
3V, 5V, 4-Channel 2-Terminal Read/Write Device
Advance Information

October 1993

3

DESCRIPTION

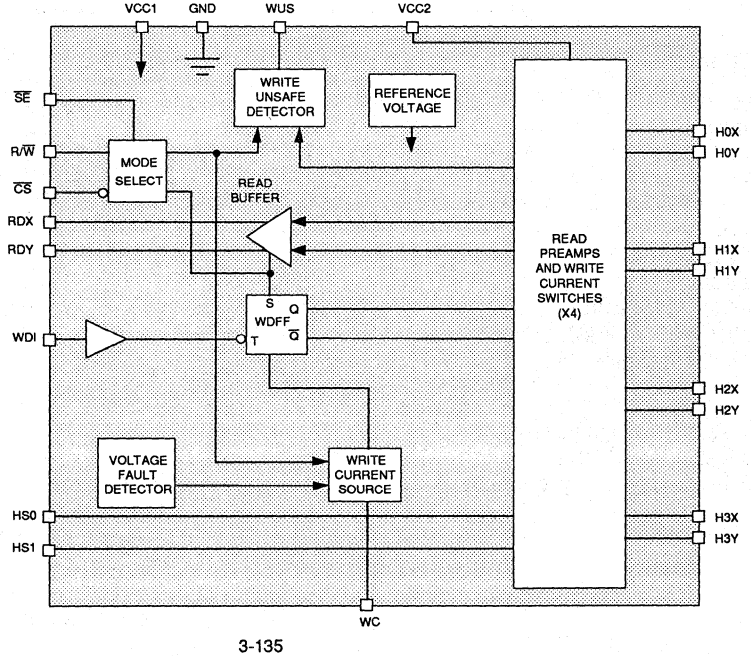
The SSI 32R2320/21/22/23/24 are BiCMOS monolithic integrated circuit designed for use with two-terminal recording heads. They provide a low noise read amplifier, write current control, and data protection circuitry for up to four channels. This family of devices has been designed to support servo bank write, TTL or ECL write data input, and write unsafe output through various bond options. In addition, versions of the devices are available with or without internal damping resistors. When configured with damping resistors, the resistors are switched in during write mode and switched out during read mode. Power supply fault protection is provided by disabling the write current generator during power sequencing. System write to read recovery time is significantly improved by making the read channel outputs high impedance.

The SSI 32R2320/21/22/23/24 require a single 3.0 to 5.5V power supply and are available in a variety of packages. They are hardware compatible with the SSI 32R4610A and SSI 32R2020R Read/Write devices.

FEATURES

- **+3.0V - 5.5V voltage supply**
- **Low power**
  - **PD = 73 mW Read mode (Nom) (@3.3V supply)**
  - **PD = 75 µW Idle (Max @ Vcc = 3.3V)**
- **High Performance:**
  - **Read mode gain = 250 V/V**
  - **Input noise = 0.50 nV/√Hz (Nom)**
  - **Input capacitance = 9 pF (Nom)**
  - **Write current range = 2-30 mA**
- **Bond options for:**
  - **Self switching damping resistance**
  - **Servo bank write**
  - **TTL or ECL write data input**
  - **Write unsafe detection**
- **Power supply fault protection**

BLOCK DIAGRAM



SSI 32R2320/21/22/23/24
3V, 5V, 4-Channel
2-Terminal Read/Write Device

FUNCTIONAL DESCRIPTION

The SSI 32R2320/21/22/23/24 have the ability to address up to 4 two-terminal heads and provide write drive or read amplification. Mode control and head selection are described in Tables 1 and 2. The TTL inputs R/$\overline{W}$, $\overline{CS}$ and DMP have internal pull-up resistors. The TTL inputs HS0 and HS1 have internal pull down resistors.

TABLE 1: Mode Select

$\overline{CS}$	R/$\overline{W}$	$\overline{SE}$	Mode
0	0	1	Write
0	1	X	Read
1	0	X	Idle
1	1	X	Idle
0	0	0	Servo Write

TABLE 2: Head Select

HS1	HS0	Head
0	0	0
0	1	1
1	0	2
1	1	3

WRITE MODE

Taking both $\overline{CS}$ and R/$\overline{W}$ low selects write mode which configures the device as a current switch and activates the Write Unsafe (WUS) detector circuitry. Head current is toggled between the X and Y side of the selected head on each high to low transition of the Write Data Input (WDI). Note that a preceding Read to Write transition or Idle to Write transition initializes the Write Data Flip-Flop to pass write current into the "X" side of the device. In this case, the Y side is higher potential than the X side. The magnitude of the write current (0-pk) is given by:

$$Iw = Aw \bullet \frac{Vwc}{Rwc} = K/Rwc$$

where Aw is the write current gain.
RWC is connected from pin WC to GND. Note the actual head current Ix, y is given by:

$$Ix, y = \frac{Iw}{1 + Rh/Rd}$$

Where:

Rh = Head resistance plus external wire resistance
Rd = Damping resistance

In Write mode a 350Ω damping resistor is switched in across the Hx, Hy ports.

VOLTAGE FAULT

A voltage Fault detection circuit improves data security by disabling the write current generator during a voltage fault or power startup in Read or Write mode.

WRITE UNSAFE

Any of the following conditions will be indicated as a high level on the Write Unsafe, WUS, open collector output.

- WDI frequency too low
- Device in Read mode
- Device not selected
- Open head
- Head short to ground
- No write current

WRITE UNSAFE (continued)

WUS is valid in the write current/head characteristic region defined by 5 < Ih • Lh < 50 mA • µH, and 1 < Rh < 1.25/Ih. After the fault condition is removed, one negative transition on WDI is required to clear WUS.

READ MODE

The Read mode configures the SSI 32R2320RZ as a low noise differential amplifier and deactivates the write current generator. The damping resistor is switched out of the circuit allowing a high impedance input to the read amplifier. The RDX and RDY output are driven by emitter followers. They should be AC coupled to the load. The HnX, HnY inputs are non-inverting to the RDX, RDY outputs.

Note that in Idle or Write mode, the read amplifier is deactivated and RDX, RDY outputs become high impedance. This facilitates multiple R/W applications (wired-OR RDX, RDY) and minimizes voltage change when switching from Write to Read mode. Note also that the write current source is deactivated for both the Read and Idle mode.

IDLE MODE

Taking $\overline{CS}$ high selects the Idle mode which switches the RDX and RDY outputs into a high impedance state and deactivates the device. Power consumption in this mode is held to a minimum at $\overline{CS}$, input is greater than (Vcc - 0.3V).

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PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
HS0, HS1 †	I	Head Select: selects one of four heads
$\overline{CS}$	I	Chip Select: a high inhibits the chip
R/$\overline{W}$ †	I	Read/Write : a high selects Read mode
WUS †	O	Write Unsafe: a high indicates an unsafe writing condition
WDI/$\overline{WDI}$ †	I	Write Data Input: On TTL versions, a negative transition on WDI changes the direction of the current in the recording head. On ECL versions, a positive transition on the WDI (negative transition on $\overline{WDI}$ changes the direction of the current in the recording head. $\overline{WDI}$ is only present on the ECL versions.
H0X - H3X; H0Y - H3Y	I/O	X, Y Head Connections
RDX, RDY †	O	X, Y Read Data: differential read data output
WC		Write Current: used to set the magnitude of the write current
VCC1	I	Power Supply
GND	I	Ground
$\overline{SE}$	I	Servo Enable: A low input on this line enables the servo bank write mode when $\overline{CS}$ and R/$\overline{W}$ are both low.
WUS/SE	I	Write Unsafe/Servo Enable (32R2323/24 only): Under normal operation, a high level output on this pin indicates a write unsafe condition. When this pin is driven externally above VCC and $\overline{CS}$ and R/$\overline{W}$ are both low, servo write mode is activated.
DMP	I	Damping Resistor Enable (32R2322 only): A high (or open) level on this input enables the switchable damping resistor. A low level on this input disables the damping resistor.

† When more that one R/W device is used, signals can be wire OR'ed

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may permanently damage the device.

PARAMETER		RATING
DC Supply Voltage	VCC1	-0.3 to +7 VDC
	VCC2	-0.3 to +7 VDC
Write Current	Iw	30 mA
Digital Input Voltage	Vin	-0.3 to VCC1 +0.3 VDC
Head Port Voltage	VH	-0.3 to VCC2 +0.3 VDC
Output Current: RDX, RDY	I0	-10 mA
	WUS	+8 mA
Storage Temperature	Tstg	-55 to +150°

RECOMMENDED OPERATING CONDITIONS

PARAMETER		RATING
DC Supply Voltage		3.3 ±10%, 5.0 ±10% VDC
Recommended Head Load Range	Lh	0.3 - 5.0 µH
WUS Operating Range	Iw • Lh	5.0 - 50.0 mA • µH
Head Differential Load Capacitance		15 pF max
Ambient Operating Temperature*		0 - 70 °C

* Derating is required when in Servo Write mode.

DC CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VCC1 Supply Current	Vcc = 3.3V ±10% Read		22.0	30.0	mA
	Vcc = 3.3V ±10% Write		5+1.2 • Iw	9+1.4 • Iw	mA
	Vcc = 3.3V ±10% Servo		6+4.5 • Iw	11+4.7 • Iw	mA
	Vcc = 3.3V ±10% Idle, $\overline{CS}$ = Vcc		3	20	µA
	Vcc = 3.3V ±10% Idle, $\overline{CS}$ = 2.7V		30	200	µA
Power Dissipation	Vcc = 3.3V ±10% Read		73	110	mW
	Vcc = 3.3V ±10% Write		17+4 • Iw	33+5 • Iw	mW
	Vcc = 3.3V ±10% Servo		20+15 • Iw	40+17 • Iw	mW
	Vcc = 3.3V ±10% Idle, $\overline{CS}$ = Vcc		9	75	µW
	Vcc = 3.3V ±10% Idle, $\overline{CS}$ = 2.7V		100	730	µW

DC CHARACTERISTICS (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VCC1 Supply Current	Vcc = 5.0V ±10% Read		23.0	32.0	mA
	Vcc = 5.0V ±10% Write		6+1.2 • Iw	10+1.3 • Iw	mA
	Vcc = 5.0V ±10% Servo		7+4.4 • Iw	12+4.7 • Iw	mA
	Vcc = 5.0V ±10% Idle, $\overline{CS}$ = Vcc		5	30	µA
	Vcc = 5.0V ±10% Idle, $\overline{CS}$ = 2.7V		250	450	µA
Power Dissipation	Vcc = 5.0V ±10% Read		115	180	mW
	Vcc = 5.0V ±10% Write		30+6 • Iw	55+7 • Iw	mW
	Vcc = 5.0V ±10% Servo		35+22 • Iw	66+26 • Iw	mW
	Vcc = 5.0V ±10% Idle, $\overline{CS}$ = Vcc		0.03	0.17	mW
	Vcc = 5.0V ±10% Idle, CS = 2.7V		1.25	2.5	mW

DIGITAL INPUTS

Input Low voltage (VIL)	$\overline{CS}$, R/$\overline{W}$, WDI, HSn and $\overline{SE}$			0.8	VDC
Input High Voltage (VIH)	$\overline{CS}$, R/$\overline{W}$, WDI, HSn and $\overline{SE}$	2.0			VDC
Input Low Current	VIL = 0.4 Vcc = 3.6V	-0.4	-.09		mA
	$\overline{CS}$, R/$\overline{W}$, WDI, $\overline{SE}$ Vcc = 5.5V	-0.4	-0.13		mA
Input High Current	VIH = 2.7V $\overline{CS}$, R/$\overline{W}$, WDI, $\overline{SE}$		0	20	µA
WUS Output Low Voltage (VOL)	Iol = 2 mA max		0.35	0.5	VDC
Input Low Current	HSn and $\overline{SE}$ VIL = 0.4V		10	40	µA
Input High Current	HSn and $\overline{SE}$ VIH = 2.7V		100	400	µA
Input Low Voltage	WD, $\overline{WD}$	Vcc -1.0		Vcc -0.4	V
Input High Voltage	WD, $\overline{WD}$	Vcc -2.0		Vcc -0.8	V
Δ VIN	|WD - $\overline{WD}$|	0.4	0.8		V
Input Low Current	WD, $\overline{WD}$ Vcc = 5V VIH = Vcc - 0.8V		100	200	µA
Input High Current	WD, $\overline{WD}$ Vcc = 5V VIL = Vcc - 1.6V		75	150	µA

ELECTRICAL SPECIFICATIONS (continued)

WRITE CHARACTERISTICS

Recommended operating conditions apply unless otherwise specirfied.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VCC1 Fault Voltage	Iw < 0.2 mA		2.5	2.75	VDC
Write Current Gain (Aw)	Iw = 2-5 mA Vcc = 3.3V±10%	19.5	22.0	26.4	mA/mA
	Iw = 5-30 mA Vcc = 3.3V±10%	18.3	20.5	23.0	mA/mA
	Iw = 2-5 mA Vcc = 5.0V±10%	20.6	23.1	28.0	mA/mA
	Iw = 5-30 mA Vcc = 5.0V±10%	19.3	21.7	24.5	mA/mA
Write Current Error	Rwc = 2 kΩ, head to head @ Write mode*	-5		+5	%
	Rwc = 2 kΩ, head to head @ Servo mode*	-5		+5	%
	Rwc = 2 kΩ, Write to Servo	-7		+7	%
Write Current Voltage (VWC)		1.2	1.3	1.4	V
Differential Head Voltage Swing	Open head, $\overline{SE}$ = 1	4.0	4.8		Vpp
	Open head, Vcc = 5V, $\overline{SE}$ = 0	4.0	4.8		Vpp
	Open head, Vcc = 3.3V, $\overline{SE}$ = 0	3.4	4.8		Vpp
Unselected Head Current	AC			1	mA (pk)
	DC			0.1	mA
Head Differential Load	R version	300	400	500	Ω
Resistance (Rd)	non-R version	2400	3000	3600	Ω
WDI Pulse Width	Vil ≤ 0.8V, Vih ≥ 2.0V PWH	5			ns
	$t_f = t_r$ = 1ns PWL	10			ns
Write Current Range (Iw)		2		30	mA

* Error from average of the four heads.

READ CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified. CL (RDX, RDY) < 20 pF, RL (RDX, RDY) = 1 kΩ.

Differential Voltage Gain		Vin = 1 mVpp @1 MHz	200	250	300	V/V
Voltage BW	-1dB	|Zs| < 5Ω, Vin = 1 mVpp	20	40		MHz
	-3dB		40	80		MHz
Input Noise Voltage		BW = 15 MHz, Lh = 0, Rh = 0		0.50	0.75	nV/√Hz
Differential Input Capacitance		Vin = 1 mVpp, f = 5 MHz		9	14	pF
Differential Input Resistance		Vin = 1 mVpp, f = 5 MHz	500	750	1800	Ω

READ CHARACTERISTICS (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Dynamic Range	AC input voltage where gain falls to 90% of its small signal gain value, f = 5 MHz	2	5		mVpp
Common Mode Rejection Ratio	Vin = 0 VDC + 100 mVpp @ 5 MHz	45	60		dB
Power Supply Rejection Ratio	100 mVpp @ 5 MHz on VCC	40	70		dB
Channel Separation	Unselected channels driven with Vin = 0 VDC + 100 mVpp	45	60		dB
Output Offset Voltage	Head shorted	-250		+250	mV
	Head opened	-300		+300	mV
Single Ended Output Resistance	f = 5 MHz		60	100	Ω
Output Current	AC coupled load, RDX to RDY	1.0	2.0		mA
RDX, RDY Common Mode Output Voltage		Vcc-1.0	Vcc-1.35	Vcc-1.70	VDC

SWITCHING CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified. Rwc = 2kΩ, Lh = 1.0 µH, Rh = 30Ω f(Data) = 5 MHz.

R/$\overline{W}$	Read to Write	R/$\overline{W}$ to 90% of write current; WUS valid		0.3	1.0	µs
	Write to Read	R/$\overline{W}$ to 90% of 100 mV Read signal envelope		0.4	1	µs
$\overline{CS}$	Unselect to Select	$\overline{CS}$ to 90% of 100 mV 10 MHz Read signal envelope		0.6	2	µs
	Select to Unselect	$\overline{CS}$ to 10% of write current		0.4	1	µs
HS0,1 to any Head		To 90% of 100 mV 10 MHz Read signal envelope		0.2	1	µs
WUS*	Safe to Unsafe (TD1)	Write mode, loss of WDI transitions; Defines max WDI period for WUS operation	0.6	2.0	3.6	µs
	Unsafe to Safe (TD2)	Fault cleared: from first negative WDI transition		0.2	1.0	µs
WDI	Frequency Range	Valid WUS	1.67		25	MHz
* 5 < Iw • Lh < 50 mA • µH, 1 < Rh ≤ 1.25/Iw, WUS available in bonding option.						

SWITCHING CHARACTERISTICS (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Head Current	Lh = 0, Rh = 0				
WDI to Ix - Iy (TD3)	from 50% points		25	40	ns
Asymmetry	WDI has 1 ns rise/fall time			1.5	ns
Rise/fall Time	10% to 90% points				
	Rwc = 2kΩ, Rh = 0, Lh = 0		2	9	ns
	Rwc = 2kΩ, Rh = 30Ω, Lh = 1μH		14	18	ns

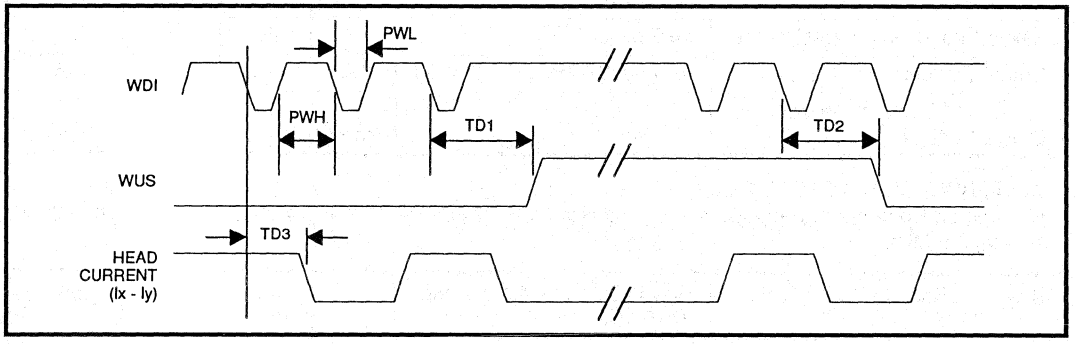


FIGURE 1: Write Mode Timing Diagram

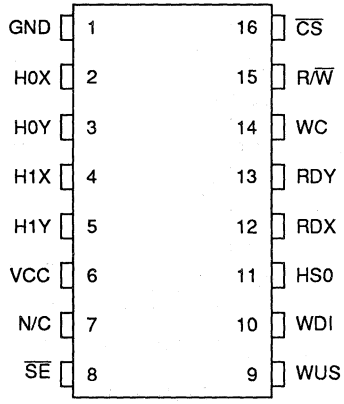
TABLE 1: Device Option Summary

Device #	WDI Type	Servo Enable	Damping Resistor	WUS
32R2320W	TTL	$\overline{SE}$	No	No
32R2320RW	TTL	$\overline{SE}$	350Ω	No
32R2321W	ECL	$\overline{SE}$	No	No
32R2321RW	ECL	$\overline{SE}$	350Ω	No
32R2322RW	TTL	SE	DMP pin	Yes
32R2323W	TTL	WUS/SE	No	Yes
32R2323RW	TTL	WUS/SE	350Ω	Yes
32R2324W	ECL	WUS/SE	No	Yes
32R2324RW	ECL	WUS/SE	350Ω	Yes

PACKAGE PIN DESIGNATIONS

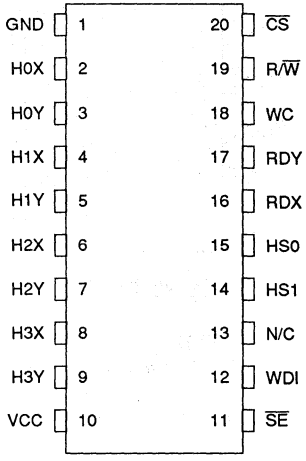
(Top View)

32R2320 Package Options



16-Pin Packages:

32R2320RW-2CL (SOL)
32R2320W-2CL (SOL)
32R2320RW-2CN (SON)
32R2320W-2CN (SON)



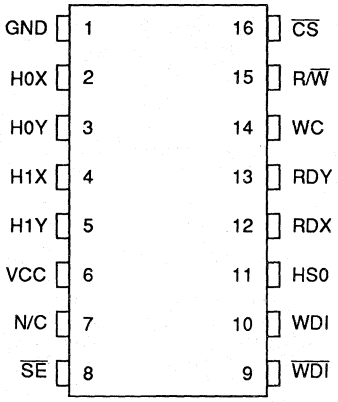
20-Pin Packages:

32R2320RW-4CL (SOL)
32R2320W-4CL (SOL)
32R2320RW-4CV (VSOP)
32R2320W-4CV (VSOP)
32R2320RW-4CVT (VTSOP)
32R2320W-4CVT (VTSOP)

CAUTION: Use handling procedures necessary for a static sensitive component.

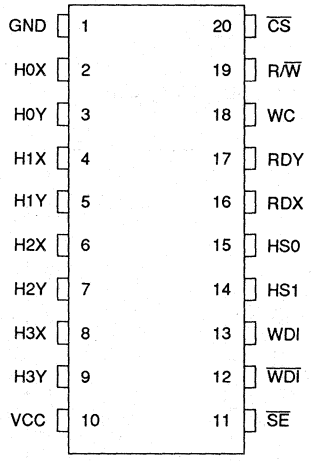
SSI 32R2320/21/22/23/24
3V, 5V, 4-Channel
2-Terminal Read/Write Device

32R2321 Package Options



16-Pin Packages:

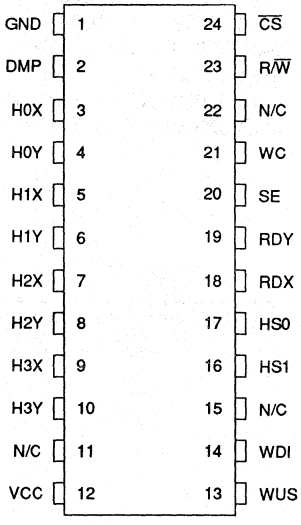
32R2321RW-2CL (SOL)
32R2321W-2CL (SOL)
32R2321RW-2CN (SON)
32R2321W-2CN (SON)



20-Pin Packages:

32R2321RW-4CL (SOL)
32R2321W-4CL (SOL)
32R2321RW-4CV (VSOP)
32R2321W-4CV (VSOP)
32R2321RW-4CVT (VTSOP)
32R2321W-4CVT (VTSOP)

32R2322 Package Options



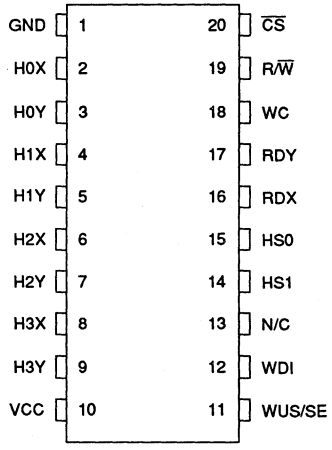
24-Pin Packages:
32R2322RW-4CVT (VTSOP)

CAUTION: Use handling procedures necessary for a static sensitive component.

PACKAGE PIN DESIGNATIONS (continued)

(Top View)

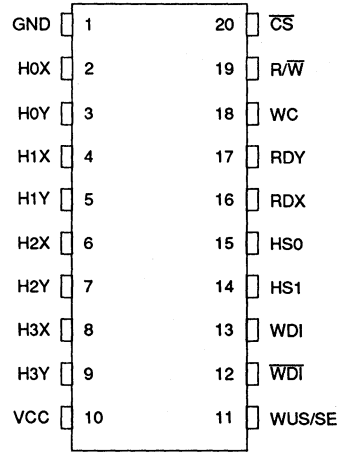
32R2323 Package Options



20-Pin Packages:

32R2323RW-4CV (VSOP)
32R2323W-4CV (VSOP)

32R2324 Package Options



20-Pin Packages:

32R2324RW-4CV (VSOP)
32R2324W-4CV (VSOP)

CAUTION: Use handling procedures necessary for a static sensitive component.

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914

Notes:

silicon systems®
A TDK Group Company

SSI 32R2420
5V, 4-Channel 2-Terminal Read/Write Device

Advance Information

November 1993

3

DESCRIPTION

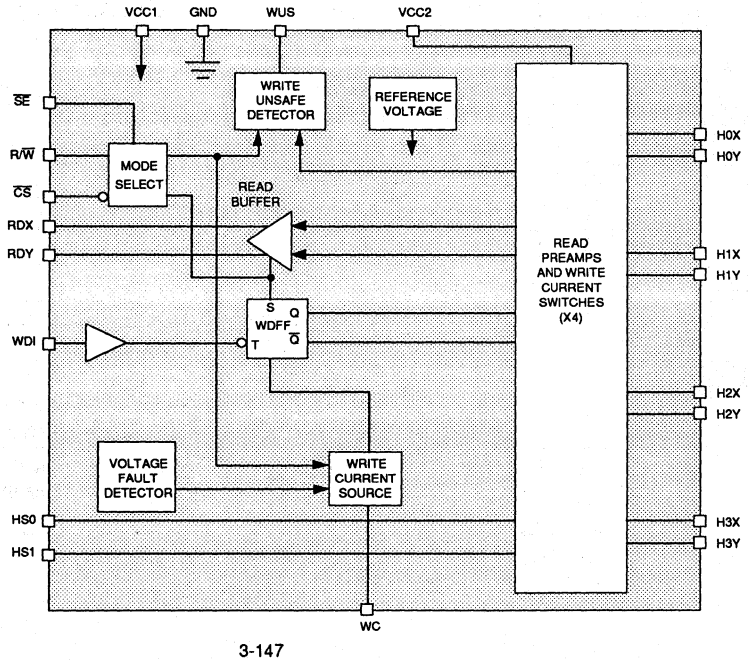
The SSI 32R2420 is a BiCMOS monolithic integrated circuit designed for use with two-terminal recording heads. It provides a low noise read amplifier, write current control, and data protection circuitry for up to four channels. This device has been designed to support servo bank write, TTL or ECL write data input, and write unsafe output through various bond options. In addition, versions of the devices are available with or without internal damping resistors. When configured with damping resistors, the resistor is switched in during Write mode and switched out during Read mode. Power supply fault protection is provided by disabling the write current generator during power sequencing. System write to read recovery time is significantly improved by making the read channel outputs high impedance.

The SSI 32R2420 requires a single 5.0V power supply and is available in a variety of packages. It is hardware compatible with the SSI 32R4610A and SSI 32R2020R Read/Write devices.

FEATURES

- **5.0V power supply**
- **Low power**
  - **PD = 115 mW Read mode (Nom)**
  - **PD = 0.17 mW Idle (Max @ $\overline{CS}$ = Vcc)**
- **High Performance:**
  - **Read mode gain = 250 V/V**
  - **Input noise = 0.50 nV/√Hz (Nom)**
  - **Input capacitance = 9 pF (Nom)**
  - **Write current range = 2-30 mA**
- **Bond options for:**
  - **Self switching damping resistance**
  - **Servo bank write**
  - **TTL or ECL write data input**
  - **Write unsafe detection**
- **Power supply fault protection**

BLOCK DIAGRAM



SSI 32R2420
5V, 4-Channel
2-Terminal Read/Write Device

CIRCUIT OPERATION

The SSI 32R2420 has the ability to address up to 4 two-terminal heads and provide write drive or read amplification. Mode control and head selection are described in Tables 1 and 2. The TTL inputs R/$\overline{W}$, $\overline{CS}$ and DMP have internal pull-up resistors. The TTL inputs HS0 and HS1 have internal pull down resistors.

TABLE 1: Mode Select

$\overline{CS}$	R/$\overline{W}$	$\overline{SE}$	Mode
0	0	1	Write
0	1	X	Read
1	0	X	Idle
1	1	X	Idle
0	0	0	Servo Write

TABLE 2: Head Select

HS1	HS0	Head
0	0	0
0	1	1
1	0	2
1	1	3

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
HS0, HS1 †	I	Head Select: selects one of four heads
$\overline{CS}$	I	Chip Select: a high inhibits the chip
R/$\overline{W}$ †	I	Read/Write: a high selects Read mode
WUS †	O	Write Unsafe: a high indicates an unsafe writing condition
WDI/$\overline{WDI}$ †	I	Write Data Input: On TTL versions, a negative transition on WDI changes the direction of the current in the recording head. On ECL versions, a positive transition on the WDI (negative transition on $\overline{WDI}$ changes the direction of the current in the recording head. $\overline{WDI}$ is only present on the ECL versions.
H0X - H3X; H0Y - H3Y	I/O	X, Y Head Connections
RDX, RDY †	O	X, Y Read Data: differential read data output
WC		Write Current: used to set the magnitude of the write current
VCC1	I	Power Supply
GND	I	Ground
$\overline{SE}$	I	Servo Enable: A low input on this line enables the Servo Bank Write mode when $\overline{CS}$ and R/$\overline{W}$ are both low.
WUS/SE	I	Write Unsafe/Servo Enable: Under normal operation, a high level output on this pin indicates a write unsafe condition. When this pin is driven externally above VCC and $\overline{CS}$ and R/$\overline{W}$ are both low, servo Write mode is activated.
DMP	I	Damping Resistor Enable: A high (or open) level on this input enables the switchable damping resistor. A low level on this input disables the damping resistor.

†When more that one R/W device is used, signals can be wire OR'ed

WRITE MODE

Taking both $\overline{CS}$ and R/$\overline{W}$ low selects Write mode which configures the device as a current switch and activates the Write Unsafe (WUS) detector circuitry. Head current is toggled between the X and Y side of the selected head on each high to low transition of the Write Data Input (WDI). Note that a preceding Read to Write transition or Idle to Write transition initializes the Write Data Flip-Flop to pass write current into the "X" side of the device. In this case, the Y side is higher potential than the X side. The magnitude of the write current (0-pk) is given by:

$$Iw = Aw \cdot \frac{Vwc}{Rwc} = K/Rwc$$

where Aw is the write current gain.
RWC is connected from pin WC to GND. Note the actual head current Ix, y is given by:

$$Ix, y = \frac{Iw}{1 + Rh/Rd}$$

where:

Rh = Head resistance plus external wire resistance
Rd = Damping resistance

In Write mode a 350Ω damping resistor is switched in across the Hx, Hy ports.

VOLTAGE FAULT

A voltage Fault detection circuit improves data security by disabling the write current generator during a voltage fault or power startup in Read or Write mode.

WRITE UNSAFE

Any of the following conditions will be indicated as a high level on the Write Unsafe, WUS, open collector output.

- WDI frequency too low
- Device in Read mode
- Device not selected
- Open head
- Head short to ground

WUS is valid in the write current/head characteristic region defined by 5 < Ih • Lh < 50 mA • µH, and 1 < Rh < 1.25/Ih. After the fault condition is removed, one negative transition on WDI is required to clear WUS.

READ MODE

The Read mode configures the SSI 32R2420 as a low noise differential amplifier and deactivates the write current generator. The damping resistor is switched out of the circuit allowing a high impedance input to the read amplifier. The RDX and RDY output are driven by emitter followers. They should be AC coupled to the load. The HnX, HnY inputs are non-inverting to the RDX, RDY outputs.

Note that in Idle or Write mode, the read amplifier is deactivated and RDX, RDY outputs become high impedance. This facilitates multiple R/W applications (wired-OR RDX, RDY) and minimizes voltage change when switching from Write to Read mode. Note also that the write current source is deactivated for both the Read and Idle mode.

IDLE MODE

Taking $\overline{CS}$ high selects the Idle mode which switches the RDX and RDY outputs into a high impedance state and deactivates the device. Power consumption in this mode is held to a minimum.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may permanently damage the device.

PARAMETER		RATING
DC Supply Voltage	VCC1	-0.3 to +7 VDC
	VCC2	-0.3 to +7 VDC
Write Current	Iw	30 mA
Digital Input Voltage	Vin	-0.3 to VCC1 +0.3 VDC
Head Port Voltage	VH	-0.3 to VCC2 +0.3 VDC
Output Current: RDX, RDY	Io	-10 mA
	WUS	+8 mA
Storage Temperature	Tstg	-55 to +150°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	RATING
DC Supply Voltage	5.0 ±10% VDC
Recommended Head Load Range Lh	0.3 - 5.0 µH
WUS Operating Range Iw • Lh	5.0 - 50.0 mA • µH
Head Differential Load Capacitance	15 pF max
Ambient Operating Temperature*	0 - 70 °C

* Derating is required when in Servo Write mode.

DC CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VCC1 Supply Current	Read		23.0	32.0	mA
	Write		6 + 1.2 • Iw	10 + 1.3 • Iw	mA
	Servo		7 + 4.4 • Iw	12 + 4.7 • Iw	mA
	Idle, $\overline{CS}$ = Vcc		5	30	µA
	Idle, $\overline{CS}$ = 2.7V		250	450	µA
Power Dissipation	Read		115	180	mW
	Write		30 + 6 • Iw	55 + 7 • Iw	mW
	Servo		35 + 22 • Iw	66 + 26 • Iw	mW
	Idle, $\overline{CS}$ = 2.7V		1.25	2.5	mW
	Idle, $\overline{CS}$ = Vcc		0.03	0.17	mW

DIGITAL INPUTS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Input Low voltage (VIL)				0.8	VDC
Input High Voltage (VIH)		2.0			VDC
Input Low Current	VIL = 0.4	-0.4	-0.13		mA
Input High Current	VIH = 2.7V		0	20	µA
WUS Output Low Voltage (VOL)	Iol = 2 mA max		.35	0.5	VDC

WRITE CHARACTERISTICS

Recommended operating conditions apply unless otherwise specirfied.

VCC1 Fault Voltage	Iw < 0.2 mA		2.5	2.75	VDC
Write Current Gain (Aw)	Iw = 2-5 mA	20.6	23.1	28.0	mA/mA
	Iw = 5-30 mA	19.3	21.7	24.5	mA/mA
Write Current Error	Rwc = 2 kΩ, head to head @ Write mode	-5		+5	%
	Rwc = 2 kΩ, head to head @ Servo mode	-5		+5	%
	Rwc = 2 kΩ, Write to Servo	-7		+7	%
Write Current Voltage (Vwc)		1.2	1.3	1.4	V
Differential Head Voltage Swing	Open head, $\overline{SE}$ = 1	4.0	4.8		Vpp
	Open head, Vcc = 5V, $\overline{SE}$ = 0	4.0	4.8		Vpp
Unselected Head Current	AC			1.0 Iw	mA (pk)
	DC			0.1	mA
Head Differential Load	R version	300	400	500	Ω
Resistance (Rd)	Non-R version	2400	3000	3600	Ω
WDI Pulse Width	Vil ≤ 0.8V, Vih ≥ 2.0V PWH	5			ns
	$t_f = t_r$ = 1ns PWL	10			ns
Write Current Range (Iw)		2		30	mA

READ CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified. CL (RDX, RDY) < 20 pF, RL (RDX, RDY) = 1 kΩ.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Differential Voltage Gain	Vin = 1 mVpp @1 MHz	200	250	300	V/V
Voltage BW -1 dB	|Zs| < 5Ω, Vin = 1 mVpp	20	45		MHz
-3 dB		40	70		MHz
Input Noise Voltage	BW = 15 MHz, Lh = 0, Rh = 0		0.50	0.75	nV/√Hz
Input Noise Current			3		pA/√Hz
Differential Input Capacitance	Vin = 1 mVpp, f = 5 MHz		9	14	pF
Differential Input Resistance	Vin = 1 mVpp, f = 5 MHz	500	750	1800	Ω
Dynamic Range	AC input voltage where gain falls to 90% of its small signal gain value, f = 5 MHz	2	5		mVpp
Common Mode Rejection Ratio	Vin = 0 VDC + 100 mVpp @ 5 MHz	45	60		dB
Power Supply Rejection Ratio	100 mVpp @ 5 MHz on VCC	40	70		dB
Channel Separation	Unselected channels driven with Vin = 0 VDC + 100 mVpp	45	60		dB
Output Offset Voltage	Head shorted	-250		+250	mV
	Head opened	-300		+300	mV
Single Ended Output Resistance	f = 5 MHz		60	100	Ω
Output Current	AC coupled load, RDX to RDY	1.0	2.0		mA
RDX, RDY Common Mode Output Voltage		Vcc - 1.0	Vcc - 1.35	Vcc - 1.70	VDC

SWITCHING CHARACTERISTICS

Recommended operating conditions apply unless otherwise specified. Rwc = 2 kΩ, Lh = 1.0 µH, Rh = 30Ω f(Data) = 5 MHz.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
R/$\overline{W}$	Read to Write	R/$\overline{W}$ to 90% of write current; WUS valid		0.3	1.0	µs
	Write to Read	R/$\overline{W}$ to 90% of 100 mV Read signal envelope		0.4	1	µs
$\overline{CS}$	Unselect to Select	$\overline{CS}$ to 90% of 100 mV 10 MHz Read signal envelope		0.6	2	µs
	Select to Unselect	$\overline{CS}$ to 10% of write current		0.4	1	µs
HS0,1 to any Head		To 90% of 100 mV 10 MHz Read signal envelope		0.2	1	µs
WUS*	Safe to Unsafe (TD1)	Write mode, loss of WDI transitions; Defines max WDI period for WUS operation	0.6	2.0	3.6	µs
	Unsafe to Safe (TD2)	Fault cleared: from first negative WDI transition		0.2	1.0	µs
WDI	Frequency Range	Valid WUS	1.67		25	MHz
Head Current		Lh = 0, Rh = 0		25	40	ns
	WDI to Ix - Iy (TD3)	from 50% points				
	Asymmetry	WDI has 1 ns rise/fall time			1.5	ns
	Rise/fall Time	10% to 90% points Rwc = 2 kΩ, Rh = 0, Lh = 0		2	9	ns
		Rwc = 2 kΩ, Rh = 30Ω, Lh = 1µH		14	18	ns

* 5 < Iw • Lh < 50 mA • µH, 1 < Rh ≤ 1.25/Iw, WUS available in bonding option.

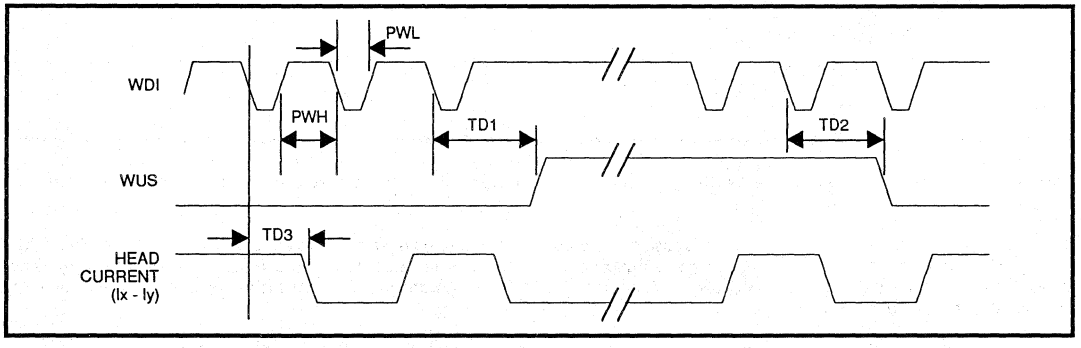
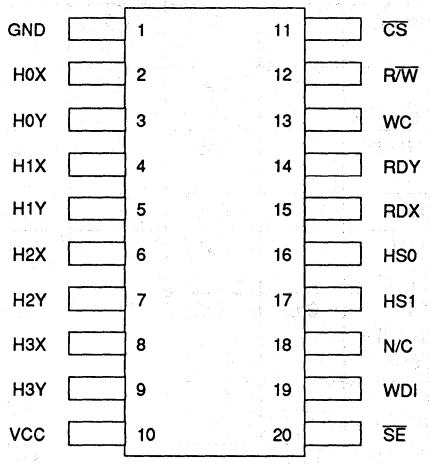


FIGURE 1: Write Mode Timing Diagram

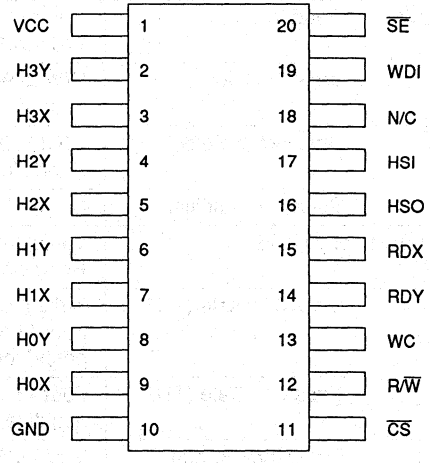
SSI 32R2420
5V, 4-Channel
2-Terminal Read/Write Device

PACKAGE PIN DESIGNATIONS
(Top View)



20-Lead VSOP

32R2420RW-4CV (VSOP)
32R2420W-4CV (VSOP)



20-Lead VSOP (Inverted)

32R2420RIW-4CV
32R2420IW-4CV

CAUTION: Use handling procedures necessary for a static sensitive component.

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914

Section 4

DISCRETE CHANNEL

silicon systems®
A TDK Group Company

SSI 32D5396/5396A

Data Sync/1, 7 RLL ENDEC with Write Precomp. and Window Shift

Advance Information

October 1993

DESCRIPTION

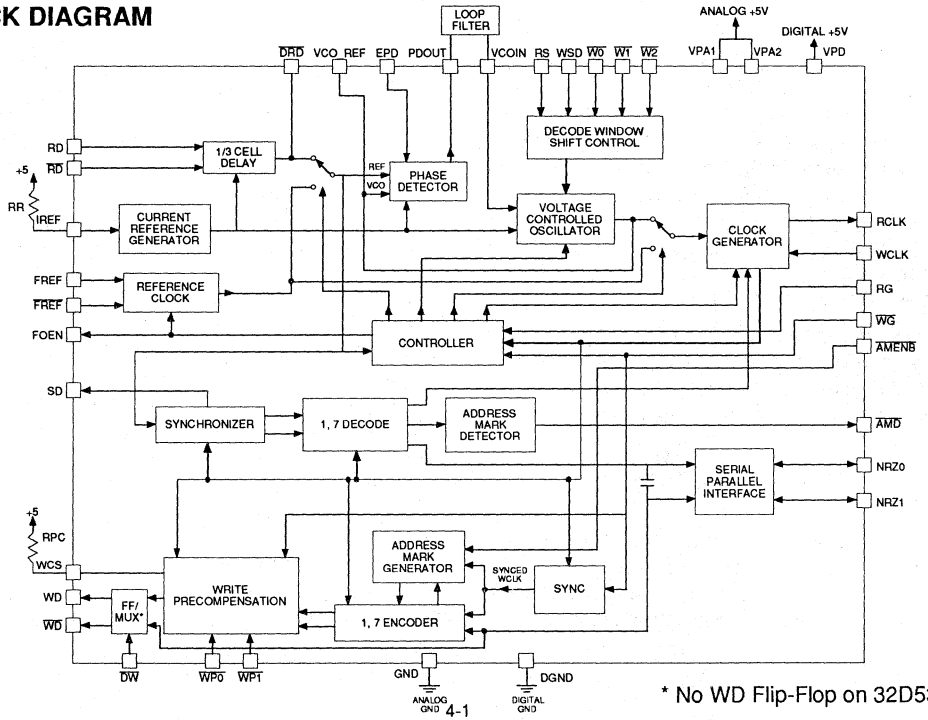
The SSI 32D5396/96A Data Synchronizer/1, 7 RLL ENDEC provides data recovery and data encoding for storage systems which employ a 1, 7 RLL encoding format. Data synchronization is performed with a fully integrated high performance PLL. A zero phase restart technique is used to minimize PLL acquisition time. The VCO frequency setting elements are incorporated within the SSI 32D5396/96A for enhanced performance and reduced board space. Data rate is established with a single external programming resistor. The SSI 32D5396/96A utilizes an advanced bipolar process technology which affords precise decode window control without the requirement of external devices. The SSI 32D5396/96A requires a single +5V supply and is available in 44-Pin PLCC and 36-Lead SOM packages.

FEATURES

- **Data synchronizer and 1, 7 RLL ENDEC**
- **Dual bit NRZ bus**
- **24 to 54 Mbit/s operation**
  - **Data rate programmed with a single external resistor or current source**
- **Fast acquisition phase locked loop with improved zero phase restart technique**
- **Fully integrated data separator**
  - **No external delay lines or active devices required**
- **Programmable decode window symmetry control**
  - **Includes delayed read data and VCO clock monitor points**
- **Programmable write precompensation**
- **Hard and soft sector operation**
- **Uses standard 5V ± 5% supply**

4

BLOCK DIAGRAM



* No WD Flip-Flop on 32D5396A

FUNCTIONAL DESCRIPTION

DATA/CLOCK RECOVERY CIRCUIT

The circuit is designed to perform data recovery and data encoding in rotating memory systems which utilize a 1, 7 RLL encoding format. In the read mode the circuit performs data synchronization, sync field search and detect, address mark detect, and data decoding. In the write mode, the circuit converts NRZ data into the 1, 7 RLL format described in Table 1, performs write precompensation, generates the preamble field and inserts address marks as requested.

This data rate is established by a single 1% external resistor, RR, connected from the IREF pin to VPA. This resistor establishes a reference current which sets the VCO center frequency and the phase detector gain. The value of this resistor is given by:

$$RR = (185/DR) - 1.7\ k\Omega$$

Where: DR = data rate in Mbit/s

Alternately, the IREF pin can be driven from the SSI 32D4666 in a constant density recording application.

$$IREF\ (mA) = \frac{4.3}{185/DR - 117}$$

The circuit employs a dual mode phase detector; harmonic in the read mode and non-harmonic in the write and idle modes. In the read mode, the harmonic phase detector updates the PLL with each occurrence of a DLYD DATA pulse. In the write and idle modes, the non-harmonic phase detector is continuously enabled, thus maintaining both phase and frequency lock. By acquiring both phase and frequency lock to the input reference frequency and utilizing a zero phase restart technique, false lock to DLYD DATA is eliminated.

The phase detector incorporates a charge pump in order to drive the loop filter directly. The polarity and width of the output current pulses correspond to the direction and magnitude of the phase error.

The READ GATE (RG) and WRITE GATE ($\overline{WG}$) inputs control the mode of the data/clock recovery section of the chip.

RG is an asynchronous input that should be initiated at the start of a valid preamble or address mark. $\overline{WG}$ is also an asynchronous input, but should not be terminated prior to the last output write data pulse.

READ OPERATION

The data synchronizer utilizes a fully integrated fast acquisition PLL to accurately develop the decode window. Read Gate, RG, initiates the PLL locking sequence and selects the PLL reference input; a high level (Read Mode) selects the RD input and a low level selects the external reference clock.

In the read mode the falling edge of $\overline{DRD}$ enables the phase detector while the rising edge is phase compared to the rising edge of VCO. As depicted in Figure 1, $\overline{DRD}$ is a 1/3 cell wide (TVCO/2) pulse whose leading edge is defined by the leading edge of RD. A decode window is developed from the VCO clock.

Shifting the symmetry of the VCO clock effectively shifts the relative position of the $\overline{DRD}$ pulse within the decode window. Decode window control is provided via the WS controls.

In the non-read modes, the PLL is locked to the external reference clock. When the reference input to the PLL is switched, the VCO is stopped momentarily, then restarted in an accurate phase alignment with the next PLL reference input pulse, and the VCO clock divider is reset.

ADDRESS MARK DETECT

In soft sector read operation the circuit must first detect an address mark to be able to initiate the rest of the read lock sequence. An address mark consists of two sets of 7 "0" patterns followed by two sets of 11 "0" patterns. To begin the read lock sequence the Address Mark Enable ($\overline{AMENB}$) is asserted low by the controller. The address mark detect ($\overline{AMD}$) circuit then initiates a search of the read data (RD) for an address mark. First the $\overline{AMD}$ looks for a set of 6 "0"s within the 7 "0" patterns. Having detected a 6 "0" the $\overline{AMD}$ then looks for a 9 "0" set within the 11 "0"s. If $\overline{AMD}$ does not detect 9 "0"s within 5 RD bits after detecting 6 "0"s it will restart the address mark detect sequence and look for 6 "0"s. When the $\overline{AMD}$ has acquired a 6 "0," 9 "0" sequence, the $\overline{AMD}$ transitions low. $\overline{AMD}$ will remain low for the duration of $\overline{AMENB}$. When $\overline{AMENB}$ is released, $\overline{AMD}$ will be released.

PREAMBLE SEARCH

After the Address Mark (AM) has been detected, a Read Gate (RG) can be asserted high, initiating the remainder of the read lock sequence. When RG is asserted, an internal counter counts positive transi-

tions of the incoming read data (RD) looking for 3 consecutive "3T" preambles. Once the counter reaches count 3 the internal read gate enables, switching the phase detector from the external reference clock to the delayed read data input ($\overline{DRD}$); at the same time a zero phase (internal) restart signal restarts the VCO in phase with the $\overline{DRD}$. This prepares the VCO to be synchronized to data when the bit sync circuitry is enabled after VCO lock is established.

VCO LOCK AND BIT SYNC ENABLE

When the internal counter counts 16 more data pulses or a total of 19 positive transitions from RG enable, an internal VCO lock signal enables. The VCO lock signal activates the decoder bit synchronization circuitry to define the proper decode boundaries. Also, at count 19, the internal RCLK source switches from the external reference clock to VCO clock signal which is phase locked to $\overline{DRD}$. The VCO is assumed locked at this point. A maximum of 2 RCLK time periods may occur for the RCLK transition, however, no short duration glitches will occur. After the bit sync circuitry sets the proper decode window (VCO in sync with RCLK and RCLK in sync with the data) NRZ is enabled and data is toggled in to be decoded for the duration of the read gate.

HARD SECTOR OPERATION

In hard sector operation, a high $\overline{AMENB}$ disables the Address Mark Detection circuitry and $\overline{AMD}$ remains inactive. A hard sector read operation does not require an address mark search but starts with a preamble search as with soft sector and sequences identically. In all respects, with exception to the address mark search sequence, hard sector read operation is the same as soft sector read.

WRITE MODE

In the write mode the circuit converts NRZ data from the controller into 1, 7 RLL formatted data for storage on the disk. The circuit can operate with a soft or hard sector hard drive.

In soft sector operation the circuit generates a "7, 7, 11, 11" address mark and a preamble pattern ("3T's"). In hard sector operation the circuit generates a 19 x "3T" preamble pattern but no preceding address mark.

NRZ data is clocked into the circuit and latched on defined cell boundaries. The NRZ input data must be synchronous with the rising edges of the WCLK.

Write precompensation circuitry is provided to compensate for media bit shift caused by intersymbol interference. The circuit recognizes specific write data patterns and can add or subtract delays in the time position of write data bits to counteract the read back bit shift. The magnitude of the time shift, TPC, is determined by an external resistor on the WCS pin. The circuit performs write precompensation according to the algorithm outlined in Table 4.

The SSI 32D5396 includes an internal write data flip-flop that divides the WD frequency by 2. The SSI 32D5396A does not include the WD flip-flop, so this device must be used with a preamp that includes a WD flip-flop.

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SOFT SECTOR

In soft sector operation, when read gate (RG) transitions low, VCO source and RCLK source switch from RD and 2VCO/3, respectively, to the external reference clock. At the same time the VCO (internal) lock goes inactive but the VCO is locked to the external reference clock. After delay of 1 NRZ time period (min) from RG low, the write gate ($\overline{WG}$) can be enabled low while NRZ is maintained (NRZ write data) low. The address mark enable ($\overline{AMENB}$) is made active (low) a minimum of 1 NRZ time period later. The address mark (consisting of 7 "0"s, 7 "0"s, 11 "0"s, 11 "0"s) and the 19 x "3T" preamble is then written by WD. While the preamble is being written, WCLK is clocking in an all "0" NRZ bit pair. At the end of the write cycle, 8 WCLK cycles of NRZ "0" time passes to insure the encoder is flushed of data; $\overline{WG}$ then goes high. WD stops toggling a maximum of 1 NRZ time periods after $\overline{WG}$ goes high.

HARD SECTOR

In hard sector operation, when read gate (RG) transitions low, VCO source and RCLK switch references and VCO lock (internal) goes inactive as with soft sector but the $\overline{AMENB}$ (Address Mark Enable) is kept high.

The circuit then sequences from RG disable to $\overline{WG}$ enable and NRZ active as in soft sector operation.

TEST POINTS

The SSI 32D5396 provides two (2) test points which can be utilized to evaluate window margin characteristics.

(a) $\overline{\text{DRD}}$, delayed read data – the positive edges represent the data bit position

(b) VCO REF, the VCO reference which represents the input to the Phase Detector, synchronizer, and 1,7 decoder

The following figure describes the relationship between the various test points:

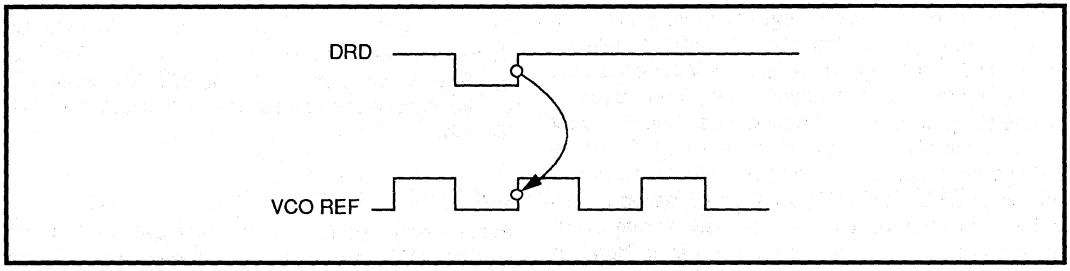


FIGURE 1: Test Point Relationships

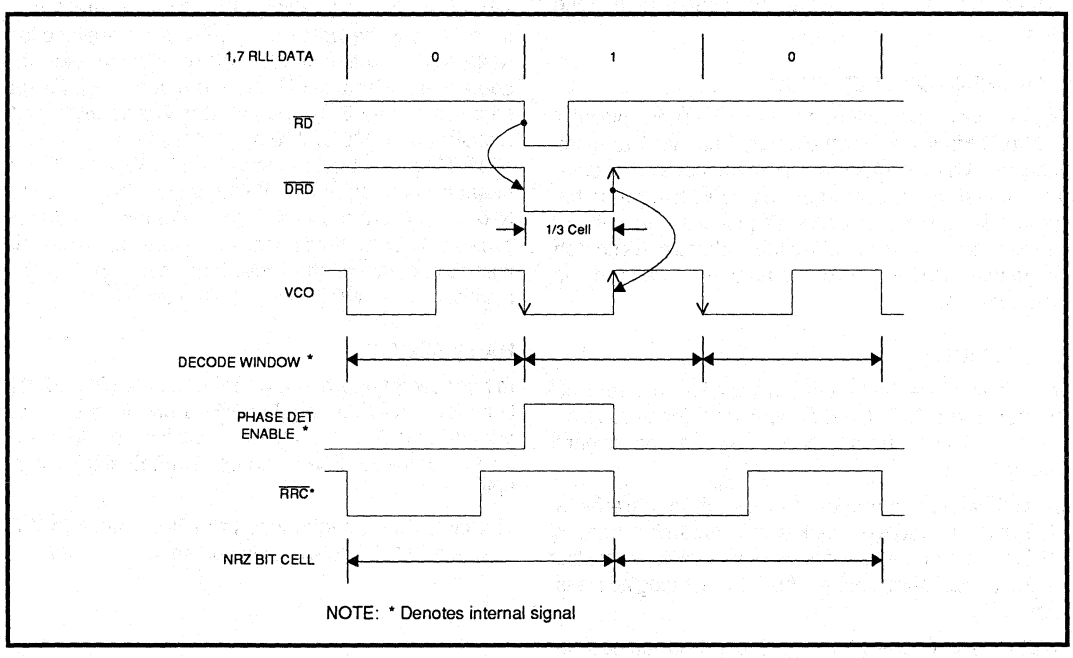


FIGURE 2: Data Synchronization Waveform

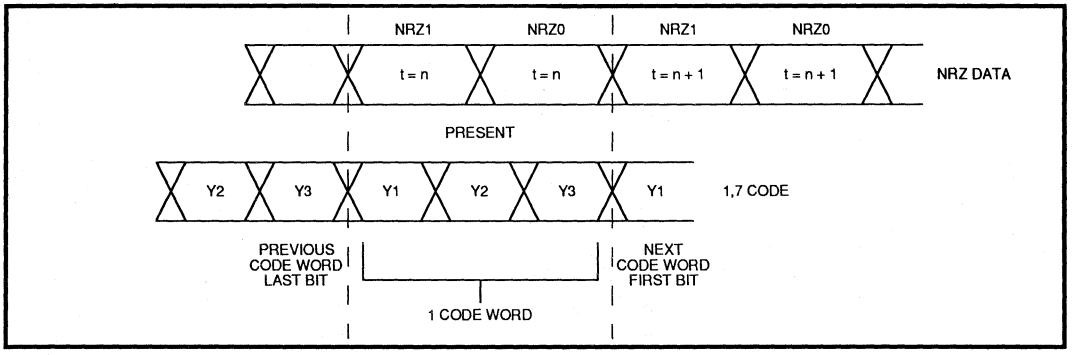


FIGURE 3: NRZ Data Word Comparision to 1, 7 Code Word (See Tables 1, and 2 for Decode Scheme)

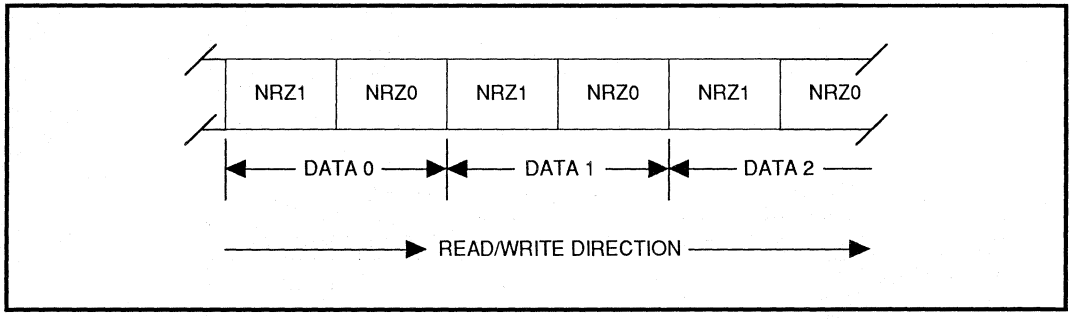


FIGURE 4: Parallel/Serial Conversion Format

TABLE 1: Decode Table for (1, 7) RLL Code Set

ENCODED READ DATA						DECODED DATA		
Previous		Present			Next			
Y	Y	Y	Y	Y	Y	NRZ	NRZ	
2'	3'	1	2	3	1	2	1	0	
0	0	0	0	0	X	X	0	1	
1	0	0	0	0	X	X	0	0	
0	1	0	0	0	X	X	0	1	
X	X	1	0	0	X	X	1	1	
X	0	0	1	0	0	0	1	1	
X	0	0	1	0	1	0	1	0	
X	0	0	1	0	0	1	1	0	
X	1	0	1	0	0	0	0	1	
X	1	0	1	0	1	0	0	0	
X	1	0	1	0	0	1	0	0	
0	0	0	0	1	X	X	0	1	
1	0	0	0	1	X	X	0	0	
0	1	0	0	1	X	X	0	0	(Preamble)
X	X	1	0	1	X	X	1	0	

TABLE 2: Encode Table for (1, 7) RLL Code Set

NRZ DATA				ENCODED WRITE DATA			
Present		Next		Previous	Present		
NRZ	NRZ	NRZ	NRZ	Y	Y	Y	Y
1	0	1	0	3	1	2	3
0	0	0	X	X	0	0	1
0	0	1	X	0	0	0	0
0	0	1	X	1	0	1	0
1	0	0	X	0	1	0	1
1	0	1	X	0	0	1	0
0	1	0	0	0	0	0	1
0	1	0	0	1	0	1	0
0	1	1	0	0	0	0	0
0	1	1	0	1	0	0	0
0	1	0	1	0	0	0	1
0	1	0	1	1	0	0	0
0	1	1	1	0	0	0	0
0	1	1	1	1	0	0	0
1	1	0	0	0	0	1	0
1	1	1	0	0	1	0	0
1	1	0	1	0	1	0	0
1	1	1	1	0	1	0	0

NOTE: X = Don't Care

TABLE 3: Clock Frequency

$\overline{WG}$	RG	VCO REF	RCLK	DECCLK	ENCCLK	MODE
1	0	FREF	FREF/3	N/A	N/A	IDLE
1	1	RD	VCO/3	VCO	FREF	READ
0	0	FREF	FREF/3	FREF	FREF	WRITE
0	1	Undefined	Undefined	Undefined	Undefined	Undefined

Note 1: Until the VCO locks to the new source, the VCO entries will be FREF.

2: Until the VCO locks to the new source, the VCO/3 entries will be FREF/3.

4

TABLE 4: Write Precompensation Algorithm

BIT	BIT	BIT	BIT	BIT	COMPENSATION
n-2	n-1	n	n+1	n+2	BIT n
1	0	1	0	1	NONE
0	0	1	0	0	NONE
1	0	1	0	0	EARLY
0	0	1	0	1	LATE

LATE: Bit n is time shifted (delayed) from its nominal time position towards the bit n+1 time position.

EARLY: Bit n is time shifted (advanced) from its nominal time position towards the bit n-1 time position.

TABLE 5: Write Precompensation Magnitude

$\overline{WP1}$	$\overline{WP0}$	MAGNITUDE (WP)
0	0	3
0	1	2
1	0	1
1	1	0

TPC = WP x TPC0
The nominal magnitude,TPC0 is externally set with a resistor on pin WCS.

TABLE 6: Window Shift Direction

WSD	DIRECTION
0	Early window (+TS)
1	Late window (-TS)

TABLE 7: Window Shift Magnitude

$\overline{W2}$	$\overline{W1}$	$\overline{W0}$	MAGNITUDE (TS0)
1	1	1	No shift
1	1	0	4% Minimum shift
1	0	1	8%
1	0	0	12%
0	1	1	15%
0	1	0	18%
0	0	1	20%
0	0	0	22% Maximum shift
With resistor, RRS, connected between pins RS and VPA: TS = TS0 [RRS/(RRS + 0.8)] 2kΩ < RRS			

PIN DESCRIPTION

INPUT PINS

NAME	TYPE	DESCRIPTION
VPA1, VPA2	I	5 volt analog power supply pins
VPD	I	5 volt digital power supply pin
AGND	-	Analog ground pin
DGND	-	Digital ground pin
$\overline{AMENB}$	I	ADDRESS MARK ENABLE. Used to enable the address mark detection and address mark generation circuitry. Active low TTL input levels.
DW	I	DIRECT WRITE ENABLE. Used to enable the direct write mode. A high level allows normal write operation. A low level enables the encoder bypass path mode. In this bypass mode, NRZ0 will directly clock the WD Flip-Flop while $\overline{WG}$ = 0. Pin $\overline{DW}$ has an internal pull up resistor. TTL input levels.
EPD	I	ENABLE PHASE DETECTOR. A low level (coast mode) disables the phase detector and enables the Test Mode. This opens the PLL and the VCO will run at the frequency commanded by the voltage on the VCO IN pin. (In the Test Mode, functions normally driven by the VCO are switched to FREF.) Pin EPD has an internal pull-up resistor. TTL input levels.
FREF/$\overline{FREF}$	I	REFERENCE FREQUENCY INPUT. The input frequency is at one and one-half times the data rate. FREF/$\overline{FREF}$ should be driven by direct coupled differential PECL signals.
RD, $\overline{RD}$	I	READ DATA. Encoded Read Data from the disk drive read channel. Differential +5 volts offset ECL (PECL) input levels.

INPUT PINS (continued)

NAME	TYPE	DESCRIPTION
RG	I	READ GATE. Selects the PLL reference input and initiates the PLL synchronization sequence. A high level selects the RD input and enables the read mode/address detect sequences. A low level selects the XTAL input. See Table 2. TTL input levels.
$\overline{W0}$, $\overline{W1}$, $\overline{W2}$	I	WINDOW CONTROL BITS. In Read Mode, pins $\overline{W0}$ and $\overline{W1}$ and $\overline{W2}$ control the magnitude of the decode window shift. Each pin has an internal pull-up resistor. TTL input levels.
WCLK	I	WRITE CLOCK. Write mode dual-bit clock. Must be synchronous with the NRZ input. For short cable delays, WCLK may be connected directly to pin RCLK. For long cable delays, WCLK should be connected to an RCLK return line matched to the NRZ data bus line delay. TTL input levels.
$\overline{WP0}$,$\overline{WP1}$	I	WRITE PRECOMPENSATION CONTROL BITS. In Write Mode, pins $\overline{WP0}$ and $\overline{WP1}$ control the magnitude of the write precompensation. Each pin has an internal pull-up resistor. TTL input levels.
$\overline{WG}$	I	WRITE GATE. Enables the write mode. See Table 2. Active low TTL input levels.
WSD	I	WINDOW SYMMETRY DIRECTION CONTROL. Controls the direction of the decode window shift. Pin WSD has an internal pull-up resistor. TTL input levels.

OUTPUT PINS

$\overline{AMD}$	O	ADDRESS MARK DETECT. Tristate output pin that is in its high impedance state when $\overline{WG}$ is low or $\overline{AMENB}$ is high. When $\overline{AMENB}$ is low, this output indicates address mark search status. A latched low level output appears when an address mark has been detected. A high level on pin $\overline{AMENB}$ resets pin $\overline{AMD}$. TTL output levels.
$\overline{DRD}$	O	DELAYED READ DATA. An open emitter ECL output test point. The positive edges of this signal indicate the data bit position. The positive edges of the $\overline{DRD}$ and VCO_REF outputs can be used to estimate window centering. The time jitter of DRD's positive edge is an indication of media bit jitter. Two external resistors are required to use this pin. They should be removed during normal operation to reduce power dissipation.
FOEN	O	REFERENCE CLOCK ENABLE. When this output is high, the FREF clock is controlling the internal timing. When this output is low, the FREF clock is internally disabled. The output from pin FOEN can be used to disable the clock applied to the FREF pin to reduce VCO jitter during read modes. TTL output levels.
RCLK	O	READ CLOCK. A multiplexed dual-bit clock source used by the controller, see Table 2. During a mode change, no glitches are generated and no more than one lost clock pulse will occur. When RG goes high, RCLK initially remains synchronized to FREF/3. After 19 read data pulses, RCLK is synchronized to the Read Data. When RG goes low, RCLK is synchronized back to the FREF/3. TTL output levels.

PIN DESCRIPTION (continued)

OUTPUT PINS (continued)

NAME	TYPE	DESCRIPTION
SD	O	SYNCHRONIZED DATA. An open emitter PECL output test point. Synchronized data before the decoder. Two external resistors are required to use this pin. They should be removed during normal operation to reduce power dissipation.
VCO REF	O	VCO REFERENCE. An open emitter PECL output test point. This is the VCO reference input to the phase detector. The positive edges are phase locked to Delayed Read Data. The negative edges of this open emitter output signal indicate the edges of the decode window. Two external resistors are required to use this pin. They should be removed during normal operation to reduce power dissipation.
WD, WD	O	WRITE DATA. Encoded write data output. The data is automatically resynchronized (independent of the delay between RRC and WCLK) to the FREF reference clock. Differential PECL output levels. Termination resistors are required.

BIDIRECTIONAL PINS

NRZ0, NRZ1	B	NRZ READ DATA PORT. Dual-bit port. Read data output when RG is high, Write data input when WG is low. TTL input and output levels.

ANALOG PINS

IREF	I	CURRENT REFERENCE INPUT. The VCO center frequency, the 1/3 cell delay, and the phase detector gain are a function of the current sourced into this pin.
PD OUT	O	PHASE DETECTOR OUTPUT. Drives the loop filter input.
RS	I	WINDOW SYMMETRY ADJUST PIN. This pin allows analog adjustment of the decode window shift magnitude. Used in conjunction with the digital controls W) and W! and W@ this pin can be used to scale the magnitude of the preset window shift. Connect resistor to VPA.
VCO IN	I	VCO CONTROL INPUT. Driven by the loop filter output.
WCS	I	WRITE PRECOMPENSATION SET. Pin for the reference current to set the write precompensation magnitude value. Connect resistor to VPA.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may damage the device.

PARAMETER	RATING
Supply Voltage, VPA1, VPA2, VPD	-0.3 to 6V
Storage Temperature	-65 to 150 °C
Lead Temperature (Soldering 10 sec.) FOEN,NRZ, WD, $\overline{WD}$, $\overline{AMD}$, $\overline{DRD}$,	260 °C
VCOREF pins All other pins	-0.3 to (VPA/VPD+0.3)V or +12 mA -0.3 to (VPA/VPD+0.3)V

RECOMMENDED OPERATING CONDITIONS

Supply Voltage, VPA1 = VPA2 = VPD = VCC	4.75 < VCC < 5.25V
Junction Temperature, Tj	0 < Tj < 135 °C
Ambient Temperature, Ta	0 < Ta < 70 °C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, 4.75 < VPA/VPD < 5.25, 0°C < T(ambient) < 70 °C, 25 °C < T(junction) < 135 °C. Currents flowing into the chip are positive. Current maximums are currents with the highest absolute value.

POWER SUPPLY CURRENTS AND POWER

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
ICC (VPA, VPD) Supply Current	Outputs and test point pins open, Ta = 70 °C		180		mA
PWR Power Dissipation	Outputs and test point pins open, Ta = 70 °C		0.9		W

DIGITAL INPUTS AND OUTPUTS

TTL Compatible Inputs: $\overline{AMENB}$, EPD, $\overline{DW}$, RG, $\overline{W0}$, $\overline{W1}$, $\overline{W2}$, WCLK, $\overline{WG}$, $\overline{WP0}$, $\overline{WP1}$, NRZ0, NRZ1, WSD Pins

Input Low Voltage (VIL)		-0.3		0.8	V
Input High Voltage (VIH)		2.0		VPD+0.3	V
Input Low Current	VIL = 0.4 V	0.0		-0.4	mA
Input High Current	VIH = 2.4 V			100	µA

DIGITAL INPUTS AND OUTPUTS (continued)

TTL Compatible Outputs: $\overline{AMD}$, FOEN, NRZ0, NRZ1, RCLK pins

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Output Low Voltage	Iol = 4.0 mA			0.5	V
Output High Voltage	Ioh= -400µA	2.4			V

Digital Differential Inputs: RD, $\overline{RD}$, FREF, $\overline{FREF}$ pins

Input Low Voltage (VIL)		VPA-2.2		VIH-0.5	V
Input High Voltage (VIH)		VIL+0.5		VPA-0.5	V
Differential Voltage	$\lvert V_{RD} - \overline{V}_{\overline{RD}} \rvert$	0.5			V
Input Low Current	VIL = Min	-100			µA
Input High Current	VIH = Max			+100	µA

Digital Differential Outputs: WD, $\overline{WD}$ pins

Output Low Voltage	Iol = TBD	VPD-2.1			V
Output High Voltage	Ioh = TBD			VPD-0.7	V
Differential Voltage	$\lvert V_{WD} - \overline{V}_{\overline{WD}} \rvert$	0.5			V

Test Point Output Levels

Test Point Output High Level (DRD, VCOREF)	262Ω to VPA, 402Ω to GND, VPA = 5V		VPA -1.02		V
Test Point Output Low Level (DRD,VCOREF)	262Ω to VPA, 402Ω to GND, VPA = 5V			VPA -1.625	V

DYNAMIC CHARACTERISTICS AND TIMING

READ MODE (See Figure 5)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Read Data Pulse Width (TPRD)		8		(2)TVCO -8	ns
Read Data Rise Time (TRRD)	20% to 80%, CL ≤ 10 pF			5	ns
Read Data Fall Time (TFRD)	80% to 20%, CL ≤ 10 pF			5	ns
Read Clock Rise Time (TRRC)	0.8V to 2.0V, CL ≤ 15 pF			5	ns
Read Clock Fall Time (TFRC)	2.0V to 0.8V, CL ≤ 15 pF			5	ns
NRZ (out) Set Up & Hold Time (TDS, TDH)		10			ns
RCLK Low Time (TLRC)	0.8V, CL ≤ 15 pF	13			ns
RCLK High Time (THRC)	2.0V, CL ≤ 15 pF	15			ns
$\overline{AMD}$ Set Up & Hold Time (TAS, TAH)		13			ns
RRC re-sync period (Tdc2)		TORC		(2)TORC	ns
Decode Window Centering Accuracy				±0.75	ns
Decode Window		TVCO -0.75			ns

WRITE MODE (See Figure 6)

Write Data Rise Time (TRWD)	20% to 80% Points 110Ω to VPD, 160Ω to DGND			5	ns
Write Data Fall Time (TFWD)	80% to 20% Points 110Ω to VPD, 160Ω to DGND			5	ns
Write Data Clock Rise Time (TRWC) CL ≤ 15 pF	0.8V to 2.0V,			10	ns
Write Data Clock Fall Time (TFWC) CL ≤ 15 pF	2.0V to 0.8V,			8	ns
NRZ Set Up Time (TSNRZ)		5			ns
NRZ Hold Time (THNRZ)		5			ns
Precompensation Time Shift Magnitude Accuracy (TPC)	TPCO = 0.22 (Rc + 0.53) Rc min=1 kΩ, TPC max=0.3TFREF				
	$\overline{W0}$ = 1, $\overline{W1}$ =1	-0.5		0.5	ns
	$\overline{W0}$ = 0, $\overline{W1}$ =1		TPCO		ns
	$\overline{W0}$ = 1, $\overline{W1}$ =0		2TPCO		ns
	$\overline{W0}$ = 0, $\overline{W1}$ =0		3TPCO		ns

DATA SYNCHRONIZATION

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VCO Center Frequency Period (TVCO)	VCO IN=2.7V, VPA=VPD=5V TO=3.6 (RR+1.7), RR=(185/DR)-1.7K	0.8TO		1.2TO	ns
VCO Frequency Dynamic Range	1.0 V ≤ VCO IN ≤ VPA - 0.6V VPA=VPD = 5 V	± 25		± 45	%
VCO Control Gain (KVCO)	wo = 2π/TVCO 1.0 V ≤ VCO IN ≤ VPA - 0.6V	0.14 wo		0.26 wo	rad/s V
Phase Detector Gain (KD)	VPA = VPD = 5V Read: KD = 660/(RR+0.53) PLL REF = $\overline{RD}$, 1T Pattern Non-Read: KD = 330/(RR+0.53)	0.83KD		1.17KD	µA/rad
KVCO x KD Product Accuracy		0		±28	%
VCO Phase Restart Error	Referred to RRC	0		±1	rad
1/3 Cell Delay	TD=1.8 (RR + 1.7); RR = kΩ	0.8TD		1.2TD	ns
Phase Detect Centering	$\left(\pm\frac{TVCO}{2}\right)$	0		±5	%

MODE CONTROL

$\overline{WG}$	RG	$\overline{AMENB}$	MODES	DESCRIPTION
1	0	1	Idle	Idle mode. VCO locked to external FREF reference. RCLK synchronized to FREF. $\overline{AMD}$ tri-state.
1	0	0	AM Search	Read mode Address Mark search. VCO locked to external FREF reference. RCLK synchronized to FREF. $\overline{AMD}$ active.
1	1	1	Read Data	Read mode preamble search and data acquisition. VCO switched from FREF to RD after preamble lock. RCLK synchronized to RD after 19 "3T" patterns.
1	1	0	Undefined	Illegal state.
0	0	0	Write AM	Write mode Address Mark insertion. VCO locked to external FREF reference. WD, $\overline{WD}$ active. $\overline{AMD}$ tri-state.
0	0	1	Write Data	Write mode preamble insertion and data write. VCO locked to external FREF reference. RCLK synchronized to FREF. WD, $\overline{WD}$ active. $\overline{AMD}$ tri-state.
0	1	1	Undefined	Illegal state.
0	1	0	Undefined	Illegal state.

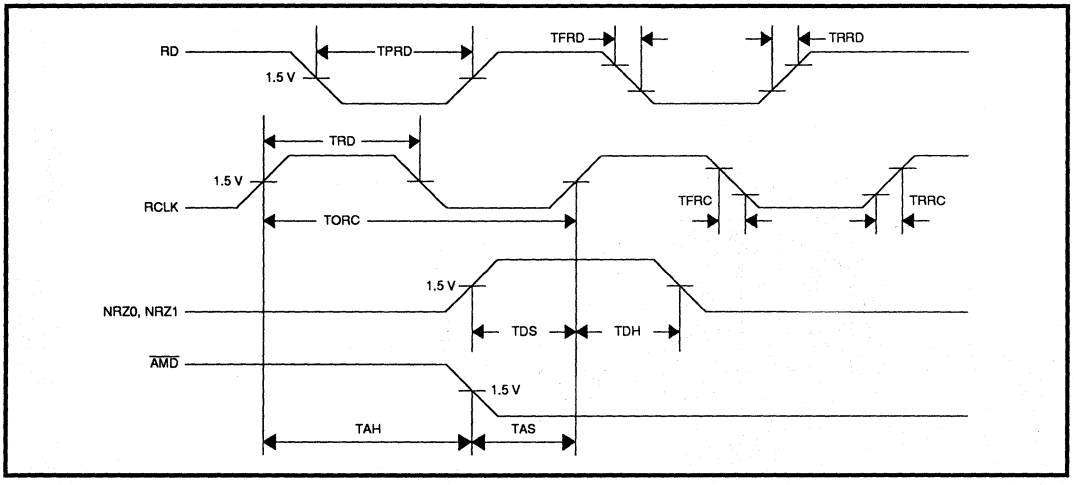


FIGURE 5: Read Timing

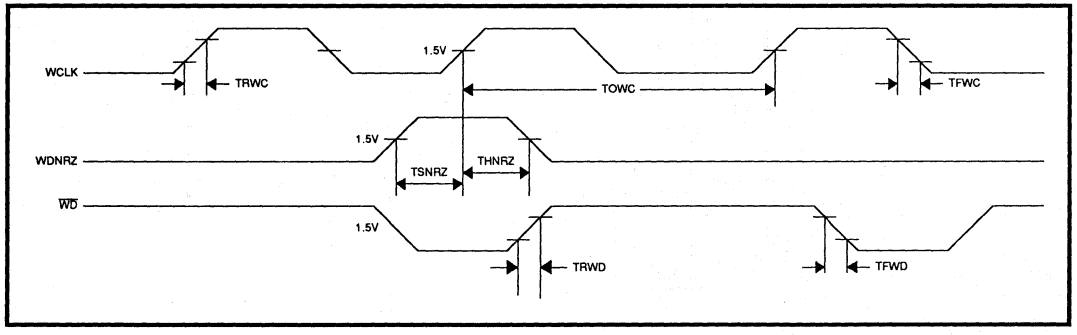


FIGURE 6: Write Timing

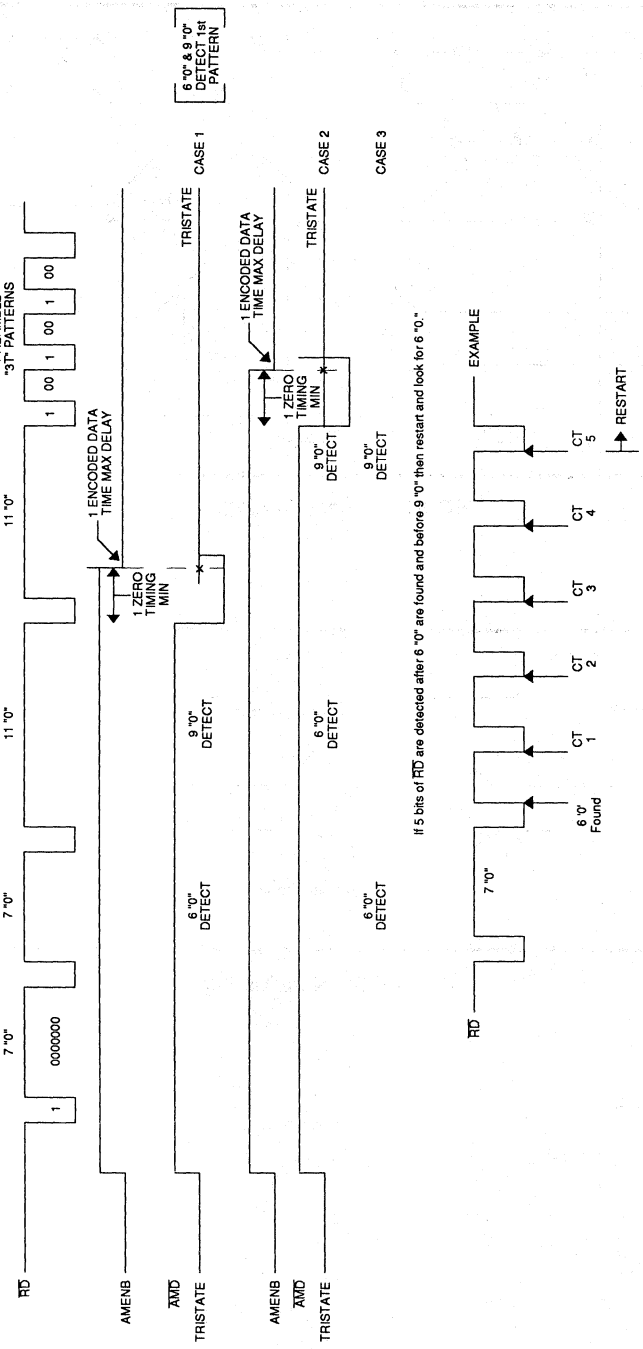


FIGURE 7: Address Mark Search

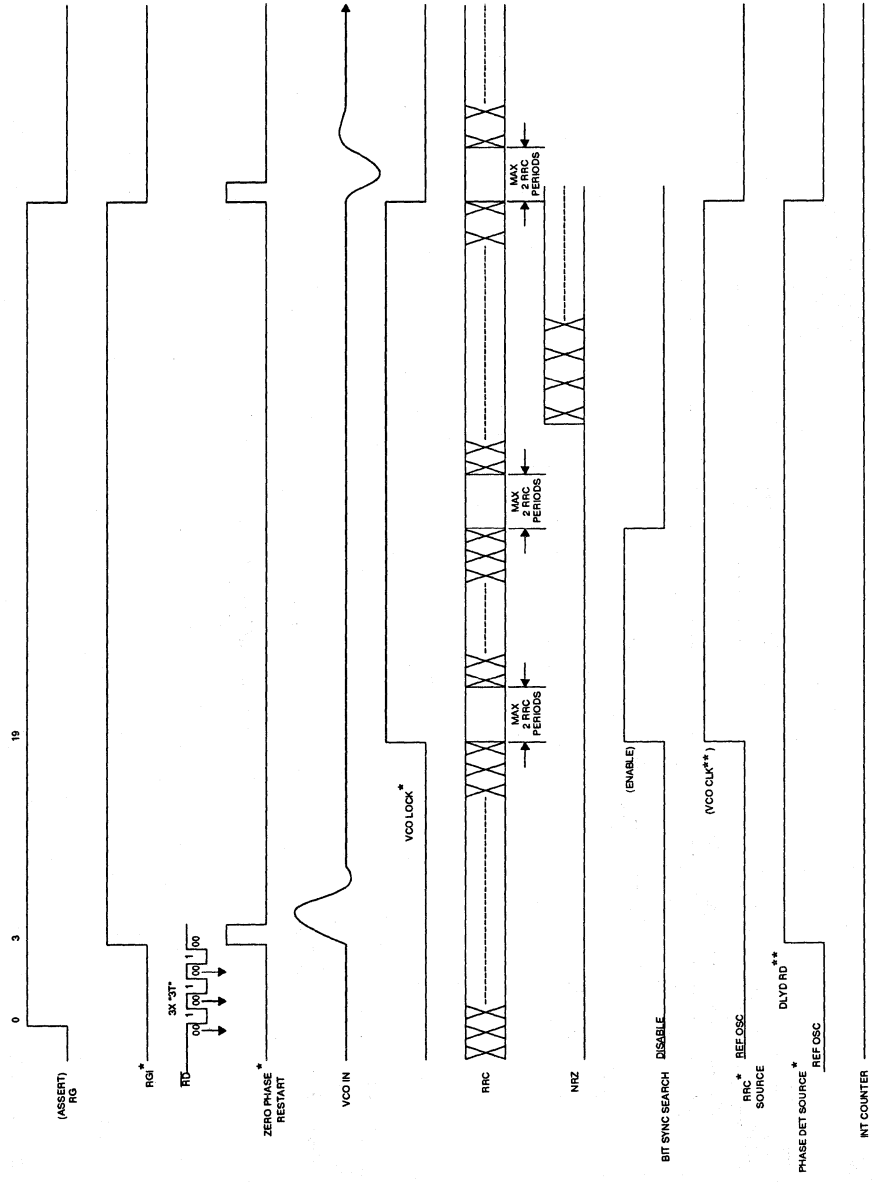


FIGURE 8: Read Mode Locking Sequence (Soft and Hard Sector)

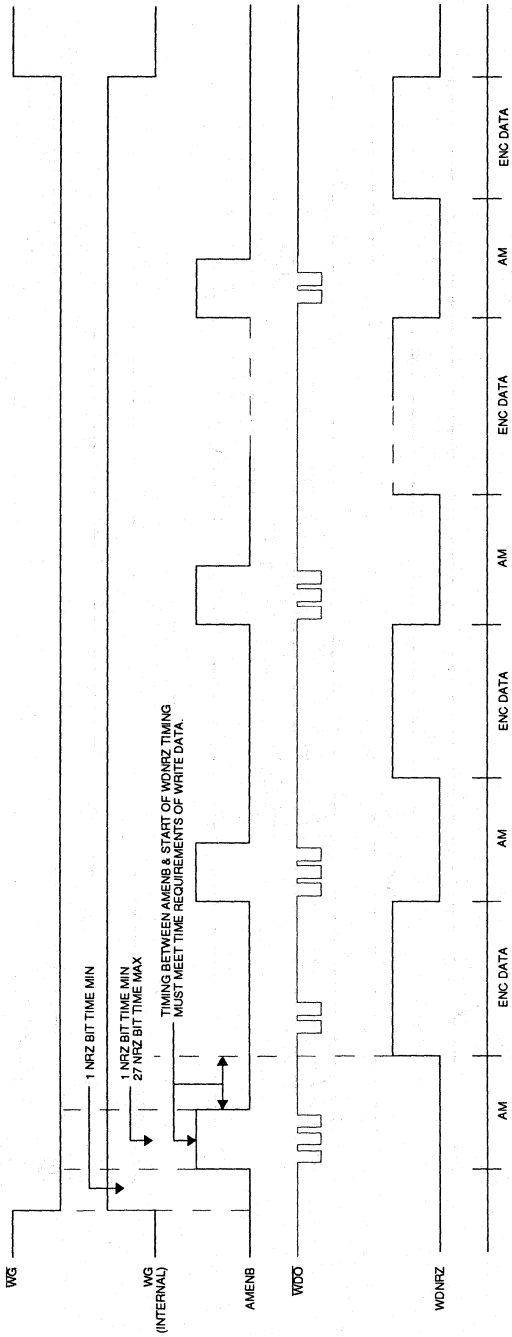


FIGURE 9: Multiple Address Mark Write

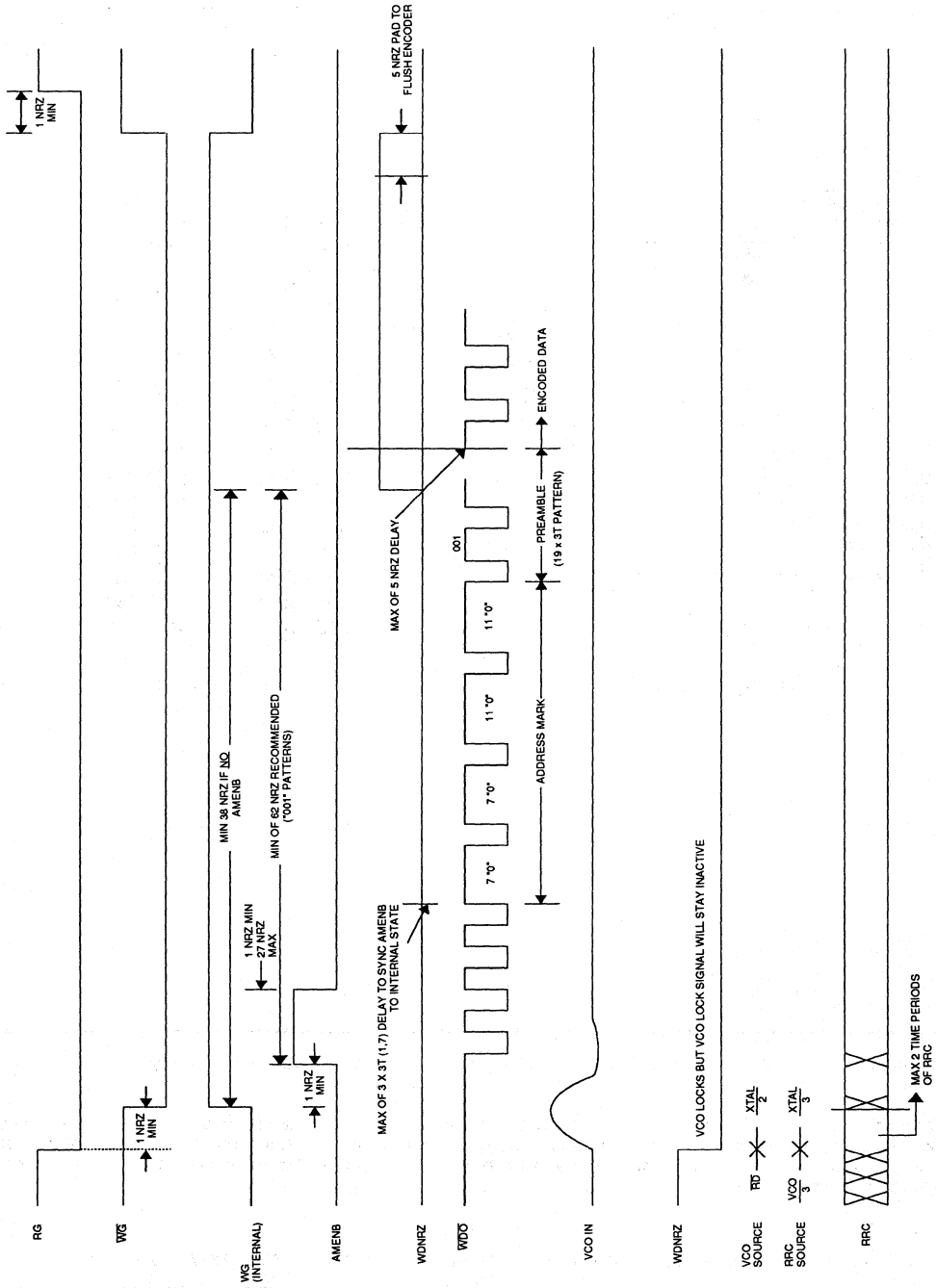
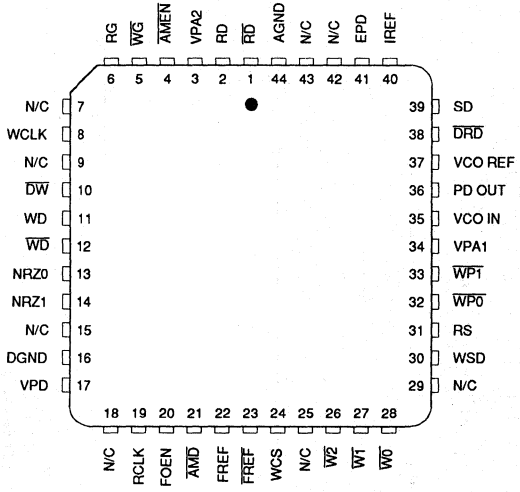


FIGURE 10: Write Data

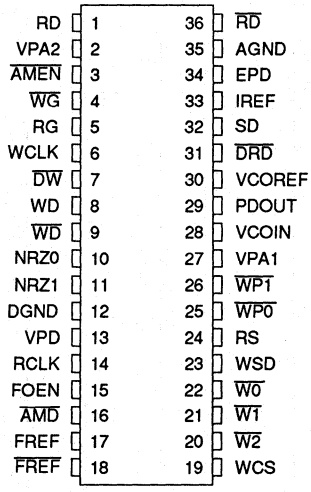
SSI 32D5396/5396A
Data Sync/1, 7 RLL ENDEC
with Write Precomp. and Window Shift

PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



44-Pin PLCC



36-Pin SOM

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914

silicon systems®
A TDK Group Company

SSI 32D4666
Time Base Generator

Preliminary Data

September 1993

DESCRIPTION

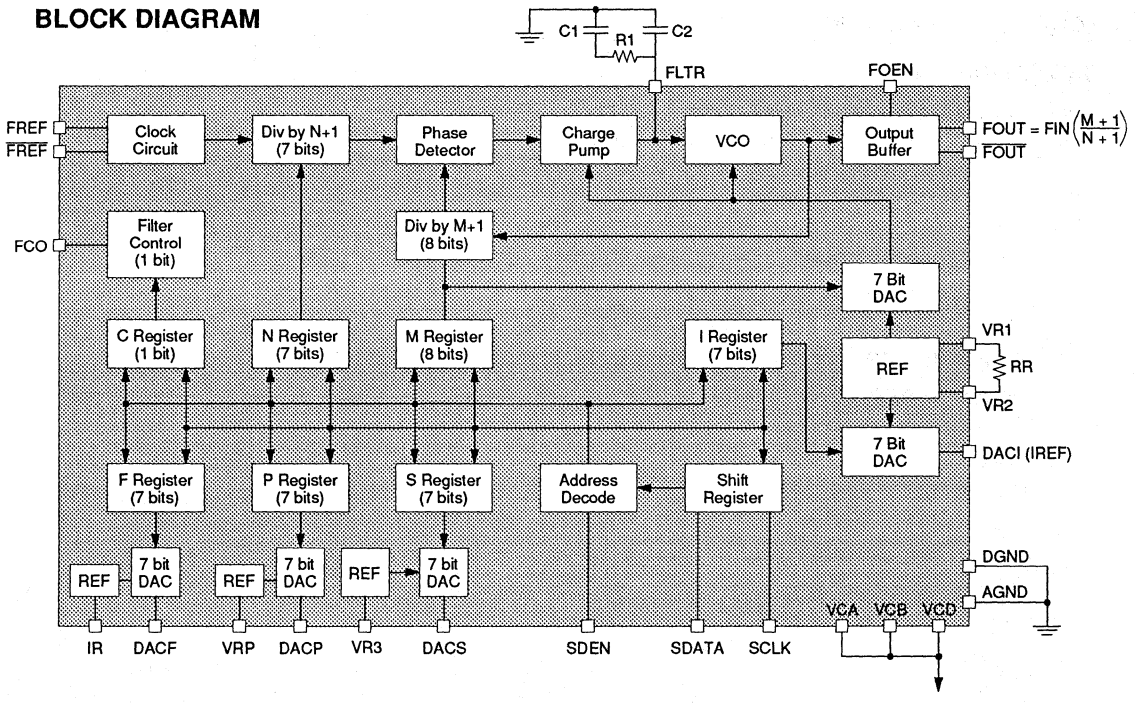
The SSI 32D4666 is a high performance bipolar device that provides a programmable frequency reference and four internal control DACs to support hard disk drive applications that use zoned recording techniques. It is optimized for use with the 32P3000 family of pulse detector/filter devices and the 32D53X family of data separators. The frequency reference can be programmed up to 108 MHz with better than 1% resolution. The 7-bit DACs provide control of the 3 dB cutoff frequency and pulse slimming of the electronic filter, the hysteresis level of the pulse qualifier, and the center frequency of the data separator. A single latched TTL output is also provided to control switching of external loop filter components on the data separator. A serial microprocessor interface reduces the pin count and provides convenient access to the internal program storage registers. The 32D4666 requires a +5 VDC supply and is available in a 24-lead SO and VSOP package.

FEATURES

- **Programmable frequency output up to 108 MHz**
- **1% frequency resolution**
- **Differential PECL reference clock input (FREF)**
- **Differential PECL frequency reference output (FOUT)**
- **7-bit DAC for data separator center frequency control (DACI)**
- **7-bit DAC for filter Fc control (DACF)**
- **7-bit DAC for filter boost/equalization control (DACS)**
- **7-bit DAC for hysteresis level control (DACP)**
- **+5 VDC operation**
- **Available in small footprint 24-lead SOL and VSOP packages**

4

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

FREQUENCY REFERENCE OPERATION

The 32D4666 programmable frequency reference accepts a differential PECL compatible clock source and generates a differential PECL compatible reference output (FOUT/$\overline{\text{FOUT}}$). The output frequency of FOUT is controlled by programming internal M and N counters to set up internal divide-by ratios. The 7-bit N register sets the divide-by factor for the input clock source. This will determine the update frequency for the phase detector. The value of this register is set based upon the frequency of the input clock according to the following equation:

$$N = [(FIN \times 256)/108] - 1$$

where FIN is in MHz

The 8-bit M register sets the divide-by term for the VCO reference clock feeding back into the phase detector and determines the center frequency of the VCO. The value set in the M register is independent of the input clock frequency. The value of the M register is determined by the following equation:

$$FOUT = [(M+1)/(N+1)] \times FIN$$

DAC OPERATION

The output of each of the four 7-bit DACs is controlled by programming the associated register. In addition, each DAC has a reference input that determines the maximum DAC output. The following equations are used to calculate the DAC outputs:

$$I_{DACF} = IR \times FREG \times 4/127 \text{ mA}$$

$$I_{DACI} = (7.41E - 2 \times IREG)/RR \text{ mA, where RR is in k}\Omega$$

$$V_{DACP} = [2 \times PREG \times (VRP - (VCA - VR3))]/127V$$

$$V_{DACS} = (SREG \times VR3)/127V$$

SERIAL PORT OPERATION

The 32D4666 provides a simple serial port interface that allows programming of the device's internal registers. The write-only serial port is a three-line interface that requires an enable signal (SDEN) along with clock (SCLK) and data (SDATA) signals to program the internal registers of the 32D4666. Data is shifted into the registers in 8-bit bytes that are divided into four bits of address and four bits of data. To load data into the device, the enable pin (SDEN) is asserted for eight clock cycles during which data can be presented on the SDATA input pin. Data on the SDATA pin is clocked into the device on the falling edges of the clock signal provided on the SCLK pin. The falling edge of SDEN latches the data internally and initiates the function selected. To save power the serial port circuitry is powered down when the SDEN line is low. Because of this, there is a minimum set-up and hold time for the SDEN signal (refer to specifications.) Table 1 provides the address-to-function mapping for the internal registers.

TABLE 1: Data Packet Fields (X = Don't care bit)

ADDRESS BITS				REGISTER	DATA BITS			
D7	D6	D5	D4		D3	D2	D1	D0
0	1	0	0	P Register	X	P6	P5	P4
0	1	0	1	P Register	P3	P2	P1	P0
0	1	1	0	I Register	X	I6	I5	I4
0	1	1	1	I Register	I3	I2	I1	I0
1	0	0	0	S Register	X	S6	S5	S4
1	0	0	1	S Register	S3	S2	S1	S0
1	0	1	0	F,C Register	C0	F6	F5	F4
1	0	1	1	F Register	F3	F2	F1	F0
1	1	0	0	M Register	M7	M6	M5	M4
1	1	0	1	M Register	M3	M2	M1	M0
1	1	1	0	N Register	X	N6	N5	N4
1	1	1	1	N Register	N3	N2	N1	N0

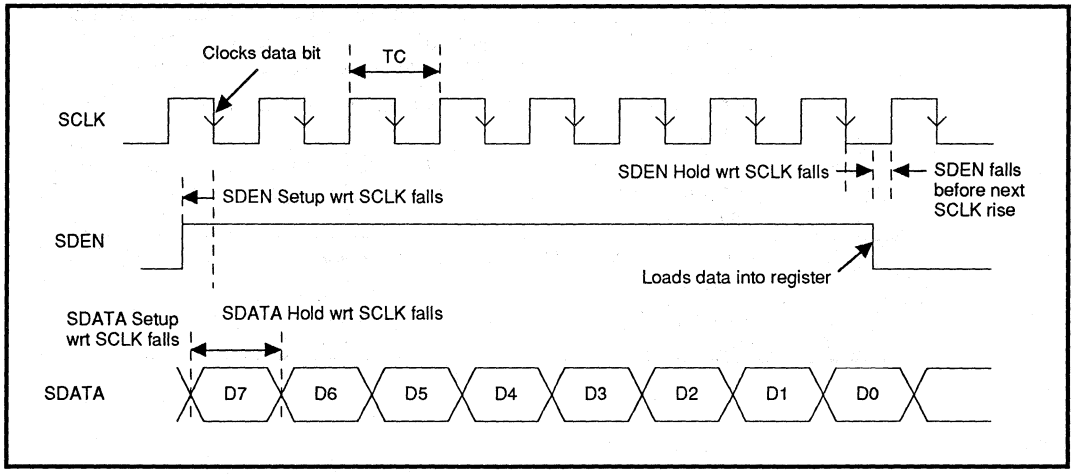


FIGURE 1: Serial Port Timing Relationship

PIN DESCRIPTION

INPUT PINS

NAME	TYPE	DESCRIPTION
AGND	I	Analog ground pin.
DGND	I	Digital ground pin.
VCA, B	I	+5V analog power supply pins.
VCD	I	+5V digital power supply pin.
FOEN	I	This is a TTL compatible input that disables the output buffer of the FOUT pin with a TTL low signal. This function is used to reduce jitter when the reference output is not required.
FREF/$\overline{\text{FREF}}$	I	Reference clock inputs. An 8 to 20 MHz differential PECL reference clock is applied to these input pins. This serves as the reference for the internal PLL.
IR	I	Reference Current Input. The current applied to this pin provides the reference for DACF.
SDATA	I	Serial port input data. Data input for an 8-bit internal shift register. The data packet is transmitted MSB (D7) first. The first four bits are the register address and the last four bits are the data value. For loading data into both registers of a DAC or the M and N counters, it is suggested that the registers be loaded with a minimum delay between packets to reduce the output transients.
SCLK	I	Serial Data Clock. Serial data is clocked into the internal shift register on the falling edge of this input.
SDEN	I	Serial Data Enable. A high level TTL input on this pin will enable the clocking of the internal shift register. The data in the shift register is latched on the falling edge of SDEN.
VR3	I	Reference Input Voltage. The voltage applied to this pin establishes the reference for DACS.
VRP	I	Reference Input Voltage. The voltage applied to this pin establishes the reference for DACP.

OUTPUT PINS

NAME	TYPE	DESCRIPTION
DACF	O	Current DAC output. The output of this 7-bit current DAC is determined by the contents of the F register and the current applied to the IR pin.
DACI	O	Current DAC output. The output of this 7-bit current DAC is determined by the contents of the I register and the resistor across the VR1/VR2 pins.
DACP	O	Voltage DAC output. The output of this 7-bit voltage DAC is determined by the contents of the P register.
DACS	O	Voltage DAC output. The output of this 7-bit voltage DAC is determined by the contents of the S register.
FCO	O	Filter Control Output. This is a latched TTL output that can be used to switch an external FET for changing the components of the data separator loop filter. When C0 is set to TTL high ("1") in the F register, the FCO output will be high.
FOUT/$\overline{\text{FOUT}}$	O	Frequency Output. A differential PECL frequency reference output that is determined by the M and N registers and the FREF/$\overline{\text{FREF}}$ input frequency. This output should be AC coupled into the reference input of the data separator device.

ANALOG PINS

FLTR	–	PLL loop filter. An RC filter is connected to this pin to control the VCO voltage.
VR1/VR2	–	Current setting resistor. A resistor is connected between these pins to set the current reference for DACI.

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, the recommended operating conditions are as follows: 4.65V < POSITIVE SUPPLY VOLTAGE < 5.25V, 0°C < T (ambient) < 70°C, and 25°C < T(junction) < 135°C. Currents flowing into the chip are positive. Current maximums are currents with the highest absolute value.

ABSOLUTE MAXIMUM RATINGS

Operation beyond the maximum ratings may damage the device.

PARAMETER	RATING
Storage Temperature	-65 to 150°C
Junction Operating Temperature, Tj	+150°C
Positive Supply Voltage (VCA, VCB, VCD)	-0.5V to 7V
Voltage Applied to Logic Inputs	-0.5V to Vp+0.5V

RECOMMENDED OPERATING CONDITIONS

Positive Supply Voltage (VCA, VCB, VCD)	4.65V to 5.25V
Junction Operating Temperature, Tj	$0 \leq Tj \leq 130°C$
Ambient Temperature, Ta	$0 \leq Ta \leq 70°C$

POWER SUPPLY CURRENT AND POWER DISSIPATION

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
ICC (VCA, B, D)	Outputs and test point pins open		77	110	mA
Pd Power Dissipation	Outputs and test point pins open		385	540	mW

TTL COMPATIBLE INPUTS

Input low voltage	VIL				0.8	V
Input high voltage	VIH		2.0			V
Input low current	IIL	VIL=0.4V			-1.5	mA
Input high current	IIH	VIH = 2.7V			20	µA

TTL COMPATIBLE OUTPUTS

Output low voltage	VOL	IOL = 2.0 mA			0.5	V
Output high voltage	VOH	IOH = -400 µA	2.4			V

PECL OUTPUT LEVELS (FOUT/$\overline{\text{FOUT}}$)

Output high level	VCA = 5.0 V	VCA-1.02			V
Output low level	VCA = 5.0 V			VCA-1.45	V
Single-ended output voltage swing	VCA = 5.0 V	0.75		0.95	V
Output current IFOUT		-4.0		+4.0	mA

PECL INPUT LEVELS (FREF/$\overline{FREF}$)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Input high level	VFIH	VCA = 5.0 V	VFIL-0.5		VCA-0.5	V
Input high current	IFIH				100	µA
Input low level	VFIL	VCA = 5.0 V	VCA-2.2		VFIH-0.5	V
Input low current	IFIL		-100			µA
Differential input		VCA = 5.0 V	0.5			V

FREQUENCY REFERENCE OUTPUT

Unless otherwise specified, FOUT = 30 MHz; loop filter components are C1 = 3300 pF, C2 = 270 pF, R1 = 4.12 kΩ; 4.65V ≤ VCn ≤ 5.25V; 0 ≤ Ta ≤ 70 °C.

Reference frequency	FIN		8		20	MHz
Output frequency	FOUT				108	MHz
Output jitter	JFO				0.5% x TVCO	ps(RMS)
Output duty cycle	DFO	50% amplitude, FOUT = 108 MHz	42		58	%
M counter value			80		255	
N counter value			18		127	
RR resistor value			4.5		5.25	kΩ
VCO center frequency	TVCO	TVCO = (4.01 E-10) (RR/M) + 2.4 nsec; VCA = 5.0V, RR = 4.75 kΩ, FLTR = 2.7V, M = 100, FIN = 20 MHz	0.77 TVCO		1.23 TVCO	ns
VCO dynamic range		1V < FLTR < VCA - 0.5 FOUT = 108 MHz, VCA = 5.0V	±25		±45	%
VCO control gain	KVCO	wi = 2π/TVCO	0.14 ωi		0.26 ωi	rad/s V
Phase detector gain	KD	K_D = (4.39E - 3) x M/RR		K_D		A/rad

CONTROL DACS

Differential linearity (monotonicity)		DACF, I, P, S 0 ≤ Ta ≤ 70°C 4.75V ≤ VCA ≤ 5.25V	-1LSB			
DACF output current	IOF	VCA = 5.0V IOF = (0.98) x F x 4 x IR)/127 Rx = 2.74 kΩ IR = VR3/(4 x Rx)	0.97 IOF -3/4LSB		1.04 IOF +3/4LSB	A

ELECTRICAL SPECIFICATIONS (continued)

CONTROL DACS (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Rx resistor value		2.5		3.0	kΩ
DACF output resistance				3.7	kΩ
DACI output accuracy	VCA = 5.0V IOI = (7.421E - 2) x I/RR RR = 4.75 kΩ	0.95 x IOI -3/4 LSB		1.05 x IOI +3/4 LSB	A
DACI/F output voltage				2	V
DACP output voltage VOP	VCA = 5.0V VOP = 2 x P x [VRP - (VCA - VR3)]/127 RR = 4.75 kΩ VR3 = 2.2V VRP = 3.6V	0.97V -3/4LSB -25 mV		1.04V +3/4LSB +25 mV	V
DACP output range		VCA- VR3		VCA- 0.9	V
DACP output resistance		50		200	Ω
VRP input voltage		(VCA -VR3) + 0.2		VCA -1.0	V
VRP input current	2.0V ≤ VRP ≤ VCA			20	µA
DACS output voltage VOS	VCA = 5.0V VOS = (0.98 x 5 x VR3)/127	0.97 x VOS -3/4LSB -15 mV		1.03 x VOS +3/4LSB +15 mV	V
DACS output range		0.1		2.4	V
DACS output resistance				3.7	kΩ
VR3 input voltage		2.0		2.4	V
VR3 input current	VR3 = 2.2V			1.0	mA

SERIAL PORT TIMING

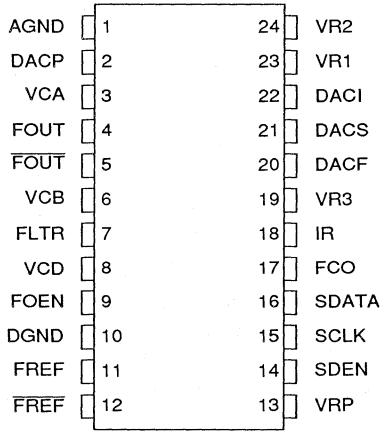
SCLK period		100			ns
SDEN Setup wrt first SCLK falls		10		TC/2 - 10	ns
SDEN Hold wrt last SCLK falls		10		TC/4	ns
SDEN falls wrt next SCLK rise		25			ns
SDATA Setup/Hold wrt SCLK falls		25			ns

PACKAGE PIN DESIGNATIONS

(Top View)

Thermal Characteristics: θjA

24-Lead SOL	80°C/W
24-Lead VSOP	110°C/W



24-Lead SOL/VSOP

CAUTION: Use handling procedures necessary for a static sensitive component.

4

ORDERING INFORMATION

PART DESCRIPTION		ORDER NUMBER	PACKAGE MARK
SSI 32D4666	24-Lead SOL	32D4666-CL	32D4666-CL
	24-Lead VSOP	32D4666-CV	32D4666-CV

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

Silicon Systems, Inc. 14351 Myford Road, Tustin, CA 92680-7022, (714) 573-6000, FAX (714) 573 6914

Notes:

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SSI 32D4680
80 Mbit/s Time Base Generator

Target Specification

January 1994

DESCRIPTION

The SSI 32D4680 Time Base Generator provides a programmable reference generator for constant density recording applications. It is optimized to operate with the SSI 32P4782 Read Channel Device for a high data rate (20 - 80 Mbit/s) Hard Disk Drive.

The SSI 32D4680 contains a high performance programmable PLL for 1 % reference frequency control. A serial microprocessor interface reduces pin count and provides convenient access to the internal program storage registers. The SSI 32D4680 only requires a +5V supply and is available in 16-Lead SO package(s).

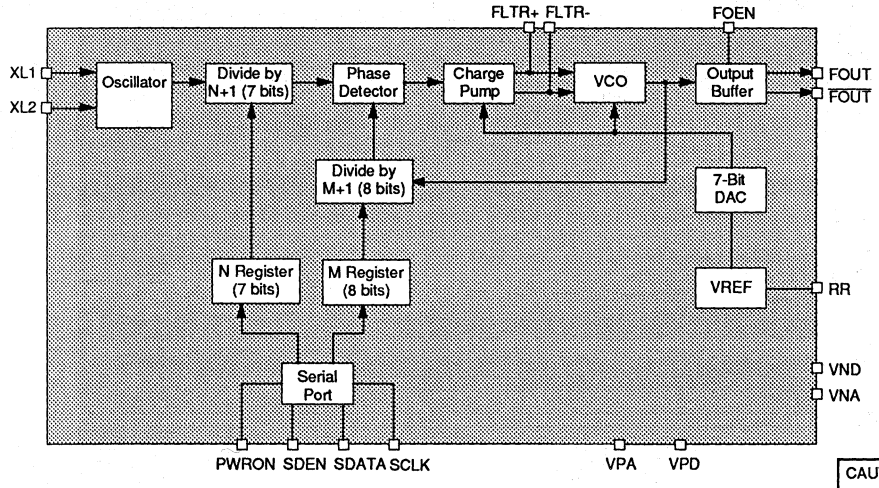
The SSI 32D4680 utilizes an advanced BiCMOS process technology along with patented circuit design techniques, resulting in a high performance device with low power consumption.

FEATURES

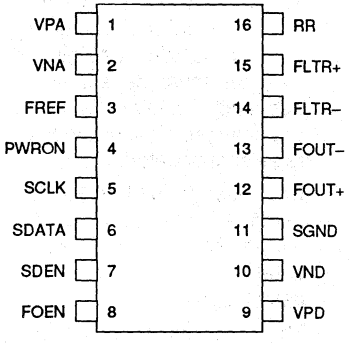
- **For constant density recording applications when utilized with SSI 32P4782**
- **Reference frequency control**
- **Up to 120 MHz operation**
- **1% frequency resolution**
- **No external active components required**
- **+ 5V only operation**
- **16-Lead SO package**

4

BLOCK DIAGRAM



PIN DIAGRAM



16-Lead SON

CAUTION: Use handling procedures necessary for a static sensitive component.

The target specification is intended as an initial disclosure of specification goals for the product. The specifications are based on design goals, subject to change and are not guaranteed. Silicon Systems assumes no obligation regarding future manufacture unless agreed to in writing.

FUNCTIONAL DESCRIPTION

The SSI 32D4680 Time Base Generator, a PLL based circuit, provides a programmable reference frequency to the data separator (of the SSI 32P4782) for constant density recording applications. The data separator reference frequency runs at 1.5 times the NRZ data rate. This time base generator output frequency can be programmed with a better than 1% accuracy via the M, N, and DR Registers.

The time base generator requires an external passive loop filter to control its PLL locking characteristics. This filter is fully differential and balanced in order to suppress the common mode noise.

In Read, Write and Idle modes, the time base generator is programmed to provide a stable reference frequency for the data separator. However, in the Read mode, the TBG outputs are disabled after the internal VCO lock signal (of the 32P4782 device) is asserted to minimize signal coupled to the data separator PLL. This is done through the FOEN pin. A logic low level at the FOEN will disable the TBG outputs.

The reference frequency is programmed using the M and N registers of the time base generator via the serial port, and is related to the external reference clock input, FREF, as follows:

$$FTBG = FREF ((M + 1) / (N + 1))$$

The M and N values should be chosen with the consideration of phase detector update rate and the external passive loop filter design. The Data Rate Register must be set to the correct VCO center frequency. The time base generator PLL responds to any changes to the M and N registers, only after the DR register is updated.

Data rates from 20 to 80 Mbit/s can be programmed using an internal DAC (DACI) whose reference current, set by a single external 4.75 kΩ resistor RR, determines the VCO center frequency, and the phase detector gain.

The VCO center frequency is programmed by the following equation and should be set close to 1.5 times the NRZ data rate.

$$Fvco (MHz) = (K1 \times DR) + K2,$$

while, K1 = TBD, K2 = TBD

SERIAL INTERFACE PORT

The time base generator output frequency is programmed via the M, N and DR Registers. Data (address and contents) are transferred through the serial interface port. For data transfers, SDEN is first brought high, serial data is presented at the SDATA pin, and a serial clock is applied to SCLK pin. After the SDEN goes high, the first 16 pulses applied to the SCLK pin will shift the data presented at the SDATA pin into an internal shift register on the rising edge of each clock. An internal counter prevents more than 16 bits from being shifted into the register. The data in the shift register is latched when SDEN goes low. If less than 16 clock pulses are provided before SDEN goes low, the data transfer is aborted.

In addition, there is a control A Register. It controls different Enable and Test modes of the device.

All transfers are shifted into the serial port LSB first. The first byte of the transfer is address and instruction information. The LSB of this byte is the R/W bit which determines if the transfer is a READ (1) or a WRITE (0). The remaining 7- bits determine the internal register to be accessed. Table 1 provides register mapping information. The second byte contains the programming data.

In Read mode (R/W = 1), the 32D4680 will output the register contents of the selected address. In Write mode the device will load the selected register with data presented on the SDATA pin.

At initial power-up, the contents of the internal registers will be in an unknown state and they must be programmed prior to operation.

TABLE 1: Control Register

M Counter Register (address = 0001110)		
BIT	**NAME**	**FUNCTION**
Bits 7 -0	M7 -0	M counter value
N Counter Register (address = 0000110)		
Bit 7		Not used, don't care
Bits 6 -0	N6 -0	N counter value
Data Rate Register (address = 0010110)		
Bit 7		Not used, don't care
Bit 6 -0	DR6 -0	VCO's center frequency biasing, Fvco = 1.5 X NRZ data rate = K1 X DR + K2, While K1, K2 = TBD
Control A Register (address = 0011110)		
Bit 0, D0	TBG_EN	Enable TBG
Bit 1, D1	EPDT	Enable Phase Detector
Bit 2, D2	UT	Enable Pump Up current
Bit 3, D3	DT	Enable Pump Down current
Bit 4, D4	TM1	Enable FOUT1/$\overline{\text{FOUT1}}$ Test outputs
Bit 5, D5		Not used, don't care
Bit 6, D6	TM2	Enable Test output Biasing circuit
Bit 7, D7	TM3	Enable IDAC Testing

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
PWRON	I	Power Enable, CMOS compatible. A high level input enables the power. A low level disables the power.
SDATA	I	Serial data, CMOS compatible. Data input for an 8 - bit control shift register.
SCLK	I	Serial data clock, CMOS compatible. Positive edge triggered clock input for the serial data.
SDEN	I	Serial data enable, CMOS compatible. A high level input enables data loading. Data is latched when the input is low.
FOEN	I	Frequency output enable, CMOS compatible. A high level input enables the FOUTP, FOUTN outputs. A low level disables the outputs.
FOUTP, FOUTN	O	Frequency outputs. A P-ECL level swing which minimizes data separator jitter and must be AC coupled to the data separator inputs.

ANALOG PINS

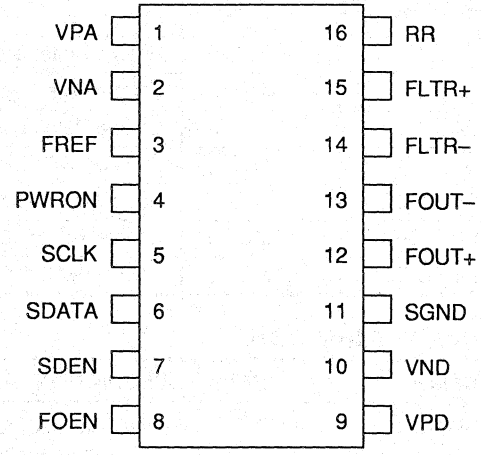
NAME	TYPE	DESCRIPTION
FREF	–	Reference frequency input for the TBG. FREF is driven by a direct coupled TTL compatible signal.
RR	–	Current setting register connection. An external resistor connected between RR and Gnd sets the DACI currents.
FLTRP, FLTRN	–	PLL loop filter connections. FLTRP is the positive output of the phase detector, FLTRN is the negative output of the phase detector. The effective VCO voltage is, FLTRP - FLTRN.

POWER SUPPLY PINS

VND, VNA	–	Digital and analog ground.
VPD, VPA	–	Digital and analog +5V supply.
SGND	–	Substrate ground.

PACKAGE PIN DESIGNATIONS

(Top View)



16-Lead SON

CAUTION: Use handling procedures necessary for a static sensitive component.

Target Specification: The target specification is intended as an initial disclosure of specification goals for the product. The specifications are based on design goals, subject to change and are not guaranteed. Silicon Systems assumes no obligation regarding future manufacture unless agreed to in writing.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914

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SSI 32P541C
Pulse Detector

Preliminary Data

December 1993

DESCRIPTION

The SSI 32P541C is a bipolar integrated circuit that provides all data processing necessary for detection and qualification of MFM or RLL encoded read signals.

In Read mode the SSI 32P541C provides amplification and qualification of head preamplifier outputs. Pulse qualification is accomplished using level qualification of differentiated input zero crossings. An AGC amplifier is used to compensate for variations in head preamp output levels, presenting a constant input level to the pulse qualification circuitry. The AGC loop can be disabled so that a constant gain can be used for embedded servo decoding or other processing needs.

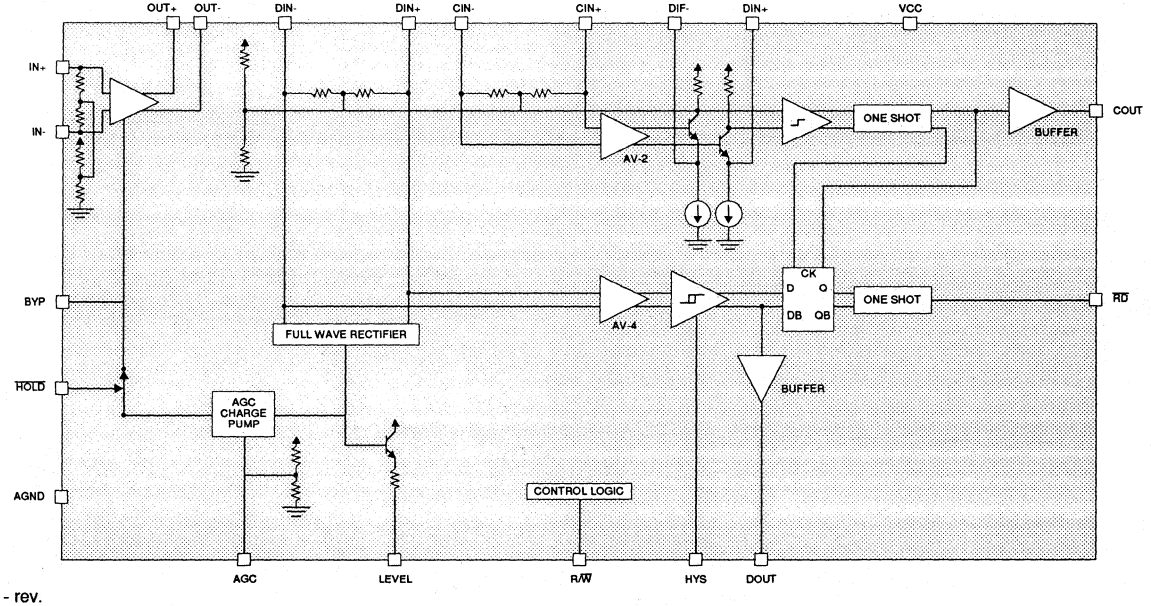
In Write mode the circuitry is disabled and the AGC gain stage input impedance is switched to a lower level to allow fast settling of the input coupling capacitors during a write to read transition. The SSI 32P541C requires a +5V power supply and is available in a 28-pin PLCC package.

FEATURES

- **Level qualification supports high resolution MFM and RLL encoded data retrieval**
- **Wide bandwidth AGC input amplifier**
- **Standard +5V ±10% supplies**
- **Write to read transient suppression**
- **Fast and slow AGC attack regions for fast transient recovery**
- **≤1.0 ns pulse pairing**
- **32 Mbit/s operation**
- **Low power**

4

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

READ MODE

In Read mode (R/$\overline{W}$ input high or open) the input signal is amplified and qualified using an AGC amplifier and pulse level qualification of the detected signal peaks.

An amplified head output signal is AC coupled to the IN+ and IN- pins of the AGC amplifier. Gain control is accomplished by full wave rectifying and amplifying the [(DIN+)-(DIN-)] voltage level and comparing it to a reference voltage level at the AGC pin.

The 32P541C contains a dual rate attack charge pump. The value of the attack current is dependent on the instantaneous level at DIN±. For signal levels above 125% of the desired level a Fast Attack mode is invoked that supplies a 1.2 mA charge current to the network on the BYP pin. Between 125% and 100% of the desired level the circuit enters a Slow Attack mode and supplies 0.17 mA of charge current to the BYP pin.

Two Decay modes are available and are automatically controlled within the device.

Upon a switch to Write mode, the device will hold the gain at its previous value. When the device is then switched back to Read mode the AGC holds the gain and stays in a low impedance state for 0.9 µs. It then switches into a Fast/Slow Attack mode if the new gain required is less than the previously held gain or a Fast Decay mode if the gain required is more than its previous value. The fast decay current is 0.10 mA and stays on for 0.9 µs. After the 0.9 µs time period the device stays in a steady state slow attack, Slow Decay mode. The slow decay discharge current is 4.5 µA.

The AGC pin is internally biased so that the target differential voltage input at DIN± is 1.0 Vpp under nominal conditions. The voltage on this pin can be modified by tying a resistor between AGC and GND or VPA. A resistor to GND decreases the voltage level, while a resistor to VPA increases it. The resulting AGC voltage level is shown in Figure 1; where:

V = Voltage at AGC w/pin open (2.2V, nom)

Rint = AGC pin input impedance (3.9 kΩ, typ)

Rext = External resistor

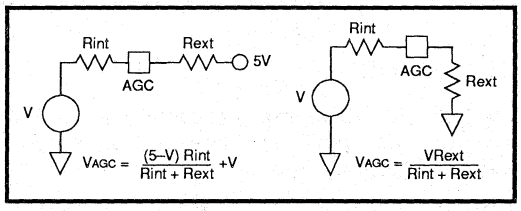


FIGURE 1: AGC Voltage

The new DIN± input target level is nominally: 0.45 Vpp/V • VAGC.

The maximum AGC amplifier output swing is 3.0 Vpp at OUT±, which allows for up to 6 dB loss in any external filter between OUT± and DIN±.

AGC gain is a linear function of the BYP-pin voltage (VBYP) as shown in Figure 2.

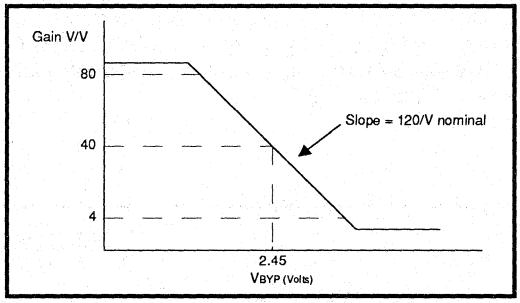


FIGURE 2: AGC Gain

In the amplitude channel the signal is sent to a hysteresis comparator. The hysteresis threshold level is set so that it will be tripped only by valid signal pulses and not by baseband noise. It can be a fixed level or a fraction of the DIN± voltage level.

The latter approach is accomplished by using an external filter/network between the LEVEL and HYS pins. This allows setting the AGC slow attack and decay times slow enough to minimize time channel distortion and setting a shorter time constant for the hysteresis level. The LEVEL pin output is a rectified and amplified version of DIN±, 1.0 Vpp at DIN± results in 1.0 V0-pk nominally, at the LEVEL pin. A voltage divider is used from LEVEL to ground to set the Hysteresis threshold at a percentage of the peak DIN± voltage. For example,

if DIN± is 1.0 Vpp, then using an equal valued resistor divider will result in 0.5 Vpk at the HYS pin. This will result in a nominal ±0.18V threshold or a 36% threshold of a ±0.500V DIN± input. The capacitor is chosen to set an appropriate time constant. This "feed forward" technique speeds up transient recovery by allowing qualification of the input pulses while the AGC is still settling. This helps in the two critical areas of write to read and head change recovery. Some care in the selection of the hysteresis level time constant must be exercised so as to not miss pattern (resolution) induced lower amplitude signals. The output of the hysteresis comparator is the "D" input of a D-type flip-flop. The DOUT pin is a comparator output signal for testing purposes only.

In the time channel the signal is differentiated to transform signal peaks to zero crossings which are detected and used to trigger a bi-directional one-shot. The one-shot output pulses are used as the clock input of the D flip-flop. The COUT pin provides the one-shot output for test purposes.

The differentiator function is accomplished by an external network between the DIF+ and DIF- pins. The transfer function from CIN± to the comparator input (not DIF±) is:

$$Av = \frac{-3536Cs}{LCs^2 + C(R+52)s + 1}$$

where: C, L, R are external passive components
$15\ pF < C < 125\ pF$
$s = j\omega = j2\pi f$

OFF-CHIP DIFFERENTIATION

For constant density recording applications, a differentiation function with a low pass bandwidth tracking data rate can maximize the signal-to-noise ratio performance. A time differentiated input can be applied at the CIN± pins, separated from the DIN± pins. A 2.0 kΩ resistor should be placed across the DIF± pins. This function can best be supported by the Silicon Systems programmable filters, such as the SSI 32F8020A and the SSI 32F8120A. The filters feature both a normal low pass output and a differentiated low pass output. The low pass bandwidth is programmable by the user to track the data rate. The signal delays of the two signal paths are well matched.

During normal operation, the time channel clocks the D flip-flop on every positive and negative peak of the CIN± input. The D input to the flip-flop only changes state when the DIN± input exceeds the hysteresis comparator threshold opposite in polarity to the previous threshold exceeding peak.

The time channel, then, determines signal peak timing and the amplitude channel determines validity by blocking signal peaks that do not exceed the hysteresis comparator threshold. The delays in each of these channels to the D flip-flop inputs are well matched.

WRITE MODE

In Write Mode the SSI 32P541C Pulse Detector section is disabled and preset for the following Read Mode. The digital circuitry is disabled, the input AGC amplifier gain is held at its previous value and the AGC amplifier input impedance is reduced.

Holding the AGC amplifier gain and reducing input impedance shortens system Write to Read recovery times.

The lowered input impedance improves settling time by reducing the time constant of the network between the SSI 32P541C and a head preamplifier such as the SSI 32R2020R. Write to read timing is controlled to maintain the reduced impedance for 0.9 µs before the AGC circuitry is activated. Coupling capacitors should be chosen with as low a value as possible consistent with adequate bandwidth to allow more rapid settling.

MODE CONTROL

The SSI 32P541C Circuit mode is controlled by the $\overline{PDWN}$, $\overline{HOLD}$, and R/$\overline{W}$ pins as shown in Table 1.

TABLE 1: Mode Control

R/$\overline{W}$	$\overline{HOLD}$	
1	1	Read mode, AGC Active
1	0	Read mode AGC gain held constant*
0	X	Write mode AGC gain held constant* Input impedance reduced

* AGC gain will drift at a rate determined by BYP and Hold mode discharge current.

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
VCC	I	+5V power supply for pulse detector
AGND	I	Analog ground pin for pulse detector block
DGND	I	Digital ground pin
IN+, IN–	I	Analog signal input pins to AGC amplifier
OUT+, OUT–	O	Read path AGC Amplifier output pins
DIN+, DIN–	I	Analog input to the hysteresis comparator
CIN+, CIN–	I	Analog input to the differentiator
DIF+, DIF–	I/O	Pins for external differentiating network
COUT	O	Test point for monitoring the flip-flop clock input. 5 kΩ resistor to GND is needed to use this pin as a test point. Leave it open in normal operation to save power dissipation.
DOUT	O	Test point for monitoring the flip-flop D-input. 5 kΩ resistor to GND is needed to use this pin as a test point. Leave it open in normal operation to save power dissipation.
$\overline{RD}$	O	TTL compatible read output
BYP	I/O	An AGC timing capacitor or network is tied between this pin and AGND1
AGC	I	Reference input voltage for the read data AGC loop
LEVEL	O	Output from fullwave rectifier that may be used for input to the hysteresis comparator
HYS	I	Hysteresis level setting input to the hysteresis comparator
$\overline{HOLD}$	I	TTL compatible pin that holds the AGC gain when pulled low
R/$\overline{W}$	I	Selects Read or Write mode

ELECTRICAL SPECIFICATIONS

Recommended conditions apply unless otherwise specified.

ABSOLUTE MAXIMUM RATINGS

Operation outside these rating limits may cause permanent damage to this device.

PARAMETER	RATING
5V Supply Voltage, VCC	6.0V
Pin Voltage	-0.3 to VCC, + 0.3V
Storage Temperature	65 to 150°C
Lead Temperature (Soldering 10 sec.)	260°C

RECOMMENDED OPERATING CONDITIONS

Currents flowing into the chip are positive.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Supply Voltage, VCC		4.5	5.0	5.5	V
Junction Temperature, Tj		25		135	°C
Ambient Temperature, Ta		0		70	°C

POWER SUPPLY

IVCC	Supply Current	Outputs unloaded; $\overline{PDWN}$ = high or open	19	34	42	mA
PD	Power dissipation	Ta = 25°C, outputs unloaded		170	230	mW

LOGIC SIGNALS

VIL	Input Low Voltage		-0.3		0.8	V
VIH	Input High Voltage		2.0		VCC+0.3	V
IIL	Input Low Current	VIL = 0.4V	-0.4			mA
IIH	Input High Current	VIH = 2.4V			100	µA
VOL	Output Low Voltage	IOL = 4.0 mA			0.5	V
VOH	Output High Voltage	IOH = -400 µA	2.4			V

ELECTRICAL SPECIFICATIONS (continued)

MODE CONTROL

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Read to Write Transition Time	R/$\overline{W}$ pin high to low			1.0	µs
Write to Read Transition Time	R/$\overline{W}$ pin low to high AGC settling not included	0.5	0.9	1.3	µs
$\overline{HOLD}$ Off to $\overline{HOLD}$ On Transition Time	$\overline{HOLD}$ pin transitions from high to low			1.0	µs

READ MODE (R/$\overline{W}$ is high)

AGC AMPLIFIER

Unless otherwise specified, recommended operating conditions apply. Input signals are AC coupled to IN± and amplitude is between 25 mVpp & 250 mVpp differential. OUT± are loaded differentially with >600Ω, and each side is loaded with < 10 pF to AGND, and AC coupled to DIN±. A 2000 pF capacitor is connected between BYP and AGND. AGC pin is open.

Gain Range	1.0 Vpp ≤ OUT± ≤ 3.0 Vpp	4		80	V/V
Output Offset Voltage	Over entire gain range	-200	0	+200	mV
Maximum Output	Set by BYP pin	3.0			Vpp
Voltage Swing	THD ≤ 5%				
Differential Input Resistance	IN± = 100 mVpp @ 2.5 MHz		5.0		kΩ
Differential Input Capacitance	IN± = 100 mVpp @ 2.5 MHz			10	pF
Common Mode Input	R/$\overline{W}$ = high		1.5		kΩ
Impedance	R/$\overline{W}$ = low		250		Ω
Input Noise Voltage	Gain set to maximum		5.5	15	nV/$\sqrt{Hz}$
Bandwidth	-3 dB bandwidth at maximum gain	32			MHz
OUT+ & OUT- Pin Current	No DC path to AGND		3		mA
CMRR (Input Referred)	IN± = 0 VDC + 100 mVpp @ 2.5 MHz, gain set to max	40	63		dB
PSRR (Input Referred)	100 mVpp @ 2.5 MHz on VCC, gain set to max	30	66		dB

AGC AMPLIFIER (Continued)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
DIN± Input Swing vs. AGC Input	25 mVpp ≤ IN± ≤ 250 mVpp, $\overline{HOLD}$ = high, 0.5 Vpp ≤ DIN± ≤ 1.5 Vpp	0.38	0.45	0.56	Vpp/V
DIN± Input Voltage Swing Variation	25 mVpp ≤ IN± ≤ 250 mVpp			6.0	%
AGC Voltage	AGC open	1.8	2.2	2.6	V
AGC Pin Input Impedance		3.5	3.9	5.5	kΩ
Slow AGC Discharge Current	(DIN+) - (DIN-) = 0V	3.5	4.3	6	µA
Fast AGC Discharge Current	Starts at 0.9 µs after R/$\overline{W}$ goes high, stops at 1.8 µs after R/$\overline{W}$ goes high	70	102	150	µA
AGC Leakage Current	$\overline{HOLD}$ = low	-0.2	0	+0.2	µA
Slow AGC Charge Current	(DIN+) - (DIN-) = 0.8 VDC, vary AGC until slow charge begins	-0.12	-0.17	-0.24	mA
Fast AGC Charge Current	(DIN+) - (DIN-) = 0.8 VDC, V_{AGC} = 3.0V	-0.9	-1.2	-1.7	mA
Fast to Slow Attack Switchover Point	$\frac{[(DIN+)-(DIN-)]}{[(DIN+)-(DIN-)]FINAL}$		125		%
Gain Decay Time (Td)	IN± = 250 mVpp to 125 mVpp @ 2.5 MHz, OUT± to 90% final value		20		µs
	IN± = 50 mVpp to 25 mVpp at 2.5 MHz OUT± to 90% final value		70		µs
Gain Attack Time	R/$\overline{W}$ = low to high IN± = 250 mVpp @ 2.5 MHz, OUT± to 110% final value		2		µs

WRITE MODE (R/$\overline{W}$ is low)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Common Mode Input Impedance			250		Ω

ELECTRICAL SPECIFICATIONS (continued)

HYSTERESIS COMPARATOR

Unless otherwise specified, recommended operating conditions apply. Input (DIN+) - (DIN-) is an AC coupled, 1.0 Vpp, 2.5 MHz sine wave. 0.5 VDC is applied to the HYS pin. R/$\overline{W}$ pin is high.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Input Signal Range		0.6	1.0	1.5	Vpp
Differential Input Resistance	DIN± = 100 mVpp @ 2.5 MHz	17.5	20	22.5	kΩ
Differential Input Capacitance	DIN± = 100 mVpp @ 2.5 MHz			5.0	pF
Common Mode Input Impedance (Both Sides)		3	4.8	5.5	kΩ
Level Pin Output Voltage vs. DIN±	0.6 Vpp < DIN± < 1.5 Vpp, 10 kΩ between LEVEL pin and AGND		1		V/Vpp
Level Pin Output Offset Voltage	10 kΩ between LEVEL pin and AGND	120	170	250	mV
Level Pin Output Impedance	I_{LEVEL} = 0.2 mA		330		Ω
Level pin Maximum Output Current		2.0			mA
Hysteresis Voltage at DIN± vs. HYS Pin Voltage	0.3 V < HYS < 1.0V		0.19		V/V
HYS Pin Input Current	0.5 V < HYS < 1.5V	-10.0		0	µA
Comparator Offset Voltage	HYS pin at AGND ≤1.5 kΩ across DIN±			5.0	mV
DOUT Pin Output Low Voltage	5 kΩ from DOUT to GND		VPA -2.8		V
DOUT Pin Output High Voltage	5 kΩ from DOUT to GND		VPA -2.4		V

ACTIVE DIFFERENTIATOR

Unless otherwise specified, recommended operating conditions apply. Input CIN± is an AC-coupled, 1.0 Vpp, 2.5 MHz sine wave. 100Ω in series with 65 pF are tied from DIF+ to DIF-.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Input Signal Range		0.6	1.0	1.5	Vpp
Differential Input Resistance	CIN± = 100 mVpp @ 2.5 MHz	17.5	20	22.5	kΩ
Differential Input Capacitance	CIN± = 100 mVpp @ 2.5 MHz			5.0	pF
Common Mode Input Impedance	Both sides	3.5	4.5	5.5	kΩ
Voltage Gain From CIN± to DIF±	Resistor across DIF± is 2 kΩ		1		V/V
DIF+ to DIF- PIn Current	Differentiator impedance must be set so as to not clip the the signal for this current level	-0.7		0.7	mA
COUT Pin Output Low Voltage	5 kΩ from COUT to GND		VPA -2.8		V
COUT Pin Output High Voltage	5 kΩ from COUT to GND		VPA -2.4		V
COUT Pin Output Pulse Width			47		ns

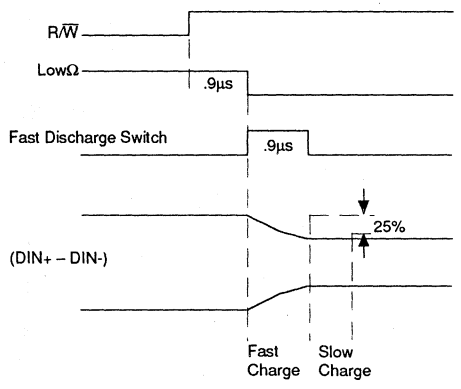


Figure A: AGC Attack Sequence

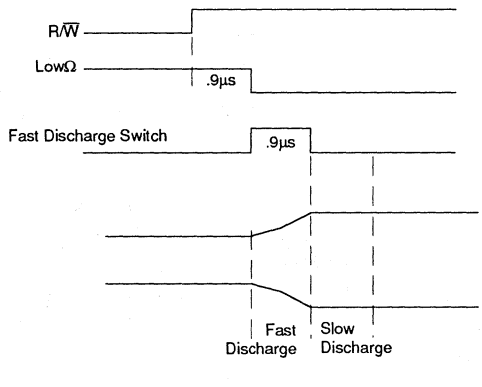


Figure B: AGC Decay Sequence

FIGURE 7: AGC Timing Diagram

ELECTRICAL SPECIFICATIONS (continued)

QUALIFIER TIMING

Unless otherwise specified, recommended operating conditions apply. Inputs CIN± and DIN± are in-place as a coupled, 1.0 Vpp, 2.5 MHz sine wave. 100Ω in series with 65 pF are tied from DIF+ to DIF-. 0.5V is applied to the HYS pin. COUT and DOUT each have a 5 kΩ pull-down resistor (for test purposes only.) R/$\overline{W}$ pin is high.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Td1	D Flip-Flop Set Up Time	Minimum allowable time delay from (DIN+) - (DIN-) exceeding hysterisis point to (DIF+) - (DIF-) hitting a peak value.	0			ns
Td3	Propagation Delay	From positive peak to $\overline{RD}$ output pulse		28		ns
Td4	Propagation Delay	From negative peak to $\overline{RD}$ output pulse		28		ns
|Td3-Td4|	Pulse Pairing			1.0		ns
Td5	$\overline{RD}$ Output Pulse Width	$\overline{RD}$ pin open	8		14	ns

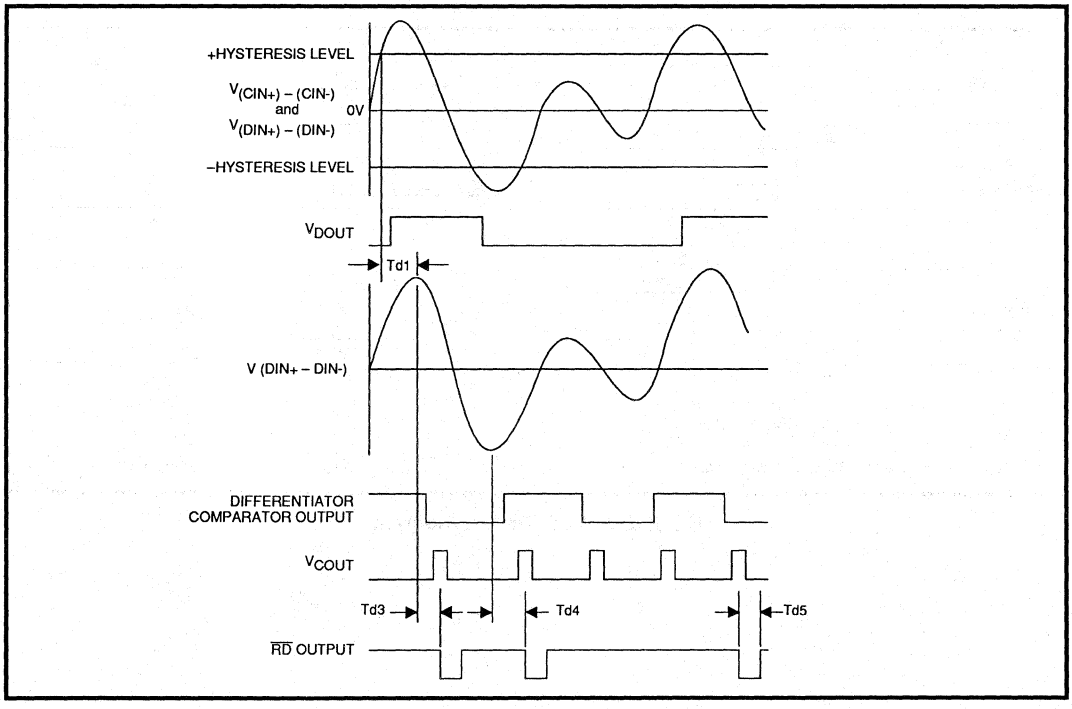
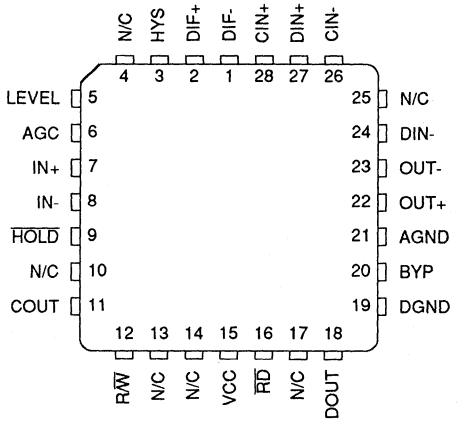


FIGURE 8: Read Mode Digital Section Timing Diagram

PACKAGE PIN DESIGNATIONS

(Top View)



28-Pin PLCC

THERMAL CHARACTERISTICS: θja

28-Pin PLCC	65°C/W

CAUTION: Use handling procedures necessary for a static sensitive component.

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32P541C		
28-Pin PLCC	32P541C-CH	32P541C-CH

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914

Notes:

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SSI 32P3013
Pulse Detector with Programmable Filter

November 1993

DESCRIPTION

The SSI 32P3013 is a bipolar integrated circuit that provides all the data processing for pulse detection and four-burst servo capture from encoded read signals. This device can handle a NRZ data rate of 64 Mbit/s.

The SSI 32P3013 includes an AGC amplifier with AGC charge pump, a programmable 7-pole Bessel low pass filter, a pulse qualification circuit, and a 4-burst servo capture circuit. Automatic AGC control maintains a constant signal level into the pulse qualifier, and achieves fast write-to-read recovery. A time differentiator is included in the servo signal path, if so needed.

Ideal for constant density recording applications, the SSI 32P3013 low pass filter has a programmable 9-27 MHz bandwidth and 0-13 dB boost for pulse slimming. A time derivative of the read signal is also provided by the filter for time qualification in peak detection.

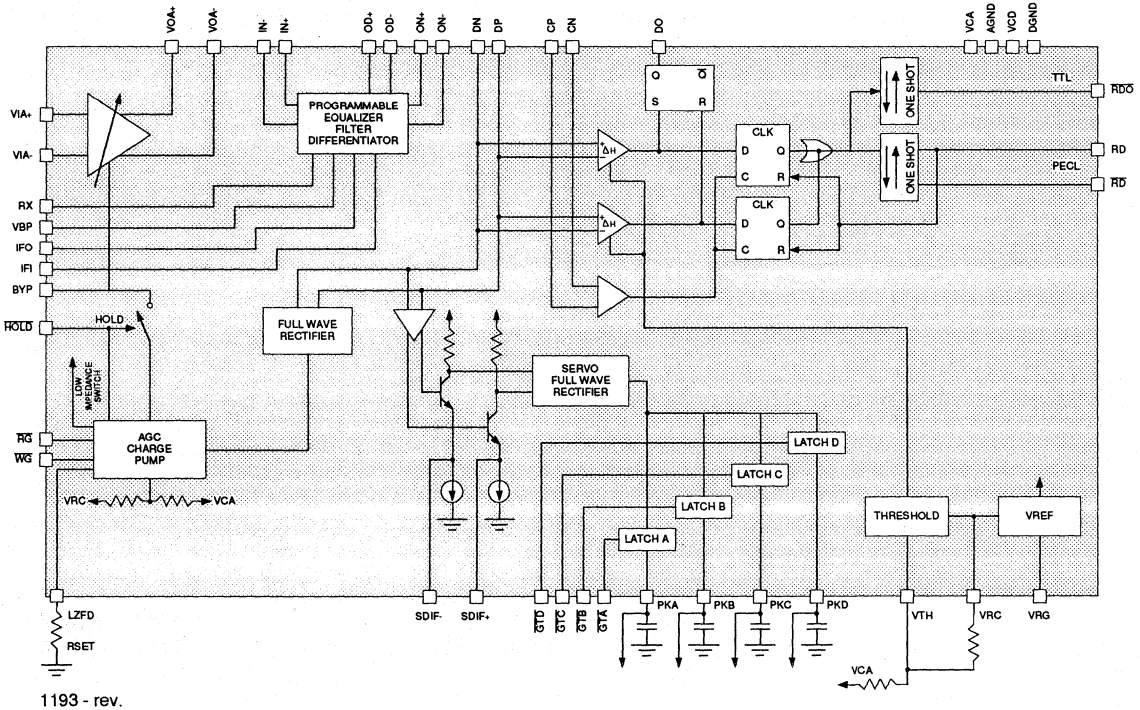
The SSI 32P3013 requires only a +5V power supply and is available in a 44-lead SOM package.

FEATURES

- Compatible with 64 Mbit/s data rate operation
- Fast Attack/Decay modes for rapid AGC recovery
- Automatic AGC actions: Low Drift AGC hold, fast AGC recovery, and low AGC input impedance control signals
- Includes programmable pulse slimming equalization and programmable channel filter and differentiator with no external filter components
- ±0.5 ns filter group delay variation from 0.3 FC to FC, FC = 27 MHz
- Independent positive and negative threshold qualification to suppress error propagation
- 0.5 ns max pulse pairing
- Servo differentiator and 4-burst servo capture
- +5V only operation
- 44-lead SOM package

4

BLOCK DIAGRAM



1193 - rev.

SSI 32P3013
Pulse Detector with Programmable Filter

FUNCTIONAL DESCRIPTION

The SSI 32P3013 Pulse Detector/Filter with 4-Burst Servo Capture is designed to support a 64 Mbit/s NRZ data rate. The signal processing circuits include a wide band variable gain amplifier, a sophisticated dual-rate AGC charge pump, a programmable electronic filter, a pulse qualifier, a servo differentiator and a 4-burst servo capture circuit.

Modes of Operation

The SSI 32P3013 can operate in one of three modes as controlled by $\overline{RG}$ and $\overline{WG}$.

Normal Read Mode $\overline{RG}$ = 0, $\overline{WG}$ = 1

In the normal Read Mode, the AGC actions are active. The AGC amplifier processes the input signal pulses; one-shot pulses are generated at the RD and $\overline{RD}$ outputs for each qualified signal peak. The $\overline{RDO}$ output buffer, which is a TTL buffer of the RD/$\overline{RD}$, is disabled and its output is pulled up high to reduce jitter and noise.

Servo Read Mode $\overline{RG}$ = 1, $\overline{WG}$ = 1

In the servo Read Mode, the AGC actions remain active (See note 1). The servo signal is amplified, fullwave rectified, differentiated and gated to the proper peak capture capacitor. The pulse qualifier remains active, and the $\overline{RDO}$ output is active to aid in servo decode.

Write Mode $\overline{RG}$ = X, $\overline{WG}$ = 0

In the Write Mode, the AGC actions are suspended. The AGC amplifier input impedance is clamped low to facilitate fast recovery. The $\overline{RDO}$ output is disabled and pulled up high to reduce jitter and noise.

AGC Amplifier

The wide band AGC amplifier amplifies the read signal from the read/write pre-amp to a signal level acceptable at the pulse qualifier. The AGC amplifier gain is an exponential function of the BYP voltage when referenced to VR.

$$Av = Ao \exp[\frac{(V_{BYP} - VR)}{K}] \quad \text{(See note 2)}$$

AGC Actions

The AGC loop maintains a constant DP/DN signal level at a nominal level, ~1 Vppd. The AGC actions are current charging and discharging to/from the external BYP integrating capacitor, and are classified into the following modes:

Normal Read and Servo Read Mode ($\overline{RG}$ = X, $\overline{WG}$ = 1)

Slow Decay: When the DP/DN signal is below 1 Vppd, a slow decay current, Id, charges the BYP capacitor. The AGC amplifier gain is increased slowly. This slow decay current tracks with the bandwidth of the filter. Id = 0.008 x IFI. At T = 27°C, the typical Id is 4.8 µA when the filter cutoff frequency is 27 MHz.

Slow Attack: When the DP/DN signal exceeds 1 Vppd, but is below 1.25 Vppd, a slow attack current, Ich, discharges the BYP capacitor. The AGC amplifier gain is decreased. The slow attack current is 20 times that of the slow decay current. Thus, for a given BYP capacitor, the slow attack response time is quicker than the slow decay response.

Fast Attack: When the DP/DN signal exceeds 1.25 Vppd, the device enters a Fast Attack mode. A fast attack current, Ichf, discharges the BYP capacitor. The AGC amplifier gain is quickly lowered. The fast attack current is seven times that of the slow attack current.

In servo Read Mode, constant AGC amplifier gain is generally desirable. Without an external AGC hold control, the servo data amplitude should be made lower than that of the data signal prior to the servo read mode. The SSI 32P3013 then enters the slow decay mode, which has a very slow effect on the AGC amplifier gain.

Write Mode ($\overline{RG}$ = X, $\overline{WG}$ = 0)

In the Write mode, the AGC charge pump is disabled. This holds the AGC amplifier gain at its previous value.

Notes:

1. The servo signal should have a lower amplitude than the data signal prior to the servo Read mode. Servo read should be completed before and significant change in AGC amplifier gain is resulted from the slow decay AGC mode.

2. In a closed AGC loop, the sensitivity of Ao and K to typical process variations is irrelevant. The typical values of Ao and K are provided for reference only, and not tested in production. Ao = 11, K = 0.22, VR = 3.6.

Write-to-Read Transition ($\overline{RG}$ = X, $\overline{WG}$ = 0-to-1)

When the SSI 32P3013 switches from the write to Read mode, i.e., $\overline{WG}$ 0-to-1 transition, the device remains in the low input impedance state for a preset time period, TLZ. For the next time period, TFD, the device then enters either the fast decay or Attack mode depending on the signal level at the DP/DN pins. The time periods are determined by an external resistor, RT, from the LZ/FD pin to ground.

TLZ (μs) = RT/78-0.26

TFD (μs) = RT/37-0.85, where RT is in kΩ.

RT must be greater than 45 kΩ.

Programmable Filter

The SSI 32P3013 includes a programmable low pass filter following the AGC amplifier for (1) 2X voltage gain from the AGC amplifier output to the pulse qualifier input, (2) noise limiting, (3) pulse slimming, and (4) provision of a time differentiated signal. The low pass filter is of a 7-pole 2-zero Bessel type. The filter's unboosted -3 dB bandwidth, defined as the cutoff frequency, is programmable from 9-27 MHz; the high frequency equalization is programmable from 0-13 dB at the cutoff frequency.

The filter input is ac-coupled from the AGC amplifier output. The filter's normal low pass output is ac-coupled to the data channel of the pulse qualifier. The differentiated low pass output is ac-coupled to the time channel of the pulse qualifier.

The normalized 7-pole 2-zero Bessel filter transfer function is given in Figure 1.

The cutoff frequency, fc, is programmable with 3 pins: RX, IFO and IFI. At the RX pin, an external resistor to ground establishes a reference current:

$$IFO = \frac{0.75}{Rx}, \text{at } T = 27°C$$

IFI should be made proportional to IFO for fc temperature stability. The cutoff frequency is related to the RX resistor, IFO and IFI currents as the following:

$$fc(MHz) = 27 \cdot \frac{IFI}{IFO} \cdot \frac{1.25}{Rx(k\Omega)}$$

For a fixed cutoff frequency setting, IFO and IFI can be tied together. The cutoff frequency equation then reduces to:

$$fc(MHz) = 27 \cdot \frac{1.25}{Rx(k\Omega)}$$

For programmable cutoff frequency, an external current DAC can be used. IFO should be the reference current into the DAC. The DAC output current drives IFI, which is then proportional to the IFO. The DACF in the SSI 32D4661 Time Base Generator is designed to control fc of the Silicon Systems programmable filters. When the DACF, which has a 4X current gain from its reference to fullscale output, is used, 5 kΩ RX is used. The fc is then given by:

$$fc(MHz) = 27 \cdot \frac{F\_Code}{127}$$

where F_Code is the decimal code equivalent to the 7-bit input into the DACF.

The high frequency equalization is programmable with two pins: VRG and VBP. The VRG is a bandgap reference voltage, 2.3V typically. The voltage at the VBP pin determines the amount of high frequency boost at the cutoff frequency. The boost function is as follows:

$$Boost(dB) = 20\log_{10}[(\frac{Kb \cdot VBP}{VRG}) + 1]$$

$$Kb = 3.041 + 0.0276 \cdot fci$$

where fci is the ideal cutoff frequency in MHz.

For a fixed boost setting, a resistor divider between VRG to ground can be used with the divided voltage at the VBP pin. For programmable equalization, an external voltage DAC can be used. VRG should be the reference voltage to the DAC. The DAC output voltage is then proportional to the VRG. The DAC in the SSI 32D4661 is designed to control the magnitude equalization of Silicon Systems programmable filters.

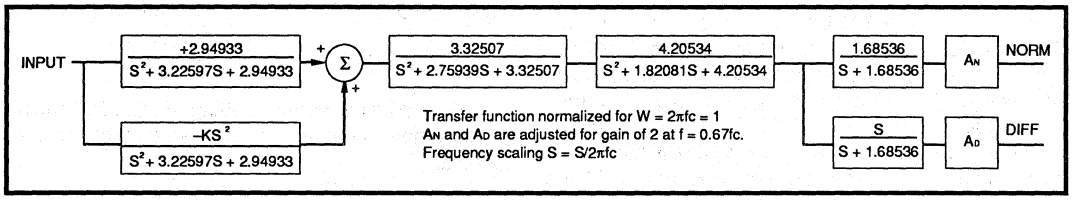


FIGURE 1: Bessel Filter Transfer Function

$$K = 2.94933\,(10^{\frac{BOOST(dB)}{20}} - 1)$$

TABLE 1: Typical Change in f - 3 dB Point with Boost

Boost (dB)	Gain@*f*c (dB)	Gain@peak (dB)	*f*Peak/fc	*f*-3dB/fc	K
0	-3	0.00	no peak	1.00	0
1	-2	0.00	no peak	1.20	0.36
2	-1	0.00	no peak	1.47	0.76
3	0	0.15	0.62	1.74	1.22
4	1	1.00	1.08	1.96	1.73
5	2	2.12	1.24	2.13	2.30
6	3	3.35	1.24	2.28	2.94
7	4	4.56	1.39	2.42	3.65
8	5	5.82	1.39	2.54	4.46
9	6	7.04	1.39	2.66	5.36
10	7	8.24	1.39	2.77	6.38
11	8	9.41	1.39	2.88	7.52
12	9	10.55	1.39	2.98	8.79
13	10	11.70	1.55	3.08	10.22

Notes: 1. *f*c is the original programmed cutoff frequency with no boost.
2. *f* - 3 dB is the new -3 dB value with boost implemented.
3. *f*peak is the frequency where the magnitude peaks with boost implementd.

e.g., *f*c = MHz when boost = 0 dB
if boost is programmed to 5 x dB then *f* - 3 dB = 27.69 MHz
*f*peak = 16.12 MHz

When DACs are used, the boost relation then reduces to:

$$\text{Boost(dB)} = 20\log_{10}[(Kb \bullet \frac{S\_Code}{127}) + 1]$$

Pulse Qualification

The SSI 32P3013 validates each DP/DN peak by a combination of level qualification and time qualification. In level qualification, a dual-comparator threshold detection eliminates errors due to low level additive noise. In time qualification, the filter's differentiated output is used to locate signal peaks.

Level Qualification

The dual-comparator architecture allows independent detection for positive and negative peaks. One comparator detects a positive peak by comparing the data signal with a positive threshold. The other comparator detects a negative peak by comparing the data signal with a negative threshold. Each comparator has a small hysteresis, 20% of the set threshold, to help qualify signals which just clear the set threshold.

The SSI 32P3013 comparator thresholds are set by a DC voltage at the VTH pin, such as from a resistor divider from VCA to VRC (see note 3). The threshold at each comparator can be computed as: Hysteresis Gain x (VTH - VRC). The thresholds at the two comparators are of the same magnitude, but of opposite polarity.

The SSI 32P3013 has three sets of pulse detector outputs: RD/$\overline{RD}$, $\overline{RDO}$, and DO. RD/$\overline{RD}$ output is the pseudo-ECL differential output. Corresponding to each validated peak of the DP/DN signal, a one-shot pulse occurs at the RD/$\overline{RD}$ output. The pulse width of the one-shot pulse is determined by an internal timing circuit, and specified in the electrical specification.

$\overline{RDO}$ is the TTL output of the pulse detector, logically equivalent to RD/$\overline{RD}$. Again, a one-shot pulse occurs at the $\overline{RDO}$ output for each validated peak of the DP/DN signal. The pulse width of this one-shot pulse is also specified in the electrical specification. The DO output is a test point used to monitor the output of the internal comparators, it is an open-emitter output requiring a 5 kΩ external resistor pull-down to ground.

Four-Burst Servo Differentiator and Capture

The SSI 32P3013 supports advanced embedded 4-burst servo technique. The signal at the DP/DN input can be time differentiated, fullwave rectified, and gated onto the selected peak capture output. A peak capture output is selected by pulling its corresponding $\overline{GT}$ x to logic '0.'

The transfer function from the DP/DN to the servo fullwave rectifier input is:

$$Av = \frac{2380Cs}{LCs^2 + (R + 48.1)Cs + 1}$$

where: R, L, and C are external passive components across SDIF±

$$15\ pF < C < 125\ pF$$
$$s = jw$$

When the time differentiation function is not desired, a 2 kΩ resistor should be used across the SDIF± pins.

The transfer function from the servo fullwave rectifier input to the peak capture output is set so that a 1 Vppd DP/DN signal produces 0.95 Vpeak output. With no signal input, the outputs are set close to ground, with a finite offset common to all four channels.

Note 3: VCA is the +5V supply. VRC is the bandgap voltage referenced from VCA, i.e., VRC = VCA - VRG.

PIN DESCRIPTION

INPUT PINS

NAME	TYPE	DESCRIPTION
VIA+, VIA-	I	AGC Amplifier input pins.
IN+, IN-	I	Equalizer/filter input pins.
DP, DN	I	Data inputs to data comparators and fullwave rectifier.
CP, CN	I	Differentiated data inputs to the clock comparator.
VTH	I	Threshold level setting input for the data comparators.
$\overline{WG}$	I	TTL compatible input. When low the device is in Write Mode.

PIN DESCRIPTION (continued)

INPUT PINS

NAME	TYPE	DESCRIPTION
$\overline{RG}$	I	TTL compatible input. When low, the device is in normal Read Mode.
$\overline{WG}$	I	TTL compatible input. When low, the device is in Write Mode. When both $\overline{RG}$ and $\overline{WG}$ are high, the device is in Servo Mode.
$\overline{GTA}$, $\overline{GTB}$, $\overline{GTC}$, $\overline{GTD}$	I	TTL compatible input. When low the corresponding servo gate channel is enabled.
$\overline{HOLD}$	I	TTL compatible input. When low the AGC action is suspended.
OUTPUT PINS		
VOA+, VOA-	O	AGC amplifier output pins.
ON+, ON-	O	Equalizer/filter normal output pins.
OD+, OD-	O	Equalizer/filter differentiated output pins.
DO	O	ECL compatible data comparator latch output pin.
RD, $\overline{RD}$	O	ECL compatible read data output pins.
$\overline{RDO}$	O	TTL compatible read data output.
SDIF+, SDIF-	-	Pins for external differentiating network for servo data.
PKA, PKB PKC, PKD	O	Open non emitter outputs that provide a fullwave rectified signal from the servo differentiator. These outputs are referenced to AGND. These outputs are high impedance when not enabled by $\overline{GTX}$
ANALOG PINS		
VRC	-	Reference voltage pin for SERVO and LEVEL. VRC is referenced to VCA.
VRG	-	Reference voltage pin for the programmable filter.VRG is referenced to ground.
VBP	-	The equalizer high frequency boost is set by an external voltage applied to this pin. VBP must be proportional to VRG. Programmable boost is implemented by using a DAC that uses VRG as its reference. A fixed amount of boost can be set by an external resistor divide network connected from VBP to VRG and GND.
RX	-	Pin to set filter reference current. External resistor Rx from this pin to ground sets the filter reference current IFO.
IFO	-	Reference current output pin. The reference current is normally supplied as the reference current to a current DAC which generates the programmable input current for the IFI pin.
IFI	-	Programmable filter input current pin. The filter cutoff frequency is proportional to the current into this pin. The current must be proportional to the reference current out of IFO. A fixed filter cutoff frequency is generated by connecting IFO to IFI and selecting Rx to set the desired frequency.
LZ/FD	-	Pin for external resistor to set timing for both Low-Z input and Fast Decay modes.
BYP	-	The AGC integrating capacitor C_A is connected between BYP and VCA.
VCA, VCD	-	Analog and Digital +5 volts.
AGND, DGND	-	Analog and Digital grounds.

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, 4.5V < VCC < 5.5V, 0°C < Ta < 70°C

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may damage the device.

PARAMETER	RATING
Storage Temperature	-65 to +150°C
Junction Operating Temperature,Tj	+130°C
Supply Voltage, VCA, VCD	-0.7 to 7V
Voltage Applied to Inputs	-0.7 to VCA + 0.7V, -0.7 to VCD + 0.7V

RECOMMENDED OPERATING CONDITIONS

PARAMETER	RATING
Supply Voltage VCA = VCD = VCC	4.5V < VCC < 5.5V
Ambient Temperature, Ta	0°C < Ta < 70°C

POWER SUPPLY

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
PD	Power Dissipation	Outputs unloaded 4.5V < VCA, VCD < 5.5V		420	600	mW

LOGIC SIGNALS

VIL	TTL Input Low Voltage		-0.3		0.8	V
VIH	TTL Input High Voltage		2.0		VCC + 0.3	V
IIL	TTL Input Low Current	VIL = 0.4V	-0.4			mA
IIH	TTL Input High Current	VIH = 2.7V			0.1	mA
VOHE	ECL Output High Voltage		VCC -1.02		VCC -0.4	V
VES	ECL Differential Output Swing		0.3		0.6	V
TRF	EC1 Output Rise and Fall Time	CL ≤ 10 pF			3.5	ns
TS	Control Input Switching Times				0.1	µs
VOLT	TTL Output Low Voltage	IOL = 4 mA	0.5			V
VOHT	TTL Output High Voltage	IOH = -400 mA			2.7	V

ELECTRICAL SPECIFICATIONS (continued)

AGC AMPLIFIER

The input signals are AC coupled to VIA+ and VIA-. VOA+ and VOA- are AC coupled to IN+ and IN-. ON+ and ON- are AC coupled to DP and DN. Ca 1000 pF. Fin = 4 MHz. Unless otherwise specified, the output is measured differentially at VOA+ and VOA-.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
VIB	Input Range	Filter boost at fc = 0 dB	24		240	mVppd
		Filter boost at fc = 11 dB	20		100	mVppd
VD	DP-DN Voltage	VIA± = 0.1 Vppd	0.90		1.10	Vppd
VDV	DP-DN Voltage Variation	24 mVppd < VIA± < 240 mVppd			8.0	%
AV	Gain Range		2.0		28	V/V
AVPV	Gain Sensitivity w.r.t. BYP Voltage			38		dB/V
DR	VOA+ VOA- Dynamic Range	THD = 1% max, Vin = 24 mVp-p	0.75			Vppd
		THD = 2% max, Vin = 240 mVp-p				
RINDA	Differential Input Impedance	$\overline{WG}$ = 1	3.7	5.2	7.4	kΩ
RINSA	Single Ended Input Impedance	$\overline{WG}$ = 1		2.6		kΩ
		$\overline{WG}$ = 0		80		Ω
VOS	Differential Output Offset Variation	from min. gain to max. gain	-200		+200	mV
VIN	Input Referred Noise Voltage	gain = max, Rs = 0Ω filter not connected to VOA+ and VOA-, BW = 15 MHz		14	20	nV/√Hz
BW	Bandwidth	No AGC action, Gain = 22	50	70		MHz
CMRR	Common Mode Rejection Ratio	gain = 22, Vin = 0 VDC + 100 mVpp @ 5 MHz	40	62		dB
PSRR	Power Supply Rejection Ratio	gain = 22, 100 mVpp @ 5 MHz on VCA, VCD	45	57		dB
TGD	Gain Decay Time	VIA± = 120 mV to 240 mV VOA± < 0.9 Final Value IFI = 600 µA		25		µs
TGA	Gain Attack Time	VIA± = 120 mV to 240 mV VOA± < 1.1 Final Value IFI = 600 µA		25		µs

AGC CONTROL

The input signals are AC coupled to DP and DN. Ca = 1000 pF, 110 µA < IFI < 600 µA.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
ID	Discharge Current	$\overline{WG}$ = 1, DP - DN = 0V		0.008 x IFI		A
IDF	Fast Discharge Current			20 x Id		A
ICH	Charge Pump Attack Current	$\overline{WG}$ = 1, DP - DN = 0.55V		40 x Id		A
ICHF	Charge Pump Fast Attack Current, Ichf	$\overline{WG}$ = 1, DP - DN = 0.675V		7 x Ich		A
IK	BYP Pin Leakage Current	$\overline{WG}$ or $\overline{HOLD}$ = 0, VBYP = VCC - 1.5V	-0.1		+0.1	µA
VRC	VRC Reference Voltage			VCA -VRG		V
IVRC	VRC Output Drive		-0.75		+0.75	mA
VRG	VRG Reference Voltage	Isource 0 mA to 1 mA	2.2		2.45	V
TLZ	Low-Z Timing Accuracy	TLZ (µs) = RT(kΩ)/78-0.26, RT > 45 kΩ	-40		+40	%
TFD	Fast Decay Timing Accuracy	TFD (µs) = RT(kΩ)/37-0.85, RT > 45 kΩ	-40		+40	%

EQUALIZER/FILTER

The input signals are AC coupled to IN+ and IN-.

fc	Filter Cutoff Frequency	RX = 5 kΩ *fc* = 27 x IFI/(4 x IFO) MHz 4 ≥ IFO/IFI ≥ 4/3	9		27	MHz
IFO	IFO Reference Current	IFO = 0.75/RX; Tj = 27°C 5 kΩ > RX > 1.25 kΩ	0.15		0.6	mA
IFI	IFI Program Current Range	Tj = 27°C, 27 MHz > *fc* > 9 MHz	0.2		0.6	mA
FCA	FCA Filter FC Accuracy	*fc* = 27 MHz	-13		13	%
RX	RX Range		1.25		5	kΩ
AO	Normal Low Pass Gain AO = (ON ±) / (IN±)	Fin = 0.67*fc*	1.4		2.2	V/V
AD	Differentiated Low Pass Gain AD = (OD ±) / (IN±)	Fin = 0.67*fc*	0.8AO		1.2AO	V/V
FBA	Frequency Boost Accuracy	VBP = VRG	-1.5		+1.5	dB
		VBP/VRG = 0.5	-1.0		+1.0	dB

EQUALIZER/FILTER (continued)
The input signals are AC coupled to IN+ and IN-.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TGD1	Group Delay Variation	fc = 27 MHz, VBP = 0 to VRG fc > Fin > 0.3 fc	-0.7		+0.7	ns
TGD2		fc = 9 to 27 MHz, VBP = 0 to VRG fc > Fin > 0.3 fc	-2.5		+2.5	%
VOSVF	Output Offset Voltage Variation	200 µA < IFI < 600 µA	-200		200	mV
DRF	VOF Filter Output Dynamic Range	Fin = 0.67 fc THD = 1.5% max, ON± THD = 2.5% max, OD±	1.2			Vpp
RINF	Filter Input Resistance		3.0	3.9		kΩ
CINF	Filter Input Capacitance				7	pF
ROF	Filter Output Resistance	IO+ = 1.0 mA		30	60	Ω
IOF	Filter Output Current		-1.0		1.0	mA
VNN	Eout Output Noise Voltage; ON+, ON-	BW = 100 MHz, RS = 50Ω VBP = 0, fc = 27 MHz		2.8	5.0	mVRms
		BW = 100 MHz, RS = 50Ω VBP = VRG, fc = 27 MHz		5.8	8.5	mVRms
VND	Eout Output Noise Voltage; OD+, OD-	BW = 100 MHz, RS = 50Ω VBP = 0, fc = 27 MHz		5.2	7.5	mVRms
		BW = 100 MHz, RS = 50Ω VBP = VRG, fc = 27 MHz		15.0	21.0	mVRms

DATA COMPARATOR
The input signals are AC coupled to DP and DN.

RIND	Differential Input Resistance		8	9.6	14	kΩ
CIND	Differential Input Capacitance			2	5	pF
VOSD	Comparator Offset Voltage (Note 1)				4	mV
HYS	Threshold Voltage Gain	VTH - VRC = 0.3V	0.40		0.52	V/V
		VTH - VRC = 0.9V	0.42		0.49	V/V
VSH	Threshold Voltage Hysteresis (Note 1)			.20 x GHYS x (VTH -VRC)		V/V
TPDD	Propagation Delay	To DO		6		ns
IVTH	VTH Input Bias Current				2	µA

Note 1: Not directly measureable

CLOCKING

The input signals are AC coupled to CP and CN.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
VOSC	Comparator Offset Voltage (Note 1)				4	mV
RINC	Differential Input Resistance		8	9.7	14	kΩ
CINC	Differential Input Capacitance			1.4	5	pF
TDS	D Flip-Flop Set Up Time	DP-DN threshold to CP-CN zero cross, CP-CN = 1 Vppd at 18 MHz		0.3	1	ns
PP	Pulse Pairing	Vs = 1 Vpp, F = 18 MHz		0.1	0.5	ns
TPDC	Propagation Delay from CP-CN zero crossing to RD	Vs = 20 mVpp square wave		8		ns
PWRD	RD Output Pulse Width		10		16	ns
PWRT	$\overline{RDO}$, TTL Output Pulse Width		30		45	ns

SERVO DIFFERENTIATOR/FULL-WAVE RECTIFIER

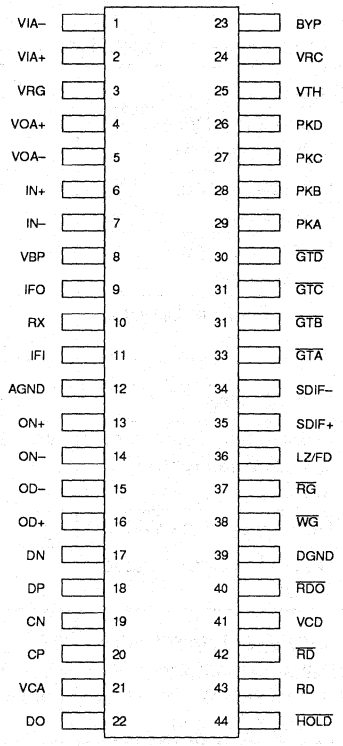
An external series network with R = 600Ω, C = 27 pF, L = 22 µF is connected between SDIF and $\overline{SDIF}$ to determine the servo differentiator transfer function. The input signals are AC coupled to DP and DN. Fin = 6.7 MHz at 1.0 Vppd.

ISDIF	SDIF+ to SDIF- pin current	Differentiator impedance must be set so as not to dip the signal for this level	1.4	2.0	2.6	mA
RDIF	Internal differentiator pull-up resistors	Cannot be directly tested	0.4	0.6	0.8	kΩ
FWR	Input voltage range to maintain FWR voltage gain	Cannot be directly tested	0.1		2.0	Vppd
RERR	Rectification Error		-10		10	%
AFWR	FWR Voltage Gain from DP/DN Inputs to PKA-D Outputs	0.1 Vppd ≤ V(DP/DN) ≤ 1.0 Vppd V(PKx) = 0.09+ 0.096 V(DP/DN), Fin = 4 MHz	-20		20	%
ISL	Servo Output Leakage Current	Channel disabled		0.1	1	µA
VCOS	PKA-D Channel to Channel Offset	1 Vppd input to DP/DN PKA-PKB, PKC-PKD	-10		+10	mV
VAOS	PKA-D Absolute Offset Magnitude	1 Vppd input to DP/DN (across all channels)	0		20	mV

Note 1: Not directly measureable

SSI 32P3013
Pulse Detector with Programmable Filter

PACKAGE PIN DESIGNATIONS
(Top View)



44-Lead SOM

CAUTION: Use handling procedures necessary for a static sensitive component.

THERMAL CHARACTERISTICS: θjA

44-Lead SOM	70°C/W

ORDERING INFORMATION

PART DESCRIPTION	ORDER NUMBER	PACKAGE MARK
SSI 32P3013 40-Lead SOM	32P3013-CM	32P3013-CM

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914

silicon systems®
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SSI 32P3015/3016
Pulse Detector with Programmable Filter
Advance Information

October 1993

DESCRIPTION

The SSI 32P3015/3016 is a bipolar integrated circuit that provides all the data processing for pulse detection and four-burst servo capture from encoded read signals. This device can handle a NRZ data rate of 72 Mbit/s.

The SSI 32P3015/3016 includes an AGC amplifier with AGC charge pump, a programmable 7-pole Bessel low pass filter, a pulse qualification circuit, and a 4-burst servo capture circuit. Automatic AGC control maintains a constant signal level into the pulse qualifier, and achieves fast write-to-read recovery. A time differentiator is included in the servo signal path, if so needed. The 32P3016 also has a level pin output.

Ideal for constant density recording applications, the SSI 32P3015/3016 low pass filter has a programmable 9-27 MHz bandwidth and 0-13 dB boost for pulse slimming. A time derivative of the read signal is also provided by the filter for time qualification in peak detection.

The SSI 32P3015/3016 requires only a +5V supply voltage and are available in a 48-pin TQFP package. The 32P3015 is also available in a 44-pin SOM package.

FEATURES

- **Compatible with 72 Mbit/s data rate operation**
- **Fast attack/decay modes for rapid AGC recovery**
- **Automatic AGC actions: Low Drift AGC hold, fast AGC recovery, and low AGC input impedance control signals**
- **Includes programmable pulse slimming equalization and programmable channel filter and differentiator with no external filter components**
- **±0.5 ns filter group delay variation from 0.3FC to FC = 27 MHz**
- **Independent positive and negative threshold qualification to suppress error propagation**
- **0.5 ns max pulse pairing**
- **Servo differentiator and 4-burst servo capture**
- **+5V only operation**
- **48-pin TQFP package, 44-pin SOM 32P3015 only**

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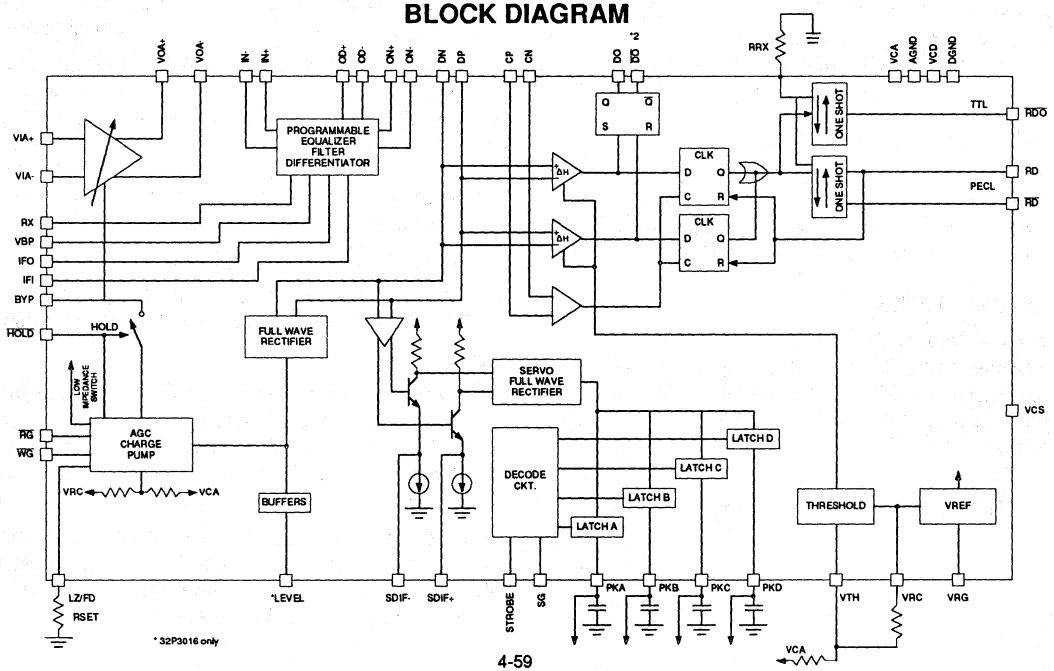
BLOCK DIAGRAM



SSI 32P3015/3016
Pulse Detector with Programmable Filter

FUNCTIONAL DESCRIPTION

The SSI 32P3015/3016 Pulse Detector/Filter with 4-Burst Servo Capture is designed to support a 72 Mbit/sNRZ data rate. The signal processing circuits include a wide band variable gain amplifier, a sophisticated dual-rate AGC charge pump, a programmable electronic filter, a pulse qualifier, a servo differentiator and a 4-burst servo capture circuit.

MODES OF OPERATION

The SSI 32P3015/3016 can operate in one of three modes as controlled by RG, WG, and SG.

Normal Read Mode RG = 0, WG = 1, SG = X

In the normal Read Mode, the AGC actions are active. The AGC amplifier processes the input signal pulses; one-shot pulses are generated at the RD and RD outputs for each qualified signal peak. The RDO output buffer, which is a TTL buffer of the RD/RD, is disabled and its output is pulled up high to reduce jitter and noise.

Servo Read Mode RG = 1, WG = 1, SG = 1

In the servo Read Mode, the AGC actions remain active (See note 1). The servo signal is amplified, fullwave rectified, differentiated and gated to the proper peak capture capacitor. The pulse qualifier remains active, and the RDO output is active to aid in servo decode.

Write Mode RG = X, WG = 0, SG =X

In the Write Mode, the AGC actions are suspended. The AGC amplifier input impedance is clamped low to facilitate fast recovery. The RDO output is disabled and pulled up high to reduce jitter and noise.

AGC AMPLIFIER

The wide band AGC amplifier amplifies the read signal from the read/write pre-amp to a signal level acceptable at the pulse qualifier. The AGC amplifier gain is an exponential function of the BYP voltage when referenced to VR.

$$Av = Ao \exp[\frac{(V_{BYP} - VR)}{K}] \quad \text{(See note 2)}$$

AGC ACTIONS

The AGC loop maintains a constant DP/DN signal level at a nominal level, ~1 Vppd. The AGC actions are current charging and discharging to/from the external BYP integrating capacitor, and are classified into the following modes:

Normal Read and Servo Read Mode

($\overline{RG}$ = X, $\overline{WG}$ = 1) SG = X

Slow Decay: When the DP/DN signal is below 1 Vppd, a slow decay current, Id, charges the BYP capacitor. The AGC amplifier gain is increased slowly. This slow decay current tracks with the bandwidth of the filter. Id = 0.008 x IFI. At T = 27°C, the maximum Id is 4.5 µA when the filter cutoff frequency is 27 MHz.

Slow Attack: When the DP/DN signal exceeds 1 Vppd, but is below 1.25 Vppd, a slow attack current, Ich, discharges the BYP capacitor. The AGC amplifier gain is decreased. The slow attack current is 20 times that of the slow decay current. Thus, for a given BYP capacitor, the slow attack response time is quicker than the slow decay response.

Fast Attack: When the DP/DN signal exceeds 1.25 Vppd, the device enters a fast attack mode. A fast attack current, Ichf, discharges the BYP capacitor. The AGC amplifier gain is quickly lowered. The fast attack current is seven times that of the slow attack current.

In servo Read Mode, constant AGC amplifier gain is generally desirable. Without an external AGC hold control, the servo data amplitude should be made lower than that of the data signal prior to the servo read mode. The SSI 32P3015/3016 then enters the slow decay mode, which has a very slow effect on the AGC amplifier gain.

Write Mode ($\overline{RG}$ = X, $\overline{WG}$ = 0) SG = X

In the write mode, the AGC charge pump is disabled. This holds the AGC amplifier gain at its previous value.

Notes:

1. The servo signal should have a lower amplitude than the data signal prior to the servo read mode. Servo read should be completed before and significant change in AGC amplifier gain is resulted from the slow decay AGC mode.

2. In a closed loop, the sensitivity of Ao and K to typical process variations is irrelevant. The typical values of Ao and K are provided for reference only, and not tested in production. A0 = 11, K = 0.22, VR = 3.6.

Write-to-Read Transition ($\overline{RG}$ = X, $\overline{WG}$ = 0-to-1) SG = X

When the SSI 32P3015/3016 switches from the write to read mode, i.e., $\overline{WG}$ 0-to-1 transition, the device remains in the low input impedance state for a preset time period. For the next time period, the device then enters either the fast decay or attack mode depending on the signal level at the DP/DN pins. The time period, t, is determined by an external resistor, RT, from the LZ/FD pin to ground.

$$\tau(\mu s) = \frac{RT(k\Omega)}{28}$$

For example, with RT = 38 kΩ, each time period is 1.36 µs.

PROGRAMMABLE FILTER

The SSI 32P3015/3016 includes a programmable low pass filter following the AGC amplifier for (1) 2X voltage gain from the AGC amplifier output to the pulse qualifier input, (2) noise limiting, (3) pulse slimming, and (4) provision of a time differentiated signal. The low pass filter is of a 7-pole 2-zero Bessel type. The filter's unboosted -3 dB bandwidth, defined as the cutoff frequency, is programmable from 9-27 MHz; the high frequency equalization is programmable from 0-13 dB at the cutoff frequency.

The filter input is ac-coupled from the AGC amplifier output. The filter's normal low pass output is ac-coupled to the data channel of the pulse qualifier. The differentiated low pass output is ac-coupled to the time channel of the pulse qualifier.

The normalized 7-pole 2-zero Bessel filter transfer function is given in Figure 1.

The cutoff frequency, fc, is programmable with 3 pins: RX, IFO and IFI. At the RX pin, an external resistor to ground establishes a reference current:

$$IFO = \frac{0.75}{Rx}, \text{at } T = 27°C$$

IFI should be made proportional to IFO for fc temperature stability. The cutoff frequency is related to the RX resistor, IFO and IFI currents as the following:

$$fc(MHz) = 27 \cdot \frac{IFI}{IFO} \cdot \frac{1.25}{Rx(k\Omega)}$$

For a fixed cutoff frequency setting, IFO and IFI can be tied together. The cutoff frequency equation then reduces to:

$$fc(MHz) = 27 \cdot \frac{1.25}{Rx(k\Omega)}$$

For programmable cutoff frequency, an external current DAC can be used. IFO should be the reference current into the DAC. The DAC output current drives IFI, which is then proportional to the IFO. The DACF in the SSI 32D4661 Time Base Generator is designed to control fc of the Silicon Systems programmable filters. When the DACF, which has a 4X current gain from its reference to fullscale output, is used, 5 kΩ RX is used. The fc is then given by:

$$fc(MHz) = 27 \cdot \frac{F\_Code}{127}$$

where F_Code is the decimal code equivalent to the 7-bit input into the DACF.

The high frequency equalization is programmable with two pins: VRG and VBP. The VRG is a bandgap reference voltage, 2.3V typically. The voltage at the VBP pin determines the amount of high frequency boost at the cutoff frequency. The boost function is as follows:

$$Boost(dB) = 20\log_{10}\left[\left(\frac{Kb \cdot VBP}{VRG}\right) + 1\right]$$

$$Kb = 3.041 + 0.0276 \cdot fci$$

where fci is the ideal cutoff frequency in MHz.

For a fixed boost setting, a resistor divider between VRG to ground can be used with the divided voltage at the VBP pin. For programmable equalization, an external voltage DAC can be used. VRG should be the reference voltage to the DAC. The DAC output voltage is then proportional to the VRG. The DAC in the SSI 32D4661 is designed to control the magnitude equalization of Silicon Systems programmable filters.

When DACs are used, the boost relation then reduces to:

$$Boost(dB) = 20\log_{10}\left[\left(Kb \cdot \frac{S\_Code}{127}\right) + 1\right]$$

PULSE QUALIFICATION

The SSI 32P3015/3016 validates each DP/DN peak by a combination of level qualification and time qualification. In level qualification, a dual-comparator threshold detection eliminates errors due to low level additive noise. In time qualification, the filter's differentiated output is used to locate signal peaks.

Level Qualification

The dual-comparator architecture allows independent detection for positive and negative peaks. One comparator detects a positive peak by comparing the data signal with a positive threshold. The other comparator detects a negative peak by comparing the data signal with a negative threshold. Each comparator has a small hysteresis, 20% of the set threshold, to help qualify signals which just clear the set threshold.

FUNCTIONAL DESCRIPTION (continued)

The SSI 32P3015/3016 comparator thresholds are set by a DC voltage at the VTH pin, such as from a resistor divider from VCA to VRC (see note 3). The threshold at each comparator can be computed as: Hysteresis Gain x (VTH - VRC). The thresholds at the two comparators are of the same magnitude, but of opposite polarity.

The SSI 32P3015/3016 has three sets of pulse detector outputs: RD/$\overline{RD}$, $\overline{RDO}$, and DO. RD/$\overline{RD}$ output is the pseudo-ECL differential output. Corresponding to each validated peak of the DP/DN signal, a one-shot pulse occurs at the RD/$\overline{RD}$ output. The pulse width of the one-shot pulse is determined by an internal timing circuit, and can be calculated by the equation below:

PWRD = 0.1 ns + (1.33 ns/kΩ) RRX

RDO is the TTL output of the pulse detector, logically equivalent to RD/$\overline{RD}$. Again, a one-shot pulse occurs at the RDO output for each validated peak of the DP/DN signal. The pulse width of this one-shot pulse is also specified in the electrical specification. DO output is a test point used to monitor the outputs of the internal comparators. It is an open-emitter output requiring a 5 kΩ external resistor pull-down to ground.

The 32P3016 has a level output which is an amplified peak capture of DP-DN. It can be computed as level gain x DP - DN ppd + VRC.

Four-Burst Servo Differentiator and Capture

The SSI 32P3015/3016 supports advanced embedded 4-burst servo technique. The signal at the DP/DN input can be time differentiated, fullwave rectified, and gated onto the selected peak capture output.

The transfer function from the DP/DN to the servo fullwave rectifier input is:

$$Av = \frac{2380\,Cs}{LCs^2 + (R + 48.1)Cs + 1}$$

where: R, L, and C are external passive components across SDIF±

$$15\ pF < C < 125\ pF$$

$$s = jw$$

When the time differentiation function is not desired, a 2 kΩ resistor should be used across the SDIF± pins.

The transfer function from the servo fullwave rectifier input to the peak capture output is set so that a 1 Vppd DP/DN signal produces 0.95 Vpeak output. With no signal input, the outputs are set close to ground, with little or no offset common to all four channels.

GTA, GTB, GTC, and GTD are now generated on-chip, using STROBE and SG as inputs. N.B.: There must be exactly 4 strobe pulses withing the TRUE time of SG.

A two-bit counter and 4 gates produce:

GTA from the first STROBE pulse,

GTB from the second STROBE pulse,

GTC from the third STROBE pulse,

GTD from the fourth STROBE pulse.

Resetting of PKA, PKB, PKC, and PKD must still be done externally.

VCS Pin: This is a third +5V pin, intended not to be switched off by the customer in order to power down.

VCS is used as the high-voltage tie point for the ESD diodes from the 5 TTL-level input pins:

1) STROBE
2) SG
3) $\overline{RG}$
4) $\overline{WG}$
5) $\overline{HOLD}$

The purpose of this is to make it impossible for one or more of the TTL-level input drives to attempt to support the chip, via ESD diodes, when VCC and VCD are switched off.

VCS also supports the held servo voltages at pins PKA, PKB, PKC, and PKD. This is done by using VCN as the +5V supply for SSIN, PKCTRLN (via VPB), and LSERVO.

RRX Pin: This pin connects to an external precision, low T-C resistor, which is used to set the discharge currents of the one-shots, OSE_A and OSE_B, which in turn determine the pulse widths of the TTL ouput pulse, $\overline{RDT}$, and of the ECL ouput pulses, RD and $\overline{RD}$. This permits adjustment of the pulse widths for different applications and/or for variations in on-chip capacitances, and reduces the pulse-width changes caused by "corner" conditions.

Note 3: VCA is the +5V supply. VRC is the bandgap voltage referenced from VCA, i.e., VRC = VCA - VRG.

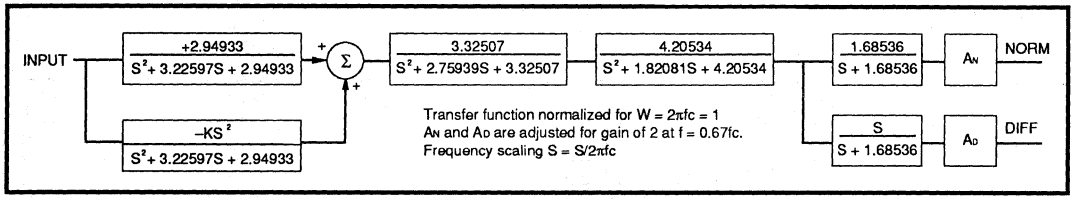


FIGURE 1: Bessel Filter Transfer Function

$$K = 2.94933\ (10^{\frac{BOOST\ (dB)}{20}} - 1)$$

4

TABLE 1: Typical Change in *f* - 3 dB Point with Boost

Boost (dB)	Gain@*fc* (dB)	Gain@peak (dB)	*f*Peak/*fc*	*f*-3dB/*fc*	K
0	-3	0.00	no peak	1.00	0
1	-2	0.00	no peak	1.20	0.36
2	-1	0.00	no peak	1.47	0.76
3	0	0.15	0.62	1.74	1.22
4	1	1.00	1.08	1.96	1.73
5	2	2.12	1.24	2.13	2.30
6	3	3.35	1.24	2.28	2.94
7	4	4.56	1.39	2.42	3.65
8	5	5.82	1.39	2.54	4.46
9	6	7.04	1.39	2.66	5.36
10	7	8.24	1.39	2.77	6.38
11	8	9.41	1.39	2.88	7.52
12	9	10.55	1.39	2.98	8.79
13	10	11.70	1.55	3.08	10.22

Notes: 1. *fc* is the original programmed cutoff frequency with no boost.
2. *f* - 3 dB is the new -3 dB value with boost implemented.
3. *f*peak is the frequency where the magnitude peaks with boost implemented.

e.g., *fc* = 13 MHz when boost = 0 dB
if boost is programmed to 5 x dB then *f* - 3 dB = 27.69 MHz
*f*peak = 16.12 MHz

PIN DESCRIPTION

INPUT PINS

NAME	TYPE	DESCRIPTION
VIA+, VIA-	I	AGC Amplifier input pins.
IN+, IN-	I	Equalizer/filter input pins.
DP, DN	I	Data inputs to data comparators and fullwave rectifier.
CP, CN	I	Differentiated data inputs to the clock comparator.
VTH	I	Threshold level setting input for the data comparators.
STROBE	I	TTL input. Enables servo gate according to Figure 3.
$\overline{RG}$	I	TTL compatible input. When low, the device is in normal Read Mode.
$\overline{WG}$	I	TTL compatible input. When low, the device is in Write Mode. When both $\overline{RG}$ and $\overline{WG}$ are low, the device is in Servo Mode.
SG	I	TTL compatible input. When high the corresponding servo gate channel is enabled.
$\overline{HOLD}$	I	TTL compatible input. When low the AGC action is suspended.

OUTPUT PINS

NAME	TYPE	DESCRIPTION
VOA+, VOA-	O	AGC amplifier output pins.
ON+, ON-	O	Equalizer/filter normal output pins.
OD+, OD-	O	Equalizer/filter differentiated output pins.
DO	O	ECL compatible data comparator latch output pin.
RD, $\overline{RD}$	O	ECL compatible read data output pins.
$\overline{RDO}$	O	TTL compatible read data output.
SDIF+, SDIF-	–	Pins for external differentiating network for servo data.
PKA, PKB	O	Open npn emitter outputs that provide a fullwave rectified signal from the
PKC, PKD		servo differentiator. These outputs are referenced to AGND. These outputs are high impedance when not enabled by STROBE and SG.
LEVEL	O	Open NPN emitter output that provides an amplified fullwave rectified signal of DP-DN (32P3016 only.) The signal is referenced to VRC.

ANALOG PINS

NAME	TYPE	DESCRIPTION
RRX	–	Pin to set, via external R, output pulse widths.
VRC	–	Reference voltage pin for SERVO and LEVEL. VRC is referenced to VCA.
VRG	–	Reference voltage pin for the programmable filter. VRG is referenced to ground.
VBP	–	The equalizer high frequency boost is set by an external voltage applied to this pin. VBP must be proportional to VRG. Programmable boost is implemented by using a DAC that uses VRG as its reference. A fixed amount of boost can be set by an external resistor divide network connected from VBP to VRG and GND.
RX	–	Pin to set filter reference current. External resistor Rx from this pin to ground sets the filter reference current IFO.
IFO	–	Reference current output pin. The reference current is normally supplied as the reference current to a current DAC which generates the programmable input current for the IFI pin.
IFI	–	Programmable filter input current pin. The filter cutoff frequency is proportional to the current into this pin. The current must be proportional to the reference current out of IFO. A fixed filter cutoff frequency is generated by connecting IFO to IFI and selecting Rx to set the desired frequency.
LZ/FD	–	Pin for external resistor to set timing for both Low-Z input and fast decay modes.
BYP	–	The AGC integrating capacitor C_A is connected between BYP and VCA.
VCA, VCD, VCS	–	Analog, Digital, and Servo +5V
AGND, DGND	–	Analog and Digital grounds.

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, 4.5V<VCC<5.5V, 0°C<Ta<70°C

ABSOLUTE MAXIMUM RATINGS (Operation above maximum ratings may damage the device.)

PARAMETER	RATING
Storage Temperature	-65 to +150°C
Junction Operating Temperature,Tj	+130°C
Supply Voltage, VCA, VCD	-0.7 to 7V
Voltage Applied to Inputs	-0.7 to VCA, VCD V and VCS

RECOMMENDED OPERATING CONDITIONS

Supply Voltage, VCS = VCA = VCD = VCC	4.5V < VCC < 5.5V
Ambient Temperature, Ta	0°C<Ta<70°C

POWER SUPPLY

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
PD	Power Dissipation	Outputs unloaded 4.5V < VCA, VCD < 5.5V		490	640	mW

LOGIC SIGNALS

VIL	TTL Input Low Voltage		-0.3		0.8	V
VIH	TTL Input High Voltage		2.0		VCC +0.3	V
IIL	TTL Input Low Current	VIL = 0.4V	-0.4			mA
IIH	TTL Input High Current	VIH = 2.7V			0.1	mA
VOL	ECL Output High Voltage	VCC = 5V	VCC -1.02			V
VOE	ECL Differential Output Swing	VCC = 5V	0.3			V
TRF	EC Output Rise and Fall Time	CL ≤ 10 pF			3.5	ns
TS	Control Input Switching Times				0.1	µs
VOLT	TTL Output Low Voltage	IOL = 4mA	0.5			V
VOHT	TTL Output High Voltage	IOH = -400 mA			2.7	V

AGC AMPLIFIER

The input signals are AC coupled to VIA+ and VIA-. VOA+ and VOA- are AC coupled to IN+ and IN-. ON+ and ON- are AC coupled to DP and DN. Ca 1000 pF. Fin = 4 MHz. Unless otherwise specified, the output is measured differentially at VOA+ and VOA-.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
VIB	Input Range	Filter boost at fc = 0 dB	24		240	mVppd
		Filter boost at fc = 11 dB	20		100	mVppd
VD	DP-DN Voltage	VIA± = 0.1 Vppd	0.90		1.10	Vppd
VDV	DP-DN Voltage Variation	24 mV < VIA± < 240 mV			8.0	%
AV	Gain Range		1.9		22	V/V
AVPV	Gain Sensitivity w.r.t. BYP Voltage			28		dB/V
DR	VOA+ VOA- Dynamic Range	THD = 1% max	0.75			Vppd
RINDA	Differential Input Impedance	$\overline{WG}$ = 1	4.7		8.4	kΩ
		$\overline{WG}$ = 0		1		
RINSA	Single Ended Input Impedance	$\overline{WG}$ = 1		3		kΩ
		$\overline{WG}$ = 0		0.5		kΩ
VOS	Differential Output Offset Variation	from min. gain to max. gain	-200		+200	mV
VIN	Input Referred Noise Voltage	gain = max, Rs = 0Ω filter not connected to VOA+ and VOA-, BW = 15 MHz			15	nV/√Hz
BW	Bandwidth	No AGC action, Gain = 22	55			MHz
CMRR	Common Mode Rejection Ratio	gain = 22, Vin = 0 VDC + 100 mVpp @ 5 MHz	40			dB
PSRR	Power Supply Rejection Ratio	gain = 22, 100 mVpp on VCA, VCD @ 5 MHz	45			dB
TGD	Gain Decay Time	VIA± = 240 mV to 120 mV VOA± < 0.9 Final Value IFI = 600 µA		TBD		µs
TGA	Gain Attack Time	VIA± = 120 mV to 240 mV VOA± < 1.1 Final Value IFI = 600 µA		TBD		µs

ELECTRICAL SPECIFICATIONS (continued)

Unless otherwise specified, 4.5V<VCC<5.5V, 0°C<Ta<70°C

AGC CONTROL

The input signals are AC coupled to DP and DN. 110 µA<IFI<600 µA.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
VDI	DP-DN Signal Input Range				1.5	Vpp
ID	Discharge Current	WG = 1, DP - DN = 0V		0.008 x IFI		A
IDF	Fast Discharge Current			20 x Id		A
ICH	Charge Pump Attack Current	WG = 1, DP - DN = 0.55V		40 x Id		A
ICHF	Charge Pump Fast Attack Current, Ichf	WG = 1, DP - DN = 0.675V		7 x Ich		A
IK	BYP Pin Leakage Current	WG or HOLD = 0	-0.1		+0.1	µA
VRC	VRC Reference Voltage			VCA -VRG		V
IVRC	VRC Output Drive		-0.75		+0.75	mA
VRG	VRG Reference Voltage	Isource 0 to 1 mA	2.2		2.45	V
TLZ	Low-Z and Fast Decay Timing Accuracy	T = RT/28	-30		+30	%

EQUALIZER/FILTER

The input signals are AC coupled to IN+ and IN-.

fc	Filter Cutoff Frequency	RX = 5kΩ *fc* = 27 x IFI/(4 x IFO) MHz 4 ≥ IFO/IFI ≥ 4/3	9		27	MHz
IFO	IFO Reference Current	IFO = 0.75/RX; Tj = 27°C 5kΩ > RX > 1.25 kΩ	0.15		0.6	mA
IFI	IFI Program Current Range	Tj = 27°C, 27 MHz > *fc* > 9 MHz	0.2		0.6	mA
FCA	FCA Filter FC Accuracy	*fc* = 27 MHz	-13		13	%
RX	RX Range		1.25		5	kΩ
AO	Normal Low Pass Gain AO = (ON ±) / (IN±)	Fin = 0.67*fc*	1.4		2.2	V/V
AD	Differentiated Low Pass Gain AD = (OD ±) / (IN±)	Fin = 0.67*fc*	0.8AO		1.2AO	V/V
FBA	Frequency Boost Accuracy	VBP = VRG	-1.5		+1.5	dB
		VBP/VRG = 0.5	-1.0		+1.0	dB
TGD1	Group Delay Variation	*fc* = 27 MHz, VBP = 0 to VRG *fc* > Fin > 0.3 *fc*	-0.5		+0.5	ns
TGD2		*fc* = 9 to 27 MHz, VBP = 0 to VRG *fc* > Fin > 0.3 *fc*	-2.5		+2.5	%

EQUALIZER/FILTER (continued)
The input signals are AC coupled to IN+ and IN-.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
VOSVF	Output Offset Voltage Variation	200 µA,IFI<600 µA	-200		200	mV
DRF	VOF Filter Output Dynamic Range	THD = 1.5% max Fin = 0.67 *fc*	1.2			Vpp
RINF	Filter Input Resistance		3.0			kΩ
CINF	Filter Input Capacitance				7	pF
ROF	Filter Output Resistance	IO+ = 1.0 mA			60	Ω
IOF	Filter Output Current		-1.0		1.0	mA
VNN	Eout Output Noise Voltage; ON+, ON-	BW = 100 MHz, RS = 50Ω VBP = 0, *fc* = 27 MHz		2.7		mVRms
		BW = 100 MHz, RS = 50Ω VBP = VRG, *fc* = 27 MHz		5.7		mVRms
VND	Eout Output Noise Voltage; OD+, OD-	BW = 100 MHz, RS = 50Ω VBP = 0, *fc* = 27 MHz		5.5		mVRms
		BW = 100 MHz, RS = 50Ω VBP = VRG, *fc* = 27 MHz		13.0		mVRms

DATA COMPARATOR
The input signals are AC coupled to DP and DN.

VID	DP-DN Signal Range				1.5	Vpp
RIND	Differential Input Resistance		8		14	kΩ
CIND	Differential Input Capacitance				5	pF
VOSD*	Comparator Offset Voltage				4	mV
LG**	Level Output Gain	DP - DN = 0.25 to 0.5 VDC LG = (VLEVEL - VRC)/2 • (DP -DN)	0.712		0.788	V/V
LBW**	Level Output Bandwidth	±1 dB referenced to 1 MHz	20			MHz
VLOS**	Level Offset Voltage	Output - VRC, IL = 50 µA	-30		+30	mV
HYS	Threshold Voltage Gain	0.3 < VTH-VRC < 0.9	0.42		0.49	V/V
VSH*	Threshold Voltage Hysteresis			.20 x GHYS x (VTH -VRC)		V/V
TPDD	Propagation Delay	To DO, DO		6		ns
IVTH	VTH Input Bias Current				2	µA

* Not externally measurable ** 32P3016 only

ELECTRICAL SPECIFICATIONS (continued)

Unless otherwise specified, 4.5V<VCC<5.5V, 0°C<Ta<70°C

CLOCKING

The input signals are AC coupled to CP and CN.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
VIC	CP-CN Signal Range				1.5	Vppd
VOSC	Comparator Offset Voltage				4	mV
RINC	Differential Input Resistance		8		14	kΩ
CINC	Differential Input Capacitance				5	pF
TDS	D Flip-Flop Set Up Time	DP-DN threshold to CP-CN zero cross, CP-CN = 1Vppd at 18 MHz			1	ns
PP	Pulse Pairing	CP-CN = 20 mVppd square wave			0.5	ns
TPDC	Propagation Delay from CP-CN zero crossing to RD			9		ns
PWRD	RD Output Pulse Width	RRX = 7.87 kΩ CL = 10 pF	8		13	ns
PWRT	RDO, TTL Output Pulse Width	RRX = 7.87 kΩ CL = 10 pF	15		30	ns

SERVO DIFFERENTIATOR/FULL-WAVE RECTIFIER

An external series network is connected between SDIF and SDIF to determine the servo differentiator transfer function. The input signals are AC coupled to DP and DN. Fin = 6.7 MHz at 1.0 Vppd.

ISDIF	SDIF+ to SDIF- pin current	Differentiator ipedance must be set so as not to dip the signal for this level	1.4	2.0	2.6	mA
RDIF	Internal differentiator pull-up resistors	Cannot be directly tested	0.4	0.6	0.8	kΩ
FWR	Input voltage range to maintain FWR voltage gain	Cannot be directly tested	0.1		2.0	Vppd
RERR	Rectification Error				5	%
AFWR	FWR Voltage Gain from FWR Input to PKA-D Outputs		TBD	0.97	TBD	Vpp/ Vppd
ISL	Servo Output Leakage Current	Channel disabled			10	µA
VCOS	PKA-D Channel to Channel Offset	1Vppd input to servo FWR	TBD		TBD	mV
VAOS	PKA-D Absolute Offset	1Vppd input to servo FWR	TBD		TBD	mV

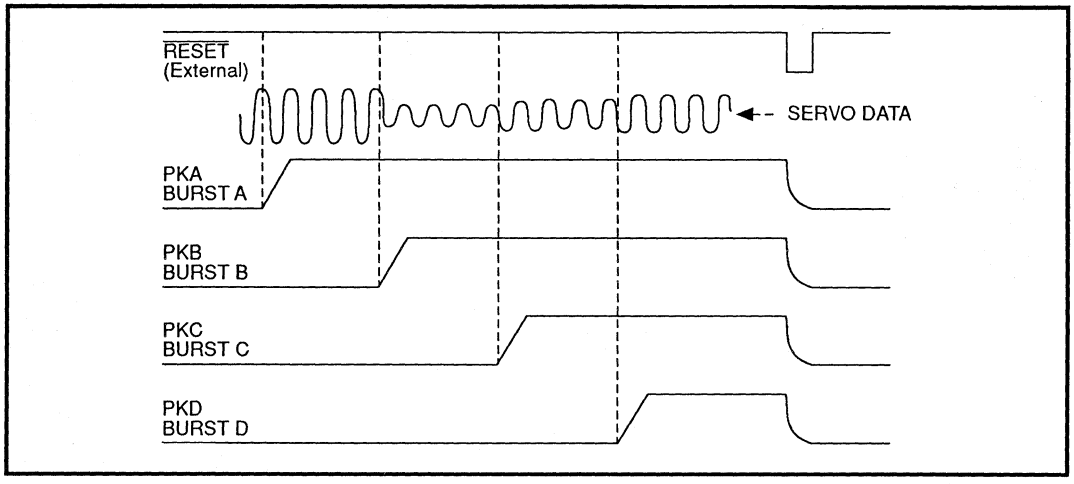


FIGURE 2: Servo Gate Timing

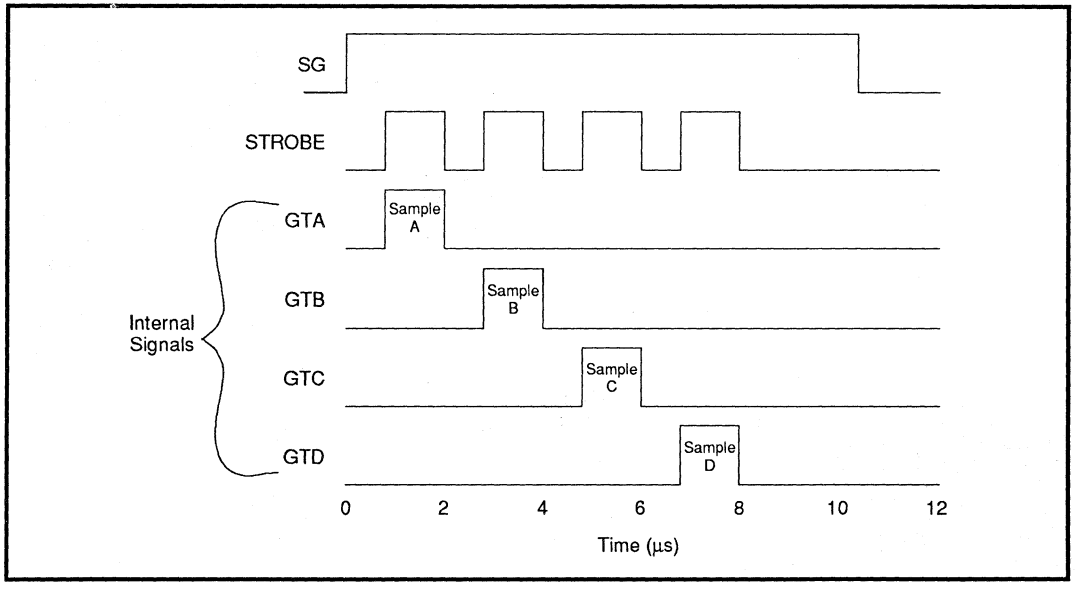


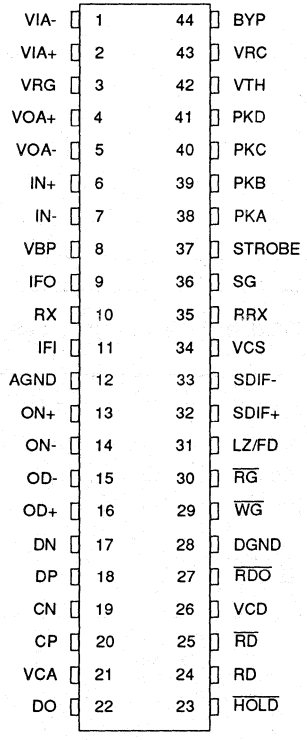
FIGURE 3: Servo Capture Timing Diagram

SSI 32P3015/3016
Pulse Detector with Programmable Filter

PACKAGE PIN DESIGNATIONS
(Top View)

THERMAL CHARACTERISTICS: θja

44-Lead SOM	**70°C/W**
48-Lead TQFP	**81°C/W**



44-Lead SOM
SSI 32P3015 only

PACKAGE PIN DESIGNATIONS
(Top View)

THERMAL CHARACTERISTICS: θja

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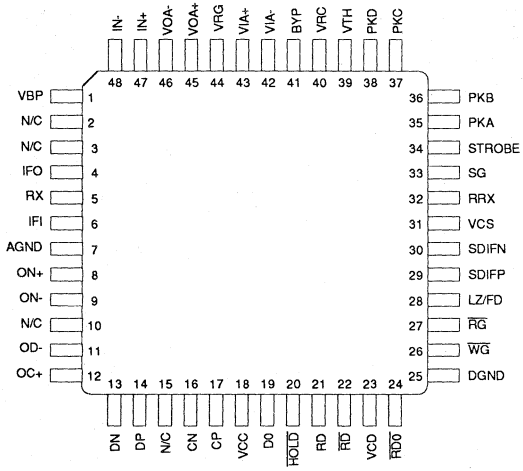
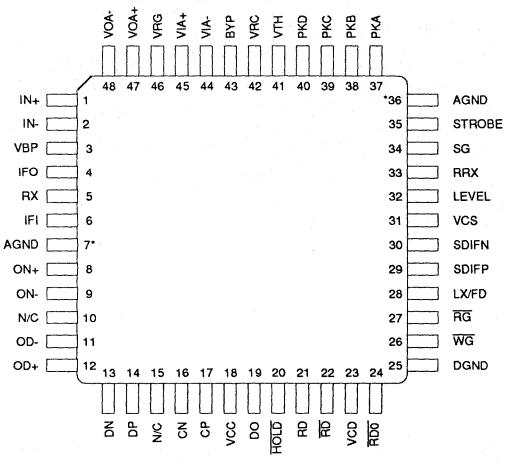
48-Lead TQFP	81°C/W



SSI 32P3015
48-Lead TQFP



SSI 32P3016
48-Lead TQFP

*Both Pin 7 and Pin 36 of the 32P3016 must be connected to PCB analog ground. Pin 36 is not connected to the chip's circuits. It is used as an electrostatic shield.

4

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914

Notes:

silicon systems®
A TDK Group Company

SSI 32P3040
Pulse Detector with Programmable Filter

January 1994

DESCRIPTION

The SSI 32P3040 is a bipolar integrated circuit that provides all data processing necessary for detection and qualification of encoded read signals. The circuit will handle a data rate of 32 Mbit/s.

In read mode the SSI 32P3040 provides amplification and qualification of head preamplifier outputs. Pulse qualification is accomplished using level qualification of differentiated input zero crossings. An AGC amplifier is used to compensate for variations in head preamp output levels, presenting a constant input level to the pulse qualification circuitry. The AGC loop can be disabled so that a constant gain can be used for embedded servo decoding or other processing needs.

Write to read transient recovery is enhanced by providing AGC input impedance switching and a selectable Fast Recovery mode that provides a higher decay current.

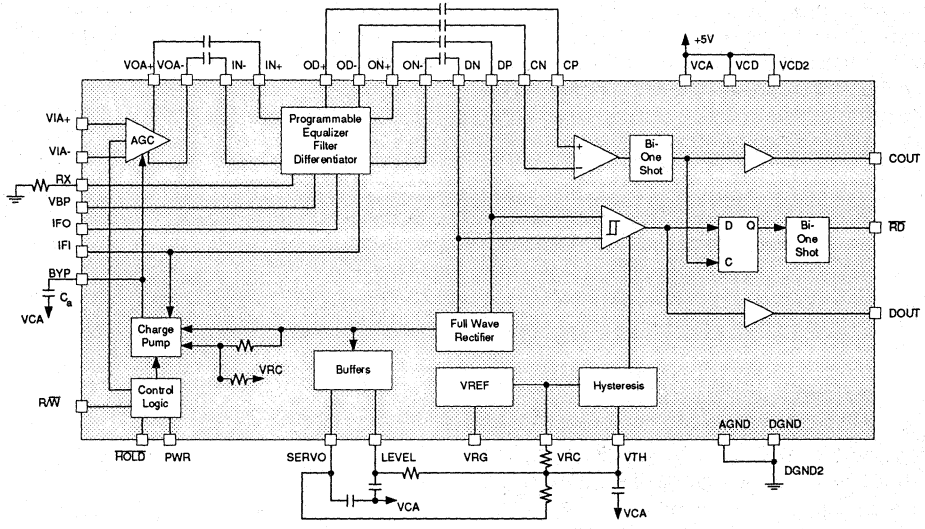
Additionally, the SSI 32P3040 contains an integrated programmable electronic filter with cutoff frequencies between 2.5 and 13 MHz. High frequency boost (for pulse slimming) of up to +9 dB is also provided. The SSI 32P3040 requires only a +5V power supply and is available in 36-lead SOM and 32-lead TQFP packages.

FEATURES

- **Compatible with 32 Mbit/s data rate operation**
- **Fast attack/decay modes for rapid AGC recovery**
- **Dual rate charge pump for fast transient recovery charge pump currents track programmable channel bandwidth**
- **Low drift AGC hold, fast AGC recovery, and low AGC input impedance control signals. Circuitry supports programmable gain non-AGC operation**
- **Temperature compensated, exponential control AGC**
- **Precision wide bandwidth fullwave rectifier**
- **Supports programmable pulse slimming equalization and programmable channel filter and differentiator with no external filter components**
- **±2% Filter group delay variation from 0.3FC to FC**
- **Servo burst output available**
- **Differential hysteresis qualifier comparator to ease clock channel timing**
- **Accurate feed forward or fixed threshold set**

4

BLOCK DIAGRAM



SSI 32P3040
Pulse Detector with Programmable Filter

FEATURES (continued)

- 1 ns max pulse pairing with sine wave input
- 5 mW low power idle mode
- TTL read data output
- +5V only operation
- 36-pin SOM and 32-pin TQFP packages

FUNCTIONAL DESCRIPTION

The SSI 32P3040 Pulse Detector is designed to support a 32 Mbit/s data rate. The signal processing circuits include a wide band variable gain amplifier, a programmable electronic filter, differentiator and pulse slimming equalizer, a precision wide bandwidth fullwave rectifier, and a dual rate charge pump. A fully differential filter, differentiator, equalizer, and fullwave rectifier are provided to minimize external noise pick-up. To optimize recovery for constant density recording, the AGC charge pump current tracks the programmable filter current IFI. The differentiator zero tracks the programmable filter cutoff frequency. Thus in constant density recording applications, an approximately constant differentiated signal amplitude is maintained. The desired filter response and equalization are easily programmed with the SSI 32D4661, Time Base Generator DACs. A dual rate attack charge pump and a Fast Decay mode are included for fast transient recovery. At maximum IFI current, the normal AGC attack current is 0.28 mA. When the signal exceeds 125% of the nominal signal level, the attack current is increased by a factor of 5. The nominal decay current at max IFI is 5.6 µA. The decay current is increased 20 times when in the fast decay mode. In this mode, transients that produce low gain will recover more rapidly with the fast decay current, while transients that produce high gain will put the circuit in the fast attack recovery mode. The decay modes are automatically controlled within the device. When R/$\overline{W}$ is low, the AGC is in its hold mode and its input impedance is switched low. When R/$\overline{W}$ is switched high, the AGC remains in the hold and low input impedance state for 0.7 µs and then switches to the fast decay mode for 0.7 µs. The AGC amplifier input impedance is reduced to allow quick recovery of the AGC amplifier input AC coupling capacitors. When the $\overline{HOLD}$ input is low, the AGC action is stopped and the AGC amplifier gain is set by the voltage at the BYP pin. In most applications, the BYP pin voltage is stored on an external capacitor when $\overline{HOLD}$ goes low. In applications where AGC action is not desired, the BYP voltage can be set by a resistor divider network connected from VCC to VRC. If a programmable gain is desired, the resistor network could be driven by a current DAC. The precision fullwave rectifier produces an accurate Level and Servo output signal. These outputs are referenced to the reference voltage VRC. SERVO and LEVEL are buffered open emitter outputs with 100 ohm series current limiting resistors. These outputs could be further filtered with external capacitors.

LEVEL has an internal 50 µA discharge current source. An optional Servo output capacitor discharge circuit can be included. An external resistor connected to the RX pin sets the electronic filter reference current which is the source from pin IFO. If a programmable frequency response is desired, a portion of the current from IFO, which is proportional to absolute temperature, must be injected into pin IFI. This could be accomplished by a current DAC. Some frequency response programming may be accomplished by connecting IFO to IFI and switching different resistors to pin RX. Frequency boost is accomplished by varying the voltage at VBP. VBP has a nominal 100 mV built-in offset so that the circuit has 0 dB boost for VBP below 100 mV. The voltage at VBP should be proportional to the reference voltage at pin VRG.

A differential comparator with floating hysteresis threshold allows differential signal qualification for noise rejection. An accurate feed forward qualification level is generated by comparing the difference between LEVEL and VRC. VRC is referenced to VCA. Thus with the VTH resistor network connected from VCA to VRC, an accurate fixed threshold can be established. The threshold is clamped to a minimum value of 50 mV. Thus a qualified signal must exceed this minimum level even when the VTH-VRC voltage is zero. A qualified signal zero crossing triggers the output one shot. The one shot period is set internally. Low level differential outputs are provided for high speed operation and to minimize noise generation.

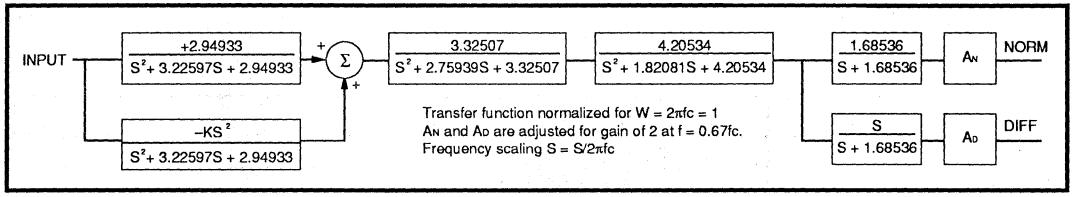


FIGURE 1: Bessel Filter Transfer Function

$$K = 2.94933\ (10^{\frac{BOOST\ (dB)}{20}} - 1)$$

4

TABLE 1: Typical Change in *f* - 3 dB Point with Boost

Boost (dB)	Gain@*fc* (dB)	Gain@peak (dB)	*f*Peak/*fc*	*f*-3dB/*fc*	K
0	-3	0.00	no peak	1.00	0
1	-2	0.00	no peak	1.20	0.36
2	-1	0.00	no peak	1.47	0.76
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e.g., *fc* = 13 MHz when boost = 0 dB
if boost is programmed to 5 dB, then *f* - 3 dB = 27.69 MHz
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DP, DN	I	Data inputs to data comparators and fullwave rectifier.
CP, CN	I	Differentiated data inputs to the clock comparator.
VTH	I	Threshold level setting input for the data comparators.
R/$\overline{W}$	I	TTL compatible input when high puts the charge pump in the normal mode.
PWR	I	TTL compatible input when high puts the circuit in its normal operating mode.
$\overline{HOLD}$	I	TTL compatible input when low disables the AGC action by turning off the charge pump.
OUTPUT PINS		
VOA+, VOA-	O	AGC amplifier output pins.
ON+, ON-	O	Equalizer/filter normal output pins.
OD+, OD-	O	Equalizer/filter differentiated output pins.
DOUT	O	Test point for monitoring the data F/F D-input. Usage requires an external 2.4 kΩ resistor from DOUT to GND. (Not available in 32-pin TQFP package.)
COUT	O	Test points for monitoring the data F/F clock inputs. Usage requires an external 2.4 kΩ resistor from DOUT to GND. (Not available in 32-pin TQFP package.)
$\overline{RD}$	O	TTL compatible read data output pins.
LEVEL	O	Open NPN emitter output that provides a fullwave rectified signal for the VTH input. The signal is referenced to VRC.
SERVO	O	Open NPN emitter output that provides a fullwave rectified servo signal. The signal is referenced to VRC.
ANALOG PINS		
VRC	-	Reference voltage pin for SERVO and LEVEL. VRC is referenced to VCA.
VRG	-	Reference voltage pin for the programmable filter. VRG is referenced to ground.
VBP	-	The equalizer high frequency boost is set by an external voltage applied to this pin. VBP must be proportional to VRG. Programmable boost is implemented by using a DAC that uses VRG as its reference. A fixed amount of boost can be set by an external resistor divide network connected from VBP to VRG and GND.
RX	-	Pin to set filter reference current. External resistor Rx from this pin to ground sets the filter reference current IFO.
IFO		Reference current output pin. The reference current is normally supplied as the reference current to a current DAC which generates the programmable input current for the IFI pin.

PIN DESCRIPTION (continued)

ANALOG PINS (continued)

NAME	TYPE	DESCRIPTION
IFI		Programmable filter input current pin. The filter cutoff frequency is proportional to the current into this pin. The current must be proportional to the reference current out of IFO. A fixed filter cutoff frequency is generated by connecting IFO to IFI and selecting Rx to set the desired frequency.
BYP		The AGC integrating capacitor C_A is connected between BYP and VCA.
VCA, VCD,VCD2		Analog and Digital +5 volts.
AGND, DGND, DGND2		Analog and Digital grounds.

4

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, 4.5V<VCC<5.5V, 0°C<Ta<70°C

ABSOLUTE MAXIMUM RATINGS (Operation above maximum ratings may damage the device.)

PARAMETER	RATING
Storage Temperature	-65 to +150°C
Junction Operating Temperature,Tj	+130°C
Supply Voltage, VCA, VCD	-0.7 to 7V
Voltage Applied to Inputs	-0.5 to VCA, VCD +0.5V

RECOMMENDED OPERATING CONDITIONS

PARAMETER		RATING
Supply Voltage	VCA = VCD = VCC	4.5V<VCC<5.5V
Ambient Temperature, Ta		0°C<Ta<70°C

POWER SUPPLY

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
ISS	Supply Voltage Current	Active mode		75	90	mA
		Low-Power mode		1	1.5	mA
PD	Power Dissipation	Active mode		400	500	mW
		Low-Power mode		5	8	mW

ELECTRICAL SPECIFICATIONS (continued)

Unless otherwise specified, 4.5V<VCC<5.5V, 0°C<Ta<70°C

LOGIC SIGNALS

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
VIL	TTL Input Low Voltage		-0.3		0.8	V
VIH	TTL Input High Voltage		2.0		VCC +0.3	V
IIL	TTL Input Low Current	VIL = 0.4V	-0.4			mA
IIH	TTL Input High Current	VIH = 2.7V			0.1	mA
VOH	TTL Output High Voltage	IOH = -400µA	2.4			V
VOL	TTL Output Low Voltage	IOL = 3 mA			0.5	V
TRDRF	Output Rise and Fall Time	CL = 15 pF			7	ns
TH	Hold Input Switching Times				0.3	µs
TWR	Write to Read Recovery Time	R/$\overline{W}$ pin low to high	0.5		1.4	µs

AGC AMPLIFIER

The input signals are AC coupled to VIA+ and VIA-, VOA+ and VOA- are AC coupled to IN+ and IN-, ON+ and ON- are AC coupled to DP and DN, Ca 1000 pF, Fin = 4 MHz. Unless otherwise specified, the output is measured differentially at VOA+ and VOA-, Fin = 4 MHz and filter boost at Fc = 0dB.

VIR	Input Range	Filter boost at FC = 0 dB	24		240	mVppd
		Filter boost at FC = 9 dB	20		120	mVppd
VDPN	DP-DN voltage	VIA± = 0.1 Vpp	0.85		1.05	Vppd
VDPNV	DP-DN Voltage Variation	24 mV < VIA± < 240 mV			8.0	%
AV	Gain Range		1.9		22	V/V
AVPV	Gain Sensitivity			38		dB/V
VOADR	VOA+, VOA- Dynamic Range	THD = 1% max	0.75			Vpp
ZIN	Input Impedance	R/$\overline{W}$= high	3.0		7.5	kΩ
ZCMIN	Common Mode	R/$\overline{W}$ = high		1.5		kΩ
	Input Impedance	R/$\overline{W}$ = low		200		Ω
VOS	Output Offset Voltage Variation	Over gain range	-200		+200	mV
VINO	Input Noise Voltage	gain = max, filter not connected to VOA±, Rs = 0Ω, Bw = 15 MHz		5	10	nV/√Hz
BW	Bandwidth	No AGC action	55	75		MHz
CMRR	Common-mode Rejection Ratio	gain = max, Vin = 0 VDC + 100 mVpp @ 5 MHz	40	65		dB
PSRR	Power Supply Rejection Ratio	gain = max, 100 mVpp @ 5 MHz on VCA, VCD, VCD2	45	67		dB
TGD	Gain Decay Time	VIA± = 240 mV to 120 mV VOA± >0.9 Final Value BYP ≤, 1000 pF, IFI = max		34	44	µs

ANALOG PINS (continued)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TGA	Gain Attack Time	VIA± = 120 mV to 240 mV VOA± <1.1 Final Value BYP ≤, 1000 pF, IFI = max		1.5	2	µs

AGC CONTROL

The input signals are AC coupled to DP and DN. Ca = 1000 pF, LEVEL load = 50 µA, SERVO load = 100 µA.

VDI	DP-DN Signal Input Range				1.4	Vpp
ALO	Level (Servo) Output Gain	DP-DN = 0.25 to 0.5 VDC LG = (V_{LEVEL} - V_{RC})/2(DP-DN)	0.73		0.81	V/V
BWL	Level (Servo) Output Bandwidth	1 dB	15			MHz
VLO	Level Offset Voltage	Output-VRC, IL = 50 µA			30	mV
VSO	Servo Offset Voltage	Output - VRC, IL = 100 µA			30	mV
ZLS	Level (Servo) Output Impedance	IL = 100 µA		200	300	Ω
ID	Discharge Current			0.008 x IFI		mA
IDF	Fast Discharge Current	0.7 to 1.4 µs after R/$\overline{W}$ goes high		20 x ID		mA
ICH	Charge Pump Attack Current			50 x ID		mA
ICHF	Charge Pump Fast Attack Current	DP-DN = 1.35 Vpp		5 x ICH		mA
IBYP	Pin Leakage Current	$\overline{HOLD}$ = low, V_{BYP} = VCC -1.5V	-0.1		0.1	µA
VRC	Reference Voltage		VCC-2.52		VCC-2.15	V
IVRC	Output Drive		-0.75		0.75	mA
VRG	Reference		2.15		2.5	V
IVRG	Source Current		1			mA
VAGC	Pin Voltage			VRC+1.0		V

EQUALIZER/FILTER The input signals are AC coupled to IN+ and IN-.

fc	Filter Cutoff Frequency	*fc* = 19.14(IFI/IFO)(1/Rx)	2.5		13.5	MHz
V_{RX}	PTAT Reference Current Set Output Voltage	TA = 25°C I_{RX} = 0 - 0.7 mA Rx > 1.21 kΩ		850		mV
IFOR	PTAT Reference Current Output Current Range	TA = 25°C 1.21 kΩ < Rx < 7.73 kΩ IFO = V_{RX}/Rx	0.11		0.7	mA

EQUALIZER/FILTER (continued)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
IFIR	PTAT Programming Current Range	TA = 25°C, V_{RX} = 850 mV	0.11		0.7	mA
VBPR	Input Voltage Range		0		VRG	V
IBP	Input Bias Current				3	µA
FCA	Filter FC Accuracy	FC = 5 to 13.5 MHz	-12		+12	%
AO	[(ON±)]/[(IN±)] Normal Gain	F = 0.67 FC	1.4		2.2	V/V
AD	[(OD±)]/[(IN±)] Diff Gain	F = 0.67 FC	1.0AO		1.3AO	V/V
FB	Frequency Boost at FC	FB = 20 log [1.884(VBP-0.1) /VRG+1] VBP -0.1>0	0		9.5	dB
FBA	Frequency Boost Accuracy	FB = max	-1		+1	dB
TGD	Group Delay Variation	0.3 FC to FC = 13.5 MHz FB = 0 to max	-2		+2	%
VOO	Output Offset Voltage	Variation over entire frequency range	-200		+200	mV
VOF	Filter Output Dynamic Range	THD = 1.5% max	1.0			Vpp
		THD = 3.0% max F = 0.67 FC	1.25			Vpp
RINF	Filter Input Resistance		4.0	6.0	8.0	kΩ
CINF	Filter Input Capacitance				7	pF
RO	Filter Output Resistance	IO = 0.5 mA		70	85	Ω
IFOD	Filter Output Drive Current		-1		+1	mA
VNN	Eout Output Noise Voltage ON±	BW = 100 MHz, Rs = 50Ω IFI = 0.7 mA, VBP = 0		2.2	3.0	mVRMS
		BW = 100 MHz, Rs = 50Ω IFI = 0.7 mA, VBP = VRG		3.0	4.5	mVRMS
VND	Eout Output Noise Voltage OD±	BW = 100 MHz, Rs = 50Ω IFI = 0.7 mA, VBP = 0		5.4	6.4	mVRMS
		BW = 100 MHz, Rs = 50Ω IFI = 0.7 mA, VBP = VRG		9.6	10.6	mVRMS

DATA COMPARATOR
The input signals are AC coupled to DP and DN.

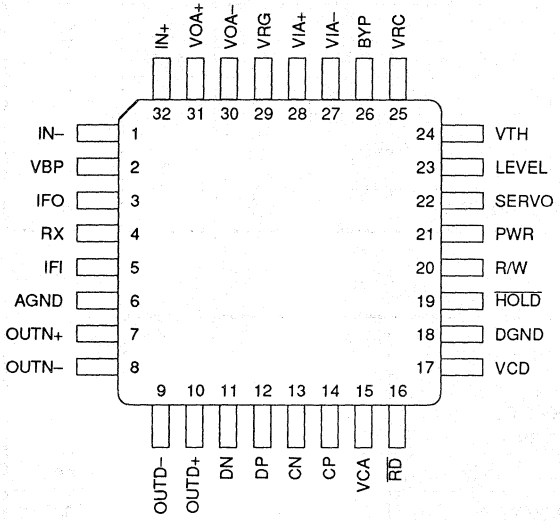
RINDC Differential Input Resistnace		7		14	kΩ
CINDC Differential Input Capacitance				5	pF
ATH Threshold Voltage Gain, Kth	0.3 < VTH-VRC < 0.75	0.42		0.49	V/V
VIAMIN Minimum Threshold Voltage	VTH-VRC ≤ 0.11V		.05		V
TPDDC Propagation Delay	To DOUT		10		ns
ITH VTH Input Bias Current				2	μA
DOUTSS DOUT Signal Swing	2.4 kΩ from DOUT to GND		0.5		V

CLOCKING
The input signals are AC coupled to CP and CN.

RINCL Differential Input Resistance		7		14	kΩ
CINCL Differential Input Capacitance				5	pF
TDS D F/F Set Up Time	DP-DN threshold to CP-CN zero cross	0			ns
TPP Pulse Pairing	Vs = 1Vpp, F = 2.5 MHz			1	ns
TPDCL Propagation Delay to RD	Vs = 20 mVpp sq wave		14	20	ns
RDPW Output Pulse Width	Measured at 1.4V level	10		27	ns
COUTS Signal Swing	2.4 kΩ from COUT to GND		0.5		V

SSI 32P3040
Pulse Detector with Programmable Filter

PACKAGE PIN DESIGNATIONS
(Top View)

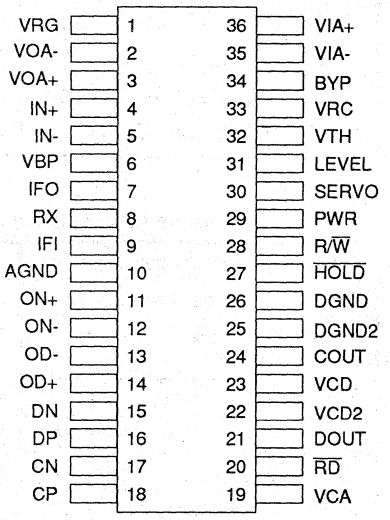


32-Lead TQFP

CAUTION: Use handling procedures necessary for a static sensitive component.

THERMAL CHARACTERISTICS: θja

32-Lead TQFP	124° C/W
36-Lead SOM	75° C/W



36-Lead SOM

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32P3040		
32-Lead Thin Quad Flatpack	32P3040-CGT	32P3040-CGT
36-Lead Small Outline	32P3040-CM	32P3040-CM

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914

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SSI 32P3041
Pulse Detector with Programmable Filter

December 1993

DESCRIPTION

The SSI 32P3041 is a bipolar integrated circuit that provides all data processing necessary for detection and qualification of encoded read signals. The circuit will handle a data rate of 32 Mbit/s.

In read mode the SSI 32P3041 provides amplification and qualification of head preamplifier outputs. Pulse qualification is accomplished using level qualification of differentiated input zero crossings. An AGC amplifier is used to compensate for variations in head preamp output levels, presenting a constant input level to the pulse qualification circuitry. The AGC loop can be disabled so that a constant gain can be used for embedded servo decoding or other processing needs.

Write to read transient recovery is enhanced by providing AGC input impedance switching and a selectable Fast Recovery mode that provides a higher decay current.

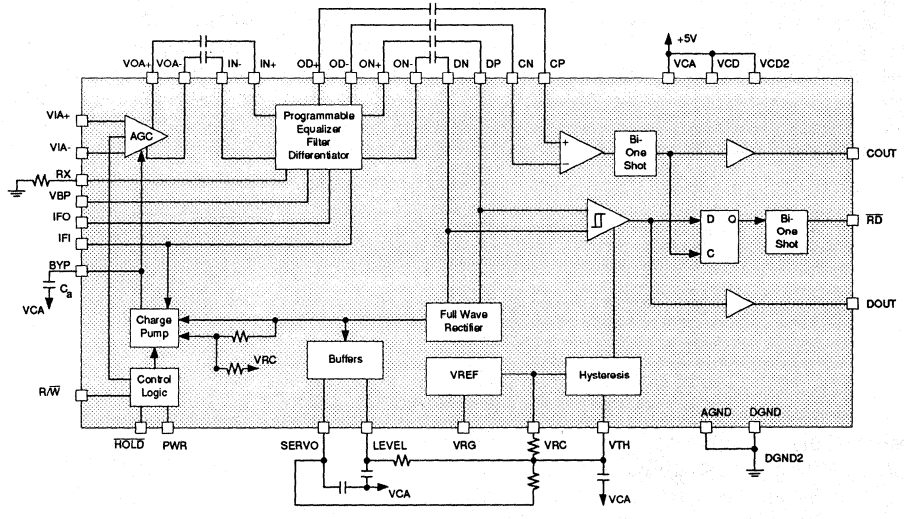
Additionally, the SSI 32P3041 contains an integrated programmable electronic filter with cutoff frequencies between 2.5 and 13 MHz. High frequency boost (for pulse slimming) of up to 9.5 dB is also provided. The SSI 32P3041 requires only a +5V power supply and is available in 36-lead SOM and 32-lead TQFP packages.

FEATURES

- **Compatible with 32 Mbit/s data rate operation**
- **Fast attack/decay modes for rapid AGC recovery**
- **Dual rate charge pump for fast transient recovery charge pump currents track programmable channel bandwidth**
- **Low drift AGC hold, fast AGC recovery, and low AGC input impedance control signals. Circuitry supports programmable gain non-AGC operation**
- **Temperature compensated, exponential control AGC**
- **Precision wide bandwidth fullwave rectifier**
- **Supports programmable pulse slimming equalization and programmable channel filter and differentiator with no external filter components**
- **±2% Filter group delay variation from 0.3 FC to FC**
- **Servo burst output available**
- **Differential hysteresis qualifier comparator to ease clock channel timing**
- **Accurate feed forward or fixed threshold set**

4

BLOCK DIAGRAM



SSI 32P3041
Pulse Detector with Programmable Filter

FEATURES (continued)

- 1 ns max pulse pairing with sine wave input
- 5 mW low power idle mode
- TTL read data output
- +5V only operation
- 36-pin SOM and 32-pin TQFP packages

FUNCTIONAL DESCRIPTION

The SSI 32P3041 Pulse Detector is designed to support a 32 Mbit/s data rate. The signal processing circuits include a wide band variable gain amplifier, a programmable electronic filter, differentiator and pulse slimming equalizer, a precision wide bandwidth fullwave rectifier, and a dual rate charge pump. A fully differential filter, differentiator, equalizer, and fullwave rectifier are provided to minimize external noise pick-up. To optimize recovery for constant density recording, the AGC charge pump current tracks the programmable filter current IFI. The differentiator zero tracks the programmable filter cutoff frequency. Thus in constant density recording applications, an approximately constant differentiated signal amplitude is maintained. The desired filter response and equalization are easily programmed with the SSI 32D4661, Time Base Generator DACs. A dual rate attack charge pump and a Fast Decay mode are included for fast transient recovery. At maximum IFI current, the normal AGC attack current is 0.28 mA. When the signal exceeds 125% of the nominal signal level, the attack current is increased by a factor of 5. The nominal decay current at max IFI is 5.6 µA. The decay current is increased 20 times when in the fast decay mode. In this mode, transients that produce low gain will recover more rapidly with the fast decay current, while transients that produce high gain will put the circuit in the fast attack recovery mode. The decay modes are automatically controlled within the device. When R/$\overline{W}$ is low, the AGC is in its hold mode and its input impedance is switched low. When R/$\overline{W}$ is switched high, the AGC remains in the hold and low input impedance state for 2.3 µs and then switches to the fast decay mode for 0.7 µs. The AGC amplifier input impedance is reduced to allow quick recovery of the AGC amplifier input AC coupling capacitors. When the $\overline{HOLD}$ input is low, the AGC action is stopped and the AGC amplifier gain is set by the voltage at the BYP pin. In most applications, the BYP pin voltage is stored on an external capacitor when $\overline{HOLD}$ goes low. In applications where AGC action is not desired, the BYP voltage can be set by a resistor divider network connected from VCC to VRC. If a programmable gain is desired, the resistor network could be driven by a current DAC. The precision fullwave rectifier produces an accurate Level and Servo output signal. These outputs are referenced to the reference voltage VRC. SERVO and LEVEL are buffered open emitter outputs with 100 ohm series current limiting resistors. These outputs could be further filtered with external capacitors.

LEVEL has an internal 50 µA discharge current source. An optional Servo output capacitor discharge circuit can be included. An external resistor connected to the RX pin sets the electronic filter reference current which is the source from pin IFO. If a programmable frequency response is desired, a portion of the current from IFO, which is proportional to absolute temperature, must be injected into pin IFI. This could be accomplished by a current DAC. Some frequency response programming may be accomplished by connecting IFO to IFI and switching different resistors to pin RX. Frequency boost is accomplished by varying the voltage at VBP. VBP has a nominal 100 mV built-in offset so that the circuit has 0 dB boost for VBP below 100 mV. The voltage at VBP should be proportional to the reference voltage at pin VRG.

A differential comparator with floating hysteresis threshold allows differential signal qualification for noise rejection. An accurate feed forward qualification level is generated by comparing the difference between LEVEL and VRC. VRC is referenced to VCA. Thus with the VTH resistor network connected from VCA to VRC, an accurate fixed threshold can be established. The threshold is clamped to a minimum value of 50 mV. Thus a qualified signal must exceed this minimum level even when the VTH-VRC voltage is zero. A qualified signal zero crossing triggers the output one shot. The one shot period is set internally. Low level differential outputs are provided for high speed operation and to minimize noise generation.

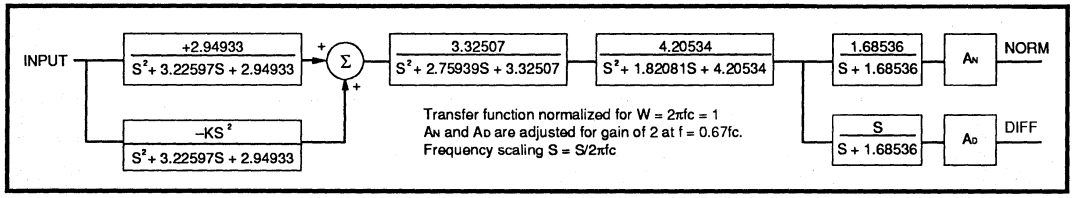


FIGURE 1: Bessel Filter Transfer Function

$$K = 2.94933\,(10^{\frac{BOOST\ (dB)}{20}} - 1)$$

4

TABLE 1: Typical Change in *f* - 3 dB Point with Boost

Boost (dB)	Gain@*fc* (dB)	Gain@peak (dB)	*f*Peak/*fc*	*f*-3dB/*fc*	K
0	-3	0.00	no peak	1.00	0
1	-2	0.00	no peak	1.20	0.36
2	-1	0.00	no peak	1.47	0.76
3	0	0.15	0.62	1.74	1.22
4	1	1.00	1.08	1.96	1.73
5	2	2.12	1.24	2.13	2.30
6	3	3.35	1.24	2.28	2.94
7	4	4.56	1.39	2.42	3.65
8	5	5.82	1.39	2.54	4.46
9	6	7.04	1.39	2.66	5.36
10	7	8.24	1.39	2.77	6.38
11	8	9.41	1.39	2.88	7.52
12	9	10.55	1.39	2.98	8.79
13	10	11.70	1.55	3.08	10.22

Notes: 1. *f*c is the original programmed cutoff frequency with no boost.
2. *f* - 3 dB is the new -3 dB value with boost implemented.
3. *f*peak is the frequency where the magnitude peaks with boost implemented.

e.g., *f*c = 13 MHz when boost = 0 dB
if boost is programmed to 5 dB, then *f* - 3 dB = 27.69 MHz
*f*peak = 16.12 MHz

PIN DESCRIPTION

INPUT PINS

NAME	TYPE	DESCRIPTION
VIA+, VIA-	I	AGC Amplifier input pins.
IN+, IN-	I	Equalizer/filter input pins.
DP, DN	I	Data inputs to data comparators and fullwave rectifier.
CP, CN	I	Differentiated data inputs to the clock comparator.
VTH	I	Threshold level setting input for the data comparators.
R/$\overline{W}$	I	TTL compatible input when high puts the charge pump in the normal mode.
PWR	I	TTL compatible input when high puts the circuit in its normal operating mode.
$\overline{HOLD}$	I	TTL compatible input when low disables the AGC action by turning off the charge pump.
OUTPUT PINS		
VOA+, VOA-	O	AGC amplifier output pins.
ON+, ON-	O	Equalizer/filter normal output pins.
OD+, OD-	O	Equalizer/filter differentiated output pins.
DOUT	O	Test point for monitoring the data F/F D-input. Usage requires an external 2.4 kΩ resistor from DOUT to GND. (Not available in 32-pin TQFP package.)
COUT	O	Test points for monitoring the data F/F clock inputs. Usage requires an external 2.4 kΩ resistor from COUT to GND. (Not available in 32-pin TQFP package.)
$\overline{RD}$	O	TTL compatible read data output pins.
LEVEL	O	Open NPN emitter output that provides a fullwave rectified signal for the VTH input. The signal is referenced to VRC.
SERVO	O	Open NPN emitter output that provides a fullwave rectified servo signal. The signal is referenced to VRC.
ANALOG PINS		
VRC	-	Reference voltage pin for SERVO and LEVEL. VRC is referenced to VCA.
VRG	-	Reference voltage pin for the programmable filter. VRG is referenced to ground.
VBP	-	The equalizer high frequency boost is set by an external voltage applied to this pin. VBP must be proportional to VRG. Programmable boost is implemented by using a DAC that uses VRG as its reference. A fixed amount of boost can be set by an external resistor divide network connected from VBP to VRG and GND.
RX	-	Pin to set filter reference current. External resistor Rx from this pin to ground sets the filter reference current IFO.
IFO		Reference current output pin. The reference current is normally supplied as the reference current to a current DAC which generates the programmable input current for the IFI pin.

PIN DESCRIPTION (continued)

ANALOG PINS (continued)

NAME	TYPE	DESCRIPTION
IFI		Programmable filter input current pin. The filter cutoff frequency is proportional to the current into this pin. The current must be proportional to the reference current out of IFO. A fixed filter cutoff frequency is generated by connecting IFO to IFI and selecting Rx to set the desired frequency.
BYP		The AGC integrating capacitor C_A is connected between BYP and VCA.
VCA, VCD,VCD2		Analog and Digital +5 volts.
AGND, DGND, DGND2		Analog and Digital grounds.

4

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, 4.5V<VCC<5.5V, 0°C<Ta<70°C

ABSOLUTE MAXIMUM RATINGS (Operation above maximum ratings may damage the device.)

PARAMETER	RATING
Storage Temperature	-65 to +150°C
Junction Operating Temperature,Tj	+130°C
Supply Voltage, VCA, VCD	-0.7 to 7V
Voltage Applied to Inputs	-0.5 to VCA, VCD +0.5V

RECOMMENDED OPERATING CONDITIONS

PARAMETER		RATING
Supply Voltage	VCA = VCD = VCC	4.5V<VCC<5.5V
Ambient Temperature, Ta		0°C<Ta<70°C

POWER SUPPLY

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
ISS Supply Voltage Current	Active mode		75	90	mA
	Low-Power mode		1	1.5	mA
PD Power Dissipation	Active mode		400	500	mW
	Low-Power mode		5	8	mW

ELECTRICAL SPECIFICATIONS (continued)

Unless otherwise specified, 4.5V<VCC<5.5V, 0°C<Ta<70°C

LOGIC SIGNALS

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
VIL	TTL Input Low Voltage		-0.3		0.8	V
VIH	TTL Input High Voltage		2.0		VCC +0.3	V
IIL	TTL Input Low Current	VIL = 0.4V	-0.4			mA
IIH	TTL Input High Current	VIH = 2.7V			0.1	mA
VOH	TTL Output High Voltage	IOH = -400µA	2.4			V
VOL	TTL Output Low Voltage	IOL = 3 mA			0.5	V
TRDRF	Output Rise and Fall Time	CL = 15 pF			7	ns
TH	Hold Input Switching Times				0.3	µs

AGC AMPLIFIER

The input signals are AC coupled to VIA+ and VIA-, VOA+ and VOA- are AC coupled to IN+ and IN-, ON+ and ON- are AC coupled to DP and DN, Ca 1000 pF, Fin = 4 MHz. Unless otherwise specified, the output is measured differentially at VOA+ and VOA-, Fin = 4 MHz and filter boost at Fc = 0dB.

VIR	Input Range	Filter boost at FC = 0 dB	24		240	mVppd
		Filter boost at FC = 9 dB	20		120	mVppd
VDPN	DP-DN voltage	VIA± = 0.1 Vpp	0.85		1.05	Vppd
VDPNV	DP-DN Voltage Variation	24 mV < VIA± < 240 mV			8.0	%
AV	Gain Range		1.9		22	V/V
AVPV	Gain Sensitivity			38		dB/V
VOADR	VOA+, VOA- Dynamic Range	THD = 1% max	0.75			Vpp
ZIN	Input Impedance	R/$\overline{W}$= high	3.0		7.5	kΩ
ZCMIN	Common Mode	R/$\overline{W}$ = high		1.5		kΩ
	Input Impedance	R/$\overline{W}$ = low		200		Ω
VOS	Output Offset Voltage Variation	Over gain range	-200		+200	mV
VINO	Input Noise Voltage	gain = max, filter not connected to VOA±, Rs = 0Ω, Bw = 15 MHz		5	10	nV/√Hz
BW	Bandwidth	No AGC action	55	75		MHz
CMRR	Common-mode Rejection Ratio	gain = max, Vin = 0 VDC + 100 mVpp @ 5 MHz	40	65		dB
PSRR	Power Supply Rejection Ratio	gain = max, 100 mVpp @ 5 MHz on VCA, VCD, VCD2	45	67		dB
TGD	Gain Decay Time	VIA± = 240 mV to 120 mV VOA± >0.9 Final Value BYP ≤, 1000 pF, IFI = max		34	44	µs
TGA	Gain Attack Time	VIA± = 120 mV to 240 mV VOA± <1.1 Final Value BYP ≤, 1000 pF, IFI = max		1.5	2	µs

EQUALIZER/FILTER (continued)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TLZ	Low Impedance Mode Time	R/$\overline{W}$ transitions from low to high	1.5		3.0	µs

AGC CONTROL

The input signals are AC coupled to DP and DN. Ca = 1000 pF, LEVEL load = 50 µA, SERVO load = 100 µA.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
VDI	DP-DN Signal Input Range				1.4	Vpp
ALO	Level (Servo) Output Gain	DP-DN = 0.25 to 0.5 VDC LG = (V_{LEVEL} - V_{RC})/2 ($_{DP-DN}$)	0.73		0.81	V/V
BWL	Level (Servo) Output Bandwidth	1 dB	15			MHz
VLO	Level Offset Voltage	Output-VRC, IL = 50 µA			30	mV
VSO	Servo Offset Voltage	Output - VRC, IL = 100 µA			30	mV
ZLS	Level (Servo) Output Impedance	IL = 100 µA		200	300	Ω
ID	Discharge Current			0.008 x IFI		mA
IDF	Fast Discharge Current	2.3 to 3.0 µs after R/$\overline{W}$ goes high		20 x ID		mA
ICH	Charge Pump Attack Current			50 x ID		mA
ICHF	Charge Pump Fast Attack Current	DP-DN = 1.35 Vpp		5 x ICH		mA
IBYP	Pin Leakage Current	$\overline{HOLD}$ = low, V_{BYP} = VCC -1.5V	-0.1		0.1	µA
VRC	Reference Voltage		VCC-2.52		VCC-2.15	V
IVRC	Output Drive		-0.75		0.75	mA
VRG	Reference		2.15		2.5	V
IVRG	Source Current		1			mA
VAGC	Pin Voltage			VRC+1.0		V

EQUALIZER/FILTER The input signals are AC coupled to IN+ and IN-.

fc	Filter Cutoff Frequency	*fc* = 19.14(IFI/IFO)(1/Rx)	2.5		13.5	MHz
V_{RX}	PTAT Reference Current Set Output Voltage	TA = 25°C I_{RX} = 0 - 0.7 mA Rx > 1.21 kΩ		850		mV
IFOR	PTAT Reference Current Output Current Range	TA = 25°C 1.21 kΩ < Rx < 7.73 kΩ IFO = V_{RX}/Rx	0.11		0.7	mA

EQUALIZER/FILTER (continued)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
IFIR	PTAT Programming Current Range	TA = 25°C, VRX = 850 mV	0.11		0.7	mA
VBPR	Input Voltage Range		0		VRG	V
IBP	Input Bias Current				3	µA
FCA	Filter FC Accuracy	FC = 5 to 13.5 MHz	-10		+10	%
AO	[(ON±)]/[(IN±)] Normal Gain	F = 0.67 FC	1.4		2.2	V/V
AD	[(OD±)]/[(IN±)] Diff Gain	F = 0.67 FC	1.0AO		1.3AO	V/V
FB	Frequency Boost at FC	FB = 20 log [1.884(VBP-0.1) /VRG+1] VBP -0.1>0	0		9.5	dB
FBA	Frequency Boost Accuracy	FB = max	-1		+1	dB
TGD	Group Delay Variation	0.3 FC to FC = 13.5 MHz FB = 0 to max	-2		+2	%
VOO	Output Offset Voltage	Variation over entire frequency range	-200		+200	mV
VOF	Filter Output Dynamic Range	THD = 1.5% max	1.0			Vpp
		THD = 3.0% max F = 0.67 FC	1.25			Vpp
RINF	Filter Input Resistance		4.0	6.0	8.0	kΩ
CINF	Filter Input Capacitance				7	pF
RO	Filter Output Resistance	IO = 0.5 mA		70	85	Ω
IFOD	Filter Output Drive Current		-1		+1	mA
VNN	Eout Output Noise Voltage ON±	BW = 100 MHz, Rs = 50Ω IFI = 0.7 mA, VBP = 0		2.2	3.0	mVRMS
		BW = 100 MHz, Rs = 50Ω IFI = 0.7 mA, VBP = VRG		3.0	4.5	mVRMS
VND	Eout Output Noise Voltage OD±	BW = 100 MHz, Rs = 50Ω IFI = 0.7 mA, VBP = 0		5.4	6.4	mVRMS
		BW = 100 MHz, Rs = 50Ω IFI = 0.7 mA, VBP = VRG		9.6	10.6	mVRMS

DATA COMPARATOR
The input signals are AC coupled to DP and DN.

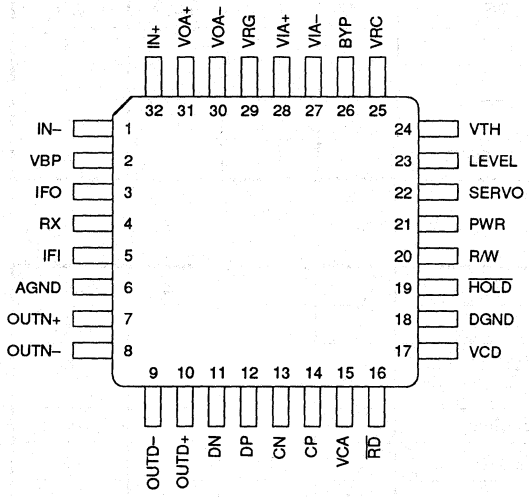
RINDC Differential Input Resistnace		7		14	kΩ
CINDC Differential Input Capacitance				5	pF
ATH Threshold Voltage Gain, Kth	0.3 < VTH-VRC < 0.75	0.42		0.49	V/V
VIAMIN Minimum Threshold Voltage	VTH-VRC ≤ 0.11V		.05		V
TPDDC Propagation Delay	To DOUT		10		ns
ITH VTH Input Bias Current				2	µA
DOUTSS DOUT Signal Swing	2.4 kΩ from DOUT to GND		0.5		V

CLOCKING
The input signals are AC coupled to CP and CN.

RINCL Differential Input Resistance		7		14	kΩ
CINCL Differential Input Capacitance				5	pF
TDS D F/F Set Up Time	DP-DN threshold to CP-CN zero cross	0			ns
TPP Pulse Pairing	Vs = 1Vpp, F = 2.5 MHz			1	ns
TPDCL Propagation Delay to RD	Vs = 20 mVpp sq wave		14	20	ns
RDPW Output Pulse Width	Measured at 1.4V level	10		20	ns
COUTS Signal Swing	2.4 kΩ from COUT to GND		0.5		V

SSI 32P3041
Pulse Detector with Programmable Filter

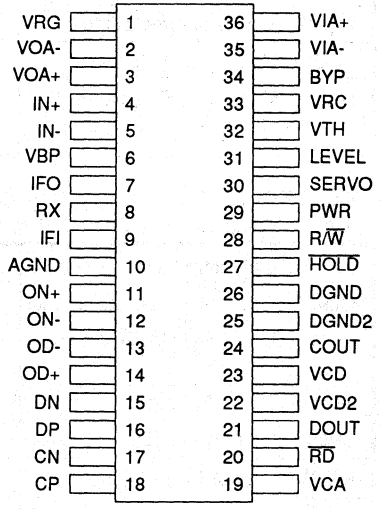
PACKAGE PIN DESIGNATIONS
(Top View)



32-Lead TQFP

THERMAL CHARACTERISTICS: θja

32-Lead TQFP	124° C/W
36-Lead SOM	75° C/W



36-Lead SOM

CAUTION: Use handling procedures necessary for a static sensitive component.

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32P3041		
32-Lead Thin Quad Flatpack	32P3041-CGT	32P3041-CGT
36-Lead Small Outline	32P3041-CM	32P3041-CM

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914

Section 5

PROGRAMMABLE ELECTRONIC FILTERS

silicon systems®
A TDK Group Company

SSI 32F8001
Low-Power Programmable Electronic Filter

October 1993

DESCRIPTION

The SSI 32F8001 Programmable Electronic Filter provides an electronically controlled low–pass filter with a separate differentiated low–pass output. A seven–pole, low–pass filter is provided along with a single-pole, single-zero differentiator. Both outputs have matched delays. The delay matching is unaffected by any amount of programmed equalization or bandwidth. This programability combined with low group delay variation make the SSI 32F8001 ideal for use in constant density recording applications. Pulse slimming equalization is accomplished by a two–pole, low–pass with a two–pole, high–pass feed forward section to provide complimentary real axis zeros. A variable attenuator is used to program the zero locations.

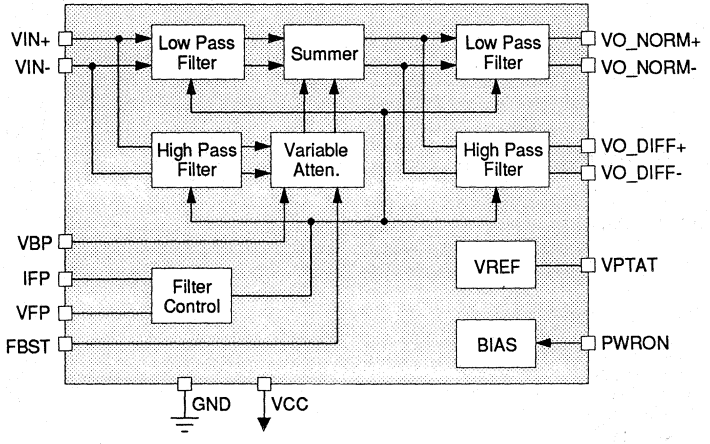
The SSI 32F8001 programmable equalization and bandwidth characteristics can be controlled by external DACs. Fixed characteristics are easily accomplished with three external resistors, in addition equalization can be switched in or out by a logic signal. The SSI 32F8001 requires only a +5V supply and is available in 16-lead SON and SOL packages.

FEATURES

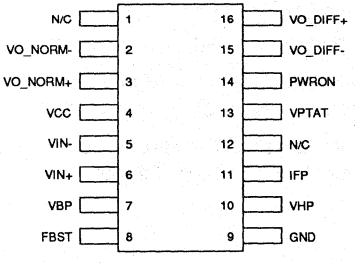
- **Ideal for multi-rate systems applications**
- **Programmable filter cutoff frequency (fc = 9 to 27 MHz, 32F8001)**
- **Programmable pulse slimming equalization (0 to 13.5 dB boost at the filter cutoff frequency)**
- **Matched normal and differentiated low-pass outputs**
- **Differential filter inputs and outputs**
- **±12% cutoff frequency accuracy**
- **±2% maximum group delay variation from 0.2 fc to fc**
- **Total harmonic distortion less than 1%**
- **No external filter components required**
- **+5V only operation**
- **16-lead SON and SOL package**
- **Pin compatible with SSI 32F8011**

5

BLOCK DIAGRAM



PIN DIAGRAM



16-Lead SOL, SON

CAUTION: Use handling procedures necessary for a static sensitive component.

SSI 32F8001
Low-Power Programmable Electronic Filter

FUNCTIONAL DESCRIPTION

The SSI 32F8001 is a high performance programmable electronic filter. It features a 7-pole 0.05° equiripple linear phase filter with matched normal and differentiated outputs.

CUTOFF FREQUENCY PROGRAMMING

The SSI 32F8001 programmable electronic filter can be set to a filter cutoff frequency from 9 to 27 MHz with no boost.

Cutoff frequency programming can be established using either a current source fed into pin IFP whose output current is proportional to the SSI 32F8001 output reference voltage VPTAT, or by means of an external resistor tied from the output voltage reference pin VPTAT to pin VFP. The former method is optimized using the SSI 32D4661 Time Base Generator, since the current source into pin IFP is available at the DAC F output of the SSI 32D4661. Furthermore, the voltage reference input is supplied to pin VR3 of the SSI 32D4661 by the reference voltage from the VPTAT pin of the SSI 32F8001. This reference voltage is internally generated by a band-gap circuit in conjunction with a temperature varying reference to create a voltage which is proportional to absolute temperature.

The VPTAT voltage will compensate for internal temperature variation of the fc and boost circuits.

The cutoff frequency, determined by the -3dB point relative to a very low frequency value (< 10 kHz), is related to the current IVFP injected into pin IFP by the following formulas.

fc (ideal, in MHz)

32F8001 = 45.0 • IFP = 45.0 • IVFP • 1.8/VPTAT

where IFP and IVFP are in mA, 0.2 < IFP < 0.6 mA, VPTAT is in volts, and Ta = 25°C.

If a current source is used to inject current into pin IFP, pin VFP should be left open.

If the SSI 32F8001 cutoff frequency is set using voltage VPTAT to bias up a resistor tied to pin VFP, the cutoff frequency is related to the resistor value by the following formulas.

fc (ideal, in MHz)

32F8001 = 45.0 • IFP = 45.0 • 1.8/(3 • Rx)

Rx in kΩ

If pin VFP is used to program cutoff frequency, pin IFP should be left open.

MAGNITUDE EQUALIZATION PROGRAMMING

The magnitude equalization, measured in dB, is the amount of high frequency peaking at the cutoff frequency relative to the original -3 dB point. For example, when 12 dB boost is applied, the magnitude response peaks up 9 dB above the DC gain.

The amplitude of the input signal at frequencies near the cutoff frequency can be increased using this feature. Applying an external voltage to pin VBP which is proportional to reference output voltage VPTAT (provided by the VPTAT pin) will set the amount of boost. A fixed amount of boost can be set by an external resistor divider network connected from pin VBP to pins VPTAT and GND. No boost is applied if pin FBST, frequency boost enable, is at a low logic level.

The amount of boost FB at the cutoff frequency Fc is related to the voltage VBP by the formula

FB (ideal, in dB) = 20 $\log_{10}$[3.73(VBP/VPTAT)+1], where 0 < VBP < VPTAT.

POWER ON / OFF

The SSI 32F8001 supports a power down mode for minimal idle mode power dissipation. When PWRON is pulled up to logic 1, the device is in normal operation mode. When PWRON is pulled down to logic 0, or left open, the device is in the power down mode.

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
VIN+, VIN-	I	Differential Signal Inputs. The input signals must be AC coupled to these pins.
VO_NORM+, VO_NORM-	O	Differential Normal Outputs. The output signals must be AC coupled.
VO_DIFF+, VO_DIFF-	O	Differential Differentiated Outputs. For minimum time skew, these outputs should be AC coupled.
IFP	I	Frequency Program Input. The filter cutoff frequency fc, is set by an external current IFP, injected into this pin. IFP must be proportional to voltage VPTAT. This current can be set with an external current generator such as a DAC. VFP should be left open when using this pin.
VFP	I	Frequency Program Input. The filter cutoff frequency can be set by programming a current through a resistor from VPTAT to this pin. IFP should be left open when using this pin.
VBP	I	Frequency Boost Program Input. The high frequency boost is set by an external voltage applied to this pin. VBP must be proportional to voltage VPTAT. A fixed amount of boost can be set by an external resistor divider network connected from VBP to VPTAT and GND. No boost is applied if the FBST pin is grounded, or at logic low.
FBST	I	Frequency Boost. A high logic level or open enables the frequency boost circuitry. A low input disables this function.
PWRON	I	Power On. A high logic level enables the chip. A low level or open pin puts the chip in a low power state.
VPTAT	O	PTAT Reference Voltage. This pin outputs a reference voltage which is proportional to absolute temperature (PTAT). VBP, VFP or IFP must be referenced to this pin for proper operation.
VCC	O	+5 Volt Supply.
GND	I	Ground

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ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may damage the device.

PARAMETER	RATINGS
Storage Temperature	-65°C to +150°C
Junction Operating Temperature, Tj	+130°C
Supply Voltage, VCC	-0.5V to 7V
Voltage Applied to Inputs	-0.5V to VCC

ELECTRICAL SPECIFICATIONS (continued)

RECOMMENDED OPERATING CONDITIONS

PARAMETER	RATINGS
Supply voltage, VCC	4.50V < VCC < 5.50V
Ambient Temperature	0°C < Ta < 70°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified recommended operating conditions apply.

Power Supply Characteristics

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Power Supply Current	ICC	PWRON ≤ 0.8V		0.1	0.5	mA
Power Supply Current	ICC	PWRON ≥ 2.0V		46	60	mA
Power Dissipation	PD	PWRON ≥ 2.0V, VCC = 5.0V		230	300	mW
		PWRON ≥ 2.0V, VCC = 5.5V		275	330	mW
		PWRON ≤ 0.8V		0.5	2.5	mW

DC Characteristics

High Level Input Voltage	VIH	TTL input	2.0			V
Low Level Input Voltage	VIL				0.8	V
High Level Input Current	IIH	VIH = 2.7V			20	µA
Low Level Input Current	IIL	VIL = 0.4V	-1.5			mA

Filter Characteristics

Filter Cutoff Frequency *(*f -3dB)	*fc	32F8001 $fc = \frac{45\ \text{MHz}}{\text{mA}}(\text{IVFP})$ IVFP = 0.2 to 0.6 mA, Ta = 25v °C	9.0		27.0	MHz
Filter fc Accuracy	FCA	fc = max.	-12		+12	%
VO_NORM Diff Gain	AO	F = 0.67 fc, FB = 0 dB	0.8		1.2	V/V
VO_DIFF Diff Gain	AD	F = 0.67 fc, FB = 0 dB	0.8AO		1.2AO	V/V
Frequency Boost at fc	FB	VBP = VPTAT fc = max.	12.0	13.5	15.0	dB
		fc = min.	11.5	13.0	14.5	dB
Frequency Boost Accuracy	FBA	VBP/VPTAT = 1.0 fc = max.	-1.5		+1.5	dB
Group Delay Variation Without Boost	TGDO	fc = max., $\frac{\text{VBP}}{\text{VPTAT}}=0$ F = 0.2 fc to fc	-500		+500	ps
		fc = min., $\frac{\text{VBP}}{\text{VPTAT}}=0$ F = 0.2 fc to fc	-1.5		+1.5	ns

FILTER CHARACTERISTICS (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Group Delay Variation TGDO Without Boost (continued)	fc = 9 MHz - 27 MHz F = 0.2 fc to fc $\frac{VBP}{VPTAT}=0$	-2		+2	%
	fc = 9 MHz - 27 MHz, $\frac{VBP}{VPTAT}=0$ F = fc to 1.75 fc	-4		+4	%
Group Delay Variation TGDB with Boost	fc = max, VBP = VPTAT F = 0.2 fc to fc	-500		+500	ps
	fc = min., VBP = VPTAT F = 0.2 to fc	-1.5		+1.5	ns
	fc = 9 MHz - 27 MHz F = 0.2 fc TO fc, VBP = VPTAT	-2.5		+2.5	%
	fc = 9 MHz - 27 MHz, F = fc to 1.75 fc, VBP = VPTAT	-4		+4	%
Filter Input Dynamic Range VIF	THD = 1% max, F = 0.67 fc, VBP = 0V (1000 pF across Rx)	1.0			Vpp
	THD = 1.7% max, F = 0.67 fc, VBP = 0V, Normal output (1000 pF across Rx)	1.5			Vpp
Filter Input Dynamic Range VIF	THD = 3.5% max, F = 0.67 fc, VBP = 0V, Differentiated output (1000 pF across Rx)	1.5			Vpp
Filter Output Dynamic RangeVOF	THD = 1% max, F = 0.67 fc $R_{LOAD} \geq 1k\Omega$ (1000 pF across Rx)	1.0			Vpp
Filter Diff Input Resistance RIN		3.0	4.3		kΩ
Filter Input Capacitance CIN				3	pF
Output Noise Voltage EOUT Differentiated Output	BW = 100 MHz, Rs = 50Ω fc = max, VBP = 0V		3.5	5.4	mVRms
Output Noise Voltage EOUT Normal Output	BW = 100 MHz, Rs = 50Ω fc = max, VBP = 0V		2.3	3.45	mVRms
Output Noise Voltage EOUT Differentiated Output	BW = 100 MHz, Rs = 50Ω fc = max, VBP = VPTAT		7.7	10.75	mVRms
Output Noise Voltage EOUT Normal Output	BW = 100 MHz, Rs = 50Ω fc = max, VBP = VPTAT		3.8	4.75	mVRms
Filter Output Sink Current IO –		1.0			mA
Filter Output Source CurrentIO +				2.0	mA
Filter Output Resistance RO (Single ended)	IO+ = 1.0 mA			60	Ω

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ELECTRICAL SPECIFICATIONS (continued)

FILTER CONTROL CHARACTERISTICS

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Reference Voltage	VPTAT	Tj = 25°C		1.8		V
PTAT Voltage Input	VFP			2/3 VPTAT		V
Programming Current Range	IVFP	Ta = 25°C	0.2		0.6	mA
Programming Voltage Range	V_{VBP}		0		VPTAT	V
Voltage at pin IFP	V_{IFP}	I_{VFP} = 0 mA		2/3 VPTAT		V
Power Up Time		fc = 9 MHz			1.5	µs
		fc = 27 MHz			1.0	µs
Power Down Time					1.0	µs

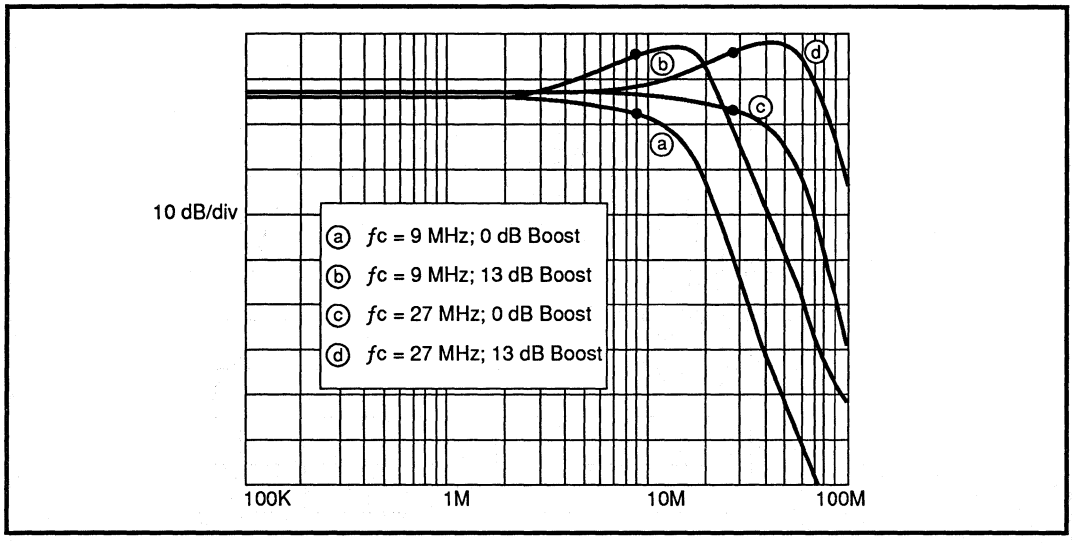


FIGURE 1: 32F8001 Normal Low Pass Response

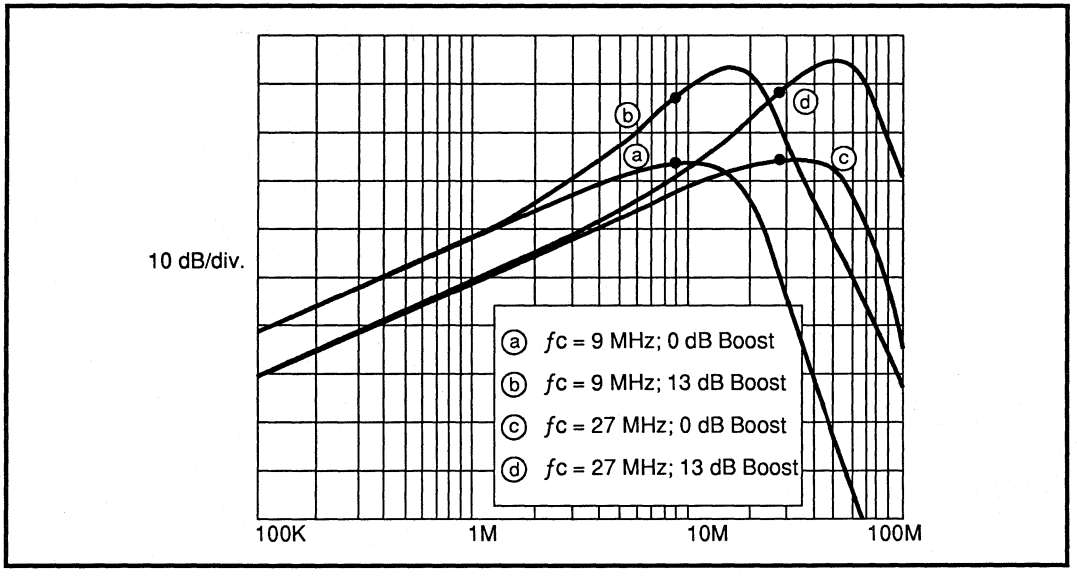


FIGURE 2: 32F8001 Differentiated Low Pass Response

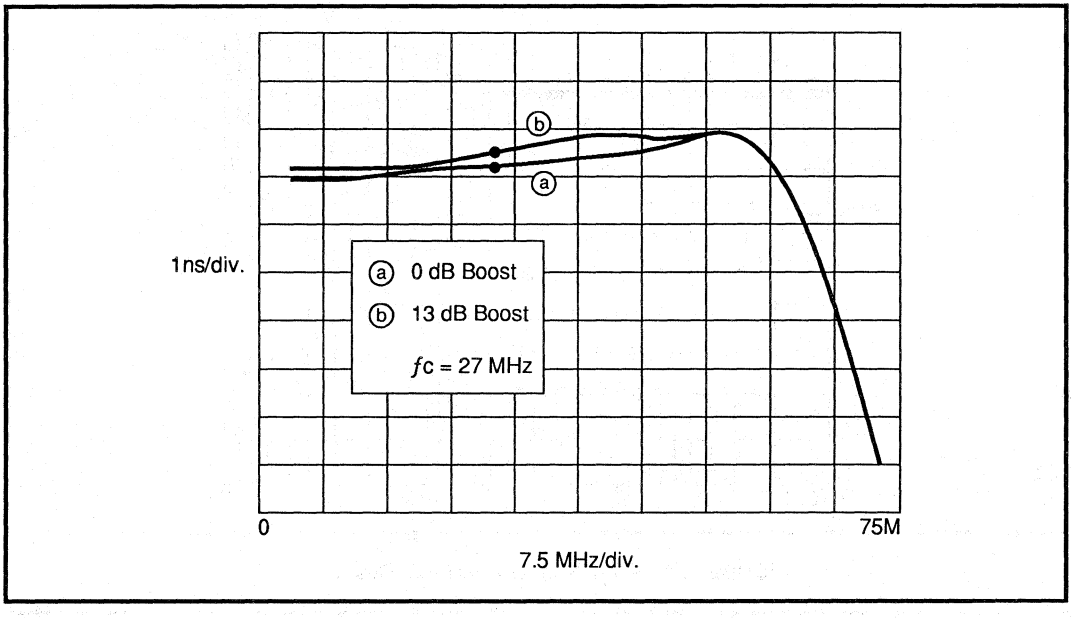
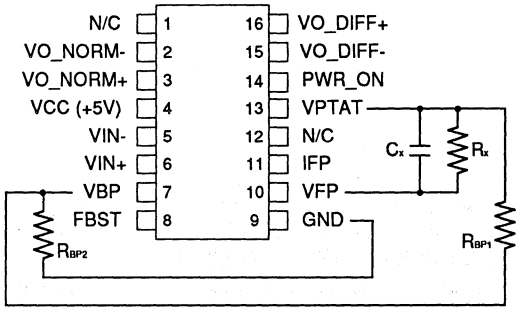


FIGURE 3: 32F8001 Group Delay Response with fc = 27 MHz



VPTAT = 1.8V (25°C)

V_{VFP} = 2/3 (VPTAT)

IVFP range: 0.2 mA to 0.6 mA @25°C

(9 to 27 MHz no boost 32F8001)

Fixed frequency programming is accomplished as shown in the drawing above.

In this case IVFP (programming current) is equivalent to $\frac{VPTAT}{3} \cdot \frac{1}{R_x}$

i.e., fc = 27 MHz then

IVFP = 0.6 mA @25°C Rx = 1 KΩ

Fixed boost programming is also accomplished as shown above. In this case V_{VBP} is set by a voltage divider, where V_{VBP} is a fraction of VPTAT.

i.e., boost = 9 dB then,

VBP/VPTAT = 0.488 9 dB = 20 log [3.73 (0.488) + 1]

$$\frac{R_{BP2}}{R_{BP1}} = \frac{1}{\left(\frac{VPTAT}{VBP} - 1\right)} = 0.953$$

Cx = 1000 pF - Cx is needed for lower THD at lower fc.

FIGURE 4: 32F8001 Applications Setup

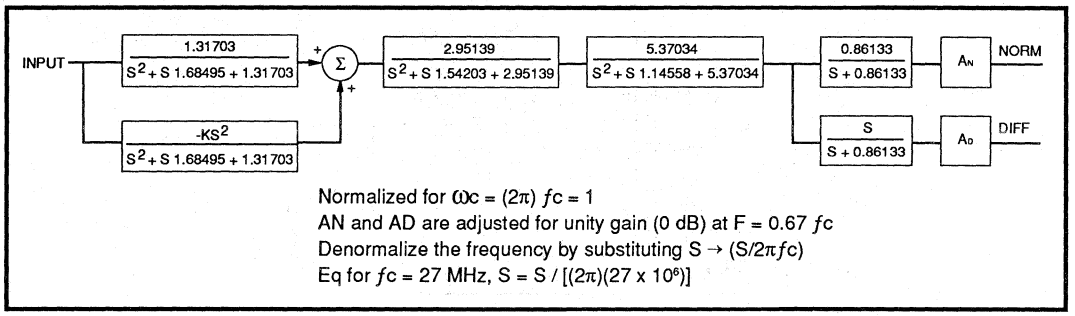


FIGURE 5: 32F8001 Normalized Block Diagram

TABLE 1: 32F8001 Frequency Boost Calculations, K = 1.31703 (10 BOOST (dB)/20 - 1)

Assuming 13 dB boost for VBP = VPTAT

$$\frac{VBP}{VPTAT} \cong \frac{(10^{(FB/20)}) - 1}{3.73}$$

Boost	K	VBP/VPTAT	Boost	K	VBP/VPTAT
1 dB	0.16	0.033	6 dB	1.31	0.267
2 dB	0.34	0.069	7 dB	1.63	0.332
3 dB	0.54	0.110	8 dB	1.99	0.405
4 dB	0.77	0.157	9 dB	2.40	0.488
5 dB	1.03	0.209	10 dB	2.85	0.580
			11 dB	3.36	0.683
			12 dB	3.43	0.799
			13 dB	4.57	0.929

or,

$$\text{boost in dB} = 20\log\left[3.73\left(\frac{VBP}{VPTAT}\right)+1\right]$$

VBP/VPTAT	Boost	VBP/VPTAT	Boost
0.1	2.753 dB	0.6	10.206 dB
0.2	4.841 dB	0.7	11.153 dB
0.3	6.523 dB	0.8	12.006 dB
0.4	7.391 dB	0.9	12.784 dB
0.5	9.142 dB	1.0	13.5 dB

TABLE 2: Calculations

Typical change in f-3 dB point with boost

Boost (dB)	Gain@fc (dB)	Gain@ peak (dB)	$f$peak/fc	f-3dB/fc
0	-3	0.00	no peak	1.00
1	-2	0.00	no peak	1.21
2	-1	0.00	no peak	1.51
3	0	0.15	0.70	1.80
4	1	0.99	1.05	2.04
5	2	2.15	1.23	2.20
6	3	3.41	1.33	2.33
7	4	4.68	1.38	2.43
8	5	5.94	1.43	2.51
9	6	7.18	1.46	2.59
10	7	8.40	1.48	2.66
11	8	9.59	1.51	2.73
12	9	10.77	1.51	2.80
13	10	11.92	1.53	2.87
14	11	13.06	1.53	2.93

Notes: 1. fc is the original programmed cutoff frequency with no boost

2. f-3 dB is the new -3 dB value with boost implemented

3. $f$peak is the frequency where the amplitude reaches its maximum value with boost implemented

i.e., fc = 9 MHz when boost = 0 dB

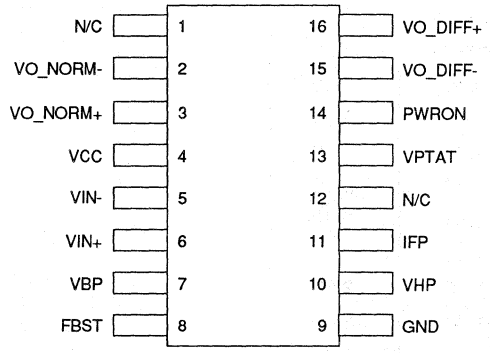
if boost is programmed to 5 dB then f-3 dB = 19.8 MHz

$f$peak = 11.07 MHz

5

SSI 32F8001
Low-Power Programmable Electronic Filter

PACKAGE PIN DESIGNATIONS
(Top View)



16-Lead SON, SOL

THERMAL CHARACTERISTICS: θja

16-lead SON (150 mil)	105°C/W
16-lead SOL (300 mil)	100°C/W

CAUTION: Use handling procedures necessary for a static sensitive component.

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32F8001		
16-Lead SOL	32F8001-CL	32F8001-CL
16-Lead SON	32F8001-CN	32F8001-CN

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914

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A TDK Group Company

SSI 32F8002/8003
Low-Power Programmable Electronic Filter
Preliminary Data

December 1993

DESCRIPTION

The SSI 32F8002/8003 Programmable Electronic Filters provide an electronically controlled low–pass filter with a separate differentiated low–pass output. A seven–pole, low–pass filter is provided along with a single-pole, single-zero differentiator. Both outputs have matched delays. The delay matching is unaffected by any amount of programmed equalization or bandwidth. This programability combined with low group delay variation make the SSI 32F8002/8003 ideal for use in constant density recording applications. Pulse slimming equalization is accomplished by a two–pole, low–pass with a two–pole, high–pass feed forward section to provide complimentary real axis zeros. A variable attenuator is used to program the zero locations.

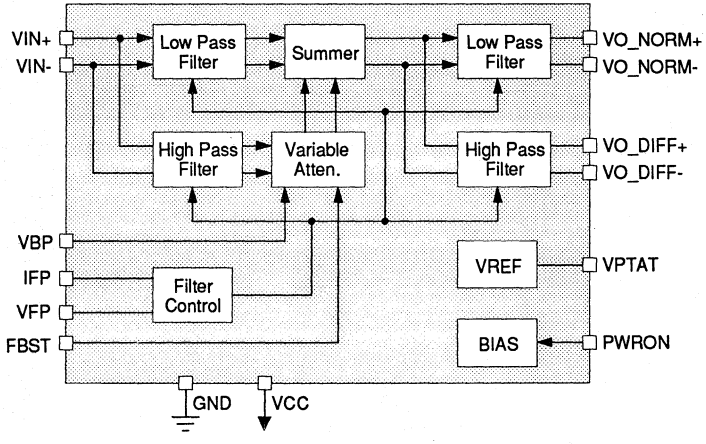
The SSI 32F8002/8003 programmable equalization and bandwidth characteristics can be controlled by external DACs. Fixed characteristics are easily accomplished with three external resistors, in addition equalization can be switched in or out by a logic signal. The SSI 32F8002/8003 require only a +5V supply and is available in 16-lead SON and SOL packages.

FEATURES

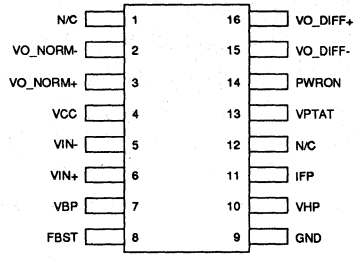
- **Ideal for multi-rate systems applications**
- **Programmable filter cutoff frequency (fc = 6 to 18 MHz, 32F8002; fc = 4 to 13 MHz, 32F8003)**
- **Programmable pulse slimming equalization (0 to 13.5 dB boost at the filter cutoff frequency)**
- **Matched normal and differentiated low-pass outputs**
- **Differential filter inputs and outputs**
- **±10% cutoff frequency accuracy**
- **±2% maximum group delay variation from 0.2 fc to fc**
- **Total harmonic distortion less than 1%**
- **No external filter components required**
- **+5V only operation**
- **16-lead SON and SOL package**
- **Pin compatible with SSI 32F8011**

5

BLOCK DIAGRAM



PIN DIAGRAM



16-Lead SOL, SON

CAUTION: Use handling procedures necessary for a static sensitive component.

SSI 32F8002/8003
Low-Power Programmable Electronic Filter

FUNCTIONAL DESCRIPTION

The SSI 32F8002/8003 are high performance programmable electronic filter. They feature a 7-pole 0.05° equiripple linear phase filter with matched normal and differentiated outputs.

CUTOFF FREQUENCY PROGRAMMING

The SSI 32F8001 programmable electronic filter can be set to a filter cutoff frequency from 9 to 27 MHz with no boost.

Cutoff frequency programming can be established using either a current source fed into pin IFP whose output current is proportional to the SSI 32F8001 output reference voltage VPTAT, or by means of an external resistor tied from the output voltage reference pin VPTAT to pin VFP. The former method is optimized using the SSI 32D4661 Time Base Generator, since the current source into pin IFP is available at the DAC F output of the SSI 32D4661. Furthermore, the voltage reference input is supplied to pin VR3 of the SSI 32D4661 by the reference voltage from the VPTAT pin of the SSI 32F8001. This reference voltage is internally generated by a band-gap circuit in conjunction with a temperature varying reference to create a voltage which is proportional to absolute temperature.

The VPTAT voltage will compensate for internal temperature variation of the fc and boost circuits.

The cutoff frequency, determined by the -3dB point relative to a very low frequency value (< 10 kHz), is related to the current IVFP injected into pin IFP by the following formulas.

fc (ideal, in MHz)

32F8002 = 30.0 • IFP = 30.0 • IVFP • 1.8/VPTAT

32F8003 = 21.67 • IFP = 21.67 • IVFP • 1.8/VPTAT

where IFP and IVFP are in mA, VPTAT is in volts, Ta = 25°C, 0.2 mA ≤ IFP ≤ 0.6 mA for F8002, and 0.185 ≤ IFP ≤ 0.6 mA for F8003.

If a current source is used to inject current into pin IFP, pin VFP should be left open.

If the SSI 32F8002/8003 cutoff frequency is set using voltage VPTAT to bias up a resistor tied to pin VFP, the cutoff frequency is related to the resistor value by the following formulas.

fc (ideal, in MHz)

32F8002 = 30.0 • IFP = 30.0 • 1.8/(3 • Rx)

32F8003 = 21.67 • IFP = 21.67 • 1.8/(3 • Rx)

Rx in kΩ

If pin VFP is used to program cutoff frequency, pin IFP should be left open.

MAGNITUDE EQUALIZATION PROGRAMMING

The magnitude equalization, measured in dB, is the amount of high frequency peaking at the cutoff frequency relative to the original -3 dB point. For example, when 12 dB boost is applied, the magnitude response peaks up 9 dB above the DC gain.

The amplitude of the input signal at frequencies near the cutoff frequency can be increased using this feature. Applying an external voltage to pin VBP which is proportional to reference output voltage VPTAT (provided by the VPTAT pin) will set the amount of boost. A fixed amount of boost can be set by an external resistor divider network connected from pin VBP to pins VPTAT and GND. No boost is applied if pin FBST, frequency boost enable, is at a low logic level.

The amount of boost FB at the cutoff frequency Fc is related to the voltage VBP by the formula

FB (ideal, in dB) = 20 $\log_{10}$[3.73(VBP/VPTAT)+1], where 0 < VBP < VPTAT.

POWER ON / OFF

The SSI 32F8002/8003 support a Power Down mode for minimal Idle mode power dissipation. When PWRON is pulled up to TTL logic high, the device is in Normal Operation mode. When PWRON is pulled down to TTL logic low, or left open, the device is in the Power Down mode.

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
VIN+, VIN-	I	Differential Signal Inputs. The input signals must be AC coupled to these pins.
VO_NORM+, VO_NORM-	O	Differential Normal Outputs. The output signals must be AC coupled.
VO_DIFF+, VO_DIFF-	O	Differential Differentiated Outputs. For minimum time skew, these outputs should be AC coupled.
IFP	I	Frequency Program Input. The filter cutoff frequency fc, is set by an external current IFP, injected into this pin. IFP must be proportional to voltage VPTAT. This current can be set with an external current generator such as a DAC. VFP should be left open when using this pin.
VFP	I	Frequency Program Input. The filter cutoff frequency can be set by programming a current through a resistor from VPTAT to this pin. IFP should be left open when using this pin.
VBP	I	Frequency Boost Program Input. The high frequency boost is set by an external voltage applied to this pin. VBP must be proportional to voltage VPTAT. A fixed amount of boost can be set by an external resistor divider network connected from VBP to VPTAT and GND. No boost is applied if the FBST pin is grounded, or at logic low.
FBST	I	Frequency Boost. A high logic level or open enables the frequency boost circuitry. A low input disables this function.
PWRON	I	Power On. A high logic level enables the chip. A low level or open pin puts the chip in a low power state.
VPTAT	O	PTAT Reference Voltage. This pin outputs a reference voltage which is proportional to absolute temperature (PTAT). VBP, VFP or IFP must be referenced to this pin for proper operation.
VCC	O	+5 Volt Supply.
GND	I	Ground

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may damage the device.

PARAMETER	RATINGS
Storage Temperature	-65°C to +150°C
Junction Operating Temperature, Tj	+130°C
Supply Voltage, VCC	-0.5V to 7V
Voltage Applied to Inputs	-0.5V to VCC

ELECTRICAL SPECIFICATIONS (continued)

RECOMMENDED OPERATING CONDITIONS

PARAMETER	RATINGS
Supply voltage, VCC	4.50V < VCC < 5.50V
Ambient Temperature	0°C < Ta < 70°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified recommended operating conditions apply.

Power Supply Characteristics

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Power Supply Current	ICC	PWRON ≤ 0.8V		0.1	0.5	mA
Power Supply Current	ICC	PWRON ≥ 2.0V		46	60	mA
Power Dissipation	PD	PWRON ≥ 2.0V, VCC = 5.0V		230	300	mW
		PWRON ≥ 2.0V, VCC = 5.5V		275	330	mW
		PWRON ≤ 0.8V		0.5	2.5	mW

DC Characteristics

High Level Input Voltage	VIH	TTL input	2.0			V
Low Level Input Voltage	VIL				0.8	V
High Level Input Current	IIH	VIH = 2.7V			20	µA
Low Level Input Current	IIL	VIL = 0.4V	-1.5			mA

Filter Characteristics

Filter Cutoff Frequency *(*f* -3dB)	**fc*	32F8002 $fc = \frac{30\,MHz}{mA}(IVFP)$	6.0		18.0	MHz
		32F8003 $fc = \frac{21.67\,MHz}{mA}(IVFP)$	4		13	MHz
Filter *fc* Accuracy	FCA	*fc* = max.	-10		+10	%
VO_NORM Diff Gain	AO	F = 0.67 *fc*, FB = 0 dB	0.8		1.2	V/V
VO_DIFF Diff Gain	AD	F = 0.67 *fc*, FB = 0 dB	0.8AO		1.2AO	V/V
Frequency Boost at *fc*	FB	VBP = VPTAT *fc* = max.	12.0	13.5	15.0	dB
		fc = min.	11.5	13.0	14.5	dB
Frequency Boost Accuracy	FBA	VBP/VPTAT = 1.0 *fc* = max.	-1.5		+1.5	dB

FILTER CHARACTERISTICS (continued)

PARAMETER	CONDITIONS		MIN	NOM	MAX	UNIT
Group Delay Variation TGDO Without Boost (continued)	fc = max, $\frac{VBP}{VPTAT}=0$	8002	-750		+750	ps
	F = 0.2 fc to fc	8003	-1		+1	ns
	fc = min, $\frac{VBP}{VPTAT}=0$	8002	-2.25		+2.25	ns
	F = 0.2 fc to fc	8003	-3		+3	ns
	fc = 6 - 18 MHz, fc = 4 - 13 MHz, F = 0.2 fc to fc, $\frac{VBP}{VPTAT}=0$	8002 8003	-2		+2	%
	fc = 6 - 18 MHz, fc = 4 - 13 MHz, F = fc to 1.75 fc $\frac{VBP}{VPTAT}=0$	8002 8003	-3		+3	%
Group Delay Variation TGDB With Boost	fc = max, VBP = VPTAT	8002	-750		+750	ps
	F = 0.2 fc to fc	8003	-1		+1	ns
	fc = min, VBP = VPTAT	8002	-2.25		+2.25	ns
	F = 0.2 to fc	8003	-3		+3	ns
	fc = 6 - 18 MHz, fc = 4 - 13 MHz, F = 0.2 fc TO fc, VBP = VPTAT	8002 8003	-2		+2	%
	fc = 6 - 18 MHz, fc = 4 - 13 MHz, F = fc to 1.75 fc, VBP = VPTAT	8002 8003	-3		+3	%
Filter Input Dynamic Range VIF	THD = 1% max, F = 0.67 fc, VBP = 0V (1000 pF across Rx)		1			Vpp
	THD = 1.5% max, F = 0.67 fc, VBP = 0V, Normal output (1000 pF across Rx)		1.5			Vpp
Filter Input Dynamic Range VIF	THD = 2.0% max, F = 0.67 fc, VBP = 0V, Differentiated output (1000 pF across Rx)		1.5			Vpp
Filter Output Dynamic RangeVOF	THD = 1% max, F = 0.67 fc $R_{LOAD} \geq 1k\Omega$ (1000 pF across Rx)		1			Vpp
Filter Diff Input Resistance RIN			3	4.3		kΩ
Filter Input Capacitance CIN					7	pF
Output Noise Voltage EOUT	BW = 100 MHz, Rs = 50Ω	8002		3.3		mVRms
Differentiated Output	fc = max, VBP = 0V	8003		3		mVRms

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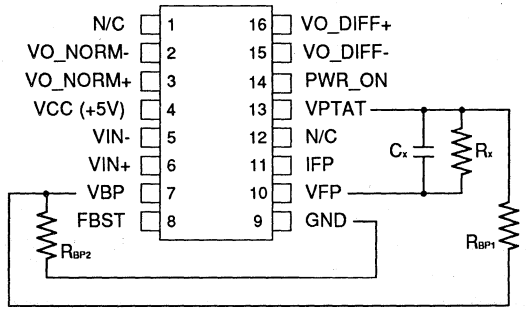
ELECTRICAL SPECIFICATIONS (continued)

FILTER CONTROL CHARACTERISTICS

PARAMETER		CONDITIONS		MIN	NOM	MAX	UNIT
Output Noise Voltage	EOUT	BW = 100 MHz, Rs = 50Ω	8002		2		mVRms
Normal Output		fc = max, VBP = 0V	8003		1.8		mVRms
Output Noise Voltage	EOUT	BW = 100 MHz, Rs = 50Ω	8002		5.0		mVRms
Differentiated Output		fc = max, VBP = VPTAT	8003		4.3		mVRms
Output Noise Voltage	EOUT	BW = 100 MHz, Rs = 50Ω	8002		2.5		mVRms
Normal Output		fc = max, VBP = VPTAT	8003		2.2		mVRms
Filter Output Sink Current	IO –			1			mA
Filter Output Source Current	IO +					2	mA
Filter Output Resistance (Single ended)	RO	IO+ = 1.0 mA				60	Ω
Reference Voltage	VPTAT	Tj = 25°C			1.8		V
PTAT Voltage Input	VFP				2/3 VPTAT		V
Programming Current	IVFP	Ta = 25°C	8002	0.2		0.6	mA
Range			8003	0.185		0.6	mA
Programming Voltage Range	V_{VBP}			0		VPTAT	V
Voltage at pin IFP	V_{IFP}	I_{VFP} = 0 mA			2/3 VPTAT		V
Power Up Time		fc = min				1.5	µs
		fc = max				1	µs
Power Down Time						1	µs



VPTAT = 1.8V (25°C)

V_{VFP} = 2/3 (VPTAT)

IVFP range: 0.2 mA to 0.6 mA @25°C, 32F8002

IVFP range: 0.185 mA to 0.6 mA @25°C, 32F8003

Fixed frequency programming is accomplished as shown in the drawing above.

In this case IVFP (programming current) is equivalent to $\frac{VPTAT}{3} \cdot \frac{1}{R_x}$

i.e., fc = 27 MHz then

IVFP = 0.6 mA @25°C Rx = 1 KΩ

Fixed boost programming is also accomplished as shown above. In this case V_{VBP} is set by a voltage divider, where V_{VBP} is a fraction of VPTAT.

i.e., boost = 9 dB then,

VBP/VPTAT = 0.488 9 dB = 20 log [3.73 (0.488) + 1]

$$\frac{R_{BP2}}{R_{BP1}} = \frac{1}{\left(\frac{VPTAT}{VBP} - 1\right)} = 0.953$$

Cx = 1000 pF - Cx is needed for lower THD at lower fc.

FIGURE 4: 32F8002/8003 Applications Setup

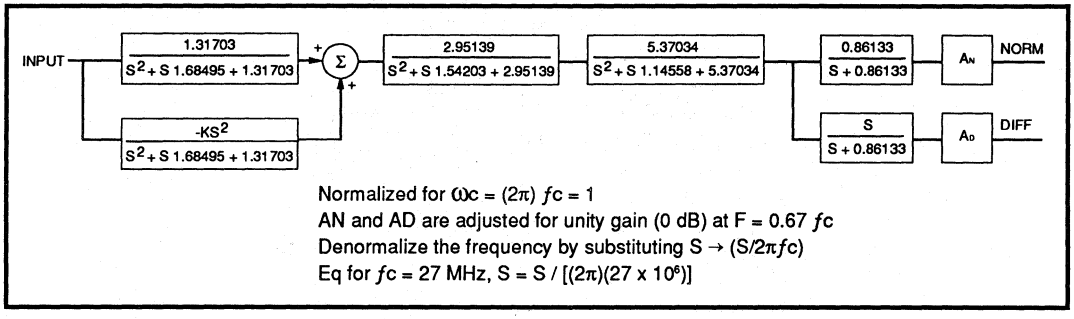


FIGURE 5: 32F8001 Normalized Block Diagram

TABLE 1: 32F8001 Frequency Boost Calculations, K = 1.31703 ($10^{\text{BOOST (dB)}/20} - 1$)

Assuming 13 dB boost for VBP = VPTAT

$$\frac{VBP}{VPTAT} \cong \frac{(10^{(FB/20)}) - 1}{3.73}$$

Boost	K	VBP / VPTAT	Boost	K	VBP / VPTAT
1 dB	0.16	0.033	6 dB	1.31	0.267
2 dB	0.34	0.069	7 dB	1.63	0.332
3 dB	0.54	0.110	8 dB	1.99	0.405
4 dB	0.77	0.157	9 dB	2.40	0.488
5 dB	1.03	0.209	10 dB	2.85	0.580
			11 dB	3.36	0.683
			12 dB	3.43	0.799
			13 dB	4.57	0.929

or,

$$\text{boost in dB} = 20\log\left[3.73\left(\frac{VBP}{VPTAT}\right)+1\right]$$

VBP / VPTAT	Boost	VBP / VPTAT	Boost
0.1	2.753 dB	0.6	10.206 dB
0.2	4.841 dB	0.7	11.153 dB
0.3	6.523 dB	0.8	12.006 dB
0.4	7.391 dB	0.9	12.784 dB
0.5	9.142 dB	1.0	13.5 dB

TABLE 2: Calculations

Typical change in f-3 dB point with boost

Boost (dB)	Gain@fc (dB)	Gain@ peak (dB)	$f$peak/fc	f-3dB/fc
0	-3	0.00	no peak	1.00
1	-2	0.00	no peak	1.21
2	-1	0.00	no peak	1.51
3	0	0.15	0.70	1.80
4	1	0.99	1.05	2.04
5	2	2.15	1.23	2.20
6	3	3.41	1.33	2.33
7	4	4.68	1.38	2.43
8	5	5.94	1.43	2.51
9	6	7.18	1.46	2.59
10	7	8.40	1.48	2.66
11	8	9.59	1.51	2.73
12	9	10.77	1.51	2.80
13	10	11.92	1.53	2.87
14	11	13.06	1.53	2.93

Notes: 1. fc is the original programmed cutoff frequency with no boost

2. f-3 dB is the new -3 dB value with boost implemented

3. $f$peak is the frequency where the amplitude reaches its maximum value with boost implemented

i.e., fc = 9 MHz when boost = 0 dB

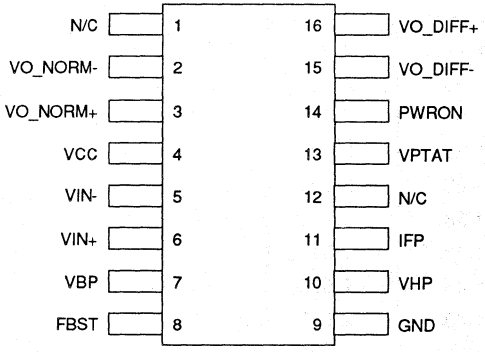
if boost is programmed to 5 dB then f-3 dB = 19.8 MHz

$f$peak = 11.07 MHz

5

SSI 32F8002/8003
Low-Power Programmable Electronic Filter

PACKAGE PIN DESIGNATIONS
(Top View)



16-Lead SON, SOL

THERMAL CHARACTERISTICS: θja

16-lead SON (150 mil)	105°C/W
16-lead SOL (300 mil)	100°C/W

CAUTION: Use handling procedures necessary for a static sensitive component.

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32F8002		
16-Lead SOL	32F8002-CL	32F8002-CL
16-Lead SON	32F8002-CN	32F8002-CN
SSI 32F8003		
16-Lead SOL	32F8003-CL	32F8003-CL
16-Lead SON	32F8003-CN	32F8003-CN

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914

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SSI 32F8011/8012
Programmable Electronic Filter

December 1993

DESCRIPTION

The SSI 32F8011/8012 Programmable Electronic Filter provides an electronically controlled low–pass filter with a separate differentiated low–pass output. A seven–pole, Bessel–type, low–pass filter is provided along with a single-pole, single-zero differentiator. Both outputs have matched delays. The delay matching is unaffected by any amount of programmed high frequency peaking (boost) or bandwidth. This programmability, combined with low group delay variation makes the SSI 32F8011/8012 ideal for use in many applications. Double differentiation high frequency boost is accomplished by a two–pole, low–pass with a two–pole, high–pass feed forward section to provide complementary real axis zeros. A variable attenuator is used to program the zero locations, which controls the amount of boost.

The SSI 32F8011/8012 programmable boost and bandwidth characteristics can be controlled by external DACs or DACs provided in the SSI 32D4661 Time Base Generator. Fixed characteristics are easily accomplished with three external resistors, in addition boost can be switched in or out by a logic signal.

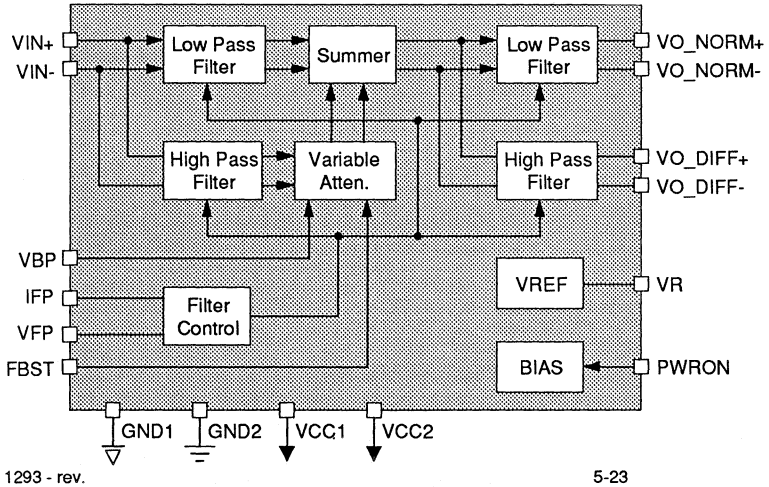
The SSI 32F8011/8012 requires only a +5V supply and is available in 16-pin SON and SOL packages.

FEATURES

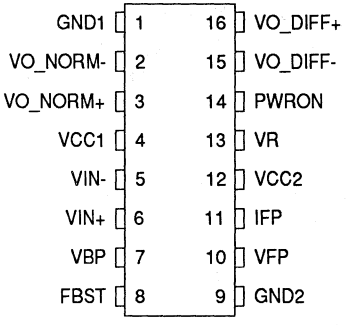
- **Ideal for:**
  - **constant density recording applications**
  - **cellular telephone applications**
  - **radio**
  - **data acquisition**
  - **LAN**
- **Programmable filter cutoff frequency**
  (SSI 32F8011 *fc* = 5 to 13 MHz)
  (SSI 32F8012 *fc* = 6 to 15 MHz)
- **Programmable high frequency peaking**
  (0 to 9.5 dB boost at the filter cutoff frequency)
- **Matched normal and differentiated low-pass outputs**
- **Differential filter input and outputs**
- **±0.75 ns group delay variation from 0.2 *fc* to *fc* = 13 MHz**
- **Total harmonic distortion less than 1%**
- **+5V only operation**
- **16-lead SON, and SOL packages**

5

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

SSI 32F8011/8012 Programmable Electronic Filter

FUNCTIONAL DESCRIPTION

The SSI 32F8011/8012, a high performance programmable electronic filter, provides a low pass Bessel-type seven pole filter with matched normal and differentiated outputs. The device has been optimized for usage with several Silicon Systems products, including the SSI 32D4661 Time Base Generator, the SSI 32P54x family of Pulse Detectors, and the SSI 32P4720 Combo chip (Data Separator and Pulse Detector).

CUTOFF FREQUENCY PROGRAMMING

The programmable electronic filter can be set to a filter cutoff frequency from 5 to 13 MHz (with no boost) for SSI 32F8011 and 6 to 15 MHz for SSI 32F8012.

Cutoff frequency programming can be established using either a current source fed into pin IFP whose output current is proportional to the SSI 32F8011/8012 output reference voltage VR, or by means of an external resistor tied from the output voltage reference pin VR to pin VFP. The former method is optimized using the SSI 32D4661 Time Base Generator, since the current source into pin IFP is available at the DAC F output of the 32D4661. Furthermore, the voltage reference input is supplied to pin VR3 of the 32D4661 by the reference voltage VR from the VR pin of the 32F8011/8012. This reference voltage is an internally generated bandgap reference, which typically varies less than 1% over supply voltage and temperature variation.

The cutoff frequency, determined by the -3dB point relative to a very low frequency value (< 10 kHz), is related to the current IVFP injected into pin IFP by the following formulas.

SSI 32F8011
Fc (ideal, in MHz) = 16.25•IFP = 16.25•IVFP•2.2/VR

SSI 32F8012
Fc (ideal, in MHz) = 18.75•IFP = 18.75•IVFP•2.2/VR
where IFP and IVFP are in mA, 0.31<IFP<0.8 mA, and VR is in volts.

If a current source is used to inject current into pin IFP, pin VFP should be left open.

If the 32F8011/8012 cutoff frequency is set using voltage VR to bias up a resistor tied to pin VFP, the cutoff frequency is related to the resistor value by the following formulas.

SSI 32F8011
Fc (ideal, in MHz) = 16.25•IFP = 16.25•2.2/(3•Rx)

SSI 32F8012
Fc (ideal, in MHz) = 18.75•IFP = 18.75•2.2/(3•Rx)
where Rx is in kΩ, 0.917<Rx<2.366 kΩ.

If pin VFP is used to program cutoff frequency, pin IFP should be left open.

SLIMMER HIGH FREQUENCY BOOST PROGRAMMING

The amplitude of the output signal at frequencies near the cutoff frequency can be increased using this feature. Applying an external voltage to pin VBP which is proportional to reference output voltage VR (provided by the VR pin) will set the amount of boost. A fixed amount of boost can be set by an external resistor divider network connected from pin VBP to pins VR and GND. No boost is applied if pin FBST, frequency boost enable, is at a low logic level.

The amount of boost FB at the cutoff frequency Fc is related to the voltage VBP by the formula

FB (ideal, in dB) = $20 \log_{10}[1.884(VBP/VR)+1]$, where 0<VBP<VR.

PIN DESCRIPTION

NAME	DESCRIPTION
VIN+, VIN-	DIFFERENTIAL SIGNAL INPUTS. The input signals must be AC coupled to these pins.
VO_NORM+, VO_NORM-	DIFFERENTIAL NORMAL OUTPUTS. The output signals must be AC coupled.
VO_DIFF+, VO_DIFF-	DIFFERENTIAL DIFFERENTIATED OUTPUTS. For minimum time skew, these outputs should be AC coupled to the pulse detector.
IFP	FREQUENCY PROGRAM INPUT. The filter cutoff frequency FC, is set by an external current IFP, injected into this pin. IFP must be proportional to voltage VR. This current can be set with an external current generator such as a DAC. VFP should be left open when using this pin.
VFP	FREQUENCY PROGRAM INPUT. The filter cutoff frequency can be set by programming a current through a resistor from VR to this pin. IFP should be left open when using this pin.
VBP	FREQUENCY BOOST PROGRAM INPUT. The high frequency boost is set by an external voltage applied to this pin. VBP must be proportional to voltage VR. A fixed amount of boost can be set by an external resistor divider network connected from VBP to VR and GND. No boost is applied if the FBST pin is grounded, or at logic low.
FBST	FREQUENCY BOOST. A high logic level or open input enables the frequency boost circuitry.
PWRON	POWER ON. A high logic level or open circuit enables the chip. A low level puts the chip in a low power state.
VR	REFERENCE VOLTAGE. Internally generated reference voltage.
VCC1, VCC2	+5 VOLT SUPPLY.
GND1, GND2	GROUND

5

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may damage the device.

PARAMETER	RATINGS
Storage Temperature	-65 to +150°C
Junction Operating Temperature, Tj	+130°C
Supply Voltage, VCC1, VCC2	-0.5 to 7V
Voltage Applied to Inputs	-0.5 to VCC + 0.5V
IFP, VFP Inputs Maximum Current*	≤1.2mA

* Exceeding this current may cause frequency programming lockup.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	RATINGS
Supply voltage, VCC1, VCC2	4.5 < VCC1,2 < 5.5V
Ambient Temperature	0 < Ta < 70°C

ELECTRICAL CHARACTERISTICS

Power Supply Characteristics (Unless otherwise specified, recommended operating conditions apply.)

PARAMETER		CONDITIONS		MIN	NOM	MAX	UNITS
ICC	Power Supply Current	PWRON ≤ 0.8V	VBP = VR		14	17	mA
			VBP = 0V		12	15	mA
ICC	Power Supply Current	PWRON ≥ 2.0V			67	80	mA

DC Characteristics

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
VIH	High Level Input Voltage	TTL input	2.0		VCC+0.3	V
VIL	Low Level Input Voltage		-0.3		0.8	V
IIH	High Level Input Current	VIH = 2.7V			20	µA
IIL	Low Level Input Current	VIL = 0.4V	–1.5			mA

Filter Characteristics

PARAMETER		CONDITIONS		MIN	NOM	MAX	UNITS
FCA	Filter *fc* Accuracy	using VFP pin	32F8011	11.7		14.3	MHz
		Rx = 0.917 kΩ	32F8012	13.5		16.5	MHz
AO	VO_NORM Diff Gain	F = 0.67 *fc*, FB = 0 dB		0.8		1.20	V/V
AD	VO_DIFF Diff Gain	F = 0.67 *fc*, FB = 0 dB		0.8AO		1.0AO	V/V
FBA	Frequency Boost Accuracy	VBP = VR @ *fc* = 5 MHz		8.5	9.5	10.5	dB
TGD0	Group Delay Variation Without Boost*	*fc* = Max *fc*, VBP = 0V F = 0.2 *fc* to *fc*		–0.75		+0.75	ns
TGDB	Group Delay Variation With Boost*	*fc* = Max *fc*, VBP = VR F = 0.2 *fc* to *fc*		–0.75		+0.75	ns
VIF	Filter Input Dynamic Range	THD = 1% max, F = 0.67 *fc* (no boost)		1.5			Vpp
VOF	Filter Output Dynamic Range	THD = 1% max, F = 0.67 *fc*		1.5			Vpp
RIN	Filter Diff Input Resistance			3.0	3.8		kΩ
CIN	Filter Diff Input Capacitance*				2.5	7	pF
EOUT	Output Noise Voltage* Differentiated Output	BW = 100 MHz, Rs = 50Ω, I*fp* = 0.8 mA, VBP = 0.0V			5.5	6.8	mVRms
EOUT	Output Noise Voltage* Normal Output	BW = 100 MHz, Rs = 50Ω I*fp* = 0.8 mA, VBP = 0.0V			2.75	3.6	mVRms
EOUT	Output Noise Voltage* Differentiated Output	BW = 100 MHz, Rs = 50Ω I*fp* = 0.8 mA, VBP = VR			6.0	8.1	mVRms
EOUT	Output Noise Voltage* Normal Output	BW = 100 MHz, Rs = 50Ω I*fp* = 0.8 mA, VBP = VR			3.25	4.4	mVRms

* Not directly testable in production, design characteristic.

ELECTRICAL CHARACTERISTICS (continued)

Filter Characteristics (continued)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
IO–	Filter Output Sink Current		1.0			mA
IO+	Filter Output Source Current		2.0			mA
RO	Filter Output Resistance Single ended	Source Current (IO+) = 1 mA			60	Ω

Filter Control Characteristics

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
VR	Reference Voltage Output		2.0		2.40	V
I_{VR}	Reference Output Source Current				2.0	mA

5

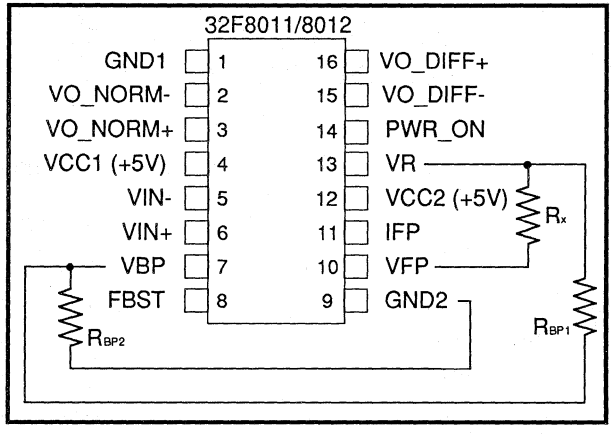


FIGURE 1: 32F8011/8012 Applications Setup, 16-Pin SO or DIP

VR = 2.2V

VFP = 0.667 VR

IVfp = 0.33VR/Rx

IVfp range: 0.31 mA to 0.8 mA
(5 MHz to 13 MHz for SSI 32F8011)
(6 MHz to 15 MHz for SSI 32F8012)

VFP is used when programming current is set with a resistor from VR. When VFP is used IFP must be left open.

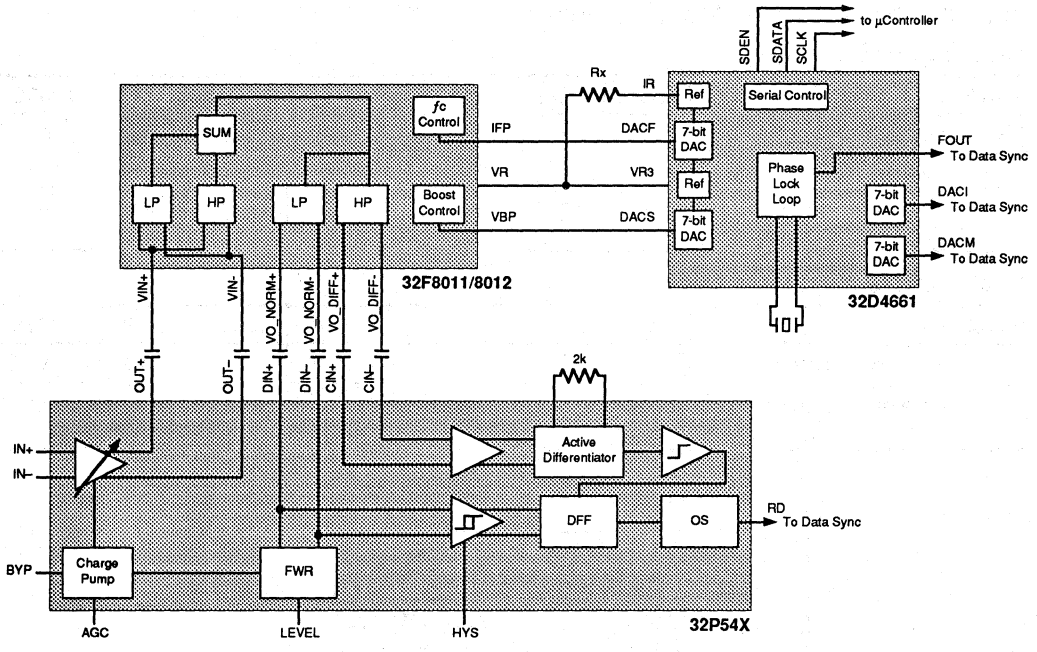


FIGURE 2: Applications Setup, Constant Density Recording
32F8011/8012, 32P54X, 32D4661

IOF = DACF output current

IOF = (0.98F•VR)/127Rx

Rx = (0.98F•VR)/127IOF

Rx = current reference setting resistor

VR = Voltage Reference = 2.2V

F = DAC setting: 0-127

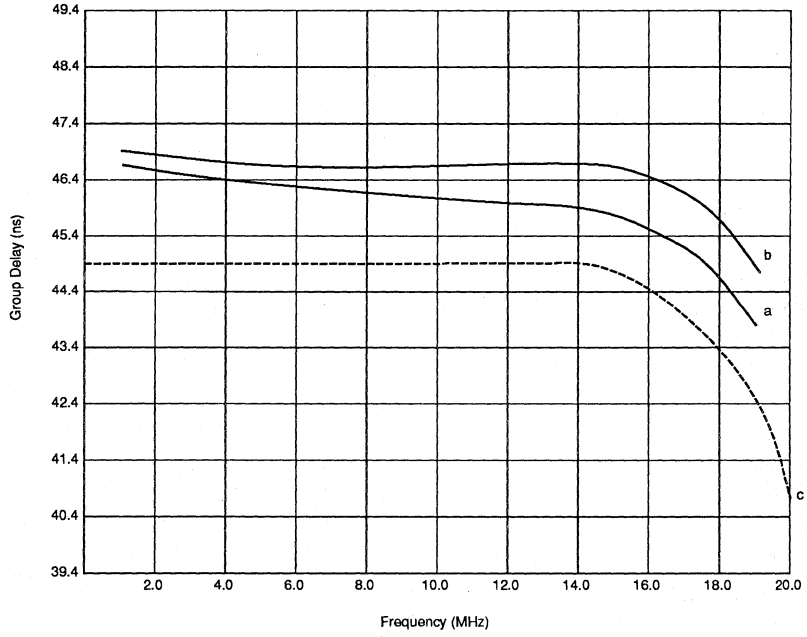
Full scale, F = 127

For range of Max f_c then IFP = 0.8 mA

Therefore, for Max programming current range to 0.8 mA:

Rx = (0.98)(2.2/0.8) = 2.7 kΩ

Please note that in setups such as this where IFP is used for cutoff frequency programming VFP must be left open.



fc = 10.4 MHz

a) No Boost
b) Max Boost
c) Ideal Bessel Filter

FIGURE 3: 32F8011/8012 Typical Group Delay Variation (Differentiated Output)

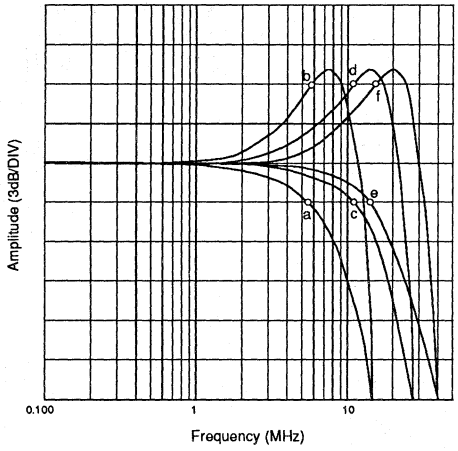


FIGURE 4: 32F8011/8012 Normal Low Pass Output Response (VO_NORM)

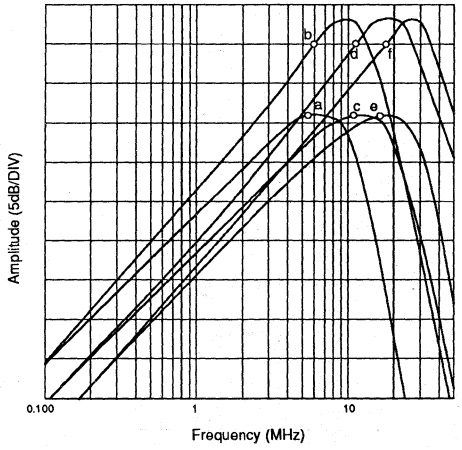
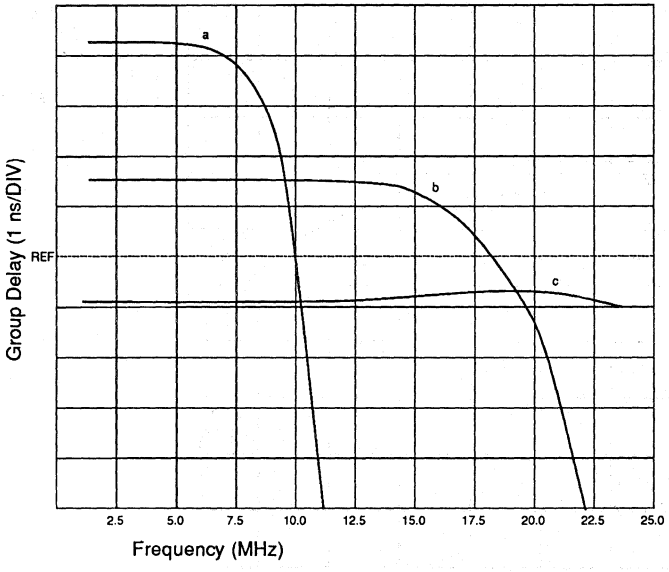


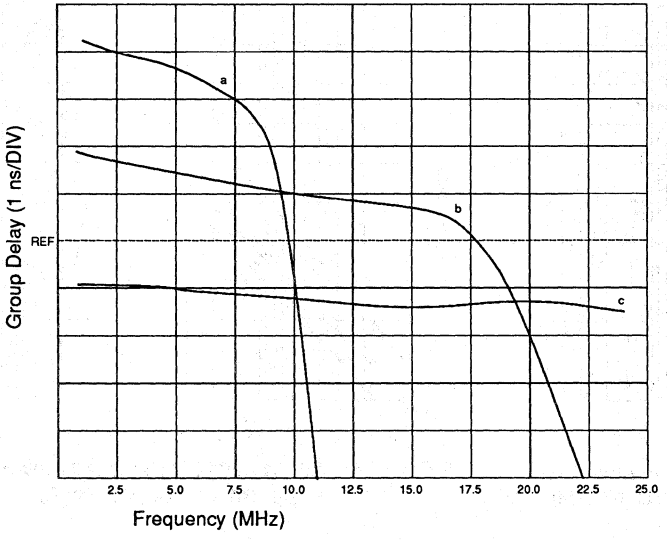
FIGURE 5: 32F8011/8012 Differented Low Pass Output Response (VO_DIFF)

a) fc = 5 MHz No Boost
b) fc = 5 MHz Max Boost
c) fc = 10 MHz No Boost
d) fc = 10 MHz Max Boost
e) fc = 15 MHz No Boost
f) fc = 15 MHz Max Boost



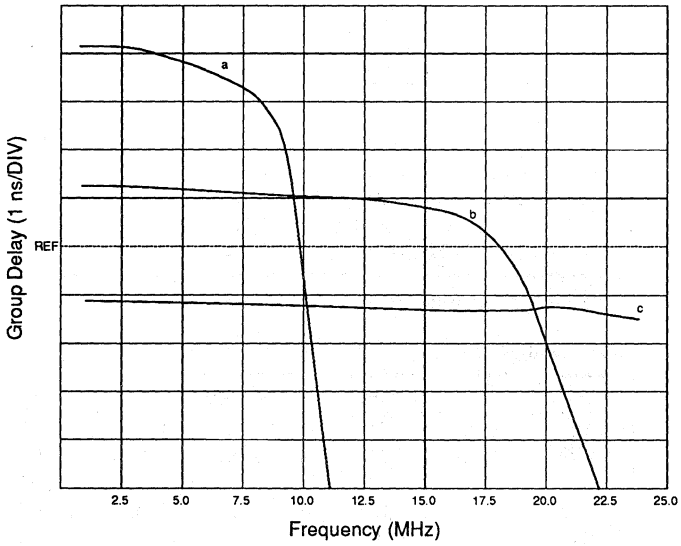
a) fc = 5 MHz (Ref = 80 ns)
b) fc = 10 MHz (Ref = 45 ns)
c) fc = 15 MHz (Ref = 35 ns)

FIGURE 6: 32F8011/8012 Typical Group Delay Variation (Differentiated Output) Maximum Boost



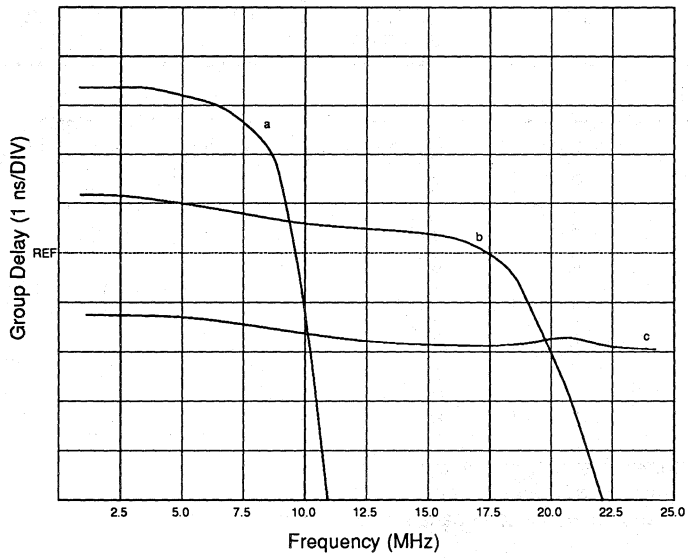
a) fc = 5 MHz (Ref = 80 ns)
b) fc = 10 MHz (Ref = 45 ns)
c) fc = 15 MHz (Ref = 35 ns)

FIGURE 7: 32F8011/8012 Typical Group Delay Variation (Differentiated Output) No Boost



a) fc = 5 MHz (Ref = 80 ns)
b) fc = 10 MHz (Ref = 45 ns)
c) fc = 15 MHz (Ref = 35 ns)

FIGURE 8: 32F8011/8012 Typical Group Delay Variation (Normal Low Pass Output) Maximum Boost



a) fc = 5 MHz (Ref = 80 ns)
b) fc = 10 MHz (Ref = 45 ns)
c) fc = 15 MHz (Ref = 35 ns)

FIGURE 9: 32F8011/8012 Typical Group Delay Variation (Normal Low Pass Output) No Boost

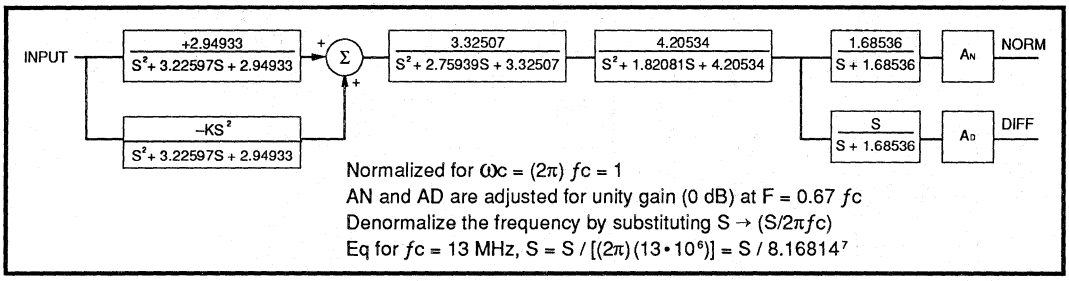


FIGURE 12: 32F8011/8012 Normalized Block Diagram

TABLE 1: 32F8011/8012 Frequency Boost Calculations

Assuming 9.2 dB boost for VBP = VR

$$\frac{VBP}{VR} \cong \frac{\left(10^{(FB/20)}\right)-1}{1.884}$$

Boost	K	VBP/VR	Boost	K	VBP/VR
1 dB	0.36	0.065	6 dB	2.94	0.528
2 dB	0.76	0.137	7 dB	3.65	0.658
3 dB	1.22	0.219	8 dB	4.46	0.802
4 dB	1.73	0.310	9 dB	5.36	0.965
5 dB	2.30	0.413			

or,

$$\text{boost in dB} \cong 20 \log\left[1.884\left(\frac{VBP}{VR}\right)+1\right]$$

VBP/VR	Boost	VBP/VR	Boost
0.1	1.499 dB	0.6	6.569 dB
0.2	2.777 dB	0.7	7.305 dB
0.3	3.891 dB	0.8	7.984 dB
0.4	4.879 dB	0.9	8.613 dB
0.5	5.765 dB	1.0	9.200 dB

TABLE 2: Calculations

Typical change in *f*-3 dB point with boost

Boost (dB)	Gain @ *fc* (dB)	Gain @ peak (dB)	fpeak/*fc*	f-3dB/*fc*
0	-3	0.00	no peak	1.00
1	-2	0.00	no peak	1.20
2	-1	0.00	no peak	1.47
3	0	0.15	0.62	1.74
4	1	1.00	1.08	1.96
5	2	2.12	1.24	2.13
6	3	3.35	1.24	2.28
7	4	4.56	1.39	2.42
8	5	5.82	1.39	2.54
9	6	7.04	1.39	2.66

Notes: 1. *fc* is the original programmed cutoff frequency with no boost
2. *f*-3 dB is the new -3 dB value with boost implemented
3. fpeak is the frequency where the magnitude peaks with boost implemented

i.e., *fc* = 13 MHz when boost = 0 dB
if boost is programmed to 5 dB then f-3 dB = 27.69 MHz, fpeak = 16.12 MHz

TABLE 3: Typical Change in f - 3 dB Point with Boost - $K = 2.94933\,(10^{\frac{BOOST\,(dB)}{20}} - 1)$

Boost (dB)	Gain@fc (dB)	Gain@peak (dB)	fPeak/fc	f-3dB/fc	K
0	-3	0.00	no peak	1.00	0
1	-2	0.00	no peak	1.20	0.36
2	-1	0.00	no peak	1.47	0.76
3	0	0.15	0.62	1.74	1.22
4	1	1.00	1.08	1.96	1.73
5	2	2.12	1.24	2.13	2.30
6	3	3.35	1.24	2.28	2.94
7	4	4.56	1.39	2.42	3.65
8	5	5.82	1.39	2.54	4.46
9	6	7.04	1.39	2.66	5.36
10	7	8.24	1.39	2.77	6.38

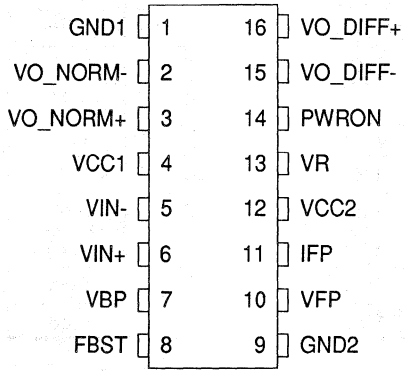
Notes: 1. fc is the original programmed cutoff frequency with no boost.
2. f - 3 dB is the new -3 dB value with boost implemented.
3. $f$peak is the frequency where the magnitude peaks with boost implemented.

e.g., fc = 13 MHz when boost = 0 dB
if boost is programmed to 5 dB then f - 3 dB = 27.69 MHz
$f$peak = 16.12 MHz

SSI 32F8011/8012
Programmable
Electronic Filter

PIN DIAGRAM

(Top View)



16-lead SON, SOL

Thermal Characteristics: θjA

16-lead SON (150 mil)	105° C/W
16-lead SOL (300 mil)	100° C/W

CAUTION: Use handling procedures necessary for a static sensitive component.

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32F8011		
16-lead SON (150 mil)	32F8011-CN	32F8011-CN
16-lead SOL (300 mil)	32F8011-CL	32F8011-CL
SSI 32F8012		
16-lead SON (150 mil)	32F8012-CN	32F8012-CN
16-lead SOL (300 mil)	32F8012-CL	32F8012-CL

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914

SSI 32F8020A/8022A/8021/8023
Low-Power Programmable Electronic Filter

December 1993

DESCRIPTION

The SSI 32F8020A/8022A Programmable Electronic Filter provides an electronically controlled low–pass filter with a separate differentiated low–pass output. A seven–pole, 0.05° Equiripple-type linear phase, low–pass filter is provided along with a single-pole, single-zero differentiator. Both outputs have matched delays. The delay matching is unaffected by any amount of programmed equalization or bandwidth. The SSI 32F8021/8023 does not have differentiated outputs. This programability combined with low group delay variation makes the SSI 32F8020A/8022A/8021/8023 ideal for use in constant density recording applications. Double differentiation pulse slimming equalization is accomplished by a two–pole, low–pass with a two–pole, high–pass feed forward section to provide complimentary real axis zeros. A variable attenuator is used to program the zero locations.

The SSI 32F8020A/8022A programmable equalization and bandwidth characteristics can be controlled by external DACs or DACs provided in the SSI 32D4661

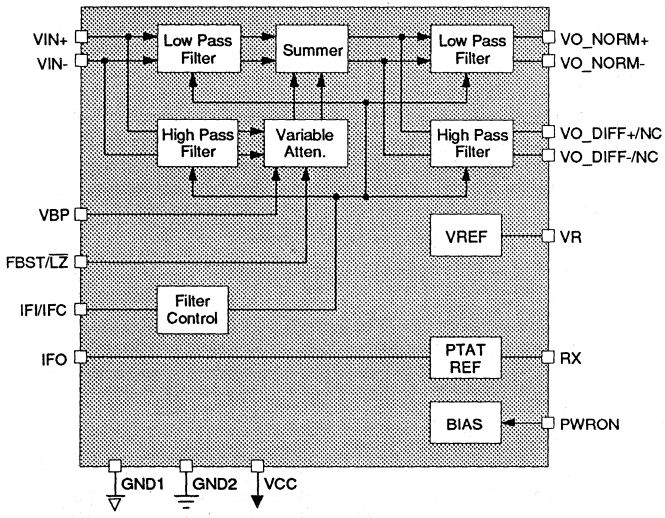
(continued)

FEATURES

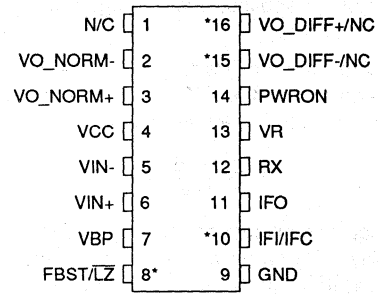
- **Ideal for constant density recording applications**
- **Programmable filter cutoff frequency (fc = 1.5 to 8 MHz)**
- **Programmable pulse slimming equalization (0 to 9 dB boost at the filter cutoff frequency)**
- **Matched normal and differentiated low-pass outputs (SSI 32F8020A/8022A)**
- **Differential filter input and outputs**
- **±10% cutoff frequency accuracy**
- **±2% maximum group delay variation from 1.5 - 8 MHz**
- **Total harmonic distortion less than 1%**
- **No external filter components required**
- **+5V only operation**
- **16-pin SON and SOL package**

5

BLOCK DIAGRAM



PIN DIAGRAM



* Pin 8 = FBST - SSI 32F8020A/8021
LZ - SSI 32F8022A/8023

* Pin 10 = IFI - SSI 32F8020A/8022A
IFC - SSI 32F8021/8023

* Pin 15 & 16 = VO_DIFF - SSI 32F8020A/8022A
N/C - SSI 32F8021/8023

DESCRIPTION (continued)

SSI 32D4661 time base generator. Fixed characteristics are easily accomplished with three external resistors. External DACs are required for the SSI 32F8021/8023 to program the cutoff frequency. For the SSI 32F8020A/8021, equalization can be switched in or out by a logic signal. The input impedance of the SSI 32F8022A/8023 can be clamped low for fast recovery from input overload.

The SSI 32F8020A/8022A/8021/8023 require only a +5V supply and are available in 16-Lead SON and SOL packages.

FUNCTIONAL DESCRIPTION

The SSI 32F8020A/8022A/8021/8023 is a high performance programmable electronic filter. It features a 7-pole 0.05° phase equiripple filter with matched normal and differentiated outputs. The device has been optimized for usage with several Silicon Systems products, including the SSI 32D4661 Time Base Generator, the SSI 32P54X family pulse detectors, and the SSI 32P4720 combo chip (Data Separator and Pulse Detector).

CUTOFF FREQUENCY PROGRAMMING

The cutoff frequency, fc, of the SSI 32F8020A/8022A is defined as the -3dB filter bandwidth with no magnitude equalization applied, and is programmable from 1.5 MHz to 8 MHz.

The cutoff frequency is programmable with 3 pins: RX, IFO and IFI. At the RX pin, an external resistor to ground establishes a reference current:

$$IFO = \frac{0.75}{RX} \text{ at } T = 27°C$$

IFI should be made proportional to IFO for temperature stability. The cutoff frequency is related to the RX resistor, IFO and IFI currents as follows:

$$fc(MHz) = 8x\frac{IFI}{IFO}x\frac{1.25}{Rx(k\Omega)}$$

For a fixed cutoff frequency setting, IFO and IFI can be tied together. The cutoff frequency equation then reduces to:

$$fc(MHz) = 8x\frac{1.25}{Rx(k\Omega)}$$

For programmable cutoff frequency, an external current DAC can be used. The IFO should be the reference current into the DAC. The DAC output current drives IFI, which is then proportional to IFO. The DACF in the SSI 32D4661 Time Base Generator is designed to control fc of the Silicon Systems programmable filters. When the DACF, which has a 4X current from its reference to full scale output is used, a 5-kΩ RX is used. The fc is then given as follows:

$$fc(MHz) = 8x\frac{F\_Code}{127}$$

where F_Code is the decimal code equivalent to the 7-bit digital input for the DACF. The cutoff frequency programming for the SSI 32F8021/8023 is shown in Figure 3.

MAGNITUDE EQUALIZATION PROGRAMMING

The magnitude equalization, measured in dB, is the amount of high frequency peaking at the cutoff frequency relative to the original -3 dB point. For example, when 9 dB boost is applied, the magnitude response peaks up 6 dB above the DC gain.

The magnitude equalization is programmable with two pins: VR and VBP. The VR is a bandgap reference voltage, 2.3V typically. The voltage at the VBP pin determines the amount of high frequency boost. The boost function is as follows:

$$Boost(dB) = 20\log_{10}[1.884(\frac{VBP}{VR}) + 1]$$

For a fixed boost setting, a resistor divider between VR to ground can be used with the divided voltage at the VBP pin. For programmable equalization, an external voltage DAC can be used. VR should be the reference voltage to the DAC. The DAC output voltage is then proportional to VR. The DACS in the SSI 32D4661 is designed to control the magnitude equalization of Silicon Systems programmable filters. When DACS is used, the boost relation then reduces to:

$$Boost(dB) = 20\log_{10}[1.884(\frac{S\_Code}{127}) + 1]$$

where S_Code is the decimal code equivalent to the 7-bit digital input for the DACS.

For the SSI 32F8020A/8021, the equalization function can be disabled when FBST is pulled to logic 0. For the SSI 32F8022A/8023, the VBP pin should be grounded to achieve 0 dB boost.

LOW INPUT IMPEDANCE (SSI 32F8022A/8023 only)

When the LZ is at logic 1 or left open, the SSI 32F8022A/8023 input is at high impedance state. When the LZ is pulled to logic 0, the SSI 32F8022A/8023 input is clamped to a low impedance state, 200 Ω typical.

POWER ON/OFF

The SSI 32F8020A/8022A/8021/8023 support a power down mode for minimal Idle mode power dissipation. When PWRON is pulled up to logic 1, the device is in normal operation mode. When PWRON is pulled down to logic 0, or left open, the device is in the power down mode.

PIN DESCRIPTION

NAME	DESCRIPTION
VIN+, VIN-	DIFFERENTIAL SIGNAL INPUTS.
VO_NORM+, VO_NORM-	DIFFERENTIAL NORMAL OUTPUTS.
VO_DIFF+ VO_DIFF-	DIFFERENTIAL DIFFERENTIATED OUTPUTS.
RX	PTAT REFERENCE CURRENT SET. PTAT (proportional to absolute temperature) reference current IFO is equivalent to the current set on this pin.
IFO	PTAT CURRENT REFERENCE OUTPUT. This pin ouputs a PTAT reference current which is externally scaled for control input into IFI.
IFI	FREQUENCY PROGRAM INPUT. The filter cutoff frequency fc, is set by an external current IFI, injected into this pin. IFI must be proportional to current IFO. This current can be set with an external current generator such as a DAC, referenced to IFO.
VBP	FREQUENCY BOOST PROGRAM INPUT. The slimmer high frequency boost is set by an external voltage applied to this pin. VBP must be proportional to voltage VR. A fixed amount of boost can be set by an external resistor divider network connected from VBP to VR and GND. No boost is applied if the FBST pin is grounded, or at logic low.
FBST (32F8020A/8021)	FREQUENCY BOOST. A high logic level or open input enables the frequency boost circuitry. No boost is applied if the FBST pin is grounded, or at logic low.
$\overline{LZ}$ (32F8022A /8023)	LOW IMPEDANCE MODE. With a low logic level, the analog input impedance is switched low for fast recovery from input overload. With a high logic level or left open, the input is at high impedance state.
PWRON	POWER ON. A high logic level circuit enables the chip. A low level puts the chip in a low power state. A low or open circuit disables the chip.
VR	REFERENCE VOLTAGE. Internally generated reference voltage.
VCC	+5 VOLT SUPPLY.
GND	GROUND

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may damage the device.

PARAMETER	RATING
Storage Temperature	-65 to +150°C
Junction Operating Temperature, Tj	+130°C
Supply Voltage, VCC	-0.5 to 7V
Voltage Applied to Inputs	-0.5 to VCCV

RECOMMENDED OPERATING CONDITIONS

Supply voltage, VCC	4.50V < VCC < 5.50V
Ambient Temperature	0°C < Ta < 70°C

Power Supply Characteristics

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
ICC	Power Supply Current	PWRON ≤ 0.8V			0.5	mA
		PWRON ≥ 2.2V SSI 32F8021/8023		26	32	mA
		PWRON ≥ 2.2V SSI 32F8020A/8022A		35	41	mA
PD	Power Dissipation	PWRON ≤ 0.8V			3	mW
		PWRON ≥ 2.2V, VCC = 5V SSI 32F8021/8023		130	160	mW
		PWRON ≥ 2.2V, VCC = 5.5V SSI 32F8021/8023		143	176	mW
		PWRON ≥ 2.2V, VCC = 5V SSI 32F8020A/8022A		175	205	mW
		PWRON ≥ 2.2V, VCC = 5.5V SSI 32F8020A/8022A		193	226	mW

DC Characteristics

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
VIH	High Level Input Voltage	TTL input	2.0			V
VIL	Low Level Input Voltage				0.8	V
IIH	High Level Input Current	VIH = 2.7V			20	µA
IIL	Low Level Input Current	VIL = 0.4V	-1.5			mA
VICM	VIN± Input Common Mode Voltage		(V_{CC} -1.5) -0.3		(V_{CC} -1.5) +0.3	V
VOCM	VO_NORM± Output Common Mode Voltage		VCC-2.3 -0.5		VCC-2.3 +0.5	V
VOFF	VO_NORM± Output Offset	VIN± open	-0.4		+0.4	V

Filter Characteristics

fc	Filter Cutoff Frequency	Rx = 5kΩ $fc\ (MHz) = 8 \cdot \frac{IFI}{4 \cdot IFO}$ (32F8020A/8022A) $fc\ (MHz) = 8 \cdot \frac{IFC}{4 \cdot IFO}$ (32F8021/8023)	1.5		8.0	MHz
FCA	Filter fc Accuracy	fc (nominal) = 8 MHz	–10		+10	%
AO	VO_NORM Diff Gain	F = 0.67 fc, FB = 0 dB	0.8	1.0	1.2	V/V
AD	VO_DIFF Diff Gain (32F8020A/8022A)	F = 0.67 fc, FB = 0 dB	0.8AO		1.2AO	V/V
FB	Frequency Boost at fc	$FB(db)=20 \log \left[1.884\left(\frac{VBP}{VR}\right)+1\right]$ VBP = VR		9.2		dB
FBA	Frequency Boost Accuracy	FB (ideal) = 9.2 dB	–1		+1	dB
TGD0	Group Delay Variation Without Boost	fc = 8 MHz, VBP = 0V F = 0.2 fc to 1.75 fc	–1.3		+1.3	ns
		fc = 1.5 MHz - 8 MHz F = 0.2 fc to 1.75 fc, VBP = 0V	–2		+2	%
TGDB	Group Delay Variation With Boost	fc = 8 MHz, VBP = VR F = 0.2 fc to 1.75 fc	–1.3		+1.3	ns
		fc = 1.5 MHz - 8 MHz F = 0.2 fc to 1.75 fc, VBP = VR	–2		+2	%

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ELECTRICAL SPECIFICATIONS (continued)

Filter Characteristics (continued)

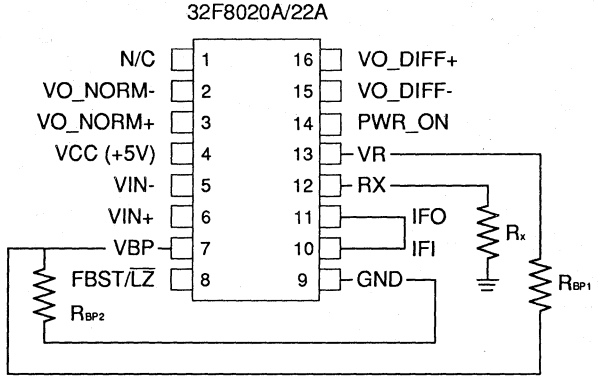
PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VOF Filter Output Dynamic Range	THD = 1% max, F = 0.67 *fc*	1.0			Vpp
VOF Filter Output Dynamic Range	THD = 1.5%, F = 0.67 *fc* VO_DIFF±, *fc* =1.5 MHz, 0 < Ta < 10°C, THD = 2%, F = 0.67 *fc*	1.5			Vpp
RIN Filter Diff Input Resistance	32F8020A/8021 32F8022A/8023 LZ = 1 or open	3.0	4.0		kΩ
	32F8022A/8023 LZ = 0		200	400	Ω
CIN Filter Input Capacitance				7	pF
EOUT Output Noise Voltage Differentiated Output	BW = 100 MHz, Rs = 50Ω *fc* = 8 MHz, VBP = 0.0V (32F8020A/8022A)		6.3	7.5	mVRms
EOUT Output Noise Voltage Normal Output	BW = 100 MHz, Rs = 50Ω *fc* = 8 MHz, VBP = 0.0V		2.7	4.0	mVRms
EOUT Output Noise Voltage Differentiated Output	BW = 100 MHz, Rs = 50Ω *fc* = 8 MHz, VBP = VR (32F8020A/8020A)		9.4	11.0	mVRms
EOUT Output Noise Voltage Normal Output	BW = 100 MHz, Rs = 50Ω *fc* = 8 MHz, VBP = VR		3.7	4.5	mVRms
IO– Filter Output Sink Current		1.0			mA
IO+ Filter Output Source Current		2.0			mA
RO Filter Output Resistance (Single ended)	IO+ = 1.0 mA			60	Ω

Filter Control Characteristics

VR	Reference Voltage		2.2		2.45	V
VBP	Frequency Boost Control Voltage Range	VR = 2.3V FBOOST = 0 to 9.2 dB	0		2.3	V
VRX	PTAT Reference Current Set Output Voltage	TA = 25°C IRX = 0 - 0.6 mA Rx > 1.25 kΩ		750		mV
IFO	PTAT Reference Current, Output Current Range	TA = 25°C 1.25 kΩ < Rx < 6.8 kΩ IFO = VRX/Rx VRX = 750 mV	0.11		0.6	mA
RIFO	IFO Output Impedance		50			kΩ
VIFO	IFO Voltage Compliance		0		Vcc -1	V

Filter Control Characteristics

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
IFI	PTAT Programming Current Range	TA = 25°C, VRX = 750 mV 32F8020A/8022A	0.11		0.6	mA
RIFI	IFI Input Impedance	32F8020A/8022A	1.0		2.5	kΩ
VIFI	IFI Voltage Compliance	32F8020A/8022A	0.5		2.5	V
IFC	PTAT Programming Current Range	TA = 25 °C, VRX = 750 mV 32F8021/8023	0.11		0.6	mA
TPWR	Power On Recovery Time	DC voltages within 20 mV of final values			500	ns
TBST	Boost Change Recovery	DC voltages within 20 mV of final values			500	ns
TFBW	Bandwidth Change Recovery	DC voltages within 20 mV of final values			500	ns



VR = 2.3V

VRX = 750 mV @25°C

IFO = V_{RX}/R_X

IFI range: 0.11 mA to 0.60 mA @25°C

(1.5 to 8 MHz NO BOOST)

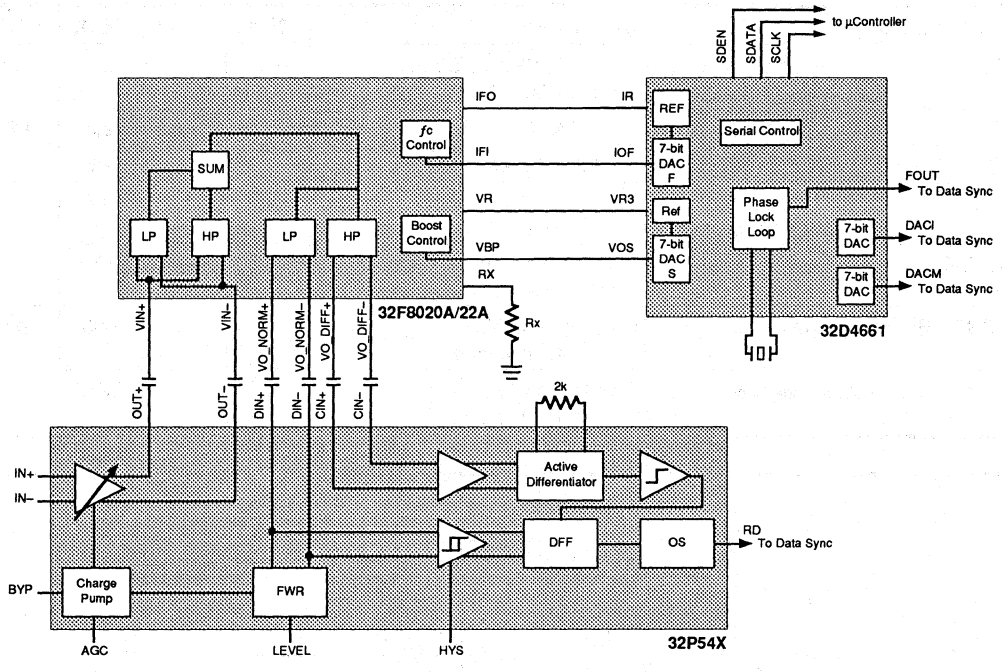
Fixed frequency programming is accomplished as shown in the drawing above. In this case IFI (programming current) is equivalent to IFO (reference current). Programming current is then set by V_{RX}/R_X.

where: fc = 8.0 MHz then

IFI = IFO = 0.60 mA @25 °C

Rx = 750 mV/0.60 mA = 1.25 kΩ

FIGURE 1: 32F8020A/8022A Applications Setup



VR = 2.3V

VRX = 750 mV @25°C

IFO = VRX/Rx

IFI range: 0.11 mA to 0.60 mA @25°C

(1.5 to 8 MHz NO BOOST)

In this case the IFI (programming current) is scaled from IFO (reference current) through DACF on the 32D4661. DACF has a current gain of 4; therefore, the reference current should be set to 25% of the maximum desired IFI (programming current).

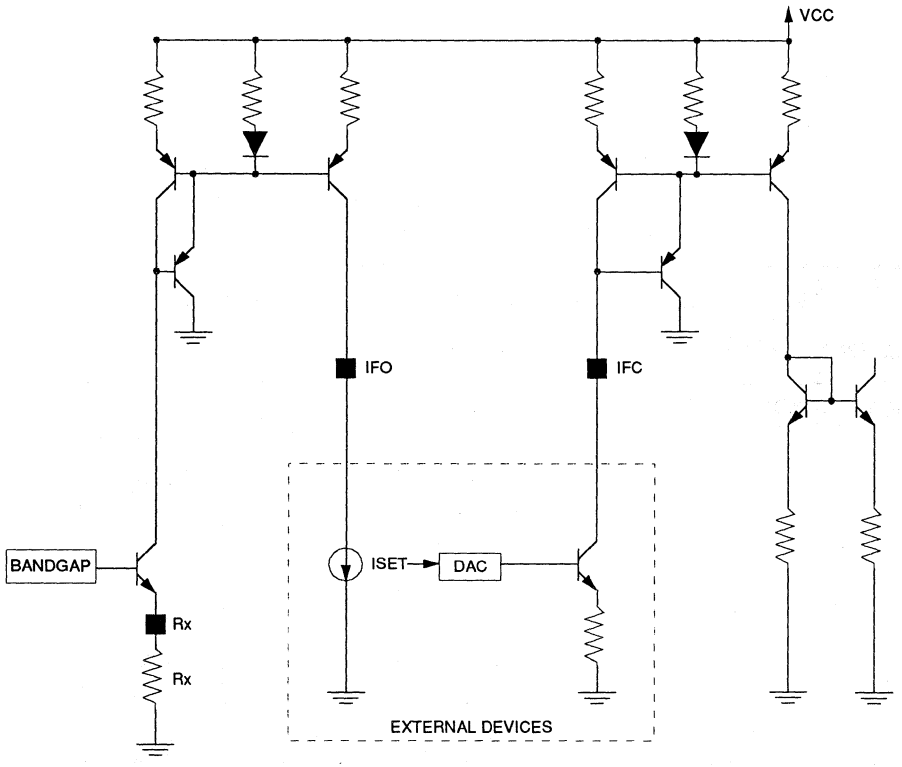
where: fc (max) = 8.0 MHZ then

IFI (max) = 0.60 mA @25°C

IFO (max) = 0.15 mA

therefore Rx = 750 mV/0.15 mA = 5 kΩ

FIGURE 2: Applications Setup, Constant Density Recording 32F8020A/8022A, 32P54X, 32D4661



VRX = 750 mV @25°C

IRX = IFO

IFC programming range: 0.11 mA to 0.60 mA @25°C
(1.5 to 8.0 MHz: No Boost)

The IFC (programming current) is scaled from IFO (reference current) by the set-up shown above. Assuming the DAC current gain = 4.0, then programming is accomplished as follows:

MAX programming current required: IFC = 0.6 mA (fc = 8.0 MHz) @25°C

IFO = IFC/8 = 0.075 mA (MAX) @25°C

IRX = IFO

IRX = 750mV/Rx @25°C

Rx = 5 kΩ

FIGURE 3: 32F8021/8023 Frequency Programming

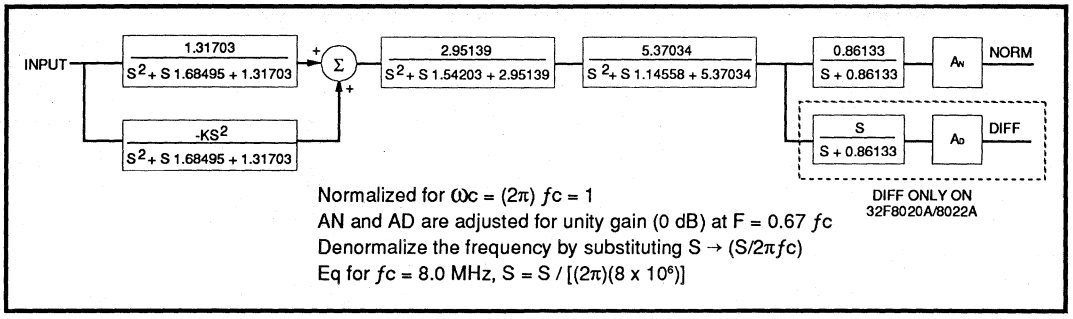


FIGURE 4: 32F8020A/8022A/8021/8023 Normalized Block Diagram

TABLE 1: 32F8020A/8022A Frequency Boost Calculations. $K = 1.31703\,(10^{\frac{BOOST\ (dB)}{20}} - 1)$

Assuming 9.2 dB boost for **VBP = VR**

$$\frac{VBP}{VR} \cong \frac{\left(10^{(FB/20)}\right) - 1}{1.884}$$

Boost	VBP/VR	K
1 dB	0.065	0.16
2 dB	0.137	0.34
3 dB	0.219	0.54
4 dB	0.310	0.77
5 dB	0.413	1.03
6 dB	0.528	1.31
7 dB	0.658	1.63
8 dB	0.802	1.99
9 dB	0.965	2.40

or,

$$\text{boost in dB} \cong 20 \log \left[1.884 \left(\frac{VBP}{VR} \right) + 1 \right]$$

VBP/VR	Boost
0.1	1.499 dB
0.2	2.777 dB
0.3	3.891 dB
0.4	4.879 dB
0.5	5.765 dB
0.6	6.569 dB
0.7	7.305 dB
0.8	7.984 dB
0.9	8.613 dB
1.0	9.200 dB

TABLE 2: Calculations
Typical change in f-3 dB point and frequency peak with boost.

Boost (dB)	Gain@fc (dB)	Gain@peak (dB)	$f$peak/fc	f-3 dB/fc
0	-3	0.00	no peak	1.00
1	-2	0.00	no peak	1.21
2	-1	0.00	no peak	1.51
3	0	0.15	0.70	1.80
4	1	0.99	1.05	2.04
5	2	2.15	1.23	2.20
6	3	3.41	1.33	2.33
7	4	4.68	1.38	2.43
8	5	5.94	1.43	2.51
9	6	7.18	1.46	2.59

NOTES: 1. fc is the original programmed cutoff frequency with no boost.

2. f-3 dB is the new -3 dB value with boost implemented.

3. $f$peak is the frequency where the magnitude peaks when boost is implemented.

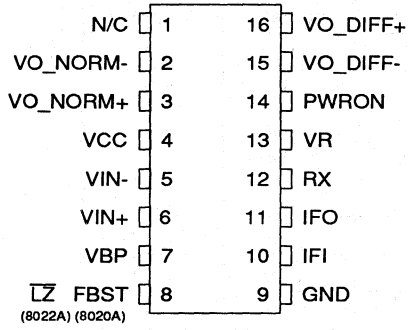
i.e., fc = 8 MHz when boost = 0 dB if boost is programmed to 5 dB then

f-3 dB = 17.6 MHz

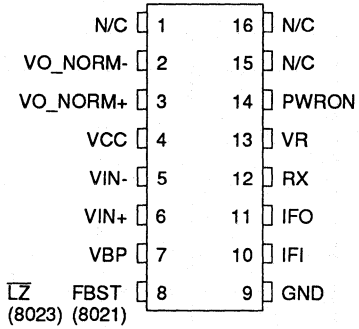
$f$peak = 9.84 MHz

SSI 32F8020A/8022A/8021/8023
Low-Power Programmable Electronic Filter

PACKAGE PIN DESIGNATIONS
(Top View)



32F8020A/8022A
16-Lead SON, SOL



32F8021/8023
16-Lead SON, SOL

THERMAL CHARACTERISTICS: θja

16-Lead SON, SOL (150 mil)	105° C/W

CAUTION: Use handling procedures necessary for a static sensitive component.

ORDERING INFORMATION

PART DESCRIPTION		ORDER NUMBER	PACKAGE MARK
SSI 32F8020A	16-Lead SON	32F8020A-CN	32F8020A-CN
	16-Lead SOL	32F8020A-CL	32F8020A-CL
SSI 32F8022A	16-Lead SON	32F8022A-CN	32F8022A-CN
	16-Lead SOL	32F8022A-CL	32F8022A-CL
SSI 32F8021	16-Lead SON	32F8021-CN	32F8021-CN
	16-Lead SOL	32F8021-CL	32F8021-CL
SSI 32F8023	16-Lead SON	32F8023-CN	32F8023-CN
	16-Lead SOL	32F8023-CL	32F8023-CL

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914

silicon systems®
A TDK Group Company

SSI 32F8030
Programmable Electronic Filter

December 1993

DESCRIPTION

The SSI 32F8030 Programmable Electronic Filter provides an electronically controlled low–pass filter with a separate differentiated low–pass output. A seven–pole, 0.05° Equiripple-type linear phase, low–pass filter is provided along with a single-pole, single-zero differentiator. Both outputs have matched delays. The delay matching is unaffected by any amount of programmed high frequency peaking (boost) or bandwidth. This programability, combined with low group delay variation makes the SSI 32F8030 ideal for use in many applications. Double differentiation high frequency boost is accomplished by a two–pole, low–pass with a two–pole, high–pass feed forward section to provide complementary real axis zeros. A variable attenuator is used to program the zero locations, which controls the amount of boost.

The SSI 32F8030 programmable boost and bandwidth characteristics can be controlled by external DACs or DACs provided in the SSI 32D4661 Time Base Generator. Fixed characteristics are easily accomplished with three external resistors. In addition, boost can be switched in or out by a logic signal.

The SSI 32F8030 requires only a +5V supply and is available in 16-Lead SON, and SOL packages.

FEATURES

- **Ideal for:**
  - **constant density recording applications**
  - **magnetic tape recording**
- **Programmable filter cutoff frequency (fc = 250 kHz to 2.5 MHz)**
- **Programmable high frequency peaking (0 to 9 dB boost at the filter cutoff frequency)**
- **Matched normal and differentiated low-pass outputs**
- **Differential filter input and outputs**
- **±3.0% group delay variation from 0.2 fc to 1.75 fc, 0.25 MHz ≤ fc ≤ 2.5 MHz**
- **Total harmonic distortion less than 1%**
- **+5V only operation**
- **16-Lead SON, and SOL packages**
- **5 mW idle mode**

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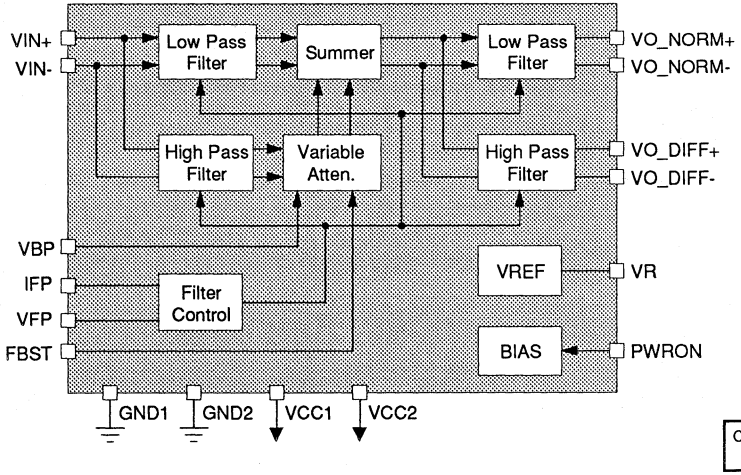
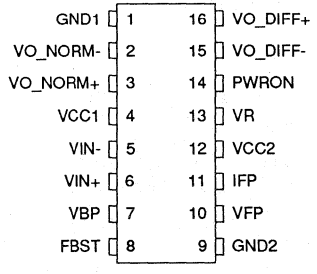
BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

FUNCTIONAL DESCRIPTION

The SSI 32F8030, a high performance programmable electronic filter, provides a low pass 0.05° Equiripple-type linear phase seven pole filter with matched normal and differentiated outputs. The device has been optimized for usage with several Silicon Systems products, including the SSI 32D4661 Time Base Generator, the SSI 32P54x family of Pulse Detectors, and the SSI 32P4720 Combo device (Data Separator and Pulse Detector).

CUTOFF FREQUENCY PROGRAMMING

The SSI 32F8030 programmable electronic filter can be set to a filter cutoff frequency from 250 kHz to 2.5 MHz (with no boost).

Cutoff frequency programming can be established using either a current source fed into the IFP pin, whose output current is proportional to the SSI 32F8030 output reference voltage VR, or by means of an external resistor tied from the output voltage reference pin VR to pin VFP. The former method is optimized using the SSI 32D4661 Time Base Generator, since the current source into pin IFP is available at the DAC F output of the 32D4661. Furthermore, the voltage reference input is supplied to pin VR3 of the 32D4661 by the reference voltage VR from the VR pin of the 32F8030. This reference voltage is an internally generated bandgap reference, which typically varies less than 1 % over voltage supply and temperature variation. (For the calculations below IVFP = current into IFP or VFP pins).

The cutoff frequency, determined by the -3dB point relative to a very low frequency value (< 10kHz), is related to the current IVFP injected into pin IFP by the formula

Fc (ideal, in MHz) = 3.125•IFP = 3.125•IVFP•2.2/VR, where IFP and IVFP are in mA, 0.08<IFP<0.8 mA, and VR is in volts.

If a current source is used to inject current into pin IFP, pin VFP should be left open.

If the 32F8030 cutoff frequency is set using voltage VR to bias up a resistor tied to pin VFP, the cutoff frequency is related to the resistor value by the formula

Fc (ideal, in MHz) = 3.125•IFP = 3.125•2.2/(3•Rx) where Rx is in kΩ, & 0.917 kΩ <Rx<9.17 kΩ.

If pin VFP is used to program cutoff frequency, pin IFP should be left open.

SLIMMER HIGH FREQUENCY BOOST PROGRAMMING

The amplitude of the output signal at frequencies near the cutoff frequency can be increased using this feature. Applying an external voltage to pin VBP which is proportional to reference output voltage VR (provided by the VR pin) will set the amount of boost. A fixed amount of boost can be set by an external resistor divider network connected from pin VBP to pins VR and GND. No boost is applied if pin FBST, frequency boost enable, is at a low logic level.

The amount of boost FB at the cutoff frequency Fc is related to the voltage VBP by the formula

FB (ideal, in dB) = $20 \log_{10}[1.884(VBP/VR)+1]$, where 0<VBP<VR.

PIN DESCRIPTION

NAME	DESCRIPTION
VIN+, VIN-	DIFFERENTIAL SIGNAL INPUTS. The input signals must be AC coupled to these pins.
VO_NORM+, VO_NORM-	DIFFERENTIAL NORMAL OUTPUTS. The output signals must be AC coupled.
VO_DIFF+, VO_DIFF-	DIFFERENTIAL DIFFERENTIATED OUTPUTS. For minimum time skew, these outputs should be AC coupled to the pulse detector.
IFP	FREQUENCY PROGRAM INPUT. The filter cutoff frequency FC, is set by an external current IFP, injected into this pin. IFP must be proportional to voltage VR. This current can be set with an external current generator such as a DAC. VFP should be left open when using this pin.
VFP	FREQUENCY PROGRAM INPUT. The filter cutoff frequency can be set by programming a current through a resistor from VR to this pin. IFP should be left open when using this pin.
VBP	FREQUENCY BOOST PROGRAM INPUT. The high frequency boost is set by an external voltage applied to this pin. VBP must be proportional to voltage VR. A fixed amount of boost can be set by an external resistor divider network connected from VBP to VR and GND. No boost is applied if the FBST pin is grounded, or at logic low.
FBST	FREQUENCY BOOST. A high logic level or open input enables the frequency boost circuitry.
PWRON	POWER ON. A high logic level enables the chip. A low level puts the chip in a low power state.
VR	REFERENCE VOLTAGE. Internally generated reference voltage.
VCC1, VCC2	+5 VOLT SUPPLY.
GND1, GND2	GROUND

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ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may damage the device.

PARAMETER	RATING
Storage Temperature	-65 to +150°C
Junction Operating Temperature, Tj	+130°C
Supply Voltage, VCC1, VCC2	-0.5 to 7V
Voltage Applied to Inputs	-0.5 to VCC + 0.5V
IFP, VFP Inputs Maximum Current	≤1.2 mA

RECOMMENDED OPERATING CONDITIONS

PARAMETER	RATING
Supply voltage, VCC1, VCC2	4.5 < VCC1,2 < 5.50V
Ambient Temperature	0 < Ta < 70°C

ELECTRICAL SPECIFICATIONS

Power Supply Characteristics

Unless otherwise specified, recommended operating conditions apply.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
ICC	Power Supply Current	PWRON ≤ 0.8V			0.5	mA
ICC	Power Supply Current	PWRON ≥ 2.0V		28	42	mA
PD	Power Dissipation	PWRON ≥ 2.0V		140	231	mW
PD	Power Dissipation	PWRON ≤ 0.8V			3	mW

DC Characteristics

VIH	High Level Input Voltage	TTL input	2.0		VCC+0.3	V
VIL	Low Level Input Voltage		-0.3		0.8	V
IIH	High Level Input Current	VIH = 2.7V			20	µA
IIL	Low Level Input Current	VIL = 0.4V	–1.5			mA

Filter Characteristics

fc = 1.25 MHz unless otherwise stated

FCA	Filter fc Accuracy	using IFP pin: IFP = 0.4 mA or using VFP pin: Rx = 1.84 kΩ	1.125		1.375	MHz
AO	VO_NORM Diff Gain	F = 0.67 fc, FB = 0 dB	0.8		1.20	V/V
AD	VO_DIFF Diff Gain	F = 0.67 fc, FB = 0 dB	0.9AO		1.1AO	V/V
FBA	Frequency Boost Accuracy	VBP = VR	8.0	9.2	10.4	dB
TGD0	Group Delay Variation Without Boost*	0.25 MHz ≤ fc ≤ 2.5 MHz F = 0.2 fc to 1.75 fc	–3		+3	%
TGDB	Group Delay Variation With Boost*	0.25 MHz ≤ fc ≤ 2.5 MHz VBP = VR, F = 0.2 fc to 1.75 fc	–3		+3	%
VIF	Filter Input Dynamic Range	THD = 1% max, F = 0.67 fc (no boost, 1000 pF capacitor across Rx)	1.0			Vpp
VOF	Filter Normal Output Dynamic Range	THD = 1% max, F = 0.67 fc VBP = 0 (1000 pF capacitor across Rx)	1.0			Vpp
VOF	Filter Normal Output Dynamic Range	THD = 1% max, F = 0.67 fc VBP = VR (1000 pF capacitor across Rx)	1.0			Vpp
VOF	Filter Differentiated Output Dynamic Range	THD = 1% max, F = 0.67 fc VBP = 0 (1000 pF capacitor across Rx)	1.0			Vpp
VOF	Filter Differentiated Output Dynamic Range	THD = 1% max, F = 0.67 fc VBP = VR (1000 pF capacitor across Rx)	1.0			Vpp

Filter Characteristics (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
RIN Filter Diff Input Resistance		3.0	4.0	5.0	kΩ
CIN Filter Diff Input Capacitance*			3.0		pF
EOUT Output Noise Voltage* Differentiated Output	BW = 100 MHz, Rs = 50Ω, Ifp = 0.8 mA, VBP = 0.0V		2.7	3.2	mVRms
EOUT Output Noise Voltage* Normal Output	BW = 100 MHz, Rs = 50Ω Ifp = 0.8 mA, VBP = 0.0V		1.6	2.0	mVRms
EOUT Output Noise Voltage* Differentiated Output	BW = 100 MHz, Rs = 50Ω Ifp = 0.8 mA, VBP = VR		3.1	3.8	mVRms
EOUT Output Noise Voltage* Normal Output	BW = 100 MHz, Rs = 50Ω Ifp = 0.8 mA, VBP = VR		1.8	2.2	mVRms
EOUT Output Noise Voltage* Differentiated Output	BW = 10 MHz, Rs = 50Ω, Ifp = 0.08 mA, VBP = 0.0V		1.8	2.1	mVRms
EOUT Output Noise Voltage* Normal Output	BW = 10 MHz, Rs = 50Ω Ifp = 0.08 mA, VBP = 0.0V		1.0	1.2	mVRms
EOUT Output Noise Voltage* Differentiated Output	BW = 10 MHz, Rs = 50Ω Ifp = 0.08 mA, VBP = VR		2.0	2.5	mVRms
EOUT Output Noise Voltage* Normal Output	BW = 10 MHz, Rs = 50Ω Ifp = 0.08 mA, VBP = VR		1.1	1.5	mVRms
IO- Filter Output Sink Current		1.0			mA
IO+ Filter Output Source Current		2.0			mA
RO Filter Output Resistance**	Sinking 1 mA from pin			70	Ω

* Not directly testable in production, design characteristic.
** Single ended

Filter Control Characteristics

VR Reference Voltage Output		2.0		2.40	V
I_{VR} Reference Output Source Current				2.0	mA

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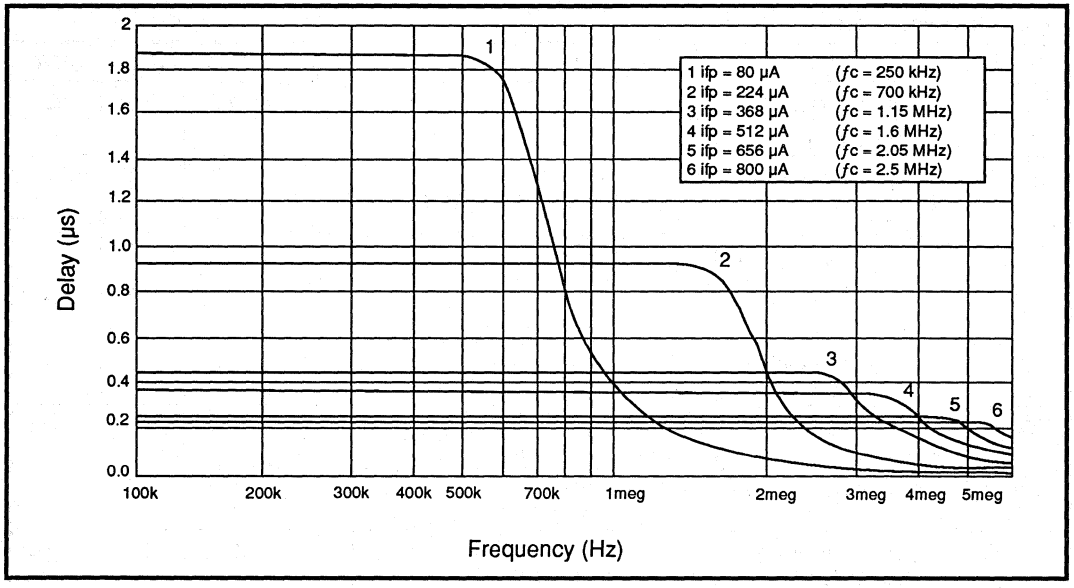


FIGURE 1: Typical Normal/Differentiated Output Group Delay Response

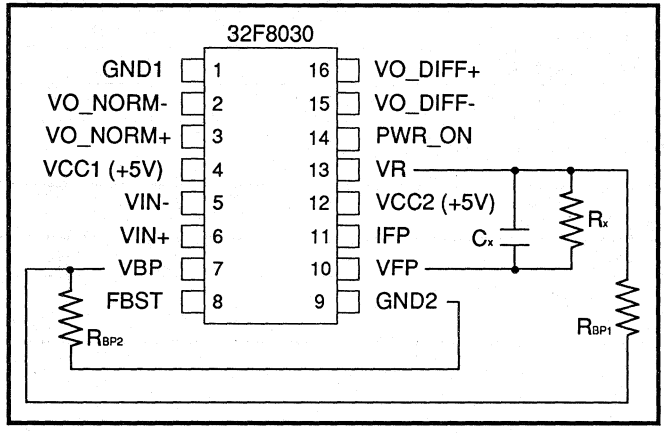


FIGURE 1: 32F8030 Applications Setup 16-Pin SO

VR = 2.2V

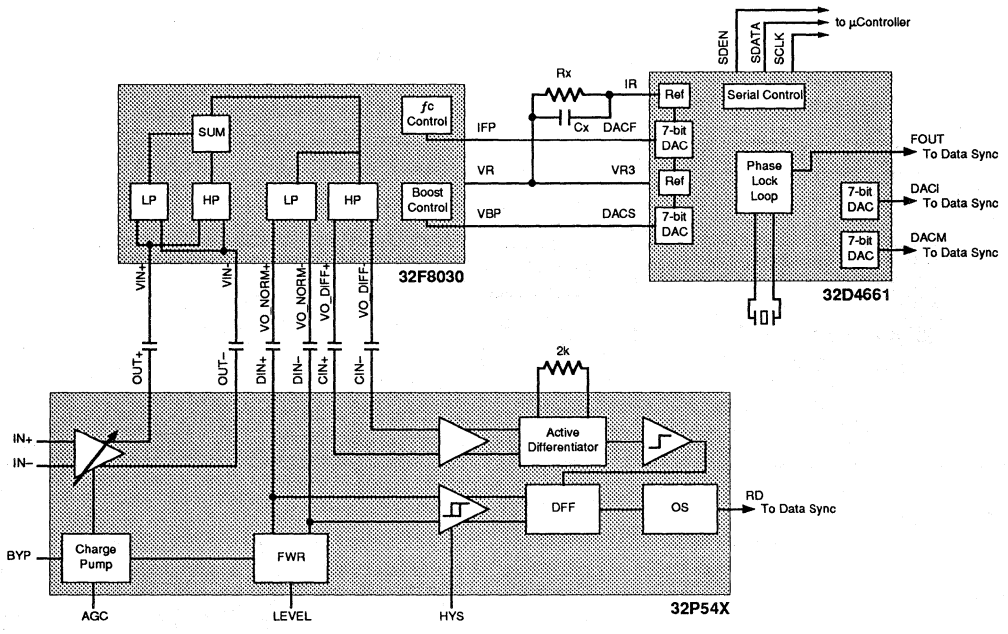
VFP = .667 VR

IVfp = .33VR/Rx

IVfp range: 0.08 mA to 0.8 mA
(0.25 MHz to 2.5 MHz)

Cx = 1000 pF needed for THD at low fc

VFP is used when programming current is set with a resistor from VR.
When VFP is used IFP must be left open.



IOF = DACF output current

IOF = (0.98F•VR)/127Rx

Rx = (0.98F•VR)/127IOF

Rx = current reference setting resistor

VR = Voltage Reference = 2.2V

F = DAC setting: 0-127

Full scale, F = 127

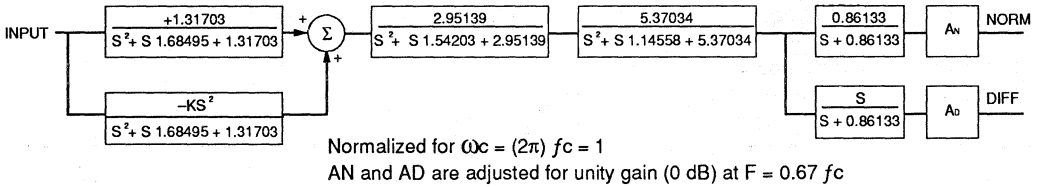
For range of Max fc = 2.5 MHz then IFP = 0.8 mA

Therefore, for Max programming current range to 0.8 mA:

Rx = (0.98)(2.2/0.8) = 2.7 kΩ

Please note that in setups such as this where IFP is used for cutoff frequency programming VFP must be left open.

FIGURE 2: Applications Setup, Constant Density Recording 32F8030, 32P54X, 32D4661



Normalized for $\omega c = (2\pi)\ fc = 1$

AN and AD are adjusted for unity gain (0 dB) at F = 0.67 fc

Denormalize the frequency by substituting $S \rightarrow (S/2\pi fc)$

Eq for fc = 2.5 MHz, $S = S / [(2\pi)(2.5 \cdot 10^6)] = S / (1.57080 \cdot 10^7)$

FIGURE 3: 32F8030 Normalized Block Diagram

TABLE 1: 32F8030 Frequency Boost Calculations - K = 1.31703 ($10^{BOOST(dB)/20}$ -1)

Assuming 9.2 dB boost for VBP = VR

$$\frac{VBP}{VR} \cong \frac{\left(10^{(FB/20)}\right)-1}{1.884}$$

Boost	K	VBP/VR	Boost	K	VBP/VR
1 dB	0.16	0.065	6 dB	1.31	0.288
2 dB	0.34	0.137	7 dB	1.63	0.358
3 dB	0.54	0.219	8 dB	1.99	0.437
4 dB	0.77	0.310	9 dB	2.40	0.526
5 dB	1.03	0.413			

or,

$$\text{boost in dB} = 20\log\left[1.884\left(\frac{VBP}{VR}\right)+1\right]$$

VBP/VR	Boost	VBP/VR	Boost
0.1	1.499 dB	0.6	6.569 dB
0.2	2.777 dB	0.7	7.305 dB
0.3	3.891 dB	0.8	7.984 dB
0.4	4.879 dB	0.9	8.613 dB
0.5	5.765 dB	1.0	9.200 dB

TABLE 2: Calculations

Typical change in *f*-3 dB point with boost

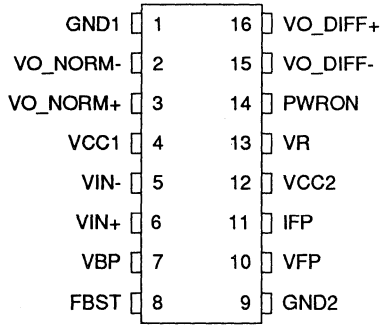
Boost (dB)	Gain @ *f*c(dB)	Gain @ peak(dB)	*f*peak/*f*c	f-3 dB/*f*c
0	-3	0.00	no peak	1.00
1	-2	0.00	no peak	1.21
2	-1	0.00	no peak	1.51
3	0	0.15	0.70	1.80
4	1	0.99	1.05	2.04
5	2	2.15	1.23	2.20
6	3	3.41	1.33	2.33
7	4	4.68	1.38	2.43
8	5	5.94	1.43	2.51
9	6	7.18	1.46	2.59

Notes: 1. *f*c is the original programmed cutoff frequency with no boost
2. *f*-3 dB is the new -3 dB value with boost implemented
3. *f*peak is the frequency where the magnitude peaks with boost implemented

i.e., *f*c = 2.5 MHz when boost = 0 dB
if boost is programmed to 5 dB then f-3 dB = 5.5 MHz
*f*peak = 3.075 MHz

PACKAGE PIN DESIGNATIONS

(Top View)



16-Lead SON, SOL

Thermal Characteristics: θjA

16-lead SON (150 mil)	105° C/W
16-lead SOL (300 mil)	100° C/W

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CAUTION: Use handling procedures necessary for a static sensitive component.

ORDERING INFORMATION

PART DESCRIPTION	ORDER NUMBER	PACKAGE MARK
16-lead SON (150 mil)	32F8030-CN	32F8030-CN
16-lead SOL (300 mil)	32F8030-CL	32F8030-CN

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914

Notes:

silicon systems®
A TDK Group Company

SSI 32F8101/8102/8103/8104
Low-Power Programmable Filter

Advance Information

December 1993

DESCRIPTION

The 32F810X is a high performance, low power, digitally programmable low-pass filter for applications requiring variable-frequency filtering. The device consists of three functional blocks: [1] a 7th-order 0.05° Equiripple Low-Pass filter, [2] two DACs for controlling the filter cutoff frequency and high-frequency peaking (boost), and [3] a Serial Port for programming the fc and Boost DACs. The device is offered in four frequency options: the 32F8101, 9-27 MHz; 32F8102, 6-18 MHz; 32F8103, 4-12 MHz; & 32F8104, 3-9 MHz.

Cutoff frequency and boost are controlled by the two on-chip 7-bit DACs, which are programmed via the 3-line serial interface. Boost is programmable from 0 to 14.3 dB nominally at maximum fc, and is implemented using two symmetrical, real-axis zeroes. Both boost and fc control do not affect the flat group delay response.

The 32F810X device is ideal for variable data rate and variable frequency shaping applications. It requires only a +5V supply and has an Idle mode for minimal power dissipation. The SSI 32F810X is available in 16-lead SON, and 20-Lead SOV packages.

FEATURES

- **Programmable cutoff frequency:**
  - **32F8101 - 9 to 27 MHz**
  - **32F8102 - 6 to 18 MHz**
  - **32F8103 - 4 to 12 MHz**
  - **32F8104 - 3 to 9 MHz**
- **Programmable boost/equalization of 0 to 14.3 dB**
- **Matched normal and differentiated outputs**
- **± 10% fc accuracy**
- **± 2% maximum group delay variation**
- **Less than 1% total harmonic distortion**
- **Low-Z input switch controlled by $\overline{\text{LOWZ}}$ pin**
- **No external filter components required**
- **95 mW nominal power, <5 mW idle**

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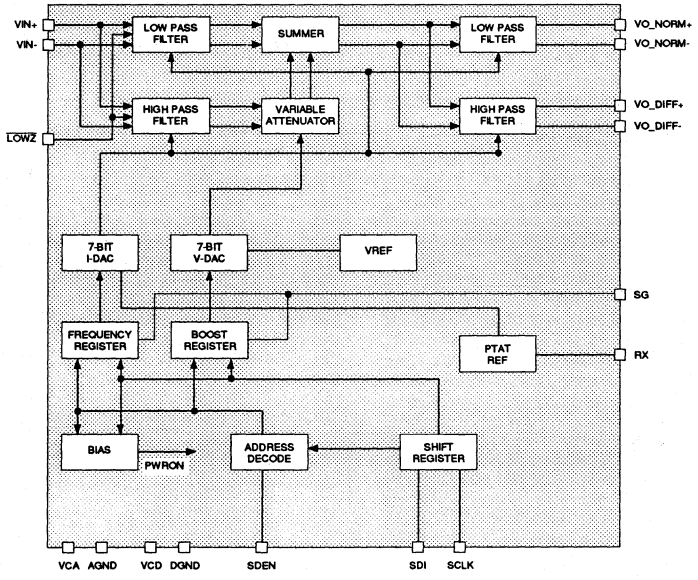
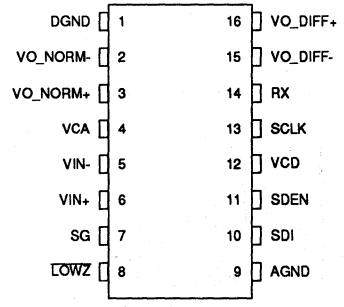
BLOCK DIAGRAM



PIN DIAGRAM



16-Lead SON

CAUTION: Use handling procedures necessary for a static sensitive component.

SSI 32F8101/8102/8103/8104
Low-Power Programmable Filter

FUNCTIONAL DESCRIPTION

The SSI 32F810X programmable filter consists of an electronically controlled low-pass filter with a separate differentiated low-pass output. A seven-pole, low-pass filter is provided along with a single-pole, single-zero differentiator. Both outputs have matched delays. The delay matching is unaffected by any amount of programmed equalization or bandwidth. Programmable bandwidth and boost/equalization is provided by internal 7-bit control DACs. High-frequency boost equalization is accomplished by a two-pole, low-pass with a two-pole, high-pass feed forward section to provide complimentary real axis zeros. A variable attenuator is used to program the zero locations.

The filter implements a 0.05 degree equiripple linear phase response. The normalized transfer functions (i.e., $\omega c = 2\pi fc = 1$) are:

$$Vnorm/Vi = 13.65983 \cdot [(-Ks^2 + 1.31703)/D(s)] \cdot An$$

and

$$Vdiff/Vi = (Vnorm/Vi) \cdot (s/0.86133) \cdot Ad$$

Where D (s)=
$(S^2+1.68495s+1.31703)(S^2+1.54203\ s+2.95139)$
$(S^2+1\ .4558s+5.37034)(s+0.86133)$,

An and Ad are adjusted for a gain of 1 at $fs=(2/3)fc$.

FILTER OPERATION

Normally AC coupled differential signals are applied to the VIN± inputs of the filter, although DC coupling can be implemented. To improve settling time of the coupling capacitors, the VIN± inputs are placed into a Low-Z state when the $\overline{LOWZ}$ pin is brought high. The programmable bandwidth and boost/equalization features are controlled by internal DACs and the registers programmed through the serial port. The current reference for both DACs is set using a single 13.3 kΩ external resistor connected from pin RX to ground. The voltage at pin RX is proportional to absolute temperature (PTAT), hence the current for the DACs is a PTAT reference current.

Bandwidth Control: The programmable bandwidth is set by the filter cutoff DAC. This DAC has two separate 7-bit registers that can program the DAC value as follows:

***fc* = 0.2126 • DACF (MHz)** for the 32F8101
***fc* = 0.1417 • DACF (MHz)** for the 32F8102
***fc* = 0.09449 • DACF (MHz)** for the 32F8103
***fc* = 0.07087 • DACF (MHz)** for the 32F8104
where DACF = Cutoff Frequency Control Register value (decimal)

The filter cutoff set by the internal DAC is the unboosted 3 dB frequency. When boost/equalization is added, the actual 3 dB point will move out. Table 1 provides information on boost versus 3 dB frequency.

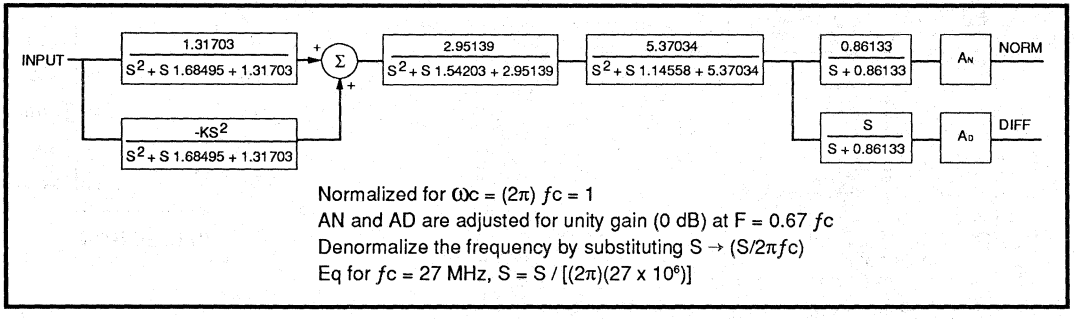


FIGURE 1: 32F8101/8102/8103/8104 Normalized Block Diagram

TABLE 1: Calculations

Typical change in f-3 dB point with boost

Boost (dB)	Gain@fc (dB)	Gain@ peak (dB)	$f$peak/fc	f-3dB/fc	K
0	-3	0.00	no peak	1.00	0
1	-2	0.00	no peak	1.21	0.16
2	-1	0.00	no peak	1.51	0.34
3	0	0.15	0.70	1.80	0.54
4	1	0.99	1.05	2.04	0.77
5	2	2.15	1.23	2.20	1.03
6	3	3.41	1.33	2.33	1.31
7	4	4.68	1.38	2.43	1.63
8	5	5.94	1.43	2.51	1.97
9	6	7.18	1.46	2.59	2.40
10	7	8.40	1.48	2.66	2.85
11	8	9.59	1.51	2.73	3.36
12	9	10.77	1.51	2.80	3.93
13	10	11.92	1.53	2.87	4.57
14	11	13.06	1.53	2.93	5.28
15	12	14.18	1.56	3.0	6.09

Notes:
1. fc is the original programmed cutoff frequency with no boost
2. f-3 dB is the new -3 dB value with boost implemented
3. $f$peak is the frequency where the amplitude reaches its maximum value with boost implemented

   i.e., fc = 9 MHz when boost = 0 dB

   if boost is programmed to 5 dB then f-3 dB = 19.8 MHz

   $f$peak = 11.07 MHz

4. $K = 1.31703\,(10^{\frac{\text{BOOST (dB)}}{20}} - 1)$

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BOOST/EQUALIZATION CONTROL

The programmable equalization is also controlled by an internal DAC. The 7-bit Filter Boost Control Register (FBCR) determines the amount of equalization that will be added to the 3 dB cutoff frequency, as follows:

$$\text{Boost} = 20 \log [(0.0339 \cdot \text{FBCR}) + 1] \text{ (dB)}$$
$$20 \log [(0.0283 \cdot \text{FBCR}) + (3.75 \cdot 10^{-5} \cdot \text{FBCR} \cdot \text{DACF}) + 1]$$

For example, with the DAC set for maximum output (FBCR = 7F hex or 127) at the maximum cutoff frequency (DACF = 7F hex or 127) there will be 14.3 dB of boost added at the 3 dB frequency. This will result in +10 dB of signal boost above the 0 dB baseline.

SERIAL INTERFACE OPERATION

The serial interface is a CMOS bi-directional port for reading and writing programming data from/to the internal registers of the 32F810X. For data transfers SDEN is brought high, serial data is presented at the SDATA pin, and a serial clock is applied to the SCLK pin.

After the SDEN goes high, the first 16 pulses applied to the SCLK pin will shift the data presented at the SDATA pin into an internal shift register on the rising edge of each clock. An internal counter prevents more than 16 bits from being shifted into the register. The data in the shift register is latched when SDEN goes low. If less than 16 clock pulses are provided before SDEN goes low, the data transfer is aborted.

All transfers are shifted into the serial port LSB first. The first byte of the transfer is address and instruction information. The LSB of this byte is the R/W bit which determines if the transfer is a read (1) or a write (0). The remaining seven bits determine the internal register to be accessed. The second byte contains the programming data. At initial power-up, the contents of the internal registers will be in an unknown state and they must be programmed prior to operation. During power down modes, the serial port remains active and register programming data is retained.

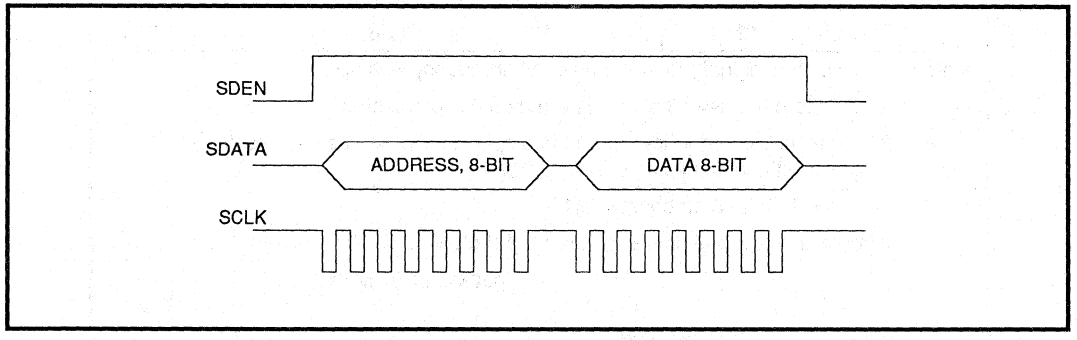

FIGURE 2: Serial Port Data Transfer Format

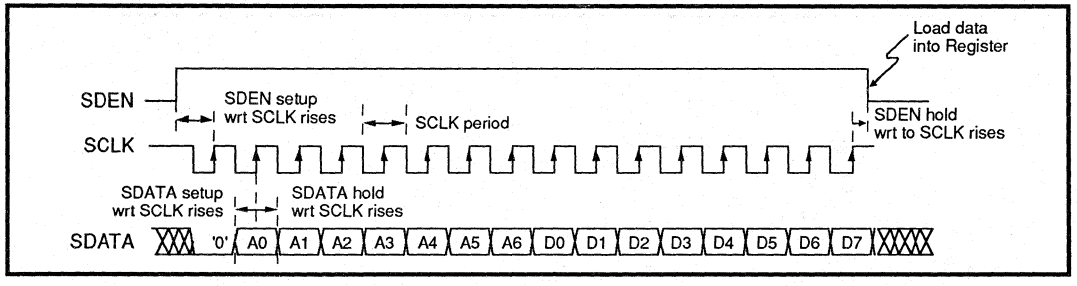

FIGURE 3: Serial Interface Timing Diagram - Writing Control Register

TABLE 2: Serial Port Register Mapping

REGISTER NAME	A6			ADDRESS			A0	R/W	D7	DATA BIT MAP						D0
POWER DOWN CONTROL	0	0	0	0	0	1	0	0	--	--	--	--	--	FILTER 1=DISABLE 0=ENABLE	--	
DATA MODE CUTOFF	0	0	0	0	0	1	1	0	*	DAC BIT 6	DAC BIT 5	DAC BIT 4	DAC BIT 3	DAC BIT 2	DAC BIT 1	DAC BIT 0
SERVO MODE CUTOFF	0	0	1	0	0	1	1	0	*	DAC BIT 6	DAC BIT 5	DAC BIT 4	DAC BIT 3	DAC BIT 2	DAC BIT 1	DAC BIT 0
FILTER BOOST, DATA	0	0	0	1	0	1	1	0	--	DAC BIT 6	DAC BIT 5	DAC BIT 4	DAC BIT 3	DAC BIT 2	DAC BIT 1	DAC BIT 0
FILTER BOOST, SERVO	0	0	1	1	0	1	1	0	--	DAC BIT 6	DAC BIT 5	DAC BIT 4	DAC BIT 3	DAC BIT 2	DAC BIT 1	DAC BIT 0

* These bits are used only for testing. They should be programmed to 0 in actual operation.

PIN DESCRIPTION

POWER SUPPLY PINS

NAME	TYPE	DESCRIPTION
VCA	-	Filter analog power supply pin
VCD	-	Serial port power supply pin
AGND	-	Filter analog ground pin
DGND	-	Serial port digital ground pin

INPUT PINS

VIN+, VIN-	I	FILTER SIGNAL INPUTS: The AGC output signals must be AC coupled into these pins.
SG	I	SERVO GATE: TTL input when high enables servo frequency and boost registers to the control DACs. When low the data frequency and boost registers are enabled.
$\overline{\text{LOWZ}}$	I	LOW_Z CONTROL: TTL input when low reduces the filter input resistance. When high, the input is at high impedance state.

OUTPUT PINS

VO_DIFF+, VO_DIFF-	O	DIFFERENTIAL DIFFERENTIATED OUTPUTS: Filter differentated outputs. These outputs are normally AC coupled.
VO_NORM+, VO_NORM-	O	DIFFERENTIAL NORMAL OUTPUTS: Filter normal low pass output signals. These outputs are normally AC coupled.
RX	-	REFERENCE RESISTOR INPUT: An external 13.3 kΩ, 1% resistor is connected from this pin to ground to establish a precise PTAT (proportional to absolute temperature) reference current for the filter.

SERIAL PORT PINS

SDEN	I/O	SERIAL DATA ENABLE: Serial enable CMOS compatible input. A high level TTL input enables the serial port.
SDI	I/O	SERIAL DATA: Serial data CMOS compatible input. NRZ programming data for the internal registers is applied to this input.
SCLK	I/O	SERIAL CLOCK: Serial clock CMOS compatible input. The clock applied to this pin is synchronized with the data applied to SDATA.

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, the recommended operating conditions are as follows: 4.5V < POSITIVE SUPPLY VOLTAGE < 5.5V, 0 °C < T (ambient) < 70 °C, and 25 °C < T(junction) < 135 °C. Currents flowing into the chip are positive. Current maximums are currents with the highest absolute value.
Rx = 13.3 kΩ, Cx = 1000 pF from Rx pin to VCA. Input signals are AC-coupled into VIN±.

ABSOLUTE MAXIMUM RATINGS

Operation beyond the maximum ratings may damage the device.

PARAMETER	RATING
Storage Temperature	-65 to 150 °C
Junction Operating Temperature	+130 °C
Positive Supply Voltage (Vp)	-0.5 to 7V
Voltage Applied to Logic Inputs	-0.5V to Vp + 0.5V
All other Pins	-0.5V to Vp + 0.5V

5

POWER SUPPLY CURRENT AND POWER DISSIPATION

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
ICC (VCA,D)	Output pins open Ta = 27 °C VP = 5.0 V, DACF = 127 Boost = 0 dB		19		mA
PWR Power Dissipation	Output pins open Ta = 27 °C VP = 5.0 V, Boost = 0 dB DACF = 127		95		mW
Sleep Mode Power	PWRON = 1			5	mW

TTL COMPATIBLE INPUTS

Input low voltage (VIL)		-0.3		0.8	V
Input high voltage (VIH)		2.0		VPD +0.3	V
Input low current (IIL)	VIL = 0.4V	-0.4			mA
Input high current (IIH)	VIH = 2.4V			100	µA

CMOS COMPATIBLE INPUTS

Input low voltage	Vp = 5.0V			1.5	V
Input high voltage	Vp = 5.0V	3.5			V

ELECTRICAL SPECIFICATIONS (continued)

SERIAL PORT

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
SCLK period		Read from serial port	140			ns
		Write to serial port	100			ns
SCLK low time	TCKL	Read from serial port	60			ns
		Write to serial port	40			ns
SCLK high time	TCKH	Read from serial port	60			ns
		Write to serial port	40			ns
Enable to SCLK	TSENS		35			ns
SCLK to disable	TSENH		100			ns
Data set-up time	TDS		15			ns
Data hold time	TDH		15			ns
SDATA tri-state delay	TSENDL				50	ns
SDATA turnaround time	TTRN		70			ns
SDEN low time	TSL		200			ns

PROGRAMMABLE FILTER CHARACTERISTICS

Filter cutoff range (32F8101)	fc @ -3 dB point fc = (0.2126 MHz) x DACF, Boost = 0 dB 42 ≤ DACF ≤ 127	9		27	MHz
Filter cutoff range (32F8102)	fc @ -3 dB point fc = (0.1417 MHz) x DACF, Boost = 0 dB 42 ≤ DACF ≤ 42	6		18	MHz
Filter cutoff range (32F8103)	fc @ -3 dB point fc = (0.09449 MHz) x DACF, Boost = 0 dB 42 ≤ DACF ≤ 127	4		12	MHz
Filter cutoff range (32F8104)	fc @ -3 dB point fc = (0.07087 MHz) x DACF, Boost = 0 dB 42 ≤ DACF ≤ 127	3		9	MHz
Filter cutoff accuracy	DACF = 42 and 125	-15		15	%
FNP,FNN differential gain AN	f=0.67xfc, boost=0 dB	0.7	1.0	1.25	V/V
FDP, FDN differential gain AD	f=0.67xfc, boost=0 dB	0.8AN		1.2AN	V/V

PROGRAMMABLE FILTER CHARACTERSITICS (continued)

PARAMETER	CONDITIONS		MIN	NOM	MAX	UNITS
Boost accuracy	6.3 dB, DACF = 42, DACS = 36		-1.0		+1.0	dB
	6.8 dB, DACF = 127, DACS = 36		-1.0		+1.0	dB
	9.5 dB, DACF = 42, DACS = 67		-1.25		+1.25	dB
	10 dB, DACF = 127, DACS = 67		-1.25		+1.25	dB
	13.6 dB, DACF = 42, DACS = 127		1.5		+1.5	dB
	14.3 dB, DACF = 127, DACS = 127		-1.5		+1.5	dB
Data mode group delay variation, DACF = 42 to 127, DACS = 0 to 127	fc = 3 to 9 MHz f = 0.2 fc to fc		-2		+2	%
	f = fc to 1.75 fc		-3		+3	%
Data mode group delay variation, DACS = 0 to 127	fc = max f = 0.2 fc to fc	32F8101	-0.5		+0.5	ns
		32F8102	-0.75		+0.75	ns
		32F8103	-1.0		+1.0	ns
		32F8104	-1.25		+1.25	ns
	fc = min f = 0.2 fc to fc	32F8101	-1.25		+1.25	ns
		32F8102	-1.9		+1.9	ns
		32F8103	-2.5		+2.5	ns
		32F8104	-3.75		+3.75	ns
	fc = max f = fc to 1.75fc	32F8101	-0.75		+0.75	ns
		32F8102	-1.15		+1.15	ns
		32F8103	-1.5		+1.5	ns
		32F8104	-1.9		+1.9	ns
	fc = min f = fc to 1.75fc	32F8101	-1.9		+1.9	ns
		32F8102	-2.85		+2.85	ns
		32F8103	-3.75		+3.75	ns
		32F8104	-5.65		+5.65	ns
Filter differential input dynamic range	THD = 1.5%, f = 0.67fc boost = 0 dB, normal and differentiated outputs		1.0			Vpp
Filter differential output dynamic range	THD = 1.5%, f = 0.67fc boost = 0 dB, normal and differentiated outputs		1.0			Vpp
Filter differential input resistance	Normal		5.0			kΩ
	Low-Z			600		Ω
Filter differential input capacitance					7.0	pF

5

ELECTRICAL SPECIFICATIONS (continued)

PROGRAMMABLE FILTER CHARACTERSITICS (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Output Noise Voltage: BW = 100 MHz, Rs = 50Ω					
32F8101					
differentiated output	fc = 27 MHz, boost = 0 dB		4.4	6.6	mV Rms
differentiated output	fc = 27 MHz, DACS =127		7.7	11.6	mV Rms
normal output	fc = 27 MHz, boost = 0 dB		2.5	3.8	mV Rms
normal output	fc = 27 MHz, DACS =127		3.7	5.6	mV Rms
32F8102					
differentiated output	fc = 18 MHz, boost = 0 dB		3.8	5.7	mV Rms
differentiated output	fc = 18 MHz, DACS =127		6.9	10.4	mV Rms
normal output	fc = 18 MHz, boost = 0 dB		2.2	3.3	mV Rms
normal output	fc = 18 MHz, DACS =127		3.2	4.8	mV Rms
32F8103					
differentiated output	fc = 9 MHz, boost = 0 dB		4.1	6.2	mV Rms
differentiated output	fc = 9 MHz, DACS =127		6.5	9.8	mV Rms
normal output	fc = 9 MHz, boost = 0 dB		2.2	3.3	mV Rms
normal output	fc = 9 MHz, DACS =127		3.1	4.7	mV Rms
32F8104					
differentiated output	fc = 9 MHz, boost = 0 dB		3.6	5.4	mV Rms
differentiated output	fc = 9 MHz, DACS =127		5.6	8.4	mV Rms
normal output	fc = 9 MHz, boost = 0 dB		2.0	3.0	mV Rms
normal output	fc = 9 MHz, DACS =127		2.7	4.1	mV Rms
Filter output sink current			0.5		mA
Filter output offset voltage		-200		200	mV
Filter output source current		2.0			mA
Filter output resistance	single ended			200	Ω
Rx pin voltage	Ta = 27 °C		600		mV
	Ta = 127 °C		800		mV
Rx resistance	1% fixed value		13.3		kΩ

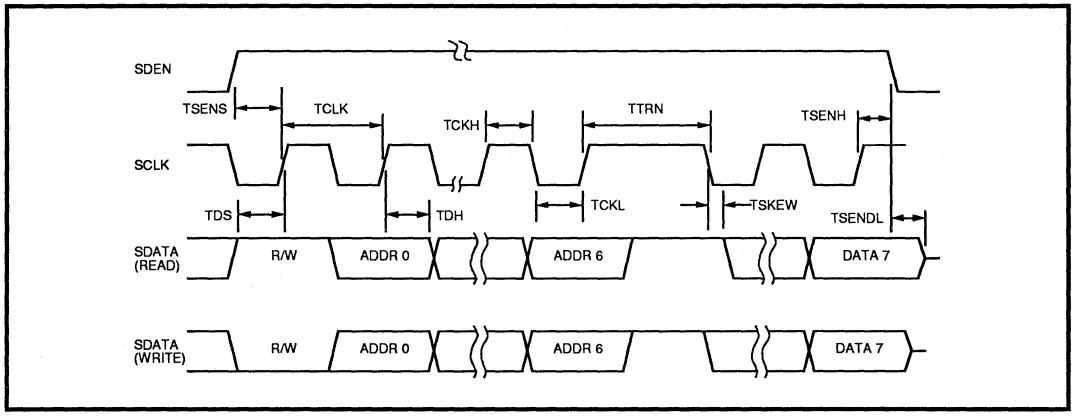

FIGURE 4: Serial Port Timing Information

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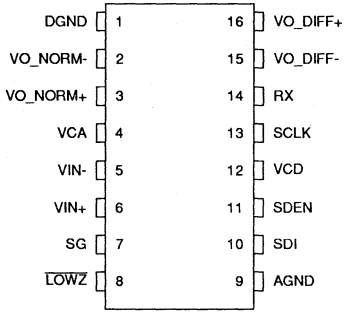
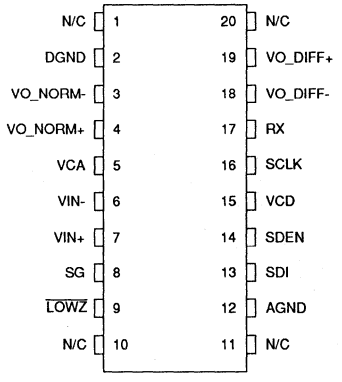
PACKAGE PIN DESIGNATIONS

(Top View)



16-Lead SON



20-Lead SOV

THERMAL CHARACTERISTICS: θja

16-lead SON	100° C/W
20-lead SOV	125° C/W

CAUTION: Use handling procedures necessary for a static sensitive component.

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914

Notes:

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SSI 32F8120
Low-Power Programmable Electronic Filter

January 1994

DESCRIPTION

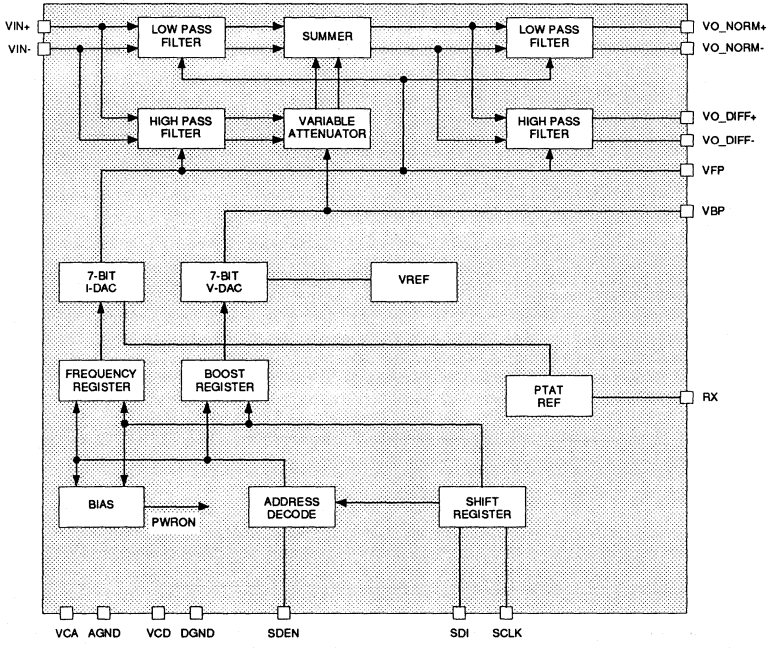
The SSI 32F8120 is a continuous time, low pass filter with programmable bandwidth and high frequency boost. The low pass filter is a 2 zero / 7 pole 0.05° phase equiripple type, featuring excellent group delay characteristics. It features 1.5 - 8 MHz programmable bandwidth and 0-10 dB programmable boost. Both functions are controlled by 7-bit command words, which are input via a 3-line serial interface.

FEATURES

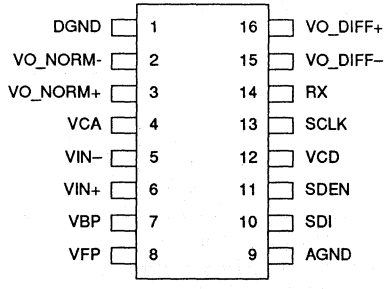
- **Programmable filter cutoff frequency (fc =1.5 to 8 MHz) with no external components**
- **Programmable pulse slimming equalization (0 to 10 dB boost at the filter cutoff frequency)**
- **± 10% cutoff frequency accuracy**
- **Matched normal and differentiated low-pass outputs**
- **Differential filter inputs and outputs**
- **Device Idle mode**
- **+5V only operation**
- **No external filter components required**
- **Supports constant density recording**

5

BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

SSI 32F8120
Low-Power Programmable Electronic Filter

FUNCTIONAL DESCRIPTION

CUTOFF FREQUENCY PROGRAMMING

The SSI 32F8120 programmable electronic filter can be set to a filter cutoff frequency from 1.5 to 8 MHz. The cutoff frequency can be set by using the serial port through pins SDI, SDEN, and SCLK. SDI is the serial data input for an 8-bit control shift register, SDEN is the control register enable, and SCLK is the control register clock. The data packet is transmitted MSB (D7) first. The first four bits are the register address, the last four are the data bits. Registers larger than four bits must be loaded with two 8-bit data packets. See Table 1.

fc is determined by the equation:

fc (MHz) = 0.061321 (F_Code) + 0.212264

1.5 MHz ≤ fc ≤ 8 MHz

21 ≤ F_ Code ≤ 127

SLIMMER HIGH FREQUENCY BOOST PROGRAMMING

The amplitude of the input signal at frequencies near the cutoff frequency can be increased using this feature. By controlling the V-DAC output, the boost can be determined. The amount of boost at the cutoff frequency is related to the V-DAC output by the following formula:

$$[\text{Output of V-DAC} = \text{VBP} = \text{VREF} \times \frac{\text{S\_Code}}{127}]$$

BOOST (dB) = 20•log [0.01703 (S_Code) +1].

TABLE 1

ADDRESS BITS				USAGE	DATA BITS			
D7	D6	D5	D4		D3	D2	D1	D0
X	0	0	0	S-MSB REGISTER	X	S6	S5	S4
X	0	0	1	S-LSB REGISTER	S3	S2	S1	S0
X	0	1	0	F-MSB REGISTER	X	F6	F5	F4
X	0	1	1	F-LSB REGISTER	F3	F2	F1	F0
X	1	1	1	P REGISTER	X	X	X	P0

X = Don't Care
S = 7-bit Boost (Slimming) Control
F = 7-bit Frequency (Bandwidth) Control
P = Power Down Control; PO = 1 for power up; PO = 0 for power down

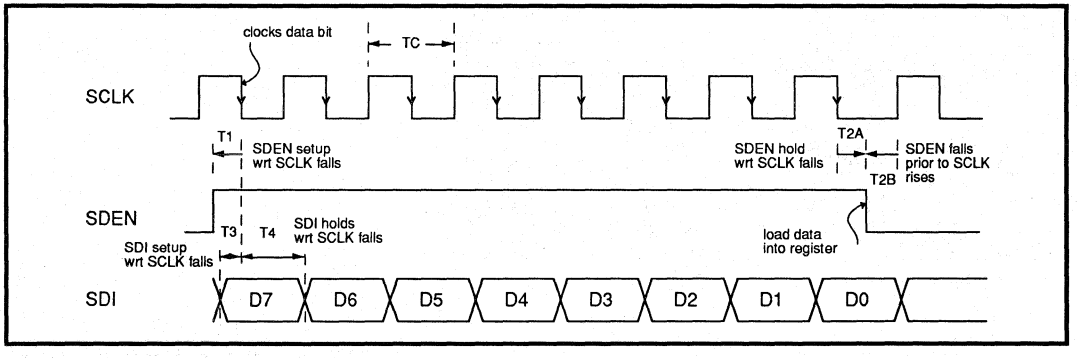


FIGURE 1: Serial Port Timing Diagram

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
VIN+, VIN–	I	DIFFERENTIAL FILTER INPUTS. The input signals must be AC coupled to these pins.
VO_NORM+, VO_NORM–	O	DIFFERENTIAL NORMAL OUTPUTS. The output signals must be AC coupled to the pulse detector.
VO_DIFF+ VO_DIFF–	O	DIFFERENTIAL DIFFERENTIATED OUTPUTS. For minimum pulse pairing, these outputs should be AC coupled to the pulse detector.
SDEN	I	SERIAL DATA ENABLE. A logic HIGH level allows SERIAL CLOCK to clock data into the control register via the SERIAL DATA input. A logic LOW level latches the register data and issues the information to the appropriate circuitry.
SCLK	I	SERIAL CLOCK. Negative edge triggered clock input for serial register.
SDI	I	SERIAL DATA INPUT.
RX	–	REFERENCE CURRENT SET. With an external resistor (Rx = 5 kΩ ±1%) to ground, this pin gives a voltage proportional to the absolute temperature, setting the range for VFP.
VCA	I	ANALOG +5 VOLT SUPPLY.
VCD	I	DIGITAL +5 VOLT SUPPLY.
AGND	I	ANALOG GROUND.
DGND	I	DIGITAL GROUND.
VBP	O	BOOST PROGRAMMING VOLTAGE. Output of V-DAC which programs the boost.
VFP	O	CUTOFF FREQUENCY PROGRAMMING VOLTAGE. Output of I-DAC which programs the cutoff frequency.*

*A minimum load resistance of 150 kΩ should be used to avoid affecting the total minimum on-chip resistance of 1.35 kΩ.

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ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may damage the device.

PARAMETER	RATING
Storage Temperature	-65 to +150 °C
Junction Operating Temperature, Tj	+130 °C
Supply Voltage, VCC	-0.5 to 7V
Voltage Applied to Inputs*	-0.5 to VCC V
Maximum Power Dissipation, fc = 8 MHz, Vcc = 5.5V	0.5W
T1 Lead Temperature (1/16" from case for 10 seconds)	260 °C
* Analog input signals of this magnitude shall not cause any change or degradation in filter performance after signal has returned to normal operating range.	

RECOMMENDED OPERATING CONDITIONS

Supply voltage, VCC	4.5V < VCC < 5.5V
Ambient Temperature	0 °C < Ta < 70 °C
Tj Junction Temperature	0 °C < Tj < 130 °C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified recommended operating conditions apply.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Isupply	VCC = 5.5V, outputs unloaded		55	75	mA
Idle Mode Current			9	13	mA
Idle to Active Mode Recovery Time				50	µs
Serial port program to output response time				50	µs

DC Characteristics

VIH	High Level Input Voltage	TTL input	2.0			V
VIL	Low Level Input Voltage				0.8	V
IIH	High Level Input Current	VIH = 2.7V			20	µA
IIL	Low Level Input Current	VIL = 0.4V	–1.5			mA

Filter Characteristics

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
fc Filter Cutoff Frequency	21 ≤ F_Code ≤ 127	1.5		8	MHz
FCA Filter fc Accuracy	F_Code = 127	-10		+10	%
	F_Code = 21	-15		+15	%
Cutoff Resolution	1.5 to 8 MHz	100			kHz
AO VO_NORM Diff Gain	F = 0.67 fc	0.7		1.1	V/V
AD VO_DIFF Diff Gain	F = 0.67 fc	0.90 AO		1.2 AO	V/V
FB Frequency Boost at fc	FB(dB) = 20 log [0.01703 (S_Code) +1]	0		10	dB
FBA Frequency Boost Accuracy	0 to 10 dB, Ta < 22 °C	–1.5		+1.5	dB
FBA Frequency Boost Accuracy	0 to 10 dB, Ta > 22 °C	–1		+1	dB
TGD0 Group Delay Variation Without Boost	0.2 fc - fc	–2% gdm		+2% gdm	ns
fc = 1.5 - 8 MHz gdm = group delay magnitude	fc - 1.75 fc	–3% gdm		+3% gdm	ns
TGDB Group Delay Variation With Boost	0.2 fc - fc	–2% gdm		+2% gdm	ns
fc = 1.5 - 8 MHz	fc - 1.75 fc	–3% gdm		+3% gdm	ns
Boost Resolution	1.5 to 8 MHz	.25			dB
VOF Filter Output Dynamic Range	THD = 1.5% max, VBP = 0, VO_NORM 1000 pF capacitor across Rx F_Code = 127	1.5			Vppd
VOF Filter Output Dynamic Range	THD = 3.5% max, VBP = 0, VO_DIFF 1000 pF capacitor across Rx F_Code = 127	1.5			Vppd
VOF Filter Output Dynamic Range	THD = 1.5% max, VBP = 0, VO_NORM 1000 pF capacitor across Rx F_Code = 21	1.0			Vppd
VOF Filter Output Dynamic Range	THD = 2.0% max, VBP = 0, VO_DIFF 1000 pF capacitor across Rx F_Code = 21	1.0			Vppd

ELECTRICAL SPECIFICATIONS (continued)

Filter Characteristics (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
RIN Filter Diff Input Resistance		3.0			kΩ
CIN Filter Input Capacitance				7	pF
EOUT Output Noise Voltage (VO_NORM)	BW = 100 MHz, 0 dB Boost 50Ω input fc = 8 MHz 10 dB Boost		1.8 2.35	3 4	mVRms mVRms
EOUT Output Noise Voltage (VO_DIFF)	BW = 100 MHz, 0 dB Boost 50Ω input fc = 8 MHz 10 dB Boost		4.2 5.85	6 9	mVRms mVRms
IO- Filter Output Sink Current		1.0			mA
IO+ Filter Output Source Current		3.0			mA
RO Filter Output Resistance (Single ended)	Output source current, IO+ = 1 mA			60	Ω
TC Period, SCLK		100			ns
T1 SDEN Setup to SCLK Falls		10		TC/2-10	ns
T2A SDEN Hold wrt SCLK Falls		10		TC/4	ns
T2B SDEN Falls prior to SCLK Rises		25			ns
T3 SDI Setup to SCLK Falls		25			ns
T4 SDI Hold to SCLK Falls		25			ns
Power Supply Rejection Ratio	100 mVpp @ 5 MHz on VCA, VCD	40	70		dB
Common Mode Rejection Ratio	Vin = 0 VDC + 100 mVpp @5 MHz	30	50		dB
Bias: Vin+, Vin-	VCC = 5V	2.5	2.9	3.3	V
VO_NORM+, VO_NORM–	VCC = 5V	2.8	3.2	3.6	V
VO_DIFF+, VO_DIFF-	VCC = 5V	2.8	3.2	3.6	V
Output offset Normal and Differentiated		-150		+150	mV

TABLE 2: Calculations

Typical change in f-3 dB point with boost

Boost (dB)	Gain@fc (dB)	Gain@ peak (dB)	$f$peak/fc	f-3dB/fc	K
0	-3	0.00	no peak	1.00	0
1	-2	0.00	no peak	1.21	0.16
2	-1	0.00	no peak	1.51	0.34
3	0	0.15	0.70	1.80	0.54
4	1	0.99	1.05	2.04	0.77
5	2	2.15	1.23	2.20	1.03
6	3	3.41	1.33	2.33	1.31
7	4	4.68	1.38	2.43	1.63
8	5	5.94	1.43	2.51	1.97
9	6	7.18	1.46	2.59	2.40
10	7	8.40	1.48	2.66	2.85

Notes: 1. fc is the original programmed cutoff frequency with no boost

2. f-3 dB is the new -3 dB value with boost implemented

3. $f$peak is the frequency where the amplitude reaches its maximum value with boost implemented

i.e., fc = 2 MHz when boost = 0 dB

if boost is programmed to 5 dB then f-3 dB = 4.40 MHz

$f$peak = 2.46 MHz

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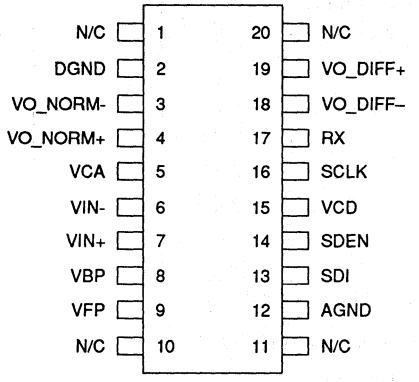
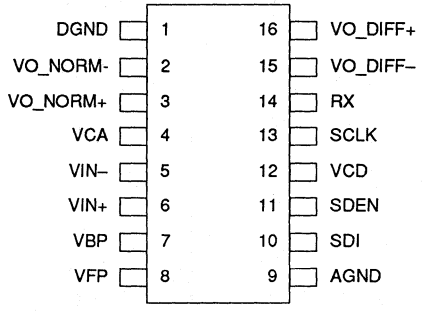
SSI 32F8120
Low-Power Programmable Electronic Filter

PACKAGE PIN DESIGNATIONS
(Top View)



20-Lead SOV



16-Lead SOL

THERMAL CHARACTERISTICS: θja

16-lead SOL	100° C/W
20-lead SOV	125° C/W

CAUTION: Use handling procedures necessary for a static sensitive component.

ORDERING INFORMATION

PART DESCRIPTION		ORDER NUMBER	PACKAGE MARK
SSI 32F8120	16-Lead SOL	32F8120-CL	32F8120-CL
	20-Lead SOV	32F8120-CV	32F8120-CV

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX 714/573-6914

Patent No. 5,063,309, Patent Pending 823,067

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SSI 32F8130/8131
Low-Power Programmable Electronic Filter

November 1993

DESCRIPTION

The SSI 32F8130/8131 Programmable Electronic Filters are digitally controlled low pass filters with a normal low pass output and a time differentiated low pass output. The low pass filter is of a 7-pole / 2-zero 0.05° phase equiripple type, with flat group delay response beyond the passband.

The SSI 32F8130/8131 bandwidth and boost are controlled by two on-chip 7-bit DACs, which are programmed via a 3-line serial interface. The SSI 32F8130 filter bandwidth is programmable from 200 kHz to 2.2 MHz. The SSI 32F8131 is programmable from 150 kHz to 1.4 MHz. The boost is programmable from 0 to 10 dB. Because the boost function is implemented as two zeros on the real axis with opposite sign, the flat group delay characteristic is not affected by the boost programming.

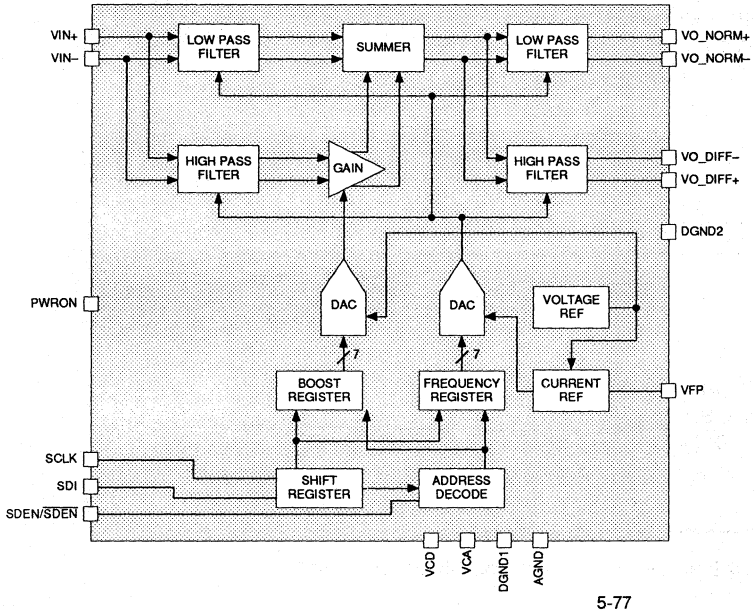
The SSI 32F8130/8131 are ideal for multi-rate, equalization applications. They require only a +5V supply and have a Power Down mode for minimal idle dissipation. The SSI 32F8130/8131 is available in a 16-lead SOL package.

FEATURES

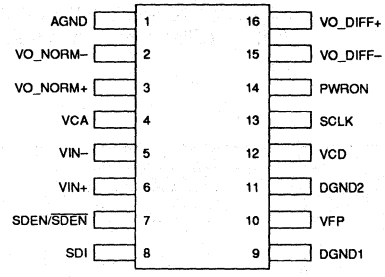
- **Programmable filter cutoff frequency (SSI 32F8130 FC=0.20 to 2.2 MHz, SSI 32F8131: FC = 0.15 to 1.4 MHz) with no external components, serial data connections to minimze pin count**
- **Power Down mode (<5 mW)**
- **Programmable pulse slimming equalization (0 to 10 dB boost at the filter cutoff frequency)**
- **Matched normal and differentiated low-pass outputs**
- **Differential filter inputs and outputs**
- **Programming via internal 7-bit DACs**
- **No external filter components required**
- **+5V only operation**
- **Supports constant density recording**

5

BLOCK DIAGRAM



PIN DIAGRAM



SSI 32F8130: Lead 7 = SDEN
SSI 32F8131: Lead 7 = $\overline{\text{SDEN}}$

CAUTION: Use handling procedures necessary for a static sensitive component.

SSI 32F8130/8131
Low-Power Programmable Electronic Filter

FUNCTIONAL DESCRIPTION

The SSI 32F8130/8131, a high performance programmable electronic filter, provides a 7-pole / 2-zero 0.05° equiripple linear phase low pass function with matched normal and time differentiated outputs. The device includes multiple biquads and first-order sections to accomplish the filter function, two 7-bit DACs for bandwidth and boost controls, a 3-line serial interface, and complete bias reference circuits. Only one external precision 8.25 kΩ resistor should be connected from the VFP pin to ground for operation. See Figure 1.

SERIAL INTERFACE

The SSI 32F8130/8131 allows easy digital controls of filter bandwidth and magnitude equalization via a 3-line serial interface. The three pins are SDI, SDEN and SCLK. SDI is the serial data input to an internal 8-bit shift register. SDEN is the shift register enable. SCLK is the shift register clock. Besides the 8-bit shift register which accepts data from the SDI input, there are four 4-bit registers which hold the filter bandwidth and boost controls. Two 4-bit registers are assigned to each control function, because a 7-bit binary control is required for each function.

The S-MSB register, whose address code is X000, holds the 3 MSBs of the boost control. The S-LSB register, whose address code is X001, holds the 4 LSBs of the boost control. The F-MSB register, whose address code is X010, holds the 4 MSBs of the cutoff frequency control. The F-LSB register, whose address code is X011, holds the 4 LSBs of the cutoff frequency control.

The serial interface consists of data packets, which are structured as 4-bit address decode followed by 4-bit data. Figure 2 shows the serial interface timing to successfully program the SSI 32F8130/8131.

CUTOFF FREQUENCY PROGRAMMING

The cutoff frequency, fc, is defined as the -3 dB bandwidth with no magnitude equalization applied, and is programmable from 200 kHz to 2.2 MHz for SSI 32F8130, and 150 kHz to 1.4 MHz for SSI 32F8131. While the fc is controlled by an on-chip 7-bit DAC, the cutoff frequency resolution is better than 20-kHz step.

Let F_Code be the decimal equivalent of the 7-bit control. The cutoff frequency can be determined by the following equations:

SSI 32F8130 fc (kHz) = 17.3 x F_Code

SSI 32F8131 fc (kHz) = 10.81 x F_Code +37

where 12 ≤ F_Code ≤ 127.

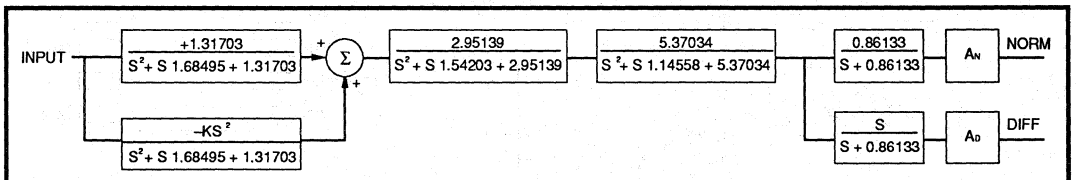
MAGNITUDE EQUALIZATION PROGRAMMING

The magnitude equalization, measured in dB, is the amount of high frequency peaking at the cutoff frequency relative to the original -3 dB point. For example, when 10 dB boost is applied, the magnitude response peaks up 7 dB above the DC gain. This equalization function is also controlled by an on-chip 7-bit DAC.

Let S_Code be the decimal equivalent of the 7-bit control. The magnitude equalization can be determined by the equation:

Boost (dB) = 20 x $\log_{10}$ [0.01703 x S_Code + 1]

where 0 ≤ S_Code ≤ 127.



Normalized for ωc = (2π) fc = 1
AN and AD are adjusted for unity gain (0 dB) at F = 0.67 fc
Denormalize the frequency by substituting S → (S/2π fc)
Eq for fc = 2.5 MHz, S = S / [(2π) (2.5 • 10^6)] = S / (1.57080 • 10^7)

$$K = 1.31703\left(10^{\frac{Boost(dB)}{20}} - 1\right)$$

FIGURE 1: Normalized Transfer Function of the SSI 32F8130/8131

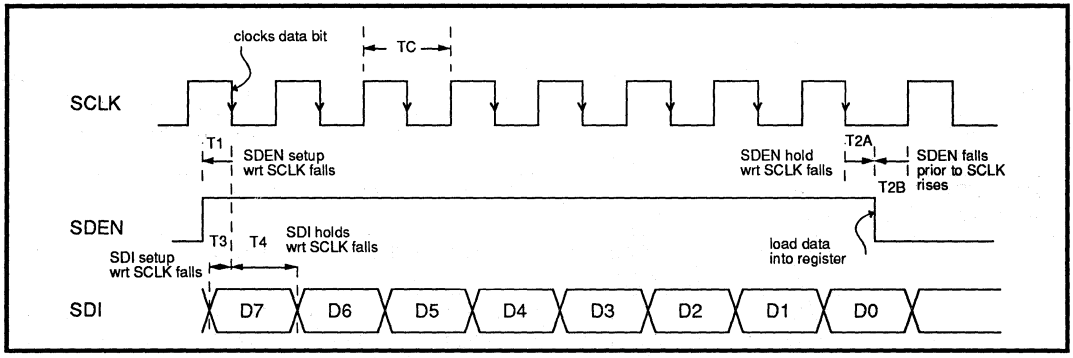


FIGURE 2: Serial Port Timing Relationship

Note:
The serial data enable function of the SSI 32F8130 and that of the SSI 32F8131 are of opposite polarity.

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TABLE 1: Data Packet Fields

	ADDRESS BITS				USAGE	DATA BITS			
	D7	D6	D5	D4		D3	D2	D1	D0
R0	X	0	0	0	S - MSB REGISTER	X	S6	S5	S4
R1	X	0	0	1	S - LSB REGISTER	S3	S2	S1	S0
R2	X	0	1	0	F - MSB REGISTER	X	F6	F5	F4
R3	X	0	1	1	F - LSB REGISTER	F3	F2	F1	F0

X = Don't care bit.

PIN DESCRIPTION

NAME	DESCRIPTION
VIN+, VIN–	DIFFERENTIAL FILTER INPUTS. The input signals must be AC coupled to these pins.
VO_NORM+, VO_NORM–	DIFFERENTIAL NORMAL OUTPUTS. The output signals must be AC coupled to the load.
VO_DIFF+ VO_DIFF–	DIFFERENTIAL DIFFERENTIATED OUTPUTS. These outputs should be AC coupled to the load.
PWR_ON	POWER ON. A TTL high logic level enables the chip. A low level or open circuit puts the chip into a low power state.
SDEN (8130) $\overline{\text{SDEN}}$ (8131)	SERIAL DATA ENABLE. An active level allows SCLK to clock data into the shift register via the SDI input. An inactive level latches the register data and issues the information to the appropriate circuitry. Active level for SSI 32F8130 is HIGH, for SSI 32F8131 is LOW.
SCLK	SERIAL CLOCK. Negative edge triggered clock input for serial register.
SDI	SERIAL DATA INPUT.
VCA	ANALOG +5 VOLT SUPPLY.
VCD	DIGITAL +5 VOLT SUPPLY.
AGND	ANALOG GROUND.
DGND1 DGND2	DIGITAL GROUND.
VFP	CUTOFF FREQUENCY PROGRAMMING REFERENCE. A resistor of 8.25 kΩ should be connected between this pin and AGND.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may permanently damage the device.

PARAMETER	RATINGS
Storage Temperature	-65 to +150°C
Junction Operating Temperature, Tj	+130°C
Supply Voltage, VCC	-0.5 to 7V
Voltage Applied to Inputs*	-0.5 to VCCV
T1 Lead Temperature (1/16" from case for 10 seconds)	260°C

* Analog input signals of this magnitude shall not cause any change or degradation in filter performance after signal has returned to normal operating range.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	RATINGS
Supply voltage, VCC	4.50 < VCC < 5.50V
Ambient Temperature	0 < Ta < 70°C
Tj Junction Temperature	0 < Tj < 130°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified recommended operating conditions apply. F_Code = 64, S_Code = 0.

PARAMETER	CONDITIONS		MIN	NOM	MAX	UNIT
Idle Mode Current					1	mA
Isupply				60	70	mA
Power Dissipation	PWR_ON ≤ 0.8V				6	mW
	PWR_ON ≥ 2.0V			303	385	mW
Idle to Active Mode Recovery Time					50	µs
Serial port program to output response time					50	µs
DC Characteristics						
VIH High Level Input Voltage	TTL input		2.0			V
VIL Low Level Input Voltage					0.8	V
IIH High Level Input Current	VIH = 2.7V				20	µA
IIL Low Level Input Current	VIL = 0.4V		-1.5			mA
Filter Characteristics						
fc Filter Cutoff Frequency	12 < F_Code < 127					
	SSI 32F8130		0.20		2.2	MHz
	SSI 32F8131		0.15		1.4	MHz
FCA Filter *fc* Accuracy	over *fc* range		-10		+10	%
Cutoff Resolution	$\text{Resolution} = \frac{\text{Max fc}}{127}$	F8130		20		kHz
		F8131		12		kHz
AO VO_NORM Diff Gain	F = 0.67 *fc*		0.8		1.2	V/V
AD VO_DIFF Diff Gain	F = 0.67*fc*	32F8131	1.0 AO		1.2 AO	V/V
		32F8130	0.9 AO		1.1 AO	V/V
FB Frequency Boost at *fc*	FB(dB) = 20 log [.01703 (S_Code) + 1] 0 ≤ S_Code ≤ 127		0		10	dB
FBA Frequency Boost Accuracy	10 dB nominal		-1.5		+1.5	dB
TGD0 Group Delay Variation Without Boost	0.2 *fc* - *fc*		-2% gdm		+2% gdm	ns
fc = 0.25 - 2.5 MHz gdm = group delay magnitude	*fc* - 1.75 *fc*		-3% gdm		+3% gdm	ns
TGDB Group Delay Variation With Boost	0.2 *fc* - *fc*		-2% gdm		+2% gdm	ns
	fc - 1.75 *fc*		-3% gdm		+3% gdm	ns
Boost Resolution			0.25			dB
VOF_N Filter Output Dynamic Range	THD = 1% max, Normal Output		1			Vpp

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ELECTRICAL CHARACTERISTICS (continued)
Unless otherwise specified recommended operating conditions apply. F_Code = 64, S_Code = 0.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Filter Characteristics (continued)					
VOF_D Filter Output Dynamic Range	THD = 1% max, Differentiated Output	1			Vpp
RIN Filter Diff Input Resistance		3.0	4.0	5.0	kΩ
CIN Filter Input Capacitance			3.0		pF
EOUT Output Noise Voltage (VO_NORM)	BW = 100 MHz, 50Ω input, fc = Max fc, 0 dB Boost		1.2	1.9	mVRms
	BW = 100 MHz, 50Ω input, fc = Max fc, 10 dB Boost		1.4	2.0	mVRms
EOUT Output Noise Voltage (VO_DIFF)	BW = 100 MHz, 50Ω input, fc = Max fc, 0 dB Boost		2.1	2.7	mVRms
	BW = 100 MHz, 50Ω input, fc = Max fc, 10 dB Boost		2.5	3.4	mVRms
IO– Filter Output Sink Current		1.0			mA
IO+ Filter Output Source Current		3.0			mA
RO Filter Output Resistance (Single ended)	Output source current, IO+ = 1 mA		50	70	Ω
T1 SDEN Set-up WRT SCLK Falls		10		TC/2-10	ns
T2A SDEN Hold WRT SCLK Falls		10		TC/4	ns
T2B SDEN Falls (rises for 8131) prior to SCLK rises		25			ns
T3 SDI Set-up WRT SCLK Falls		25			ns
T4 SDI Hold WRT SCLK Falls		25			ns
SCLK Period, TC		100			ns
Power Supply Rejection Ratio VO_NORM	100 mVpp from 10 kHz to 10 MHz on VCA, VCD	30	40		dB
Power Supply Rejection Ratio VO_DIFF		20	30		dB
Common Mode Rejection Ratio VO_NORM	Vin = 0VDC + 10 mVpp from 10 kHz to 10 MHz	30	40		dB
Common Mode Rejection Ratio VO_DIFF		20	30		dB
Bias: VO_NORM±	VCC = 5V	2.40	2.75	3.10	V
Vin±		2.20	2.35	2.80	V
VO_DIFF±		2.40	2.75	3.10	V
Normal Output Offset Variation	F_Code switched from 12-127	-200		200	mV
Differentiated Output Offset Variation	F_Code switched from 12-127	-200		200	mV

TABLE 1: Calculations

Typical change in f-3 dB point with boost

Boost (dB)	Gain@fc (dB)	Gain@ peak (dB)	$f$peak/fc	f-3dB/fc	K
0	-3	0.00	no peak	1.00	0
1	-2	0.00	no peak	1.21	0.16
2	-1	0.00	no peak	1.51	0.34
3	0	0.15	0.70	1.80	0.54
4	1	0.99	1.05	2.04	0.77
5	2	2.15	1.23	2.20	1.03
6	3	3.41	1.33	2.33	1.31
7	4	4.68	1.38	2.43	1.63
8	5	5.94	1.43	2.51	1.97
9	6	7.18	1.46	2.59	2.40
10	7	8.40	1.48	2.66	2.85

Notes: 1. fc is the original programmed cutoff frequency with no boost

2. f-3 dB is the new -3 dB value with boost implemented

3. $f$peak is the frequency where the amplitude reaches its maximum value with boost implemented

i.e., fc = 1 MHz when boost = 0 dB

if boost is programmed to 5 dB then f-3 dB = 2.20 MHz

$f$peak = 1.23 MHz

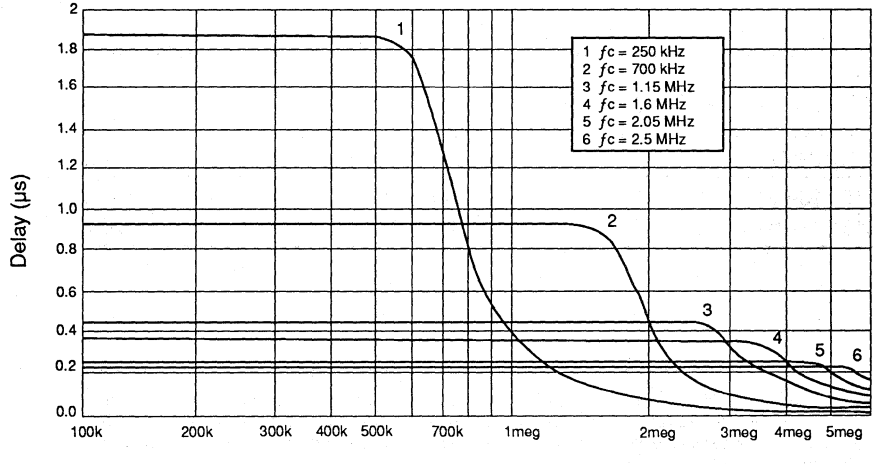


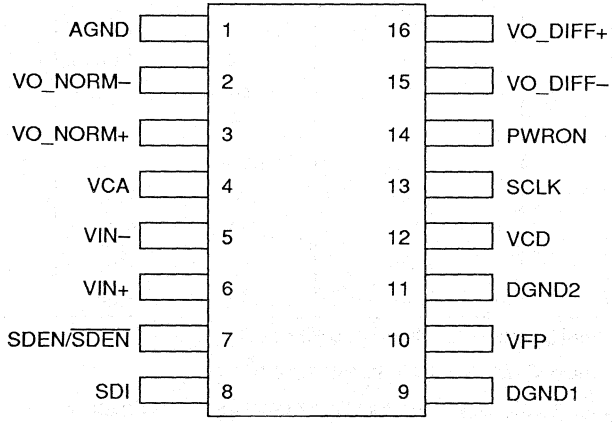
FIGURE 3: Typical Normal/Differentiated Output Group Delay Response

SSI 32F8130/8131
Low-Power Programmable Electronic Filter

PACKAGE PIN DESIGNATIONS
(Top View)

THERMAL CHARACTERISTICS: θjA

16-Lead SOL	100° C/W



16-Lead SOL

SSI 32F8130: Lead 7 = SDEN
SSI 32F8131: Lead 7 = $\overline{SDEN}$

CAUTION: Use handling procedures necessary for a static sensitive component.

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32F8130 16-Lead SOL	32F8130-CL	32F8130-CL
SSI 32F8131 16-Lead SOL	32F8131-CL	32F8131-CL

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914

silicon systems®
A TDK Group Company

SSI 32F8144
Programmable Electronic Filter

January 1994

DESCRIPTION

This custom integrated circuit incorporates a pulse equalizer of variable equalization and variable bandwidth with a transfer function of a 2 zero/7 pole linear phase filter, as well as variable gain stages controlled by DACs. Equalization, gain and bandwidth changes are user-programmable via three serial lines to a microprocessor. The equalizer is totally contained and calibrating. It is realized in a high speed fully differential mode. A seven pole linear phase equiripple ± 0.05 degree filter forms the low-pass function. The cutoff frequency of the low-pass section is programmed via a 7-bit serial shift register and can be programmed from 7 to 27 MHz. Pulse slimming equalization uses two programmable magnitude, opposite sign zeroes on the real axis. Pulse slimming boost is from 0 to 9.5 dB at the filter cutoff frequency using a 7 bit serial shift register. Gain can be programmed from 10 V/V to 100 V/V for normal outputs and from 10 V/V to 50 V/V for differentiated outputs.

FEATURES

- **Programmable filter cutoff frequency (7 MHz ≤ *fc* ≤ 27 MHz) with no external components**
- **± 10% cutoff frequency accuracy**
- **Programmable pulse slimming equalization (0 to 9.5 dB boost at the filter cutoff frequency)**
- **Matched delay normal and differentiated low-pass outputs**
- **Differential filter inputs and outputs**
- **Device idle mode (45 mW nom.)**
- **+5V only operation**
- **Supports constant density recording**
- **Input stage gain control with DAC**
- **Relative gain between normal and differentiated outputs controlled with serial port**

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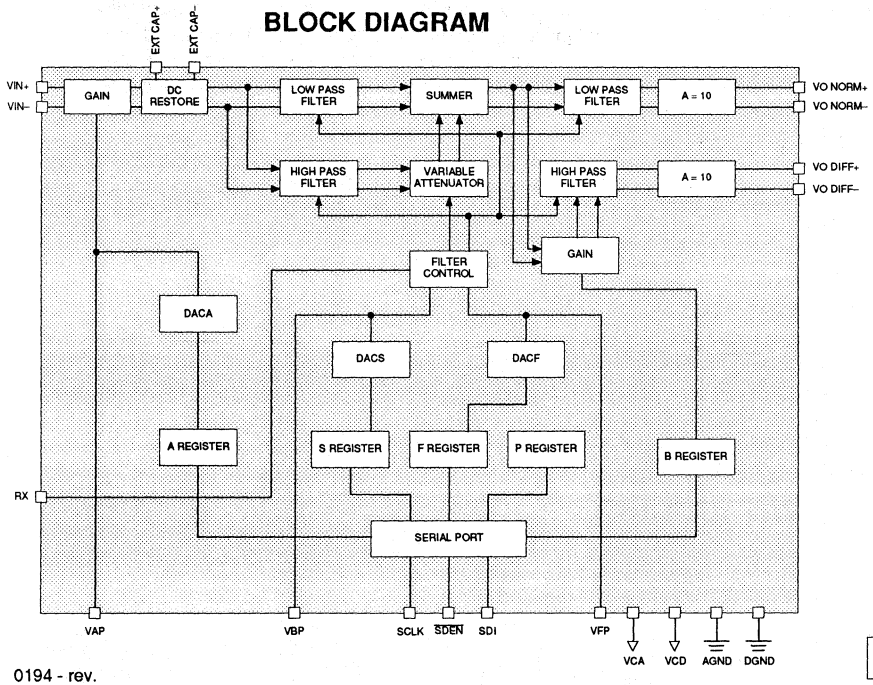
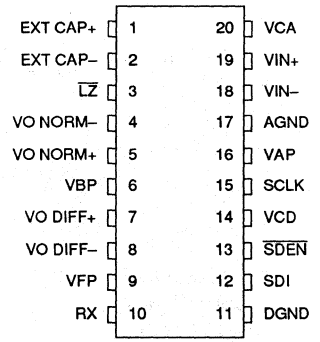
BLOCK DIAGRAM



PIN DIAGRAM



20-lead SOL

CAUTION: Use handling procedures necessary for a static sensitive component.

0194 - rev.

SSI 32F8144
Programmable
Electronic Filter

FUNCTIONAL DESCRIPTION

The SSI 32F8144, a high performance programmable electronic filter, provides a low pass equiripple type seven pole filter with matched normal and differentiated outputs with variable gain using DACs.

The SSI 32F8144 has seven control registers: A, B, S1, S2, F1, F2 and P registers. Register A contains four bits, B is three bits, and P is one bit. S1, S2, F1, and F2 contain seven bits. Register A controls the gain of the input stage and register B controls the gain between the normal and differentiated outputs. Since the F, S registers contain 7 bits, they require two data packets which must be loaded sequentially. S1-2 registers are for high frequency boost. F1-2 registers are for cutoff frequency control. The P register is for power down command. The structure and command of each register are described as follows.

Data is loaded serially with MSB first. Each data packet contains 8 bits. The first four bits (D7 - D4) are designated as address bits with D7 always a "don't care." The last four bits (D3 - D0) are the data bits (see Table 1).

The registers are loaded by using the serial port through the SDI, $\overline{\text{SDEN}}$ and SCLK pins. The SDI pin is the serial bit input. The $\overline{\text{SDEN}}$ pin is the control register enable. The SCLK is the control register clock. The packet is transmitted MSB (D7) first.

GAIN PROGRAMMING

The input gain stage is programmed with register A (Register 4, R4). The A_Code programs this gain as follows:

$$Av(V/V) = 10 \cdot \frac{A\_Code}{15}$$

$$1 \le A\_Code \le 15$$

This input gain stage is DC coupled to the filter core through DC restore circuitry. A large capacitor (1 µF) is placed between pins EXT_CAP+ and EXT_CAP- to null the input offset to the filter. Register B (Register 5, R5) controls the relative gain between the normal and differentiated outputs. There are three discrete options which are listed as follows:

AN/AD = 1.0 B_Code = 3 (B2 = 0, B1 = 1, B0 = 1)
A_Code = 1

AN/AD = 1.5 B_Code = 5 (B2 = 1, B1 = 0, B0 = 1)
A_Code = 7

AN/AD = 2.0 B_Code = 6 (B2 = 1, B1 = 1, B0 = 0)
A_Code = 15 (B3 is a "don't care")

CUTOFF FREQUENCY PROGRAMMING

The filter cutoff frequency can be set from 7 to 27 MHz. The 7-bit F_Code programs the cutoff frequency as follows:

$$fc(MHz) = 27 \cdot \frac{F\_Code}{127} \qquad 33 \le F\_Code \le 127$$

SLIMMER HIGH FREQUENCY BOOST PROGRAMMING

The amplitude of the input signal at frequencies near the cutoff frequency can be increased using this feature. By controlling the DACS output, the boost can be determined. The amount of boost at the cutoff frequency is related to the DACS output by the following formula:

BOOST (dB) = 20 • log [0.01563(S_Code) +1].

The 7-bit S_Code is loaded into S1 and S2 registers (registers 0 and 1 - R0, R1).

POWER-DOWN CONTROL

The D0 bit of the P register (register 7, R7) determies the power up/down state of the SSI 32F8144. Upon initial power up, the D0 bit of the P register should be initialized to "1" for normal operation. D3 - D1 are "don't care."

By programming D0 to "0," the SSI 32F8144 is switched into a power-down state, dissipating minimum idle power. The filter is switched off. The serial port remains active awaiting the next command.

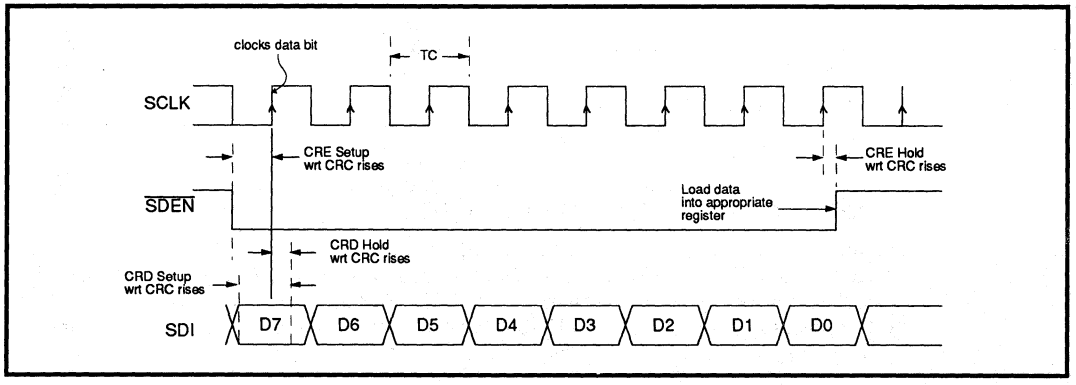


FIGURE 1: Serial Port Timing Relationship

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TABLE 1: Control Register Assignment

ADDRESS BITS					USAGE	DATA BITS			
	D7	D6	D5	D4		D3	D2	D1	D0
R0	X	0	0	0	S1 REGISTER	X	S6	S5	S4
R1	X	0	0	1	S2 REGISTER	S3	S2	S1	S0
R2	X	0	1	0	F1 REGISTER	X	F6	F5	F4
R3	X	0	1	1	F2 REGISTER	F3	F2	F1	F0
R4	X	1	0	0	A REGISTER	A3	A2	A1	A0
R5	X	1	0	1	B REGISTER	X	B2	B1	B0
R7	X	1	1	1	P REGISTER	X	X	X	P0

X = Don't Care
S = Boost (Slimming) Control
F = Frequency (Bandwidth) Control
A = Gain Setting (0-10)
B = Gain of VO_DIFF relative to the gain of VO_NORM
P = Sleep Mode Control (P0 = 1, On Mode; P0 = 0, Sleep Mode)

SDI is the serial data input for an 8-bit control shift register. The data packet is transmitted Most Significant Bit (D7) first. The first four bits are the register address, the last four are the data bits. Registers larger than four bits must be loaded with two 8-bit data packets. These packets should be loaded sequentially.

PIN DESCRIPTION

NAME	DESCRIPTION
VIN+, VIN-	DIFFERENTIAL SIGNAL INPUTS
VO_NORM+, VO_NORM-	DIFFERENTIAL NORMAL OUTPUTS
VO_DIFF+ VO_DIFF-	DIFFERENTIAL DIFFERENTIATED OUTPUTS
$\overline{SDEN}$	CONTROL REGISTER ENABLE. A logic LOW level allows CONTROL REGISTER CLOCK to clock data into the control register via the CONTROL REGISTER DATA input. A logic HIGH level latches the register data and issues the information to the appropriate circuitry. This is a TTL input.
SCLK	CONTROL REGISTER CLOCK. Positive edge triggered clock input for serial register. This is a TTL input.
SDI	CONTROL REGISTER DATA. This is a TTL input (see Figure 1).
RX	CURRENT SET RESISTOR. This external resistor to ground provides a reference current. (RX = 5 kΩ ±1%) A 1000 pF capacitor must be connected in parallel with Rx.
VCA	ANALOG +5V SUPPLY.
VCD	DIGITAL +5V SUPPLY.
AGND	ANALOG GROUND.
DGND	DIGITAL GROUND.
VAP	ANALOG TO DIGITAL TEST VOLTAGE. This is an analog voltage that is proportional to the setting on the digital output on the A/D convertor. This is a test pin related to the variable gain.
VBP	BOOST PROGRAMMING VOLTAGE. A voltage that is related to the boost. A test pin.
VFP	CUTOFF FREQUENCY PROGRAMMING VOLTAGE. A voltage that is related to the cutoff frequency. A test pin.
EXT CAP+ EXT CAP-	EXTERNAL CAPACITOR. These pins are available for an external capacitor which is used in a feedback network to null the input offset. $C_{EXT} \geq 0.47\ \mu F$, 1.0 μF nominal.
$\overline{LZ}$	LOW IMPEDANCE. This is a control signal which causes the input impedance of the filter to be low when this pin is low. The impedance is high if the pin is open or in the high state. This is a TTL input.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may damage the device.

PARAMETER	RATINGS
Storage Temperature	-65 to +150°C
Junction Operating Temperature, Tj	+130°C
Supply Voltage, VCC	-0.5 to 7V
Voltage Applied to Inputs*	-0.5 to VCCV
Maximum Power Dissipation, fc = 27 MHz, Vcc = 5.5V	.55W
T1 Lead Temperature (1/16" from case for 10 seconds)	260°C

* Analog input signals of this magnitude shall not cause any change or degradation in filter performance after signal has returned to normal operating range.

5

RECOMMENDED OPERATING CONDITIONS

Supply voltage, VCC	4.50 < VCC < 5.50	V
Ambient Temperature	0 < Ta < 70	°C
Tj Junction Temperature	0 < Tj < 130	°C

ELECTRICAL CHARACTERISTICS

Unless otherwise specified recommended operating conditions apply.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Idle Mode Current	P0 = "0"		11	15	mA
Supply Current	Vcc = 5.5V		85	100	mA
PD Power Dissipation	P0 = "0"		45	71.5	mW
	P0 = "1"		400	550	mW
Idle to Active Mode Recovery Time				50	µs
Serial port program to output response time				50	µs
DC Characteristics					
VIH High Level Input Voltage	TTL input	2.0			V
VIL Low Level Input Voltage				0.8	V
IIH High Level Input Current	VIH = 2.7V			20	µA
IIL Low Level Input Current	VIL = 0.4V			–1.5	mA
Filter Characteristics					
fc Filter Cutoff Frequency	33 ≤ F_Code ≤ 127	7		27	MHz

ELECTRICAL CHARACTERISTICS (continued)
Unless otherwise specified recommended operating conditions apply.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
FCA	Filter *fc* Accuracy	Over full *fc* range, 33 ≤ F_Code ≤ 127	-10		10	%
AO	VO_NORM Diff Gain (Note)	F = 0.67 *fc*	10		100	V/V
AD	VO_DIFF Diff Gain (Note)	F = 0.67 *fc*, set with serial port	10		50	V/V
VO_NORM Gain Tolerance		A_O = 100	-15		15	%
VO_DIFF Gain Tolerance		A_D = 50	-15		15	%
FB	Frequency Boost at *fc*	FB(dB) = 20 log [.01563 (S_Code) +1]	0		9.5	dB
FBA	Frequency Boost Accuracy	0 to 9.5 dB	–1.25		+1.25	dB
TGD0	Group Delay Variation Without Boost	0.2 *fc* - *fc*	–2% gdm		+2% gdm	ns
	gdm = group delay magnitude	*fc* - 1.75 *fc*	–3% gdm		+3% gdm	ns
TGDB	Group Delay Variation With Boost	0.2 *fc* - *fc*	–2% gdm		+2% gdm	ns
		fc - 1.75 *fc*	–3% gdm		+3% gdm	ns
VOF	Filter Output Dynamic Range	Vo_NORM, T_{HD} = 1.5%	1			Vpp
		Vo_DIFF, T_{HD} = 2.0%	1			Vpp
		Vo_NORM, T_{HD} = 2.0%	1.5			Vpp
		Vo_DIFF, T_{HD} = 3.0%	1.5			Vpp
RIN	Filter Diff Input Resistance		3.0	3.5	4.0	kΩ
CIN	Filter Input Capacitance				7	pF
EOUT	Output Noise Voltage (VO_NORM)	BW = 100 MHz, 0 dB Boost, 50Ω input		2.5	4.0	mV rms
		fc = 27 MHz 9.5 dB Boost		3.7	10	mV rms
EOUT	Output Noise Voltage (VO_DIFF)	BW = 100 MHz, 0 dB Boost, 50Ω input		4.4	6	mV rms
		fc = 27 MHz 9.5 dB Boost		7.8	14	mV rms
IO–	Filter Output Sink Current		1.0			mA
IO+	Filter Output Source Current		3.0			mA
RO	Filter Output Resistance (Single ended)	IO+ = 1 mA		30	50	Ω
$\overline{SCLK}$ Period, TC			100			ns
$\overline{SDEN}$ Set-up WRT $\overline{SCLK}$ Rising Edge			10		25	ns
$\overline{SDEN}$ Hold WRT $\overline{SCLK}$ Rising Edge			5		TC/2-10	ns

Note: The overall gain of VO_DIFF with respect to VIN is 10 to 50 V/V. Additionally, the gain of VO_NORM with respect to VO_DIFF will be adjustable and have gain values of 1.0, 1.5 and 2.0.

ELECTRICAL CHARACTERISTICS (continued)
Unless otherwise specified recommended operating conditions apply.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
$\overline{SDEN}$ Rises Prior to $\overline{SCLK}$ Falls		15			ns
SDI Set-up WRT $\overline{SCLK}$ Rising Edge		15			ns
SDI Hold WRT $\overline{SCLK}$ Rising Edge		15			ns
Power Supply Rejection Ratio	100 mVpp in VCA, VCD from 100 kHz to 10 MHz	45	70		dB
Common Mode Rejection Ratio	VIN = 0 VDC + 100 mVpp from 100 kHz to 10 MHz	40	65		dB
DC Bias: VO_NORM+, VO_NORM- VO_DIFF+, VO_DIFF-	VCC = 5V, single ended	2.05	2.55	3.05	V
Vin+, Vin-		2.5	3.0	3.5	V
Delay mismatch normal and differentiated outputs				1	ns

5

TABLE 2: Calculations

Typical change in f-3 dB point with boost

Boost (dB)	Gain@fc (dB)	Gain@ peak (dB)	$f$peak/fc	f-3dB/fc	K
0	-3	0.00	no peak	1.00	0
1	-2	0.00	no peak	1.21	0.16
2	-1	0.00	no peak	1.51	0.34
3	0	0.15	0.70	1.80	0.54
4	1	0.99	1.05	2.04	0.77
5	2	2.15	1.23	2.20	1.03
6	3	3.41	1.33	2.33	1.31
7	4	4.68	1.38	2.43	1.63
8	5	5.94	1.43	2.51	1.97
9	6	7.18	1.46	2.59	2.40
10	7	8.40	1.48	2.66	2.85

Notes: 1. fc is the original programmed cutoff frequency with no boost
2. f-3 dB is the new -3 dB value with boost implemented
3. $f$peak is the frequency where the amplitude reaches its maximum value with boost implemented

e.g., fc = 9 MHz when boost = 0 dB
if boost is programmed to 5 dB then f-3 dB = 19.8 MHz
$f$peak = 11.07 MHz

SSI 32F8144
Programmable
Electronic Filter

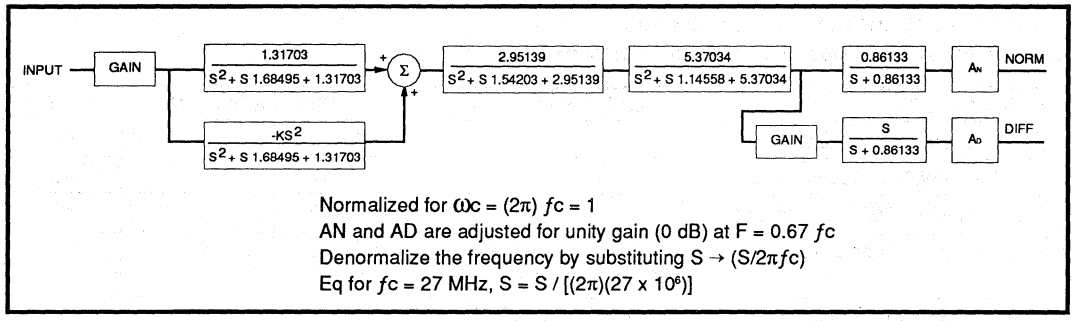


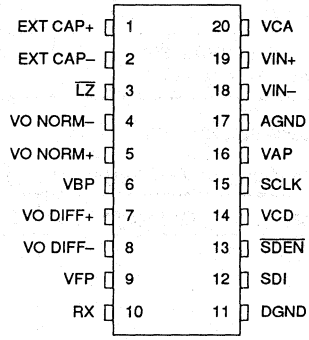
FIGURE 2: 32F8144 Normalized Block Diagram

PACKAGE PIN DESIGNATIONS

(Top View)

THERMAL CHARACTERISTICS: θja

20-lead SOL	95°C/W
20-Lead SOV	125°C/W



20-lead SOL, SOV

CAUTION: Use handling procedures necessary for a static sensitive component.

ORDERING INFORMATION

PART DESCRIPTION		ORDERING NUMBER	PACKAGE MARK
SSI 32F8144	20-Lead SOL (300 mil)	32F8144 - CL	32F8144 - CL
SSI 32F8144	20-Lead SOV (220mil)	32F8144 - CV	32F8144 - CV

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914

Section 6

READ CHANNEL COMBINATION DEVICE

SSI 32P4340/4341
Read Channel Devices

silicon systems®
A TDK Group Company

Advance Information

December 1993

DESCRIPTION

The 32P4340/4341 device is a high performance BiCMOS single chip read channel IC that contains all the functions needed to implement a complete zoned recording read channel for hard disk drive systems. Functional blocks include the pulse detector, programmable filter, 4-burst servo capture, time base generator, and data separator with 1,7 RLL ENDEC. Data rates from 14 to 40 Mbit/s can be programmed using an internal DAC whose reference current is set by a single external resistor.

Programmable functions of the 32P4340/4341 device are controlled through a bi-directional serial port and banks of internal registers. This allows zoned recording applications to be supported without changing external component values from zone to zone.

FEATURES

- GENERAL
  - Power supply range (3.0 to 5.5 volts)
  - Programmable 14 to 40 Mbit/s data rate
  - Complete zoned recording support
  - Low power operation (350 mW typical @ 3.3V)
  - Bi-directional serial port for register access
  - Register programmable power management (Sleep mode <1.0W)
  - Small footprint 64-lead TQFP package
- PULSE DETECTOR:
  - Dual rate charge pump for fast transient recovery
  - Low Drift AGC hold circuitry
  - Temperature compensated, exponential control AGC
  - Wide bandwidth, high precision full-wave rectifier
  - Dual mode pulse qualification circuitry
  - CMOS $\overline{\text{RDIO}}$ output for servo timing
  - User selectable internal LOW-Z and fast decay period
  - 0.75 ns max. pulse pairing (sine wave input)
  - Adjustable level decay current (4-bit)
- SERVO CAPTURE
  - 4-burst servo capture (A-B, C-D 32P4340) (A, B, C, D 32P4341)
  - Internal hold capacitors
  - Separate registers for servo fc and V_{TH}
  - Adjustable level decay current (4-bit)
  - Adjustable servo peak detector current
- PROGRAMMABLE FILTER
  - Programmable cutoff frequency of 4.5 to 15 MHz
  - Programmable boost/equalization of 0 to 13 dB
  - Matched normal and differentiated outputs
  - ± 10% fc accuracy
  - ± 30% programmable group delay variation
  - Less than 1% total harmonic distortion
  - No external filter components required
- TIME BASE GENERATOR
  - Better than 1% frequency resolution
  - Up to 60 MHz frequency output
  - Independent M and N divide-by registers
  - VCO center frequency matched to data synchronizer VCO
- DATA SEPARATOR
  - Fast acquisition phase lock loop with zero phase restart technique
  - Integrated 1,7 RLL Encoder/Decoder
  - Programmable decode window symmetry
    - Window shift control ±15% (4-bit)
    - Includes delayed read data and VCO clock monitor points
  - Programmable write precompensation (3-bit)

6

This is an abridged version of the SSI 32P4340/4341 data sheet. For a complete copy contact your local Silicon Systems sales office, or call 1-800-624-8999, ext. 151.

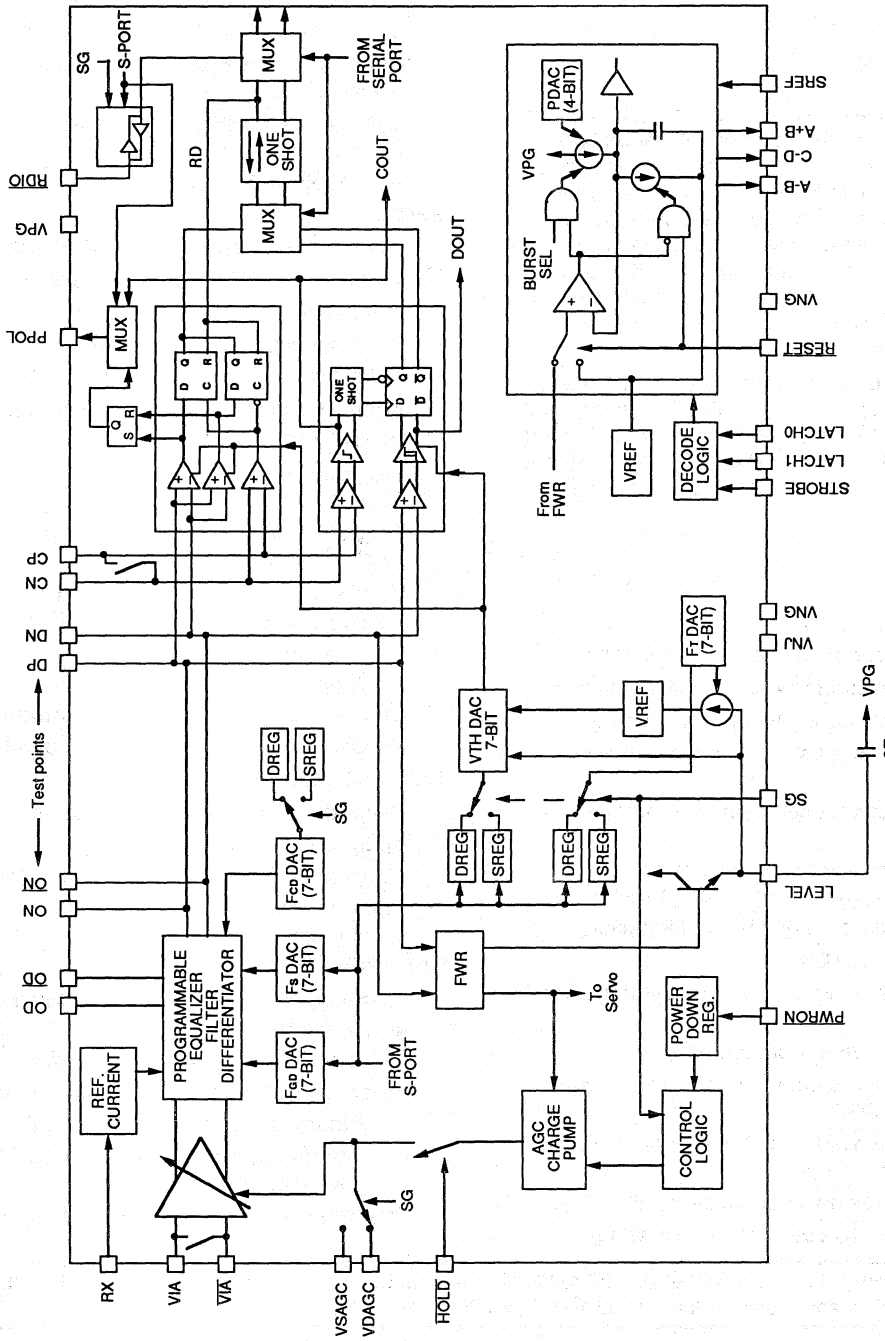


FIGURE 1(a): 32P4340 Front End Block Diagram

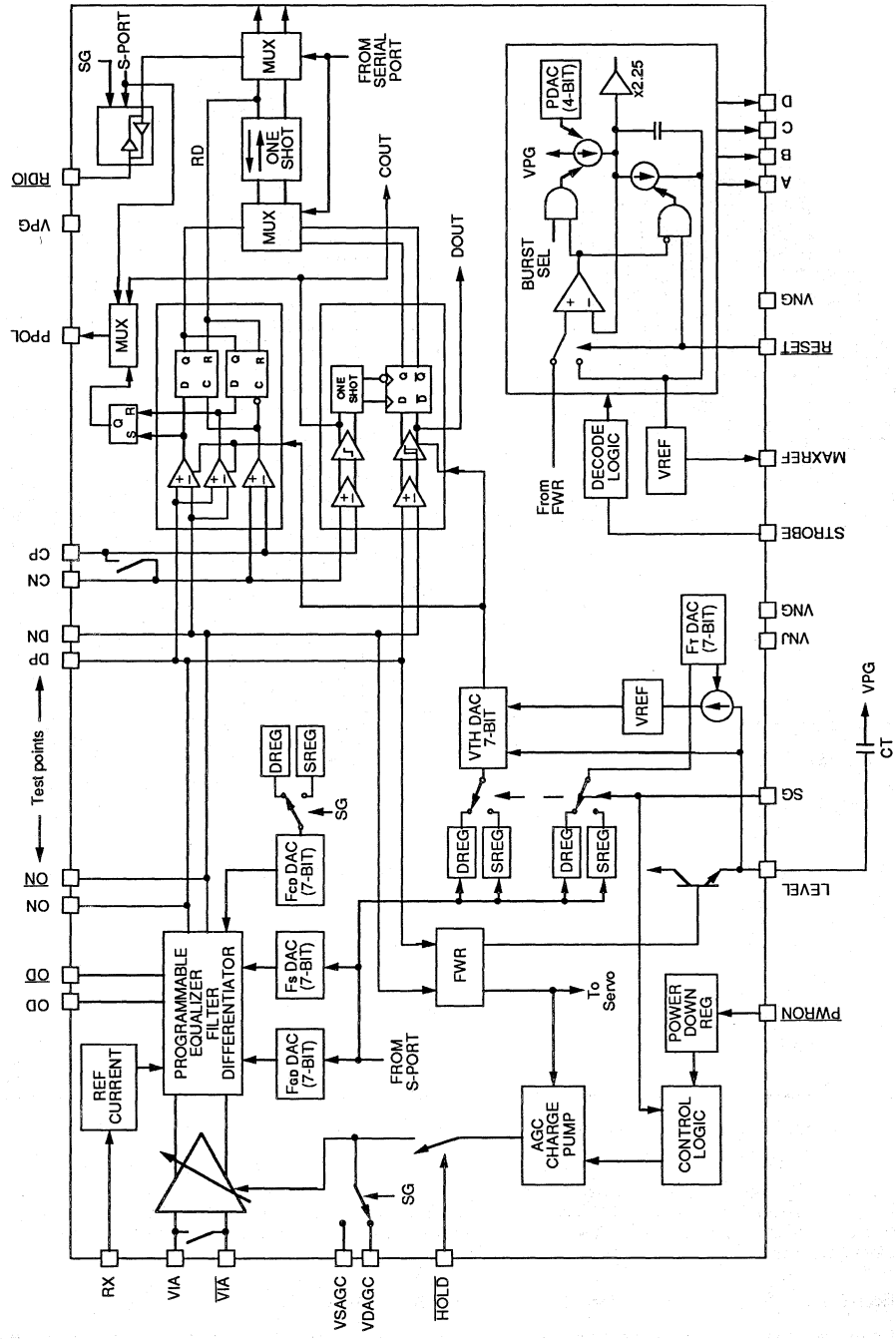


FIGURE 1(b): 32P4341 Front End Block Diagram

6

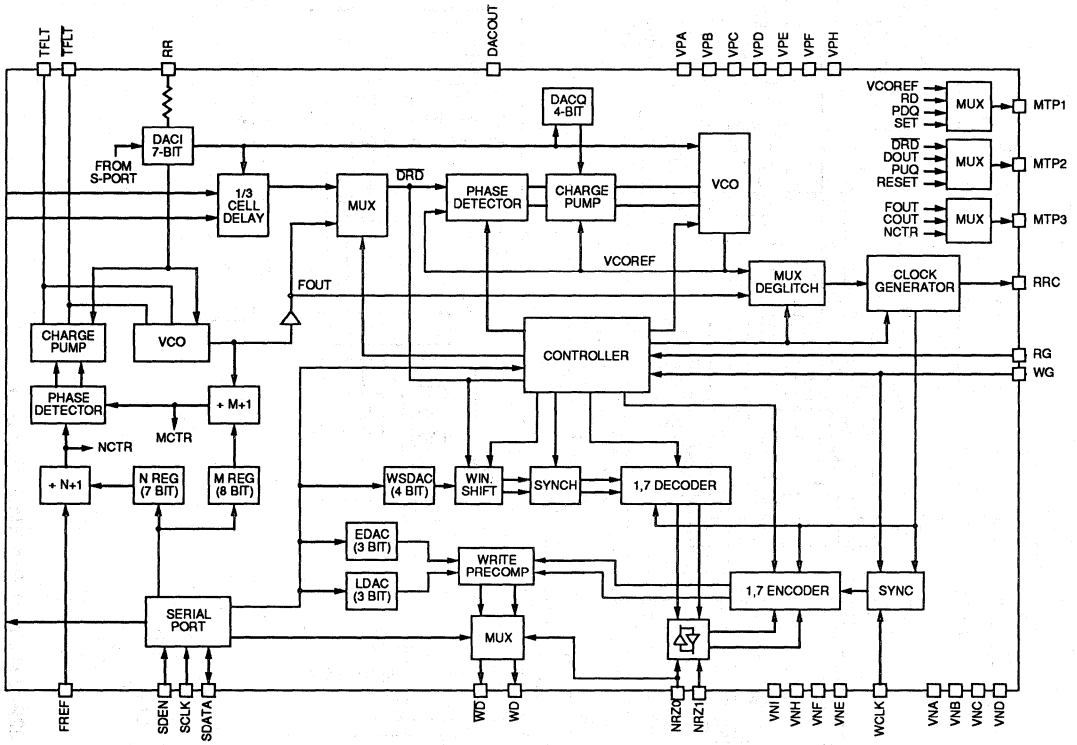


FIGURE 1(c): 32P4340/4341 Back End Block Diagram

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

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silicon systems®
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SSI 32P4742/4742A/4746/4746A

Read Channel with 1,7 ENDEC, 4-burst Servo

Advance Information

December 1993

DESCRIPTION

The SSI 32P4742/4742A/4746/4746A devices are high performance BiCMOS single chip read channel ICs that contain all the functions needed to implement a complete zoned recording read channel for hard disk drive systems. Functional blocks include the pulse detector, programmable filter, 4-burst servo capture, time base generator, and data separator with 1,7 RLL ENDEC. Data rates from 16 to 48 Mbit/s can be programmed using an internal DAC whose reference current is set by a single external resistor. For reduced clocking speeds, the 32P4742/4742A/4746/4746A employs a dual-bit parallel interface to the controller.

Programmable functions of the SSI 32P4742/4742A/4746/4746A devices are controlled through a bi-directional serial port and banks of internal registers. This allows zoned recording applications to be supported without changing external component values from zone to zone.

The SSI 32P4742/4742A/4746/4746A utilize an advanced BiCMOS process technology along/ with advanced circuit design techniques which result in high performance devices with low power consumption.

The 32P4742/4742A provide four servo bursts with A, B, C, and D outputs; the 32P4746/4746A also provide four servo bursts with A-B, C-D, and A+B outputs.

FEATURES

GENERAL:

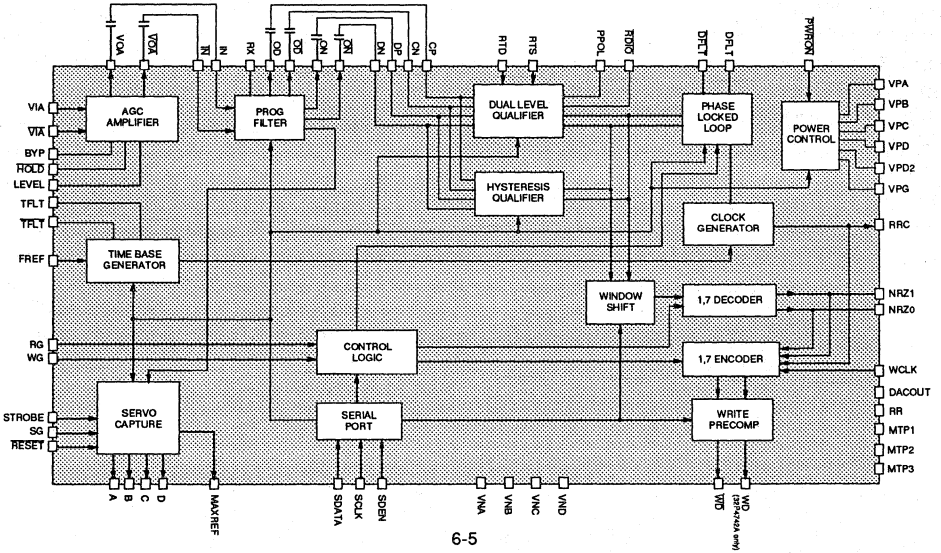
- DAC controlled programmable data rates from 16 to 48 Mbit/s
- Complete zoned recording application support
- Low power operation < 500 mW typical at 5V
- Bi-directional serial port for register access
- Register programmable power management (Sleep mode <0.5 mA)
- Power supply range (4.5 to 5.5 volts)
- Small footprint 64-lead TQFP package

PULSE DETECTOR:

- Fast attack/Decay modes for rapid AGC recovery
- Dual rate charge pump for fast transient recovery
- Low Drift AGC hold circuitry
- Temperature compensated, exponential control AGC
- Wide bandwidth, high precision full-wave rectifier
- Dual mode pulse qualification circuitry (user selectable)
- CMOS $\overline{\text{RDIO}}$ signal output for servo timing support
- Internal LOW-Z and fast decay timing
- 0.2 ns max. pulse pairing at 48 Mbit/s using a 18 MHz sine wave input

(continued)

BLOCK DIAGRAM



FEATURES (continued)

SERVO CAPTURE:

- 4-burst servo capture with A, B, C, D outputs (32P4742/4742A)
- 4-burst servo capture with A-B, C-D and A+B outputs (32P4746/4746A)
- Internal hold capacitors
- Separate registers for fc and V_{TH} during Servo mode
- 4-bit DAC for AGC level control (0.75 to 1.0 Vpp)

PROGRAMMABLE FILTER:

- Programmable cutoff frequency of 6 to 18 MHz
- Programmable boost/equalization of 0 to 13 dB
- Matched normal and differentiated outputs
- ± 10% fc accuracy
- ± 2% maximum group delay variation to fc
- Less than 1.5% total harmonic distortion
- Low-Z input switch
- No external filter components required

TIME BASE GENERATOR:

- Better than 1% frequency resolution
- Up to 75 MHz frequency output
- Independent M and N divide-by registers
- VCO center frequency matched to data synchronizer VCO

DATA SEPARATOR:

- Fast acquisition phase lock loop with zero phase restart technique
- Dual-bit NRZ interface
- Integrated 1,7 RLL Encoder/Decoder
- Programmable decode window symmetry control via serial port
  - Window shift control TBD (4-bit)
  - Includes delayed read data and VCO clock monitor points
- Programmable early/late write precomp (3-Bits each)
- TTL write data output - 32P4742/4746
- Differential PECL write data output - 32P4742A/4746A
- Hard sector operation
- VCO and Synchronized Read Data test points

FUNCTIONAL DESCRIPTION

The SSI 32P4742/4742A implement a high performance complete read channel, including pulse detector, 4-burst servo capture, programmable active filter, time base generator, and data separator with 1,7 RLL ENDEC, at data rates up to 48 Mbit/s.

PULSE DETECTOR CIRCUIT DESCRIPTION

The pulse detector, in conjunction with the programmable filter, provides all the data processing functions necessary for detection and qualification of encoded read signals. The signal processing circuits include a wide band variable gain amplifier; a wide bandwidth, high precision fullwave rectifier; and a dual rate charge pump. The entire signal path is fully-differential to minimize external noise pick up.

AGC CIRCUIT

The gain of the AGC amplifier is controlled by the voltage (V_{BYP}) stored on the BYP hold capacitor (C_{BYP}), Figure 1. A dual rate charge pump drives C_{BYP} with currents that depend on the instantaneous differential voltage at the DP/DN pins. Attack currents lower V_{BYP} which reduces the amplifier gain, while decay currents increase V_{BYP} which increases the amplifier gain. When the signal at DP/DN is greater than 100% of the programmed AGC level, the nominal attack current of 0.17 mA is used to reduce the amplifier gain. If the signal is greater than 125% of the programmed AGC level, a fast attack current of eight (8) times nominal is used to reduce the gain. This dual rate approach allows AGC gain to be quickly decreased when it is too high yet minimizes distortion when the proper AGC level has been acquired.

A constant decay current of 4 µA increases the amplifier gain when the signal at DP/DN is less than the programmed AGC level. The large ratio (0.17 mA:4 µA) of the nominal attack and nominal decay currents enables the AGC loop to respond to the peak amplitudes of the incoming read signal rather than the average value. A Fast Decay Current mode is provided by setting bit 7 of the CAR to "0," to allow the AGC gain to be rapidly increased to reduce the recovery time between mode switches.

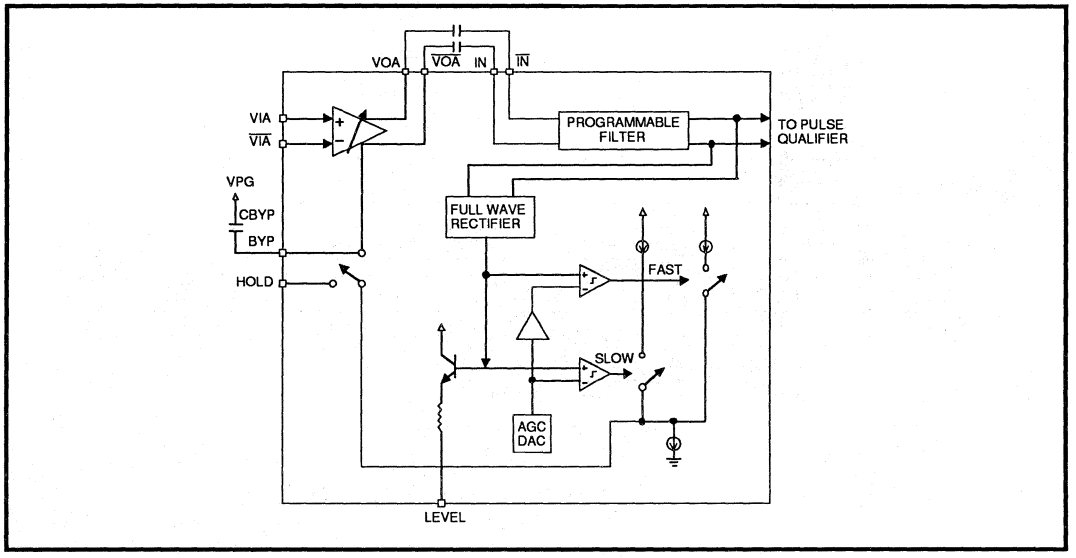


FIGURE 1: AGC Block

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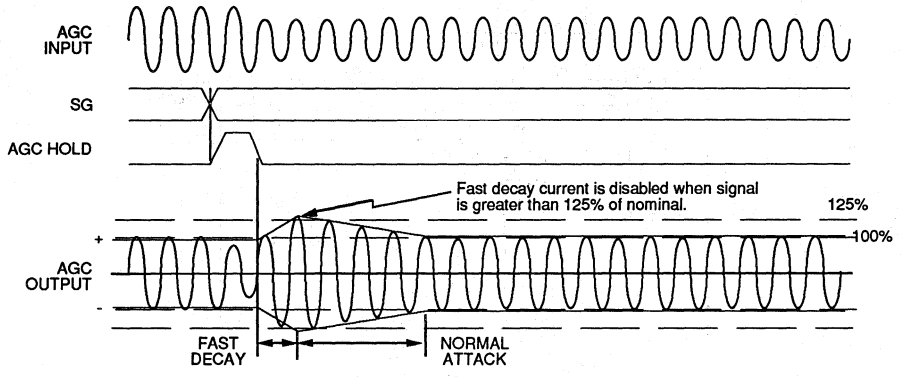
AGC MODE CONTROL

When write gate (WG) is driven high, the dual rate charge pump is disabled causing the AGC amplifier gain to be held constant. The input impedance of both the AGC amplifier and the programmable filter is reduced. When the WG pin transitions from high to low, the Low-Z mode is activated. In this mode, the input impedance at both the AGC amplifier and the programmable filter remain low to allow for quick recovery of the AC coupling capacitors. Directly following the Low-Z mode is the Fast Decay mode which allows rapid acquisition of the proper AGC level. In Fast Decay mode, an internal FET is switched on to drive a high current into the BYP pin. The current remains active until the signal at DP/DN is above 125% of the nominal amplitude, or until an internal timer expires. After the fast decay current is disabled, the normal AGC sequence is enabled. The duration of both the Low-Z and fast Decay modes can be set to either 1 µs or 2 µs by programming bit D7 in the N Counter register. A fast decay sequence is also initiated on the edges of servo gate (SG). Each edge of SG triggers a 400 ns (typ.) AGC hold period to allow the filter to settle. The fast decay current is enabled at the end of the HOLD period. When the pulse detector is powered-down, V_{BYP} will be held constant subject to leakage currents only. Upon power-up, the Low-Z/fast decay sequence is executed to rapidly recover from any transients or drift which may have occurred on the BYP hold capacitor, Figure 2.

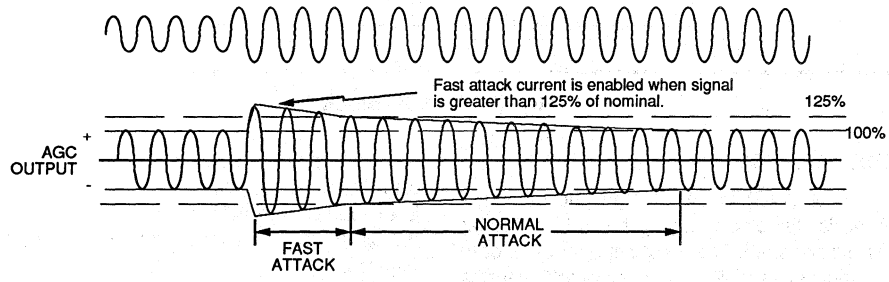
External control for enabling the dual rate charge pump is also provided. Driving the $\overline{HOLD}$ pin low forces the dual rate charge pump output current to zero. In this mode, V_{BYP} will be held constant subject only to leakage currents.

$\overline{RDIO}$ Output Pin

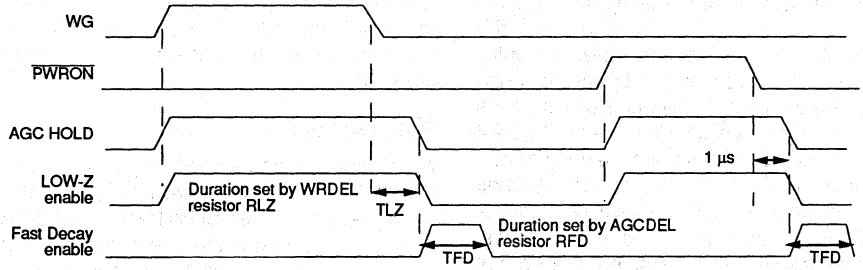
A TTL compatible inverted Read Data I/O ($\overline{RDIO}$) is provided to monitor the pulse detector output. This pin will be held high when SG is low and either RG or WG are high to reduce noise and accompanying jitter during Read or Write modes. Its falling edge indicates the occurrence of valid data pulse.



Servo mode gain recovery



High gain to low gain recovery



Low-Z timing

FIGURE 2: AGC Timing Diagrams

FUNCTIONAL DESCRIPTION (continued)

QUALIFIER SELECTION

The 32P4742/4742A provides both hysteresis and dual comparator pulse qualification circuits that may be independently selected for Read mode and Servo mode operation, Figure 3. For Read mode operation the pulse qualifier method is selected by setting the MSB in the data threshold control register (DTCR). The lower 7 bits of the DTCR also set the hysteresis level of the comparators for Read mode. For Servo mode operation the pulse qualifier method is selected by setting the MSB in the servo threshold control register (STCR). The lower 7 bits of the STCR set the hysteresis level of the comparators for Servo mode.

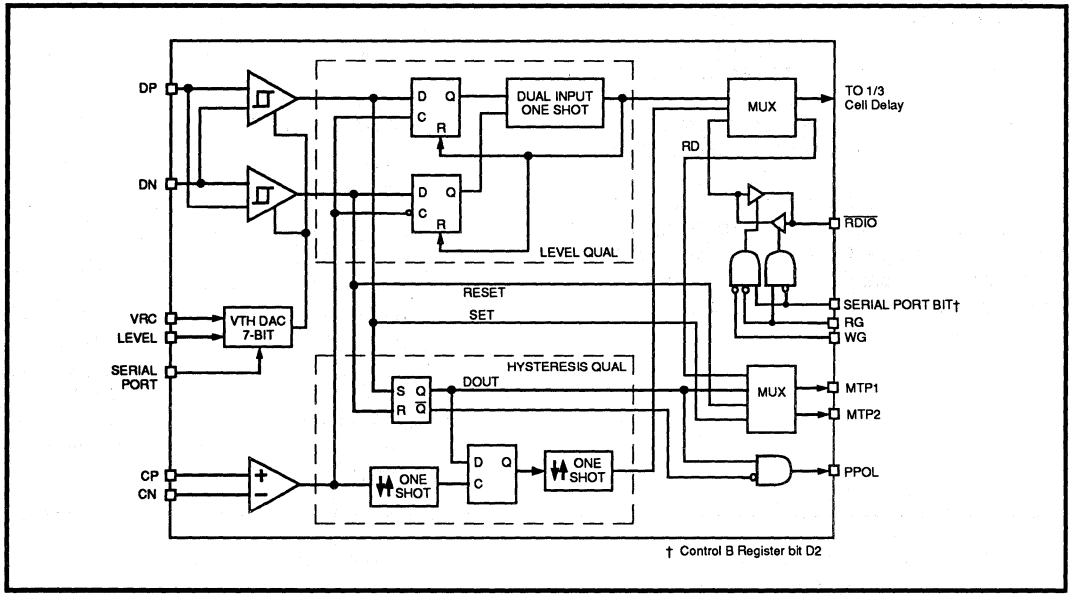


FIGURE 3: Pulse Qualification

FUNCTIONAL DESCRIPTION (continued)

DUAL COMPARATOR QUALIFICATION

When in Dual Comparator mode, independent positive and negative threshold qualification comparators are used to suppress the error propagation of a positive and negative threshold hysteresis comparator. However a slight amount of hysteresis is included to increase the comparator output time when a signal that just exceeds the threshold level is detected. This eases the timing with respect to the zero crossing clock comparator. A differential comparator with programmable hysteresis threshold allows differential signal qualification for noise rejection. The programmable hysteresis threshold, VTH, is driven by a multiplying DAC which is driven by the LEVEL voltage and referenced to VRC (VRC is the internal bandgap reference). Hysteresis thresholds from 30 to 80% may be set with a resolution of better than 1%. A parallel R-C network of RTD and CT sets the hysteresis threshold time constant when not in the Servo mode. A qualified signal zero crossing at the CP-CN inputs triggers the output one shot, Figure 4.

HYSTERESIS COMPARATOR QUALIFICATION

When the Hysteresis Qualification mode is selected, the same threshold qualification comparators and clock comparators are used to implement a polarity checking rule. In this mode, a positive peak that clears the established threshold level will set the hysteresis comparator and trigger the bidirectional one-shot that creates the read data pulses. In order to get another pulse clocked out, a peak of the opposite polarity must clear the negative threshold level to reset the hysteresis comparator and trigger the bidirectional one-shot, Figure 5.

SERVO DEMODULATOR CIRCUIT DESCRIPTION

The 32P4742/4742A servo sections capture four separate servo bursts and provide A, B, C, and D burst outputs, Figure 6(a); the 32P4746/4746A provide A+B, A-B and C-D outputs , Figure 6(b). Internal burst hold capacitors are provided to support low leakage burst capture and reduce external component count. To support embedded servo applications, the 32P4742/4742A provides additional programming registers that set the filter cutoff frequency (fc) and the hysteresis threshold level (VTH) for Servo mode. When SG is activated or deactivated there is a nominal 0.3 µs settling time for the internal DACs to recover from the register switching.

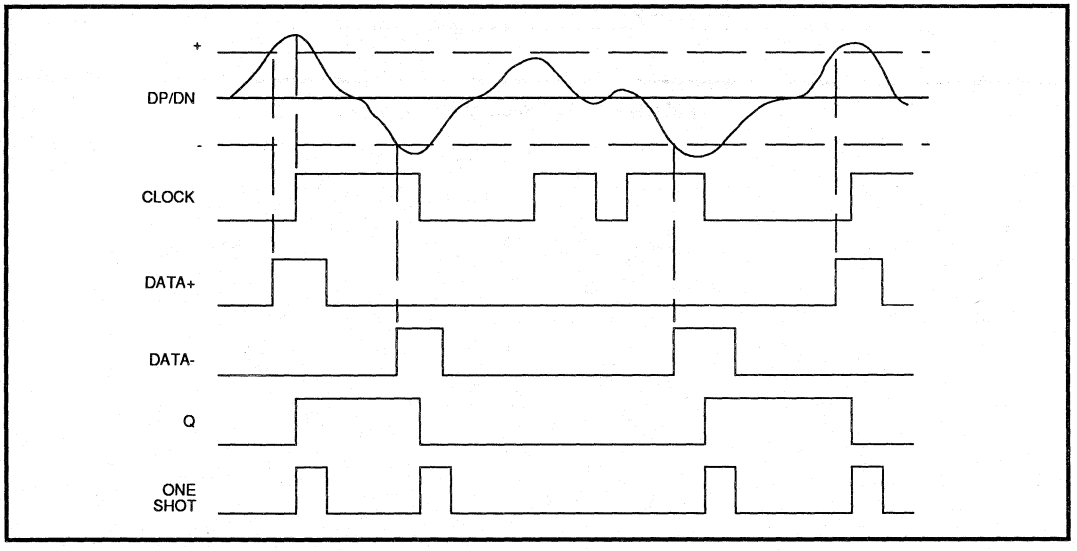


FIGURE 4: Dual Comparator Timing Diagram

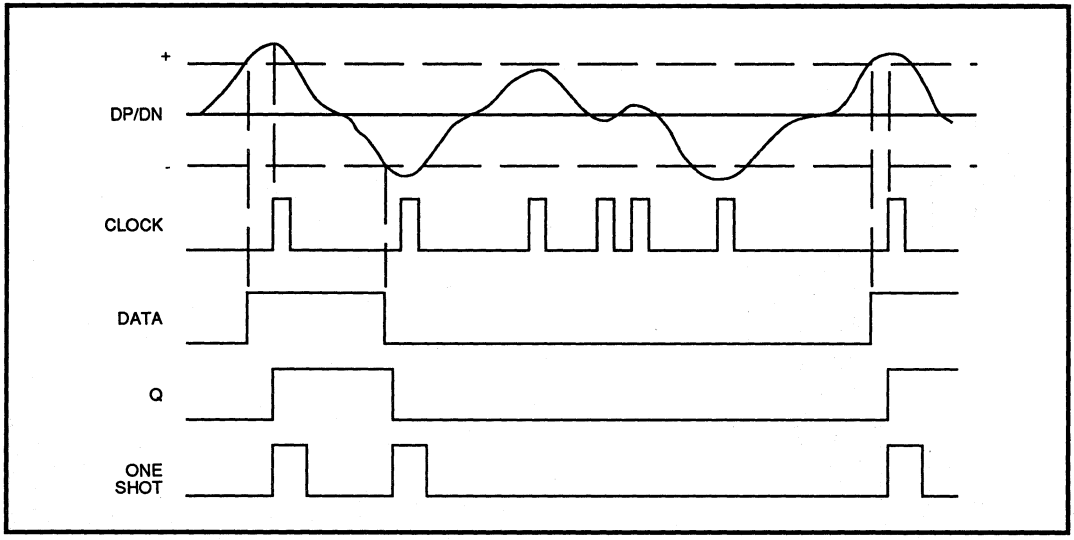


FIGURE 5: Hysteresis Comparator Timing Diagram

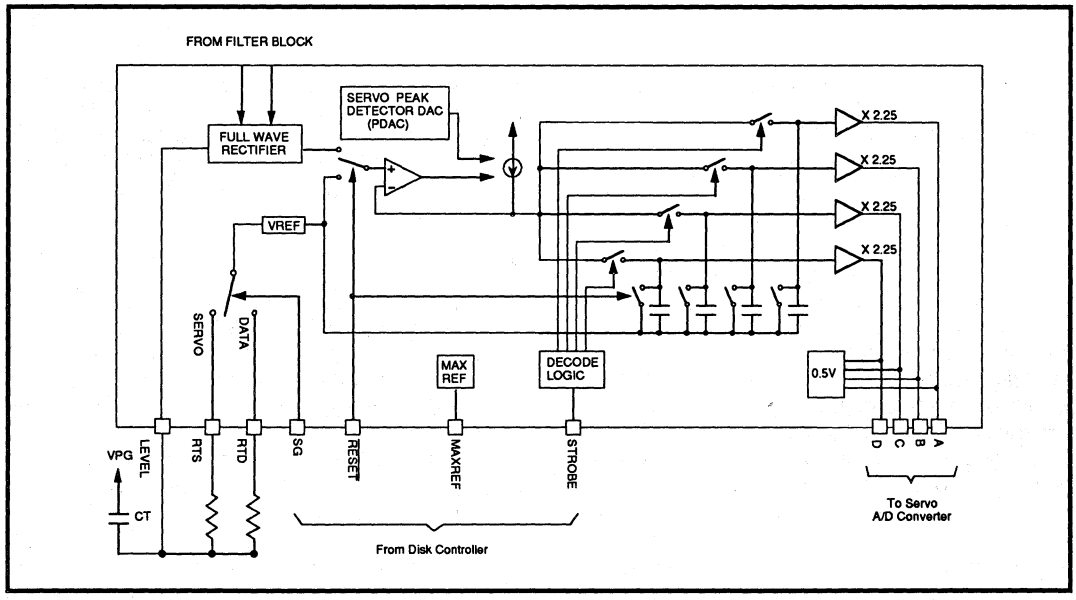


FIGURE 6(a): 32P4742/4742A Servo Capture

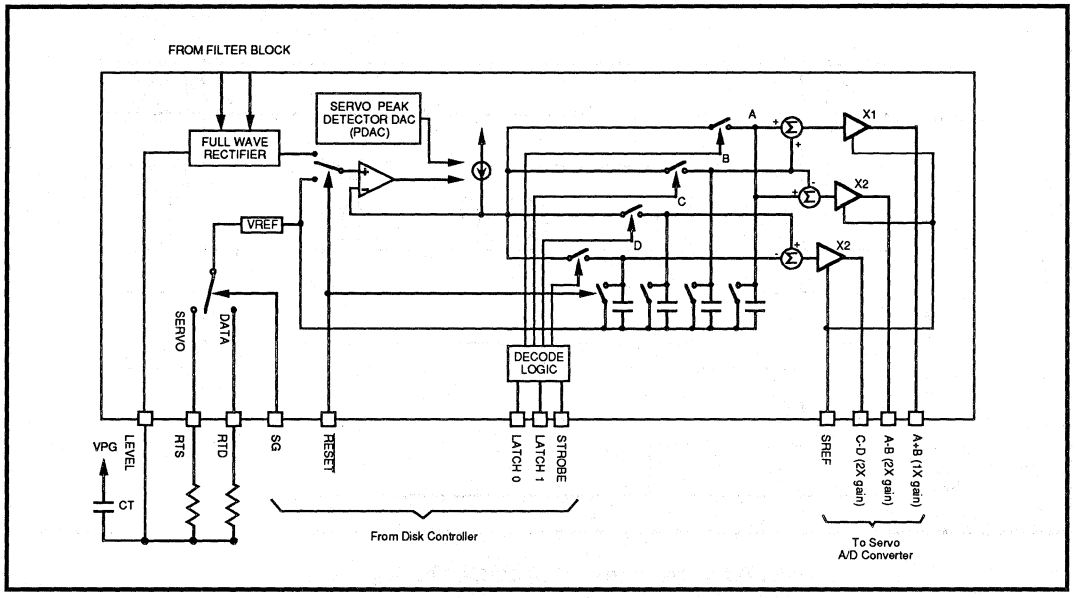


FIGURE 6(b): 32P4746/4746A Servo Capture

FUNCTIONAL DESCRIPTION (continued)

SERVO MODE OPERATION

When the servo gate (SG) is asserted, the control DACs for *fc* and VTH switch from the Data mode registers to the Servo mode registers and the AGC goes into the HOLD/Fast Decay mode. In addition, filter boost is disabled (as determined by the boost control bit), the AGC level is adjusted according to the AGC Level DAC and the RTS servo time constant setting resistor is connected to VRC (VRC is the internal bandgap reference.) By disabling the boost and providing the servo control register for *fc* the servo signal to noise ratio can be greatly improved. When SG is activated or deactivated there is a nominal 0.3 µs settling time for the internal DACs to recover from the register switching. During Servo mode, the AGC circuit remains active. A 4-bit DAC (DACA) is used to set the AGC level over a range of 0.75 to 1.00 Vpp as follows:

VAGC = 1.00 - (DACA x 0.01667) Vpp
where DACA is the value of the AGC Level register

Typically, a servo preamble is used to achieve the desired AGC level and then the $\overline{\text{HOLD}}$ pin is asserted to hold the AGC gain. When SG goes low to terminate the Servo mode, the AGC goes into the HOLD (0.4 µs)/ Fast Decay (1.0 µs) mode to allow for fast transition into the Read or Write mode.

BURST CAPTURE

For 32P4742/4742A, burst capture is controlled by a single external pin designated STROBE and an internal counter. When SG is active, the first pulse on the STROBE pin gates the output of the servo peak detector to the A burst hold capacitor. The capacitor charges for as long as the STROBE pulse is high. On the falling edge of the STROBE signal, the internal counter is incremented. The next STROBE pulse will then gate the servo peak detector output to the B burst hold capacitor. Again, the capacitor charges for as long as the STROBE pulse is high. On the falling edge of STROBE, the counter is incremented again and the C burst is captured on the next STROBE pulse. On the

next falling edge of STROBE, the counter is incremented again and the D burst is captured on the next STROBE pulse. After the falling edge of the fourth STROBE pulse, the counter is reset to zero and the burst capture process can be repeated. See Figure 7(a) for timing information. The internal counter is also reset when the SG pin is deactivated. The voltage level on each hold capacitor is then provided to buffer amplifiers which generate the servo output signals. A 1.0 Vp-p differential voltage at the DP/DN pins will result in a 2.25V peak burst amplitude. The servo output signals (A, B, C, D) are referenced above an internal baseline of 0.5 volts. The output voltage at the MAXREF pin is a nominal 3.0V, and represents the maximum voltage to which the servo signal outputs will swing. It is typically used as the reference voltage for an external A/D converter. MAXREF is internally reduced to a 0.5 volt level, and establishes the servo zero-signal baseline.

For 32P4746/4746A, four servo control inputs; LATCH0, LATCH1, STROBE, and $\overline{\text{RESET}}$, control the servo peak sample and hold functions. LATCH0 and LATCH1 are decoded to select one of the four internal burst hold capacitors. Driving the STROBE pin high gates the output of the servo peak detector to the selected internal burst hold capacitor. Reference Figure 7(b) for servo timing information.

The voltage level on each hold capacitor is then provided to summing amplifiers which generate the servo output signals. A 1.0V differential voltage at the DP/DN pins will result in a 2.0V peak burst amplitude at the A-B and C-D pins, but only 1.0V at the A+B pin. An input voltage applied to the SREF pin will establish the DC reference voltage for the servo outputs. When A-B = 0, then A-B output will be a SREF.

All four internal burst hold capacitors are discharged when the $\overline{\text{RESET}}$ pin is driven low. The $\overline{\text{RESET}}$ control input overrides the STROBE signals. There are two Reset modes available. A "0" in the MSB of the Write Precomp/Servo Reset register enables the normal or Unidirectional Current Reset mode. The resulting hold capacitor reset voltage will be slightly less than the zero-signal baseline when observed at the BURST output pins. A "1" written to the MSB location results in a high-resolution, or bi-directional current reset in which the capacitor baseline voltage will be equal to the zero-signal baseline voltage.

The drive current of the servo peak detector charge pump is set by a 4-bit word (PDAC) addressed through the serial port. The LSB value is 6 μA, and the offset is 1 LSB such that "0000" corresponds to 6 μA and "1111" results in 96 μA. Maximum noise immunity is obtained in the servo peak detector by choosing the smallest value of charge current to charge the internal 10 pF hold capacitor during the burst acquisition time, see Figure 8.

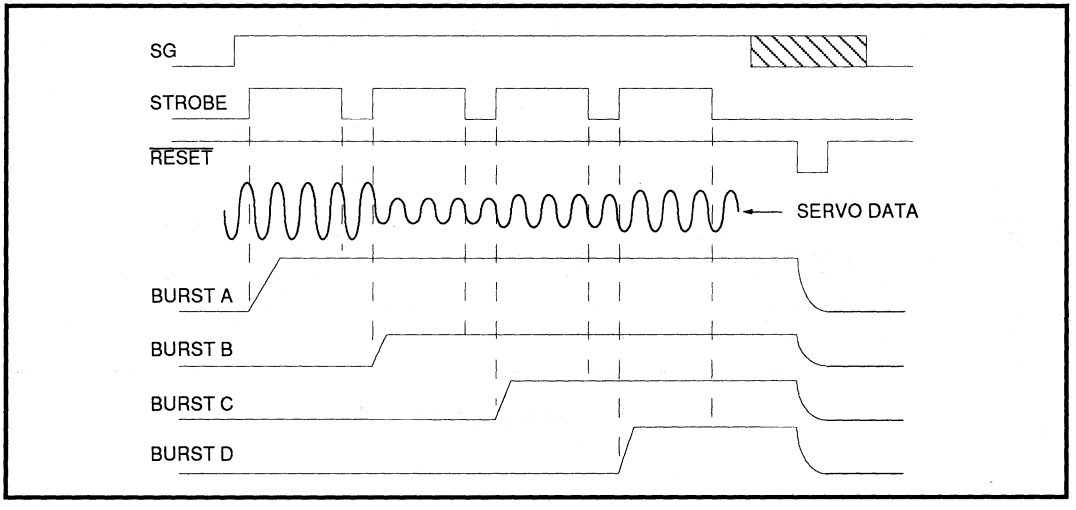


FIGURE 7(a): 32P4742/4742A Servo Capture Timing Diagram

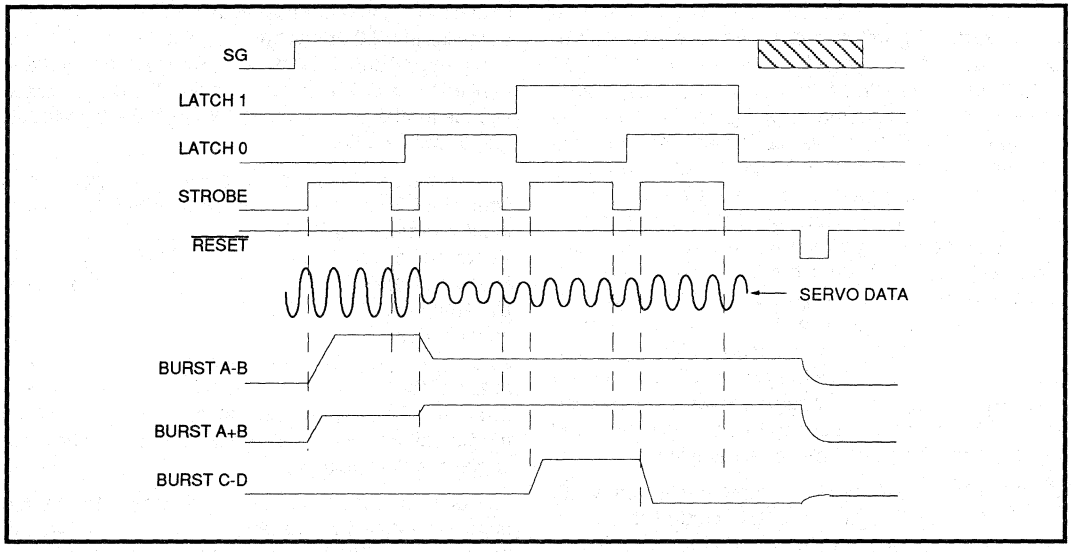


FIGURE 7(b): 32P4746/4746A Servo Capture Timing Diagram

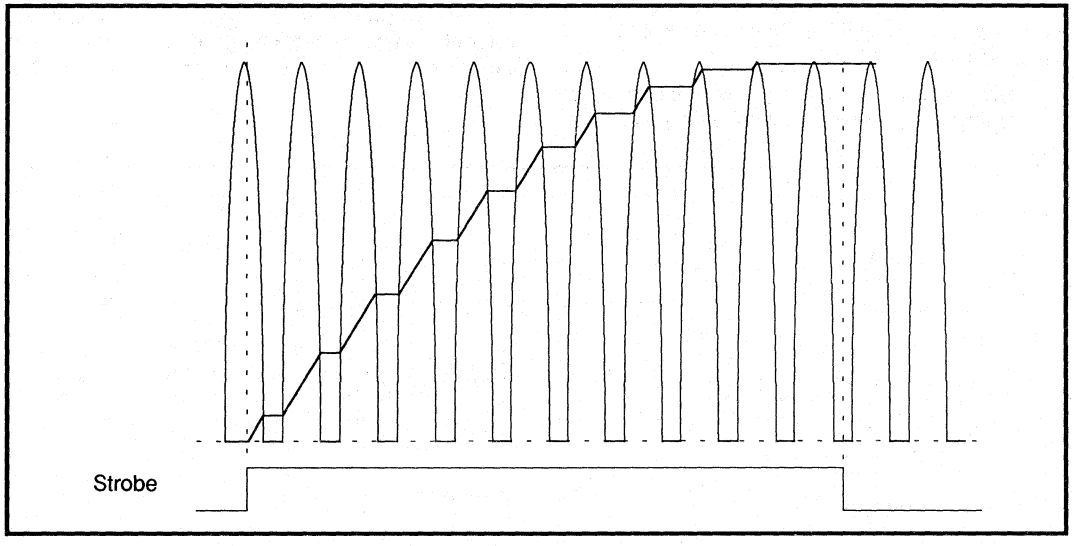


FIGURE 8: Servo Burst Acquisition (SG = $\overline{\text{RESET}}$ = 1)

BURST CAPTURE (continued)

Table 1 shows the recommended PDAC settings as a function of the strobe command duration to achieve acquisition to 99.5% of intended final value. These values are calculated with Fservo = 6.66 MHz at DP/DN.

TABLE 1: PDAC Settings vs Strobe Time

PDAC Word:	0000	00001	0010	0011	0100	0101	0110	0111	1000
Strobe Time (µses):	6.8	4.8	3.4	2.1	1.5	1.2	0.83	0.77	0.74
PDAC Word:	1001	1010	1011	1100	1101	1110	1111		
Strobe Time (µses):	0.71	0.68	0.66	0.64	0.63	0.62	0.61		

The transfer characteristic of the servo demodulator is shown in Figure 9. The peak detector exhibits constant gain for inputs at DP/DN from 0.2 to 1.2 Vp-p with small non-linearities below 0.2V.

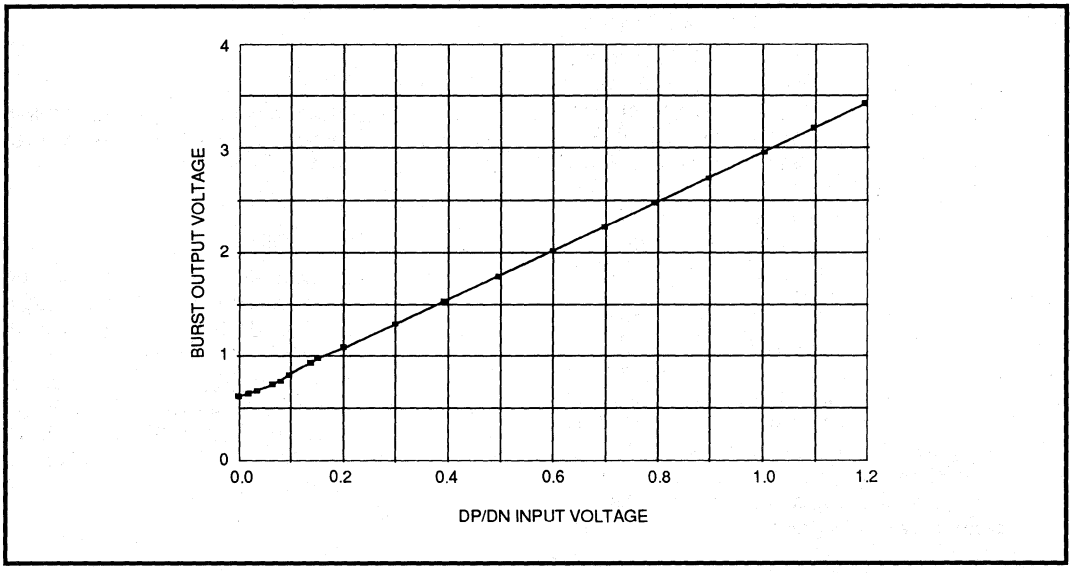


FIGURE 9: Servo Demodulator Transfer Curve

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FUNCTIONAL DESCRIPTION (continued)

TIMING OUTPUTS

To support servo timing recovery, the pulse detector section provides a TTL output of the servo information via the $\overline{RDIO}$ pin. A negative pulse is generated for each servo peak that is qualified through the pulse detector circuitry. Additional servo timing information is supported by the PPOL output. The PPOL pin provides pulse polarity information for the qualified peaks, where a high level TTL output indicates a positive pulse. To reduce noise progagation, $\overline{RDIO}$ will be held high and PPOL will be held low when SG is low and either RG or WG are high.

PROGRAMMABLE FILTER CIRCUIT DESCRIPTION

The SSI 32P4742/4742A programmable filter consist of an electronically controlled low-pass filter with a separate differentiated low-pass output. A seven-pole, low-pass filter is provided along with a single-pole, single-zero differentiator. Both outputs have matched group delays (< 1 ns typical.) A fixed delay of 1.25 ns (typ.) is added to the differentiated outputs to guarantee set-up timing in the data qualifier circuit. The delay matching is unaffected by any amount of programmed equalization or bandwidth. Programmable bandwidth and boost/equalization is provided by internal 7-bit control DACs. The programmable characteristics are automatically switched during Servo mode to improve signal to noise ration. Differentiation pulse slimming equalization is accomplished by a two-pole, low-pass with a two-pole, high-pass feed forward section to provide complimentary real axis zeros. A variable attenuator is used to program the zero locations. The filter implements a 0.05 degree equiripple linear phase response.

The normalized transfer functions (i.e., $\omega c = 2\pi fc = 1$) are:

$$Vnorm/Vi = [(-Ks^2 + 17.98016)/D(s)] \times An$$

and

$$Vdiff/Vi = (Vnorm/Vi) \times (s/0.86133) \times Ad$$

Where D (s) =

$$(s^2+1.68495s+1.31703)(s^2+1.54203\,s+2.95139)(s^2 + 1.14558s + 5.37034)(s + 0.86133),$$

An and Ad are adjusted for a gain of 2 at fs = (2/3)fc.

FILTER OPERATION

AC coupled differential signals from the AGC amplifier are applied to the IN/$\overline{IN}$ inputs of the filter. To improve settling time of the coupling capacitors, the IN/$\overline{IN}$ inputs are placed into a Low-Z state for 1.0 µs when WG goes inactive or when the $\overline{PWRON}$ pin is brought low. The programmable bandwidth and boost/equalization features are controlled by internal DACs and the registers programmed through the serial port. The current reference for both DACs is set using a single external resistor connected from pin RX to ground. The voltage at pin RX is proportional to absolute temperature (PTAT), hence the current for the DACs is a PTAT reference current. A 1000 pF capacitor should be connected in parallel with RX to reduce harmonic distortion.

BANDWIDTH CONTROL

The programmable bandwidth is set by the filter cutoff DAC. This DAC has two separate 7-bit registers that can program the DAC value as follows:

$$fc = 0.1485 \times DACF - 0.9013 \text{ (MHz)}$$

where DACF = DMCR or SMCR value

In the Data mode, the Data Mode Cutoff Register (DMCR) is used to determine the filter's 3 dB cutoff frequency. In the Servo mode, the Servo Mode Cutoff Register (SMCR) is used. Switching of the registers is controlled by the servo gate (SG) pin. The filter cutoff set by the internal DAC is the unboosted 3 dB frequency. When boost/equalization is added, the actual 3 dB point will move out. Table 2 provides information on boost verses 3 dB frequency.

TABLE 2: 3 dB Cutoff Frequency versus Boost Magnitude

BOOST (dB)	*fc* Multiplier	BOOST (dB)	*fc* Multiplier
0	1.00	7	2.42
1	1.21	8	2.51
2	1.50	9	2.59
3	1.80	10	2.66
4	2.04	11	2.73
5	2.20	12	2.80
6	2.32	13	2.86

BOOST/EQUALIZATION CONTROL

The programmable equalization is also controlled by an internal DAC. The 7-bit Filter Boost Control Register (FBCR) determines the amount of equalization that will be added to the 3 dB cutoff frequency, as follows:

$$\text{Boost} = 20 \log [2.65 \times 10^{-2} \times \text{DACS}) + (6.0 \times 10^{-5} \times \text{DACS} \times \text{DACF}) + 1] \text{ (dB)}$$

where DACF is the cutoff register and DACS is the boost register.

For example, with the DAC set for maximum output (FBCR = 7F or 127) there will be 13 dB of boost added at the 3 dB frequency. This will result in +10 dB of signal boost above the 0 dB baseline. When SG is active the boost can be disabled by setting bit 7 in FBCR. When bit 7 is "0" and SG is active the boost will automatically be set to 0 dB. If bit 7 is "1" the boost will remain at its programmed value regardless of the state of SG.

TIME BASE GENERATOR CIRCUIT DESCRIPTION

The time base generator, which is a PLL based circuit, provides programmable reference frequency FOUT, Figure 10. The frequency can be programmed with an accuracy better than 1%. An external passive loop filter is required to control the PLL locking characteristics. The filter is fully-differential and balanced in order to suppress Common mode noise.

In Read, Write and Idle modes, the time base generator is programmed to provide a stable reference frequency (FOUT) for the data synchronizer. In Write and Idle modes, FOUT is the output of the time base generator. In Read mode FOUT is disabled after the data synchronizer has achieved lock and switched over to read data as the source for the RRC. This minimizes jitter in the data synchronizer PLL. The reference frequency is programmed using the M and N registers of the time base generator via the serial port, and is related to the external reference clock input, FREF, as follows:

$$\text{FOUT} = ((M+1)/(N+1))\text{FREF}$$

The VCO center frequency and the phase detector gain of the time base generator are controlled by an internal IDAC addressed through the data recovery control register (DRCR). To insure precise tracking of the data separator to the time base VCO, the control voltage from the VCO is converted to a current which is provided to the data separator VCO and 1/3 cell delay. The VCO frequency equation is:

$$\text{Fvco} = [12.5/(\text{RR} + 0.4)] \times [(0.614 \times \text{IDAC}) + 3.84] \text{ MHz}$$

where IDAC is the value in the DRCR and RR is the value (kΩ) of the external RR resistor.

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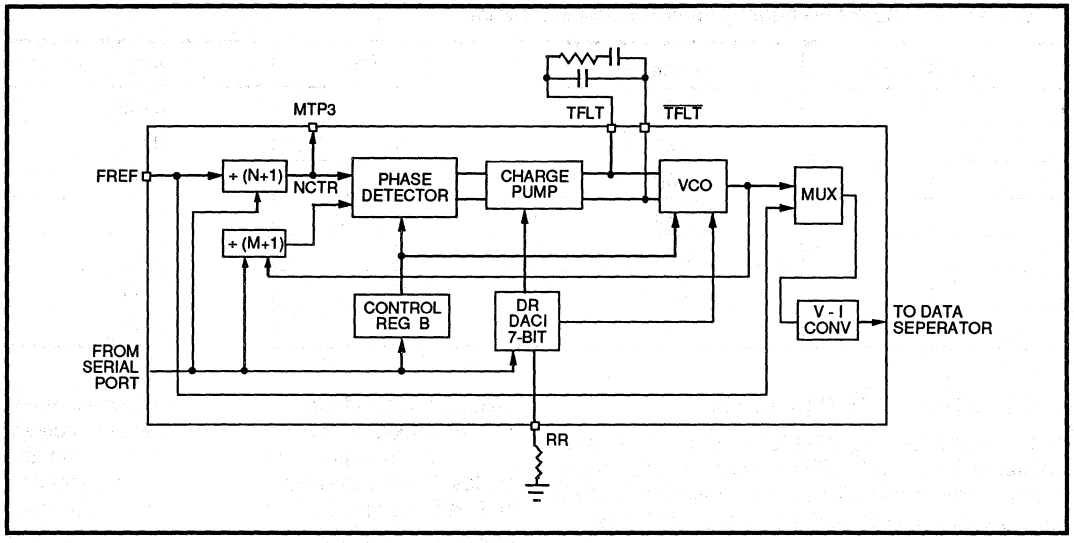

FIGURE 10: Time Base Generator Phase Locked Loop

FUNCTIONAL DESCRIPTION (continued)

DATA SEPARATOR CIRCUIT DESCRIPTION

The data separator circuit provides complete encoding, decoding, and synchronization for RLL 1,7 format data. In the Read mode, the circuit performs sync field search and detect, data synchronization and data decoding. In the Write mode, the circuit provides data encoding and write precompensation for NRZ data applied to the NRZ0/1 pins. Data rate is established by the internal time base generator and the 1/3 cell delay.

PHASE LOCKED LOOP

The circuit employs a dual mode phase detector; harmonic in the Read mode and non-harmonic in the Write and Idle modes, Figure 11. In the Read mode the harmonic phase detector updates the PLL with each occurrence of a $\overline{\text{DRD}}$ pulse. In the Write and Idle modes the non-harmonic phase detector is continuously enabled, thus maintaining both phase and frequency lock onto the reference frequency of the internal time base generator. By acquiring both phase and frequency lock to the input reference frequency and utilizing a zero phase restart technique, the VCO transient is minimized and false lock to read data is eliminated. The phase detector incorporates a charge pump in order to drive the loop filter directly. The polarity and width of the output current pulses correspond to the direction and magnitude of the phase error.

The data synchronizer also requires an external passive loop filter to control its PLL locking characteristics. This filter is also fully-differential and balanced in order to suppress common mode noise.

READ/WRITE MODE CONTROL

The read gate (RG) and write gate (WG) inputs control device operation in Data mode. RG is an asynchronous input that must be initiated at the start of a valid preamble field. It can be terminated at any position on the disk. WG is also an asynchronous input. It can be initiated at any time but should not be terminated prior to the last output write data pulse. To insure that the device will not enter any unknown states, RG overrides WG.

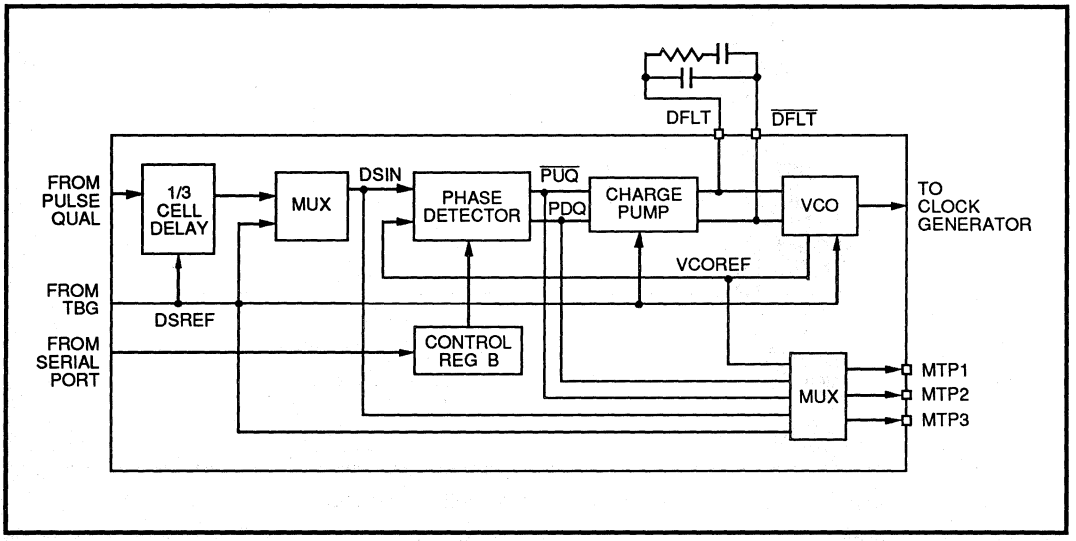

FIGURE 11: Data Separator Phase Locked Loop

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READ MODE

The data synchronizer utilizes a fully integrated fast acquisition PLL to accurately develop the decode window. Read gate (RG) initiates the PLL locking sequence and selects the PLL reference input; a high level (Read mode) selects the internal RD input and a low level selects the reference clock. In the Read mode the falling edge of $\overline{DRD}$ enables the phase detector while the rising edge is phase compared to the rising edge of the VCO reference (VCOR.) As depicted in Figure 12, $\overline{DRD}$ is a 1/3 NRZ bit cell wide pulse whose leading edge is defined by the falling edge of $\overline{RD}$. A decode window is developed from the VCOR clock.

VCO Lock and Bit Sync Enable

One of two VCO locking modes will be entered depending on the state of the gain shift (GS) bit, or bit 1, in the Control B register. An internal read gate is asserted 3 $\overline{DRD}$ transitions after read gate is asserted. The phase detector then enters a High Gain mode of operation to support fast phase acquisition. After an internal counter counts a total of 14 transitions of the internal $\overline{DRD}$ signal, including the 3 transitions prior to internal read gate, the gain is reduced by a factor of 3 if GS = 1. If GS = 0 the gain remains constant. This gain shift reduction reduces the bandwidth and damping factor of the loop by $\sqrt{3}$ which provides improved jitter performance in the Data Follow mode. The counter continues to count the next 5 $\overline{DRD}$ transitions (a total of 19 x 3T from assertion of RG) and then asserts an internal VCO lock signal. The VCO lock signal activates the decoder bit synchronization circuitry to define the proper decode boundries. The next 2 x 3T patterns are used to set the proper decode window so that VCO is in sync with RRC and RRC is in sync with the data. Following this, the NRZ outputs are enabled and the data is toggled through the decoder for the duration of the RG.

When the VCO lock signal is asserted, the internal RRC source is switched from the time base generator output to the VCO output signal that is phase locked to $\overline{DRD}$. During the internal RRC switching period the external RRC signal may be held for a maximum of 1 NRZ clock period, however no short duration glitches will occur.

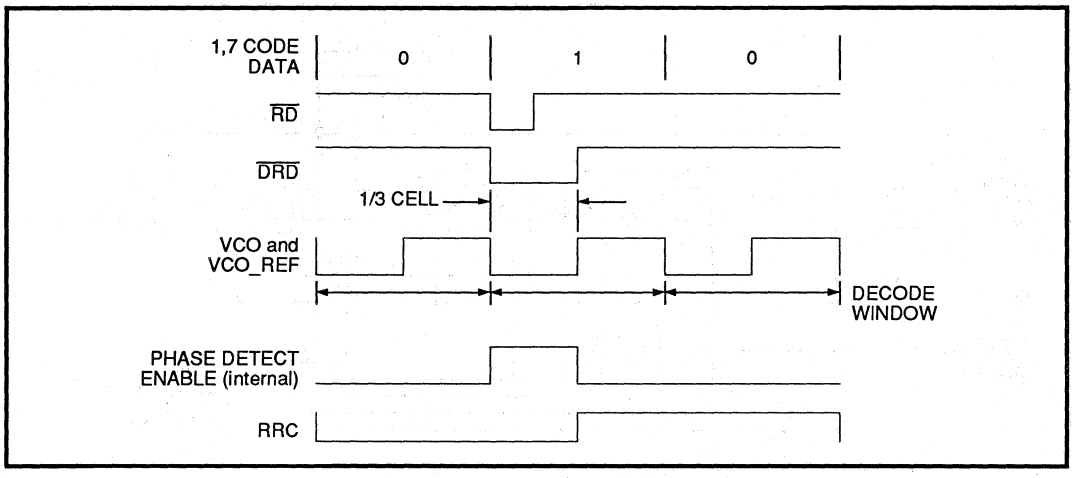

FIGURE 12: Data Synchronization Waveform

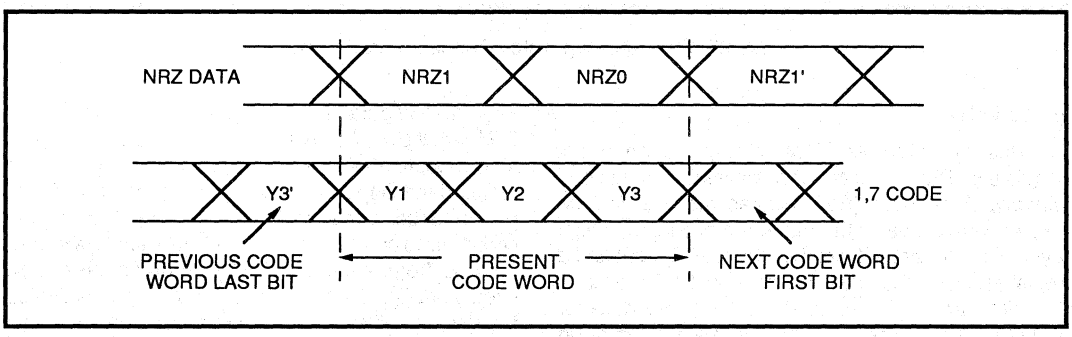

FIGURE 13: NRZ Data Word to 1,7 Code Word Bit Comparison
(Reference Table 4 for decode scheme)

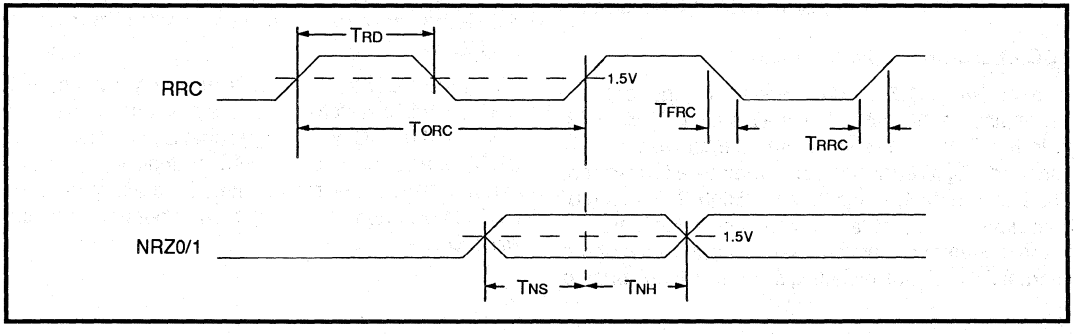

FIGURE 14: NRZ Read Timing

READ MODE (continued)

Window Shift

Shifting the phase of the VCO clock effectively shifts the relative position of the $\overline{DRD}$ pulse within the decode window. Decode window control is provided via the WS control bits of the Window Shift Control Register (WSCR).

NON READ MODE

In the non-Read modes, the PLL is locked to the reference clock. This forces the VCO to run at a frequency which is very close to that required for tracking actual data. When the reference input to the PLL is switched, the VCO is stopped momentarily, then restarted in an accurate phase alignment with the next PLL reference input pulse. By minimizing the phase alignment error in this manner, the acquisition time is substantially reduced.

WRITE MODE

In the Write mode the circuit converts NRZ data from the controller into 1,7 RLL formatted data for storage on the disk. Write mode is entered by asserting the write gate (WG) while the RG and SG are held low. During Write mode the VCO and the RRC are referenced to the internal time base generator signal. The write data output is a negative going TTL signal for the 32P4742 and a differential PECL signal for the 32P4742A. For the 32P4742A, the rising edge of the WD pin is the active edge. External termination of the WD/$\overline{WD}$ pins is required on the 32P4742A.

Write Mode Operation

Write mode is entered by asserting WG high ("1") while RG and SG are held low ("0"). A preamble pattern of at least 19 '3T' patterns must be generated before any coded data can be written. The 3T preamble is written by holding both NRZ0 and NRZ1 low ("0") while WCLK is toggled. The first non zero NRZ input bits indicate the end of the preamble pattern. After a delay of 3 WCLK time periods, non-preamble data begins to toggle out WD. At the end of the write cycle, 3 WCLK cycles of blank NRZ should be added to insure the encoder is flushed of data before the WG can be transitioned low. WD stops toggling a maximum of 2 WCLK time periods after WG goes low. Reference Figures 15 and 17 for detailed timing information. In Figure 15, note that the NRZ1 bit is shifted into the encoder first and the NRZ0 bit is shifted into the encoder second. Because two bits are clocked into the device on each WCLK pulse, the encoder will always generate a predictable pattern.

Direct Write Function

The 32P4742 includes a Direct Write (DW) function that allows the NRZ0 data to bypass the encoder and write precomp circuitry. When the DW bit is set in the CBR, the data applied to NRZ0 will bypass the encoder and write precomp and directly control the WDI output buffer. This allows the user to perform DC erase and media tests. A rising edge at NRZ0 causes a rising edge on $\overline{WD}$, a falling edge at NRZ0 causes a falling edge on $\overline{WD}$. This information applies to the 32P4742.

A rising edge at NRZ0 causes a rising edge on $\overline{WD}$ and a falling edge on WD. A falling edge at NRZ0 causes a falling edge on $\overline{WD}$ and a rising edge on WD. This information applies to the 32P4742A.

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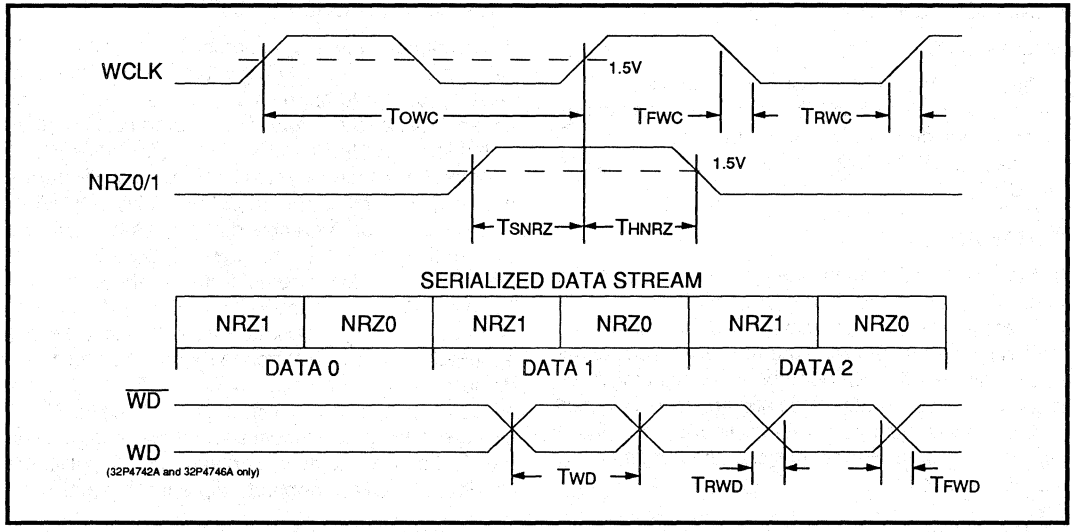

FIGURE 15: $\overline{WD}$ and NRZ Write Timing

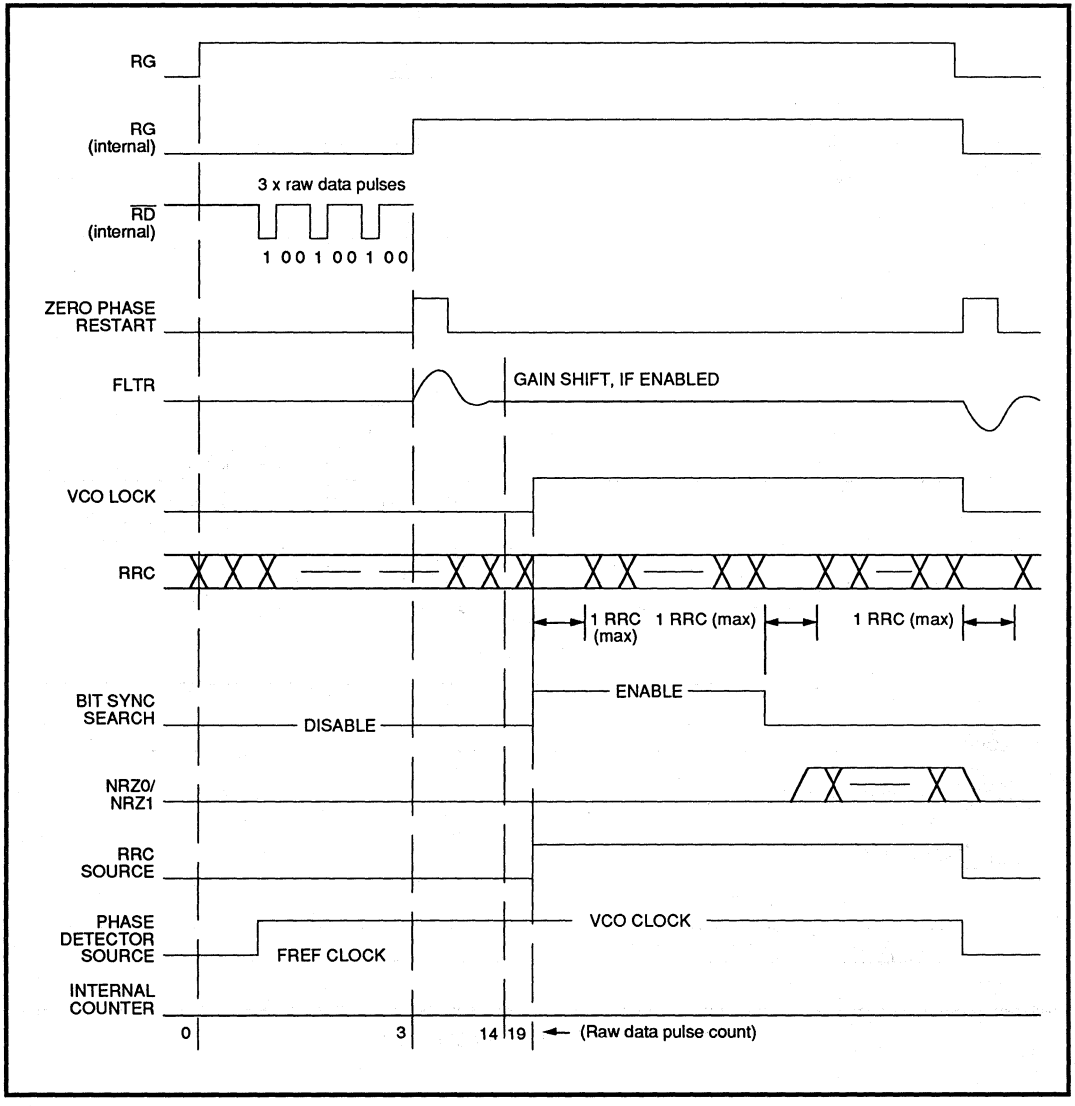

FIGURE 16: Read Mode Locking Sequence

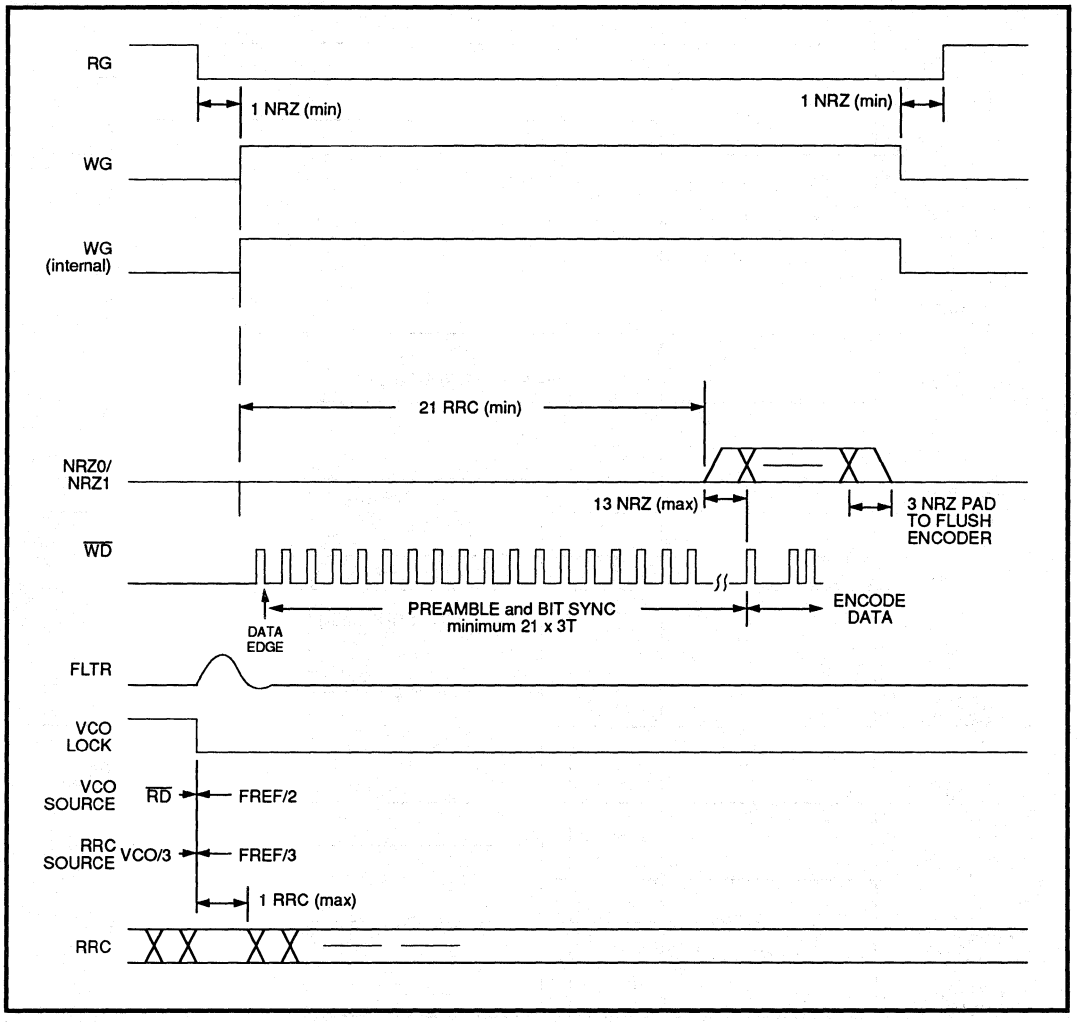

FIGURE 17: Write Data Operation

FUNCTIONAL DESCRIPTION (continued)

OPERATING MODES AND CONTROL

The device has several operating modes that support read, write, servo, and power management functions. Mode selection is accomplished by controlling the read gate (RG), write gate (WG), servo gate (SG), and $\overline{\text{PWRON}}$ pins. Additional modes are also controlled by programming the Power Down Control Register (PDCR), the Control A (CAR) register, and the Control B (CBR) register via the serial port.

External Mode Control

All operating modes of the device are controlled by driving the read gate (RG), write gate (WG), servo gate (SG), and $\overline{\text{PWRON}}$ pins with TTL compatible signals (refer to Table 3). For normal operation the $\overline{\text{PWRON}}$ pin is driven low. During normal operation the device is controlled by the read gate (RG), write gate (WG), and servo gate (SG) pins. Servo gate (SG) determines the active mode of the device. When SG is high, the device enters the Servo mode, regardless of the state of either RG or WG. When SG is low, RG and WG can be used. When RG is high the device is in Read mode regardless of the state of WG. When SG and RG are both low, WG is brought high to enter Write mode. If SG, RG, and WG pins are all low the device will be in Idle mode.

REGISTER DESCRIPTION

Control Registers

The serial port registers allow the user to configure the device. The register map for the device is shown in Table 4. The bits of these registers are defined as follows:

POWER DOWN CONTROL REGISTER (PDCR)

BIT	NAME	DESCRIPTION
0	PD/SVO	Pulse detector/servo power enable: Determines the state of the pulse detector and servo circuits when $\overline{\text{PWRON}}$ pin is low. 0 = Circuits enabled 1 = Circuits powered down
1	TBGKD	Time base KD select: Determines the phase detector gain of the time base generator. 0 = KD is 3x nominal value 1 = KD is 1x nominal value
2	FLTR	Filter power enable: Determines the state of the filter when $\overline{\text{PWRON}}$ pin is low. 0 = Filter enabled 1 = Filter powered down
3	DS	Data separator power enable: Determines the state of the data separator circuit when $\overline{\text{PWRON}}$ pin is low. 0 = Data separator enabled 1 = Data separator powered down
4	TBG	Time base generator power enable: Determines the state of the Time base generator circuit when $\overline{\text{PWRON}}$ pin is low. 0 = Time base generator enabled 1 = Time base generator powered down
5-7	N/A	Device ID: These bits are a read only ID code for the device.

REGISTER DESCRIPTION (continued)

DATA MODE CUTOFF (DACF)

BIT	NAME	DESCRIPTION
0-6	DMC	Filter cutoff setting for Data mode. Substitute this value for DACF into the cutoff calculation for the filter in Data mode operation.
7	N/A	Not used. Set to zero.

SERVO MODE CUTOFF (DACF)

0-6	DMC	Filter cutoff setting for Servo mode. Substitute this value for DACF into the cutoff calculation for the filter in Servo mode operation.
7	WDB	Buffer type: Determines if the TTL write data buffer is enabled. 0 = enabled 1 = disabled

FILTER BOOST REGISTER (DACS)

0-6	FBC	Filter boost setting. Substitute this value for DACS into filter calculations.
7	SBE	Servo boost enable: Determines if boost is enabled when SG is high. 0 = Boost disabled when SG is high 1 = Boost enabled when SG is high

DATA THRESHOLD REGISTER (VTHDAC)

0-6	DTH	Data threshold setting. Substitute this value for VTHDAC into the threshold calculation for Data mode operation.
7	DQ	Qualifier select: Determines the type of qualifier used in Data mode. 0 = Hysteresis qualifier 1 = Dual comparitor qualifier

SERVO THRESHOLD REGISTER (VTHDAC)

0-6	STH	Servo threshold setting. Substitute this value for VTHDAC into the threshold calculation for Servo mode operation.
7	SQ	Qualifier select: Determines the type of qualifier used in Servo mode. 0 = Hysteresis qualifier 1 = Dual comparitor qualifier

CONTROL A REGISTER (CAR)

BIT	NAME	DESCRIPTION
0	EPDT	Enable Phase Detector (Time Base Generator): This bit disables the output of the phase detector to the VCO. An external voltage applied across the TFLT pins drives the VCO to a fixed frequency. 0 = Phase detector charge pump disabled 1 = Phase detector charge pump enabled
1	UT	Enable Pump Up Current (Time Base Generator): This bit enables a test mode for checking the charge pump output current. The charge pump will source a fixed DC current from TFLT and sink the current at $\overline{\text{TFLT}}$. 0 = No current 1 = Pump up current enabled
2	DT	Enable Pump Down Current (Time Base Generator): This bit enables a test mode for checking the charge pump output current. The charge pump will source a fixed DC current from $\overline{\text{TFLT}}$ and sink the current at TFLT. 0 = No current 1 = Pump down current enabled
3	MTP3E	This bit enables the MTP3 test point output buffer. 0 = Test point disabled 1 = Test point enabled
4	BYPT	This bit enables a Time Base Generator Bypass mode where the FREF input is connected to the data separator phase detector input. 0 = Time base enabled 1 = Time base bypassed
5/6	TMS0/1	These bits select the test point signal sources (ref Table 8)
7	FDTM	This bit continuously enables the AGC fast decay current. 0 = Fast decay current always on 1 = Normal fast decay operation Set to 1 for normal operation.

REGISTER DESCRIPTION (continued)

CONTROL B REGISTER (CBR)

BIT	NAME	DESCRIPTION
0	DW	This bit enables the direct write (Bypass Endec) function. 0 = Normal operation 1 = Bypass encoder, NRZ0 buffered to $\overline{WD}$ (or $\overline{WD}$/WD for 32P4742A and 32P4746A)
1	GS	This enables the data sep. phase detector gain switch in Read mode. 0 = Normal operation 1 = Gain shift until 14 x 3T (Read mode only)
2	RDIO	This bit enables the $\overline{RDIO}$ pin as an input. 0 = $\overline{RDIO}$ is an output 1 = $\overline{RDIO}$ is an input
3	EPDD	Enable Phase Detector (Data Separator): This bit disables the output of the phase detector to the VCO. An external voltage applied across the DFLT pins drives the VCO to a fixed frequency. 0 = Phase detector charge pump disabled 1 = Phase detector active
4	UD	Enable Pump Up Current (Data Separator): This bit enables a test mode for checking the charge pump output current. The charge pump will source a fixed DC current from DFLT and sink the current at $\overline{DFLT}$. 0 = No current 1 = Pump up current enabled
5	DD	Enable Pump Down Current (Data Separator): This bit enables a test mode for checking the charge pump output current. The charge pump will source a fixed DC current from $\overline{DFLT}$ and sink the current at DFLT. 0 = No current 1 = Pump down current enabled
6	MTP1,2E	This bit enables the multiplexed test points (MTP1, 2) 0 = Test points disabled 1 = Test points enabled
7	-	Not used. Set to zero.

N COUNTER REGISTER

0-6	N	N counter value.
7	LZT	Low-Z time period: Determines the time period for the Low-Z and fast decay one-shots. 0 = 1 µs nominal time-out (0.4 µs HOLD on SG edges) 1 = 2 µs nominal time-out (0.5 µs HOLD on SG edges)

M COUNTER REGISTER

0-7	M	M counter value.

DATA RECOVERY REGISTER (DRCR)

BIT	NAME	DESCRIPTION
0-6	IDAC	Center frequency DAC value. Sets the center frequency for the data synchronizer VCO and the TBG VCO.
7	TM	Test mode bit: SSi use only. Set to 0 for normal operation.

WINDOW SHIFT REGISTER (WSR)

<table>
<tr><td>0-3</td><td>WS</td><td colspan="3">Window shift DAC value.</td></tr>
<tr><td>4</td><td>WSD</td><td colspan="3">Window shift direction.
0 = Early
1 = Late</td></tr>
<tr><td>5</td><td>WSE</td><td colspan="3">Window shift enable.
0 = Disable
1 = Enable</td></tr>
<tr><td rowspan="3">6-7</td><td rowspan="3">TDAC0/1</td><td colspan="3">DACOUT test point select: Selects the DAC output to be provided on the DACOUT test point. The preferred setting when DACOUT is not being monitored is to set TDAC0 = 1 and TDAC1 = 0:</td></tr>
<tr><td>TDAC1</td><td>TDAC0</td><td>DAC MONITORED</td></tr>
<tr><td>0
0
1
1</td><td>0
1
0
1</td><td>Filter Fc DAC
Qualifier threshold DAC (VTH)
Window shift DAC
Write precomp DAC; the selection of the early or late DAC is controlled by the WPE bit.
WPE = 0 — Late
WPE = 1 — Early</td></tr>
</table>

WRITE PRECOMP REGISTER (WPR)

0-2	WPE	Write precomp early DAC value.
3	WPE	Write precomp enable. 0 = Disable 1 = Enable
4-6	WPL	Write precomp late DAC value.
7	SRST	Servo reset select. Set to 1 for normal operation.

REGISTER DESCRIPTION (continued)

AGC LEVEL REGISTER (ALR)

0-3	ADAC	AGC level DAC value. Sets AGC level in Servo mode. 0000 = 1 Vpp 1111 = 0.75 Vpp
4-7	PDAC	Servo peak detector current DAC value. Sets the servo peak detector current in 6 µA steps. 0000 = 6 µA charge current 1111 = 96 µA charge current

Power Down Control

For power management, the $\overline{\text{PWRON}}$ pin can be used in conjunction with the Power Down Control Register (PDCR) to set the Operating mode of the device. The PDCR provides a control bit for each of the functional blocks. When the $\overline{\text{PWRON}}$ pin is brought high ("1") the device is placed into Sleep mode (<0.5 mA) and all circuits are powered down except the serial port. This allows the user to program the serial port registers while still conserving power. Register information is retained during the Sleep mode so it is not necessary to reprogram the serial port registers after returning to an Active mode. When the $\overline{\text{PWRON}}$ pin is low ("0"), the contents of the PDCR determine which blocks will be active. Register mapping for the PDCR is shown in Table 4. To improve recovery time from the Sleep mode, the inputs to the filter and AGC circuits are placed into a Low-Z mode.

TABLE 3: Mode Control Table

CONTROL LINE				DEVICE MODE	DAC CONTROL			
$\overline{PWRON}$	RG	SG	WG		VTH	FC	BOOST	HYSTERESIS
1	X	X	X	**SLEEP MODE:** All functions are powered down. The serial port registers remain active and register programming data is saved.	off	off	off	off
0	0	0	1	**WRITE MODE:** The pulse detector is inactive. The data synchronizer VCO is locked to the internal time base generator Write precomp circuit is clocked by internal time base.	DR	DR	DR	DR
0	1	0	X	**READ MODE:** The pulse detector is active. The data synchronizer begins the preamble lock sequence.	DR	DR	DR	DR
0	X	1	X	**SERVO MODE:** The pulse detector is active and the servo control registers are enabled for the Fc DAC and the VTH DAC. $\overline{RDIO}$ is also active. The data synchronizer and time base generator can be disabled using the PDCR.	SR	SR	off ↑ On if SBE = 1	SR
0	0	0	0	**IDLE MODE:** The contents of the PDCR determine which blocks are powered-up. In normal operation with all blocks powered-up, the pulse detector is active, the data synchronizer VCO is locked to the time base generator, and the data control registers are used for VTH and FC.	DR	DR	DR	DR
				If multiple control signals are active, the priority order will be $\overline{PWRON}$, SG, RG, and WG. For example, if SG and RG are both "1", the Servo mode will be active.				

DAC Control Key: DR = data register, SR = servo register, off = disabled

DAC Control Key: DR = data register, SR = servo register, off = disabled

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TABLE 4: Serial Port Register Mapping

REGISTER NAME	A6						A0	R/W	D7							D0
	ADDRESS								DATA BIT MAP							
POWER DOWN CONTROL	0	0	0	0	0	1	0	0	--	--	--	TBG 1 = Disable 0 = Enable	DATA SEP 1 = Disable 0 = Enable	FILTER 1 = Disable 0 = Enable	TBG KD 1 = 1x KD 0 = 3 x KD	PD/SERVO 1 = Disable 0 = Enable
DATA MODE CUTOFF	0	0	0	0	0	1	1	0	*	FcDDACF BIT 6	FcDDACF BIT 5	FcDDACF BIT 4	FcDDACF BIT 3	FcDDACF BIT 2	FcDDACF BIT 1	FcDDACF BIT 0
SERVO MODE CUTOFF	0	0	1	0	0	1	1	0	Buffer Type 1 = 4742A 0 = 4742	FcsDACF BIT 6	FcsDACF BIT 5	FcsDACF BIT 4	FcsDACF BIT 3	FcsDACF BIT 2	FcsDACF BIT 1	FcsDACF BIT 0
FILTER BOOST	0	0	0	1	0	1	1	0	Servo Boost 1 = Enable 0 = Disable	DACS BIT 6	DACS BIT 5	DACS BIT 4	DACS BIT 3	DACS BIT 2	DACS BIT 1	DACS BIT 0
DATA THRESHOLD	0	0	0	1	0	1	0	0	Data Qual. 1 = Dual 0 = Hys	TDDAC BIT 6	TDDAC BIT 5	TDDAC BIT 4	TDDAC BIT 3	TDDAC BIT 2	TDDAC BIT 1	TDDAC BIT 0
SERVO THRESHOLD	0	0	1	0	0	1	0	0	Servo Qual. 1 = Dual 0 = Hys	TSDAC BIT 6	TSDAC BIT 5	TSDAC BIT 4	TSDAC BIT 3	TSDAC BIT 2	TSDAC BIT 1	TSDAC BIT 0
CONTROL A	0	0	1	1	0	1	0	0	FD Test 1 = Disable 0 = Enable	TMS1	TMS0	TBG 1 = Bypass 0 = Normal	MTP3 1 = Enable 0 = Disable	PUMP DWN 1 = ON 0 = OFF	PUMP UP 1 = ON 0 = OFF	PHASE DET 1 = Enable 0 = Disable
CONTROL B	0	0	0	1	1	0	0	0	*	MTP1/2 1 = Enable 0 = Disable	PUMP DWN 1 = ON 0 = OFF	PUMP UP 1 = ON 0 = OFF	PHASE DET 1 = Enable 0 = Disable	RDIO 1 = Input 0 = Output	GAIN SHFT 1 = ON 0 = OFF	DIR WRITE 1 = ON 0 = OFF
N COUNTER	0	0	0	0	1	1	0	0	Low-Z Time 1 = 2 µs 0 = 1 µs	N COUNT BIT 6	N COUNT BIT 5	N COUNT BIT 4	N COUNT BIT 3	N COUNT BIT 2	N COUNT BIT 1	N COUNT BIT 0
M COUNTER	0	0	0	1	1	1	0	0	M COUNT BIT 7	M COUNT BIT 6	M COUNT BIT 5	M COUNT BIT 4	M COUNT BIT 3	M COUNT BIT 2	M COUNT BIT 1	M COUNT BIT 0
DATA RECOVERY	0	0	0	0	1	0	0	0	Test Mode 1 = Reset 0 = Normal	DAC BIT 6	DAC BIT 5	DAC BIT 4	DAC BIT 3	DAC BIT 2	DAC BIT 1	DAC BIT 0
WINDOW SHIFT	0	0	0	0	1	0	1	0	TDAC 1	TDAC 0	WIN SHFT 1 = Enable 0 = Disable	WS DIR 1 = Late 0 = Early	$\overline{WS3}$	$\overline{WS2}$	$\overline{WS1}$	$\overline{WS0}$
WRITE PRECOMP	0	0	0	1	1	0	1	0	Servo Reset 1 = Hi Res 0 = Normal	$\overline{WL2}$	$\overline{WL1}$	$\overline{WL0}$	WR PRCMP 1 = Enable 0 = Disable	$\overline{WE2}$	$\overline{WE1}$	$\overline{WE0}$
AGC LEVEL	0	1	0	0	0	1	0	0	PDAC BIT 3	PDAC BIT 2	PDAC BIT 1	PDAC BIT 0	ADAC BIT 3	ADAC BIT 2	ADAC BIT 1	ADAC BIT 0

*** Denotes SSI internal test bits. These bits should be set to 0 in normal operation.**

REGISTER DESCRIPTION (continued)

SERIAL INTERFACE OPERATION

The serial interface is a bi-directional port for reading and writing programming data from/to the internal registers of the 32P4742. For data transfers SDEN is brought high, serial data is presented at the SDATA pin, and a serial clock is applied to the SCLK pin. After the SDEN goes high, the first 16 pulses applied to the SCLK pin will shift the data presented at the SDATA pin into an internal shift register on the rising edge of each clock. An internal counter prevents more than 16 bits from being shifted into the register. The data in the shift register is latched when SDEN goes low. If less than 16 clock pulses are provided before SDEN goes low, the data transfer is aborted.

All transfers are shifted into the serial port LSB first. The first byte of the transfer is address and instruction information. The LSB of this byte is the R/W bit which determines if the transfer is a read (1) or a write (0). The remaining 7-bits determine the internal register to be accessed. Table 4 provides register mapping information. The second byte contains the programming data. In Read mode (R/W=1) the 32P4742 will output the register contents of the selected address. In Write mode the device will load the selected register with data presented on the SDATA pin. At initial power-up, the contents of the internal registers will be in an unknown state and they must be programmed prior to operation. During power down modes, the serial port remains active and register programming data is retained.

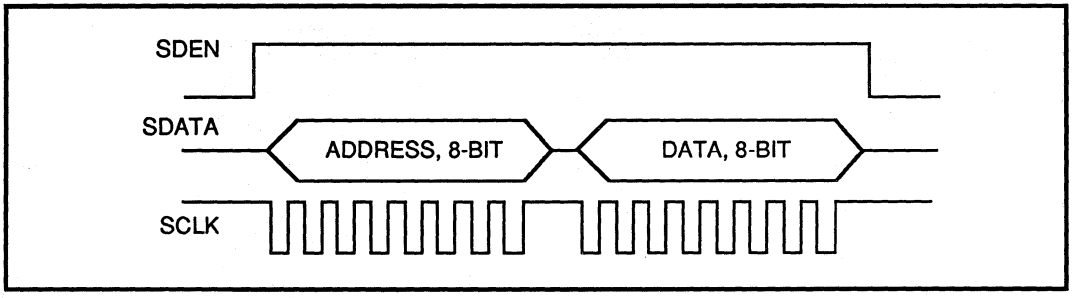

FIGURE 18: Serial Port Transfer Format

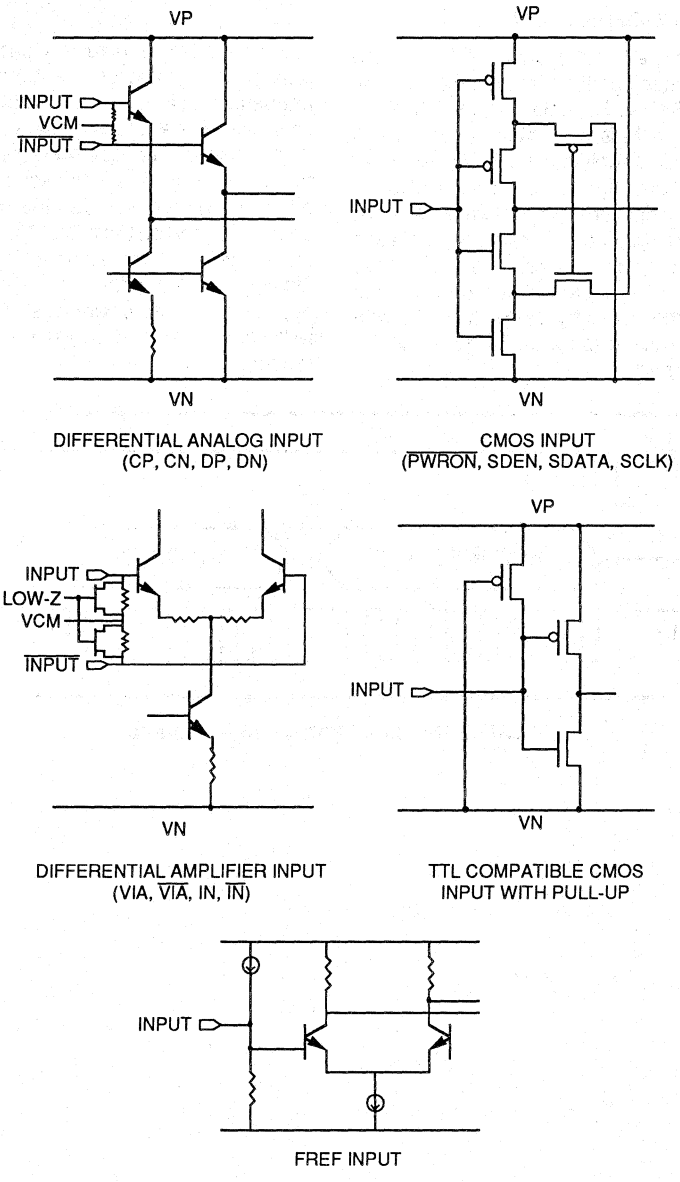

FIGURE 19(a): Input Structures

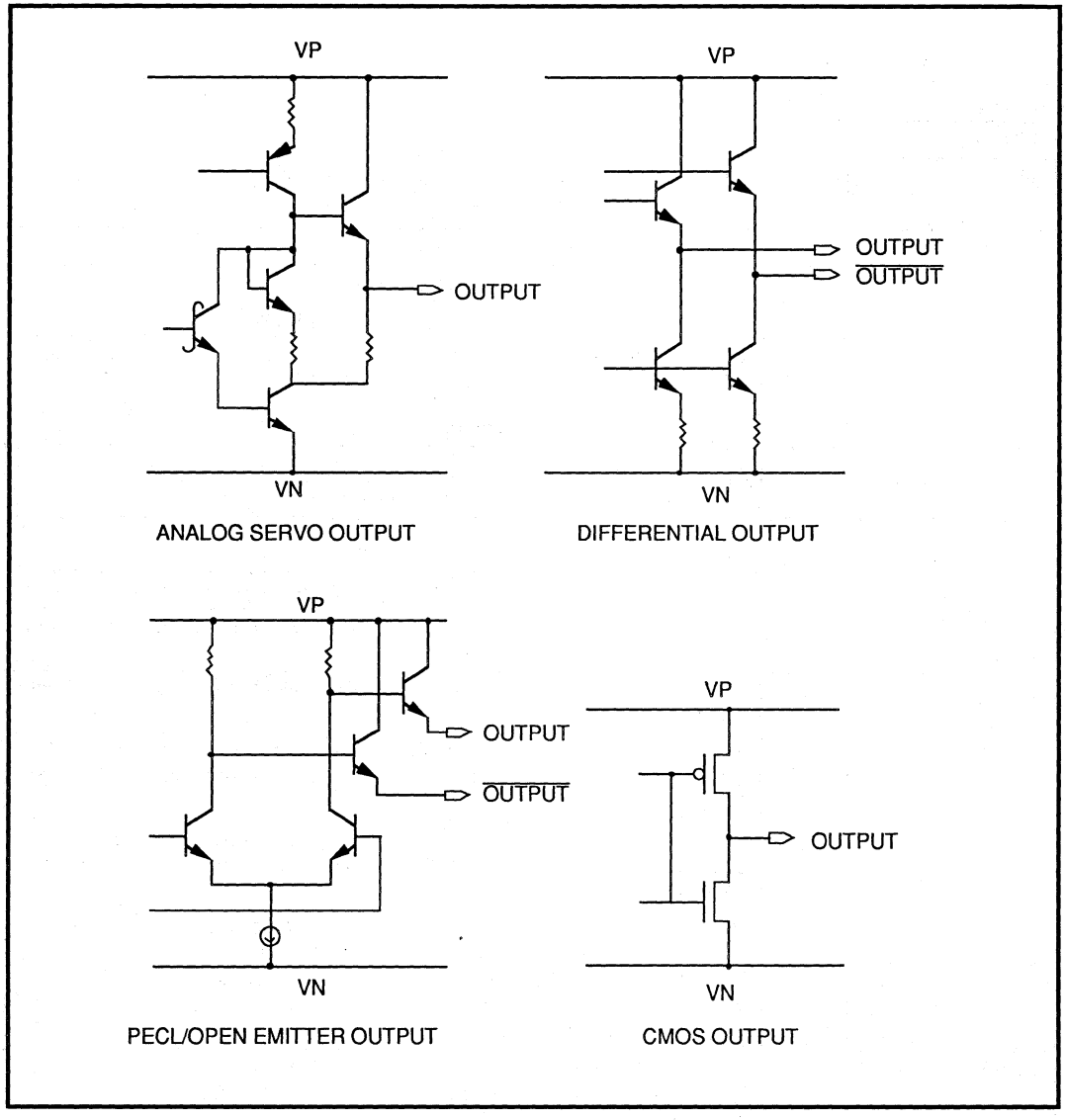

FIGURE 19(b): Output Structures

PIN DESCRIPTION

POWER SUPPLY PINS

NAME	TYPE	DESCRIPTION
VPA		Data separator PLL analog power supply pin
VPB		Time base generator PLL analog power supply pin
VPC		Internal ECL, CMOS logic power supply pin
VPD		$\overline{WD}$ buffer digital power supply pin
VPD2		TTL buffer I/O digital power supply pin
VPG		Pulse detector, filter, servo analog power supply pin
VNA		Data separator PLL analog ground pin
VNB		Time base generator PLL analog ground pin
VNC		Internal ECL, CMOS logic ground pin
VND		TTL buffer I/O digital ground pin
VNG		Pulse detector, filter, servo analog ground pin

INPUT PINS

VIA, $\overline{VIA}$	I	AGC AMPLIFIER INPUTS: Differential AGC amplifier input pins.
DP, DN	I	ANALOG INPUTS FOR DATA PATH: Differential analog inputs to data comparators, full-wave rectifier.
CP, CN	I	ANALOG INPUTS FOR CLOCK PATH: Differential analog inputs to the clock comparator.
$\overline{PWRON}$	I	Power Enable: TTL compatible CMOS power control input. A low level CMOS input enables power to circuitry according to the contents of the PDCR. A high level CMOS input shuts down all circuitry.
$\overline{HOLD}$	I	HOLD CONTROL: TTL compatible CMOS control pin which, when pulled low, disables the AGC charge pump and holds the AGC amplifier gain at its present value.
STROBE	I	BURST STROBE: TTL compatible CMOS burst strobe input. A high level TTL input will enable the servo peak detector to charge one of the burst capacitors. The falling edge of STROBE increments an internal counter that determines which burst capacitor will charge on the next STROBE pulse (reference Figure 7(a), 7(b) for timing.)
$\overline{RESET}$	I	RESET CONTROL INPUT: TTL compatible CMOS reset input. A low level TTL input will discharge the internal servo burst hold capacitors on channels A-D.
IN, $\overline{IN}$	I	FILTER SIGNAL INPUTS: The AGC output signals must be AC coupled into these pins.

INPUT PINS (continued)

FREF	I	REFERENCE FREQUENCY INPUT: Frequency reference input for the time base generator. FREF should be driven either by a direct coupled TTL signal or by an AC coupled ECL signal.
NRZ0/1	I/O	NRZ I/O PORT: TTL compatible CMOS NRZ data port. In Read mode, valid data is output on these pins with each cycle of RRC. In Write mode, data input on these pins is clocked into the device by WCLK.
RG	I	READ GATE: TTL compatible CMOS read gate input. A high level TTL input selects the RD input and enables the Read mode/address detect sequences. A low level selects the FREF input.
SG	I	SERVO GATE: TTL compatible CMOS servo gate input. A high level TTL input activates the Servo mode by selecting the servo control registers, the $\overline{\text{RDIO}}$ pin active in Idle mode, the PPOL pin also active in Idle mode, and the RTS resistor.
WCLK	I	WRITE CLOCK: TTL compatible CMOS write clock input. Must be synchronous with the Write Data NRZ0/1 input. For short cable delays, WCLK may be connected directly to pin RRC.For long cable delays, WCLK should be connected to an RRC return line matched to the NRZ data bus line delay.
WG	I	WRITE GATE: TTL compatible CMOS write gate input. A high level input enables the Write mode.

OUTPUT PINS

MTP1,2,3	O	MULTIPLEXED TEST POINTS: Open emitter ECL output test points. Internal test signals are routed to these test points as determined by the CAR and CBR. Two pull up and down resistors are required to use this pin. They should be removed during normal operation to reduce power dissipation. (Reference Table 8)
OD, $\overline{\text{OD}}$	O	FILTER DIFFERENTIATED OUTPUTS: Filter differentiated outputs. These outputs are AC coupled into the CP/CN inputs.
ON, $\overline{\text{ON}}$	O	FILTER NORMAL OUTPUTS: Filter normal low pass output signals. These outputs are AC coupled into the DP/DN inputs.
PPOL	O	PULSE POLARITY: Pulse polarity CMOS compatible output. The output is high when the pulse being qualified is positive and it is low when the pulse being qualified is negative.
$\overline{\text{RDIO}}$	O	READ DATA I/O: Bi-directional TTL compatible CMOS pin. $\overline{\text{RDIO}}$ outputs $\overline{\text{RD}}$ pulses when in Idle or Servo modes of operation. $\overline{\text{RDIO}}$ is an input when the RDIO bit is enabled in the CBR.
RRC	O	READ REFERENCE CLOCK: Read clock CMOS compatible output. During a mode change, no glitches are generated and no more than one lost clock pulse will occur. When RG goes high, RRC initially remains synchronized to FOUT. When the Sync Bits are detected, RRC is synchronized to the $\overline{\text{DRD}}$. When RG goes low, RRC is synchronized back to the FOUT.

OUTPUT PINS (continued)

VOA, $\overline{VOA}$	O	AGC AMPLIFIER OUTPUT: Differential AGC amplifier output pins. These outputs are ac coupled into the filter inputs (IN/$\overline{IN}$).
$\overline{WD}$	O	WRITE DATA (32P4742/4746): CMOS encoded write data. The falling edge of $\overline{WD}$ represents the data bit. $\overline{WD}$ is internally synchronized to the FOUT reference clock. When direct write is active $\overline{WD}$ is toggled by the signal presented on the NRZ0 pin.
WD/$\overline{WD}$	O	WRITE DATA (32P4742A/4746A): Differential PECL encoded write data. This output format is a bond option. The rising edge of the WD pin represents the data bit (precomped edge). These are open emitter outputs, and an external pull-down resistor is required.

ANALOG PINS

A, B, C, D (32P4742/4742A)		SERVO OUTPUTS: These outputs are processed versions of the voltages captured on the servo hold capacitors. They are referenced to an internally generated, 0.5V baseline.
A-B, C-D, A+B (32P4746/4746A)		SERVO OUTPUTS: These outputs are processed versions of the voltages captured on the servo hold capacitors. They are referenced to SREF.
BYP		The AGC integrating capacitor CA, is connected between BYP and VPG.
TFLT/$\overline{TFLT}$		PLL LOOP FILTER: These pins are the connection points for the time base generator loop filter.
DACOUT		DAC VOLTAGE TEST POINT: This test point monitors the outputs of the internal DACs. The source DAC is selected by programming the two MSBs of the WSCR register.
DFLT/$\overline{DFLT}$		PLL LOOP FILTER: These pins are the connection points for the data separator loop filter.
LEVEL		An NPN emitter output that provides a full-wave rectified signal from the DP, DN inputs. An external capacitor should be connected from LEVEL to VPG to set the hysteresis threshold time constant in conjunction with RTS and RTD. An internal current source provides 60 µA of pull-down current at this pin.
RR		REFERENCE RESISTOR INPUT: An external 1% resistor is connected from this pin to VNA to establish a precise internal reference current for the data separator and time base generator.
RTS		SERVO TIME CONSTANT RESISTOR INPUT: An external resistor is connected from this pin to LEVEL to establish the hysteresis threshold time constant when in Servo mode.
RTD		DATA TIME CONSTANT RESISTOR INPUT: An external resistor is connected from this pin to LEVEL to establish the hysteresis threshold time constant when not in Servo mode.

ANALOG PINS (continued)

RX		REFERENCE RESISTOR INPUT: An external 1% resistor is connected from this pin to VNG to establish a precise PTAT (proportional to absolute temperature) reference current for the filter. A 1000 pF capacitor should be placed in parallel with this resistor.
MAXREF		SERVO REFERENCE: An external voltage output that can be used as the reference for an external A/D converter. This represents the maximum output voltage for the A, B, C, and D outputs.

SERIAL PORT PINS

SDEN		SERIAL DATA ENABLE: Serial enable CMOS input. A high level input enables the serial port.
SDATA		SERIAL DATA: Serial data CMOS input. NRZ programming data for the internal registers is applied to this input.
SCLK		SERIAL CLOCK: Serial clock CMOS input. The clock applied to this pin is synchronized with the data applied to SDATA.

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, the recommended operating conditions are as follows: 4.5V < POSITIVE SUPPLY VOLTAGE < 5.5V, 0°C < T (ambient) < 70°C, and 25°C < T(junction) < 135°C. Currents flowing into the chip are positive. Current maximums are currents with the highest absolute value.

ABSOLUTE MAXIMUM RATINGS

Operation beyond the maximum ratings may damage the device

Storage temperature	-65 to 150°
Junction operating temperature	+130°C
Positive supply voltage (Vp)	-0.5 to 7V
Voltage applied to any pin	-0.5V to Vp+0.5V

ELECTRICAL SPECIFICATIONS (continued)

POWER SUPPLY CURRENT AND POWER DISSIPATION

Unless otherwise specified, Ta = 26°C and data rate = max. All test points and outputs are open. The test points are disabled.

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
ICC	VPn	$\overline{PWRON}$ = 0 All blocks enabled		85	125	mA
PWR Power Dissipation		$\overline{PWRON}$ = 0 All blocks enabled		425	690	mW
Sleep Mode Current		$\overline{PWRON}$ = 1 SG, RG, WG, STROBE, $\overline{RESET}$, WCLK = 0 All other CMOS inputs = 1			0.5	mA
Servo Mode Current		$\overline{PWRON}$ = 0 SG = 1 Power Reg. = 14 hex		45	70	mA

DIGITAL INPUTS AND OUTPUTS

TTL COMPATIBLE INPUTS

Inputs will float high "1" if left open.

Input low voltage	VIL				0.8	V
Input high voltage	VIH		2.0			V
Input low current	IIL	VIL = 0.4V			-20	µA
Input high current	IIH	VIH = 2.4V			-20	µA

CMOS COMPATIBLE INPUTS

Schmitt trigger type, do not leave open. Nominal 1.0V hysteresis around VPD/2.

Input low voltage	VPC = 5.0 volts			1.5	V
Input high voltage	VPC = 5.0 volts	3.5			V

CMOS COMPATIBLE OUTPUTS

Output low voltage	IOL = 4.0 mA, VPD = 5.0V			0.5	V
Output high voltage	IOH = -4.0 mA, VPD = 5.0V	4.5			V
Rise time	0.8 to 2.0 volts CL ≤ 15 pF			5	ns
Fall time	2.0 to 0.8 volts CL ≤ 15 pF			5	ns

FREF INPUT

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Recommended input level	AC-coupled	1.5		2.0	Vp-p
Input resistance	Ref. only, not measured on ATE		11		kΩ

TEST POINT OUTPUT LEVELS (MTP1, MTP2, MTP3)

Output high level	261Ω to VPA 402Ω to VNA for reference use only	VPA - 1.0			V
Output low level	261Ω to VPA 402Ω to VNA for reference use only			VPA - 1.62	V

PECL OUTPUT LEVELS (WD,$\overline{WD}$ for 32P4742A)

Output high level	402Ω to VND	VPA - 1.0			V
Output low level	402Ω to VND			VPA - 1.60	V

SERIAL PORT

SCLK Data Clock period		Read from Serial Port	140			ns
		Write to Serial Port	100			ns
SCLK low time	TCKL	Read from Serial Port	60			ns
		Write to Serial Port	40			ns
SCLK high time	TCKH	Read from Serial Port	60			ns
		Write to Serial Port	40			ns
Enable to SCLK	TSENS		35			ns
SCLK to disable	TSENH		100			ns
Data set-up time	TDS		15			ns
Data hold time	TDH		15			ns
SDATA tri-state delay	TSENDL				50	ns
SDATA turnaround time	TTRN		70			ns
SCLK falls to Valid Data	TDSKEW	Cload ≤ 15 pF	0		50	ns
SDEN low time	TSL		200			ns

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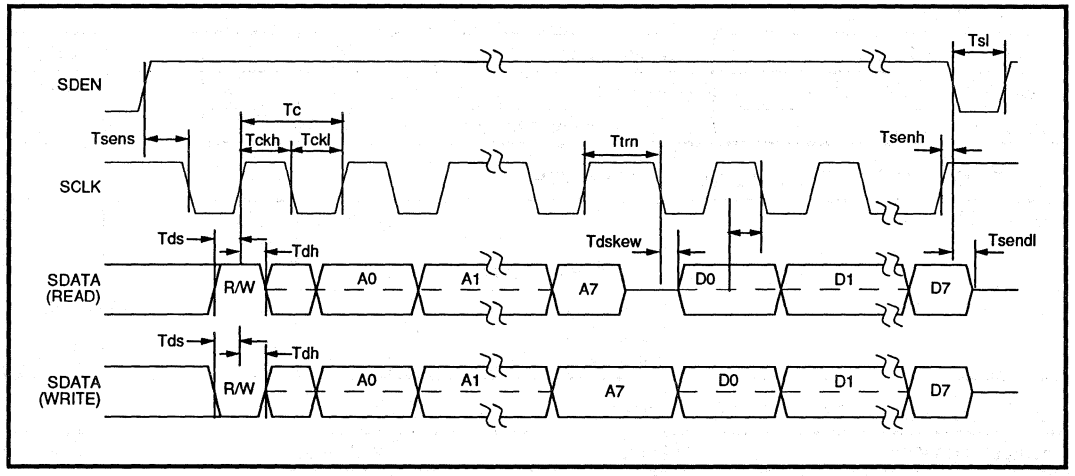

FIGURE 18: Serial Port Timing

ELECTRICAL SPECIFICATIONS (continued)

PULSE DETECTOR CHARACTERISTICS

AGC AMPLIFIER

Input signals are AC coupled to VIA/$\overline{\text{VIA}}$, VOA/$\overline{\text{VOA}}$ outputs are AC coupled to IN/$\overline{\text{IN}}$, and ON/$\overline{\text{ON}}$ are AC coupled to DP/DN. A 1000 pF capacitor (CBYP) is connected from BYP to VPG. Unless otherwise specified, outputs are measured differentially at VOA/$\overline{\text{VOA}}$, FIN = 8 MHz, and filter boost = 0 dB.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Input range	Fin = Fc, 0 dB boost	22		240	mVpp
	13 dB boost	20		100	mVpp
DP-DN voltage	22 ≤ VIA ≤ 240 mVpp $\overline{\text{HOLD}}$ = 1, boost = 0 dB	0.85		1.15	Vpp
	20 ≤ VIA ≤ 100 mVpp $\overline{\text{HOLD}}$ = 1, boost = 13 dB	0.85		1.15	Vpp
DP-DN voltage (servo)	SG = 1, DACA = 0000	0.85	1.0	1.15	Vpp
	SG = 1, DACA = 1111	0.60	0.75	0.90	Vpp
AGC gain minimum	$\overline{\text{HOLD}}$ = 0 I @ BYP = -50 µA			1.0	V/V
AGC gain maximum	I @ BYP = +50 µA	22			V/V
Gain sensitivity	BYP voltage change	23	28	33	dB/V
AGC output total harmonic distortion	VOA-$\overline{\text{VOA}}$ = 0.75 Vpp VIA = 100 mVp-p			1.0	%

AGC AMPLIFIER (continued)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Differential input impedance	WG = low	4.7	6.0	8.4	kΩ
	WG = high; or Low-Z	100	350	600	Ω
Single-ended input impedance	WG = low	2.5	3.3	5.0	kΩ
	WG = high; or Low-Z	150	250	350	Ω
Output offset voltage	Gain = 1.0 to 22			200	mV
Input noise voltage	Gain = 22, VIA/$\overline{\text{VIA}}$ are shorted		10	15	nV/√Hz
Bandwidth	Gain = 22, CL ≤ 15 pF	35			MHz
CMRR	Gain = 22, F = 5 MHz	40			dB
PSRR	Gain = 22, Fc = 5MHz	45			dB
Single-ended output resistance			125	275	Ω

AGC CONTROL

The input signals are AC coupled into DN/DP, CBYP = 1000 pF to VPA. CT = 10000 pF, RTS = RTD = open.

Decay current	VBYP = VPG - 2.3V, DP-DN = 0V Normal decay (ID)	-3.0	-4.0	-5.0	µA
	Fast Decay mode (IDF)	-0.8	-1.2	-1.6	mA
Attack current	VBYP = VPG - 2.3V Normal attack (ICH) DP-DN = 0.55V	0.13	0.17	0.22	mA
	Fast Attack mode (ICHF) DP-DN = 0.675V	7x ICH	8 x ICH	9.6 x ICH	mA
BYP leakage current	$\overline{\text{HOLD}}$ = 0, 1 ≤ Gain ≤ 22	-50		50	nA
Low-Z duration	WG 1 to 0 Low-Z bit = 0	0.5	1.0	1.5	µs
	Low-Z bit = 1		2.0		µs
Fast decay duration	Low-Z bit = 0	0.5	1.0	1.5	µs
	Low-Z bit = 1		2.0		µs
LEVEL output voltage (with respect to RTD/RTS)	FIN = 6 to 18 MHz |DP-DN| = 0.5	0.29	0.33	0.37	V/Vpp
	|DP-DN| = 1.0	0.60	0.67	0.74	V/Vpp
	|DP-DN| = 1.5	0.88	1.0	1.12	V/Vpp
LEVEL pull-down current	Vlevel = VPG - 2.3V	40	60	80	µA

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ELECTRICAL SPECIFICATIONS (continued)

DATA COMPARATOR

The input signals are AC coupled into DP/DN.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Differential input resistance	WG = 0	6.5	9	12.5	kΩ
Single-ended input resistance	WG = 1	200	500	725	Ω
Threshold (T%) accuracy	41 < VTHDAC < 109 0.3 ≤ VLEVEL - VRTD ≤ 0.75 T% = TnDAC x 93%/127	T% - 5		T% + 5	%

CLOCK SECTION

The input signals are AC coupled into CP/CN.

Differential input resistance		6.5	9	12.5	kΩ
Pulse pairing	Data threshold register = 196 and 63 Measured at the falling edge of $\overline{RDIO}$ Data rate = 16 Mbit/s Fc = 9 MHz, 0 dB boost VIA = 100 mVpp @6 MHz			0.6	ns

SERVO CAPTURE CHARACTERISTICS

Unless otherwise specified: a 4 MHz sine wave is AC-coupled into DP/DN inputs; STROBE and $\overline{RESET}$ durations are 1.0 µs; and DACP is set to "0100" with the Servo Reset bit set to "1".

MAXREF output voltage	ISOURCE = 0 mA	2.94	3.1	3.26	V
MAXREF load regulation	ISOURCE = 0 to -4.5 mA			40	mV
A, B, C, D output low voltage	ISINK = 0.2 mA $\overline{RESET}$ = 0	0.16 x MAXREF	0.17 x MAXREF	0.18 x MAXREF + 0.15	V
MAXREF-A,B,C,D high voltage	ISOURCE = 0 mA	0			V
A, B, C, D output resistance	ISOURCE/SINK = 0.2 mA			50	Ω
A, B, C, D gain	0.2 Vpp < (DP - DN) ≤ 1.0 Vpp	2.15	2.25	2.35	V/V
	0.0 Vpp ≤ (DP - DN) ≤ 0.2 Vpp	0		2.35	V/V
SREF input range		0.35 x VPG	0.4 x VPG	0.55 x VPG	V
SREF input bias current	0.35 x VPG ≤ SREF ≤ 0.55 x VPG		0.2	1.0	µA
A-B, C-D, A+B high voltage		VPG - 0.75			V
A-B, C-D, A+B low voltage				0.5	V

SERVO CAPTURE CHARACTERISTICS (continued)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
A-B, C-D gain	0.2 Vpp < (DP - DN) ≤ 1 Vpp	1.8	2.0	2.2	V/V
	0 Vpp ≤ (DP - DN) ≤ 0.2 Vpp	0		2.2	V/V
A+B gain	0.2 Vpp < (DP - DN) ≤ 1 Vpp	0.9	1.0	1.1	V/V
	0 Vpp ≤ (DP - DN) ≤ 0.2 Vpp	0		1.1	V/V
A-B, C-D, offset voltage	DP/DN = 0.5 Vpp Offset = |output ($\overline{\text{RESET}}$ = 0) - output ($\overline{\text{RESET}}$ = 1)|			30	mV
Burst capture time	DP - DN = 1.0 Vpp Output ≥ 95% of final value			1.0	µs
Burst reset time	DP - DN = 1.0 Vpp Output ≤ 5% of final value			1.0	µs
$\overline{\text{RESET}}$ on/off delay	From $\overline{\text{RESET}}$ 1.4V crossing			150	ns
A,B,C,D offset voltage	DP-DN = 0.5 Vpp, $\overline{\text{RESET}}$ = 1 Offset = difference between any two channels			60	mV
$\overline{\text{RDIO}}$ pulse width	CL = 15 pF Measured at 1.5V crossing	10		15	ns
PPOL to $\overline{\text{RDIO}}$ setup time	PPOL rise/fall to $\overline{\text{RDIO}}$ fall measured @ 1.5V crossing CL ≤ 15 pF	8			ns

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ELECTRICAL SPECIFICATIONS (continued)

PROGRAMMABLE FILTER CHARACTERISTICS

Unless otherwise specified: Rx = 12.1 kΩ, Cx = 1000 pF from Rx pin to VNG. Input signals are AC-coupled into IN/$\overline{IN}$.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Filter cutoff range	Fc @ -3 dB point Fc = (0.1417 MHz) x DACF Boost = 0 dB, 42 < DACF < 127	6		18	MHz
Filter cutoff accuracy	DACF = 42 and 127	-15		15	%
ON differential gain AN	F = 0.67 x Fc, boost = 0 dB DACF = 42 and 127	1.5	2.0	2.5	V/V
OD differential gain AD	F = 0.67 x Fc, boost = 0 dB DACF = 42 and 127	0.8 x AN		1.2 x AN	V/V
Frequency boost @ Fc	DACS = 127		13		dB
Boost accuracy	6 dB, DACF = 42, DACS = 36	-1		+1	dB
	6 dB, DACF = 127, DACS = 30	-1		+1	dB
	9 dB, DACF = 42, DACS = 67	-1.25		+1.25	dB
	9 dB, DACF = 127, DACS = 59	-1.25		+1.25	dB
	13 db, DACF = 42, DACS = 111	-1.5		+1.5	dB
	13 db, DACF = 127, DACS = 100	-1.5		+1.5	dB
Group delay variation	F = 0.2 Fc to Fc DACF = 42 and 127 Boost = 0 and 3 dB	-2		2	%
	F = Fc to 1.75 Fc DACF = 42 and 127 Boost = 3 dB	-3		3	%
OD output THD @ 1 Vpp	F = 0.67 Fc, DACF = 42 and 127			1.5%	Vpp
Differential input resistance	WG = 0	5.0	6.5	8.0	kΩ
	WG = 1	100	300	600	Ω
Single-ended output resistance			100	200	Ω
Output sink current		0.5			mA
Differential output offset	@ ON/$\overline{ON}$, DACF = 42 and 127			200	mV
Output noise voltage ON/$\overline{ON}$ output	BW = 100 MHz, Rs = 50Ω DACF = 127, boost = 0 dB		2.2	3.3	mV Rms
ON/$\overline{ON}$ output	DACF = 127, boost = 13 dB		3.2	4.8	mV Rms
OD/$\overline{OD}$ output	DACF = 127, boost = 0 dB		3.8	5.7	mV Rms
OD/$\overline{OD}$ output	DACF = 127, boost = 13 dB		6.9	10.4	mV Rms

TIME BASE GENERATOR CHARACTERISTICS

Unless otherwise specified: RR = 12.1 kΩ. Loop filter values are R = 453Ω, C1 = 0.47 µF, and C2 = 0.047 µF. Clock source is AC coupled into FREF, 1.5 ≤ VFREF ≤ 2.0 Vpp.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
FREF input range	TRISE/TFALL ≤ 5 ns	8		20	MHz
FREF input low time		20			ns
FREF input high time		20			ns
M counter range		2		255	
N counter range		2		127	
Output frequency	FREF = 20 MHz			75	MHz
Output jitter	≥ 10K samples			200	psec(RMS)
VCO center frequency FTBG	TFLT - $\overline{TFLT}$ = 0V FTBG = [12.5/(RR + 0.4)] x [(0.614 x IDAC) + 3.84] MHz	0.85 x TBG		1.15 x TBG	MHz
VCO dynamic range	-2V < TFLT - $\overline{TFLT}$ < +2V FVCO = 48 MHz	±25		±45	%
VCO control gain KVCO	ωi = 2π x FVCO -1.0V ≤ TFLT - $\overline{TFLT}$ ≤ +1.0V	0.12 ωi		0.24 ωi	rad/(V-S)
Phase detector gain KD	KD = [12.5/(RR + 0.4)] x [0.633 x IDAC + 0.92] PDCR D1 = 1, KD = 1x PDCR D1 = 0, KD = 3x	0.83 x KD		1.17 x KD	µA/rad
KVCO x KD product accuracy		-28		+28	%

6

ELECTRICAL SPECIFICATIONS (continued)

DATA SEPARATOR CHARACTERISTICS

Unless otherwise specified, RR = 12.1 kΩ. Loop filter components are R = 1.82 kΩ, C1 = 270 pF, and C2 = 27 pF. Data Rate = 48 Mbit/s.

READ MODE

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Read clock rise time	TRRC	0.8 to 2.0V, CL ≤ 15 pF			5	ns
Read clock fall time	TFRC	2.0 to 0.8V, CL ≤ 15 pF			5	ns
RRC duty cycle	TRD	1.5V - 1.5V, CL ≤ 15 pF	40		60	%
NRZ set-up/hold	TNS/TNH		8			ns
NRZ propagation delay	TPNRZ		-5		5	ns
Phase Window Centering		At 16 and 48 Mbit/s Difference between early, late phase reversal points / phase window	-20		+20	%

WRITE MODE

The $\overline{WD}$ information is for the 32P4742. 32P4742A WD information will be added.

$\overline{WD}$ rise time	TRWD	0.8 to 2.0V CL ≤ 15 pF			5	ns
$\overline{WD}$ fall time	TFWD	2.0 to 0.8V CL ≤ 15 pF			5	ns
$\overline{WD}$ jitter		WD out = fixed 2T pattern			500	psec(RMS)
Required WCLK rise time	TRWC	0.8 to 2.0V			10	ns
Required WCLK fall time	TFWC	2.0 to 0.8V			8	ns
NRZ set-up time	TSNRZ		5			ns
NRZ hold time	THNRZ		5			ns
$\overline{WD}$ pulse width	TWD	Without precomp, TW = 1/FTBG CL ≤ 15 pF	0.82 x TW		1.18 x TW	ns
Write Precomp magnitude accuracy		TPCO = 0.04/FTBG TPC = n X TPCO 0 ≤ n ≤ 7	0.8 x TPC - 1		1.2 x TPC + 1	ns

DATA SYNCHRONIZATION

Unless otherwise specified: RR = 12.1 kΩ. Loop filter values are R = 1.82 kΩ, C1 = 270 pF, and C2 = 27 pF. Clock source is AC coupled into FREF, 1.5 ≤ VFREF ≤ 2.0 Vpp.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
VCO center frequency FVCO	DFLT - $\overline{DFLT}$ = 0 V FVCO = [12.5/(RR+0.4)] x [(0.614 x IDAC) + 3.84] MHz	0.85 x FVCO		1.15 x FVCO	MHz
VCO dynamic range	-2V < DFLT - $\overline{DFLT}$ < +2V at 72 MHz	±25		±45	%
VCO control gain KVCO	ωi = 2π/TVCO -1.0V < DFLT- $\overline{DFLT}$ < +1.0V at 72 MHz	0.14 ωi	0.175 ωi	0.26 ωi	rad/(V-S)
Phase detector gain KD	KD = [12.5/(RR + 0.4)] x [0.633 x IDAC + 0.92] RG = 1, gain shift: KD = 1x RG = 1, no gain shift: KD = 3x RG = 0: KD = 1x	0.83 x KD		1.17 x KD	µA/rad
KVCO x KD product accuracy		-28		+28	%
VCO phase restart error		-2		+2	ns
Decode window center accuracy	Based on 50% error points at 48 Mbit/s	-0.75		0.75	ns
Decode window width	Based on 15% error rate Data rate = 48 Mbit/s	1/FVCO - 0.75			ns
Decode window shift magnitude accuracy	TWSO = 0.02/FVCO TWS = n x TWSO 0 ≤ n ≤ 15	0.8 x TWS - 1		1.2 x TWS + 1	ns

ELECTRICAL SPECIFICATIONS (continued)

WINDOW SHIFT CONTROL

Window shift magnitude is set by the value in the Window Shift (WS) register. The WS register bits are as follows:

BIT	NAME	FUNCTION
0	$\overline{WS0}$	
1	$\overline{WS1}$	
2	$\overline{WS2}$	
3	$\overline{WS3}$	
4	WSD	Window shift direction. 0 = early, 1 = late
5	WSE	Window shift enable
6	TDAC0	Used to route signals to DAC test point
7	TDAC1	Used to route signals to DAC test point

The window shift magnitude is set as a percentage of the decode window, in 2% steps. Window shift should be set during non-read mode.

$\overline{WS3}$	$\overline{WS2}$	$\overline{WS1}$	$\overline{WS0}$	SHIFT MAGNITUDE
1	1	1	1	No shift
1	1	1	0	2% (minimum shift)
1	1	0	1	4%
1	1	0	0	6%
1	0	1	1	8%
1	0	1	0	10%
1	0	0	1	12%
1	0	0	0	14%
0	1	1	1	16%
0	1	1	0	18%
0	1	0	1	20%
0	1	0	0	22%
0	0	1	1	24%
0	0	1	0	26%
0	0	0	1	28%
0	0	0	0	30% (maximum shift)

WRITE PRECOMP CONTROL

Write precomp magnitude is set by the value in the Write precomp (WP) register. The WP register bits are as follows:

BIT	NAME	FUNCTION	BIT	NAME	FUNCTION
0	$\overline{WE0}$	Early bit 0	4	$\overline{WL0}$	Late bit 0
1	$\overline{WE1}$	Early bit 1	5	$\overline{WL1}$	Late bit 1
2	$\overline{WE2}$	Early bit 2	6	$\overline{WL2}$	Late bit 2
3	WPE	Write precomp enable			

The write precomp magnitude is calculated as:

$$TPC = n \times 0.04/F_{TBG}$$

where n = precomp magnitude scaling factor as shown below. T_{TBG} is the period of the reference frequency provided by the internal time base generator.

$\overline{W2}$	$\overline{W1}$	$\overline{W0}$	PRECOMP MAGNITUDE SCALING FACTOR
1	1	1	No precomp
1	1	0	1X
1	0	1	2X
1	0	0	3X
0	1	1	4X
0	1	0	5X
0	0	1	6X
0	0	0	7X (maximum)

BIT N-2	BIT N-1	BIT N	BIT N+1	BIT N+2	BIT N COMPENSATION
1	0	1	0	1	None
0	0	1	0	0	None
1	0	1	0	0	Early
0	0	1	0	1	Late

Late = Bit N is time shifted toward the N+1 bit by the programmed magnitude
Early = Bit N is time shifted toward the N-1 bit by the programmed magnitude

ELECTRICAL SPECIFICATIONS (continued)

TABLE 5: 1,7 RLL ENCODE TABLE (X = Don't care)

NRZ DATA				ENCODED WRITE DATA			
Present Bits		Next Bits		Previous	Present		
NRZ1	NRZ0	NRZ1'	NRZ0'	Y3	Y1	Y2	Y3
0	0	0	X	X	0	0	1
0	0	1	X	0	0	0	0
0	0	1	X	1	0	1	0
1	0	0	X	X	1	0	1
1	0	1	X	X	0	1	0
0	1	0	0	0	0	0	1
0	1	0	0	1	0	1	0
0	1	1	0	X	0	0	0
0	1	0	1	0	0	0	1
0	1	0	1	1	0	0	0
0	1	1	1	X	0	0	0
1	1	0	0	0	0	1	0
1	1	1	0	0	1	0	0
1	1	0	1	0	1	0	0
1	1	1	1	0	1	0	0

TABLE 6: 1,7 RLL DECODE TABLE (X = Don't care)

ENCODED READ DATA					DECODED DATA				
Previous		Present			Next				
Y2'	Y3'	Y1	Y2	Y3	Y1	Y2	NRZ1	NRZ0	
0	0	0	0	0	X	X	0	1	
1	0	0	0	0	X	X	0	0	
0	1	0	0	0	X	X	0	1	
X	X	1	0	0	X	X	1	1	
X	0	0	1	0	0	0	1		
X	0	0	1	0	1	0	1	0	
X	0	0	1	0	0	1	1	0	
X	1	0	1	0	0	0	0	1	
X	1	0	1	0	1	0	0	0	
X	1	0	1	0	0	1	0	0	
0	0	0	0	1	X	X	0	1	
1	0	0	0	1	X	X	0	0	
0	1	0	0	1	X	X	0	0	(Preamble)
X	X	1	0	1	X	X	1	0	

TABLE 7: CLOCK SOURCE AND FREQUENCY VS. MODE

WG	RG	VCO REF	RCLK	DECODE CLOCK	ENCODE CLOCK	MODE
0	0	FOUT	2FOUT/3	FOUT	FOUT	IDLE
0	1	$\overline{DRD}$	2VCO/3	VCO	FOUT	READ
1	0	FOUT	2FOUT/3	FOUT	FOUT	WRITE

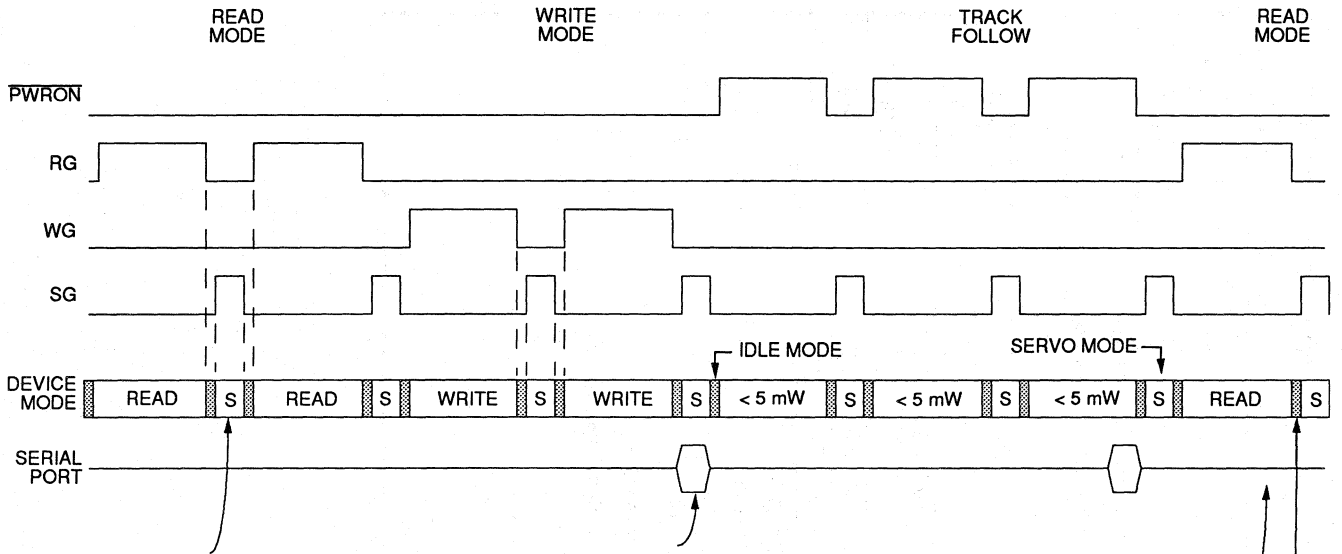
NOTE 1: Until the VCO locks to the new source, the VCO entries will be FOUT.

NOTE 2: Until the VCO locks to the new source, the 2VCO/3 entries will be 2FOUT/3.

TABLE 8: MULTIPLEXED TEST POINT SIGNAL SELECTION

MTPEn	TMS1	TMS0	MTP1	MTP2	MTP3
0	X	X	OFF	OFF	OFF
1	0	0	VCOREF	DSIN	SRD
1	0	1	RD	DOUT	DSREF
1	1	0	PDQ	$\overline{PUQ}$	SRD
1	1	1	SET	RESET	NCTR

DOUT = Output of the pulse qualifier data comparators
$\overline{DSIN}$ = Input to the data synchronizer phase detector
DSREF = Output of the time base generator
NCTR = N counter output of the time base generator
PDQ = Data separator phase detector pump down edge
$\overline{PUQ}$ = Data separator phase detector pump up edge (inverted)
RD = Read data output from the pulse qualifier
RESET = Output of the negative threshold comparator
SET = Output of the positive threshold comparator
SRD = Synchronized read data
VCOREF = Data separator VCO reference clock



NOTES:

1) When the PWRON pin is LOW ("0") the Power Down Control Register is active. All blocks that have their control bit set to "1" will be powered down. When the PWRON pin is HIGH ("1") the device goes into a Sleep mode with all blocks powered down except the serial port.

2) When the threshold DAC reference is switched, there is a maximum settling time of 1.5 µs for the DAC.

FIGURE 19: Power Control Timing

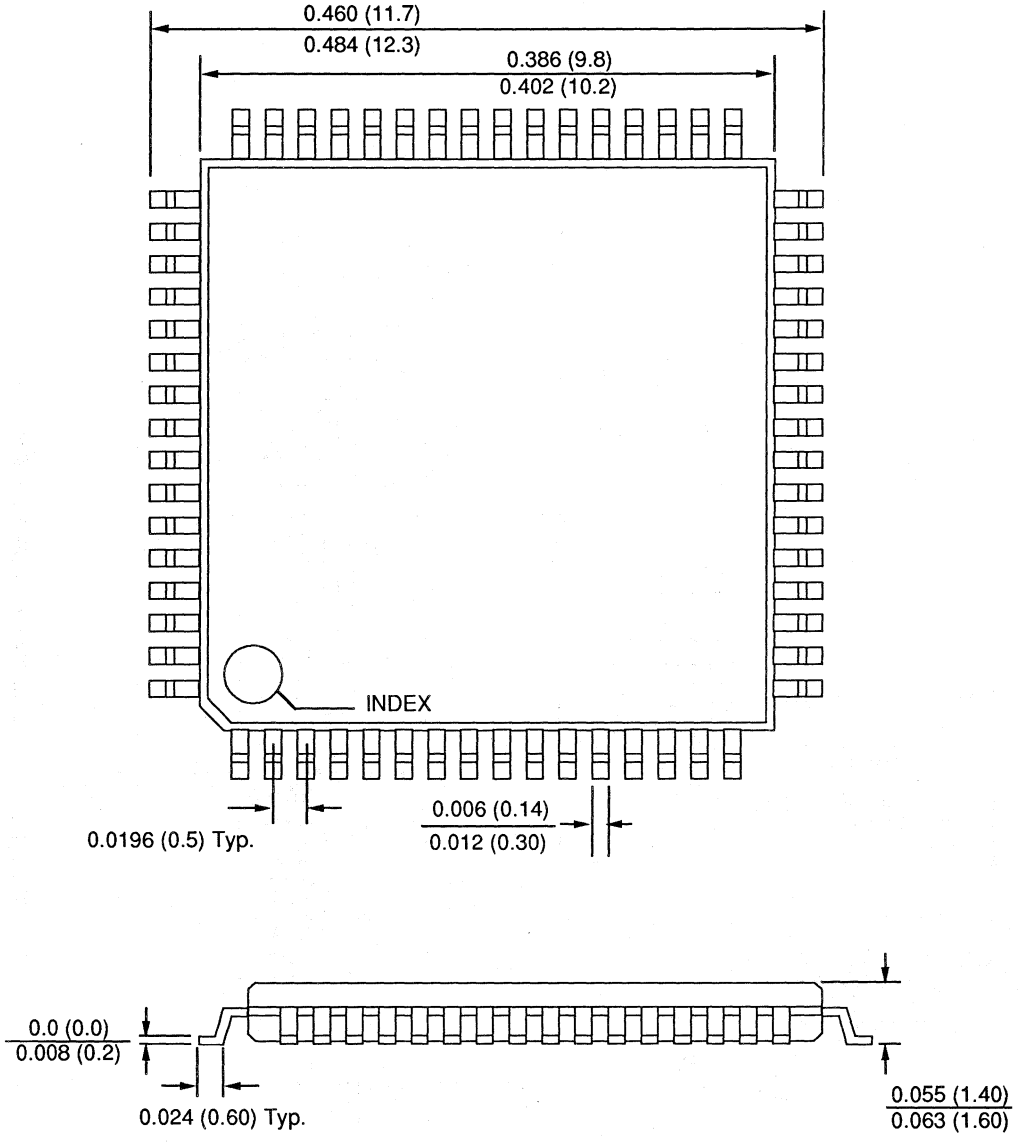


FIGURE 20: Package Information
64-Lead Thin Quad Flatpack (TQFP)

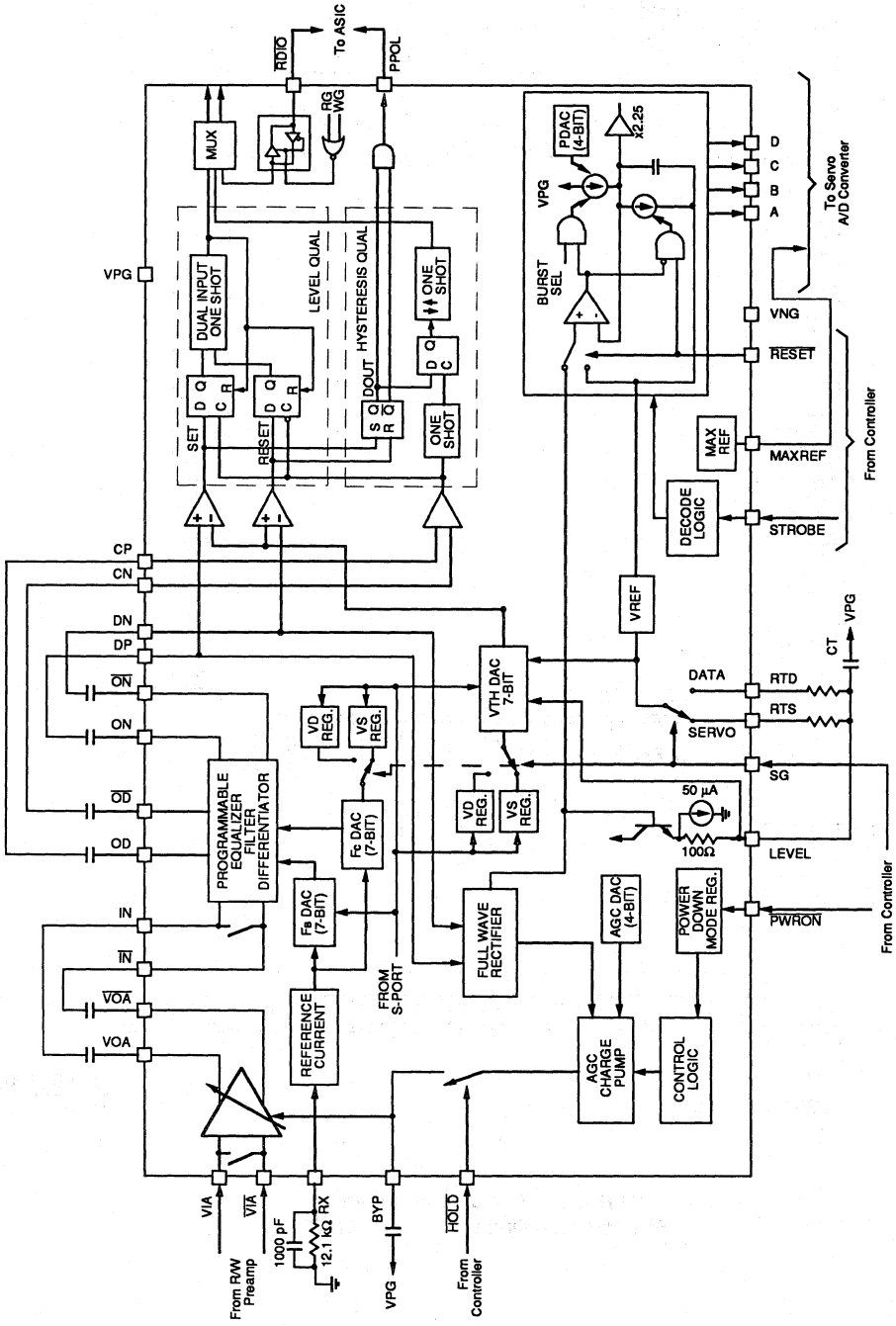


FIGURE 21(a): 32P4742/32P4742A Application Diagram

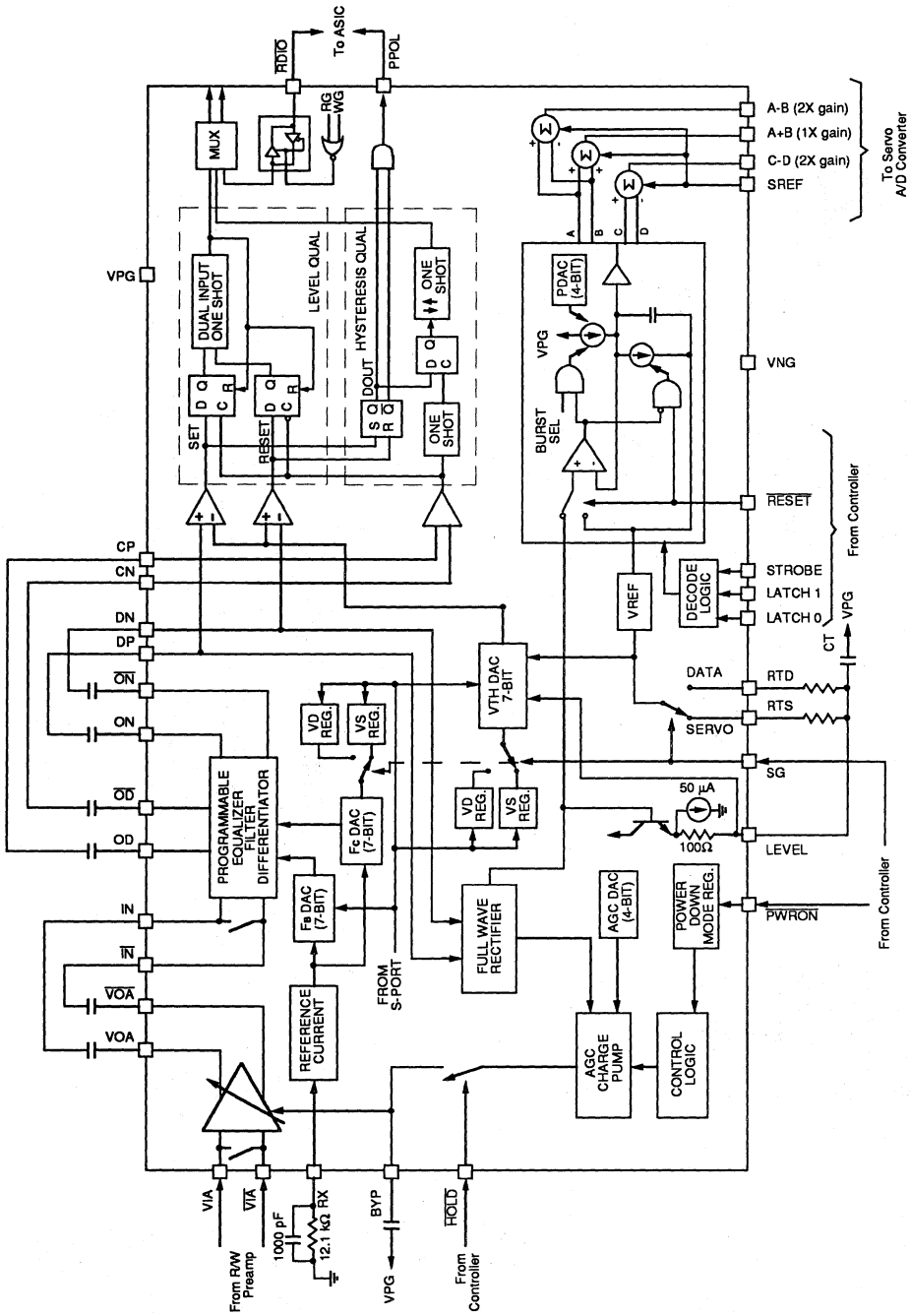


FIGURE 21(b): 32P4746/32P4746A Application Diagram

6

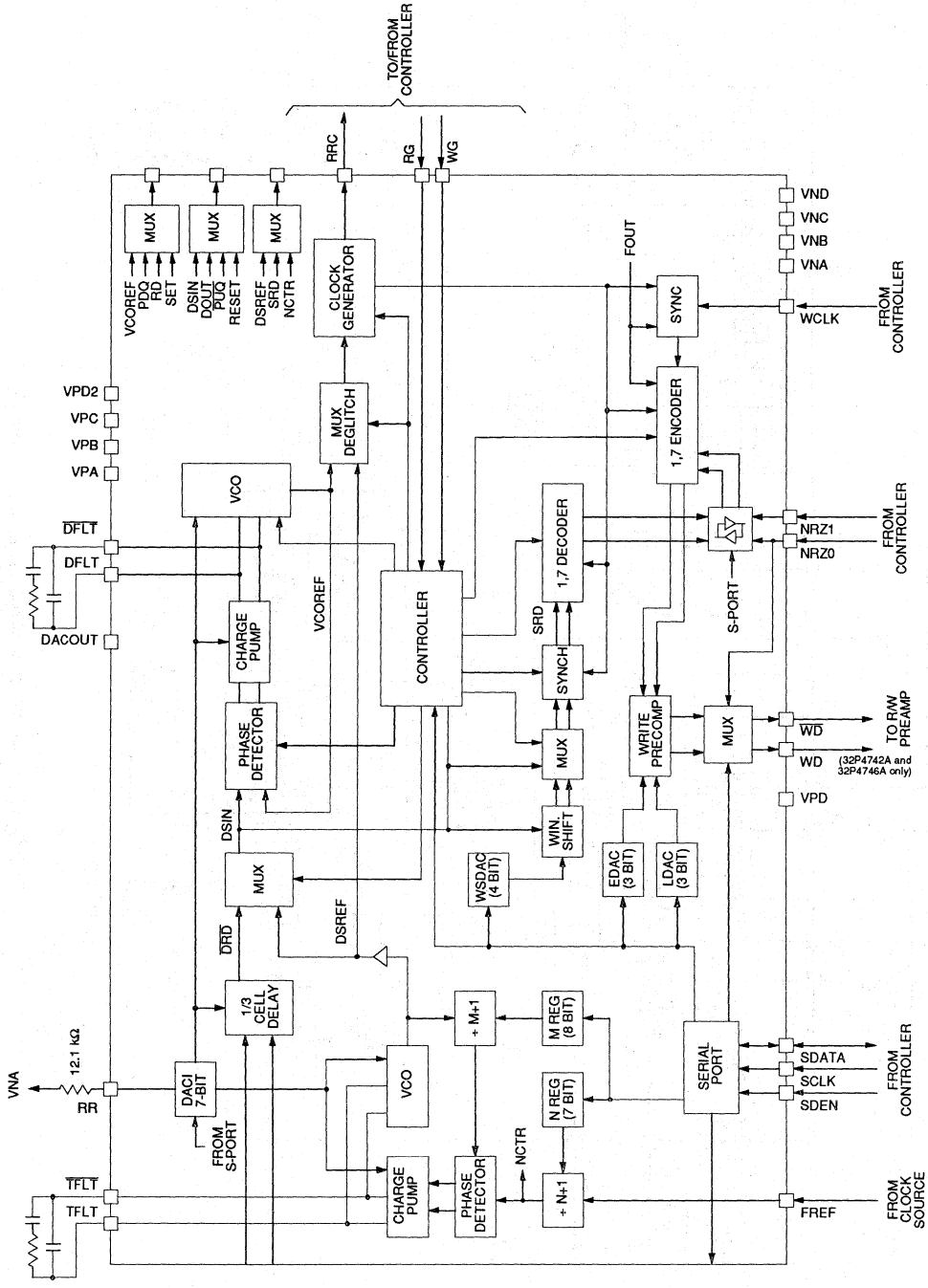
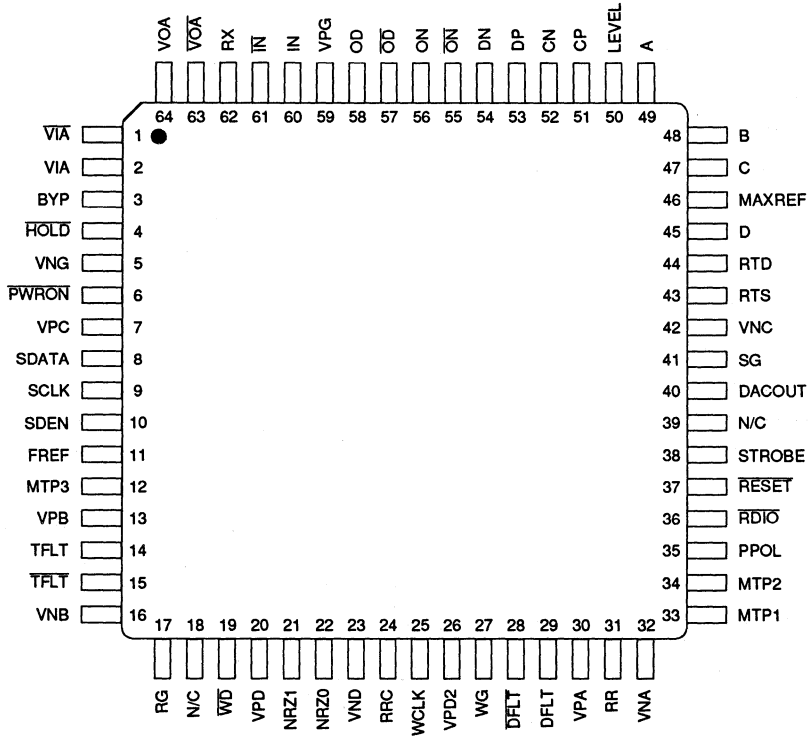


FIGURE 21(c): 32P4742/32P4742A/4746/4746A Application Diagram

PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



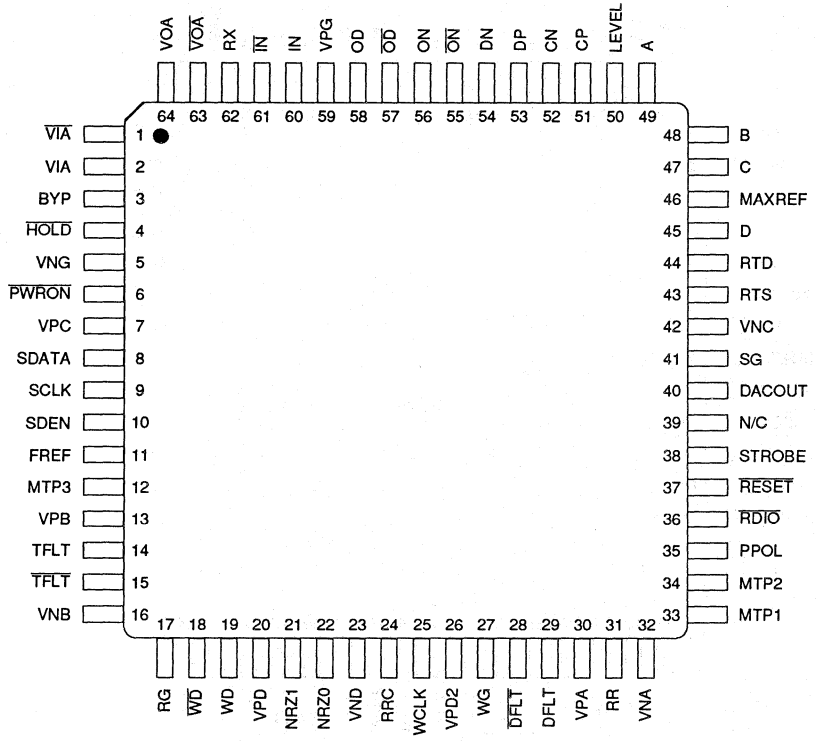
32P4742
64-Lead TQFP

6

SSI 32P4742/4742A/4746/4746A
Read Channel with
1,7 ENDEC, 4-burst Servo

PACKAGE PIN DESIGNATIONS
(Top View)

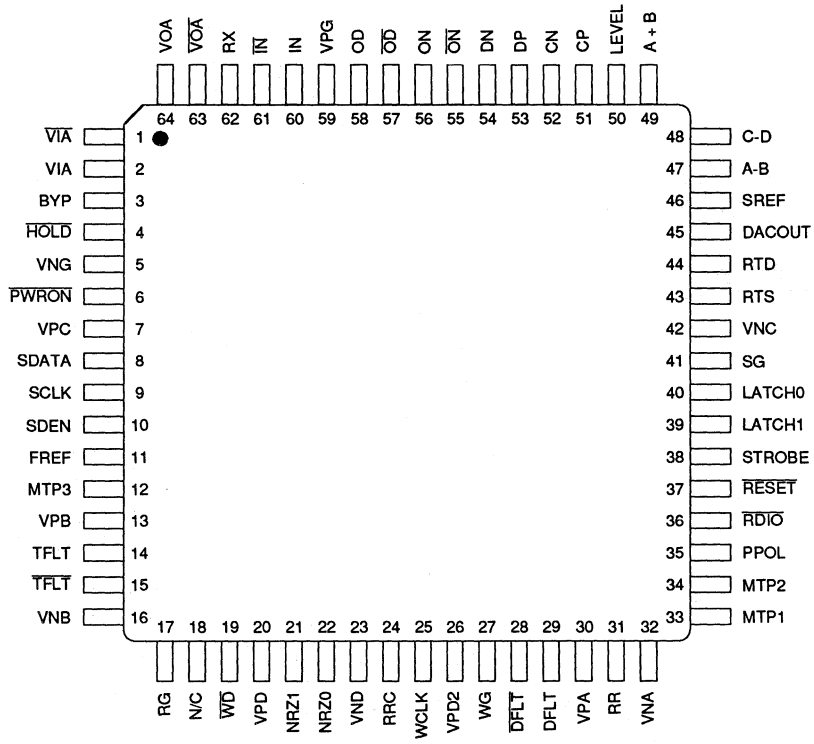
CAUTION: Use handling procedures necessary for a static sensitive component.



32P4742A
64-Lead TQFP

PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



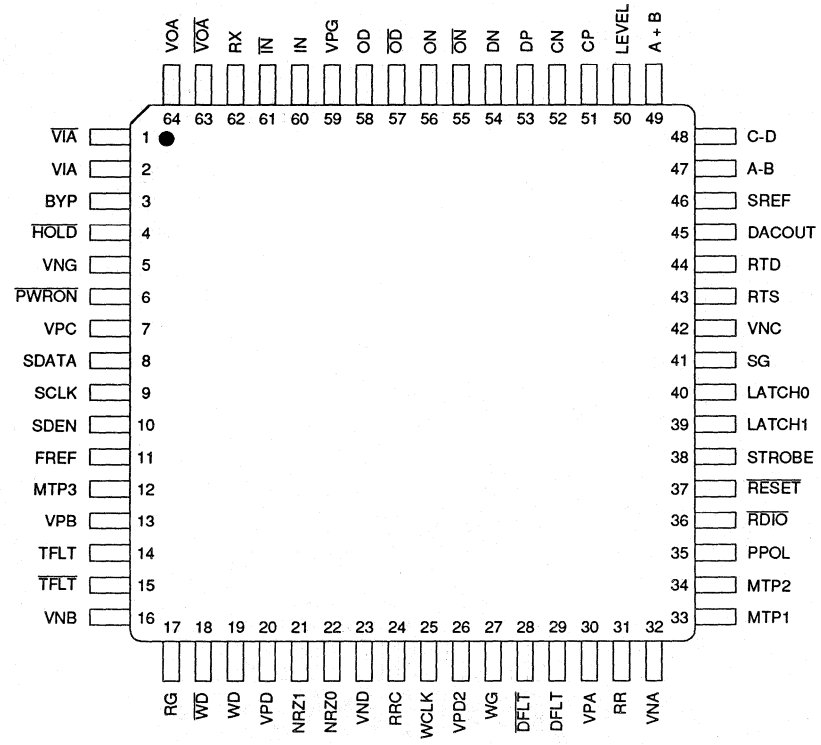
32P4746
64-Lead TQFP

6

SSI 32P4742/4742A/4746/4746A
Read Channel with
1,7 ENDEC, 4-burst Servo

PACKAGE PIN DESIGNATIONS
(Top View)

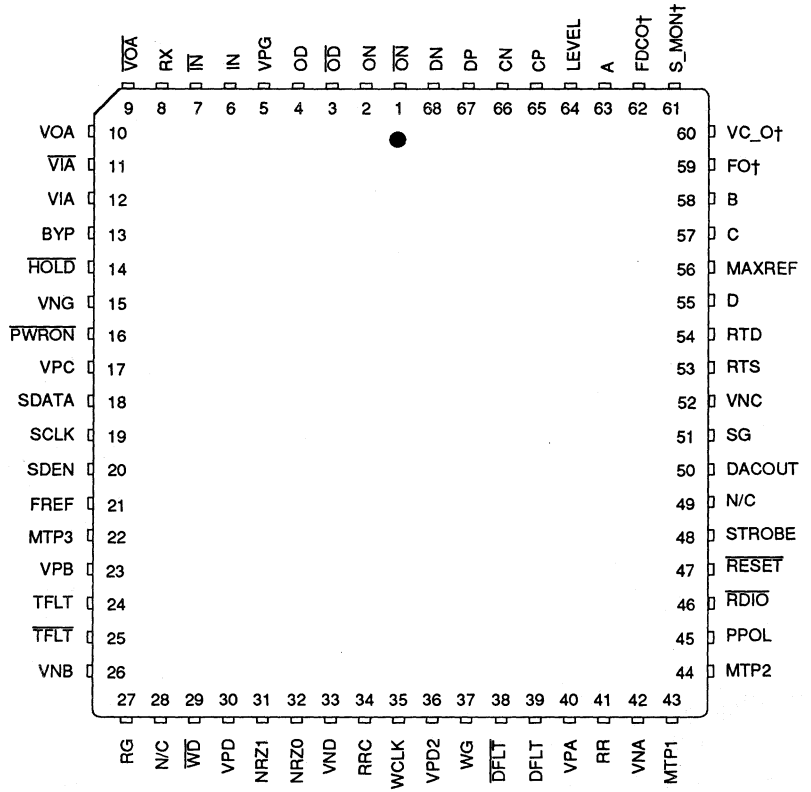
CAUTION: Use handling procedures necessary for a static sensitive component.



32P4746A
64-Lead TQFP

PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



†These pins are for SSi test purposes only.
They should be left open in normal use.

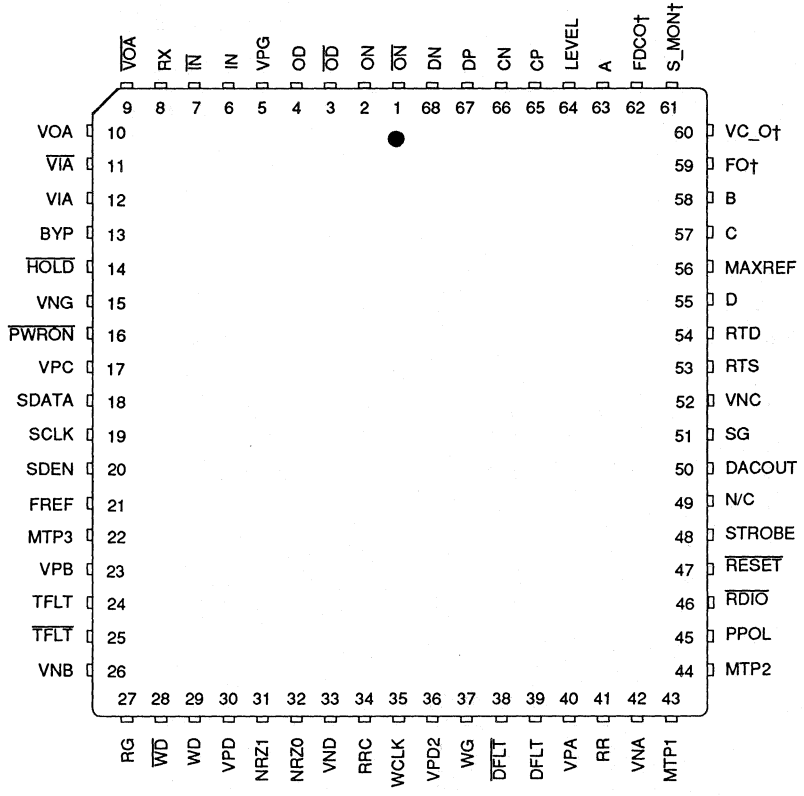
32P4742
68-Pin CLCC

6

SSI 32P4742/4742A/4746/4746A
Read Channel with
1,7 ENDEC, 4-burst Servo

PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.

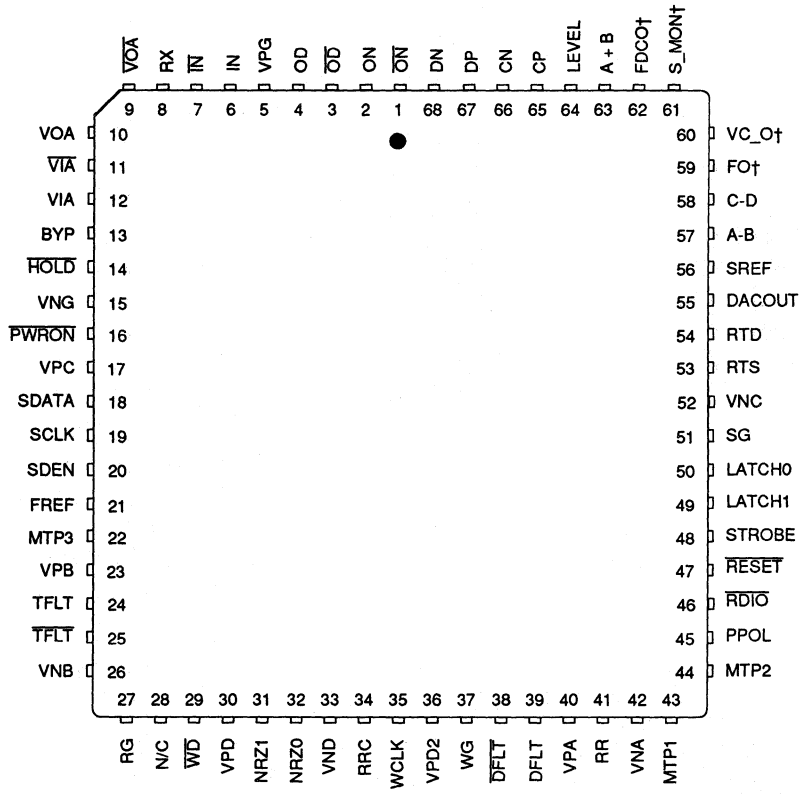


†These pins are for SSi test purposes only.
They should be left open in normal use.

32P4742A
68-Pin CLCC

PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



†These pins are for SSi test purposes only.
They should be left open in normal use.

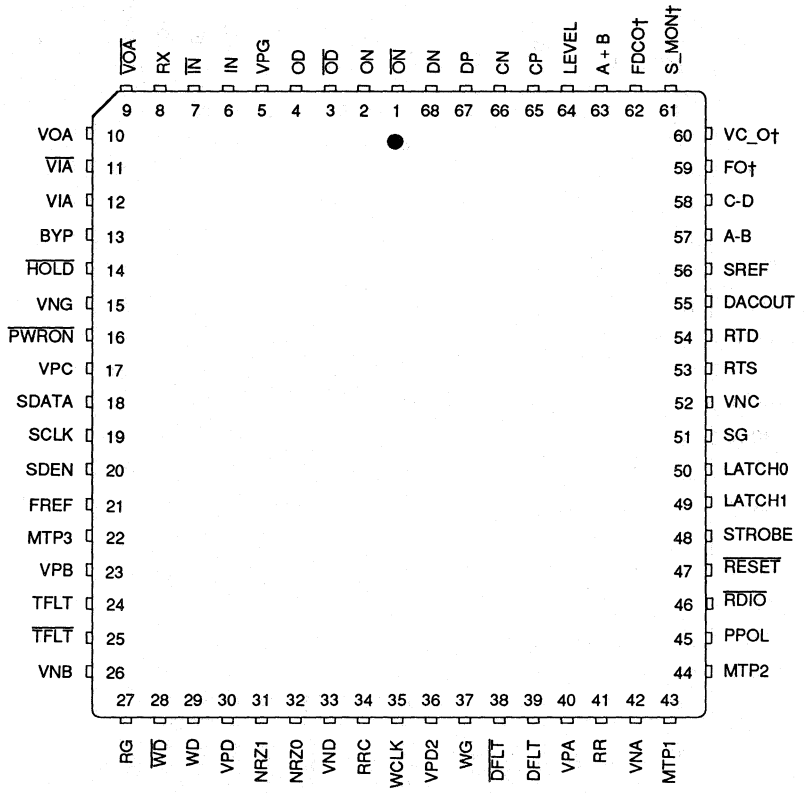
32P4746
68-Pin CLCC

6

SSI 32P4742/4742A/4746/4746A
Read Channel with
1,7 ENDEC, 4-burst Servo

PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



†These pins are for SSi test purposes only.
They should be left open in normal use.

32P4746A
68-Pin CLCC

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914

silicon systems®
A TDK Group Company

SSI 32P4782
80 Mbit/s Read Channel Device

Target Specification

January 1994

DESCRIPTION

The 32P4782 device is a high performance BiCMOS single chip read channel IC that, together with the 32D4680 timebase generator, contains all the functions needed to implement a complete zoned recording read channel for hard disk drive systems. Functional blocks include the pulse detector, programmable filter, servo functions, data synchronizer, window shift, write precomp and 1,7 RLL ENDEC. Data rates from 25 to 80 Mbit/s can be programmed using an internal DAC whose reference current is set by a single external resistor.

The programmable functions of the 32P4782 device are controlled through a bi-directional serial port and banks of internal registers. This allows zoned recording applications to be supported without changing external component values from zone to zone.

The 32P4782 utilizes an advanced BiCMOS process technology along with advanced circuit design techniques which result in a high performance device with low power consumption.

FEATURES

GENERAL

- **Programmable data rate, internal DAC controlled: 25 to 80 Mbit/s**
- **Complete zoned recording application support**
- **Low power operation (550 mW typical @ 5V)**
- **Bi-directional serial port for register access**
- **Register programmable power management (Sleep mode <5 mW)**
- **Power supply range (4.5 to 5.5 volts)**
- **Small footprint 64-lead TQFP package**

AGC

- **LowZ and fast Decay timing independently set by two external resistors**
- **Fast Decay current set by an external resistor**
- **Low Drift AGC Hold circuitry**
- **Separate Read and Servo AGC levels (4-bit DAC)**
- **Temperature compensated, exponential control AGC**
- **Wide bandwidth, high precision full-wave rectifier**
- **Wide bandwidth, high precision multirate charge pump**

PULSE DETECTOR

- **DP, DN pins LowZ switch for rapid transient recovery**
- **Pulse qualification circuitry can be configured via serial port to support one of three modes of operation:**
  - **bit by bit qualification with polarity check**
  - **bit by bit qualification without polarity check**
  - **analog Viterbi detector**
- **Independent control of positive and negative thresholds levels in the data comparators**
- **CMOS RDIO signal output for servo timing support**
- **0.3 ns max. pulse pairing with sine wave input guaranteed by design**

SERVO CAPTURE

- **4-burst servo capture with A, B, C and D outputs.**
- **Separate full wave rectifier connected to filter differentiated output.**
- **Separate registers for filter cutoff, AGC level and qualification threshold during Servo mode**

(continued)

6

FEATURES (continued)

PROGRAMMABLE FILTER

- Cutoff frequency programmable via serial port:
  - 9 to 27 MHz (3 to 9 MHz at degraded specs for filtering in Servo mode)
- Advanced architecture minimizes filter settling characteristics when switching between Servo mode and Data mode
- Programmable boost/equalization range of 0 to 13 dB
- Programmable Group Delay Equalization with asymmetric zeroes control
- Matched normal and differentiated outputs
- ±10% Fc accuracy over operating temperature and supply ranges
- ±2% maximum group delay variation (≤500 ps @ fc = 27 MHz)
- Less than 1% total harmonic distortion
- No external filter components required

DATA SEPARATOR

- High performance dual-bit NRZ interface
- Integrated 1,7 RLL Encoder Decoder
- Fast acquisition phase lock loop with zero phase restart technique
- Fully integrated data separator
  - no external delay lines or active components are required
  - no external active PLL components are required
- Programmable decode window symmetry control via serial port
  - window shift control ±35% (3-bit)
  - delayed read data and VCO clock monitor points
- Programmable write precompensation (3-bit)
  - independent control of three precompensation levels

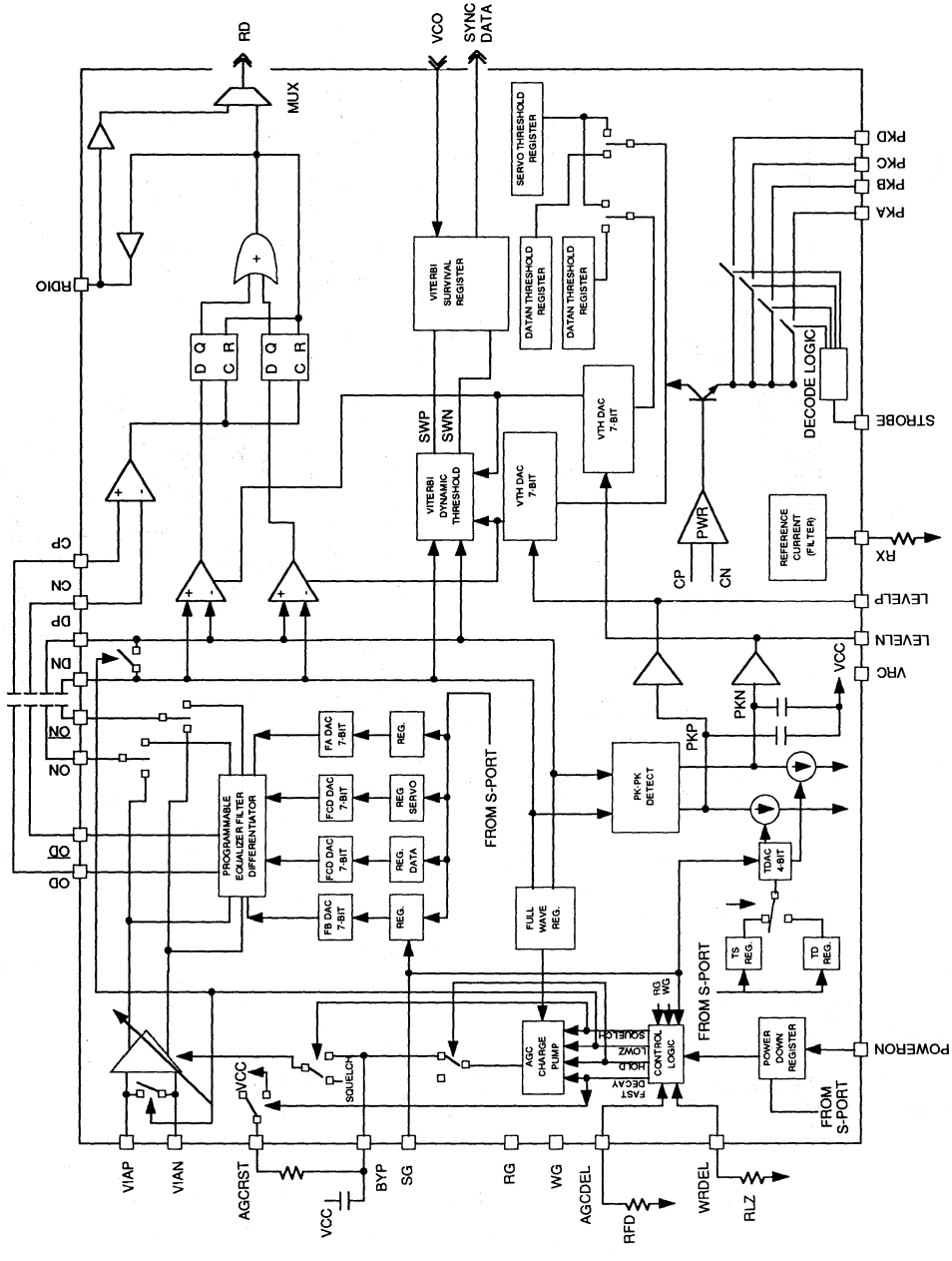


FIGURE 1: Block Diagram (Front-end)

6

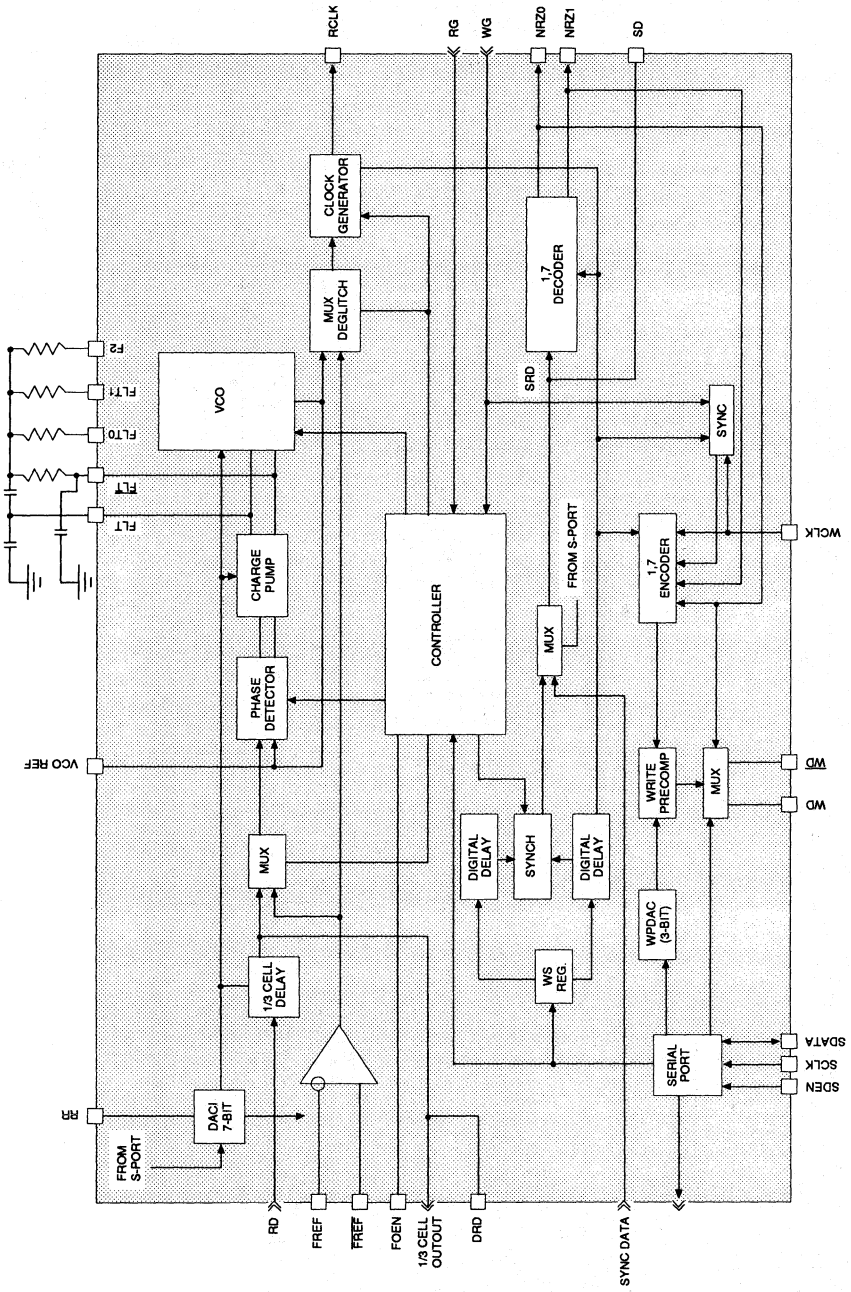
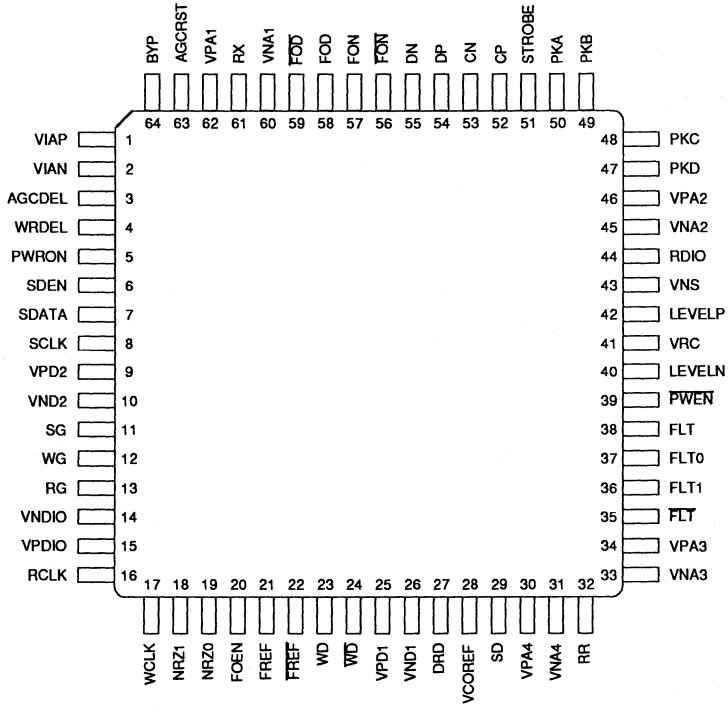


FIGURE 2: Block Diagram (Back-end)

The target specification is intended as an initial disclosure of specification goals for the product. The specifications are based on design goals, subject to change and are not guaranteed. Silicon Systems assumes no obligation regarding future manufacture unless agreed to in writing.

PACKAGE PIN DESIGNATIONS

(Top View)



64-Lead TQFP

CAUTION: Use handling procedures necessary for a static sensitive component.

6

Target Specification: The target specification is intended as an initial disclosure of specification goals for the product. The specifications are based on design goals, subject to change and are not guaranteed. Silicon Systems assumes no obligation regarding future manufacture unless agreed to in writing.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914

Notes:

Abridged Version

SSI 32P4901

PRML Read Channel with PR4, 8/9 ENDEC, FWR Servo

Advance Information

January 1994

GENERAL DESCRIPTION

The SSI 32P4901 is a high performance BiCMOS read channel IC that provides all of the functions needed to implement an entire Partial Response Class 4 (PR4) read channel for zoned recording hard disk drive systems with data rates from 24 to 72 Mbit/s.

Functional blocks include AGC, programmable filter, adaptive transversal filter, Viterbi qualifier, 8/9 GCR ENDEC, data synchronizer, time base generator, and FWR servo. Programmable functions such as data rate, filter cutoff, filter boost, etc. are controlled by writing to the serial port registers so no external component changes are required to change zones.

The SSI 32P4901 utilizes an advanced BiCMOS process technology along with advanced circuit design techniques which result in high performance devices with low power consumption.

The part requires a single +5V power supply and is available in a 100-Lead TQFP package.

FEATURES

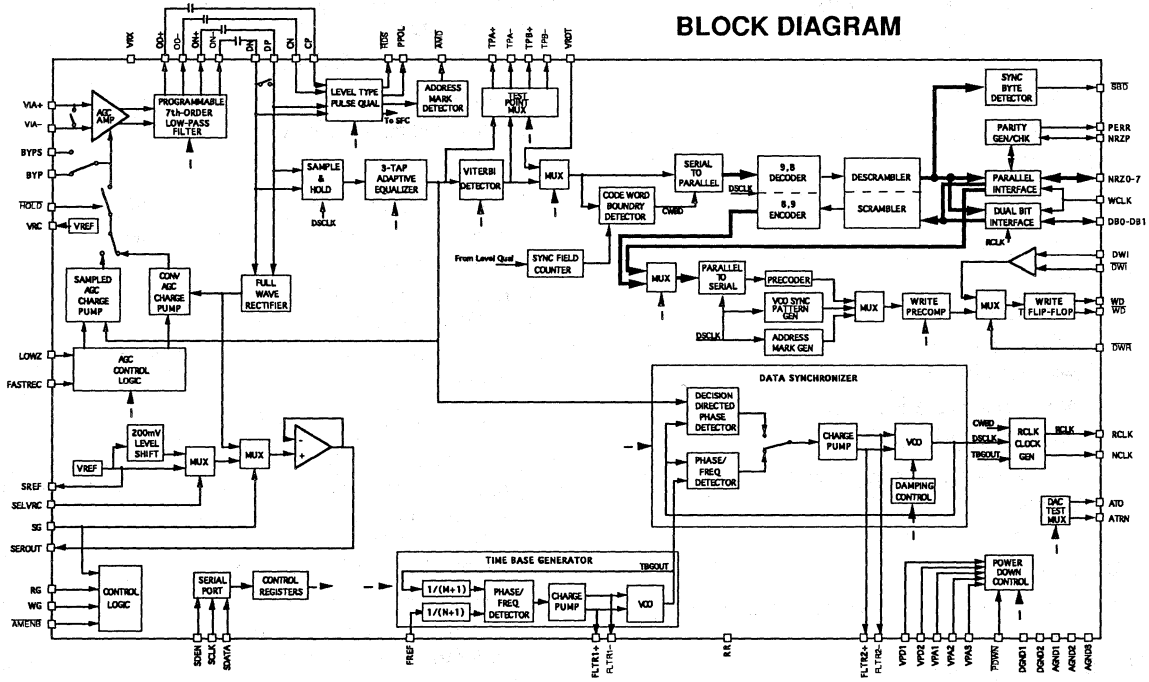
GENERAL:

- **Register programmable data rates from 24 to 72 Mbit/s**
- **Sampled data read channel with Viterbi qualification**
- **Programmable filter for PR4 equalization**
- **Three tap transversal filter for adaptive PR4 equalization**
- **8/9 GCR ENDEC**
- **Data Scrambler/Descrambler**
- **Programmable write precompensation**
- **Low operating power (0.75W typical at 5V)**
- **Register programmable power management (<5 mW Power Down mode)**

(continued)

6

BLOCK DIAGRAM



SSI 32P4901
PRML Read Channel with PR4, 8/9 ENDEC, FWR Servo

FEATURES (continued)

- Dual-bit and byte wide bi-directional NRZ data interfaces
- Serial interface port for access to internal program storage registers
- Single power supply (5V ± 10%)
- Small footprint 100-pin TQFP package

AUTOMATIC GAIN CONTROL:

- Dual mode AGC, analog during acquisition, sampled during read data
- Separate AGC level storage pins for data and servo
- Dual rate attack and decay charge pump for rapid AGC recovery
- Programmable, symmetric, charge pump currents during read data
- Charge pump currents track programmable data rate
- Low drift AGC hold circuitry
- Low Z input switch
- AGC hold, fast recovery, and AGC input impedance control signals
- Wide bandwidth, precision full-wave rectifier

FILTER/EQUALIZER:

- Programmable, 7-pole, continuous time filter provides:
  - Channel filter and pulse slimming equalization for equalization to PR4
  - Programmable cutoff frequency from 8 to 24 MHz
  - Programmable boost /equalization of 0 to 13 dB
  - ±0.5 ns group delay variation from 0.3 Fc to Fc, with Fc = 24 MHz
  - Minimizes size and power
  - Low Z input switch
- Three tap self adapting transversal filter for fine equalization to PR4
- No external components required

PULSE QUALIFICATION:

- Sampled Viterbi qualification of signal equalized to PR4
- Dual level pulse qualifier for servo reads

TIME BASE GENERATOR:

- Better than 1% frequency resolution
- Up to 81 MHz frequency output
- Independent M and N divide-by registers
- No active external components required

DATA SEPARATOR:

- Fully integrated data separator includes data synchronizer and 8/9 GCR ENDEC
- Register programmable to 72 Mbit/s operation
- Fast Acquisition, sampled data phase lock loop
- Decision directed clock recovery from data samples
- Adaptive (+) and (-) clock recovery thresholds for use with asymmetrical amplitude signals (e.g. from MR heads)
- Programmable damping ratio for data synchronizer PLL is constant for all data rates
- Data scrambler/descrambler to reduce fixed pattern effects
- Dual-bit and byte wide NRZ data interfaces
- Time base tracking, programmable write precompensation
- Differential PECL write data output
- Integrated sync byte detection
- Hard and soft sector operation

SERVO:

- Wide bandwidth, precision full-wave rectifier
- Buffered FWR analog servo output with selectable reference voltage
- Separate, automatically selected, registers for servo Fc, boost, and threshold
- Compatible with SSI 32H6521 Embedded Servo Controller

FUNCTIONAL DESCRIPTION

The SSI 32P4901 implements a complete high performance PR4 read channel, including an AGC, programmable filter/equalizer, adaptive transversal filter, Viterbi pulse qualifier, time base generator, data separator with 8, 9 ENDEC and scrambler/descrambler, and FWR servo, that supports data rates up to 72 Mbit/s.

A serial port is provided to write control data to the 16 internal program storage registers.

AGC CIRCUIT DESCRIPTION

The automatic gain control (AGC) circuit is used to maintain a constant signal amplitude at the input of the pulse detector while the input to the amplifier varies. The circuit consists of a loop of circuit blocks that include the AGC amplifier and charge pump, the programmable continuous time filter, and the precision wide band full wave rectifier. Depending on whether the read is of servo or data type, the specific blocks utilized in the loop are slightly different. Both loop paths are fully differential to minimize susceptibility to noise.

During servo reads the loop consists of the AGC amplifier with a continuous dual rate charge pump, the programmable continuous time filter, and the precision wide band full wave rectifier. The gain of the AGC amplifier is controlled by the voltage stored on the BYPS hold capacitor (C_{BYPS}). The dual rate charge pump drives C_{BYPS} with currents that drive the differential voltage at DP/DN to 1.27 Vppd. Attack currents lower the V_{BYPS} which reduces the amplifier gain. The dual rate attack charge pump is included for fast transient recovery. At maximum data rate, the normal AGC attack current is 180 µA. When the signal exceeds 125% of the nominal signal level, the attack current is increased by a factor of 7. The nominal decay current at maximum data rate is 10 µA, and increases by 8 times when the FASTREC input is high. In this mode, transients that produce low gain will recover more rapidly with the Fast Decay current, while transients that produce high gain will put the circuit in the fast attack Recovery mode.

For data reads, the loop described above is used during address mark detection and until the data synchronizer is locked to the incoming VCO preamble, except that the BYP hold capacitor (C_{BYP}) is now used. After this point, the loop is switched to include the AGC amplifier with a sampled dual rate charge pump, the programmable continuous time filter, full wave rectifier, and the sampling 3-tap adaptive equalizer to more accurately control the signal amplitude into the Viterbi qualifier. In this sampled AGC mode, a symmetrical attack and decay charge pump is used. The "1" sample amplitudes are sampled and held and compared to a threshold to generate the error current. The maximum charge pump current value can be programmed from the *Sample Loop Control Register* to 0, 20, 40, or 60 µA.

To optimize recovery for constant density recording, both of the AGC charge pumps' currents track the data rate value loaded in the *Data Rate Register.*

For maximum application flexibility, all AGC mode control inputs are designed to be externally controlled. When the LOWZ input is high, Low-Z mode is activated. In the Low-Z mode, the AGC amplifier input impedance is reduced to allow quick recovery of the AGC amplifier input AC coupling capacitors. This mode should be activated during and for a short time after a write operation.

When the $\overline{\text{HOLD}}$ input is low, the dual rate attack charge pumps are disabled. This de-activates the AGC loop. The AGC amplifier gain will be held constant at a level set by the voltage at the BYP or BYPS pins.

In most applications, the BYP and BYPS pin voltages are stored on external capacitors. In applications where AGC action is not desired, the BYP and BYPS voltages can be set by resistor divider networks connected from VPA to VRC. If programmable gain is desired, the resistor network could be driven by a current DAC.

PULSE QUALIFICATION CIRCUIT DESCRIPTIONS

This device utilizes two different types of pulse qualification, one primarily for servo reads and the other for data reads.

Dual Level Qualifier

During servo reads (SG high) a dual level type of pulse qualifier is used. The level qualification thresholds are set by a 7-bit DAC which is controlled by the *Servo Level Threshold Register.* The register value is relative to the peak voltage at the output of the continuous time filter, and the DAC is referenced to a fixed internal reference voltage. The positive and negative thresholds are equal in magnitude. The state of the adaptive threshold level enable (ALE) bit in the *WP/LT Register* does not affect this DAC's reference. The $\overline{\text{RDS}}$ and the PPOL outputs of the level qualifier indicate a qualified servo pulse and the polarity of the pulse, respectively.

In Data Read mode (RG high), the same dual level qualifier as was used for servo reads, is used for Address Mark Detection and for ensuring pulse polarity changes during VCO sync field counting. It's qualification thresholds are set by a 7-bit DAC which is controlled by or the *Data Level Threshold Register.* The register value is relative to the peak voltage at output of the continuous time filter and the DAC is referenced to an fixed internal reference voltage. The positive and negative thresholds are equal in magnitude. The state of the adaptive threshold level enable (ALE) bit in the *WP/LT Register* does not affect the DAC's reference until the sync field count has been achieved. The $\overline{\text{RDS}}$

Dual Level Qualifier (continued)

and the PPOL outputs of the level qualifier are not active in Data Read mode.

Viterbi Qualifier

The second type of pulse qualification, the viterbi qualifier, is only used during Data Read mode after the sync field count has been achieved. The viterbi qualifier has two significant blocks, one that feeds the other. The first block is the sampled pulse detector and the second is the survival sequence register.

The sampled pulse detector performs the pulse acquisition/detection in the sampled domain. It aquires pulses by comparing the code clock sampled level of the analog waveform to the positive and negative thresholds established by the programmable viterbi threshold window. The viterbi threshold window is defined to be the difference between the positive and negative threshold levels. The threshold window, Vth, is set by a 7-bit DAC which is controlled by the *Viterbi Detector Control Register*. While the window size is fixed by the programmed Vth value, the actual positive and negative thresholds track the most positive and the most negative samples of the equalized input signal. For example, the Viterbi positive signal threshold, Vpt = Vpeak (+) max if the previous detected level was (+). If the previous detect level was (-), Vpt = Vpeak(-)max + Vth, where Vpeak (-) max is the maximum amplitude of the previously detected negative signal. Normally Vth is set to equal Vpeak (approx. 500 mV).

After the pulses have been detected they must be further qualified by the survival sequence registers and associated logic. This logic guarantees that for sequential pulses of the same polarity within the maximum run length, only the latest is qualified. By definition, this is the pulse of greatest amplitude.

The viterbi qualifier is implemented as two parallel qualifiers that operate on interleaved samples. Each qualifier has a survival sequence register length of 5.

PROGRAMMABLE FILTER CIRCUIT DESCRIPTION

The on-chip, continuous time, low pass filter has register programmable cutoff and boost settings, and provides both normal and differentiated outputs. It is a 7th order filter that provides a 0.05° phase equiripple response. The group delay is relatively constant up to twice the cutoff frequency. For pulse slimming two zero programmable boost equalization is provided with no degradation to the group delay performance. The differentiated output is created by a single-pole, single-zero differentiator. Both the boost and the filter cutoff frequency are programmed through internal 7-bit DACs,

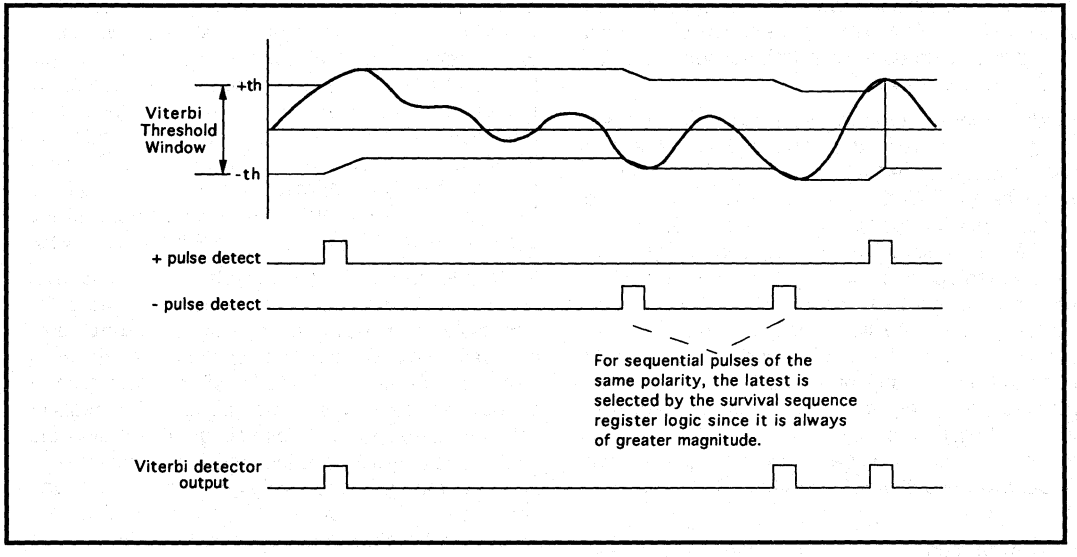


FIGURE 1: Viterbi Detection

accessed via the serial port logic. The nominal boost range at the cutoff frequency is 0 to 13 dB and is controlled by the *Data Boost Register* or the *Servo Boost Register* in the Servo mode. The cutoff frequency, Fc is variable from 3 to 24 MHz and controlled by the *Data Cutoff Register* or *Servo Cutoff Register* in the Servo mode. The cutoff and boost values for Servo reads are automatically switched when Servo mode is entered.

The current reference for the filter DACs is set using a single 12.1K resistor, from the VRX pin to ground. The voltage at VRX is proportional-to-absolute-temperature (PTAT).

ADAPTIVE EQUALIZER CIRCUIT DESCRIPTION

Up to 7 dB of cosine equalization for fine shaping of the incoming read signal to the PR4 waveshape is provided by a 3 tap, sampled analog, transversal filter with an adaptive multiplier coefficient. The same multiplier coefficient (k_m) is used for both of the outside taps. The value of k_m is adjusted to force "zero" samples to zero volts. A special equalizer training pattern, located after the VCO sync field in the sector format, is used to provide an optimum signal for the equalizer to adapt to. The adaptive property of the equalizer is enabled or disabled by the AEE bit in the *Sample Loop Register*. If the adaptive property is enabled, whether adaptation occurs only during the training pattern or both during the training pattern and the user data is controlled by the AED bit in the *Sample Loop Register*.

TIME BASE GENERATOR CIRCUIT DESCRIPTION

The time base generator (TBG) is a PLL based circuit, that provides a programmable reference frequency to the data separator for constant density recording applications. This time base generator output frequency can be programmed with a better than 1% accuracy via the M, N and DR Registers. The TBG output frequency, Fout, should be programmed as close as possible to ((9/8) • NRZ Data Rate). The time base also supplies the timing reference for write precompensation so that the precompensation tracks the reference time base period.

The time base generator requires an external passive loop filter to control its PLL locking characteristics. This filter is fully-differential and balanced in order to reduce the effects of Common mode noise.

In Read, Write and Idle modes, the programmable time base generator is used to provide a stable reference frequency for the data separator. In the Write and Idle modes, the Time Base Generator output, when selected by the *Control Test Mode Register*, can be monitored at the TPA+ and TPA– test pins. In the Read mode, the TBG output should not be selected for output on the test pins so that the possibility of jitter in the data separator PLL is minimized.

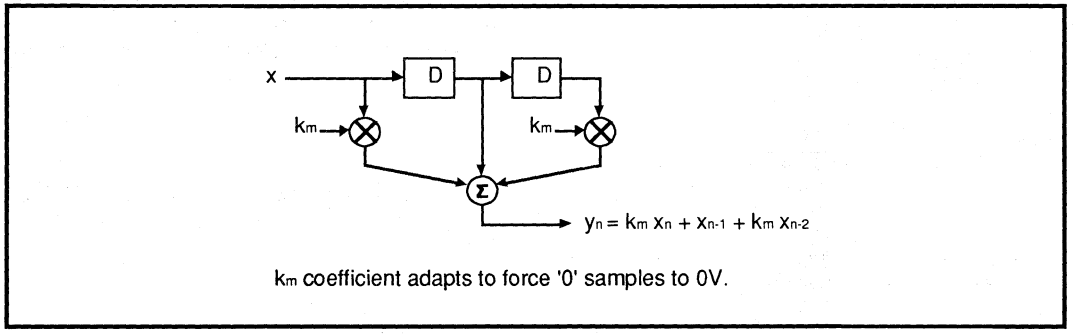


FIGURE 2: 3-Tap Adaptive Equalizer

TIME BASE GENERATOR CIRCUIT DESCRIPTION

(continued)

The reference frequency is programmed using the M and N registers of the time base generator via the serial port, and is related to the external reference clock input, FREF, as follows:

$$FTBG = FREF\,[(M+1) \div (N+1)]$$

The M and N values should be chosen with the consideration of phase detector update rate and the external passive loop filter design. The *Data Rate Register* must be set to the correct VCO center frequency. The time base generator PLL responds to any changes to the M and N registers, only after the DR register is updated.

The DR register value, directly affects the following:

- center frequency of the time base generator VCO,
- center frequency of the data separator VCO,
- phase detector gain of the time base generator phase detector,
- phase detector gain of the data separator phase detector,
- write precompensation

The reference current for the DR DAC is set by an external resistor, RR, connected between the GND and RR pins.

RR = 12.1 kΩ

DATA SEPARATOR CIRCUIT DESCRIPTION

The Data Separator circuit provides complete encoding, decoding, and synchronization for 8/9 (0,4,4) GCR data. In Data Read mode, the circuit performs address mark detect, clock recovery, code word synchronization, decoding, sync byte detection, descrambling, and NRZ interface conversion. In the Write mode, the circuit generates address marks, generates the VCO sync field, scrambles and converts the NRZ data into 8/9 (0,4,4) GCR format, precodes the data, and performs write precompensation.

The circuit consists of five major functional blocks; the data synchronizer, 8/9 ENDEC, NRZ scrambler/descrambler, NRZ interface, and write precompensation.

Data Synchronizer

The data synchronizer uses a fully integrated, fast acquisition, PLL to perform two main functions.

The first of these functions is used in Data Read mode to recover the code rate clock from the incoming read data. The second is used in Write mode to generate a code rate clock that is used to encode and precode NRZ data to form the write data (WD, $\overline{WD}$) outputs. To achieve these two functions, the data synchronizer PLL uses two separate phase detectors to drive the loop. A decision-directed phase detector is used in the Read mode and phase-frequency detector is used in the Idle, Servo, and Write modes.

In the Read mode the decision-directed timing recovery updates the PLL by comparing amplitudes of adjacent "one" samples or comparing the "zero" sample magnitude to ground for the entire sample period. The determination of whether a sample is a "one" or a "zero" is performed by a dedicated, Dual mode, threshold

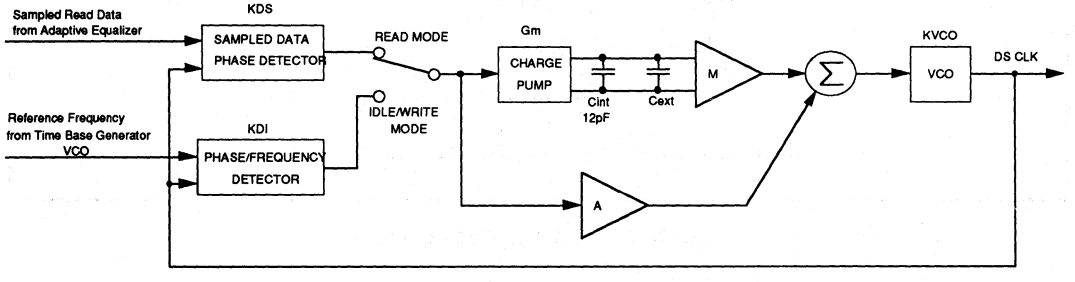


FIGURE 3: Data Synchronizer Phase Locked Loop

comparator. This comparator's threshold levels are determined by the value, Lth, programmed in the *Data Threshold Register.* The fixed level threshold before the sync field count (SFC) has been achieved will be 1.27 times the threshold level after SFC since this is the ratio of the peak signal to the sampled *WP/LT Register.*

The adaptive reference allows the specification of the threshold value to be a percentage of an averaged peak value. When Adaptive mode is selected, the fixed thresholds are used until the sync field count (SFC) has been reached, then the adaptive levels are internally enabled. The time constant of the single pole filter that controls the rate of adaptation, is programmable by bits TC3-1 in the *WP/LT Register.*

In the Write and Idle modes the non-harmonic phase-frequency detector is continuously enabled, thus maintaining both phase and frequency lock to the time base generator's VCO output signal, F_{TBG}. The polarity and width of the detector's output current pulses correspond to the direction and magnitude of the phase error.

The two phase detectors' outputs are muxed into a single differential charge pump which drives the loop filter directly. The loop filter requires an external capacitor. The loop damping ratio is programmed by bits 6-0 in the *Damping Ratio Control Register.* The programmed damping ratio is independent of data rate.

ENDEC

The ENDEC implements an 8/9 (0,4,4) Group Coded Recording (GCR) algorithm. The code has a minimum of no zeros between ones and a maximum of four zeros between ones for the interleaved samples. During write operations the encoder portion of the ENDEC converts 8 bit parallel, scrambled or nonscrambled, data to 9 bit parallel code words that are then converted to serial format. In data read operation, after the code word boundry has been detected, the decoder portion of the ENDEC converts 9 bit parallel, viterbi qualified, data to 8 bit NRZ format.

Scrambler/Descrambler

The scrambler/descrambler circuit is provided to reduce fixed pattern effects on the channel's performance. It is enabled or disabled by bit 2 of the *Control Operating Register.* In Write mode, if enabled, the circuit scrambles the 8 bit internal NRZ data before passing it to the encoder. Only user data, i.e., the NRZ data following the sync byte, is scrambled. In Data Read mode, only the decoded NRZ data after the sync byte is descrambled. The scrambler polynomial is:

$H(X) = 1 \otimes X7 \otimes X10.$

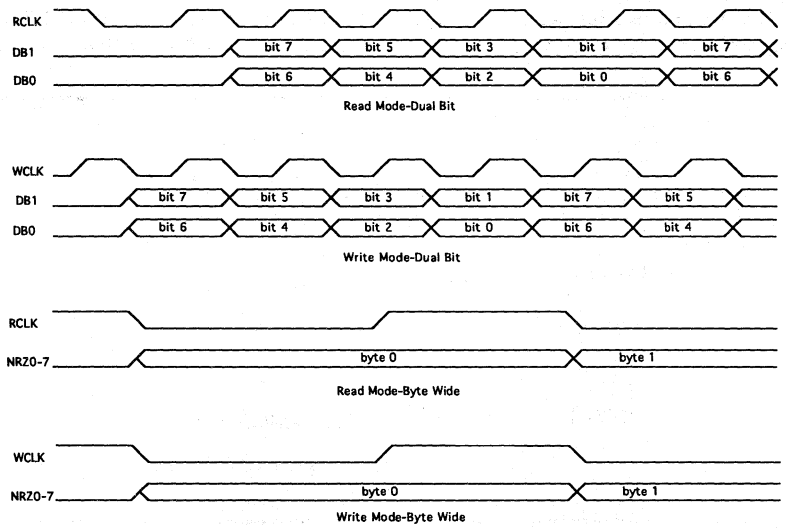


FIGURE 4: RCLK, WCLK vs. NRZ Data

NRZ Interface

The NRZ interface circuit provides the ability to interface with either a dual bit or Byte wide controller. The NRZ interface type is specified by the programming of bit 4 of the *Control Operating Register*. If byte Wide mode is selected, the circuit does not reformat the data before passing it to and from the internal 8 bit bus. If Dual Bit mode is selected, the NRZ interface circuit converts the external dual bit bus to the internal 8 bit bus. Only the selected NRZ interface is enabled and the other can be left floating. Both the byte wide and dual bit interfaces define the most significant bit of the interface as the most significant bit of the data and the dual bit interface defines the first pair clocked in or out as the most significant pair.

For both byte wide and dual bit operation, the NRZ write data is latched by the 32P4901 on the rising edge of the WCLK input. The WCLK frequency must be appropriate for the data rate chosen or else overflow/underflow will occur. It is recommended that WCLK be connected to RCLK to prevent this from occurring. In Byte-Wide mode, as each NRZ byte is input to the 32P4901, its parity is checked against the controller supplied parity bit NRZP. If an error is detected, the PERR output pin goes high and remains high until WG goes low.

In Data Read mode, the NRZ data will be presented to the controller near the falling edge of RCLK so that it can be latched by the controller on the rising edge of RCLK. When RG goes high, the selected NRZ interface will output low data until the sync byte has been detected. The first non-zero data presented will be the sync byte (96H). The NRZ interface is at a high impedance state when not in Data Read mode. In Byte-Wide mode, an even parity bit, NRZP, is generated for each output byte.

Write Precompensation

The write precompensation circuitry is provided to compensate for media bit shift caused by magnetic nonlinearities. The circuit recognizes specific write data patterns and can add delays in the time position of write data bits to counteract the magnetic nonlinearity effect. The magnitude of the time shift, WPC, is programmable via the *Write Precomp Register* and is made proportional to the time base generator's VCO period (i.e., data rate). The circuit performs write precompensation only on the second of two consecutive "ones" and only shifts in the late direction. If more than two consecutive "ones" are written, all but the first are precompensated in the late direction.

SERVO CIRCUIT DESCRIPTION

Embedded servo capture is provided with a buffered full-wave rectified (FWR) output. The differential signal across the DP/DN inputs is applied to a full-wave rectifier. The output signal of the rectifier is the rectified servo burst signal, level-shifted above SREF (which is a bandgap reference from VPA1). The output at the SEROUT pin is selectable between the FWR output and two references, SREF and SREF + 200 mV. When the SG is high (active) the FWR output is selected for

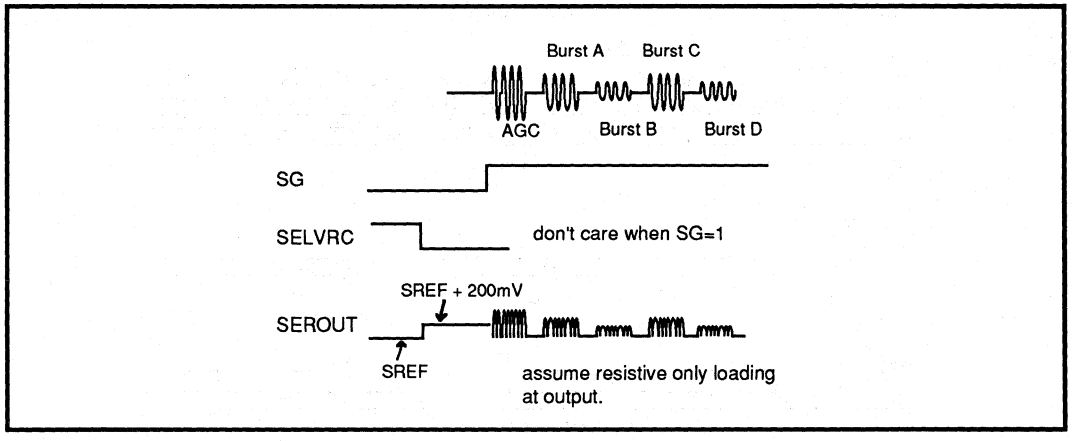


FIGURE 5: Servo Function Diagram

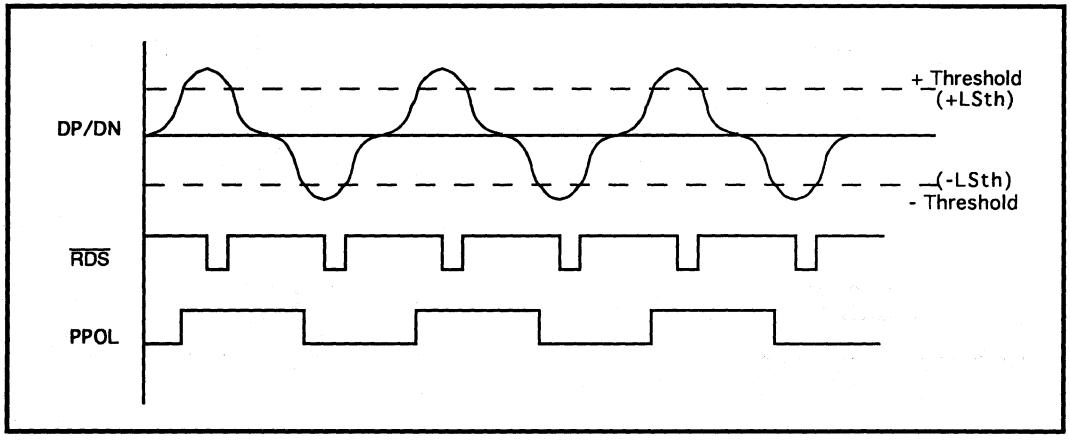


FIGURE 6: $\overline{RDS}$ and PPOL vs. DP/DN Relationship

the SEROUT pin. When SG is low (i.e., during the data field) then the SEROUT pin is selected between SREF and SREF + 200 mV, depending on the input at SELVRC.

The dual level pulse qualifier outputs $\overline{RDS}$ and PPOL are enabled when the servo gate input (SG) goes high and provide the indication of a qualified servo pulse and the polarity of the pulse, respectively.

SG	SELVRC	SEROUT
1	1	FWR Output
1	0	FWR Output
0	1	SREF
0	0	SREF + 200 mV

SERIAL PORT CIRCUIT DESCRIPTION

The serial port interface is used to program the 32P4901's sixteen internal registers. The serial port is enabled for data transfer when the Serial Data Enable (SDEN) pin is high (0).

When SDEN is high, the data presented to the Serial Data (SDATA) pin will be latched into the 32P4901 on each rising edge of the Serial Clock (SCLK). Rising edges of SCLK should only occur when the desired bit of address or data is being presented on the serial data line. Serial data transmissions must occur in 16-bit packets. If more than 16 rising edges of SCLK are received during the time that SDEN is high, the additional SCLK and SDATA information will be ignored. During a serial data transmission, if SDEN is switched low before 16 SCLK pulses are received, that serial transmission will be aborted. For all valid transmissions, the data is latched into the internal register on the falling edge of SDEN.

Each 16 bit transmission consists of 8 address bits first, and then the 8 data bits. The address bits select the internal register to be written to. The address and data fields are input LSB first, MSB last, where LSB is defined as Bit 0. The four MSB address bits are reserved for other types of devices using the SSI serial port protocol and must be set to zero when addressing the 32P4901. Figure 7 shows the serial interface timing diagram.

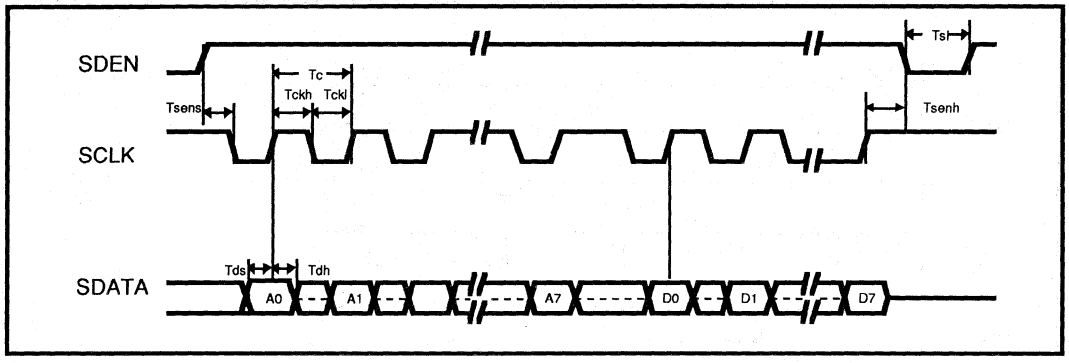


FIGURE 7: Serial Interface Timing

DESCRIPTION OF OPERATING MODES

The fundamental Operating modes of the 32P4901 are controlled by the SERVO GATE (SG), READ GATE (RG), and WRITE GATE (WG) input pins. The exclusive assertion of any these inputs causes the device to enter that mode. If none of these inputs is asserted, the device is in the IDLE mode. If more than one of the inputs is asserted, the mode is determined by the following hierarchy: SG overrides RG which overrides WG. The mode that is overriding takes effect immediately.

RG and SG are asynchronous inputs and may be initiated or terminated at any position on the disk. WG is also an asynchronous input, but should not be terminated prior to the last output write data (WD/$\overline{WD}$) pulse.

IDLE MODE OPERATION

If SG, RG, and WG are not active, the 32P4901 is in Idle mode. When in Idle mode, the Time Base Generator and the Data Separator PLL are running and the Data Separator PLL is phase-frequency locked to the TBG VCO output. The AGC, continuous time filter, and pulse qualifiers are active but the outputs of the pulse qualifiers are disabled. The continuous time filter is using its programmed values for cutoff frequency and boost determined by the Data mode registers.

SERVO MODE OPERATION

If SG is high, the device is in the Servo mode. This mode is the same as Idle except that the filter cutoff and boost settings are switched from those programmed for Data Read mode to those programmed for Servo mode, and the $\overline{RDS}$, PPOL, and SEROUT outputs are enabled. The assertion of SG causes Read mode, Write mode, and the power down register settings for the front end to be overriden.

WRITE MODE OPERATION

The 32P4901 supports three different Write modes; Normal Write mode, direct Write mode #1 and direct Write mode #2. The Direct Write modes require that either the Direct write bit, bit 0 of the *Control Operating Register*, or the $\overline{DWR}$ pin be active. All three Write modes require that the data separator be powered on.

Normal Write Mode

The 32P4901 is in the normal Write mode if WG is high, $\overline{DWR}$ is high, and the direct write bit in the *Control Operating Register* is low. A minimum of one NRZ time period must elapse after RG goes low before WG can be set high. The data separator PLL is phase-frequency locked to the TBG VCO output in this mode.

In normal Write mode, the circuit first auto generates an address mark (soft sector only), then auto generates the VCO sync pattern, and finally scrambles the incoming NRZ data from the controller, encodes it into 8/9 GCR formatted data, precodes it, precompensates it, feeds it to a write data toggle flip-flop, and outputs it to the preamp for storage on the disk. The write data flip-flop is reset when WG goes low to ease testing. The circuit can operate in either soft or hard Sector modes.

Normal Write Mode - Soft Sector

In soft sector operation, when the write gate (WG) goes high, the NRZ inputs must be low and must be held low

for the duration of the address mark and VCO sync field generation. The address mark enable ($\overline{AMENB}$) should be made active (low) a minimum of 1 NRZ time period after rising WG to initiate the generation of the address mark sequence at the WD/$\overline{WD}$ outputs. The address mark sequence consists of four 8 "0" gaps (=9T). {(1, 1, 1, 1, 1, 1, 1, 1, -1, -1, -1, -1, -1, -1, -1, -1, -1, 1, 1, 1, 1, 1, 1, 1, 1, 1, 1, -1, -1, -1, -1, -1, -1, -1, -1, -1, -1) in the write current domain} $\overline{AMENB}$ should be held low for 5 NRZ time periods minimum and then returned high. Next, the circuit generates the VCO sync field (=2T) at the WD/$\overline{WD}$ outputs. {(1,1,-1,-1,1,1,-1,-1...) in the write current domain} While the preamble is being written, WCLK must continue to clock in all (0) NRZ data. After the required sync field has been written (approximately 8 byte times, min.), the NRZ data must be changed to 93H for a minimum of 5 byte times to write the minimum 5 byte equalizer training pattern. The device will continue to autogenerate the sync field pattern until the first 93H is latched at NRZ interface, and detected. Next, the NRZ data must be changed to 96H for 1 byte time to write the sync byte. Now the user NRZ data may be written. Finally, after the last byte of user data has been clocked in, the WG must remain high for a minimum of 34 NRZ bit times in Byte-Wide mode to ensure the that the device is flushed of data (The delay is 37 NRZ bit times in Dual Bit mode). WG can then go low. WD/$\overline{WD}$ stops toggling a maximum of 2 NRZ (RCLK) time periods after WG goes low.

Normal Write - Hard Sector

In hard sector operation, the circuit performs exactly the same as in soft sector except that the $\overline{AMENB}$ input pin will be held high so the address mark pattern is not generated.

Direct Write Mode #1

In this Direct Write mode, the NRZ data from the byte-wide interface bypasses the scrambler and the 8/9 encoder, but is precoded and precompensated before going to the write data flip-flop and then to the WD/$\overline{WD}$ output pins. WCLK is required to clock the byte-wide NRZ data into the NRZ interface. Direct Write mode #1 is entered simply by setting the DW bit (bit 0) in the Control Operating Register. This mode is not valid when using the dual-bit NRZ interface.

Direct Write Mode #2

In this Direct Write mode, the data presented at the DWI/$\overline{DWI}$ input pins directly toggles the write data flip-flop which drives the WD/$\overline{WD}$ output pins. No WCLK is required in this mode, and the WD/$\overline{WD}$ output is not

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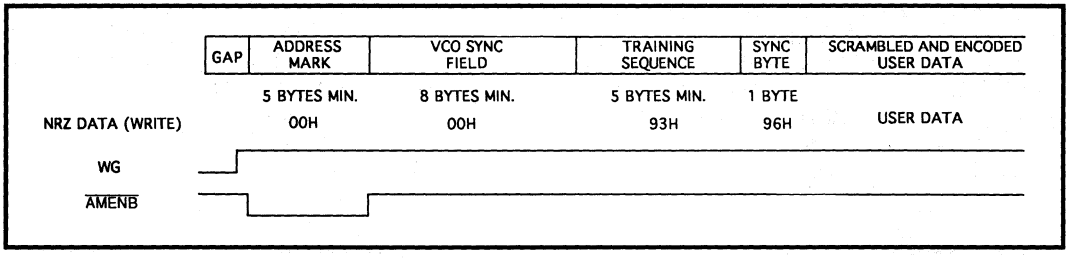

FIGURE 8: Soft Sector Write Sequence

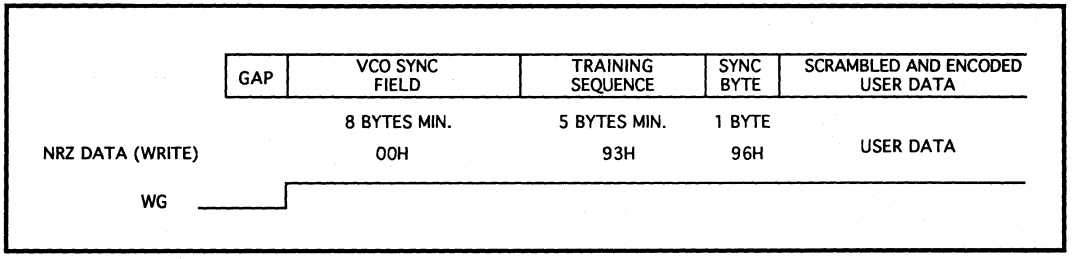

FIGURE 9: Hard Sector Write Sequence

Direct Write Mode #2 (continued)

resynchronized. Direct Write mode #2 is entered simply by driving the $\overline{DWR}$ input low.

Data Read Mode Operation

Data Read mode is initiated by setting the Read Gate (RG) input pin high. This action causes the data synchronizer to begin to acquisition of the clock from the incoming VCO sync pattern. To achieve this, the data synchronizer utilizes a fully integrated fast acquisition PLL to accurately develop the sample clock. This PLL is normally locked to the time base generator output, but when the Read Gate input (RG) goes high, the PLL's reference input is switched to the filtered incoming read signal.

SOFT SECTOR OPERATION

In soft sector read operation the circuit must first detect an address mark before initiating the rest of the read lock sequence.

Address Mark Detect

The address mark consists of four sets of 8 "0" (=9T) patterns{(1,0,0,0,0,0,0,0,0,-1,0,0,0,0,0,0,0,0,1,0,0,0,0, 0,0,0,0,-1,0,0,0,0,0,0,0,0,1) in the read domain}. This pattern was chosen because the interval between polarity changes of the read back pattern has 9 nominal clock periods which is illegal in an 8/9 (0,4,4) code. The maximum zero read data pattern for a legal 8/9 (0,4, 4) code word is 5 nominal clock periods between polarity changes. The read signal polarity changes are detected by the dual level pulse detector. Address mark detection is accomplished by counting the clocks (as "0's") between the polarity changes.

To begin the soft sector read sequence the Address Mark Enable ($\overline{AMENB}$) input pin must be asserted low. The address mark detect ($\overline{AMD}$) circuit then initiates a search of the level qualified read data (RD) for an address mark. First the $\overline{AMD}$ looks for a set of 7 "0's" within the 8 "0" patterns. Having detected a 7 "0" the $\overline{AMD}$ then looks for two more 7 "0" gaps. If the $\overline{AMD}$ does not detect three 7 "0" gaps within 38 code clock periods it will restart the address mark detect sequence and look for 7 "0's." When the $\overline{AMD}$ has acquired a 7 "0" 3-gap sequence, the $\overline{AMD}$ output pin transitions low. The $\overline{AMD}$ will remain low for the duration of $\overline{AMENB}$. When the $\overline{AMENB}$ is released, the $\overline{AMD}$ will be released.

Acquisition of DS VCO Sync

After the Address Mark (AM) has been detected, the Read Gate input can be asserted high, initiating the remainder of the read sequence. When RG is asserted an internal counter begins counting the pulses that are qualified by the dual level pulse qualifier given the polarity changes of the incoming 1,1,-1,-1,1,1 read back pattern defined by the VCO sync field. When the count reaches 4, the internal read gate is asserted and the DS PLL input is switched from the TBG's VCO output to the sampled data input. This is also the point at which the DS PLL's phase detector is switched from the phase-frequency detector to the decision directed phase detector. The counter is also used to determine whether the selected sync field count, SFC, has been achieved. The SFC, is the point at which the data synchronizer PLL is assumed to be locked and settled (VCO lock). At SFC is also when the phase detector gain switch and the AGC mode switch occur. To allow for different preamble lengths, the SFC can be set to

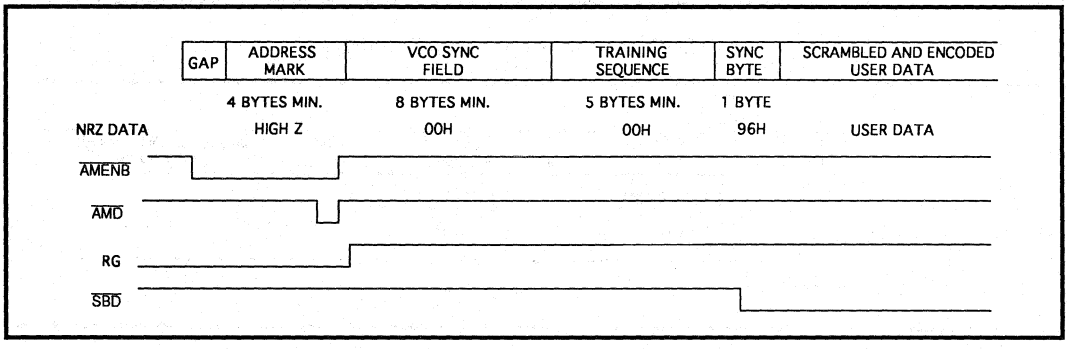

Figure 10: Soft Sector Read Sequence

64, 80, 96 or 128 from the *Sample Loop Control Register*. These values for the SFC may be thought of as the number of code clock periods in the sync field, but they actually represent twice the number of incoming polarity changes required.

VCO Lock, PD Gain, AGC Mode Switch, and Code Word Boundry Detector Enable

At SFC, one of two phase tracking methods will be chosen depending on the Enable Phase Detector Gain Switching (GS) bit in the *Control B Register*. When the GS bit is low, the phase detector gain is reduced by a factor of 5 after the SFC count is reached. When the GS bit is high, no phase detector gain switching takes place.

Also after SFC, the AGC feedback will be switched from the continuous time fullwave rectifier to sampled data feedback.

At SFC, the internal VCO lock signal activates the code word boundry detection circuitry to define the proper decode boundaries. Also, at count SFC, the RCLK generator source switches from the TBG's VCO output to the DS VCO clock signal which is phase locked to the incoming read data samples. The DS VCO is assumed locked to the incoming read samples at this point. A maximum of 1 RCLK time period may occur for the RCLK transition, however, no short duration glitches will occur. After the code word detection circuitry finds the proper code word boundry, the RCLK generator is resynchronized to guarantee that the RCLK is in sync with the data. The RCLK and NCLK outputs will not glitch and may not toggle during the RCLK generator resynchronization for up to 2 byte times maximum.

Also at the code word boundry detect, the internal 9-bit code words are allowed to pass to the ENDEC for decoding. This decoding will occur until read gate is deasserted.

Adaptive Equalizer Training Sequence

As was previously discussed, in a normal write sequence, a minimum of 5 bytes of NRZ 93H and one byte of 96H must be written between the end of the VCO sync field and the beginning of the user data. The 5 bytes of 93H are 8/9 encoded and precoded during Write mode to produce the adaptive equalizer training pattern. During Read mode, this sequence (100110011 read data sequence) is used to adaptively train the three tap transversal filter in a zero forcing manner. The error at the filter output is integrated to derive the tap weight multiplying coefficient, Km. The filter input and output tap will have the same Km. It is anticipated that the continuous time equalizer will be used for coarse equalization and that transversal filter will be used adaptively for fine tuning. This will reduce Km's range and accuracy requirements. Since there are encoded user data patterns that will not produce an equalizer correction error, an equalization hold during Data mode can selected from the *Sample Loop Control Register*. After the training pattern, if the loop is active during data, the equalizer loop gain will be reduced by 4. The loop's integration time constant is made inversely proportional to the selected data rate.

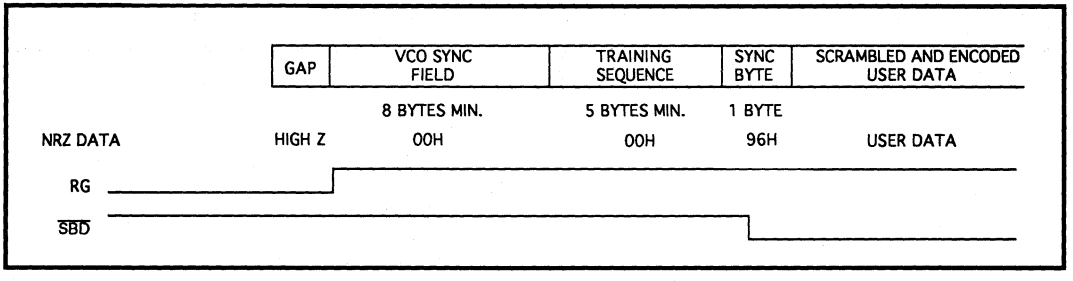

FIGURE 11: Hard Sector Read Sequence

Sync Byte Detect and NRZ Output

As the read data is 8/9 decoded, it is compared to an internally fixed sync byte (96H). When a match is found, the sync byte detect ($\overline{SBD}$) pin goes low and the NRZ output data that until now was held low, is changed to 96H. The next byte presented on the NRZ outputs is the first byte of user data. $\overline{SBD}$ will remain low and NRZ data will continue to be presented at the NRZ interface until the read gate is deasserted at which point $\overline{SBD}$ goes high and the NRZ outputs go to a high impedance state.

HARD SECTOR OPERATION

In hard sector operation, Address Mark search and detection is not required, so by setting $\overline{AMENB}$ high, the Address Mark Detection circuitry is disabled and $\overline{AMD}$ remains inactive. A hard sector read operation begins with the assertion of RG which starts the VCO sync field counting as in soft Sector mode and sequences identically. In all respects, with exception of the lack of an address mark search sequence, hard sector read operation is the same as soft sector read.

POWER DOWN OPERATION

The power Management modes of the 32P4901 are determined by the states of the *Power Down Register* bits and the $\overline{PDWN}$ and SG inputs. The individual sections of the chip can be powered down or up using the *Power Down Register*. A high level in a *Power Down Register* bit disables that section of the circuit. The power down information from the *Power Down Register* takes effect immediately after the SDEN pin goes low.

When the $\overline{PDWN}$ input is low, the chip goes into full Power Down mode regardless of the power down register settings or the state of the SG input.

When $\overline{PDWN}$ is high and SG will force the AGC, filter, and pulse qualifier circuits (front end) to be active by overriding the front end register bit. The back end Power Down register bits, which include the Data Separator and Tme Base Generator are not affected by the SG input.

The serial port is active in all Power Down modes.

The time to restart from a full power down is dependent on the PLL loop filter and the data rate.

The truth table for the various modes of operation is shown below.

TABLE 1: Operation Mode Truth Table

SG, $\overline{PDWN}$	1,1	1,0	0,1	0,0
Front End	ON	OFF	R	OFF
Data Separator	R	OFF	R	OFF
Timebase Generator	R	OFF	R	OFF
Serial Port	ON	ON	ON	ON
R = Controlled by register bit.				

(Register bit =1 turns circuits OFF, Register bit = 0 turns circuits ON)

PIN DESCRIPTION

POWER SUPPLY PINS

NAME	TYPE	DESCRIPTION
VPA	–	AGC/Filter analog circuit supply
VPF	–	Time Base Generator PLL analog circuit supply
VPT	–	Time Base Generator digital supply
VPP	–	Data Separator PLL analog circuit supply
VPD	–	TTL Buffer I/O digital supply
VPC	–	Internal ECL, CMOS logic digital supply
VPS	–	Sampled data processor supply
VNA	–	AGC/Filter analog circuit ground
VNF	–	Time Base Generator PLL analog circuit ground
VNT	–	Time Base Generator digital ground
VNP	–	Data Separator PLL analog circuit ground
VND	–	TTL Buffer I/O digital ground
VNC	–	Internal ECL, CMOS logic digital ground
VNS	–	Sampled data processor ground

ANALOG INPUT PINS

VIA+, VIA–	I	AGC AMPLIFIER INPUTS: Differential AGC amplifier input pins
DP, DN	I	ANALOG INPUTS FOR DATA PATH: Differential analog inputs to data comparators, full-wave rectifier
CP, CN	I	ANALOG INPUTS FOR CLOCK PATH: Differential analog inputs to the clock comparator

ANALOG OUTPUT PINS

NAME	TYPE	DESCRIPTION
TPA+, TPA–	O	TEST PINS: Emitter output test points. Various signals are multiplexed to these test points by the *Test Point Control Register*. The signals include the equalizer control voltage and output, various timing loop control signals and the viterbi survival register outputs. The test points are provided to show how the signal is being processed. Internal "pull down" resistors to ground are provided. To save power when not in Test mode, the Control Test Register bits 3 - 5 must be set to "0".
TPB+, TPB–	O	TEST PINS: Emitter output test points similar to TPA+ and TPA-. The pins are used to look at the other phase of the interleaved signals.
ATO	O	ANALOG TEST OUT: A test point used to indicate the operation of controlled functions which cannot be easily determined by direct testing of the circuit pins. The selected output is determined by the address in the serial control register.

ANALOG OUTPUT PINS (CONTINUED)

NAME	TYPE	DESCRIPTION
ATRN	O	ANALOG TEST OUT RETURN: A test point used as the ATO return.
ON+, ON–	O	FILTER NORMAL OUTPUTS: These are the filter normal low pass output. They should be AC coupled to the data comparator in the pulse qualifier. Open emitter output with internal pulldown. If driving more than coupling cap, external pull down resistor to ground may be required.
OD+, OD–	O	FILTER DIFFERENTIATED OUTPUTS: These are the filter time differentiated low pass output. They should be AC coupled, for low DC offset, to the clock comparator in the pulse qualifier. Open emitter output with internal pulldown. If driving more than coupling cap, external pull down resistor to ground may be required.
SEROUT	O	MULTIPLEXED SERVO OUTPUT: Open Emitter. Requires external pull down to GND.
SREF	O	SERVO REFERENCE OUTPUT: +2.0V DC reference voltage, baseline for servo bursts. Open Emitter. Requires external pull down to GND.

ANALOG CONTROL PINS

BYP	–	The data AGC integrating capacitor, CBYP, is connected between BYP and VPA. This pin is used when in data Read mode (RG = 1).
BYPS	–	The servo AGC integrating capacitor, CBYPS, is connected between BYPS and VPA. This pin is used when in servo Read mode (SG = 1).
FLTR1+, FLTR1–	–	TBG PLL LOOP FILTER: Differential connection points for the time base generator PLL loop filter components.
FLTR2+, FLTR2–	–	DS PLL LOOP FILTER: Differential connection points for the data separator PLL loop filter capacitor.
RR	–	CURRENT REFERENCE RESISTOR INPUT: An external 1% 12.1 kΩ resistor is connected from this pin to ground to establish a precise internal reference current for the data separator and the time base generator DACs.
VRX	–	FILTER REFERENCE RESISTOR INPUT: An external 1% 12.1 kΩ resistor is connected from this pin to ground to establish a precise PTAT (proportional to absolute temperature) reference current for the filter DACs.
VRC	–	AGC REFERENCE VOLTAGE: VRC is derived by a bandgap reference from VPA1.

DIGITAL INPUT PINS

LOWZ	I	LOW-Z MODE INPUT: TTL compatible control pin which, when pulled high, the input impedance is reduced to allow rapid recovery of the input coupling capacitor. When pulled low, keeps the AGC amplifier and filter input impedance high. An open pin is a logic high.
FASTREC	I	FAST RECOVERY: TTL compatible control pin which, when pulled high, puts the AGC charge pump in the fast Decay mode. An open pin is a logic high.

DIGITAL INPUT PINS (continued)

NAME	TYPE	DESCRIPTION
$\overline{\text{AMENB}}$	I	ADDRESS MARK ENABLE: TTL compatible control pin which, when pulled low, enables the address mark detection and generation circuitry. An open pin is a logic high.
$\overline{\text{PDWN}}$	I	POWER DOWN CONTROL CONTROL: TTL compatible power control pin. When set to logic low, the entire chip is in Sleep mode with all circuitry, except serial port, shut down. This pin should be set to logic high in normal Operating mode. Selected circuitry can be shut down by the *Power Down Register.* An open pin is a logic high.
$\overline{\text{HOLD}}$	I	AGC HOLD CONTROL INPUT: TTL compatible control pin which, when pulled low, holds the AGC amplifier gain constant by turning off the AGC charge pump. The AGC loop is active when this pin is either at high or open.
FREF	I	REFERENCE FREQUENCY INPUT: Reference frequency for the time base generator. FREF may be driven either by a direct coupled TTL signal or by an AC coupled ECL signal. When bits 2 or 7 of the *Control Test Register* are set, FREF replaces the VCO as the input to the data separator.
WCLK	I	WRITE CLOCK: TTL compatible input that latches in the data at the selected NRZ interface on the rising edge. Must be synchronous with the write data NRZ input. For short cable delays, WCLK may be connected directly to pin RCLK. For long cable delays, WCLK should be connected to an RCLK return line matched to the NRZ data bus line delay. An open pin is at logic high.
RG	I	READ GATE: TTL compatible input that, when pulled high, selects the PLL reference input and initiates the PLL synchronization sequence. A high level selects the RD input and enables the Read mode/address detect sequences. A low level selects the time base generator output. An open pin is at logic high.
WG	I	WRITE GATE: TTL compatible input that, when pulled high, enables the Write mode. An open pin is at logic high.
SG	I	SERVO GATE: TTL compatible input that, when pulled low, enables the Servo Read mode. An open pin is at logic high.
SELVRC	I	SERVO REFERENCE SELECT: TTL compatible input. When SG is low this input selects between the SREF reference (SELVRC = high) and the SREF + 200 mV level (SELVRC = low) for presentation at the SEROUT output.
VRDT	I	VITERBI READ DATA: A TTL or AC coupled PECL compatible input to the data separator back end, for testing purposes only. This pin is controlled by the VRDT bit in the *Control Test Register.*
$\overline{\text{DWR}}$	I	DIRECT WRITE MODE 2 ENABLE: Enables DWI, $\overline{\text{DWI}}$ inputs to the write data flip-flop when input is low. TTL levels. Open pin ia at logic high.
DWI, $\overline{\text{DWI}}$	I	DIRECT WRITE INPUTS: Inputs connect to the toggle input of the write data flip-flop when $\overline{\text{DWR}}$ is low. PECL input levels. Can be left open.

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DIGITAL INPUT PINS (continued)

NAME	TYPE	DESCRIPTION
SCLK	I	SERIAL DATA CLOCK: Positive edge triggered clock input for the serial data. TTL input levels.
SDATA	I	SERIAL DATA: Input pin for serial data; 8 address bits first followed by 8 data bits. The address and data bits are entered LSB first, MSB last. TTL input levels.
SDEN	I	SERIAL DATA ENABLE: A high level input enables data loading. The data is internally parallel latched when this input goes low. TTL input levels.

DIGITAL BIDIRECTIONAL PINS

NAME	TYPE	DESCRIPTION
NRZ0-7	I/O	BYTE WIDE NRZ DATA PORT: TTL compatible bi-directional input/output. Input to the encoder when WG is high. Output from the decoder when RG is high. Can be left open if not used.
NRZP	I/O	NRZ DATA PARITY BIT: Active when in Byte Wide mode. TTL compatible bi-directional input/output. Generates even read parity when RG is high, and accepts even write parity when WG is high. Can be left open if not used.
DB0-1	I/O	DUAL BIT NRZ DATA PORT: TTL compatible bi-directional input/output. Input to the encoder when WG is high. Output from the decoder when RG is high. Can be left open if not used.

DIGITAL OUTPUT PINS

RCLK	O	READ REFERENCE CLOCK: A multiplexed clock source used by the controller. When RG is low, RCLK is synchronized to the time base generator output, F_{TBG}. When RG goes high, RCLK remains synchronized to F_{TBG} until the SFC is reached. At that time, RCLK is synchronized to the data separator VCO. During a mode change, no glitches are generated and no more than one lost clock pulse will occur. TTL output levels.
NCLK	O	NIBBLE CLOCK: A half-byte clock synchronized to RCLK. It runs at twice the frequency of RCLK. CMOS output levels.
$\overline{AMD}$	O	ADDRESS MARK DETECT: Tristate output pin that is in its high impedance state when WG is high or $\overline{AMENB}$ is high. When $\overline{AMENB}$ is low, this output indicates address mark search status. A latched low level output appears when an address mark has been detected. A high level on pin $\overline{AMENB}$ resets pin $\overline{AMD}$. CMOS output levels.
$\overline{SBD}$	O	SYNC BYTE DETECT: Transitions low upon detection of sync byte. This transition is synchronized to the sync byte. Once it transitions low, $\overline{SBD}$ remains low until RG goes low, at which point it returns high. CMOS output.
WD, $\overline{WD}$	O	WRITE DATA: Write data flip-flop output. The data is automatically resynchronized (independent of the delay between RCLK and WCLK) to the reference clock F_{TBG}, unless in Direct Write mode. Differential PECL output levels.
VRDT	O	VITERBI READ DATA: An input to the data separator back end, used for testing. TTL input levels or an AC coupled ECL signal. This pin is controlled by the VRDT bit in the *Control Test Register*.
$\overline{RDS}$	O	SERVO READ DATA: Read Data Pulse output for servo read data. Active low CMOS output. Output active when SG is high, and high when SG is low.
PPOL	O	SERVO READ DATA POLARITY: Read Data Pulse polarity output for servo read data. Active high CMOS output. Negative pulse = low, positive pulse = high. Output active when SG is high.

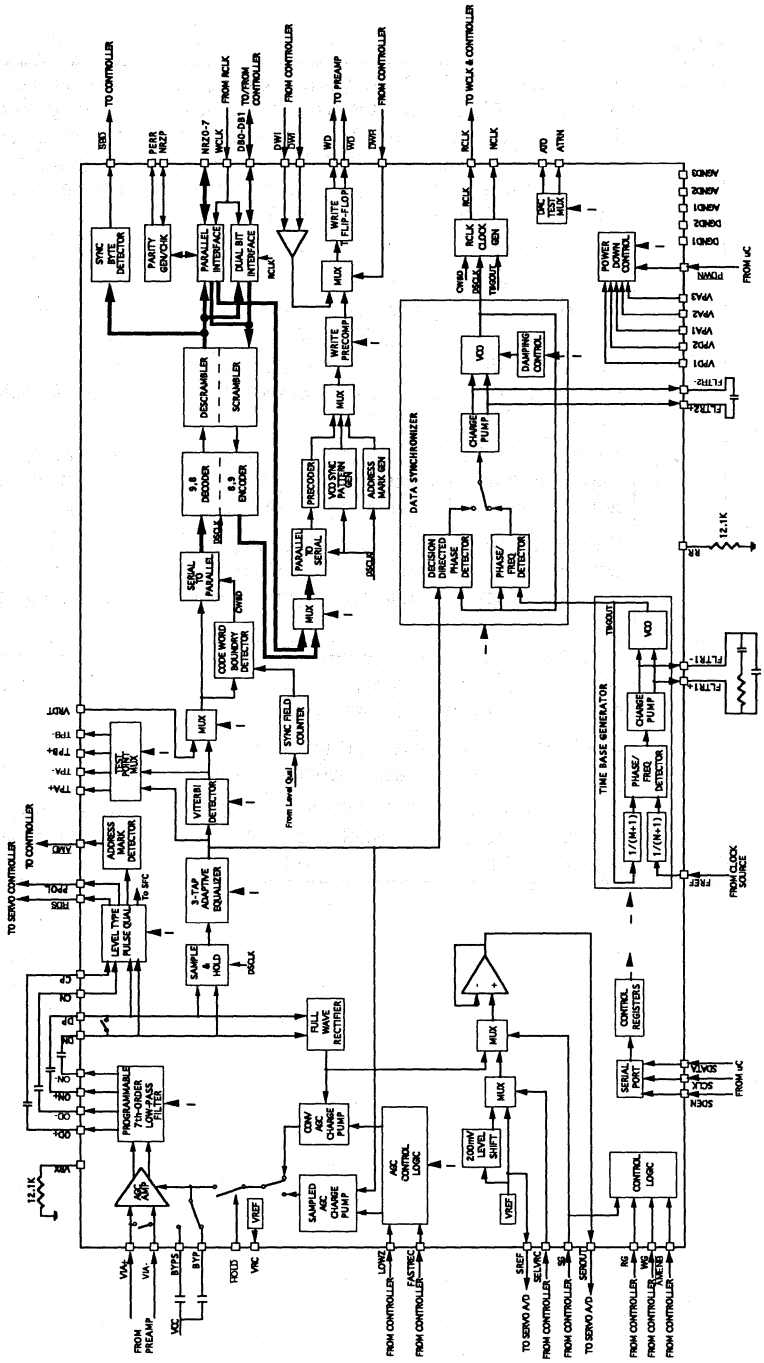
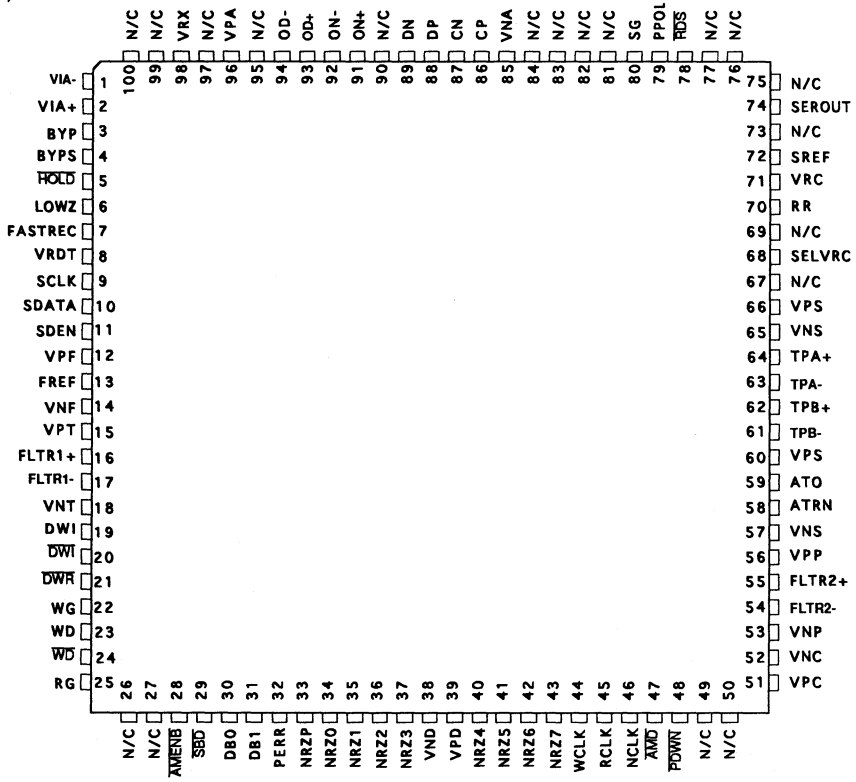


FIGURE 12: Application Diagram

PACKAGE PIN DESIGNATIONS

(Top View)



100-Lead TQFP

CAUTION: Use handling procedures necessary for a static sensitive component.

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NOTE: This is an abridged version of the 32P4901 (x2) data sheet. For a complete copy call 1-800-624-8999 ext. 151

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914

Notes:

Section 7

HDD HEAD POSITIONING

silicon systems®
A TDK Group Company

SSI 32H569
Servo Motor Driver

December 1993

DESCRIPTION

The SSI 32H569 Servo Motor Driver is a bipolar device intended for use in Winchester disk drive head positioning systems employing linear or rotary voice coil motors. When used in conjunction with a position controller, such as the SSI 32H6220 Servo Controller, and a position reference, such as the SSI 32H6210 Servo Demodulator, the device allows the construction of a high performance, dedicated surface head positioning system.

The SSI 32H569 serves as a transconductance amplifier by driving 4 MOSFETs in an H-bridge configuration, performs motor current sensing and limits motor current and velocity. In its linear tracking mode, class B operation is guaranteed by crossover protection circuitry, which ensures that only one MOSFET in each leg of the H-bridge is active. The MOSFET drivers are disabled when motor velocity or current exceed externally programmable limits. In addition, automatic head retraction and spindle braking may be initiated by a low voltage condition or upon external command.

(continued)

FEATURES

- **Predriver for linear and rotary voice coil motors**
- **Interfaces directly to MOSFET H-Bridge motor driver**
- **Class B linear mode and constant velocity retract mode**
- **Precision differential amplifier for motor current sensing**
- **Motor current and velocity limiting circuitry**
- **Automatic head retract and spindle braking signal on power failure**
- **External digital enable**
- **Servo loop parameters programmed with external components**
- **Advanced bipolar IC requires under 240 mW from 12V supply**
- **Available in 20-pin DIP or SO packaging**

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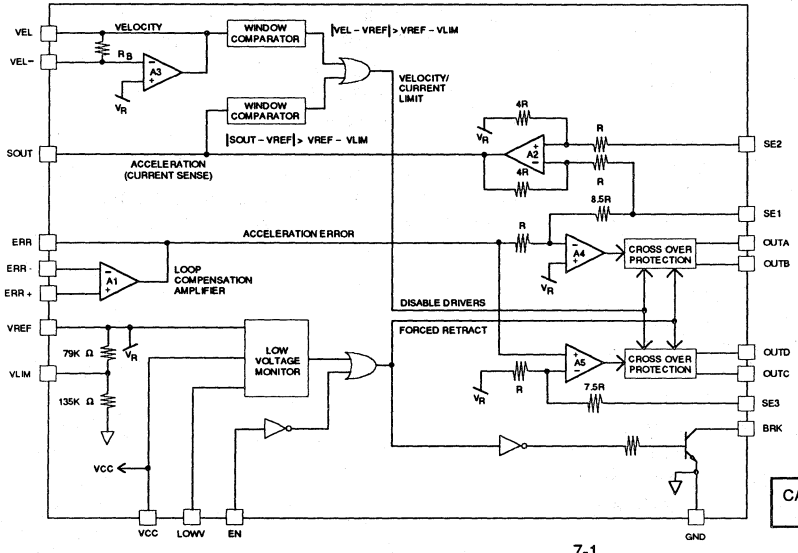
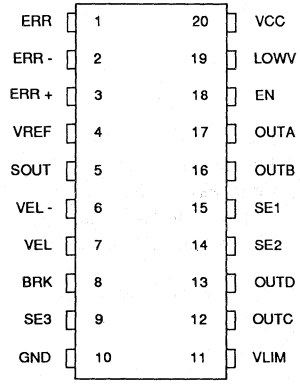
BLOCK DIAGRAM



PIN DIAGRAM



20-Pin SO, DIP

CAUTION: Use handling procedures necessary for a static sensitive component.

DESCRIPTION (continued)

The SSI 32H569 is implemented in an advanced bipolar process and dissipates less than 240 mW from a 12V supply. The IC is available in 20-pin DIP and 20-pin SO packaging.

FUNCTIONAL DESCRIPTION

(Refer to block diagram and typical application Fig.2)

The SSI 32H569 has two modes of operation, linear and retract. The retract mode is activated by a power supply failure or when the control signal EN is false. Otherwise the device operates in linear mode.

During linear operation, an acceleration signal from the servo controller is applied through amplifier A1, whose three connections are all available externally. RC components may be used to provide loop compensation at this stage. The ERR signal drives two precision amplifiers, each with a gain of 8.5. The first of these amplifiers is inverting, and is formed from opamp A4, an on-chip resistor divider and an off-chip complementary MOSFET pair. The second is non-inverting, and is formed in a similar manner from opamp A5. Feedback from the MOSFET drains, on sense inputs SE1 and SE3, allows the amplifiers gains to be established precisely. The voice coil motor and a series current sense resistor are connected between SE1 and SE3.

Crossover protection circuitry between the outputs of A4 and A5, and the external MOSFETs, ensures class B operation by allowing only one MOSFET in each leg of the H-bridge to be in conduction. The crossover separation threshold, illustrated in Figure 5, is the maximum drive on any MOSFET gate when the motor voltage changes sign. The crossover circuitry can also disable all MOSFETS simultaneously (to limit motor current or velocity) or apply a constant voltage across the motor (to retract the heads at a constant velocity).

Motor current is sensed by a small resistor placed in series with the motor. The voltage drop across this resistor is amplified by a differential amplifier with a gain of 4 (A2 and associated resistors), whose inputs are SE1 and SE2. The resulting voltage, SOUT, is proportional to motor current, and hence acceleration. This signal is externally fed back to A1, so that the signal ERR represents the difference between the desired acceleration (from the servo controller) and the actual motor acceleration. If SOUT is integrated, using opamp A3 and an external RC network, the resulting signal, VEL, is proportional to the motor velocity.

Both SOUT and VEL are connected to window comparators, which are used to detect excessive motor current or velocity. The comparator outputs disable the MOSFET drivers until the motor comes within limits again. The VLIM pin may be used to program the voltage limits for the window comparators. The maximum voltage excursion allowed about VREF is (VREF-VLIM). An on-chip resistor divider sets a default value for VLIM and if VLIM is connected to ground, the windowing is effectively disabled.

The SSI 32H569 has low voltage monitor circuitry that will detect a loss of voltage on the VREF, VCC or LOWV pins. The power supply pin, VCC, should be connected to the disk drive's spindle motor so that its stored rotational energy may be used to hold up VCC briefly during a power failure. LOWV is used to detect a system power supply failure. When a low voltage condition is detected, the MOSFET drivers switch from linear operation to retract mode. In this mode a constant voltage is applied across the motor which will cause the heads to move at a constant speed. A mechanical stop must be provided for the heads when they reach a safe location. The current limiting circuitry will disable the MOSFET drivers when motor current increases due to loss of the velocity-induced back EMF. An open collector output, BRK, which is active while the device is in retract mode, is provided for spindle motor braking. An external RC delay may be used to defer braking until the heads are retracted. For proper operation of the SSI 32H569, a pullup resistor on BRK is required even if the BRK output is not used.

An example of an entire servo path implemented with the SSI 32H569 and its companion devices, the SSI 32H6210 and 32H6220, is shown in Figure10.

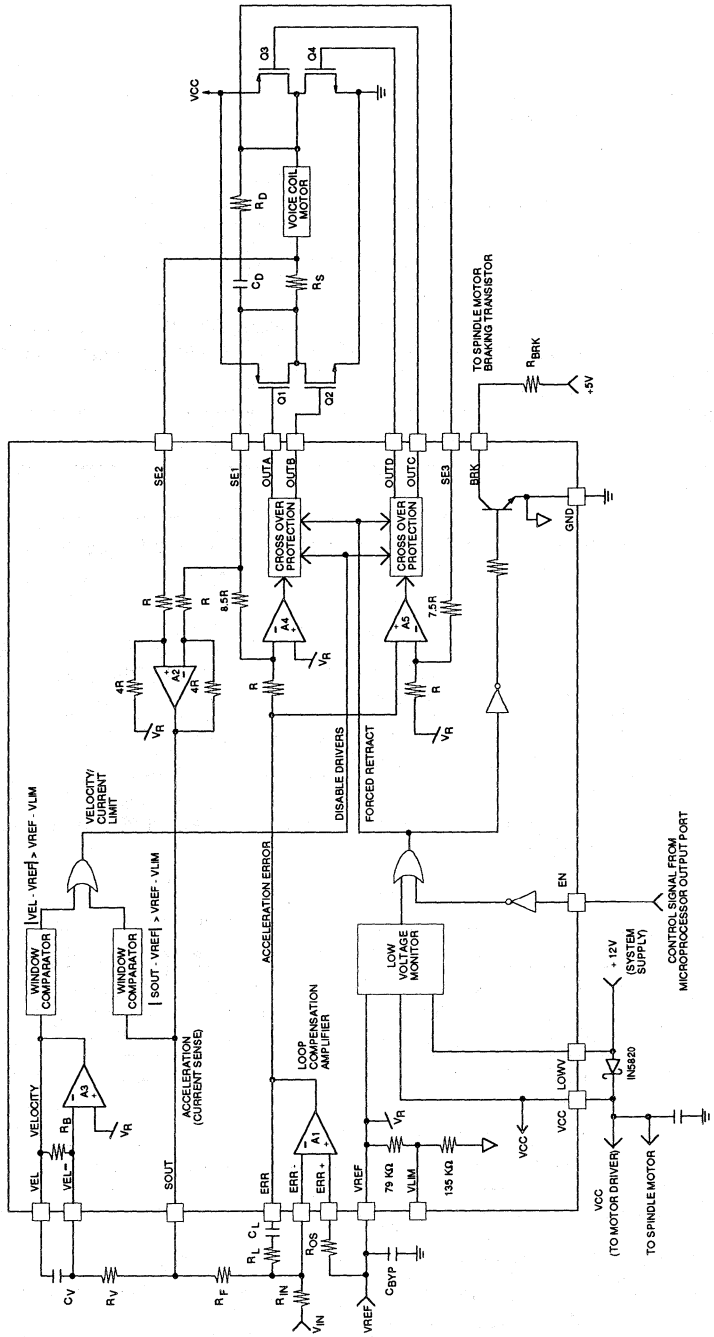


FIGURE 2: Typical Application

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PIN DESCRIPTION

POWER

NAME	PIN	TYPE	DESCRIPTION
VCC	20	-	POSITIVE SUPPLY - 12V power supply. Usually taken from spindle motor supply. Spindle motor stored energy permits head retraction during power failure. If VCC falls below 9V, a forced head retraction occurs.
LOWV	19	I	LOW VOLTAGE - System 12V supply. If this input falls below 9V, a forced head retraction occurs.
VREF	4	I	REFERENCE VOLTAGE - 5.4V input. All analog signals are referenced to this voltage. If VREF falls below 4.3V, a forced head retraction occurs.
GND	10	-	GROUND

CONTROL

NAME	PIN	TYPE	DESCRIPTION
ERR	1	O	POSITION ERROR- Loop compensation amplifier output. This signal is amplified by the MOSFET drivers and applied to the motor by an external MOSFET H-bridge, as follows: SE3-SE1 = 17(ERR-VREF)
ERR-	2	I	POSITION ERROR INVERTING INPUT - Inverting input to the loop compensation amplifier.
ERR+	3	I	POSITION ERROR NON-INVERTING INPUT - Non-inverting input to the loop compensation amplifier.
SOUT	5	O	MOTOR CURRENT SENSE OUTPUT - This output provides a voltage proportional to the voltage drop across the external current sense resistor, as follows: SOUT-VREF=4(SE2-SE1)
VEL-	6	I	VELOCITY INVERTING INPUT - Inverting input to the velocity integrating amplifier. The non-inverting input is connected internally to VREF.
VEL	7	O	VELOCITY OUTPUT - Output of the velocity integration amplifier. This signal is internally applied to a window comparator whose output limits motor drive current when the voltage at VEL exceeds a set limit.
BRK	8	O	BRAKE OUTPUT - Active high, open collector output which may be used to enable an external spindle motor braking transistor upon power failure or deassertion of EN.
VLIM	11	I	LIMITING VOLTAGE - The voltage at this pin sets motor current and velocity limits. Limiting occurs when: |SOUT-VREF|>VREF-VLIM or |VEL-VREF|>VREF-VLIM. An internal resistor divider establishes a default value that may be externally adjusted.

CONTROL (Continued)

NAME	PIN	TYPE	DESCRIPTION
SE2	14	I	MOTOR CURRENT SENSE INPUT - Non-inverting input to the current sense differential amplifier. It should be connected to one side of an external current sensing resistor in series with the motor. The inverting input of the differential amplifier is connected internally to SE1.
EN	18	I	ENABLE - Active high TTL compatible input enables linear tracking mode. A low level will initiate a forced head retract.

FET DRIVE

NAME	PIN	TYPE	DESCRIPTION
SE3	9	I	MOTOR VOLTAGE SENSE INPUT - This input provides feedback to the non-inverting MOSFET driver amplifier. It is connected to one side of the motor. The gain to this point is: SE3-VREF = 8.5(ERR-VREF)
OUTC	12	O	P-FET DRIVE (NON-INVERTING) - Drive signal for a P channel MOSFET connected between one side of the motor and VCC. This MOSFET drain is connected to SE3.
OUTD	13	O	N-FET DRIVE (NON-INVERTING) - Drive signal for an N channel MOSFET connected between one side of the motor and GND. This MOSFET drain is connected to SE3. Crossover protection circuitry ensures that the P and N channel devices driven by OUTC and OUTD are never enabled simultaneously.
SE1	15	I	MOTOR VOLTAGE SENSE INPUT - This input provides feedback to the inverting MOSFET driver amplifier. It is connected to the current sensing resistor which is in series with the motor. The gain to this point is: SE1-VREF = -8.5(ERR-VREF) This input is internally connected to the current sense differential amplifier inverting input.
OUTB	16	O	N-FET DRIVE (INVERTING) - Drive signal for an N channel MOSFET connected between the current sense resistor and GND. This MOSFET drain is also connected to SE1.
OUTA	17	O	P-FET DRIVE (INVERTING) - Drive signal for a P channel MOSFET connected between the current sense resistor and VCC. This MOSFET drain is also connected to SE1. Crossover protection circuitry ensures that the P and N channel devices driven by OUTC and OUTD are never enabled simultaneously.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

(Maximum limits indicates where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC operating characteristics.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VCC		0		16	V
VREF		0		10	V
SE1, SE2, SE3		-1.5		15	V
All other pins		0		14	V
Storage temperature		-45		165	°C
Solder temperature	10 sec duration			260	°C

RECOMMENDED OPERATION CONDITIONS (Unless otherwise noted, the following conditions are valid throughout this document.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VCC	Normal Mode	9	12	13.2	V
	Retract Mode	3.5V		14	V
VREF		5		7	V
Operating temperature		0		70	°C

DC CHARACTERISTICS

ICC, VCC current				20	mA
IREF, VREF current				2	mA

A1, LOOP COMPENSATION AMPLIFIER

Input bias current				500	nA
Input offset voltage				3	mV
Voltage swing	About VREF	2			V
Common mode range	About VREF	±1			V
Load resistance	To VREF	4			kΩ
Load capacitance				100	pF
Gain		80			dB
Unity gain bandwidth		0.5			MHz
CMRR	f<20 kHz	60			dB
PSRR	f<20 kHz	60			dB

A2, CURRENT SENSE AMPLIFIER

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input impedance	SE1 to SE2	3.5	5		kΩ
Input offset voltage				2	mV
Output voltage swing		VREF-4		VCC-1.2	V
Common mode range		0		VCC-0.2	V
Load Resistance	To VREF	4			kΩ
Load Capacitance				100	pF
Output impedance	f<40 kHz			20	Ω
Gain (SOUT-VREF)/(SE1-SE2)	$V_{SE2} = V_{REF}$	3.9	4	4.1	V/V
Unity gain bandwidth		0.5			MHz
CMRR	f<20 kHz	52			dB
PSRR	f<20 kHz	60			dB

A3, VELOCITY INTEGRATING AMPLIFIER

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input bias current				250	nA
Input offset voltage				2	mV
Voltage swing		VREF-4		VCC-1.2	V
Common mode range		4.5		6	V
Load resistance	To VREF	10			kΩ
Load capacitance				100	pF
RB, internal feedback resistor		80		150	kΩ

WINDOW COMPARATORS AND LIMITING

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Window comparator threshold (SOUT-VREF or VEL-VREF)		VREF-VLIM			V
Threshold hysteresis		35	50	65	%
VLIM voltage	No external parts	VREF-1.8		VREF-2.2	V
VLIM input resistance		50			kΩ

POWER SUPPLY MONITOR

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VCC fail threshold		8.5	9	9.8	V
LOWV fail threshold	|ILowv| < 0.5 mA	8.5	9	9.8	V
VREF fail threshold		3.9	4.3	4.8	V
Hysteresis (LOWV, VCC)			250		mV
Hysteresis (VREF)			110		mV
EN input low voltage	|IIL| < 0.5 mA	0.8			V
EN input high voltage	|IIH| < 40 uA			2	V
BRK voltage	normal mode, |IOL| < 1 mA			0.4	V
BRK leakage current	retract mode			10	µA
BRK delay (from power fail or EN false to BRK floating)				1	ms

MOSFET DRIVERS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SE3 Input impedance	To VREF	10	25		kΩ
OUTA, OUTC voltage swing |Io|<1 mA		0.7		VCC-1	V
OUTB, OUTD voltage swing |Io|<1 mA		1		VCC-1	V
VTH, Crossover separation threshold				2	V
Slew rate (OUTA, OUTB, OUTC, OUTD)	Cl<1000 pF	1.4			V/µs
Crossover time	300 mV step at ERR			5	µs
Output impedance (OUTA,B,C,D)			50		kΩ
Transconductance I(OUTA,B,C,D)/(ERR-VREF)			8		mA/V
Gain (-(SE1-VREF)/(ERR-VREF) or (SE3-VREF)/(ERR-VREF))		8	8.5	9	V/V
Offset current	R_S = 0.2Ω, R_F = R_{IN}, V_{IN}=VREF			20	mA
Retract motor voltage (SE1-SE3)		0.7	1	1.3	V

APPLICATIONS INFORMATION

A typical SSI 32H569 application is shown in Figure 2. The selection criteria for the external components shown are discussed below. Figure 3 shows the equivalent circuit and equations for the DC motor used in the following derivations. While the nomenclature chosen is for a rotating motor, the results are equally applicable to linear motors.

MOTOR CURRENT SENSE AND LIMITING

The series resistor which senses motor current, Rs, is chosen to be small compared to the resistance of the motor, Rm. A value of Rs = 0.2Ω is typical in disk drive applications. The window comparator threshold, programmed by VLIM, must be chosen to cause limiting when the motor current reaches its maximum permissible value. If iMAX is the maximum motor current in Amps, then this value may be chosen as follows:

$$VLIM = VREF - 4 \cdot R_s \cdot iMAX \ (V)$$

VLIM may be set with a resistor divider whose thevenin resistance is substantially less than the output resistance of the VLIM pin (50 kΩ). The window comparators have hysteresis (typically 50% of their threshold, VREF-VLIM) to prevent multiple triggerings of the driver disable signal.

VELOCITY LIMITING

The values of Rv and Cv in the velocity integrator are chosen to produce a voltage excursion of VREF-VLIM, when the motor speed is at its maximum permissible value. Rv must be large enough to prevent overloading of opamp A2. The following equation ignores the effect of RB, the internal resistor between VEL and VEL- which prevents saturation of A3 due to offsets. For the motor in Figure 3, with maximum velocity ωMAX (rad/s) these components may be chosen as follows:

$$R_V \,//\, R_F > 4\,k\Omega \ (\text{A2 output loading restriction})$$

$$C_V = \frac{4 R_s \cdot J\theta \cdot \omega MAX}{(VREF - VLIM) \cdot R_V \cdot K_m} \ (F)$$

LOOP COMPENSATION

The transfer function of the SSI 32H569 in the application of Figure 2 is shown in Figure 4(a). If the zero due to RL and CL in the loop compensation circuit is chosen to cancel the pole due to the motor inductance, Lm, then the transfer function can be simplified as shown in figure 4(b), under the assumption that this pole and the pole due to the motor mechanical response are widely separated. CL may then be chosen to set the desired open loop unity gain bandwidth.

$$C_L = \frac{68 \cdot R_s}{2 \cdot \pi \cdot R_F \cdot (R_m + R_s) \cdot BW}$$

where BW is the unity gain open loop bandwidth

$$R_L = \frac{L_m}{C_L \cdot (R_m + R_s)}$$

The closed loop response of the servo driver and motor combination, using the component values and simplifying assumptions given above, is given by:

$$\frac{i_m}{V_{in}}(s) = -\frac{1}{R_{in}} \cdot \frac{R_F}{4 \cdot R_s} \cdot \frac{1}{\left(1 + \frac{s}{2 \cdot \pi \cdot BW}\right)}$$

(This analysis neglects the pole due to the output impedance of the MOSFET drivers and the MOSFET gate capacitance, an effect that may be significant in some systems).

RF is chosen to be sufficiently large to avoid overloading A2 ($R_F \,//\, R_V > 4k\Omega$). The input resistor, RIN, sets the conversion factor from servo controller output voltage to servo motor current. RIN is chosen such that the servo controller internal voltages are scaled conveniently. The resistor ROS is optional and cancels out the effect of the input bias current of A1.

$$R_{os} = R_{in} \,//\, R_F$$

The external components RD and CD have no effect on the motor dynamics, but may be used to improve the stability of the MOSFET drivers. The load represented by the motor, ZM, is given by:

At frequencies above $(Rs+Rm)/(2 \cdot \pi \cdot Lm)$ Hz, this load

$$ZM = (R_s + R_m)\left(1 + s\frac{L_m}{R_s + R_m}\right)\left(1 + \frac{K_m^2}{s \cdot J\theta \cdot (R_s + R_m)}\right)(\Omega)$$

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LOOP COMPENSATION (continued)

becomes entirely inductive, which is undesireable. R_D and C_D may be used to add some parallel resistive loading at these frequencies.

H-BRIDGE MOSFETS

The MOSFETs chosen for the H-bridge should have gate capacitances in the range of 500-1000 pF. The MOSFET input capacitance forms part of the compensation for the MOSFET drivers, so values below 500 pF may cause some driver instability. Excessive input capacitance will degrade the slew mode performance of the drivers.

When the motor voltage is changing polarity, the crossover protection circuits at outputs OUTA-OUTD ensure that the maximum MOSFET gate drive is less than 2V (the crossover separation threshold), as illustrated in Figure 5. The thresholds of the MOSFET devices chosen should be as large as possible to minimize conduction in this region. If the device thresholds are significantly less than the crossover separation threshold, the N and P channel devices in each leg of the H-bridge will conduct simultaneously, causing unnecessary power dissipation.

POWER FAILURE OPERATION

The power supply for the SSI 32H569, VCC, should be taken from the system 12V supply through a Schottky diode (maximum 0.5V drop at If = 3A) and connected to the disk drive spindle motor. If the system power fails, the IC will continue to operate as the spindle motor becomes a generator. The SSI 32H569 will detect the power failure and cause a forced head retract, continuing to operate with VCC as low as 3.5V. The power fail mode will commence if either VCC or LOWV falls below 9V, or VREF falls below 4.3V, or EN is false. Hysteresis on the low voltage thresholds prevents the device from oscillating between operating modes when the power supply is marginal.

The BRK output, which is pulled low during normal operation, floats during a power failure. This allows an external transistor to be enabled for spindle motor braking. An external RC delay may be added to defer braking until head retraction is complete, since the spindle motor is required to generate the supply voltage during retraction.

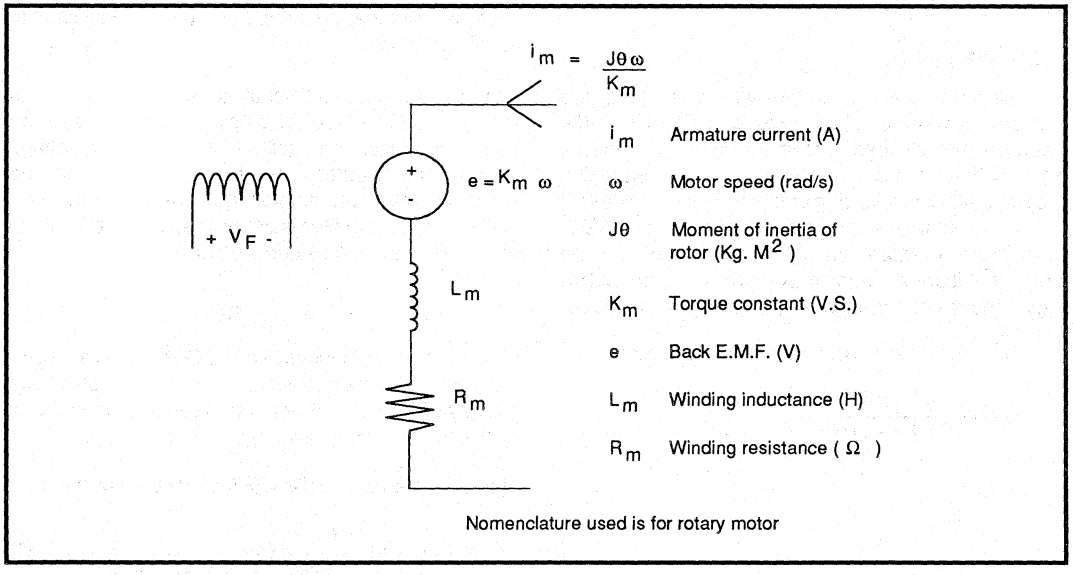


FIGURE 3: Equivelant Circuit For Fixed Field DC Motor

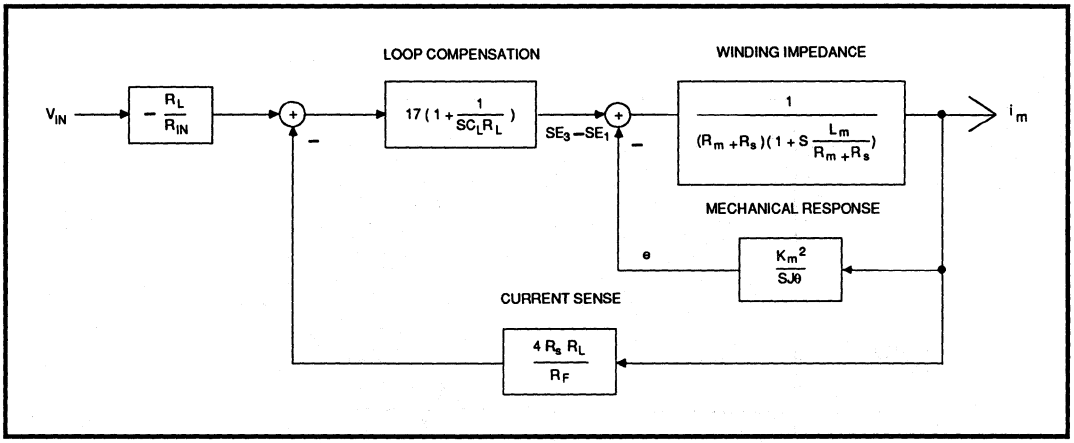


FIGURE 4(A): Transfer Function of SSI 32H569 in Typical Application with Fixed Field DC Motor

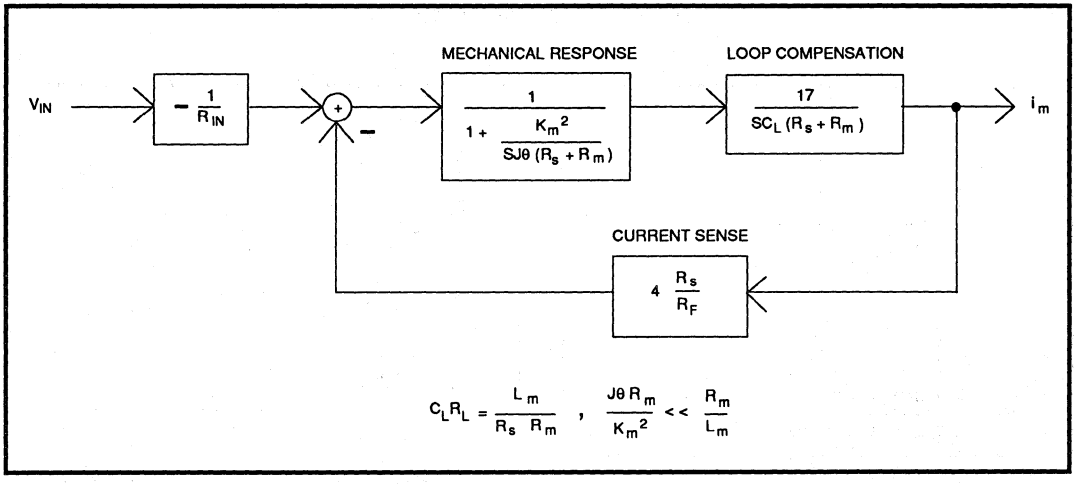


FIGURE 4(B): Simplified Transfer Function of SSI 32H569 in DC Motor Application

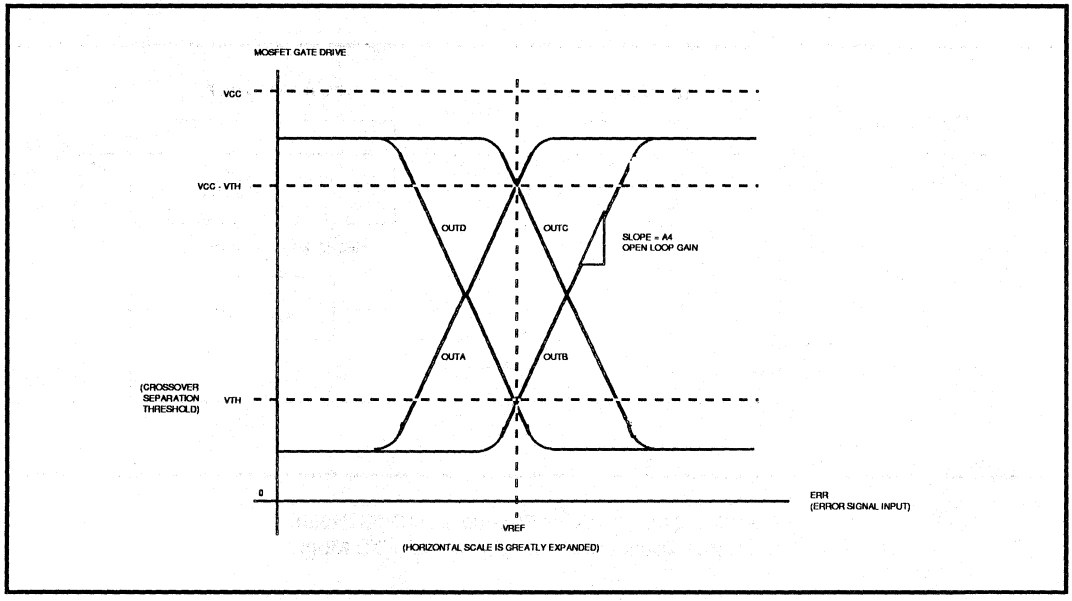


FIGURE 5): Crossover Protection

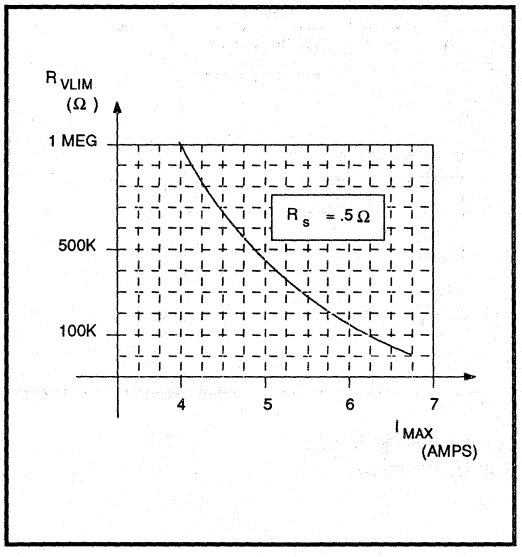


FIGURE 6: RVLIM To Ground Typical Motor Current Limit

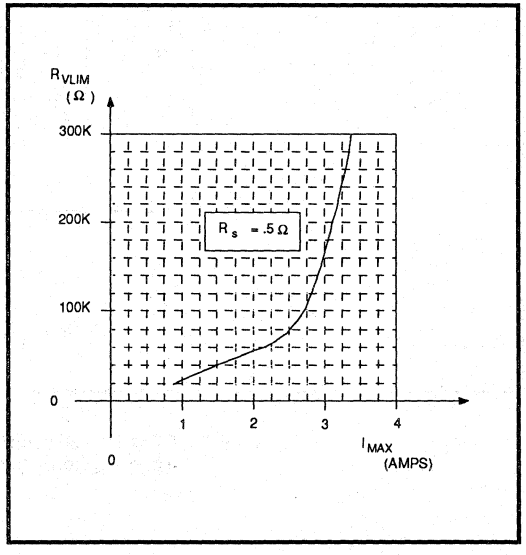


FIGURE 7: RVLIM To VREF Typical Motor Current Limit

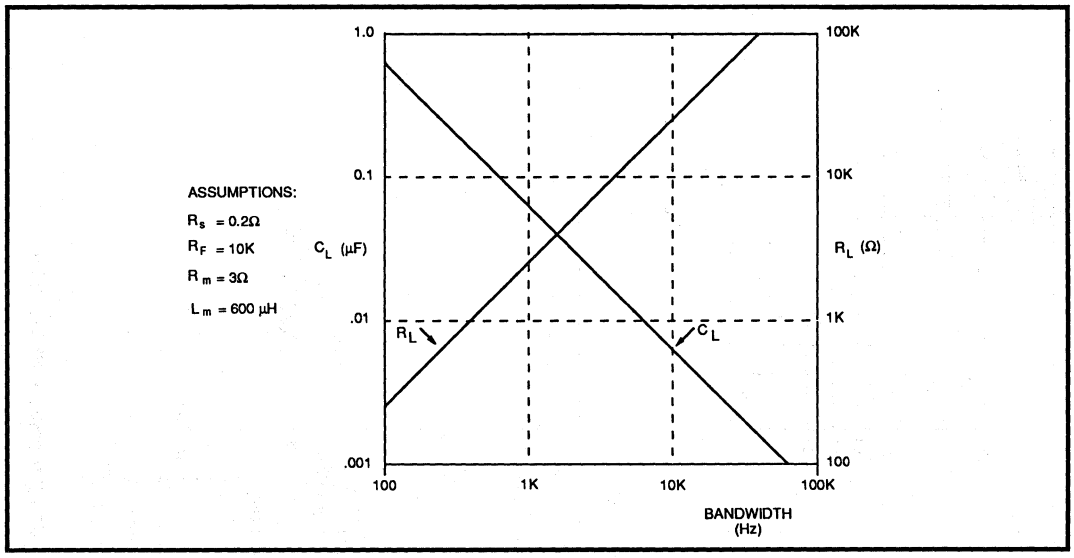


FIGURE 8: Typical Motor Driver Compensation

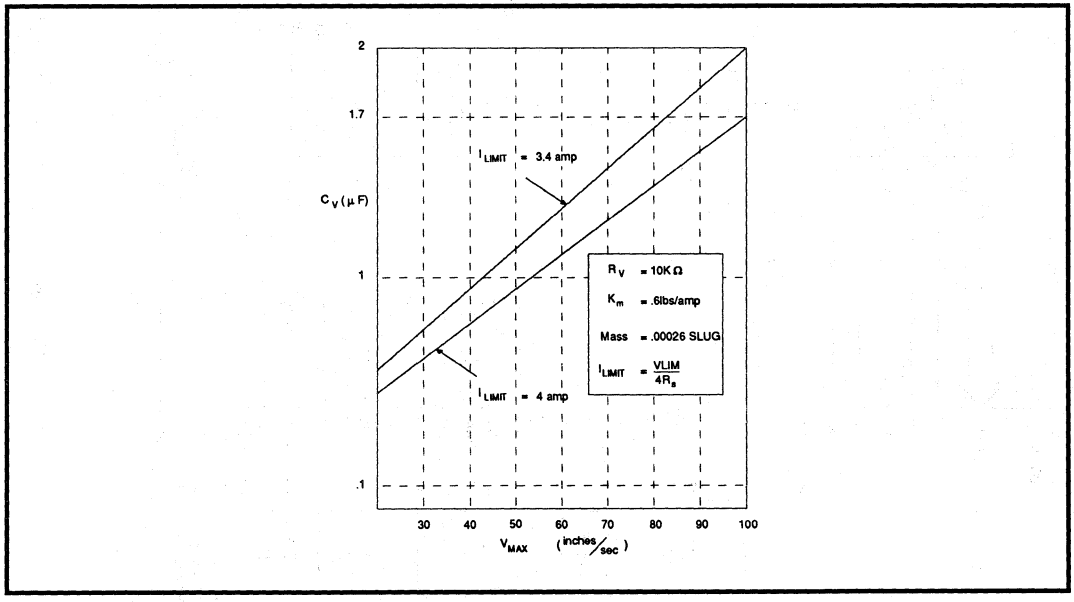


FIGURE 9: Typical Motor Velocity Limit

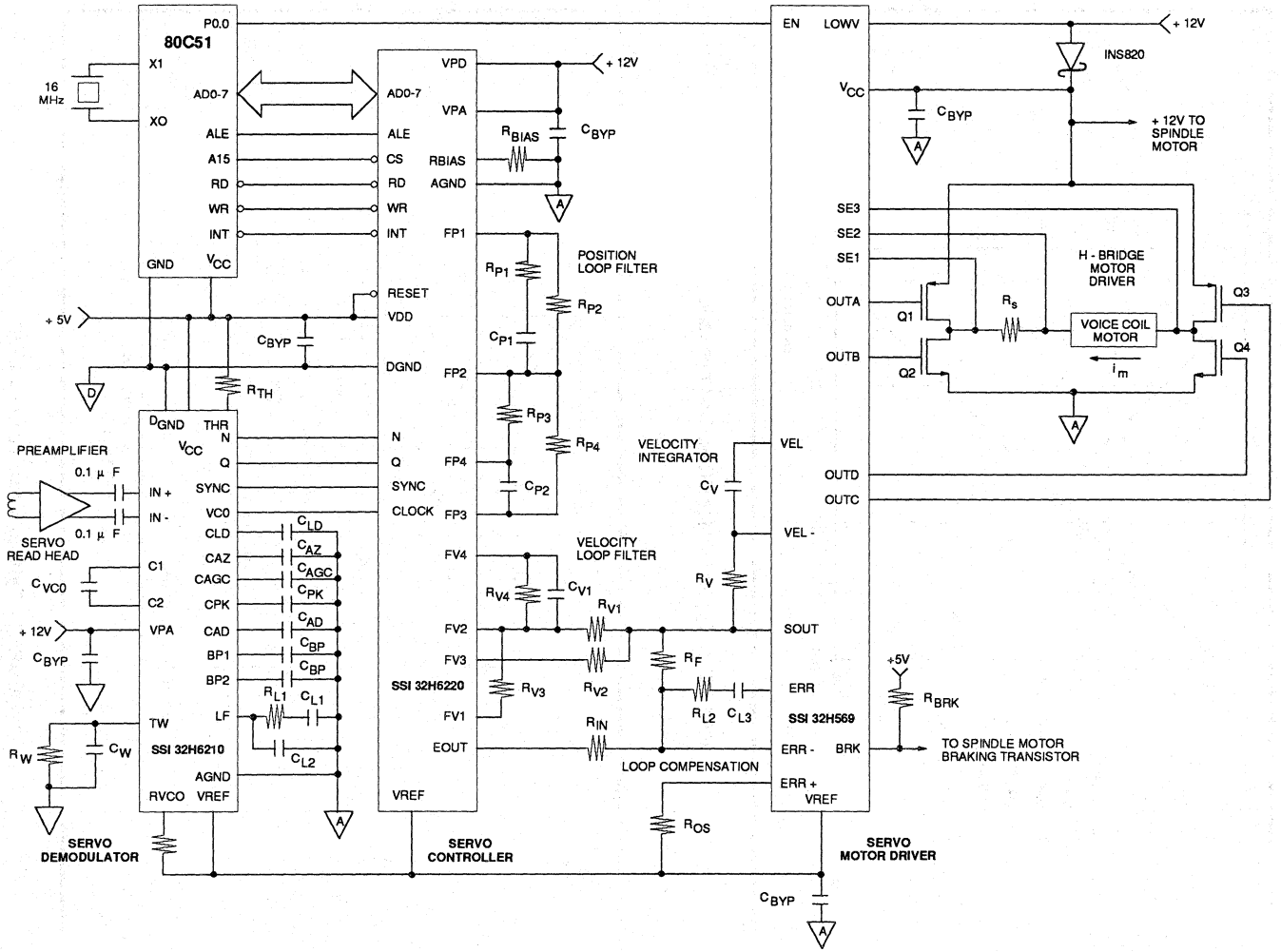
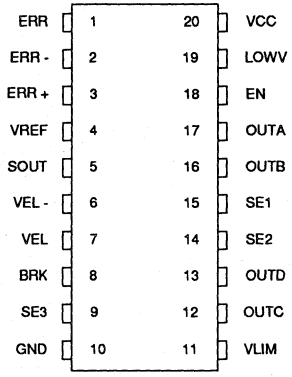


FIGURE 10: Complete Example of Servo Path Electronics Using the SSI 32H6210/ 6220/ 569

PACKAGE PIN DESIGNATIONS

(Top View)



20-Pin SO, DIP

CAUTION: Use handling procedures necessary for a static sensitive component.

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ORDERING INFORMATION

PART DESCRIPTION	ORDER NUMBER	PACKAGE MARK
SSI 32H569, Servo Motor Driver		
20-Pin DIP	32H569-CP	32H569-CP
20-Pin SOL	32H569-CL	32H569-CL

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914

Notes:

silicon systems®
A TDK Group Company

SSI 32H4633
Hybrid Servo & Spindle Controller
Preliminary Data

December 1992

DESCRIPTION

The SSI 32H4633 is a CMOS monolithic integrated circuit housed in a 100-pin QFP and operates on a single +5V supply. In addition to supporting Winchester disk drives with embedded servo sectors and dedicated servo surface, it contains all timing and control functions necessary to start, drive, and brake a 3-phase, 4/8/12 pole brushless DC spindle motor without sensors. It also provides an 8-bit A/D converter at a conversion rate up to 250 kHz and a Motorola/Intel compatible bus interface (Motel) to popular microcontrollers such as the 8051 and 68HC11. The features for each functionally different section are summarized in the following:

FEATURES

Servo Head Positioning Control

- Servo control for Winchester disk drives with hybrid servo head positioning systems
- For use in microprocessor-based digital servo applications
- Accepts quadrature position signals N, Q from a dedicated servo demodulator
- 12-bit double-buffered cylinder crossing counter for dedicated seek algorithms
- Timing controller for embedded servo position burst sampling
- Peak detect and sample/hold circuits for up to four embedded servo bursts
- H-bridge MOSFET predriver for linear and rotary voice coil motor
- Class B linear mode and constant voltage retract mode
- Active head retract on power failure

Spindle Motor Speed Control

- 3-phase 4/8/12 pole bipolar/unipolar operation without need for sensors
- Precision speed regulation at 5400 RPM, with ±0.018% speed resolution
- "At speed" indication
- Motor peak current limiting function
- Pulse amplitude modulation (PAM) for bridge MOSFET drivers
- Dynamic braking function on power failure

Data Acquisition and Microprocessor Bus Interface

- Motel bus interface compatible with 8051 and 68HC11
- Ten internal registers and address decoding
- Internal 250 kHz 8-bit A/D and D/A converters

General Functions

- Voltage fault detection for up to two supply voltages
- Write gate guarding
- Low power CMOS design
- 100 pin QFP package

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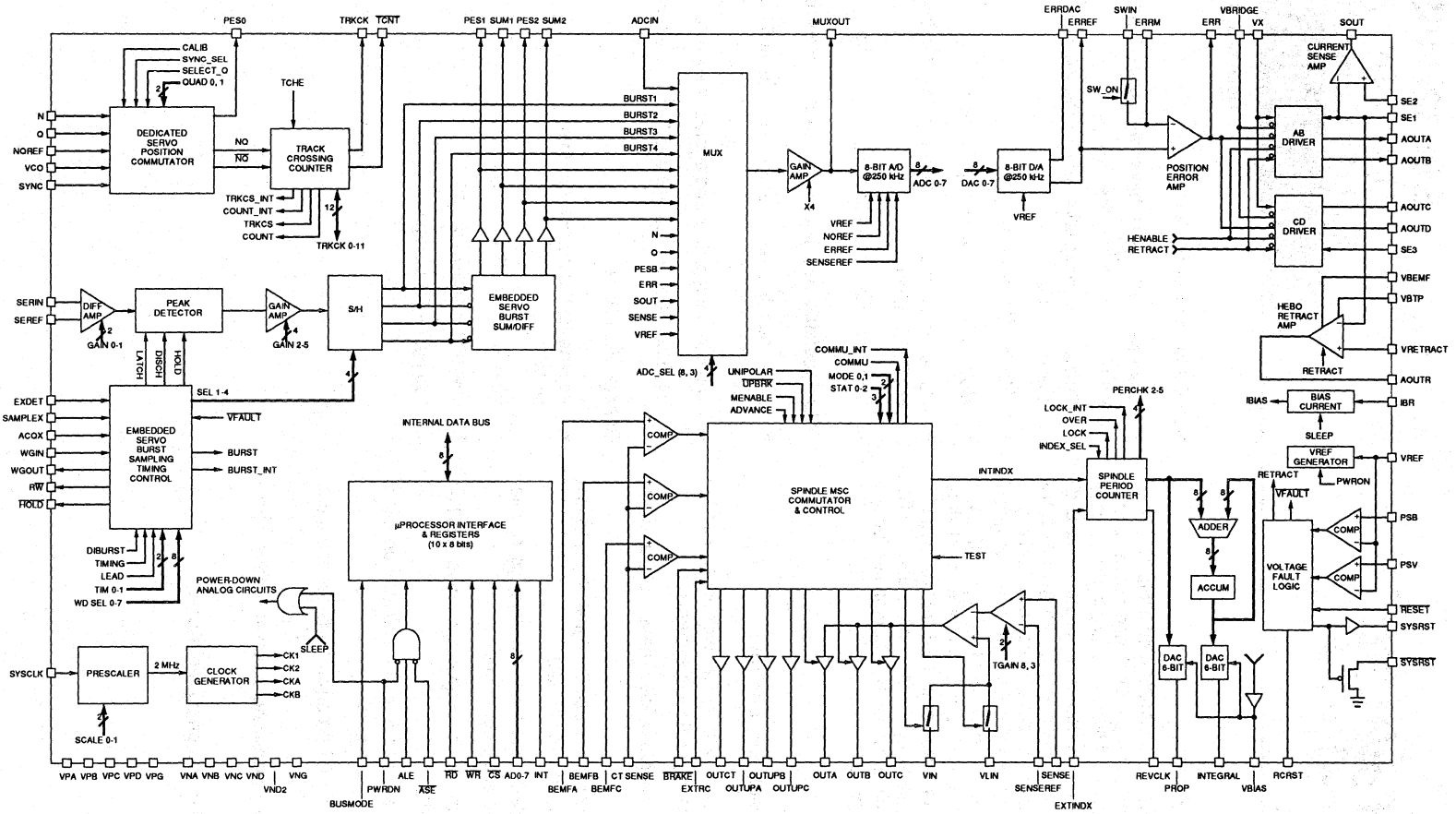

FIGURE 1: SSI 32H4633 Block Diagram

FUNCTIONAL DESCRIPTION

As shown in Figure 1, the SSI 32H4633 can be divided into three major sections: servo head positioning control, spindle motor speed control, data acquisition and microprocessor bus interface.

SERVO HEAD POSITIONING CONTROL

The SSI 32H4633 is intended for a servo head positioner for Winchester disk drives with both embedded servo sectors and a dedicated servo surface. The servo head positioning control section contains the following functions:

1. Dedicated servo position processor
2. Embedded servo burst amplitude processor
3. Embedded servo burst timing controller
4. Servo position error amplifier
5. H-bridge MOSFET predriver
6. Actuator current sense
7. Voltage fault detection and servo head retract

Figure 2 shows dedicated servo position processor. Figure 3 shows embedded servo burst amplitude processor with embedded servo burst timing controller. Figure 4 shows servo position error amplifier, H-bridge MOSFET predriver, actuator current sense. Figure 5 shows voltage fault and servo head retract logic.

DEDICATED SERVO POSITION PROCESSOR

The dedicated servo position processor receives quadrature position information from a servo demodulator, such as SSI 32H6210, through analog inputs N, Q and NQREF. The NQREF is applied to establish a DC reference level for N and Q samples. N and Q are sampled at the falling edge of SYNC. The SYNC frequency, which is the servo frame rate on the dedicated servo surface, is generated from the servo demodulator and is no more than 500 kHz. The VCO provides the necessary clock signal to sample N and Q signals. The timing relationship among VCO, SYNC and N, Q is indicated in Figure 2. If it is not necessary to synchronize to N, Q samples, the SYNC input must be grounded and the SYNC SEL bit in the SERVO CONTROL register set HIGH. In this case, the SYSCLK input will be divided down internally to generate the frame rate to sample N and Q signals. The position processor compares N with both Q and -Q to generate digital signals NQ (N>Q) and $N\overline{Q}$ (N>-Q). Since N and Q signals span four tracks per period, NQ and $N\overline{Q}$ provide additional information on which track the head is positioned. In order to produce the position error signal PES0, the position processor selects N, Q, -N or -Q, based upon either the values of bits QUAD0 and QUAD1 when SELECT Q is enable; or the values of the digital signals NQ and $N\overline{Q}$ when SELECT Q is disabled. Note that the analog inputs N and Q to the position processor will switch to the DC reference level, NQREF, when the CALIB bit in the HYBRID SERVO CONTROL register is enabled. This allows calibrating the internal offset of the position error signal, PES0. For digital servo applications, N, Q and PES0 are provided to the internal multiplexed 8-bit A/D converter under µP control.

The SSI 32H4633 supports both hardware and software track counting techniques. The software track counting technique interfaces with bits NQ, $N\overline{Q}$ and TRKCS in the SERVO STATUS register. On each track crossing, either NQ or $N\overline{Q}$ changes state.

An internal timing hysteresis can be provided to prevent multiple state changes on NQ, $N\overline{Q}$ and TRKCS at low head velocities by setting the bit TCHE in the EMBEDDED SERVO GAIN CONTROL register. The TRKCS bit will be reset LOW when the SERVO STATUS REGISTER is read by the µP. The hardware track technique interfaces with TRKCK, an output clock intended to drive a hardware counter such as is available in the Intel 8051 family. TRKCK is normally LOW and pulses HIGH once whenever a track boundary is crossed. A 12-bit double-buffered down counter with programmable loading capability is implemented to aid seek algorithms. The counter is decremented at the LOW-TO-HIGH transition of TRKCK and the register is updated at the HIGH-TO-LOW transition of TRKCK. The 12-bit counter register stops updating after the LSB is read. This ensures consecutive reads provide information that corresponds to a single track. Therefore, one should read the LSB and then the MSB without exception. The counter will produce a LOW level on $\overline{TCNT}$ when the terminal count is reached. $\overline{TCNT}$ remains LOW until the counter is loaded with a new initial value.

EMBEDDED SERVO BURST AMPLITUDE PROCESSOR

The embedded servo burst amplitude processor extracts the fine head position error information from the embedded servo bursts. The circuit acquires up to 4 burst amplitudes BURST1, BURST2, BURST3, and BURST4 from a read data channel, such as the SSI 32P4620, through analog inputs SERIN and SEREF. The SEREF is applied to establish a DC reference level for the full wave-rectified analog signal SERIN.
To accommodate a wide range of servo burst amplitudes, the differential signal between SERIN and SEREF is scaled by a 2-bit programmable gain amplifier under µP control. The gain of the differential amplifier ranges from -6 dB to 3 dB as defined in the EMBEDDED SERVO GAIN CONTROL register. The output of the differential amplifier is then provided to a peak detector which captures the peak voltage within a time interval derived from the internal timing controller or an external timing source through SAMPLEX. The peak voltage is further scaled by a 4-bit programmable gain amplifier under µP control. Thus the gain error introduced by the peak detector can be accurately corrected with this programmable gain amplifier. The gain adjustment ranges from 0 dB to 3 dB in 0.2 dB steps, as defined in the EMBEDDED SERVO GAIN CONTROL register. Each of the following four S/H circuits transfers and holds the scaled peak voltages onto their respective holding capacitors during a time interval defined by the internal timing controller or an external timing source through ACQX. The outputs of S/H circuits, BURST1, BURST2, BURST3, and BURST4, are provided to the 8-bit A/D converter under µP control. Note that the timing windows to acquire the scaled peak voltages can be configurated in any order, as defined in the EMBEDDED SERVO TIMING WINDOW CONTROL register. Therefore, the µP can mix and commutate servo bursts to accommodate for a variety of servo burst formats and maintain the position error signal in a proper polarity. The timing controller also issues a timing signal to discharge the captive voltage for each servo burst.

The captive signals are provided to two difference circuits to extract the differential signals between BURST1, BURST2 and BURST 3, BURST4, respectively. Typically, these differential signals define the distance between the read head and the center of a data track and one of them should be zero while the read head is at the center of a data track. These outputs, available externally on PES1 and PES2, are provided to the 8-bit A/D converter under µP control. Also, two summers add BURST1, BURST2 and BURST3, BURST4, respectively, and their outputs at SUM1 and SUM2 are provided to the 8-bit A/D converter as well.

EMBEDDED SERVO BURST TIMING CONTROLLER

The embedded servo burst timing controller generates all the timing signals to sample the position bursts, as shown in Figures 3 and 4. These timing signals control the discharge, sample, and hold of the peak detector and the four S/H circuits. The EMBEDDED SERVO TIMING WINDOW CONTROL register can be programmed by the µP to select and sample the servo burst pairs in any order. The number of servo position bursts supported are either two or four. The DIBURST bit in the SERVO CONTROL register, when set HIGH, configures the internal timing controller to sample only two servo position bursts. When reset, four servo position bursts are sampled. During position burst sampling, $\overline{HOLD}$ and $R\overline{W}$ will be asserted and WGOUT held LOW.

An external timing controller may be used to provide all the timing signals for the discharge, sample, and hold of the peak detector and the four S/H circuits by setting the TIMING bit HIGH in the SERVO CONTROL register. Usually, in this mode, an external timing controller ASIC will be required to provide the timing signals at SAMPLEX and ACQX for servo position burst sampling while the internal servo timing controller is disabled.

SERVO POSITION ERROR AMPLIFIER

The servo driver has two modes of operation, linear and retract. The retract mode is activated by a power supply failure or when the control signal $\overline{RESET}$ is LOW. Otherwise the driver operates in linear mode. During linear operation, the microcontroller acquires servo burst amplitudes and analyzes them to establish a position error signal. This signal travels through an 8-bit D/A converter and is applied to an amplifier whose three connections, ERRM, ERREF and ERR, are available externally. External RC components may be used to establish the gain and bandwidth of this amplifier. Additional analog input via SWIN may be provided to this amplifier by setting the SW ON bit in the SERVO CONTROL register.

FUNCTIONAL DESCRIPTION (continued)

H-BRIDGE MOSFET PREDRIVER

The error signal ERR generated from the position error amplifier drives two precision differential amplifiers, each with a gain of 15. The differential amplifier outputs, AOUTA, AOUTB, AOUTC and AOUTD drive an external MOSFET bridge powered by VBRIDGE. Feedback from the MOSFET drain terminals via sense inputs SE1 and SE3 allow the differential amplifier gains to be established precisely. The voice coil actuator and a current sense resistor are connected in series between SE1 and SE3. Included in the output control circuitry is a crossover protection function which ensures class B operation by permitting only one MOSFET in each leg of the bridge to be in conduction. The crossover circuit can be adjusted for different MOSFET threshold voltages with a resistor connected to VX. The crossover circuitry can be commanded by the µP to shut down the MOSFET drivers and thus remove current to the external bridge.

MOTOR CURRENT SENSE

Motor current is sensed by a small resistor placed in series with the actuator. The voltage drop across the resistor is level-shifted and amplified by a differential amplifier with a gain of 4. The resulting signal, SOUT, is proportional to actuator current. This signal is externally fed back to the position error amplifier so that the error signal ERR represents the difference between the desired and actual actuator currents.

VOLTAGE FAULT DETECTION AND SERVO HEAD RETRACT

A voltage fault detector which can monitor up to two voltage supplies is included to prevent the actuator from responding to a false error signal during a power failure. Retract mode is started when a power supply failure is sensed by the PSB or PSV comparators or when $\overline{\text{RESET}}$ is pulled LOW externally. During retract, a constant voltage is applied across the actuator in order to cause a constant velocity head retraction. This is accomplished by applying the voltage stored on VBYP to AOUTD and by driving AOUTR with an amplifier that monitors SE1. The amplifier is powered by VBEMF. During retract, VRETRACT is biased by an internal voltage reference and determines the retract voltage. At other times, power is saved by disconnecting VRETRACT from the voltage reference and letting it be pulled to VBEMF by a high value resistor. External components (a diode, for instance) can be connected between VRETRACT and ground to modify the retract voltage.

An open-drain output, $\overline{\text{SYSRST}}$, which is active LOW while the servo driver is in retract mode, is provided for spindle motor braking. An external RC delay may be used to defer braking until the head is retracted. The amount of $\overline{\text{SYSRST}}$ delay is determined by the external capacitor which is connected to the pin, RCRST.

SPINDLE MOTOR SPEED CONTROL

A functional block diagram for the spindle motor control is shown in Figure 1. In conjunction with several external components, the spindle motor speed control provides the starting, accelerating, and precise rotational speed regulation functions. The circuit will control 4, 8, or 12 pole brushless DC motors without the need for Hall sensors. It will operate in either bipolar or unipolar drive mode. Control, configuration, and status monitoring are handled by the µP. The complete speed control loop is contained in the circuit and the µP is only required during start and to monitor status.

SPINDLE MOTOR START-UP

Motor starting is accomplished with the µP utilizing various features contained in the motor speed control circuitry. The µP can write to the commutation counter and set it to a predetermined value with STATE0, STATE1, STATE2 bits. The counter can then be incremented with the ADVANCE bit which also excludes internal commutations when set HIGH. Bits COMMU, PERCHK 2, 3, 4, 5 provide feedback to the µP on motor activity. The µP can enable the drivers with MENABLE and UNIPOLAR bits as required, as well as cause a "soft" brake with $\overline{\text{UPBRK}}$.

Under µP control, initial open-loop commutation sequence is provided to the commutation logic which thereby advances and accelerates the spindle motor. The start-up process settles the motor initially by selecting the bits STATE0, STATE1, STATE2 in the SPINDLE CONTROL register to energize a proper motor winding. Motor current is enabled by setting the MEANABLE bit in the SPINDLE CONTROL register. The commutation state is advanced by providing ADVANCE pulses in the SPINDLE CONTROL register. The period of the ADVANCE pulses will be based upon the motor and load characteristics and decreased

gradually during the acceleration of the motor. The µP may look at the COMMU bit in the SPINDLE STATUS register for feedback indicating whether the motor has achieved a sufficient speed. Once the motor has achieved a sufficient speed, the µP will cease generating ADVANCE pulses and motor starting is thus completed.

SPINDLE MOTOR SPEED REGULATION

Motor speed regulation is accomplished with mixed analog and digital techniques, converting a motor speed error derived from a reference clock and a period counter into a voltage. The voltage translates into a motor current across the current sense resistor regulating the motor speed. The speed regulation loop consists of a period counter, proportional and integral channels, two 6-bit D/A converters and a linear transconductance amplifier.

In operation, the motor speed error is determined by measuring the period of each revolution with a 500 kHz clock signal. Period resolution is therefore 2 microseconds with the desired period being 5555 counts (11.11 milliseconds or 5400.54 RPM). Motor rotor position is determined by monitoring the coil voltage of the winding that is not presently being driven by the drivers. The back-emf at the coil in conjunction with the state of the output drivers indicates rotor position. The back-emf is compared to a reference at CTSENSE and initiates "commutation events" when the appropriate comparison is made. The commutation is the sequential switching of the drive current to the motor windings. Since the back-emf comparison event occurs prior to the time when optimum commutation should occur, it is thus required to delay actual commutation by a predetermined time after the comparison. The commutation delay is provided by a non-retriggerable one-shot circuit wherein the time delay is a function of external RC timing components connected at EXTRC. Because commutation of the motor windings typically results in large transient voltages which could falsely indicate "commutation events," the one-shot circuit also provides a "noise filter" function which holds off retriggering further and blanks the back-emf comparison events for a period of time (approximately one half the commutation delay) after commutation. The commutation states are defined in the SPINDLE CONTROL register.

The period counter is loaded with a count of 5555 initially, and period measurement results in residual counts (ideally zero) in the period counter as it counts down during the index-to-index time interval. The residual count is fed to the proportional D/A converter (5 bit plus sign) whose output is provided at PROP. No period error will output half of VBIAS at PROP, too short a period will output a value less than half of VBIAS, and too long a period will output a value greater than half of VBIAS depending on the amount of error.

When the residual count is within ± 15 counts of zero, the motor is indicated as "in lock." The lower eight bits of the period counter are fed to an accumulator which adds the present period residue to the previous accumulation thus accomplishing an integrating effect to force the speed error to zero over time. The upper six bits of the accumulator are fed to the integral DAC whose output is INTEGRAL. Gross period errors will cause PROP and INTEGRAL to saturate at the appropriate extreme to achieve the maximum corrective control voltage.

The outputs at PROP and INTERGRAL are connected to VIN with an external resistor network. The resistor values should be selected to set the required loop response based upon motor requirements. The input VIN is the non-inverting input of the linear transconductance amplifier which uses the lower driver transistor that is presently active per the commutation state. An external resistor is used to sense the current flowing through the drive transistor drain (and hence the motor coil current). The voltage across the sense resistor, the difference between SENSE and SENSEREF, is amplified by a programmable gain stage and fed to the inverting input of the transconductance amplifier. The gain of the programmable amplifier is determined by TGAIN0 and TGAIN1 bits.

Motor speed control includes a speed range check circuit, which provides in the SPINDLE STATUS register a LOCK status bit, when the motor is at the target speed within ±0.27%, along with OVER status bit, when the motor is over or under the target speed. The LOCK and OVER status bits are available to the µP for diagnostics and spindle fault conditions.

Additional low-speed period measurement data is available to the µP as the PERCHK2,3,4,5 bits in the SPINDLE STATUS register.

FUNCTIONAL DESCRIPTION (continued)

MOTOR PEAK CURRENT LIMITING

When the period error exceeds 256 counts too slow, the voltage at VLIM is selected as the control voltage in lieu of VIN. VLIM is to be used to set the motor peak current during start-up and acceleration.

MOTOR BRAKING

Fault conditions on power supplies and internal voltage reference generator will trigger an internal retract condition. The internal retract condition will cause all predriver outputs to the states which will turn the driver transistors off, allowing the motor to coast. $\overline{\text{BRAKE}}$ typically has a capacitor to ground attached and is connected to pin $\overline{\text{SYSRST}}$ via a resistor. $\overline{\text{SYSRST}}$ goes LOW in the retract condition, and thus $\overline{\text{BRAKE}}$ will go LOW after the RC delay. When $\overline{\text{BRAKE}}$ goes LOW, all lower drivers are activated to achieve dynamic braking of the motor. The circuitry for these operations is powered by the back-emf of the spindle motor and will operate without either 5 or 12 volt supply.

Dynamic braking can also be activated under µP control by setting $\overline{\text{UPBRK}}$ to LOW in the SPINDLE CONTROL register. During dynamic braking, the control loop is opened.

Two other motor speed control functions related to other circuit functions in the SSI 32H4633 are SLEEP mode and internal bias current. Two modes of SLEEP are provided for the SSI 32H4633, but the effect on the motor speed control is the same for both modes, i.e., all analog circuitry is de-biased, the clock is disabled, the upper driver outputs become logic HIGH (to turn off all upper drivers including the center tap if used), and the lower driver outputs become logic HIGH. The internal bias currents for analog functions are set by an external resistor connected between IBR and ground. A 22.6 KΩ, ±1% resistor should be used for proper operations.

EXTERNAL INDEX APPLICATION

Normal operation is performed with an internal index signal derived from the commutation counter (scaled via the MODE0 and MODE1 bits based upon the number of motor poles). The period of the index signals is measured and controlled by the circuit to result in a rotational rate of 5400 RPM. Within the range from 5384.9 to 5415.1 RPM, the spindle will be "in lock."

After the motor is started and accelerated to speed (LOCK bit HIGH), an external index signal may be selected. Applying external index pulses at a rate within the lock range and setting INDEX SEL bit to HIGH will start the following sequence:

The circuit will complete the period measurement of the latest internal index period and then begin to measure the time between the last internal index and the next external index pulse. This will most likely be shorter than the nominal assuming the two events are asynchronous. If the period measured is not within 4.6% of the expected value, 11.11 milliseconds, the proportional and integral D/A converters will not be updated with a new correction value but will continue to output the previous value. The LOCK bit will be set to LOW indicating "out of lock." The next period measured will be between the first and second external index pulses and will presumably be within the lock range so that LOCK will be set to HIGH. If the period is within 4.5% of the desired value, the proportional and integral D/A converters will be updated. Similarly, during operation with external index, a missing index pulse would look like a gross speed error and no update on proportional and integral D/A converters will take place. The µP must perform the corrective actions in such cases, by examining LOCK bit, the PERCHK2,3,4,5 bits, and the source of the (missing) index pulses. A single missing index should require no action other than checking that LOCK returns to HIGH (in lock) in the next interval.

DATA ACQUISITION AND MICROPROCESSOR BUS INTERFACE

Figure 1 shows data acquisition circuits along with the microprocessor bus interface. To facilitate microprocessor-based servo applications, the SSI 32H4633 contains a high-speed 8-bit A/D converter at a conversion rate up to 250 kHz, an 8-bit D/A converter, and Motel bus interface compatible with commonly used 12 MHz 8051 and 8 MHz 68HC11. The A/D converter can be multiplexed to sixteen different analog inputs by programming the ADC_SEL0, ADC_SEL1, ADC_SEL2 and ADC_SEL3 bits in the ADC ADDRESS register by the µP. The analog inputs can be scaled by a gain of 4 by setting the X4 bit HIGH. The output of the gain stage is available externally at MUXOUT for diagnostics. The A/D converter runs synchronously with the internal 500 kHz clock which is used for various circuits on the SSI 32H4633. Therefore, there would be a maximum of 2

microseconds of latency between a conversion request and the actual start of the conversion. Conversion is started by reading the A/D output register. The output is coded in 2's complement. Note that different voltage references corresponding to one half of the A/D full scale are used for different analog inputs as defined in the ADC ADDRESS register.

Similarly, the D/A converter runs synchronously with the internal 500 kHz clock and conversion is started by writing to the D/A input register. The output at ERRDAC is referenced to ERREF and is held constant between conversions.

The "Motel" interface to both Motorola and Intel µP's is provided for a direct connection to the SSI 32H4633. Three bus control signals are interpreted differently based upon the type of µP being used. The pin BUSMODE should be tied to HIGH for an Intel bus interface. The table below illustrates how both µPs connect to the SSI 32H4633. The $\overline{ASE}$ pin gates the AL/ASE input and can be used to shut off the ALE/AS to minimize noise on chip when the µP interface is not active. The $\overline{CS}$ pin performs a similar function on the rest of the µP bus inputs. The timing diagrams for Intel and Motorola µP interface are shown in Figures 5 and 6, respectively.

Intel	Motorola	32H4633
ALE	AS	ALE
$\overline{RD}$	DS;E; or Clock Phase 2	$\overline{RD}$
$\overline{WR}$	R/$\overline{W}$	$\overline{WR}$

REGISTER DESCRIPTIONS

The SSI 32H4633 contains ten 8-bit internal registers which provide control, option select and status monitoring. The registers are addressed with a 4-bit register address which is latched from inputs at AD0, AD1, AD2, and AD3 on the falling edge of ALE. The registers from 0 to 5 are read/write memory, the registers from 6 to 9 are write only. The registers are summarized in Table 1.

TABLE 1: SSI 32H4633 Internal Registers

ADDRESS	TYPE	REGISTER NAME
0	R/W	Interrupt Control/Status
1	R/W	Spindle Control/Status
2	R/W	Servo Control/Status
3	R/W	ADC Address/Data
4	R/W	Track Count LSB
5	R/W	Track Count MSB & Hybrid Servo Control
6	W	Error DAC Data
7	W	Embedded Servo Gain Control
8	W	Transconductance, Prescaler and Mode Control
9	W	Embedded Servo Timing Window Control

INTERRUPT CONTROL/STATUS REGISTER

Address: 0 Access: Read/Write Reset: 00
Register contents when Written to enable or disable interrupt events:

BIT	NAME	DESCRIPTION
0	COMMU INT	When set HIGH, interrupt is enabled on a state change of the back-emf commutation clock COMMU.
1	LOCK INT	When set HIGH, interrupt is enabled on a state change of the spindle speed lock.
2	BURST INT	When set HIGH, interrupt is enabled on the embedded servo position bursts ready.
3	TRKCS INT	When set HIGH, interrupt is enabled on each track crossing.
4	COUNT INT	When set HIGH, interrupt is enabled on the terminal count (000_H) of the track crossing counter.
5,6	-	Undefined.
7	MST INT	When set HIGH, the microprocessor signal $\overline{INT}$ is enabled.

Register contents when Read

BIT	NAME	DESCRIPTION
0	COMMU INT	Active high indicates a state change of the back-emf commutation clock COMMU.
1	LOCK INT	Active high indicates a state change of the spindle speed lock.
2	BURST INT	Active high indicates that the embedded servo position bursts are ready.
3	TRKCS INT	TRKCS INT is asserted when NQ or $N\overline{Q}$ changes state, i.e., on each track crossing.
4	COUNT INT	COUNT INT is asserted when the terminal count (000_H) of the track crossing counter is reached.
5,6	-	Undefined.
7	MST INT	Active high indicates that one or more interrupts are pending.

Each interrupt event status is reset when the µP reads the corresponding status register. Specifically, interrupt events COMMU INT and LOCK INT are reset whenever the SPINDLE STATUS register (ADDRESS=1) is read. Interrupt events TRKCS INT, COUNT INT and BURST INT are reset whenever the SERVO STATUS register (ADDRESS=2) is read. All interrupt events may be read as interrupt status regardless of their corresponding interrupt mask settings. The interrupt control register determines which event will actually cause a latched assertion of the µP signal $\overline{INT}$. Note that the MST INT is a master enable which disables all interrupt events from asserting $\overline{INT}$ when active low. Also, when read, MST INT indicates if any mask enabled interrupt events are still pending for service and reflects the internal state of the µP signal $\overline{INT}$.

SPINDLE CONTROL/STATUS REGISTER

Address: 1 Access: Read/Write Reset: 00
Register contents when Written:

BIT	NAME	DESCRIPTION
0	$\overline{\text{UPBRK}}$	When set LOW, dynamic braking will be initiated where upper drivers are disabled and lower drivers are activated.
1	UNIPOLAR	This bit is set HIGH when unipolar motor is used. For unipolar motors, all upper drivers are disabled and OUTCT is activated.
2	INDEX SEL	When set HIGH, the input signal at EXTINDX, one pulse per revolution, is selected as the spindle speed indicator. Otherwise, the internal revolution clock developed from the back-emf sensing circuit is selected.
3	MENABLE	Driver Enable Control. When set LOW, both upper and lower drivers are turned off to deny power to the motor. This overrides all other output conditions. When set HIGH, drive outputs are activated per the state of the commutation state counter.

Register contents when Written:

BIT	NAME	DESCRIPTION
4	ADVANCE	Each LOW-TO-HIGH transition advances the edge-trigged commutation state counter by one. When set HIGH, the internal clock (derived from the back-emf events) to the commutation state counter is inhibited. When set LOW, normal operation is resumed.
5 6 7	STAT0 STAT1 STAT2	Preset Commutation State. During start-up, the commutation state counter will be preset to the state decoded by these 3 bits per table 2:

TABLE 2:

STAT2	STAT1	STAT0	OUTA	OUTB	OUTC	OUTUPA	OUTUPB	OUTUPC
0	0	0	OFF	ON	OFF	ON	OFF	OFF
0	0	1	OFF	OFF	ON	ON	OFF	OFF
0	1	0	OFF	OFF	ON	OFF	ON	OFF
0	1	1	ON	OFF	OFF	OFF	ON	OFF
1	0	0	ON	OFF	OFF	OFF	OFF	ON
1	0	1	OFF	ON	OFF	OFF	OFF	ON
1	1	0	Normal Operation					
1	1	1	Normal Operation					

SPINDLE CONTROL/STATUS REGISTER (continued)

Register contents when Read:

BIT	NAME	DESCRIPTION
0	LOCK	Active high indicates that the spindle motor is within ±15 counts of the nominal value (5555 counts with the counter clocked at 500 kHz) or ±0.27%. The corresponding interrupt event LOCK INT will be reset whenever this register is read by the µP.
1	OVER	Active high indicates that the spindle speed is faster than the nominal value; active low indicates that the spindle speed is slower than the nominal value.
2	COMMU	Back-emf commutation clock divided by 2. Each state change of COMMU indicates that the commutation state counter has advanced by one. The corresponding interrupt event COMMU INT will be reset whenever this register is read by the µP.
3 4 5 6	PERCHK5 PERCHK4 PERCHK3 PERCHK2	Spindle Speed Check Bits. These bits are used to estimate the spindle speed if it is slower than the nominal value. **P2 P3 P4 P5 SPEED,rps** 0 0 0 0 SPEED ≥65 1 0 0 0 51≤ SPEED ≥65 1 1 0 0 36≤ SPEED ≥51 1 1 1 0 22≤ SPEED ≥36 1 1 1 1 SPEED ≥22
7	Undefined	

7

SERVO CONTROL/STATUS REGISTER

Address: 2 Access: Read/Write Reset: 00
Register contents when Written:

BIT	NAME	DESCRIPTION
0	HENABLE	H-bridge Driver Enable. When set HIGH, H-bridge MOSFET drivers are enabled.
1	SW ON	When set HIGH, the analog switch between the ERRM and SWIN pins is turned on.
2	-	Undefined
3	TIMING	Timing Controller Disable. When set HIGH, the timing signals required to sample/hold embedded servo position bursts are derived from an external timing source via SAMPLEX and ACQX. Otherwise, the internal timing controller is used.
4	DIBURST	When HIGH, only two servo bursts, BURST1 and BURST2 are sampled. Otherwise, four servo burst amplitudes are sampled.
5	LEAD	Write Gate Guard Lead Enable. When set HIGH, the write gate guard is enabled one burst period prior to the sampling of the first position burst field. Otherwise, the write gate guard is enabled essentially at the same time as the sampling of the first position burst field.
6 7	TIM0 TIM1	Burst Field Length Select. These two bits define the time duration of each embedded servo position burst field per table below:

TIM1	TIM0	Burst Duration, μsec
0	0	5
0	1	6
1	0	8
1	1	10

Register contents when Read:

0	-	Undefined
1	-	Undefined
2	BURST	Active HIGH indicates that the embedded servo position bursts are ready.
3	TRKCS	Active HIGH indicates a track crossing, i.e., NQ or $N\overline{Q}$ changes state.
4	COUNT	Active HIGH indicates that the terminal count (000_H) of the track crossing counter is reached.
5	-	Undefined
6	NQ	Active HIGH when N>Q and reset otherwise.
7	$N\overline{Q}$	Active HIGH when N>-Q and reset otherwise.

The corresponding interrupt events TRKCS INT, COUNT INT and BURST INT will be reset when this register is read by the μP. Also, the TRKCS, COUNT and BURST bits in this register are reset after being read.

ADC ADDRESS/DATA REGISTER

Address: 3 Access: Read/Write Reset: Undefined

Description: When Written, the least significant 4 bits of the register define the analog input to the 8-bit A/D converter. After conversion, the 8-bit digital word of the analog input is stored into the register.

Register contents when Written:

BIT	NAME	DESCRIPTION
0 1 2 3	ADC SEL0 ADC SEL1 ADC SEL2 ADC SEC3	A/D Converter Input Select. These 4 bits define the analog input to the A/D converter per table below:
4	X4	X4 Enable. When set HIGH, the analog input to the A/D converter will be multiplied by 4 before converted into a digital value.
5,6,7	-	Undefined

BIT3	BIT2	BIT1	BIT0	ADC INPUT	ADC Vref
0	0	0	0	BURST1	VREF
0	0	0	1	BURST2	VREF
0	0	1	0	BURST3	VREF
0	0	1	1	BURST4	VREF
0	1	0	0	PES1	VREF
0	1	0	1	PES2	VREF
0	1	1	0	PES0	VREF
0	1	1	1	N	NQREF
1	0	0	0	Q	NQREF
1	0	0	1	ERR	VREF
1	0	1	0	SOUT	VREF
1	0	1	1	SENSE	SENSEREF
1	1	0	0	ADCIN	VREF
1	1	0	1	VREF	VREF
1	1	1	0	SUM1	VREF
1	1	1	1	SUM2	VREF

Register contents when Read:

BIT	NAME	DESCRIPTION
0..7	ADC0..7	Digital output of the A/D converter in 2's complement format. ADC7 corresponds to the sign bit.

TRACK COUNT AND HYBRID SERVO CONTROL REGISTER

Address: 4 and 5 Access: Read/Write Reset: 00

Description: In a hybrid servo application, the dedicated servo channel is supported by a 12-bit track crossing counter with a 4-bit hybrid control register. The counter is preset by the µP and counts down by one whenever the head crosses a track boundary. The LSB 8 bits of the counter are defined at register 4 as follows:

BIT	NAME	DESCRIPTION
0..7	TRACK0..7	LSB of the track crossing counter 0..7. When written, these bits preset the track counter. When read, they reflect the counter state.

The MSB 4 bits of the counter along with the hybrid control bits are latched when the LSB 8 bits are read. The hybrid control bits, QUAD0, QUAD1, SELECT Q and CALIB are "write only." They are defined at register 5 as follows:

BIT	NAME	DESCRIPTION
0..3	TRACK8..11	MSB of track crossing counter 8..11. When written, these bits preset the track counter. When read, they reflect the counter state.
4 5	QUAD0 QUAD1	Quadrant Select. These 2 bits select the quadrant per table below: QUAD1 QUAD0 Quadrant Selected 0 0 -Q 0 1 N 1 0 -N 1 1 Q
6	SELECT Q	Quadrant Select Enable. Select quadrant with QUAD0 and QUAD1 when set HIGH.
7	CALIB	Calibration Enable. When set HIGH, the device is in the calibration mode in which analog inputs N and Q are tied to a DC reference level, NQREF; the analog input SERIN is tied to the DC reference level, SEREF.

ERROR DAC DATA REGISTER

Address: 6 Access: Write Reset: 00

BIT	NAME	DESCRIPTION
0..7	DAC0..7	Digital input to the D/A converter in 2's complement format. DAC7 corresponds to the sign bit.

EMBEDDED SERVO GAIN CONTROL REGISTER

Address: 7 Access: Write Reset: 00

<table>
<tr><th>BIT</th><th>NAME</th><th>DESCRIPTION</th></tr>
<tr><td>0</td><td>GAIN0</td><td>Embedded Servo Burst Amplitude Gain Select.</td></tr>
<tr><td>1</td><td>GAIN1</td><td>These two bits define the gain setting for the embedded servo differential amplifier per table below:
GAIN1 GAIN0 Gain, dB
0 0 -6
0 1 -3
1 0 0
1 1 3</td></tr>
<tr><td>2
3
4
5</td><td>GAIN2
GAIN3
GAIN4
GAIN5</td><td>Embedded Servo Burst Amplitude Gain Select.
These four bits define the gain setting for the sample/hold amplifier per table below:
GAIN5 GAIN4 GAIN3 GAIN2 Gain, dB
0 0 0 0 0.0
0 0 0 1 0.2
0 0 1 0 0.4
0 0 1 1 0.6
0 1 0 0 0.8
0 1 0 1 1.0
0 1 1 0 1.2
0 1 1 1 1.4
1 0 0 0 1.6
1 0 0 1 1.8
1 0 1 0 2.0
1 0 1 1 2.2
1 1 0 0 2.4
1 1 0 1 2.6
1 1 1 0 2.8
1 1 1 1 3.0</td></tr>
<tr><td>6</td><td>SYNC SEL</td><td>Sync Input Select. When set HIGH, the frame rate to sample dedicated quadrature position signals N and Q is derived internally from SYSCLK. Otherwise, it is provided externally from the servo demodulator through SYNC and VCO inputs.</td></tr>
<tr><td>7</td><td>TCHE</td><td>Track Clock Hysteresis Enable. When set HIGH, an internal timing hysteresis is added for deriving the TRKCK output.</td></tr>
</table>

TRANSCONDUCTANCE, PRESCALER & MODE CONTROL REGISTER

Address: 8 Access: Write Reset: Bit 4 and 5 only

Bit	Name	Description
0	TEST	Test Mode Enable. When set HIGH, the device is in the test mode where the testing time for the spindle motor speed control function is shortened.
1	SLEEP	Power-down Mode Enable. When set HIGH, the device is in the power-down mode where all analog circuitry is de-biased, the clock is disabled and the output drivers are pulled to logical HIGH.
2 3	TGAIN0 TGAIN1	Transconductance Select. The transconductance gain of spindle motor lower drivers is defined per table below: **TGAIN1 TGAIN0 Gain** 0 0 2 0 1 4 1 0 8 1 1 16
4 5	SCALE0 SCALE1	SYSCLK Prescaler. To accommodate different system clocks which may be used, the prescaler selects a proper divider to generate a fixed clock at 500 kHz per table below: **SCALE1 SCALE0 SYSCLK(MHz) Divider** 0 0 10 20 0 1 8 16 1 0 6 12 1 1 4 8
6 7	MODE0 MODE1	Spindle Mode Control. These two bits define the number of motor poles per table below: **MODE1 MODE0 POLES COMMU/INDEX** 0 0 4 12 0 1 8 24 1 0 12 36 1 1 N/A N/A

EMBEDDED SERVO TIMING WINDOW CONTROL REGISTER

Address: 9 Access: Write Reset: 00

Description: The embedded servo position burst timing controller generates four timing windows. The sample control register matches these timing windows with four SAMPLE/HOLD circuits. The µP writes into the register a control pattern which will provide a necessary sampling to compare the required bursts in a proper polarity and sequence. In this manner, the µP can mix and commutate the bursts so that the position error signal is always in the same direction.

BIT	NAME	DESCRIPTION
0,1	WD SH1	Define timing window for SAMPLE/HOLD 1. Bit 0 is LSB.
2,3	WD SH2	Define timing window for SAMPLE/HOLD 2. Bit 2 is LSB.
4,5	WD SH3	Define timing window for SAMPLE/HOLD 3. Bit 4 is LSB.
6,7	WD SH4	Define timing window for SAMPLE/HOLD 4. Bit 6 is LSB.

The timing window is selected per table below:

MSB	LSB	S/H Timing Window
0	0	Timing window 1
0	1	Timing window 2
1	0	Timing window 3
1	1	Timing window 4

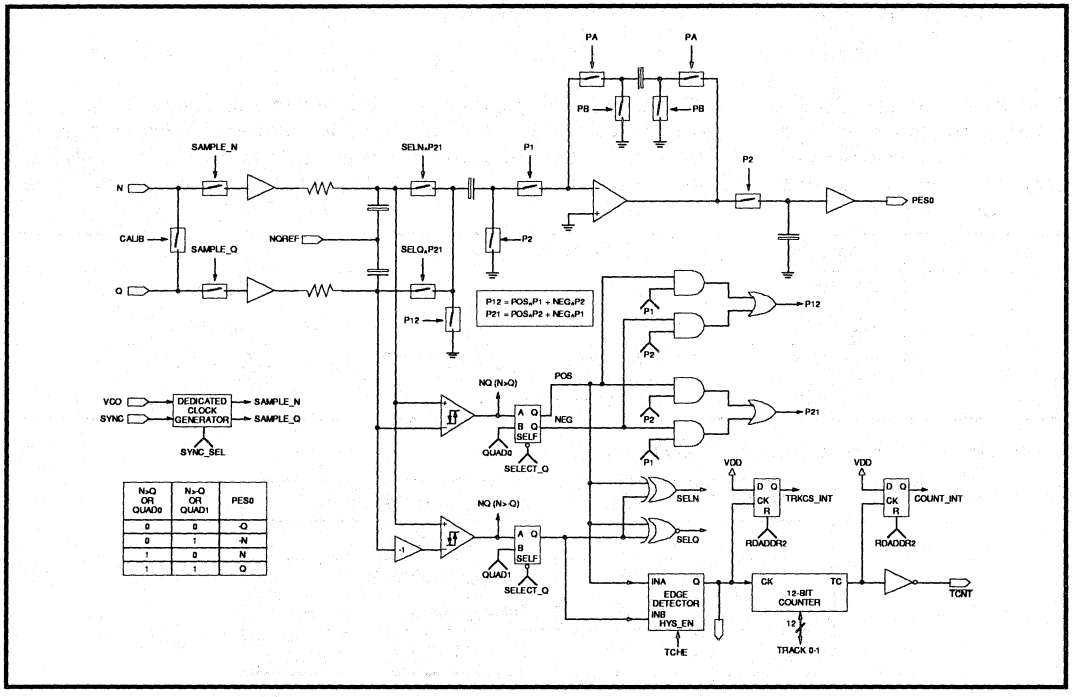

FIGURE 2: Dedicated Servo Position Processor

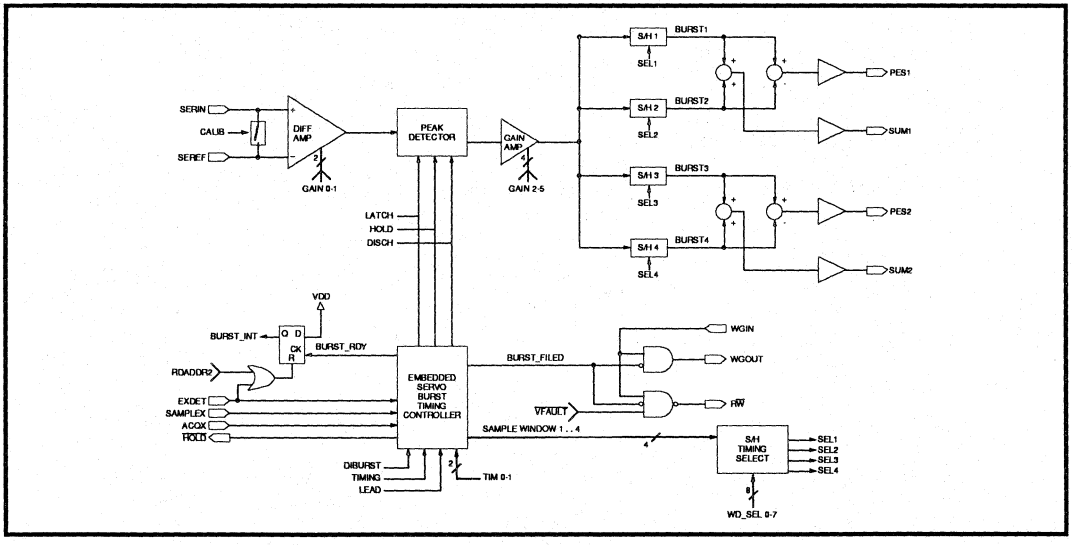

FIGURE 3: Embedded Servo Burst Amplitude Processor & Timing Controller

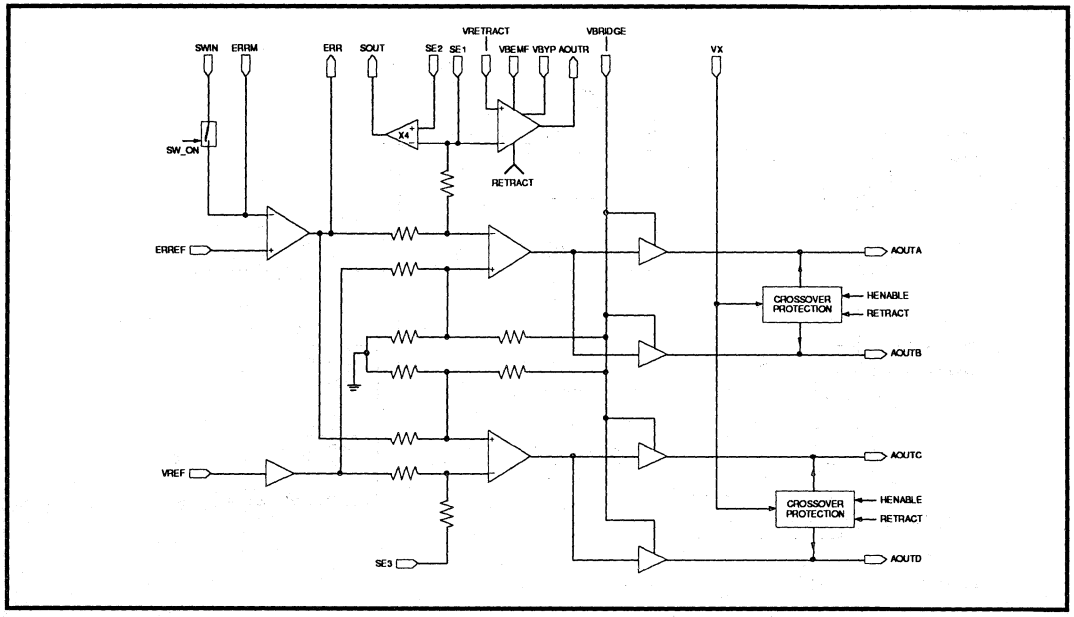

FIGURE 4: Servo Position Error Amplifier

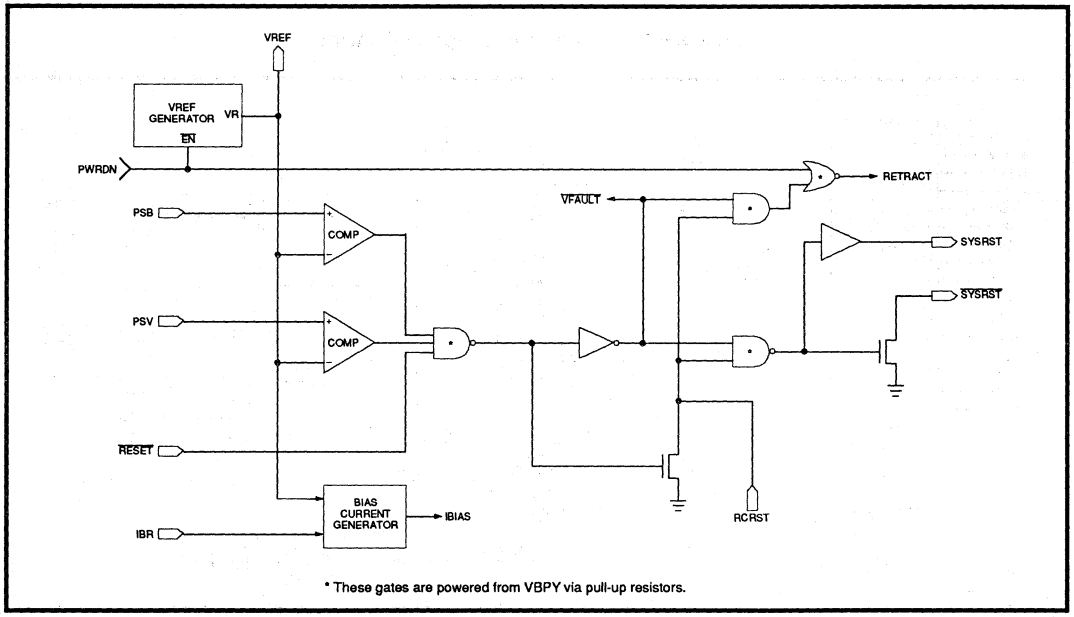

FIGURE 5: Voltage Fault & Servo Head Retract Logic

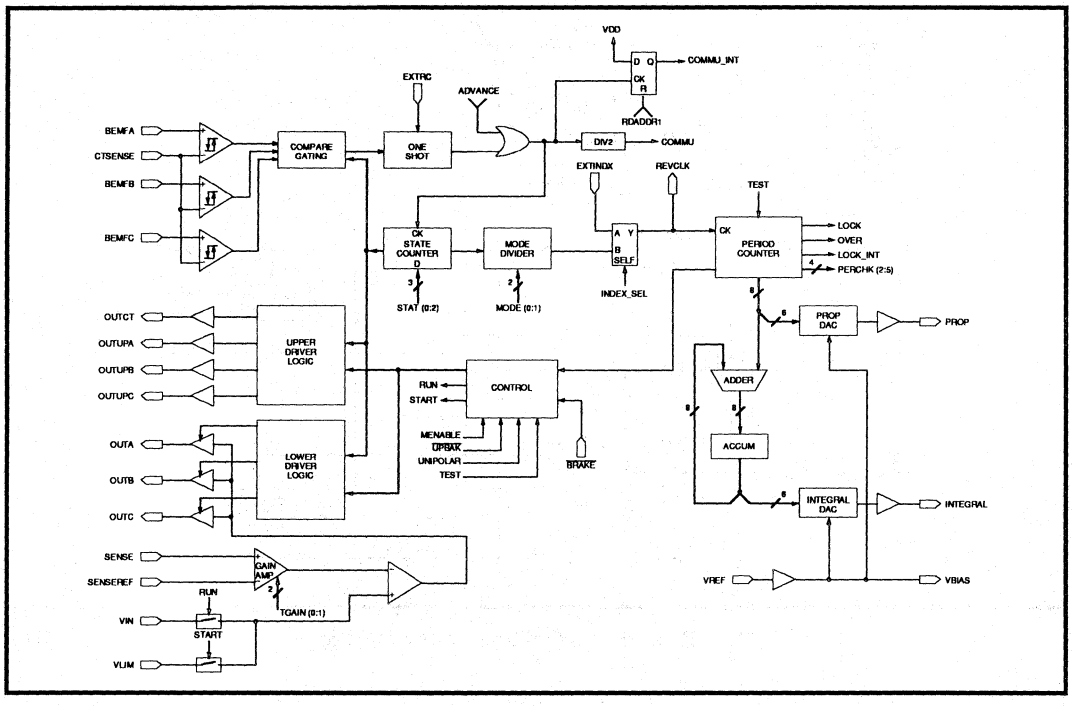

FIGURE 6: Spindle Motor Speed Control

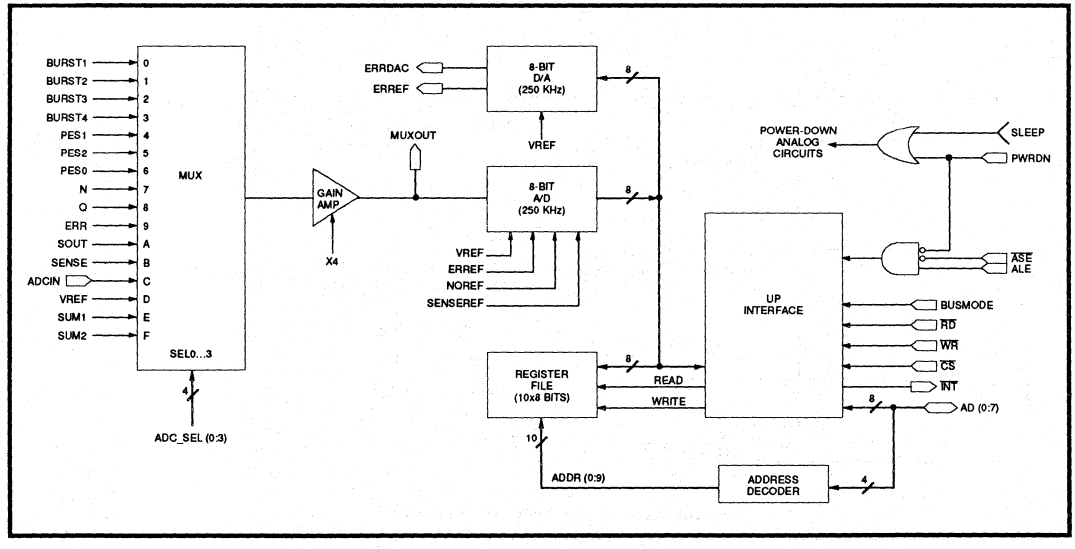

FIGURE 7: Data Acquisition & Microprocessor Bus Interface

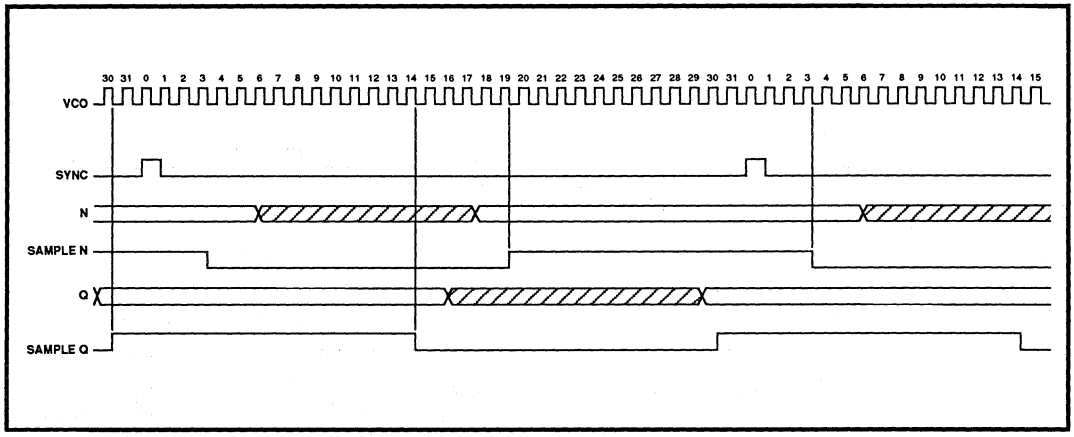

FIGURE 8: Dedicated Servo Timing Diagram

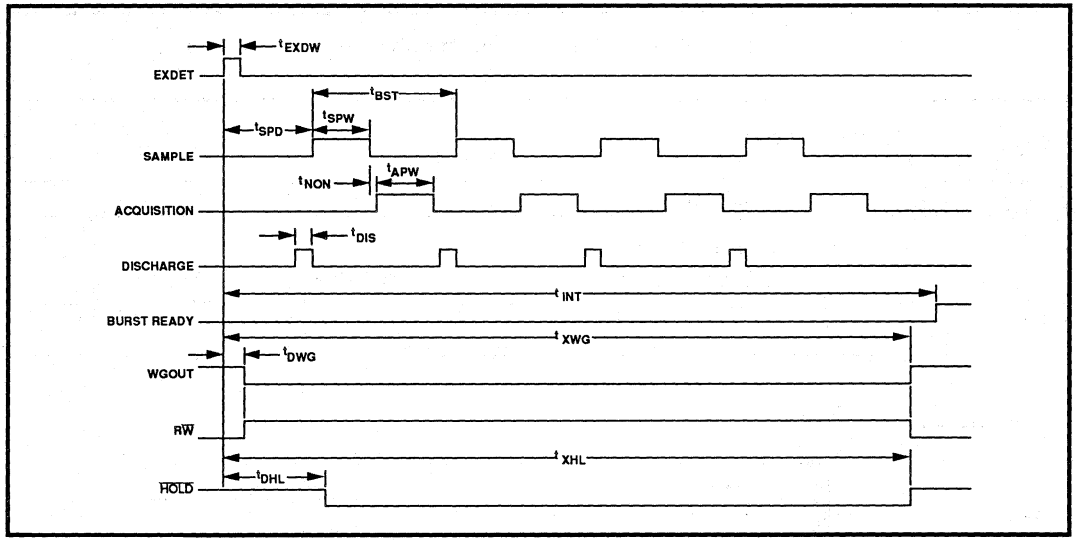

FIGURE 9: Embedded Servo Timing Diagram with Internal Timing Source

7

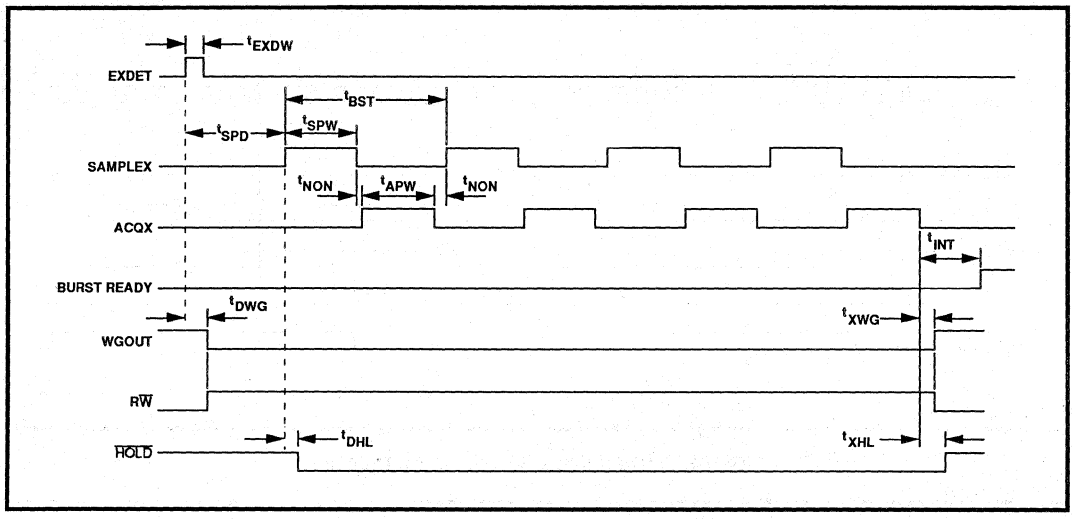

FIGURE 10: Embedded Servo Timing Diagram with External Timing Source

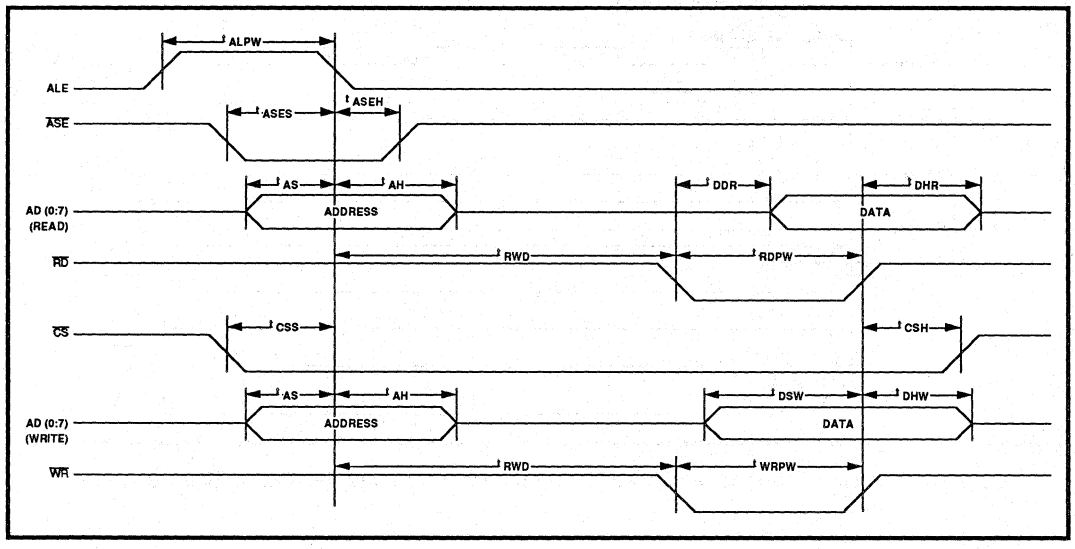

FIGURE 11: Intel Microprocessor Bus Interface Timing Diagram

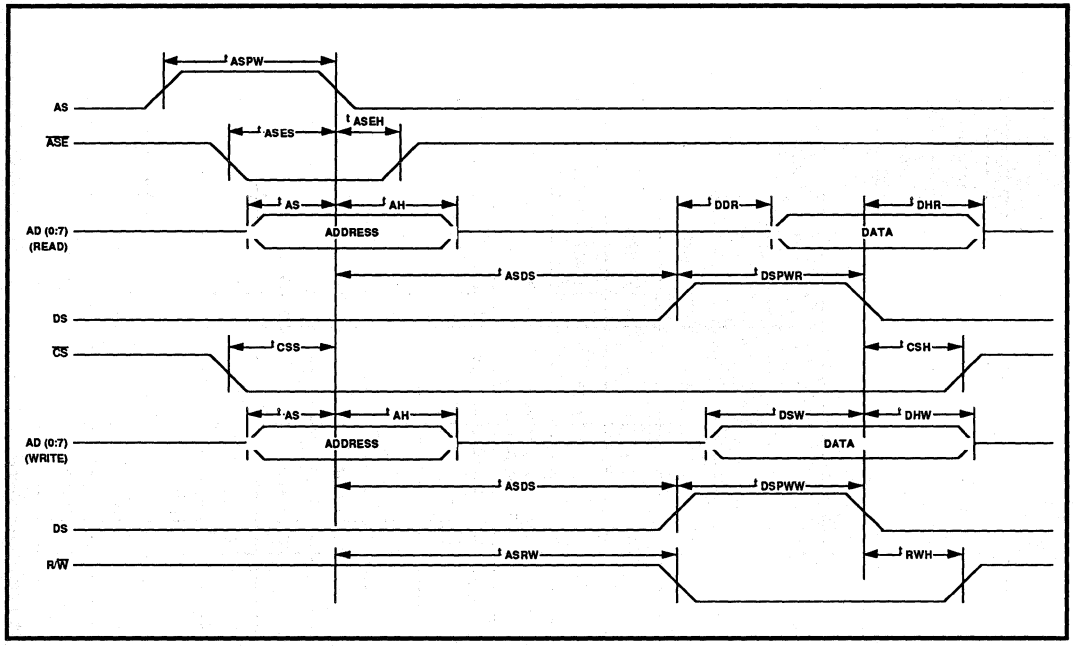

FIGURE 12: Motorola Microprocessor Bus Interface Timing Diagram

7

0: INTERRUPT CONTROL/STATUS			1: SPINDLE CONTROL/STATUS			2: SERVO CONTROL/STATUS			3: ADC CONTROL/STATUS			4:TRACK COUNT LSB		
#	WRITE	READ	#	WRITE	READ	#	WRITE	READ	#	WRITE	READ	#	WRITE	READ
0	COMMU INT	COMMU INT	0	$\overline{\text{UPBRK}}$	LOCK	0	HENABLE		0	ADC SEL0	ADC0	0	TRACK0	TRACK0
1	LOCK INT	LOCK INT	1	UNIPOLAR	OV ER	1	SW ON		1	ADC SEL1	ADC1	1	TRACK1	TRACK1
2	BURST INT	BURST INT	2	INDEX SEL	COMMU	2		BURST	2	ADC SEL2	ADC2	2	TRACK2	TRACK2
3	TRKS INT	TRKS INT	3	MENABLE	PERCHK5	3	TIMING	TRKS	3	ADC SEL3	ADC3	3	TRACK3	TRACK3
4	COUNT INT	COUNT INT	4	ADVANCE	PERCHK4	4	DIBURST	COUNT	4	X4	ADC4	4	TRACK4	TRACK4
5			5	STAT0	PERCHK3	5	LEAD		5		ADC5	5	TRACK5	TRACK5
6			6	STAT1	PERCHK2	6	TIM0	NQ	6		ADC6	6	TRACK6	TRACK6
7	MST INT	MST INT	7	STAT2		7	TIM1	$\overline{\text{NQ}}$	7		ADC7	7	TRACK7	TRACK7

5: TRACK COUNT MSB & HYBRID SERVO CONTROL			6: ERROR DAC DATA			7: EMBEDDED SERVO GAIN CONTROL			8: TRANSCONDUCTANCE PRESCALER & MODE CONTROL			9: EMBEDDED SERVO TIMING WINDOW CONTROL		
#	WRITE	READ	#	WRITE	READ	#	WRITE	READ	#	WRITE	READ	#	WRITE	READ
0	TRACK8	TRACK8	0	DAC0		0	GAIN0		0	TEST		0	WD SEL0	
1	TRACK9	TRACK9	1	DAC1		1	GAIN1		1	SLEEP		1	WD SEL1	
2	TRACK10	TRACK10	2	DAC2		2	GAIN2		2	TGAIN0		2	WD SEL2	
3	TRACK11	TRACK11	3	DAC3		3	GAIN3		3	TGAIN1		3	WD SEL3	
4	QUAD0		4	DAC4		4	GAIN4		4	SCALE0		4	WD SEL4	
5	QUAD1		5	DAC5		5	GAIN5		5	SCALE1		5	WD SEL5	
6	SELECT Q		6	DAC6		6	SYNC SEL		6	MODE0		6	WD SEL6	
7	CALIB		7	DAC7		7	TCHE		7	MODE1		7	WD SEL7	

FIGURE 13: SSI 32H4633 Register Map

PIN DESCRIPTION

This section describes the names of the pins, their symbols, their functions and their active states. The pins are grouped together into function for clarity.

POWER SUPPLIES

NAME	TYPE	DESCRIPTION
VPA, B, C, G	-	Analog +5V supplies. They must be shorted externally.
VPD	-	Digital +5V supply. It must be shorted to analog +5V supplies externally.
VNA, B, C, G	-	Analog grounds. They must be shorted externally.
VND, VND2	-	Digital grounds. They must be shorted to analog grounds externally.

SERVO HEAD POSITION PROCESSOR

N	I	Normal Input - Analog position signal from a dedicated servo demodulator. This input along with quadrature input is used to extract the position information from a dedicated servo surface.
Q	I	Quadrature Input - Analog position signal from a dedicated servo demodulator.
NQREF	I	Dedicated Position Error Reference - DC reference voltage for both normal and quadrature analog inputs.
SYNC	I	Sync Input - A clock signal generated from a dedicated servo demodulator. The falling edge of this clock causes the analog signals N and Q to be sampled.
VCO	I	VCO Input - A clock signal generated from a dedicated servo demodulator. The VCO should be synchronous with N and Q inputs.
TRKCK	O	Track Crossing Clock - This digital output drives external hardware track counter and is compatible with the counter function available in the Intel 8051 family of microcontrollers. It is normally LOW and pulses HIGH once per track crossing.
$\overline{\text{TCNT}}$	O	Terminal Count - The terminal count output is normally HIGH and goes LOW when the 12-bit counter reaches zero.
PES0	O	Position Error Output - Test point for the analog output of the position processor. This signal is proportional to the radial displacement of the head from the center of the current track, based upon the values of bits QUAD0, QUAD1 and SELECT Q.
SERIN	I	Embedded Servo Input - Full-wave rectified analog signal generated from a read data channel. This input is to extract the position information from embedded servo bursts.
SEREF	I	Embedded Servo Burst Reference - A DC reference level for the full-wave rectified analog signal SERIN.
SAMPLEX	I	Servo Burst Sample - This TTL compatible input, when HIGH, activates the peak detector. This input is used only when the TIMING bit in the SERVO CONTROL register is set HIGH for an external timing source.

SERVO HEAD POSITION PROCESSOR (continued)

NAME	TYPE	DESCRIPTION
ACQX	I	Servo Burst Acquisition - This TTL compatible input, when HIGH, activates the transfer of the voltage captured by the peak detector onto holding capacitors. This input is used only when the TIMING bit in the SERVO CONTROL register is set HIGH for an external timing source.
PES1 PES2	O	Position Error Signal - Test point for differential signals which are defined as: PES1 = BURST1-BURST2 PES2 = BURST3-BURST4
SUM1 SUM2	O	Position Sum Signal - Test point for summed signals which are defined as: SUM1 = BURST1+BURST2 SUM2 = BURST3+BURST4

HEAD POSITIONER MOSFET DRIVER AND VOLTAGE FAULT DETECTION

ERRM	I	Actuator Inverting Input - Inverting input to the position error amplifier of the MOSFET predriver.
SWIN	I	This input is shorted to ERRM when the bit SW ON is set HIGH. SWIN floats otherwise.
ERR	O	Acceleration Error - Position error amplifier output. This signal is amplified by the MOSFET drivers and applied to the actuator through an external MOSFET H-bridge as follows: SE3-SE1 = 30 (ERR-VREF)
AOUTA AOUTC	O	PFET Driver - Drive signals for P channel MOSFETs connected between VBRIDGE and the voice coil actuator. Crossover protection circuitry ensures that the P and N channel devices driven by OUTC and OUTD are never enabled simultaneously.
AOUTB AOUTD	O	NFET Driver - Drive signals for N channel MOSFETs connected between the current sense resistor and the voice coil actuator.
VBRIDGE	I	Bridge Voltage Supply - Pin for connection to the voltage supply provided to external power transistors.
VRETRACT	I	Retract Voltage - In head retract mode this voltage is applied across the actuator to force the heads to move at a constant speed.
AOUTR	O	Head Retract Amplifier Output - Voltage output to drive an external head retract circuit.
SE1 SE3	I	Motor Voltage Sense Input - These inputs provide feedback to the internal MOSFET drive amplifier.
SE2	I	Motor Current Sense Input - Non-inverting input to the current sense differential amplifier. It should be connected to an external current sense resistor. The inverting input of the differential amplifier is SE1.
SOUT	O	Motor Current Sense Output - This output provides a voltage proportional to the voltage drop across the external current sense resistor as follows: SOUT-ERREF = 4 (SE2-SE1)

HEAD POSITIONER MOSFET DRIVER AND VOLTAGE FAULT DETECTION (continued)

NAME	TYPE	DESCRIPTION
VX	O	Crossover Protection Voltage - The current source output at VX is converted to a voltage with an external resistor. The value of the resistor should be adjusted so that VX is less than the specified minimum threshold voltage of the MOSFET bridge.
VBYP	I	Bypass Voltage Supply - The VBRIDGE voltage is stored on this node for use during retract.
PSB PSV	I	Fault Voltage Comparator Inputs - Voltage inputs for the low voltage comparators. These two inputs should be connected to separate external resistor dividers. Each resistor divider divides its corresponding supply voltage to a proper value which is comparable with the internal voltage reference at 2.35 volts.
VREF	O	Internal Voltage Reference - A voltage reference at 2.35 volts is generated internally for the DC reference level throughout the device. Due to limited drive capability provided with on-chip voltage reference, this pin shall be used only for connecting an external bypass capacitor of 10 μF.
IBR	O	Bias Current Reference - Pin for connection to an external resistor (from GND) to establish a reference current for bias currents used in analog circuits.
$\overline{\text{RESET}}$	I	Reset Input - When set LOW, all the internal registers are reset and a forced head retraction is activated.
$\overline{\text{SYSRST}}$	O	Reset Output - Active LOW output signal, which is generated by a supply voltage fault or $\overline{\text{RESET}}$ being pulled LOW externally.
SYSRST	O	Reset Output - Active HIGH output signal which is inverted version of $\overline{\text{SYSRST}}$.
RCRST	I	Pin for connection to an external capacitor to extend the active low duration of $\overline{\text{SYSRST}}$.

SPINDLE MOTOR SPEED CONTROL

EXTINDX	I	External Index Input - This TTL compatible input, when selected via the INDEX SEL bit, is used to provide a once-per-revolution indication of angular position and speed to the device. The falling edge of EXTINDX is the reference.
SYSCLK	I	System Clock Input - A TTL compatible input is provided to derive internal timing signals.
EXTRC	I	Pin for connection to a resistor (from VDD) and a capacitor (from GND) to provide the commutation delay. The commutation delay is 0.56 RC. After the commutation delay, the timing block provides a noise rejection interval to reject transients on the motor coils due to commutations. This noise rejection is an additional 0.29 RC. The total time (commutation delay and noise rejection internal) must be less than a commutation cycle time.

SPINDLE MOTOR SPEED CONTROL (continued)

NAME	TYPE	DESCRIPTION
$\overline{\text{BRAKE}}$	I	Spindle Braking Enable - This input, when active LOW, dynamically brakes the spindle motor. A resistor (from $\overline{\text{SYSRST}}$) and a capacitor (from GND) are connected to this pin to provide a delay between the initiation of fault-induced head retraction and motor braking. RC are selected such that 1.2 RC is equal to the maximum time required for head retraction.
VBIAS	O	Buffered Bias Voltage - VBIAS is buffered VREF to be used for VLIM and motor speed setting bias. (In some applications, it is necessary to create an "offset" to the speed control loop to obtain proper speed regulation.)
PROP	O	Proportional Channel D/A Output - The proportional channel output is the least significant 5 bits plus sign of the period measuring counter. The LSB signifies a 2 microsecond period variation.
INTEGRAL	O	Integral Channel D/A Output - The integral channel output is the most significant 6 bits of an 8-bit accumulator. The accumulator adds the least 8 bits of the period measurement counter to the previous value obtained from prior period measurements and accumulations.
VIN	I	Speed Control Voltage Input - The combination of external driver transistors and internal predriver circuits forms a transconductance amplifier which will define the motor current in relation to VIN. In conjunction with the SENSE input and the gain setting for the sense amplifier, the transconductance gain is given by: $g_m=I_m/VIN=1/(R_S \cdot A_V)$ where I_m is the current flowing through the spindle motor coils, R_S the current sense resistor and A_V the transconductance gain defined by TGAIN0 and TGAIN1 bits.
VLIM	I	Current Limit Setting Voltage - The spindle motor current will be limited to a value determined by R_S, VLIM and Av such that Imax=VLIM/($R_S \cdot A_V$). VLIM is used whenever the spindle speed is measured less than 5151 RPM.
SENSE	I	Current Sense Amplifier Noninverting Input - The external driver transistor sources are connected to a current sense resistor R_S to monitor motor current. The device will control the voltage across the sense resistor to match either VIN (during normal operation) and VLIM (during acceleration).
SENSEREF	I	Current Sense Amplifier Reference Input - Pin for a Kelvin connection to the ground side of the sense resistor.
OUTA OUTB OUTC	O	Predriver Outputs - These predriver outputs drive the gates of external power NFETs. They are configured as open-drain outputs with internal 10 KΩ pull-up resistors to VBEMF.
OUTUPA OUTUPB OUTUPC	O	Upper Pull-up Outputs - These predriver outputs drive the gates of external power PFETs. They are configured as open-drain outputs with internal 10 KΩ pull-up resistors to VBEMF.
OUTCT	O	Center Tap Predriver - This output drives an external PFET driver which connects the motor center tap to the positive power supply for unipolar drive applications. OUTCT has the same characteristics as OUTUPA,B,C and is enabled via the UNIPOLAR bit.

SPINDLE MOTOR SPEED CONTROL (continued)

NAME	TYPE	DESCRIPTION
VBEMF	I	Back-emf Voltage - A power diode voltage drop from the motor power supply is defined as VBEMF. The external PFET sources are connected to VBEMF as is this pin. During power failure, this voltage is used to provide power for head retraction and motor braking.
BEMFA BEMFB BEMFC CTSENSE	I	Back-emf Inputs - Inputs to be connected to their respective motor coils and the center tap for sensing generated back-emf voltages. The device uses the back-emf voltages to determine the rotor position and effect commutation.
REVCLK	O	Revolution Clock Output - This output generates a once-per-revolution indication of motor activity derived from back-emf events.

DATA ACQUISITION AND MICROPROCESSOR BUS INTERFACE

ALE	I	Address Latch Enable - Falling edge latches the register address from the AD0..AD7 address/data bus.
$\overline{ASE}$	I	Address Strobe Enable - When set LOW, this input enables ALE input to the device.
$\overline{CS}$	I	Chip Select - Active LOW signal enables the device to respond to µP read or write.
$\overline{WR}$	I	Write Strobe - In Intel µP applications, active LOW signal causes the data on the address/data bus to be written to the addressed register if $\overline{CS}$ is also active.
$\overline{RD}$	I	Read Strobe - In Intel µP applications, active LOW signal causes the contents of the addressed register to be placed on the address/data bus if $\overline{CS}$ is also active.
AD0..AD7	I/O	Address/Data Bus - 8-bit bus which carries register address information and bidirectional data. These pins are in the high impedance state when not used.
BUSMODE	I	Mode Select - When active HIGH, Intel bus interface is selected. Otherwise, Motorola bus interface is selected.
$\overline{INT}$	O	Interrupt Strobe - Active LOW output signals the µP to respond to the device. It is released when all the pending interrupts have been serviced by the µP.
PWRDN	I	Power-down Mode Enable - When set HIGH, the device is in the power-down mode where all analog circuitry is de-biased, the clock is disabled and the output drivers are pulled to logical HIGH.
ERRDAC	O	Error DAC Output - An 8-bit D/A output which converts a digital word from the µP into an analog signal. This signal is fed back to the position error amplifier through external RC components.
ERREF	O	Reference voltage for D/A output ERRDAC.
ADCIN	I	External A/D input.
MUXOUT	O	Test point for the X4 amplifier output which is the input to the A/D converter.

EMBEDDED SERVO TIMING CONTROLLER

NAME	TYPE	DESCRIPTION
EXDET	I	Bit Synchronization Input - The internal servo timing controller is synchronized with this TTL compatible input.
$\overline{HOLD}$	O	AGC Gain Hold - TTL compatible control signal holds the input AGC amplifier gain of a pulse detector, such as 32P4620, when pulled LOW.
WGIN	I	Write Gate Input - TTL compatible input from the storage controller.
WGOUT	O	Write Gate Output - TTL compatible control signal derived from WGIN. This output will be pulled LOW during embedded servo position burst sampling.
$R\overline{W}$	O	Read/Write Control Output - TTL compatible control signal derived from WGIN. This output will be pulled HIGH during embedded servo position burst sampling or when a low voltage fault occurs.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device or affect reliability.

PARAMETER	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNITS
Supply voltage applied at VPA, VPB, VPC, VPD, VPG	VDD		0.1		7.0	V
Signal ground applied at VNA, VNB, VNC, VND, VND2, VNG	GND		0.0		0.0	V
Bridge voltage applied at VBRIDGE	VBRIDGE		0.1		14.0	V
Bypass voltage applied at VBYP	VBYP		0.1		14.0	V
Back-emf voltage applied at VBEMF	VBEMF		0.1		20.0	V
VBEMF current if VBEMF>18V	IBEMF		-		5.0	mA
Digital input voltages	VIND		-0.3		VDD+0.3	V
Analog input voltages	VINA		-0.3		VDD+0.3	V
Storage temperature	Tstg		-65		150	°C
Lead temperature	TI		-		300	°C

OPERATING ENVIRONMENT LIMITATIONS

The recommended operating conditions for the device are indicated in the table below. Performance specifications do not apply where the device is operating outside these limits.

PARAMETER	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
Supply voltage applied at VPA,VPB,VPC,VPD,VPG	VDD		4.75	-	5.25	V
Signal ground applied at VNA,VNB,VNC,VND, VND2,VNG	GND		0.0	-	0.0	V
Bridge voltage applied at VBRIDGE	VBRIDGE		4.75	-	13.2	V
Bypass voltage applied at VBYP	VBRIDGE -VBYP		0.0	-	0.8	V
Back-emf voltage applied at VBEMF	VBRIDGE -VBEMF		-5.0	-	0.8	V
Ambient temperature	TA		0.0	-	70.0	°C
System clock (10 MHz, Max)	Fc		-	-	±0.01	%
Capacitive load on digital outputs	CL		-	-	100	pF
Analog input impedance	Rin		100	-	-	kΩ
	Cin		-	-	20	pF
Load on analog outputs	Rout		10	-	-	kΩ
	Cout		-	-	40	pF
Bias resistor (22.6 kΩ, Typ)	RBIAS		-	-	±1	%

DC CHARACTERISTICS

The following electrical specifications apply to the digital input and output signals over the recommended operating range unless otherwise noted. Positive current is defined as entering the device. Minimum and maximum are based upon the magnitude of the number.

Supply current Normal mode	IDD	VDD=5.25V	-	-	50	mA
Power-down mode	-		-	-	5	mA
Output logic "1" voltage	Voh	Ioh=-0.4 mA VDD=4.75V	2.4	-	-	V
Output logic "0" voltage	Vol	Iol=1.6 mA VDD=4.75V	-	-	0.4	V
Input logic "1" voltage	Vih	VDD=4.75V	2.0	-	-	V
Input logic "0" voltage	Vil	VDD=4.75V	-	-	0.8	V

ELECTRICAL SPECIFICATIONS (continued)

DC CHARACTERISTICS (continued)

PARAMETER	SYMBOL	CONDITIONS	MIN	NOM	MAX	UNIT
Input logic "1" current	Iih	Vih=5.25V VDD=5.25V	-	-	10	µA
Input logic "0" current	Iil	Vil=0.0 VDD=5.25V	-	-	-10	µA
Input capacitance	Cin		-	-	10	pF

FUNCTIONAL CHARACTERISTICS

Dedicated Servo Position Processor

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
N,Q comparator hysteresis		5	-	30	mV
Commutator comparator offset		-	-	±30	mV
N,Q input voltage w.r.t GND		0.5	-	3.7	V
NQREF w.r.t. GND		1.9	-	2.9	V
N,Q input voltage w.r.t NQREF		-	-	±1.1	V
Channel gain from N,Q to PES0		0.96	1.0	1.04	V/V
PES0 offset		-	-	±50	mV
PES0 output corner frequency		60	85	120	kHz

Embedded Servo Burst Amplitude Processor

SERIN w.r.t. GND		2.0	-	VDD	V
SEREF w.r.t. GND		2.0	-	3.0	V
SERIN input voltage swing w.r.t. SEREF	Channel gain=-6 dB	0.0	-	2.0	Vp
	Channel gain=0 dB	0.0	-	1.0	Vp
Servo burst frequency		0.5	-	2.0	MHz
Input impedance at SERIN, SEREF		20	-	-	kΩ
		-	-	10	pF
DC offset at PES1,PES2	BURST1=BURST2=0.5V BURST3=BURST4=0.5V	-30	-	20	mV
DC offset at SUM1,SUM2	BURST1=BURST2=0.5V BURST3=BURST4=0.5V	0	-	-250	mV

Embedded Servo Burst Amplitude Processor (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Differential gain error at PES1,PES2,SUM1,SUM2		-	-	±0.1	dB
Integral gain error at PES1,PES2,SUM1,SUM2		-	-	±1.0	dB
PES1,PES2 output swing w.r.t. VREF		-	-	±1.1	V
SUM1,SUM2 output swing w.r.t. VREF		-	-	1.1	V
Allowable load at PES1, PES2,		10	-	-	kΩ
SUM1,SUM2 to VREF		-	-	40	pF

Embedded Servo Timing

The following timing specifications are applied when the internal servo timing block is selected by pulling the TIMING bit to logical LOW. Timing measurements are defined in Figure 3 and made at 50% VDD with 50 pF load capacitances for all pins, unless otherwise noted.

PARAMETER	SYMBOL	MIN	NOM	MAX	UNIT
Burst cell time	t_{BST}				
TIM0='0' TIM1='0'		-	5.0	-	µs
TIM0='1' TIM1='0'		-	6.0	-	µs
TIM0='0' TIM1='1'		-	8.0	-	µs
TIM0='1' TIM1='1'		-	10.0	-	µs
EXDET pulse width	t_{EXDW}	0.5	-	t_{BST}	µs
Internal first sampling time from EXDET rise	t_{SPD}				
LEAD='0'		1.0	-	1.7	µs
LEAD='1'		(t_{BST}+1.0)	-	(t_{BST}+1.7)	µs
Sampling pulse width	t_{SPW}				
TIM0='0' TIM1='0'		-	2.0	-	µs
TIM0='1' TIM1='0'		-	3.0	-	µs
TIM0='0' TIM1='1'		-	5.0	-	µs
TIM0='1' TIM1='1'		-	7.0	-	µs
Acquisition pulse width	t_{APW}	-	2.0	-	µs
Discharge pulse width	t_{DIS}	-	0.75	-	µs
Nonoverlapping time between sampling & acquisition pulses	t_{NON}	-	0.25	-	µs

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Embedded Servo Timing (continued)

PARAMETER	SYMBOL	MIN	NOM	MAX	UNIT
Burst ready interrupt from EXDET rise	t_{INT}				
DIBURST='0' LEAD='0'		$(4t_{BST}+5.2)$	-	$(4t_{BST}+5.9)$	µs
DIBURST='1' LEAD='0'		$(2t_{BST}+5.2)$	-	$(2t_{BST}+5.9)$	µs
DIBURST='0' LEAD='1'		$(5t_{BST}+5.2)$	-	$(5t_{BST}+5.9)$	µs
DIBURST='1' LEAD='1'		$(3t_{BST}+5.2)$	-	$(3t_{BST}+5.9)$	µs
WGOUT & $\overline{RW}$ delay time from EXDET rise	t_{DWG}	0.0	-	0.1	µs
WGOUT & $\overline{RW}$ hold time from EXDET rise	t_{XWG}				
DIBURST='0' LEAD='0'		$(4t_{BST}+1.0)$	-	$(4t_{BST}+1.7)$	µs
DIBURST='1' LEAD='0'		$(2t_{BST}+1.0)$	-	$(2t_{BST}+1.7)$	µs
DIBURST='0' LEAD='1'		$(5t_{BST}+1.0)$	-	$(5t_{BST}+1.7)$	µs
DIBURST='1' LEAD='1'		$(3t_{BST}+1.0)$	-	$(3t_{BST}+1.7)$	µs
$\overline{HOLD}$ delay time from EXDET rise	t_{DHL}				
LEAD='0'		0.2	-	0.7	µs
LEAD='1'		$(t_{BST}+0.2)$		$(t_{BST}+0.7)$	µs
$\overline{HOLD}$ hold time from EXDET rise	t_{XHL}				
DIBURST='0' LEAD='0'		$(4t_{BST}+1.0)$	-	$(4t_{BST}+1.7)$	µs
DIBURST='1' LEAD='0'		$(2t_{BST}+1.0)$	-	$(2t_{BST}+1.7)$	µs
DIBURST='0' LEAD='1'		$(5t_{BST}+1.0)$	-	$(5t_{BST}+1.7)$	µs
DIBURST='1' LEAD='1'		$(3t_{BST}+1.0)$	-	$(3t_{BST}+1.7)$	µs

The following timing specifications are applied when the internal servo timing block is selected by pulling the TIMING bit to logical HIGH. Timing measurements are defined in Figure 4 and made at 50% VDD with 50 pF load capacitances for all pins, unless otherwise noted.

EXDET pulse width	t_{EXDW}	0.5	-	5.0	µs
SAMPLEX delay time from EXDET rise	t_{SPD}	0.2	-	-	µs
SAMPLEX pulse width	t_{SPW}	3	-	-	µs
ACQX pulse width	t_{APW}	2	-	-	µs
Nonoverlapping time between SAMPLEX & ACQX pulses	t_{NON}	0.0	-	-	µs
Burst ready interrupt from last ACQX fall	t_{INT}	5.2	-	5.9	µs
WGOUT & $\overline{RW}$ delay time from EXDET rise	t_{DWG}	0.0	-	0.1	µs

Embedded Servo Timing (continued)

PARAMETER	SYMBOL	MIN	NOM	MAX	UNIT
WGOUT & R/$\overline{W}$ hold time from last ACQX fall	t_{XWG}	1.0	-	1.7	µs
$\overline{HOLD}$ delay time from first SAMPLEX rise	t_{DHL}	0.2	-	0.7	µs
$\overline{HOLD}$ hold time from last ACQX fall	t_{XHL}	1.0	-	1.7	µs

Head Positioner MOSFET Driver

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VRETRACT voltage	VBEMF = 3V	0.3	-	0.9	V
	VBEMF = 12V	0.4	-	1.2	V
Retract offset					
VBEMF = 3V	VRETRACT = 0.5V	-70	-	50	mV
VBEMF = 6V	VBYP = 4V to 13V	-70	-	70	mV
VBEMF = 12V	I_{AOUTR}<1mA	-150	-	150	mV
Voh at AOUTR	Ioh = -1mA				
VBEMF = 4V VBYP = 4V		1.5	-	-	V
VBEMF = 3V VBYP = 4V		1.3	-	-	V
Leakage current at AOUTR	RETRACT = LOW AOUTR = 0V to 14V	-	-	1	µA
Voh at AOUTA, AOUTC	Ioh = -1 mA	VBRIDGE-1.5	-	-	V
	Ioh = -1 µA	VBRIDGE-0.1	-	-	V
Vol at AOUTA, AOUTC	Iol = 10 µA	-	-	1	V
Voh at AOUTB	Ioh = -10 µA	VBRIDGE-0.5	-	-	V
Voh at AOUTD	Ioh = -10 µA	VBYP-0.5	-	-	V
Vol at AOUTB, AOUTD	Iol = 1 mA	-	-	1	V
	Iol = 10 µA	-	-	0.2	V
Input offset at SOUT		-	-	±3	mV
SOUT/(SE1-SE2)		3.9	-	4.1	V/V
SE1/ERR, SE3/ERR		14.0	-	15.4	V/V
ERRAMP input offset		-	-	±10	mV
ERRAMP gain		1000	-	-	V/V
Output crossover time CL = 600 pF at AOUTA,C CL = 150 pF at AOUTB,D	PFET VTH = -2V NFET VTH = 2V R_X = 50 kΩ	-	-	45	µs
Input impedance at SE1, SE2,SE3		20	-	-	kΩ

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Head Positioner MOSFET Driver (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Output resistance at SOUT		-	-	350	Ω
Analog switch on-resistance at SWIN		-	-	600	Ω
Output resistance at ERR		-	-	100	Ω
Output voltage at VX		1.0	-	1.4	V

Voltage Reference and Voltage Fault Circuit

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VPB voltage for $\overline{SYSRST}$ & RCRST in operation		2.0	-	-	V
On resistance at RCRST					
VPB>3.5V VBYP>4V		-	-	800	Ω
VPB>3.5V VBYP>10V		-	-	550	Ω
RCRST input threshold	VBYP=4V	0.2	-	1.2	V
IBR voltage w.r.t. VREF		-80	-	20	mV
Output voltage at VREF	|II|<10μA	2.27	2.34	2.41	V
PSB,PSV comparator offset		-	-	±15	mV

Spindle Motor Speed Control

SYSCLK duty cycle		40	-	60	%
EXTINDX pulse width		200	-	-	ns
Advance pulse width		3	-	-	μs
Timing resistor at EXTRC		0.01	-	10	MΩ
Timing capacitor at EXTRC		100	-	-	pF
Delay time variation relative to T0*		-	-	±5	%
Vil at $\overline{BRAKE}$	VBEMF = 5V	0	-	0.3	V
Vih at $\overline{BRAKE}$	VBEMF = 5V	1.5	-	-	V
Output voltage swing at PROP & INTEGRAL	I_{out}<0.1mA	0	-	VBIAS±5%	V
DAC step size at PROP & INTEGRAL		32	-	39	mV
Output impedance at PROP & INTEGRAL	0.5V<V_{out}<2.0V I_{out}=0.1mA	-	-	300	Ω

Spindle Motor Speed Control (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Kp,proportional gain**		0.31	-	0.38	V/rad/s
Ki,integral gain		7.00	-	8.55	V/rad
VBIAS output w.r.t. VREF		-50	-	25	mV
Input voltage at VIN & VLIM		0	-	2.35	V
Input leakage current at VIN & VLIM		-	-	±1	µA
Output resistance at OUTUPA,B,C & OUTCT	Output in HIGH state, pulled to VBEMF	5	-	20	kΩ
Vol at OUTUPA,B,C & OUTCT	I_{out}<3mA VBEMF=13.2V	-	-	1.0	V
Output resistance at OUTA,B,C	Output in HIGH state, pulled to VBEMF	5	-	20	kΩ
Vol at OUTA,B,C	I_{out}<5mA	-	-	1.0	V
Input voltage at SENSE	A_V=2	0.0	-	1.0	V
Input voltage at SENSEREF		0.0	-	0.05	V
Input leakage current at SENSE	0.0V<V_{in}<1.0V	-	-	±10	µA
Input leakage current at SENSEREF	0.0V<V_{in}<0.05V	-200	-	10	µA
Input capacitance at SENSE & SENSEREF		-	-	20	pF
Gain variation***	A_V=2,4,8,16	-	-	±10	%
Input impedance at BEMFA,B,C	-0.3V<V_{in}<15V	100 -	- -	- 10	kΩ pF
Input impedance at CTSENSE		30 -	- -	- 10	kΩ pF
LOCK indication range		5384.9	-	5415.1	RPM
Speed resolution		-	-	±0.018	%

*T0 is the commutation delay and is given by the relationship T0 = 0.56RC. Suggested value for C would be 470 to 1000 pF. An external R and C must be provided such that T0 is greater than 10 µs (R=22 kΩ, C=470 pF).

**The motor speed control loop can be described as: $H(s)=K_p+K_i/s$

***The transconductance gain from VIN or VLIM to the steady-state current flowing through the motor is given by $G = 1/(R_{SENSE} \cdot A_V)$

DATA ACQUISITION

A/D Converter

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
ADCIN full-scale	X4=LOW	-	±(VREF/2)	-	V
swing w.r.t. VREF	X4-HIGH	-	±(VREF/8)	-	V
Resolution		-	8	-	Bits
Conversion time*		-	4.0	-	µs
LSB voltage	X4=LOW	-	VREF/256	-	mV
	X4=HIGH	-	VREF/1024	-	mV
Differential linearity error		-	-	±0.75	LSB
Relative accuracy**		-	-	±1.0	LSB
Power supply sensitivity		-	-	±0.5	LSB

*A maximum of 2 µs of latency between a conversion request and the actual start of conversion must be added to this conversion time of 4 µs to calculate the total delay time from a conversion request to the completion of conversion.

**Relative accuracy is the deviation of the analog value at any code (relative to the full analog range of the A/D transfer characteristic) from its theoretical value (relative to the same range), after the full-scale range has been calibrated.

Error D/A Converter

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
ERRDAC full-scale voltage swing w.r.t ERREF		-	±(VREF/2)	-	V
Resolution		-	8	-	Bits
Conversion time*		-	4.0		µs
LSB voltage		-	VREF/256	-	mV
Output voltage at ERREF		1.56	1.61	1.66	V
ERRDAC offset w.r.t. ERREF		-	-	±5	mV
Differential linearity error		-	-	±0.5	LSB
Relative accuracy**		-	-	±1.0	LSB
Power supply sensitivity		-	-	±0.5	LSB

*A maximum of 2 µs of latency between a conversion request and the actual start of conversion must be added to this conversion time of 4 µs to calculate the total delay time from a conversion request to the completion of conversion.

**Relative accuracy is the deviation of the analog value at any code (relative to the full analog range of the D/A transfer characteristic) from its theoretical value (relative to the same range), after the full-scale range has been calibrated.

Intel Microprocessor Interface Timing

The following timing specifications are applied when an Intel bus interface is selected by pulling the BUSMODE pin to logical HIGH. Timing measurements are defined in Figure 5 and made at 50% VDD with 50 pF load capacitances for all pins, unless otherwise noted.

PARAMETER	SYMBOL	MIN	NOM	MAX	UNIT
Pulse width, ALE HIGH	t_{ALPW}	45	-	-	ns
Muxed address valid time to ALE fall	t_{AS}	7.5	-	-	ns
Muxed address hold time from ALE fall	t_{AH}	20	-	-	ns
Read data delay time from $\overline{RD}$ fall	t_{DDR}	-	-	149	ns
Read data hold time from $\overline{RD}$ rise	t_{DHR}	0	-	55	ns
Pulse width, $\overline{RD}$ LOW	t_{RDPW}	200	-	-	ns
Write data set up time to $\overline{WR}$ rise	t_{DSW}	70	-	-	ns
Write data hold time from $\overline{WR}$ rise	t_{DHW}	10	-	-	ns
Pulse width, $\overline{WR}$ LOW	t_{WRPW}	100	-	-	ns
$\overline{RD}$ or $\overline{WR}$ delay time from ALE fall	t_{RWD}	25	-	-	ns
$\overline{CS}$ valid time to ALE fall	t_{CSS}	0	-	-	ns
$\overline{CS}$ hold time from $\overline{RD}$ or $\overline{WR}$ rise	t_{CSH}	0	-	-	ns
$\overline{ASE}$ valid time to ALE fall	t_{ASES}	45	-	-	ns
$\overline{ASE}$ hold time from ALE fall	t_{ASEH}	0	-	-	ns

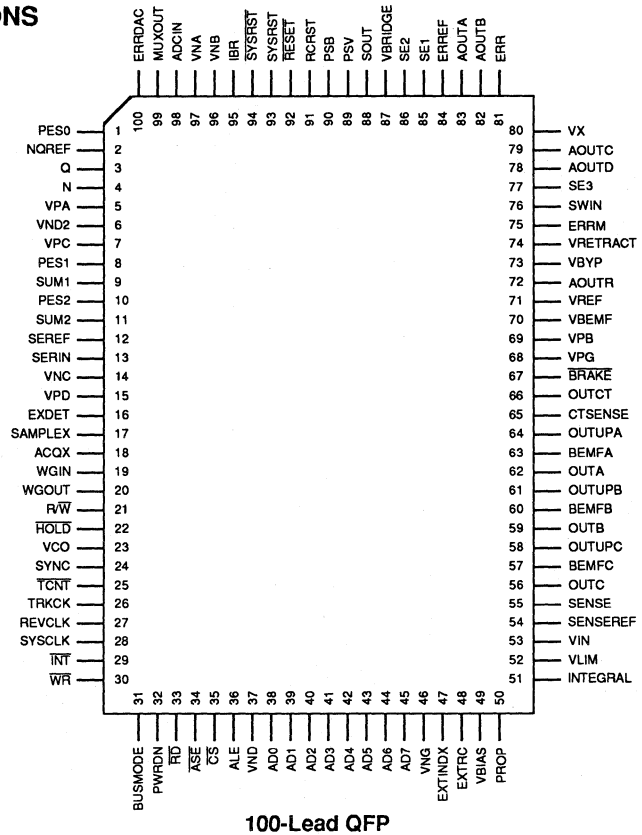
Motorola Microprocessor Interface Timing

The following timing specifications are applied when a Motorola bus interface is selected by pulling the BUSMODE pin to logical LOW. Timing measurements are defined in Figure 6 and made at 50% VDD with 50 pF load capacitances for all pins, unless otherwise noted.

PARAMETER	SYMBOL	MIN	NOM	MAX	UNIT
Pulse width, AS HIGH	t_{ASPW}	45	-	-	ns
Muxed address valid time to AS fall	t_{AS}	10	-	-	ns
Muxed address hold time from AS fall	t_{AH}	20	-	-	ns
Read data delay time from DS rise	t_{DDR}	-	-	180	ns
Read data hold time from DS fall	t_{DHR}	0	-	80	ns
Pulse width, DS HIGH during READ	t_{DSPWR}	200	-	-	ns
Write data setup time to DS fall	t_{DSW}	70	-	-	ns
Write data hold time from DS fall	t_{DHW}	10	-	-	ns
Pulse width, DS HIGH during WRITE	t_{DSPWW}	100	-	-	ns
DS delay time from AS fall	t_{ASDS}	25	-	-	ns
R/$\overline{W}$ delay time from AS fall during WRITE	t_{ASRW}	25	-	-	ns
R/$\overline{W}$ hold time from DS fall during WRITE	t_{RWH}	0	-	-	ns
$\overline{CS}$ valid time to AS fall	t_{CSS}	0	-	-	ns
$\overline{CS}$ hold time from DS fall	t_{CSH}	0	-	-	ns
$\overline{ASE}$ valid time to AS fall	t_{ASES}	45	-	-	ns
$\overline{ASE}$ hold time from AS fall	t_{ASEH}	0	-	-	ns

PACKAGE PIN DESIGNATIONS

(Top View)



100-Lead QFP

CAUTION: Use handling procedures necessary for a static sensitive component.

7

ORDERING INFORMATION

PART DESCRIPTION	ORDER NUMBER	PACKAGE MARK
SSI 32H4633 100-Lead QFP	32H4633-CG	32H4633-CG

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680 (714) 573-6000, FAX (714) 573-6914

Notes:

silicon systems®
A TDK Group Company

SSI 32H6110
Differential Amplifier

December 1992

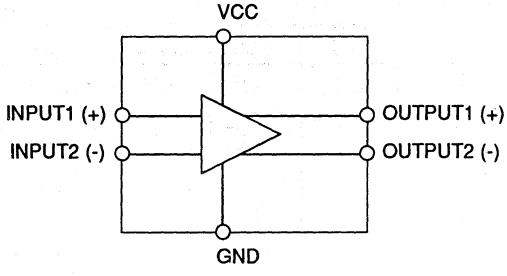
DESCRIPTION

The SSI 32H6110 is a high performance, differential amplifier used as a preamplifier for the magnetic servo thin-film head in Winchester disk drives. The SSI 32H6110 is offered in an 8-pin SON package.

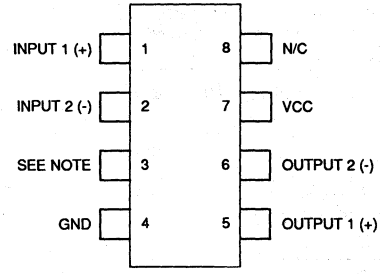
FEATURES

- **High gain (Av=300)**
- **Low noise, 0.85 nV/$\sqrt{Hz}$ maximum**
- **Operates with a +5V power supply**

BLOCK DIAGRAM



PIN DIAGRAM



8-Pin SON

7

CAUTION: Use handling procedures necessary for a static sensitive component.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS – operating above maximum ratings may damage the device

PARAMETER	RATING	UNIT
Power Supply Voltage (VCC)	7	V
Differential Input Voltage	±1	V
Storage Temperature Range	-65 to 150	°C
Operating Ambient Temperature, Ta	10 to 100	°C
Operating Junction Temperature, Tj	10 to 135	°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Supply Voltage (VCC)		4.50	5.0	5.50	V
Input Signal (Vin)			1.0		mVpp
Ambient Temperature		0		+100	°C
Operating Junction Temperature		0		+135	°C

ELECTRICAL CHARACTERISTICS
Unless otherwise specified, recommended operating conditions apply.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Gain (Differential)	R_L = 120Ω	Vin = 1mVpp, R_L = 120Ω Ta = 25°C, f = 1 MHz	225	300	375	mV/mV
	R_L = 100Ω	Vin = 1mVpp, R_L = 100Ω Ta = 25°C, f = 1 MHz	200	250	300	mV/mV
Bandwidth (3 dB)		Vin = 1mVpp, C_L = 15 pF R_L = 120Ω	10	30		MHz
Gain Sensitivity (Supply)		Ta = 25°C			4.0	%/V
Gain Sensitivity (Temp.)		15°C < Ta < 55°C			–0.16	%/°C
Input Noise Voltage		Input Referred, Rs = 0		0.6	0.85	nV/$\sqrt{Hz}$
Input Capacitance (Differential)		Vin = 1 mVpp, f = 5 MHz			35	pF
Input Resistance (Differential)				200		Ω
Common Mode Rejection Ratio (Input Referred)		Vin = 100 mVpp, f = 1 MHz	60			dB
Power Supply Rejection Ratio (Input Referred)		Vin = 100 mVpp, f = 1 MHz	54			dB

ELECTRICAL CHARACTERISTICS, (Continued)
Unless otherwise specified, recommended operating conditions apply.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Input Dynamic Range (Differential)	AC input voltage where gain falls to 90% of its small signal value, f = 5MHz, R_L = 120Ω	5.0			mVpp
Output Offset Voltage (Differential)	Inputs shorted	-400	±50	+400	mV
Output Voltage (Common Mode)	Inputs shorted together and Outputs shorted, R_L = 120Ω	VCC-0.56	VCC-0.88	VCC-1.2	V
Single Ended Output Capacitance				10	pF
Power Supply Current	VCC = 5V		23	34	mA
Input DC Voltage	Common Mode		2.0		V

APPLICATION INFORMATION

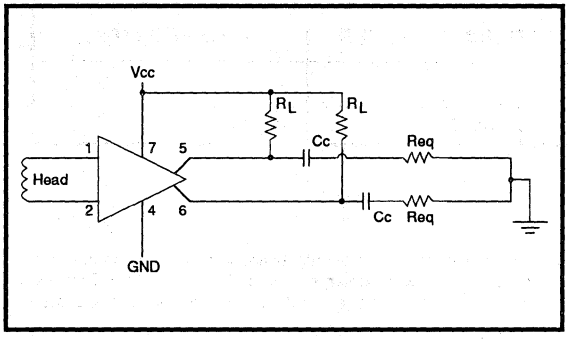


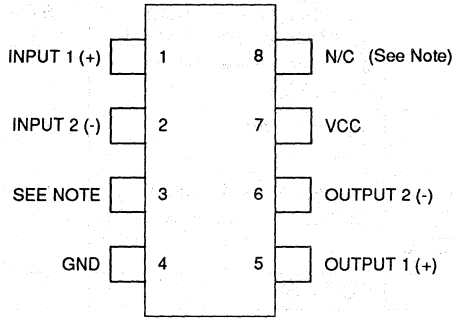
FIGURE 1: Connection Diagram

RECOMMENDED LOAD CONDITIONS

1. Input is directly coupled to the head.
2. Cc's are AC coupling capacitors.
3. RL's are DC bias and termination resistors, 120Ω recommended.
4. REQ. represents equivalent load resistance.
5. Ceramic capacitors (0.1 µF) are recommended for good power supply noise filtering.

SSI 32H6110
Differential Amplifier

PACKAGE PIN DESIGNATIONS
(Top View)



8-Pin SON

NOTE : N/C pin must be left open and not connected to any circuit etch.

ORDERING INFORMATION

PART DESCRIPTION	ORDERING NUMBER	PACKAGE MARK
SSI 32H6110 Differential Amplifier		
8-Pin SON	32H6110-CN	H6110

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914

silicon systems®
A TDK Group Company

SSI 32H6210
Servo Demodulator

Preliminary Data

February 1992

DESCRIPTION

The SSI 32H6210 Servo Demodulator is a bipolar device intended for use in Winchester disk drives with dedicated surface head positioning systems. It processes a di-bit quadrature pattern read from the servo surface by a preamplifier, such as the SSI 32H101 or SSI 32H116, and generates normal and quadrature (N and Q) position reference signals. These signals provide the servo controller with position error feedback. A complete position control system can be realized with the SSI 32H6210 and its companion devices, the SSI 32H6220 Servo Controller and SSI 32H6230 Servo Motor Driver.

The SSI 32H6210 incorporates an input amplifier with automatic gain control and offset cancellation, a phase locked loop and sync separator to recover timing information, and pulse area detectors to recover the position information. External components are used to set the operating characteristics of the SSI 32H6210, such as AGC response, VCO center frequency, PLL response and sync separator threshold. Its high performance analog/digital circuitry is capable of supporting servo frame rates of up to 400 kHz.

FEATURES

- **Servo signal demodulation for dedicated surface head positioning systems**
- **Supports industry standard di-bit quadrature servo pattern with frame rates up to 400 kHz**
- **N, Q outputs convey track crossing and position error information**
- **PLL for timing recovery and synchronization**
- **Adjustable sync separator threshold**
- **Auto-zeroing AGC input amplifier**
- **AGC reference level adjustment**
- **Precision bandgap voltage reference output**
- **Advanced bipolar process dissipates less than 900 mW (5V, 12V)**
- **Available in 28-pin PLCC, DIP, SO packages**

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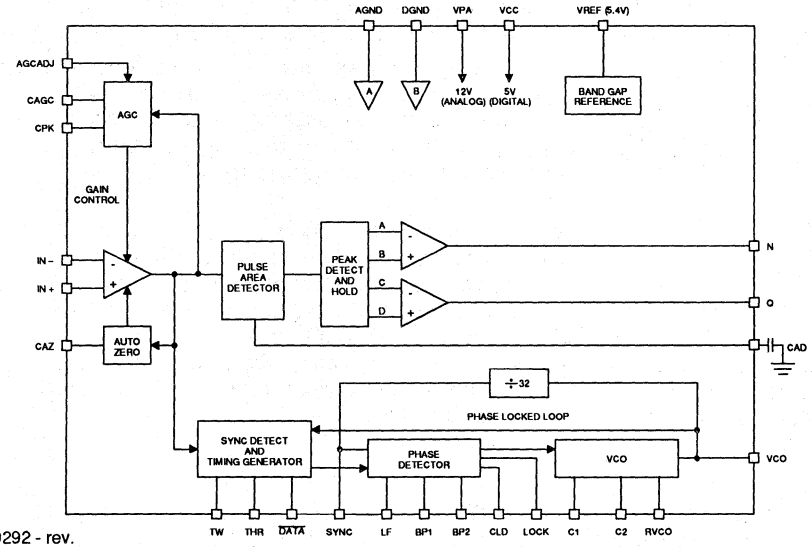
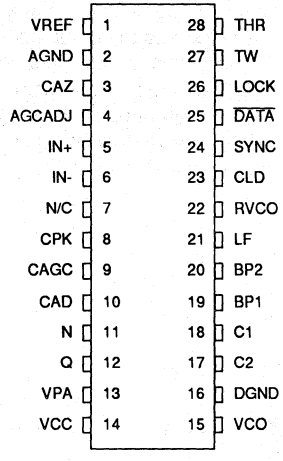
BLOCK DIAGRAM



PIN DIAGRAM



28-PIN DIP, SO

FUNCTIONAL DESCRIPTION

(Refer to block diagram, and typical application, Fig.2)

The SSI 32H6210 processes servo position information which is read from a dedicated surface by a pre-amplifier. The servo information must conform to the 'di-bit quadrature' pattern which is illustrated in Figure 4. Servo frames, consisting of data and sync pulses followed by four information pulses (A, B, C, D) are prerecorded along each track of the servo surface. All the servo frames on an individual track are identical, but in the radial direction four different frame types are encountered, with every fourth track being identical. The N signal generated by the SSI 32H6210 is proportional to the difference in sizes of pulses A and B, while the Q signal is proportional to the difference between pulses C and D. When the read head is off track, the read signal is effectively a linear interpolation between the prerecorded information of two adjacent tracks, making it possible to sense the head displacement exactly.

The SSI 32H6210 has a differential input amplifier which incorporates offset voltage cancellation and automatic gain control. An external read preamplifier must provide a differential input signal of 23 to 400 mV peak to peak from the servo read head. This signal is applied to a pulse detector whose output is proportional to the area under the input pulse.

An AGC circuit adjusts the input gain so that the maximum pulse detector output is 2V peak. The AGC circuit incorporates a peak detector which stores the maximum pulse area signal on the external capacitor C_{PK}. This signal is compared to an internal amplitude reference and the input amplifier gain is adjusted until they are equal. The capacitor C_{AGC} determines the response time of the gain control circuit. An offset cancellation circuit , whose response is set with the external capacitor C_{AZ}, ensures that the average level at the differential amplifier output is zero.

An AGC adjust (AGCADJ) pin allows the user to adjust the AGC reference level. AGCADJ can be driven with a potentiometer or a D/A (a simple Pulse Width Modulated signal is usually sufficient.) This pin is left open if no AGC adjustment is required.

All internal analog signals are referenced to a 5.4V bandgap reference voltage. This level is available at the VREF output, which is capable of supplying 10 mA to the rest of the servo path electronics.

In a standard servo frame, the data and sync pulses are more closely spaced than the information pulses (A-D). This allows the sync detect circuit to recover the SYNC pulses. A threshold, which is defined as percentage of the peak signal at the output of the AGC amplifier, is set externally with R_{TH}. Pulses which exceed this threshold are defined as valid pulses. As illustrated in Figure 6, at the end of the positive going half of a valid pulse, a window, whose width is set by Rw and Cw, is opened. If a second valid pulse occurs within this window, it is recognized as a SYNC pulse. This pulse becomes the input signal to a phase locked loop whose VCO clock frequency is 32 times the SYNC frequency (servo frame rate). The $\overline{DATA}$ output rises after a missing data pulse. The example illustrated in Figure 6 includes the case of a missing DATA pulse. The SYNC clock output, which marks the start of a new servo frame, is derived from the VCO output so that the clock continues to run when a data pulse is missing. Absolute positioning information such as track 0 and guardband flags may be encoded on the servo surface by the omission of data pulses.

To generate the servo pattern shown in the timing diagram, Figure 5, the DATA and SYNC pulses must be written to overlap as shown in Figure 7.

The phase detector compares the detected sync pulses with the SYNC output. A current pulse proportional to the phase error is applied to an external loop filter network connected to the LF pin, to generate the VCO control voltage. If improved power supply rejection is required, bypassing may be provided at pins BP1 and BP2. The VCO center frequency is determined by the external components R_{VCO} and C_{VCO}.

A lock detect circuit measures the phase difference between the detected sync pulses and the sync output. When this difference exceeds half of a VCO clock cycle, a pulse of discharge current is applied to CLD. Otherwise a pulse of charging current is applied to CLD.

A clamp circuit limits the swing of the CLD pin and also insures that a small amount of hysteresis is present. When the voltage on CLD falls below the upper clamp level by more than the "lock margin," the open collector LOCK output transistor is turned on. Likewise, when the voltage on CLD rises above the lower clamp level by more than the "unlock margin," the LOCK output transistor is turned off.

FUNCTIONAL DESCRIPTION (Continued)

Internal timing windows are generated from the recovered SYNC pulse and VCO clock. These windows, WA, WB, WC, and WD, in Figure 5, enable the four peak detectors to capture the A, B, C and D information pulses. The N and Q analog outputs are formed by differencing adjacent pulses. These outputs change during a servo frame and only become valid after the D pulse has been detected. N and Q should be sampled by the servo controller on the next falling edge of the SYNC output clock.

An example of an entire servo path implemented with the SSI 32H6210 and its companion devices, the SSI 32H6220 and SSI 32H6230, is shown in Figure 9.

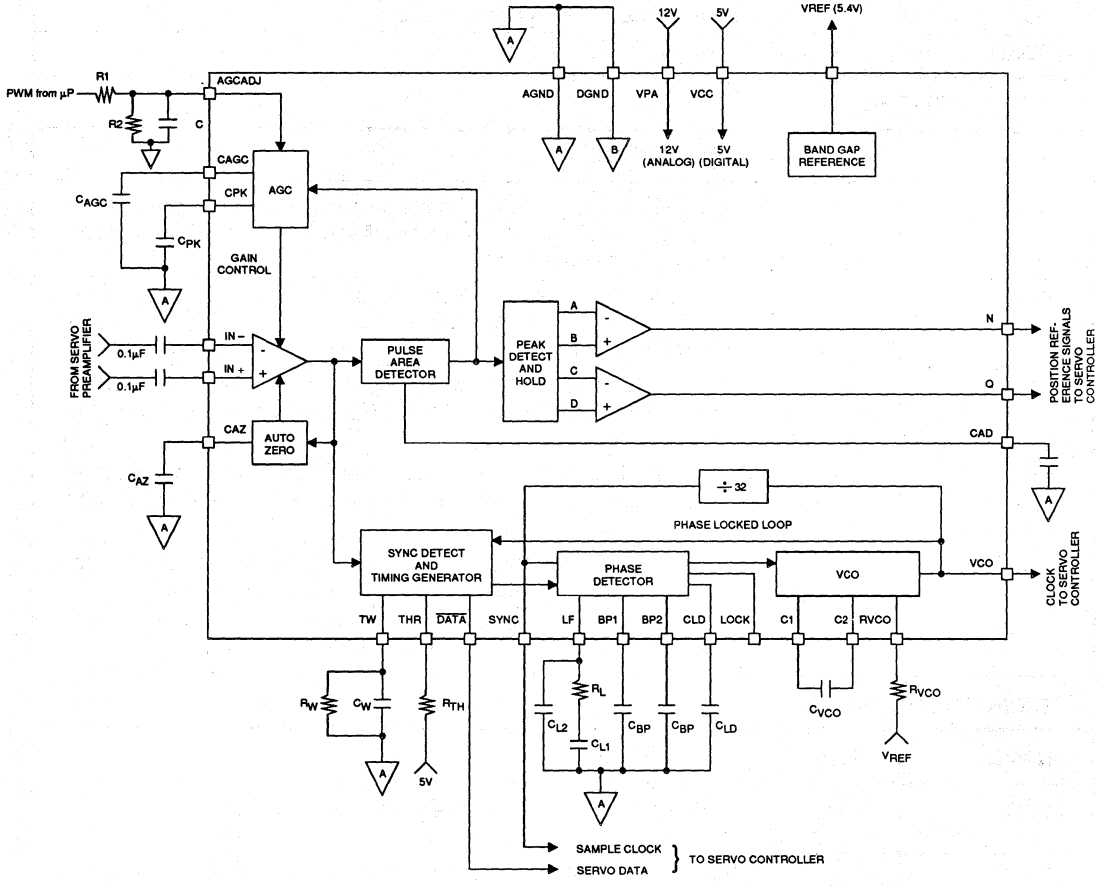


FIGURE 2: Typical Application

PIN DESCRIPTION

POWER

NAME	TYPE	DESCRIPTION
VREF	O	REFERENCE VOLTAGE - 5.4V output. All analog signals are referenced to this voltage.
AGND	-	ANALOG GROUND
VPA	-	ANALOG SUPPLY - 12V power supply.
VCC	-	DIGITAL SUPPLY - 5V power supply.
DGND	-	DIGITAL GROUND

INPUT AMPLIFIER

NAME	TYPE	DESCRIPTION
CAZ	-	AUTOZERO CAPACITOR - A capacitor which sets the response of the input amplifier offset cancellation circuit should be connected between this pin and analog ground.
IN +	I	NON-INVERTING INPUT - AGC input amplifier connection. The non-inverting output of the differential servo pre-amplifier should be AC coupled to this pin.
IN -	I	INVERTING INPUT - AGC input amplifier connection. The inverting output of the differential servo pre-amplifier should be AC coupled to this pin.
CPK	-	PEAK HOLD CAPACITOR - A capacitor which is used by the peak detector of the AGC circuitry must be connected between this pin and analog ground.
CAGC	-	AGC CAPACITOR - A capacitor which sets the AGC attack and decay times must be connected between this pin and analog ground.
AGCADJ	I	AGC Adjust - This pin allows for AGC reference level adjustment. It is driven by a potentiometer or D/A. Normally this pin is left open.

TIMING RECOVERY

NAME	TYPE	DESCRIPTION
VCO	O	VCO OUTPUT - TTL compatible digital clock which is 32 times the sync frequency (servo frame rate).
C2,C1	-	VCO CAPACITOR - Connection points for a capacitor which sets the VCO center frequency in conjunction with an external resistor connected to RVCO.
BP1,BP2	-	PLL BYPASS - Bypass capacitors may be connected between these pins and analog ground to provide additional power supply rejection in the phase locked loop.

TIMING RECOVERY (Continued)

NAME	TYPE	DESCRIPTION
LF	-	PHASE LOCKED LOOP FILTER - An external RC network which sets the PLL loop characteristics must be connected between this pin and analog ground.
RVCO	-	VCO RESISTOR - Connection for a resistor which sets the VCO center frequency, in conjunction with the capacitor between pins C1 and C2. The resistor must be connected between this pin and the VREF output.
SYNC	O	SYNC OUTPUT - TTL compatible digital clock whose falling edge indicates the presence of valid analog signals on the N and Q outputs. There is one SYNC cycle per servo frame.
$\overline{\text{DATA}}$	O	DATA OUTPUT - Active low TTL compatible digital output that indicates the presence of a data pulse in the servo frame. This signal is updated on the falling edge of the SYNC output.
TW	-	TIMING WINDOW - A resistor and capacitor must be connected in parallel between this pin and analog ground to set a timing window which is used in detecting SYNC pulses.
THR	-	PULSE THRESHOLD - A resistor which sets a threshold for SYNC and $\overline{\text{DATA}}$ pulse detection must be connected between this pin and VCC (digital 5V supply).
CLD	-	LOCK DETECT CAPACITOR - The value of this capacitor determines how quickly the LOCK output responds (1000 pF).
LOCK	O	LOCK OUTPUT - An open collector output that indicates the lock status of the PLL.

POSITION INFORMATION

NAME	TYPE	DESCRIPTION
CAD	-	AREA DETECTOR CAPACITOR - A capacitor, which forms an integrator to sense the pulse area of the servo position signals, must be connected between this point and analog ground.
N	O	N OUTPUT - This sampled analog signal is the normal position reference output. N is referenced to VREF and is periodic in radial displacement, with a period of 4 tracks.
Q	O	Q OUTPUT - This sampled analog signal is the quadrature position reference output. Q is referenced to VREF and is periodic in radial displacement, with a period of 4 tracks. It is 90 degrees out of phase with N.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

(Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC operating characteristics.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VCC voltage		0		8	V
VPA voltage		0		16	V
Voltage on PLL inputs		-0.5		VCC+0.5	V
Voltage on other inputs		0		14	V
Storage Temp.		-45		160	°C
Solder Temp.	10 sec. duration			260	°C

RECOMMENDED OPERATION CONDITIONS (Unless otherwise noted, the following conditions are valid throughout this document.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VPA, analog supply		10.8	12	13.2	V
Supply noise	F<1 MHz			0.1	Vpp
VCC, digital supply		4.75	5	5.25	V
Ta, ambient temperature		0		70	°C
VCO operating range				12.8	MHz
Load resistance	To VREF	10			kΩ
Load capacitance				50	pF

DC CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
IPA, VPA current				50	mA
ICC, VCC current				60	mA
VOH, digital output high	|IOH|<40 µA	2.4			V
VOL, digital output low	|IOL|<1.6 mA			0.5	V
IREF, VREF output current capacity		10			mA
VREF output voltage	|IREF|<10 mA	5.1	5.4	5.7	V

ELECTRICAL SPECIFICATIONS (Continued)

AC CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VREF output impedance	IOUT = 0-10 mA 1 µF bypass to AGND Frequency<15MHz			12	Ω
N, Q outputs					
Output impedance	F = 1 MHz			100	Ω
Voltage per track	Referenced to VREF 23-400 mVpp differential AGCADJ open	1.8	2	2.2	V
Offset voltage				20	mV
Output noise	10 Hz<F<1 kHz		-55		dBV
Input amplifier					
Input resistance		5			kΩ
Input resistance mismatch				1	%
Input capacitance				20	pF
PSRR	F<0.5MHz	35			dB
AGC headroom		2			dB
AGC bandwidth	Open loop unity gain C_{AGC}=0.04 µF C_{PK}=1500 pF	5		15	kHz
Autozero pole	C_{AZ} in µF		220/C_{AZ}		Hz
AGCADJ					
Open circuit voltage		0.7	0.76	0.82	V
Gain		-1.6	-1.4	-1.2	V/V
Volts per track adj range		1.0		2.6	V
Input impedance, R_{AGC}	Ta = 25°C	4	5.5	7	kΩ
	Temp. coefficient		2600		ppm/°C
SYNC detector					
Timing window	Rw in Ω, Cw in pF	$0.4(R_W \cdot C_W) + 43 \cdot 10^{-9}$			s
Valid pulse threshold	R_{TH} in kΩ (% of full scale)		0.37/R_{TH}		%

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ELECTRICAL SPECIFICATIONS (Continued)

AC CHARACTERISTICS (Continued)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
LOCK Detector					
CLD up current	RVCO = 11K ± 1%	0.7		3	µA
CLD down current	RVCO = 11K ± 1%	3		10	µA
CLD lock margin		0.5		1.3	V
CLD unlock margin		0.5		1.3	V
CLD hysteresis		75		400	mV
Phase locked loop					
Capture range	Centered on selected fNOM	±5			%
VCO phase shift	Missing DATA pulse			0.005	rad/frame
VCO phase delay	Relative to sync pulse zero crossing			70	ns
VCO gain	fvco in Hz		10.47 fvco		rad/s/V
Phase detector gain			32		uA/rad

TIMING CHARACTERISTICS

(Digital output load capacitance Cl<15 pF, VCO frequency fvco <12.8 MHz, timing measurements for digital signals are measured at 1.3V, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
TDD, data delay				30	ns
TW, sync pulse width		40			ns
TSKW, SYNC to VCO skew		0		40	ns
SYNC fall time				20	ns
TADS, N or Q output settling time				260	ns
TADH, N or Q output hold time		0			ns

APPLICATIONS INFORMATION

A typical SSI 32H6210 application is shown in Figure 2. The selection criteria for the external components shown are discussed below.

INPUT AMPLIFIER

The autozero circuit is effectively a high pass filter, whose pole frequency is given by:

$$f_{AZ} = \frac{220}{C_{AZ}(\mu F)} Hz$$

With a value of 10 µF for C_{AZ}, the autozero circuit's corner frequency will be 22 Hz. This is sufficient for DC offset rejection and it will not interfere with the servo signal.

The AGC response may be characterized in terms of the open loop unity gain bandwidth of its control loop. The nominal value for this loop is set by C_{AGC} as follows:

$$f_{BW} = \frac{390}{C_{AGC}(\mu F)} Hz$$

For a nominal bandwidth of 10 kHz, C_{AGC} should be 0.039 µF. With a 1% capacitor, the variation in actual bandwidth will be +/- 50% due to the tolerance of internal components. The AGC peak detector capacitor should always be set to 1500 pF. This represents a reasonable tradeoff between leakage current tolerance and storage aperture time.

The pulse area detector storage capacitor must be chosen to keep the AGC circuit operating within its linear range. Its value is related to the VCO frequency as follows:

$$C_{AD} = \frac{620}{f_{VCO}(MHz)} pF$$, where f_{VCO} is the VCO freq.

Larger values for CAD are required with lower VCO frequencies in order to maintain constant signal levels within the device, since the integration time is increased.

$$K = 2\frac{V_{AGCADJ}(typ)}{VCC(min)} \qquad dv = \frac{\Delta V}{AGCADJGain(max)}$$

$$R1 = \frac{R_{AGC}(min)}{K}\left(\frac{V_{AGCADJ}(min)}{dv} - 1\right)$$

$$R2 = \frac{K}{1-K}(R1)$$

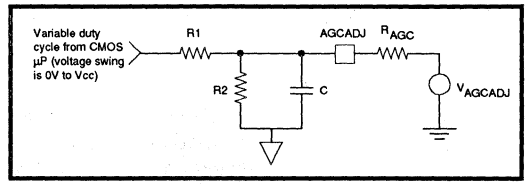

FIGURE 3: AGCADJ Input

for example if: $\Delta V = 0.4V$, $VCC = 5V \pm 5\%$, $Ta = 0\text{-}70°C$
$VREF = 5.4V \pm 6\%$

then: $K = .318$, $dv = 0.26V$, $R1 = 20.4k$,
$R2 = 9.5k$

The amplitude of N & Q signals can be adjusted using the AGCADJ input. If it is desired to adjust the N & Q amplitude by ± ΔV volts, the values of R1 and R2 can be calculated from K and dv as shown in figure 3.

When R1 & R2 are calculated, a filter capacitor C is calculated from the replication rate of the µP duty cycle output. The parallel combination of R1, R2, R_{AGC} minimizes the ripple of V_{AGC}, and yet still provides sufficient response time to changes in duty cycle.

SYNC DETECTOR

Two sync detector parameters may be adjusted with external components. The first is the valid pulse threshold. The threshold is expressed as a percentage of a full scale pulse (since the sync detector follows the AGC and input amplitude variations are removed). The threshold is determined with resistor R_{TH} as follows:

$$Threshold = \frac{0.44}{R_{TH}(k\Omega)} \cdot 100(\%)$$

For example, a value of R_{TH} = 1.0 kΩ sets the valid pulse threshold at 44% of full scale. This prevents false triggering on noisy signals, but does not unduly shorten the sync pulse.

A timing window is used to detect sync pulses, since the sync and data pulses are more closely spaced than any other pulses in a valid servo signal. The delay from the zero crossing of the data pulse to the leading edge of the sync pulse is 1.5 cycles of the VCO clock. The next most closely spaced pulses (which must be rejected by the sync detect circuit) are separated by 3

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APPLICATIONS INFORMATION (Continued)

SYNC DETECTOR (Continued)

VCO cycles. Thus the timing window should be set for 2 cycles of the VCO clock, to allow reliable detection of the sync pulse while suppressing false syncs. The timing window is determined as follows:

$$0.4\,(R_W \cdot C_W) + 43 \cdot 10^{-9}$$

The resistor Rw should always be set to 5.6 kΩ, which means that for a 2 cycle window, Cw is given by:

$$Cw = \frac{900}{fvco(MHz)} - 19pF$$

For a 12.8 MHz clock, Cw should be chosen as 51 pF.

LOCK DETECTOR

The LOCK detector behavior is controlled by the value of C_{LD}. A value too small will be prone to unlock prematurely and give false warnings to the system. A typical value for C_{LD} is 0.001µF.

PHASE LOCKED LOOP

The VCO center frequency is determined by Rvco and Cvco. Rvco should always be set to 11 kΩ ± 1%. Cvco may then be chosen by:

$$C_{VCO} = \frac{830}{f_{VCO}} - 10.6\,pF,$$

where fvco is the desired center frequency in MHz.

For fvco = 12.8 MHz, Cvco = 54 pF and for fvco = 4 MHz, Cvco = 200 pF. If 1% tolerance external components are used, the VCO absolute frequency accuracy will be 15%. The VCO output frequency is related to the control voltage at the loop filter pin, V_{LF}, as follows:

$$fo/fvco = 1 + 1.667(V_{LF} - V_{BPI})$$

This means that the VCO gain, K_O, is given by:

$$K_O = 2 \cdot \pi \cdot fvco(Hz) \cdot 1.667\ rads/s/V$$

The phase detector is a digitally controlled charge pump, which injects a current into the loop filter whose average value is proportional to the phase error. The detector gain, K_d, is fixed at 32 µA/rad. If a loop filter consisting of a series resistor and capacitor is used, as shown in Figure 2, the phase locked loop becomes a second order system with the following transfer function:

$$\frac{\text{phase error}}{\text{input phase}}(s) = \frac{(s/\omega n)^2}{1 + 2 \cdot \zeta \cdot s/\omega n + (s/\omega n)^2}$$

where:

$$\omega n\,(\text{natural freq.}) = \sqrt{((K_d \cdot K_O/(32 \cdot C_{L1}))}\ rad/s$$

$$\zeta(\text{damping factor}) = 0.5 \cdot R_L \cdot C_{L1} \cdot \omega n$$

As an example, the values for Cvco, R_L and C_L are

$$fvco = 12.8\,MHz,\ \omega n/(2 \cdot \pi) = 4600\,Hz,\ \zeta = 0.68$$

$$C_{VCO} = \frac{830}{fvco} - 10.6 = 54pF$$

$$C_{L1} = \frac{K_d K_O}{32 \cdot \omega n^2} = \frac{(32 \cdot 10e-6)(10.47 \cdot f_{VCO})}{32(2 \cdot \pi \cdot 4600)^2} = .2\mu F$$

$$R_L = \frac{2 \cdot z}{C_{L1} \cdot \omega n} = 470\,\Omega$$

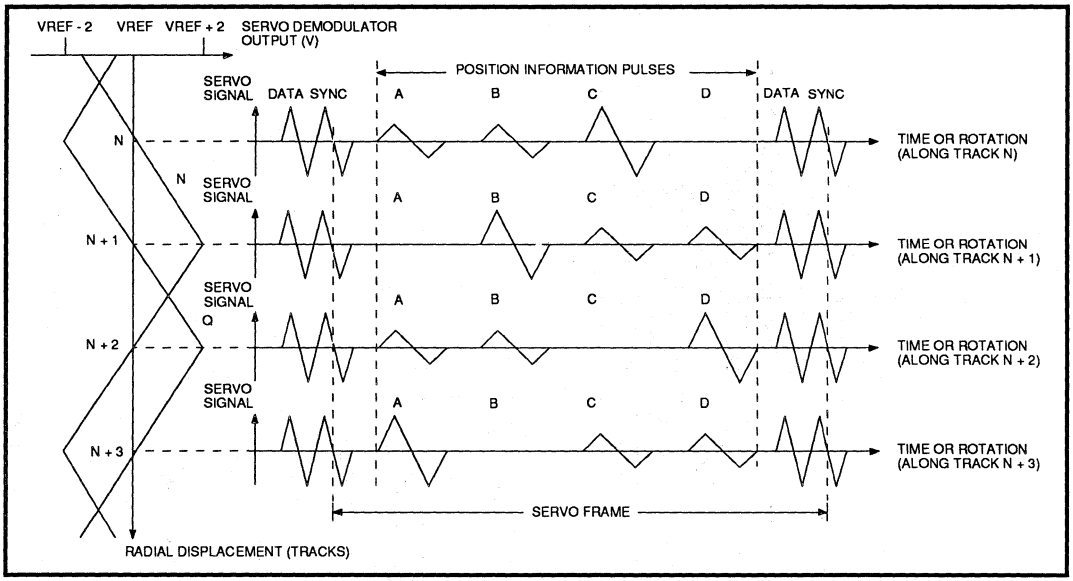

FIGURE 4: Pre-recorded Servo Signal and Servo Demodulator Output vs. Radial Displacement

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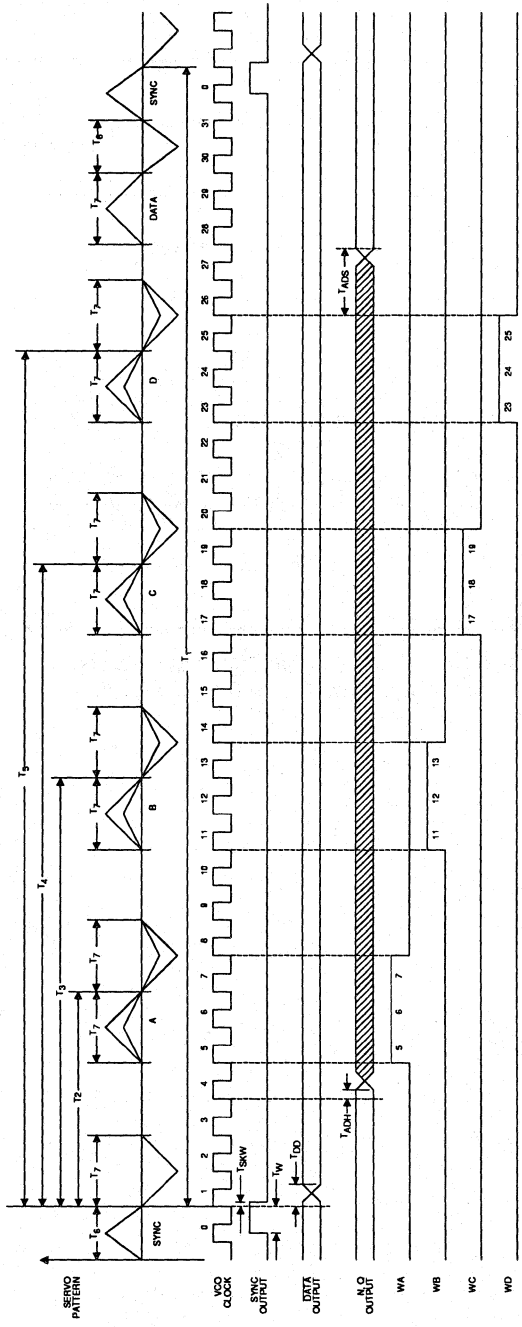


FIGURE 5: Timing Diagram

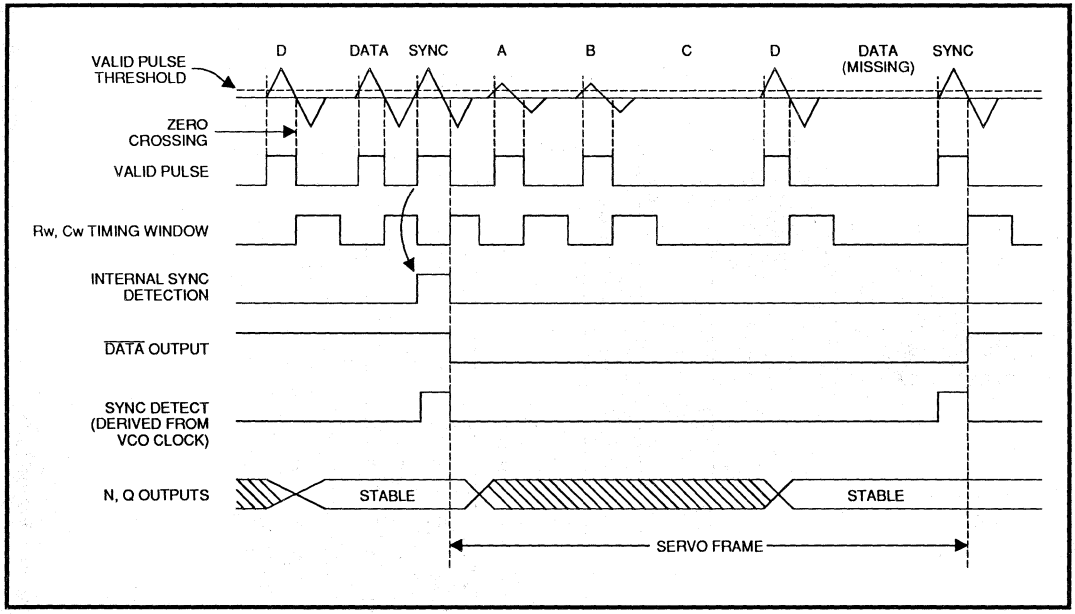


FIGURE 6 : Sync and $\overline{DATA}$ Pulse Detection

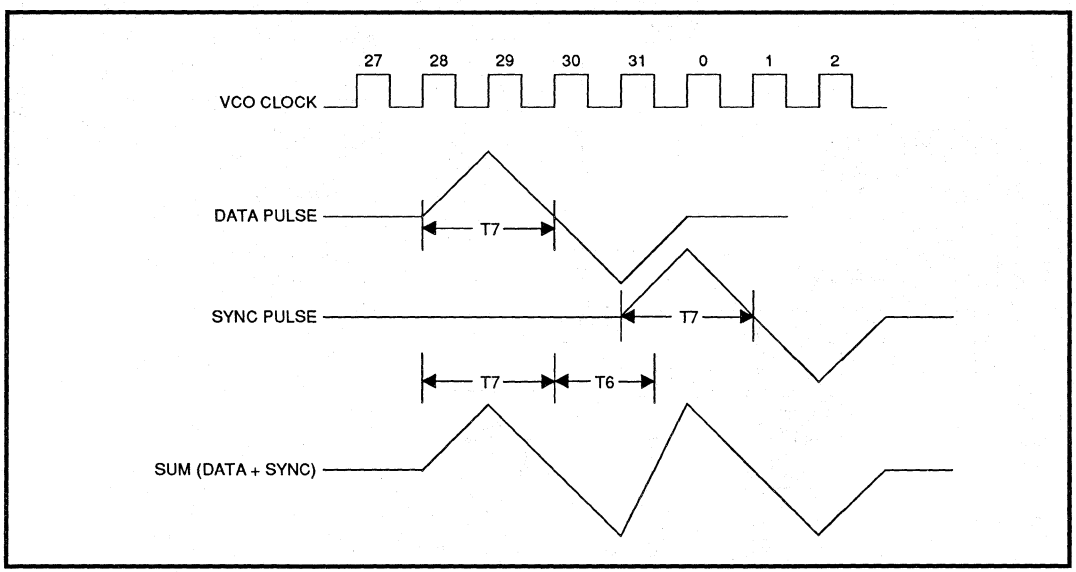


FIGURE 7 : Servo Writer Data-Sync Pulse Generation

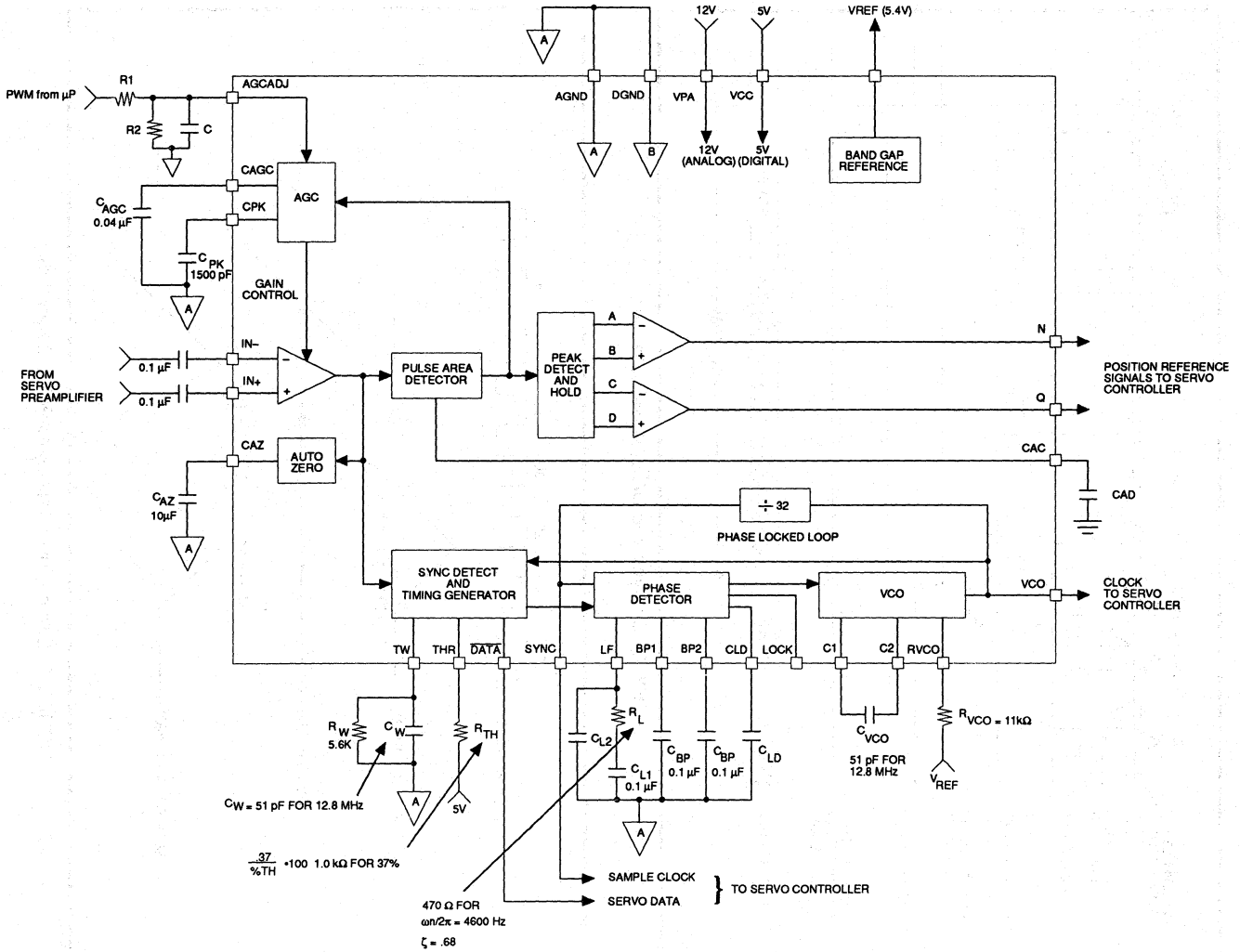


FIGURE 8: Design Example for 400 kHz Frame Rate

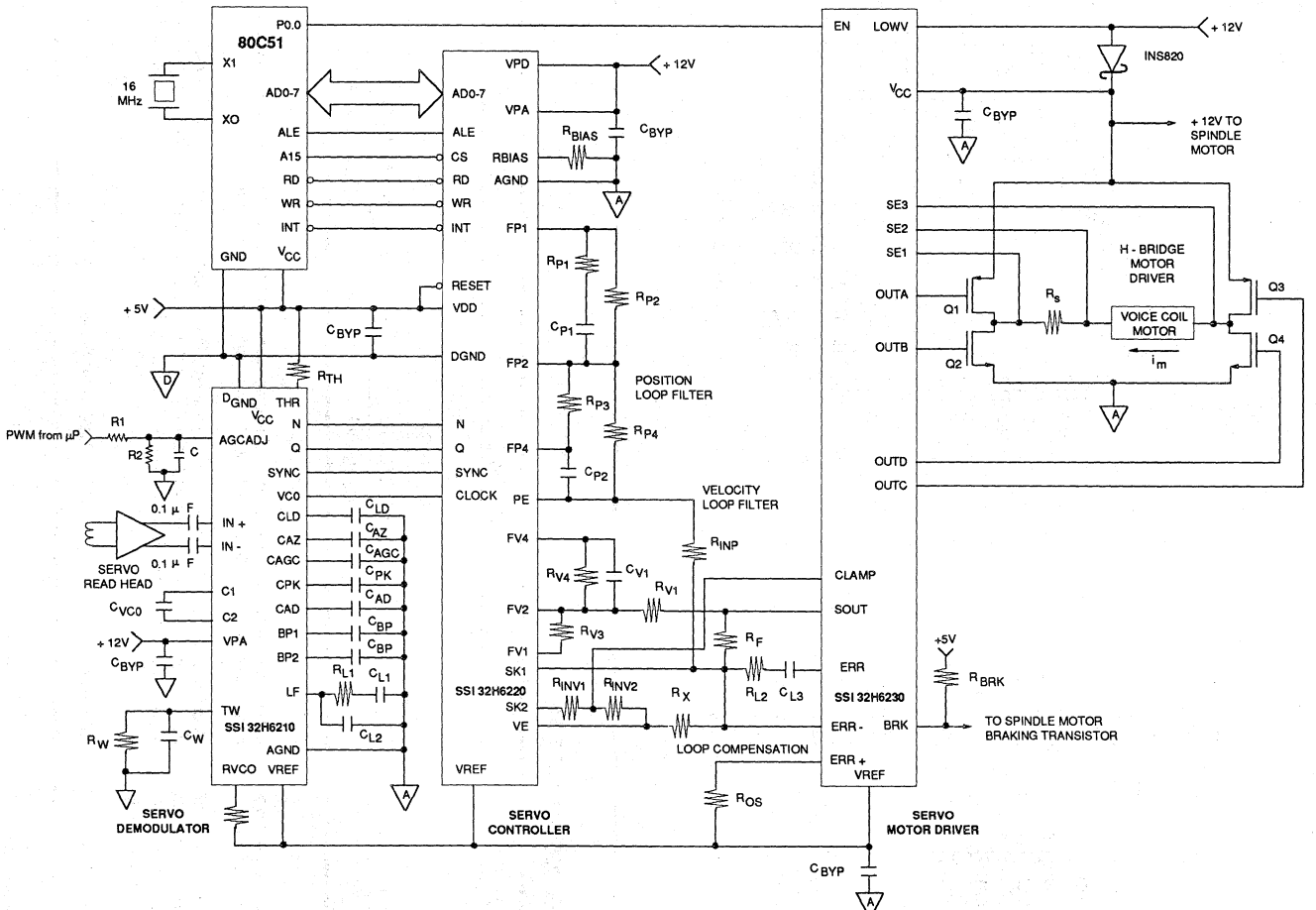
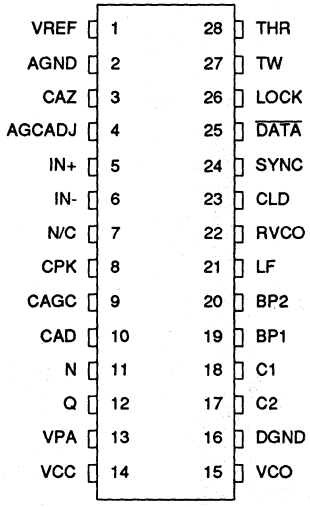


FIGURE 9: Complete Example of Servo Path Electronics Using SSI 32H6210/6220/6230 Chip Set

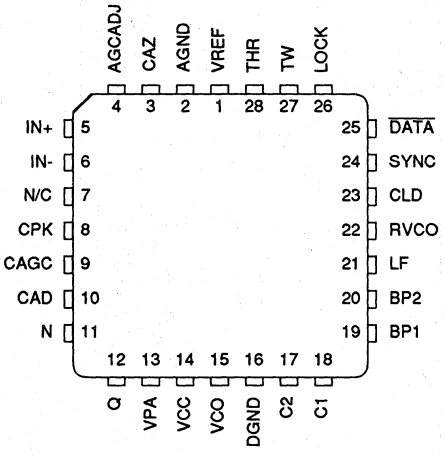
SSI 32H6210
Servo Demodulator

PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



28-Pin DIP,SOL



28-Pin PLCC

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32H6210		
28-Pin DIP	32H6210-CP	32H6210-CP
28-Lead SOL	32H6210-CL	32H6210-CL
28-Lead PLCC	32H6210-CH	32H6210-CH

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914

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SSI 32H6215
Servo Demodulator

Advance Information

January 1993

DESCRIPTION

The SSI 32H6215 Servo Demodulator is a BiCMOS device intended for use in Winchester disk drives with dedicated surface head positioning systems. It processes a di-bit quadrature pattern read from the servo surface by a preamplifier, such as the SSI 32H6110, and generates normal and quadrature (N and Q) position reference signals. These signals provide the servo controller with position error feedback. A complete position control system can be realized with the SSI 32H6215 and its companion device, the SSI 32H4633 Servo Controller and Servo Motor Pre-Driver.

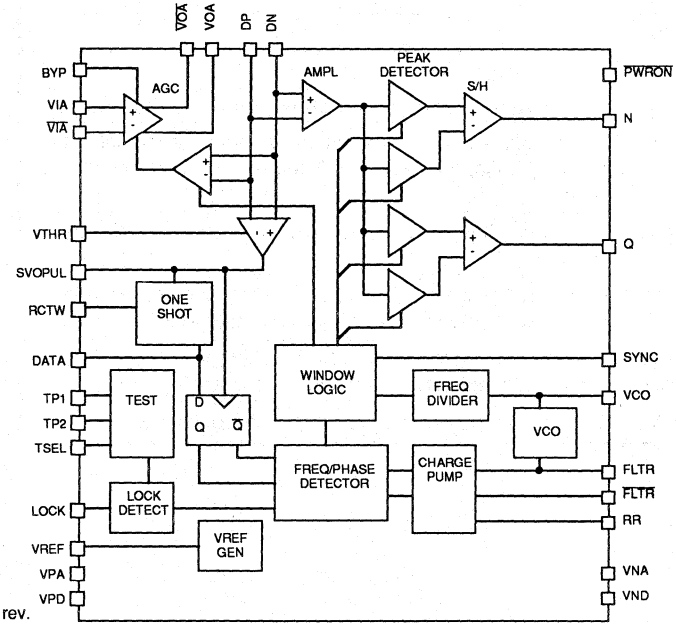
The SSI 32H6215 incorporates an input amplifier with automatic gain control and offset cancellation, a phase locked loop and sync separator to recover timing information, and pulse peak detectors to recover the position information. External components are used to set the operating characteristics of the SSI 32H6215, such as AGC response, VCO center frequency, PLL response and sync separator threshold. Its high performance analog/digital circuitry is capable of supporting servo frame rates of up to 500 kHz.

FEATURES

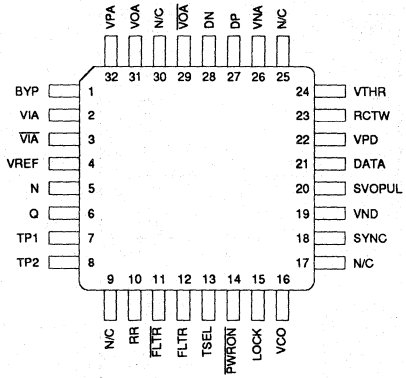
- **Servo signal demodulation for dedicated surface head positioning systems**
- **Supports industry standard di-bit quadrature servo pattern with frame rates up to 500 kHz**
- **N, Q outputs convey track crossing and position error information**
- **PLL for timing recovery and synchronization**
- **Adjustable sync separator threshold**
- **AGC reference level adjustment**
- **Precision bandgap voltage reference output**
- **Advanced BiCMOS process dissipates less than 200 mW (5V)**
- **Available in 32-lead TQFP package**

7

BLOCK DIAGRAM



PIN DIAGRAM



32-Lead TQFP

0193 - rev.

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
VPA	-	Analog Supply: 5V power supply.
VPD	-	Digital Supply: 5V power supply.
BYP	-	AGC Bypass: AGC bypass capacitor.
VOA	O	AGC Output: AGC analog output
$\overline{\text{VOA}}$	O	AGC Output: AGC analog output.
DP	O	Differential Positive Input: Positive input of peak detect circuit.
DN	O	Differential Negative Input: Negative input of peak detect circuit.
VNA	-	Analog Ground.
VND	-	Digital Ground.
VTHR	-	Pulse Threshold: A resistor which sets a threshold for SYNC and DATA pulse detection must be connected between this pin and VCC (digital 5V supply).
SVOPUL	O	Servo Output Level.
RCTW	-	RC Timing Window: A resistor and capacitor must be connected in parallel between this pin and analog ground to set a timing window which is used in detecting SYNC pulses.
DATA	O	Data Output: Active high TTL compatible digital output that indicates the presence of a data pulse in the servo frame. This signal is updated on the falling edge of the sync pulses.
TP1	I/O	Test Point 1.
TP2	I/O	Test Point 2.
TSEL	I	Test Select.
$\overline{\text{PWRON}}$	I	Power On: Active low power on input.
LOCK	O	Lock Output: An open collector output that indicates the lock status of the PLL.
SYNC	O	Sync Output: TTL compatible digital clock whose falling edge indicates the presence of valid analog signal on the N and Q outputs. There is one SYNC cycle per servo frame.
VCO	O	VCO Output: TTL compatible digital clock which is 32 times the sync frequency (servo frame).
FLTR	-	Phase Lock Loop Filter: An external RC network which sets the PLL loop characteristics must be connected between this pin and analog ground.
$\overline{\text{FLTR}}$	-	Phase Lock Loop Filter: An external RC network which sets the PLL loop characteristics must be connected between this pin and analog ground.
VREF	O	Reference Voltage: All analog voltages are referenced to this voltage.

PIN DESCRIPTION (contiued)

NAME	TYPE	DESCRIPTION
N	O	N Output: This sampled and held analog output is the normal position reference output. N is referenced to VREF and is periodic in radial displacement with a period of 4 tracks.
Q	O	Q Output: This sampled and held analog output is the quadrature position reference output. Q is referenced to VREF and is periodic in radial displacement with a period of 4 tracks.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation beyond the maximum ratings may damage the device.

PARAMETER	RATING
VCC voltage	0 to 8V
VPA voltage	0 to 8V
Voltage on PLL inputs	-0.5 to VCC + 0.5V
Voltage on other inputs	0 to 8V
Storage Temp.	-45 to 160°C
Solder Temp. 10 sec. duration	260°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VPA, analog voltage		4.5		5.5	V
Supply noise				0.1	Vpp
VCC, digital supply		4.5		5.5	V
Ta, ambient temperature		0		70	°C
VCO operating range				16	MHz
Load resistance		10			kΩ
Load capacitance				50	pF

DC CHARACTERISTICS

IPA, VPA current				30	mA
ICC, VCC current				20	mA
Sleep current	IPA + ICC			0.5	mA
VOH, digital output high		2.4			V
VOL, digital output low				0.5	V
IREF, VREF output current capacity		10			mA
VREF output voltage					V

AGC AMPLIFIER

Input signals are AC coupled to VIA/$\overline{\text{VIA}}$, VOA/$\overline{\text{VOA}}$ outputs are AC coupled to DP/DN. A 1000 pF capacitor (CBYP) is connected from BYP to VCA. Unless otherwise specified outputs are measured differentially at VOA/$\overline{\text{VOA}}$, FIN = 4 MHz.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Input Range		25		375	mVpp
DP-DN Voltage	VIA-$\overline{\text{VIA}}$ = 0.1Vpp	0.9		1.1	Vpp
DP-DN Voltage variation	25mV < VIA-$\overline{\text{VIA}}$ < 375mV			8	%
Gain Range		2.5		40	V/V
Differential input impedance		4.7	6	8.4	kΩ
Single ended input impedance			3.3		kΩ
Output offset voltage	Gain = 22	-200		200	mV
Input noise voltage	Gain = 22, VIA/$\overline{\text{VIA}}$ short		10		nV/√Hz
CMRR	Gain = 22, fc = 5MHz	40			dB
PSRR	Gain = 22, fc = 5MHz	45			dB
Single ended output resistance			150		Ω

AGC CONTROL

The input signals are AC coupled into DP/DN, CBYP = 1000 pF to VPA.

Decay current	Normal delay (ID)		4		µA
Attack current	Normal attack (ICH)		0.18		mA
BYP Leakage current		-10		10	nA

VOLTAGE REFERENCE

Voltage		1.9	2	2.1	V
Output Impedance				20	Ω
Output current capability		-0.5		5	mA

N,Q OUTPUTS

Output impedance				250	Ω
Volts per track		0.9	1	1.1	V/track
Offset voltage				20	mV

ELECTRICAL SPECIFICATIONS (continued)

VCO

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VCO center frequency fc		TBD		TBD	MHz
Frequency dynamic range VCO		±25		±45	%
VCO control gain KVCO		0.14 ωi		0.26 ωi	Rad/(V-s)
Phase detector gain constant KD		0.83 KD		1.17 KD	A/rad
KVCO x KD product accuracy		-28		28	%
VCO output frequency f VCO				16	MHz
Precision external resistor RR			12.5		kΩ

VALID PULSE DETECTOR

Input voltage range	Vsd	At,DP, DN	0.9	1	1.1	Vpp
Threshold voltage	Vthr	Resistor divider from VPA to Vref	Vref			V
Threshold input current	Ithr	DP, DN shorted, Vth r= Vref + 0.5V			TBD	µA
Detector zero crossing	Tdp	Vsd=1.1Vpp Measured at SVOPUL T.P.			TBD	nsec

SYNC SEPARATOR

Timing window	Tw	Rw(Ω), Cw(F)		0.92 RwCw		Sec
Window resistance	Rw		10			kΩ
RCTW output low voltage	Vol				0.1	V

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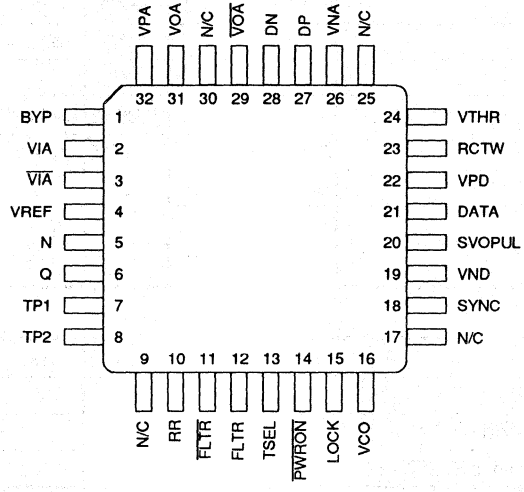
SSI 32H6215
Servo Demodulator

PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



32-Lead TQFP

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

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SSI 32H6230
Servo Motor Driver

June 1993

DESCRIPTION

The SSI 32H6230 Servo Motor Driver is a bipolar device intended for use in Winchester disk drive head positioning systems employing linear or rotary voice coil motors. When used in conjunction with a position controller, such as the SSI 32H6220 Servo Controllers, and a position reference, such as the SSI 32H6210 Servo Demodulator, the device allows the construction of a high performance, dedicated surface head positioning system.

The SSI 32H6230 serves as a transconductance amplifier by driving 4 MOSFETs in an H-bridge configuration, performs motor current sensing and limits motor current. In its linear tracking mode, class B operation is guaranteed by crossover protection circuitry, which ensures that only one MOSFET in each leg of the H-bridge is active. The MOSFET drivers are disabled when motor velocity or current exceed externally programmable limits. In addition, automatic head retraction and spindle braking may be initiated by a low voltage condition or upon external command.

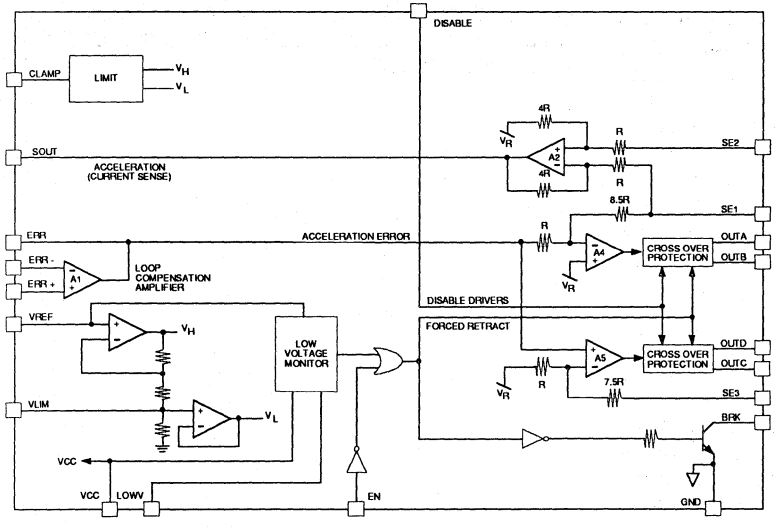
(Continued)

FEATURES

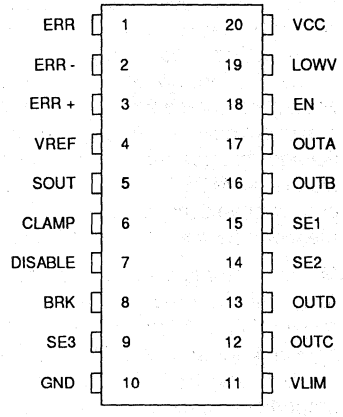
- **Predriver for linear and rotary voice coil motors**
- **Interfaces directly to MOSFET H-Bridge motor driver**
- **Class B linear mode and constant velocity retract mode**
- **FET disable function**
- **Precision differential amplifier for motor current sensing**
- **Clamp for motor current limiting**
- **Automatic head retract and spindle braking signal on power failure**
- **External digital enable**
- **Servo loop parameters programmed with external components**
- **Advanced bipolar IC requires under 240 mW from 12V supply**
- **Available in 20-pin DIP or SO packaging**

7

BLOCK DIAGRAM



PIN DIAGRAM



DESCRIPTION (continued)

The SSI 32H6230 is implemented in an advanced bipolar process and dissipates less than 240 mW from a 12V supply. The IC is available in 20-pin DIP and 20-pin SO packaging.

FUNCTIONAL DESCRIPTION

(Refer to block diagram and typical application Fig.2)

The SSI 32H6230 has two modes of operation, linear and retract. The retract mode is activated by a power supply failure or when the control signal EN is false. Otherwise the device operates in linear mode.

During linear operation, an acceleration signal from the servo controller is applied through amplifier A1, whose three connections are all available externally. RC components may be used to provide loop compensation at this stage. The ERR signal drives two precision amplifiers, each with a gain of 8.5. The first of these amplifiers is inverting, and is formed from opamp A4, an on-chip resistor divider and an off-chip complementary MOSFET pair. The second is non-inverting, and is formed in a similar manner from opamp A5. Feedback from the MOSFET drains, on sense inputs SE1 and SE3, allows the amplifiers gains to be established precisely. The voice coil motor and a series current sense resistor are connected between SE1 and SE3.

Crossover protection circuitry between the outputs of A4 and A5, and the external MOSFETs, ensures class B operation by allowing only one MOSFET in each leg of the H-bridge to be in conduction. The crossover separation threshold, illustrated in Figure 5, is the maximum drive on any MOSFET gate when the motor voltage changes sign. The crossover circuitry can also disable all MOSFETS simultaneously (to limit motor current or velocity) or apply a constant voltage across the motor (to retract the heads at a constant velocity).

Motor current is sensed by a small resistor placed in series with the motor. The voltage drop across this resistor is amplified by a differential amplifier with a gain of 4 (A2 and associated resistors), whose inputs are SE1 and SE2. The resulting voltage, SOUT, is proportional to motor current, and hence acceleration. This signal is externally fed back to A1, so that the signal ERR represents the difference between the desired acceleration (from the servo controller) and the actual motor acceleration.

An adjustable voltage clamp is provided to prevent over current to the motor. It accomplishes the current limiting by clamping the voltage excursion at the input of A1. The voltage clamp values are programmed by VREF and VLIM. VLIM is the lower clamp value and the upper clamp limit is 2 • VREF - VLIM.

The disable function will cause all 4 bridge FETs to turn off. Note that this function does not override the retract function.

The SSI 32H6230 has low voltage monitor circuitry that will detect a loss of voltage on the VREF, VCC or LOWV pins. The power supply pin, VCC, should be connected to the disk drive's spindle motor so that its stored rotational energy may be used to hold up VCC briefly during a power failure. LOWV is used to detect a system power supply failure. When a low voltage condition is detected, the MOSFET drivers switch from linear operation to retract mode. In this mode a constant voltage is applied across the motor which will cause the heads to move at a constant speed. A mechanical stop must be provided for the heads when they reach a safe location. The current limiting circuitry will disable the MOSFET drivers when motor current increases due to loss of the velocity-induced back EMF. An open collector output, BRK, which is active while the device is in retract mode, is provided for spindle motor braking. An external RC delay may be used to defer braking until the heads are retracted.

Two examples of an entire servo path implemented with the SSI 32H6230 and its companion devices, the SSI 32H567, 32H568, and the SSI 32H6210, 32H6220 are shown in Figure 7.

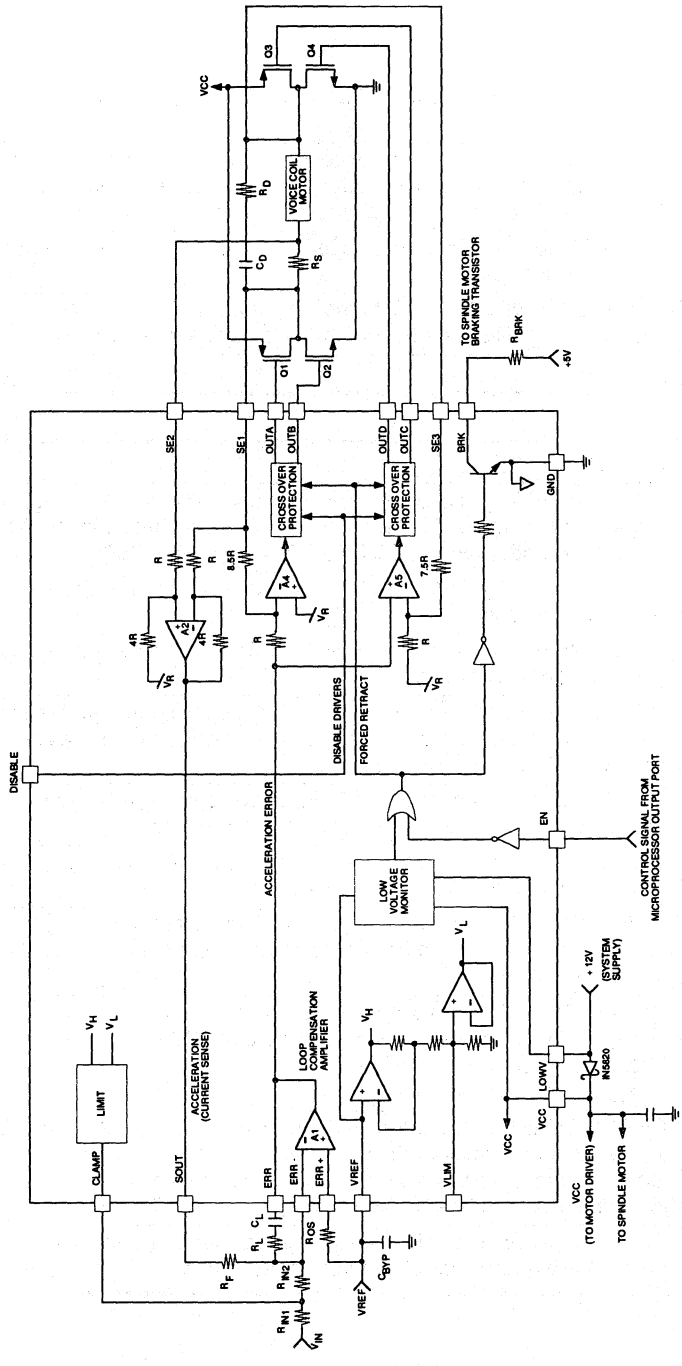


FIGURE 2: Typical Application

7

PIN DESCRIPTION

POWER

NAME	TYPE	DESCRIPTION
VCC		POSITIVE SUPPLY - 12V power supply. Usually taken from spindle motor supply. Spindle motor stored energy permits head retraction during power failure. If VCC falls below 9V, a forced head retraction occurs.
LOWV	I	LOW VOLTAGE - System 12V supply. If this input falls below 9V, a forced head retraction occurs.
VREF	I	REFERENCE VOLTAGE - 5.4V input. All analog signals are referenced to this voltage. If VREF falls below 4.3V, a forced head retraction occurs.
GND		GROUND

CONTROL

NAME	TYPE	DESCRIPTION
ERR	O	POSITION ERROR- Loop compensation amplifier output. This signal is amplified by the MOSFET drivers and applied to the motor by an external MOSFET H-bridge, as follows: SE3-SE1 = 17(ERR-VREF)
ERR-	I	POSITION ERROR INVERTING INPUT - Inverting input to the loop compensation amplifier.
ERR+	I	POSITION ERROR NON-INVERTING INPUT - Non-inverting input to the loop compensation amplifier.
SOUT	O	MOTOR CURRENT SENSE OUTPUT - This output provides a voltage proportional to the voltage drop across the external current sense resistor, as follows: SOUT-VREF=4(SE2-SE1)
DISABLE	I	DISABLE INPUT – Active High TTL input will cause all 4 bridge FETs to turn off. DISABLE does not override the retract function.
CLAMP	I	CLAMP – A clamp pin to limit the input error voltage. The voltage swing at this pin is limited to VREF +- (VREF - VLIM).
BRK	O	BRAKE OUTPUT – Active high, open collector output which may be used to enable an external spindle motor braking transistor upon power failure or deassertion of EN.
VLIM	I	VOLTAGE LIMIT – The voltage at this pin sets the upper and lower clamp voltage limits in conjunction with the voltage at VREF. Upper Clamp Limit = 2 • VREF - VLIM Lower Clamp Limit = VLIM.
SE2	I	MOTOR CURRENT SENSE INPUT - Non-inverting input to the current sense differential amplifier. It should be connected to one side of an external current sensing resistor in series with the motor. The inverting input of the differential amplifier is connected internally to SE1.
EN	I	ENABLE - Active high TTL compatible input enables linear tracking mode. A low level will initiate a forced head retract.

FET DRIVE

NAME	TYPE	DESCRIPTION
SE3	I	MOTOR VOLTAGE SENSE INPUT - This input provides feedback to the non-inverting MOSFET driver amplifier. It is connected to one side of the motor. The gain to this point is: SE3-VREF = 8.5(ERR-VREF)
OUTC	O	P-FET DRIVE (NON-INVERTING) - Drive signal for a P channel MOSFET connected between one side of the motor and VCC. This MOSFET drain is connected to SE3.
OUTD	O	N-FET DRIVE (NON-INVERTING) - Drive signal for an N channel MOSFET connected between one side of the motor and GND. This MOSFET drain is connected to SE3. Crossover protection circuitry ensures that the P and N channel devices driven by OUTC and OUTD are never enabled simultaneously.
SE1	I	MOTOR VOLTAGE SENSE INPUT - This input provides feedback to the inverting MOSFET driver amplifier. It is connected to the current sensing resistor which is in series with the motor. The gain to this point is: SE1-VREF = -8.5(ERR-VREF) This input is internally connected to the current sense differential amplifier inverting input.
OUTB	O	N-FET DRIVE (INVERTING) - Drive signal for an N channel MOSFET connected between the current sense resistor and GND. This MOSFET drain is also connected to SE1.
OUTA	O	P-FET DRIVE (INVERTING) - Drive signal for a P channel MOSFET connected between the current sense resistor and VCC. This MOSFET drain is also connected to SE1. Crossover protection circuitry ensures that the P and N channel devices driven by OUTC and OUTD are never enabled simultaneously.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

(Maximum limits indicates where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC operating characteristics.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VCC		0		16	V
VREF		0		10	V
SE1, SE2, SE3, OUT D		-1.5		15	V
All other pins		-.3		VCC + .3	V
Storage temperature		-45		165	°C
Solder temperature	10 sec duration			260	°C

RECOMMENDED OPERATION CONDITIONS

(Unless otherwise noted, the following conditions are valid throughout this document.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VCC	Normal Mode	9	12	13.2	V
	Retract Mode	3.5V		14	V
VREF		5		7	V
Operating temperature		0		70	°C

DC CHARACTERISTICS

ICC, VCC current				20	mA
IREF, VREF current				2	mA

A1, LOOP COMPENSATION AMPLIFIER

Input bias current				500	nA
Input offset voltage				3	mV
Voltage swing	About VREF	2			V
Common mode range	About VREF	±1			V
Load resistance	To VREF	4			kΩ
Load capacitance				100	pF
Gain		80			dB
Unity gain bandwidth		1			MHz
CMRR	f <20 kHz	60			dB
PSRR	f <20 kHz	60			dB

A2, CURRENT SENSE AMPLIFIER

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input impedance	SE1 to SE2	3.5	5		kΩ
Input offset voltage				2	mV
Output voltage swing		VREF-4		VCC-1.2	V
Common mode range		0		VCC-0.2	V
Load Resistance	To VREF	4			kΩ
Load Capacitance				100	pF
Output impedance	f < 40 kHz			20	Ω
Gain (SOUT-VREF)/(SE1-SE2)	VSE2 = VREF	3.9	4	4.1	V/V
Unity gain bandwidth		1			MHz
CMRR	f < 20 kHz	52			dB
PSRR	f < 20 kHz	60			dB

VOLTAGE CLAMP

CLAMP bias current	CLAMP = VREF			0.1	µA
Upper CLAMP limit (VREF + 1/3 VREF)	ICLAMP = 10 µA VLIM open		$\frac{4}{3}$VREF		V
Lower CLAMP limit (VREF - 1/3 VREF)	ICLAMP = -10 µA VLIM open		$\frac{2}{3}$VREF		V
CLAMP accuracy	| ICLAMP | = 10 µA	-3		3	%
CLAMP Impedance	1.0 mA> | ICLAMP | >10 µA			20	Ω
VLIM Voltage			$\frac{2}{3}$VREF		V
VLIM Accuracy		-1		+1	%

POWER SUPPLY MONITOR

VCC fail threshold		8.5	9	9.8	V
LOWV fail threshold	|ILowv| < 0.5 mA	8.5	9	9.8	V
VREF fail threshold		3.9	4.3	4.8	V
Hysteresis (LOWV, VCC)			250		mV
Hysteresis (VREF)			110		mV
EN input low voltage	|IIL| < 0.5 mA	0.8			V
EN input high voltage	|IIH| < 40 uA			2	V
BRK voltage	normal mode, |IOL| < 1 mA			0.4	V
BRK leakage current	retract mode			10	µA
BRK delay (from power fail or EN false to BRK floating)				1	ms

ELECTRICAL SPECIFICATIONS (continued)

MOSFET DRIVERS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SE3 Input impedance	To VREF	10	25		kΩ
OUTA, OUTC voltage swing |Io|<1 mA		0.7		VCC-1	V
OUTB, OUTD voltage swing |Io|<1 mA		1		VCC-1	V
VTH, Crossover separation threshold				2	V
Slew rate (OUTA, OUTB, OUTC, OUTD)	Cl<1000 pF	1.4			V/µs
Crossover time	300 mV step at ERR			5	µs
Output impedance (OUTA,B,C,D)			50		kΩ
Transconductance I(OUTA,B,C,D)/(ERR-VREF)			8		mA/V
Gain (-(SE1-VREF)/(ERR-VREF) or (SE3-VREF)/(ERR-VREF))		8	8.5	9	V/V
Offset current	R_S = 0.2Ω, R_F = R_{IN}, V_{IN}=VREF			20	mA
Retract motor voltage (SE1-SE3)		0.7	1	1.3	V

APPLICATIONS INFORMATION

A typical SSI 32H6230 application is shown in Figure 2. The selection criteria for the external components shown are discussed below. Figure 3 shows the equivalent circuit and equations for the DC motor used in the following derivations. While the nomenclature chosen is for a rotating motor, the results are equally applicable to linear motors.

MOTOR CURRENT SENSE AND LIMITING

The series resistor which senses motor current, Rs, is chosen to be small compared to the resistance of the motor, Rm. A value of Rs = 0.2Ω is typical in disk drive applications.

VLIM, RIN1, and RIN2 must be chosen to keep the motor current below Imax. The voltage clamp values programmed by VREF and VLIM must be chosen to cause limiting when the motor current reaches its maximum permissible current in amps, this value may be chosen as follows:

$$|Imax| = \frac{CLAMP}{RIN2} \cdot \frac{RF}{4 \cdot Rs}$$

Where the upper clamp limit is 2 • VREF - VLIM and the lower clamp limit is VLIM. If VLIM is left open, a value of 0.667 • VREF will appear. The upper clamp limit is then 1.33 • VREF and the lower clamp limit is 0.667 • VREF. The values of RIN1, RIN2 must be chosen to satisfy the maximum swing of Vin before limiting occurs,

$$Vin(max) = CLAMP\left(1 + \frac{RIN1}{RIN2}\right) - \frac{RIN1}{RIN2}(VREF) + VREF$$

and they should also satisfy the maximum current VCLAMP can source or sink

$$\frac{Vin\ (max)\ [Actual] - CLAMP}{RIN1} \leq 1mA$$

LOOP COMPENSATION

The transfer function of the SSI 32H6230 in the application of Figure 2 is shown in Figure 4(a). If the zero due to R_L and C_L in the loop compensation circuit is chosen to cancel the pole due to the motor inductance, Lm, then the transfer function can be simplified as shown in Figure 4(b), under the assumption that this pole and the pole due to the motor mechanical response are widely separated. C_L may then be chosen to set the desired open loop unity gain bandwidth.

$$C_L = \frac{68 \cdot R_s}{2 \cdot \pi \cdot R_F \cdot (R_m + R_s) \cdot BW}$$

where BW is the unity gain open loop bandwidth

$$R_L = \frac{L_m}{C_L \cdot (R_m + R_s)}$$

The closed loop response of the servo driver and motor combination, using the component values and simplifying assumptions given above, is given by:

$$\frac{i_m}{V_{in}}(s) = -\frac{1}{R_{in}} \cdot \frac{R_F}{4 \cdot R_s} \cdot \frac{1}{\left(1 + \frac{s}{2 \cdot \pi \cdot BW}\right)}$$

Where: Rin = RIN1 + RIN2

(This analysis neglects the pole due to the output impedance of the MOSFET drivers and the MOSFET gate capacitance, an effect that may be significant in some systems.)

RF is chosen to be sufficiently large to avoid overloading A2 (R_F > 4 kΩ). The input resistor, R_{IN}, sets the conversion factor from servo controller output voltage to servo motor current. R_{IN} is chosen such that the servo controller internal voltages are scaled conveniently. The resistor R_{OS} is optional and cancels out the effect of the input bias current of A1.

$$R_{os} = R_{in} // R_F$$

The external components R_D and C_D have no effect on the motor dynamics, but may be used to improve the stability of the MOSFET drivers. The load represented by the motor, ZM, is given by:

$$ZM = (R_s + R_m)\left(1 + s\frac{L_m}{R_s + R_m}\right)\left(1 + \frac{K_m^2}{s \cdot J\theta \cdot (R_s + R_m)}\right)(\Omega)$$

At frequencies above (Rs+Rm)/(2π • Lm) Hz, this load becomes entirely inductive, which is undesireable. R_D and C_D may be used to add some parallel resistive loading at these frequencies.

7

APPLICATIONS INFORMATION (continud)

H-BRIDGE MOSFETS

The MOSFETs chosen for the H-bridge should have gate capacitances in the range of 500-1000 pF. The MOSFET input capacitance forms part of the compensation for the MOSFET drivers, so values below 500 pF may cause some driver instability. Excessive input capacitance will degrade the slew mode performance of the drivers.

When the motor voltage is changing polarity, the crossover protection circuits at outputs OUTA-OUTD ensure that the maximum MOSFET gate drive is less than 2V (the crossover separation threshold), as illustrated in Figure 5. The thresholds of the MOSFET devices chosen should be as large as possible to minimize conduction in this region. If the device thresholds are significantly less than the crossover separation threshold, the N and P channel devices in each leg of the H-bridge will conduct simultaneously, causing unnecessary power dissipation.

POWER FAILURE OPERATION

The power supply for the SSI 32H6230, VCC, should be taken from the system 12V supply through a schottky diode (maximum 0.5V drop at If = 3A) and connected to the disk drive spindle motor. If the system power fails, the IC will continue to operate as the spindle motor becomes a generator. The SSI 32H6230 will detect the power failure and cause a forced head retract, continuing to operate with VCC as low as 3.5V. The power fail mode will commence if either VCC or LOWV falls below 9V, or VREF falls below 4.3V, or EN is false. Hysteresis on the low voltage thresholds prevents the device from oscillating between operating modes when the power supply is marginal.

The BRK output, which is pulled low during normal operation, floats during a power failure. This allows an external transistor to be enabled for spindle motor braking. An external RC delay may be added to defer braking until head retraction is complete, since the spindle motor is required to generate the supply voltage during retraction.

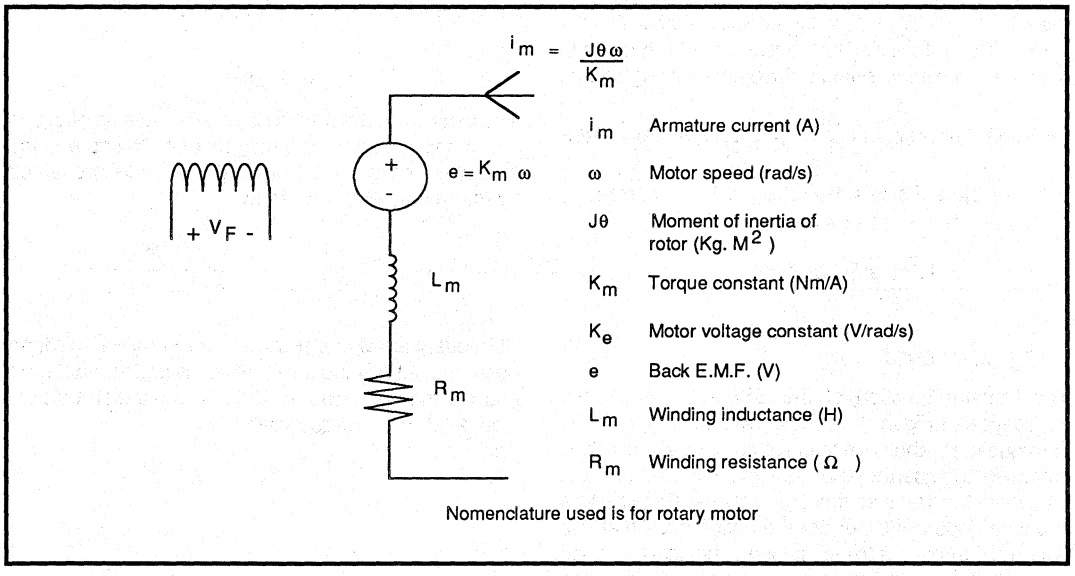


FIGURE 3: Equivalent Circuit for Fixed Field DC Motor

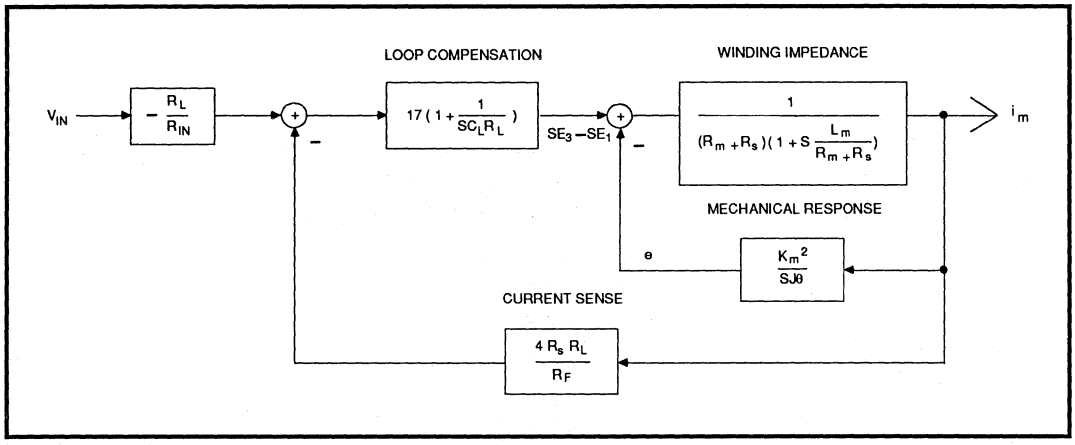


FIGURE 4A: Transfer Function of SSI 32H6230 in Typical Application with Fixed Field DC Motor

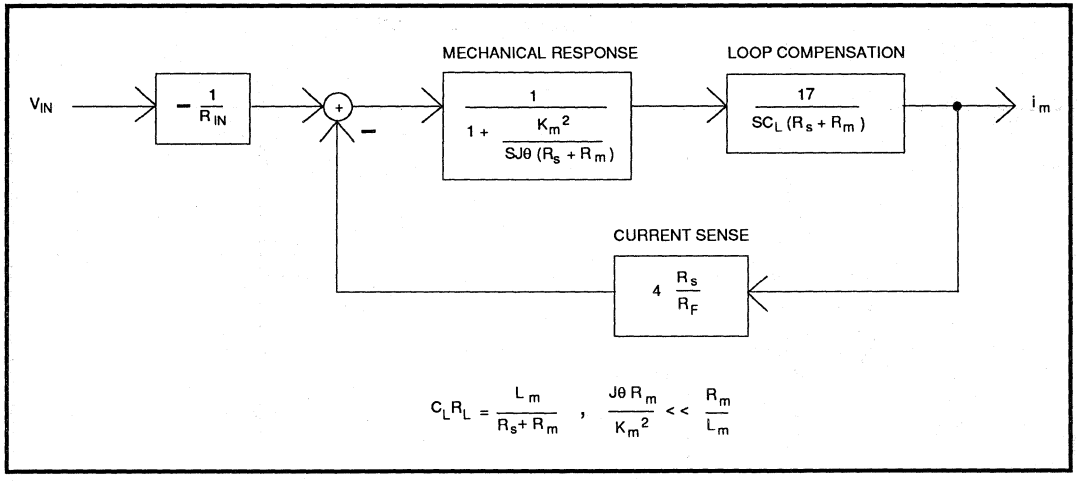


FIGURE 4B: Simplified Transfer Function of SSI 32H6230 in DC Motor Application

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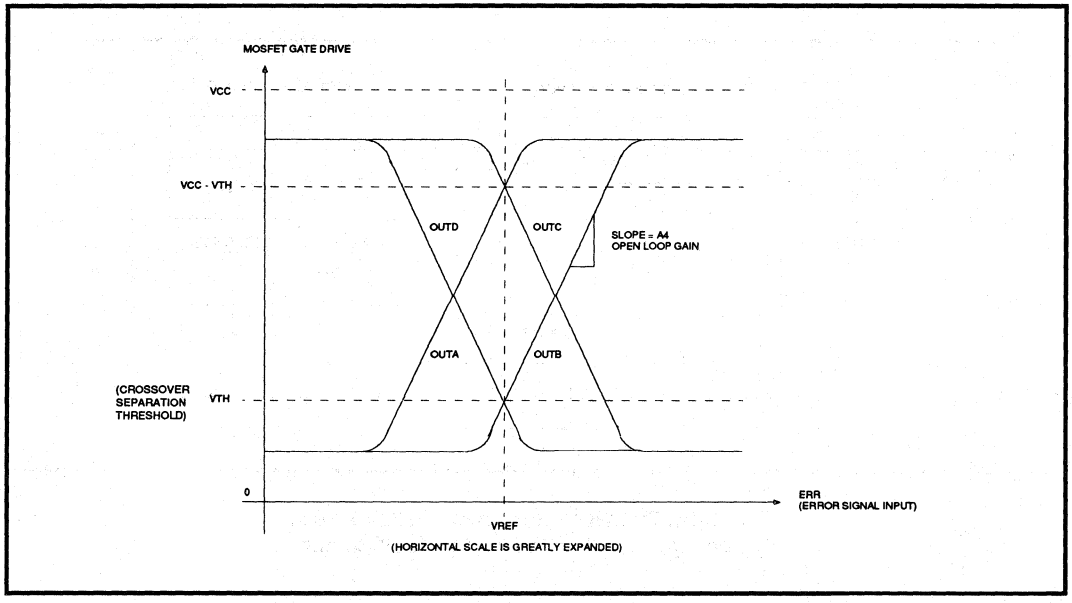


FIGURE 5: Crossover Protection

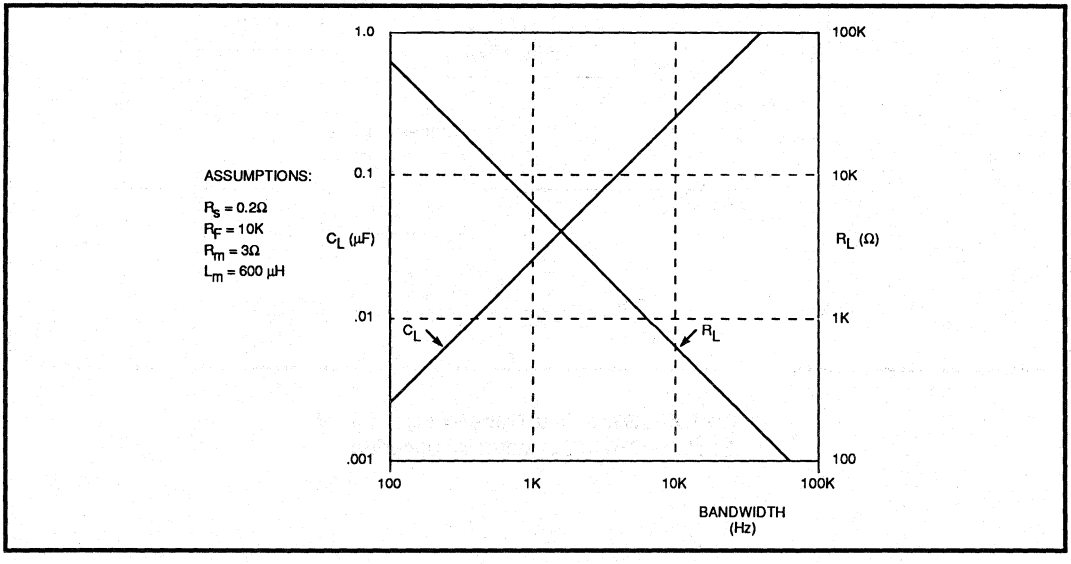


FIGURE 6: Typical Motor Driver Compensation

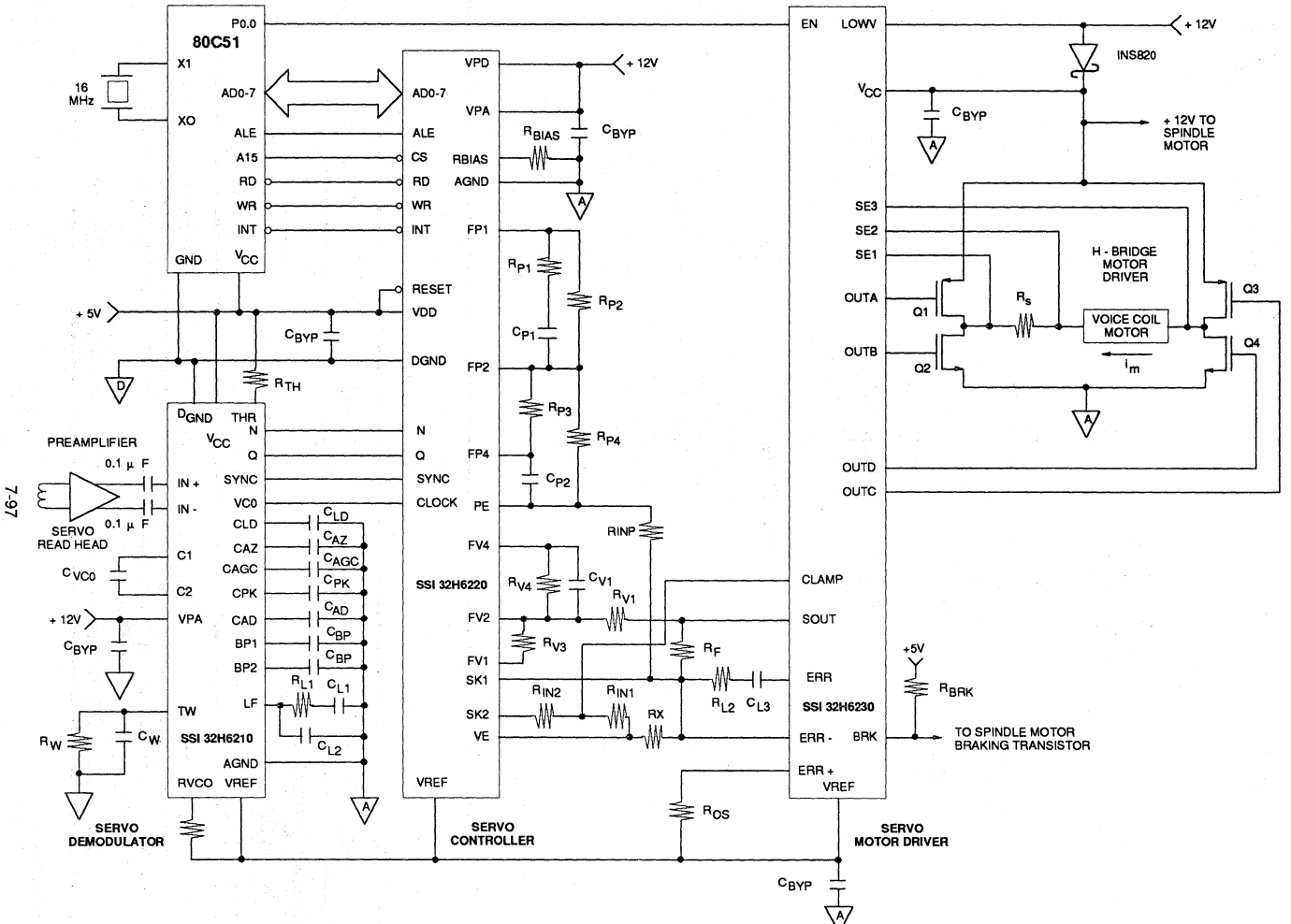
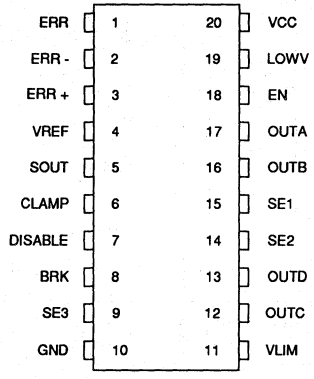


FIGURE 7: Complete Example of Servo Path Electronics Using the SSI 32H6210/6220/6230 Chip Set

SSI 32H6230
Servo Motor Driver

PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



20-Pin DIP, SO

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32H6230, Servo Motor Driver		
20-Pin DIP	32H6230-CP	32H6230-CP
20-Lead SOL	32H6230-CL	32H6230-CL

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914

silicon systems®
A TDK Group Company

SSI 32H6231
Servo Motor Driver

June 1993

DESCRIPTION

The SSI 32H6231 Servo Motor Driver is a bipolar device intended for use in Winchester disk drive head positioning systems employing linear or rotary voice coil motors.

The SSI 32H6231 serves as a transconductance amplifier by driving 4 MOSFETs in an H-bridge configuration, performs motor current sensing and limits motor current and velocity. In its linear tracking mode, class B operation is guaranteed by crossover protection circuitry, which ensures that only one MOSFET in each leg of the H-bridge is active. Head retraction and spindle braking may be initiated by a low voltage condition or upon external command.

The SSI 32H6231 is implemented in a precision bipolar process and dissipates less than 240 mW from a 12V supply. The IC is available in 20-pin SOV packaging.

FEATURES

- **Predriver for linear and rotary voice coil motors**
- **Interfaces directly to MOSFET H-Bridge motor driver**
- **Class B linear mode and constant velocity retract mode**
- **Precision differential amplifier for motor current sensing**
- **External digital enable**
- **Servo loop parameters programmed with external components**
- **Precision bipolar IC requires under 240 mW from 12V supply**
- **Available in 20-pin SOV packaging**

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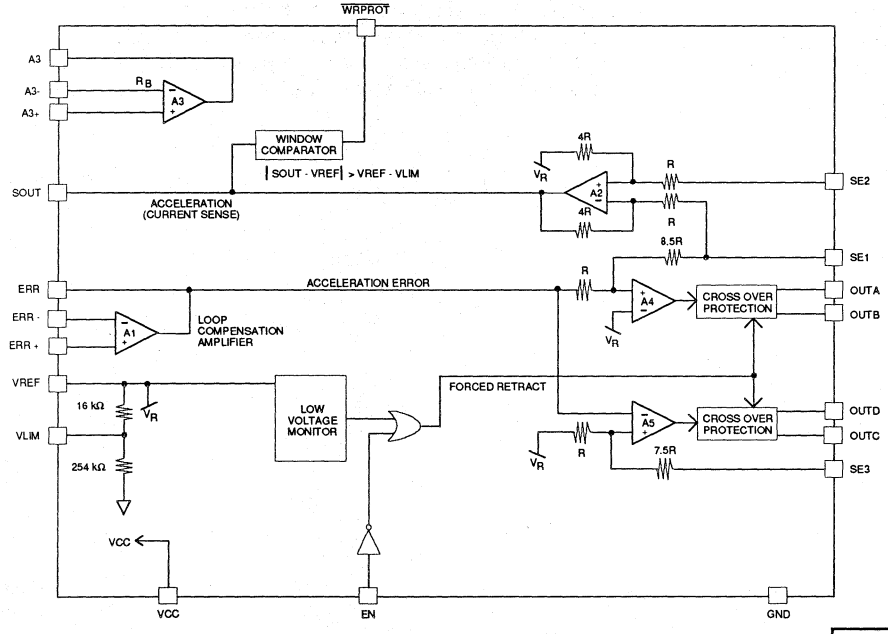
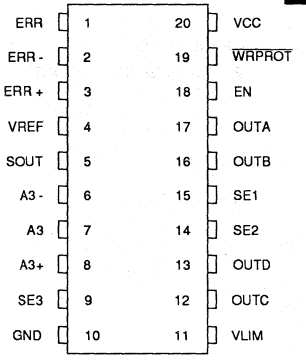
BLOCK DIAGRAM



PIN DIAGRAM



20-Pin SOV

FUNCTIONAL DESCRIPTION

(Refer to block diagram and typcial application Fig. 2)

The SSI 32H6231 has two modes of operation, linear and retract. The retract mode is activated by a VREF failure or when the control signal EN is false. Otherwise the device operates in linear mode.

During linear operation, an acceleration signal from the servo controller is applied through amplifier A1, whose three connections are all available externally. RC components may be used to provide loop compensation at this stage. The ERR signal drives two precision amplifiers, each with a gain of 8.5. The first of these amplifiers is inverting, and is formed from opamp A4, an on-chip resistor divider and an off-chip complementary MOSFET pair. The second is non-inverting, and is formed in a similar manner from opamp A5. Feedback from the MOSFET drains, on sense inputs SE1 and SE3, allows the amplifiers gains to be established precisely. The voice coil motor and a series current sense resistor are connected between SE1 and SE3.

Crossover protection circuitry between the outputs of A4 and A5, and the external MOSFETs, ensures class B operation by allowing only one MOSFET in each leg of the H-bridge to be in conduction. The crossover separation threshold, illustrated in Figure 5, is the maximum drive on any MOSFET gate when the motor voltage changes sign. The crossover circuitry can also apply a constant voltage across the motor (to retract the heads at a constant velocity).

Motor current is sensed by a small resistor placed in series with the motor. The voltage drop across this resistor is amplified by a differential amplifier with a gain of 4 (A2 and associated resistors), whose inputs are SE1 and SE2. The resulting voltage, SOUT, is proportional to motor current, and hence acceleration. This signal is externally fed back to A1, so that the signal ERR represents the difference between the desired acceleration (from the servo controller) and the actual motor acceleration.

SOUT is connected to a window comparator, which is used to detect excessive motor current. When excessive current is detected, $\overline{\text{WRPROT}}$ is pulled low. The VLIM pin may be used to program the voltage limit for the window comparator. The maximum voltage excursion allowed about VREF is (VREF-VLIM). An on-chip resistor divider sets a default value for VLIM and if VLIM is connected to ground, the windowing is effectively disabled.

The SSI 32H6231 has low voltage monitor circuitry that will detect a loss of voltage on VREF. The power supply pin, VCC, should be connected to the disk drive's spindle motor so that its stored rotational energy may be used to hold up VCC briefly during a power failure. When a low voltage condition is detected, the MOSFET drivers switch from linear operation to retract mode. In this mode a constant voltage is applied across the motor which will cause the heads to move at a constant speed. A mechanical stop must be provided for the heads when they reach a safe location.

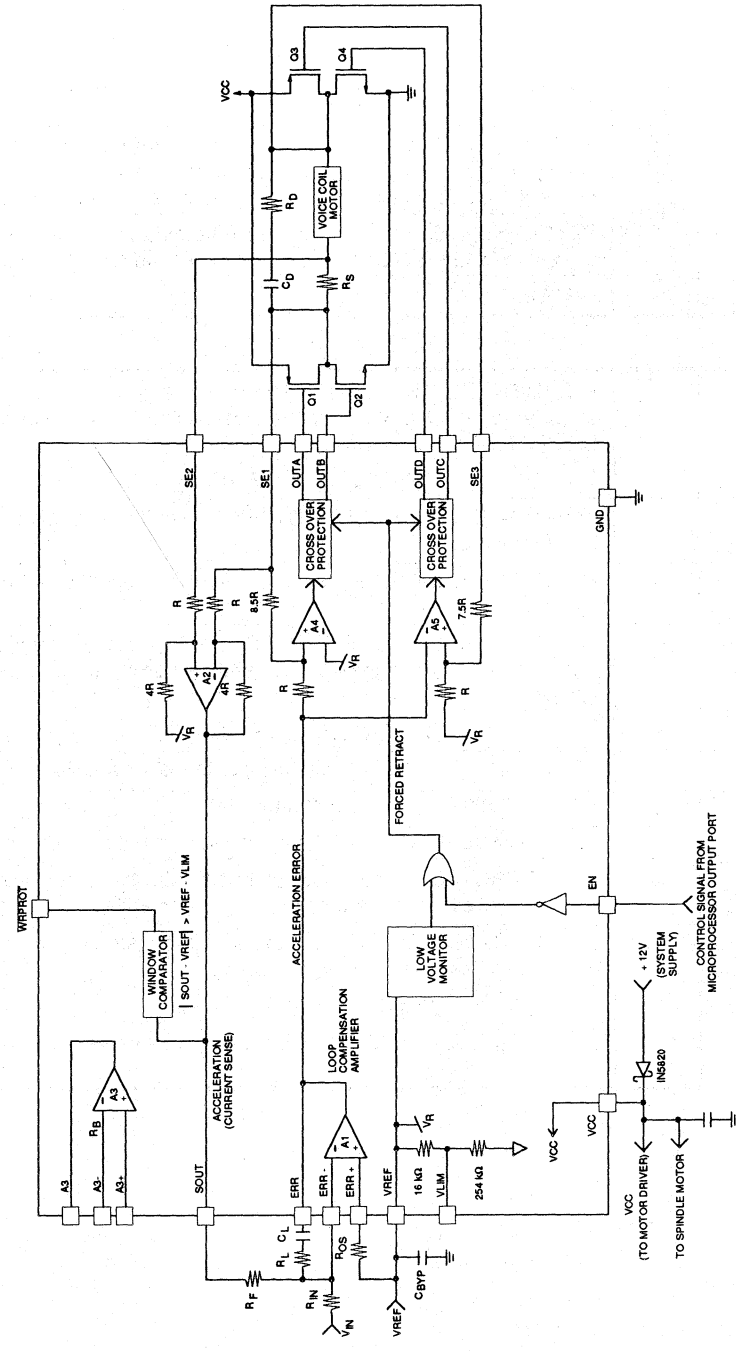


FIGURE 2: Typcial Application

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PIN DESCRIPTION

POWER

NAME	TYPE	DESCRIPTION
VCC	I	POSITIVE SUPPLY - 12V power supply. Usually taken from spindle motor supply. Spindle motor stored energy permits head retraction during power failure. If VCC falls below 9V, a forced head retraction occurs.
VREF	I	REFERENCE VOLTAGE - 5.4V input. All analog signals are referenced to this voltage. If VREF falls below 4.3V, a forced head retraction occurs.
GND	-	GROUND

CONTROL

ERR	O	POSITION ERROR - Loop compensation amplifier output. This signal is amplified by the MOSFET drivers and applied to the motor by an external MOSFET H-bridge, as follows: SE3-SE1 = 17(ERR-VREF)
ERR-	I	POSITION ERROR INVERTING INPUT - Inverting input to the loop compensation amplifier.
ERR+	I	POSITION ERROR NON-INVERTING INPUT - Non-inverting input to the loop compensation amplifier.
SOUT	O	MOTOR CURRENT SENSE OUTPUT - This output provides a voltage proportional to the voltage drop across the external current sense resistor, as follows: SOUT-VREF=4(SE2-SE1)
A3-	I	A3 INVERTING INPUT - Inverting input to the A3 amplifier.
A3	O	A3 OUTPUT - Output of the A3 amplifier.
A3+	I	A3 NON-INVERTING INPUT - Non-inverting input to the A3 amplifier.
$\overline{\text{WRPROT}}$	O	WRITE PROTECT - Active low, an open collector output which is asserted when SOUT exceeds the window comparator limits.
VLIM	I	LIMITING VOLTAGE - The voltage at this pin sets the $\overline{\text{WRPROT}}$ window comparator limits. Limiting occurs when: |SOUT-VREF|>VREF-VLIM An internal resistor divider establishes a default value that may be externally adjusted.

NAME	TYPE	DESCRIPTION
SE2	I	MOTOR CURRENT SENSE INPUT - Non-inverting input to the current sense differential amplifier. It should be connected to one side of an external current sensing resistor in series with the motor. The inverting input of the differential amplifier is connected internally to SE1.
EN	I	ENABLE - Active high TTL compatible input enables linear tracking mode. A low level will initiate a forced head retract.

FET DRIVE

SE3	I	MOTOR VOLTAGE SENSE INPUT - This input provides feedback to the non-inverting MOSFET driver amplifier. It is connected to one side of the motor. The gain to this point is: SE3-VREF = 8.5(ERR-VREF)
OUTC	O	P-FET DRIVE (NON-INVERTING) - Drive signal for a P channel MOSFET connected between one side of the motor and VCC. This MOSFET drain is connected to SE3.
OUTD	O	N-FET DRIVE (NON-INVERTING) - Drive signal for an N channel MOSFET connected between one side of the motor and GND. This MOSFET drain is connected to SE3. Crossover protection circuitry ensures that the P and N channel devices driven by OUTC and OUTD are never enabled simultaneously.
SE1	I	MOTOR VOLTAGE SENSE INPUT - This input provides feedback to the inverting MOSFET driver amplifier. It is connected to the current sensing resistor which is in series with the motor. The gain to this point is: SE1-VREF = -8.5(ERR-VREF) This input is internally connected to the current sense differential amplifier inverting input.
OUTB	O	N-FET DRIVE (INVERTING) - Drive signal for an N channel MOSFET connected between the current sense resistor and GND. This MOSFET drain is also connected to SE1.
OUTA	O	P-FET DRIVE (INVERTING) - Drive signal for a P channel MOSFET connected between the current sense resistor and VCC. This MOSFET drain is also connected to SE1. Crossover protection circuitry ensures that the P and N channel devices driven by OUTC and OUTD are never enabled simultaneously.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

(Maximum limits indicates where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC operating characteristics.)

PARAMETER	RATING
VCC	0 to 16V
VREF	0 to 10V
SE1, SE2, SE3	-1.5 to 15V
All other pins	0 to 14V
Storage temperature	-45 to 165°C
Solder temperature - 10 sec duration	260°C

RECOMMENDED OPERATION CONDITIONS (Unless otherwise noted, the following conditions are valid throughout this document.)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VCC	Normal Mode	9	12	13.2	V
	Retract Mode	3.5		14	V
VREF		4.8		7	V
Operating temperature		0		70	°C

DC CHARACTERISTICS

ICC, VCC current				20	mA
IREF, VREF current				2	mA

A1, LOOP COMPENSATION AMPLIFIER

Input bias current				500	nA
Input offset voltage				3	mV
Voltage swing	About VREF, VREF = 5.4	2			V
Common mode range	About VREF, VREF < Vcc-3	±1			V
Load resistance	To VREF	4			kΩ
Load capacitance				100	pF
Gain		80			dB
Unity gain bandwidth		0.5	1		MHz
CMRR	f<20 kHz	60			dB
PSRR	f<20 kHz	60			dB

A2, CURRENT SENSE AMPLIFIER

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Input impedance	SE1 to SE2	1.0	1.5		kΩ
	SE2 to VR	5	7.5		kΩ
Input offset voltage				2.0	mV
Output voltage swing	VREF = 5.4	VREF-4		VCC-2.0	V
Common mode range		0		VCC-0.2	V
Load Resistance	To VREF	20			kΩ
Load Capacitance				100	pF
Output impedance	f<40 kHz			20	Ω
Gain (SOUT-VREF)/(SE1-SE2)		3.9	4	4.1	V/V
Unity gain bandwidth		0.5	1		MHz
CMRR	f<20 kHz	52			dB
PSRR	f<20 kHz	60			dB

A3 AMPLIFIER

Input bias current				250	nA
Input offset voltage				2	mV
Voltage swing		VREF-4		VCC-1.2	V
Common mode range		2.5		6	V
Load resistance	To VREF	10			kΩ
Load capacitance				100	pF
Gain		60			dB
Unity gain bandwidth		150	250		kHz

WINDOW COMPARATOR

Window comparator threshold (SOUT-VREF)	|SOUT - VREF| increasing	VREF-VLIM			V
Threshold hysteresis			30		mV
VLIM voltage	No external parts	92	94	96	% VREF
VLIM input resistance		8	15		kΩ

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ELECTRICAL SPECIFICATIONS (continued)

POWER SUPPLY MONITOR

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VREF fail threshold		2.6	3.3	4.0	V
Hysteresis (VREF)			85		mV
EN input low voltage	|Iil| < 40 µA	0.8			V
EN input high voltage	|Iih| < 1 mA			2	V
$\overline{\text{WRPROT}}$ Vol	|Iol| < 1 mA			0.4	V
$\overline{\text{WRPROT}}$ leakage current				10	µA
$\overline{\text{WRPROT}}$ delay	SOUT = VREF to VREF + 0.6V			10	µs

MOSFET DRIVERS

SE3 Input impedance	To VREF	10	25		kΩ
OUTA, OUTC voltage swing |Io|<1 mA		0.7		VCC-1	V
OUTB, OUTD voltage swing |Io|<1 mA		1		VCC-1	V
VTH, Crossover separation threshold				2	V
Slew rate (OUTA, OUTB, OUTC, OUTD)	Cl<1000 pF	0.5	1.4		V/µs
Crossover time	300 mV step at ERR			6	µs
Output impedance (OUTA,B,C,D)			50		kΩ
Transconductance I(OUTA,B,C,D)/(ERR-VREF)			8		mA/V
Gain (-(SE1-VREF)/(ERR-VREF) or (SE3-VREF)/(ERR-VREF))		8.2	8.7	9.2	V/V
Offset current	R_S = 0.2Ω, R_F = R_{IN}, V_{IN}=VREF			20	mA
Retract motor voltage (SE1-SE3)	Vcc = 6V	0.7	1	1.3	V

APPLICATION INFORMATION

A typical SSI 32H6231 application is shown in Figure 2. The selection criteria for the external components shown are discussed below. Figure 2 shows the equivalent circuit and equations for the DC motor used in the following derivations. While the nomenclature chosen is for a rotating motor, the results are equally applicable to linear motors.

LOOP COMPENSATION

The transfer function of the SSI 32H6231 in the application of Figure 2 is shown in Figure 4(a). If the zero due to R_L and C_L in the loop compensation circuit is chosen to cancel the pole due to the motor inductance, L_m, then the transfer function can be simplified as shown in Figure 4(b), under the assumption that this pole and the pole due to the motor mechanical response are widely separated. C_L may then be chosen to set the desired open loop unity gain bandwidth.

$$C_L = \frac{68 \cdot R_s}{2 \cdot \pi \cdot R_F \cdot (R_m + R_s) \cdot BW}$$

where BW is the unity gain open loop bandwidth

$$R_L = \frac{L_m}{C_L \cdot (R_m + R_s)}$$

The closed loop response of the servo driver and motor combination, using the component values and simplifying assumptions given above, is given by:

$$\frac{i_m}{V_{in}}(s) = -\frac{1}{R_{in}} \cdot \frac{R_F}{4 \cdot R_s} \cdot \frac{1}{\left(1 + \frac{s}{2 \cdot \pi \cdot BW}\right)}$$

(This analysis neglects the pole due to the output impedance of the MOSFET drivers and the MOSFET gate capacitance, an effect that may be significant in some systems).

RF is chosen to be sufficiently large to avoid overloading A2 (R_F // R_V > 4 kΩ). The input resistor, R_{IN}, sets the conversion factor from servo controller output voltage to servo motor current. R_{IN} is chosen such that the servo controller internal voltages are scaled conveniently. The resistor R_{OS} is optional and cancels out the effect of the input bias current of A1.

$$R_{os} = R_{in} // R_F$$

The external components R_D and C_D have no effect on the motor dynamics, but may be used to improve the stability of the MOSFET drivers. The load represented by the motor, ZM, is given by:

At frequencies above $(R_s+R_m)/(2 \cdot \pi \cdot L_m)$ Hz, this load

$$ZM = (R_s + R_m)\left(1 + s\frac{L_m}{R_s + R_m}\right)\left(1 + \frac{K_m^2}{s \cdot J\theta \cdot (R_s + R_m)}\right)(\Omega)$$

becomes entirely inductive, which is undesireable. R_D and C_D may be used to add some parallel resistive loading at these frequencies.

H-BRIDGE MOSFET

The MOSFETs chosen for the H-bridge should have gate capacitances in the range of 500-1000 pF. The MOSFET input capacitance forms part of the compensation for the MOSFET drivers, so values below 500 pF may cause some driver instability. Excessive input capacitance will degrade the slew mode performance of the drivers.

When the motor voltage is changing polarity, the crossover protection circuits at outputs OUTA-OUTD ensure that the maximum MOSFET gate drive is less than 2V (the crossover separation threshold), as illustrated in Figure 4. The thresholds of the MOSFET devices chosen should be as large as possible to minimize conduction in this region. If the device thresholds are significantly less than the crossover separation threshold, the N and P channel devices in each leg of the H-bridge will conduct simultaneously, causing unnecessary power dissipation.

7

APPLICATION INFORMATION (continued)

POWER FAILURE OPERATION

The power supply for the SSI 32H6231, VCC, should be taken from the system 12V supply through a Schottky diode (maximum 0.5V drop at If = 3A) and connected to the disk drive spindle motor. If the system power fails, the IC will continue to operate as the spindle motor becomes a generator. The SSI 32H6231 can be commanded to perform a forced head retract, continuing to operate with VCC as low as 3.5V. The head retract mode will commence if VREF falls below 3.3V, or EN is false. Hysteresis on the low voltage threshold prevents the device from oscillating between operating modes when the power supply is marginal.

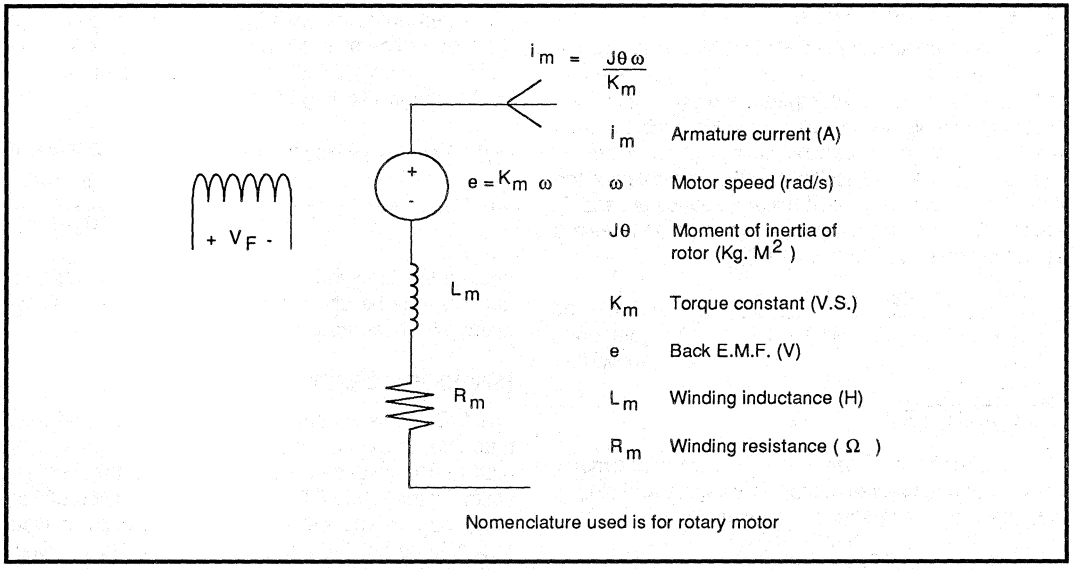

FIGURE 3: Equivalent Circuit for Fixed Field DC Motor

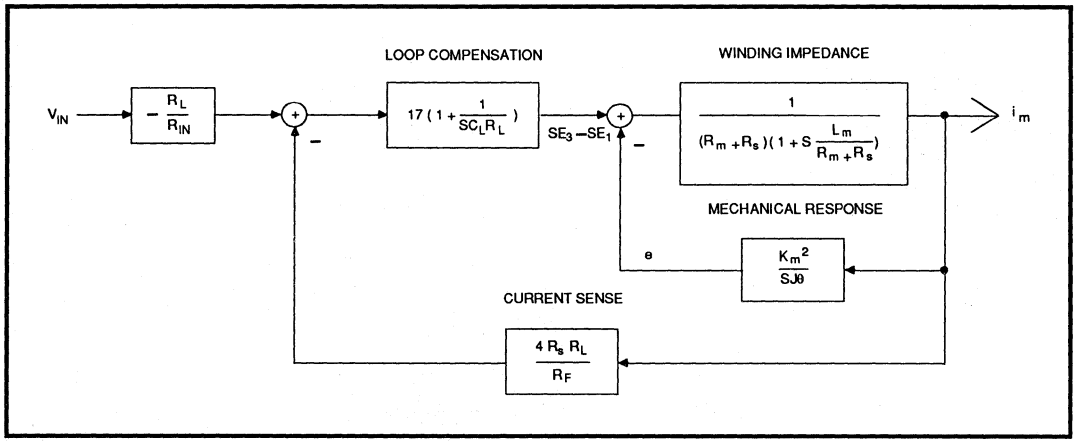

FIGURE 4A: Transfer Function of SSI 32H6231 in Typical Application with Fixed Field DC Motor

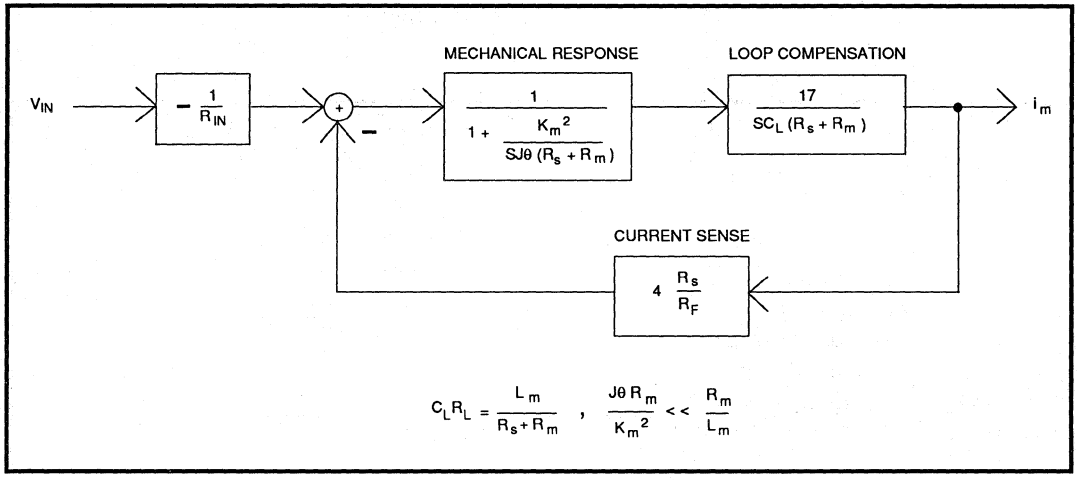

FIGURE 4B: Simplified Transfer Function of SSI 32H6231 in DC Motor Application

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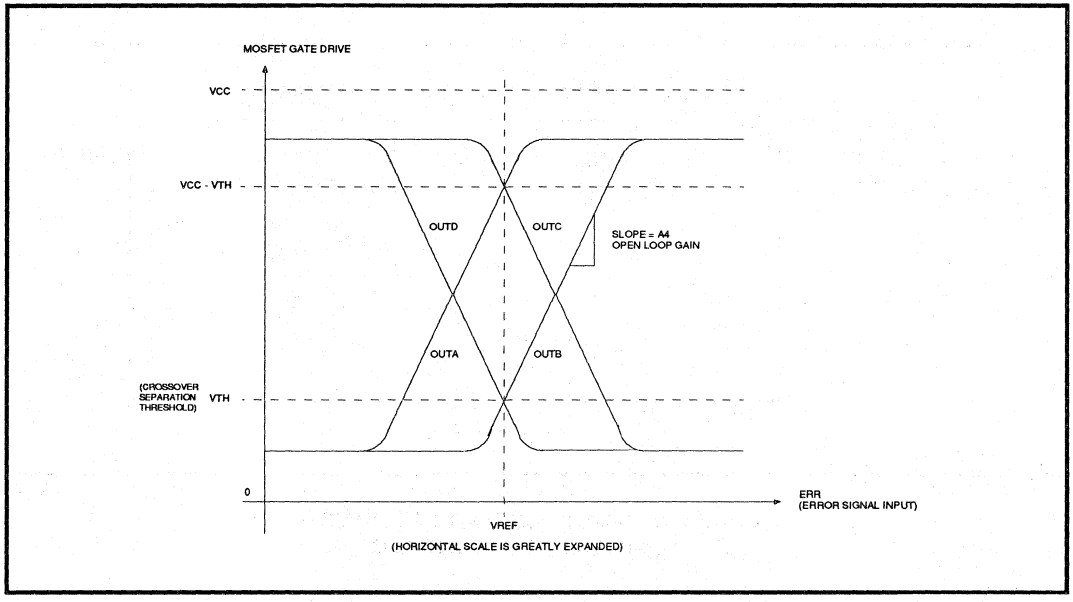


FIGURE 5: Crossover Protection

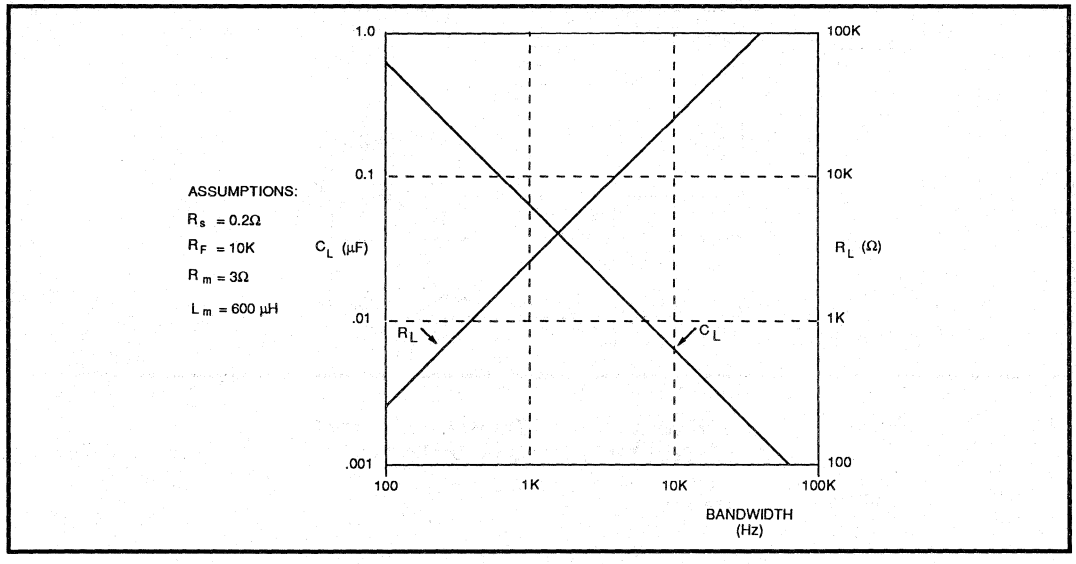
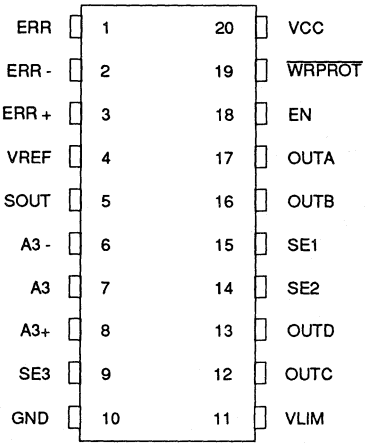


FIGURE 6: Typical Motor Driver Compensation

PACKAGE PIN DESIGNATIONS

(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



20-Lead SOV

7

ORDERING INFORMATION

PART DESCRIPTION	ORDER NUMBER	PACKAGE MARK
SSI 32H6231 20-Lead SOV	32H6231-CV	32H6231-CV

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914

Notes:

silicon systems®
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SSI 32H6240
Servo Motor Driver

Advance Information

December 1992

DESCRIPTION

The SSI 32H6240 Servo Motor Driver is a bipolar device intended for use in Winchester disk drive head positioning systems employing linear or rotary voice coil motors. When used in conjunction with a position controller, such as the SSI 32H6220 Servo Controllers, and a position reference, such as the SSI 32H567 Servo Demodulator, the device allows the construction of a high performance, dedicated surface head positioning system.

The SSI 32H6240 serves as a transconductance amplifier by driving 4 bipolar power transistors in an H–bridge configuration and performs motor current sensing by using an on-chip differential amplifier. In its linear tracking mode, class B operation is guaranteed by crossover protection circuitry, which ensures that only one transistor in each leg of the H-bridge is active. Automatic head retraction and spindle braking may be initiated by a low voltage condition or upon external command.

The SSI 32H6240 is implemented in an advanced bipolar process and dissipates less than (240 mW) from a 12V supply. The SSI 32H6240 is available in a 28-pin PLCC.

FEATURES

- **Predriver for linear and rotary voice coil motors**
- **Interfaces directly to Bipolar H-Bridge motor driver**
- **Class B linear mode and constant velocity retract mode**
- **Power transistor disable function**
- **Precision differential amplifier for motor current sensing**
- **On-chip precision power fail detect**
- **Automatic head retract and spindle braking signal on power failure**
- **External digital enable**
- **Servo loop parameters programmed with external components**
- **Advanced bipolar IC requires under (240 mW) from 12V supply**
- **Available in 28-pin PLCC packaging**
- **+5V, +12V operation**

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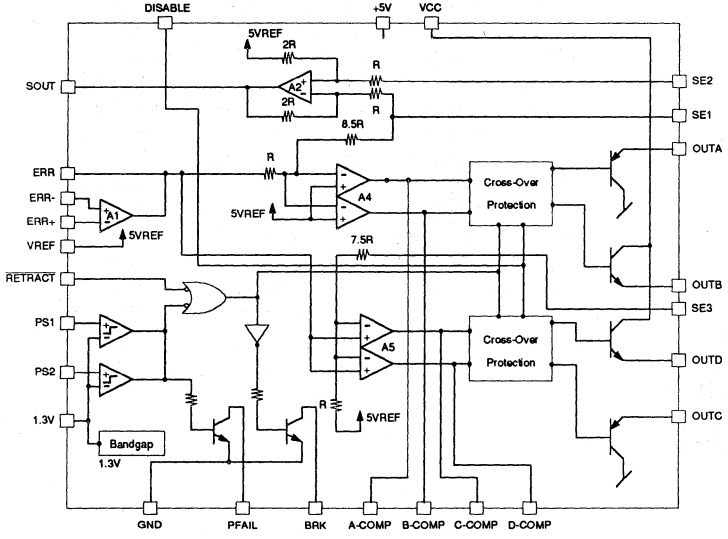
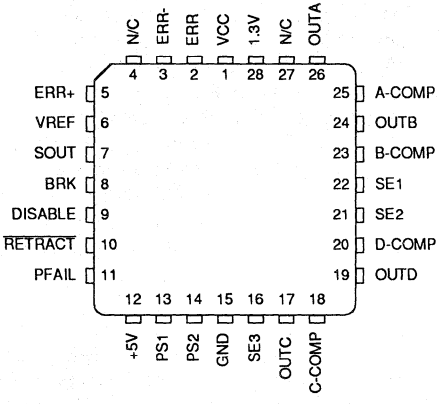
BLOCK DIAGRAM



PIN DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

FUNCTIONAL DESCRIPTION

(Refer to block diagram and typical application Fig.2)

There are three modes of operation of the SSI 32H6240: Disable, Retract, and Linear. The circuit mode is controlled by the DISABLE , $\overline{\text{RETRACT}}$, PS1, and PS2 pins.

DISABLE mode turns off the output drivers. OUTA and OUTC are pulled to VCC through internal 1.5 kΩ resistors. OUTB and OUTD are pulled to GND through internal 1.5 kΩ resistors. Disable mode does not override Retract mode.

RETRACT mode turns off OUTB and OUTC. OUTD is turned on. OUTA is turned on in a special manner to force 1V at SE1. Retract mode does override Disable mode.

POWER FAIL mode occurs when either PS1 or PS2 fall below 1.3V. Power fail overrides Retract and Disable inputs and forces the chip into RETRACT mode.

When the $\overline{\text{RETRACT}}$ pin is pulled low the SSI 32H6240 will go into retract mode. The BRK pin will go high. When the DISABLE pin is pulled high it will cause all 4 bridge power transistors to turn off. PFAIL and BRK will remain low if PS1, PS2, and $\overline{\text{RETRACT}}$ pins do not change.

During linear mode operation an acceleration signal from the servo controller is applied through amplifier A1. Amplifier A1's three connections are available for connection to external loop compensation components. The ERR signal drives two precision amplifiers, each with a gain of 8.5. The first of these amplifiers is inverting, and is formed from opamp A4, an on-chip resistor divider, and an off-chip complementary Bipolar Power Transistor pair. The second amplifier is non-inverting and is formed in a similar manner from opamp A5. Feedback from external transistor's collectors on sense inputs SE1 and SE3 allows the amplifier's gains to be precisely set. The voice coil motor and a series current sense resistor are connected between SE1 and SE3. The output of the amplifiers will provide the base current for the external H-Bridge Bipolar Power Transistors. The chip is designed to work with external transistors with a minimum Beta of 40 and minimum f_T of 40 MHz. The base bias resistors for the external bridge transistors are internal to the IC.

Cross over protection circuitry between the outputs of A4 and A5 and the external power transistors ensure Class B operation by allowing only one transistor in each leg of the H-bridge to be in conduction. The crossover circuitry can also disable all Power Transistors simultaneously (to limit motor current or velocity) or apply a constant voltage across the motor (to retract the heads at a constant velocity.)

Motor current is sensed by a small resistor placed in series with the motor. The voltage drop across this resistor is amplified by a differential amplifier with a gain of 2 (A2 and associated resistors), whose inputs are SE1 and SE2. The resulting output voltage, SOUT, is proportional to motor current, and hence acceleration. This signal is externally fed back to A1 so that the signal ERR represents the difference between the desired acceleration (from the servo controller) and the actual motor acceleration. The total output offset current (Vin = Vref, Rsense = 0.5 Ω) is less than 5.5 mA.

The SSI 32H6240 has low voltage monitor circuitry that will detect a decrease in the voltage at PS1 and PS2 pins. The +5V and +12V power supplies are divided down by external resistors and then compared to an internal 1.25V ±5% reference. The power supply pin, VCC, should be connected to the disk drive's spindle motor so that its stored rotational energy may be used to hold up VCC briefly during a power failure. When a low voltage condition is detected on either the PS1 or PS2 pins the BIPOLAR drivers switch from linear operation to retract mode. In this mode a constant voltage is applied across the motor which will cause the heads to move at a constant speed. A mechanical stop must be provided for the heads when they reach a safe location. External current limiting circuitry is required for both the linear and retract modes of operation. An open collector output, PFAIL, which is low in the linear mode, will go high to indicate a power failure. This signal is gated with the $\overline{\text{RETRACT}}$ input signal to force the chip into the Retract mode during power failure and to signal a BRK spindle. A BRK spindle is signaled by forcing a High level on the BRK open collector output which is normally low in the Linear mode. The BRK pin is provided for spindle motor braking. An external RC delay may be used to defer braking until the heads are retracted.

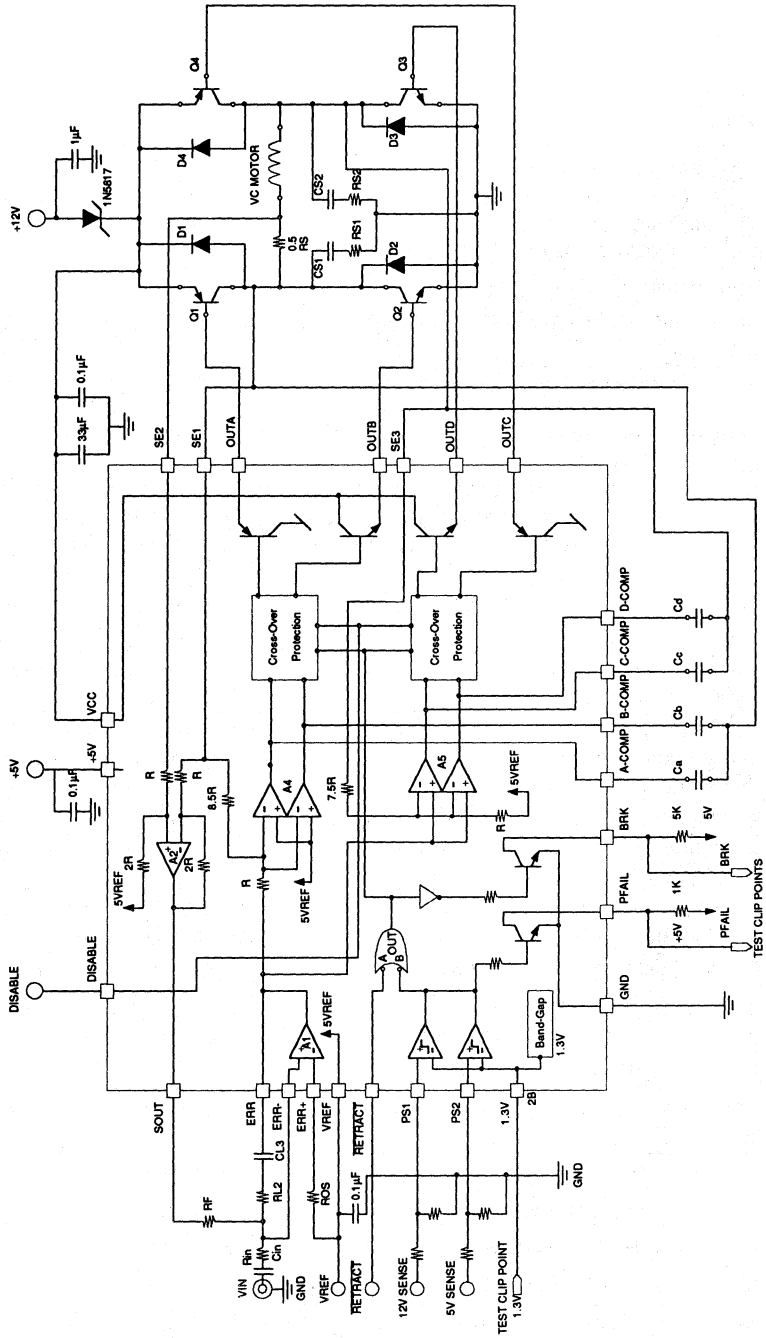


FIGURE 2: SSI 32H6240 Typical Application

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PIN DESCRIPTION

POWER

NAME	TYPE	DESCRIPTION
VCC	-	POSITIVE SUPPLY - Usually taken from spindle motor supply. Spindle motor stored energy permits head retraction during power failure. If either a "Power Failure" or a "Retract" is asserted a forced head retraction occurs. Usually supplied through a power Schottky diode from Spindle Motor Supply.
+5V	I	5-volt power supply
VREF	I	REFERENCE VOLTAGE - 5.0V input. All analog signals are referenced to this input.
GND	-	GROUND

CONTROL

NAME	TYPE	DESCRIPTION
ERR	O	POSITION ERROR- Loop compensation amplifier output. This signal is amplified by the BIPOLAR drivers and applied to the motor by an external BIPOLAR H-bridge, as follows: SE3-SE1 = 17 (ERR-VREF)
ERR-	I	POSITION ERROR INVERTING INPUT - Inverting input to the loop compensation amplifier.
ERR+	I	POSITION ERROR NON-INVERTING INPUT - Non-inverting input to the loop compensation amplifier.
SOUT	O	MOTOR CURRENT SENSE OUTPUT - This output provides a voltage proportional to the voltage drop across the external current sense resistor, as follows: SOUT-VREF=4 (SE2-SE1)
BRK	O	BRAKE OUTPUT - Active high, open collector output which may be used to enable an external spindle motor braking transistor upon power failure. External resistor may be tied to +5 or +12V.
DISABLE	I	DISABLE DRIVERS INPUT – Logic level input. An input high level will cause all 4 bridge BIPOLAR Power Devices to turn off. DISABLE does not override retract.
$\overline{\text{RETRACT}}$	I	$\overline{\text{RETRACT}}$ INPUT – Logic level low will assert a forced head retraction. RETRACT will override DISABLE. $\overline{\text{RETRACT}}$ will continue to work at VCC=3.5V.
PS1	I	POWER SENSE 1 – 12V sense input to power fail comparator.
PS2	I	POWER SENSE 2 – 5V sense input to power fail comparator.
PFAIL	O	POWER FAIL – Power fail indicator open collector output. Floats if either supply goes below threshold.
1.3V	O	INTERNAL REFERENCE MONITOR - Used for testing purposes only.
A-COMP	O	AMPLIFIER A COMPENSATION - Compensation capacitor pin
B-COMP	O	AMPLIFIER B COMPENSATION - Compensation capacitor pin
C-COMP	O	AMPLIFIER C COMPENSATION - Compensation capacitor pin
D-COMP	O	AMPLIFER D COMPENSATION - Compensation capacitor pin

CONTROL (Continued)

NAME	TYPE	DESCRIPTION
SE2	I	MOTOR CURRENT SENSE INPUT - Non-inverting input to the current sense differential amplifier. It should be connected to one side of an external current sensing resistor in series with the motor. The inverting input of the differential amplifier is connected internally to SE1.

BIPOLAR DRIVE

SE3	I	MOTOR VOLTAGE SENSE INPUT - This input provides feedback to the non-inverting BIPOLAR driver amplifier. It is connected to one side of the motor. The gain to this point is: SE3-VREF = 8.5 (ERR-VREF)
SE1	I	MOTOR VOLTAGE SENSE INPUT - This input provides feedback to the inverting BIPOLAR driver amplifier. It is connected to the current sensing resistor which is in series with the motor. The gain to this point is: SE1 - VREF = -8.5 (ERR-VREF)
OUTA	O	PNP DRIVE (INVERTING) - Drive signal for a PNP power transistor connected between the current sense resistor and VCC. The PNP collector is also connected to SE1. Crossover protection circuitry ensures that the PNP and NPN devices driven by OUTA and OUTB are never simultaneously enabled.
OUTB	O	NPN DRIVE (INVERTING) - Drive signal for an NPN power transistor connected between the current sense resistor and GND. This NPN collector is also connected to SE1.
OUTC	O	PNP DRIVE (NON-INVERTING) - Drive signal for a PNP power transistor connected between one side of the motor and VCC. This PNP collector is connected to SE3. Crossover protection circuitry ensures that the PNP and NPN devices driven by OUTC and OUTD are never simultaneously enabled.
OUTD	O	NPN DRIVE (NON-INVERTING) - Drive signal for an NPN power transistor connected between one side of the motor and GND. This NPN collector is connected to SE3. Crossover protection circuitry ensures that the PNP and NPN devices driven by OUTC and OUTD are never simultaneously enabled.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

(Maximum limits indicates where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC operating characteristics.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VCC		0		16	V
VREF		0		10	V
+5V		0		7	V
SE1, SE2, SE3		-1.5		15	V
DISABLE, $\overline{\text{RETRACT}}$		-.3		+5V + .3	V
All other pins		-.3		VCC + .3	V
Storage temperature		-45		165	°C
Solder temperature	10 sec duration			260	°C

RECOMMENDED OPERATION CONDITIONS (Unless otherwise noted, the following conditions are valid throughout this document.)

VCC	Normal Mode	9	12	13.2	V
	Retract Mode	3.5V		13.2	V
+5V		4.5	5	5.5	V
VREF		4.5	5	5.5	V
Operating temperature		0		70	°C

DC CHARACTERISTICS

ICC, VCC current			13	20	mA
I5V, +5V Current			0.6	1	mA
IREF, VREF current			300		µA

A1, LOOP COMPENSATION AMPLIFIER

Input bias current				500	nA
Input offset voltage				3	mV
Voltage swing	About VREF		2		V
Common mode range	About VREF	±1			V
Load resistance	To VREF	4			kΩ
Gain			80		dB
Unity gain bandwidth			1		MHz
CMRR	f<20 kHz		60		dB
PSRR	f<20 kHz		60		dB

A2, CURRENT SENSE AMPLIFIER

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input impedance	SE1 to SE2	7.0	10		kΩ
Input offset voltage	SE1 = SE2 = VREF			2	mV
Output voltage swing		VREF-4		VCC-1.2	V
Common mode range		0		VCC-0.2	V
Load Resistance	To VREF	4			kΩ
Output impedance	f<40 kHz			20	Ω
Gain (SOUT-VREF)/(SE1-SE2)	VSE2 = VREF	1.95	2	2.05	V/V
Unity gain bandwidth			1		MHz
CMRR	f<20 kHz		52		dB
PSRR	f<20 kHz		60		dB

POWER SUPPLY MONITOR

1.3V pin voltage	1.3V pin open	1.18	1.25	1.31	V
PS1 threshold			1.25		V
PS2 threshold			1.25		V
PS1, PS2 Hysteresis			20		mV
PS1, PS2 Input Bias Current	PS1, PS2 = 1.3V		1		µA
PFAIL VOL	Linear mode IOC = 1mA			0.4	V
BRK VOL	Linear mode IOC = 1mA			0.4	V
PFAIL IOH	Retract mode VOH = 12V			10	µA
BRK IOH	Retract mode VOH = 12V			10	µA
DISABLE IIL	VIL = 0.8V		2	20	µA
$\overline{\text{RETRACT}}$ IIL	VIL = 0.8V		2	10	µA
DISABLE IIH	VIH = 2.4		1	10	µA
$\overline{\text{RETRACT}}$ IIH	VIH = 2.4		1	10	µA
DISABLE and $\overline{\text{RETRACT}}$ Threshold Voltage			1.4		V

BIPOLAR DRIVERS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SE3 Input Impedance	To VREF	10	25		kΩ
A Comp, C Comp Voltage Swing	w/ External Trans.	VCC - 1.4		VCC - .7	V
B comp, D Comp Voltage Swing	w/ External Trans.	0.7		1.4	V
Output Impedance A, B, C, D Comp	Output Off, No External Trans.		75		kΩ
Transconductance I (A, B, C, D Comp)/(ERR-VREF)			6		mA/V
Gain -(SE1-VREF)/(ERR-VREF) or (SE3-VREF)/(ERR-VREF)	Includes External Trans.	8	8.5	9	V/V
Offset Current (A2 Vos)	Rs = 0.5Ω Rf = Rin Vin = Vref		3.5		mA
Retract Motor Voltage (SE1-SE3)		0.7	1.3	1.7	V
Out B, Out D Source Current	Vout = 0.8V	20			mA
Out B, Out D Current Limit	Vcc = 10.8V, Out B, D = 0.8V Vcc = 12.0V, Out B, D = 0.8V	20 23	25 27	30 33	mA mA
Out A, Out C Sink Current	Vout = 11.2V	20			mA
B and D Output NPN Output Transistor Beta	Ic = 20mA Vce = 10V		20		V/V
A and C Output PNP Output Transistor Beta	Ic = 20mA Vce = 10V		10		V/V

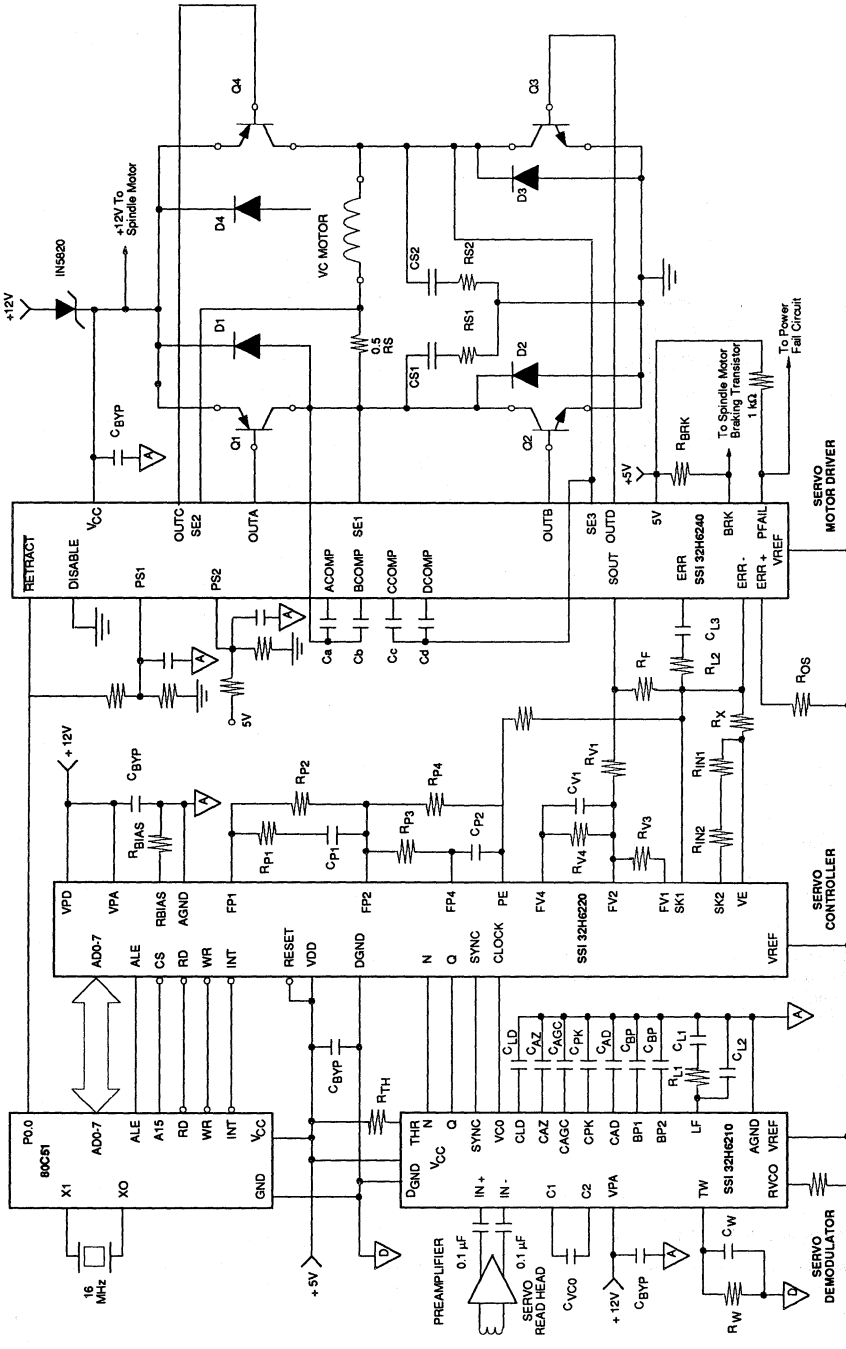

FIGURE 3: Complete Example of Servo Path Electronics using the SSI 32H6210/6220/6240 Chip Set

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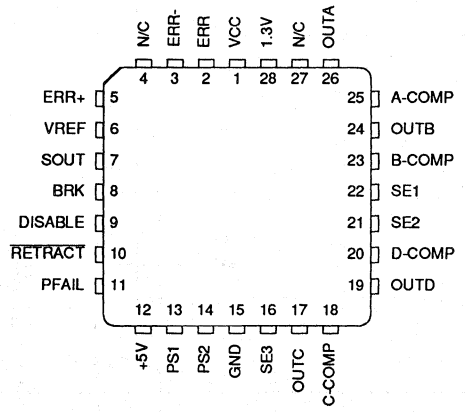
SSI 32H6240
Servo Motor Driver

PACKAGE PIN DESIGNATIONS
(TOP VIEW)

CAUTION: Use handling procedures necessary for a static sensitive component.



28-Pin PLCC

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX: (714) 573-6914

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SSI 32H6510
5V Servo Driver

Preliminary Data

January 1993

DESCRIPTION

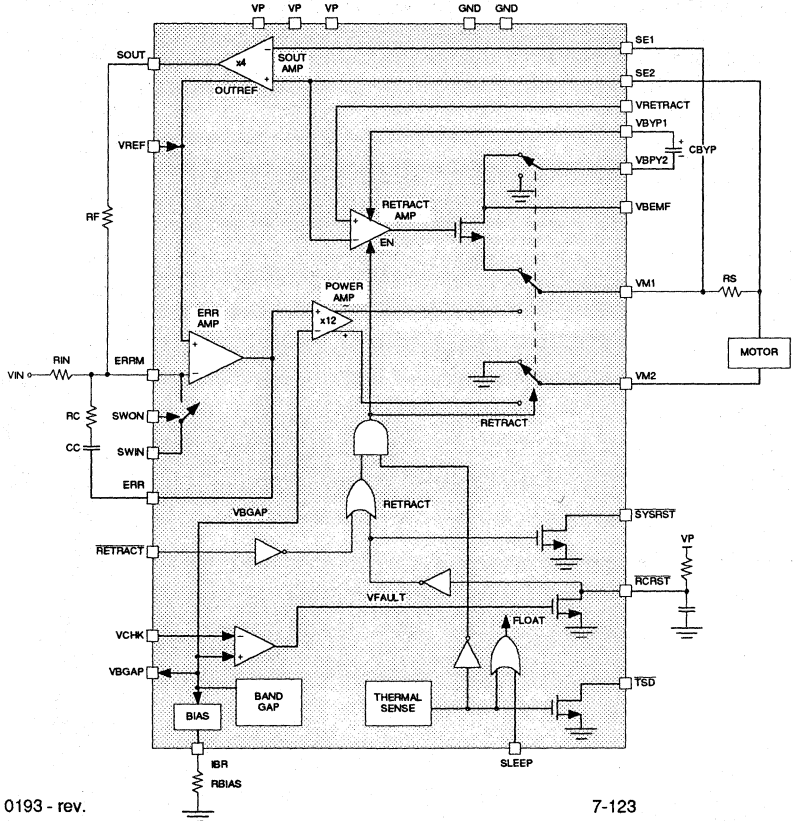
The SSI 32H6510 is a fully integrated power amplifier for use in disk drive head positioning systems employing linear or rotary voice coil motors. It is intended for use in 5V systems and is capable of generating ±1 Amp motor currents. The part is internally thermal overload protected.

The SSI 32H6510 is a power transconductance amplifier for use in driving voice coil type servo motors (VCMs). The SSI 32H6510 has two primary modes of operation, normal (or linear) and retract. The retract mode is activated by a power supply failure or when $\overline{\text{RETRACT}}$ is asserted. Otherwise the device operates in linear mode.

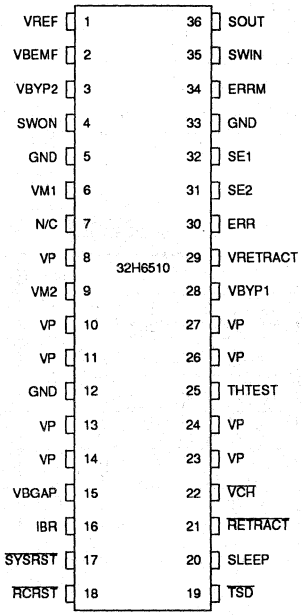
FEATURES

- **36-pin SO package**
- **Internal 1A power devices**
- **NMOS output stage**
- **Total on resistance less than 1.3Ω at 500 mA**
- **Thermal overload protection**
- **No deadband, low distortion, class B output**
- **Low power sleep mode**
- **Gain select switch optimizes performance with 8-bit DACs**
- **Built in retract circuitry**
- **Power fault detection**

BLOCK DIAGRAM



PIN DIAGRAM



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CAUTION: Use handling procedures necessary for a static sensitive component.

DESCRIPTION (continued)

The SSI 32H6510 consists of five major blocks: SOUT amplifier, ERR amplifier, retract amplifier, power amplifier, and control circuitry. These parts are each described in this section. External components needed for proper operation of the SSI 32H6510 are also described.

SOUT AMPLIFIER

This amplifier generates a voltage at SOUT that is proportional to positioner current. It does this by sensing the voltage across Rs, amplifying it, and referencing the result to VREF. Since the common mode voltage on Rs can range over the full power supply, while the differential voltage is a few millivolts, the SOUT amplifier is designed to have very high input common mode rejection, and very low input offset.

ERR AMPLIFIER

The ERR amplifier is a high gain op amp. Due to the fixed gain of the power amp, ERR is proportional to the VCM voltage. The negative input of this amplifier is the system summing junction--currents proportional to the desired VCM current, the measured VCM current, and the VCM voltage are summed here.

POWER AMPLIFIER

The power amplifier is a fixed gain voltage amplifier with differential inputs and outputs. Its input is the differential voltage between ERR and VBGAP. Its output drives the VCM directly.

RETRACT AMPLIFIER

When a voltage fault is sensed, or when $\overline{\text{RETRACT}}$ is asserted, the SSI 32H6510 enters retract mode. In this mode, it is assumed that no current is available from VP (VP may actually be at GND potential). Thus power for this mode comes from VBEMF, the rectified spindle back EMF voltage, and from VBYP1, a voltage generated from the external storage capacitor CBYP. The retract amplifier is powered by VBYP1. It senses the voltage at VRETRACT and raises VM1 to be equal to VRETRACT. The drain of the source follower is VBEMF.

CONTROL CIRCUITRY

The control circuitry consists of voltage monitoring circuitry, a thermal overload circuit, and control logic. The inputs to the control circuitry are the external signals $\overline{\text{RETRACT}}$, VCHK, and SLEEP, along with internal signal from the thermal overload detector (visible externally on $\overline{\text{TSD}}$). Table 1 describes the behavior of the part in response to these inputs.

TABLE 1: IC Mode Selection

INPUT				CHIP FUNCTION		
SLEEP	$\overline{\text{RETRACT}}$	VCHK>VBGAP	$\overline{\text{TSD}}$	BRIDGE	RETRACT	$\overline{\text{SYSRST}}$
X	X	0	0	Off	Off	0
X	X	0	1	Off	On	0
X	X	1	0	Off	Off	1
X	0	1	1	Off	On	1
0	1	1	1	On	Off	1
1	1	1	1	Off	Off	1

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
VP	Power	The positive power supply. The VP pins are thermally connected to the die and provide a low thermal resistance path to the circuit board. All VP pins should be shorted together.
GND	Power	The negative power supply. All GND pins should be shorted together.
SWON	Dig In	Turns on the switch between ERRM and SWIN.
SWIN	An In	One side of an analog switch connected to ERRM.
SOUT	An Out	The current sense amplifier output. SOUT is referenced to VREF.
ERR	An Out	The error amplifier output. ERR is used to provide compensation to the transconductance loop. ERR is referenced to VBGAP.
ERRM	An In	The error amplifier negative input.
VREF	An In	The reference voltage for the error amplifier and the current sense amplifier.
$\overline{\text{RETRACT}}$	Dig In	When low, forces a retract.
THTEST	Dig In	Test input.
VCHK	An In	Comparator input for power supply monitoring. When VCHK is below VBGAP, an internal voltage fault is generated.
VBGAP	An Out	An internal voltage reference for use with the power supply monitor comparator.
IBR	An Out	A resistor is tied from this pin to ground to establish the bias current for internal circuitry.
SLEEP	Dig In	Turns off the output drivers. Does not override the retract function when a voltage fault occurs. Powers down all but the voltage monitor and retract circuitry.
$\overline{\text{TSD}}$	O/C Out	Thermal Shut Down. When low, this open collector output indicates that the junction temperature has exceeded the recommended operating range and that the part is in thermal shutdown.
$\overline{\text{RCRST}}$	O/C Out	This pin serves the dual purpose of providing power-on-reset and stretching short VFAULT pulses to a width suitable for the host microcontroller. An external RC network sets the minimum width of any $\overline{\text{SYSRST}}$ pulse.
$\overline{\text{SYSRST}}$	O/C Out	When low, this open collector output indicates that an internal voltage fault has occurred.
VRETRACT	An In	The retract voltage. Supplied externally by a diode reference.
VBYP1	An In	The bypassed power supply. An external capacitor is connected to this node to store charge for use by the retract circuitry.
VBYP2	An In	The other side of the bypass capacitor is connected here.
VBEMF	An In	Rectified spindle back emf voltage. This input provides current to the internal retract power FET.

PIN DESCRIPTION (continued)

NAME	TYPE	DESCRIPTION
VM2	An Out	One side of the voice coil motor.
VM1	An Out	The other side of the voice coil motor and sense resistor combination.
SE1, SE2	An In	The sense voltages around the sense resistor.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation of the part outside these limits may result in degradation or failure of the device.

PARAMETER	RATING	UNITS
Power Supply, VP	7	V
Voltage on any pin		
VBEMF, VBYP1, VBYP2, $\overline{\text{SYSRST}}$, $\overline{\text{RCRST}}$	-0.3 to 16	V
VM1, VM2, SE1, SE2	-0.3 to 12	V
All others	-0.3 to VP+.3	V
Storage Temperature	-45 to 165	°C
Solder Temperature (10 sec duration)	260	°C
Output Current - I(VM1), I(VM2)	2	Amp
Junction Temperature	150	°C

RECOMMENDED OPERATING CONDITIONS

The performance specifications for this part apply only when the operating environment is within this specified range.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Power Supply, VP		4.75		5.25	V
Junction Temperature		0		125	°C
Output Current - I(VM1), I(VM2)				1.0	Amp
VBEMF		1.0		14	V
VREF		0.5		VP-2	V
RF		10			kΩ
RC		10			kΩ
RBIAS		21.5		22.5	kΩ
VBYP1 - Retract Mode		3		14	V

PERFORMANCE SPECIFICATIONS

DESCRIPTION	CONDITIONS	MIN	NOM	MAX	UNITS
VP Supply Current:					
Normal operation, Imotor = 0				15	mA
Sleep mode				2	mA
SOUT gain		3.9		4.1	V/V
SOUT input offset (SOUT = VREF)		-3		3	mV
SOUT output swing		0.15		VP-1	V
ERRM input offset (ERR = ERRM)		-10		10	mV
ERR output swing		1.6		3.25	V
GAIN (VM1-VM2)/(ERR-VBGAP)		11		13	V/V
VBGAP		2.13		2.37	V
VCHK offset		-15		15	mV
Retract offset					
VRETRACT = 0.5V		-50		50	mV
VRETRACT input impedance		500			kΩ
Output voltage drop: VP-|VM1-VM2|					
Imotor = ± 0.5A, Tj = 25°C				0.65	V
Imotor = ± 0.1A, Tj = 25°C				0.15	V
Thermal shutdown temperature		120		140	°C
Thermal shutdown hysteresis		3		7	°C
Crossover time					
Imotor = 10mA p 1000 Hz				45	µs
Crossover distortion					
Imotor = 10mA p 1000 Hz				2	%THD
Digital open collector output, sink current:					
$\overline{SYSRST}$, $\overline{RC\_RST}$, $\overline{TSD}$					
Vol = 0.4V		1.6			mA
SWIN on resistance				250	Ω

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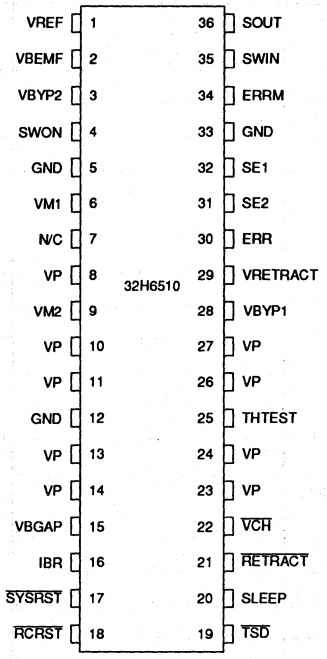
SSI 32H6510
5V Servo Driver

PACKAGE PIN DESIGNATIONS
(Top View)



36-Lead SOM

ORDERING INFORMATION

PART DESCRIPTION	ORDER NUMBER	PACKAGE MARK
SSI 32H6510 36-Lead SOM	32H6510	32H6510

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914

silicon systems®
A TDK Group Company

SSI 32H6520
Embedded Servo Controller

Preliminary Data

December 1993

DESCRIPTION

The 32H6520 Embedded Servo Controller is a CMOS monolithic integrated circuit housed in a 48-pin TQFP and operates on a single +5.0 volt supply. It provides one 10-bit A/D converter with 2.5 µs conversion time, and two 10-bit D/A converters with 2.5 µs digital delay as well as Motorola/Intel compatible bus interface (Motel) to commonly used microcontrollers such as 80C196 and 68HC11. In addition, it includes bus interface logic to support DSP-based, such as TMS320XX, digital servo applications.

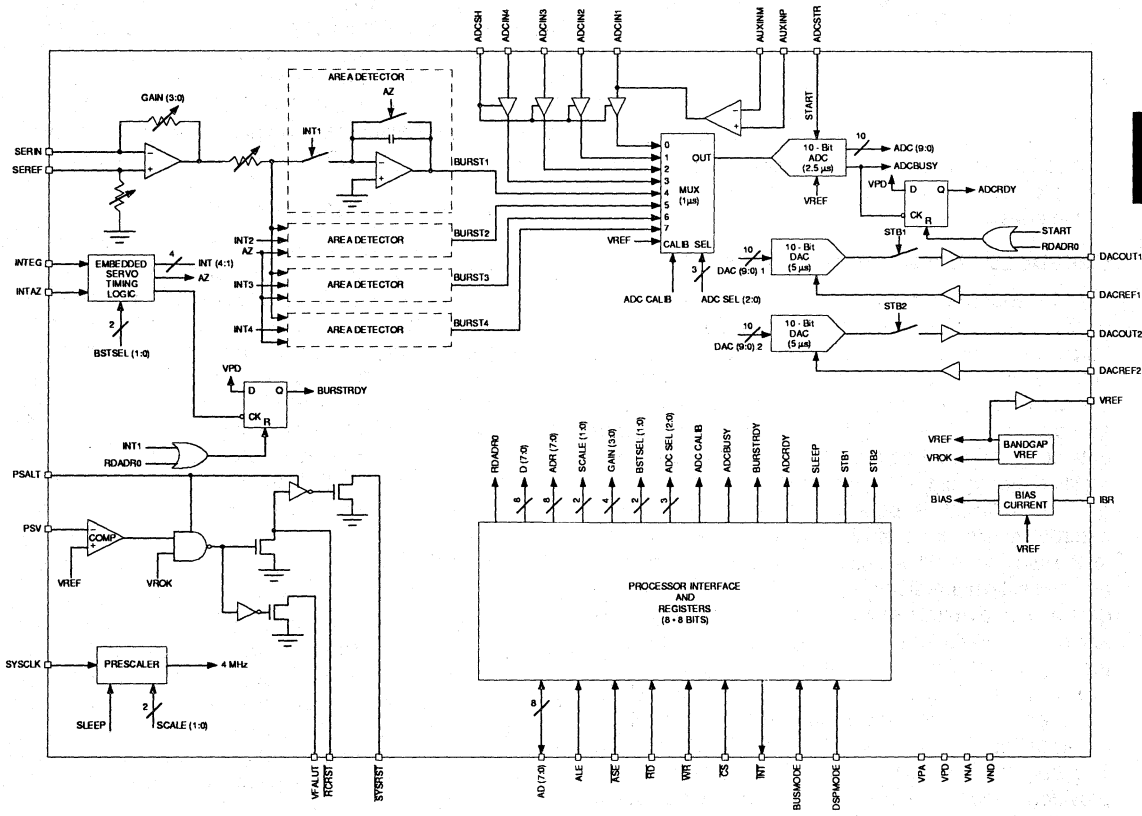
FEATURES

Embedded Servo Burst Processor

- Servo control for Winchester disk drives with embedded servo sectors
- For use in µP/DSP-based digital servo applications
- Pulse area detects and S/H circuits for up to four embedded servo bursts
- Programmable gain adjustment from -2.8 dB to 3.2 dB

(continued)

BLOCK DIAGRAM



FEATURES (continued)

Data Acquisition and Microprocessor/DSP Bus Interface

- Motel bus interface compatible with 80C196 and 68HC11
- Bus interface logic to support DSP-based digital servo applications
- Eight internal registers and address decoding
- Two 10-bit D/A converters with 2.5 µs digital delay
- One 8-channel 10-bit A/D converter with 2.5 µs conversion time

General Functions

- Voltage fault detection
- Low power CMOS design
- 48-pin TQFP

FUNCTIONAL DESCRIPTION

The 32H6520 can be divided into four major sections: embedded servo burst processor, voltage fault detector/logic, data acquisition and microprocessor/DSP bus interface.

EMBEDDED SERVO BURST PROCESSOR

The embedded servo burst processor extracts the head position error information from the embedded servo bursts using an area detection technique. The area detection technique provides improved noise immunity over peak detector. The embedded servo burst processor contains a differential/gain amplifier, four pulse area detectors and required timing logic. First, a full wave-rectified analog signal from a read data channel, such as SSI 32P4620, is provided at SERIN through an external resistor equal to Rint and a DC reference level for the full wave-rectified analog signal at SEREF through another external resistor equal to Rint. To accommodate a wide dynamic range of servo burst amplitudes and process variations of the integration capacitor Cint, the differential signal between SERIN and SEREF is scaled under µP control. The gain of the differential amplifier ranges from -2.8 dB to 3.2 dB in a step of 0.4 dB, as defined in the SERVO GAIN CONTROL register. The output of the differential/gain amplifier is then provided to four pulse area detectors whose output are proportional to the area above the DC reference level during time intervals defined by an external timing source through INTEG. Each area detector applies an on-chip capacitor Cint equal to 10 pF to integrate the incoming pulses during the integration interval and then hold the integrated voltage outputs thereafter. Note that the max ±20% tolerance of on-chip capacitors can be calibrated out by adjusting the gain of the preceding amplifier. Finally, the integrated voltage outputs at BURST1, BURST2, BURST3 and BURST4 are provided to a 10–bit A/D converter under µP control and will be discharged during a time interval defined by an external timing source through INTAZ. For proper operatons, the time interval defined by the INTAZ must be no less than 0.5 µs and be applied only once per servo frame preceding the integration pulses defined by the INTEG.

Limited timing logic is included to generate all the timing signals required for the embedded servo burst processor, per figure 1. These timing signals control the integration, sample/hold of the pulse area detectors. The number of embedded servo bursts supported by this circuit are two, three or four. The BSTSEL0 and BSTSEL1 bits in the SERVO CONTROL register configure the internal timing logic to generate a servo burst ready interrupt after the last servo burst is captured.

VOLTAGE FAULT DETECTOR/LOGIC

The voltage fault detector monitors the power supply applied at PSV through an external resistor divider, which defines the trigger level for power supply failure. An open-drain output VFAULT is pulled HIGH by an external resistor when a power supply failure is sensed by the PSV comparator. The user-defined trigger level for voltage failure is applied at PSV. Another open-drain output, opposite logic polarity as the pin VFAULT and with an additional RC delay, is provided at $\overline{\text{SYSRST}}$. The amount of $\overline{\text{SYSRST}}$ delay is determined by an external RC connected to the pin, $\overline{\text{RCRST}}$.

DATA ACQUISITION

The A/D converter is multiplexed to eight different analog inputs by programming the ADC SEL0, ADC SEL1, and ADC SEL2 bits in the ADC ADDRESS register by the µP. The eight analog inputs multiplexed to the A/D converter are four embedded servo processor outputs at BURST1, BURST2, BURST3 and BURST4 and four external analog inputs through four T/H amplifiers. These T/H amplifiers sample external

DATA ACQUISITION (continued)

analog inputs during the time interval defined by an external timing source applied at ADCSH. If the sampling of four external analog inputs is not necessarily synchronized, ADCSH must be tied to HIGH. The A/D conversions on these external analog inputs are always referenced to the internal voltage reference at 2.23 volts. An operational amplifier with uncommitted inputs is provided to implement a level shifting function for the external analog input applied to AUXINP. The output of the operational amplifier is tied to ADCIN1.

The A/D converter starts to acquire a new analog input whenever the conversion is completed. A minimum of 1 µs is required to acquire an analog input to the A/D converter. Actual conversion is started by reading the A/D MSB register or by an external timing source applied to ADCSTR. The A/D address lines ADC SEL0, ADC SEL1, and ADC SEL2 will be incremented by one after the A/D conversion is started. The automatic increment of the address lines is employed to eliminate repetitive write operations by the µP to the ADC ADDRESS register required for converting the consecutive analog inputs.

The A/D converter runs synchronously with the internal 4 MHz clock which is used for various circuits on the 32H6520 and divided down from the system clock SYSCLK by a prescaler. Therefore there would be a maximum of 0.25 µs of latency between a conversion request and the actual start of the conversion. The output is coded in 2's complement.

Similarly, the D/A converters run synchronously with the internal 2 MHz clock and the conversion is started by writing to the corresponding D/A input register. The output of the first D/A converter is referenced to an external analog input, DACREF1 and the output of the second D/A converter is referenced to an external analog input, DACREF2. In the "normal" mode when STBEN1 (STBEN2) bit in the ADC ADDRESS register is reset, the D/A output will be automatically applied to DACOUT1 (DACOUT2) during the conversion. In the "strobe" mode, the D/A output will be applied to DACOUT1 (DACOUT2) at the falling edge of $\overline{RD}$ for a read to the corresponding D/A MSB DATA register.

MICROPROCESSOR/DSP BUS INTERFACE

The 32H6520 is provided with Motorola/Intel compatible bus interface for a direct connection to popular microcontrollers such as 80C196 and 68HC11. It also contains logic to interface with TMS320XX for DSP-based servo applications. Bus control signals ALE, $\overline{RD}$, $\overline{WR}$ and BUSMODE are interpreted differently, as described in table 1, based upon the type of processors being used. When the 32H6520 is interfaced with TMS320XX, the pin DSPMODE must be tied to HIGH and the pin BUSMODE is redefined as XFER/$\overline{SEL}$. The pin BUSMODE must be tied to HIGH for an Intel bus interface and LOW for a Motorola bus interface. The $\overline{ASE}$ pin gates the ALE/AS input and can be used to shut off the ALE/AS to minimize noise on the chip when the µP interface is not active. The $\overline{CS}$ pin performs a similar function on the rest of the µP bus inputs. The timing diagrams for different processors are depicted in Figures 2, 3 and 4.

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TABLE 1: Microprocessor/DSP Bus Interface

32H6520	Intel	Motorola	TMS320XX
DSPMODE	LOW	LOW	HIGH
BUSMODE	HIGH	LOW	XFER/$\overline{SEL}$ (PA0)
$\overline{CS}$	$\overline{CS}$	$\overline{CS}$	$\overline{CS}$ (PA1)
ALE	ALE	AS	N/C
$\overline{RD}$	$\overline{RD}$	DS;E; or Clock Phase 2	$\overline{REN}$
$\overline{WR}$	$\overline{WR}$	R/$\overline{W}$	$\overline{WE}$

REGISTER DESCRIPTIONS

The 32H6520 contains eight 8-bit internal registers which provide control, option select and status monitoring. The registers are addressed with a 3-bit register address which is latched from inputs at AD0(LSB), AD1, and AD2(MSB) at the falling edge of ALE. The registers 0, 2, and 3 are read/write memory, and the registers 1, 4, 5, 6, and 7 are write only memory. The registers are summarized in Table 2.

TABLE 2: Register Descriptions

ADDRESS	TYPE	REGISTER NAME
0	R/W	INTERRUPT MASK/STATUS
1	W	SERVO GAIN CONTROL & PRESCALER
2	R/W	ADC LSB DATA
3	R/W	ADC ADDRESS & MSB DATA
4	W	DAC1 LSB DATA
5	W	DAC1 MSB DATA
6	W	DAC2 LSB DATA
7	W	DAC2 MSB DATA

INTERRUPT MASK/STATUS REGISTER

Address: 0
Access: Read/Write
Reset: Bit 0, 1 only

Register contents when Written:

BIT	NAME	DESCRIPTION
0	BURST INT	When set HIGH, interrupt is enabled on the embedded servo position bursts ready.
1	ADC INT	When set HIGH, interrupt is enabled on the completion of the A/D conversion.
2 - 7		Unused.

Register contents when Read:

BIT	NAME	DESCRIPTION
0	BURSTRDY	Active high indicates that the embedded servo bursts are ready.
1	ADCRDY	Active high indicates that the A/D conversion is completed.

Each interrupt event status will be reset after the µP reads this register. The interrupt control register determines if the event will actually cause a latched assertion of the µP signal $\overline{INT}$.

SERVO GAIN CONTROL & PRESCALER REGISTER

Address: 1
Access: Write
Reset: 00

BIT	NAME	DESCRIPTION
0 1	SCALE0 SCALE1	SYSCLK Prescaler. To accommodate different system clocks, the prescaler selects a proper divider to generate a fixed clock at 4 MHz per table below:

SCALE1	SCALE0	SYSCLK(MHz)	Divider
0	0	16	4
0	1	12	3
1	0	8	2
1	1	4	1

BIT	NAME	DESCRIPTION
2 3 4 5	GAIN0 GAIN1 GAIN2 GAIN3	Servo Burst Amplitude Gain Select. These four bits define the gain setting for the differential/gain amplifier per table below:

GAIN3	GAIN4	GAIN3	GAIN0	Gain, dB
0	0	0	0	-2.8
0	0	0	1	-2.4
0	0	1	0	-2.0
0	0	1	1	-1.6
0	1	0	0	-1.2
0	1	0	1	-0.8
0	1	1	0	-0.4
0	1	1	1	+0.0
1	0	0	0	+0.4
1	0	0	1	+0.8
1	0	1	0	+1.2
1	0	1	1	+1.6
1	1	0	0	+2.0
1	1	0	1	+2.4
1	1	1	0	+2.8
1	1	1	1	+3.2

BIT	NAME	DESCRIPTION
6 7	BSTSEL0 BSTSEL1	Burst Number Select. These two bits define the number of embedded servo bursts per sector.

BSTSEL1	BSTSEL0	# of Bursts
0	0	2
0	1	3
1	0	4

ADC LSB DATA REGISTER

Address: 2
Access: Read/Write
Reset: Bit 5, 6, 7 only

Register contents when Written:

BIT	NAME	DESCRIPTION
0 - 4		Unused.
5	SLEEP	Power-down Mode Enable. When set HIGH, the device is in the sleep mode where all analog circuitry are de-biased, the clock is disabled, and the bandgap voltage, reference voltage fault logic and processor interface stay active.
6	STBEN1	When set HIGH, the analog output of the DAC1 is transferred and held onto DACOUT1.
7	STBEN2	When set HIGH, the analog output of the DAC2 is transferred and held onto DACOUT2.

Register contents when Read:

Description: After A/D conversion, the least significant 2 bits of the 10-bit digital word is stored into the register.

0 - 5		Unused. Logic LOW is provided to these bits.
6,7	ADC0, ADC1	The LSB 2 bits of the A/D converter output in 2's complement format.

ADC ADDRESS & MSB DATA REGISTER

Address: 3
Access: Read/Write
Reset: Bits 0, 1, 2, and 3 only

Description: When Written, the least significant 3 bits of the register define the analog input to the 10-bit A/D converter. After conversion, the most significant 8 bits of the 10-bit digital word is stored into the register.

Register contents when Written:

0 1 2	ADC SEL0 ADC SEL1 ADC SEL2	A/D Converter Input Select. These 3 bits define the analog input to the A/D converter per table below:

BIT2	BIT1	BIT0	ADC INPUT
0	0	0	ADCIN1
0	0	1	ADCIN2
0	1	0	ADCIN3
0	1	1	ADCIN4
1	0	0	BURST1
1	0	1	BURST2
1	1	0	BURST3
1	1	1	BURST4

ADC ADDRESS & MSB DATA REGISTER (continued)

BIT	NAME	DESCRIPTION
3	ADC CALIB	When set HIGH, VREF (2.23 volts) is applied to the A/D converter input.
4 - 7		Unused.

Register contents when Read:

0 - 7	ADC2 - 9	The MSB 8 bits of the A/D converter output in 2's complement. ADC9 is the sign bit.

DAC1 LSB DATA REGISTER

Address: 4
Access: Write
Reset: 00

0 - 5		Unused.
6, 7	DAC0, DAC1	The LSB 2 bits to the DAC1 in 2's complement.

DAC1 MSB DATA REGISTER

Address: 5
Access: Write
Reset: 00

0 - 7	DAC2 - 9	The MSB 8 bits to the DAC1 in 2's complement, DAC9 is the sign bit.

DAC2 LSB DATA REGISTER

Address: 6
Access: Write
Reset: 00

0 - 5		Unused.
6 7	DAC0, DAC1	The LSB 2 bits to the DAC2 in 2's complement.

DAC2 MSB DATA REGISTER

Address: 7
Access: Write
Reset: 00

0 - 7	DAC2 - 9	The MSB 8 bits to the DAC2 in 2's complement. DAC9 is the sign bit.

PIN DESCRIPTION

POWER SUPPLIES

NAME	DESCRIPTION
VPA	Analog +5V supply.
VPD	Digital +5V supply. It must be shorted to analog +5V supply externally.
VNA	Analog ground.
VND	Digital ground. It must be shorted to analog ground externally.
PSALT	Alternate Voltage Supply to power the voltage fault logic during a voltage fault. This power supply should be taken from the system +5V supply through a Schottky diode and be connected to a capacitor, which is used to hold up PSALT briefly during a voltage fault.

EMBEDDED SERVO BURST PROCESSOR

NAME	TYPE	DESCRIPTION
SERIN	I	Servo Burst Input - Full-wave rectified analog signal generated from a read data channel. This input is to extract the position information from embedded servo bursts.
SEREF	I	Servo Burst Reference - A DC reference level for the full-wave rectified analog signal SERIN.
INTEG	I	Pulse Area Detector Enable - This TTL compatible input, when HIGH, activates the pulse area detectors.
INTAZ	I	Integrator Capacitor Reset - This TTL compatible input, when HIGH, discharges the holding capacitors, Cint.

VOLTAGE FAULT DETECTION

PSV	I	Fault Voltage Comparator Input - A voltage input for the low voltage comparator. This input should be connected to an external resistor divider. The resistor divider divides its corresponding supply voltage to a proper value which is comparable with the internal voltage reference at 2.23 volts.
VREF	O	VREF Output - A buffered voltage reference at 2.23 volts.
IBR	O	Pin for connection to an external resistor (from GND) to establish a reference current for bias currents required for analog circuits.
VFAULT	O	Voltage Fault Indication - An open-drain output which is pulled HIGH when a supply voltage fault is detected.
$\overline{\text{SYSRST}}$	O	Reset Output - An open-drain output which is pulled LOW with an amount of delay determined by an external RC connected to the pin RCRST when a supply voltage fault is detected.
$\overline{\text{RCRST}}$	O	Pin for connection to an external RC to implement the delay of active LOW $\overline{\text{SYSRST}}$.

MICROPROCESSOR/DSP BUS INTERFACE

NAME	TYPE	DESCRIPTION
ALE	I	Address Latch Enable - Falling edge latches the register address from the AD0 - AD7 address/data bus.
$\overline{ASE}$	I	Address Strobe Enable - When set LOW, this input enables ALE input to the device.
$\overline{CS}$	I	Chip Select - Active LOW signal enables the device to respond to µP read or write.
$\overline{WR}$	I	Write Strobe - In Intel µP applications, active LOW signal causes the data on the address/data bus to be written to the addressed register if $\overline{CS}$ is also active.
$\overline{RD}$	I	Read Strobe - In Intel µP applications, active LOW signal causes the contents of the addressed register to be placed on the address/data bus if $\overline{CS}$ is also active.
AD0 - AD7	I/O	Address/Data Bus - 8-bit bus which carries register address information and bidirectional data. These pins are in the high impedance state when not used.
BUSMODE	I	Mode Select - When active HIGH, Intel bus interface is selected. Otherwise, Motorola bus interface is selected. For DSP interface, when DSPMODE set HIGH, this input is redefined as XFER/$\overline{SEL}$.
$\overline{INT}$	O	Interrupt Strobe - An open-drain output which signals the µP to respond to the device. It is released when all pending interrupts have been serviced by the µP.
DSPMODE	I	DSP Mode Select - When active HIGH, DSP bus interface is selected.
SYSCLK	I	System Clock Input - A TTL compatible input for the system clock which is divided down with a prescaler to generate internal timing signals.

DATA ACQUISITION

DACOUT1	O	DAC1 Output - A 10-bit D/A output which converts a digital word from the µP into an analog signal.
DACREF1	I	DAC1 Output Reference - An external analog input to be provided to DAC1 as a reference voltage for DACOUT1.
DACOUT2	O	DAC2 Output - A 10-bit D/A output which converts a digital word from the µP into an analog signal.
DACREF2	I	DAC2 Output Reference - An external analog input to be provided to DAC2 as a reference voltage for DACOUT2.
ADCIN1 ADCIN2 ADCIN3 ADCIN4	I	External A/D inputs.
ADCSH	I	A/D Analog Sampling Input Strobe - A TTL compatible control signal. During active HIGH, four track/hold amplifiers prior to the A/D converter will sample external A/D analog inputs.

DATA ACQUISITION (continued)

NAME	TYPE	DESCRIPTION
ADCSTR	I	A/D Conversion Start Strobe - A TTL compatible control signal whose rising edge triggers the start of the A/D conversion.
AUXINP	I	Level Shifter Noninverting Input - Noninverting input to the level-shifting amplifier.
AUXINM	I	Level Shifter Inverting Input - Inverting input to the level-shifting amplifier.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device or affect device reliability.

SYMBOL	PARAMETER	RATING
VDD	Supply voltage applied at VPA, VPD	-0.3 to 7.0V
GND	Signal ground applied at VNA, VND	0.0V
PSALT	Supply voltage applied at PSALT	-0.3 to 7.0V
VIND	Digital input voltages	-0.3 to VDD +0.3V
VINA	Analog input voltages	-0.3 to VDD +0.3V
Tstg	Storage temperature	-65 to 150 °C
TI	Lead temperature (10 seconds)	300 °C

RECOMMENDED OPERATING CONDITIONS

The recommended operating conditions for the device are indicated in the table below. Performance specifications do not apply where the device is operating outside these limits.

SYMBOL	PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VDD	Supply voltage applied at VPA, VPD		4.5		5.25	V
GND	Signal ground applied at VNA, VND		0.0		0.0	V
PSALT	Supply voltage applied at PSALT		3.0		6.0	V
TA	Ambient temperature		0.0		70.0	°C
Fc	System clock (16MHz, Max)				±0.1	%
Tc	System clock duty cycle		40		60	%

RECOMMENDED OPERATING CONDITIONS (continued)

SYMBOL	PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
CLOAD	Capacitive load on digital outputs		-		100	pF
RBIAS	Bias resistor (22.6 kΩ)				±1	%

DC CHARACTERISTICS

The following electrical specifications apply to the digital input and output signals over the recommended operating range unless otherwise noted. Positive current is defined as entering the device. Minimum and maximum are based upon the magnitude of the number.

IDD	Supply current Normal mode Sleep mode	VDD = 5.25V	 - -		 25 2	 mA mA
Voh	Output logic "1" voltage	Ioh = -0.4mA, VDD = 4.5V	2.4		-	V
Vol	Output logic "0" voltage	Iol = 1.6mA, VDD = 4.5V	-		0.4	V
Vih	Input logic "1" voltage	VDD = 4.5V	2.0		-	V
Vil	Input logic "0" voltage	VDD = 4.5V	-		0.8	V
Iih	Input logic "1" current	Vih = 5.25V, VDD = 5.25V	-		1	µA
Iil	Input logic "0" voltage	Vil = 0.0, VDD = 5.25V	-		-1	µA
Cin	Input capacitance		-		10	pF

FUNCTIONAL CHARACTERISTICS

EMBEDDED SERVO BURST AMPLITUDE PROCESSOR

SERIN with respect to GND		1.0	-	VDD	V
SEREF with respect to GND		1.0		3.0	V
SERIN input voltage	Servo gain = -2.8 dB	0.0	-	1.5	Vp
swing with respect to SEREF	Servo gain = 0 dB	0.0	-	1.0	Vp
Servo burst frequency		1.0	-	5.0	MHz
Input impedance at	Servo gain = -2.8 dB	15	20	25	kΩ
SERIN, SEREF	Servo gain = 0 dB	18	24	30	kΩ
Cin = 2 pF nominal	Servo gain = 3.2 dB	21	28	35	kΩ
C_{int} integration time, t_{INT}	Integrates to within 1% of	1.0			µs
C_{int} discharge time, t_{DISCH}		0.5			µs
Burst integration timing window separation, t_{NON}		0.5			µs
Servo burst ready, t_{RDY}		0.1			µs

EMBEDDED SERVO BURST AMPLITUDE PROCESSOR (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Servo channel ouput when SERIN shorted with SEREF	SEREF = 2V R_{int} = 63 kΩ	1.40	-	1.75	V
Servo channel gain step size	Guaranteed Monotonic	1.0	1.05	1.1	V/V
Servo channel slope deviation	SERIN from 0.2 V_p to 0.8 V_p R_{int} = 63 kΩ	-	-	±6	%

VOLTAGE REFERENCE AND VOLTAGE FAULT CIRCUIT

VPA voltage for $\overline{SYSRST}$ & RCRST in operation		2	-	5.25	V
On resistance at RCRST		-	-	100	Ω
RCRST input threshold	PSALT = 3V	0.8	-	1.6	V
IBR voltage with respect to VREF			-	±40	mV
VREF voltage	No load	2.16	2.23	2.30	V
Allowable load at VREF		10		-	kΩ
		-		100	pF
PSV comparator offset			-	±15	mV

A/D INPUT UNCOMMITTED OPERATIONAL AMPLIFIER

AUXINP Input Voltage	With respect to GND	1.25	-	2.5	V
Unit-gain bandwidth		2	-	-	MHz
Input-referred D.C. offset		-	-	±10	mV
Allowable load at ADCIN		5.0	-	-	kΩ
				40	pF

DATA ACQUISITION

A/D Converter

ADCIN full-scale voltage with respect to VREF		-	± (VREF/2)	-	V
Resolution		-	10	-	Bits
Acquisition time		-	1.0		µs
Conversion time		-	2.5		µs
LSB voltage		-	VREF/ 1024	-	V
Differential nonlinearity	Guaranteed Monotonic	-	-	±1.0	LSB

D/A Converter

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
DAC full-scale voltage with respect to DACREF		-	±(VREF/2)	-	V
Resolution		-	10	-	Bits
Digital delay		-	2.5	-	µs
Output settling time	To within ±0.5 LSB	-	5.0	-	µs
LSB voltage		-	VREF/ 1024	-	V
Differential nonlinearity	Guaranteed Monotonic	-	-	±1.0	LSB
DACREF1, DACREF2		1.5		2.3	V
DACOUT1, DACOUT2		0.3		3.5	V

Intel Microprocessor Interface Timing

The following timing specifications are applied when an Intel bus interface is selected by pulling the BUSMODE pin to logical HIGH and the DSPMODE pin to logical LOW. Timing measurements are made at 50% VDD with 100 pF load capacitances for all pins, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
t_{ALPW}	Pulse width, ALE HIGH		45		-	ns
t_{AS}	Muxed address valid time to ALE fall		7.5		-	ns
t_{AH}	Muxed address hold time after ALE fall		20		-	ns
t_{DDR}	Read data delay time from $\overline{RD}$ fall		-		60	ns
t_{DHR}	Read data hold time after $\overline{RD}$ rise		0		50	ns
t_{RDPW}	Pulse width, $\overline{RD}$ LOW		75		-	ns
t_{DSW}	Write data setup time to $\overline{WR}$ rise		40			ns
t_{DHW}	Write data hold time after $\overline{WR}$ rise		10		-	ns
t_{WRPW}	Pulse width, $\overline{WR}$ LOW		50		-	ns
t_{RWD}	$\overline{RD}$ or $\overline{WR}$ delay time from ALE fall		25		-	ns
t_{CSS}	$\overline{CS}$ setup time prior to ALE fall		0		-	ns
t_{CSH}	$\overline{CS}$ hold time after $\overline{RD}$ or $\overline{WR}$ rise		0		-	ns
t_{ASES}	$\overline{ASE}$ setup time prior to ALE fall		45		-	ns
t_{ASEH}	$\overline{ASE}$ hold time to ALE fall		0		-	ns

7

Motorola Microprocessor Interface Timing

The following timing specifications are applied when a Motorola bus interface is selected by pulling the BUSMODE pin to logical LOW and the DSPMODE pin to logical LOW. Timing measurements are made at 50% VDD with 100 pF load capacitances for all pins, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
t_{ASPW}	Pulse width, AS HIGH		45		-	ns
t_{AS}	Muxed address valid time to AS fall		7.5		-	ns
t_{AH}	Muxed address hold time after AS fall		20		-	ns
t_{DDR}	Read data delay time from DS rise		-		100	ns
t_{DHR}	Read data hold time after DS fall		0		50	ns
t_{DSPWR}	Pulse width, DS HIGH during READ		100		-	ns
t_{DSW}	Write data setup time prior to DS fall		60		-	ns
t_{DHW}	Write data hold time after DS fall		10		-	ns
t_{DSPWW}	Pulse width, DS HIGH during WRITE		100		-	ns
t_{ASDS}	DS delay time from AS fall		25		-	ns
t_{ASRW}	R/$\overline{W}$ delay time from AS fall during WRITE		25		-	ns
t_{RWH}	R/$\overline{W}$ hold time after DS fall during WRITE		0		-	ns
t_{CSS}	$\overline{CS}$ setup time prior to AS fall		0		-	ns
t_{CSH}	$\overline{CS}$ hold time after DS fall		0		-	ns
t_{ASES}	$\overline{ASE}$ setup time prior to AS fall		45		-	ns
t_{ASEH}	$\overline{ASE}$ hold time after AS fall		0		-	ns

DSP Interface Timing

The following timing specifications are applied when a DSP bus interface is selected by pulling the DSPMODE pin to logical HIGH. Timing measurements are made at 50% VDD with 100 pF load capacitances for all pins, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
t_{ALPW}	Pulse width, XFER/$\overline{SEL}$ LOW		75		-	ns
t_{ALHW}	XFER/$\overline{SEL}$ hold time after $\overline{WR}$ rise		0		-	ns
t_{DDR}	Read data delay time from $\overline{REN}$ fall		-		60	ns
t_{DHR}	Read data hold time after $\overline{REN}$ rise		0		50	ns
t_{RDPW}	Pulse width $\overline{REN}$ LOW		50		-	ns
t_{DSW}	Write data setup time prior to $\overline{WR}$ rise		40		-	ns
t_{DHW}	Write data hold time after $\overline{WR}$ rise		10		-	ns
t_{WRPW}	Pulse width, $\overline{WR}$ LOW		50		-	ns
t_{CSSW}	$\overline{CS}$ setup time prior to $\overline{WR}$		25		-	ns
t_{CSSR}	$\overline{CS}$ setup time prior to $\overline{REN}$		25		-	ns
t_{CSH}	$\overline{CS}$ hold time after $\overline{REN}$ or $\overline{WR}$ rise		0		-	ns

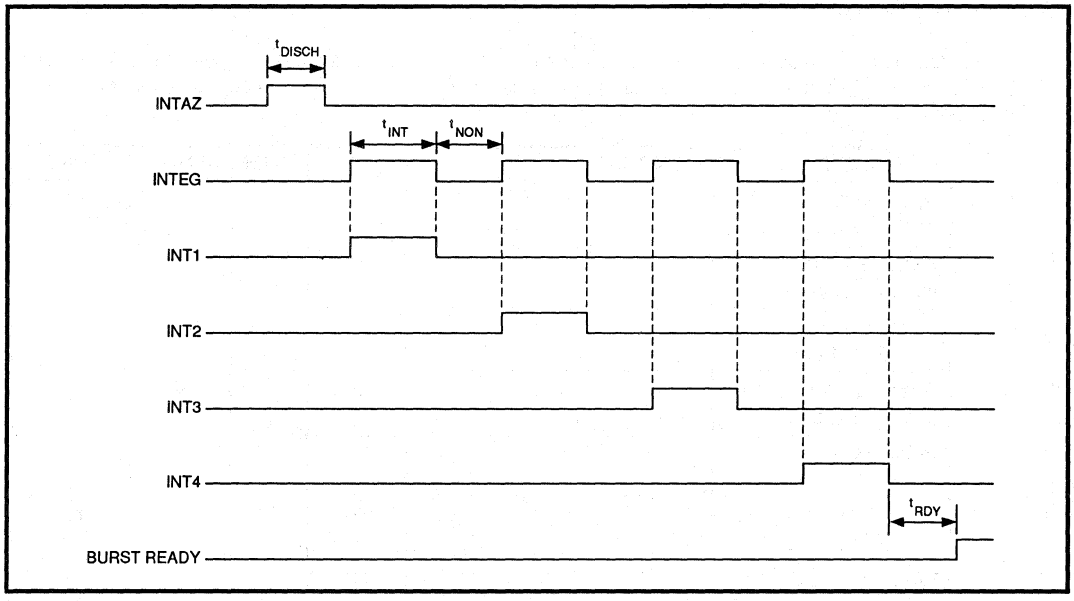


FIGURE 1: Embedded Servo Burst Processor Timing Diagram

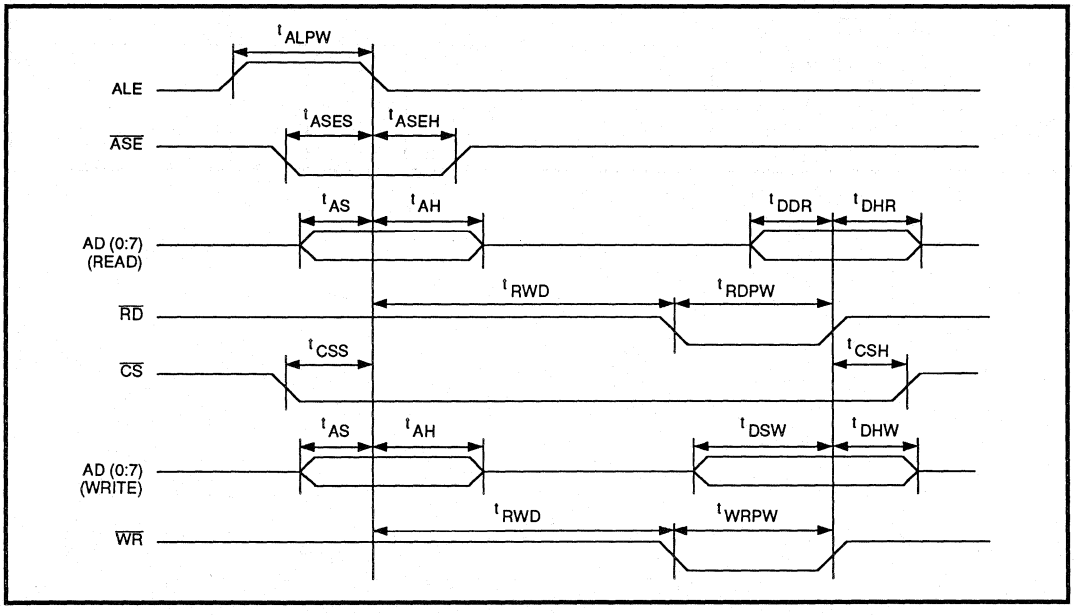


FIGURE 2: Intel Microprocessor Bus Interface Timing Diagram

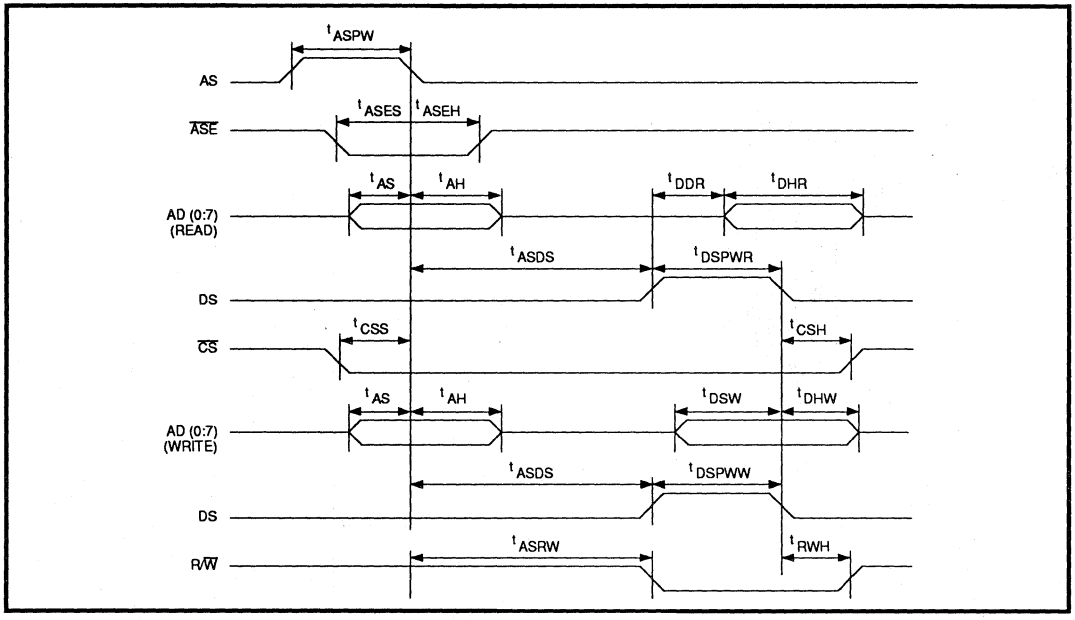


FIGURE 3: Motorola Microprocessor Bus Interface Timing Diagram

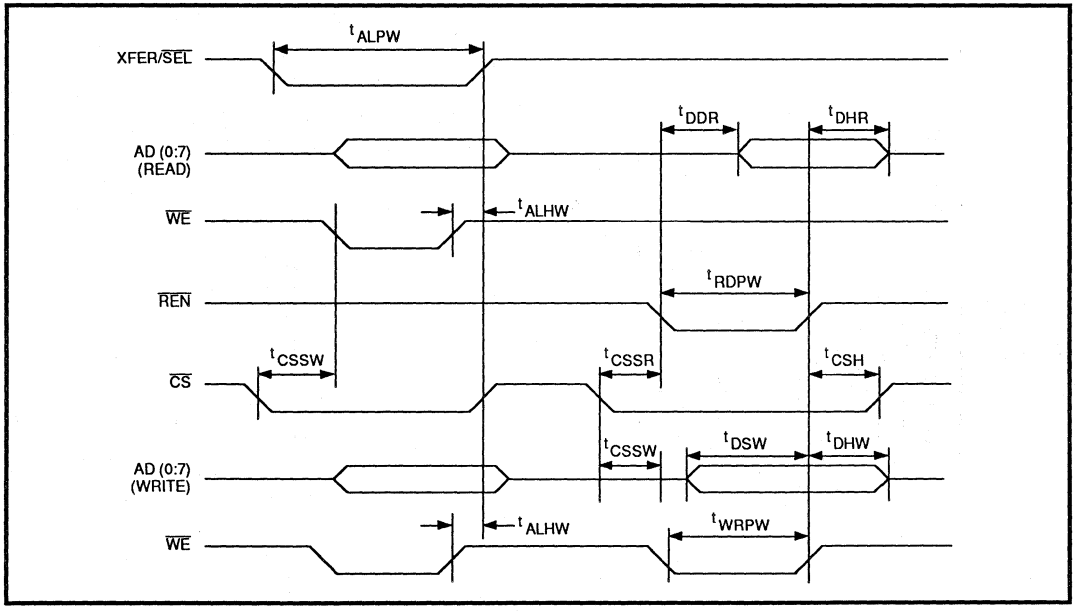


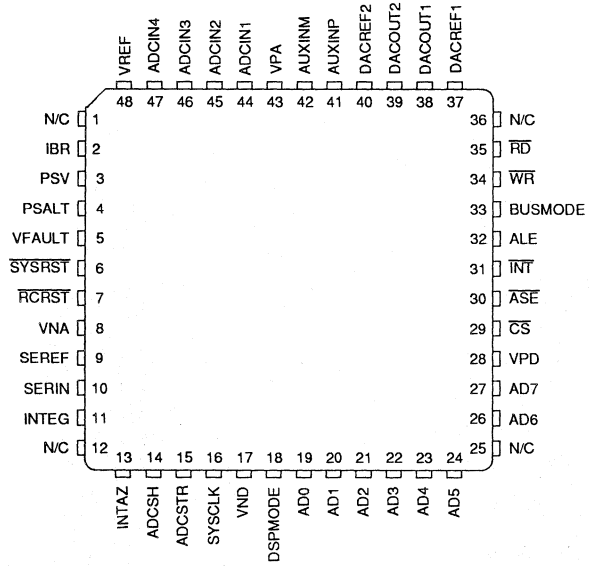
FIGURE 4: TMS320XX Bus Interface Timing Diagram

0: INTERRUPT MASK/STATUS			1: SERVO GAIN CONTROL & PRESCALER			2: ADC LSB DATA			3: ADC ADDRESS & MSB DATA		
#	WRITE	READ	#	WRITE	READ	#	WRITE	READ	#	WRITE	READ
0	BURST INT	BURSTRDY	0	SCALE0		0		'0'	0	ADC SEL0	ADC2
1	ADC INT	ADCRDY	1	SCALE1		1		'0'	1	ADC SEL1	ADC3
2			2	GAIN0		2		'0'	2	ADC SEL2	ADC4
3			3	GAIN1		3		'0'	3	ADC CALIB	ADC5
4			4	GAIN2		4		'0'	4		ADC6
5			5	GAIN3		5	SLEEP	'0'	5		ADC7
6			6	BSTSEL0		6	STBEN1	ADC0	6		ADC8
7			7	BSTSEL1		7	STBEN2	ADC1	7		ADC9
4: DAC1 LSB DATA			5: DAC1 MSB DATA			6: DAC2 LSB DATA			7: DAC2 MSB DATA		
#	WRITE	READ	#	WRITE	READ	#	WRITE	READ	#	WRITE	READ
0			0	DAC2 1		0			0	DAC2 2	
1			1	DAC3 1		1			1	DAC3 2	
2			2	DAC4 1		2			2	DAC4 2	
3			3	DAC5 1		3			3	DAC5 2	
4			4	DAC6 1		4			4	DAC6 2	
5			5	DAC7 1		5			5	DAC7 2	
6	DAC0 1		6	DAC8 1		6	DAC0 2		6	DAC8 2	
7	DAC1 1		7	DAC9 1		7	DAC1 2		7	DAC9 2	

FIGURE 5: SSI 32H6520 Embedded Servo Processor Register Map

PACKAGE PIN DESIGNATIONS

(Top View)



48-pin TQFP

CAUTION: Use handling procedures necessary for a static sensitive component.

ORDERING INFORMATION

PART DESCRIPTION	ORDER NUMBER	PACKAGE MARK
SSI 32H6520 48-pin TQFP	32H6520-CGT	32H6520-CGT

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

Silicon Systems, Inc. 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914

Notes:

silicon systems®
A TDK Group Company

SSI 32H6521
Embedded Servo Controller

Preliminary Data

December 1993

DESCRIPTION

The SSI 32H6521 Embedded Servo Controller is a CMOS monolithic integrated circuit housed in a 44-lead SO and operates on a single +5.0 volt supply. It provides one 10-bit A/D converter with 2.5 µs conversion time, and two 10-bit D/A converters with 2.5 µs digital delay. In addition, it includes bus interface logic to support DSP-based, such as TMS320C25, digital servo applications.

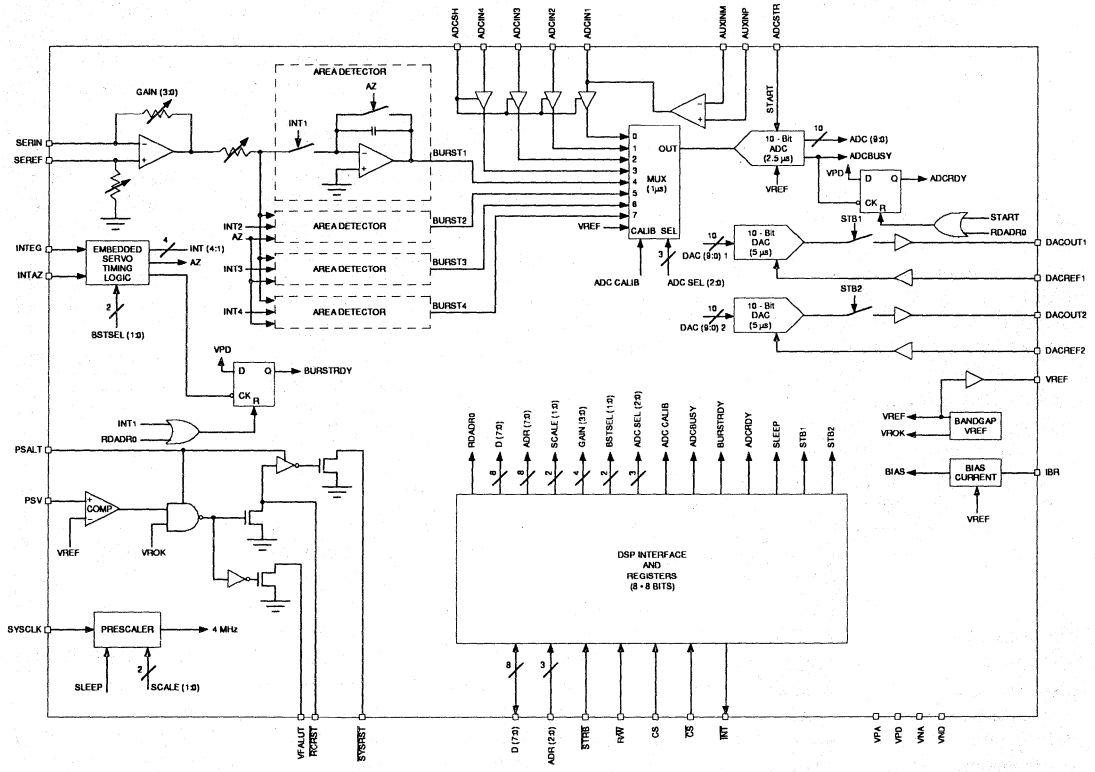
FEATURES

Embedded Servo Burst Processor

- Servo control for Winchester disk drives with embedded servo sectors
- For use in DSP-based digital servo applications
- Pulse area detects and S/H circuits for up to four embedded servo bursts
- Programmable gain adjustment from -2.8 dB to 3.2 dB

(continued)

BLOCK DIAGRAM



FEATURES (continued)

Data Acquisition and DSP Bus Interface

- Bus interface logic to support DSP-based digital servo applications
- Eight internal registers and address decoding
- Two 10-bit D/A converters with 2.5 µs digital delay
- One 8-channel 10-bit A/D converter with 2.5 µs conversion time

General Functions

- Voltage fault detection
- Low power CMOS design

FUNCTIONAL DESCRIPTION

The SSI 32H6521 can be divided into four major sections: embedded servo burst processor, voltage fault detector/logic, data acquisition and DSP bus interface.

EMBEDDED SERVO BURST PROCESSOR

The embedded servo burst processor extracts the head position error information from the embedded servo bursts using an area detection technique. The area detection technique provides improved noise immunity over peak detection. The embedded servo burst processor contains a differential/gain amplifier, four pulse area detectors and required timing logic. First, a full wave-rectified analog signal from a read data channel, such as SSI 32P4622, is provided at SERIN through an external resistor equal to Rint and a DC reference level for the full wave-rectified analog signal at SEREF through another external resistor equal to Rint. To accommodate a wide dynamic range of servo burst amplitudes and process variations of the integration capacitor Cint, the differential signal between SERIN and SEREF is scaled under DSP control. The gain of the differential amplifier ranges from -2.8 dB to 3.2 dB in a step of 0.4 dB, as defined in the SERVO GAIN CONTROL register. The output of the differential/gain amplifier is then provided to four pulse area detectors whose outputs are proportional to the area above the DC reference level during time intervals defined by an external timing source through INTEG. Each area detector applies an on-chip capacitor Cint equal to 10 pF to integrate the incoming pulses during the integration interval and then hold the integrated voltage outputs thereafter. Note that the max ±20% tolerance of on-chip capacitors can be calibrated out by adjusting the gain of the preceding amplifier. Finally, the integrated voltage outputs at BURST1, BURST2, BURST3 and BURST4 are provided to a 10–bit A/D converter under DSP control and will be discharged during a time interval defined by an external timing source through INTAZ. For proper operatons, the time interval defined by the INTAZ must be no less than 0.5 µs and be applied only once per servo frame preceding the integration pulses defined by the INTEG.

Limited timing logic is included to generate all the timing signals required for the embedded servo burst processor, per Figure 1. These timing signals control the integration, sample/hold of the pulse area detectors. The number of embedded servo bursts supported by this circuit are two, three or four. The BSTSEL0 and BSTSEL1 bits in the SERVO CONTROL register configure the internal timing logic to generate a servo burst ready interrupt after the last servo burst is captured.

VOLTAGE FAULT DETECTOR/LOGIC

The voltage fault detector monitors the power supply applied at PSV through an external resistor divider, which defines the trigger level for power supply failure. An open-drain output VFAULT is pulled HIGH by an external resistor when a power supply failure is sensed by the PSV comparator. The user-defined trigger level for voltage failure is applied at PSV. Another open-drain output, opposite logic polarity as the pin VFAULT and with an additional RC delay, is provided at $\overline{\text{SYSRST}}$. The amount of $\overline{\text{SYSRST}}$ delay is determined by an external RC connected to the pin, $\overline{\text{RCRST}}$.

DATA ACQUISITION

The A/D converter is multiplexed to eight different analog inputs by programming the ADC SEL0, ADC SEL1, and ADC SEL2 bits in the ADC ADDRESS register by the DSP. The eight analog inputs multiplexed to the A/D converter are four embedded servo processor outputs at BURST1, BURST2, BURST3 and BURST4 and four external analog inputs through four T/H amplifiers. These T/H amplifiers sample external analog inputs during the time interval defined by an external timing source applied at ADCSH. If the sampling of four external analog inputs is not necessarily synchronized, ADCSH must be tied to HIGH. The A/D

conversions on these external analog inputs are always referenced to the internal voltage reference at 2.23 volts. An operational amplifier with uncommitted inputs is provided to implement a level shifting function for the external analog input applied to AUXINP. The output of the operational amplifier is tied to ADCIN1.

The A/D converter starts to acquire a new analog input whenever the conversion is completed. A minimum of 1 µs is required to acquire an analog input to the A/D converter. Actual conversion is started by reading the A/D MSB register or by an external timing source applied to ADCSTR. The A/D address lines ADC SEL0, ADC SEL1, and ADC SEL2 will be incremented by one after the A/D conversion is started. The automatic increment of the address lines is employed to eliminate repetitive write operations by the DSP to the ADC ADDRESS register required for converting the consecutive analog inputs.

The A/D converter runs synchronously with the internal 4 MHz clock which is used for various circuits on the SSI 32H6521 and divided down from the system clock SYSCLK by a prescaler. Therefore there would be a maximum of 0.25 µs of latency between a conversion request and the actual start of the conversion. The output is coded in 2's complement.

Do not read from the device during A/D conversion. Digital noise generated by the read cycle may be coupled into the A/D converter. Coupled noise can prevent 10-bit accuracy.

Similarly, the D/A converters run synchronously with the internal 2 MHz clock and the conversion is started by writing to the corresponding D/A input register. The output of the first D/A converter is referenced to an external analog input, DACREF1 and the output of the second D/A converter is referenced to an external analog input, DACREF2. In the "normal" mode when STBEN1 (STBEN2) bit in the ADC ADDRESS register is reset, the D/A output will be automatically applied to DACOUT1 (DACOUT2) during the conversion. In the "strobe" mode, the D/A output will be applied to DACOUT1 (DACOUT2) at the falling edge of $\overline{RD}$ for a read to the corresponding D/A MSB DATA register.

DSP BUS INTERFACE

The SSI 32H6521 provides interface logic for a direct connection to TMS320CXX DSP. It contains an 8-bit data bus and 3 address lines for communicating with eight internal registers. Bus control signals are $\overline{CS}$, CS, $\overline{STRB}$ and R/$\overline{W}$. The address lines are internally latched when the device is selected ($\overline{CS}$ active low and CS active high). The timing requirements for the DSP bus interface are depicted in Figure 2.

Avoid accessing this device while the servo burst capture, D/A or A/D conversion is in progress. Digital bus noise will couple into the signal path through the substrate and corrupt the signal. To maintain signal integrity, it is recommended that read operations be avoided during servo burst capture, and sufficient time be allowed for the last A/D conversion to be completed.

REGISTER DESCRIPTIONS

The 32H6521 contains eight 8-bit internal registers which provide control, option select and status monitoring. The registers are addressed with a 3-bit register address which is latched from inputs at ADR0(LSB), ADR1, and ADR2(MSB) while the device is selected. The registers 0, 2, and 3 are read/write memory, and the registers 1, 4, 5, 6, and 7 are write only memory. The registers are summarized in Table 2.

TABLE 2: Register Descriptions

ADDRESS	TYPE	REGISTER NAME
0	R/W	INTERRUPT MASK/STATUS
1	W	SERVO GAIN CONTROL & PRESCALER
2	R/W	ADC LSB DATA
3	R/W	ADC ADDRESS & MSB DATA
4	W	DAC1 LSB DATA
5	W	DAC1 MSB DATA
6	W	DAC2 LSB DATA
7	W	DAC2 MSB DATA

INTERRUPT MASK/STATUS REGISTER

Address: 0
Access: Read/Write
Reset: Bit 0, 1 only

Register contents when Written:

BIT	NAME	DESCRIPTION
0	BURST INT	When set HIGH, interrupt is enabled on the embedded servo position bursts ready.
1	ADC INT	When set HIGH, interrupt is enabled on the completion of the A/D conversion.
2 - 7		Unused.

Register contents when Read:

BIT	NAME	DESCRIPTION
0	BURSTRDY	Active high indicates that the embedded servo bursts are ready.
1	ADCRDY	Active high indicates that the A/D conversion is completed.

Each interrupt event status will be reset after the DSP reads this register. The interrupt control register determines if the event will actually cause a latched assertion of the DSP signal $\overline{INT}$.

SERVO GAIN CONTROL & PRESCALER REGISTER

Address: 1
Access: Write
Reset: 00

BIT	NAME	DESCRIPTION
0 1	SCALE0 SCALE1	SYSCLK Prescaler. To accommodate different system clocks, the prescaler selects a proper divider to generate a fixed clock at 4 MHz per table below:

SCALE1	SCALE0	SYSCLK(MHz)	Divider
0	0	16	4
0	1	12	3
1	0	8	2
1	1	4	1

BIT	NAME	DESCRIPTION
2 3 4 5	GAIN0 GAIN1 GAIN2 GAIN3	Servo Burst Amplitude Gain Select. These four bits define the gain setting for the differential/gain amplifier per table below:

GAIN3	GAIN4	GAIN3	GAIN0	Gain, dB
0	0	0	0	-2.8
0	0	0	1	-2.4
0	0	1	0	-2.0
0	0	1	1	-1.6
0	1	0	0	-1.2
0	1	0	1	-0.8
0	1	1	0	-0.4
0	1	1	1	+0.0
1	0	0	0	+0.4
1	0	0	1	+0.8
1	0	1	0	+1.2
1	0	1	1	+1.6
1	1	0	0	+2.0
1	1	0	1	+2.4
1	1	1	0	+2.8
1	1	1	1	+3.2

BIT	NAME	DESCRIPTION
6 7	BSTSEL0 BSTSEL1	Burst Number Select. These two bits define the number of embedded servo bursts per sector.

BSTSEL1	BSTSEL0	# of Bursts
0	0	2
0	1	3
1	0	4

ADC LSB DATA REGISTER

Address: 2
Access: Read/Write
Reset: Bit 5, 6, 7 only

Register contents when Written:

BIT	NAME	DESCRIPTION
0 - 4		Unused.
5	SLEEP	Power-down Mode Enable. When set HIGH, the device is in the sleep mode where all analog circuitry are de-biased, the clock is disabled, and the bandgap voltage, reference voltage fault logic and processor interface stay active.
6	STBEN1	When set HIGH, the analog output of the DAC1 is transferred and held onto DACOUT1.
7	STBEN2	When set HIGH, the analog output of the DAC2 is transferred and held onto DACOUT2.

Register contents when Read:

Description: After A/D conversion, the least significant 2 bits of the 10-bit digital word is stored into the register.

0 - 5		Unused. Logic LOW is provided to these bits.
6,7	ADC0, ADC1	The LSB 2 bits of the A/D converter output in 2's complement format.

ADC ADDRESS & MSB DATA REGISTER

Address: 3
Access: Read/Write
Reset: Bits 0, 1, 2, and 3 only

Description: When Written, the least significant 3 bits of the register define the analog input to the 10-bit A/D converter. After conversion, the most significant 8 bits of the 10-bit digital word is stored into the register.

Register contents when Written:

0 1 2	ADC SEL0 ADC SEL1 ADC SEL2	A/D Converter Input Select. These 3 bits define the analog input to the A/D converter per table below:			
		BIT2	BIT1	BIT0	ADC INPUT
		0	0	0	ADCIN1
		0	0	1	ADCIN2
		0	1	0	ADCIN3
		0	1	1	ADCIN4
		1	0	0	BURST1
		1	0	1	BURST2
		1	1	0	BURST3
		1	1	1	BURST4

ADC ADDRESS & MSB DATA REGISTER (continued)

BIT	NAME	DESCRIPTION
3	ADC CALIB	When set HIGH, VREF (2.23 volts) is applied to the A/D converter input.
4 - 7		Unused.

Register contents when Read:

0 - 7	ADC2 - 9	The MSB 8 bits of the A/D converter output in 2's complement. ADC9 is the sign bit.

DAC1 LSB DATA REGISTER

Address: 4
Access: Write
Reset: 00

0 - 5		Unused.
6, 7	DAC0, DAC1	The LSB 2 bits to the DAC1 in 2's complement.

DAC1 MSB DATA REGISTER

Address: 5
Access: Write
Reset: 00

0 - 7	DAC2 - 9	The MSB 8 bits to the DAC1 in 2's complement, DAC9 is the sign bit.

DAC2 LSB DATA REGISTER

Address: 6
Access: Write
Reset: 00

0 - 5		Unused.
6 7	DAC0, DAC1	The LSB 2 bits to the DAC2 in 2's complement.

DAC2 MSB DATA REGISTER

Address: 7
Access: Write
Reset: 00

0 - 7	DAC2 - 9	The MSB 8 bits to the DAC2 in 2's complement. DAC9 is the sign bit.

PIN DESCRIPTION

POWER SUPPLIES

NAME	DESCRIPTION
VPA	Analog +5V supply.
VPD	Digital +5V supply. It must be shorted to analog +5V supply externally.
VNA	Analog ground.
VND	Digital ground. It must be shorted to analog ground externally.
PSALT	Alternate Voltage Supply to power the voltage fault logic during a voltage fault. This power supply should be taken from the system +5V supply through a Schottky diode and be connected to a capacitor, which is used to hold up PSALT briefly during a voltage fault.

EMBEDDED SERVO BURST PROCESSOR

NAME	TYPE	DESCRIPTION
SERIN	I	Servo Burst Input - Full-wave rectified analog signal generated from a read data channel. This input is to extract the position information from embedded servo bursts.
SEREF	I	Servo Burst Reference - A DC reference level for the full-wave rectified analog signal SERIN.
INTEG	I	Pulse Area Detector Enable - This TTL compatible input, when HIGH, activates the pulse area detectors.
INTAZ	I	Integrator Capacitor Reset - This TTL compatible input, when HIGH, discharges the holding capacitors, Cint.

VOLTAGE FAULT DETECTION

PSV	I	Fault Voltage Comparator Input - A voltage input for the low voltage comparator. This input should be connected to an external resistor divider. The resistor divider divides its corresponding supply voltage to a proper value which is comparable with the internal voltage reference at 2.23 volts.
VREF	O	VREF Output - A buffered voltage reference at 2.23 volts.
IBR	O	Pin for connection to an external resistor (from GND) to establish a reference current for bias currents required for analog circuits.
VFAULT	O	Voltage Fault Indication - An open-drain output which is pulled HIGH when a supply voltage fault is detected.
$\overline{\text{SYSRST}}$	O	Reset Output - An open-drain output which is pulled LOW with an amount of delay determined by an external RC connected to the pin RCRST when a supply voltage fault is detected.
$\overline{\text{RCRST}}$	O	Pin for connection to an external RC to implement the delay of active LOW $\overline{\text{SYSRST}}$.

DSP BUS INTERFACE

NAME	TYPE	DESCRIPTION
D0 - D7	I/O	8-Bit Bidirectional Data Bus. - These bidirectional data pins are in the high impedance state when the device is not selected
ADR0 - ADR2	I	3-bit address lines to select an internal register for I/O.
$\overline{STRB}$	I	Data Strobe. - The data on the data bus is written to the addressed register at the rising edge of $\overline{STRB}$.
R/$\overline{W}$	I	READ/$\overline{WRITE}$ Enable. - When low, the data is to be written to the addressed register. Otherwise, the contents of the addressed register are placed on the data bus.
$\overline{CS}$, CS	I	2-Bit Chip Select Lines. - This device is selected when $\overline{CS}$ is low and CS is high.
$\overline{INT}$	O	Interrupt - An open-drain output which signals the DSP to respond to the device. It is released when all pending interrupts have been serviced by the DSP.
SYSCLK	I	System Clock Input - A TTL compatible input for the system clock which is divided down with a prescaler to generate internal timing signals.

DATA ACQUISITION

DACOUT1	O	DAC1 Output - A 10-bit D/A output which converts a digital word from the DSP into an analog signal.
DACREF1	I	DAC1 Output Reference - An external analog input to be provided to DAC1 as a reference voltage for DACOUT1.
DACOUT2	O	DAC2 Output - A 10-bit D/A output which converts a digital word from the DSP into an analog signal.
DACREF2	I	DAC2 Output Reference - An external analog input to be provided to DAC2 as a reference voltage for DACOUT2.
ADCIN1 ADCIN2 ADCIN3 ADCIN4	I	External A/D inputs.
ADCSH	I	A/D Analog Sampling Input Strobe - A TTL compatible control signal. During active HIGH, four track/hold amplifiers prior to the A/D converter will sample external A/D analog inputs.
ADCSTR	I	A/D Conversion Start Strobe - A TTL compatible control signal whose rising edge triggers the start of the A/D conversion.
AUXINP	I	Level Shifter Noninverting Input - Noninverting input to the level-shifting amplifier.
AUXINM	I	Level Shifter Inverting Input - Inverting input to the level-shifting amplifier.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device or affect device reliability.

SYMBOL	PARAMETER	RATING
VDD	Supply voltage applied at VPA, VPD	-0.3 to 7.0V
GND	Signal ground applied at VNA, VND	0.0V
PSALT	Supply voltage applied at PSALT	-0.3 to 7.0V
VIND	Digital input voltages	-0.3 to VDD + 0.3V
VINA	Analog input voltages	-0.3 to VDD + 0.3V
Tstg	Storage temperature	-65 to 150 °C
TI	Lead temperature (10 seconds)	300 °C

RECOMMENDED OPERATING CONDITIONS

The recommended operating conditions for the device are indicated in the table below. Performance specifications do not apply where the device is operating outside these limits.

SYMBOL	PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VDD	Supply voltage applied at VPA, VPD		4.5		5.25	V
GND	Signal ground applied at VNA, VND		0.0		0.0	V
PSALT	Supply voltage applied at PSALT		3.0		6.0	V
TA	Ambient temperature		0.0		70.0	°C
Fc	System clock (16MHz, Max)				±0.1	%
Tc	System clock duty cycle		40		60	%
C_{LOAD}	Capacitive load on digital outputs		-		50	pF
R_{BIAS}	Bias resistor (22.6 kΩ)				±1	%

DC CHARACTERISTICS

The following electrical specifications apply to the digital input and output signals over the recommended operating range unless otherwise noted. Positive current is defined as entering the device. Minimum and maximum are based upon the magnitude of the number.

SYMBOL	PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
IDD	Supply current Normal mode Sleep mode	VDD = 5.25V	 - -		 25 5	 mA mA
Voh	Output logic "1" voltage	Ioh = -0.4mA, VDD = 4.5V	2.4		-	V
Vol	Output logic "0" voltage	Iol = 1.6mA, VDD = 4.5V	-		0.4	V
Vih	Input logic "1" voltage	VDD = 4.5V	2.0		-	V
Vil	Input logic "0" voltage	VDD = 4.5V	-		0.8	V
Iih	Input logic "1" current	Vih = 5.25V, VDD = 5.25V	-		1	µA
Iil	Input logic "0" voltage	Vil = 0.0, VDD = 5.25V	-		-1	µA
Cin	Input capacitance		-		10	pF

FUNCTIONAL CHARACTERISTICS

EMBEDDED SERVO BURST AMPLITUDE PROCESSOR

SERIN with respect to GND		1.0	-	VDD	V
SEREF with respect to GND		1.0		3.0	V
SERIN input voltage	Servo gain = -2.8 dB	0.0	-	1.5	Vp
swing with respect to SEREF	Servo gain = 0 dB	0.0	-	1.0	Vp
Servo burst frequency		1.0	-	5.0	MHz
Input impedance at	Servo gain = -2.8 dB	15	20	25	kΩ
SERIN, SEREF	Servo gain = 0 dB	18	24	30	kΩ
Cin = 2 pF nominal	Servo gain = 3.2 dB	21	28	35	kΩ
C_{int} integration time, t_{INT}	Integrates to within 1% of	1.0			µs
C_{int} discharge time, t_{DISCH}		0.5			
Burst integration timing window separation, t_{NON}		0.1			µs
Servo burst ready, t_{RDY}		0.1			µs

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EMBEDDED SERVO BURST AMPLITUDE PROCESSOR (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Servo channel ouput when SERIN shorted with SEREF	SEREF = 2V R_{int} = 63 kΩ	1.45	-	1.75	V
Servo channel gain step size	Guaranteed Monotonic	1.0	1.05	1.1	V/V
Servo channel slope deviation	SERIN from 0.2 V_p to 0.8 V_p R_{int} = 63 kΩ	-	-	±10	mV
Channel mismatch				100	mV

Note: Servo channel includes the servo burst capture circuit, A/D and D/A converters.

VOLTAGE REFERENCE AND VOLTAGE FAULT CIRCUIT

VPA voltage for $\overline{SYSRST}$ & RCRST in operation		2	-	5.25	V
On resistance at RCRST		-	-	100	Ω
RCRST input threshold	PSALT = 3V	0.8	-	1.6	V
IBR voltage with respect to VREF			-	±100	mV
VREF voltage	No load	2.16	2.23	2.30	V
Allowable load at VREF		10		-	kΩ
		-		100	pF
PSV comparator offset			-	±15	mV

A/D INPUT UNCOMMITTED OPERATIONAL AMPLIFIER

AUXINP Input Voltage	With respect to GND	1.25	-	3.25	V
Unit-gain bandwidth		1	-	-	MHz
Input-referred D.C. offset		-	-	±10	mV
Allowable load at ADCIN		5.0	-	-	kΩ
				40	pF

DATA ACQUISITION

A/D Converter

ADCIN full-scale voltage with respect to VREF		-	± (VREF/2)	-	V
Resolution		-	10	-	Bits
Acquisition time		-	1.0		µs
Conversion time		-	2.5		µs
LSB voltage		-	VREF/ 1024	-	V
Differential nonlinearity	Guaranteed Monotonic	-	-	±1.0	LSB

D/A Converter

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
DAC full-scale voltage with respect to DACREF		-	±(VREF/2)	-	V
Resolution		-	10	-	Bits
Digital delay		-	2.5	-	µs
Output settling time	To within ±1 LSB	-	5.0	-	µs
LSB voltage		-	VREF/ 1024	-	V
Differential nonlinearity	Guaranteed Monotonic	-	-	±1.0	LSB
DACREF1, DACREF2		1.5		2.3	V
DACOUT1, DACOUT2		0.3		3.5	V

DSP Interface Timing

The following timing specifications are applied for a DSP bus interface . Timing measurements are made at 50% VDD with 50 pF load capacitances for data pins, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
t_{STRBS}	ADR0..2/CS/$\overline{CS}$/R/$\overline{W}$ setup time prior to $\overline{STRB}$ fall		10		-	ns
t_{DDR}	Read data delay time from $\overline{STRB}$ fall		-		50	ns
t_{DHR}	Read data hold time after $\overline{STRB}$ rise		0		20	ns
t_{DSW}	Write data setup time prior to $\overline{STRB}$ rise		20		-	ns
t_{DHW}	Write data hold time after $\overline{STRB}$ rise		10		-	ns

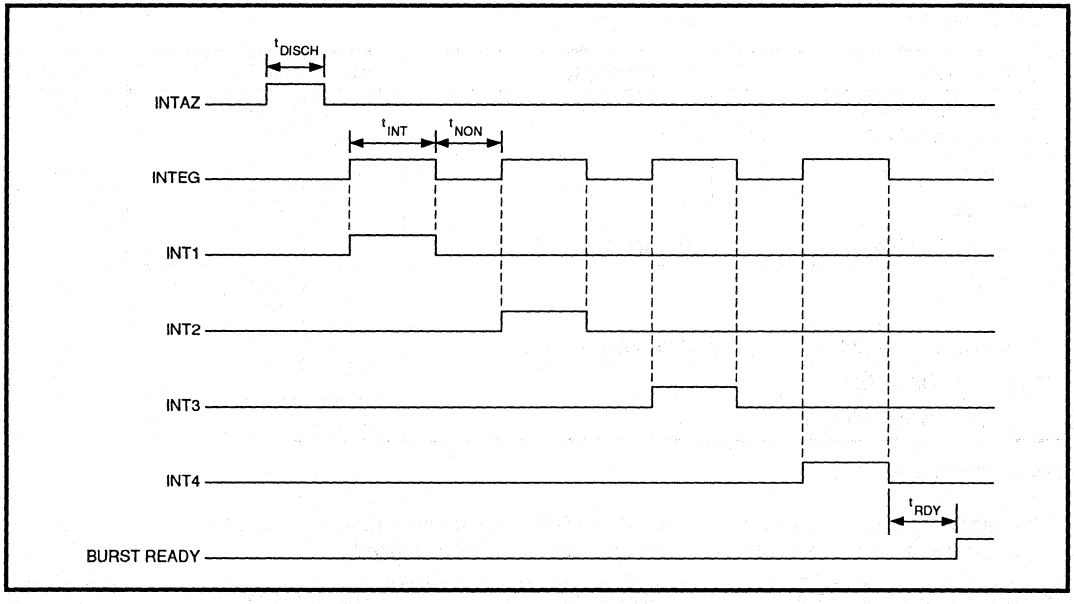


FIGURE 1: Embedded Servo Burst Processor Timing Diagram

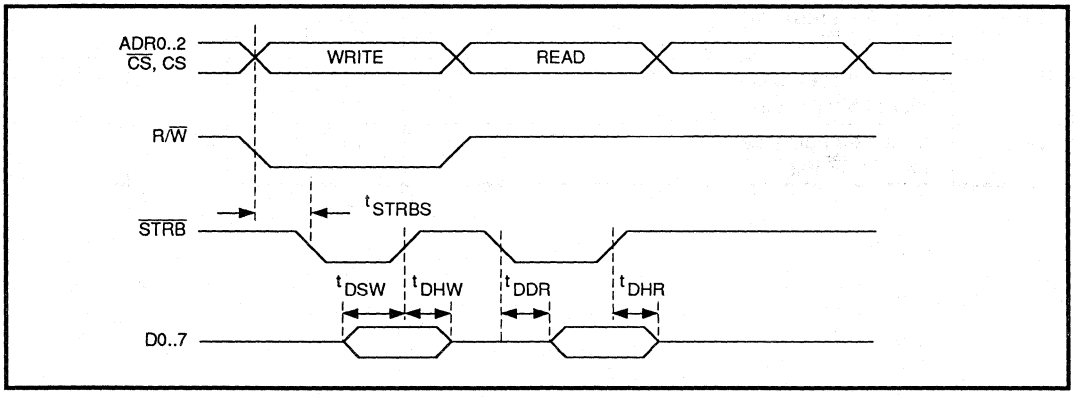


FIGURE 2: TMS320CXX DSP Bus Interface Timing Diagram

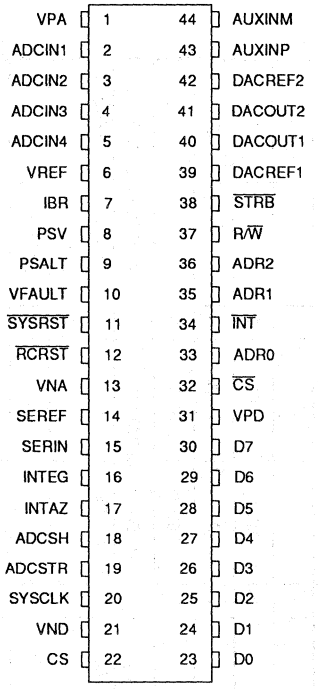
0: INTERRUPT MASK/STATUS			1: SERVO GAIN CONTROL & PRESCALER			2: ADC LSB DATA			3: ADC ADDRESS & MSB DATA		
#	WRITE	READ	#	WRITE	READ	#	WRITE	READ	#	WRITE	READ
0	BURST INT	BURSTRDY	0	SCALE0		0		'0'	0	ADC SEL0	ADC2
1	ADC INT	ADCRDY	1	SCALE1		1		'0'	1	ADC SEL1	ADC3
2			2	GAIN0		2		'0'	2	ADC SEL2	ADC4
3			3	GAIN1		3		'0'	3	ADC CALIB	ADC5
4			4	GAIN2		4		'0'	4		ADC6
5			5	GAIN3		5	SLEEP	'0'	5		ADC7
6			6	BSTSEL0		6	STBEN1	ADC0	6		ADC8
7			7	BSTSEL1		7	STBEN2	ADC1	7		ADC9
4: DAC1 LSB DATA			5: DAC1 MSB DATA			6: DAC2 LSB DATA			7: DAC2 MSB DATA		
#	WRITE	READ	#	WRITE	READ	#	WRITE	READ	#	WRITE	READ
0			0	DAC2 1		0			0	DAC2 2	
1			1	DAC3 1		1			1	DAC3 2	
2			2	DAC4 1		2			2	DAC4 2	
3			3	DAC5 1		3			3	DAC5 2	
4			4	DAC6 1		4			4	DAC6 2	
5			5	DAC7 1		5			5	DAC7 2	
6	DAC0 1		6	DAC8 1		6	DAC0 2		6	DAC8 2	
7	DAC1 1		7	DAC9 1		7	DAC1 2		7	DAC9 2	

FIGURE 5: SSI 32H6520 Embedded Servo Processor Register Map

SSI 32H6521
Embedded Servo Controller

PACKAGE PIN DESIGNATIONS

(Top View)



44-lead SOM

CAUTION: Use handling procedures necessary for a static sensitive component.

ORDERING INFORMATION

PART DESCRIPTION	ORDER NUMBER	PACKAGE MARK
SSI 32H6521 44-pin SOM	32H6521-CM	32H6521-CM

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

Silicon Systems, Inc. 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914

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A TDK Group Company

SSI 32H6810A/6810B
5V Servo & Motor Speed Drivers

Preliminary Data

December 1993

DESCRIPTION

The SSI 32H6810A/6810B Servo/MSC Drivers, a CMOS monolithic integrated circuit housed in a 48-lead TQFP package, operates from a single 5V supply. It provides a fully integrated servo driver and a spindle motor commutator with internal power FETs. The servo driver is intended for use in disk drive head positioning systems employing linear or rotary voice coil motors. The commutator in conjunction with a microprocessor (μP) or digital signal processor (DSP), provides a complete spindle motor speed control system. The device is ideal for use in 5V small-form disk drive applications.

FEATURES

- 48-lead TQPF package
- Internal 1.0A Servo/MSC drivers
- NMOS output stage, no blocking diodes required
- No deadband, low distortion, class-B output for Servo driver
- Gain select switch for a wide dynamic range of servo inputs
- Optimal commutation delay without external components or Hall sensors
- Reduced dv/dt on commutation - no snubber networks required
- Unipolar and Bipolar modes for MSC driver
- Multiple Brake/Retract modes
- Internal precision voltage reference
- Power fault detection with built-in retract circuitry
- Thermal overload protection
- Low power CMOS design with Sleep mode

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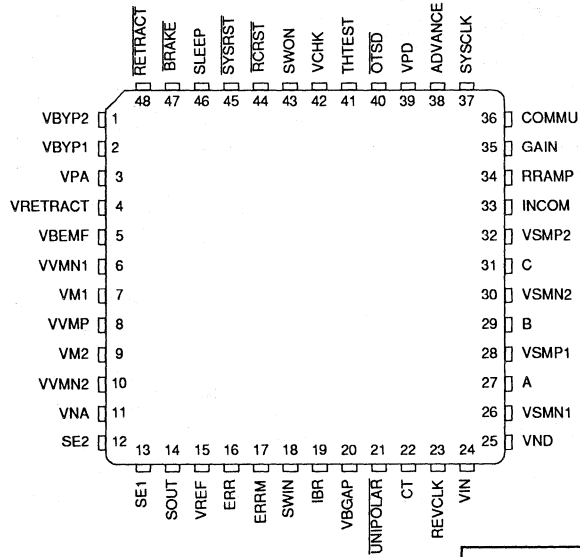
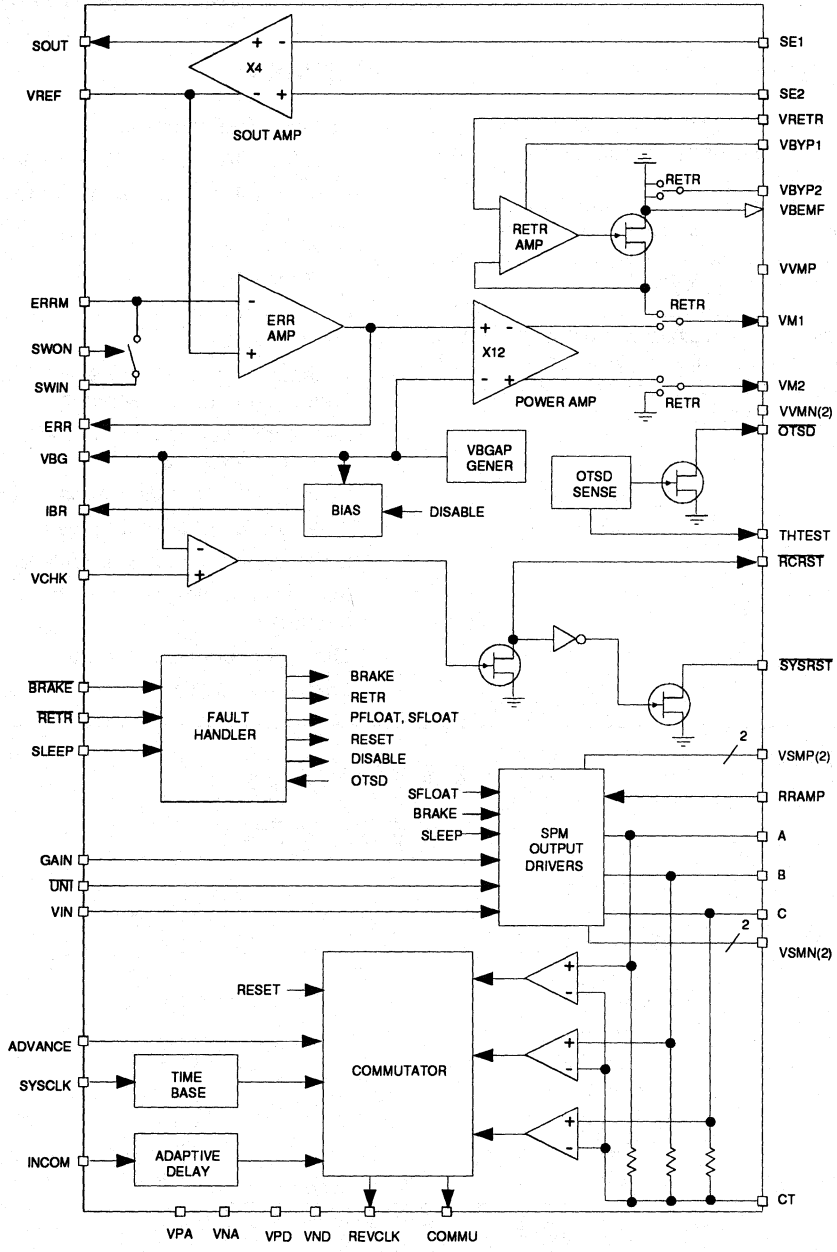
PIN DIAGRAM



48-Lead TQFP

CAUTION: Use handling procedures necessary for a static sensitive component.



BLOCK DIAGRAM

FUNCTIONAL DESCRIPTION

As shown in the block diagram, the SSI 32H6810A/6810B can be divided into three major sections: servo positioner, spindle motor commutator/driver, control circuitry.

SERVO POSITIONER

The servo positioner is a power transconductance amplifier for use in driving a voice coil servo motor (VCM). It has two primary modes of operation, normal (or linear) and retract. The retract mode is activated by a power supply failure or upon an external command per Table 2. Otherwise the device operates in linear mode. The servo positioner consists of SOUT amplifier, ERR amplifier, retract amplifier, power amplifier.

SOUT Amplifier

The SOUT amplifier generates a voltage at SOUT, proportional to positioner current, by sensing the voltage across an external resistor, Rs, amplifying and referencing to VREF. Since the common mode voltage on Rs can range over the full power supply, while the differential voltage is in the order of millivolts, the SOUT amplifier is realized with a high input common mode rejection and low input offset.

ERR Amplifier

The ERR amplifier is a high gain op amp. Due to the fixed gain of the power amp, ERR is proportional to the VCM voltage. The negative input of this amplifier is the system summing junction for the currents which are proportional to the desired VCM current, the measured VCM current, and the VCM voltage.

Power Amplifier

The power amplifier is a fixed gain voltage amplifier with differential inputs and outputs. Its input is the differential voltage between ERR and VBG. Its output drives the VCM directly through an internal NMOS bridge. An internal charge pump generates gate voltages higher than VVMP so the upper NMOS devices can drive VM1 and VM2 up to VVMP. Class B operation is guaranteed by a crossover protection circuitry, which ensures that only one NMOS in each leg of the H-bridge is active.

Retract Amplifier

When a voltage fault is sensed or upon an external command, the servo positioner enters into retract mode. In this mode, it is assumed that no current is available from VVMP. Thus power for this mode comes from VBEMF, from the rectified spindle back emf voltage, and from VBYP1, a voltage generated from the external storage capacitor C_{BYP}. The retract amplifier is powered by VBYP1. It senses the voltage at VRETR and, through a power NMOS source follower, raises VM1 to VRETR. The drain of the source follower is VBEMF.

SPINDLE MOTOR COMMUTATOR/DRIVER

The spindle motor commutator in conjunction with external components provides the motor driving capability for starting, accelerating and rotational speed regulation for brushless DC motors without the need for Hall sensors. Its control is accomplished via ADVANCE, $\overline{\text{RETR}}$, $\overline{\text{BRAKE}}$, SLEEP, GAIN, $\overline{\text{UNI}}$, and INCOM and its operation is monitored via COMMU, REVCLK. The speed regulation control loop is completed with a µP or DSP external to this device.

Commutator

Motor armature position is determined by monitoring the coil voltage of the winding that is not presently being driven by the drivers. The back emf from the coil, in conjunction with the state of the output drivers, indicates the armature position. The back emf is compared with a reference at CT and initiates commutation "events" when the appropriate comparison is made. Commutation is the sequential switching of drive current to the motor windings. Because the back emf comparison event occurs prior to the time when optimum commutation should occur, it is preferred to delay commutation by a predetermined time after the comparison. The commutation delay is provided by a circuitry that measures the interval between comparison events and delays commutation by a time equal to 3/7 of the prior measured interval. The circuit is adaptive and will provide the optimum delay for a wide range of motor speeds (-80% to 50% of the nominal value). Since the commutation of motor coils typically causes transients, the commutation delay circuit also provides a noise blanking function that prevents the circuit from responding back emf comparison events for a period of time equal to 4/7 of the interval between events after the comparison event. The commutation table is described in Table 1.

Motor speed control may be accomplished by measuring the period of the output signal at COMMU.

SPINDLE MOTOR COMMUTATOR/DRIVER (continued)

Transconductance Amplifier

Input pin VIN is the non-inverting input of a transconductance amplifier that uses the lower driver transistor, that is presently active per the commutation state, as the power driver element. An external resistor is used to sense the current flowing through the drive transistor source (and hence the motor coil current). The voltage across the sense resistor is amplified by a gain stage (Av=5 or 10 selected by the GAIN pin) and fed to the inverting input of the transconductance output stage.

Power Amplifier

The output pins A, B and C are intended to drive motor coils directly. The output drivers operate to reduce switching noise transients by limiting dv/dt during commutation. Each output consists of two N-channel MOSFET drivers, one for pull-up to VSMP and one for pull-down to VSMN. The pull-up FET functions as a switch with voltage rise and fall times of about 25 µsec. The pull-down FET is a part of the transconductance amplifier that converts the voltage VIN into motor current (Imotor=VIN/($\overline{\text{RSENSE}}$ Av), where Av is either 5 or 10). When the pull-down output is commutating to the off state, dv/dt on the respective pin is controlled such that dv/dt is approximately 15/RRAMP volts per µsec, where RRAMP is measured in kohms.

Motor Start-up

Motor starting is accomplished by a companion µP or DSP via ADVANCE, SLEEP, $\overline{\text{BRAKE}}$ and COMMU. The commutation counter is reset to state 0 during power-up or upon a µP command asserting SLEEP high. Once it has been reset to this known state 0, the commutation counter can then be incremented by one with each rising edge of subsequent ADVANCE pulses. A typical start-up begins with $\overline{\text{BRAKE}}$ low (by asserting $\overline{\text{RETR}}$ low to ensure the servo head is retracted and the spindle motor is in stationary), SLEEP high (to reset the commutation counter to state 0), and ADVANCE high (to exclude internal commutations), then follows with $\overline{\text{BRAKE}}$ high and SLEEP low. Up to this time, the commutation counter will be state 0, but the lower driver output B remains inactive to prevent current from flowing through the motor (out of A that is high). At the first rising edge of subsequent ADVANCE pulses, the commutation state 1 is selected and the drivers are per Table 1. Note that ADVANCE at logic high excludes internal commutations. COMMU provides feedback to the µP on motor activity.

CONTROL CIRCUITRY

The control circuitry consists of a power fault detector, a thermal overload circuit, and control logic. The inputs to the control circuitry are VCHK, SLEEP, $\overline{\text{RETR}}$, and $\overline{\text{BRAKE}}$, along with the internal signals from the thermal overload detector.

The power fault detector monitors the system power supply Vdd to prevent the VCM driver from responding to a false command during a power failure. The system power supply is applied at VCHK through an external resistor divider and compared with an internal voltage reference at VBG. When a power failure is sensed, the $\overline{\text{SYSRST}}$ is asserted low and the retract mode is activated.

The thermal overload circuit monitors the die temperature to prevent an excessive current flowing through VCM or SPM drivers. If the die temperature exceeds approximately 135°C, the $\overline{\text{OTSD}}$ is asserted low and both drivers are turned off. The drivers will become operative after the temperature is reduced and the ADVANCE is asserted high.

Seven operating modes are selected via SLEEP, $\overline{\text{RETR}}$ and $\overline{\text{BRAKE}}$ (when the system power supply is present) per Table 2. If the system power supply is not present (VCHK<VBG), power for the braking circuitry during retract and spin-down is provided by the charge stored on an external capacitor on VBYP1, power for the retract circuitry is provided by the back emf voltage at VBEMF and the retract circuitry itself is driven by the charge stored on the capacitor between VBPY1 and VBYP2.

STATE	COMMU	Pull-Downs A	B	C	Pull-Ups A	B	C
0, (Reset state)	0	off	on (1)	off	on	off	off
1	1	off	off	on	on	off	off
2	0	off	off	on	off	on	off
3	1	on	off	off	off	on	off
4	0	on	off	off	off	off	on
5	1	off	on	off	off	off	on
(1) B is off in reset state, see text.							

TABLE 1: Commutation States

VCHK>VBGAP	SLEEP	$\overline{\text{BRAKE}}$	$\overline{\text{RETRACT}}$	CONDITION	ANALOG	POSITIONER	A, B, C
0	X	1	X	Power Fault	On	Retract	Float
0	X	0	X	Power Fault	On	Retract	Low Z to GND
1	1	1	1	Sleep	Off	Float	Float
1	1	0	1	Sleep/Brake	Off	Float	Low Z to GND
1	1	0	0	Sleep/Retract	Off	Retract	Low Z to GND
1	1	1	0	Sleep/Retract	Off	Retract	Float
1	0	0	X	Brake/Retract	On	Retract	Low Z to GND
1	0	1	0	Retract (Spindle Run)	On	Retract	Active
1	0	1	1	Run	On	Active	Active
X	X	X	X	Thermal Shutdown	On	Float	Float

TABLE 2: Operating Mode Control

NOTES:
1. $\overline{\text{BRAKE}}$ internally linked to force retract.
2. Voltage fault circuit is never turned off.
3. Counter is reset when sleep input is high.

The circuit also provides an over temperature detection function. If the die temperature exceeds 135°C (approximately), $\overline{\text{OTSD}}$ is asserted low and all output drivers are turned off. The drivers will become operative after the temperature is reduced and ADVANCE is asserted high.

PIN DESCRIPTION

POWER SUPPLIES

NAME	TYPE	DESCRIPTION
VPA	I	Supply: Analog positive power supply.
VNA	I	Ground: Analog ground.
VPD	I	Supply: Digital positive power supply.
VND	I	Ground: Digital ground. VND is circuitry ground and also the low side input to the current SENSE amplifier and thus care should be taken to see that VND and the low side of the external Rsense resistor are at the same potential.
VVMP	I	Supply: Positve supply for voice coil motor.
VVMN1, VVMN2	I	Supply: Negative supply for voice coil motor.

POSITIONER

SWON	I	Turns on the switch between ERRM and SWIN.
SWIN	I	Analog switch, the other side of the switch is connected to ERRM.
SOUT	O	The current sense amplifier output. SOUT is referenced to VREF.
ERR	O	The error amplifier output. ERR is used to provide compensation to the transconductance loop. ERR is referenced to VBGAP.
ERRM	I	The error amplifier negative input.
VREF	I	The reference voltage for the error amplifier and the current sense amplifier.
VRETRACT	I	The retract voltage. If left open, the retract voltage will be the default setting. This value can be over-ridden by biasing VRETRACT externally.
VM1	O	Connection for voice coil motor and sense resistor.
VM2	O	Connection for the other side of voice coil motor.
SE1, SE2	I	Sense voltage on the sense resistor.

MOTOR SPEED CONTROL

SYSCLK	I	System clock (input) pin. SYSCLK is 2 MHz nominal and is used to generate internal timing signals.
COMMU	O	Commutation count pin. COMMU is the LSB of the commutation counter.
REVCLK	O	REVCLK is COMMU divided by six.
UNIPOLAR	I	Unipolar mode (inverse) select pin. This pin will turn all upper drivers off when low. Pulled high internally to provide the default bipolar mode.

MOTOR SPEED CONTROL (continued)

NAME	TYPE	DESCRIPTION
ADVANCE	I	Advance pin. ADVANCE is controlled by microprocessor during start mode to increment the commutation counter. The rising edge of ADVANCE will increment the counter. ADVANCE held high will inhibit internal incrementing of the counter, ADVANCE held low permits the normal operation of commutation from back-emf events.
INCOM	I	Commutation delay control. Adaptive commutation delay may be adjusted from its nominal value of 3/7 of the commutation interval by sinking or sourcing current from this pin. It is recommended that INCOM pin be pulled high during start-up.
VIN	I	Control Voltage input pin. The internal driver transistors and internal predriver circuits form a transconductance amplifier which will set motor current in relation to VIN. In conjunction with Rsense at VSMN input and the gain of the Sense amplifier, transconductance (Gm) will be Gm = Im/VIN =
		1/ (Rsense • 5).
A, B, C	O	Motor Drive Outputs. These pins provide drive to the motor coils.
CT	I	Back EMF input from motor coil center tap. Input connected to the center tap for sensing generated back emf voltages. It is also derived internally from A, B, C through a resistor network (y-connection).The circuit uses the back-emf voltages to determine rotor position and effect commutation.
RRAMP	I	Lower driver turn-off dv/dt setting resistor. External resistor from VPD to this pin sets the dv/dt slope of the motor coil voltage when the lower drivers are commutating to the off state. The dv/dt is given approximately by the relationship dv/dt (volts/second) = 1.5 • 10E10/Rramp. Typical value: RRAMP = 200K.
GAIN	I	Sense amplifier gain control pin. In normal operation, this pin is tied to high to set sense amplifier gain = 5. In low motor current operation, amplifier gain = 10 can be set by tying this input to low.
VSMP1,VSMP2	I	Supply: Positive supply for spindle motor.
VSMN1, VSMN2	I	Supply: Negative for spindle motor. Current monitoring sense amplifier (high side) input pin and motor current returns to ground. **All pins must be connected with low resistance circuit board traces.** The lower driver transistor current (hence motor current) comes out of these pins to Rsense resistor to monitor motor current. During normal (at speed) operation, the circuit will control the voltage across this resistor (multiplied by the gain of 5 in the sense amplifier) to match VIN.
		VVMP, VVMN, VSMP and VSMN conductors must be sized in accordance with anticipated motor current. The analog and digital supplies should be bypassed separately. VPA and VPD should be shorted externally, VNA and VND should be shorted externally.

PIN DESCRIPTION

MISCELLANEOUS

NAME	TYPE	DESCRIPTION
VBYP1	I	The bypassed power supply. An external voltage for BRAKE and RETRACT circuitry. An external capacitor is attached to this pin and an internal circuit will charge this pin to VCC. The charge on this capacitor is used by the brake and retract function when VCC is removed (power-off). The capacitor must hold sufficient charge during the period when VCC is lost while retract is taking place (20 to 50 ms) so it will have enough voltage to drive the outputs during braking. Very little current is used during power-off braking so that C can be chosen from the retract conditions:
		C ≥ Tretract • Ivbyp (float mode) / .5 volt
		or approximately:
		C ≥ 40E-6 • Tretract
		This pin is normally a diode drop below VPA, rising by VBEMF during retract.
VBYP2	I	The other side of the bypass capacitor connection. This pin is normally at VNA, rising to VBEMF during retract.
VBEMF	I	Rectified spindle back emf voltage. This voltage drives the internal retract FET.
SLEEP	I	Sleep pin. When asserted high, internal counters and registers are cleared. Refer to Table 2. Also forces an internal voltage fault which causes a head retract. Disables all output drivers, powers down all other circuitry except the over-temperature and voltage fault circuitry.
RETRACT	I	Retract (inverse) pin. When asserted low, forces a retract. Refer to Table 2.
BRAKE	I	Brake (inverse) pin. BRAKE is used to provide a delay between the initiation of fault-induced head retract and motor braking. A capacitor to ground and a resistor to SYSRST are selected such that 1.2 • R • C is equal to the maximum time required for retract. Refer to Table 2.
OTSD	O	Over-Temperature Sense Detect. Excessive die temperature will bring this open drain output low. Spindle motor and positioner drivers are disabled whenever OTSD is asserted.
VCHK	I	Comparator input for power supply monitoring.
VBGAP	O	An internal voltage reference for use with the power supply monitor comparator.
IBR	O	A resistor is tied from this pin to ground to establish the bias current for internal circuitry.
RCRST	I/O	This pin serves the dual purpose of providing power on reset and stretching short VFAULT pulses to a width suitable for the host microcontroller. An external RC network sets the minimum width of any SYSRST pulse.
SYSRST	O	When low, this open drain output indicates that an internal voltage fault has occured or that RCRST has been pulled low.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Operation above absolute maximum ratings may permanently damage the device.

PARAMETER		RATING
Supply Voltage	VPA, VPD, VVMP, VSMP (1, 2)	-0.3 to 7V -0.3 to 7V
Output Current	Imax (in or out of A, B, C, VM1, VM2)	-1.0 to 1 Amp
Analog I/O	VIN, RRAMP,	-0.3 to VPD + 0.3V
Voltage on pins	CT, A, B, C, VBEMF, VBYP1, VBYP2	-0.3 to 12V
	VM1, VM2, SE1, SE2	-0.3 to 7V
	All other pins	-0.3 to VPD + 0.3V
Storage Temperature	Tstg	-65 to 150°C
Lead Temperature (10 sec duration)	Tlead	0 to 300°C

OPERATING CONDITIONS

Supply Voltage	VPA, VPD VVMP, VSMP	4.5 to 5.5V 4.5 to 5.5V
Supply Current	I (VPA + VPD)	20 mA
	I (VPA + VPD + VVMP + VSMP) Sleep mode	20 mA
	IVVMP	0.4 A
	IVSMP	0.5 A
VBEMF		1 to 10V
VREF		0.5 to VPA-2V
VIN		0 to 2.5V
Vin, VSMN1, VSMN2 *	Normal operation	0 to 0.5V
RF		10 kΩ
RC		10 kΩ
RBIAS		112 to 114 kΩ
Ambient Temperature	Ta	0 to 70°C
Capacitive Load Digital I/O	Cl	0 to 100 pF

* Transconductance gain from VIN to motor current (steady-state) will be given by: G = Imotor/VIN = 1/(Rsense • 5)

OPERATING CONDITIONS (continued)

PARAMETER		RATING
Analog Outputs	Cl	0 to 50 pF
Resistive Load Analog Outputs	Rl	10 kΩ
Power Dissipation	Pd	500 mW

PARAMETRIC REQUIREMENTS

Digital Input/Output

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Fclk, SYSCLK		1.5		2.5	MHz
Twh, Twl, SYSCLK width high or low		40			ns
Input Leakage ($\overline{\text{UNIPOLAR}}$)		-50		10	µA
Input Leakage (all other pins)				10	µA
Vil ($\overline{\text{BRAKE}}$)				1.2	V
Vih ($\overline{\text{BRAKE}}$)		2			V
Vil (all other digital inputs)				0.8	V
Vih (all other digital inputs)		2			V
Output Sink current	Vo = 0.4V	1.6			mA
$\overline{\text{RCRST}}$, $\overline{\text{OTSD}}$					
$\overline{\text{SYSRST}}$	Vo = 0.4V	4			mA

Digital Output COMMU, REVCLK

Voh	Iout = -100 µA	2.4			V
Vol	Iout = 2.0 mA			0.4	V

VIN

Input Current	0 ≤ Vin < 2.5V	-1		+1	µA

Outputs A, B, C

Total voltage drop across power FETs 32H6810A	Imotor = 500 mA, V_{PD} = 4.5V			0.85V	V

CT, And A, B, C, When Not Driving

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Rin	-0.3V ≤ Vin < 7V	5K	9K		Ω
Cin @ CT				20	pF
Cin @ A, B, C				200	pF

VBYP1

IVBYP1 (run)	VDD = 4.5V			100	µA
IVBYP1 (retract)	VDD = 0.5V, VBYP1 = 3V			20	µA
IVBYP1 (brake)	VDD ≤ 0.5V, VBYP1 = 3V			10	µA

BEMF

IBEMF	VBEMF = 4V			300	µA
IBEMF (retract)	I (VM1) = I (VM2) = 0, I (VBYP2) = 0			20	µA

SOUT

Gain		3.9		4.1	V/V
Input Offset	SOUT = VREF	-3		3	mV
Output Swing	R_L = 10 kΩ to VREF	0.15		VP-1	V

ERR

ERRM Input Offset	ERR = ERRM	-15		15	mV
ERR Output Swing		1.55		VP -1.25	V

POSITIONER

(VM1 - VM2) / (ERR - VBGAP)	11		13	V	
Crossover Time	Imotor = 10 mA, PP @ 1 kHz, RL= 16Ω, RSENSE = 0.5Ω		10	25	µs
Output Distortion	Imotor = 100 mA, PP @ 100 Hz RL= 16Ω, RSENSE = 0.5Ω			2	%THD

VBGAP

Bandgap Voltage	Iout < ±0.2 mA	2.13		2.37	V

VCHK

Offset		-15		15	mV

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OUTPUT VM1, VM2

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Total voltage drop across power FETs I = 400 mA				1	V

SWIN

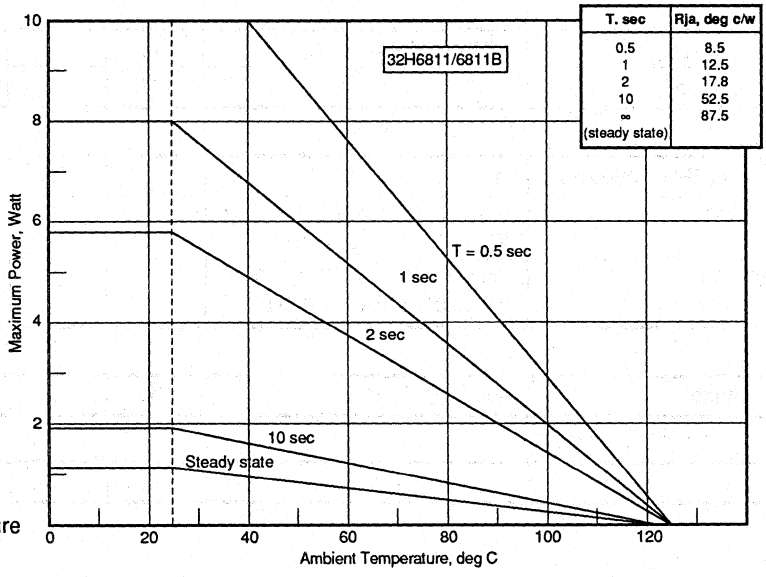
On Resistance				250	Ω

RETRACT

VRETRACT Offset	VRETRACT = 0.1V VBEMF ≥ 1V RL = 16Ω	-100		0	mV
Short Circuit Current	VRETRACT = 0.5V VBEMF = 1V VBYP1 = 4.5V VM1 = VM2	60			mA
	VRETRACT = 0.5V VBEMF = 1.5V VBYP1 = 4.5V VM1 = VM2	100			mA

$\overline{\text{OTSD}}$ (Thermal Shutdown)

Die temperature	125		145	°C	

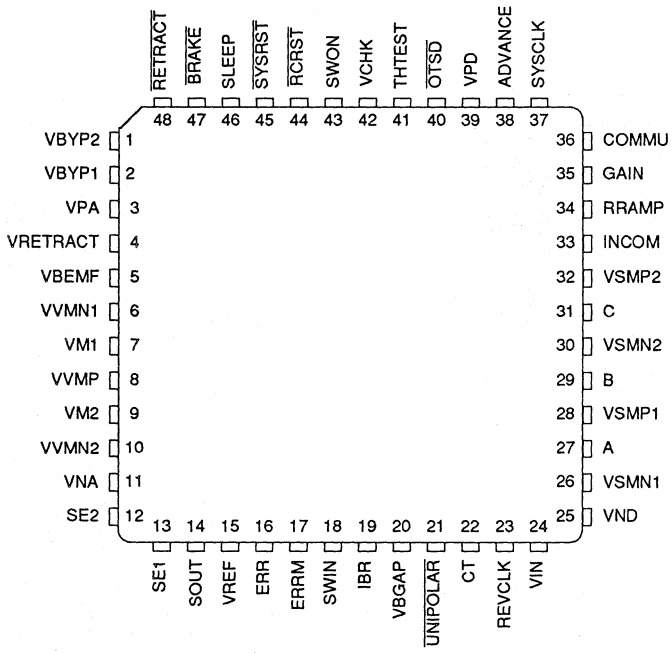


Junction temperature at 125°C is assumed

FIGURE 1: Power Dissipation Derating

PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



48-Lead TQFP

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ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PACKAGE MARK
SSI 32H6810A 48-Lead TQFP	32H6810A-CGT	32H6810A-CGT
SSI 32H6810B 48-Lead TQFP	32H6810B-CGT	32H6810B-CGT

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914

Notes:

silicon systems®
A TDK Group Company

SSI 32H6811/6811B
Servo Motor Speed 5V Driver/DACs

Advance Information

December 1993

DESCRIPTION

The SSI 32H6811/6811B Servo and MSC Drivers, a CMOS monolithic integrated circuit housed in a 64-lead TQFP package, operates from a single 5V supply. It provides a fully integrated servo driver and a spindle motor commutator with internal power FETs. The servo driver is intended for use in disk drive head positioning systems employing linear or rotary voice coil motors. The commutator in conjunction with a microprocessor (μP) or digital signal processor (DSP), provides a complete spindle motor speed control system. It also includes two 10-bit D/A converters, with a serial interface to commonly used μP or DSP, for commanding the servo positioner and the spindle motor respectively. The device is ideal for use in 5V small-form disk driver applications.

FEATURES

- **Internal 1.0A servo driver with no deadband, class-B output**
- **Thermal overload protection**
- **Power fault detection with built-in retract circuitry**
- **10-bit VCM D/A converter with 4 μs digital delay**
- **Gain select switch for a wide dynamic range of servo inputs**
- **Internal precision voltage reference**
- **Programmable commutation delay for optimal motor efficiency**
- **10-bit MSC D/A converter with 4 μs digital delay**
- **Internal 1.0A spindle driver**
- **Switch-mode current limiting for spindle motor start-up**
- **Serial interface compatible with 80C196 and 68HC16**
- **Low power CMOS design with Sloop mode**
- **64-lead TQPF package**

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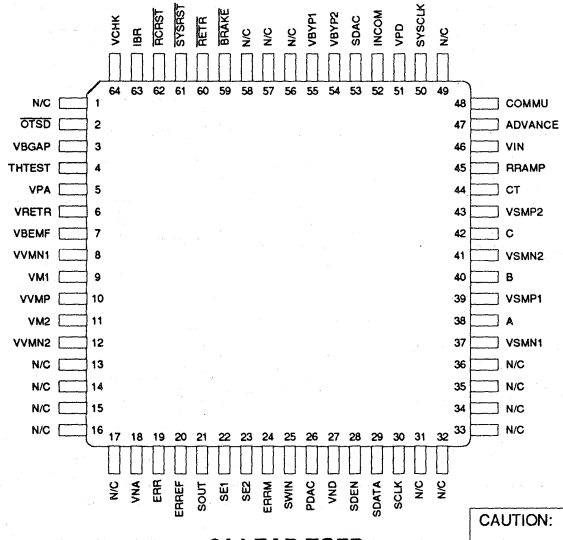
PIN DIAGRAM



64-LEAD TQFP

CAUTION: Use handling procedures necessary for a static sensitive component.

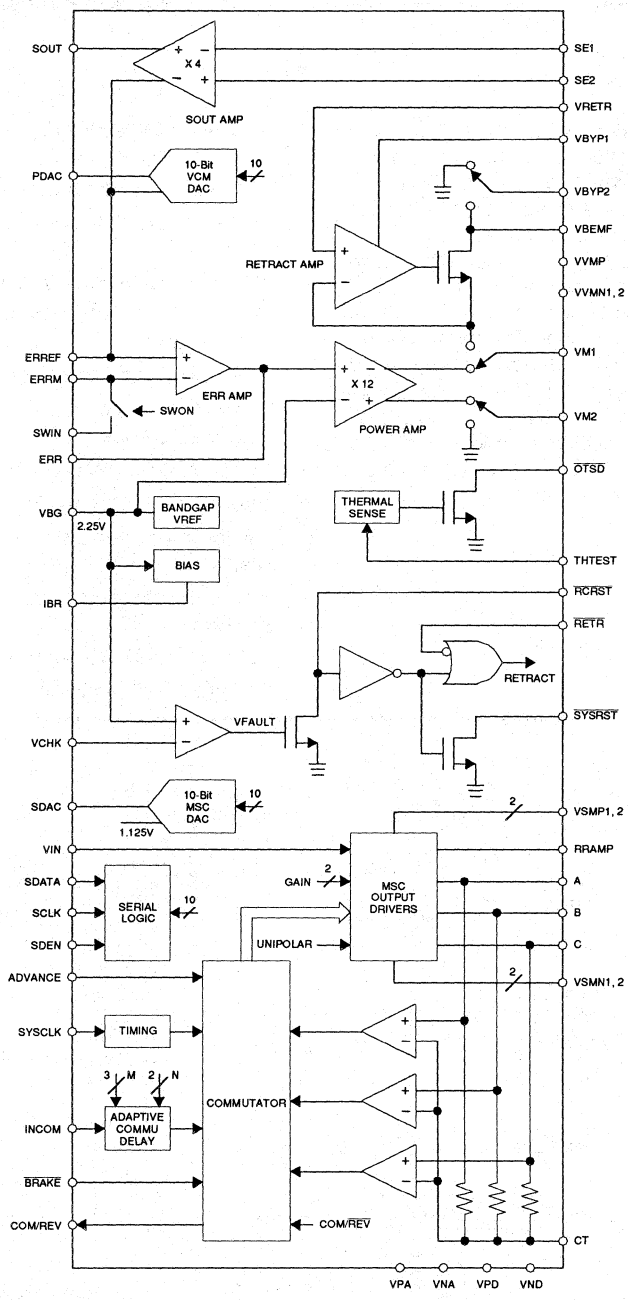


FIGURE 1: SSI 32H6811/6811B Functional Block Diagram

FUNCTIONAL DESCRIPTION

As shown in Figure 1, the SSI 32H6811 can be divided into four major sections: Servo positioner, Spindle motor commutator/driver, Control circuitry and Serial interface port.

Servo Positioner

The servo positioner is a power transconductance amplifier for use in driving a voice coil servo motor (VCM). It has two Primary modes of operation, normal (or linear) and retract. The Retract mode is activated by a power supply failure or when $\overline{\text{RETR}}$ is asserted low while $\overline{\text{BRAKE}}$ being high. Otherwise the device operates in Linear mode. The servo positioner consists of SOUT amplifier, ERR amplifier, retract amplifier, power amplifier and 10-bit VCM D/A converter.

SOUT Amplifier

The SOUT amplifier generates a voltage at SOUT, proportional to positioner current, by sensing the voltage across Rs, amplifying and referencing to ERREF. Since the Common mode voltage on Rs can range over the full power supply, while the differential voltage is in the order of millivolts, the SOUT amplifier is realized with a high input Common mode rejection and low input offset.

ERR Amplifier

The ERR amplifier is a high gain op amp. Due to the fixed gain of the power amp, ERR is proportional to the VCM voltage. The negative input of this amplifier is the system summing junction for the currents which are proportional to the desired VCM current, the measured VCM current, and the VCM voltage.

Power Amplifier

The power amplifier is a fixed gain voltage amplifier with differential inputs and outputs. Its input is the differential voltage between ERR and VBG. Its output drives the VCM directly through an internal NMOS bridge. An internal charge pump generates gate voltages higher than VVMP so the upper NMOS devices can drive VM1 and VM2 up to VVMP.

Retract Amplifier

When a voltage fault is sensed, or when $\overline{\text{RETR}}$ is asserted low while $\overline{\text{BRAKE}}$ being high, the servo positioner enters into Retract mode. In this mode, it is assumed that no current is available for VVMP. Thus power for this mode comes from VBEMF, the rectified spindle back emf voltage, and from VBYP1, a voltage generated from an external storage capacitor CBYP. The retract amplifier is powered by VBYP1. It senses the voltage at VRETR and, through a power NMOS source follower, raises VM1 to VRETR. The drain of the source follower is VBEMF.

VCM D/A Converter

Switched-capacitor circuit technique is employed to implement the VCM D/A converter with two non-overlapped clock phases, one phase for auto-zeroing and another one for evaluation. These two phases run synchronously with an internal 250 kHz clock, which is derived directly from the system clock at SYSCLK.

The request of the VCM D/A converter is initiated by writing to the VCM D/A register (00) through the serial interface port. The input data word must be coded in two's complement form. Note that there would be a maximum of 2 µsec of latency between a conversion request and the actual start of conversion. The conversion delay from the actual start of conversion to when the analog output begins to slew to a new value is 2 µsec. Therefore a maximum of 4 µsec is required for a conversion in addition to the time needed for completion of a serial data transfer, which is equal to 16/SCLK.

The VCM D/A converter provided at PDAC is referenced to ERREF, which also serves as a reference voltage for the error amplifier and the current sense amplifier.

Spindle Motor Commutator/Driver

The spindle motor commutator in conjunction with external components provides the motor driving capability for starting, accelerating and rotational speed regulation for brushless DC motors without the need for Hall sensors. The speed regulation control loop is completed with a µP or DSP external to this device.

Commutator

Motor armature position is determined by monitoring the coil voltage of the winding that is not presently being driven by the drivers. The back EMF from the coil, in conjunction with the state of the output drivers, indicates the armature position. The back EMF is compared with a reference at CT and initiates commutation is compared with a reference at CT and initiates commutation "events" when the appropriate comparison is

made. Commutation is the sequential switching of drive current to the motor windings. Because the back comparison should occur, it is preferred to delay commutation by a predetermined time after the comparison. There are two modes of commutation delay, namely adaptive or one-shot, which can be selected via the M, N bits in the mode register (10) per table 1. In Adaptive mode (default), the commutation delay is provided by a circuit which measures the interval between comparison events and delays commutation by a time equal to 3/7 of the prior measured interval. The circuit is adaptive and will provide the optimum delay for a wide range of motor speeds (-80% to 50% of the nominal value). Since the commutation of motor coils typically causes transients, the commutation delay circuit also provides a noise blanking function which prevents the circuit from responding back EMF comparison events for a period of time equal to the maximum of 5/7 of the interval between events and 64 µs after the comparison event. INCOM pin can be selected as a test pin if it is high impedance, otherwise it should be selected as "IN" for the Adaptive mode to work properly.

In one-shot mode, an input voltage at INCOM pin will provide a fixed delay and noise blank. For start-up, INCOM = VDD/2 is recommended; delay will be about 500 microseconds and noise blank about 850 microseconds. The commutation table is described in Table 2.

Motor speed control may be accomplished by measuring the period of the output signal at COM/$\overline{\text{REV}}$. COM/REV may be defined as either COMMU, the LSB of the commutation counter, or REVCLK, the revolution clock of the motor, selected via the bit COM/REV in the mode register (10).

Transconductance Amplifier

Input pin VIN is the non-inverting input of a transconductance amplifier which uses the lower driver transistor, that is presently active per the commutation state, as the power driver element. An external resistor is used to sense the current flowing through the drive transistor source (and hence the motor coil current). The voltage across the sense resistor is amplified by a gain stage (Av = 5, 10, 20 or 30 selected by the GAIN bits in the MODE register) and fed to the inverting input of the transconductance output stage.

The 10-bit MSC D/A converter, referenced to VBG/2, is provided at SDAC for converting the commanding signal in digital format into an analog voltage. Its operation is similar to the VCM D/A converter, but is initiated by writing to the MSC D/A register (01) in two's complement form.

Power Amplifier

The output pins A, B and C are intended to drive motor coils directly. The output drivers operate to reduce switching noise transients by limiting dv/dt during commutation. Each output consists of two N-channel MOSFET drivers, one for pullup to VSMP1 or VSMP2 and one for pulldown to VSMN1 or VSMN2. The pullup FET functions as a switch (1.5Ω maximum) with voltage rise and fall times of about 25 microseconds. The pulldown FET is a part of the transconductance amplifier which converts the voltage VIN into motor current (Imotor = VIN/(Rsense • Av), where Av is either 5, 10, 20 or 30). When the pulldown output is commutating to the off state, dv/dt on the respective pin is controlled such that dv/dt is approximately 15/RRAMP volts per microseconds, where RRAMP is measured in kohms.

TABLE 1: Modes of Commutation Delay

MODE REGISTER (10) M	N	SWITCH MODE	DELAY MODE	INCOM PIN
0	0	NO	Adaptive	Test (default)
0	1,2	NO	Adaptive	In
0	3	NO	Adaptive	In
>0	X	YES	One Shot	In

Motor Start-Up

Motor starting is accomplished by a companion µP or DSP via ADVANCE, $\overline{RETR}$, $\overline{BRAKE}$ and COM/REV. The µP can assert $\overline{RETR}$ and $\overline{BRAKE}$ low to initialize the commutation counter and then increment the counter with ADVANCE. After $\overline{RETR}$ and $\overline{BRAKE}$ are asserted low and de-asserted (the power-up condition for preparation to begin a starting sequence), the commutation state will be state 0 per TABLE 1, but the lower driver output B remains inactive to prevent current flowing through the motor (out of A which is high). On the first ADVANCE set high, the commutation state 1 is selected and the drivers are per TABLE 1. ADVANCE at logic high excludes internal commutations. COMMU provides feedback to the µP on motor activity.

Switch-Mode Operation

Switch-mode operation is provided for limiting the motor current during motor start-up. Two values M and N, loaded into the mode register (10) through the serial interface, determines the basic switching parameters for the operation. The M (3 bits) sets the minimum "on" time of the lower drivers and sample delay time. The N (2 bits) sets the switching period. The timing is given by:

Minimum "on" time = (M+1) • 4.5 µs

Sample delay time = M • 4.5 µs

Switching period = (N+2) • (M+1) • 4.5 µs

Hence, Minimum duty cycle = 1/(N+2)

Sample delay time, defined as the time from turning the lower drivers "on" until switching transients have settled, is a function of the particular application and will be determined by the user.

The value of M=0 is defined as Linear mode, no switching except normal commutation will occur.

Switch-Mode Operation (continued)

For a proper switch-mode operation, three flyback diodes from outputs A, B, and C, and a blocking diode from the system power supply VCC to the VSMP1 and

		Pullups			Pulldowns		
STATE	COMMU	A	B	C	A	B	C
0	0	OFF	ON	OFF	ON	OFF	OFF
1	1	OFF	OFF	ON	ON	OFF	OFF
2	0	OFF	OFF	ON	OFF	ON	OFF
3	1	ON	OFF	OFF	OFF	ON	OFF
4	0	ON	OFF	OFF	OFF	OFF	ON
5	1	OFF	ON	OFF	OFF	OFF	ON

TABLE 1: Commutation States

$\overline{OTSD}$	VCHK > VBG	$\overline{RETR}$	$\overline{BRAKE}$	Mode	Analog	Counter	VCM Driver	MSC Driver
0	x	x	x	Shutdown	ON	Active	Float	Float
1	0	x	0	Fault/Break	OFF	Active	Retract	Low Z
1	0	x	1	Fault/Retract	OFF	Active	Retract	Float
1	1	0	0	Sleep	OFF	Reset	Float	Float
1	1	0	1	Retract	ON	Active	Retract	Float
1	1	1	0	Brake	ON	Active	Float	Low Z
1	1	1	1	Run	ON	Active	Active	Active

TABLE 2: Mode of Operations

VSMP2 pins are required. The flyback diodes will provide power for retract (during power failure) at pins VSMP1 and VSMP2.

Control Circuitry

The control circuitry consists of a power fault detector, a thermal overload circuit, and control logic. The inputs to the control circuitry are VCHK, $\overline{\text{RETR}}$, and $\overline{\text{BRAKE}}$, along with the internal signals from the thermal overload detector. The voltage fault detector monitors the system power supply VCC to prevent the VCM driver from responding to a false command during a power failure. The system power supply is applied at VCHK through an external resistor divider and compared with an internal voltage reference at VBG.

Four operating modes are selected via $\overline{\text{RETR}}$ and $\overline{\text{BRAKE}}$ (when the system power supply is present) per Table 2. With $\overline{\text{RETR}}$ and $\overline{\text{BRAKE}}$ asserted low, the VCM drivers are in a high impedance state, the MSC driver outputs A, B, and C are low impedance to ground (without current limiting), and analog circuits are de-biased. This is the "Sleep" mode. It also provides dynamic braking to the spindle motor. With $\overline{\text{RETR}}$

BIT	NAME	DESCRIPTION
0 (LSB)	R/W	Read/Write control. It must be '0' for this device since all of its registers are write only.
1, 2, 3	DID0..2	Device ID. These three bits define the SSI device for which the serial communication is to be established. '111' is designated for this device.
4, 5	ADDR0..1	Register address. These two bits define the internal register to which data is transferred.

ADDR1	ADDR0	Register
0	0	VCM D/A
0	1	MSC D/A
1	0	Mode
1	1	Reserved

The mode register (10) is defined as:		
0	SWON	Analog switch enable
1, 2	GAIN0, 1	Sense amplifier gain select, default 0,0

GAIN1	GAIN0	Gain
0	0	30
0	1	20
1	0	10
1	1	5

3	UNIPOLAR	Unipolar mode enable
4	N0	LSB of N value - minimum duty cycle
5	N1	MSB of N value
6	M0	LSB of M value - sample delay time
7	M1	M value
8	M2	MSB of M value.
9	COM/$\overline{\text{REV}}$	Select COMMU (=0) or REVCLK (=1)

asserted, $\overline{\text{BRAKE}}$ de-asserted, both VCM and MSC drivers are in a high impedance state, and the retract amplifier is activated and powered by the back emf of a spinning motor for retracting heads. For $\overline{\text{BRAKE}}$ asserted, and $\overline{\text{RETR}}$ de-asserted, the VCM drivers are in a high impedance state, the MSC driver outputs are low impedance to ground (without current limiting), and analog circuits are biased. Normal mode is given for $\overline{\text{RETR}}$ and $\overline{\text{BRAKE}}$ de-asserted.

When a power failure is sensed, the $\overline{\text{SYSRST}}$ is asserted low and the Retract mode is activated. If the die temperature exceeds approximately 135 °C, the $\overline{\text{OTSD}}$ is asserted low and all output drivers (both VCM and MSC) are turned off. The drivers will become operative after the temperature is reduced and the ADVANCE is asserted high.

Serial Interface Port

A synchronous serial port, compatible with the commonly used µP such as 80C196 and 68HC16, is used to input digital words for D/A converters and mode registers. It is shift register based I/O interface and consists of three pins SDEN, SCLK and SDATA. Data from uP is transferred 8 bits (one byte) at a time with the LSB first. A complete transfer requires two bytes which are formatted into an instruction and a data field.

Data received through SDATA is clocked into an internal 16-bit shift register at the rising edge of SCLK while SDEN is active high. At the end of each transfer, SDEN must return low. If SDEN remains high after the last bit (which is the MSB of the second byte) is received, any additional data on SDATA will be ignored. Data must be two bytes for each transfer. If, for any reasons, SDEN is brought low prior to the completion of the second byte, the write operation of the data will be aborted.

The instruction field includes the first six bits of the first byte and is defined per the table below. The data field is 10-bit wide and includes the last two bits of the first byte and the second byte.

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PIN DESCRIPTION

POWER SUPPLIES

NAME	TYPE	DESCRIPTION
VPA		Analog positive supply.
VNA		Analog ground.
VPD		Digital positive supply. It should be shorted externally with VPA.
VND		Digital ground. It should be shorted externally with VNA. VND is also the low side input to the current sense amplifier of the spindle motor and thus care should be taken to keep VND and the low side of the external resistor Rsense at the same potential.
VVMP *		Positive supply used for voice coil motor.
VVMP1, 2		Negative supply used for voice coil motor.
VSMP1, 2		Positive supply used for spindle motor.
VSMN1, 2		Negative supply used for spindle motor. They are also the high side inputs to the current sense amplifier of the spindle motor.

* The circuit board contacts for VVMP, VVMN1, VVMN2, VSMP1, VSMP2, VSMN1, and VSMN2 must be sized in accordance with anticipated motor currents. All pins must be connected with low resistance circuit board traces.

SERVO POSITIONER

SWIN	I	The analog switch input. The other side of the switch is connected to ERRM.
ERRM	I	The inverting input of the error amplifier.
ERREF	I	The reference voltage for the error amplifier, the VCM D/A converter and the current sense amplifier.
ERR	O	The error amplifier output. ERR is to provide compensation to the transconductance loop and is reference to VBG.
SOUT	O	The current sense amplifier output. SOUT is referenced to ERREF.
VRETR	I	The retract voltage. If left open, the retract voltage will be the default setting. Otherwise, it can be over-ridden by biasing VRETR externally.
VBYP1	I	The bypassed power supply. An external capacitor is connected to this node to store charge for use by the retract circuitry. This pin is normally a diode drop below VCC, rising by VBEMF during retract.
VBYP2	I	The other side of the bypass capacitor is connected to this pin. It is normally at ground, rising to VBEMF during retract.
VBEMF	I	Rectified spindle back emf voltage. This input provides current to the internal retract power amplifier.

SERVO POSITIONER (continued)

NAME	TYPE	DESCRIPTION
VM1	O	One side of the voice coil motor.
VM2	O	The other side of the voice coil motor and sense resistor combination.
SE1,SE2	I	The voltage across the sense resistor for the voice motor current.
$\overline{\text{RETR}}$	I	When asserted low, it forces a retract. Refer to Table 2.
PDAC	O	The 10-bit VCM D/A converter output. It is referenced to ERREF.

SPINDLE MOTOR COMMUTATOR/DRIVER

SYSCLK	I	System clock input. SYSCLK is internally divided by a divider to generate an internal clock at 2 MHz.
COM/REV	O	When the COM/$\overline{\text{REV}}$ bit in the mode regsiter is low, this pin is defined as the LSB of the commutation counter. Otherwise, it is defined as the revolution clock of the spindle motor.
ADVANCE	I	ADVANCE is used to increment the commutation counter externally. The rising edge of ADVANCE will increment the counter by 1. When held high, it inhibits the counter from internal incrementing. When held low, it permits the normal operation of commutation from back emf events.
INCOM	I	Commutation delay control. Adaptive commutation delay may be adjusted from its nominal value of one half the commutation interval by sinking or sourcing current from this pin. This should be done via an external control loop which can compensate for the range of internal circuit parameter variations.
SDAC	O	The 10-bit MSC D/A converter output. It is referenced to VBG/2.
VIN	I	Control voltage input. The combination of the MOSFET drivers and the predriver circuit forms a transconductance amplifier which sets the motor current in relation to VIN. In conjunction with Rsense connected at VSMN and the gain of the sense amplifier, the transconductance is defined by: Gm = Im/VIN = 1/($\overline{\text{Rsense}}$ • 4)
A, B, C	O	Spindle motor driver outputs.
CT	I	Back emf input from spindle motor coil center tap. Internal circuit uses the back emf voltages to determine the rotor position and effect commutation.
RRAMP	I	Lower driver turn-off dv/dt setting resistor. External resistor from VPA to this pin sets the dv/dt slope of the motor coil voltage when the lower drivers are commutating to the off state. The dv/dt is approximately given by the relationship: dv/dt=15/RRAMP, where dv/dt is expressed in volts/µs and RRAMP in kΩ.
$\overline{\text{BRAKE}}$	I	$\overline{\text{BRAKE}}$ is used to provide a delay between the initiation of fault-induced head retract and spindle motor braking. A capacitor to ground and a resistor to $\overline{\text{SYSRST}}$ are selected such that 1.2RC is equal to the maximum time required for retract.

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CONTROL CIRCUITRY

NAME	TYPE	DESCRIPTION
VCHK	I	Comparator input for power supply monitoring. When VCHK is below VBG, an internal voltage fault is generated.
VBG	O	Voltage reference, generated from the internal bandgap voltage, for use with the power supply monitor comparator.
IBR	O	A resistor is tied from this pin to ground to establish a bias current for internal circuitry.
$\overline{\text{RCRST}}$	O/C	This pin serves the dual purpose of providing power-on-reset and stretching short internal VFAULT pulses to a width suitable for the host micro controller. An external RC network sets the minimum width of any $\overline{\text{SYSRST}}$ pulse. If $\overline{\text{RCRST}}$ is pulled low by external circuitry, this device will enter into the Retract mode and pull $\overline{\text{SYSRST}}$ low.
$\overline{\text{SYSRST}}$	O/C	When low, this open-collector output indicates that an internal voltage fault has occurred.
$\overline{\text{OTSD}}$	O/C	Thermal shut-down. When low, this open- collector output indicates that the junction temperature has exceeded the recommended operating range and the device is in thermal shut-down. In thermal shut-down, all output drivers are turned off and analog circuit de-biased.
THTEST	I	Biased low with an internal pull-down. When asserted high, $\overline{\text{RETR}}$ will be connected to the thermal overload test circuitry for use as a test input.

SERIAL INTERFACE PORT

SDATA	I	Serial data input passing digital words for internal registers.
SCLK	I	Serial data timing reference. The rising edge of the SCLK is to strobe SDATA while SDEN is asserted high.
SDEN	I	Serial data transfer enable. When active high, the serial data transfer is enabled.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device or affect device reliability.

PARAMETER		RATING
Supply voltage @ VPA, VPD, VVMP, VSMP1, VSMP2	Vdd-0.3	7.0 V
Motor current @ A, B, C, VM1, VM2	Imax	±1.0 A
Input voltage @ VIN, RRAMP	Vin	-0.3 to VDD + 0.3 V
Input voltage @		
CT, A, B, C, VBEMF, VBYP1, VBYP2		-0.3 to 12.0 V
VM1, VM2, SE1, SE2		-0.3 to 7.0 V
Other pins		-0.3 to Vdd V
Storage temperature	Tstg	-65 to 150°C
Lead temperature (10 sec duration)	Tlead	0 to 300 °C

RECOMMENDED OPERATING CONDITIONS

The recommended operating conditions for the device are indicated in the table below. Performance specifications do not apply when the device is operated outside the recommended conditions.

PARAMETER		MIN	NOM	MAX	UNIT
Supply voltage	Vdd	4.5		5.5	V
Supply current					
VPA,VPD	Idd			25	mA
Sleep mode	Isleep			1.0	mA
VBYP1,braking	Ibrk			10	µA
VBYP1,retract	Iret			20	µA
Input voltage @ VBEMF		1.0		10	V
Input voltage @ ERREF		0.5	VBG	VDD-2.0	V
Input voltage @ VIN		0		2.5	V
Ambient temperature	Ta	0		70	°C
Capacitive load on digital outputs	Cl			100	pF

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RECOMMENDED OPERATING CONDITIONS (continued)

PARAMETER	SYMBOL	MIN	NOM	MAX	UNIT
Analog output load	Cl			40	pF
	Rl	10			kΩ
System clock					
Frequency tolerance	*fc*	6		10	MHz
Pulse width	Twh, Twl	40			ns
Biasing resistor Rbias = 22.6 kΩ	Rbias	22		24	kΩ
External resistors	Rf,Rc	10			kΩ
Power dissipation	Pd			500	mW

PERFORMANCE SPECIFICATIONS

DIGITAL I/O

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Digital input @ SDATA, SCLK, SDEN, ADVANCE, SYSCLK, $\overline{\text{RETR}}$					
Vil		0.8			V
Vih				2.0	V
Iil, Iih				±10	µA
Digital input @ $\overline{\text{BRAKE}}$					
Vil		1.2			V
Vih				2.0	V
Iil, Iih				±10	µA
Digital O/C output @ $\overline{\text{RCRST}}$, $\overline{\text{SYSRST}}$, $\overline{\text{OTSD}}$					
Ioh	Voh = Vdd			10	µA
Iol	Vol = 0.4	4			mA
Digital Output @ COM/REV					
Vol	Iol = 2.0 mA			0.4	V
Voh	Ioh = -100 µA	2.4			V

SERVO POSITIONER

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
BEMF current					
Normal mode	VBEMF = 4V			300	µA
Retract mode	VBEMF = 3V, Imotor = 0			20	µA
	IVBYP2 = 0				
SOUT amplifier					
Gain		3.9		4.1	V/V
Input offset	SOUT = VBG	-3		3	mV
Output swing	R_L = 10 kΩ to ERREF	0.15		VDD-1	V
ERRAMP amplifier					
Input offset	ERR = ERRM			±15	mV
Output swing		0.15		VDD-1.25	V
Gain		60			dB
Unit Gain Bandwidth	ERR = ERRM	-15		15	mV
Power amplifier (VCM Driver)					
Gain (VM1-VM2)/(ERR-VBG)		11		13	V/V
Output voltage drop	R_L = 16Ω Tj = 25°C,	0.4		0.6	A/V
	Imotor = 0.2A				
Bridge crossover time					
Ivcm = 10 mA, pp @ 1 kHz	R_L = 16Ω			25	µs
VCM output THD					
Ivcm=100 mA, pp @ 100 Hz	R_L = 16Ω			2	%
SWIN on resistance				250	Ω
Retract amplifier (retract), VRETR = 0.5V, VBEMF > 1V, R_L = 16Ω					
offset		-100		0	mV
VRETR		-1		1	µA
Maximum output current, VRETR = 0.5V, VBYP1 = 4.5V					
VBEMF = 1V, VM1 = VM2		60			mA
VBEMF = 1.5V, VM1 = VM2		100			mA
Retract Amplifier (normal)				±10	µA
VRETR leakage					

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SPINDLE MOTOR COMMUTATOR/DRIVER

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Tshift, Shift Range in commu delay	INCOM = 0 to 0.8V 8-pole Motor @ 3600 rpm			±15	%
Input current @ VIN	0 < VIN < 2.5V			±1	µA
Total FETs voltage drop	Imotor = 0.5A			0.85	V
Outputs @ CT, A, B, C while not driving					
Rin	-0.3V < Vin < 7V	10			kΩ
Cin	CT			20	pF
Cin	A, B, C			200	pF

CONTROL CIRCUITRY

Vdd voltage for $\overline{\text{SYSRST}}$ & $\overline{\text{RCRST}}$ in operation		2		5.5	V
VBG	Iout < +0.2 mA	2.13		2.37	V
VCHK comparator offset				±15	mV
Thermal shutdown					
Temperature threshold			125		°C
Hysteresis			5		°C

D/A CONVERTER

Full-scale voltage			VBG		V
Resolution			10		bits
Digital Delay				4	µs
LSB volatge			VBG/1024		V
Differential nonlinearity				±1	LSB
ERREF			VBG/2	VBG	V

SERIAL INTERFACE PORT

SDEN setup time prior to SCLK	Tsens	35			ns
SDEN hold time after SCLK	Tsenh	50			ns
SDATA setup time prior to SCLK rise	Tds	15			ns
SDATA hold time after SCLK fall	Tdh	15			ns
SCLK pulse width	Tpw	100			ns

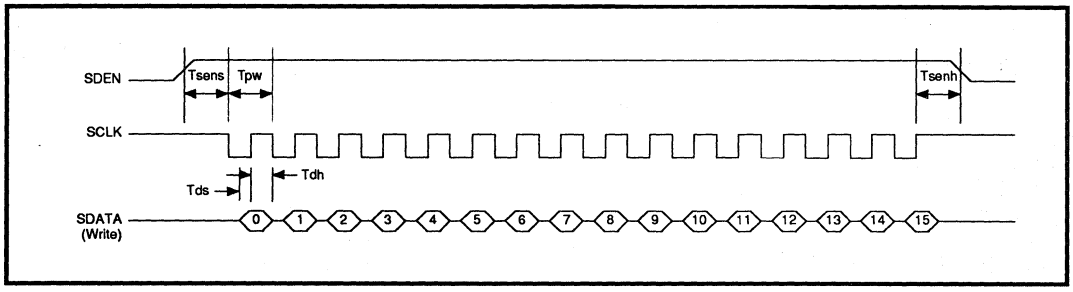


FIGURE 2: SSI 32H6811 Serial Interface Timing Diagram

APLICATIONS INFORMATION

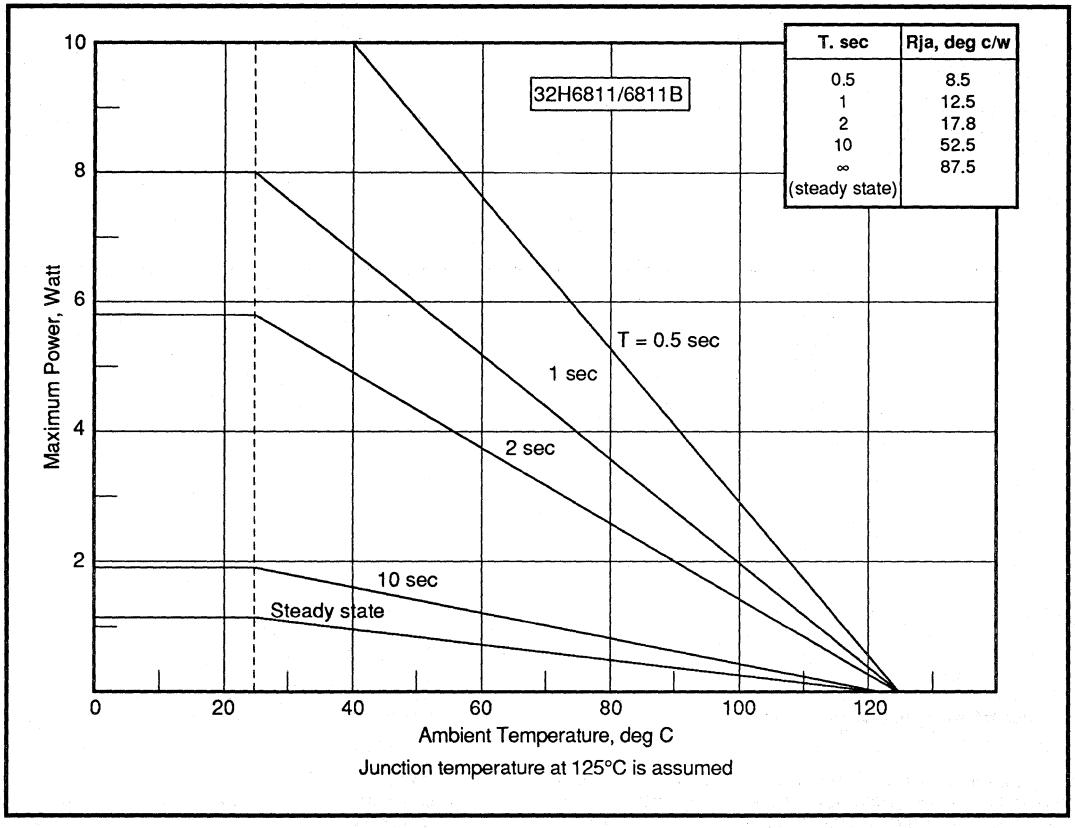
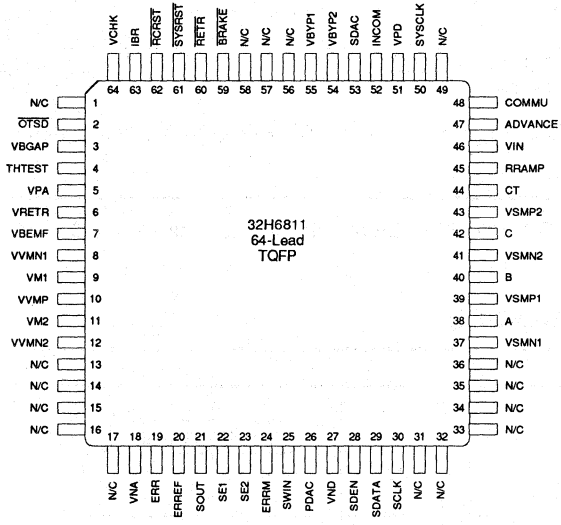


FIGURE 3: Power Dissipation Derating

SSI 32H6811/6811B
Servo Motor Speed
5V Driver/DACs

PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



64-LEAD TQFP

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914

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A TDK Group Company

SSI 32H6812
Servo & Spindle Driver with Shock Detection

Advance Information

November 1993

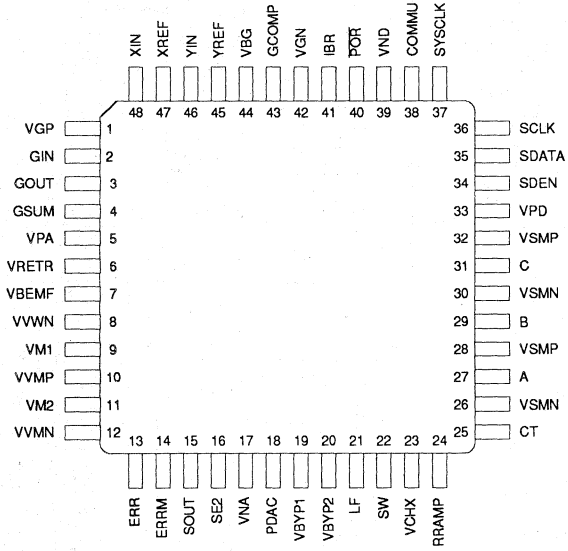
DESCRIPTION

The 32H6812 Servo/MSC Driver, a CMOS monolithic integrated circuit housed in a 48-lead TQFP package, operates from a single 5V supply. It provides a fully integrated servo driver and a spindle motor speed controller with internal power FETs. The servo driver is intended for use in disk drive head positioning systems employing linear or rotary voice coil motors. The spindle driver in conjunction with a microprocessor (μP) or digital signal processor (DSP), provides a complete spindle motor speed control system. It also includes one 10-bit D/A converter, a serial interface compatible with commonly used μP or DSP, and power fault circuitry. The device is ideal for use in 5V small form-factor disk drive applications and is available in a 48-Lead TQFP package.

FEATURES

- **48-lead TQPF package**
- **Internal 1A servo driver with no deadband, class-B output**
- **Power fault detection with built-in retract circuitry**
- **10-bit VCM D/A converter with 4 μs digital delay**
- **Internal precision voltage reference**
- **Programmable commutation delay for optimal motor efficiency**
- **Closed loop speed control at 5400 rpm**
- **Internal 1A spindle driver**
- **Serial interface compatible with Intel 80C196 and Motorola 68HC16**
- **Low power CMOS design with Sleep mode**
- **Internal shock detection circuitry**

PIN DIAGRAM



48-Lead TQFP

CAUTION: Use handling procedures necessary for a static sensitive component.

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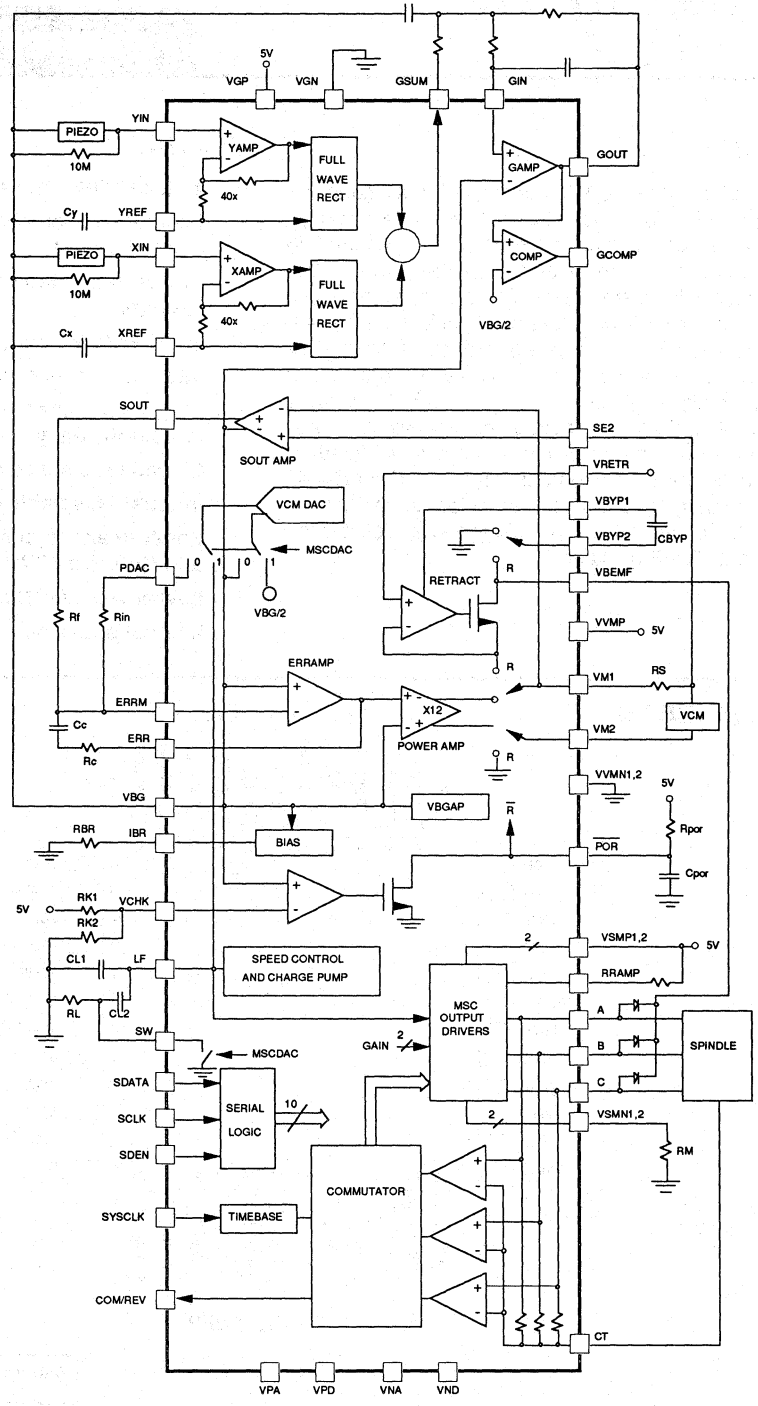
BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

As shown in the block diagram, the 32H6812 can be divided into four major sections: servo positioner, spindle motor speed controller/driver, control circuitry and serial interface port.

SERVO POSITIONER

The servo positioner is a power transconductance amplifier for use in driving a voice coil servo motor (VCM). It has two primary modes of operation, normal (or linear) and retract. The retract mode is activated by a power supply failure or when $\overline{\text{RETR}}$ bit is asserted low with $\overline{\text{BRAKE}}$ (bit) being high. Otherwise the device operates in linear mode. The servo positioner consists of SOUT amplifier, ERR amplifier, retract amplifier, power amplifier and 10-bit VCM D/A converter.

SOUT Amplifier

The SOUT amplifier generates a voltage at SOUT proportional to positioner current, by sensing the voltage across an external resistor Rs, amplifying it and referencing it to VBG. Since the common mode voltage on Rs can range over the full power supply, while the differential voltage is in the order of millivolts, the SOUT amplifier is realized with high input common mode rejection and low input offset.

ERR Amplifier

The ERR amplifier is a high gain op amp. Due to the fixed gain of the power amp, ERR is proportional to the VCM voltage. The negative input of this amplifier is the system summing junction for the currents which are proportional to the desired VCM current, the measured VCM current, and the VCM voltage.

Power Amplifier

The power amplifier is a fixed gain voltage amplifier with differential inputs and outputs. Its input is the differential voltage between ERR and VBG. Its output drives the VCM directly through an internal NMOS bridge. An internal charge pump generates gate voltages higher than VVMP so the upper NMOS devices can drive VM1 and VM2 up to VVMP.

Retract Amplifier

When a voltage fault is sensed, or when $\overline{\text{RETR}}$ bit is asserted low while $\overline{\text{BRAKE}}$ bit is high, the servo positioner enters into Retract mode. In this mode, it is assumed that no current is available for VVMP. Thus power for this mode comes from VBEMF, the rectified spindle back emf voltage, and from VBYP1, a voltage generated from the external storage capacitor CBYP. The retract amplifier is powered by VBYP1. It senses the voltage at VRETR and, through a power NMOS source follower, raises VM1 to VRETR. The drain of the source follower is VBEMF.

VCM D/A Converter

Switched-capacitor circuitry is employed to implement the VCM D/A converter with two non-overlapped clock phases, one phase for auto-zeroing and another one for evaluation. These two phases run synchronously with an internal 500 KHz clock, which is derived directly from the system clock at SYSCLK.

The request of the VCM D/A converter is initiated by writing to the VCM D/A register (00) through the serial interface port. The input data word must be coded in two's complement form. Note that there would be a maximum of 2 µs of latency between a conversion request and the actual start of conversion. The conversion delay from the actual start of conversion to when the analog output begins to slew to a new value is 2 µs. Therefore a maximum of 4 µs is required for a conversion, in addition to the time needed for completion of a serial data transfer, which is equal to 16/SCLK.

When MSCDAC bit in the MSC_MODE register is low (default), VCM D/A converter output is provided at PDAC and is referenced to VBG. VBG also serves as a reference voltage for the error amplifier and the current sense amplifier. If MSCDAC bit is asserted high, D/A converter output will be switched to LF pin and referenced to VBG/2.

SPINDLE MOTOR SPEED CONTROLLER/DRIVER (CONTINUED)

The spindle motor speed controller in conjunction with a µP or DSP and external components provides the motor driving capability for starting, accelerating and rotational speed regulation for brushless DC motors without the need for Hall sensors.

SPINDLE MOTOR START-UP

Typical spindle motor start-up is accomplished with a companion µP. The commutation counter and the period counter can be initiated at power on or at START bit (MSC_MODE bit 6) rising edge. START bit should be held high during start-up to mask false commutation due to transient on the motor coils (A, B, C). STANDBY bit (CONT_MODE bit 2) can then be asserted to high along with $\overline{RETR} = \overline{BRAKE} = 1$ (this is Standby mode, see Table 2) to activate the spindle drivers and align the motor to start-up position (state 0). Each ADVANCE bit (MSC_MODE bit 0) rising edge will advance the motor to next commutation state (see Table 1).

When the motor achieves sufficient speed to generate adequate back EMF voltage, ADVANCE and START bits are reset by the µP. The motor will then continue to accelerate using the internal commutation delay selected by the DELAY bits (MSC_MODE bits 4 and 5).

To set the motor start-up current, MSCDAC bit (MSC_MODE bit 7) should be asserted to high. The transconductance amplifier input LF will then be provided from the VCM D/A converter. By programming VCM DAC and sense amplifier gain (GAIN0,1 bits in MSC_MODE), motor start-up current will be:

$$I_{Motor} = \frac{V_{LF}}{R_{Sense}} \cdot Gain$$

where voltage at LF pin will be precharged to the DAC output voltage. For fast precharging, external LF resistor (RL in Fig. 1) will also be shorted to ground through the SW pin.

Table 1: Commutation States

STATE	COMMU	PULLDOWNS			PULLUPS		
		A	B	C	A	B	C
0	0	OFF	ON	OFF	ON	OFF	OFF
1	1	OFF	OFF	ON	ON	OFF	OFF
2	0	OFF	OFF	ON	OFF	ON	OFF
3	1	ON	OFF	OFF	OFF	ON	OFF
4	0	ON	OFF	OFF	OFF	OFF	ON
5	1	OFF	ON	OFF	OFF	OFF	ON

SPINDLE MOTOR SPEED REGULATION

The motor speed regulation loop consists of a period counter, speed error detector, charge pump, loop filter and transconductance loop; as well as a commutator to determine the sequential switching of driver current to the motor winding.

Period Counter

A 500 kHz period counter starts with counts 5555 (5400.54 rpm) at the beginning of each revolution and counts down. Period resolution is therefore 2 µs. The counter resets at the end of each revolution.

Speed Error Detector

The speed error detector measures the difference between each motor revolution (8-pole or 12-pole selected by POLE in MSC_MODE bit 3) and the period counter and feeds this speed error to the charge pump circuit. When speed error is within ±32 µs (15.55 rpm) the motor is in "LOCK." The LOCK condition can be monitored on COM/REV pin by setting CRL0 = 0 and CRL1 = 1 (MSC_MODE bits 8 and 9). A logic HIGH on COM/REV pin then indicates motor speed is in LOCK.

If the speed error exceeds 1024 µs (497.66 rpm) too slow, the TOOSLOW condition can be monitored on COM/REV pin by setting CRL0 = 1 and CRL1 = 1. A logic HIGH on COM/REV pin will then indicate motor speed is too slow.

Charge Pump

A constant current source of 60 µA is used to charge or discharge for a 2 µs time multiple determined by the pulse-width modulation of the speed error. When the motor speed error exceeds 1024 µs too fast, the charge pump will discharge the LF pin for the whole period.

When the MSCDAC bit is asserted to high, the charge pump is disabled. LF voltage will then be provided from the VCM D/A converter. If the MSCDAC bit is low (default) and the speed regulation loop is activated, LF voltage will be limited to VBG to avoid excess current on the drivers. Since leakage current on LF pin can introduce speed error, leakage current on LF pin is limited to within 60 nA in order to achieve the highest speed accuracy.

Loop Filter

An external RC lowpass filter must be connected at the LF pin. LF also serves as the input to the transconductance amplifier. When the MSCDAC bit is asserted high during start-up and acceleration, external resistor RL is shorted to ground and the VCM D/A converter will be used to precharge the external capacitors at the LF pin, and thus set the motor start current.

Transconductance Loop

Input pin LF is the non-inverting input of a transconductance amplifier, which uses the lower driver transistor that is presently active per the commutation state, as the power driver element. An external resistor is used to sense the motor coil current. The voltage across the sense resistor is amplified by a gain stage (Gain = 5, 10, 20 or 30 selected by the GAIN bits in the MSC_MODE register) and fed to the inverting input of the transconductance amplifier.

The output pins A, B and C are intended to drive motor coils directly. The output drivers operate to reduce switching noise transients by limiting dv/dt during commutation. Each output consists of two N-channel MOSFET drivers, one for pullup to VSMP1 or VSMP2 and one for pulldown to VSMN1 or VSMN2. The pullup FET functions as a switch with voltage rise and fall times of about 25 microseconds. The pulldown FET is a part of the transconductance amplifier which converts the voltage LF into motor current (Imotor = VLF/(RSENSE • Gain)). When the pulldown output is commutating to the off state, dv/dt on the respective pin is controlled such that dv/dt is approximately 15/RRAMP volts per µs, where RRAMP is measured in kΩ.

SPINDLE MOTOR SPEED REGULATION (CONTINUED)

Commutator

Motor armature position is determined by monitoring the coil voltage of the winding that is not presently being driven by the drivers. The back EMF from the coil, in conjunction with the state of the output drivers, indicates the armature position. The back EMF is compared with a reference at center tap and initiates commutation "events" when the appropriate comparison is made. Because the back EMF comparison event occurs prior to the time when optimum commutation should occur, it is preferred to delay commutation by a predetermined time after the comparison. There are two modes of commutation delay: adaptive and fixed delay. These are selected via the DELAY bits in the MSC_MODE register. In adaptive mode (default), the commutation delay is provided by a circuit which measures the interval between comparison events and delays commutation by a time equal to 3/7 of the prior measured interval. The circuit is adaptive and will provide the optimum delay for a wide range of motor speeds (-80% to 50% of the nominal value). Since the commutation of motor coils typically causes transients, the commutation delay circuit also provides a noise blanking function which prevents the circuit from responding to back EMF comparison events for a period of time equal to the greater of 5/7 of the interval between events or 64 µs after the comparison event. In fixed delay mode, a fixed delay and noise blank is provided. A longer fixed delay might be desirable during start-up to prevent the device from adapting to high frequency noise. The commutation table is shown in Table 1.

CONTROL CIRCUITRY

The control circuitry consists of a power fault detector, a shock detection circuit, and control logic.

The voltage fault detector monitors the system power supply VCC to prevent the VCM driver from responding to a false command during a power failure. The system power supply is applied at VCHK through an external resistor divider and compared with an internal voltage reference at VBG. Hysteresis is generated internally at the VCHK comparator. When a power fault is sensed, even for a brief power drop, $\overline{POR}$ pin will be pulled low regardless of the capacitance loading. Retract mode is activated during power fault.

Three power saving modes are provided, "Sleep," "Standby" and "Shockslp," along with three operating modes. All are selected with $\overline{RETR}$, $\overline{BRAKE}$, STANDBY, and SHOCKSLP bits per Table 2. With $\overline{RETR}$ and $\overline{BRAKE}$ low, both the VCM drivers and MSC drivers are in a high impedance state, and analog circuits are de-biased; this is the "Sleep" mode. With $\overline{RETR}$ and $\overline{BRAKE}$ high, and STANDBY high, MSC section is biased with spindle drivers activated; this is the "Standby" mode. With $\overline{RETR}$ low, $\overline{BRAKE}$ high, both VCM and MSC drivers are in a high impedance state, and the retract amplifier is activated and powered by the back EMF of a spinning motor for retracting heads. With $\overline{BRAKE}$ low, and $\overline{RETR}$ high, the VCM drivers are in a high impedance state, the MSC driver outputs are low impedance to ground (without current limiting), and the analog circuits are biased. Run mode occurs when $\overline{RETR}$ and $\overline{BRAKE}$ bits are high and STANDBY and SHOCKSLP bits are low.

A 2-axis shock detection circuitry is implemented to sense the shock signal at XIN and YIN pins. The shock signal across XIN, XREF pins (and YIN, YREF pins) is amplified and full-wave rectified and then summed with the other axis component at GSUM. This signal then goes through a lowpass filter and is compared to VBG/2. When SHOCKSLP is high, the shock detection circuitry is turned off; this is "SHOCKSLP" mode.

TABLE 2: Power Management/Operation Modes

MODE	$\overline{POR}$	$\overline{RETR}$	$\overline{BRAKE}$	STAND-BY	SHOCK-SLP	VCM ANALOG	SPM ANALOG	VCM DRIVER	SPM DRIVER	SHOCK DETECTION
FAULT	0	X	X	X	X	OFF	OFF	RETRACT	FLOAT	OFF
SLEEP	1	0	0	X	X	OFF	OFF	FLOAT	FLOAT	OFF
STANDBY	1	1	1	1	0/1	OFF	ON	FLOAT	ACTIVE	ON/OFF
RUN	1	1	1	0	0/1	ON	ON	ACTIVE	ACTIVE	ON/OFF
RETRACT	1	0	1	X	0/1	ON	ON	RETRACT	FLOAT	ON/OFF
BRAKE	1	1	0	X	0/1	ON	ON	FLOAT	LOW Z	ON/OFF

NOTE: During Power Fault and Sleep mode, all circuitry on chip will sleep, including the whole shock detection circuit. In modes other than Fault and Sleep, the shock detection circuit can be turned partially off (X, Y AMP will remain ON) with SHOCKSLP.

REGISTER DESCRIPTION

SERIAL INTERFACE DATA FORMAT AND DEFINITION

BIT	NAME	DESCRIPTION
0 (LSB)	R/W	Read/write control. It must be '0' for this device since all of its registers are write only.
1,2,3	DID0..2	Device ID. These three bits define the SSI device for which the serial communication is to be established. '111' is designated for this device.
4,5	ADDR0..1	Register address. These two bits define the internal register to which data is transferred. ADDR1 / ADDR0 / REGISTER 0 / 0 / VCM D/A 0 / 1 / CONT_MODE 1 / 0 / MSC_MODE 1 / 1 / Reserved

THE CONT_MODE REGISTER (ADDRESS 1)

0	$\overline{\text{RETR}}$	$\overline{\text{RETR}}$ select bit. See Table 2. Default is low.
1	$\overline{\text{BRAKE}}$	$\overline{\text{BRAKE}}$ select bit. See Table 2. Default is low.
2	STANDBY	STANDBY select bit. See Table 2. Default is low.
3	SHOCKSLP	SHOCKSLP select bit. See Table 2. Default is low.

THE MSC_MODE REGISTER (ADDRESS 2)

0	ADVANCE	ADVANCE is used by the µP to increment the commutation counter. The rising edge of ADVANCE will increment the counter by one. When held high, it inhibits the counter being incremented by the internal generated clock. When held low, it permits the normal operation of commutation from back EMF events. ADVANCE default is low. See also START, bit 6.
1,2	GAIN0, 1	Sense amplifier gain select. GAIN1 / GAIN0 / GAIN 0 / 0 / 30 (Default) 0 / 1 / 20 1 / 0 / 10 1 / 1 / 5
3	POLE	Select number of poles of spindle motor. POLE low indicates 8 pole motor while POLE high selects 12 poles.

THE MSC_MODE REGISTER (ADDRESS 2) (continued)

BIT	NAME	DESCRIPTION
4,5	DELAY	0,1 Delay mode select. **DELAY1** **DELAY0** **DELAY MODE** 0 0 Adaptive(default) 0 1 Fix delay = 150 µs 1 0 Fix delay = 300 µs 1 1 Fix delay = 500 µs
6	START	Start-up false commutation mask bit START should be held high along with ADVANCE bit during motor start up. Default is low.
7	MSCDAC	MSCDAC is used to select the input to LF pin. When MSCDAC is low (default), speed regulation loop and charge pump is activated and LF voltage is the loop filter output. When MSCDAC is high, LF voltage is connected to VCM D/A converter output and the charge pump is disabled. For fast precharging, MSCDAC will also short the external resistor on the SW pin to ground.
8,9	CRL0,1	COM/REV Pin mode select bits. **CRL1** **CRL0** **COM/REV** 0 0 Commutation Clock 0 1 Revolution Clock 1 0 Lock Indicator 1 1 Too Slow Indicator When CRL1 is high and CRL0 is low, a logic HIGH at COM/REV indicates a lock condition. If COM/REV is low, the motor speed is out of lock. When CRL1 = CRL0 = 1, a logic HIGH at COM/REV indicates the speed error exceeds 1024 µs too slow. CRL0 = CRL1 = 0 is the default.

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PIN DESCRIPTION

POWER SUPPLIES

NAME	TYPE	DESCRIPTION
VPA	-	Analog positive supply.
VNA	-	Analog ground.
VPD	-	Digital positive supply. It must be shorted externally with VPA.
VND	-	Digital ground. It must be shorted externally with VNA. VND is also the low side input to the current sense amplifier of the spindle motor and thus care should be taken to keep VND and the low side of the external resistor Rsense at the same potential.
VVMP[1]	-	Positive supply used for voice coil motor.
VVMN1,2	-	Negative supply used for voice coil motor.
VSMP1,2	-	Positive supply used for spindle motor.
VSMN1,2	-	Negative supply used for spindle motor. They are also the high side inputs to the current sense amplifier of the spindle motor.
VGP	-	Positive supply used for shock detection circuit.
VGN	-	Negative supply used for shock detection circuit.

SERVO POSITIONER

ERRM	I	The inverting input of the error amplifier. ERRM is referenced to VBG.
ERR	O	The error amplifier output. ERR is to provide compensation to the transconductance loop and is referenced to VBG.
SOUT	O	The current sense amplifier output. SOUT is referenced to VBG.
VRETR	I	The retract voltage must be provided externally.
VBYP1	I	The bypassed power supply. An external bypass capacitor is connected to this node to store charge for use by the retract circuitry. This pin is normally a diode drop below VCC, raised by VBEMF during retract.
VBYP2	I	The negative side of the bypass capacitor is connected to this pin. It is normally at ground, rising to VBEMF during retract.
VBEMF	I	Rectified spindle back emf voltage. This input provides current to the internal retract power amplifier.
VM1	O	One side of the voice coil motor sense resistor, and sense resistor combination.
VM2	O	The other side of the voice coil motor.
SE2	I	The voltage across the sense resistor for the voice motor current.
PDAC	O	The 10-bit VCM D/A converter output. It is referenced to VBG if MSCDAC is low, when MSCDAC bit is high, PDAC pin will be floated.

[1] The circuit board contacts for VVMP, VVMN1, VVMN2, VSMP1, VSMP2, VSMN1, and VSMN2 must be sized in accordance with anticipated motor currents. All pins must be connected with low resistance circuit board traces.

SPINDLE MOTOR COMMUTATOR/DRIVER

NAME	TYPE	DESCRIPTION
SYSCLK	I	System clock input at 1 MHz.
COM/REV	O	When the CRL0 bit and CRL1 bit in the MSC_MODE regsiter are low, this pin is defined as the LSB of the commutation counter. If CRL1 bit is low while CRL0 bit is high, it is defined as the revolution clock of the spindle motor. If CRL1 bit is high and CRL0 is low, COM/REV pin becomes lock indicator. A logic HIGH on this pin indicates motor speed is in lock condition. If CRL0 = CRL1 = 1, a logic HIGH on COM/REV pin then indicates speed is too slow by greater than 1024 µs.
LF	I	Control voltage input. The combination of the MOSFET drivers and the predriver circuit forms a transconductance amplifier which sets the motor current in relation to LF. In conjunction with R_{sense} connected at VSMN and the gain of the sense amplifier, the transconductance is defined by: Gm = Im/VIN = 1/(RSENSE x Gain), Gain = 5, 10, 20, 30 When MSCDAC bit is low, LF is provided from charge pump; When MSCDAC bit is high, LF is connected to VCM D/A converter output. An external RC loop filter must be connected at this pin.
SW	O	One side of the external resistor RL in the loop filter. When MSCDAC bit is asserted high, RL is shorted to ground through SW.
A,B,C	O	Spindle motor driver outputs.
CT	I	Back EMF input from spindle motor coil center tap.
RRAMP	I	Lower driver turn-off dv/dt setting resistor. External resistor from VPA to this pin sets the dv/dt slope of the motor coil voltage when the lower drivers are commutating to the off state. The dv/dt is approximately given by the relationship: dv/dt = 15/RRAMP, where dv/dt is expressed in volts/µs and RRAMP in kΩ.

CONTROL CIRCUITRY

VCHK	I	Comparator input for power supply monitoring. When VCHK is below VBG, an internal voltage fault is generated. Normally a resistor divider from VCC is connected at this pin. A capacitor can be connected at this pin to filter out noise transients.
VBG	O	Voltage reference, generated from the internal bandgap voltage, for use with the power supply monitor comparator.
IBR	O	A 21.5 kΩ ±1% resistor is tied from this pin to ground to establish a bias current for internal circuitry.
$\overline{POR}$	O/D	This pin serves the dual purpose of providing power-on-reset and of stretching short internal voltage fault pulses to a width suitable for the host micro controller. An external RC network sets the minimum width of any $\overline{POR}$ pulse. The circuit is designed so that even if a short power fault on VCHK is sensed, $\overline{POR}$ will be pulled low regardless of the capacitance loading.

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CONTROL CIRCUITRY (continued)

NAME	TYPE	DESCRIPTION
XIN	I	X-axis shock detection input.
XREF	I	X-axis reference. XREF is ac-coupled externally to VBG.
YIN	I	Y-axis shock detection input.
YREF	I	Y-axis reference. YREF is ac-coupled externally to VBG.
GSUM	O	The summing node of full-wave rectified X-axis and Y-axis shock signals.
GIN	I	Negative input of GAMP. External RC components are connected between GIN and GOUT to have the required low pass filter response output at GOUT.
GOUT	O	Output of GAMP.
GCOMP	O	Output of GCOMP comparator. GCOMP is active low.

SERIAL INTERFACE PORT

SDATA	I	Serial data shifted into internal registers.
SCLK	I	Serial data timing reference. The rising edge of the SCLK shifts SDATA in while SDEN is asserted high.
SDEN	I	Serial data transfer enable. When active high, the serial data transfer is enabled.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device or affect device reliability.

PARAMETER	RATING
Supply voltage @ VPA,VPD,VVMP,VSMP1,2 VGP	-0.3 to 7.0V
Motor current @ A,B,C,VM1,VM2	1.0A
Input voltage @ LF,RRAMP	-0.3 to VDD + 0.3V
Input voltage @	
A, B, C, VBEMF, VBYP1, VBYP2	-0.3 to 12.0V
VM1, VM2, SE2	-0.3 to 7.0V
All other pins	-0.3 to Vdd
Storage temperature	-65 to 50°C
Lead temperature (10 sec duration)	0 to 300°C

RECOMMENDED OPERATING CONDITIONS

The recommended operating conditions for the device are indicated in the table below. Performance specifications do not apply when the device is operated outside the recommended conditions.

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Supply voltage	Vdd		4.5		5.5	V
Supply current						
VPA,VPD	Idd				20	mA
VVMP	Ivmp				0.4	A
VSMP1, 2	Ismp				0.5	A
Standby mode	Istandby				15	mA
Sleep mode	Isleep				1.0	mA
VGP	Ivgp				4	mA
VGP Sleep	Igsleep				1	mA
Input voltage @ VBEMF			1.0		10	V
Input voltage @ LF			0		2.5	V
Ambient temperature	Ta		0		70	°C
Capacitive load on digital outputs	Cl				100	pF

RECOMMENDED OPERATING CONDITIONS (continued)

The recommended operating conditions for the device are indicated in the table below. Performance specifications do not apply when the device is operated outside the recommended conditions.

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Analog output load	Cl				40	pF
	Rl				10	kΩ
System clock fc = 1 MHz						
Freq. tolerance	fc		-0.1		0.1	%
Pulse width	Twh,Twl		0.4		0.6	µs
Biasing resistor	Rbias		-1		1	%
Rbias = 21.5 kΩ						
External resistors	Rf, Rc		10			kΩ

PERFORMANCE SPECIFICATIONS

Digital I/O

Digital input @ SDATA, SCLK, SDEN, SYSCLK	Vil				0.8	V
	Vih		2.0			V
	Iil,Iih				±1	µA
Digital O/D output @ $\overline{POR}$	Ioh	Voh = Vdd			1	µA
	Iol	Vol = 0.4V	4.0			mA
	Vol	Iol = 4 mA			0.4	V
Digital Output @ COM/REV	Vol	Iol = 2.0 mA			0.4	V
	Voh	Ioh = -100 µA	2.4			V

Servo Positioner

VBYP1 current	Normal mode				100	µA
	Retract mode	Power off, VBYP1 = 3V			20	µA
BEMF current	Normal mode	VBEMF = 4V			300	µA
	Retract mode	Imotor = 0, VBEMF = 3V, Power off, VRETR = 0.5V			20	µA

Servo Positioner (continued)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
SOUT amplifier Gain		3.9		4.1	V/V
Input offset	SOUT = VBG	-3		3	mV
Output swing	RL = 10 kΩ to VBG	0.15		Vdd-1	V
CMRR		60			dB
ERRAMP amplifier Gain		60			dB
Unit gain bandwidth			1		MHz
Input offset	ERR = ERRM	-10		10	mV
Output swing		0.15		Vdd-1.25	V
Power amplifier (VCM Driver)	Gain (VM2-VM1)/(ERR-VBG)	11		13	V/V
Total voltage drop across Power FET's(PFET)	Imotor = 200 mA			1.0	V
Bridge crossover time	Ivcm = 10 mA, pp step input, RL = 16Ω			10	µs
VCM output THD	Ivcm = 100 mA, pp @ 100 Hz, RL = 16Ω			2	%
Retract amplifier (normal)	VRETR leakage	-1		1	µA
Retract amplifier (retract)	VRETR = 0.5V, VBEMF ≥ 1V, RL = 16Ω				
Offset		-100		0	mV
Maximum output current	VRETR = 0.5V, VBYP1 = 4.5V, VM1 = VM2 VBEMF = 1.0V	40			mA
	VBEMF = 1.5V	60			mA

Spindle Motor Speed Controller/Driver

Charge pump current		48		72	µA
Leakage current @ LF	0 < VIN < 2.5V	-25		25	nA
Total voltage drop across	I = 200 mA			0.4	V
power FETs(SFET)	I = 500 mA			1.0	V
Outputs impedance @ A,B,C Rin while not driving	-0.3V < Vin < 7V	10			kΩ
Output impedance @ CT Rin	-0.3V < Vin < 7V	3			kΩ

RECOMMENDED OPERATING CONDITIONS (continued)
The recommended operating conditions for the device are indicated in the table below. Performance specifications do not apply when the device is operated outside the recommended conditions.

Control Circuitry

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
On resistance at $\overline{POR}$				200	Ω
VBG	Iout < ±0.2 mA	2.16		2.30	V
VCHK comparator offset w.r.t. VBG Hysteresis		-15 40		15 120	mV mV

Shock Detection Circuitry

XAMP,YAMP	Gain,XIN or YIN to GSUM 0.5 mV,peak < V(IN) < 20 mV,peak 1KHz < V(IN) < 5 KHz	36		44	V/V
	Differential input resistance	2850			Ω
	Input leakage current	-50		50	nA
GAMP	Input referred offset	-15		15	mV
	Output swing	0.75		VBG + 0.1	V
	Bandwidth		1		MHz
GCOMP Comparator Threshold w.r.t. VBG		-1.05		1.2	V

D/A Converter

Full-scale voltage			VBG		V
Resolution			10		bits
Digital Delay				4	µs
LSB voltage			VBG/1024		V
Differential nonlinearity				1	LSB

Serial Interface Port

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
SDEN setup time prior to SCLK	Tsens	3 5			ns
SDEN hold time after SCLK	Tsenh	50			ns
SDATA setup time prior to SCLK rise	Tds	15			ns
SDATA hold time after SCLK rise	Tdh	15			ns
SCLK pulse width	Tpw	100			ns

APPLICATIONS INFORMATION

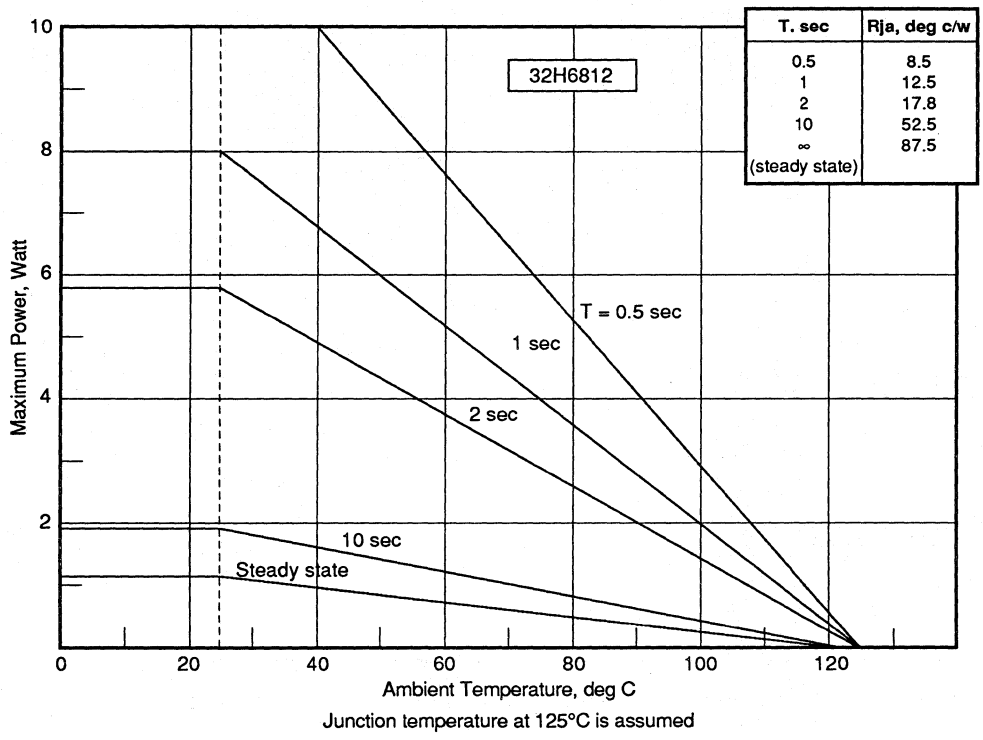
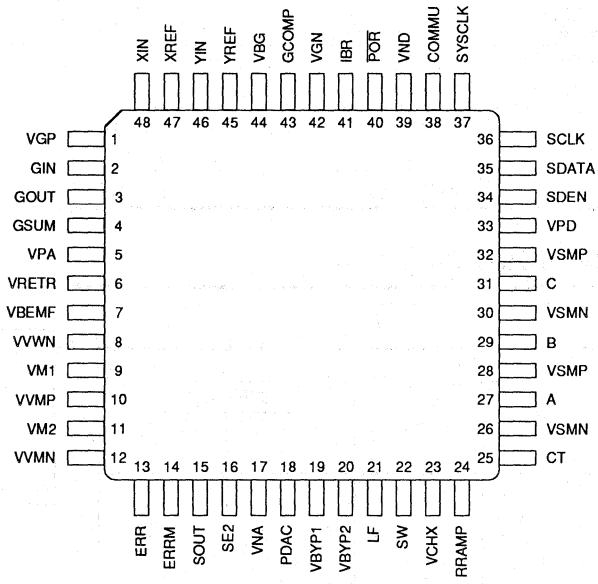


FIGURE 1: Power Dissipation Derating

SSI 32H6812
Servo & Spindle Driver with Shock Detection

PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



48-Lead TQFP

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

Silicon Systems, Inc. 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914

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SSI 32H6814
5V Servo/Motor Speed Driver

Advance Information

January 1994

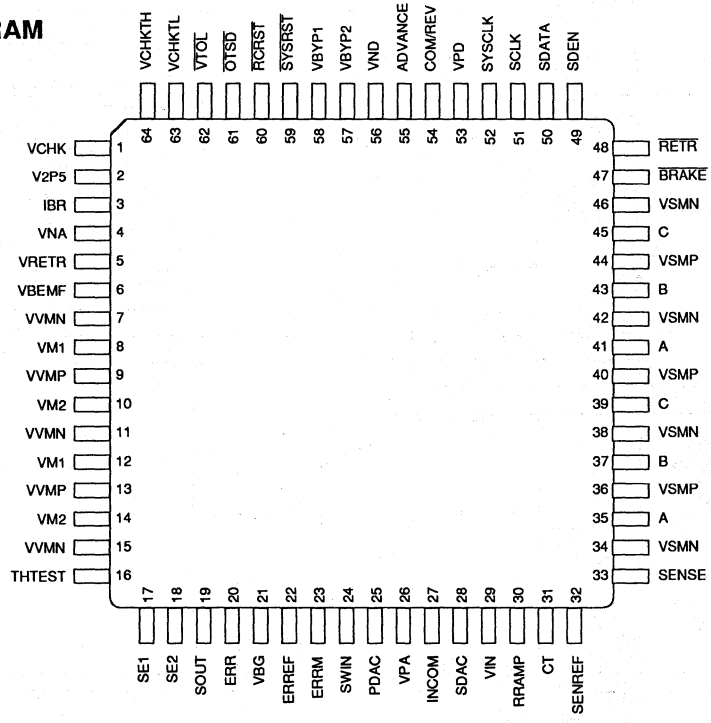
DESCRIPTION

The SSI 32H6814 Servo/MSC Driver is a CMOS monolithic integrated circuit housed in a 64-lead TQFP package which operates from a single 5V supply. It provides a fully integrated servo driver and a spindle motor commutator with internal power FETs. The servo driver is intended for use in disk drive head positioning systems employing linear or rotary voice coil motors. The commutator in conjunction with a microprocessor (μP) or digital signal processor (DSP), provides a complete spindle motor speed control system. It also includes two 10-bit D/A converters, with a serial interface to commonly used μP or DSP, for commanding the servo positioner and the spindle motor, respectively. The device is ideal for use in 5V small-form disk drive applications.

FEATURES

- **64-lead TQPF package**
- **Internal 1.0A servo driver with no deadband, class-B output**
- **Thermal overload protection**
- **Power fault detection with built-in retract circuitry**
- **10-bit VCM D/A converter with 4 μs digital delay**
- **Gain select switch for a wide dynamic range of servo inputs**
- **Internal precision voltage reference**
- **Programmable commutation delay for optimal motor efficiency**
- **Internal 1.25A spindle driver**

PIN DIAGRAM



64-Lead TQFP

CAUTION: Use handling procedures necessary for a static sensitive component.

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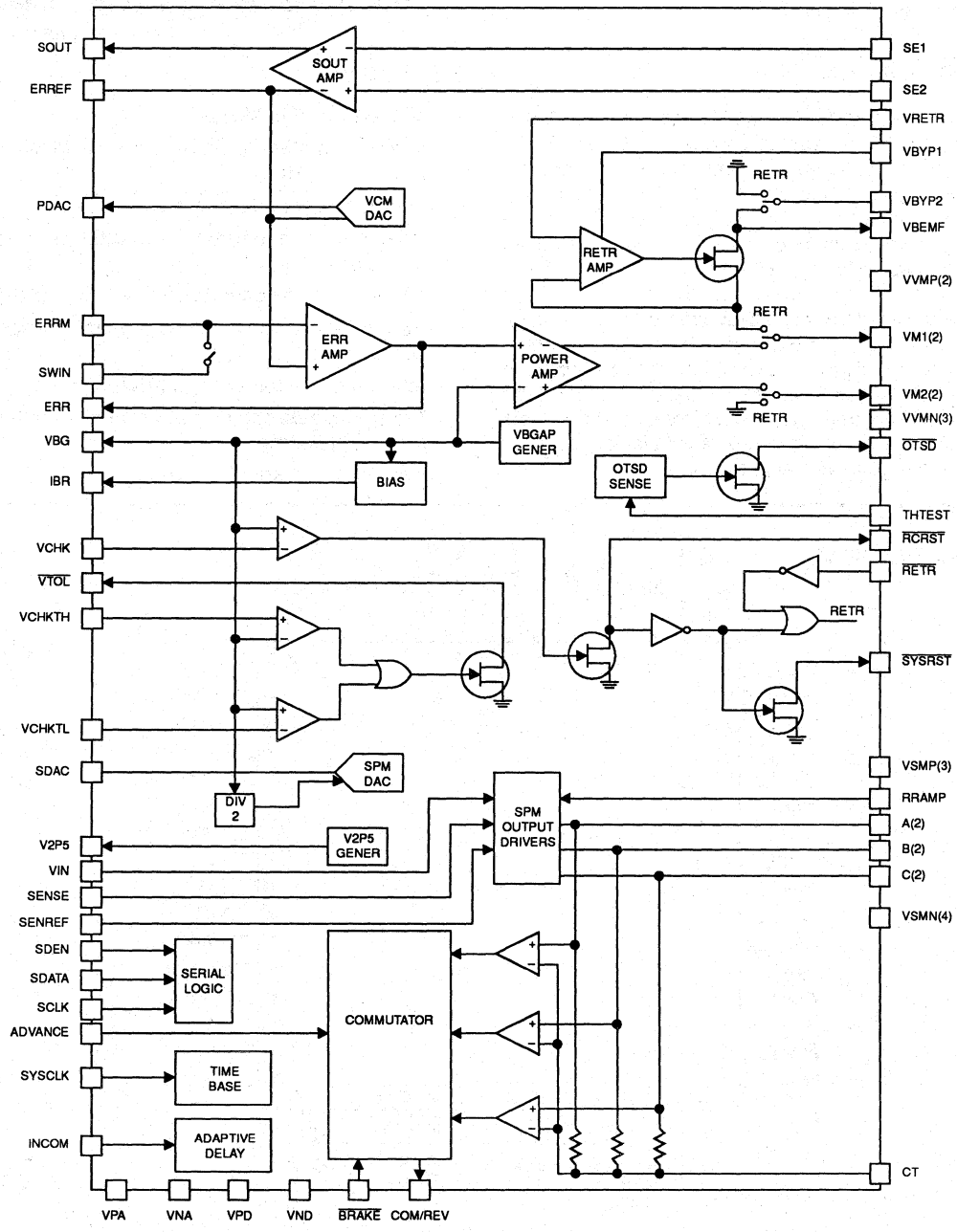

Figure 1: Block Diagram

FEATURES (continued)

- Switch-mode current limiting for spindle motor start-up
- Serial interface compatible with 80C196 and 68HC16
- Low power CMOS design with Sleep mode

FUNCTIONAL DESCRIPTION

As shown in the block diagram, the SSI 32H6814 can be divided into four major sections: servo positioner, spindle motor commutator/driver, control circuitry and serial interface port.

SERVO POSITIONER

The servo positioner is a power transconductance amplifier for use in driving a voice coil servo motor (VCM). It has two primary modes of operation, normal (or linear) and retract. The retract mode is activated by a power supply failure or when $\overline{\text{RETR}}$ is asserted low while $\overline{\text{BRAKE}}$ being high. Otherwise the device operates in linear mode. The servo positioner consists of SOUT amplifier, ERR amplifier, retract amplifier, power amplifier and 10-bit VCM D/A converter.

SOUT AMPLIFIER

The SOUT amplifier generates a voltage at SOUT, proportional to positioner current, by sensing the voltage across an external resistor Rs, amplifying and referencing to ERREF. Since the common mode voltage on Rs can range over the full power supply, while the differential voltage is in the order of millivolts, the SOUT amplifier is realized with a high input common mode rejection and low input offset.

ERR AMPLIFIER

The ERR amplifier is a high gain op amp. Due to the fixed gain of the power amp, ERR is proportional to the VCM voltage. The negative input of this amplifier is the system summing junction for the currents which are proportional to the desired VCM current, the measured VCM current, and the VCM voltage.

POWER AMPLIFIER

The power amplifier is a fixed gain voltage amplifier with differential inputs and outputs. Its input is the differential voltage between ERR and VBG. Its output drives the VCM directly through an internal NMOS bridge. An internal charge pump generates gate voltages higher than VVMP so the upper NMOS devices can drive VM1 and VM2 up to VVMP.

RETRACT AMPLIFIER

When a voltage fault is sensed, or when $\overline{\text{RETR}}$ is asserted low while $\overline{\text{BRAKE}}$ being high, the servo positioner enters into retract mode. In this mode, it is assumed that no current is available from VVMP. Thus power for this mode comes from VBEMF, the rectified spindle back emf voltage, and from VBYP1, a voltage generated from the external storage capacitor CBYP. The retract amplifier is powered by VBYP1. It senses the voltage at VRETR and, through a power NMOS source follower, raises VM1 to VRETR. The drain of the source follower is VBEMF.

VCM D/A CONVERTER

Switched-capacitor circuit technique is employed to implement the VCM D/A converter with two non-overlapped clock phases, one phase for auto-zeroing and another one for evaluation. These two phases run synchronously with an internal 500 kHz clock, which is derived directly from the system clock at SYSCLK.

The request of the VCM D/A converter is initiated by writing to the VCM D/A register (00) through the serial interface port. The input data word must be coded in two's complement form. Note that there would be a maximum of 2 µs of latency between a conversion request and the actual start of conversion. The conversion delay from the actual start of conversion to when the analog output begins to slew to a new value is 2 µs. Therefore a maximum of 4 µs is required for a conversion, in addition to the time needed for completion of a serial data transfer, which is equal to 16/SCLK. The VCM D/A converter provided at PDAC is referenced to ERREF, which also serves as a reference voltage for the error amplifier and the current sense amplifier.

SPINDLE MOTOR COMMUTATOR/DRIVER

The spindle motor commutator in conjunction with external components provides the motor driving capability for starting, accelerating and rotational speed regulation for brushless DC motors without the need for Hall sensors. The speed regulation control loop is completed with a µP or DSP external to this device.

FUNCTIONAL DESCRIPTION (continued)

COMMUTATOR

Motor armature position is determined by monitoring the coil voltage of the winding that is not presently being driven by the drivers. The back emf from the coil, in conjunction with the state of the output drivers, indicates the armature position. The back emf is compared with a reference at CT and initiates commutation "events" when the appropriate comparison is made. Commutation is the sequential switching of drive current to the motor windings. Because the back emf comparison event occurs prior to the time when optimum commutation should occur, it is preferred to delay commutation by a predetermined time after the comparison. There are two modes of commutation delay, namely adaptive or one shot, which can be selected via the M, N bits in the mode register (10) per table 1. In adaptive mode (default), the commutation delay is provided by a circuitry which measures the interval between comparison events and delays commutation by a time equal to 3/7 of the prior measured interval. The circuit is adaptive and will provide the optimum delay for a wide range of motor speeds (-80% to 50% of the nominal value). Since the commutation of motor coils typically causes transients, the commutation delay circuit also provides a noise blanking function which prevents the circuit from responding back emf comparison events for a period of time equal to the maximum of 5/7 of the interval between events and 64 µs after the comparison event. INCOM pin can be selected as a test pin if it is high impedance in the adaptive mode, otherwise it should be selected as "IN" for the adaptive mode to work properly. In one shot mode, an input voltage at INCOM pin will provide a fix delay and noise blank. For start-up, INCOM = Vdd/2 is recommended, delay will be about 500 µs and noise blank about 850 µs. The commutation table is described in Table 2.

Motor speed control may be accomplished by measuring the period of the output signal at COM/REV. COM/REV may be defined as either COMMU, the LSB of the commutation counter, or REVCLK, the revolution clock of the motor, selected via the bit $\overline{\text{COM}}$/REV in the mode register (10).

TRANSCONDUCTANCE AMPLIFIER

Input pin VIN is the non-inverting input of a transconductance amplifier which uses the lower driver transistor, that is presently active per the commutation state, as the power driver element. An external resistor is used to sense the current flowing through the drive transistor source (and hence the motor coil current). The voltage across the sense resistor is amplified by a gain stage (Av=5,10, 20 or 30 selected by the GAIN bits in the MODE register) and fed to the inverting input of the transconductance output stage.

The 10-bit SPM D/A converter, referenced to VBG/2, is provided at SDAC for converting the commanding signal in digital format into an analog voltage. Its operation is similar to the VCM D/A converter, but is initiated by writing to the SPM D/A register (01) in two's complement form.

POWER AMPLIFIER

The output pins A, B and C are intended to drive motor coils directly. The output drivers operate to reduce switching noise transients by limiting dv/dt during commutation. Each output consists of two N-channel MOSFET drivers, one for pullup to VSMP and one for pulldown to VSMN. The pullup FET functions as a switch with voltage rise and fall times of about 25 µs. The pulldown FET is a part of the transconductance amplifier which converts the voltage VIN into motor current (Imotor=VIN/($\overline{\text{RSENSE}}$Av), where Av is either 5,10,20 or 30). When the pulldown output is commutating to the off state, dv/dt on the respective pin is controlled such that dv/dt is approximately 15/RRAMP volts per µs, where RRAMP is measured in kΩ.

TABLE 1: Modes of Commutation Delay

MODE REGISTER (10) M	N	SWITCH DELAY MODE	DELAY MODE	INCOM PIN
0	0	No	Adaptive	Test (Default)
0	1,2	No	Adaptive	In
0	3	No	One Shot	In
0	X	Yes	One Shot	In

MOTOR START-UP

Motor starting is accomplished by a companion µP or DSP via ADVANCE, $\overline{\text{RETR}}$, $\overline{\text{BRAKE}}$ and COM/REV. The µP can assert $\overline{\text{RETR}}$ and $\overline{\text{BRAKE}}$ low to initiate the commutation counter and then increment the counter with ADVANCE. After $\overline{\text{RETR}}$ and $\overline{\text{BRAKE}}$ are asserted low and de-asserted (the power-up condition for preparation to begin a starting sequence), the commutation state will be state 0 per Table 1, but the lower driver output B remains inactive to prevent current flowing through the motor (out of A which is high). On the first ADVANCE set high, the commutation state 1 is selected and the drivers are per Table 2. ADVANCE at logic high excludes internal commutations. COMMU provides feedback to the µP on motor activity.

SWITCH-MODE OPERATION

Switch-mode operation is provided for limiting the motor current during motor start-up. Two values M and N, loaded into the mode register (10) through the serial interface, determines the basic switching parameters for the operation. The M (3 bits) sets the minimum "on" time of the lower drivers and sample delay time. The N (2 bits) sets the switching period. The timing is given by:

Minimum "on" time $= (M + 1) \cdot 4\ \mu s$

Sample delay time $= M \cdot 4\ \mu s$

Switching period $= (N + 2) \cdot (M + 1) \cdot 4\ \mu s$

Hence, Minimum duty cycle = 1/(N+2)

Sample delay time, defined as the time from turning the lower drivers "on" until switching transients have settled, is a function of the particular application and will be determined by the user.

The value of M=0 (Default) is defined as linear mode, no switching except normal commutation will occur.

For a proper switch-mode operation, three flyback diodes from outputs A, B, and C, and a blocking diode from the system power supply VCC to the VSMP pins are required. The flyback diodes will provide power for retract (during power failure) at pins VSMP. Also, a voltage level should be provided at INCOM pin as the threshold for the one-shot commutation delay.

CONTROL CIRCUITRY

The control circuitry consists of a power fault detector, a thermal overload circuit, a voltage tolerance detector, and control logic. The inputs to the control circuitry are VCHK, VCHKTL, VCHKTH, $\overline{\text{RETR}}$, and $\overline{\text{BRAKE}}$, along with the internal signals from the thermal overload detector.

The power fault detector monitors the system power supply VCC to prevent the VCM driver from responding to a false command during a power failure. The system power supply is applied at VCHK through an external resistor divider and compared with an internal voltage reference at VBG. When a power failure is sensed, the $\overline{\text{SYSRST}}$ is asserted low and the retract mode is activated.

The thermal overload circuit monitors the die temperature to prevent an excessive current flowing through VCM or SPM drivers. If the die temperature exceeds approximately 135°C, the $\overline{\text{OTSD}}$ is asserted low and both drivers are turned off. The drivers will become operative after the temperature is reduced and the ADVANCE is asserted high.

The voltage tolerance detector generates an active low signal $\overline{\text{VTOL}}$ when either VCHTL goes below VBG or VCHTH goes above VBG. Note that no servo retract is activated in this case.

Four operating modes are selected via $\overline{\text{RETR}}$ and $\overline{\text{BRAKE}}$ (when the system power supply is present) per Table 3. With $\overline{\text{RETR}}$ and $\overline{\text{BRAKE}}$ asserted low, both

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TABLE 2: Commutation States

STATE	COMMU	PULLDOWN A	PULLDOWN B	PULLDOWN C	PULLUP A	PULLUP B	PULLUP C
0	0	OFF	ON	OFF	ON	OFF	OFF
1	1	OFF	OFF	ON	ON	OFF	OFF
2	0	OFF	OFF	ON	OFF	ON	OFF
3	1	ON	OFF	OFF	OFF	ON	OFF
4	0	ON	OFF	OFF	OFF	OFF	ON
5	1	OFF	ON	OFF	OFF	OFF	ON

FUNCTIONAL DESCRIPTION (continued)

CONTROL CIRCUITRY

the VCM drivers and SPM drivers are in a high impedance state, and analog circuits are de-biased. This is the "sleep" mode. With $\overline{RETR}$ asserted, $\overline{BRAKE}$ de-asserted, both VCM and SPM drivers are in a high impedance state, and the retract amplifier is activated and powered by the back emf of a spinning motor for retracting heads. For $\overline{BRAKE}$ asserted, and $\overline{RETR}$ de-asserted, the VCM drivers are in a high impedance state, the SPM driver outputs are low impedance to ground (without current limiting), and analog circuits are biased. Normal mode is given for $\overline{RETR}$ and $\overline{BRAKE}$ de-asserted.

SERIAL INTERFACE PORT

A synchronous serial port, compatible with the commonly used µP such as 80C196 and 68HC16, is used to input digital words for D/A converters and mode registers. It is shift register based I/O interface and consists of three pins: SDEN, SCLK and SDATA. Data from µP is transferred 8 bits (one byte) at a time with LSB first, MSB last, where LSB is defined as Bit 0 A complete transfer requires two bytes which are formatted into an instruction and a data field. Figure 2 shows the serial interface timing diagram.

The serial port is enabled for data transfers when the Serial Data Enable (SDEN) pin is pulled high. SDEN should be asserted high prior to any transmission and it should remain high until the completion of the transfer. At the end of each transfer SDEN should be brought low.

Serial data applied to SDATA is clocked into an internal 16-bit shift register at the rising edge of SCLK while SDEN is active high. At the end of each transfer, SDEN must return low. If SDEN remains high after the last bit (which is the MSB of the second byte) is received, any additional data on SDATA will be ignored. Data must be two bytes for each transfer. If, for any reasons, SDEN is brought low prior to the completion of the second byte, the write operation of the data will be aborted.

The instruction field, as defined in Table 4, includes the first 6 bits of the first byte. The data field is 10-bit wide and includes the last two bits of the first byte and the second byte.

TABLE 3: Mode of Operations

$\overline{OTSD}$	VCHK >VBG	$\overline{RETR}$	$\overline{BRAKE}$	MODE	ANALOG	SPEED COUNTER	VCM DRIVER	SPM DRIVER
0	x	x	x	Shutdown	ON	Active	Float	Float
1	0	x	0	Fault/Brk	OFF	Active	Retract	Low Z
1	0	x	1	Fault/Ret	OFF	Active	Retract	Float
1	1	0	0	Sleep/Brk	OFF	Reset	Float	Float
1	1	0	1	Retract	ON	Active	Retract	Float
1	1	1	0	Brake	ON	Active	Float	Low Z
1	1	1	1	Run	ON	Active	Active	Active

TABLE 4: Instruction Field Definition

BIT	NAME	DESCRIPTION
0 (LSB)	R/W	Read/write control. It must be '0' for this device since all of its registers are write only.
1,2,3	DID0..2	These three bits define the SSI device for which the serial communication is to be established. '111' is designated for this device.
4,5	ADDR0..1	Register address. These two bits define the internal register to which data is transferred.

ADDR1	ADDR0	Register Name
0	0	VCM D/A
0	1	SPM D/A
1	0	Mode
1	1	Reserved

The mode register (10) is defined in Table 5.

TABLE 5: Mode Register Definition

BIT	NAME	DESCRIPTION
0	SWON	Analog switch enable.
1	GAIN0	Sense amplifier gain select.
2	GAIN1	GAIN1 GAIN0 Gain Selected 0 0 30(Default) 0 1 20 1 0 10 1 1 5
3	START	Start-up mode enable. It should be asserted high during spindle start-up when the commutation is commanded by a train of ADVANCEpulses. During spindle running, it should be asserted low (default) to allow self internal commutation
4	N0	LSB of N value - minimum duty cycle.
5	N1	MSB of N value.
6	M0	LSB of M value - sample delay time.
7	M1	M value.
8	M2	MSB of M value.
9	$\overline{COM}$/REV	Select COMMU ($\overline{COM}$/REV=0, default) or REVCLK ($\overline{COM}$/REV=1).

PIN DESCRIPTION

POWER SUPPLIES

NAME	TYPE	DESCRIPTION
VPA	–	Analog positive supply.
VNA	–	Analog ground.
VPD	–	Digital positive supply. It must be shorted externally with VPA.
VND	–	Digital ground. It must be shorted externally with VNA.
VVMP	–	Positive supply used for voice coil motor.
VVMN	–	Negative supply used for voice coil motor.
VSMP	–	Positive supply used for spindle motor.
VSMN	–	Negative supply used for spindle motor.

SERVO POSITIONER

NAME	TYPE	DESCRIPTION
SWIN	I	The analog switch input. The other side of the switch is connected toERRM.
ERRM	I	The inverting input of the error amplifier.
ERREF	I	The reference voltage for the error amplifier, the VCM D/A converter and the current sense amplifier.
ERR	O	The error amplifier output. ERR is to provide compensation to the transconductance loop and is reference to VBG.
SOUT	O	The current sense amplifier output. SOUT is referenced to ERREF.
VRETR	I	The retract voltage. Retract voltage must be provided externally at VRETR pin.
VBYP1	I	The bypassed power supply. An external bypass capacitor is connected to this node to store charge for use by the retract circuitry. This pin is normally a diode drop below VCC, rising by VBEMF during retract.
VBYP2	I	The other side of the bypass capacitor is connected to this pin. It is normally at ground, rising to VBEMF during retract.
VBEMF	I	Rectified spindle back emf voltage. This input provides current to the internal retract power amplifier.
VM1	O	One side of the voice coil motor.
VM2	O	The other side of the voice coil motor and sense resistor combination.
SE1,SE2	I	The voltage across the sense resistor for the voice motor current.
$\overline{\text{RETR}}$	I	Retract control pin. Refer to Table 3.
PDAC	O	The 10-bit VCM D/A converter output. It is referenced to ERREF.

SPINDLE MOTOR COMMUTATOR/DRIVER

NAME	TYPE	DESCRIPTION
SYSCLK	I	System clock input at 10 MHz.
COM/REV	O	When the $\overline{\text{COM}}$/REV bit in the mode register is low, this pin is defined as the LSB of the commutation counter. Otherwise, it is defined as the revolution clock of the spindle motor.
ADVANCE	I	ADVANCE is used to increment the commutation counter externally. The rising edge of ADVANCE will increment the counter by 1. When held high, it inhibits the counter from internal incrementing. When held low, it permits the normal operation of commutation from back emf events.
INCOM	I	Commutation delay control. Adaptive commutation delay may be adjusted from its nominal value of one half the commutation interval by sinking or sourcing current from this pin. This should be done via an external control loop which can compensate for the range of internal circuit parameter variations.
SDAC	O	The 10-bit SPM D/A converter output. It is referenced to VBG/2.
VIN	I	Control voltage input. The combination of the MOSFET drivers and the predriver circuit forms a transconductance amplifier which sets the motor current in relation to VIN. In conjunction with Rsense connected at VSMN and the gain of the sense amplifier, the transconductance is defined by Gm = Im/VIN = 1/($\overline{\text{RSENSE}}$gain), gain=5, 10, 20, 30.
A,B,C	O	Spindle motor driver outputs.
CT	I	Back emf input from spindle motor coil center tap. Internal circuit uses the back emf voltages to determine the rotor position and effect commutation.
RRAMP	I	Lower driver turn-off dv/dt setting resistor. External resistor from VPA to this pin sets the dv/dt slope of the motor coil voltage when the lower drivers are commutating to the off state. The dv/dt is approximately given by the relationship: dv/dt=15/RRAMP, where dv/dt is expressed in volts/µs and RRAMP in kΩ.
SENSE	I	Current sense amplifier non-inverting input. The current sense resistor connected to the sources of lower driver transistors is to monitor the current flowing through the spindle motor. The device will control the voltage across the sense resistor to match VIN. This pin provides a Kelvin connection to the high side of the sense resistor and must be shorted with VSMN externally.
SENREF	I	Current sense amplifier inverting input. It provides a Kelvin connection to the low side of the sense resistor.
$\overline{\text{BRAKE}}$	I	$\overline{\text{BRAKE}}$ is used to provide a delay between the initiation of fault-induced head retract and spindle motor braking. A capacitor to ground and a resistor to $\overline{\text{SYSRST}}$ are selected such that 1.2RC is equal to the maximum time required for retract.

PIN DESCRIPTION (continued)

CONTROL CIRCUITRY

NAME	TYPE	DESCRIPTION
VCHK	I	Comparator input for monitoring power supply. When VCHK goes below VBG, an internal voltage fault is generated and hence the servo head retract is activated.
VBG	O	Voltage reference at 2.23V, generated from the internal bandgap voltage, for use with the power supply monitor comparator.
VCHKTL	I	Comparator input for monitoring supply voltage tolerance. When VCHKTL goes below VBG, $\overline{\text{VTOL}}$ will be pulled low.
VCHKTH	I	Comparator input for monitoring supply voltage tolerance. When VCHKTH goes above VBG, $\overline{\text{VTOL}}$ will be pulled low.
$\overline{\text{VTOL}}$	O/D	When low, this open-collector output indicates that either VCHKTL goes below or VCHKTH goes above VBG.
V2P5	O	Voltage reference at 2.5V, generated from the internal bandgap voltage.
IBR	O	A resistor is tied from this pin to ground to establish a bias current for internal circuitry.
$\overline{\text{RCRST}}$	O/D	This pin serves the dual purpose of providing power-on-reset and stretching short internal voltage fault pulses to a width suitable for the host micro controller. An external RC network sets the minimum width of any $\overline{\text{SYSRST}}$ pulse. If $\overline{\text{RCRST}}$ is pulled low by external circuitry, this device will enter into the retract mode and pull $\overline{\text{SYSRST}}$ low.
$\overline{\text{SYSRST}}$	O/D	When low, this open-collector output indicates that an internal voltage fault has occurred.
$\overline{\text{OTSD}}$	O/D	Thermal Shut down. When low, this open-collector output indicates that the junction temperature has exceeded the recommended operating range and the device is in thermal shut-down. In thermal shut-down, all output drivers are turned off and analog circuit de-biased.
THTEST	I	Biased low with an internal pulldown. When asserted high, $\overline{\text{RETR}}$ will be connected to the thermal overload test circuitry for use as a test input.

SERIAL INTERFACE PORT

SDATA	I	Serial data input passing digital words for internal registers.
SCLK	I	Serial data timing reference. The rising edge of the SCLK is to strobe SDATA while SDEN is asserted high.
SDEN	I	Serial data transfer enable. When active high, the serial data transfer is enabled.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device or affect device reliability.

PARAMETER		RATING
Supply voltage @ VPA, VPD, VVMP, VSMP	Vdd	-0.3 to 7V
Motor current @ VM1, VM2 A, B, C	 Ivcm Ispm	 ±1A ±1.25A
Input voltage @ CT, A, B, C, VBEMF, VBYP1, VBYP2 VM1, VM2, SE1, SE2 All other pins	Vin	 -0.3 to 12V -0.3 to 7V -0.3 to Vdd + 0.3
Storage temperature	Tstg	-65 to 150°C
Lead temperature	Tlead	0 to 300°C

RECOMMENDED OPERATING CONDITIONS

The recommended operating conditions for the device are indicated in the table below. Performance specifications do not apply when the device is operated outside the recommended conditions.

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Supply voltage	Vdd		4.5		5.5	V
Supply current						
VPA, VPD	Idd				20	mA
VVMP	Ivmp				0.6	A
VSMP	Ismp				1	A
Sleep mode	Isleep				1	mA
Input voltage @ VBEMF	VBEMF		1		10	V
Input voltage @ VIN	VIN		0		2.5	V
Input voltage @ ERREF	ERREF		VBG/2		VBG	V
Ambient temperature	Ta		0		70	°C
Capacitive load on digital outputs	Cl				100	pF
Analog output load	Cl				40	pF
	Rl		10			kΩ
System clock fc = 10 MHz						
Frequency tolerance	fc				±0.1	%
Pulse Width	Twh, Twl		40		60	ns
Biasing resitor, Rbias = 22.6 kΩ	Rbias				±5	%
External resistors	Rf, Rc		10			kΩ

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ELECTRICAL SPECIFICATIONS (continued)

DIGITAL I/O

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Digital input @ SDATA,SCLK,SDEN ADVANCE,SYSCLK,$\overline{RETR}$					
Vil		0.8			V
Vih				2	V
Iil, Iih				±1	µA
Digital input @ $\overline{BRAKE}$					
Vil		1.2			V
Vih				2.4	V
Iil, Iih				±1	µA
Digital O/C output @ $\overline{RCRST}$,$\overline{SYSRST}$,$\overline{OTSD}$,$\overline{VTOL}$					
Ioh	Voh=Vdd			1	µA
Iol	Vol=0.4V	-4.0			mA
Digital output @ COM/REV					
Vol	Iol=2.0 mA			0.4	V
Voh	Ioh=-100 µA	2.4			V

SERVO POSITIONER

The following VCM performance specifications are measured with 7.5Ω resistive load, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VBYP1 current					
Normal mode				100	µA
Retract mode	Power off, VBYP1=3V			10	µA
Brake mode	Power off, VBYP1=3V			10	µA
BEMF current					
Normal mode	VBEMF=4V			300	µA
Retract mode	Power off, VBEMF=3V VRETR=0.5V, VBYP1=4V			10	µA
SOUT amplifier					
Gain		3.9		4.1	V/V
Input offset	SOUT = ERREF			±3	mV
Output swing	RL = 10 kΩ to ERREF	0.15		Vdd-1	V
CMRR					
ERRAMP amplifier					
Gain		60			dB
Unit gain bandwidth		1			MHz
Input offset				±10	mV
Output swing		0.15		Vdd-1.25	V
Power amplifier gain (VM1-VM2)/(ERR-VBG)		11		13	V/V

SERVO POSITIONER (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Total voltage drop across power FETs	Imotor=0.6A			0.9	V
VCM bridge crossover time	Ivcm=10 mA,peak step input			10	µs
VCM output THD	Ivcm=0.1A,peak @ 100 Hz			2	%
SWIN on resistance				100	Ω
Retract amplifier (normal) VRETR leakage current				±1	µA
Retract amplifier (retract)					
VRETR input impedance	VRETR=0.5V,VBEMF≥1V	500			kΩ
Offset		-100		0	mV
Maximum output current	VBYP1=4.5V,VM1=VM2				
VBEMF=1.0V	VRETR=0.5V	60			mA
VBEMF=1.5V		100			mA

SPINDLE MOTOR COMMUTATOR/DRIVER PARAMETER

Input leakage current @ VIN	0≤VIN≤2.5V			+1	µA
Total voltage drop across power FETs	Imotor=1.0A			1	V
Rin @ A,B,C while not driving	-0.3V≤Vin≤7V	10			kΩ
Rin @ CT while not driving	-0.3V≤Vin≤7V	3			kΩ

CONTROL CIRCUITRY

Vdd voltage for $\overline{\text{SYSRST}}$ & $\overline{\text{RCRST}}$ in operation		2			V
On resistance at $\overline{\text{RCRST}}$				100	Ω
VBG	Iout<±0.2 mA	2.16		2.3	V
VCHK comparator offset				+10	mV
V2P5	Iout<±0.2 mA	2.42		2.58	V
VCHKTL, VCHKTH comparator offset				+10	mV
Thermal shutdown temperature threshold		125		145	°C

ELECTRICAL SPECIFICATIONS (continued)

D/A CONVERTER

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Full-scale voltage			VBG		V
Resolution			10		bits
Digital delay				4	µs
LSB voltage			VBG/1024		V
Differential nonlinearity				1	LSB

SERIAL INTERFACE PORT

The following timing measurements are made at 50% Vdd for all signals, unless otherwise noted.

SDEN setup time prior to SCLK fall	Tsens		35			ns
SDEN hold time after SCLK rise	Tsenh		50			ns
SDEN low time	Tsl		200			ns
SDATA setup time prior to SCLK rise	Tds		15			ns
SDATA hold time after SCLK rise	Tdh		15			ns
SCLK pulse width	Tckpw		100			ns
SCLK high time	Tckh		40			ns
SCLK low time	Tckl		40			ns

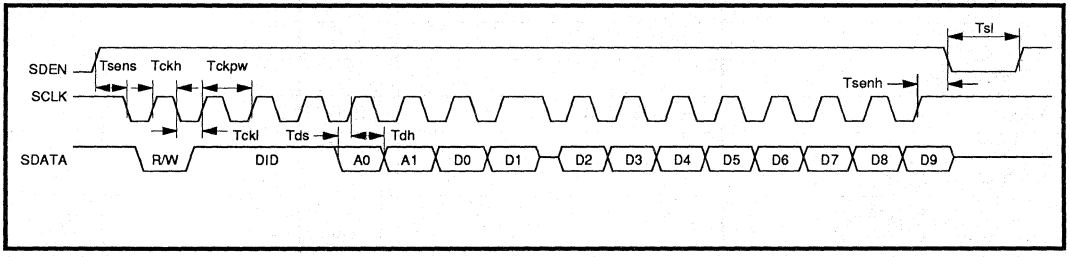
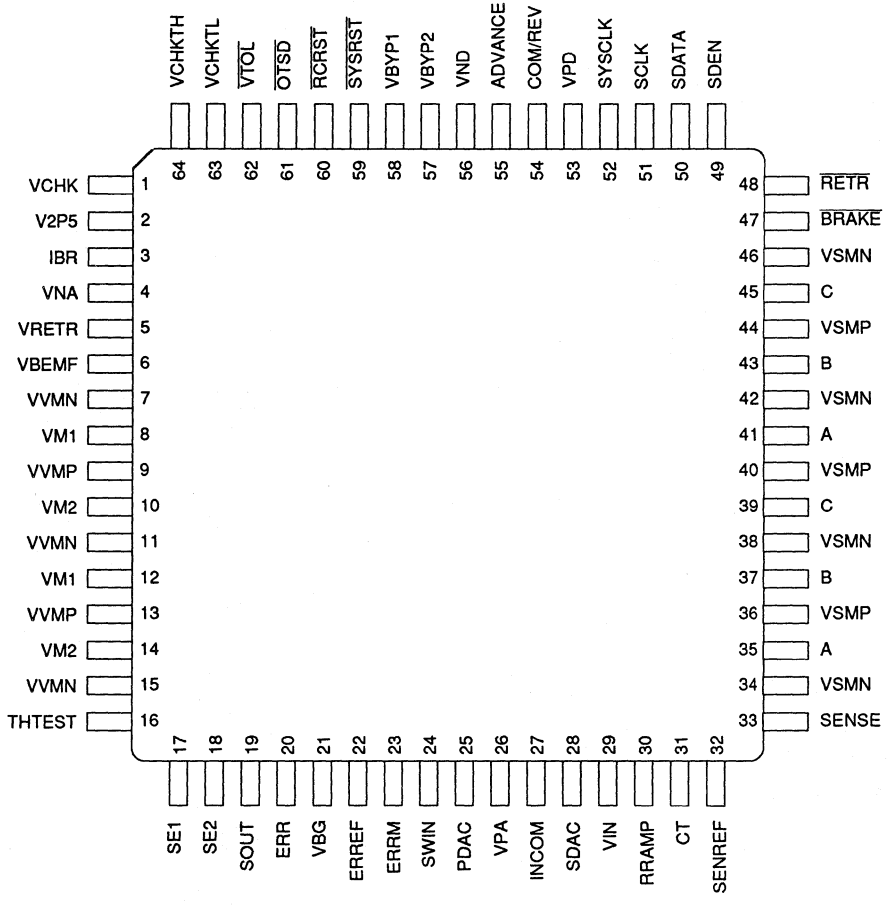


FIGURE 2: Serial Interface Port Timing Diagram

PACKAGE PIN DESIGNATIONS

(Top View)



64-Lead TQFP

CAUTION: Use handling procedures necessary for a static sensitive component.

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Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914

Notes:

silicon systems®
A TDK Group Company

SSI 32H6820
Servo/Spindle Predriver

Advance Information

November 1993

DESCRIPTION

The SSI 32H6820 is a CMOS monolithic integrated circuit housed in a 64-pin TQFP, operates from a single +5V supply and provides control signals for external FET drivers operating on 5 to 12 volt supplies. In addition to supporting disk drives with embedded servo sectors, it contains all timing and control functions necessary to start, drive, and brake a 3-phase, 4-, 8-, 12-, 16-pole brushless DC spindle motor without sensors. The circuit is controlled via the Silicon Systems standard 3-wire serial port.

FEATURES

Servo Head Positioning Control

- **Servo control for embedded servo head positioning systems**
- **H-bridge MOSFET pre-driver for linear and rotary voice coil motor**
- **Class B linear mode and constant voltage retract mode**
- **Active head retract on power failure**

Spindle Motor Speed Control

- **3-phase 4-, 8-, 12-, 16-pole bipolar/unipolar operation without need for sensors**
- **Programmable precision speed regulation 2µs speed resolution**
- **"At speed" indication**
- **Motor peak current limiting function**
- **Pulse amplitude modulation (PAM) for bridge MOSFET drivers**
- **Dynamic braking function on power failure**

General Functions

- **Voltage fault detection for two supply voltages**
- **Low power CMOS design, two low power idle states**
- **Three wire serial control interface**
- **8 bit Digital-to-analog converter for voice coil control**
- **Available in 64-lead TQFP package**

FUNCTIONAL DESCRIPTION

As shown in Figure 1, the SSI 32H6820 can be divided into four major sections: servo head positioning control, spindle motor speed control, digital control, and miscellaneous functions.

SERVO HEAD POSITIONING CONTROL

The SSI 32H6820 is intended for a servo head positioner for disk drives with embedded servo sectors. The head positioning control section contains the following sections: servo position error amplifier, H-bridge MOSFET pre-driver, actuator current sense, and voltage fault detection and servo head retract.

SERVO POSITION ERROR AMPLIFIER

The servo driver has two modes of operation, linear and retract. The retract mode is activated by a power supply failure or when the control signal RETRACT is low. Otherwise the driver operates in linear mode. During linear operation, the microcontroller acquires servo burst amplitudes and analyzes them to establish a position error signal. The microcontroller develops a digital error signal which is sent to the 8-bit D/A converter (with output ERRDAC and reference ERRREF) and is applied to an amplifier whose three connections, ERRM, ERRP and ERR, are available externally. External R-C components may be used to establish the gain and bandwidth of this amplifier. Additional analog input via SWIN may be provided to this amplifier by setting the SWON bit in the SERVO CONTROL register.

H-BRIDGE MOSFET PRE-DRIVER

The error signal ERR generated from the position error amplifier drives two precision differential amplifiers, each with a gain of 15. The differential amplifier outputs, AOUTA, AOUTB, AOUTC and AOUTD drive an external MOSFET bridge powered by VBRIDGE. Feedback from the MOSFET drain terminals via sense inputs SE1 and SE3 allow the differential amplifier gains to be established precisely. The voice coil actuator and a current sense resistor are connected in series between SE1 and SE3. Included in the output control circuitry is a crossover protection function which ensures class B operation by permitting only one MOSFET in each leg of the bridge to be in conduction. The crossover circuit can be adjusted for different MOSFET threshold voltages with a resistor connected to VX. The crossover

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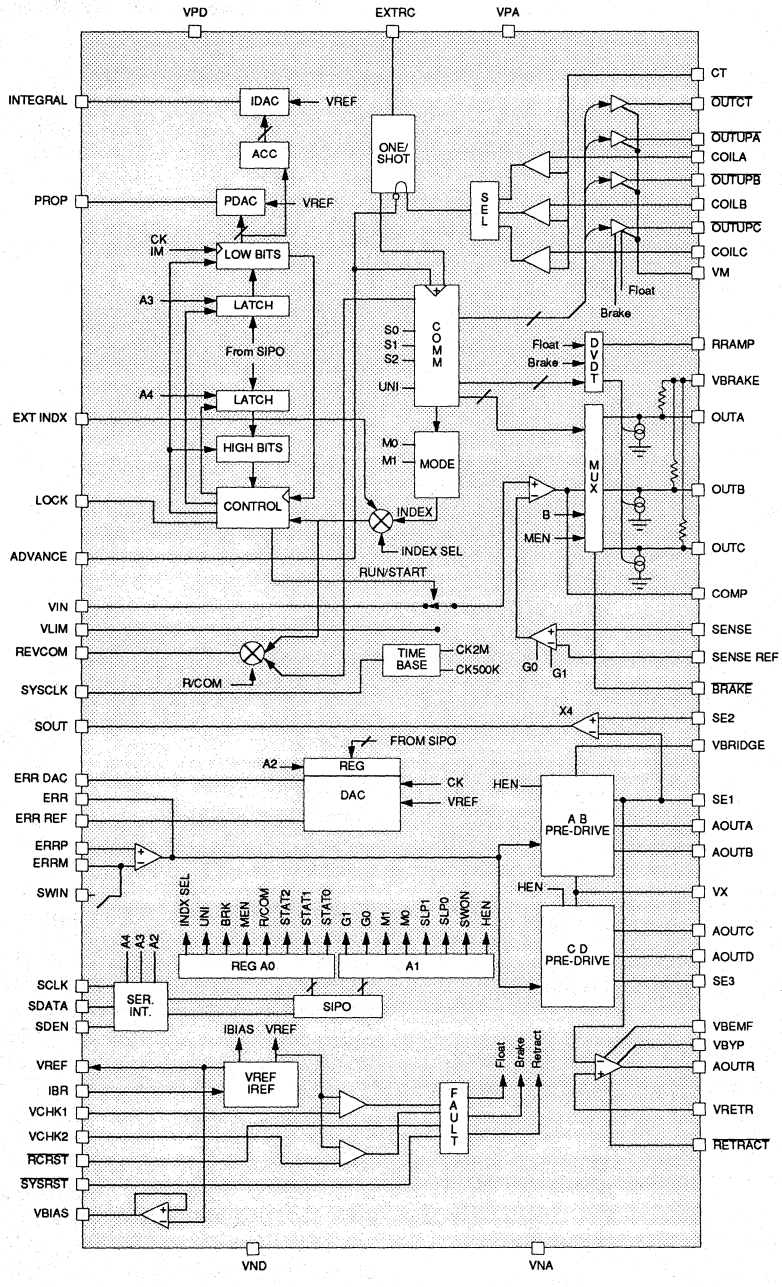


Figure 1: SSI 32H6820 Block Diagram

FUNCTIONAL DESCRIPTION (continued)

H-BRIDGE MOSFET PRE-DRIVER (continued)

circuitry can be commanded by the µP to shut down the MOSFET drivers and thus remove current to the external bridge.

MOTOR CURRENT SENSE

Motor current is sensed by a resistor placed in series with the actuator. The voltage drop across the resistor is level-shifted and amplified by a differential amplifier with a gain of 4. The resulting signal, SOUT, is proportional to actuator current. This signal is externally fed back to the position error amplifier so that the error signal ERR represents the difference between the desired and actual actuator currents.

VOLTAGE FAULT DETECTION AND SERVO HEAD RETRACT

During retract, a constant voltage is applied across the actuator in order to cause a constant velocity head retraction. This is accomplished by applying the voltage stored on VBYP to AOUTD and by driving AOUTR with an amplifier that monitors SE1. The amplifier is powered by VBEMF. During retract, VRETR is biased by an internal voltage reference and determines the retract voltage. At other times, power is saved by disconnecting VRETR from the voltage reference and letting it be pulled to VBEMF by a high value resistor. External components (a diode, for instance) can be connected between VRETR and ground to modify the retract voltage.

An open-drain output, $\overline{\text{SYSRST}}$, which is active low while the servo driver is in retract mode, is provided for spindle motor braking. An external R-C delay may be used to defer braking until the head is retracted. The minimum duration of $\overline{\text{SYSRST}}$ being active low is determined by the external capacitor which is connected to pin $\overline{\text{RCRST}}$.

SPINDLE MOTOR SPEED CONTROL

In conjunction with several external components, the spindle motor speed control provides the starting, accelerating, and precise rotational speed regulation functions. The circuit will control 4-, 8-, 12-, or 16-pole brushless DC motors without the need for Hall sensors. It will operate in either bipolar or unipolar drive mode. Control, configuration, and status monitoring are handled by a companion ASIC or µP. The complete speed control loop is contained in the circuit and the µP is only required during start and to monitor status.

SPINDLE MOTOR START-UP

Motor starting is accomplished with the µP utilizing various features contained in the motor speed control circuitry. The µP can write to the commutation counter and set it to a predetermined value with STAT0, STAT1, STAT2 bits. The counter can then be incremented with the ADVANCE pin which also excludes internal commutations when held HIGH. Bit REVCOM informs the µP on motor activity. The µP can enable the drivers with MEN and UNI bits as required.

Under µP control, initial open-loop commutation sequence is provided to the commutation logic which thereby advances and accelerates the spindle motor. The start-up process settles the motor initially by selecting the bits STAT0, STAT1, STAT2 in Register 0 to energize a proper motor winding. Motor current is enabled by setting the MEN bit in Register 0. The commutation state is advanced by raising the ADVANCE pin. The period between ADVANCE pulses will be based upon the motor and load characteristics and decreased gradually during the acceleration of the motor. The µP may look at the REVCOM pin information indicating whether the motor has achieved a sufficient speed. Once the motor has achieved a sufficient speed, ADVANCE is held low and the motor will accelerate to target speed.

Motor rotor position is determined by monitoring the coil voltage of the winding that is not presently being driven by the drivers. The back-emf at the coil in conjunction with the state of the output drivers indicates rotor position. The back-emf is compared to a reference at CT and initiates "commutation events" when the appropriate comparison is made. Commutation is the sequential switching of the drive current to the motor windings. Since the back-emf comparison event occurs prior to the time when optimum commutation should occur, it is thus required to delay actual commutation by a predetermined time after the comparison. The commutation delay is provided by a non-retriggerable one-shot circuit wherein the time delay is a function of external R-C timing components connected at EXTRC. Because commutation of the motor windings typically results in large transient voltages which could falsely indicate "commutation events," the one-shot circuit also provides a "noise filter" function which holds off retriggering further and blanks the back-emf comparison events for a period of time (approximately one half the commutation delay) after commutation (Figure 3). The commutation states are defined inTable 4.

FUNCTIONAL DESCRIPTION (continued)

SPINDLE MOTOR SPEED REGULATION

Motor speed regulation is accomplished with mixed analog and digital techniques, converting a motor speed error derived from a reference clock and a period counter into a voltage. The voltage translates into a motor current across the current sense resistor regulating the motor speed. The speed regulation loop consists of a period counter, proportional and integral channels, two 6-bit D/A converters and a linear transconductance amplifier.

In operation, the motor speed error is determined by measuring the period of each revolution with a 500 kHz clock signal. Period resolution is therefore 2 µs with the desired period being given by:

period = (load count + 6) • 2.0 µsec

Both register 3 and register 4 must be written, in order, via the serial data interface to accomplish writing a new period value.

The period counter is loaded with the desired count initially, and period measurement results in residual counts (ideally zero) in the period counter as it counts down during the index-to-index time interval. The residual count is fed to the proportional D/A converter (5-bit plus sign) whose output is provided at PROP. No period error will output half of VBIAS at PROP, too short a period will output a value less than half of VBIAS, and too long a period will output a value greater than half of VBIAS depending on the amount of error. When the residual count is within ±15 counts of zero, the motor is indicated as "in lock." The lower eight bits of the period counter are fed to an accumulator which adds the present period residue to the previous accumulation thus accomplishing an integrating effect to force the speed error to zero over time. The upper six bits of the accumulator are fed to the integral DAC whose output is INTEGRAL. Gross period errors will cause PROP and INTEGRAL to saturate at the appropriate extreme to achieve the maximum corrective control voltage.

The outputs at PROP and INTEGRAL are connected to VIN with an external resistor network. The outputs of the proportional DAC and Integral DAC give coefficients given by:

$$K_p = (RPS^{-2})/(2.35v/64)/4\pi e^{-6})$$

$$K_I = (RPS^{-1})/(2.35v/64)/(16\pi e^{-6})$$

(RPS is the desired motor speed in revolutions per second.)

The resistor values should be selected to modify the coefficients given above to values required for proper loop response based upon motor requirements. The input VIN is the non-inverting input of the linear transconductance amplifier which uses the lower driver transistor that is presently active per the commutation state. An external resistor is used to sense the current flowing through the drive transistor drain (and hence the motor coil current). The voltage across the sense resistor, the difference between SENSE and SENSEREF, is amplified by a programmable gain stage and fed to the inverting input of the transconductance amplifier. The gain of the programmable amplifier is determined by G0 and G1 bits.

MOTOR PEAK CURRENT LIMITING

When the period error exceeds 256 counts too slow, the voltage at VLIM is selected as the control voltage in lieu of VIN. VLIM is to be used to set the motor peak current during start-up and acceleration. The motor current is limited to a value such that the voltage across the sense resistor (SENSE - SENSEREF) times the gain of the sense amplifier (5, 10, 15, 20) is equal to VLIM.

MOTOR BRAKING

Fault conditions on power supplies and internal voltage reference generator will trigger an internal retract condition. The internal retract condition will cause all pre-driver outputs to the states which will turn the driver transistors off, allowing the motor to coast. $\overline{\text{BRAKE}}$ typically has a capacitor to ground attached and is connected to pin $\overline{\text{SYSRST}}$ via a resistor. $\overline{\text{SYSRST}}$ goes low in the retract condition, and thus $\overline{\text{BRAKE}}$ will go low after the R-C delay. When $\overline{\text{BRAKE}}$ goes low, all external N-FETs are activated to achieve dynamic braking of the motor. The circuitry for these operations is powered by voltage on VBRAKE stored on an external capacitor.

Dynamic braking can also be activated under external serial port control by setting BRK to HIGH in REG 0. During dynamic braking, the control loop is opened.

EXTERNAL INDEX APPLICATION

Normal operation is performed with an internal index signal derived from the commutation counter (scaled via the M0 and M1 bits based upon the number of motor poles). For both an internal "index" or External Index, the period between index signals is measured as described above and used to control the PROP and INTEGRAL outputs.

DATA CONVERSION AND SERIAL INTERFACE

An 8-bit D/A converter which runs synchronously with the internal 500 kHz clock is provided. The converter is 2's complement format (7 Fhex is positive full scale, 80 hex is negative full scale and Reset condition is 00 hex, midscale). Conversion is started by writing to the D/A register address, Register 2. The output of the D/A converter is ERRDAC and is referenced to ERREF. The output is held constant between data loads. The circuit is configured and controlled via the Serial data inputs in accordance with the standard Silicon Systems Serial interface Specifications.

Per the timing diagram (Figure 2), data are clocked into the serial port on the rising edge of SCLK. It is required that 16 data clocks be used for all transfers for proper operation. The data are loaded from the serial interface to the destination registers (controlled parameter) when SDEN is lowered signalling the end of serial data transfer.

MISCELLANEOUS FUNCTIONS

The miscellaneous functions include generating the reference voltages VREF and VBIAS, and the voltage fault detection circuits which activate power fault retract and braking operation. A voltage fault detector which can monitor two voltage supplies is included to prevent the actuator from responding to a false error signal during a power failure. Retract mode is started when a power supply failure is sensed by the VCHK1 or VCHK2 comparators or when $\overline{\text{RETRACT}}$ is pulled low externally.

The internal bias currents for analog functions are set by an external resistor connected between IBR and ground. A 23.7 kΩ ±1% resistor should be used for proper operations.

TABLE 1: Serial Data Format

Data bit 1	R/$\overline{\text{W}}$ control - must be a 0, this circuit is write-only
Data bit 2	Circuit ID bit - must be 1
Data bit 3	Circuit ID bit - must be 1
Data bit 4	Circuit ID bit - must be 1
Data bit 5	Register address bit 0
Data bit 6	Register address bit 1
Data bit 7	Register address bit 2
Data bit 8	Register address bit 3 - not used, 1 or 0 allowed
Data bit 9	Register data bit 0
Data bit 10	Register data bit 1
Data bit 11	Register data bit 2
Data bit 12	Register data bit 3
Data bit 13	Register data bit 4
Data bit 14	Register data bit 5
Data bit 15	Register data bit 6
Data bit 16	Register data bit 7

TABLE 2: Operating Modes

MODE	VFAULT condition	$\overline{\text{RETRACT}}$ PIN	$\overline{\text{BRAKE}}$ PIN	SLEEP BIT	HEN BIT	MEN BIT	BRK BIT	POS driver	SPINDLE driver
SLEEP (1)	X	X	X	1	X	X	X	float	float
VFAULT retract (2)	1	X	1	0	X	X	X	retract	float
VFAULT brake (3)	1	X	0	0	X	X	X	retract	brake
RETRACT	0	0	1/0	0	X	X	X	retract	float/brake
BRAKE	0	1/0	0	0	X	X	X	float/retract	brake
BRAKE Register	0	1	1	0	1/0	X	1	on/float	brake
IDLE	0	1	1	0	0	0	0	float	float
SPIN only	0	1	1	0	0	1	0	float	on
SERVO coast	0	1	1	0	1	0	0	on	float
RUN	0	1	1	0	1	1	0	on	on

(1) All analog circuits off
(2) Initiated by low power supply voltage
(3) Vfault followed by RC delay from $\overline{\text{SYSRST}}$ to $\overline{\text{BRAKE}}$

REGISTER DESCRIPTIONS

The SSI 32H6820 contains five 8-bit internal registers which provide control and option select. Writing to an address other than 0 to 4 will have no effect.

TABLE 3: Internal Registers

ADDRESS 0

BIT	NAME	FUNCTION
0	STAT0	LSB of commutation state counter preset value - Refer to Table 4.
1	STAT1	Commutation state counter preset value.
2	STAT2	MSB of commutation state counter preset value.
3	R/COM	Selects REVCLK (once per revolution) when set low or COMMU when set high as output on pin REVCOM.
4	MEN	Motor enable. Active high enables spindle motor drive. Reset to low on power on.
5	BRK	BRAKE function when set high. Spindle lower drivers full on with no current limiting.
6	UNI	Selects UNIPOLAR mode, upper spindle drivers off, $\overline{CT}$ driver on (low).
7	INDX_SEL	Selects external index when set high.

ADDRESS 1

0	HEN	Enable head driver outputs. Reset to low on power on.
1	SWON	Close switch between ERR and SWIN. Set open on power on reset.
2	SLP0	Sleep mode control bit. When set high, head positioner and motor analog circuits are inactive with drivers off. Miscellaneous circuitry is still active.
3	SLP1	Full SLEEP mode select. Overrides SLP0 bit. All analog circuits de-biased and internal clocks are off. Only the serial data port is operable.
4	M0	Spindle motor pole configuration mode. See below.
5	M1	Spindle motor pole configuration. M0 = 0, M1 = 0 for 4 poles M0 = 1, M1 = 0 for 8 poles M0 = 0, M1 = 1 for 12 poles M0 = 1, M1 = 1 for 16 poles
6	G0	Spindle motor current sense amplifier gain control.
7	G1	Spindle motor current sense amplifier gain control. G0 = 0, G1 = 0 for gain of 5 G0 = 1, G1 = 0 for gain of 10 G0 = 0, G1 = 1 for gain of 15 G0 = 1, G1 = 1 for gain of 20

REGISTER DESCRIPTIONS (continued)

ADDRESS 2

BIT	NAME	FUNCTION
0	DAC0	DAC LSB
1	DAC1	DAC data bit 1
2	DAC2	DAC data bit 2
3	DAC3	DAC data bit 3
4	DAC4	DAC data bit 4
5	DAC5	DAC data bit 5
6	DAC6	DAC data bit 6
7	DAC7	DAC MSB

ADDRESS 3

0	CNT0	Period counter LSB
1	CNT1	Period counter bit 1
2	CNT2	Period counter bit 2
3	CNT3	Period counter bit 3
4	CNT4	Period counter bit 4
5	CNT5	Period counter bit 5
6	CNT6	Period counter bit 6
7	CNT7	Period counter bit 7

ADDRESS 4

0	CNT8	Period counter bit 8
1	CNT9	Period counter bit 9
2	CNT10	Period counter bit 10
3	CNT11	Period counter bit 11
4	CNT12	Period counter bit 12
5	CNT13	Period counter bit 13
6	CNT14	Period counter bit 14
7	CNT15	Period counter MSB - Always load 0 in this bit

TABLE 4 (See Table 2)

STATE	STAT 2	STAT 1	STAT 0	OUTA	OUTB	OUTC	$\overline{\text{OUTUPA}}$	$\overline{\text{OUTUPB}}$	$\overline{\text{OUTUPC}}$	REVCOM (COMMU SELECTED)
0	0	0	0	OFF	ON	OFF	ON	OFF	OFF	1
1	0	0	1	OFF	OFF	ON	ON	OFF	OFF	0
2	0	1	0	OFF	OFF	ON	OFF	ON	OFF	1
3	0	1	1	ON	OFF	OFF	OFF	ON	OFF	0
4	1	0	0	ON	OFF	OFF	OFF	OFF	ON	1
5	1	0	1	OFF	ON	OFF	OFF	OFF	ON	0
	1	1	0	No load for						
	1	1	1	110 or 111						

PIN DESCRIPTION

POWER SUPPLIES

NAME	TYPE	DESCRIPTION
VPA	P	Analog +5V supply.
VPD	P	Digital +5V supply. VPA and VPD must be within 0.3V of each other at all times.
VNA	P	Analog ground.
VND	P	Digital ground.

HEAD POSITIONER MOSFET DRIVER AND VOLTAGE FAULT DETECTION

ERRM	I	Error Amplifier Inverting Input - Inverting input to the position error amplifier of the MOSFET pre-driver.
ERRP	I	Error Amplifier Non-inverting Input - Non-inverting input of the error amplifier. Typically connected to ERRREF pin directly.
SWIN	I	This input is shorted to ERRM when the bit SWON is set HIGH. SWIN floats otherwise.
ERR	O	Acceleration Error - Position error amplifier output. This signal is amplified by the MOSFET drivers and applied to the actuator through an external MOSFET H-bridge as follows:
		SE3-SE1 = 30 (ERR-VREF)
ERRDAC	O	DAC output pin, referenced to ERREF.
ERREF	O	Reference voltage for DAC output. Connected to non-inverting input of error amplifier.
AOUT(A,C)	O	PFET Driver - Drive signals for P-channel MOSFETs connected between VBRIDGE and the voice coil actuator. Crossover protection circuitry ensures that the external P- and N-channel FETs driven by AOUT(A,C) and AOUT(B,D) are never enabled simultaneously.
AOUT(B,D)	O	NFET Driver - Drive signals for N-channel MOSFETs connected between the current sense resistor and the voice coil actuator.

PIN DESCRIPTION (continued)

HEAD POSITIONER MOSFET DRIVER AND VOLTAGE FAULT DETECTION (continued)

NAME	TYPE	DESCRIPTION
VBRIDGE	I	Bridge Voltage Supply - Pin for connection to the voltage supply provided to external power transistors.
VRETR	I	Retract Voltage - In head retract mode this voltage is applied across the actuator to force the heads to move at a constant speed.
AOUTR	O	Head Retract Amplifier Output - Voltage output to drive an external head retract circuit.
SE1, SE3	I	Motor Voltage Sense Input - These inputs provide feedback to the internal MOSFET drive amplifier.
SE2	I	Motor Current Sense Input - Non-inverting input to the current sense differential amplifier. It should be connected to an external current sense resistor. The inverting input of the differential amplifier is SE1.
SOUT	O	Motor Current Sense Output - This output provides a voltage proportional to the voltage drop across the external current sense resistor as follows:
		SOUT-ERREF = 4 (SE2-SE1)
VX	O	Crossover Protection Voltage - The current source output at VX is converted to a voltage with an external resistor. The value of the resistor should be adjusted so that VX is less than the specified minimum threshold voltage of the MOSFET bridge.
VBYP	I	Bypass Voltage Supply - The VBRIDGE voltage is stored on this node for use during retract.
VCHK1, VCHK2	I	Fault Voltage Comparator Inputs - Voltage inputs for the low voltage comparators. These two inputs should be connected to separate external resistor dividers. Each resistor divider divides its corresponding supply voltage to a proper value which is comparable with the internal voltage reference at 2.35 volts.
VREF	O	Internal Voltage Reference - A voltage reference at 2.35 volts is generated internally for the DC reference level throughout the device. Due to limited drive capability provided with on-chip voltage reference, this pin shall be used only for connecting an external bypass capacitor of 10 μF.
IBR	O	Bias Current Reference - Pin for connection to an external resistor (from VNA) to establish a reference current for bias currents used in analog circuits.
$\overline{\text{RETRACT}}$	I	Retract Input - When set low, the head positioner is put into retract mode.
SYSRST	O	Active low, open drain output signal which indicates that a voltage fault has occurred or $\overline{\text{RCRST}}$ pin has been pulled low externally.
RCRST	I	An external R/C network at this pin will stretch short (internally detected) voltage fault pulses and set a minimum $\overline{\text{SYSRST}}$ pulse width. When this pin is pulled low externally, $\overline{\text{SYSRST}}$ will go low and the device will enter the retract mode.

SPINDLE MOTOR SPEED CONTROL

NAME	TYPE	DESCRIPTION
EXTINDX	I	External Index Input - This TTL compatible input, when selected via the INDEXSEL bit, is used to provide a once-per-revolution indication of angular position and speed to the device. The falling edge of EXTINDX is the reference.
SYSCLK	I	System Clock Input - A 4 MHz, TTL compatible input is provided to derive internal timing signals.
ADVANCE	I	Input signal used to increment the commutation state counter. When held high, the commutation counter is prevented from incrementing due to back-emf signals from the motor.
EXTRC	I	Pin for connection to a resistor (from VPD) and a capacitor (from VND) to provide the commutation delay. The commutation delay is 0.56 R-C. After the commutation delay, the timing block provides a noise rejection interval to reject transients on the motor coils due to commutations. This noise rejection is an additional 0.29 R-C. The total time (commutation delay and noise rejection internal) must be less than a commutation cycle time.
BRAKE	I	Spindle Braking Enable - This input, when active low, dynamically brakes the spindle motor. A resistor (from $\overline{\text{SYSRST}}$) and a capacitor (from VND) are connected to this pin to provide a delay between the initiation of fault-induced head retraction and motor braking. R-C are selected such that 1.2 R-C is equal to the maximum time required for head retraction.
VBIAS	O	Buffered Bias Voltage - VBIAS is buffered VREF to be used for VLIM and motor speed setting bias. (In some applications, it is necessary to create an "offset" to the speed control loop to obtain proper speed regulation.)
PROP	O	Proportional Channel D/A Output - The proportional channel output is the least significant 5 bits plus sign of the period measuring counter. The LSB signifies a 2 µs period variation.
INTEGRAL	O	Integral Channel D/A Output - The integral channel output is the most significant 6 bits of an 8-bit accumulator. The accumulator adds the least 8 bits of the period measurement counter to the previous value obtained from prior period measurements and accumulations.
VIN	I	Speed Control Voltage Input - The combination of external driver transistors and internal pre-driver circuits forms a transconductance amplifier which will define the motor current in relation to VIN. In conjunction with the SENSE input and the gain setting for the sense amplifier, the transconductance gain is given by: gm=IMOTOR/VIN=1/(RSENSE•Gain) where IMOTOR is the current flowing through the spindle motor coils, RSENSE the current sense resistor and Gain is the gain of the current sense amplifier as set by the gain control bits G0 and G1.
VLIM	I	Current Limit Setting Voltage - The spindle motor current will be limited to a value determined by RSENSE, VLIM and Gain such that Imax=VLIM/(RSENSE•Gain). VLIM is used whenever the spindle speed is measured to be 256 counts too slow.

PIN DESCRIPTION (continued)

SPINDLE MOTOR SPEED CONTROL (continued)

NAME	TYPE	DESCRIPTION
SENSE	I	Current Sense Amplifier Non-inverting Input - The external driver transistor sources are connected to a current sense resistor RSENSE to monitor motor current. The device will control the voltage across the sense resistor to match either VIN (during normal operation) and VLIM (during acceleration) such that: (VSENSE - VSENSEREF) • Gain = VLIM or VIN
SENSEREF	I	Current Sense Amplifier Reference Input - Pin for a Kelvin connection to the ground side of the sense resistor.
OUT(A,B,C)	O	Pre-driver Outputs - These pre-driver outputs drive the gates of external power NFETs.
$\overline{\text{OUTUP}}$(A,B,C)	O	Upper Pull-up Outputs - These pre-driver outputs drive the gates of external power PFETs. They are configured as open-drain outputs with internal 10 kΩ pull-up resistors to VM.
$\overline{\text{OUTCT}}$	O	Center Tap Pre-driver - This output drives an external PFET driver which connects the motor center tap to VM for unipolar drive applications. $\overline{\text{OUTCT}}$ has the same characteristics as $\overline{\text{OUTUP}}$ (A,B,C) and is enabled via the UNI bit.
VM	I	Spindle motor upper driver power supply pin.
VBRAKE	I	This pin provides the power for spindle motor braking upon power loss. An external diode from VM is used to charge an energy storage capacitor (10 µF, typical) which provides gate drive voltage for the external NFETs.
RRAMP	I	An external resistor (to VPD) sets the lower driver turn-off characteristics for noise reduction, 100 KΩ typical.
VBEMF	I	Back-emf Voltage - A power diode voltage drop from the system power supply is defined as VBEMF. For "power-fail" retract and braking, VBEMF is connected to VM and the external PFET sources. During power failure, the diodes in the PFETs rectify the motor voltage for head retract power.
COIL(A,B,C)	I	Back-emf Inputs - Inputs to be connected to their respective motor coils and the center tap for sensing generated back-emf voltages. The device uses the back-emf voltages to determine the rotor position and effect commutation.
CT	I	Center tap of motor used as reference for back-emf comparison.
REVCOM	O	Output selected by R/COM bit in REG 0 to be either REVCLK (once per revolution) or COMMU, the LSB of the commutation state counter.
LOCK	O	Output true indicates rotational period of motor is within ± 30 µs of desired value.
COMP	I	Compensation capacitor for the spindle transconductance loop. Typical value 0.01 µF to 0.1 µF.

SERIAL DATA INTERFACE

NAME	TYPE	DESCRIPTION
SDEN	I	Serial Data Enable, active high. SDEN is raised prior to serial data input and lowered after 16 SCLK pulses.
SCLK	I	Serial Data clock, falling edge clocks serial data into circuit.
SDATA	I	Serial Data input consisting of 8-bit mode and address word followed by 8-bit data word (MSB last). The first bit clocked in is the mode bit which for this circuit is Write mode only, (write a zero).

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device or affect reliability.

PARAMETER		RATING
Voltage applied to VPA, VPD	VDD	0.1 to 14.0
Voltage applied to VBRIDGE	VBRIDGE	0.1 to 14.0
Voltage applied to VBYP	VBYP	0.1 to 14.0
Voltage applied to VBEMF	VBEMF	0.1 to 18
Voltage applied to VM	VM	0.1 to 14.0
Voltage applied to VBRAKE	VBRAKE	0.1 to 14.0
VBEMF current if VBEMF>18V	IBEMF	5.0
Signal pins	VMAX	-0.3 to VDD + 0.3
Storage temperature	Tstg	-65 to 150
Lead temperature	Tlead	300

OPERATING ENVIRONMENT LIMITATIONS

The recommended operating conditions for the device are indicated in the table below. Performance specifications do not apply where the device is operating outside these limits.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Supply voltage applied at VPA,VPD	VDD		4.5	-	5.5	V
Bridge voltage applied at VBRIDGE, VM	VBRIDGE VM		4.5	-	13.2	V
Ambient temperature	Ta		0.0	-	70.0	°C
System clock	Fc		3.92	4	4.08	MHz
Capacitive load	CL				100	pF
digital outputs						
Analog input impedance	Rin		100	-	-	kΩ

ELECTRICAL SPECIFICATIONS (continued)

OPERATING ENVIRONMENT LIMITATIONS (continued)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
	Cin		-	-	20	pF
Load on analog outputs	Rout		10	-	-	kΩ
	Cout		-	-	40	pF
Bias resistor	RBIAS	23.7 kΩ		±1		%

DC CHARACTERISTICS

The following electrical specifications apply to the digital input and output signals over the recommended operating range unless otherwise noted. Positive current is defined as entering the device. Minimum and maximum are based upon the magnitude of the number.

Supply current	IDD	VDD = 5.5V	-	-	30	mA
		SLP0	-	-	15	mA
		SLP1			50	µA
Supply current on VBRAKE	IBRK	VBRAKE = 12V VDD = 0V	-	-	25	µA
Supply current on VBYP	IBYP	VBYP = 12V	-	-	25	µA
Output logic 1	Voh	Ioh = -0.4 mA VDD = 4.5V	2.4	-	-	V
Output logic 0	Vol	Iol=1.6 mA VDD=4.5V	-	-	0.4	V
Input logic 1	Vih	VDD=4.5V	2.0	-	-	V
Input logic 0	Vil	VDD=4.5V	-	-	0.8	V
Input logic 1 current	Iih	Vih=5.5V VDD=5.5V	-	-	10	µA
Input logic 0 current	Iil	Vil=0.0 VDD=5.5V	-	-	-10	µA
Input capacitance	Cin		-	-	10	pF

FUNCTIONAL CHARACTERISTICS

Head Positioner MOSFET Driver

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VRETR voltage	VBEMF = 3V	0.3	-	0.9	V
	VBEMF = 12V	0.4	-	1.2	V
Retract offset	VBEMF = 3V VRETRACT = 0.5V	-70		50	mV
	VBEMF = 6V VBYP = 4V to 13V	-70		70	mV
	VBEMF = 12V IAOUTR < 1mA	-150	-	150	mV
Voh at AOUTR	Ioh = -1 mA VBEMF = 4V VBYP = 4V	1.5	-	-	V
	VBEMF = 3V VBYP = 4V	1.3	-	-	V
Leakage current at AOUTR	$\overline{\text{RETRACT}}$ = LOW AOUTR = 0V to 14V	-	-	1	µA
Voh at AOUTA, AOUTC	Ioh = -1 mA	VBRIDGE -1.5			V
	Ioh = -1 µA	VBRIDGE -0.1		-	V
Vol at AOUTA, AOUTC	Iol = 10 µA	-		1	V
Voh at AOUTB	Ioh = -10 µA	VBRIDGE -0.5		-	V
Voh at AOUTD	Ioh = -10 µA	VBYP -0.5		-	V
Vol at AOUTB, AOUTD	Iol = 1 mA	-	-	1	V
	Iol = 10 µA		-	0.2	V
Input offset at SOUT		-	-	±3	mV
SOUT/(SE1-SE2)		3.9	-	4.1	V/V
SE1/ERR, SE3/ERR		14.0		15.4	V/V
ERRAMP input offset		-	-	±10	mV
ERRAMP gain			1000	-	V/V
Output crossover time PFET VTH = -2V CL = 600 pF at AOUTA,C NFET VTH = 2V CL = 150 pF at AOUTB,D RX = 50 kΩ		-	-	45	µs
Input impedance at SE1, SE2, SE3		20	-	-	kΩ
Output resistance at SOUT		-	-	350	Ω
Analog switch on-resistance at SWIN		-	-	600	Ω
Output resistance at ERR		-	-	100	Ω
Output current from VX			TBD		µA

ELECTRICAL SPECIFICATIONS (continued)

FUNCTIONAL CHARACTERISTICS (continued)

Voltage Reference and Voltage Fault Circuit

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VPA voltage for $\overline{SYSRST}$ & $\overline{RCRST}$ in operation		2.0		-	V
On resistance at $\overline{RCRST}$ VPA > 3.5V VBRAKE > 4V		-	-	800	Ω
VPA > 3.5V VBRAKE > 10V		-	-	550	Ω
$\overline{RCRST}$ input threshold VBRAKE = 4V		0.8	-	2.0	V
IBR voltage w.r.t. VREF		-80	-	20	mV
Output voltage at VREF |IL| < 10 µA		2.28	2.35	2.42	V
VCHK1, VCHK2 comparator offset		2.25	-	2.45	V

Spindle Motor Speed Control

SYSCLK duty cycle		40	-	60	%
EXTINDX pulse width		200	-	-	ns
Advance pulse width		3	-	-	µs
Timing resistor at EXTRC		0.01	-	10	MΩ
Timing capacitor at EXTRC		100	-	-	pF
Delay time variation relative to T0*		-	-	±5	%
Vil at $\overline{BRAKE}$	VBRAKE = 5V	0	-	0.8	V
Vih at $\overline{BRAKE}$	VBRAKE = 5V	2.0	-	-	V
Output voltage swing at PROP & INTEGRAL	Iout < 0.1 mA	0	-	VBIAS ±5%	V
DAC step size at PROP, INTEGRAL		33	-	40	mV
Output impedance at PROP, INTEGRAL	0.5V < Vout < 2.0V Iout = 0.1 mA	-	-	300	Ω
VBIAS output w.r.t. VREF		-50	-	25	mV
Input voltage at VIN & VLIM		0	-	2.35	V
Input leakage current at VIN & VLIM		-	-	±1	µA

* NOTE: T0 is the commutation delay and is given by the relationship T0 = 0.56RC. Suggested value for C would be 470 to 1000 pF. An external R and C must be provided such that T0 is greater than 10 µs (R = 22 kΩ, C = 470 pF).

Spindle Motor Speed Control (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Output resistance at $\overline{\text{OUTUP}}$ (A,B,C) & $\overline{\text{OUTCT}}$	Output HIGH pulled to VM	5	-	20	kΩ
Vol at OUTUP (A,B,C) & OUTCT	Iout = 3mA VM = 13.2V		-	1.0	V
Voh, OUT (A,B,C)	Vpd = 5V, Vm ≥ 6V Iout = -50 µA	4.5	-		V
Vol at OUT (A,B,C)	Iout = 1 mA		-	1.0	V
Input voltage at SENSE	Av = 5	0.0		0.5	V
Input voltage at SENSEREF		0.0	-	0.05	V
Input leakage current at SENSE	0.0V < Vin < 1.0V	-	-	±10	µA
Input leakage current at SENSEREF	0.0V < Vin < 0.05V	-200	-	10	µA
Input capacitance at SENSE & SENSEREF		-	-	20	pF
Gain variation	Av = 5,10,15,20	-	-	±10	%
Input impedance at COIL(A,B,C)	-0.3V < Vin < 15V	100	-	-	kΩ
Input capacitance at COIL(A,B,C)		-	-	10	pF
Input impedance at CT		30	-	-	kΩ
Input capacitance at CT		-	-	10	pF
LOCK indication range		-30	-	+30	µs
Speed resolution			2		µs

The motor speed control loop can be described as: H(s)=Kp+Ki/s

The transconductance gain from VIN or VLIM to the steady-state current flowing through the motor is given by G = 1/(RSENSE • AV)

Error D/A Converter

ERRDAC full-scale voltage swing w.r.t ERREF		-	±(VREF/2)	-	V
Resolution		-	8	-	Bits
Conversion time*		-	4.0		µs
LSB voltage		-	VREF/256		mV
Output voltage at ERREF		1.568	1.616	1.664	V
ERRDAC offset w.r.t. ERREF		-	-	±5	mV
Differential linearity error		-	-	±0.75	LSB
Relative accuracy**		-	-	±1.0	LSB
Power supply sensitivity		-	-	±0.5	LSB

ELECTRICAL SPECIFICATIONS(continued)

Error D/A Converter (continued)

*A maximum of 4 µs of latency between a conversion request and the actual start of conversion must be added to this conversion time of 4 µs to calculate the total delay time from a conversion request to the completion of conversion.

**Relative accuracy is the deviation of the analog value at any code (relative to the full analog range of the D/A transfer characteristic) from its theoretical value (relative to the same range), after the full-scale range has been calibrated.

Serial Data Interface

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
SDEN enable to SCLK delay	Tsens		35			ns
SDEN hold past SCLK	Tsensh		40			ns
SDATA setup	Tds		15			ns
SDATA hold time	Tdh		15			ns
SDATA address word to data word	Tad		40			ns
SCLK cycle time	Tc		100			ns
SCLK width low	Twcl		40			ns
SCLK width high	Twch		40			ns

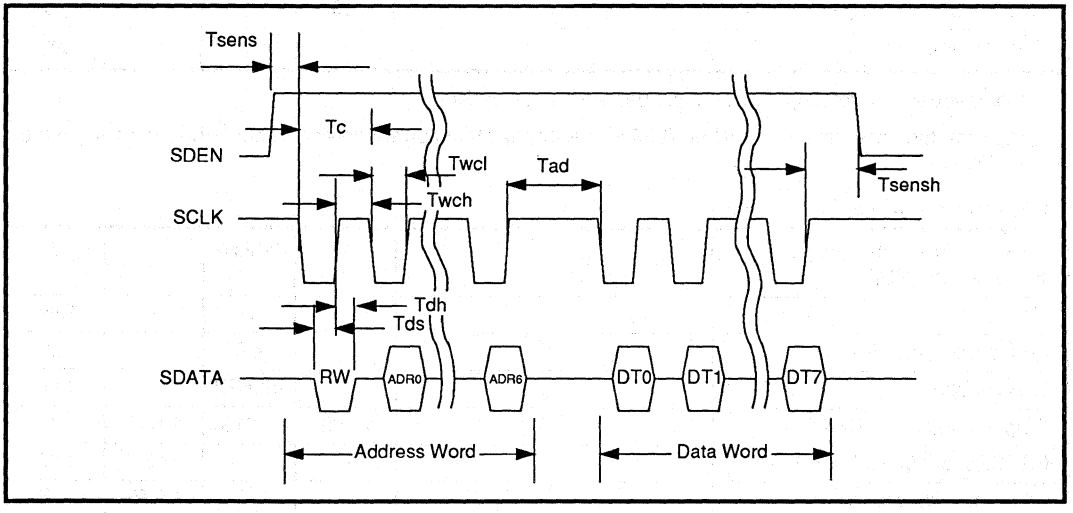


FIGURE 2: Timing Diagram

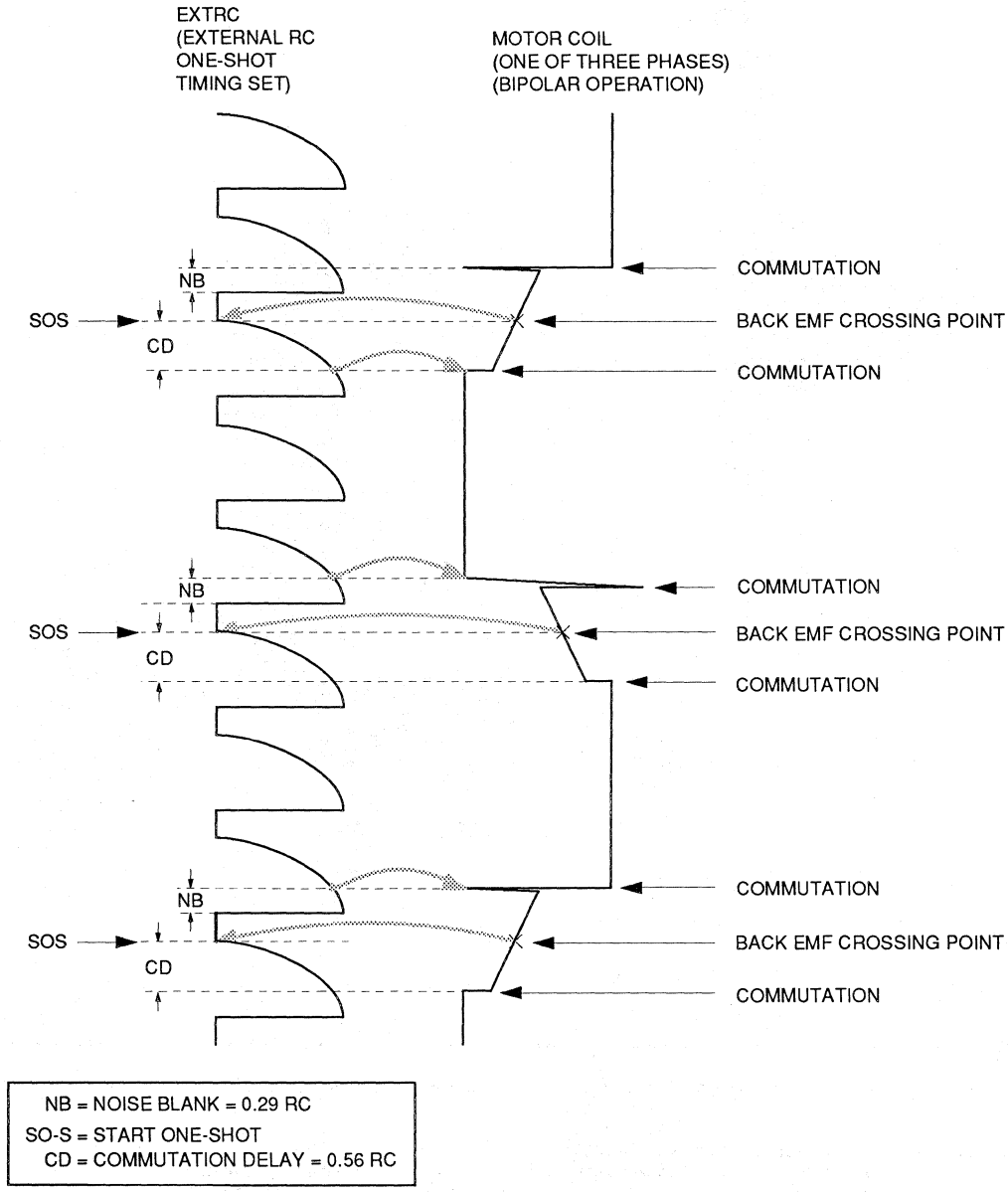
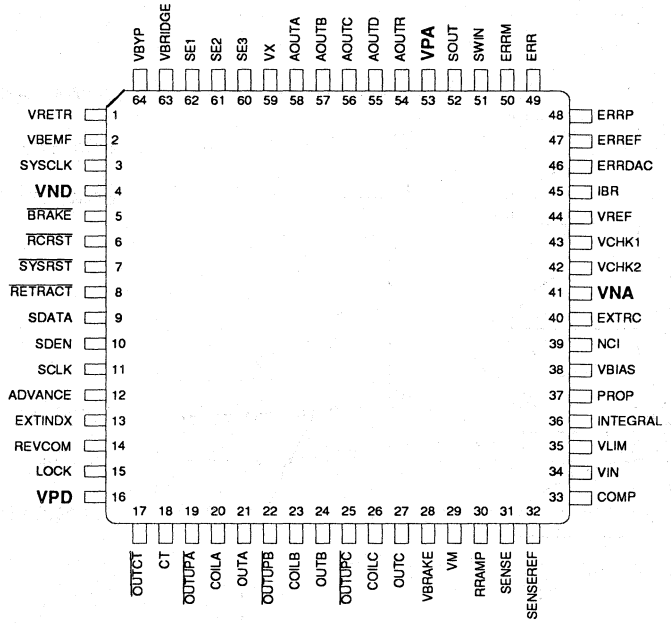


FIGURE 3: One-Shot Commutation Delay Timing Diagram

SSI 32H6820
Servo/Spindle
Predriver

PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



64-Lead TQFP

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914

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SSI 32H6825
Servo and Spindle Predriver

Advance Information

January 1994

DESCRIPTION

The Servo and Spindle Predriver (SSP) is designed to drive a 3-phase hall-sensorless motor and a voice coil actuator with external MOS power devices.

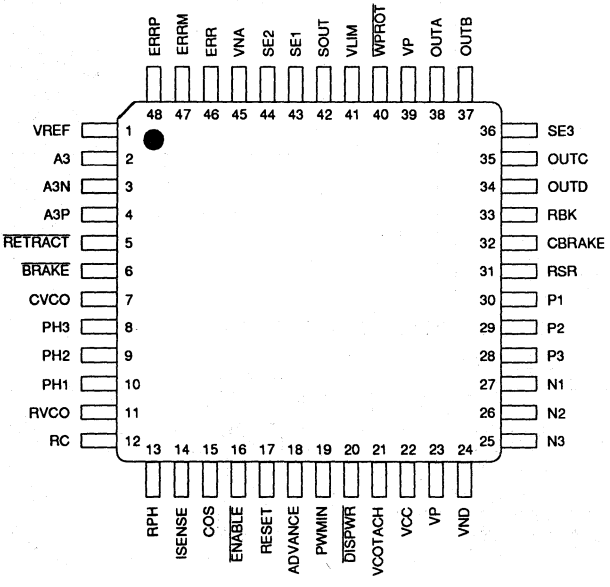
Improvements to the actuator driver include a window comparator to quickly catch high currents caused by power FET failure in the actuator bridge, an uncommitted opamp for use in a notch filter, and reduced power dissipation.

Improvements to the spindle driver include significantly reduced power dissipation, a µP controlled start up ramp to replace the imprecise analog ramp, an external PWM input to allow PWM frequencies above the audible range, active pullup on the P driver, adjustable N-channel slew rate, and improved spindle brake performance.

FEATURES

- **Spindle driver is PWM during run and start**
- **Commutator is driven by a phase lock loop for high jitter immunity**
- **Significantly reduced power dissipation**
- **Adjustable slew rate to minimize stress in the power FETs**
- **Microprocessor controlled spindle start up**
- **Window comparator to monitor actuator bridge fault**
- **Small footprint 48-Lead TQFP package**

PIN DIAGRAM

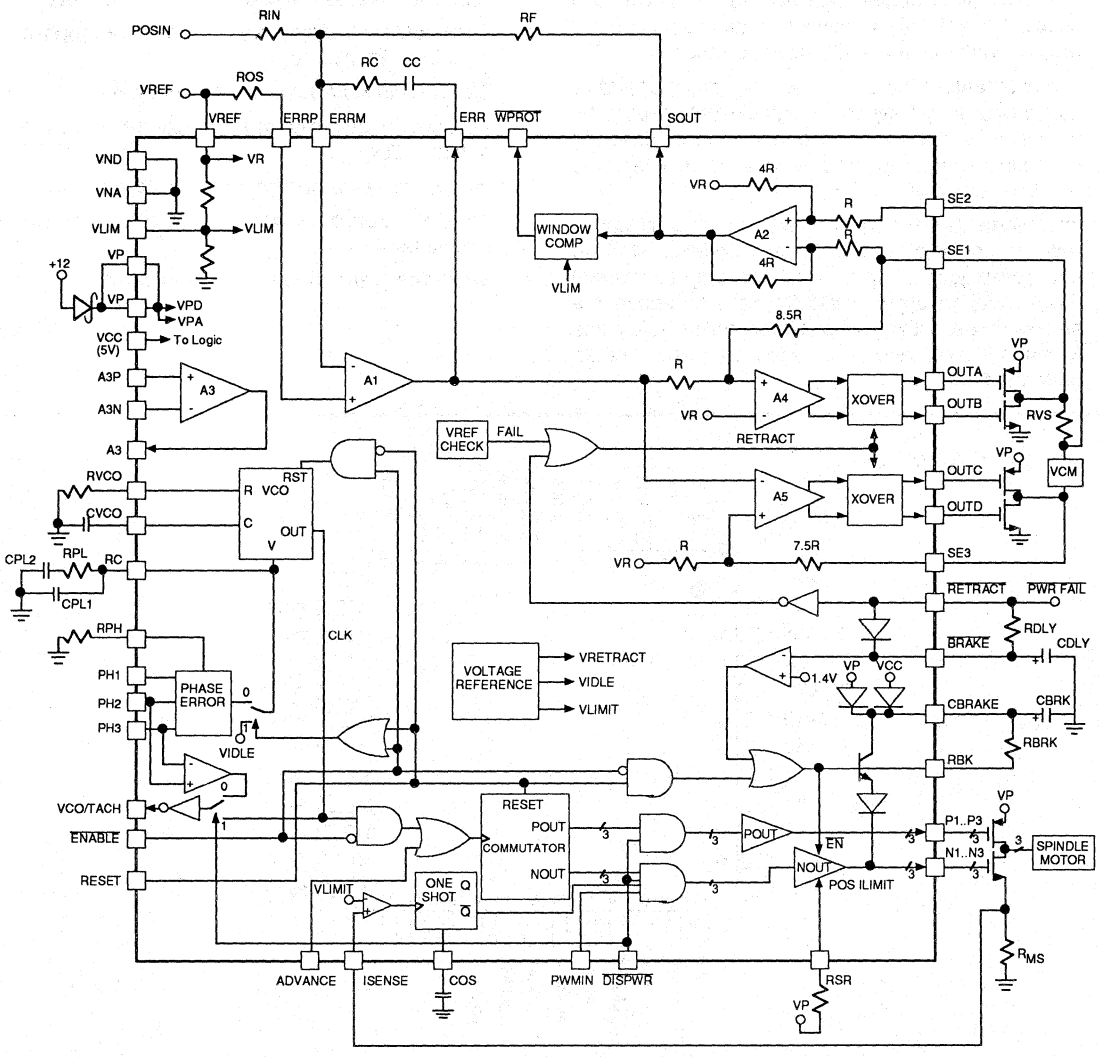


48-Lead TQFP

CAUTION: Use handling procedures necessary for a static sensitive component.

7

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

ACTUATOR

The actuator section consists of A1 through A5, the window comparator, the VREF check, and the XOVER blocks. It is functionally identical to the SSI 32H6231. During linear operation, an acceleration signal from the servo controller is applied through amplifier A1, whose three connections are all available externally. RC components may be used to provide loop compensation at this stage. The ERR signal drives two precision amplifiers, each with a gain of 8.5. The first of these amplifiers is inverting, and is formed from opamp A4, an on-chip resistor divider and an off-chip complementary MOSFET pair. The second is non-inverting, and is formed in a similar manner from opamp A5. Feedback from the MOSFET drains, on sense inputs SE1 and SE3, allows the amplifiers gains to be established precisely. The voice coil motor and a series current sense resistor are connected between SE1 and SE3.

Crossover protection circuitry between the outputs of A4 and A5, and the external MOSFETs, ensures class B operation by allowing only one MOSFET in each leg of the H-bridge to be in conduction. The crossover separation threshold, illustrated in Figure 1, is the maximum drive on any MOSFET gate when the motor voltage changes sign. The crossover circuitry can also apply a constant voltage across the motor (to retract the heads at a constant velocity).

Motor current is sensed by a small resistor placed in series with the motor. The voltage drop across this resistor is amplified by a differential amplifier with a gain of 4 (A2 and associated resistors), whose inputs are SE1 and SE2. The resulting voltage, SOUT, is proportional to motor current, and hence acceleration. This signal is externally fed back to A1, so that the signal ERR represents the difference between the desired acceleration (from the servo controller) and the actual motor acceleration.

SOUT is connected to a window comparator, which is used to detect excessive motor current. When excessive current is detected, WRPROT is pulled low. The VLIM pin may be used to program the voltage limit for the window comparator. The maximum voltage excursion allowed about VREF is (VREF-VLIM). An on-chip resistor divider sets a default value for VLIM and if VLIM is connected to ground, the windowing is effectively disabled.

The SSI 32H6825 has low voltage monitor circuitry that will detect a loss of voltage on VREF. The power supply pin, VP, should be connected to the disk drive's spindle motor so that its stored rotational energy may be used to hold up VP briefly during a power failure. When a low voltage condition is detected, the MOSFET drivers switch from linear operation to retract mode. In this mode a constant voltage is applied across the motor which will cause the heads to move at a constant speed. A mechanical stop must be provided for the heads when they reach a safe location.

The spindle driver monitors spindle back EMF and generates drive signals to 3 MOSFET power bridges. This section includes current limit, a back EMF monitoring circuit to determine commutation points, a phase locked loop to remove jitter from the commutation times, and a delayed spindle brake circuit.

COMMUTATOR

The commutator drives the spindle motor windings in the proper sequence to operate the 3 phase spindle motor. In Run mode, the commutator is clocked by CLK, the VCO output. In Start mode, the commutator is clocked by external pulses applied to the ADVANCE pin. Table 1 shows the commutator sequence and identifies which power FETS are on.

The commutator phase detector technology is licensed from Synektron, patent no. 4,928,043.

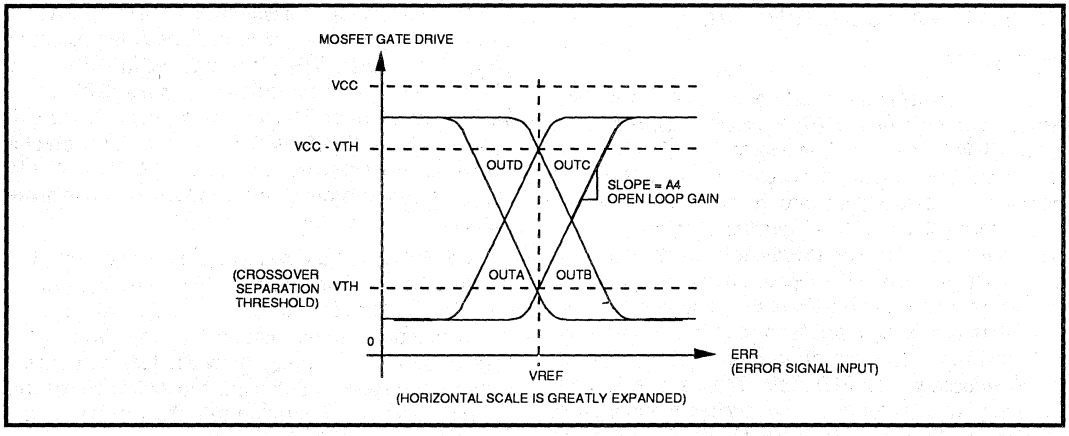


FIGURE 1: Crossover Protection

Table 1: Commutator Sequence

STATE	N1	N2	N3	P1	P2	P3
RST	OFF	ON	OFF	ON	OFF	ON
A	OFF	OFF	ON	ON	OFF	OFF
B	OFF	OFF	ON	OFF	ON	OFF
C	ON	OFF	OFF	OFF	ON	OFF
D	ON	OFF	OFF	OFF	OFF	ON
E	OFF	ON	OFF	OFF	OFF	ON
F	OFF	ON	OFF	ON	OFF	OFF

PHASE ERROR AMPLIFIER

The PHASE ERROR circuit compares the undriven winding with the average of the other two voltages. Depending on the result of the comparison and the state of the commutator, a positive or negative current is put out on the RC pin. Table 2 shows which winding is undriven and which polarity of current is output when that winding is positive with respect to the average of the other two.

Table 2: Undriven Winding and Polarity

Commutator State	Undriven Winding	Polarity
A	PH2	Source
B	PH1	Sink
C	PH3	Source
D	PH2	Sink
E	PH1	Source
F	PH3	Sink

FUNCTIONAL DESCRIPTION (continued)

PHASE ERROR AMPLIFIER (continued)

The PHASE ERROR circuit is only used when mode = RUN. In all other modes, RC is forced to V_{IDLE}, an internally generated voltage that will cause the VCO to idle at approximately 1/20 of the run rate.

The magnitude of the current at RC is the sum of a constant current and a current proportional to the VCO frequency. The constant current value is set by RPH which is biased to 1.2V nominally. The proportional current is set by RVCO, the same resistor that controls the VCO current. The RVCO pin is nominally the same voltage as the RC pin.

VCO

The VCO is a triangle wave oscillator with a wide frequency range set by RVCO and CVCO. The voltage swing on CVCO is nominally 2.2V. The frequency formula is:

$$F_{VCO} = \frac{V_{RC}}{8.8\ R_{VCO}\ C_{VCO}}$$

The VCO is reset if $\overline{ENABLE}$ = 1 and RESET = 0. During VCO reset, the CLK output is forced low. The first VCO clock will occur immediately on exiting reset. This timing relationship is shown in Figure 1.

ONE SHOT

The one shot is triggered whenever ISENSE exceeds VLIMIT (nominally 0.1V). When the one shot times out, it will remain high if ISENSE is still above VLIMIT. During the time the one shot output is high, the N drivers are turned off. This behavior implements PWM over-current limit, where the peak current is VLIMIT/ R_{MS}.

VOLTAGE REFERENCE

The voltage reference circuit generates voltage and current references for the rest of the MSC section. Specifically, these voltages are 3.3V, VRETRACT, and VLIMIT. The circuit also generates the bias voltage: 1.2V + V_{be}(40 µA).

NOUT AND POUT

The NOUT drivers drive the gates of the N channel power FETs. They have an adjustable source current set by R_{SR}. During BRAKE, the NOUT drivers are disabled and all N channel power FETs are turned on. The POUT drivers drive the P channel power FETs. The POUT drivers are not deactivated during PWM.

DIGITAL INPUTS

All digital inputs are pulled to ground with a 20 kΩ (nominal) resistor to ensure a known state during system power failure.

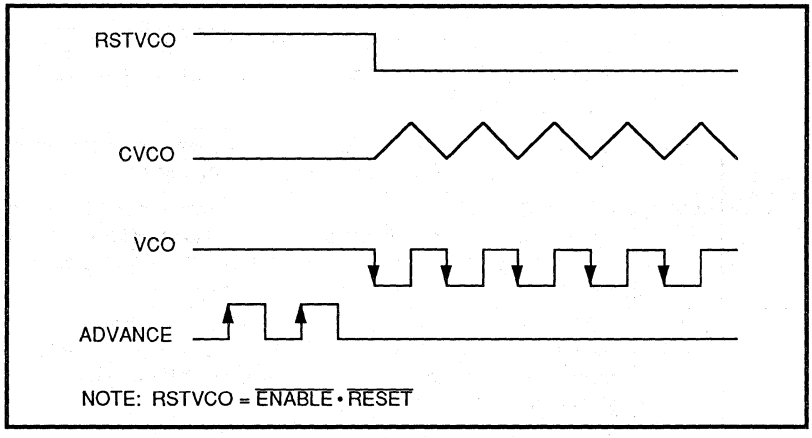


FIGURE 2: VCO Timing Diagram

PIN DESCRIPTION

SUPPLIES

NAME	TYPE	DESCRIPTION
GNDD GNDA	GROUND	Digital and Analog Grounds.
VCC	POWER	System 5V power supply.
VP	POWER	The 12V supply, diode protected from system 12V. Bridge supply for the spindle and actuator FETs.

ACTUATOR

VREF	AN INPUT	REFERENCE VOLTAGE. All actuator analog signals are referenced to this voltage.
VLIM	AN INPUT	LIMITING VOLTAGE. The voltage at this pin sets the $\overline{\text{WRPROT}}$ window comparator limits. Limiting occurs when: |SOUT-VREF| > VREF-VLIM An internal resistor divider establishes a default value that may be externally adjusted.
ERR	AN OUTPUT	POSITION ERROR. The loop compensation amplifier output. This signal is amplified by the MOSFET drivers and applied to the motor by an external MOSFET H-bridge as follows: SE3-SE1 = 17(ERR-VREF)
ERRM	AN INPUT	POSITION ERROR INVERTING INPUT. Inverting input to the loop compensation amplifier.
ERRP	AN INPUT	POSITION ERROR NON-INVERTING INPUT. Non-inverting input to the loop compensation amplifier.
SOUT	AN OUTPUT	MOTOR CURRENT SENSE OUTPUT. This output provides a voltage proportional to the voltage drop across the external current sense resistor, as follows: SOUT-VREF = 4(SE2-SE1)
$\overline{\text{WRPROT}}$	AN OUTPUT	WRITE PROTECT. Active low, an open collector output which is asserted when SOUT exceeds the window comparator limits.
SE2	AN INPUT	MOTOR CURRENT SENSE INPUT. Non-inverting input to the current sense differential amplifier. It should be connected to one side of an external current sensing resistor in series with the actuator. The inverting input of the differential amplifier is connected internally to SE1.
SE1	AN INPUT	MOTOR VOLTAGE SENSE INPUT. This input provides feedback to the inverting MOSFET driver amplifier and to the current sense amplifier. It is connected to the current sensing resistor which is in series with the motor. The gain to this point from ERR is: SE1-VREF = -8.5(ERR-VREF)

PIN DESCRIPTION (continued)

ACTUATOR (continued)

NAME	TYPE	DESCRIPTION
SE3	AN INPUT	MOTOR VOLTAGE SENSE INPUT. This input provides feedback to the non inverting MOSFET driver amplifier. It is connected to one side of the motor. The gain to this point from ERR is: SE3-VREF = 8.5(ERR-VREF)
OUTA, OUTC	AN OUTPUT	P-FET DRIVE. Drive signal for a P channel MOSFET connected between one side of the motor and VP.
OUTB, OUTD	AN OUTPUT	N-FET DRIVE. Drive signal for an N channel MOSFET connected between one side of the motor and GND. Crossover protection circuitry ensures that the P and N channel devices connected to the same side of the motor are never enabled simultaneously.
A3P	AN INPUT	NON-INVERTING A3 INPUT. Positive input to A3, the uncommitted opamp.
A3N	AN INPUT	INVERTING A3 INPUT. Negative input to A3, the uncommitted opamp.
A3	AN OUTPUT	A3 OUTPUT. The output of A3, the uncommitted opamp.

SPINDLE

P1, P2, P3	AN OUTPUT	P CHANNEL SPINDLE FET DRIVERS. These pins are connected to the three P channel power MOSFETs in the spindle motor power bridge.
N1, N2, N3	AN OUTPUT	N CHANNEL SPINDLE FET DRIVERS. These pins are connected to the three N channel power MOSFETs in the spindle motor power bridge.
RSR	COMPONENT	SOURCE CURRENT LIMIT. The peak source current at N1..N3 is set at 20x the current through RSR.
PWMIN	DIG INPUT	PULSE WIDTH MODULATION INPUT. Modulates the N channel power MOSFETs to control spindle motor current.
COS	COMPONENT	ONE SHOT CAPACITOR. Sets the time delay in the one shot. The one shot is clocked whenever the current in the spindle exceeds a limit controlled by R_{MS}.
ISENSE	AN INPUT	SPINDLE CURRENT SENSE. Connects to the spindle current sense resistor, R_{MS}, and is used during startup as part of the current limit circuitry.
VCO/TACH	DIG OUTPUT	SPEED CONTROL OUTPUT. Under normal operation ($\overline{DISPWR}$ = 1), this pin provides the speed sensitive signal used by the µP to control spindle speed. When $\overline{DISPWR}$ = 0, the pin provides the output of the TACH comparator.
RVCO	COMPONENT	VCO RESISTOR. Sets the speed range of the VCO. The voltage at RVCO is forced to track RC.

SPINDLE (continued)

NAME	TYPE	DESCRIPTION
CVCO	COMPONENT	VCO CAPACITOR. Sets the speed range of the VCO.
RC	COMPONENT	PLL LOOP FILTER. Sets the time constant for the PLL in Run mode. In all other modes, it is connected to a DC voltage, V_{IDLE}. V_{IDLE} determines the VCO frequency at which crossover from startup to run should occur (by lowering $\overline{ENABLE}$).
RPH	COMPONENT	PHASE ERROR CURRENT SET. The pump current in the phase error amplifier is the sum of the VCO current (through RVCO) and the current through RPH.
PH1, PH2, PH3	AN INPUT	SPINDLE MOTOR TERMINALS. These pins are used to calculate the phase error in the PLL.

CONTROL

$\overline{RETRACT}$	DIG INPUT	POWER FAIL. Active low, this digital input should be asserted by external power fault detection circuitry. When low, this pin forces an actuator retract.
$\overline{BRAKE}$	AN INPUT	BRAKE. Active low, this input is pulled low by external circuitry to perform a delayed brake.
CBRAKE	COMPONENT	BRAKE CAPACITOR. A large capacitor is connected to CBRAKE to provide pullup to the N channel spindle MOSFETs during brake.
RBK	O/C OUTPUT	BRAKE RESISTOR. A high value (10 Meg) resistor is connected between CBRAKE and RBK to pull up the base of the brake transistor. This pin is pulled low while BRAKE is not asserted.
$\overline{DISPWR}$	DIG INPUT	DISABLE POWER. Active low, this input turns off the high and low sides of the spindle drivers. A brake command will over-ride $\overline{DISPWR}$. An internal pull down resistor guarantees a logic 0 when $\overline{DISPWR}$ floats.
$\overline{ENABLE}$ RESET	DIG INPUT	MODE CONTROLS. These inputs control the spindle modes according to the following truth table:

$\overline{ENABLE}$	RESET	MODE	RC	VCO	Commutator
0	0	Run	Run	Run	Run
0	1	Brake	V_{IDLE}	Idle	Rst
1	0	Start	V_{IDLE}	Rst	Run
1	1	Preset	V_{IDLE}	Idle	Rst

Note:
Spindle braking is activated in Brake mode. Brake mode, whether activated by $\overline{ENABLE}$ and RESET or by a power failure is internally latched and can only be turned off by asserting Preset mode.

ADVANCE	DIG INPUT	COMMUTATION ADVANCE. A rising edge on this pin will cause the commutator to advance whenever RESET is low. While high, ADVANCE prevents other commutation clocks from occurring.

ELECTRICAL SPECIFICATIONS

Recommended conditions apply unless otherwise specified.

ABSOLUTE MAXIMUM RATINGS

Operation outside these rating limits may cause permanent damage to this device.

PARAMETER	RATING
VP	0 to 14V
VCC	0 to 7V
VREF	0 to 10V
SE1, SE2, SE3, N1, N2, N3, $\overline{\text{BRAKE}}$, CBRAKE, RBK, OUTD	0 to 15V
PH1, PH2, PH3	-2 to 15V
VCOTACH, $\overline{\text{DISPWR}}$, PWMIN, ADVANCE,RESET, $\overline{\text{ENABLE}}$, $\overline{\text{RETRACT}}$	0 to VCC
All other pins	0 to VP
Storage Temperature	-45 to 165°C
Solder temperature - 10 sec duration	260°C

RECOMMENDED OPERATING CONDITIONS

Unless otherwise noted, the following conditions are valid throughout this document.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
VP	Normal Mode	9	12	13.2	V
	Retract Mode	3.5		14.0	V
VREF		4.5		7	V
Operating Temperature		0		70	°C

DC CHARACTERISTICS

VP Current			20	35	mA
VCC Current			~5	10	mA
VREF Current	SE2 = VREF			2	mA

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A1, LOOP COMPENSATION AMPLIFIER

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Input bias current				500	nA
Input offset voltage				3	mV
Voltage swing	About VREF = 5.4	±2			V
Common mode range V_{IL}				1	V
V_{IH}, wrt VP		-1.3			V
Load resistance	to VREF	4			kΩ
Load capacitance				100	pF
Gain		80			dB
Unity gain bandwidth		0.5			MHz
CMRR		60			dB
PSRR		60			dB

A2, CURRENT SENSE AMPLIFIER

Input Impedance - SE1	SE2 = VREF	1.8	3.3		kΩ
Input Impedance - SE2	SE1 = VREF	4.8	9.6		kΩ
Input offset voltage	SE1 = SE2 = VREF			2.0	mV
Output voltage swing V_{OL}				1.4	V
V_{OH}, wrt VP		-1.3			V
Common mode range V_{IL}				0	V
V_{IH}, wrt VP	VP ≥ 10.0V, VREF = 5.0	-0.2			V
Load Resistance	to VREF	20			kΩ
Load capacitance				100	pF
Output impedance				20	Ω
Gain (SOUT-VREF)/SE1-SE2)		3.9	4.0	4.1	V/V
Unity gain bandwidth		0.5			MHz
CMRR		52			dB
PSRR		60			dB

ELECTRICAL SPECIFICATIONS (continued)

A3 AMPLIFIER

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Input bias current				250	nA
Input offset voltage				2	mV
Voltage swing V_{OL}				1.4	V
V_{OH}, wrt VP		-1.2			V
Common mode range V_{IL}				2.5	V
V_{IH}, wrt VP		-3			V
Load resistance	to VREF	10			kΩ
Load capacitance				100	pF
Gain		60			dB
Unity gain bandwidth		150			kHz
CMRR		60			dB
PSRR		60			dB

WINDOW COMPARATOR

Window comparator threshold	|SOUT-VREF| increasing	VREF-VLIM			V
Threshold hysteresis			50		mV
VLIM voltage	No external parts	92	94	96	%VREF
VLIM input resistance		8	15		kΩ
$\overline{\text{WRPROT}}$ Vol	Iol < 1 mA			0.4	V
$\overline{\text{WRPROT}}$ input leakage				10	µA
$\overline{\text{WRPROT}}$ delay	SOUT = VREF to VREF + 0.6V			10	µs

VREF MONITOR

VREF fail threshold	VREF Descending	2.6	3.3	4.0	V
Hysteresis			85		mV

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ACTUATOR MOSFET DRIVERS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
SE3 Input impedance	to VREF	10	25		kΩ
OUTA, OUTC voltage swing	|IOUT| < 1 mA	0.7		VCC-1	V
OUTB, OUTD voltage swing	|IOUT| < 1 mA	1		VCC-1	V
VTH, crossover separation threshold				2	V
Slew rate, OUTA..D	CL < 1000 pF	0.5			V/µs
Crossover time	300 mV step at ERR			6	µs
Output impedance, OUTA..D			50		kΩ
Transconductance I(OUTA..D)/(ERR-VREF)			8		mA/V
Gain -(SE1-VREF)/(ERR-VREF) or (SE3-VREF)/(ERR-VREF)		8	8.5	9	V/V
Retract motor voltage	VP > 5V	0.7	0.82	1.0	V

VCO (unless otherwise specified, CVCO = 0.01 µF, RVCO = 12 kΩ)

Typical frequency		$\frac{V_{RC}}{8.8\ R_{VCO}\ C_{VCO}}$			Hz
Run Frequency	RC = 2.0V	1705	1894	2083	Hz
Idle Frequency	Mode = Preset	85	100	115	Hz
Reset Phase Error	RC = V_{IDLE}			36	Degree

PHASE ERROR AMPLIFIER (unless otherwise specified, RVCO=12 kΩ, RPH=not used)

VRC (VIDLE)	Mode = Preset		100		mV
Pump Current at RC					
Start Mode	$V_{RC} = V_{IDLE}$, RPH = ∞		4		µA
Run Mode, at speed	V_{RC} = 2V		80		µA
Source/Sink Current Mismatch	V_{RC} = 2V			5	%
PH1 Input Offset, State B	PH2 = VP, PH3 = 0	-60		60	mV
PH1 Input Offset, State E	PH2 = 0, PH3 = VP	-60		60	mV
PH2 Input Offset, State A	PH1 = VP, PH3 = 0	-60		60	mV
PH2 Input Offset, State D	PH1 = 0, PH3 = VP	-60		60	mV
PH3 Input Offset, State F	PH1 = VP, PH2 = 0	-60		60	mV
PH3 Input Offset, State C	PH1 = 0, PH2 = VP	-60		60	mV
RPH Voltage	RPH = 120 kΩ		1.2		V

ELECTRICAL SPECIFICATIONS (continued)

MOTOR CURRENT CONTROL

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
ISENSE threshold (VLIMIT)		90	100	110	mV
One shot off time	COS = 0.002 µF	15	25	35	µs

BRAKING CIRCUIT

$\overline{\text{BRAKE}}$ threshold	T_A = 25°C	0.8	1.2	1.6	V
$\overline{\text{BRAKE}}$ bias current				0.1	µA

NMOS MOTOR DRIVER OUTPUTS (N1, N2, N3)

Source Current	RSC = 50k, VOUT = 4V	3		6	mA
	RSC = 100k, VOUT = 4V	2		4	mA
Sink Current	VOUT = 4V	9		25	mA
Output Low Voltage	Isink = 5 mA			1	V
Output High Voltage (wrt VP)	Isource = 0.1 mA			-2.5	V

PMOS MOTOR DRIVER OUTPUTS (P1, P2, P3)

Source Current	VOUT = VP-4	20			mA
Sink Current	VOUT = VP-4	9		25	mA
Output Low Voltage	Isink = 1 mA			1.5	V
Output High Voltage (wrt VP)	$Isource_P$ = $Isource_N$ = 5 mA			-1	V

DIGITAL INPUTS;

V_{IL}		0.8			V
V_{IH}				2.0	V
I_{IH} (excluding $\overline{\text{RETRACT}}$)	V_{IN} = 4V			200	µA
Open circuit voltage (excluding $\overline{\text{RETRACT}}$)				0.4	V
I_{IH} ($\overline{\text{RETRACT}}$)	V_{IN} = 4V			20	µA

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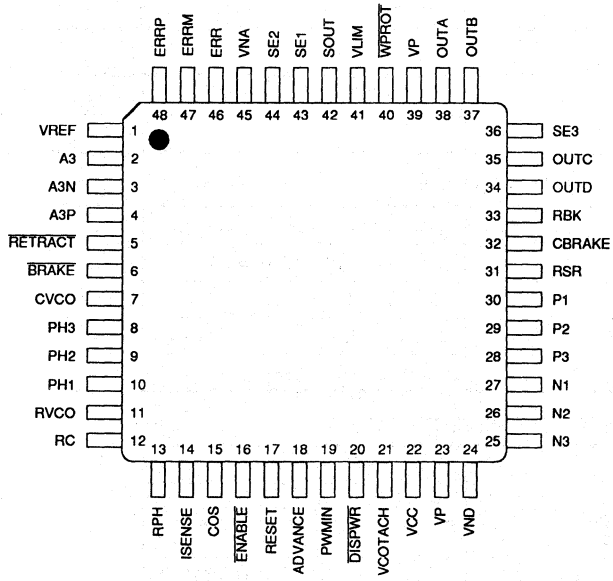
SSI 32H6825
Servo and Spindle Predriver

PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



48-Lead TQFP

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914

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SSI 32H6830
Servo DSP

Advance Information

December 1993

DESCRIPTION

The SSI 32H6830, designated as the SEEKER™, contains a DSP, a 10-bit ADC, two 10-bit DACs, and sufficient I/O pins to perform the servo and MSC functions of a hard disk drive with no overhead to the master microprocessor. When fully programmed, the SEEKER™ performs self-contained seek, track, and spindle control functions. When the device is given a track destination, it will seek to the desired track, generate an interrupt when it arrives on track, and then servo on the track. As a spindle controller, the SEEKER™ will start the motor, spin it up to a speed indicated by the microprocessor, and generate an interrupt when proper speed has been achieved. The spindle controller is also capable of phase locking to a master spindle index and maintaining a specified phase with respect to the master index. The DSP will allow more sophisticated algorithms with better phase margin than those implemented with a microprocessor. The program and constants for the DSP are stored in the microprocessor ROM and are uploaded to the DSP. The part is optimized for use with the SSI 32H6810A motor speed commutator and servo amplifier device.

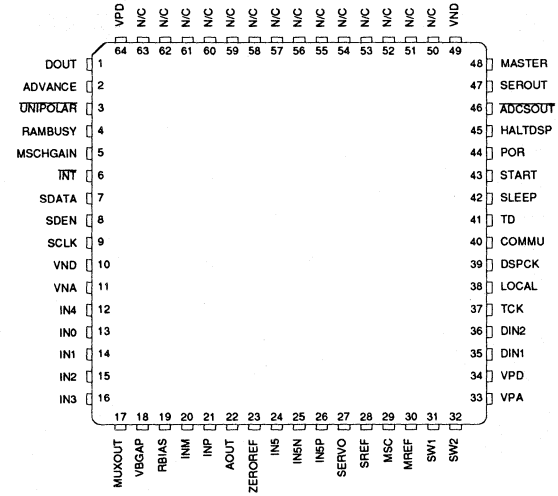
The SEEKER™ offloads all sector rate processing from the microprocessor and allows it to spend nearly 100% of its time dealing with the controller chip; an essential feature as data rates approach 48 Mbit/s. It also allows better algorithms to be implemented with less phase delay. This results in faster, quieter seek times and higher track bandwidths.

FEATURES

- **Self contained seek, track, spindle start, spindle run, and spindle sync capability**
- **Can operate at a multiple of the sector rate to reduce latency time between seek command and start of seek**
- **DSP with 16 x 16 multiply in 200 ns**
- **10-bit 2 µs ADC with 6 input MUX**
- **Two 10 bit DACs**
- **Serial µP port for uploading program memory from system µP**
- **Interfaces with pulse detectors containing on board peak detectors such as SSI 32P548 and SSI 32P4730**

7

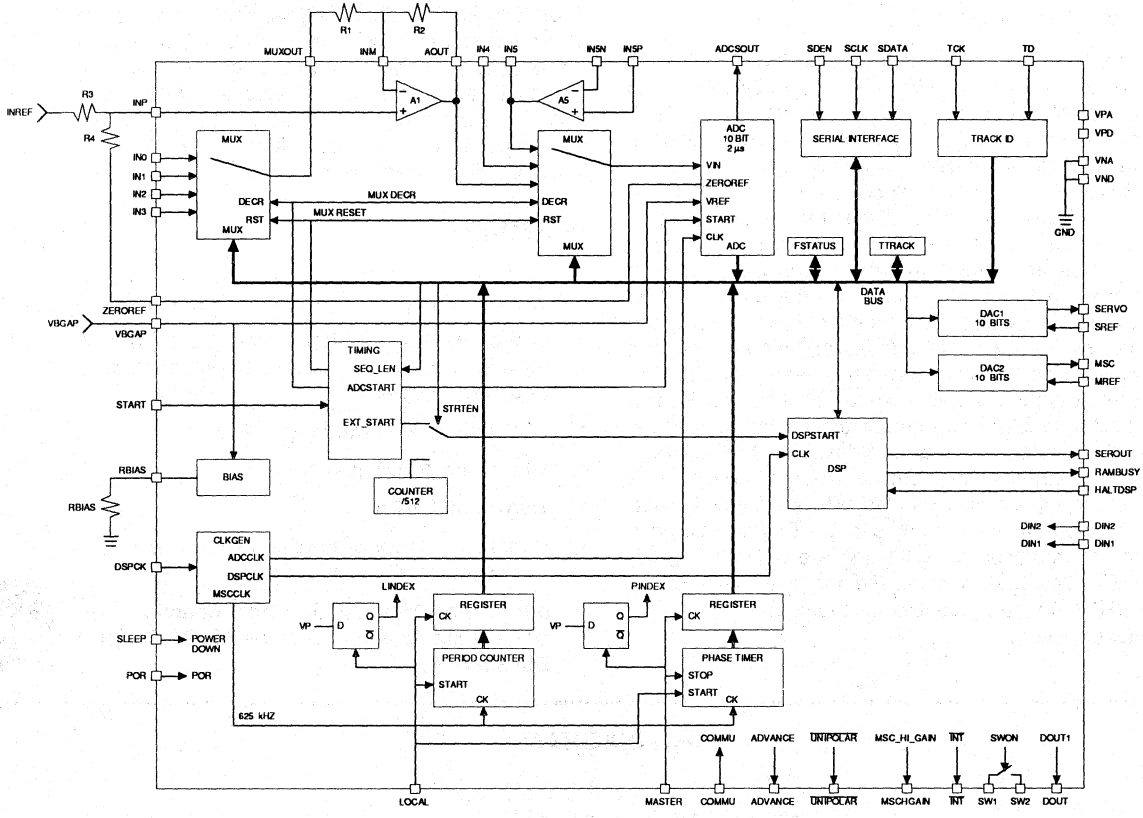
PIN DIAGRAM



64-Lead TQFP

CAUTION: Use handling procedures necessary for a static sensitive component.

BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

HARDWARE FUNCTIONAL BLOCKS

Front End

The SEEKER™ front end consists of a 10-bit two's complement ADC, a 6-input MUX and some amplifiers whose gain can be set with external components. The front end is intended to be driven by pulse detectors like the SSI 32P548 that have internal peak detectors or integrators. External resistors perform gain and offset correction.

Front End Timing

A start pulse sets the MUX address to five, raises RAMBUSY, and initiates a sequence of consecutive ADC conversions. The result of each conversion is stored in the data RAM (DRAM) address 0 through 5, respectively. The MUX inputs are converted in reverse numerical order for IN0 through IN3. When the conversions are complete, other status words such as the state of the period and phase timers, the target track, and the current track are inserted in the DSP DRAM and a DSP code pass is started.

The start pulse can be generated by hardware (the START pin or an internal counter) or software (STARTBIT in FSTATUS.) If STRTEN (in FSTATUS) is high, the start signal is taken from the START pin. If it is low, the internal counter generates a start signal every 512 DSP clocks. STARTBIT generates a start regardless of any other pin or bit.

DSP Timing

When the DSP is started, the ADC values, DSPIN, TTRACK, PHTIME, PTIME, and TRACK have already been loaded in DRAM. These values will not be updated again until the next start pulse occurs. When the DSP reaches a STOP instruction, it halts, lowers RAMBUSY and waits for another start signal.

Track ID

The current track ID is demodulated and converted to binary by external circuitry. It is then supplied to the SEEKER™ through a dedicated serial port. The track ID is transferred to DRAM address 10 when a DSP start pulse is received. Depending on the TRKMSB bit in the FSTATUS word, track ID is received either LSB or MSB first. Since the track ID register can handle up to 16 bits, the unused bits can be utilized as flag bits from the demodulator. Some possible uses for the flag bits are: warning the DSP that certain sector data as bad, and in oversampling applications, indicating to the DSP which start pulses are at the beginning of a sector.

Spindle Control Hardware

The MSC portion of the seeker will support start, run, and synchronized spindle modes. The MSC hardware consists of a period timer and a phase timer. The period counter starts on the rising edge of LOCAL and transfers its count to a latch when the next rising edge occurs. A status bit, LINDEX, is set whenever new data is available at the latch. The status bit will be high for one DSP code pass. The phase timer is also started on every LOCAL rising edge. It is stopped when MASTER rises. A status bit, MINDEX, indicates when new data from the phase timer is available. By comparing the value of the period timer and the phase timer, the actual phase error between local and master can be determined. The DSP controls spindle start by monitoring COMMU and asserting ADVANCE. See the SSI 32H6810 or equivalent data sheet for more details.

µP Serial Port

Through the serial port, the µP can read FSTATUS and any DRAM or IRAM memory word. It can write the FSTATUS and TTRACK registers as well as any DRAM or IRAM word. The registers are internally double buffered and can be accessed by the µP at any time. Access to RAM must be limited to when the DSP is idle. The format of the serial port data string is consistent with other Silicon Systems serial interfaces.

DAC1 and DAC2

These DACs are 10 bits wide. They are memory mapped to DRAM address 2 and 3 for DAC 1 and 2, respectively. Each DAC has its own zero-reference input. The full scale swing of each DAC is ±VBGAP/2. These DACs are intended to drive the servo and spindle buffers.

TTRACK Memory

This 16 bit word is accessed by the µP serial port. It is double buffered so the µP does not need to synchronize to RAMBUSY. When TTRACK is programmed to a new target track, the next DSPSTART pulse will transfer it to DRAM and cause a seek to begin.

FUNCTIONAL DESCRIPTION (continued)

FSTATUS Memory

This 16-bit word can be read and written by the µP. It is double buffered so the µP does not need to synchronize to RAMBUSY.

Interrupt

The $\overline{INT}$ output is controlled by the DSP. It is typically used to indicate an event of interest to the µP such as spindle control achieving lock, or the head arriving at its target, or at other times, spindle control losing lock or the head falling off track. Upon receiving the interrupt, the µP should read FSTATUS to determine the interrupt type. Reading FSTATUS clears the $\overline{INT}$ output.

SEROUT

This is an output serial port used for diagnostic purposes. Whenever the DSP writes to this port, the bits are shifted out at the DSP clock rate. SEROUT normally sits high. A leading zero prefixes all outputs as a marker. This pin is useful for monitoring internal data words while the DSP is operating in real time.

Software Interface to µP

The µP is able to read or write any word in the IRAM or DRAM. In addition, it is able to read and write the FSTATUS register, and to write the TTRACK register.

FSTATUS Register—Read

The first 4 bits are interrupt status bits. They are written by the DSP and cause an interrupt to be initiated whenever they change state. The second four bits are information bits and do not affect $\overline{INT}$. The third group of 4 bits are interrupt flags, indicating which of the interrupt status bits caused an interrupt. The last 4 bits are for version control and future reserved functions. Note that whenever FSTATUS is read, $\overline{INT}$ is deasserted and the interrupt flags are cleared.

Bit	Name	Description
0	Spare_INT	When this bit changes state, $\overline{INT}$ is asserted.
1	Ontrack	Indicates that the head is on track. When this bit changes state, $\overline{INT}$ is asserted.
2	At_speed	Indicates that the spindle is at speed. When this bit changes state, $\overline{INT}$ is asserted.
3	Phase_lock	Indicates that the local index is phase locked to the master index. When this bit changes state, $\overline{INT}$ is asserted.
4	Track/Seek	Indicates if the DSP is in track mode.
5	RAMBUSY	Indicates the DSP RAM is servicing the DSP and is "locked out" of the µP serial interface.
6	DSTAT11	Bit 11 of DSPSTATUS
7	DSTAT12	Bit 12 of DSPSTATUS
8	INTF0	Is set when bit 0 changes state. Is cleared when FSTATUS is read.
9	INTF1	Is set when bit 1 changes state. Is cleared when FSTATUS is read.
10	INTF2	Is set when bit 2 changes state. Is cleared when FSTATUS is read.
11	INTF3	Is set when bit 3 changes state. Is cleared when FSTATUS is read.

FSTATUS Register—Read (continued)

Bit	Name	Description
12	REV0	LSB of revision number.
13	REV1	MSB of revision number.
14	RESERVED	
15	RESERVED	

FSTATUS Register—Write

0	STRTEN	Selects DSPSTART from the timing block instead of the divide-by-512 counter.
1	TRKMSB	Sets the TRACK ID serial to parallel converter to "MSB first" mode.
2	HALTBIT	Serves the same purpose as the HALTDSP pin. When asserted, the DSP will continue executing its current code pass and then will remain idle, ignoring both external and internal hardware start pulses. This bit should be set by the µP during initialization of the SEEKER™.
3	STARTBIT	Is a third way of creating a "start." When HALTBIT is asserted, this is the only way to create a "start." If this bit is programmed to 1, the usual sequence of ADC conversions and data transfers to DRAM is initiated. The DSP code pass will not be initiated, however. Instead the DSP will wait for SS pulses. STARTBIT is automatically cleared after it is written.
4	SS	This bit is ignored except if HALTBIT is asserted. In that case, every "one" written to SS causes the DSP to advance one clock cycle. SS is automatically cleared after it is written.
5	RESETBIT	Resets the SEEKER™ to the state where the µP serial interface has complete access. This bit should be set by the µP before initializing the SEEKER™.
6	RESUMEBIT	Terminates the single step mode by resuming DSP execution at full speed.
7	FS7	A spare bit for communication from µP to DSP.

FUNCTIONAL DESCRIPTION (continued)

Serial Port

The serial port is designed to be shared by other devices. For this reason, a device ID is included in the preamble. The device ID conforms to the Silicon Systems standard: 1-R/W, 2-Pulse Det, 3-Filter, 4-Data Sep, 5-ENDEC, 6-Time Base, 7-Servo/MSC. Bit 0 of the serial port is received first. Each bit string received by the serial port can be unlimited in length but consists of the following initial fields:

Bit #	Field	Description
0	R/W	Indicates whether data is to be read or written.
1..3	Device ID	Identifies the device being programmed (LSB is bit 1). Must be '7' to communicate with this part.
4..5	Type	Indicates which memory is addressed (LSB is bit 4): 0 FSTATUS 1 TTRACK (write only) 2 DRAM or ACCUMULATOR 3 IRAM or PROGRAM COUNTER
6..7	Address bank	The bank address for memories with more than 256 words. These bits are ignored if FSTATUS or TTRACK is being accessed. Note that if bank is 11, type 2 and 3 become ACCUMULATOR and PROGRAM COUNTER respectively.
8.115	Address	The RAM address (LSB is bit 8). This field must always be sent except when accessing FSTATUS or TTRACK.
16.. or 8..	Data	The data (LSB first). If RAM data is being read or written, consecutive data words can be concatenated. The address will automatically increment after each 16 (DRAM) or 20 (IRAM) bits. The address bank is automatically incremented when necessary.

DSP Memory Map

The DSP communicates with the SEEKER™ chip through memory mapped regions of DRAM. The first 10 words are mapped to various hardware resources as defined below. Note that the first four words are "write protected." The remaining words are initialized at the beginning of each DSP code pass and may then be modified or overwritten by the DSP.

DRAM Address	Read by DSP	Written by DSP
0	ADC5 (write protected)	DSPSTATUS
1	ADC4 (write protected)	SEROUT
2	ADC3 (write protected)	DAC1
3	ADC2 (write protected)	DAC2
4	ADC1	
5	ADC0	
6	DSPIN	
7	TTRACK	
8	PTIME (period time)	
9	PHTIME (phase time)	
10	TRACK	

DSPSTATUS and DSPIN

DSPIN is the word the DSP uses to communicate with bits set by the µP or by SEEKER™ input pins. DSPSTATUS is the word the DSP uses to control bits read by the µP and external pins controlled by the DSP. Whenever the first 4 bits of DSPSTATUS are changed by the DSP, $\overline{INT}$ is asserted. The bits in DSPIN and DSPSTATUS are defined below.

BIT	DSPIN (Read by DSP)	DSPSTATUS (Written by DSP)
0	COMMU (from COMMU pin)	SPARE_INT (to FSTATUS)
1	LINDEX (from period timer)	ONTRACK (to FSTATUS)
2	MINDEX (from phase timer)	ATSPEED (to FSTATUS)
3	DIN1 (from DIN1 pin)	PHLOCK (to FSTATUS)
4	DIN2 (from DIN2 pin)	TRACK/SEEK (to FSTATUS)
5	LOCAL (from LOCAL pin)	$\overline{UNIPOLAR}$ (to pin)
6	MASTER (from MASTER pin)	MSCHGAIN (to pin)
7	FS7 (from FSTATUS)	ADVANCE (to pin)
8		DOUT (to pin)

FUNCTIONAL DESCRIPTION (continued)

DSPSTATUS and DSPIN (continued)

BIT	DSPIN (Read by DSP)	DSPSTATUS (Written by DSP)
9		SWON (to SW1, SW2 switch)
10		DSTAT11 (to FSTATUS)
11		DSTAT12 (to FSTATUS)
12		not used
13		not used
14		not used
15		not used

PIN DESCRIPTION

The following description lists each pin, associates a pin type to it, and provides a brief description of the pin's function.

NAME	TYPE	DESCRIPTION
VPA, VPD	VCC	Analog and digital power supplies.
VNA, VND	GND	Analog and digital grounds.
IN0, IN1, IN2, IN3	Ana In	The four primary inputs automatically converted by the A/D. These inputs drive a low resistance analog switch.
MUXOUT	Ana Out	The output of the IN0..IN3 mux.
INM	Ana In	The inverting input to amplifier A1.
AOUT	Ana Out	The output of amplifier A1.
INP	Ana In	The non-inverting input to A1.
VBGAP	Ana In	The voltage reference input. This will determine the full scale swing of the ADC and the two DACs.
ZEROREF	Ana Out	The ADC zero reference output. Can be used by the A1 resistor network to level shift IN0 through IN3.
IN4	Ana In	A direct input to the ADC mux.
IN5	Ana Out	The output of amplifier A5.
IN5N, IN5P	Ana In	The inputs to amplifier A5.
RBIAS	Ana Out	A resistor to ground from this pin sets the bias current for the analog circuitry.
SERVO	Ana Out	The output of the servo DAC.
SREF	Ana In	The servo DAC reference. The DAC output swing will be SREF-0.5•VBGAP to SREF+0.5•VBGAP.
MSC	Ana Out	The output of the MSC DAC.
MREF	Ana In	The MSC DAC reference. The DAC output swing will be MREF-0.5•VBGAP to MREF+0.5•VBGAP.

NAME	TYPE	DESCRIPTION
SW1, SW2	Ana In	The two terminals of an uncommitted analog switch. The switch is controlled by the SWON bit in the DSP STATUS word.
ADCSOUT	Dig Out	A test point from the ADC. This test point is connected to the output of the ADC comparator.
START	Dig In	A rising edge on START initiates consecutive ADC conversions and causes a pass through the DSP code to begin.
DSPCK	Dig In	The master clock (20 MHz) for the chip.
SLEEP	Dig In	Reduces the supply current of the chip. All analog circuitry is deactivated, with outputs becoming high impedence. The chip clock is deactivated. No data will be lost in RAM due to the use of static RAM.
POR	Dig In	Chip reset. This pin is for diagnostic purposes and should be grounded in normal operation.
SDEN	Dig In	The µP serial interface enable. SCLK and SDATA are ignored and the interface reset when SDEN is low.
SCLK	Dig In	The µP serial interface clock.
SDATA	Dig I/O	The µP serial interface data. This pin is an input except for the data cycles of a serial read request.
TCK	Dig In	The clock for the current track serial input.
TD	Dig In	The data for the current track serial input.
SEROUT	Dig Out	The serial output from the SEROUT word memory mapped into DRAM. This output can be used to monitor the DSP during real time applications.
RAMBUSY	Dig Out	When high, the DSP is executing code. When low, it is waiting for a START pulse.
HALTDSP	Dig In	When high, halts the DSP. Similar in function to HALTBIT in FSTATUS. This pin or HALTBIT should be asserted during µP access of DRAM and IRAM.
LOCAL	Dig In	The local index pulse. The period counter measures the time between LINDEX pulses.
MASTER	Dig In	The master index pulse. The phase timer measures the time from LINDEX to MINDEX.
COMMU	Dig In	The input from the BEMF comparator on the MSC chip.
ADVANCE	Dig Out	The output to the MSC chip.
$\overline{\text{UNIPOLAR}}$	Dig Out	An uncommitted DSP output bit that can be used to command the external MSC commutator to switch to unipolar mode.
MSCHGAIN	Dig Out	An uncommitted DSP output bit that can be used to command the external MSC commutator to switch gains.
$\overline{\text{INT}}$	Dig O/D	The interrupt output for the DSP.
DOUT	Dig Out	An uncommitted output bit that can be programmed by the DSP.
DIN1, DIN2	Dig In	Uncommitted input bit that can be read by the DSP.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Exposure to absolute maximum rating conditions for extended periods may cause permanent damage to the device or affect device reliability.

PARAMETER			RATING
Supply voltage VPA, VPD		Vdd	-0.3 to 7.0V
Pin voltage	Ana In	Vinai	-0.3 to VDD+0.3V
	Ana Out	Vinao	-0.3 to VDD+0.3V
	Dig In	Vindi	-0.3 to VDD+0.3V
	Dig Out	Vindo	-0.3 to VDD+0.3V
Storage temperature		Tstg	-65 to 150°C
Lead temperature (10 sec duration)		Tlead	0 to 300°C

RECOMMENDED OPERATING CONDITIONS

The recommended operating conditions for the device are indicated in the table below. Performance specifications do not apply when the device is operated outside the recommended conditions.

PARAMETER			RATING
Supply voltage		Vdd	4.5 to 5.5V
Ambient temperature		Ta	0 to 70°C
Capacitive load on digital outputs		Cl	50 pF
Analog output load			
	Cl		50 pF
	Rl		20 kΩ
System clock fc = 20 MHz			
	Freq. tolerance	fc	-0.01 to 0.01%
	Pulse width	Twh,Twl	20 to 30 ns
Biasing resistor, Rbias = 56.3 kΩ		Rbias	-5 to 5%
VBGAP tolerance, VBGAP = 2.25V		VBGAP	-5 to 5%

PERFORMANCE SPECIFICATIONS

SUPPLY CURRENT (FSTART = 5 kHz, DSP ACTIVE TIME = 25 µs)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
VPA	Idda				24	mA
VPD	Idd				13	mA
VPA, Sleep mode	Iddas				TBD	mA
VPD, Sleep mode	Idds				TBD	mA

DIGITAL I/O

Digital input					
Vil		0.8			V
Vih				2.0	V
Iil,Iih				1	µA
Digital Output (except $\overline{INT}$)					
Vol	Iol = 2.0 mA			0.4	V
Voh	Ioh = -100 µA	Vdd-.4			V
Digital Output ($\overline{INT}$)					
Vol	Iol = 4.0 mA			0.4	V

SERVO D/A CONVERTER

Positive Full-scale voltage Digital=0x1FF			SREF+ VBGAP/2		V
Negative Full-scale voltage Digital=0x200			SREF- VBGAP/2		V
Resolution			10		bits
Digital Delay				4	µs
LSB voltage			VBGAP/ 1024		V
Differential nonlinearity				1	LSB
Offset				TBD	mV

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ELECTRICAL SPECIFICATIONS (continued)

MSC D/A CONVERTER

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Positive Full-scale voltage Digital = 0x1FF			MREF+ VBGAP/2		V
Negative Full-scale voltage Digital = 0x200			MREF- VBGAP/2		V
Resolution			10		bits
Digital Delay				4	µs
LSB voltage				VBGAP/ 1024	V
Differential nonlinearity				1	LSB
Offset				TBD	mV

ADC CONVERTER

Positive full-scale input Digital Output = 0x1 FF			VBGAP		V
Negative full scale input Digital Output = 0x200			VBGAP/9		V
Resolution			10		bits
Conversion time (includes MUX delay)				2	µs
LSB voltage			VBGAP/ 1152		V
Differential nonlinearity				1	LSB

AMPLIFIERS

Gain		50			dB
Unit gain bandwidth		1			MHz
Input offset		-20		20	mV
Output swing		0.2		3.5	V
Input common mode Range		0		Vdd	V
Settling time to 0.1%full scale step, inverting unity gain				1.8	µs

MUX

On Resistance				100	Ω

SW1, SW2 SWITCH

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
On Resistance				100	Ω

µP SERIAL INTERFACE PORT TIMING

SCLK						
Period	TCLK		50			ns
Low Time	TCKL		15			ns
High Time	TCKH		25			ns
SDEN						
Setup Time	TSENS		20			ns
Hold Time	TSENH		60			ns
SDATA						
Setup Time	TDS		5			ns
Hold Time	TDH		2			ns
Read Delay	TPD	CL = 0 to 50 pF	4		60	ns
Disable Delay	TSENDL				25	ns

µP TRACK ID PORT TIMING

TCK						
Period	TCLK		20			ns
Low Time	TCKL		10			ns
High Time	TCKH		10			ns
TD						
Setup Time	TDS		3			ns
Hold Time	TDH		2			ns

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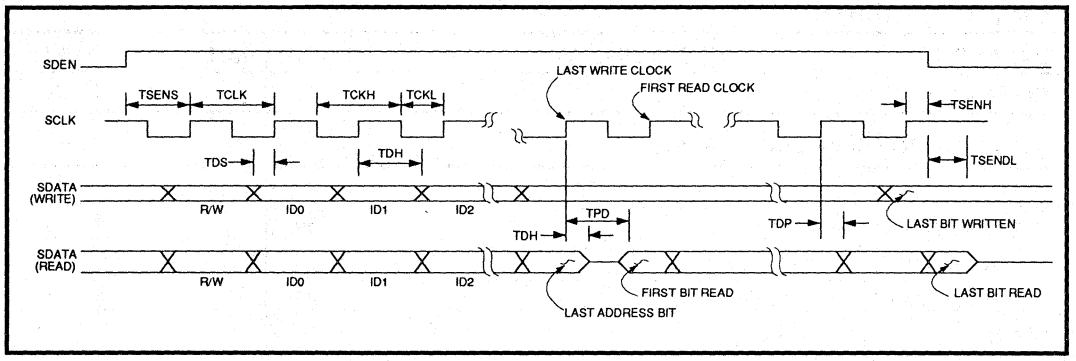


FIGURE 1: Serial Port Data Transfer Format

PROGRAMMER'S DESCRIPTION

This programmer's description of the SEEKER™ DSP contains a register level description of the DSP that is detailed enough to illustrate each opcode. It also contains a description of each opcode.

REGISTER LEVEL DESCRIPTION

The DSP consists of an arithmetic unit and an instruction unit. The arithmetic unit consists of a data RAM (DRAM), a shifter, an ALU, and an accumulator. The instruction unit consists of instruction RAM (IRAM) and a program counter. Figure 2 shows the contents of the DSP.

In a one-clock cycle, the DSP is capable of shifting a data word up to ±15 bits and adding it to the accumulator. A 4-cycle multiply is implemented in the multiply and accumulate functions.

DRAM

The DRAM stores data and coefficients for use by the DSP. The first 11 addresses of the DRAM are memory mapped to on-chip resources. In addition, a lookup command allows the DSP to use portions of DRAM as lookup tables.

DATA REG AND MULT REG

These registers store the data from the DRAM. This permits the DRAM to perform other operations during a multiply. A STORE or the setup cycle of an MLD or MADD instruction will be executed while a previous MLD or MADD instruction is completing.

SEQUENCER

This logic block controls the execution of instructions by monitoring the state of the accumulator, the DRAM, and the IRAM. When the resources required by the next instruction are available, the sequencer permits that instruction to execute.

FLAGS

Certain instructions cause one of the three flags to be updated with the sign bit of the accumulator. The flags are used by the instruction unit during conditional jumps.

SHIFTER

The shifter shifts the DATA REG word up to ±15 bits in one clock cycle. Unused left hand bits are sign extended and unused right hand bits are zero filled. The shifter has a 24-bit input and output width. The 16-bit word from DATA REG is sign extended 4 bits and padded with 4 zero bits below the LSB before entering the shifter.

ALU

The ALU is capable of performing an add, subtract, absolute value, XOR, AND, OR, and NEG function. The list of opcodes details the choices.

ACCUMULATOR

The accumulator is 16 bits with 4 extra LSB bits and 4 extra sign bits. The extra LSB bits minimize the rounding error when partial products are summed during a multiply. The top 4 sign bits are used as an aid in identifying overflow. They also are used in extended precision calculations where they are shifted to the least significant bits of the 16-bit accumulator.

MULTIPLIER DESCRIPTION

The multiplier returns the top 16 bits of a 16x16 product. An additional 4 LSBs are calculated to improve the truncation accuracy of the product. A RADIX register shifts the multiplicand (pointed to by DR) a certain number of bits to the left.

This multiplier facilitates the use of the two's complement fractional representation. For instance if RADIX is set to zero, each 16 bit number should be thought of as a signed fraction whose full scale value approaches ±1.0. The value of the fraction is calculated by the following equation:

$$\text{value} = -2^{0}b_{15} + 2^{-1}b_{14} + 2^{-2}b_{13} + \ldots + 2^{-15}b_{0}$$

Two such numbers multiplied together will yield an answer in the same format. For instance 0x4000 (0.5) multiplied by 0x4000 (0.5) results in 0x2000 (0.25).

Alternatively, if it is desired to represent numbers whose integer value can approach ±16, set RADIX to 4 and use the following formula:

$$\text{value} = -2^{4}b_{15} + 2^{3}b_{14} + 2^{2}b_{13} + \ldots + 2^{-11}b_{0}$$

With this format, 0x0400 (0.5) multiplied by 0x1800 (3.0) results in 0x0C00 (1.5).

OPCODE LIST

The following opcodes are implemented in the SEEKER™ DSP. Parameters in [square] brackets are optional. Parameters enclosed in {curly} brackets form a list from which only one parameter may be chosen. Parameters may be placed in any order within all instructions except MLD and MADD. Opcodes, symbols and all options are case insensitive.

SHORT/LONG FORM DESCRIPTION

There is instruction memory capacity for 1K by 10-bit short form commands or 500 bytes by 20-bit long form commands. Short form is a 10-bit command which uses relative addressing, whereas long form is a 20-bit command with direct addressing.

DR, MR, and SR are three different pointers to DRAM which are updated with each reference. The assembler will insert short forms of each command if the pointer reference is close enough to its previous reference that relative addressing can be used. Every instruction has a short form except AND, OR, XOR, store commands that use /RET, and jump instructions conditional on F2 or F3. The relative address distance is listed in each opcode description.

If it is desired to force a long or short version of a particular command, an .L or .S suffix can be appended to the command. Alternatively, a short instruction can be forced by specifying a relative address such as '+1' or '+2'.

ALU INSTRUCTIONS WITH MULTIPLY

MLD *DramDR DramMR* [/F1]

Loads the data register with *DramDR* and the multiplier register with *DramMR* and initiates a multiply and load. The value in *DramDR* is shifted left by RADIX before being multiplied. The MLD instruction requires either 4 or 5 cycles to execute. The 5th cycle is not needed if the previous ALU instruction was an MLD or MADD and was followed by fewer than 4 non-ALU instructions. If F1 is specified, the F1 flag will be updated with the sign bit of the accumulator result. Relative address distance for both DR and MR addresses is +2, -1.

MADD *DramDR DramMR* [/F1]

Loads the data register with *DramDR* and the multiplier register with *DramMR* and initiates a multiply and add. The value in *DramDR* is shifted left by RADIX before being multiplied. The MADD instruction requires either 4 or 5 cycles to execute. The 5th cycle is not needed if the previous ALU instruction was an MLD or MADD and was followed by fewer than 4 non-ALU instructions. If F1 is specified, the F1 flag will be updated with the sign bit of the accumulator result. Relative address distance for both DR and MR addresses is +2, -1.

MULTIPLIER CONTROL INSTRUCTIONS

RADIX n [/RET]

Sets the amount of left shift "bias" to be performed on DR during MLD and MADD instructions. This command is effectively defining the location of the radix point in the MR word. The RET option will cause a subroutine return. The RADIX command is always short form and is the only short form instruction with a RET option.

ALU INSTRUCTIONS WITH SHIFT

LDS *DramDR* {/SHL=n, /SHR=n} [/F1] [/ABS]

Loads the contents of *DramDR* in the accumulator after being shifted as specified. Relative address distance is +2, -1. F1 indicates that the F1 flag is to be updated with the sign of the result. ABS indicates that the absolute value of *DramDR* is to be used. If F1 or ABS is specified, the long form of the instruction is used.

LDNS *DramDR* {/SHL=n, /SHR=n} [/F1]

Loads the negative contents of *DramDR* in the accumulator after being shifted as specified. Relative address distance is +2, -1. F1 indicates that the F1 flag is to be updated with the sign of the result. If F1 is specified, the long form of the instruction is used.

ADDS *DramDR* {/SHL=n, /SHR=n} [/ABS] [/F1]

Adds the contents of *DramDR* to the accumulator after being shifted as specified. F1 indicates that the F1 flag is to be updated with the sign of the result. ABS indicates that the absolute value of *DramDR* is to be used. If F1 or ABS is specified, the long form of the instruction is used. Relative address distance is +2, -1.

SUBS *DramDR* {/SHL=n, /SHR=n} [/ABS] [/F1]

Subtracts the contents of *DramDR* to the accumulator after being shifted as specified. F1 indicates that the F1 flag is to be updated with the sign of the result. ABS indicates that the absolute value of *DramDR* is to be used. If F1 or ABS is specified, the long form of the instruction is used. Relative address distance is +2, -1.

XSIGN *DramDR* {/SHL=n, /SHR=n} [/F1]

Multiplies the accumulator by the sign of *DramDR*—if *DramDR* is negative, the accumulator will be inverted. If F1 is specified, the F1 flag is updated with the sign of the accumulator at the end of the command's execution. Relative address distance is +4, -3.

AND *DramDR* [/INV] {/SHL=n, /SHR=n}

ANDs the contents of *DramDR* to the accumulator after being inverted and shifted as specified. There is no short form of this instruction.

OR *DramDR* {/SHL=n, /SHR=n}

ORs the contents of *DramDR* to the accumulator after being shifted as specified. There is no short form of this instruction.

XOR *DramDR* {/SHL=n, /SHR=n}

XORs the contents of *DramDR* to the accumulator after being shifted as specified. There is no short form of this instruction.

ALU INSTRUCTIONS

LD *DramDR* [/ABS] [/F1]

Loads the contents of *DramDR* in the accumulator. If [ABS] is specified, the absolute value of *DramDR* is loaded. If F1 is specified, the F1 flag is updated with the sign of the accumulator at the end of the command's execution. Relative address distance is +4, -3.

LDN *DramDR* [/F1]

Loads the negative contents of *DramDR* in the accumulator. If F1 is specified, the F1 flag is updated with the sign of the accumulator at the end of the command's execution. Relative address distance is +4, -3.

ADD *DramDR* [/ABS] [/F1]

Adds the contents of *DramDR* to the accumulator. If [ABS] is specified, the absolute value of *DramDR* is added. If F1 is specified, the F1 flag is updated with the sign of the accumulator at the end of the command's execution. Relative address distance is +4, -3.

SUB *DramDR* [/ABS] [/F1]

Subtracts the contents of *DramDR* from the accumulator. If [ABS] is specified, the absolute value of *DramDR* is subtracted. If F1 is specified, the F1 flag is updated with the sign of the accumulator at the end of the command's execution. Relative address distance is +4, -3.

XSIGN *DramDR* [/F1]

Multiplies the accumulator by the sign of *DramDR*—if *DramDR* is negative, the accumulator will be inverted. If F1 is specified, the F1 flag is updated with the sign of the accumulator at the end of the command's execution. Relative address distance is +4, -3.

NOP

An arithmetic command that does nothing.It is sometimes useful before STO and conditional JMP commands. This command is always short.

LKUP

Loads the accumulator with the left justified DRAM value pointed to by the accumulator. The upper 8 bits of the accumulator are used as the DRAM address. The SAT module is always activated during LKUP. This command is always short.

STORE COMMANDS

STO *DramSR* [/RET] [{/F2, /F3}]

Store the accumulator in *DramSR*. If F2 or F3 is specified, the appropriate flag will be updated with the sign of the value being stored. Relative address distance is +2, -1. If RET is specified, the long form of this instruction is used.

STOSAT *DramSR* [/RET] [{/F2, /F3}]

Store the accumulator in *DramSR* with saturation logic enabled. If F2 or F3 is specified, the appropriate flag will be updated with the sign of the value being stored. Relative address distance is +2, -1. If RET is specified, the long form of this instruction is used.

STOLSW *DramSR* [/RET] [{/F2, /F3}]

Store the least significant word. This command stores the accumulator in *DramSR* and then shifts the sign bits right by 16 bits. The extra LSB bits are cleared. If F2 or F3 is specified, the appropriate flag will be updated with the sign of the value being stored. Relative address distance is +2, -1. If RET is specified, the long form of this instruction is used.

STODR *DramSR* [/RET] [{/F2, /F3}]

Stores the DATA REG contents in *DramSR*. This command permits fast data moves since the data does not have to flow through the accumulator pipeline. If F2 or F3 is specified, the appropriate flag will be updated with the sign of the value being stored. Relative address distance is +2, -1. If RET is specified, the long form of this instruction is used.

PROGRAM CONTROL

JMP *label:*

An unconditional jump. Relative address distance is +8, -7.

JSUB *label:*

An unconditional subroutine call. This is always a long instruction.

JF *label:* {/F1, /F2, /F3}

Jump if flag is one. Relative address distance is +8, -7. If F2 or F3 is specified, the long form is used.

JFB *label:* {/F1, /F2, /F3}

Jump if flag is zero. Relative address distance is +8, -7. If F2 or F3 is specified, the long form is used.

JALU

A computed jump. The jump address is taken from the bottom 9 bits of the accumulator. This is a short instruction.

STOP

Stops execution of the program. The program restarts on a rising edge of DSPSTART pulse.

COMMAND SEQUENCING

Although the SEEKER™ DSP is a pipeline architecture, instruction sequencing is unaffected except in one case.

Commands that depend on accumulator results such as STORE and conditional jump must allow one cycle to occur after the accumulator instruction completes. If the accumulator instruction requires more than one cycle to complete (MLD or MADD), the STORE or conditional jump must be placed one ALU instruction after the accumulator command. This allows the result to propagate into the accumulator before it is stored.

Example 1: Calculate C=A•B and E=A•B+D.

```
MLD   A B    ;load accumulator with A•B
ADD   D      ;add D to accumulator
STO   C      ;store A•B in C
STO   E      ;store A•B+D in E
```

Example 2: Calculate C=A•B and E=A•B+D•F.

```
MLD   A B    ;load accumulator with A•B
MADD  D F    ;add D•F to accumulator
STO   C      ;store A•B in C
NOP          ;NOP is an ALU instruction
STO   E      ;store A•B+D•F in E
```

CYCLE COUNTING

All instructions execute in one cycle except MLD and MADD instructions which require a setup cycle and 4 ALU cycles. During a multiply, the sequencer will execute up to 4 non-ALU instructions until it encounters another ALU command. Non-ALU commands include JUMP, STORE, and the setup cycle of MLD and MADD instructions. Thus it is often possible to store results and setup the next multiply without consuming clock cycles.

Example 3: Calculate a 2 pole Chebyshev low pass:

$$v_{out} = z^{-1}(v_x + K_3 v_{out})$$

$$v_x = v_x z^{-1} + v_{in} K_1 - v_{out} K_2$$

```
LD      VX          ;(1 clock) load vx
MADD    VIN K1      ;(5 clock) OLDVX + K1•VIN
MADD    VOUTNK2     ;(4 clock) the setup for this
                    instruction occurs during the
                    previous instruction.
MADD    VOUT K3     ;(4 clock) the setup for this
                    instruction occurs during the
                    previous instruction.
STO     VX          ;(0 clock) VX=OLDVX +
                    K1•VIN + K2•VOUT
LD      VX          ;(1 clock) begin new
                    calculation
STO     VOUT        ;(1 clock) VOUT=VX +
                    K3•VOUT
```

Thus this biquad requires 16 cycles to execute. Note that NK2 = -K2.

ASSEMBLER INPUT FILE

The assembler input file contains both DRAM initialization information and IRAM instructions. A typical structure for the file is:

```
;*****************************sample input file*********************
;sample.asm
;comments extend from ; to end of line
;
.dorg 0                 ;indicates the beginning of a DRAM section which will specify addresses
                        ;beginning with 0. If no value is specified, the addressing will start where the last
                        ;.dorg section ended.

zero:   data 0          ;values can be expressed in decimal
qrtr:   data 0x2000     ;or hex
x2:     data 256
        data
        data            ;DRAM labels are optional
prod:   data 0
adc1:
dac1:   data 0          ;more than one label can refer to the same address
temp:   data jump1      ;a DRAM value can be another DRAM or IRAM label.

.org            ;indicates the beginning of an IRAM section. As in the .dorg case, a value can be
                ;specified to indicate where in the IRAM the code is to be inserted.

lds     qrtr /shl=1     ;load qrtr into accumulator after being shifted by 1 bit to the left
radix   1               ;indicate that multipliers have the radix point 1 bit from left
sto     x2              ;store 0x4000 into x2
madd    adc1 qrtr  /f1  ;multiply adc1 times qrtr times two (due to RADIX), update f1
nop                     ;wait one arith cycle before result is valid for sto or jmp
jf /f1  jump1           ;jump if f1 is one
sto     prod            ;sto prod if positive
jmp     end
jump1:                  ;labels can be on a line by themselves
sto     dac1            ;if neg, send prod to dac1
end:    stop
;*****************************end of sample file*******************
```

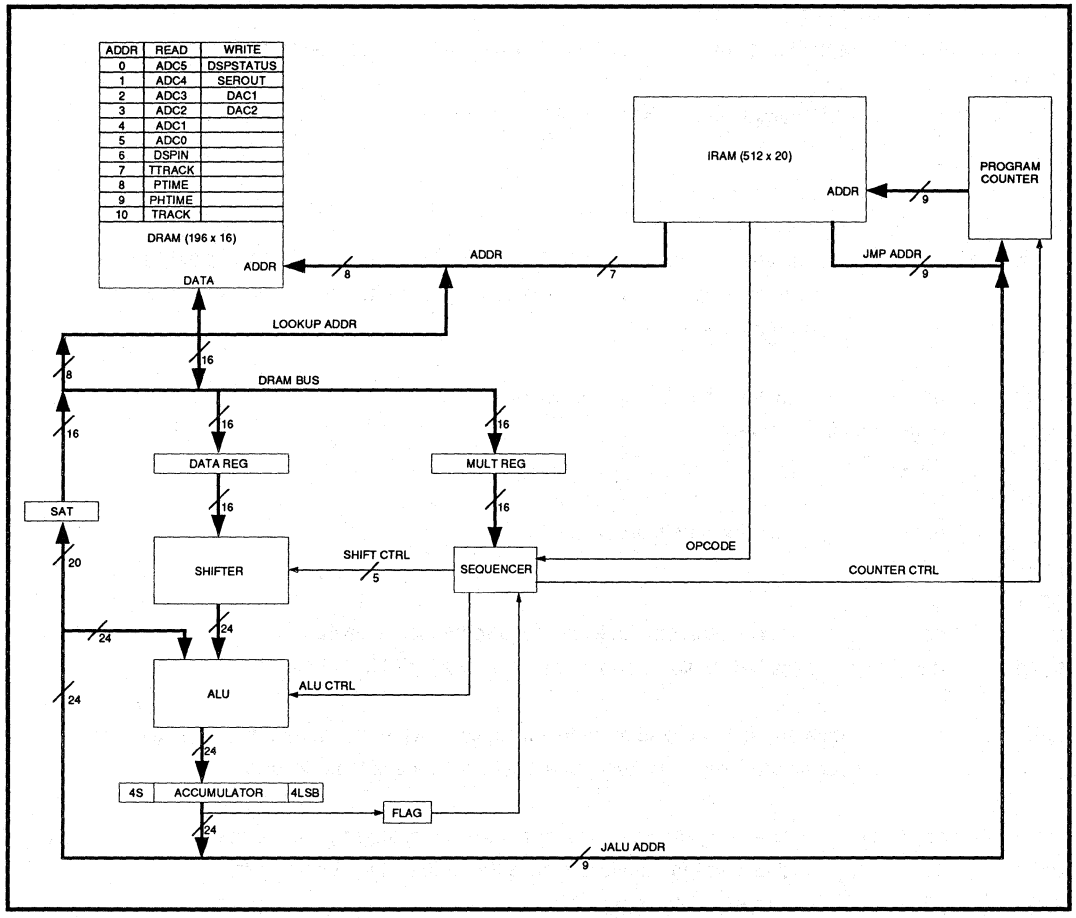
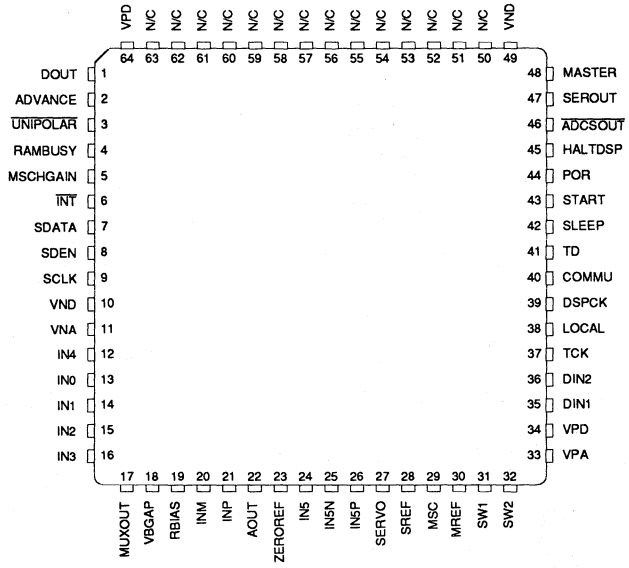


FIGURE 2: Programmer's Model

PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



64-Lead TQFP

7

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

Silicon Systems, Inc. 14351 Myford Road, Tustin, CA 92680 7022 (714) 573-6000, FAX (714) 573-6914

Notes:

Section 8

HDD SPINDLE MOTOR CONTROL

silicon systems®
A TDK Group Company

SSI 32M7010
Hall-Sensorless Motor Speed Control
Preliminary Data

February 1992

DESCRIPTION

The (Spindle) Motor Speed Control in conjunction with several external components, provides starting, accelerating, and precise rotational speed regulation functions. Different circuit versions are provided to control 4-, 8-, or 12-pole brushless DC motors without the need for Hall sensors. Control is accomplished via five pins and operation is monitored via two pins. The complete speed regulation control loop is contained in the circuit and the companion microprocessor is only required during start and to monitor status.

Motor speed control is accomplished by measuring the period of each revolution with a 500 kHz clock signal (SYSCLK divided by four). Period resolution is therefore 2 microseconds with the desired period being 8333 counts (16.66 milliseconds, or 3600.144 RPM).

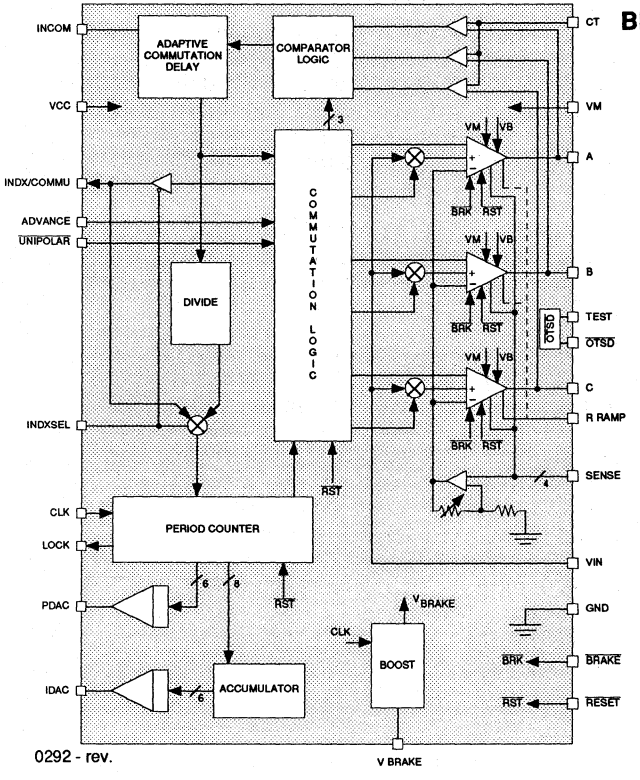
Motor armature position is determined by monitoring the coil voltage of the winding that is not presently being driven by the drivers. The back-emf at the coil in conjunction with the state of the output drivers, indicates armature position. The back emf is compared to a reference (CT) and initiates commutation when the

(continued)

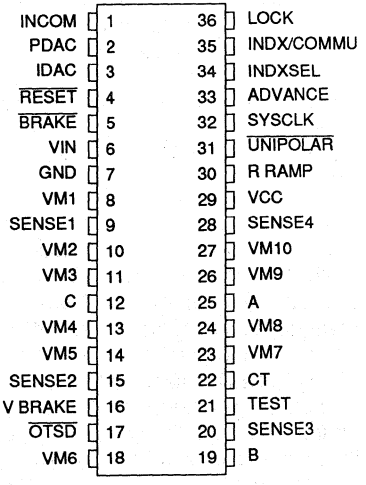
FEATURES

- **Precise speed control**
- **1 amp peak drivers**
- **No blocking diode**
- **Adaptive commutation delay**
- **Commutation transient suppression**
- **Convenient Retract / Brake Control**

BLOCK DIAGRAM



0292 - rev.



36-Pin SOM
PIN DIAGRAM

CAUTION: Use handling procedures necessary for a static sensitive component.

8

TABLE 1: Output Driver States

STATE	COMMU	PULL DOWNS A	B	C	PULL UP UPA	UPB	UPC
0, (Reset State)	1	off	on, (off)	off	on	off	off
1	0	off	off	on	on	off	off
2	1	off	off	on	off	on	off
3	0	on	off	off	off	on	off
4	1	on	off	off	off	off	on
5	0	off	on	off	off	off	on

DESCRIPTION (Continued)

appropriate comparison is made. Because the back-emf comparison event occurs prior to the time when optimum commutation should occur, commutation is delayed by a predetermined time after the comparison. The commutation delay is provided by a circuit which measures the interval between comparison events and delays commutation by a time equal to 0.43 of the prior interval. (The delay is set at 0.43 not 0.50 in order to compensate for commutation delays and motor current build-up time.) The circuit is adaptive and will provide the optimum delay for a wide range of motor speeds. Since the commutation of motor coils typically causes transients, the circuit also provides a noise blanking function which prevents response to back-emf comparison events for a period of time equal to 5/7 of the interval (between events) after the comparison event. The commutation delay can be externally modified by ±15% with the INCOM pin. The commutation states are shown in Table 1.

The period counter is loaded with a count of 8333 initially, and the period measurement results in residual counts (ideally zero) in the period counter as it counts down during the index to index time. The residual count is fed to the proportional DAC (5 bits plus sign). When there is no period error the PDAC will output 1/2 full scale (2.25/2 volts) from PDAC, too short a period will output a lower voltage, and too long a period will output a higher voltage, each depending on the amount of period error. When the residual count is within ± 15 counts of zero, the motor status is indicated as "in lock." The lower eight bits of the period counter are fed to an accumulator which adds the present period residue to the previous accumulation thus accomplishing an integrating effect which forces the speed error to zero over time. The upper six bits of the accumulator are fed to the integral DAC whose output is IDAC. Gross period errors will cause PDAC and IDAC to saturate at the appropriate extremes to achieve the maximum corrective control voltage.

The outputs PDAC and IDAC are connected to VIN with an external resistor network. The resistor values are selected to set the required loop response based on motor and system requirements. Input pin VIN is the non-inverting input of a linear transconductance amplifier which uses the lower driver transistor that is presently active per the commutation state as the power driver element. An external resistor is used to sense the current in the drive transistor source (and hence the motor coil current). The voltage across the sense resistor is amplified by a gain stage (Av=8) and fed to the inverting input of the transconductance output stage.

When the speed error is more than 3% slow, 2.25 volts is selected as the control voltage in lieu of VIN. Maximum motor current is limited to a value such that Imotor ≤ 2.25V/ (4 • R_{SENSE}).

Four operating conditions are selected via $\overline{BRAKE}$ and $\overline{RESET}$. With $\overline{BRAKE}$ and $\overline{RESET}$ asserted (low), outputs A, B, and C are low impedance to ground, (without current limiting function) and analog circuits are de-biased. This is the "sleep" condition. It also provides dynamic braking to the motor. With $\overline{BRAKE}$ asserted, and $\overline{RESET}$ de-asserted, drivers are low impedance to ground (without current limit function) and the analog circuitry is biased. For $\overline{RESET}$ asserted, $\overline{BRAKE}$ de-asserted, the output drivers are in a high impedance state. This will allow the user to take energy from the back-emf of a spinning motor for retracting heads. Normal operation is given for $\overline{BRAKE}$ and $\overline{RESET}$ de-asserted.

DESCRIPTION (Continued)

TABLE 2: Rout Low to SENSE

$\overline{\text{BRAKE}}$	$\overline{\text{RESET}}$	CONDITION	ANALOG	COUNTERS	A, B, C
0	0	SLEEP/BRAKE	OFF	RESET	Rout low to SENSE
0	1	BRAKE	ON	ACTIVE	Rout low to SENSE
1	0	RETRACT	ON	ACTIVE	FLOAT
1	1	RUN	ON	ACTIVE	ACTIVE

Motor starting is accomplished with a companion microprocessor utilizing ADVANCE, $\overline{\text{RESET}}$ and COMMU. The microprocessor can assert $\overline{\text{RESET}}$ to initialize the commutation counter and then increment the counter with ADVANCE. ADVANCE at logic high excludes internal commutations. COMMU provides feedback to the microprocessor on motor activity.

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
$\overline{\text{RESET}}$	I	When asserted low, internal counters and registers are cleared. Refer to Table 2.
$\overline{\text{BRAKE}}$	I	$\overline{\text{BRAKE}}$ is used to provide a delay between the initiation of Fault-induced head retract and motor braking. A capacitor to ground and a resistor to $\overline{\text{RESET}}$ are selected such that 1.2•R•C is equal to the maximum time required for retract.
SYSCLK	I	Reference frequency for motor speed measurement. A 2.000 MHz SYSCLK will result in 3600 RPM motor speed for 8-pole motors. SYSCLK can be set to other frequencies to obtain a different rotational speed or operate with motors other than 8-pole configurations (use of an external index signal is only valid for 8-pole motors).
INDX/COMMU	I/O	When selected with INDXSEL set high, this pin is used to provide a once-per-revolution indication of rotational position and speed to the circuit. With INDXSEL low, COMMU (the LSB of the commutation counter) is presented as an output.
INDXSEL	I	See above.
LOCK	O	When the motor period is within ±15 counts of nominal, the motor is indicated as "in lock" with LOCK high.
ADVANCE	I	ADVANCE is used to increment the commutation counter. The rising edge of ADVANCE will increment the counter. ADVANCE held high will inhibit internal incrementing of the counter, ADVANCE held low permits the normal operation of commutation from back-emf events.
VM 1 - 10	-	Motor Power Supply.

PIN DESCRIPTION (continued)

NAME	TYPE	DESCRIPTION
INCOM	I	Adaptive commutator delay test point.
PDAC	O	Proportional DAC output pin. The proportional channel output is the lowest 5 bits plus sign of the period measuring counter. The LSB signifies a 2 microsecond period variation for SYSCLK = 2.00 MHz.
IDAC	O	Integral DAC output pin. The integral channel output comes from the upper six bits of an eight bit accumulator. The accumulator adds the lower eight bits of the period measurement to the previous value obtained from prior period measurements and accumulations.
VIN	I	Control Voltage input pin. The internal driver transistors and internal predriver circuits form a transconductance amplifier which will set motor current in relation to VIN. In conjunction with the SENSE input and the gain of the sense amplifier, transconductance (Gm) will be: Gm = Im/VIN = 1/ (Rs • 8).
SENSE1 SENSE2 SENSE3 SENSE4	I	Current monitoring sense amplifier (high side) input pin. The lower driver transistor current (hence motor current) is sent through a current sensing resistor to monitor motor current. The circuit will control the voltage across this resistor (multiplied by the gain of 8 in the sense amplifier) to match either VIN (during normal operation) or internal 2.25V (during low-speed operation with Av = 4).
A, B, C	O	Motor Drive Outputs. These pins provide drive to the motor coils.
CT	I	Back-EMF input from motor coil center tap. Input connected to the center tap for sensing generated back-emf voltages. The circuit uses the back-emf voltages to determie rotor position and effect commutation.
VCC	-	5V power pin.
V BRAKE	O	External capacitor to store charge for driver circuitry. The stored charge is used by the lower drivers in fault conditions to achieve dynamic braking.
GND	-	Ground connection. GND is the low side input to the current SENSE amplifier and care should be taken to see that GND and the low side of the sense resistor are at the same potential.
$\overline{\text{OTSD}}$	O	Indicates over temperature condition.
R RAMP	I	External resistor. Sets DV/DT for lower driver turn-off. DV/DT is approximately 4E 10 • R RAMP.
$\overline{\text{UNIPOLAR}}$	I	Select line for Unipolar or Bipolar mode.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

(Exposure to conditions in excess of the conditions given below may result in permanent damage or affect device reliability.)

PARAMETER		RATING
Supply Voltage	VCC	-0.3 to 7V
	VM	-0.3 to 15V
Digital Inputs/Outputs	SYSCLK, ADVANCE INDXSEL, INDX/COMMU, LOCK	-0.3 to VCC +0.3V
Analog I/O	PDAC, IDAC, VIN	-0.3 to VCC +0.3V
Motor Interface Voltage	CT, A, B, C, $\overline{\text{BRAKE}}$, SENSE, $\overline{\text{RESET}}$	-0.3 to 20V
Motor Interface Current	A, B, C, VM, SENSE	-1.0 to +1.0A
Storage Temperature, Tstg		-65 to 150°C
Lead Temperature, Tlead		300°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	VCC		4.75		5.25	V
	VM		4.75		5.25	V
Supply Current	ICC		1.0		10.0	mA
	ICC, Sleep Mode		0.05		1.0	mA
	IVM		0		0.75	A
	IVM, Sleep Mode		0.1		1.5	mA
Ambient Temperature	Ta		0		70	°C
Capacitive Load Digital I/O	Cl		0		100	pF
Resistive Load PROP, INTEGRAL	Rla		5000			Ω
Capacitive Load PROP, INTEGRAL	Cla		0		40	pF

8

ELECTRICAL SPECIFICATIONS (Continued)

DIGITAL INPUTS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Fmax, SYSCLK				4.5	MHz
Twh, Twl, SYSCLK width high or low		40			ns
External Index, INDX/COMMU (as input) Pulse Width		200			ns
Input Leakage, INDX/COMMU				10	µA
Input Leakage, others				1	µA
Vil (EXTINDX, SYSCLK, ADVANCE, INDXSEL)				0.8	V
Vih (inputs above)		2.0			V
Vil ($\overline{\text{RESET}}$, $\overline{\text{BRAKE}}$)	VBRAKE ≥ 4.5V			0.8	V
Vih ($\overline{\text{RESET}}$, $\overline{\text{BRAKE}}$)	VBRAKE ≥ 4.5V	2.0			V

PROPORTIONAL (PDAC), INTEGRAL (IDAC) OUTPUTS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Output Voltage	Iout ≤ 0.1 mA VCC = 5.0 V	0		2.25V ±5%	V
DAC Step Size	VCC = 5.0V	0.32		0.39	V
Output Impedance	0.5V ≤V out <2.0V Iout = 0.10 mA			200	Ω
Kp, Porportional Gain		0.70		0.85	V/rad/s
Ki, Integral Gain		10.48		12.75	V/rad

DIGITAL OUTPUTS, LOCK, INDX/COMMU

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Voh	Iout = -100 µA	2.4			V
Vol	Iout = 2.0 mA			0.4	V
Tdts, Time delay to tri-state output	INDXSEL high to high impedance on INDX/COMMU	10		100	ns
Tdoe, Time delay to enable as output pin	INDXSEL low to drive state	10		100	ns

ELECTRICAL SPECIFICATIONS (Continued)

VIN

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage		0		2.25	V
Input Current	0 ≤ Vin < 2.5V	-1		+1	µA

OUTPUTS A, B, C

Routup	Output in high state VM = 4.75V	0.05		1.0	Ω
Routlow	Output driving low, VM = 4.75V	0.05		1.0	Ω

SENSE

Vin, SENSE	Normal operation	0.0		0.4	V
	Low speed operation	0.0		0.8	V
Iin, SENSE	0.0 ≤ Vin < 1.0V	-10		+10	µA
Cin				20	pF
Transconductance gain from VIN to motor current (steady-state) will be given by: G = Imotor/VIN = 1/Rsense • 8, for rotational speeds greater than 3490 RPM.					

CT

Rin	-0.3V ≤Vin < 15V	30K			Ω
Cin				10	pF

V BRAKE

Ibst (run)	VCC = 4.75V			100	µA
Ibst (float)	VCC ≤ 0.5V			10	µA
Ibst (brake)	VCC ≤ 0.5V			10	µA

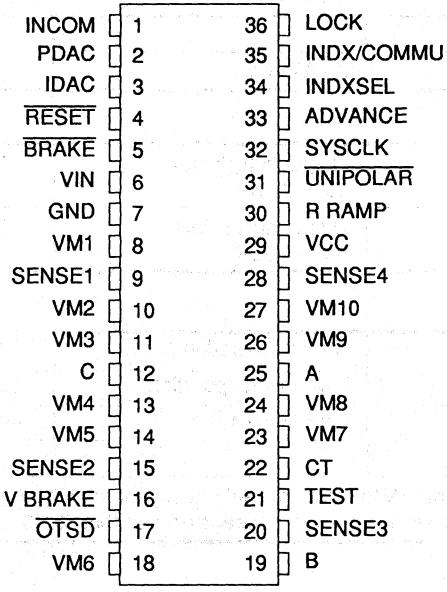
OPERATING REQUIREMENTS

LOCK Indication Range	SYSCLK = 2.000 MHz, 8-pole	3593.5		3606.5	RPM
Speed Resolution		-.012		+0.012	%

SSI 32M7010
Hall-Sensorless
Motor Speed Control

PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



36-Pin SOM

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 32M7010, Hall-Sensorless Motor Speed Control		
36-Pin SOM	32M7010-CM	32M7010

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914

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A TDK Group Company

SSI 32M7011
Hall-Sensorless Motor Speed Commutator
Advance Information

December 1993

DESCRIPTION

The (Spindle) Motor Commutator in conjunction with a companion microcontroller, provides starting, accelerating, precise rotational speed regulation functions, coasting (for retract), and dynamic brake. The circuit can be used with 4-, 8-, or 12-pole, 3 phase, brushless DC motors without the need for Hall sensors.

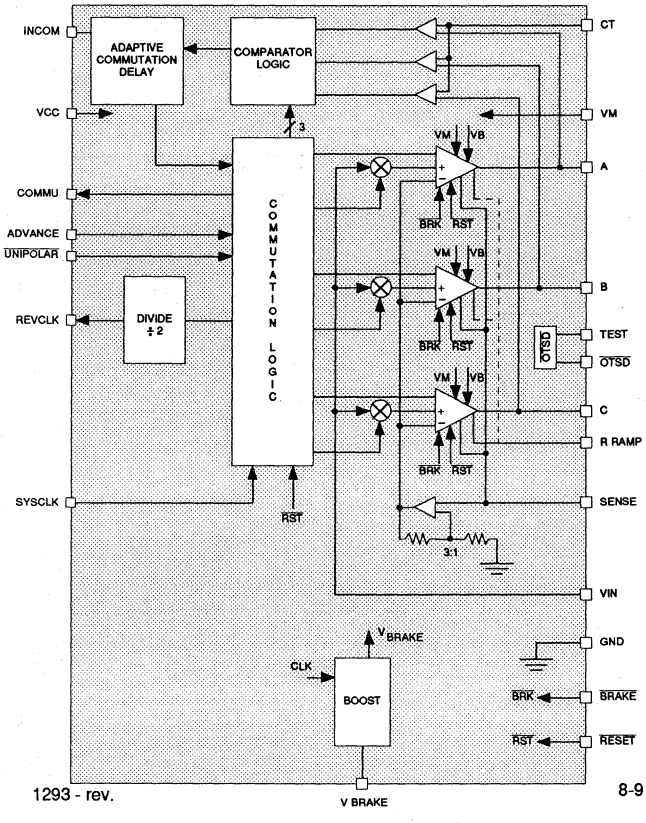
The commutator determines motor armature position by monitoring the coil voltage of the winding that is not presently being driven by the drivers. The back-emf at the coil in conjunction with the state of the output drivers, indicates armature position. The back emf is compared to a reference (CT) and initiates commutation when the appropriate comparison is made.

Because the back-emf comparison event occurs prior

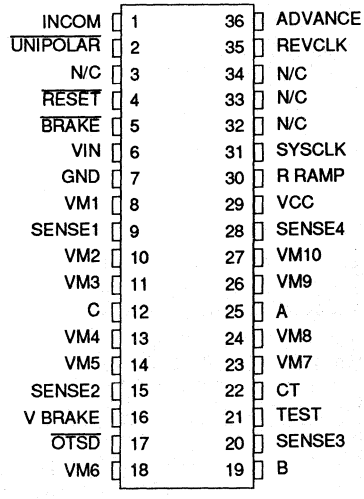
(continued)

FEATURES

- **Optimum commutation without external components**
- **Retract coast and brake modes supported**
- **1Ω FET drivers**
- **Commutation without Hall sensors**
- **Reduced DV/DT on commutation - no snubber networks required**
- **No blocking diode required**
- **Immune to brown outs and load transients**



BLOCK DIAGRAM



36-Pin SOM

PIN DIAGRAM

CAUTION: Use handling procedures necessary for a static sensitive component.

8

DESCRIPTION (Continued)

to the time when optimum commutation should occur, commutation is delayed by a predetermined time after the comparison. The commutation delay is provided by a circuit which measures the interval between prior comparison events and delays commutation by a time equal to 0.43 of the prior interval. (The delay is set at 0.43 not 0.50 in order to compensate for commutation delays and motor current build-up time.) The circuit is adaptive and will provide the optimum delay for a wide range of motor speeds. Since the commutation of motor current typically causes transients, the circuit also provides a noise blanking function which prevents response to back-emf comparison events for a period of time equal to 0.71 of the interval (between events) after the comparison event. The commutation delay can be externally modified by ±15% with the INCOM pin. The commutation states are shown in Table 1.

Input pin VIN is the non-inverting input of a linear transconductance amplifier which uses the lower driver transistor that is presently active per the commutation state as the power driver element. An external resistor is used to sense the current in the drive transistor source (and hence the motor coil current). The voltage across the sense resistor is amplified by a gain stage (Av=4) and fed to the inverting input of the transconductance output stage. Input voltage VIN must be generated from external means that use either REVCLK or other external rotational index indicators to measure rotational speed.

Four operating conditions are selected via $\overline{\text{BRAKE}}$ and $\overline{\text{RESET}}$. With $\overline{\text{BRAKE}}$ and $\overline{\text{RESET}}$ asserted (low), outputs A, B, and C are low impedance to ground, (without current limiting function) and analog circuits are de-biased. This is the "sleep" condition. It also provides dynamic braking to the motor. With $\overline{\text{BRAKE}}$ asserted, and $\overline{\text{RESET}}$ de-asserted, drivers are low impedance to ground (without current limit function) and the analog circuitry is biased. For $\overline{\text{RESET}}$ asserted, $\overline{\text{BRAKE}}$ de-asserted, the output drivers are in a high impedance state. This will allow the user to take energy from the back-emf of a spinning motor for retracting heads. Normal operation is given for $\overline{\text{BRAKE}}$ and $\overline{\text{RESET}}$ de-asserted.

Note that circuit utilizes NMOS driver transistors and does not require a Schottky blocking diode to prevent current flow from the spinning motor to the power supply. During RETRACT conditions, the motor is isolated from VM.

TABLE 1: Output Driver States

STATE	COMMU	PULL DOWNS A	B	C	PULL UP UPA	UPB	UPC
0, (Reset State)	1	off	on, (off)	off	on	off	off
1	0	off	off	on	on	off	off
2	1	off	off	on	off	on	off
3	0	on	off	off	off	on	off
4	1	on	off	off	off	off	on
5	0	off	on	off	off	off	on

TABLE 2: Rout Low to SENSE

$\overline{\text{BRAKE}}$	$\overline{\text{RESET}}$	CONDITION	ANALOG	COUNTERS	A, B, C
0	0	SLEEP/BRAKE	OFF	RESET	Rout low to SENSE
0	1	BRAKE	ON	ACTIVE	Rout low to SENSE
1	0	RETRACT	ON	ACTIVE	FLOAT
1	1	RUN	ON	ACTIVE	ACTIVE

Motor starting is accomplished with a companion microprocessor utilizing ADVANCE, $\overline{\text{RESET}}$ and COMMU. The microprocessor can assert $\overline{\text{RESET}}$ to initialize the commutation counter and then increment the counter with ADVANCE. ADVANCE at logic high excludes internal commutations. COMMU provides feedback to the microprocessor on motor activity.

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
$\overline{\text{RESET}}$	I	Refer to Table 2.
$\overline{\text{BRAKE}}$	I	$\overline{\text{BRAKE}}$ is used to provide a delay between the initiation of Fault-induced head retract and motor braking. A capacitor to ground and a resistor to $\overline{\text{RESET}}$ are selected such that 1.2•R•C is equal to the maximum time required for retract.
SYSCLK	I	2.0 MHz clock input signal.
COMMU	O	COMMU is the LSB of the commutation counter.
REVCLK	O	Indicates 1 revolution of 4-pole motor, 1/2 revolution of 8-pole, and 1/3 revolution of 12-pole motor.
ADVANCE	I	ADVANCE is used to increment the commutation counter. The rising edge of ADVANCE will increment the counter. ADVANCE held high will inhibit internal incrementing of the counter, ADVANCE held low permits the normal commutation due to back-emf events.
VM 1 - 10	Power	Motor Power Supply.
INCOM	I	Adaptive commutator delay trim. Generally a no-connect.
VIN	I	Control Voltage input pin. The internal driver transistors and internal predriver circuits form a transconductance amplifier which will set motor current in relation to VIN. In conjunction with the SENSE input and the gain of the sense amplifier, transconductance (Gm) will be Gm = Im/VIN = 1/ (Rs•4). The voltage at VIN must be controlled by external circuitry to accomplish speed control.
SENSE1 SENSE2 SENSE3 SENSE4	Power	Current monitoring sense amplifier (high side) input pin. The lower driver transistor current (hence motor current) is sent through a current sensing resistor to monitor motor current. The circuit will control the voltage across this resistor (multiplied by the gain of 4 in the sense amplifier) to match VIN.
A, B, C	O	Motor Drive Outputs. These pins provide drive to the motor coils.
CT	I	Back-EMF input from motor coil center tap. Input connected to the center tap for sensing generated back-emf voltages. The circuit uses the back-emf voltages to determine rotor position and effect commutation. 3 equal value resistors from A, B, and C attached to CT will suffice to synthesize a center-tap potential on three terminal motors. 4 terminal motors should use this terminal.
VCC	Power	5-volt power pin.

PIN DESCRIPTION (continued)

NAME	TYPE	DESCRIPTION
V BRAKE	O	External capacitor to store charge for driver circuitry. The stored charge is used by the lower drivers in fault conditions to achieve dynamic braking.
GND	-	Ground connection. GND is the low side input to the current SENSE amplifier and care should be taken to see that GND and the low side of the sense resistor are at the same potential.
$\overline{\text{OTSD}}$	O	Indicates over temperature condition and forces drivers off. Operation after cool down is restored by asserting ADVANCE.
R RAMP	I	External resistor. Sets DV/DT for lower driver turn-off. DV/DT is approximately $25 \cdot \frac{10^9}{\text{RRAMP}}$ (Volts / Second)
$\overline{\text{UNIPOLAR}}$	I	Select line for Unipolar or Bipolar mode. $\overline{\text{UNIPOLAR}}$ = low will de-activate upper drivers. Note: for BRAKE and SLEEP modes user must guarantee that external Unipolar driver transistor(s) do not conflict with lower driver transistors on circuit.
TEST	I/O	No connect, leave open circuited.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

(Exposure to conditions in excess of the conditions given below may result in permanent damage or affect device reliability.)

PARAMETER	SYMBOL	MIN	MAX	UNIT
Supply Voltage	VCC	-0.3	7	V
	VM	-0.3	7	V
Digital Inputs/Outputs	SYSCLK, ADVANCE COMMU, REVCLK	-0.3	VCC +0.3	V
Analog I/O	VIN, RRAMP, INCOM, TEST	-0.3	VCC +0.3	V
Motor Interface Voltage	CT, A, B, C, $\overline{\text{BRAKE}}$, SENSE, $\overline{\text{RESET}}$	-0.3	20	V
Motor Interface Current	A, B, C, VM, SENSE	-1.0	+1.0	A
Storage Temperature, Tstg		-65	150	°C
Lead Temperature, Tlead		-	300	°C

ELECTRICAL SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	VCC		4.75		5.25	V
	VM		4.75		5.25	V
Supply Current	ICC		1.0		10.0	mA
	ICC, Sleep Mode		0.05		1.0	mA
	IVM		0		0.75	A
	IVM, Sleep Mode		0		1.5	mA
Ambient Temperature	Ta		0		70	°C
Capacitive Load Digital I/O	Cl		0		100	pF

DIGITAL INPUTS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Fmax, SYSCLK		1.0	2.0	4.5	MHz
Twh, Twl, SYSCLK width high or low		40			ns
Advance Pulse Width		200			ns
Input Leakage, others				1	µA
Vil (SYSCLK, ADVANCE)				0.8	V
Vih (inputs above)		2.0			V
Vil ($\overline{\text{RESET}}$, $\overline{\text{BRAKE}}$)	VBRAKE ≥ 4.5V			0.8	V
Vih ($\overline{\text{RESET}}$, $\overline{\text{BRAKE}}$)	VBRAKE ≥ 4.5V	2.0			V

DIGITAL OUTPUTS, COMMU, REVCLK

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Voh	Iout = -100 µA	2.4			V
Vol	Iout = 2.0 mA			0.4	V

VIN

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage		0		2.25	V
Input Current	0 ≤ Vin < 2.5V	-1		+1	µA

ELECTRICAL SPECIFICATIONS (Continued)

OUTPUTS A, B, C

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Routup	Output in high state VM = 4.75V	0.05		1.0	Ω
Routlow	Output driving low, VM = 4.75V	0.05		1.0	Ω

SENSE

Vin, SENSE	Normal operation	0.0		0.5	V
Iin, SENSE	0.0 ≤ Vin < 1.0V	-10		+10	µA
Cin				20	pF
Transconductance gain from VIN to motor current (steady-state) will be given by: G = Imotor/VIN = 1/Rsense • 4.					

CT

Rin	-0.3V ≤Vin < 15V	30K			Ω
Cin				10	pF

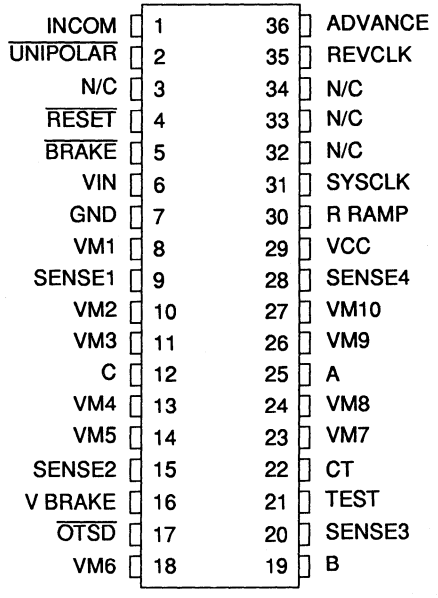
V BRAKE

Ibst (run)	VCC = 4.75V			100	µA
Ibst (float)	VCC ≤ 0.5V		25	100	µA
Ibst (brake)	VCC ≤ 0.5V		3	10	µA

PACKAGE PIN DESIGNATIONS

(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



36-Pin SOM

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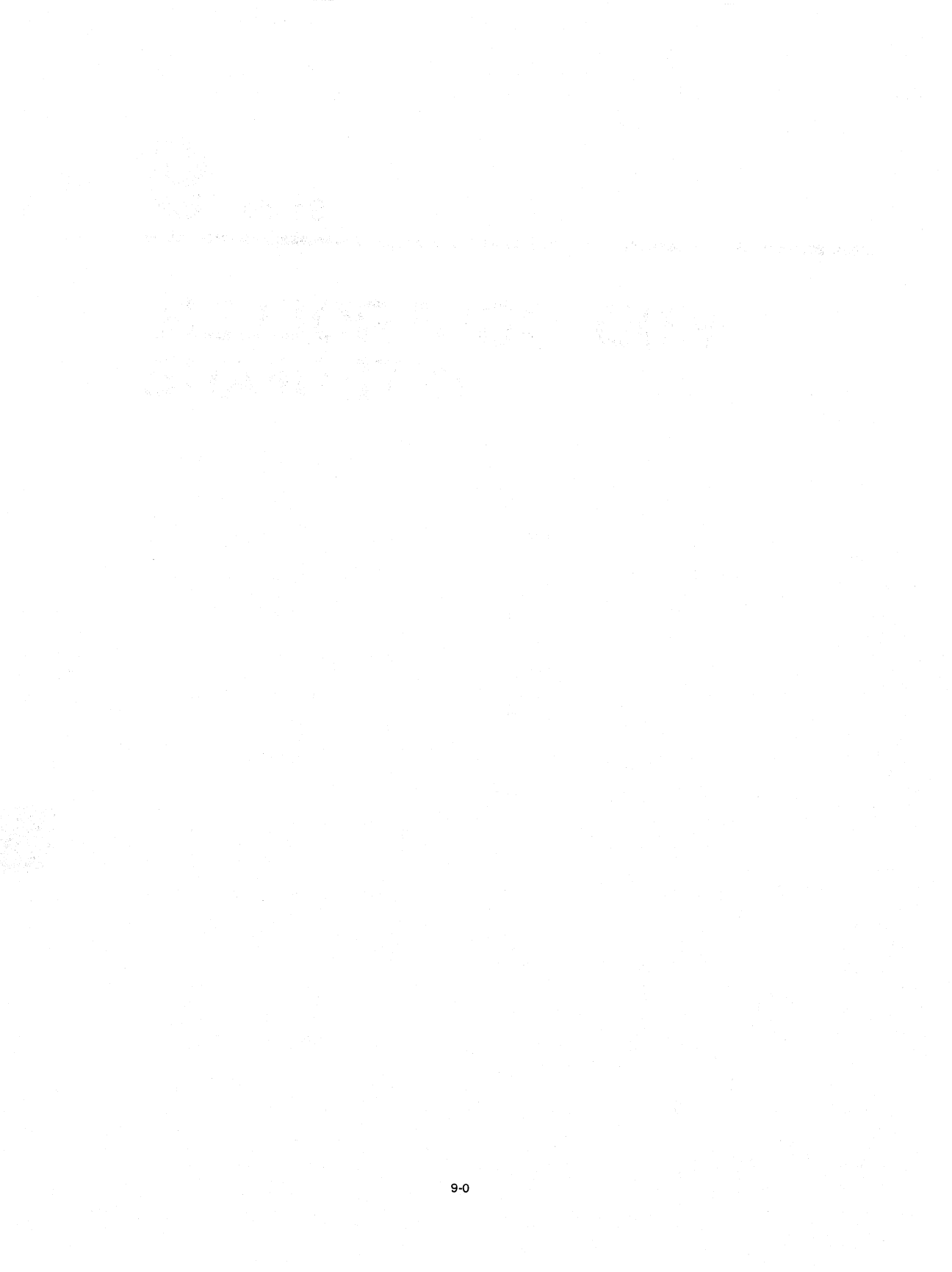
Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914

Notes:

Section 9

HDD CONTROLLER/ INTERFACE



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SSI 32C9001
PC-AT Combo Controller With Reed Solomon, 48 Mbit/s

Advance Information

January 1994

DESCRIPTION

The SSI 32C9001 is an advanced CMOS VLSI device which integrates major portions of the hardware needed to build an ATA disk drive. The circuitry of the SSI 32C9001 includes a complete ATA interface, an advanced buffer manager, a high performance disk formatter and an 88-bit Reed-Solomon ECC with fast "on-the-fly" hardware correction. The SSI 32C9001 provides maximum performance while minimizing micro controller intervention.

The SSI 32C9001 is capable of concurrent transfers of up to 48 megabits per second on the disk interface and 6 megawords (16-bit transfers) per second across the ATA bus. In addition, on-the-fly error corrections and micro controller accesses to the buffer memory will not degrade the throughput during transfers.

The high level of integration within the SSI 32C9001 represents a major reduction in parts count. When the SSI 32C9001 ATA Controller is combined with the

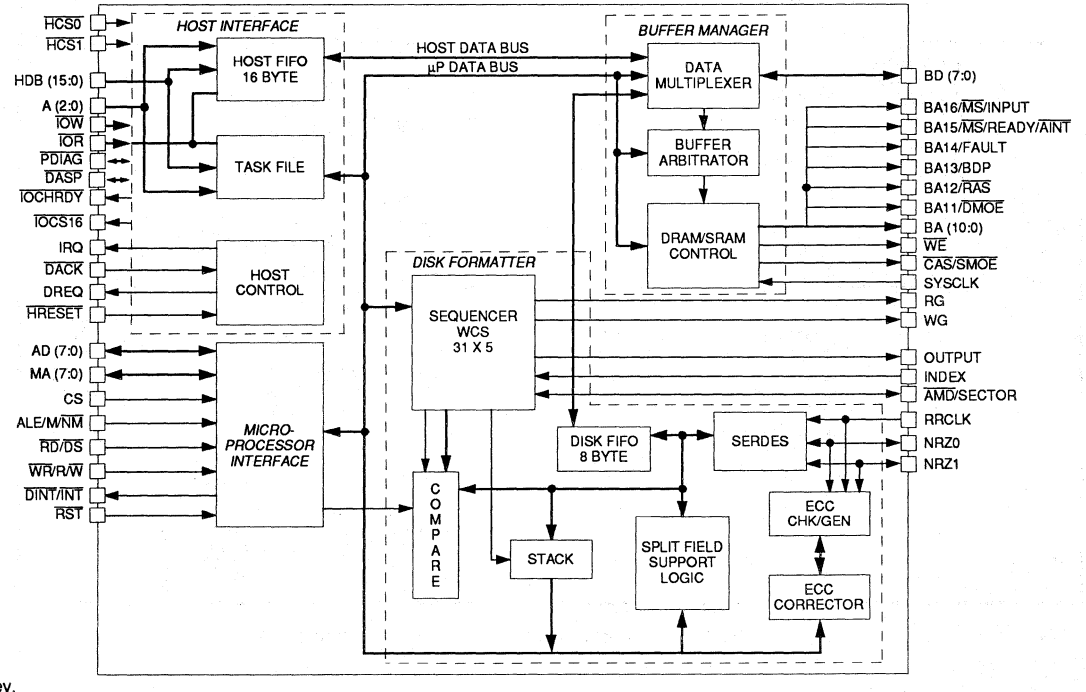
(continued)

FEATURES

- **ATA Interface**
  - **Single Chip PC AT Controller**
  - **Full ANSI ATA Compliance**
  - **Direct PC Bus connection with on board 12 mA drivers**
  - **PC transfers to 6 megawords/second (12 megabytes/second)**
  - **Supports PIO, DMA and multiword DMA (EISA Class B Demand DMA)**
  - **Logic for daisy chaining 2 drives**
  - **Operates as Master, Slave or both**
  - **Automatic command decoding of write, write long, write DMA, write multiple, write buffer and format commands.**
  - **Automatic updates of the host task file registers in both Cyl/Hd/Sec and LBA modes**

(continued)

BLOCK DIAGRAM



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SSI 32C9001
PC-AT Combo Controller
With Reed Solomon, 48 Mbit/s

DESCRIPTION (continued)

SSI 32R2010 Read/Write device, the SSI 32P3000 Pulse Detector, the SSI 32D5391 Data Synchronizer with 1,7 ENDEC, the SSI 32H4631 Servo and Motor Speed Controller, an appropriate micro controller and memory, a complete, cost efficient, high performance intelligent drive solution is created.

FEATURES (continued)

- Hardware support for write-multiple and read-mutiple commands
- Hardware added to provide Multi-Sector data transfers without microprocessor intervention
- Automatic Host Interrupt and Busy for multiple sector transfers
- 16 byte FIFO to improve performance
- Power Down I/O pins

• Buffer Manager
- Direct support of DRAM or SRAM
- SRAM: up to 128k bytes of memory with throughput to 20 megabytes per second
- DRAM: up to 1 megabyte of memory with throughput to 17.78 megabytes per second
- Programmable memory timing
- Supports page mode DRAM access
- Programmable page mode burst length
- Programmable DRAM refresh period
- Buffer RAM segmentation with flexible segment sizes from 256 bytes to 1 megabyte
- Dedicated host, disk and microprocessor address pointers
- Buffer Streaming with internal buffer protection circuit providing buffer integrity

• Disk Formatter
- NRZ Data Rates to 48 megabits per second
- Automatic multi-sector transfer
- Header or microprocessor based split data field support
- Advanced sequencer organized in 31 x 5 bytes
- Advanced branch and interrupt logic
- 88-bit Reed Solomon ECC with "on-the-fly" fast hardware correction circuitry
- Capable of correcting up to four 10-bit symbols in error

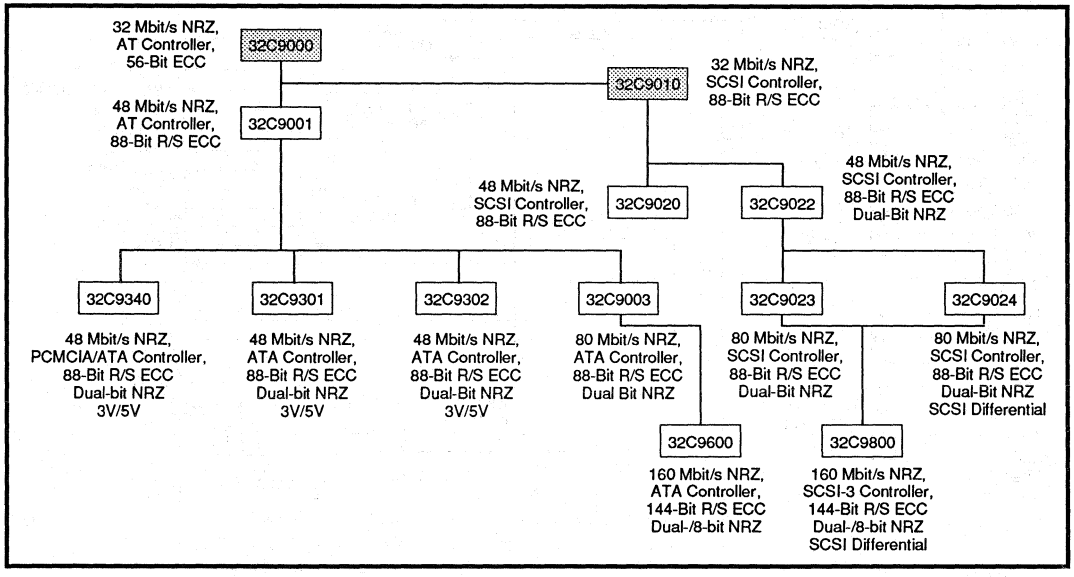

FIGURE 1: Silicon Systems' Disk Controller Chip Hierarchy

  - Guaranteed to correct one 31-bit burst or two 11-bit bursts
  - Hardware on-the-fly correction of an 11-bit single burst error within a half sector time
  - Detects up to one 51-bit burst or three 11-bit bursts
- Microprocessor Interface
  - Supports both multiplexed or non-multiplexed microprocessors
  - Separate or combined disk and host interrupts
- Other Features
  - Internal Power Down mode
  - Available in 100-lead TQFP

FUNCTIONAL DESCRIPTION

The SSI 32C9001 contains the following four major functional blocks:

Microprocessor Interface

ATA Interface

Disk Formatter

Buffer Manager

The Microprocessor Interface allows the local microprocessor access to all of the SSI 32C9001 internal control registers and any location within the buffer memory. The microprocessor, by writing and reading the internal registers, can control all activities of the SSI 32C9001. The microprocessor can elect to perform host and/or disk operations directly, or it can enable the advanced features of the SSI 32C9001 which can perform these operations automatically.

The ATA Interface block handles all PC AT bus activities. The ATA interface includes 12 mA drivers allowing for direct connection of the SSI 32C9001 to the PC AT bus. The ATA interface block is highly automated, capable of performing multiple block transfers without micro controller involvement. The ATA block interfaces directly with the Buffer Manager via an internal speed matching FIFO. This FIFO, the bandwidth capabilities of the Buffer Manager, plus the advanced features of the ATA Interface guarantee sustained full speed transfers across the PC AT bus.

The Disk Formatter performs the serialization and deserialization of data. It provides all of the necessary functions to control track formatting, header search, and the reading and writing of data. The heart of the Disk Formatter is an advanced programmable sequencer. The sequencer can contain 31 instructions, each of which is 5 bytes (40 bits) in width. The width of the instructions allows for sophisticated branching techniques which increase the flexibility and power of the sequencer. The disk interface can be configured through a wide range of capabilities, allowing the SSI 32C9001 to interface with nearly any read/write channel. This allows the user of the SSI 32C9001 to select the read/write channel best suited to the device. Of course, by selecting the SSI 32C9001 controller and the SSI 32D5391 Data Synchronizer with 1,7 ENDEC, you are guaranteed a problem free interface.

Within the Disk Formatter are the ECC generator/checker and ECC corrector. The generator/checker provides the ability to generate or check a 32-bit ECC for headers and an 88- bit Reed Solomon code for data. If the checker detects an error using the 88 bit Reed Solomon code, the syndrome information is transferred into the corrector. The corrector then performs the necessary operations to determine if the error was correctable and, if it was correctable, the corrector interfaces directly with the buffer controller and performs the correction automatically. The corrector performs its correction within one quarter of a sector. This guarantees that the corrector will always be available to correct the next sector if necessary.

The Buffer Manager manages the data buffer of the controller. The Buffer Manager can support either SRAM or DRAM. When configured to operate with DRAM, the Buffer Manager automatically performs necessary refresh cycles. The buffer manager creates all of the necessary timing and control signals for a wide range of memory types and speeds. Besides interfacing with the buffer memory, the Buffer Manager interfaces with the ATA Interface block, the Disk Formatter block, the ECC corrector and the microprocessor. If more than one of these devices requires access to the buffer memory, the Buffer Manager arbitrates the requests automatically. The Buffer Manager of the SSI 32C9001 can sustain ATA operations at the rate of 6 megawords per second, Disk Formatter operations at 48 megabits per second (6 megabytes per second) and still has sufficient band width left to handle on-the-fly ECC corrections and microprocessor accesses without degrading performance on any of the interfaces.

PIN DESCRIPTION

The following convention is used in the pin description:

- (I) denotes an input
- (O) denotes an output
- (I/O) denotes a bidirectional signal
- (Z) denotes a tri-state output
- (OD) denotes an open drain output

Active low signals are denoted by a bar on top of the signal name and dual function pins are denoted with a slash between the two signals — $\overline{AMD}$/SECTOR.

GENERAL

NAME	TYPE	DESCRIPTION
VDD		POWER SUPPLY PIN
GND		GROUND

HOST INTERFACE

A(2:0)	I	HOST ADDRESS LINES. The Host Address lines A(2:0) are used to access the various PC/AT control/status, and data registers.
$\overline{HCS1}$	I	HOST CHIP SELECT 1. This pin is used to access the control block task file registers.
$\overline{HCS0}$	I	HOST CHIP SELECT 0. This pin is used to access the command block task file resisters.
$\overline{IOCS16}$	OD	16 BIT DATA TRANSFER. An active low output that indicates that a 16-bit transfer is active.
IRQ	O, Z	INTERRUPT REQUEST. Asserted active high to indicate to the Host that the controller needs attention.
IORDY	O, Z	I/O READY. Active low, this signal is asserted to extend the host's I/O cycle.
DREQ	O, Z	DMA REQUEST. The active high DMA Request signal is used during DMA transfer between the Host and the controller to initiate DMA Transfers.
$\overline{DACK}$	I	DMA ACKNOWLEDGE. This active low signal is used during DMA to transfer data between the host and the controller.
$\overline{IOR}$	I	INPUT READ SELECT. This active low pin is asserted by the Host during a Host read operation. When asserted with $\overline{HCS0}$, $\overline{HCS1}$, or DACK, data from the device is enabled onto the host data bus.
$\overline{IOW}$	I	INPUT WRITE SELECT. Asserted active low by the Host during a Host write operation. When asserted with $\overline{HCS0}$, $\overline{HCS1}$, or DACK, data from the host data bus is strobed into the device.

HOST INTERFACE (continued)

NAME	TYPE	DESCRIPTION
$\overline{\text{HRESET}}$	I	HOST RESET. This active low signal stops all commands in progress and initializes the control/status registers — see Design Guide for Register Reset conditions. This signal can also "wake up" the device while it is in power down mode.
HDB (15:0)	I/O	HOST DATA BUS. These bits are used for word transfers between the Buffer Memory and the Host; note that for transferring commands, status or ECC only bits (7:0) are used.
$\overline{\text{PDIAG}}$	I, OD	PASSED DIAGNOSTICS. This active low pin is used as the passed diagnostics signal, and may be an input or an open-drain output.
$\overline{\text{DASP}}$	I, OD	DRIVE ACTIVE-SLAVE PRESENT. This pin is used as the Drive Active/Slave Present signal, and is an input or an open-drain output. This pin is used for Master/Slave drive communication and/or for driving an LED.

DISK INTERFACE

INDEX/INPUT	I	INDEX/INPUT. This pin serves as the index function for the disk sequencer. When the INPUT function is not available on the BA 15 pin, this pin can function as input or index.
OUTPUT	O	DISK SEQUENCER OUTPUT. This pin is controlled by bit 2 of the Control Field of the disk sequencer.
$\overline{\text{AMD}}$/SECTOR	I/O	ADDRESS MARK DETECT/SECTOR. In Hard Sector mode, this is the input for the sector pulse from the disk drive. In Soft Sector mode, a low-level input during a read indicates an address mark was detected.
RG	O	READ GATE. This active high output enables the reading of the disk. It is asserted by the sequencer Control Field bits 5 and 6. It is automatically deasserted at the end of the CRC or ECC.
WG	O	WRITE GATE. This active high output enables writing onto the disk. It is asserted and deasserted by the sequencer Control Field bits 5 and 6.
RRCLK	I	READ/REFERENCE CLOCK. This pin is used in conjunction with the NRZ pin to clock data in and out of the SSI 32C9001 device. This input must be glitch-free to ensure correct operation of the chip.
NRZ0	I/O	NRZ BIT 0. This signal is the read data input from the disk drive when the read gate signal is asserted; it is the write data output to the disk drive when the write gate signal is asserted. This pin is used for the least significant bit in dual bit NRZ mode; it is used for the serial data stream in single bit NRZ mode.
NRZ1	I/O	NRZ BIT1. This signal is the read data input from the disk drive when the read gate signal is asserted; it is the write data output to the disk drive when the write gate signal is asserted. This pin is used for the most significant bit in dual bit NRZ mode; it is not used in single bit NRZ mode.

PIN DESCRIPTION (continued)

MICROPROCESSOR INTERFACE

NAME	TYPE	DESCRIPTION
$\overline{RST}$	I	RESET. An asserted active low input generates a component reset that holds the internal registers of the SSI 32C9001 at reset, stops all operations within the chip, and deasserts all output signals. All input/output signals and Host outputs are set to the high-Z state.
ALE/$\overline{M}$/NM	I	ADDRESS LATCH ENABLE/MULTIPLEXED/NON-MULTIPLEXED ADDRESS SELECT. When tied high, the microprocessor interface is configured as non-multiplexed. When driven low, the microprocessor interface is configured as multiplexed. In this case this pin functions as the address latch enable, and the MA(7:0) pins are the demultiplexed address outputs.
CS	I	CHIP SELECT. This signal must be asserted high for all microprocessor accesses to the registers of this chip.
$\overline{WR}$/R/$\overline{W}$	I	WRITE STROBE/READ/WRITE. In the Multiplexed address/data bus mode, when an active low signal is present with CS signal asserted high, the data on the AD0:7 is written to the internal registers. In the Non-Multiplexed address/data bus mode, this signal acts as the R/$\overline{W}$ signal. A high on this input along with the $\overline{RD}$/DS signal asserted and the CS signal asserted high indicates a read operation. A low on this input along with the $\overline{RD}$/DS signal asserted and the CS signal asserted high indicates a write operation. See table below.

CS	$\overline{WR}$/R/$\overline{W}$	$\overline{RD}$/DS	Mux/Non-Mux	Action
High	Low	High	Intel Multiplexed	Write to internal registers.
High	High	Low	Intel Multiplexed	Read from internal registers.
High	Low	High	Motorola Multiplexed	Write to internal registers.
High	Low	Low	Non-Multiplexed	Write to internal registers.
High	High	High	Motorola Multiplexed	Read from internal registers.
High	High	Low	Non-Multiplexed	Read from internal registers.
Low	X	X	M or N	No action.

Note: X denotes don't care.

$\overline{RD}$/$\overline{DS}$	I	READ STROBE/DATA STROBE. In the Multiplexed address data bus mode, when an active low signal is present with CS signal high, internal registers will be accessed. In the Non-Multiplexed address data mode, this signal acts as the DS signal. A high on R/$\overline{W}$, with the CS and DS signals asserted, indicates a read operation. A low on the R/$\overline{W}$ signal, with the DS and the CS symbols asserted, indicates a write operation to the internal registers. Note: DS is active high in multiplexed mode, active low in non-multiplexed.
$\overline{DINT}$/$\overline{INT}$	O, OD	INTERRUPT. This signal is an interrupt line to the microprocesor. It is the combined interrupt line of the disk side and host side interrupts when pin RDY/$\overline{AINT}$ is programmed as ready; otherwise, it only signals the occurrence of disk side interrupt events. This signal is programmable for either a push-pull or open-drain output circuit. This signal powers up as an open drain output. May be programmed as active high or low; reset state is active low.

MICROPROCESSOR INTERFACE (continued)

NAME	TYPE	DESCRIPTION
AD(7:0)	I/O	ADDRESS/DATA BUS. When configured in the Multiplexed address data mode, these lines are multiplexed, bidirectional data path to the microprocessor. During the beginning of the memory cycle the bus captures the low order byte of the microprocessor address. These lines provide communication with the controller device's internal registers and the buffer memory. When configured in the Non-Multiplexed Microprocessors mode, these lines are bidirectional data lines only.
MA(7:0)	I/O	MICROPROCESSOR ADDRESS BUS. This 8-bit output bus is the AD(7:0) bus latched by the ALE pin during the address phase of a Multiplexed address data type microprocessor cycle. These signals are the address input when used with a non-multiplexed bus microprocessor.

BUFFER MANAGER INTERFACE

BA16/$\overline{MS}$/INPUT	I/O	BUFFER ADDRESS 16/MEMORY SELECT/DISK INPUT. In SRAM mode, this pin may be configured as buffer address 16, memory select, or as the input pin to the disk sequencer. In DRAM mode, this pin is configured as the input pin. If the input function is not available on this pin, then the INDEX pin may be used for the index function or the input function.
BA15/$\overline{MS}$/READY/$\overline{AINT}$	O	BUFFER ADDRESS 15/MEMORY SELECT/AT INTERRUPT/READY. In SRAM mode, this pin may be configured as buffer address 15, memory select, as a separate local microprocessor interrupt for the host interface, or as the ready function for adding wait states to local microprocessor accesses. In DRAM mode, AT interrupt or Ready may be selected. After $\overline{RST}$ is asserted, this signal is configured as Ready.
BA14/FAULT	I/O	BUFFER MEMORY ADDRESS 14/DISK FAULT. This signal is used for addressing the buffer memory in SRAM mode, or as the disk fault pin in DRAM mode. Assertion of the fault pin will cause the disk sequencer to halt immediately.
BA13/BDP	I/O	BUFFER MEMORY ADDRESS 13/BUFFER MEMORY PARITY. This signal is used for addressing the buffer memory in SRAM mode, or as the buffer data parity value in DRAM mode.
BA12/$\overline{RAS}$	O	BUFFER MEMORY ADDRESS 12/ROW ADDRESS STROBE: This signal is used for addressing the buffer memory in SRAM mode or as the row address strobe in DRAM mode. After $\overline{RST}$ is asserted, this signal will be high.
BA11/$\overline{DMOE}$	O	BUFFER MEMORY ADDRESS 11/DRAM MEMORY OUTPUT ENABLE. This signal is used for addressing the buffer memory in SRAM mode, or as the memory output enable pin in DRAM mode. After $\overline{RST}$ is asserted, this signal will be high.
BA(10:0)	O	BUFFER MEMORY ADDRESS LINES. These are signals 10-0 for addressing the buffer memory.
BD(7:0)	I/O	BUFFER MEMORY DATA BUS. These eight signals are bits 7-0 of the 8-bit parallel data lines to/from the buffer memory. Note that BD6 is used to select between the Intel- and Motorola-style microprocessor interfaces. If BD6 is externally pulled up when $\overline{RST}$ is asserted, Intel mode is used; if BD6 is externally pulled down when $\overline{RST}$ is asserted, Motorola mode is used.

PIN DESCRIPTION (continued)

BUFFER MANAGER INTERFACE (continued)

NAME	TYPE	DESCRIPTION
$\overline{CAS}/\overline{SMOE}$	O	COLUMN ADDRESS STROBE/SRAM MEMORY OUTPUT ENABLE. This signal is used as the column address strobe in DRAM mode, or the memory output enable in SRAM mode. After $\overline{RST}$ is asserted, this signal will be high.
$\overline{WE}$	O	MEMORY OUTPUT ENABLE. This active low output signal is used to strobe the data into the RAMs from the DAta bus. For both buffer memory applications, this line is tied directly to the SRAM or DRAM control pin.
SYSCLK	I	SYSTEM CLOCK. This signal is used to synchronize the buffer RAM access, including the generation of memory address lines, write enable WE, and memory output enable MOE. In power down mode, this signal is shut off from the internal logic and hence buffer memory access is inhibited.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC operating characteristics.

PARAMETER	RATING
Power Supply Voltage, VCC	7V
Ambient Temperature	0 to 70°C
Storage Temperature	-65 to 150°C
Power Dissipation	750 mW
Input, Output pins	-0.5 to VCC + 0.5V

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VCC Power Supply Voltage		4.5		5.5	V
ICC Supply Current				50	mA
ICCS Supply Current	Note 1			250	µA
VIL Input Low Voltage		-0.5		0.8	V
VIH Input High Voltage		2		VCC+0.5	V
VOL Output Low Voltage IOL = 2 mA	Note 2			0.4	V
VOL Output Low Voltage IOL = 24 mA	Note 3			0.5	V
VOH Output High Voltage IOH = -400 µA		2.4			V
IL Input Leakage Current 0 < VIN < VCC		-10		10	µA
CIN Input Capacitance				10	pF
COUT Output Capacitance				10	pF

ELECTRICAL CHARACTERISTICS (continued)

Note: (1) 4DH bit 6, 87H bits 4 and 3 set. RRCLK and SYSCLK internally inhibited.
(2) All interface pins except Host Interface pins.
(3) Host Interface pins.

MULTIPLEXED BUS MICROPROCESSOR INTERFACE TIMING PARAMETERS (FIGURES 2 THROUGH 5)

Ta	Ale Width		20			ns
Tma	Address valid to MA0:7 valid				30	ns
Tr	$\overline{RD}$ Width		80			ns
As	Address Valid to ALE ↓		5			ns
Ah	ALE ↓ to Address Invalid		10			ns
Cs	CS Valid to $\overline{RD}$ ↓ or $\overline{DS}$ ↓		20			ns
Ch	$\overline{RD}$ ↑ or $\overline{DS}$ ↑ to CS ↓		0			ns
Tda	$\overline{RD}$ ↓ or DS ↓ to Read Data Valid	Except Read of WCS			30	ns
	$\overline{RD}$ ↓ or DS ↓ to Read Data Valid	Read of WCS			50	ns
Tds	$\overline{DS}$ width		80			ns
Tdh	$\overline{RD}$ ↑ or $\overline{DS}$ ↑ to Read Data Invalid		0		25	ns
Tsrw	R/$\overline{W}$ valid to $\overline{DS}$ ↓		20			ns
Thrw	$\overline{DS}$ ↑ to R/W Invalid		20			ns
Tdrdy	$\overline{RD}$ ↓ to READY ↓ (Intel) or $\overline{DS}$ ↓ to READY ↓ (Motorola)				30	ns
Wds	Write data valid to $\overline{WR}$ ↑ or $\overline{DS}$ ↑		40			ns
Wdh	$\overline{WR}$ ↑ or $\overline{DS}$ ↑ to write data invalid		10			ns
Note:	↑ indicates rising edge	↓ indicates falling edge				

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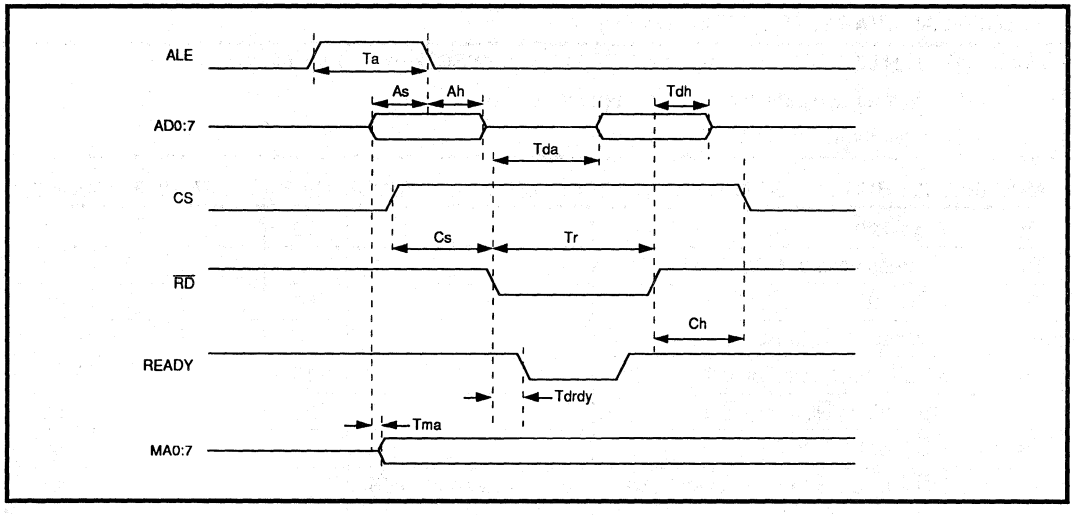


FIGURE 2: Intel Register Read Timing

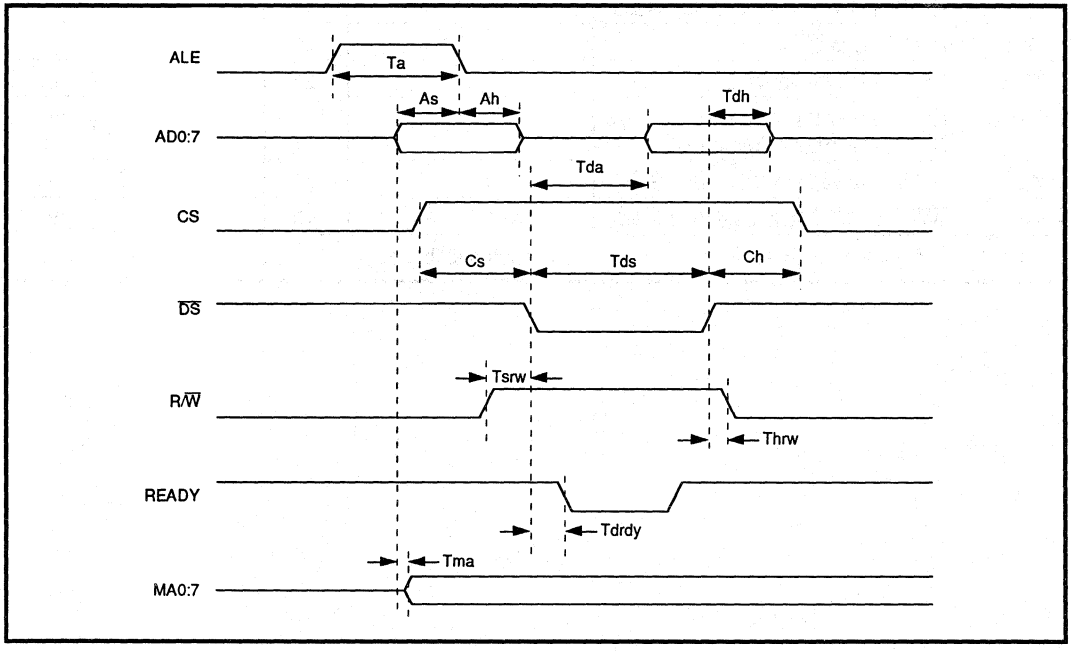


FIGURE 3: Motorola Register Multiplexed Read Timing

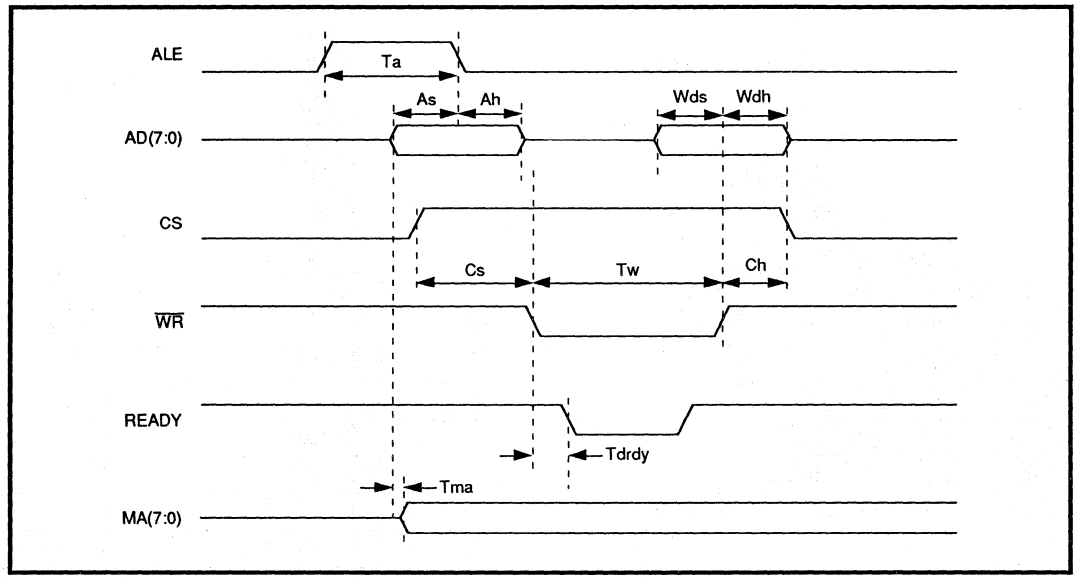


FIGURE 4: Intel Register Multiplexed Write Timing

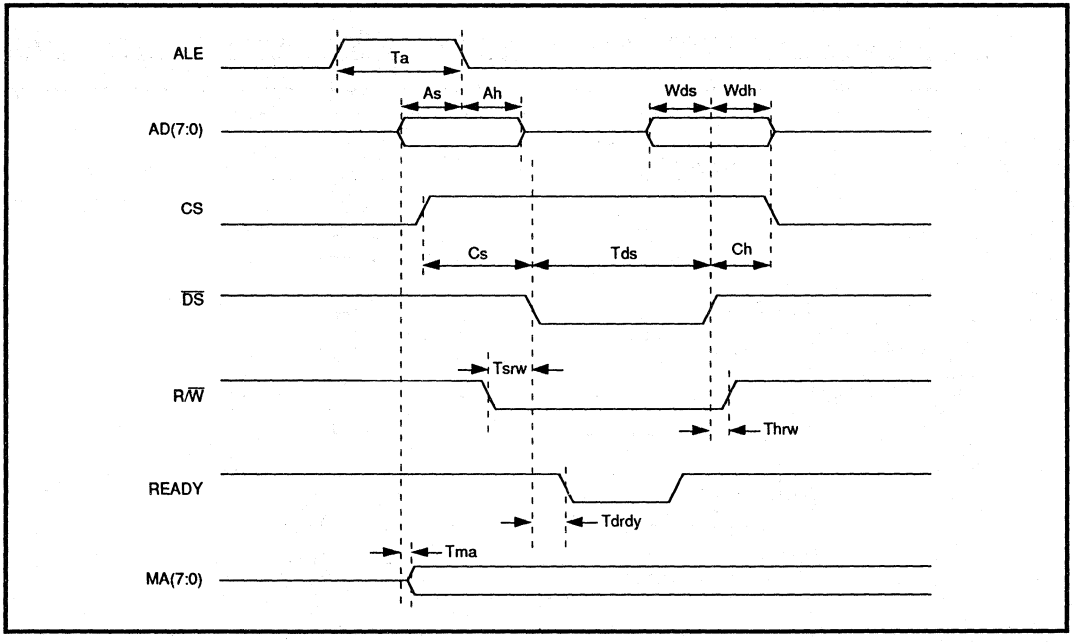


FIGURE 5: Motorola Register Multiplexed Write Timing

ELECTRICAL SPECIFICATIONS (continued)

NON-MULTIPLEXED BUS MICROPROCESSOR INTERFACE TIMINGS (FIGURE 6)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Tmas	MA(7:0) valid to $\overline{DS}$ ↑		5			ns
Tmah	$\overline{DS}$ ↓ to MA(7:0) invalid		5			ns
Cs	CS valid to $\overline{DS}$ ↑		20			ns
Ch	$\overline{DS}$ ↓ to CS ↓		0			ns
Tda	$\overline{RD}$ ↓ or DS ↓ to Read Data Valid	Except Read of WCS			30	ns
	$\overline{RD}$ ↓ or DS ↓ to Read Data Valid	Read of WCS			50	ns
Tds	DS width		80			ns
Tdh	$\overline{DS}$ ↓ to read data invalid		0		25	ns
Tsrw	R/$\overline{W}$ valid to $\overline{DS}$ ↑		20			ns
Thrw	DS ↑ to R/$\overline{W}$ invalid		20			ns
Tdrdy	$\overline{DS}$ ↑ to READY ↓ (Motorola) Note 3				30	ns
Wds	Write data valid to R/$\overline{W}$ ↑ or $\overline{DS}$ ↓		40			ns
Wdh	R/$\overline{W}$ ↑ or $\overline{DS}$ ↓ to write data invalid		10			ns

Note 1: ↑ indicates rising edge ↓ indicates falling edge

Note 2: Loading capacitor = 30pF

Note 3: Ready is not shown and is not used by Motorola processors. Timing provided for information only.

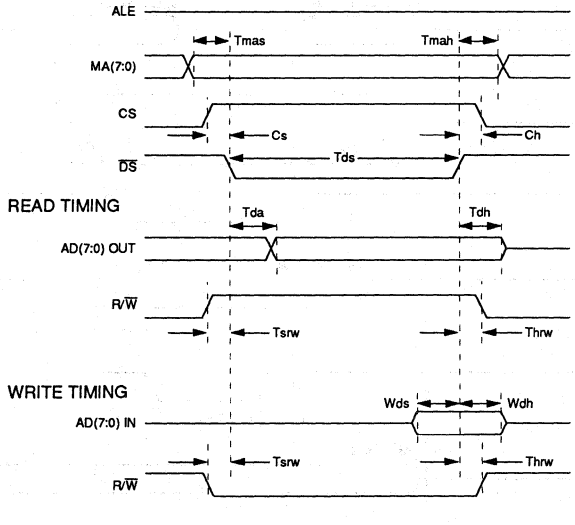


FIGURE 6: Non-Multiplexed Bus Timing Diagrams

DISK READ/WRITE TIMING (FIGURES 7 AND 8)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
T	RRCLK	Single bit NRZ	20.8			ns
		Dual bit NRZ	41			ns
T/2	RRCLK high/low time	Single bit NRZ	8.5			ns
		Dual bit NRZ	16			ns
Tr = Tf	RRCLK rise and fall time		0		2	ns
Ds	NRZ in valid to RRCLK ↑		3			ns
Dh	RRCLK ↑ to NRZ in invalid		4			ns
As*	$\overline{AMD}$ valid to RRCLK ↑		3			ns
Dv	RRCLK ↑ to NRZ out		3		20	ns
Wv*	RRCLK ↑ to WAM out		3		20	ns

Note: ↑ indicates rising edge ↓ indicates falling edge

* These specifications are only applicable in the Soft Sector mode.

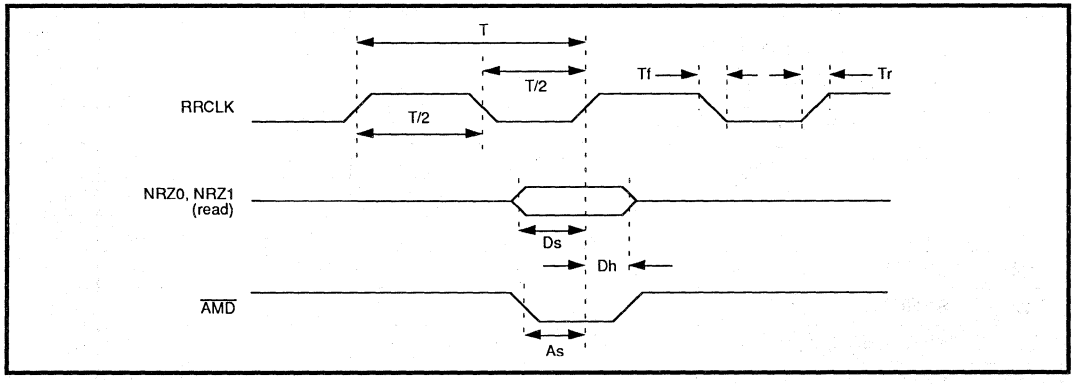


FIGURE 7: Disk Read Timing

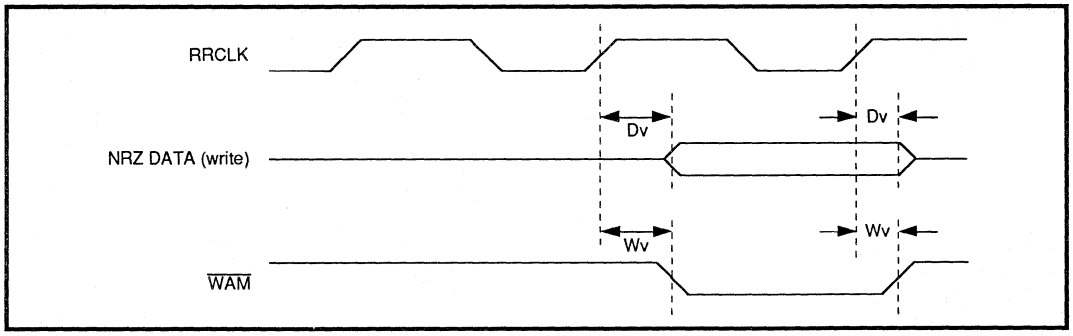


FIGURE 8: Disk Write Timing

ELECTRICAL SPECIFICATIONS (continued)

BUFFER MEMORY READ/WRITE TIMING PARAMETERS (FIGURES 9 THROUGH 13)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
T	SYSCLK period		25			ns
T/2	SYSCLK high/low time		10			ns
Tav	SYSCLK ↑ to address valid	Note 1			18	ns
Tmsv	SYSCLK ↑ to $\overline{MS}$↓	Notes 1, 6			18	ns
Tmsh	SYSCLK ↑ to $\overline{MS}$↑	Note 1			18	ns
Tmv	SYSCLK ↑ to $\overline{MOE}$↓	Note 1			18	ns
Tmh	SYSCLK ↑ to $\overline{MOE}$↑	Note 1			18	ns
Twv	SYSCLK ↑ to $\overline{WE}$↓	Note 1			18	ns
Twh	SYSCLK ↑ to $\overline{WE}$↑	Note 1			18	ns
Tdov	SYSCLK ↑ to data out valid	Note 1			18	ns
Tdoh	SYSCLK ↑ to data out invalid	Note 1			18	ns
Tdis	Data in valid to $\overline{MOE}$ ↑ (SRAM)		5			ns
	Data in valid to $\overline{CAS}$ ↑ (DRAM)		5			ns
Tdih	$\overline{MOE}$ ↑ to data in valid (SRAM)		0			ns
	$\overline{CAS}$ ↑ to data in valid (DRAM)		0			ns
Trv	SYSCLK ↑ to $\overline{RAS}$↓	Note 1			18	ns
Trh	SYSCLK ↑ to $\overline{RAS}$↑	Note 1			18	ns
Trav	SYSCLK to row address valid	Note 1			18	ns
Trah	SYSCLK ↑ to row address invalid	Note 1			18	ns
Tcv	SYSCLK ↑ to $\overline{CAS}$↓	Note 1			18	ns
Tch	SYSCLK ↑ to $\overline{CAS}$↑	Note 1			18	ns
Tcav	SYSCLK ↑ to column address valid	Note 1			18	ns
Tcah	SYSCLK ↑ to column address invalid		0			ns

BUFFER MEMORY READ/WRITE FUNCTIONAL PARAMETERS (FIGURES 9 THROUGH 13) (continued)

PARAMETER		CONDITIONS	MIN	UNIT
Trwl	$\overline{RAS}\downarrow$ to $\overline{RAS}\uparrow$	Notes 2, 3	((RWL + 3)•T)	ns
Trwh	$\overline{RAS}\uparrow$ to $\overline{RAS}\downarrow$	Notes 2, 4	((RWH + 1)•T)	ns
Tcwl	$\overline{CAS}\downarrow$ to $\overline{CAS}\uparrow$	Note 2	((CWL + 1)•T)	ns
Tcwl	$\overline{CAS}\uparrow$ to $\overline{CAS}\downarrow$	Notes 2, 5	((CWL + 1)•T)	ns

Note: Loading capacitance = 30 pF

Note 1: The measured delay for any of the signal indicated by this note will not vary from the measured delay of any other signal indicated by this note by more than ±2 ns.

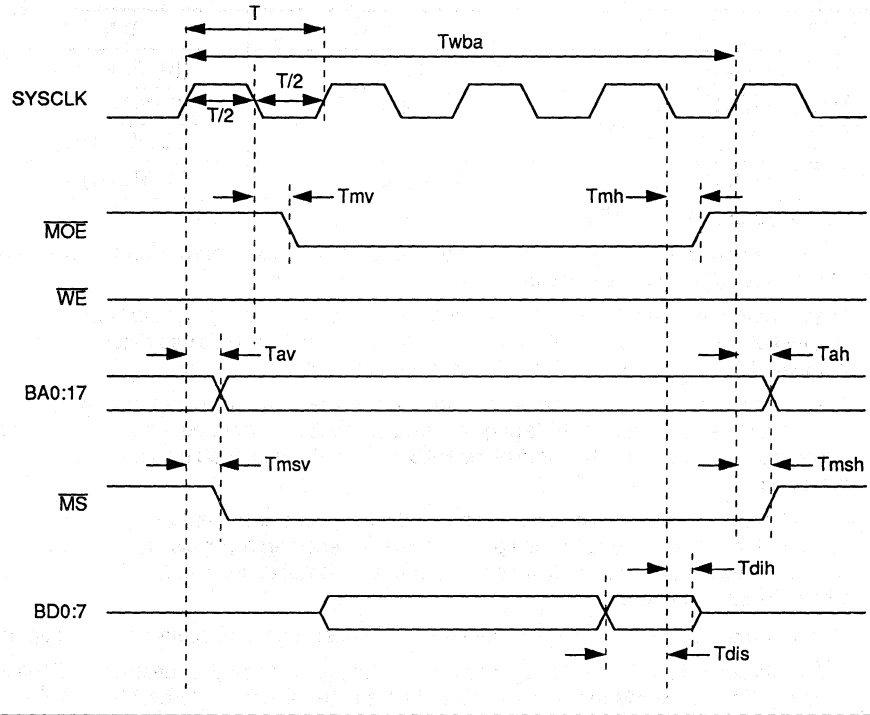
Note 2: RWL, RWH, CWL and CWH are fields in the Buffer Manager Timing Control Register (54H). Each is a two bit field which can contain a value of 0, 1, 2, or 3. These values determine the minimum number of SYSCLK periods (T) for the associated signal width.

Note 3: The minimum width value of Trwl will be generated for refresh cycles and for any buffer memeory access cycle except when multiple page mode accesses are performed. When multiple page mdoe accesses are performed, the width of the $\overline{RAS}$ low pulse is extended until the end of the last $\overline{CAS}$ low cycle.

Note 4: The minumum value of Trwh will be generated whenever the Buffer Manager determines that a buffer request is pending at the ocmpletion of the current memory cycle and a page mode access can not be used either because page mode operation is not enabled or the needed location is not within the current page.

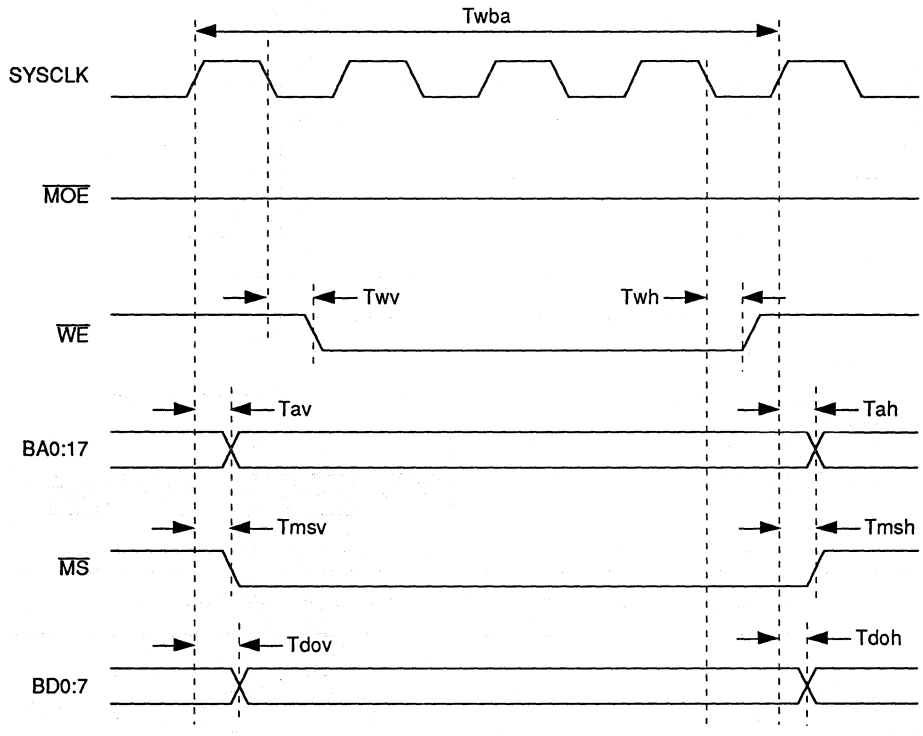
Note 5: The minumum value of Tcwh will be generated only between consecutive page mode accesses.

Note 6: $\overline{MS}$ will rise only if the Buffer Manager determines that no additional requests for buffer access are pending. If the Buffer Manager determines that another access is to be Made, $\overline{MS}$ is kept low between the accesses for improved speed.



Note: Twba equals one buffer RAM access cycle in SYSCLK periods.

FIGURE 9: SRAM Read Timing



Note: Twba equals one buffer RAM access cycle in SYSCLK periods.

FIGURE 10: SRAM Write Timing

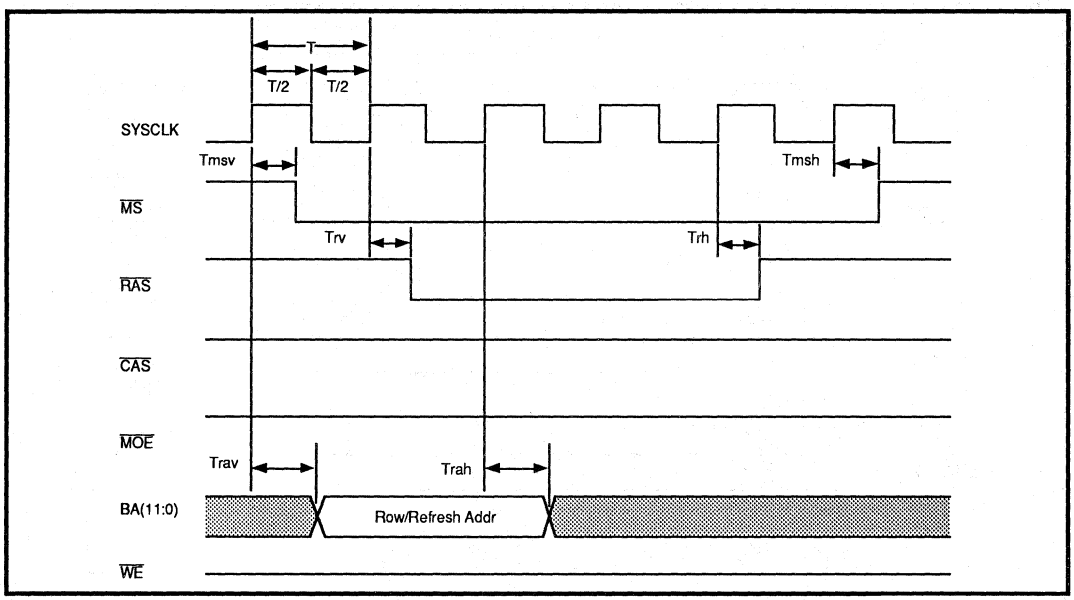


FIGURE 11: DRAM Timing, Refresh Cycle (Shown with WRL = 0)

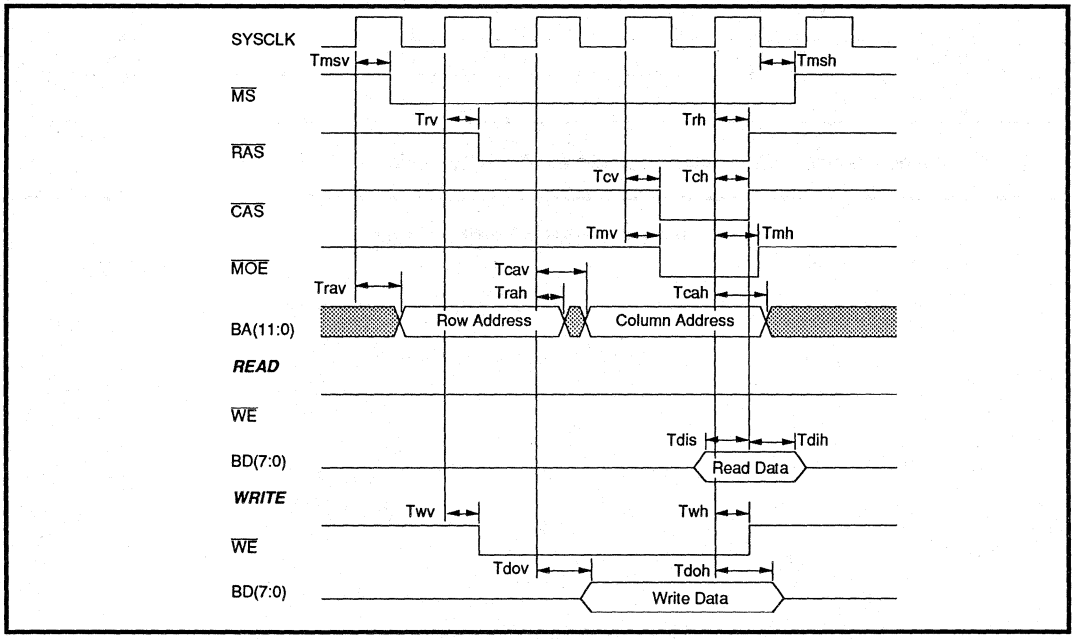


FIGURE 12: DRAM Timing, Standard Cycle (Shown with RWL = 0 and CWL = 0)

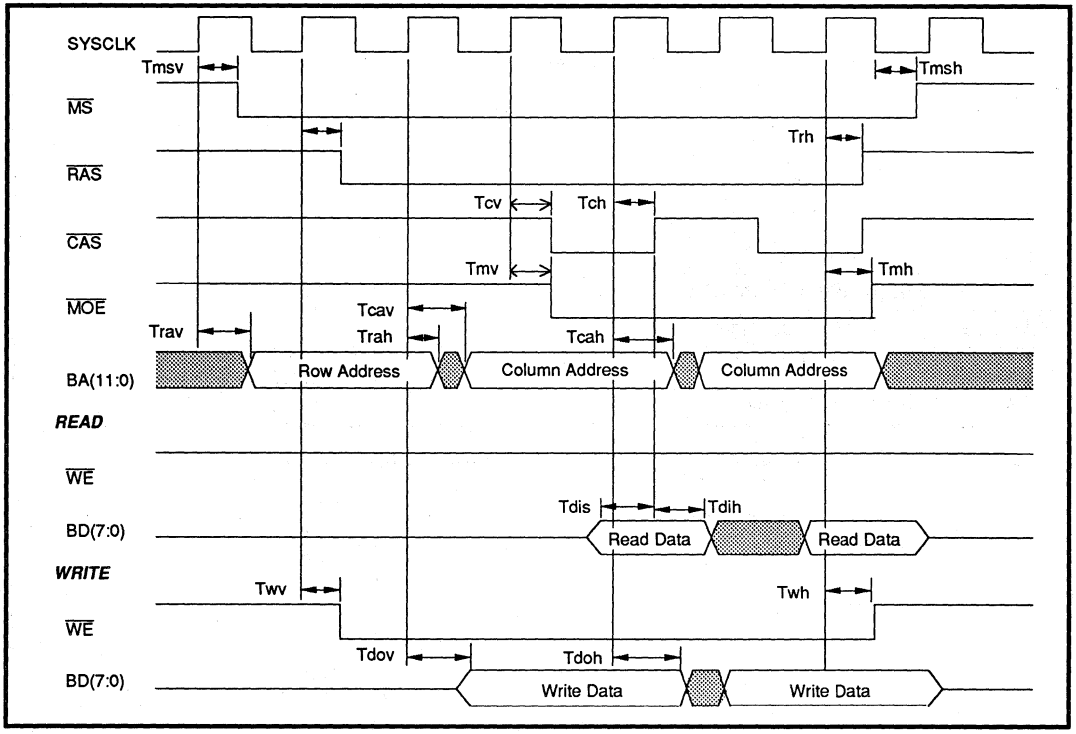


FIGURE 13: DRAM Timing, Fast Page Cycles (Shown with RWL = 0, RWH = 0, CWL = 0 and CWH = 0)

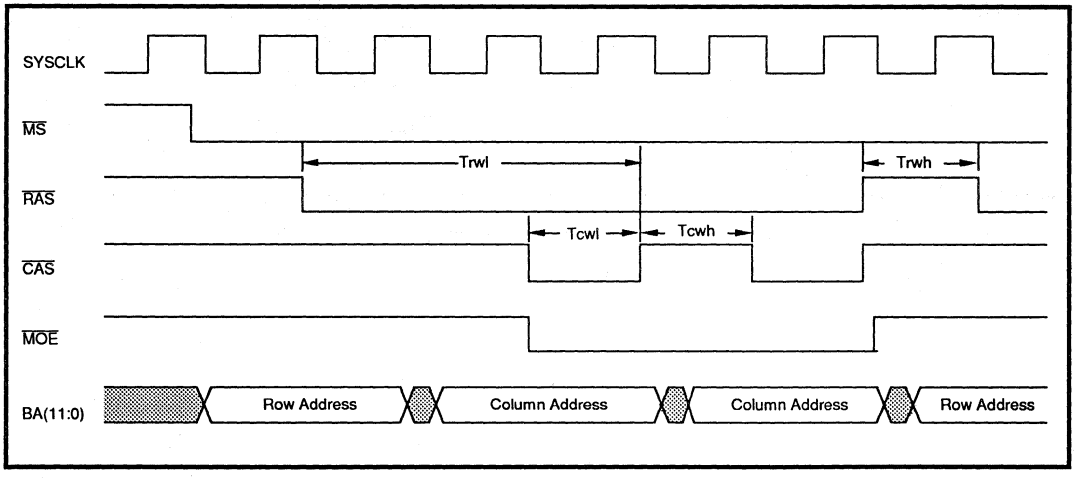


FIGURE 14: DRAM Timing (Showing the Relationship of RWL, RWH, CWL and CWH to overall timing)

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ELECTRICAL SPECIFICATIONS (continued)

HOST DMA 8/16-BIT INTERFACE TIMING PARAMETERS (FIGURE 15)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
DREQL	DREQ ↓ from $\overline{DACK}$ ↓				40	ns
RDTA	$\overline{IOR}$ ↓ to HD[0:15] valid				50	ns
RDHLD	$\overline{IOR}$ ↑ to HD[0:15] tri-state		2		25	ns
WDS	HD[0:15] setup to $\overline{IOW}$ ↑		30			ns
WDHLD	HD[0:15] hold from $\overline{IOW}$ ↑		10			ns
RWPULSE	$\overline{IOR}$/$\overline{IOW}$ pulse width		80			ns
DMASET	$\overline{DACK}$ ↓ to $\overline{IOR}$/$\overline{IOW}$ ↓		0			ns
DMAHLD	$\overline{DACK}$ hold from $\overline{IOR}$/$\overline{IOW}$ ↑		0			ns

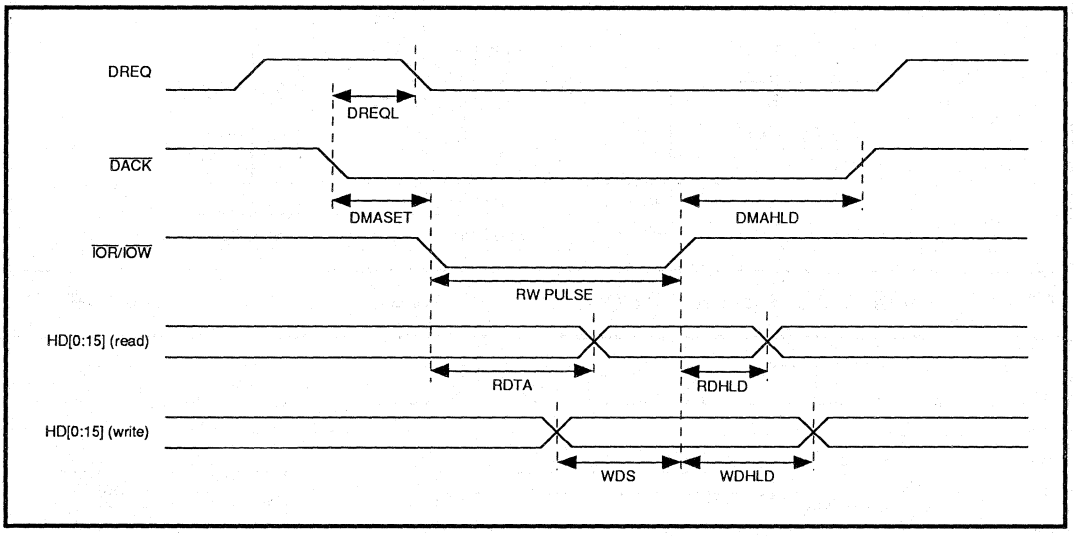


FIGURE 15: Host DMA 8/16-Bit Interface Timing

HOST DMA 8/16-BIT INTERFACE TIMING PARAMETERS (DEMAND MODE) (FIGURE 16)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
DMASET	$\overline{DACK}$ ↓ to $\overline{IOR}$/$\overline{IOW}$ ↓		0			ns
RDTA	$\overline{IOR}$ ↓ to HD [0:15} valid				50	ns
RDHLD	$\overline{IOR}$ ↑ to HD [0:15] tristate		2		25	ns
WDS	HD [0:15] setup to $\overline{IOW}$ ↑		30			ns
WDHLD	HD [0:15] hold from $\overline{IOW}$ ↑		10			ns
RWPULSE	$\overline{IOR}$/$\overline{IOW}$ low		80			ns
RWPAUSE	$\overline{IOR}$/$\overline{IOW}$ high		40			ns
DREQL	DREQ ↓ from $\overline{IOR}$/$\overline{IOW}$ ↓				40	ns
DMAHLD	$\overline{DACK}$ hold from $\overline{IOR}$/$\overline{IOW}$ ↑		0			ns

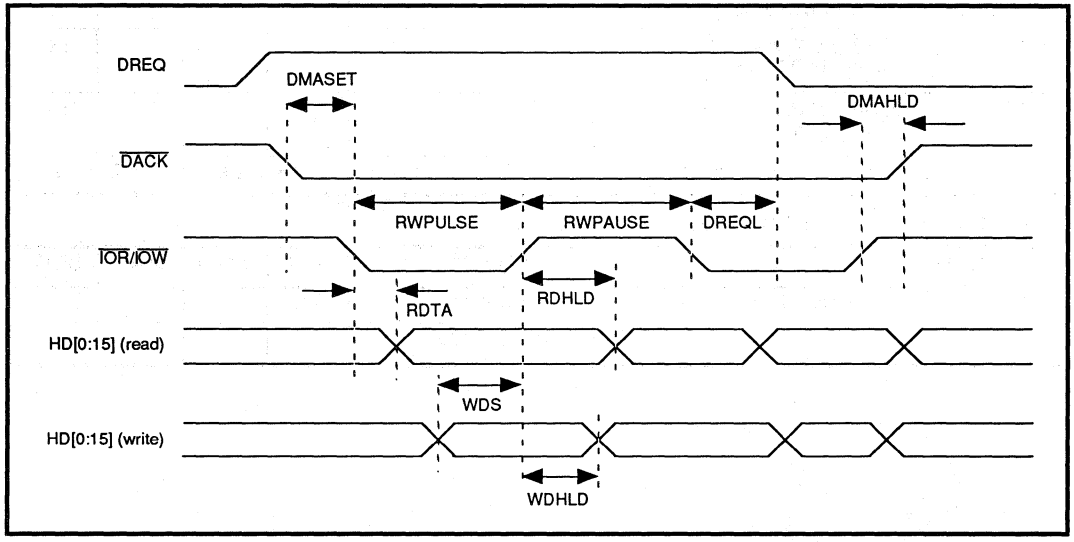


FIGURE 16: Host DMA 8/16-Bit Interface Timing (Demand Mode)

9

ELECTRICAL SPECIFICATIONS (continued)

HOST PROGRAMMED I/O TIMING PARAMETERS (FIGURE 16)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
CS16L	$\overline{HCS0}$ ↓, A0:2, A9 ↓, or $\overline{HSC1}$ ↑ to $\overline{IOCS16}$ ↓				25	ns
IOCHL	$\overline{IOR}$/$\overline{IOW}$ ↓ to $\overline{IOCHRDY}$ ↓				30	ns
IOCHTW *	IOCHRDY pulse width		0		5 x BCLK	ns
RDTA	$\overline{IOR}$ ↓ to HD[0:15] valid				50	ns
RDHLD	$\overline{IOR}$ ↑ to HD[0:15] tri-state		2		20	ns
WDS	HD[0:15] setup to $\overline{IOW}$ ↑		30			ns
WDHLD	HD[0:15] hold from $\overline{IOW}$ ↑		10			ns
RWPULSE	$\overline{IOR}$/$\overline{IOW}$ pulse width		80			ns
ADRSET	$\overline{HCS0}$, A0:2, A9/$\overline{HCS1}$ setup to $\overline{IOR}$/$\overline{IOW}$ ↓		25			ns
ADRHLD	$\overline{HCS0}$, A0:2, A9,$\overline{HCS1}$ hold, from $\overline{IOR}$/$\overline{IOW}$ ↑		5			ns

* Maximum specification applies when Auto Wait State Generation is disabled (Register 40H, Bit 2 is reset)

RESET ASSERTION TIMING PARAMETERS (FIGURE 17)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Trpwl	$\overline{RST}$ pulse width low	Not power on reset	500			ns
		Power on reset	7.5			µs

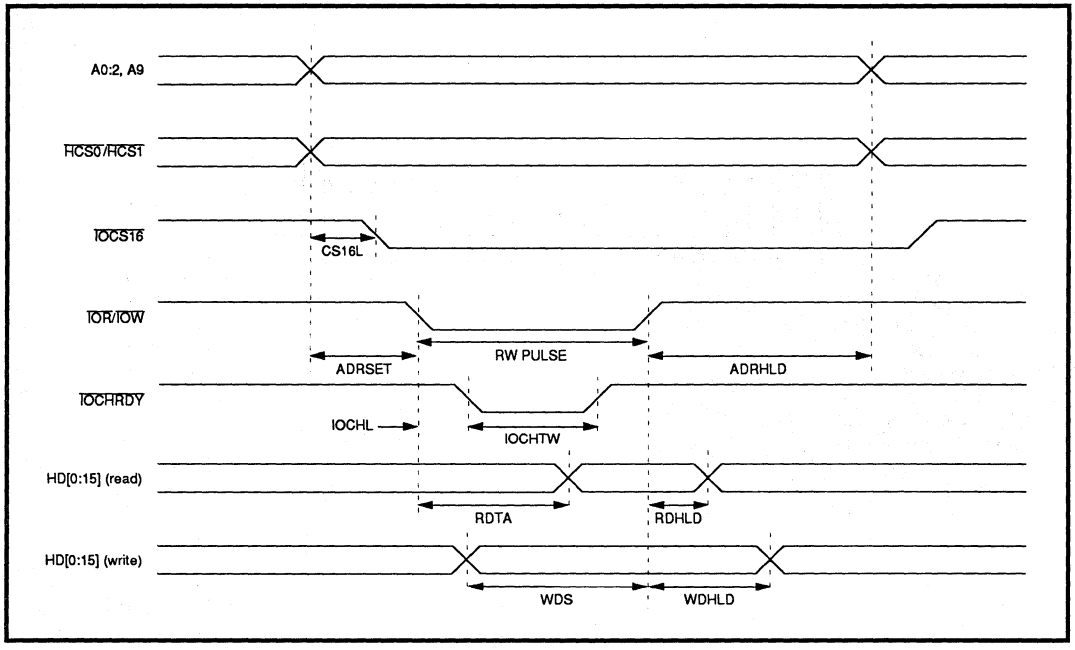
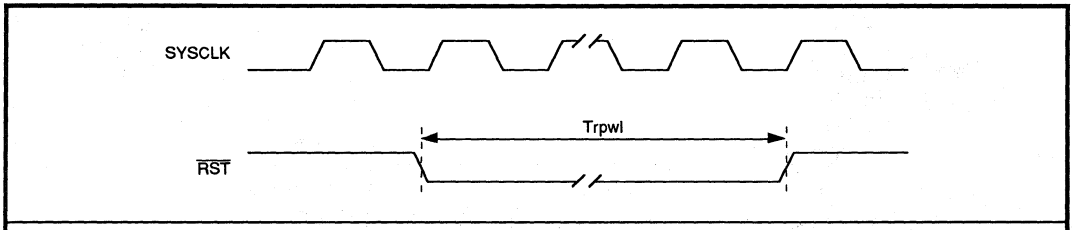


FIGURE 16: Host Programmed I/O 8/16-Bit Timing



Note: $\overline{RST}$ must be low for a minimum of 11 periods of SYSCLK.

FIGURE 17: RESET Assertion Timing

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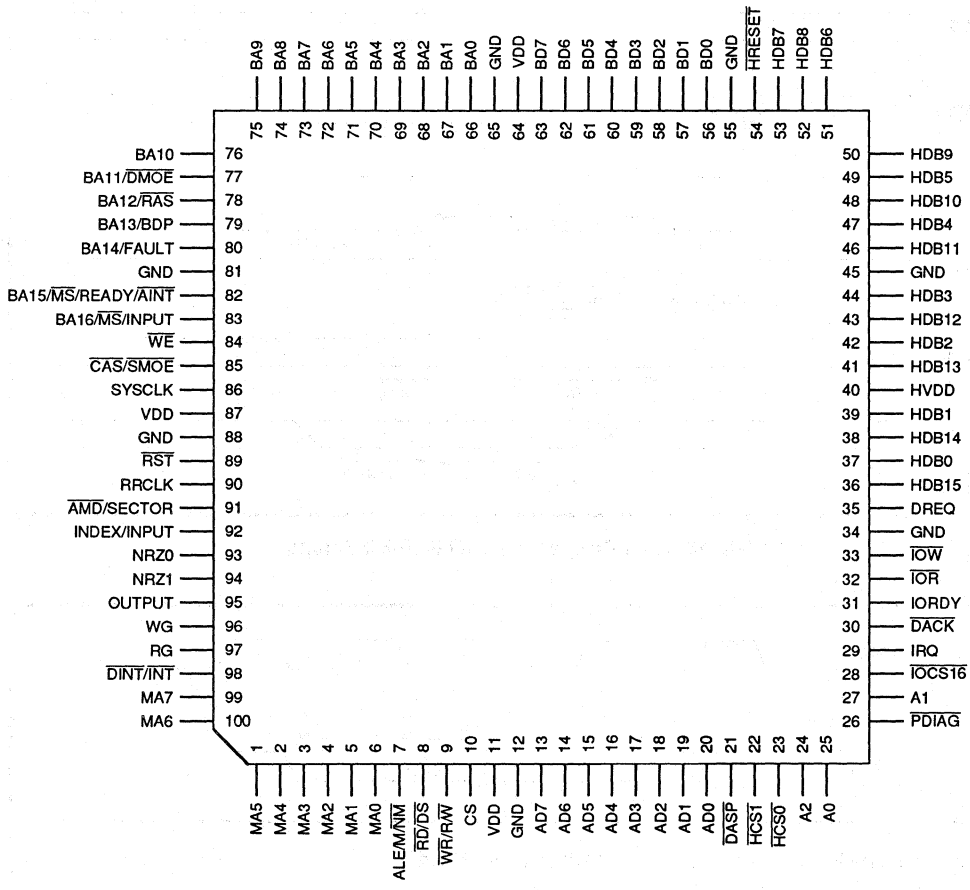
SSI 32C9001
PC-AT Combo Controller
With Reed Solomon, 48 Mbit/s

PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



100-Lead TQFP

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX: (714) 573-6914

silicon systems®
A TDK Group Company

SSI 32C9003
PC-AT Combo Controller
80 Mbit/s, Dual Bit NRZ Interface

Preliminary Data

January 1994

DESCRIPTION

The SSI 32C9003 is an advanced CMOS VLSI device which integrates major portions of the hardware needed to build an ATA disk drive. The 32C9003 has a dual bit NRZ interface to allow interfacing with channel ICs supporting this interface. The circuitry of the SSI 32C9003 includes a complete ATA interface, an advanced buffer manager, a high performance disk formatter and an 88 bit Reed-Solomon ECC with fast "on-the-fly" hardware correction. The SSI 32C9003 provides maximum performance while minimizing micro controller intervention.

The SSI 32C9003 is capable of transfers of up to 80 megabits per second on the disk interface and 6 megawords per second across the ATA bus. In addition, on-the-fly error corrections and microcontroller accesses to the buffer memory can occur during transfers.

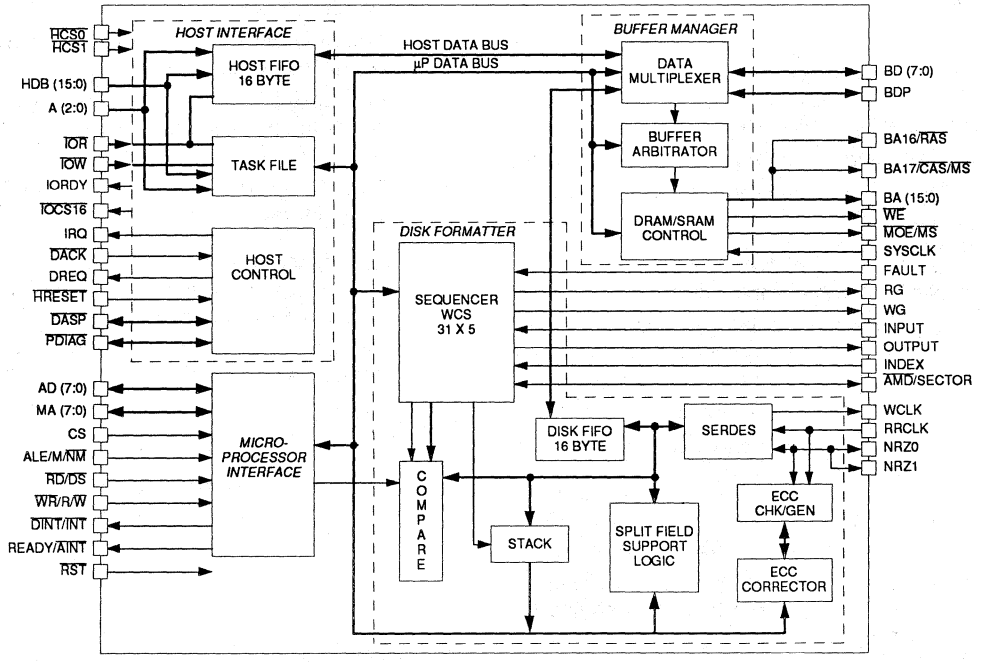
(continued)

FEATURES

- **ATA Interface**
  - **Single chip PC AT controller**
  - **Full ANSI ATA compliance**
  - **Direct PC bus connection with on board 24 mA drivers**
  - **PC transfers to 6.7 megawords per second**
  - **Supports PIO, DMA and Multiword DMA (EISA Class B Demand DMA)**
  - **Logic for daisy chaining 2 drives**
  - **Operate as master, slave or both**
  - **Hardware support for write-multiple and read-multiple commands**
  - **Automatic command decoding of Write, Write Long, Write DMA, Write Multiple, Write Buffer and Format commands**

(continued)

BLOCK DIAGRAM



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SSI 32C9003
PC-AT Combo Controller
80 Mbit/s, Dual Bit NRZ Interface

DESCRIPTION (continued)

The SSI 32C9003 is one of a family of Silicon Systems' single chip disk controllers which support a wide range of device interfaces. The 32C9301 and 32C9302 are both 3.3/5 volt dual voltage ATA controllers with a dual bit and single bit NRZ disk formatter interface. The SSI 32C9001 is a 5 volt only version of the 32C9301 which is 100% firmware and pinout compatible. The SSI 32C9020, SSI 32C9022 and SSI 32C9023 family members are SCSI disk controllers providing many of the same features as the SSI 323C9003. The SSI 32C9340 disk controller completes the family providing PCMCIA/ATA compliant interfaces. All members are based on a common architecture allowing major portions of firmware to be reused. The Silicon Systems' chip family is illustrated in hierarchy chart shown in Figure 1.

The high level of integration within the SSI 32C9003 represents a major reduction in parts count. When the SSI 32C9003 ATA Controller is combined with the SSI 32R2010 Read/Write device, the SSI 32P3000 Pulse Detector, the SSI 32D4040 Dual Bit Data Synchronizer with 1,7 ENDEC, the SSI 32H4631 Servo and Motor Speed Controller, an appropriate micro controller and memory a complete, cost efficient, high performance intelligent drive solution is created.

FEATURES (continued)

- **ATA Interface** (continued)
  - **Automatic updates of the host task file registers in both Cyl/Hd/Sec and LBA modes**
  - **Automatic Multi-Sector data transfers without microprocessor intervention**
  - **Automatic Host Interrupt and Busy for multiple sector transfers integrated with buffer streaming logic**
  - **16 byte FIFO to improve performance**
  - **Power management, including power down at I/O pins**
- **Buffer Manager**
  - **Direct support of DRAM or SRAM**
    - **SRAM: up to 256k bytes of memory with throughput to 20 megabytes per second**
    - **DRAM: up to 1 megabyte of memory with throughput to 17.78 megabytes per second**
  - **Programmable memory timing**
  - **Buffer RAM segmentation with flexible segment sizes from 256 bytes to 1 megabyte**
  - **Dedicated host, disk and microprocessor address pointers**
  - **Buffer Streaming with internal buffer protection circuit providing buffer integrity**
- **Disk Formatter**
  - **Dual Bit NRZ interface supporting data rates to 80 megabits per second**
  - **Automatic multi–sector transfer**
  - **Header or microprocessor based split data field support**
  - **Advanced sequencer organized in 31 x 5 bytes**
  - **88–bit Reed Solomon ECC with "on-the-fly" fast hardware correction circuitry**
  - **Capable of correcting up to four 10-bit symbols in error**
  - **Guaranteed to correct one 31-bit burst or two 11-bit bursts**
  - **Hardware on-the-fly correction of an 11-bit single burst error within a one half sector time**
  - **Detects up to one 51-bit burst or three 11-bit bursts**
- **Microprocessor Interface**
  - **Supports both multiplexed or non-multiplexed microprocessors**
  - **Separate or combined host and disk interrupts**
- **Other Features**
  - **Internal power down modes**
  - **Available in 120 and 128-Lead TQFP, and 128 QFP packages**

FUNCTIONAL DESCRIPTION

The SSI 32C9003 contains the following four major functional blocks:

Microprocessor Interface
ATA Interface
Disk Formatter
Buffer Manager

The Microprocessor Interface allows the local microprocessor access to all of the SSI 32C9003 internal control registers and any location within the buffer memory. The microprocessor, by writing and reading the internal registers, can control all activities of the SSI 32C9003. The microprocessor can elect to perform host and/or disk operations directly, or it can enable the advanced features of the SSI 32C9003 which can perform these operations automatically.

The ATA Interface block handles all PC AT bus activities. The ATA interface includes 24 mA drivers allowing for direct connection of the SSI 32C9003 to the PC AT bus. The ATA interface block is highly automated, capable of performing multiple block transfers without micro controller involvement. The ATA block interfaces directly with the Buffer Manager via an internal speed matching FIFO.

The Disk Formatter performs the serialization and deserialization of data. If provides all of the necessary functions to control track formatting, header search, and the reading and writing of data. The heart of the Disk Formatter is an advanced programmable sequencer. The sequencer can contain 31 instructions, each of which is 5 bytes (40 bits) in width. The width of the instructions allows for sophisticated branching techniques which increase the flexibility and power of the sequencer. The disk interface can be configured through a wide range of capabilities. This allows the SSI 32C9003 to interface with nearly any read/write channel and allows the user of the SSI 32C9003 to select the read/write channel best suited to the device. Of course, by selecting the SSI 32C9003 controller and the SSI 32D4040 Data Synchronizer with 1,7 ENDEC, you are guaranteed a problem free interface.

Within the Disk Formatter are the ECC generator/checker and ECC corrector. The generator/checker provides the ability to generate or check an enhanced 16 bit CRC for headers and an 88 bit Reed Solomon code for data. If the checker detects an error using the 88 bit Reed Solomon code, the syndrome information is transferred into the corrector. The corrector then performs the necessary operations to determine if the

(continued)

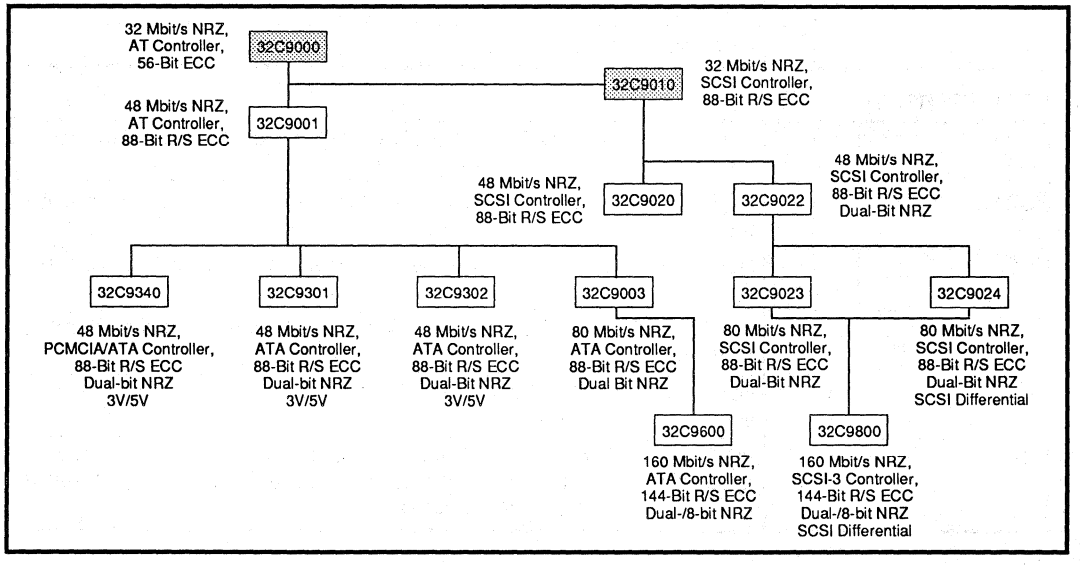

FIGURE 1: Silicon Systems' Disk Controller Chip Hierarchy

FUNCTIONAL DESCRIPTION (continued)

error was correctable and, if it was correctable, the corrector interfaces directly with the buffer controller and performs the correction automatically. The corrector performs its correction within one half of a sector. This guarantees that the corrector will always be available to correct the next sector if necessary.

The Buffer Manager can support either SRAM or DRAM. When configured to operate with DRAM, the Buffer Manager automatically performs necessary refresh cycles. The buffer manager creates all of the necessary timing and control signals for a wide range of memory types and speeds. Besides interfacing with the buffer memory, the Buffer Manager interfaces with the ATA Interface block, the Disk Formatter block, the ECC corrector and the microprocessor. If more than one of these devices requires access to the buffer memory, the Buffer Manager arbitrates the requests automatically.

PIN DESCRIPTION

The following convention is used in the pin description:

- (I) denotes an input
- (O) denotes an output
- (I/O) denotes a bidirectional signal
- (Z) denotes a tri-state output
- (OD) denotes an open drain output

Active low signals are denoted by a bar on top of the signal name and dual function pins are denoted with a slash between the two signals — $\overline{AMD}$/SECTOR

GENERAL

NAME	TYPE	DESCRIPTION
VDD		POWER SUPPLY PIN
GND		GROUND

HOST INTERFACE

A(2:0)	I	HOST ADDRESS LINES. The Host Address lines A(2:0) are used to access the various PC/AT control/status, and data registers.
$\overline{HCS1}$	I	HOST CHIP SELECT 1. This pin selects access to the control block task file registers.
$\overline{HCS0}$	I	HOST CHIP SELECT 0. This pin selects access to the command block task file registers.
$\overline{IOCS16}$	OD	16 BIT DATA TRANSFER. An open drain active low output that indicates that a 16-bit buffer transfer is active.
IRQ	O,Z	HOST INTERRUPT. Asserted active high to indicate to the Host that the controller needs attention.
IORDY	O,Z	I/O CHANNEL READY. This signal is asserted low to extend host transfer cycles when the controller is not ready to respond. This pin will be tristated when a read or write is not in progress.

HOST INTERFACE (continued)

NAME	TYPE	DESCRIPTION
DREQ	O,Z	DMA REQUEST. The active high DMA Request signal is used during DMA transfer between the Host and the controller.
$\overline{\text{DACK}}$	I	DMA ACKNOWLEDGE. This active low signal is used during DMA to complete the DMA handshake for data transfer between the host and the controller.
$\overline{\text{IOR}}$	I	I/O READ. This active low pin is asserted by the Host during a Host read operation. When asserted with $\overline{\text{HCS0}}$, $\overline{\text{HCS1}}$, or $\overline{\text{DACK}}$, data from the device is enabled onto the host data bus.
$\overline{\text{IOW}}$	I	I/O WRITE. Asserted active low by the HOST during a HOST write operation. When asserted with $\overline{\text{HCS0}}$, $\overline{\text{HCS1}}$, or $\overline{\text{DACK}}$, data from the host data bus is strobed into the device.
$\overline{\text{HRESET}}$	I	HOST RESET. This active low signal stops all commands in progress and initializes the control/status registers — This signal can also "wake up" the device while it is in power down mode.
HDB(15:0)	I/O	HOST DATA BUS. These bits are used for word transfers between the Buffer Memory and the Host; bits (7:0) are used for status, commands, or ECC byte transfers.
$\overline{\text{DASP}}$	I,OD	DRIVE ACTIVE/DRIVE 1 PRESENT. This is a time-multiplexed signal which indicates that a drive is active, or that Drive 1 is present.
$\overline{\text{PDIAG}}$	I,OD	PASSED DIAGNOSTICS. This signal is an output when configured as Drive 1 and an input when configured as Drive 0.

DISK INTERFACE

INDEX	I	INDEX. This input is a pulse that occurs once per revolution and defines the start of first sector.
OUTPUT	O	DISK SEQUENCER OUTPUT. This pin is controlled by bit 2 of the control field of the disk sequencer.
INPUT	I	INPUT. This signal is used to synchronize the disk sequencer to an external event.
$\overline{\text{AMD}}$/ SECTOR	I	ADDRESS MARK DETECT/SECTOR. This pin is configured to operate in Hard or Soft Sector mode by initializing the Disk Formatter Mode Control Register: 4FH, bit 1. In the hard sector mode it is used as the sector input — a pulse on this pin indicates a sector mark is found. In the soft sector mode, an active low input indicates an address mark was detected. The device powers up in soft sector mode.
RG	O	READ GATE. This active high output enables the reading of the disk. It is asserted at the beginning of the PLO for header and data field by the sequencer — sequencer Control Field bits 5 and 6. It is automatically deasserted at the end of the CRC or ECC.

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PIN DESCRIPTION (continued)

DISK INTERFACE

NAME	TYPE	DESCRIPTION
WG	O	WRITE GATE. This active high output enables writing onto the disk. It is asserted and deasserted by the sequencer Control Field bits 5 and 6.
RRCLK	I	READ REFERENCE CLOCK. This pin is used in conjunction with the NRZs pin to clock data in. It is also used as a clock for the disk sequencer and is used to generate WCLK.
WCLK	O	WRITECLOCK. This signal clocks the NRZ data out.
NRZ0, 1	I/O	NON RETURN TO ZERO. These signals are the read data input 0 and 1 from the disk drive when the read gate signal is asserted; it is the write data output to the disk drive when the write gate signal is asserted. NRZ1 is the most significant bit.
FAULT	I	Fault: Asserting this pin causes the disk sequencer to stop immediately.

MICROPROCESSOR INTERFACE

$\overline{RST}$	I	RESET. An asserted active low input generates a component reset that holds the internal registers of the controller at reset, stops all operations within the chip, and deasserts all output signals. All input/output signals and Host outputs are set to the high-Z state.
ALE	I	ADDRESS LATCH ENABLE/Multiplexed or Non-multiplexed address select: If this input is constantly low, the microprocessor interface is configured with non-multiplexed address and data busses. If this input is ever high, the microprocessor interface is configured with a multiplexed address and data bus. In this case, this pin functions as the address latch enable, and the latched address is output on the MA(7:0) pins.
CS	I	CHIP SELECT. This signal must be asserted high for all microprocessor accesses to the registers of this chip.
$\overline{WR}$/R/$\overline{W}$	I	WRITE STROBE/READ/WRITE. When the Intel bus control interface is selected, this signal acts as the $\overline{WR}$ signal. When the Write strobe signal is asserted low and the CS signal is asserted high, the data on the AD lines will be written to the register. When the Motorola bus control interface is selected, this signal acts as the R/$\overline{W}$ signal. A high on this input along with the $\overline{RD}$/$\overline{DS}$ signal asserted and the CS signal asserted high indicates a read operation. A low on this input along with the $\overline{RD}$/$\overline{DS}$ signal asserted and the CS signal asserted high indicates a write operation.

MICROPROCESSOR INTERFACE (continued)

NAME	TYPE	DESCRIPTION
$\overline{RD}/\overline{DS}$	I	READ STROBE/DATA STROBE. When the Intel bus control interface is selected, this signal acts as the $\overline{RD}$ signal. When the read strobe signal is asserted low and the CS signal is asserted high, the data from the specified register will be driven onto the AD signals. When the Motorola bus control interface is selected, this signal acts as the $\overline{DS}$ signal. A high on the R/$\overline{W}$ signal along with this signal asserted and the CS signal asserted high indicates a read operation. A low on the R/$\overline{W}$ signal along with this signal asserted and the CS signal asserted high indicates a write operation.
$\overline{DINT}/\overline{INT}$	O, OD	DISK INTERRUPT. This signal is an interrupt line to the microprocessor. It is the combined interrupt line of the disk side and host side interrupts when pin RDY/$\overline{HINT}$ is programmed as Ready; otherwise, it only signals the occurrence of disk side interrupt events. This signal is programmable for either a push-pull or open-drain output circuit. This signal powers up in the high-Z state.
AD(7:0)	I/O	ADDRESS/DATA BUS. When configured in the Multiplexed mode, these lines are multiplexed, bidirectional data path to the microprocessor. During the beginning of the memory cycle the bus captures the low order byte of the microprocessor address. These lines provide communication with the controller device's internal registers and the buffer memory. When configured in the Non-multiplexed mode, these lines are bidirectional data lines.
MA(7:0)	I/O	MICROPROCESSOR ADDRESS BUS: This 8-bit output bus is the AD(7:0) bus latched by the ALE pin during the low order address phase of a Multiplexed type microprocessor cycle. These signals are non-multiplexed address input when used with a Non-multiplexed microprocessor.
READY/$\overline{AINT}$	O, OD	READY/HOST SIDE INTERRUPT: When programmed as the Ready function, this signal is deasserted low for the microprocessor to insert wait states to allow time for the chip to respond to the access. When programmed as the host side interrupt, this pin interrupts the microprocessor when there is a host related interrupt event. The interrupt signal is programmable for either a push-pull or open-drain output circuit. This signal powers up as the 'Ready' function.

PIN DESCRIPTION (continued)

BUFFER MANAGER INTERFACE

BA(15:0)	O	BUFFER MEMORY ADDRESS LINES 15 through 0. These sixteen outputs provide address lines for the dynamic memory or static memory chips used to implement the buffer memory.
BA16/$\overline{RAS}$	O	BUFFER MEMORY ADDRESS 16: In SRAM mode, this pin generates the address: A16 for direct connection to a Static RAM address line 16. BUFFER ROW ADDRESS STROBE: This active low output signal is generated to strobe the row — high order — address into the dynamic RAMs. It is intended to be directly tied to the RAMs input control pin.
BA17/$\overline{CAS}$/$\overline{MS}$	O	BUFFER MEMORY ADDRESS 17/COLUMN ADDRESS STROBE/ MEMORY SELECT: This signal is used for addressing the buffer memory in SRAM mode or as the column address strobe in DRAM mode. When configured as $\overline{MS}$ this signal is active during both buffer memory reads and buffer memory writes. After $\overline{RST}$ is asserted, this signal will be high.
BD(7:0)	I/O	BUFFER MEMORY DATA BUS. 7 through 0. The bidirectional Data Bus connects directly to the buffer memory. This bus is designed for high speed data transfer.
BDP	I/O	BUFFER MEMORY PARITY: This bit is the parity value for BD(7:0).
$\overline{MOE}$/$\overline{MS}$	O	MEMORY OUTPUT ENABLE/MEMORY SELECT. When configured as $\overline{MOE}$, this signal is active during buffer memory reads. When configured as $\overline{MS}$, this signal is active during both buffer memory reads and buffer memory writes, The timing of the $\overline{MS}$ signal follows that of the address pins.
$\overline{WE}$	O	WRITE ENABLE. This active low output signal is used to strobe the data into the RAMs from the Data bus. For both buffer memory applications, this line is tied directly to the SRAM or DRAM control pin.
SYSCLK	I	SYSTEM CLOCK. This signal is used to synchronize the buffer RAM access, including the generation of memory address lines, write enable WE, and memory output enable MOE. In power down mode, this signal is shut off from the internal logic and hence buffer memory access is inhibited.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC operating characteristics.

PARAMETER	RATING
Power Supply Voltage, VCC	7V
Ambient Temperature	0 to 70°C
Storage Temperature	-65 to 150°C
Power Dissipation	750 mW
Input, Output pins	-0.5 to VCC+0.5V

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VDD Power Supply Voltage		4.5		5.5	V
IDD Supply Current				50	mA
IDDS Standby Current	Note 1			250	µA
VIL Input Low Voltage		-0.5		0.8	V
VIH Input High Voltage	Except $\overline{RST}$ pin	2.0		VCC+0.5	V
VIH Input High Voltage	$\overline{RST}$ pin	3.9		VCC+0.5	V
VOL Output Low Voltage	Note 2			0.4	V
VOL Output Low Voltage	Note 3			0.5	V
VOH Output High Voltage IOH = -400 µA		2.4			V
IL Input Leakage Current 0 < VIN < VCC		-10		10	µA
CIN Input Capacitance				10	pF
COUT Output Capacitance				10	pF

Note: (1) Synchronization and Clock Control Register, 7FH: bits 3 and 4 set. RRCLK and SYSCLK internally inhibited.

(2) All interface pins except Host Interface pins. IOL= 2 mA.

(3) Host Interface pins, IOL = 24 mA.

MICROPROCESSOR INTERFACE TIMING PARAMETERS

Multiplexed Bus Interface Timings (Figures 2, 3, 4, 5)

Ta	ALE Width		20			ns
Tma	Address valid to MA (7:0) valid				30	ns
Tr	$\overline{RD}$ Width		80			ns
As	Address valid to ALE ↓		5			ns
Ah	ALE ↓ to address invalid		10			ns
Cs	CS valid to $\overline{RD}$ ↓ or $\overline{DS}$ ↓		20			ns
Ch	$\overline{RD}$ ↑ or $\overline{DS}$ ↑ to CS ↓		0			ns
Tda	$\overline{RD}$ ↓ or $\overline{DS}$ ↓ to read data valid	Except Read of WCS			30	ns
Tda	$\overline{RD}$ ↓ or $\overline{DS}$ ↓ to read data valid	Read of WCS			50	ns
Tds	$\overline{DS}$ width		80			ns
Tdh	$\overline{RD}$ ↑ to or $\overline{DS}$ ↑ read data invalid		0		25	ns
Tsrw	R/$\overline{W}$ valid to $\overline{DS}$ ↓		20			ns
Thrw	$\overline{DS}$ ↑ to R/W invalid		20			ns
Tdrdy	$\overline{RD}$ ↓ to READY ↓ (Intel) or $\overline{DS}$ ↓ to READY ↓ (Motorola)				30	ns
Wds	Write data valid to $\overline{WR}$ ↑ or $\overline{DS}$ ↑		40			ns
Wdh	$\overline{WR}$ ↑ or $\overline{DS}$ ↑ to write data invalid		10			ns

ELECTRICAL SPECIFICATIONS (continued)

Non-Multiplexed Bus Interface Timings (Figure 6)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Tmas	MA (7:0) valid to $\overline{DS}$ ↓		5			ns
Tmah	$\overline{DS}$ ↑ to MA (7:0) invalid		5			ns
Cs	CS valid to $\overline{DS}$ ↓		20			ns
Ch	$\overline{DS}$ ↑ to CS ↓		0			ns
Tda	$\overline{DS}$ ↑ to read data valid	Except Read of WCS			30	ns
Tda	RD ↓ or $\overline{DS}$ ↑ to read data valid	Read of WCS			50	ns
Tds	DS width		80			ns
Tdh	DS ↑ to read data invalid		0		25	ns
Tsrw	$\overline{R/W}$ valid to $\overline{DS}$ ↓		20			ns
Thrw	$\overline{DS}$ ↑ to $\overline{R/W}$ invalid		20			ns
Tdrdy	$\overline{DS}$ ↓ to READY ↓ (Motorola)				30	ns
Wds	Write data valid to $\overline{WR}$ ↑ or $\overline{DS}$ ↑		40			ns
Wdh	$\overline{WR}$ ↑ or $\overline{DS}$ ↑ to write data invalid		10			ns

Note: (1) Loading capacitor = 30 pF
(2) ↑ indicates rising edge ↓ indicates falling edge

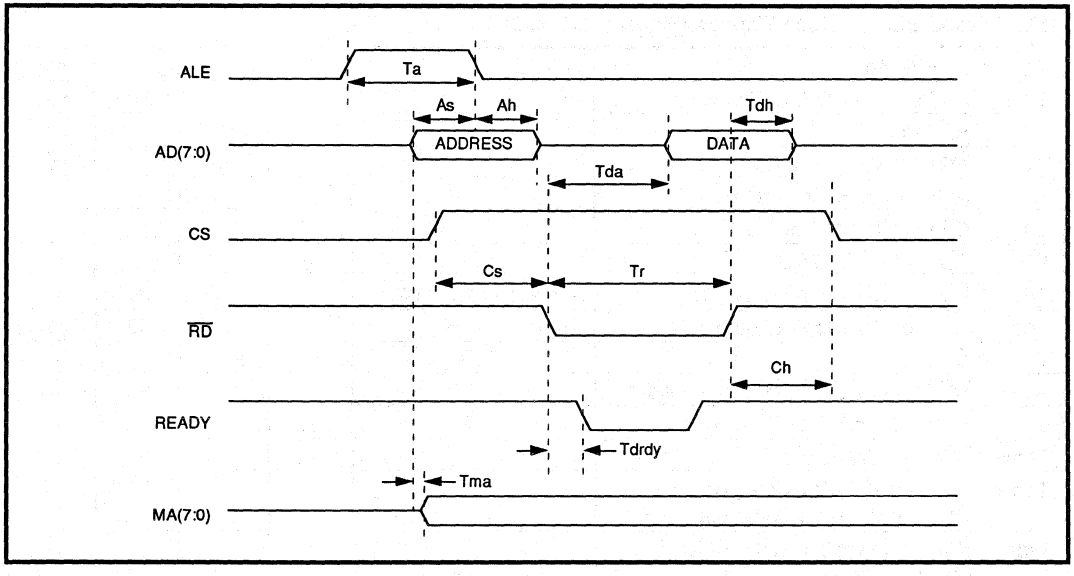

FIGURE 2: Intel Register Multiplexed Read Timing

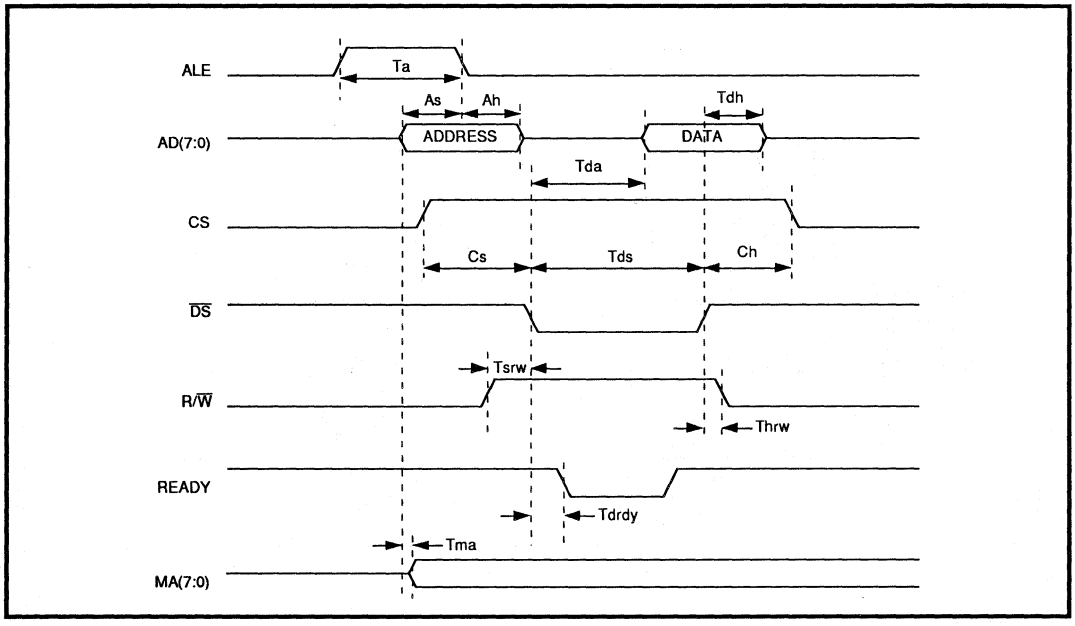

FIGURE 3: Motorola Register Multiplexed Read Timing

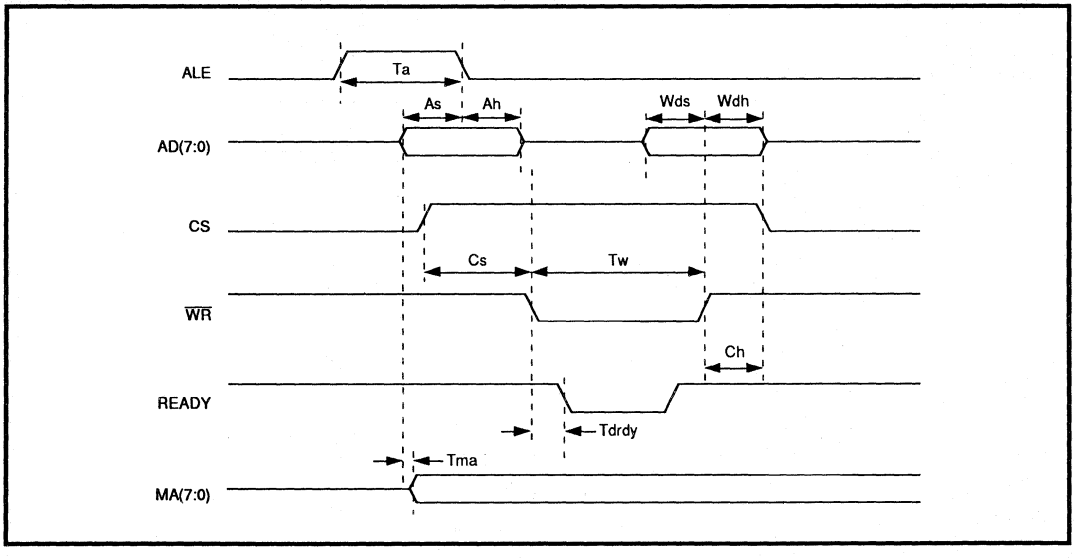

FIGURE 4: Intel Register Multiplexed Write Timing

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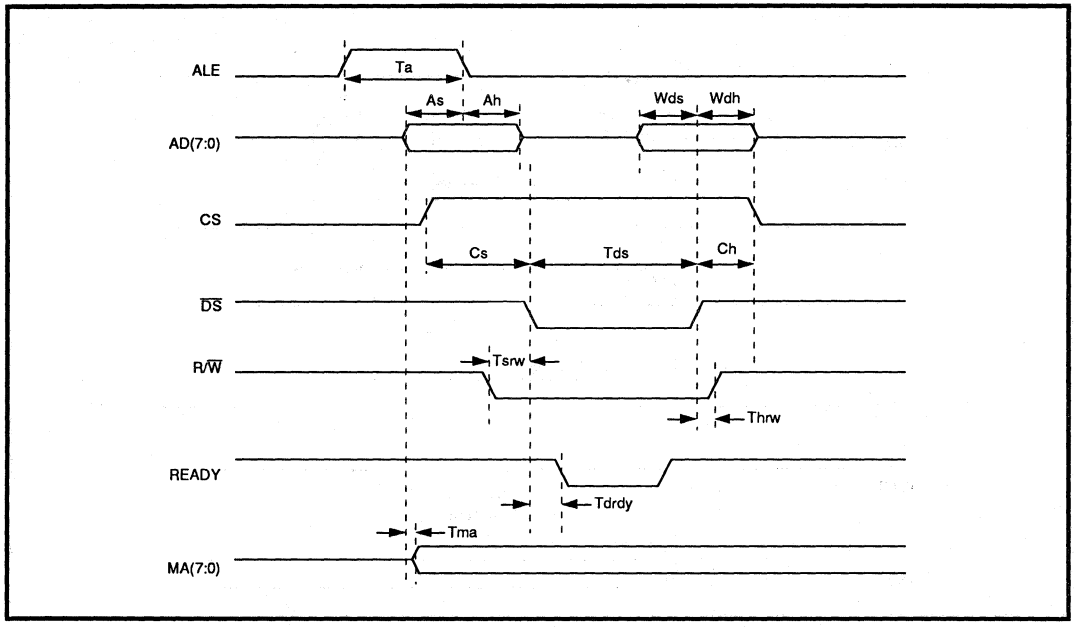


FIGURE 5: Motorola Register Multiplexed Write Timing

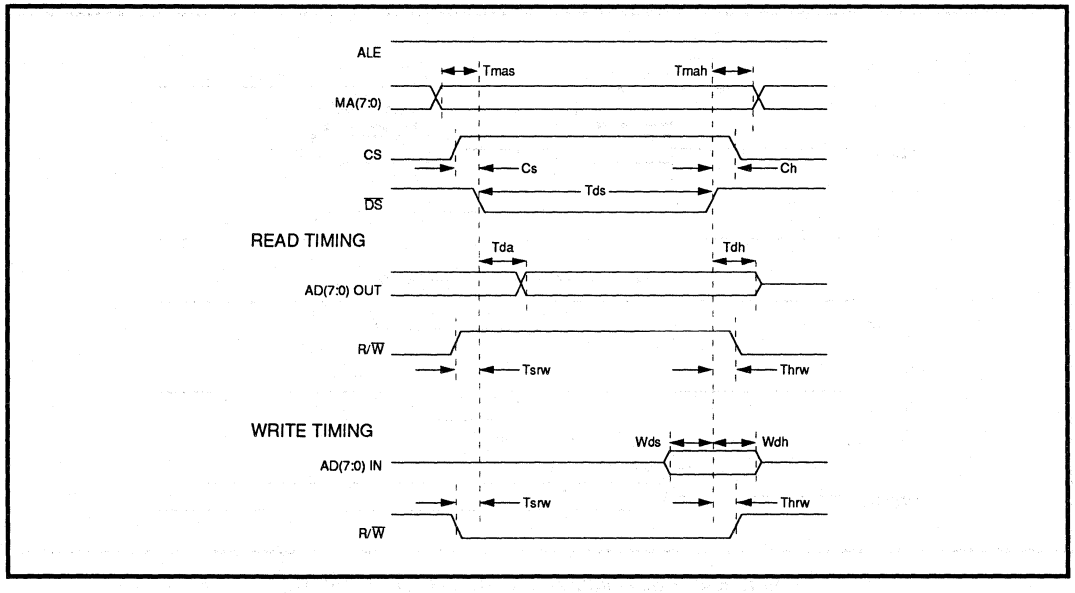


FIGURE 6: Non-Multiplexed Bus Timing Diagrams

ELECTRICAL SPECIFICATIONS (continued)

Disk Read/Write Timing (Figure 7)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Trrc	RRCLK period (dual bit)		27.8			ns
Trrc	RRCLK period (single bit)		20.8			ns
Trrcl	RRCLK low time (dual bit)		11.1			ns
Trrcl	RRCLK low time (single bit)		8.5			ns
Trrch	RRCLK high time (dual bit)		11.1			ns
Trrch	RRCLK high time (single bit)		8.5			ns
Dis	NRZ in valid to RRCLK high		3			ns
Dih	RRCLK high to NRZ in invalid		3			ns
As	$\overline{AMD}$ valid to RRCLK high (soft sector only)		3			ns
Dv	RRCLK high to NRZ1, NRZ0 out valid				18	ns
Dvw	WCLK low to NRZ1, NRZ0 out valid		-3		+3	ns
Trwl	RRCLK high to WCLK low				18	ns
Trwh	RRCLK low to WCLK high				18	ns
Twckh	WCLK high time (dual bit)		8.3			ns
Twckh	WCLK high time (single bit)		6.3			ns
Twckl	WCLK low time (dual bit)		8.3			ns
Twckl	WCLK low time (single bit)		6.3			ns
Note: Loading capacitance = 10 pF						

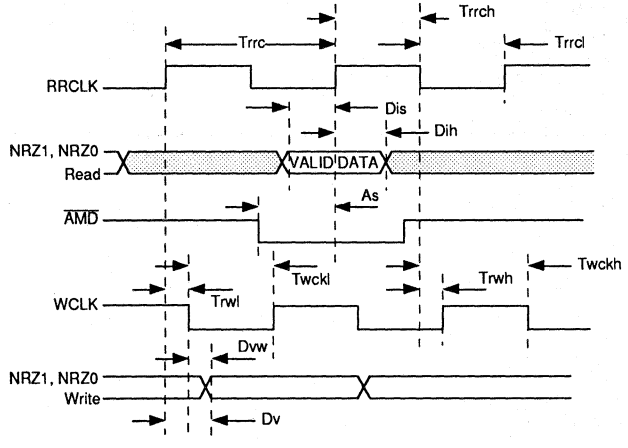


FIGURE 7: Disk Interface Timing

ELECTRICAL SPECIFICATIONS (continued)

BUFFER MEMORY READ/WRITE TIMING PARAMETERS (Figures 8 through 14)

PARAMETER		MIN	NOM	MAX	UNIT
T	SYSCLK period	25			ns
T/2	SYSCLK high/low time	10			ns
Tav	SYSCLK ↑ to address valid (Note 1)			18	ns
Tmsv	SYSCLK ↑ to $\overline{MS}$ ↓ (Notes 1, 6)			18	ns
Tmsh	SYSCLK ↑ to $\overline{MS}$ ↓ (Note 1)			18	ns
Tmv	SYSCLK ↑ to $\overline{MOE}$ ↓ (Note 1)			18	ns
Tmh	SYSCLK ↑ to $\overline{MOE}$ ↓ (Note 1)			18	ns
Twv	SYSCLK ↑ to $\overline{WE}$ ↓ (Note 1)			18	ns
Twh	SYSCLK ↑ to $\overline{WE}$ ↓ (Note 1)			18	ns
Tdov	SYSCLK ↑ to data out valid (Note 1)			18	ns
Tdoh	SYSCLK ↑ to data out invalid (Note 1)			18	ns
Tdis	Data in valid to $\overline{MOE}$ ↑ (SRAM) Data in valid to $\overline{CAS}$ ↑ (DRAM)	5			ns
Tdih	$\overline{MOE}$ ↑ to data in valid (SRAM) $\overline{CAS}$ ↑ to data in valid (DRAM)	0			ns
Trv	SYSCLK ↑ to $\overline{RAS}$ ↓ (Note 1)			18	ns
Trh	SYSCLK ↑ to $\overline{RAS}$ ↑ (Note 1)			18	ns
Trav	SYSCLK ↑ to row address valid (Note 1)			18	ns
Trah	SYSCLK ↑ to row address invalid (Note 1)			18	ns
Tcv	SYSCLK ↑ to $\overline{CAS}$ ↓ (Note 1)			18	ns
Tch	SYSCLK ↑ to $\overline{CAS}$ ↑ (Note 1)			18	ns
Tcav	SYSCLK ↑ to column address valid (Note 1)			18	ns
Tcah	SYSCLK ↑ to column address invalid	0			ns

BUFFER MEMORY READ/WRITE FUNCTIONAL PARAMETERS (Figures 8 through 14) (continued)

PARAMETER		CONDITIONS	TYPICAL	UNIT
Trwl	$\overline{RAS}\downarrow$ to $\overline{RAS}\uparrow$	Notes 2, 3	(RWL + 3)•T	ns
Trwh	$\overline{RAS}\uparrow$ to $\overline{RAS}\downarrow$	Notes 2, 4	(RWH + 1)•T	ns
Tcwl	$\overline{CAS}\downarrow$ to $\overline{CAS}\uparrow$	Note 2	(CWL + 1)•T	ns
Tcwh	$\overline{CAS}\uparrow$ to $\overline{CAS}\downarrow$	Notes 2, 5	(CWL + 1)•T	ns

Notes: Loading capacitance = 30 pF

Note 1: The measured delay for any of the signal indicated by this note will not vary from the measured delay of any other signal indicated by this note by more than ±2 ns.

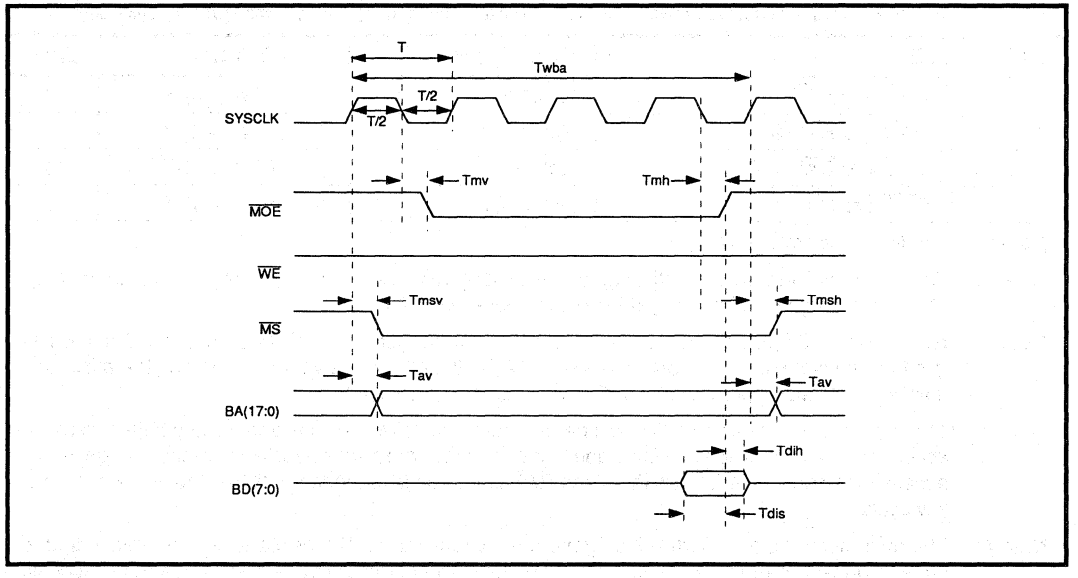
Note 2: RWL, RWH, CWL and CWH are fields in the Buffer Manager Timing Control Register (54H). Each is a two bit field which can contain a value of 0, 1, 2, or 3. These values determine the minimum number of SYSCLK periods (T) for the associated signal width.

Note 3: The minimum width value of Trwl will be generated for refresh cycles and for any buffer memory access cycle except when multiple page mode accesses are performed. When multiple page mode accesses are performed, the width of the $\overline{RAS}$ low pulse is extended until the end of the last $\overline{CAS}$ low cycle.

Note 4: The minumum value of Trwh will be generated whenever the Buffer Manager determines that a buffer request is pending at the completion of the current memory cycle and a page mode access can not be used because the needed location is not within the current page, or a new memory request is being processed.

Note 5: The minumum value of Tcwh will be generated only between consecutive page mode accesses.

Note 6: $\overline{MS}$ will rise only if the Buffer Manager determines that no additional requests for buffer access are pending. If the Buffer Manager determines that another access is to be made, $\overline{MS}$ is kept low between the accesses for improved speed.



Note: Twba is a functional parameter that gives the duration of one RAM data buffer access cycle in SYSCLK periods. The value is programmed in bits 1-0 of register 54H. These examples show Twba = 4T.

FIGURE 8: SRAM Read Timing

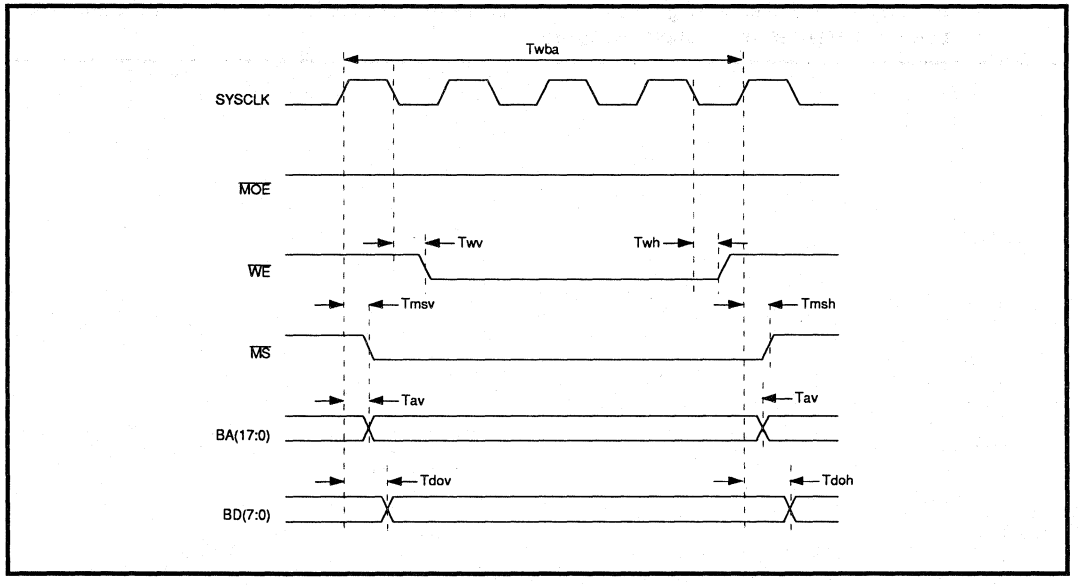


FIGURE 9: SRAM Write Timing

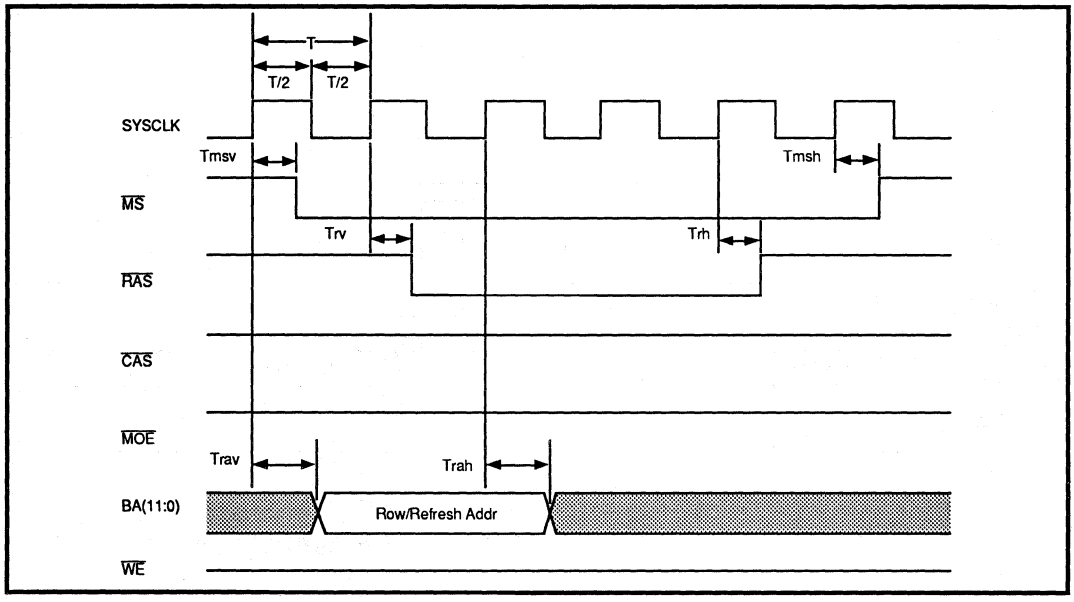


FIGURE 10: DRAM Timing, Refresh Cycle (Shown with WRL = 0)

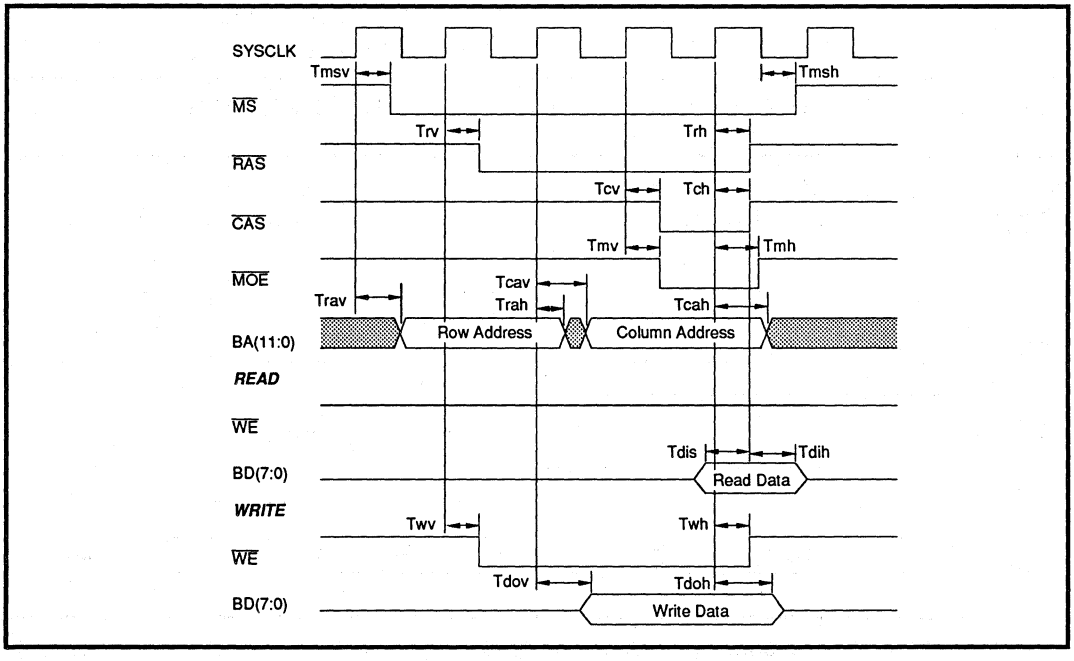


FIGURE 11: DRAM Timing, Standard Cycle (Shown with RWL = 0 and CWL = 0)

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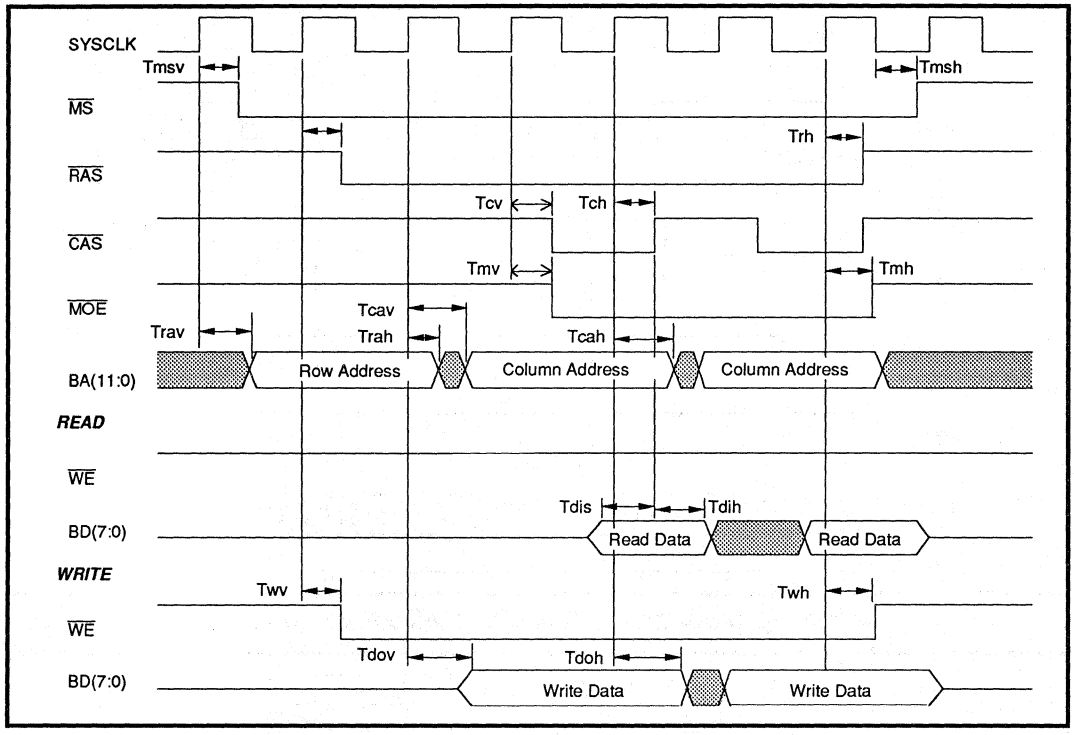

FIGURE 12: DRAM Timing, Fast Page Cycles (Shown with RWL = 0, RWH = 0, CWL = 0 and CWH = 0)

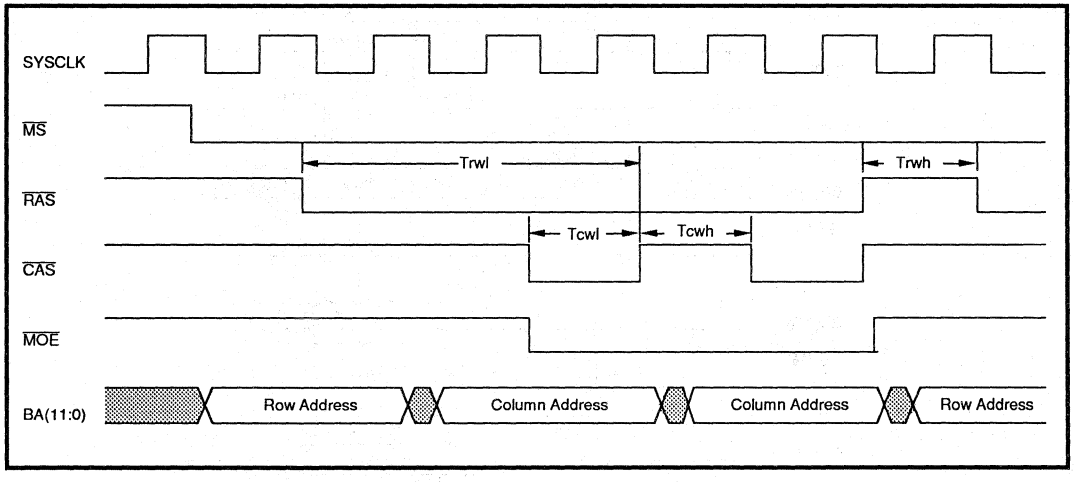

FIGURE 13: DRAM Timing (Showing the Relationship of RWL, RWH, CWL and CWH to overall timing)

ELECTRICAL SPECIFICATIONS (continued)

AT Host Interface Timing Parameters

PARAMETER		MIN	NOM	MAX	UNIT
DREQL	$\overline{DACK}$ ↓ to DREQ ↓			40	ns
DREQD	$\overline{IOR}$ ↓ or $\overline{IOW}$ ↓ to DREQ ↓			40	ns
RDTA	$\overline{IOR}$ ↓ to HD(15:0) valid			50	ns
DMASET	$\overline{DACK}$ ↓ to $\overline{IOW}$ ↓ or $\overline{IOR}$ ↓	0			ns
DMAHLD	$\overline{IOR}$ ↑ or $\overline{IOW}$ ↑ to $\overline{DACK}$ ↑	0			ns
RDHLD	$\overline{IOR}$ ↑ to HD (15:0) hi-Z	2		20	ns
WDS	HD(15:0) setup to $\overline{IOW}$ ↑	30			ns
WDHLD	HD(15:0) hold from $\overline{IOW}$ ↑	10			ns
RWPULSE	$\overline{IOR}$ or $\overline{IOW}$ low pulse width	80			ns
RWH	$\overline{IOR}$ or $\overline{IOW}$ high pulse width	50			ns
CS16L	$\overline{HCS0}$ ↓, A(2:0) ↓, A9 ↓ or $\overline{HCS1}$ ↑ to $\overline{IOCS16}$ ↓			20	ns
IOCHL	$\overline{IOR}$ or $\overline{IOW}$ ↓ to $\overline{IOCHRDY}$ ↓			25	ns
ADRSET	$\overline{HCS0}$, A(2:0), A9/$\overline{HCS1}$ setup to $\overline{IOR}$ ↓ or $\overline{IOW}$ ↓	25			ns
ADRHLD	$\overline{HCS0}$, A(2:0), A9/$\overline{HCS1}$ hold from $\overline{IOR}$ ↑ or $\overline{IOW}$ ↑	5			ns
Note: Loading capacitance = 30 pF					

Functional Specification

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
IOCHTW	$\overline{IOCHRDY}$ pulse width		0		5xBCLK	ns

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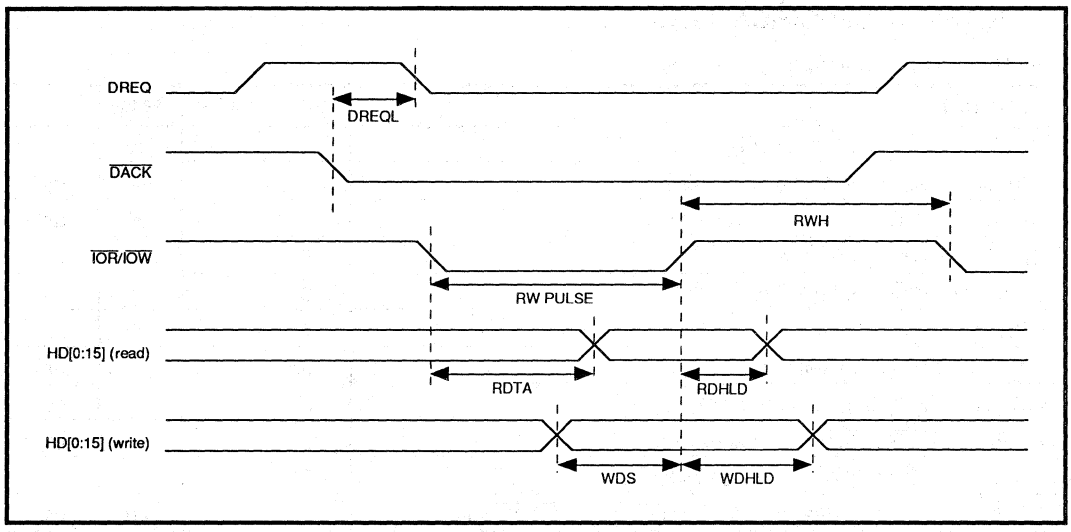


FIGURE 14: Host DMA 8-16 Bit Interface Timing (Non-demand mode)

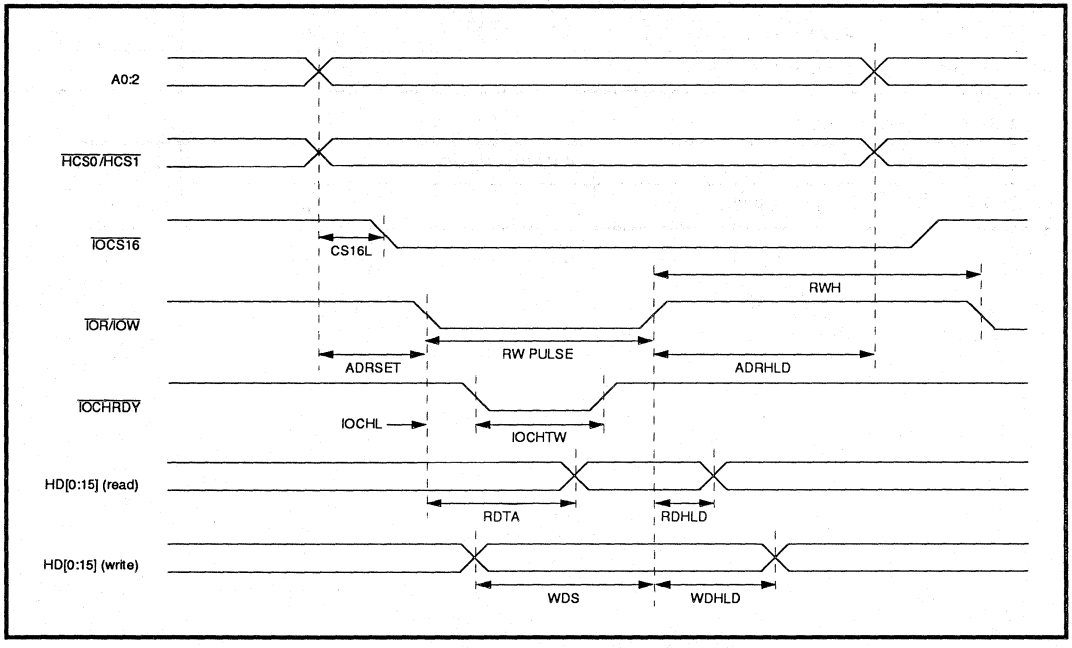


FIGURE 15: Host Programmed I/O 8-16 Bit Timing

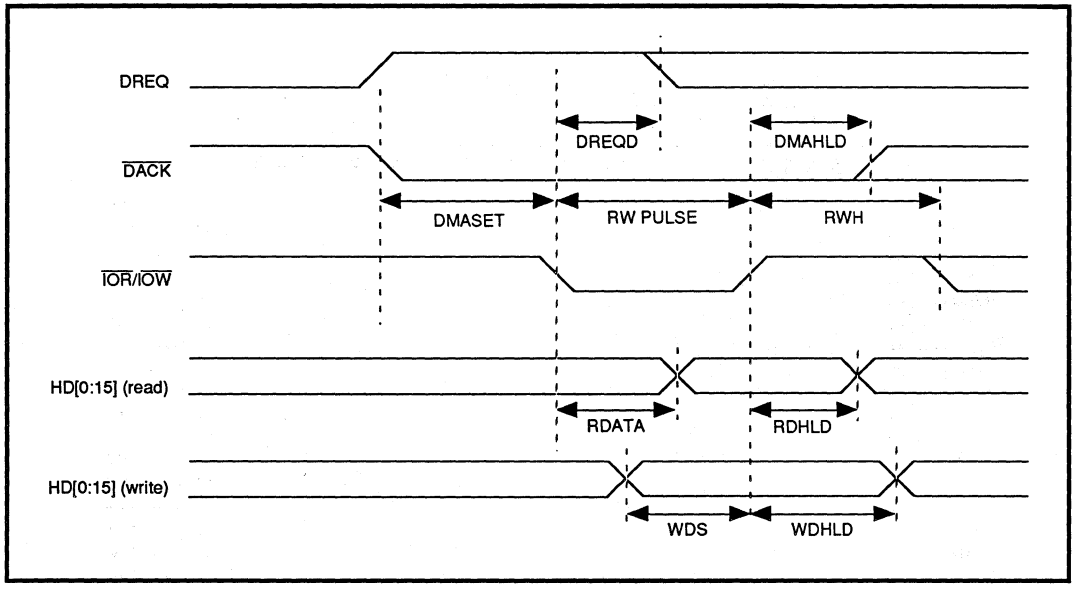


FIGURE 16: Host DMA 8/16-Bit Interface Timing (Demand Mode)

ELECTRICAL SPECIFICATIONS (continued)

RESET Assertion Timing Parameters (Figure 17)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Trpwl	$\overline{RST}$ pulse width low	NOT Power On Reset	500			ns
		Power On Reset	7.5			µs

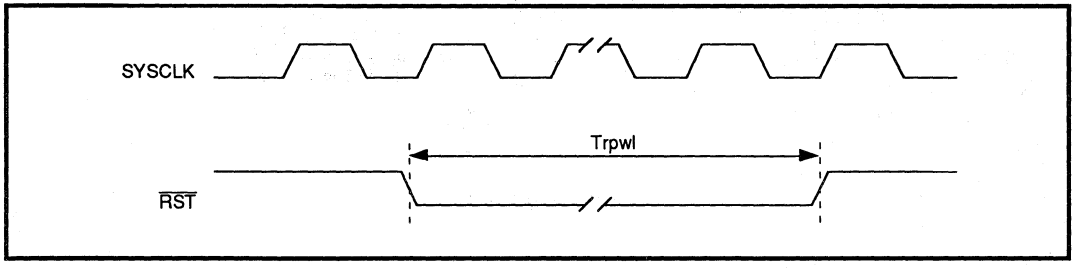
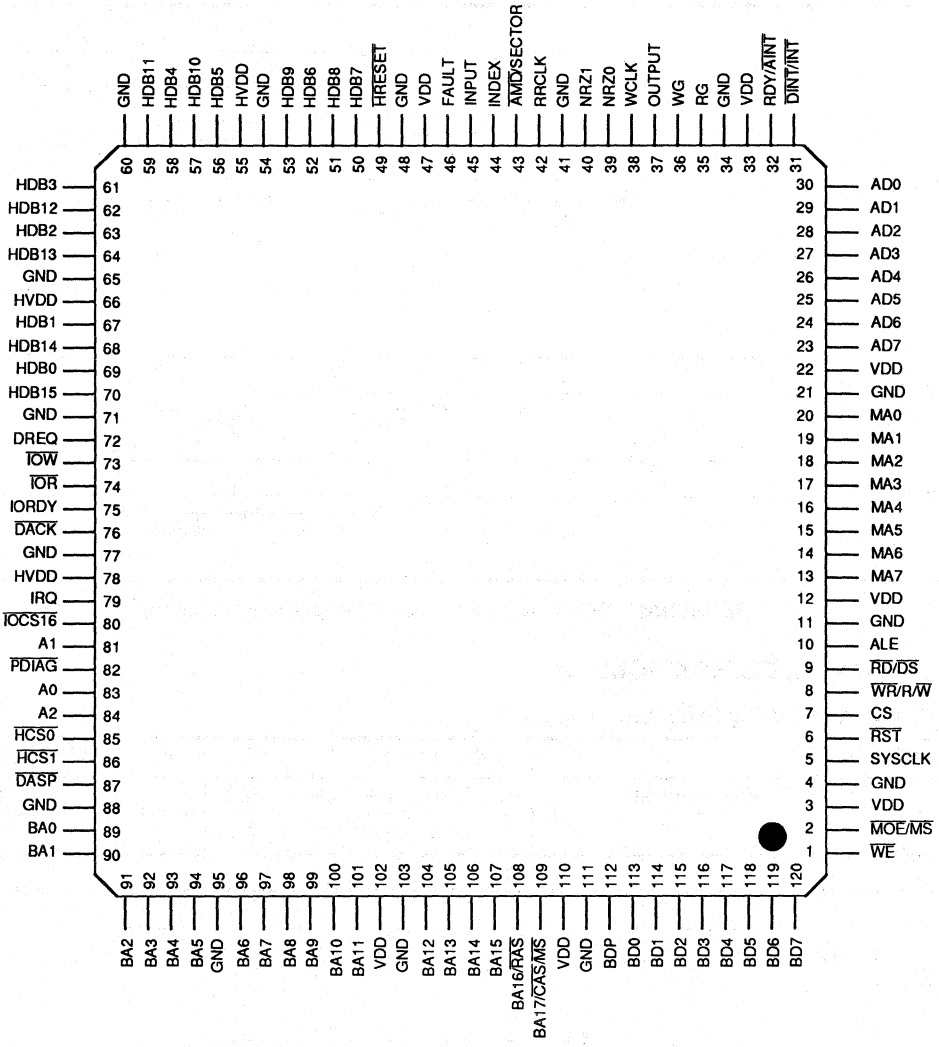


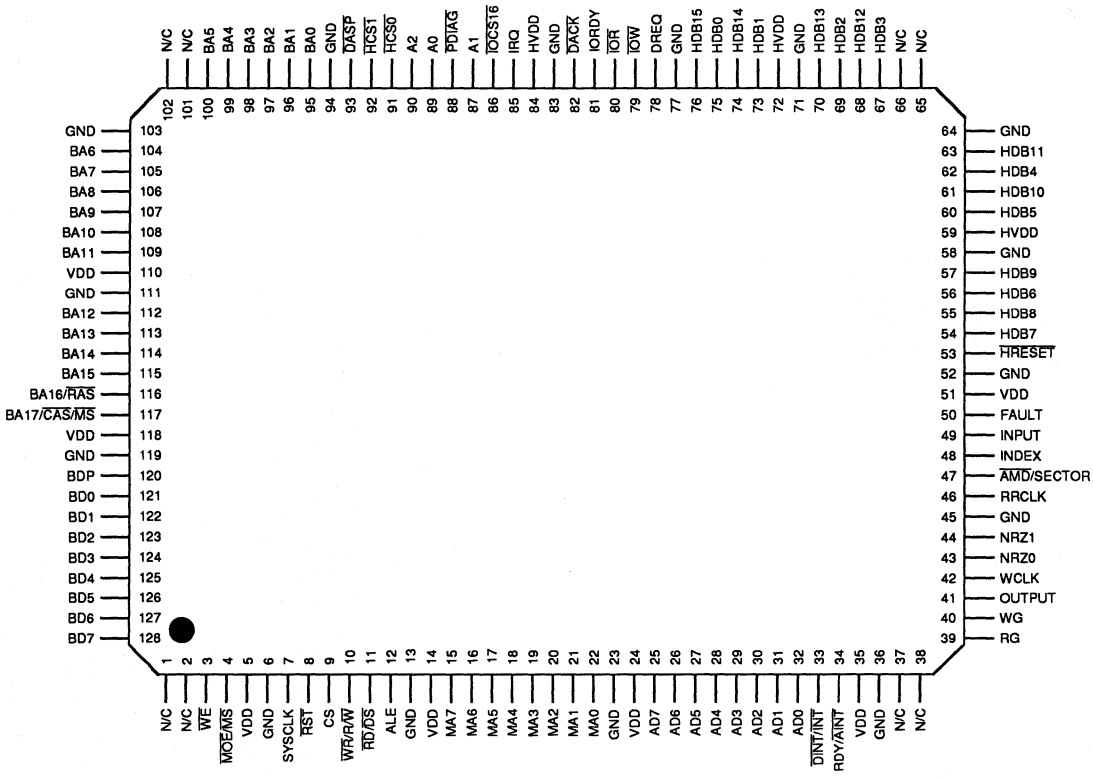
FIGURE 17: RESET Assertion Timing

SSI 32C9003
PC-AT Combo Controller
80 Mbit/s, Dual Bit NRZ Interface



120-Lead TQFP

CAUTION: Use handling procedures necessary for a static sensitive component.



128-Lead TQFP

CAUTION: Use handling procedures necessary for a static sensitive component.

9

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
120-Lead TQFP	SSI 32C9003-CGT2	SSI 32C9003-CGT2
128-Lead TQFP	SSI 32C9003-CGT	SSI 32C9003-CGT
128-Lead QFP	SSI 32C9003-CG	SSI 32C9003-CG

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX: (714) 573-6914

Notes:

silicon systems®
A TDK Group Company

SSI 32C9020
SCSI Combo Controller
48 Mbit/s; single bit NRZ interface

Advance Information

January 1994

DESCRIPTION

The SSI 32C9020 is an advanced CMOS VLSI device which integrates major portions of the hardware needed to build an SCSI disk drive. The circuitry of the SSI 32C9020 includes a complete SCSI target interface, an advanced buffer manager, a high performance disk formatter and an 88-bit Reed-Solomon ECC with fast "on-the-fly" hardware correction. The SSI 32C9020 provides maximum performance while minimizing micro controller intervention.

The SSI 32C9020 is capable of concurrent transfers of up to 48 megabits per second on the disk interface and 10 megabytes per second across the SCSI bus. In addition, on-the-fly error corrections and micro controller accesses to the buffer memory will not degrade the throughput during transfers.

The SSI 32C9020 is one of a family of Silicon Systems' single chip disk controllers which support a wide range

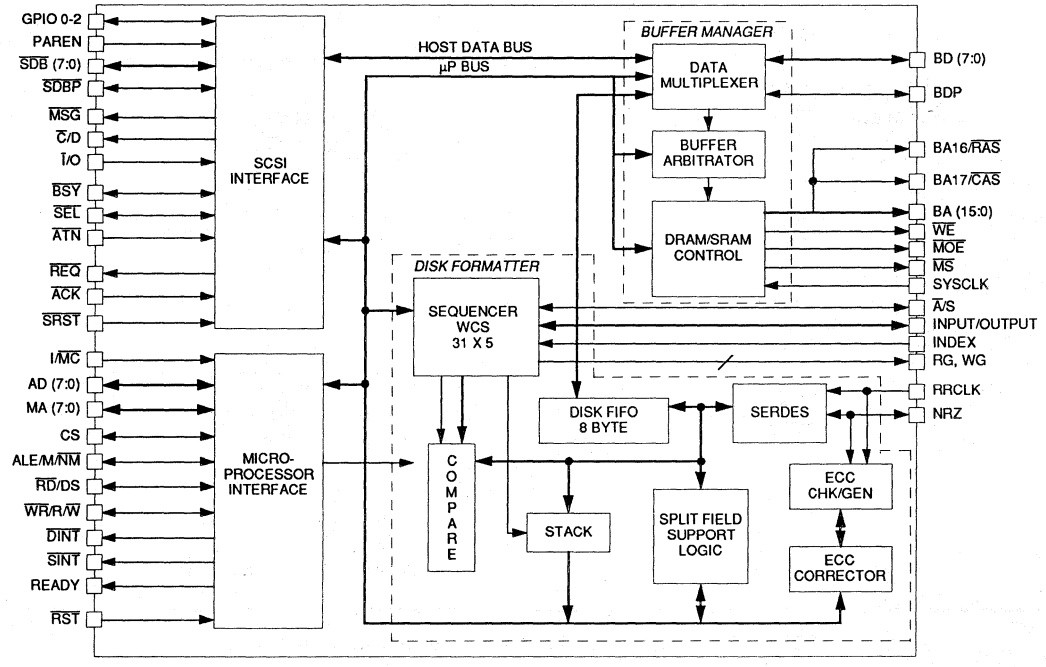
(continued)

FEATURES

- **SCSI Bus Interface**
  - **Full SCSI-2 Compatibility**
  - **Direct bus interface logic with on-chip 48 mA drivers**
  - **Synchronous transfer rates up to 10 megabytes per second**
  - **Asynchronous transfer rates up to 5 megabytes per second**
  - **Parity generation and checking**
  - **Auto Command Mode (ACM) SCSI state machine performs high level SCSI sequences without microprocessor intervention**
  - **Four level ACM command FIFO supports automatic execution of multiple ACM commands**

(continued)

BLOCK DIAGRAM



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SSI 32C9020
SCSI Combo Controller
48 Mbit/s; single bit NRZ interface

DESCRIPTION (continued)

of device interfaces. The SSI 32C9022 provides the same basic capabilities as the SSI 32C9020 but has a dual NRZ disk interface. Other family members support AT and PCMCIA interfaces. All members are based on a common architecture allowing major portions of firmware to be reused. The Silicon Systems' chip family is illustrated in the hierarchy chart shown in Figure 1.

The high level of integration within the SSI 32C9020 represents a major reduction in parts count. When the SSI 32C9020 SCSI Controller is combined with the SSI 32R2010 Read/Write device, the SSI 32P3000 Pulse Detector, the SSI 32D5391 Data Synchronizer with 1,7 ENDEC, the 32H4631 Servo and Motor Speed Controller, an appropriate micro controller and memory, a complete, cost efficient, high performance intelligent drive solution is created.

FEATURES (continued)

- Hardware support for automatic handling of SCSI-2 command queuing
- Automatic SCSI CDB size determination
- Automatic SCSI Disconnect and Reconnect
- Sixteen byte data FIFO between SCSI channel and Buffer Manager
- Buffer Manager
  - Direct support of DRAM or SRAM
  - SRAM throughput to 20 megabytes per second
  - SRAM size up to 256k bytes
  - DRAM throughput to 17.78 megabytes per second
  - DRAM size up to 1 megabyte
  - Programmable memory timing
  - Buffer RAM segmentation with flexible segment sizes from 256 bytes to 1 megabyte
  - Dedicated host, disk and microprocessor address pointers
  - Internal buffer protection circuit provides buffer integrity
- Disk Formatter
  - NRZ Data Rates to 48 megabits/s
  - Automatic multi-sector transfer
  - Header or microprocessor based split data field support
  - Advanced sequencer organized in 31 x 5 bytes
  - 88-bit Reed Solomon ECC with "on-the-fly" fast hardware correction circuitry

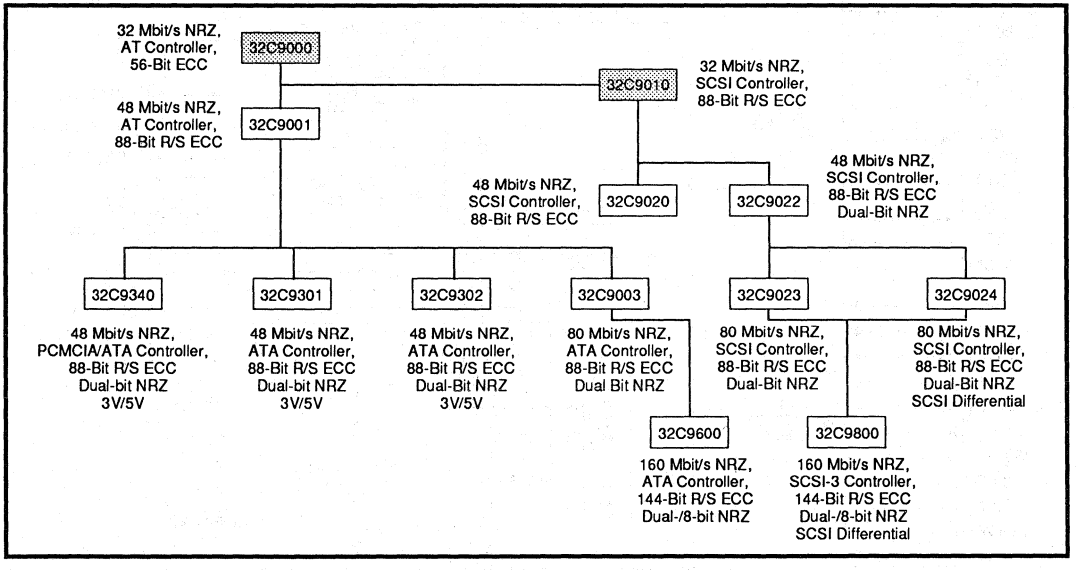


FIGURE 1: Silicon Systems' Disk Controller Chip Hierarchy

  - Capable of correcting up to four 10-bit symbols in error
  - Guaranteed to correct one 31-bit burst or two 11-bit bursts
  - Hardware on-the-fly correction of either an 11- or 31-bit single burst error within a half sector time
  - Detects up to one 51-bit burst or three 11-bit bursts
- Microprocessor Interface
  - Supports both multiplexed or non-multiplexed microprocessors
  - Separate or combined host and disk interrupts
  - Programmable wait state insertion
- Other Features
  - Internal power down mode
  - Available in 100-pin QFP

FUNCTIONAL DESCRIPTION

The SSI 32C9020 contains the following four major functional blocks:

Microprocessor Interface

SCSI Interface

Disk Formatter

Buffer Manager

The Microprocessor Interface allows the local microprocessor access to all of the SSI 32C9020 internal control registers and any location within the buffer memory. The microprocessor, by writing and reading the internal registers can control all activities of the SSI 32C9020. The microprocessor can elect to perform SCSI and/or disk operations directly, or it can enable the advanced features of the SSI 32C9020 which can perform all typical operations automatically.

The SCSI Interface block handles all SCSI activities. The SCSI interface includes 48 mA drivers allowing for direct connection of the SSI 32C9020 to the SCSI bus. The SCSI interface logic includes Auto Command Mode (ACM) logic, an advanced state machine capable of handling a variety of complex SCSI sequences without microprocessor intervention. The microprocessor can queue up to four ACM commands into the ACM Command FIFO to create even more sophisticated command sequences. The SCSI block interfaces directly with the Buffer Manager via an internal speed matching FIFO. This FIFO, plus the bandwidth capabilities of the Buffer Manager guarantee sustained full speed transfers across the SCSI bus. The high level of automation of the ACM minimizes SCSI bus overhead. The net result is maximized performance with minimum SCSI bus band width utilization.

The Disk Formatter performs the serialization and deserialization of data. It provides all of the necessary functions to control track formatting, header search, and the reading and writing of data. The heart of the Disk Formatter is an advanced programmable sequencer which is flexible enough to interface to a wide variety of read/write channels. The sequencer can contain 31 instructions, each of which is 5 bytes (40 bits) in width. The width of the instructions allows for sophisticated branching techniques which increase the flexibility and power of the sequencer. The flexible disk interface can be configured through a wide range of capabilities. This allows the SSI 32C9020 to interface with nearly any read/write channel and allows the user of the SSI 32C9020 to select the read/write channel best suited to the device. Of course, by selecting the SSI 32C9020 controller and the SSI 32D5391 Data Synchronizer with 1,7 ENDEC, you are guaranteed a problem free interface.

Within the Disk Formatter are the ECC generator/checker and ECC corrector. The generator/checker provides the ability to generate or check a 32-bit ECC for headers and an 88-bit Reed Solomon code for data. If the checker detects an error in an 88-bit Reed Solomon data field, the syndrome information is transferred into the corrector. The corrector performs the necessary operations to determine if the error was correctable and interfaces directly with the buffer controller to perform the correction automatically. The corrector performs its correction within one half of a sector time. This guarantees that the corrector will always be available to correct the next sector if necessary.

As its name implies, the Buffer Manager manages the data buffer of the controller. The Buffer Manager can support either SRAM or DRAM. When configured to operate with DRAM, the Buffer Manager automatically performs necessary refresh cycles. The buffer manager creates all of the necessary timing and control signals for a wide range of memory types and speeds. The Buffer Manager interfaces with the buffer memory, the SCSI Interface block, the data path of the Disk Formatter block, the ECC corrector and the microprocessor. If more than one of these devices

requires access to the buffer memory, the Buffer Manager arbitrates the requests automatically. The Buffer Manager of the SSI 32C9020 can sustain SCSI operations at the rate of 10 megabytes per second, Disk Formatter operations at 48 megabits per second (6 megabytes per second) and still have sufficient band width left to handle on-the-fly ECC corrections and microprocessor accesses without degrading performance on any of the interfaces.

PIN DESCRIPTION

The following convention is used in the pin description:

- (I) denotes an input
- (O) denotes an output
- (Z) denotes a tri-state output
- (OD) denotes an open drain output

GENERAL

NAME	TYPE	DESCRIPTION
VDD		POWER SUPPLY PIN, VCC
GND		GROUND

HOST INTERFACE

$\overline{SDBP}$	I/O	SCSI DATA BUS PARITY. Odd parity bit for the SCSI data bus.
$\overline{SDB(7:0)}$	I/O	SCSI DATA BUS BITS 7-0.
$\overline{ATN}$	I	ATTENTION. This active low signal is used by the initiator to request a message out phase.
$\overline{BSY}$	I/O	BUSY. This active low signal is used to indicate when the bus is active.
$\overline{ACK}$	I	ACKNOWLEDGE. This active low signal is used in the handshake protocol to indicate the completion of a data byte transfer.
$\overline{SRST}$	I	SCSI RESET. This active low signal is used to reset the SCSI controller.
$\overline{MSG}$	O	MESSAGE. This active low signal is used to indicate a message phase.
$\overline{SEL}$	I/O	SELECT. This active low signal is used to indicate either a selection or reselection phase.
$\overline{C}$/D	O	COMMAND/DATA. This signal is used to indicate either a command or data phase.
$\overline{REQ}$	I	REQUEST. This active low signal is used in the handshake protocol to initiate a data byte transfer.
$\overline{I}$/O	I	INPUT/OUTPUT. This signal is used to indicate the direction of data transfer.
PAREN	I	SCSI PARITY ENABLE. This active high signal is used to enable parity checking of the SCSI data bus. Parity checking is disabled when this pin is held low.

DISK INTERFACE

NAME	TYPE	DESCRIPTION
GPIO(2:0)	I/O	INPUT/OUTPUT. These pins are used to indicate the SCSI ID of the target device. The pins can be programmed as outputs for test purposes only.
INDEX	I	INDEX. Input for index pulse received from the drive.
INPUT/	I/O	DISK SEQUENCER INPUT/OUTPUT. A general purpose control (output) and status (input) pin configured by the Output Enable Bit of Register 71H, bit 7. At power-on, this pin is an input. As an input, it can be used to synchronize the disk sequencer to an external event. As an output, it is controlled by bit 2 of the Control Field of the disk sequencer.
$\overline{\text{AMD}}$/SECTOR	I/O	ADDRESS MARK DETECT/SECTOR. This pin is used in the hard sector mode as the sector input. A pulse on this pin indicates a sector mark is found. In the soft sector mode a low-level input indicates an address mark was detected. The device powers up in soft sector default mode.
RG	O	READ GATE. During disk data read, this pin is asserted. Active high.
WG	O	WRITE GATE. During disk data write, this pin is asserted. Active high.
RRCLK	I	READ/REFERENCE CLOCK. This pin is used to clock data on the NRZ pin into and out of the device.
NRZ0	I/O	NON RETURN TO ZERO. This signal is the read data input from the disk drive when the read gate signal is asserted; it is the write data output to the disk drive when the write gate signal is asserted.

MICROPROCESSOR INTERFACE

$\overline{\text{RST}}$	I	RESET. An asserted low input generates a component reset that holds the internal registers at reset, stops all operations within the chip, and deasserts all output signals. All input/output signals are set to the high-Z state during the assertion of this signal.
ALE/M/$\overline{\text{NM}}$	I	ADDRESS LATCH ENABLE/MULTIPLEXED/NON-MULTIPLEXED ADDRESS SELECT. When tied high or left floating after reset, the microprocessor interface is configured as non-multiplexed. When driven low, then the microprocessor interface is configured as multiplexed. In this case this pin functions as the address latch enable, and the MA(7:0) pins are the demultiplexed address outputs.
CS	I	CHIP SELECT. Active high signal, when asserted, the internal registers of the SSI 32C9020 can be accessed.
$\overline{\text{WR}}$/R/$\overline{\text{W}}$	I	WRITE STROBE/READ/WRITE. In the Intel bus mode, when an active low signal is present with CS signal high, the data is written to the internal registers. In the Motorola bus mode, this signal acts as the R/$\overline{\text{W}}$ signal.
$\overline{\text{RD}}$/DS	I	READ STROBE/DATA STROBE. In the Intel bus mode, when an active low signal is present with CS signal high, internal register data is read. In the Motorola mode, this signal acts as the DS signal. DS when active high is data strobe.

MICROPROCESSOR INTERFACE (continued)

NAME	TYPE	DESCRIPTION
$\overline{DINT}$	O, OD,Z	DISK INTERRUPT. An active low signal indicates the controller is requesting microprocessor service from the disk side. This signal is programmable for either a push-pull or open-drain output circuit. This signal powers up in the high-Z state. Register 4F bit 3 enables the pull-up.
$\overline{SINT}$	O, OD,Z	SCSI INTERRUPT. This signal is generated by the SCSI controller and is an interrupt line to the microprocessor. It is programmable for either a push-pull or open drain output circuit. This signal powers up in the high-Z state. The interrupt is sourced from the SCSI Interrupt Register. Register 4F bit 3 enables the pull-up. This signal is also programmable to be either an active high or low interrupt.
AD(7:0)	I/O	ADDRESS/DATA BUS. When configured in the Intel mode, these lines are multiplexed, bidirectional microprocessor register address and data lines. When configured in the Motorola mode, these lines are bidirectional data lines.
MA(7:0)	I/O	MICROPROCESSOR ADDRESS BUS: These signals are nonmultiplexed address input or latched address output lines.
READY	O	READY: When this signal is deasserted low, the microprocessor shall insert wait states to allow time for the chip to respond.
I/$\overline{MC}$	I	INTEL/MOTOROLA: This signal selects the microprocessor interface to be used. When this signal is asserted high, it selects the Intel bus control interface. When this signal is deasserted low, it selects the Motorola bus control interface. This signal has an internal pull-up to allow the default selection of the Intel bus control interface.

BUFFER MANAGER INTERFACE

BA(15:0)	O	BUFFER MEMORY ADDRESS LINES 0:15. Active high, for direct connection to a Static or Dynamic RAM address lines 0:15.
BA16/$\overline{RAS}$	O	BUFFER MEMORY ADDRESS 16: In SRAM mode, for direct connection to a Static RAM address line 16. ROW ADDRESS STROBE: In DRAM mode, for direct connection to a Dynamic RAM Row Address Strobe signal.
BA17/$\overline{CAS}$	O	BUFFER MEMORY ADDRESS 17: In SRAM mode, for direct connection to a Static RAM address line 17. ROW ADDRESS STROBE: In DRAM mode, active low, for direct connection to a Dynamic RAM Column Address Strobe signal.
BD(7:0)	I/O	BUFFER MEMORY DATA BUS. 7 through 0. Active high, buffer data bus that connects directly to the buffer RAM data lines.

BUFFER MANAGER INTERFACE

NAME	TYPE	DESCRIPTION
BDP	I/O	BUFFER MEMORY DATA PARITY. This signal provides odd parity for the buffer memory data bus during transfers to/from the buffer memory to the buffer RAM.
$\overline{MOE}$	O	MEMORY OUTPUT ENABLE. This signal is asserted low only for buffer memory read operations.
$\overline{WE}$	O	WRITE ENABLE. Active low, write enable for the buffer RAM.
SYSCLK	I	SYSTEM CLOCK. This signal is used to synchronize the buffer RAM access, including the generation of memory address bits, write enable $\overline{WE}$, and memory output enable $\overline{MOE}$.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC operating characteristics.

PARAMETER	RATING
Power Supply Voltage, VCC	7V
Ambient Temperature	0 to 70°C
Storage Temperature	-65 to 150°C
Power Dissipation	750 mW
Input, Output pins	-0.5 to VCC + 0.5V

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
VCC Power Supply Voltage		4.5		5.5	V
ICC Supply Current	Ta = 25°C Outputs Unloaded			50	mA
ICCS Supply Current				250	µA
VIL Input Low Voltage		-0.5		0.8	V
V0IH Input High Voltage		2		VCC + 0.5	V
VOL Output Low Voltage	All pins except SCSI interface, IOL = 2 mA			0.4	
VOL Output Low Voltage	SCSI interface pins, IOL = 48 mA			0.5	V
VOH Output High Voltage	IOH = -400 µA			2.4	V
IL Input Leakage Current	0 < VIN < VCC	-10		10	µA
CIN Input Capacitance				10	pF
COUT Output Capacitance				10	pF

9

ELECTRICAL SPECIFICATIONS (continued)

Microprocessor Interface Timing Parameters

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
Ta	Ale width		20			ns
Tma	Address valid to MA0:7 valid				30	ns
Tr	$\overline{RD}$ Width		80			ns
As	Address valid to ALE ↓		5			ns
Ah	ALE ↓ to address invalid		10			ns
Cs	CS Valid to $\overline{RD}$ ↓ or DS ↑		20			ns
Ch	$\overline{RD}$ ↑ or DS ↓ to CS ↓		0			ns
Tda	$\overline{RD}$ ↓ or DS ↑ to read data valid				60	ns
Tds	DS width		80			ns
Tdh	$\overline{RD}$ ↑ or DS ↓ to read data invalid		0		25	ns
Tsrw	R/$\overline{W}$ valid to DS ↑		20			ns
Thrw	DS ↓ to R/$\overline{W}$ invalid		20			ns
Tdrdy	$\overline{RD}$ ↓ to READY ↓ (Intel) or DS ↑ to READY ↓ (Motorola)				30	ns
Wds	Write data valid to $\overline{WR}$ ↑ or DS ↓ to write data invalid		40			ns
Wdh	$\overline{WR}$ ↑ or DS ↓ to write data invalid		10			ns
Note:	↑ indicates rising edge	↓ indicates falling edge				

Non-Multiplexed Bus Interface Timings

Tmas	MA(7:0) valid to DS ↓		5			ns
Tmah	DS ↑ to MA(7:0) invalid		5			ns
Cs	CS valid to DS ↓		20			ns
Ch	DS ↑ to CS ↓		0			ns
Tda	DS ↑ to read data valid				60	ns
Tds	DS width		80			ns
Tdh	DS ↑ to read data invalid		0		25	ns
Tsrw	R/$\overline{W}$ valid to DS ↓		20			ns
Thrw	DS ↑ to R/$\overline{W}$ invalid		20			ns
Tdrdy	DS ↑ to READY ↓ (Motorola)				30	ns
WDS	Write data valid to $\overline{WR}$ ↑ or DS ↓		40			ns
Wdh	$\overline{WR}$ ↑ or DS ↓ to write data invalid		10			ns

Note 1: ↑ indicates rising edge ↓ indicates falling edge
Note 2: Loading capacitor = 30 pF

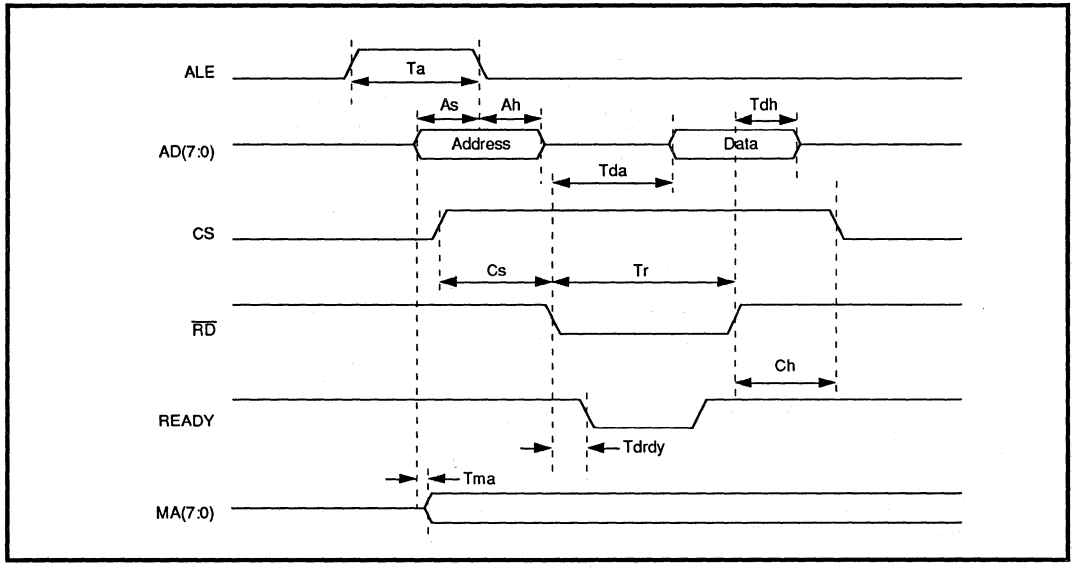


FIGURE 2: Intel Register Multiplexed Read Timing

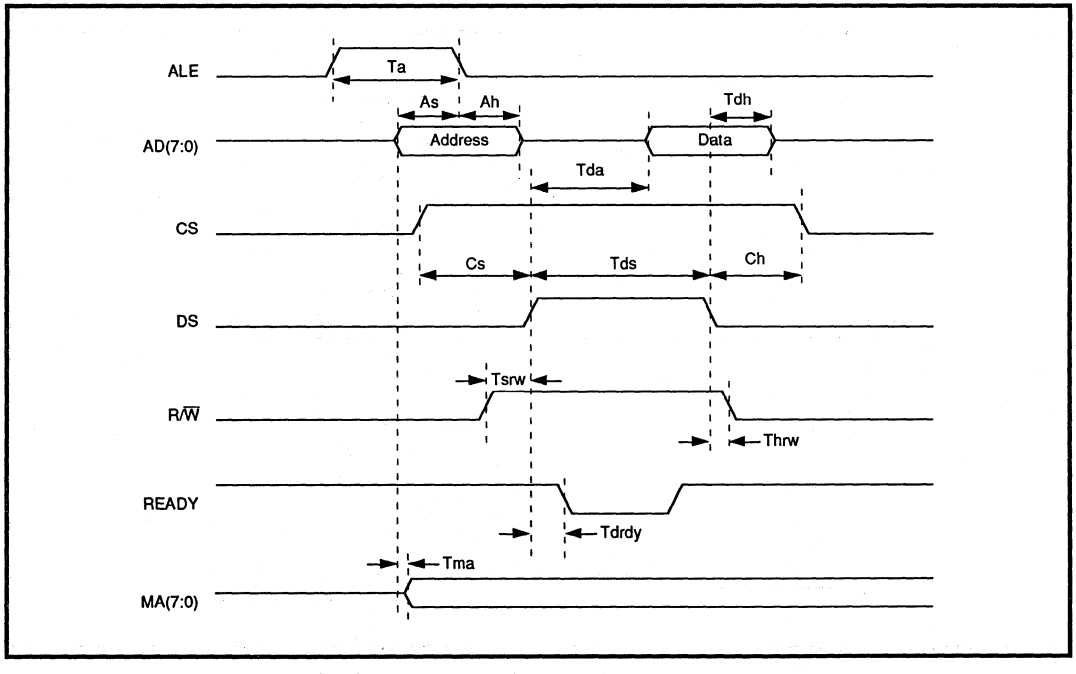


FIGURE 3: Motorola Register Multiplexed Read Timing

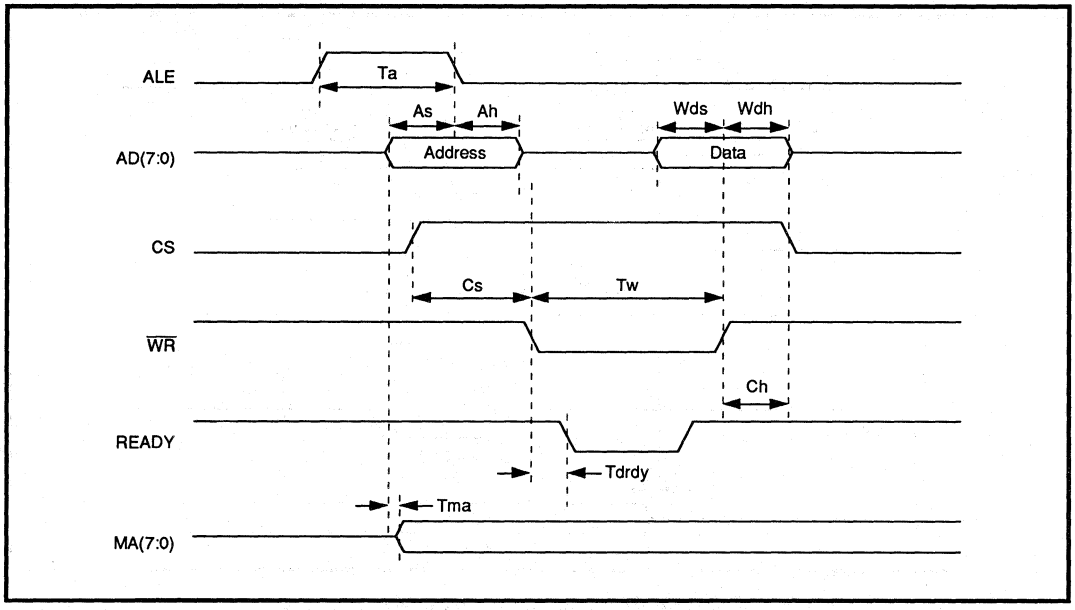


FIGURE 4: Intel Register Multiplexed Write Timing

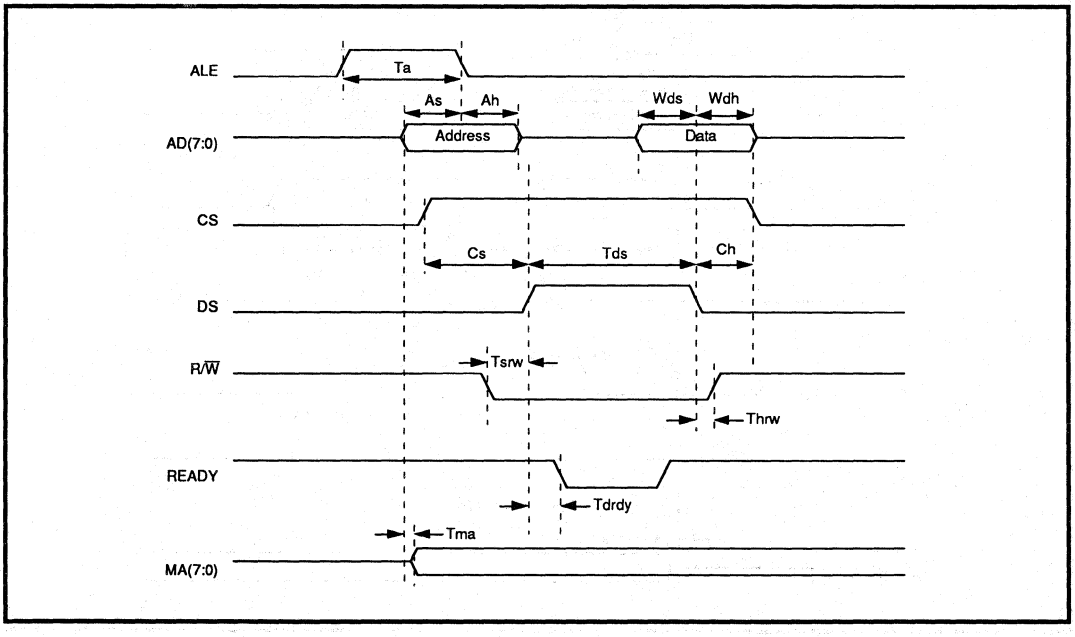


FIGURE 5: Motorola Register Multiplexed Write Timing

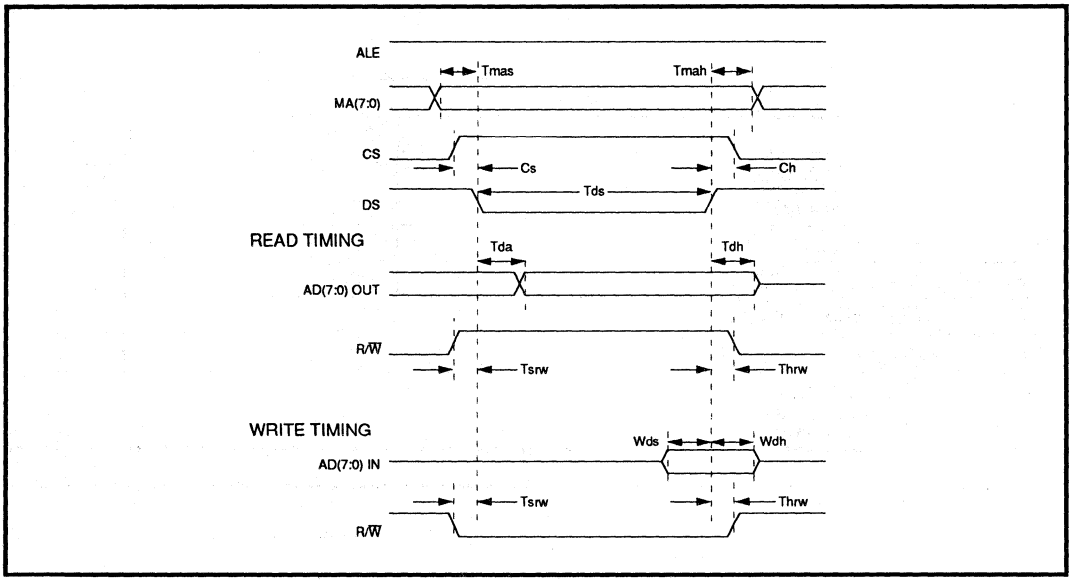


FIGURE 6: Non-Multiplexed Bus Timing Diagrams

ELECTRICAL SPECIFICATIONS (continued)

Disk Interface Timing

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
T	RRCLK		20.8			ns
T/2	RRCLK high/low time		8.5			ns
Tr, Tf	RRCLK rise and fall time		0		2	ns
Ds	NRZ in valid to RRCLK ↑		3			ns
Dh	RRCLK ↑ to NRZ in invalid		3			ns
As	$\overline{AME}$ valid to RRCLK ↑		3			ns
Dv	RRCLK ↑ to NRZ out		3		15	ns
Note:	↑ indicates rising edge					
Loading capacitor = 10 pF						

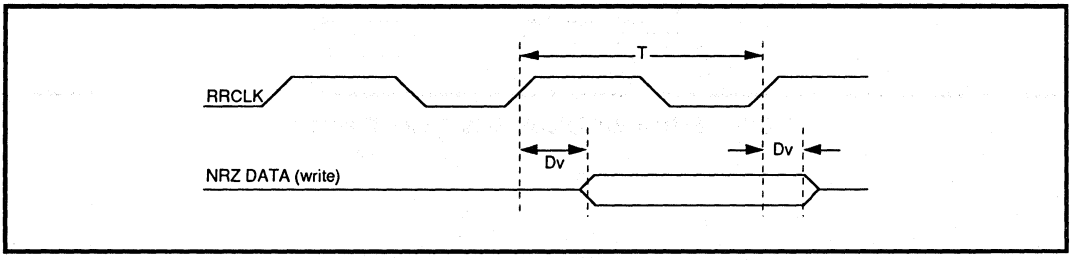


FIGURE 7: Disk Write Timing

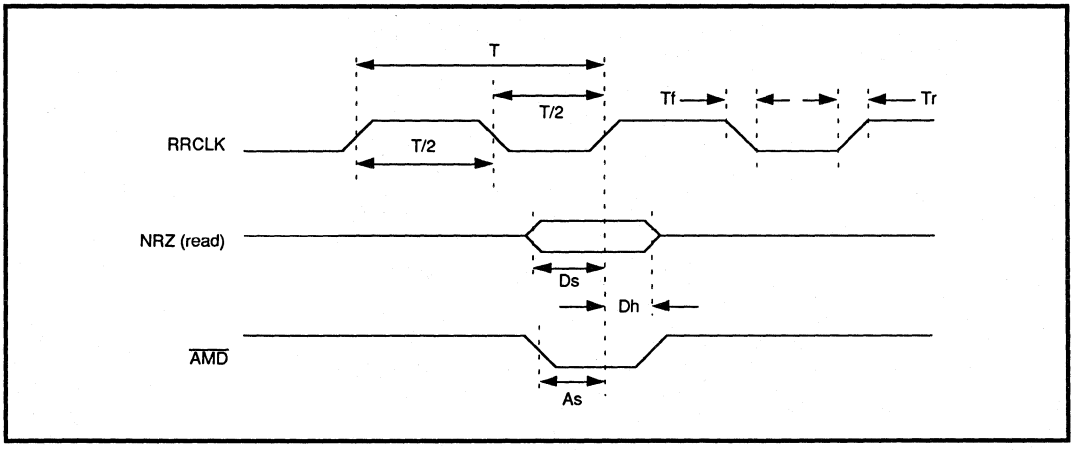


FIGURE 8: Disk Read Timing

BUFFER MEMORY READ/WRITE TIMING PARAMETERS (Figures 9 through 14)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
T	SYSCLK period		25			ns
T/2	SYSCLK high/low time		10			ns
Tav	SYSCLK ↑ to address valid	Note 1			18	ns
Tmsv	SYSCLK ↑ to $\overline{MS}$↓	Notes 1, 6			18	ns
Tmsh	SYSCLK ↑ to $\overline{MS}$↑	Note 1			18	ns
Tmv	SYSCLK ↑ to $\overline{MOE}$↓	Note 1			18	ns
Tmh	SYSCLK ↑ to $\overline{MOE}$↑	Note 1			18	ns
Twv	SYSCLK ↑ to $\overline{WE}$↓	Note 1			18	ns
Twh	SYSCLK ↑ to $\overline{WE}$↑	Note 1			18	ns
Tdov	SYSCLK ↑ to data out valid	Note 1			18	ns
Tdoh	SYSCLK ↑ to data out invalid	Note 1			18	ns
Tdis	Data in valid to $\overline{MOE}$ ↑ (SRAM) Data in valid to $\overline{CAS}$ ↑ (DRAM)		5			ns
Tdih	$\overline{MOE}$ ↑ to data in valid (SRAM) $\overline{CAS}$ ↑ to data in valid (DRAM)		0			ns
Trv	SYSCLK ↑ to $\overline{RAS}$↓	Note 1			18	ns
Trh	SYSCLK ↑ to $\overline{RAS}$↑	Note 1			18	ns
Trav	SYSCLK ↑ to row address valid	Note 1			18	ns
Trah	SYSCLK ↑ to row address invalid	Note 1			18	ns
Tcv	SYSCLK ↑ to $\overline{CAS}$↓	Note 1			18	ns
Tch	SYSCLK ↑ to $\overline{CAS}$↑	Note 1			18	ns
Tcav	SYSCLK ↑ to column address valid	Note 1			18	ns
Tcah	SYSCLK ↑ to column address invalid		0			ns

ELECTRICAL SPECIFICATIONS (continued)

BUFFER MEMORY READ/WRITE TIMING PARAMETERS (Figures 9 through 14) (continued)

PARAMETER		CONDITIONS	MIN	UNIT
Trwl	$\overline{RAS}\downarrow$ to $\overline{RAS}\uparrow$	Notes 2, 3	((RWL + 3) • T)	ns
Trwh	$\overline{RAS}\uparrow$ to $\overline{RAS}\downarrow$	Notes 2, 4	((RWH + 1) • T)	ns
Tcwl	$\overline{CAS}\downarrow$ to $\overline{CAS}\uparrow$	Note 2	((CWL + 1) • T)	ns
Tcwl	$\overline{CAS}\uparrow$ to $\overline{CAS}\downarrow$	Notes 2, 5	((CWL + 1) • T)	ns

Note: Loading capacitance = 30 pF

Note 1: The measured delay for any of the signal indicated by this note will not vary from the measured delay of any other signal indicated by this note by more than ±1 ns.

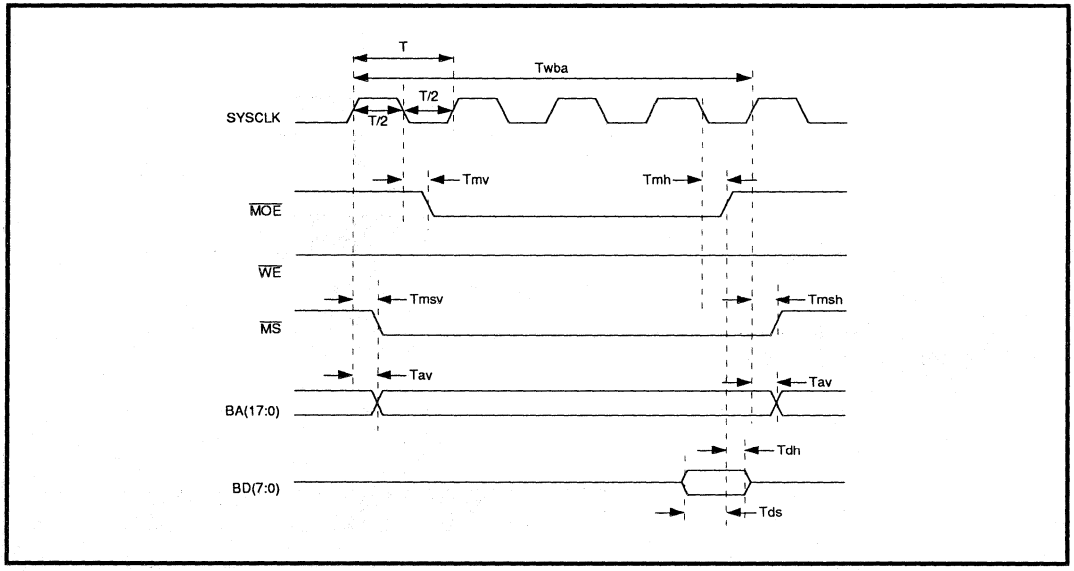
Note 2: RWL, RWH, CWL and CWH are fields in the Buffer Manager Timing Control Register (54H). Each is a two bit field which can contain a value of 0, 1, 2, or 3. These values determine the minimum number of SYSCLK periods (T) for the associated signal width.

Note 3: The minimum width value of Trwl will be generated for refresh cycles and for any buffer memory access cycle except when multiple page mode accesses are performed. When multiple page mode accesses are performed, the width of the $\overline{RAS}$ low pulse is extended until the end of the last $\overline{CAS}$ low cycle.

Note 4: The minumum value of Trwh will be generated whenever the Buffer Manager determines that a buffer request is pending at the ocmpletion of the current memory cycle and a page mode access can not be used either because page mode operation is not enabled or the needed location is not within the current page.

Note 5: The minumum value of Tcwh will be generated only between consecutive page mode accesses.

Note 6: $\overline{MS}$ will rise only if the Buffer Manager determines that no additional requests for buffer access are pending. If the Buffer Manager determines that another access is to be Made, $\overline{MS}$ is kept low between the accesses for improved speed.



Note: Twba is a functional parameter that gives the duration of one RAM data buffer access cycle in SYSCLK periods. The value is programmed in bits 1-0 of register 54H. These examples show Twba = 4T.

FIGURE 9: SRAM Read Timing

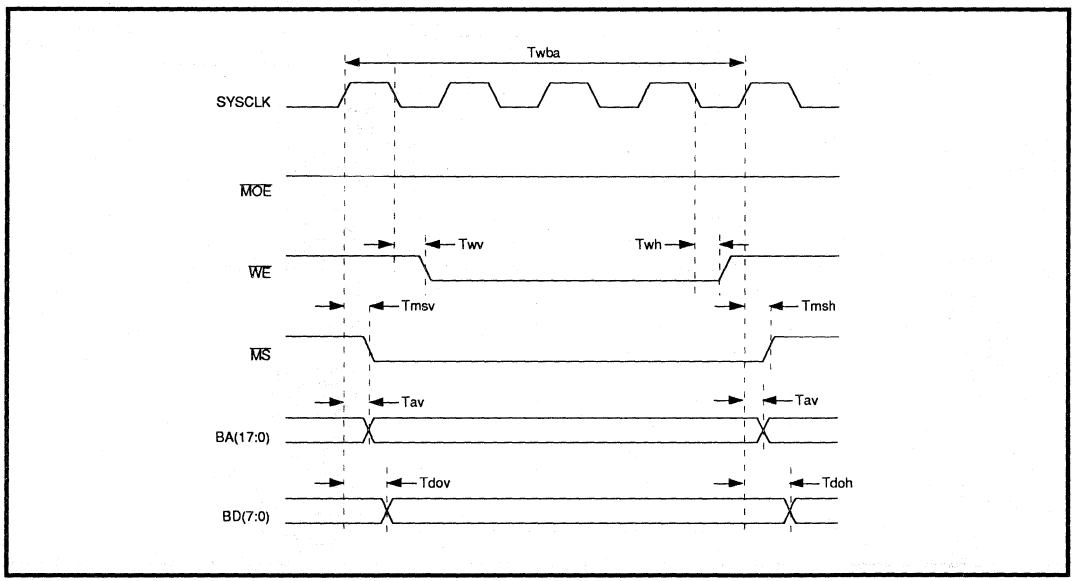


FIGURE 10: SRAM Write Timing

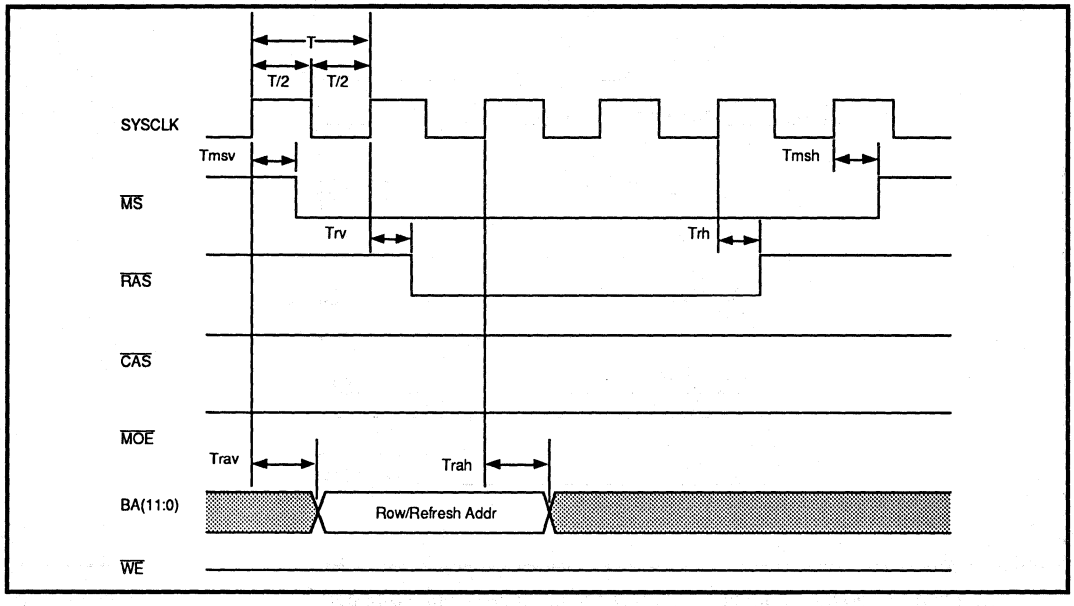


FIGURE 11: DRAM Timing, Refresh Cycle (Shown with WRL = 0)

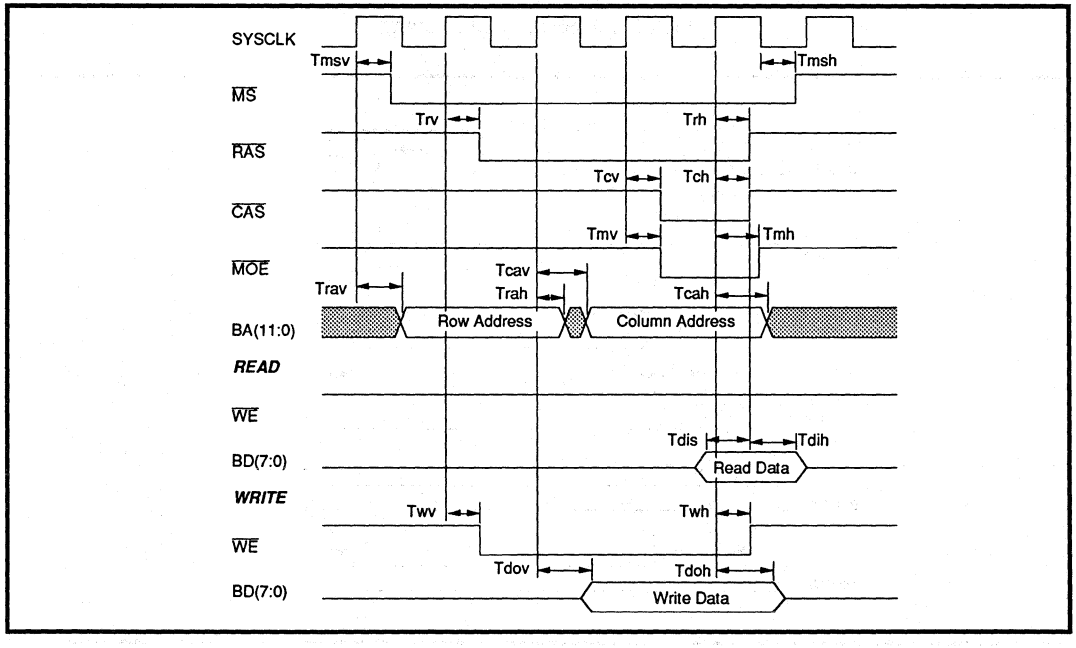


FIGURE 12: DRAM Timing, Standard Cycle (Shown with RWL = 0 and CWL = 0)

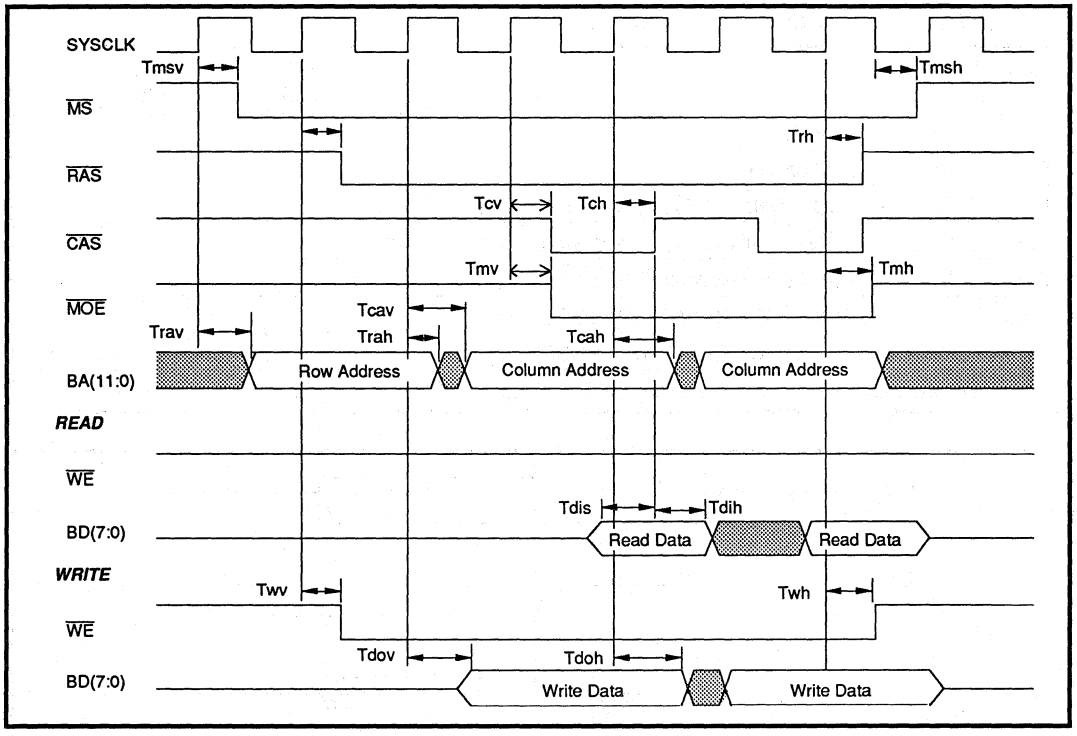


FIGURE 13: DRAM Timing, Fast Page Cycles (Shown with RWL = 0, RWH = 0, CWL = 0 and CWH = 0)

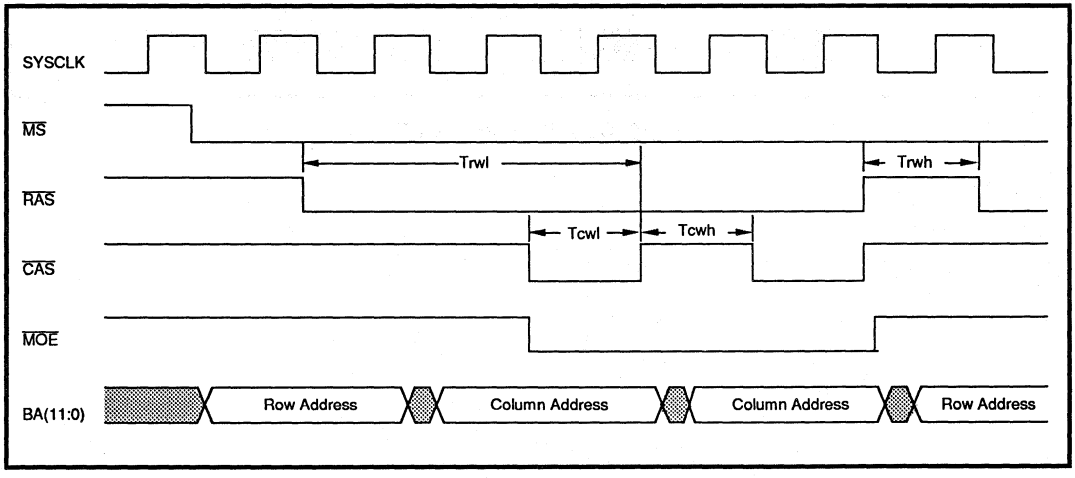


FIGURE 14: DRAM Timing (Showing the Relationship of RWL, RWH, CWL and CWH to overall timing)

ELECTRICAL SPECIFICATIONS (continued)

PARAMETER		MIN (Fast)	MAX (Fast)	MIN (Slow)	MAX (Slow)	UNIT
Trh	$\overline{REQ}$ Assertion Time	37	48			ns
Trl	$\overline{REQ}$ Deassertion Time	63	52			ns
Tids	Setup time SCSI Data to $\overline{REQ}\downarrow$ (write to SCSI bus)	43				ns
Tidh	Hold time $\overline{REQ}\downarrow$ to SCSI Data invalid (write to bus)	43				ns
Tal	Minimum $\overline{ACK}$ Assertion Width Required	10				ns
Tods	Data Hold from $\overline{ACK}\downarrow$ (Read from the SCSI bus)	5				ns
Todh	Data Hold from $\overline{ACK}\downarrow$ (Read from the SCSI bus)	12				ns
Note: All timing parameters are measured with 200 pF load, two SCSI terminator loads, $\overline{ACK}$ filter turned off.						

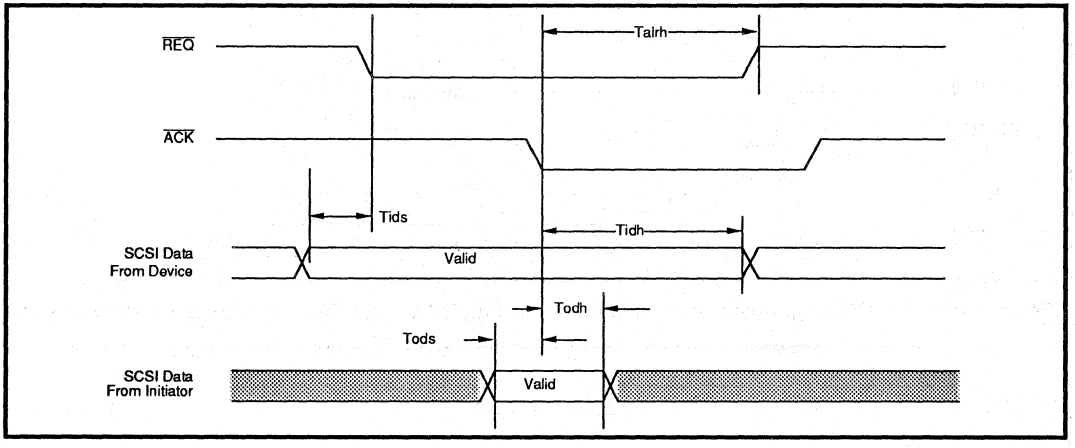


FIGURE 15: SCSI Synchronous Timing

ELECTRICAL SPECIFICATIONS (continued)

PARAMETER		MIN	MAX	UNIT
Tods	Data Setup to $\overline{ACK}\downarrow$ (SCSI Output phase)	5		ns
Todh	Data Hold form $\overline{ACK}\downarrow$ (SCSI Output phase)	12		ns
Talrh	$\overline{ACK}\downarrow$ to $\overline{REQ}\uparrow$		49	ns
Tids	Data Setup to $\overline{REQ}\downarrow$ (SCSI Input phase)	80		ns
Tidh	Data Hold from $\overline{ACK}\downarrow$ (SCSI Input phase)	29		ns
Note: All timing parameters are measured with 200 pF load, two SCSI terminator loads, $\overline{ACK}$ filter turned off.				

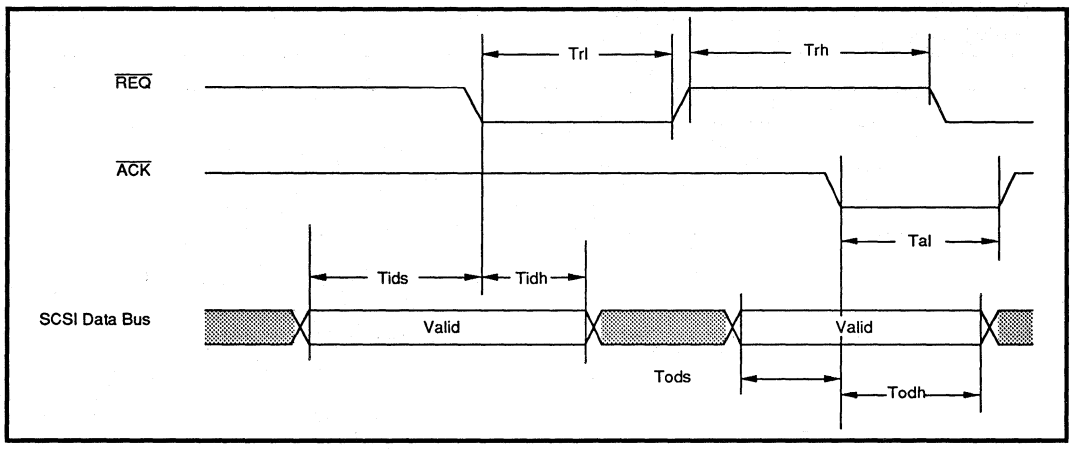


FIGURE 16: SCSI Asynchronous Timing

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Synchronous Data In/Out Phase

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
Txtrp*	Synchronous Transfer Period	(see note)				ns
Tsrl	SYSFREQ high to $\overline{REQ}$ low				50	
Tsrh	SYSFREQ high to $\overline{REQ}$ high				60	ns
Tdov	SYSFREQ high to data out valid				40	ns
Tdsu	Data setup to $\overline{ACK}$ low		55			ns
Tdh	Data hold from $\overline{ACK}$ low		40			ns

Note: Txtrp is the Synchronous Transfer Period as defined by the Synchronous Control Register (Reg: 43H). SYSFREQ is a function of the BUFCLK and is determined by the prescale value as defined by the Clock Control Register (Reg: 49H).

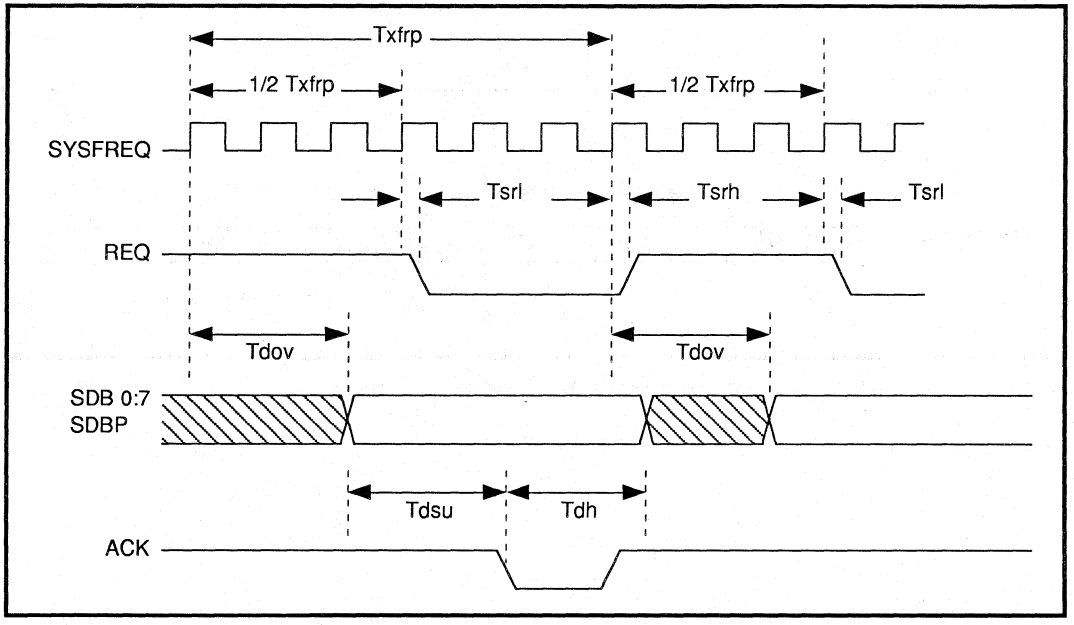


FIGURE 17: Even Number of SYSFREQ Cycles/SCSI Transfer Period

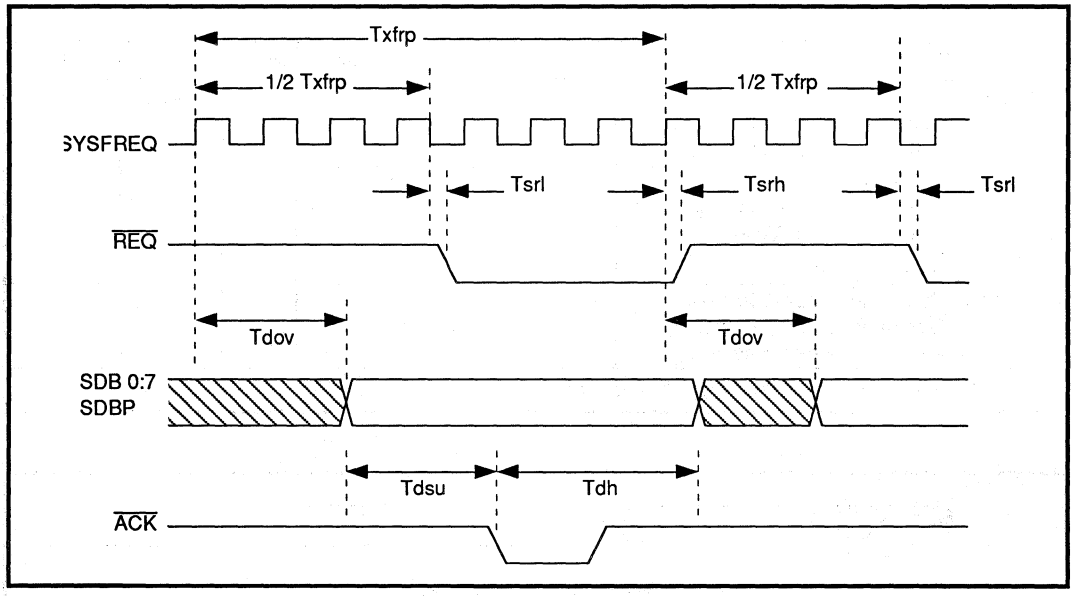


FIGURE 18: Odd Number of SYSFREQ Cycles/SCSI Transfer Period

Wait for Selection

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
Tbsd	Bus Settle Delay (400 ns) to the assertion of $\overline{BSY}$		3T + 90		4T + 90	ns
Note: T is the SCSI Clock Period (SCP) as defined in Register 49H (CLKCTL).						

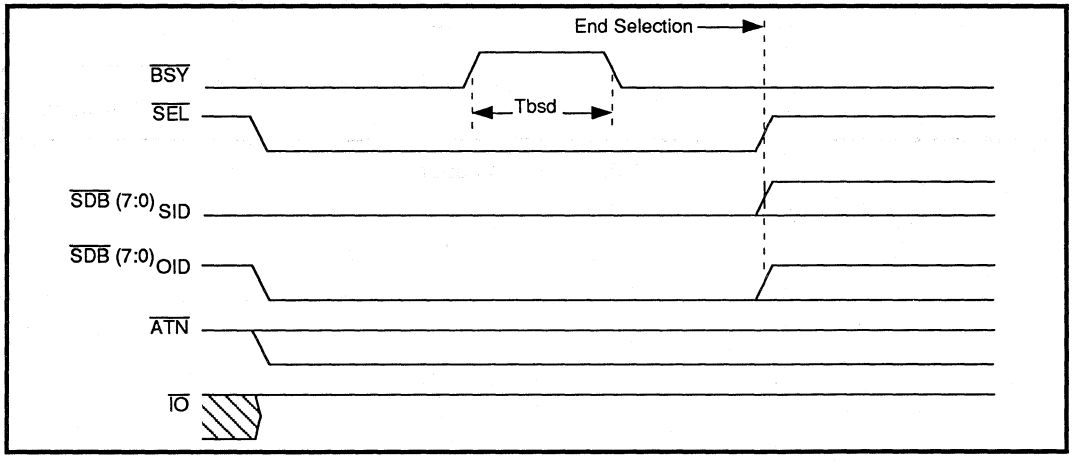


FIGURE 19: Wait for Selection

Arbitration

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
Tbfsd	Bus Settle Delay (400 ns) + Bus Free Delay (800 ns) to the assertion of BSY and $\overline{SDB}_{OID}$		6T + 110		7T + 110	ns
Tad	Arbitration Delay (2.4 µsec) to the assertion of $\overline{SEL}$ (win) or deassertion of $\overline{BSY}$ and $\overline{SDB}_{OID}$ (lost)		-		13T + 100	ns
Tbcsd	Bus Clear Delay (800 ns)+ Bus Settle Delay (400 ns) to end of Arbitration Phase		-		6T + 100	ns
Note: T is the SCSI Clock Period (SCP) as defined in Register 61H (CLKCTL).						

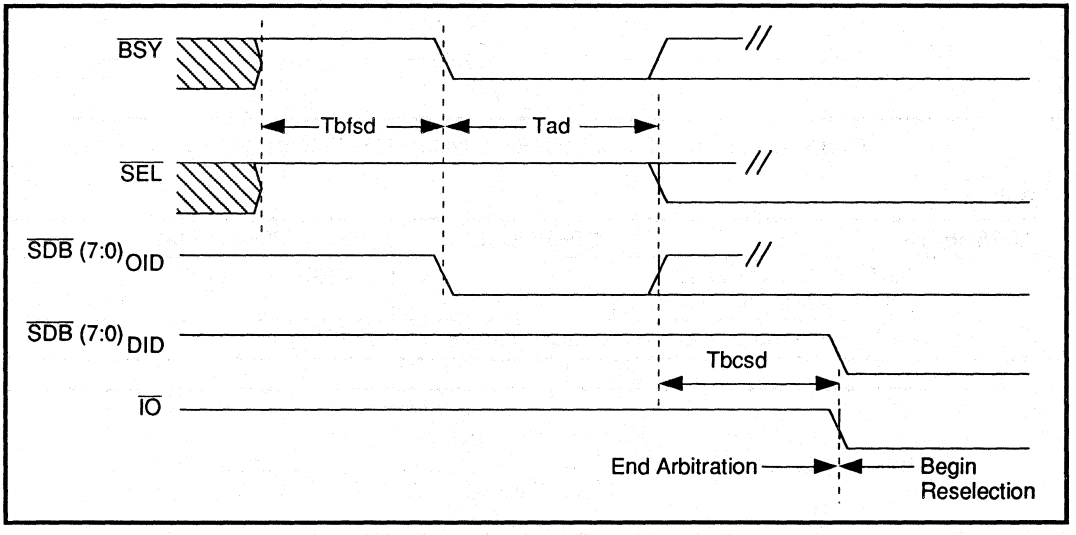


FIGURE 20: Arbitration

Reselection

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
Tbcsd	Bus Clear Delay (800 ns) + Bus Settle Delay (400 ns) to end of Arbitration Phase		-		6T + 100	ns
Tdskd1	Two Deskew Delays (90 ns) to the deassertion of $\overline{BSY}$		-		160	ns
Tbsd	Bus Settle Delay (400 ns) to the assertion of $\overline{BSY}$		-		2T + 40	ns
Tdskd2	Two Deskew Delays (90 ns) to the deassertion of SEL, $\overline{SDB}_{OID}$, and $\overline{SDB}_{DID}$		1T +70		2T + 70	ns
Note: T is the SCSI Clock Period (SCP) as defined in Register 61H (CLKCTL).						

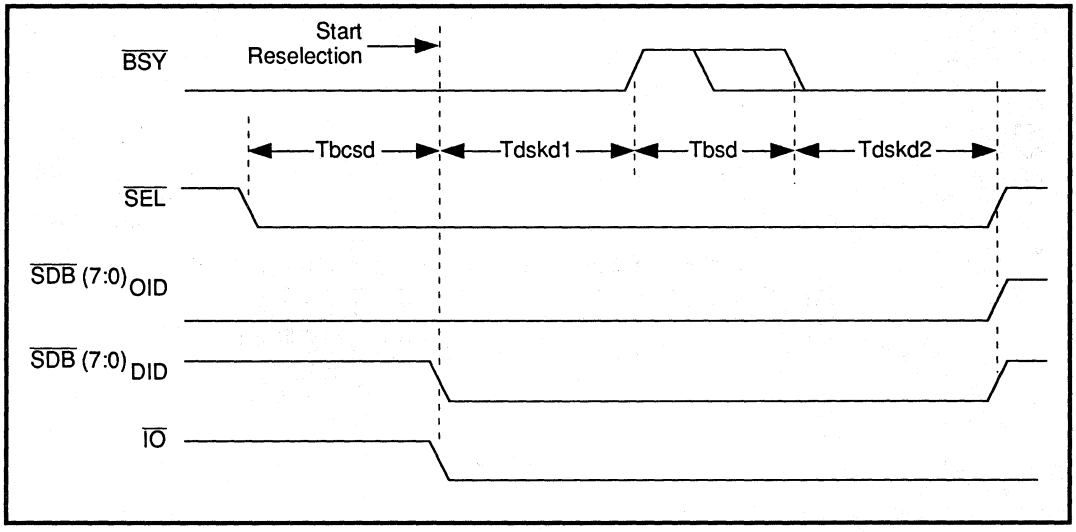
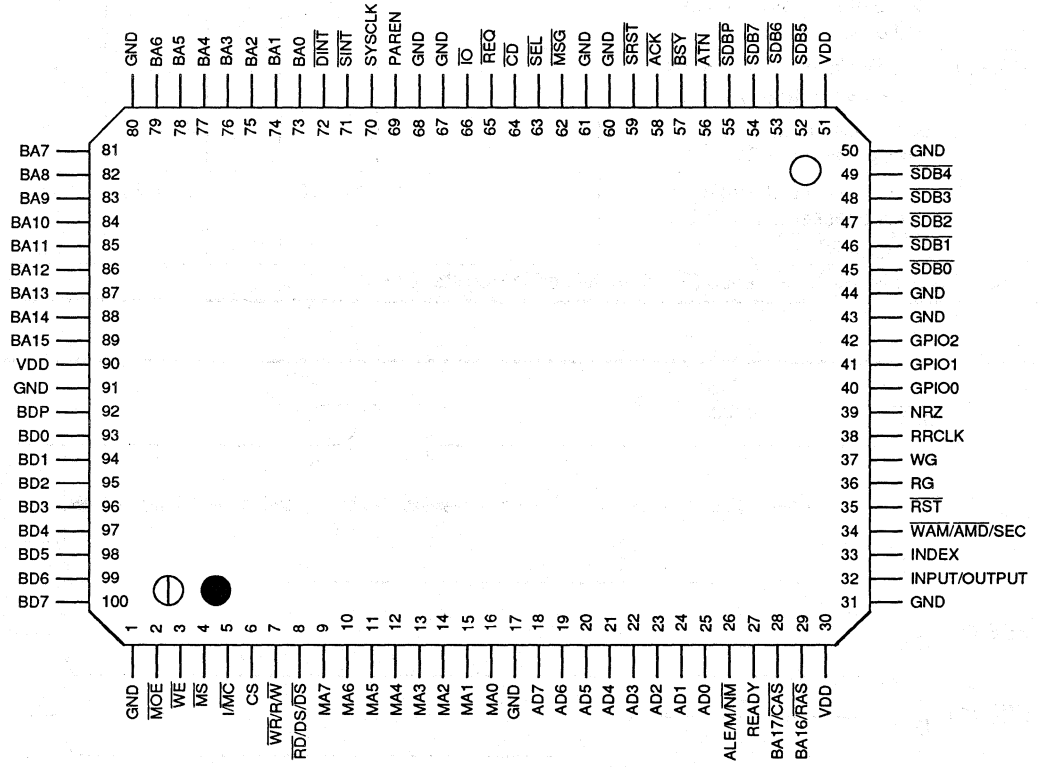


FIGURE 21: Reselection

SSI 32C9020
SCSI Combo Controller
48 Mbit/s; single bit NRZ interface

PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



100-pin QFP

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX: (714) 573-6914

silicon systems®
A TDK Group Company

SSI 32C9022
SCSI Combo Controller
48 Mbit/s; dual bit NRZ interface
Advance Information

January 1994

DESCRIPTION

The SSI 32C9022 is an advanced CMOS VLSI device which integrates major portions of the hardware needed to build a SCSI disk drive. The circuitry of the SSI 32C9023 includes a complete SCSI target interface, an advanced buffer manager, a high performance disk formatter and an 88-bit Reed-Solomon ECC with fast "on-the-fly" hardware correction. The SSI 32C9022 provides maximum performance while minimizing micro controller intervention.

The SSI 32C9022 provides a dual bit and single bit NRZ interface to the ENDEC. Both Interfaces allow an effective transfer rate of up to 48 megabits per second on the disk interface. The dual bit Interface utilizes two parallel NRZ data signals and a clock rate of 24 MHz. The reduction of overall clock rates between the SSI 32C9022 and the ENDEC can be of great benefit to the designer.

The SSI 32C9022 can sustain concurrent transfers of up to 48 megabits per second transfer rate to the disk and 10 megabytes per second across the SCSI bus.

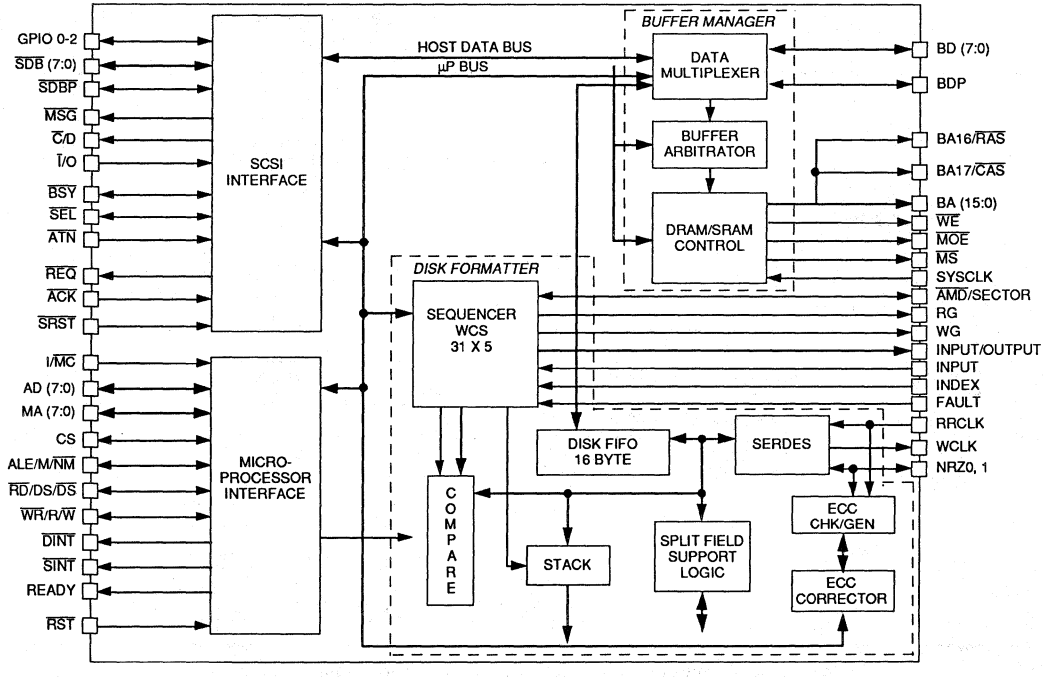
(continued)

FEATURES

- **SCSI Bus Interface**
  - **Full SCSI-2 Compatibility**
  - **Direct bus interface logic with on-chip 48 mA drivers**
  - **Synchronous transfer rates up to 10 megabytes per second**
  - **Asynchronous transfer rates up to 5 megabytes per second**
  - **Parity generation and checking**
  - **Auto Command Mode (ACM) SCSI state machine performs high level SCSI sequences without microprocessor intervention**
  - **Four level ACM command FIFO supports automatic execution of multiple ACM commands**
  - **Hardware support for automatic handling of SCSI-2 command queuing**
  - **Automatic SCSI CDB size determination**
  - **Automatic SCSI Disconnect and Reconnect**
  - **Sixteen byte data FIFO between SCSI channel and Buffer Manager**

(continued)

BLOCK DIAGRAM



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SSI 32C9022
SCSI Combo Controller
48 Mbit/s; dual bit NRZ interface

DESCRIPTION (continued)

In addition, on-the-fly error corrections and microcontroller accesses to the buffer memory will not degrade the throughput during transfers.

The SSI 32C9022 is one of a family of Silicon Systems' single chip disk controllers which support a wide range of device interfaces. The SSI 32C9020 is similar to the SSI 32C9022, but is contained in a 100-pin package, giving up some features for size. Other family members support AT and PCMCIA interfaces. All members are based on a common architecture allowing major portions of firmware to be reused. The Silicon Systems' chip family is illustrated in the hierarchy chart shown in Figure 1.

The high level of integration within the SSI 32C9022 represents a major reduction in parts count. When the SSI 32C9022 SCSI Controller is combined with the SSI 32R2110 Read/Write device, the SSI 32P3000 Pulse Detector, the SSI 32D5392 Dual Bit Data Synchronizer with 1,7 ENDEC, the SSI 32H4631 Servo and Motor Speed Controller, an appropriate microcontroller and memory, a complete, cost efficient, high performance intelligent drive solution is created.

FEATURES (continued)

- Buffer Manager
  - Direct support of DRAM or SRAM
    - SRAM throughput to 20 megabytes per second
    - SRAM size up to 256k bytes
    - DRAM throughput to 17.78 megabytes per second
    - DRAM size up to 1 megabyte
  - Programmable memory timing
  - Buffer RAM segmentation with flexible segment sizes from 256 bytes to 1 megabyte
  - Dedicated host, disk and microprocessor address pointers
  - Internal buffer protection circuit provides buffer integrity
- Disk Formatter
  - Dual bit or serial NRZ interface
  - Effective data rates to 80 megabits/s
  - Automatic multi-sector transfer
  - Header or microprocessor based split data field support
  - Advanced sequencer organized in 31 x 5 bytes
  - 88-bit Reed Solomon ECC with "on-the-fly" fast hardware correction circuitry
  - Capable of correcting up to four 10-bit symbols in error

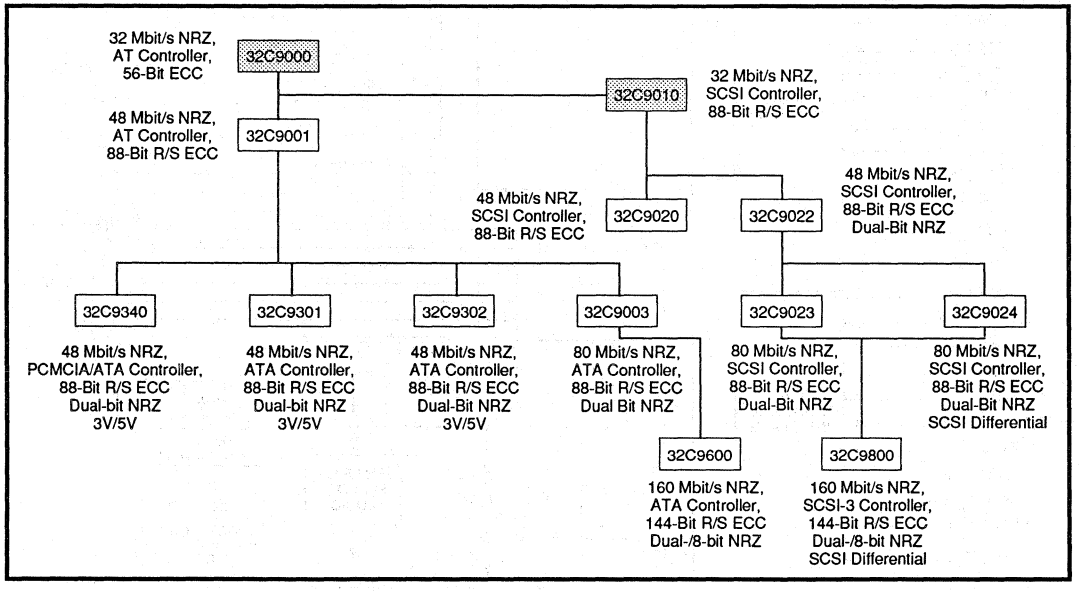

FIGURE 1: Silicon Systems' Single Chip Controller Hierarchy

  - Guaranteed to correct one 31-bit burst or two 11-bit bursts
  - Hardware on-the-fly correction of an 11-bit single burst error within a half sector time
  - Detects up to one 51-bit burst or three 11-bit bursts
- Microprocessor Interface
  - Supports both multiplexed or non-multiplexed microprocessors
  - Separate or combined host and disk interrupts
  - Programmable wait state insertion
- Other Features
  - Internal Power Down modes
  - Available in 128-pin QFP

FUNCTIONAL DESCRIPTION

The SSI 32C9022 contains the following four major functional blocks:

Microcontroller Interface
SCSI Interface
Disk Formatter
Buffer Manager

The microprocessor interface allows the local microprocessor access to all of the SSI 32C9022 internal control registers and any location within the buffer memory. The microprocessor, by writing and reading the internal registers can control all activities of the SSI 32C9022. The microprocessor can elect to perform SCSI and/or disk operations directly, or it can enable the advanced features of the SSI 32C9022 which can perform all typical operations automatically.

The SCSI Interface block handles all SCSI activities. The SCSI interface includes 48 mA drivers allowing for direct connection of the SSI 32C9022 to the SCSI bus. The SCSI interface logic includes Auto Command Mode (ACM) logic, an advanced state machine capable of handling a variety of complex SCSI sequences without microprocessor intervention. The microprocessor can queue up to four ACM commands into the ACM Command FIFO to create even more sophisticated command sequences. The SCSI block interfaces directly with the buffer manager via an internal speed matching FIFO. This FIFO, plus the bandwidth capabilities of the buffer manager guarantee sustained full speed transfers across the SCSI bus. The high level of automation of the ACM minimizes SCSI bus overhead. The net result is maximized performance with minimum SCSI bus bandwidth utilization.

The disk formatter performs the serialization and deserialization of data. If provides all of the necessary functions to control track formatting, header search, and the reading and writing of data. The heart of the disk formatter is an advanced programmable sequencer which is flexible enough to interface to a wide variety of read/write channels. The sequencer can contain 31 instructions, each of which is 5 bytes (40 bits) in width. The width of the instructions allows for sophisticated branching techniques which increase the flexibility and power of the sequencer. The flexible disk interface can be configured through a wide range of capabilities. This allows the SSI 32C9022 to interface with nearly any read/write channel and allows the user of the SSI 32C9022 to select the read/write channel best suited to the device. Of course, by selecting the SSI 32C9022 controller and the SSI 32D5392 Data Synchronizer with 1,7 ENDEC, you are guaranteed a problem free interface.

Within the disk formatter are the ECC generator/checker and ECC corrector. The generator/checker provides the ability to generate or check a 32-bit ECC for headers and an 88-bit Reed Solomon code for data. If the checker detects an error in an 88-bit Reed Solomon data field, the syndrome information is transferred into the corrector. The corrector performs the necessary operations to determine if the error was correctable and interfaces directly with the buffer controller to perform the correction automatically. The corrector performs its correction within one half of a sector time. This gaurantees that the corrector will always be available to correct the next sector if necessary.

As its name implies, the buffer manager manages the data buffer of the controller. The buffer manager can support either SRAM or DRAM. When configured to operate with DRAM, the buffer manager automatically performs necessary refresh cycles. The buffer manager creates all of the necessary timing and control signals for a wide range of memory types and speeds. The buffer manager interfaces with the buffer memory, the SCSI Interface block, the data path of the disk formatter block, the ECC corrector and the microprocessor. If more than one of these devices requires access to the buffer memory, the buffer manager arbitrates the requests automatically. The buffer manager of the SSI 32C9022 can sustain SCSI operations at the rate of 10 megabytes per second, disk formatter operations at 48 megabits per second (6 megabytes per second) and still have sufficient band width left to handle on-the-fly ECC corrections and microprocessor accesses without degrading performance on any of the interfaces.

PIN DESCRIPTION

The following convention is used in the pin description:

(I) denotes an input
(O) denotes an output
(Z) denotes a tri-state output
(OD) denotes an open drain output

GENERAL

NAME	TYPE	DESCRIPTION
VDD		POWER SUPPLY PIN
GND		GROUND

HOST INTERFACE

$\overline{SDBP}$	I/O	SCSI DATA BUS PARITY. Odd parity bit for the SCSI data bus.
$\overline{SDB(7:0)}$	I/O	SCSI DATA BUS BITS 7-0.
$\overline{ATN}$	I	ATTENTION. This active low signal is used by the initiator to request a message out phase.
$\overline{BSY}$	I/O	BUSY. This active low signal is used to indicate when the bus is active.
$\overline{ACK}$	I	ACKNOWLEDGE. This active low signal is used in the handshake protocol to indicate the completion of a data byte transfer.
$\overline{SRST}$	I	SCSI RESET. This active low signal is used to reset the SCSI controller.
$\overline{MSG}$	O	MESSAGE. This active low signal is used to indicate a message phase.
$\overline{SEL}$	I/O	SELECT. This active low signal is used to indicate either a selection or reselection phase.
$\overline{C}$/D	O	COMMAND/DATA. This signal is used to indicate either a command or data phase.
$\overline{REQ}$	I	REQUEST. This active low signal is used in the handshake protocol to initiate a data byte transfer.
$\overline{I}$/O	I	INPUT/OUTPUT. This signal is used to indicate the direction of data transfer.
GPIO(2:0)	I/O	INPUT/OUTPUT. These pins are used to indicate the SCSI ID of the target device. The pins can be programmed as outputs for test purposes only.

DISK INTERFACE

INDEX	I	INDEX. Input for index pulse received from the drive.
INPUT/ OUTPUT	I/O	DISK SEQUENCER INPUT/OUTPUT. A general purpose control (output) and status (input) pin configured by the Output Enable Bit of Register 71H, bit 7. At power-on, this pin is an input. As an input, it can be used to synchronize the disk sequencer to an external event. As an output, it is controlled by bit 2 of the Control Field of the disk sequencer.
INPUT	I	INPUT. This pin can be used to synchronize the disk to an external event.
$\overline{AMD}$/ SECTOR	I/O	ADDRESS MARK DETECT/SECTOR. This pin is used in the hard sector mode as the sector input. A pulse on this pin indicates a sector mark is found. In the soft sector mode, a low-level input indicates an address mark was detected. The device powers up in soft sector default mode.

DISK INTERFACE (continued)

NAME	TYPE	DESCRIPTION
RG	O	READ GATE. During disk data read, this pin is asserted. Active high.
WG	O	WRITE GATE. During disk data write, this pin is asserted. Active high.
RRCLK	I	READ/REFERENCE CLOCK. This is a clock signal generated from an external data synchronizer. This clock is used to synchronize the input NRZ data and clock the disk formatter of the chip.
WCLK	O	WRITE CLOCK. This signal clocks the NRZ data out in the dual NRZ interface mode.
NRZ1	I/O	NON RETURN TO ZERO 1. In dual NRZ mode, this signal is the most significant bit read data input from the disk drive when the read gate signal is asserted; it is the most significant bit write data output to the disk drive when the write gate signal is asserted. In single NRZ mode, this signal is not used and should be grounded. NRZ1 is the leading bit of the bit pair. In Write mode, the MSB of the data bytes always appears on NRZ1.
NRZ0	I/O	NON RETURN TO ZERO. In dual NRZ mode, this signal is the least significant bit read data input from the disk drive when the read gate signal is asserted; it is the least significant bit write data output to the disk drive when the write gate signal is asserted. In single NRZ mode, this signal is used to transfer NRZ data to/from the read channel chip.
FAULT	I	FAULT. This input when asserted indicates to the chip that a fault has occured with the disk. The disk sequencer will stop and both RG and WG pins will be deasserted.

MICROPROCESSOR INTERFACE

$\overline{RST}$	I	RESET. An asserted low input generates a component reset that holds the internal registers at reset, stops all operations within the chip, and deasserts all output signals. All input/output signals are set to the high-Z state during the assertion of this signal.
ALE/M/$\overline{NM}$	I	ADDRESS LATCH ENABLE/MULTIPLEXED/NON-MULTIPLEXED ADDRESS SELECT. When tied high or left floating after reset, the microprocessor interface is configured as non-multiplexed. When driven low, then the microprocessor interface is configured as multiplexed. In this case this pin functions as the address latch enable, and the MA(7:0) pins are the demultiplexed address outputs.
CS	I	CHIP SELECT. Active high signal, when asserted, the internal registers of the SSI 32C9022 can be accessed.
$\overline{WR}$/R/$\overline{W}$	I	WRITE STROBE/READ/WRITE. In the Intel bus mode, when an active low signal is present with CS signal high, the data is written to the internal registers. In the Motorola bus mode, this signal acts as the R/$\overline{W}$ signal.
$\overline{RD}$/DS/$\overline{DS}$	I	READ STROBE/DATA STROBE. When the Intel bus control interface is selected (the I/$\overline{MC}$ is high), this signal acts as the $\overline{RD}$ signal. When the read strobe signal is asserted low and the CS signal is asserted high, the data from the specified register will be driven to the AD signals. When the Motorola bus control interface is selected (the I/$\overline{MC}$ is low) this signal acts as the data strobe signal. A high on the R/$\overline{W}$ signal along with this signal asserted and the CS signal asserted high indicates a read operation. A low on the R/$\overline{W}$ signal along with this signal asserted and the CS signal asserted high indicates a write operation. Note when non-multiplexed Mototrola bus configuration is chosen, the data strobe is an active low input.
$\overline{DINT}$	O, OD,Z	DISK INTERRUPT. An active low signal indicates the controller is requesting microprocessor service from the disk side. This signal is programmable for either a push-pull or open-drain output circuit. This signal powers up in the high-Z state. Register 4F bit 3 enables the pull-up.

MICROPROCESSOR INTERFACE (continued)

NAME	TYPE	DESCRIPTION
$\overline{SINT}$	O, OD,Z	SCSI INTERRUPT. This signal is generated by the SCSI controller and is an interrupt line to the microprocessor. It is programmable for either a push-pull or open drain output circuit. This signal powers up in the high-Z state. The interrupt is sourced from the SCSI Interrupt Register. Register 4F bit 3 enables the pull-up. This signal is also programmable to be either an active high or low interrupt.
AD(7:0)	I/O	ADDRESS/DATA BUS. When configured in the Intel mode, these lines are multiplexed, bidirectional microprocessor register address and data lines. When configured in the Motorola mode, these lines are bidirectional data lines.
MA(7:0)	I/O	MICROPROCESSOR ADDRESS BUS: These signals are nonmultiplexed address input or latched address output lines.
READY	O	READY: When this signal is deasserted low, the microprocessor shall insert wait states to allow time for the chip to respond.
I/$\overline{MC}$	I	INTEL/MOTOROLA: This signal selects the microprocessor interface to be used. When this signal is asserted high, it selects the Intel bus control interface. When this signal is deasserted low, it selects the Motorola bus control interface. This signal has an internal pull-up to allow the default selection of the Intel bus control interface.

BUFFER MANAGER INTERFACE

BA(15:0)	O	BUFFER MEMORY ADDRESS LINES 15 through 0. Active high, for direct connection to a Static or Dynamic RAM address lines.
BA16/$\overline{RAS}$	O	BUFFER MEMORY ADDRESS 16: In SRAM mode, for direct connection to a Static RAM address line 16. ROW ADDRESS STROBE: In DRAM mode, for direct connection to a Dynamic RAM Row Address Strobe signal.
BA17/$\overline{CAS}$	O	BUFFER MEMORY ADDRESS 17: In SRAM mode, for direct connection to a Static RAM address line 17. ROW ADDRESS STROBE: In DRAM mode, active low, for direct connection to a Dynamic RAM Column Address Strobe signal.
BD(7:0)	I/O	BUFFER MEMORY DATA BUS. 7 through 0. Active high, buffer data bus that connects directly to the buffer RAM data lines.
BDP	I/O	BUFFER MEMORY DATA PARITY. This signal provides odd parity for the buffer memory data bus during transfers to/from the buffer memory to the buffer RAM.
$\overline{MOE}$	O	MEMORY OUTPUT ENABLE. In SRAM mode this signal is asserted low when every buffer memory access is active. In DRAM mode this signal is asserted low only for buffer memory read operation.
$\overline{MS}$	O	MEMORY SELECT. An active low signal indicates external memory is selected.
$\overline{WE}$	O	WRITE ENABLE. Active low, write enable for the buffer RAM.
SYSCLK	I	SYSTEM CLOCK. This signal is used to synchronize the buffer RAM access, including the generation of memory address bits, write enable $\overline{WE}$, and memory output enable $\overline{MOE}$.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC operating characteristics.

PARAMETER	RATING
Power Supply Voltage, VCC	7V
Ambient Temperature	0 to 70°C
Storage Temperature	-65 to 150°C
Power Dissipation	750 mW
Input, Output pins	-0.5 to VCC+0.5V

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
VCC Power Supply Voltage		4.50		5.50	V
ICC Supply Current	Ta = 25°C Outputs Unloaded			50	mA
ICCS Supply Current				250	µA
VIL Input Low Voltage		-0.5		0.8	V
V0IH Input High Voltage		2.0		VCC+0.5	V
VOL Output Low Voltage	All pins except SCSI interface, IOL = 2 mA			0.4	V
VOL Output Low Voltage	SCSI interface pins, IOL = 48 mA			0.5	V
VOH Output High Voltage	IOH = -400 µA			2.4	V
IL Input Leakage Current	0 < VIN < VCC	-10		10	µA
CIN Input Capacitance				10	pF
COUT Output Capacitance				10	pF

MICROPROCESSOR INTERFACE TIMING

Multiplexed Interface Timing Parameters (Figures 2-5)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
Ta	ALE width		20			ns
Tma	Address valid to MA(7:0) valid				30	ns
Tr	$\overline{RD}$ width		80			ns
As	Address valid to ALE ↓		5			ns
Ah	ALE ↓ to address invalid		10			ns
Cs	CS valid to $\overline{RD}$ ↓ or DS ↑		20			ns
Ch	$\overline{RD}$ ↑ or DS ↓ to CS ↓		0			ns
Tda	$\overline{RD}$ ↓ or DS ↑ to read data valid				60	ns
Tds	DS width		80			ns
Tdh	$\overline{RD}$ ↑ or DS ↓ to read data invalid		0		25	ns
Tsrw	R/$\overline{W}$ valid to DS ↑		20			ns
Thrw	DS ↓ to R/$\overline{W}$ invalid		20			ns
Tdrdy	$\overline{RD}$ ↓ to READY ↓ (Intel) or DS ↑ to READY ↓ (Motorola)				30	ns
Wds	Write data valid to $\overline{WR}$ ↑ or DS ↓		40			ns
Wdh	$\overline{WR}$ ↑ or DS ↓ to write data invalid		10			ns

Note: ↑ indicates rising edge ↓ indicates falling edge

Non-Multiplexed Bus Interface Timings (Figure 6)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
Tmas	MA(7:0) valid to DS ↓		5			ns
Tmah	DS ↑ to MA(7:0) invalid		5			ns
Cs	CS valid to DS ↓		20			ns
Ch	DS ↑ to CS ↓		0			ns
Tda	DS ↑ to read data valid				60	ns
Tds	DS width		80			ns
Tdh	DS ↑ to read data invalid		0		25	ns
Tsrw	R/$\overline{W}$ valid to DS ↓		20			ns
Thrw	DS ↑ to R/$\overline{W}$ invalid		20			ns
Tdrdy	DS ↑ to READY ↓ (Motorola)				30	ns
Wds	Write data valid to $\overline{WR}$ ↑ or DS ↓		40			ns
Wdh	$\overline{WR}$ ↑ or DS ↓ to write data invalid		10			ns

Note 1: ↑ indicates rising edge ↓ indicates falling edge

Note 2: Loading capacitor = 30 pF

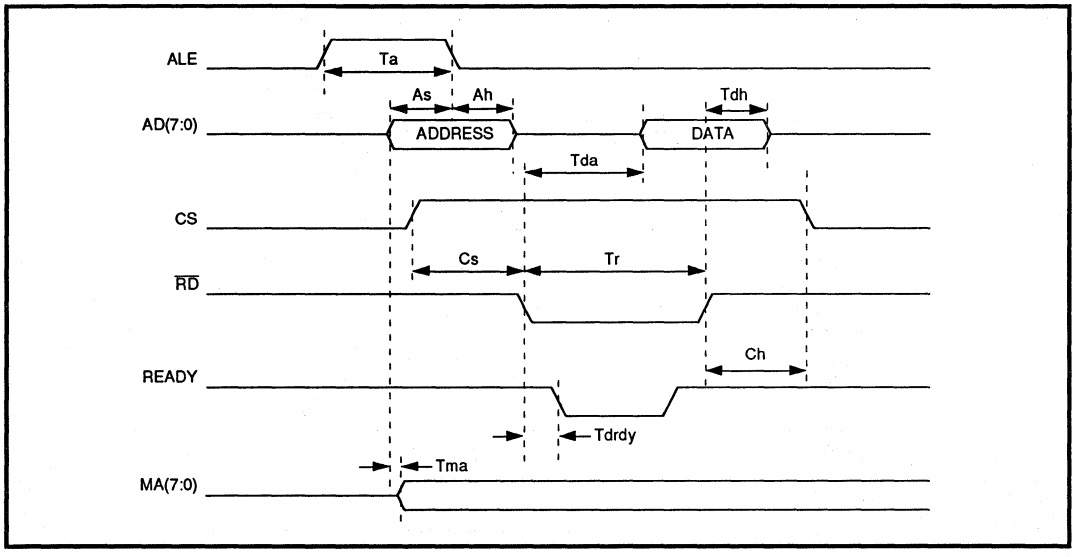

FIGURE 2: Intel Register Multiplexed Read Timing

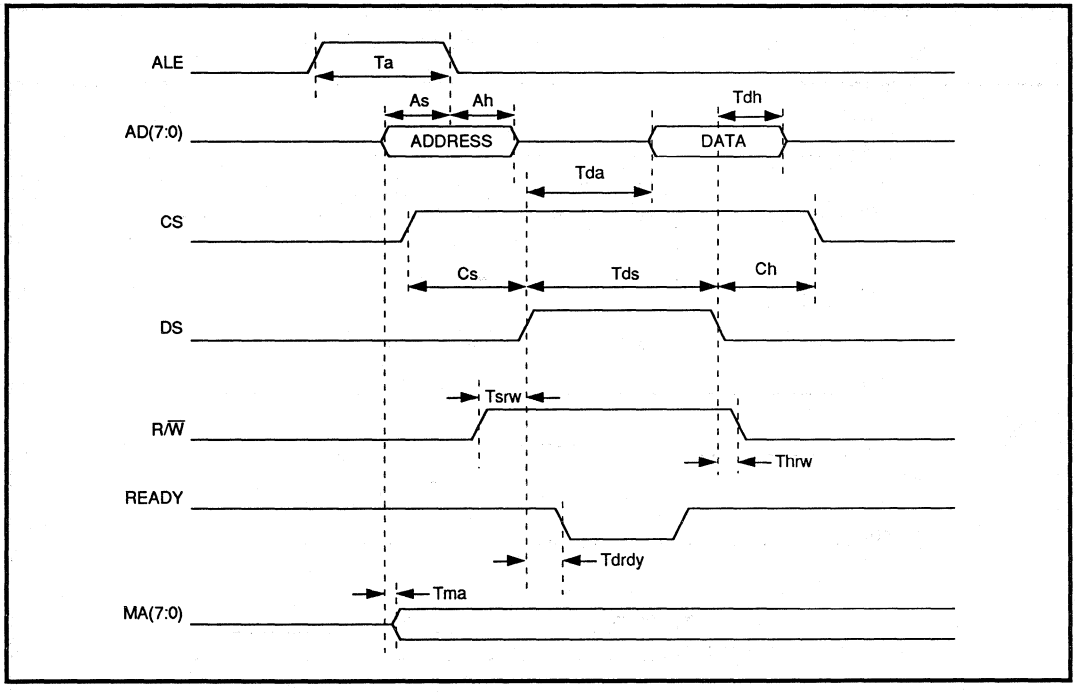

FIGURE 3: Motorola Register Multiplexed Read Timing

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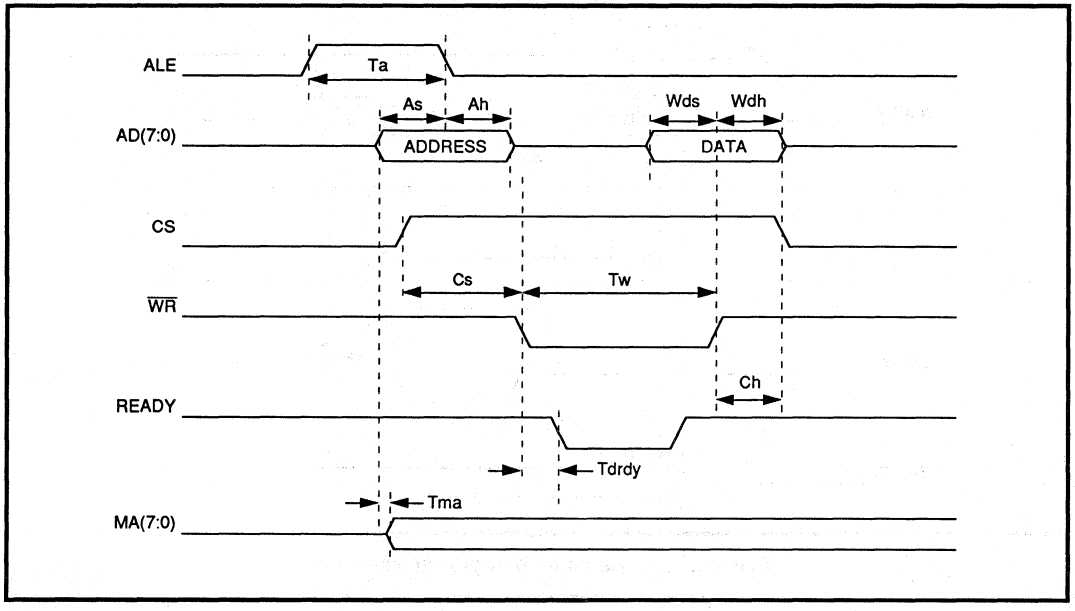

FIGURE 4: Intel Register Multiplexed Write Timing

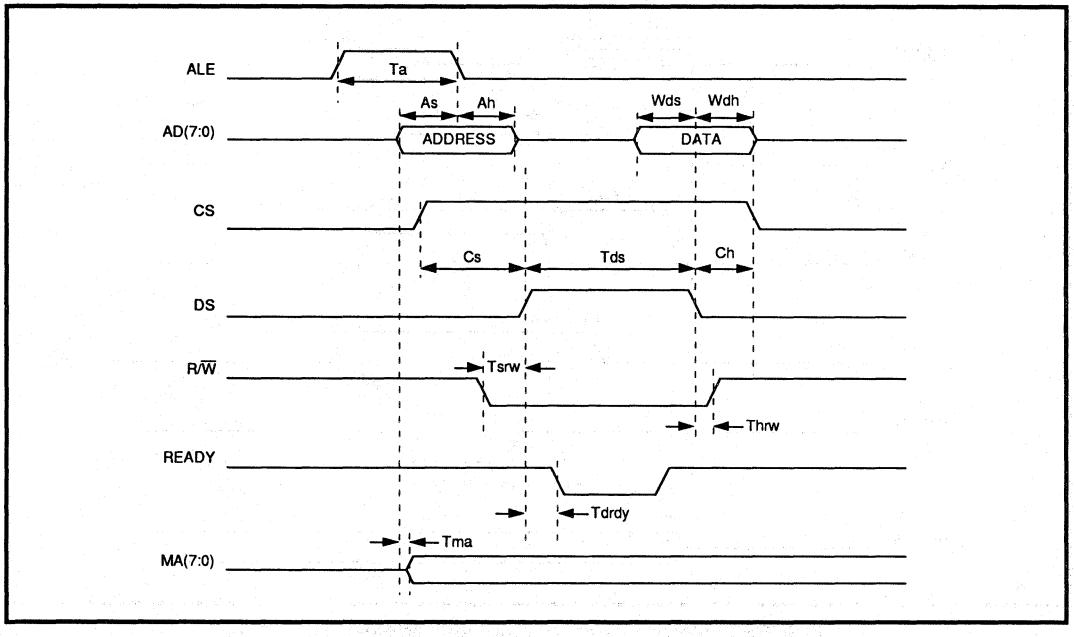

FIGURE 5: Motorola Register Multiplexed Write Timing

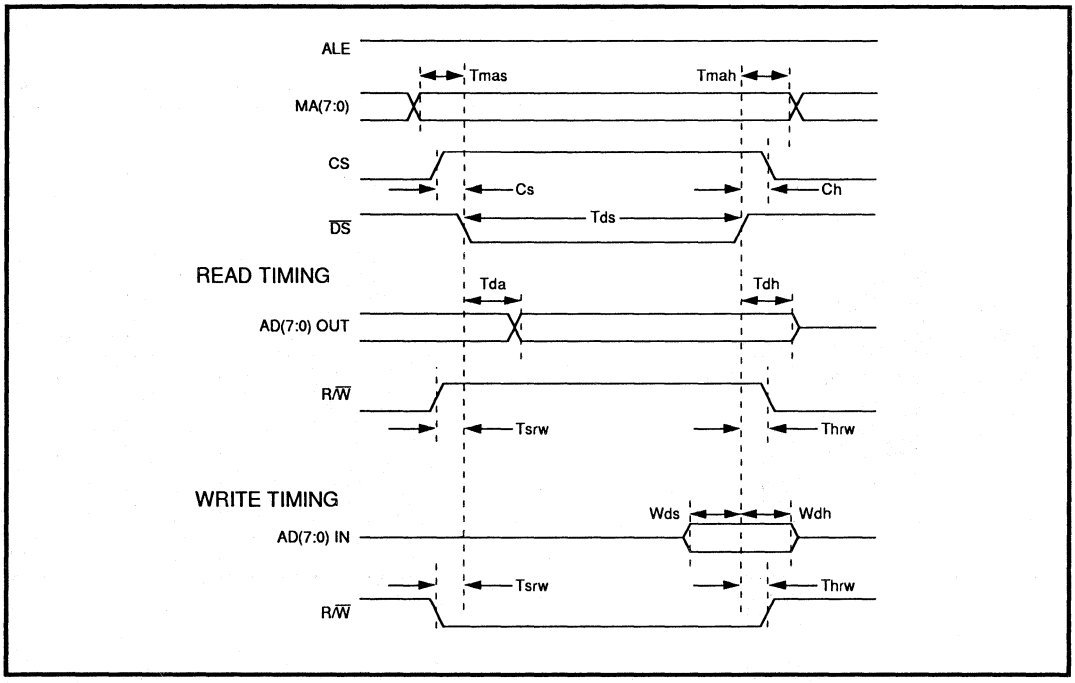

FIGURE 6: Non-Multiplexed Bus Timing Diagrams

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ELECTRICAL SPECIFICATIONS (continued)

Disk Interface Timing

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
T	Dual bit interface RRCLK period		40			ns
	Single bit interface RRCLK period		20.8			ns
T/2	Dual bit interface RRCLK high/low time		16			ns
	Single bit interface RRCLK high/low time		8.5			ns
Tr, Tf	RRCLK rise/fall time				3	ns
Dis	NRZ in valid to RRCLK ↑		3			ns
Dih	RRCLK ↑ to NRZ in invalid		3			ns
As	$\overline{AMD}$ valid to RRCLK ↑		3			ns
Tckd	RRCLK ↓ to WCLK ↓				8	ns
Dvr	RRCLK ↓ to NRZ out valid				18	ns
Dv	WCLK ↓ to NRZ out valid				±2	ns

Note: ↑ indicates rising edge ↓ indicates falling edge

Loading capacitor = 10 pF

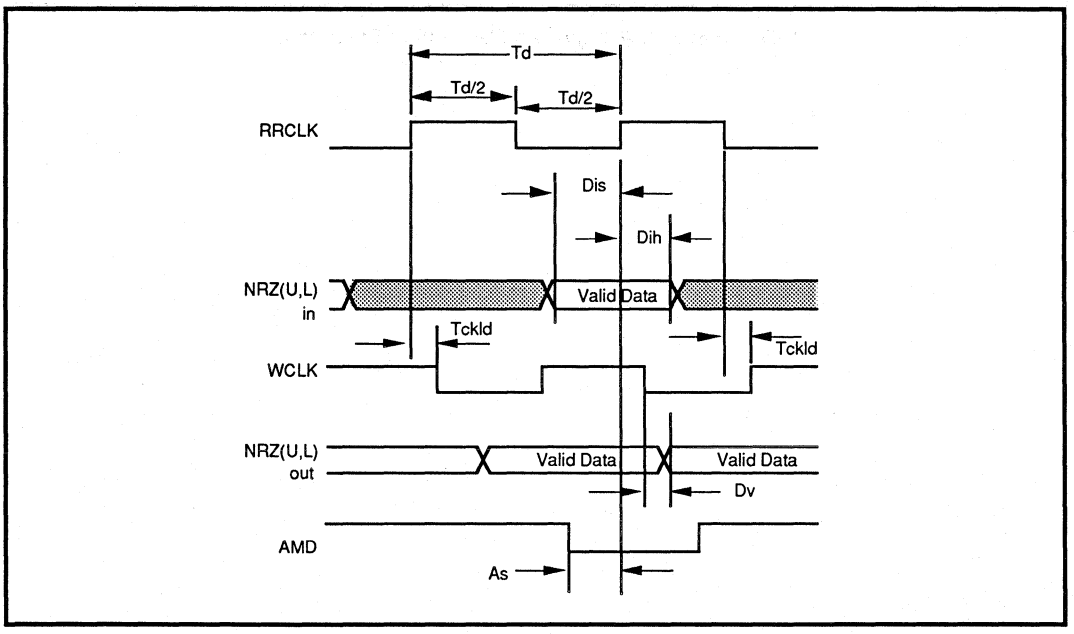


FIGURE 7: Disk Interface Timing

BUFFER MEMORY READ/WRITE TIMING PARAMETERS (Figures 8 through 13)

PARAMETER		MIN	MAX	UNIT
T	SYSCLK period	25		ns
T/2	SYSCLK high/low time	10		ns
Tav	SYSCLK ↑ to address valid (Note 1)		18	ns
Tmsv	SYSCLK ↑ to $\overline{MS}$↓ (Notes 1, 6)		18	ns
Tmsh	SYSCLK ↑ to $\overline{MS}$↑ (Note 1)		18	ns
Tmv	SYSCLK ↑ to $\overline{MOE}$↓ (Note 1)		18	ns
Tmh	SYSCLK ↑ to $\overline{MOE}$↑ (Note 1)		18	ns
Twv	SYSCLK ↑ to $\overline{WE}$↓ (Note 1)		18	ns
Twh	SYSCLK ↑ to $\overline{WE}$↑ (Note 1)		18	ns
Tdov	SYSCLK ↑ to data out valid (Note 1)		18	ns
Tdoh	SYSCLK ↑ to data out invalid (Note 1)		18	ns
Tdis	Data in valid to $\overline{MOE}$ ↑ (SRAM) Data in valid to $\overline{CAS}$ ↑ (DRAM)	5		ns
Tdih	$\overline{MOE}$ ↑ to data in valid (SRAM) $\overline{CAS}$ ↑ to data in valid (DRAM)	0		ns
Trv	SYSCLK ↑ to $\overline{RAS}$↓ (Note 1)		18	ns
Trh	SYSCLK ↑ to $\overline{RAS}$↑ (Note 1)		18	ns
Trav	SYSCLK ↑ to row address valid (Note 1)		18	ns
Trah	SYSCLK ↑ to row address invalid (Note 1)		18	ns
Tcv	SYSCLK ↑ to $\overline{CAS}$↓ (Note 1)		18	ns
Tch	SYSCLK ↑ to $\overline{CAS}$↑ (Note 1)		18	ns
Tcav	SYSCLK ↑ to column address valid (Note 1)		18	ns
Tcah	SYSCLK ↑ to column address invalid	0		ns

ELECTRICAL SPECIFICATIONS (continued)

BUFFER MEMORY READ/WRITE FUNCTIONAL PARAMETERS (Figures 8 through 13) (continued)

PARAMETER		CONDITIONS	MIN	UNIT
Trwl	$\overline{RAS}\downarrow$ to $\overline{RAS}\uparrow$	Notes 2, 3	((RWL + 3)•T)	ns
Trwh	$\overline{RAS}\uparrow$ to $\overline{RAS}\downarrow$	Notes 2, 4	((RWH + 1)•T)	ns
Tcwl	$\overline{CAS}\downarrow$ to $\overline{CAS}\uparrow$	Note 2	((CWL + 1)•T)	ns
Tcwl	$\overline{CAS}\uparrow$ to $\overline{CAS}\downarrow$	Notes 2, 5	((CWL + 1)•T)	ns

Note: Loading capacitance = 30 pF

Note 1: The measured delay for any of the signal indicated by this note will not vary from the measured delay of any other signal indicated by this note by more than ±2 ns.

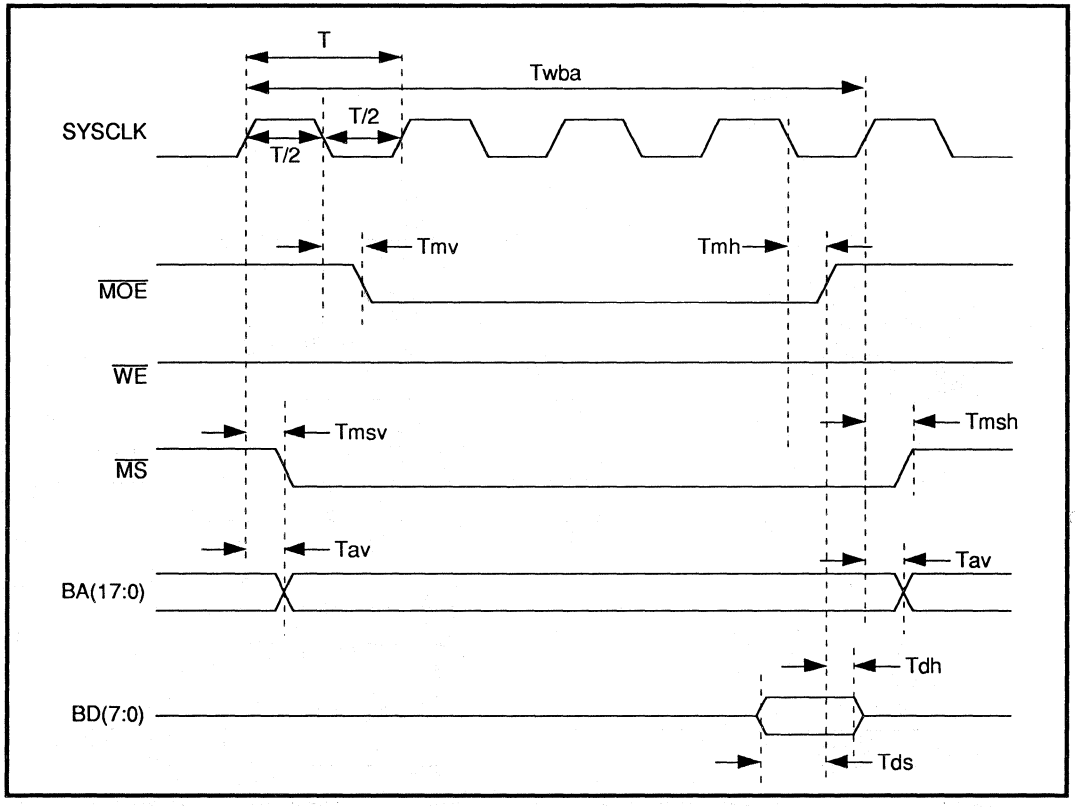
Note 2: RWL, RWH, CWL and CWH are fields in the Buffer Manager Timing Control Register (54H). Each is a two bit field which can contain a value of 0, 1, 2, or 3. These values determine the minimum number of SYSCLK periods (T) for the associated signal width.

Note 3: The minimum width value of Trwl will be generated for refresh cycles and for any buffer memory access cycle except when multiple page mode accesses are performed. When multiple page mode accesses are performed, the width of the $\overline{RAS}$ low pulse is extended until the end of the last $\overline{CAS}$ low cycle.

Note 4: The minumum value of Trwh will be generated whenever the Buffer Manager determines that a buffer request is pending at the completion of the current memory cycle and a page mode access can not be used either because page mode operation is not enabled or the needed location is not within the current page.

Note 5: The minumum value of Tcwh will be generated only between consecutive page mode accesses.

Note 6: $\overline{MS}$ will rise only if the Buffer Manager determines that no additional requests for buffer access are pending. If the Buffer Manager determines that another access is to be Made, $\overline{MS}$ is kept low between the accesses for improved speed.



Note: Twba is a functional parameter that gives the duration of one RAM data buffer access cycle in SYSCLK periods. The value is programmed in bits 1-0 of register 54H. These examples show Twba = 4T.

FIGURE 8: SRAM Read Timing

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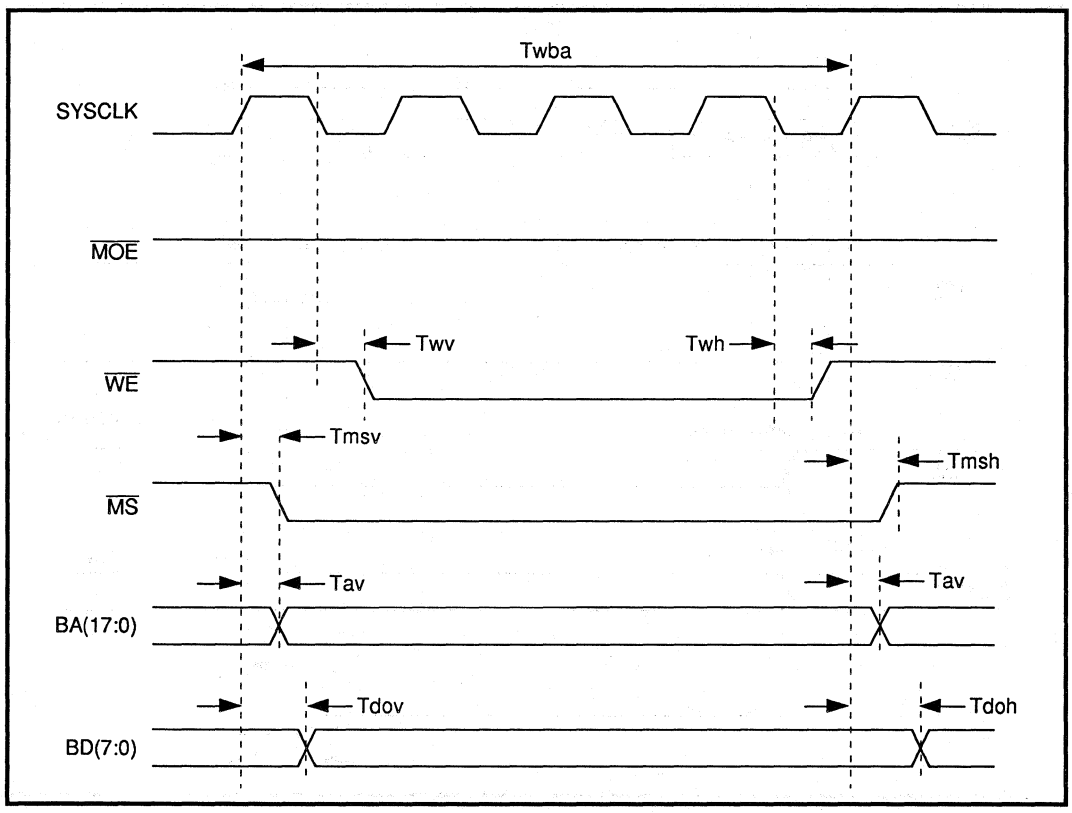

FIGURE 9: SRAM Write Timing

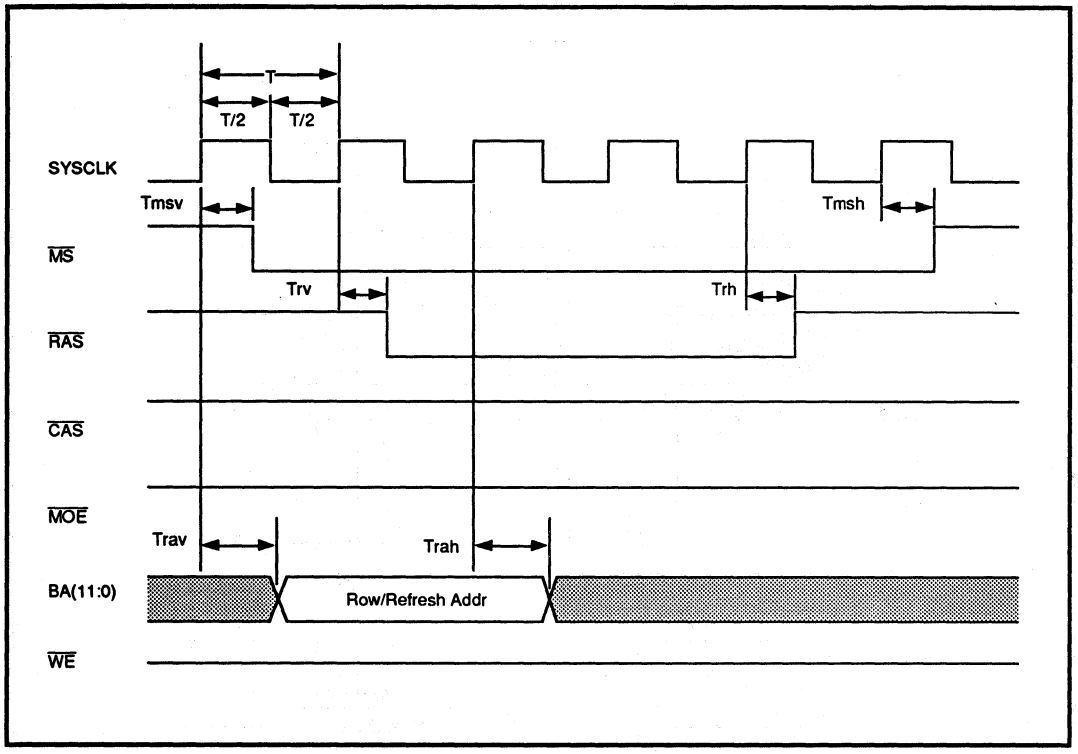

FIGURE 10: DRAM Timing, Refresh Cycle (Shown with WRL = 0)

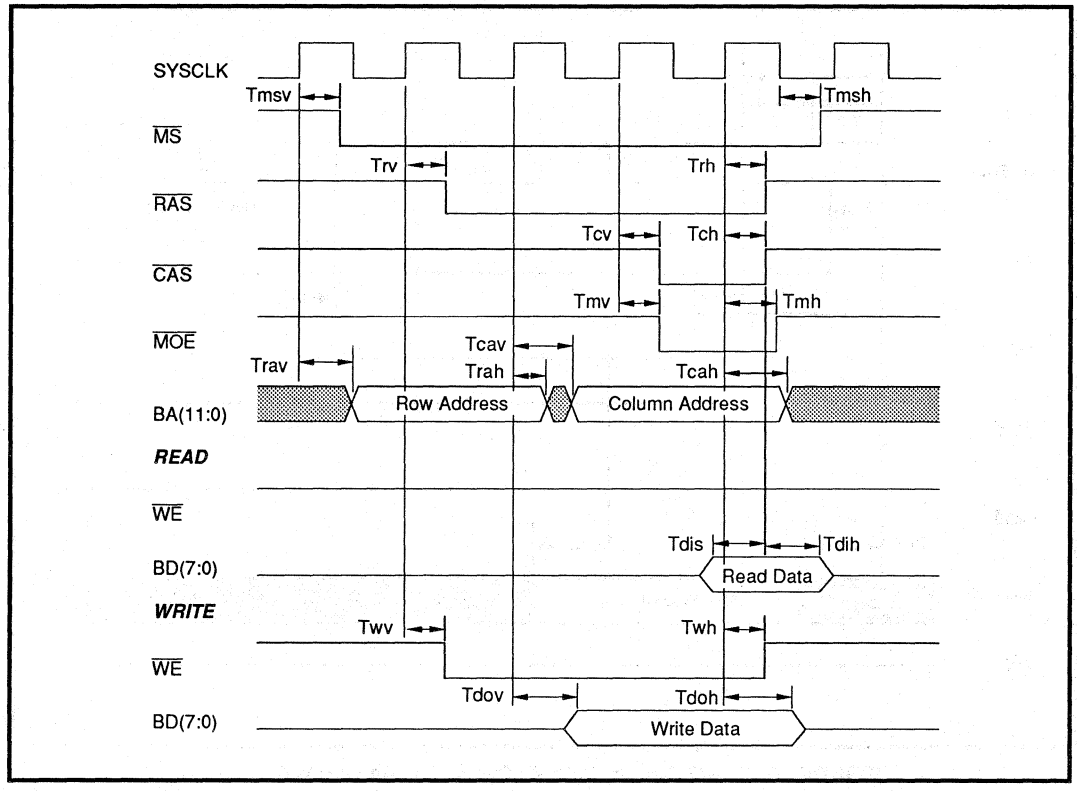

FIGURE 11: DRAM Timing, Standard Cycle (Shown with RWL = 0 and CWL = 0)

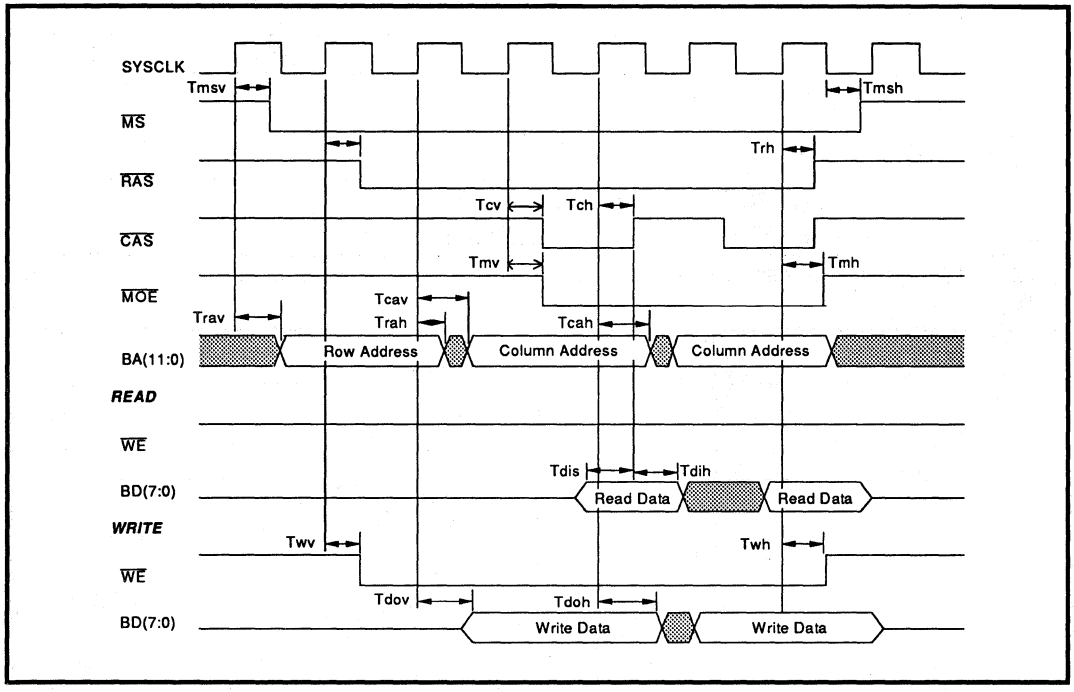

FIGURE 12: DRAM Timing, Fast Page Cycles (Shown with RWL = 0, RWH = 0, CWL = 0 and CWH = 0)

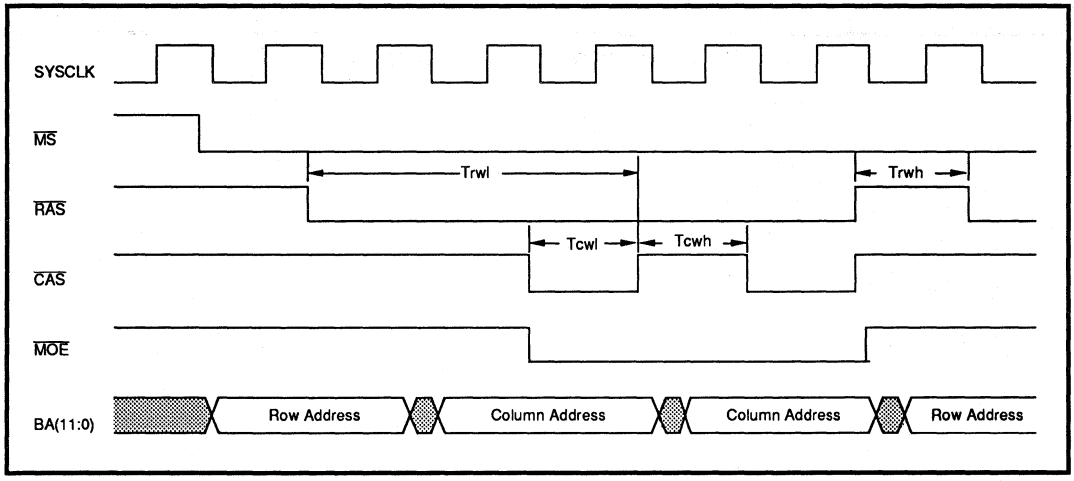

FIGURE 13: DRAM Timing (Showing the Relationship of RWL, RWH, CWL and CWH to overall timing)

SCSI Asynchronous Timing Paraemeters

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
Tods	Data Setup to $\overline{ACK}\downarrow$	SCSI Output Phase	5			ns
Todh	Data Hold from $\overline{ACK}\downarrow$	SCSI Output Phase	12			ns
Talrh	$\overline{ACK}\downarrow$ to $\overline{REQ}\uparrow$				49	ns
Tids	Data Setup to $\overline{REQ}\downarrow$	SCSI Input Phase	80			ns
Tidh	Data Hold from $\overline{ACK}\downarrow$	SCSI Input Phase	29			ns

Note: All timing parameters are measured with 200 pf load, two SCSI terminator loads with $\overline{ACK}$ Filter turned off.

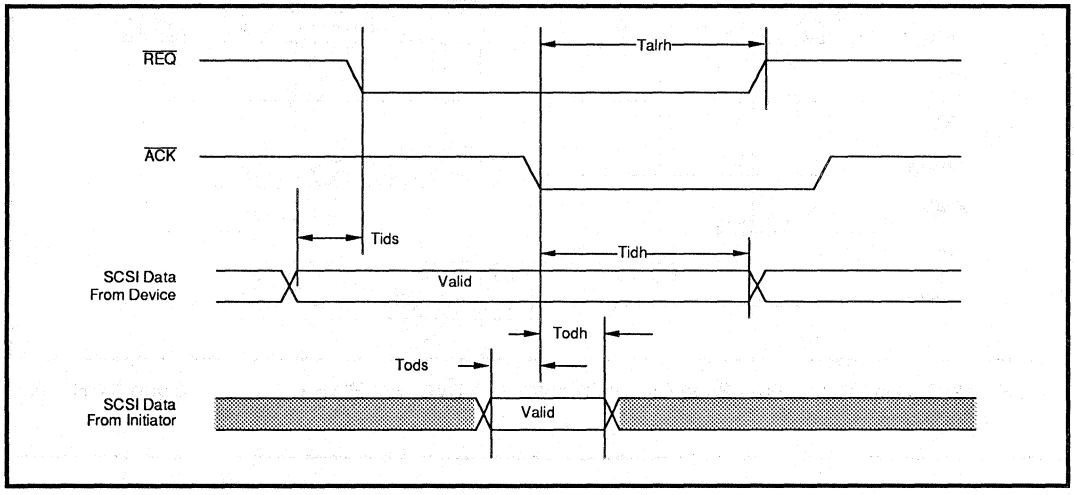

FIGURE 14: SCSI Asynchronous Timing

SCSI Synchronous Timing Paramenters

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
Trh	$\overline{REQ}$ Assertion Time		37		48	ns
Trl	$\overline{REQ}$ Deassertion Time		63		52	ns
Tids	Setup time SCSI Data to $\overline{REQ}\downarrow$	Write to SCSI bus	43			ns
Tidh	Hold time $\overline{REQ}\downarrow$ to SCSI Data invalid	Write to bus	43			ns
Tal	Minimum $\overline{ACK}$ Assertion Width Required		10			ns
Tods	Data Setup to $\overline{ACK}\downarrow$	Read from the SCSI bus	5			ns
Todh	Data Hold from $\overline{ACK}\downarrow$	Read from the SCSI bus	12			ns

Note: All timing parameters are measured with 200 pf load, two SCSI terminator loads, $\overline{ACK}$ filter turned off.

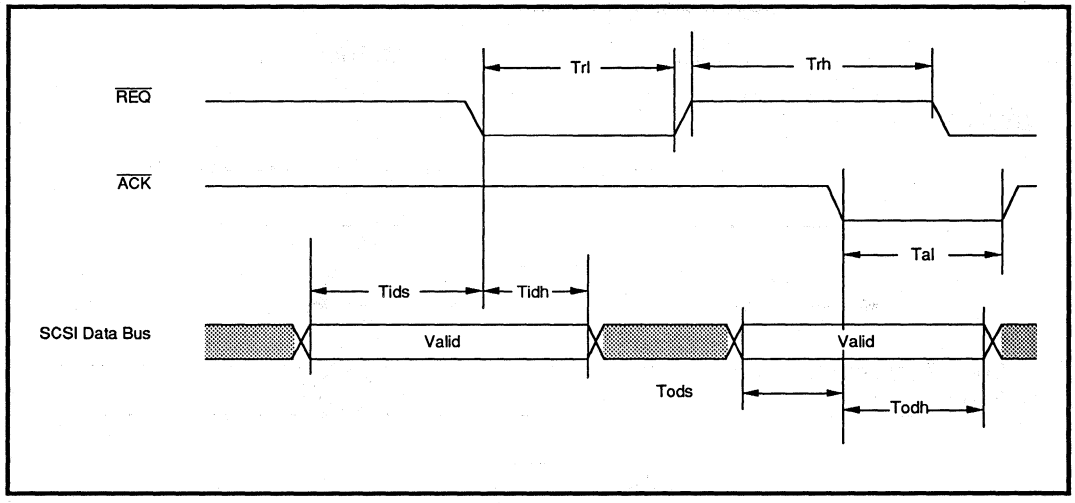

FIGURE 15: SCSI Synchronous Timing

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Synchronous Data In/Out Phase

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
Txtrp*	Synchronous Transfer Period	(see note)				ns
Tsrl	SYSFREQ high to $\overline{REQ}$ low				50	ns
Tsrh	SYSFREQ high to $\overline{REQ}$ high				60	ns
Tdov	SYSFREQ high to data out valid				40	ns
Tdsu	Data setup to $\overline{ACK}$ low		55			ns
Tdh	Data hold from $\overline{ACK}$ low		40			ns

Note: Txtrp is the Synchronous Transfer Period as defined by the Synchronous Control Register (Reg: 43H). SYSFREQ is a function of the BUFCLK and is determined by the prescale value as defined by the Clock Control Register (Reg: 49H).

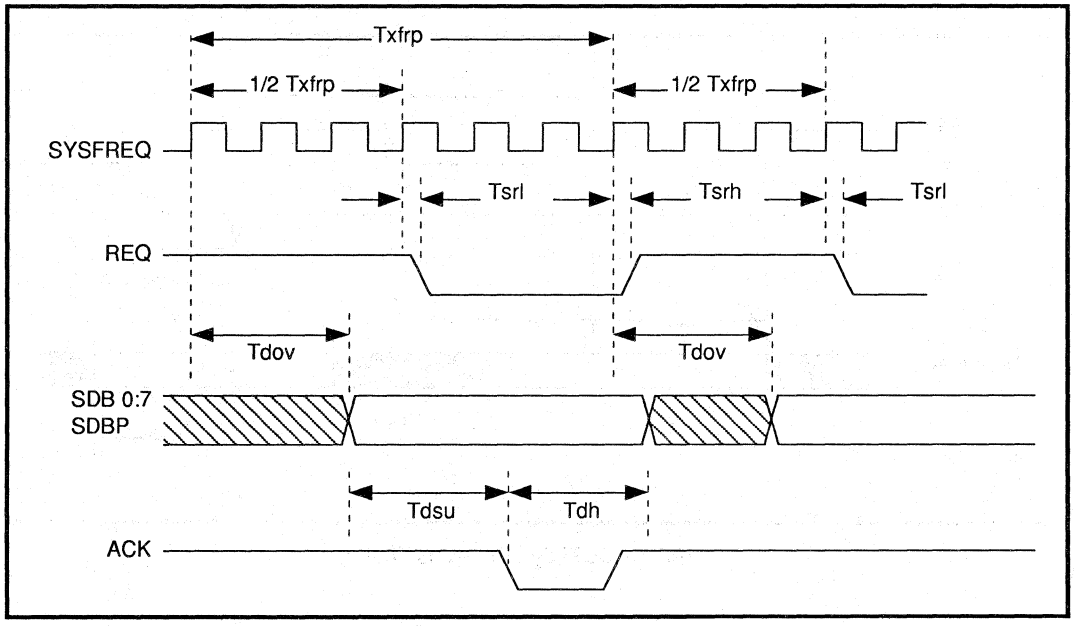


FIGURE 16: Even Number of SYSFREQ Cycles/SCSI Transfer Period

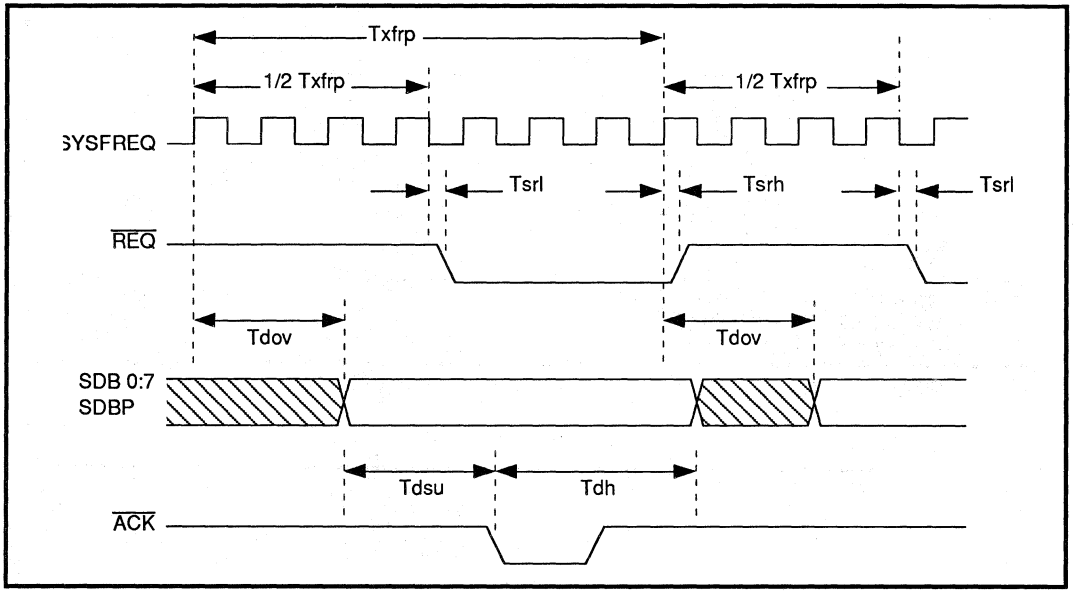


FIGURE 17: Odd Number of SYSFREQ Cycles/SCSI Transfer Period

Wait for Selection

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
Tbsd	Bus Settle Delay (400 ns) to the assertion of $\overline{BSY}$		3T + 90		4T + 90	ns

Note: T is the SCSI Clock Period (SCP) as defined in Register 49H (CLKCTL).

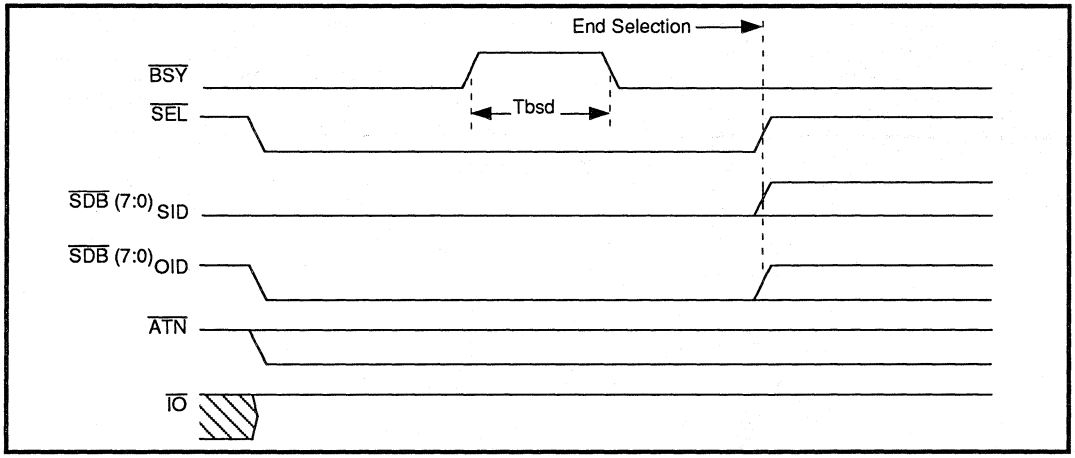


FIGURE 18: Wait for Selection

Arbitration

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
Tbfsd	Bus Settle Delay (400 ns) + Bus Free Delay (800 ns) to the assertion of BSY and $\overline{SDB}_{OID}$		6T + 110		7T + 110	ns
Tad	Arbitration Delay (2.4 µsec) to the assertion of $\overline{SEL}$ (win) or deassertion of $\overline{BSY}$ and $\overline{SDB}_{OID}$ (lost)		-		13T + 100	ns
Tbcsd	Bus Clear Delay (800 ns)+ Bus Settle Delay (400 ns) to end of Arbitration Phase		-		6T + 100	ns

Note: T is the SCSI Clock Period (SCP) as defined in Register 61H (CLKCTL).

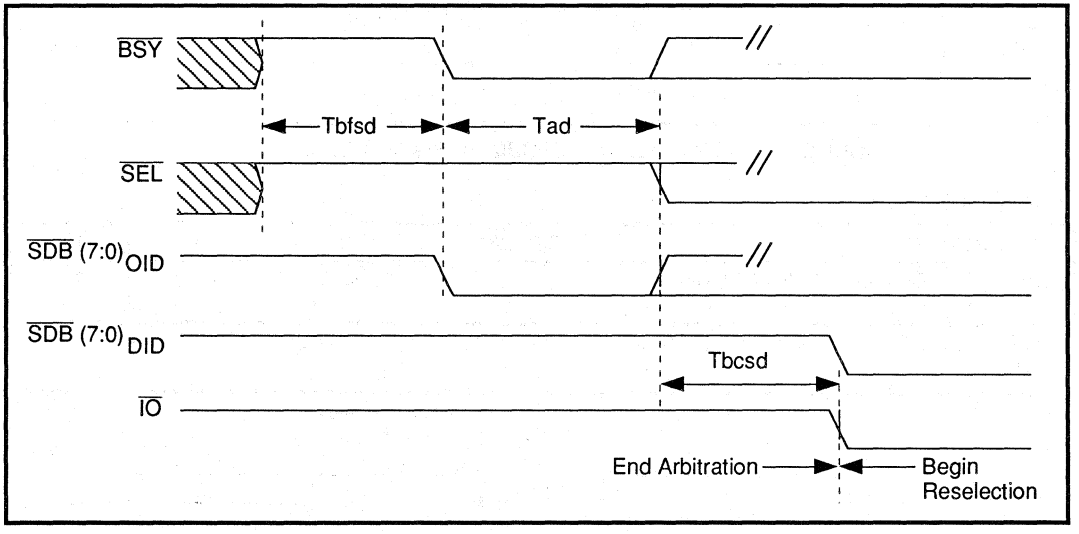


FIGURE 19: Arbitration

Reselection

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
Tbcsd	Bus Clear Delay (800 ns) + Bus Settle Delay (400 ns) to end of Arbitration Phase		-		6T + 100	ns
Tdskd1	Two Deskew Delays (90 ns) to the deassertion of $\overline{BSY}$		-		160	ns
Tbsd	Bus Settle Delay (400 ns) to the assertion of $\overline{BSY}$		-		2T + 40	ns
Tdskd2	Two Deskew Delays (90 ns) to the deassertion of SEL, $\overline{SDB}_{OID}$, and $\overline{SDB}_{DID}$		1T +70		2T + 70	ns

Note: T is the SCSI Clock Period (SCP) as defined in Register 61H (CLKCTL).

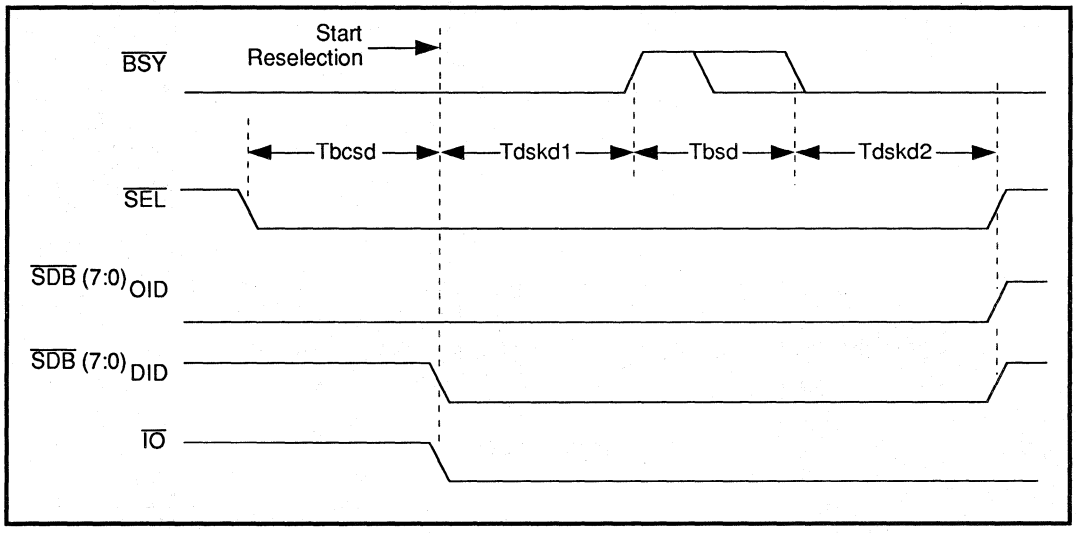
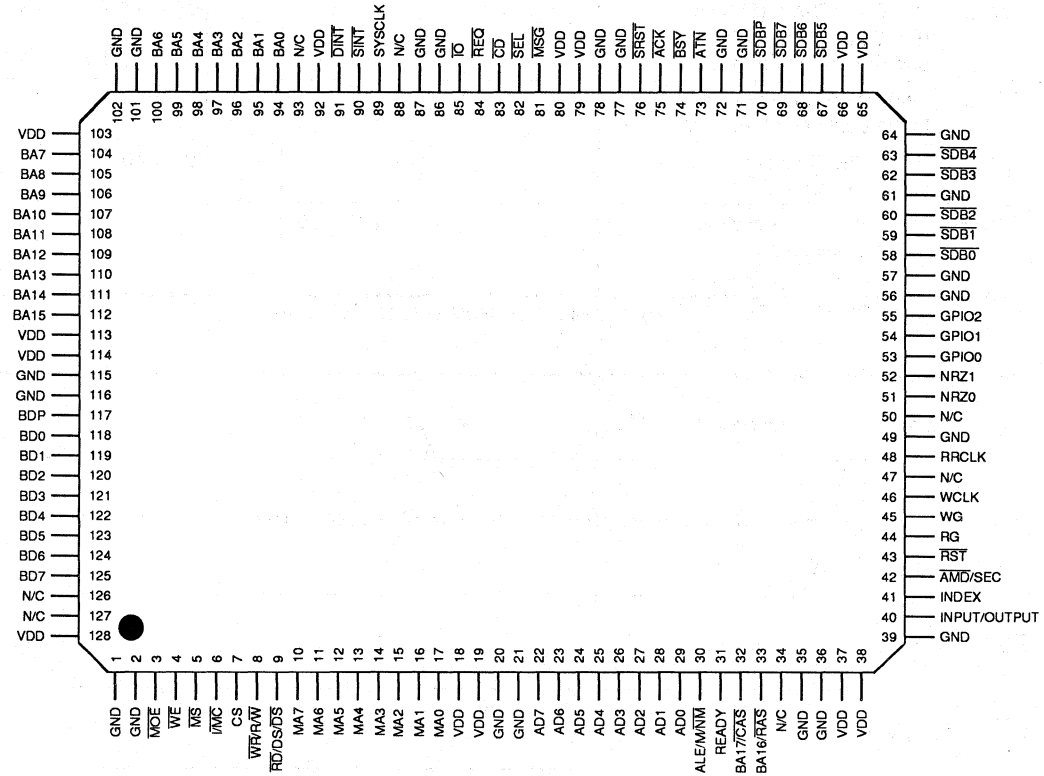


FIGURE 20: Reselection

SSI 32C9022
SCSI Combo Controller
48 Mbit/s; dual bit NRZ interface

PACKAGE PIN DESIGNATIONS

(Top View)



128-Lead QFP

CAUTION: Use handling procedures necessary for a static sensitive component.

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX: (714) 573-6914

silicon systems®
A TDK Group Company

SSI 32C9023
SCSI Combo Controller
80 Mbit/s; dual bit NRZ interface
Advance Information

January 1994

DESCRIPTION

The SSI 32C9023 is an advanced CMOS VLSI device which integrates major portions of the hardware needed to build a SCSI disk drive. The circuitry of the SSI 32C9023 includes a complete SCSI target interface, an advanced buffer manager, a high performance disk formatter and an 88 bit Reed-Solomon ECC with fast "on-the-fly" hardware correction. The SSI 32C9023 provides maximum performance while minimizing micro controller intervention.

The SSI 32C9023 provides a dual bit interface to the ENDEC. The dual bit Interface allows an effective transfer rate of up to 80 megabits per second on the disk interface by utilizing two parallel NRZ data signals and a clock rate of 40 MHz. The reduction of overall clock rates between the SSI 32C9023 and the ENDEC can be of great benefit to the designer.

The SSI 32C9023 can sustain concurrent transfers of up to 80 megabits per second transfer rate to the disk and 10 megabytes per second across the SCSI bus.

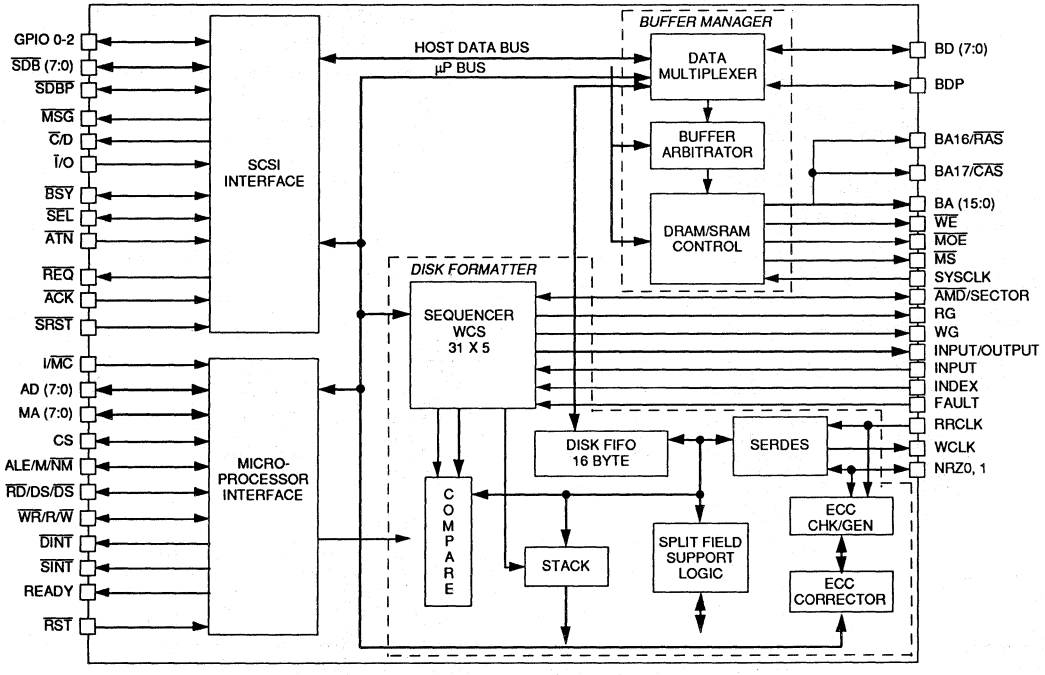
(continued)

FEATURES

- **SCSI Bus Interface**
  - **Full SCSI-2 Compatibility**
  - **Direct bus interface logic with on-chip 48 mA drivers**
  - **Synchronous transfer rates up to 10 megabytes per second**
  - **Asynchronous transfer rates up to 5 megabytes per second**
  - **Parity generation and checking**
  - **Auto Command Mode (ACM) SCSI state machine performs high level SCSI sequences without microprocessor intervention**
  - **Four level ACM command FIFO supports automatic execution of multiple ACM commands**
  - **Hardware support for automatic handling of SCSI-2 command queuing**
  - **Automatic SCSI CDB size determination**
  - **Automatic SCSI Disconnect and Reconnect**
  - **Sixteen byte data FIFO between SCSI channel and Buffer Manager**

(continued)

BLOCK DIAGRAM



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SSI 32C9023
SCSI Combo Controller
80 Mbit/s; dual bit NRZ interface

DESCRIPTION (continued)

The SSI 32C9023 is one of a family of Silicon Systems' single chip disk controllers which support a wide range of device interfaces. The SSI 32C9020 is similar to the SSI 32C9023, but is contained in a 100-pin package, giving up some features for size. The SSI 32C9022 is pin compatible with the SSI 32C9023 but supports disk data transfer rates up to only 48 megabits per second with a dual bit or single bit NRZ disk formatter interface. Other family members support AT and PCMCIA interfaces. The Silicon Systems' chip family is illustrated in the hierarchy chart shown in Figure 1. All members are based on a common architecture allowing major portions of firmware to be reused.

The high level of integration within the SSI 32C9023 represents a major reduction in parts count. When the SSI 32C9023 SCSI Controller is combined with the SSI 32R2110 Read/Write device, the SSI 32P4782 combination read channel, SSI 32D4680 time base generator, the SSI 32H4631 Servo and Motor Speed Controller, an appropriate microcontroller and memory, a complete, cost efficient, high performance intelligent drive solution is created.

FEATURES (continued)

- Buffer Manager
  - Direct support of DRAM or SRAM
    - SRAM throughput to 20 megabytes per second
    - SRAM size up to 256k bytes
    - DRAM throughput to 17.78 megabytes per second
    - DRAM size up to 1 megabyte
  - Programmable memory timing
  - Buffer RAM segmentation with flexible segment sizes from 256 bytes to 1 megabyte
  - Dedicated host, disk and microprocessor address pointers
  - Internal buffer protection circuit provides buffer integrity
- Disk Formatter
  - Dual bit NRZ interface
  - Effective data rates to 80 megabits/s
  - Automatic multi-sector transfer
  - Header or microprocessor based split data field support
  - Advanced sequencer organized in 31 x 5 bytes
  - 88-bit Reed Solomon ECC with "on-the-fly" fast hardware correction circuitry
  - Capable of correcting up to four 10-bit symbols in error

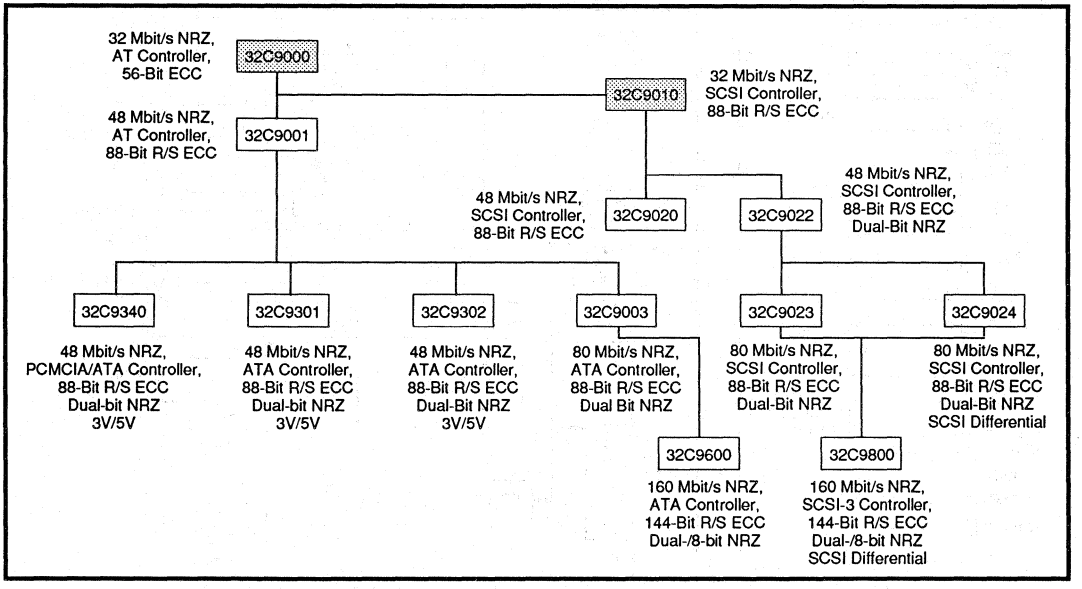

FIGURE 1: Silicon Systems' Single Chip Controller Hierarchy

  - Guaranteed to correct one 31-bit burst or two 11-bit bursts
  - Hardware on-the-fly correction of an 11-bit single burst error within a half sector time
  - Detects up to one 51-bit burst or three 11-bit bursts
- Microprocessor Interface
  - Supports both multiplexed or non-multiplexed microprocessors
  - Separate or combined host and disk interrupts
  - Programmable wait state insertion
- Other Features
  - Internal Power Down modes
  - Available in 128-lead QFP

FUNCTIONAL DESCRIPTION

The SSI 32C9023 contains the following four major functional blocks:

Microcontroller Interface
SCSI Interface
Disk Formatter
buffer manager

The microprocessor interface allows the local microprocessor access to all of the SSI 32C9023 internal control registers and any location within the buffer memory. The microprocessor, by writing and reading the internal registers can control all activities of the SSI 32C9023. The microprocessor can elect to perform SCSI and/or disk operations directly, or it can enable the advanced features of the SSI 32C9023 which can perform all typical operations automatically.

The SCSI Interface block handles all SCSI activities. The SCSI interface includes 48 mA drivers allowing for direct connection of the SSI 32C9023 to the SCSI bus. The SCSI interface logic includes Auto Command Mode (ACM) logic, an advanced state machine capable of handling a variety of complex SCSI sequences without microprocessor intervention. The microprocessor can queue up to four ACM commands into the ACM Command FIFO to create even more sophisticated command sequences. The SCSI block interfaces directly with the buffer manager via an internal speed matching FIFO. This FIFO, plus the bandwidth capabilities of the buffer manager guarantee sustained full speed transfers across the SCSI bus. The high level of automation of the ACM minimizes SCSI bus overhead. The net result is maximized performance with minimum SCSI bus bandwidth utilization.

The disk formatter performs the serialization and deserialization of data. If provides all of the necessary functions to control track formatting, header search, and the reading and writing of data. The heart of the disk formatter is an advanced programmable sequencer which is flexible enough to interface to a wide variety of read/write channels. The sequencer can contain 31 instructions, each of which is 5 bytes (40 bits) in width. The width of the instructions allows for sophisticated branching techniques which increase the flexibility and power of the sequencer. The flexible disk interface can be configured through a wide range of capabilities. This allows the SSI 32C9023 to interface with nearly any read/write channel and allows the user of the SSI 32C9023 to select the read/write channel best suited to the device. Of course, by selecting the SSI 32P4782 combination Read Channel, you are guaranteed a problem free interface.

Within the disk formatter are the ECC generator/checker and ECC corrector. The generator/checker provides the ability to generate or check a 32 bit ECC for headers and an 88 bit Reed Solomon code for data. If the checker detects an error in an 88 bit Reed Solomon data field, the syndrome information is transferred into the corrector. The corrector performs the necessary operations to determine if the error was correctable and interfaces directly with the buffer controller to perform the correction automatically. The corrector performs its correction within one half of a sector time. This gaurantees that the corrector will always be available to correct the next sector if necessary.

As its name implies, the buffer manager manages the data buffer of the controller. The buffer manager can support either SRAM or DRAM. When configured to operate with DRAM, the buffer manager automatically performs necessary refresh cycles. The buffer manager creates all of the necessary timing and control signals for a wide range of memory types and speeds. The buffer manager interfaces with the buffer memory, the SCSI Interface block, the data path of the disk formatter block, the ECC corrector and the microprocessor. If more than one of these devices requires access to the buffer memory, the buffer manager arbitrates the requests automatically. The buffer manager of the SSI 32C9023 can sustain SCSI operations at the rate of 10 megabytes per second, disk formatter operations at 80 megabits per second (10 megabytes per second).

PIN DESCRIPTION

The following convention is used in the pin description:

(I) denotes an input
(O) denotes an output
(Z) denotes a tri-state output
(OD) denotes an open drain output

GENERAL

NAME	TYPE	DESCRIPTION
VDD		POWER SUPPLY PIN
GND		GROUND

HOST INTERFACE

$\overline{SDBP}$	I/O	SCSI DATA BUS PARITY. Odd parity bit for the SCSI data bus.
$\overline{SDB(7:0)}$	I/O	SCSI DATA BUS BITS 7-0.
$\overline{ATN}$	I	ATTENTION. This active low signal is used by the initiator to request a message out phase.
$\overline{BSY}$	I/O	BUSY. This active low signal is used to indicate when the bus is active.
$\overline{ACK}$	I	ACKNOWLEDGE. This active low signal is used in the handshake protocol to indicate the completion of a data byte transfer.
$\overline{SRST}$	I	SCSI RESET. This active low signal is used to reset the SCSI controller.
$\overline{MSG}$	O	MESSAGE. This active low signal is used to indicate a message phase.
$\overline{SEL}$	I/O	SELECT. This active low signal is used to indicate either a selection or reselection phase.
$\overline{C}$/D	O	COMMAND/DATA. This signal is used to indicate either a command or data phase.
$\overline{REQ}$	I	REQUEST. This active low signal is used in the handshake protocol to initiate a data byte transfer.
$\overline{I}$/O	I	INPUT/OUTPUT. This signal is used to indicate the direction of data transfer.
GPIO(2:0)	I/O	INPUT/OUTPUT. These pins are used to indicate the SCSI ID of the target device. The pins can be programmed as outputs for test purposes only.

DISK INTERFACE

INDEX	I	INDEX. Input for index pulse received from the drive.
INPUT/ OUTPUT	I/O	DISK SEQUENCER INPUT/OUTPUT. A general purpose control (output) and status (input) pin configured by the Output Enable Bit of Register 71H, bit 7. At power-on, this pin is an input. As an input, it can be used to synchronize the disk sequencer to an external event. As an output, it is controlled by bit 2 of the Control Field of the disk sequencer.
INPUT	I	INPUT. This pin can be used to synchronize the disk to an external event.
$\overline{AMD}$/ SECTOR	I/O	ADDRESS MARK DETECT/SECTOR. This pin is used in the hard sector mode as the sector input. A pulse on this pin indicates a sector mark is found. In the soft sector mode, a low-level input indicates an address mark was detected. The device powers up in soft sector default mode.

DISK INTERFACE (continued)

NAME	TYPE	DESCRIPTION
RG	O	READ GATE. During disk data read, this pin is asserted. Active high.
WG	O	WRITE GATE. During disk data write, this pin is asserted. Active high.
RRCLK	I	READ/REFERENCE CLOCK. This is a clock signal generated from an external data synchronizer. This clock is used to synchronize the input NRZ data and clock the disk formatter of the chip.
WCLK	O	WRITE CLOCK. This signal clocks the NRZ data out in the dual NRZ interface mode.
NRZ1	I/O	NON RETURN TO ZERO 1. In dual NRZ mode, this signal is the most significant bit read data input from the disk drive when the read gate signal is asserted; it is the most significant bit write data output to the disk drive when the write gate signal is asserted. In single NRZ mode, this signal is not used and should be grounded. NRZ1 is the leading bit of the bit pair. In Write mode, the MSB of the data bytes always appears on NRZ1.
NRZ0	I/O	NON RETURN TO ZERO. In dual NRZ mode, this signal is the least significant bit read data input from the disk drive when the read gate signal is asserted; it is the least significant bit write data output to the disk drive when the write gate signal is asserted. In single NRZ mode, this signal is used to transfer NRZ data to/from the read channel chip.
FAULT	I	FAULT. This input when asserted indicates to the chip that a fault has occured with the disk. The disk sequencer will stop and both RG and WG pins will be deasserted.

MICROPROCESSOR INTERFACE

$\overline{RST}$	I	RESET. An asserted low input generates a component reset that holds the internal registers at reset, stops all operations within the chip, and deasserts all output signals. All input/output signals are set to the high-Z state during the assertion of this signal.
ALE/M/$\overline{NM}$	I	ADDRESS LATCH ENABLE/MULTIPLEXED/NON-MULTIPLEXED ADDRESS SELECT. When tied high or left floating after reset, the microprocessor interface is configured as non-multiplexed. When driven low, then the microprocessor interface is configured as multiplexed. In this case this pin functions as the address latch enable, and the MA(7:0) pins are the demultiplexed address outputs.
CS	I	CHIP SELECT. Active high signal, when asserted, the internal registers of the SSI 32C9022 can be accessed.
$\overline{WR}$/R/$\overline{W}$	I	WRITE STROBE/READ/WRITE. In the Intel bus mode, when an active low signal is present with CS signal high, the data is written to the internal registers. In the Motorola bus mode, this signal acts as the R/$\overline{W}$ signal.
$\overline{RD}$/DS/$\overline{DS}$	I	READ STROBE/DATA STROBE. When the Intel bus control interface is selected (the I/$\overline{MC}$ is high), this signal acts as the $\overline{RD}$ signal. When the read strobe signal is asserted low and the CS signal is asserted high, the data from the specified register will be driven to the AD signals. When the Motorola bus control interface is selected (the I/$\overline{MC}$ is low) this signal acts as the data strobe signal. A high on the R/$\overline{W}$ signal along with this signal asserted and the CS signal asserted high indicates a read operation. A low on the R/$\overline{W}$ signal along with this signal asserted and the CS signal asserted high indicates a write operation. Note when non-multiplexed Mototrola bus configuration is chosen, the data strobe is an active low input.
$\overline{DINT}$	O, OD,Z	DISK INTERRUPT. An active low signal indicates the controller is requesting microprocessor service from the disk side. This signal is programmable for either a push-pull or open-drain output circuit. This signal powers up in the high-Z state. Register 4F bit 3 enables the pull-up.

MICROPROCESSOR INTERFACE (continued)

NAME	TYPE	DESCRIPTION
$\overline{SINT}$	O, OD,Z	SCSI INTERRUPT. This signal is generated by the SCSI controller and is an interrupt line to the microprocessor. It is programmable for either a push-pull or open drain output circuit. This signal powers up in the high-Z state. The interrupt is sourced from the SCSI Interrupt Register. Register 4F bit 3 enables the pull-up. This signal is also programmable to be either an active high or low interrupt.
AD(7:0)	I/O	ADDRESS/DATA BUS. When configured in the Intel mode, these lines are multiplexed, bidirectional microprocessor register address and data lines. When configured in the Motorola mode, these lines are bidirectional data lines.
MA(7:0)	I/O	MICROPROCESSOR ADDRESS BUS: These signals are nonmultiplexed address input or latched address output lines.
READY	O	READY: When this signal is deasserted low, the microprocessor shall insert wait states to allow time for the chip to respond.
I/$\overline{MC}$	I	INTEL/MOTOROLA: This signal selects the microprocessor interface to be used. When this signal is asserted high, it selects the Intel bus control interface. When this signal is deasserted low, it selects the Motorola bus control interface. This signal has an internal pull-up to allow the default selection of the Intel bus control interface.

BUFFER MANAGER INTERFACE

BA(15:0)	O	BUFFER MEMORY ADDRESS LINES 15 through 0. Active high, for direct connection to a Static or Dynamic RAM address lines.
BA16/$\overline{RAS}$	O	BUFFER MEMORY ADDRESS 16: In SRAM mode, for direct connection to a Static RAM address line 16. ROW ADDRESS STROBE: In DRAM mode, for direct connection to a Dynamic RAM Row Address Strobe signal.
BA17/$\overline{CAS}$	O	BUFFER MEMORY ADDRESS 17: In SRAM mode, for direct connection to a Static RAM address line 17. ROW ADDRESS STROBE: In DRAM mode, active low, for direct connection to a Dynamic RAM Column Address Strobe signal.
BD(7:0)	I/O	BUFFER MEMORY DATA BUS. 7 through 0. Active high, buffer data bus that connects directly to the buffer RAM data lines.
BDP	I/O	BUFFER MEMORY DATA PARITY. This signal provides odd parity for the buffer memory data bus during transfers to/from the buffer memory to the buffer RAM.
$\overline{MOE}$	O	MEMORY OUTPUT ENABLE. In SRAM mode this signal is asserted low when every buffer memory access is active. In DRAM mode this signal is asserted low only for buffer memory read operation.
$\overline{MS}$	O	MEMORY SELECT. An active low signal indicates external memory is selected.
$\overline{WE}$	O	WRITE ENABLE. Active low, write enable for the buffer RAM.
SYSCLK	I	SYSTEM CLOCK. This signal is used to synchronize the buffer RAM access, including the generation of memory address bits, write enable $\overline{WE}$, and memory output enable $\overline{MOE}$.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC operating characteristics.

PARAMETER	RATING
Power Supply Voltage, VCC	7V
Ambient Temperature	0 to 70°C
Storage Temperature	-65 to 150°C
Power Dissipation	750 mW
Input, Output pins	-0.5 to VCC+0.5V

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
VCC Power Supply Voltage		4.50		5.50	V
ICC Supply Current	Ta = 25°C Outputs Unloaded			50	mA
ICCS Supply Current				250	µA
VIL Input Low Voltage		-0.5		0.8	V
V0IH Input High Voltage		2.0		VCC+0.5	V
VOL Output Low Voltage	All pins except SCSI interface, IOL = 2 mA			0.4	V
VOL Output Low Voltage	SCSI interface pins, IOL = 48 mA			0.5	V
VOH Output High Voltage	IOH = -400 µA			2.4	V
IL Input Leakage Current	0 < VIN < VCC	-10		10	µA
CIN Input Capacitance				10	pF
COUT Output Capacitance				10	pF

MICROPROCESSOR INTERFACE TIMING

Multiplexed Interface Timing Parameters (Figures 2-5)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
Ta	ALE width		20			ns
Tma	Address valid to MA(7:0) valid				30	ns
Tr	$\overline{RD}$ width		80			ns
As	Address valid to ALE ↓		5			ns
Ah	ALE ↓ to address invalid		10			ns
Cs	CS valid to $\overline{RD}$ ↓ or DS ↑		20			ns
Ch	$\overline{RD}$ ↑ or DS ↓ to CS ↓		0			ns
Tda	$\overline{RD}$ ↓ or DS ↑ to read data valid				60	ns
Tds	DS width		80			ns
Tdh	$\overline{RD}$ ↑ or DS ↓ to read data invalid		0		25	ns
Tsrw	R/$\overline{W}$ valid to DS ↑		20			ns
Thrw	DS ↓ to R/$\overline{W}$ invalid		20			ns
Tdrdy	$\overline{RD}$ ↓ to READY ↓ (Intel) or DS ↑ to READY ↓ (Motorola)				30	ns
Wds	Write data valid to $\overline{WR}$ ↑ or DS ↓		40			ns
Wdh	$\overline{WR}$ ↑ or DS ↓ to write data invalid		10			ns

Note: ↑ indicates rising edge ↓ indicates falling edge

Non-Multiplexed Bus Interface Timings (Figure 6)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
Tmas	MA(7:0) valid to DS ↓		5			ns
Tmah	DS ↑ to MA(7:0) invalid		5			ns
Cs	CS valid to DS ↓		20			ns
Ch	DS ↑ to CS ↓		0			ns
Tda	DS ↑ to read data valid				60	ns
Tds	DS width		80			ns
Tdh	DS ↑ to read data invalid		0		25	ns
Tsrw	R/$\overline{W}$ valid to DS ↓		20			ns
Thrw	DS ↑ to R/$\overline{W}$ invalid		20			ns
Tdrdy	DS ↑ to READY ↓ (Motorola)				30	ns
Wds	Write data valid to $\overline{WR}$ ↑ or DS ↓		40			ns
Wdh	$\overline{WR}$ ↑ or DS ↓ to write data invalid		10			ns

Note 1: ↑ indicates rising edge ↓ indicates falling edge

Note 2: Loading capacitor = 30 pF

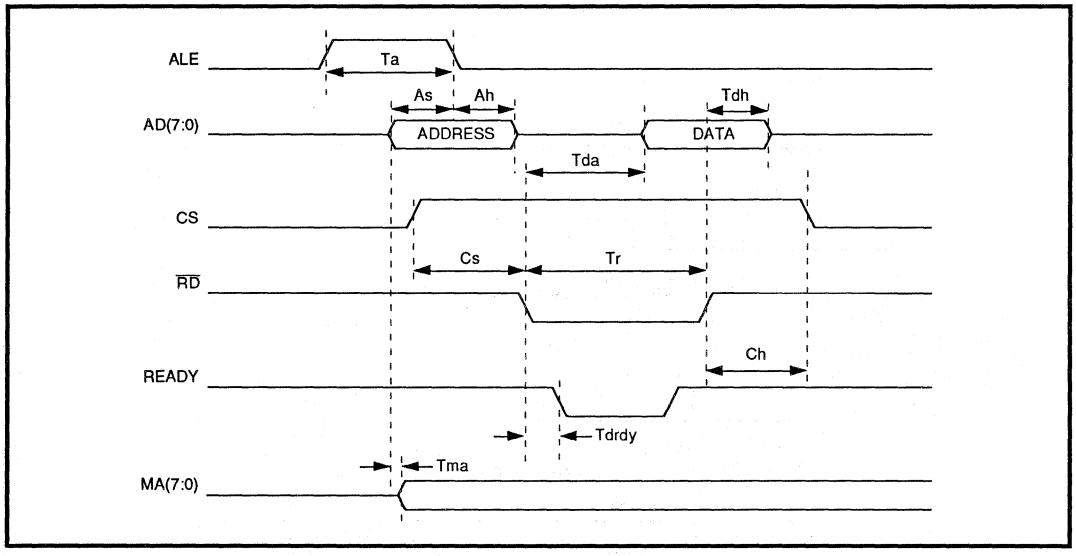

FIGURE 2: Intel Register Multiplexed Read Timing

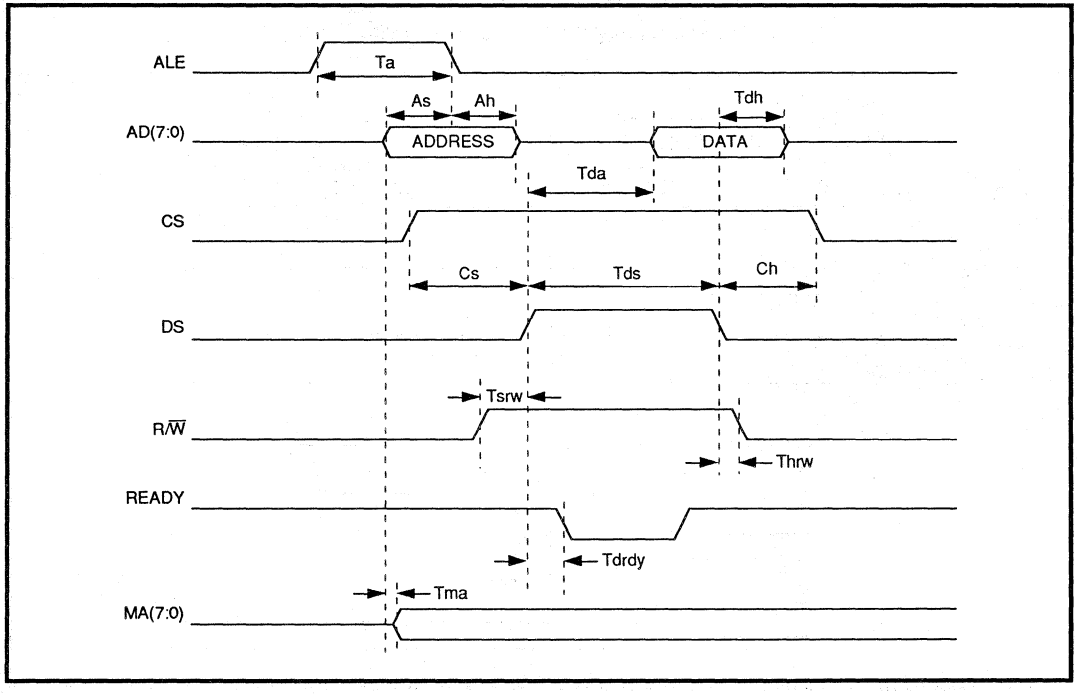

FIGURE 3: Motorola Register Multiplexed Read Timing

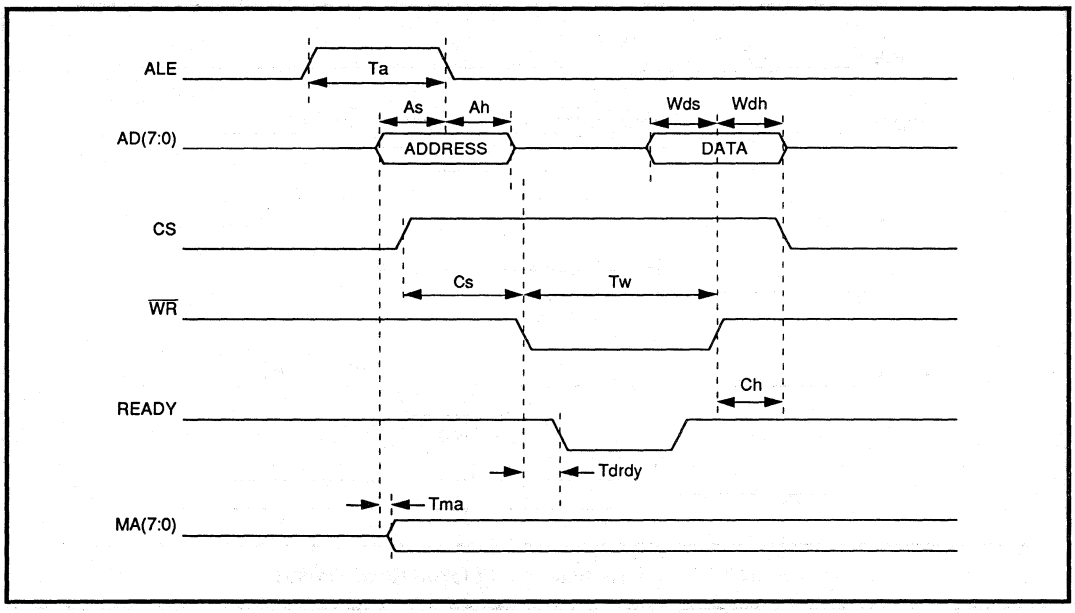

FIGURE 4: Intel Register Multiplexed Write Timing

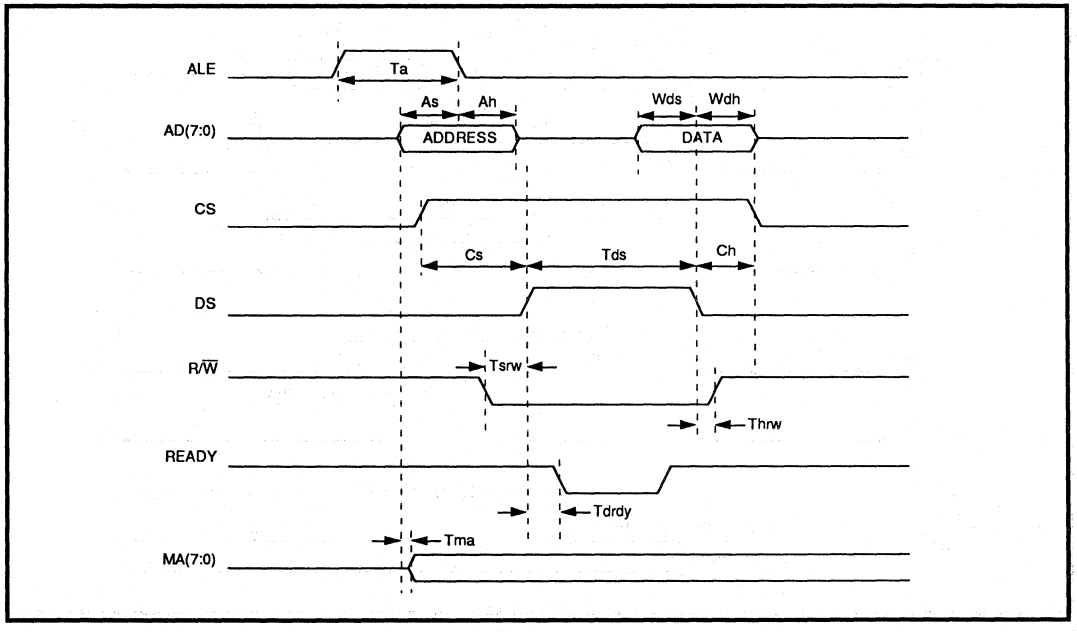

FIGURE 5: Motorola Register Multiplexed Write Timing

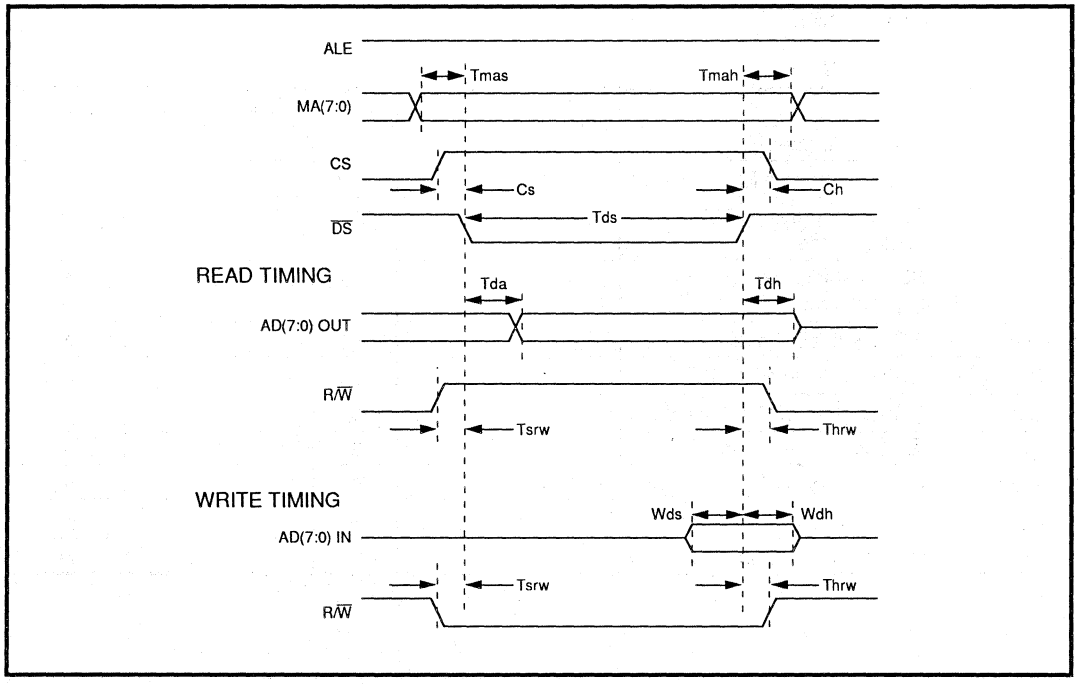

FIGURE 6: Non-Multiplexed Bus Timing Diagrams

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ELECTRICAL SPECIFICATIONS (continued)

Disk Interface Timing

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
T	Dual bit interface RRCLK period		25			ns
	Single bit interface RRCLK period		20.8			ns
T/2	Dual bit interface RRCLK high/low time		11.2			ns
	Single bit interface RRCLK high/low time		8.5			ns
Tr, Tf	RRCLK rise/fall time				3	ns
Dis	NRZ in valid to RRCLK ↑		3			ns
Dih	RRCLK ↑ to NRZ in invalid		3			ns
As	$\overline{AMD}$ valid to RRCLK ↑		3			ns
Tckd	RRCLK ↓ to WCLK ↓				8	ns
Dvr	RRCLK ↓ to NRZ out valid				18	ns
Dv	WCLK ↓ to NRZ out valid				±2	ns

Note: ↑ indicates rising edge ↓ indicates falling edge

Loading capacitor = 10 pF

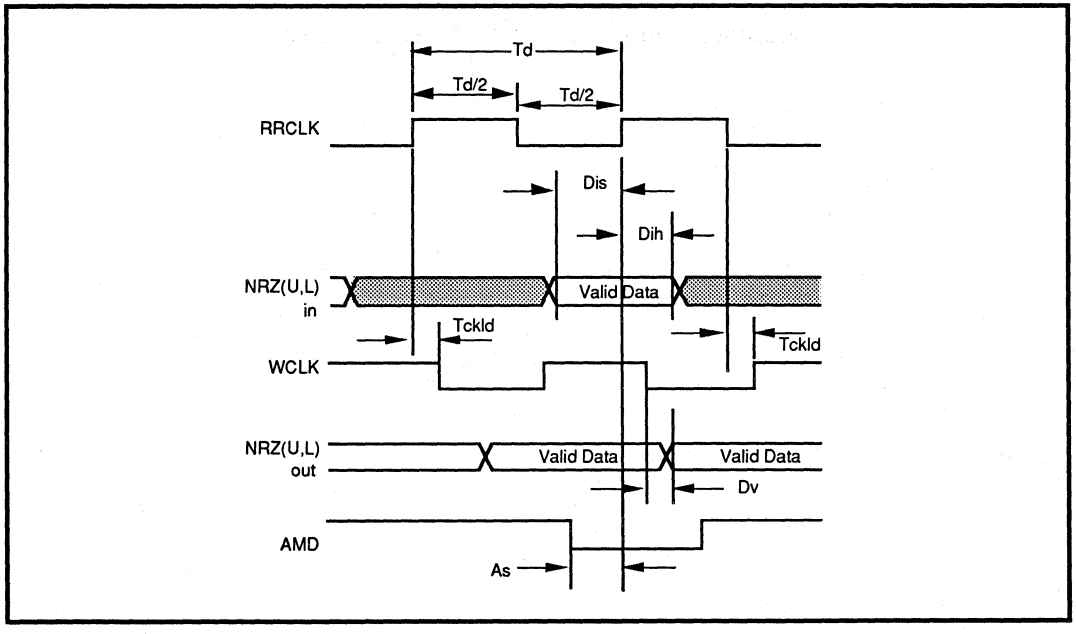


FIGURE 7: Disk Interface Timing

BUFFER MEMORY READ/WRITE TIMING PARAMETERS (Figures 8 through 13)

PARAMETER		MIN	MAX	UNIT
T	SYSCLK period	25		ns
T/2	SYSCLK high/low time	10		ns
Tav	SYSCLK ↑ to address valid (Note 1)		18	ns
Tmsv	SYSCLK ↑ to $\overline{MS}$↓ (Notes 1, 6)		18	ns
Tmsh	SYSCLK ↑ to $\overline{MS}$↑ (Note 1)		18	ns
Tmv	SYSCLK ↑ to $\overline{MOE}$↓ (Note 1)		18	ns
Tmh	SYSCLK ↑ to $\overline{MOE}$↑ (Note 1)		18	ns
Twv	SYSCLK ↑ to $\overline{WE}$↓ (Note 1)		18	ns
Twh	SYSCLK ↑ to $\overline{WE}$↑ (Note 1)		18	ns
Tdov	SYSCLK ↑ to data out valid (Note 1)		18	ns
Tdoh	SYSCLK ↑ to data out invalid (Note 1)		18	ns
Tdis	Data in valid to $\overline{MOE}$ ↑ (SRAM) Data in valid to $\overline{CAS}$ ↑ (DRAM)	5		ns
Tdih	$\overline{MOE}$ ↑ to data in valid (SRAM) $\overline{CAS}$ ↑ to data in valid (DRAM)	0		ns
Trv	SYSCLK ↑ to $\overline{RAS}$↓ (Note 1)		18	ns
Trh	SYSCLK ↑ to $\overline{RAS}$↑ (Note 1)		18	ns
Trav	SYSCLK ↑ to row address valid (Note 1)		18	ns
Trah	SYSCLK ↑ to row address invalid (Note 1)		18	ns
Tcv	SYSCLK ↑ to $\overline{CAS}$↓ (Note 1)		18	ns
Tch	SYSCLK ↑ to $\overline{CAS}$↑ (Note 1)		18	ns
Tcav	SYSCLK ↑ to column address valid (Note 1)		18	ns
Tcah	SYSCLK ↑ to column address invalid	0		ns

ELECTRICAL SPECIFICATIONS (continued)

BUFFER MEMORY READ/WRITE FUNCTIONAL PARAMETERS (Figures 8 thorugh 13) (continued)

PARAMETER		CONDITIONS	MIN	UNIT
Trwl	$\overline{RAS}\downarrow$ to $\overline{RAS}\uparrow$	Notes 2, 3	((RWL + 3)•T)	ns
Trwh	$\overline{RAS}\uparrow$ to $\overline{RAS}\downarrow$	Notes 2, 4	((RWH + 1)•T)	ns
Tcwl	$\overline{CAS}\downarrow$ to $\overline{CAS}\uparrow$	Note 2	((CWL + 1)•T)	ns
Tcwl	$\overline{CAS}\uparrow$ to $\overline{CAS}\downarrow$	Notes 2, 5	((CWL + 1)•T)	ns

Note: Loading capacitance = 30 pF

Note 1: The measured delay for any of the signal indicated by this note will not vary from the measured delay of any other signal indicated by this note by more than ±2 ns.

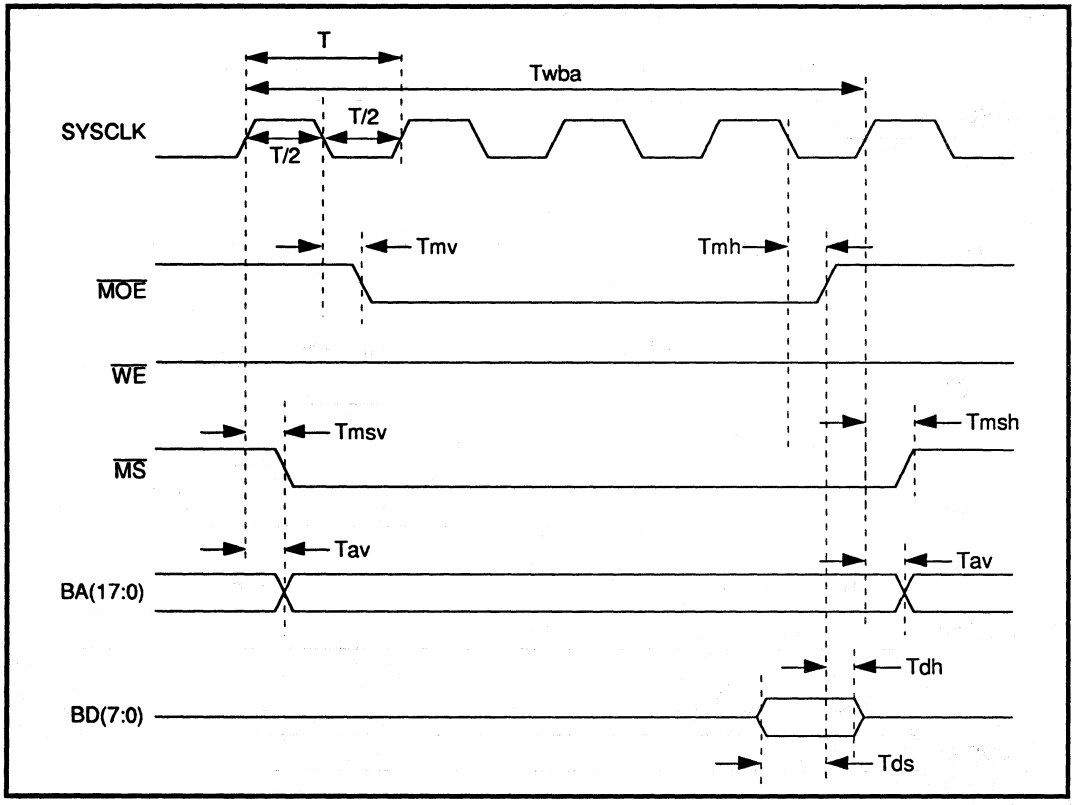
Note 2: RWL, RWH, CWL and CWH are fields in the Buffer Manager Timing Control Register (54H). Each is a two bit field which can contain a value of 0, 1, 2, or 3. These values determine the minimum number of SYSCLK periods (T) for the associated signal width.

Note 3: The minimum width value of Trwl will be generated for refresh cycles and for any buffer memory access cycle except when multiple page mode accesses are performed. When multiple page mode accesses are performed, the width of the $\overline{RAS}$ low pulse is extended until the end of the last $\overline{CAS}$ low cycle.

Note 4: The minumum value of Trwh will be generated whenever the Buffer Manager determines that a buffer request is pending at the completion of the current memory cycle and a page mode access can not be used either because page mode operation is not enabled or the needed location is not within the current page.

Note 5: The minumum value of Tcwh will be generated only between consecutive page mode accesses.

Note 6: $\overline{MS}$ will rise only if the Buffer Manager determines that no additional requests for buffer access are pending. If the Buffer Manager determines that another access is to be Made, $\overline{MS}$ is kept low between the accesses for improved speed.



Note: Twba is a functional parameter that gives the duration of one RAM data buffer access cycle in SYSCLK periods. The value is programmed in bits 1-0 of register 54H. These examples show Twba = 4T.

FIGURE 8: SRAM Read Timing

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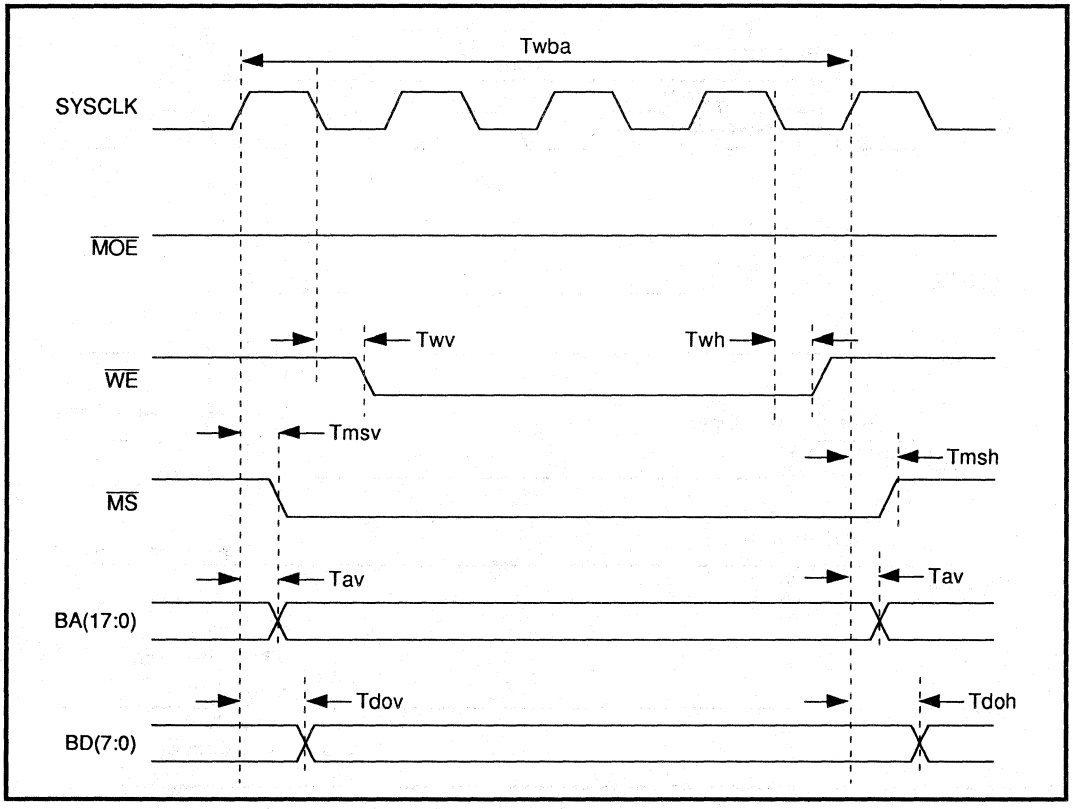

FIGURE 9: SRAM Write Timing

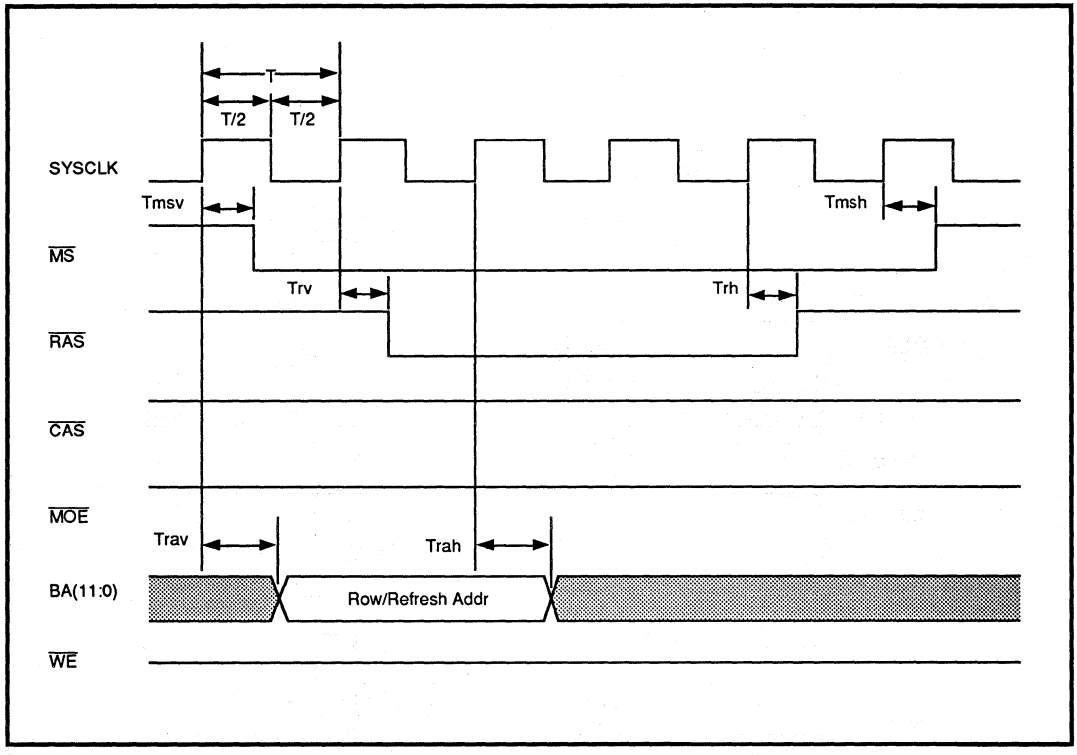

FIGURE 10: DRAM Timing, Refresh Cycle (Shown with WRL = 0)

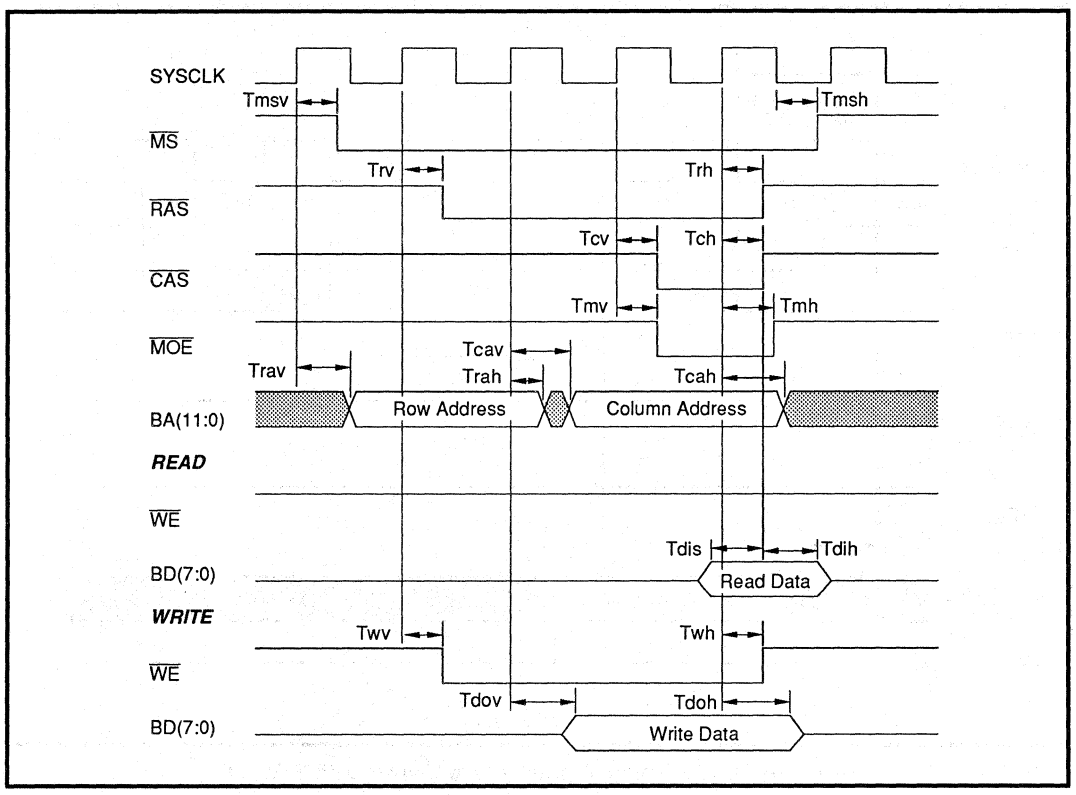

FIGURE 11: DRAM Timing, Standard Cycle (Shown with RWL = 0 and CWL = 0)

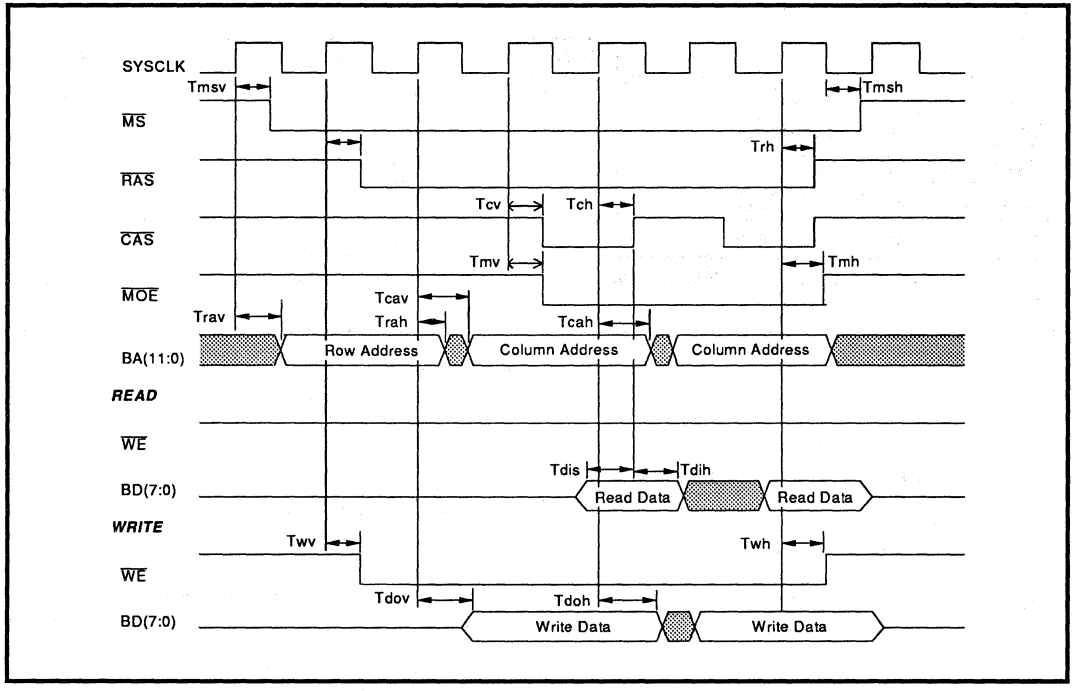

FIGURE 12: DRAM Timing, Fast Page Cycles (Shown with RWL = 0, RWH = 0, CWL = 0 and CWH = 0)

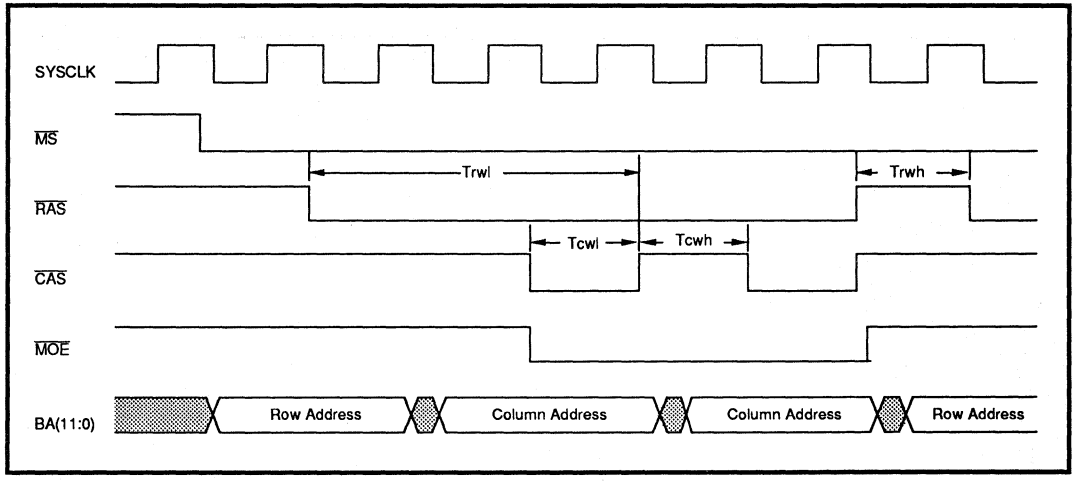

FIGURE 13: DRAM Timing (Showing the Relationship of RWL, RWH, CWL and CWH to overall timing)

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SCSI Asynchronous Timing Paraemeters

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
Tods	Data Setup to $\overline{ACK}\downarrow$	SCSI Output Phase	5			ns
Todh	Data Hold from $\overline{ACK}\downarrow$	SCSI Output Phase	12			ns
Talrh	$\overline{ACK}\downarrow$ to $\overline{REQ}\uparrow$				49	ns
Tids	Data Setup to $\overline{REQ}\downarrow$	SCSI Input Phase	80			ns
Tidh	Data Hold from $\overline{ACK}\downarrow$	SCSI Input Phase	29			ns

Note: All timing parameters are measured with 200 pf load, two SCSI terminator loads with $\overline{ACK}$ Filter turned off.

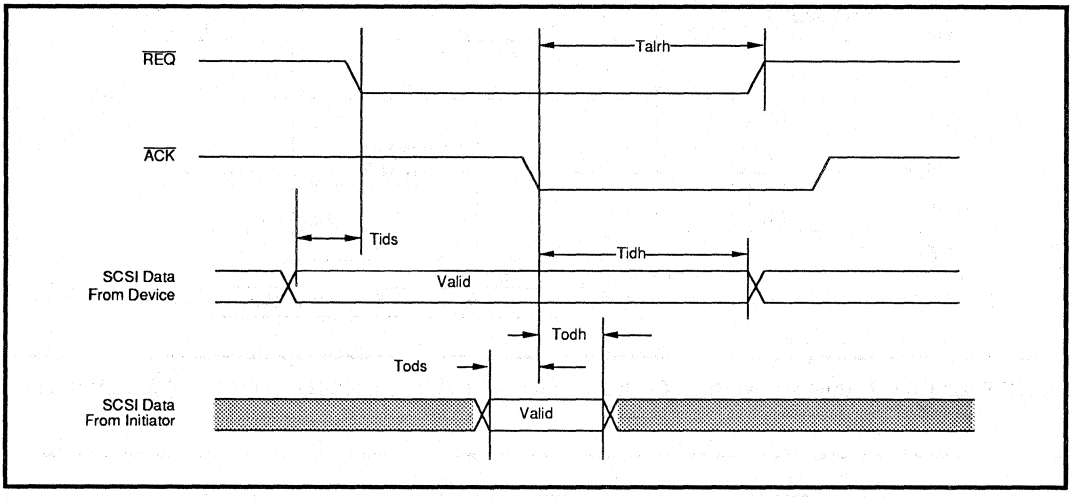

FIGURE 14: SCSI Asynchronous Timing

SCSI Synchronous Timing Paramenters

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
Trh	$\overline{REQ}$ Assertion Time		37		48	ns
Trl	$\overline{REQ}$ Deassertion Time		63		52	ns
Tids	Setup time SCSI Data to $\overline{REQ}\downarrow$	Write to SCSI bus	43			ns
Tidh	Hold time $\overline{REQ}\downarrow$ to SCSI Data invalid	Write to bus	43			ns
Tal	Minimum $\overline{ACK}$ Assertion Width Required		10			ns
Tods	Data Setup to $\overline{ACK}\downarrow$	Read from the SCSI bus	5			ns
Todh	Data Hold from $\overline{ACK}\downarrow$	Read from the SCSI bus	12			ns

Note: All timing parameters are measured with 200 pf load, two SCSI terminator loads, $\overline{ACK}$ filter turned off.

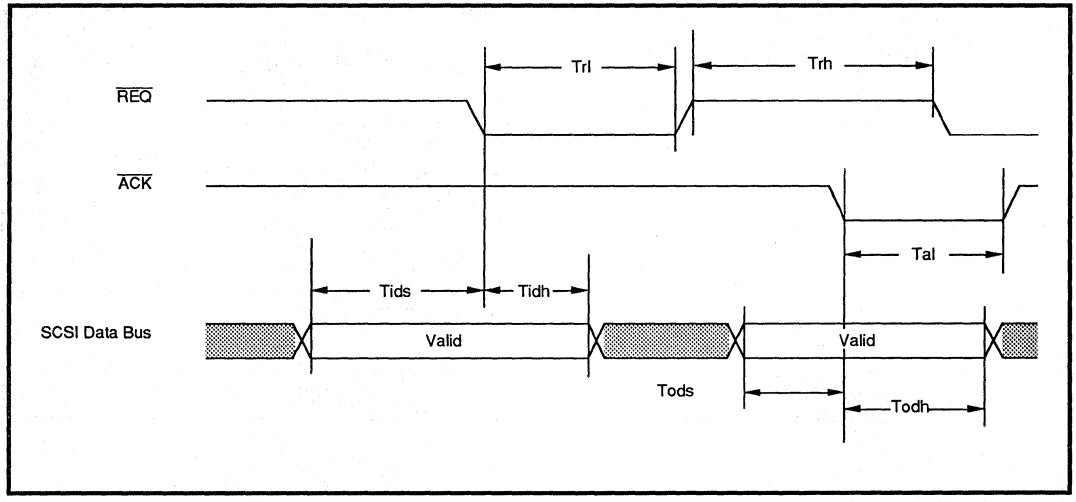

FIGURE 15: SCSI Synchronous Timing

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Synchronous Data In/Out Phase

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
Txtrp*	Synchronous Transfer Period	(see note)				ns
Tsrl	SYSFREQ high to $\overline{REQ}$ low				50	ns
Tsrh	SYSFREQ high to $\overline{REQ}$ high				60	ns
Tdov	SYSFREQ high to data out valid				40	ns
Tdsu	Data setup to $\overline{ACK}$ low		55			ns
Tdh	Data hold from $\overline{ACK}$ low		40			ns

Note: Txtrp is the Synchronous Transfer Period as defined by the Synchronous Control Register (Reg: 43H). SYSFREQ is a function of the BUFCLK and is determined by the prescale value as defined by the Clock Control Register (Reg: 49H).

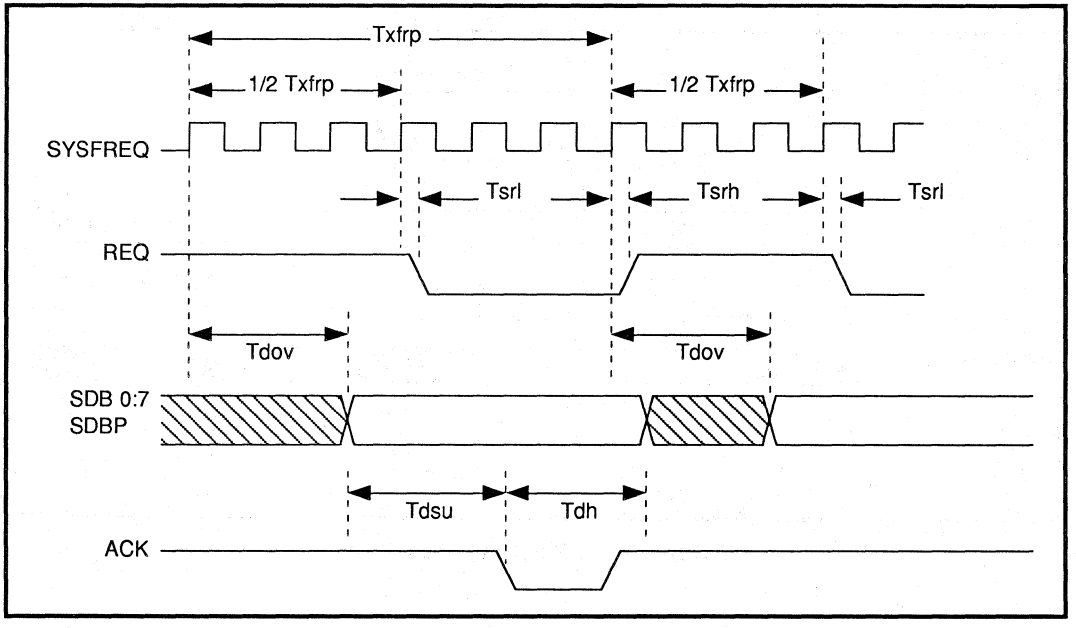


FIGURE 16: Even Number of SYSFREQ Cycles/SCSI Transfer Period

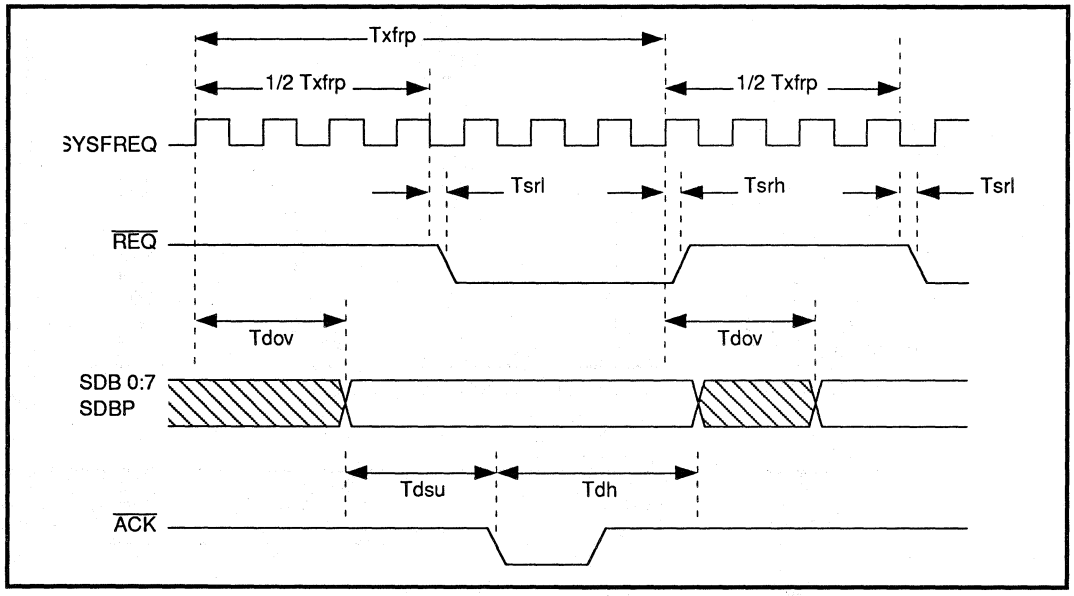


FIGURE 17: Odd Number of SYSFREQ Cycles/SCSI Transfer Period

Wait for Selection

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
Tbsd	Bus Settle Delay (400 ns) to the assertion of $\overline{BSY}$		3T + 90		4T + 90	ns

Note: T is the SCSI Clock Period (SCP) as defined in Register 49H (CLKCTL).

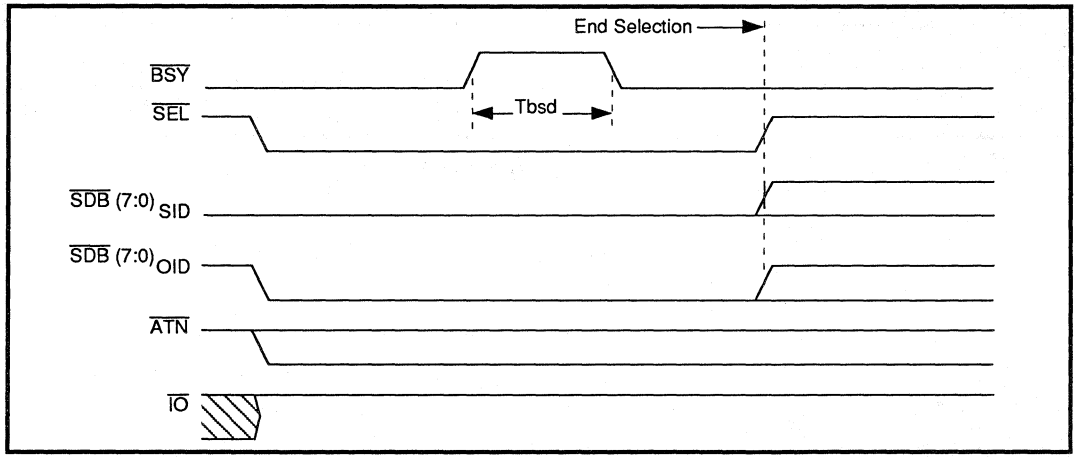


FIGURE 18: Wait for Selection

Arbitration

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
Tbfsd	Bus Settle Delay (400 ns) + Bus Free Delay (800 ns) to the assertion of BSY and $\overline{SDB}_{OID}$		6T + 110		7T + 110	ns
Tad	Arbitration Delay (2.4 µsec) to the assertion of $\overline{SEL}$ (win) or deassertion of $\overline{BSY}$ and $\overline{SDB}_{OID}$ (lost)		-		13T + 100	ns
Tbcsd	Bus Clear Delay (800 ns)+ Bus Settle Delay (400 ns) to end of Arbitration Phase		-		6T + 100	ns

Note: T is the SCSI Clock Period (SCP) as defined in Register 61H (CLKCTL).

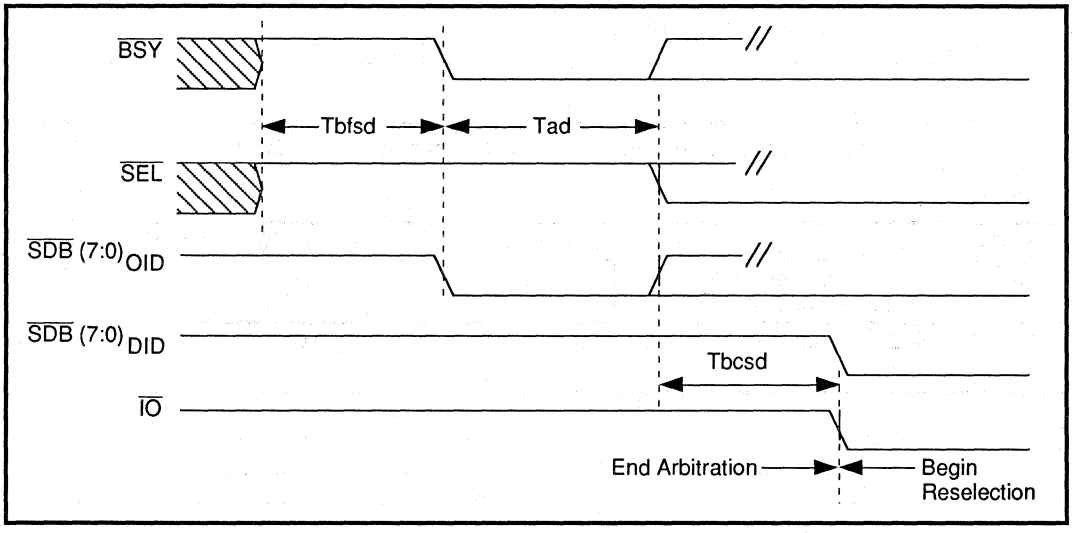


FIGURE 19: Arbitration

Reselection

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
Tbcsd	Bus Clear Delay (800 ns) + Bus Settle Delay (400 ns) to end of Arbitration Phase		-		6T + 100	ns
Tdskd1	Two Deskew Delays (90 ns) to the deassertion of $\overline{BSY}$		-		160	ns
Tbsd	Bus Settle Delay (400 ns) to the assertion of $\overline{BSY}$		-		2T + 40	ns
Tdskd2	Two Deskew Delays (90 ns) to the deassertion of SEL, $\overline{SDB}_{OID}$, and $\overline{SDB}_{DID}$		1T +70		2T + 70	ns

Note: T is the SCSI Clock Period (SCP) as defined in Register 61H (CLKCTL).

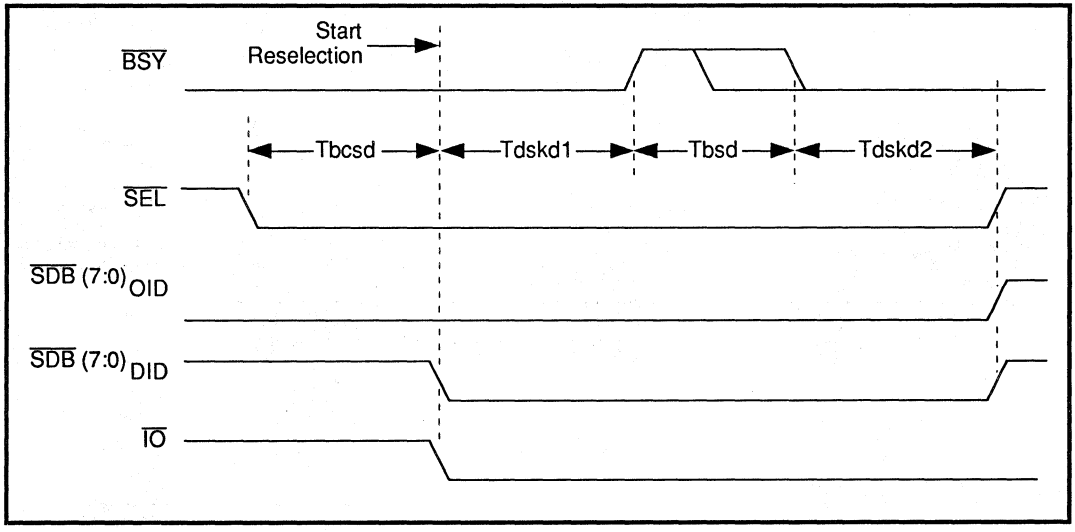
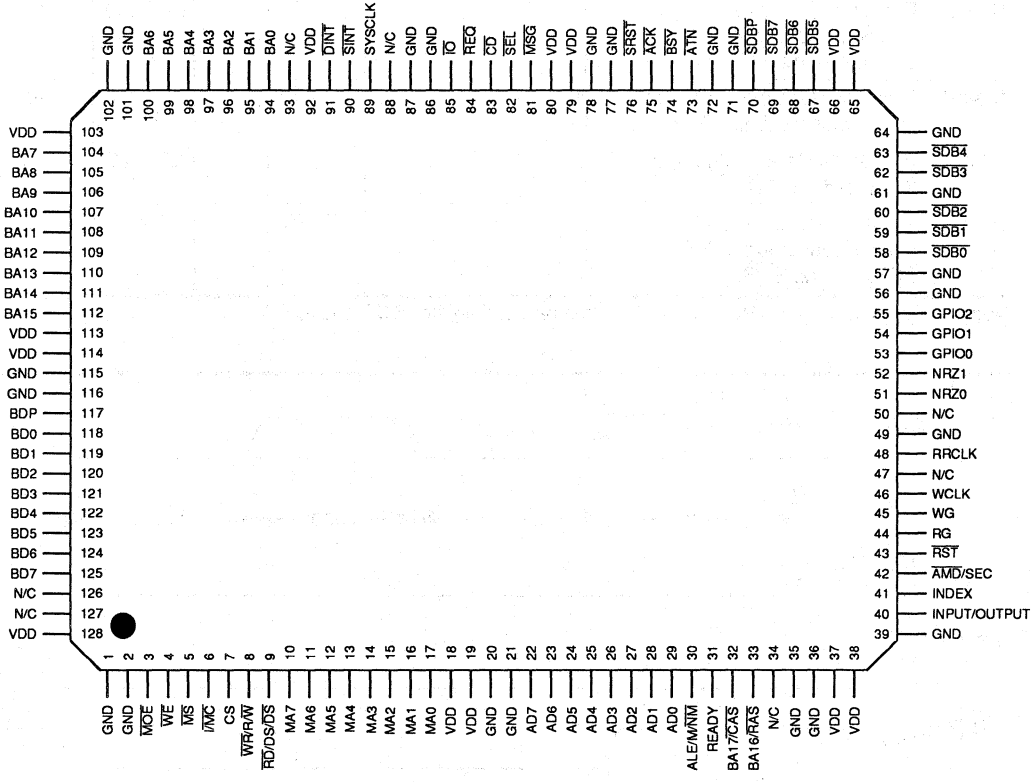


FIGURE 20: Reselection

SSI 32C9023
SCSI Combo Controller
80 Mbit/s; dual bit NRZ interface

PACKAGE PIN DESIGNATIONS

(Top View)



128-Lead QFP

CAUTION: Use handling procedures necessary for a static sensitive component.

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX: (714) 573-6914

silicon systems®
A TDK Group Company

SSI 32C9024
Differential SCSI Combo Controller
80 Mbit/s; dual bit NRZ interface
Advance Information

December 1993

DESCRIPTION

The SSI 32C9024 is an advanced CMOS VLSI device which integrates major portions of the hardware needed to build a SCSI disk drive with differential support. The circuitry of the SSI 32C9024 includes a complete SCSI target interface, an advanced buffer manager, a high performance disk formatter and an 88 bit Reed-Solomon ECC with fast "on-the-fly" hardware correction. The SSI 32C9024 provides maximum performance while minimizing micro controller intervention.

The SSI 32C9024 provides a Dual Bit Interface to the ENDEC. The Dual Bit Interface allows an effective transfer rate of up to 80 megabits per second on the disk interface by utilizing two parallel NRZ data signals and a clock rate of 40 MHz. The reduction of overall clock rates between the SSI 32C9024 and the ENDEC can be of great benefit to the designer.

The SSI 32C9024 can sustain concurrent transfers of up to 80 megabits per second transfer rate to the disk and 10 megabytes per second across the SCSI bus.

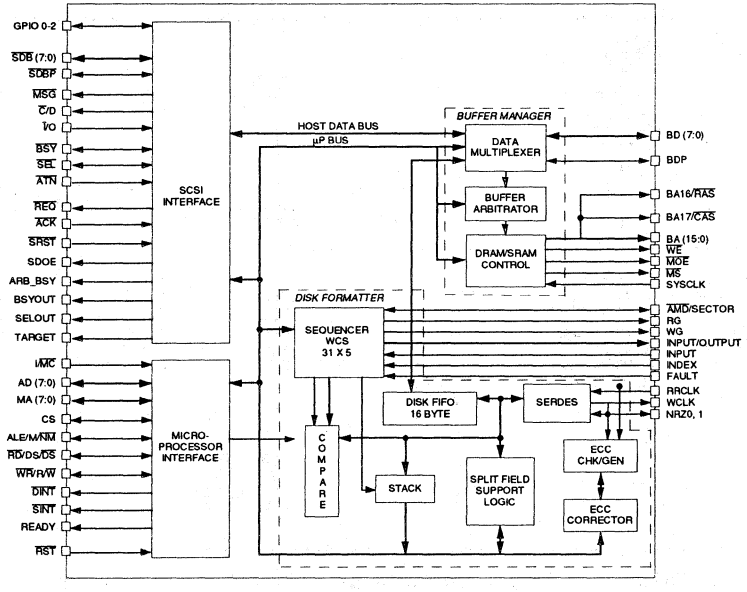
(continued)

FEATURES

- **SCSI Bus Interface**
  - **Full SCSI-2 Compatibility**
  - **Direct bus interface logic with on-chip 48 mA drivers for single ended operation**
  - **Control signals for operation with external differential tranceivers**
  - **Synchronous transfer rates up to 10 megabytes per second**
  - **Asynchronous transfer rates up to 5 megabytes per second**
  - **Parity generation and checking**
  - **Auto Command Mode (ACM) SCSI state machine performs high level SCSI sequences without microprocessor intervention**
  - **Four level ACM command FIFO supports automatic execution of multiple ACM commands**
  - **Hardware support for automatic handling of SCSI-2 command queuing**
  - **Automatic SCSI CDB size determination**
  - **Automatic SCSI Disconnect and Reconnect**
  - **Sixteen byte data FIFO between SCSI channel and Buffer Manager**

(continued)

BLOCK DIAGRAM



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SSI 32C9024
Differential SCSI Combo Controller
80 Mbit/s; dual bit NRZ interface

DESCRIPTION (continued)

The SSI 32C9024 is one of a family of Silicon Systems' single chip disk controllers which support a wide range of device interfaces. The SSI 32C9023 is a single ended only version of the SSI 32C9024. The SSI 32C9022 is pin compatible with the SSI 32C9024 but supports disk data transfers rate up to only 48 megabits per second. Other family members support AT and PCMCIA interfaces. The Silicon Systems' chip family is illustrated in the hierarchy chart shown in Figure 1. All members are based on a common architecture allowing major portions of firmware to be reused.

The high level of integration within the SSI 32C9024 represents a major reduction in parts count. When the SSI 32C9024 SCSI Controller is combined with the SSI 32R2110 Read/Write device, SSI 32P4782 Combination Read Channel, SSI 32D4680 Time Base Generator, SSI 32H4631 Servo and Motor Speed Controller, an appropriate microcontroller and memory, a complete, cost efficient, high performance intelligent drive solution is created.

FEATURES (continued)

- Buffer Manager
  - Direct support of DRAM or SRAM
    - SRAM throughput to 20 megabytes per second
    - SRAM size up to 256k bytes
    - DRAM throughput to 17.78 megabytes per second
    - DRAM size up to 1 megabyte
  - Programmable memory timing
  - Buffer RAM segmentation with flexible segment sizes from 256 bytes to 1 megabyte
  - Dedicated host, disk and microprocessor address pointers
  - Internal buffer protection circuit provides buffer integrity
- Disk Formatter
  - Dual Bit NRZ Interface
  - Effective Data Rates to 80 megabits/s
  - Automatic multi-sector transfer
  - Header or microprocessor based split data field support
  - Advanced sequencer organized in 31 x 5 bytes
  - 88-bit Reed Solomon ECC with "on-the-fly" fast hardware correction circuitry
  - Capable of correcting up to four 10-bit symbols in error

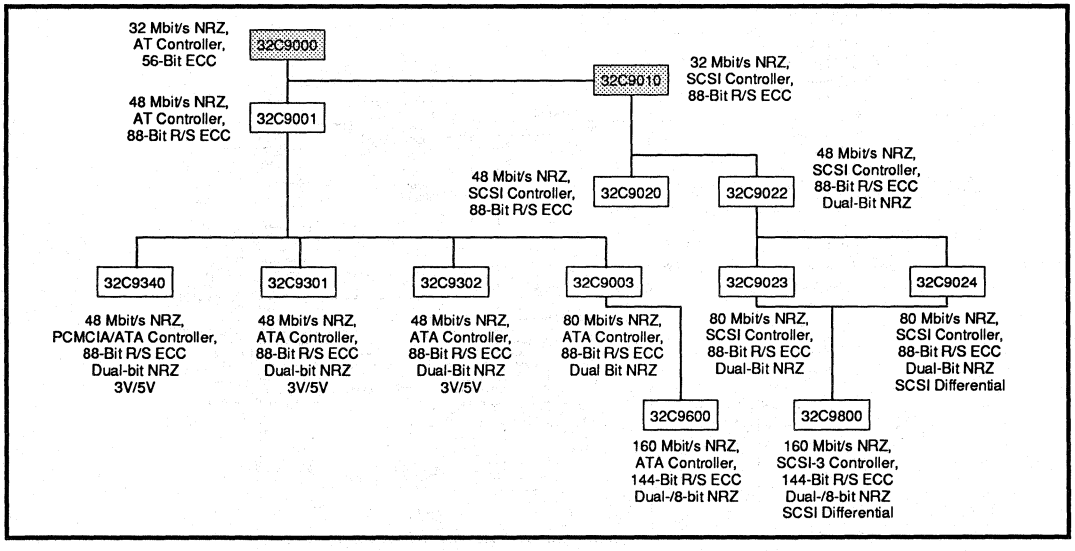

FIGURE 1: Silicon Systems' Single Chip Controller Hierarchy

  - Guaranteed to correct one 31-bit burst or two 11-bit bursts
  - Hardware on-the-fly correction of an 11-bit single burst error within a half sector time
  - Detects up to one 51-bit burst or three 11-bit bursts
- Microprocessor Interface
  - Supports both multiplexed or non-multiplexed microprocessors
  - Separate or combined host and disk interrupts
  - Programmable wait state insertion
- Other Features
  - Internal power down modes
  - Available in 128-pin QFP

FUNCTIONAL DESCRIPTION

The SSI 32C9024 contains the following four major functional blocks:

Microcontroller Interface
SCSI Interface
Disk Formatter
Buffer Manager

The Microprocessor Interface allows the local microprocessor access to all of the SSI 32C9024 internal control registers and any location within the buffer memory. The microprocessor, by writing and reading the internal registers can control all activities of the SSI 32C9024. The microprocessor can elect to perform SCSI and/or disk operations directly, or it can enable the advanced features of the SSI 32C9024 which can perform all typical operations automatically.

The SCSI Interface block handles all SCSI activities. The SCSI interface includes all of the signals necessary for implementing a differential SCSI interface using external differential transceivers. The SSI 32C9024 also includes 48 mA drivers allowing for direct connection of the SSI 32C9024 to the SCSI bus. The SCSI interface logic includes Auto Command Mode (ACM) logic, an advanced state machine capable of handling a variety of complex SCSI sequences without microprocessor intervention. The microprocessor can queue up to four ACM commands into the ACM Command FIFO to create even more sophisticated command sequences. The SCSI block interfaces directly with the Buffer Manager via an internal speed matching FIFO. This FIFO, plus the bandwidth capabilities of the Buffer Manager guarantee sustained full speed transfers across the SCSI bus. The high level of automation of the ACM minimizes SCSI bus overhead. The net result is maximized performance with minimum SCSI bus bandwidth utilization.

The Disk Formatter performs the serialization and deserialization of data. If provides all of the necessary functions to control track formatting, header search, and the reading and writing of data. The heart of the Disk Formatter is an advanced programmable sequencer which is flexible enough to interface to a wide variety of read/write channels. The sequencer can contain 31 instructions, each of which is 5 bytes (40 bits) in width. The width of the instructions allows for sophisticated branching techniques which increase the flexibility and power of the sequencer. The flexible disk interface can be configured through a wide range of capabilities. This allows the SSI 32C9024 to interface with nearly any read/write channel and allows the user of the SSI 32C9024 to select the read/write channel best suited to the device. Of course, by selecting the SSI 32C9024 controller and the 32P4782 Combination Read Channel, you are guaranteed a problem free interface.

Within the Disk Formatter are the ECC generator/checker and ECC corrector. The generator/checker provides the ability to generate or check a 32 bit ECC for headers and an 88 bit Reed Solomon code for data. If the checker detects an error in an 88 bit Reed Solomon data field, the syndrome information is transferred into the corrector. The corrector performs the necessary operations to determine if the error was correctable and interfaces directly with the buffer controller to perform the correction automatically. The corrector performs its correction within one half of a sector time. This guarantees that the corrector will always be available to correct the next sector if necessary.

As its name implies, the Buffer Manager manages the data buffer of the controller. The Buffer Manager can support either SRAM or DRAM. When configured to operate with DRAM, the Buffer Manager automatically performs necessary refresh cycles. The Buffer Manager creates all of the necessary timing and control signals for a wide range of memory types and speeds. The Buffer Manager interfaces with the buffer memory, the SCSI Interface block, the data path of the Disk Formatter block, the ECC corrector and the microprocessor. If more than one of these devices requires access to the buffer memory, the Buffer Manager arbitrates the requests automatically. The Buffer Manager of the SSI 32C9024 can sustain SCSI operations at the rate of 10 megabytes per second, Disk Formatter operations at 80 megabits per second (10 megabytes per second).

PIN DESCRIPTION

The following convention is used in the pin description:

(I) denotes an input
(O) denotes an output
(Z) denotes a tri-state output
(OD) denotes an open drain output

GENERAL

NAME	TYPE	DESCRIPTION
VDD		POWER SUPPLY PIN
GND		GROUND

HOST INTERFACE

$\overline{SDBP}$	I/O	SCSI DATA BUS PARITY. Odd parity bit for the SCSI data bus.
SDB(7:0)	I/O	SCSI DATA BUS BITS 7-0.
$\overline{ATN}$	I	ATTENTION. This active low signal is used by the initiator to request a message out phase.
$\overline{BSY}$	I/O	BUSY. This active low signal is used to indicate when the bus is active.
$\overline{ACK}$	I	ACKNOWLEDGE. This active low signal is used in the handshake protocol to indicate the completion of a data byte transfer.
$\overline{SRST}$	I	SCSI RESET. This active low signal is used to reset the SCSI controller.
$\overline{MSG}$	O	MESSAGE. This active low signal is used to indicate a message phase.
$\overline{SEL}$	I/O	SELECT. This active low signal is used to indicate either a selection or reselection phase.
$\overline{C}$/D	O	COMMAND/DATA. This signal is used to indicate either a command or data phase.
$\overline{REQ}$	I	REQUEST. This active low signal is used in the handshake protocol to initiate a data byte transfer.
$\overline{I}$/O	I	INPUT/OUTPUT. This signal is used to indicate the direction of data transfer.
GPIO(2:0)	I/O	INPUT/OUTPUT. These pins are used to indicate the SCSI ID of the target device. The pins can be programmed as outputs for test purposes only.

DIFFERENTIAL SCSI

SDOE	O	SCSI DATA BUS OUTPUT ENABLE.
ARB_BSY	O	Enables BSY output in arbitration phase.
BSYOUT	O	Enables BSY output in phases other than arbitration phase.
SELOUT	O	Enables SEL output.
TARGET	O	Enables Target mode; used to control the SCSI phase signals $\overline{IO}$, $\overline{CD}$, and $\overline{MSG}$.

DISK INTERFACE

NAME	TYPE	DESCRIPTION
INDEX	I	INDEX. Input for index pulse received from the drive.
INPUT/ OUTPUT	I/O	DISK SEQUENCER INPUT/OUTPUT. A general purpose control (output) and status (input) pin configured by the Output Enable Bit of Register 71H, bit 7. At power-on, this pin is an input. As an input, it can be used to synchronize the disk sequencer to an external event. As an output, it is controlled by bit 2 of the Control Field of the disk sequencer.
INPUT	I	INPUT: This pin can be used to synchronize the disk to an external event.
$\overline{\text{AMD}}$/ SECTOR	I/O	ADDRESS MARK DETECT/SECTOR. This pin is used in the Hard Sector mode as the sector input. A pulse on this pin indicates a sector mark is found. In the Soft Sector mode, a low-level input indicates an address mark was detected. The device powers up in Soft Sector Default mode.
RG	O	READ GATE. During disk data read, this pin is asserted. Active high.
WG	O	WRITE GATE. During disk data write, this pin is asserted. Active high.
RRCLK	I	READ/REFERENCE CLOCK. This is a clock signal generated from an external data synchronizer. This clock is used to synchronize the input NRZ data and clock the disk formatter of the chip.
WCLK	O	WRITE CLOCK. This signal clocks the NRZ data out in the dual NRZ Interface mode.
NRZ1	I/O	NON RETURN TO ZERO 1. In dual NRZ mode, this signal is the most significant bit read data input from the disk drive when the read gate signal is asserted; it is the most significant bit write data output to the disk drive when the write gate signal is asserted. In single NRZ mode, this signal is not used and should be grounded. NRZ1 is the leading bit of the bit pair. In Write mode, the MSB of the data bytes always appears on NRZ1.
NRZ0	I/O	NON RETURN TO ZERO. In dual NRZ mode, this signal is the least significant bit read data input from the disk drive when the read gate signal is asserted; it is the least significant bit write data output to the disk drive when the write gate signal is asserted. In single NRZ mode, this signal is used to transfer NRZ data to/from the read channel chip.
FAULT	I	FAULT: This input when asserted indicates to the chip that a fault has occurred with the disk. The disk sequencer will stop and both RG and WG pins will be deasserted.

MICROPROCESSOR INTERFACE

$\overline{\text{RST}}$	I	RESET. An asserted low input generates a component reset that holds the internal registers at reset, stops all operations within the chip, and deasserts all output signals. All input/output signals are set to the high-Z state during the assertion of this signal.
ALE/M/$\overline{\text{NM}}$	I	ADDRESS LATCH ENABLE/MULTIPLEXED/NON-MULTIPLEXED ADDRESS SELECT. When tied high or left floating after reset, the microprocessor interface is configured as non-multiplexed. When driven low, then the microprocessor interface is configured as multiplexed. In this case this pin functions as the address latch enable, and the MA(7:0) pins are the demultiplexed address outputs.
CS	I	CHIP SELECT. Active high signal, when asserted, the internal registers of the SSI 32C9022 can be accessed.
$\overline{\text{WR}}$/R/$\overline{\text{W}}$	I	WRITE STROBE/READ/WRITE. In the Intel bus mode, when an active low signal is present with CS signal high, the data is written to the internal registers. In the Motorola bus mode, this signal acts as the R/$\overline{\text{W}}$ signal.

MICROPROCESSOR INTERFACE (continued)

NAME	TYPE	DESCRIPTION
$\overline{RD}$/DS/$\overline{DS}$	I	READ STROBE/DATA STROBE. When the Intel bus control interface is selected (the I/$\overline{MC}$ is high), this signal acts as the $\overline{RD}$ signal. When the read strobe signal is asserted low and the CS signal is asserted high, the data from the specified register will be driven to the AD signals. When the Motorola bus control interface is selected (the I/$\overline{MC}$ is low) this signal acts as the data strobe signal. A high on the R/$\overline{W}$ signal along with this signal asserted and the CS signal asserted high indicates a read operation. A low on the R/$\overline{W}$ signal along with this signal asserted and the CS signal asserted high indicates a write operation. Note when *non-multiplexed Motorola* bus configuration is chosen, the data strobe is an active low input.
$\overline{DINT}$	O, OD,Z	DISK INTERRUPT. An active low signal indicates the controller is requesting microprocessor service from the disk side. This signal is programmable for either a push-pull or open-drain output circuit. This signal powers up in the high-Z state. Register 4F bit 3 enables the pull-up.
$\overline{SINT}$	O, OD,Z	SCSI INTERRUPT. This signal is generated by the SCSI controller and is an interrupt line to the microprocessor. It is programmable for either a push-pull or open drain output circuit. This signal powers up in the high-Z state. The interrupt is sourced from the SCSI Interrupt Register. Register 4F bit 3 enables the pull-up. This signal is also programmable to be either an active high or low interrupt.
AD(7:0)	I/O	ADDRESS/DATA BUS. When configured in the Intel mode, these lines are multiplexed, bidirectional microprocessor register address and data lines. When configured in the Motorola mode, these lines are bidirectional data lines.
MA(7:0)	I/O	MICROPROCESSOR ADDRESS BUS: These signals are nonmultiplexed address input or latched address output lines.
READY	O	READY: When this signal is deasserted low, the microprocessor shall insert wait states to allow time for the chip to respond.
I/$\overline{MC}$	I	INTEL/MOTOROLA: This signal selects the microprocessor interface to be used. When this signal is asserted high, it selects the Intel bus control interface. When this signal is deasserted low, it selects the Motorola bus control interface. This signal has an internal pull-up to allow the default selection of the Intel bus control interface.

BUFFER MANAGER INTERFACE

BA(15:0)	O	BUFFER MEMORY ADDRESS LINES 15 through 0. Active high, for direct connection to a Static or Dynamic RAM address lines.
BA16/$\overline{RAS}$	O	BUFFER MEMORY ADDRESS 16: In SRAM mode, for direct connection to a Static RAM address line 16. ROW ADDRESS STROBE: In DRAM mode, for direct connection to a Dynamic RAM Row Address Strobe signal.
BA17/$\overline{CAS}$	O	BUFFER MEMORY ADDRESS 17: In SRAM mode, for direct connection to a Static RAM address line 17. ROW ADDRESS STROBE: In DRAM mode, active low, for direct connection to a Dynamic RAM Column Address Strobe signal.
BD(7:0)	I/O	BUFFER MEMORY DATA BUS. 7 through 0. Active high, buffer data bus that connects directly to the buffer RAM data lines.

ELECTRICAL SPECIFICATIONS

BUFFER MANAGER INTERFACE (continued)

BDP	I/O	BUFFER MEMORY DATA PARITY. This signal provides odd parity for the buffer memory data bus during transfers to/from the buffer memory to the buffer RAM.
$\overline{MOE}$	O	MEMORY OUTPUT ENABLE. In SRAM mode this signal is asserted low when every buffer memory access is active. In DRAM mode this signal is asserted low only for buffer memory read operation.
$\overline{MS}$	O	MEMORY SELECT. An active low signal indicates external memory is selected.
$\overline{WE}$	O	WRITE ENABLE. Active low, write enable for the buffer RAM.
SYSCLK	I	SYSTEM CLOCK. This signal is used to synchronize the buffer RAM access, including the generation of memory address bits, write enable $\overline{WE}$, and memory output enable $\overline{MOE}$.

ABSOLUTE MAXIMUM RATINGS

Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC operating characteristics.

PARAMETER	RATING
Power Supply Voltage, VCC	7V
Ambient Temperature	0 to 70°C
Storage Temperature	-65 to 150°C
Power Dissipation	750 mW
Input, Output pins	-0.5 to VCC + 0.5V

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
VCC Power Supply Voltage		4.50		5.50	V
ICC Supply Current	Ta = 25°C Outputs Unloaded			50	mA
ICCS Supply Current				250	µA
VIL Input Low Voltage		-0.5		0.8	V
V0IH Input High Voltage		2.0		VCC + 0.5	V
VOL Output Low Voltage	All pins except SCSI interface, IOL = 2 mA			0.4	V
VOL Output Low Voltage	SCSI interface pins, IOL = 48 mA			0.5	V
VOH Output High Voltage	IOH = -400 µA			2.4	V
IL Input Leakage Current	0 < VIN < VCC	-10		10	µA
CIN Input Capacitance				10	pF
COUT Output Capacitance				10	pF

MICROPROCESSOR INTERFACE TIMING

Multiplexed Interface Timing Parameters (Figures 2-5)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
Ta	ALE width		20			ns
Tma	Address valid to MA(7:0) valid				30	ns
Tr	$\overline{RD}$ width		80			ns
As	Address valid to ALE ↓		5			ns
Ah	ALE ↓ to address invalid		10			ns
Cs	CS valid to $\overline{RD}$ ↓ or DS ↑		20			ns
Ch	$\overline{RD}$ ↑ or DS ↓ to CS ↓		0			ns
Tda	$\overline{RD}$ ↓ or DS ↑ to read data valid				60	ns
Tds	DS width		80			ns
Tdh	$\overline{RD}$ ↑ or DS ↓ to read data invalid		0		25	ns
Tsrw	R/$\overline{W}$ valid to DS ↑		20			ns
Thrw	DS ↓ to R/$\overline{W}$ invalid		20			ns
Tdrdy	$\overline{RD}$ ↓ to READY ↓ (Intel) or DS ↑ to READY ↓ (Motorola)				30	ns
Wds	Write data valid to $\overline{WR}$ ↑ or DS ↓		40			ns
Wdh	$\overline{WR}$ ↑ or DS ↓ to write data invalid		10			ns

Note: ↑ indicates rising edge ↓ indicates falling edge

Non-Multiplexed Bus Interface Timings (Figure 6)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
Tmas	MA(7:0) valid to DS ↓		5			ns
Tmah	DS ↑ to MA(7:0) invalid		5			ns
Cs	CS valid to DS ↓		20			ns
Ch	DS ↑ to CS ↓		0			ns
Tda	DS ↑ to read data valid				60	ns
Tds	DS width		80			ns
Tdh	DS ↑ to read data invalid		0		25	ns
Tsrw	R/$\overline{W}$ valid to DS ↓		20			ns
Thrw	DS ↑ to R/$\overline{W}$ invalid		20			ns
Tdrdy	DS ↑ to READY ↓ (Motorola)				30	ns
Wds	Write data valid to $\overline{WR}$ ↑ or DS ↓		40			ns
Wdh	$\overline{WR}$ ↑ or DS ↓ to write data invalid		10			ns

Note 1: ↑ indicates rising edge ↓ indicates falling edge

Note 2: Loading capacitor = 30 pF

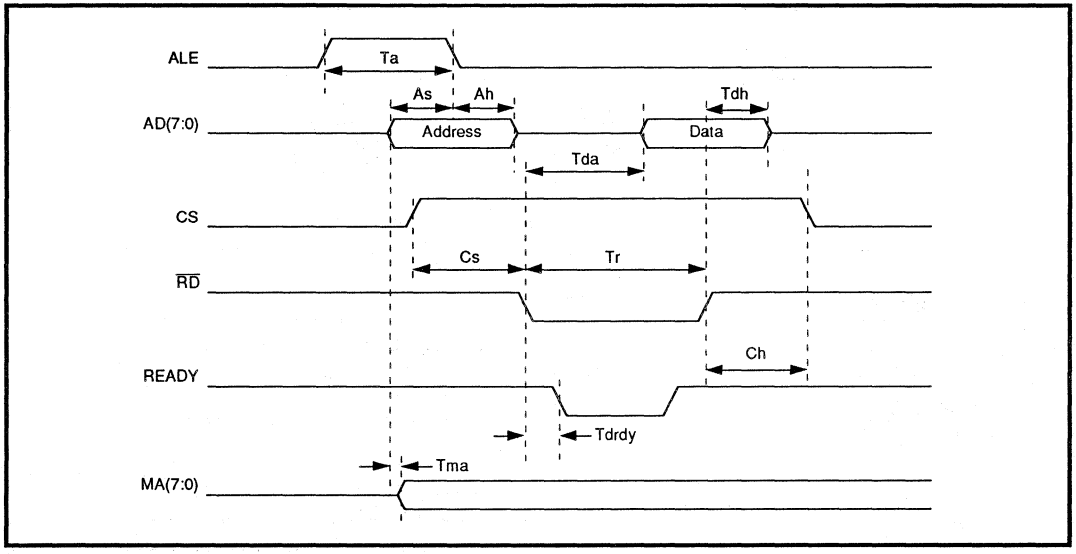

FIGURE 2: Intel Register Multiplexed Read Timing

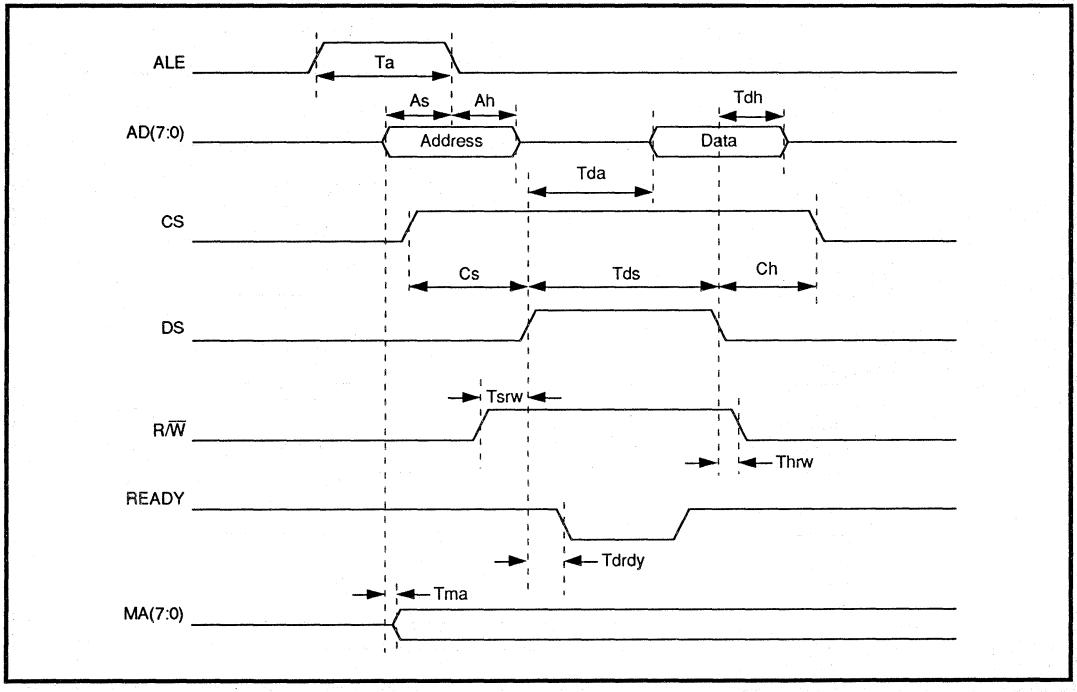

FIGURE 3: Motorola Register Multiplexed Read Timing

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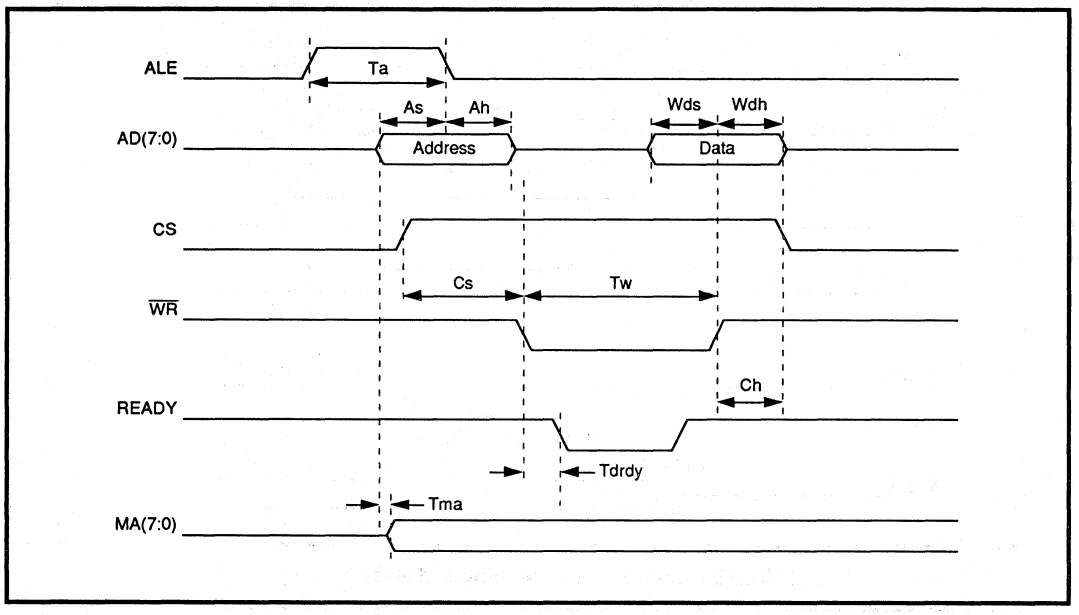

FIGURE 4: Intel Register Multiplexed Write Timing

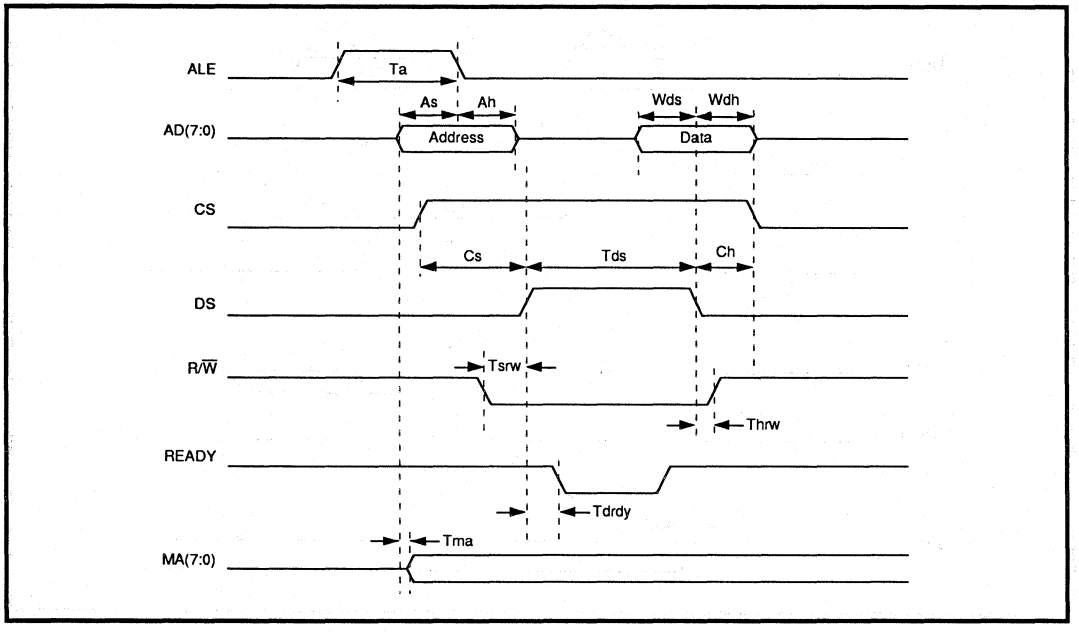

FIGURE 5: Motorola Register Multiplexed Write Timing

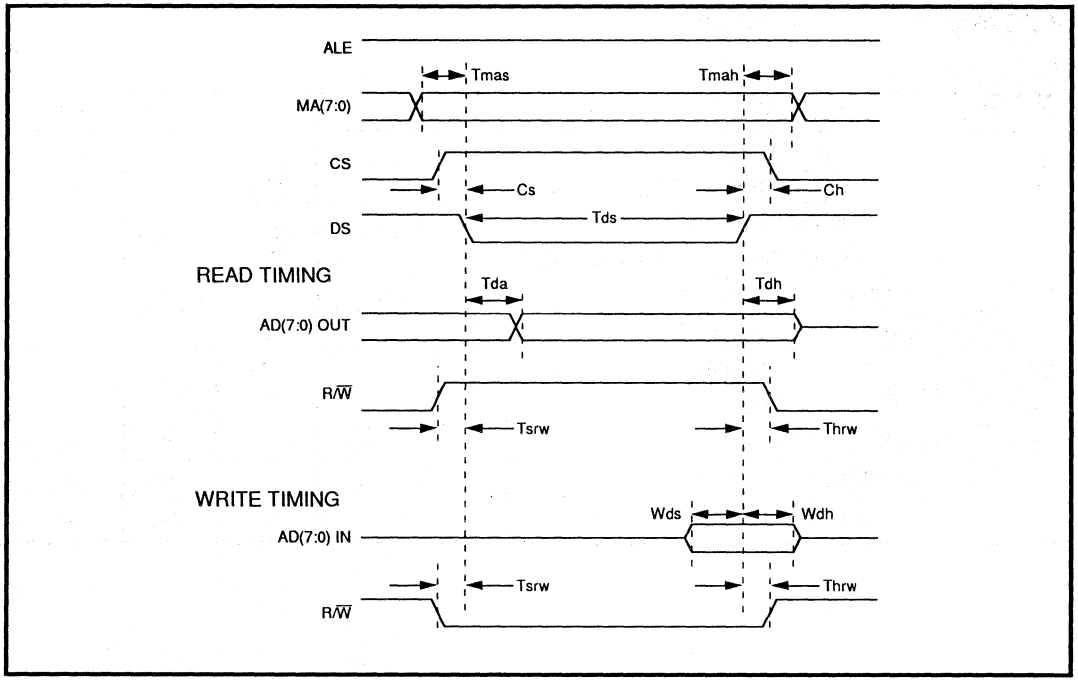

FIGURE 6: Non-Multiplexed Bus Timing Diagrams

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ELECTRICAL SPECIFICATIONS (continued)

Disk Interface Timing

SYMBOL	PARAMETER	MIN	MAX	UNIT
T	Dual bit interface RRCLK period	25		ns
T/2	Dual bit interface RRCLK high/low time	11.2		ns
T	Single bit interface RRCLK period	20.8		ns
T/2	Single bit interface RRCLK high/low time	8.5		ns
Tr,Tf	RRCLK rise/fall time		3	ns
Dis	NRZ in valid to RRCLK ↑	3		ns
Dih	RRCLK ↑ to NRZ in invalid	3		ns
As	$\overline{AMD}$ valid to RRCLK	3		ns
Tckd	RRCLK ↓ to WCLK ↓		8	ns
Dvr	RRCLK ↓ to NR out valid		18	ns
Dv	WCVLK ↓ to NRZ out valid		±2	ns

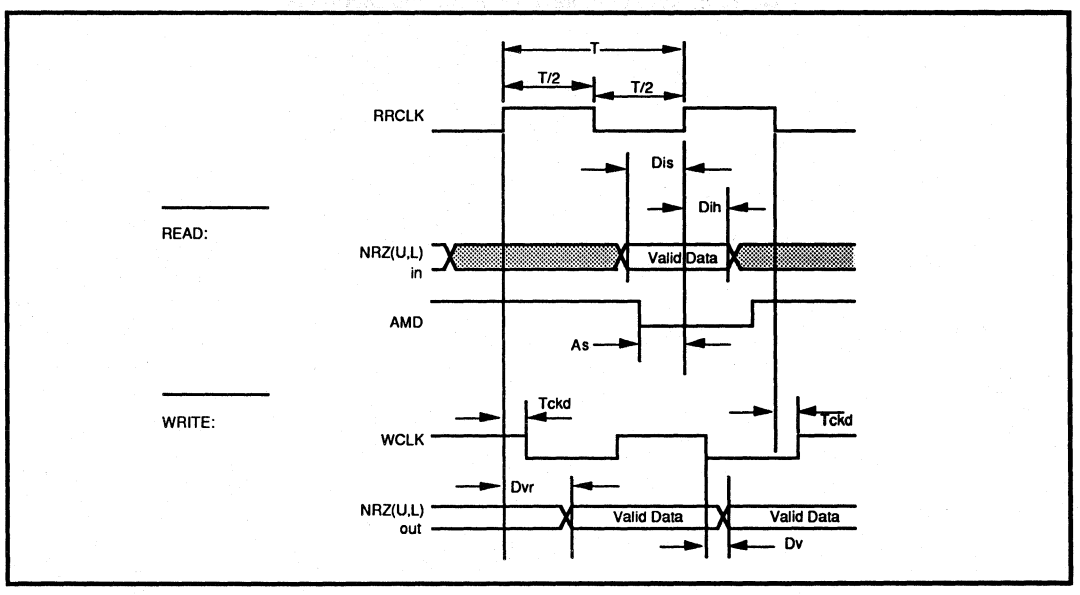


FIGURE 7: Disk Interface Timing

BUFFER MEMORY READ/WRITE TIMING PARAMETERS

PARAMETER		MIN	MAX	UNIT
T	SYSCLK period	25		ns
T/2	SYSCLK high/low time	10		ns
Tav	SYSCLK ↑ to address valid (Note 1)		18	ns
Tmsv	SYSCLK ↑ to $\overline{MS}$ ↓ (Notes 1, 6)		18	ns
Tmsh	SYSCLK ↑ to $\overline{MS}$ ↑ (Note 1)		18	ns
Tmv	SYSCLK ↓ to $\overline{MOE}$ ↓ (Note 1)		18	ns
Tmh	SYSCLK ↓ to $\overline{MOE}$ ↑ (Note 1)		18	ns
Twv	SYSCLK ↓ to $\overline{WE}$ ↓ (Note 1)		18	ns
Twh	SYSCLK ↓ to $\overline{WE}$ ↑ (Note 1)		18	ns
Tdov	SYSCLK to data out valid (Note 1)		18	ns
Tdoh	SYSCLK to data out invalid (Note 1)		18	ns
Tds	Data in valid to $\overline{MOE}$ ↑ (SRAM) Data in valid to $\overline{CAS}$ ↑ (DRAM)	5		ns
Tdh	$\overline{MOE}$ ↑ to data in valid (SRAM) $\overline{CAS}$ ↑ to data in valid (DRAM)	0		ns
Trv	SYSCLK ↑ to $\overline{RAS}$ ↓ (Note 1)		18	ns
Trh	SYSCLK ↑ to $\overline{RAS}$ ↑ (Note 1)		18	ns
Trav	SYSCLK ↑ to row address valid (Note 1)		18	ns
Trah	SYSCLK ↑ to row address invalid (Note 1)		18	ns
Tcv	SYSCLK ↑ to $\overline{CAS}$ ↓ (Note 1)		18	ns
Tch	SYSCLK ↑ to $\overline{CAS}$ ↑ (Note 1)		18	ns
Tcav	SYSCLK ↑ to column address valid (Note 1)		18	ns
Tcah	SYSCLK ↑ to column address invalid	0		ns

ELECTRICAL SPECIFICATIONS (continued)

BUFFER MEMORY READ/WRITE FUNCTIONAL PARAMETERS (continued)

PARAMETER		CONDITIONS	MIN	UNIT
Trwl	$\overline{RAS}\downarrow$ to $\overline{RAS}\uparrow$	Notes 2, 3	((RWL + 3)•T)	ns
Trwh	$\overline{RAS}\uparrow$ to $\overline{RAS}\downarrow$	Notes 2, 4	((RWH + 1)•T)	ns
Tcwl	$\overline{CAS}\downarrow$ to $\overline{CAS}\uparrow$	Note 2	((CWL + 1)•T)	ns
Tcwl	$\overline{CAS}\uparrow$ to $\overline{CAS}\downarrow$	Notes 2, 5	((CWL + 1)•T)	ns

Note: Loading capacitance = 30 pF

Note 1: The measured delay for any of the signal indicated by this note will not vary from the measured delay of any other signal indicated by this note by more than ±2 ns.

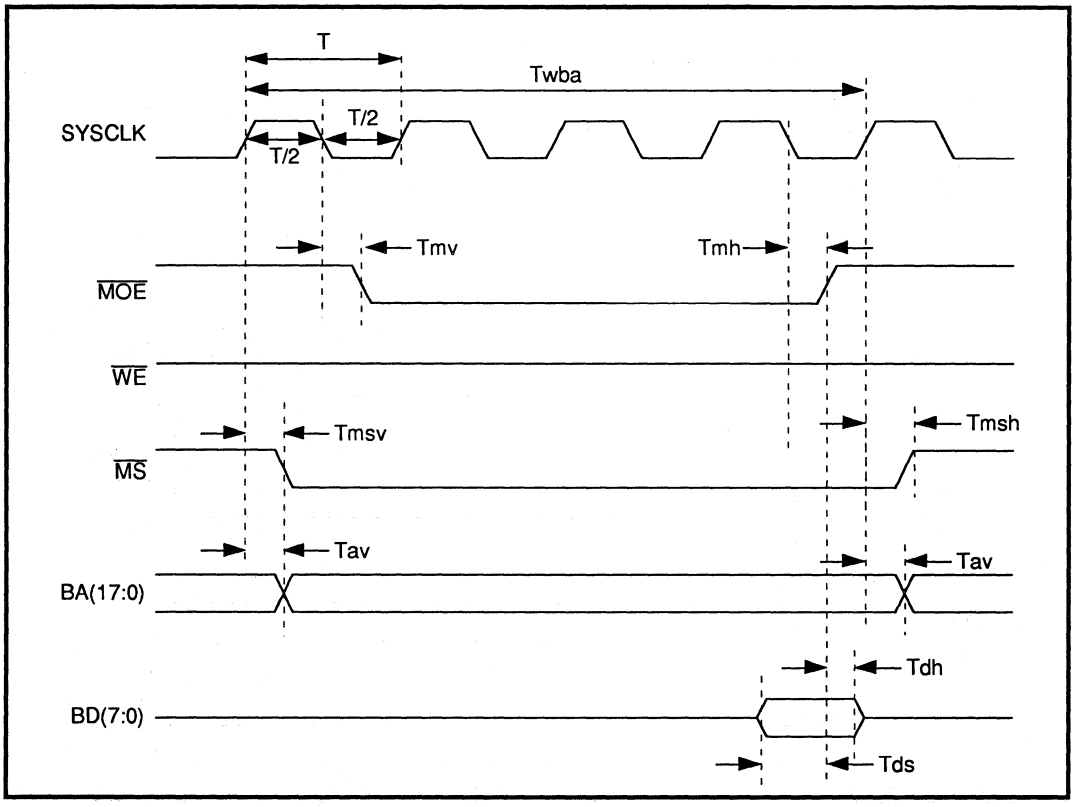
Note 2: RWL, RWH, CWL and CWH are fields in the Buffer Manager Timing Control Register (54H). Each is a two bit field which can contain a value of 0, 1, 2, or 3. These values determine the minimum number of SYSCLK periods (T) for the associated signal width.

Note 3: The minimum width value of Trwl will be generated for refresh cycles and for any buffer memory access cycle except when multiple page mode accesses are performed. When multiple page mode accesses are performed, the width of the $\overline{RAS}$ low pulse is extended until the end of the last $\overline{CAS}$ low cycle.

Note 4: The minumum value of Trwh will be generated whenever the Buffer Manager determines that a buffer request is pending at the completion of the current memory cycle and a page mode access can not be used either because page mode operation is not enabled or the needed location is not within the current page.

Note 5: The minumum value of Tcwh will be generated only between consecutive page mode accesses.

Note 6: $\overline{MS}$ will rise only if the Buffer Manager determines that no additional requests for buffer access are pending. If the Buffer Manager determines that another access is to be Made, $\overline{MS}$ is kept low between the accesses for improved speed.



Note: Twba is a functional parameter that gives the duration of one RAM data buffer access cycle in SYSCLK periods. The value is programmed in bits 1-0 of register 54H. These examples show Twba = 4T.

FIGURE 8: SRAM Read Timing

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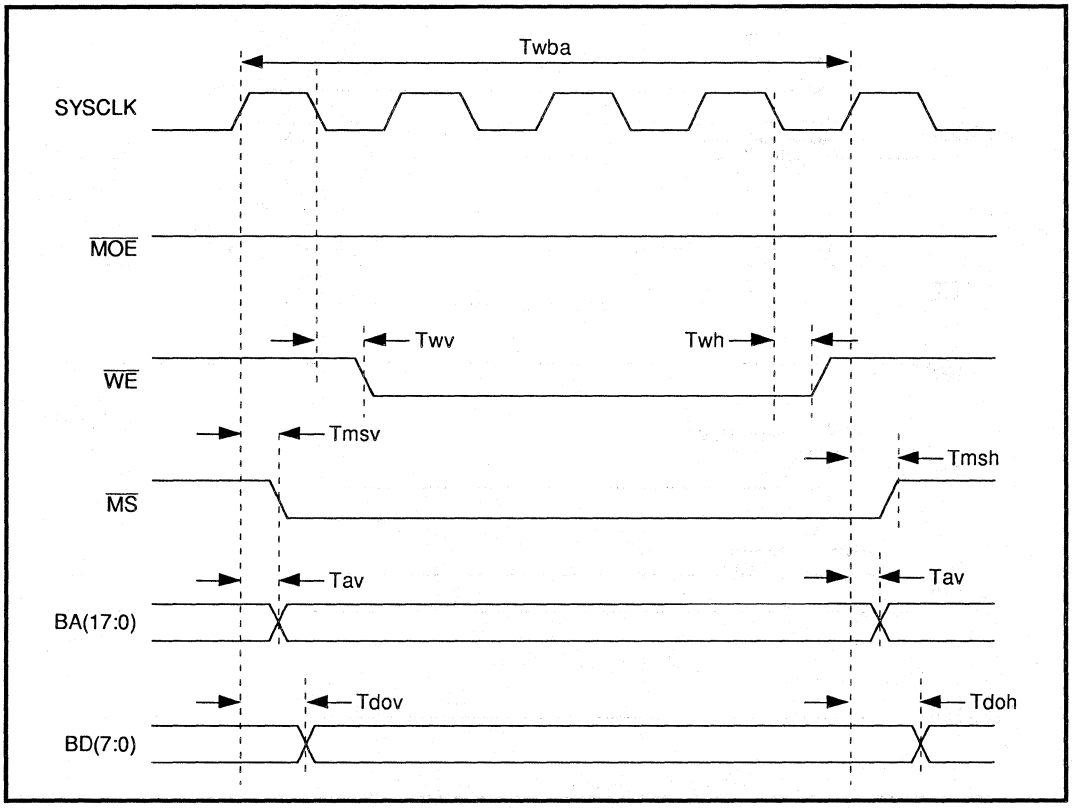

FIGURE 9: SRAM Write Timing

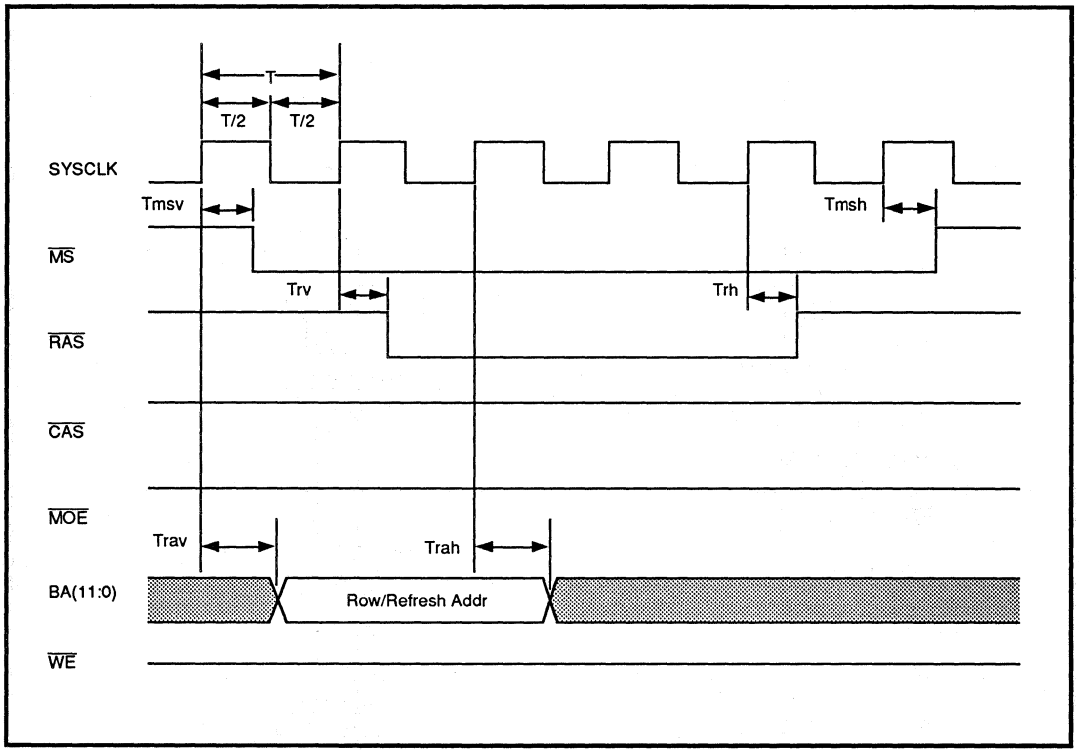

FIGURE 10: DRAM Timing, Refresh Cycle (Shown with WRL = 0)

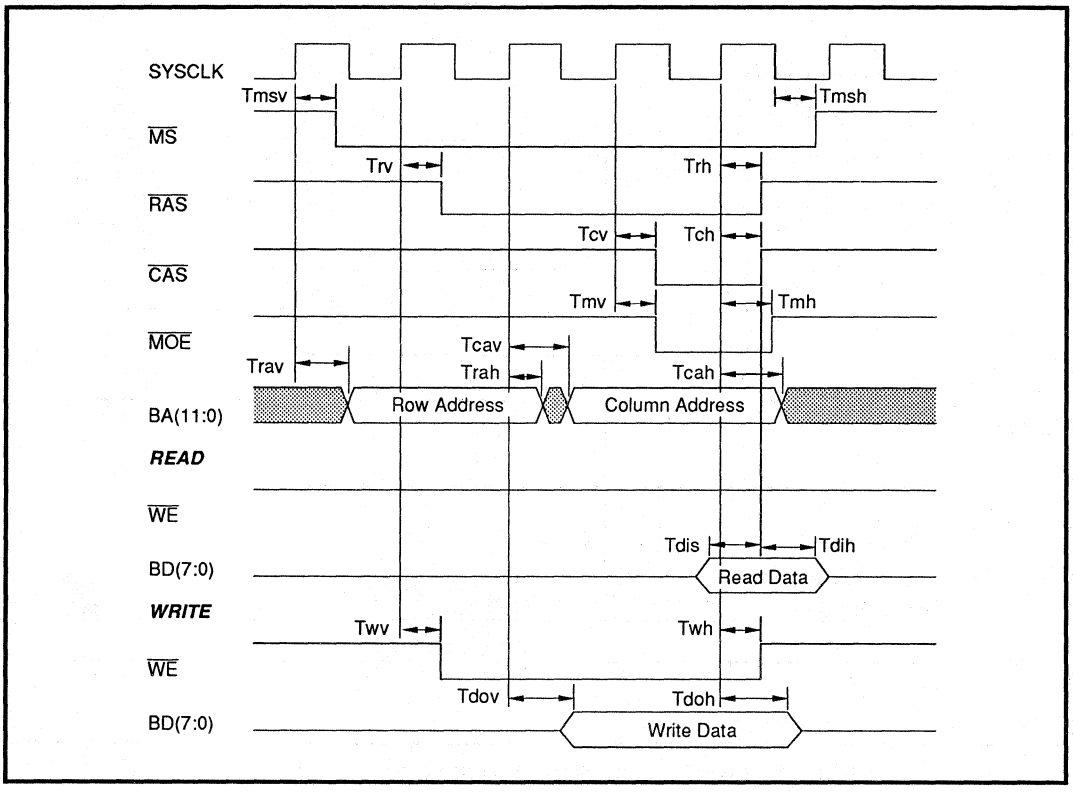

FIGURE 11: DRAM Timing, Standard Cycle (Shown with RWL = 0 and CWL = 0)

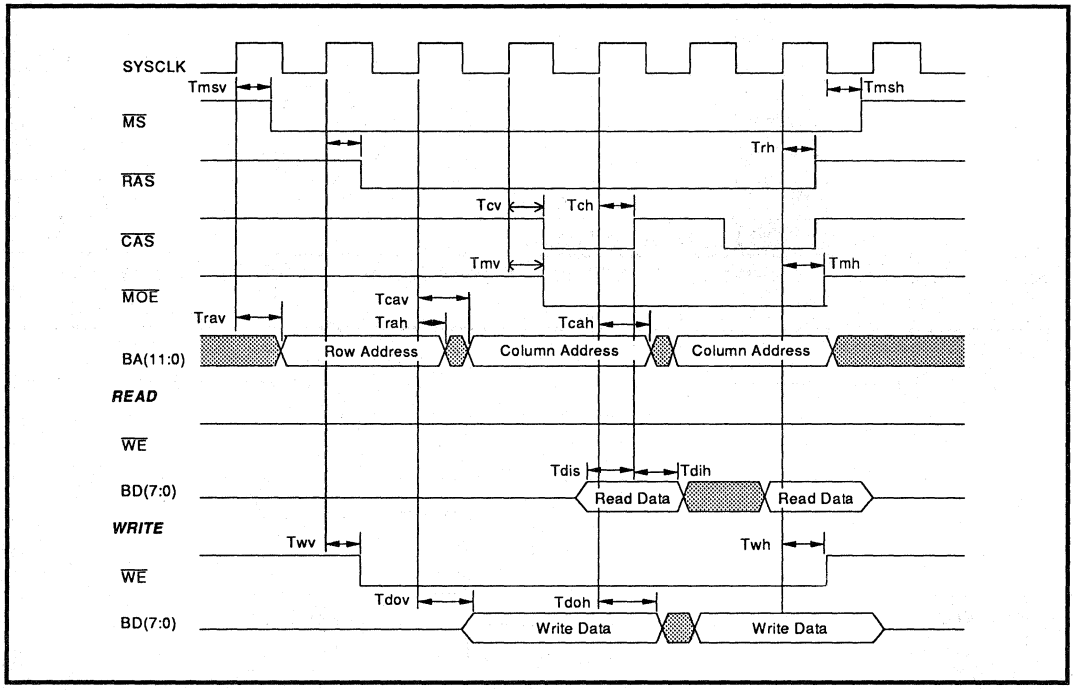

FIGURE 12: DRAM Timing, Fast Page Cycles (Shown with RWL = 0, RWH = 0, CWL = 0 and CWH = 0)

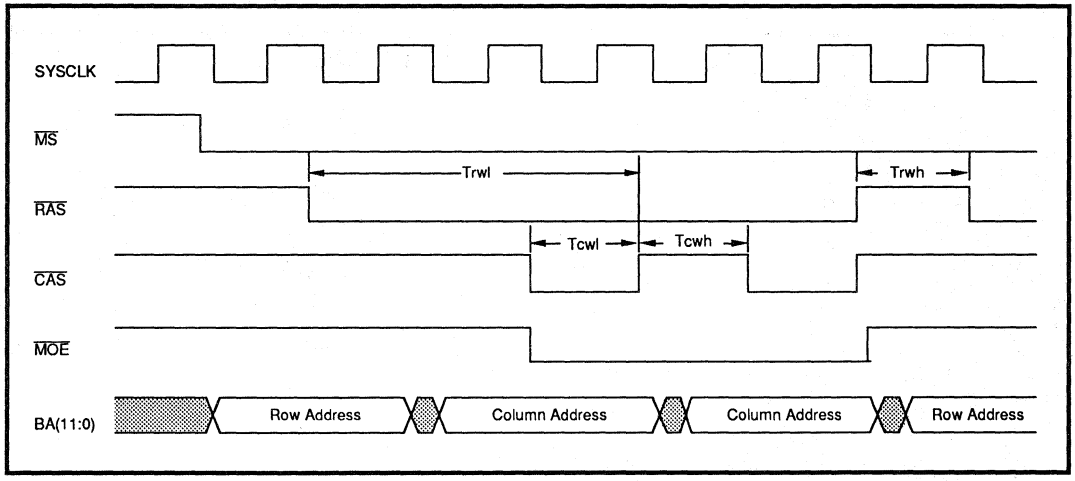

FIGURE 13: DRAM Timing (Showing the Relationship of RWL, RWH, CWL and CWH to overall timing)

SCSI Asynchronous Timing Paraemeters

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
Tods	Data Setup to $\overline{ACK}\downarrow$	SCSI Output Phase	5			ns
Todh	Data Hold from $\overline{ACK}\downarrow$	SCSI Output Phase	12			ns
Talrh	$\overline{ACK}\downarrow$ to $\overline{REQ}\uparrow$				49	ns
Tids	Data Setup to $\overline{REQ}\downarrow$	SCSI Input Phase	80			ns
Tidh	Data Hold from $\overline{ACK}\downarrow$	SCSI Input Phase	29			ns

Note: All timing parameters are measured with 200 pf load, two SCSI terminator loads with $\overline{ACK}$ Filter turned off.

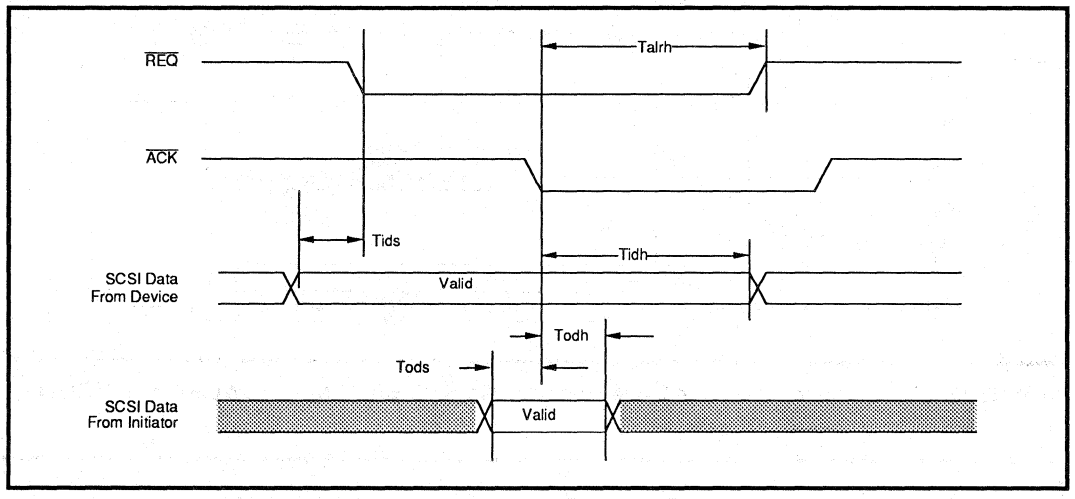

FIGURE 14: SCSI Asynchronous Timing

SCSI Synchronous Timing Paramenters

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
Trh	$\overline{REQ}$ Assertion Time		37		48	ns
Trl	$\overline{REQ}$ Deassertion Time		63		52	ns
Tids	Setup time SCSI Data to $\overline{REQ}\downarrow$	Write to SCSI bus	43			ns
Tidh	Hold time $\overline{REQ}\downarrow$ to SCSI Data invalid	Write to bus	43			ns
Tal	Minimum $\overline{ACK}$ Assertion Width Required		10			ns
Tods	Data Setup to $\overline{ACK}\downarrow$	Read from the SCSI bus	5			ns
Todh	Data Hold from $\overline{ACK}\downarrow$	Read from the SCSI bus	12			ns

Note: All timing parameters are measured with 200 pf load, two SCSI terminator loads, $\overline{ACK}$ filter turned off.

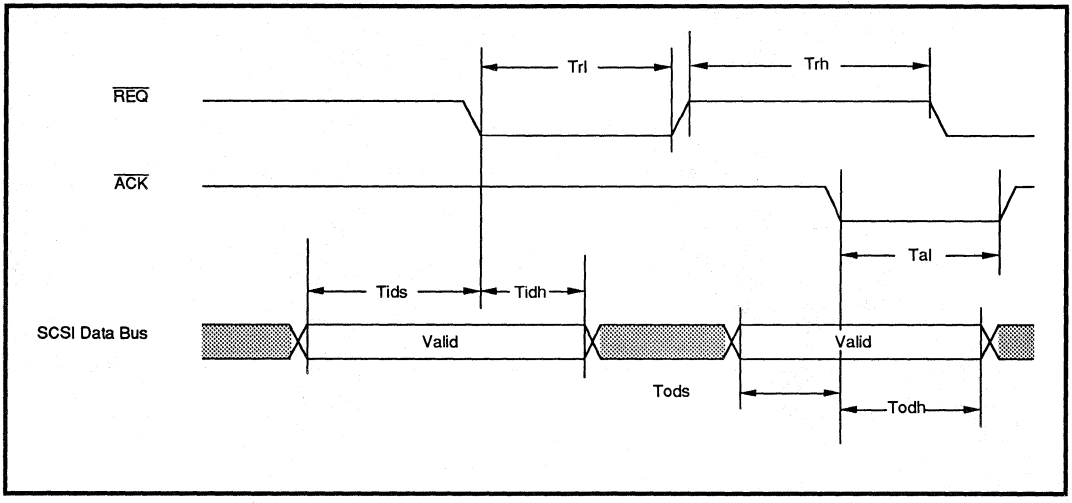

FIGURE 15: SCSI Synchronous Timing

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Synchronous Data In/Out Phase

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
Txtrp*	Synchronous Transfer Period	(see note)				ns
Tsrl	SYSFREQ high to $\overline{REQ}$ low				50	ns
Tsrh	SYSFREQ high to $\overline{REQ}$ high				60	ns
Tdov	SYSFREQ high to data out valid				40	ns
Tdsu	Data setup to $\overline{ACK}$ low		55			ns
Tdh	Data hold from $\overline{ACK}$ low		40			ns

Note: Txtrp is the Synchronous Transfer Period as defined by the Synchronous Control Register (Reg: 43H). SYSFREQ is a function of the BUFCLK and is determined by the prescale value as defined by the Clock Control Register (Reg: 49H).

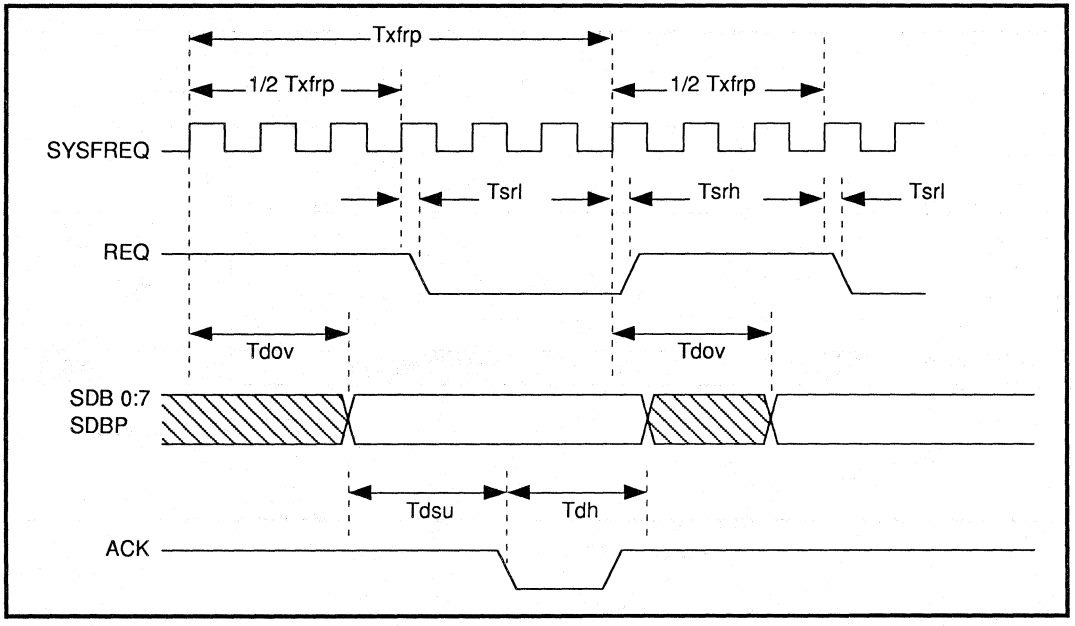


FIGURE 16: Even Number of SYSFREQ Cycles/SCSI Transfer Period

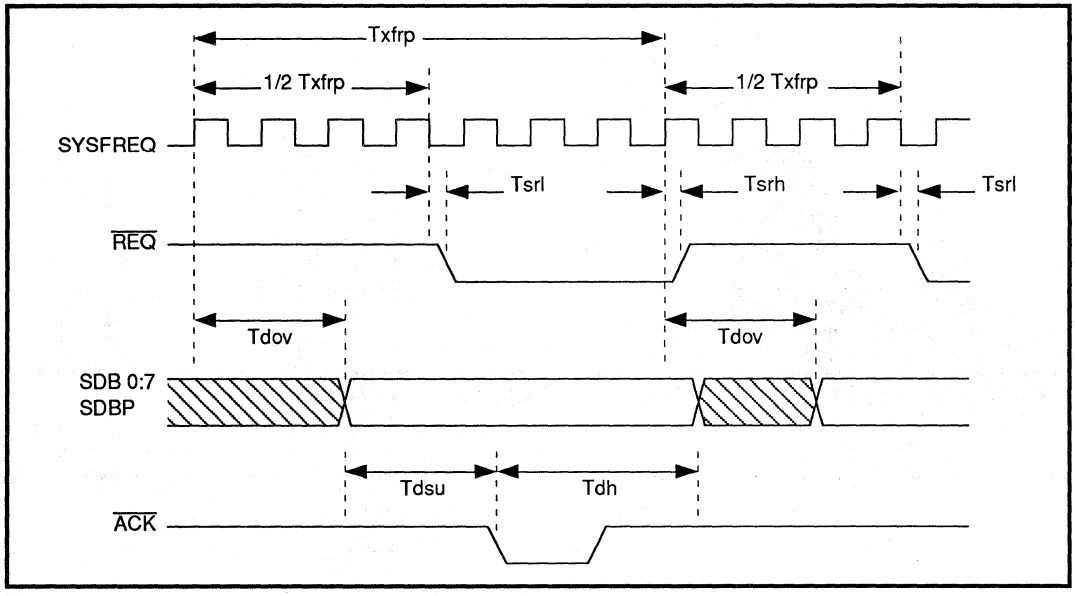


FIGURE 17: Odd Number of SYSFREQ Cycles/SCSI Transfer Period

Wait for Selection

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Tbsd Bus Settle Delay (400 ns) to the assertion of $\overline{BSY}$		3T + 90		4T + 90	ns

Note: T is the SCSI Clock Period (SCP) as defined in Register 49H (CLKCTL).

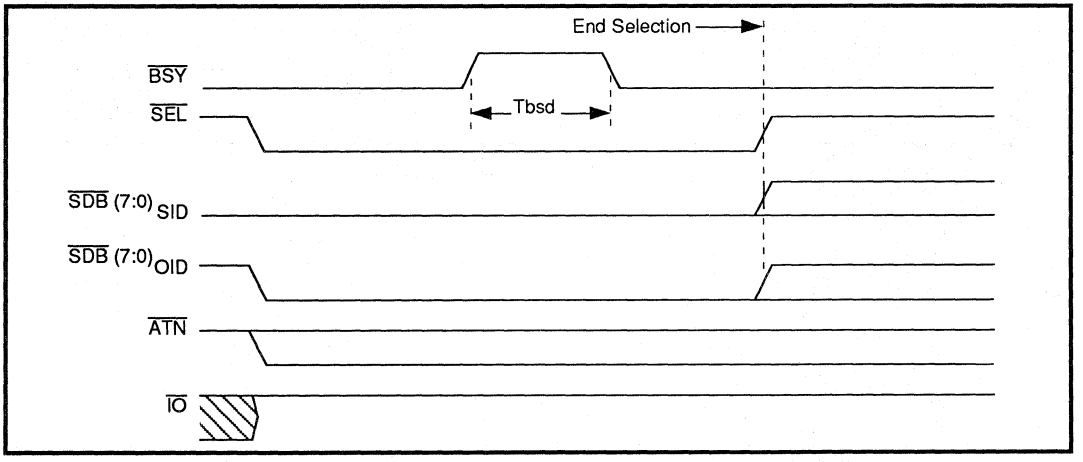


FIGURE 18: Wait for Selection

Arbitration

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Tbfsd Bus Settle Delay (400 ns) + Bus Free Delay (800 ns) to the assertion of BSY and $\overline{SDB}_{OID}$		6T + 110		7T + 110	ns
Tad Arbitration Delay (2.4 µsec) to the assertion of $\overline{SEL}$ (win) or deassertion of $\overline{BSY}$ and $\overline{SDB}_{OID}$ (lost)		-		13T + 100	ns
Tbcsd Bus Clear Delay (800 ns)+ Bus Settle Delay (400 ns) to end of Arbitration Phase		-		6T + 100	ns

Note: T is the SCSI Clock Period (SCP) as defined in Register 61H (CLKCTL).

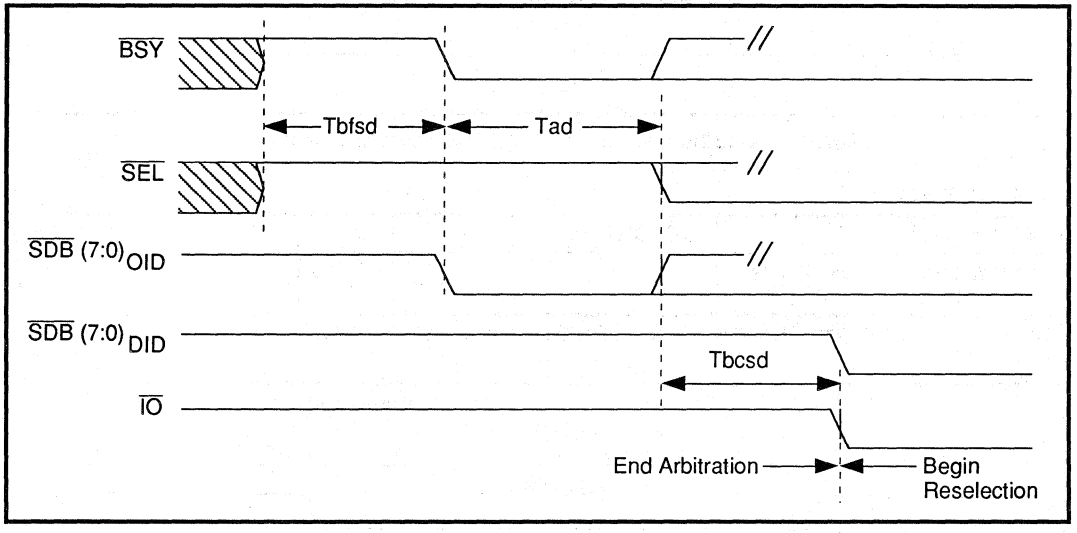


FIGURE 19: Arbitration

Reselection

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
Tbcsd	Bus Clear Delay (800 ns) + Bus Settle Delay (400 ns) to end of Arbitration Phase		-		6T + 100	ns
Tdskd1	Two Deskew Delays (90 ns) to the deassertion of $\overline{BSY}$		-		160	ns
Tbsd	Bus Settle Delay (400 ns) to the assertion of $\overline{BSY}$		-		2T + 40	ns
Tdskd2	Two Deskew Delays (90 ns) to the deassertion of SEL, $\overline{SDB}_{OID}$, and $\overline{SDB}_{DID}$		1T +70		2T + 70	ns

Note: T is the SCSI Clock Period (SCP) as defined in Register 61H (CLKCTL).

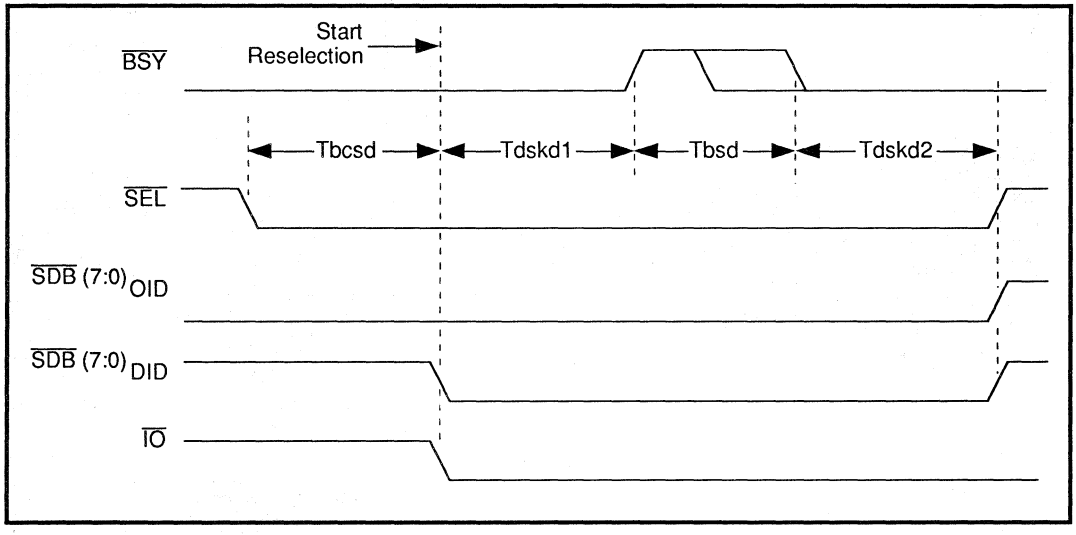
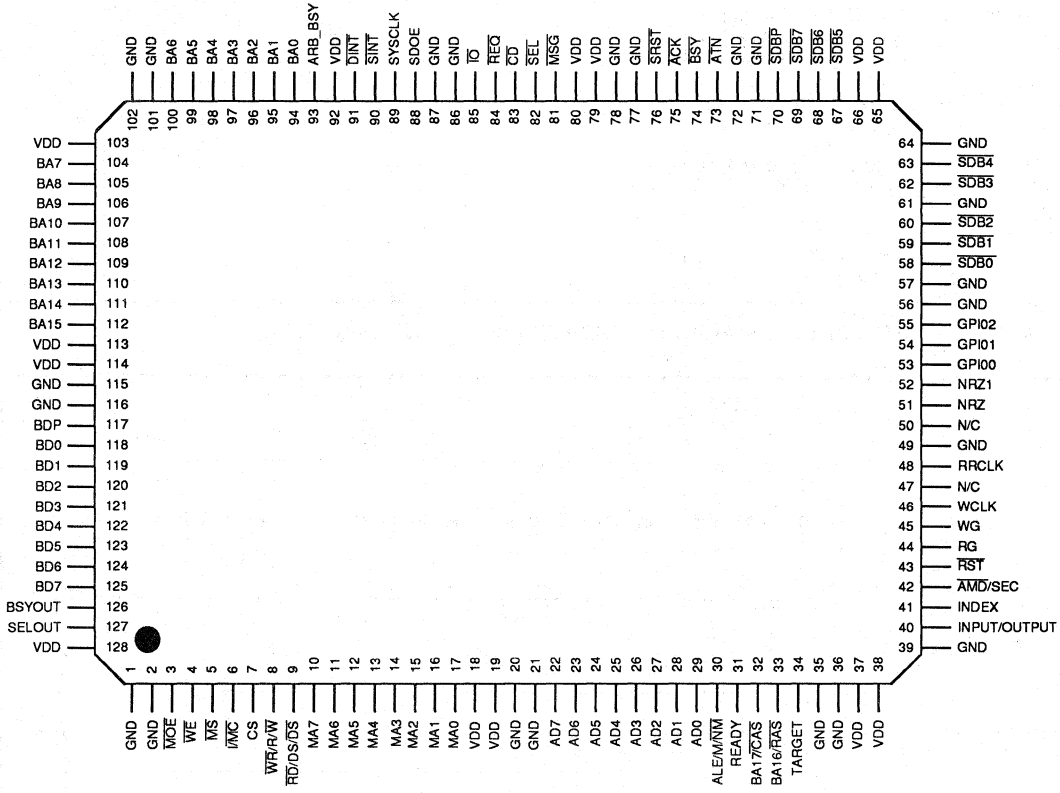


FIGURE 20: Reselection

SSI 32C9024
Differential SCSI Combo Controller
80 Mbit/s; dual bit NRZ interface

PACKAGE PIN DESIGNATIONS

(Top View)



128-Lead QFP

CAUTION: Use handling procedures necessary for a static sensitive component.

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX: (714) 573-6914

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SSI 32C9301
PC-AT Combo Controller With Reed Solomon, 3V Operation

Advance Information

January 1994

DESCRIPTION

The SSI 32C9301 is an advanced CMOS VLSI device which integrates major portions of the hardware needed to build an ATA disk drive. The SSI 32C9301 can operate on 3.3 volts or 5 volts allowing use in 3.3 volt or 5 disk drives. The circuitry of the SSI 32C9301 includes a complete ATA interface, an advanced buffer manager, a high performance disk formatter and an 88 bit Reed-Solomon ECC with fast "on-the-fly" hardware correction. The SSI 32C9301 provides maximum performance while minimizing micro controller intervention.

When operating in a 3.3 volt environment, the SSI 32C9301 is capable of concurrent transfers of up to 48 megabits per second on the disk interface and 3 megawords (16 bit transfers) per second across the

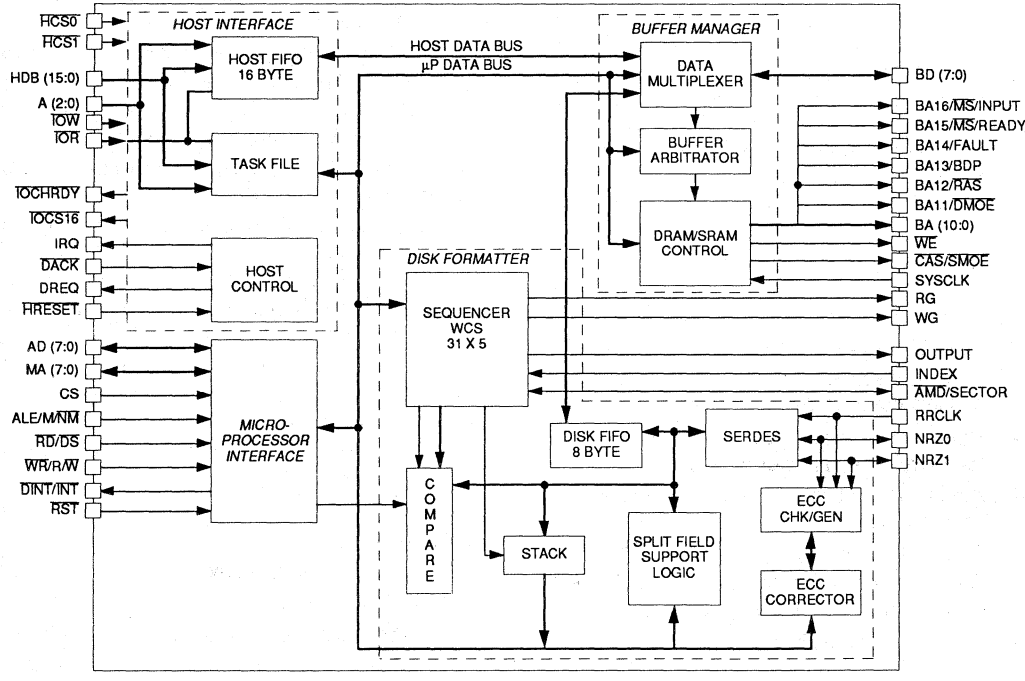
(continued)

FEATURES

- **ATA Interface**
  - **Single Chip PC AT Controller**
  - **Full ANSI ATA Compliance**
  - **Direct PC Bus connection with on board 8 mA (12 mA @5v) drivers**
  - **PC transfers to 4 (6.7 @5v) megawords per second**
  - **Supports PIO, DMA and multiword DMA (EISA Class B Demand DMA)**
  - **Logic for daisy chaining 2 drives**
  - **Operates as master, slave or both**
  - **Automatic command decoding of write, write long, write DMA, write multiple, write buffer and format commands**

(continued)

BLOCK DIAGRAM



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SSI 32C9301
PC-AT Combo Controller
With Reed Solomon, 3V Operation

DESCRIPTION (continued)

ATA bus. In a 5 volt environment, the SSI 32C9301 is capable of concurrent transfers of up to 48 megabits per second on the disk interface and 6 megawords per second across the ATA bus. The SSI 32C9301 is capable of performing concurrent disk data transfers, host data transfers, on-the-fly error corrections and micro controller accesses of the buffer memory without any degradation of performance on any interface.

The SSI 32C9301 is one of a family of Silicon Systems' single chip disk controllers which support a wide range of device interfaces. The SSI 32C9001 is a 5 volt only version of the 32C9301 which is 100% firmware and pin out compatible. The 32C9302 is another 3.3/5 volt ATA controller which supports a dual NRZ disk formatter interface. The SSI 32C9020, SSI 32C9022, SSI 32C9023 and SSI 32C9024 family members are SCSI disk controllers. The SSI 32C9340 disk controller completes the family by providing PCMCIA/ATA compliant interfaces. All members are based on a common architecture allowing major portions of firmware to be reused. The Silicon Systems' chip family is illustrated in hierarchy chart shown in Figure 1.

The high level of integration within the SSI 32C9301 represents a major reduction in parts count. When the SSI 32C9301 ATA Controller is combined with the SSI 32R2300 Read/Write device, the SSI 32P4330 Pulse Detector with 1,7 ENDEC, the SSI 32H6300 Servo and Motor Speed Controller, an appropriate micro controller and memory, a complete, cost efficient, high performance intelligent drive solution is created.

FEATURES (continued)

- Automatic updates of the host task file registers in both Cyl/Hd/Sec and LBA modes
- Hardware support for write-multiple and read-multiple commands.
- Hardware added to provide Multi-Sector data transfers without microprocessor intervention
- Automatic Host Interrupt and Busy for multiple sector transfers
- 16 byte FIFO to improve performance
- Separate host interface VDD to allow 3.3 volt drives to plug into 5 volt systems
- Power Down I/O pins

- Buffer Manager
  - Direct support of DRAM or SRAM
  - SRAM: up to 128k bytes of memory with throughput to 16 (20 @5v) megabytes per second
  - DRAM: up to 1 megabyte of memory with throughput to 12 (17.78 @5v) megabytes per second
  - Programmable memory timing
  - Supports page mode DRAM access
  - Programmable page mode burst length
  - Programmable DRAM refresh period
  - Buffer RAM segmentation with flexible segment sizes from 256 bytes to 1 megabyte
  - Dedicated host, disk and microprocessor address pointers
  - Buffer Streaming with internal buffer protection circuit providing buffer integrity
- Disk Formatter
  - NRZ Data Rates to 48 megabits per second
  - Automatic multi-sector transfer
  - Header or microprocessor based split data field support
  - Advanced sequencer organized in 31 x 5 bytes
  - Advanced branch and interrupt logic
  - 88-bit Reed Solomon ECC with "on-the-fly" fast hardware correction circuitry
  - Capable of correcting up to four 10-bit symbols in error
  - Guaranteed to correct one 31-bit burst or two 11-bit bursts
  - Hardware on-the-fly correction of either an 11- bit single burst error within one half of a sector time
  - Detects up to one 51-bit burst or three 11-bit bursts
- Microprocessor Interface
  - Supports both Intel and Motorola microprocessors
  - Separate or combined host and disk interrupts
- Other Features
  - Internal power down mode
  - Available in 100-pin TQFP
  - Automatic power supply level detection
  - Conforms to JEDEC 3.3 volt specifications
  - TTL compatible input receivers at 3.3V or 5V

FUNCTIONAL DESCRIPTION

The SSI 32C9301 contains the following four major functional blocks:

Microprocessor Interface

ATA Interface

Disk Formatter

Buffer Manager

The Microprocessor Interface allows the local microprocessor access to all of the SSI 32C9301 internal control registers and any location within the buffer memory. The microprocessor, by writing and reading the internal registers, can control all activities of the SSI 32C9301. The microprocessor can elect to perform host and/or disk operations directly, or it can enable the advanced features of the SSI 32C9301 which can perform these operations automatically.

The ATA Interface block handles all PC AT bus activities. The ATA interface includes 8 mA (12 mA @5v) drivers allowing for direct connection of the SSI 32C9301 to the PC AT bus. The ATA interface block is highly automated, capable of performing multiple block transfers without micro controller involvement. The ATA block interfaces directly with the Buffer Manager via an internal speed matching FIFO. This FIFO, the bandwidth capabilities of the Buffer Manager, plus the advanced features of the ATA Interface guarantee sustained full speed transfers across the PC AT bus.

The Disk Formatter performs the serialization and deserialization of data. It provides all of the necessary functions to control track formatting, header search, and the reading and writing of data. The heart of the Disk Formatter is an advanced programmable sequencer. The sequencer can contain 31 instructions, each of which is 5 bytes (40 bits) in width. The width of the instructions allows for sophisticated branching techniques which increase the flexibility and power of the sequencer. The disk interface can be configured through a wide range of capabilities, allowing the SSI 32C9301 to interface with nearly any read/write channel. This allows the user of the SSI 32C9301 to select the read/write channel best suited to the device. Of course, by selecting the SSI 32C9301 controller and the SSI 32P4330 Read Channel with 1,7 ENDEC, you are guaranteed a problem free interface.

Within the Disk Formatter are the ECC generator/checker and ECC corrector. The generator/checker provides the ability to generate or check a 32-bit ECC for headers and an 88-bit Reed Solomon code for data. If the checker detects an error using the 88-bit Reed Solomon code, the syndrome information is transferred

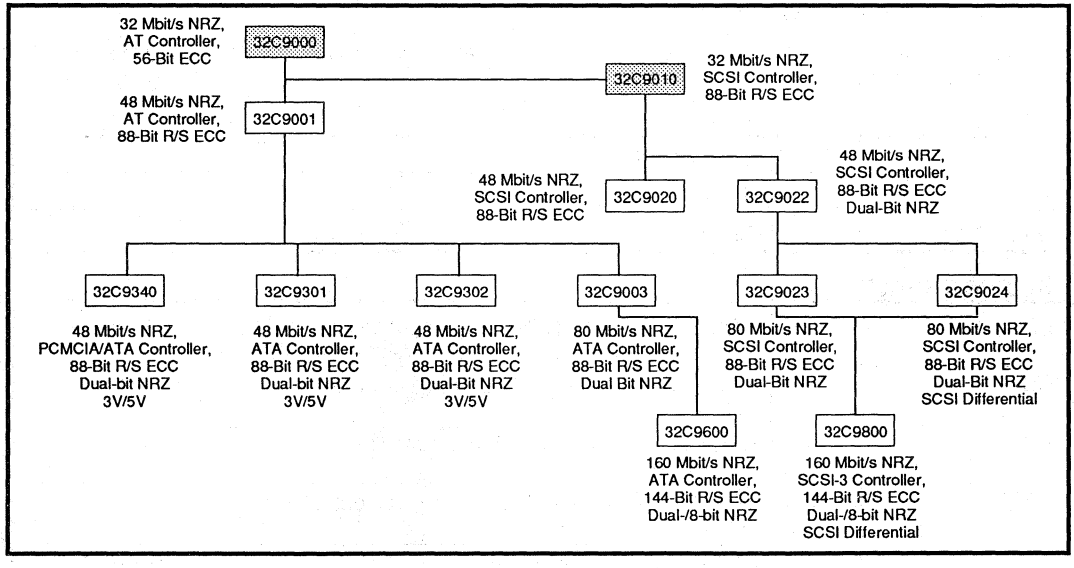


FIGURE 1: Silicon Systems' Disk Controller Chip Hierarchy

FUNCTIONAL DESCRIPTION (continued)

into the corrector. The corrector then performs the necessary operations to determine if the error was correctable and, if it was correctable, the corrector interfaces directly with the buffer controller and performs the correction automatically. The corrector performs its correction within one quarter of a sector. This guarantees that the corrector will always be available to correct the next sector if necessary.

The Buffer Manager manages the data buffer of the controller. The Buffer Manager can support either SRAM or DRAM. When configured to operate with DRAM, the Buffer Manager automatically performs necessary refresh cycles. The buffer manager creates all of the necessary timing and control signals for a wide range of memory types and speeds. Besides interfacing with the buffer memory, the Buffer Manager interfaces with the ATA Interface block, the Disk Formatter block, the ECC corrector of the Disk Formatter block and the microprocessor. If more than one of these devices requires access to the buffer memory, the Buffer Manager arbitrates the requests automatically. The Buffer Manager of the SSI 32C9301 can sustain ATA operations at the rate of 3 (6 @5v) megawords per second, Disk Formatter operations at 48 megabits per second and still has sufficient band width left to handle on-the-fly ECC corrections and microprocessor accesses without degrading performance on any of the interfaces.

PIN DESCRIPTION

The following convention is used in the pin description:

- (I) denotes an input
- (I/S) denotes a Schmitt trigger input
- (O) denotes an output
- (I/O) denotes a bidirectional signal
- (Z) denotes a tri-state output
- (OD) denotes an open drain output

Active low signals are denoted by a bar on top of the signal name and dual function pins are denoted with a slash between the two signals — $\overline{\text{AMD}}$/SECTOR

GENERAL

NAME	TYPE	DESCRIPTION
VDD		POWER SUPPLY PIN
GND		GROUND

HOST INTERFACE

A(2:0)	I	HOST ADDRESS LINES. The Host Address lines A(2:0) and A9 are used to access the various PC/AT control/status, and data registers.
$\overline{\text{HCS1}}$	I	HOST CHIP SELECT 1. This pin is used to select the control block task file register.
$\overline{\text{HCS0}}$	I	HOST CHIP SELECT 0. This pin is used to access the command block task file registers.
$\overline{\text{IOCS16}}$	OD	16 BIT DATA TRANSFER. An active low output that indicates that a 16-bit buffer transfer is active.
IRQ	O	INTERRUPT REQUEST. Asserted active high to indicate to the Host that the controller needs attention.

HOST INTERFACE (continued)

NAME	TYPE	DESCRIPTION
$\overline{\text{IORDY}}$	O,Z	I/O READY. Active low, this signal is asserted whenever the internal host FIFO is not ready to transfer data.
DREQ	O,Z	DMA REQUEST. The active high DMA Request signal is used during DMA to transfer between the Host and the SSI 32C9301.
$\overline{\text{DACK}}$	I	DMA ACKNOWLEDGE. This active low signal is used during DMA to transfer data between the host and the controller.
$\overline{\text{IOR}}$	I	INPUT READ SELECT. This active low pin is asserted by the Host during a Host read operation. When asserted with $\overline{\text{HCS0}}$, $\overline{\text{HCS1}}$, or $\overline{\text{DACK}}$, data from the device is enabled onto the host data bus.
$\overline{\text{IOW}}$	I	INPUT WRITE SELECT. Asserted active low by the HOST during a HOST write operation. When asserted with $\overline{\text{HCS0}}$, $\overline{\text{HCS1}}$, or $\overline{\text{DACK}}$, data from the host data bus is strobed into the device.
$\overline{\text{HRESET}}$	I	HOST RESET. This active low signal stops all commands in progress and initializes the control/status registers. This signal can also "wake up" the device while it is in power down mode.
HDB(15:0)	I/O	HOST DATA BUS. These bits are used for word transfers between the Buffer Memory and the Host; bits (7:0) are used for status, commands, or ECC byte transfers.
$\overline{\text{PDIAG}}$	I,OD	PASSED DIAGNOSTICS. This pin is used as the Passed Diagnostics signal, and may be an input or an open-drain output.
$\overline{\text{DASP}}$	I, OD	DRIVE ACTIVE-SLAVE PRESENT. This pin is used as the Drive Active/ Slave Present signal, and is an input or and open-drain output. This pin is used for Master/Slave drive communication and/or for driving an LED.

DISK INTERFACE

INDEX/INPUT	I	INDEX/INPUT. This pin serves as the index function for the disk sequencer. When the INPUT function is not available on the BA16 pin, this pin can function as input or index.
OUTPUT	O	DISK SEQUENCER OUTPUT. This pin is controlled by bit 2 of the control field of the disk sequencer.
$\overline{\text{AMD}}$/SECTOR	I/O	ADDRESS MARK DETECT/SECTOR. In Hard Sector mode, this is the input for the sector pulse from the disk drive. In Soft Sector mode, a low-level input during a read indicates an address mark was detected.
RG	O	READ GATE. This active high output enables the reading of the disk. It is asserted at the beginning of the PLO for header and data field by the sequencer — sequencer Control Field bits 5 and 6. It is automatically deasserted at the end of the CRC or ECC.

PIN DESCRIPTION (continued)

DISK INTERFACE (continued)

NAME	TYPE	DESCRIPTION
WG	O	WRITE GATE. This active high output enables writing onto the disk. It is asserted and deasserted by the sequencer Control Field bits 5 and 6.
RRCLK	I	READ/REFERENCE CLOCK. This pin is used in conjunction with the NRZ pin to clock data in and out of the SSI 32C9001 device. This input must be glitch-free to ensure correct operation of the chip.
NRZ0	I/O	NRZ BIT 0. This signal is the read data input from the disk drive when the read gate signal is asserted; it is the write data output to the disk drive when the write gate signal is asserted. This pin is used for the least significant bit in dual bit NRZ mode; it is used for the serial data stream in single bit NRZ mode.
NRZ1	I/O	NRZ BIT 1. This signal is the read data input from the disk drive when the read gate signal is asserted; it is the write data output to the disk drive when the write gate signal is asserted. This pin is used for the most significant bit in dual bit NRZ mode; it is not used in single bit NRZ mode.

MICROPROCESSOR INTERFACE

$\overline{RST}$	I/S	RESET. An asserted active low input generates a component reset that holds the internal registers of the SSI 32C9301 at reset, stops all operations within the chip, and deasserts all output signals. All input/output signals and Host outputs are set to the high-Z state.
ALE/M/$\overline{NM}$	I	ADDRESS LATCH ENABLE/MULTIPLEXED/NON-MULTIPLEXED ADDRESS SELECT. When tied high or left floating after reset, the microprocessor interface is configured as non-multiplexed. When driven low, then the microprocessor interface is configured as multiplexed. In this case this pin functions as the address latch enable, and the MA(7:0) pins are the demultiplexed address outputs.
CS	I	CHIP SELECT. This signal must be asserted high for all microprocessor accesses to the registers of this chip.
$\overline{WR}$/R/$\overline{W}$	I	WRITE STROBE/READ/WRITE. In the Multiplexed Microprocessors bus mode, when an active low signal is present with CS signal asserted high, the data on the AD0:7 is written to the internal registers. In the Non-Multiplexed Microprocessors bus mode, this signal acts as the R/$\overline{W}$ signal. A high on this input along with the $\overline{RD}$/DS signal high and the CS signal asserted high indicates a read operation. A low on this input along with the $\overline{RD}$/DS signal asserted and the CS signal asserted high indicates a write operation. See table below.

I/$\overline{MC}$	CS	$\overline{WR}$/R/$\overline{W}$	$\overline{RD}$/DS	Action	Mux/Non-Mux
High	High	Low	High	Write to internal registers.	M
High	High	High	Low	Read from internal registers.	M
Low	High	Low	High	Write to internal registers.	N
Low	High	High	High	Read from internal registers.	N
X	Low	X	X	No action.	M or N

Note: X denotes don't care.

MICROPROCESSOR INTERFACE (continued)

$\overline{RD}/\overline{DS}$	I	READ STROBE/DATA STROBE. In the Multiplexed Microprocessors bus mode, when an active low signal is present with CS signal high, internal registers will be accessed. In the Non-Multiplexed Microprocessors mode, this signal acts as the DS signal. A high on the DS, R/$\overline{W}$, and the CS signals, indicates a read operation. A low on the R/$\overline{W}$ signal, highs on both the DS and the CS, indicates a write operation to the internal registers.
$\overline{DINT}/\overline{INT}$	O, OD, Z	INTERRUPT. An active low signal indicates the controller is requesting microprocessor service from the disk side. This signal is programmable for either a push-pull with an internal pull up resistor or open-drain output circuit. This signal powers up in the high-Z state. Disk Formatter Mode Control Register, 4FH: bit 3 set high, programs this pin as a push-pull, and when set low programs it as an open drain output signal.
AD(7:0)	I/O	ADDRESS/DATA BUS. When configured in the Multiplexed Microprocessors mode, these lines are multiplexed, bidirectional data path to the microprocessor. During the beginning of the memory cycle the bus captures the low order byte of the microprocessor address. These lines provide communication with the controller device's internal registers and the buffer memory. When configured in the Non-Multiplexed Microprocessors mode, these lines are bidirectional data lines.
MA(7:0)	I/O	MICROPROCESSOR ADDRESS BUS: This 8-bit output bus is the AD(7:0) bus latched by the ALE pin during the low order address phase of an Multiplexed Microprocessors type microprocessor cycle. These signals are nonmultiplexed address input when used with a non-multiplexed bus microprocessor — Non-Multiplexed Microprocessors interface.

BUFFER MANAGER INTERFACE

BA16/$\overline{MS}$/INPUT	I/O	BUFFER ADDRESS 16/MEMORY SELECT/DISK INPUT. In SRAM mode, this pin may be configured as buffer address 16, memory select, or as the input pin to the disk sequencer. In DRAM mode, this pin is configured as the input pin. If the input function is not available on this pin, then the INDEX pin may be used for the index function or the input function.
BA15/$\overline{MS}$/READY/$\overline{AINT}$	O	BUFFER ADDRESS 15/MEMORY SELECT/AT INTERRUPT/READY. In SRAM mode, this pin may be configured as buffer address 15, memory select, as a separate local microprocessor interrupt for the host interface, or as the ready function for adding wait states to local microprocessor accesses. In DRAM mode, AT interrupt or Ready may be selected. After $\overline{RST}$ is asserted, this signal is configured as Ready.
BA14/FAULT	I/O	BUFFER MEMORY ADDRESS 14/DISK FAULT. This signal is used for addressing the buffer memory in SRAM mode, or as the disk fault pin in DRAM mode. Assertion of the fault pin will cause the disk sequencer to halt immediately.
BA13/BDP	I/O	BUFFER MEMORY ADDRESS 13/BUFFER MEMORY PARITY. This signal is used for addressing the buffer memory in SRAM mode, or as the buffer data parity value in DRAM mode.

PIN DESCRIPTION (continued)

BUFFER MANAGER INTERFACE (continued)

NAME	TYPE	DESCRIPTION
BA12/$\overline{RAS}$	O	BUFFER MEMORY ADDRESS 12/ROW ADDRESS STROBE: This signal is used for addressing the buffer memory in SRAM mode or as the row address strobe in DRAM mode. After $\overline{RST}$ is asserted, this signal will be high.
BA11/$\overline{DMOE}$	O	BUFFER MEMORY ADDRESS 11/DRAM MEMORY OUTPUT ENABLE. This signal is used for addressing the buffer memory in SRAM mode, or as the memory output enable pin in DRAM mode. After $\overline{RST}$ is asserted, this signal will be high.
BA(10:0)	O	BUFFER MEMORY ADDRESS LINES. These are signals 10-0 for addressing the buffer memory.
BD(7:0)	I/O	BUFFER MEMORY DATA BUS. 7 through 0. The bidirectional Data Bus connects directly to the buffer memory. This bus is designed for high speed data transfer.
$\overline{CAS}$/$\overline{SMOE}$	O	COLUMN ADDRESS STROBE/SRAM MEMORY OUTPUT ENABLE. This signal is used as the column address strobe in DRAM mode, or the memory output enable in SRAM mode. After $\overline{RST}$ is asserted, this signal will be high.
$\overline{WE}$	O	MEMORY OUTPUT ENABLE. This active low output signal is used to strobe the data into the RAMs from the Data bus. For both buffer memory applications, this line is tied directly to the SRAM or DRAM control pin.
SYSCLK	I	SYSTEM CLOCK. This signal is used to synchronize the buffer RAM access, including the generation of memory address lines, write enable WE, and memory output enable MOE. In power down mode, this signal is shut off from the internal logic and hence buffer memory access is inhibited.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC operating characteristics.

PARAMETER	RATING
Power Supply Voltage, VCC	7V
Ambient Temperature	0 to 70°C
Storage Temperature	-65 to 150°C
Power Dissipation	750 mW
Input, Output pins	-0.5 to VCC + 0.5V

ELECTRICAL CHARACTERISTICS

PARAMETER		CONDITIONS	MIN 3.3V	MAX 3.3V	MIN 5V	MAX 5V	UNIT
VDD	Power Supply Voltage		3	3.6	4.5	5.5	V
IDD	Supply Current			30		50	mA
IDDS	Standby Current	Note 1		250		250	µA
VIL	Input Low Voltage		-0.5	0.8	-0.5	0.8	V
VIH	Input High Voltage	Except $\overline{RST}$ pin	2	VCC + 0.5	2	VCC + 0.5	V
VIH	Input High Voltage	$\overline{RST}$ pin	2	VCC + 0.5	3.9	VCC + 0.5	V
VOL	Output Low Voltage	Note 2		0.4		0.4	V
VOL	Output Low Voltage	Note 3		0.5		0.5	V
VOH	Output High Voltage	IOH = -400 µA	2.15		2.4		V
IL	Input Leakage Current	0 < VIN < VCC	-10	10	-10	10	µA
CIN	Input Capacitance			10		10	pF
COUT	Output Capacitance			10		10	pF

Note: (1) Synchronization and Clock Control Register, 7FH: bits 3 and 4 set. RRCLK and SYSCLK internally inhibited.

(2) All interface pins except Host Interface pins. IOL = 2 mA.

(3) Host Interface pins, IOL = 16 mA @ 3.3V, IOL = 24 mA @ 5.0V.

ELECTRICAL SPECIFICATIONS (continued)

MICROPROCESSOR INTERFACE TIMING PARAMETERS

Multiplexed Bus Interface Timings (Figures 2, 3, 4, 5)

PARAMETER		CONDITIONS	MIN 3.3V	MAX 3.3V	MIN 5V	MAX 5V	UNIT
Ta	ALE Width		20		20		ns
Tma	Address valid to MA (7:0) valid			45		30	ns
Tr	$\overline{RD}$ Width		80		80		ns
As	Address valid to ALE ↓		5		5		ns
Ah	ALE ↓ to address invalid		10		10		ns
Cs	CS valid to $\overline{RD}$ ↓ or $\overline{DS}$ ↓		20		20		ns
Ch	$\overline{RD}$ ↑ or $\overline{DS}$ ↑ to CS ↓		0		0		ns
Tda	$\overline{RD}$ ↓ or $\overline{DS}$ ↓ to read data valid	Except Read of WCS		40		30	ns
Tda	$\overline{RD}$ ↓ or $\overline{DS}$ ↓ to read data valid	Read of WCS		60		50	ns
Tds	$\overline{DS}$ width		80		80		ns
Tdh	RD ↑ to or $\overline{DS}$ ↑ read data invalid		0	25	0	25	ns
Tsrw	R/$\overline{W}$ valid to $\overline{DS}$ ↓		20		20		ns
Thrw	$\overline{DS}$ ↑ to R/$\overline{W}$ invalid		20		20		ns
Tdrdy	$\overline{RD}$ ↓ to READY ↓ (Intel) or $\overline{DS}$ ↓ to READY ↓ (Motorola)			45		30	ns ns
Wds	Write data valid to $\overline{WR}$ ↑ or $\overline{DS}$ ↑		40		40		ns
Wdh	$\overline{WR}$ ↑ or $\overline{DS}$ ↑ to write data invalid		10		10		ns

Non-Multiplexed Bus Interface Timings (Figure 6)

Tmas	MA (7:0) valid to $\overline{DS}$ ↓		5		5		ns
Tmah	$\overline{DS}$ ↑ to MA (7:0) invalid		5		5		ns
Cs	CS valid to $\overline{DS}$ ↓		20		20		ns
Ch	$\overline{DS}$ ↑ to CS ↓		0		0		ns
Tda	$\overline{RD}$ ↓ or $\overline{DS}$ ↓ to read data valid	Except Read of WCS		40		30	ns
Tda	$\overline{RD}$ ↓ or $\overline{DS}$ ↓ to read data valid	Read of WCS		60		50	ns
Tds	$\overline{DS}$ width		80		80		ns
Tdh	$\overline{DS}$ ↑ to read data invalid		0	25	0	25	ns
Tsrw	R/$\overline{W}$ valid to $\overline{DS}$ ↓		20		20		ns
Thrw	$\overline{DS}$ ↑ to R/$\overline{W}$ invalid		20		20		ns
Tdrdy	$\overline{DS}$ ↓ to READY ↓ (Motorola)			45		30	ns
Wds	Write data valid to $\overline{WR}$ ↑ or $\overline{DS}$ ↑		40		40		ns
Wdh	$\overline{WR}$ ↑ or $\overline{DS}$ ↑ to write data invalid		10		10		ns

Note: (1) Loading capacitor = 30 pF
(2) ↑ indicates rising edge ↓ indicates falling edge

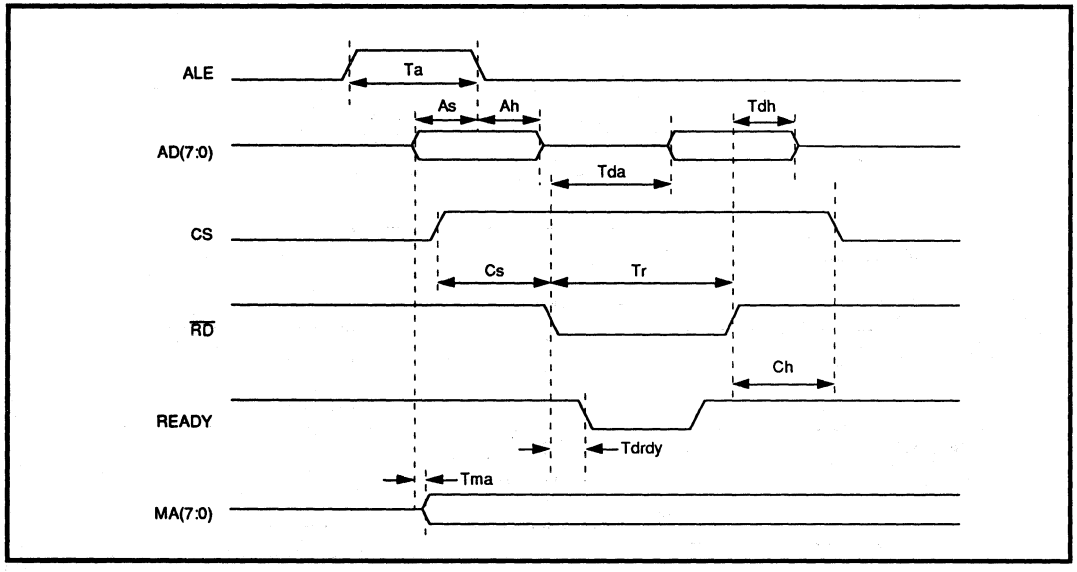


FIGURE 2: Intel Register Multiplexed Read Timing

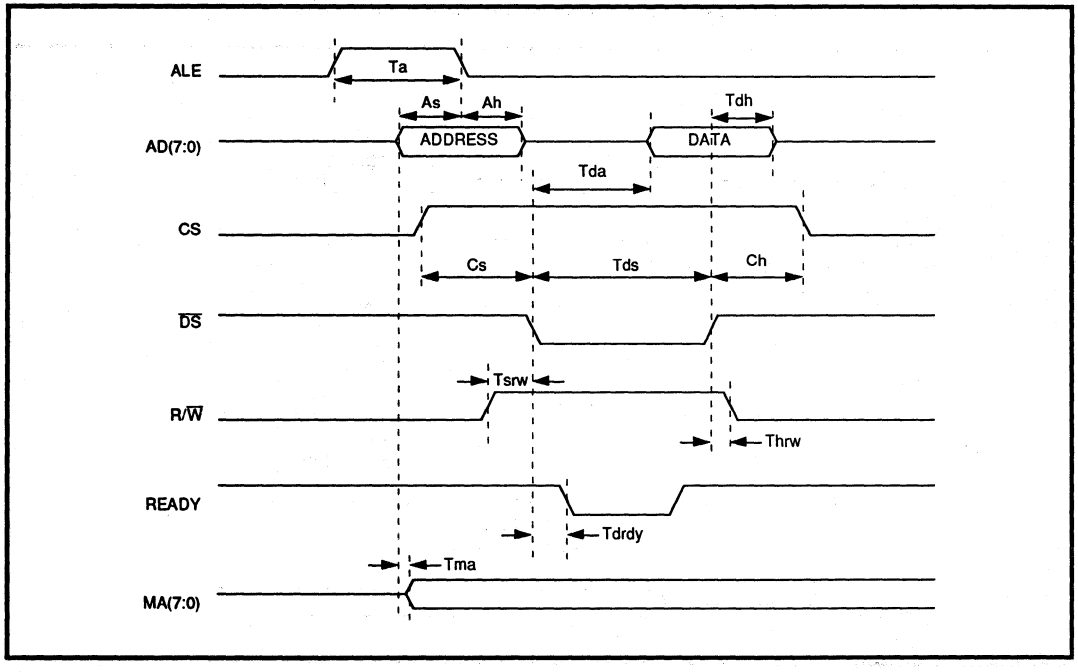


FIGURE 3: Motorola Register Multiplexed Read Timing

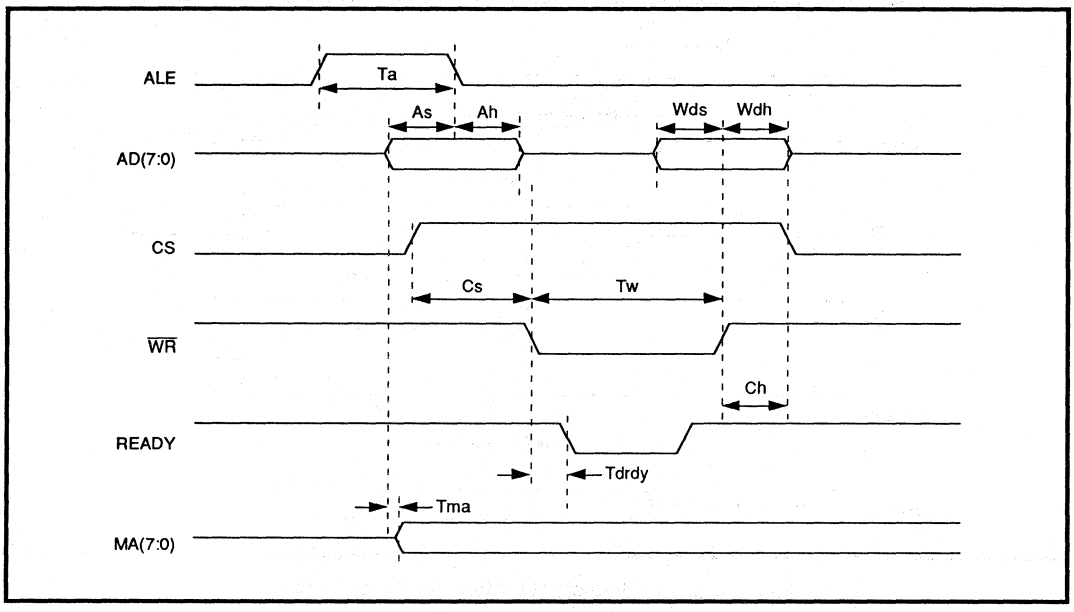


FIGURE 4: Intel Register Multiplexed Write Timing

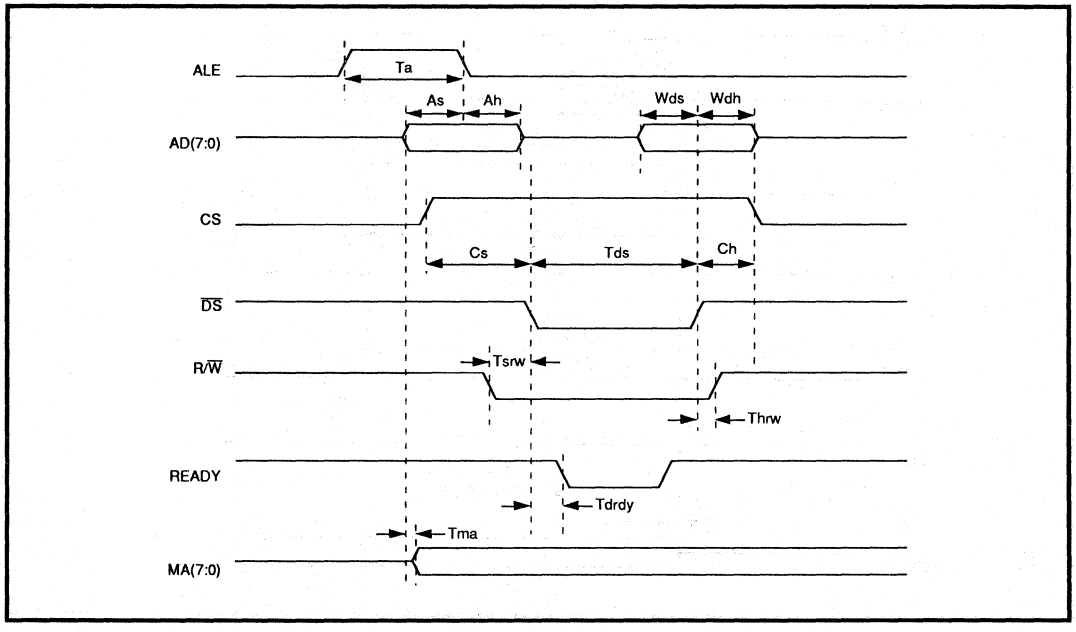


FIGURE 5: Motorola Register Multiplexed Write Timing

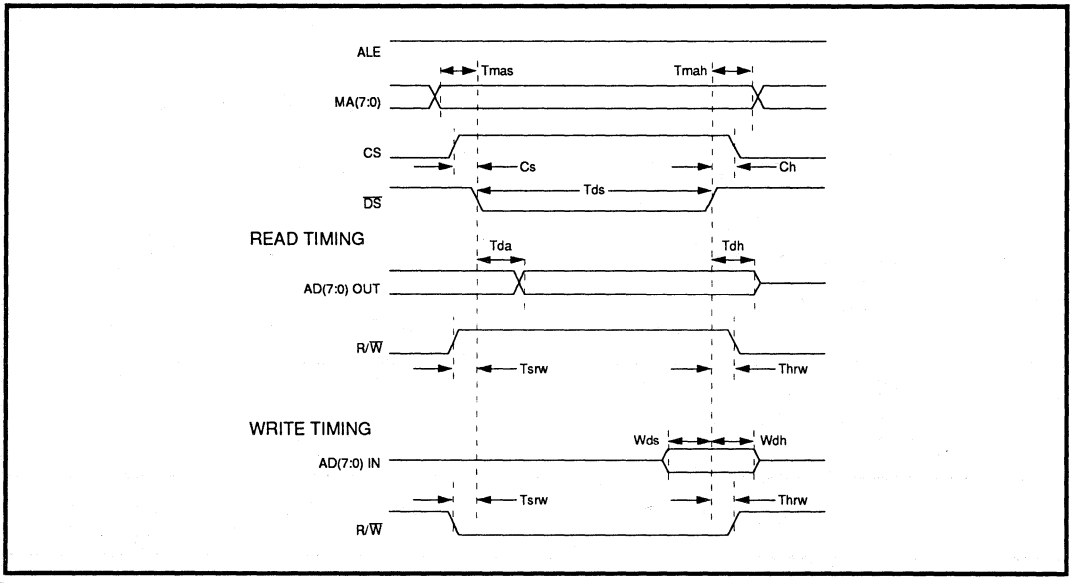


FIGURE 6: Non-Multiplexed Bus Timing Diagrams

ELECTRICAL SPECIFICATIONS (continued)

MICROPROCESSOR INTERFACE TIMING PARAMETERS

Disk Read/Write Timing (Figure 7)

PARAMETER		CONDITIONS	MIN 3.3V	MAX 3.3V	MIN 5V	MAX 5V	UNIT
T	RRCLK period (dual bit)		41		41		ns
	RRCLK period (single bit)		31		20.8		ns
T/2	RRCLK low time (dual bit)		16		16		ns
	RRCLK low time (single bit)		12		8.5		ns
Ds	NRZ in valid to RRCLK high		5		3		ns
Dh	RRCLK high to NRZ in invalid		5		3		ns
As	$\overline{AMD}$ valid to RRCLK high (soft sector only)		5		3		ns
Dv	RRCLK high to NRZ1, NRZ0 out valid		5	27	3	18	ns
Tr, Tt	RRCLK rise and fall time			3		2	ns
Note:	Loading capacitance = 10 pF						

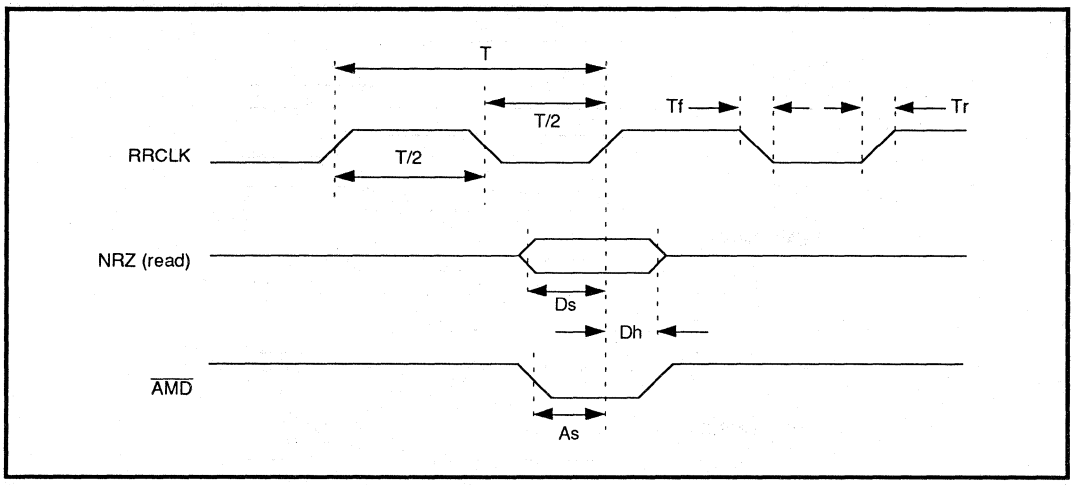


FIGURE 7: Disk Read Timing

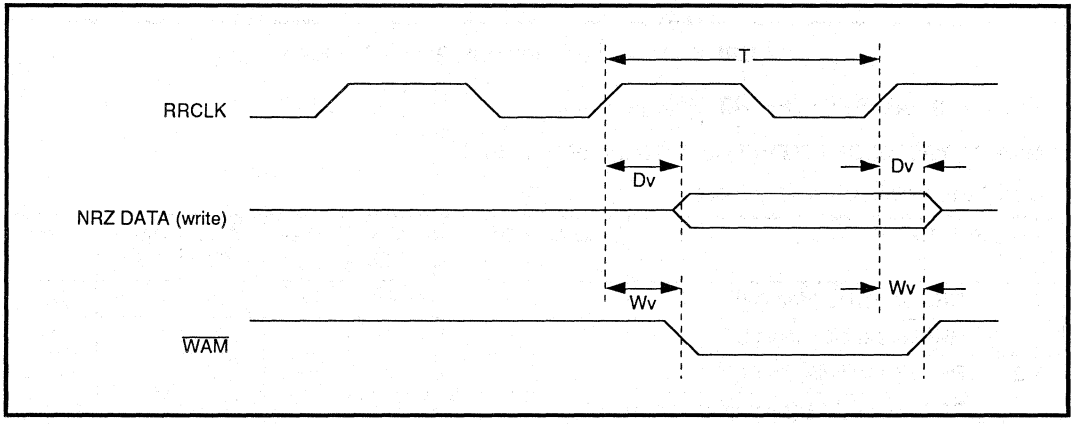


FIGURE 8: Disk Write Timing

BUFFER MEMORY READ/WRITE TIMING PARAMETERS (Figures 8 through 13)

PARAMETER		CONDITIONS	MIN 3.3V	MAX 3.3V	MIN 5V	MAX 5V	UNIT
T	SYSCLK period		28		25		ns
T/2	SYSCLK high/low time		12		10		ns
Tav	SYSCLK ↑ to address valid	(Note 1)		35		18	ns
Tmsv	SYSCLK ↑ to $\overline{MS}$↓	(Notes 1, 6)		35		18	ns
Tmsh	SYSCLK ↑ to $\overline{MS}$↑	(Note 1)		35		18	ns
Tmv	SYSCLK ↑ to $\overline{MOE}$↓	(Note 1)		35		18	ns
Tmh	SYSCLK ↑ to $\overline{MOE}$↑	(Note 1)		35		18	ns
Twv	SYSCLK ↑ to $\overline{WE}$↓	(Note 1)		35		18	ns
Twh	SYSCLK ↑ to $\overline{WE}$↑	(Note 1)		35		18	ns
Tdov	SYSCLK ↑ to data out valid	(Note 1)		35		18	ns
Tdoh	SYSCLK ↑ to data out invalid	(Note 1)		35		18	ns
Tdis	Data in valid to $\overline{MOE}$↑ (SRAM) Data in valid to $\overline{CAS}$↑ (DRAM)		5		5		ns
Tdih	$\overline{MOE}$↑ to data in valid (SRAM) $\overline{CAS}$↑ to data in valid (DRAM)		0		0		ns
Trv	SYSCLK ↑ to $\overline{RAS}$↓	(Note 1)		35		18	ns
Trh	SYSCLK ↑ to $\overline{RAS}$↑	(Note 1)		35		18	ns
Trav	SYSCLK ↑ to row address valid	(Note 1)		35		18	ns
Trah	SYSCLK ↑ to row address invalid	(Note 1)		35		18	ns
Tcv	SYSCLK ↑ to $\overline{CAS}$↓	(Note 1)		35		18	ns
Tch	SYSCLK ↑ to $\overline{CAS}$↑	(Note 1)		35		18	ns
Tcav	SYSCLK ↑ to column address valid	(Note 1)		35		18	ns
Tcah	SYSCLK ↑ to column address invalid		0		0		ns

ELECTRICAL SPECIFICATIONS (continued)

BUFFER MEMORY READ/WRITE FUNCTIONAL PARAMETERS (Figures 9 through 12) (continued)

PARAMETER		CONDITIONS	MIN	UNIT
Trwl	$\overline{RAS}\uparrow$ to $\overline{RAS}\downarrow$	Notes 2, 3	(RWL + 3)•T	ns
Trwh	$\overline{RAS}\downarrow$ to $\overline{RAS}\uparrow$	Notes 2, 4	(RWH + 1)•T	ns
Tcwl	$\overline{CAS}\uparrow$ to $\overline{CAS}\downarrow$	Note 2	(CWL + 1)•T	ns
Tcwl	$\overline{CAS}\downarrow$ to $\overline{CAS}\uparrow$	Notes 2, 5	(CWL + 1)•T	ns

Note: Loading capacitance = 30 pF

Note 1: The measured delay for any of the signal indicated by this note will not vary from the measured delay of any other signal indicated by this note by more than TBD (3V), ±2 ns (5V).

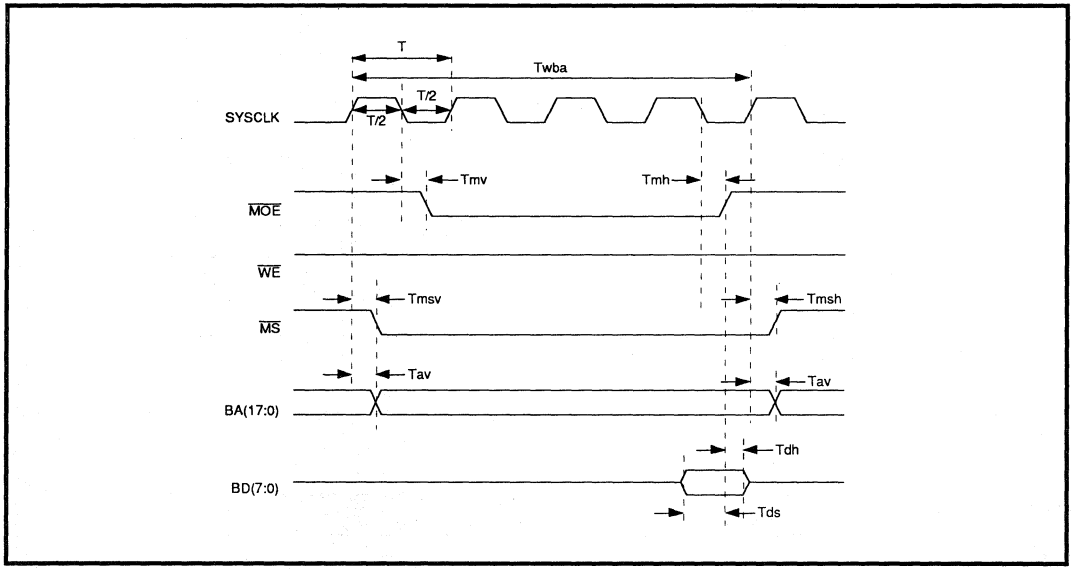
Note 2: RWL, RWH, CWL and CWH are fields in the Buffer Manager Timing Control Register (54H). Each is a two bit field which can contain a value of 0, 1, 2, or 3. These values determine the minimum number of SYSCLK periods (T) for the associated signal width.

Note 3: The minimum width value of Trwl will be generated for refresh cycles and for any buffer memory access cycle except when multiple page mode accesses are performed. When multiple page mode accesses are performed, the width of the $\overline{RAS}$ low pulse is extended until the end of the last $\overline{CAS}$ low cycle.

Note 4: The minumum value of Trwh will be generated whenever the Buffer Manager determines that a buffer request is pending at the completion of the current memory cycle and a page mode access can not be used either because page mode operation is not enabled or the needed location is not within the current page.

Note 5: The minumum value of Tcwh will be generated only between consecutive page mode accesses.

Note 6: $\overline{MS}$ will rise only if the Buffer Manager determines that no additional requests for buffer access are pending. If the Buffer Manager determines that another access is to be made, $\overline{MS}$ is kept low between the accesses for improved speed.



Note: Twba is a functional parameter that gives the duration of one RAM data buffer access cycle in SYSCLK periods. The value is programmed in bits 1-0 of register 54H. These examples show Twba = 4T.

FIGURE 9: SRAM Read Timing

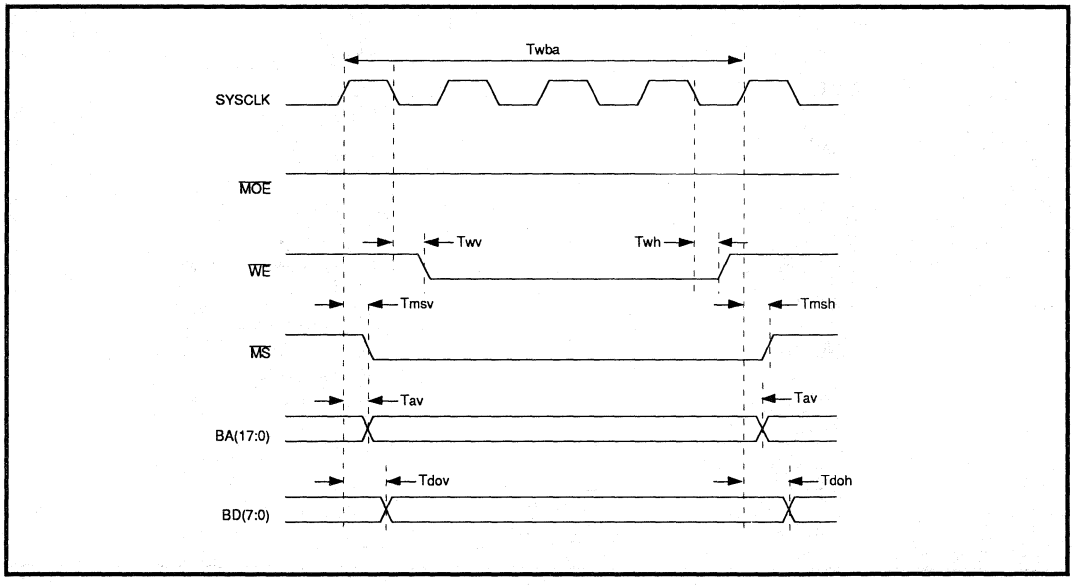


FIGURE 10: SRAM Write Timing

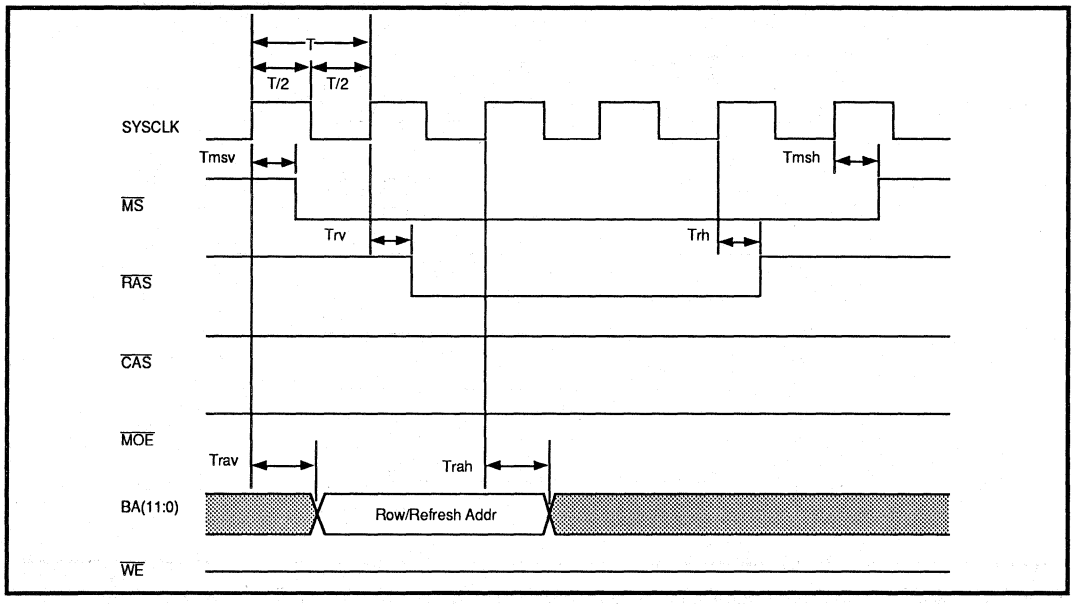


FIGURE 11: DRAM Timing, Refresh Cycle (shown with WRL = 0)

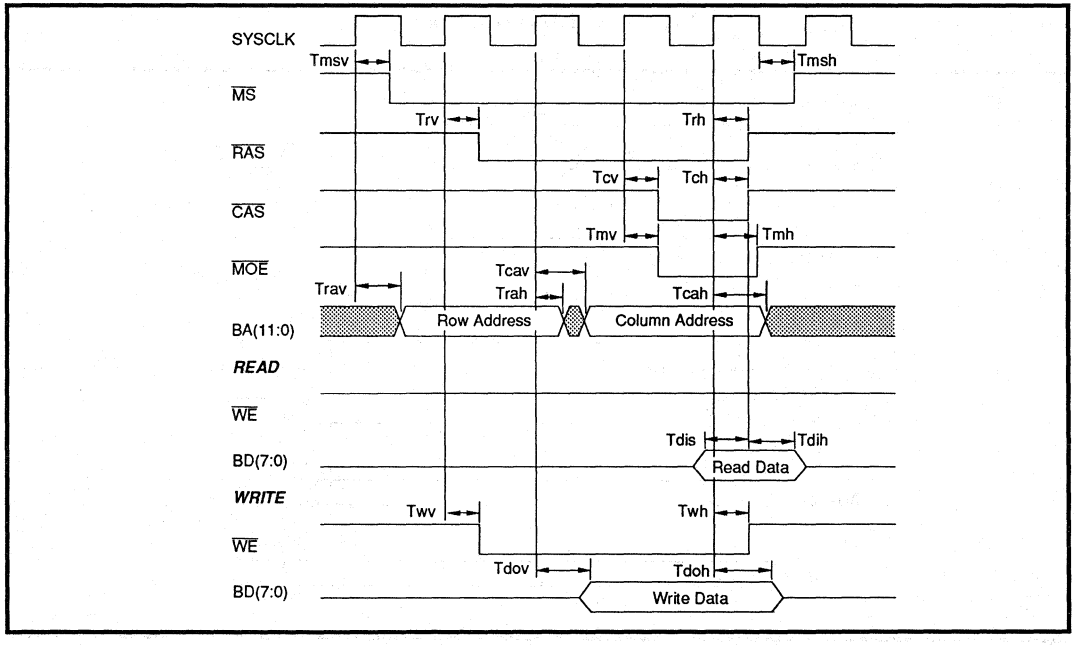


FIGURE 12: DRAM Timing, Standard Cycle (shown with RWL = 0 and CWL = 0)

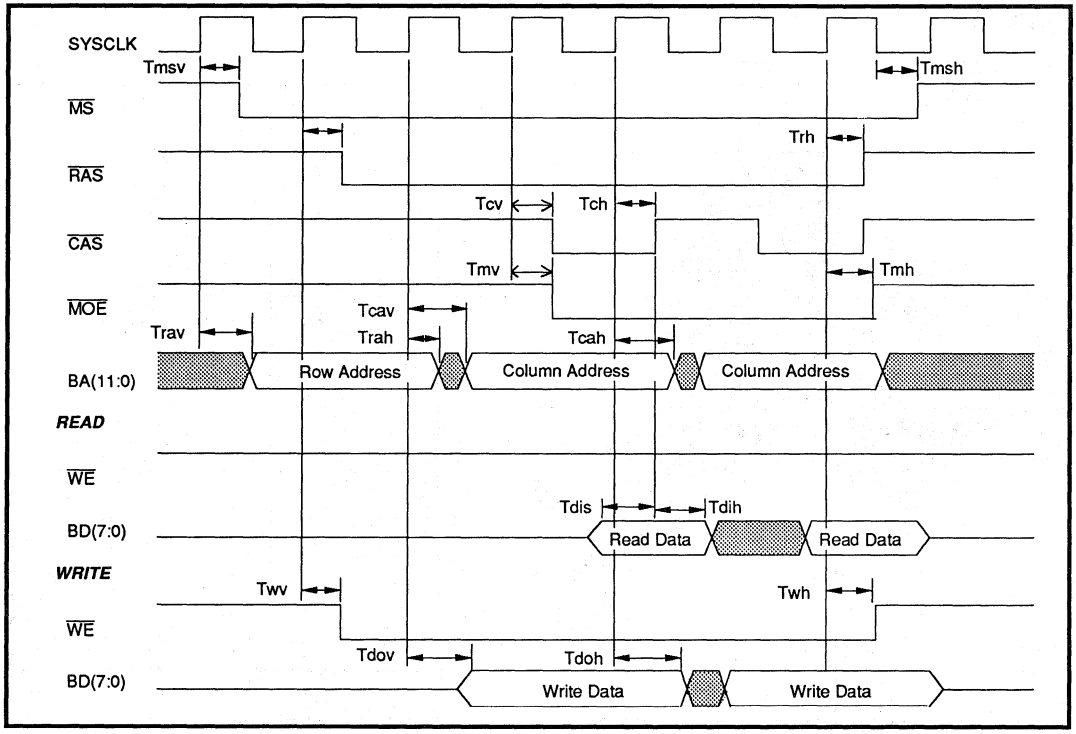


FIGURE 13: DRAM Timing, Fast Page Cycles (shown with RWL = 0, RWH = 0, CWL = 0 and CWH = 0)

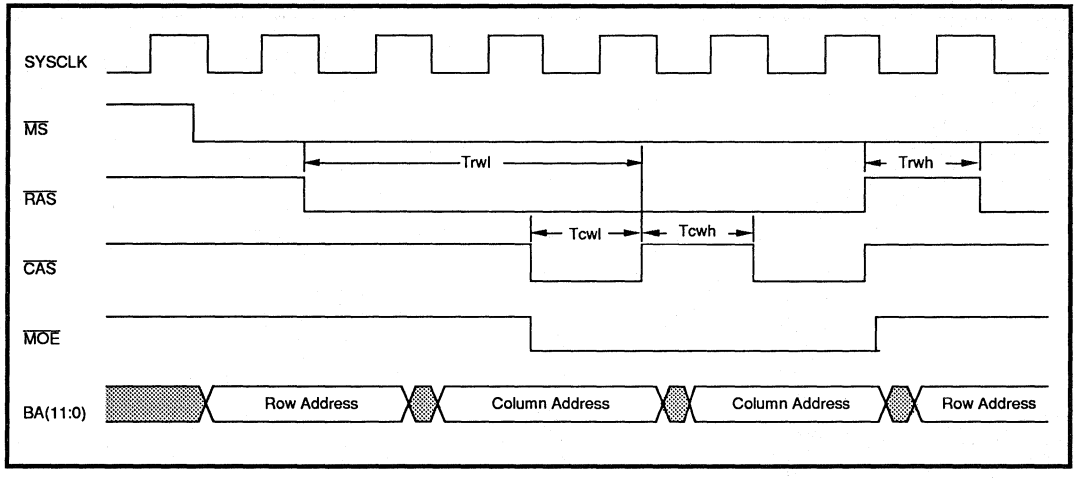


FIGURE 14: DRAM Timing (showing the relationship of RWL, RWH, CWL and CWH to overall timing)

ELECTRICAL SPECIFICATIONS (continued)

AT Host Interface Timing Parameters

PARAMETER		MIN 3.3V	MAX 3.3V	MIN 5V	MAX 5V	UNIT
DREQL	$\overline{DACK}$ ↓ to DREQ ↓		50		40	ns
RDTA	$\overline{IOR}$ ↓ to HD(15:0) valid		70		50	ns
DMASET	$\overline{DACK}$ ↓ to $\overline{IOW}$ ↓ or $\overline{IOR}$ ↓	0		0		ns
DMAHLD	$\overline{IOR}$ ↑ or $\overline{IOW}$ ↑ to $\overline{DACK}$ ↑	0		0		ns
RDHLD	$\overline{IOR}$ ↑ to HD (15:0) hi-Z	2	25	2	25	ns
WDS	HD(15:0) setup to $\overline{IOW}$ ↑	40		30		ns
WDHLD	HD(15:0) hold from $\overline{IOW}$ ↑	10		10		ns
RWPULSE	$\overline{IOR}$ or $\overline{IOW}$ low pulse width	80		80		ns
RWH	$\overline{IOR}$ or $\overline{IOW}$ high pulse width	50		50		ns
CS16L	$\overline{HCS0}$ ↓, A(2:0) ↓, A9 ↓ or $\overline{HCS1}$ ↑ to $\overline{IOCS16}$ ↓		30		25	ns
IOCHL	$\overline{IOR}$ ↓ or $\overline{IOW}$ ↓ to $\overline{IOCHRDY}$ ↓		35		30	ns
ADRSET	$\overline{HCS0}$, A(2:0), A9/$\overline{HCS1}$ setup to $\overline{IOR}$ ↓ or $\overline{IOW}$ ↓	25		25		ns
ADRHLD	$\overline{HCS0}$, A(2:0), A9/$\overline{HCS1}$ hold from $\overline{IOR}$ ↑ or $\overline{IOW}$ ↑	10		5		ns
Note: Loading capacitance = 30 pF						

Functional Specification

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
IOCHTW	$\overline{IOCHRDY}$ pulse width		0		5xBCLK	ns

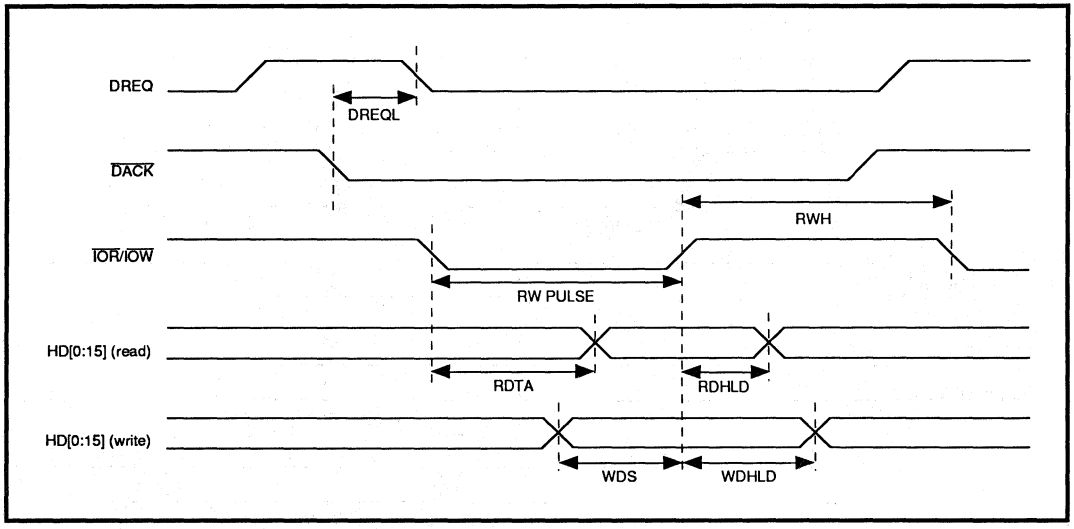


FIGURE 15: Host Programmed I/O 8-16 Bit Timing

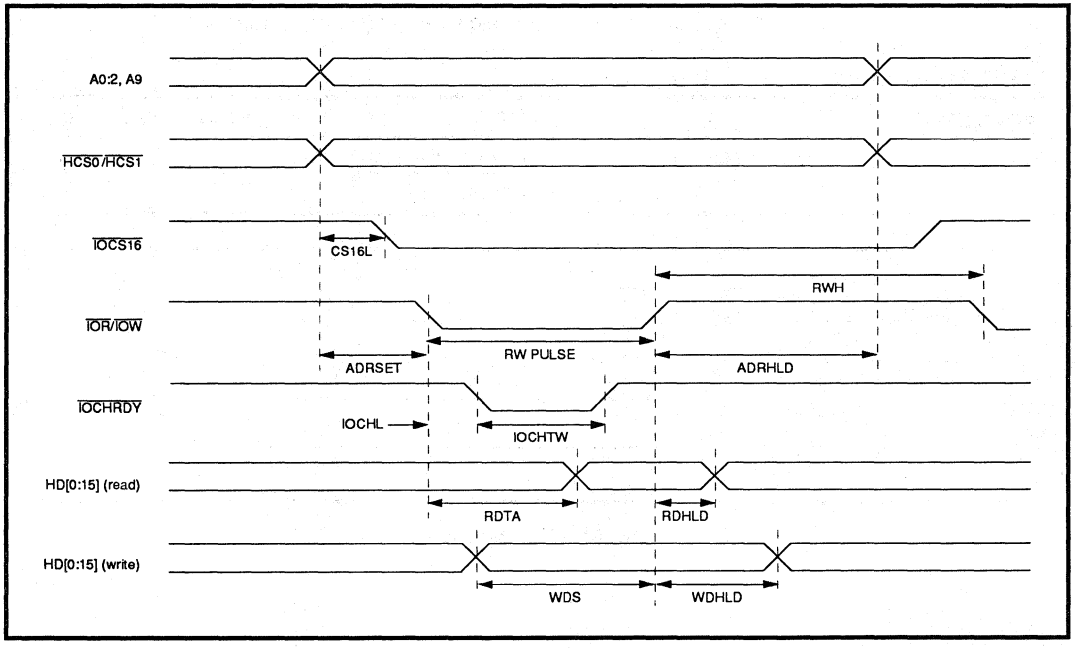


FIGURE 16: Host DMA 8-16 Bit Interface Timing (Non-demand mode)

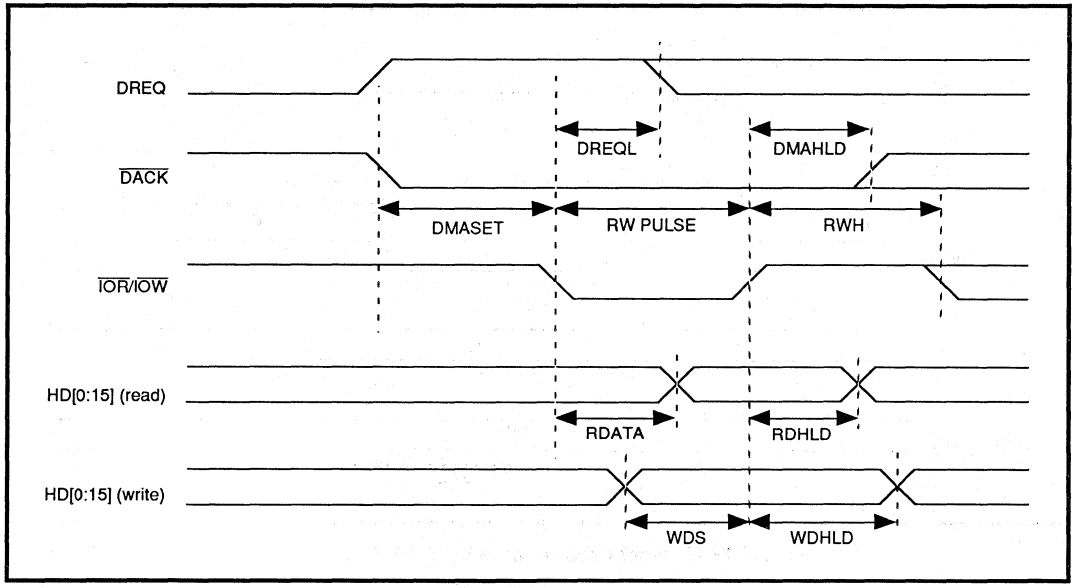


FIGURE 17: Host DMA 8/16-Bit Interface Timing (Demand Mode)

RESET Assertion Timing Parameters (Figure 18)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Trpwl	$\overline{RST}$ pulse width low	NOT Power On Reset	500			ns
		Power On Reset	7.5			µs

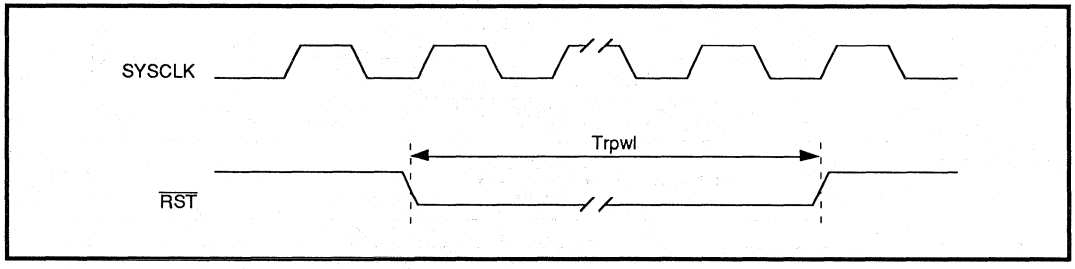
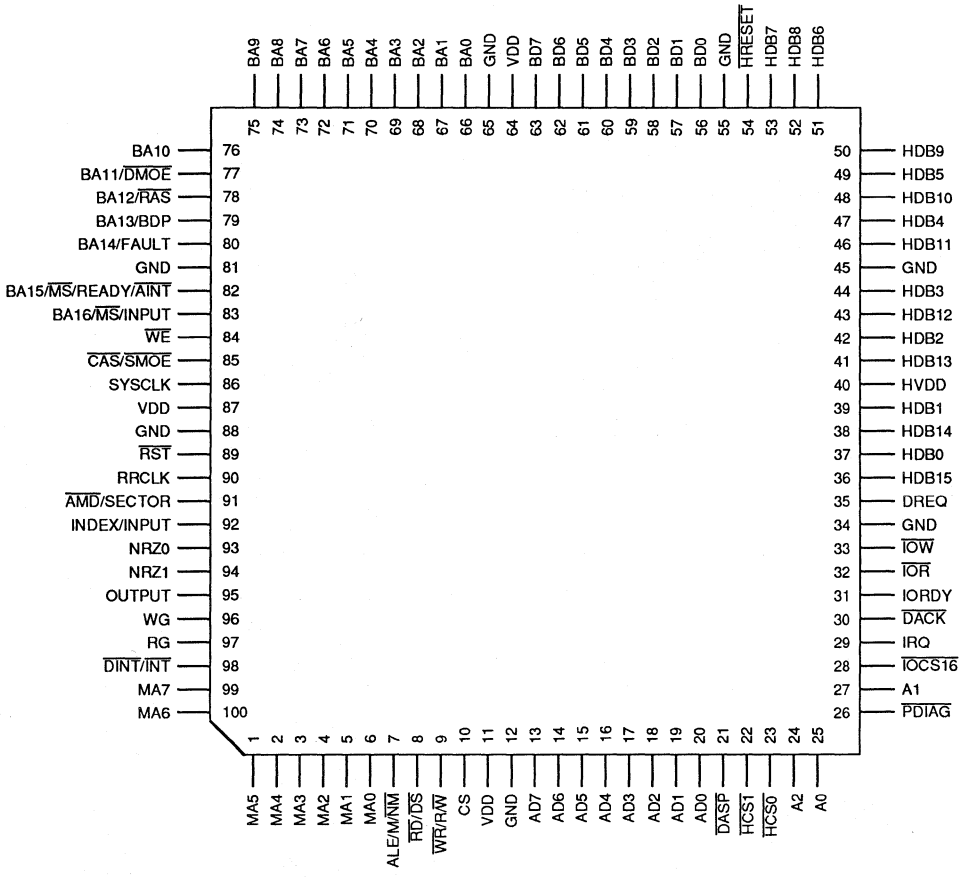


FIGURE 18: RESET Assertion Timing

PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



100-Lead TQFP

9

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX: (714) 573-6914

Notes:

silicon systems®
A TDK Group Company

SSI 32C9302
PC-AT Combo Controller With Reed Solomon, 3.3V Operation

Advance Information

December 1993

DESCRIPTION

The SSI 32C9302 is an advanced CMOS VLSI device which integrates major portions of the hardware needed to build an ATA disk drive. The SSI 32C9302 can operate on 3.3V or 5V allowing use in 3.3V, 5V, or dual voltage disk drives. The 32C9302 has a dual bit NRZ interface to allow interfacing with channel ICs supporting this interface. The 32C9302 also supports serial NRZ mode to allow interfacing with ICs supporting this interface. The circuitry of the SSI 32C9302 includes a complete ATA interface, an advanced buffer manager, a high performance disk formatter and an 88-bit Reed-Solomon ECC with fast "on-the-fly" hardware correction. The SSI 32C9302 provides maximum performance while minimizing micro controller intervention.

When operating in a 3.3V environment, the SSI 32C9302 is capable of concurrent transfers of up

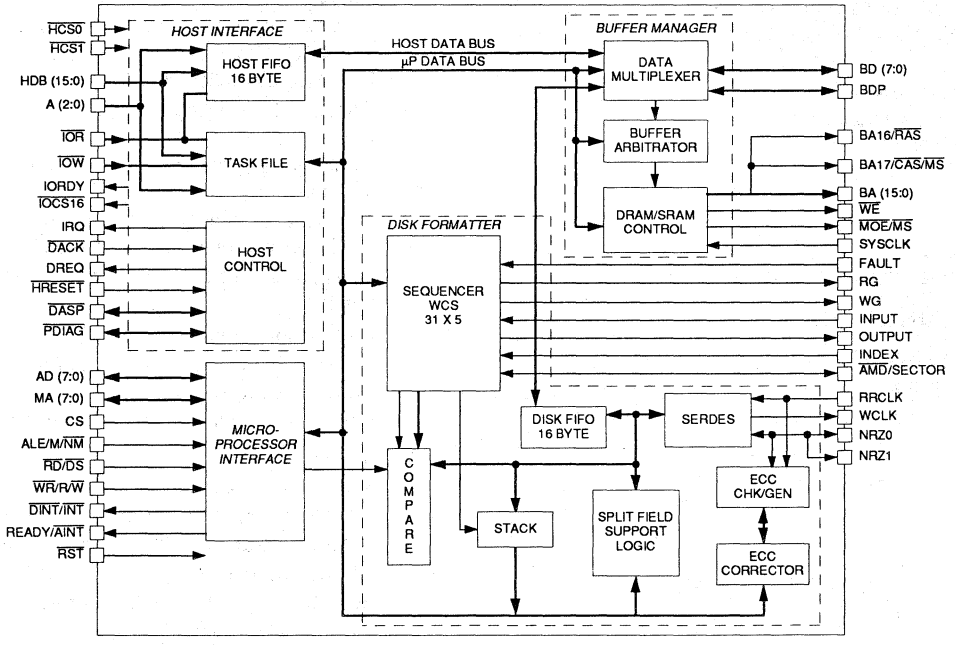
(continued)

FEATURES

- **ATA Interface**
  - **Single Chip PC AT Controller**
  - **Full ANSI ATA Compliance**
  - **Direct PC Bus connection with on board 16 mA (24 mA @ 5V) drivers**
  - **PC transfers to 4 (6.7 @ 5V) megawords per second**
  - **Supports PIO, DMA and Multiword DMA (EISA Class B Demand DMA)**
  - **Logic for daisy chaining 2 drives**
  - **Operates as Master, Slave or both**
  - **Automatic command decoding of Write, Write Long, Write DMA, Write Multiple, Write Buffer and Format commands**
  - **Hardware Support for Write Multiple and Read Multiple Commands**

(continued)

BLOCK DIAGRAM



SSI 32C9302
PC-AT Combo Controller
With Reed Solomon, 3.3V Operation

DESCRIPTION (continued)

to 48 Mbit/s on the disk interface and 4 megawords (16-bit transfers) per second across the ATA bus.

In a 5V environment, the SSI 32C9302 is capable of concurrent transfers of up to 48 Mbit/s on the disk interface and 6.7 megawords per second across the ATA bus. In addition, on-the-fly error corrections and micro controller accesses to the buffer memory will not degrade the throughput during transfers.

The SSI 32C9302 is one of a family of Silicon Systems' single chip disk controllers which support ATA, SCSI and PCMCIA device interfaces. The 32C9301 is another 3.3/5V dual voltage ATA controller and is contained in a 100-lead TQFP, but does not support all of the features of the SSI 32C9302. The SSI 32C9001 is a 5V only version of the SSI 32C9301 which is 100% firmware and pinout compatible. The SSI 32C9003 is firmware and pinout compatible with the SSI 32C9302, but is a 5V only part with disk data rates to 80 Mbit/s. The SSI 32C9020, SSI 32C9022 and SSI 32C9023 family members are SCSI disk controllers. The SSI 32C9340 disk controller completes the family providing a PCMCIA/ATA compliant interface. The SSI 32C9340 controller operates in either a 3.3V or 5.0V environment. All members are based on a common architecture allowing major portions of firmware to be reused. The Silicon Systems' chip family is illustrated in hierarchy chart shown in Figure 1.

The high level of integration within the SSI 32C9302 represents a major reduction in parts count. When the SSI 32C9302 ATA Controller is combined with the SSI 32R2300 Read/Write device, the SSI 32P4342 Pulse Detector with 1,7 ENDEC, the 32H6300 Servo and Motor Speed Controller, an appropriate micro controller and memory a complete, cost efficient, high performance intelligent drive solution is created.

FEATURES (continued)

- ATA Interface (continued)
  - Automatic updates of the host task file registers in both Cyl/Hd/Sec and LBA modes
  - Automatic Multi-Sector data transfers without microprocessor intervention
  - Automatic Host Interrupt and Busy for multiple sector transfers integrated with buffer streaming logic
  - 16-byte FIFO to improve performance
  - Separate host interface VDD to allow 3.3V drives to plug into 5V systems
  - Power management, including power down of I/O pins
- Buffer Manager
  - Direct support of DRAM or SRAM
    - SRAM: up to 256k bytes of memory with throughput to 14 (20 @ 5V) MB/s
    - DRAM: up to 1 megabyte of memory with throughput to 12 (17.78 @ 5V) MB/s
  - Programmable memory timing
  - Buffer RAM segmentation with flexible segment sizes from 256 bytes to 1 megabyte
  - Dedicated host, disk and microprocessor address pointers
  - Buffer Streaming with internal buffer protection circuit providing buffer integrity
- Disk Formatter
  - Dual Bit NRZ interface supporting data rates to 48 Mbit/s
  - Single Bit NRZ supporting data transfer rates to 32 Mbit/s (48 @ 5V)
  - Automatic multi-sector transfer
  - Header or microprocessor based split data field support
  - Advanced sequencer organized in 31 x 5 bytes
  - 88-bit Reed Solomon ECC with "on-the-fly" fast hardware correction circuitry
  - Capable of correcting up to four 10-bit symbols in error
  - Guaranteed to correct one 31-bit burst or two 11-bit bursts
  - Hardware on-the-fly correction of an 11-bit single burst error within a half sector time
  - Detects up to one 51-bit burst or three 11-bit bursts
- Microprocessor Interface
  - Supports both multiplexed or non-multiplexed microprocessors
  - Separate or combined host and disk interrupts
- Other Features
  - Internal power down modes
  - Automatic power supply level detection
  - Conforms to JEDEC 3.3V specifications
  - TTL compatible input receivers at 3.3V or 5V
  - Available in 120-lead TQFP, 128-Lead QFP, and 128-Lead TQFP packages

FUNCTIONAL DESCRIPTION

The SSI 32C9302 contains the following four major functional blocks:

Microprocessor Interface
ATA Interface
Disk Formatter
Buffer Manager

The Microprocessor Interface allows the local microprocessor access to all of the SSI 32C9302 internal control registers and any location within the buffer memory. The microprocessor, by writing and reading the internal registers, can control all activities of the SSI 32C9302. The microprocessor can elect to perform host and/or disk operations directly, or it can enable the advanced features of the SSI 32C9302 which can perform these operations automatically.

The ATA Interface block handles all PC AT bus activities. The ATA interface includes 16 mA (24 mA @ 5V) drivers allowing for direct connection of the SSI 32C9302 to the PC AT bus. The ATA interface block is highly automated, capable of performing multiple block transfers without micro controller involvement. The ATA block interfaces directly with the Buffer Manager via an internal speed matching FIFO. This FIFO, the bandwidth capabilities of the Buffer Manager, plus the advanced features of the ATA Interface guarantee sustained full speed transfers across the PC AT bus.

The Disk Formatter performs the serialization and deserialization of data. If provides all of the necessary functions to control track formatting, header search, and the reading and writing of data. The heart of the Disk Formatter is an advanced programmable sequencer. The sequencer can contain 31 instructions, each of which is 5 bytes (40 bits) in width. The width of the instructions allows for sophisticated branching techniques which increases the flexibility and power of the sequencer. The disk interface can be configured through a wide range of capabilities. This allows the SSI 32C9302 to interface with nearly any read/write channel and allows the user of the SSI 32C9302 to select the read/write channel best suited to the device. Of course, by selecting the SSI 32C9302 controller and the SSI 32P4342 Read Channel with 1,7 ENDEC, you are guaranteed a problem free interface.

Within the Disk Formatter are the ECC generator/checker and ECC corrector. The generator/checker provides the ability to generate or check a 16-bit CRC for headers and an 88-bit Reed Solomon code for data. If the checker detects an error using the 88-bit Reed Solomon code, the syndrome information is transferred into the corrector. The corrector then performs the necessary operations to determine if the error was

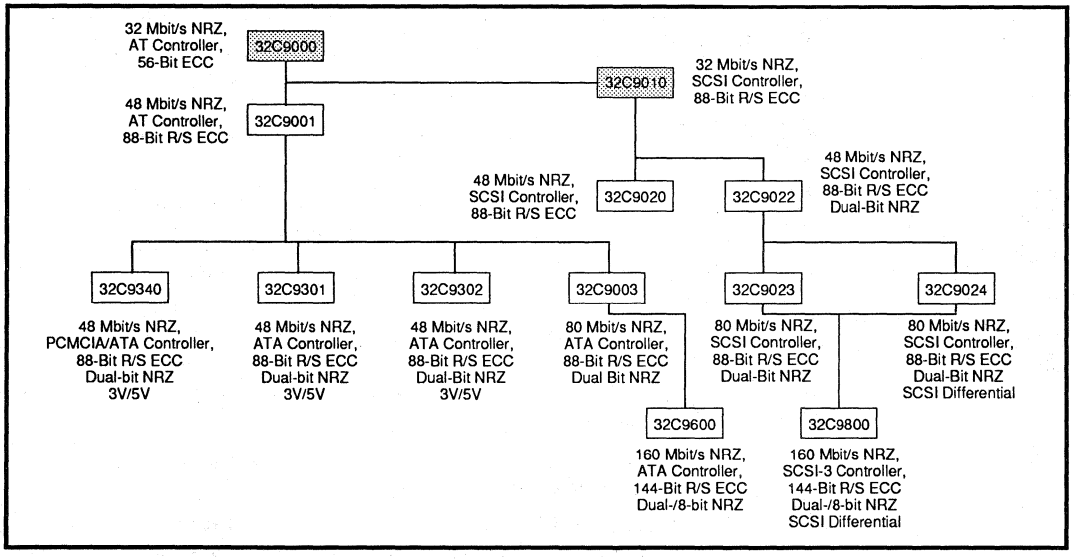


FIGURE 1: Silicon Systems' Disk Controller Chip Hierarchy

FUNCTIONAL DESCRIPTION (continued)

correctable and, if it was correctable, the corrector interfaces directly with the buffer controller and performs the correction automatically. The corrector performs its correction within one half of a sector. This guarantees that the corrector will always be available to correct the next sector if necessary.

The Buffer Manager manages the data buffer of the controller. The Buffer Manager can support either SRAM or DRAM. When configured to operate with DRAM, the Buffer Manager automatically performs necessary refresh cycles. The Buffer Manager creates all of the necessary timing and control signals for a wide range of memory types and speeds. Besides interfacing with the buffer memory, the Buffer Manager interfaces with the ATA Interface block, the Disk Formatter block, the ECC corrector and the microprocessor. If more than one of these devices requires access to the buffer memory, the Buffer Manager arbitrates the requests automatically. The Buffer Manager of the SSI 32C9302 can sustain ATA operations at the rate of 4 (6.7 @ 5V) megawords per second, Disk Formatter operations at 48 Mbit/s and still has sufficient band width left to handle on-the-fly ECC corrections and microprocessor accesses without degrading performance on any of the interfaces.

PIN DESCRIPTION

The following convention is used in the pin description:

- (I) denotes an input
- (O) denotes an output
- (I/O) denotes a bidirectional signal
- (Z) denotes a tri-state output
- (OD) denotes an open drain output

Active low signals are denoted by a bar on top of the signal name and dual function pins are denoted with a slash between the two signals — $\overline{\text{AMD}}$/SECTOR.

GENERAL

NAME	TYPE	DESCRIPTION
VDD		POWER SUPPLY PIN
GND		GROUND

HOST INTERFACE

A(2:0)	I	HOST ADDRESS LINES. The Host Address lines A(2:0) are used to access the various PC/AT control/status, and data registers.
$\overline{\text{HCS1}}$	I	HOST CHIP SELECT 1. This pin selects access to the control block task file registers.
$\overline{\text{HCS0}}$	I	HOST CHIP SELECT 0. This pin selects access to the command block task file registers.
$\overline{\text{IOCS16}}$	OD	16-BIT DATA TRANSFER. An open drain active low output that indicates that a 16-bit buffer transfer is active.
IRQ	O,Z	HOST INTERRUPT. Asserted active high to indicate to the Host that the controller needs attention.
IORDY	O,Z	I/O CHANNEL READY. This signal is asserted low to extend host transfer cycles when the controller is not ready to respond. This pin will be tristated when a read or write is not in progress.

HOST INTERFACE (continued)

NAME	TYPE	DESCRIPTION
DREQ	O,Z	DMA REQUEST. The active high DMA Request signal is used during DMA transfer between the Host and the controller.
$\overline{\text{DACK}}$	I	DMA ACKNOWLEDGE. This active low signal is used during DMA to complete the DMA handshake for data transfer between the host and the controller.
$\overline{\text{IOR}}$	I	I/O READ. This active low pin is asserted by the Host during a Host read operation. When asserted with $\overline{\text{HCS0}}$, $\overline{\text{HCS1}}$, or $\overline{\text{DACK}}$, data from the device is enabled onto the host data bus.
$\overline{\text{IOW}}$	I	I/O WRITE. Asserted active low by the HOST during a HOST write operation. When asserted with $\overline{\text{HCS0}}$, $\overline{\text{HCS1}}$, or $\overline{\text{DACK}}$, data from the host data bus is strobed into the device.
$\overline{\text{HRESET}}$	I	HOST RESET. This active low signal stops all commands in progress and initializes the control/status registers — This signal can also "wake up" the device while it is in power down mode.
HDB(15:0)	I/O	HOST DATA BUS. These bits are used for word transfers between the Buffer Memory and the Host; bits (7:0) are used for status, commands, or ECC byte transfers.
$\overline{\text{DASP}}$	I,OD	DRIVE ACTIVE/DRIVE 1 PRESENT. This is a time-multiplexed signal which indicates that a drive is active, or that Drive 1 is present.
$\overline{\text{PDIAG}}$	I,OD	PASSED DIAGNOSTICS. This signal is an output when configured as Drive 1 and an input when configured as Drive 0.

DISK INTERFACE

INDEX	I	INDEX. This input is a pulse that occurs once per revolution and defines the start of first sector.
OUTPUT	O	DISK SEQUENCER OUTPUT. This pin is controlled by bit 2 of the control field of the disk sequencer.
INPUT	I	INPUT. This signal is used to synchronize the disk sequencer to an external event.
$\overline{\text{AMD}}$/ SECTOR	I	ADDRESS MARK DETECT/SECTOR. This pin is configured to operate in Hard or Soft Sector mode by initializing the Disk Formatter Mode Control Register: 4FH, bit 1. In the hard sector mode it is used as the sector input — a pulse on this pin indicates a sector mark is found. In the soft sector mode, an active low input indicates an address mark was detected. The device powers up in soft sector mode.
RG	O	READ GATE. This active high output enables the reading of the disk. It is asserted at the beginning of the PLO for header and data field by the sequencer — sequencer Control Field bits 5 and 6. It is automatically deasserted at the end of the CRC or ECC.

PIN DESCRIPTION (continued)

DISK INTERFACE

NAME	TYPE	DESCRIPTION
WG	O	WRITE GATE. This active high output enables writing onto the disk. It is asserted and deasserted by the sequencer Control Field bits 5 and 6.
RRCLK	I	READ REFERENCE CLOCK. This pin is used in conjunction with the NRZs pin to clock data in. It is also used as a clock for the disk sequencer and is used to generate WCLK.
WCLK	O	WRITECLOCK. This signal clocks the NRZ data out.
NRZ0, 1	I/O	NON RETURN TO ZERO. These signals are the read data input 0 and 1 from the disk drive when the read gate signal is asserted; it is the write data output to the disk drive when the write gate signal is asserted. NRZ1 is the most significant bit.
FAULT	I	Fault: Asserting this pin causes the disk sequencer to stop immediately.

MICROPROCESSOR INTERFACE

$\overline{RST}$	I	RESET. An asserted active low input generates a component reset that holds the internal registers of the controller at reset, stops all operations within the chip, and deasserts all output signals. All input/output signals and Host outputs are set to the high-Z state.
ALE	I	ADDRESS LATCH ENABLE/Multiplexed or Non-multiplexed address select: If this input is constantly low, the microprocessor interface is configured with non-multiplexed address and data busses. If this input is ever high, the microprocessor interface is configured with a multiplexed address and data bus. In this case, this pin functions as the address latch enable, and the latched address is output on the MA(7:0) pins.
CS	I	CHIP SELECT. This signal must be asserted high for all microprocessor accesses to the registers of this chip.
$\overline{WR}$/R/$\overline{W}$	I	WRITE STROBE/READ/WRITE. When the Intel bus control interface is selected, this signal acts as the $\overline{WR}$ signal. When the Write strobe signal is asserted low and the CS signal is asserted high, the data on the AD lines will be written to the register. When the Motorola bus control interface is selected, this signal acts as the R/$\overline{W}$ signal. A high on this input along with the $\overline{RD}$/$\overline{DS}$ signal asserted and the CS signal asserted high indicates a read operation. A low on this input along with the $\overline{RD}$/$\overline{DS}$ signal asserted and the CS signal asserted high indicates a write operation.

MICROPROCESSOR INTERFACE (continued)

NAME	TYPE	DESCRIPTION
$\overline{RD}/\overline{DS}$	I	READ STROBE/DATA STROBE. When the Intel bus control interface is selected, this signal acts as the $\overline{RD}$ signal. When the read strobe signal is asserted low and the CS signal is asserted high, the data from the specified register will be driven onto the AD signals. When the Motorola bus control interface is selected, this signal acts as the $\overline{DS}$ signal. A high on the R/$\overline{W}$ signal along with this signal asserted and the CS signal asserted high indicates a read operation. A low on the R/$\overline{W}$ signal along with this signal asserted and the CS signal asserted high indicates a write operation.
$\overline{DINT}/\overline{INT}$	O, OD	DISK INTERRUPT. This signal is an interrupt line to the microprocessor. It is the combined interrupt line of the disk side and host side interrupts when pin READY/$\overline{AINT}$ is programmed as Ready; otherwise, it only signals the occurrence of disk side interrupt events. This signal is programmable for either a push-pull or open-drain output circuit. This signal powers up in the high-Z state.
AD(7:0)	I/O	ADDRESS/DATA BUS. When configured in the Multiplexed mode, these lines are multiplexed, bidirectional data path to the microprocessor. During the beginning of the memory cycle the bus captures the low order byte of the microprocessor address. These lines provide communication with the controller device's internal registers and the buffer memory. When configured in the Non-multiplexed mode, these lines are bidirectional data lines.
MA(7:0)	I/O	MICROPROCESSOR ADDRESS BUS: This 8-bit output bus is the AD(7:0) bus latched by the ALE pin during the low order address phase of a Multiplexed type microprocessor cycle. These signals are non-multiplexed address input when used with a Non-multiplexed microprocessor.
READY/$\overline{AINT}$	O, OD	READY/HOST SIDE INTERRUPT: When programmed as the Ready function, this signal is deasserted low for the microprocessor to insert wait states to allow time for the chip to respond to the access. When programmed as the host side interrupt, this pin interrupts the microprocessor when there is a host related interrupt event. The interrupt signal is programmable for either a push-pull or open-drain output circuit. This signal powers up as the 'Ready' function.

PIN DESCRIPTION (continued)

BUFFER MANAGER INTERFACE

BA(15:0)	O	BUFFER MEMORY ADDRESS LINES 15 through 0. These sixteen outputs provide address lines for the dynamic memory or static memory chips used to implement the buffer memory.
BA16/$\overline{RAS}$	O	BUFFER MEMORY ADDRESS 16: In SRAM mode, this pin generates the address: A16 for direct connection to a Static RAM address line 16. BUFFER ROW ADDRESS STROBE: This active low output signal is generated to strobe the row — high order — address into the dynamic RAMs. It is intended to be directly tied to the RAMs input control pin.
BA17/$\overline{CAS}$/$\overline{MS}$	O	BUFFER MEMORY ADDRESS 17/COLUMN ADDRESS STROBE/ MEMORY SELECT: This signal is used for addressing the buffer memory in SRAM mode or as the column address strobe in DRAM mode. When configured as $\overline{MS}$ this signal is active during both buffer memory reads and buffer memory writes. After $\overline{RST}$ is asserted, this signal will be high.
BD(7:0)	I/O	BUFFER MEMORY DATA BUS. 7 through 0. The bidirectional Data Bus connects directly to the buffer memory. This bus is designed for high speed data transfer.
BDP	I/O	BUFFER MEMORY PARITY: This bit is the parity value for BD(7:0).
$\overline{MOE}$/$\overline{MS}$	O	MEMORY OUTPUT ENABLE/MEMORY SELECT. When configured as $\overline{MOE}$, this signal is active during buffer memory reads. When configured as $\overline{MS}$, this signal is active during both buffer memory reads and buffer memory writes. The timing of the $\overline{MS}$ signal follows that of the address pins.
$\overline{WE}$	O	WRITE ENABLE. This active low output signal is used to strobe the data into the RAMs from the Data bus. For both buffer memory applications, this line is tied directly to the SRAM or DRAM control pin.
SYSCLK	I	SYSTEM CLOCK. This signal is used to synchronize the buffer RAM access, including the generation of memory address lines, write enable WE, and memory output enable MOE. In power down mode, this signal is shut off from the internal logic and hence buffer memory access is inhibited.

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC operating characteristics.

PARAMETER	RATING
Power Supply Voltage, VCC	7V
Ambient Temperature	0 to 70°C
Storage Temperature	-65 to 150°C
Power Dissipation	750 mW
Input, Output pins	-0.5 to VCC + 0.5V

ELECTRICAL CHARACTERISTICS

PARAMETER		CONDITIONS	MIN 3.3V	MAX 3.3V	MIN 5V	MAX 5V	UNIT
VDD	Power Supply Voltage		3	3.6	4.5	5.5	V
IDD	Supply Current			30		50	mA
IDDS	Standby Current	Note 1		250		250	µA
VIL	Input Low Voltage		-0.5	0.8	-0.5	0.8	V
VIH	Input High Voltage	Except $\overline{RST}$ pin	2	VCC + 0.5	2	VCC + 0.5	V
VIH	Input High Voltage	$\overline{RST}$ pin	2	VCC + 0.5	3.9	VCC + 0.5	V
VOL	Output Low Voltage	Note 2		0.4		0.4	V
VOL	Output Low Voltage	Note 3		0.5		0.5	V
VOH	Output High Voltage	IOH = -400 µA	2.15		2.4		V
IL	Input Leakage Current	0 < VIN < VCC	-10	10	-10	10	µA
CIN	Input Capacitance			10		10	pF
COUT	Output Capacitance			10		10	pF

Note: (1) Synchronization and Clock Control Register, 7FH: bits 3 and 4 set. RRCLK and SYSCLK internally inhibited.

(2) All interface pins except Host Interface pins. IOL = 2 mA.

(3) Host Interface pins, IOL = 16 mA @ 3.3V, IOL = 24 mA @ 5.0V.

ELECTRICAL SPECIFICATIONS (continued)

MICROPROCESSOR INTERFACE TIMING PARAMETERS

Multiplexed Bus Interface Timings (Figures 2, 3, 4, 5)

PARAMETER		CONDITIONS	MIN 3.3V	MAX 3.3V	MIN 5V	MAX 5V	UNIT
Ta	ALE Width		20		20		ns
Tma	Address valid to MA (7:0) valid			45		30	ns
Tr	$\overline{RD}$ Width		80		80		ns
As	Address valid to ALE ↓		5		5		ns
Ah	ALE ↓ to address invalid		10		10		ns
Cs	CS valid to $\overline{RD}$ ↓ or $\overline{DS}$ ↓		20		20		ns
Ch	$\overline{RD}$ ↑ or $\overline{DS}$ ↑ to CS ↓		0		0		ns
Tda	$\overline{RD}$ ↓ or $\overline{DS}$ ↓ to read data valid	Except Read of WCS		40		30	ns
Tda	$\overline{RD}$ ↓ or $\overline{DS}$ ↓ to read data valid	Read of WCS		60		50	ns
Tds	$\overline{DS}$ width		80		80		ns
Tdh	RD ↑ to or $\overline{DS}$ ↑ read data invalid		0	25	0	25	ns
Tsrw	R/$\overline{W}$ valid to $\overline{DS}$ ↓		20		20		ns
Thrw	$\overline{DS}$ ↑ to R/W invalid		20		20		ns
Tdrdy	$\overline{RD}$ ↓ to READY ↓ (Intel) or $\overline{DS}$ ↓ to READY ↓ (Motorola)			45		30	ns ns
Wds	Write data valid to $\overline{WR}$ ↑ or $\overline{DS}$ ↑		40		40		ns
Wdh	$\overline{WR}$ ↑ or $\overline{DS}$ ↑ to write data invalid		10		10		ns

Non-Multiplexed Bus Interface Timings (Figure 6)

Tmas	MA (7:0) valid to $\overline{DS}$ ↓		5		5		ns
Tmah	$\overline{DS}$ ↑ to MA (7:0) invalid		5		5		ns
Cs	CS valid to $\overline{DS}$ ↓		20		20		ns
Ch	$\overline{DS}$ ↑ to CS ↓		0		0		ns
Tda	$\overline{RD}$ ↓ or $\overline{DS}$ ↓ to read data valid	Except Read of WCS		40		30	ns
Tda	$\overline{RD}$ ↓ or $\overline{DS}$ ↓ to read data valid	Read of WCS		60		50	ns
Tds	$\overline{DS}$ width		80		80		ns
Tdh	$\overline{DS}$ ↑ to read data invalid		0	25	0	25	ns
Tsrw	R/$\overline{W}$ valid to $\overline{DS}$ ↓		20		20		ns
Thrw	$\overline{DS}$ ↑ to R/$\overline{W}$ invalid		20		20		ns
Tdrdy	$\overline{DS}$ ↓ to READY ↓ (Motorola)			45		30	ns
Wds	Write data valid to $\overline{WR}$ ↑ or $\overline{DS}$ ↑		40		40		ns
Wdh	$\overline{WR}$ ↑ or $\overline{DS}$ ↑ to write data invalid		10		10		ns

Note: (1) Loading capacitor = 30 pF
(2) ↑ indicates rising edge ↓ indicates falling edge

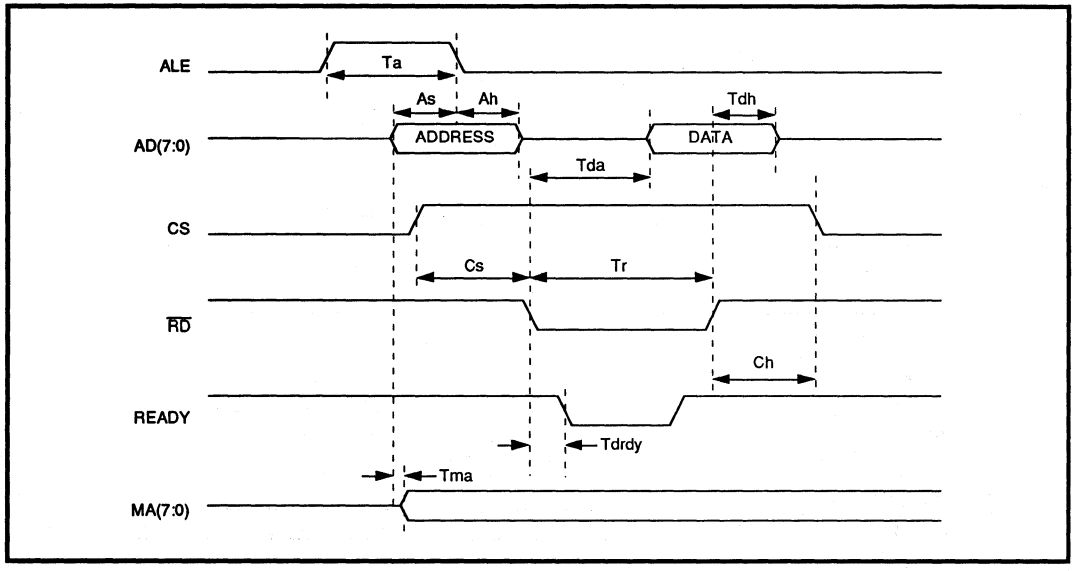


FIGURE 2: Intel Register Multiplexed Read Timing

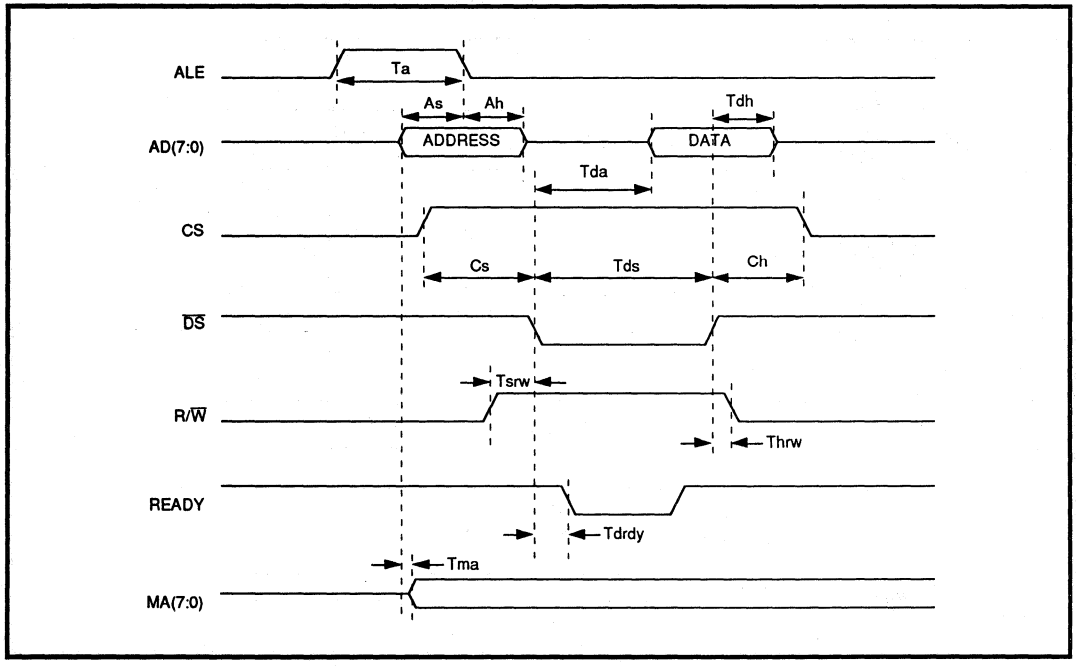


FIGURE 3: Motorola Register Multiplexed Read Timing

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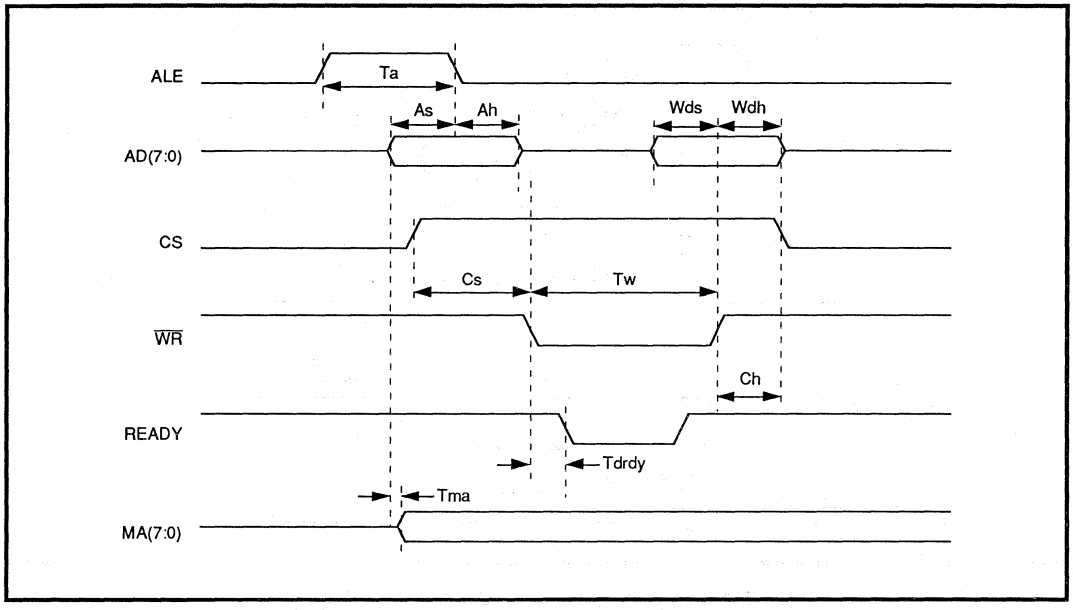

FIGURE 4: Intel Register Multiplexed Write Timing

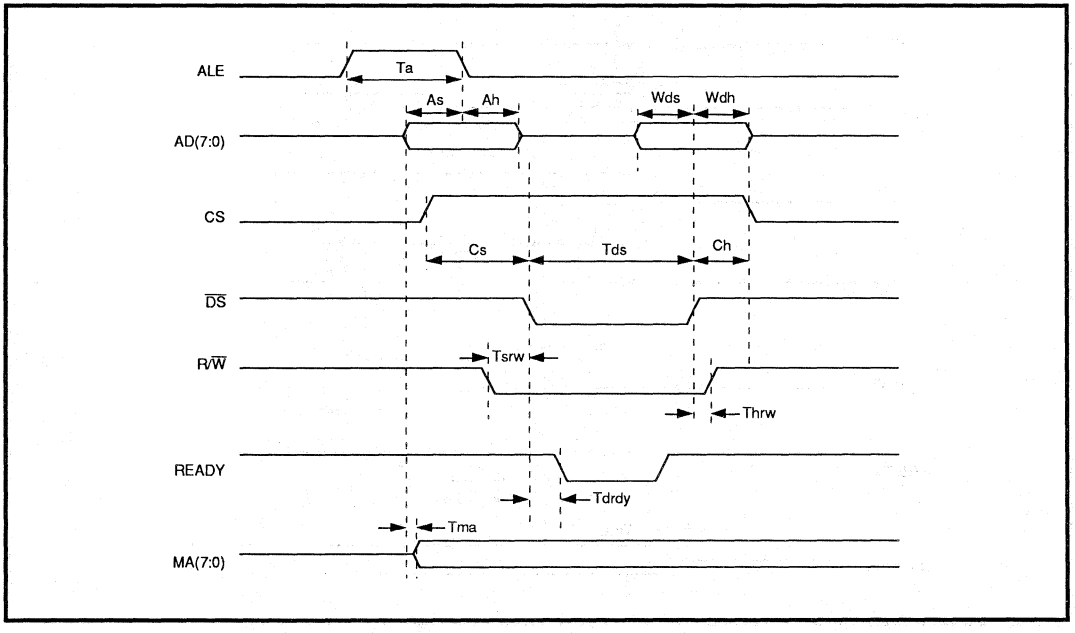

FIGURE 5: Motorola Register Multiplexed Write Timing

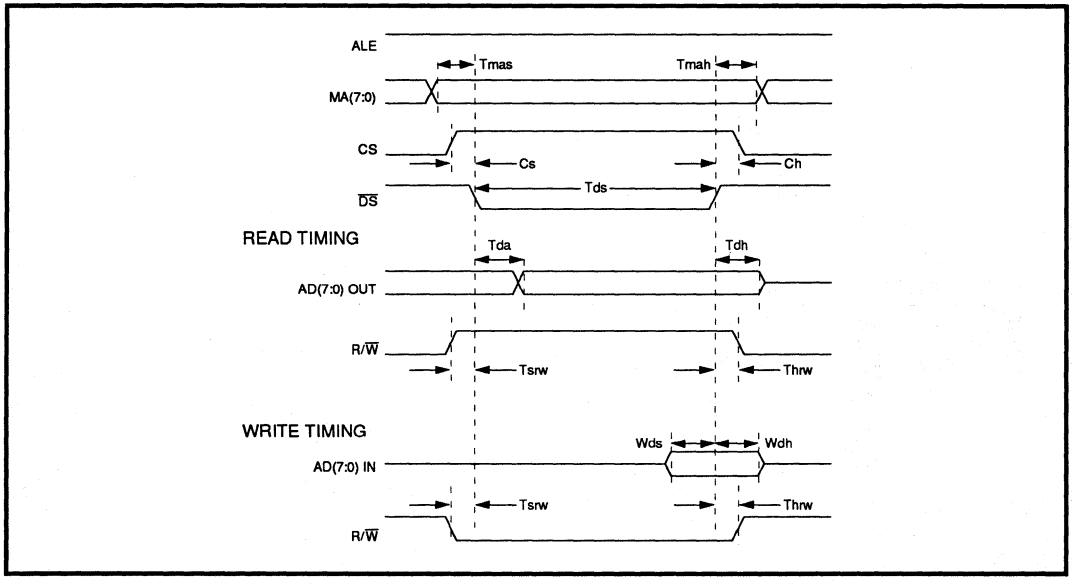

FIGURE 6: Non-Multiplexed Bus Timing Diagrams

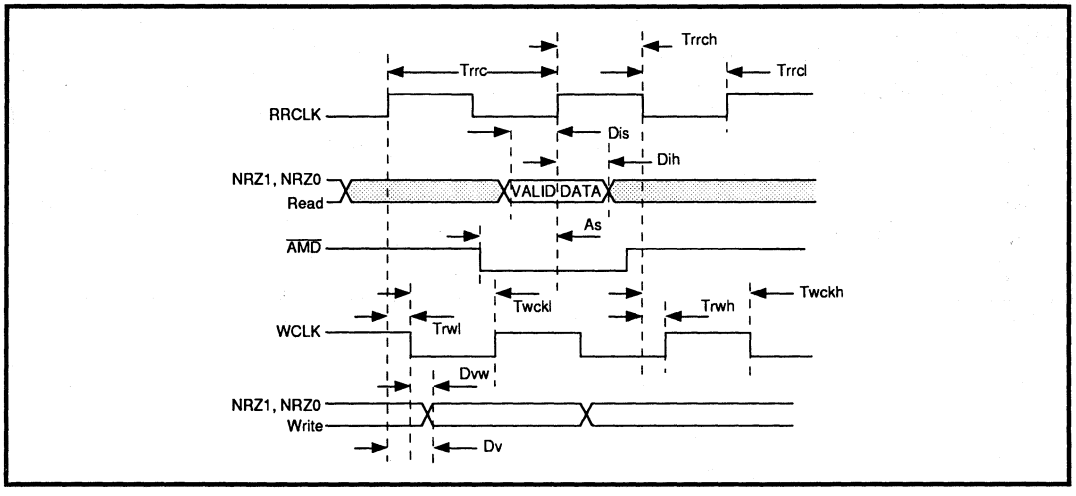

FIGURE 7: Disk Interface Timing

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ELECTRICAL SPECIFICATIONS (continued)

MICROPROCESSOR INTERFACE TIMING PARAMETERS

Disk Read/Write Timing (Figure 7)

PARAMETER		CONDITIONS	MIN 3.3V	MAX 3.3V	MIN 5V	MAX 5V	UNIT
Trrc	RRCLK period (dual bit)		41		41		ns
Trrc	RRCLK period (single bit)		31		20.8		ns
Trrcl	RRCLK low time (dual bit)		16		16		ns
Trrcl	RRCLK low time (single bit)		12		12		ns
Trrch	RRCLK high time (dual bit)		16		16		ns
Trrch	RRCLK high time (single bit)		12		12		ns
Dis	NRZ in valid to RRCLK high		5		3		ns
Dih	RRCLK high to NRZ in invalid		5		3		ns
As	$\overline{AMD}$ valid to RRCLK high (soft sector only)		5		3		ns
Dv	RRCLK high to NRZ1, NRZ0 out valid			27		18	ns
Dvw	WCLK low to NRZ1, NRZ0 out valid		-3	+3	-3	+3	ns
Trwl	RRCLK high to WCLK low			27		18	ns
Trwh	RRCLK low to WCLK high			27		18	ns
Twckh	WCLK high time (dual bit)		12		12		ns
Twckh	WCLK high time (single bit)		9		9		ns
Twckl	WCLK low time (dual bit)		12		12		ns
Twckl	WCLK low time (single bit)		9		9		ns
Note:	Loading capacitance = 10 pF						

BUFFER MEMORY READ/WRITE TIMING PARAMETERS (Figures 8 through 13)

PARAMETER		CONDITIONS	MIN 3.3V	MAX 3.3V	MIN 5V	MAX 5V	UNIT
T	SYSCLK period		35		25		ns
T↑2	SYSCLK high↑low time		12		10		ns
Tav	SYSCLK ↑ to address valid	(Note 1)		30		18	ns
Tmsv	SYSCLK ↑ to $\overline{MS}$↓	(Notes 1, 6)		30		18	ns
Tmsh	SYSCLK ↑ to $\overline{MS}$↑	(Note 1)		30		18	ns
Tmv	SYSCLK ↑ to $\overline{MOE}$↓	(Note 1)		30		18	ns
Tmh	SYSCLK ↑ to $\overline{MOE}$↑	(Note 1)		30		18	ns
Twv	SYSCLK ↑ to $\overline{WE}$↓	(Note 1)		30		18	ns
Twh	SYSCLK ↑ to $\overline{WE}$↑	(Note 1)		30		18	ns
Tdov	SYSCLK to data out valid	(Note 1)		30		18	ns
Tdoh	SYSCLK to data out invalid	(Note 1)		30		18	ns
Tdis	Data in valid to $\overline{MOE}$↑ (SRAM) Data in valid to $\overline{CAS}$↑ (DRAM)		5		5		ns
Tdih	$\overline{MOE}$↑ to data in valid (SRAM) $\overline{CAS}$↑ to data in valid (DRAM)		0		0		ns
Trv	SYSCLK ↑ to $\overline{RAS}$↓	(Note 1)		30		18	ns
Trh	SYSCLK ↑ to $\overline{RAS}$↑	(Note 1)		30		18	ns
Trav	SYSCLK to row address valid	(Note 1)		30		18	ns
Trah	SYSCLK ↑ to row address invalid	(Note 1)		30		18	ns
Tcv	SYSCLK ↑ to $\overline{CAS}$↓	(Note 1)		30		18	ns
Tch	SYSCLK ↑ to $\overline{CAS}$↑	(Note 1)		30		18	ns
Tcav	SYSCLK ↑ to column address valid	(Note 1)		30		18	ns
Tcah	SYSCLK ↑ to column address invalid		0		0		ns

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ELECTRICAL SPECIFICATIONS (continued)

BUFFER MEMORY READ/WRITE FUNCTIONAL PARAMETERS (Figures 8 through 13) (continued)

PARAMETER		CONDITIONS	TYPICAL	UNIT
Trwl	$\overline{RAS}\downarrow$ to $\overline{RAS}\uparrow$	Notes 2, 3	(RWL + 3)•T	ns
Trwh	$\overline{RAS}\uparrow$ to $\overline{RAS}\downarrow$	Notes 2, 4	(RWH + 1)•T	ns
Tcwl	$\overline{CAS}\downarrow$ to $\overline{CAS}\uparrow$	Note 2	(CWL + 1)•T	ns
Tcwh	$\overline{CAS}\uparrow$ to $\overline{CAS}\downarrow$	Notes 2, 5	(CWL + 1)•T	ns

Notes: Loading capacitance = 30 pF

Note 1: The measured delay for any of the signal indicated by this note will not vary from the measured delay of any other signal indicated by this note by more than ±2 ns.

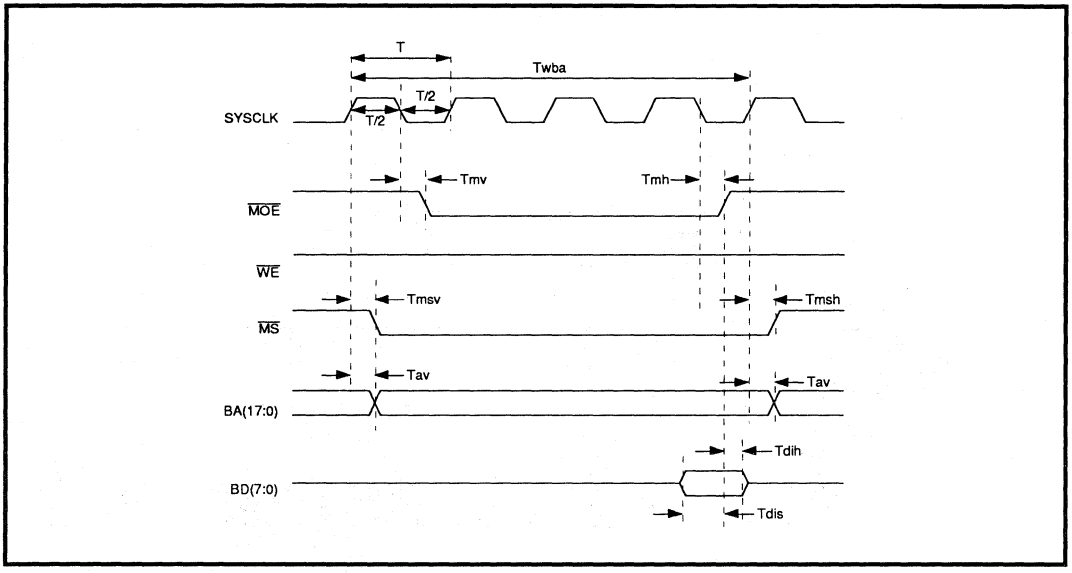
Note 2: RWL, RWH, CWL and CWH are fields in the Buffer Manager Timing Control Register (54H). Each is a two bit field which can contain a value of 0, 1, 2, or 3. These values determine the minimum number of SYSCLK periods (T) for the associated signal width.

Note 3: The minimum width value of Trwl will be generated for refresh cycles and for any buffer memory access cycle except when multiple page mode accesses are performed. When multiple page mode accesses are performed, the width of the $\overline{RAS}$ low pulse is extended until the end of the last $\overline{CAS}$ low cycle.

Note 4: The minumum value of Trwh will be generated whenever the Buffer Manager determines that a buffer request is pending at the completion of the current memory cycle and a page mode access can not be used because the needed location is not within the current page, or a new memory request is being processed.

Note 5: The minumum value of Tcwh will be generated only between consecutive page mode accesses.

Note 6: $\overline{MS}$ will rise only if the Buffer Manager determines that no additional requests for buffer access are pending. If the Buffer Manager determines that another access is to be made, $\overline{MS}$ is kept low between the accesses for improved speed.



Note: Twba is a functional parameter that gives the duration of one RAM data buffer access cycle in SYSCLK periods. The value is programmed in bits 1-0 of register 54H. These examples show Twba = 4T.

FIGURE 8: SRAM Read Timing

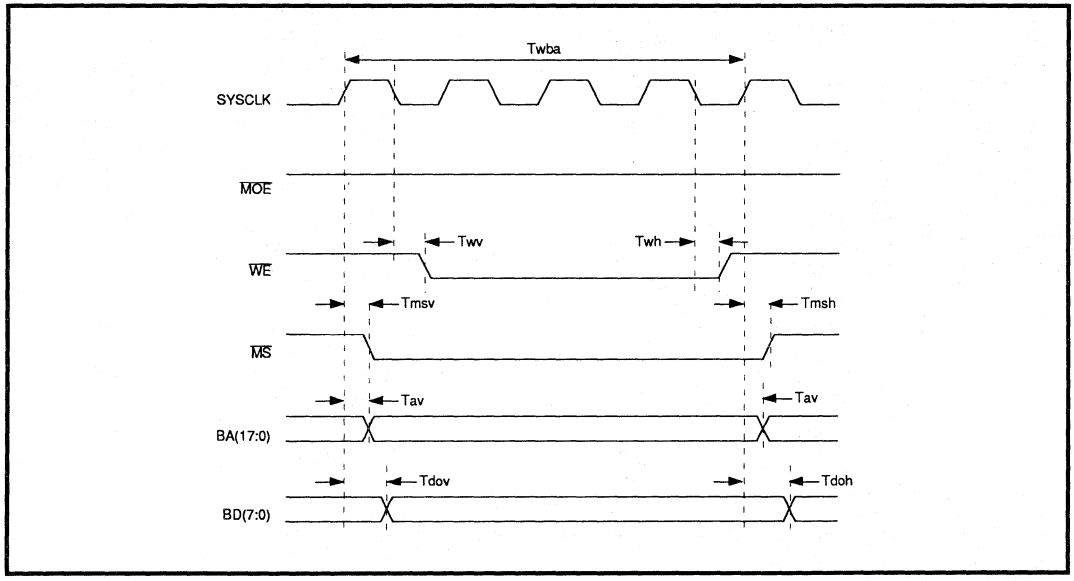


FIGURE 9: SRAM Write Timing

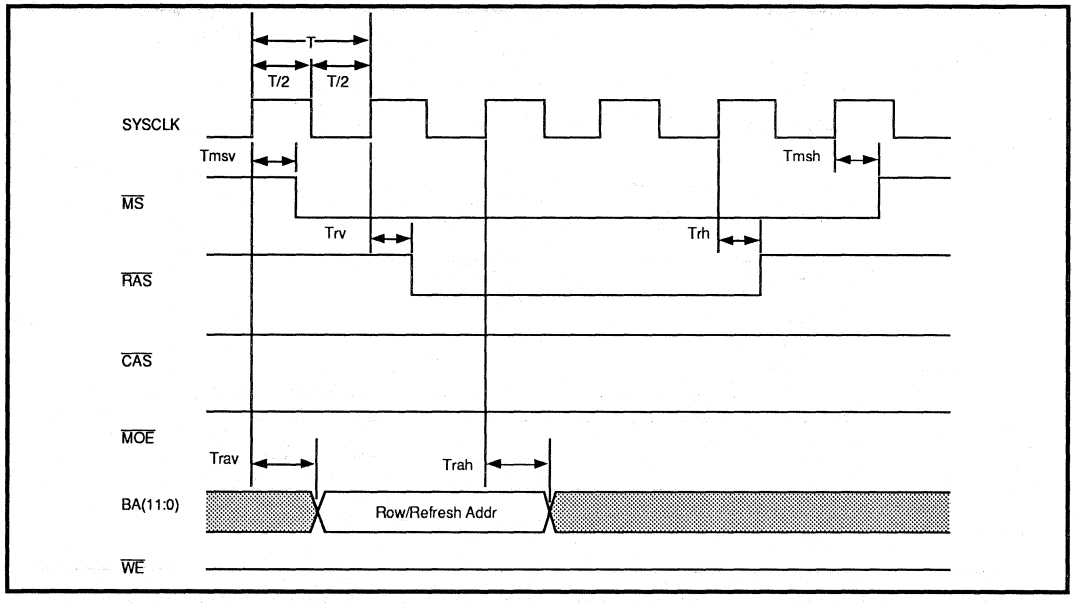


FIGURE 10: DRAM Timing, Refresh Cycle (Shown with WRL = 0)

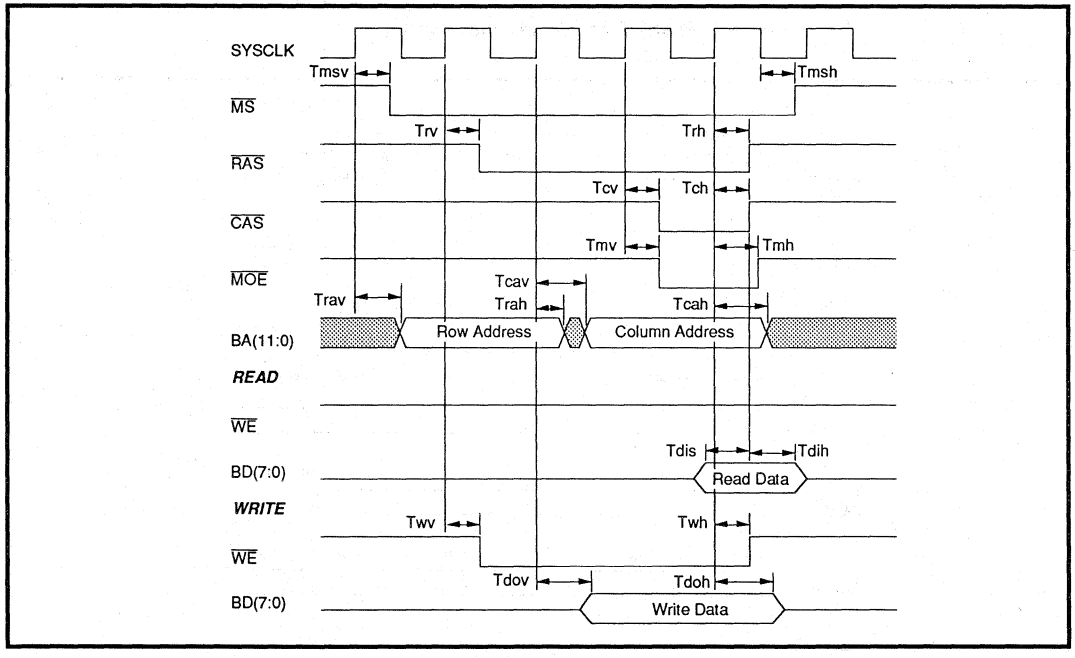


FIGURE 11: DRAM Timing, Standard Cycle (Shown with RWL = 0 and CWL = 0)

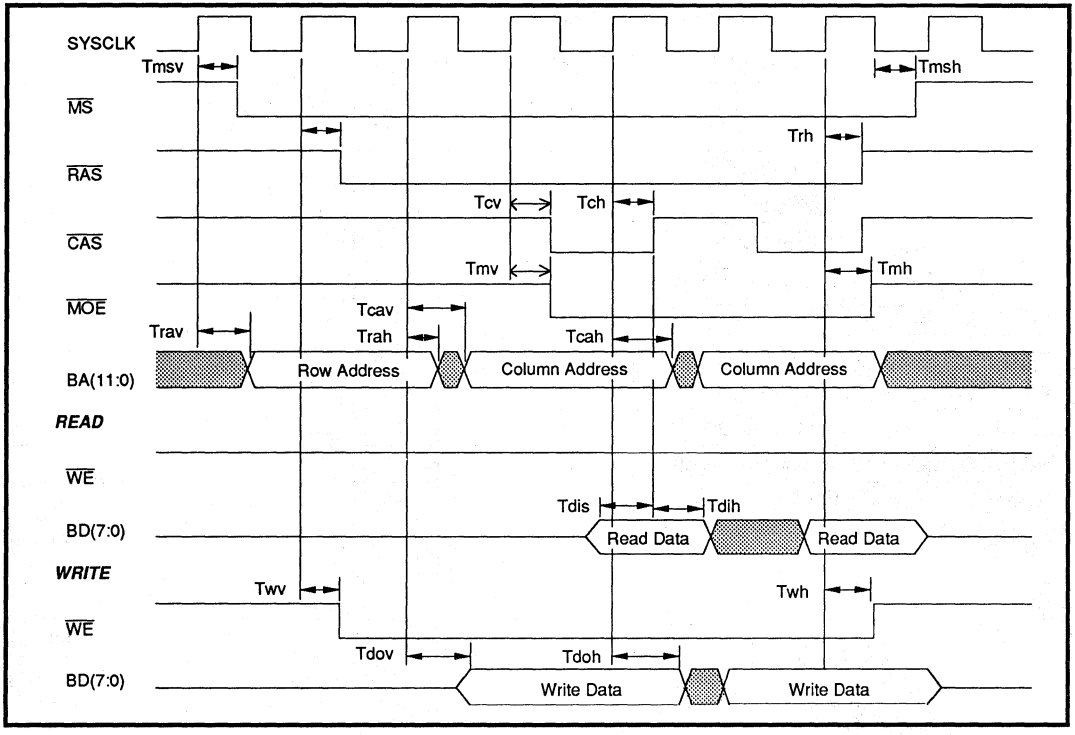


FIGURE 12: DRAM Timing, Fast Page Cycles (Shown with RWL = 0, RWH = 0, CWL = 0 and CWH = 0)

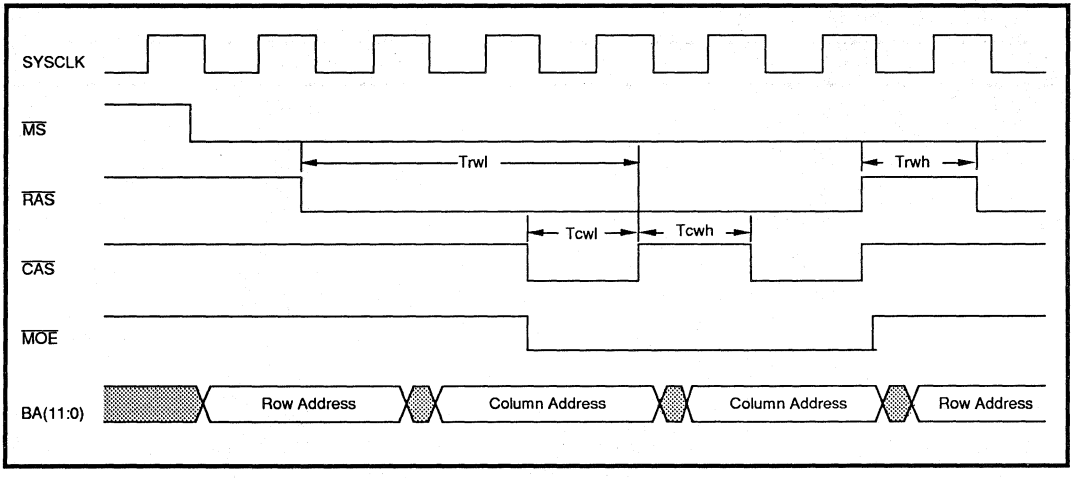


FIGURE 13: DRAM Timing (Showing the Relationship of RWL, RWH, CWL and CWH to overall timing)

ELECTRICAL SPECIFICATIONS (continued)

AT HOST INTERFACE TIMING PARAMETERS (Figures 14 through 16)

PARAMETER		CONDITIONS	MIN 3.3V	MAX 3.3V	MIN 5V	MAX 5V	UNIT
DREQL	$\overline{DACK}$ ↓ to DREQ ↓			50		40	ns
DREQD	$\overline{IOR}$ ↓ or $\overline{IOW}$ ↓ to DREQ ↓			50		40	ns
RDTA	$\overline{IOR}$ ↓ to HD(15:0) valid			70		50	ns
DMASET	$\overline{DACK}$ ↓ to $\overline{IOW}$ ↓ or $\overline{IOR}$ ↓		0		0		ns
DMAHLD	$\overline{IOR}$ ↑ or $\overline{IOW}$ ↑ to $\overline{DACK}$ ↑		0		0		ns
RDHLD	$\overline{IOR}$ ↑ to HD (15:0) hi-Z		2	20	2	20	ns
WDS	HD(15:0) setup to $\overline{IOW}$ ↑		30		30		ns
WDHLD	HD(15:0) hold from $\overline{IOW}$ ↑		10		10		ns
RWPULSE	$\overline{IOR}$ or $\overline{IOW}$ low pulse width		80		80		ns
RWH	$\overline{IOR}$ or $\overline{IOW}$ high pulse width		50		50		ns
CS16L	$\overline{HCS0}$ ↓, A(2:0) ↓ or $\overline{HCS1}$ ↑ to $\overline{IOCS16}$ ↓			30		20	ns
IOCHL	$\overline{IOR}$ or $\overline{IOW}$ ↓ to $\overline{IOCHRDY}$ ↓			35		25	ns
ADRSET	$\overline{HCS0}$, A(2:0), $\overline{HCS1}$ setup to $\overline{IOR}$ ↓ or $\overline{IOW}$ ↓				25		ns
ADRHLD	$\overline{HCS0}$, A(2:0), $\overline{HCS1}$ hold from $\overline{IOR}$ ↑ or $\overline{IOW}$ ↑		5		5		ns
Note: Loading capacitance = 30 pF							

FUNCTIONAL SPECIFICATION

IOCHTW	$\overline{IOCHRDY}$ pulse width		0	5xBCLK	0	5xBCLK	ns

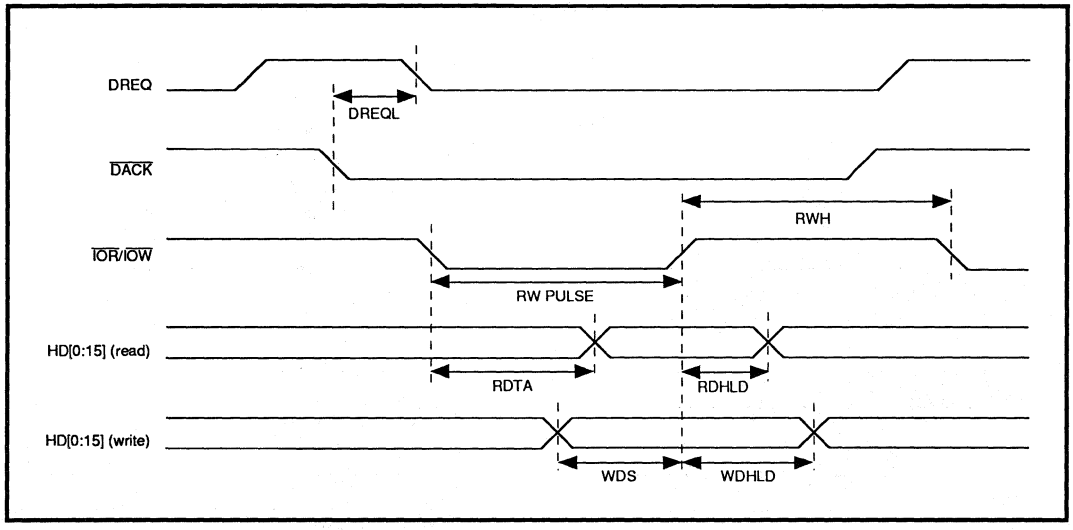


FIGURE 14: Host DMA 8-16 Bit Interface Timing (Non-demand mode)

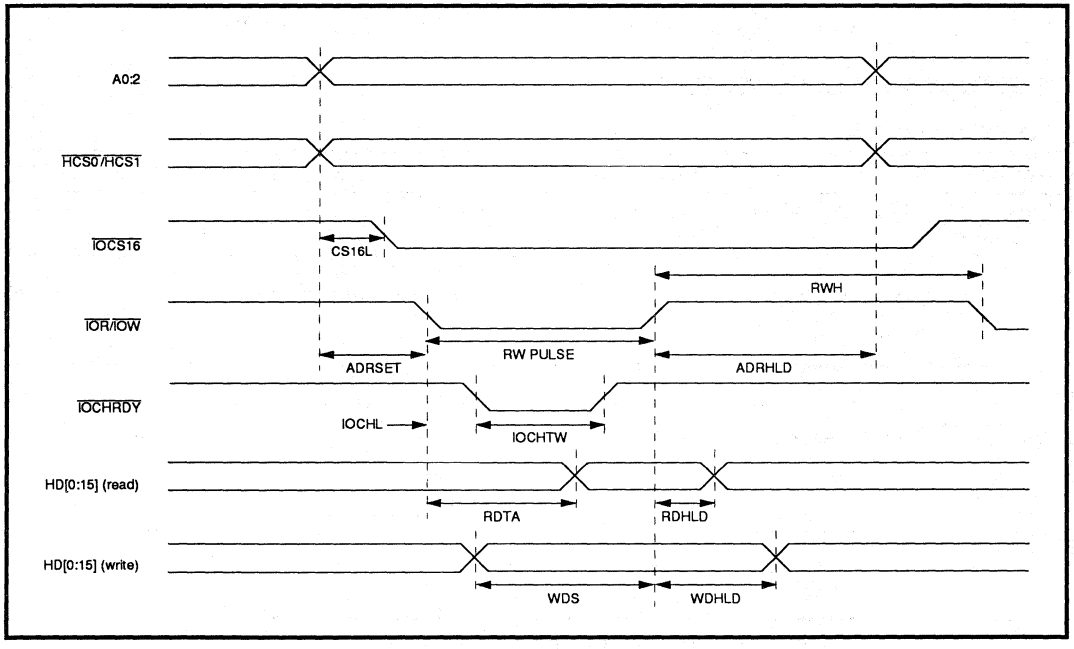


FIGURE 15: Host Programmed I/O 8-16 Bit Timing

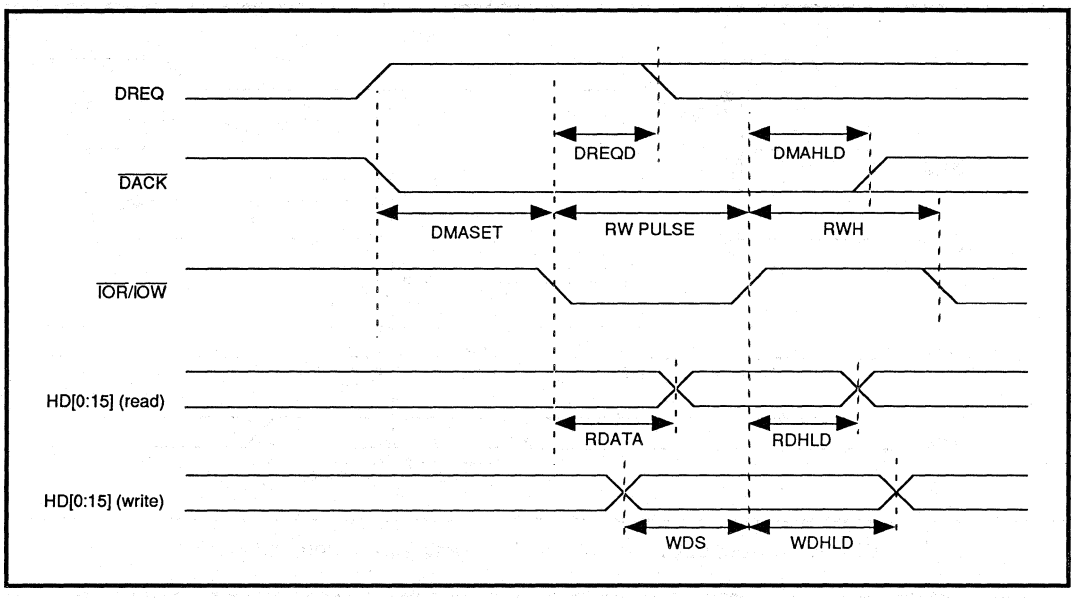


FIGURE 16: Host DMA 8/16-Bit Interface Timing (Demand Mode)

ELECTRICAL SPECIFICATIONS (continued)

POWER SUPPLY

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Trpwl $\overline{RST}$ pulse width low	NOT Power On Reset	500			ns
	Power On Reset	7.5			µs

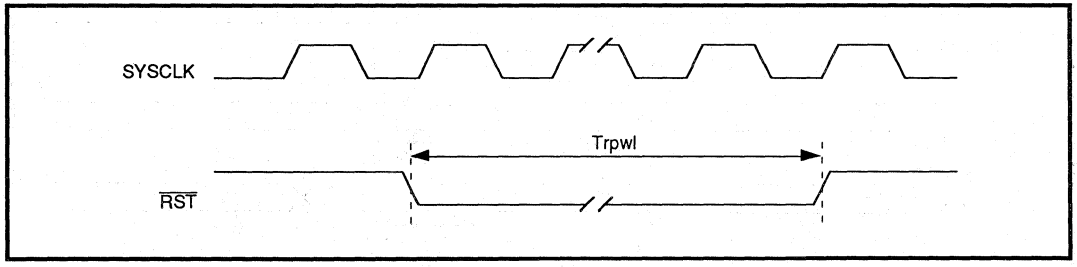
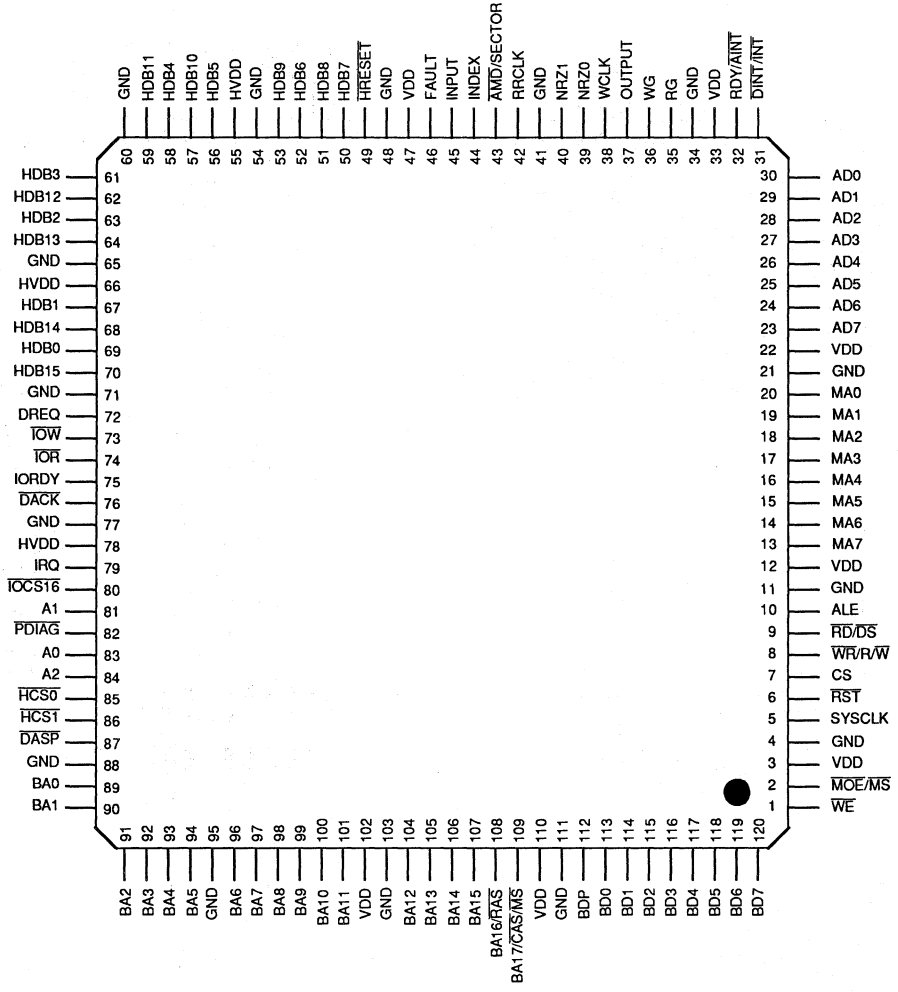


FIGURE 17: RESET Assertion Timing

PACKAGE PIN DESIGNATION
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



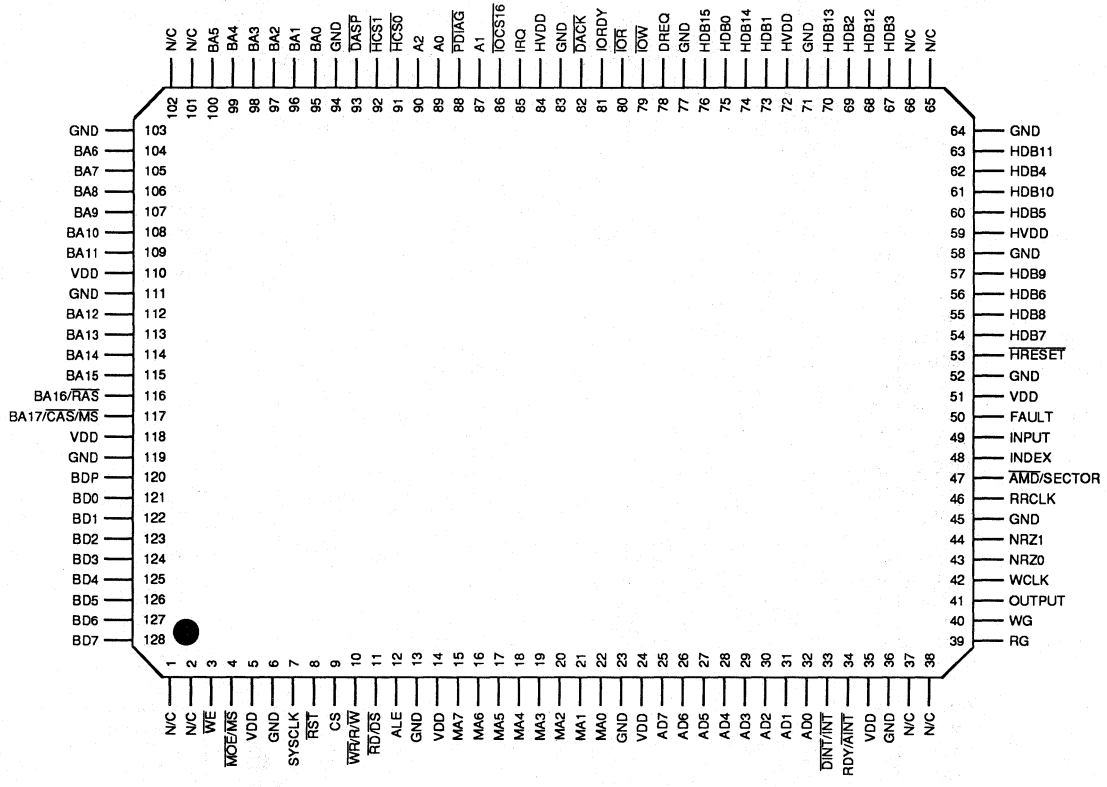
120-Lead TQFP

9

SSI 32C9302
PC-AT Combo Controller
With Reed Solomon, 3.3V Operation

PACKAGE PIN DESIGNATION
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



128-Lead QFP, TQFP

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only. Do not use for final design.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX: (714) 573-6914

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A TDK Group Company

SSI 32C9340
PCMCIA Combo Controller with Reed Solomon, 48 Mbit/s
Target Specification

January 1994

DESCRIPTION

The SSI 32C9340 is a CMOS VLSI device which integrates major portions of the hardware needed to build a PCMCIA and/or ATA drive hard disk controller. The SSI 32C9340's place in the Silicon Systems' chip family is illustrated in the hierarchy chart in Figure 1. It provides most of the functional circuitry necessary to build a PCMCIA intelligent disk.

The SSI 32C9340 is capable of supporting interleaved host and disk transfers while maintaining a disk data transfer rate of up to 48 Mbit/s.

The SSI 32C9340 includes a multi-port Buffer Manager, a storage controller and a high performance PCMCIA host interface block that incorporates extensive hardware support — including direct connection to a PCMCIA or ATA bus.

The SSI 32C9340 performs all the controller functions for the peripheral device including: Serialization and deserialization of data; and, ECC generation, checking and on-the-fly data correction.

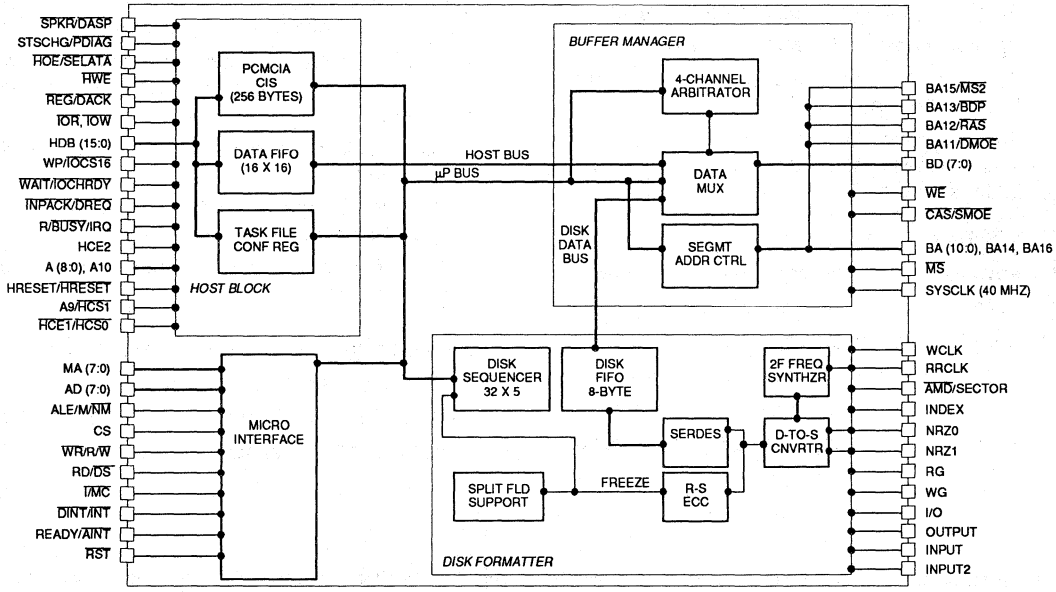
FEATURES

HOST INTERFACE:

- **PCMCIA/ATA and ATA compatible host interface**
- **Hardware and software compatible with PCMCIA bus standard, revision 2.0**
- **Programmable 256-byte PCMCIA CIS integrated**
- **High Current drivers for direct connection to the PCMCIA or AT bus**
- **Both memory and I/O interfaces supported for PCMCIA**
- **Includes IBM AT compatible Task File registers and PCMCIA configuration registers**
- **Hardware added to provide Multi-Sector data transfers without microprocessor intervention**
- **Automatic BUSY, INTRQ**
- **16 byte FIFO to improve throughput**
- **PC transfers to 4(6.7 @ 5V) megawords/second**

(continued)

BLOCK DIAGRAM



SSI 32C9340
PCMCIA Combo Controller with Reed Solomon, 48 Mbit/s

FEATURES (continued)

- Automatic command decoding of write, write long, write DMA, write multiple, write buffer and format commands
- Automatic update of the host task file registers in both LBA mode and Cyl/Hd/Sec mode
- Support for ATA master/slave operation
- Power-down IO pins

BUFFER MANAGER:

- Supports Buffer RAM throughput up to:
  5V: 20 MByte/sec for SRAM and 17.78 MByte/sec for DRAM (with 40MHz SYSCLK)
  3.3V: 16 MByte/sec for SRAM and 14 MByte/sec for DRAM (with 30 MHz SYSCLK)
- Programmable microprocesssor scratch pad area
- Auto data streaming capability
- Supports Multiple sector host data transfer
- Supports up to 1M byte DRAM and up to 128K SRAM
- Supports variable DRAM and SRAM timings and sizes
- Reload transfer counter and host address pointers
- Supports page mode DRAM access
- Programmable DRAM page mode burst length
- Programmable DRAM refresh period
- Separate host, disk, and microprocessor buffer RAM address pointers
- Provides protection logic for buffer data allowing simultaneous host and disk accesses to the same buffer segment.

DISK FORMATTER:

- Advanced sequencer organized in 31 x 5 bytes
- Advanced branch and interrupt logic
- Defect management support
- Supports multiple-sector data transfers
- NRZ byte synchronization time out timer
- Three-index counter providing limit of search and retry
- 8-byte stack for header information storage
- 16-byte disk data FIFO
- Sector header or microprocessor-based split data field processing logic supporting embedded servo and zone-bit recording
- Supports variable data field length
- Disk transfer rate up to 48 Mbit/s NRZ
- Power Down Mode

MICROPROCESSOR INTERFACE:

- High speed internal register access
- Programmable wait state insertion
- Supports both Intel and Motorola type microprocessers

ERROR CORRECTION LOGIC:

- Enhanced 16-bit CRC polynomial with one order of magnitude better burst error detection than CCITT-CRC16
- Non-interleaved 88-bit Reed Solomon Code of degree 8 operation on 10-bit symbols
- Automatic on-the-fly in-buffer error correction
- Selectable on-the-fly error correction span of 11 bits signal burst
- Calculation of buffer offsets and masks for on-the-fly ECC within one half of a sector time
- On the fly in-buffer correction accomplished in no more than 3 buffer reads and writes through an independent channel
- Capable of correcting by software four 10-bit symbols in error
- Guaranteed to correct by software one 31-bit burst or two 11-bit bursts
- Detects up to one 51-bit burst or three 11-bit bursts

OTHERS:

- Automatic power supply level detection circuit
- JEDEC conformant 3.3V specification
- TTL-Level compatible input receivers at 3.3V or 5V
- Avaiable in 120-pin surface mount TQFP

FUNCTIONAL DESCRIPTION

The SSI 32C9340 is capable of operating in either a 3.3 volt or 5 volt environment.

The SSI 32C9340 contains the following four major functional blocks:

Microprocessor Interface

PCMCIA/ATA Interface

Disk Formatter

Buffer Manager

The Microprocessor Interface allows the local microprocessor access to all of the SSI 32C9340 internal control registers and any location within the buffer memory. The microprocessor, by writing and reading the internal registers, can control all activities of the SSI 32C9340. The microprocessor can elect to perform host and/or disk operations directly, or it can enable the advanced features of the SSI 32C9340 which can perform these operations automatically.

The PCMCIA/ATA Interface block can interface with the PCMCIA interface as a PCMCIA/ATA device or with a PC AT bus. The SSI 32C9340 has on-board sensing logic to help determine whether it is operating in either the PCMCIA or ATA mode. The interface includes 12 mA (8 mA @3.3V) drivers allowing for direct connection of the SSI 32C9340 to either the PCMCIA or PC AT bus. The interface is highly automated, capable of performing multiple block transfers without micro- controller involvement. The PCMCIA/ATA block interfaces directly with the Buffer Manager via an internal speed matching FIFO. This FIFO, the bandwidth capabilities of the Buffer Manager, plus the advanced features of the PCMCIA/ATA Interface guarantee sustained full speed transfers.

The Disk Formatter performs the serialization and deserialization of data. It provides all of the necessary functions to control track formatting, header search, and the reading and writing of data. The heart of the Disk Formatter is an advanced programmable sequencer. The sequencer can contain 31 instructions, each of which is 5 bytes (40 bits) in width. The width of the instructions allows for sophisticated branching techniques which increase the flexibility and power of the sequencer. The disk interface can be configured through a wide range of capabilities. This allows the SSI 32C9340 to interface with nearly any read/write channel. This allows the user of the SSI 32C9340 to select the read/write channel best suited to the device. Of course, by selecting the SSI 32C9340 controller and the SSI 32P4330 Read Channel with 1,7 ENDEC, you are guaranteed a problem free interface.

Within the Disk Formatter are the ECC generator/checker and ECC corrector. The generator/checker provides the ability to generate or check a 32 bit ECC for headers and an 88 bit Reed Solomon code for data. If the checker detects an error in an 88 bit Reed Solomon data field, the syndrome information is transferred into the corrector. The corrector then performs the necessary operations to determine if the error was correctable and, if it was correctable, the corrector interfaces directly with the buffer controller and performs the correction automatically. The corrector performs its correction within one half of a sector. This guarantees that the corrector will always be available to correct the next sector if necessary.

The Buffer Manager manages the data buffer of the controller. The Buffer Manager can support either SRAM or DRAM. When configured to operate with DRAM, the Buffer Manager automatically performs necessary refresh cycles. The buffer manager creates all of the necessary timing and control signals for a wide range of memory types and speeds. Besides interfacing with the buffer memory, the Buffer Manager interfaces with the ATA Interface block, the Disk Formatter block, the ECC corrector and the microprocessor. If more than one of these devices requires access to the buffer memory, the Buffer Manager arbitrates the requests automatically. The Buffer Manager of the SSI 32C9340 can sustain ATA operations at the rate of 4 (6.7 @ 5V) megawords per second, Disk Formatter operations at 48 megabits per second and still have sufficient bandwidth left to handle on-the-fly ECC corrections and microprocessor accesses without degrading performance on any of the interfaces.

SSI 32C9340
PCMCIA Combo Controller with Reed Solomon, 48 Mbit/s

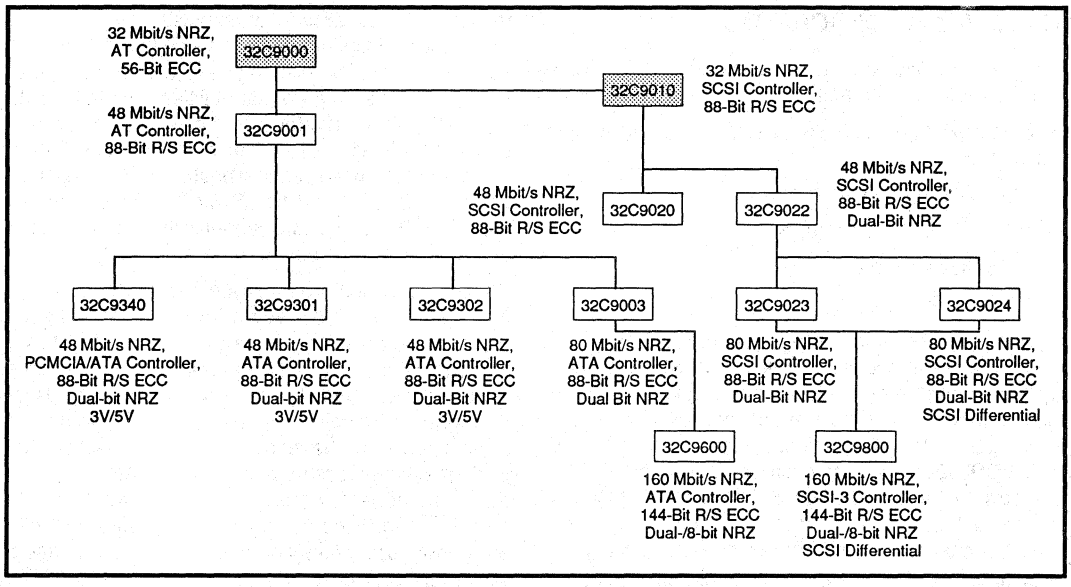


FIGURE 1: Silicon Systems's Disk Controller Chip Hierarchy

PIN DESCRIPTION

I = input, O = output; Z = tri-state output, OD = open drain output. All unused inputs must be tied to the inactive state to VCC or GND, respectively.

BUFFER MANAGER INTERFACE

NAME	TYPE	DESCRIPTION
BA16	I/O	BUFFER ADDRESS 16. In SRAM mode, this pin may be configured as buffer address 16.
BA15/$\overline{MS2}$	O	BUFFER ADDRESS 15/MEMORY SELECT. In SRAM mode, this pin may be configured as buffer address 15 or memory select 2 for 2nd bank of memory. After $\overline{RST}$ is asserted, this signal will be high.
BA14	I/O	BUFFER MEMORY ADDRESS 14. This signal is used for addressing the buffer memory in SRAM mode.
BA13/BDP	I/O	BUFFER MEMORY ADDRESS 13/BUFFER MEMORY PARITY. This signal is used for addressing the buffer memory in SRAM mode, or as the buffer data parity value in DRAM mode.
BA12/$\overline{RAS}$	O	BUFFER MEMORY ADDRESS 12/ROW ADDRESS STROBE: This signal is used for addressing the buffer memory in SRAM mode or as the row address strobe in DRAM mode. After $\overline{RST}$ is asserted, this signal will be high.
BA11/$\overline{DMOE}$	O	BUFFER MEMORY ADDRESS 11/DRAM MEMORY OUTPUT ENABLE. This signal is used for addressing the buffer memory in SRAM mode, or as the memory output enable pin in DRAM mode. After $\overline{RST}$ is asserted, this signal will be high.
BA(10:0)	O	BUFFER MEMORY ADDRESS LINES. These are signals 10-0 for addressing the buffer memory.
BD(7:0)	I/O	BUFFER MEMORY DATA BUS. These eight signals are bits 7-0 of the 8-bit parallel data lines to/from the buffer memory. Note that BD6 is used to select between the Intel- and Motorola-style microprocessor interfaces. If BD6 is externally pulled up when $\overline{RST}$ is asserted, Intel mode is used; if BD6 is externally pulled down when $\overline{RST}$ is asserted, Motorola mode is used.
$\overline{CAS}$/$\overline{SMOE}$	O	COLUMN ADDRESS STROBE/SRAM MEMORY OUTPUT ENABLE. This signal is used as the column address strobe in DRAM mode, or the memory output enable in SRAM mode. After RST is asserted, this signal will be high.
$\overline{MS}$	O	MEMORY SELECT. An active low signal indicates external memory is selected (chip enabled) or 1st bank of memory is selected.
SYSCLK	I	SYSTEM CLOCK. This signal is used to synchronize the buffer RAM access, including the generation of memory address lines, write enable WE, and memory output enable MOE. In power down mode, this signal is shut off from the internal logic and hence buffer memory access is inhibited.
WE	O	WRITE ENABLE. This active low output signal is used to strobe the data into the RAMs from the DAta bus. For both buffer memory applications, this line is tied directly to the SRAM or DRAM control pin.

PIN DESCRIPTION (continued)

MICROPROCESSOR INTERFACE

NAME	TYPE	DESCRIPTION
$\overline{RST}$	I	RESET. An asserted active low input generates a component reset that holds the internal registers of the SSI 32C9001 at reset, stops all operations within the chip, and deasserts all output signals. All input/output signals and Host outputs are set to the high-Z state.
ALE/M/$\overline{NM}$	I	ADDRESS LATCH ENABLE/MULTIPLEXED/NON-MULTIPLEXED ADDRESS SELECT. When tied high, the microprocessor interface is configured as non-multiplexed. When driven low, the microprocessor interface is configured as multiplexed. In this case this pin functions as the address latch enable, and the MA(7:0) pins are the demultiplexed address outputs.
CS	I	CHIP SELECT. This signal must be asserted high for all microprocessor accesses to the registers of this chip.
$\overline{WR}$/R/$\overline{W}$	I	WRITE STROBE/READ/WRITE. In the Multiplexed address/data bus mode, when an active low signal is present with CS signal asserted high, the data on the AD0:7 is written to the internal registers. In the Non-Multiplexed address/data bus mode, this signal acts as the R/$\overline{W}$ signal. A high on this input along with the $\overline{RD}$/DS signal asserted and the CS signal asserted high indicates a read operation. A low on this input along with the $\overline{RD}$/DS signal asserted and the CS signal asserted high indicates a write operation. See table below.

CS	$\overline{WR}$/R/$\overline{W}$	$\overline{RD}$/DS	Mux/Non-Mux	Action
High	Low	High	Intel Multiplexed	Write to internal registers.
High	High	Low	Intel Multiplexed	Read from internal registers.
High	Low	High	Motorola Multiplexed	Write to internal registers.
High	Low	Low	Non-Multiplexed	Write to internal registers.
High	High	High	Motorola Multiplexed	Read from internal registers.
High	High	Low	Non-Multiplexed	Read from internal registers.
Low	X	X	M or N	No action.

Note: X denotes don't care.

$\overline{RD}$/DS	I	READ STROBE/DATA STROBE. In the Multiplexed address data bus mode, when an active low signal is present with CS signal high, internal registers will be accessed. In the Non-Multiplexed address data mode, this signal acts as the DS signal. A high on R/$\overline{W}$, with the CS and DS signals asserted, indicates a read operation. A low on the R/$\overline{W}$ signal, with the DS and the CS symbols asserted, indicates a write operation to the internal registers. Note: DS is active high in multiplexed mode, active low in non-multiplexed.

NAME	TYPE	DESCRIPTION
$\overline{DINT}/\overline{INT}$	O, OD	INTERRUPT. This signal is an interrupt line to the microprocesor. It is the combined interrupt line of the disk side and host side interrupts when pin READY/$\overline{AINT}$ is programmed as ready; otherwise, it only signals the occurrence of disk side interrupt events. This signal is programmable for either a push-pull or open-drain output circuit. This signal powers up as an open drain output. May be programmed as active high or low; reset state is active low.
AD(7:0)	I/O	ADDRESS/DATA BUS. When configured in the Multiplexed address data mode, these lines are multiplexed, bidirectional data path to the microprocessor. During the beginning of the memory cycle the bus captures the low order byte of the microprocessor address. These lines provide communication with the controller device's internal registers and the buffer memory. When configured in the Non-Multiplexed Microprocessors mode, these lines are bidirectional data lines only.
MA(7:0)	I/O	MICROPROCESSOR ADDRESS BUS. This 8-bit output bus is the AD(7:0) bus latched by the ALE pin during the address phase of a Multiplexed address data type microprocessor cycle. These signals are the address input when used with a non-multiplexed bus microprocessor.
READY/$\overline{AINT}$	O, OD	READY/HOST SIDE INTERRUPT. When programmed as the Ready function, this signal is deasserted low for the microprocessor to insert wait states to allow time for the chip to respond to the access. When programmed as the host side interrupt, this pin interrupts the microprocessor when there is a host related interrupt event. The interrupt signal is programmable for either a push-pull or open-drain output circuit. This signal powers up as the 'Ready' function.

DISK FORMATTER INTERFACE

INDEX	I	INDEX. This pin serves as the index function for the disk sequencer.
INPUT	I	INPUT. This signal is used to synchronize the disk sequencer to an external event.
INPUT2 (FAULT)	I	INPUT2. This pin is an input to the sequencer for tracking operations or can be used as a fault function to stop the sequencer.
OUTPUT	O	DISK SEQUENCER OUTPUT. This pin is controlled by bit 2 of the Control Field of the disk sequencer.
$\overline{AMD}$/SECTOR	I/O	ADDRESS MARK DETECT/SECTOR. In Hard Sector mode, this is the input for the sector pulse from the disk drive. In Soft Sector mode, a low-level input during a read indicates an address mark was detected.
RG	O	READ GATE. This active high output enables the reading of the disk. It is asserted by the sequencer Control Field bits 5 and 6. It is automatically deasserted at the end of the CRC or ECC.
WG	O	WRITE GATE. This active high output enables writing onto the disk. It is asserted and deasserted by the sequencer Control Field bits 5 and 6.
RRCLK	I	READ/REFERENCE CLOCK. This pin is used in conjunction with the NRZ pin to clock data in and out of the SSI 32C9001 device. This input must be glitch-free to ensure correct operation of the chip.

PIN DESCRIPTION (continued)

DISK FORMATTER INTERFACE (continued)

NAME	TYPE	DESCRIPTION
WCLK	O	WRITE CLOCK. This signal clocks the NRZ data out
NRZ0	I/O	NRZ BIT 0. This signal is the read data input from the disk drive when the read gate signal is asserted; it is the write data output to the disk drive when the srite gate signal is asserted. This pin is used for the least significant bit in dual bit NRZ mode; it is used for the serial data stream in single bit NRZ mode.
NRZ1	I/O	NRZ BIT1. This signal is the read data input from the disk drive when the read gate signal is asserted; it is the write data output to the disk drive when the write gate signal is asserted. This pin is used for the most significant bit in dual bit NRZ mode; it is not used in single bit NRZ mode.

HOST INTERFACE PINS

WP/$\overline{\text{IOCS16}}$	O, OD	WRITE PROTECT OR 16-BIT DATA SELECT. This signal can be used for write protect or 16-bit transfer for PCMCIA common memory mode. In ATA mode it indicates a 16-bit transfer is active on the host busl.
R/$\overline{\text{BUSY}}$/IRQ	O, Z	READY/$\overline{\text{BUSY}}$/HOST INTERRUPT REQUEST. In PCMCIA mode, this pin is the Ready/$\overline{\text{BUSY}}$ signal when configured with a memory interface. In ATA mode, or in PCMCIA mode when configured with an I/O interface, this pin is the host interrupt request, and is asserted to indicate to the host that the controller needs attention. As an interrupt request, this pin is active high in ATA mode, but active low in PCMCIA mode. This pin is always driven in PCMCIA mode, but will be tri-stated when the drive is not selected or interrupts are not enabled in ATA mode. This pin is driven low while $\overline{\text{RST}}$ is asserted, and remains so until the interface mode (PCMCIA or ATA) is determined. If PCMCIA mode is selected after reset, the chip is configured with a memory interface, and this pin will reflect the status of the BUSY bit in the Drive Status Register.
A(8:0), A10	I	HOST ADDRESS LINES. The host address lines A(8:0) and A10 are used to access the various PC/AT control, status, and data registers.
A9/$\overline{\text{HCS1}}$	I	A9/$\overline{\text{HCS1}}$. This is a multiplexed input pin. When in PCMCIA mode, or when register 4CH, bit 3 is reset, this is host address line A9. When register 4CH, bit 3 is set in ATA mode, this is Host chip select 1 (active low).
$\overline{\text{HCE1}}$/$\overline{\text{HCS0}}$	I	HOST CHIP SELECT 0/CARD ENABLE 1. This signal when low, selects access to the control, status, and data registers. It is configured as $\overline{\text{HCS0}}$ in ATA mode, and as $\overline{\text{HCE1}}$ (card enable 1) in PCMCIA mode.
WAIT/IOCHRDY	O, Z	WAIT/I/O CHANNEL READY. This signal is asserted low to extend host transfer cycles when the controller is not ready to respond. This pin is always driven in PCMCIA mode, but will be tri-stated when a read or write is not in progress in ATA mode. This pin is tri-state while $\overline{\text{RST}}$ is asserted, and remains so until the interface mode (PCMCIA or ATA) is determined.

NAME	TYPE	DESCRIPTION
$\overline{\text{INPACK}}$/DREQ	O, Z	INPUT ACKNOWLEDGE/DMA REQUEST. In PCMCIA mode, this pin is configured as $\overline{\text{INPACK}}$, and is asserted when a valid address and chip select are present. In ATA mode, this pin is configured as the DMA request signal, and is used during DMA transfer between the host and the controller. In ATA mode, this pin is tri-stated when DMA transfers are not enabled. This pin is tri-state while $\overline{\text{RST}}$ is asserted, and remains so until the interface mode (PCMCIA or ATA) is determined.
$\overline{\text{REG}}$/$\overline{\text{DACK}}$	I	REGISTER SELECT AND I/O $\overline{\text{ENABLE}}$/DMA $\overline{\text{ACKNOWLEDGE}}$. In PCMCIA mode, this pin is configured as $\overline{\text{REG}}$, and selects the attribute memory space or I/O space when asserted. In ATA mode, this pin is configured as $\overline{\text{DACK}}$, and is used as the DMA acknowledge signal during DMA data transfers.
$\overline{\text{IOR}}$	I	I/O READ. Asserted by the host during a host I/O read operation. When asserted with a valid address and chip selects, status or data is enabled onto the host data bus.
$\overline{\text{IOW}}$	I	I/O WRITE. Asserted by the host during a host I/O write operation. When asserted with a valid address and chip selects, data from the host data bus is strobed into the controller.
HRESET/$\overline{\text{HRESET}}$	I	HOST RESET. This signal, when active, initializes the control/status registers and stops any command in process. It is active low in ATA mode, but active high in PCMCIA mode.
HDB(15:0)	I/O	HOST DATA BUS. This bus is used to transfer data and status between the host and the controller. These pins are not driven while $\overline{\text{RST}}$ is asserted, and remain so until the interface mode (PCMCIA or ATA) is determined.
$\overline{\text{HCE2}}$	I	CARD ENABLE 2. This signal, when low, selects access to the control, status, and data registers and may enable use of the upper half of the data bus. It is used only in PCMCIA mode.
$\overline{\text{HOE}}$/$\overline{\text{SELATA}}$	I	OUTPUT ENABLE/SELECT ATA MODE. To determine which host interface to use, this pin is sampled starting at least 8 µs after $\overline{\text{RST}}$ is deasserted, and continuing until at least 25 µs after $\overline{\text{RST}}$ is deasserted. If this pin is high at any time during this sampling period, the interface will immediately be configured for PCMCIA mode, and the sampling will end. If the pin remains low throughout the sampling period, the interface will be configured for ATA mode. Once in PCMCIA mode, this pin is configured as output enable ($\overline{\text{HOE}}$), and is asserted by the host during a common memory or attribute memory read. When asserted with a valid address and chip select, data is enabled onto the host data bus. In ATA mode, this signal is ignored.

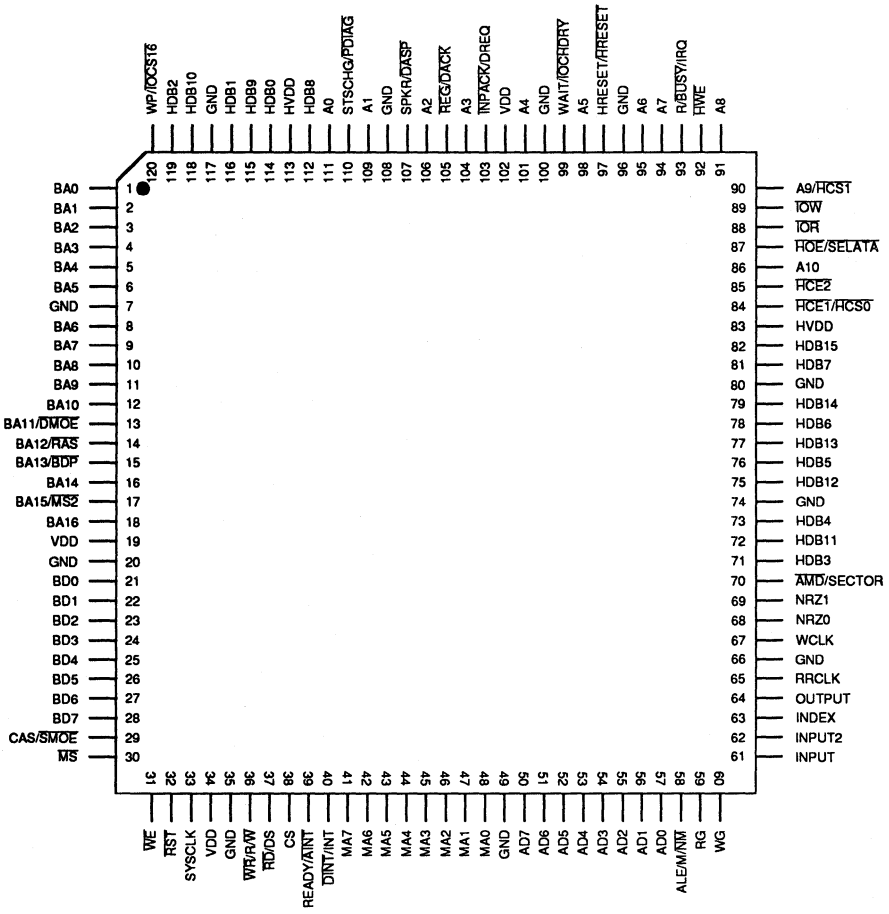
PIN DESCRIPTION (continued)

HOST INTERFACE PINS (continued)

NAME	TYPE	DESCRIPTION
$\overline{HWE}$	I	WRITE ENABLE. In PCMCIA mode, this signal is asserted by the host during a common memory or attribute memory write. When asserted with a valid address and chip select, data from the host data bus is strobed into the controller. In ATA mode, this signal is ignored.
$\overline{STSCHG}/PDIAG$	I, O	STATUS CHANGED/PASSED DIAGNOSTICS. In PCMCIA mode, this pin is used as the Status Changed output. In ATA mode, this pin is used as the Passed Diagnostics signal and may be an input or an open-drain output. This pin is tri-state while $\overline{RST}$ is asserted, and remains so until the interface mode (PCMCIA or ATA) is determined.
$\overline{SPKR}/\overline{DASP}$	I/OD	SPEAKER/DRIVE ACTIVE-SLAVE PRESENT. In PCMCIA mode, this pin is used as the Speaker pin, and is a push-pull output. In ATA mode, this pin is used as the Drive Active/Slave Present signal, and is an input or an open-drain output. In ATA mode, this pin is used for Master/Slave drive communications and/or for driving an LED. This pin is tri-state while $\overline{RST}$ is asserted, and remains so until the interface mode (PCMCIA or ATA) is determined.

PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



120-Lead TQFP

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX: (714) 573-6914

Notes:

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SSI 32C9600
ATA-2 Storage Controller
160 Mbit/s, 8-Bit NRZ Interface
Target Specification

January 1994

DESCRIPTION

The SSI 32C9600 is an advanced CMOS VLSI device which integrates major portions of the hardware needed to build an ATA disk drive. The SSI 32C9600 has an eight bit wide NRZ channel interface with disk transfers rates up to 160 Megabits per second, an advanced ATA interface which supports host transfer rates up to 20 megabytes per second, and a sixteen bit wide data buffer interface capable of supporting concurrent full speed transfers on both disk and host interfaces. The circuitry of the SSI 32C9600 includes: a complete, highly automated ATA interface; an advanced, fully integrated Buffer Manager; a high performance Disk Formatter; and two fast Reed-Solomon ECC's, one for the header field and a second for the data field, both with on-the-fly hardware correction. The SSI 32C9600 maximizes performance while minimizing microcontroller intervention.

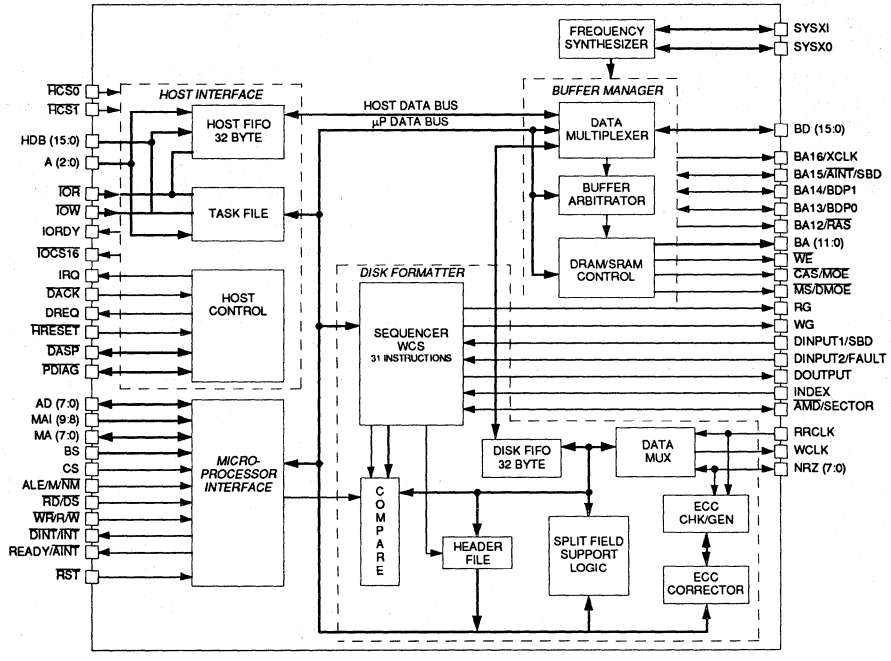
(continued)

FEATURES

- **ATA Interface**
  - **Single chip PC AT controller (IDE)**
  - **Full ANSI ATA-1 and ATA-2 compliance**
  - **Direct PC bus connection with on-board 12 mA drivers**
  - **PC transfers to 10 megawords (20 megabytes) per second**
  - **Supports PIO, DMA and Multiword DMA (EISA Class B Demand DMA)**
  - **Logic for daisy chaining 2 drives**
  - **Operates as Master, Slave or both**
  - **Automatic command decoding of Write, Write Long, Write Multiple, Write DMA, Write Buffer and Format commands.**

(continued)

BLOCK DIAGRAM



SSI 32C9600
ATA-2 Storage Controller
160 Mbit/s, 8-Bit NRZ Interface

DESCRIPTION (continued)

The SSI 32C9600 also supports dual bit NRZ interfaces. In dual bit mode, transfer rates up to 100 megabits per second on the disk interface are supported.

The highly automated Header ECC logic performs corrections on the header within one or two byte times, and Data ECC is capable of performing corrections in real time, allowing the SSI 32C9600 to read every sector on the disk in a single revolution even if every sector contained a correctable error.

The SSI 32C9600 is the latest in a line of sophisticated disk storage controllers. Other Silicon Systems' disk storage controllers include: the SSI 32C9800 SCSI-3 controller, with host transfer rates up to 20 megabytes per second and disk data rates of up to 160 megabits per second. The SSI 32C9001, SSI 32C9301, SSI 32C9302 and SSI 32C9003 ATA controllers provide dual and serial NRZ data rates to 80 Megabits per second and ATA speeds to 13.3 megabytes per second. The SSI 32C9020, SSI 32C9022, SSI 32C9023 and SSI 32C9024 family members are SCSI disk controllers supporting fast, 8-bit wide SCSI interface, with disk data rates to 80 Megabits per second. The SSI 32C9340 disk controller completes the family providing PCMCIA/ATA compliant interfaces. All members are based on a common architecture allowing major portions of firmware to be reused. The Silicon Systems' chip family is illustrated in the hierarchy chart shown in Figure 1.

The high level of integration within the SSI 32C9600 represents a major reduction in parts count. When the SSI 32C9600 ATA Controller is combined with the SSI 32R1510BR or SSI 32R2110R Read/Write device, the SSI 32P4782 Read Channel (1,7) or SSI 32P4901 PRML Read Channel (8/9), the 32H4631 Servo and Motor Speed Controller, an appropriate microcontroller and memory, a complete, cost efficient, high performance intelligent drive solution is created.

FEATURES (continued)

- Hardware support for Read Multiple and Write Multiple commands
- Hardware support for Cyl/Hd/Sec and LBA addressing modes, including automatic updates of the host task file registers in both modes
- Automatic Multi-Sector data transfers without microprocessor intervention
- Automatic Host Interrupt and Busy for multiple sector transfers
- 32 byte FIFO to improve performance
- Extensive Power Down modes

- Buffer Manager
  - Direct support of DRAM or SRAM
    - SRAM: up to 256k bytes of memory with throughput to 40 megabytes per second
    - DRAM: up to 8 megabyte of memory with throughput to 36 megabytes per second
  - Buffer CRC and/or buffer parity for increased data integrity
  - Programmable memory timing
  - Flexible buffer RAM segmentation
  - Dedicated host, disk and microprocessor address pointers
  - Buffer streaming with internal buffer protection circuit providing buffer integrity
- Disk Formatter
  - 8-Bit NRZ interface supporting data rates to 160 megabits per second, or
  - 2-Bit NRZ interface supporting data rates to 100 megabits per second
  - Automatic multi-sector transfers
  - Error tolerant sync detection
  - Header based split data field support
  - Advanced sequencer organized in 31 x 4 bytes
  - Timeouts for sync detection, sector or index pulse detection, and retry limiting
  - 144-bit Reed Solomon ECC for the data field, with "on-the-fly" fast hardware correction circuitry

  - Capable of correcting up to six 8-bit symbols in error
  - Guaranteed to correct a single 41-bit error burst, or two 17-bit error bursts
  - Fast hardware on-the-fly correction assures continuous data transfers even if consecutive sectors are in error
- 40-bit Reed Solomon ECC for the header field, with "on-the-fly" hardware correction circuitry which completes within 1 or 2 byte times
  - Guaranteed to correct a single 9-bit error burst

- Microprocessor Interface
  - Supports both multiplexed or non-multiplexed microprocessors
  - Separate host and disk interrupts
  - 1024 byte buffer window with wait stated or polled access
- Other Features
  - Frequency synthesizers for buffer clock
  - Internal Power Down mode
  - Available in 128-pin QFP or TQFP

FUNCTIONAL DESCRIPTION

The SSI 32C9600 contains the following four major functional blocks:

Microprocessor Interface
ATA Interface
Disk Formatter
Buffer Manager

The microprocessor interface allows the local microprocessor access to all of the SSI 32C9600 internal control registers and any location within the buffer memory. The microprocessor, by writing and reading the internal registers, can control all activities of the SSI 32C9600. The microprocessor can elect to perform host and/or disk operations directly, or it can enable the advanced features of the SSI 32C9600 which can perform these operations automatically.

The ATA Interface block handles all PC AT bus activities. The ATA interface includes 12 mA drivers allowing for direct connection of the SSI 32C9600 to the PC AT bus. The ATA interface block is highly automated, capable of performing multiple block transfers without micro-controller involvement. The ATA block interfaces directly with the Buffer Manager via an internal speed matching

(continued)

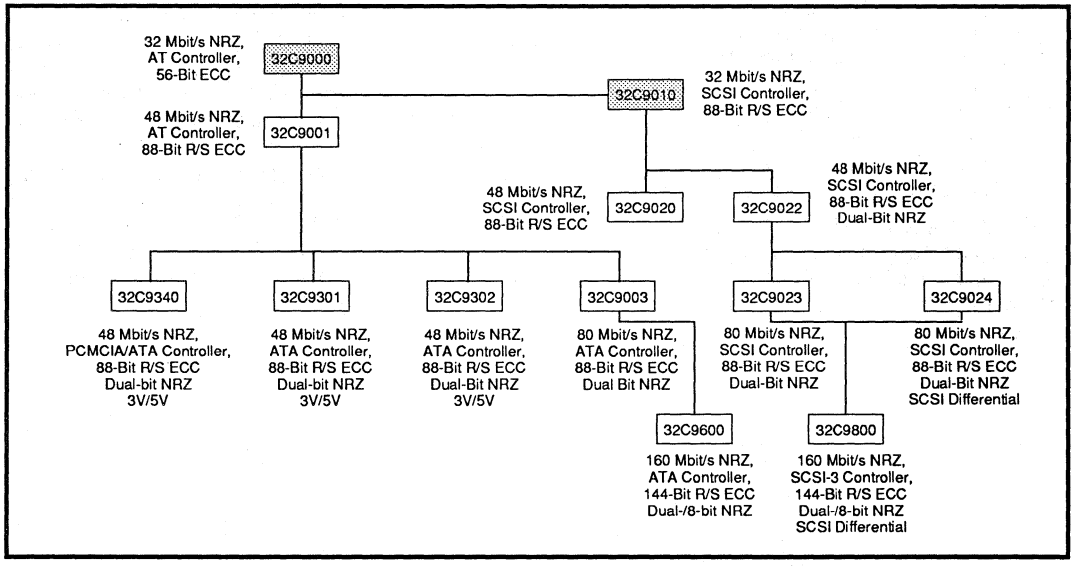


FIGURE 1: Silicon Systems' Disk Controller Chip Hierarchy

FUNCTIONAL DESCRIPTION (continued)

FIFO. This FIFO, the bandwidth capabilities of the Buffer Manager, plus the advanced features of the ATA Interface guarantee sustained full speed transfers across the PC AT bus.

The disk formatter performs the serialization and deserialization of data. It provides all of the necessary functions to control track formatting, header search, and the reading and writing of data. The heart of the disk formatter is an advanced programmable sequencer. The sequencer can contain 31 instructions, each of which is 4 bytes (32 bits) in width. The width of the instructions allows for sophisticated branching techniques which increase the flexibility and power of the sequencer. The flexible disk interface can be configured through a wide range of capabilities.

This allows the SSI 32C9600 to interface with many different read/write channels and allows the user of the SSI 32C9600 to select the read/write channel best suited to the device. Of course, by selecting the SSI 32C9600 controller and the SSI 32P4901 PRML read channel (8/9), you are guaranteed a problem free interface.

Within the disk formatter are the ECC generator/checker and ECC corrector. The generator/checker provides the ability to generate or check a 40-bit Reed-Solomon ECC for headers and a 144-bit Reed-Solomon code for data. The header ECC circuitry performs correction of the header bytes within one or two byte times, minimizing delays. The data ECC correction circuitry performs data corrections rapidly. The data ECC circuitry guarantees that the correction logic will always be available to correct the next sector if necessary.

The disk formatter provides additional reliability by use of error tolerant sync detection. This feature allows the creation of a multi-byte sync field and the detection of data synchronization even in the event of errors within the sync field.

The buffer manager manages the data buffer of the controller. The buffer manager can support either SRAM or DRAM. When configured to operate with DRAM, the buffer manager automatically performs necessary refresh cycles. The buffer manager creates all of the necessary timing and control signals for a wide range of memory types and speeds. Besides interfacing with the buffer memory, the buffer manager interfaces with the ATA Interface block, the disk formatter block, the ECC corrector and the microprocessor. If more than one of these blocks requires access to the buffer memory, the buffer manager arbitrates the requests automatically. The buffer manager of the SSI 32C9600 can sustain ATA operations at the rate of 10 megawords (20 megabytes) per second, disk formatter operations at 160 megabits per second and still has sufficient band-width left to handle on-the-fly ECC corrections and microprocessor accesses without degrading performance on any of the interfaces.

Besides the ability to generate and check data parity, the ATA interface also includes a CRC generation and checking capability. During writes, a CRC can be generated on data received from the host and checked when the data is transferred to the Disk Formatter. The CRC is part of the data ECC and is always written by the Disk Formatter. If the ATA interface generates the CRC, then the Disk formatter writes the CRC field that was generated by the ATA interface to the media, or the Disk Formatter generates the CRC itself. During reads the CRC is read from the media by the Disk Formatter. If buffer CRC is enabled, the Disk Formatter writes the CRC to the buffer and the CRC is re-checked by the ATA interface when the data is transferred to the host, or the Disk Formatter checks the CRC that is read from the media. The addition of CRC to the ATA interface adds a high degree of integrity, and detects most memory errors that may occur in the buffer memory.

PIN DESCRIPTION

The following convention is used in the pin description:

(I) denotes an input
(O) denotes an output
(I/O) denotes a bidirectional signal
(Z) denotes a tri-state output
(OD) denotes an open drain output

Active low signals are denoted by a bar on top of the signal name and dual function pins are denoted with a slash between the two signals — A9/$\overline{HCS1}$.

GENERAL

NAME	TYPE	DESCRIPTION
VDD	-	POWER SUPPLY PIN
GND	-	GROUND

HOST INTERFACE

A(2:0)	I	HOST ADDRESS LINES. The Host Address lines A(2:0) are used to access the various host control, status, and data registers.
$\overline{HCS1}$	I	HOST CHIP SELECT 1. This pin selects access to the control block task file registers.
$\overline{HCS0}$	I	HOST CHIP SELECT 0. This pin selects access to the command block task file registers.
$\overline{IOCS16}$	OD	16 BIT DATA TRANSFER. An open drain active low output that indicates that a 16-bit buffer transfer is active.
IRQ	O,Z	HOST INTERRUPT. Asserted active high to indicate to the Host that the controller needs attention.
IORDY	O,Z	I/O CHANNEL READY. This signal is asserted low to extend host transfer cycles when the controller is not ready to respond. This pin will be tristated when a read or write is not in progress.
DREQ	O,Z	DMA REQUEST. The active high DMA Request signal is used during DMA transfer between the Host and the controller.
$\overline{DACK}$	I	DMA ACKNOWLEDGE. This active low signal is used during DMA transfer between the host and the controller.
$\overline{IOR}$	I	I/O READ. This active low pin is asserted by the Host during a Host read operation. When asserted with $\overline{HCS0}$, $\overline{HCS1}$, or $\overline{DACK}$, data from the device is enabled onto the host data bus if the device is currently selected.
$\overline{IOW}$	I	I/O WRITE. Asserted active low by the HOST during a HOST write operation. When asserted with $\overline{HCS0}$, $\overline{HCS1}$, or $\overline{DACK}$, data from the host data bus is strobed into the device.

PIN DESCRIPTION (continued)

HOST INTERFACE (continued)

$\overline{\text{HRESET}}$	I	HOST RESET. This active low signal stops all commands in progress and initializes the control/status registers — This signal can also "wake up" the device while it is in power down mode.
HDB(15:0)	I/O	HOST DATA BUS. These bits are used for word transfers between the Buffer Memory and the Host; bits (7:0) are used for status, commands, or ECC byte transfers.
$\overline{\text{DASP}}$	I,OD	DRIVE ACTIVE/DRIVE 1 PRESENT. This is a time-multiplexed signal which indicates that a drive is active, or that Drive 1 is present.
$\overline{\text{PDIAG}}$	I,OD	PASSED DIAGNOSTICS. This signal is an output when configured as Drive 1 and an input when configured as Drive 0.

DISK INTERFACE

NAME	TYPE	DESCRIPTION
INDEX	I	INDEX. This pin serves as the index function for the disk sequencer. When the INPUT function is not available on the BA16 pin, this pin can function as input or index.
DOUTPUT	O	DISK SEQUENCER OUTPUT. This pin is controlled by bit 2 of the control field of the disk sequencer.
DINPUT1/SBD	I	DISK SEQUENCER INPUT 1: This pin may be used to synchronize the sequencer to an external event.
DINPUT2/FAULT	I	DISK SEQUENCER INPUT 2: This pin may be used to synchronize the sequencer to an external event, or as a write fault signal.
AMD/SECTOR	I	ADDRESS MARK DETECT/SECTOR. In Hard Sector mode, this is the input for the sector pulse from the disk drive. In Soft Sector mode, a low-level input during a read indicates an address mark was detected.
RG	O	READ GATE. This active high output enables the reading of the disk. It is asserted at the beginning of the PLO for header and data field by the sequencer. It is automatically deasserted at the end of the CRC or ECC.
WG	O	WRITE GATE. This active high output enables writing onto the disk. It is asserted and deasserted by the sequencer.
RRCLK	I	READ REFERENCE CLOCK. This pin is used in conjunction with the NRZs pin to clock data in. It is also used as a clock for the disk sequencer and is used to generate WCLK.
WCLK	O	WRITE CLOCK. This signal clocks the NRZ data out.
NRZ (7:0)	I/O	NON RETURN TO ZERO. These signals are the read data input 0 through 7 from the disk drive when the read gate signal is asserted; it is the write data output to the disk drive when the write gate signal is asserted. NRZ7 is the most significant bit.

MICROPROCESSOR INTERFACE

NAME	TYPE	DESCRIPTION
$\overline{RST}$	I	RESET. An asserted active low input generates a component reset that holds the internal registers of the controller at reset, stops all operations within the chip, and deasserts all output signals. All input/output signals and Host outputs are set to the high-Z state.
ALE/M/$\overline{NM}$	I	ADDRESS LATCH ENABLE/Multiplexed or Non-multiplexed address select: If this input is constantly low, the microprocessor interface is configured with non-multiplexed address and data busses. If this input is ever high, the microprocessor interface is configured with a multiplexed address and data bus. In this case, this pin functions as the address latch enable, and the latched address is output on the MA(7:0) pins.
CS	I	CHIP SELECT. This signal must be asserted high for all microprocessor accesses to the registers of this chip.
$\overline{WR}$/R/$\overline{W}$	I	WRITE STROBE/READ/WRITE. When the Intel bus control interface is selected, this signal acts as the $\overline{WR}$ signal. When the Write strobe signal is asserted low and the CS signal is asserted high, the data on the AD lines will be written to the register. When the Motorola bus control interface is selected, this signal acts as the R/$\overline{W}$ signal. A high on this input along with the $\overline{RD}$/$\overline{DS}$ signal asserted and the CS signal asserted high indicates a read operation. A low on this input along with the $\overline{RD}$/$\overline{DS}$ signal asserted and the CS signal asserted high indicates a write operation.
$\overline{RD}$/$\overline{DS}$	I	READ STROBE/DATA STROBE. When the Intel bus control interface is selected, this signal acts as the $\overline{RD}$ signal. When the read strobe signal is asserted low and the CS signal is asserted high, the data from the specified register will be driven onto the AD signals. When the Motorola bus control interface is selected, this signal acts as the $\overline{DS}$ signal. A high on the R/$\overline{W}$ signal along with this signal asserted and the CS signal asserted high indicates a read operation. A low on the R/$\overline{W}$ signal along with this signal asserted and the CS signal asserted high indicates a write operation.
$\overline{DINT}$/$\overline{INT}$	O, OD	DISK INTERRUPT. This signal is an interrupt line to the microprocessor. It is the combined interrupt line of the disk side and host side interrupts when pin READY/$\overline{AINT}$ is programmed as Ready; otherwise, it only signals the occurrence of disk side interrupt events. This signal is programmable for either a push-pull or open-drain output circuit. This signal powers up in the high-Z state.
AD(7:0)	I/O	ADDRESS/DATA BUS. When configured in the Multiplexed mode, these lines are multiplexed, bidirectional data path to the microprocessor. During the beginning of the memory cycle the bus captures the low order byte of the microprocessor address. These lines provide communication with the controller device's internal registers and the buffer memory. When configured in the Non-multiplexed mode, these lines are bidirectional data lines.

PIN DESCRIPTION (continued)

MICROPROCESSOR INTERFACE (continued)

NAME	TYPE	DESCRIPTION
MA(7:0)	I/O	MICROPROCESSOR ADDRESS BUS: This 8-bit output bus is the AD(7:0) bus latched by the ALE pin during the low order address phase of a Multiplexed type microprocessor cycle. These signals are non-multiplexed address input when used with a Non-multiplexed microprocessor.
MAI (9:8)	I	MICROPROCESSOR ADDRESS INPUTS: These signals are address input lines for bits 9 and 8 of the address. They are inputs regardless of whether multiplexed or non-multiplexed data and address busses are used. In the multiplexed mode, these bits are latched internally with the ALE signal; in the non-multiplexed mode, they are not latched.
READY/$\overline{\text{AINT}}$	O, OD	READY/HOST SIDE INTERRUPT: When programmed as the Ready function, this signal is deasserted low for the microprocessor to insert wait states to allow time for the chip to respond to the access. When programmed as the host side interrupt, this pin interrupts the microprocessor when there is a host related interrupt event. The interrupt signal is programmable for either a push-pull or open-drain output circuit. This signal powers up as the 'Ready' function.
BS	I	BUFFER WINDOW SELECT: This signal is asserted during microprocessor access of the buffer window.

BUFFER MANAGER INTERFACE

NAME	TYPE	DESCRIPTION
SYSXI	I	CRYSTAL INPUT/SYSTEM CLOCK: This is the crystal input to the buffer manager frequency synthesizer, or the clock input that is used to generate buffer memory access cycles when the frequency synthesizer is bypassed.
SYSXO	O	CRYSTAL OUTPUT.
$\overline{\text{CAS}}$/$\overline{\text{SMOE}}$	O	COLUMN ADDRESS STROBE/SRAM MEMORY OUTPUT ENABLE: This signal is used as the column address strobe in DRAM mode, or the memory output enable in SRAM mode. After $\overline{\text{RST}}$ is asserted, this signal will be high.
$\overline{\text{WE}}$	O	WRITE ENABLE: This signal is asserted low when a buffer memory write operation is active.
BD(15:0)	I/O	BUFFER MEMORY DATA BUS: These signals are bits 15-0 of the 16-bit parallel data lines to/from the buffer memory.
BA16/XCLK	O	BUFFER ADDRESS 16/SYNTHESIZER OUTPUT CLOCK: This signal is either the output of the frequency synthesizer, or buffer address 16. At reset, this signal is the equivalent of the signal at SYSXI (input clock to the frequency synthesizer.)
BA15/$\overline{\text{AINT}}$/SBD	I/O	BUFFER ADDRESS 15/AT INTERRUPT/SYNC BYTE DETECT: This signal may be used for addressing the buffer memory in SRAM mode, or as a separate local microprocessor interrupt for the host interface, or as a sync byte detect signal input for the disk formatter. After $\overline{\text{RST}}$ is asserted, this signal will be configured as SBD (i.e., as an input).

BUFFER MANAGER INTERFACE

NAME	TYPE	DESCRIPTION
BA14/BDP1	I/O	BUFFER MEMORY ADDRESS 14/BUFFER DATA PARITY 1: This signal is used for addressing the buffer memory in SRAM mode, or as the parity bit for BD(15:8) in DRAM mode.
BA13/BDP0	I/O	BUFFER MEMORY ADDRESS 13/BUFFER DATA PARITY 0: This signal is used for addressing the buffer memory in SRAM mode, or as the parity bit for BD (7:0) in DRAM mode.
BA12/$\overline{RAS}$	O	BUFFER MEMORY ADDRESS 12/ROW ADDRESS STROBE: This signal is used for addressing the buffer memory in SRAM mode, or as the row address strobe in DRAM mode. After $\overline{RST}$ is asserted, this signal will be high.
BA (11:0)	O	BUFFER MEMORY ADDRESS LINES: These are bits 11-0 for addressing the buffer memory.
$\overline{MS}$/$\overline{DMOE}$	O	MEMORY SELECT/DRAM MEMORY OUTPUT ENABLE: This pin is configured as memory select in SRAM mode, or as memory output enable in DRAM mode.

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Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914

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160 Mbit/s, 8-Bit NRZ Interface
Target Specification

December 1993

DESCRIPTION

The SSI SSI 32C9800 is an advanced CMOS VLSI device which integrates major portions of the hardware needed to build an SCSI disk drive. The SSI 32C9800 has an eight bit wide NRZ channel interface with disk transfers rates up to 160 Megabits per second, an advanced SCSI-3 interface which supports host transfer rates up to 20 megabytes per second, and a sixteen bit wide data buffer interface capable of supporting concurrent full speed transfers on both disk and host interfaces. The circuitry of the SSI SSI 32C9800 includes: a complete, highly automated SCSI interface; an advanced, fully integrated Buffer

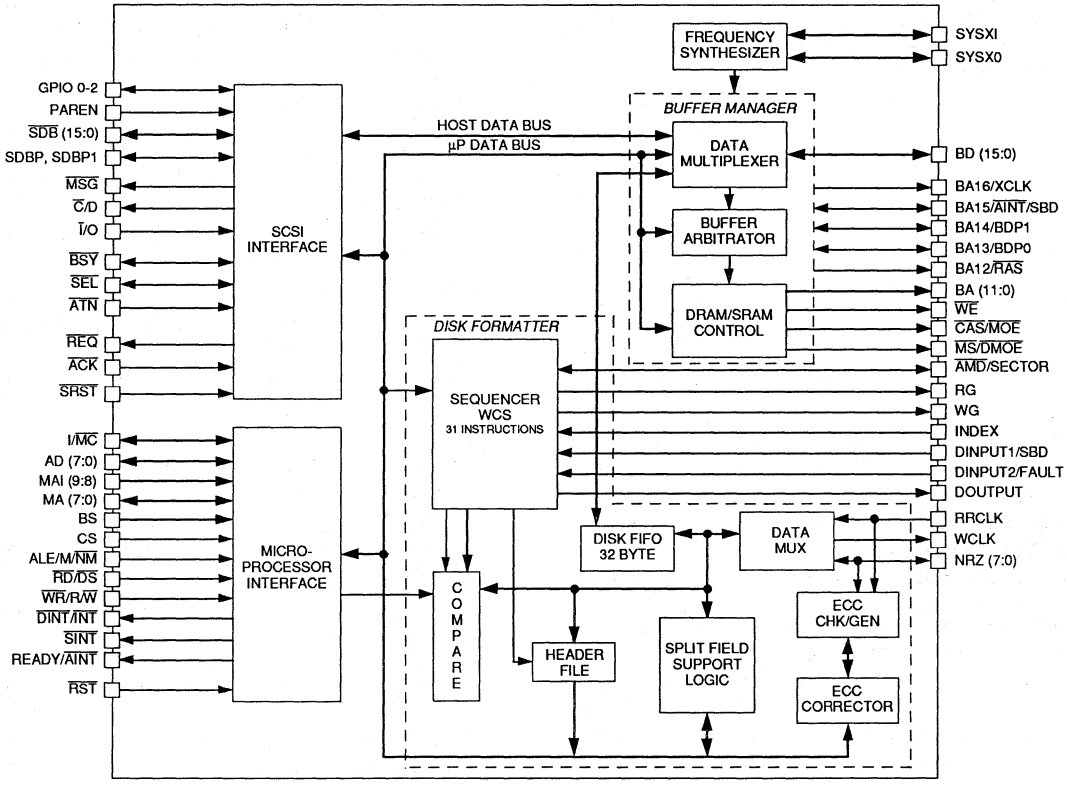
(continued)

FEATURES

- **SCSI Bus Interface**
  - **Full SCSI-2 and SCSI-3 compatibility**
  - **Direct bus interface logic with on-chip 48 mA SCSI tolerant drivers**
  - **Synchronous transfer rates up to 20 megabytes per second (fast and wide)**
  - **Asynchronous transfer rates up to 10 megabytes per second (wide)**
  - **Parity generation and checking**

(continued)

BLOCK DIAGRAM



SSI 32C9800
SCSI-3 Storage Controller
160 Mbit/s, 8-Bit NRZ Interface

DESCRIPTION (continued)

Manager; a high performance Disk Formatter; and two fast Reed-Solomon ECC's, one for the header field and a second for the data field, both with on-the-fly hardware correction. The SSI SSI 32C9800 maximizes performance while minimizing microcontroller intervention.

The SSI SSI 32C9800 also supports dual bit NRZ interfaces. In dual bit mode, transfer rates up to 100 megabits per second on the disk interface are supported.

The highly automated Header ECC logic performs corrections on the header within one or two byte times, and Data ECC is capable of performing corrections in real time, allowing the SSI 32C9800 to read every sector on the disk in a single revolution even if every sector contained a correctable error.

The SSI SSI 32C9800 is the latest in a line of sophisticated disk storage controllers. Other Silicon Systems' disk storage controllers include: the SSI 32C9600 ATA-2 controller, with host transfer rates up to 22 megabytes per second and disk data rates of up to 160 megabits per second. The SSI 32C9001, SSI 32C9301, SSI 32C9302 and SSI 32C9003 ATA controllers provide dual and serial NRZ data rates to 80 Megabits per second and ATA speeds to 13.3 megabytes per second. The SSI SSI 32C9020, SSI 32C9022, 32C9023 and SSI 32C9024 family members are SCSI disk controllers supporting fast, 8-bit wide SCSI interface, with disk data rates to 80 Megabits per second. The SSI SSI 32C9340 disk controller completes the family providing PCMCIA/ATA compliant interfaces. All members are based on a common architecture allowing major portions of firmware to be reused. The Silicon Systems' chip family is illustrated in the hierarchy chart shown in Figure 1.

The high level of integration within the SSI SSI 32C9800 represents a major reduction in parts count. When the SSI SSI 32C9800 SCSI Controller is combined with the SSI SSI 32R1510BR or SSI SSI 32R2110R Read/Write device, the SSI SSI 32P4782 Read Channel (1,7) or SSI 32P4901 PRML Read Channel (8/9), the SSI 32H4631 Servo and Motor Speed Controller, an appropriate microcontroller and memory, a complete, cost efficient, high performance intelligent drive solution is created.

FEATURES (continued)

- Auto Command Mode (ACM) SCSI state machine performs high level SCSI sequences without microprocessor intervention
- Four level ACM command FIFO supports automatic execution of multiple ACM commands
- Hardware support for automatic handling of command queuing
- Automatic SCSI CDB size determination
- Automatic SCSI disconnect and reconnect
- Thirty-two byte data FIFO between SCSI channel and Buffer Manager

• Buffer Manager
- Direct support of DRAM or SRAM
  - SRAM: up to 256k bytes of memory with throughput to 40 megabytes per second
  - DRAM: up to 8 megabyte of memory with throughput to 36 megabytes per second
- Buffer CRC or buffer parity for increased data integrity
- Programmable memory timing
- Flexible buffer RAM segmentation
- Dedicated host, disk and microprocessor address pointers
- Buffer streaming with internal buffer protection circuit providing buffer integrity

• Disk Formatter
- 8-Bit NRZ interface supporting data rates to 160 megabits per second, or
- 2-Bit NRZ interface supporting data rates to 100 megabits per second
- Automatic multi-sector transfers
- Error tolerant sync detection
- Header or microprocessor based split data field support
- Advanced sequencer organized in 31 x 4 bytes
- Timeouts for sync detection, sector or index pulse detection, and retry limiting
- 144-bit Reed Solomon ECC for the data field, with "on-the-fly" fast hardware correction circuitry
  - Capable of correcting up to six 8-bit symbols in error

  - Guaranteed to correct a single 41-bit error burst, or two 17-bit error bursts
  - Fast hardware on-the-fly correction assures continuous data transfers even if consecutive sectors are in error
- 40-bit Reed Solomon ECC for the header field, with "on-the-fly" hardware correction circuitry which completes within 1 or 2 bytes time
  - Guaranteed to correct a single 9-bit error burst

- Microprocessor Interface
  - Supports both multiplexed or non-multiplexed microprocessors
  - Separate host and disk interrupts
  - 1024 byte buffer window with wait states or pulled access
- Other Features
  - Internal power down mode
  - Frequency synthesizer for buffer clock
  - Available in 144 QFP or TQFP and 128 QFP or TQFP packages

FUNCTIONAL DESCRIPTION

The SSI 32C9800 contains the following four major functional blocks:

Microprocessor Interface
ATA Interface
Disk Formatter
Buffer Manager

The microprocessor interface allows the local microprocessor access to all of the SSI 32C9800 internal control registers and any location within the buffer memory. The microprocessor, by writing and reading the internal registers, can control all activities of the SSI 32C9800. The microprocessor can elect to perform host and/or disk operations directly, or it can enable the advanced features of the SSI 32C9800 which can perform these operations automatically.

The SCSI Interface block handles all SCSI activities. The SCSI interface includes 48 mA drivers allowing for direct connection of the SSI 32C9800 to the SCSI bus. In addition, the SCSI interface contains control signals for use with off-chip differential transcievers. The SCSI interface logic includes Auto Command Mode (ACM)

(continued)

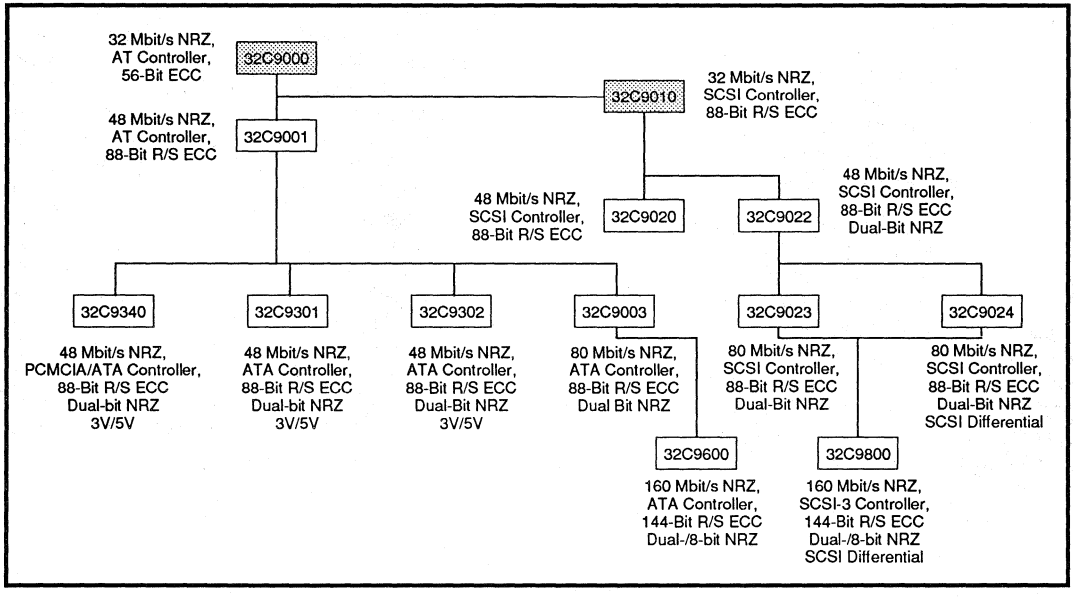


FIGURE 1: Silicon Systems' Disk Controller Chip Hierarchy

FUNCTIONAL DESCRIPTION (continued)

logic, an advanced state machine capable of handling a variety of complex SCSI sequences without microprocessor intervention. The microprocessor can queue up to four ACM commands into the ACM Command FIFO to create even more sophisticated command sequences. The SCSI block interfaces directly with the Buffer Manager via an internal speed matching FIFO. This FIFO, plus the bandwidth capabilities of the Buffer Manager guarantee sustained full speed transfers across the SCSI bus. The high level of automation of the ACM minimizes SCSI bus overhead. The net result is maximized performance with minimum SCSI bus band width utilization.

The disk formatter performs the serialization and deserialization of data. It provides all of the necessary functions to control track formatting, header search, and the reading and writing of data. The heart of the disk formatter is an advanced programmable sequencer. The sequencer can contain 31 instructions, each of which is 4 bytes (32 bits) in width. The width of the instructions allows for sophisticated branching techniques which increase the flexibility and power of the sequencer. The flexible disk interface can be configured through a wide range of capabilities. This allows the SSI 32C9800 to interface with many different read/write channels and allows the user of the SSI 32C9800 to select the read/write channel best suited to the device. Of course, by selecting the SSI 32C9800 controller and the SSI 32P4901 PRML read channel (8/9), you are guaranteed a problem free interface.

Within the disk formatter are the ECC generator/checker and ECC corrector. The generator/checker provides the ability to generate or check a 40-bit Reed-Solomon ECC for headers and a 144-bit Reed-Solomon code for data. The header ECC circuitry performs correction of the header bytes within one or two byte times, minimizing delays. The data ECC correction circuitry performs data corrections rapidly. The data ECC circuitry guarantees that the correction logic will always be available to correct the next sector if necessary.

The disk formatter provides additional reliability by use of error tolerant sync detection. This feature allows the creation of a multi-byte sync field and the detection of data synchronization even in the event of errors within the sync field.

The buffer manager manages the data buffer of the controller. The buffer manager can support either SRAM or DRAM. When configured to operate with DRAM, the buffer manager automatically performs necessary refresh cycles. The buffer manager creates all of the necessary timing and control signals for a wide range of memory types and speeds. Besides interfacing with the buffer memory, the buffer manager interfaces with the ATA Interface block, the disk formatter block, the ECC corrector and the microprocessor. If more than one of these devices requires access to the buffer memory, the buffer manager arbitrates the requests automatically. The buffer manager of the SSI 32C9800 can sustain SCSI operations at the rate of 10 megawords (20 megabytes) per second, disk formatter operations at 160 megabits per second and still has sufficient band-width left to handle on-the-fly ECC corrections and microprocessor accesses without degrading performance on any of the interfaces.

Besides the ability to generate and check data parity, the SCSI interface also includes a CRC generation and checking capability. During writes, a CRC can be generated on data received from the host and checked when the data is transferred to the Disk Formatter. The CRC is part of the data ECC and is always written by the Disk Formatter. If the SCSI interface generates the CRC, then the Disk Formatter writes the CRC field that was generated by the SCSI interface to the media, or the Disk Formatter generates the CRC itself. During reads, the CRC is read from the media ;by the Disk Formatter. If Buffer CRC is enabled, the Disk Formatter writes the CRC to the buffer and the CRC is re-checked by the SCSI interface when the data is transferred to the host, or the Disk Formatter checks the CRC that is read from the media. The addition of CRC to the SCSI interface adds a high degree of integrity, and detects most memory errors that may occur in the buffer memory.

PIN DESCRIPTION

The following convention is used in the pin description:

(I) denotes an input
(O) denotes an output
(Z) denotes a tri-state output
(OD) denotes an open drain output

GENERAL

NAME	TYPE	DESCRIPTION
VDD	-	POWER SUPPLY PIN
GND	-	GROUND

HOST INTERFACE

$\overline{SDBP}$, $\overline{SDBP1}$	I/O	SCSI DATA BUS PARITY. Odd parity bit for the SCSI data bus.
$\overline{SDB}$(15:0)	I/O	SCSI DATA BUS BITS 7-0.
$\overline{ATN}$	I	ATTENTION. This active low signal is used by the initiator to request a message out phase.
$\overline{BSY}$	I/O	BUSY. This active low signal is used to indicate when the bus is active.
$\overline{ACK}$	I	ACKNOWLEDGE. This active low signal is used in the handshake protocol to indicate the completion of a data byte transfer.
$\overline{SRST}$	I	SCSI RESET. This active low signal is used to reset the SCSI controller.
$\overline{MSG}$	O	MESSAGE. This active low signal is used to indicate a message phase.
$\overline{SEL}$	I/O	SELECT. This active low signal is used to indicate either a selection or reselection phase.
$\overline{C}$/D	O	COMMAND/DATA. This signal is used to indicate either a command or data phase.
$\overline{REQ}$	I	REQUEST. This active low signal is used in the handshake protocol to initiate a data byte transfer.
$\overline{I}$/O	I	INPUT/OUTPUT. This signal is used to indicate the direction of data transfer.
GPIO(2:0)	I/O	INPUT/OUTPUT. These pins are used to indicate the SCSI ID of the target device. The pins can be programmed as outputs for test purposes only.

DISK INTERFACE

INDEX	I	INDEX. This pin serves as the index function for the disk sequencer. When the INPUT function is not available on the BA16 pin, this pin can function as input or index.
DOUTPUT	O	DISK SEQUENCER OUTPUT. This pin is controlled by bit 2 of the control field of the disk sequencer.
DINPUT1/SBD	I	DISK SEQUENCER INPUT 1: This pin may be used to synchronize the sequencer to an external event.
DINPUT2/FAULT	I	DISK SEQUENCER INPUT 2: This pin may be used to synchronize the sequencer to an exteranl event, or as a write fault signal.

PIN DESCRIPTION (continued)

DISK INTERFACE (continued)

NAME	TYPE	DESCRIPTION
AMD/SECTOR	I	ADDRESS MARK DETECT/SECTOR. In Hard Sector mode, this is the input for the sector pulse from the disk drive. In Soft Sector mode, a low-level input during a read indicates an address mark was detected.
RG	O	READ GATE. This active high output enables the reading of the disk. It is asserted at the beginning of the PLO for header and data field by the sequencer. It is automatically deasserted at the end of the CRC or ECC.
WG	O	WRITE GATE. This active high output enables writing onto the disk. It is asserted and deasserted by the sequencer.
RRCLK	I	READ REFERENCE CLOCK. This pin is used in conjunction with the NRZs pin to clock data in. It is also used as a clock for the disk sequencer and is used to generate WCLK.
WCLK	O	WRITECLOCK. This signal clocks the NRZ data out.
NRZ (7:0)	I/O	NON RETURN TO ZERO. These signals are the read data input 0 through 7 from the disk drive when the read gate signal is asserted; it is the write data output to the disk drive when the write gate signal is asserted. NRZ7 is the most significant bit.

MICROPROCESSOR INTERFACE

NAME	TYPE	DESCRIPTION
$\overline{RST}$	I	RESET. An asserted active low input generates a component reset that holds the internal registers of the controller at reset, stops all operations within the chip, and deasserts all output signals. All input/output signals and Host outputs are set to the high-Z state.
ALE/M/$\overline{NM}$	I	ADDRESS LATCH ENABLE/Multiplexed or Non-multiplexed address select: If this input is constantly low, the microprocessor interface is configured with non-multiplexed address and data busses. If this input is ever high, the microprocessor interface is configured with a multiplexed address and data bus. In this case, this pin functions as the address latch enable, and the latched address is output on the MA(7:0) pins.
CS	I	CHIP SELECT. This signal must be asserted high for all microprocessor accesses to the registers of this chip.
$\overline{WR}$/R/$\overline{W}$	I	WRITE STROBE/READ/WRITE. When the Intel bus control interface is selected, this signal acts as the $\overline{WR}$ signal. When the Write strobe signal is asserted low and the CS signal is asserted high, the data on the AD lines will be written to the register. When the Motorola bus control interface is selected, this signal acts as the R/$\overline{W}$ signal. A high on this input along with the $\overline{RD}$/$\overline{DS}$ signal asserted and the CS signal asserted high indicates a read operation. A low on this input along with the $\overline{RD}$/$\overline{DS}$ signal asserted and the CS signal asserted high indicates a write operation.

MICROPROCESSOR INTERFACE (continued)

NAME	TYPE	DESCRIPTION
$\overline{RD}/\overline{DS}$	I	READ STROBE/DATA STROBE. When the Intel bus control interface is selected, this signal acts as the $\overline{RD}$ signal. When the read strobe signal is asserted low and the CS signal is asserted high, the data from the specified register will be driven onto the AD signals. When the Motorola bus control interface is selected, this signal acts as the $\overline{DS}$ signal. A high on the R/$\overline{W}$ signal along with this signal asserted and the CS signal asserted high indicates a read operation. A low on the R/$\overline{W}$ signal along with this signal asserted and the CS signal asserted high indicates a write operation.
$\overline{DINT}/\overline{INT}$	O, OD	DISK INTERRUPT. This signal is an interrupt line to the microprocessor. It is the combined interrupt line of the disk side and host side interrupts when pin RDY/$\overline{AINT}$ is programmed as Ready; otherwise, it only signals the occurrence of disk side interrupt events. This signal is programmable for either a push-pull or open-drain output circuit. This signal powers up in the high-Z state.
AD(7:0)	I/O	ADDRESS/DATA BUS. When configured in the Multiplexed mode, these lines are multiplexed, bidirectional data path to the microprocessor. During the beginning of the memory cycle the bus captures the low order byte of the microprocessor address. These lines provide communication with the controller device's internal registers and the buffer memory. When configured in the Non-multiplexed mode, these lines are bidirectional data lines.
MA(7:0)	I/O	MICROPROCESSOR ADDRESS BUS: This 8-bit output bus is the AD(7:0) bus latched by the ALE pin during the low order address phase of a Multiplexed type microprocessor cycle. These signals are non-multiplexed address input when used with a Non-multiplexed microprocessor.
MAI (9:8)	I	MICROPROCESSOR ADDRESS INPUTS: These signals are address input lines for bits 9 and 8 of the address. They are inputs regardless of whether multiplexed or non-multiplexed data and address busses are used. In the multiplexed mode, these bits are latched internally with the ALE signal; in the non-multiplexed mode, they are not latched.
RDY/AINT	O, OD	READY/HOST SIDE INTERRUPT: When programmed as the Ready function, this signal is deasserted low for the microprocessor to insert wait states to allow time for the chip to respond to the access. When programmed as the host side interrupt, this pin interrupts the microprocessor when there is a host related interrupt event. The interrupt signal is programmable for either a push-pull or open-drain output circuit. This signal powers up as the 'Ready' function.
BS	I	BUFFER WINDOW SELECT: This signal is asserted during microprocessor access of the buffer window.

PIN DESCRIPTION (continued)

BUFFER MANAGER INTERFACE

NAME	TYPE	DESCRIPTION
SYSXI	I	CRYSTAL INPUT/SYSTEM CLOCK: This is the crystal input to the buffer manager frequency synthesizer, or the clock input that is used to generate buffer memory access cycles when the frequency synthesizer is bypassed.
SYSXO	O	CRYSTAL OUTPUT.
$\overline{\text{CAS}}/\overline{\text{SMOE}}$	O	COLUMN ADDRESS STROBE/SRAM MEMORY OUTPUT ENABLE: This signal is used as the column address strobe in DRAM mode, or the memory output enable in SRAM mode. After $\overline{\text{RST}}$ is asserted, this signal will be high.
$\overline{\text{WE}}$	O	WRITE ENABLE: This signal is asserted low when a buffer memory write operation is active.
BD(15:0)	I/O	BUFFER MEMORY DATA BUS: These signals are bits 15-0 of the 16-bit parallel data lines to/from the buffer memory.
BA16/XCLK	O	BUFFER ADDRESS 16/SYNTHESIZER OUTPUT CLOCK: This signal is either the output of the frequency synthesizer, or buffer address 16. At reset, this signal is the equivalent of the signal at SYSXI (input clock to the frequency synthesizer.)
BA15/$\overline{\text{AINT}}$/SBD	I/O	BUFFER ADDRESS 15/AT INTERRUPT/SYNC BYTE DETECT: This signal may be used for addressing the buffer memory in SRAM mode, or as a separate local microprocessor interrupt for the host interface, or as a sync byte detect signal input for the disk formatter. After $\overline{\text{RST}}$ is asserted, this signal will be configured as SBD (i.e., as an input).
BA14/BDP1	I/O	BUFFER MEMORY ADDRESS 14/BUFFER DATA PARITY 1: This signal is used for addressing the buffer memory in SRAM mode, or as the parity bit for BD(15:8) in DRAM mode.
BA13/BDP0	I/O	BUFFER MEMORY ADDRESS 13/BUFFER DATA PARITY 0: This signal is used for addressing the buffer memory in SRAM mode, or as the parity bit for BD (7:0) in DRAM mode.
BA12/$\overline{\text{RAS}}$	O	BUFFER MEMORY ADDRESS 12/ROW ADDRESS STROBE: This signal is used for addressing the buffer memory in SRAM mode, or as the row address strobe in DRAM mode. After $\overline{\text{RST}}$ is asserted, this signal will be high.
BA (11:0)	O	BUFFER MEMORY ADDRESS LINES: These are bits 11-0 for addressing the buffer memory.
$\overline{\text{MS}}/\overline{\text{DMOE}}$	O	MEMORY SELECT/DRAM MEMORY OUTPUT ENABLE: This pin is configured as memory select in SRAM mode, or as memory output enable in DRAM mode.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914

Section 10

OPTICAL/FLOPPY CIRCUITS

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SSI 33P3700
8-48 Mbit/s Magneto Optical Read Channel
Target Specification

January 1994

DESCRIPTION

The SSI 33P3700 is a high performance BiCMOS single chip read channel IC that contains all the functions needed to implement a complete zoned recording read channel for magneto optical (MO) drive systems. Functional blocks include a sum and difference amplifier, input attenuator, pulse detector, programmable filter, time base generator, and data synchronizer. MO data rates from 8 to 48 Mbit/s for 1,7 code or 6 to 36 Mbit/s for 2,7 code can be programmed using an internal DAC whose reference current is set by a single external resistor.

Programmable functions of the SSI 33P3700 device are controlled through a bidirectional serial port and banks of internal registers. This allows zoned recording applications to be supported without changing external component values from zone to zone.

The SSI 33P3700 utilizes an advanced BiCMOS process technology along with advanced circuit design techniques which result in a high performance device with low power consumption.

FEATURES

GENERAL
- Programmable MO/EMBOSS data rates of 8 to 48 Mbit/s (1,7 RLL), or 6 to 36 Mbit/s (2,7 RLL) internal DAC controlled
- Complete zoned recording application support
- Low power operation (TBD mW typical @ 5V)
- Bidirectional serial port register access
- Register programmable power management (Sleep mode < TBD mW)
- Power supply range (4.5 to 5.5 V)
- Small footprint 64-lead TQFP package

PULSE DETECTOR
- Provides head amplifier difference for MO signals and sum for emboss signals
- Dual programmable attenuator (x 1/16 min, 4 bit resolution) for emboss and MO data with Low-Z switch and internal multiplexer
- Fast Attack/Decay modes for rapid AGC recovery
- Dual rate charge pump for fast transient recovery
- Low drift AGC hold circuitry
- Temperature compensated, exponential control AGC
- Wide bandwidth, high precision full-wave rectifier
- Programmable LEVEL pin time constant with separate MO and emboss
- Optimized pulse qualification circuitry for pit mark recording with input clamp circuit
- Internal fast decay timing
- External Low-Z control pin
- 0.5 ns maximum pulse pairing with sine wave input

PROGRAMMABLE FILTER
- Programmable cutoff frequency of 4 to 24 MHz
- Programmable boost/equalization of 0 to 13 dB
- Matched normal and differentiated outputs
- ±20% Fc accuracy (Fc = 4 to 8 MHz)
- ±15% Fc accuracy (Fc = 8 to 24 MHz)
- ±3% maximum group delay variation
- Less than 1.5% total harmonic distortion
- Low-Z input switch controlled by $\overline{\text{LOW\_Z}}$ pin
- No external filter components required

TIME BASE GENERATOR
- Better than 1% frequency resolution
- Up to 75 MHz frequency output
- Independent divide by M and N registers
- VCO center frequency matched to data synchronizer VCO
- VCO (FOUT) output available in all modes but power down

DATA SYNCHRONIZER
- Fast acquisition phase lock loop with zero phase restart technique
- Fully integrated data synchronizer — no external delay lines, active devices, or active PLL components
- Programmable decode window symmetry control via serial port
  - Window shift control ±30% (4-bit)
  - Includes delayed read MO/emboss data and VCO clock monitor points
- Separate qualifier output (RDO) and data separator input (RDI)

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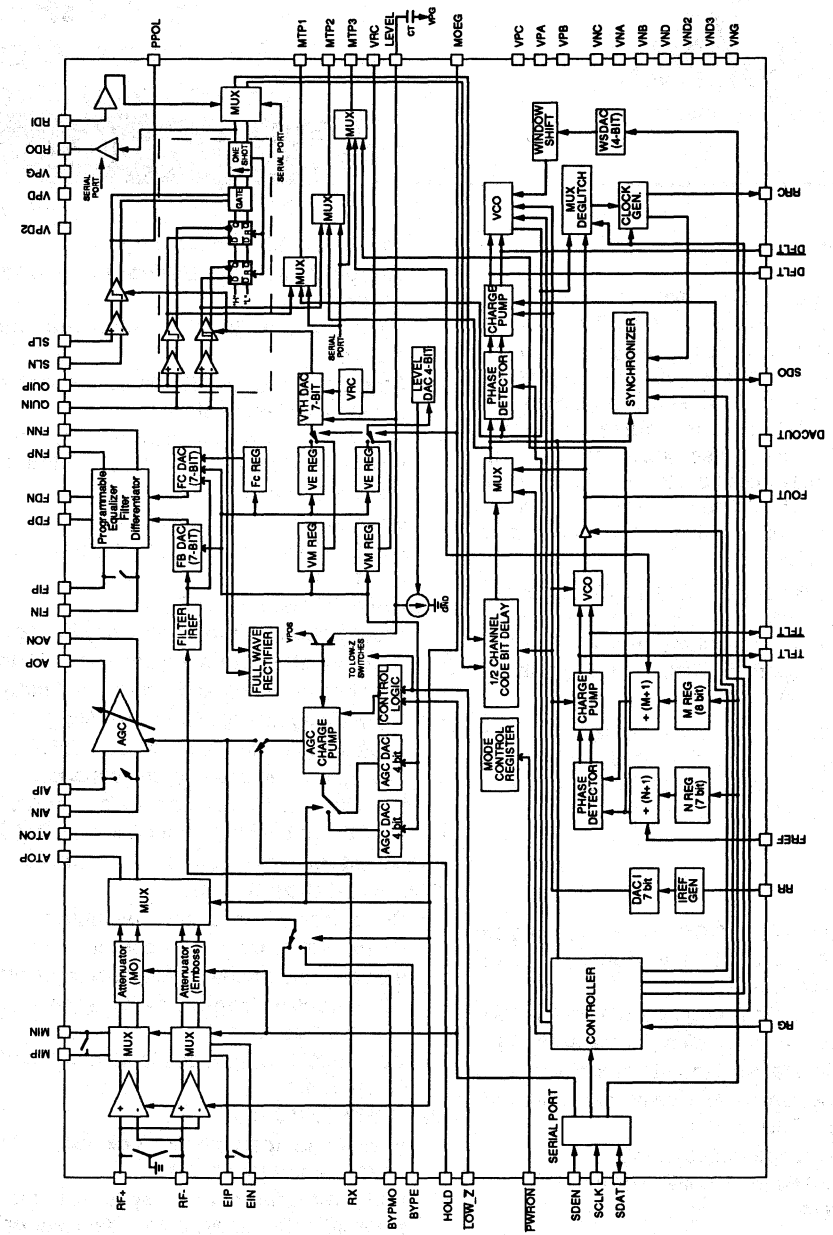

BLOCK DIAGRAM

CAUTION: Use handling procedures necessary for a static sensitive component.

Target Specification: The target specification is intended as an initial disclosure of specification goals for the product. The specifications are based on design goals, subject to change and are not guaranteed.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914

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SSI 33P3733A
8-26.5 Mbit/s Read Channel w/Pit Mark Pulse Qualifier
Preliminary Data

December 1993

DESCRIPTION

The SSI 33P3733A device is a high performance BiCMOS single chip read channel IC that contains all the functions needed to implement a complete zoned recording read channel for magneto-optical (MO) drive systems. Functional blocks include the pulse detector, programmable filter, time base generator, and data synchronizer. MO data rates from 8 to 26.5 Mbit/s for (1,7) code, 6 to 20 Mbit/s for (2,7) code can be programmed using an internal DAC whose reference current is set by a single external resistor.

Programmable functions of the SSI 33P3733A device are controlled through a bi-directional serial port and banks of internal registers. This allows zoned recording applications to be supported without changing external component values from zone to zone.

The SSI 33P3733A utilizes an advanced BiCMOS process technology along with advanced circuit design techniques which result in a high performance device with low power consumption.

FEATURES

- **Programmable MO data rate of 8 to 26.5 Mbit/s for (1,7) code, 6 to 20 Mbit/s for (2,7) code, internal DAC controlled**
- **Complete zoned recording application support**
- **Low-power operation (375 mW typical @ 5V)**
- **Bi-directional serial port for register access**
- **Register programmable power management (Sleep mode <5 mW)**
- **Power supply range (4.5 to 5.5 volts)**
- **Small footprint 64-lead TQFP package**

PULSE DETECTOR

- **Fast Attack/Decay modes for rapid AGC recovery**
- **Dual rate charge pump for fast transient recovery**
- **Low Drift AGC hold circuitry**
- **Temperature compensated, exponential control AGC**
- **Wide bandwidth, high precision full-wave rectifier**
- **Programmable LEVEL pin time constant with separate MO data and emboss registers**
- **Separate Read and emboss AGC levels (4-bit DAC)**
- **Pulse qualification circuitry is provided for Pit Mark detection**
- **Internal fast decay timing**
- **External $\overline{\text{LOW\_Z}}$ control pin**
- **0.5 ns max. pulse pairing with sine wave input**

PROGRAMMABLE FILTER

- **Programmable cutoff frequency of 4 to 12 MHz**
- **Programmable boost/equalization of 0 to 13 dB**
- **Matched normal and differentiated outputs**
- **± 10 to 15% *fc* accuracy**
- **± 2% maximum group delay variation**
- **Less than 1.5% total harmonic distortion**
- **Low-Z input switch controlled by $\overline{\text{LOW\_Z}}$ pin**
- **No external filter components required**

TIME BASE GENERATOR

- **Better than 1% frequency resolution**
- **Up to 75 MHz frequency output**
- **Independent divide-by M and N registers**
- **VCO center frequency matched to data synchronizer VCO**
- **VCO (FOUT) output available independent of the mode**

DATA SEPARATOR

- **Fast acquisition phase lock loop with zero phase restart technique**
- **Fully integrated data separator**
  - **No external delay lines, active devices, or active PLL components required**
- **Programmable decode window symmetry control via serial port**
  - **Window shift control ± 30% (4-bit)**
  - **Includes delayed read MO data and VCO clock monitor points**

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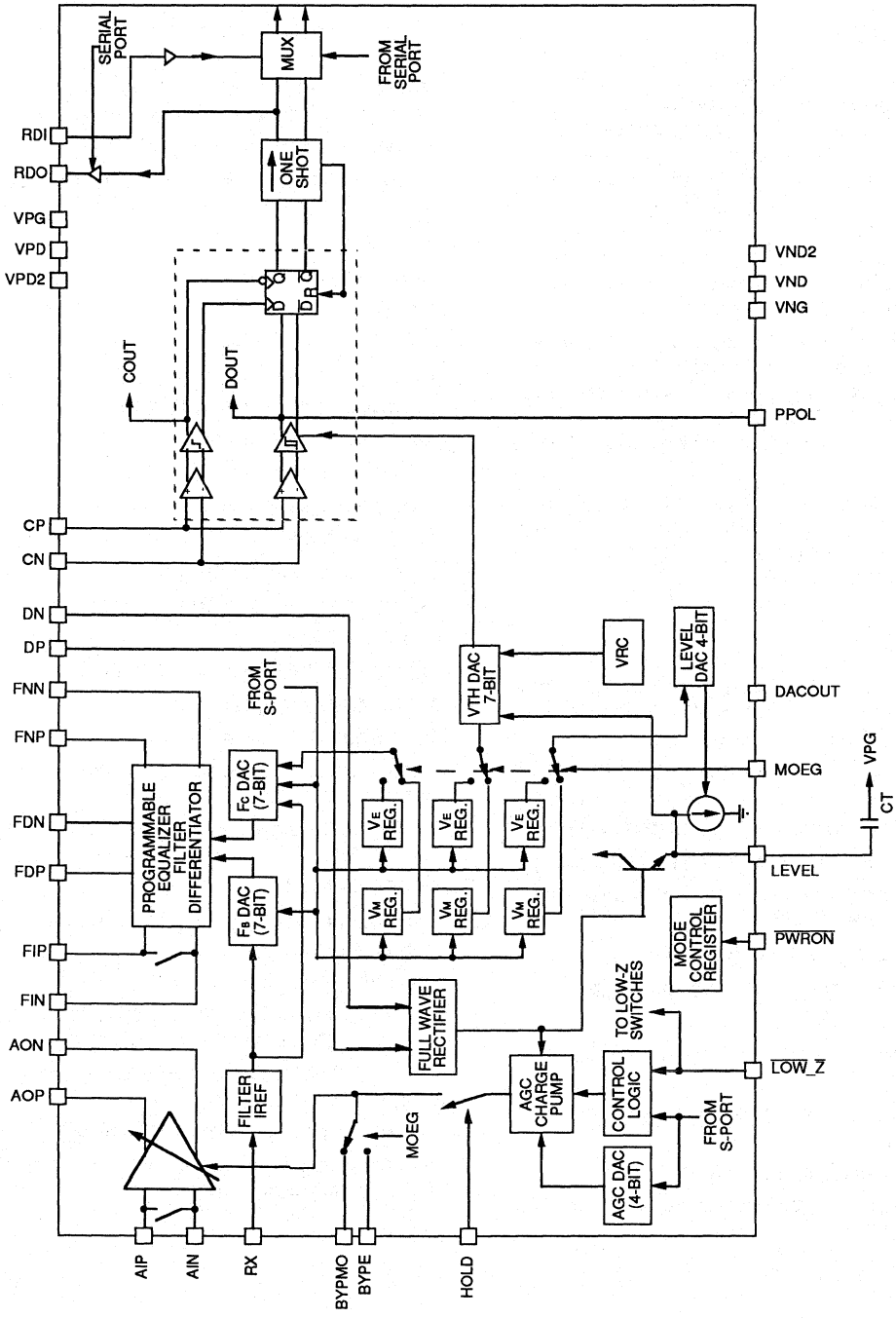

FIGURE 1A: Block Diagram, Front End

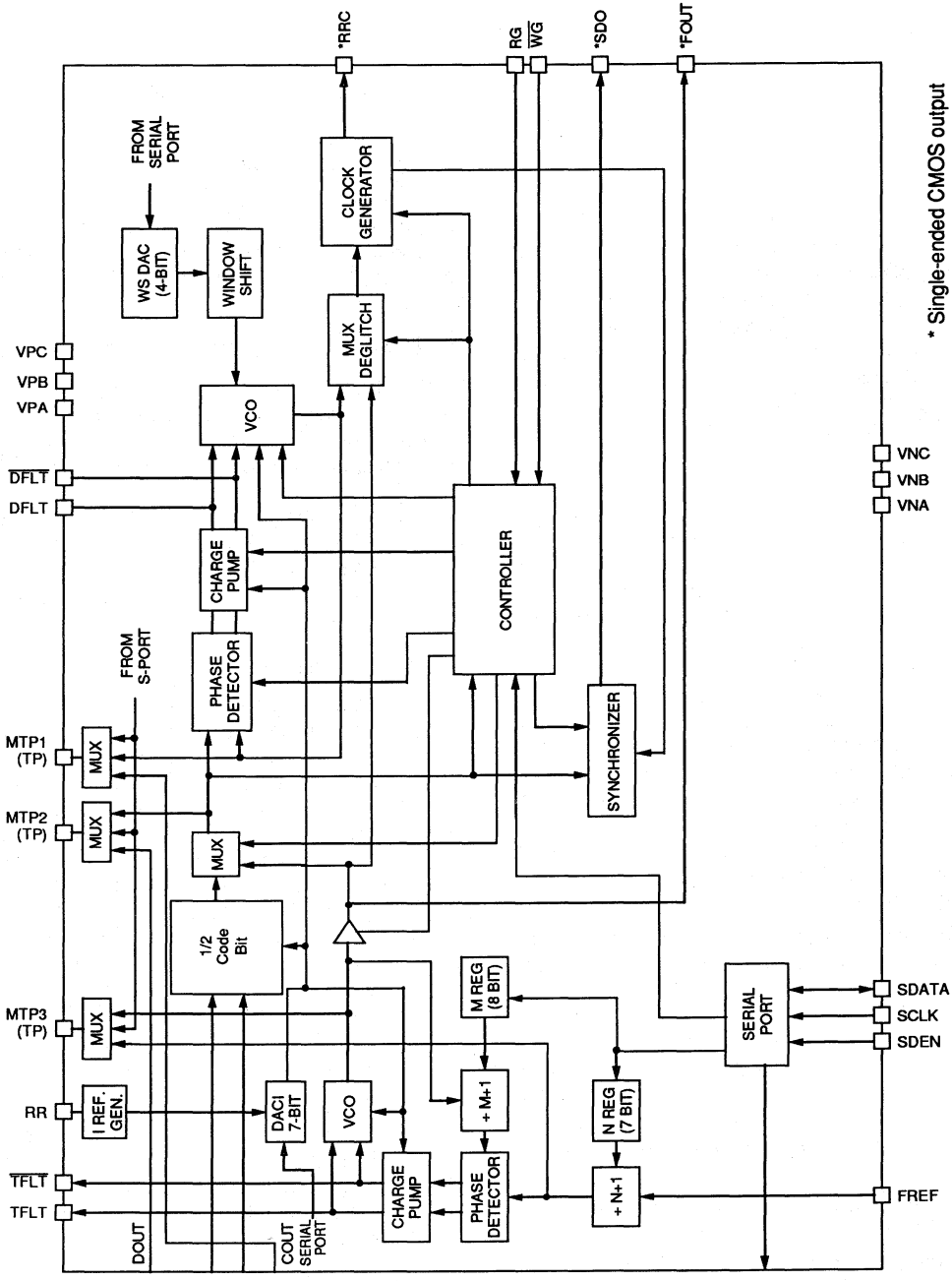

FIGURE 1B: Block Diagram, Back End

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FUNCTIONAL DESCRIPTION

The SSI 33P3733A implements a high performance complete read channel, including pulse detector, programmable active filter, time base generator, and data synchronizer, at MO data rates up to 26.5 Mbit/s for (1,7) code, 20 Mbit/s for (2,7) code. A circuit block diagram is shown in Figure 1.

PULSE DETECTOR CIRCUIT DESCRIPTION

The pulse detector, in conjunction with the programmable filter, provides all the MO data processing functions necessary for detection and qualification of encoded read signals. The signal processing circuits include a wide bandwidth variable gain amplifier, a precision wide bandwidth fullwave rectifier, and a dual rate charge pump. The entire signal path is fully-differential to minimize external noise pick up.

AGC CIRCUIT

The gain of the AGC amplifier is controlled by the voltage (V_{BYPx}) stored on the BYPx hold capacitor (C_{BYPx}). A dual rate charge pump drives C_{BYPx} with currents that depend on the instantaneous differential voltage at the DP/DN pins. Attack currents lower V_{BYPx} which reduces the amplifier gain, while decay currents increase V_{BYPx} which increases the amplifier gain. When the signal at DP/DN is greater than 100% of the programmed AGC level, the nominal attack current of 0.18 mA is used to reduce the amplifier gain. If the signal is greater than 125% of the programmed AGC level, a fast attack current of eight (8) times nominal is used to reduce the gain. This dual rate approach allows AGC gain to be quickly decreased when it is too high/low yet minimizes distortion when the proper AGC level has been acquired.

A constant decay current of 4 µA acts to increases the amplifier gain when the signal at DP/DN is less than the programmed AGC level. The large ratio (0.18 mA:4 µA) of the nominal attack and nominal decay currents enable the AGC loop to respond to the peak amplitudes of the incoming read signal rather than the average value. A Fast Decay Current mode is provided to allow the AGC gain to be rapidly increased, if required. In Fast Decay mode, the decay current is increased by a factor of 21.

In Read mode and Write mode, the reference voltage for the AGC charge pump is a nominal 1.0V. When MOEG is high, the reference voltage for the AGC charge pump is set by a 4-bit DAC (DACA) controlled by the serial port. The DAC output voltage is offset so that "1111" results in a 0.75V output, and "0000" results in a 1.00V output:

$$V_{AGC} = 1.00 - (DACA \times 0.01667)\ Vpp$$

where DACA is the decimal value of the DACA register

When the chip is in Power Down mode, the AGC dual rate charge pump is disabled.

Upon power up, the Low-Z/fast decay sequence should be executed to rapidly recover from any transients or drift which may have occurred on the BYPx hold capacitors.

BYPMO AND BYPE CONTROL VOLTAGE

The BYPMO capacitor voltage will be held constant (subject to leakage currents) during Sleep mode, Emboss mode (MOEG = high), Write mode, or when the HOLD signal is high. Upon the transition of $\overline{PWRON}$ from high to low, there is a 1 µs delay inserted before the AGC charge pump is allowed to drive the BYPMO capacitor. When MOEG is high, the charge pump drives the BYPE capacitor. When MOEG is low, the BYPE capacitor voltage will be held constant (subject to leakage currents).

AGC MODE CONTROL

When write gate ($\overline{WG}$) is driven low, the dual rate charge pump is disabled causing the AGC amplifier gain to be held constant. When the WG pin transitions from low to high, the LOW_Z mode can be entered using the $\overline{LOW\_Z}$ control pin. When this pin is brought low, the input impedance at both the AGC amplifier and the programmable filter are reduced to allow for quick recovery of the AC coupling capacitors. When the $\overline{LOW\_Z}$ pin goes high, the Fast Decay mode is triggered allowing rapid acquisition of the proper AGC level. The duration of the Fast Decay mode is internally set at a nominal 1 µs. Fast Decay mode is also triggered by a transition of the MO/emboss gate (MOEG) pin in either direction. When the pulse detector is powered-down, V_{BYPx} will be held constant subject to leakage currents only.

External control for enabling the dual rate charge pump is also provided. Driving the HOLD pin high forces the dual rate charge pump output current to zero. In this mode, V_{BYPx} will be held constant subject to leakage currents only.

RDO OUTPUT PIN

A CMOS compatible, 6 ns wide (min), Raw Data Output (RDO) signal is provided. This pin will be held low when either RG is high or WG is low to reduce noise and accompanying jitter during Read or Write modes. This pin is also controlled by CBR bit 2 (RDI/O register bit). When CBR bit 2 goes high, RDO will be held High-Z.

RDI INPUT PIN

A TTL compatible pin read data input (RDI) is provided as a read data input to the data synchronizer from an external qualification circuit. RDI is available when CBR bit 2 (RDI/O register bit) goes high.

HYSTERESIS COMPARATOR QUALIFICATION

The SSI 33P3733A provides a hysteresis comparator pulse qualification circuit for Pit Mark detection. This circuit uses only the differentiated signal for qualification. The differentiated signal is connected to both the hysteresis and zero cross comparators. A positive peak that clears the established threshold level will set the hysteresis comparator. A peak of the opposite polarity must clear the negative threshold level to reset the hysteresis comparator. A positive edge of the hysteresis comparator output sets the D-Flip-Flop Q high. This in turn feeds into the D-input of the second D-Flip-Flop which is triggered by the negative edge of the zero cross comparator output. This output triggers the one-shot. Timing for the hysteresis comparator is shown in Figure 2.

PROGRAMMABLE FILTER CIRCUIT DESCRIPTION

The SSI 33P3733A programmable filter consists of an electronically controlled low-pass filter with a separate differentiated low-pass output. A seven-pole, low-pass filter is provided along with a single-pole, single-zero differentiator. Both outputs have matched delays. The delay matching is unaffected by any amount of programmed equalization or bandwidth. Programmable bandwidth and boost/equalization is provided by internal 7-bit control DACs. The programmable characteristics are automatically switched during Emboss mode to improve signal to noise ratio. Differentiation pulse slimming equalization is accomplished by a two-pole, low-pass with a two-pole, high-pass feed forward section to provide complimentary real axis zeros. A variable attenuator is used to program the zero locations.

The filter implements a 0.05 degree equiripple linear phase response. The normalized transfer functions (i.e., $Wc = 2\pi fc = 1$) are:

$$Vnorm/Vi = [(-Ks2 + 17.98016)/D(s)] \times A_N$$

and

$$Vdiff/Vi = (Vnorm/Vi) \times (s/0.86133) \times A_D$$

where D (s)=

$$(S^2 + 1.68495s + 1.31703)(S^2 + 1.54203s + 2.95139)(S^2 + 1.14558s + 5.37034)(s + 0.86133),$$

A_N and A_D are adjusted for a gain of 2 at $fs = (2/3)fc$.

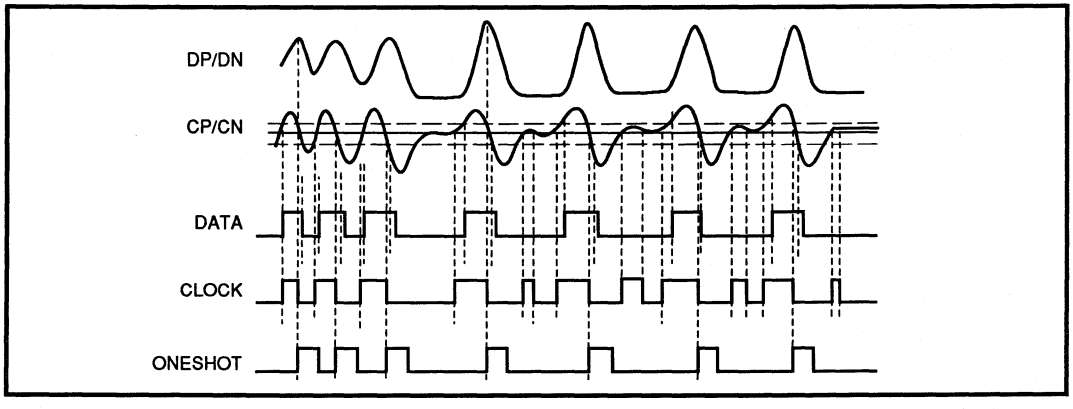

FIGURE 2: Hysteresis Comparator Timing Diagram

FUNCTIONAL DESCRIPTION (continued)

FILTER OPERATION

AC coupled differential signals from the AGC are applied to the FIP/FIN inputs of the filter. To improve settling time of the coupling capacitors, the FIP/FIN inputs are placed into a Low-Z state when the $\overline{LOW\_Z}$ pin is brought low. The programmable bandwidth and boost/equalization features are controlled by internal DACs and the registers programmed through the serial port. The current reference for both DACs is set using a single 12.1 kΩ external resistor connected from pin RX to ground. The voltage at pin RX is proportional to absolute temperature (PTAT), hence the current for the DACs is a PTAT reference current.

BANDWIDTH CONTROL

The programmable bandwidth is set by the filter cutoff DAC. This DAC has two separate 7-bit registers that can program the DAC value as follows:

fc = 0.09449 x DACF (MHz)
where DACF = MODMCR or EMCR value

In the MO Data mode, the MO Data Mode Cutoff Register (MODMCR) is used to determine the filter's 3 dB cutoff frequency. In the Emboss mode, the Emboss Mode Cutoff Register (EMCR) is used. Switching of the registers is controlled by the MO/emboss gate (MOEG) pin. The filter cutoff set by the internal DAC is the unboosted 3 dB frequency. When boost/equalization is added, the actual 3 dB point will move out. Table 1 provides information on boost verses 3 dB frequency.

TABLE 1: 3 dB cutoff frequency versus boost magnitude.

BOOST (dB)	fc (3 dB)	BOOST (dB)	fc (3 dB)
0	1.00	7	2.42
1	1.21	8	2.51
2	1.50	9	2.59
3	1.80	10	2.66
4	2.04	11	2.73
5	2.20	12	2.80
6	2.32	13	2.86

BOOST/EQUALIZATION CONTROL

The programmable equalization is also controlled by an internal DAC. The 7-bit Filter Boost Control Register (FBCR) determines the amount of equalization that will be added to the 3 dB cutoff frequency, as follows:

Boost = 20 log [(0.0273 x FBCR) + 1] (dB)

For example, with the DAC set for maximum output (FBCR = 7fH or 127) there will be 13 dB of boost added at the 3 dB frequency. This will result in +10 dB of signal boost above the 0 dB baseline. When MOEG is active the boost can be disabled by setting bit 7 in Control A register (CAR). When bit 7 is "0" and MOEG is active the boost will automatically be set to 0 dB. If bit 7 is "1" the boost will remain at its programmed value regardless of the state of MOEG.

TIME BASE GENERATOR CIRCUIT DESCRIPTION

The time base generator, which is a PLL based circuit, provides a programmable frequency reference for constant density recording applications. The frequency can be programmed with an accuracy better than 1%. An external passive loop filter is required to control the PLL locking characteristics. The filter is fully-differential and balanced in order to suppress common mode noise generated, for example, from the data synchronizer's PLL.

In Read, Write and Idle modes, the time base generator is programmed to provide a stable reference frequency for the data synchronizer. In Read mode the internal reference clock is disabled after the data synchronizer has achieved lock and switched over to read MO data as the source for the RRC. This minimizes jitter in the data synchronizer PLL. The reference frequency is programmed using the M and N registers of the time base generator via the serial port, and is related to the external reference clock input, FREF, as follows:

Reference Frequency = ((M+1)/(N+1))FREF

TIME BASE GENERATOR CIRCUIT DESCRIPTION (continued)

The VCO center frequency and the phase detector gain of the time base generator are controlled by an internal DAC addressed through the MO data recovery control register (MODRCR). This DAC also sets the 1/3 cell delay for (1,7) code or 1/4 cell delay for (2,7) code, VCO center frequency, and phase detector gain for the data synchronizer circuitry. When changing frequencies, the M and N registers must be loaded first, followed by the MODRCR register. A frequency change is initiated only when the MODRCR register has been changed.

$$Fvco = [12.5/(RR + 0.4)] \times [(0.622 \times IDAC) + 4.27] \text{ MHz};$$
for $Fvco < 24$ MHz

$$Fvco = [12.5/(RR + 0.4)] \times [(0.7 \times IDAC) + 1.4] \text{ MHz}$$

Where IDAC is the value in the MODRCR and RR is the value (kΩ) of the external RR resistor.

DATA SYNCHRONIZER CIRCUIT DESCRIPTION

In the Read mode, the data synchronizer performs sync field search and data synchronization. In the Write mode, the circuit provides write precompensation. Data rate is established by the time base generator and the internal reference DACI controlled by the MODRCR. The DAC generates a reference current which sets the VCO center frequency, the phase detector gain, and the 1/3 or 1/4 cell delay.

PHASE LOCKED LOOP

The circuit employs a Dual mode phase detector; harmonic in the Read mode and non-harmonic in the Write and Idle modes. In the Read mode the harmonic phase detector updates the PLL with each occurrence of a $\overline{DRD}$ pulse. In the Write and Idle modes the non-harmonic phase detector is continuously enabled, thus maintaining both phase and frequency lock onto the reference frequency of the internal time base generator. By acquiring both phase and frequency lock to the input reference frequency and utilizing a zero phase restart technique, the VCO transient is minimized and false lock to DLYD DATA is eliminated. The phase detector incorporates a charge pump in order to drive the loop filter directly. The polarity and width of the output current pulses correspond to the direction and magnitude of the phase error.

The data synchronizer also requires an external passive loop filter to control its PLL locking characteristics. The filter is again fully-differential and balanced in order to suppress common mode noise which may be generated from the time base generator's PLL.

MODE CONTROL

The read gate (RG) and write gate (WG) inputs control the Device Operating mode. RG is an asynchronous input and may be initiated or terminated at any position on the disk. WG is also an asynchronous input, but should not be terminated prior to the last output write MO data pulse.

READ MODE

The data synchronizer utilizes a fully integrated fast acquisition PLL to accurately develop the decode window. Read gate (RG) initiates the PLL locking sequence and selects the PLL reference input; a high level (Read mode) selects the internal RD input and a low level selects the reference clock. In the Read mode the falling edge of $\overline{DRD}$ enables the phase detector while the rising edge is phase compared to the rising edge of the VCO reference (VCOR). $\overline{DRD}$ is a 1/3 (for (1,7) code or 1/4 for (2,7) code) cell wide (TVCO) pulse whose leading edge is defined by the falling edge of RD. A decode window is developed from the VCOR clock.

PREAMBLE SEARCH

When RG is asserted, an internal counter is triggered to count positive transitions of the incoming read MO data, RD. Once the counter reaches a count of 3, the internal read gate is enabled. This switches the phase detector reference from the internal time base to the delayed read data ($\overline{DRD}$) signal. At the same time an internal zero phase restart signal restarts the VCO in phase with the $\overline{DRD}$. This prepares the VCO to be synchronized to MO data when the bit sync circuitry is enabled after VCO lock is established.

FUNCTIONAL DESCRIPTION (continued)

VCO LOCK AND BIT SYNC ENABLE

One of two VCO locking modes will be entered depending on the state of the gain shift (GS) bit, or bit 1, in the Control B register. If GS = "1," the phase detector will enter a Gain Shift mode of operation. The phase detector starts out in a High Gain mode of operation to support fast phase acquisition. After an internal counter counts the first 11 transitions of the internal $\overline{DRD}$ signal, the gain is reduced by a factor of 3. This reduces the bandwidth and dampening factor of the loop by $\sqrt{3}$ which provides improved jitter performance in the MO data follow mode. The counter continues to count the next 5 $\overline{DRD}$ transitions (a total of 19 pulses from assertion of RG) and then asserts an internal VCO lock signal.

When the VCO lock signal is asserted, the internal RRC source is also switched from the time base generator to the VCO clock signal that is phase locked to $\overline{DRD}$. During the internal RRC switching period the external RRC signal may be held for a maximum of 2 VCO clock periods, however no short duration glitches will occur.

When the GS bit is set to "0" the phase detector gain shift function is disabled. The VCO lock sequence is identical to that of the Gain Shift mode explained above, except that no gain shift is made after the first 11 transitions.

WINDOW SHIFT

Shifting the phase of the VCO clock effectively shifts the relative position of the $\overline{DRD}$ pulse within the decode window. Decode window control is provided via the WS control bits of the Window Shift Control Register (WSCR). Further description of the WSCR is provided in the window shift control section.

NON-READ MODE

In the Non-Read modes, the PLL is locked to the reference clock. This forces the VCO to run at a frequency which is very close to that required for tracking actual MO data. When the reference input to the PLL is switched, the VCO is stopped momentarily, then restarted in an accurate phase alignment with the next PLL reference input pulse. By minimizing the phase alignment error in this manner, the acquisition time is substantially reduced.

WRITE MODE

Write mode is entered by asserting the write gate ($\overline{WG}$) while the RG is held low. During Write mode the VCO and the RRC are referenced to the internal time base generator signal.

OPERATING MODES AND CONTROL

The SSI33P3733A has several operating modes that support Read, Write, Emboss, and power management functions. Mode selection is accomplished by controlling the read gate (RG), write gate ($\overline{WG}$), MO/emboss gate (MOEG), and $\overline{PWRON}$ pins. Additional modes are also controlled by programming the Power Down Control Register (PDCR), the Control A register (CAR), and the Control B register (CBR) via the serial port.

EXTERNAL MODE CONTROL

All operating modes of the device are controlled by driving the read gate (RG), write gate ($\overline{WG}$), MO/emboss gate (MOEG), and $\overline{PWRON}$ pins with TTL compatible signals. For normal operation the $\overline{PWRON}$ pin is driven low. During normal operation the SSI 33P3733A is controlled by the read gate (RG), write gate ($\overline{WG}$), and MO/emboss gate (MOEG) pins. When RG is high and $\overline{WG}$ is high the device is in Read mode. When $\overline{WG}$ is low and RG is low the device is in Write mode. If the RG is low and $\overline{WG}$ is high the device will be in Idle mode. During the Idle mode, the MOEG pin can be activated to enable the Emboss mode of operation.

POWER DOWN CONTROL

For power management, the $\overline{PWRON}$ pin can be used in conjunction with the Power Down Control Register (PDCR) to set the Operating mode of the device. The PDCR provides a control bit for each of the functional blocks. When the $\overline{PWRON}$ pin is brought high ("1") the device is placed into Sleep mode (<5 mW) and all circuits are powered down except the serial port. This allows the user to program the serial port registers while still conserving power. Register information is retained during the Sleep mode so it is not necessary to reprogram the serial port registers after returning to an Active mode. When the $\overline{PWRON}$ pin is driven low ("0"), the contents of the PDCR determine which blocks will be active. Register mapping for the PDCR is shown in Table 3. To improve recovery time from the Sleep mode, the $\overline{LOW\_Z}$ pin should be asserted following power down to initiate the AGC recovery sequence.

SERIAL INTERFACE OPERATION

The serial interface is a CMOS bi-directional port for reading and writing programming data from/to the internal registers of the SSI 33P3733A. The serial port data transfer format is shown in Figure 3. For data transfers SDEN is brought high, serial data is presented at the SDATA pin, and a serial clock is applied to the SCLK pin. After the SDEN goes high, the first 16 pulses applied to the SCLK pin will shift the data presented at the SDATA pin into an internal shift register on the rising edge of each clock. An internal counter prevents more than 16 bits from being shifted into the register. The data in the shift register is latched when SDEN goes low. If less than 16 clock pulses are provided before SDEN goes low, the data transfer is aborted.

All transfers are shifted into the serial port LSB first. The first byte of the transfer is address and instruction information. The LSB of this byte is the R/W bit which determines if the transfer is a read (1) or a write (0). The remaining 7-bits determine the internal register to be accessed. Table 3 provides register mapping information. The second byte contains the programming data. In Read mode (R/W=1) the SSI 33P3733A will output the register contents of the selected address. In Write mode the device will load the selected register with data presented on the SDATA pin. At initial power-up, the contents of the internal registers will be in an unknown state and must be programmed prior to operation. During power down modes, the serial port remains active and register programming data is retained. Detailed timing information is provided in Figure 4.

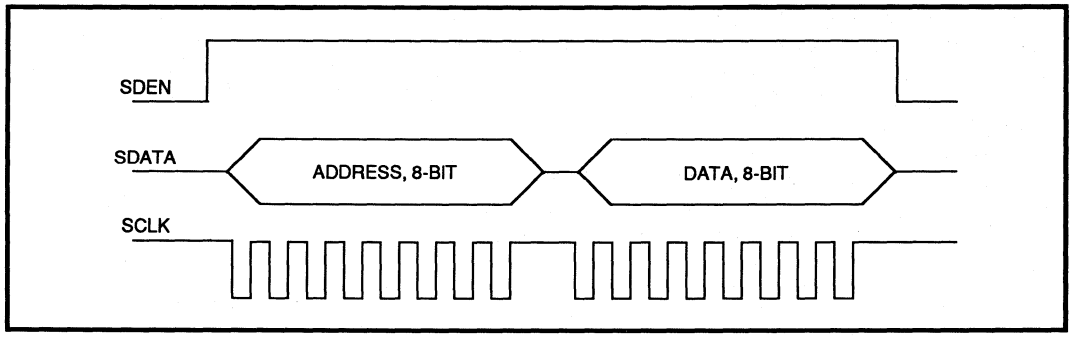

FIGURE 3: Serial Port Data Transfer Format

TABLE 2: MODE CONTROL

CONTROL LINE				DEVICE MODE	DAC CONTROL			
$\overline{PWRON}$	RG	MOEG	$\overline{WG}$		VTH	FC	BOOST	HYSTERESIS
1	X	X	X	**SLEEP MODE:** All functions are powered down. The serial port registers remain active and register programming data is saved.	off	off	off	off
0	0	0	0	**WRITE MODE:** The pulse detector is inactive. The data synchronizer VCO is locked to the internal time base generator.	MR	MR	MR	MR
0	1	0	1	**READ MODE:** The pulse detector is active. The data synchronizer begins the preamble lock sequence. RDIO is active	MR	MR	MR	MR
0	0	1	1	**EMBOSS MODE:** The pulse detector is active and the emboss control registers are enabled for the Fc DAC and the VTH DAC. The data synchronizer and time base generator can be disabled using the PDCR.	ER	ER	off	ER
0	0	0	1	**IDLE MODE:** The contents of the PDCR determine which blocks are powered-up. In normal operation with all blocks powered-up, the pulse detector is active, the data synchronizer VCO is locked to the time base generator, and the MO data control registers are used for VTH and FC.	MR	MR	MR	MR
-	-	-	-	All other states are illegal. If an illegal state is programmed, the chip function will be in an indeterminable state, but no damage will occur.	MR	MR	MR	MR

DAC CONTROL KEY: MR = MO DATA REGISTER, ER = EMBOSS RIGISTER, OFF = DISABLED

REGISTER NAME	A6			ADDRESS			A0	R/W	D7			DATA BIT MAP				D0
POWER DOWN CONTROL	0	0	0	0	0	1	0	0	--	--	--	TBG 1=DISABLE 0=ENABLE	DATA SEP 1=DISABLE 0=ENABLE	FILTER 1=DISABLE 0=ENABLE	--	PD 1=DISABLE 0=ENABLE
MO DATA MODE CUTOFF	0	0	0	0	0	1	1	0	--	FCM DAC BIT 6	FCM DAC BIT 5	FCM DAC BIT 4	FCM DAC BIT 3	FCM DAC BIT 2	FCM DAC BIT 1	FCM DAC BIT 0
EMBOSS MODE CUTOFF	0	0	1	0	0	1	1	0	--	FCE DAC BIT 6	FCE DAC BIT 5	FCE DAC BIT 4	FCE DAC BIT 3	FCE DAC BIT 2	FCE DAC BIT 1	FCE DAC BIT 0
FILTER BOOST	0	0	0	1	0	1	1	0	EMBOSS BOOST 1=ENABLE 0=DISABLE	FBDAC BIT 6	FB DAC BIT 5	FB DAC BIT 4	FB DAC BIT 3	FB DAC BIT 2	FB DAC BIT 1	FB DAC BIT 0
MO DATA THRESHOLD	0	0	0	1	0	1	0	0	1=DUAL 0=HYS	TMDAC BIT 6	TM DAC BIT 5	TM DAC BIT 4	TM DAC BIT 3	TM DAC BIT 2	TM DAC BIT 1	TM DAC BIT 0
EMBOSS THRESHOLD	0	0	1	0	0	1	0	0	1=DUAL 0=HYS	TEDAC BIT 6	TE DAC BIT 5	TE DAC BIT 4	TE DAC BIT 3	TE DAC BIT 2	TE DAC BIT 1	TE DAC BIT 0
CONTROL A	0	0	1	1	0	1	0	0	Fast Decay test mode 0=ENABLE	TMS1	TMS0	TBG 1=BYPASS 0=NORMAL	TBG TEST POINT ENABLE	PUMP DWN 1=TP ON 0=TP OFF	PUMP UP 1=TP ON 0=TP OFF	PHASE DET 1=ENABLE 0=DISABLE
CONTROL B	0	0	0	1	1	0	0	0	--	MTPE 1=ENABLE 0=DISABLE	PUMP DWN 1=TP ON 0=TP OFF	PUMP UP 1=TP ON 0=TP OFF	PHASE DET 1=ENABLE 0=DISABLE	RDI/O 1 = RDI INPUT RDO HIGH-Z 0 = RDI DISABLE	GAIN SHFT 1 = ON 0 = OFF	--
N COUNTER	0	0	0	0	1	1	0	0	--	N COUNT BIT 6	N COUNT BIT 5	N COUNT BIT 4	N COUNT BIT 3	N COUNT BIT 2	N COUNT BIT 1	N COUNT BIT 0
M COUNTER	0	0	0	1	1	1	0	0	M COUNT BIT 7	M COUNT BIT 6	M COUNT BIT 5	M COUNT BIT 4	M COUNT BIT 3	M COUNT BIT 2	M COUNT BIT 1	M COUNT BIT 0
DATA RECOVERY	0	0	0	0	1	0	0	0	--	DAC I BIT 6	DAC I BIT 5	DAC I BIT 4	DAC I BIT 3	DAC I BIT 2	DAC I BIT 1	DAC I BIT 0
WINDOW SHIFT	0	0	0	0	1	0	1	0	TDAC 1	TDAC 0	WIN SHFT 1=ENABLE 0=DISABLE	WS DIR 1=LATE 0=EARLY	$\overline{WS3}$	$\overline{WS2}$	$\overline{WS1}$	$\overline{WS0}$
AGC LEVEL	0	1	0	0	0	1	0	0	--	--	--	--	AGC DAC BIT 3	AGC DAC BIT 2	AGC DAC BIT 1	AGC DAC BIT 0
HYSTERESIS DECAY	0	1	0	1	0	1	0	0	EMBOSS BIT 3	EMBOSS BIT 2	EMBOSS BIT 1	EMBOSS BIT 0	DATA BIT 3	DATA BIT 2	DATA BIT 1	DATA BIT 0

TABLE 3: Serial Port Register Mapping

FUNCTIONAL DESCRIPTION (continued)

CONTROL REGISTERS

Control registers CAR and CBR allow the user to configure the SSI 33P3733A test points for evaluation of different internal signals and also control other device functions. CAR controls functions of the pulse detector, filter, and time base generator. CBR controls test points and functions of the data separator. The bits of the CA and CB registers are defined as follows:

CONTROL REGISTER CA

BIT	NAME	FUNCTION
0	EPDT	Enable Phase Detector (Time Base Generator)
1	UT	Pump Up (TFLTR sources current, $\overline{\text{TFLTR}}$ sinks Current)
2	DT	Pump Down (TFLTR sinks current, $\overline{\text{TFLTR}}$ sources Current)
3	ET	Enable Time Base Generator Test Point Output
4	BYPT	Bypass Time Base Generator Circuit Function
5	TMS0	Control bit for selecting test point source (see Table 4)
6	TMS1	Control bit for selecting test point source (see Table 4)
7	FDTM	Constant fast decay current test mode

CONTROL REGISTER CB

0	-	Not Used
1	GS	Enable Phase Detector Gain Switching
2	RDI/O	RDI and RDO pins control
3	EPDD	Enable Phase Detector (Data Separator)
4	UD	Pump Up (DFLTR sources current, $\overline{\text{DFLTR}}$ sinks current)
5	DD	Pump Down (DFLTR sinks current, $\overline{\text{DFLTR}}$ sources current)
6	MTPE	Enable Test Points MTP1, 2, 3 (see Table 4)
7	-	Not used

PIN DESCRIPTION

POWER SUPPLY PINS

NAME	TYPE	DESCRIPTION
VPA	-	Data separator PLL analog power supply pin
VPB	-	Time base generator PLL analog power supply pin
VPC	-	Internal ECL, CMOS logic power supply pin
VPD, VPD2	-	CMOS buffer I/O digital power supply pin
VPG	-	Pulse detector, filter, analog power supply pin
VNA	-	Data separator PLL analog ground pin
VNB	-	Time base generator PLL analog ground pin
VNC	-	Internal ECL, CMOS logic ground pin
VND, VND2	-	CMOS buffer I/O digital ground pin
VNG	-	Pulse detector, filter, analog ground pin

INPUT PINS

AIP, AIN	I	AGC AMPLIFIER INPUTS: Differential AGC amplifier input pins.
DP, DN	I	ANALOG INPUTS FOR MO DATA PATH: Differential analog inputs to full-wave rectifier. These inputs do not have the internal DC bias.
CP, CN	I	ANALOG INPUTS FOR CLOCK PATH: Differential analog inputs to the clock comparator, and data comparators. (connect CP to DP, CN to DN externally)
$\overline{\text{LOW\_Z}}$	I	LOW IMPEDANCE ENABLE: TTL compatible input pin that activates the Low-Z switches. A low level activates the switches and the falling edge of the internal LOW_Z triggers the fast decay circuit.
$\overline{\text{PWRON}}$	I	POWER ENABLE: TTL compatible power control input. A low level input enables power to circuitry according to the contents of the PDCR. A high level input shuts down all circuitry.
HOLD	I	HOLD CONTROL: TTL compatible control pin which, when pulled high, disables the AGC charge pump and holds the AGC amplifier gain at its present value.
FIP, FIN	I	FILTER SIGNAL INPUTS: The AGC output signals must be AC coupled into these pins.
FREF	I	REFERENCE FREQUENCY INPUT: Frequency reference input for the time base generator. FREF may be driven either by a direct coupled TTL signal or by an AC coupled ECL signal. Pin FREF has an internal pull down resistor.
RDI	I	READ DATA INPUT: TTL compatible input. RDI is provided as a read data input to the data synchronizer from an external qualification circuit. RDI is available when CBR bit 2 goes high.

INPUT PINS (continued)

NAME	TYPE	DESCRIPTION
RG	I	READ GATE: TTL compatible read gate input. A high level TTL input selects the RD input and enables the Read mode/address detect sequences. A low level selects the FREF input.
MOEG	I	MO/emboss GATE: TTL compatible MO/emboss gate input. A high level TTL input activates the Emboss mode by selecting the emboss control registers, the RTS resistor, and the BYPE capacitor.
$\overline{WG}$	I	WRITE GATE: TTL compatible write gate input. A low level TTL input enables the Write mode.

OUTPUT PINS

MTP1-3	O	MULTIPLEXED TEST POINTS: Open emitter ECL output test points. Internal test signals are routed to these test points as determined by the CAR and CBR. External resistors are required to use these pins. They should be removed during normal operation to reduce power dissipation.
SDO	O	SYNCHRONIZED READ DATA: CMOS output pin. Read MO data output when RG is high.
FDP, FDN	O	DIFFERENTIAL DIFFERENTIATED OUTPUTS: Filter differentiated outputs. These outputs are AC coupled into the CP/CN inputs.
FNP, FNN	O	DIFFERENTIAL NORMAL OUTPUTS: Filter normal low pass output signals. These outputs are AC coupled into the DP/DN inputs.
RDO	O	RAW DATA OUTPUT: CMOS output pin. The rising edge of RDO indicates the presence of a valid MO data pulse. RDO is low when either RG is high or WG is low. When CBR bit 2 goes high, RDO will be held High-Z.
RRC	O	READ REFERENCE CLOCK: Read clock CMOS output. During a mode change, no glitches are generated and no more than one lost clock pulse will occur. When RG goes high, RRC initially remains synchronized to the reference clock. When the Sync Bits are detected, RRC is synchronized to the Read MO Data. When RG goes low, RRC is synchronized back to the reference clock.
AOP, AON	O	AGC AMPLIFIER OUTPUT: Differential AGC amplifier output pins. These outputs are AC coupled into the filter inputs (FIP/FIN).
FOUT	O	TIME BASE GENERATOR VCO OUTPUT: CMOS output pin. This clock signal is the data separator PLL reference. This output is independent of the RG/WG pin.
PPOL	O	PULSE POLARITY: Pulse polarity CMOS output pin. The output is high when the pulse being qualified is positive and it is low when the pulse being qualified is negative.

ANALOG PINS

NAME	TYPE	DESCRIPTION
BYPMO	-	The AGC Read mode integration capacitor CBYPMO, is connected between BYPMO and VPG.
BYPE	-	The AGC Emboss mode integration capacitor CBYPE, is connected between BYPE and VPG.
DACOUT	-	DAC VOLTAGE TEST POINT: This test point monitors the outputs of the internal DACs. The source DAC is selected by programming the two MSBs of the WSCR register (see Table 5).
TFLT, $\overline{\text{TFLT}}$	-	PLL LOOP FILTER: These pins are the connection points for the time base generator loop filter.
DFLT, $\overline{\text{DFLT}}$	-	PLL LOOP FILTER: These pins are the connection points for the data separator loop filter.
LEVEL	-	An NPN emitter output that provides a full-wave rectified signal from the DP, DN inputs. An external capacitor should be connected from LEVEL to VPG to set the hysteresis threshold time constant in conjunction with the internal current DAC, (DACA).
RR	-	REFERENCE RESISTOR INPUT: An external 12.1 kΩ, 1% resistor is connected from this pin to VNA to establish a precise internal reference current for the data separator and time base generator.
RX	-	REFERENCE RESISTOR INPUT: An external 12.1 kΩ, 1% resistor is connected from this pin to ground to establish a precise PTAT (proportional to absolute temperature) reference current for the filter.

SERIAL PORT PINS

SDEN	-	SERIAL DATA ENABLE: Serial enable CMOS input. A high level TTL input enables the serial port.
SDATA	-	SERIAL DATA: Serial data CMOS input. NRZ programming data for the internal registers is applied to this input.
SCLK	-	SERIAL CLOCK: Serial clock CMOS input. The clock applied to this pin is synchronized with the data applied to SDATA.

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, the recommended operating conditions are as follows: 4.5V < POSITIVE SUPPLY VOLTAGE < 5.5V, 0°C < T (ambient) < 70°C, and 25°C < T(junction) < 135°C. Currents flowing into the chip are positive. Current maximum are currents with the highest absolute value.

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may damage the device.

PARAMETER	RATING
Storage Temperature	-65 to 150°C
Junction Operating Temperature	+135°C
Positive Supply Voltage (Vp)	-0.5 to 7V
Voltage Applied to Logic Inputs	-0.5V to Vp + 0.5V
All other Pins	-0.5V to Vp + 0.5V

POWER SUPPLY CURRENT AND POWER DISSIPATION

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
ICC (VPA,B,C,D,G)	Outputs and test point pins open, Ta = 27°C, VPn = 5V, 24 Mbit/s		75		mA
PWR Power Dissipation	Outputs and test point pins open, Ta = 27°C, VP = 5V, 24 Mbit/s		375		mW
Sleep mode Power	$\overline{\text{PWRON}}$ = 1			5	mW
Emboss mode Power	$\overline{\text{PWRON}}$ = 0 TBG Disabled Data Sep. Disabled		200		mW

DIGITAL INPUTS AND OUTPUTS

TTL Compatible Inputs

Input low voltage	VIL		-0.3		0.8	V
Input high voltage	VIH		2		VPD + 0.3	V
Input low current	IIL	VIL = 0.4V			-100	µA
Input high current	IIH	VIH = 2.4V			50	µA

CMOS Compatible Inputs - Schmitt trigger type (not to be left open.) Nominal 1.0V hysteresis around VPD/2.

Input low voltage		-0.3		1.5	V
Input high voltage		3.5		VPD + 0.3	V

CMOS Compatible Outputs

Output low voltage	5V, 25°C IOL = 4.07 mA			0.5	V
Output high voltage	5V, 25°C IOH = -4.83 mA	4.5			V
Rise time	4.5V, 70°C, C = 15 pF			8	ns
Fall time	4.5V, 70°C, C = 15 pF			8	ns

PSEUDO ECL OUTPUT LEVELS (MTP1, MTP2, MTP3)
For all tests, 261Ω to VPA and 402Ω to VNA with VPA = 5.0V

Output high level		VPA -1.02			V
Output low level				VPA -1.62	V

SERIAL PORT

SCLK period	T_{CLK}		100			ns
SCLK low time	T_{CKL}		40			ns
SCLK high time	T_{CKH}		40			ns
Enable to SCLK	T_{SENS}		35			ns
SCLK to disable	T_{SENH}		35			ns
Data set-up time	T_{DS}		15			ns
Data hold time	T_{DH}		15			ns
SDATA tri-state delay	T_{SENDL}				50	ns
SDATA turnaround time	T_{TRN}		70			ns
SDEN low time	T_{SL}		200			ns

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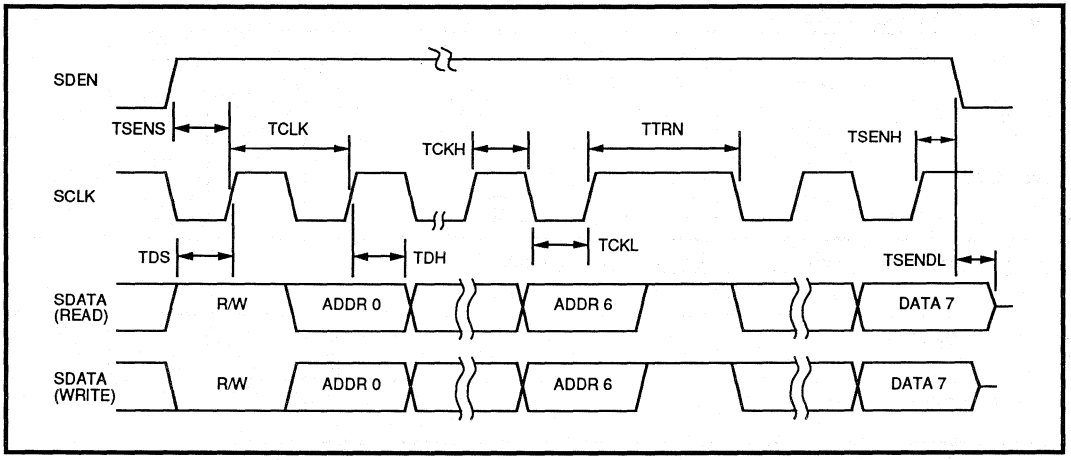

FIGURE 4: Serial Port Timing Information

ELECTRICAL SPECIFICATIONS (continued)

PULSE DETECTOR CHARACTERISTICS

AGC Amplifier

Input signals are AC coupled to AIP/AIN, AOP/AON outputs are AC coupled to FIP/FIN, and FDP/FDN are AC coupled to CP/CN. CP/CN and DP/DN are connected to each other. 1000 pF capacitors are connected from BYPMO to VPG (C_{BYPMO}) and from BYPE to VPG (C_{BYPE}). Unless otherwise specified, outputs are measured differentially at AOP/AON, FIN = 8 MHz, and filter boost = 0 dB.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Input range	Filter boost 0 to 13 dB	20		190	mVpp
DP-DN voltage	AIP - AIN = 0.1 Vpp	0.9	1	1.1	Vpp
	MOEG = high, AGC DAC = 0	0.9	1	1.1	Vpp
	MOEG = high, AGC DAC = 15	0.68	0.76	0.84	Vpp
DP-DN voltage variation	20 mV < AIP - AIN < 190 mV			8	%
Gain range		0.45		18	V/V
Gain sensitivity	BYPx voltage change		28		dB/V
AOP-AON dynamic range	THD = 1%	0.6			Vpp
Differential input impedance	$\overline{LOW\_Z}$ = high	4.7	6	8.4	kΩ
	$\overline{LOW\_Z}$ = low		350		Ω
Single-ended input impedance	$\overline{LOW\_Z}$ = high		3.3		kΩ
	$\overline{LOW\_Z}$ = low		250		Ω
Single-ended output impedance	AOP/AON to ground			120	Ω
Output offset voltage variation	Gain = 0.45 to 18			200	mV
Input noise voltage	Gain = 18, AOP - AON = 0V			20	nV/√Hz
Bandwidth	Gain = 18, CL ≤ 15 pF	35			MHz
CMRR Gain = 18, fc = 5 MHz		40			dB
PSRR Gain = 18, fc = 5 MHz		45			dB
Gain decay time	AIP - AIN = 250 to 125 mV, AOP - AON > 0.9 Final Value		36		µs
Gain attack time	AIP - AIN = 125 to 250 mV, AOP - AON < 1.1 Final Value		0.65		µs

AGC Control

The input signals are AC coupled into DN/DP, C_{BYPX} = 1000 pF to VPG, MOEG = low.

DP-DN input range	For test only			1	1.5	Vpp
Decay current	Normal decay	I_D		4		µA
	Fast Decay mode	I_{DF}		21 x I_D		µA
Attack current	Normal attack	I_{CH}		0.18		mA
	Fast Attack mode	I_{CHF}		8 x I_{CH}		mA

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AGC Control (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
BYPMO leakage current	$\overline{WG}$ = high	-10		10	nA
Fast decay duration			1		µs
LEVEL output gain	|DP-DN| = 0.5 to 1.5V	0.60	0.65	0.70	V/Vpp
LEVEL output bandwidth	-1 dB	10			MHz
LEVEL pin pull-down current	DACL = 0000	1.56	3.125	4.69	µA
	DACL = 1111 where I_{LEVEL} = 3.125 x (1 + DACL) µA	47	50	53	µA

Data Comparator
The input signals are AC coupled into DP/DN.

DP-DN input range			1	1.5	Vpp
Differential input resistance		1			MΩ
Differential input capacitance				5	pF
Threshold voltage hysteresis			10		%T
Threshold voltage gain (K_{TH}) tolerance	0.47 < |DP - DN| < 1.19 T = V_{THDAC} x 0.93/127 38 < V_{THDAC} < 127	T - 10		T + 10	%
Minimum threshold voltage	|DP - DN| < 0.16 V_{THMIN} = V_{THDAC} • 97.6%/127		V_{THMIN}		V
PPOL rise time	10% to 90% points, CL ≤ 15 pF			8	ns
PPOL fall time	90% to 10% points, CL ≤ 15 pF			8	ns

Clock Section
The input signals are AC coupled into CP/CN.

CP-CN input range				1.5	Vpp
Comparator offset voltage		-4		4	mV
Differential input resistance	$\overline{LOW\_Z}$ = Off	2.5		7.5	kΩ
	$\overline{LOW\_Z}$ = On	0.6		1.6	kΩ
Differential input capacitance				5	pF
Pulse pairing	DP/DN = 1 Vpp sine, CP/CN = 1 Vpp - 90°sine Fsine = 8 MHz			0.5	ns
RDO pulse width	CL ≤ 15 pF	6		15	ns
RDI input pulse width		10			ns
RDO rise time	10% to 90% points, CL ≤ 15 pF			8	ns
RDO fall time	90% to 10% points, CL ≤ 15 pF			8	ns

Programmable Filter Characteristics

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Filter cutoff range	*fc* @ -3 dB point *fc* = (0.09449 MHz) x DACF, Boost = 0 dB 42 ≤ DACF ≤ 127 DACF = MODMCR	4		12	MHz
Filter cutoff accuracy	DACF = 127	-10		10	%
	DACF = 42 to DACF < 127	-15		15	%
FNP, FNN differential gain (A_N)	F = 0.67 x *fc*, boost = 0 dB	1.6	2	2.4	V/V
FDP, FDN differential gain (A_D)	F = 0.67 x *fc*, boost = 0 dB	0.8 A_N		1.2 A_N	V/V
Frequency boost @ *fc* = 12 MHz	DACS = 127		13		dB
Boost accuracy	@ 6 dB, DACS = 37	-1		+1	dB
	@ 9 dB, DACS = 67	-1.25		+1.25	dB
	@ 13 db, DACS = 127	-1.5		+1.5	dB
MO/Emboss mode group delay variation	*fc* = 4 to 12 MHz F = 0.2 *fc* to *fc*, Boost = 0 and 3dB	-2		+2	%
FNP, FNN; FDP, FDN	*fc* = 4 to 12 MHz F = *fc* to 1.75 *fc*, Boost = 3dB	-3		+3	%
Filter output THD @ 1 Vpp	F = 0.67 *fc* *fc* = 4 to 12 MHz			1.5	%
Filter differential input resistance	Normal	3			kΩ
	Low-Z		140		Ω
Filter differential input capacitance				7	pF
Output noise voltage	BW = 100 MHz, Rs = 50Ω				
differentiated output	*fc* = 12 MHz, boost = 0 dB		2.6		mV Rms
differentiated output	*fc* = 12 MHz, boost = 13 dB		5.6		mV Rms
normal output	*fc* = 12 MHz, boost = 0 dB		2		mV Rms
normal output	*fc* = 12 MHz, boost = 13 dB		3.6		mV Rms
Filter output sink current			0.5		mA
Filter output offset voltage				200	mV
Filter output source current		2			mA
Filter output resistance	single ended			200	Ω
Rx pin voltage	Ta = 27°C		600		mV
	Tj = 127°C		800		mV
Rx resistance 1% fixed value			12.1		kΩ

PULSE DETECTOR CHARACTERISTICS (continued)

Time Base Generator Characteristics

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
FREF input range		8		20	MHz
FOUT frequency range				75	MHz
FOUT jitter	TOUT = 1/FOUT Loop acquisition time = 30 µs	-TBD goal = 200		+TBD goal = 200	ps (rms)
M counter range		2		255	
N counter range		2		127	
VCO center frequency period (TVCO)	FVCO = [12.5/(RR + 0.4)] x [(0.622 x IDAC)+ 4.27] MHz TFLT - $\overline{TFLT}$ = TBD FVCO < 24 MHz FVCO = [12.5/(RR + 0.4)] x [(0.7 x IDAC) + 1.4] MHz	0.85 T0		1.15 T0	ns
VCO dynamic range	-2V ≤ TFLT - $\overline{TFLT}$ ≤ +2V FOUT = 36 MHz RR = 12.1 kΩ	±25		±45	%
VCO control gain KVCO	ωi = 2π/TVCO -2V ≤ TFLT - $\overline{TFLT}$ ≤ +2V	0.12 ωi		0.24 ωi	rad/(V-S)
Phase detector gain KD	KD = [12.5/(RR+0.4)] x (0.656 x IDAC + 3.38) x 10^{-6}	0.83 KD		1.17 KD	A/rad
KVCO x KD product accuracy		-28		+28	%
RR resistor range			12.1		kΩ
FREF input low time		20			ns
FREF input high time		20			ns
FOUT rise time	10% to 90% points, CL ≤ 20 pF			8	ns
FOUT fall time	90% to 10% points, CL ≤ 20 pF			8	ns

DATA SYNCHRONIZER CHARACTERISTICS

Read Mode

Read clock rise time TRRC	10% to 90% points CL ≤ 15 pF			8	ns
Read clock fall time TFRC	90% to 10% points CL ≤ 15 pF			8	ns
RRC duty cycle	Except during re-sync	40		60	%
TRD	During re-sync	40			%
SD0 out set-up and hold time (TSDS, TSDH)		10			ns
1/2 code bit cell delay	TD = TVCO/2	0.8 TD		1.2 TD	ns

Data Synchronization

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VCO center frequency period (TVCO)	Fvco = [12.5/(RR + 0.4)] x [(0.622 x IDAC) + 4.27] MHz TVCO = 1/FVCO, DFLT - $\overline{DFLT}$ = TBD RR = 12.1 kΩ Fvco < 24 MHz Fvco = [12.5/(RR + 0.4)] x [(0.7 x IDAC) + 1.4] MHz	0.85 T0		1.15 T0	ns
VCO dynamic range	-2V ≤ DFLT - $\overline{DFLT}$ ≤ +2V	±25		±45	%
VCO control gain KVCO	ωi = 2π/TVCO -2V ≤ DFLT- $\overline{DFLT}$ +2V	0.12 ωi		0.24 ωi	rad/(V-S)
Phase detector gain KD	Idle mode = 1 x KD Read mode = 3 x KD Read mode after gain shift = 1 x KD KD = [12.5/(RR + 0.4)] x (0.656 x IDAC + 3.38) x 10^{-6}	0.83 KD		1.17 KD	A/rad
VCO phase restart error	Fvco = 72 MHz	-2		+2	ns
Decode window center accuracy		-0.75		+0.75	ns
Decode window width		TVCO - 0.75			ns

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APPLICATIONS INFORMATION

WINDOW SHIFT CONTROL

Window shift magnitude is set by the value in the Window Shift (WS) register. The WS register bits are as follows:

BIT	NAME	FUNCTION
0	$\overline{WS0}$	
1	$\overline{WS1}$	
2	$\overline{WS2}$	
3	$\overline{WS3}$	
4	WSD	Window shift direction. 0=early, 1=late
5	WSE	Window shift enable
6	TDAC0	Used to route signals to DAC test point
7	TDAC1	Used to route signals to DAC test point

The window shift magnitude is set as a percentage of the full decode window, in 2% steps. This results in a window shift capability of ± 30% of the full decode window. The tolerance of the window shift magnitude is ± 30%. Window shift should be set during Idle mode or Write mode.

$\overline{WS3}$	$\overline{WS2}$	$\overline{WS1}$	$\overline{WS0}$	Shift Magnitude
1	1	1	1	No shift
1	1	1	0	2% (minimum shift)
1	1	0	1	4%
1	1	0	0	6%
1	0	1	1	8%
1	0	1	0	10%
1	0	0	1	12%
1	0	0	0	14%
0	1	1	1	16%
0	1	1	0	18%
0	1	0	1	20%
0	1	0	0	22%
0	0	1	1	24%
0	0	1	0	26%
0	0	0	1	28%
0	0	0	0	30% (maximum shift)

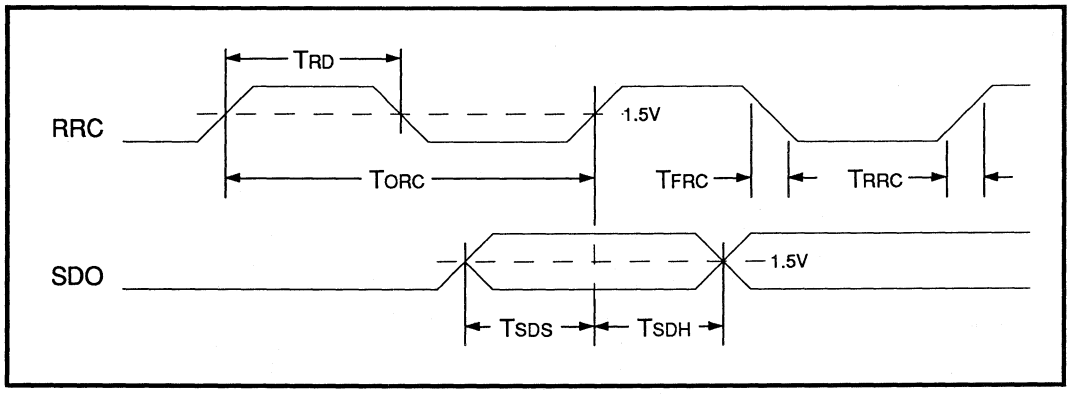


FIGURE 5: SDO Read Timing

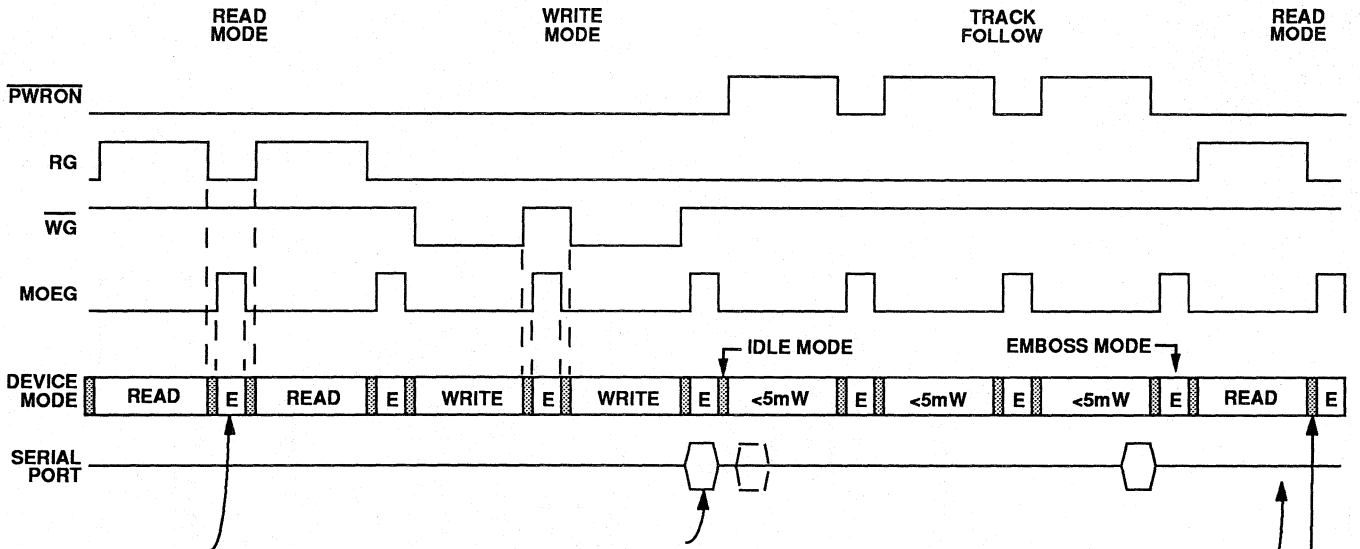
TABLE 4: Multiplexed Test Point Signal Selection

MTPE	TMS1	TMS0	MTP1	MTP2	MTP3
0	X	X	OFF	OFF	OFF
1	0	0	VCOREF	$\overline{DRD}$	DSREF
1	0	1	RD	DOUT	COUT
1	1	0	—	—	NCTR
1	1	1	SET	RESET	COUT

COUT Output of the pulse qualifier clock circuit
DOUT Output of the pulse qualifier data comparators
DSREF Output of the time base generator
NCTR Ncounter output of the time base generator
RD Read MO data output from the pulse qualifier
RESET Output of the negative threshold comparator
SET Output of the positive threshold comparator

TABLE 5: DACOUT Test Point Signal Selection

TDAC1	TDAC0	DAC MONITORED
0	0	Filter fc DAC
0	1	Qualifier threshold DAC (VTH)
1	0	Window shift DAC
1	1	Unused



When MOEG is HIGH the device will switch to the VE register for the threshold DAC and Fc DAC and the RTS resistor for the LEVEL pin output.

Prior to entering the Track Follow mode, the Power Down Control Register is changed to disable the Data Separator and Time Base Generator blocks. Data can be loaded with PWRON either LOW or HIGH.

Prior to returning to read mode (or write mode) the Power Down Control Register is changed to enable the Data Separator and Time Base Generator blocks. Load data while PWRON is HIGH.

When RG is low and WG is high, the device will enter an idle state where the AGC is active and the data synchronizer is locked to the internal FREF.

NOTES:

1) When the PWRON pin is LOW ("0") the Power Down Control Register is active. All blocks that have their control bit set to "1" will be powered down. When the PWRON pin is HIGH ("1") the device goes into a sleep mode with all blocks powered down except the serial port.

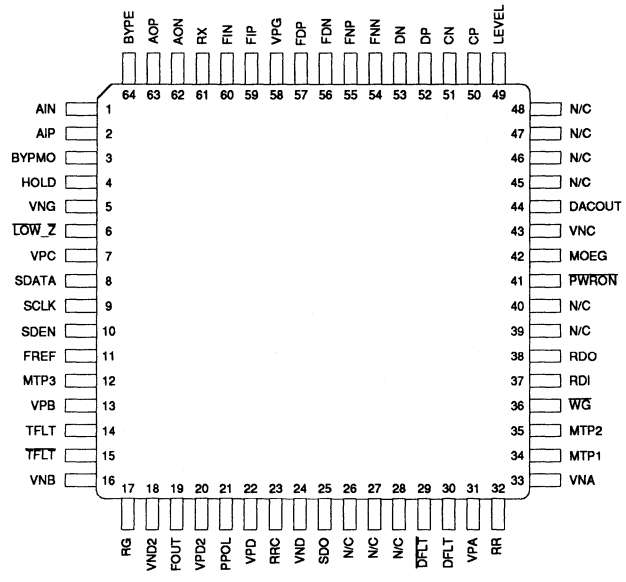
2) When the threshold DAC reference is switched, there is a maximum settling time of 1.5 μsec for the DAC.

FIGURE 6: Power Control Timing

PACKAGE PIN DESIGNATIONS
(Top View)

Thermal Characteristics: θjA

64-lead TQFP	75° C/W



64-Lead TQFP

CAUTION: Use handling procedures necessary for a static sensitive component.

ORDERING INFORMATION

PART DESCRIPTION	ORDER NUMBER	PACKAGE MARK
SSI 33P3733A 64-Lead TQFP	33P3733A-CGT	33P3733A-CGT

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Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914

Notes:

silicon systems®
A TDK Group Company

SSI 33P3733/34
8-26.5 Mbit/s Read Channel

Preliminary Data

December 1993

DESCRIPTION

The SSI 33P3733/34 device is a high performance BiCMOS single chip read channel IC that contains all the functions needed to implement a complete zoned recording read channel for magneto-optical (MO) drive systems. Functional blocks include the pulse detector, programmable filter, time base generator, and data synchronizer. MO data rates from 8 to 26.5 Mbit/s for (1,7) code, 6 to 20 Mbit/s for (2,7) code can be programmed using an internal DAC whose reference current is set by a single external resistor.

Programmable functions of the SSI 33P3733/34 device are controlled through a bi-directional serial port and banks of internal registers. This allows zoned recording applications to be supported without changing external component values from zone to zone.

The SSI 33P3733/34 utilizes an advanced BiCMOS process technology along with advanced circuit design techniques which result in a high performance device with low power consumption.

FEATURES

- **Programmable MO data rate of 8 to 26.5 Mbit/s for (1,7) code, 6 to 20 Mbit/s for (2,7) code, internal DAC controlled**
- **Complete zoned recording application support**
- **Low-power operation (375 mW typical @ 5V)**
- **Bi-directional serial port for register access**
- **Register programmable power management (Sleep mode <5 mW)**
- **Power supply range (4.5 to 5.5 volts)**
- **Small footprint 64-lead TQFP package**

PULSE DETECTOR

- **Fast Attack/Decay modes for rapid AGC recovery**
- **Dual rate charge pump for fast transient recovery**
- **Low Drift AGC hold circuitry**
- **Temperature compensated, exponential control AGC**
- **Wide bandwidth, high precision full-wave rectifier**
- **Programmable LEVEL pin time constant with separate MO data and emboss registers**
- **Separate Read and emboss AGC levels (4-bit DAC)**
- **Dual mode pulse qualification circuitry (user selectable)**
- **Internal fast decay timing**
- **External $\overline{\text{LOW\_Z}}$ control pin**
- **0.5 ns max. pulse pairing with sine wave input**

PROGRAMMABLE FILTER

- **Programmable cutoff frequency of 4 to 12 MHz**
- **Programmable boost/equalization of 0 to 13 dB**
- **Matched normal and differentiated outputs**
- **± 10 to 15% *fc* accuracy**
- **± 2% maximum group delay variation**
- **Less than 1.5% total harmonic distortion**
- **Low-Z input switch controlled by $\overline{\text{LOW\_Z}}$ pin**
- **No external filter components required**

TIME BASE GENERATOR

- **Better than 1% frequency resolution**
- **Up to 75 MHz frequency output**
- **Independent divide-by M and N registers**
- **VCO center frequency matched to data synchronizer VCO**
- **VCO (FOUT) output available in both Read and Write mode**

DATA SEPARATOR

- **Fast acquisition phase lock loop with zero phase restart technique**
- **Fully integrated data separator**
  - **No external delay lines, active devices, or active PLL components required**
- **Programmable decode window symmetry control via serial port**
  - **Window shift control ± 30% (4-bit)**
  - **Includes delayed read MO data and VCO clock monitor points**
- **Programmable write precompensation (3-bit) (33P3734)**

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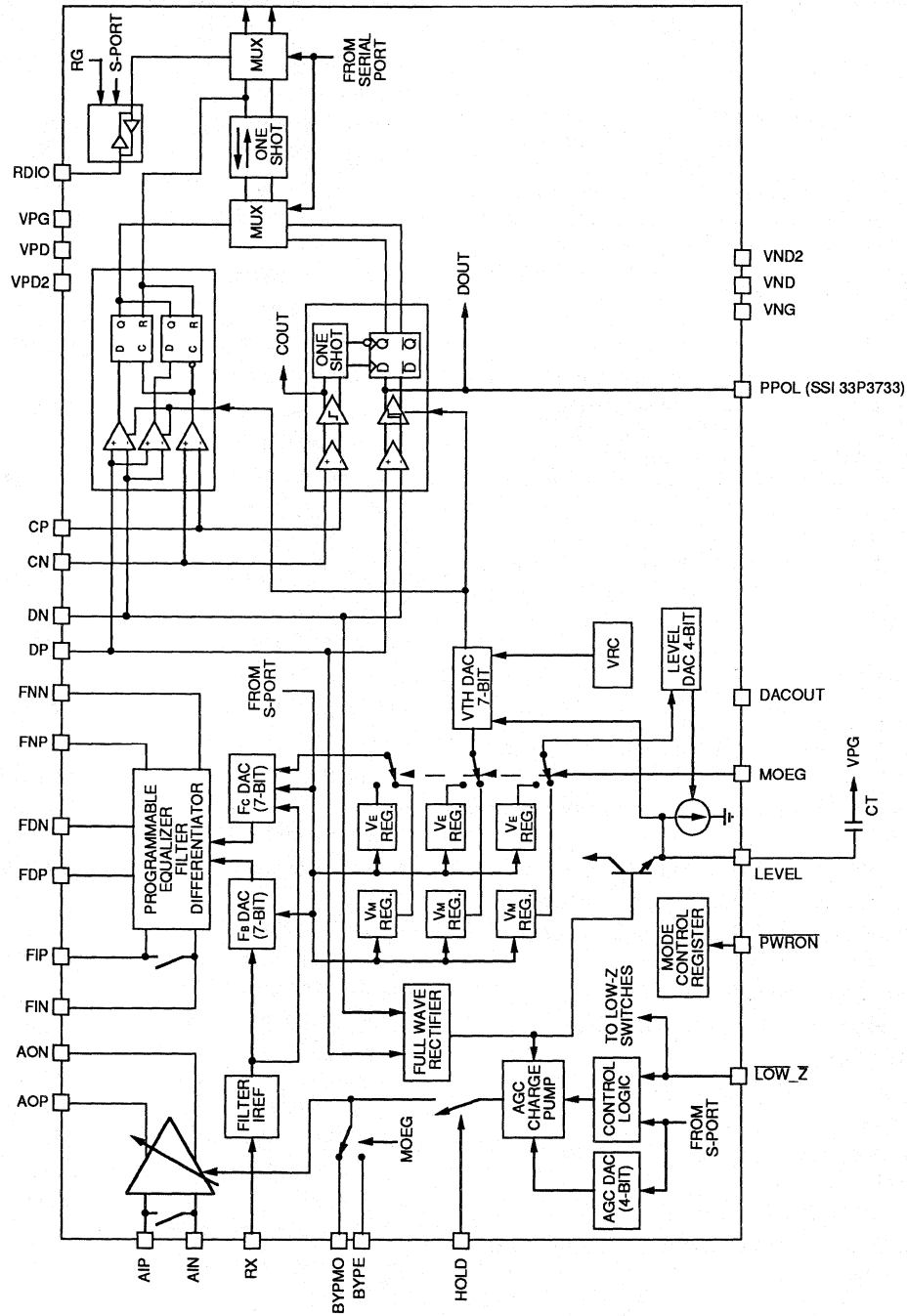

FIGURE 1A: Block Diagram, Front End

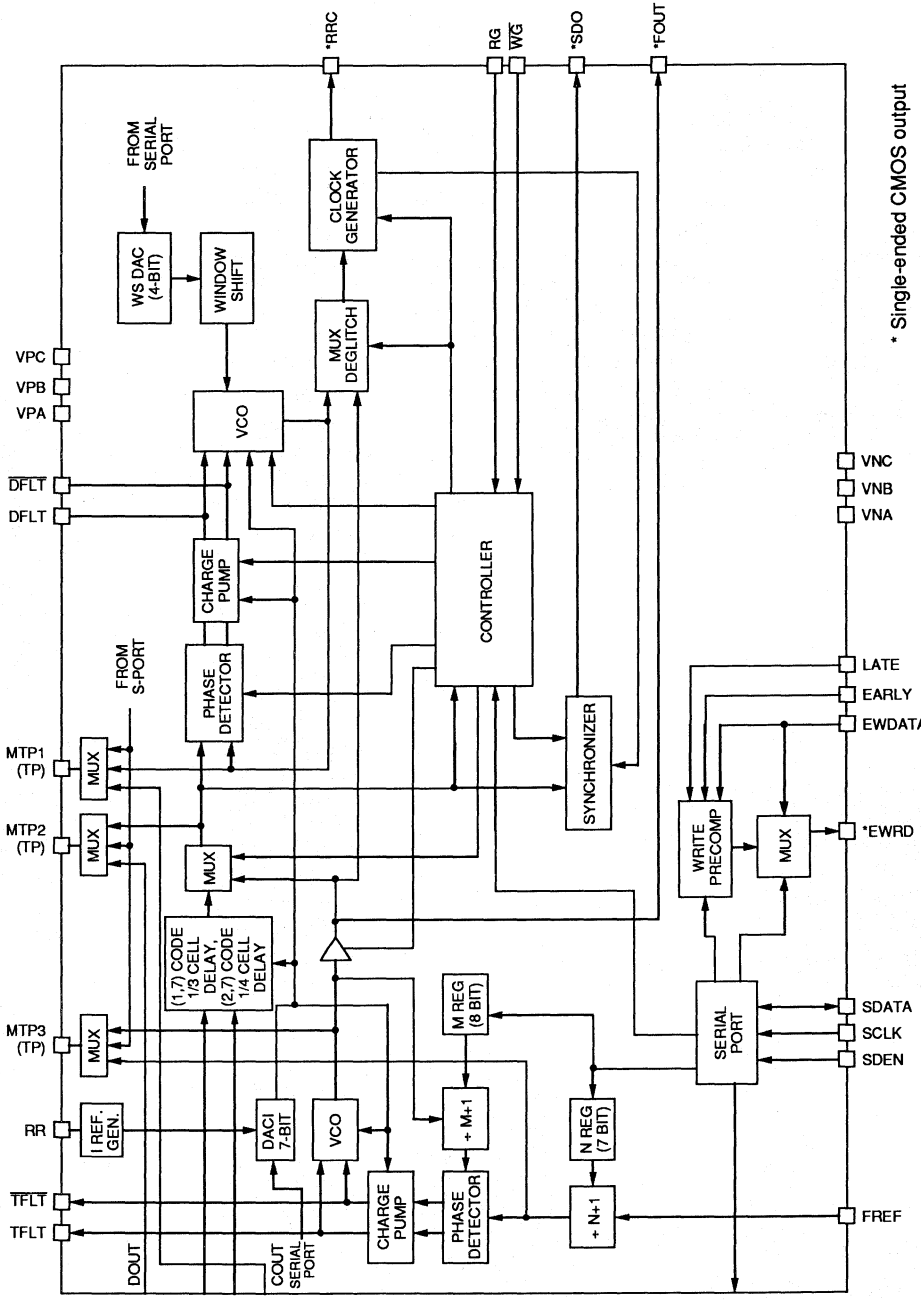

FIGURE 1B: Block Diagram, Back End

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FUNCTIONAL DESCRIPTION

The SSI 33P3733/34 implements a high performance complete read channel, including pulse detector, programmable active filter, time base generator, and data synchronizer, at MO data rates up to 26.5 Mbit/s for (1,7) code, 20 Mbit/s for (2,7) code. A circuit block diagram is shown in Figure 1.

PULSE DETECTOR CIRCUIT DESCRIPTION

The pulse detector, in conjunction with the programmable filter, provides all the MO data processing functions necessary for detection and qualification of encoded read signals. The signal processing circuits include a wide bandwidth variable gain amplifier, a precision wide bandwidth fullwave rectifier, and a dual rate charge pump. The entire signal path is fully-differential to minimize external noise pick up.

AGC CIRCUIT

The gain of the AGC amplifier is controlled by the voltage (V_{BYPx}) stored on the BYPx hold capacitor (C_{BYPx}). A dual rate charge pump drives C_{BYPx} with currents that depend on the instantaneous differential voltage at the DP/DN pins. Attack currents lower V_{BYPx} which reduces the amplifier gain, while decay currents increase V_{BYPx} which increases the amplifier gain. When the signal at DP/DN is greater than 100% of the programmed AGC level, the nominal attack current of 0.18 mA is used to reduce the amplifier gain. If the signal is greater than 125% of the programmed AGC level, a fast attack current of eight (8) times nominal is used to reduce the gain. This dual rate approach allows AGC gain to be quickly decreased when it is too high/low yet minimizes distortion when the proper AGC level has been acquired.

A constant decay current of 4 µA acts to increases the amplifier gain when the signal at DP/DN is less than the programmed AGC level. The large ratio (0.18 mA:4 µA) of the nominal attack and nominal decay currents enable the AGC loop to respond to the peak amplitudes of the incoming read signal rather than the average value. A Fast Decay Current mode is provided to allow the AGC gain to be rapidly increased, if required. In Fast Decay mode, the decay current is increased by a factor of 21.

In Read mode and Write mode, the reference voltage for the AGC charge pump is a nominal 1.0V. When MOEG is high, the reference voltage for the AGC charge pump is set by a 4-bit DAC (DACA) controlled by the serial port. The DAC output voltage is offset so that "1111" results in a 0.75V output, and "0000" results in a 1.00V output:

$$V_{AGC} = 1.00 - (DACA \times 0.01667)\ Vpp$$

where DACA is the decimal value of the DACA register

When the chip is in Power Down mode, the AGC dual rate charge pump is disabled.

Upon power up, the Low-Z/fast decay sequence should be executed to rapidly recover from any transients or drift which may have occurred on the BYPx hold capacitors.

BYPMO AND BYPE CONTROL VOLTAGE

The BYPMO capacitor voltage will be held constant (subject to leakage currents) during Sleep mode, Emboss mode (MOEG = high), Write mode, or when the HOLD signal is high. Upon the transition of $\overline{PWRON}$ from high to low, there is a 1 µs delay inserted before the AGC charge pump is allowed to drive the BYPMO capacitor. When MOEG is high, the charge pump drives the BYPE capacitor. When MOEG is low, the BYPE capacitor voltage will be held constant (subject to leakage currents).

AGC MODE CONTROL

When write gate ($\overline{WG}$) is driven low, the dual rate charge pump is disabled causing the AGC amplifier gain to be held constant. When the WG pin transitions from low to high, the LOW_Z mode can be entered using the $\overline{LOW\_Z}$ control pin. When this pin is brought low, the input impedance at both the AGC amplifier and the programmable filter are reduced to allow for quick recovery of the AC coupling capacitors. When the $\overline{LOW\_Z}$ pin goes high, the Fast Decay mode is triggered allowing rapid acquisition of the proper AGC level. The duration of the Fast Decay mode is internally set at a nominal 1 µs. Fast Decay mode is also triggered by a transition of the MO/emboss gate (MOEG) pin in either direction. When the pulse detector is powered-down, V_{BYPx} will be held constant subject to leakage currents only.

External control for enabling the dual rate charge pump is also provided. Driving the HOLD pin high forces the dual rate charge pump output current to zero. In this mode, V_{BYPx} will be held constant subject to leakage currents only.

RDIO OUTPUT PIN

A CMOS compatible, 10 ns wide (min), Raw Data Output (RDIO) signal is provided. This pin will be held low when either RG is high or WG is low to reduce noise and accompanying jitter during Read or Write modes. Its rising edge indicates the presence of a valid MO data pulse.

QUALIFIER SELECTION

The 33P3733/34 provides both hysteresis and dual comparator pulse qualification circuits that may be independently selected for Read mode and Embossed mode operation. For Read mode operation the pulse qualifier method is selected by setting the MSB in the MO data threshold control register (MODTCR). The lower 7 bits of the MODTCR also set the hysteresis level of the comparators for Read mode. For Emboss mode operation the pulse qualifier method is selected by setting the MSB in the emboss threshold control register (ETCR). The lower 7 bits of the ETCR set the hysteresis level of the comparators for Emboss mode.

DUAL COMPARATOR QUALIFICATION

When in Dual Comparator mode, independent positive and negative threshold qualification comparators are used to suppress the error propagation of a positive and negative threshold hysteresis comparator. However a slight amount of hysteresis is included to increase the comparator output time when a signal that just exceeds the threshold level is detected. This eases the timing with respect to the zero crossing clock comparator. A differential comparator with programmable hysteresis threshold allows differential signal qualification for noise rejection. The floating hysteresis threshold, VTH, is driven by a multiplying DAC which is driven by LEVEL and referenced to VRC. Hysteresis thresholds from 10 to 80% may be set with a resolution of 1%. The internal current sink LEVEL DAC (DACL) and external capacitor CT set the hysteresis threshold time constant. DACL is switched between two 4-bit registers by MO/emboss gate (MOEG) to determine the sink current magnitude in MO Data mode and Emboss mode. In MO Data mode, the four LSBs of the Hysteresis Decay Register (HDR) determine the value of the pull-down current. In Emboss mode the four MSBs are selected. The LSB value of DACL is 3.125 μA, and DACL is offset by 1 LSB such that "0000" corresponds to 3.125 μA, and "1111" results in 50 μA. A qualified signal zero crossing at the CP-CN inputs triggers the output one shot. Dual comparator timing is shown in Figure 2A.

HYSTERESIS COMPARATOR QUALIFICATION

When the Hysteresis Qualification mode is selected, the same threshold qualification comparators and clock comparators are used to implement a polarity checking rule. In this mode, a positive peak that clears the established threshold level will set the hysteresis comparator and trigger the bidirectional one-shot that creates the read MO data pulses. In order to get another pulse clocked out, a peak of the opposite polarity must clear the negative threshold level to reset the hysteresis comparator and trigger the bidirectional one-shot. Hysteresis comparator timing is shown in Figure 2B.

PROGRAMMABLE FILTER CIRCUIT DESCRIPTION

The SSI 33P3733/34 programmable filter consists of an electronically controlled low-pass filter with a separate differentiated low-pass output. A seven-pole, low-pass filter is provided along with a single-pole, single-zero differentiator. Both outputs have matched delays. The delay matching is unaffected by any amount of programmed equalization or bandwidth. Programmable bandwidth and boost/equalization is provided by internal 7-bit control DACs. The programmable characteristics are automatically switched during Emboss mode to improve signal to noise ratio. Differentiation pulse slimming equalization is accomplished by a two-pole, low-pass with a two-pole, high-pass feed forward section to provide complimentary real axis zeros. A variable attenuator is used to program the zero locations.

The filter implements a 0.05 degree equiripple linear phase response. The normalized transfer functions (i.e., $Wc = 2\pi fc = 1$) are:

$$Vnorm/Vi = [(-Ks2 + 17.98016)/D(s)] \times A_N$$

and

$$Vdiff/Vi = (Vnorm/Vi) \times (s/0.86133) \times A_D$$

where D (s)=

$$(S^2 + 1.68495s + 1.31703)(S^2 + 1.54203s + 2.95139)(S^2 + 1.14558s + 5.37034)(s + 0.86133),$$

A_N and A_D are adjusted for a gain of 2 at $fs = (2/3)fc$.

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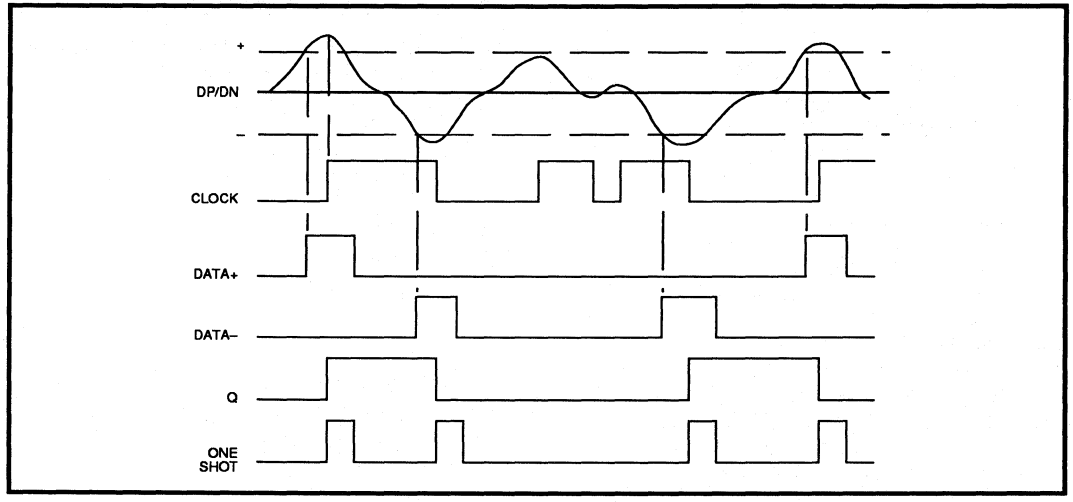

FIGURE 2A: Dual Comparator Timing Diagram

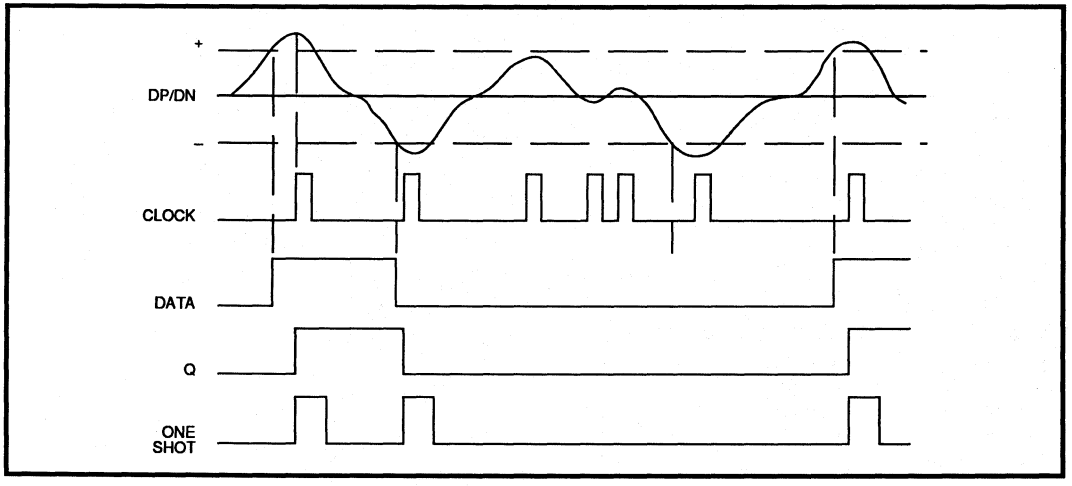

FIGURE 2B: Hysteresis Comparator Timing Diagram

FUNCTIONAL DESCRIPTION (continued)

FILTER OPERATION

AC coupled differential signals from the AGC are applied to the FIP/FIN inputs of the filter. To improve settling time of the coupling capacitors, the FIP/FIN inputs are placed into a Low-Z state when the $\overline{LOW\_Z}$ pin is brought low. The programmable bandwidth and boost/equalization features are controlled by internal DACs and the registers programmed through the serial port. The current reference for both DACs is set using a single 12.1 kΩ external resistor connected from pin RX to ground. The voltage at pin RX is proportional to absolute temperature (PTAT), hence the current for the DACs is a PTAT reference current.

BANDWIDTH CONTROL

The programmable bandwidth is set by the filter cutoff DAC. This DAC has two separate 7-bit registers that can program the DAC value as follows:

fc = 0.09449 x DACF (MHz)
where DACF = MODMCR or EMCR value

In the MO Data mode, the MO Data Mode Cutoff Register (MODMCR) is used to determine the filter's 3 dB cutoff frequency. In the Emboss mode, the Emboss Mode Cutoff Register (EMCR) is used. Switching of the registers is controlled by the MO/emboss gate (MOEG) pin. The filter cutoff set by the internal DAC is the unboosted 3 dB frequency. When boost/equalization is added, the actual 3 dB point will move out. Table 1 provides information on boost verses 3 dB frequency.

TABLE 1: 3 dB cutoff frequency versus boost magnitude

BOOST (dB)	fc (3 dB)	BOOST (dB)	fc (3 dB)
0	1.00	7	2.42
1	1.21	8	2.51
2	1.50	9	2.59
3	1.80	10	2.66
4	2.04	11	2.73
5	2.20	12	2.80
6	2.32	13	2.86

BOOST/EQUALIZATION CONTROL

The programmable equalization is also controlled by an internal DAC. The 7-bit Filter Boost Control Register (FBCR) determines the amount of equalization that will be added to the 3 dB cutoff frequency, as follows:

Boost = 20 log [(0.0273 x FBCR) + 1] (dB)

For example, with the DAC set for maximum output (FBCR = 7 fH or 127) there will be 13 dB of boost added at the 3 dB frequency. This will result in +10 dB of signal boost above the 0 dB baseline. When MOEG is active the boost can be disabled by setting bit 7 in Control A register (CAR). When bit 7 is "0" and MOEG is active the boost will automatically be set to 0 dB. If bit 7 is "1" the boost will remain at its programmed value regardless of the state of MOEG.

TIME BASE GENERATOR CIRCUIT DESCRIPTION

The time base generator, which is a PLL based circuit, provides a programmable frequency reference for constant density recording applications. The frequency can be programmed with an accuracy better than 1%. An external passive loop filter is required to control the PLL locking characteristics. The filter is fully-differential and balanced in order to suppress common mode noise generated, for example, from the data synchronizer's PLL.

In Read, Write and Idle modes, the time base generator is programmed to provide a stable reference frequency for the data synchronizer. In Read mode the internal reference clock is disabled after the data synchronizer has achieved lock and switched over to read MO data as the source for the RRC. This minimizes jitter in the data synchronizer PLL. The reference frequency is programmed using the M and N registers of the time base generator via the serial port, and is related to the external reference clock input, FREF, as follows:

Reference Frequency = ((M+1)/(N+1))FREF

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TIME BASE GENERATOR CIRCUIT DESCRIPTION (continued)

The VCO center frequency and the phase detector gain of the time base generator are controlled by an internal DAC addressed through the MO data recovery control register (MODRCR). This DAC also sets the 1/3 cell delay for (1,7) code or 1/4 cell delay for (2,7) code, VCO center frequency, and phase detector gain for the data synchronizer circuitry. When changing frequencies, the M and N registers must be loaded first, followed by the MODRCR register. A frequency change is initiated only when the MODRCR register has been changed.

$$Fvco = [12.5/(RR + 0.4)] \times [(0.622 \times IDAC) + 4.27] \text{ MHz;}$$
for $Fvco < 24$ MHz

$$Fvco = [12.5/(RR + 0.4)] \times [(0.7 \times IDAC) + 1.4] \text{ MHz}$$

where IDAC is the value in the MODRCR and RR is the value (kΩ) of the external RR resistor.

DATA SYNCHRONIZER CIRCUIT DESCRIPTION

In the Read mode, the data synchronizer performs sync field search and data synchronization. In the Write mode, the circuit provides write precompensation. Data rate is established by the time base generator and the internal reference DACI controlled by the MODRCR. The DAC generates a reference current which sets the VCO center frequency, the phase detector gain, and the 1/3 or 1/4 cell delay.

PHASE LOCKED LOOP

The circuit employs a dual mode phase detector; harmonic in the Read mode and non-harmonic in the Write and Idle modes. In the Read mode the harmonic phase detector updates the PLL with each occurrence of a $\overline{DRD}$ pulse. In the Write and Idle modes the non-harmonic phase detector is continuously enabled, thus maintaining both phase and frequency lock onto the reference frequency of the internal time base generator. By acquiring both phase and frequency lock to the input reference frequency and utilizing a zero phase restart technique, the VCO transient is minimized and false lock to DLYD DATA is eliminated. The phase detector incorporates a charge pump in order to drive the loop filter directly. The polarity and width of the output current pulses correspond to the direction and magnitude of the phase error.

The data synchronizer also requires an external passive loop filter to control its PLL locking characteristics. The filter is again fully-differential and balanced in order to suppress common mode noise which may be generated from the time base generator's PLL.

MODE CONTROL

The read gate (RG) and write gate (WG) inputs control the Device Operating mode. RG is an asynchronous input and may be initiated or terminated at any position on the disk. WG is also an asynchronous input, but should not be terminated prior to the last output write MO data pulse.

READ MODE

The data synchronizer utilizes a fully integrated fast acquisition PLL to accurately develop the decode window. Read gate (RG) initiates the PLL locking sequence and selects the PLL reference input; a high level (Read mode) selects the internal RD input and a low level selects the reference clock. In the Read mode the falling edge of $\overline{DRD}$ enables the phase detector while the rising edge is phase compared to the rising edge of the VCO reference (VCOR). $\overline{DRD}$ is a 1/3 (for (1,7) code or 1/4 for (2,7) code) cell wide (TVCO) pulse whose leading edge is defined by the falling edge of RD. A decode window is developed from the VCOR clock.

PREAMBLE SEARCH

When RG is asserted, an internal counter is triggered to count positive transitions of the incoming read MO data, RD. Once the counter reaches a count of 3, the internal read gate is enabled. This switches the phase detector reference from the internal time base to the delayed read data ($\overline{DRD}$) signal. At the same time an internal zero phase restart signal restarts the VCO in phase with the $\overline{DRD}$. This prepares the VCO to be synchronized to MO data when the bit sync circuitry is enabled after VCO lock is established.

VCO LOCK AND BIT SYNC ENABLE

One of two VCO locking modes will be entered depending on the state of the gain shift (GS) bit, or bit 1, in the Control B register. If GS = "1", the phase detector will enter a gain shift mode of operation. The phase detector starts out in a high gain mode of operation to support fast phase acquisition. After an internal counter counts the first 11 transitions of the internal $\overline{DRD}$ signal, the gain is reduced by a factor of 3. This reduces the bandwidth and dampening factor of the loop by $\sqrt{3}$ which provides improved jitter performance in the MO data follow mode. The counter continues to count the next 5 $\overline{DRD}$ transitions (a total of 19 pulses from assertion of RG) and then asserts an internal VCO lock signal.

When the VCO lock signal is asserted, the internal RRC source is also switched from the time base generator to the VCO clock signal that is phase locked to $\overline{DRD}$. During the internal RRC switching period the external RRC signal may be held for a maximum of 2 VCO clock periods, however no short duration glitches will occur.

When the GS bit is set to "0" the phase detector gain shift function is disabled. The VCO lock sequence is identical to that of the gain shift mode explained above, except that no gain shift is made after the first 11 transitions.

WINDOW SHIFT

Shifting the phase of the VCO clock effectively shifts the relative position of the $\overline{DRD}$ pulse within the decode window. Decode window control is provided via the WS control bits of the Window Shift Control Register (WSCR). Further description of the WSCR is provided in the window shift control section.

NON-READ MODE

In the Non-Read modes, the PLL is locked to the reference clock. This forces the VCO to run at a frequency which is very close to that required for tracking actual MO data. When the reference input to the PLL is switched, the VCO is stopped momentarily, then restarted in an accurate phase alignment with the next PLL reference input pulse. By minimizing the phase alignment error in this manner, the acquisition time is substantially reduced.

WRITE MODE (SSI 33P3734)

Write mode is entered by asserting the write gate ($\overline{WG}$) while the RG is held low. During Write mode the VCO and the RRC are referenced to the internal time base generator signal.

DIRECT WRITE FUNCTION

The SSI 33P3734 includes a Direct Write (DW) function that allows the EWDATA MO data to bypass the write precomp circuitry. When the D3 bit of the WPR is set to zero, the MO data applied to EWDATA will bypass the write precomp and directly control the EWRD output buffer. This allows the user to perform DC erase and media tests.

OPERATING MODES AND CONTROL

The SSI 33P3733/34 has several operating modes that support Read, Write, Emboss, and power management functions. Mode selection is accomplished by controlling the read gate (RG), write gate ($\overline{WG}$), MO/emboss gate (MOEG), and $\overline{PWRON}$ pins. Additional modes are also controlled by programming the Power Down Control Register (PDCR), the Control A register (CAR), and the Control B register (CBR) via the serial port.

EXTERNAL MODE CONTROL

All operating modes of the device are controlled by driving the read gate (RG), write gate ($\overline{WG}$), MO/emboss gate (MOEG), and $\overline{PWRON}$ pins with TTL compatible signals. For normal operation the $\overline{PWRON}$ pin is driven low. During normal operation the SSI 33P3733/34 is controlled by the read gate (RG), write gate ($\overline{WG}$), and MO/emboss gate (MOEG) pins. When RG is high and $\overline{WG}$ is high the device is in Read mode. When $\overline{WG}$ is low and RG is low the device is in Write mode. If the RG is low and $\overline{WG}$ is high the device will be in Idle mode. During the Idle mode, the MOEG pin can be activated to enable the Emboss mode of operation.

FUNCTIONAL DESCRIPTION (continued)

POWER DOWN CONTROL

For power management, the $\overline{\text{PWRON}}$ pin can be used in conjunction with the Power Down Control Register (PDCR) to set the operating mode of the device. The PDCR provides a control bit for each of the functional blocks. When the $\overline{\text{PWRON}}$ pin is brought high ("1") the device is placed into Sleep mode (<5 mW) and all circuits are powered down except the serial port. This allows the user to program the serial port registers while still conserving power. Register information is retained during the Sleep mode so it is not necessary to reprogram the serial port registers after returning to an active mode. When the $\overline{\text{PWRON}}$ pin is driven low ("0"), the contents of the PDCR determine which blocks will be active. Register mapping for the PDCR is shown in Table 3. To improve recovery time from the Sleep mode, the $\overline{\text{LOW\_Z}}$ pin should be asserted following power down to initiate the AGC recovery sequence.

SERIAL INTERFACE OPERATION

The serial interface is a CMOS bi-directional port for reading and writing programming data from/to the internal registers of the SSI 33P3733/34. The serial port data transfer format is shown in Figure 3. For data transfers SDEN is brought high, serial data is presented at the SDATA pin, and a serial clock is applied to the SCLK pin. After the SDEN goes high, the first 16 pulses applied to the SCLK pin will shift the data presented at the SDATA pin into an internal shift register on the rising edge of each clock. An internal counter prevents more than 16 bits from being shifted into the register. The data in the shift register is latched when SDEN goes low. If less than 16 clock pulses are provided before SDEN goes low, the data transfer is aborted.

All transfers are shifted into the serial port LSB first. The first byte of the transfer is address and instruction information. The LSB of this byte is the R/W bit which determines if the transfer is a read (1) or a write (0). The remaining 7-bits determine the internal register to be accessed. Table 3 provides register mapping information. The second byte contains the programming data. In Read mode (R/W=1) the SSI 33P3733/34 will output the register contents of the selected address. In Write mode the device will load the selected register with data presented on the SDATA pin. At initial power-up, the contents of the internal registers will be in an unknown state and must be programmed prior to operation. During power down modes, the serial port remains active and register programming data is retained. Detailed timing information is provided in Figure 4.

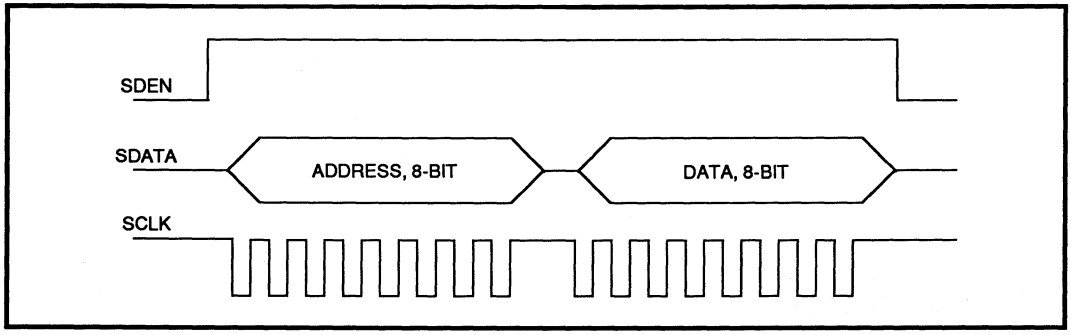

FIGURE 3: Serial Port Data Transfer Format

TABLE 2: MODE CONTROL

CONTROL LINE				DEVICE MODE	DAC CONTROL			
$\overline{PWRON}$	RG	MOEG	$\overline{WG}$		VTH	FC	BOOST	HYSTERESIS
1	X	X	X	**SLEEP MODE:** All functions are powered down. The serial port registers remain active and register programming data is saved.	off	off	off	off
0	0	0	0	**WRITE MODE:** The pulse detector is inactive. The data synchronizer VCO is locked to the internal time base generator. Write precomp circuit is clocked by internal time base. (SSI 33P3734)	MR	MR	MR	MR
0	1	0	1	**READ MODE:** The pulse detector is active. The data synchronizer begins the preamble lock sequence. RDIO is active	MR	MR	MR	MR
0	0	1	1	**EMBOSS MODE:** The pulse detector is active and the emboss control registers are enabled for the Fc DAC and the VTH DAC. The data synchronizer and time base generator can be disabled using the PDCR.	ER	ER	off	ER
0	0	0	1	**IDLE MODE:** The contents of the PDCR determine which blocks are powered-up. In normal operation with all blocks powered-up, the pulse detector is active, the data synchronizer VCO is locked to the time base generator, and the MO data control registers are used for VTH and FC.	MR	MR	MR	MR
-	-	-	-	All other states are illegal. If an illegal state is programmed, the chip function will be in an indeterminable state, but no damage will occur.	MR	MR	MR	MR

DAC CONTROL KEY: MR = MO DATA REGISTER, ER = EMBOSS RIGISTER, OFF = DISABLED

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REGISTER NAME	A6			ADDRESS			A0	R/W	D7	DATA BIT MAP						D0
POWER DOWN CONTROL	0	0	0	0	0	1	0	0	--	--	--	TBG 1=DISABLE 0=ENABLE	DATA SEP 1=DISABLE 0=ENABLE	FILTER 1=DISABLE 0=ENABLE	--	PD 1=DISABLE 0=ENABLE
MO DATA MODE CUTOFF	0	0	0	0	0	1	1	0	--	F_{CM} DAC BIT 6	F_{CM} DAC BIT 5	F_{CM} DAC BIT 4	F_{CM} DAC BIT 3	F_{CM} DAC BIT 2	F_{CM} DAC BIT 1	F_{CM} DAC BIT 0
EMBOSS MODE CUTOFF	0	0	1	0	0	1	1	0	--	F_{CE} DAC BIT 6	F_{CE} DAC BIT 5	F_{CE} DAC BIT 4	F_{CE} DAC BIT 3	F_{CE} DAC BIT 2	F_{CE} DAC BIT 1	F_{CE} DAC BIT 0
FILTER BOOST	0	0	0	1	0	1	1	0	EMBOSS BOOST 1=ENABLE 0=DISABLE	F_BDAC BIT 6	F_B DAC BIT 5	F_B DAC BIT 4	F_B DAC BIT 3	F_B DAC BIT 2	F_B DAC BIT 1	F_B DAC BIT 0
MO DATA THRESHOLD	0	0	0	1	0	1	0	0	1=DUAL 0=HYS	T_MDAC BIT 6	T_M DAC BIT 5	T_M DAC BIT 4	T_M DAC BIT 3	T_M DAC BIT 2	T_M DAC BIT 1	T_M DAC BIT 0
EMBOSS THRESHOLD	0	0	1	0	0	1	0	0	1=DUAL 0=HYS	T_EDAC BIT 6	T_E DAC BIT 5	T_E DAC BIT 4	T_E DAC BIT 3	T_E DAC BIT 2	T_E DAC BIT 1	T_E DAC BIT 0
CONTROL A	0	0	1	1	0	1	0	0	Fast Decay test mode 0=ENABLE	TMS1	TMS0	TBG 1=BYPASS 0=NORMAL	TBG TEST POINT ENABLE	PUMP DWN 1=TP ON 0=TP OFF	PUMP UP 1=TP ON 0=TP OFF	PHASE DET 1=ENABLE 0=DISABLE
CONTROL B	0	0	0	1	1	0	0	0	--	MTPE 1=ENABLE 0=DISABLE	PUMP DWN 1=TP ON 0=TP OFF	PUMP UP 1=TP ON 0=TP OFF	PHASE DET 1=ENABLE 0=DISABLE	RDIO 1 = INPUT 0 = OUTPUT	GAIN SHFT 1 = ON 0 = OFF	--
N COUNTER	0	0	0	0	1	1	0	0	--	N COUNT BIT 6	N COUNT BIT 5	N COUNT BIT 4	N COUNT BIT 3	N COUNT BIT 2	N COUNT BIT 1	N COUNT BIT 0
M COUNTER	0	0	0	1	1	1	0	0	M COUNT BIT 7	M COUNT BIT 6	M COUNT BIT 5	M COUNT BIT 4	M COUNT BIT 3	M COUNT BIT 2	M COUNT BIT 1	M COUNT BIT 0
DATA RECOVERY	0	0	0	0	1	0	0	0	--	DAC I BIT 6	DAC I BIT 5	DAC I BIT 4	DAC I BIT 3	DAC I BIT 2	DAC I BIT 1	DAC I BIT 0
WINDOW SHIFT	0	0	0	0	1	0	1	0	TDAC 1	TDAC 0	WIN SHFT 1=ENABLE 0=DISABLE	WS DIR 1=LATE 0=EARLY	$\overline{WS3}$	$\overline{WS2}$	$\overline{WS1}$	$\overline{WS0}$
WRITE PRECOMP	0	0	0	1	1	0	1	0	--	$\overline{WL2}$	$\overline{WL1}$	$\overline{WL0}$	WR PRCMP 1=ENABLE 0=DISABLE	$\overline{WE2}$	$\overline{WE1}$	$\overline{WE0}$
AGC LEVEL	0	1	0	0	0	1	0	0	--	--	--	--	AGC DAC BIT 3	AGC DAC BIT 2	AGC DAC BIT 1	AGC DAC BIT 0
HYSTERESIS DECAY	0	1	0	1	0	1	0	0	EMBOSS BIT 3	EMBOSS BIT 2	EMBOSS BIT 1	EMBOSS BIT 0	DATA BIT 3	DATA BIT 2	DATA BIT 1	DATA BIT 0

TABLE 3: Serial Port Register Mapping

FUNCTIONAL DESCRIPTION (continued)

CONTROL REGISTERS

Control registers CAR and CBR allow the user to configure the SSI 33P3733/34 test points for evaluation of different internal signals and also control other device functions. CAR controls functions of the pulse detector, filter, and time base generator. CBR controls test points and functions of the data separator. The bits of the CA and CB registers are defined as follows:

CONTROL REGISTER CA

BIT	NAME	FUNCTION
0	EPDT	Enable Phase Detector (Time Base Generator)
1	UT	Pump Up (TFLTR sources current, $\overline{\text{TFLTR}}$ sinks Current)
2	DT	Pump Down (TFLTR sinks current, $\overline{\text{TFLTR}}$ sources Current)
3	ET	Enable Time Base Generator Test Point Output
4	BYPT	Bypass Time Base Generator Circuit Function
5	TMS0	Control bit for selecting test point source (see Table 4)
6	TMS1	Control bit for selecting test point source (see Table 4)
7	FDTM	Constant fast decay current test mode

CONTROL REGISTER CB

0	-	Not Used
1	GS	Enable Phase Detector Gain Switching
2	RDI	RDIO Pin Input Control
3	EPDD	Enable Phase Detector (Data Separator)
4	UD	Pump Up (DFLTR sources current, $\overline{\text{DFLTR}}$ sinks current)
5	DD	Pump Down (DFLTR sinks current, $\overline{\text{DFLTR}}$ sources current)
6	MTPE	Enable Test Points MTP1, 2, 3 (see Table 4)
7	-	Not used

PIN DESCRIPTION

POWER SUPPLY PINS

NAME	TYPE	DESCRIPTION
VPA	-	Data separator PLL analog power supply pin
VPB	-	Time base generator PLL analog power supply pin
VPC	-	Internal ECL, CMOS logic power supply pin
VPD, VPD2	-	CMOS buffer I/O digital power supply pin
VPG	-	Pulse detector, filter, analog power supply pin
VNA	-	Data separator PLL analog ground pin
VNB	-	Time base generator PLL analog ground pin
VNC	-	Internal ECL, CMOS logic ground pin
VND, VND2	-	CMOS buffer I/O digital ground pin
VNG	-	Pulse detector, filter, analog ground pin

INPUT PINS

AIP, AIN	I	AGC AMPLIFIER INPUTS: Differential AGC amplifier input pins.
DP, DN	I	ANALOG INPUTS FOR MO DATA PATH: Differential analog inputs to MO data comparators, full-wave rectifier.
CP, CN	I	ANALOG INPUTS FOR CLOCK PATH: Differential analog inputs to the clock comparator.
$\overline{\text{LOW\_Z}}$	I	LOW IMPEDANCE ENABLE: TTL compatible input pin that activates the Low-Z switches. A low level activates the switches and the falling edge of the internal LOW_Z triggers the fast decay circuit.
$\overline{\text{PWRON}}$	I	POWER ENABLE: TTL compatible power control input. A low level input enables power to circuitry according to the contents of the PDCR. A high level input shuts down all circuitry.
HOLD	I	HOLD CONTROL: TTL compatible control pin which, when pulled high, disables the AGC charge pump and holds the AGC amplifier gain at its present value.
FIP, FIN	I	FILTER SIGNAL INPUTS: The AGC output signals must be AC coupled into these pins.
FREF	I	REFERENCE FREQUENCY INPUT: Frequency reference input for the time base generator. FREF may be driven either by a direct coupled TTL signal or by an AC coupled ECL signal. Pin FREF has an internal pull down resistor.
EWDATA	I	WRITE INPUT: TTL compatible write MO data input. (SSI 33P3734)
EARLY, LATE	I	WRITE PRECOMPENSATION CONTROL: TTL compatible inputs. The EARLY and LATE signals control on-the-fly precompensation of the EWDATA. (SSI 33P3734)

INPUT PINS (continued)

NAME	TYPE	DESCRIPTION
RG	I	READ GATE: TTL compatible read gate input. A high level TTL input selects the RD input and enables the Read mode/address detect sequences. A low level selects the FREF input.
MOEG	I	MO/emboss GATE: TTL compatible MO/emboss gate input. A high level TTL input activates the Emboss mode by selecting the emboss control registers, the RTS resistor, and the BYPE capacitor.
$\overline{WG}$	I	WRITE GATE: TTL compatible write gate input. A low level TTL input enables the Write mode.

OUTPUT PINS

MTP1-3	O	MULTIPLEXED TEST POINTS: Open emitter ECL output test points. Internal test signals are routed to these test points as determined by the CAR and CBR. External resistors are required to use these pins. They should be removed during normal operation to reduce power dissipation.
SDO	O	SYNCHRONIZED READ DATA: CMOS output pin. Read MO data output when RG is high.
FDP, FDN	O	DIFFERENTIAL DIFFERENTIATED OUTPUTS: Filter differentiated outputs. These outputs are AC coupled into the CP/CN inputs.
FNP, FNN	O	DIFFERENTIAL NORMAL OUTPUTS: Filter normal low pass output signals. These outputs are AC coupled into the DP/DN inputs.
RDIO	I/O	READ MO DATA I/O: Bi-directional CMOS output / TTL compatible input pin. RDIO is an output when RG is low and the RDIO bit is low in the CBR. RDIO is an input when the RDIO bit is high in the CBR. The minimum RDIO input pulse width is TBD ns. The RG and pulse detector functions override the bit in the CBR. When RDIO is used as an input pin, 1/3 or 1/4 cell delay in the data synchronizer is made from the rising edge.
RRC	O	READ REFERENCE CLOCK: Read clock CMOS output. During a mode change, no glitches are generated and no more than one lost clock pulse will occur. When RG goes high, RRC initially remains synchronized to the reference clock. When the Sync Bits are detected, RRC is synchronized to the Read MO Data. When RG goes low, RRC is synchronized back to the reference clock.
AOP, AON	O	AGC AMPLIFIER OUTPUT: Differential AGC amplifier output pins. These outputs are AC coupled into the filter inputs (FIP/FIN).
EWRD	O	WRITE MO DATA: Encoded write MO data CMOS output. When direct write is active EWRD is directly driven by EWDATA.
FOUT	O	TIME BASE GENERATOR VCO OUTPUT: CMOS output pin. This clock signal is the data separator PLL reference. This output is independent of the RG/WG pin.
PPOL	O	PULSE POLARITY: Pulse polarity CMOS output pin. The output is high when the pulse being qualified is positive and it is low when the pulse being qualified is negative. (SSI 33P3733)

PIN DESCRIPTION (continued)

ANALOG PINS

NAME	TYPE	DESCRIPTION
BYPMO	-	The AGC Read mode integration capacitor CBYPMO, is connected between BYPMO and VPG.
BYPE	-	The AGC Emboss mode integration capacitor CBYPE, is connected between BYPE and VPG.
DACOUT	-	DAC VOLTAGE TEST POINT: This test point monitors the outputs of the internal DACs. The source DAC is selected by programming the two MSBs of the WSCR register (see Table 5).
TFLT, $\overline{\text{TFLT}}$	-	PLL LOOP FILTER: These pins are the connection points for the time base generator loop filter.
DFLT, $\overline{\text{DFLT}}$	-	PLL LOOP FILTER: These pins are the connection points for the data separator loop filter.
LEVEL	-	An NPN emitter output that provides a full-wave rectified signal from the DP, DN inputs. An external capacitor should be connected from LEVEL to VPG to set the hysteresis threshold time constant in conjunction with the internal current DAC, (DACA).
RR	-	REFERENCE RESISTOR INPUT: An external 12.1 kΩ, 1% resistor is connected from this pin to VNA to establish a precise internal reference current for the data separator and time base generator.
RX	-	REFERENCE RESISTOR INPUT: An external 12.1 kΩ, 1% resistor is connected from this pin to ground to establish a precise PTAT (proportional to absolute temperature) reference current for the filter.

SERIAL PORT PINS

SDEN	-	SERIAL DATA ENABLE: Serial enable CMOS input. A high level TTL input enables the serial port.
SDATA	-	SERIAL DATA: Serial data CMOS input. NRZ programming data for the internal registers is applied to this input.
SCLK	-	SERIAL CLOCK: Serial clock CMOS input. The clock applied to this pin is synchronized with the data applied to SDATA.

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, the recommended operating conditions are as follows: 4.5V < POSITIVE SUPPLY VOLTAGE < 5.5V, 0°C < T (ambient) < 70°C, and 25°C < T(junction) < 135°C. Currents flowing into the chip are positive. Current maximum are currents with the highest absolute value.

ABSOLUTE MAXIMUM RATINGS

Operation above maximum ratings may damage the device.

PARAMETER	RATING
Storage Temperature	-65 to 150°C
Junction Operating Temperature	+135°C
Positive Supply Voltage (Vp)	-0.5 to 7V
Voltage Applied to Logic Inputs	-0.5V to Vp + 0.5V
All other Pins	-0.5V to Vp + 0.5V

POWER SUPPLY CURRENT AND POWER DISSIPATION

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
ICC (VPA,B,C,D,G)	Outputs and test point pins open, Ta = 27°C, VPn = 5V, 24 Mbit/s		75		mA
PWR Power Dissipation	Outputs and test point pins open, Ta = 27°C, VP = 5V, 24 Mbit/s		375		mW
Sleep mode Power	$\overline{\text{PWRON}}$ = 1			5	mW
Emboss mode Power	$\overline{\text{PWRON}}$ = 0 TBG Disabled Data Sep. Disabled		200		mW

DIGITAL INPUTS AND OUTPUTS

TTL COMPATIBLE INPUTS

Input low voltage	VIL		-0.3		0.8	V
Input high voltage	VIH		2		VPD + 0.3	V
Input low current	IIL	VIL = 0.4V			-100	µA
Input high current	IIH	VIH = 2.4V			50	µA

CMOS COMPATIBLE INPUTS - Schmitt trigger type (not to be left open.) Nominal 1.0V hysteresis around VPD/2.

Input low voltage		-0.3		1.5	V
Input high voltage		3.5		VPD + 0.3	V

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DIGITAL INPUTS AND OUTPUTS (continued)

CMOS COMPATIBLE OUTPUTS

Output low voltage	5V, 25°C IOL = 4.07 mA			0.5	V
Output high voltage	5V, 25°C IOH = -4.83 mA	4.5			V
Rise time	4.5V, 70°C, C = 15 pF			8	ns
Fall time	4.5V, 70°C, C = 15 pF			8	ns

PSEUDO ECL OUTPUT LEVELS (MTP1, MTP2, MTP3)
For all tests, 261Ω to VPA and 402Ω to VNA with VPA = 5.0V

Output high level		VPA -1.02			V
Output low level				VPA -1.62	V

SERIAL PORT

SCLK period	T_{CLK}		100			ns
SCLK low time	T_{CKL}		40			ns
SCLK high time	T_{CKH}		40			ns
Enable to SCLK	T_{SENS}		35			ns
SCLK to disable	T_{SENH}		35			ns
Data set-up time	T_{DS}		15			ns
Data hold time	T_{DH}		15			ns
SDATA tri-state delay	T_{SENDL}				50	ns
SDATA turnaround time	T_{TRN}		70			ns
SDEN low time	T_{SL}		200			ns

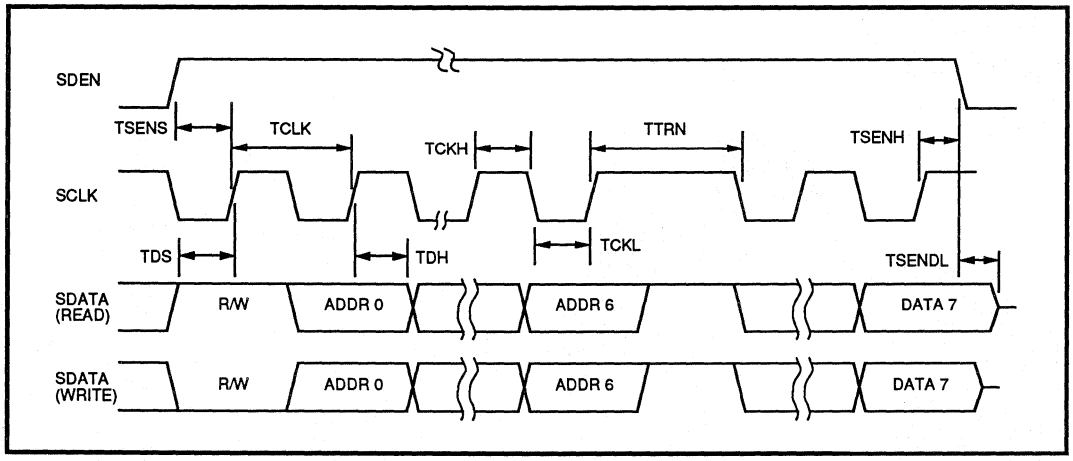

FIGURE 4: Serial Port Timing Information

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ELECTRICAL SPECIFICATIONS (continued)

PULSE DETECTOR CHARACTERISTICS

AGC AMPLIFIER

Input signals are AC coupled to AIP/AIN, AOP/AON outputs are AC coupled to FIP/FIN, and FNP/FNN are AC coupled to DP/DN. 1000 pF capacitors are connected from BYPMO to VPG (C_{BYPMO}) and from BYPE to VPG (C_{BYPE}). Unless otherwise specified, outputs are measured differentially at AOP/AON, FIN = 8 MHz, and filter boost = 0 dB.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Input range	Filter boost 0 to 13 dB	20		190	mVpp
DP-DN voltage	AIP - AIN = 0.1 Vpp	0.9	1	1.1	Vpp
	MOEG = high, AGC DAC = 0	0.9	1	1.1	Vpp
	MOEG = high, AGC DAC = 15	0.68	0.76	0.84	Vpp
DP-DN voltage variation	20 mV < AIP - AIN < 190 mV			8	%
Gain range		0.45		18	V/V
Gain sensitivity	BYPx voltage change		28		dB/V
AOP-AON dynamic range	THD = 1%	0.6			Vpp
Differential input impedance	$\overline{LOW\_Z}$ = high	4.7	6	8.4	kΩ
	$\overline{LOW\_Z}$ = low		350		Ω
Single-ended input impedance	$\overline{LOW\_Z}$ = high		3.3		kΩ
	$\overline{LOW\_Z}$ = low		250		Ω
Single-ended output impedance	AOP/AON to ground			120	Ω
Output offset voltage variation	Gain = 0.45 to 18			200	mV
Input noise voltage	Gain = 18, AOP - AON = 0V			20	nV/√Hz
Bandwidth	Gain = 18, CL ≤ 15 pF	35			MHz
CMRR Gain = 18, fc = 5 MHz		40			dB
PSRR Gain = 18, fc = 5 MHz		45			dB
Gain decay time	AIP - AIN = 250 to 125 mV, AOP - AON > 0.9 Final Value		36		µs
Gain attack time	AIP - AIN = 125 to 250 mV, AOP - AON < 1.1 Final Value		0.65		µs

AGC CONTROL

The input signals are AC coupled into DN/DP, C_{BYPX} = 1000 pF to VPG, MOEG = low.

DP-DN input range	For test only		1	1.5	Vpp
Decay current	Normal decay I_D		4		µA
	Fast Decay mode I_{DF}		21 x I_D		µA
Attack current	Normal attack I_{CH}		0.18		mA
	Fast Attack mode I_{CHF}		8 x I_{CH}		mA

AGC CONTROL (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
BYPMO leakage current	$\overline{WG}$ = high	-10		10	nA
Fast decay duration			1		µs
LEVEL output gain	|DP-DN| = 0.5 to 1.5V	0.60	0.65	0.70	V/Vpp
LEVEL output bandwidth	-1 dB	10			MHz
LEVEL pin pull-down current	DACL = 0000	1.56	3.125	4.69	µA
	DACL = 1111 where I_{LEVEL} = 3.125 x (1 + DACL) µA	47	50	53	µA

DATA COMPARATOR

The input signals are AC coupled into DP/DN.

DP-DN input range			1	1.5	Vpp
Differential input resistance	$\overline{LOW\_Z}$ = Off	8.0		14	kΩ
	$\overline{LOW\_Z}$ = On	0.4		1.2	kΩ
Differential input capacitance				5	pF
Threshold voltage hysteresis			10		%T
Threshold voltage gain (K_{TH}) tolerance	0.47 < |DP - DN| < 1.19 T = V_{THDAC} x 0.93/127 38 < V_{THDAC} < 127	T - 10		T + 10	%
Minimum threshold voltage	|DP - DN| < 0.16 V_{THMIN} = V_{THDAC} • 97.6%/127		V_{THMIN}		V
PPOL rise time (SSI 33P3733)	10% to 90% points, CL ≤ 15 pF			8	ns
PPOL fall time (SSI 33P3733)	90% to 10% points, CL ≤ 15 pF			8	ns

CLOCK SECTION

The input signals are AC coupled into CP/CN.

CP-CN input range				1.5	Vpp
Comparator offset voltage		-4		4	mV
Differential input resistance		8		14	kΩ
Differential input capacitance				5	pF
Pulse pairing	DP/DN = 1 Vpp sine, CP/CN = 1 Vpp - 90°sine Fsine = 8 MHz			0.5	ns
RDIO pulse width	CL ≤ 15 pF	6		15	ns
RDIO input pulse width		10			ns
RDIO rise time	10% to 90% points, CL ≤ 15 pF			8	ns
RDIO fall time	90% to 10% points, CL ≤ 15 pF			8	ns

PULSE DETECTOR CHARACTERISTICS (continued)

PROGRAMMABLE FILTER CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Filter cutoff range	fc @ -3 dB point fc = (0.09449 MHz) x DACF, Boost = 0 dB 42 ≤ DACF ≤ 127 DACF = MODMCR	4		12	MHz
Filter cutoff accuracy	DACF = 127	-10		10	%
	DACF = 42 to DACF < 127	-15		15	%
FNP, FNN differential gain (A_N)	F = 0.67 x fc, boost = 0 dB	1.6	2	2.4	V/V
FDP, FDN differential gain (A_D)	F = 0.67 x fc, boost = 0 dB	0.8 A_N		1.2 A_N	V/V
Frequency boost @ fc = 12 MHz	DACS = 127		13		dB
Boost accuracy	@ 6 dB, DACS = 37	-1		+1	dB
	@ 9 dB, DACS = 67	-1.25		+1.25	dB
	@ 13 db, DACS = 127	-1.5		+1.5	dB
MO/Emboss mode group delay variation	fc = 4 to 12 MHz F = 0.2 fc to fc, boost = 0 and 3 dB	-2		+2	%
FNP, FNN; FDP, FDN	fc = 4 to 12 MHz F = fc to 1.75 fc, boost = 3 dB	-3		+3	%
Filter Output THD @ 1 Vpp	F = 0.67 fc fc = 4 to 12 MHz			1.5	%
Filter differential input resistance	Normal	3			kΩ
	Low-Z		140		Ω
Filter differential input capacitance				7	pF
Output noise voltage	BW = 100 MHz, Rs = 50Ω				
differentiated output	fc = 12 MHz, boost = 0 dB		2.6		mV Rms
differentiated output	fc = 12 MHz, boost = 13 dB		5.6		mV Rms
normal output	fc = 12 MHz, boost = 0 dB		2		mV Rms
normal output	fc = 12 MHz, boost = 13 dB		3.6		mV Rms
Filter output sink current			0.5		mA
Filter output offset voltage				200	mV
Filter output source current		2			mA
Filter output resistance	Single ended			200	Ω
Rx pin voltage	Ta = 27°C		600		mV
	Tj = 127°C		800		mV
Rx resistance 1% fixed value			12.1		kΩ

TIME BASE GENERATOR CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
FREF input range		8		20	MHz
FOUT frequency range				75	MHz
FOUT jitter	TOUT = 1/FOUT Loop acquisition time = 30 µs	-TBD goal = 200		+TBD goal = 200	ps (rms)
M counter range		2		255	
N counter range		2		127	
VCO center frequency TVCO period	FVCO = [12.5/(RR + 0.4)] x [(0.622 x IDAC)+ 4.27] MHz TFLT - $\overline{TFLT}$ = TBD FVCO < 24 MHz FVCO = [12.5/(RR + 0.4)] x [(0.7 x IDAC) + 1.4] MHz	0.85 T0		1.15 T0	ns
VCO dynamic range	-2V ≤ TFLT - $\overline{TFLT}$ ≤ +2V FOUT = 36 MHz RR = 12.1 kΩ	±25		±45	%
VCO control gain KVCO	ωi = 2π/TVCO -2V ≤ TFLT - $\overline{TFLT}$ ≤ +2V	0.12 ωi		0.24 ωi	rad/(V-S)
Phase detector gain KD	KD = [12.5/(RR+0.4)] x (0.656 x IDAC + 3.38) x 10^{-6}	0.83 KD		1.17 KD	A/rad
KVCO x KD product accuracy		-28		+28	%
RR resistor range			12.1		kΩ
FREF input low time		20			ns
FREF input high time		20			ns
FOUT rise time	10% to 90% points, CL ≤ 20 pF			8	ns
FOUT fall time	90% to 10% points, CL ≤ 20 pF			8	ns

DATA SYNCHRONIZER CHARACTERISTICS

READ MODE

Read clock rise time	TRRC	10% to 90% points CL ≤ 15 pF			8	ns
Read clock fall time	TFRC	90% to 10% points CL ≤ 15 pF			8	ns
RRC duty cycle	TRD	Except during re-sync	40		60	%
		During re-sync	40			%
SD0 out set-up and hold time	TSDS, TSDH		10			ns
1/3 or 1/4 cell delay		TD = TVCO/2	0.8 TD		1.2 TD	ns

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DATA SYNCHRONIZER CHARACTERISTICS (continued)

WRITE MODE (SSI 33P3734)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Write MO data pulse width TWD	1.5V, CL ≤ 15 pF	TVCO -0.5		TVCO +0.5	ns
Write MO data rise time TRWD	10% to 90% points, CL ≤ 15 pF			8	ns
Write MO data fall time TFWD	90% to 10% points, CL ≤ 15 pF			8	ns
EARLY, LATE set-up time TSEL		5			ns
EARLY, LATE hold time THEL		5			ns
Write MO data input rise time TRWC	0.8 to 2V CL ≤ 15 pF			10	ns
Write MO data input fall time TFWC	2 to 0.8V, CL ≤15 pF			8	ns
Write MO data jitter	24 Mbit/s, 3T	-1		1	ns

DATA SYNCHRONIZATION

VCO center frequency period TVCO	FVCO = [12.5/(RR + 0.4)] x [(0.622 x IDAC) + 4.27] MHz TVCO = 1/FVCO, DFLT - $\overline{DFLT}$ = TBD RR = 12.1 kΩ FVCO < 24 MHz FVCO = [12.5/(RR + 0.4)] x [(0.7 x IDAC) + 1.4] MHz	0.85 T0		1.15 T0	ns
VCO dynamic range	-2V ≤ DFLT - $\overline{DFLT}$ ≤ +2V	±25		±45	%
VCO control gain KVCO	ωi = 2π/TVCO -2V ≤ DFLT- $\overline{DFLT}$ +2V	0.12 ωi		0.24 ωi	rad/(V-S)
Phase detector gain KD	Idle mode = 1 x KD Read mode = 3 x KD Read mode after gain shift = 1 x KD KD = [12.5/(RR + 0.4)] x (0.656 x IDAC + 3.38) x 10^{-6}	0.83 KD		1.17 KD	A/rad
VCO phase restart error	FVCO = 72 MHz	-2		+2	ns
Decode window center accuracy		-0.75		+0.75	ns
Decode window width		TVCO - 0.75			ns

WINDOW SHIFT CONTROL

Window shift magnitude is set by the value in the Window Shift (WS) register. The WS register bits are as follows:

BIT	NAME	FUNCTION
0	$\overline{WS0}$	
1	$\overline{WS1}$	
2	$\overline{WS2}$	
3	$\overline{WS3}$	
4	WSD	Window shift direction. 0=early, 1=late
5	WSE	Window shift enable
6	TDAC0	Used to route signals to DAC test point
7	TDAC1	Used to route signals to DAC test point

The window shift magnitude is set as a percentage of the full decode window, in 2% steps. This results in a window shift capability of ± 30% of the full decode window. The tolerance of the window shift magnitude is ± 30%. Window shift should be set during Idle mode or Write mode.

$\overline{WS3}$	$\overline{WS2}$	$\overline{WS1}$	$\overline{WS0}$	Shift Magnitude
1	1	1	1	No shift
1	1	1	0	2% (minimum shift)
1	1	0	1	4%
1	1	0	0	6%
1	0	1	1	8%
1	0	1	0	10%
1	0	0	1	12%
1	0	0	0	14%
0	1	1	1	16%
0	1	1	0	18%
0	1	0	1	20%
0	1	0	0	22%
0	0	1	1	24%
0	0	1	0	26%
0	0	0	1	28%
0	0	0	0	30% (maximum shift)

DATA SYNCHRONIZER CHARACTERISTICS (continued)

WRITE PRECOMP CONTROL (SSI 33P3734)

Write precomp magnitude is set by the value in the Write Precomp (WP) register. The WP register bits are as follows:

BIT	NAME	FUNCTION
0	$\overline{WE0}$	
1	$\overline{WE1}$	
2	$\overline{WE2}$	
3	WPE	Write precomp enable
4	$\overline{WL0}$	
5	$\overline{WL1}$	
6	$\overline{WL2}$	
7	-	Not used

The write precomp magnitude is calculated as:

$$TPE = n \times 0.04 \times TREF$$

where n = precomp magnitude scaling factor as shown below. The magnitude of early precomp is set by the $\overline{WEx}$ bits. The magnitude of late precomp is set by the $\overline{WLx}$ bits. TREF is the period of the reference frequency provided by the internal time base generator.

$\overline{WE2}$	$\overline{WE1}$	$\overline{WE0}$	Precomp Magnitude Scaling Factor	$\overline{WL2}$	$\overline{WL1}$	$\overline{WL0}$
1	1	1	No precomp	1	1	1
1	1	0	1X	1	1	0
1	0	1	2X	1	0	1
1	0	0	3X	1	0	0
0	1	1	4X	0	1	1
0	1	0	5X	0	1	0
0	0	1	6X	0	0	1
0	0	0	7X (maximum)	0	0	0

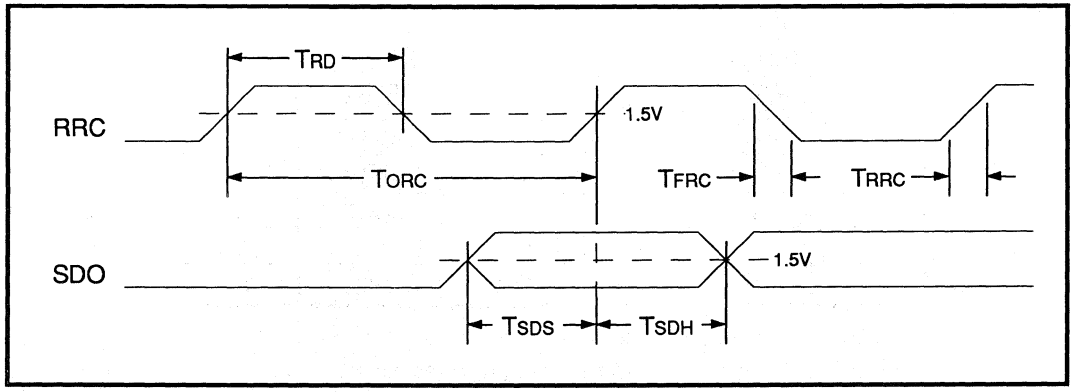

FIGURE 5: SDO Read Timing

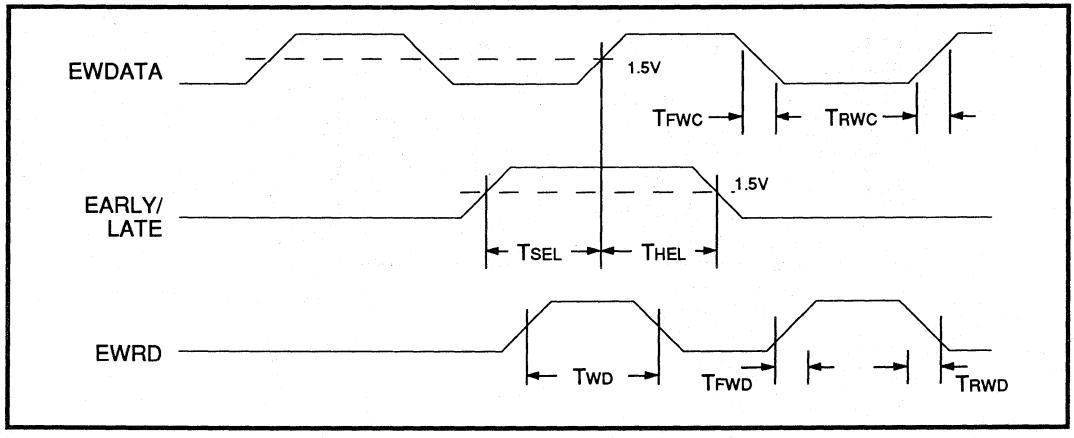

FIGURE 6: EWRD and EWDATA Write Timing

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DATA SYNCHRONIZER CHARACTERISTICS (continued)

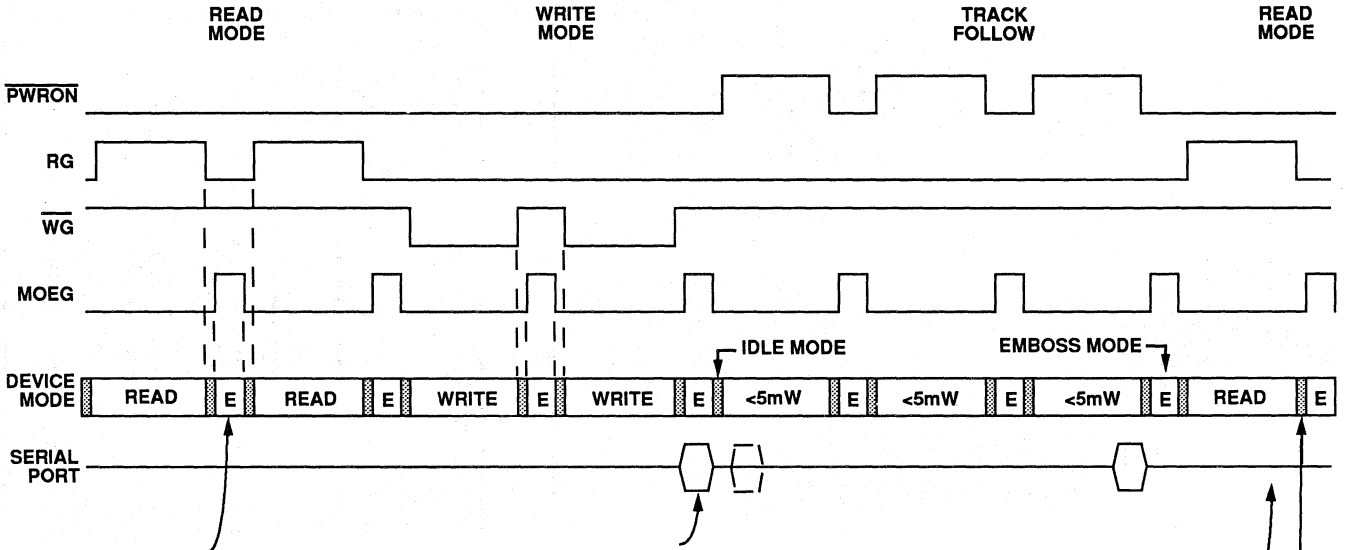
TABLE 4: Multiplexed Test Point Signal Selection

MTPE	TMS1	TMS0	MTP1	MTP2	MTP3
0	X	X	OFF	OFF	OFF
1	0	0	VCOREF	$\overline{DRD}$	DSREF
1	0	1	RD	DOUT	COUT
1	1	0	—	—	NCTR
1	1	1	SET	RESET	COUT

COUT Output of the pulse qualifier clock circuit
DOUT Output of the pulse qualifier data comparators
DSREF Output of the time base generator
NCTR Ncounter output of the time base generator
RD Read MO data output from the pulse qualifier
RESET Output of the negative threshold comparator
SET Output of the positive threshold comparator

TABLE 5: DACOUT Test Point Signal Selection

TDAC1	TDAC0	DAC MONITORED
0	0	Filter fc DAC
0	1	Qualifier threshold DAC (VTH)
1	0	Window shift DAC
1	1	Write precomp DAC



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NOTES:

1) When the PWRON pin is LOW ("0") the Power Down Control Register is active. All blocks that have their control bit set to "1" will be powered down. When the PWRON pin is HIGH ("1") the device goes into a sleep mode with all blocks powered down except the serial port.

2) When the threshold DAC reference is switched, there is a maximum settling time of 1.5µsec for the DAC.

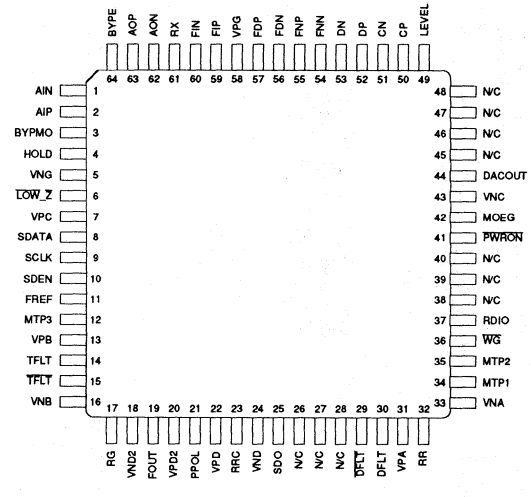
FIGURE 7: Power Control Timing

SSI 33P3733/34
8-26.5 Mbit/s Read Channel

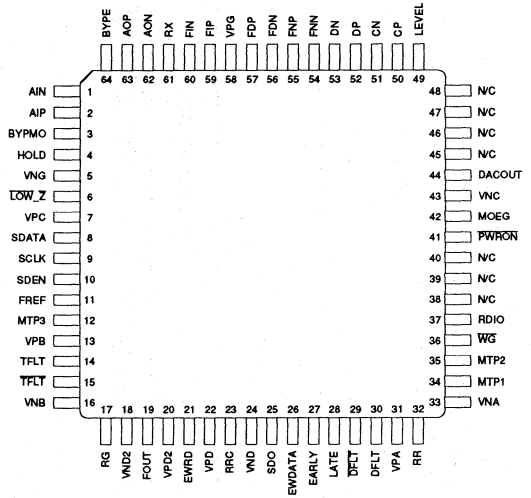
PACKAGE PIN DESIGNATIONS
(Top View)

Thermal Characteristics: θjA

64-lead TQFP	75° C/W



64-Lead TQFP
SSI 33P3733



64-Lead TQFP
SSI 33P3734

CAUTION: Use handling procedures necessary for a static sensitive component.

ORDERING INFORMATION

PART DESCRIPTION		ORDER NUMBER	PACKAGE MARK
SSI 33P3733	64-Lead TQFP	33P3733-CGT	33P3733-CGT
SSI 33P3734	64-Lead TQFP	33P3734-CGT	33P3734-CGT

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914

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SSI 34P553/5531
Pulse Detector & Data Synchronizer

December 1993

DESCRIPTION

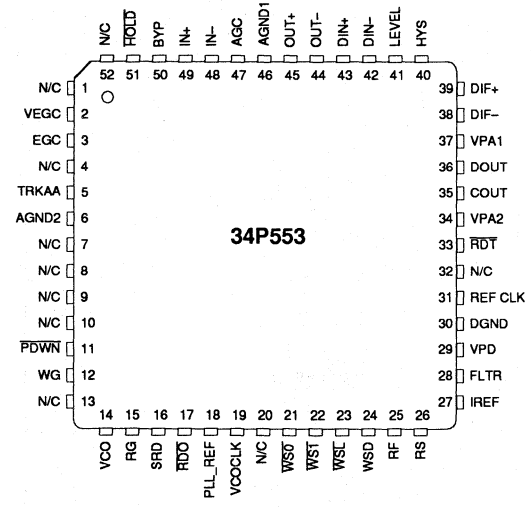
The SSI 34P553/5531 is a low power, high performance Pulse Detection, Data Synchronization combination device. This device is designed for use in low power applications requiring +5V only power supplies. The pulse detection portion of this device detects and validates amplitude peaks in the output from a disk drive read amplifier. The data synchronization portion is an MFM and 1, 7 data synchronizer with window shift capability. The SSI 34P553/5531 achieves low system operating power two ways, with a low operating power (+5V only design) and with a power down mode. The power down mode is a complete shutdown or sleep mode. The SSI 34P553/5531 is available in a 52-lead fine pitch QFP package.

The 34P5531 is the same device, but with separate CIN+, CIN- inputs, for use with active filters such as the SSI 32F8030 (a 2 kΩ resistor would be placed across DIF+/DIF- in this case).

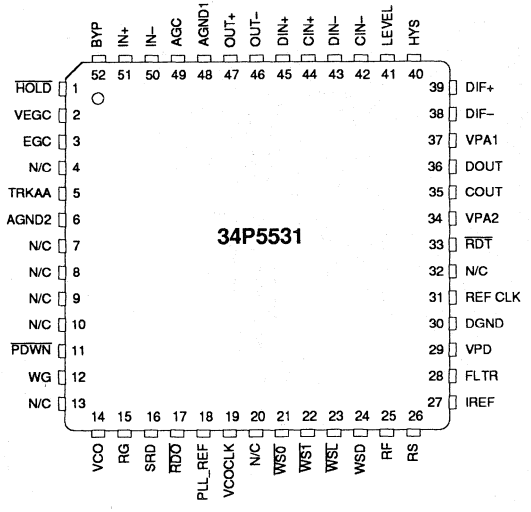
FEATURES

- **Highly Integrated Pulse Detector and Data Synchronizer**
- **+5V only Power Supplies**
- **790 mW max. power**
- **Low Pulse Pairing**
- **0.6-1.6 Mbit/s operation**

PIN DIAGRAMS



52-Lead QFP



52-Lead QFP

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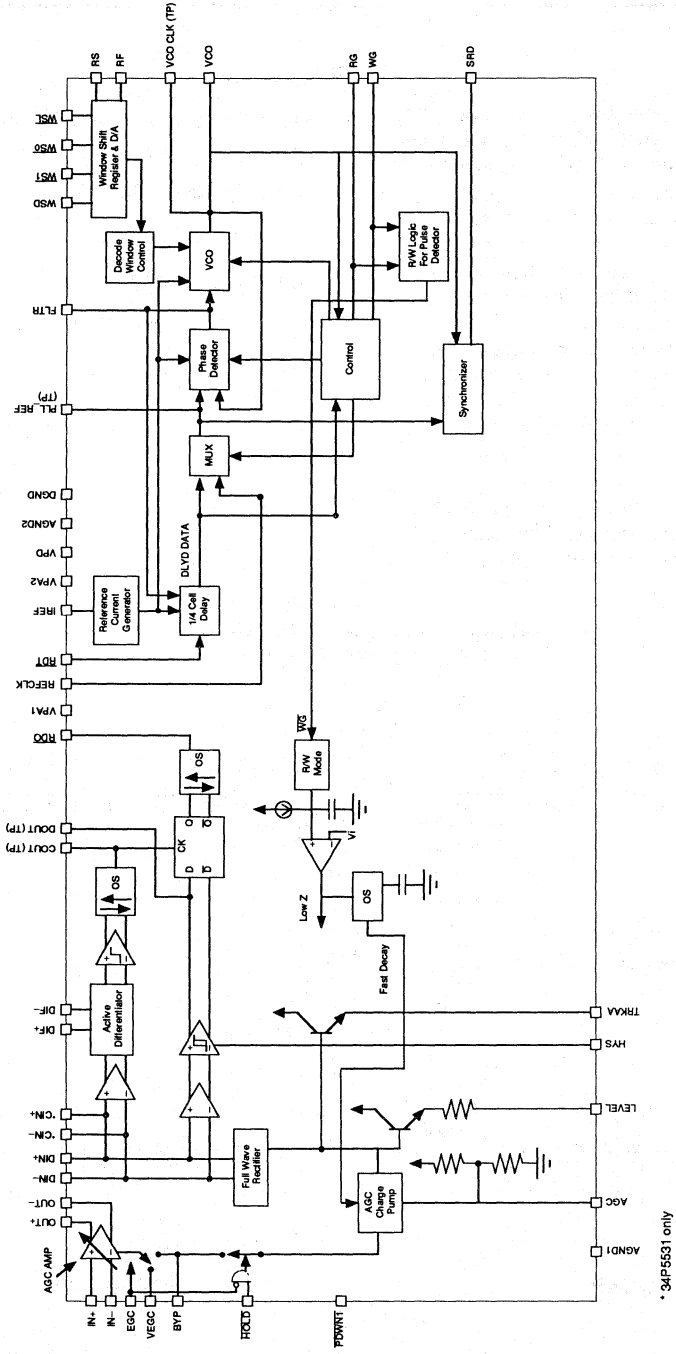
CAUTION: Use handling procedures necessary for a static sensitive component.

BLOCK DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

CIRCUIT OPERATION

PULSE DETECTOR SECTION

READ MODE

The SSI 34P553/5531 enters into the Read mode when the WG pin is pulled low. In the Read mode, the SSI 34P553/5531 provides amplification and pulse level qualification of the signal applied to the input pins of the AGC amplifier.

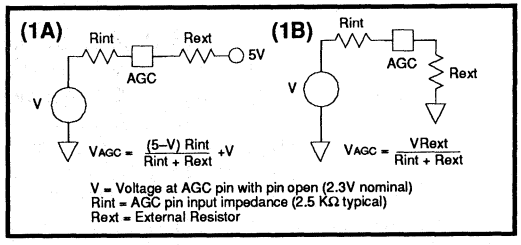
AGC AMPLIFIER

An amplified head output signal is AC coupled to the IN+ and IN- pins of the AGC amplifier. To control the gain of the AGC amplifier, the signal at the DIN± pins is full-wave rectified and amplified. The resulting voltage is compared to the voltage level present at the AGC pin. If the voltage level is higher than the AGC pin reference level, the SSI 34P553/5531 will enter into an Attack mode. If it is lower than the AGC pin voltage the device will enter into a Decay mode.

Attack Mode. The SSI 34P553/5531 contains a dual rate attack charge pump that is controlled by the instantaneous level at DIN±. When the voltage from the full wave rectifier exceeds the AGC pin voltage by greater than 125%, a Fast Attack mode is entered. During fast attack, 1.4 mA of current is supplied to the network on the BYP pin. When the full wave rectifier voltage exceeds the AGC pin voltage by 100 to 125%, the Slow Attack mode is entered. During slow attack the charge current supplied to the BYP pin is 0.18 mA. This dual rate charge pump allows the AGC to recover rapidly during write to read transitions while minimizing distortion once the AGC amplitude is within range.

Decay Mode. Two internally controlled Decay modes are provided by the SSI 34P553/5531. Upon a switch to Write mode, the device holds the gain at its last value and the AGC inputs are switched to low impedance. When the device is switched back from write to read, the gain remains held and the AGC inputs remain in a low impedance state for 0.9 µs. At this time, if the new gain required is more than the held value the device enters into the Decay mode. A fast decay current of 0.12 mA is automatically switched on for a period of 0.9 µs. After 0.9 µs the device will sink a steady state slow decay current of 4.5 µA (reference Figure 7.)

AGC Level Control. The AGC level is controlled by the voltage presented on the AGC pin. The AGC pin is internally biased at approximately 2.3V which sets the signal at the DIN± pins to 1.0 Vpp under nominal conditions. The voltage at the AGC pin can be externally controlled by connecting a resistor between the AGC pin and either VPA1 or AGND1. When a resistor is connected from AGC to VPA1 the voltage on the AGC pin can be increased (Figure 1a). When a resistor is connected from AGC to AGND1 the voltage on the AGC pin can be decreased (Figure 1b). The new DIN± input target level is nominally (VAGC -0.75)•0.64 Vpp. The output of the AGC amplifier has a maximum swing of 3.0 Vpp that can be controlled using the AGC pin. The 3.0 Vpp swing supports the use of external filters that have up to 6 dB of loss. A multi-pole Bessel or an equiripple linear phase filter is typically used for its linear phase or constant group delay characteristics.



FIGURES 1A & 1B: AGC Voltage

The gain of the AGC amplifier is directly controlled by the voltage at the BYP pin (VBYP) or the VEGC pin as shown in Figure 2. The AGC amplifier has open collector outputs that can sink up to 4.0 mA of current. For correct operation over the gain range each output should be pulled up to VPAI through a 340 Ω resistor as shown in Figure 3.

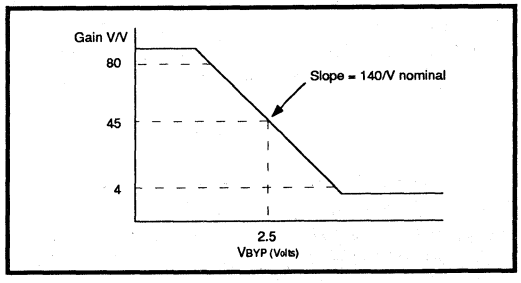


FIGURE 2: AGC Gain

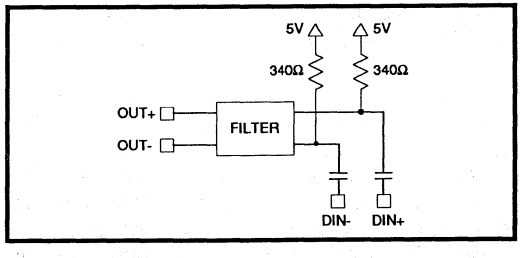


FIGURE 3: AGC Filter

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SSI 34P553/5531
Pulse Detector & Data Synchronizer

PULSE QUALIFICATION

The SSI 34P553/5531 uses both amplitude and time qualification to digitize the incoming data pulses. In the amplitude channel the signal is sent to a hysteresis comparator. A hysteresis trip level is externally set such that only pulses that exceed the required signal level will trip the comparator. This prevents false qualification of baseband noise. The hysteresis trip level can be either a fixed level or a fraction of the DIN± voltage level.

Hysteresis Level. A fixed hysteresis level can be set by applying a DC voltage to the HYS pin. This is a simple method for hysteresis control but it does not compensate well for internal variances from device to device. A more effective approach is to feed forward a percentage of the voltage level at the DIN± pins. This approach is accomplished by using a filter/divider network between the LEVEL and HYS pins. The LEVEL pin output voltage is a rectified and amplified version of the voltage level applied to the DIN± pins. The gain in this circuit is set so that a 1 Vpp signal applied to DIN± will result in a 1 Vpk (typical) output signal at the LEVEL pin. An external capacitor to AGND1 should be used on the LEVEL pin to maintain a DC level. An external voltage divider can be connected between the LEVEL pin and AGND1 to provide the hysteresis programming voltage to the HYS pin. The HYS pin voltage determines the percentage of the DIN± input signal that will trip the hysteresis comparator of the SSI 34P553/5531. The transfer function of the HYS pin for setting the threshold percentage is:

$$\text{Hysteresis Threshold} = 0.41 \times \text{VHYS}$$

where VHYS is the voltage applied to the HYS pin. For example, with a 1.0 Vpp signal at DIN± the LEVEL pin output will be 1.0 Vpk. Using a 50% resistor divider between LEVEL and AGND1 would result in a HYS pin voltage of 0.5V and that would produce a hysteresis threshold of 0.20V in both the positive and negative direction. This translates to a hysteresis threshold percentage of 40% of DIN±.

Because the SSI 34P553/5531 circuits are internally biased to the same levels, the technique of feeding forward the LEVEL pin voltage helps to offset process related internal tolerance variations. In addition, the feed forward technique speeds up transient recovery by allowing qualification of input pulses while the AGC is still settling, such as during write to read recovery or head change recovery. Care should be taken in selecting the hysteresis level time constant so that pattern induced low amplitude signals are not missed. The SSI 34P553/5531 has a built in minimum of ±50 mV threshold for level qualification even when the HYS pin is grounded. This prevents false triggering due to baseband noise during a DC erase gap.

The outputs of the hysteresis comparator are the "D" inputs of the D-type flip-flop. One side of the hysteresis comparator outputs is provided as the DOUT pin test point. The DOUT pin can be monitored by connecting a 3 to 6 kΩ resistor to AGND2. When the DOUT pin is not used, it can be pulled up to VPA1 to save power.

In the time channel the signal is differentiated to transform signal peaks to zero crossings which are detected and used to trigger a bi-directional one-shot. The one-shot output pulses are used as the clock input of the D flip-flop. The COUT pin provides the one-shot output for test purposes. It also requires an external 3 to 6 KΩ pull-down resistor for testing.

The differentiator function is accomplished by an external network between the DIF+ and DIF- pins. The transfer function from DIN± to the comparator input (not DIF±) is:

$$Av = \frac{-2000Cs}{LCs^2 + C(R+92)s + 1}$$

where: C, L, R are external passive components
$20\ pF < C < 500\ pF$
$s = j\omega = j2\pi f$

During normal operation, the time channel clocks the D flip-flop on every positive and negative peak of the DIN± input. The D input to the flip-flop only changes state when the DIN± input exceeds the hysteresis comparator threshold opposite in polarity to the previous threshold exceeding peak.

The time channel, then, determines signal peak timing and the amplitude channel determines validity by blocking signal peaks that do not exceed the hysteresis comparator threshold. The delays in each of these channels to the D flip-flop inputs are well matched. The D flip-flop output triggers a one-shot that sets the $\overline{\text{RDO}}$ output pulse width.

WRITE MODE

In Write Mode the SSI 34P553/5531 Pulse Detector section is disabled and preset for the following Read Mode. The digital circuitry is disabled, ($\overline{RDO}$ pin held high), the input AGC amplifier gain is held at its previous value and the AGC amplifier input impedance is reduced.

Holding the AGC amplifier gain and reducing input impedance shortens system Write to Read recovery times.

The lowered input impedance improves settling time by reducing the time constant of the network between the SSI 34P553/5531 and a head preamplifier such as the SSI 34R1203R. Write to read timing is controlled to maintain the reduced impedance for 0.9 µs before the AGC circuitry is activated. Coupling capacitors should be chosen with as low a value as possible consistent with adequate bandwidth to allow more rapid settling.

DATA SYNCHRONIZER SECTION

The SSI 34P553/5531 is designed to perform data synchronization in rotating memory systems which utilize a 1, 7 RLL and MFM encoding format. In the Read Mode the SSI 34P553/5531 performs Data Synchronization. The interface electronics and architecture of the SSI 34P553/5531 have been optimized for use as a companion device to the WD 42C22 controllers.

The SSI 34P553/5531 can operate with data rates ranging from .6 to 1.6 Mbit/s. This data rate is established by a single 1% external resistor, RR, connected from pin IREF to VPA2. This resistor establishes a reference current which sets the VCO center frequency, the phase detector gain, and the 1/4 cell delay. The value of this resistor is given by:

$$RR = \frac{5.97}{DR} - 1.78\,(k\Omega)\ \text{MFM}$$

$$RR = \frac{7.96}{DR} - 1.78\,(k\Omega)\ 1,7$$

Where: DR = Data Rate in Mbit/s

An external TTL compatible reference may be applied to REFCLK

The SSI 34P553/5531 employs a Dual Mode Phase Detector: Harmonic in the Read Mode and Non-Harmonic in Write and Idle Modes. In the Read Mode the Harmonic Phase Detector updates the PLL with each occurrence of a DLYD DATA pulse. In the Write and Idle Modes the Non-Harmonic Phase Detector is continuously enabled, thus maintaining both phase and frequency lock. By acquiring both phase and frequency lock to the crystal reference oscillator and utilizing a zero phase restart technique, false lock to DLYD DATA is eliminated.

The phase detector incorporates a charge pump in order to drive the loop filter directly. The polarity and width of the output current pulses correspond to the direction and magnitude of the phase error. Figure 4 depicts the average output current as function of the input phase error (relative to the VCO period.)

The READ GATE (RG), and WRITE GATE (WG), inputs control the device mode as described in Table 1. RG is an asynchrouous input and may be initiated or terminated at any position on the disk. WG is also an asynchronous input, but should not be terminated prior to the last output Write Data pulse.

READ OPERATION

The Data Synchronizer utilizes a fully integrated fast acquisition PLL to accurately develp the decode window. Read Gate, RG, initiates the PLL locking sequence and selects the PLL reference input; a high level (Read Mode) selects the Read Data input and low level selects the crystal reference oscillator.

In the Read Mode the rising edge of DLYD DATA enables the Phase Detector while the falling edge is phase compared to the rising edge of the VCO. As depicted in Figure 5, DLYD DATA is a 1/4 cell wide (TVCO/2) pulse whose leading edge is defined by the leading edge of Read Data. VCO is generated from the rising edges of the VCO clock. By utilizing a fully integrated symmetrical VCO running at the code rate, VCO is insured to be accurate and centered symmetrically about the falling edges of DLYD DATA. The accuracy of the 1/4 cell delay only affects the retrace angle of the phase detector and does not influence the accuracy of VCO.

Shifting the symmetry of the VCO clock effectively shifts the relative position of the DLYD DATA pulse within the decode window. This powerful capability easily facilitates defect mappings, automatic calibration, window margin testing, error recovery, and systematic error cancellation. For enhanced disk drive testability and error recovery, decode window control is provided via a µP port ($\overline{WSL}$, WSD, $\overline{WS0}$, $\overline{WS1}$) as described in Table 2. In application not utilizing this feature, $\overline{WSL}$ should be left open or connected to VPA2, while WSD, $\overline{WS0}$, and $\overline{WS1}$ can be left open.

Window shifts in the range of ±5% to ±20% of TVCO are easily programmed by latching the appropriate control word into the Window Shift Register with the WSL pin. Shifts in the positive or negative directions result in early or late decode windows respectively, as depicted in Figure 6. Additionally, for small systematic error cancellation, a resistor, R, connected from either RS (Early) or RF (Late) to ground will provide analog control over the decode window. The magnitude of this shift, TSA is determined by:

$$TSA = 0.25\,TVCO\left(1 - \frac{3260+R}{5950+R}\right)$$

Where: R is in Ω

Pins RF and RS are intended to be used as a trim and should be restricted to ±3% window shifts. They can be used in conjunction with the digital control port.

In Non-Read Modes, the PLL is locked to REFCLK. This forces the VCO to run at a frequency which is very close to that required for tracking actual data and thus minimizes the associated frequency step during acquisition. When RG transitions, the VCO is stopped momentarily, then restarted in an accurate phase alignment with the next PLL reference input pulse. By minimizing the phase alignment in this manner, the acquisition time is substantially reduced.

POWER DOWN MODE

A Power Down mode is provided to reduce power usage during the idle periods. Taking $\overline{PDWN}$ low causes the device to go into complete shutdown.

MODE CONTROL

The SSI 34P553/5531 Circuit mode is controlled by the $\overline{PDWN}$, $\overline{HOLD}$, RG, and WG pins as shown in Table 1.

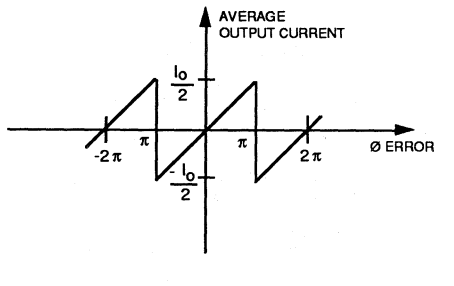
TABLE 1: Mode Control

WG	RG	$\overline{HOLD}$	$\overline{PDWN1}$	
0	0	1	1	Read Mode VCO Locked to XTAL
0	1	1	1	Read Mode VCO Locked to Read Data
0	X	0	1	Read Mode AGC gain held constant*
1	0	X	1	Write Mode AGC gain held constant* Input impedance reduced
X	X	X	0	Power shutdown mode

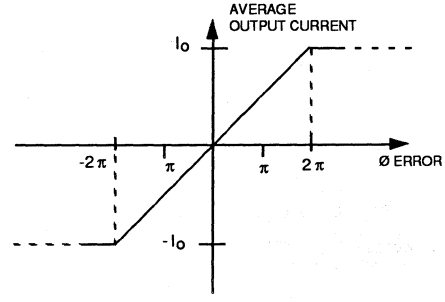
* AGC gain will drift at a rate determined by BYP capacitor and Hold mode leakage current.

TABLE 2: Decode Window Symmetry Control

Ts, NOMINAL WINDOW SHIFT	WSD	$\overline{WS1}$	$\overline{WS0}$
+TS3	0	0	0
+TS2	0	0	1
+TS1	0	1	0
0	0	1	1
-TS3	1	0	0
-TS2	1	0	1
-TS1	1	1	0
0	1	1	1



a) HARMONIC MODE



b) NON-HARMONIC MODE

Note 1) Io is the magnitude of the charge pump current.
2) Phase error is relative to the VCO period

FIGURE 4: Phase Detector Transfer Function

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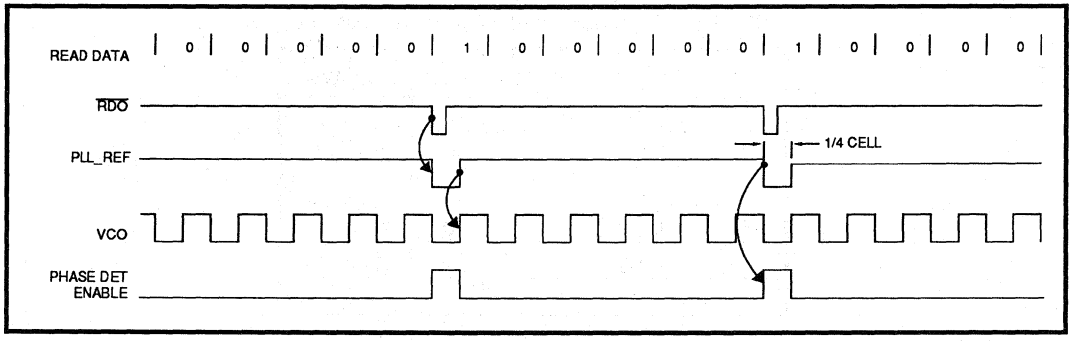

FIGURE 5: Data Synchronization Waveform Diagram

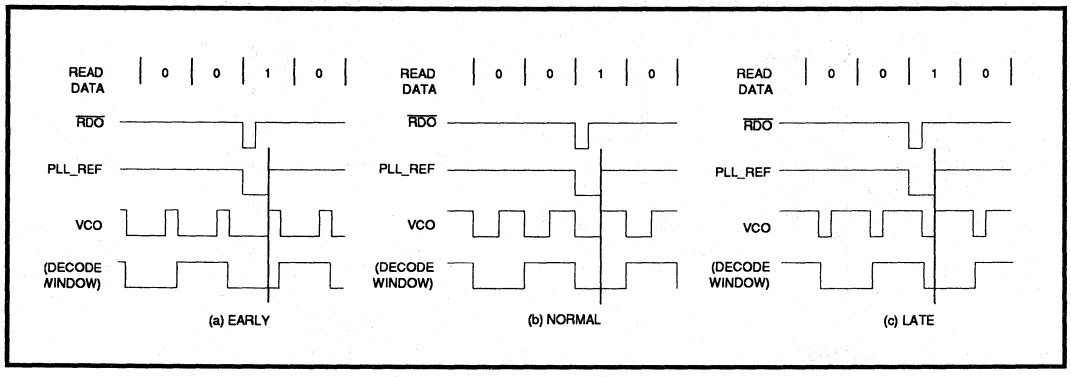

FIGURE 6: Decode Window

PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
VPA1	I	Analog (+5V) power supply for pulse detector.
AGND1	I	Analog ground pin for pulse detector block.
VPA2	I	Analog (+5V) supply pin for data synchronizer block.
AGND2	I	Analog ground pin for data synchronizer block.
VPD	I	Digital (+5V) power supply pin.
DGND	I	Digital ground pin.
IN+, IN–	I	Analog signal input pins.
OUT+, OUT–	O	Read path AGC Amplifier output pins.
DIN+, DIN–	I	Analog input to the hysteresis comparator, and differentiator.
CIN+, CIN–	I	Analog input to the clock comparator, differentiator. (34P5531 only)
DIF+, DIF–	I/O	Pins for external differentiating network.
COUT	O	Test point for monitoring the flip-flop clock input. A 5 kΩ pull down resistor is required. When not in use, leave open or pull up to VPA1 to save power.
DOUT	O	Test point for monitoring the flip-flop D-input. A 5 kΩ pull down resistor is required. When not in use, leave open or pull up to VPA1 to save power.
BYP	I/O	An AGC timing capacitor or network is tied between this pin and AGND1.
AGC	I	Reference input voltage for the read data AGC loop.
LEVEL	O	Output from fullwave rectifier that may be used for input to the hysteresis comparator.
HYS	I	Hysteresis level setting input to the hysteresis comparator.
TRKAA	O	Full wave rectifier output. This output has the same DC level as the LEVEL pin, i.e., ≤ 0.3V with no AC signal and ≈ $1V_{OP}$ with a $1V_{PP}$ AC signal at DIN+/ DIN-.
$\overline{\text{HOLD}}$	I	TTL compatible pin that holds the AGC gain when pulled low.
EGC	I	External Gain Control. This is a TTL input pin that allows the AGC gain to be controlled by either BYP or the VEGC pin voltage. When EGC is high, the AGC gain is controlled by VEGC and the internal charge pump to BYP is disabled.
VEGC	I	The voltage at this pin is used to control the AGC gain when the EGC pin is held high.
$\overline{\text{RDO}}$	O	Read Data Output. This is the TTL output from the pulse detector. This signal may be fed directly into the $\overline{\text{RDT}}$ input.
IREF	I	Timing program pin: the VCO center frequency, Phase Detector Gain and the 1/4 cell delay are a function of the current source into pin IREF. The current is set by an external resistor, RR connected from IREF to VPA2.
FLTR	I/O	Filter pin: the phase detector output and VCO input node. The loop filter is connected to this pin.

PIN DESCRIPTION (continued)

NAME	TYPE	DESCRIPTION
SRD	O	Synchronized Read Data: read data that has been re-synchronized to VCO clock.
WSD	I	Window Symmetry Direction: controls the directions of the optional window symmetry shift. Pin WSD has an internal resistor pull-up.
$\overline{WS0}$	I	Window symmetry control bit: a low level introduces a window shift of 5% TORC (read reference clock period) in the direction established by WSD pin. $\overline{WS0}$ has an internal resistor pull-up.
$\overline{WS1}$	I	Window Symmetry Control bit: a low level introduces a window shift of 15% TORC (read reference clock period) in the direction established by WSD. A low level at both $\overline{WS0}$ and $\overline{WS1}$ will produce the sum of the two window shifts. Pin $\overline{WS1}$ has an internal resistor pull-up.
$\overline{WSL}$	I	Window Symmetry Latch: used to latch the input window symmetry control bits WSD, $\overline{WS0}$, $\overline{WS1}$ into the internal DAC. An active low level latches the input bits.
RF, RS	I	WINDOW SYMMETRY ADJUST PINS: Provides analog control over the decode window symmetry; typically used to null out any window symmetry offset. A resistor connected from either RF or RS to AGND will provide magnitude and direction control. They can be used in conjunction with the digital control port WSD, $\overline{WS0}$, $\overline{WS1}$.
RG	I	Read gate: selects the PLL reference input and initiates the PLL synchronization sequence. A high level selects the internal RD± inputs. A low level selects the crystal reference oscillator, Pin RG has an internal resistor pullup.
WG	I	Write Gate: enables the Write mode. Pin WG has an internal resistor pullup.
VCO CLK	O	VCO CLK: An open emitter ECL output test point. Two external resistors are required to perform this test. They should be removed during normal operation for reduced power dissipation.
$\overline{RDT}$	I	Read Data input. This TTL input comes from the $\overline{RDO}$ output of the pulse detector. This signal is active low.
$\overline{PDWN}$	I	Power Down input. When this input is low, the chip enters Low Power mode. This pin has an internal pullup resistor, and may be left open or tied high if not used.
REF CLK	I	Reference Clock. This is a TTL input at the code rate that is used as the reference for the VCO in Idle mode.
VCO	O	VCO output. This is the VCO signal converted to a TTL level.
PLL_REF	O	PLL Reference Test Point. In Write and Idle modes, this is the reference oscillator signal. In Read mode, it is the delayed read data (DRD) signal. This is an ECL level output. PLL_REF can be compared to VCOCLK to see the window centering accuracy.

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, 4.5V ≤ VPA 2 ≤ 5.5V, 25°C ≤ Tj ≤ 135°C, 1.2 MHz ≤ 1/TVCO ≤ 2.4 MHz.

ABSOLUTE MAXIMUM RATINGS

Operation outside these rating limits may cause permanent damage to this device.

PARAMETER	RATING
5V Supply Voltage, VPA1, VPA2, VPD	6.0 V
Pin Voltage (Analog pins)	-0.3 to VPA1, 2 + 0.3 V
Pin Voltage (All others)	-0.3 to VPD + 0.3 V or +12 mA
Storage Temperature	-65 to 150 °C
Lead Temperature (Soldering 10 sec.)	260 °C

RECOMMENDED OPERATING CONDITIONS

Currents flowing into the chip are positive.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Supply Voltage (VPA1, 2 & VPD)		4.5	5.0	5.5	V
Tj Junction Temperature		25		135	°C

POWER SUPPLY

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
IVPA1, 2 Supply Current IVPD	Outputs unloaded $\overline{PDWN}$= high or open		110	143	mA
	$\overline{PDWN}$ = low Outputs unloaded		44	57	mA
Pd Power dissipation	Ta = 25°C, outputs unloaded $\overline{PDWN}$= high or open		550	790	mW
	$\overline{PDWN}$ = low Outputs unloaded		220	315	mW

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ELECTRICAL SPECIFICATIONS (continued)

LOGIC SIGNALS

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
VIL Input Low Voltage		-0.3		0.8	V
VIH Input High Voltage		2.0		VCC+0.3	V
IIL Input Low Current	VIL = 0.4V	-0.4			mA
IIL WG Input Low Current	VIL = 0.4V	-0.8			mA
IIH Input High Current	VIH = 2.4V			100	µA
VOL Output Low Voltage	IOL = 4.0 mA			0.5	V
VOH Output High Voltage	IOH = -400 µA	2.4			V
VOHT Test Point Output High Level PLL_ REF, VCOCLK	262Ω to VPD 402Ω to GND VPD = 5.0V VOHT - VPD		-0.85		V
VOLT Test Point Output Low Level PLL_REF, VCOCLK	262Ω to VPD 402Ω to GND VPD = 5.0V, VOHT - VPD		-1.75		V

* Output load is a 4K resistor to 5V and a 10 pF capacitor to DGND.

MODE CONTROL

Enable to/from $\overline{\text{PDWN}}$ Transition Time	Settling time of external capacitors not included, $\overline{\text{PDWN}}$ pin high to/from low			20	µs
Read to Write Transition Time	WG pin low to high			1.0	µs
Write to Read Transition Time	WG pin high to low AGC setting not included	0.4	0.9	1.6	µs
$\overline{\text{HOLD}}$ On to/from $\overline{\text{HOLD}}$ Off Transition Time	$\overline{\text{HOLD}}$ pin high to/from low			1.0	µs
RG Time Delay				100	ns

READ MODE (WG is low)

AGC AMPLIFIER

Unless otherwise specified, recommended operating conditions apply. Input signals are AC coupled to IN±. OUT± are loaded differentially with 340Ω x 2 to VPA1, and each side is loaded with < 10 pF to AGND1, and AC coupled to DIN±. A 0.1 µF capacitor is connected between BYP and AGND1. AGC pin is open.

Gain Range	1.0 Vpp ≤ (OUT+) - (OUT-) ≤ 3.0 Vpp	4		80	V/V
AGC Input Range	AGC output = 1Vpp differential	25		250	mVpp
Output Offset Voltage Variation	Over entire gain range	-500		+500	mV
Maximum Output Voltage Swing	Set by BYP or VEGC pin	3.0			Vpp

AGC AMPLIFIER (continued)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Differential Input Resistance	(IN+) - (IN-) = 100 mVpp @ 2.5 MHz	4	5.4	7.5	kΩ
Differential Input Capacitance	(IN+) - (IN-) = 100 mVpp @ 2.5 MHz		5	10	pF
Single Ended Input	WG = low, IN+ or IN-	2	2.7	4	kΩ
Impedance	WG = high, IN+ or IN-		160	250	Ω
Input Noise Voltage	Gain set to maximum, Rs = 0 BW = 15 MHz		5	15	nV/√Hz
Bandwidth	-3 dB bandwidth at maximum gain	12			MHz
OUT+ & OUT- Pin Current	No DC path to AGND1	2.5	4.0		mA
CMRR (Input Referred)	(IN+) = (IN-) = 100 mVpp @ 5 MHz, gain set to max	40			dB
PSRR (Input Referred)	VPA1, 2 = 100 mVpp @ 5 MHz, gain set to max	30			dB
(DIN+) - (DIN-) Input Swing vs. AGC Input (DIN+) - (DIN-) = (V_{AGC} - K1) • K2	25 mVpp ≤ (IN+) - (IN-) ≤ 250 mVpp, $\overline{HOLD}$ = high, 0.5 Vpp ≤ (DIN+) - (DIN-) ≤ 1.5 Vpp				
	K1	0.5	0.8	0.95	V
	K2	0.54	0.64	0.74	Vpp/V
(DIN+) - (DIN-) Input Voltage Swing Variation	25 mVpp ≤ (IN+) - (IN-) ≤ 250 mVpp			5.0	%
AGC Voltage	AGC open	2.0	2.3	2.6	V
AGC Pin Input Impedance		1.8	2.5	3.8	kΩ
Slow AGC Discharge Current	(DIN+) - (DIN-) = 0V, AGC pin open	2.8	4.5	6	µA
Fast AGC Discharge Current	Starts at 0.9 µs after WG goes low, stops at 1.8 µs after WG goes low		0.12		mA
BYP Leakage Current	$\overline{HOLD}$ = low	-0.2		+0.2	µA
Slow AGC Charge Current	(DIN+) - (DIN-) = 0.563 VDC, AGC pin open	-0.11	-0.18	-0.25	mA
Fast AGC Charge Current	(DIN+) - (DIN-) = 0.8 VDC, AGC pin open	-0.9	-1.4	-1.9	mA
Fast to Slow Attack Switchover Point	$\frac{[(DIN+)-(DIN-)]}{[(DIN+)-(DIN-)]FINAL}$		125		%

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ELECTRICAL SPECIFICATIONS (continued)

AGC AMPLIFIER (continued)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Gain Decay Time (Td)	(IN+) - (IN-) = 250 mVpp to 125 mVpp @ 0.6 MHz, (OUT+) - (OUT-) to 90% final value		100	180	µs
	(IN+) - (IN-) = 50 mVpp to 25 mVpp at 0.6 MHz (OUT+) - (OUT-) to 90% final value	190	300	550	µs
Gain Attack Time	WG = high to low (IN+) - (IN-) = 250 mVpp @ 0.6 MHz, (OUT+) - (OUT-) to 110% final value		8	15	µs

WRITE MODE (WG is high)

Single Ended Input Impedance (Each Side)	IN+ or IN-		160	250	Ω

HYSTERESIS COMPARATOR

Unless otherwise specified, recommended operating conditions apply. Input (DIN+) - (DIN-) is an AC coupled, 1.0 Vpp, 0.6 MHz sine wave. 0.5 VDC is applied to the HYS pin. WG pin is low.

Input Signal Range				1.5	Vpp
Differential Input Resistance	(DIN+) - (DIN-) = 100 mVpp @ 0.6 MHz	3	5.5	8	kΩ
Differential Input Capacitance	(DIN+) - (DIN-) = 100 mVpp @ 0.6 MHz		4	8	pF
Single Ended Input Impedance (Each Side)	DIN+ or DIN-	1.5	2.75	4	kΩ
Level Gain	0.6 Vpp < (DIN+) - (DIN-) < 1.5 Vpp, 10K between LEVEL and AGND	0.80	1.00	1.25	V/Vpp
Slope of Level Gain	Calculated from 0.6 Vpp < (DIN+) - (DIN-) < 1.5 Vpp	0.75	0.87	1.00	V/Vpp
Intercept of Level Gain	DIN± = 0 Vpp	-0.6	-0.4	-0.2	V
Level Gain		Slope + (Intercept/DIN)			
Level Pin Output Impedance	I_{LEVEL} = 0.2 mA	100	200	300	Ω
Level pin Maximum Output Current		1.5			mA

HYSTERESIS COMPARATOR (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Hysteresis Gain	0.3V < HYS < 1.0V	0.30	0.41	0.50	V/V
Slope of Hysteresis Gain	Calculated from 0.3V < HYS < 1.0V	0.34	0.42	0.46	V/Vpp
Intercept of Hysteresis Gain	HYS = 0V	-0.05	0.00	0.05	V
Hysteresis Gain		Slope + (Intercept/HYS V)			
HYS Pin Current	0.3 V < HYS < 1.0V	0.0		-5	µA
DOUT Pin Output Low Voltage	5 kΩ from DOUT to AGND2	VPA2 -2.5	VPA2 -2	VPA2 -1.35	V
DOUT Pin Output High Voltage	5 kΩ from DOUT to AGND2	VPA2 -2.0	VPA2 -1.6	VPA2 -1.1	V

ACTIVE DIFFERENTIATOR

Unless otherwise specified, recommended operating conditions apply. Input (DIN+) - (DIN-) is an AC-coupled, 1.0 Vpp, 0.6 MHz sine wave. 100 Ω in series with 265 pF are tied from DIF+ to DIF-.

Input Signal Range				1.5	Vp-p
Differential Input Resistance	(CIN+) - (CIN-) = 100 mVp-p @ 2.5 MHz	8	10	14	kΩ
Differential Input Capacitance	(CIN+) - (CIN-) = 100 mVp-p @ 2.5 MHz			5.0	pF
Common Mode Input Impedance	Both sides	2.0	2.5	3.5	kΩ
Voltage Gain From CIN± to DIF±	(DIF+ to DIF-) = 2 kΩ		1		V/V
DIF+ to DIF- Pin Current	Differentiator impedance must be set so as to not clip the signal for this current level	-0.7		+0.7	mA
COUT Pin Output Low Voltage	5 kΩ from COUT to GND	VPA2 -2.5	VPA2 -2	VPA2 -1.35	V
COUT Pin Output High Voltage	5 kΩ from COUT to GND	VPA2 -2	VPA2 -1.6	VPA2 -1.1	V
COUT Pin Output Pulse Width			36		ns

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ELECTRICAL SPECIFICATIONS (continued)

QUALIFIER TIMING (See Figure 8)

Unless otherwise specified, recommended operating conditions apply. Inputs (DIN+) - (DIN-) are an AC coupled, 1.0 Vpp, 0.6 MHz sine wave. 100Ω in series with 265 pF are tied from DIF+ to DIF-. 0.5V is applied to the HYS pin. COUT and DOUT have a 5 kΩ pull-down resistor (for test purposes only.) WG pin is low. $\overline{RDO}$ is loaded with a 4 kΩ resistor to VPD and a 10 pF capacitor to DGND.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Td1	D Flip-Flop Set Up Time	Minimum allowable time delay from (DIN+) - (DIN-) exceeding hysteresis point to (DIF+) - (DIF-) hitting a peak value.	0			ns
Td3	Propagation Delay	From positive peak of DP/DN to $\overline{RDO}$ output pulse		60	110	ns
Td4	Propagation Delay	From negative peak of DP/DN to $\overline{RDO}$ output pulse		60	110	ns
|Td3-Td4|	Pulse Pairing				6	ns
Td5	Output Pulse Width		25	36	55	ns

SYNCHRONIZER SECTION

READ MODE

TRVCO, VCO Output Rise Time	0.8V to 2.0V, CL ≤ 15 pF			8	ns
TFVCO, VCO Output Fall Time	2.0V to 0.8V, CL ≤ 15 pF			5	ns
TSRD, SRD Output Pulse Width		(TVCO) -12		(TVCO) +12	ns
TRSRD, Read Data Rise Time	0.8V to 2.0V, CL ≤ 15 pF			10	ns
TFSRD, Read Data Fall Time	2.0V to 0.8V, CL ≤ 15 pF			8	ns
TPSRD, SRD Output Setup/HoldTime	Falling edge of VCO to either edge of SRD	-15		15	ns
TRD, $\overline{RDT}$ Input Pulse Width		20		(TVCO) -20	ns
TFRD, $\overline{RDT}$ Input Fall Time				15	ns
TWVCO, VCO Output		0.26TVCO		0.74TVCO	ns
Pulse Width (Includes Effects of Window Shift)		-10		+10	

WINDOW SYMMETRY CONTROL CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
TWSS $\overline{WS0}$, $\overline{WS1}$, WSD Set Up Time		50			ns
TWSH $\overline{WS0}$, $\overline{WS1}$, WSD Hold Time		0			ns

DATA SYNCHRONIZATION

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TVCO	VCO Center Frequency Period	VCO IN = 2.7V TO = 83.8 (RR + 1.78), RR = 3k to 9k VPA2 = 5.0V	0.8TO		1.2TO	ns
	VCO Frequency Dynamic Range	1.0V ≤ VCO IN ≤ VPA2-0.6V VPA2 = 5.0V	±22		±45	%
KVCO	VCO Control Gain	$\omega o = 2\pi / TO$ 1.0V ≤ VCO IN ≤ VPA2-0.6V	0.16 ωo		0.25 ωo	rad/s V
KD	Phase Detector Gain	KD = 0.538 / (RR+500) VPA2 = 5.0V	0.83 KD		1.17 KD	A/rad
*	KVCO x KD Product Accuracy		-28		+28	%
*	VCO Phase Restart Error			12		ns
	Decode Window Centering Accuracy		-.02 TVCO		.02 TVCO	ns
	Decode Window		0.9 TVCO			ns
TS1	Decode Window Time Shift	TWS1 = .05 TVCO $\overline{WSO}$ = 0; $\overline{WSI}$ = 1		TWS1		ns
TS2	Decode Window Time Shift	TWS2 = .15 TVCO $\overline{WSO}$ = 1; $\overline{WSI}$ = 0		TWS2		ns
TS3	Decode Window Time Shift	TWS3 = .2 TVCO $\overline{WSO}$ = 0; $\overline{WSI}$ = 0		TWS3		ns
TSA	Decode Window Time Shift	$TWSA = 0.29\,TVCO\left(1-\frac{3260+R}{5950+R}\right)$ $\overline{WSO}$ = 1; $\overline{WSI}$ = 1		TWSA		ns
*	Not directly testable; design characteristics					

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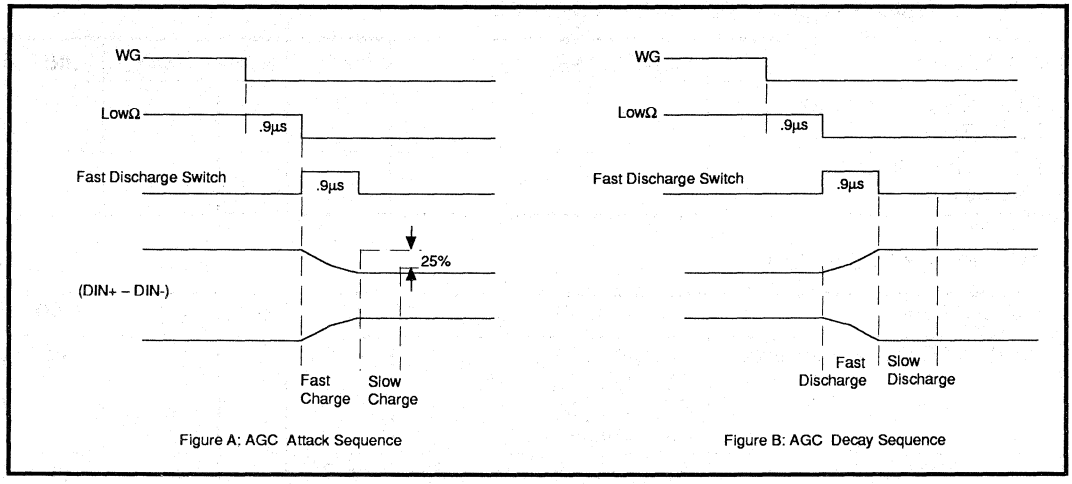

FIGURE 7: AGC Timing Diagram

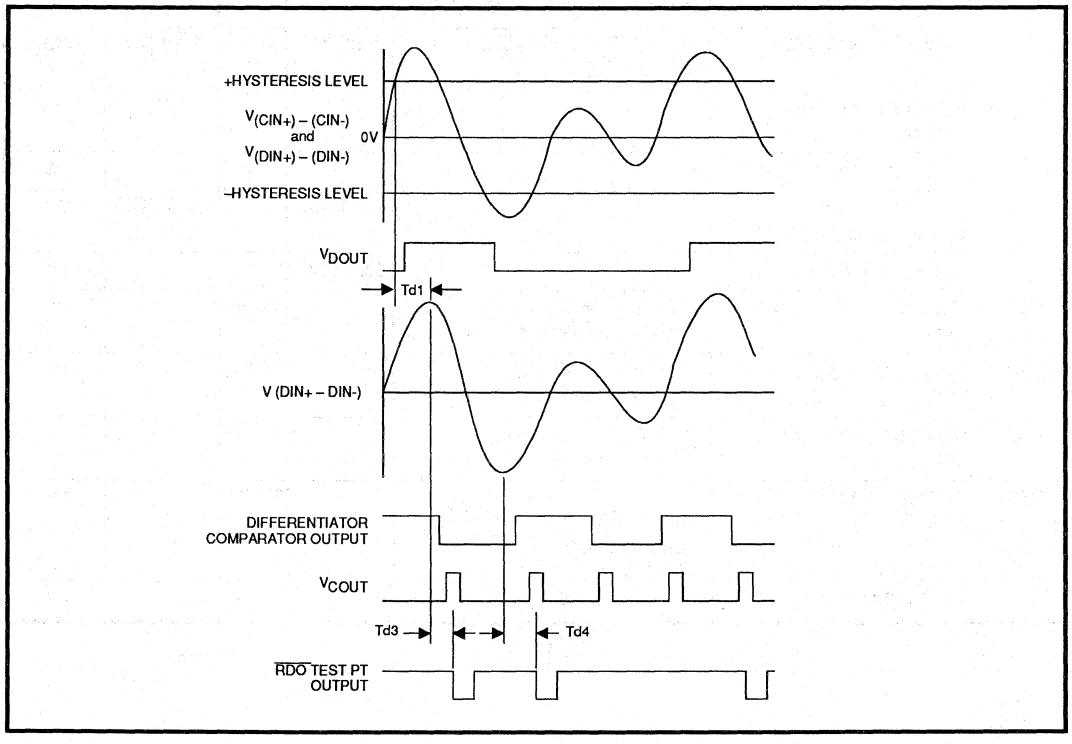

FIGURE 8: Read Mode Digital Section Timing Diagram

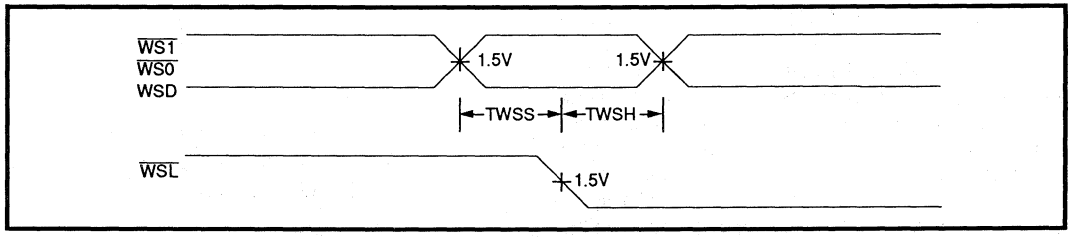

FIGURE 9: Window Symmetry Control Timing

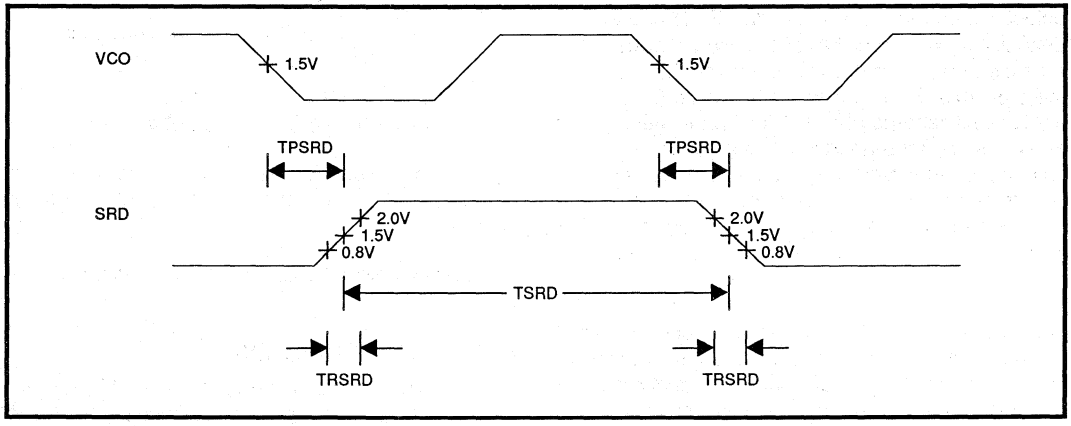

FIGURE 10: Read Mode Timing

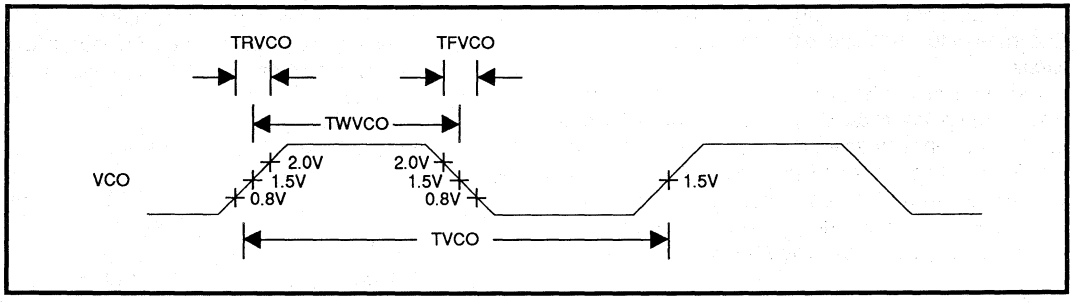

FIGURE 11: VCO Timing

SSI 34P553/5531
Pulse Detector & Data Synchronizer

APPLICATIONS INFORMATION

The SSI 34P553/5531 PLL uses a new architecture which incorporates an accurate quarter cell delay circuit. The standard architecture of a data synchronizer PLL is shown in Figure14A. In read mode, the rising edge of the quarter cell delay enables the phase detector, and the falling edge is locked to the VCO. Ideally, the quarter cell delay enables the phase detector one half of an encoded bit cell time before the phase comparison takes place. A data bit could then shift early or late by one half of an encoded bit cell time before a phase detector output error would occur. If the quarter cell delay is not exactly one half of an encoded bit cell time, a phase detector error will occur when the read data shifts by an amount that is smaller than one half of an encoded bit cell time when shifting in one direction and an amount larger than one half of an encoded bit cell time in the other direction. In addition, when an error occurs, the resulting charge pump output goes from maximum output one way to maximum output the other way. This can cause loss of lock to occur. The timing is shown in Figure 15.

The SSI 34P553/5531 achieves an accurate quarter cell delay time by using the VCO control voltage to compensate the quarter cell delay one-shot circuit for process, temperature and power supply induced timing variations. The modified architecture of the SSI 34P553/5531 data synchronizer is shown in Figure 16B. Because the quarter cell delay timing is adjusted by the VCO control voltage, there is an effect on the PLL transfer function due to the new quarter cell delay circuit.

The quarter cell delay circuit produces a time delay output in response to a voltage input. In order to include this function in a phase-locked loop, the time delay function must be converted into a phase function. This is straightforward, since a time delay is equivalent to a phase angle. The equivalent phase representation of the quarter cell delay is derived below.

For the VCO: $K_o = \frac{d\omega_o}{dV}$ (1a)

$$\frac{dT_O}{dV} \quad \frac{d}{dV}\left(\frac{1}{f_O}\right) = -\frac{1}{f_O{}^2}\frac{df_O}{dV} = -T_O{}^2\frac{df_O}{dV} = -\frac{T_O{}^2}{2\pi}\frac{dw_O}{dV} \quad (1b)$$

where:

K_0 = VCO gain
ω_0 = VCO center frequency (rad/s)
f_0 = VCO center frequency (Hz)
T_0 = VCO center frequency (sec)

For the quarter cell delay,

$$K_T = \frac{dq_o}{dV} = \frac{2\pi}{T_o}a\frac{dT_0}{dV} = -\alpha T_o\frac{dw_o}{dV} = -\alpha T_oK_o$$

where:

θ_0 = Phase due to quarter cell delay circuit
T_0 = VCO center frequency period
T_Q = Quarter cell delay time
$\alpha = T_Q/T_0 = 0.5$ for the 32P548

The gain of the quarter cell delay block is constant in the SSI 34P553/5531, regardless of the values of other components.

For the SSI 34P553/5531, the nominal value of K_T is 0.17π.

PLL TRANSFER FUNCTION

There are two modes of operation of the PLL, and two transfer functions. In Write and Idle modes, the PLL is locked to the reference oscillator, and the quarter cell delay does not enter into the transfer function. In Read, mode, the PLL is locked to read data, and the quarter cell delay is included in the transfer function. In addition, the effective loop gain of the PLL increases in Idle mode due to the phase detector. This will be explained later in more detail.

The transfer functions for Read and Idle modes are given in (3) and (4), respectively.

$$\frac{\theta_O(s)}{\theta_r(s)} = \frac{\frac{nK_OK_dF(s)}{S}}{1+nK_TK_dF(s)+\frac{nK_OK_dF(s)}{S}} \quad (3)$$

$$\frac{\theta_O(s)}{\theta_r(s)} = \frac{\frac{nK_OK_dF(s)}{S}}{1+\frac{nK_OK_dF(s)}{S}} \quad (4)$$

where:

K_T = Quarter cell delay one-shot gain
K_O = VCO gain
K_d = Phase detector gain
F(s) = Loop filter transfer function
n = Ratio of input freq. to reference freq.

In (3) the K term in the denominator is a result of the quarter cell delay. Substituting $K_T = \alpha K_O T_O$ into (3),

$$\frac{\theta_o(s)}{\theta_r(s)} = \frac{\frac{nK_OK_dF(s)}{S}}{1+(1-s\alpha T_O)\frac{nK_OK_dF(s)}{S}}$$

The additional $-s\alpha T_O$ term in the denominator due to the quarter cell delay introduces positive feedback. However, the gain of the positive feedback is always less than one, so there is no instability. The additional term is not always negligible, and must be taken into account in the loop analysis and design.

Two loop filter configurations, shown in Figure 12, will be considered. Both filters result in a second order type 2 loop transfer function, with only minor differences in the loop equation.

The transfer function of the loop filter for a charge-pump PLL is the transimpedance, V_o/I_i (s), where V_o (s) is the output voltage, and I_i (s) is the input current. The transfer functions of (a) and (b) are given by:

$$F_a(s) = \frac{sR_1C_1+1}{s(C_1+C_2)\left(sR_1\frac{C_1C_2}{C_1+C_2}+1\right)} \quad (6)$$

$$F_b(s) = \frac{sR_1(C_1+C_2)+1}{sC(sR_1C_2+1)} \quad (7)$$

For loop filter (a), C_2 is normally chosen to be much smaller than C_1 so that it does not affect the loop transfer function significantly. Assuming that $C_1 \gg C_2$ and $sR_1C_1 \ll 1$ at the frequencies of interest, (6) reduces to:

$$F_a(s) = \frac{sR_1C_1+1}{sC_1} \quad (8)$$

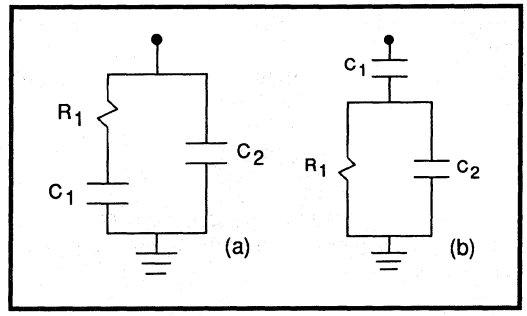

FIGURE 12: Loop Filter

For loop filter (b), C_2 is normallly chosen to be much smaller than C_1 so that it does not affect the loop transfer function significantly. Assuming that $C_1 \gg C_2$ and that $sR_1C_2 \ll 1$ at the frequencies of interest, (7) reduces to:

$$F_b(s) = \frac{sR_1C_1+1}{sC_1} \quad (9)$$

Equations (8) and (9) are the same, and either loop filter may be used. Substituting (8) into (3) gives:

(10)

$$\frac{\theta_o(s)}{\theta_r(s)} = \frac{\frac{nK_OK_d}{C_1(1-\alpha T_OnK_OK_dR_1)}(sR_1C_1+1)}{s^2+s\frac{nK_OK_d}{1-\alpha T_OnK_OK_dR_1}\left(R_1-\frac{\alpha T_O}{C_1}\right)+\frac{nK_OK_d}{C_1(1-\alpha T_OnK_OK_dR_1)}}$$

This is in the form of a standard second order transfer fucntion. The denominator has the form:

$$D(s) = s^2 + 2\zeta\omega_n s + \omega_n^2 \quad (11)$$

where: ζ = damping factor
ω_n = natural frequency

The damping factor and natural frequency of (10) can be extracted:

$$\omega_n = \sqrt{\frac{nK_OK_d}{C_1(1-\alpha T_OnK_OK_dR_1)}} \quad (12)$$

$$\zeta = \frac{R_1-\frac{\alpha T_O}{C_1}}{2}\sqrt{\frac{nK_OK_dC_1}{1-\alpha T_OnK_OK_dR_1}} \quad (13)$$

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Substituting (8) into (4) gives the transfer function for Idle mode:

$$\frac{\theta_0(s)}{\theta_r(s)} = \frac{\frac{nK_0K_d}{C_1}(sR_1C_1+1)}{s^2+s(nK_0K_dR_1)+\frac{nK_0K_d}{C_1}} \quad (14)$$

Again, this is in the form of a second order transfer function. The damping factor and natural frequency are found to be:

$$\omega_n = \sqrt{\frac{nK_0K_d}{C_1}} \quad (15)$$

$$\zeta = \frac{R_1}{2}\sqrt{nK_0K_dC_1} \quad (16)$$

To design the loop for proper read mode operation using (12) and (13), R, and C, must be found in terms of the damping factor and natural frequency.

To do this, first find ζ/ω_n, then solve for R_1C_1.

$$R_1C_1 = \frac{2\zeta}{\omega_n} + \alpha T_0 \quad (17)$$

Substitute this value for R_1C_1 into the equation for ω_n and solve for C_1.

$$C_1 = \frac{nK_0K_d}{\omega_n^2} + \alpha T_0 nK_0K_d\left(\frac{2\zeta}{\omega_n} + \alpha T_0\right) \quad (18)$$

Now that C_1 is known, R_1 can be found by dividing (17) through by C_1.

$$R_1 = \left(\frac{2\zeta}{\omega_n} + \alpha T_0\right)\frac{1}{C_1} \quad (19)$$

EXAMPLE 1

Assume that the data rate is 0.6 Mbit/s, $\zeta = 0.7$, a length of 20 2T patterns for the loop to lock is used, and $\omega_n t = 5.7$ for error < 1%.

n = 0.5 due to the 2T pattern.

$$T_0 = \frac{1}{f_0} = \frac{1}{1.2 \cdot 10^6} = 833\text{ns}$$

$\omega_0 = 2\pi f_0 = 2\pi (1.2 \cdot 10^6) = 7.54 \cdot 10^6$ rad/s

$\alpha_0 = 0.5$

For the SSI 34P553: $RR = \frac{5.97}{DR} - 1.79(\text{k}\Omega) = 8.17\text{k}\Omega$

where DR = Data Rate in Mbit/s

$$K_0 = 0.17\omega_0 = 1.28 \cdot 10^6 \frac{\text{rad/sec}}{\text{Volt}}$$

$$K_d = \frac{0.62}{RR+500} = 71.51 \cdot 10^{-6}\ \text{A/rad}$$

$K_T = 0.17\pi = 0.534$

Assuming a length of 20 2T patterns, then:
t = (20) (2) (833) ns = 33.3 µs

$$\omega n = \frac{5.7}{33.3\mu s} = 1.71 \cdot 10^5\ \text{rad/s}$$

C_1 = 1565 pF + 165.6 pF = 1.73 nF

R_1 = 5.02 kΩ

The resulting loop filter is shown in Figure 13.

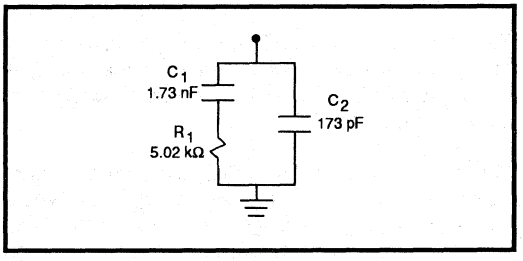


FIGURE 13

The value of $C_2 = C_1/10$ is chosen to damp out transients on the FILT pin and meet the requirement $C_2 \ll C_1$.

When the loop locks to the reference oscillator in Idle mode, the loop transfer function is given by (14), and ω_n and ζ are given by (15) and (16). R_1 and C_1 from Example 1 can be substituted into these equations to find the resulting natural frequency and damping factor in Idle mode.

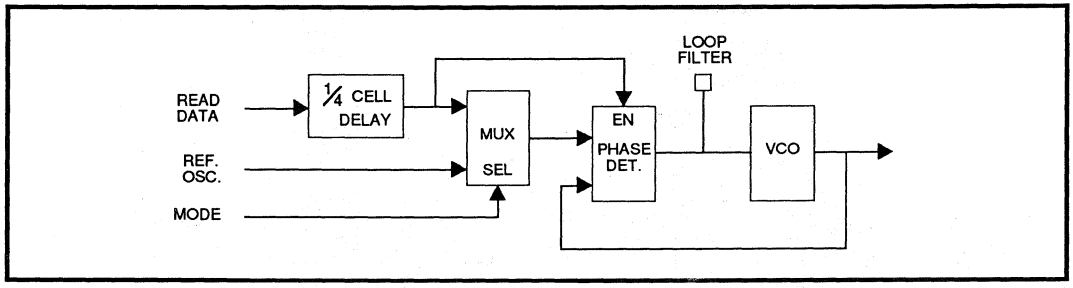


FIGURE 14A: Standard Configuration of a Data Synchronizer Phase-Locked Loop

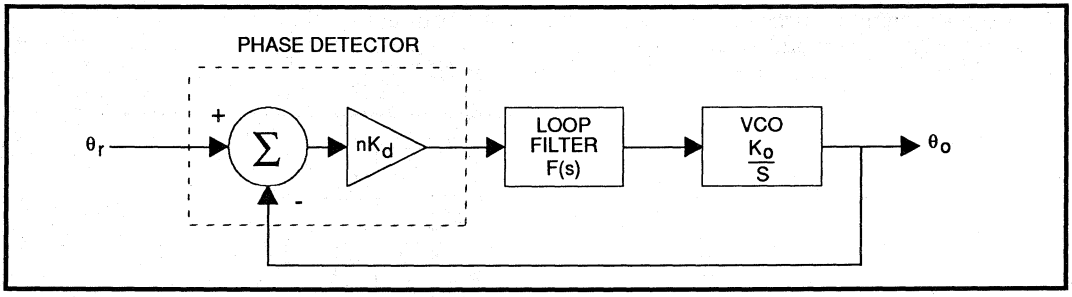


FIGURE 14B: Phase-Lock Loop System Representation

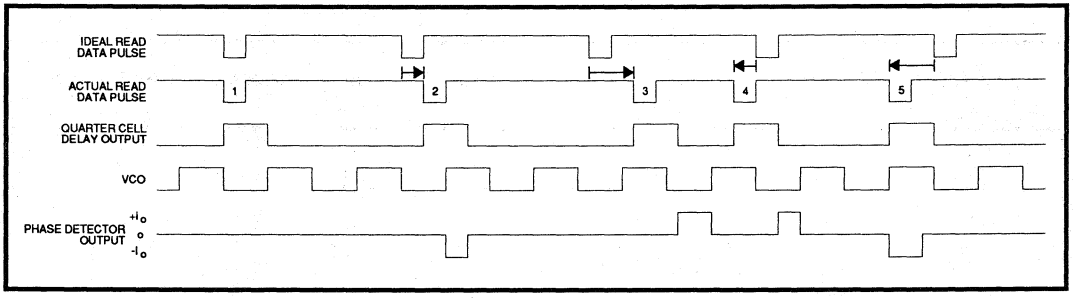


FIGURE 15A: Phase Detector Timing with Ideal Quarter Cell Delay. For an ideal pulse (1), there is no phase detector output. When a pulse is shifted late (2) or early (4) by less than the quarter cell delay time, the phase detector output is negative or positive, respectively. When the read data is shifted late (3) or early (5) by more than the quarter cell delay time, a phase detector output polarity error occurs. In this case, the output polarity becomes positive for a late shifted pulse and negative for an early shifted pulse.

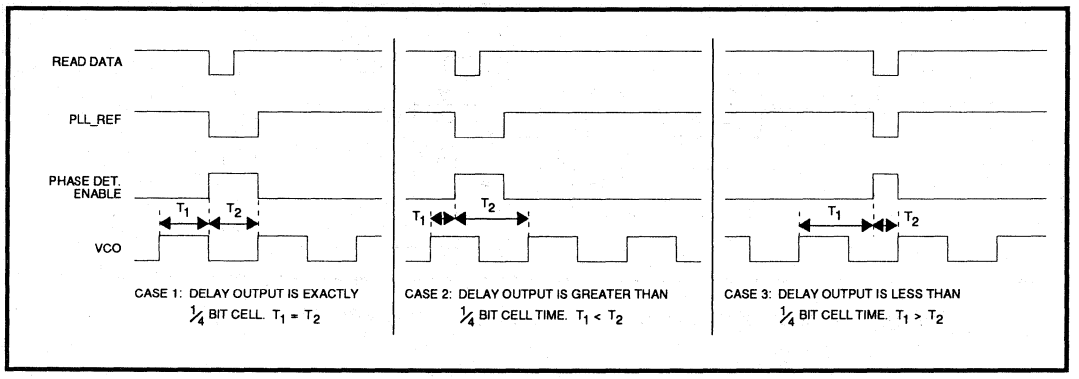


FIGURE 15B: Timing of Phase Detector Enable Logic. The read data input pulse can shift to the left by T1 and to the right by T2 before an error occurs in the phase detector output polarity, If the quarter cell delay output is not exactly 1/4 bit cell wide, then T1 ≠ T2, as shown in cases 2 and 3.

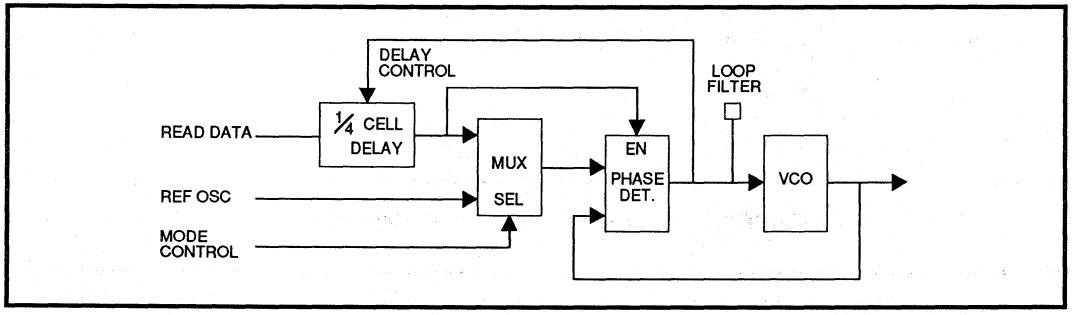


FIGURE 16A: Modified Data Synchronizer Phase-Locked-Loop with Quarter Cell Delay Control

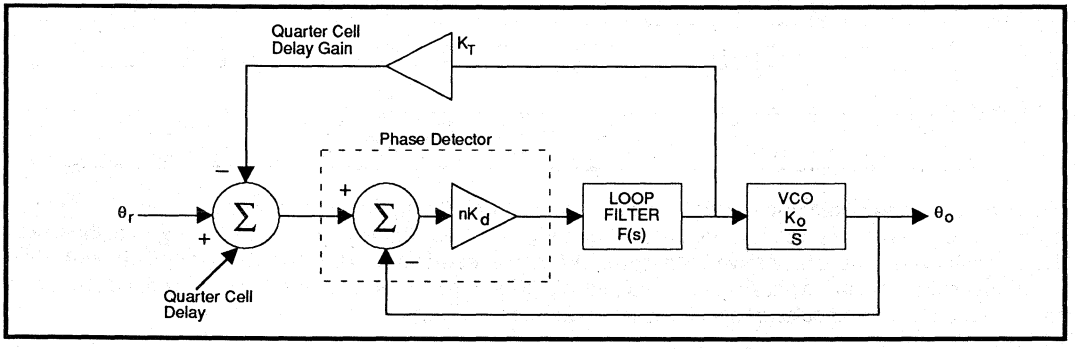
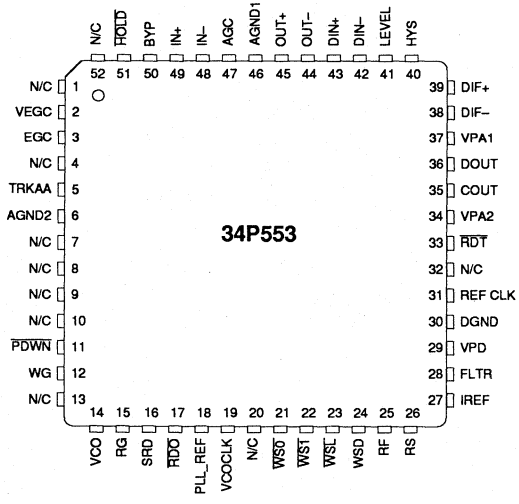


FIGURE 16B: Modified Data Synchronizer System Representation

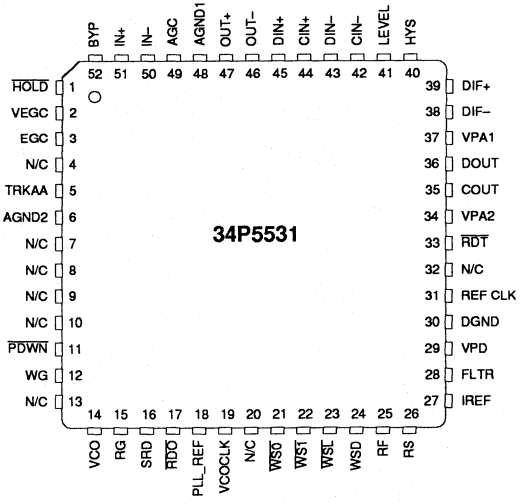
PACKAGE PIN DESIGNATIONS
(Top View)

THERMAL CHARACTERISTICS: θja

52-Lead QFP	75° C/W



52-Lead QFP



52-Lead QFP

CAUTION: Use handling procedures necessary for a static sensitive component.

ORDERING INFORMATION

PART DESCRIPTION	ORDERING NUMBER	PACKAGE MARK
SSI 32P553 Pulse Detector & Data Synchronizer		
52-Lead QFP	32P553-CG	32P553-CG
SSI 32P5531 Pulse Detector & Data Synchronizer		
52-Lead QFP	32P5531-CG	32P5531-CG

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Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914

Notes:

silicon systems®
A TDK Group Company

SSI 34P3200
Pulse Detector & Data Synchronizer for High Density Floppy Storage

Preliminary Data

December 1993

DESCRIPTION

The SSI 34P3200 is a high performance pulse detector and data synchronizer integrated circuit. This device is designed for use in high density floppy storage applications conforming to the JEIDA standard. The pulse detection portion of this device detects and validates amplitude peaks output from a disk drive read amplifier. The data synchronization portion is a 2,7 RLL or MFM data synchronizer with window shift and write pre-compensation capability. The SSI 34P3200 supports a Sleep mode for minimal power dissipation in non-operational periods.

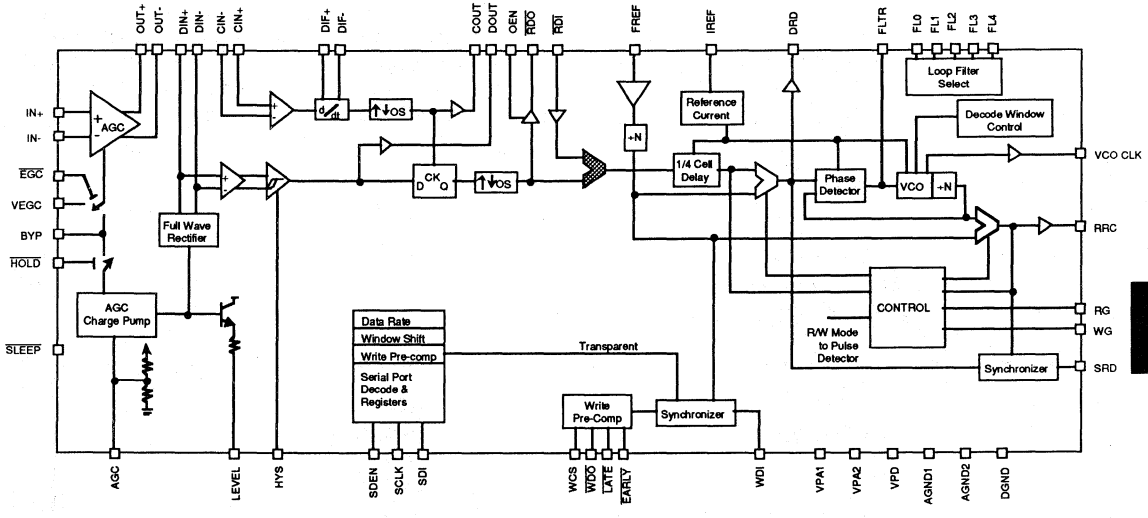
The SSI 34P3200 features a 3-pin serial port for easy selection of data rate and operating configurations

The SSI 34P3200 is available in a 52-lead QFP package.

FEATURES

- **Highly Integrated Pulse Detector & Data Synchronizer**
- **Ideal for High Density Floppy Storage Application in JEIDA Standard**
- **Operating Data Rate: 250K/500K/1M/2M/3M/ 4.5M/6M NRZ bits per second**
- **Supports 2,7 RLL or MFM Encoding Format**
- **3-Pin Serial Port Programming: Data Rate Selection, Window Symmetry Control & Test Mode**
- **Fast Acquisition Phase Lock Loop & Zero Phase Restart Technique**
- **5V Operation only**
- **Low Operating Power**
- **Sleep Mode**

BLOCK DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

SSI 34P3200
Pulse Detector & Data Synchronizer for High Density Floppy Storage

FUNCTIONAL DESCRIPTION

The SSI 34P3200 is a pulse detector and data synchronizer circuit. Its three main functions are:

- Validate and time-position preserve the analog pulses (IN±) from a read-write pre-amplifier.
- Extract the encoded data bit and its corresponding clock signal.
- Provide write precompensation function for write data signal.

The SSI 34P3200 major functional blocks are:

- AGC amplifier & AGC control
- Pulse qualifier
- Data synchronizer
- Window shift
- Write precompensation
- Serial port decode & registers

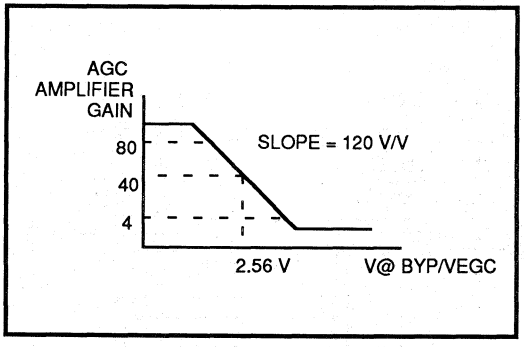


FIGURE 1: AGC Amplifier Gain vs BYP/VEGC Voltage

AGC AMPLIFIER & AGC CONTROL

The AGC amplifier provides signal amplification prior to pulse qualification. The amplifier gain is a linear function of a gain control voltage, Figure 1. The gain control voltage is either the BYP voltage when $\overline{EGC}$ = logic high, or the VEGC voltage when $\overline{EGC}$ = logic low.

In the normal Read mode, i.e., with the AGC active, the DIN± input signal is regulated to a nominal level which is set by the voltage at the AGC pin. With the AGC pin open, the nominal DIN± level is 1 V_{PPD} (peak-to-peak differential). This nominal DIN± level can be adjusted with an external resistor tied from the AGC pin to either VPA1 or AGND1, as shown in Figure 2. The DIN± voltage level is nominally 1.0 Vppd/V x V_{AGC}.

The AGC actions are current charging and discharging the external BYP integrating capacitor. They are described as follows:

Slow Decay

When the instantaneous DIN± signal is below the nominal level, a slow decay current, 4.5 µA, discharges the BYP capacitor. The AGC amplifier gain is increased slowly.

Slow Attack

When the instantaneous DIN± signal exceeds the nominal level but is below 125% of the nominal level, a slow attack current, 0.18 mA, charges the BYP capacitor. The AGC amplifier gain is decreased.

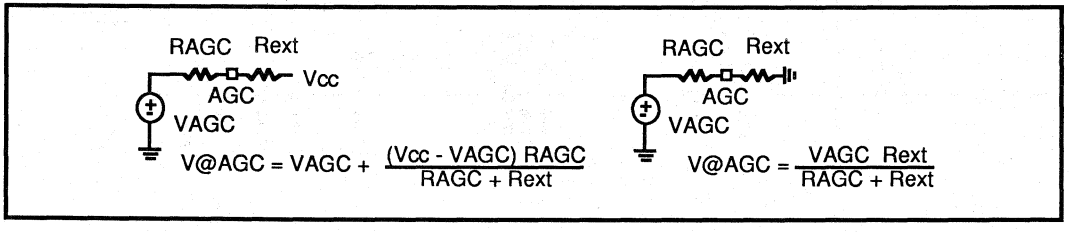


FIGURE 2: AGC Loop Reference Adjustment

Fast Attack

When the instantaneous DIN± signal exceeds 125% of the nominal level, the device enters a fast attack mode. A fast attack current, 1.3 mA, charges the BYP capacitor. The AGC amplifier gain is quickly lowered.

Write-to-Read Recovery

With a logic high to logic low transition of the WG, the SSI 34P3200 enters the write-to-read recovery mode. The input impedance remains in low impedance state for 0.9 µs for fast input DC coupling recovery. Then, the device restores to high input impedance state, and enters into a fast decay mode for 0.9 µs. In the fast decay mode, a continuous 0.12 mA current discharges the BYP capacitor. The AGC amplifier gain is increased very quickly. (Otherwise only the slow decay mode is available to increase the AGC amplifier gain.) Figure 3 shows the write-to-read AGC action timing.

The following AGC actions, except that of write-to-read recovery, can be suspended with the $\overline{HOLD}$ = logic low. The AGC amplifier gain is then held constant, except for leakage effect.

With $\overline{EGC}$ = logic low, the AGC amplifier gain is determined by the VEGC voltage. With a fixed external DC voltage, or a second AGC control loop at the VEGC pin, the AGC amplifier gain is set independent of the on-chip AGC control loop, such as when read signal is over a servo demodulation field.

The AGC amplifier outputs are emitter follower outputs.

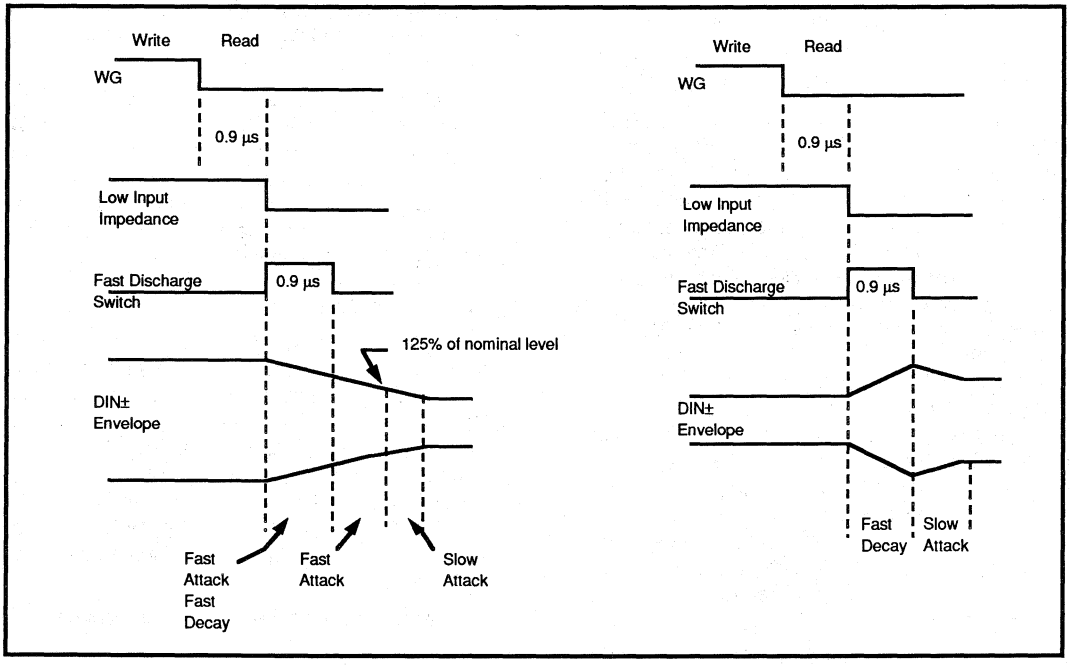


FIGURE 3: AGC Action Timing in Write-to-Read Recovery

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FUNCTIONAL DESCRIPTION (continued)

PULSE QUALIFIER

The pulse qualifier validates each DIN± peak by a combination of level qualification and time qualification. In level qualification, a hysteresis comparator eliminates errors due to low level additive noise. In time qualification, the AGC amplifier output is time differentiated to locate the signal peaks in time.

Level Qualification

The level qualification is accomplished by comparing the DIN± signal with a set threshold. The SSI 34P3200 allows two ways of setting the thresholds: fixed threshold or DIN± tracking threshold. Fixed threshold can be simply set by a DC voltage at the HYS pin, such as a resistor from VPA1 to ground. The threshold at the comparator can be computed as:

Hysteresis Gain x V@HYS.

For high performance system application, however, DIN± tracking threshold is recommended.

DIN± tracking threshold has the advantage of shorter write-to-read recovery time and lower probability of error with input amplitude drop out. The threshold is designed as a percentage of the DIN± peak voltage. This technique can be implemented by feeding the LEVEL output, through a resistor divider, to the HYS pin. The LEVEL output, amplified peak capture of DIN± signal, can be computed as: Level Gain x DIN± ppd. With the resistor divider, a fraction of the LEVEL output is presented at the HYS pin. The threshold, as a function of DIN±, can be summarized as: Level Gain x Resistor Dividing Ratio x Hysteresis Gain x DIN± ppd. For a typical case of 1 Vppd DIN± signal, assume equal value resistors in the divider network, the threshold is 1 x 0.5 x 0.36 x 1 =0.18V. This represents 36% threshold on a 1 Vppd signal. While both the Level Gain and the Hysteresis Gain bear a moderate tolerance due to typical process variation, they inversely track each other to yield a much tighter threshold accuracy in a closed loop.

While the external resistor divider ratio determines the qualification setting, the total resistance and the peak capture capacitor should be optimized for the system data rate. The RC time constant must be small enough to allow good response to changing DIN± peak, but large enough to provide a constant threshold after a long duration of input absence.

Time Qualification

Time qualification is used to locate DIN± peaks. With time differentiation, each DIN± peak is translated into a zero crossing, which clocks a on-chip flip-flop in the pulse qualifier. The SSI 34P3200 supports on-chip or off-chip differentiation.

On-Chip Differentiation

The on-chip differentiation is accomplished by connecting an external RLC network across the DIF± pins. The DIN+ and CIN+ pins should be tied together, as well as the DIN- and CIN- pins.

Off-Chip Differentiation

For constant density recording applications, a differentiation function with a low pass cut-off frequency tracking the data rate can maximize the signal-to-noise ratio performance. A time differentiated input can be applied at the CIN± pins, separated from the DIN± pins. A 3.5 kΩ resistor should be placed across the DIF± pins.

This function can best be supported by the Silicon Systems programmable filters, such as the SSI 32F8030, F8130/8131. The filters feature both a normal low pass output and a differentiated low pass output. The low pass cut-off frequency is programmable by the user to track the data rate. The signal delays of the two signal paths are well matched.

Qualified Read Data

Upon level and time qualification, a one-shot data pulse is generated for every validated peak of the DIN± signal. This read data pulse can be monitored at the $\overline{\text{RDO}}$ pin, when OEN = Logic high. In high speed normal Read mode, it is recommended that the $\overline{\text{RDO}}$ output be disabled for lower noise performance with OEN = Logic low. The pulse detector read data can be used as input to the data synchronizer. Alternately, external input at the $\overline{\text{RDI}}$ pin can be used as input to the data synchronizer.

Figure 4 summarizes the pulse detector function.

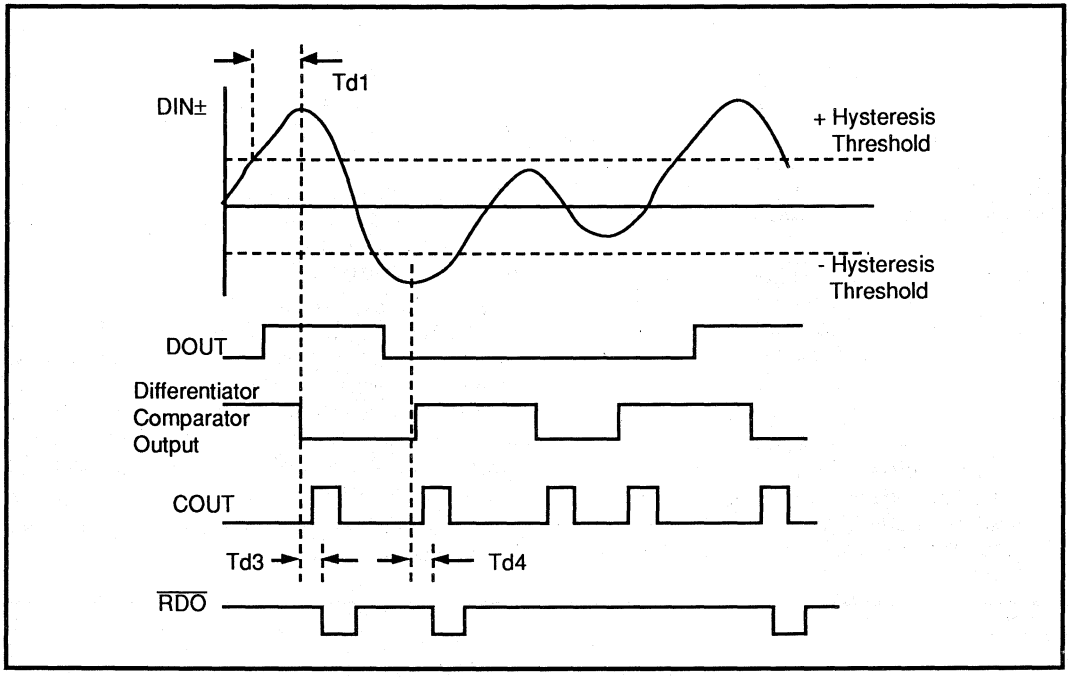


FIGURE 4: Read Mode Pulse Detector Timing

DATA SYNCHRONIZER

The data synchronizer is used to extract the clock and the encoded data signals from the read data signal. The input source to the data synchronizer can be from the pulse qualifier or from an external source via the $\overline{RDI}$ pin.

The SSI 34P3200 is designed to perform data synchronization for the following operating data rates, which are selected through a serial port register R0:

Rate	NRZ Data Rate	Encoding Format
1	6 Mbit/s	2,7 RLL
2	4.5 Mbit/s	2,7 RLL
3	3 Mbit/s	2,7 RLL
4	2 Mbit/s	MFM
5	1 Mbit/s	MFM
6	500 Kbit/s	MFM
7	250 Kbit/s	MFM

For both the 2,7 RLL and MFM encoding formats, the encoded bit rate, as well as the data synchronizer clock, is at twice the NRZ data rate. Thus, the required data synchronizer clock rate is from 500 kHz to 12 MHz.

To accommodate the wide data rate dynamic range, the SSI 34P3200 employs a novel data synchronizer phase locked loop (PLL) architecture (see block diagram). While the voltage controlled oscillator (VCO) operates only between 6 MHz to 12 MHz, a divide-down function is used to generate the lower frequency clock. For Rates 1-3, the VCO operates at 12 MHz, 9 MHz and 6 MHz, respectively. For Rates 4-7, the VCO operates at 8 MHz and the divide-down factor, N, is from 2 to 16.

FUNCTIONAL DESCRIPTION (continued)

DATA SYNCHRONIZER (continued)

With the serial register R0 programmed for a specific data rate, the SSI 34P3200 would properly decode the proper VCO frequency and the divide-down factor. Furthermore, the 1/4 cell delay duration, i.e., one half of the encoded bit period, is also set properly for each operating mode.

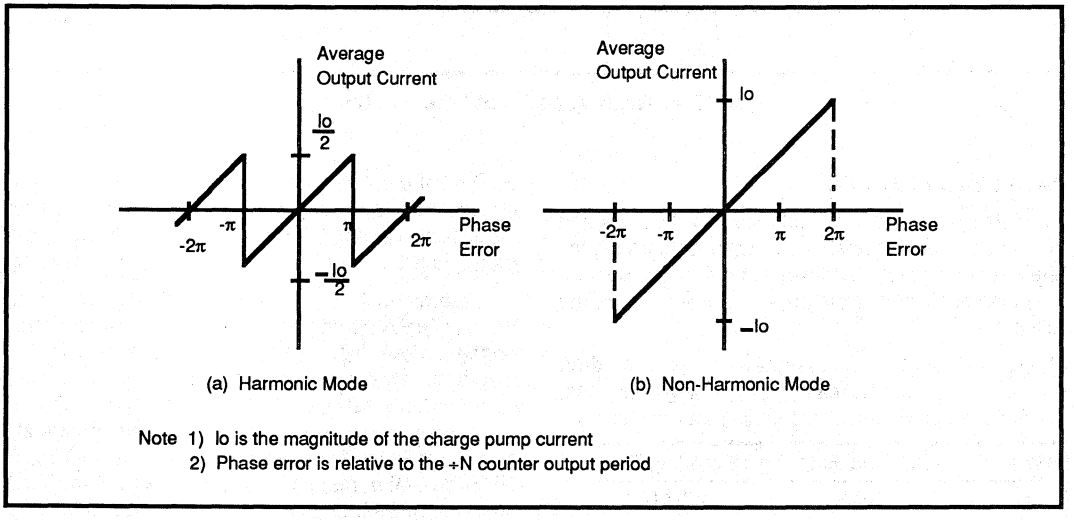
When the SSI 34P3200 is in the Idle mode, the VCO should lock to an external reference clock, FREF. For Rates 1-3, the FREF should be 12 MHz, 9 MHz and 6 MHz, respectively. For Rates 4-7, the FREF should be 8 MHz.

The SSI 34P3200 employs a dual mode phase detector: harmonic in the Read mode and non-harmonic in the Write and Idle modes. In the Read mode, the harmonic phase detector updates the PLL with each occurrence of a read data pulse from the pulse qualifier. In the Write and Idle modes, the non-harmonic phase detector is continuously enabled, thus maintaining both phase and frequency lock. Figure 5 shows the phase detector transfer function. By acquiring both phase and frequency lock to the FREF and utilizing a zero phase restart technique, false lock to the pulse detector read data is eliminated.

The phase detector incorporates a charge pump in order to drive the loop filter directly. The polarity and width of the output current pulses correspond to the direction and magnitude of the phase error.

Because of the wide data rate dynamic range, the SSI 34P3200 provides four high impedance/low impedance switchable nodes, FL1-4, for external loop filter component switching. When the node is in high impedance state, the external component connected to this node is switched out. When the node is in low impedance state, the external component is included in the loop filter network.

The various operating modes of the data synchronizer are discussed in the following section.



Note 1) Io is the magnitude of the charge pump current
2) Phase error is relative to the ÷N counter output period

FIGURE 5: Phase Detector Transfer Function

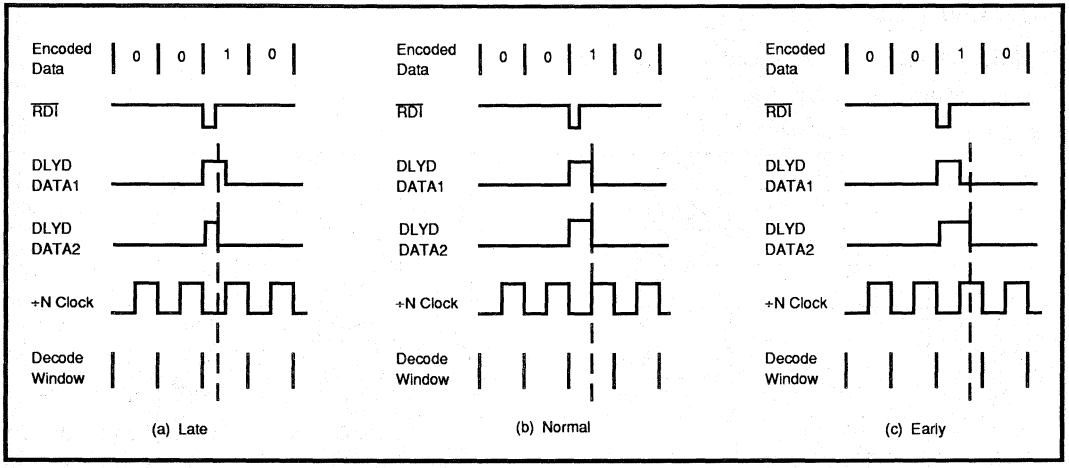


FIGURE 6: Decode Window & Window Shift Directions

WINDOW SHIFT

To enhance the data decode function, the SSI 34P3200 supports a window shift function for the highest three data rate operations. Shifting the pulse width of the ¼ cell delay output shifts the relative position of the DLYD DATA pulse within the decode window. This powerful capability, supported through serial register R1, easily facilitates defect mappings, automatic calibration, window margin testing, error recovery, and systematic error cancellation.

The window shift can be set to ±5%, ±7.5% or ±10% of the decode window. Figure 6 defines the direction of the window shift. Refer to the Serial Port Decode & Registers section for serial port register assignment.

WRITE PRECOMPENSATION

Write precompensation circuitry is provided to compensate for media bit shift caused by intersymbol interference. The magnitude of the time shift, TPC, is determined by an external resistor on the WCS pin, with Rp from WCS to VPA2. TPC is given as:

$$TPC = 1.6 \times 10^{-3} R_p ns$$

SERIAL PORT DECODE & REGISTERS

The SSI 34P3200 provides a 3-pin serial port to facilitate the following digital controls:

- Data rate (Register 0: Bits 2-0)
- Window shift (Register 1: Bits 3-0)
- Write pre-comp (Register 2: Bit 0)
- Data synchronizer input source (Register 2: Bit 2)

The 3 serial port pins are SDEN, SDI and SCLK. Figure 7 shows a timing diagram of the serial data transmission. Each data transmission consists of a 8-bit packet. Bit 7 being the most significant bit (MSB). The 8-bit packet is divided into two fields: Bit7-4 address field, Bit 3-0 data field. These registers are reset to 0 when the power-on function is used.

FUNCTIONAL DESCRIPTION (continued)

SERIAL PORT DECODE & REGISTERS (continued)

The register assignment is as follows:

Register 0 Address 0000

Bit 3	Not used							
Bit 2-0	NRZ Data Rate	VCOFrequency	Divide Down	FL0	FL1	FL2	FL3	FL4
000	6 Mbit/s	12 MHz	1	LowZ	Hi-Z	Hi-Z	Hi-Z	Hi-Z
001	4.5 Mbit/s	9 MHz	1	LowZ	Hi-Z	Hi-Z	Hi-Z	Hi-Z
010	3 Mbit/s	6 MHz	1	LowZ	Hi-Z	Hi-Z	Hi-Z	Hi-Z
011	2 Mbit/s	8 MHz	2	Hi-Z	LowZ	Hi-Z	Hi-Z	Hi-Z
100	1 Mbit/s	8 MHz	4	Hi-Z	LowZ	LowZ	Hi-Z	Hi-Z
101	500 Kbit/s	8 MHz	8	Hi-Z	LowZ	LowZ	LowZ	Hi-Z
110	250 Kbit/s	8 MHz	16	Hi-Z	LowZ	LowZ	LowZ	LowZ

Register 1 Address 0001

The window shift function is available for the 6 Mbit/s, 4.5 Mbit/s and 3 Mbit/s data rates.

Bit 3	Window shift Enable
0	Disabled
1	Enabled
Bit 2	Window shift direction
0	Early
1	Late
Bits 1-0	Window shift magnitude
00	10 % of RRC period
01	7.5 %
10	5 %
11	0 %

Register 2 Address 0010

Bits 3, 1	Not used
Bit 2	Data Synchronizer Input Source
0	From internal pulse qualifier output
1	From the $\overline{RDI}$ pin
Bit 0	Write Pass Through
1	Write synchronizer is a simple buffer
0	Write synchronizer & pre-comp is active

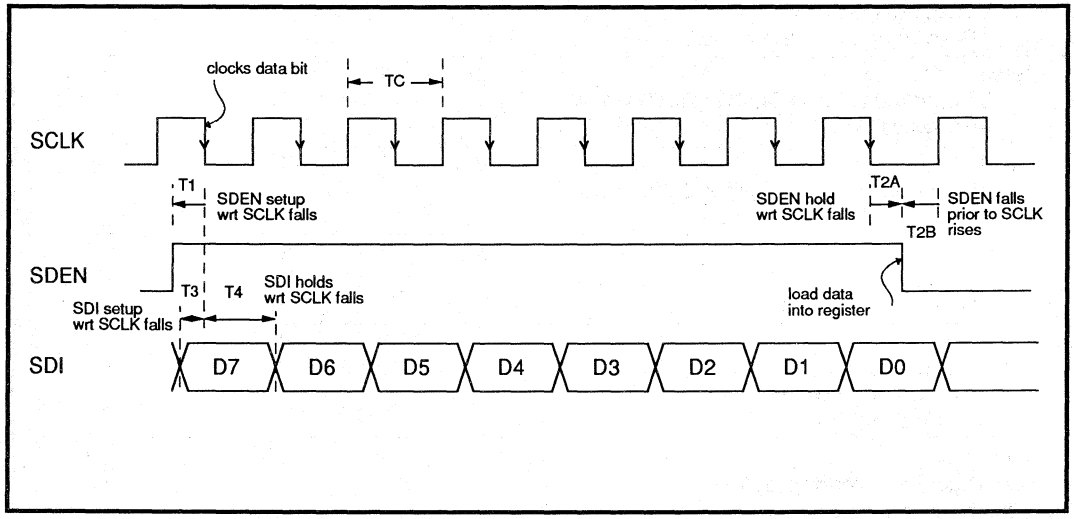


FIGURE 7: Serial Port Timing

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OPERATION MODES

The SSI 32P3200 can support the following operating modes:

Mode	WG	RG	$\overline{\text{HOLD}}$	$\overline{\text{EGC}}$	$\overline{\text{SLEEP}}$
Idle VCO locked to FREF AGC active	0	0	1	1	1
Idle VCO locked to FREF AGC gain held constant by BYP	0	0	0	1	1
Idle VCO locked to FREF AGC gain held constant by VEGC	0	0	X	0	1
Read VCO locked to Pulse Qualifier DLYD DATA AGC active	0	1	1	1	1
Read VCO locked to Pulse Qualifier DLYD DATA AGC gain held constant by BYP	0	1	0	1	1
Read VCO locked to Pulse Qualifier DLYD DATA AGC gain held constant by VEGC	0	1	X	0	1
Write AGC gain held constant by BYP Input impedance lowered VCO locked to FREF	1	X	X	1	1
Write AGC gain held constant by VEGC Input impedance lowered VCO locked to FREF	1	X	X	0	1
Power Shutdown	X	X	X	X	0

READ MODE

In the Read mode, the rising edge of DLYD DATA enables the phase detector while the falling edge is phase compared to the rising edge of the ÷N counter. As depicted in Figure 8, DLYD DATA is 1/4 cell wide (TVCO / 2 / N) pulse whose leading edge is defined by the leading edge of Read Data. RRC is generated from the rising edge of the ÷N counter output. The accuracy of the 1/4 cell delay only affects the retrace angle of the phase detector and does not influence the accuracy of RRC.

In the non-Read modes, the PLL is locked to FREF. This forces the VCO to run at a frequency which is very close to that required for tracking actual data and thus minimizes the associated frequency step during acquisition. When RG transitions, the VCO is stopped momentarily, then restarted in an accurate phase alignment with the next PLL reference input pulse. By minimizing the phase alignment in this manner (phase error ≤ 0.5 rads), the acquisition time is substantially reduced.

With the PLL in lock, the encoded data bit is re-synchronized before output to the SRD pin. Figure 9 shows the Read mode timing.

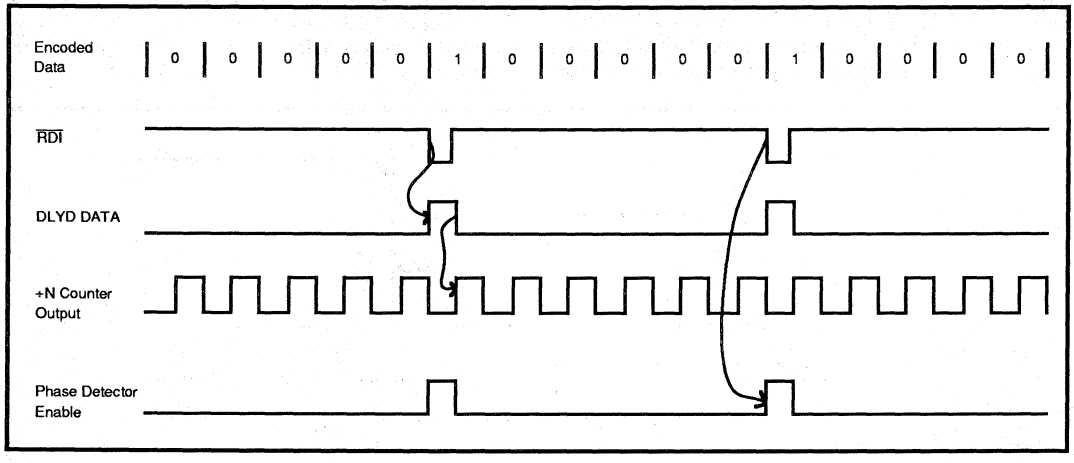

FIGURE 8: Data Sychronizer Timing

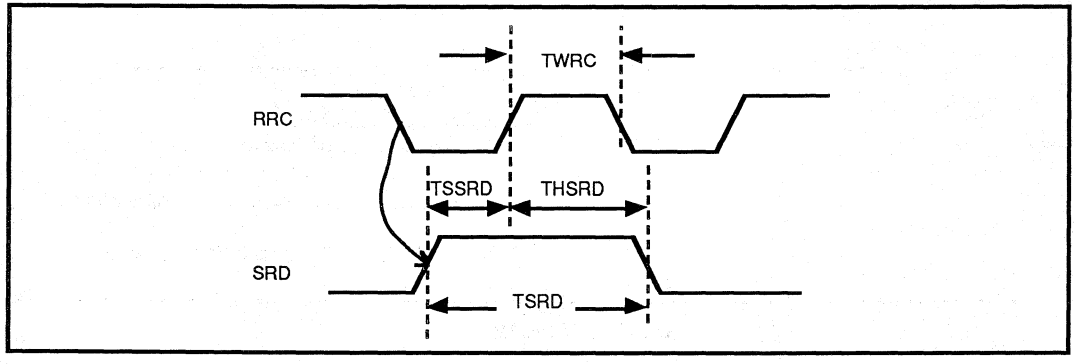

FIGURE 9: Read Mode Timing

OPERATION MODES (continued)

WRITE MODE

In the Write mode, the SSI 34P3200 pulse detector is disabled and preset for the subsequent Read mode. The digital circuitry is disabled, the input AGC amplifier gain is held at its previous value and the AGC amplifier input impedance is reduced.

Holding the AGC amplifier gain and reducing input impedance shortens system write-to-read recovery times.

The lowered input impedance improves settling time by reducing the time constant of the network between the SSI 34P3200 and a head preamplifier such as the SSI 34R1203R. Write-to-read timing is controlled to maintain the reduced impedance for 0.9 µs before the AGC circuitry is activated. Coupling capacitors should be chosen with as low a value as possible consistent with adequate bandwidth to allow more rapid settling.

Write Data Input can be re-synchronized to the Read Reference Clock before feeding to a write driver. Figure 10 shows the Write mode timing.

By a serial register bit control, the SSI 34P3200 can be placed in the write pass through mode. The synchronizer and the pre-comp function are disabled and act as a buffer only.

POWER SHUTDOWN

For reduced power dissipation during non-operational periods, the SSI 34P3200 can be switched into a Sleep mode. The serial port registers will remain powered up during Sleep mode. Therefore no reprogramming is required following a logic low to logic high $\overline{\text{SLEEP}}$ transition.

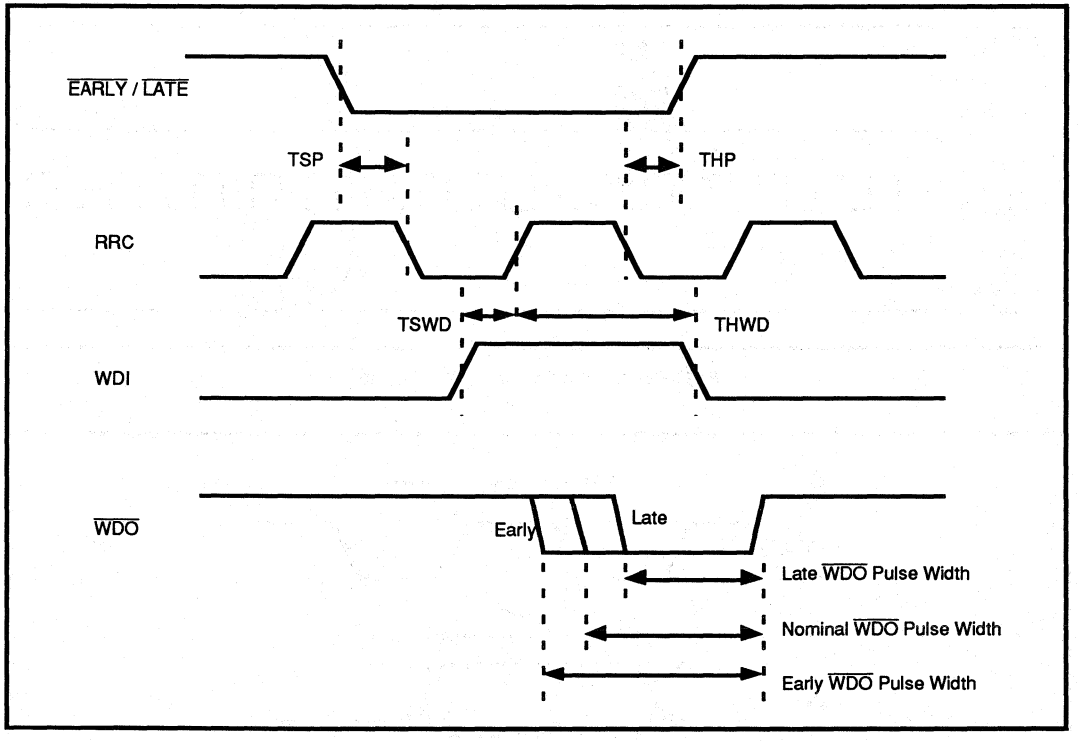

FIGURE 10: Write Mode Timing

PIN DESCRIPTION

ANALOG INPUT PINS

NAME	TYPE	DESCRIPTION
IN+, IN-	I	AGC amplifier inputs.
DIN+, DIN-	I	Data inputs to hysteresis comparator and full-wave rectifier.
CIN+, CIN-	I	Data inputs to time-channel qualification.
HYS	I	Hysteresis input to establish the hysteresis threshold of the data comparator.
AGC	I	The voltage at the AGC pin determines the nominal level at the DIN± pins.
BYP	I	The voltage at the BYP pin controls the AGC amplifier gain when $\overline{EGC}$ = logic high.
VEGC	I	The voltage at the VEGC pin controls the AGC amplifier gain when $\overline{EGC}$ = logic low.

DIGITAL INPUT PINS:

FREF	I	TTL reference clock input to data synchronizer.
OEN	I	TTL $\overline{RDO}$ Output Enable input: $\overline{RDO}$ enabled with OEN=logic high, $\overline{RDO}$ forced to high with OEN=logic low.
$\overline{RDI}$	I	TTL external input source to the data synchronizer.
RG	I	TTL Read Gate input.
WG	I	TTL Write Gate input. Enables Write mode.
WDI	I	TTL Write Data Input.
$\overline{EARLY}$	I	TTL write precompensation control input to shift write data pulse early.
$\overline{LATE}$	I	TTL write precompensation control input to shift write data pulse late.
$\overline{SLEEP}$	I	TTL power shutdown control. The device is in power shutdown mode when $\overline{SLEEP}$ = logic low. The device is in normal operational state when $\overline{SLEEP}$ = logic high, or left open.
$\overline{HOLD}$	I	TTL input that holds the AGC gain constant when pulled to low. When left open, this input is at logic high.
$\overline{EGC}$	I	TTL input. When $\overline{EGC}$ = logic low, the AGC amplifier gain is controlled by the voltage at VEGC.When $\overline{EGC}$ = logic high, or left open, the AGC amplifier gain is controlled by the voltage at BYP.
SDI	I	TTL Serial Data Input.
SCLK	I	TTL Serial Clock. Negative edge triggered clock input for serial register.
SDEN	I	TTL Serial Data Enable. A high level input enables data loading. The data is latched on the falling edge of SDEN.

PIN DESCRIPTION (continued)

ANALOG OUTPUT PINS:

NAME	TYPE	DESCRIPTION
OUT+, OUT-	O	AGC amplifier emitter follower output pins.
LEVEL	O	Open emitter output from fullwave rectifier that may be used for input to the HYS pin.
FL0-4	O	Loop filter connection pins. Either high impedance or low impedance state.

ANALOG CONTROL PINS:

DIF+, DIF-	-	Pins for external differentiating network. When off-chip differentiator is used, a 3.5 kΩ resistor should be tied across DIF+ and DIF-.
IREF	-	Input reference current for VCO bias. A 7.5 kΩ resistor should be tied between IREF and VPA2.
FLTR	-	Loop filter pin.
WCS	-	Write precomp set: used to set the magnitude of the write pre-compensation time via an external resistor, Rp to AGND2.

DIGITAL OUTPUT PINS:

$\overline{\text{RDO}}$	O	TTL output of the pulse detector read data. This output is enabled with OEN=logic high. It is forced to high with OEN=logic low.
RRC	O	Read Reference Clock: a multiplexed TTL clock source used by the controller. In the Read mode, this clock is the encoded bit rate. In the Write mode, it is the FREF divided down by the N factor. No short clock pulses are generated during a mode change.
SRD	O	Synchronized Read Data: a TTL read data that has been re-synchronized to read clock.
$\overline{\text{WDO}}$	O	Write Data Output: a TTL output that is an input to the R/W amplifier.
COUT	O	Time qualification one-shot test point: open emitter output which requires an external 1 kΩ pull down resistor when used. The pin should be left open in normal operation to reduce power.
DOUT	O	Data comparator test point: open emitter output which requires an external 1 kΩ pull down resistor when used. The pin should be left open in normal operation to reduce power.
DRD	O	Delay Read Data test point: open emitter output which requires an external 5 kΩ pull down resistor when used.
VCO CLK	O	VCO test point: open emitter output which requires an external 5 kΩ pull down resistor when used.

POWER & GROUND

NAME	TYPE	DESCRIPTION
VPA1	-	Analog supply to the pulse detector section.
VPA2	-	Analog supply to the data synchronizer section.
VPD	-	Digital supply.
AGND1	-	Analog ground to the pulse detector section.
AGND2	-	Analog ground to the data synchronizer section.
DGND	-	Digital ground.

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, the recommended operating conditions apply.

ABSOLUTE MAXIMUM RATINGS

Operation beyond the maximum ratings may damage the device.

PARAMETER	RATING
Storage Temperature	-65 to +150°C
Junction Operating Temperature	+130°C
Supply Voltage, VPA1-2, VPD	-0.7 to +7V
Voltage Applied to Inputs	-0.3 to Supply + 0.3V

RECOMMENDED OPERATING CONDITIONS

Supply Voltage	4.5V < VPA1, VPA2, VPD < 5.5V
Ambient Temperature, Ta	0°C < Ta < 70 °C

POWER SUPPLY

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Power Dissipation Active	PD	Outputs unloaded 4.5V < VPA1, VPA2, VPD < 5.5V		450	650	mW
Power Down Dissipation	PDS	Output unloaded; $\overline{\text{SLEEP}}$ = logic low		40	60	mW

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ELECTRICAL SPECIFICATIONS (continued)

LOGIC SIGNALS

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
TTL Input Low Voltage	VIL		-0.3		0.8	V
TTL Input High Voltage	VIH		2		VCC + 0.3	V
TTL Input Low Current	IIL	VIL = 0.4V	-0.4			mA
TTL Input High Current	IIH	VIH = 2.7V			0.1	mA
TTL Input Switching Time	TS	0.8V - 2.0V transition			0.1	µs
TTL Output Low Voltage	VOL	IOL = 4.0 mA			0.5	V
TTL Output High Voltage	VOH	IOH = -400 µA	2.7			V
Test Point Output High Voltage (DOUT, COUT)	VOHT1	1 kΩ to DGND		VPA - 2.4		V
Test Point Output Low Voltage (DOUT, COUT)	VOLT1	1 kΩ to DGND		VPA - 2.8		V
Test Point Output High Voltage (VCOCLK, DRD)	VOHT2	5 kΩ to DGND		4.2		V
Test Point Output Low Voltage (VCOCLK, DRD)	VOLT2	5 kΩ to DGND		3.6		V

MODE CONTROL

Read-to-Write Transition	TDRW	WG pin logic low to logic high			1	µs
Write-to-Read Transition	TDWR	WG pin logic high to logic low; AGC settling not included	0.5	0.9	1.3	µs
$\overline{\text{HOLD}}$ On to Off/Off to On Transition	TDH	$\overline{\text{HOLD}}$ pin high to/from low transition			1	µs
Power shutdown mode to Read/Write Delay	TDSL	Settling time of external capacitor not included		0.1		µs
Read/Write Mode to power shutdown Delay	TDOFF	Settling time of external capacitor not included		10		µs
Low Input Impedance Pulse Width	PWIMS	WG pin logic high to logic low. Not directly testable		0.9		µs
Fast Discharge Pulse Width	PWFDC	WG pin logic high to logic low following PWIMS. Not directly testable		0.9		µs

AGC AMPLIFIER

Unless otherwise specified, recommended operating conditions apply. Input signals, 100 mVppd at 1.0 MHz, are AC coupled to IN±. OUT± are AC coupled to DIN±.

A 2000 pF capacitor is connected between BYP and AGND1. AGC pin is open.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Minimum Gain Range	MIGR	1.0 Vppd ≤ OUT± ≤ 3.0 Vppd			4	V/V
Maximum Gain Range	MAGR		80			V/V
Output Offset Voltage Variation	VOS	Over entire gain range	-200	0	200	mV
Maximum Output Voltage Swing	VOMX	Set by AGC pin	3			Vppd
Differential Input Impedance	RIN	IN± = 100 mVppd		5		kΩ
Differential Input Capacitance	CIN	IN± = 100 mVppd @ 1.0 MHz			10	pF
Single Ended Input Impedance	ZCMH	WG = logic low, IN+ = IN-		1.5		kΩ
		WG = logic high, IN+ = IN-			250	Ω
Input Noise Voltage	VIN	Gain set to maximum, BW = 3 MHz, short IN+ to IN-			15	nV/√Hz
Bandwidth	BW	Gain set to maximum referenced to 1.0 MHz	15			MHz
Single Ended Output Impedance on OUT±	ROUT				100	Ω
Input Referred Common Mode Rejection	CMRR	IN+ = IN- = 100 mVpp @ 1.0 MHz gain set to maximum	40			dB
Input Referred Power Supply Rejection	PSRR	1.0 Vpp @ 1.0 MHz on VPA1 gain set to maximum	80			dB
DIN± Input Swing vs AGC Input	KAGC	25 mVppd ≤ IN± ≤ 250 mVppd ; $\overline{HOLD}$ = logic high 0.5 Vppd ≤ DIN± ≤ 1.5 Vppd	0.7	1	1.3	Vppd/V
DIN± Input Swing Variation with IN±	ΔDIN	25 mVppd ≤ IN± ≤ 250 mVppd	-6		6	%
AGC Open Voltage	VAGC	AGC open	0.8	1	1.2	V
AGC Pin Input Impedance	RAGC		2.5	3.8	6.0	kΩ
Slow AGC Discharge Current	ISD	DIN± = 0V	3	4.5	6	μA
Fast AGC Discharge Current	IFD	Starts at 0.9 μs after WG high to low transition Stops at 1.8 μs after WG high to low transition	0.08	0.12	0.16	mA
AGC Leakage Current	ILK	$\overline{HOLD}$ = logic low	-50	0	50	nA
Slow AGC Charge Current	ISC	DIN± = 0.8 VDC vary AGC until slow charge begins	-0.12	-0.18	-0.24	mA
Fast AGC Charge Current	IFC	DIN± = 0.8 VDC vary AGC until fast charge begins	-0.9	-1.3	-1.7	mA

ELECTRICAL SPECIFICATIONS (continued)

AGC AMPLIFIER (continued)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Fast to Slow Attack Switchover Point	FSSP	DIN±(fast) / DIN±(slow)		125		%
Gain Decay Time	TGD	IN± = 250 mVppd to 125 mVppd @ 1.0 MHz OUT± to 90% final value		12		µs
		IN± = 50 mVppd to 25 mVppd @ 1.0 MHz OUT± to 90% final value		60		µs
Gain Attack Time	TGA	WG = logic high to logic low IN± = 250 mVppd @ 1.0 MHz OUT± to 110% final value		2		µs

HYSTERESIS COMPARATOR

Unless otherwise specified, recommended operating conditions apply. Input DIN± is AC coupled, 1.0 Vppd @ 1.0 MHz sinewave. 0.5 VDC is applied to the HYS pin. WG = 0

Input Signal Range	IRHC				1.5	Vppd
Differential Input Resistance	RHCD	DIN± = 100 mVppd	15	20	25	kΩ
Differential Input Capacitance	CHCD	DIN± = 100 mVppd @ 1.0 MHz			5	pF
Single Ended Input Impedance	RHCC	DIN+ = DIN-	4	5	6	kΩ
Level Gain from DIN± to LEVEL	KLD	0.5 Vppd ≤ DIN± ≤ 1.5 Vppd 10 kΩ from LEVEL to AGND1 270 pF from LEVEL to AGND1	0.75	1	1.25	V/Vppd
Level Pin Output Offset Voltage	VLOS	DIN± = 0 Vppd; 10 kΩ from LEVEL to AGND1		100		mV
Level Pin Output Impedance	ZLV	I @ LEVEL = -0.2 mA, DIN± = 0.5 VDC		350		Ω
Level Pin Maximum Output Current	ILMX		1.5			mA
Hysteresis Gain	KHYS	0.3V < HYS < 1.0 V		0.36		V/V
HYS Pin Current	IHYS	0.5V < HYS < 1.5 V	-10		0	µA
Comparator Offset Voltage	VHCOS	HYS pin at AGND; < 1.5 kΩ across DIN+ to DIN- 5 kΩ from DOUT to DGND			10	mV

ACTIVE DIFFERENTIATOR

Unless otherwise specified, recommended operating conditions apply. Input CIN± is AC coupled, 1.0 Vppd, 1.0 MHz sinewave.

100Ω resistor in series with 220 pF capacitor are tied across DIF+ to DIF-.

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Input Signal Range	IRAD				1.5	V
Differential Input Resistance	RADD	CIN± = 100 mVppd	15	20	25	kΩ
Differential Input Capcitance	CADD	CIN± = 100 mVppd @ 2.0 MHz			5	pF
Single Ended Input Impedance	RADC	CIN+ = CIN-	4	5	6	kΩ
Voltage Gain from CIN± to DIF±	KAD	3.5 kΩ from DIF+ to DIF-		1		V/V
DIF+ to DIF- Pin Current	IDIF	Differentiator impedance must be set so as not to clip the signal for this current level	-1.0		1.0	mA
Comparator Offset Voltage	VADOS	DIF± AC coupled, 5 kΩ from COUT to DGND		0	5	mV
COUT Pin Output High Voltage	PWC	5 kΩ from COUT to DGND		30		ns

QUALIFIER TIMING

Unless otherwise specified, recommended operating conditions apply. Inputs CIN± and DIN± are in-place as AC coupled, 1.0 Vppd, 1.0 MHz sinewave. 100Ω resistor in series with 220 pF capacitor are tied from DIF+ to DIF-. 0.5V is applied to the HYS pin.

$\overline{RDO}$ is enabled as output. OEN = 1. WG = 0

D Flip Flop Set Up Time	TD1	Minimum allowable time delay from DIN± exceeding hysteresis point to DIF± hitting a peak value.	0			ns
Propagation Delay from Positive Peak to $\overline{RDO}$ Pulse	TD3			60		ns
Propagation Delay from Negative Peak to $\overline{RDO}$ Pulse	TD4			60		ns
Pulse Pairing | TD3 - TD4 |	PP				3	ns
$\overline{RDO}$ Pulse Width	TRD		20	25	30	ns

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ELECTRICAL SPECIFICATIONS (continued)

SYNCHRONIZER SECTION

WRITE MODE

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
Write Data Input Setup Time to RRC	TSWD	Rising edge of WDI to rising edge of RRC	15			ns
Write Data Input Hold Time after RRC	THWD	Falling edge of WDI to rising edge of RRC	3			ns
EARLY-/LATE- Input Setup Time to RRC	TSP	Falling edge of EARLY- / LATE- to falling edge of RRC	40			ns
EARLY-/LATE- Input Hold Time after RRC	THP	Rising edge of EARLY- / LATE- to second falling edge of RRC	10			ns
Precomp Time Shift Magnitude	TPC	TPC0 = 1.6 x 10^{-3} Rp VPA2 = 5.0V	0.8 x TPC0	TPC0	1.2 TPC0	ns
Write Data Output Pulse Width	TWD	CL ≤ 15 pF To = Read Reference Clock Period	T0 -2TPC0	T0 -TPC0	T0 + 2TPC0	ns
Write Pass Through Delay from WDI to $\overline{WDO}$	TPD				30	ns

READ MODE

Read Reference Clock Rise Time	TRRC	0.8V to 2.0V; CL ≤ 15 pF			8	ns
Read Reference Clock Fall Time	TFRC	2.0V to 0.8V; CL ≤ 15 pF			5	ns
Read Reference Clock Pulse Width	TWRC	To = Read Reference Clock Period	0.5•To-10		0.5•To+10	ns
Read Data Pulse Width	TSRD	To = Read Reference Clock Period	To -5		To+5	ns
Read Data Rise Time	TRSRD	0.8V to 2.0V ; CL ≤ 15 pF			10	ns
Read Data Fall Time	TFSRD	2.0V to 0.8V ; CL ≤ 15 pF			8	ns
SRD Output Setup wrt RRC Rise	TSSRD		15			ns
SRD Output Hold wrt RRC Rise	THSRD		15			ns
$\overline{RDI}$ Pulse Width	TRDI	To = Read Reference Clock Period	15		To	ns

DATA SYNCHRONIZATION

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
VCO Center Frequency Period	TVCO	V@FLTR = 2.7V, VPA2 = 5.0V Serial Reg 0 = X000 T1= 83 ns Serial Reg 0 = X001 T1 = 111 ns Serial Reg 0 = X010 T1 = 167 ns Serial Reg 0 = Other T1 = 125 ns	0.8 T1	T1	1.2 T1	ns
VCO Frequency Dynamic Range	VDR	1.0V ≤ V @ FLTR ≤ VPA2 - 0.6V VPA2 = 5V	±24	±34	±45	%
VCO Control Gain	KVCO	V @ FLTR = 2.7V; ωo = 2π/TVCO	0.14 ωo	0.20 ωo	0.26 ωo	rad/s-V
Phase Detector Gain	KD	KD = 0.62/(RR + 527) VPA2 = 5V (RR = 7.5 kΩ)	0.83 KD	KD	1.17 KD	A/rad
FL1-4 High Impedance	FLZH		2			kΩ
FL1-4 Low Impedance	FLZL				100	Ω
KVCO x KD Product Accuracy	KPA		-28	0	28	%
VCO Phase Restart Error	PRE			4		ns
Decode Window	DW	To = Read Refrence Clock Period	To - 2	To		ns
Decode Window Center Accuracy	DWCA		-5% To		+5% To	ns
Decode Window Shift Magnitude	TS1	Serial Register 1 = 1X00		±10% To		ns
	TS2	Serial Register 1 = 1X01		±7.5% To		ns
	TS3	Serial Register 1 = 1X10		±5% To		ns

MISCELLANEOUS TIMING

RG, WG Time Delay	RWTD				100	ns

SERIAL PORT SECTION

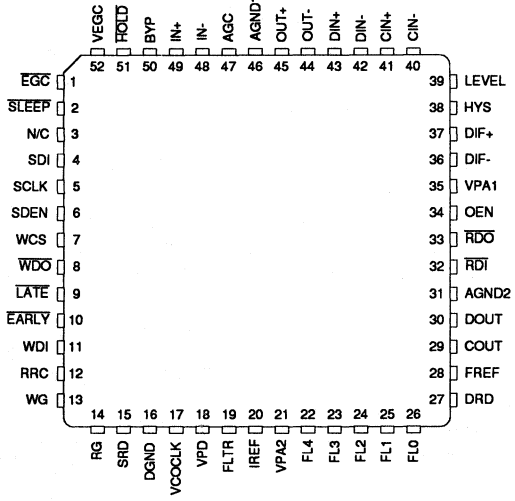
SCLK Period	TC		100			ns
SDEN Setup to SCLK	T1		10		TC/2 -10	ns
SDEN Hold after SCLK	T2A		10		TC -10	ns
SDEN Falls prior to SCLK rises	T2B		25			ns
SDI Setup to SCLK	T3		25			ns
SDI Hold after SCLK	T4		25			ns

SSI 34P3200
Pulse Detector & Data Synchronizer for High Density Floppy Storage

PACKAGE PIN DESIGNATIONS
(Top View)

THERMAL CHARACTERISTICS: θja

52-lead QFP	75°C/W



52-Lead QFP

CAUTION: Use handling procedures necessary for a static sensitive component.

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 34P3200 - 52-lead QFP	34P3200-CG	34P3200-CG

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

Silicon Systems, Inc. 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914

silicon systems®
A TDK Group Company

SSI 34P3201

Pulse Detector & Data Synchronizer, 250K to 8.0 Mbit/s

Preliminary Data

December 1993

DESCRIPTION

The SSI 34P3201 is a high performance pulse detector and data synchronizer integrated circuit. This device is designed for use in high density floppy storage applications. The pulse detection portion of this device detects and validates amplitude peaks output from a disk drive read amplifier. The data synchronization portion is a 1,7 RLL or MFM data synchronizer with window shift. The SSI 34P3201 supports a Sleep mode for minimal power dissipation in non-operational periods.

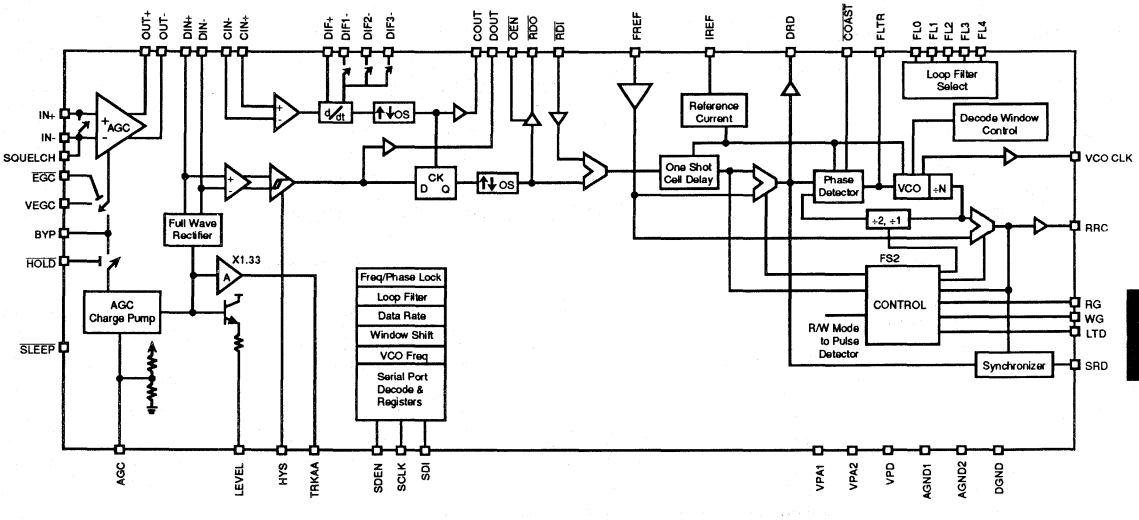
The SSI 34P3201 features a 3-pin serial port for easy selection of data rate and operating configurations.

The SSI 34P3201 is available in a 52-lead QFP package.

FEATURES

- **Highly Integrated Pulse Detector & Data Synchronizer**
- **Ideal for High Density Floppy Storage Applications**
- **Operating Data Rate: 250K to 8.0M NRZ bits per second selectable through the serial port**
- **Supports 1,7 RLL, MFM, FM, and GCR Encoding Format**
- **3-Pin Serial Port Programming: Data Rate Selection, Window Shift & Test Mode**
- **Fast Acquisition Phase Lock Loop & Zero Phase Restart Technique**
- **5V Operation only**
- **Low Operating Power**
- **Sleep Mode**

BLOCK DIAGRAM



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FUNCTIONAL DESCRIPTION

The SSI 34P3201 is a pulse detector and data synchronizer circuit. Its two main functions are:

- Validate and time-position preserve the analog pulses (IN±) from a read-write preamplifier.
- Extract the encoded data bit and its corresponding clock signal.

The SSI 34P3201 major functional blocks are:

- AGC amplifier & AGC control
- Pulse qualifier
- Data synchronizer
- Window shift
- Serial port decode & registers

AGC AMPLIFIER & AGC CONTROL

The AGC amplifier is to provide signal amplification prior to pulse qualification. The amplifier gain is a linear function of a gain control voltage, Figure 1. The gain control voltage is either the BYP voltage when $\overline{EGC}$ = logic high, or the VEGC voltage when $\overline{EGC}$ = logic low.

In the normal Read mode, i.e., with the AGC active, the DIN± input signal is regulated to a nominal level which is set by the voltage at the AGC pin. With the AGC pin open, the nominal DIN± level is 1 Vppd (peak-to-peak differential). This nominal DIN± level can be adjusted with an external resistor tied from the AGC pin to either VPA1 or AGND1, as shown in Figure 2. The DIN± voltage level is nominally 1.0 Vppd/V x V_{AGC}.

The AGC actions are current charging and discharging the external BYP integrating capacitor. They are described as follows:

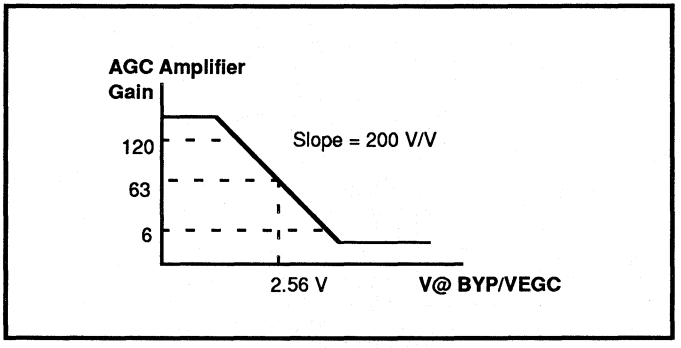

FIGURE 1: AGC Amplifier Gain vs. BYP/VEGC Voltage

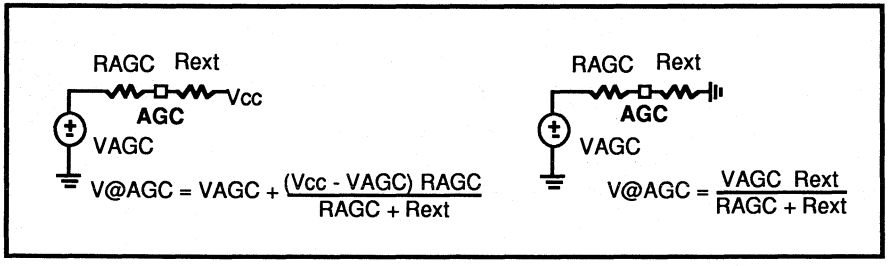

FIGURE 2: AGC Loop Reference Adjustment

Slow Decay 1 (R4, bit 0 = 0)

When the instantaneous DIN± signal is below the nominal level, a slow decay current, 4.5 µA, discharges the BYP capacitor. The AGC amplifier gain is increased slowly.

Slow Decay 2 (R4, bit 0 = 1)

When the instantaneous DIN± signal is below the nominal level, a slow decay current, 0.1 mA, discharges the BYP capacitor. The AGC amplifier gain is increased.

Slow Attack

When the instantaneous DIN± signal exceeds the nominal level but is below 125% of the nominal level, a slow attack current, 0.18 mA, charges the BYP capacitor. The AGC amplifier gain is decreased.

Fast Attack

When the instantaneous DIN± signal exceeds 125% of the nominal level, the device enters a Fast Attack mode. A fast attack current, 1.3 mA, charges the BYP capacitor. The AGC amplifier gain is quickly lowered.

Write-to-Read Recovery

With a logic high to logic low transition of the WG, the SSI 34P3201 enters the Write-to-Read Recovery mode except while SQUELCH is set to high. The input impedance remains in the low impedance state for 0.9 µs for fast input DC coupling recovery. The device then restores to high input impedance state, and enters into a Fast Decay mode for 0.9 µs. In the Fast Decay mode, a continuous 0.1 mA current discharges the BYP capacitor. The AGC amplifier gain is increased very quickly. This additional Fast Decay mode current is disabled when the Slow Decay 2 mode is active. Figure 3 shows the nominal write-to-read AGC action timing.

The AGC input impedance is also controlled by the SQUELCH pin. When SQUELCH is asserted high, the AGC input impedance becomes low impedance.

The above AGC actions, except that of write-to-read recovery, can be suspended with the $\overline{\text{HOLD}}$ = logic low. The AGC amplifier gain is then held constant, except for leakage effect.

With $\overline{\text{EGC}}$ = logic low, the AGC amplifier gain is determined by the VEGC voltage. With a fixed external DC voltage, or a second AGC control loop at the VEGC pin, the AGC amplifier gain is set independent of the on-chip AGC control loop, such as when read signal is over a servo demodulation field.

The AGC amplifier outputs are emitter follower outputs.

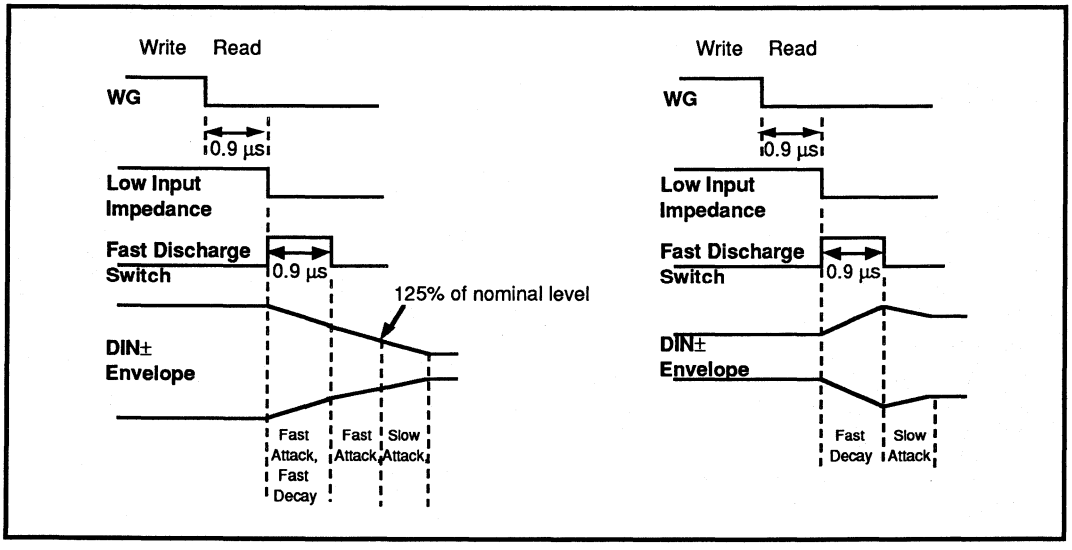

FIGURE 3: AGC Action Timing in Write-to-Read Recovery

FUNCTIONAL DESCRIPTION (continued)

PULSE QUALIFIER

The pulse qualifier validates each DIN± peak by a combination of level qualification and time qualification. In level qualification, a hysteresis comparator eliminates errors due to low level additive noise. In time qualification, the AGC amplifier output is time differentiated to locate the signal peaks in time.

Level Qualification

The level qualification is accomplished by comparing the DIN± signal with a set threshold. The SSI 34P3201 allows two ways of setting the thresholds: fixed threshold or DIN± tracking threshold. Fixed threshold can be simply set by a DC voltage at the HYS pin, such as a resistor from VPA1 to ground. The threshold at the comparator can be computed as: Hysteresis Gain x V@HYS. For high performance system application, however, DIN± tracking threshold is recommended.

DIN± tracking threshold has the advantage of shorter write-to-read recovery time and lower probability of error with input amplitude drop out. The threshold is designed as a percentage of the DIN± peak voltage. This technique can be implemented by feeding the LEVEL output, through a resistor divider, to the HYS pin. The LEVEL output, amplified peak capture of DIN± signal, can be computed as: Level Gain x DIN±ppd. With the resistor divider, a fraction of the LEVEL output is presented at the HYS pin. The threshold, as a function of DIN±, can be summarized as: Level Gain x Resistor Dividing Ratio x Hysteresis Gain x DIN±ppd. For a typical case of 1 Vppd DIN± signal, assume equal value resistors in the divider network, the threshold is 1 x 0.5 x 0.38 x 1 = 0.19V. This represents 38% threshold on a 1 Vppd signal. While both the Level Gain and the Hysteresis Gain bear a moderate tolerance due to typical process variation, they inversely track each other to yield a much tighter threshold accuracy in a closed loop.

While the external resistor divider ratio determines the qualification setting, the total resistance and the peak capture capacitor should be optimized for the system data rate. The RC time constant must be small enough to allow good response to changing DIN± peak, but large enough to provide a constant threshold after a long duration of input absence.

Time Qualification

Time qualification is used to locate DIN± peaks. With time differentiation, each DIN± peak is translated into a zero crossing, which clocks an on-chip flip-flop in the pulse qualifier. The SSI 34P3201 supports on-chip or off-chip differentiation.

ON-CHIP DIFFERENTIATION

The on-chip differentiation is accomplished by connecting an external RLC network across the DIF± pins. The DIF1-, DIF2-, and DIF3- pins are provided for wide code rate variation. These differentiators are selected by Register 4, bits 1 and 2. The DIN+ and CIN+ pins should be tied together, as well as the DIN- and CIN- pins.

OFF-CHIP DIFFERENTIATION

For constant density recording applications, a differentiation function with a low pass cut-off frequency tracking data rate can maximize the signal-to-noise ratio performance. A time differentiated input can be applied at the CIN± pins, separated from the DIN± pins. A 1.2 kΩ resistor should be placed across the DIF± pins.

This function can best be supported by the Silicon Systems programmable filters, such as the SSI 32F8030 and the SSI 32F8130/8131. The filters feature both a normal low pass output and a differentiated low pass output. The low pass cut-off frequency is programmable by the user to track the data rate. The signal delays of the two signal paths are well matched.

Qualified Read Data

Upon level and time qualification, a one-shot data pulse is generated for every validated peak of the DIN± signal. This read data pulse can be monitored at the $\overline{\text{RDO}}$ pin, when $\overline{\text{OEN}}$ = logic low. In high speed normal Read mode, it is recommended that the $\overline{\text{RDO}}$ output be disabled for lower noise performance with $\overline{\text{OEN}}$ = logic high. The pulse detector read data can be used as input to the data synchronizer. Alternately, external input at the $\overline{\text{RDI}}$ pin can be used as input to the data synchronizer.

Figure 4 summarizes the pulse detector function.

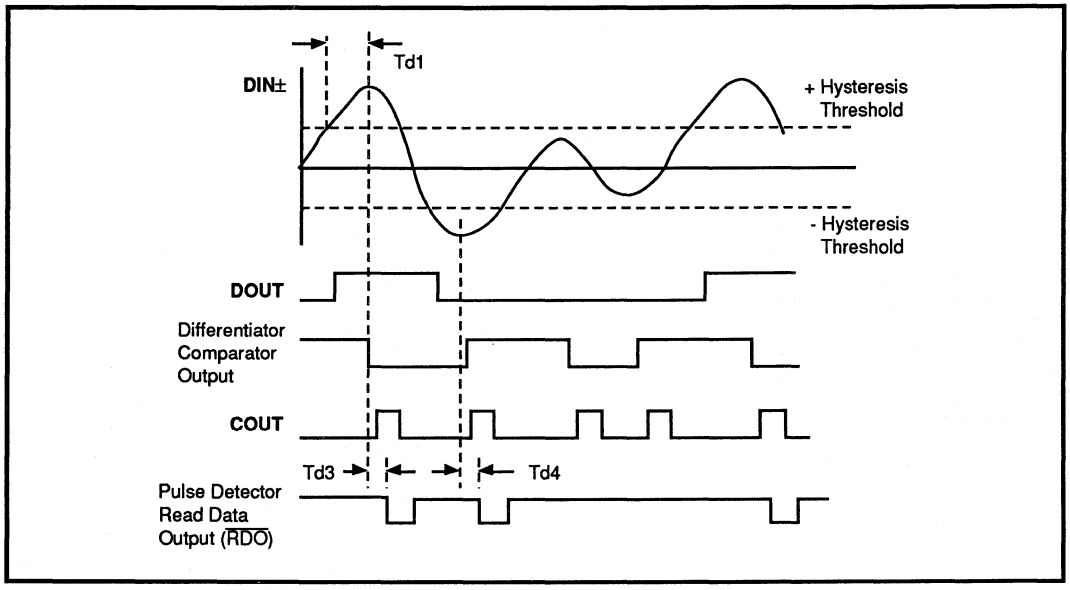

FIGURE 4: Read Mode Pulse Detector Timing Diagram

DATA SYNCHRONIZER

The data synchronizer is used to extract the clock and the encoded data signals from the read data signal. The input source to the data synchronizer can be from the pulse qualifier or from an external source via the $\overline{RDI}$ pin.

The SSI 34P3201 is designed to perform data synchronization for operating data rates of 250K to 8.0M NRZ bits per second. Data rates are selected through a combination of serial port register R0 for ÷N and serial port register R2 for VCO center frequency. The following is a partial list of possible data rates:

NRZ Data Rate	Encoding Format	VCO Freq	÷N	Code Clk (MHz)
8 Mbit/s	1,7 RLL	12	1	12.0
6 Mbit/s	MFM	12	1	12.0
4 Mbit/s	1,7 RLL	12	2	6.0
3.429 Mbit/s	1,7 RLL	10.286	2	5.143
3.2 Mbit/s	1,7 RLL	9.6	2	4.8
3.0 Mbit/s	1,7 RLL	9.0	2	4.5
2.667 Mbit/s	1,7 RLL	8.0	2	4.0
2.4 Mbit/s	MFM	9.6	2	4.8
1.6 Mbit/s	1,7 RLL	9.6	4	2.4
1.2 Mbit/s	MFM	9.6	4	2.4
1.0 Mbit/s	MFM	8.0	4	2.0
600 Kbit/s	MFM	9.6	8	1.2
500 Kbit/s	FM	8.0	8	1.0

DATA SYNCHRONIZER (continued)

For the 1,7 RLL format, the encoded bit rate, as well as the data synchronizer clock, is at 1.5 times the NRZ data rate. For the MFM encoding format, the encoded bit rate, as well as the data synchronizer clock, is at twice the NRZ data rate. Thus, the required data synchronizer clock rate is from 0.5 to 12 MHz.

To accommodate the wide data rate dynamic range, the SSI 34P3201 employs a novel data synchronizer phase locked loop (PLL) architecture (see Block Diagram). While the voltage controlled oscillator (VCO) operates only between 6 MHz to 12 MHz, a divide-down function is used to generate the lower frequency clocks.

With the serial register R0 programmed for a specific divide-down factor and serial register R2 programmed for a specific VCO center frequency, the SSI 34P3201 would decode the proper NRZ data rate. The 1/2 code cell delay duration is also set properly for each operating mode.

When the SSI 34P3201 is in the Idle mode, the VCO should lock to an external reference clock, FREF, which needs to be the same frequency as the VCO divided by N for proper operation.

The SSI34P3201 employs a dual mode phase detector: Phase Lock mode and Frequency Lock mode. In the Read mode, the mode of the phase detector is programmable. With Fast Sync = logic low, the phase detector operates in the Phase Lock mode whereby the phase detector updates the PLL with each occurrence of a read data pulse from the pulse qualifier. With Fast Sync = logic high, the phase detector operates in the Frequency Lock mode. In the Write and Idle modes, the Frequency Lock mode phase detector is continuously enabled, thus maintaining both phase and frequency lock. Figure 5 shows the phase detector transfer function. By acquiring both phase and frequency lock to the FREF and utilizing a zero phase restart technique, false lock to the pulse detector read data is eliminated.

The phase detector incorporates a charge pump in order to drive the loop filter directly. The polarity and width of the output current pulses correspond to the direction and magnitude of the phase error. The charge pump gain during the PLL acquisition phase in the preamble area is controlled by LTD as shown in Figure 6. The selection of Frequency Lock mode (Fast sync 2: FS2) or Phase Lock mode (Fast sync 1: FS1) during preamble area is controlled through the serial port. The phase detector and charge pump output (high Z) are disabled when $\overline{\text{COAST}}$ is low.

Because of the wide data rate dynamic range, the SSI 34P3201 provides five high impedance/low impedance switchable nodes, FL0-4, for external loop filter component switching. The impedance of these FL0-4 nodes are controlled by register 2 bit 0 and register 3 bit 0-3. When the node is in high impedance state, the external component connected to this node is switched out. When the node is in low impedance state, the external component is included in the loop filter network.

The various operating modes of the data synchronizer are discussed in the Operation Modes section.

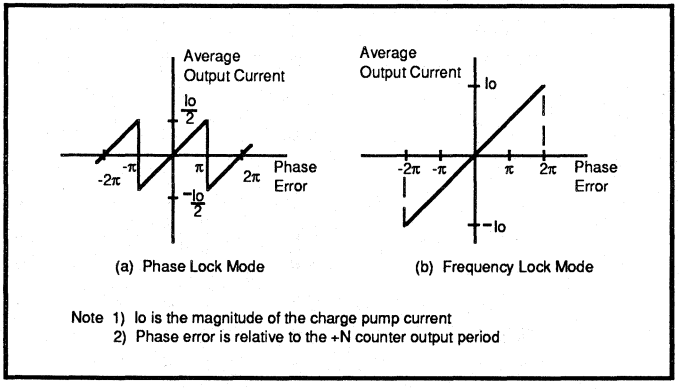

FIGURE 5: Phase Detector Transfer Function

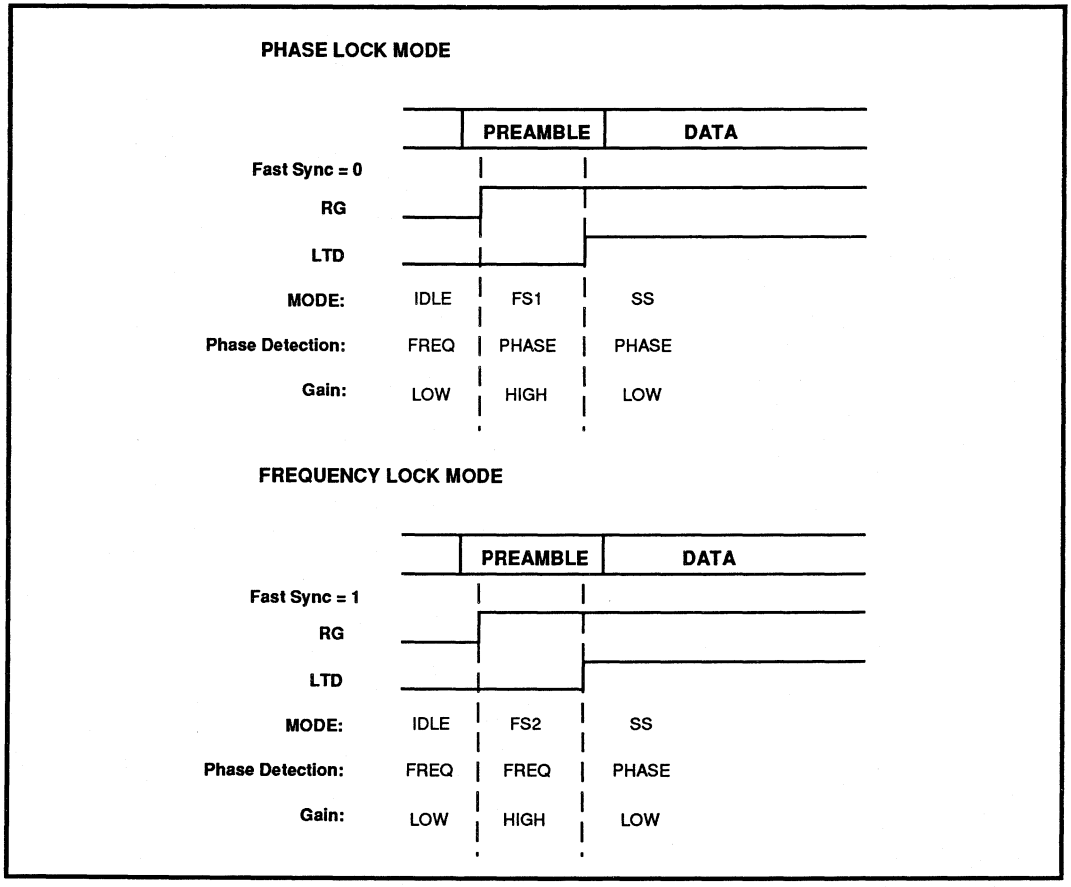

FIGURE 6: PLL Acquisition Mode During Preamble

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FUNCTIONAL DESCRIPTION (continued)

WINDOW SHIFT

To enhance the data decode function, the SSI 34P3201 supports a window shift function for code rates 3 Mbit/s and above. Shifting the pulse width of the ½ code cell delay output shifts the relative position of the DLYD DATA pulse within the decode window. This powerful capability, supported through serial register R1, easily facilitates defect mappings, automatic calibration, window margin testing, error recovery, and systematic error cancellation.

The window shift can be set to ±20%, ±30% or ±40% of the decode half window. Figure 7 defines the direction of the window shift. Refer to the Serial Port Decode & Registers section for serial port register assignment.

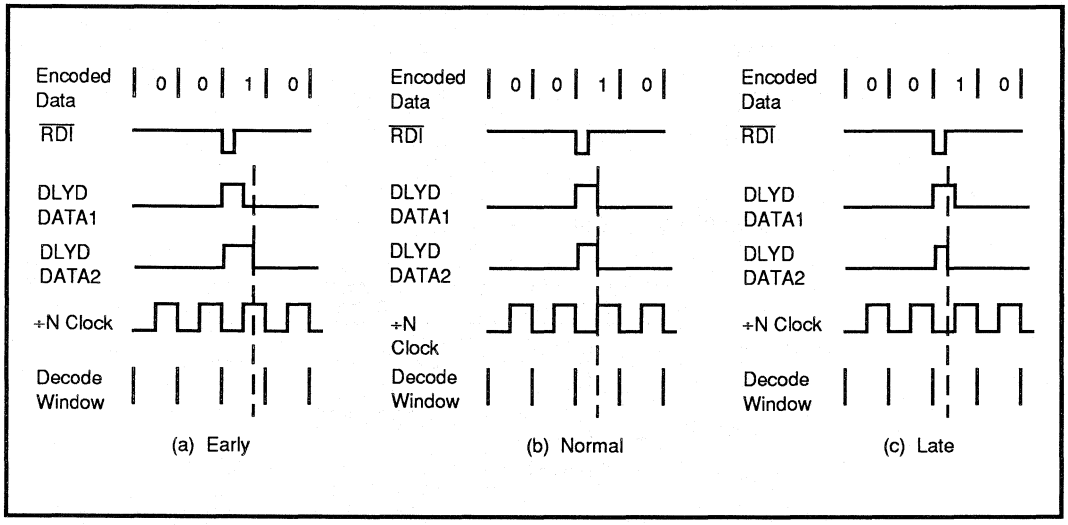

FIGURE 7: Decode Window & Window Shift Directions

SERIAL PORT DECODE & REGISTERS

The SSI 34P3201 provides a 3-pin serial port to facilitate the following digital controls:

- Phase/Frequency Lock mode (Register 0: Bit 3)
- N value (Register 0: Bits 2-0)
- Window shift (Register 1: Bits 3-0)
- VCO center frequency (Register 2: Bits 3-1)
- FL0-4 switch control (Register 2: Bit 0, Register 3: Bits 3-0)
- Data sychronizer input source (Register 4: Bit 3)
- DIF (Register 4: Bits 2 - 1)
- ISD (Register 4: Bit 0)

The 3 serial port pins are SDEN, SDI and SCLK. Figure 8 shows a timing diagram of the serial data transmission. Each data transmission consists of an 8-bit packet, Bit 7 being the most significant bit (MSB). The 8-bit packet is divided into two fields: Bit 7-4 address field, Bit 3-0 data field. All register bits are reset to 0 at power-up.

The register assignment is as follows:

Register 0 Address 0000

Bit 3 Fast Sync register

0 : Phase Lock mode (FS1)

1 : Freq Lock mode (FS2)

Bits 2, 1, 0 N register

0 0 0 : N = 1

0 0 1 : 2

0 1 0 : 4

0 1 1 : 8

1 X X : 16

Register 1 Address 0001 Window Shift

Bit 3

0 : Disable

1 : Enable

Bit 2

0 : Direction Early

1 : Direction Late

Bit 1, 0 Window shift magnitude

0 0 : 40% of half window

0 1 : 30% of half window

1 0 : 20% of half window

1 1 : 0% of half window

Register 2 Address 0010

Bits 3, 2, 1 VCO register

0 0 0 VCO center frequency = 6 MHz

0 0 1 VCO center frequency = 7 MHz

0 1 0 VCO center frequency = 8 MHz

0 1 1 VCO center frequency = 9 MHz

1 0 0 VCO center frequency = 10 MHz

1 0 1 VCO center frequency = 11 MHz

1 1 0 VCO center frequency = 12 MHz

1 1 1 VCO center frequency = 13 MHz

Bit 0 MSB of FL register

Register 3 Address 0011 FL0-4 Switch Control

Register 2 Register 3

Bit 0 Bits 3, 2, 1, 0

0 0 0 0 0 All off (All Hi Z)

x x x x 1 FL0 on (FL0 : Low Z)

x x x 1 x FL1 on (FL1 : Low Z)

x x 1 x x FL2 on (FL2 : Low Z)

x 1 x x x FL3 on (FL3 : Low Z)

1 x x x x FL4 on (FL4 : Low Z)

Register 4 Address 0100 DIF and ISD Register

Bit 3 Data synchronizer input source

0 : From interanl pulse qualification output

1 : From the $\overline{RDI}$ pin

Bit 2, 1 DIF Register

0 0 : DIF1-

0 1 : DIF2-

1 0 : DIF3-

1 1 : Unused

Bit 0 ISD Register

0 : Slow Decay 1

1 : Slow Decay 2

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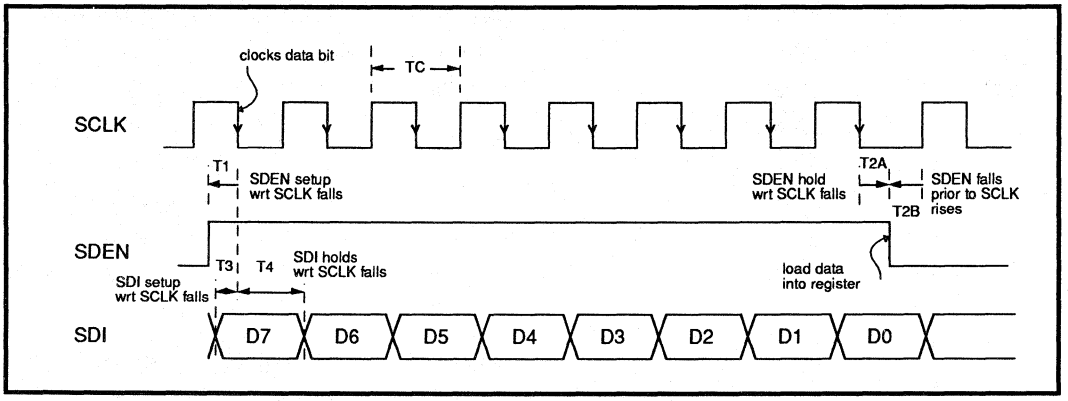

FIGURE 8: Serial Port Timing Diagram

OPERATION MODES

The SSI 34P3201 can support the following operating modes:

Mode	WG	RG	$\overline{\text{HOLD}}$	$\overline{\text{EGC}}$	$\overline{\text{SLEEP}}$	LTD
Idle VCO locked to FREF AGC active Frequency lock phase detection I charge pump X1 (KD2)	0	0	1	1	1	X
Idle VCO locked to FREF AGC gain held constant by BYP Frequency lock phase detection I charge pump X1 (KD2)	0	0	0	1	1	X
Idle VCO locked to FREF AGC gain held constant by VEGC Frequency lock phase detection I charge pump X1 (KD2)	0	0	X	0	1	X
Read VCO locked to Pulse Qualifier DLYD DATA AGC active Phase lock phase detection I charge pump X1 (KD2)	0	1	1	1	1	1

Mode	WG	RG	$\overline{\text{HOLD}}$	$\overline{\text{EGC}}$	$\overline{\text{SLEEP}}$	LTD
Read VCO locked to Pulse Qualifier DLYD DATA AGC gain held constant by BYP Phase lock phase detection I charge pump X1 (KD2)	0	1	0	1	1	1
Read VCO locked to Pulse Qualifier DLYD DATA AGC gain held constant by VEGC Phase lock phase detection I charge pump X1 (KD2)	0	1	X	0	1	1
Write AGC gain held constant by BYP Input impedance lowered VCO locked to FREF	1	X	X	1	1	X
Write AGC gain held constant by VEGC Input impedance lowered VCO locked to FREF	1	X	X	0	1	X
FS1 Serial port register 0, bit 3 = 0 VCO locked to preamble Phase lock phase detection I charge pump X3 (KD1)	0	1	X	X	1	0
FS2 Serial port register 0, bit 3 = 1 VCO locked to preamble Frequency lock phase detection I charge pump X3 (KD1)	0	1	X	X	1	0
Power Shutdown	X	X	X	X	0	X

OPERATION MODES (continued)

READ MODE

In the Read mode, the rising edge of DLYD DATA enables the phase detector while the falling edge is phase compared to the rising edge of the ÷N counter. As depicted in Figure 9, DLYD DATA is ½ code cell wide (TVCO / 2 / N) pulse whose leading edge is defined by the leading edge of Read Data. RRC is generated from the rising edge of the ÷N counter output. The accuracy of the ½ code cell delay only affects the retrace angle of the phase detector and does not influence the accuracy of RRC.

In the Non-Read modes, the PLL is locked to FREF. This forces the VCO to run at a frequency which is very close to that required for tracking actual data and thus minimizes the associated frequency step during acquisition. When RG transitions, the VCO is stopped momentarily, then restarted in an accurate phase alignment with the next PLL reference input pulse. By minimizing the phase alignment in this manner (phase error ≤ 0.5 rads), the acquisition time is substantially reduced.

With the PLL in lock, the encoded data bit is re-synchronized before output to the SRD pin. Figure 10 shows the Read mode timing.

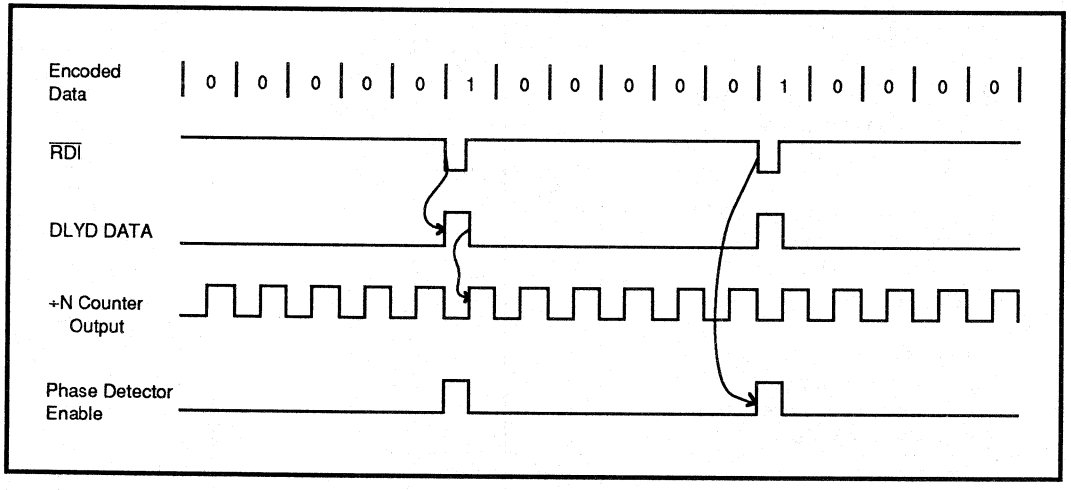

FIGURE 9: Data Synchronizer Timing

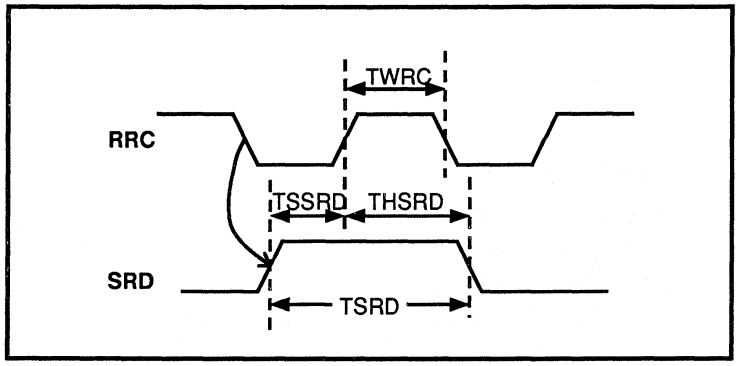

FIGURE 10: Read Mode Timing

WRITE MODE

In the Write mode, the SSI 34P3201 pulse detector is disabled and preset for the subsequent Read mode. The digital circuitry is disabled, the input AGC amplifier gain is held at its previous value and the AGC amplifier input impedance is reduced.

Holding the AGC amplifier gain and reducing input impedance shortens system write-to-read recovery times.

The lowered input impedance improves settling time by reducing the time constant of the network between the SSI 34P3201 and a head preamplifier such as the SSI 34R1203R. Write-to-read timing is controlled to maintain the reduced impedance for 0.9 µs before the AGC circuitry is activated. Coupling capacitors should be chosen with as low a value as possible consistent with adequate bandwidth to allow more rapid settling.

POWER SHUTDOWN

For reduced power dissipation during non-operational periods, the SSI 34P3201 can be switched into a Sleep mode. The serial port registers will remain powered up during Sleep mode. Therefore no reprogramming is required following a logic low to logic high $\overline{\text{SLEEP}}$ transition.

PIN DESCRIPTION

ANALOG INPUT PINS

NAME	TYPE	DESCRIPTION
IN+, IN-	I	AGC amplifier inputs.
DIN+, DIN-	I	Data inputs to hysteresis comparator and full-wave rectifier.
CIN+, CIN-	I	Data inputs to time-channel qualification.
HYS	I	Hysteresis input to establish the hysteresis threshold of the data comparator.
AGC	I	The voltage at the AGC pin determines the nominal level at the DIN± pins.
BYP	I	The voltage at the BYP pin controls the AGC amplifier gain when $\overline{EGC}$ = logic high.
VEGC	I	The voltage at the VEGC pin controls the AGC amplifier gain when $\overline{EGC}$ = logic low.

DIGITAL INPUT PINS

FREF	I	TTL reference clock input to data synchronizer.
$\overline{OEN}$	I	TTL $\overline{RDO}$ Output Enable input: $\overline{RDO}$ enabled with $\overline{OEN}$ = logic low, $\overline{RDO}$ forced to high with $\overline{OEN}$ = logic high.
$\overline{RDI}$	I	TTL external input source to the data synchronizer.
RG	I	TTL Read Gate input.
WG	I	TTL Write Gate input. Enables Write mode.
LTD	I	TTL Lock to Data asynchronous input.
$\overline{SLEEP}$	I	TTL power shutdown control. The device is in Power Shutdown mode when $\overline{SLEEP}$ = logic low. The device is in normal operational state when $\overline{SLEEP}$ = logic high, or left open.
$\overline{HOLD}$	I	TTL input that holds the AGC gain constant when pulled low. When left open, this input is at logic high.
$\overline{EGC}$	I	TTL input. When $\overline{EGC}$ = logic low, the AGC amplifier gain is controlled by the voltage at VEGC. When $\overline{EGC}$ = logic high, or left open, the AGC amplifier gain is controlled by the voltage at BYP.
SQUELCH	I	TTL input. The AGC input impedance is reduced when SQUELCH = logic high. When SQUELCH = logic low, the AGC input impedance is normal.
$\overline{COAST}$	I	TTL input. When $\overline{COAST}$ = logic low, the phase detector and charge pump output are disabled (high Z).
SDI	I	TTL Serial Data Input.
SCLK	I	TTL Serial Clock. Negative edge triggered clock input for serial register.
SDEN	I	TTL Serial Data Enable. A high level enables data loading. The data is latched on the falling edge of SDEN.

ANALOG OUTPUT PINS

NAME	TYPE	DESCRIPTION
OUT+, OUT-	O	AGC amplifier emitter follower output pins.
LEVEL	O	Open emitter output from fullwave rectifier that may be used for input to the HYS pin.
TRKAA	O	Open emitter output from fullwave rectifier with an additional gain of 1.333 over LEVEL.
FL0-4	O	Loop filter connection pins. Either high impedance or low impedance state.

ANALOG CONTROL PINS

DIF+, DIF1-, DIF2-, DIF3-	O	Pins for external differentiating network. When off-chip differentiator is used, a 1.2 kΩ resistor should be tied across DIF+ and DIFX-.
IREF	O	Input reference current for VCO bias. A 7.5 kΩ resistor should be tied between IREF and VPA2.
FLTR	O	Loop filter pin.

DIGITAL OUTPUT PINS

$\overline{RDO}$	O	TTL output of the pulse detector read data. This output is enabled with $\overline{OEN}$ = logic low. It is forced high with $\overline{OEN}$ = logic high.
RRC	O	Read Reference Clock: a multiplexed TTL clock source used by the controller. In the Read mode, this clock is the encoded bit rate. In the Write mode, it is FREF. No short clock pulses are generated during a mode change.
SRD	O	Synchronized Read Data: a TTL read data that has been re-synchronized to read clock.
COUT	O	Time qualification one-shot test point: open emitter output which requires an external 1 kΩ pull down resistor when used.
DOUT	O	Data comparator test point: open emitter output which requires an external 1 kΩ pull down resistor when used.
DRD	O	Delay Read Data test point: open emitter output which requires an external 5 kΩ pull down resistor when used.
VCO CLK	O	VCO test point: open emitter output which requires an external 5 kΩ pull down resistor when used.

POWER & GROUND

VPA1	-	Analog supply to the pulse detector section.
VPA2	-	Analog supply to the data synchronizer section.
VPD	-	Digital supply.
AGND1	-	Analog ground to the pulse detector section.
AGND2	-	Analog ground to the data synchronizer section.
DGND	-	Digital ground.

ELECTRICAL SPECIFICATIONS

Unless otherwise specified, the recommended operating conditions apply.

ABSOLUTE MAXIMUM RATINGS

Operation beyond the maximum ratings may damage the device.

PARAMETER	RATING
Storage Temperature	-65 to +150°C
Junction Operating Temperature	+130°C
Supply Voltage, VPA1-2, VPD	-0.7 to +7V
Voltage Applied to Inputs	-0.3 to Supply + 0.3V

RECOMMENDED OPERATING CONDITIONS

PARAMETER	RATING
Supply voltage	4.5V < VPA1, VPA2, VPD < 5.5V
Ambient Temperature, Ta	0°C < Ta < 70°C

POWER SUPPLY

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Power Dissipation Active	PD	Outputs unloaded 4.5V < VPA1, VPA2, VPD < 5.5V		450	650	mW
Power Down Dissipation	PDS	Output unloaded; $\overline{\text{SLEEP}}$ = logic low		50	70	mW

LOGIC SIGNALS

TTL Input Low Voltage	VIL		-0.3		0.8	V
TTL Input High Voltage	VIH		2		VCC+0.3	V
TTL Input Low Current	IIL	VIL = 0.4V	-0.4			mA
TTL Input High Current	IIH	VIH = 2.7V			0.1	mA
TTL Input Switching Time	TS	0.8V - 2.0V transition			0.1	µs
TTL Output Low Voltage	VOL	IOL = 4.0 mA			0.5	V
TTL Output High Voltage	VOH	IOH = -400 µA	2.7			V
Test Point Output High Voltage (DOUT, COUT)	VOHT1	1 kΩ to DGND		VPA - 2.4		V
Test Point Output Low Voltage (DOUT, COUT)	VOLT1	1 kΩ to DGND		VPA - 2.8		V
Test Point Output High Voltage (VCOCLK, DRD)	VOHT2	5 kΩ to DGND		4.2		V
Test Point Output High Voltage (VCOCLK, DRD)	VOLT2	5 kΩ to DGND		3.6		V

MODE CONTROL

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Read-to-Write Transition TDRW	WG pin logic low to logic high			1	µs
Write-to-Read Transition TDWR	WG pin logic high to logic low; AGC settling not included	0.5	0.9	1.3	µs
$\overline{\text{HOLD}}$ On to Off/Off to On Transition TDH	$\overline{\text{HOLD}}$ pin, high to/from low transition			1	µs
Power Shutdown mode to Read/Write Delay TDSL	Settling time of external capacitor not included		0.1		µs
Read/Write Mode to power shutdown Delay TDOFF			10		µs
Low Input Impedance Pulse Width PWIMS	WG pin logic high to logic low Not directly testable		0.9		µs
Fast Discharge Pulse Width PWFDC	WG pin logic high to logic low following PWIMS. Not directly testable		0.9		µs

AGC AMPLIFIER

Unless otherwise specified, recommended operating conditions apply. Input signals, 100 mVppd at 1.0 MHz, are AC coupled to IN±. OUT± are AC coupled to DIN±.

A 2000 pF capacitor is connected between BYP and AGND1. AGC pin is open.

Minimum Gain Range MIGR	1.0 Vppd ≤ OUT± ≤ 3.0 Vppd			6	V/V
Maximum Gain Range MAGR	1.0 Vppd ≤ OUT± ≤ 3.0 Vppd	120			V/V
AGC Input Range IN±	6 ≤ gain ≤ 120, OUT± = 1 Vpp	8.33		166.7	mVpp
	6 ≤ gain ≤ 120, OUT± = 2 Vpp	16.66		333.33	mVpp
Output Offset Voltage Variation VOS	Over entire gain range	-400	0	400	mV
Maximum Output Voltage Swing VOMX	Set by AGC pin	3			Vppd
Differential Input Impedance RIN	IN± = 100 mVppd SQUELCH = logic low, WG = logic low		5		kΩ
	IN± = 100 mVppd SQUELCH = logic high or WG = logic high		100	150	Ω
Differential Input Capacitance CIN	IN± = 100 mVppd @ 1.0 MHz			10	pF
Single Ended Input Impedance ZCMH	SQUELCH = logic low, WG = logic low, IN+ = IN-		1.5		kΩ
	SQUELCH = logic high or WG = logic high, IN+ = IN-			250	Ω

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AGC AMPLIFIER (continued)

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Input Noise Voltage	VIN	Gain set to maximum, BW = 4.5 MHz, short IN+ to IN-			40	nV/√Hz
Bandwidth	BW	Gain set to maximum referenced to 1.0 MHz	15			MHz
Single Ended Output Impedance on OUT±	ROUT		25	40	55	Ω
OUT± Pin Current	IOUT		±3.0			mA
Input Referred Common Mode Rejection	CMRR	IN+ = IN- = 100 mVpp @ 1.0 MHz; gain set to maximum	40			dB
Input Referred Power Supply Rejection Ratio	PSRR	1.0 Vpp @ 1.0 MHz on VPA1; gain set to maximum	83			dB
Power Supply Rejection	PSR	1.0 Vpp injected power supply signal; gain set to maximum	45			dB
DIN± Input Swing vs AGC Input	KAGC	16.67 mVppd ≤ IN± ≤166.7 mVppd; $\overline{HOLD}$ = logic high 0.5 Vppd ≤ DIN± ≤ 1.5 Vppd	0.7	1	1.3	Vppd/V
DIN± Input Swing Variation with IN±	ΔDIN	8.33 mVppd ≤IN±≤166.7 mVppd	-6		6	%
AGC Open Voltage	VAGC	AGC open	0.8	1	1.2	V
AGC Pin Input Impedance	RAGC		2.5	3.8	6.0	kΩ
VEGC Input Impedance	ZVEGC	$\overline{EGC}$ = logic low	30			MΩ
Slow AGC Discharge Current (Slow Decay 1 Mode)	ISD	DIN± = 0V	3	4.5	6	µA
Slow AGC Discharge Current (Slow Decay 2 Mode)	ISD	DIN± = 0V	0.07	0.1	0.13	mA
Fast AGC Discharge Current	IFD	Starts at 0.9 µs after WG high to low transition Stops at 1.8 µs after WG high to low transition Slow Decay 1 mode	0.07	0.1	0.13	mA
AGC Leakage Current	ILK	$\overline{HOLD}$ = logic low	-50	0	50	nA
Slow AGC Charge Current	ISC	DIN± = 0.8 VDC Vary AGC until slow charge begins	-0.12	-0.18	-0.24	mA
Fast AGC Charge Current	IFC	DIN± = 0.8 VDC Vary AGC until fast charge begins	-0.9	-1.3	-1.7	mA

AGC AMPLIFIER (continued)

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
Fast to Slow Attack Switchover Point	FSSP	DIN±(fast) / DIN±(slow)		125		%
Gain Decay Time	TGD1	IN± = 250 mVppd to 125 mVppd @ 1.0 MHz OUT± to 90% final value, Slow Decay 2 Mode		1.8		µs
		IN± = 250 mVppd to 125 mVppd @ 1.0 MHz OUT± to 90% final value, Slow Decay 1 Mode		12		µs
	TGD2	IN± = 50 mVppd to 25 mVppd @ 1.0 MHz OUT± to 90% final value, Slow Decay 2 Mode		3.6		µs
		IN± = 50 mVppd to 25 mVppd @ 1.0 MHz OUT± to 90% final value, Slow Decay 1 Mode		60		µs
Gain Attack Time	TGA	WG = logic high to logic low IN± = 250 mVppd @ 1.0 MHz OUT± to 110% final value		2		µs

HYSTERESIS COMPARATOR

Unless otherwise specified, recommended operating conditions apply. Input DIN± is AC coupled, 1.0 Vppd @ 1.0 MHz sinewave. 0.5 VDC is applied to the HYS pin. WG = logic low

Input Signal Range	IRHC				1.5	Vppd
Differential Input Resistance	RHCD	DIN± = 100 mVppd	15	20	25	kΩ
Differential Input Capacitance	CHCD	DIN± = 100 mVppd @ 2.0 MHz			5	pF
Single Ended Input Impedance	RHCC	DIN+ = DIN-	4	5	6	kΩ
Level Gain from DIN± to LEVEL	KLD	0.5 Vppd ≤ DIN± ≤ 1.5 Vppd 10 kΩ from LEVEL to AGND1 270 pf from LEVEL to AGND1	0.75	1	1.25	V/Vppd
Level Pin Output Offset Voltage	VLOS	DIN± = 0 Vppd; 10 kΩ from LEVEL to AGND1		100		mV
Level Pin Output Impedance	ZLV	I@LEVEL = -0.2 mA DIN± = 0.5 VDC		350		Ω
Level Pin Maximum Output Current	ILMX		1.5			mA

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HYSTERESIS COMPARATOR (continued)

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
TRKAA Gain from DIN± to TRKAA	KTD	0.5 Vppd ≤ DIN ± ≤ 1.5 Vppd 10 kΩ from TRKAA to AGND1 360 pF from TRKAA to AGND1	1.0	1.33	1.66	V/Vppd
TRKAA Pin Output Offset Voltage	VTOS	DIN± = 0 Vppd; 10 kΩ from TRKAA to AGND1		100		mV
TRKAA Pin Output Impedance	ZTV	I@TRKAA = -0.2 mA DIN± = 0.5 VDC		300		Ω
TRKAA Pin Maximum Output Current	ITMX		1.5			mA
Hysteresis Gain	KHYS	0.3V < HYS < 1.0V	0.34	0.38	0.42	V/V
HYS Pin Current	IHYS	0.5V < HYS < 1.5V	-10		0	µA
Comparator Offset Voltage	VHCOS	HYS pin at AGND; < 1.5 kΩ across DIN+ to DIN-, 5 kΩ from DOUT to DGND		5	15	mV

ACTIVE DIFFERENTIATOR

Unless otherwise specified, recommended operating conditions apply. Input CIN± is AC coupled, 1.0 Vppd, 1.0 MHz sinewave.

100Ω resistor in series with 150 pF capacitor are tied across DIF+ to DIF1-.

Input Signal Range	IRAD				1.5	V
Differential Input Resistance	RADD	CIN± = 100 mVppd	15	20	25	kΩ
Differential Input Capacitance	CADD	CIN± = 100 mVppd @ 2.0 MHz			5	pF
Single Ended Input Impedance	RADC	CIN+, CIN-	4	5	6	kΩ
Voltage Gain from CIN± to DIF±	KAD	1.2 kΩ from DIF+ to DIF-		1		V/V
DIF+ to DIF- Pin Current	IDIF	Differentiator impedance must be set so as not to clip the signal for this current level	-1.0		+1.0	mA
Comparator Offset Voltage	VADOS	DIF± AC coupled, 5 kΩ from COUT to DGND		0	5	mV
COUT Pin Output High Voltage	PWC	5 kΩ from COUT to DGND		30		ns

QUALIFIER TIMING

Unless otherwise specified, recommended operating conditions apply. Inputs CIN± and DIN± are in-place as AC coupled, 1.0 Vppd, 1.0 MHz sinewave. 100Ω resistor in series with 150 pF capacitor are tied from DIF+ to DIF1-. 0.5V is applied to the HYS pin.

$\overline{RDO}$ is enabled as an output, $\overline{OEN}$ = logic low, WG = logic low

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
D Flip-Flop Set Up Time	TD1	Minimum allowable time delay from DIN± exceeding hysteresis point to DIF± hitting a peak value	0			ns
Propagation Delay from Positive Peak to $\overline{RDO}$ Pulse	TD3			50		ns
Propagation Delay from Negative Peak to $\overline{RDO}$ Pulse	TD4			50		ns
Pulse Pairing |TD3 - TD4|	PP				3	ns
$\overline{RDO}$ Pulse Width	TRD		20	25	30	ns

SYNCHRONIZER SECTION

READ MODE

Read Reference Clock Rise Time	TRRC	0.8V to 2.0V; CL ≤ 15 pF			8	ns
Read Reference Clock Fall Time	TFRC	2.0V to 0.8V; CL ≤ 15 pF			5	ns
Read Reference Clock Pulse Width	TWRC	To = Read Reference Clock Period	0.5•To-10		0.5•To+10	
Read Data Pulse Width	TSRD	To = Read Reference Clock Period	To - 5	To	To + 5	ns
Read Data Rise Time	TRSRD	0.8V to 2.0V; CL ≤ 15 pF			10	ns
Read Data Fall Time	TFSRD	2.0V to 0.8V; CL ≤ 15 pF			8	ns
SRD Output Setup wrt RRC Rise	TSSRD		15			ns
SRD Output Hold wrt RRC Rise	THSRD		15			ns
$\overline{RDI}$ Pulse Width	TRDI	To = Read Reference Clock Period	15		To/2	ns

SYNCHRONIZER SECTION (continued)

DATA SYNCHRONIZATION

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
VCO Center Frequency Period	TVCO	V@FLTR = 2.7V, VPA2 = 5.0V Serial Reg 2 = 000X T1 = 167 ns Serial Reg 2 = 001X T1 = 143 ns Serial Reg 2 = 010X T1 = 125 ns Serial Reg 2 = 011X T1 = 111 ns Serial Reg 2 = 100X T1 = 100 ns Serial Reg 2 = 101X T1 = 91 ns Serial Reg 2 = 110X T1 = 83 ns Serial Reg 2 = 111X T1 = 77 ns	0.8 T1	T1	1.2 T1	ns
VCO Frequency Dynamic Range	VDR	1.0V ≤ V@FLTR ≤ VPA2 - 0.6V VPA2 = 5.0V	±24	±34	±45	%
VCO Control Gain	KVCO	V@FLTR = 2.7V; ωo = 2π/TVCO	0.14 ωo	0.20 ωo	0.26 ωo	rad/s-V
Phase Detector Gain	KD2	KD2 = 0.62/(RR + 527) VPA2 = 5V (RR = 7.5 kΩ)	0.83 KD2	KD2	1.17 KD2	A/rad
	KD1	KD1 = 3 x KD2 VPA2 = 5V (RR = 7.5 kΩ)	0.83 KD1	KD1	1.17 KD1	A/rad
FL1-4 High Impedance	FLZH		2			kΩ
FL1-4 Low Impedance	FLZL				100	Ω
KVCO x KD Product Accuracy	KPA		-28	0	28	%
VCO Phase Restart Error	PRE			4		ns
Decode Window	DW	To = Read Reference Clock Period	To - 2	To		ns
Decode Window Center Accuracy	DWCA		-5% To		+5% To	ns
Decode Window Shift Magnitude		Serial Register 1 = 1X00 TS1 = ±40% To/2 To = RRC period	0.8 TS1	TS1	1.2 TS1	ns
		Serial Register 1 = 1X01 TS2 = ±30% To/2 To = RRC period	0.8 TS2	TS2	1.2 TS2	ns
		Serial Register 1 = 1X10 TS3 = ±20% To/2 To = RRC period	0.8 TS3	TS3	1.2 TS3	ns

MISCELLANEOUS TIMING

PARAMETER		CONDITION	MIN	NOM	MAX	UNIT
RG, WG Time Delay	RWTD				100	ns

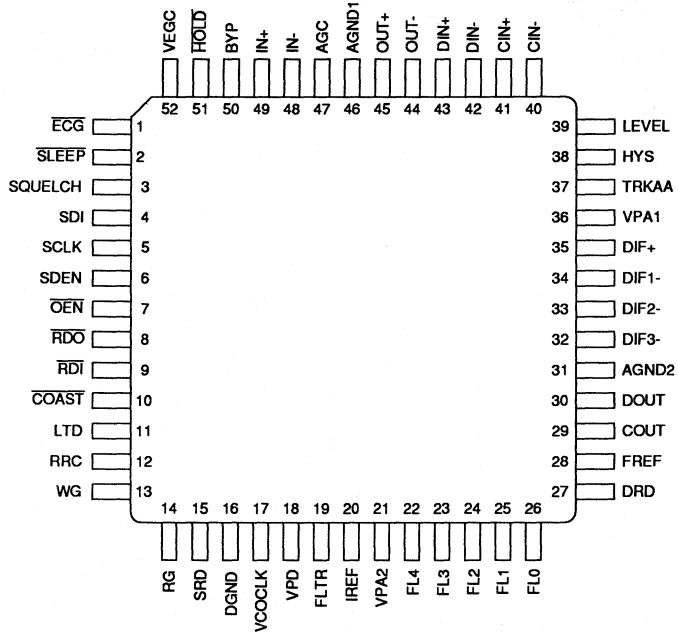
SERIAL PORT SECTION

SCLK Period	TC		100			ns
SDEN Setup to SCLK	T1		10		TC/2 -10	ns
SDEN Hold after SCLK	T2A		10		TC/4	ns
SDEN Falls prior to SCLK rises	T2B		25			ns
SDI Setup to SCLK	T3		25			ns
SDI Hold after SCLK	T4		25			ns

SSI 34P3201
Pulse Detector & Data Synchronizer, 250K to 8.0 Mbit/s

PACKAGE PIN DESIGNATIONS
(Top View)

CAUTION: Use handling procedures necessary for a static sensitive component.



52-Lead QFP

ORDERING INFORMATION

PART DESCRIPTION	ORDER NO.	PKG. MARK
SSI 34P3201 - 52-Lead QFP	34P3201-CG	34P3201-CG

Preliminary Data: Indicates a product not completely released to production. The specifications are based on preliminary evaluations and are not guaranteed. Small quantities are available, and Silicon Systems should be consulted for current information.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914

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SSI 34R1203R
+5V, 2, 4-Channel, 3-Terminal Read/Write Device

January 1994

DESCRIPTION

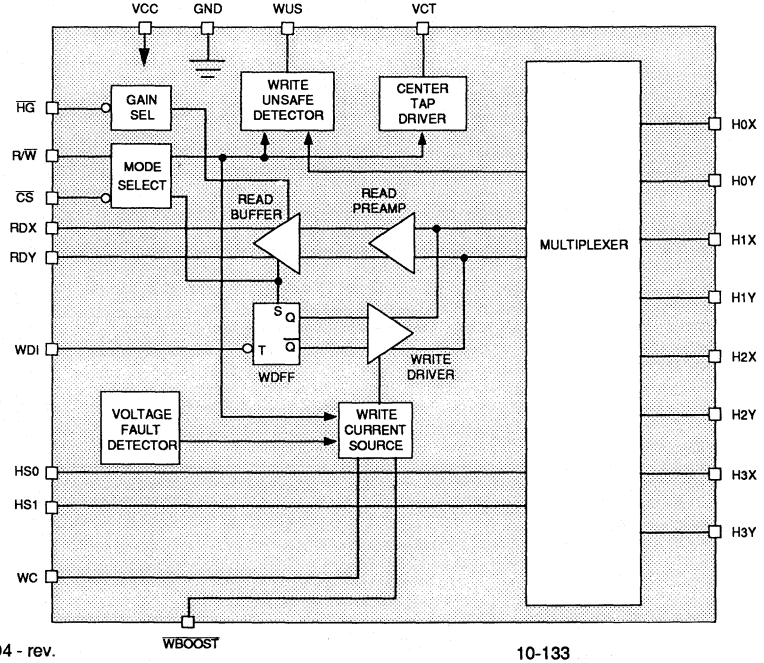
The SSI 34R1203R is a bipolar monolithic integrated circuit designed for use with center-tapped ferrite or MIG recording heads. It provides a low noise read path with selectable gains of 85 and 250 V/V, write current control, and data protection circuitry for as many as 4 channels. Power supply fault protection is provided by disabling the write current generator during power sequencing. A Power Down mode (Idle) is provided to reduce power consumption to less than 10 mW. Included is a write current boost feature which can be selected without using additional external resistors.

Internal 750Ω damping resistors are provided. It requires only a +5V power supply and is available in a surface mount package.

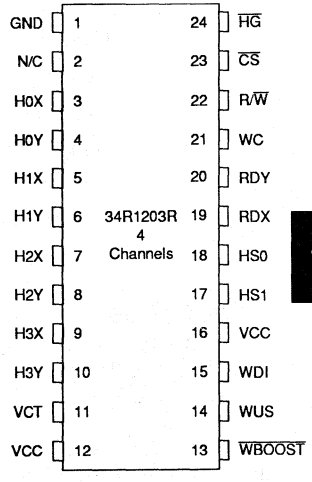
FEATURES

- **Pin selectable gain, 250 V/V and 85 V/V**
- **+5V only power supply**
- **Low power**
  - **Pd ≤ 220 mW Read mode**
  - **Pd ≤ 10 mW Idle mode**
- **High Performance**
  - **Input noise = 1.2 nV/√Hz max.**
  - **Input capacitance = 19 pF max.**
  - **Write current range = 15 - 50 mA**
  - **Head voltage swing = 6.0 Vpk**
- **Designed for center-tapped ferrite or MIG heads**
- **TTL selectable write current boost**
- **Power supply fault protection**
- **Includes write unsafe detection**
- **Enhanced Write to Read recovery**

BLOCK DIAGRAM



PIN DIAGRAM



24-Lead VSOP

CAUTION: Use handling procedures necessary for a static sensitive component.

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SSI 34R1203R
+5V, 2, 4-Channel, 3-Terminal Read/Write Device

DESCRIPTION

WRITE MODE

A source of recording current is provided to the head center tap by an internal voltage reference, VCT. The current is conducted through the head alternately into an HnX terminal or an HnY terminal according to the state of an internal flip-flop. The flip-flop is triggered by the negative transition of the Write Data Input line (WDI). A preceding read mode selection initializes the write data flip-flop, WDFF, to pass write current through the "X" side of the head. The write current magnitude is determined by the value of an external resistor Rwc connected between WC terminal and GND, and is given by:

Iw = K/Rwc, where K = Write Current Constant

In addition, this current can be given a 30% boost without switching in additional resistance values by pulling $\overline{\text{WBOOST}}$ low .

WRITE MODE FAULT DETECT CIRCUIT

Several circuits are dedicated to detecting fault conditions associated with the Write mode. A logical high level will be present at the Write Unsafe (WUS) terminal if any of the following write fault conditions are present:

- Head open
- Head center tap open
- Head shorted
- Head shorted to ground
- No write current
- WDI frequency too low
- Device in read or idle mode

The Write Unsafe output is open-collector and is usually terminated by an external resistor connected to VCC. Two negative transitions on WDI, after the fault is corrected, will clear the WUS flag.

A safe condition, WUS low , requires alternating voltage spikes on both HnX and HnY that exceed VCT + 1.5V at a rate equal to or higher than the Minimum Rate of WDI for Safe condition.

In addition, the power supply voltage level is monitored by a circuit that inhibits the write current if VCC is too low to permit valid data recording.

READ MODE

In Read Mode, (R/$\overline{\text{W}}$ high and $\overline{\text{CS}}$ low), the circuit functions as a low noise gain selectable differential amplifier. The read amplifier input terminals are determined by the Head Select inputs. The read amplifier outputs (RDX, RDY) are emitter follower sources, providing low impedance outputs. The amplifier polarity is non-inverting between HnX, HnY inputs and RDX, RDY outputs. Taking $\overline{\text{HG}}$ low selects high gain (250 V/V). Taking $\overline{\text{HG}}$ high or open selects low gain (85 V/V).

IDLE MODE

Taking $\overline{\text{CS}}$ high selects the Idle mode which switches the RDX and RDY outputs into a high impedance state and deactivates the device. Power consumption in this mode is held to a minimum.

MODE SELECTION AND INDICATION CIRCUIT

Logical control inputs which select mode and head channel are TTL compatible. Their functions are described in Table 1 and Table 2.

TABLE 1: Head Select Table

Head Selected	HS1	HS0
0	0	0
1	0	1
2	1	0
3	1	1

TABLE 2: Mode Select Table

Mode Select		Selected Mode	Indicating & Fault Outputs
$\overline{\text{CS}}$	R/$\overline{\text{W}}$		WUS
1	X	Idle	high
0	1	Read	high
0	0	Write	active

PIN DESCRIPTION

NAME	I/O	DESCRIPTION
HS0, HS1	I*	Head Select: Logical combinations select one of four Heads. See Table 1
$\overline{CS}$	I	Chip Select: a low level enables device. Has internal pull-up resistor.
R/$\overline{W}$	I*	Read/Write: a high level selects read mode. Has internal pull-up resistor.
WUS	O*	Write Unsafe: a high level indicates an unsafe writing condition.
WDI	I*	Write Data In: negative transition toggles direction of head current.
H0X-H3X H0Y-H3Y	I/O	X, Y head connections
RDX, RDY	O*	X, Y Read Data: differential read signal output.
WC	-	Write Current: used to set the magnitude of the write current.
$\overline{WBOOST}$	I*	A logic low signal on this pin increases the magnitude of write current by typically 30%.
VCT	-	Voltage Center Tap: voltage source for head center tap.
VCC	-	+5V
GND	-	Ground
$\overline{HG}$	I*	Gain select: $\overline{HG}$ low selects 250 V/V. $\overline{HG}$ high or open selects 85 V/V.
* When more than one R/W device is used, these signals can be wire OR'ed with unselected R/W devices.		

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND. Currents into device are positive.)

PARAMETER		RATING
DC Supply Voltage	VCC	-0.3 to +6 VDC
Digital Input Voltage Range HS1, HS0, WDI, R/$\overline{W}$, $\overline{CS}$, $\overline{WBOOST}$, $\overline{HG}$		-0.3 to (VCC + 0.3 VDC)
Head Port Voltage Range	VH	-0.3 to (VCC + 3.0 VDC)
Write Current Pin Voltage	Vwc	-0.3 to (VCC + 0.3 VDC)
WUS Pin Voltage Range	Vwus	-0.3 to +6.0 VDC
Write Current Zero–Peak	IW	60 mA
RDX, RDY Output Current	Io	-10 mA
RDX, RDY Pin Voltage		VCC + 0.3 VDC
VCT Output Current Range	IVCT	-60 mA to +10 mA
WUS Output Current Range	Iwus	-0.1 mA to +10 mA
Storage Temperature Range	Tstg	-65 to 150 °C
Package Temperature (20 sec Reflow)		215 °C

RECOMMENDED OPERATION CONDITIONS

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
DC Supply Voltage	VCC		4.75	5.0	5.25	VDC
Head Inductance	Lh		1		15	µH
Write Current Range	IW		15		50	mA
Junction Temperature Range	Tj		+25		+135	°C

DC CHARACTERISTICS

(Unless otherwise specified, recommended operating conditions apply.)

POWER SUPPLY

VCC Supply Current (ICC)	Read Mode		32	42	mA
	Idle Mode		1.4	2.0	mA
	Write Mode		31 + Iw	44 + Iw	mA
Power Dissipation	Read Mode		160	220	mW
	Idle Mode		7	10.5	mW
	Write Mode		155 + 5 Iw	230 + 5.5 Iw	mW

DIGITAL I/O

Input Low Voltage $\overline{CS}$, R/$\overline{W}$ WDI, HS0, HS1, $\overline{WBOOST}$, $\overline{HG}$	VIL				0.8	VDC
Input High Voltage $\overline{CS}$, R/$\overline{W}$ WDI, HS0, HS1, $\overline{WBOOST}$, $\overline{HG}$	VIH		2.0			VDC
Input Low Current $\overline{CS}$, R/$\overline{W}$ WDI, HS0, HS1, $\overline{WBOOST}$, $\overline{HG}$	IIL	VIL = 0.4V	-0.4			mA
Input High Current $\overline{CS}$, R/$\overline{W}$ WDI, HS0, HS1, $\overline{WBOOST}$, $\overline{HG}$	IIH	VIH = 2.7V			20	µA
WUS Output Low Voltage	VOL	IOL = 4.0 mA			0.5	VDC
WUS Output High Current	IOH	VOH = 5.0V			100	µA

WRITE MODE

Center Tap Voltage	VCT	Write Mode/Idle Mode		Vcc - 0.9		VDC
Head Current (per side)		Write Mode, Voltage Fault $0 \le VCC \le 3.9V$	-200		200	µA
Write Current Range		$1.0\ k\Omega \le Rwc \le 3.3\ k\Omega$	15		50	mA

WRITE MODE (continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Write Current Constant "K"		46	50	54	mA-kΩ
Iwc to Head Current Gain			20		mA/mA
$\overline{\text{WBOOST}}$ - Write Current Boost Factor	$\overline{\text{WBOOST}}$ = Low	1.25	1.30	1.35	mA/mA
Unselected Head Leakage Current				85	µA
RDX, RDY Common Mode Output Voltage		Vcc - 3	Vcc - 2.4	Vcc - 2	VDC
WDI Minimum Pulse Width	PWH VIL ≥ 0.2V		11		ns
See Figure 1	PWL VIN ≥ 2.4V		4		ns

READ MODE

Center Tap Voltage VCT			Vcc - 1.5		VDC
Input Bias Current (per side)	From VCT to HnX or HnY		20	60	µA
Output Offset Voltage	RDX - RDY	-200		+200	mV
Common Mode Output Voltage	$\frac{\text{RDX + RDY}}{2}$	2	Vcc - 2.4	3.5	VDC
Common Mode Output Voltage Change from Write to Read Mode		-100		+100	mV

FAULT DETECTION CHARACTERISTICS

Unless otherwise specified recommended conditions apply, Iw = 30 mA, Lh = 5 µH, F(WDI) = 10 MHz.

Minimum Rate of WDI Input for Safe condition		150			kHz
Maximum Rate of WDI Input for Unsafe condition				50	kHz
Minimum voltage value for guaranteed write current turn-on		4.4			VDC
Maximum voltage value for guaranteed write current turn-off				3.9	VDC

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DYNAMIC CHARACTERISTICS AND TIMING

(Unless otherwise specified, recommended operating conditions apply and Iw = 30 mA, Lh = 5 µH, f(WDI) = 5 MHz, CL(RDX, RDY) ≤ 20 pF.)

WRITE MODE

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNITS
Differential Head Voltage Swing		6.0	6.4		V(pk)
Unselected Head Transient Current	1 µH ≤ Lh ≤ 9.5 µH			2	mA(pk)
Differential Output Capacitance				15	pF
Differential Output Resistance		600		960	Ω

READ MODE

Differential Voltage Gain	Vin = 1 mVrms @ 1 MHz				
	$\overline{HG}$ = High	68	85	102	V/V
	$\overline{HG}$ = Low	200	250	300	V/V
Bandwidth (-3dB)	|Zs| < 5Ω, Vin = 1 mVpp	30	60		MHz
Input Noise Voltage	BW = 15 MHz, Lh = 0, Rh = 0		0.85	1.2	nV/√Hz
Differential Input Capacitance	Vin = 1 mVrms, f = 5MHz		16	19	pF
Differential Input Resistance		460		860	Ω
Dynamic Range	AC input voltage where gain falls to 90% of its small signal gain value, f = 5 MHz	2			mVpp
Common Mode Rejection Ratio	Vcm = 100 mVpp @ 1 MHz < f < 10 MHz	50	75		dB
Power Supply Rejection Ratio	ΔVcc =100 mVpp @ 1 MHz < f < 10 MHz	45			dB
Channel Separation	Unselected Channels: Vin = 20 mVpp 1 MHz < f < 10 MHz	45	54		dB
RDX, RDY Single Ended Output Resistance				30	Ω
Output Current	AC Coupled Load, RDX to RDY	±1.5			mA

SWITCHING CHARACTERISTICS

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNITS
R/$\overline{W}$	Read to Write	R/$\overline{W}$ to 90% of write current		50	400	ns
	Write to Read	R/$\overline{W}$ to 90% of 100 mV 10 MHz read signal envelope or to 10% IW		0.15	1.0	µs
$\overline{CS}$	Unselect to Select	$\overline{CS}$ to 90% of 100 mV 10 MHz read signal envelope		1.0	2.0	µs
	Select to Unselect	$\overline{CS}$ to 10% Ih		0.05	0.6	µs
HS0, 1 to any Head		To 90% of 100 mV 10 MHz read signal envelope			0.6	µs
WUS	Safe to Unsafe (TD1)		7		30	µs
	Unsafe to Safe (TD2)	Write mode, after fault cleared after 2nd transition			350	ns
Head Current		Rh = 0, Lh = 0				
	Prop. Delay (TD3)	From 50% points		25	40	ns
	Asymmetry	WDI has 50% Duty Cycle and 1 ns Rise/Fall Time			2	ns
	Rise/Fall Time	10% - 90% Points		4	20	ns

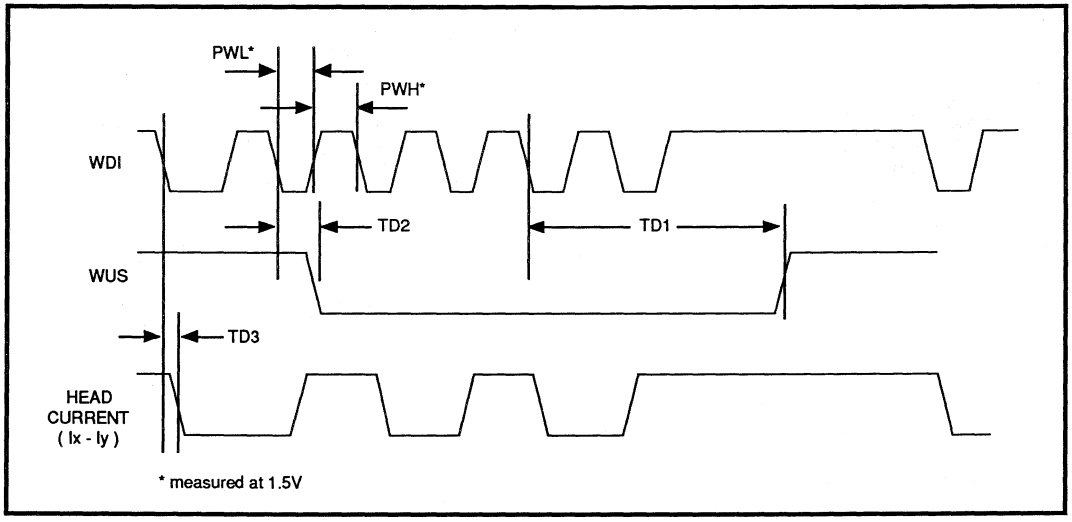

FIGURE 1: Write Mode Timing Diagram

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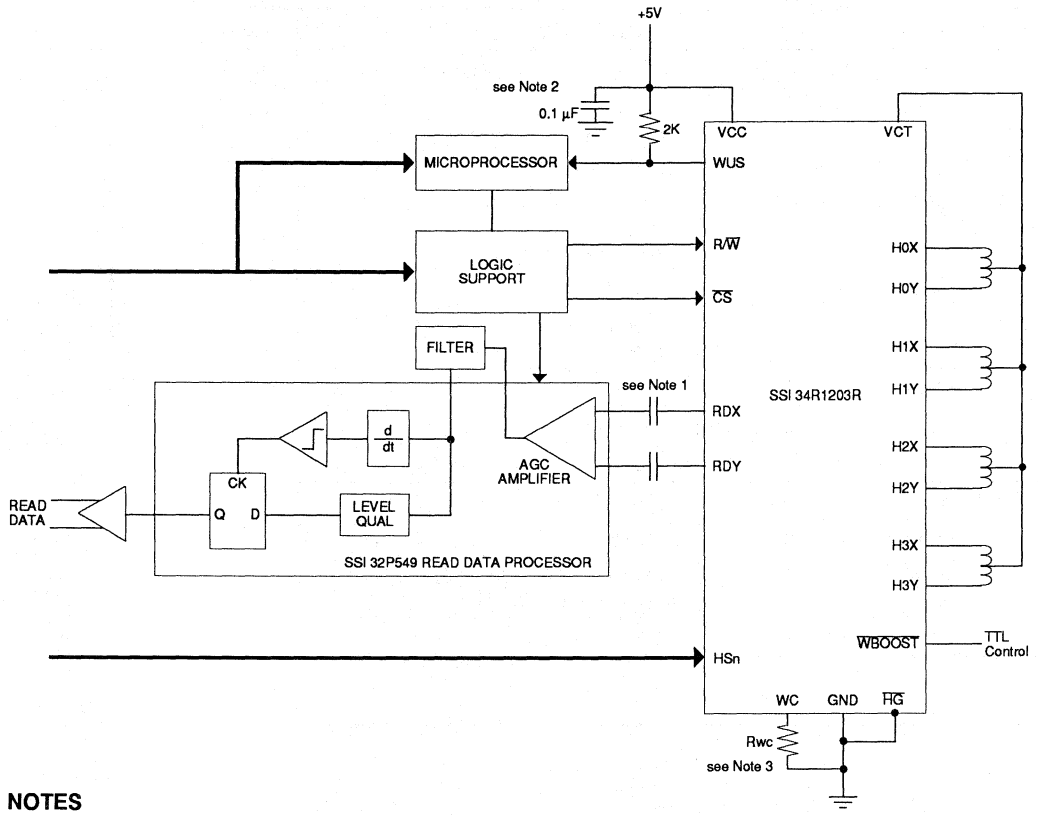


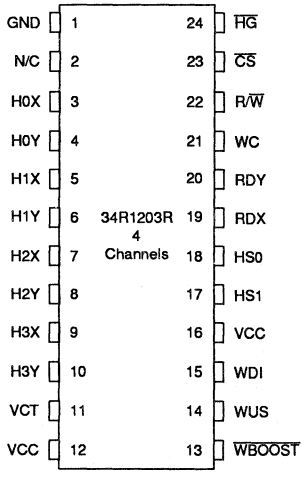
NOTES

1. Limit DC current from RDX and RDY to 100 µA and load capacitance to 20 pF. In multi-chip application these outputs can be wire-OR'ed.
2. The power bypassing capacitor must be located close to the 34R1203R with its ground returned directly to device ground, with as short a path as possible.
3. To reduce ringing due to stray capacitance this resistor should be located close to the 34R1203R. Where this is not desirable a series resistor can be used to buffer a long WC line.

FIGURE 2: Applications Information

PACKAGE PIN DESIGNATIONS

(Top View)



24-Lead VSOP

THERMAL CHARACTERISTICS: θja

24-lead VSOP	110°C/W

CAUTION: Use handling procedures necessary for a static sensitive component.

ORDERING INFORMATION

PART DESCRIPTION	ORDERING NUMBER	PACKAGE MARK
SSI 34R1203R 24-Lead VSOP	SSI 34R1203R-4CV	34R1203R-4CV

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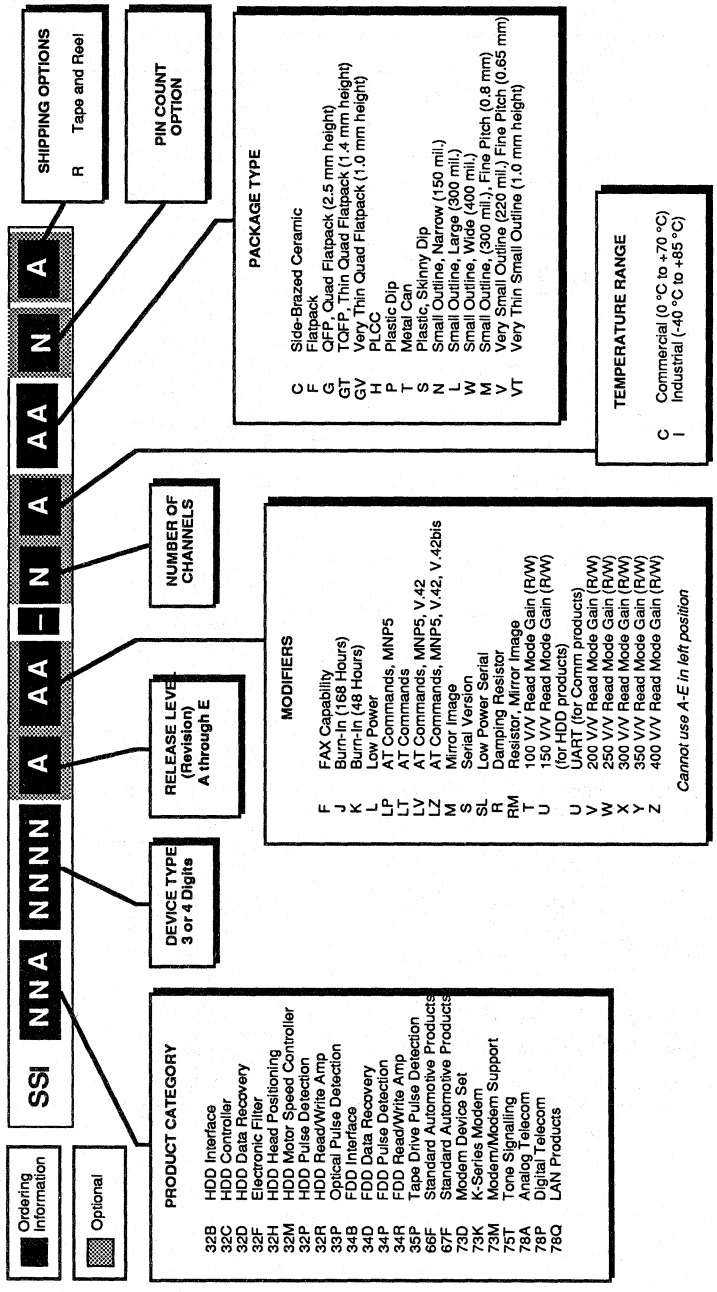
Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX: (714) 573-6914

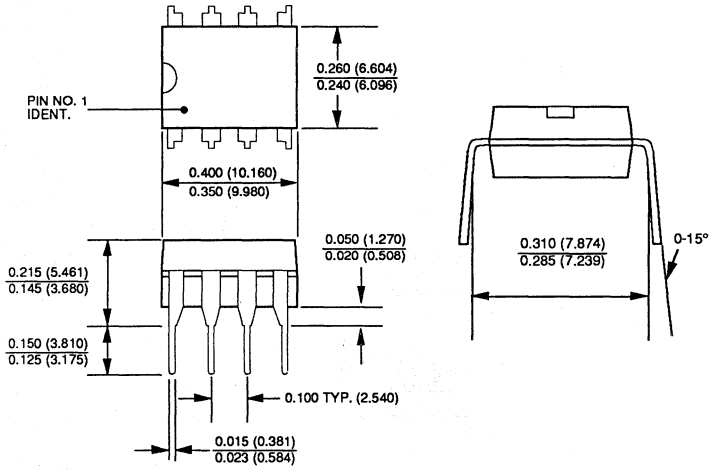
Notes:

Section 11

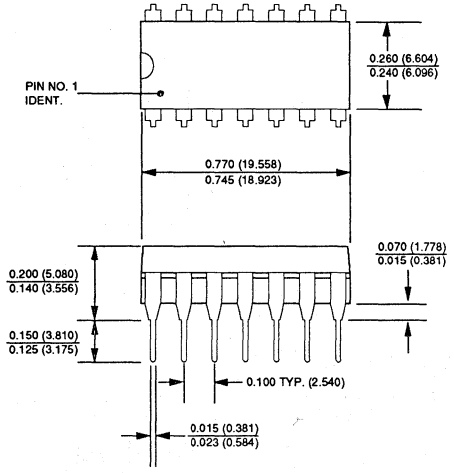
PACKAGING/ORDERING INFORMATION

Silicon Systems
Packaging Index

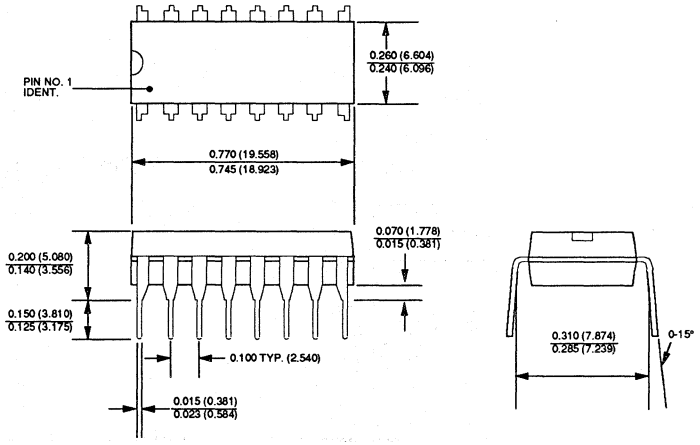

Ordering Information
Optional
SSI NNA NNNN A AA – N A AA N A
PRODUCT CATEGORY
32B HDD Interface
32C HDD Controller
32D HDD Data Recovery
32F Electronic Filter
32H HDD Head Positioning
32M HDD Motor Speed Controller
32P HDD Pulse Detection
32R HDD Read/Write Amp
33P Optical Pulse Detection
34B FDD Interface
34D FDD Data Recovery
34P FDD Pulse Detection
34R FDD Read/Write Amp
35P Tape Drive Pulse Detection
66F Standard Automotive Products
67F Standard Automotive Products
73D Modem Device Set
73K K-Series Modem
73M Modem/Modem Support
75T Tone Signalling
78A Analog Telecom
78P Digital Telecom
78Q LAN Products
DEVICE TYPE 3 or 4 Digits
RELEASE LEVEL (Revision) A through E
MODIFIERS
F FAX Capability
J Burn-In (168 Hours)
K Burn-In (48 Hours)
L Low Power
LP AT Commands, MNP5
LT AT Commands
LV AT Commands, MNP5, V.42
LZ AT Commands, MNP5, V.42, V.42bis
M Mirror Image
S Serial Version
SL Low Power Serial
R Damping Resistor
RM Resistor, Mirror Image
T 100 V/V Read Mode Gain (R/W)
U 150 V/V Read Mode Gain (R/W) (for HDD products)
U UART (for Comm products)
V 200 V/V Read Mode Gain (R/W)
W 250 V/V Read Mode Gain (R/W)
X 300 V/V Read Mode Gain (R/W)
Y 350 V/V Read Mode Gain (R/W)
Z 400 V/V Read Mode Gain (R/W)
Cannot use A-E in left position
NUMBER OF CHANNELS
PACKAGE TYPE
C Side-Brazed Ceramic
F Flatpack
G QFP, Quad Flatpack (2.5 mm height)
GT TQFP, Thin Quad Flatpack (1.4 mm height)
GV Very Thin Quad Flatpack (1.0 mm height)
H PLCC
P Plastic Dip
T Metal Can
S Plastic, Skinny Dip
N Small Outline, Narrow (150 mil.)
L Small Outline, Large (300 mil.)
W Small Outline, Wide (400 mil.)
M Small Outline, (300 mil.), Fine Pitch (0.8 mm)
V Very Small Outline (220 mil.) Fine Pitch (0.65 mm)
VT Very Thin Small Outline (1.0 mm height)
TEMPERATURE RANGE
C Commercial (0 °C to +70 °C)
I Industrial (-40 °C to +85 °C)
PIN COUNT OPTION
SHIPPING OPTIONS
R Tape and Reel



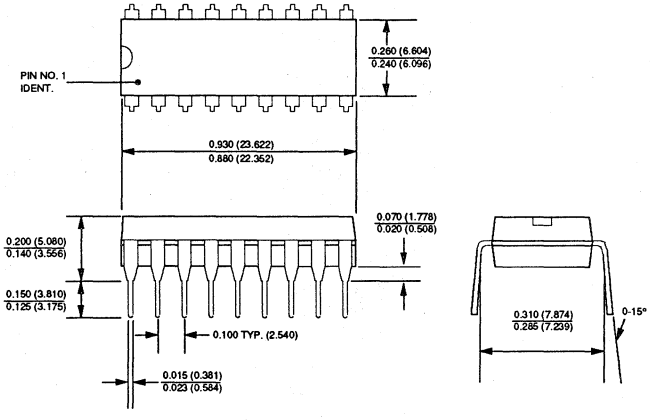
8-Pin Plastic



14-Pin Plastic

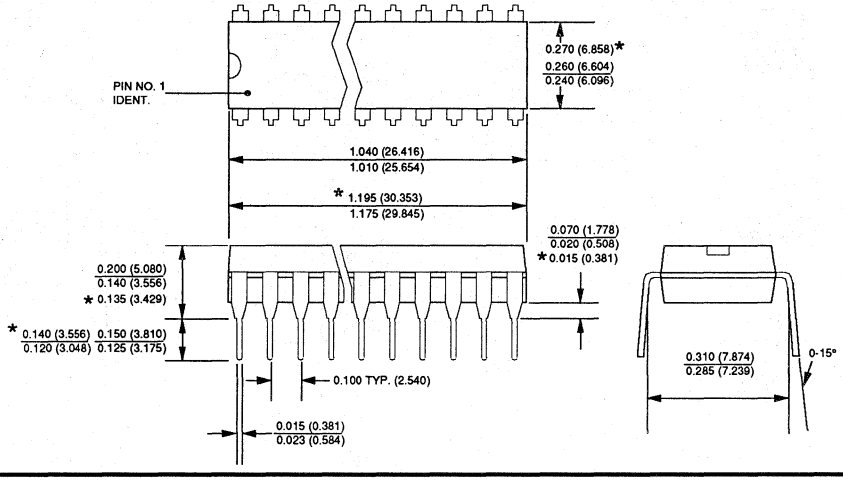


16-Pin Plastic

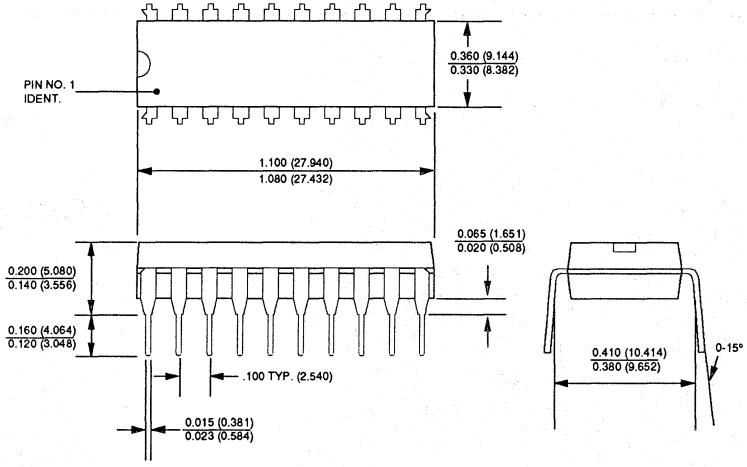


18-Pin Plastic

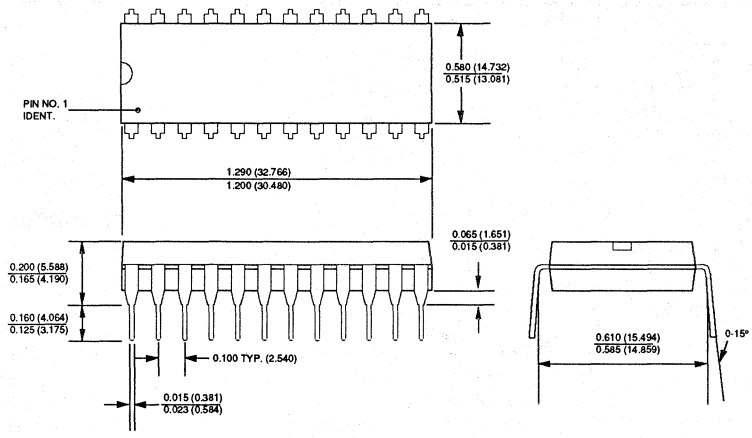
Package Information



20 Pin Plastic
***24S Pin Plastic**

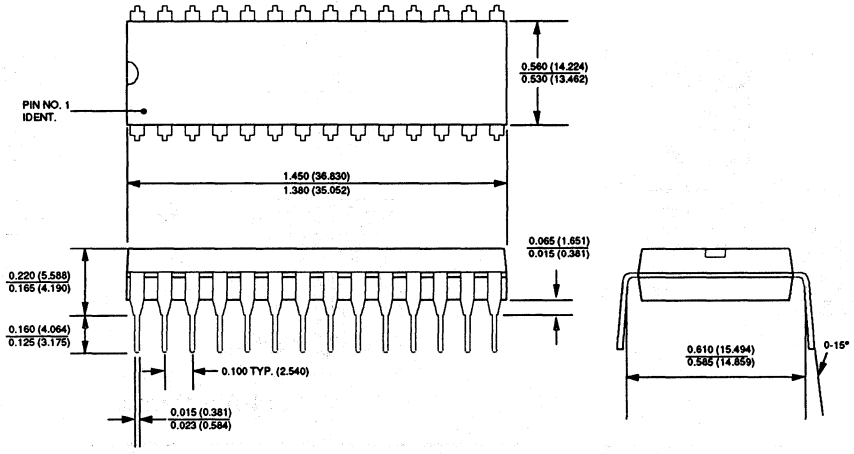


22-Pin Plastic

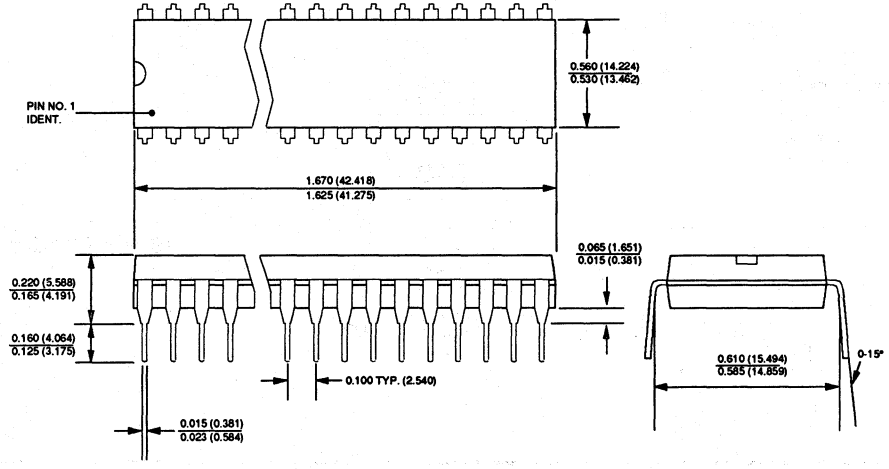


24-Pin Plastic

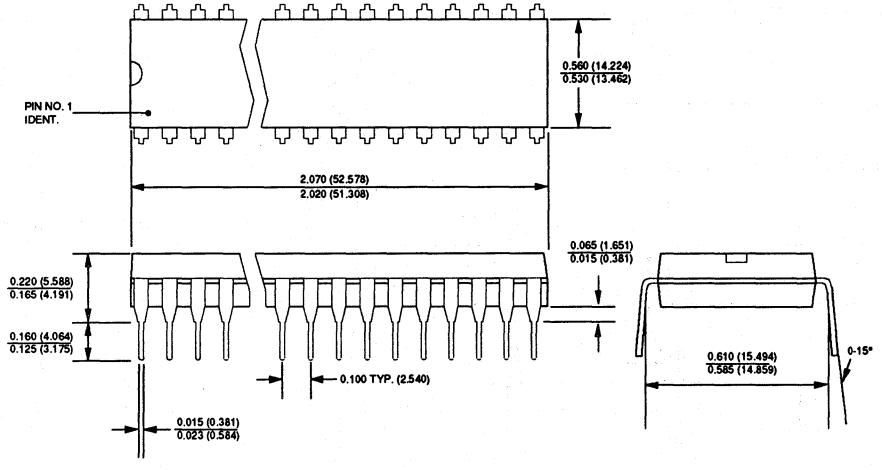
Package Information



28-Pin Plastic

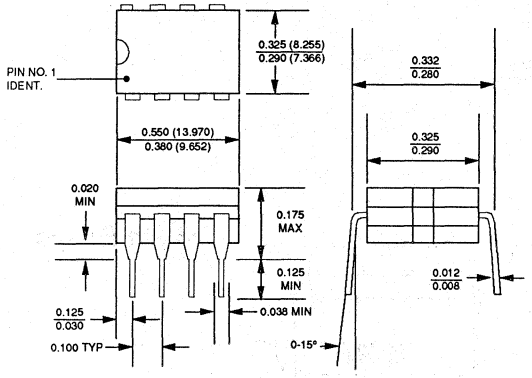


32-Pin Plastic

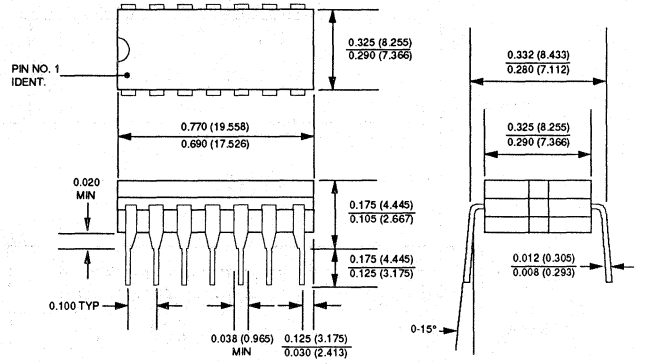


40-Pin Plastic

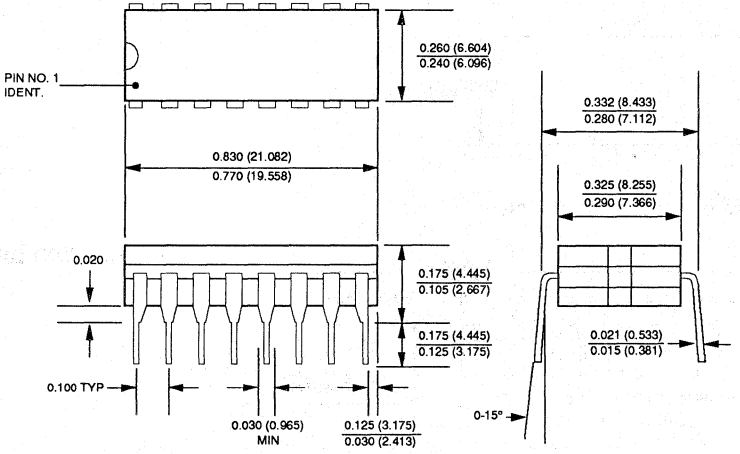
11



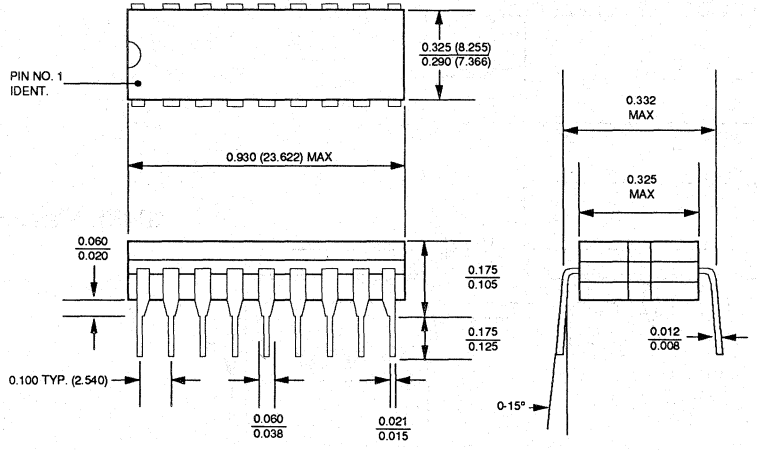
8-Pin Cerdip



14-Pin Cerdip

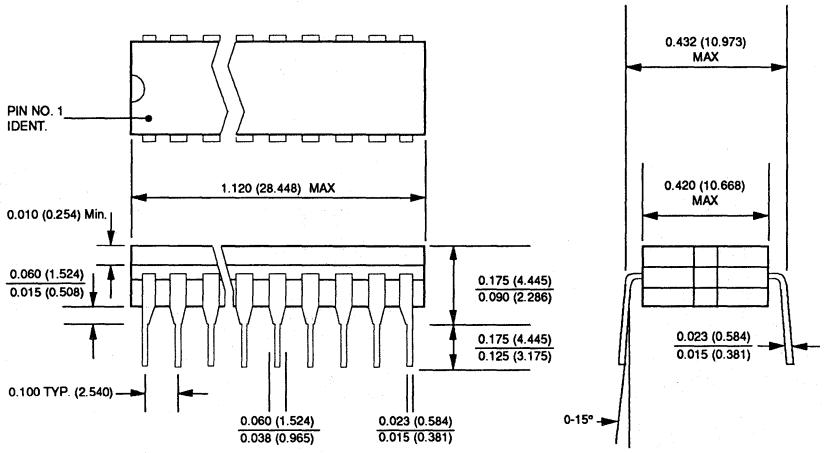


16-Pin Cerdip

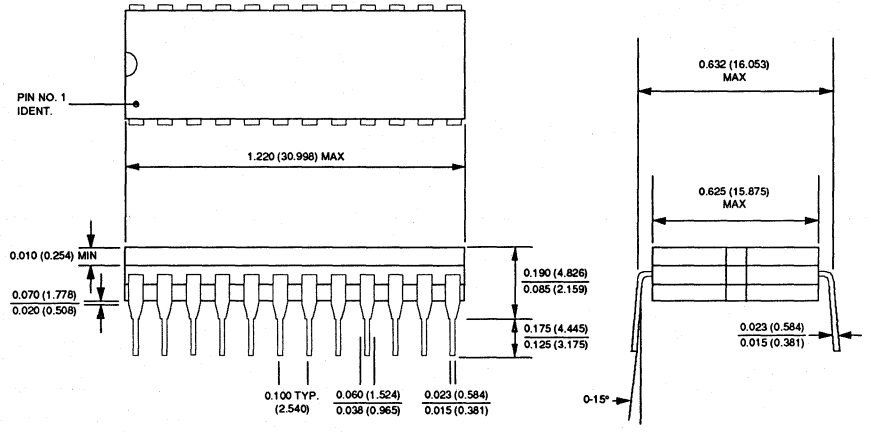


18-Pin Cerdip

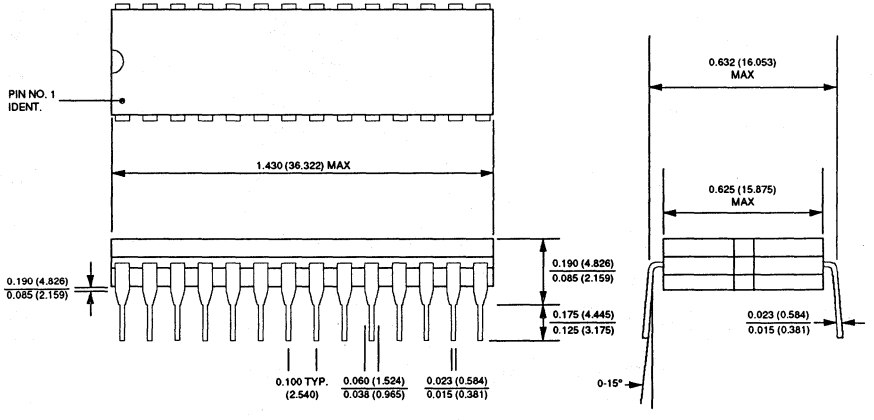
Package Information



22-Pin Cerdip

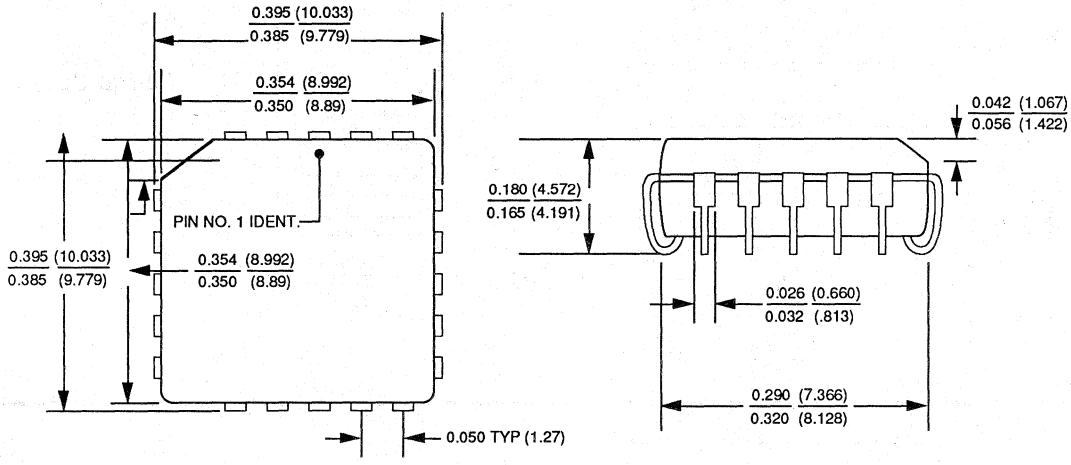


24-Pin Cerdip

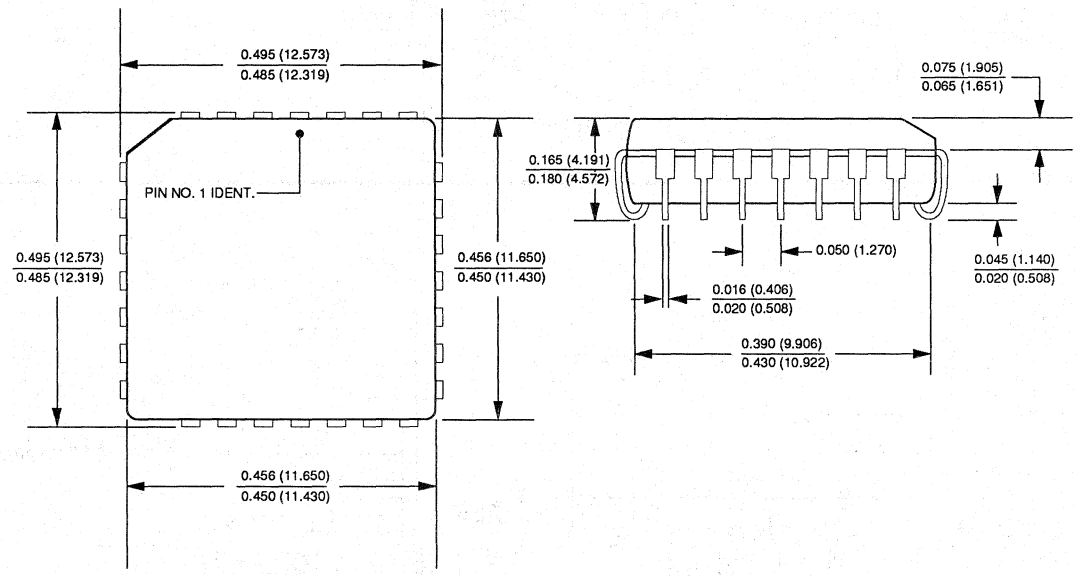


28-Pin Cerdip

11



20-Pin Quad PLCC



28-Pin Quad PLCC

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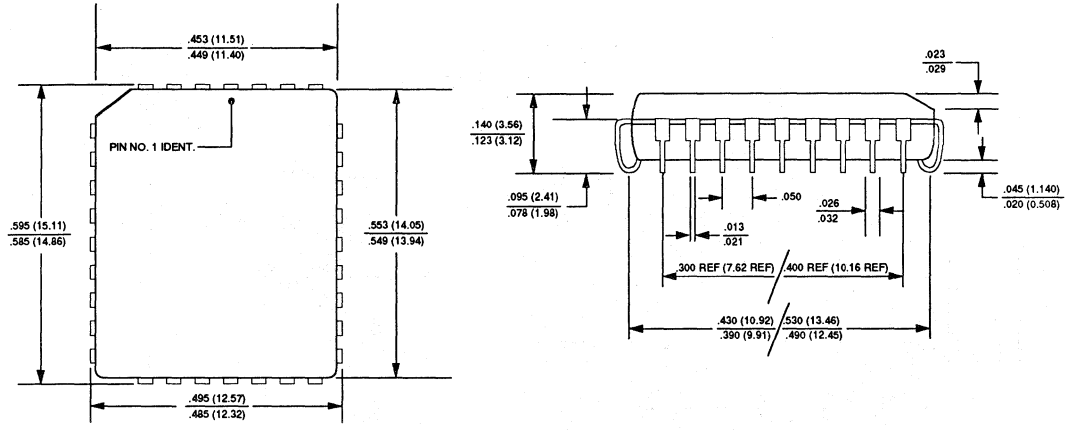
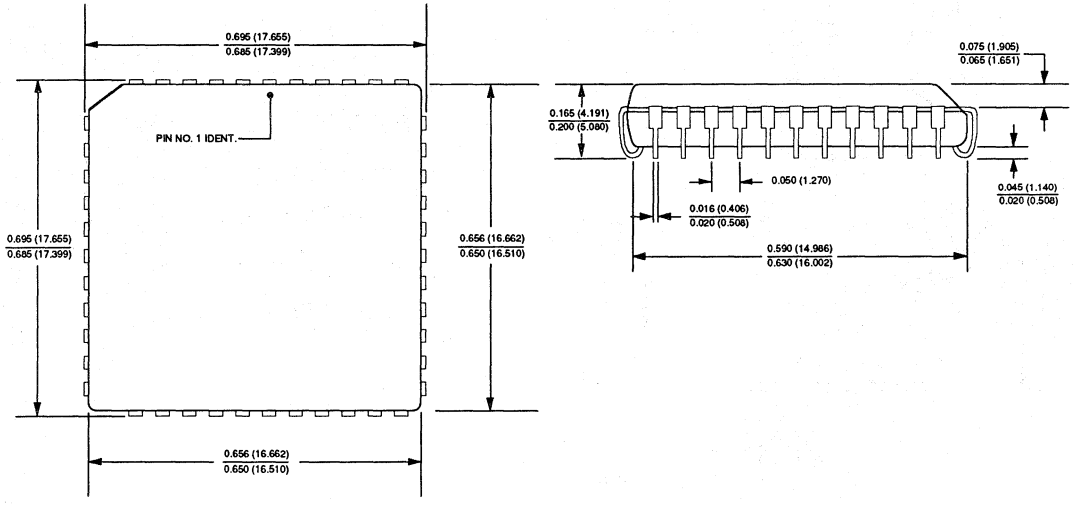


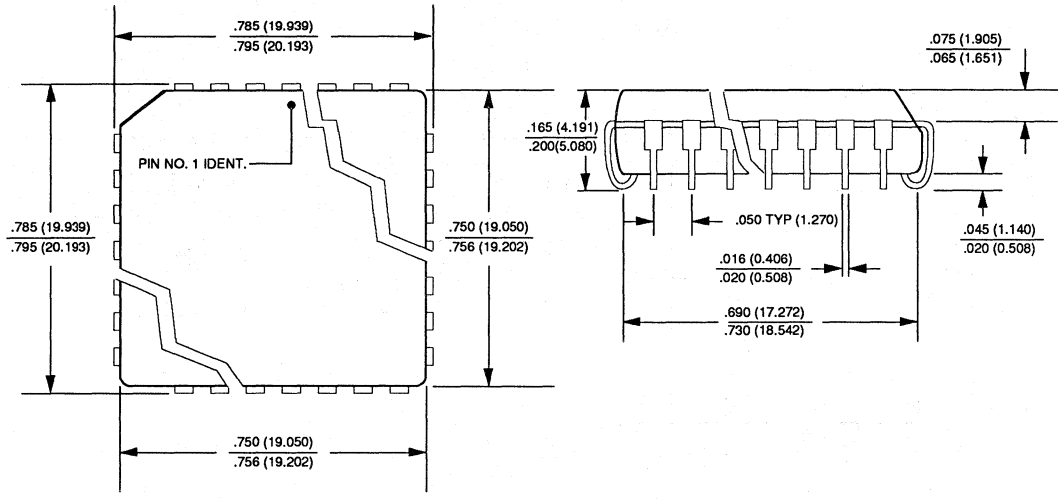
32-Pin Quad PLCC



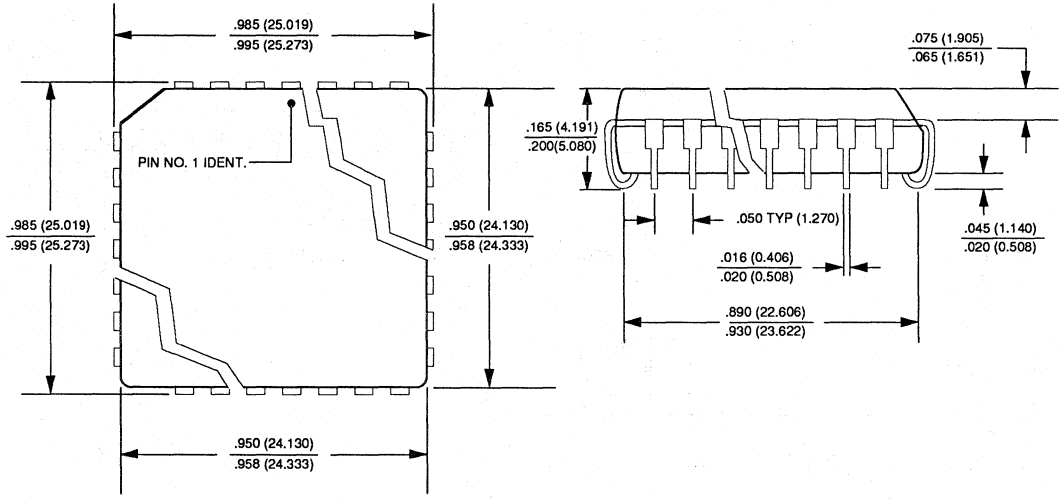
44-Pin Quad PLCC

11

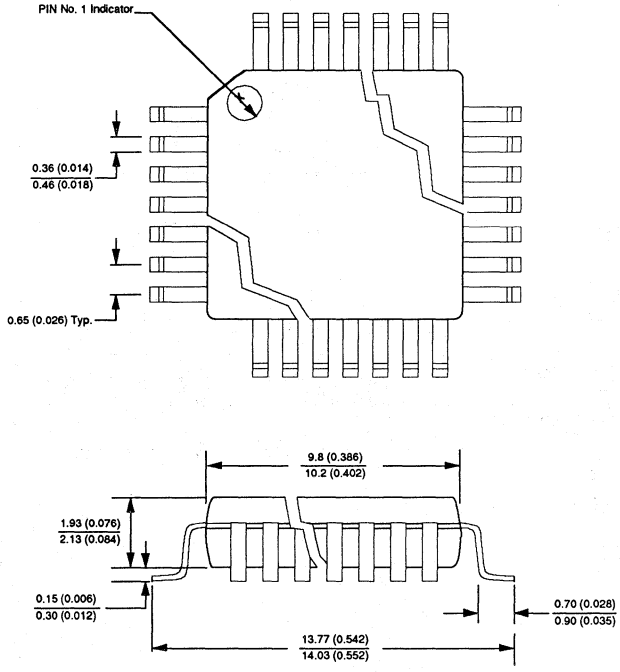
Package Information



52-Pin Quad PLCC

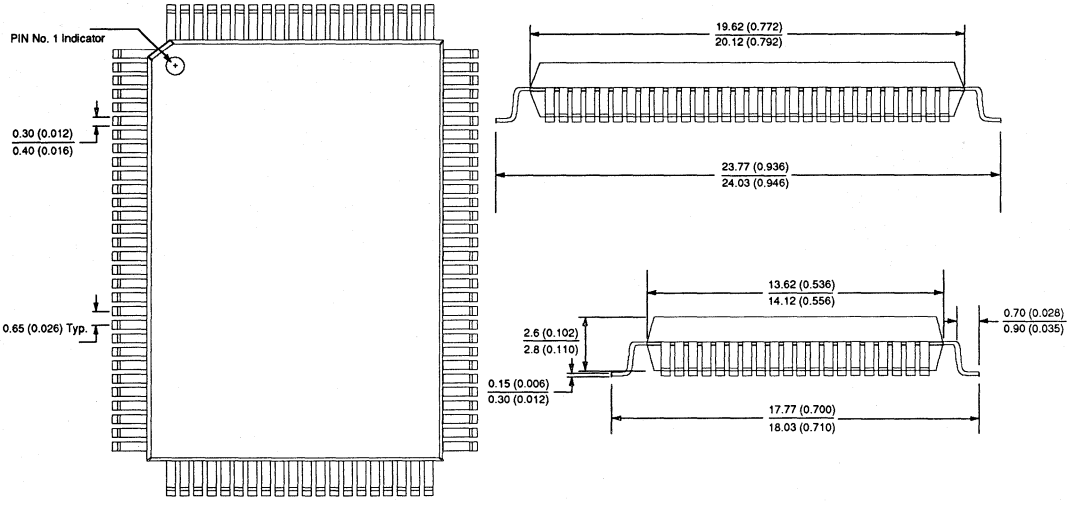


68-Pin Quad PLCC



52-Lead Quad Flatpack

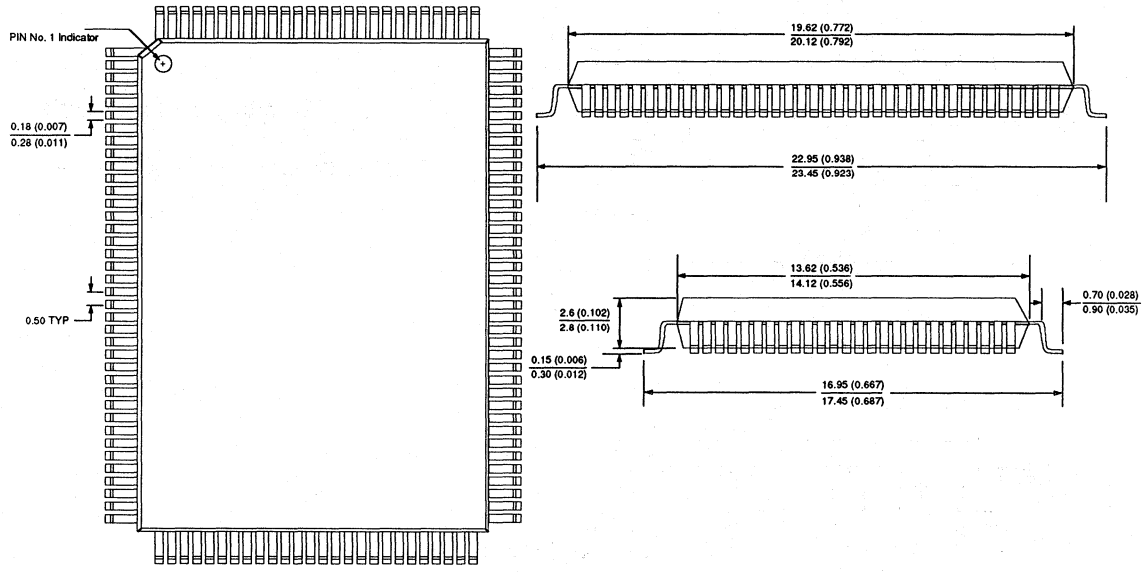
NOTE: Controlling dimensions are in mm



100-Lead Quad Flatpack

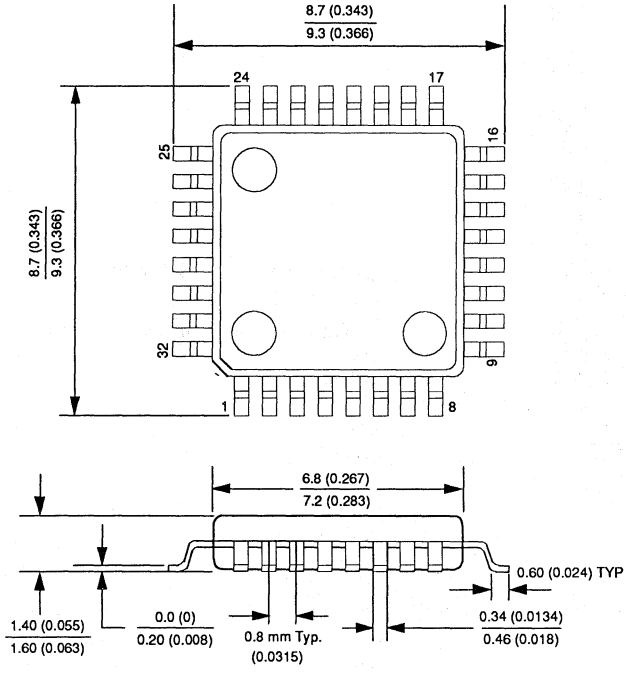
NOTE: Controlling dimensions are in mm

Package Information



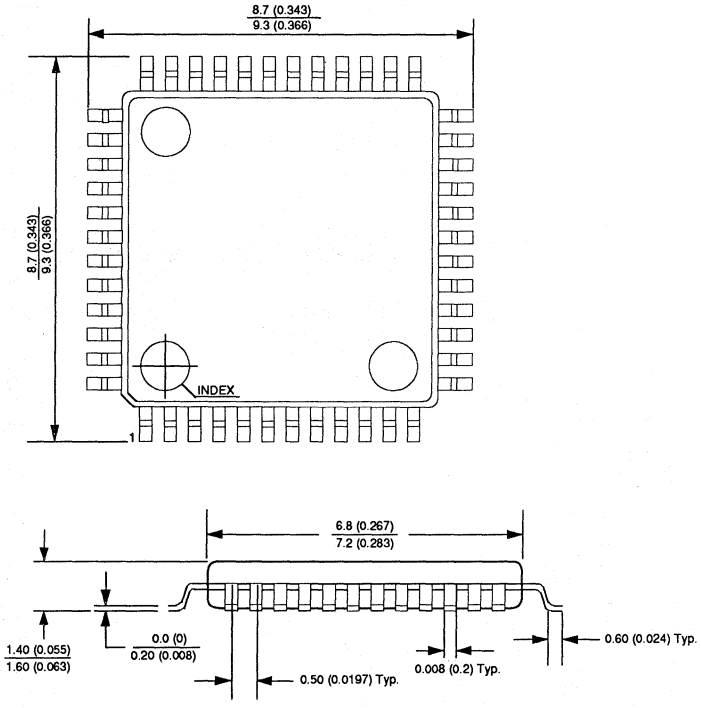
128-Lead Quad Flatpack

NOTE: Controlling dimensions are in mm



32-Lead Thin Quad Flatpack

NOTE: Controlling dimensions are in mm

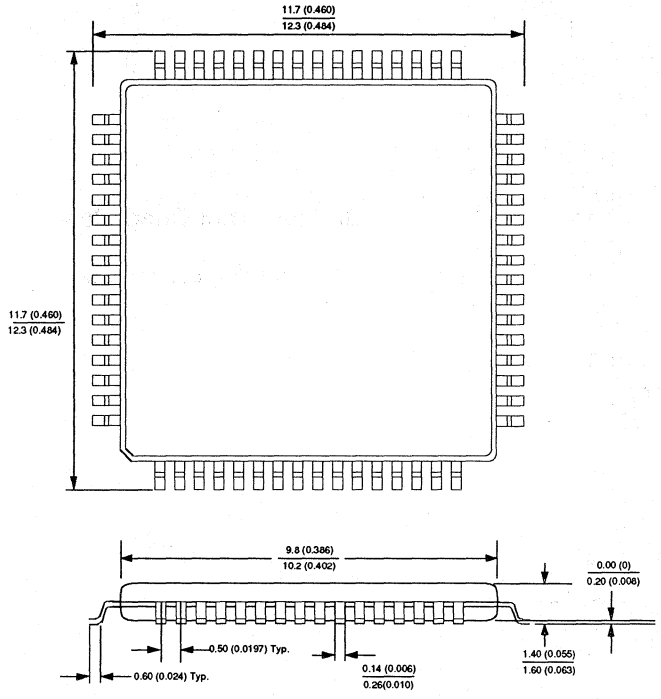


48-Lead Thin Quad Flatpack

NOTE: Controlling dimensions are in mm

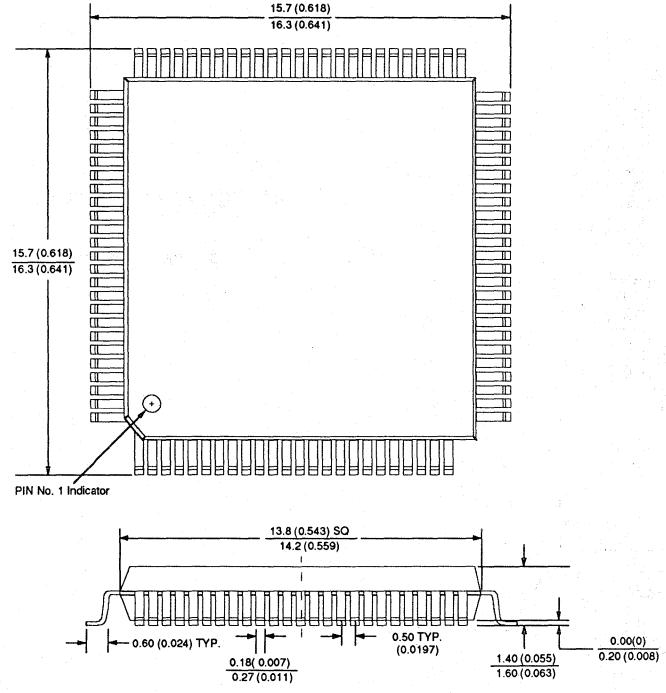
11

Package Information



64-Lead Thin Quad Flatpack

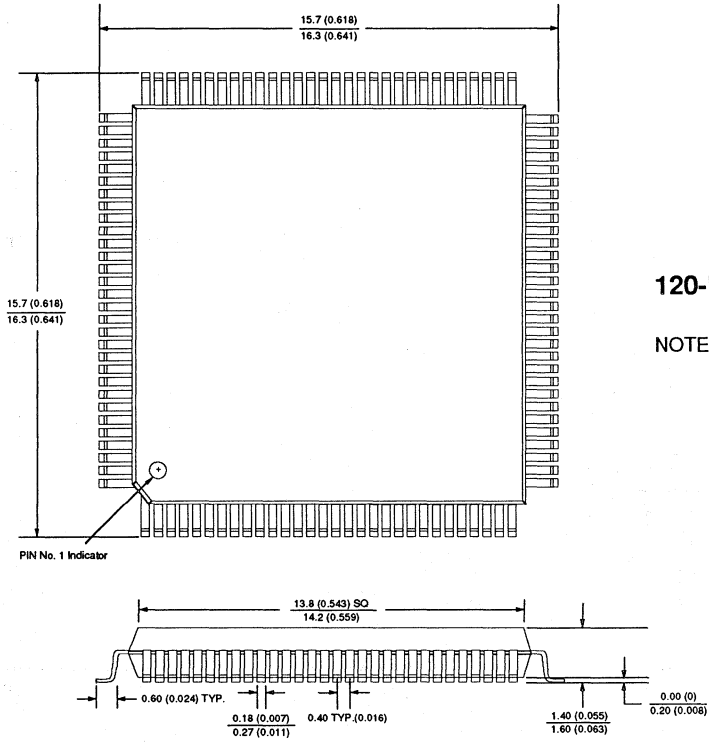
NOTE: Controlling dimensions are in mm



100-Lead Thin Quad Flatpack

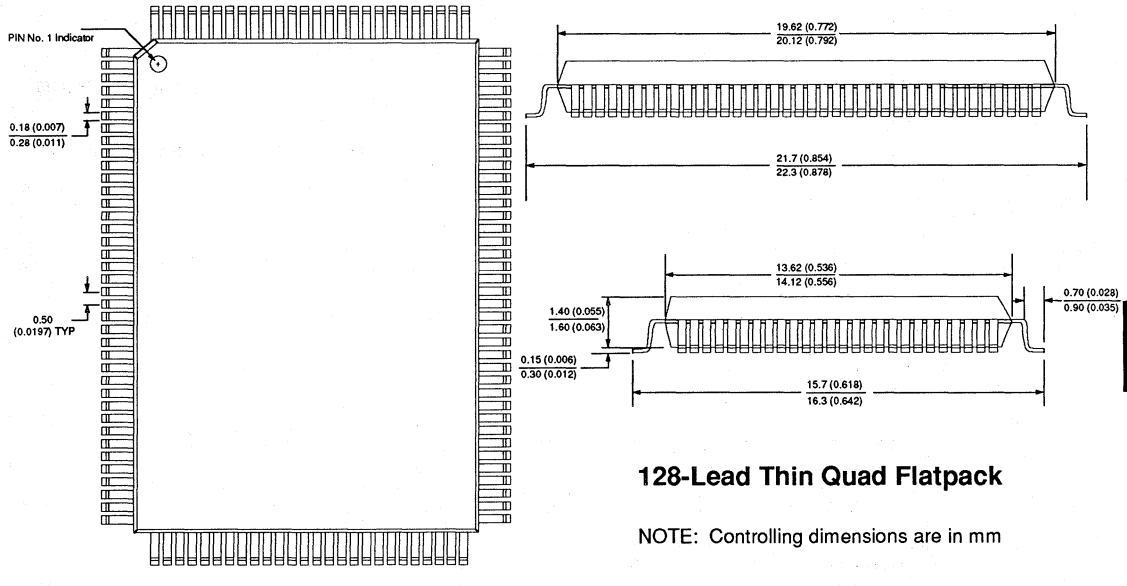
NOTE: Controlling dimensions are in mm

Package Information



120-Lead Thin Quad Flatpack

NOTE: Controlling dimensions are in mm

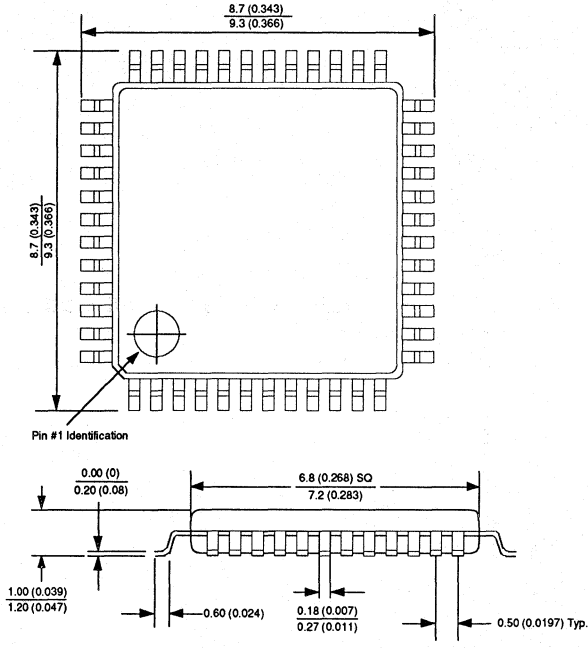


128-Lead Thin Quad Flatpack

NOTE: Controlling dimensions are in mm

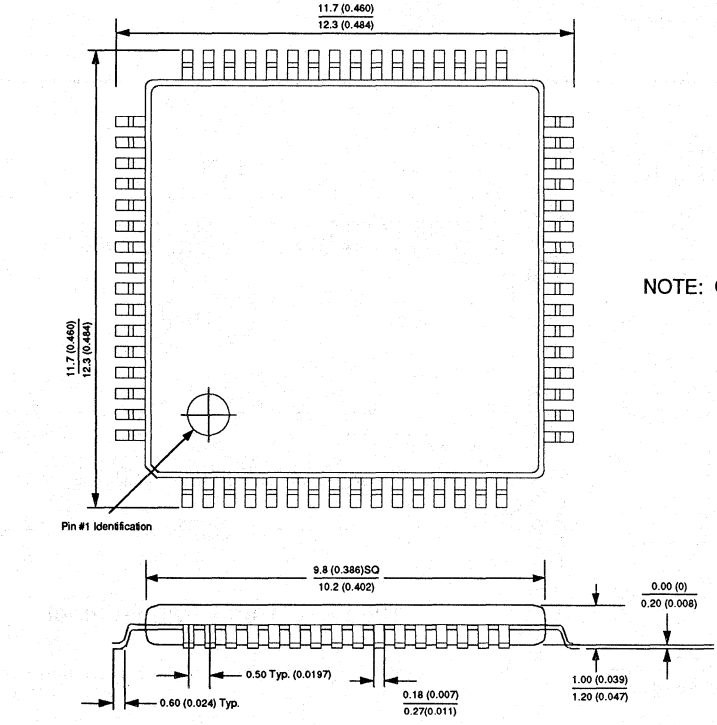
11

Package Information Very Thin Quad Flatpack (VTQFP)



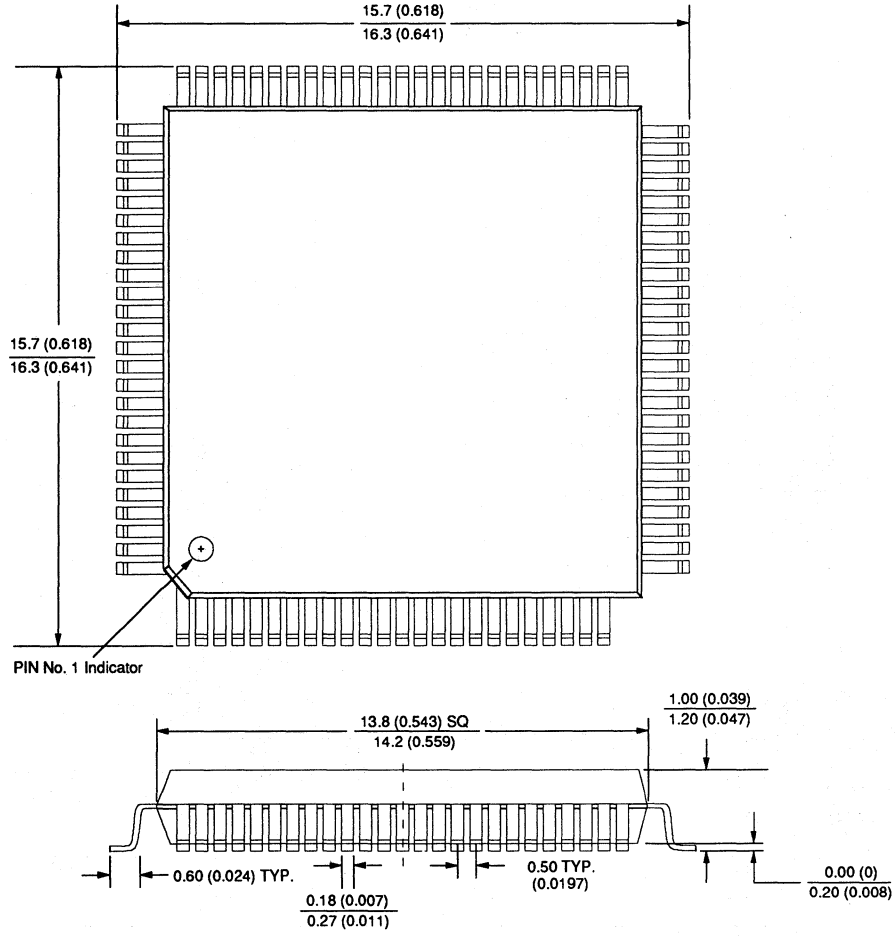
48-Lead VTQFP

NOTE: Controlling dimensions are in mm



64-Lead VTQFP

NOTE: Controlling dimensions are in mm

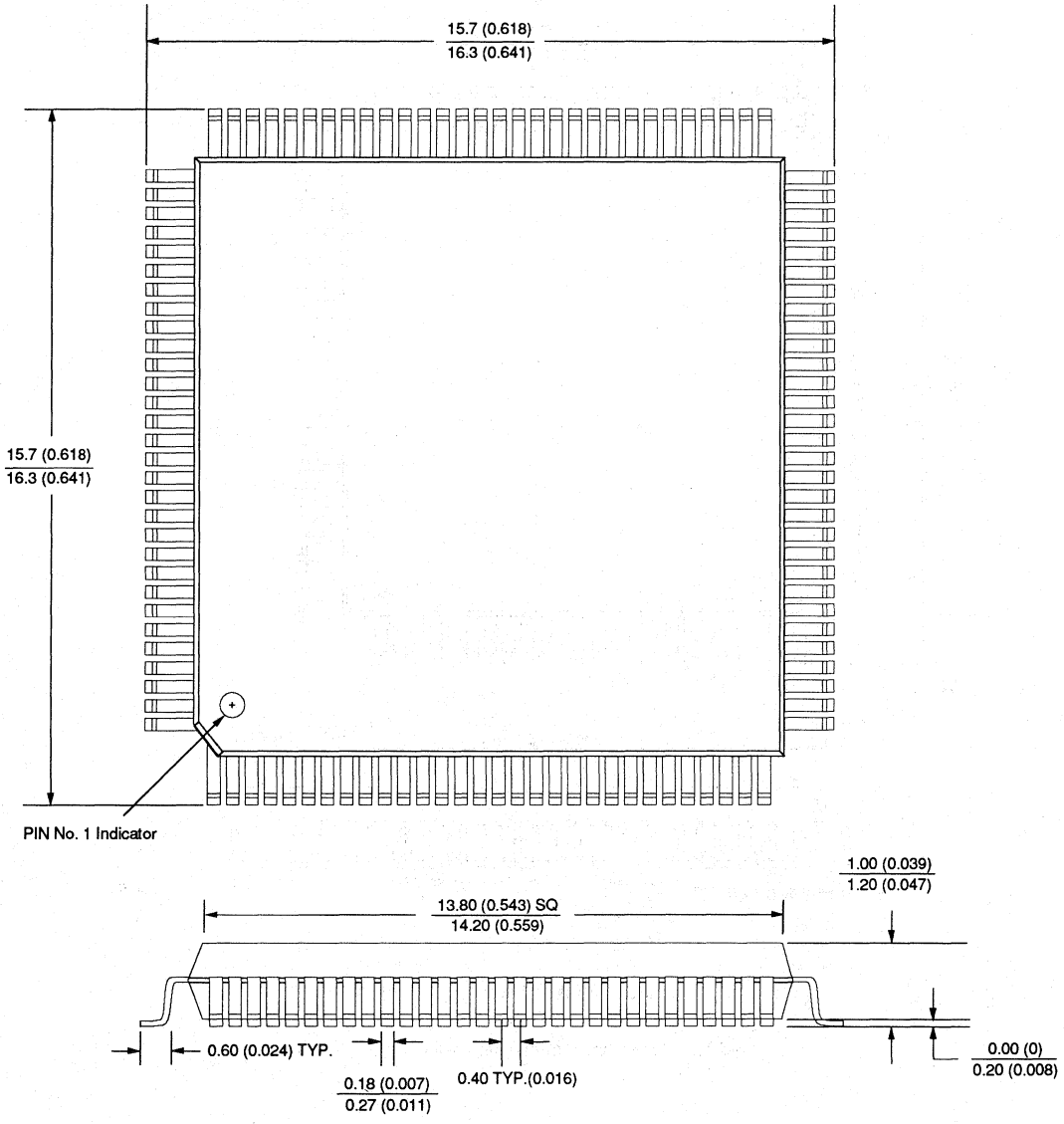


100-Lead VTQFP

NOTE: Controlling dimensions are in mm

11

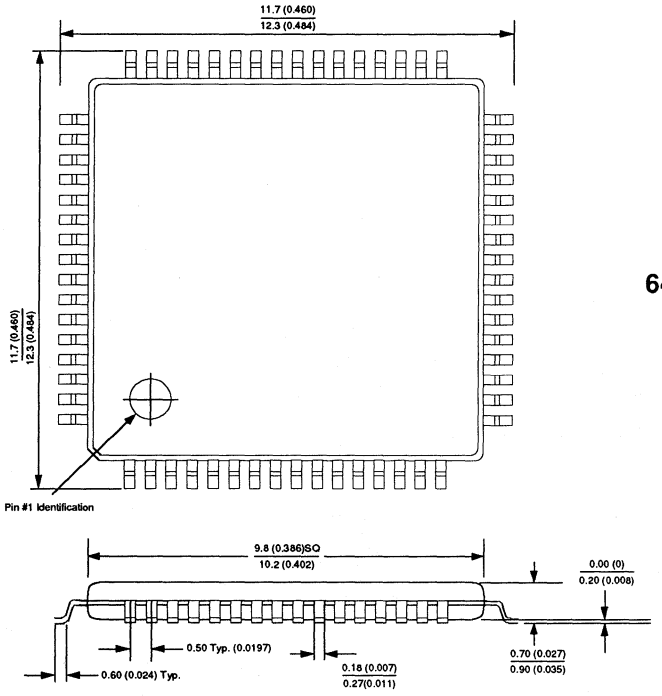
Package Information



120-Lead VTQFP

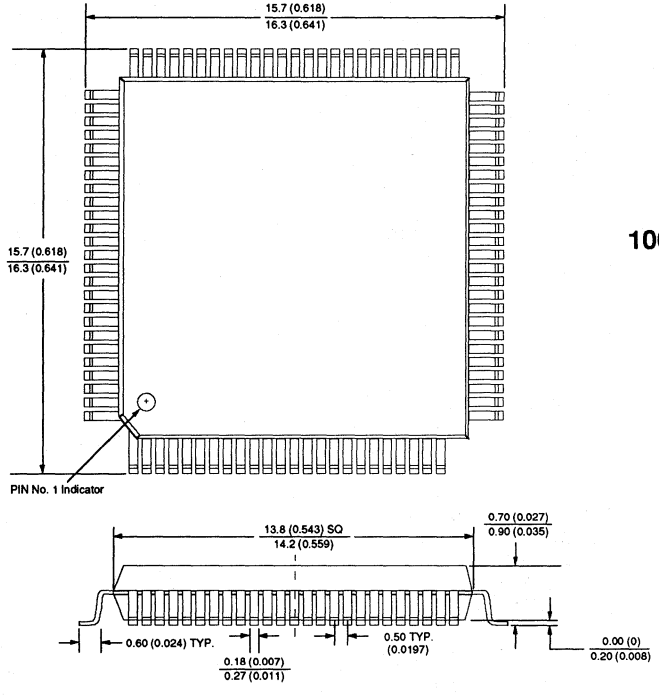
NOTE: Controlling dimensions are in mm

Package Information Ultra Thin Quad Flatpack (UTQFP)



64-Lead Ultra Thin Quad Flatpack

NOTE: Controlling dimensions are in mm

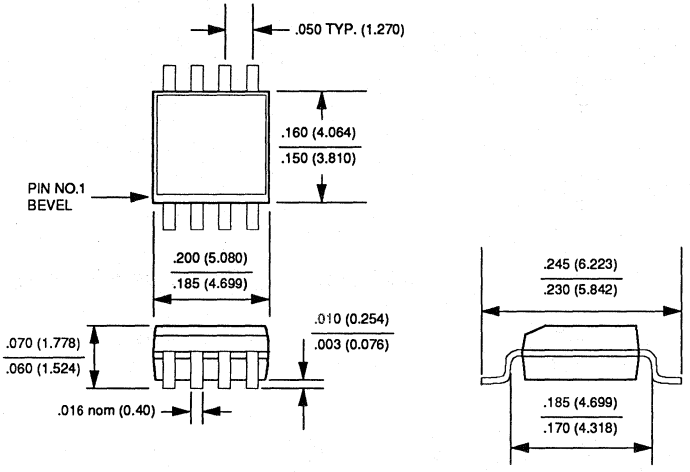


100-Lead Ultra Thin Quad Flatpack

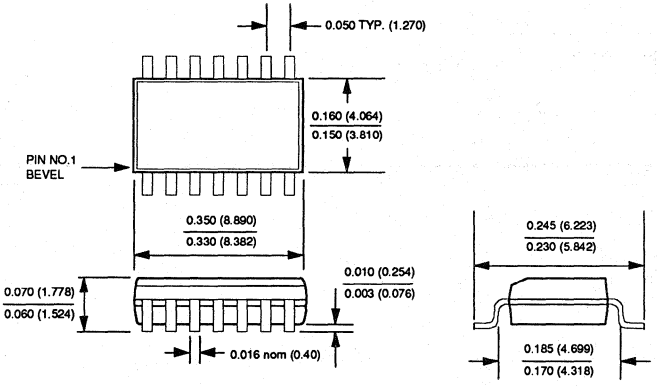
NOTE: Controlling dimensions are in mm

11

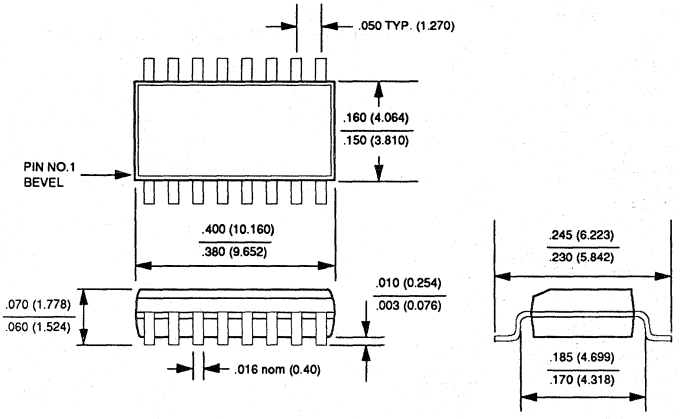
8-Lead SON

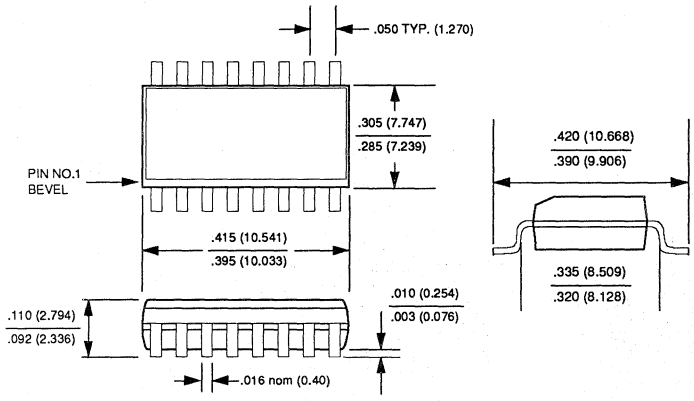


14-Lead SON

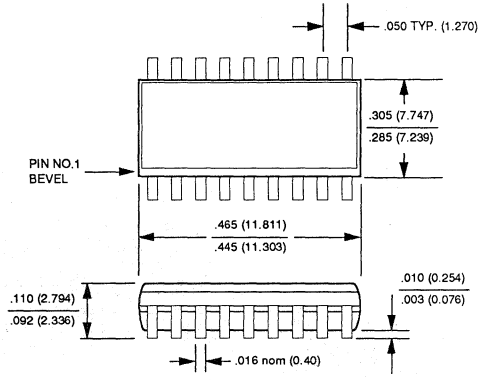


16-Lead SON

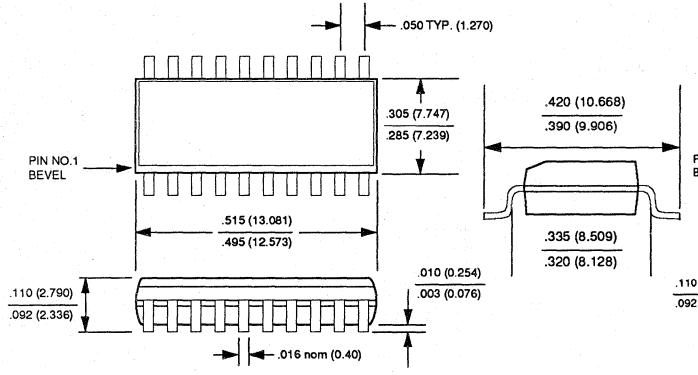




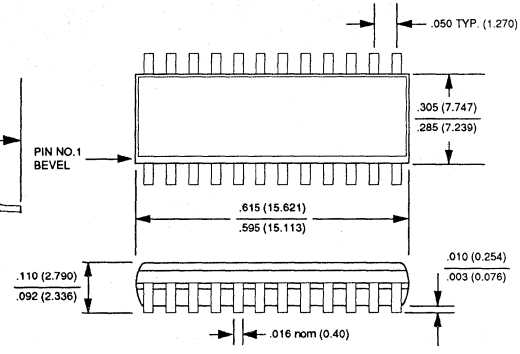
16-Lead SOL



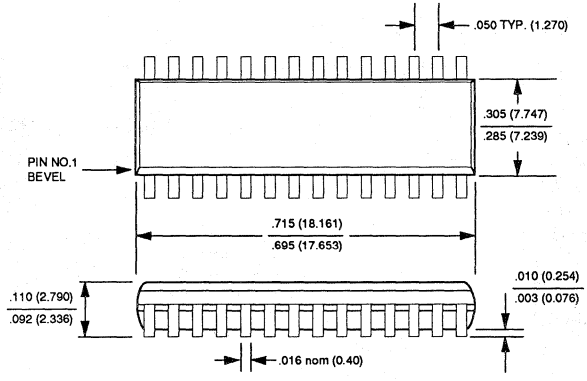
18-Lead SOL



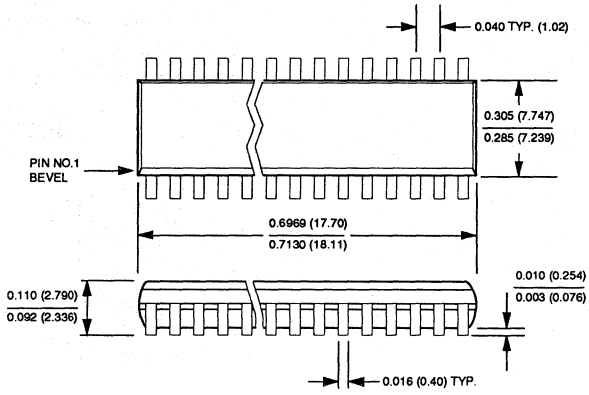
20-Lead SOL



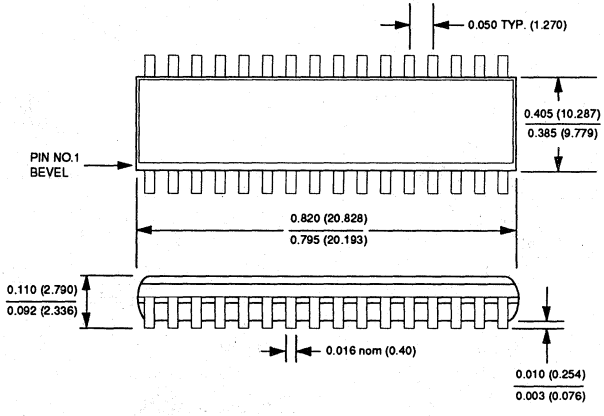
24-Lead SOL



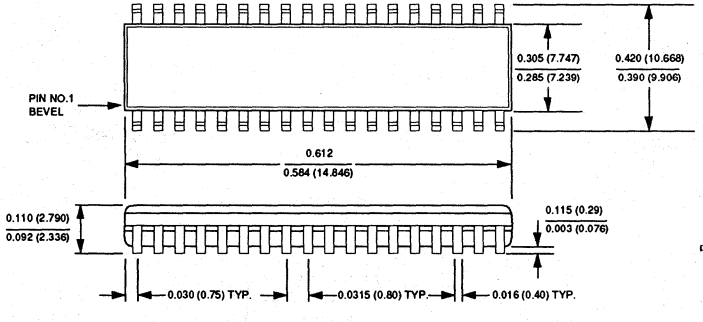
28-Lead SOL



34-Lead SOL

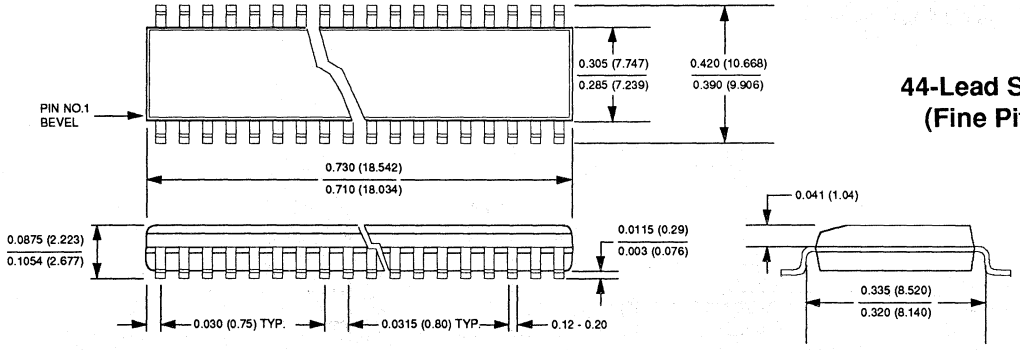


32-Lead SOW



36-Lead SOM (Fine Pitch)

Package Information

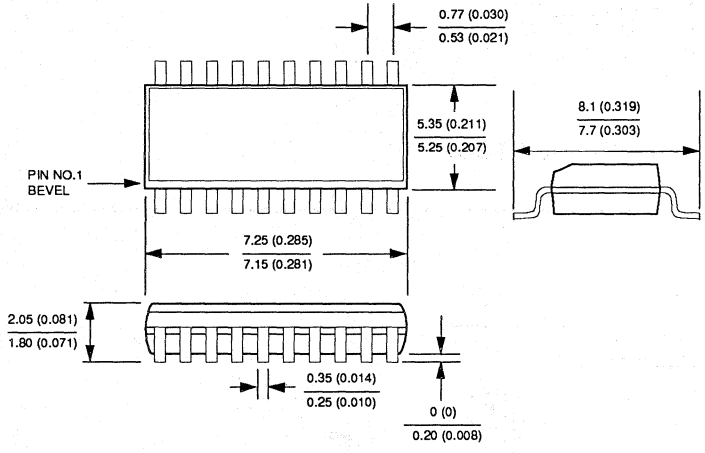


44-Lead SOM (Fine Pitch)

Package Information

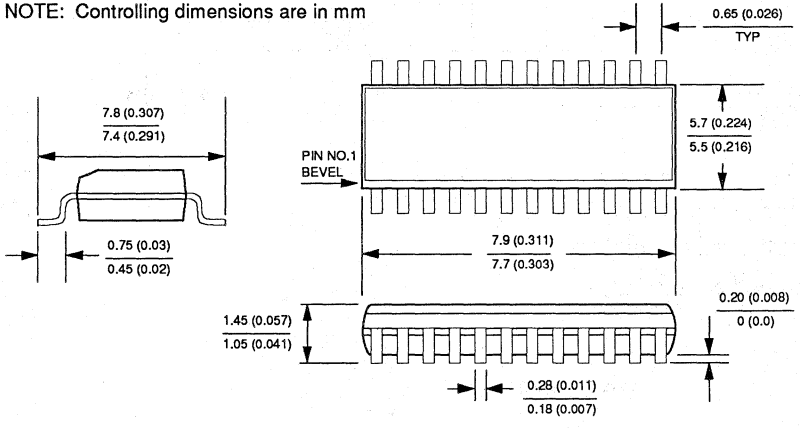
VSOP

NOTE: Controlling dimensions are in mm



20-Lead VSOP

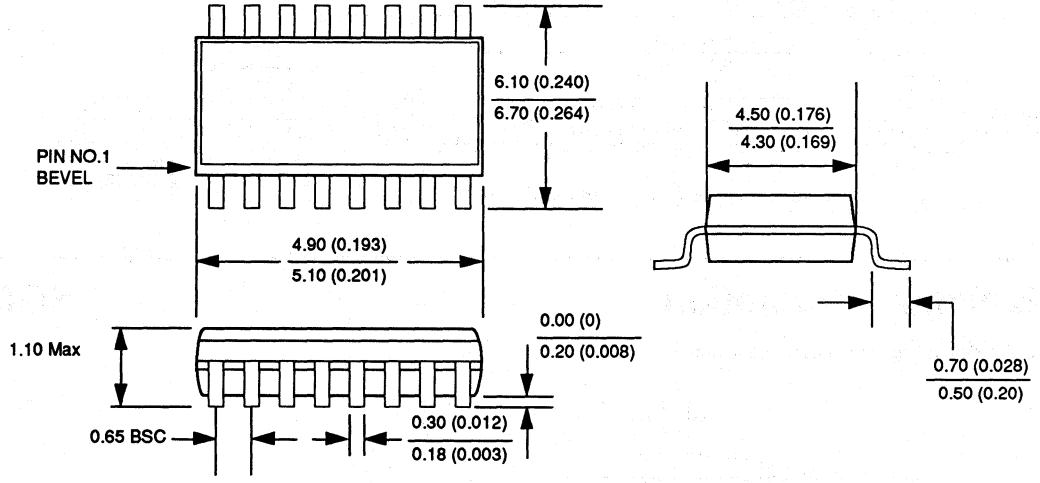
NOTE: Controlling dimensions are in mm



24-Lead VSOP

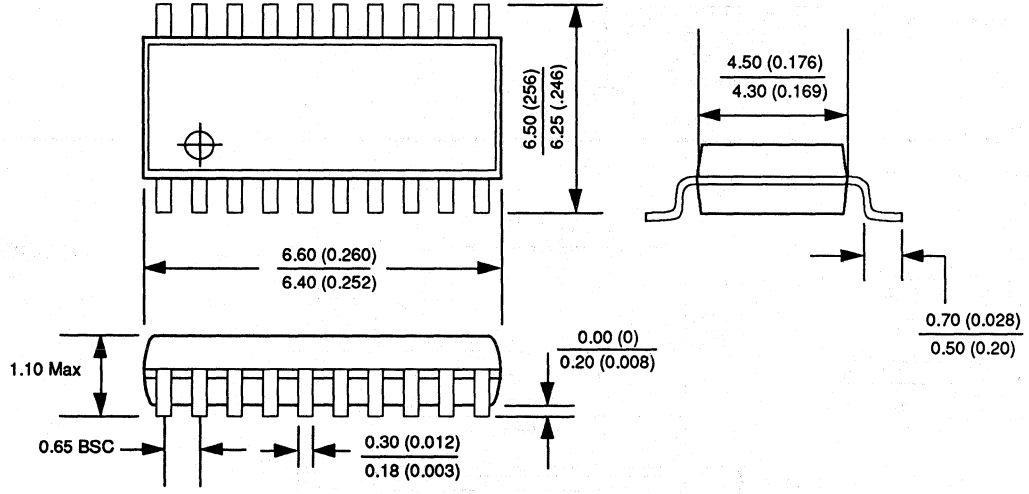
11

NOTE: Controlling dimensions are in mm



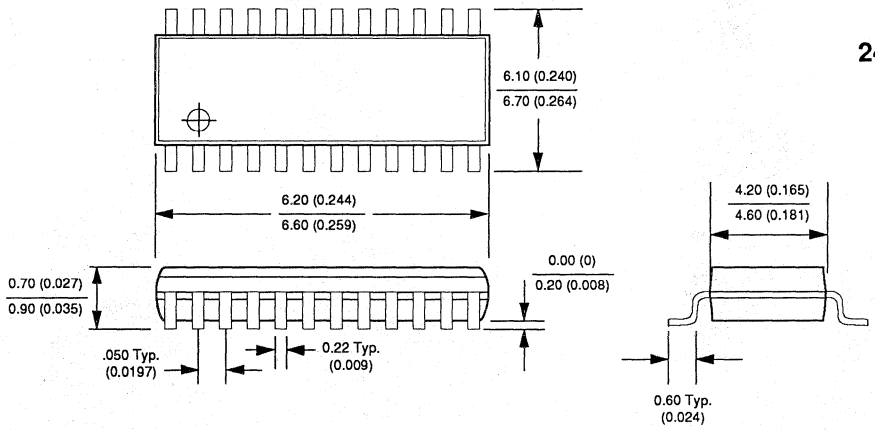
16-Lead VTSOP

NOTE: Controlling dimensions are in mm

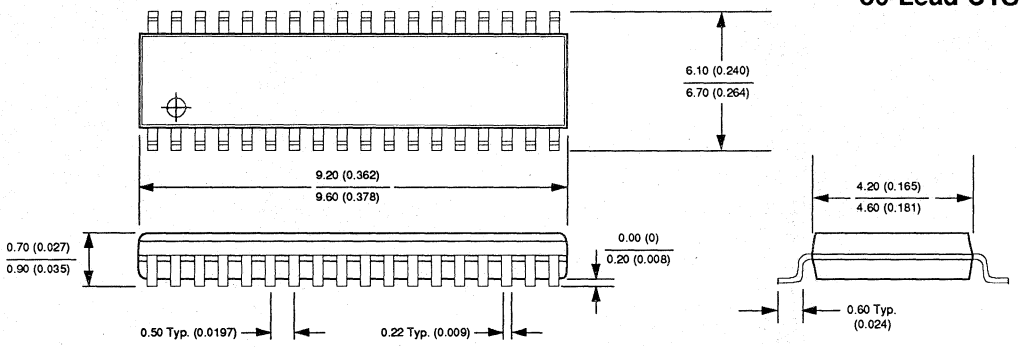


20-Lead VTSOP

24-Lead UTSOP



36-Lead UTSOP



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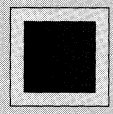
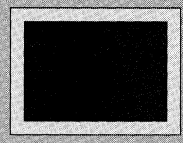
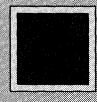
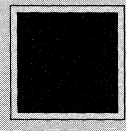
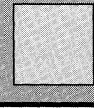
Small Form Factor Package Selector Guide

Quad Flatpack Packages

PACKAGE TYPE	ACTUAL SIZE (AREA)	BODY SIZE (PITCH) mm	LAYOUT AREA mm^2	ACTUAL SIZE (THICKNESS)	THICKNESS mm
52 G (QFP)		10.0 x 10.0 (0.65)	13.9 x 13.9 = 193.21		2.2
100 G (QFP)		20.0 x 14.0 (0.65)	23.9 x 17.9 = 427.81		2.9
128 G (QFP)		20.0 x 14.0 (0.5)	23.2 x 17.2 = 399.04		2.9
32 GT (TQFP)		7.0 x 7.0 (0.8)	9.0 x 9.0 = 81		1.4
48 GT (TQFP)		7.0 x 7.0 (0.5)	9.0 x 9.0 = 81		1.4
64 GT (TQFP)		10.0 x 10.0 (0.5)	12.0 x 12.0 = 144		1.4
100 GT (TQFP)		14.0 x 14.0 (0.5)	16 x 16 = 256		1.4

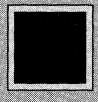
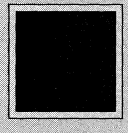
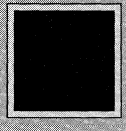
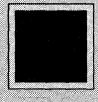
 = Actual Body Size

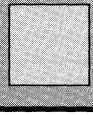
 = Full Layout Area

All dimensions are nominal values.

Small Form Factor Package Selector Guide

Quad Flatpack Packages

PACKAGE TYPE	ACTUAL SIZE (AREA)	BODY SIZE (PITCH) mm	LAYOUT AREA mm^2	ACTUAL SIZE (THICKNESS)	THICKNESS mm
120 GT (TQFP)		14.0 x 14.0 (0.4)	16.0 x 16.0 = 256		1.4
128 GT (TQFP)		20.0 x 14.0 (0.5)	22.0 x 16.0 = 352		1.4
48 GV (VTQFP)		7.0 x 7.0 (0.5)	9.0 x 9.0 = 81		1.0
64 GV (VTQFP)		10.0 x 10.0 (0.5)	12.0 x 12.0 = 144		1.0
100 GV (VTQFP)		14.0 x 14.0 (0.5)	16.0 x 16.0 = 256		1.0
120 GV (VTQFP)		14.0 x 14.0 (0.4)	16.0 x 16.0 = 256		1.0
64 GU (UTQFP)		10.0 x 10.0 (0.5)	12.0 x 12.0 = 144		0.7

 = Actual Body Size  = Full Layout Area All dimensions are nominal values.

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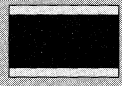
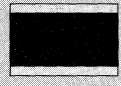
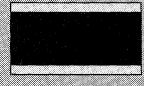
silicon systems® A TDK Group Company

Small Form Factor Package Selector Guide

Small Outline Packages

PACKAGE TYPE	ACTUAL SIZE (AREA)	BODY SIZE (PITCH) mm	LAYOUT AREA mm^2	ACTUAL SIZE (THICKNESS)	THICKNESS mm
16 SON		9.8 x 3.9 (1.27)	9.8 x 6.0 = 58.8		1.65
16 SOL		10.2 x 7.5 (1.27)	10.2 x 10.2 = 104		2.54
20 SOL		12.8 x 7.5 (1.27)	12.8 x 10.2 = 130.6		2.54
24 SOL		15.4 x 7.5 (1.27)	15.4 x 10.2 = 157		2.54
20 SOV (VSOP)		7.2 x 5.4 (0.65)	7.9 x 7.2 = 56.9		1.9
24 SOV (VSOP)		7.8 x 5.6 (0.65)	7.8 x 7.6 = 59.28		1.15
36 SOM (SSOP)		15.1 x 7.5 (0.8)	15.1 x 10.2 = 154		2.54
44 SOM (SSOP)		18.3 x 7.5 (0.8)	18.3 x 10.2 = 186.7		2.54
16 VT (VTSOP)		5.0 x 4.4 (0.65)	6.4 x 5.0 = 32		0.9
20 VT (VTSOP)		6.5 x 4.4 (0.65)	6.5 x 6.4 = 41.6		0.9

 = Actual Body Size

 = Full Layout Area

All dimensions are nominal values.

Section 12

SALES OFFICES/ DISTRIBUTORS

United States
Regional Offices & Sales Representatives

NORTHWEST

HEADQUARTERS
Jon Tammel, Area Director
Silicon Systems, Inc.
2001 Gateway Place
Suite 301 East
San Jose, CA 95110
Ph: (408) 432-7100
FAX: (408) 453-5988

CALIFORNIA
Magna Sales

Santa Clara
Ph: (408) 727-8753
FAX: (408) 727-8573

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FAX: (208) 376-8706

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Ph: (509) 922-7600
FAX: (509) 922-7603

SOUTHWESTERN

HEADQUARTERS
Larry Cleland, Area Manager
Silicon Systems, Inc.
3445 Penrose Place, Suite 140
Boulder, CO 80301
Ph: (303) 440-9780
FAX: (303) 440-9783
Tustin Office
Ph: (714) 832-5310
FAX: (714) 832-5247

ARIZONA
Western High Tech Marketing, Inc.

Scottsdale
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FAX: (602) 860-2712

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EASTERN

HEADQUARTERS
Wayne Taylor, Area Manager
Silicon Systems, Inc.
53 Stiles Road
Salem, NH 03079
Ph: (603) 898-1444
FAX: (603) 898-9538

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108 E. Grand River, Suite 6
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Melville
Ph: (516) 351-8833
FAX: (516) 351-8667

NO. CAROLINA
Technology Mktg. Assoc. (TMA)

Raleigh
Ph: (919) 872-5104
FAX: (919) 872-5086

OHIO
Makin Associates

Cincinnati
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Section 13

APPLICATION NOTES

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SSI 32F8001
Programmable Electronic Filter

Application Note

November 1993

INTRODUCTION

Analog filtering is a universal requirement in any signal processing system. Filter design is now made easy with the programmable filters from Silicon Systems Inc. Whether the requirement is a fixed filtering characteristic or a programmable response, this family of programmable filters offers distinct advantages of design simplicity, accuracy, versatility and board space saving. Additional features, such as high frequency boost, differentiated outputs, are also available. This application note focuses on the SSI 32F8001, cutoff frequency programmable from 9-27 MHz.

The objectives of this application note are:

- To present a description of the SSI 32F8001
- To discuss its applications
- To present a typical fixed response design
- To present a programmable response application

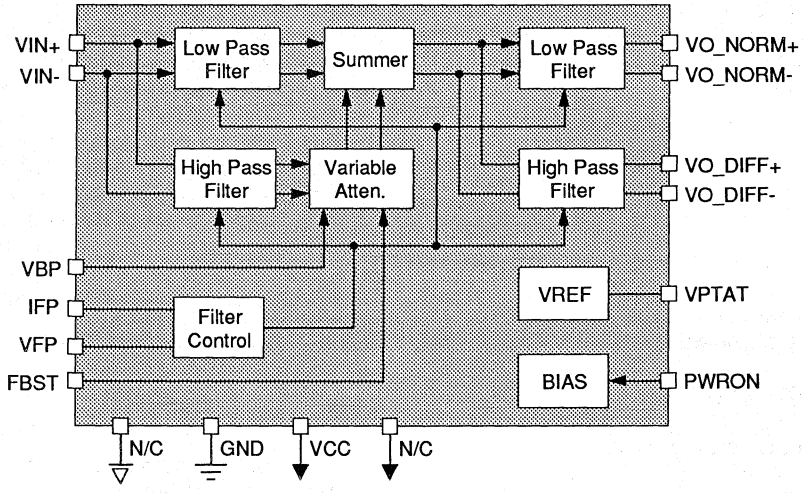

FIGURE 1: Block Diagram

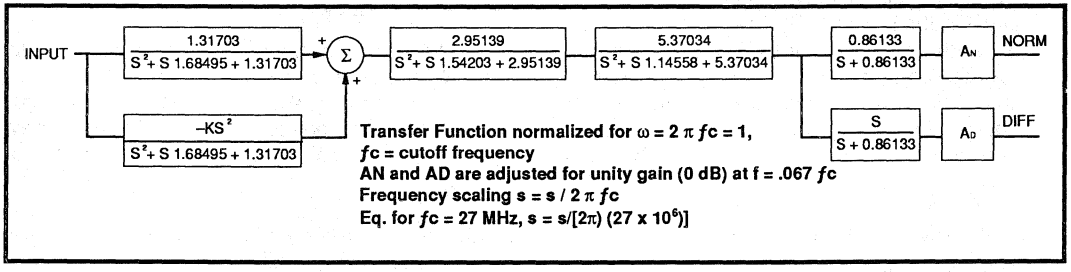

FIGURE 2: The SSI 32F8001 Transfer Function

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SSI 32F8001
Programmable Electronic Filter

1.0 DESCRIPTION

The SSI 32F8001 is a programmable 7-pole 0.05° equiripple linear phase low pass filter in a silicon bipolar integrated circuit. Figures 1 and 2 show the block diagram and the filter transfer function.

The SSI 32F8001 cutoff frequency and high frequency boost can be independently controlled by two control signals. Two sets of filter outputs are available: normal low pass output and differentiated low pass output. As an equiripple linear phase type filter, the filter outputs exhibit constant group delay in the pass band and out to 1.75 fc. Furthermore, the delays through the normal output and the differentiated output are well matched.

The input and outputs of the SSI 32F8001 are differential signals, requiring external AC coupling capacitors. The given transfer function shows the relationship between the input and the two sets of outputs. Typical differential input resistance is 4 kΩ.

1.1 CUTOFF FREQUENCY PROGRAMMING

The cutoff frequency, defined to be the -3dB corner frequency with no boost, can be programmed between 9 - 27 MHz. It can be set by one of three methods:

- A resistor can be inserted between the VPTAT and the VFP pins. This setting is only used for a fixed response design. The IFP pin should be left open. The design equation for this resistor value is:

  Rx (kΩ) = 27 / fc (MHz)

  A design example is given in Section 4.

- A current source input can be fed into the IFP pin. The VFP pin should be left open. A current source digital-to-analog converter (DAC), such as the DACF in the SSI 32D4661 Time Base Generator, allows a microcontroller to change the filter response dynamically. To achieve the highest accuracy the current source DAC should be referenced to the reference voltage at the VPTAT pin. The design equation for this current source value is:

  IFP (mA) = 0.0222 x fc (MHz)

  A design example is given in Section 4.

- A current sink input can be fed into the IFP pin. A 1 kΩ resistor should be placed across the VPTAT and the VFP pins. With a current sink DAC, this design also allows a microcontroller to change the filter response dynamically. To achieve the highest accuracy and temperature stability, the current sink DAC should be referenced to the reference voltage at the VPTAT pin. The design equation for this current sink value is:

  IFP (mA) = 0.0222 x (27 - fc) (MHz)

  A design example is given in Section 4.

1.2 HIGH FREQUENCY BOOST CONTROL

The high frequency boost function is especially desirable for pulse slimming and magnitude equalization applications. This function can be enabled or disabled by a TTL logic input at the FBST pin. With FBST = TTL logic high or open, the amount of high frequency boost, measured at the cutoff frequency, can be programmed from 0 to 13.5 dB at fc by a voltage input at the VBP pin. External resistors can be designed in for a fixed filter response. For a programmable high frequency boost, a voltage DAC, such as the DACS in the SSI 32D4661 Time Base Generator, can be used to control the VBP pin. This input voltage should be made proportional to the reference voltage at the VPTAT pin for accuracy. The design equation for this control voltage is:

VBP = VPTAT x (10^(FB/20) - 1) / 3.46 where FB is in dB.

Design example is given in Section 3.

With a finite boost, the magnitude response peaks at a frequency slightly higher than the original cutoff frequency. The effective pass band bandwidth is wider.

1.3 OTHER FEATURES OF THE SSI 32F8001

The SSI 32F8001 features excellent constant group delay. At fc = 27 MHz, the group delay variation from 0.2 fc to fc is less than 0.5 ns. Furthermore, the high frequency boost function does not affect the group delay variation. Group delay variation is within ±4% out to 1.75 fc.

In addition to the normal low pass output, the SSI 32F8001 also provides a differentiated low pass output of the input signal. The signal delay is well matched to the normal output.

The SSI 32F8001 provides a reference voltage VPTAT for the DAC references. Because the internal filter control circuitry is referenced to VPTAT, the control current for filter cutoff frequency and control voltage for high frequency boost should be referenced to VPTAT.

The SSI 32F8001 can be switched into a sleep mode, dissipating less than 2.5 mW, by a TTL input at PWRON.

Two package options are available for the SSI 32F8001: 16-lead SOL and 16-lead SON. The small feature size of the 16-lead SON package offers significant board space saving.

2.0 APPLICATIONS

A programmable filter is a versatile component in any signal processing system. Some areas of applications include fixed response filtering, variable data rate processing and adaptive equalization.

For fixed response filtering applications, the SSI 32F8001 offers a simple-to-use solution. The once complex design of cutoff frequency or magnitude equalization is now rendered to simple resistance calculation. The narrow 16-pin small outline package offers significant board space economy.

In variable data rate processing, a programmable filter can be used to optimize bandwidth and signal-to-noise tradeoff. One application is constant density recording for high capacity storage products. As the data rate increases from the inner tracks to the outer tracks, the filter cutoff frequency can be scaled accordingly to maximize the signal-to-noise performance. The high frequency boost function provides pulse slimming for accurate pulse detection.

A programmable filter offers a revolutionary approach to adaptive equalization. In signal transmission applications, an equalization filter is used to combat channel distortion. The magnitude of channel distortion is often not known a priori. Adaptive equalization can dynamically shape the equalization function. With an appropriate external adaptive sensing function, the cutoff frequency and the high frequency boost of the SSI 32F8001 can be dynamically programmed through microprocessor control.

3.0 FIXED RESPONSE DESIGN PROCEDURE

This section suggests some design guidelines to apply the SSI 32F8001 as a fixed response filter. Figure 3 shows the design schematic. Rx determines the filter's cutoff frequency, defined as the -3 dB frequency with no boost. The ratio of RB1 and RB2 determines the amount of high frequency boost.

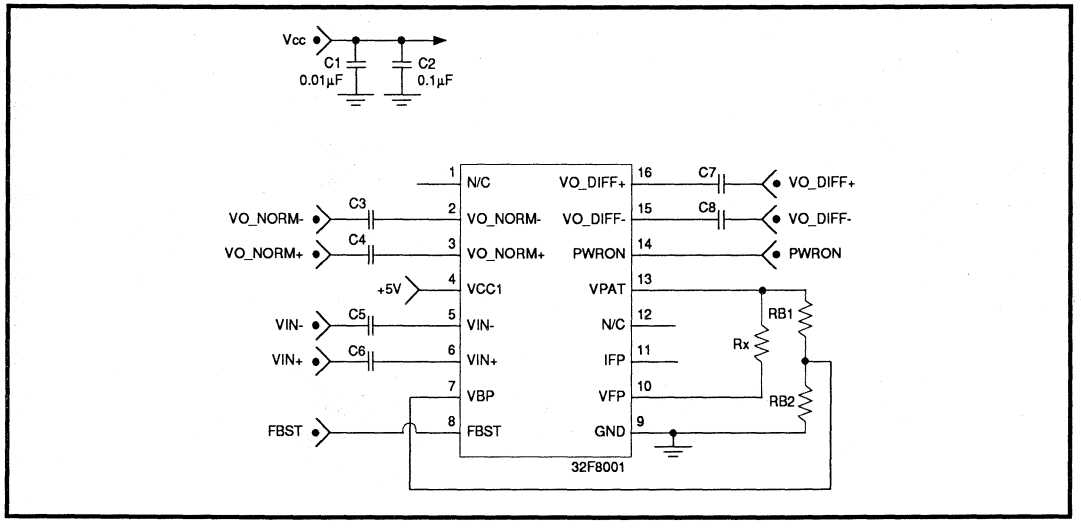

FIGURE 3: The 32F8001 Setup as a Fixed Response Filter

3.0 FIXED RESPONSE DESIGN PROCEDURE (continued)

Given fc, cutoff frequency in MHz, and FB, high frequency boost in dB:

- Rx can be calculated, as given in Section 1.
  Rx (kΩ) = 27 / fc (MHz)
  Voltage across Rx is 0.33 VPTAT. The current through Rx is 0.33 (VPTAT / Rx).
  Rx should be between 1 kΩ to 3 kΩ, i.e., fc between 9 MHz to 27 MHz.
- RB1/RB2 sets FB, and can be determined as follows:
  RB1 / RB2 = 3.46 / (10^(FB / 20) - 1) - 1
- Total current drawn out of the VPTAT pin should be limited to 2 mA max. Thus, RB1 and RB2 should be designed accordingly.
- The IFP pin should be left open.

4.0 PROGRAMMABLE RESPONSE DESIGN PROCEDURE

This section suggests some design guidelines to apply the SSI 32F8001 as a programmable filter. The high frequency boost can be controlled by a voltage DAC driving the VBP pin. The VBP voltage should be between 0 and VPTAT. The cutoff frequency can be controlled by a current DAC. The application setup for using a current source DAC is different from the one using a current sink DAC. Both are presented below.

4.1 PROGRAMMABLE FILTER USING A CURRENT SOURCE DAC

Figure 4 shows the setup schematic of the SSI 32F8001 using an external current source DAC to control the filter's cutoff frequency.

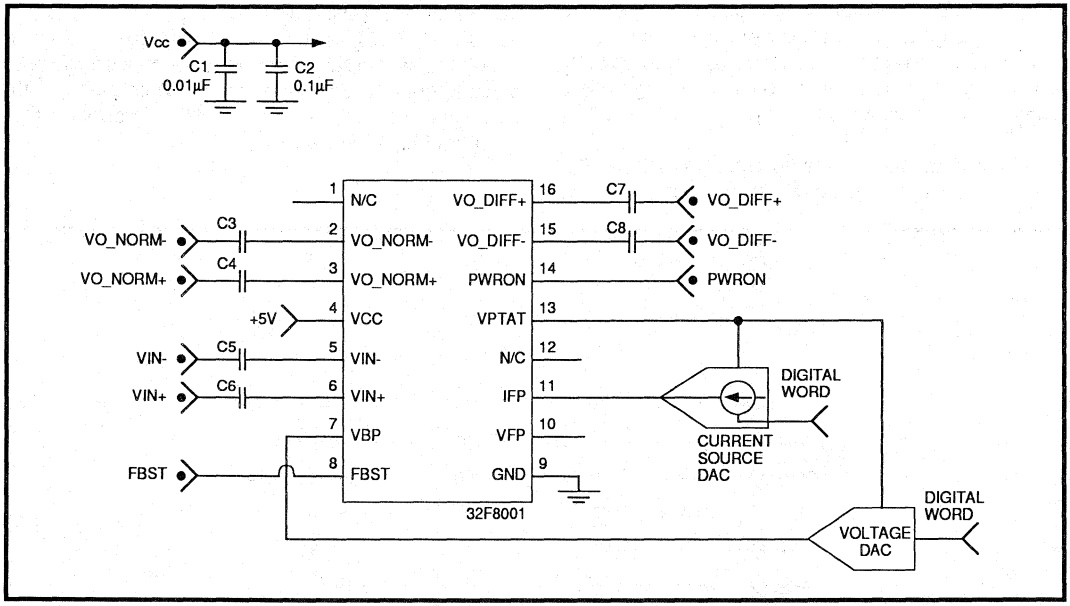

FIGURE 4: The SSI 32F8001 Setup Schematic Using a Current Source DAC for Cutoff Frequency Control

Design guidelines for the SSI 32F8001:

- The VFP pin should be left open.
- Both the current source DAC and the voltage DAC should reference to VPTAT for accuracy.
- The reference bias current drawn from VR should be less than 2 mA.
- The IFP current and the filter cutoff frequency are related as follows:

  $fc\ (MHz) = 45 \times IFP\ (mA) \times \frac{1.8}{VPTAT}$

  IFP should be between 0.2 mA to 0.6 mA with VPTAT = 1.8V (at room temperature).
- The VBP voltage and the high frequency boost are related as follows:

  FB = 20 x log (3.46 x VBP / VPTAT + 1) dB

4.2 PROGRAMMABLE FILTER USING CURRENT SINK DAC

Figure 5 shows the setup schematic of the SSI 32F8001 using an external current sink DAC to control the filter's cutoff frequency. The high frequency boost control is the same as in Section 4.1.

Some design guidelines:

- Rx should be set to 1 kΩ between VPTAT and VFP.
- Both the current source DAC and the voltage DAC should reference to VPTAT for accuracy and temperature stability.
- The total current drawn from VPTAT should be less than 2mA. This includes the 0.6mA through Rx. Thus, the current sink DAC and the voltage DAC reference should not draw more than 1.4 mA.
- The IFP current and the cutoff frequency are related as follows:

  $fc\ (MHz) = 27 - 45 \times IFP\ (mA) \times \frac{VPTAT}{1.8}$

  IFP should be between 0 mA to 0.4 mA.

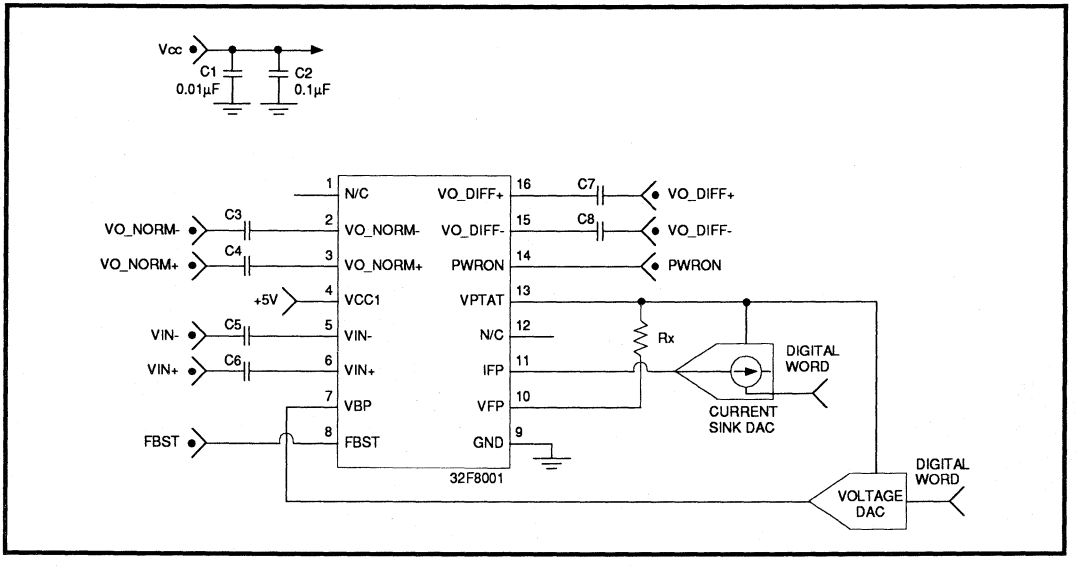

FIGURE 5: The SSI 32F8001 Setup Schematic Using a Current Sink DAC for Cutoff Frequency Control

Notes:

SSI 32F8011
Programmable Electronic Filter

Application Note

November 1993

INTRODUCTION

Analog filtering is a universal requirement in any signal processing system. Filter design is now made easy with the programmable filters from Silicon Systems Inc. Whether the requirement is a fixed filtering characteristic or a programmable response, this family of programmable filters offers distinct advantages of design simplicity, accuracy, versatility and board space saving. Additional features, such as high frequency boost, differentiated outputs, are also available. This application note focuses on the SSI 32F8011, cutoff frequency programmable from 5 - 13 MHz.

The objectives of this application note are:

- To present a description of the SSI 32F8011
- To discuss its applications
- To present a typical fixed response design
- To present a programmable response application

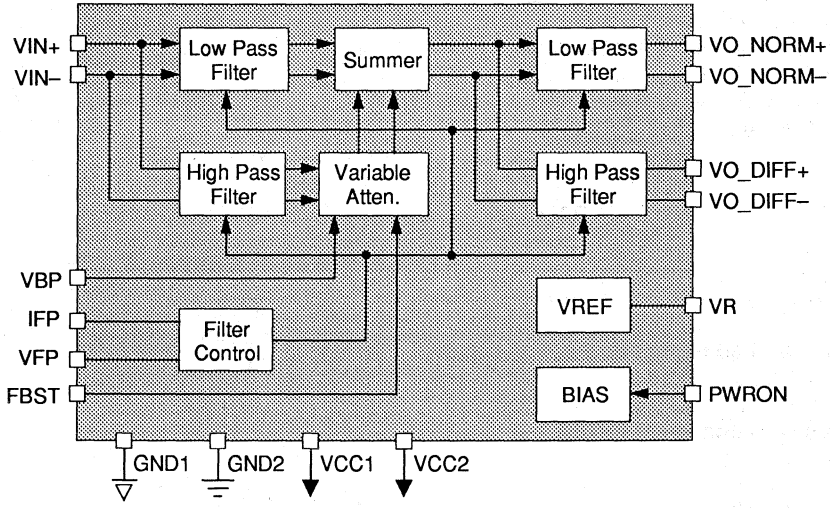

FIGURE 1: Block Diagram

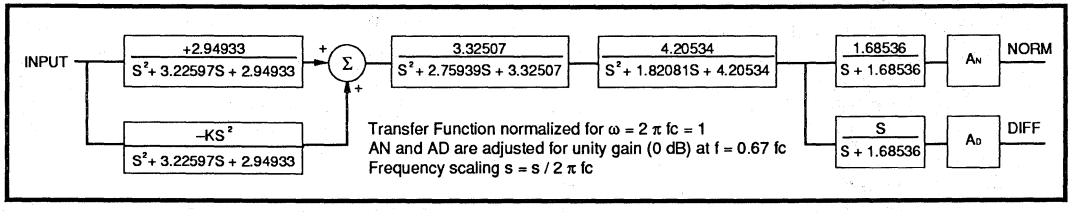

FIGURE 2: The SSI 32F8011 Transfer Function

SSI 32F8011
Programmable Electronic Filter

Application Note

1.0 DESCRIPTION

The SSI 32F8011 is a programmable 7-pole Bessel low pass filter in a silicon bipolar integrated circuit. Figures 1 and 2 show the block diagram and the filter transfer function.

The SSI 32F8011 cutoff frequency and high frequency boost can be independently controlled by two control signals. Two sets of filter outputs are available: normal low pass output and differentiated low pass output. As a Bessel type filter, the filter outputs exhibit constant group delay in the pass band. Furthermore, the delays through the normal output and the differentiated output are well matched.

The input and outputs of the SSI 32F8011 are differential signals, requiring external AC coupling capacitors. The given transfer function shows the relationship between the input and the two sets of outputs. The maximum input signal is 1.5 Vpp differential, with differential input resistance 4 kΩ typical. The minimum recommended output load is 1 kΩ differential, AC coupled.

1.1 CUTOFF FREQUENCY PROGRAMMING

The cutoff frequency, defined to be the -3 dB corner frequency with no boost, can be programmed between 5 - 13 MHz. It can be set by one of three methods:

- A resistor can be inserted between the VR and the VFP pins. This setting is only used for a fixed response design. The IFP pin should be left open. The design equation for this resistor value is:

  Rx (kΩ) = 11.92 / fc (MHz)

  A design example is given in Section 4.

- A current source input can be fed into the IFP pin. The VFP pin should be left open. With a current source digital-to-analog converter (DAC), such as the DACF in the SSI 32D4661, this design allows a microcontroller to change the filter response dynamically. To achieve the highest accuracy and temperature stability, the current source DAC should be referenced to the temperature compensated reference voltage at the VR pin. The design equation for this current source value is:

  IFP (mA) = 0.0615 x fc (MHz)

  A design example is given in Section 4.

- A current sink input can be fed into the IFP pin. A 917Ω resistor should be placed across the VR and the VFP pins. With a current sink DAC, this design also allows a microcontroller to change the filter response dynamically. To achieve the highest accuracy and temperature stability, the current sink DAC should be referenced to the temperature compensated reference voltage at the VR pin. The design equation for this current sink value is:

  IFP (mA) = 0.0615 x (13 - fc) (MHz)

  A design example is given in Section 4.

1.2 HIGH FREQUENCY BOOST CONTROL

The high frequency boost function is especially desirable for pulse slimming and magnitude equalization applications. This function can be enabled or disabled by a TTL logic input at the FBST pin. With FBST = '1' or open, the amount of high frequency boost, measured at the cutoff frequency, can be programmed from 0 to 9 dB at fc by a voltage input at the VBP pin. External resistors can be designed in for a fixed filter response. For a programmable high frequency boost, a voltage DAC, such as the DACS in the SSI 32D4661 Time Base Generator, can be used to control the VBP pin. This input voltage should be made proportional to the reference voltage at the VR pin for accuracy and temperature stability. The design equation for this control voltage is:

VBP = VR x (10^(FB/20) - 1) / 1.884 where FB is in dB.

Design example is given in Section 3.

With a finite boost, the magnitude response peaks at a frequency slightly higher than the original cutoff frequency. The effective pass band bandwidth is wider.

1.3 OTHER FEATURES OF THE SSI 32F8011

The SSI 32F8011 is a 7-pole Bessel type filter. It features excellent constant group delay. At fc = 13 MHz, the group delay variation from 0.2 fc to fc is less than 1ns. Furthermore, the high frequency boost function does not affect the group delay variation.

In addition to the normal low pass output, the SSI 32F8011 also provides a differentiated low pass output of the input signal. The signal delay is well matched to the normal output.

The SSI 32F8011 provides a temperature compensated reference voltage, VR, for the DAC references. Because the internal filter control circuitry is referenced to VR, the control current for filter cutoff frequency and control voltage for high frequency boost should be referenced to VR.

The SSI 32F8011 can be switched into a sleep mode, dissipating only 60 mW, by a TTL input at PWRON.

Two package options are available for the SSI 32F8011: 16-lead SOL and 16-lead SON. The small feature size of the 16-pin SON package offers significant board space saving.

2.0 APPLICATIONS

A programmable filter is a versatile component in any signal processing system. Some areas of applications include fixed response filtering, variable data rate processing and adaptive equalization.

For fixed response filtering applications, the SSI 32F8011 offers a simple-to-use solution. The once complex design of cutoff frequency or magnitude equalization is now rendered to simple resistance calculation. The narrow 16-pin small outline package offers significant board space economy.

In variable data rate processing, a programmable filter can be used to optimize bandwidth and signal-to-noise tradeoff. One application is constant density recording for high capacity storage products. As the data rate increases from the inner tracks to the outer tracks, the filter cutoff frequency can be scaled accordingly to maximize signal-to-noise performance. The high frequency boost function provides pulse slimming for accurate pulse detection.

Programmable filter offers a revolutionary approach to adaptive equalization. In signal transmission applications, an equalization filter is used to combat channel distortion. The magnitude of channel distortion is often not known a priori. Adaptive equalization can dynamically shape the equalization function. With an appropriate external adaptive sensing function, the cutoff frequency and the high frequency boost of the SSI 32F8011 can be dynamically programmed through microprocessor control.

3.0 FIXED RESPONSE DESIGN PROCEDURE

This section suggests some design guidelines to apply the SSI 32F8011 as a fixed response filter. Figure 3 shows the design schematic. Rx determines the filter's cutoff frequency, defined as the -3 dB frequency with no boost. The ratio of RB1 and RB2 determines the amount of high frequency boost.

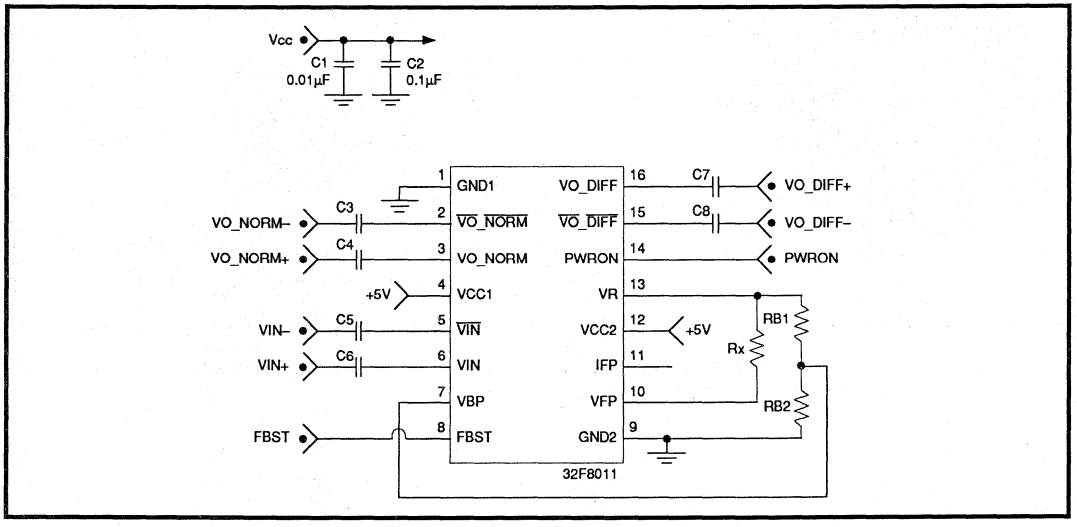

FIGURE 3: The 32F8011 Setup as a Fixed Response Filter

3.0 FIXED RESPONSE DESIGN PROCEDURE (continued)

Given fc, cutoff frequency in MHz, and FB, high frequency boost in dB:

- Rx can be calculated, as given in Section 1.
  Rx (kΩ) = 11.92 / fc (MHz)
  Voltage across Rx is 0.33 VR. The current through Rx is 0.33 (VR / Rx).
  Rx should be between 917 Ω to 2.38 kΩ, i.e., fc between 5 MHz to 13 MHz.
- RB1/RB2 sets FB, and can be determined as follows:
  RB1 / RB2 = 1.884 / (10^(FB / 20) - 1) - 1
- Total current drawn out of the VR pin should be limited to 2 mA max. Thus, RB1 and RB2 should be designed accordingly.
- The IFP pin should be left open.

4.0 PROGRAMMABLE RESPONSE DESIGN PROCEDURE

This section suggests some design guidelines to apply the SSI 32F8011 as a programmable filter. The high frequency boost can be controlled by a voltage DAC driving the VBP pin. The VBP voltage should be between 0 and VR. The cutoff frequency can be controlled by a current DAC. The application setup for using a current source DAC is different from the one using a current sink DAC. Both are presented below.

4.1 PROGRAMMABLE FILTER USING A CURRENT SOURCE DAC

Figure 4 shows the setup schematic of the SSI 32F8011 using an external current source DAC to control the filter's cutoff frequency.

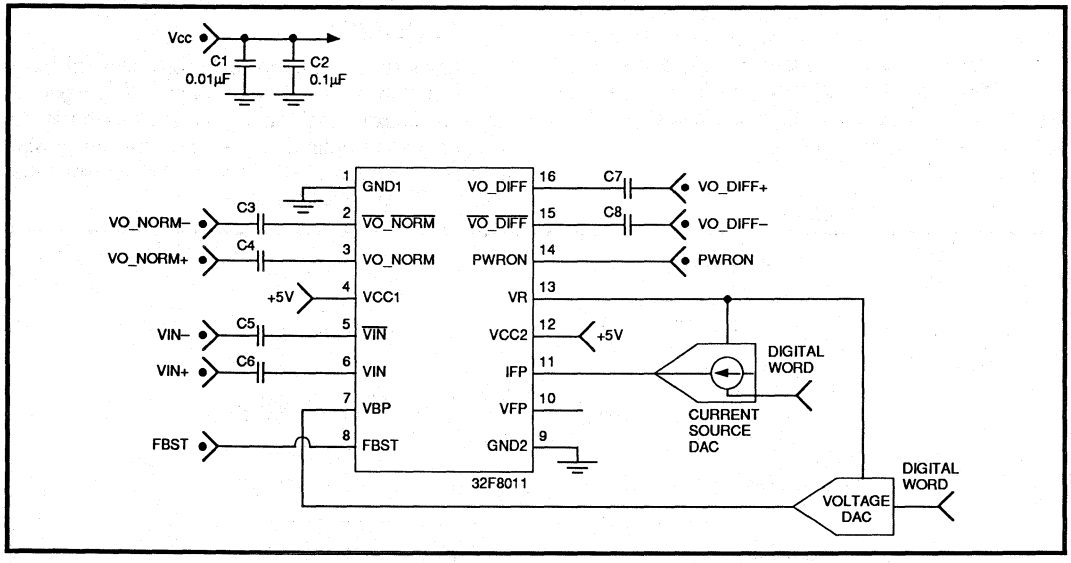

FIGURE 4: The SSI 32F8011 Setup Schematic Using a Current Source DAC for Cutoff Frequency Control

Some design guidelines:

- The VFP pin should be left open.
- Both the current source DAC and the voltage DAC should reference to VR for accuracy and temperature stability.
- The reference bias current drawn from VR should be less than 2 mA.
- The IFP current and the filter cutoff frequency are related as follows:

  $fc\ (MHz) = 16.25 \times IFP\ (mA) \times \frac{VR}{2.2}$

  IFP should be between 0.31 mA to 0.8 mA with VR = 2.2V.
- The VBP voltage and the high frequency boost are related as follows:

  $FB = 20 \times \log (1.884 \times VBP / VR + 1)\ dB$

4.2 PROGRAMMABLE FILTER USING CURRENT SINK DAC

Figure 5 shows the setup schematic of the SSI 32F8011 using an external current sink DAC to control the filter's cutoff frequency. The high frequency boost control is the same as in Section 4.1.

Some design guidelines:

- Rx should be set to 917Ω between VR and VFP.
- Both the current source DAC and the voltage DAC should reference to VR for accuracy and temperature stability.
- The total current drawn from VR should be less than 2mA. This includes the 0.8mA through Rx. Thus, the current sink DAC and the voltage DAC reference should not draw more than 1.2 mA.
- The IFP current and the cutoff frequency are related as follows:

  $fc\ (MHz) = 13 - 16.25 \times IFP\ (mA) \times \frac{VR}{2.2}$

  IFP should be between 0 mA to 0.49 mA.

Notes:

SSI 32F8020A
Programmable Electronic Filter

Application Note

November 1993

INTRODUCTION

Analog filtering is a universal requirement in any signal processing system. Filter design is now made easy with the programmable filters from Silicon Systems Inc. Whether the requirement is a fixed filtering characteristic or a programmable response, this family of programmable filters offers distinct advantages of design simplicity, accuracy, versatility and board space savings. Additional features, such as high frequency boost, differentiated outputs, are also available. This application note focuses on the SSI 32F8020A, cutoff frequency programmable from 1.5 - 8 MHz.

The objectives of this application note are:

- To present a description of the SSI 32F8020A
- To discuss its applications
- To present a typical fixed response design
- To present a programmable response application

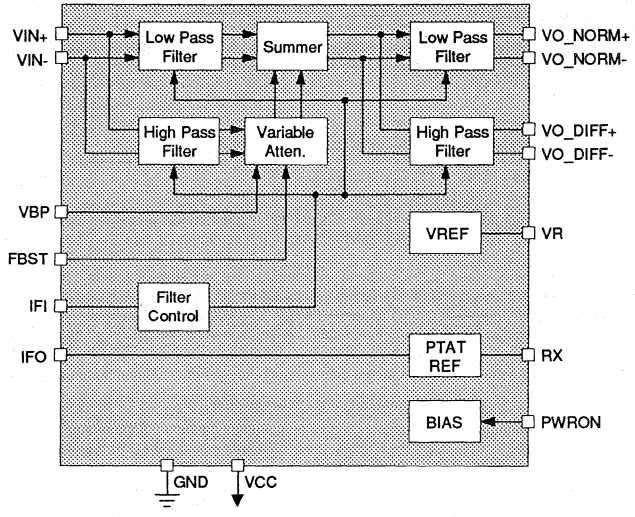

FIGURE 1: Block Diagram

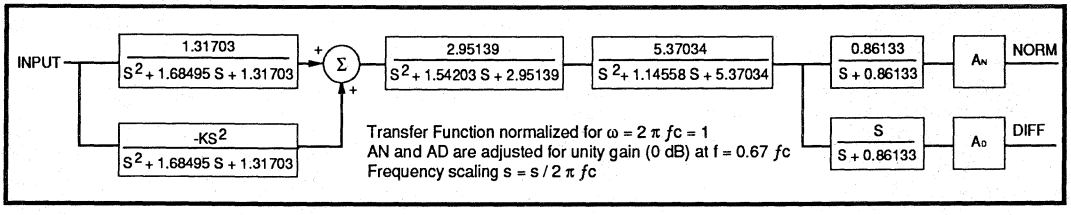

FIGURE 2: The SSI 32F8020A Transfer Function

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SSI 32F8020A
Programmable Electronic Filter

Application Note

1.0 DESCRIPTION

The SSI 32F8020A is a programmable 7-pole 0.05° equiripple low pass filter in a silicon bipolar integrated circuit. Figures 1 and 2 show the block diagram and the filter transfer function.

The SSI 32F8020A cutoff frequency and high frequency boost can be independently controlled by two control signals. Two sets of filter outputs are available: normal low pass output and differentiated low pass output. As a 0.05° equiripple type filter, the filter outputs exhibit constant group delay beyond its cutoff frequency. Furthermore, the delays through the normal output and the differentiated output are well matched.

The input and outputs of the SSI 32F8020A are differential signals, requiring external ac coupling capacitors. The given transfer function shows the relationship between the input and the two sets of outputs. The maximum input signal is 2.0 Vpp differential. The differential input resistance is 4 kΩ (typ.).

1.1 CUTOFF FREQUENCY CONTROL

The cutoff frequency, defined to be the -3dB corner frequency with no boost, is programmable from 1.5 - 8 MHz. It can be set by one of three methods:

1) A resistor is connected between Rx and Ground. The IFO and IFI pins are shorted. This setting is only used for a fixed response design. The design equation for this resistor value is:

   Rx (kΩ) = 10.00 / fc (MHz)

   A design example is given in Section 3.

2) A current source input can be fed into the IFI pin. With a current source digital-to-analog converter (DAC), such as the DACF in the SSI 32D4661 Time Base Generator, this design allows a microcontroller to change the filter response dynamically. A resistor from Rx to Ground is needed to establish a bias current on the IFO pin. To achieve the highest accuracy and temperature stability, this bias current on the IFO pin is used to reference the current source DAC. This bias current should be set such that the maximum DAC output current is 0.6 mA at room temperature. The design equations for Rx and the current source value are:

   Rx (kΩ) = 0.75 / IFO (mA) at T = 27°C

   IFI (mA) = 0.075 x fc (MHz)

   A design example is given in Section 4.

3) A current sink input can be fed into the IFI pin. With a current sink DAC, this design also allows a microcontroller to change the filter response dynamically. To achieve the highest accuracy and temperature stability, the current sink DAC should be referenced to the proportional to absolute temperature voltage at the Rx pin, nominally at 750 mV. The DAC maximum sinking current should be at least 0.49 mA. A resistor from Rx to Ground is needed. The total current drawn from the Rx pin needs to be 0.6 mA at room temperature. The IFO and IFI pins are shorted. The design equations for Rx and this current sink value are:

   Rx (kΩ) = 0.75 / (0.6 - $I_{DAC\ Bias}$) (mA)

   IFI (mA) = 0.60 - 0.075 x fc (MHz)

   A design example is given in Section 4.

1.2 HIGH FREQUENCY BOOST CONTROL

The high frequency boost function is especially desirable for pulse slimming and magnitude equalization applications. This function can be enabled or disabled by a TTL logic input at the FBST pin. With FBST = TTL logic high or open, the amount of high frequency boost, measured at the cutoff frequency, can be programmed from 0 to 9 dB by a voltage input at the VBP pin. External resistors can be used in for a fixed filter response. For a programmable high frequency boost, a voltage DAC, such as the DACS in the SSI 32D4661, can be used to control the VBP pin. This input voltage should be made proportional to the reference voltage at the VR pin for accuracy and temperature stability. The design equation for this control voltage is:

VBP = VR x (10^(FB/20) - 1) / 1.884

where FB is in dB.

Design example is given in Section 3.

With a finite boost, the magnitude response peaks at a frequency slightly higher than the original cutoff frequency. The effective pass band bandwidth is also wider.

1.3 OTHER FEATURES OF THE SSI 32F8020A

The SSI 32F8020A is a 7-pole 0.05° equiripple type filter. It features excellent constant group delay. The group delay variation from 0.2 fc to 1.75 fc is less than ± 2% of the total filter delay. Furthermore, the high frequency boost function does not affect the group delay variation.

In addition to the normal low pass output, the SSI 32F8020A also provides a differentiated low pass output of the input signal. The signal delay is well matched to the normal output.

The SSI 32F8020A provides a temperature compensated reference voltage, VR, and a proportional to absolute temperature voltage, Rx, for the DAC references. The filter cutoff frequency should be referenced to the current at the Rx pin. The high frequency boost control should be referenced to the voltage at the VR pin.

The SSI 32F8020A can be switched into a sleep mode, dissipating less than 2.5 mW, by a TTL low level input at the PWRON pin.

Two package options are available for the SSI 32F8020A: 16-pin SOL and 16-pin SON. The small feature size of the 16-pin SON package offers significant board space saving.

2.0 APPLICATIONS

A programmable filter is a versatile component in any signal processing system. Some areas of applications include fixed response filtering, variable data rate processing and adaptive equalization.

For fixed response filtering applications, the SSI 32F8020A offers a simple-to-use solution. The once complex design of cutoff frequency or magnitude equalization is now rendered to simple resistance calculations. The narrow 16-pin small outline package offers significant board space economy.

In variable data rate processing, a programmable filter can be used to optimize bandwidth and signal-to-noise tradeoff. One application is constant density recording for high capacity storage products. As the data rate increases from the inner tracks to the outer tracks, the filter cutoff frequency can be scaled accordingly to maximize signal-to-noise performance. The high frequency boost function provides pulse slimming for accurate pulse detection.

A programmable filter offers a revolutionary approach to adaptive equalization. In signal transmission applications, an equalization filter is used to combat channel distortion. The magnitude of channel distortion is often not known a priori. Adaptive equalization can dynamically shape the equalization function. With an appropriate external adaptive sensing function, the cutoff frequency and the high frequency boost of the SSI 32F8020A can be dynamically programmed through microprocessor control.

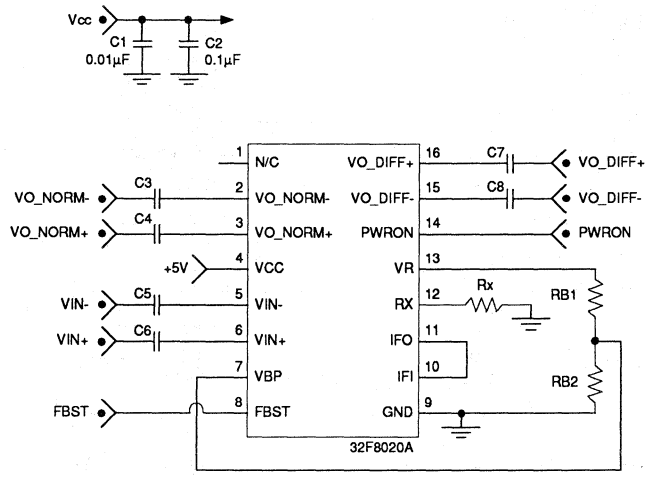

FIGURE 3: The 32F8020A Setup as a Fixed Response Filter

3.0 FIXED RESPONSE DESIGN PROCEDURE

This section suggests some design guidelines to apply the SSI 32F8020A as a fixed response filter. Figure 3 shows the design schematic. Rx determines the filter's cutoff frequency, defined as the -3 dB frequency with no boost. The ratio of RB1 and RB2 determines the amount of high frequency boost.

Given fc, cutoff frequency in MHz, and FB, high frequency boost in dB:

- Rx can be calculated, as given in Section 1.

  Rx (kΩ) = 10.00 / fc (MHz)

  Voltage across Rx is 0.75V, and is proportional to the absolute temperature.

  Rx should be between 1.25 kΩ to 6.67 kΩ, i.e., fc between 1.5 MHz to 8 MHz.

- RB1/RB2 sets FB, and can be determined as follows:

  RB1 / RB2 = 1.884 / (10^(FB / 20) - 1) - 1

- Total current drawn out of the VR pin should be limited to 2 mA max. Thus, RB1 and RB2 should be designed accordingly.
- The IFO and IFI pins are shorted together.

4.0 PROGRAMMABLE RESPONSE DESIGN PROCEDURE

This section suggests some design guidelines to apply the SSI 32F8020A as a programmable filter. The high frequency boost can be controlled by a voltage DAC driving the VBP pin. The VBP voltage should be between 0 and VR. The cutoff frequency can be controlled by a current DAC. The application setup for using a current source DAC is different from the one using a current sink DAC. Both are presented below.

4.1 PROGRAMMABLE FILTER USING A CURRENT SOURCE DAC

Figure 4 shows the setup schematic of the SSI 32F8020 using an external current source DAC to control the filter's cutoff frequency.

Some design guidelines:

- The current source DAC should be referenced to the IFO current. The voltage DAC should reference to VR.
- The reference bias current drawn from VR should be less than 2 mA.
- The IFO current biases the current source DAC for 0.6 mA maximum output at room temperature.

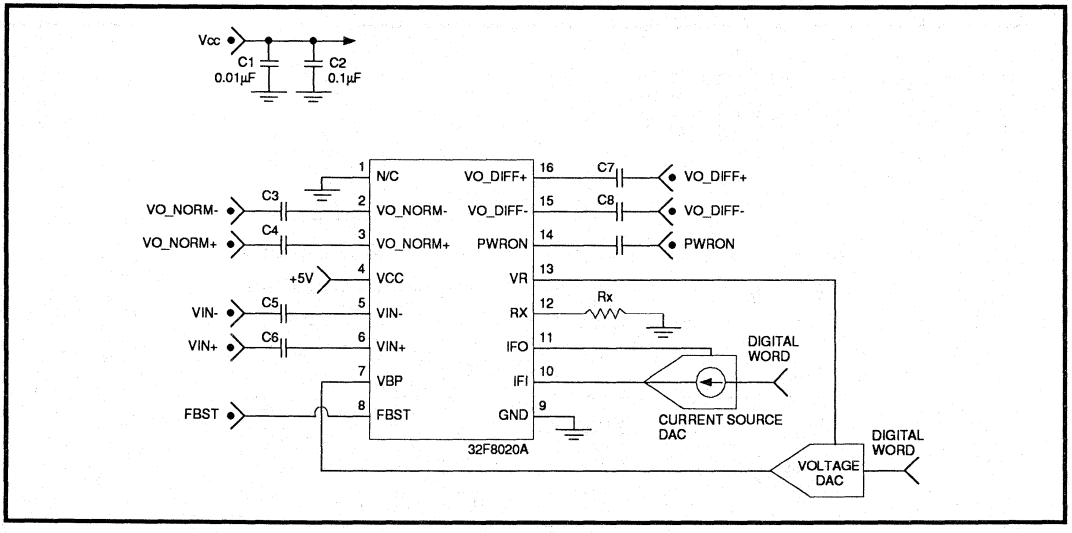

FIGURE 4: The SSI 32F8020A Setup Schematic Using a Current Source DAC for Cutoff Frequency Control

4.1 PROGRAMMABLE FILTER USING A CURRENT SOURCE DAC (continued)

- The Rx resistor determines the IFO current.

  Rx (kΩ) = 0.75 / $I_{DAC\ Bias}$ (mA)

- The IFI current and the filter cutoff frequency are related as follows:

  fc (MHz) = 13.33 x IFI (mA)

  IFI should be between 0.11 mA to 0.6 mA at room temperature.

- The VBP voltage and the high frequency boost are related as follows:

  FB = 20 x log (1.884 x VBP / VR + 1) dB

4.2 PROGRAMMABLE FILTER USING CURRENT SINK DAC

Figure 5 shows the setup schematic of the SSI 32F8020 using an external current sink DAC to control the filter's cutoff frequency. The high frequency boost control is the same as in Section 4.1.

Some design guidelines:

- The current sink DAC should reference to the voltage at the Rx pin.

  The voltage DAC should reference to VR.

- The IFO and IFI pins are shorted.

- The total current drawn from VR should be less than 2 mA.

  The total current drawn from the Rx pin should be 0.6 mA.

  Rx (kΩ) = 0.75 / (0.6 - $I_{DAC\ Bias}$) (mA)

- The IFI current and the cutoff frequency are related as follows:

  fc (MHz) = 8 - 13.33 x IFI (mA)

  IFI should be between 0 mA to 0.49 mA.

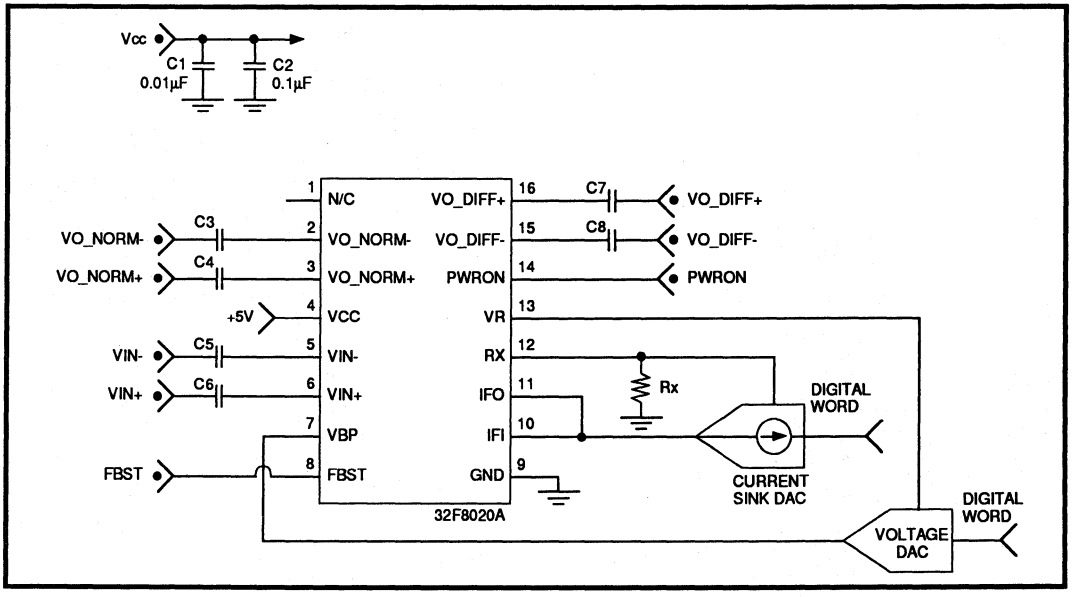

FIGURE 5: The SSI 32F8020A Setup Schematic Using a Current Sink DAC for Cutoff Frequency Control

Notes:

SSI 32F8030
Programmable Electronic Filter

Application Note

November 1993

INTRODUCTION

Analog filtering is a universal requirement in any signal processing system. Filter design is now made easy with the programmable filters from Silicon Systems Inc. Whether the requirement is a fixed filtering characteristic or a programmable response, this family of programmable filters offers distinct advantages of design simplicity, accuracy, versatility and board space savings. Additional features, such as high frequency boost, differentiated outputs, are also available. This application note focuses on the SSI 32F8030, cutoff frequency programmable from 250 kHz - 2.5 MHz.

The objectives of this application note are:

- To present a description of the SSI 32F8030
- To discuss its applications
- To present a typical fixed response design
- To present a programmable response application

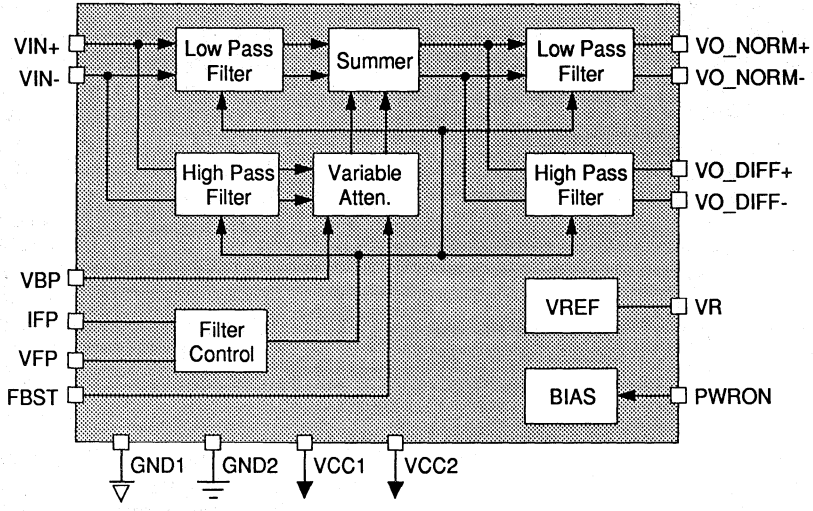

FIGURE 1: Block Diagram

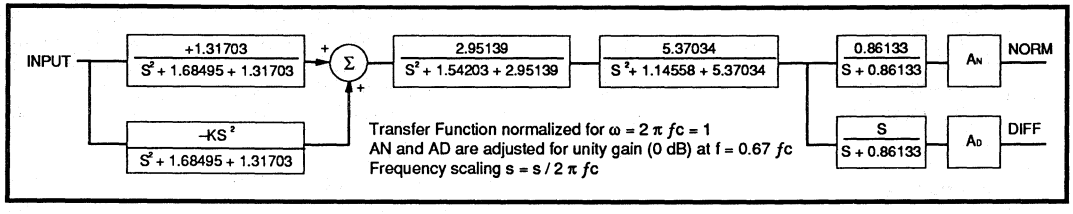

FIGURE 2: The SSI 32F8030 Transfer Function

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1.0 DESCRIPTION

The SSI 32F8030 is a programmable 7-pole 0.05° Equiripple low pass filter in a silicon bipolar integrated circuit. Figures 1 and 2 show the block diagram and the filter transfer function.

The SSI 32F8030 cutoff frequency and high frequency boost can be independently controlled by two control signals. Two sets of filter outputs are available: normal low pass output and differentiated low pass output. As a 0.05° Equiripple type filter, the filter outputs exhibit constant group delay beyond the pass band. Furthermore, the delays through the normal output and the differentiated output are well matched.

The input and outputs of the SSI 32F8030 are differential signals, requiring external AC coupling capacitors. The given transfer function shows the relationship between the input and the two sets of outputs. The maximum input signal is at least 1.0 Vpp differential, with differential input resistance 4 kΩ typical.

1.1 CUTOFF FREQUENCY PROGRAMMING

The cutoff frequency, defined to be the -3 dB corner frequency with no boost, can be programmed between 250 kHz - 2.5 MHz. It can be set by one of three methods:

- A resistor can be inserted between the VR and the VFP pins. This setting is only used for a fixed response design. The IFP pin should be left open. The design equation for this resistor value is:

  Rx (kΩ) = 2.292 / fc (MHz)

  A design example is given in Section 4.

- A current source input can be fed into the IFP pin. The VFP pin should be left open. A current source digital-to-analog converter (DAC), such as the DACF in the SSI 32D4661 Time Base Generator, allows a microcontroller to change the filter response dynamically. To achieve the highest accuracy and temperature stability, the current source DAC should be referenced to the temperature compensated reference voltage at the VR pin. The design equation for this current source value is:

  IFP (mA) = 0.320 x fc (MHz)

  A design example is given in Section 4.

- A current sink input can be fed into the IFP pin. A 917Ω resistor should be placed across the VR and the VFP pins. With a current sink DAC, this design also allows a microcontroller to change the filter response dynamically. To achieve the highest accuracy and temperature stability, the current sink DAC should be referenced to the temperature compensated reference voltage at the VR pin. The design equation for this current sink value is:

  IFP (mA) = 0.320 x (2.5 - fc) (MHz)

  A design example is given in Section 4.

1.2 HIGH FREQUENCY BOOST CONTROL

The high frequency boost function is especially desirable for pulse slimming and magnitude equalization applications. This function can be enabled or disabled by a TTL logic input at the FBST pin. With FBST = TTL logic high or open, the amount of high frequency boost measured at the cutoff frequency can be programmed from 0 to 9 dB by a voltage input at the VBP pin. External resistors can be designed in for a fixed filter response. For a programmable high frequency boost, a voltage DAC, such as the DACS in the SSI 32D4661 Time Base Generator, can be used to control the VBP pin. This input voltage should be made proportional to the reference voltage at the VR pin for accuracy and temperature stability. The design equation for this control voltage is:

VBP = VR x (10^(FB/20) - 1) / 1.884 where FB is in dB.

Design example is given in Section 3.

With a finite boost, the magnitude response peaks at a frequency slightly higher than the original cutoff frequency. The effective pass band bandwidth is wider.

1.3 OTHER FEATURES OF THE SSI 32F8030

The SSI 32F8030 is a 7-pole 0.05° Equiripple filter. It features excellent constant group delay. The group delay variation from 0.2 fc to 1.75 fc is less than 3% of mean group delay. Furthermore, the high frequency boost function does not affect the group delay variation.

In addition to the normal low pass output, the SSI 32F8030 also provides a differentiated low pass output of the input signal. The signal delay is well matched to the normal output.

The SSI 32F8030 provides a temperature compensated reference voltage, VR, for the DAC references. Because the internal filter control circuitry is referenced to VR, the control current for filter cutoff frequency and control voltage for high frequency boost should be referenced to VR.

The SSI 32F8030 can be switched into a sleep mode, dissipating < 5 mW, by a TTL input at PWRON.

Two package options are available for the SSI 32F8030: 16-pin SOL and 16-pin SON. The small feature size of the 16-pin SON package offers significant board space saving.

2.0 APPLICATIONS

A programmable filter is a versatile component in any signal processing system. Some areas of applications include fixed response filtering, variable data rate processing and adaptive equalization.

For fixed response filtering applications, the SSI 32F8030 offers a simple-to-use solution. The once complex design of cutoff frequency or magnitude equalization is now rendered to simple resistance calculation. The narrow 16-pin small outline package offers significant board space economy.

In variable data rate processing, a programmable filter can be used to optimize bandwidth and signal-to-noise tradeoff. One application is constant density recording for high capacity storage products. As the data rate increases from the inner tracks to the outer tracks, the filter cutoff frequency can be scaled accordingly to maximize the signal-to-noise performance. The high frequency boost function provides pulse slimming for accurate pulse detection.

Programmable filter offers a revolutionary approach to adaptive equalization. In signal transmission applications, an equalization filter is used to combat channel distortion. The magnitude of channel distortion is often not known a priori. Adaptive equalization can dynamically shape the equalization function. With an appropriate external adaptive sensing function, the cutoff frequency and the high frequency boost of the SSI 32F8030 can be dynamically programmed through a microprocessor control.

3.0 FIXED RESPONSE DESIGN PROCEDURE

This section suggests some design guidelines to apply the SSI 32F8030 as a fixed response filter. Figure 3 shows the design schematic. Rx determines the filter's cutoff frequency, defined as the -3 dB frequency with no boost. The ratio of RB1 and RB2 determines the amount of high frequency boost.

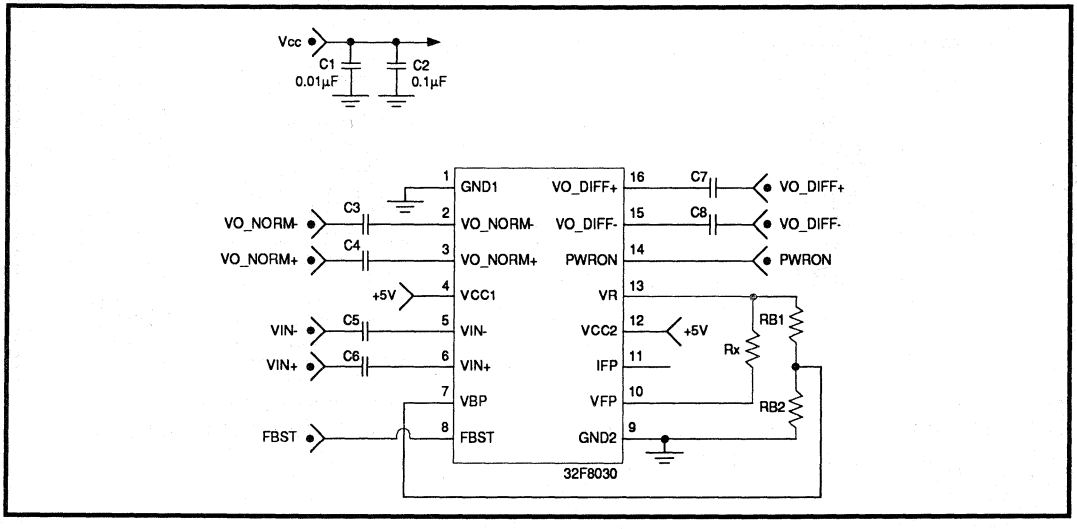

FIGURE 3: The 32F8030 Setup as a Fixed Response Filter

3.0 FIXED RESPONSE DESIGN PROCEDURE (continued)

Given fc, cutoff frequency in MHz, and FB, high frequency boost in dB:

- Rx can be calculated, as given in Section 1.
  Rx (kΩ) = 2.292 / fc (MHz)
  Voltage across Rx is 0.33 VR. The current through Rx is 0.33 (VR / Rx).
  Rx should be between 917Ω to 9.17 kΩ, i.e., fc between 250 kHz to 2.5 MHz.
- RB1/RB2 sets FB, and can be determined as follows:
  RB1 / RB2 = 1.884 / (10^(FB / 20) - 1) - 1
- Total current drawn out of the VR pin should be limited to 2 mA max. Thus, RB1 and RB2 should be designed accordingly.
- The IFP pin should be left open.

4.0 PROGRAMMABLE RESPONSE DESIGN PROCEDURE

This section suggests some design guidelines to apply the SSI 32F8030 as a programmable filter. The high frequency boost can be controlled by a voltage DAC driving the VBP pin. The VBP voltage should be between 0 and VR. The cutoff frequency can be controlled by a current DAC. The application setup for using a current source DAC is different from the one using a current sink DAC. Both are presented below.

4.1 PROGRAMMABLE FILTER USING A CURRENT SOURCE DAC

Figure 4 shows the setup schematic of the SSI 32F8030 using an external current source DAC to control the filter's cutoff frequency.

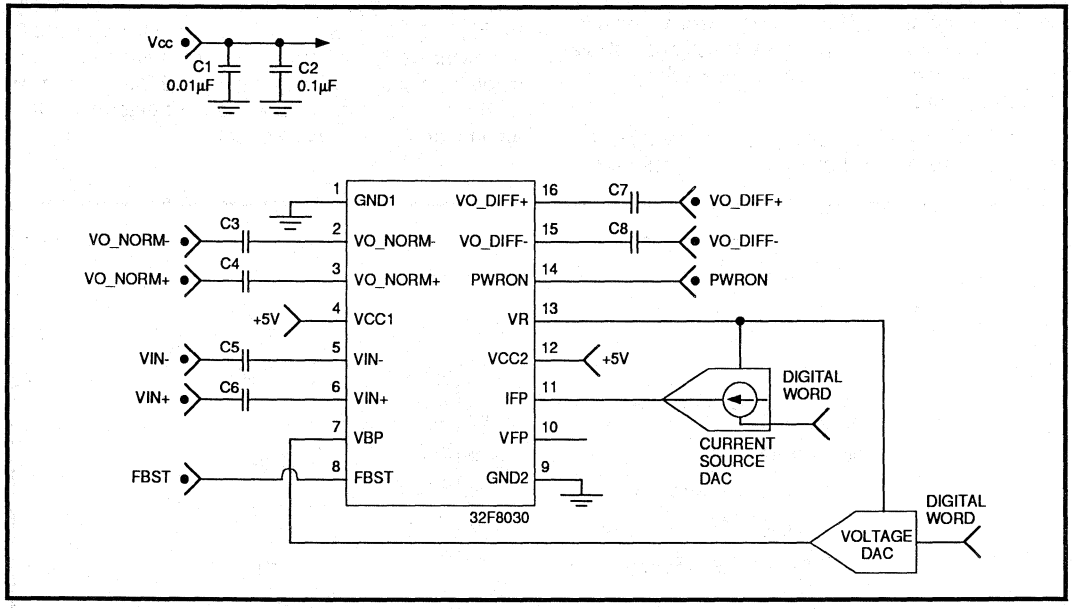

FIGURE 4: The SSI 32F8030 Setup Schematic Using a Current Source DAC for Cutoff Frequency Control

Design guidelines for the SSI 32F8030:

- The VFP pin should be left open.
- Both the current source DAC and the voltage DAC should reference to VR for accuracy and temperature stability.
- The reference bias current drawn from VR should be less than 2 mA.
- The IFP current and the filter cutoff frequency are related as follows:

  fc (MHz) = 3.125 x IFP (mA)

  IFP should be between 0.08 mA to 0.8 mA.
- The VBP voltage and the high frequency boost are related as follows:

  FB = 20 x log (1.884 x VBP / VR + 1) dB

4.2 PROGRAMMABLE FILTER USING CURRENT SINK DAC

Figure 5 shows the setup schematic of the SSI 32F8030 using an external current sink DAC to control the filter's cutoff frequency. The high frequency boost control is the same as in Section 4.1.

Some design guidelines:

- Rx should be set to 917Ω between VR and VFP.
- Both the current source DAC and the voltage DAC should reference to VR for accuracy and temperature stability.
- The total current drawn from VR should be less than 2 mA. This includes the 0.8 mA through Rx. Thus, the current sink DAC and the voltage DAC reference should not draw more than 1.2 mA.
- The IFP current and the cutoff frequency are related as follows:

  fc (MHz) = 2.5 - 3.125 x IFP (mA)

  IFP should be between 0 mA to 0.72 mA.

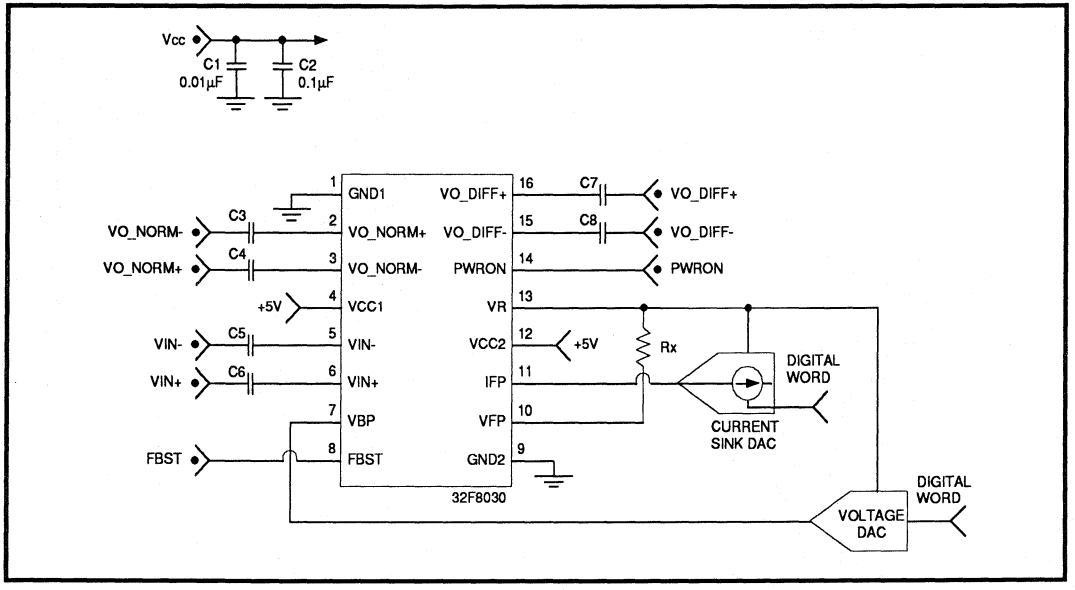

FIGURE 5: The SSI 32F8030 Setup Schematic Using a Current Sink DAC for Cutoff Frequency Control

Notes:

November 1993

INTRODUCTION

The SSI 32P3000 is a high performance pulse detector for 48 Mbit/s storage system applications. It provides the complete solution for detection and qualification of encoded read signals. The AGC function, noise limiting filtering, pulse slimming, level and time qualifications are all integrated into one chip. Additional features include input impedance control, fast AGC recovery from write-to-read transition, and independent positive and negative threshold qualifications.

The objectives of this application note are to:

- Present a brief description of the SSI 32P3000
- Present a description of the evaluation board of the SSI 32P3000
- Explain in detail key features of the SSI 32P3000

While the evaluation board design does not suggest optimized component values, which vary with system requirements, it presents a means to evaluate the performance of the SSI 32P3000. Test setups in evaluation of pulse pairing, exercise of fast recovery function and others are suggested in this application note.

1.0 DESCRIPTION OF THE SSI 32P3000

The AGC amplifier compensates for variations in head preamp output levels, and presents a constant input level to the pulse qualification circuitry. The AGC action can be suspended to hold at a constant gain in embedded servo decode or other processing needs.

A programmable 7-pole Bessel low pass filter is included. Two sets of filter outputs are available: normal low pass output and differentiated low pass output. The signal delays of the two outputs are well matched, ideal in pulse qualification. The filter cutoff frequency can be

(continued)

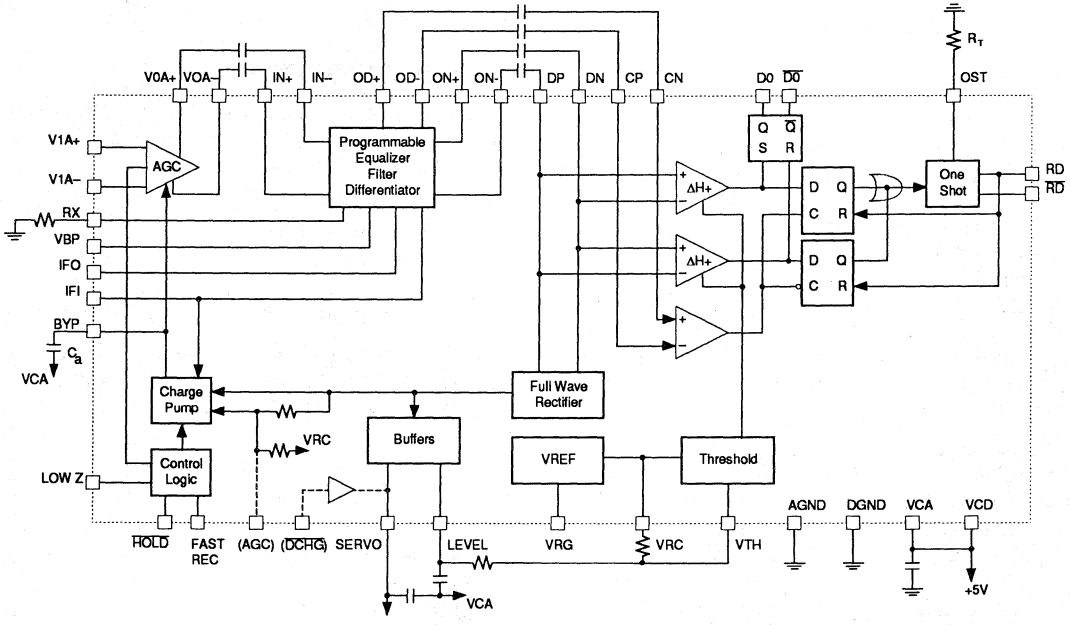

Figure 1: The SSI 32P3000 Block Diagram

1.0 DESCRIPTION OF THE SSI 32P3000 (continued)

programmed from 9 to 27 MHz, via a current input. Up to 13 dB high frequency boost (for pulse slimming) can also be independently programmed. The SSI 32P3000 is ideal for constant density recording.

Both level qualification and time qualification are used in the SSI 32P3000 pulse qualification. For level qualification, the filter output peak can be fed forward to establish the comparator hysteresis threshold. This allows the threshold to track the comparator input amplitude, and to qualify data while AGC amplifier settling is still in transition. The 32P3000 employs a dual-comparator qualification scheme, which allows independent positive and negative threshold detection. This has the advantage of reducing error propagation. For time qualification, the differentiated filter output translates each input peak into a zero crossing, and is used in clocking the comparator outputs.

For each peak of the VIA+/-, there is a one-shot pulse at the differential RD output. The pulse width of the one-shot pulse is determined by a user selected resistor at the OST pin.

The SSI 32P3000 is available in a 36-pin SOM package.

2.0 DESCRIPTION OF THE EVALUATION BOARD

The SSI 32P3000 can be evaluated with the 48 Mbit/s Demo Board from Silicon Systems. This board is designed with the Silicon Systems 48 Mbit/s chip set: 32P3000 (36-pin SOM) as the pulse detector, 32D4661 (24-pin DIP) as the time base generator; and 32D539 (44-pin PLCC) as the data synchronizer with 1,7 RLL ENDEC. The SSI 32D4661 provides two digital-to-analog converters (DAC) to program the filter cutoff frequency and the high frequency boost function of the SSI 32P3000 filter. In evaluating the SSI 32P3000, the SSI 32D539 is not needed.

This evaluation board requires the Silicon Systems Parallel Port Cable to interface between a PC parallel port and the SSI 32P4661. This reduces the filter programming to simple inputs through an IBM PC. Details in programming steps are discussed in a later section.

The analog inputs, VIA+/-, mode control inputs, LOWZ, $\overline{\text{HOLD}}$- and FAST REC, and read data outputs, RD+/- of the SSI 32P3000 are accessible through pin terminals. The filter inputs and outputs are not brought out to pin terminals, but accessible at the pads of their respective coupling capacitors.

3.0 EQUIPMENT AND SOFTWARE REQUIREMENTS

To facilitate the following demonstrations of the SSI 32P3000 with the Silicon Systems 48 MB Demo Board, the following equipment and software are needed:

- IBM PC with parallel port
- Silicon Systems proprietary software 4 bit.exe
- Silicon Systems parallel port cable
- +5V power supply to Silicon Systems 48 MB Demo Board
- TTL pattern generator
- Signal generator, with amplitude modulation input
- Oscilloscope
- Spectrum analyzer, with a tracking output, for filter characteristics measurements
- Time interval analyzer, for pulse pairing measurement

4.0 DEMONSTRATIONS

Four demonstration setups are presented in this section for:

- general functionality
- pulse pairing
- filter characteristic
- fast recovery exercise

4.1 SOFTWARE SETUP & COMMANDS

To facilitate filter cutoff frequency and high frequency boost control, a parallel port and Silicon Systems software are used to command the two 7-bit DACs in the SSI 32D4661.

Type 4 bit v 25 to access the Silicon Systems proprietary software program for controlling the DACs.

In evaluating the SSI 32P3000, only two functions are controlled from the keyboard: the filter cutoff frequency and the high frequency boost. Because each DAC in the SSI 32D4661 is a 7-bit DAC and the Silicon Systems Serial Comm Board data is 4-bit wide, two registers are needed for each function control. Registers (address) 8 and 9 are for high frequency boost control; Registers 10

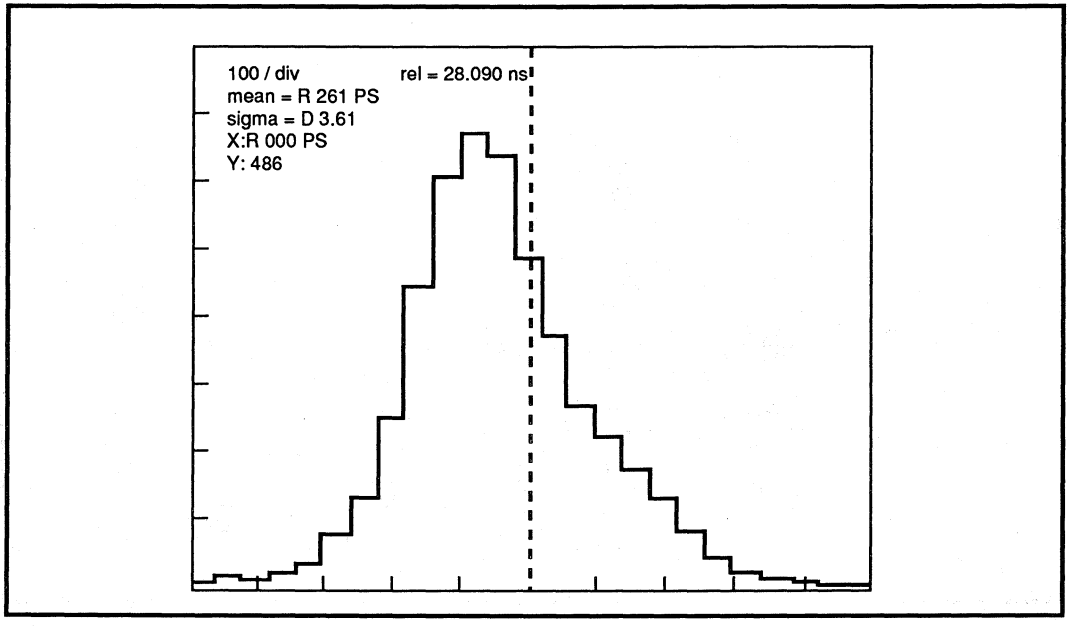

Figure 5: Histogram of RD Periods with 18 MHz Sinusoidal Input
No Bimodal Distribution => Pulse Pairing less than 500 ps

4.3 PULSE PAIRING MEASUREMENT (continued)

The test procedure is as follows:

- Feed a low jitter sinusoidal input
- Measure the time distance between RD pulses, corresponding to one positive peak detection and one negative peak detection
- Histogram plot measurements
- Significant pulse pairing will appear as a bimodal distribution of time period measurements
- Pulse pairing can be calculated as half of the time distance between two peaks in the histogram plot

Figure 4 shows a setup for the pulse pairing measurement. The SSI 32P3000 has demonstrated less than 500 ps pulse pairing, as shown in Figure 5.

4.4 FILTER CHARACTERISTIC

The SSI 32P3000 is ideal for constant density recording application with its programmable filter. The filter is a 7-pole Bessel low pass filter with normal output, as well as differentiated output. The normal output is for level qualification; the differentiated output is for time qualification. Their signal delays are well matched. The group delay is maintained within ±300 ps from 0.3 fc to fc. The filter cutoff frequency can be programmed from 9 MHz to 27 MHz through a current input at the IFI pin. The high frequency boost can be programmed from 0 to 13 dB through a voltage input at the VBP pin.

fc = 45 x IFI MHz; IFI in mA (at room temp.)

Boost = 20 x log [Kb (VBP / VRG) + 1] dB;
VRG is reference voltage at Pin 1.

Kb = 3.041 + 0.0276 x fci, where fci is the ideal cutoff frequency.

Figure 6 shows a test setup to evaluate the frequency response of the SSI 32P3000 filter. The SSI 32D4661 provides two 7-bit DACs for ease of programming.

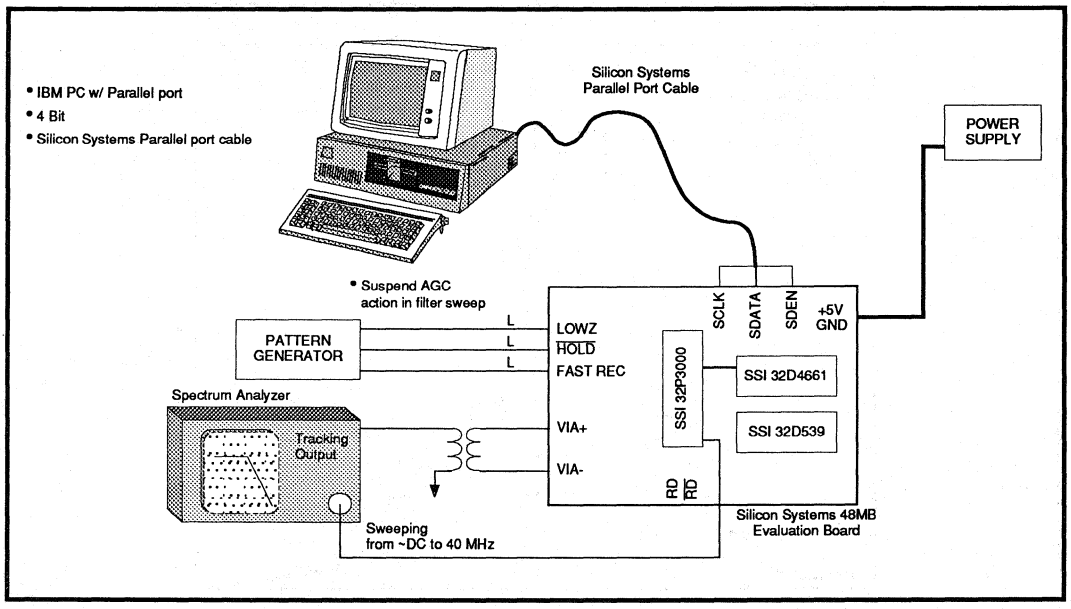

Figure 6: SSI 32P3000 Evaluation Board Filter Characteristic Setup

The full scale DAC value, i.e., Code 127, corresponds to maximum cutoff frequency, 27 MHz, or maximum boost, 13 dB. In decimal code, the cutoff frequency and high frequency boost can be calculated as follows:

fc = 27 MHz x (DACF Code) / 127;
42 ≤ DACF Code ≤ 127

Boost = 20 x log [Kb x (DACS Code) / 127 + 1] dB;
0 ≤ DACS Code ≤ 127

Because the Silicon Systems Serial Communication Board works with 4-bit nibbles, each 7-bit code is divided into two registers. For cutoff frequency control, R10 and R11 represents the 3 most significant bits (MSB) and the 4 least significant bits (LSB), respectively. Only the lower 3 bits of R10 4-bit nibble is used. For high frequency boost control, R8 and R9 represents the 3 MSBs and the 4 LSBs, respectively.

For example, the user wants to program the filter to 14 MHz cutoff with 3 dB boost. The DAC codes are calculated as the following:

DACF Code = 127 x 14 / 27 = 66, R10=4 R11=2;

DACS Code = 127 x [10^(3 / 20) -1] / 3.467 = 15,

R8=0 R9=15.

At the keyboard, the user enters **R8=0 R9=15 R10=4 R11=2**, followed by Alt. T.

To evaluate the frequency response of the filter, the AGC amplifier gain must be held constant, $\overline{\text{HOLD}}$=0. The tracking output of the spectrum analyzer sweeps the signal over a frequency spectrum. The filter output can be examined at the pad of C5 on the board. Figure 7 shows the filter responses at 9 MHz and at 27 MHz. Figure 8 shows the filter response with no boost and that with maximum boost.

and 11 are for filter cutoff frequency control. Other registers are used to control the SSI 32D539 functions which are not covered in this application note.

Upon power up of the evaluation board, these registers must be initialized by the user. Press Alt 8 (selects register 8), Alt 9 (selects register 9), Alt A (selects register 10) and Alt B (selects register 11). Using the cursor keys, position the cursor to the appropriate value column. Press the enter key and then backspace to erase its contents. Key in the new value and press enter again. Pressing Alt T transmits all selected registers. For now, type **R8=0 R9=0 R10=7 R11=15**, followed by Alt T. Details are given in Section 5.4 filter characteristics discussion. The above command sets the filter at 27 MHz cutoff frequency with no boost.

4.2 GENERAL FUNCTIONALITY

Figure 2 shows a general setup to evaluate the SSI 32P3000. In normal read operation, the following conditions should be set: LOWZ=0, $\overline{\text{HOLD}}$=1 and FAST REC=0. With an 18 MHz, 200 mVpp sinusoidal input, the RD/$\overline{\text{RD}}$ shows a pulse corresponding to each positive peak and each negative peak, as shown in Figure 3. The pulse width has been preset to be ~ 10 ns, with RT = 3 kΩ. The user may change the pulse width by replacing RT.

RT = 196Ω + Pulse Width / [0.157 (22 pF + Cstray)]
RT should be between 2 kΩ to 8 kΩ.

4.3 PULSE PAIRING MEASUREMENT

The SSI32P3000 has demonstrated excellent pulse pairing performance, less than 500 ps. Pulse pairing is one of the most critical parameters of any pulse detector. It is defined to be the systematic time error from ideal, caused by comparator threshold offset, in pulse detection of an input signal peak.

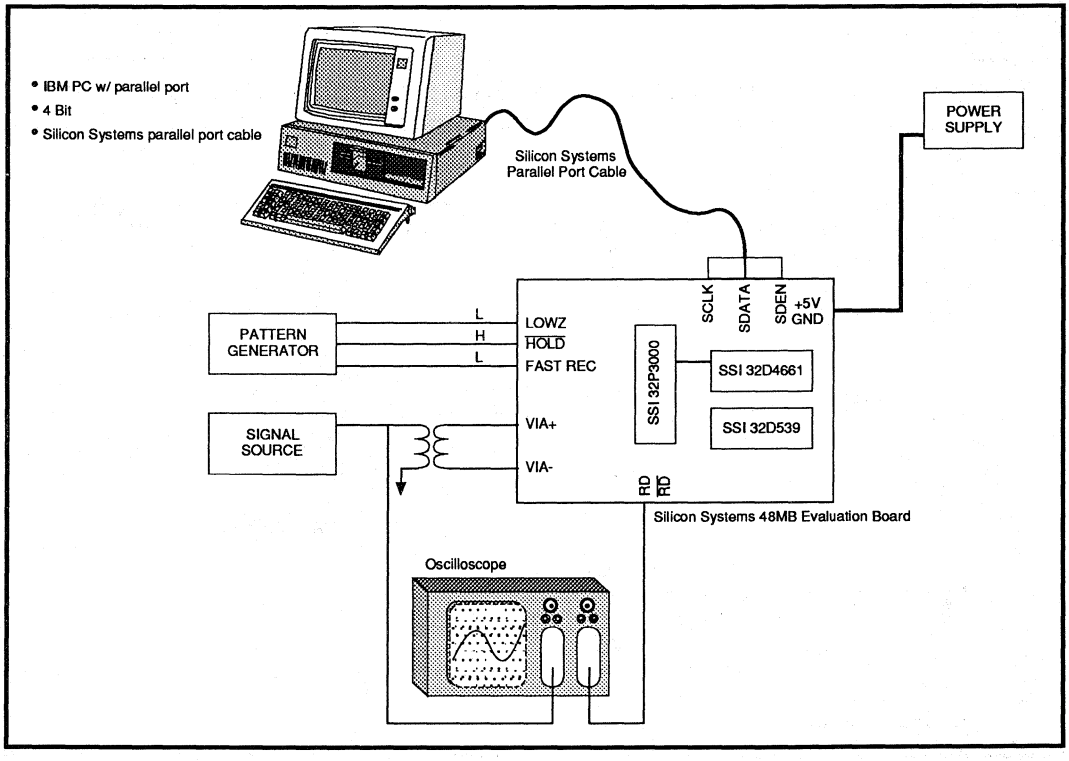

Figure 2: SSI 32P3000 Evaluation Board General Setup

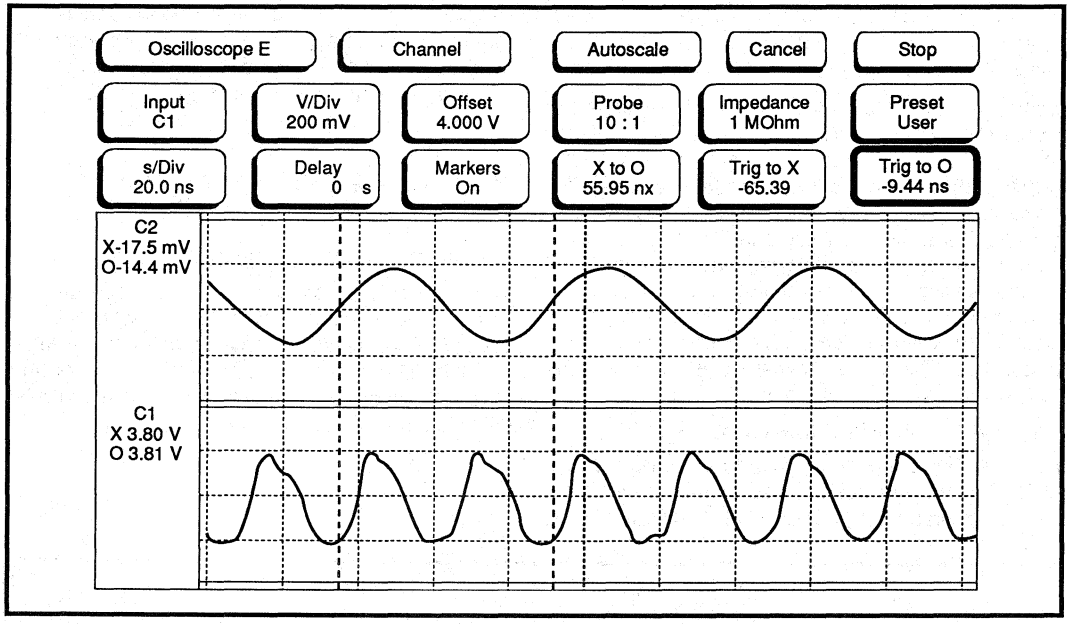

Figure 3: Normal Read Function: 18 MHz Sinusoidal Input (top) and RD Pulses (bottom)

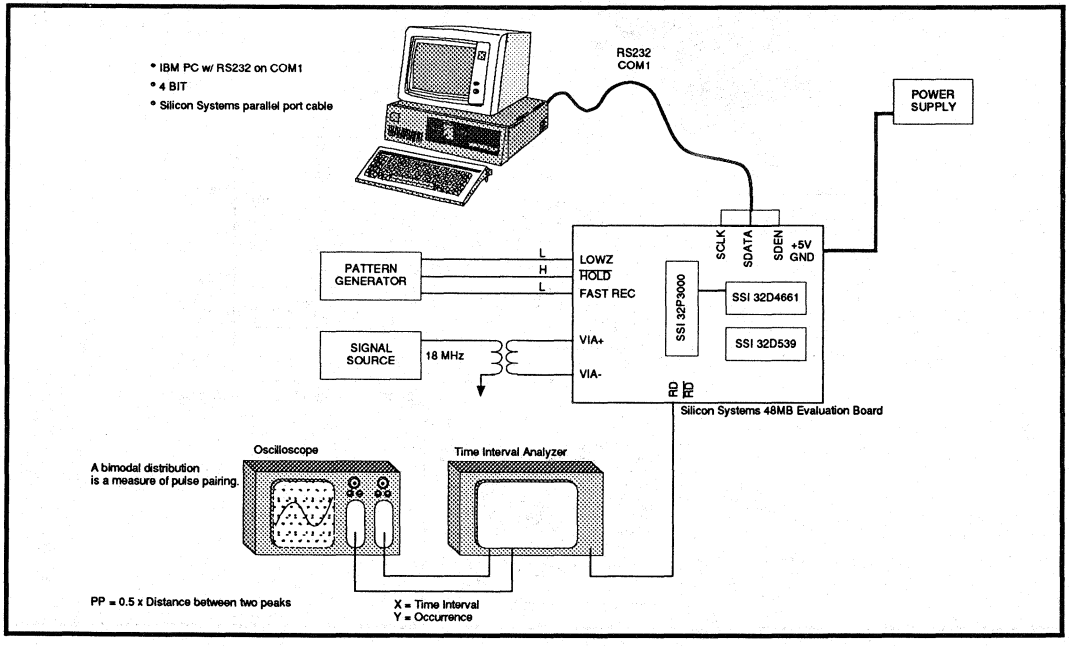

Figure 4: SSI 32P3000 Evaluation Board Pulse Pairing Setup

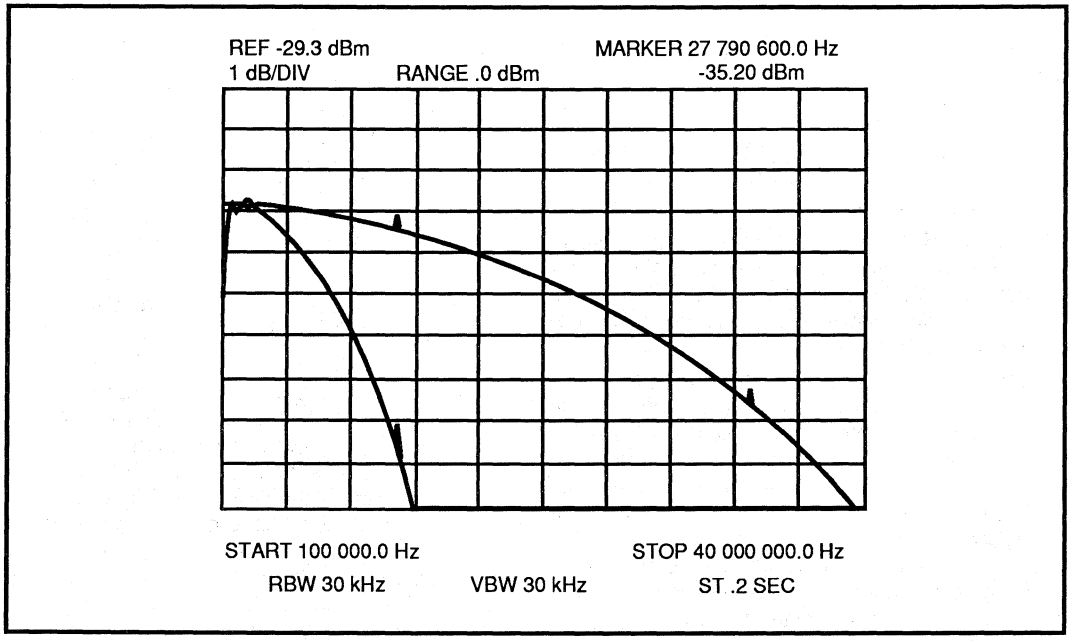

Figure 7: SSI 32P3000 Filter Magnitude Responses at 9 MHz (left) and 27 MHz (right) Cutoff

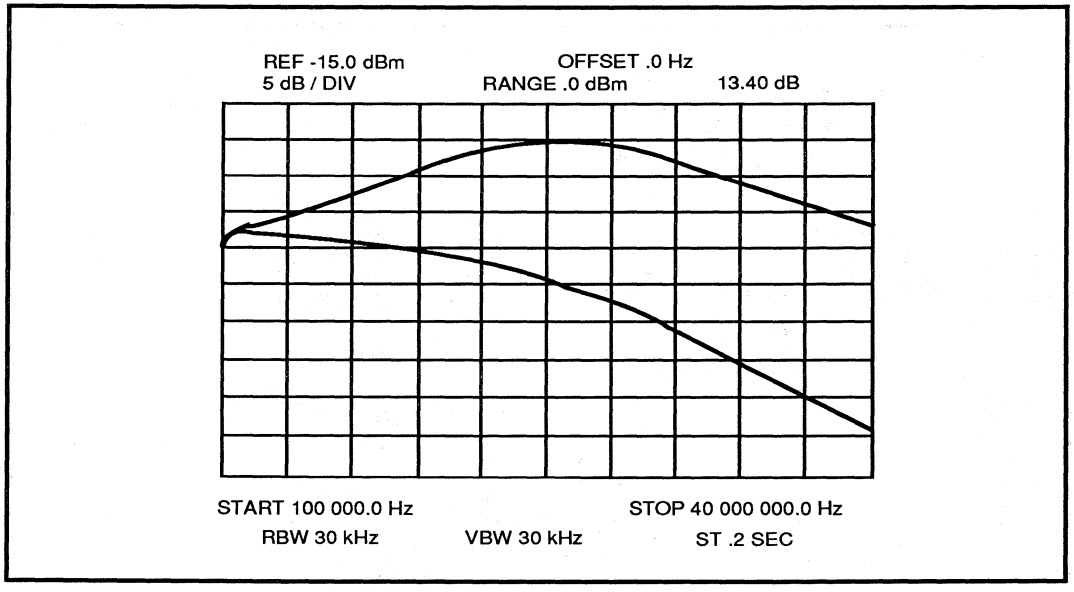

Figure 8: Cutoff Frequency = 14 MHz. The SSI 32P3000 Filter Response with no boost (bottom) and with maximum boost (top)

4.5 AGC ACTIONS & RECOVERY

The SSI 32P3000 has the following AGC control features:

- Automatic
  Fast Attack: When the DIN+/- input exceeds the preset nominal level (1 Vpp) by 25%, a fast attack current, 2.24 x IFI, quickly discharges CBYP and lowers the AGC amplifier gain.

  Slow Attack: When DIN+/- input exceeds the preset nominal level by less than 25%, a slow attack current, 0.32 x IFI, discharges CBYP and lowers the AGC amplifier gain until DIN+/- returns to nominal level.

  Slow Decay: When the DIN+/- input falls below the preset nominal level, a small decay current, 0.008 x IFI, charges CBYP and increases the AGC amplifier gain until DIN+/- returns to nominal. Because Fast Attack and Slow Attack currents are much larger than that of Slow Decay, it is obvious that AGC amplifier gain can be lowered quickly, but can only be increased very slowly. The purpose of the large ratio between attack/decay current is to ensure that the AGC settles to the peak-to-peak voltage amplitude.

- User Control
  Fast Recovery: To recover the AGC amplifier gain from a low gain condition rapidly, the FAST REC can be asserted. With FAST REC = 1, a fast decay current, 0.16 x IFI, charges CBYP continuously, independent of signal level. While the Fast and Slow Attacks are still active, the AGC amplifier gain settles quickly to ~125% of nominal. When the FAST REC returns to 0, the Fast Attack and Slow Attack actions restore the AGC amplifier gain to 100% level.

  Hold: When $\overline{HOLD}$ = 0, all the above AGC actions are suspended. The AGC amplifier gain is held constant, except for leakage effects.

The setup in Figure 9 is used to demonstrate the advantage of the FAST REC function. Figures 10 & 11 show the AGC amplifier gain recovery time without and with the FAST REC function, respectively. Without the FAST REC function, the AGC amplifier gain slowly recovers to the 100% nominal level, due to the small decay current. With the FAST REC function, the AGC amplifier gain quickly reaches 125%+. When the FAST REC returns to 0, the attack time is very short. One application of the FAST REC function is immediately after a long hold period during which the gain could have drifted low.

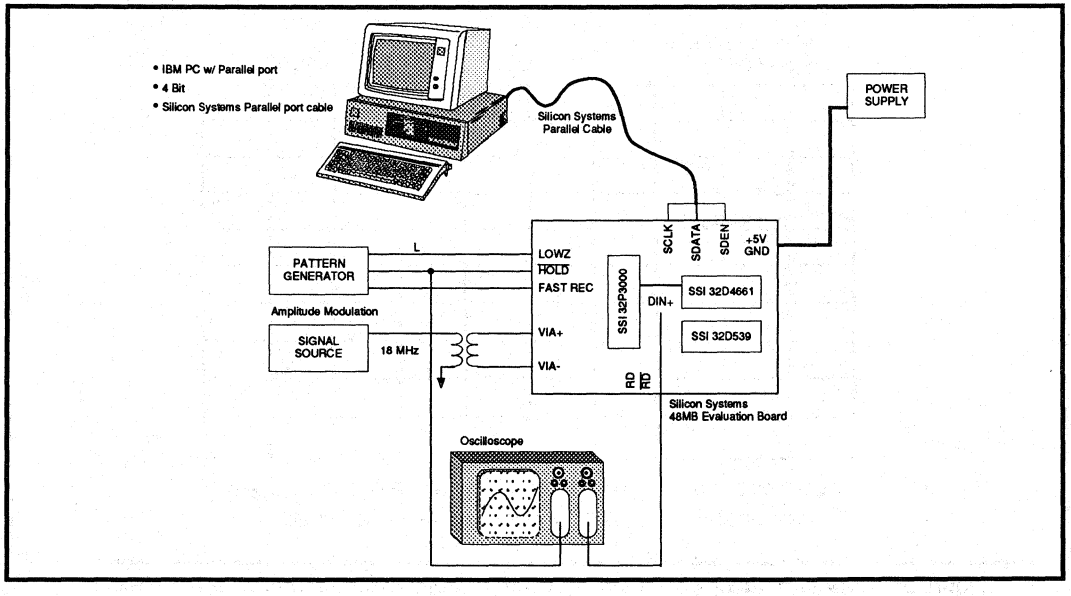

Figure 9: SSI 32P3000 Evaluation Board AGC Recovery Setup

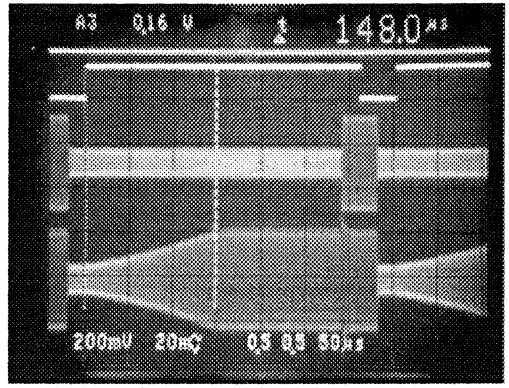

Figure 10: AGC Recovery Without Using FAST REC
FAST REC = 0
$\overline{\text{HOLD}}$
Analog Input: Amplitude Modulated to Simulate Gain Change
DIN±

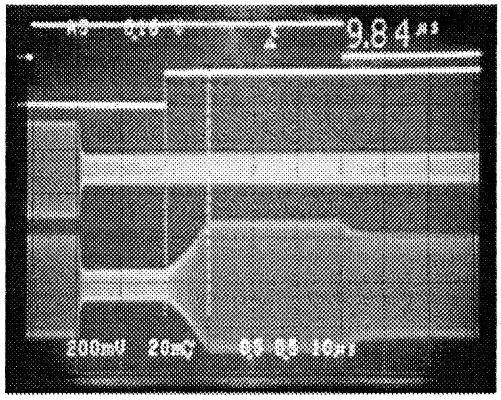

Figure 11: AGC Recovery With FAST REC
FAST REC
$\overline{\text{HOLD}}$
Analog Input
DIN±: Note fast recovery settling to above 100% and attacking at the end of fast recovery

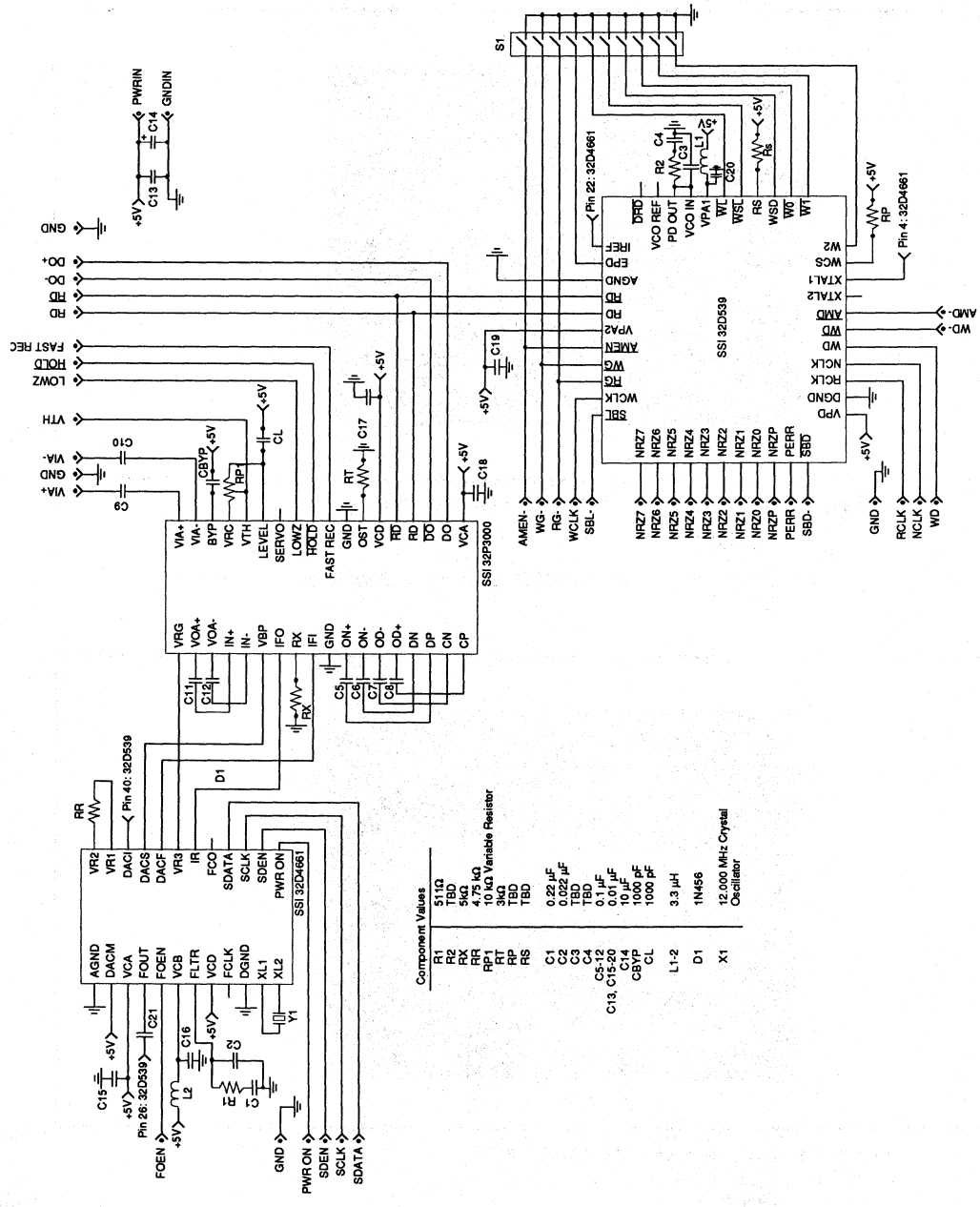

FIGURE 12: SSI 32P3000 / SSI 32D539 / SSI 32D4661 Evaluation Board Schematic

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX: (714) 573-6914

silicon systems®
A TDK Group Company

Using an SSI 32P4730/31/41/42/44/46 Single-Chip Read Channel Device

APPLICATION NOTE

January 1994

INTRODUCTION

Silicon Systems is pleased to introduce the SSI 32P4730/31/41/42/44/46, the highest performance single-chip read channel devices available. These devices contain all the functions needed to implement a complete zoned recording read channel for hard disk drive systems. The functional blocks include a pulse detector, programmable filter, 4-burst servo circuit, time base generator, and a data separator with a 1,7 RLL ENDEC. Refer to the respective data sheets for functional block diagrams. The operating NRZ data rate is programmable from 8 to 27.3 Mbit/s for the SSI 32P4730/31, 16-40 Mbit/s for the SSI 32P4741/44, and 16-48 Mbit/s for the SSI 32P4742/46.

While the SSI 32P4730/44/46 and SSI 32P4731/41/42 provide a 4-burst servo capture circuitry, the distinction is in the servo output form. The SSI 32P4730/44/46 features A+B, A-B and C-D outputs. The SSI 32P4731/41/42 features individual Burst A, B, C and D outputs.

This application note details the operation of all functional blocks of the SSI 32P4730/31/41/42/44/46. This is an abridged version of the application notes, a more detailed note is available upon request. Design notes and evaluation techniques are suggested when applicable. This note is intended to supplement the data sheet. For updated device parameter limits, the user is recommended to refer to the electrical specification.

FEATURES

- **Programmable data rate 8-27 Mbit/s for SSI 32P4730/31, 14-40 Mbit/s for SSI 32P4741/44, and 16-48 for SSI 32P4742/46**
- **Low power dissipation:**
  - **400 mW typ @ 24 Mbit/s and 5V supply for the SSI 32P4730/31**
  - **425 mW typ @ 40 Mbit/s and 5V supply for the SSI 32P4741/44**
  - **<500 mW typ @ 48 Mbit/s and 5V supply for the SSI 32P4742/46**
- **Bi-directional serial port programming**
- **Flexible power management less than 1 mW in complete power down**
- **Wide power supply range 4.5 to 5.5 V**
- **Small footprint 64-pin TQFP package**

PULSE DETECTOR

- **Fast Attack/Decay mode for rapid AGC recovery**
- **Dual rate charge pump for fast transient recovery**
- **Programmable qualification threshold**
- **Low drift AGC hold circuitry**
- **Temperature compensated, exponential control AGC**
- **Wide bandwidth, high precision full-wave rectifier**
- **Dual mode pulse qualification circuitry (user selectable)**
- **CMOS $\overline{\text{RDIO}}$ and PPOL signal output for servo timing support**
- **Internal Low-Z and fast decay timing for rapid transient recovery and AGC acquisition**
- **0.5 ns max pulse pairing**

SERVO CAPTURE

- **4-burst servo capture**
- **Internal hold capacitors**
- **Separate registers for filter cutoff and qualification threshold in Servo mode**
- **Servo AGC level programmable via 4-bit DAC**
- **P4730/44/46 : A+B, A-B and C-D outputs**
- **P4731/41/42 : Burst A, B, C and D outputs**

PROGRAMMABLE FILTER

- **Cutoff frequency programmable from 3 to 9 MHz, within ±10% accuracy (6-18 MHz for 41/42/44)**
- **Boost programmable from 0 to 13 dB**

NOTE: This document serves as a supplement to the data sheet for the device. The user is recommended to refer to the data sheet electrical specifications for performance limits. The information within this document is preliminary. Verification is in progress.

13

Using an SSI 32P4730/31/41/42/44/46 Single-Chip Read Channel Device

FEATURES (continued)

- Matched normal and differentiated outputs
- Constant group delay, within ±2% variation
- Low Z input switch for rapid transient recovery
- No external filter components needed
- < 1% THD

TIME BASE GENERATOR

- Better than 1% frequency resolution
- Up to 75 MHz frequency output
- Independent M and N divide-by counters
- VCO center frequency matched to data synchronizer VCO

DATA SEPARATOR

- Fast acquisition phase lock loop with zero phase restart technique
- Programmable phase detector gain switch for fast acquisition and low jitter.
- Integrated 1,7 RLL encoder/decoder (Dual bit interface for 4742/46)
- Fully integrated Data Synchronizer-no external active devices needed
- Programmable decode window symmetry control via serial port
- Programmable write precompensation with independent early and late shift magnitudes (3-bit)
- Hard and soft sector operation (soft sector not available on the 4742/46)

CONTROL REGISTER MAPPING & SERIAL INTERFACE DESCRIPTION

For flexible system applications, the SSI 32P4730/31/41/42/44/46 features 14 control registers for device configuration. The control words can be loaded to or read back from these registers via the 3-pin serial interface. This section defines the register mapping and the serial interface timing.

Upon power up from no supply voltage state, the control register are at random state, and should be programmed before system operation. The control register contents are retained when the device is powered down to Idle mode, i.e., with $\overline{\text{PWRON}}$ = 1.

COMMAND REGISTER MAPPING

Power Down Control Register Address (A6..A0) = 0000010 = 02_{HEX}

D7 (MSB) - D5		Internal hardwired for factory use only.
D4	= 1 = 0	Time Base Generator is disabled, reducing power dissipation by 100 mW. Time Base Generator is active. (Normal mode)
D3	= 1 = 0	Data Separator is disabled, reducing power dissipation by 120 mW. Data Separator is active. (Normal mode)
D2	= 1 = 0	Programmable Filter is disabled, reducing power dissipation by 100 mW. Programmable Filter is active. (Normal mode)
D1	= 1 = 0	Timebase Generator phase detector gain = 1 X KD. Timebase Generator phase detector gain = 3 X KD (• - Normal mode).
D0 (LSB)	= 1 = 0	Pulse Detector/Servo is disabled, reducing power dissipation by 75 mW. Pulse Detector/Servo is active. (Normal mode).

Data mode Cutoff Register Address (6..A0) = 0000011= 03_{HEX}

D7 (MSB)	= 0	Set to zero
D6..D0		Filter cutoff frequency control in the data Read mode. fc (MHz) = 9 • Code/127 (18 • Code/127 for 41/42/44/46) Maximum code, 1111111 or 127 decimal, represents the maximum 9 MHz cutoff frequency (18 MHz for 41/42/44/46). Minimum code is 42, for 3 MHz cutoff frequency (6 MHz for 41/42/44/46).

Servo mode Cutoff Register Address (A6..A0) = 0010011 = 13_{HEX}

D7 (MSB)	= 1 = 0	TTL $\overline{WD}$ buffer disabled (SSI 32P4742/46 only). TTL $\overline{WD}$ buffer enabled (Normal mode)
D6..D0		Filter cutoff frequency control in the Servo mode.

Filter Boost Register Address (A6..A0) = 0001011 = $0B_{HEX}$

D7 (MSB)	= 1 = 0	Filter boost remains active in the Servo mode. Filter boost is disabled in the Servo mode.
D6..D0		Filter boost control setting Boost (dB) = 20 log [(0.0273 • Code) + 1] Maximum boost, 13 dB, is set with Code = 127 decimal. Minimum code, 0, represents no boost.

Data Threshold Register Address (A6..A0) = 0001010 = $0A_{HEX}$

D7 (MSB)	= 1 = 0	Window Threshold Qualification in Data mode Hysteresis Threshold Qualification in Data mode
D6..D0		Qualification threshold percentage setting in Data mode Qual % = 93% • Code/127 Qual % should be limited between 30% to 80%. Thus, this code should be restricted from 41 to 109.

CONTROL REGISTER MAPPING & SERIAL INTERFACE DESCRIPTION (continued)

Servo Threshold Register Address (A6..A0) = 0010010 = 12_{HEX}

D7 (MSB)	= 1 = 0	Window Threshold Qualification in Servo mode Hysteresis Threshold Qualification in Servo mode
D6..D0		Qualification threshold percentage setting in Servo mode

Control A Register Address (A6..A0) = 0011010 = $1A_{HEX}$

D7 (MSB)	= 1 = 0	Not in fast decay current Test mode (Normal mode) Fast decay current is always turned on, for test use only other AGC actions, such as $\overline{HOLD}$, attack, ... remain active.
D6-5		Test point source select bits, work in combination with Control B Register: D6
D4	= 1 = 0	Frequency synthesizer is bypassed. TBG output = FREF. Frequency synthesizer is active. TBG output = FREF • [(M+1)/(N+1)] (Normal mode).
D3	= 1 = 0	Enables test point MTP3. Test point MTP3 forced to Logic 1 (Normal mode).
D2	= 1 = 0	TBG phase detector pump down state, for test use only. Not in TBG phase detector pump down Test mode (Normal mode).
D1	= 1 = 0	TBG phase detector pump up state, for test use only. Not in TBG phase detector pump up Test mode (Normal mode)
D0	= 1 = 0	TBG phase detector active (Normal mode) TBG phase detector disabled, allowing pump up/down Test modes

Only one bit of {D0, D1, D2} can be set to 1 at any one time. Violation causes indeterminate state.

Control B Register Address (A6..A0) = 0001100 = $0C_{HEX}$

D7 (MSB)	= 0	Set to zero for normal use
D6	= 1 = 0	Enables test points MTP1 and MTP2 Test points MTP1 and MTP2 forced to Logic 1 (Normal mode)
D5	= 1 = 0	Data Separator phase detector pump down state, for test use only Not in Data Separator phase detector pump down Test mode (Normal mode)
D4	= 1 = 0	Data Separator phase detector pump up state, for test use only Not in Data Separator phase detector pump up Test mode (Normal mode)
D3	= 1 = 0	Data Separator phase detector active (Normal mode) Data Separator phase detector disabled, allowing pump up/down Test modes

Only one bit of {D3, D4, D5} can be set to 1 at any one time. Violation causes indeterminate state.

Control B Register (continued)

D2	= 1 = 0	The RDIO pin is an input pin The RDIO pin is an output pin (Normal mode)
D1	= 1 = 0	Data Separator phase detector gain shift is enabled Data Separator phase detector gain shift is disabled (Normal mode)
D0	= 1 = 0	Direct write enabled, i.e., write data bypasses the ENDEC direct write disabled, i.e., write data is encoded before appearing at write data output (Normal mode)

N Counter Register Address (A6..A0) = 0000110 = 06_{HEX}

D7 (MSB)	= X	= 1 Extended 2 µs low-Z write to read recovery = 0 Normal 1 µs low-Z recovery (Normal mode)
D6..D0		7-bit N counter code in Time Base Generator frequency synthesizer. N Counter can be programmed anytime, but becomes effective only after a subsequent Date Rate Register programming.

M Counter Register Address (A6..A0) = 0001110 = $0E_{HEX}$

D7..D0		8-bit M counter code in Time Base Generator frequency synthesizer. Fout = [(M + 1)/(N + 1)] • Fref, Fout = TBG output frequency Fref = Reference frequency @ FREF pin M Counter can be programmed anytime, but becomes effective only after a subsequent Date Rate Register programming.

Data Rate Register Address (A6..A0) = 0000100 = 04_{HEX}

D7 (MSB)	= 1 = 0	Test mode- resets internal flip-flops Normal use (Normal mode)
D6..D0		Per data rate, code sets the VCO center biasing SSI 32P4730/31: IDAC Code = (3 • DR MHz - 3.84)/0.614 SSI 32P4741/42/44/46: IDAC Code = (1.5 • DR MHz - 3.84)/0.614

For 20 Mbit/s (40 Mbit/s for 41/42/44/46) operation, Code = 91, i.e., 1011011

Window Shift Register Address (A6..A0) = 0000101 = 05_{HEX}

D7..D6	= 00 = 01 = 10 = 11	Fc DAC output, i.e., filter cutoff, @ DACOUT Vth DAC output, i.e., qualification threshold, @ DACOUT WS DAC output, i.e., window shift, @ DACOUT WP DAC output, i.e., write precomp, @ DACOUT Selection of early or late DAC is made by the WP enable bit in the Write Precomp Reg.

Note: The DACOUT pin must not be loaded. Loading affects DAC performance.

CONTROL REGISTER MAPPING & SERIAL INTERFACE DESCRIPTION (continued)

Window Shift Register (continued)

D5	= 1 = 0	Window shift function enabled Window shift function disabled
D4	= 1 = 0	Window shift direction: Late Window shift direction: Early
D3-0		4-bit code to set the window shift magnitude. Window Shift % of Data Separator VCO Period = 30% - Code • 2%. For 20% shift, Code = 5, i.e., 0101

Write Precomp Register Address (A6..A0) = 0001101 = $0D_{HEX}$

D7	=1 = 0	High Resolution Peak Detector Reset. Peak detector capacitors are reset at the 0.5 volt baseline. (Normal mode) Low Resolution Peak Detector Reset. Capacitors are reset below the 0.5 volt baseline.
D6..D4		3-bit code to set the write precomp late magnitude.
D3	= 1 = 0	Write Precomp function enabled. Write Precomp function disabled.
D2..D0		3-bit code to set the write precomp early magnitude. The need and direction of write precomp is determined by data pattern. But precomp magnitude is programmable via this register as the following:
	= 000	7 x TS TS = 0.04 •Encoded bit period
	= 001	6 x
	= 010	5 x
	= 011	4 x
	= 100	3 x
	= 101	2 x
	= 110	1 x
	= 111	No Precomp

AGC Level Register Address (A6..A0) = 0100010 = 22_{HEX}

D7..D4		DACP 4-bit code to set peak detector current used to charge the internal 10 pF hold capacitor during the burst acquisition from 6 µA to 96 µA. Code = (I-6 µA)/5.625. For 6 µA code =0, i.e., 0000
D3..D0		4-bit code to set the AGC nominal level at the DP/DN in the Servo mode only. Nominal level at DP/DN = 1 - Code • 0.0153 Vppd For 0.8 Vppd at DP/DN, code = 13, i.e., 1101

SERIAL INTERFACE FORMAT

The SSI 32P4730/31/41/42/44/46 supports a 3-pin serial interface to write to and read from the control registers. The three pins are SDEN which enables/disables a serial transfer, SCLK which synchronizes the transfer, and SDATA which is the bi-directional data pin.

Writing to a Control Register

A data transfer is enabled with SDEN = 1. The data packet is structured as a 16-bit word: '0' for writing + 7 address bits (with LSB first) + 8 command bits (with LSB first). Each rising edge of SCLK clocks the data into a 16-bit shift register. Only the first 16 SCLK rising edges after SDEN becomes 1 are recognized by the serial interface. The SCLK rising edges after the first 16 are ignored. The 16th rising edge loads the command bits into the designated register. If less than 16 clock pulses are provided before SDEN goes low, the data transfer is aborted. Figure 1 illustrates the timing diagram of loading command into a register.

Reading from a Control Register

A control register read is also enabled with SDEN =1. The user must first input the read instruction bit and the register address. The register content is then subsequently clocked out at the SDATA pin. The data packet is structured as: '1' for reading + 7 address bits (with LSB first) + tristate delay + 8 data bits (with LSB output first). Each rising edge of SCLK clocks the instruction bit & the address bits into the device. A falling edge clocks out the register content. Thus, the controller may use the rising edge to receive the data. The SDEN falling edge returns the SDATA pin as an input pin. Figure 2 illustrates the timing diagram of reading from a control register.

It is important to terminate the external source at the SDATA pin within the tristate delay to avoid contention with the output buffer of the SSI 32P4730/31/41/42/44/46.

The SDEN, SCLK and SDATA are schmitt trigger CMOS compatible inputs. The minimum input high threshold is VPD/2 + 0.5V. The maximum input low threshold is VPD/2 - 0.5 V. VPD is the digital +5V power supply. These pins should not be left floating at any time. External pull ups, either through external resistors to VPD or by external source, are required to bias them at a known state.

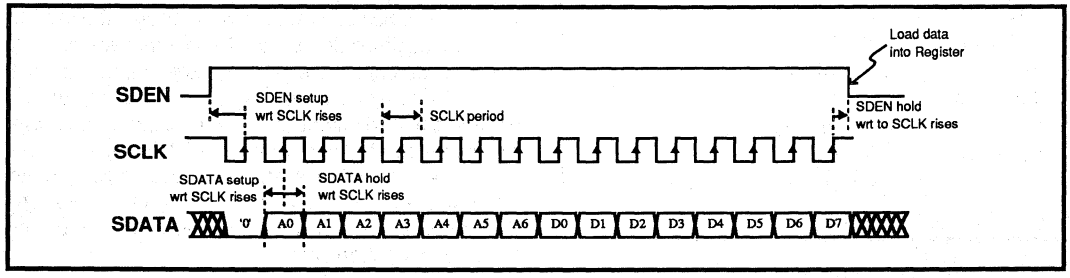

FIGURE 1: Serial Interface Timing Diagram - Writing Control Register

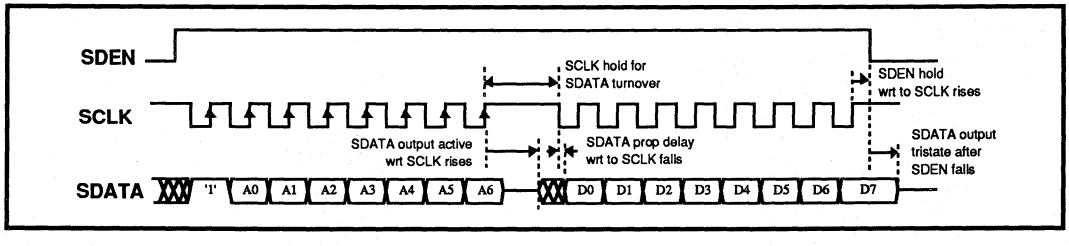

FIGURE 2: Serial Interface Timing Diagram - Reading Control Register

CONTROL REGISTER MAPPING & SERIAL INTERFACE DESCRIPTION

(continued)

REGISTER DECODE TIMING

An important consideration in the use of the serial port is the time taken to decode and change DAC and control settings. The following is a list of nominal decode timings taken for the SSI 32P4730/31/41/42/44/46, actual times are application dependent. These measurements are taken from the 16th rising edge of SCLK to the occurrence of the programmed change.

REGISTER NAME	REGISTER ITEM	DECODE TIME
Power Down	TBG	Power Up = 2 µs
	Data Separator	Power Up = 0.5 µs
	Filter	Power Up = 25 µs
	Pulse Detector	Power Up = 50 µs
Data mode Cutoff	Max *fc* change	<1 µs
Servo mode Cutoff	Max *fc* change	<1 µs
Filter Boost change	Max boost	<1 µs
Data Threshold	Threshold % change	0.3 µs
Servo Threshold	Threshold % change	0.3 µs
Control A	MTP3 enable	0.1 µs
Control B	MTP1,2 enable	0.1 µs
	$\overline{\text{RDIO}}$ input/ output	0.5 µs

MODES OF OPERATION & POWER MANAGEMENT

The SSI 32P4730/31/41/42/44/46 has several Operating modes that support Read, Write, Servo and power management functions. Mode selection is accomplished by controlling the read gate (RG), write gate (WG), servo gate (SG) and PWRON pins. Additional modes are controlled by programming the Power Down Control Register (PDCR), the Control A Register (CAR), and the Control B Register (CBR). This section discusses the controls of each mode. The detailed operating functions are presented in the following the following section.

POWER MANAGEMENT

For optimal overall system power saving, the SSI 32P4730/31/41/42/44/46 allows flexible power down options. With PWRON = 1, the entire device is powered down, except the serial interface and the control register. With PWRON = 0, the device is in Normal Operation mode. Each individual function can be powered down by programming the Power Down Control Register. An important consideration in exercising the power down functions is the recovery time.

The recovery time from a Power Down mode is application dependent. While most of the internal nodes within the device can recover very quickly, the I/O DC bias settling times depend on the external ac-coupling and bypass capacitors. All TTL logic inputs are not affected by any power down state. However, for low power down dissipation, these logic inputs are recommended to logic '1' state. All TTL logic outputs are in high impedance states. These logic outputs return to active state in less than 1 µs after power up. The following are some notes on the other I/Os power down recovery behavior.

I/Os power down recovery behavior

Pin	Nominal Voltage	Power Down Voltage	Typical Recovery Time
VIA±	3.5V	4.0V	2 µs
VOA±	3.5V	4.6V	3 µs
IN±	3.5V	3.9V	5 µs
ON±	2.3V	4.7V	2.8 µs
OD±	2.3V	4.7V	0.5 µs
DP, DN	3.4V	5.0V	6 µs
CP, CN	3.6V	4.6V	12 µs
RX	0.7V	0V	1.5 µs
MTP1,2,3	3.6V	3.6V	350 µs
TFLT±	~ 2V	0V	13 µs loop filter dependent
DFLT±	~ 2V	0V	13 µs loop filter dependent
LEVEL	0.67(Vpp@DP/DN)+2.6V	Leakage effect only	< 1 µs
RR	1.6V	0V	0.5 µs
RTS (Data mode)	3.0V	3.9V	20 µs
RTS (Servo mode)	2.6V	3.9V	0.8 µs
RTD (Data mode)	2.6V	3.9V	0.8 µs
RTD (Servo mode)	3.0V	3.9V	20 µs
A-B	At SREF when Reset	5V	0.5 µs
C-D	At SREF when Reset	5V	0.5 µs
A+B	At SREF when Reset	5V	0.5 µs
BYP	2- 3.5V	Leakage effect only	
MAXREF	3.1V	0V	0.5 µs
A, B, C, D	At 0.5V when Reset	0V	0.5 µs
DACOUT		5.0V	1 µs
$\overline{\text{RDIO}}$, PPOL			1 µs

MODES OF OPERATION & POWER MANAGEMENT (continued)

READ MODE

When $\overline{PWRON}$ = 0, RG = 1, WG = X, and SG = 0, the SSI 32P4730/31/41/42/44/46 is in data Read mode. All the control bits in the Power Down Control Register must be reset to 0.

In the data Read mode, all functions of the SSI 32P4730/31/41/42/44/46, except the servo, are active. The AGC amplifier amplifies the read signal. The low pass filter bandlimits the high frequency noise and applies pulse slimming. The pulse qualifier validates each valid signal peaks. The time base generator provides an internal frequency reference to the data separator at 3X (1.5X for the SSI 32P4741/42/44/46) the NRZ data rate. The data separator phase locked loop is locked onto the read data pulses from the pulse qualifier. The clock is extracted from the data bits. The data is re-synchronized and decoded into NRZ data.

The servo outputs remain valid and are held constant from the previous servo sampling.

WRITE MODE

When PWRON = 0, RG = 0, WG = 1, and SG = 0, the SSI 32P4730/31/41/42/44/46 is in Write mode. At the least the data separator and the time base generator control bits in the Power Down Control Register must be reset to 0.

In the Write mode, the SSI 32P4730/31/41/44/46 accepts the NRZIN input at each rising edge of the WCLK. The data is encoded into 1,7 RLL codes, unless the ENDEC bypass is chosen for direct write. Write precompensation, if enabled, is applied to selected data pattern. The coded data is re-synchronized at the WD output by the internal data separator reference clock.

The pulse detector and programmable filter are not used in the Write mode. The AGC amplifier gain is held constant at prior to entering the Write mode. The servo outputs remain valid and are held constant from the previous servo sampling.

SERVO MODE

When PWRON = 0, RG = X, WG = X, and SG = 1, the SSI 32P4730/31/41/42/44/46 is in Servo mode. At the least, the pulse detector/servo and the programmable filter control bits in the Power Down Control Register must be reset to 0.

While the SSI 32P4730/44/46 and the SSI 32P4731/41/42 feature different servo outputs, all share the same servo sampling sequence in operation. In the Servo mode, the AGC amplifier remains active. A servo AGC pattern should be provided for servo AGC with the HOLD input at '1'. With the HOLD input at '0', the AGC amplifier gain is held constant. The servo A, B, C and D bursts are sampled and captured.

The servo operation, with the distinctions between the SSI 32P4730/44/46 and the SSI 32P4731/41/42, is detailed in the following section.

READ MODE EVALUATION

As a single-chip read channel IC, the SSI 32P4730/31/41/42/44/46 supports many functions in Read mode alone. This section discusses the functions of the various blocks. Where appropriate, lab experiments are suggested in evaluation.

PULSE DETECTOR FUNCTION

The pulse detector is the first block in the block diagram of the SSI 32P4730/31/41/42/44/46. It amplifies, validates and time-preserves the read signal from a read/write pre-amp, such as the SSI 32R2020. The pulse detector block includes the wideband AGC amplifier, the AGC control circuitry, the 7-pole programmable low pass filter, and the pulse qualifier.

AGC AMPLIFIER & CONTROL

The wideband AGC amplifier accepts a low amplitude read signal, typically <200 mVppd, and amplifies it to a larger amplitude prior to pulse qualification. Because of varying head-to-media conditions, the amplifier gain is automatic-gain controlled to provide a 1 V_{ppd} signal at the DP/DN pins. The amplifier gain is an exponential function of the voltage at the BYP pin. For reference use only, the gain function is $Av = 12 \exp\{2.5 (V@BYP + 2.15 - VPA)\}$. Internal clamp circuitry clamps the BYP pin voltage between ~2.0V and ~3.5V. The clamp resistance is <10Ω. It is advised not to sink or source more than 3 mA at the BYP pin.

The AGC actions are current charging and discharging the external BYP integrating capacitor to maintain a 1 V_{ppd} at the DP/DN pins. They are described as follow:

- **Slow Decay**

  When the instantaneous DP/DN signal is below 1 Vppd, a slow decay current, 4.0 uA, charges the BYP capacitor. The AGC amplifier gain is increased slowly.

- **Slow Attack**

  When the instantaneous DP/DN signal exceeds 1 Vppd, but is below 1.25 Vppd, a slow attack current, 0.18 mA, discharges the BYP capacitor. The AGC amplifier gain is decreased.

- **Fast Attack**

  When the instantaneous DP/DN signal exceeds 1.25 Vppd, the device enters a Fast Attack mode. A fast attack current, 1.26 mA, discharges the BYP capacitor. The AGC amplifier gain is quickly lowered.

- **Write-to-Read Recovery**

  With a 1-to-0 transition of the WG, the SSI 32P4730/31/41/42/44/46 enters the Write-to-Read Recovery mode. The input impedance remains in low impedance state for 1 µs for fast input DC coupling recovery. Then, the device restores to high input impedance state, and enters into a Fast Decay mode. In the Fast Decay mode, a continuous high current quickly charges the BYP capacitor until the signal at DP/DN exceeds 125% of nominal. After reaching 125%, the high current is disabled and the slow attack sequence commences. (Otherwise only the Slow Decay mode is available to increase the AGC amplifier gain.) Figure 3 shows the write-to-read AGC action timing. This same sequence is executed when the device switches from Power Down to Power Up mode.

- **Read-to-Servo, Servo-to-Read Recovery**

  With a 1-to-0 or 0-to-1 transition of the SG, the SSI 32P4730/31/41/42/44/46 enters a HOLD/Fast Decay mode time period as set by the Low-Z time bit in the N-Counter Register. When bit D7 = 0 and there is a transition of SG, the AGC enters a HOLD mode for 0.4 µs. Following the HOLD period, the AGC enters a Fast Decay mode until the signal at DP/DN exceed 125% of the level set by the SERVO AGC Level register in Servo mode, or 1 Vpp in Data mode. If the signal does not reach 125% within the timeout period, as set by the Low-Z time bit in the N-Counter Register, nominally 1 µs, the fast decay sequence ends and normal AGC actions are reinstated.

All the AGC actions are suspended in any one of the following conditions:

- HOLD = 0, or
- Write mode.

The AGC amplifier gain is then held constant, except for leakage effect.

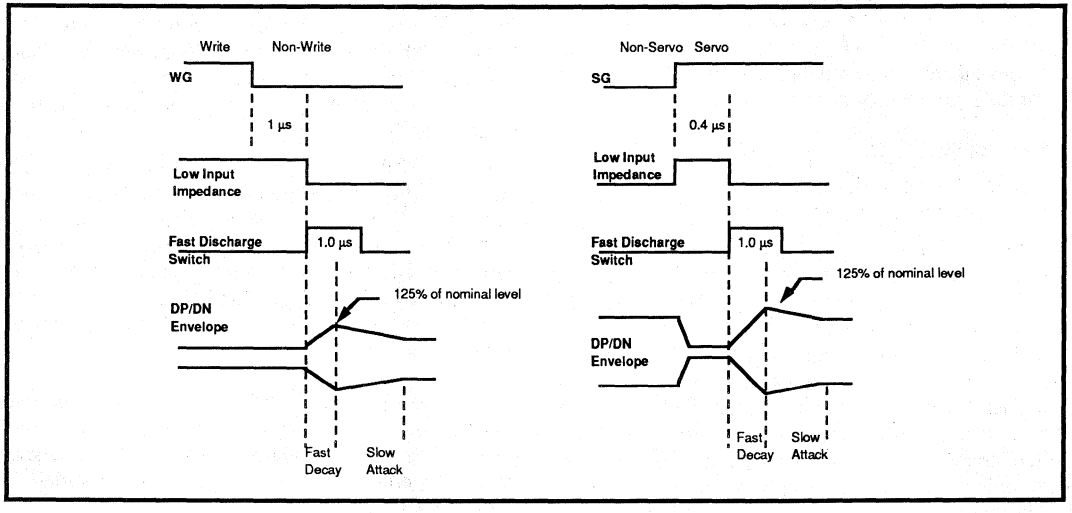

FIGURE 3: AGC Action Timing In Recovery

READ MODE EVALUATION (continued)

Low Pass Filter Function

From the head/media point to the AGC amplifier output, the signal path should have very wide bandwidth, and is therefore noisy. To reduce false pulse qualification, the SSI 32P47XX includes a 7-pole 0.05° phase equiripple programmable low pass filter to reject noise beyond the signal frequency of interest. In addition, this filter provides pulse slimming equalization for improved pulse pairing performance. Ideal for zoned bit recording applications, the filter bandwidth and the pulse slimming equalization are both programmable through the serial port. The filter's normal low pass output, ON±, is the input to the pulse qualifier.

An additional function of the filter is to provide a time differentiated signal of the read data, i.e., 90° phase lead. Each read data peak is translated into a zero-crossing at the OD±. This time differentiated output is used in time qualification as described in the next topic.

The control and the dynamics of the filter are discussed in the following sections.

Pulse Qualifier Function

The pulse qualifier transforms each valid analog read data pulse into a digital pulse, while preserving the relative time position of each valid pulse peak. Each DP/DN pulse is validated by a combination of level qualification and time qualification. The SSI 32P47XX supports two methods of level qualification: window threshold qualification and hysteresis qualification. In time qualification, the time differentiated filter output is used to locate the signal peaks in time.

Level Qualification

The two options in level qualification are: window threshold qualification and hysteresis qualification.

Window Threshold (Dual Comparator) Qualification: When in window Threshold Qualification mode, independent positive and negative threshold qualification comparators are used. A slight amount of local hysteresis is included to increase the comparator output time when a signal that just exceeds the threshold level is detected. This eases the timing with respect to the zero crossing clock comparator. Any peak, regardless of polarity, which exceeds the programmed threshold level triggers the read data one-shot. Qualification thresholds from 10% to 80% may be set with a resolution of 1%. A parallel R-C network of RTD and CT set the hysteresis threshold time constant when not in the Servo mode.

Hysteresis Qualification: When the Hysteresis Qualification mode is selected, the same Threshold Qualification mode is selected, the same threshold qualification comparators and clock comparators are used to implement a polarity checking rule. In this mode, a positive peak that clears the established threshold level will set the hysteresis comparator and trigger the bidirectional one-shot that creates the read data pulses. In order to get another pulse clocked out, a peak of the opposite polarity must clear negative threshold level to reset the hysteresis comparator and trigger the bidirectional one-shot.

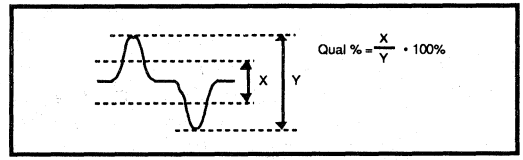

FIGURE 4: Qualification Percentage Definition

Qualification threshold in percentage is defined to be the distance between the positive threshold and the negative threshold as a percentage of the DP/DN peak-to-peak. The SSI 32P47XX has a 7-bit DAC to allow flexibility in qualification % setting through serial port programming, with better than 1% resolution.

Qualification Percentage = 93% • DAC Code/127.

Because the qualification percentage should be between 30% to 80%, the DAC Code must be limited between 41 and 109, in decimal. Operation outside of this range may result in qualification percentage setting inaccuracy.

The qualification threshold DAC can accept its 7-bit input code from one of two registers, Data Threshold Register or Servo Threshold Register, depending on the Operation mode. Thus, the qualification percentage can be set separately for the normal data Read mode and the Servo mode. The MSB bit (D7) of each register selects the level qualification method, either window threshold or hysteresis.

Qualification Threshold Time Constant: Because the qualification threshold is set as a percentage of the pulse qualifier input's peak-to-peak swing, this threshold can track with any long term signal amplitude variation at the DP/DN input.

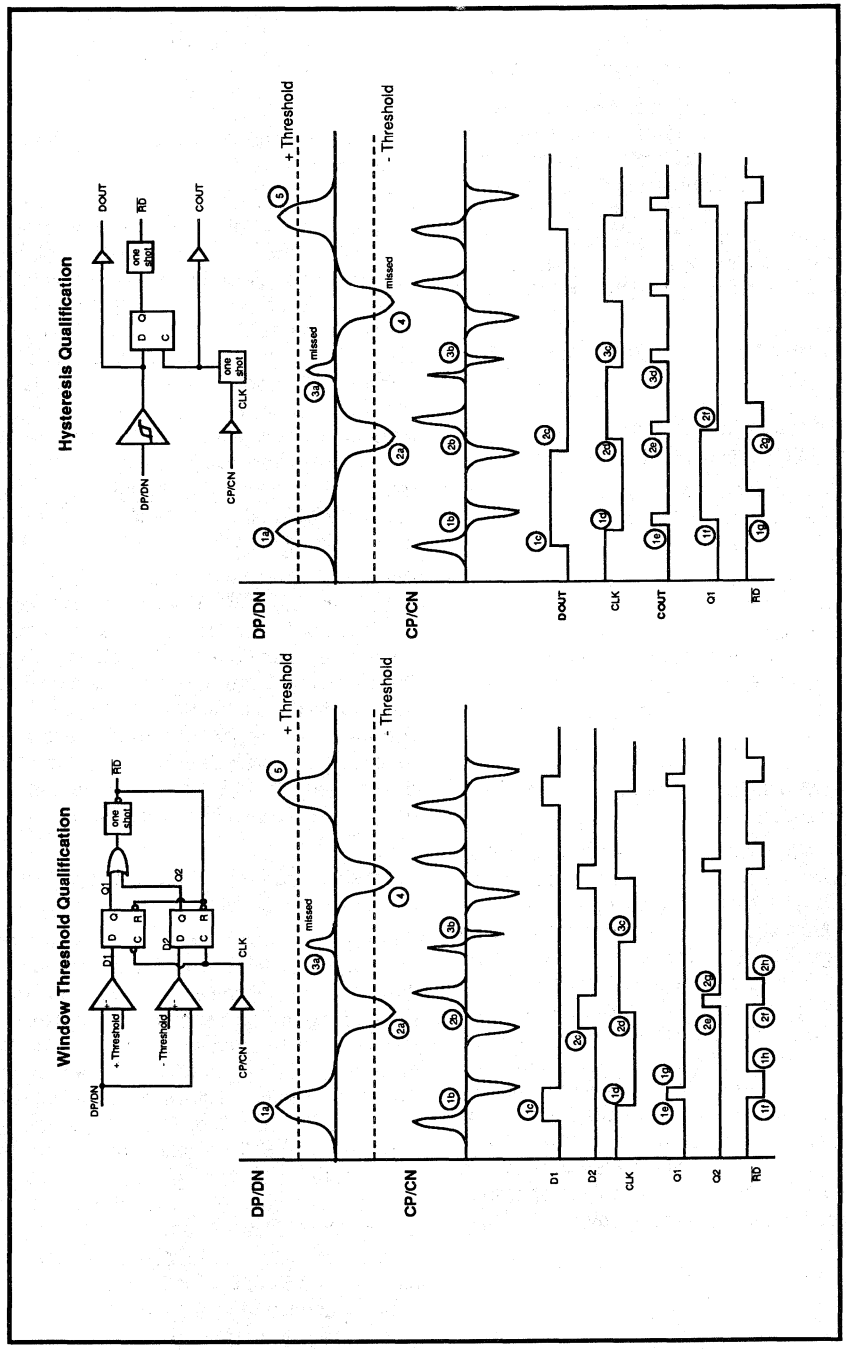

FIGURE 5: Window Threshold Qualification & Hysteresis Qualification

READ MODE EVALUATION (continued)

Qualification Threshold Time Constant (continued)

An external R-C network, with an internal 50 µA pull down current source, from the LEVEL output to the RTD pin (or the RTS pin for Servo mode) determines the tracking time constant. During the AGC Fast Decay mode, there is an internal 1.8 mA pull-down current to discharge the capacitor at LEVEL. The advantage of this function is to allow the qualification voltage to be set after the AGC has settled, guaranteeing that it is not set too high.

There are two constraints in determining this R-C time constant:

- This time constant should not be too small such that the threshold may track the noise.
- This time constant should not be too large such that reasonably lower amplitude pulses are not qualified.

Both constraints are system dependent, specifically the head/media combination. The user must determine these limits. However, it is accurate to say that the time constant should be smaller than that of the AGC loop. Otherwise, the AGC loop will restore 1 Vppd at the DP/DN input, and this defeats the purpose of the tracking threshold.

Lab Experiment 6.1 Pulse Detector Qualification Threshold Time Constant

The SSI 32P47XX supports a tracking qualification threshold in pulse detection. Given a change in input signal amplitude, at a rate faster than the AGC loop can respond, the qualification threshold can remain as a fixed percentage of the signal level, if its time constant is set properly. This qual threshold time constant is determined by an external R-C network between the LEVEL pin and the RTD (or RTS) pin, with an internal 50 µA pull down current at the LEVEL pin. Because the LEVEL voltage is the reference voltage for the internal 7-bit threshold setting DAC, the percentage difference in (V@LEVEL - RTD) is the same as the qualification threshold voltage. The key point is then to allow the LEVEL voltage track with any change in signal amplitude with the two constraints discussed above.

For this experiment, the AGC time constant is made artificially large with a 0.01 uF BYP capacitor. This is to suppress the AGC action to emphasis the qualification threshold time constant effects.

What would happen if the qualification threshold time constant is too large?

A 0.033 µF capacitor is connected between the LEVEL pin and the VPG pin. The resistor is omitted, but the internal pull down current provides a discharge path. With 50 µA discharge current, the maximum decay rate at the LEVEL pin is 50 µA/0.033 µF = 1.52 mV/µs. Nominally, the LEVEL voltage is at 0.65V above the RTD(RTS) voltage. Thus, the percentage change rate of the qualification threshold voltage is 1.52/650 x 100% per µs = 0.24%/µs. (The actual qualification percentage change is then 0.24%/µs x Set Qual Level. If the qualification level is set at 50%, for example, the qualification percentage change rate is 0.12%/µs.) If the DP/DN signal changes faster than this rate, the qualification threshold may not stay at 50% level.

Photo 1A shows the dynamic input signal, the LEVEL voltage and the $\overline{\text{RDIO}}$. The input signal changes gradually from 100 mVppd to 40 mVppd, and remains at 40 mVppd for 10 µs. The qualification level is set at 50%. Because of the large time constant, the LEVEL voltage does not track with the input amplitude. The qualification threshold remains at 50% of the larger input signal. As a result, the pulses of 40 mVppd are not qualified and missed. Photo 6.1.2 shows the same signal dynamics with a 330 pF capacitor from the LEVEL pin to the VPG pin.

What would happen if the qualification threshold time constant is too small?

To exaggerate the effects, no external capacitor, except parasitics from scope probe, is placed between the LEVEL pin and the VPG pin. As shown in Photo 1A, the input signal has a sequence of 100 mVppd pulses, followed by a '0' period for 500 ns and two weak pulses of 20 mVppd. The qualification level is set at 50%. Should the threshold stays rigid, the two weak pulses would not be qualified. Because of the small time constant, the LEVEL voltage varies very rapidly with the instantaneous input signal. The qualification threshold drops very quickly. As a result, the two weak pulses are qualified. Photo 6.1.4 shows the same input dynamics, but with a 330 pF capacitor across the LEVEL pin and the VPG pin. The LEVEL voltage is kept to a small change during the 500 ns period. The weak pulses are not qualified.

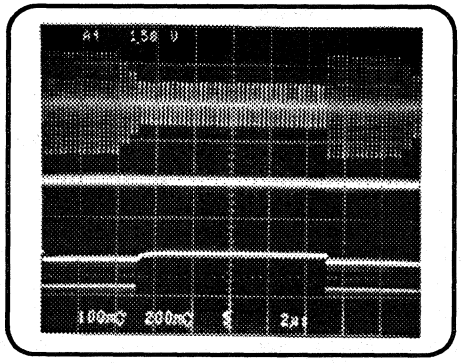

PHOTO 1A: Qualification threshold at 50%; 0.33 µF from LEVEL to VPG. Input changes from 100 mVppd. Large qual threshold time constant >> Missing RDIO pulses.

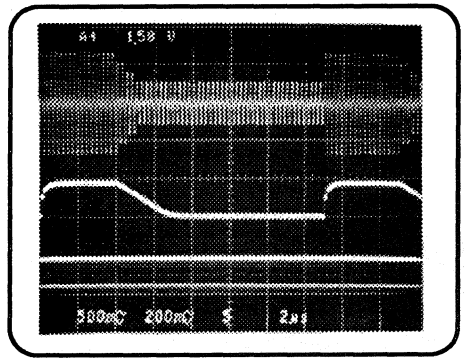

PHOTO 1B: Qualification threshold at 50%; 330 pF from LEVEL to VPG. Input changes from 100 mVppd. Proper qual threshold time constant >> All RDIO pulses present.

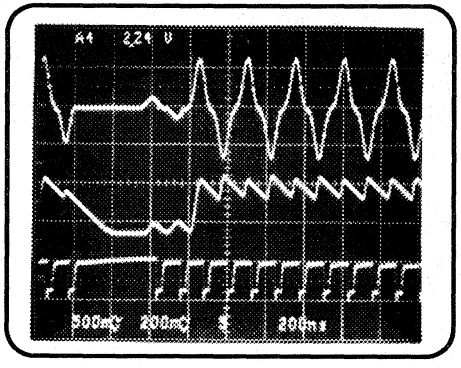

PHOTO 1C: Qualification threshold at 50%; no cap from LEVEL to VPG. Input with "noise blips" at 20% amplitude. Small qual threshold time constant >> False trigered RDIO pulses.

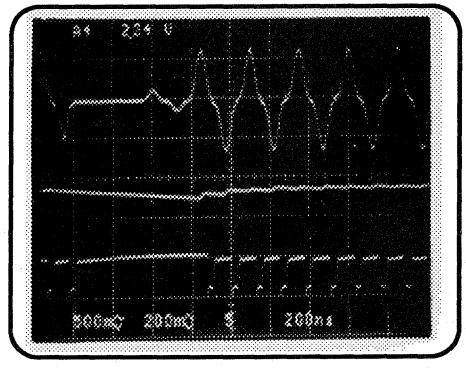

PHOTO 1D: Qualification threshold at 50%; 330 pF from LEVEL to VPG Input with "noise blips" at 20% amplitude. Proper qual threshold time constant >> No false trigered RDIO pulses.

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READ MODE EVALUATION (continued)

PULSE DETECTOR I/O & TEST POINTS

An excellent troubleshooting aid is to know the inputs, the outputs and the available test points. For the pulse detector portion, this is a list of the related pins:

NAME	TYPE	DESCRIPTION
VIA±	I	Differential analog input to the AGC amplifier: The input should be ac-coupled from the source. The input amplitude should be limited to between 20 mVppd to 240 mVppd when no boost is applied at the filter. When boost is applied, the input amplitude should be lowered, as not to exceed the dynamic range of the AGC amplifier and the filter. The DC bias voltage is approximately 3.5V.
VOA±	O	Differential analog output of the AGC amplifier: The output should be ac-coupled to the the filter input. In a closed AGC loop, its amplitude depends on the filter cutoff and boost setting. The DC bias voltage is approximately 3.5V.
BYP	I	AGC amplifier gain control pin: The input voltage controls the AGC amplifier gain. An integrating capacitor should be connected from the BYP pin to VCC. This voltage should be between 2V to 3.5V.
$\overline{\text{HOLD}}$	I	TTL logic input: When $\overline{\text{HOLD}}$ = 0, the AGC amplifier gain is held constant. When $\overline{\text{HOLD}}$ = 1, or left open, the AGC loop is active.
IN±	I	Differential analog input of the filter: The DC bias voltage is approximately 3.5V. The VOA± should be ac-coupled to this input.
ON±	O	Differential normal low pass filter output: This output should be ac-coupled to the DP/DN input. It is simply the filtered version of the IN±. In a closed AGC loop, it should be ~ 1 Vppd. The filter has a nominal gain of 2.0V/V in the passband. However, the gain can be higher at frequency where boost is applied. The DC bias voltage is approximately 2.3V.
OD±	O	Differential differentiated low pass filter output: This output should be ac-coupled to the CP/CN input. It is the bandlimited time differentiated version of the IN±. Every peak (positive or negative) is translated into a zero crossing. Its amplitude is frequency dependent. The DC bias voltage is approximately 2.3V.
DP/DN	I	Differential input to the pulse qualifier: The ON± should be ac-coupled to this input. The DC bias voltage is approximately 3.6V.
CP/CN	I	Differential input to the time qualifier: The OD± should be ac-coupled to this input. The DC bias voltage is approximately 3.6V.
RDIO	I/O	Read data I/O pin: This is a bi-directional TTL compatible pin. When Control B Register D2 = 1, the $\overline{\text{RDIO}}$ is an input pin for the data separator. When the Control B Register D2 = 0, the $\overline{\text{RDIO}}$ is an output pin. When this pin is configured as an output pin and both RG = WG = 0, the $\overline{\text{RDIO}}$ represents the pulse detector read data output. A pulse is generated for every qualified peak. With either RG or WG being 1, the $\overline{\text{RDIO}}$ is held at static 1.
PPOL	I/O	Pulse polarity indicator: This is an optional TTL output indicating the polarity of the input pulse. A positive qualified pulse puts a logic '1' at the PPOL output. A negative qualified pulse puts a logic '0' at the PPOL output. This output is enabled when RG = WG = 0.

PULSE DETECTOR I/O & TEST POINTS (continued)

NAME	TYPE	DESCRIPTION
DACOUT	O	Multiplexed DAC output: When Window Shift Register (05 HEX): D7-6 = 01, DACOUT represents the qualification threshold setting DAC output. The qualification threshold DACOUT voltage can be estimated to be about 4.96 - (0.0129 x DACVth) Volts, where DACVth is equal to the 7 bit register value of the pulse detector qualification threshold in data or Servo mode
MTP1-3	–	Open emitter output test points: These test points are governed by the following logic control.

	Control B Reg			Control A Reg		
	D6	D5	D6	MTP1	MTP2	MTP3
	0	0	X	1	1	1
	0	1	X	1*	1*	1*
	1	0	0	VCO REF	DS-IN	SRD
	1	0	1	RD	DOUT	DSREF
	1	1	0	PDQ	$\overline{PUQ}$	SRD
	1	1	1	SET	RESET	NCTR

VCO REF	I	= reference input to the data synchronizer phase detector, VCO REF = VCO /2(= VCO for 4741/42/44)
DS-IN	I	= input to data synchronizer in Read mode, this is the delayed read data. In non Read mode, this is the output of the time base generator/2 (/1 for 4741/42/44)
DS REF	O	= reference frequency to the data separator, i.e., time base generator output
N CTR	I	= time base FREF divided down signal, an input to the time base phase detector
RD	I	= Read data output of the pulse detector, i.e., input to the 1/3 cell delay
DOUT	O	= output of the data comparator in hysteresis qualification
SET	O	= output of the positive threshold comparator in window threshold qualification
RESET	O	= output of the negative threshold comparator in window hreshold qualification
SRD	I	= Synchronized Read Data, qualified pulses sychronized to the DS VCO, input to the Decoder
PDQ	–	= Data Separator Phase Detector pump down edge, for testing use
$\overline{PUQ}$	–	= Data Separator Phase Detector pump up edge (inverted), for testing use
1	–	= logic 1
1*		= logic 1, but with slightly higher power dissipation

READ MODE EVALUATION (continued)

PULSE PAIRING

Pulse pairing causes decode window margin degradation. In pulse detection, each signal peak, positive or negative, transforms into a digital pulse. Due to comparator offset in the time channel qualification, a positive peak and a negative peak may be detected with a slight time skew. Pulse pairing is defined in Figure 6.

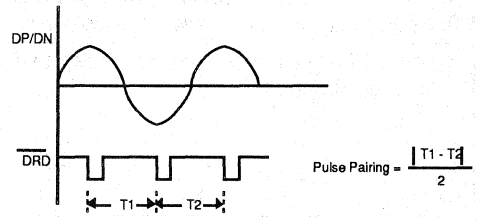

FIGURE 6: Pulse Pairing Definition

Lab Experiment 2 Pulse Pairing

Pulse pairing degrades the decode window margin the most when the decode window is the smallest, i.e., the highest data rate. Pulse pairing is expected to be worse with signal having slower slew rate at the qualification thresholds. This lab experiment examines the pulse pairing with a 2.25 MHz sinusoidal input, i.e., the lowest frequency signal of 24 Mbit/s operation. A 1 Vppd sine wave is fed directly into DP/DN at 2.25 MHz, the same signal is fed into CP/CN with a 90° phase-lead, and filtered to remove 2nd and 3rd harmonics. With a time interval analyzer, the distance between successive pulses at the RD is "histogram-ed". The histogram will include the effect of pulse pairing from the pulse detector. While the jitter is gaussian distributed, the pulse pairing is a systematic error for a given part. When significant pulse pairing is present, the historgram would show a bi-modal distribution with two peaks. In a jitter dominant distribution, the insignificant pulse pairing would be unobservable.

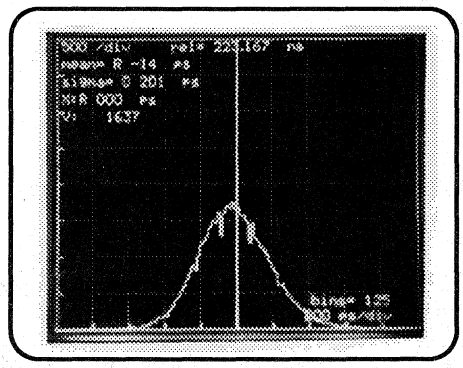

PHOTO 1E: Time Distribution of RD with 2.25 MHz sinusoidal input. Guassian distribution - no bi-modal distribution. Noise jitter - 201 ps; Pulse pairing < 0.05 ns.

Higher frequency read data signals produce faster transitions through zero at the CP/CN inputs. This reduces the effect of any offset at the clock comparator. Pulse slimming equalization emphasizes the high frequency components of the input signal which leads to less pulse pairing.

PROGRAMMABLE FILTER CHARACTERISTICS

The SSI 32P4731/31/41/42/44/46 features a on-chip programmable 7-pole 0.05° phase equiripple low pass filter/equalizer. This filter serves three functions: (1) noise limiting low pass filter of the read data signal, (2) time differentiating the read data signal for signal peak location, and (3) high frequency boost for pulse slimming equalization. The cutoff frequency, to be defined below, is programmable from 3 MHz to 9 MHz(6 to 18 MHZ for SSI 32P4741/42/44/46). The boost function can be programmed up to 13 dB. Both functions are controlled by command registers programmable via the serial interface.

The cutoff frequency, fc, is defined to be the -3 dB bandwidth with no boost. When finite boost is applied, the effective -3 dB bandwidth is higher than the cutoff frequency. Table 2 lists the bandwidth increase vs the applied boost.

Table 1 Filter Bandwidth Increase vs Boost

Boost (dB)	New -3dB Bandwidth / Cutoff Frequency	Boost (dB)	New -3dB Bandwidth / Cutoff Frequency
0	1.00	7	2.42
1	1.21	8	2.51
2	1.50	9	2.59
3	1.80	10	2.66
4	2.04	11	2.73
5	2.20	12	2.80
6	2.32	13	2.86

The high frequency boost is defined to be the amount of magnitude rise at the cutoff frequency, relative to the original -3 dB point. A 13 dB boost would mean a 10 dB peaking above the passband.

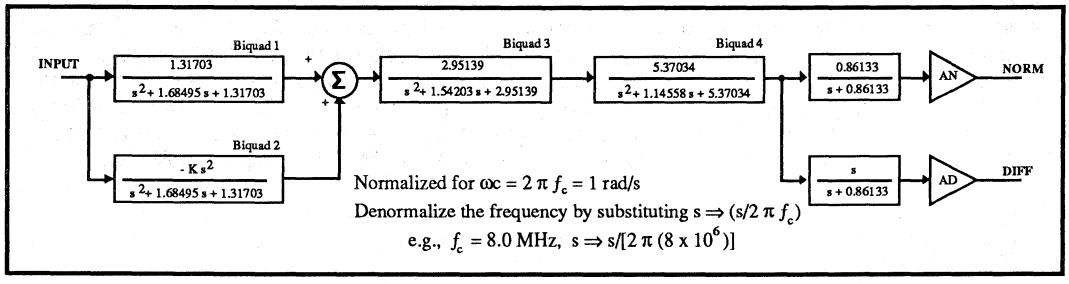

FIGURE 7: Programmable Filter Normalized Transfer Function
AN = 1.17 and AD = 1.51 for unity gain (0 dB) at 0.67 f_c
K varies from 0 to 4.57 for boost up to 13 dB, where
Boost (dB) = 20 log 0.759284 (1.31703 + K)

Figure 7 shows the normalized transfer function of the programmable filter. As a 0.05° phase equiripple filter, the group delay variation is minimal within the passband and up to ~ 2 x fc. One fact not denoted in the transfer function diagram is that the DIFF± output is delayed by 1.2 ns relative to the NORM±. This is to ensure sufficient data setup time for a flip-flop in the pulse qualifier.

An 1% 12.1 kΩ resistor and a 0.01 µF are needed from the RX pin to ground for filter biasing.

READ MODE EVALUATION (continued)

CUTOFF CONTROL

For optimized signal-to-noise performance in a zoned recording application, the SSI 32P4731/31/41/42/44/46 provides a programmable low pass filter. The filter cutoff frequency is programmable from 3 MHz to 9 MHz(6 to 18 MHZ for4741/42/44) by the fc DAC, an on-chip 7-bit DAC. In any non-Servo mode, i.e., SG = 0, the Fc DAC is controlled by the Data mode Cutoff Register. In the Servo mode, i.e., SG = 1, the fc DAC is controlled by the Servo mode Cutoff Register. This allows immediate bandwidth adjustment switching between data Read and Servo modes.

The filter cutoff frequency is determined as: fc (MHz) = 9 • Code/127 (18•Code/127 for SSI 32P4741/42/44/46). In general, the cutoff frequency should be set to about the maximum signal frequency at the given data rate. However, the user should optimize the filter cutoff setting for a given head/media system combination.

BOOST CONTROL

For pulse slimming application, the programmable filter allows high frequency boost equalization. The filter boost is programmable from 0 to 13 dB by the Fb DAC, an on-chip 7-bit DAC. The Fb DAC is controlled by the lower 7 bits of the Filter Boost Register. In the Servo mode, i.e., SG = 1, the boost can be enabled/disabled by the MSB of this control register.

The filter boost is set as: Boost (dB) = 20 log [(0.0273 • Code) + 1]. This boost setting should be optimized for lowest bit error rate for a given head/media system combination.

Lab Experiment 3 Programmable Filter Frequency Response.

In zoned bit recording application, the data transfer rate increases from the inner zone toward the outer zone. For optimized signal-to-noise performance, the accuracy in setting the programmable cutoff and boost is critical. This lab experiment is to examine the filter's magnitude and group delay response.

Magnitude & Group Delay Frequency Response

With a network analyzer, the frequency response of the SSI 32P4731/31/41/42/44/46 programmable filter can be swept very easily. The sweeping source is applied to the filter input directly. The filter output is returned to the network analyzer for magnitude & group delay response analysis. One note is that the source signal must be kept small enough such that its output is within 1 Vppd at all time, not to exceed the dynamic range. The filter has a nominal gain of 2 V/V without boost applied. When maximum 13 dB boost is applied, the input source should be kept below 150 mVppd. For this experiment, the input source is set to 100 mVppd. Furthermore, the device is in Idle mode. The Fc DAC is controlled by the Data mode Cutoff Register.

BANDWIDTH CONTROL SWITCH FROM DATA MODE CUTOFF REGISTER TO SERVO MODE CUTOFF REGISTER

To support system application flexibility, the SSI 32P4730/31/41/42/44/46 allows automatic filter bandwidth switch from the Data Read mode to the Servo mode. When SG = 0, the cutoff control is from the Data mode Cutoff Register. When SG = 1, the cutoff control is from the Servo mode Cutoff Register. In the Servo mode, when the boost is enabled by the MSB of the Filter Boost Register, the same boost setting is used as in the data Read mode. The boost function can be disabled in the Servo mode by setting the MSB to 1.

However, there is no easy way to monitor bandwidth change in the frequency domain following a SG transition. One method to assess the bandwidth switching time is measure the settling time of the filter output amplitude, which is caused to change due to bandwidth switching. This experiment is done as follows:

- Program the Data mode Cutoff Register to 127, i.e., 9 MHz fc in Data Read mode,
- Program the Servo mode Cutoff Register to 42, i.e., 3 MHz fc in Servo Read mode,
- Program the Filter Boost Register to 127, and boost disabled in Servo mode,
- Input a 100 mVppd @ 9 MHz signal,
- Stay in data Read mode for 10 µs, with AGC loop active,
- Remain in Data Read mode for 5 µs, with AGC gain held constant,
- Switch to Servo mode,
- Observe the filter output amplitude change, because input frequency is out of servo cutoff.
- Return to data Read mode and activate the AGC loop.

Photo 1F shows the SG transition and the filter output amplitude change. After the SG 0-to-1 transition, the filter output amplitude settles in 320 ns.

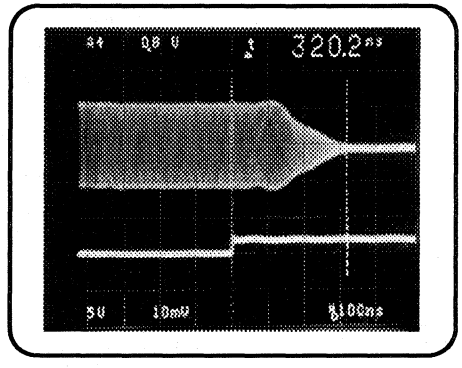

PHOTO 1F: SSI 32P4730/31 Filter Control Switching from Data Mode to Servo Mode

READ MODE EVALUATION (continued)

Programmable Filter I/O & Test Points

In troubleshooting the programmable filter, the following I/O and test points should be examined:

IN±	Differential analog input of the filter: The DC bias voltage is approximately 3.5V. The AGC amplifier output, VOA±, should be ac-coupled to this input.
ON±	Differential normal low pass filter output: This output should be ac-coupled to the DP/DN input. It is simply the filtered version of the IN±. In a closed AGC loop, it should be ~ 1 V_{ppd}. The filter has a nominal gain of 2.0V/V in the passband. However, the gain can be higher at frequency where boost is applied. The DC bias voltage is approximately 2.3V.
OD±	Differential differentiated low pass filter output: This output should be ac-coupled to the CP/CN input. It is the bandlimited time differentiated version of the IN±. Every peak (positive or negative) is translated into a zero crossing. Its amplitude is frequency dependent. The DC bias voltage is approximately 2.3V.
RX	Reference resistor pin: An external 1% 12.1 kΩ resistor and a 0.01 µF capacitor should be connected from this pin to ground. The voltage at this pin is proportional to absolute temperature. At room temperature ambient, this voltage is typically measured to be 700 mV.
DACOUT	Multiplexed DAC output: When Window Shift Register (05 HEX): D7-6 = 00, DACOUT = fc DAC. The voltage at DACOUT in this mode can be estimated to be 0.7 +(0.006425 • $DACF_c$) where $DACF_c$ is the 7-bit register value of filter cutoff frequency in data or Servo mode.

TIME BASE GENERATOR FUNCTIONALITY

The SSI 32P4731/31/41/42/44/46 includes a time base generator to support the variable data rate in a zoned recording application. The data separator VCO requires a 3X (1.5X for SSI 32P4741/42/44/46) data rate reference frequency (not to be confused with FREF, which is reference to the time base generator). Thus, for 24 Mbit/s operation, a 72 MHz (36 MHZ for SSI 32P4741/42/44/46) reference is needed to the data separator. The time base generator provides such a stable reference frequency.

The SSI 32P4731/31/41/42/44/46 time base generator is a phase locked loop based frequency synthesizer, Figure 6.4.1. If Control A Register: D4 = 0, the time base generator output, Fout, is made programmable by loading two divide-down factors achieving better than 1% resolution up to 75 MHz. If the Control A Register: D4 = 1, the frequency synthesizer is bypassed. The time base generator output is at the same frequency as FREF. FREF should be limited between 8 MHz to 20 MHz.

In the frequency synthesizer Active mode, Fout = FREF • [(M + 1)/(N + 1)]. The N factor is a 7-bit code in the N Counter Register. The M factor is a 8-bit code in the M Counter Register. How do you determine the optimal N and M codes? There are several important factors to consider in choosing M & N values.

- A high frequency resolution is gained by using higher M & N values.
- The size of the loop filter integrating capacitor is dependant upon the value of N. The capacitor should be kept small to avoid large physical geometry & high leakage typically associated with large capacitors.

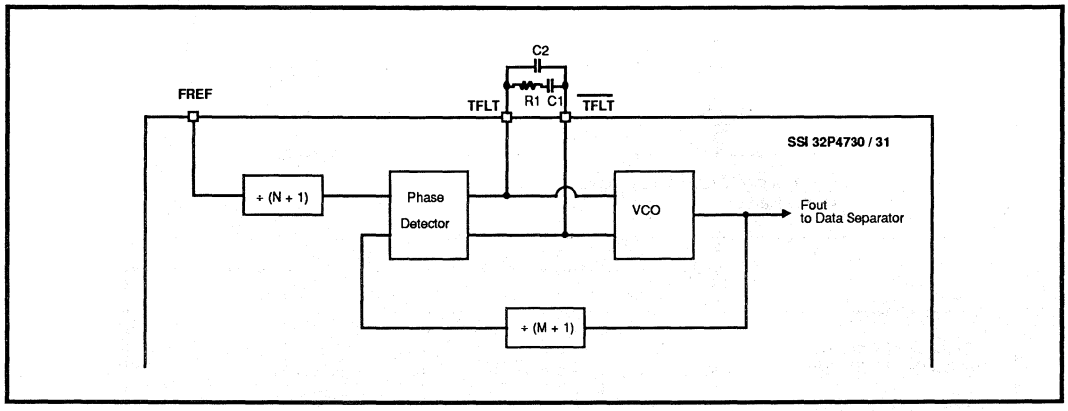

FIGURE 8: Time Base Generator Functional Model Diagram

- For a given loop filter design, the TBG must be stable for the frequency settings of all zones. In theory, if the damping factors in all zones are kept above 0.707, stability can be guaranteed. In practice, a damping factor of 1 is suggested.
- While the TBG loop filter is a differential design, any effect due to the Common mode bias mismatch between the positive and negative sides should be minimized. By using the lowest M and N values, with acceptable frequency resolution, the phase update rate would be the highest and the Common mode mismatch effect would be minimized. As an additional advantage, the integrating capacitor would be higher using lower M and N values. The integrated mismatch effect would be a smaller error voltage across the VCO control pins.

It can be seen from the analysis that follows that it is possible to maintain a damping factor of z = 1 for all zones by making (M + 1) proportional to the data rate squared. Figure 9 illustrates a flow chart to determine the M and N codes.

The M and N counters can be programmed anytime. However, they only become effective after a Data Rate Register programming. This is to reduce any transient condition for the phase locked loop in new data rate programming.

An external differential passive loop filter is needed in the phase locked loop. This loop filter design allows a design trade-off between PLL settling time and noise jitter performance. The differential architecture minimizes external noise pickup. The loop filter design details are presented in the next section.

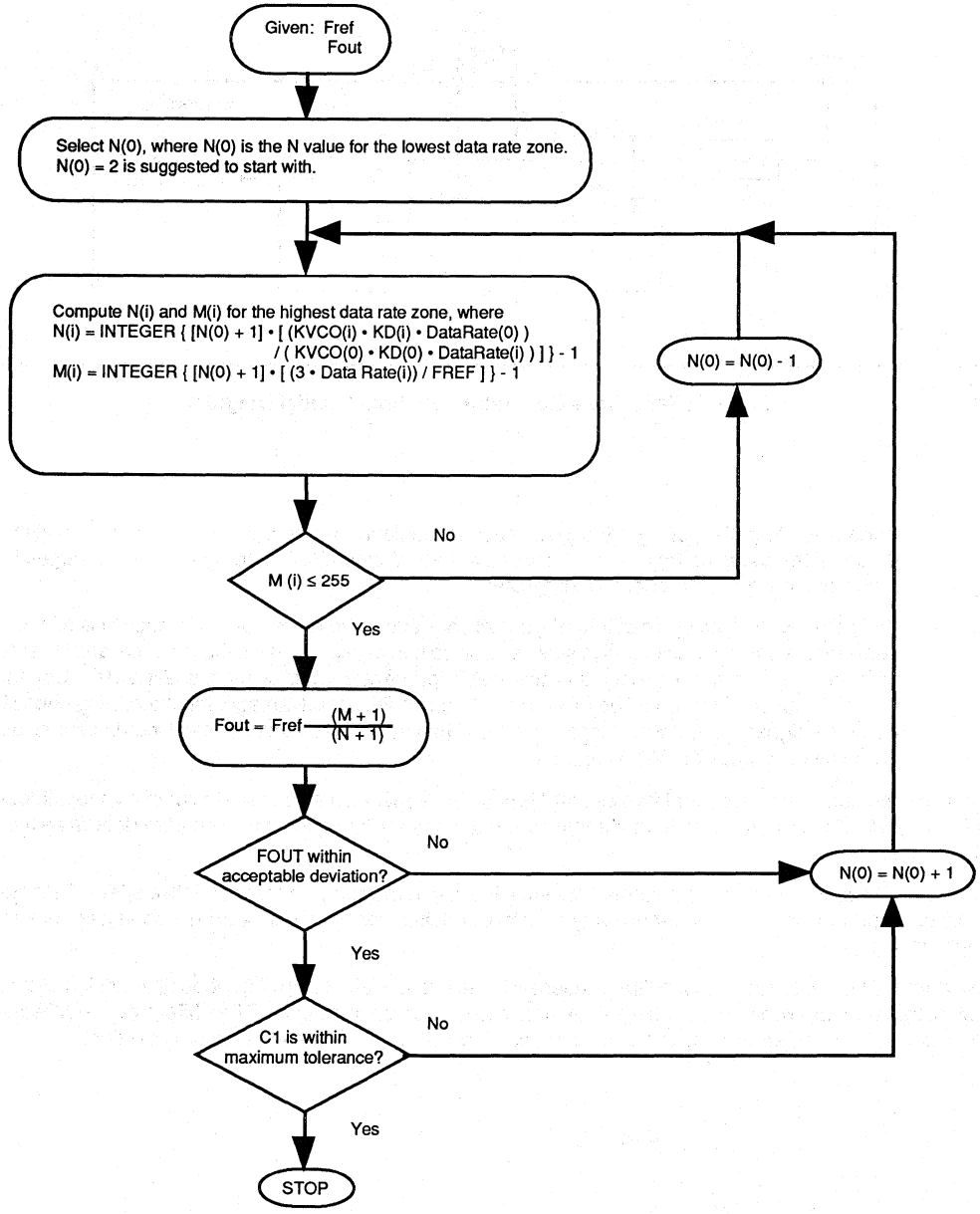

FIGURE 9: M & N Codes for Time Base Generator

READ MODE EVALUATION (continued)

Time Base Generator Loop Filter Design

The SSI 32P4731/31/41/42/44/46 requires a loop filter to control the PLL locking characterisitcs. While there are several types of filters that can be used to perform this function, a simple differential integrating filter, Figure 8 has proven to be very effective.

In designing the loop filter for the TBG PLL, two key considerations should be noted:

- PLL settling time

  In zoned recording application, the TBG output frequency must vary with data rate changes from one zone to another. When the M Counter Register is updated, the PLL will acquire and settle to the correct output frequency. This settling time should be less than the minimum track-to-track seek time.

- C1 capacitor must have low leakage. Typically, C1 should be selected to be less than 0.1 µF.

The loop filter bandwidth must be large enough for the PLL to settle fast. Yet, the time jitter performance is improved by a lower filter bandwidth. Thus, the bandwidth should only be large enough to meet the PLL settling time requirement.

Figure 8 shows the functional model diagram. C2 is typically designed to be only one-tenth of C1, for high frequency noise shunt purpose. It may be neglected in the R1 and C1 design consideration. From second-order linear analysis, the loop response can be shown to be:

$$I_{out} = KD \cdot (\theta_i - \theta_o)$$ KD = Phase Detector Gain, θ_i = reference input phase, θ_o = VCO output phase

$$V_{VCO} = I_{out} \cdot F(s)$$ F(s) = Loop Filter Transfer Function

$$\theta_o = \frac{KVCO \cdot V_{VCO}}{(M+1)} \frac{1}{s}$$ KVCO = VCO Gain

$$\frac{\theta_o}{\theta_i} = \frac{KVCO \cdot KD \cdot F(s) / (M+1)}{s + KVCO \cdot KD \cdot F(s) / (M+1)} \qquad F(s) = R_1 + \frac{1}{sC_1}$$

$$= \frac{KVCO \cdot KD \cdot (1 + s R_1 C_1)/[C_1(M+1)]}{s^2 + s\, KVCO \cdot KD \cdot \frac{R_1}{(M+1)} + \frac{KVCO \cdot KD}{C_1(M+1)}}$$

Let the characteristics equation be written as:

$$\chi(s) = s^2 + 2 s \zeta \omega_n + \omega_n^2 \qquad \omega_n^2 = \frac{KVCO \cdot KD}{C_1 (M+1)} \qquad \zeta = \frac{KVCO \cdot KD \cdot R_1}{2 (M+1) \omega_n}$$

M & N values are selected through the algorithm given in Figure 9 A damping factor of $\zeta = 1$ is chosen, and M is proportional to the data rate so that the damping factor and bandwidth remain constant as the data rate decreases. The acquisition time of the loop is set-up to accomodate a zero phase restart and allow for 1 % maximum phase error after phase acquisition. According to Figure 2 in the Data Synchronizer Family Application this gives an $w_n T = 5.2$ Where T = settling time, T must be less than track-to-track seek time, typically <0.1 ms

READ MODE EVALUATION (continued)

Time Base Generator Loop Filter Design (continued)

For the SSI 32P4730/31 at 24 Mbit/s maximum data rate and the SSI 32P4741/42/44/46 and 48 Mbit/s maximum data rate the timebase generator will run at 72 MHz. Given FREF = 18 MHz, the loop filter design is as follows: From the data sheet, KVCO = 0.17 wVCO = 0.17 • 2pi • 72 = 76.9 Mrad/(V-sec)
DR Code = 108 for 24 Mbit/s (48 Mbit/s for SSI 32P474X)
(refer to electrical spec for correct value) KD = 2.0304 • DR Code + 10.4394 = 229.7 µA/rad
C1 = 0.086 µF C2 = 0.0086 µF R1 = 447Ω

In the following table, R1, C1 and C2 are chosen based on the maximum data rate. ω_n and ζ are then recalculated based on other data rate requirements and the calculated loop filter component values.

ZONE	DATA RATE FOUT		N M	FOUT DR CODE		KD	KVCO	T	ω_n	Z
	(Mbit/s)	(ideal) MHz		(actual) MHz		(µA/rad)	Mrad/(V•s)	(ms)	Krad/s	
0	24 (48)	72	18 75	72	108	229.7	76.9	0.100	52.0	1
1	20 (40)	60	14 49	60	88	189.1	64	0.098	53.1	1.02
2	18 (36)	54	13 41	54	79	170.8	57.7	0.100	52.2	1.00
3	15 (30)	45	11 29	45	65	142.4	48	0.101	51.5	.991
4	12 (24)	36	8 17	36	50	112	38.5	0.099	52.7	1.01

Time Base Generator Jitter Performance

Jitter performance is an important figure of merit for a time base generator. For a single-chip read channel device, jitter can degrade a drive system in two areas: (1) noisy reference clock to the data separator, and (2) write data clock instability. Because the data separator is re-trained and re-locked to the read data pattern, the former is not as critical as the latter.

One method to minimize the TBG output jitter is by limiting the TBG PLL loop filter bandwidth. However, the loop bandwidth must be wide enough to allow fast acquisition time.

The SSI 32P4731/31/41/42/44/46 features very low output jitter. With the proper loop filter design, the SSI 32P4731/31/41/42/44/46 rms jitter is specified as <200 ps. For design purposes, the time jitter six sigma would be <+ or - 600 ps.

Lab Experiment 4 Time Base Generator Jitter Measurement

This lab experiment demonstrates the SSI 32P4731/31/41/42/44/46 time base generator low jitter performance. Because jitter is the uncertainty of the zero crossings at the time base generator output, the lowest output frequency signal should be the worst case representative. Using 12 Mbit/s as the lowest data rate calculated for the SSI 32P4730 in the previous section, the lowest TBG output frequency would be 36 MHz.

The loop filter is that as calculated in Section 6.4.1. The MTP3 test point is configured to monitor the data separator reference clock, which is the TBG output. The SSI 32P4730 is in Write mode, RG = SG = 0, WG =1. With an 18 MHz FREF clock to the TBG PLL, the N Counter Register is loaded with $N = 8_{decimal}$.

The M Counter Register should be programmed to $M = 17_{decimal}$ for 24 MHz TBG output and the Data Rate Register is programmed for 12 Mbit/s. The MTP3 period is histogram-ed with a time interval analyzer and an active FET probe. Photo 2A shows a Gaussian distribution of the time jitter, with one standard deviation of 150 ps. The importance of measuring TBG jitter is to see it's effect on Write Data jitter performance. The best way of measuring this is to directly measure Write Data. Using the previous settings, WCLK is tied to RRC and NRZIN is pulled low. A '3T' pattern appears as WD which is histogram-ed with a TIA. Photo 2B shows a Gaussian distribution of the time jitter, with one s.d. of 61 ps.

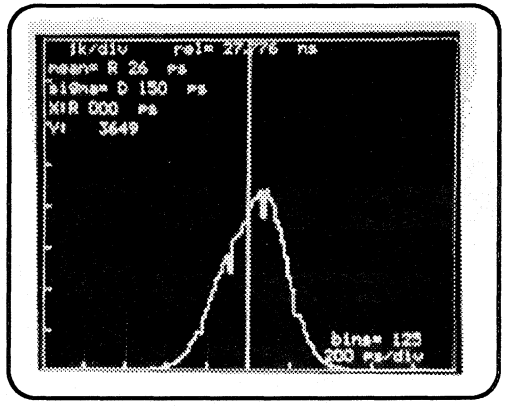

PHOTO 2A: SSI 32P4730/31 Time Base Generator Jitter Measurement.

Time Base Generator I/O & Test Points

The SSI 32P4731/31/41/42/44/46 Time Base Generator has only one input and two test points.

FREF	TTL frequency reference input: This input provides a reference input to the TBG PLL. It should be limited to between 8 MHz to 20 MHz. When the TBG is bypassed, as commanded by Control A Register: D4, the data separator PLL reference is the signal at the FREF input.
MTP3	This test point can be configured to monitor the TBG PLL output clock, FOUT.
MTP2	This test point moniters the input to the Data Separator phase detector, i.e., the timebase generator output in Idle mode.

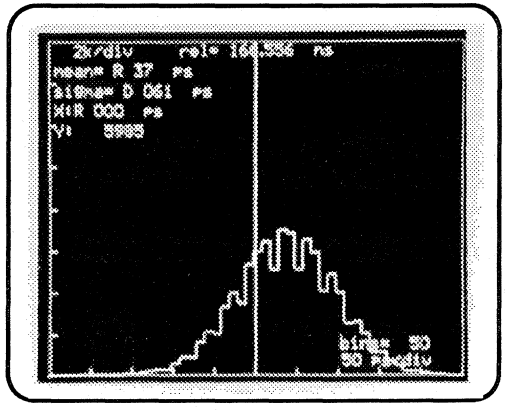

PHOTO 2B: SSI 32P4730/31 Write Data Jitter Measurement

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READ MODE EVALUATION (continued)

DATA SEPARATOR FUNCTIONALITY

The SSI 32P4731/31/41/42/44/46 Data Separator performs the following functions:

- Synchronization,
- RLL 1,7 encode & decode,
- Address mark generation & detection (for soft sector application),
- Preamble generation & detection,
- Write pre-compensation,
- Window shift adjustment.

Synchronization

For synchronization, the data separator has two objectives:

- Clock regeneration, and
- Encoded data synchronization.

Clock Regeneration

Because the data is coded with the clock signal, the clock must be regenerated for precise timing. For the SSI 32P4731/31/41/42/44/46, the clock regeneration is accomplished with a phase locked loop comprised of a phase detector, a loop filter and a voltage controlled oscillator (VCO). The VCO runs at 3X (1.5X for SSI 32P4741/42/44/46) the NRZ data rate. For 24 Mbit/s operation, the VCO should run at 72 MHz (36 MHZ for SSI 32P4741/42/44/46). How would the VCO clock align with the encoded data bits?

In the Idle mode, i.e., RG = WG = SG = 0, the VCO is phase & frequency locked to the time base generator output, Fout, which can be either a frequency synthesized signal or FREF. With the TBG output at 3X (1.5X) the NRZ data rate, the VCO is centered for a subsequent read/write cycle. The RRC is at the NRZ data rate, which is Fout/3. (Fout/1.5 for SSI 32P4741/42/44/46).

Entering into the Read mode, i.e., RG 0-to-1 transition and following the first 3 DRD transitions, the phase detector reference input switches from the TBG output to the delayed read data, DRD. A preamble pattern of 19 '3T' is used for training the VCO to phase-lock to the DRD.

To reduce the initial phase error, the SSI 32P4731/31/41/42/44/46 employs a zero-phase restart technique which, after 3 DRD transitions, halts the VCO momentarily until the 4th DRD transition is detected. The initial phase error is limited to below 2 ns of the decode window. For 24 Mbit/s operation, this represents ~ 7% error, or 0.45 radian.

One of the two VCO Locking modes will be entered depending on the state of the gain shift (GS) bit, or bit 1, in the Control B register. If GS = "1," the phase detector will enter a Gain Shift mode of operation. The phase detector starts out in a High Gain mode of operation to support fast phase acquisition. After an internal counter counts the first 14 transitions of the internal of the internal DRD signal , the gain is reduced by a factor of three. This reduces the bandwidth and damping factor of the loop by $\sqrt{3}$ which provides improved jitter performance in the Data Follow mode. The counter continues to count the next 5 DRD transitions (a total of 19 x 3T from assertion of RG) and then asserts an internal VCO lock signal.

With the internal VCO lock asserted, the following two events are initiated:

- The RRC is now switched from Fout/3(1.5 for 474X) to VCO /3(1.5 for 474X). During this switching, the RRC may be held static for a maximum of 2 NRZ clock periods. However, the SSI 32P4731/31/41/42/44/46 guarantees no glitch on RRC.
- The data synchronizer decode window, to be defined in the next section, boundaries are by the next two '3T' pattern.

Following this, the NRZ output is enabled and the data is toggled through the decoder throughout Read mode.

When the Gain Shift bit is set to "0", the phase detector gain shift function is disabled. The VCO lock sequence is identical to that of the Gain Shift mode explained above, except that no gain shift is made after the first 14 '3T's' (i.e., the phase detector is always in high Gain mode). Figure 9 illustrates the clock regeneration process.

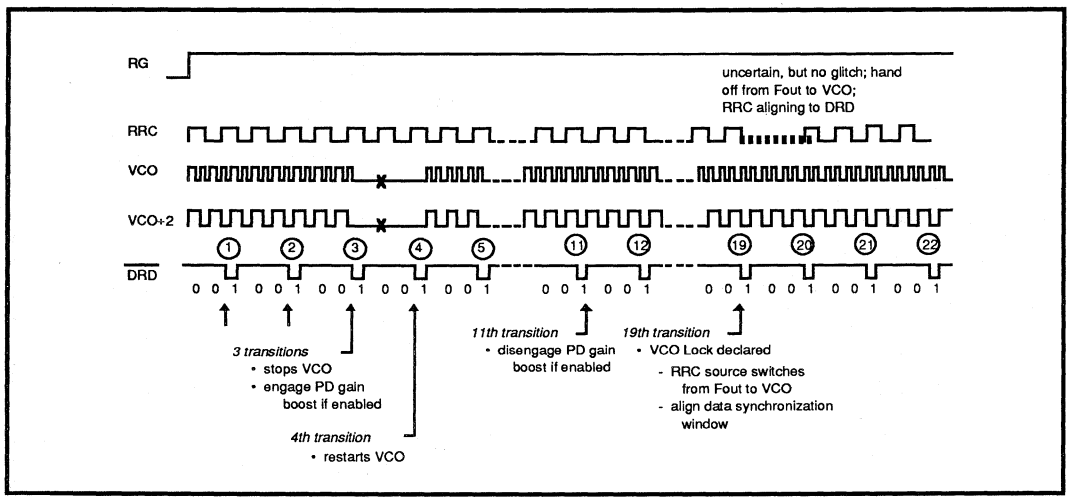

FIGURE 9: SSI 32P47XX Clock Regeneration Process

Data Separator PLL & Phase Decode Window

In the data Read mode, the VCO is locked to the $\overline{DRD}$ by phase comparing the VCO/2 (VCO for SSI 32P4741/42/44/46) and $\overline{DRD}$. Each $\overline{DRD}$ pulse corresponds to a read data '1'. Its width is one-half of the encoded bit period. Its leading (falling) edge enables the phase detector. Its trailing (rising) edge is phase compared to the rising edge of VCO/2 (VCO). The VCO is then steered in the direction to correct the phase difference. After a phase comparison, the phase detector is disabled until the next leading edge of the $\overline{DRD}$.

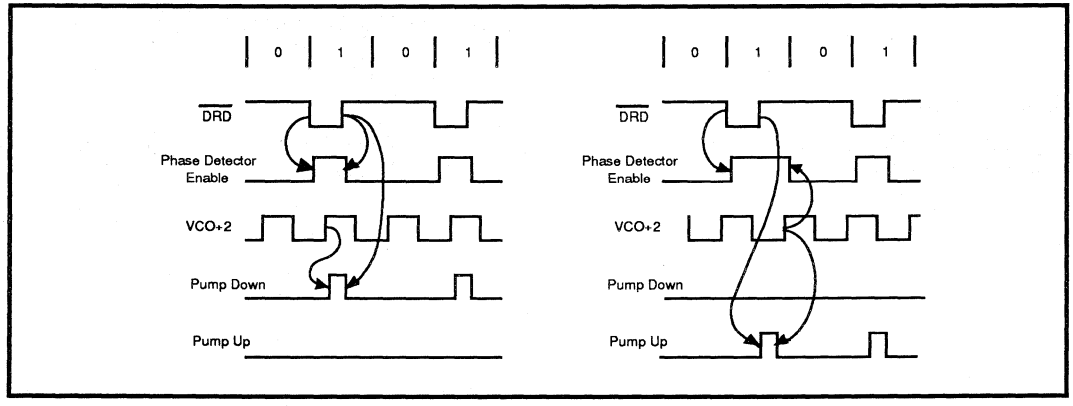

FIGURE 10: SSI 32P47XX Data Separator Phase Dectector Data Locking Mechanism

READ MODE EVALUATION (continued)

Data Separator PLL & Phase Decode Window (continued)

An important concept in the working of data separator is the phase decode window. The phase decode window is the time span between two consecutive falling edges of the VCO/2 (VCO). In a locked condition, when the phase detector is enabled at the beginning of a phase decode window, the phase decode window is said to be perfectly centered. Should a $\overline{DRD}$ bit shift by up to half of VCO/2 (VCO) period in either direction, this $\overline{DRD}$ bit would still be phase compared with the proper VCO/2 (VCO) rising edge, Figure 11. If the $\overline{DRD}$ pulse width is not matched to half of VCO/2 (VCO) period, the tolerance on bit shift is reduced. The $\overline{DRD}$ bit would be phase compared to the wrong VCO/2 (VCO) rising edge. Thus, a phase decode error has occured. It should be noted that a phase decode error would cause a transient disturbance on the VCO control voltage.

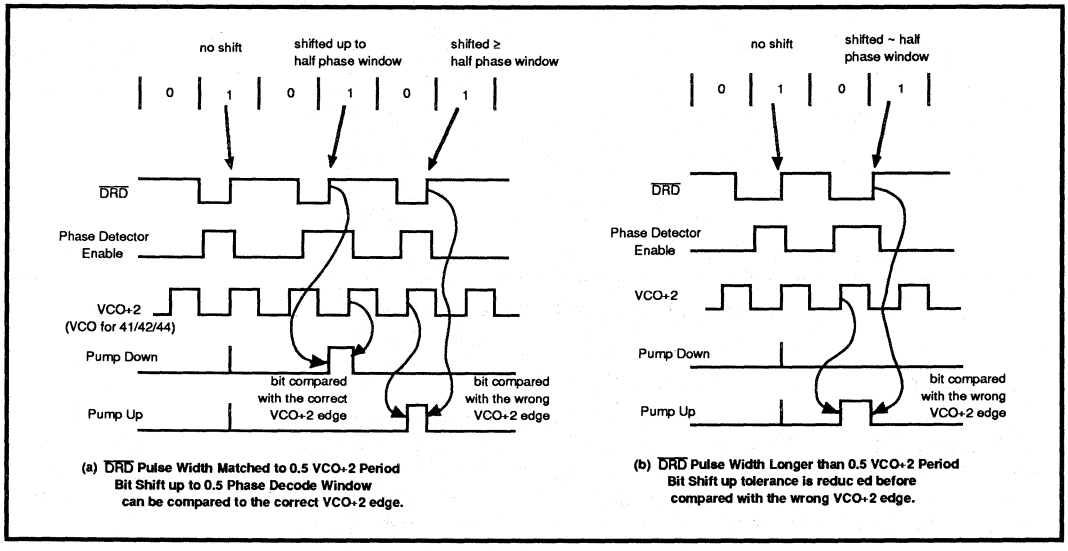

FIGURE 11: SSI 32P47XX Data Separator Phase Decode Window Asymmetry causes bit shift tolerance reduction.

Encoded Data Synchronization

With the clock extracted from the read data, the SSI 32P4731/31/41/42/44/46 re-synchronizes the encoded data prior to the 1,7 Decoder. Figure 12 illustrates the timing function of the synchronization.

READ MODE EVALUATION (continued)

DATA SEPARATOR PLL I/O & TEST POINTS

The following I/O & test points are helpful in troubleshooting the data separator PLL:

MTP1	Open emitter output test point: it can be configured to monitor the VCO/2 (VCO) reference to the phase detector.
MTP2	Open emitter output test point: it can be configured to monitor the DRD input to the phase detector.
MTP3	Open emitter output test point: it can be configured to monitor the reference frequency to the data separator PLL in the Idle mode.
DFLT & $\overline{\text{DFLT}}$	Differential VCO control pins: a differential loop filter is connected across these two pins. The Common mode voltage at these two pins should be near 2V.
RRC	TTL read reference clock output: the RRC frequency should be at the NRZ data rate.
RR	Reference resistor input: An external 1% 12.1 kΩ resistor is connected from this pin to ground to establish a precise internal reference current for the Data Separator and Timebase Generator. The voltage at this pin is proportional to absolute temperature. At room temperature ambient, this voltage is typically measured at 1.6V.

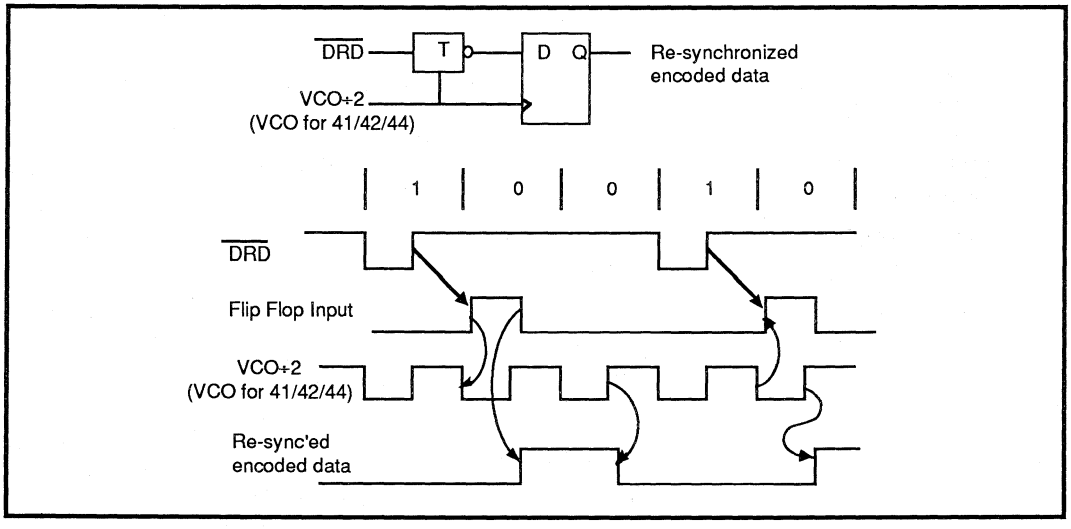

FIGURE 12: Data Resynchronization Timing.

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READ MODE EVALUATION (continued)

DATA SEPARATOR LOOP FILTER DESIGN

The SSI 32P4730/31/41/42/44/46 data separator PLL requires a differential external loop filter. Again, the same integrating loop filter topology as for the Time Base Generator can be used. The loop filter bandwidth must be sufficient large for minimal phase error at the end of the VCO training pattern. However, a narrow bandwidth is desirable for noise & jitter rejection.

The SSI 32P4730/31/41/42/44/46 features a high phase detector gain boost for fast phase acquisition, and yet narrower bandwidth in normal data read operation. When entering the Read mode, the data separator PLL utilizes a zero-phase restart technique to minimize the initial phase error between the VCO & the $\overline{DRD}$ pulses. The initial phase error is ~2 ns. For 24 Mbit/s operation, this corresponds to 0.45 rad phase error. The data separator PLL has 16 '3T' pattern period to lock onto the $\overline{DRD}$ pulses. Depending on system parameters, such as jitter expectation from the head/media combination, the user must decide the maximum acceptable final phase error at the end of the training sequence. The following presents two design examples, one utilizing the phase detector gain shift and one without.

PHASE DETECTOR GAIN SHIFT DISABLED

Assume max DR = 24 Mbit/s (48 Mbit/s for the SSI 32P4741/42/44)

$$\text{Encode Bit Perios} = \frac{1}{1.5 \bullet 24\,\text{MHz}\,(48\,\text{MHz})} = 28\text{ ns (14 ns)}$$

Sixteen '3T' pattern implies training time T = 16 • 3 • 28 ns (14 ns) = 1.33 µs (0.667 µs)

Let ζ be the damping factor. It is set to 1.4 to allow a drop as the data rate decreases.

Let the final phase error be less than 10% of initial phase error.

In the SSI Data Sychronizer Family App Note figure 2, $\omega_n T = 2.2$

Thus, ω_n = 1.65 Mrad/s (3.33 Mrad/s)

$$\omega_n^2 = \frac{KVCO \bullet KD}{3C_1} \qquad \zeta = \frac{KVCO \bullet KD \bullet R_1}{2 \bullet 3 \bullet \omega_n}$$

For the SSI 32P4730/31 at 24 Mbit/s, the loop filter design is as follows:

From the data sheet, KVCO = 0.17 $\omega_{VCO}/2$ = 0.17 • 2π • 72/2 = 38.45 Mrad/(V-sec)

KD = 2.0304 • DR Code + 10.4394 = 229.7226 µA/rad (refer to electrical spec for correct value)

DR Code = 108 for 24 Mbit/s

C1 = 1071 pF C2 = 107 pF R1 =1585 Ω

In the following table, R, C1, and C2 are chosen based on the maximum data rate. ω_n and ζ are then recalculated based on other data rate requirements and the calculated loop filter component values.

ZONE	DATA RATE	DR CODE	KD	KVCO	T	ω_n	ζ
	(Mbit/s)		(µA/rad)	Mrad/(V•s)	(µs)	Mrad/s	
0	24	108	229.7	38.5	1.333	1.65	1.4
1	20	88	189.1	32.0	1.610	1.37	1.160
2	18	79	170.8	28.8	1.785	1.23	1.046
3	15	65	142.4	24.0	2.142	1.03	0.8715
4	12	50	112.0	19.2	2.701	0.81	0.6911

For the SSI 32P4741/42/44/46 at 48 Mbit/s, the loop filter design is as follows:

From the data sheet, KVCO = 0.17 ω_{VCO} = 0.17 • 2π • 72 = 76.9 Mrad/(V-sec)

KD = 2.0304 • DR Code + 10.4394 = 229.7226 µA/rad

DR Code = 108 for 48 Mbit/s

C_1 = 535 pF C_2 = 53 pF R_1 = 1585 Ω

In the following table, R, C1, and C2 are chosen based on the maximum data rate. ω_n and ζ are then recalculated based on other data rate requirements and the calculated loop filter component values.

ZONE	DATA RATE	DR CODE	KD	KVCO	T	ω_n	ζ
	(Mbit/s)		(µA/rad)	Mrad/(V•s)	(µs)	Mrad/s	
0	48	108	229.7	76.9	0.667	3.30	1.4
1	40	88	189.1	64.1	0.805	2.73	1.160
2	36	79	170.8	57.7	0.893	2.46	1.0456
3	30	65	142.4	48.1	1.071	2.05	0.8715
4	24	50	112.0	38.5	1.351	1.63	0.6911

DATA SEPARATOR LOOP FILTER DESIGN (continued)

Phase Detector Gain Shift Enabled

Assume max DR = 24 Mbit/s (48 Mbit/s for the SSI 32P4741/42/44/46)

$$\text{Encode Bit Period} = \frac{1}{1.5 \cdot 24\,\text{MHz}\,(48\,\text{MHz})} = 27.8\,\text{ns}\,(13.9\,\text{ns})$$

Let the final phase error be less than 10% of initial phase error.
This is achieved in tow stages: with 3X the Idle mode phase detectyor gain for 11 '3T'
with 1X the Idle mode phase detector gain for 5 '3T'.

	T	KVCO	KD	FINAL PHASE(1)			ω_n
	(μs)	(Mrad/s)	(μA/rad)	Error (%)	ζ(2)	$\omega_n T$(3)	Mrad/s
Before shift	0.97 (0.459)	38.45 (76.91)	22.97	<18	2.42	0.2	0.2182 (0.4364)
After shift	0.417 (0.209)	38.45 (76.91)	76.91	<55	1.4	0.0525	0.1260 (0.2520)

(1) Final Phase Error of each stage is the % of the initial phase error at the beginning of each stage.
Let α be final phase error (as a % of the zero phase restart error) of the first stage.
Let β be final phase error (as a % of the phase error at the end of first stage) of the second stage.
Then, the final phase error at the 16 '3T pattern is $\alpha \cdot \beta = 0.10$
To take advantage of the gain shift, let the first stage correction be 3 times that of the secondc stage.
That is to say: $\beta = 3\alpha \quad \Rightarrow \alpha = 0.18; \beta = 0.55$

(2) For stability, it is desirable to have ζ larger than 0.7 at the lowest data rate after gain shift.
So, we set $\zeta = 1.4$ at the highest data rate after gain shift.
Because the KD before the shift is 3X than that without boost, its ζ is $\sqrt{3}$X or 2.42.

(3) From SSI Data Synchronizer Application Notes, to meet the final phase error requirement, $\omega_n T$ after the gain shift must be at least 0.0525.

$$\omega_n^2 = \frac{KVCO \cdot KD}{3C_1} \qquad \zeta = \frac{KVCO \cdot KD \cdot R_1}{2 \cdot 3 \cdot \omega_v}$$

For the SSI 32P4730/31 at 24 Mbit/s, the loop filter design is as follows:
During the first 11 '3T':
From the data sheet, KVCO = 0.17 $\omega_{VCO}/2 = 0.17 \cdot 2\pi \cdot 72/2 = 38.45$ Mrad/(V-sec)
KD = 2.0304 • DR Code + 10.4394 = 229.7226 μA/rad (refer to electrical spec for correct value)
DR Code = 108 for 24 Mbit/s
$\omega_n T = 0.2$ $\zeta = 2.42$ $\omega_n = 0.218$ Mrad/s
C1 =61236 pF C2 = 6123 pF R1 = 362 Ω

During the rest of Read mode:
From the data sheet, KVCO = 0.17 $\omega_{VCO}/2 = 0.17 \cdot 2\pi \cdot 72/2 = 38.45$ Mrad/(V-sec)
KD = 0.6768 • DR Code + 3.4798 = 76.57 μA/rad (refer to electrical spec for correct value)
DR Code = 108 for 24 Mbit/s
$\omega_n T = 0.0525$ $\zeta = 1.4$ $\omega_n = 0.126$ Mrad/s
C1 = 61236 pF C2 = 6123 pF R1 =362Ω

In the following table, R, C1, and C2 are chosen based on the maximum data rate. ω_n and ζ are then recalculated based on other data rate requirements and the calculated loop filter component values.

					Before shift			After shift		
ZONE	**DATA RATE**	**DR CODE**	**KD**	**KVCO**	**T**	ω_n	ζ	**T**	ω_n	ζ
	(Mbit/s)	(μA/rad)		Mrad/(V•s)	(μs)	Mrad/s		(μs)	Mrad/s	
0	24	108	229.7	38.5	0.917	0.218	2.42	0.417	0.126	1.40
1	20	88	189.1	32.0	1.107	0.181	2.00	0.503	0.105	1.16
2	18	79	170.8	28.8	1.227	0.163	1.81	0.558	0.094	1.05
3	15	65	142.4	24.0	1.473	0.136	1.51	0.669	0.079	0.872
4	12	50	112.0	19.2	1.857	0.108	1.19	0.844	0.062	0.691

For the SSI 32P4741/42/44/46/46 at 48 Mbit/s, the loop filter design is as follows:
During the first 11 '3T':
From the data sheet, KVCO = 0.17 ω_{VCO} = 0.17 • 2 π • 72 = 76.91 Mrad/(V-sec)
KD = 2.03.4 • DR Code + 10.4394 = 229.7226 μA/rad (refer to electrical spec for correct value)
DR Code = 108 for 48 Mbit/s
$\omega_n T$ = 0.2 ζ = 12.42 ω_n = 0.436

C1 =30618 pF C2 = 3061 pF R1 = 362Ω

During the rest of Read mode:
From the data sheet, KVCO = 0.17 $\omega_{VCO}/2$ = 0.17 • 2 π • 72/2 = 38.45 Mrad/(V-sec)
KD = 0.6768 • DR Code + 3.4798 = 76.57 μA/rad (refer to electrical spec for correct value)
DR Code = 108 for 48 Mbit/s
$\omega_n T$ = 0.0525 ζ = 1.4 ω_n = 0.252

C1 = 30618 pF C2 = 3061 pF R1 = 362Ω

In the following table, R, C1, and C2 are chosen based on the maximum data rate. ω_n and ζ are then recalculated base on other data rate requirements and the calculated loop filter component values.

					Before shift			After shift		
ZONE	**DATA RATE**	**DR CODE**	**KD**	**KVCO**	**T**	ω_n	ζ	**T**	ω_n	ζ
	(Mbit/s)	(μA/rad)		Mrad/(V•s)	(μs)	Mrad/s				
0	24	108	229.7	76.91	0.458	0.436	2.42	0.208	0.252	1.4
1	20	88	189.1	64.09	0.553	0.361	2.00	0.252	0.209	1.16
2	18	79	170.8	57.90	0.614	0.326	1.81	0.279	0.188	1.05
3	15	65	142.4	48.07	0.736	0.272	1.51	0.335	0.157	0.872
4	12	50	112.0	38.45	0.928	0.215	1.19	0.422	0.124	0.691

Note that, for the same final phase error, the loop filter bandwidth after gain shift is reduced to 15% of the bandwidth without using phase detector gain shift. Improved noise and jitter immunity of the data separator PLL can be acheived by finding a balance of high bandwidth during aquisition, and low bandwidth after aquisition.

READ MODE EVALUATION (continued)

RLL DECODE FUNCTION

The SSI 32P4730/31/41/42/44/46/46 supports the 1,7 RLL encode & decode function. In the Read mode, the encoded data from the read/write preamplifier is AGC amplified, pulse qualified, clock extracted and re-synchronized. The encoded data is then decoded back into the NRZ domain.

Because every three encoded bits are decoded into two NRZ bits, the leading bit of the three-bit frame must be defined. This is the bit synchronization. When the RG is asserted, nineteen 3T patterns must be detected prior to the internal VCO lock is asserted. After the internal VCO lock is asserted, the SSI 32P4730/31/41/42/44/46/46 searches for three consecutive 3T patterns for bit synchronization. The bit immediately following the last '1' bit of the three 3T patterns is defined as the leading bit of a three-bit frame. The decode function conforms to Table 3.

TABLE 3: Decode Table for 1,7 RLL Code Set

Encoded Bit Data							Decoded NRZ Data	
Previous		Present			Next			
Y 2	Y 3	Y 1	Y 2	Y 3	Y 1	Y 2	D 1	D 2
0	0	0	0	0	X	X	0	1
1	0	0	0	0	X	X	0	0
0	1	0	0	0	X	X	0	1
X	X	1	0	0	X	X	1	1
X	0	0	1	0	0	0	1	1
X	0	0	1	0	1	0	1	0
X	0	0	1	0	0	1	1	0
X	1	0	1	0	0	0	0	1
X	1	0	1	0	1	0	0	0
X	1	0	1	0	0	1	0	0
0	0	0	0	1	X	X	0	1
1	0	0	0	1	X	X	0	0
0	1	0	0	1	X	X	0	0
X	X	1	0	1	X	X	1	0

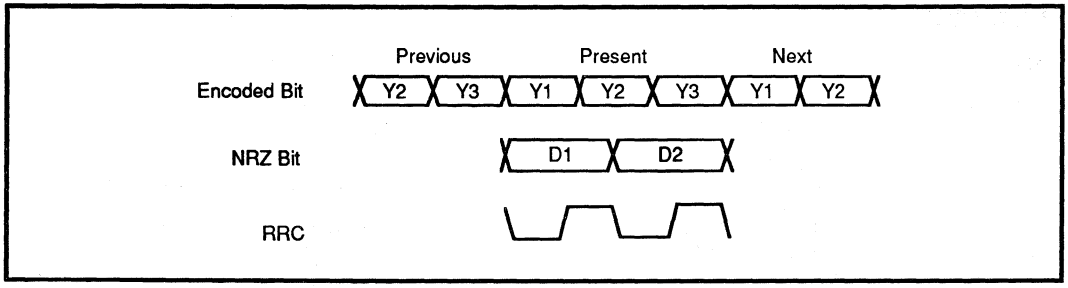


FIGURE 13: Definition of Y1-3 and D1-2 for Table 6.7.1

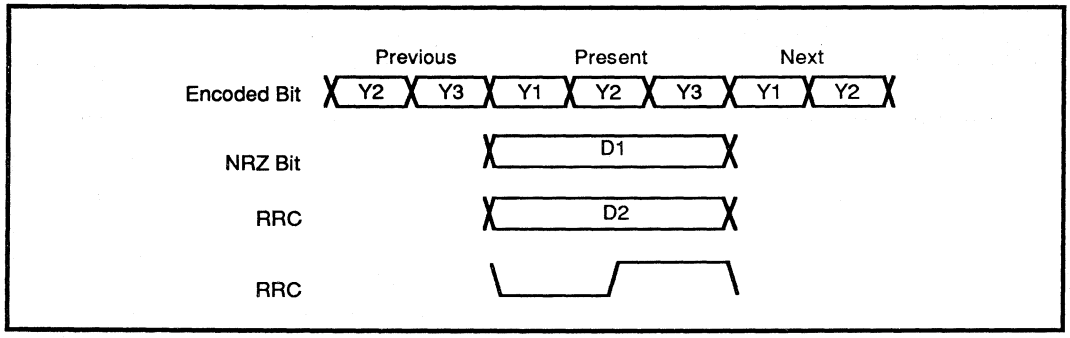


FIGURE 14: Definition of Y1-3 and D1-2 for the 32P4742/46

The decoded NRZ data appears at the NRZOUT pin. A valid NRZ data bit is clocked out by an RRC falling edge. The controller should receive the NRZ data bit by RRC rising edge. The NRZOUT bit is guranteed to be present at least 13 ns before the RRC rising edge, and at least 13 ns after the same RRC rising edge.

The SSI 32P4742/46 supports the dual bit NRZ interface. In Read mode, NRZ data is clocked out of the NRZ and NRZ1 bidirectional pins on the falling edge of RRC two bits at a time. The controller should receive the NRZ data bits by the RRC rising edge. RRC runs at half of the NRZ data rate.

In non-Read mode, i.e., RG = 0, the NRZOUT is a tri-state high impedance pin. With the RG asserted, the NRZOUT is an output pin. Refer to the electrical specification for the delay time limits.

READ MODE EVALUATION (continued)

ADDRESS MARK DETECT FUNCTION

The SSI 32P4730/31/41/44 can support both hard sector and soft sector operations. The SSI 32P4742/46 does not support Soft Sector mode.

In hard sector operation, the AMENB pin is held to logic '0' and the $\overline{AMD}$ output is in tri-state high Impedance mode. The read cycle is initiated with the RG assertion. No address mark detection is necessary.

In soft sector operation, the address mark must be detected before the RG is asserted to continue a read cycle. With the AMENB asserted to logic '1', the SSI 32P4730/31/41/44 initiates the address mark search. An address mark pattern should consist of two 8T patterns followed by two 12T patterns. The address mark detect circuitry searches for six consecutive 0's followed by nine consecutive 0's. After the six consecutive 0's are detected, the nine-0 pattern must be detected within five encoded '1' bits are detected. If no nine consecutive 0 pattern s detected before the fifth encoded '1' bit is detected, the address mark search resets and looks for the six consecutive 0's again. If the nine consecutive 0's are detected, the $\overline{AMD}$ output is pulled to logic '0' until the AMENB is released. The RG should be asserted after $\overline{AMD}$ is pulled low. Figure 15 illustrates a timing example in the soft sector Read mode.

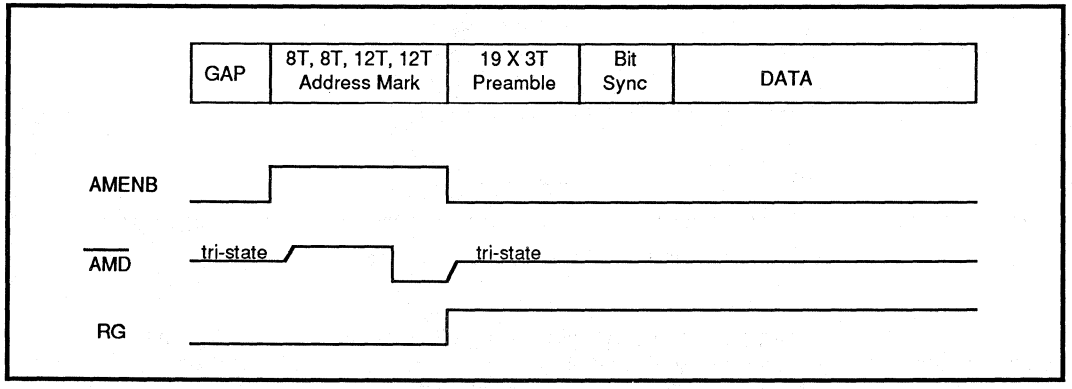
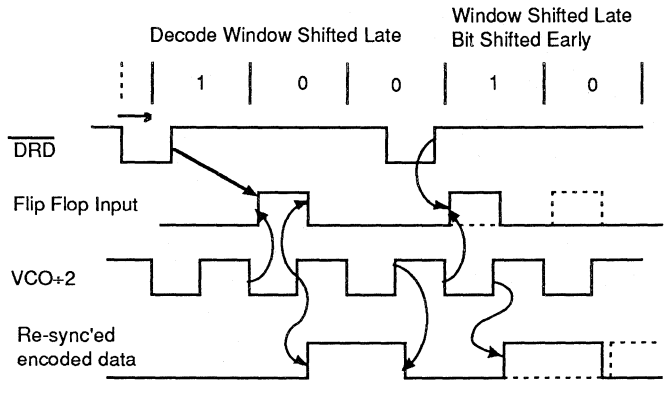


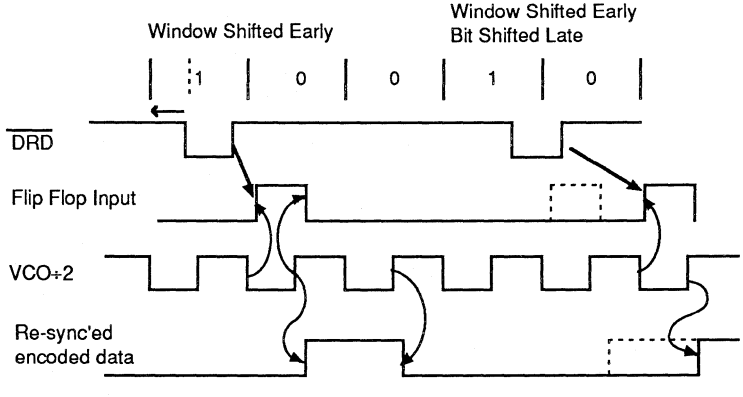
FIGURE 15: Read Mode Soft Sector Timing.

DECODE WINDOW SHIFT FUNCTION

The SSI 32P4730/31/41/42/44/46 allows the user to perform window margin testing with the window shift function. If the synchronization window is well centered without loss, the window can be theorectically shifted up to 50% in each direction without error. The window shift function is accomplished via a digital delay circuit which can delay the $\overline{DRD}$ with respect to the VCO/2, or vice versa. Figure 16 illustrates the window shift function.



(a) Window Shifted Late



(b) Window Shifted Early

FIGURE 16: Window Shift Function Illustration

By programming the Window Shift Register, the synchronization window can be shifted up to 30% in either direction. The lower 4 bits, D3..D0, sets the amount of window shift. D4 determines the window shift direction D5 enables the window shift function.

WINDOW SHIFT TEST POINT

DACOUT multiplexed DAC output: When window shift register (05 HEX): D7-6 = 10, DACOUT represents the window shift magnitude setting DAC. The voltage at DACOUT in this mode can be estimated as:

3.8276 + (0.01961 $DACW_s$) for early window shift

4.420 - (0 .01961 $DACW_s$) for late window shift

where DACWs is equal to the 4-bit register value of the window shift magnitude.

SERVO MODE EVALUATION

The SSI 32P4730/31/41/42/44/46 all support 4 burst servo capture function. Four internal peak capture 10 pF capacitors are used to sample the 4 servo bursts. While all other functions are identical between these devices, the two devices offer different servo capture schemes.

For all parts , the Servo mode is initiated by asserting the servo gate. With a 0-to-1 SG transition, the following events occur:

- the AGC control enters the HOLD/Fast Decay (gain increase) until the signal reaches 125% the desired level or 1 µs, whichever occurs first.
- the programmable filter cutoff freqeuncy is set according to the Servo mode Cutoff Register,
- the programmable filter boost is enabled/disabled according to the MSB of the Filter Boost Register,
- the pulse qualification method and percentage are set according to the Servo Threshold Register,
- the qualification threshold time constant is switched to the RTS pin,
- the AGC functions will regulate the DP/DN signal to the prescribed level according to the Servo AGC Level Register.

Because the servo signal and the data rate signal are typically of different frequency, the filter bandwidth can be set independent from the Data mode. Likewise, the boost function can be enabled or disabled. The pulse qualification percentage, method and time constant are also set independent from the Data mode.

With a 1-to-0 or 0-to-1 transition of the SG, the SSI 32P4730/31/41/42/44/46/46 enters a HOLD/Fast Decay mode time period as set by the Low-Z time bit in the N-Counter Register. When bit D7 = 0 and there is a transition of SG, the AGC enters a HOLD mode for 0.4 µs. Following the HOLD period, the AGC enters a fast Decay mode until the signal at DP/DN exceed 125% of the level set by the SERVO AGC Level register in Servo mode, or 1 Vpp in Data mode. If the signal does not reach 125% within the timeout period, as set by the Low-Z time bit in the N-Counter Register, nominally 1us, the fast decay sequence ends and normal AGC actions are reinstated. A servo preamble pattern is then expected to allow the AGC to regulate the DP/DN signal level, which is programmable from 0.77 Vppd to 1 Vppd via the Servo AGC Level Register. The $\overline{\text{HOLD}}$ pin should be pulled to logic '0' after the servo AGC preamble.

The control sequence after the servo preamble pattern differs between the P4730/44/46 and P4731/41/42.

SSI 32P4730/44/46 SERVO

The SSI 32P4730/44/46 features A + B, A - B and C - D servo outputs. Other input controls for the Servo mode include RESET, LATCH0, LATCH1, STROBE and reference input (SREF).

The $\overline{\text{RESET}}$ input, when pulled to logic '0', the four internal peak capture capacitors are discharged and reset. When the High Resolution Reset bit (D7, Reg 0D hex) is used, all outputs are expected to be at the SREF input voltage, which should be between 1V to 3V. If the High Resolution bit is not used, all outputs are expected to be below the SREF voltage. The RESET input can be active without SG activated.

SERVO MODE EVALUATION (continued)

SSI 32P4730/44/46 SERVO (continued)

Each burst channel is designated by LATCH1 and LATCH0 as following:

- LATCH1, LATCH0 = 0, 0 Burst Channel A
- LATCH1, LATCH0 = 0, 1 Burst Channel B
- LATCH1, LATCH0 = 1, 0 Burst Channel C
- LATCH1, LATCH0 = 1, 1 Burst Channel D

The amplified, filtered and full-wave rectified servo signal is peak captured onto an internal hold capacitor, designated by LATCH1 and LATCH0, when STROBE = '1'. The drive current of the servo peak detector charge pump into the internal hold capacitors is set by a 4-bit word addressed throught the serial port. The current is programmable from 6 µA to 96 µA in 6 µA increments. A low current setting may be desired to maximize noise immunity. The capacitor charging time is a function of signal amplitude, frequency and current setting. When STROBE = '0', the full-wave rectified output is disconnected from all internal hold capacitors. It is recommended that STROBE returns to '0' before LATCH1/0 change state for next burst channel.

The voltage gain from the DP/DN to the internal hold capacitors is 1 Vop/Vppd. For example, a 0.4 Vppd DP/DN signal yields 0.4V (relative to a given reference bias). The P4730/44 outputs are defined as:

- A + B = DP/DN @ Burst A + DP/DN @ Burst B + SREF
- A - B = 2 x (DP/DN @ Burst A - DP/DN @ Burst B + SREF)
- C - D = 2 x (DP/DN @ Burst C - DP/DN @ Burst D + SREF)

All DP/DN voltages are peak-to-peak differential. Each channel output buffer has a 50Ω output impedance.

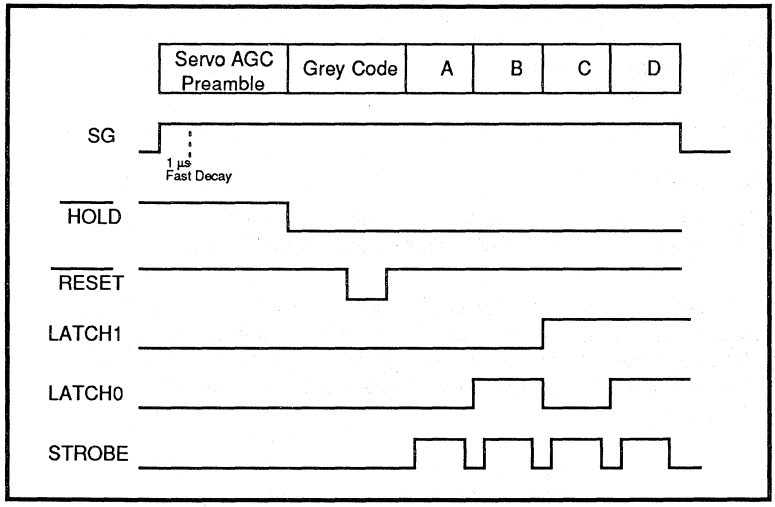


FIGURE 17: SSI 32P4730/44 Servo Control Sequence

Lab Experiment 5 SSI 32P4730/44/46 Servo Mode Functionality
This lab experiment demonstrates the SSI 32P4730/44/46 Servo mode functionality. With the SG asserted, an amplitude modulated input can be applied to VIA. Photo 17 shows the analog input, STROBE, $\overline{\text{RESET}}$, LATCH1, LATCH0 and the servo outputs.

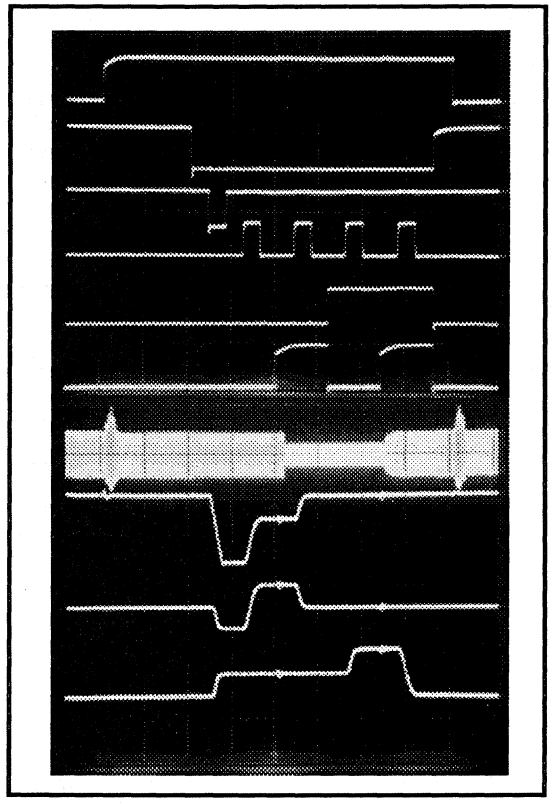


FIGURE 3A: SSI 32P4730/44/46 Servo Mode Functionality

SSI 32P4731/41/42 SERVO

The SSI 32P4731/41/42 features individual servo burst outputs: Bursts A, B, C and D. Other input controls for the Servo mode include $\overline{\text{RESET}}$, STROBE. A reference output voltage is available, MAXREF, typically 3.1V, which should be always higher than the maximum possible Bursts A, B, C and D voltage when DP/DN = 1 Vppd.

The $\overline{\text{RESET}}$ input, when pulled to logic '0', the four internal peak capture capacitors are discharged and reset. When the High Resolution Reset bit (D7, Reg 0D hex) is used, all outputs are expected to be at 0.5V. If the High Resolution bit is not used, all outputs are expected to be below 0.5V. The $\overline{\text{RESET}}$ input can be active without SG activated.

There is no burst channel address bit needed for P4731/41/42. With the $\overline{\text{RESET}}$ pulled to logic 0, the internal counter is pre-set for Burst Channel A. With the first falling edge on the STROBE input, the counter is advanced to Burst Channel B. Another falling edge advances the counter to Burst Channel C. Another falling edge advances the counter to Burst Channel D.

SERVO MODE EVALUATION (continued)

SSI 32P4730/44/46 SERVO (continued)

The amplified, filtered and full-wave rectified servo signal is peak captured onto an internal hold capacitor when STROBE = '1'. The drive current of the servo peak detector charge pump into the internal hold capacitors is set by a 4-bit word addressed throught the serial port. The current is programmable from 6 µA to 96 µA in 6 µA increments. A low current setting may be desired to maximize noise immunity. The capacitor charging time is a function of signal amplitude, frequency and current setting. When STROBE = '0', the full-wave rectified output is disconnected from all internal hold capacitors.

The voltage gain from the DP/DN to the Bursts A, B, C and D outputs is 2.25 Vop/Vppd. For example, a 0.4 Vppd DP/DN signal yields 0.9V (relative to a given reference bias). The P4731/41/42/44 burst output is:

Burst X = DP/DN @ Burst X • 2.25 + 0.5V

The DP/DN voltage is peak-to-peak differential. Each channel output buffer has a 50Ω output impedance.

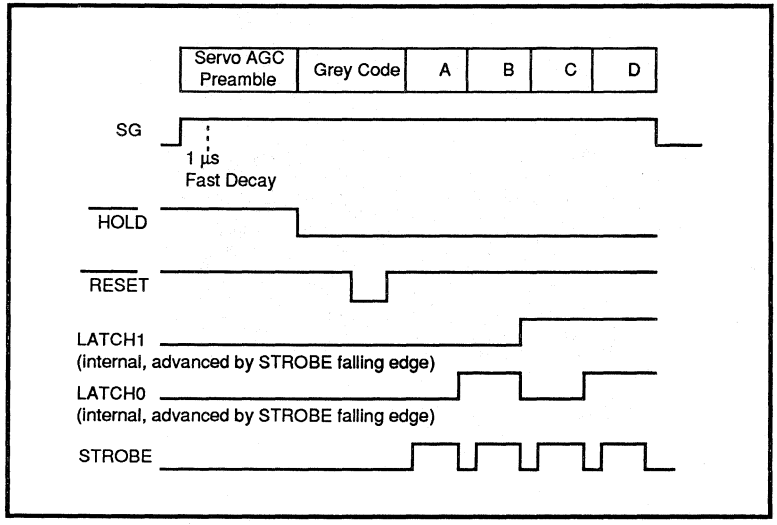


FIGURE 18: SSI 32P4731/42/42 Servo Control Sequence

Lab Experiment 6 SSI 32P4731 /41/42 Servo Mode Functionality
This lab experiment demonstrates the SSI 32P4731/41/42 Servo mode functionality. With the SG asserted, an amplitude modulated input can be applied to VIA. Photo 3B shows the analog input, STROBE, $\overline{\text{RESET}}$ and the servo outputs.

SERVO DIGITAL OUTPUTS

To support the servo timing, the SSI 32P4730/31/41/42/44/46 have two TTL digital outputs: $\overline{\text{RDIO}}$ and PPOL.

$\overline{\text{RDIO}}$	This pin must be configured as an output for this utility. In the Servo mode, a 10 ns pulse is generated for each qualified peak. This output is disabled, pulled to static '1', when either RG or WG is at logic 1.
PPOL	When RG and WG are both logic 0, this output represents the polarity of the peak being qualified. A logic 1 indicates a positive peak. A logic 0 indicates a negative peak.

Figure 19 illustrates the timing of these two digital outputs relative to the analog input.

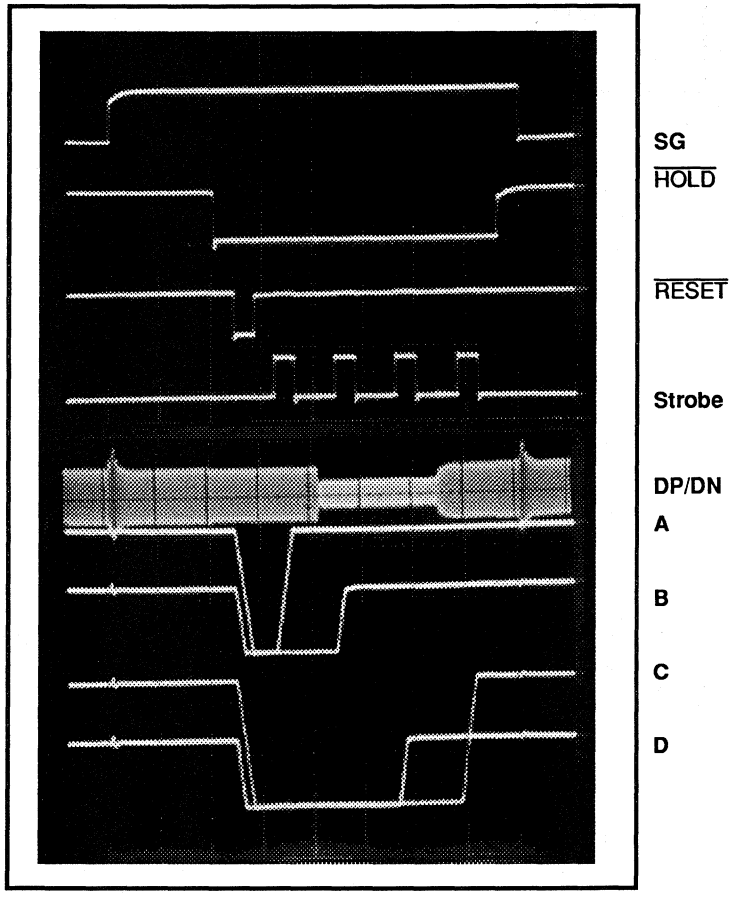


PHOTO 3B: SSI 32P4731/42/42 Servo Mode Functionality.

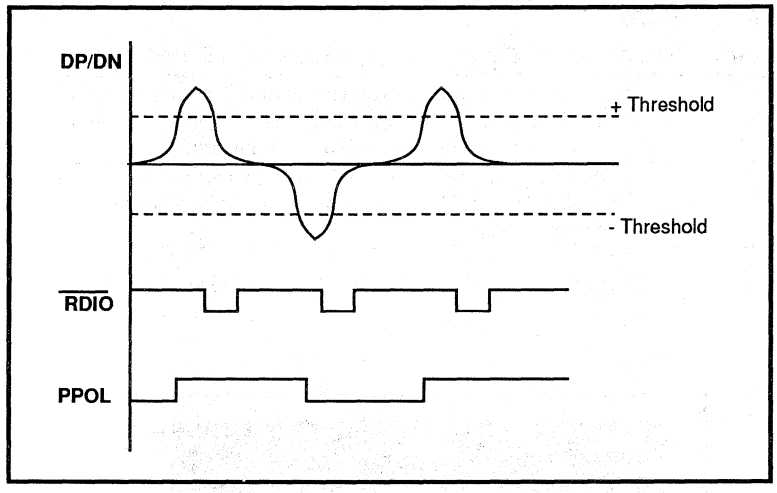


FIGURE 19: $\overline{\text{RDIO}}$ and PPOL Timing Relationship

WRITE MODE EVALUATION

In the Write mode, the SSI 32P4730/31/41/42/44/46 converts the NRZIN data into 1,7 RLL encoded data. Write mode is entered by asserting the write gate, WG, while the read gate, RG, is held to logic 0. In soft sector operation, the circuit generates an address mark and a preamble pattern. In hard sector operation, the circuit generates the preamble pattern without a preceding address mark. The NRZIN data is clocked into the encoder at each WCLK rising edge. WCLK should be synchronous with RRC. The encoded data appears at the $\overline{WD}$ output pin which feeds a write driver. The data separator PLL and the RRC are locked onto the time base generator output.

The $\overline{WD}$ is an active low signal. When an encoded '1' bit is to be written, a low pulse of 0.67 encoded bit period occurs at the $\overline{WD}$ output.

The SSI 32P4742 uses a dual bidirectional interface through NRZ1 and NRZ 0. NRZ data is clocked through two bits at a time into NRZ1 and NRZ0 at each rising edge. WCLK is synchronous with RRC which runs at half of the data rate.

ADDRESS MARK GENERATION

The address mark generation is only applicable to soft sector operation. One NRZ period after the WG 0-to-1 transition, the AMENB is asserted for at least 1 NRZ period and at most 27 NRZ period. The address mark pattern of two 8T's followed by two 12T's is automatically generated. With the NRZIN input kept at logic '0', 3T patterns are generated to follow the address mark pattern. From the WG 0-to-1 transition WCLK must be togling. The NRZIN input should be kept at logic '0' for at least 65 (for hard sector, at least 38) NRZ periods to ensure the complete preamble & bit sync pattern is written. The first nonzero NRZIN input bit indicates the end of the preamble pattern. After a delay of 8 NRZIN bit time periods (12 if Write Precomp is used), nonpreamble data begins to toggle out of WD. At the end of the NRZ data stream, at least eight additional NRZ bits are recommended before the WG returns to logic 0. WD stops toggling a maximumoft 2NRZ (RRC) time periods after WG goes low. See data sheet for Write mode timing information.

HARD SECTOR OPERATION

In hard sector operation AMENB is held low and no address mark pattern is genererated. The preamble pattern is generated in the same sequence as the soft sector operation. During preamble generation the WCLK is toggled and NRZIN data is held low ("0"). Termination of a hard sector write operation follows the same sequence as the Soft Sector of mode.

WRITE PRECOMPENSATION FUNCTION

The SSI 32P4730/31/41/42/44/46 supports a programmable write precompensation function, which can be enabled by Write Precomp Register: D3 = 1. The device examines the bit pattern to determine the write precomp direction as governed in Table 4.

TABLE 4: Write Precompensation Direction.

Bit N-2	Bit N-1	Bit N	Bit N+1	Bit N+2	Bit N Precomp Direction
1	0	1	0	1	None
0	0	1	0	0	None
1	0	1	0	0	Early
0	0	1	0	1	Late

Late = Bit N is shifted toward Bit N+1; Early = Bit N is shifted toward Bit N-1

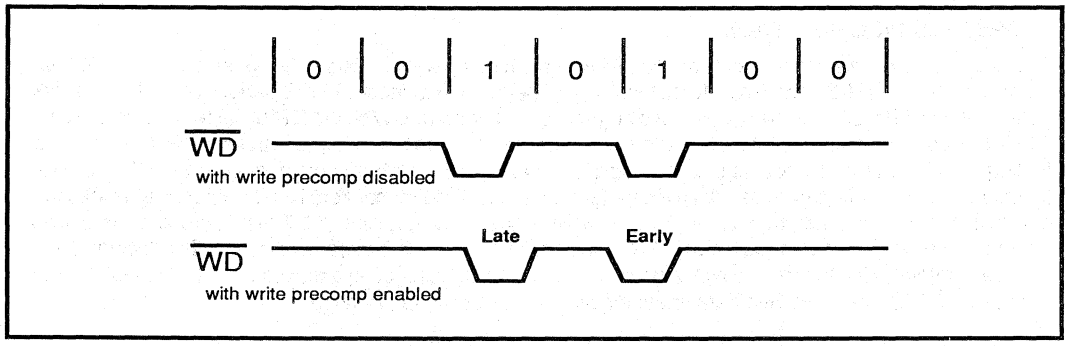


FIGURE 20: Write Precomp Effect on $\overline{WD}$.

WRITE PRECOMPENSATION FUNCTION (continued)

The 3 LSBs of the Write Precomp Register programs the amount of early write precompensation as an integral multiple (up to 7X) of4% of encoded bit period. Bits D6, D5, D4 of the write precomp register program the amount of late write precompensation as an integral multiple of 4% of the actual encoded bit period. For example, an early precomp magnitude of 16% of the encoded bit period is given by setting Write Precomp Register: D2-0 = 011.

The write precomp function is bypassed in the direct Write mode, see the following Direct Write Section.

RLL ENCODE FUNCTION

The SSI 32P4730/31/41/42/44/46converts the NRZIN data into 1, 7 RLL encoded bits as given in Table 5.

The write data output, $\overline{WD}$, is synchronized to the internal synthesized clock which can be asynchronous relative to the WCLK input. In the bit stream of the NRZ input, every two NRZ bits are paired together and encoded into three 1,7 RLL code bits. The pairing of the NRZ bits can be one of two combinations which, for discussion purposes, are termed as odd-even pair and even-odd pair. The odd-even pair and the even-odd pair will be encoded into different 1,7 RLL code bits. However, in the decode process, both pairings will result in the same NRZ pattern with a possible extra leading '0' bit. While a controller will re-frame the NRZ data, this does not create any problem in a system application.

TABLE 5: Encode Table for 1,7 RLL Code Set.

NRZ Data				Encoded Write Data			
Present		Next		Previous	Present		
D1	D2	D1	D2	Y3	Y1	Y2	Y3
0	0	0	X	0	0	0	1
0	0	1	X	0	0	0	0
0	0	1	X	1	0	1	0
1	0	0	X	0	1	0	1
1	0	1	X	0	0	0	1
0	1	0	0	0	0	0	1
0	1	0	0	1	0	1	0
0	1	1	0	0	0	0	0
0	1	1	0	1	0	0	0
0	1	0	1	0	0	0	1
0	1	0	1	1	0	0	0
0	1	1	1	0	0	0	0
0	1	1	1	1	0	0	0
1	1	0	0	0	0	1	0
1	1	1	0	0	1	0	0
1	1	0	1	0	1	0	0
1	1	1	1	0	1	0	0

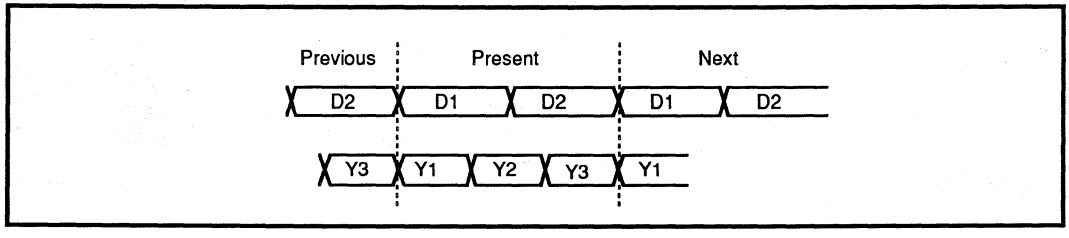


FIGURE 21: Definition of Y1-3 and D1-2 in Table 5.

Using an SSI 32P4730/31/41/42/44/46 Single-Chip Read Channel Device

RLL ENCODE FUNCTION

Consider the following NRZ bit pattern: $0AD340_{HEX}$ = 00101011010011010000

The two possible NRZ pairings are:

Odd-even pair - 00	10	10	11	01	00	11	01	00
Even-odd pair - 01	01	01	10	10	01	10	10	00

The encoded bits are:

Odd-even pair - 010	010	010	100	001	010	100	001	001
Even-odd pair - 000	001	000	010	101	000	010	101	001

DIRECT WRITE FUNCTION

The SSI 32P4730/31/41/42/44/46 supports the direct write function by setting Control B Register: D0 = 1. In the direct Write mode, the 1,7 RLL encoder and the write precompensation are bypassed in the Write mode. The NRZIN data is buffered and appears at the $\overline{WD}$. This allows the user to perform DC erase and media test

ENDEC I/O AND TEST POINTS

NRZIN	NRZ Input: TTL compatible write data NRZ input
NRZO NRZ Output Data:	NRZ data CMOS compatible output.
WCLK	Write clock: TTL compatible write clock input. Must be synchronous with the write data NRZ input and RRC. For short cable delays, WCLK may be connected directly to the RRC pin. For long cable delays, WCLK should be connected to an RCLK return line matched to the NRZ bus line delay.
RRC	Read Reference Clock: Read clock CMOS compatible output, referenced to the time-base generator VCO in non-Read mode and the data seperator VCO in Read mode.
AMENB	Address Mark Enable: TTL compatible input to generate an address mark in Write mode, or detect an address mark in Idle mode.
AMD	Address Mark Detect: CMOS compatible output. A high level indicates adress mark search status. A low level output appears when an address mark has been detected.
DACOUT	Multiplexed DAC output: when window shift register (05 HEX): D7-6 = 11, DACOUT represents the write precompensation early magnitude setting DAC. The voltage at DACOUT in this mode can be estimated as 4.265 - (0.01966 $DACW_p$) where $DACW_p$ is equal to the three bit register value of the early write precompensation magnitude.

Silicon Systems, Inc., 14351 Myford Road, Tustin, CA 92680-7022 (714) 573-6000, FAX (714) 573-6914

Servo Controllers and Motor Drivers Application Note

Servo Controllers and Motor Drivers

INTRODUCTION

Silicon Systems offers a wide range of servo controllers and motor drivers. This applications note is a comprehensive design guide explaining how the Silicon Systems servo family members are different and how to apply each of them in a design. The servo family consists of VCM (voice coil motor) predrivers, integrated power drivers, demodulators, data conversion, and digital signal processing devices. The servo devices discussed in this applications note are:

DEVICE	FUNCTION
SSI 32H569	12V VCM MOSFET Predriver
SSI 32H6230	12V VCM MOSFET Predriver
SSI 32H6231	12V VCM MOSFET Predriver
SSI 32H6240	12V VCM Bipolar Predriver
SSI 32H6510	5V Power Driver
SSI 32H6810A	5V Servo/Spindle Power Driver
SSI 32H6811	5V Servo/Spindle Power Driver with DAC
SSI 32H6812	5V Servo/Spindle Power Driver with DAC and SHOCK detection
SSI 32H6820	12V Servo/Spindle Predriver
SSI 32H6825	12V Servo/Spindle Predriver
SSI 32H6520	5V Embedded Servo Demod with ADC and DACs
SSI 32H6521	5V Embedded Servo Demod with ADC and DACs
SSI 32H4633	5/12V Servo/Spindle Predriver with demod

The Silicon Systems servo product family consists of several other members not thoroughly discussed in this applications note. The SSI 32H6210 is a 12V dedicated servo demodulator compatible with the SSI 32H6220 servo controller and both are detailed in the applications section within their respective data sheets. The SSI 32H6215 is a 5V dedicated servo demodulator similar in function to the SSI 32H6210. The Silicon Systems digital signal processor SSI 32H6830 referred to as the SEEKER™ offers various servo control functions which are referenced in this applications note. However, a separate applications note will be available covering the SSI 32H6830.

SERVO CONTROLLERS

The term servo controller is a broad one. This term can include many different hardware functions. Silicon Systems uses the term servo controller to refer to devices which contain both demodulation and data conversion functions. Silicon Systems servo demodulators may be a single function device such as the SSI 32H6210 or embedded as part of a servo controller. Silicon Systems data conversion functions are A/D and D/A converters which may appear in different configurations. Servo controllers will always include both A/D and D/A data conversion functions while many Silicon Systems servo drivers include only the D/A converter. The SSI 32H6830 SEEKER™ is a servo controller including A/D and D/A data conversion functions and digital signal processing hardware.

SERVO DEMODULATORS

Disk drives using a voice coil motor (rotary or linear VCM) require a closed-loop position control system to center the data head over the target track. The control system uses position information indicating actual head position and compares this to the desired position so that a compensating VCM error current can be generated. Figure 1 illustrates the elements making up this control system. The position information usually consists of two parts: coarse position giving track number; fine position information relative to each track and used to center the data head.

Position information is placed in servo frames. Dedicated servo systems reserve an entire data surface for the position information. Embedded servo systems interleave position information with user data. Servo demodulators decode the fine position information encoded in each servo frame.

The SSI 32H6210 and SSI 32H6215 are dedicated servo demodulators and applications information accompanies their respective data sheets. Dedicated servo systems benefit from a position signal which is essentially continuous in time. A disadvantage of dedicated servo is that the servo head and data head may become mechanically misaligned with time and temperature. All following discussion addresses Silicon Systems components applied in embedded servo systems.

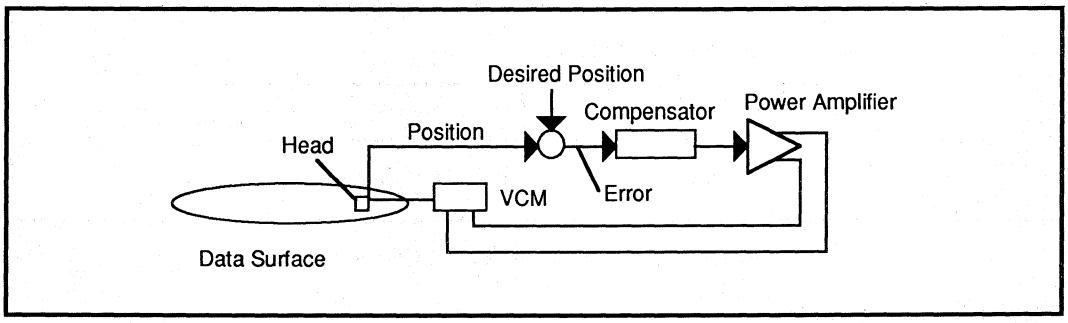


FIGURE 1: Closed-loop Position Control System

The Embedded Servo Frame

The embedded servo frame is recorded on the same surface as the user data. The embedded servo frame is interleaved with user data in a constant periodic manner. Because of this interleaving, the embedded servo system is a sampled system. Being a sampled system, it lends itself to digital implementation. Figure 2 illustrates how the embedded servo frame is interleaved with user data.

The embedded servo frame itself consists of application specific fields. Generally, the servo frame is made up of several fields such as the servo mark, digital field, and analog fine position bursts. The beginning of the servo frame is identified and qualified by the servo mark. The digital field is recorded usually with a simple encoding scheme which can be decoded using some form of asynchronous detection. The position bursts are one or more cycles of continuous carrier. Most embedded servo systems today employ four bursts so that the fine position is recorded in quadrature to improve demodulator linearity. Figure 3 illustrates the components of the embedded servo frame.

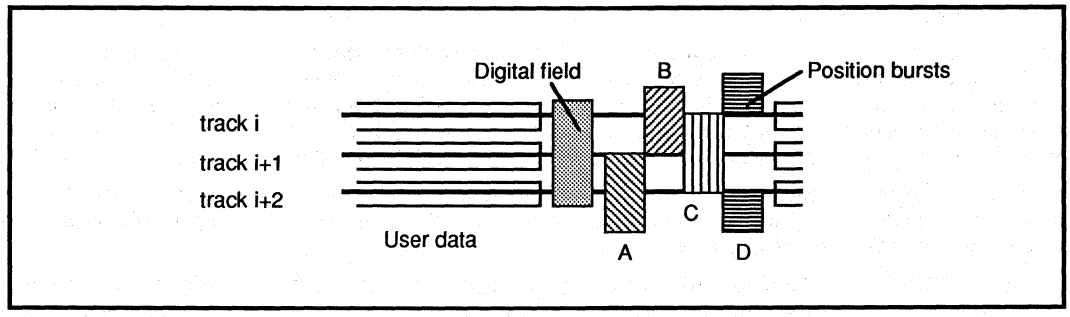


Figure 2: Embedded Servo Frame with Four Bursts

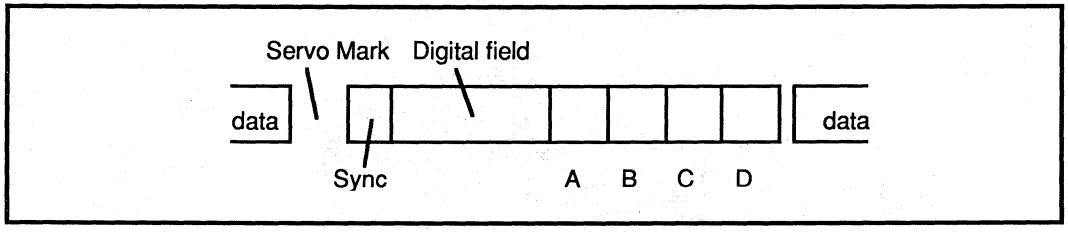


FIGURE 3: Embedded Servo Frame Components

SERVO DEMODULATORS (continued)

Demodulator Timing Generation

The embedded servo frame relies upon precise timing for decoding the various servo fields. The timing generator is usually implemented in a digital ASIC and clocked from a crystal timebase. The timing generator typically performs the following:

1. Anticipate and detect the servo mark and switch the read channel into servo mode
2. Qualify the servo mark
3. Synchronize the bit decoder for the digital field
4. Decode and capture the digital field
5. Perform basic checking of the digital field
6. Initialize the fine position demodulator
7. Hold the AGC during fine position bursts
8. Generate timing windows for position demodulation
9. Begin the A/D conversion of the first burst
10. Signal the micro controller of servo frame status
11. Restore normal data mode

The digital timing generator is usually clocked at a high frequency such as 40 MHz. This frequency is determined by the sample rate requirements necessary to asynchronously decode the digital field bits. As an example, Figure 4 illustrates a complete servo system including read channel and digital timing ASIC.

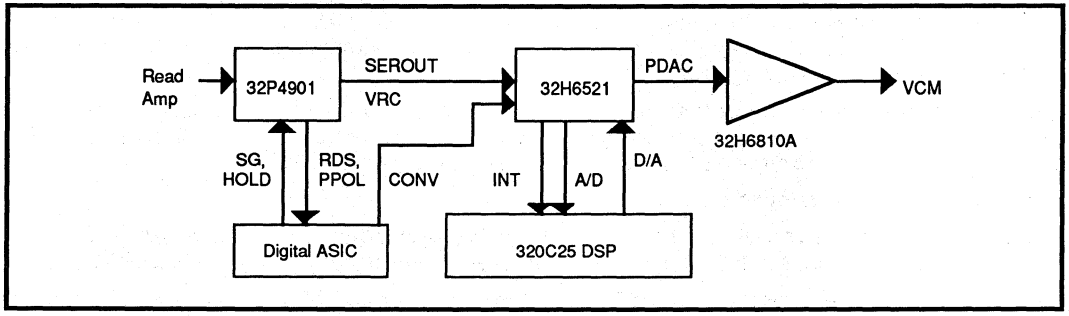


FIGURE 4: Servo System Interconnection Example

Area and Peak Detectors

Area and peak detection are different approaches to demodulating the fine position information contained in the servo frame. These two detection schemes differ in their respective features.

Area detection relies on integration of some aspect of the fine position burst signal. Area detection tends to offer superior noise rejection but requires greater timing precision. Symmetrical noise appearing during the burst will both add and subtract from the integral thereby canceling itself out. The integration window should be synchronous with the burst zero crossings for consistent area demodulation and some form of zero-crossing detector is required. Area detection can be performed over fewer cycles of burst and therefore the total servo frame time can be reduced yielding greater user data capacity.

Peak detection is simpler to implement but is more sensitive to noise. The peak detector sampling window may be enabled asynchronously with the burst carrier and therefore this type of demodulator is most compatible with digital timing ASICs. Though simple in concept, the peak detector always needs some form of signal conditioning to improve noise rejection. The attack time of the peak detector can be slowed so that the final demodulated value represents an average of multiple cycles. This averaging approach reduces the contribution of a noise spike at the expense of requiring more burst cycles to complete the sample.

The following table lists various Silicon Systems devices which offer embedded servo demodulation functions:

DEVICE	TYPE	COMMENT
SSI 32H4633	Peak	Four peak detectors
SSI 32H6520	Area	Four area detectors
SSI 32H6521	Area	Four area detectors
SSI 32H6830	external	Four differential A/D inputs
SSI 32P544	Peak	Dual peak detectors
SSI 32P3013/15/16	Peak	Four peak detectors
SSI 32P3031	Peak	Dual peak detectors
SSI 32P4741/42/46	Peak	Four peak detectors
SSI 32P4901	rectifier	Full wave rectifier only

SERVO DEMODULATORS (continued)

Read Channel and Servo Controller Interface

The interface between the servo controller and the read channel will be determined by the type of embedded servo demodulator used. Many read channel devices include peak detectors which will feed an analog multiplexer in the servo controller. Other read channel devices full-wave rectify the read signal and the servo controller demodulates the position signal using area integration.

The read channel and servo controller interface is best illustrated by two examples. The first example relies upon peak detection performed in the read channel and data conversion in the servo controller. The second example demodulates the servo position signal in the servo controller using area integration.

Peak Detection and Data Conversion

An example which implements peak detection in the read channel device and data conversion in the servo controller is found in the 32P4746/SSI 32H6521 interface. This interface consists of four signals illustrated in Figure 5.

A servo reference voltage of approximately 2.25V is supplied by the servo controller from the band-gap reference on the SSI 32H6521 to the SSI 32P4746 SREF pin. The SSI 32P4746 provides three processed position signals representing burst differences A-B, C-D and sum A+B. These three position signals are zero referenced to SREF such that when A=B, the voltage on the BURST A-B pin will be SREF.

The processed bursts from the SSI 32P4746 are directly connected to the SSI 32H6521 analog inputs ADCIN2, ADCIN3, and ADCIN4. A/D conversions may be started from the digital timing generator by triggering the ADCSTR pin on the SSI 32P4746 or by the microcontroller reading the SSI 32H6521 register address three.

In this example, the area integration capability of the SSI 32H6521 was not used; instead, the external A/D inputs through the analog multiplexer were utilized to acquire the position information. The SSI 32H6520 read channel interface is identical to the SSI 32H6521.

The SSI 32H6830 SEEKER™ DSP offers a similar data conversion interface. The SSI 32H6830 does not contain area integrators but does offer external A/D inputs like the SSI 32H6521 used above. Figure 6 illustrates the SEEKER™ interface which makes use of a configurable differential amplifier useful in scaling the burst amplitude to match the A/D conversion range.

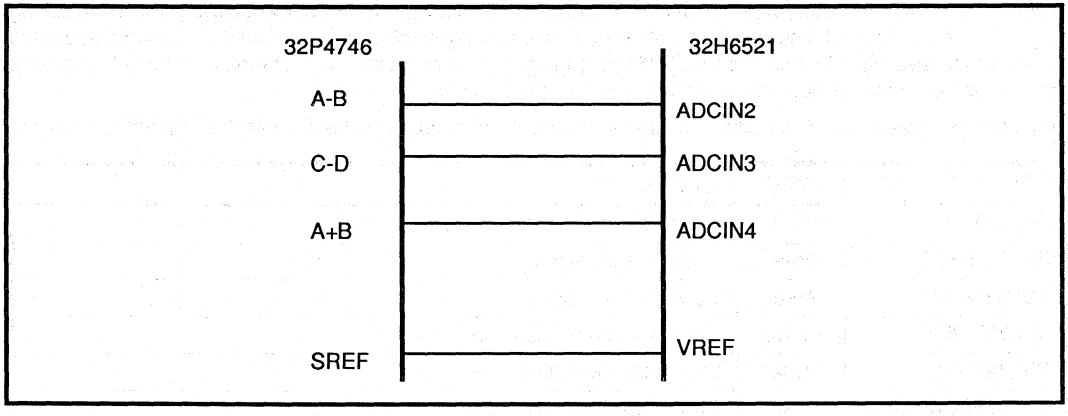


FIGURE 5: Peak Detection Interface Example

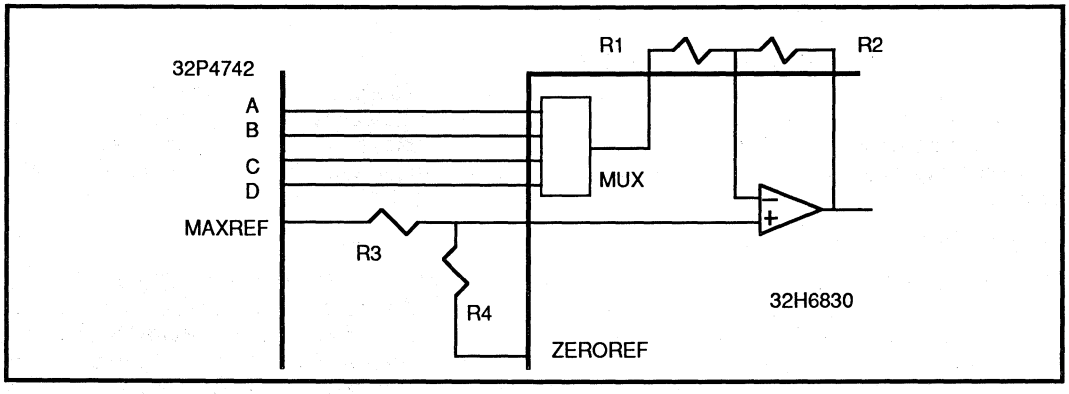


FIGURE 6: Alternative Peak Detection Example

Full-Wave Rectification and Area Integration

An example which implements full-wave rectification in the read channel device and area integration in the servo controller is found in the 32P4901/SSI 32H6521 interface. This interface consists of two signals illustrated in figure 7.

The read channel device is responsible for full-wave rectifying the servo burst. The servo controller accepts from the read channel, the full-wave rectified signal and zero signal reference. The SEROUT pin of the SSI 32P4901 is the full-wave rectified signal and the zero reference is output on pin SERREF. A differential amplifier in the servo controller internally level shifts the position signal for integration and presentation to the analog multiplexer for A/D conversion. Discrete resistors configure the integration gain constant by connecting the SSI 32H6521 SERIN and SREF pins to the SSI 32P4901 SEROUT and SERREF pins respectively.

The SSI 32H6520 read channel interface is identical to the SSI 32H6521. The SSI 32H4633 includes a programmable gain differential amplifier and peak detector which offers a similar interface as that of the SSI 32H6521.

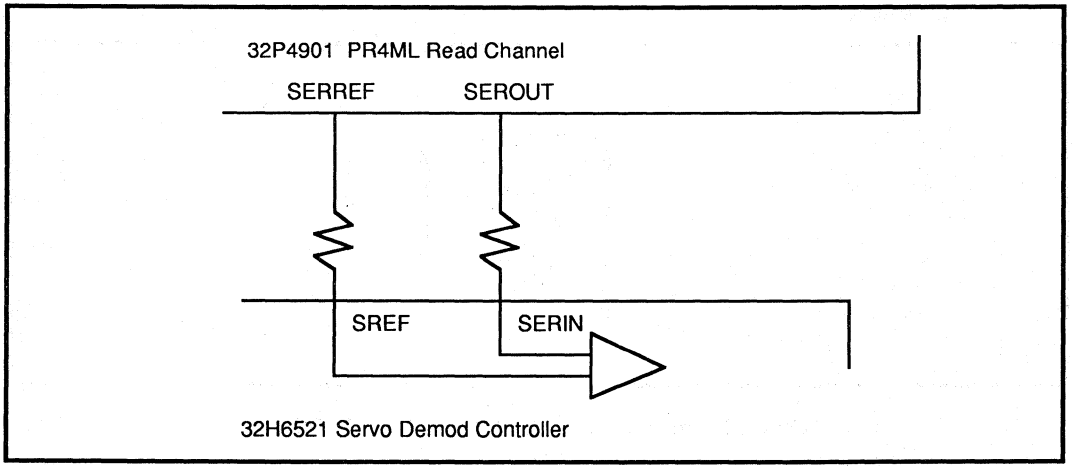


FIGURE 7: Area Detector Example

SERVO DEMODULATORS (continued)

Matching Signal Levels and Conversion Ranges

The electrical interface between the read channel and the servo controller consists of reference offsets, burst signal levels, and A/D conversion ranges. In each application, the reference and signal level of the servo burst must be matched to the servo controller A/D converter. There is considerable variety in Silicon Systems read channel servo interfaces and this section provides design details for the three representative examples outlined in the prior section.

The 32P4746/SSI 32H6521 Interface

The 32P4746/SSI 32H6521 servo interface is illustrated in figure 5. With VREF supplied by the SSI 32H6521 being 2.25V, the voltage on the A-B and C-D pins will be 2.25V when the differences are zero. The servo AGC level is programmable in the SSI 32P4746 and may be set as low as 0.75V. This lower value is preferred because the signal swing levels will be closer to the range acceptable by the A/D converter. Figure 8 illustrates the burst signal level swing compared to A/D conversion range. Note that the differencing pins (A-B and C-D) are internally amplified by 2 prior to summing with SREF while the summing pin (A+B) is unity gain.

In this example with the servo level set for 0.75V, the differencing signal swing exceeds the conversion range of the A/D converter while the zero references are identical. The differencing swing will range from 0.75 up to 3.75V absolute or ± 1.5V relative to VREF. The summing signal at the A+B pin will be 0.75V relative to VREF. The A/D conversion range of the SSI 32H6521 is ±1.125V relative to VREF.

For the differencing channels A-B and C-D, the effect of exceeding the A/D conversion range is not important. While on track, the difference should be fairly small and well within the A/D conversion range. The A/D conversion range is 75% that of the potential signal swing and sufficiently covers the linear range available from two bursts. When the difference is large, by design the alternate burst pair should be used since A and B are laid down in quadrature with C and D. Negative conversion values will be read when A<B or C<D and positive values are read when A>=B or C>=D.

The summing channel A+B voltage is always positive relative to VREF. At track center, one-half of the peak A detector and one-half the peak B detector should sum up to approximately 0.75V on the A+B pin. This value is well within the A/D converter range. The sum A+B is used to normalize the difference A-B to yield a fractional tracking error. The peak detector window timing should be "commutated" so that the bursts to track on are captured in the A and B detectors.

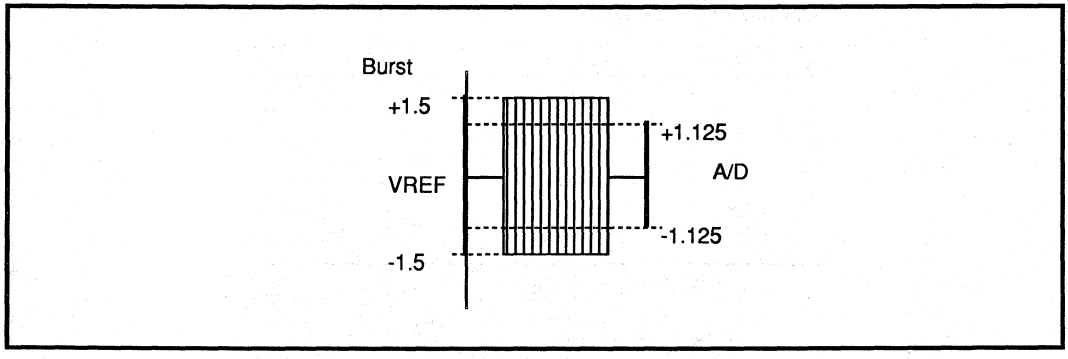


FIGURE 8: Truncated SSI 32P4746/SSI 32H6521 Range

The 32P4742/SSI 32H6830 Interface

The 32P4742/SSI 32H6830 servo interface is illustrated in figure 6. With the SSI 32H6830 VBGAP supplied externally (such as from a SSI 32H6810A) of 2.25V, the A/D zero reference will be 5/9ths VBGAP or 1.25V. The SSI 32P4742 internally generates a maximum reference MAXREF which is approximately 3V and corresponds to slightly greater than the greatest burst peak amplitude possible (available on the A,B,C, or D pins). The four bursts are internally referenced to a base line which is approximately 0.5V and is derived from MAXREF. The servo AGC level is adjustable but in this case, selection of 1V is assumed since there is no advantage in a smaller signal. With the 1V servo level, the signals at the burst pins A,B,C, and D will vary between 0.5 and 2.75V approximately. Note that each burst pin from the SSI 32P4742 is amplified internally by 2.25.

This interface requires both signal level scaling and reference matching. The SSI 32H6830 offers an interface well suited to this task. The burst signals are applied to an analog multiplexer which feeds the differential amplifier through a common resistor thereby minimizing offsets. Level scaling is achieved by selecting the gain determining resistor ratio R2/R1 and reference matching through the divider made up of R3 and R4.

Figure 9 illustrates the signal levels involved in this SSI 32P4742/SSI 32P6830 interface. Assuming the burst signals range from zero to 3V provides some saturation margin. The A/D conversion range is 2V peak-to-peak. The necessary signal level scaling will therefore map 3V to 2V and will be a gain of 2/3. As an example, choosing R1 of 30K and R2 of 20 kΩ provides such a gain.

The reference divider is chosen by selecting a nominal or on-track burst amplitude. In this example, 1.5V (one-half the assumed swing) was selected. By these design choices, when the bursts are 1.5V then the A/D conversion should indicate a value of 0. With this choice, the voltage drop across R3 will be 1.5V and R4 will be 0.25V. Choosing a divider current compatible with the MAXREF source such as 100 microamps, yields resistances of 15 kΩ for R3 and 2500Ωs for R4.

The differential amplifier in the SSI 32H6830 will invert the sense of the burst signal. With the values chosen in this design example, bursts yielding 1.5V on the output pins will yield a conversion value of zero. A missing burst of zero amplitude will yield a maximum positive conversion value (by design it will not be saturated) and a peak burst will yield a minimum negative conversion value (again not saturated by the design choices).

The assignment of nominal or on-track burst amplitude is not critical. This nominal amplitude will translate to the zero value read from the A/D converter. In practice, this nominal on-track value will vary and therefore, the track following algorithm must difference the bursts to derive a purely relative measurement without relying on absolutes. The best nominal value will be close to the center of burst variation to maximize the dynamic range available in the A/D converter.

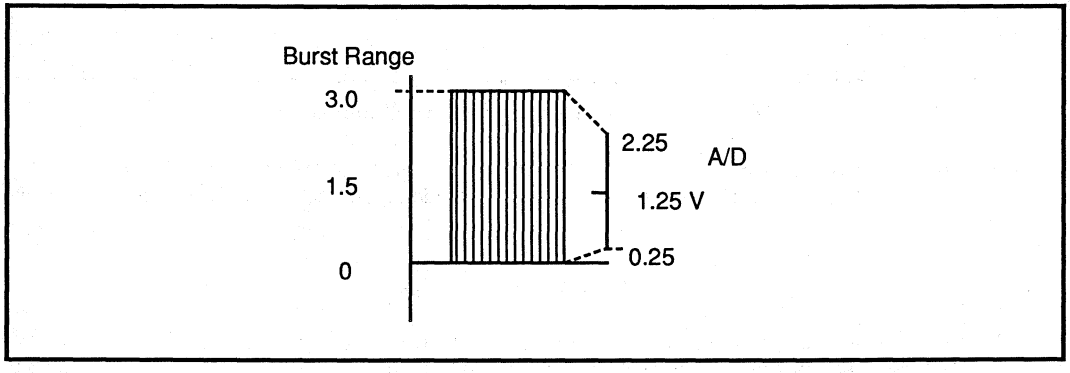


FIGURE 9: Shifted and Scaled SSI 32P4742/SSI 32H6830 Range

SERVO DEMODULATORS (continued)

The 32P4901/SSI 32H6521 Interface

The 32P4901/SSI 32H6521 servo interface is illustrated in figure 7. The interface between read channel and servo controller is particularly simple in this interface. A single signal SEROUT is generated by the SSI 32P4901 which is the full-wave rectified version of the bursts. The SEROUT signal is referenced to the voltage on the SERREF pin which is in turn generated internally within the SSI 32P4901. The offset between SEROUT and SERREF is never negative and will be no more than 50 mV.

SERREF is approximately 2V. The AGC section drives the differential voltage across the DP/DN pins to 1.27V peak-to-peak. The relative output voltage at SEROUT will be the product of the full-wave rectifier gain and the burst signal peak-to-peak amplitude. In the 32P4901, the full-wave rectifier gain is typically 0.75 so that the peak voltage from the rectifier will reach approximately 1V.

Setting the Area Integration Gain

The SSI 32H6520 and SSI 32H6521 implement area integrators. An external resistor connecting the 32P4901 SEROUT pin to the SSI 32H6521 SERIN pin configures the gain constant of the integrator. Calibration is provided to tweak the gain constant by programming the gain of the input differential amplifier. Figure 10 illustrates the area integrator arrangement.

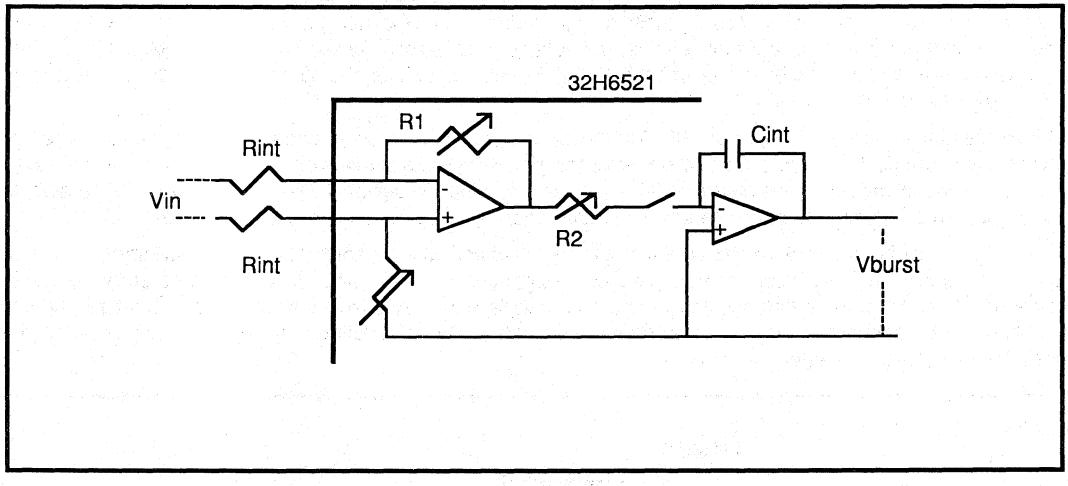


FIGURE 10: Area Integrator with Calibration Feature

Note that in this integrator, the ratio of R1 and R2 is the means to tweak the gain. Further, the gain is adjusted by the ratio of R1 and R2 as indicated in the transfer function relating integrator output to SERIN pin input below:

$$V_{BURST} / V_{SERIN} = \frac{R1}{R2} \cdot \frac{1}{sR_{INT}C_{INT}}$$

R_{INT} is the resistance which externally sets the integrator gain constant. R1 and R2 are internal and their respective ratio is programmable through the GAIN bits in register 1. The GAIN bits provide for gain adjustment of -2.8 to +3.2 dB which is sufficient to account for variation in the internal capacitor C_{INT} and R_{INT}. The tolerance of C_{INT} is 20% and the programmable gain offers adjustment of at least 28% so that a 5% tolerance R_{INT} resistor is acceptable.

The area integrators are internally level shifted such that zero input will yield an integral voltage of approximately 1.5V. The output of the integrator is sampled with an A/D converter with a zero reference of nominally 2.25V and an A/D conversion range of ± 1.125V. This implies that the peak integrator output should not exceed 1.875V as illustrated in figure 11. To allow for some margin, limit the peak integrator value to 1.5V.

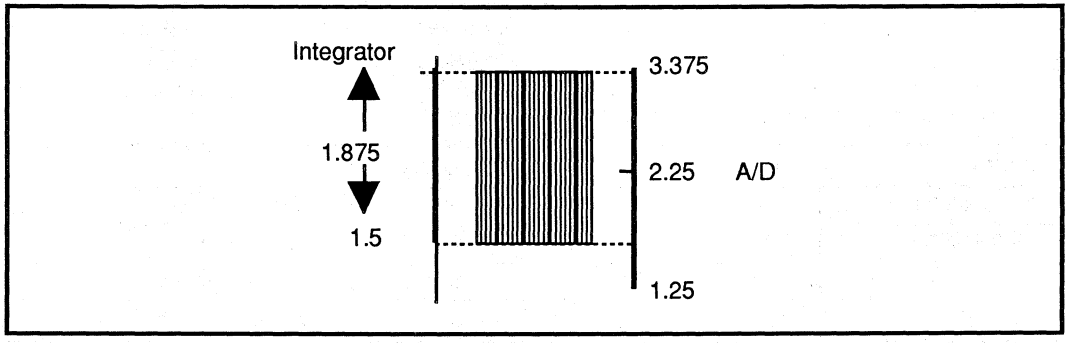


FIGURE 11: SSI 32P4901/SSI 32H6521 Range Shifting

As a design example, consider a maximum rectified burst amplitude output of 1V at SEROUT relative to SERREF from the 32P4901 which is V_{SERIN} below. The integration window is to be one microsecond and the peak integrated burst V_{BURST} is 1.5V. Choose RINT from the formula:

$$R_{INT} = \frac{V_{SERIN}}{V_{BURST}} \cdot \frac{T_W}{C_{INT}}$$

where T_W is the window width. In this example, R_{INT} is found to be approximately 66 kΩ.

Demodulator Offset Calibration

Demodulator offset calibration is a procedure which determines the servo burst signal base line. For all three read channel/servo controller interface examples given in this applications note, this calibration is implemented by placing the read channel into a specific mode which in turn forces the burst signal to a known voltage. For example, the SELSREF pin in conjunction with $\overline{SG}$ high forces SEROUT to the reference in the 32P4901. Having fixed the burst signal, an A/D conversion is performed and the corresponding value read indicates the base line or zero signal level. Each burst will require a base line measurement. This calibration may account for offsets in the read channel, servo controller analog multiplexer offset, and servo controller integrator offset. Any offset in the A/D converter itself is calibrated out separately as detailed in a later section.

A second calibration may be performed with the SSI 32H6521. Adjustment of the integrator gain constant as detailed in a prior section is implemented by adjusting the GAIN bits in register 1. After establishing the base line, the servo system may tweak the gain so that the peak burst amplitude is adjusted to some design target value such as 1.5V (relative to the base line).

SERVO CONTROLLERS (continued)

ANALOG TO DIGITAL CONVERSION

The servo controller provides A/D conversion necessary in a digital servo system for a hard disk drive. The A/D converter captures the demodulated servo position signals as discussed in detail in the prior section. In addition, the A/D may be used to capture samples of positioner motor current and other application specific signals.

Silicon Systems servo controllers all offer extensive and flexible A/D conversion resources. A/D conversion consists of source selection through an analog multiplexer, an A/D converter, and register interface. The Silicon Systems servo controllers listed below all offer A/D conversion:

DEVICE	RESOLUTION	SOURCES	COMMENT
SSI 32H4633	8-bit	16	1 external input
SSI 32H6520	10-bit	8	4 external inputs
SSI 32H6521	10-bit	8	4 external inputs
SSI 32H6830	10-bit	6	all external inputs

Analog Multiplexer

The analog multiplexer is register accessible and bits in the register are decoded to determine the source which will be routed to the A/D converter. The lists below illustrate the diversity in multiplexer sources:

SSI 32H4633	SSI 32H6520/21	SSI 32H6830
BURSTs 1..4	BURST 1..4	IN 2..5 bursts
PES 2..0	ADCIN 1..4	IN 0..1 external
N and Q	VREF	
ERR and SOUT		
SENSE		
ADCIN		
VREF		
SUM 1 and 2		

The SSI 32H4633 includes sources from the embedded servo peak detector for BURST, analog differenced signals for bursts pairs in PES 1 and 2, analog summed signals at SUM 1 and 2, dedicated servo demodulator signals PES 0 and N/Q, VCM power amplifier signals ERR and SOUT, spindle motor sense current at SENSE, an external A/D input at ADCIN, and a calibration input of VREF. The SSI 32H6520 and SSI 32H6521 provide selection of the four integrator BURST signals, four external A/D inputs at ADCIN 1..4, and VREF for calibration. The SSI 32H6830 divides source inputs into a group of four in IN 2..5 intended for burst peak capture including a differential amplifier, and two in IN 0..1 for external use.

ADC Conversion

Starting a Conversion

A/D conversion is started in the various Silicon Systems servo controllers in different ways. Two methods of starting a conversion are possible; hardware conversion relies upon a digital timing signal which initiates the A/D conversion generated from the digital timing ASIC. Programmed conversion occurs when the microcontroller reads or writes a register to initiate the next A/D conversion. The table below lists how each Silicon Systems servo controller initiates A/D conversion:

DEVICE	HARDWARE TRIGGERED	PROGRAM INITIATED
SSI 32H4633	none	Write MUX register
SSI 32H6520	ADCSTR	Read MSB of A/D
SSI 32H6521	ADCSTR	Read MSB of A/D
SSI 32H6830	START	none

In the SSI 32H4633, conversions are initiated after writing register 3 with the analog multiplexer selection code. The conversion will be complete and available in six microseconds.

The SSI 32H6520 and SSI 32H6521 offer two methods of starting a conversion. The ADCSTR pin is a hardware trigger which when raised high begins the first A/D conversion. This feature is intended to implement a pipelined conversion scheme such that the first burst is converted automatically by hardware, once the first conversion is complete the microcontroller is notified, and the microcontroller completes the conversion of the remaining bursts by reading the A/D MSB register. Figure 12 illustrates this pipelining feature of the SSI 32H6520/21. Since the A/D value is 10 bits wide in the SSI 32H6520/21, two 8-bit register reads are required. When all ten bits are desired, read the LSB first followed by the MSB to begin the next conversion. If only eight bits of resolution are needed, the LSB may be ignored.

The SSI 32H6830 implements totally automatic conversion of all six input sources. This conversion is triggered by the rising edge of the START signal. The converted values are all available in their corresponding registers which are accessible to the DSP program.

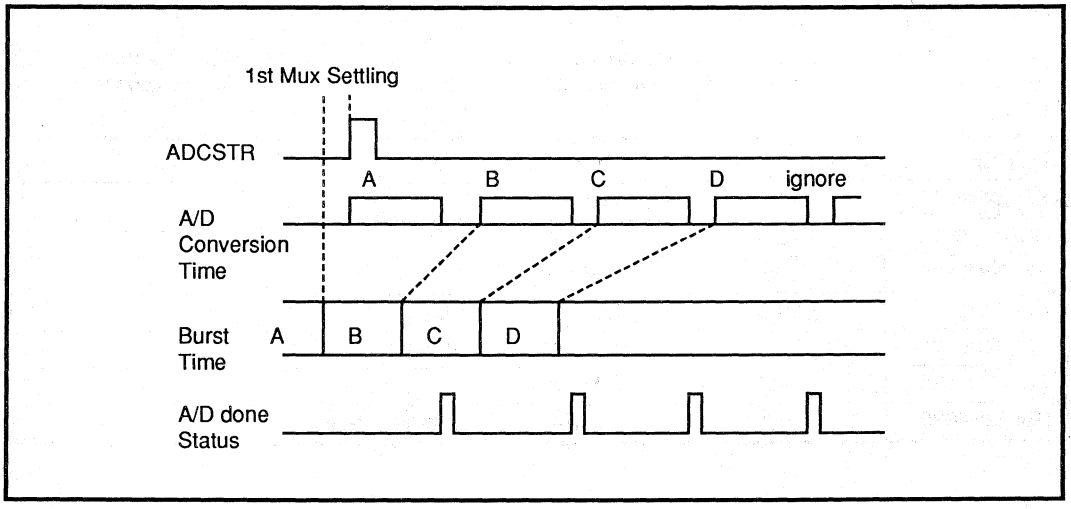


FIGURE 12: A/D Conversion Pipelining in SSI 32H6521

ANALOG TO DIGITAL CONVERSION (continued)

Conversion Time

A/D conversion time is specified for each servo controller. Total conversion time consists of delay through the multiplexer, actual A/D conversion time, and in some cases an access latency. In some devices, there is an additional digital latency time which is due to internal clocking. This latency will vary from 0 to 2 µS. The table below provides conversion timing for the various servo controllers discussed in this note:

DEVICE	MULTIPLEXER	CONVERSION	LATENCY	TOTAL (max)
SSI 32H4633	included	4.0 µs	2.0 µs	6.0 µs(max)
SSI 32H6520	1 µs	2.5 µs	0	3.5/2.5 µs Note 1
SSI 32H6521	1 µs	2.5 µs	0	3.5 µs Note 1
SSI 32H6830	included	2.0 µs	12 µs Note 2	12 µs Note 2

[1]For the SSI 32H6520/21, the multiplexer time can be pipelined and therefore will apply only to the very first conversion. Each successive conversion requires only 2.5 µS.

[2]The SSI 32H6830 automatically converts all six sources and stores the results in separate registers. Each conversion (including multiplexer delay) is 2 µS so that the total latency indicated above is really the time from START assertion to the DSP running.

ADC Offset Calibration

ADC offset calibration is implemented by forcing a known voltage into the A/D converter. This forcing voltage is the reference voltage the A/D converter uses internally such as VREF. In the SSI 32H4633, this VREF source is selectable in the MUX register. For the SSI 32H6520/21 devices, a separate bit named ADC CALIB in the ADC MSB data register overrides all other MUX selections. ADC offset calibration should be performed first and represents the electrical offset error of the A/D and multiplexer block. Later measurements may compensate for this electrical offset by subtracting this offset value in firmware.

DIGITAL TO ANALOG CONVERSION

Many Silicon Systems servo devices include D/A converters. Some of these devices are servo controllers while others are servo motor predrivers and drivers. The table below identifies those devices with D/A converters and their features:

DEVICE	RESOLUTION	COMMENT
SSI 32H6811	10-bit	Dual spindle and VCM DACs
SSI 32H6812	10-bit	VCM DAC
SSI 32H6820	8-bit	VCM DAC
SSI 32H6520	10-bit	Dual DACs with separate reference
SSI 32H6521	10-bit	Dual DACs with separate reference
SSI 32H4633	8-bit	VCM DAC
SSI 32H6830	10-bit	Dual DACs with separate reference

D/A conversion time may consist of two parts in some devices. D/A conversion time refers to the time taken by the D/A converter to settle within some specified percentage of the final value. In some devices, there is an additional digital latency time which is due to internal clocking. This latency will vary from 0 to 2 μS. The table below indicates the D/A conversion times for these devices:

DEVICE	CONVERSION	LATENCY	TOTAL
SSI 32H6811	4.0 μs		4.0 μs
SSI 32H6812	4.0 μs		4.0 μs
SSI 32H6820	4.0 μs		4.0 μs
SSI 32H6520	2.5 μs		2.5 μs
SSI 32H6521	2.5 μs		2.5 μs
SSI 32H4633	4.0 μs	2.0 μs	6.0 μs
SSI 32H6830	4.0 μs		4.0 μs

Strobe Mode

The SSI 32H6520 and SSI 32H6521 offer D/A strobe modes which allow the two D/A outputs to change simultaneously. Strobe mode is selected by manipulating the STBEN1 and STBEN2 bits in register 2. The idea of strobe mode is to allow time for the microcontroller to compute and update the D/A registers and then with a single register write, simultaneously direct both D/As to assume their new values. Figure 13 illustrates how the strobe bits may be used in an application seeking to change the D/A voltages synchronously.

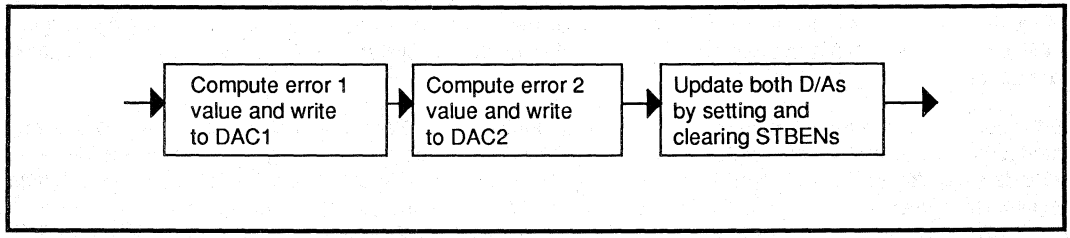


FIGURE 13: Using STBEN to Synchronously Update Both D/As

Switched Capacitor D/As

Some Silicon Systems servo controllers implement switched capacitor D/As instead of static ladder D/As. Switched capacitor D/As must be updated at a minimum frequency or else they will drift from the programmed value. For all Silicon Systems capacitor D/As, an update frequency of at least ten Hz will insure insignificant drift effects. The following servo controllers implement capacitor D/As:

SSI 32H6811
SSI 32H6812
SSI 32H6820
SSI 32H6520
SSI 32H6521
SSI 32H6830

SERVO CONTROLLERS (continued)

DIGITAL INTERFACE

The digital interface between the microcontroller and the servo controller varies considerably between individual device types. Some devices are parallel bus oriented with address, data, and control lines. Other devices rely upon a high speed synchronous serial link with an address/data protocol. The SSI 32H6830 is a DSP with internal A/D and D/A resources which appear as internal registers. The table below identifies the interface type for each servo controller:

DEVICE	INTERFACE	COMMENT
SSI 32H6811	Serial	6-bit header, 10-bit data
SSI 32H6812	Serial	6-bit header, 10-bit data
SSI 32H6820	Serial	8-bit header, 8-bit data
SSI 32H6520	Parallel	8-bit Intel/Motorola µP
SSI 32H6521	Parallel	8-bit TMS 32C025
SSI 32H4633	Parallel	8-bit Intel/Motorola µP
SSI 32H6830	Register	Internal register file

Data Format

Data format primarily deals with the orientation of the bits within words transferred between the A/D and D/A converters. For all of the Silicon Systems servo devices, the data format is such that all values are left justified. Left justification implies that the most significant bit is on the left while the least significant bit is on the right. Figure 14 illustrates how both 8 and 10-bit values compatible with Silicon Systems D/A and A/D converters are to be formatted.

In the serial links, the data portion of the serial packet matches the D/A and A/D bit width. For the parallel bus interfaces, the bus width is only eight bits wide. For 10-bit wide values, the upper eight bits are accessible in the MSB data register and the least two bits are accessible in the LSB data register. In the SSI 32H6520, the LSB data register is on an even address and the MSB data register is one ascending address higher. In this arrangement, the 10-bit value may be accessed as either two successive 8-bit values or one 16-bit word following the INTEL 80C196 convention.

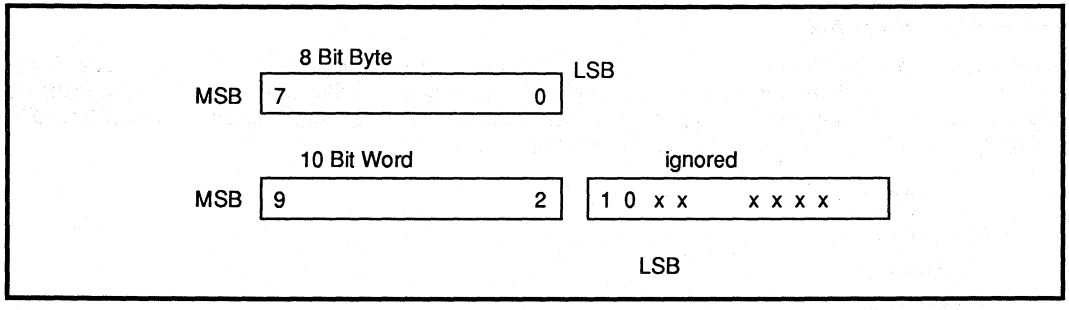


FIGURE 14: Data Format for Left Justified 8 and 10 Bit Values

Microcontroller Interfaces

The microcontroller interfaces supported by the SSI 32H6520 and SSI 32H4633 are both Intel 80C196 and Motorola 68HC11 compatible. The interface is a parallel bus consisting of 8 data lines multiplexed with three or four address lines depending upon the device. A separate control line identified as ALE decodes the register address from register data. Figure 15 illustrates the INTEL interface supported by the SSI 32H6520 and SSI 32H4633.

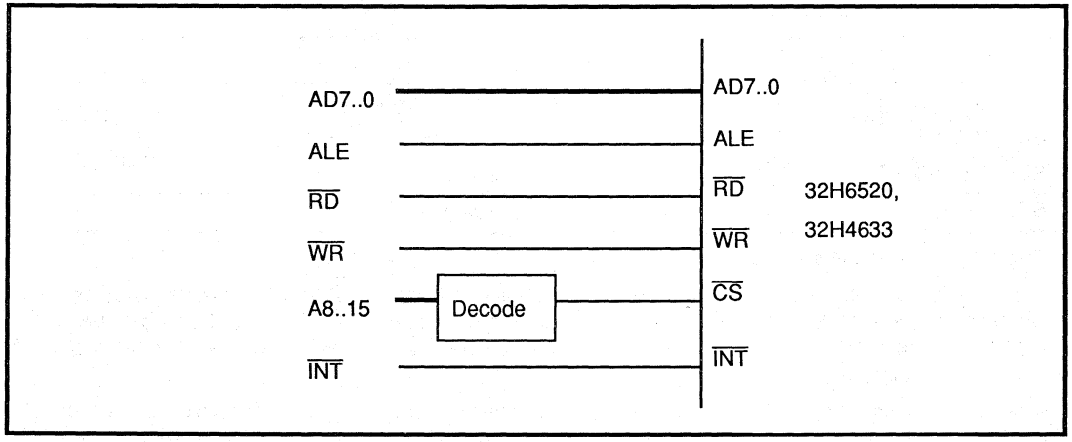


FIGURE 15: Intel Compatible Parallel Bus

DSP Interfaces

Two Silicon Systems servo controllers offer high speed bus interfaces. A high speed interface differs from the microcontroller interface due to transfer speed and demultiplexed implementation. The SSI 32H6520 provides an approximate DSP interface by breaking register transfers down into two successive cycles; the first cycle latches register address, the second cycle transfers register data. The SSI 32H6521 implements directly an 8-bit bus which is directly compatible with a TMS32C025. Figure 16 illustrates the DSP interface between the 32C025 and the SSI 32H6521.

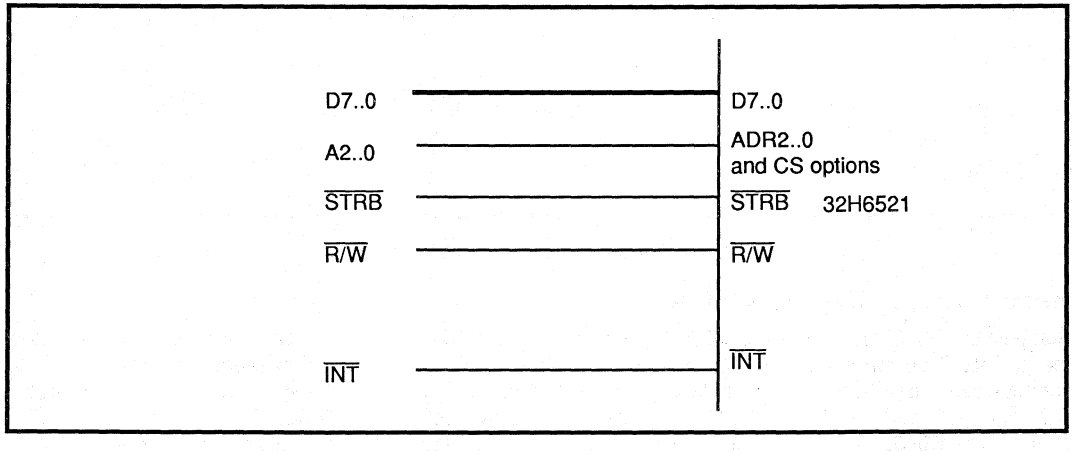


FIGURE 16: TMS 32025 Compatible Bus

DIGITAL INTERFACE (continued)

Interrupts and Status Registers

Extensive interrupt and status information is available in the different Silicon Systems servo controllers. Interrupts can be selectively enabled to notify the microcontroller of an event such as conversion completion. Status registers reflect interrupt assertion and can be polled by the microcontroller as an alternative to using interrupts. The following controllers offer these features:

DEVICE	INTERRUPT	STATUS
SSI 32H6520	$\overline{INT}$	Burst and ADC complete
SSI 32H6521	$\overline{INT}$	Burst and ADC complete
SSI 32H4633	$\overline{INT}$	Extensive MSC and VCM
SSI 32H6830	$\overline{INT}$	Extensive user definable

Using Interrupts and Status with the SSI 32H6520/21

The SSI 32H6520 and SSI 32H6521 implement two bits which reflect status for both A/D conversion and burst integration completion. Register 0 is the status register with bit 0 being BURST INT and bit 1 being ADC INT complete. For the SSI 32H6520, register 0 also serves as an interrupt mask which when written can selectively enable $\overline{INT}$ pin assertion.

Figure 17 shows a timing example of how the status and interrupt pin work together in a typical application. The $\overline{INT}$ pin assertion occurs when either enabled status bit becomes true. Any asserted interrupt event is cleared when the microcontroller reads register 0. If interrupts are not used, register 0 may be polled for completion status.

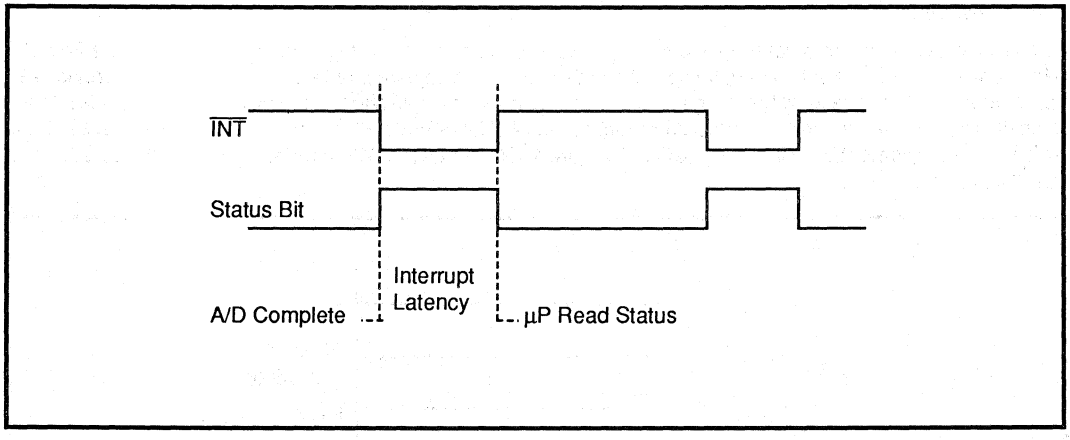


FIGURE 17: Interrupt Cycle in SSI 32H6520/21

Interrupts and Status in the SSI 32H6830

Status in the SSI 32H6830 consists of DSP execution and user definable flags. DSP execution flags indicate to the microcontroller when the DSP is busy or available for access. User definable flags provide a means of communication between the microcontroller and the DSP indicating application specific events such as on-track, seek-complete, and spindle lock. The status of the SSI 32H6830 is enhanced with flags which indicate when states change. The SSI 32H6830 can assert an interrupt to the microcontroller through the status register. Status flags and interrupts are cleared by the microcontroller when the status register FSTATUS is read.

The SSI 32H4633 Status and Interrupt System

The SSI 32H4633 interrupt system is quite extensive. This device offers status and interrupt enabling masks for events from the servo and spindle sections including commutation, speed lock, embedded servo burst capture complete, dedicated servo track crossing, and seek terminal track count. Interrupt status is read from register 0 and MSC interrupts are cleared by reading the spindle status register 1 while servo interrupts are cleared by reading servo status register 2.

VCM MOTOR CURRENT

Sampling VCM motor current is useful for two reasons. First, electrical calibration of the D/A and VCM transconductance power amplifier can be performed. Second, motor current can be used by an observer to estimate head velocity in track and seek algorithms.

SOUT and Offset

In Silicon Systems VCM drivers, motor current is measured by a differential amplifier amplifying the voltage developed across a sense resistor. The sense resistor is placed in series with the VCM motor itself and typically has a very small value such as a few tenths of an Ω. The sense amplifier has a fixed voltage gain typically of 4 and the output appears at the SOUT pin. The voltage at SOUT is fed back to the error summing amplifier to close the loop and set the VCM power amplifier gain (detailed in later sections).

Accurate measurement of VCM motor current is essential and requires minimum sense amplifier offset. The sense amplifiers implemented in Silicon Systems servo drivers are either continuous time in bipolar devices or switched capacitor in CMOS devices. The sense amplifier characteristics for the VCM drivers and predrivers are listed below:

DEVICE	SENSE INPUT OFFSET MAX	SENSE GAIN	COMMENT
SSI 32H569	2 mV	4	continuous time
SSI 32H4633	3 mV	4	switched cap
SSI 32H6230	2 mV	4	continuous time
SSI 32H6231	2 mV	4	continuous time
SSI 32H6240	2 mV	2	continuous time
SSI 32H6510	3 mV	4	switched cap
SSI 32H6810A	3 mV	4	switched cap
SSI 32H6811	3 mV	4	switched cap
SSI 32H6812	3 mV	4	switched cap
SSI 32H6820	3 mV	4	switched cap
SSI 32H6825	2 mV	4	continuous time

Sense Amplifier Gain Variation

In the bipolar predrivers including the SSI 32H569, SSI 32H6230/31, and SSI 32H6240 there is a common mode voltage sensitivity which will result in sense amplifier gain variation. The data sheets specify the sense amplifier gain to be within ±2.5%; however, this measurement is performed only at a specific common mode voltage such as 6V. As the common mode voltage swings from near zero up towards the 12V supply, the sense gain will vary.

VCM MOTOR CURRENT (continued)

Sense Amplifier Gain Variation (continued)

The voltage sensitivity is due to the input resistors making up the sense differential amplifier having a voltage coefficient. The sense gain variation can be viewed in two ways. First, sense gain tolerance will be ± 2.5% about a transfer function which accounts for the voltage coefficient. A second view lumps voltage coefficient and tolerance together for a composite uncertainty of ± 5%. In the SSI 32H569, the composite uncertainty would become 3.8 to 4.2 V/V as compared to 3.9 to 4.1 V/V.

Using Uncommitted Op-Amps

A few Silicon Systems servo controllers offer an uncommitted op-amp. This can be useful in translating or amplifying motor current for greater A/D conversion resolution. The following devices offer such an uncommitted op-amp:

DEVICE	COMMENT
SSI 32H6231	Independent op-amp A3
SSI 32H6825	Independent op-amp A3
SSI 32H6520	Op-amp with output connected as ADCIN1
SSI 32H6521	Op-amp with output connected as ADCIN1
SSI 32H6830	Op-amp with output connected as IN5

The uncommitted op-amps in the SSI 32H6231 and SSI 32H6825 are general purpose op-amps with minimum unity gain bandwidth products of 150 KHz, 60 dB gain, and low input offset of ± 2 mV. The op-amps in the SSI 32H6520, SSI 32H6521, and SSI 32H6830 are better suited to amplification of SOUT since they offer higher minimum unity gain bandwidth of at least 1 MHz.

Figure 18 illustrates an application using A5 in the SSI 32H6830 to amplify SOUT from an SSI 32H6810A VCM driver. In this example, the VCM peak current is assumed to be 0.5 amp and the sense resistor is 0.1Ω. The peak voltage relative to VREF from the SOUT pin will be computed as:

$$V_{SOUT} = 4 \cdot R_S \cdot I_M$$

so that

$$V_{SOUT} = 4 \cdot 0.1 \cdot 0.5$$

Using these example parameters, the peak SOUT voltage will be 200 mV. The A/D conversion range will be 1V peak and therefore, an amplification of four is suggested (leave some conversion margin to avoid saturation).

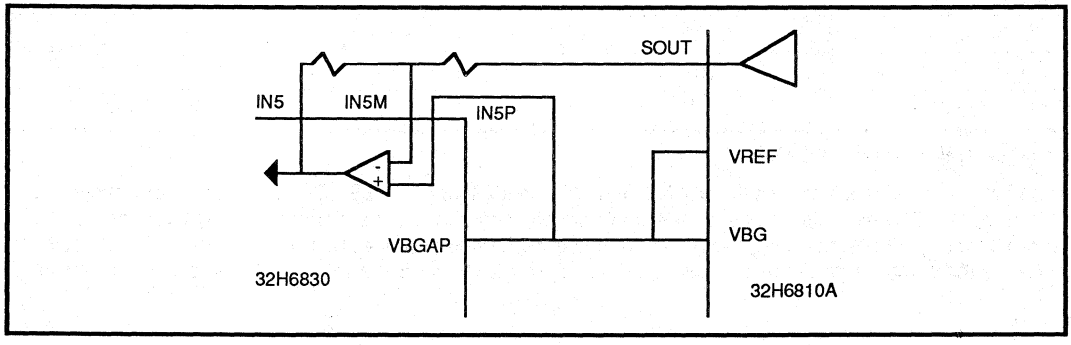


FIGURE 18: Using the Uncommitted Op-Amp to Sense Im

VCM Current Offset Calibration

VCM current offset calibration should usually be performed at power up. The intent of this calibration is to determine what value written to the D/A really corresponds to zero VCM motor current. The offset in the D/A is usually small such as ± 15 mV. Offsets in the VCM error summing amplifier may be tens of millivolts. The sense amplifier will also have an offset as listed earlier. Voltage offsets will translate into VCM current offsets. The accumulative offset can be canceled so that values written to the D/A converter are not biased.

When working to cancel output offset, some point in the measurement chain must be considered accurate. The low offset in Silicon Systems sense amplifiers suggest that the value appearing at SOUT is a good starting point. A calibration routine would program the VCM D/A to near zero current and then measure SOUT through an A/D conversion. A simple routine begins below zero and sequentially ascends higher while sampling at each point. The point where SOUT is closest to zero (of course this assumes the A/D converter offset is already calibrated out) will be the correction value to use when writing the D/A. This correction value should be subtracted from all values written to the D/A converter. If an amplifier is placed between SOUT and the A/D, the offset in this amplifier will degrade the measurement slightly.

Sense Amplifier SYSCLK Dependence

The switched capacitor sense amplifiers rely upon a system clock for timing. Sometimes, it is necessary to supply the device with a SYSCLK frequency which is not that specified in the data sheet. For example, the SSI 32H6810A specifies a nominal clock frequency of 2 MHz and a range of 1.5 to 2.5 MHz. SYSCLK in this device affects the sense amplifier, charge pump, D/A, and the adaptive commutation logic in the MSC block. The SSI 32H6811 data sheet specifies 8 MHz with a tolerance of only ±0.1%. This particular specification is actually misleading because this device likewise can be shifted in frequency over a considerable range (9 MHz is acceptable).

When SYSCLK is shifted from the data sheet value, the device behavior changes. Shifting higher in frequency is better than shifting down. When shifting higher in frequency, the sample rate for SYSCLK dependent circuits likewise is shifted higher. In general, the following effects will be noticed:

FUNCTION	SHIFT LOWER	SHIFT HIGHER
Adaptive commutation range	RPM range lower	RPM range higher
VCM Bandwidth	Reduced	Increased
VCM Slew Rate	Reduced	Increased
DAC settling time	Increased	Reduced

In general, shifts of ± 15% will be insignificant. Larger shifts in frequency should be verified with Silicon Systems.

SERVO DRIVERS

Servo drivers are actually a mix of VCM predrivers and integrated power drivers. The drivers can be characterized as either being a predriver or driver, and being 12 or 5V compatible. Beyond these characteristics, the basic topology of all Silicon Systems servo drivers are essentially the same.

5 AND 12V APPLICATIONS

Silicon Systems 5V and 12V servo applications tend to also divide down into integrated power and predrivers. In fact, all 12V servo drivers are predrivers and all 5V devices include integrated power drivers. The 12V applications will tend to be aimed at high capacity, high performance designs fitting into 3.5" and some 2.5" form factors. The 5V devices are applicable to 2.5" and smaller form factors.

PREDRIVER VERSUS INTEGRATED POWER

The predriver differs from the integrated power driver because the predriver requires external power MOSFETs. Figure 19 illustrates an interconnection between a predriver, external MOSFETs, and VCM motor. Figure 20 illustrates the direct connection made between an integrated power driver and the VCM motor.

The predriver relies on an external H bridge arrangement which consists of pairs of P and N channel MOSFETs. The upper driver is a P channel while the lower is an N channel MOSFET. Four interconnections between the predriver and MOSFETs are required to control the gates. In addition, three interconnections are required to close the legs of the H bridge locally and to differentially sense VCM motor current.

The integrated power driver connects directly to the VCM motor through a single sense resistor. Two differential interconnections are made to the sense resistor to minimize offset induced across any common PCB trace (SE1 and VM1).

Both arrangements rely upon a single error summing amplifier which accepts a VCM command voltage. Feed back is arranged to implement a transconductance gain stage which forces current through the VCM motor in response to the input command voltage. Figure 21 illustrates the basic small signal topology of the Silicon Systems' VCM servo drivers.

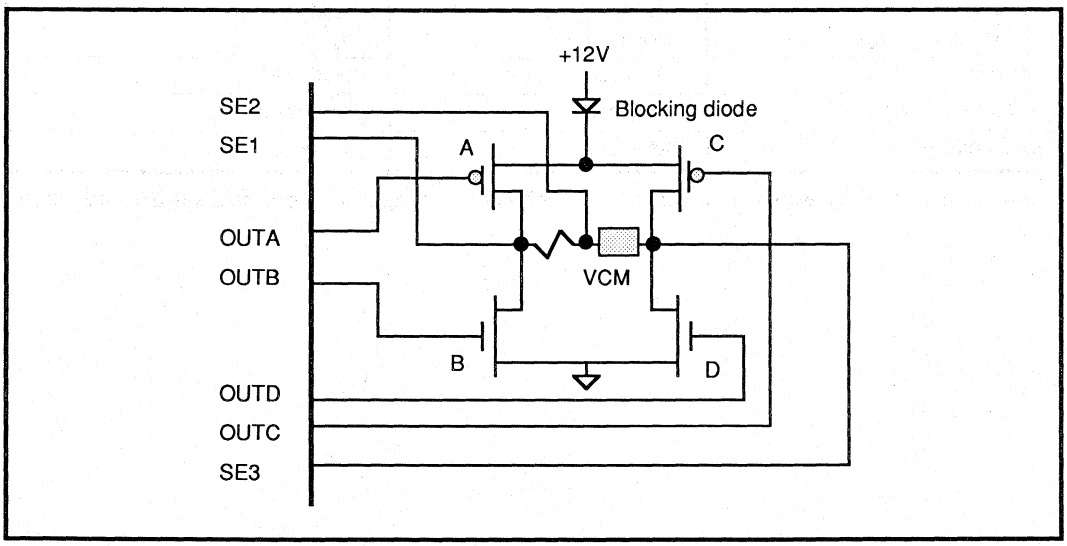


FIGURE 19: Predriver Connection to External MOSFETs

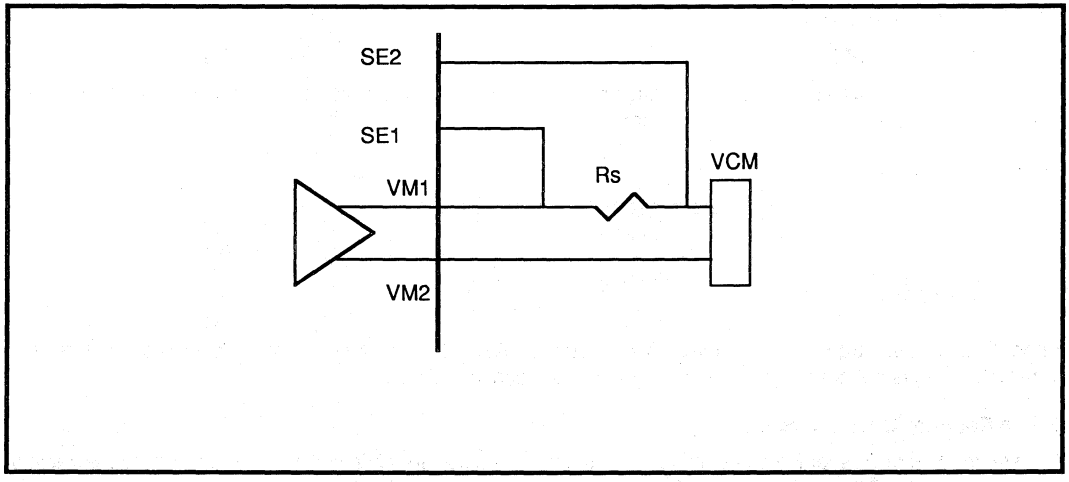


FIGURE 20: Integrated Power Driver VCM Connection

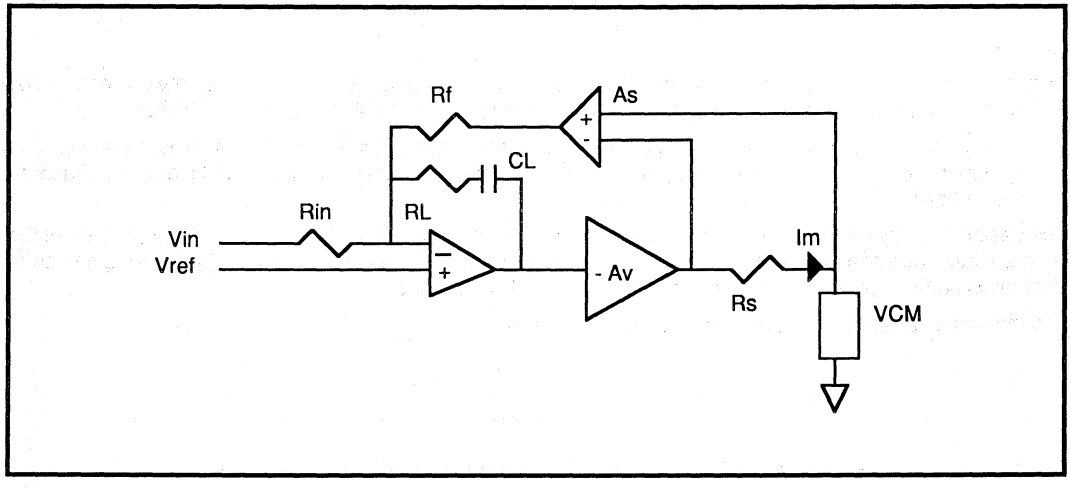


FIGURE 21: Basic Small Signal Topology of Driver

SERVO DRIVERS (continued)

VCM POWER AMPLIFIER

The VCM power amplifier may be implemented with either the Silicon Systems predriver or integrated power driver devices. This section discusses how to design VCM power amplifiers.

Transconductance Gain

The DC transconductance gain is determined by the simple equation:

$$G_{DC} = \frac{1}{R_{IN}} \cdot \frac{R_F}{A_S R_S}$$

where G_{DC} is the DC transconductance gain in amps per volt, R_{IN} is the input resistor, R_F is the feed back resistor from SOUT, A_V is the sense gain, and R_S is the current sense resistor.

Sense Resistor Characteristics

The sense resistor R_s should be chosen to be as small as possible to minimize loss. A lower limit to the value of this sense resistor is typically 0.1Ω and is based on signal to noise ratio. A non-inductive sense resistor is best and the power rating should be sufficient to avoid significant thermal shift in value. For peak currents of 500 mA and 0.5Ωs, an one-half watt rating should be sufficient.

Bandwidth

In the recommended VCM amplifier topology, a single RC network is used to both compensate the power amplifier and set the bandwidth. The following analysis provides the reasoning behind this design approach.

Figure 21 is the basic small signal driver topology. If the BEMF voltage generated when the motor is moving can be neglected, the circuit analysis is greatly simplified. Under these assumptions, the VCM is modeled simply as a series resistor R_m and inductor L_m.

The design objective is to determine values for the compensating components R_L and C_L. Determination of the compensation components requires an analysis of the circuit transfer function. A straight forward approach of analysis is summing the currents in the virtual ground node of the error summing amplifier.

Assuming the current entering the virtual ground node due to V_{IN} is I_{in}:

$$I_{IN} = \frac{V_{IN}}{R_{IN}}$$

and the currents entering the node from compensation and current feedback are I_L and I_F:

$$I_L = \frac{V_O / A_V}{R_L + 1/sC_L} \qquad I_F = \frac{I_M R_S A_S}{R_F}$$

At the virtual ground:

$$\sum I_{IN} + I_F + I_L = 0$$

V_O is the voltage across the sum of the VCM load and sense resistor. The voltage at the ERR pin determines the current through the compensation network. The input referred voltage on ERR will be V_O divided by A_V.

The voltage on SOUT is the A_S amplified voltage developed across the sense resistor R_S due to the current I_M. The sense of polarity between V_{IN} and the VCM voltage V_O is non-inverting. In the physical implementation, the VCM voltage is differential and V_O corresponds to the voltage at either the VM1 pin or A/B driver pair.

Rearranging the summation of currents yields:

$$\frac{V_{IN}}{R_{IN}} = -\left[\frac{V_O/A_V}{R_L + 1/sC_L} + \frac{I_M R_S A_S}{R_F}\right]$$

Substituting for V_O and rearranging for the required transfer function through algebraic gymnastics yields:

$$\frac{I_M}{V_{IN}} = -\frac{1}{R_{IN}} \cdot \frac{R_F A_V \left(R_L + 1/sC_L\right)}{A_V A_S R_S \left(R_L + 1/sC_L\right) + R_F \left(R_S + R_M + sL_M\right)}$$

Rewriting all frequency dependent factors in normalized form results in:

$$\frac{I_M}{V_{IN}} = -\frac{1}{R_{IN}} \cdot \frac{R_F A_V \left(sR_L C_L + 1\right)}{A_V A_S R_S \left(sR_L C_L + 1\right) + sR_L C_L \left(R_S + R_M\right)\left(s\frac{L_M}{R_S + R_M} + 1\right)}$$

To compensate the electrical pole in the denominator above due to the VCM motor, choose R_L and C_L so that the zero in the numerator exactly cancels the motor pole. To accomplish this cancelation, equate the two time constants:

$$R_L C_L = \frac{L_M}{R_S + R_M}$$

When the compensation is chosen so that the zero cancels the VCM motor pole exactly, the transfer function simplifies to:

$$\frac{I_M}{V_{IN}} = -\frac{1}{R_{IN}} \cdot \frac{R_F A_V}{A_V A_S R_S + sR_L C_L \left(R_S + R_M\right)}$$

The compensated transfer function has only one pole and can be rewritten more clearly as:

$$\frac{I_M}{V_{IN}} = -\frac{R_F}{R_{IN} A_S R_S} \cdot \frac{1}{s\frac{R_L C_L \left(R_S + R_M\right)}{A_V A_S R_S} + 1}$$

VCM POWER AMPLIFIER (continued)

Bandwidth (continued)

The closed-loop -3dB frequency will be:

$$BW = \frac{A_V A_S R_S}{R_L C_L (R_S + R_M)}$$

In an application, the required bandwidth is known. C_L can be determined to meet the bandwidth specification. R_L can be found once C_L is determined by making use of the relationship which equates the compensating zero and VCM motor pole time constants. The final component solutions are below:

$$C_L = \frac{A_V A_S R_S}{2\pi \cdot R_F (R_S + R_M) \cdot BW}$$

$$R_L = \frac{L_M}{C_L (R_S + R_M)}$$

In these equations, A_S is the sense amplifier gain and A_V is the differential gain from the output of the error summing amplifier ERR pin to the VCM load. The sense gain for each device type was listed in a prior section, the differential voltage gain A_V is listed below:

DEVICE	A_V	
SSI 32H569	17	
SSI 32H4633	29.4	
SSI 32H6230	17	
SSI 32H6231	17	
SSI 32H6240	17	
SSI 32H6510	12	
SSI 32H6810A	12	
SSI 32H6811	12	
SSI 32H6812	12	
SSI 32H6820	29.4	
SSI 32H6825	17	

External Power Devices

Silicon Systems servo predrivers require external power devices to drive the VCM. The criteria for choosing compatible power devices vary among the predrivers. The table below provides selection criteria:

	CRITERIA	EXAMPLE DEVICE
SSI 32H569	500 -1000pF, Vgs>2V	IRFR020,IRFR9020
SSI 32H4633		Si9952DY
SSI 32H6230	500 -1000 pF, Vgs >2V	IRFR020,IRFR9020
SSI 32H6231	500 -1000 pF, Vgs > 2V	IRFR020,IRFR9020
SSI 32H6240	b > 40, f_t > 40 MHz	BCP68,BCP69
SSI 32H6825		Si9952DY
SSI 32H6820		Si9952DY

The criteria for theSSI 32H569,SSI 32H6230, andSSI 32H6231 are based on two factors. The gate capacitance must be in the specified range because it contributes to the amplifier compensation. The cross-over protection level in these predrivers is fixed at approximately 2V. The MOSFET turn-on threshold Vgs must be greater than the protection level.

Cross Over Adjustment

In the SSI 32H4633 and SSI 32H6820, a means to adjust the cross-over protection threshold is available. The voltage on pin VX sets the cross-over protection level directly. The pin has a default of 1.0 to 1.4V. A resistor may be added to ground to modify the voltage on VX.

Gain Switching

Gain switching is a technique which adjusts the transconductance gain of the VCM driver to match the operating mode. Usually there are track-following and track-seeking hard disk servo modes. The D/A converter voltage range is fixed; therefore, the power amplifier gain can be adjusted to optimize the driver dynamic range for the operating mode.

In Silicon Systems servo drivers, gain switching is implemented by changing the input resistance to the error summing amplifier using an analog switch. In track-following mode, the analog switch is left open. When track-seeking, the analog switch is closed to parallel in the seek input resistor which in turn increases the transconductance gain. The following devices support the gain switching feature:

DEVICE	GAIN SWITCHING CONTROL
SSI 32H4633	SW-ON bit in servo control register
SSI 32H6810A	SWON pin
SSI 32H6811	SWON pin
SSI 32H6820	SWON bit in register 1

RETRACT AND POWER FAULT

In most hard disk drives, the data heads must be moved away from useful data areas when the power fails. This removal is referred to as head "retraction". Retract is implemented within the VCM servo driver and because of its dependency upon power fault detection, all SSI servo drivers include a power fault detector as well. Power fault detection includes comparators sensing the supply voltage, band-gap precision reference, timing circuits, and power fault control signals.

RETRACT METHODS

Head retraction in Silicon Systems servo drivers is implemented in several different ways. Fundamentally, all methods are the same because they rely upon forcing a voltage during power failure across the VCM motor to cause the positioner to move the data head into a landing area.

H Bridge Retraction

Head retraction can be implemented by unbalancing the H bridge driver so that a current will flow through the VCM. The following devices implement this kind of retraction through external power devices of the indicated type:

DEVICE	DRIVER TYPE
SSI 32H569	MOSFET
SSI 32H6230	MOSFET
SSI 32H6231	MOSFET
SSI 32H6240	Bipolar Transistor
SSI 32H6825	MOSFET

H bridge retraction is accomplished by turning on the "A" and "D" drivers while turning off the "B" and "C" drivers. For the devices implementing this retract method, the means triggering retract vary as listed below:

DEVICE	POWER SENSE	VREF	CONTROL
SSI 32H569	LOWV or VCC<9V	VREF<4.3V	EN
SSI 32H6230	LOWV or VCC<9V	VREF<4.3V	EN
SSI 32H6231	VCC<9V	VREF<3.3V	EN
SSI 32H6240	Two comparators		$\overline{\text{RETRACT}}$
SSI 32H6825		VREF<3.3V	$\overline{\text{RETRACT}}$

Velocity Limiting

The retract voltage applied across the VCM is constant and serves to limit head velocity. Head velocity is limited because the voltage across the VCM is sensed by pins SE1 and SE3 and then compared to an internal reference. The "A" predriver output is adjusted so that the feed back voltage across SE1 and SE3 equals this internal reference. When the head moves, the back-electromotive-force (BEMF) generated across the VCM adds to the total voltage developed across the VCM resistance. As the head gains velocity, the BEMF increases and ultimately is limited when the BEMF voltage equals the internal reference and the applied retract current goes to zero. When the head stops against the crash stop, the current is limited to the retract reference divided by the VCM resistance. For example, if the VCM resistance is 16Ω and the reference is approximately 1V, then the current will limit to:

$$I_{MAX} = 1/16$$
$$or\ 62\ mA$$

The tolerance in the internal reference used to establish retract voltage is fairly wide. For all but the SSI 32H6825 this reference is specified as being 0.7 to 1.3V. The SSI 32H6825 has a tighter specification of 0.7 to 1V. There is no way to adjust the retract voltage reference.

Finally, the retract circuit will typically work to a voltage at VCC as low as 3V. Below this point, the voltage across the VCM will rapidly decrease.

An Alternative Retract Scheme

This group of predrivers relies upon a blocking diode to isolate the VCM H bridge from the 12V supply during failure. An alternative retract scheme is shown in figure 22 and offers the advantage of not requiring the VCM blocking diode. Removal of the blocking diode is at the cost of adding two additional enhancement mode retract MOSFETs, some discrete components, and losing velocity limiting during retract.

During power fault, the predriver "A" and "D" outputs will turn on as usual. As the 12V supply drops to zero, the retract current due to the H bridge itself will become insignificant (since there is no blocking diode isolating VCC). However, during fault BRK will become high impedance allowing the gates of the two additional N channel MOSFETs to move upwards to spindle BEMF voltage thereby turning on the retract MOSFETs. A resistor may be necessary to limit current and the diode/resistor is added to insure noise immunity.

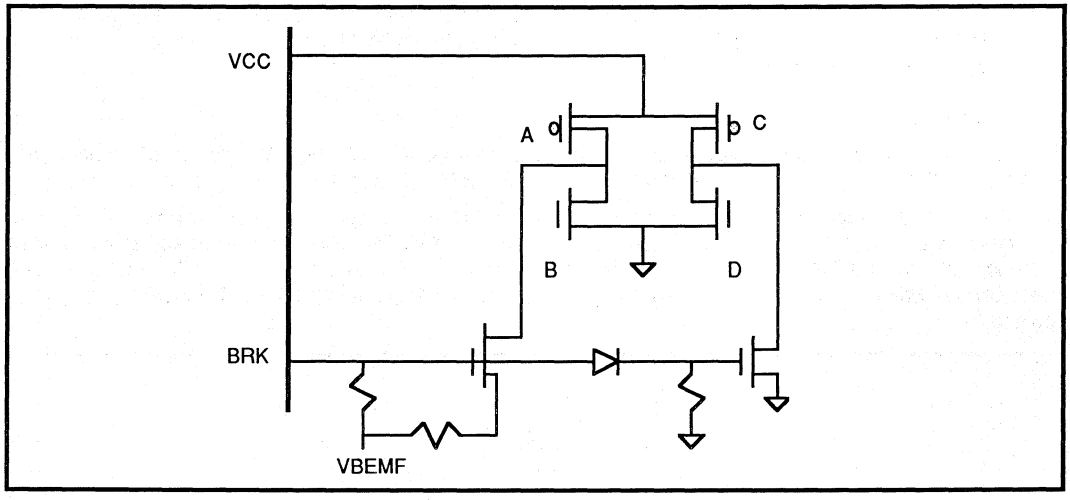


FIGURE 22. Alternative Retract Circuit

Disabling Retract

Some applications implement a mechanical retract or have other reasons to disable the automatic retract function. For this group of predrivers, the circuit shown in figure 23 may be useful. This circuit works by turning on the NPN transistor during power fault so that the gate voltage on the "D" gate driver cannot rise. The resistance in series with the "D" driver gate will introduce some phase shift and so its value must be chosen carefully.

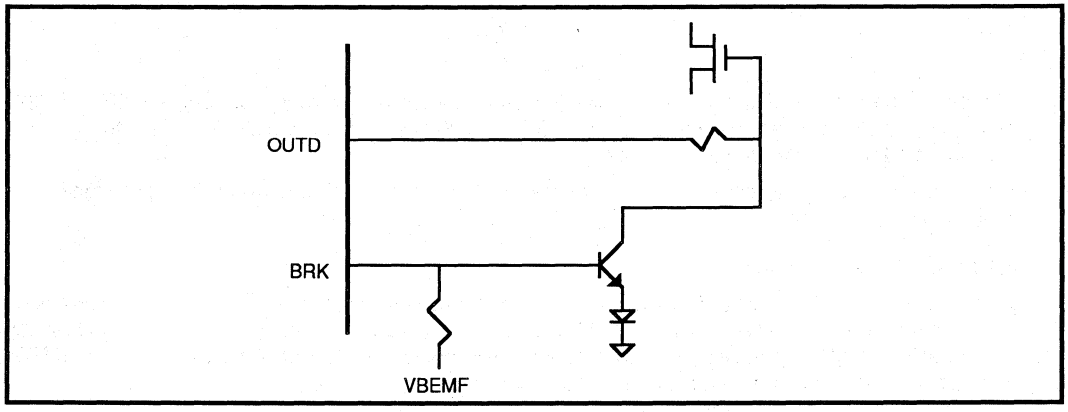


FIGURE 23: Disabling Retract in VCM Predriver

RETRACT METHODS (continued)

BRK Pin pull-up

The SSI 32H569, SSI 32H6230, and SSI 32H6240 all include a special BRK pin which is the collector of an NPN transistor. When retraction occurs, this NPN transistor is turned off thereby allowing the voltage at the collector to rise. Early data sheets indicated that this pin must be pulled high even if it is not used. This is no longer true and this pin may be left floating.

Transistor Retraction

An alternative to H bridge retraction is to source the retract current into the VCM motor through an additional device such as an NPN transistor. The SSI 32H6820 and SSI 32H4633 implement this kind of retraction.

One of the disadvantages of H bridge retraction discussed in the prior section is that the retract level is not adjustable. In the SSI 32H4633 and SSI 32H6820, a pin named VRETR accepts an externally applied retract reference voltage. VRETR has a default high impedance voltage source ranging from 0.3 to 0.9V which can be externally overdriven. Figure 24 shows how transistor retraction is implemented. This circuit will typically work down to 3V.

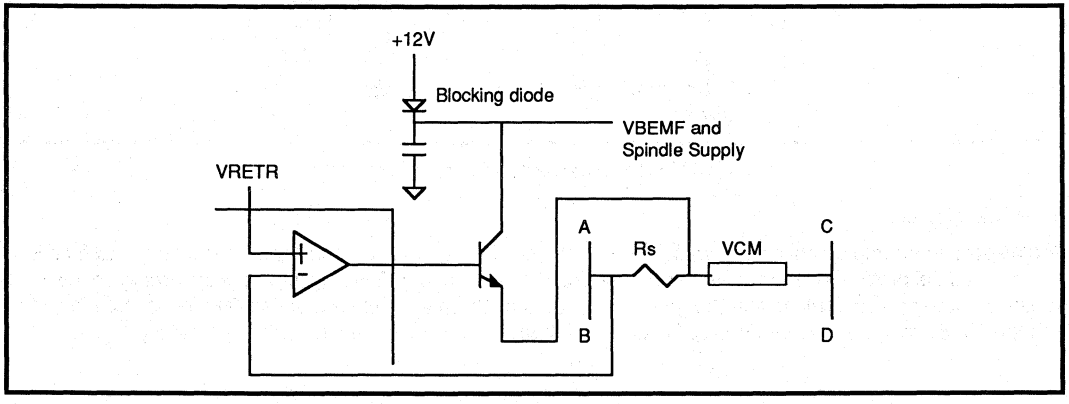


FIGURE 24: Transistor Retract

No diodes are required to protect the NPN transistor from reverse emitter/base breakdown because during normal operation, AOUTR is high impedance. If the retract level is high, the addition of a series resistor between the NPN collector and VBEMF supply is helpful to distribute power dissipation.

Velocity Limiting

The retract voltage applied across the VCM is constant and serves to limit head velocity. Head velocity is limited because the voltage across the VCM is sensed by the SE1 pin and then compared to VRETR. The base current of the NPN is adjusted so that the feed back voltage at SE1 equals VRETR. When the head moves, the back-electromotive-force (BEMF) generated across the VCM adds to the total voltage developed across the VCM resistance. As the head gains velocity, the BEMF increases and ultimately is limited when the BEMF voltage equals VRETR and the applied retract current goes to zero. When the head stops against the crash stop, the current is limited to VRETR divided by the VCM resistance.

Typically, a resistor and diode combination is used to generate the retract reference as shown in figure 25. The resistance is chosen to provide a small current such as a few hundred microamps and the diode serves to provide a fairly constant reference of approximately 0.7V. Other retract levels can be derived from dividers working off the reference diode.

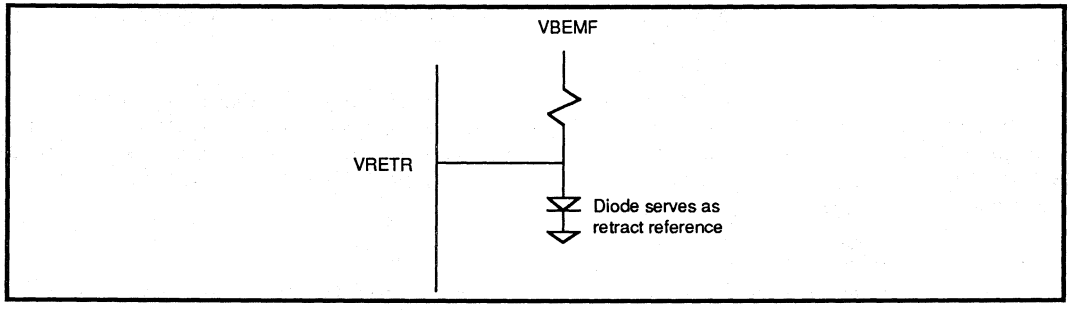


FIGURE 25: Setting Retract Level

Integrated Retraction

All Silicon Systems integrated power servo drivers implement retraction with internally dedicated MOSFETs which are enabled during retract. VM1 is switched to an internal MOSFET as the voltage source and VM2 is saturated towards ground. The following integrated power drivers implement this retract method:

SSI 32H6510

SSI 32H6810

SSI 32H6811

SSI 32H6812

All of these devices implement a programmable retract level. A VRETRACT pin is provided which requires an external voltage which in turn will set the VCM retract voltage. There is no default VRETRACT level in these devices, an external reference must be supplied.

Velocity Limiting

The retract voltage applied across the VCM is constant and serves to limit head velocity. Head velocity is limited because the voltage across the VCM is sensed by the SE2 pin and then compared to VRETRACT. The internal N channel retract MOSFET is controlled by the comparator thereby adjusting the voltage on the VCM through the VM1 pin. When the head moves, the back-electromotive-force (BEMF) generated across the VCM adds to the total voltage developed across the VCM resistance. As the head gains velocity, the BEMF increases and ultimately is

RETRACT METHODS (continued)

Velocity Limiting (continued)

limited when the BEMF voltage equals VRETRACT and the applied retract current goes to zero. When the head stops against the crash stop, the current is limited to VRETRACT divided by the VCM resistance.

Typically, a resistor and diode combination is used to generate the retract reference as shown in figure 25. The resistance is chosen to provide a small current such as a few hundred microamps and the diode serves to provide a fairly constant reference of approximately 0.7V. Other retract levels can be derived from dividers working off the reference diode.

Retract to Brake Transition

Often in hard disk designs, it is necessary to free spin the spindle motor during a retract period and then transition into a spindle braking mode. Free spinning provides the necessary energy to power the retract circuits for a few hundred milliseconds thereby insuring that the head is over a landing area prior to braking the motor. A means to implement this scheme is to use a delay circuit which is triggered by power fault and upon time out, the spindle is placed into a brake mode. Most Silicon Systems sensor-less spindle drivers provide a $\overline{\text{BRAKE}}$ pin for this purpose and the Silicon Systems Sensor-less MSC Applications Note discusses this technique in detail.

Using Spindle BEMF Voltage for Retract

A popular method for powering the retract circuit upon power failure is to full-wave rectify the spindle motor BEMF. For all Silicon Systems predrivers, an external "blocking" diode is required to isolate the 12V supply from the upper P channel MOSFETs during power fault. For Silicon Systems integrated power drivers, the MOSFETs are stacked N channel devices and no "blocking" diode is required. The Silicon Systems Sensor-less MSC Applications Note discusses this subject thoroughly.

POWER FAULT DETECTION

Power fault detection is implemented by the servo drivers in various ways. Many have internal fixed thresholds while others provide comparators accepting a user supplied sample of the supply voltages. The table below lists the types of fault detection implemented and any digital fault signals generated:

DEVICE	FAULT DETECTION METHOD	SIGNAL
SSI 32H569	VCC, LOWV, and VREF qualification	BRK
SSI 32H6230	VCC, LOWV, and VREF qualification	BRK
SSI 32H6231	VCC	
SSI 32H6240	PS1 and PS2 comparators	PFAIL,BRK
SSI 32H6510	VCHK comparator	$\overline{\text{SYSRST}}$
SSI 32H6810A	VCHK comparator	$\overline{\text{SYSRST}}$
SSI 32H6811	VCHK comparator	$\overline{\text{SYSRST}}$
SSI 32H6812	VCHK comparator	$\overline{\text{POR}}$
SSI 32H6820	VCHK1 and VCHK2 comparators	$\overline{\text{SYSRST}}$
SSI 32H6825	Internal reference qualification	
SSI 32H6520	PSV comparator	$\overline{\text{SYSRST}}$
SSI 32H6521	PSV comparator	$\overline{\text{SYSRST}}$
SSI 32H4633	VCHK1 and VCHK2 comparators	$\overline{\text{SYSRST}}$

Power Fault Operation

In some Silicon Systems devices, power fault consists of either retract or linear mode such as the SSI 32H569. Other devices provide digital signals suitable for system wide reset such as the SSI 32H6810A. Figure 26 illustrates the power fault phases in devices like the SSI 32H6810A.

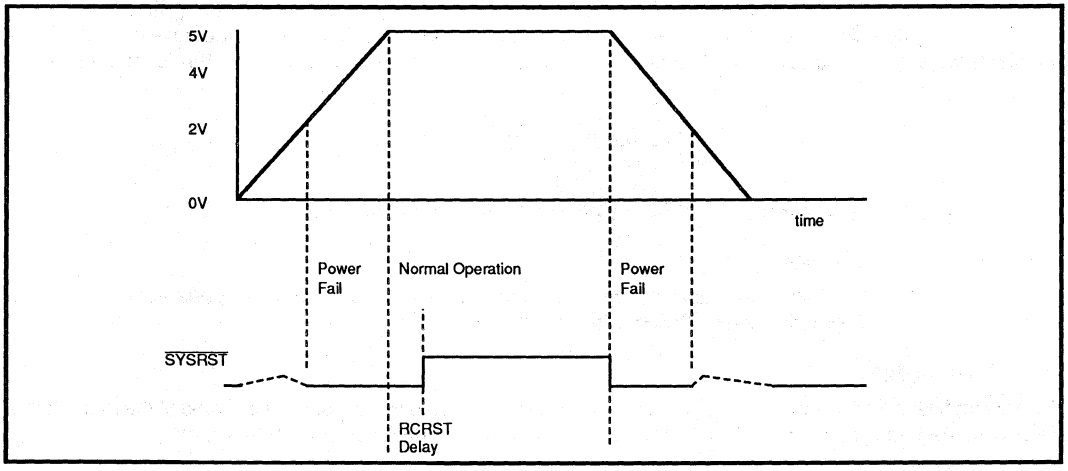


FIGURE 26: Power Fault Phases

Setting the Fault Threshold

Devices which implement a comparator for power fault detection require an external resistor divider to sample the supply voltage. Some devices have two comparators (such as the SSI 32H6240 or SSI 32H6820) so that both the 12 and 5V supplies may be monitored. The threshold voltage should be chosen carefully (particularly not too high and causing false detection) and should consider the various tolerances involved including:

1. Minimum operating supply voltage
2. Tolerance in band-gap reference
3. Tolerance in resistor divider components
4. Ccmparator offset

As a design example, consider a minimum system operating voltage of 4.5V in a SSI 32H6810A application. The band-gap tolerance is ± 3% and ± 1% resistors are to be used. The comparator offset is ± 15 mV and the nominal band-gap reference is 2.25V.

The tolerance in the two divider resistors can be additive. Factoring in the comparator offset, compute the resistor divider to yield 2.25V for a supply voltage 95% of 4.5V less 15 mV. In this example, this supply voltage trip point will be 4.26V and selecting the divider to draw 100 microamps yields values:

$$R_{upper} = \frac{(V_{trip} - 2.25)}{100 \cdot 10^{-6}}$$

$$R_{lower} = \frac{2.25}{100 \cdot 10^{-6}}$$

which yields values of 20.1K and 22.5 kΩ respectively.

POWER FAULT DETECTION (continued)

Adding Hysteresis

Hysteresis may be added to power fault detectors which rely upon a comparator and generate a SYSRST signal. A resistor added between the SSI 32H6810A VCHK pin and SYSRST will add Hysteresis to the comparator threshold. When power is first applied, SYSRST is asserted low thereby setting the power-up threshold. When SYSRST is negated high, the current through the Hysteresis resistor will add to the voltage developed at VCHK effectively lowering the power-down threshold. The Hysteresis is approximately given by the formula below:

$$V_{hysteresis} = \frac{R_{lower}}{R_{lower} + R_{hysteresis}} \cdot 5$$

If R_{lower} is 22.5 kΩ, approximately 100 mV of Hysteresis is introduced with a $R_{Hysteresis}$ of 1 MΩ.

Minimum Operating Voltage

Power fault detectors require a minimum voltage for successful operation. All devices generating a SYSRST power fault signal will correctly assert SYSRST low down to 2V.

Fault Signal Usage

The type and usage of the power fault signal will depend greatly upon how it is generated. Some of the fault signals are conditioned and compatible with microcontrollers for system wide reset while others aren't.

PFAIL and BRK

PFAIL and BRK are the collectors of NPN transistors. An external pull-up resistor is required and this pull-up is typically connected to VBEMF (the rectified spindle BEMF voltage). Typically, the minimum resistance will be 10 kΩ and use of these signals will be limited to analog circuits including switching external MOSFETs during retract. No Silicon Systems spindle drivers can accept this BRK signal to initiate braking. In the SSI 32H6240, PFAIL is available which separately reflects the power fault state while BRK also responds to the $\overline{\text{RETRACT}}$ pin.

The $\overline{\text{SYSRST}}$ Pin

$\overline{\text{SYSRST}}$ is designed to be suitable for system wide reset. In all devices supporting this fault signal, an external RC network provides conditioning which can assure minimum assertion time. Figure 27 illustrates the typical circuit found in the SSI 32H6810A. The following is a design example which will condition the $\overline{\text{SYSRST}}$ assertion so that it has a minimum pulse width of approximately 10 µS.

The RCRST threshold varies from 0.8 to 2V in the SSI 32H6820. The resistor will charge the capacitor towards 5V. The voltage on RCRST will follow the basic relationship:

$$V_{rcrst} = 5\left(1 - e^{t/rc}\right)$$

so that solving for the relationship between delay time "t" and RC when the threshold is chosen to be 0.8 yields:

$$RC = \frac{-1}{ln\left(\frac{5 - V_{rcrst}}{5}\right)}$$

or approximately:

$$RC = 5.7 \cdot t$$

With R of 47 kΩ, C is found to be approximately 1 µFd.

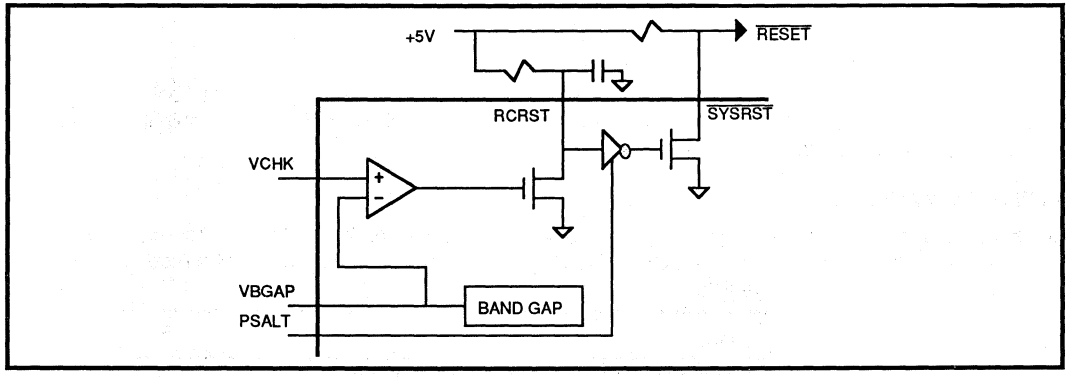


FIGURE 27. Power Fault Detector

$\overline{\text{POR}}$

In the SSI 32H6812, the device pin count has been greatly minimized. The $\overline{\text{POR}}$ pin itself shares the job of signaling power fault and conditioning. This signal will usually not be directly compatible with the microcontroller due to the slow rise time (when capacitance is added) and requires intermediate buffering. Routing $\overline{\text{POR}}$ through some form of non- inverting TTL buffer will do the job.

Capacitance may be added to $\overline{\text{POR}}$. The threshold is approximately 400 mV so an approximate RC time constant for a desired "t" can be computed from:

$$RC = 12 \cdot t$$

SLEEP MODES

Sleep modes provide a means to reduce power consumption when functions such as servo are not needed. The table below lists how each Silicon Systems servo device supports sleep modes:

DEVICE	SLEEP MODE	EFFECT
SSI 32H569	none	
SSI 32H6230	DISABLE	VCM
SSI 32H6231	none	
SSI 32H6240	DISABLE	VCM
SSI 32H6510	SLEEP	VCM
SSI 32H6810A	SLEEP	VCM and MSC
SSI 32H6811	SLEEP	VCM and MSC
SSI 32H6812	SLEEP,STANDBY,SHOCKSLP	VCM or MSC or SHOCK
SSI 32H6820	SLEEP,HEN,MEN	VCM or MSC
SSI 32H6825	$\overline{\text{DISPWR}}$	MSC only
SSI 32H6520	SLEEP	Entire Device
SSI 32H6521	SLEEP	Entire Device
SSI 32H4633	HENABLE,MENABLE,PWRDN	VCM or MSC or Device

RETRACT AND POWER FAULT (continued)

SLEEP MODES (continued)

Dual function devices like the SSI 32H6810A and SSI 32H6811 respond to sleep by turning off both the servo and spindle sections. Selective sleep modes are offered in others which allow servo/MSC combination devices to power down servo while maintaining spindle operation.

Multiple Power Down Modes

Servo/MSC combination devices which offer selective sleep modes such as the SSI 32H6812 can support multiple power down modes. As an example, the SSI 32H6812 supports the following power down modes selected by programming bits in the control register:

MODE	CONDITION
SHOCK	Independently power down shock detector
SLEEP	Both VCM and MSC float, power fault active
STANDBY	VCM float, MSC active
RUN	Both VCM and MSC active

VCM LIMITING

VCM limiting are techniques used to insure that the data head is controlled in a non-hazardous way.

VELOCITY LIMIT

Linear mode velocity limiting is supported in the SSI 32H569 only. Velocity limiting during retract is discussed in the Retract and Power Fault section. Velocity limiting is performed by integrating motor current from SOUT and comparing the result against a window. When the integrator exceeds the window, then the driver is turned off. When the driver is off, the integrator discharges and ultimately will return back into the window where the driver is enabled once more. This behavior may oscillate between enabled and disabled with a period determined by the velocity integrator gain.

In general, the servo system should never lose control of the head but if it does happen, velocity limiting can provide a means to insure that the head velocity is within the crash stop rating. Formulas and constraints for computing the necessary components are found in the SSI 32H569 data sheet.

CURRENT LIMIT

VCM current limiting is a common technique which may be implemented for different reasons and in different ways. Limiting the output current may serve to protect the head from achieving dangerous velocities. Limiting the command current allows higher power amplifier gain while maintaining a limit on peak current. Generating a write protect warning is useful in detecting conditions where a large servo error has been encountered and it is possible that any pending write operation may miss track center.

Limiting the Output Current

Only the SSI 32H569 implements output current limiting. The motor current at SOUT is compared against a window. If the current exceeds the window, the driver is disabled. When disabled, the current will decay and once again current will be within the comparison window so that the driver re-enabled. This behavior will oscillate while the excessive command current conditions exist.

Limiting the Command Current

In a transconductance amplifier, a voltage is applied as input and a current is forced through the load. The input voltage commands an output current through the load. If a limiter is placed between the command voltage and the error summing amplifier within the transconductance amplifier, then the output current will saturate when the input exceeds the limiter.

The SSI 32H6230 implements a limiting circuit. Figure 28 illustrates how the limiter is connected. The limiter voltage is a CLAMP of fixed voltage. The resistors RIN1 and RIN2 determine where the CLAMP will be in effect. The formula below computes the input command voltage (relative to VREF) at which the limiter will be active:

$$V_{limit} = \frac{R_{IN1} + R_{IN2}}{R_{IN1}} \bullet CLAMP$$

When the absolute value of the input command voltage exceeds V_{limit}, the output current will be limited to whatever V_{limit} commands. Note that in the computation of amplifier gain, RIN is the sum of RIN1 and RIN2.

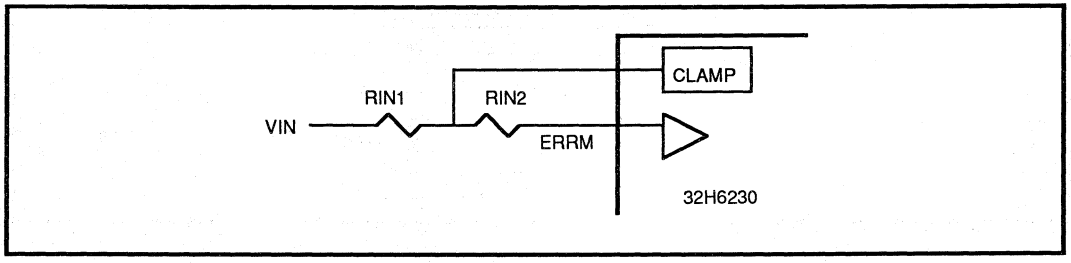


FIGURE 28: Limiting Command Current

Write Protect Warning

Write protect warning is implemented by comparing motor current at SOUT against a window. When motor current exceeds the limits of the window, a digital output signal named $\overline{\text{WRPROT}}$ is asserted. The intent of $\overline{\text{WRPROT}}$ is to stop any write operations in progress often by negating the WR line to the write amplifier and stopping the sequencer in the data formatter. Write protect is implemented in the SSI 32H6231 and SSI 32H6825. In both parts, the window is adjustable and can be defeated.

SHOCK DETECTION

The SSI 32H6812 offers a shock detection feature useful in disabling writes to the disk when the drive is mechanically shocked in plane with the head positioner motion. Two shock detectors are orthogonally mounted on the drive electronics PCB. When a mechanical shock occurs, a small voltage pulse appears across the piezoelectric crystal within the detector and the signal is amplified by the electronics within the SSI 32H6812. The amplified signal is applied to full wave rectifiers which merge both X and Y components together into a composite signal. A low pass filter smoothes the shock signal and a comparison is made to a preset threshold. When the shock signal exceeds the threshold, a digital signal is generated which can be routed to logic which will disable any active write operation and signal the microcontroller.

SHOCK DETECTORS

A representative shock sensor is manufactured by TDK. Figure 29 outlines the device mechanically. This particular device generates approximately 1.6 mV per unit gravity or G. Its capacitance is roughly 350 pF and only two of the four surface mount pads are active.

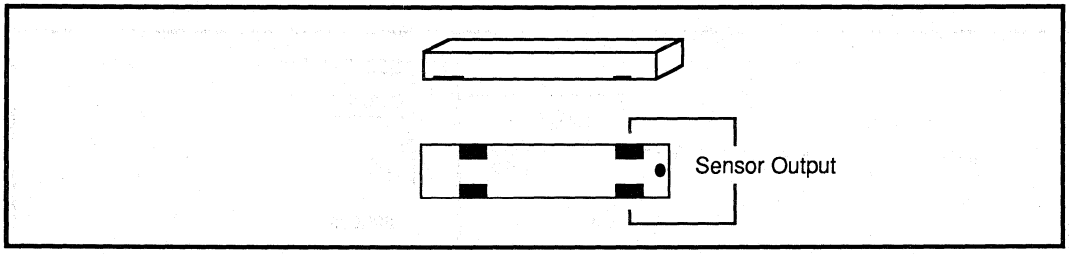


FIGURE 29: Shock Sensor

SHOCK DETECTOR CIRCUIT TOPOLOGY

Figure 30 shows the basic topology for the shock detector electronics.

As illustrated, the piezoelectric shock signal is amplified by 40, full-wave rectified, filtered, then compared. Neglecting the effect of the full-wave rectifier and writing a transfer function for the remaining amplifier and filter blocks yields:

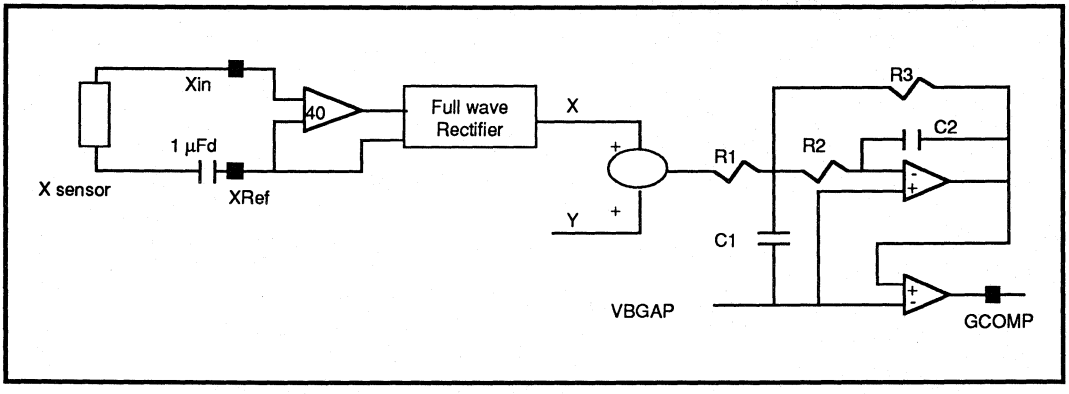


FIGURE 30: Shock Detector Topology

$$H(s) = \frac{1}{R_t} \cdot \frac{40}{s^2 C_1 C_2 R_2 + s\left(C_2 + C_2 \frac{R_2}{R_3} + C_2 \frac{R_2}{R_1}\right) + \frac{1}{R_3}}$$

As a design example, the corner frequency was chosen to be 10 KHz. Choosing the following components:

R_1=10 kΩ, R2=7.9 kΩ, R_3=37 kΩ and C_1=2300 pF, C_2=250 pF

yields the bode plot in figure 31 below:

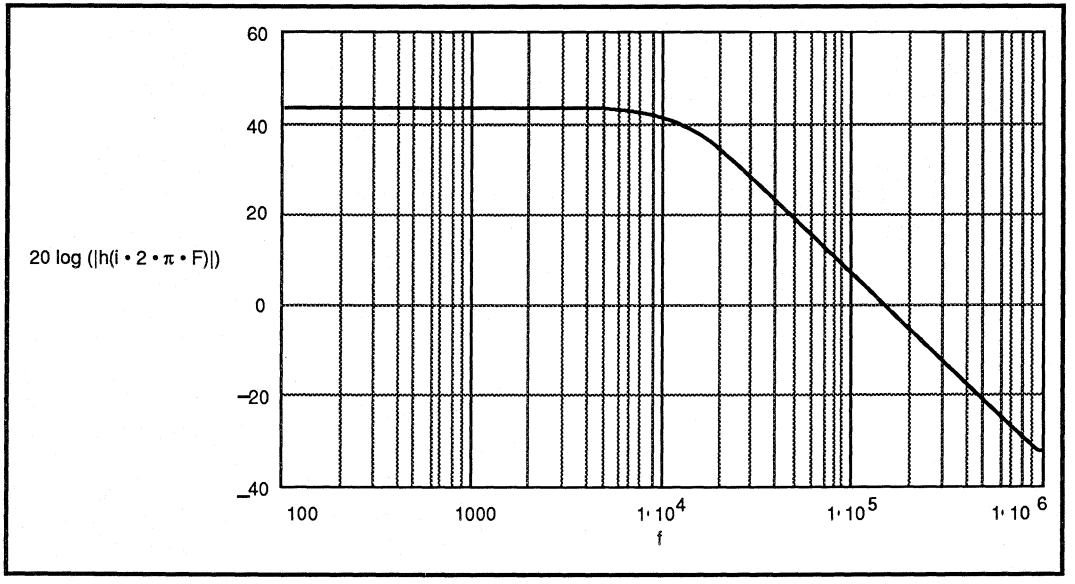
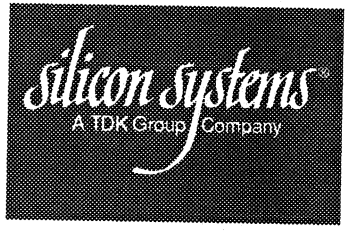


FIGURE 31: shock Sensor filter Response

The DC gain 's approximately 150 and the detection threshold is VBG/2 or 1.125V. This threshold will be crossed when the shock detector amplitude exceeds seven millivolts or approximately four G. The detection sensitivity is adjusted by changing the discrete components configuring the filter.

Notes:

Sensorless Motor Speed Control Application Note



Sensorless Motor Speed Control

INTRODUCTION

Silicon Systems offers a wide range in hall-sensorless motor speed controllers. This application note is a comprehensive MSC design guide explaining how the MSC family members are different and how to apply them successfully. The range of MSC components includes those with and without integrated power drivers or on-chip speed regulation. The Silicon Systems products discussed in this note are the following:

DEVICE	DRIVE TYPE	SPEED CONTROL
SSI 32M595	predriver	yes
SSI 32M7010	integrated	yes
SSI 32M7011	integrated	no
SSI 32H6810A	integrated	no
SSI 32H6811	integrated	no
SSI 32H6812	integrated	yes
SSI 32H6820	predriver	yes

MOTOR SPEED CONTROLLERS

Silicon Systems' motor speed control or MSC circuits are responsible for commutating DC brushless, three phase motors. In a hard-disk drive, the motor controlled is the spindle motor which is responsible for rotating the platters at a fixed and precise speed. The MSC circuit commutates the motor drivers, regulates speed, and drives current through the motor windings.

Motor commutation is the act of driving current through the motor windings in such a way as to sustain a desired rotational direction. Commutation traditionally has been implemented by placing some kind of sensor on the motor shaft. Hall effect sensors are an ideal device to place in the motor to sense absolute rotor position. For a three phase motor, three Hall sensors may be used to directly decode the next motor commutation state. Hall sensors offer a closed-loop method of absolutely determining the rotor position and to properly commutate the motor under all speed conditions. Hall sensors burden the motor design, particularly small motor design, with the need to place the sensors in the motor and the extra wires for the Hall bias and output. The SSI 32M593 and SSI 32M594 are examples of Hall sensor MSC circuits capable of driving external Power MOSFETs at 12V.

An alternative to Hall effect sensors is to electronically detect the rotor position by examining the back-electromotive-force or BEMF generated by a rotating motor. This Hall-sensorless method eliminates the need for Hall sensors to be mounted in the motor and simplifies the motor wiring. For a DELTA type motor, only the three wires for motor terminals A, B, and C connect the motor to the MSC circuit; no additional wires are required as there would be if Hall sensors were used.

The Hall sensorless technique is not as robust compared to a design using Hall sensors. Since BEMF is detected for commutation, there is a lower limit to motor speed. This lower limit is very significant particularly when starting the motor. An open-loop startup algorithm steps the motor in a manner similar to stepper motors. This stepping or ramping of the motor continues for several revolutions until the motor reaches a minimum speed necessary for reliable BEMF generation. Once the minimum speed is reached, a transition is made to sense the BEMF and the motor then operates much like a Hall sensor motor. Figure 1 graphically illustrates an open-loop startup algorithm.

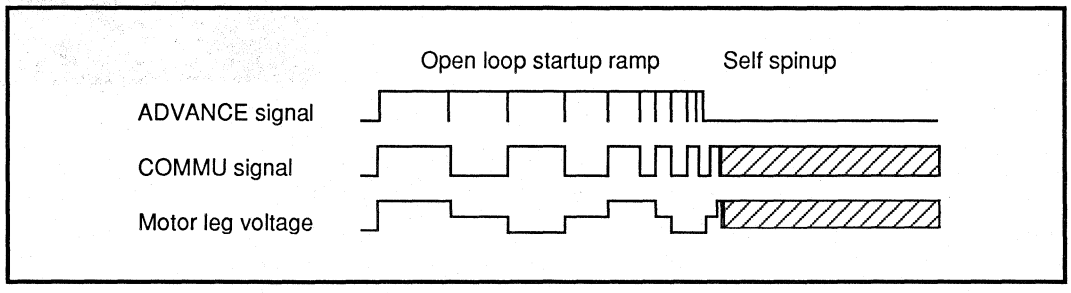


Figure 1. Open Loop Startup Waveforms

5 AND 12 VOLT

The components discussed in this MSC family application note includes those intended for a 12V or 5V motor drive. The 12V compatible components are all predrivers. The 5V components are a mix of predrivers and integrated drivers. The 5V predrivers are actually components capable of operating at either 5V or 12V such as the SSI 32M595. Examples of 5V integrated drivers include devices like the SSI 32M7010 and SSI 32H6810A.

PREDRIVER VERSUS INTEGRATED POWER

A predriver MSC circuit requires external power MOSFETs. These power MOSFETs directly connect to the motor and deliver current typically in the ampere range. The predriver translates the commutation state and motor current command into signal levels which are connected directly to the gates of the external power MOSFETs. There are three pairs of control signals, each pair consists of one signal intended for a lower N channel and one for an upper P channel MOSFET. The signal names for motor terminal "A" MOSFET drivers are OUTA (the lower N channel driver gate) and OUTUPA (the upper P channel driver gate).

An integrated MSC circuit includes power MOSFETs within its package. Such a device has three pins identified as A, B, and C which in turn directly connect to the motor. The integrated power devices from Silicon Systems use a stacked N channel arrangement which eliminates the need for a blocking diode when implementing retract upon power failure (see a later section on blocking diodes).

CONTROL METHODS

There are two major control methods used to implement speed control in MSC circuits. These two are pulse amplitude modulation PAM and pulse width modulation PWM. Most Silicon Systems MSC components implement PAM while one supports both methods.

Pulse Amplitude Modulation (Linear Control)

Pulse amplitude modulation is really a linear control scheme updated at a regular rate. In this method, an error voltage is applied to a transconductance amplifier which sets the motor current. This is a linear control scheme because the transconductance amplifier attempts to close the loop by forcing motor current to satisfy the command current (actually a voltage) presented at the VIN pin of the MSC component. As the motor is commutated, the transconductance amplifier is internally switched from motor terminal to motor terminal. Only one motor terminal at a time is controlled and the particular terminal controlled is the lower one which sinks current. The motor terminal current sourced from the upper power driver is operated in a switched mode.

Digital speed control functions found in devices such as the SSI 32M595, SSI 32H6812, SSI 32M7010, and SSI 32H6820 are intended to update the speed error once per revolution. The speed error resembles a pulse of duration equal to the motor revolution period with an amplitude determined from a proportional-integral compensator.

Linear control is often preferred to PWM because in smaller hard-disk drives, the switching noise of PWM is easily coupled into the read channel electronics. Linear control is a disadvantage for applications requiring high currents, particularly when starting since the MOSFETs will dissipate significant power while limiting the start current.

Pulse Width Modulation

Pulse width modulation is implemented in the SSI 32H6811. In the SSI 32H6811, "switch-mode operation" is enabled and configured by writing to the mode register (address 10). Bits M and N setup the switching duty cycle so that the motor start current can be controlled. Switch mode is intended to provide an alternative way of starting the motor, this particular method avoids operating the lower MOSFETs in linear mode. In switched mode, the commutation delay method is fixed in one shot mode.

For the SSI 32H6811 , switched mode is used for starting and a transition to PAM is made once the motor reaches some minimum speed. In general, PWM or switched mode makes the least power dissipation demands on the power MOSFETs.

CHOOSING COMPONENTS AND SIGNALS

This section presents detailed design information for choosing the external components and signals which must be connected to Silicon Systems' MSC components.

Transconductance Power Amplifier Gain

All Silicon Systems MSC components implement a linear transconductance power amplifier which accepts a command current (in the form of a voltage) and attempts to force a current through the motor. The pin which receives the current command is named VIN on all parts except the SSI 32H6812. For all components, motor current is sampled across a sense resistor which connects all three lower N channel MOSFET sources to ground. This sampled motor current is amplified by a sense amplifier and then compared to the command input at VIN. This is a closed transconductance loop which translates the command (in voltage) to an output current through the motor. Figure 2 illustrates how the transconductance amplifier is configured.

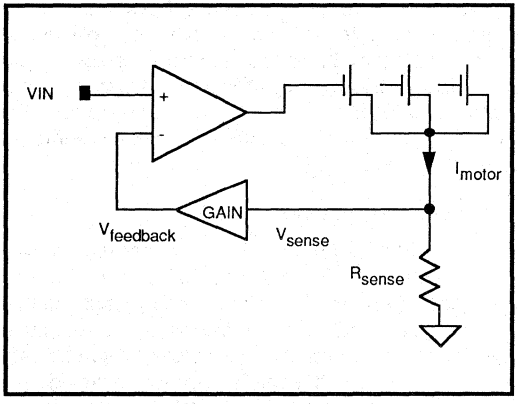


Figure 2. Transconductance Amplifier Configuration

The sense amplifier gain varies across the MSC components as indicated in the table below:

DEVICE	SENSE GAIN	PROGRAM METHOD
SSI 32M595	4	Fixed
SSI 32M7010	4/8	4 at startup, 8 in linear control mode
SSI 32M7011	4	Fixed
SSI 32H6810A	5 or 10	Pin strap
SSI 32H6812	5,10,20,30	Register
SSI 32H6811	5,10,20,30	Register
SSI 32H6820	5,10,15,20	Register

The design equations for the power amplifier gain are derived from the following relationships:

$$V_{SENSE} = I_{SENSE} \cdot R_{SENSE}$$

$$V_{FEEDBACK} = I_{SENSE} \cdot R_{SENSE}$$

The transconductance loop attempts to force the feedback voltage Vfeedback to equal the command voltage at the VIN pin. When this condition is satisfied, the amplifier is operating linearly, otherwise the amplifier is saturated. For linear operation:

$$VIN = V_{FEEDBACK} = I_{MOTOR} \cdot R_{SENSE} \cdot GAIN_{SENSE}$$

so solving for the transfer function:

$$K_a = \frac{I_{MOTOR}}{VIN} = \frac{1}{R_{SENSE} \cdot GAIN_{SENSE}}$$

where Ka is the spindle amplifier transconductance gain.

Choosing the Sense Resistor and Sense Gain

When starting the motor, the maximum value of VIN voltage should be applied which will result in a limiting peak start current. Since run current is usually much smaller than start current, trade-offs between VIN voltage, sense resistance, and sense amplifier gain may be necessary. Ideally, the amplified sense voltage Vsense should be around 0.75V so when possible, a fixed sense resistor and programmable sense gain should be employed.

The design approach for choosing the sense resistor is to first calculate Rsense to satisfy the start current requirement knowing that the input voltage at VIN (see the following section for parts with internal speed control) ranges from zero to approximately 2.5V:

$$R_{SENSE} = \frac{2.5}{I_{START} \cdot Gain_{SENSE}}$$

where $GAIN_{SENSE}$ is the smallest value available such as 5 for the SSI 32H6810A and I_{START} is the target start current. As a design example, consider a target 1A start current in a SSI 32H6810A application:

$$R_{SENSE} = \frac{2.5}{i \cdot 5} = 0.5\Omega$$

If the run current for the particular motor above drops to 150 mA, the higher sense gain of 10 should be employed to increase the amplitude of V_{SENSE} as indicated below:

IMOTOR	GAIN	VSENSE
0.15A	5	0.375V
0.15A	10	0.75V

Programmable gain offers a way of adjusting V_{SENSE} to a sufficient amplitude which maximizes the signal-to-noise ratio and generally improves the transconductance amplifier transient response. Components such as the SSI 32H6811 offer even higher sense amplifier gains.

Startup Current in Devices with Speed Control

Silicon Systems components with speed control generate the start current command internally. Instead of using the VIN pin, an internal reference voltage is selected. The table below lists what this reference is and how it is selected:

DEVICE	METHOD
SSI 32H6812	VCM DAC redirected to LF pin
SSI 32H6820	VLIM pin when more than 3% slow
SSI 32M595	2.25V when more than 3% slow
SSI 32M7010	2.25V when more than 3% slow

For the SSI 32M595 and SSI 32M7010, the start current command voltage is fixed at 2.25V. For the SSI 32H6820, the VLIM pin voltage provides a programmable start current command. In the SSI 32H6820, VLIM can be tied to the band-gap reference for simplicity. For all three parts, when the motor is faster than 3% slow, then the VIN pin is selected for motor current commands.

The SSI 32H6812 differs from the other three because a second order discrete filter is used to compensate the motor. In the SSI 32H6812, the voltage across this filter at the LF pin is directly connected to the transconductance amplifier. For starting and initialization, the VCM positioner DAC can be redirected to force the LF pin voltage. This redirection is accomplished by setting the MSCDAC bit in the MSC_MODE register.

Target Speed, Motor Poles, and SYSCLK Frequency

All Silicon Systems MSC components provide some means for indicating motor speed. Some of these devices include an internal speed control function which relies on the speed indication. The speed of the motor is determined by the number of poles in the rotor. The number of commutations a three phase motor experiences per revolution is determined by the number of rotor/stator alignments computed below:

$$Coms_{REV} = 3 \cdot N_{POLES}$$

yielding for typical pole counts:

12 for 4 pole motor,

24 for 8 pole motor, and

36 for 12 pole motor.

This $Coms_{rev}$ relationship results since each motor pole aligns once with each stator winding per revolution.

Silicon Systems MSC components determine one revolution by counting the number of commutations; the speed indicated is the time taken for one revolution to occur. The following table indicates how each component indicates motor speed:

Target Speed, Motor Poles, and SYSCLK Frequency (continued)

DEVICE	METHOD	COMMENT
SSI 32M595	8 poles assumed	Change in metal mask
SSI 32M7010	8 poles assumed	Change in metal mask
SSI 32M7011	REVCLK every 12 commutations	Externally divided for more than 4-pole applications
SSI 32H6810A	REVCLK every 12 commutations	Externally divided for more than 4-pole applications
SSI 32H6811	REV every 12 commutations	Externally divided for more than 4-pole applications
SSI 32H6812	REV every 24 or 36 commutations	8- or 12-pole motor selection
SSI 32H6820	4,8,12,16 poles	Register programmable

Devices such as the SSI 32M595 and SSI 32M7010 are fixed in the number of poles assumed; therefore, operation with motors having other than eight poles is best handled with a metal mask option. When using the either the SSI 32M595 or SSI 32M7010 (as is with eight poles assumed) with a four pole motor, two mechanical revolutions occur for every one revolution electrically detected. For a twelve pole motor, every 2/3 mechanical revolution results in the 24 commutations necessary to indicate a revolution.

For devices like the SSI 32M595 and SSI 32M7010, speed control of motors having other than eight poles is still possible. As an example, assume a four pole motor is to be controlled at 3600 RPM. Instead of supplying a 2 MHz SYSCLK to the component, supply it with a 1 MHz clock. This correction works because two mechanical revolutions of 3600 RPM will occur in 1/30th of a second, and cutting SYSCLK to one-half shifts the period timer to count down from 8333 in 1/30th of a second (instead of 1/60th). The sample rate is now 30 Hz instead of 60 Hz and the resolution is 4 µs instead of 2 µs, but for most applications this is still much higher than the control open-loop bandwidth. Twelve pole emulation is not as successful because the samples are not always based on the same commutation edge. This ping-pong sampling in 12 pole motor may introduce a small degree of speed measurement uncertainty.

Devices having internal speed control measure the period of one revolution with SYSCLK. The frequency of SYSCLK varies for the devices listed below, but internally the clock is divided by the same factors with a count resolution of 2 µs. The frequency of SYSCLK is based on a 3600 RPM target speed and is used as follows:

DEVICE	SYSCLK	SYSCLK USAGE
SSI 32M595	2 MHz	Speed control reference
SSI 32M7010	2 MHz	Speed control reference and adaptive commutation
SSI 32M7011	2 MHz	Used only for adaptive commutation circuit
SSI 32H6810A	2 MHz	Used for VCM sense and adaptive commutation
SSI 32H6811	8 MHz	Clock used by DACs, VCM sense, and adaptive commutation
SSI 32H6812	1 MHz	Speed control reference, VCM sense, and adaptive commutation
SSI 32H6820	4 MHz	Used for programmable speed control counters, VCM sense amplifier, and DAC

The devices having built-in speed control are the SSI 32M595, SSI 32M7010, SSI 32H6812, and SSI 32H6820. The SSI 32H6820 target speed is programmable by setting a revolution period value into registers. The SSI 32M595 and SSI 32M7010 may operate at other target speeds by scaling the SYSCLK frequency. This scaling is a simple linear relationship as follows:

$$F_{SYSCLK} = \frac{TARGET_{RPM}}{3600} (2\ MHz)$$

For example, an 8-pole motor operating at 5400 RPM with a SSI 32M595 would require a SYSCLK frequency of 3 MHz. Other parameters shift with frequency such as the proportional and integral DAC gains of Kp and KI. Not all parts lend themselves to scaling SYSCLK.

The target speed of the SSI 32H6812 is 5400 RPM. For the SSI 32H6812, a similar scaling relationship as given above for the SSI 32M595 can be computed for target speeds other than 5400 RPM. Change the demoninator to 5400 and the base frequency to 1 MHz. Any scaling of frequency for this component must be carefully considered since this SSI 32H6812 device is a combination of MSC and VCM functions. SYSCLK effects the VCM block also; therefore, changes in SYSCLK should be small and performed only to tweak the RPM.

External Power Drivers

Silicon Systems' MSC predrivers require external power drivers to connect to the motor. The two MSC predrivers are the SSI 32M595 and SSI 32H6820; both components are 5V and 12V compatible. Connection from the predriver to the power devices is through three pair of signals. Each pair consists of an upper P channel gate signal denoted as OUTUPx where x is A, B, or C motor terminal; and a lower N channel gate signal denoted as OUTx. Figure 3 illustrates typical connections for a predriver such as the SSI 32H6820 and external power drivers. A later section discusses blocking diodes and hard disk head retraction implementation.

The power MOSFETs chosen must be compatible with the predriver voltage levels. Of course turn-on resistance and peak current are deciding factors; however, MOSFET gate threshold is a key parameter. As an example, consider the SSI 32H6820 with the upper and lower output swings:

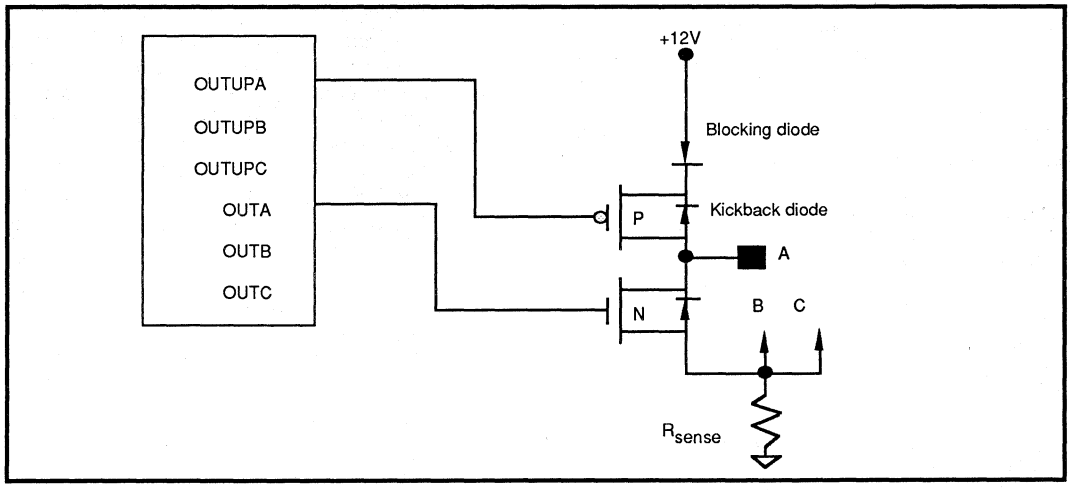


Figure 3. Predriver Connections to External MOSFETs

13

SIGNAL

OUTX

Vol 1V max @ 1 mA

Voh 4.5V min with Vm = 12V and -50 μA

OUTUPX

Vol 1V max @ 3 mA

Voh 12 V - pulled up with resistor

The lower N channel MOSFET must saturate with 4.5V on the gate and yet be completely turned off below 1V. A nominal gate threshold of 2V or 3V is necessary to meet these switching conditions. The upper P channel MOSFET has similar constraints when operating at 5V; however, for 12V operation the swing in gate voltage is so much wider that almost anything will work.

STARTING THE MOTOR

Starting a sensorless motor is more difficult than a motor with Hall sensors or brushes. Back EMF sensing requires a minimum motor speed to generate sufficient voltage for detection. When first starting the motor, no BEMF will be available and therefore some alternative scheme must be used to determine when to commutate.

Initializing Commutation State

The initial commutation state can be asserted by the microcontroller. The methods for performing this initialization vary with each component family. In general, there is little advantage in initializing the commutation state to a specific value because the rotor may be anywhere. When current is first applied, the rotor need only move forward or backward by at most one commutation angle to align with the applied stator field. The table below summarizes how each MSC component commutation state can be initialized:

DEVICE	INITIALIZATION METHOD
SSI 32M595	Clear $\overline{\text{RESET}}$ low
SSI 32M7010	Clear both $\overline{\text{BRAKE}}$ and $\overline{\text{RESET}}$ low
SSI 32M7011	Clear both $\overline{\text{BRAKE}}$ and $\overline{\text{RESET}}$ low
SSI 32H6810A	Clear both SLEEP and $\overline{\text{BRAKE}}$ low
SSI 32H6811	Clear both $\overline{\text{BRAKE}}$ and $\overline{\text{RETR}}$ low
SSI 32H6812	Program the START bit in MSC_MODE
SSI 32H6820	Program the STAT bits in register 0

Startup Methods

Various ways have been devised to compensate for the lack of BEMF when starting the motor. Most startup methods are open-loop in nature. The basic open-loop scheme is to operate the motor as if it were a stepper motor, synchronously following a commutation sequence which accelerates the motor speed up to the minimum RPM necessary for BEMF detection. The generation of the commutation sequence often is by a microprocessor, based on a table of timing values implementing a startup profile.

Open-loop startup schemes suffer in reliability when the motor or load conditions change. If the motor cannot follow the commutation sequence, the motor may fail to start. All open-loop startup methods should test for motor rotation and must retry to startup if the motor failed to spin up. Typically, two or three revolutions are all that is required to start the motor. For a 12 pole motor, the commutation sequence should provide 72 or more steps of open-loop commutation sequencing.

Computing a Startup Profile

An open loop commutation sequence can be calculated knowing the motor number of poles, number of phases, torque constant, start motor current, load inertia, and number of steps. The procedure below generates a series of commutation timing values which can serve as a starting point for the startup commutation sequence.

First, determine the distance traveled during each commutation to be:

$$\Delta = \frac{2 \cdot \pi}{N_P \cdot N_\phi} \text{ rads}$$

where N_p is number of poles and N_ϕ is number of phases.

When constant acceleration is assumed (which is reasonable for low RPM where the peak start current is constant), the angular acceleration (neglecting friction) is found from:

$$\alpha = \frac{K_T \cdot I_M}{J_\theta} = \frac{\text{rads}}{\text{sec}^2}$$

where k_T is torque constant and $J\theta$ is inertia.

Integrating α over the interval 0 to "t" yields angular velocity at time "t":

$$\omega = \int \alpha d\tau = \alpha \cdot t \ \frac{\text{rads}}{\text{sec}}$$

Absolute rotor position is found from the integral of velocity from 0 to "t":

$$\theta = \int \omega d\tau = \frac{\alpha \cdot t^2}{2}$$

The startup routine will generate a sequence of commutations in time which should result in the rotor traveling a total absolute distance of θ. Knowing the distance the rotor travels to be θ_i, the time can be found to be:

$$t_i = \sqrt{\frac{2 \cdot J_\theta}{K_T \cdot I_M} \cdot \theta_i}$$

where the subscript "i" corresponds to each commutation sequence step ranging from 0 to the number of steps required. Each distance is computed as:

$$\theta_i = i \cdot \Delta$$

The instantaneous velocity at time "t_i" is computed from:

$$\omega = \frac{K_T \cdot I_M}{J_\theta} \cdot t_i \cdot \frac{60}{2 \cdot \pi} \text{ RPM}$$

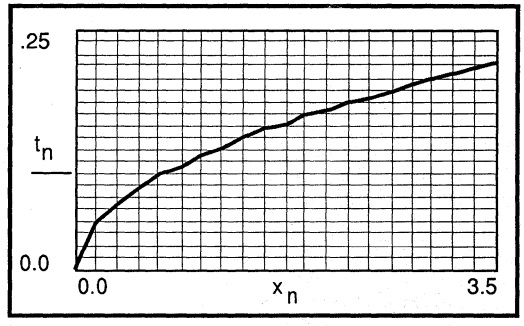
As an example, consider a design having the following properties:

$J_\theta = 0.024$ and $k_T = 3.7$ in consistent units,

$I_m = 1$A peak start current,

$N_p = 12$ poles and $N\phi = 3$ phases.

The startup profile of commutation time (absolute) to commutation position is plotted below:



Plot 1: 20 Step Startup Profile

An Open Loop Startup Method

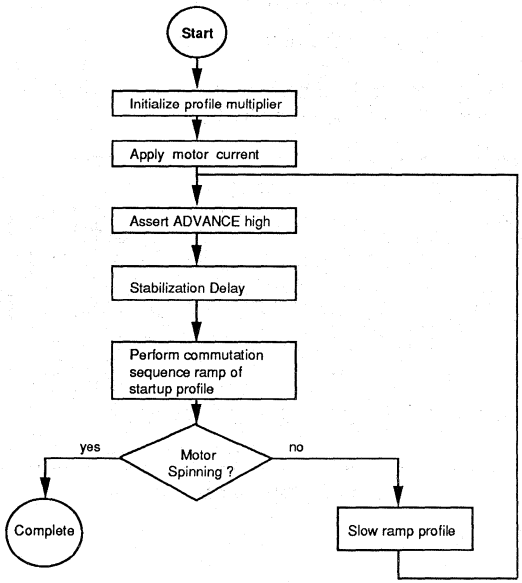
The open loop startup profile may be computed and placed in a ROM based table within the microprocessor. The microprocessor then uses the startup profile table as timing values which determine when the ADVANCE pin must be asserted. The basic startup method performs the following:

1. Initialize the motor with current
2. Ramp the motor with the startup profile
3. Check motor spin up, if it fails then repeat 1

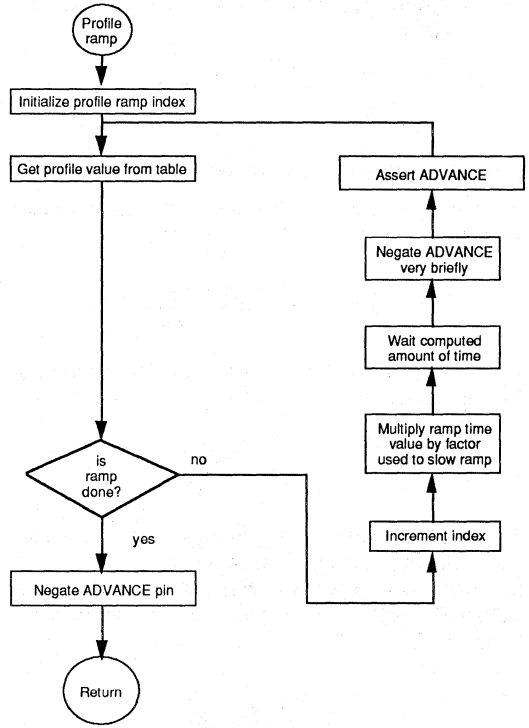
An enhancement to the basic startup method is to modify the startup profile so that a wider range of motor/load conditions can be addressed. This enhancement adds a degree of adaptivity by trying a slightly aggressive profile first, then if the motor fails to spin up, modify the profile so that it is slower. By slowing the profile, the startup method becomes more robust in its attempt to retry startup of the motor. The more robust startup method is outlined below:

1. Initialize profile setting
2. Initialize the motor with current
3. Ramp the motor with the startup profile
4. Check motor spin up, if success then complete
5. Slow the startup profile and repeat 2

Two flow charts describe the enhanced open loop startup method example. The first flow chart describes the outer loop responsible for all steps except number 3 listed above. The second flow chart describes step 3 only.



Flow Chart 1 - Outer Loop of Open Loop Startup



Flow Chart 2 - Inner Loop of Open Loop Startup

Variation on Startup for the SSI 32H6812

The basic open-loop startup method outlined above is applicable to the SSI 32H6812 as well. The SSI 32H6812 requires a few extra steps due to the way the start current command is generated and other programable options. These extra steps are outlined below:

1. Setup for Startup
2. Program the Start Current Command DAC
3. Ramp Up the Motor
4. Precharge and Speed Control

The steps outlined above are graphically represented in Figure 4.

Program the Start Current Command DAC

The start current command is determined from the voltage at the LF pin. Setting the MSCDAC bit in the MSC_MODE register redirects the 10-bit VCM positioning DAC to the LF pin. At the same time, the redirected DAC voltage is level translated down so that binary zero is half way between 0 and 2.25V. Program the VCM DAC with a value which will correspond to the start current command required.

Ramp Up the Motor

Toggle the ADVANCE bit in the MSC_MODE register as outlined earlier for open loop startup.

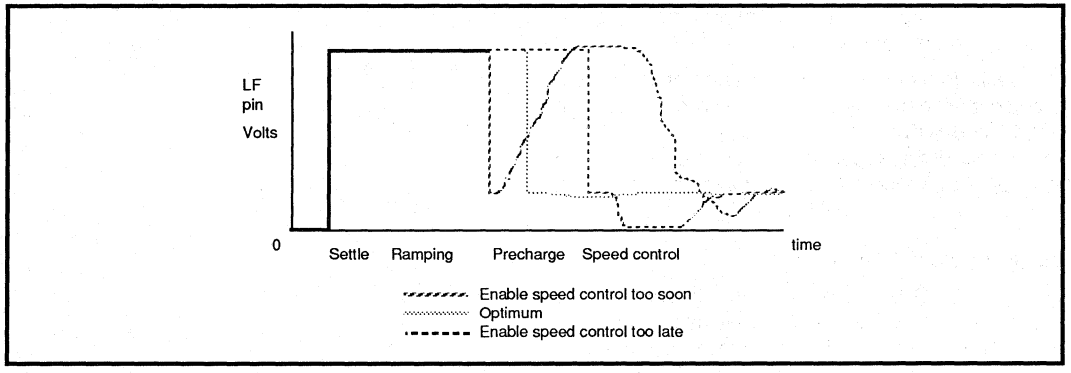


Figure 4. SSI 32H6812 Startup Sequence at LF Pin

Setup for Startup

To setup for motor startup, the START bit in the MSC_MODE register is set true. Setting START resets the commutation state counter and blocks the BEMF event detector thereby insuring that only transitions of the ADVANCE pin advance the commutation state counter. Also, the commutation delay should be set to one of the fixed values using the DELAY bits in the MSC_MODE register (see a later section on commutation delay).

Other setup includes negating $\overline{\text{RETR}}$ and $\overline{\text{BRAKE}}$ and asserting STANDBY by setting these all to binary "1" in the CONT_MODE register.

Precharge and Speed Control

At the end of the startup ramp, return the START and ADVANCE bits to zero thereby enabling BEMF events to get through and self commutate the motor. At the same time, the commutation delay should be returned to adaptive by clearing the DELAY bits in MSC_MODE.

Some time later, program the DAC to a value corresponding to the typical run time voltage at the LF pin. This programmed value will serve to "precharge" the integrator thereby initializing the LF pin voltage. When to actually precharge is a degree of freedom dependent upon how fast the motor accelerates and what the requirements are upon speed overshoot and settling time. The precharge duration itself may be fairly brief being typically a few miliseconds in length.

Precharge and Speed Control (continued)

After the precharge is complete, the MSCDAC bit is returned to zero so that the speed control loop is enabled.

If the speed control loop is entered immediately after the completion of the startup ramp, the motor will not yet have reached the target speed and the voltage on the LF pin will rise from the precharge value. The speed control loop will command more current and the LF voltage will first rise then fall back to the final steady state value.

If speed control loop is entered too late, the motor will have overshot the target speed. The LF pin voltage will discharge to zero quickly and the motor will slow down due to friction. Finally, the motor speed will pass through the target and the control loop will close thereby locking motor speed.

The decision as to when to transition from startup to speed control can be implemented in two ways. In the first method, a fixed delay to enabling speed control is emperically determined. The second method relies on the TOO SLOW indication selectable from the REV/COM pin of the SSI 32H6812.

Using the COM/REV Indicator

To use the TOO SLOW indicator, the CRL1 and CRL0 bits in the MSC_MODE register may be set such that the COM/REV pin is "1" when the motor is more than 10% too slow. The COM/REV pin is selected first to detect commutation activity to determine if the motor is spinning. After finding the motor spinning, COM/REV is reprogrammed for monitoring TOO SLOW. TOO SLOW will be asserted until the motor speed is faster than -10% of the target and should be monitored by the microcontroller. When TOO SLOW is negated, the speed control is enabled and COM/REV is reprogrammed for monitoring LOCK. The table below indicates how the COM/REV pin selections are made:

CRL1	CRL0	COM/REV
0	0	Commutation Event
0	1	Revolution Event
1	0	LOCK indicator
1	1	Too slow indicator

Firmware Startup Example

Firmware listing 1 illustrates a "C" code based startup routine implemented on an 8051 microcontroller supporting a SSI 32H6811. This particular startup example includes the ramp up logic and tests for motor spinning and oscillation. In a later section discussing speed control, a "C" code example of speed control is provided.

Listing 1. "C" Code Startup

```
/* ramp scale factors */

#define RAMP_MIN 15
#define RAMP_START 20
#define RAMP_MAX 30

const unsigned int ramp_table[RAMP_LEN] = {
   1124,465,357,301,265,239,220,205,192,182,
   173,165,159,153,147,142,138,134,130,127,
   124,121,118,115,113,111,109,107,105,103,
   101,100,98,97,95,94,93,91,90,89,
   88,87,86,85,84,83,82,81,80,79,
   79,78,77,76,76,75,74,74,73,72,
   72,71,71,70,70,69,68,68,67,67,
   66,66,66,65,65,64,64,63,63,63,
   62,62,61,61,61,60,60,60};
```

void start_motor(void)

```
{
unsigned int ramp_scale;
int i;

and_systat(~MOTOR_RUN); //turn off MOTOR_RUN bit in sys_status
or_systat(MOTOR_RUN);  // Set status to reflect motor started
and_systat(~MOTOR_START);
}
or_systat(MOTOR_START); //turn on MOTOR_START bit in sys_status

ramp_scale = RAMP_START;  // init value - adaptive feature in ramp

while(sys_status & (MOTOR_STALL | MOTOR_RACE))
  {
  /* reset commutation counter */
  clear_bit(RETR);
  clear_bit(BRAKE);

  set_bit(ADV);                  // block BEMF event feedback
  delay(USEC(1000));     // 1 mS so that reset asserted
  set_bit(RETR);
  set_bit(BRAKE);

  /* command start current - setup DAC and sense gain to 5
  send_packet(MSC | (0x1ff << DAC_SHIFT)); /* max VIN */
  send_packet(MODE | REV | GAIN_5 | (3<<N_SHIFT));

  /* pulse ADVANCE low to high to insure driver enabled*/
  clear_bit(ADV);
  set_bit(ADV);
```

void start_motor(void) (continued)

```
/* wait a LONG time for rotor to settle */
long_delay(4);

/* accelerate motor by going through the startup ramp */
for(i=0; i < RAMP_LEN; i++)
  {
  delay(ramp_scale * ramp_table[i]);
  clear_bit(ADV);
  set_bit(ADV);
  }

/* enable normal adaptive commutation */
clear_bit(ADV);
send_packet(MODE | REV | GAIN_5 | (1<<N_SHIFT));

ramp_scale = (ramp_scale < RAMP_MAX)
           ? ramp_scale + 1 : RAMP_MIN; // change for retry
long_delay(2);        /* wait before checking for successful start */
}
```

Supporting Assembly Language

Though the startup firmware is written in "C," some low level assembly language was required for serial port and high speed interrupt handling. The key assembly language subroutines are listed below for detailed reference.

The two interrupt handlers work together. Time_Int is called when timer 1 expires indicating that the motor is turning too slowly. Rev_Int is called on each high-to-low transition of the SSI 32H6811 REV_CLK pin. Rev_Int measures motor period and when necessary, it makes a call to a subroutine used to control speed (discussed in detail in a later section).

```
; 8051 Resource initialization for this example taken
; from the strip of code executed on reset.
;-------------------------------------------------------------------------------------------------------------------;

.
.
.
; 8051 Resource initialization for this example taken
; from the strip of code executed on reset.
;-------------------------------------;
        .
        .
        .
        SETB   ET1              ;enable timer1 interrupt
        SETB   EX0              ;enable REV_CLK to be interrupt
        MOV    IP,#0            ;priority mask
        MOV    SCON,#0          ;serial mode 0 for SSI 32H6811 use
        MOV    TMOD,#011h       ;both timers in mode 1
        MOV    TH1,#0           ;reset period watchdog timer
        MOV    TL1,#1
;-------------------------------------;
; initialize the 8051
        SETB   TR1              ;enable period watchdog timer
        CLR    TR0              ;turn off timer 0 (general use)
        SETB   IT0              ;select edge-triggered interrupts
        SETB   IT1
        SETB   COMREV           ;make REV_CLK pin readable
        SETB   EA               ;enable interrupts
        .
        .
        .
.
.
.
```

```
    ; send_packet: send the word stored in R2 (MSB) and R3 (LSB)
    ; to the SSI 32H6811
    ;
send_packet:
      SETB  SDEN        ; Assert SDEN to enable serial transfer
      CLR   TI
      MOV   SBUF,R3     ; Send the LSB first
      JNB   TI,$        ; wait for transfer to complete
      CLR   TI
      MOV   SBUF,R2     ; Send MSB
      JNB   TI,$
      CLR   SDEN        ; Drop SDEN to end transfer
      RET
;-------------------------------------------------;
; REVCLK watchdog interrupt handler               ;
;-------------------------------------------------;
time_int:
      CLR   EA
      CLR   TR1         ; turn off timer
      MOV   TH1,#0ffh   ;Set timer to value which signals
      MOV   TL1,#0ffh   ;that it has expired.

      ; rphase is an internal variable read in rev_cnt int
      ; and it divides rev_cnt interrupts by 3 because the
      ; test motor was 12 pole
      MOV   rphase,#3

      ; Set signals tested in C code indicated motor stalled
      ; and not locked or racing
      ORL   sys_status,#MOTOR_STALL
      ANL   sys_status,#((MOTOR_RACE OR MOTOR_LOCK) XOR 0ffh)
      SETB  EA
      RETI
;-------------------------------------------------;
; REVCLK interrupt handler                        ;
;-------------------------------------------------;
```

```
rev_int:
      CLR   EA
      DJNZ  rphase,ri00 ; decrement phase counter
      ; take this path on the 3rd interrupt, measure period now
      CLR   TR1         ; stop timer
      MOV   rphase,#3   ; reset phase counter
      MOV   revcnt,TH1  ; store timer count in locs C code sees
      MOV   revcnt+1,TL1
      MOV   TH1,#0      ; reset timer to count next period
      MOV   TL1,#1
      SETB  TR1
      SJMP  ri01
ri00: LJMP  rexit2
ri01:
      ; Save machine state here - dependent on C compiler useage
      ; clear stall flag if TH1 was < 0ffh (now in revcnt)
      MOV   A,revcnt
      INC   A
      JZ    ri1         ;jumps if was stalled
      ANL   sys_status,#(MOTOR_STALL XOR 0ffh) ;not stalled
ri1:
      ; check for racing motor (indicates stalled spindle and
      ;                 motor oscillation)
      MOV   R4,revcnt
      MOV   R5,revcnt+1
      MOV   R2,#00fh    ; 10000 RPM @ 8 MHz
      MOV   R3,#0a0h
      LCALL ?UI_CMP_LT_L02 ;Borrow compiler int compare sub
      JZ    ri2         ;nonzero means not less than such that
                        ;the motor must not be oscillating
      ORL   sys_status,#MOTOR_RACE              ; set MOTOR_RACE
      ANL   sys_status,#(MOTOR_LOCK XOR 0ffh)   ; clear MOTOR_LOCK
      SJMP  rexit
      ; motor is not racing, so clear MOTOR_RACE flag
ri2:  ANL   sys_status,#(MOTOR_RACE XOR 0ffh)

      ; if motor is supposed to be running, as indicated by
      ; MOTOR_RUN flag, then call speed control function
      MOV   A,sys_status
      ANL   A,#MOTOR_RUN
      JZ    rexit
      MOV   R1,#0       ; no parameters on stack
      LCALL speed_control
rexit:
rexit2:
      SETB  EA
      RETI
```

COMMUTATION DELAY

Silicon Systems MSC components implement two different methods for delaying motor commutation from the detection of the BEMF event. These two methods of commutation timing are fixed delay and adaptive delay. Most components implement one or the other, however, the SSI 32H6811 and SSI 32H6812 provide both. The table below identifies the methods used by the MSC family members:

DEVICE	METHOD
SSI 32M595	Fixed
SSI 32M7010	Adaptive
SSI 32M7011	Adaptive
SSI 32H6810A	Adaptive
SSI 32H6811	Both, programmable mode
SSI 32H6812	Both, programmable mode
SSI 32H6820	Fixed

Fixed Commutation Delay

Fixed commutation is implemented with a non-retriggerable oneshot. When the BEMF event is sensed, the one shot is triggered. The one shot duration is programmable with an external resistor and capacitor network in the SSI 32M595 and SSI 32H6820. The one shot duration is internally set within the SSI 32H6811 and SSI 32H6812.

The fixed commutation delay provides two functions. The first function is to delay the actual advancement of the commutation state counters from the sensing of the BEMF event. Choosing the RC network for the target RPM results in optimum motor operation. The second function of the delay circuit is to provide a noise-gating interval where the transient noise resulting from motor commutation is ignored.

When using fixed commutation delay, the same delay duration is present throughout the operating region of the motor. This means that the delay used at startup is the same as that for the target operating speed. Only the target operating speed is optimum; startup does not operate at the optimum point.

Most hard-disk motors are very trapezoidal in nature. This means that the BEMF voltage waveform across the motor windings appear to have a trapezoidal shape for a constant speed. The slope of the transition from most positive to most negative is fairly great unlike the changing slope corresponding to a sine wave. For trapezoidal motors, optimum commutation delay results in only a very slight improvement in motor efficiency.

Fixed commutation offers a simple, robust design. The single RC time constant configures the motor throughout its operating range. For a broad range of motor applications, fixed commutation delay is superior because it offers greater noise rejection compared to adaptive methods.

Extending the Noise Gate Interval

In some instances when using the SSI 32M595 or SSI 32H6820, one fixed delay is not sufficient. These instances occur when the start current transients do not die off quickly enough and false BEMF events are detected. This failure occurs because the fixed commutation delay also provides a noise blanking interval. At high target RPMs, the time constant is small so the large amplitude transients present at startup still have significant amplitude after the noise blanking interval has expired.

When a single delay time constant is not sufficient, an analog switch and series resistor may be added to extend the commutation delay over wider range of operating conditions. Figure 5 illustrates such a circuit. The analog switch is open when starting the motor, then closed usually after the startup ramp is complete. The RC time constant is based on just the resistor and capacitor itself at startup; during run the RC time constant is based on the parallel resistance of the two resistors and the capacitor. The microprocessor is responsible for closing the analog switch.

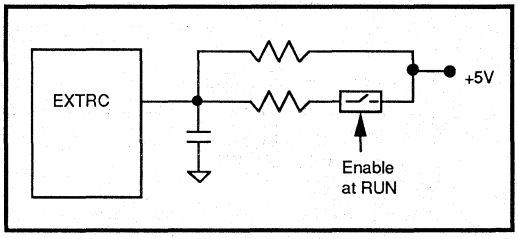


Figure 5. Extending Fixed Commutation Delay

Design Example

For the SSI 32H6820, the RC network is placed at the EXTRC pin. The capacitor goes to ground while the resistor pulls up to 5V. The minimum resistance is 10K with a maximum of 10 MΩ, capacitance must be greater than 100 pF. From the data sheets the following is given:

$$\tau_d = 0.56 \cdot R \cdot C \quad \text{sec}$$

$$\tau_n = 0.29 \cdot R \cdot C \quad \text{sec}$$

where τ_d is the commutation delay period and tn is the additional noise blanking interval occurring after the delay. These time constants must be chosen so that:

$$\tau_c < \tau_d + \tau_n$$

where τ_c is the target RPM commutation period. If this constraint is not met, the motor will fail to commutate properly at the target speed. This false commutation will appear as rough, irregular operation indicated by a very irregular drive voltage waveform at the motor terminals.

If the target speed is 5400 RPM and the motor is 12 pole, the target commutation period is:

$$\tau_c = \frac{60}{36 \cdot 5400} \text{ or approximately } 309\ \mu s$$

Choose the sum of $\tau_d + \tau_n$ to be less than τ_c to build in margin. Picking this sum to be:

$$\tau_{rc} = 0.8 \cdot \tau_c$$

allowing for 20 % total error in the RC network, yields a design target:

$$\tau_{rc} \cong 250\ \mu s$$

Choosing a common value for C of .01 µFd, yields R of:

$$R = \frac{\tau_{rc}}{C} = 25\ k\Omega$$

Adaptive Commutation Delay

Adaptive commutation delay does not require any external components. Instead, the adaptive commutation delay circuit determines the optimum commutation time by observing the prior period. In this way, the next commutation period is predicted by looking at the prior period history.

The SSI 32H6810A is an example of a device which implements only adaptive commutation delay. In the SSI 32H6810A, the adaptive circuit delays the advancement of the motor commutation state counter by 3/7ths of the prior commutation period. The noise blanking interval following motor commutation is an additional 2/7ths (specified in the data book as 5/7ths from the beginning of the commutation period).

The adaptive commutation delay circuit has a very wide range of operation. This range is specified relative to a nominal target speed of 3600 RPM. For the SSI 32H6810A, the adaptive range is -80% to +50%. Though a nominal target speed is given, this value does not suggest a necessary operating speed. Instead, the nominal speed given is based on the frequency of SYSCLK which internally sets the rate at which the adaptive circuit switched capacitors operate.

For the SSI 32H6810A, there are restrictions on what values SYSCLK can assume because this clock is used also in the positioner motor sense amplifier. In a device like the SSI 32M7011, SYSCLK can be modified freely since it only effects the adaptive circuit itself. The nominal frequency is linearly scaled with SYSCLK.

For the SSI 32H6810A, the adaptive commutation delay operating ranges versus the allowed range in SYSCLK are:

SYSCLK	RPM Low end	RPM Nominal	RPM High end
1.5 MHz	540	2700	4050
2 MHz	720	3600	5400
2.5 MHz	900	4500	6750

Adaptive commutation may improve motor operating performance slightly. It has the advantage that the motor commutation is dynamic and may improve spin up time slightly. Also, no external components are necessary to configure the commutation delay. The adaptive circuit has the disadvantage of greater noise sensitivity compared to fixed delay.

Selecting the SSI 32H6811 Delay Mode

The SSI 32H6811 provides programmable commutation modes. The mode register at address 01 contains both the M and N bits which are decoded as follows:

M	N	Commutation Delay Method	Comment
0	0	Adaptive	INCOM effects adaptive timing
0	1	Adaptive	INCOM ignored
0	2	Adaptive	INCOM ignored
0	3	Fixed, one-shot	INCOM effects one-shot timing
<>0	X	Fixed, one-shot	PWM, INCOM one-shot timing

The table above shows that both M and N bits within the mode control register effect commutation delay and the power control method. For the SSI 32H6811, PWM is a switched mode of operation intended for used only at startup.

The pin INCOM can effect the commutation delay circuits of both methods. When M is zero and N is 1 or 2, the commutation delay is adaptive and INCOM is ignored. In all other modes, INCOM is an input. Generally, INCOM is not useful in modifying the adaptive delay timing. However, the voltage on INCOM must be externally set for one-shot mode. Typically, a voltage divider is used to setup the voltage on INCOM using the following guidelines:

INCOM VOLTAGE	ONE-SHOT DELAY
0.5V	150 µs
2.5V	500 µs

Setting INCOM for 2.5V yields the best overall one-shot timing well suited for starting the motor. The 500 µs one-shot commutation delay results in a total noise blanking interval of 850 µs which should be sufficient in all cases to insure that the startup current amplitudes die down to insignificant levels. The maximum RPM before miscommutation occurs under these one-shot conditions is computed from:

$$RPM_{Max} = \frac{60}{\tau_n \cdot N_p \cdot N_\phi}$$

where: τ_n is the noise blanking interval such as 850 µs,
Np is the number of poles, and
Nϕ the number of phases.

With 12 poles and three phases, RPM_{MAX} is 1960 RPM. Clearly, the microprocessor must switch from one-shot mode into adaptive mode before this maximum RPM is reached or else miscommutation will occur. Note that if one-shot mode is desired under all conditions, set the voltage at INCOM lower so that a higher target RPM can be reached. The lower limit of INCOM voltage is approximately 0.5V.

Programming the SSI 32H6812 Delay Mode

The SSI 32H6812 offers both adaptive and fixed commutation delay like the SSI 32H6811. The SSI 32H6812 delay mode is selected by programming the DELAY bits in the MSC_MODE register as listed below:

DELAY1	DELAY0	MODE
0	0	Adaptive
0	1	Fixed at 150 µs
1	0	Fixed at 300 µs
1	1	Fixed at 500 µs

Fixed commutation places an upper bound on the operating motor speed. When the motor speed increases, the commutation period decreases and miscommutation will occur when these are equal. The maximum RPM before miscommutation occurs under these one-shot conditions is computed from:

$$RPM_{Max} = \frac{60}{\tau_n \cdot N_p \cdot N_\phi}$$

where: τ_n is the fixed delay period, such as 500 µs
Np is the number of poles, and
Nϕ the number of phases .

With 12 poles and three phases, RPM_{MAX} is 3300 RPM. Clearly, the microprocessor must switch from fixed delay mode into adaptive mode before this maximum RPM is reached or else miscommutation will occur.

MOTOR OSCILLATION

The SSI 32H6810A, SSI 32H6811, and SSI 32H6812 are intended for small form factor hard-disk drives typically of 2.5" or less. The motor voltage constant of many of these drive motors is particularly low and therefore, these devices offer sensitive comparators to detect the BEMF at low speeds. Under certain circumstances, it is possible for the motor to get into a condition where it will oscillate. When this oscillation occurs, the motor will not spin.

Motor oscillation occurs when the motor is energized but it is not turning. Under this situation, there is no BEMF for the comparators to detect. Without BMF, noise can falsely trigger a BEMF detection event. When this happens the commutation state counter is advanced and more noise is generated by the very act of commutation. If the motor is not turning, this sequence will continue and increase in frequency. Very quickly, the motor will break into oscillation.

The conditions which may lead to motor oscillation are:

1. The motor can't follow the startup ramp
2. The terminal speed at the end of the ramp is too low
3. The motor rotor is stuck

The steps to solve oscillation are:

1. Insure the motor can follow the ramp
2. Insure terminal speed generates at least 100 mV BEMF
3. Select fixed commutation delay during startup
4. Implement software detector for oscillation
5. Implement snubbers (sometimes needed in 12V drives)

By making sure the motor can follow the ramp, the occurance of oscillation will be avoided. This is because a rotating motor generates BEMF which will dominate all noise sources. Of course, the terminal speed of the ramp must provide sufficent speed to generate at least 100 mV of BEMF though more is always better.

Fixed delay offers better noise rejection compared to adaptive. In general, the longer fixed delays are better. The adaptive circuit will adapt to the noise itself and quickly move to the shortest commutation interval. In these parts, this minimum interval is 125 µs yielding a commutation state change frequency of 8 kHz.

It is possible to detect motor oscillation since the resulting frequency is much higher than the operating commutation rate. Such a detector could be implemented in the startup firmware during the test to see if the motor is spinning after the ramp. The test for spinning may involve counting the number of commutation state changes over a fixed period of time. If it is observed that the period of state changes is less than some threshold, it may be deduced that the motor is oscillating and the startup should be retried.

Finally, snubbers may eliminate oscillation. Snubbers effect the transient waveform across the motor. In 12V designs, there may be high amplitude voltage transients during startup which take a long time to die out to a negligible value. The SSI 32M595 does not implement dV/dT limiting and therefore snubbers are the only way to modify the transient response.

ADVANCE MISCOMMUTATION

ADVANCE miscommutation is the event where the commutation state counter did not properly respond to the rising edge of the ADVANCE signal during startup. The causes for miscommutation are:

1. ADVANCE pulse width too wide
2. Low BEMF and comparator noise
3. Motor following ramp too closely

ADVANCE Pulse Width Too Wide

All Silicon Systems MSC devices to date except the SSI 32H6812 rely on the ADVANCE pulse during startup to block BEMF detection. (The SSI 32H6810B and SSI 32H6811B implement a new design which prevents miscommutation; this section is not applicable to these new parts.) Internal to the device, ADVANCE is logically OR'ed with the signal associated with BEMF detection events. During startup, the rising edge of ADVANCE will increment the commutation state counter. The startup firmware should keep ADVANCE high most of the time and lower it only briefly to assert the next low-to-high transition.

In this design, there is a brief window where a collision between the ADVANCE edge and a BEMF detection event can occur. Depending upon the width of the ADVANCE pulse, the collision can result in the following outcomes:

a. No commutation error

b. Failure to commutate

c. Double commutation

ADVANCE Pulse Width Too Wide (continued)

Figure 6 below illustrates graphically the possible outcomes:

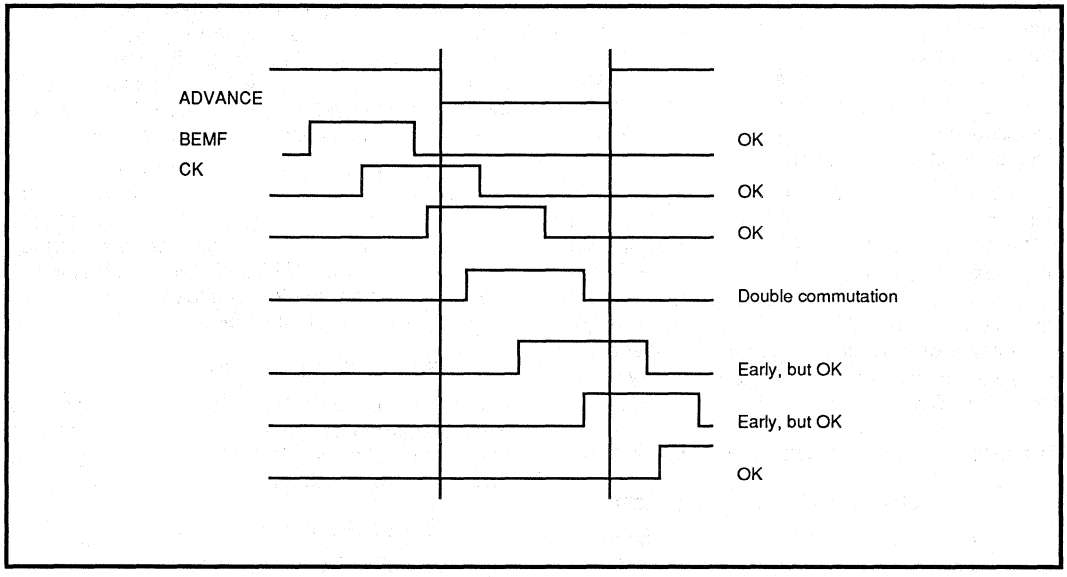


Figure 6 - Advance/BEMF Event Collisions

Low BEMF and comparator noise

In the 681X MSC devices, the comparator sensitivity is particularly high. This sensitivity is high so that the low BEMF generated by small form-factor drives can be detected. During startup, there is very little BEMF and therefore any noise may trigger the comparators to falsely detect BEMF events. This increases the chance for ADVANCE pulse collision discussed in item 1 above.

Motor following ramp too closely

During open loop startup discussed earlier, the motor is accelerated by following a commutation ramp. If the motor is following the ramp very closely such that there is essentially no "slip," then a true BEMF event may occur precisely at the time where the next ADVANCE pulse is to be generated. The occurance of this is rare but it does relate to item 1 above. Often, increasing the speed of the ramp slightly will eliminate this event from occuring.

Miscommutation Solution

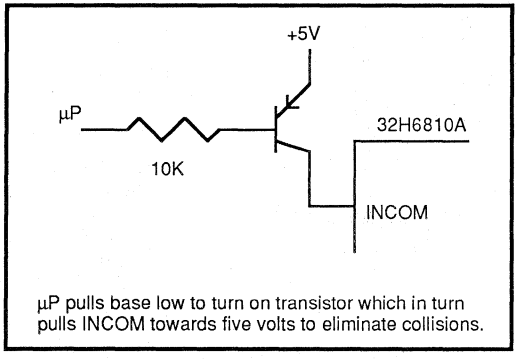
Solutions which insure proper startup commutation are itemized as follows:

DEVICE	SOLUTION
SSI 32M595	Minimize ADVANCE width, τ>2 µs
SSI 32M7010	Pull INCOM high during startup
SSI 32M7011	Pull INCOM high during startup
SSI 32M6810A	Pull INCOM high during startup
SSI 32M6811	Pull INCOM high during startup
SSI 32M6812	Assert START bit to block
SSI 32M6820	Program STAT bits to set state

The SSI 32M595, SSI 32M7010, SSI 32M7011, and SSI 32H6820 devices tend to have lower comparator sensitivity and therefore should not be subject to comparator noise. Typically for these parts, the only type of event which results in miscommutation is due to the motor following the ramp too closely.

Pulling up INCOM refers to a technique of forcing +5V

on the INCOM pin during startup. This method can be implemented by placing a PNP transistor with the emitter at +5V, collector on INCOM, and the base controlled through a resistor. Typically a 10 k Ω resistor and a 2N2222A type transistor will work. It is necessary to provide some output signal which can sink base current and turn on the transistor during startup. When switching to run, the transistor should be turned off. See Figure 7 for a circuit diagram to pull INCOM high.



µP pulls base low to turn on transistor which in turn pulls INCOM towards five volts to eliminate collisions.

Figure 7. Pull INCOM High to Eliminate Miscommutation

The SSI 32H6812 and SSI 32H6820 differ from the balance of the MSC parts. The SSI 32H6812 has a bit which when set high blocks all BEMF events and insure no miscommutation. The SSI 32H6820 has three bits which directly specify the next commutation state. In the SSI 32H6820, it is recommended to program these bits instead of pulsing ADVANCE when miscommutation is a concern.

COMMUTATION TRANSIENTS

When the motor is commutated, transient voltages and currents result. The magnitude of these transients can be reduced in various ways across the Silicon Systems MSC product family. The table below indicates what methods are available to each component in the MSC family:

DEVICE	TRANSIENT REDUCING METHOD
SSI 32M595	External Snubbers
SSI 32M7010	dV/dT limiting
SSI 32M7011	dV/dT limiting
SSI 32H6810A	dV/dT limiting
SSI 32H6811	dV/dT limiting
SSI 32H6812	dV/dT limiting
SSI 32H6820	dV/dT limiting

The commutation transient is generated by the switching off of current in a motor leg while commutating as figure 8 illustrates. Each motor leg has a significant inductance and when the conduction path for the current in the motor leg is abruptly reduced, the energy stored in the charged inductor discharges resulting in a transient.

The current rise when turning on a motor leg is determined by the electrical time constant of the motor inductance and total series resistance of the motor and drivers. By commutation sequence design, there will not be any initial current flowing in the motor leg.

When turning off a motor leg, the energy stored in the inductor can be thought of as an initial condition modeled by current source which will decay in amplitude. The decay time constant will be determined by the motor inductance and the total resistance making up the inductor discharge path. The voltage polarity of the transient is determined by which end of the motor leg is switched off. If the upper leg is switched off while the lower leg is held near ground, the transient voltage will be negative in amplitude. When the lower leg is switched off while the upper leg is held near the supply voltage, the transient voltage will be positive in amplitude.

Negative going transients are limited by diodes to ground as shown in figure 8. Positive going transients are limited in different ways depending on the circuit implementation. Figure 8 illustrates the transient response for a device with stacked N channel MOSFET integrated drivers such as the SSI 32H6810A.

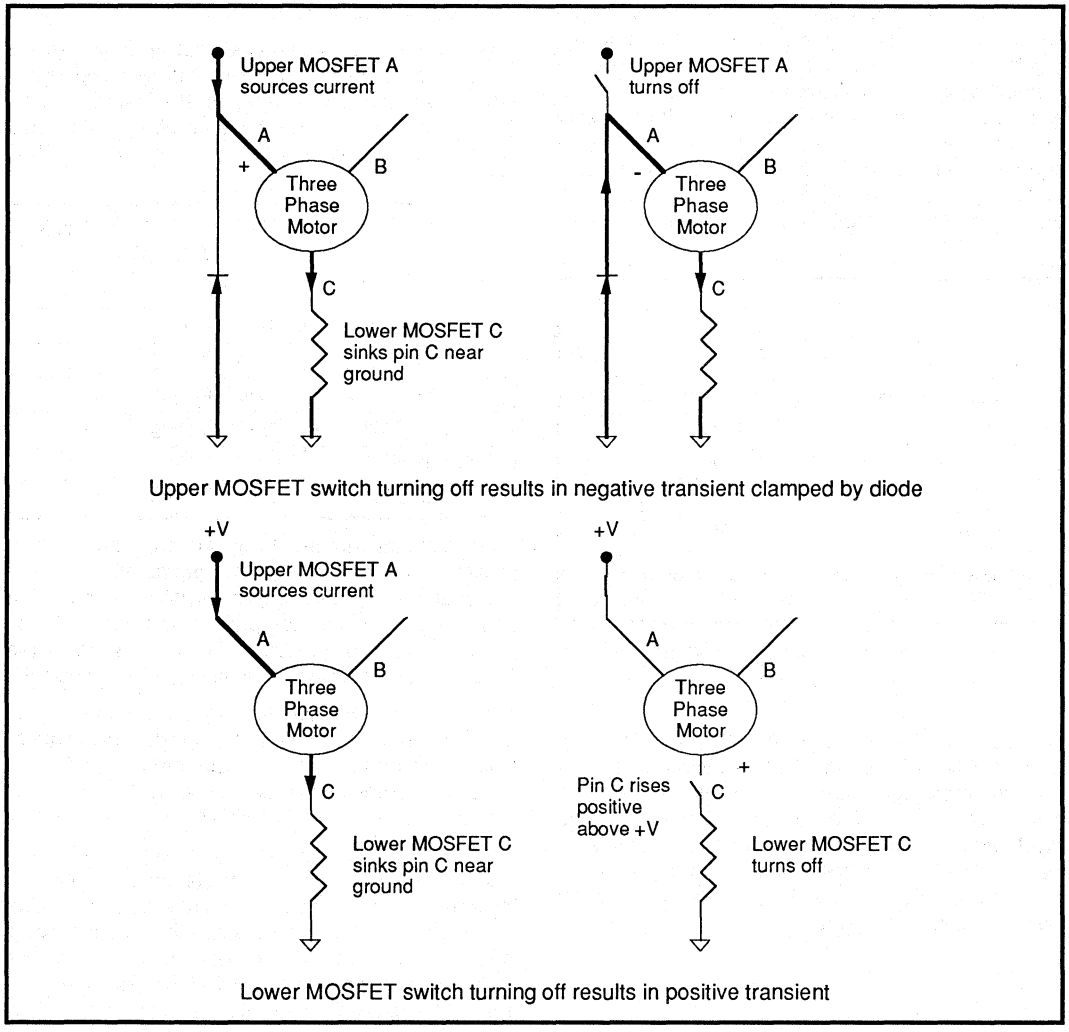


Figure 8. Switching Transients with Integrated Drivers

COMMUTATION TRANSIENTS (continued)
The SSI 32M6810A internally implements stacked N channel MOSFETs. The lower N channel devices have kick back diodes useful for rectifying the spindle motor for retract purposes. The SSI 32H6810A does not require a blocking diode since there is no inherent parasitic diode across the upper N channel FET. Three external diodes are added to complete the full-wave rectification of BEMF for retract voltage. The common point of these three diodes is connected to the VBEMF pin on the SSI 32H6810A. The positive transient discharge path is a high impedance consisting of the upper diode to and into the VBEMF pin. Limit the peak transient voltage with sufficient dV/dT adjustment.

When using external power MOSFETs such as with the SSI 32H6820, kick-back protection diodes are always found across the P and N channel MOSFET sections. The lower protection diode shunts the motor terminal to ground through the sense resistor. In a bipolar (full-wave) drive mode, the positive transient is discharged through low impedance made up by the upper kick-back diode and P channel MOSFET currently switched on. In unipolar drive mode, the discharge path is a high impedance because there isn't an upper P channel MOSFET. For unipolar mode, the peak transient voltage may significantly rise above the spindle voltage supply and must be limited by dV/dT or snubbers.

Adjusting dV/dT with RRAMP

In most Silicon Systems MSC components, the lower driver turn-off time can be adjusted. When the lower driver is turned off in a slower, controlled manner (compared to an abrupt switching off), the positive going transient voltage amplitude is reduced. This dV/dT (rate of change in voltage) limiting action of the lower driver serves to discharge the inductor and reduce the transient voltage developed across the inductor discharge path.

A resistor is used to adjust the lower driver gate turn off time. For the SSI 32H6811, the following relationship is specified:

$$\frac{dV}{dt} = \frac{15}{RRAMP} \quad \frac{V}{\mu s}$$ where RRAMP is in kΩ.

RRAMP is a resistor which sets an internal current source responsible for turning off the driver by lowering the gate voltage. The amplitude of this current source determines the speed at which the driver gate voltage drops. Actually, the lower driver turn off effects the dI/dT (rate of change in current) in the motor leg. The transient normally observed is the voltage which results across the inductor from the dropping motor current as described in the basic equation:

$$V_{inductor} = L \cdot \frac{dI}{dt}$$

Snubber Networks

Snubber networks are RC networks placed across the motor windings. "Snubbing" networks are designed to provide a path for the transient current to flow when the motor leg is turned off. The basic network is a series resistor and capacitor combination which is placed across two adjacent motor terminals, three such networks are needed for a three phase motor.

The design of the snubber network is completely discussed in the Silicon Systems application note titled: Snubbing Network Design for Spindle Motors.

INTERNAL SPEED CONTROL

Several Silicon Systems MSC family members provide internal speed control while the rest require external speed control. There are two types of internal speed control provided in Silicon Systems MSC components:

1. Digital PI configured with resistors
2. Charge pump and loop filter

Both speed control methods make use of a crystal based clock for precise digital period measurement and internally compute velocity error. The PI (proportional-intregal) type digitally integrates the error, generates analog voltages from DACs, and configures compensation with resistors. The charge pump type applies a current proportional to the speed error through a second order passive filter which configures the compensation.

Digital PI Speed Control

The SSI 32M595, SSI 32M7010, and SSI 32M6820 all provide internal digital PI speed control. The SSI 32M6820 differs slightly from the others because it has programmable target speed and number of motor poles.

Startup and Linear Control Modes

The internal speed control circuit operates in two modes. The startup mode is automatically entered when the motor speed is more than 3% slow. If the target speed is 3600 RPM, startup mode is active when the motor is not turning up through 3492 RPM. When in startup mode, the voltage applied to the spindle transconductance power amplifier is fixed. Linear control mode is entered when the motor speed is greater than 3% slow. When in linear mode, the voltage to the transconductance amplifier is taken from the VIN pin.

The fixed voltage used in startup mode varies between the three components:

DEVICE	STARTUP VOLTAGE
SSI 32M595	2.25V internally supplied
SSI 32M7010	2.25V internally supplied
SSI 32H6820	Taken from VLIM pin

The SSI 32H6820 offers another degree of freedom in choosing the sense resistor. The interaction between the startup command voltage and the current sense resistor allow tradeoffs between the two to best satisfy the dynamic range of the motor operating currents. Alternatively, VLIM may be directly strapped to VBIAS eliminating the need for external components.

PI Speed Control Model

The small signal speed control model is illustrated in Figure 9 below. In this model, the friction term typically represented by the symbol B has been assumed to be zero.

The previous model references the following parameters:

Parameter	
Target speed	377 radians/sec or 3600 RPM
Kp-dac	Proportional error gain
Ki-dac	Integral error gain
Ka	Transconductance gain
Kt	Motor torque constant
J	Motor and load inertia
S	Laplace operator
Kp	Compensator proportional term
Ki	Compensator integral term

The parameters Kp-dac and Ki-dac are speed sensitive and can be computed as follows:

$$K_{p-dac} = \frac{8333 \text{ counts}}{RPS \cdot 2 \cdot \pi \text{ rads}} \cdot .035 \frac{\text{volts}}{\text{counts}}$$

$$= 0.775 \text{ V/rad/sec @ 3600 RPM (60 RPS)}$$

and

$$K_{i\text{-dac}} = \frac{RPS}{4} \cdot K_{p\text{-dac}}$$

$$= 11.6 \text{ V/rad @ 3600 RPM}$$

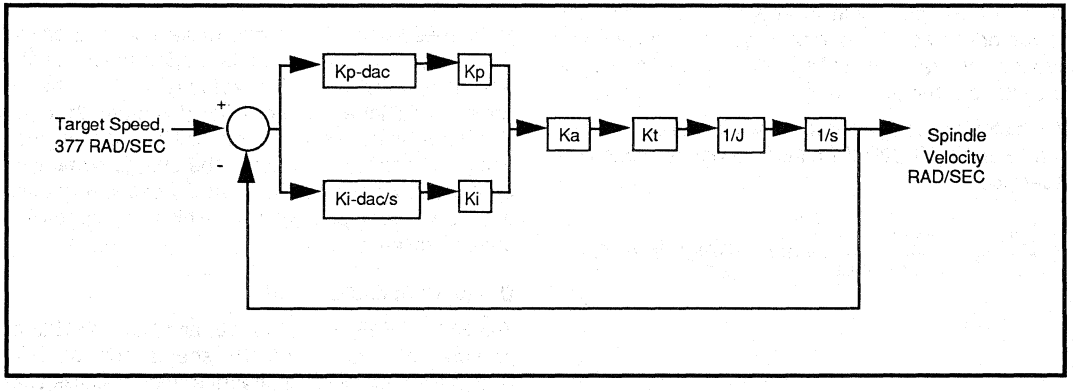


Figure 9. Small Signal Speed Control Model

PI Speed Control Model (continued)

Note that the integral term is taken from the upper 6 bits of an 8-bit digital accumulator which effectively divides the integral gain by 4. The sample rate of the accumulator is in RPS (60 for 3600 RPM) so the factor RPS/4 results.

The Silicon Systems application note titled: Setting Speed Control Loop Compensation Gains, provides a detailed design example based on the model above. The control circuit itself is not purely continuous and by design has a sample rate equal to the revolution rate of the motor. When the target bandwidth is small such as a few hertz, and the target speed is high such as 60 RPS, the model approximates a continuous system fairly well.

Resolution and Tolerance

The resolution of the speed control circuit is entirely determined by the digital clock rate used decrementing the period counter. When SYSCLK is 2 MHz in the SSI 32M7010, the period counter is clocked at 500 kHz. Due to sampling uncertainty, there is an inherent plus or minus one count of error. Since one bit is .012% at 3600 RPM, the total envelope of uncertainty is specified as 0.036%.

Regulation tolerance is a function of the entire system. The resolution of the speed control circuit is very small compared to the system variables such as bearing friction, changes in load such as when seeking, jitter in the speed indicator, and power supply variation. Setting the speed control loop compensation effects the dynamic response to changes in speed and ultimately determines how quickly the loop settles.

Programmable Speed Control

The SSI 32H6820 offers programmable speed control. Register addresses 3 and 4 hold the period counter value which is 15 bits in width. This counter is clocked at 500 kHz just like the SSI 32M595 and SSI 32M7010.

As an example, consider a 12-pole motor intended to run at a target speed of 5400 RPM. In this design example, the following parameters are computed:

$$RPS = \frac{5400}{60} = 90 \text{ revs/sec}$$

$$\tau_{rev} = \frac{1}{RPS} = 11 \frac{\text{ms}}{\text{rev}}$$

$$Count_{total} = \frac{\tau_{rev}}{2 \cdot 10^{-6}} = 5500 \text{ counts}$$

The programmed load count is 6 less than the value found from $Count_{TOTAL}$. This difference of 6 is due to internal digital delays, therefore the final load value is 5494. The bits setting the number of poles are M0 and M1 in register 1 of the SSI 32H6820. For this particular example, set M0=0 and M1=1 for 12 pole operation. The hexadecimal equivalent of 5494 is 1576H. Register 3 should be written with hexadecimal 76H followed by 15H for register 4.

Speed LOCK Indication

The three MSC components supporting internal speed control provide a speed LOCK pin. This indicator is asserted high when the period measurement is within +-15 counts or ±0.2% of the target speed. LOCK can be used as an indicator that the motor has spun up to speed from startup. In has a fairly wide tolerance which minimizes its sensitivity to brief speed error. The falling edge of LOCK could serve as an interrupt source though polling may be better.

Using an External Speed Indicator

Provisions exist in the three MSC devices with internal speed control to accept an external speed indicator. This speed indicator should transition once per indicated revolution. The devices transition to the external signal in slightly different ways:

DEVICE	SELECTION METHOD
SSI 32M595	Assert INDXSEL and apply speed signal to INDX/COMMU pin
SSI 32M7010	Assert INDXSEL and apply speed signal to INDX/COMMU pin
SSI 32H6820	Program INDX_SEL bit in register 0 and apply speed signal to EXT INDX

External speed indication may be attractive in some designs to enhance speed control tolerance. In normal Internal mode, the speed indicator is derived from the BEMF zero crossings. By dividing the zero crossings by the number of commutations per revolution, the same zero crossing is always used. Even so, there may still be some inherent uncertainty in this analog event. By taking a signal from the digital servo timing ASIC in a hard disk drive, the speed indication jitter can be greatly minimized. When an external speed indicator is

Using an External Speed Indicator (continued)

used, BEMF crossings are initially used to spin up and stabilize the motor. Then once LOCK is found, the microprocessor will transition to the external indicator.

Increasing Spindle Bandwidth

The SSI 32H6820 provides programmable speed control. When programmable speed control is used with the external speed indicator, it is possible to change sample rates under microprocessor control. Changing samples rates could be implemented by using the once-per-revolution signal derived from the BEMF zero crossings during spin up and initial speed control; then transition to the external speed indicator with a higher sample rate and corresponding smaller value in the programmable speed count registers. Changing sample rates has the disadvantage of having non-optimum compensation in one of the control modes.

An alternative to changing the sample rate is to externally derive a speed indicator from the commutation event signal REVCOM. This design would divide the REVCOM signal (either REVCLK or COMMU which is programmable) by a value which would correspond to a signal which could be derived from the servo timing ASIC. In this way, spinup and initial lock would be established using a signal actually derived from the BEMF crossings but made to look like the signal which will later be generated from the data head. When speed lock is established, the external speed indicator would be switched to the real head signal. This method would allow more samples per revolution and thus lend itself to higher speed control bandwidths.

SSI 32H6812 Charge Pump and Loop Filter

Only the SSI 32H6812 implements a charge pump and loop filter for speed control. A charge pump consisting of a current source of amplitude proportional to speed error charges or discharges the voltage across the loop filter. A second order discrete filter consisting of two capacitors and a resistor configure the compensation filter.

SSI 32H6812 Speed Control Model

Figure 10 provides a small-signal block diagram of a speed control system based on the SSI 32H6812.

The model below references the following parameters:

Parameter

Target Speed	5400 RPM
Kc	Speed error in counts/rad/sec
Kpmp	Pump circuit in: seconds/count • amp/seconds
H(s)	Impedance of loop filter
Ka	Transconductance gain in amps/volt
Kt/(sJ+B)	Motor model with: Kt - torque constant of motor
	J - inertia of motor/load
	B - friction

These model parameters above are computed as indicated below:

$$K_c = \frac{5555 \text{ counts}}{90 \text{ rev/sec}} \cdot \frac{1 \, rev}{2\pi \text{ rads}} = \frac{5555 \text{ counts}}{180\pi \text{ rad/sec}}$$

and

$$K_{pmp} = \frac{2 * 10^{-6} \text{ sec}}{\text{count}} \cdot \frac{60 \cdot 10^{-6} \text{ amp}}{1/90 \text{ sec}}$$

so that

$$K_{pmp} = 1.08 \cdot 10^{-9} \frac{\text{amp}}{\text{count}}$$

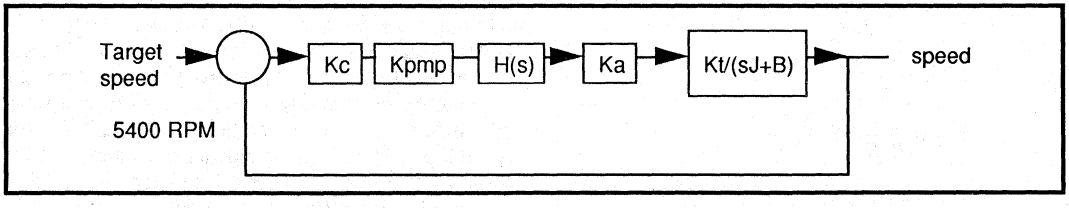


Figure 10. SSI 32H6812 Small Signal Speed Control Model

SSI 32H6812 Speed Control Model (continued)

The transconductance gain of the power amplifier is determined by both the sense resistor and sense amplifier gain setting programmed through the serial interface. Sense amplifier gain settings of 5,10, 20, and 30 are programmable. The power amplifier gain is computed from:

$$K_a = \frac{1}{G \cdot Rs}$$

where G is the sense amplifier gain and Rs is the sense resistor.

Loop Filter

The loop filter presents an impedance through which the charge pump current source is forced. Figure 11 illustrates the components making up this filter.

The voltage developed across this filter serves as the current command amplified by the transconductance power amplifier. H(s) is found to be:

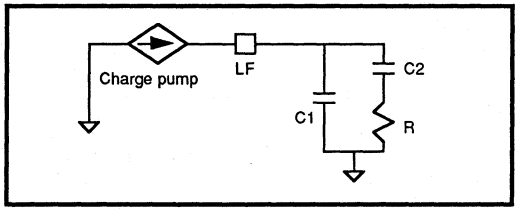


Figure 11. Loop Filter

$$H(s) = \frac{1}{C1 + C2} \cdot \frac{s\tau + 1}{s(sk\tau + 1)}$$

where

$$\tau = R \cdot C2 \qquad \text{and} \qquad k = \frac{C1}{C1 + C2}$$

The transfer function offers a "pole" at the origin which provides the integration necessary to implement a type 1 system. The numerator of H(s) provides the "zero" which is adjusted to achieve necessary phase margin. The parameter k will always be less than 1 so that the pole time-constant in the denominator will less than the zero. The corner frequencies determined by k and τ are:

$$f_z = \frac{1}{2\pi\tau} \text{ and } f_p = \frac{1}{2\pi k\tau}$$

Design Example

In a particular application, the filter components were chosen as follows:

R = 300 K

C1 = 0.1 µFd

C2 = 1.0 µFd

which yielded corner frequencies of:

fz = 0.5 Hz and fp = 5.8 Hz.

For this particular example, the constant parameters were lumped together forming a term "g" below and the friction B was assumed to be zero.

g = kc • kp • ki • ka • (kt/J)

$g = 7.345 \cdot 10^{-5}$

The modeled open-loop gain was plotted below where GH(s) was defined to be:

GH(s) = g • H(s)

From the open-loop gain plots, the 0db cross-over frequency for this particular example is approximately three hertz while the phase margin is approximately 53 degrees.

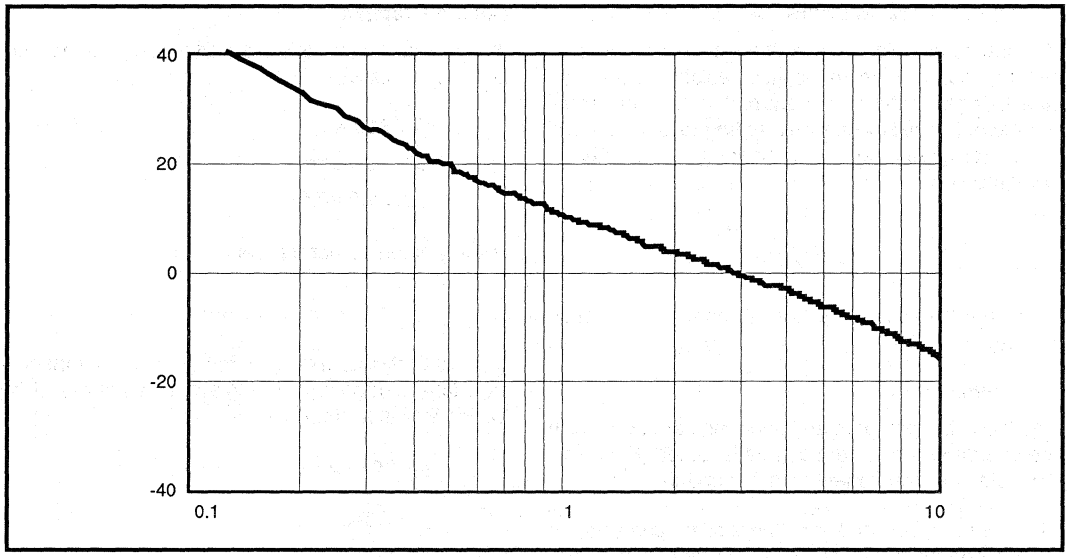


Figure 12. GH(s) Open Loop Gain Plot

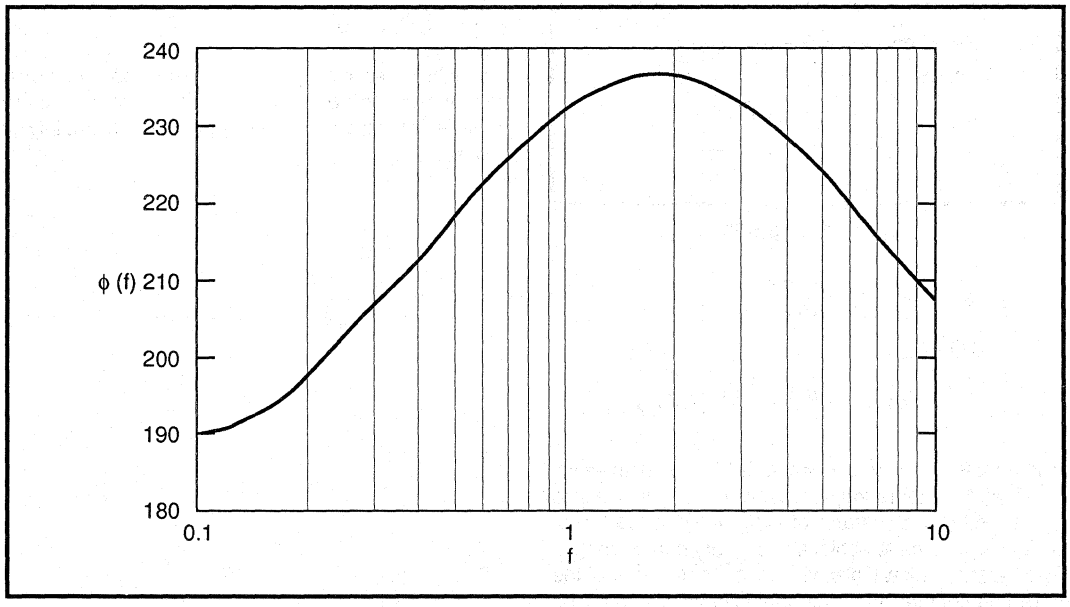


Figure 13. Open Loop Phase Plot

External Speed Control

When motor speed is externally controlled, the MSC component is responsible only for commutating and providing a transconductance amplifier for motor current control. The control signal itself is externally generated by some device designed to compare actual speed with the target speed and generate a compensating current command to make the necessary speed correction.

This section provides two digital speed control design examples. The first is implemented using the Silicon Systems digital signal processor named the SSI 32H6830 SEEKER®. The second is based on an 80C51 microcontroller. It is natural to implement speed control with a microprocessor or DSP since the startup method discussed earlier relies upon an external digital device.

Digital Design Approach

This design example approaches the problem in the following steps:

1. System operation specifications
2. Characterize the uncompensated system
3. Compute compensation to satisfy system specification
4. Implement speed control algorithm
5. Evaluate system performance

System Operating Specification

The system operating specification consists primarily of rise time, settling time, and percentage overshoot design goals. Various techniques and approximations exist for translating these transient system specifications into the frequency domain such that the open-loop phase and gain margins can be specified.

Characterize The Uncompensated System

This design example will employ a PI compensator. Both proportional and integral error components will be generated and then summed together to form a composite correction current command. This speed control compensation is determined by two gain terms identified as Kp and Ki denoting the proportional and integral gains. These gains are chosen by analyzing the Bode plot of the uncompensated system and choosing values such that the compensated system will meet the target specifications.

Digital Speed Control Model

The small signal digital speed control model is illustrated in Figure 14 below. The motor friction term typically referenced by the symbol B is assumed to be zero.

The open loop transfer function for this model is found to be:

$$T(s) = K_{tach} \cdot (K_p + \frac{K_i}{s}) \cdot K_{dac} \cdot K_a \cdot \frac{K_T}{J_\theta} \cdot \frac{1}{s}$$

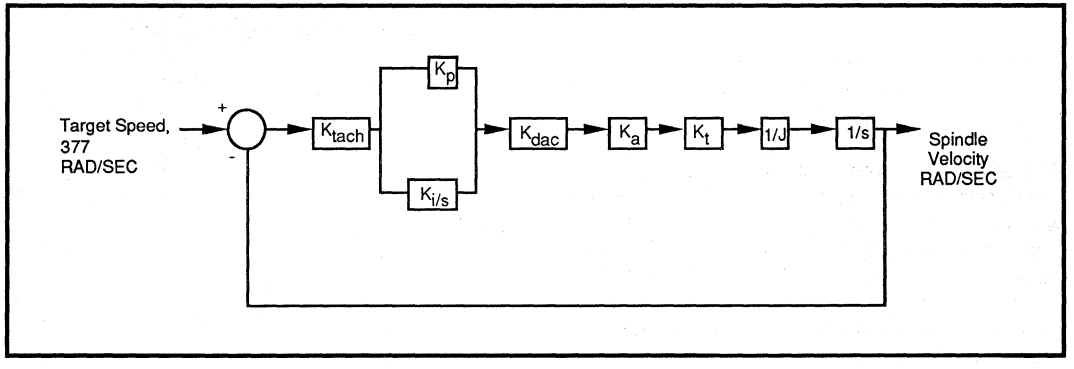


Figure 14. Small Signal Digital Speed Control Model

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Digital Speed Control Model (ontinued)

In the transfer function T(s) above, some parameters are more difficult to determine than others. The ratio K_t/J is dependent upon the motor and load conditions; K_{tach}, K_a, and K_{dac} are electrical and are easily determined. This particular design approach lumps all these factors together through characterization so that individual parameter specification is not necessary. This approach is therefore somewhat empirical and requires the uncompensated system to exist and be characterized.

System Characterization

System characterization is made possible by breaking the uncompensated control loop with the circuit shown in Figure 15. This popular technique allows the uncompensated system to continue operating while a disturbance signal is added for system evaluation. Note that the magnitude and phase of the error signal is unaltered and is summed with an external disturbance. The system open loop gain GH is found as the ratio below:

$$GH = \frac{\text{Error Signal}}{VIN}$$

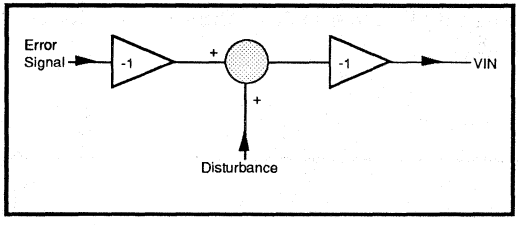

Figure 15. Breaking the Loop for Open Loop Gain Testing

The uncompensated system is characterized by introducing a disturbance signal with a magnitude which is small such as 10% of the steady state error signal, and sweeping the disturbance over a suitable range such as 100 mHz to 10Hz. The idea is to select values for Kp and Ki so that at the compensated open-loop gain crossover frequency, the loop gain is equal to 1.0 (0 dB) with the required phase margin. A Bode magnitude plot of the uncompensated open-loop response will indicate how much gain must be added to reach the desired crossover frequency. Examination of the phase plot indicates the necessary phase shift to achieve the specified phase margin.

Set K_p to 1 and K_i to 0 to obtain the uncompensated system response. In some cases, it is necessary to have more gain in the loop for stable and sufficient uncompensated operation. In these low gain cases, increase K_p as necessary but maintain K_i at 0. Use the test value for Kp as reference, and compute the required change in gain relative to this reference.

Computing Compensation

The PI compensator is:

$$K_p + \frac{K_i}{j\omega} = \frac{(j\omega \cdot K_p + K_i)}{j\omega}$$

From the uncompensated open-loop Bode plots, the necessary compensator gain and phase shift can be determined. Equating this gain Av and phase shift Θ to the compensator elements yields two conditions:

Condition 1

$$|A_v| = \sqrt{K_p^{\,2} + \left(K_i/\omega\right)^2}$$

Condition 2

$$\Theta = \text{Tan}^{-1}\left(\frac{\omega \cdot K_p}{K_i}\right) - 90 \text{ degrees}$$

Rearranging each condition so that solutions for K_p and K_i are found yields the design equations:

$$K_p = \sqrt{\frac{A_v^{\,2}}{\left(1 + \frac{1}{\text{Tan}^2(\Theta + 90)}\right)}}$$

and

$$K_i = \frac{\omega \cdot K_p}{\text{Tan}(\Theta + 90)}$$

Design Example

This PI compensation method is illustrated in the following example. The compensation method is digitally implemented with a sample rate of 78 Hz. The sample rate is important when computing the real value of K_i as will be shown later.

The motor and load system was characterized by sweeping the disturbance over the frequency range of 100 mHz to 10 Hz. The value of K_p was set to one. Figure 16 shows the uncompensated open loop response. Note that zero degrees on the plot is actually 180 degrees phase delay. This means that actual phase shift is 180-76.65 or 103.35 degrees at 2 Hz

For a 2 Hz cross-over frequency, we require 25.5 dB (18.33 V/V) of Av gain. Choosing a design goal of 45 degrees of phase margin, the compensator phase shift will need to add an additional phase shift of:

$$\theta = 135\text{-}103.35 \text{ or } 31.65 \text{ degrees.}$$

Applying the design equations for K_p and K_i yield:

$$K_p = \sqrt{\frac{18.33^2}{\left(1+\frac{1}{\text{Tan}^2(90-31.65)}\right)}} = 15.6$$

and

$$K_i = \frac{2 \cdot 2\pi \cdot 15.6}{\text{Tan}(90 - 31.65)} = 120.8$$

The values for K_i and K_p are represented in digital format as 16-bit, fixed-point binary code. In the SSI 32H6830 SEEKER® DSP, K_p will be represented as 7CCC hexadecimal where the decimal point is between bits 11 and 10 (considering the LSB as bit 0 and the MSB as bit 15). This decimal point placement is achieved in the SEEKER® by using the RADIX instruction with an argument of 4. Effectively, the RADIX 4 instruction informs the multiplier to treat Kp as a signed number with a range of ± 16. The binary representation is found as follows:

$$representation = \frac{\text{value of constant}}{\text{full scale range}} \cdot 2^{bits-1}$$

For K_p, the representation is found using the equation above to be:

$$31948 = \frac{15.6}{16} \cdot 2^{16-1} \text{ which is 07CCCH}$$

The value for K_i must be further processed by taking into account the update rate of the digital integrator. The computed value of K_i must be divided by the sample rate yielding:

$$K_{i_{real}} = \frac{K_i}{F_{sample}} \text{ where } F_{sample} \text{ is the sample rate}$$

so that

$$K_{i_{real}} = \frac{120.8}{78} = 1.55$$

Representing K_i in hexadecimal using the RADIX 4 instruction yields a hexadecimal value of 0C66H.

With the computed compensation, the open-loop system performance was evaluated and is plotted in Figure 17. As the plot indicates, the gain and phase-margin are very near the design targets. Since the sample rate to bandwidth ratio is 36 in this example, the digital compensator is a fair approximation of a continuous time solution. Errors between the target and actual performance can be traced to the digital compensator sampling effect introduced by the use of the numerical integration "backward" rule, fixed point computational limitations, and system noise.

Speed Control Algorithm Difference Equation

The digital compensator implemented in this example was derived by applying the backward rule as an approximation of H(s) by H(z):

$$s \Leftarrow \frac{z-1}{T \cdot z} \text{ where T is the sample period}$$

This translates:

$$H(s) = K_p + \frac{K_{\text{int}}}{s} \text{ into } H(z) = K_p + K_{\text{int}} \frac{T \cdot z}{z-1}$$

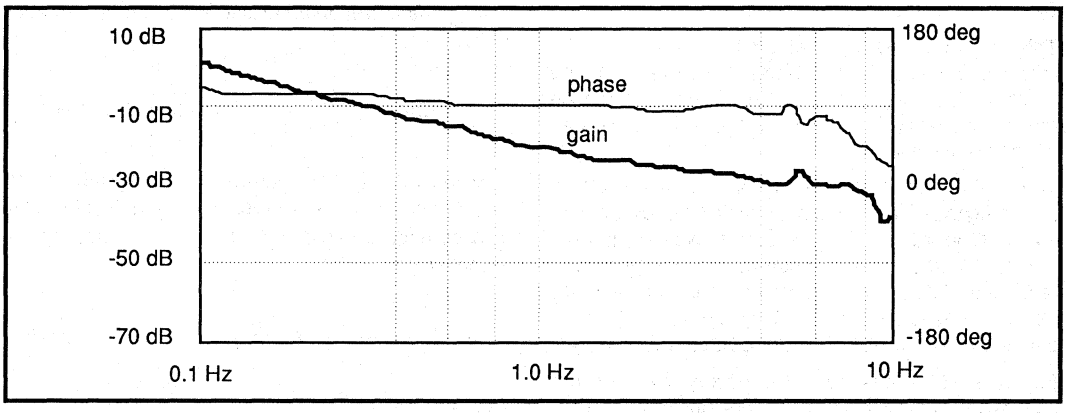

Figure 16. Uncompensated Open-Loop

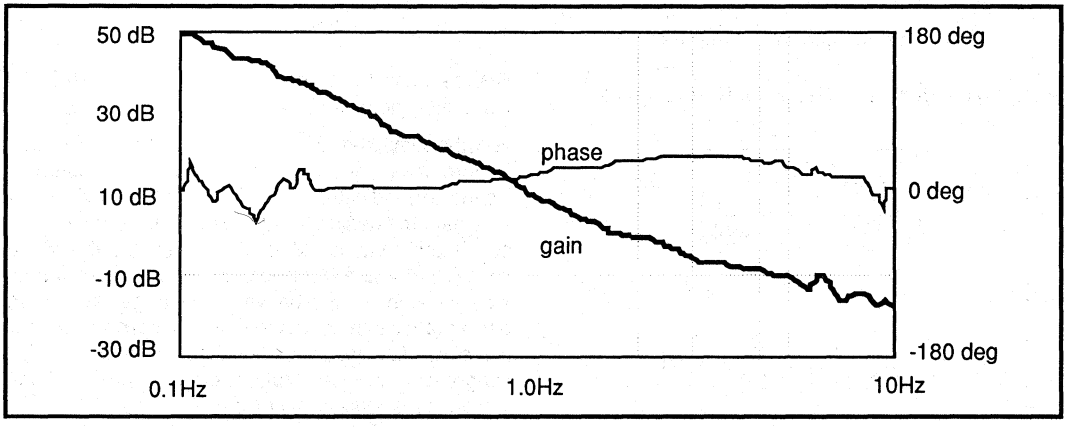

Figure 17. Compensated Open-Loop

Rearranging so that the z terms appear as powers of -1 yields:

$$H(z) = K_p + K_i \frac{1}{1 - z^{-1}}$$

where K_i above is the "real" K_i computed earlier as Kireal which is the same as Kint multiplied by T.

Expanding H(z) yields:

$$H(z) = \frac{Y(z)}{X(z)} = K_p \frac{1 - z^{-1} + K_i / K_p}{1 - z^{-1}}$$

and solving for y[k] in the time domain by recognizing that z^{-1} is the z domain delay operator as in:

$$Y[z] \Rightarrow y[k]$$

and

$$Y[z] \cdot z^{-1} \Rightarrow y[k-1]$$

finally yielding the difference equation:

$$y[k] = K_p \cdot \{x[k] - x[k-1]\} + K_i \cdot x[k] + y[k-1]$$

SEEKER® PI Code Example

The SEEKER® firmware used for the example digital speed control compensator is given in listing 2. This firmware runs on an SSI 32H6830 SEEKER® DSP. The SEEKER® has an instruction execution time of 50 ns except for the multiplier which completes in 200 ns. The device has separate ALU and multiplier functional units so in some instances, a NOP is required to synchronize internal pipeline delays and data flow. There are no immediate memory operations, all constants come from data RAM. The data RAM is 16-bits wide while the instructions have short 10-bit and long 20-bit forms.

Data references are both to general purpose RAM and to special functions. General purpose RAM references include those that are variable and those that are constant. Constants are just variables which don't change. LIMIT is an example of a constant while E0 is a variable. The reference "pTime" is a special function register which measures the period of one revolution with a bit resolution of 1.6 µs. DAC2 is the reference name for the 2's complement 10-bit DAC used to command motor current.

Listing 2. SEEKER® Speed Control

```
SPEED_SAMPLE:           ;Entry point to speed control firmware
                        ;The example sample rate was 78 Hz

        LD pTime /F1    ;Read period counter and put MSB into F1
        NOP             ;pipeline delay unique to the SEEKER
        JF OVERFLOW /F1 ;branch if period is 8000H for overflow
        JMP GETERROR    ;no overflow, compute speed error

OVERFLOW:               ;limit period counter to max pos number
        LD.L MOSTPOS    ;MOSTPOS is data location with 7FFF


GETERROR:               ;accumulator has valid period error now

        SUB.L TGTSPEED  ;e(k) = revolution period - target period
        NOP
        Sto E0 /f2      ;save e(k) in variable E0, sample MSB
                        ;and put sign of error into F2

; Perform switch based on speed error.  If too slow, assert
; maximum DAC voltage for maximum motor current command
; Also, reset integrator.  If above this minimum speed threshold,
; operate in linear control mode.

; Note that F2 holds the sign of speed error e(k). If F2 is
; true, then e(k) is negative and the motor is too fast.

        JF LIN_MODE /F2 ;If too fast, stay in linear mode
                        ;and slow down by friction

; Otherwise, e(k) is positive, compare to switch threshold
        SUB LOW_SPEED /F1  ; LOW_SPEED is the threshold to switch
        NOP
        JF LIN_MODE /F1 ;Above the minimum speed so use
                        ;linear control
```

Listing 2. SEEKER® Speed Control (continued)

```
; Force the DAC to most positive value when too slow
        LD MOSTPOS
        STODR DAC2      ;Copy directly to the MSC DAC
        STOP            ;Work all done, wait for next sample

; Linear mode velocity error computation
LIN_MODE:
        ld E0           ;Get error e(k)
        Sub.l E1        ;Compute e(k)-e(k-1)
        nop
        Sto.l Error     ;Save value in temp location for multiply

        Radix 4         ;Select RADIX 4 in Kp or Ki representation
        Mld Error Kp    ;Compute Kp(e(k)-e(k-1))
        Madd E0 Ki      ;Compute Kp(e(k)-e(k-1))+Ki*e(k)
        Stodr E1        ;Overlap Madd by updating e(k-1)=e(k)
        Add.l Y1        ;Y(k)=Kp(e(k)-e(k-1))+Ki*e(k)+Y(k-1)
        nop
        Stosat Y1 /F2   ;Update Y(k-1), use saturation, F2 is sign

        Ld Y1           ;Load saturated version of correction Y(k)

; Map the computed result to the 10 bit DAC, perform limiting
        JF CheckDwn /F2 ;If negative, check if too negative
        JMP CheckTop    ;Else check if too positive
        nop

CheckDwn:               ;Test is too negative
        add LIMIT       ;LIMIT is a variable fixed at 512
        nop
        JF fixbottom /F2;Too negative so limit at -512
        Jmp output      ;Value is ok, output as is
        nop
FixBottom:
        ld.l MOSTNEG    ;MOSTNEG is a constant of 8000H
        stodr dac2      ;Output limited value to DAC
        Stop            ;Work all done, wait for next sample

CheckTop:               ;Test if too positive
        sub.l LIMIT     ;LIMIT is a variable fixed at 512
        nop
        jf Output /F2   ;Value is OK, output as is
        jmp FixTop      ;Too positive, limit at +512
FixTop:
       ld MOSTPOS       ;MOSTPOS is constant of 7FFF
       stodr Dac2       ;Output limited value to DAC
       Stop             ;Work all done, wait for next sample
Output:                 ;Output the error command to DAC
        Lds Tmp /shl=6  ;Shift result up to map into 10 bit DAC
        nop
        stosat DAC2     ;Write to DAC using saturation

        STOP            ;Work all done, wait for next sample
```

"C" Code Speed Control Example

This section provides a "C" language speed control example which is called by the assembly language REV_INT interrupt handler in listing 1. This speed control example was implemented on an 80C51 microcontroller supporting an SSI 32H6811.

Listing 3. Speed Control

```
// Definitions and explanations concerning constants used later:

// At 8 MHz, REVCNT period should be 7407 counts for 5400 RPM,
// minus 10 counts for interrupt handler overhead */
#define TARGET (7407 - 10) // This is the target compared later
                           // to the measurement in REVCNT var

#define KP ((signed char)85) // PI coefficents
#define KI ((signed char)36)

#define USEC(a) ((unsigned int)((a)/1.5))  // uS -> int val
#define abs(a) (((a)>0) ? (a) : -(a))  // absolute value



// The following include <reg addr> <111-servo select> <0-write>
#define VCM 0x0e  /* VCM DAC is reg 0*/
#define MSC 0x1e  /* MSC DAC is reg 1*/
#define MODE 0x2e /* MODE register is reg 2*/

// bit masks used in C code below
#define REV 0x8000  // COM/REV* bit is 1 for REVCLK
#define M_SHIFT 12  // shift code to access M bit field
#define N_SHIFT 10  // shift code to access N bit field
#define DAC_SHIFT 6 // shift code to access both DAC fields
#define GAIN_30 0       // code for sense gain of 30
#define GAIN_20 0x80    // code for sense gain of 20
#define GAIN_10 0x100   // code for sense gain of 10
#define GAIN_5 0x180    // code for sense gain of 5
#define UNI 0x200     // code enabling unipolar mode
#define SWON 0x40     // code turning on analog switch

/* sys_status flags [routine responsible for setting/clearing] */
#define MOTOR_RUN 0x01  /* motor should be running
                           [start_motor,brake_motor] */
#define MOTOR_START     0x02  /* motor starting [start_motor] */
#define MOTOR_STALL     0x04  /* [watchdog interrupt] */
#define MOTOR_RACE      0x08  /* motor racing (probably stalled
                                 and oscillating) */
#define MOTOR_LOCK      0x10  /* motor speed within 15.55 RPM
                                 of target */
```

Listing 3. Speed Control (continued)

```
// Maximum period error for motor lock is 32 uSec (15.55 RPM)
#define LOCK USEC(32)       // macro used to return int for 32uS

// Implement  y1=kp(x1-x0)+ki(x1)+y0

signed char x0; // x0 is previous error, x1 is current error
short int y0;   // previous correction, y1 is next correction

void speed_control(void)
{
/* Called by REV_INT interrupt handler servicing REVCLK.
   Mustn't do anything that depends upon interrupts being enabled!
   Because interrupts are disabled during this functions
   execution, we can save time by manipulating sys_status
   directly. */

long int t;        // used to check if period is too long
short int x1;      // x1 is current error
short int y1;      // next correction to be computed below

/* compute period error */
t = ((unsigned short)revcnt - TARGET);

x1 = (t > 32767) ? 32767 : t;  // limit error to 16 bits

/* check for speed lock */
if(abs(x1) < LOCK)
  {  // Yes, in lock
  sys_status |= MOTOR_LOCK;
  }
else
  {  // No, out of lock
  sys_status &= ~MOTOR_LOCK;
  }

/* at 8 MHz, REVCNT period should be 7407 counts for 5400 RPM,   /* calculate
compensator output */

/* saturate output when we are far from being locked */
if(abs(x1) < 63)
  {  // linear region so compute correction
  // In this particular implementation, scaling has been
  // implemented for numerical reasons.  The shifting
  // below is part of this scaling along with lumped
  // scaling in Kp and Ki factors below:
  y1 = (KP*((signed char)x1 - x0) + KI*x1 + (y0<<4))>>4;

  // saturate correction value
  if(y1 > 511)
    y1 = 511;  // 10 bit DAC positive limit

  if(y1 < -512)
    y1 = -512;  // 10 bit DAC negative limit
  x0 = x1;      // update previous error term

  // In this particular example, the run gain must be 10
  send_packet(MODE | REV | GAIN_10 | (1<<N_SHIFT));
```

```
  }
else
  {  // error too large so saturate as needed
  if(x1 > 0)
    {  // much too slow, apply maximum positive correction
    y1 = 511;
    x0 = 63;
    }
  else
    {  // much too fast, apply minimum correction
    y1 = -512;
    x0 = -64;
    }
  send_packet(MODE | REV | GAIN_5 | (1<<N_SHIFT));
  }

/* update the DAC */
send_packet(MSC | (y1 << DAC_SHIFT));
y0 = y1;  // update previous correction term
}
```

Disabling On-Chip Control

For the devices having internal digital PI speed control such as the SSI 32M595, SSI 32M7010, and SSI 32H6820 an automatic switch is made from startup mode into linear control. This modal switch is based on the motor being within 3% of the target speed. In all devices, this switching can be defeated by fooling the component. This can be performed by selecting external speed indication mode and providing a signal at the INDX pin such as SYSCLK itself. With the switch mode disabled in this way, the VIN pin will always be selected as the command for motor current.

RETRACT AND BRAKING THE MOTOR

In hard disk drives, the spindle driver is responsible for providing voltage to the positioner during power fault. This voltage is necessary so that the positioner can implement a head retraction. The voltage from the spindle is full-wave rectified and presented to Silicon Systems components at the VBEMF pin.

BEMF generation

BEMF voltage is full-wave rectified by the spindle driver. In designs using external power MOSFETs, kick-back protection diodes inherent in P/N channel MOSFETs can be used to perform this function. The lower N channel diode routes current from ground, through the sense resistor, through the diode, and back into the negative going motor winding. The upper P channel diode connects the positive going motor winding to the VBEMF point. This VBEMF source now powers the positioner motor by acting as a voltage source while the spindle motor free spins using the generator action of the motor itself. Figure 18 illustrates this function.

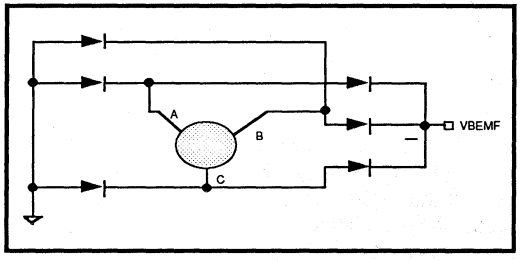

Figure 18. Generation of VBEMF for Retract

In integrated power devices like the SSI 32H6810A, the spindle drivers are stacked N channel MOSFETs. The lower diodes are built into the package. It is necessary to add three external diodes from each motor terminal to the common VBEMF point. The upper N channel MOSFET in the Silicon Systems components do not have the parasitic diode always found across P channel drivers. This design eliminates the need for blocking diodes as well.

In most designs, the diodes in the SSI 32H6810A or external MOSFET drivers will be sufficient. If the drop across them is too great, however; it may be necessary to add Schottky diodes in parallel with the integrated diodes. It may be beneficial to connect the motor windings to VBEMF with Schottky diodes.

Blocking Diodes

A blocking diode is necessary only when external MOSFET drivers are used. This need arises from the fact that the upper P channel MOSFET has an inherent parasitic diode. This upper diode can be used to complete the set necessary for full-wave rectification of spindle motor but only when the cathodes of these diodes are isolated from the power supply. For this reason, a "blocking" diode isolates the power supply (which will be dropping) from the VBEMF point. This has the disadvantage of requiring a component and reducing the voltage available to the spindle motor by the drop across one diode. Figure 3 shows the blocking diode and how it isolates VBEMF from the supply voltage.

Dynamic Braking and Free Spin

Most MSC family components have a controlled brake feature; the SSI 32H6812 does not. This feature allows the MSC operation to behave in two ways in response to a power failure. These modes of operation are determined by the voltage on the $\overline{\text{BRAKE}}$ pin. When $\overline{\text{BRAKE}}$ is above a voltage threshold, the spindle motor will free-spin during power fault. When the $\overline{\text{BRAKE}}$ voltage is below this threshold, the circuit will dynamically brake the motor. Figure 19 illustrates this bimodal braking operation.

This braking feature is intended to be used with an external RC network which provides a programmable free spin to brake delay. If an RC network is connected so that the resistor is from $\overline{\text{SYSRST}}$ (an open drain reset signal available on Silicon Systems' positioner components) to $\overline{\text{BRAKE}}$, and a capacitor connects $\overline{\text{BRAKE}}$ to ground, then the time taken for the brake capacitor voltage to decay below the threshold determines the free spin delay.

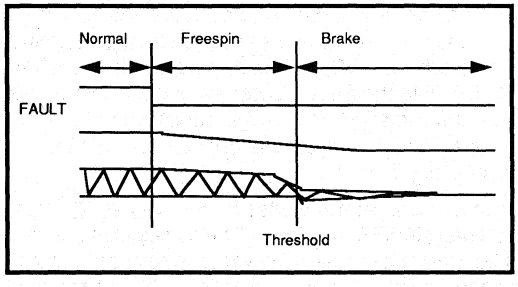

Figure 19. Bimodal Braking Operation

POWER DISSIPATION CURVES

Data sheets for Silicon Systems' devices with integrated power drivers for spindle or servo motors have typically specified drive capability in two ways. These two drive specifications are "ABSOLUTE MAXIMUM RATING" and "RECOMMENDED OPERATING CONDITIONS." The absolute maximum rating is a maximum current such as 1A beyond which the component may be damaged. The recommended operating condition is intended to suggest a typical current amplitude. In fact, the recommended operating condition is of very little use since it does not reflect power dissipation versus time. A spindle motor draws considerable current when starting then drops off while running. Silicon Systems is now providing power dissipation curves for many of its integrated power devices. Power dissipation curves provide answers to "how much current can the device deliver" based on the time duration and ambient temperature expected.

In any application, power will be dissipated in the motor loads, the sense resistors, and the drivers. Figure 20 illustrates the approximate power dissipation curves for the SSI 32H6810A (this figure is only an approximation, please request the full page plot for actual analysis). The vertical axis of the power curves is power dissipation in watts inside the SSI 32H6810A only. The horizontal axis is ambient temperature. The power curves consist of a family of individual test conditions; each test condition represents a different time duration of power dissipation.

In a hard-disk drive, power dissipation is not constant. The power dissipation during startup is greatest and then drops to a fairly small constant value while running. The VCM dissipation is very much dependent upon seek activity and is usually very small while track following. Because of the differences in power dissipation based on operating conditions, it is best to isolate operation into particular modes. Example modes are listed in the following:

Operating Modes

MODE	CONDITION
Startup	Peak 1A start current, dissipation primarily in spindle driver resistance for a few seconds
Seek	Small spindle run current typically 100 mA along with peak VCM currents possibly as high as 500 mA
Track	Small spindle run current ypically 100 mA along with small VCM currents varying in time typically with average of 50 mA (measured at IVVMP pin)
Fault	Retract current holding VCM in position and typically under 50 mA

Operating mode power dissipation can be computed using the simple equation:

$$P = I^2 \cdot R$$

where P is power, I is current, and R is resistance. For each mode, power dissipation can be computed (not counting the worst case 100 mW dissipation in other circuits such as bandgap, digital, and misc analog) as tabularized in the example below for spindle resistance of 1.7 and VCM resistance of 2.5Ω:

MODE	DISSIPATION
Startup	1.7 watts ($1^2 \cdot 1.7$)
Seek	642 mW [$(0.1^2 \cdot 1.7)+(0.5^2 \cdot 2.5)$]
Track	23 mW [$(0.1^2 \cdot 1.7)+(0.05^2 \cdot 2.5)$]
Fault	6 mW

Clearly in this example, startup is the most demanding operating mode. Looking at the power curves in Figure 20 show that the startup conditions can't be asserted indefinitely since the infinity curve intersects the vertical axis at less than 1.7 watts. The ten-second duration curve is very near 1.7 watts but this plot does not give sufficient resolution to precisely determine where its intersection is. The two-second curve intersects at approximately five watts and is well above 1.7 watts through 90°C. The plots show that the peak start current of 1A can be dissipated for nearly 10 seconds without triggering the over-temperature shut-down circuit. Seeking is an application sensitive activity; even so, the power curves indicate that the drive could seek indefinitely out to an ambient temperature of 60 or 70°C.

Many data sheets may not yet include power curve information. Please contact Silicon Systems' Servo/MSC applications for this information if you don't already have it.

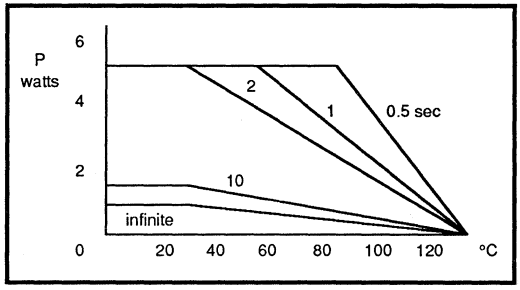

Figure 20. Power Dissipation Curves

Notes:

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Snubbing Network Design for Spindle Motors

Silicon Systems 32M595, 32H4631

Application Note

The use of an RC snubber network placed across each winding of a three-phase brushless motor may be beneficial in reducing the switching EMF and acoustic noise of the motor. Further, use of the snubber is generally required when applying the SSI 32M595 or 32H4631 in systems using 12 volt unipolar (HALF-WAVE) drive modes. Use of snubbers in the unipolar drive mode reduces the amplitude of the switching transients which can be as large as 20 volts. When the individual motor phase and snubber circuit is considered as a simple L-R-C circuit, the following design approach may be taken to compute the necessary snubber R and C values.

1. **Determine the necessary time constant for the network.**
   The motor circuit and the snubbing network to be added will be designed so as to create a second order exponentially decaying step response. The remaining amplitude should be a small value at the time the next commutation zero crossing is expected to occur. Since the zero crossing occurs roughly 1/2 of a commutation cell period after commutation occurs (due to the chip intentional commutation delay), one can calculate the allowable time for the decay and specify the snubbing network by following through this example:

   a. Peak amplitude of transient is 12 volts (12 volt UNIPOLAR)
   b. Die down to 1/1000 of initial transient in 1/2 commutation cell period. This will result in 12 mV remaining. The remaining transient voltage can alter the commutation angle. In a typical unipolar application with a K_t (torque constant) of 3.5 oz-in/Amp the magnitude of the BEMF signal used for commutation when at speed (assumes 3600 RPM) is 9.3 volts peak. The amount of commutation shift, or jitter due to residual transient voltage in degrees of electrical angle is:

   $$Angle_{shift} = \pm [SIN^{-1} (.012/9.3)] = .074°$$

   Which is, of course, negligible.
   c. Decay period (1/2 the commutation cell time) is 694 µsec for a 4-pole motor at 3600 RPM.
   d. Motor inductance is 3.5 mH, resistance is 7Ω, and torque constant, K_t, is 3.5 oz-in/Amp. Knowing that the transient dies down exponentially as:

   $$v = e^{(-t/\tau)}$$

   Where τ denotes the time constant of the motor and snubber circuit and t is the time allowed for this decay to occur. We can solve for the necessary $-(t/\tau)$ by:

   $$Log_e(1/1000) = -6.908$$

   and since $t/\tau = 6.908$, and t=694 µsec, then τ = 694e-6 ÷ 6.908, which equals 100.5 µsec.

2. **Computing the required snubbing capacitor.**
   The motor and snubber circuit equivalent circuit is shown in Figure 1.
   Solving for the transient response at

   $$v = \frac{RCS + 1}{L_m C S^2 + (R_m + R)C S + 1}$$

   Where: $L_m C = 1/w_\eta^2$, and w_η is the natural frequency in radians, and $(R_m + R)C = 2\zeta/w_\eta$, and ζ is the damping constant of the second order characteristic equation which defines the time constant,

   $$\tau = 1/(\zeta w_\eta).$$

   When critical damping is desired, as it is now, τ reduces to $1/w_\eta$.
   In our example τ is 100.5e-6 sec, and in the calculation $L_m \times C = 1/w_\eta^2$, therefore to calculate C when L_m is known:

   $$C = \tau^2 / L_m .$$

   In the example L_m is 3.5 mH, therefore $C = (100.5e-6)^2 / 3.5e-3$

   $$C = 2.89\ \mu Fd$$

Snubbing Network Design for Spindle Motors

Silicon Systems 32M595, 32H4631

3. **Computing the resistor.**
The total resistance in the circuit determines the damping factor. The characteristic equation has (R_m + R) x C equaling 2 times the damping factor divided by the natural frequency, w_η. The total resistance for a damping factor of 1 (critical damping is desired) is: $R_{(total)} = (2 \times \tau)/C$

$$R_{(total)} = (2 \times 100.5e\text{-}6)/2.89e\text{-}6$$

$$R_{(total)} = 69.7\Omega.$$

To find R (the snubbing resistor) the motor resistance is subtracted from the total resistance just calculated:

69.7 - R_m(which is 7Ω), therefore:

$$R = 62.7\Omega.$$

Summary

This approach can be iterated to result in a more common snubbing capacitor value by changing the target time constant. Too much snubbing will cause a shift in the zero crossing time resulting in poorer motor performance. Further, the snubber may result in some noticeable power and torque loss, but using this approach generally will yield good working values.

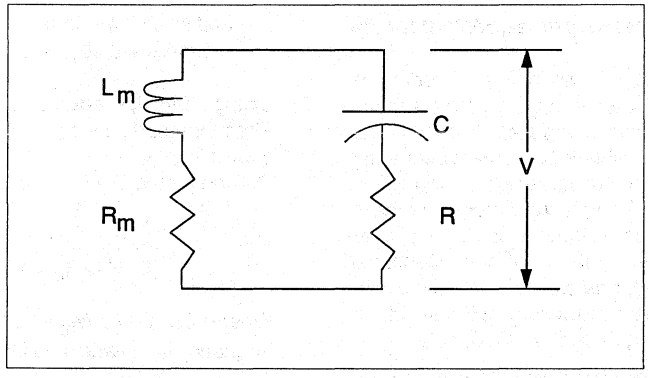

Figure 1: Motor and Snubber Circuit Equivalent Circuit

Setting Speed Control Loop Compensation Gains

Application Note

The speed control compensation is controlled by two gain terms K_p and K_i, the proportional and integral gains. These gains are set by the selection of two resistors. This document presents a method of determining those two gains and then the resistor values. The derivation of the gains will be shown by using the linearized block diagram and the transfer function obtained from that simplification. The amount of error that this will introduce due to the speed control being a sampled system is within tolerable limits at most bandwidths necessary for disk drive spindle applications. Of course the presentation of this method does not try to indicate this is the only way these gains may be determined, or even the best way. It is one method only and the user may elect another method that will best suit his needs.

The simplified, linearized block diagram is seen in Figure 1; the derivation of the open loop transfer function is shown.

This is where:

K_A is the transconductance gain of the driver circuit which is a function of R_{sense} (see the respective part data sheet).

K_T is the motor torque constant. Use units that are compatible with J such as oz-in/Amp and oz-in-sec^2, or newton-meters/Amp & Kilogram-meters^2.

J is the load rotating inertia. Use units that are compatible with K_T.

S is the Laplace operator.

K_p is the proportional gain calculated.

K_i is the integral gain calculated.

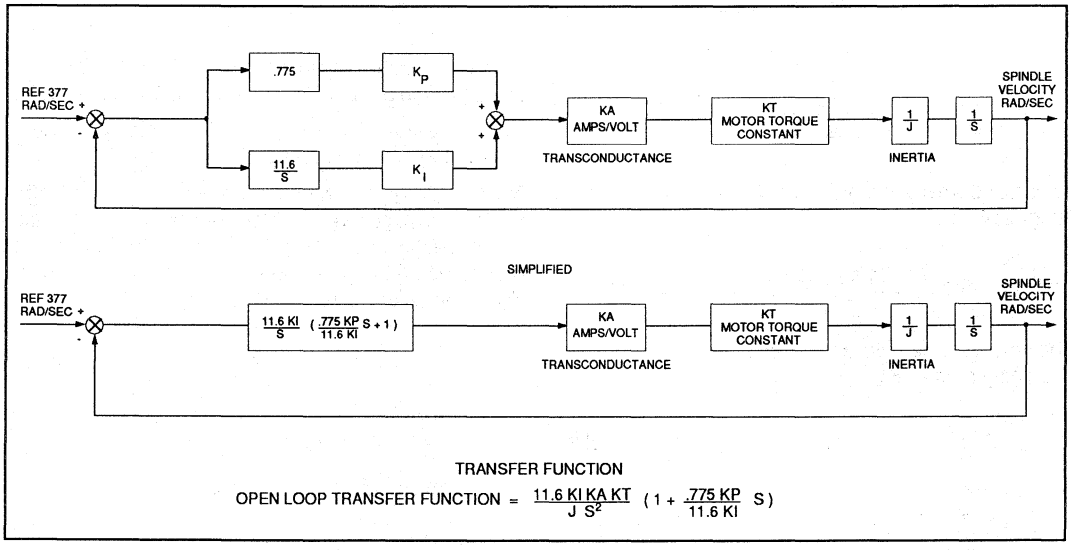

FIGURE 1: Motor Speed Control Linearized Block Diagram

Setting Speed Control Loop Compensation Gains

From the open loop transfer function the loop gain is:

$$LG = \frac{11.6\ K_i K_A K_T}{J\ S^2}\ (1 + \frac{.775\ K_P}{11.6\ K_i}\ S)$$

This can be expanded to:

$$LG = \frac{11.6\ K_i K_A K_T}{J\ S^2} + \frac{K_A K_T\ .775\ K_P}{J\ S}$$

The problem is to select values for K_p and K_i that will allow the loop gain to come to 1.0 (0 dB) at the desired bandwidth frequency; and with a phase margin of the desired amount considering stability and performance (usually 45 to 60 degrees).

Evaluate the loop gain at the bandwidth frequency and calculate the unknown gains.

Where: LG = 1.0 at an angle of -135 degrees
(45 degrees phase margin)
S = jw
BW = desired bandwidth frequency in Hertz
w = 2 πBW

$$1 \angle -135° = \frac{11.6\ K_i K_A K_T}{J\ j^2\ w^2} + \frac{K_A K_T\ .775\ K_P}{J\ jw}$$

Separate both sides of the equation into their real and imaginary parts:

$$-.707, -j\ .707 = \frac{-11.6\ K_i K_A K_T}{J\ w^2},\ -j\ \frac{K_A K_T\ .775\ K_P}{J\ w}$$

The real part can be solved directly for K_i and the imaginary part for K_p:

$$-.707 = \frac{-11.6\ K_i K_A K_T}{J\ (2\pi BW)^2} \text{ solving: } K_i = \frac{.707\ J\ (2\pi BW)^2}{11.6\ K_A K_T}$$

$$-j\ .707 = -j\ \frac{K_A K_T\ .775\ K_P}{J\ (2\pi BW)} \text{ solving: } K_P = \frac{.707\ J\ (2\pi BW)}{.775\ K_A K_T}$$

Let some values be assumed as an example and solve for the gains:
Let:

K_A = 1.0 Amp/volt
K_T = 3.5 oz-in/Amp
J = .0098 oz-in-sec²
BW = 1 Hz.

$K_i = (.707 \times .0098 \times (2\pi 1)^2)/(11.6 \times 1.0 \times 3.5) = .00674$

$K_p = (.707 \times .0098 \times (2\pi 1))/(.775 \times 1.0 \times 3.5) = .016$

These gains and assumed values can be put into the loop gain equation and as a design verification a bode plot can be made with SERVOCALC®, see Figure 2.

$$LG = \frac{11.6\ (.00674)\ (1.0)\ (3.5)}{(.0098)\ S^2}\ (1 + \frac{.775\ (.016)}{11.6\ (.00674)}\ S)$$

In polynomial form:

$$LG(s) = \frac{4.429\ S + 27.923}{S^2}$$

This polynomial is entered into the USER POLYNOMIAL module of SERVOCALC® and a Bode plot made.

As can be seen in the figure the 0 dB crossover is at 1 Hz and the phase margin is 45°.

Now that the gains have been calculated they need to be set in to the circuit with resistors R_p and R_i as in the data sheet. Let the summing resistor be R_o from the V_{in} pin to ground as on the data sheet; a suggested value is 10 KΩ. Solving for the resistors in the general case:

$$R_P = R_O\ (\frac{1 - K_i}{K_P} - 1)$$

$$R_i = R_O\ (\frac{1 - K_P}{K_i} - 1)$$

And solving for our example case:

R_p = 610 KΩ
R_i = 1.45 MΩ

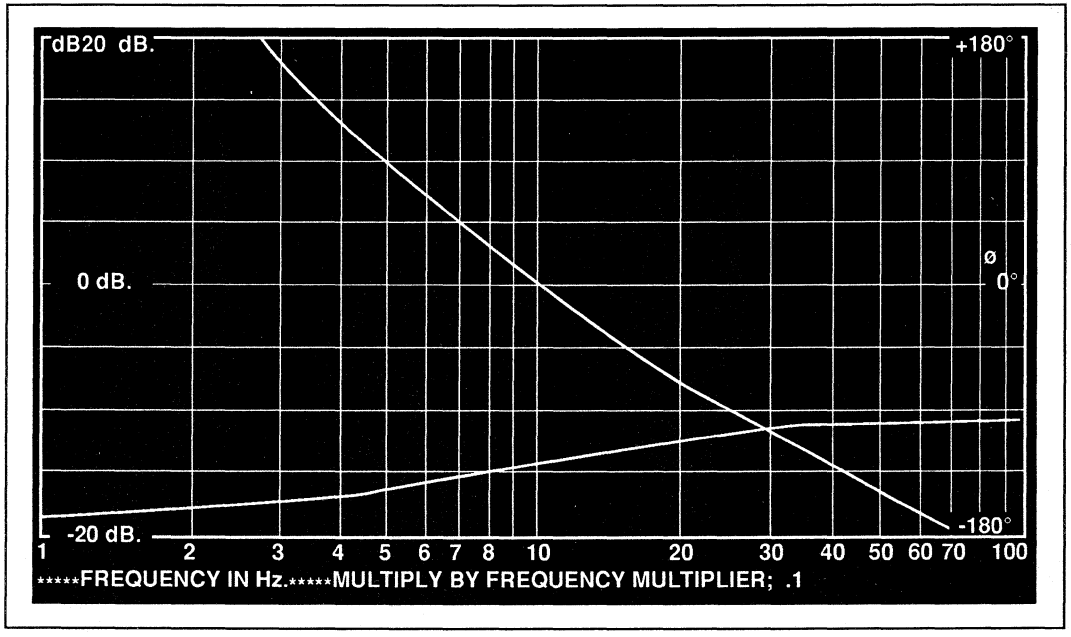

FIGURE 2: Open Loop Bode Plot

Notes:

Notes:

Notes:

Silicon Systems, Inc.
Storage Products Division
14351 Myford Road, Tustin, CA 92680
Ph (714) 573-6000, Fax (714) 573-6914