QUALITY CONTROL OF MAGNETIC SUB-ASSEMBLIES

by

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Recently digital computing systems have been designed incorporating large numbers of square hysteresis loop magnetic cores as the basic element for a variety of logical circuits. (1, 2, 3, 4) Typical applications for cores of this type are shift registers and switching cores. In addition, using such cores OR, INHIBIT, and AND circuits can be designed and combined to derive complex logical functions. The operating speeds of these magnetic circuits are being increased satisfactorily and the power required to operate these circuits is reasonable for most computer applications. It therefore appears that magnetic core circuits have become a permanent and practical component in computers.

However, the inherent reliability of magnetic core circuits can be and has been hidden in the final computer application by inadequate control of the core characteristics, by neglect of associated component tolerances, and by inadequate testing of the finished core circuit sub-assembly. These quality control problems have been studied in some detail and the general approach to their solution will now be discussed in terms of a specific type of circuit; the one core per bit shift register circuit shown in Fig. 1.

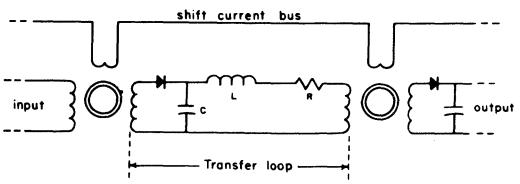

Fig. 1

The magnetic core test must reflect the requirements of the final circuit application. In the shift register circuit the core responds to current pulses and therefore, must be tested under pulse conditions and not with sinusodial currents. It is well known that the hysteresis loop characteristics of magnetic cores change as a function of the frequency of the applied sinusodial current; and it is, therefore, not surprising that these characteristics can be modified to a greater extent when the core responds to pulse waveforms. There are two core characteristic curves, which when related to the shift register transfer loop requirements, are useful in specifying a meaningful test on the basic core.

Figure 2 shows the general form under pulse conditions of the curve relating the applied magnetic field magnitude and the switching time required for total flux reversal to occur within the core. (5) Figure 3 indicates the magnitude of the flux change within the core as the magnitude of the "read" current pulse is varied holding the "write" current pulse at a constant value sufficient to completely reset the core. It should be noted that the maximum switching time of the core is restricted in this curve since the total flux change must occur before the completion of the read current pulse. These curves (Fig. 2 and Fig. 3) may be directly related to shift register design and are used to specify the core test conditions.

In order to relate the circuit requirements to the core test the characteristics of the transfer loop current pulse must be determined while the circuit is operating at the lowest design transfer current sufficient to switch the following core. The switching

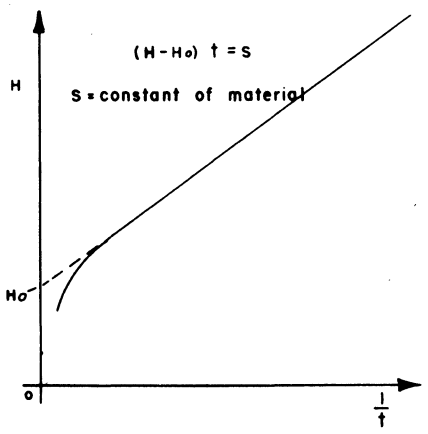

Fig. 2

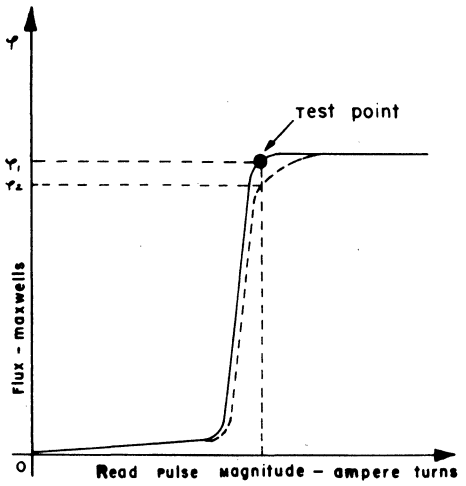

Fig. 3

time of the core as a result of this transfer current should be observed. Since the core to be switched is not connected to any low impedance load at this time in the circuit operation, these experimentally determined values may be checked against Fig. 2.

The next step is to determine experimentally, the flux change vs read pulse curve for the core when switched by a current pulse of maximum duration equal to the maximum switching time as determined in the previous experiment on the actual shift register circuit. This curve of course, will be similar to Fig. 3. A number of these curves should be plotted for various cores which operate satisfactorily in the laboratory shift register to determine an acceptable average curve and the tolerances on the flux change required. The value of the time-averaged read ampere turns (6) at the upper knee of the test flux curve should correspond to the time-averaged value of the minimum ampere turns of the input winding in the transfer loop circuit, and this amplitude value, with its associated pulse duration, define the test conditions for the basic core. This single test condition allows one to select and reject all cores whose switching time is too long, whose coercive force is too large, and whose flux change magnitude is not within specified limits. Any changes in these basic core parameters will be revealed as changes in the apparent flux change of the core. Since the test point is located on the knee of the curve any increase of the switching time or of the coercive force will result in partial switching and will cause a large scale change of total flux as indicated by the dotted line curve of Fig. 3. All cores which pass this test will always be completely switched in the shift register by the minimum transfer current.

The flux change value is obtained by integrating with respect to time, the voltage output of a single turn passing through the core. One might question the necessity of performing this integration, since there would also be large changes in the peak output voltage if the core did not meet the specifications. The answer to this question is also provided by the actual circuit configuration. The capacitor in the transfer loop is charged to the required voltage by the time average current flowing in the output winding of the core during the switching time. Detailed analysis of the circuit reveals that the total flux change which occurs during this time interval determines the magnitude of the time average current. The peak open circuit voltage is not of primary importance as it is related to the rate of change of flux when there is no load on the output winding. The integration or total flux change measurement is therefore directly related to this type of circuit application. It should be noted that this test might not apply to a different type of circuit.

This concept is not only important from the point of view of reliable one signal transfer in the shift register, but also is effective in controlling the magnitude of the zero signal. The zero flux change is realized by means of a second read current pulse before the core is switched again by the write pulse. The maximum value of the zero flux change is specified relative to the final shift register performance requirements on the signal to noise ratio.

The outlined core test displays on an os-

cillograph trace the integrated signals of one and zero flux change, and as a result of a single observation one may select cores whose basic parameters, total flux change, switching time, coercive force, and squareness ratio are acceptable for operation in the shift register. The central instrumentation problem with this type of test is that of designing an integrator capable of relatively noise free operation at low signal levels. A typical integrated signal is shown in Fig. 4. The integrated signal shown here is 10 maxwells.

In the development of a laboratory shift register design into a production model the next major step is the consideration of the tolerances required on the various individual components of a shift register stage to realize the final performance operating tolerances. These decisions must be made in terms of the physical equations describing the circuit operation. Since the purpose of this paper is not to derive these equations and since the process of introducing variations into equations to determine tolerances is well known, this aspect will not be discussed further except to state that it is an obviously important part of the quality control problem.

Final testing of the shift register stages after assembly must determine in a concise manner that each unit will perform with the anticipated margins or tolerances in the system application. A single core per bit shift register has an operating tolerance curve consisting of the peak shift current pulse amplitude plotted as a function of shift current pulse width as shown in Fig. 5. This curve defines an area within which the shift register will reliably operate. It is desirable that each shift register stage possess tolerance curves whose point-by-point values agree within certain tolerances with the desired curve. It would be extremely time-consuming to have to measure a complete tolerance curve for each shift register as it comes off the end of the production line, therefore, a correlation between a few test points and the complete curve should be established. In order that an actual correlation can be established the test points and method of test must be related as in the case of the basic core to the circuit design.

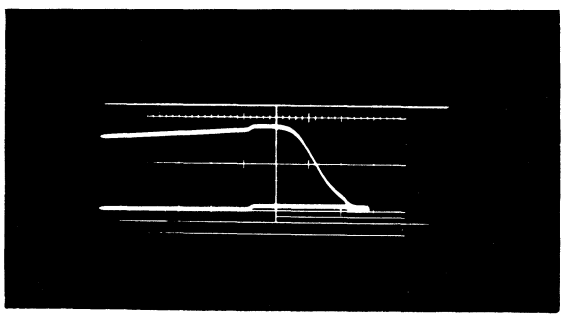

Fig. 4

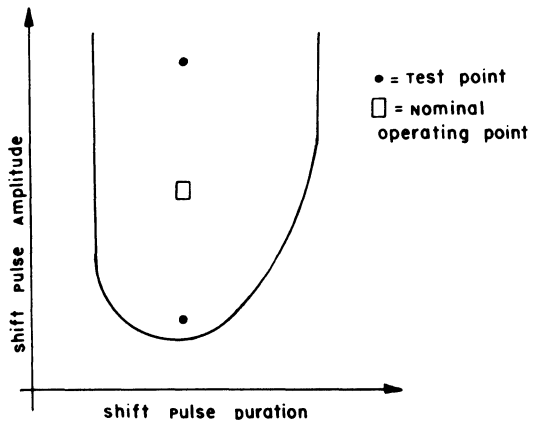

Fig. 5

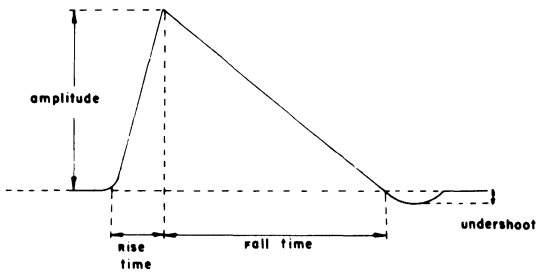

Fig. 6

It has been found by testing large numbers of single core per bit shift registers that two test points in the operating area of the tolerance curve are required for a correlated check on the overall tolerances. These two points are both located at the nominal operating shift pulse width but one point is located at the bottom of the tolerance curve with respect to current amplitude and the other point is located at twice the nominal operating current amplitude. Each stage is tested individually and its output is connected back to its own input so that the overall gain of the core and its associated transfer loop must be greater than unity for a single "one" signal to recirculate. This single stage recirculation test is more severe than inserting the stage under test in the middle of a string of nominal stages since the good stages on

either side of a low gain stage could support the poorer stage with the result that the overall gain would be satisfactory.

In addition to checking recirculation at the lower current point the voltage waveform characteristics across the capacitor are also measured. These measurements include peak amplitude, rise time, fall time and undershoot as shown in Fig. 6. The rise time is equivalent to the switching time of the core, the peak voltage amplitude is inversely proportional to the capacitor value and directly related to the total flux change and finally the fall time and undershoot serve as a check on the resistor and the inductor values. The tolerances on these parameters are, as mentioned, directly related to the circuit component tolerances. Checking for recirculation and "one" signal characteristics at the bottom of the tolerance curve is the most stringent test that could be imposed on these two general performance aspects.

The zero signal of similar waveform but much smaller in magnitude is also checked at a critical point; the upper current level test condition. The zero signal must be less than a maximum value which is chosen to insure that shift register stage will always have a signal to noise ratio satisfactory to the final system application.

Certain d-c tests should be made in addition to the pulse tests. All shift register stages are flash tested between all normally open circuit paths at a minimum of one and a half times the maximum working voltage. All stages are tested at the same points for leakage resistance to check any incipient break-down condition, and life tests are regularly conducted at elevated temperatures and voltages.

In conclusion, the general philosophy of testing single core per bit shift registers is to test the basic square loop core under conditions similar to the transfer circuit minimum current magnitudes and to measure the total flux change during the required switching time since this parameter is fundamental to the circuit operation. The component tolerances should be related by means of circuit equations to the final performance specifications. And, finally the finished shift register stage should be tested for its ability to recirculate a specified signal when operated at its required minimum shift current amplitude. This procedure has been outlined for a single core per bit shift register but can be applied to other magnetic sub-assemblies although the details of the testing will be considerably different.

Acknowledgment

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