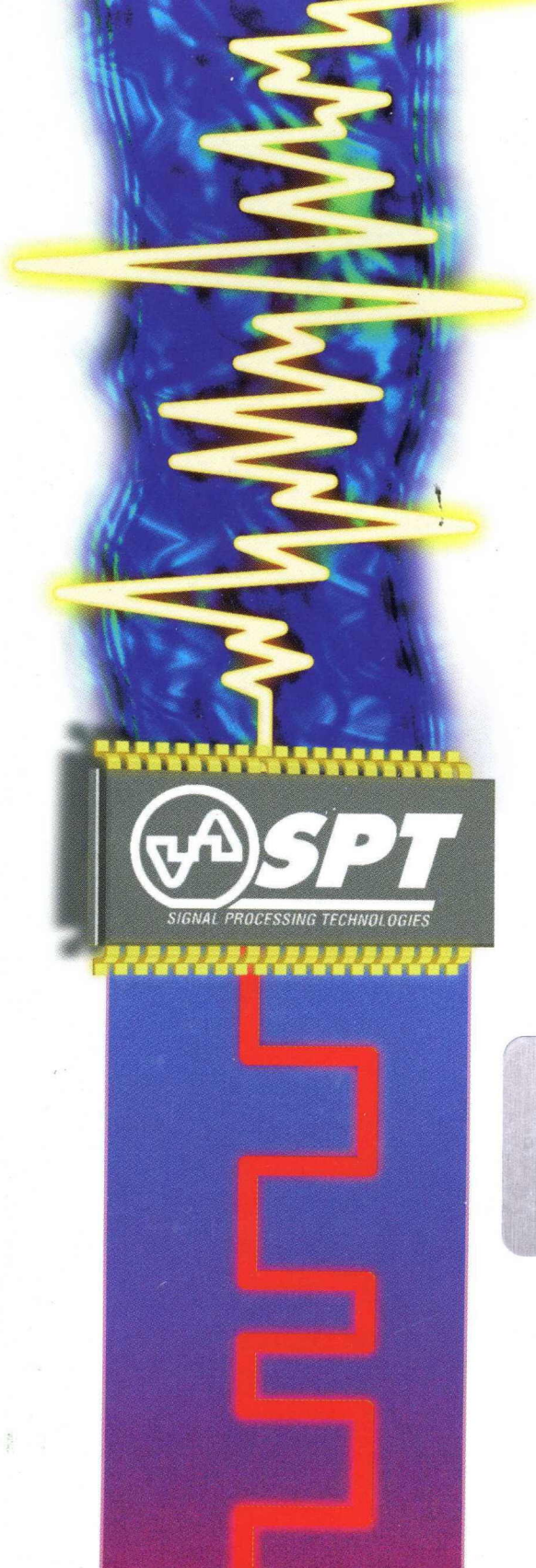
1995 DATA BOOK

SIGNAL PROCESSING TECHNOLOGIES

SPT



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Leadership in

Data Conversion

and Signal Processing

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SIGNAL PROCESSING TECHNOLOGIES

ISO 9001 CERTIFIED

SIGNAL PROCESSING TECHNOLOGIES

1995 DATA BOOK

SIGNAL PROCESSING TECHNOLOGIES, INC.

4755 FORGE ROAD, COLORADO SPRINGS, CO 80907
PHONE: (719) 528-2300 FAX: (719) 528-2370

GENERAL INFORMATION

TYPES OF DATA SHEETS

ADVANCE INFORMATION — These data sheets contain the descriptions of products that are in development. The specifications are based on engineering calculations, computer simulations and/or initial prototype evaluation.

PRELIMINARY — These data sheets contain minimum and maximum specifications that are based on initial device characterization. These limits are subject to change upon the completion of full characterization over the specified temperature and supply voltage ranges.

FINAL — These data sheets contain specifications based on complete characterizations of the devices over the specified temperature and supply voltage ranges.

WARRANTY

SPT warrants that standard products (except for board-level products) delivered hereunder shall be free from defects in material and workmanship under normal use and service for a period of one (1) year from the date of shipment from SPT's facility. Board level products delivered hereunder shall be free from defects in material and workmanship under normal use and service for a period of ninety (90) days from the date of shipment from SPT's facility. For products which are not standard products, such as dice and wafers, SPT warrants to Buyer that such products shall be free from defects in material and workmanship under normal use and service for a period of thirty (30) days from the date of shipment. Products which are "engineering samples" are sold AS IS, "WITH ALL FAULTS," and with no warranty whatsoever.

If, during such one year, ninety day or thirty-day period (i) SPT is notified promptly in writing upon discovery of any defect in the goods, including a detailed description of such defect; (ii) such goods are returned to SPT, F.O.B. SPT's facility; and (iii) SPT's examination of such goods discloses to SPT's satisfaction that such goods are defective and such defects are not caused by accident, abuse, misuse, neglect, alteration, improper installation, repair or alteration by someone other than SPT, improper testing, or use contrary to any instructions issued by SPT, within a reasonable time, SPT shall (at its sole option) either replace or credit Buyer the purchase price of such goods.

Prior to any return of goods by Buyer pursuant to the section, Buyer shall afford SPT the opportunity to inspect such goods at Buyer's location, and any such goods so inspected shall not be returned to SPT without its prior written consent.

SPT shall return any goods repaired or replaced under this warranty to Buyer, transportation prepaid, and reimburse Buyer for the transportation charges paid by Buyer for such goods. The performance of this warranty does not extend the warranty period for any goods beyond that period applicable to the goods originally delivered.

The foregoing warranty constitutes SPT's exclusive liability, and the exclusive remedy of Buyer, for any breach of any warranty or other nonconformity of the goods covered by this quotation. THIS WARRANTY IS EXCLUSIVE, AND IN LIEU OF ALL OTHER WARRANTIES, EXPRESS, IMPLIED OR STATUTORY, INCLUDING BUT NOT LIMITED TO THE WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR USE, WHICH ARE HEREBY EXPRESSLY DISCLAIMED.

PRODUCTS AND SPECIFICATIONS

Signal Processing Technologies reserves the right to make changes to its products or specifications at any time, without notice, to improve the design and/or performance in order to supply the best possible product. Signal Processing Technologies does not assume any responsibility for the use of any circuitry described in this book other than the circuitry contained within a Signal Processing Technologies' product. Signal Processing Technologies makes no representations that the circuitry described within this book is free from patent infringement or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent, patent rights, or other rights of Signal Processing Technologies.

LIFE SUPPORT APPLICATIONS POLICY

WARNING — Signal Processing Technologies' products shall not be used within any life support systems without the specific written consent of Signal Processing Technologies. A life support system is a product or system intended to support or sustain life which, if it fails, can be reasonably expected to result in a significant personal injury or death.

How to Use This Book

The front part of this book has a complete product selection guide, cross reference table and detailed ordering information. The product selection guide lists all of the products and their key features for quick reference and comparison purposes, the product cross reference guide provides a cross over reference to other manufactures by product part number, and the ordering information section provides complete ordering information by part number, grade, package type and operating temperature range.

There is a master table of contents at the front of the book that shows the beginning page number of each data sheet, and each data sheet section has its own table of contents for that section. Data sheets for the analog-to-digital converters and the digital-to-analog converters are placed in ascending order of bit resolution, and the comparator and evaluation board data sheets are placed in alphanumeric order.

Customer Service

Customer support and service is extremely important to us at SPT. Not only do we pride ourselves on high-performance data conversion products, but we pride ourselves on high-performance customer service. Factory direct assistance is available weekdays from 7:30 AM to 5:30 PM MST. Please contact our Customer Service Center at 1-800-643-3778 (USA only) or 1-719-528-2300 to place an order, return products, ask technical or applications related questions, or order technical literature. For immediate local assistance contact your local SPT sales representative. See a listing of our domestic and international sales offices, representatives and distributors at the back of this book.

Technical Literature and Applications Assistance

Contact our Customer Service Center at 1-719-528-2300 for the latest product data sheets and evaluation board information. In addition to product data sheets, SPT has a complete line of product application notes to assist in the evaluation and board layout design of our high performance data conversion products. Contact the SPT Customer Service Center to order your technical application notes.

For factory direct applications support, our applications engineers are ready to answer all of your technical questions and inquiries. Contact our Applications Engineering Center at 1-719-528-2300 weekdays from 8:00 AM to 5:00 PM MST.

Prices and Quotations

Price quotations made by Signal Processing Technologies or its authorized field sales representatives are valid for 30 days. Delivery quotations are subject to reconfirmation at the time of order placement. Call our Customer Service Center for information concerning pricing, product delivery status, product samples or information regarding the return of product.

Placing Orders

You can place orders by telephone, fax or mail with any of our authorized sales representatives, distributors, regional offices or our Colorado Springs headquarters. See the listing of sales offices, representatives and distributors at the back of this book for the location nearest you or call SPT Sales and Marketing at 1-800-643-3778 (USA only) or 1-719-528-2300 for assistance.

Returns and Warranty Service

When you need to return products to SPT, contact us prior to shipping to obtain authorization and shipping instructions. For complete instructions, contact your local sales representative, distributor or call our Colorado Springs Customer Service Center at 1-800-643-3778 (USA only) or 1-719-528-2300. See the list of domestic and international representatives and distributors at the back of this book.

If you are returning products, please call for your RMA number, then ship units prepaid and supply the original purchase order number and date, along with an explanation of the malfunction. Upon receipt of the returned product, SPT will verify the problem and inform you of the status of any warranty replacements or credits applicable.

About SPT

- ✓ Founded in 1983.
- ✓ Develops, manufactures and markets high-performance data conversion and signal conditioning products.
- ✓ Corporate headquarters in Colorado Springs, CO.
- ✓ Domestic and international manufacturing facilities.
- ✓ Wholly-owned subsidiary of Toko, Inc.
- ✓ Sales offices in the United States and Europe with sales representatives throughout North America, Europe and the Far East.

Company Background

Signal Processing Technologies, Inc. (SPT) develops, manufactures and markets high-performance data conversion and signal conditioning products and is a leader in cost-effective, highest performance monolithic analog-to-digital converters (ADCs), digital-to-analog converters (DACs), and comparators. Since 1983 SPT has provided leading-edge monolithic conversion products with industry breakthroughs in resolution, sampling rate, power and cost.

Today, we continue to expand our line of converter and comparator products to meet our customer needs in the commercial, industrial, and military market sectors worldwide. This 1995 data book includes over 20 new data conversion products as well as many new temperature performance ranges and packaging options for existing products. With our innovative product line and excellence in customer application and sales support, SPT continues to be one of the fastest growing data conversion integrated circuit (IC) suppliers in the industry.

Key Markets and Applications

SPT's products are designed for a variety of commercial, industrial, and military systems applications. Commercial and industrial applications include video capture and TV broadcast, CRT monitors, desktop scanners, medical ultrasound, IR imaging, and RF communications including satellite, cellular and microwave systems. Additional applications include high-performance instrumentation such as automated test equipment (ATE), scientific instruments, and digital oscilloscopes. SPT's high-performance products lend themselves very well to military applications which include radar, guided weapons, surveillance and reconnaissance, target acquisition, navigation and guidance.

ISO9001 Certified

As of February 1995, Signal Processing Technologies, Inc. received ISO9001 certification from the internationally recognized British Standard Institute. BSI certifies companies across the world and is one of the leading bodies of the European Quality System Certification Network (EQNET).

ISO9001 is an international standard for assessing the quality management system for companies that perform design, manufacturing and testing of products. Certification means that a complete quality management system is in place for design/development, production, and servicing of all SPT products. The SPT quality management system is audited by BSI biannually to ensure conformity to the ISO9001 standard.

SPT — Leadership in Data Conversion and Signal Processing

TABLE OF CONTENTS

TABLE OF CONTENTS
Continued

4755 Forge Road, Co. Springs, CO 80907
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PRODUCT SELECTION GUIDE

HIGH-SPEED A/D CONVERTERS

Part No.	Grades	Resolution (Bits)	Sample Rate (MSPS)	SNR (dB) or INL (LSB)	Power (Watts)	Temp Range	Packages	Pins	Qual Levels	Features
SPT7610	S	6	1,000	36	2.75	I	Q,U	44	*	Wide input BW of 1.4 GHz
SPT1175	A	8	20	46	0.09	C	D,S,N,P,U	24,28	N/A	Single supply alternative
	B	8	30	44	0.09					to TMC1175 and CXD1175
SPT7710	A	8	150	48	2.2	I,M	J,G,Q,U	42,44,46	/883	Wide bandwidth
	B	8	150	47	2.2					No *sparkle codes*
SPT7725	A	8	300	47	2.2	I,M	J,G,Q,U	42,44,46	/883	Data ready and overrange outputs. Quarter point ladder taps.
	B	8	300	46	2.2					
SPT7750	A	8	500	47	5.5	I	G,K,U	68,80	*	Demuxed output. Gray code output. Wide input BW of 900 MHz.
	B	8	500	45	5.5					
SPT7755	A	8	750	46	5.5	I	G,K,U	68,80	*	Demuxed output. Gray code output. Wide input BW of 900 MHz.
	B	8	750	44	5.5					
SPT7760	A	8	1,000	42	5.5	I	G,K,U	68,80	*	Demuxed output. Gray code output. Wide input BW of 900 MHz.
	B	8	1,000	40	5.5					
SPT7810	A	10	20	60	1.3	C,I	J,N,U	28	*	On chip track-and-hold
	B	10	20	57	1.3					Monolithic
SPT7814	A	10	40	57	1.3	C,I	J,N,U	28	*	On chip track-and-hold
	B	10	40	54	1.3					Monolithic
SPT7820	A	10	20	60	1.0	C,I,M	J,C,S,N,U	28	/883	TTL output version of the
	B	10	20	57	1.0					SPT7810
SPT7824	A	10	40	57	1.0	C,I,M	J,C,S,N,U	28	/883	TTL output version of the
	B	10	40	54	1.0					SPT7814
SPT7830	S	10	2.5	57	.07	C	S,U	8	*	Serial output
										3.3 to 5.0 V Supply Range
SPT7835	S	10	5	59	.07	C,M	D,N,S,T,U	28,32	*	On chip track-and-hold
										Tri-state outputs
SPT7840	S	10	10	58	0.1	C,M	D,N,S,T,U	28,32	*	On chip track-and-hold
										Tri-state outputs
SPT7850	S	10	20	56	0.14	C,M	D,N,S,T,U	28,32	*	On chip track-and-hold
										Tri-state outputs
SPT7852	S	10	20	56	0.17	C	T,U	44	*	Dual ADC
SPT7855	S	10	25	58	0.14	C,M	D,N,S,T,U	28,32	*	On chip track-and-hold
										Tri-state outputs
SPT7860	S	10	40	54	0.18	C,M	D,N,S,T,U	28,32	*	On chip track-and-hold
										Tri-state outputs
SPT7861	S	10	40	58	0.16	C	N,S,T,U	28,32	*	Pin compatible with
										SPT7860
SPT7870	S	10	100	56	1.4	C	J,Q,U	32,44	*	Single-ended
										ECL outputs

* Consult the factory for availability of /883 processed units.

PRODUCT SELECTION GUIDE

HIGH-SPEED A/D CONVERTERS-Continued

Part No.	Grades	Resolution (Bits)	Sample Rate (MSPS)	SNR (dB) or INL (LSB)	Power (Watts)	Temp Range	Packages	Pins	Qual Levels	Features
SPT7871	S	10	100	56	1.3	C	J,Q,U	32,44	*	Single ended TTL outputs
SPT7910	S	12	10	67	1.4	C	J,U	32	*	Includes sample-and-hold on monolithic die
SPT7912	S	12	30	66	1.4	C	J,U	32	*	Includes sample-and-hold on monolithic die
SPT7920	S	12	10	66	1.1	C,M	J,Q,U	32,44	*	TTL output version of the SPT7910
SPT7922	S	12	30	65	1.1	C,M	J,Q,U	32,44	*	TTL output version of the SPT7912
SPT7930	S	12	5	69	0.45	C,M	J,S,U	28	*	Includes sample-and-hold on monolithic CMOS die

MEDIUM-SPEED A/D CONVERTERS

Part No.	Grades	Resolution (Bits)	Conversion Time (µs)	Linearity (LSB)	Full Scale** TC (PPM/°C)	Temp Range	Packages	Pins	Qual Levels	Features
HADC574Z	A	12	25	1/2	10	C,I,M	J,D,C,U	28	/883	Input ranges 0-10, 0-20, ±5, and ±10. Low power. Alternatives for HI574 & AD574. DESC drawing available.
	B	12	25	1/2	27					
	C	12	25	1	45					
HADC674Z	A	12	15	1/2	10	C,I,M	J,D,C,U	28	/883	Input ranges 0-10, 0-20, ±5, and ±10. Low power. HI674 alternative. DESC drawing available.
	B	12	15	1/2	27					
	C	12	15	1	45					
SPT774	A	12	8	1/2	10	C, I, M	J,D,C,U	28	/883	Input ranges 0-10, 0-20, ±5, and ±10. Low power. Alternative to the HI774 and AD1674.
	B	12	8	1/2	27					
	C	12	8	1	45					

D/A CONVERTERS - GENERAL PURPOSE

Part No.	Grades	Resolution (Bits)	Settling Time (ns)	INL (LSB)	Output Type	Temp Range	Packages	Pins	Qual Levels	Features
SPT9712	S	12	8	1	I,V	I	N,P,U	28	*	ECL input compatible
SPT9713	S	12	8	1	I,V	I	N,P,U	28	*	TTL input compatible
SPT5216	B	16	150	2/6***	I,V	C	J,Q,U	32,44	*	Parallel input reference, Output range: +10 to 0, +5 to 0, ±5 or ±2.5 V
	C	16	150	2/8***	I,V					

* Consult the factory for availability of /883 processed units.
** Commercial temperature grades.
*** Over temperature.

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PRODUCT SELECTION GUIDE

D/A CONVERTERS - VIDEO

Part No.	Grades	Resolution (Bits)	Glitch Energy (PV-S)	Linearity (LSB)	Conversion Rate (MWPS)	Temp Range	Packages	Pins	Qual Levels	Features
SPT5100	S	8	-	1/2	20	C	T	32	N/A	Dual DAC
SPT5110	S	8	-	1/2	30	C	T	48	N/A	Triple DAC
SPT1018	A	8	10	1/2	275	I/M	N,U	24	/883	Video control alternative to the TDC1018
	B	8	10	1/2	165					
SPT1019	A	8	10	1/2	275	I/M	N,U	24	/883	Video control with reference
	B	8	10	1/2	165					
SPT5140	S	8	10	1/2	400	I/M	N,U	24	/883	Ref, video control
SPT5220	S	10	-	1	80	C	N	28	N/A	Single +5 V supply Video controls
SPT5230	S	10	-	1	50	C	T	52	N/A	Triple DAC

COMPARATORS

Part No.	Grades	TR/TF (ns)	Prop Delay (ns)	V_{CM} (V)	V_{OS} (mV)	Power Dissipation (mW)	Temp Range	Packages	Pins	Features
HCMP96850	S	1.76/1.76	2.4	±2.5	±3.0	90	I	D,U	16	Symmetrical TR/TF. Alternative to the AD9685
SPT9687	S	1.2/1.2	2.0	±2.5	±3.0	185	I	N,D,C,P,J,U	16,20	High performance Alternative for the AD96687
SPT9689	A	.18/.08	.65	-2.5/+4.0	±10	350	I	J,C,P,U	16,20	900 MHz bandwidth
	B	.18/.08	.65	-2.5/+4.0	±25	350				Differential latch control
SPT9691	S	0.4/0.4	2.2	-4/+8.0	±25	700	C	J,C,P,N,U	20	JFET inputs. Constant propagation delays
SPT9693	S	0.45/0.45	1.25	-3/+8.0	±25	430	C	J,C,P,U	20	JFET inputs. Constant propagation delays

* Consult the factory for availability of /883 processed units.

PRODUCT SELECTION GUIDE

PIN DRIVERS

Part No.	Grades	Speed (MHz)	Voltage Range (V)	Output Slew Rate at 3V (V/ns)	Output Capacitance (pF)	Power (W)	Temp Range	Packages	Pins	Features
SPT9500	S	300	-3 to +10	1.0	5	1.2	C	P	28	Variable output levels for ECL, TTL, and CMOS

SAMPLE-AND-HOLDS

Part No.	Grades	Acq. Time (ns) at 0.1% Accuracy	Acq. Time (ns) at 0.01% Accuracy	Aperture Time ns (typ)	Aperture Jitter ns (typ)	Droop Rate mV/µs (max)	Power Dissipation (mW)	Temp Range	Packages	Pins	Features
SPT9101	S	7.0	11.0	0.5	<0.001	20	550	I	S,C,U	20	Alternative to AD9101

Package Type Key

- J Ceramic Sidebrazed DIP
- D Cerdip
- C Leadless Chip Carrier (LCC)
- G Pin Grid Array
- K MQuad
- N Plastic Dip
- P Plastic Leaded Chip Carrier (PLCC)
- Q Cerquad
- S Small Outline Package (SOIC)
- T Quad Flat pack or Thin Quad Flat Pack
- U Die

Temperature Range Key

- C Commercial (0 to +70 °C)
- I Industrial (-25 to +85 °C)
- M Military (-55 to +125 °C)

Grades Key

- A Highest
- C Lowest
- S Single Grade

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PRODUCT CROSS REFERENCE GUIDE

(INDUSTRIAL SPT EQUIVALENT)

ANALOG DEVICES	SPT	DESCRIPTION
AD574AJD	HADC574ZCCD	12-BIT ADC
AD574AKD	HADC574ZBCD	12-BIT ADC
AD574ALD	HADC574ZACD	12-BIT ADC
AD574ASD	HADC574ZCMD	12-BIT ADC
AD574ATD	HADC574ZBMD	12-BIT ADC
AD574AUD	HADC574ZAMD	12-BIT ADC
AD674AJD	HADC674ZCCD	12-BIT ADC
AD674AKD	HADC674ZBCD	12-BIT ADC
AD674ALD	HADC674ZACD	12-BIT ADC
AD674ASD	HADC674ZCMD	12-BIT ADC
AD674ATD	HADC674ZBMD	12-BIT ADC
AD674AUD	HADC674ZAMD	12-BIT ADC
AD1674JN	SPT774CCD	12-BIT ADC
AD1674KN	SPT774BCD	12-BIT ADC
AD1674AD	SPT774CIJ	12-BIT ADC
AD1674BD	SPT774BIJ	12-BIT ADC
AD1674TD	SPT774BMJ	12-BIT ADC
AD9712	SPT9712	12-BIT DAC
AD9713	SPT9713	12-BIT DAC
AD9101	SPT9101	12-BIT THA
AD96685B	HCMP96850SID	SINGLE COMPARATOR
AD96687B	SPT9687	DUAL COMPARATOR

BURR BROWN	SPT	DESCRIPTION
ADC574AJH	HADC574ZCCD	12-BIT ADC
ADC574AKH	HADC574ZBCD	12-BIT ADC
ADC574ASH	HADC574ZCMD	12-BIT ADC
ADC574ATH	HADC574ZBMD	12-BIT ADC
ADC674AJH	HADC674ZCCD	12-BIT ADC
ADC674AKH	HADC674ZBCD	12-BIT ADC
ADC674ASH	HADC674ZCMD	12-BIT ADC
ADC674ATH	HADC674ZBMD	12-BIT ADC
ADS574JP	HADC574ZCCD	12-BIT ADC
ADS574KP	HADC574ZBCD	12-BIT ADC
ADS574SH	HADC574ZCMJ	12-BIT ADC
ADS574TH	HADC574ZBMJ	12-BIT ADC
ADS774JP	HADC774CCJ	12-BIT ADC
ADS774KP	HADC774BCJ	12-BIT ADC
ADS774SH	HADC774CMJ	12-BIT ADC
ADS774TH	HADC774BMJ	12-BIT ADC

BURR BROWN	SPT	DESCRIPTION
ADC774JH	SPT774CCJ	12-BIT ADC
ADC774KH	SPT774BCJ	12-BIT ADC
ADC774SH	SPT774CMJ	12-BIT ADC
ADC774TH	SPT774BMJ	12-BIT ADC

HARRIS	SPT	DESCRIPTION
HI1-574AJD-5	HADC574ZCCJ	12-BIT ADC
HI1-574AKD-5	HADC574ZBCJ	12-BIT ADC
HI1-574ALD-5	HADC574ZACJ	12-BIT ADC
HI1-574ASD-2	HADC574ZCMJ	12-BIT ADC
HI1-574ATD-2	HADC574ZBMJ	12-BIT ADC
HI1-574AUD-2	HADC574ZAMJ	12-BIT ADC
HI1-674AJD-5	HADC674ZCCJ	12-BIT ADC
HI1-674AKD-5	HADC674ZBCJ	12-BIT ADC
HI1-674ALD-5	HADC674ZACJ	12-BIT ADC
HI1-674ASD-2	HADC674ZCMJ	12-BIT ADC
HI1-674ATD-2	HADC674ZBMJ	12-BIT ADC
HI1-674AUD-21	HADC674ZAMJ	12-BIT ADC
HI1-774J-5	SPT774CCJ	12-BIT ADC
HI1-774K-5	SPT774BCJ	12-BIT ADC
HI1-774S-2	SPT774CMJ	12-BIT ADC
HI1-774T-2	SPT774BMJ	12-BIT ADC
HI-1175	SPT1175	8-BIT, 20 MSPS ADC

MICRO POWER	SPT	DESCRIPTION
MP8780	SPT1175	8-BIT, 20 MSPS ADC

PLESSEY	SPT	DESCRIPTION
SP9685DG	HCMP96850SID	SINGLE COMPARATOR
SP9687DG	SPT9687	DUAL COMPARATOR

SONY	SPT	DESCRIPTION
CX20116	SPT7710AIJ	8-BIT, 150 MSPS ADC
CXA1396D	SPT7710AIJ	8-BIT, 150 MSPS ADC
CXD1175AM	SPT1175	8-BIT, 20 MSPS ADC

RAYTHEON	SPT	DESCRIPTION
TDC1018	SPT1018	8-BIT, 275 MWPS DAC
TMC1175M7C20	SPT1175	8-BIT 20 MSPS ADC
TMC1175M7C30	SPT1175	8-BIT, 30 MSPS ADC

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SPECIFICATION DEFINITIONS

APERTURE DELAY

Aperture delay represents the point in time, relative to the rising edge of the CLOCK input, that the analog input is sampled.

APERTURE JITTER

The variations in aperture delay for successive samples.

DIFFERENTIAL GAIN (DG)

A signal consisting of a sine wave superimposed on various DC levels is applied to the input. Differential gain is the maximum variation in the sampled sine wave amplitudes at these DC levels.

DIFFERENTIAL PHASE (DP)

A signal consisting of a sine wave superimposed on various DC levels that is applied to the input. Differential phase is the maximum variation in the sampled sine wave phases at these DC levels.

EFFECTIVE NUMBER OF BITS (ENOB)

SINAD = 6.02N + 1.76, where N is equal to the effective number of bits.

$$N = \frac{SINAD - 1.76}{6.02}$$

+/- FULL-SCALE ERROR (GAIN ERROR)

Difference between measured full scale response [(+Fs) - (-Fs)] and the theoretical response (+4 V -2 LSBs) where the +FS (full scale) input voltage is defined as the output transition between 1-10 and 1-11 and the -FS input voltage is defined as the output transition between 0-00 and 0-01.

INPUT BANDWIDTH

Small signal (50 mV) bandwidth (3 dB) of analog input stage.

DIFFERENTIAL NONLINEARITY (DNL)

Error in the width of each code from its theoretical value. (Theoretical = $V_{FS}/2^N$)

INTEGRAL NONLINEARITY (INL)

Linearity error refers to the deviation of each individual code (normalized) from a straight line drawn from -Fs through +Fs. The deviation is measured from the edge of each particular code to the true straight line.

OUTPUT COMPLIANCE

The maximum allowable output voltage swing of a digital-to-analog converter.

OUTPUT DELAY

Time between the clock's triggering edge and output data valid.

OVERVOLTAGE RECOVERY TIME

The time required for the ADC to recover to full accuracy after an analog input signal 125% of full scale is reduced to 50% of the full-scale value.

SIGNAL-TO-NOISE RATIO (SNR)

The ratio of the fundamental sinusoid power to the total noise power. Harmonics are excluded.

SIGNAL-TO-NOISE AND DISTORTION (SINAD)

The ratio of the fundamental sinusoid power to the total noise and distortion power.

TOTAL HARMONIC DISTORTION (THD)

The ratio of the total power of the first 64 harmonics to the power of the measured sinusoidal signal.

SPURIOUS FREE DYNAMIC RANGE (SFDR)

The ratio of the fundamental sinusoidal amplitude to the single largest harmonic or spurious signal.

LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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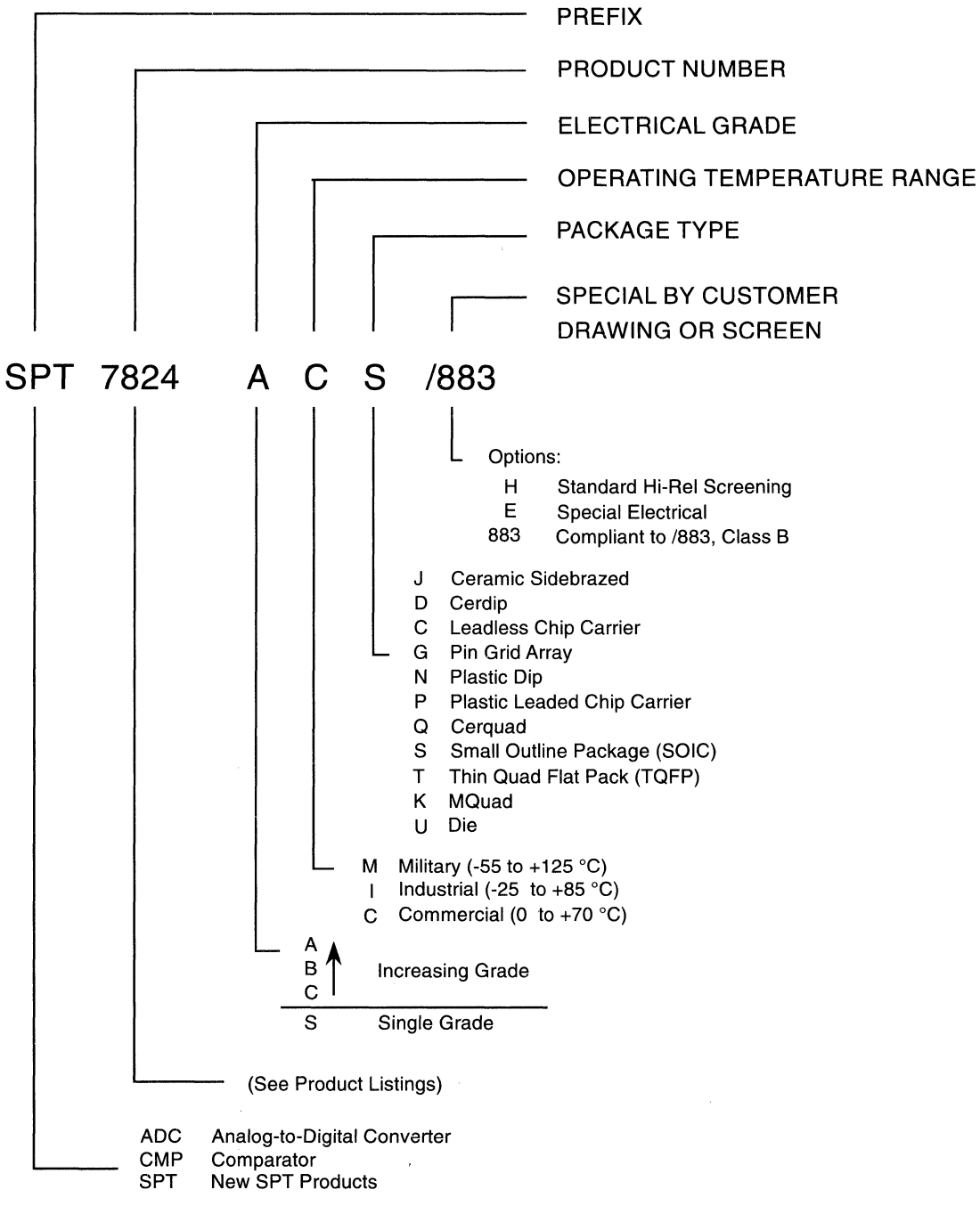
SPT PRODUCT IDENTIFICATION CODE



ORDERING INFORMATION

ANALOG-TO-DIGITAL CONVERTERS

PART NUMBER	DESCRIPTION	PACKAGE TYPE	# PINS	TEMPERATURE RANGE
HADC574ZAC(X)	12-BIT, 25 µsec ADC	SEE NOTE BELOW	28	COMMERCIAL
HADC574ZBC(X)	12-BIT, 25 µsec ADC	SEE NOTE BELOW	28	COMMERCIAL
HADC574ZCC(X)	12-BIT, 25 µsec ADC	SEE NOTE BELOW	28	COMMERCIAL
HADC574ZAI(X)	12-BIT, 25 µsec ADC	SEE NOTE BELOW	28	INDUSTRIAL
HADC574ZBI(X)	12-BIT, 25 µsec ADC	SEE NOTE BELOW	28	INDUSTRIAL
HADC574ZCI(X)	12-BIT, 25 µsec ADC	SEE NOTE BELOW	28	INDUSTRIAL
HADC574ZAM(X)	12-BIT, 25 µsec ADC	SEE NOTE BELOW	28	MILITARY
HADC574ZBM(X)	12-BIT, 25 µsec ADC	SEE NOTE BELOW	28	MILITARY
HADC574ZCM(X)	12-BIT, 25 µsec ADC	SEE NOTE BELOW	28	MILITARY
HADC574ZAM(X)/883	12-BIT, 25 µsec ADC	SEE NOTE BELOW	28	MILITARY/883
HADC574ZBM(X)/883	12-BIT, 25 µsec ADC	SEE NOTE BELOW	28	MILITARY/883
HADC574ZCM(X)/883	12-BIT, 25 µsec ADC	SEE NOTE BELOW	28	MILITARY/883
HADC574ZCCU	12-BIT, 25 µsec ADC	DIE		+25 °C
	DESC Drawing Number 5962-85127		28	MILITARY/883
HADC674ZAC(X)	12-BIT, 15 µsec ADC	SEE NOTE BELOW	28	COMMERCIAL
HADC674ZBC(X)	12-BIT, 15 µsec ADC	SEE NOTE BELOW	28	COMMERCIAL
HADC674ZCC(X)	12-BIT, 15 µsec ADC	SEE NOTE BELOW	28	COMMERCIAL
HADC674ZAI(X)	12-BIT, 15 µsec ADC	SEE NOTE BELOW	28	INDUSTRIAL
HADC674ZBI(X)	12-BIT, 15 µsec ADC	SEE NOTE BELOW	28	INDUSTRIAL
HADC674ZCI(X)	12-BIT, 15 µsec ADC	SEE NOTE BELOW	28	INDUSTRIAL
HADC674ZAM(X)	12-BIT, 15 µsec ADC	SEE NOTE BELOW	28	MILITARY
HADC674ZBM(X)	12-BIT, 15 µsec ADC	SEE NOTE BELOW	28	MILITARY
HADC674ZCM(X)	12-BIT, 15 µsec ADC	SEE NOTE BELOW	28	MILITARY
HADC674ZAM(X)/883	12-BIT, 15 µsec ADC	SEE NOTE BELOW	28	MILITARY/883
HADC674ZBM(X)/883	12-BIT, 15 µsec ADC	SEE NOTE BELOW	28	MILITARY/883
HADC674ZCM(X)/883	12-BIT, 15 µsec ADC	SEE NOTE BELOW	28	MILITARY/883
HADC674ZCCU	12-BIT, 15 µsec ADC	DIE		+25 °C
	DESC Drawing Number 5962-91690		28	MILITARY/883
SPT774AC(X)	12-BIT, 8 µsec ADC	SEE NOTE BELOW	28	COMMERCIAL
SPT774BC(X)	12-BIT, 8 µsec ADC	SEE NOTE BELOW	28	COMMERCIAL
SPT774CC(X)	12-BIT, 8 µsec ADC	SEE NOTE BELOW	28	COMMERCIAL
SPT774AI(X)	12-BIT, 8 µsec ADC	SEE NOTE BELOW	28	INDUSTRIAL
SPT774BI(X)	12-BIT, 8 µsec ADC	SEE NOTE BELOW	28	INDUSTRIAL
SPT774CI(X)	12-BIT, 8 µsec ADC	SEE NOTE BELOW	28	INDUSTRIAL
SPT774AM(X)	12-BIT, 8 µsec ADC	SEE NOTE BELOW	28	MILITARY
SPT774BM(X)	12-BIT, 8 µsec ADC	SEE NOTE BELOW	28	MILITARY
SPT774CM(X)	12-BIT, 8 µsec ADC	SEE NOTE BELOW	28	MILITARY
SPT774AM(X)/883	12-BIT, 8 µsec ADC	SEE NOTE BELOW	28	MILITARY/883
SPT774BM(X)/883	12-BIT, 8 µsec ADC	SEE NOTE BELOW	28	MILITARY/883
SPT774CM(X)/883	12-BIT, 8 µsec ADC	SEE NOTE BELOW	28	MILITARY/883
SPT774CCU	12-BIT, 8 µsec ADC	DIE		+25 °C
SPT7610SIQ	6-BIT, 1 GSPS ADC	CERQUAD	44	INDUSTRIAL
SPT7610SCU	6-BIT, 1 GSPS ADC	DIE		+25 °C

NOTE: (X) Denotes Package Type: J - SIDEBRAZED DIP; D - CERDIP; C - LCC

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ANALOG-TO-DIGITAL CONVERTERS - Continued

PART NUMBER	DESCRIPTION	PACKAGE TYPE	# PINS	TEMPERATURE RANGE
SPT1175ACD	8-BIT, 20 MSPS ADC	CERDIP	24	COMMERCIAL
SPT1175ACN	8-BIT, 20 MSPS ADC	PLASTIC DIP	24	COMMERCIAL
SPT1175ACP	8-BIT, 20 MSPS ADC	PLCC	28	COMMERCIAL
SPT1175ACS	8-BIT, 20 MSPS ADC	SOIC	24	COMMERCIAL
SPT1175BCD	8-BIT, 30 MSPS ADC	CERDIP	24	COMMERCIAL
SPT1175BCN	8-BIT, 30 MSPS ADC	PLASTIC DIP	24	COMMERCIAL
SPT1175BCP	8-BIT, 30 MSPS ADC	PLCC	28	COMMERCIAL
SPT1175BCS	8-BIT, 30 MSPS ADC	SOIC	24	COMMERCIAL
SPT1175SCU	8-BIT, 20 MSPS ADC	DIE		+25 °C
SPT7710AIJ	8-BIT, 150 MSPS ADC ±.75 LSB	SIDEBRAZED	42	INDUSTRIAL
SPT7710BIJ	8-BIT, 150 MSPS ADC ±.95 LSB	SIDEBRAZED	42	INDUSTRIAL
SPT7710AIG	8-BIT, 150 MSPS ADC ±.75 LSB	PGA	46	INDUSTRIAL
SPT7710BIG	8-BIT, 150 MSPS ADC ±.95 LSB	PGA	46	INDUSTRIAL
SPT7710AIQ	8-BIT, 150 MSPS ADC ±.75 LSB	CERQUAD	44	INDUSTRIAL
SPT7710BIQ	8-BIT, 150 MSPS ADC ±.95 LSB	CERQUAD	44	INDUSTRIAL
SPT7710AMJ	8-BIT, 150 MSPS ADC ±.75 LSB	SIDEBRAZED	42	MILITARY
SPT7710BMJ	8-BIT, 150 MSPS ADC ±.95 LSB	SIDEBRAZED	42	MILITARY
SPT7710AMQ	8-BIT, 150 MSPS ADC ±.75 LSB	CERQUAD	44	MILITARY
SPT7710BMQ	8-BIT, 150 MSPS ADC ±.95 LSB	CERQUAD	44	MILITARY
SPT7710AMJ/883	8-BIT, 150 MSPS ADC ±.75 LSB	SIDEBRAZED	42	MILITARY/883
SPT7710BMJ/883	8-BIT, 150 MSPS ADC ±.95 LSB	SIDEBRAZED	42	MILITARY/883
SPT7710AMQ/883	8-BIT, 150 MSPS ADC ±.75 LSB	CERQUAD	44	MILITARY/883
SPT7710BMQ/883	8-BIT, 150 MSPS ADC ±.95 LSB	CERQUAD	44	MILITARY/883
SPT7710BCU	8-BIT, 150 MSPS ADC ±.95 LSB	DIE		+25 °C
SPT7725AIJ	8-BIT, 300 MSPS ADC ±.75 LSB	SIDEBRAZED	42	INDUSTRIAL
SPT7725BIJ	8-BIT, 300 MSPS ADC ±.95 LSB	SIDEBRAZED	42	INDUSTRIAL
SPT7725AIG	8-BIT, 300 MSPS ADC ±.75 LSB	PGA	46	INDUSTRIAL
SPT7725BIG	8-BIT, 300 MSPS ADC ±.95 LSB	PGA	46	INDUSTRIAL
SPT7725AIQ	8-BIT, 300 MSPS ADC ±.75 LSB	CERQUAD	44	INDUSTRIAL
SPT7725BIQ	8-BIT, 300 MSPS ADC ±.95 LSB	CERQUAD	44	INDUSTRIAL
SPT7725AMJ	8-BIT, 300 MSPS ADC ±.75 LSB	SIDEBRAZED	42	MILITARY
SPT7725BMJ	8-BIT, 300 MSPS ADC ±.95 LSB	SIDEBRAZED	42	MILITARY
SPT7725AMQ	8-BIT, 300 MSPS ADC ±.75 LSB	CERQUAD	44	MILITARY
SPT7725BMQ	8-BIT, 300 MSPS ADC ±.95 LSB	CERQUAD	44	MILITARY
SPT7725AMJ/883	8-BIT, 300 MSPS ADC ±.75 LSB	SIDEBRAZED	42	MILITARY/883
SPT7725BMJ/883	8-BIT, 300 MSPS ADC ±.95 LSB	SIDEBRAZED	42	MILITARY/883
SPT7725AMQ/883	8-BIT, 300 MSPS ADC ±.75 LSB	CERQUAD	44	MILITARY/883
SPT7725BMQ/883	8-BIT, 300 MSPS ADC ±.95 LSB	CERQUAD	44	MILITARY/883
SPT7725BCU	8-BIT, 300 MSPS ADC ±.95 LSB	DIE		+25 °C
SPT7750AIG	8-BIT, 500 MSPS ADC ±1.0 LSB	PGA	68	INDUSTRIAL
SPT7750BIG	8-BIT, 500 MSPS ADC ±1.5 LSB	PGA	68	INDUSTRIAL
SPT7750AIK	8-BIT, 500 MSPS ADC ±1.0 LSB	MQUAD	80	INDUSTRIAL
SPT7750BIK	8-BIT, 500 MSPS ADC ±1.5 LSB	MQUAD	80	INDUSTRIAL
SPT7750BCU	8-BIT, 500 MSPS ADC ±1.5 LSB	DIE		+25 °C
SPT7755AIG	8-BIT, 750 MSPS ADC ±1.0 LSB	PGA	68	INDUSTRIAL
SPT7755BIG	8-BIT, 750 MSPS ADC ±1.5 LSB	PGA	68	INDUSTRIAL
SPT7755AIK	8-BIT, 750 MSPS ADC ±1.0 LSB	MQUAD	80	INDUSTRIAL
SPT7755BIK	8-BIT, 750 MSPS ADC ±1.5 LSB	MQUAD	80	INDUSTRIAL
SPT7755BCU	8-BIT, 750 MSPS ADC ±1.5 LSB	DIE		+25 °C

ORDERING INFORMATION

ANALOG-TO-DIGITAL CONVERTERS - Continued

PART NUMBER	DESCRIPTION	PACKAGE TYPE	# PINS	TEMPERATURE RANGE
SPT7760AIG	8-BIT, 1 GSPS ADC ±1.0 LSB	PGA	68	INDUSTRIAL
SPT7760BIG	8-BIT, 1 GSPS ADC ±1.5 LSB	PGA	68	INDUSTRIAL
SPT7760AIK	8-BIT, 1 GSPS ADC ±1.0 LSB	MQUAD	80	INDUSTRIAL
SPT7760BIK	8-BIT, 1 GSPS ADC ±1.5 LSB	MQUAD	80	INDUSTRIAL
SPT7760BCU	8-BIT, 1 GSPS ADC ±1.5 LSB	DIE		+25 °C
SPT7810AIJ	10-BIT, 20 MSPS ADC	SIDEBRAZED	28	INDUSTRIAL
SPT7810BIJ	10-BIT, 20 MSPS ADC	SIDEBRAZED	28	INDUSTRIAL
SPT7810ACN	10-BIT, 20 MSPS ADC	PLASTIC DIP	28	COMMERCIAL
SPT7810BCN	10-BIT, 20 MSPS ADC	PLASTIC DIP	28	COMMERCIAL
SPT7810BCU	10-BIT, 20 MSPS ADC	DIE		+25 °C
SPT7814AIJ	10-BIT, 40 MSPS ADC	SIDEBRAZED	28	INDUSTRIAL
SPT7814BIJ	10-BIT, 40 MSPS ADC	SIDEBRAZED	28	INDUSTRIAL
SPT7814ACN	10-BIT, 40 MSPS ADC	PLASTIC DIP	28	COMMERCIAL
SPT7814BCN	10-BIT, 40 MSPS ADC	PLASTIC DIP	28	COMMERCIAL
SPT7814BCU	10-BIT, 40 MSPS ADC	DIE		+25 °C
SPT7820AIJ	10-BIT, 20 MSPS ADC	SIDEBRAZED	28	INDUSTRIAL
SPT7820BIJ	10-BIT, 20 MSPS ADC	SIDEBRAZED	28	INDUSTRIAL
SPT7820AIC	10-BIT, 20 MSPS ADC	LCC	28	INDUSTRIAL
SPT7820BIC	10-BIT, 20 MSPS ADC	LCC	28	INDUSTRIAL
SPT7820ACN	10-BIT, 20 MSPS ADC	PLASTIC DIP	28	COMMERCIAL
SPT7820BCN	10-BIT, 20 MSPS ADC	PLASTIC DIP	28	COMMERCIAL
SPT7820ACS	10-BIT, 20 MSPS ADC	SOIC	28	COMMERCIAL
SPT7820BCS	10-BIT, 20 MSPS ADC	SOIC	28	COMMERCIAL
SPT7820AMJ	10-BIT, 20 MSPS ADC	SIDEBRAZED	28	MILITARY
SPT7820BMJ	10-BIT, 20 MSPS ADC	SIDEBRAZED	28	MILITARY
SPT7820AMJ/883	10-BIT, 20 MSPS ADC	SIDEBRAZED	28	MILITARY
SPT7820BMJ/883	10-BIT, 20 MSPS ADC	SIDEBRAZED	28	MILITARY
SPT7820BCU	10-BIT, 20 MSPS ADC	DIE		+25 °C
SPT7824AIJ	10-BIT, 40 MSPS ADC	SIDEBRAZED	28	INDUSTRIAL
SPT7824BIJ	10-BIT, 40 MSPS ADC	SIDEBRAZED	28	INDUSTRIAL
SPT7824AIC	10-BIT, 40 MSPS ADC	LCC	28	INDUSTRIAL
SPT7824BIC	10-BIT, 40 MSPS ADC	LCC	28	INDUSTRIAL
SPT7824ACN	10-BIT, 40 MSPS ADC	PLASTIC DIP	28	COMMERCIAL
SPT7824BCN	10-BIT, 40 MSPS ADC	PLASTIC DIP	28	COMMERCIAL
SPT7824ACS	10-BIT, 40 MSPS ADC	SOIC	28	COMMERCIAL
SPT7824BCS	10-BIT, 40 MSPS ADC	SOIC	28	COMMERCIAL
SPT7824AMJ	10-BIT, 40 MSPS ADC	SIDEBRAZED	28	MILITARY
SPT7824BMJ	10-BIT, 40 MSPS ADC	SIDEBRAZED	28	MILITARY
SPT7824AMJ/883	10-BIT, 40 MSPS ADC	SIDEBRAZED	28	MILITARY
SPT7824BMJ/883	10-BIT, 40 MSPS ADC	SIDEBRAZED	28	MILITARY
SPT7824BCU	10-BIT, 40 MSPS ADC	DIE*		+25 °C
SPT7830SCS	10-BIT, 2.5 MSPS ADC	SOIC	8	COMMERCIAL
SPT7830SCU	10-BIT, 2.5 MSPS ADC	DIE		+25 °C
SPT7835SCD	10-BIT, 5 MSPS ADC	CERDIP	28	COMMERCIAL
SPT7835SCN	10-BIT, 5 MSPS ADC	PLASTIC DIP	28	COMMERCIAL
SPT7835SCS	10-BIT, 5 MSPS ADC	SOIC	28	COMMERCIAL
SPT7835SCT	10-BIT, 5 MSPS ADC	TQFP	32	COMMERCIAL
SPT7835SCU	10-BIT, 5 MSPS ADC	DIE		+25 °C

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ANALOG-TO-DIGITAL CONVERTERS - Continued

PART NUMBER	DESCRIPTION	PACKAGE TYPE	# PINS	TEMPERATURE RANGE
SPT7840SCD	10-BIT, 10 MSPS ADC	CERDIP	28	COMMERCIAL
SPT7840SCN	10-BIT, 10 MSPS ADC	PLASTIC DIP	28	COMMERCIAL
SPT7840SCS	10-BIT, 10 MSPS ADC	SOIC	28	COMMERCIAL
SPT7840SCT	10-BIT, 10 MSPS ADC	TQFP	32	COMMERCIAL
SPT7840SCU	10-BIT, 10 MSPS ADC	DIE		+25 °C
SPT7850SCD	10-BIT, 20 MSPS ADC	CERDIP	28	COMMERCIAL
SPT7850SCN	10-BIT, 20 MSPS ADC	PLASTIC DIP	28	COMMERCIAL
SPT7850SCS	10-BIT, 20 MSPS ADC	SOIC	28	COMMERCIAL
SPT7850SCT	10-BIT, 20 MSPS ADC	TQFP	32	COMMERCIAL
SPT7850SCU	10-BIT, 20 MSPS ADC	DIE		+25 °C
SPT7852SCT	DUAL, 10-BIT, 20 MSPS ADC	TQFP	44	COMMERCIAL
SPT7852SCU	DUAL, 10-BIT, 20 MSPS ADC	DIE		+25 °C
SPT7855SCD	10-BIT, 25 MSPS ADC	CERDIP	28	COMMERCIAL
SPT7855SCN	10-BIT, 25 MSPS ADC	PLASTIC DIP	28	COMMERCIAL
SPT7855SCS	10-BIT, 25 MSPS ADC	SOIC	28	COMMERCIAL
SPT7855SCT	10-BIT, 25 MSPS ADC	TQFP	32	COMMERCIAL
SPT7855SCU	10-BIT, 25 MSPS ADC	DIE		+25 °C
SPT7860SCD	10-BIT, 40 MSPS ADC	CERDIP	28	COMMERCIAL
SPT7860SCN	10-BIT, 40 MSPS ADC	PLASTIC DIP	28	COMMERCIAL
SPT7860SCS	10-BIT, 40 MSPS ADC	SOIC	28	COMMERCIAL
SPT7860SCT	10-BIT, 40 MSPS ADC	TQFP	32	COMMERCIAL
SPT7860SCU	10-BIT, 40 MSPS ADC	DIE		+25 °C
SPT7861SCN	10-BIT, 40 MSPS ADC	PLASTIC DIP	28	COMMERCIAL
SPT7861SCS	10-BIT, 40 MSPS ADC	SOIC	28	COMMERCIAL
SPT7861SCT	10-BIT, 40 MSPS ADC	TQFP	32	COMMERCIAL
SPT7861SCU	10-BIT, 40 MSPS ADC	DIE		+25 °C
SPT7870SCJ	10-BIT, 100 MSPS ADC	SIDEBRAZED	32	COMMERCIAL
SPT7870SCQ	10-BIT, 100 MSPS ADC	CERQUAD	44	COMMERCIAL
SPT7870SCU	10-BIT, 100 MSPS ADC	DIE		+25 °C
SPT7871SCJ	10-BIT, 100 MSPS ADC	SIDEBRAZED	32	COMMERCIAL
SPT7871SCQ	10-BIT, 100 MSPS ADC	CERQUAD	44	COMMERCIAL
SPT7871SCU	10-BIT, 100 MSPS ADC	DIE		+25 °C
SPT7910SCJ	12-BIT, 10 MSPS ECL ADC	SIDEBRAZED	32	COMMERCIAL
SPT7910SCU	12-BIT, 10 MSPS ECL ADC	DIE*		+25 °C
SPT7912SCJ	12-BIT, 30 MSPS ECL ADC	SIDEBRAZED	32	COMMERCIAL
SPT7912SCU	12-BIT, 30 MSPS ECL ADC	DIE*		+25 °C
SPT7920SCJ	12-BIT, 10 MSPS TTL ADC	SIDEBRAZED	32	COMMERCIAL
SPT7920SCQ	12-BIT, 10 MSPS TTL ADC	CERQUAD	44	COMMERCIAL
SPT7920SMJ	12-BIT, 10 MSPS TTL ADC	SIDEBRAZED	32	MILITARY
SPT7920SCU	12-BIT, 10 MSPS TTL ADC	DIE*		+25 °C
SPT7921SCJ	12-BIT, 20 MSPS TTL ADC	SIDEBRAZED	32	COMMERCIAL
SPT7921SCQ	12-BIT, 20 MSPS TTL ADC	CERQUAD	44	COMMERCIAL
SPT7921SMJ	12-BIT, 20 MSPS TTL ADC	SIDEBRAZED	32	MILITARY
SPT7921SCU	12-BIT, 20 MSPS TTL ADC	DIE*		+25 °C
SPT7922SCJ	12-BIT, 30 MSPS TTL ADC	SIDEBRAZED	32	COMMERCIAL
SPT7922SCQ	12-BIT, 30 MSPS TTL ADC	CERQUAD	44	COMMERCIAL
SPT7922SMJ	12-BIT, 30 MSPS TTL ADC	SIDEBRAZED	32	MILITARY
SPT7922SCU	12-BIT, 30 MSPS TTL ADC	DIE*		+25 °C
SPT7930SCJ	12-BIT, 5 MSPS TTL ADC	SIDEBRAZED	28	COMMERCIAL
SPT7930SCS	12-BIT, 5 MSPS TTL ADC	SOIC	28	COMMERCIAL
SPT7930SCU	12-BIT, 5 MSPS TTL ADC	DIE		+25 °C

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ORDERING INFORMATION

DIGITAL-TO-ANALOG CONVERTERS

PART NUMBER	DESCRIPTION	PACKAGE TYPE	# PINS	TEMPERATURE RANGE
SPT5100SCT	DUAL, 8-BIT, 20 MWPS	TQFP	32	COMMERCIAL
SPT5110SCT	TRIPLE, 8-BIT, 30 MWPS	TQFP	48	COMMERCIAL
SPT1018AIN	8-BIT, 275 MWPS DAC	PLASTIC DIP	24	INDUSTRIAL
SPT1018BIN	8-BIT, 165 MWPS DAC	PLASTIC DIP	24	INDUSTRIAL
SPT1018AMJ	8-BIT, 275 MWPS DAC	CERDIP	24	MILITARY
SPT1018BMJ	8-BIT, 165 MWPS DAC	CERDIP	24	MILITARY
SPT1018AMJ/883	8-BIT, 275 MWPS DAC	CERDIP	24	MILITARY
SPT1018BMJ/883	8-BIT, 165 MWPS DAC	CERDIP	24	MILITARY
SPT1019AIN	8-BIT, 275 MWPS DAC W/REF	PLASTIC DIP	24	INDUSTRIAL
SPT1019BIN	8-BIT, 165 MWPS DAC W/REF	PLASTIC DIP	24	INDUSTRIAL
SPT1019AMJ	8-BIT, 275 MWPS DAC W/REF	CERDIP	24	MILITARY
SPT1019BMJ	8-BIT, 165 MWPS DAC W/REF	CERDIP	24	MILITARY
SPT1019AMJ/883	8-BIT, 275 MWPS DAC W/REF	CERDIP	24	MILITARY
SPT1019BMJ/883	8-BIT, 165 MWPS DAC W/REF	CERDIP	24	MILITARY
SPT5140SIN	8-BIT, 400 MWPS DAC W/REF	PLASTIC DIP	24	INDUSTRIAL
SPT5140SMJ	8-BIT, 400 MWPS DAC W/REF	CERDIP	24	MILITARY
SPT5140SMJ/883	8-BIT, 400 MWPS DAC W/REF	CERDIP	24	MILITARY
SPT5220SCN	10-BIT, 80 MWPS	PLASTIC DIP	28	COMMERCIAL
SPT5230SCT	TRIPLE, 10-BIT, 50 MWPS	SQFP	52	COMMERCIAL
SPT9712SIN	12-BIT, 100 MWPS ECL DAC	PLASTIC DIP	28	INDUSTRIAL
SPT9712SIP	12-BIT, 100 MWPS ECL DAC	PLCC	28	INDUSTRIAL
SPT9712SCU	12-BIT, 100 MWPS ECL DAC	DIE		COMMERCIAL
SPT9713SIN	12-BIT, 100 MWPS TTL DAC	PLASTIC DIP	28	INDUSTRIAL
SPT9713SIP	12-BIT, 100 MWPS TTL DAC	PLCC	28	INDUSTRIAL
SPT9713SCU	12-BIT, 100 MWPS TTL DAC	DIE		COMMERCIAL
SPT5216BCJ	16-BIT RES DAC W/REF	SIDEBRAZED	32	COMMERCIAL
SPT5216CCJ	16-BIT RES DAC W/REF	SIDEBRAZED	32	COMMERCIAL
SPT5216BCQ	16-BIT RES DAC W/REF	CERQUAD	44	COMMERCIAL
SPT5216CCQ	16-BIT RES DAC W/REF	CERQUAD	44	COMMERCIAL
SPT5216CCU	16-BIT RES DAC W/REF	DIE		+25 °C

COMPARATORS

PART NUMBER	DESCRIPTION	PACKAGE TYPE	# PINS	TEMPERATURE RANGE
HCMP96850SID	HIGH-SPEED COMPARATOR	CERDIP	16	INDUSTRIAL
HCMP96850SCU	HIGH-SPEED COMPARATOR	DIE		+25 °C
SPT9687SIC	DUAL HIGH-SPEED COMPARATOR	LCC	20	INDUSTRIAL
SPT9687SID	DUAL HIGH-SPEED COMPARATOR	CERDIP	16	INDUSTRIAL
SPT9687SIJ	DUAL HIGH-SPEED COMPARATOR	SIDEBRAZED	16	INDUSTRIAL
SPT9687SIN	DUAL HIGH-SPEED COMPARATOR	PLASTIC DIP	16	INDUSTRIAL
SPT9687SIP	DUAL HIGH-SPEED COMPARATOR	PLCC	20	INDUSTRIAL
SPT9687SCU	DUAL HIGH-SPEED COMPARATOR	DIE		+25 °C
SPT9689AIJ	SUB-NANOSECOND COMPARATOR	SIDEBRAZED	16	INDUSTRIAL
SPT9689BIJ	SUB-NANOSECOND COMPARATOR	SIDEBRAZED	16	INDUSTRIAL
SPT9689AIC	SUB-NANOSECOND COMPARATOR	LCC	20	INDUSTRIAL
SPT9689BIC	SUB-NANOSECOND COMPARATOR	LCC	20	INDUSTRIAL
SPT9689AIP	SUB-NANOSECOND COMPARATOR	PLCC	20	INDUSTRIAL
SPT9689BIP	SUB-NANOSECOND COMPARATOR	PLCC	20	INDUSTRIAL
SPT9689BCU	SUB-NANOSECOND COMPARATOR	DIE		+25 °C

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COMPARATORS

PART NUMBER	DESCRIPTION	PACKAGE TYPE	# PINS	TEMPERATURE RANGE
SPT9691SCJ	2NS, JFET COMPARATOR	SIDEBRAZED	20	COMMERCIAL
SPT9691SCC	2NS, JFET COMPARATOR	LCC	20	COMMERCIAL
SPT9691SCN	2NS, JFET COMPARATOR	PLASTIC DIP	20	COMMERCIAL
SPT9691SCP	2NS, JFET COMPARATOR	PLCC	20	COMMERCIAL
SPT9691SCU	2NS, JFET COMPARATOR	DIE	20	+25 °C
SPT9693SCJ	1NS, JFET COMPARATOR	SIDEBRAZED	20	COMMERCIAL
SPT9693SCC	1NS, JFET COMPARATOR	LCC	20	COMMERCIAL
SPT9693SCP	1NS, JFET COMPARATOR	PLCC	20	COMMERCIAL
SPT9693SCU	1NS, JFET COMPARATOR	DIE	20	+25 °C

PIN DRIVERS

PART NUMBER	DESCRIPTION	PACKAGE TYPE	# PINS	TEMPERATURE RANGE
SPT9500SCP	300 MHz PIN DRIVER	PLCC	28	COMMERCIAL
SPT9500SCU	300 MHz PIN DRIVER	DIE		+25 °C

SAMPLE-AND-HOLDS

PART NUMBER	DESCRIPTION	PACKAGE TYPE	# PINS	TEMPERATURE RANGE
SPT9101SIC	125 MSPS SAMPLING AMPLIFIER	LCC	28	INDUSTRIAL
SPT9101SIS	125 MSPS SAMPLING AMPLIFIER	SOIS	28	INDUSTRIAL
SPT9101SCU	125 MSPS SAMPLING AMPLIFIER	DIE		+25 °C

EVALUATION BOARDS

EB1175	SPT1175 DEMO BOARD
EB5220	SPT5220 DEMO BOARD
EB7610	SPT7610 DEMO BOARD
EB7710/25	SPT7710/25 DEMO BOARD
EB7750/55/60	SPT7750/55/60 DEMO BOARD
EB7810/14	SPT7810/7814 DEMO BOARD
EB7820/24	SPT7820/7824 DEMO BOARD
EB7830	SPT7830 DEMO BOARD
EB7835/40/50/55/60	SPT7835/40/50/55/60 DEMO BOARD
EB7870	SPT7870 DEMO BOARD
EB7871	SPT7871 DEMO BOARD
EB7910/12	SPT7910/7912 DEMO BOARD
EB7920/22	SPT7920/7922 DEMO BOARD
EB9101	SPT9101 DEMO BOARD
EB9712	SPT9712 DEMO BOARD
EB9713	SPT9713 DEMO BOARD

LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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Section 3 Analog-to-Digital Converters

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SIGNAL PROCESSING TECHNOLOGIES

HADC574Z

FAST, COMPLETE 12-BIT µP COMPATIBLE A/D CONVERTER WITH SAMPLE/HOLD

3

FEATURES

- Improved Pin-To-Pin Compatible Monolithic Version of the HI574A and AD574A
- Complete 12-Bit A/D Converter with Sample/Hold, Reference and Clock
- Low Power Dissipation (150 mW Max)
- 12-Bit Linearity (Over Temp)
- 25 µs Max Conversion Time
- No Negative Supply Required
- Full Bipolar and Unipolar Input Range

APPLICATIONS

- Military/Industrial Data Acquisition Systems
- 8 or 12-Bit µP Input Functions
- Process Control Systems
- Test and Scientific Instruments
- Personal Computer Interface

GENERAL DESCRIPTION

The HADC574Z is a complete, 12-bit successive approximation A/D converter. The device is integrated on a *single die* to make it the first monolithic CMOS version of the industry standard devices, HI574A and AD574A. Included on chip are an internal reference, clock, and a sample-and-hold. The S/H is an additional feature not available on similar devices.

The HADC574Z features 25 µs (max) conversion time of 10 or 20 volt input signals. Also, a three-state output buffer is added for direct interface to an 8, 12, or 16-bit µP bus.

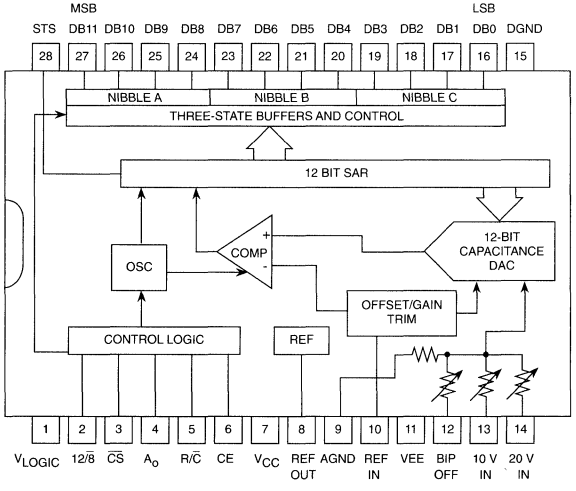
The HADC574Z is manufactured on a Bipolar Enhanced CMOS process (BEMOS) which combines CMOS logic and fast bipolar npn transistors to yield high performance digital and analog functions on one chip.

The BEMOS process and monolithic construction reduces power consumption and ground noise and keeps parasitics to a minimum. In addition, the thin film option on this process allows active adjustment of DAC and comparator offsets, linearity errors, and gain errors.

The HADC574Z has standard bipolar and unipolar input ranges of 10 V and 20 V that are controlled by a bipolar offset pin and laser trimmed for specified linearity, gain and offset accuracy.

Power requirements are +5 V and +12 V to +15 V with a maximum dissipation of 150 mW at the specified voltages. Power consumption is about five times lower than that of currently available devices, and a negative power supply is not needed. A standard military drawing is published under DESC number 5962-81527.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING (Beyond which damage may occur) [1] 25 °C

Supply Voltages

Positive Supply Voltage (V_{CC} to DGND) ..... 0 to +16.5 V
Logic Supply Voltage (V_{LOGIC} to DGND) ..... 0 to +7 V
Analog to Digital Ground (AGND to DGND) . -0.5 to +1 V

Input Voltages

Control Input Voltages (to DGND)
(CE, CS, Ao, 12/8, R/C) ..... -0.5 to V_{LOGIC} +0.5 V
Analog Input Voltage (to AGND)
(REF IN, BIP OFF, 10 Vin) ..... ±16.5 V
20 V Vin Input Voltage (to AGND) ..... ±24 V

Output

Reference Output Voltage ..... Indefinite short to GND
Momentary short to V_{CC}

Temperature

Operating Temperature, ambient ..... -55 to +125 °C
junction ..... +175 °C
Lead Temperature, (soldering 10 seconds)..... +300 °C
Storage Temperature ..... -65 to +150 °C
Power Dissipation..... 1000 mW
Thermal Resistance (θ_{jA}) ..... 48 °C/W

Note: Operation at any Absolute Maximum Rating is not implied. See Operating Conditions for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

T_A=T_{MIN} to T_{MAX}, V_{CC}=+15 V or +12 V, V_{LOGIC}=+5 V, unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEST LEVEL	HADC574ZC MIN	HADC574ZC TYP	HADC574ZC MAX	HADC574ZB MIN	HADC574ZB TYP	HADC574ZB MAX	HADC574ZA MIN	HADC574ZA TYP	HADC574ZA MAX	UNITS
DC ELECTRICAL CHARACTERISTICS												
Resolution		VI			12			12			12	BITS
Linearity Error[1]	T_A=0 to 70 °C	VI			±1			±1/2			±1/2	LSB
	T_A = -25 to +85 °C	I			±1			±1/2			±1/2	LSB
	T_A = -55 to +125 °C	I			±1			±1			±1	LSB
Differential Linearity	No Missing Codes	VI	11			12			12			BITS
Unipolar Offset; 10 V, 20 V	+25 °C Adjustable to Zero	VI		±0.1	±2		±0.1	±2		±0.1	±2	LSB
Bipolar Offset1; ±5 V, ±10 V	+25 °C Adjustable to Zero	VI			±10			±4			±4	LSB
Full Scale Calibration Error[2] All Input Ranges	+25 °C Adjustable to Zero	VI			0.3			0.3			0.3	% of FS
	No Adjustment at +25°											
	T_A = 0 to 70 °C	V		0.5			0.4			0.35		%of FS
	T_A = -25 to +85 °C	V		0.7			0.5			0.4		%of FS
	T_A = -55 to +125 °C	V		0.8			0.6			0.4		%of FS
	With Adjustment at +25 °C											
	T_A = 0 to 70 °C	V		0.22			0.12			0.05		%of FS
	T_A = -25 to +85 °C	V		0.4			0.2			0.1		%of FS
	T_A = -55 to +125 °C	V		0.5			0.25			0.12		%of FS
Temperature Coefficients[3]	Using Internal Reference											
Unipolar Offset	T_A = 0 to 70 °C	IV		±0.2	±2		±0.1	±1		±0.1	±1	LSB
					(10)			(5)			(5)	(ppm/°C)
	T_A = -25 to +85 °C	IV			±2			±1			±1	LSB
					(5)			(2.5)			(2.5)	(ppm/°C)
	T_A = -55 to +125 °C	IV			±2			±1			±1	LSB
					(5)			(2.5)			(2.5)	(ppm/°C)
Bipolar Offset	T_A = 0 to 70 °C	IV		±0.2	±2		±0.1	±1		±0.1	±1	LSB
					(10)			(5)			(5)	(ppm/°C)
	T_A = -25 to +85 °C	IV			±2			±1			±1	LSB
					(5)			(2.5)			(2.5)	(ppm/°C)

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ELECTRICAL SPECIFICATIONS

$T_A = T_{MIN}$ to T_{MAX}, V_{CC} = +15 V or +12 V, V_{LOGIC} = +5 V, unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEST LEVEL	HADC574ZC MIN	HADC574ZC TYP	HADC574ZC MAX	HADC574ZB MIN	HADC574ZB TYP	HADC574ZB MAX	HADC574ZA MIN	HADC574ZA TYP	HADC574ZA MAX	UNITS
DC ELECTRICAL CHARACTERISTICS												
Bipolar Offset (Cont.)	T_A = -55 to +125 °C	IV			±4 (10)			±2 (5)			±1 (2.5)	LSB (ppm/°C)
Full Scale Calibration	T_A = 0 to 70 °C	IV			±9 (45)			±5 (25)			±2 (10)	LSB (ppm/°C)
	T_A = -25 to +85 °C	IV			±12 (50)			±7 (25)			±3 (12)	LSB (ppm/°C)
	T_A = -55 to +125 °C	IV			±20 (50)			±10 (25)			±5 (12.5)	LSB (ppm/°C)
Power Supply Rejection	Max change in full scale calibration											
+13.5 V<V_{CC}<+16.5 V or +11.4 V<V_{CC}<+12.6 V		VI		±0.5	±2		±0.5	±1		±0.5	±1	LSB
+4.5 V<V_{LOGIC}<+5.5 V		VI		±0.1	±0.5		±0.1	±0.5		±0.1	±0.5	LSB
Analog Input Ranges												
Bipolar		VI	-5		+5	-5		+5	-5		+5	Volts
			-10		+10	-10		+10	-10		+10	Volts
Unipolar		VI	0		+10	0		+10	0		+10	Volts
			0		+20	0		+20	0		+20	Volts
Input Impedance 10 Volt Span 20 Volt Span		VI	 3.75 15	 5 20	 6.25 25	 3.75 15	 5 20	 6.25 25	 3.75 15	 5 20	 6.25 25	 kΩ kΩ
Power Supplies Operating Voltage Range												
V_{LOGIC}		VI	+4.5		+5.5	+4.5		+5.5	+4.5		+5.5	Volts
V_{CC}		VI	+11.4		+16.5	+11.4		+16.5	+11.4		+16.5	Volts
V_{EE}	Not required for circuit operation											
Operating Current												
I_{LOGIC}		VI		0.5	1		0.5	1		0.5	1	mA
I_{CC}		VI		7	9		7	9		7	9	mA
I_{EE}	Not required for circuit operation											
Power Dissipation +15 V, +5 V		VI		110	150		110	150		110	150	mW
Internal Reference Voltage Output Current[4]		VI VI	9.97	10	10.03 2	9.97	10	10.03 2	9.97	10	10.03 2	Volts mA

ELECTRICAL SPECIFICATIONS

$T_A = T_{MIN}$ to T_{MAX}, V_{CC} = +15 V or +12 V, V_{LOGIC} = +5 V, unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEST LEVEL	HADC574ZC MIN	HADC574ZC TYP	HADC574ZC MAX	HADC574ZB MIN	HADC574ZB TYP	HADC574ZB MAX	HADC574ZA MIN	HADC574ZA TYP	HADC574ZA MAX	UNITS
DIGITAL CHARACTERISTICS												
Logic Inputs (CE, $\overline{CS}$, R/$\overline{C}$, Ao, 12/$\overline{8}$)												
	Logic "0"	VI	-0.5		+0.8	-0.5		+0.8	-0.5		+0.8	Volts
	Logic "1"	VI	2.0		5.5	2.0		5.5	2.0		5.5	Volts
Current	0 to 5.5 V Input	VI		±.01	+1		±.01	+1		±.01	+1	µA
Capacitance		V		5			5			5		pF
Logic Outputs (DB11-DB0, STS)												
Logic "0"	(I_{Sink} = 1.6 mA)	VI			+0.4			+0.4			+0.4	Volts
Logic "1"	(I_{SOURCE} = 500 µA)	VI	+2.4			+2.4			+2.4			Volts
Leakage	(High Z State, DB11-DB0 Only)	VI	-5	±0.1	+5	-5	±0.1	+5	-5	±0.1	+5	µA
Capacitance		V		5			5			5		pF

Note 1: For military temperature range, the device linearity is guaranteed to be 1/2 LSB at 25 °C.
Note 2: Fixed 50 Ω resistor from REF OUT to REF IN and REF OUT to BIP OFF.
Note 3: Full Tempco testing is performed on all Grade A and MIL-STD-883 devices.
Note 4: Available for external loads; external load should not change during conversion. When supplying an external load and operating on a +12.0 V supply, a buffer amplifier must be provided for the reference output.

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ELECTRICAL SPECIFICATIONS

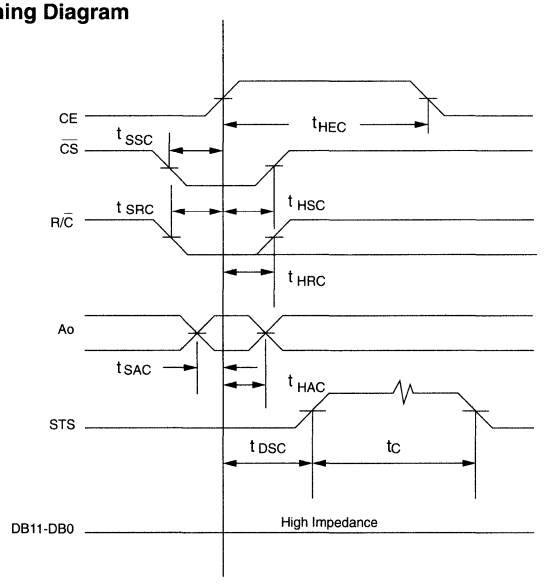
CONVERT MODE TIMING CHARACTERISTICS

T_A = +25 °C, V_{CC} = +15.0 V or +12 V, V_{LOGIC} = +5 V, unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEST LEVEL	HADC574ZC MIN	HADC574ZC TYP	HADC574ZC MAX	HADC574ZB MIN	HADC574ZB TYP	HADC574ZB MAX	HADC574ZA MIN	HADC574ZA TYP	HADC574ZA MAX	UNITS
AC ELECTRICAL CHARACTERISTICS[5]												
t_{DSC} STS Delay from CE		I			200			200			200	ns
t_{HEC} CE Pulse Width		I	50			50			50			ns
t_{SSC} $\overline{CS}$ to CE Setup		I	50			50			50			ns
t_{HSC} $\overline{CS}$ Low during CE High		I	50			50			50			ns
t_{SRC} R/$\overline{C}$ to CE Setup		I	50			50			50			ns
t_{HRC} R/$\overline{C}$ Low During CE High		I	50			50			50			ns
t_{SAC} Ao to CE Setup		I	0			0			0			ns
t_{HAC} Ao Valid During CE High		I	50			50			50			ns
t_C Conversion Time												
12-Bit Cycle	T_{MIN} to T_{MAX}	I	13	18	25	15	18	25	15	18	25	µs
8-Bit Cycle	T_{MIN} to T_{MAX}	I	10	13	19	10	13	17	10	13	17	µs

Note 5: Time is measured from 50% level of digital transitions. Paramaters are tested with a 100 pF and 3 kΩ load for high impedance to drive and tested with 10 pF and 3 kΩ load for drive to high impedance.

Figure 1 - Convert Mode Timing Diagram



ELECTRICAL SPECIFICATIONS

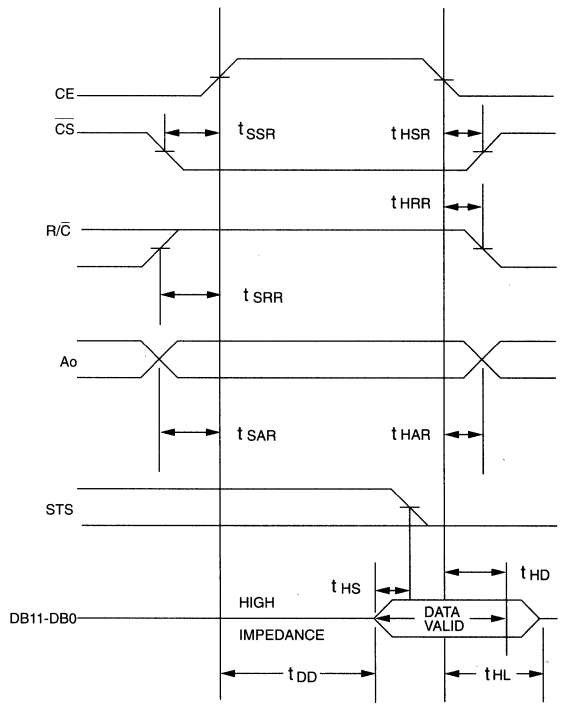
READ MODE TIMING CHARACTERISTICS

T_A = 25 °C, V_{CC} = +15.0 V or +12 V, V_{LOGIC} = +5 V, unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEST LEVEL	HADC574ZC MIN	HADC574ZC TYP	HADC574ZC MAX	HADC574ZB MIN	HADC574ZB TYP	HADC574ZB MAX	HADC574ZA MIN	HADC574ZA TYP	HADC574ZA MAX	UNITS
AC ELECTRICAL CHARACTERISTICS[6]												
t_{DD} Access Time from CE		I			150			150			150	ns
t_{HD} Data Valid After CE Low		I	25			25			25			ns
t_{HL} Output Float Delay		I			150			150			150	ns
t_{SSR} $\overline{CS}$ to CE Setup		I	50	0		50	0		50	0		ns
t_{SRR} R/$\overline{C}$ to CE Setup		I	0	0		0	0		0	0		ns
t_{SAR} Ao to CE Setup		I	50			50			50			ns
t_{HSR} $\overline{CS}$ Valid After CE Low		I	0	0		0	0		0	0		ns
t_{HRR} R/$\overline{C}$ High After CE Low		I	50			50			50			ns
t_{HS} STS Delay After Data Valid		I	300		1000	300		1000	300		1000	ns
t_{HAR} Ao Valid after CE Low		I	50			50			50			ns

Note 6: Time is measured from 50% level of digital transitions. Parameters are tested with a 100 pF and 3 kΩ load for high impedance to drive and tested with 10 pF and 3 kΩ load for drive to high impedance.

Figure 2 - Read Mode Timing Diagram



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ELECTRICAL SPECIFICATIONS

STAND-ALONE MODE TIMING CHARACTERISTICS

T_A = 25 °C, V_{CC} = +15.0 V or +12 V, V_{LOGIC} = +5 V, unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEST LEVEL	HADC574ZC MIN	HADC574ZC TYP	HADC574ZC MAX	HADC574ZB MIN	HADC574ZB TYP	HADC574ZB MAX	HADC574ZA MIN	HADC574ZA TYP	HADC574ZA MAX	UNITS
AC ELECTRICAL CHARACTERISTICS[6]												
t_{HRL} Low R/$\overline{C}$ Pulse Width		I	50			50			50			ns
t_{DS} STS Delay from R/$\overline{C}$		I			200			200			200	ns
t_{HDR} Data Valid After R/$\overline{C}$ Low		I	25			25			25			ns
t_{HS} STS Delay After Data Valid		I	300		1000	300		1000	300		1000	ns
t_{HRH} High R/$\overline{C}$ Pulse Width		I	150			150			150			ns
t_{DDR} Data Access Time		I			150			150			150	ns
SAMPLE AND HOLD												
Acquisition Time		IV	1.8	2.4	3.4	1.8	2.4	3.4	1.8	2.4	3.4	µs
Aperture Uncertainty Time		V		8			8			8		ns,RMS

Figure 3 - Low Pulse for R/$\overline{C}$ - Outputs Enabled After Conversion

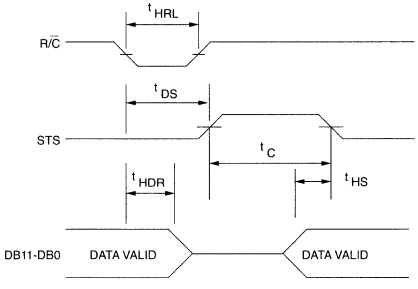
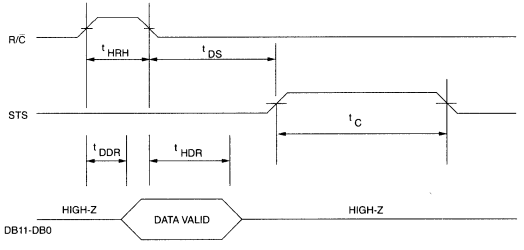


Figure 4 - High Pulse for R/$\overline{C}$ - Outputs Enabled While R/$\overline{C}$ is High, Otherwise High Impedance



TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests; therefore, $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

DEFINITION OF SPECIFICATIONS

INTEGRAL LINEARITY ERROR

Linearity error refers to the deviation of each individual code from a line drawn from zero through full scale with all offset errors nulled out. (See figures 5 and 6.) The point used as zero occurs 1/2 LSB (1.22 mV for a 10 volt span) before the first code transition (all zeros to only the LSB on). Full scale is defined as a level 1 and 1/2 LSB beyond the last code transition (to all ones). The deviation of a code from the true straight line is measured from the middle of each particular code.

The HADC574ZAC and BC grades are guaranteed for maximum nonlinearity of ±1/2 LSB. For these grades, this means that an analog value that falls exactly in the center of a given code width will result in the correct digital output code. Values nearer the upper or lower transition of the code width may produce the next upper or lower digital output code. The HADC574ZAM, BM, CC and CM grades are guaranteed to ±1 LSB maximum error. For these grades, an analog value that falls within a given code width will result in either the correct code for the region or either adjacent one. The linearity is not user-adjustable.

DIFFERENTIAL LINEARITY ERROR (NO MISSING CODES)

A specification that guarantees no missing codes requires that every code combination appear in a monotonically increasing sequence as the analog input level is increased. Thus every code must have a finite width. For the HADC574Z type AC, BC, AM and BM grades that guarantee no missing codes to 12-bit resolution, all 4096 codes must be present over the entire operating temperature ranges. The HADC574Z CC and CM grades guarantee no missing codes to 11-bit resolution over temperature; this means that all code combinations of the upper 11-bits must be present. In practice, very few of the 12-bit codes are missing.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is a measure of how much the actual quantization step width varies from the ideal step width of 1 LSB. Figure 6 shows a differential nonlinearity of 2 LSB - the actual step width is 3 LSB. The HADC574Z's specification gives the worst case differential nonlinearity in the A/D transfer function under specified dynamic operating conditions. Small, localized differential nonlinearities may be insignificant when digitizing full scale signals. However, if a low level input signal happens to fall on the part of the A/D transfer function with the differential nonlinearity error, the effect will be significant.

MISSING CODES

Missing codes represent a special kind of differential nonlinearity. The quantization step width for a missing code is 0 LSB which results in a differential nonlinearity of -1 LSB. Figure 6 points out two missed codes in the transfer function.

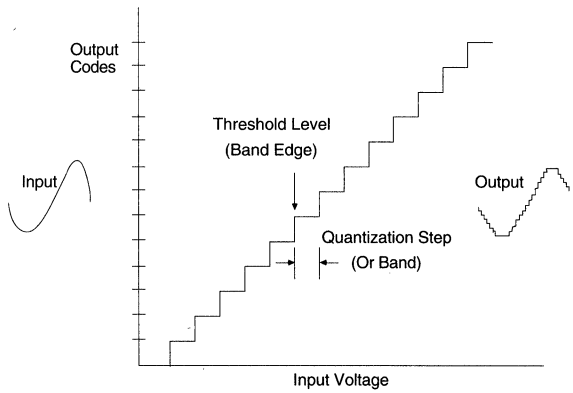
QUANTIZATION UNCERTAINTY

Analog-to-digital converters exhibit an inherent quantization uncertainty of ±1/2 LSB. This uncertainty is a fundamental characteristic of the quantization process and cannot be reduced for a converter of a given resolution.

QUANTIZATION ERROR

Quantization error is the fundamental, irreducible error associated with the perfect quantizing of a continuous (analog) signal into a finite number of digital bits (A/D transfer function). A 12-bit A/D converter can represent an input voltage with a best case uncertainty of 1 part in 2^{12} (1 part in 4096). In real A/Ds under dynamic operating conditions, the quantization bands (bit change step vs input amplitude) for certain codes can be significantly larger (or smaller) than the ideal. The ideal width of each quantization step (or band) is $Q=FSR/2^N$ where FSR=full scale range and N=12. Nonideal quantization bands represent differential non linearity errors. (See figures 5, 6 and 7.)

Figure 5 - Static Input Conditions



RESOLUTION - ACTUAL vs AVAILABLE

The available resolution of an N-bit converter is 2^N. This means it is theoretically possible to generate 2^N unique output codes.

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Figure 6 - Dynamic Conditions

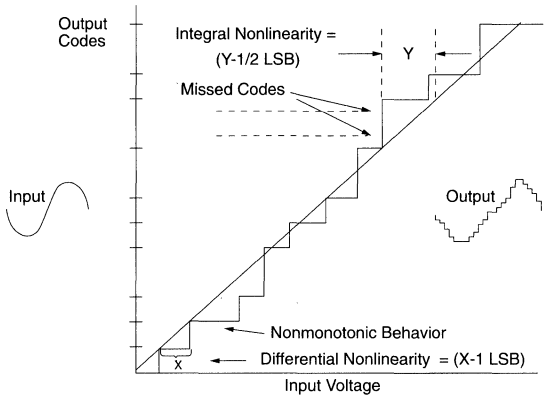
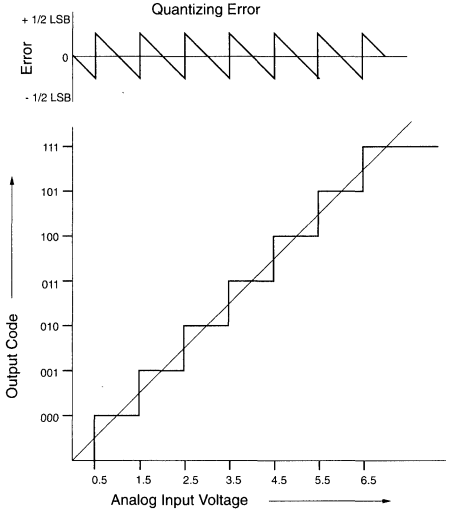


Figure 7 - Quantizing Error



THROUGHPUT

Maximum throughput is the greatest number of conversions per second at which an ADC will deliver its full rate performance. This is equivalent to the inverse of the sum of the multiplex time (if applicable), the S/H settling time and the conversion time.

GAIN

Gain is the slope of the transfer curve. Gain is generally user adjustable to compensate for long term drift.

ACQUISITION TIME/APERTURE DELAY TIME

In the HADC574Z, this is the time delay between the R/$\overline{C}$ falling edge and the actual start of the hold mode in a sample and hold function.

APERTURE JITTER

This is a specification indicating how much the aperture delay time varies between samples.

SUCCESSIVE APPROXIMATION ADC

The successive approximation converter uses an architecture with inherently high throughput rates that converts high frequency signals with great accuracy. A sample-and-hold type circuit can be used on the input to freeze these signals during conversion.

An N-bit successive approximation converter performs a sequence of tests comparing the input voltage to a successively narrower voltage range. The first range is half full scale, the next is quarter full scale, etc., until it reaches the Nth test which narrows it to a range of $1/2^N$ of full scale. The conversion time is fixed by the clock frequency and is thus independent of the input voltage.

UNIPOLAR OFFSET

The first transition should occur at a level 1/2 LSB above analog common. Unipolar offset is defined as the deviation of the actual transition from that point. This offset can be adjusted as discussed on the following pages. The unipolar offset temperature coefficient specifies the maximum change of the transition point over temperature, with and without external adjustment.

BIPOLAR OFFSET

The major carry transition (0111 1111 1111 to 1000 0000 0000) in the bipolar mode should occur for an analog value 1/2 LSB below analog common. The bipolar offset error and temperature coefficient specify the initial deviation and maximum change in the error over temperature.

CONVERSION TIME

This is the time required to complete a conversion over the specified operating range. Conversion time can be expressed as time/bit for a converter with selectable resolution or as time/conversion when the number of bits is constant. The HADC574Z is specified as time/conversion for all 12-bits. Conversion time should not be confused with maximum allowable analog input frequency which is discussed later.

FULL SCALE CALIBRATION ERROR

The last transition (from 1111 1111 1110 to 1111 1111 1111 1111) should occur for an analog value 1 and 1/2 LSB below the nominal full scale (9.9963 volts for 10.000 volts full scale). The full scale calibration error is the deviation of the actual level at the last transition from the ideal level. This error, which typically is 0.05 to 0.1% of full scale, can be trimmed out as show in figures 11 and 12. The full scale calibration error over temperature is given with and without the initial error trimmed out. The temperature coefficients for each grade indicate the maximum change in the full scale gain from the initial value using the internal 10 volt reference.

TEMPERATURE COEFFICIENTS

The temperature coefficients for full scale calibration, unipolar offset, and bipolar offset specify the maximum change from the initial (25 °C) value to the value at T_{MIN} or T_{MAX}.

POWER SUPPLY REJECTION

The standard specifications for the HADC574Z assume +5.00 and +15.00 or +12.00 volt supplies. The only effect of power supply error on the performance of the device will be a small change in the full scale calibration. This will result in a linear change in all lower order codes. The specifications show the maximum change in calibration from the initial value with the supplies at the various limits.

CODE WIDTH

The fundamental unit for A/D converter specifications is the code width. This is defined as the range of analog input values for which a given digital output code will occur. The nominal value of a code width is equivalent to one least significant bit (LSB) of the full scale range or 2.44 mV out of 10 volts for a 12-bit ADC.

LEFT-JUSTIFIED DATA

The data format used in the HADC574Z is left-justified. This means that the data represents the analog input as fraction of full scale, ranging from 0 to 4095/4096. This implies a binary point to the left of the MSB.

MONOTONICITY

This characteristic describes an aspect of the code to code progression from minimum to maximum input. A device is said to be monotonic if the output code continuously increases as the input signal increases, and if the output code continuously decreases as the input signal decreases. Figure 6 demonstrates nonmonotonic behavior.

CIRCUIT OPERATION

The HADC574Z is a complete 12-bit analog-to-digital converter that consists of a single chip version of the industry standard 574. This single chip contains a precision 12-bit capacitor digital-to-analog converter (CDAC) with voltage reference, comparator, successive approximation register (SAR), sample-and-hold, clock, output buffers and control circuitry to make it possible to use the HADC574Z with few external components.

When the control section of the HADC574Z initiates a conversion command, the clock is enabled and the successive-approximation register is reset to all zeros. Once the conversion cycle begins, it cannot be stopped or restarted and data is not available from the output buffers.

The SAR, timed by the clock, sequences through the conversion cycle and returns an end-of-convert flag to the control section of the ADC. The clock is then disabled by the control section, the output status goes low, and the control section is enabled to allow the data to be read by external command.

The internal HADC574Z 12-bit CDAC is sequenced by the SAR starting from the MSB to the LSB at the beginning of the conversion cycle to provide an output voltage from the CDAC that is equal to the input signal voltage (which is divided by the input voltage divider network). The comparator determines whether the addition of each successively-weighted bit voltage causes the CDAC output voltage summation to greater or less than the input voltage; if the sum is less, the bit is left on; if more, the bit is turned off. After testing all the bits, the SAR contains a 12-bit binary code which accurately represents the input signal to within ±1/2 LSB.

The internal reference provides the voltage reference to the CDAC with excellent stability over temperature and time. The reference is trimmed to 10.00 volts ±1% and can supply up to 2 mA to an external load in addition to that required to drive the reference input resistor (1 mA) and offset resistor (1 mA) when operating with ±15 V supplies. If the HADC574Z is used with ±12 V supplies, or if external current must be supplied over the full temperature range, and external buffer amplifier is recommended. Any external load on the HADC574Z reference must remain constant during conversion.

The sample-and-hold feature is a bonus of the CDAC architecture. Therefore the majority of the S/H specifications are included within the A/D specifications.

Although the sample-and-hold circuit is not implemented in the classical sense, the sampling nature of the capacitive DAC makes the HADC574Z appear to have a built in sample-and-hold. This sample-and-hold action substantially increases the signal bandwidth of the HADC574Z over that of similar competing devices.

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Note that even though the user may use an external sample-and-hold for very high frequency inputs, the internal sample-and-hold still provides a very useful isolation function. Once the internal sample is taken by the CDAC capacitance, the input of the HADC574Z is disconnected from the user's sample-and-hold. This prevents transients occurring during conversion from being inflicted upon the attached sample-and-hold buffer. All other 574 circuits will cause a transient load current on the sample-and-hold which will upset the buffer output and may add error to the conversion itself.

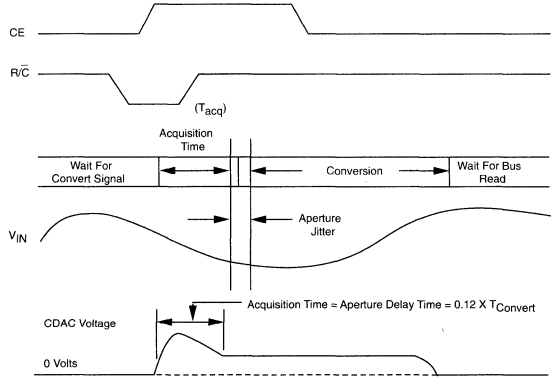
Furthermore, the isolation of the input after the acquisition time in the HADC574Z allows the user an opportunity to release the hold on an external sample-and-hold and start it tracking the next sample. This will increase system throughput with the user's existing components.

SAMPLE AND HOLD FUNCTION

When using an external S/H, the HADC574Z acts as any other 574 device because the internal S/H is transparent. The sample/hold function in the HADC574Z is inherent to the capacitor DAC structure, and its timing characteristics are determined by the internally generated clock. However, for limited frequency ranges, the internal S/H may eliminate the need for an external S/H. This function will be explained in the next two sections.

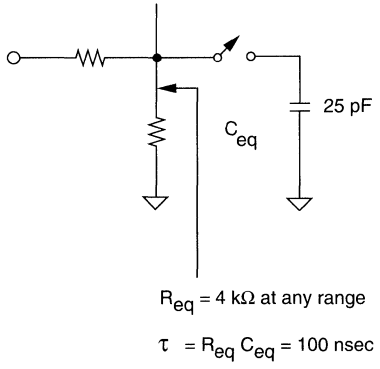
The operation of the S/H function is internal to the HADC574Z and is controlled through the normal R/$\overline{C}$ control line. (Refer to figure 8.) When the R/$\overline{C}$ line makes a negative transition, the HADC574Z starts the timing of the sampling and conversion. The first two clock cycles are allocated to signal acquisition of the input by the CDAC. (This time is defined as T_{acq}.) Following these two cycles, the input sample is taken and held. The A/D conversion follows this cycle with the duration controlled by the internal clock cycle.

Figure 8 - Sample and Hold Function



During T_{acq}, the equivalent circuit of the HADC574Z input is as shown in figure 9 (the time constant of the input is independent of which input level is used). This CDAC capacitance must be charged up to the input voltage during T_{acq}. Since the CDAC time constant is 100 nsecs, there is more than enough time for settling the input to 12-bits of accuracy during T_{acq}. The excess time left during T_{acq} allows the user's buffer amp to settle after being switched to the CDAC load.

Figure 9 - Equivalent HADC574Z Input Circuit



Note that because the sample is taken relative to the R/$\overline{C}$ transition, T_{acq} is also the traditional aperture delay of this internal sample-and-hold.

Since T_{acq} is measured in clock cycles, its duration will vary with the internal clock frequency. This results in T_{acq} =2.4 µsec between units and over temperature.

Offset, gain and linearity errors of the S/H circuit as well as the effects of its droop rate are included in the overall specifications for the HADC574Z.

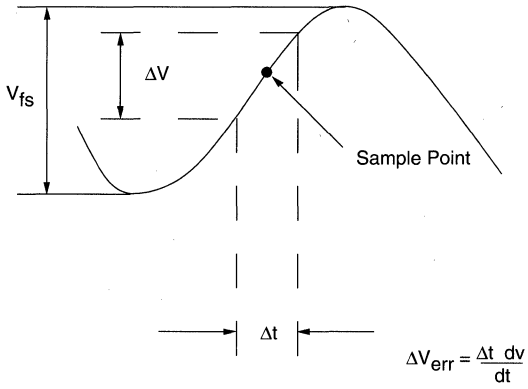
APERTURE UNCERTAINTY

Often the limiting factor in the application of the sample-and-hold is the uncertainty in the time that the actual sample is taken, i.e., the aperture jitter or T_{AJ}. The HADC574Z has a nominal aperture jitter of 8 nsec between samples. With this jitter, it is possible to accurately sample a wide range of input signals.

The aperture jitter causes an amplitude uncertainty for any input where the voltage is changing. The approximate voltage error due to aperture jitter depends on the slew rate of the signal at the sample point. (See figure 10.) The magnitude of this change for a sine wave can be calculated:

$V_{err} \leq V_{fs}/2^{N+1}$ (where V_{err} is the allowable error voltage and V_{fs} is the full scale voltage)

Figure 10 - Aperture Uncertainty



From figure 10:

$SR=\Delta V/\Delta t=2\ \pi fVp$

Let $\Delta V = V_{err} = V_{fs}\ (2 - {}^{(N+1)})$, $Vp = Vin/2$ and $\Delta t = t_{AJ}$ (The time during which unwanted voltage change occurs)

The above conditions then yield:

$$V_{fs}/2^{(N+1)} \geq \pi f V_{in}\ t_{AJ} \text{ or } f_{MAX} \leq V_{fs}/(\pi Vin\ t_{AJ})2^{(N+1)}$$

For the HADC574Z, t_{AJ}=8 nsec, therefore $f_{MAX} \leq$5 kHz.

For higher frequency signal inputs, an external sample-and-hold is recommended.

TYPICAL INTERFACE CIRCUIT

The HADC574Z is a complete A/D converter that is fully operational when powered up and issued a Start Convert Signal. Only a few external components are necessary as shown in figures 11 and 12. The two typical interface circuits are for operating the HADC574Z in either an unipolar or bipolar input mode. Information on these connections and on conditions concerning board layout to achieve the best operation are discussed below.

For each application of this device, strict attention must be given to power supply decoupling, board layout (to reduce pickup between analog and digital sections), and grounding. Digital timing, calibration and the analog signal source must be considered for correct operation.

To achieve specified accuracy, a double-sided printed circuit board with a copper ground plane on the component side is recommended. Keep analog signal traces away from digital lines. It is best to lay the PC board out such that there is an analog section and a digital section with a single point ground connection between the two through an RF bead located as closely to the device as possible. If possible, run analog signals between ground traces and cross digital lines at right angles only.

POWER SUPPLIES

The supply voltages for the HADC574Z must be kept as quiet as possible from noise pickup and also regulated from transients or drops. Because the part has 12-bit accuracy, voltage spikes on the supply lines can cause several LSB deviations on the output. Switching power supply noise can be a problem. Careful filtering and shielding should be employed to prevent the noise from being picked up by the converter.

Capacitor bypass pairs are needed from each supply pin to its respective ground to filter noise and counter the problems caused by the variations in supply current. A 10 µF tantalum and a 0.1 µF ceramic type in parallel between V_{LOGIC} (pin 1) and digital common (pin 15), and V_{CC} (pin 7) and analog common (pin 9) are sufficient. V_{EE} is generated internally so pin 11 may be grounded or connected to a negative supply if the HADC574Z is being used to upgrade an already existing design.

GROUNDING CONSIDERATIONS

Any ground path from the analog and digital ground should be as low resistance as possible to accommodate the ground currents present with this device.

The analog ground current is approximately 6 mADC while the digital ground is 3 mADC. The analog and digital common pins should be tied together as closely to the package as possible to guarantee best performance. The code dependent currents flow through the V_{LOGIC} and V_{CC} terminals and not through the analog and digital common pins.

The HADC574Z may be operated by a µP or in the stand-alone mode. The part has four standard input ranges: 0 V to +10 V, 0 V to +20 V, ±5 V and ±10 V. The maximum errors that are listed in the specifications for gain and offset may be adjusted externally to zero as explained in the next two sections.

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CALIBRATION AND CONNECTION PROCEDURES

UNIPOLAR

The calibration procedure consists of adjusting the converter's most negative output to its ideal value for offset adjustment, and then adjusting the most positive output to its ideal value for gain adjustment.

Starting with offset adjustment and referring to figure 11, the midpoint of the first LSB increment should be positioned at the origin to get an output code of all 0s. To do this, an input of +1/2 LSB or +1.22 mV for the 10 V range and +2.44 mV for the 20 V range should be applied to the HADC574Z. Adjust the offset potentiometer R1 for code transition flickers between 0000 0000 0000 and 0000 0000 0001.

The gain adjustment should be done at positive full scale. The ideal input corresponding to the last code change is applied. This is 1 and 1/2 LSB below the nominal full scale which is +9.9963 V for the 10 V range and +19.9927 V for the 20 V range. Adjust the gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111. If calibration is not necessary for the intended application, replace R2 with a 50 Ω, 1% metal film resistor and remove the network from pin 12. Connect pin 12 to pin 9. Connect the analog input to pin 13 for the 0 V to 10 V range or to pin 14 for the 0 V to 20 V range.

BIPOLAR

The gain and offset errors listed in the specification may be adjusted to zero using the potentiometers R1 and R2. (See figure 12.) If adjustment is not needed, either or both pots may be replaced by a 50 Ω, 1% metal film resistor.

To calibrate, connect the analog input signal to pin 13 for a ±5 V range or to pin 14 for a ±10 V range. First apply a DC input voltage 1/2 LSB above negative full scale which is -4.9988 V for the ±5 V range or -9.9976 V for the ±10 V range. Adjust the offset potentiometer R1 for flicker between output codes 0000 0000 0000 and 0000 0000 0001. Next, apply a DC input voltage 1 and 1/2 LSB below positive full scale which is +4.9963 V for the ±5 V range or +9.9927 V for the ±10 V range. Adjust the gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111.

ALTERNATIVE

In some applications, a full scale of 10.24 V (for an LSB of 2.5 mV) or 20.48 V (for an LSB of 5.0 mV) is more convenient. In the Unipolar mode of operation, replace R2 with a 200 Ω potentiometer and add 150 Ω in series with pin 13 for 10.24 V input range or 500 Ω in series with pin 14 for 20.48 V input range. In bipolar mode of operation, replace R1 with a 500 Ω potentiometer (in addition to the previous changes). The calibration will remain similar to the standard calibration procedure.

Figure 11 - Unipolar Input Connections

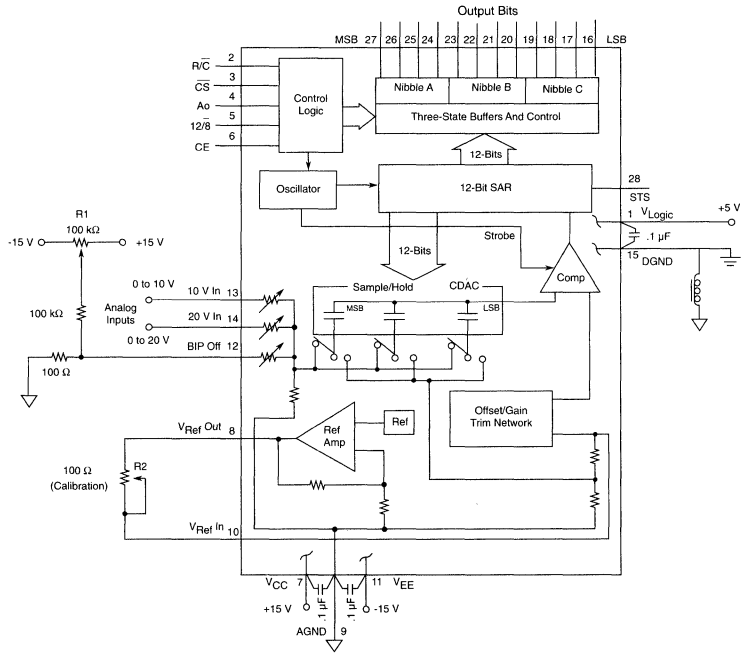
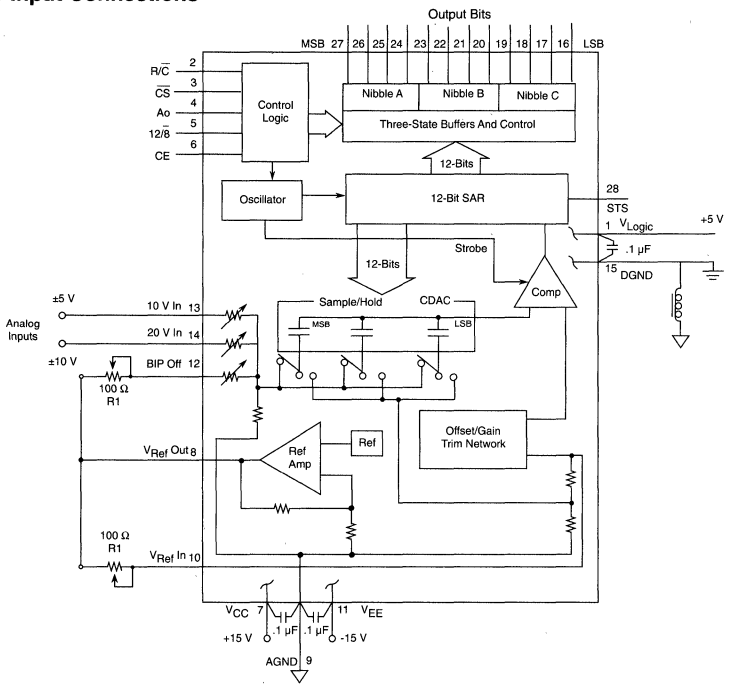


Figure 12 - Bipolar Input Connections



CONTROLLING THE HADC574Z

The HADC574Z can be operated by most microprocessor systems due to the control input pins and on-chip logic. It may also be operated in the "stand-alone" mode and enabled by the R/$\overline{C}$ input pin. Full µP control consists of selecting an 8 or 12-bit conversion cycle, initiating the conversion, and reading the output data when ready. The output read has the options of choosing either 12-bits at once or 8 bits followed by 4-bits in a left-justified format. All five control inputs are TTL/CMOS compatible and include 12/$\overline{8}$, $\overline{CS}$, Ao, R/$\overline{C}$ and CE. The use of these inputs in controlling the converter's operations is shown in table I, and the internal control logic is shown in a simplified schematic in figure 14.

STAND-ALONE OPERATION

The simplest interface is a control line connected to R/$\overline{C}$. The output controls must be tied to known states as follows: CE and 12/$\overline{8}$ are wired high, Ao and $\overline{CS}$ are wired low. The output data arrives in words of 12-bits each. The limits on R/$\overline{C}$ duty cycle are shown in figures 3 and 4. It may have a duty cycle within and including the extremes shown in the specifications. In general, data may be read when R/$\overline{C}$ is high unless STS is also high, indicating a conversion is in progress.

Figure 13 - Interfacing the HADC574Z to an 8-bit Data Bus

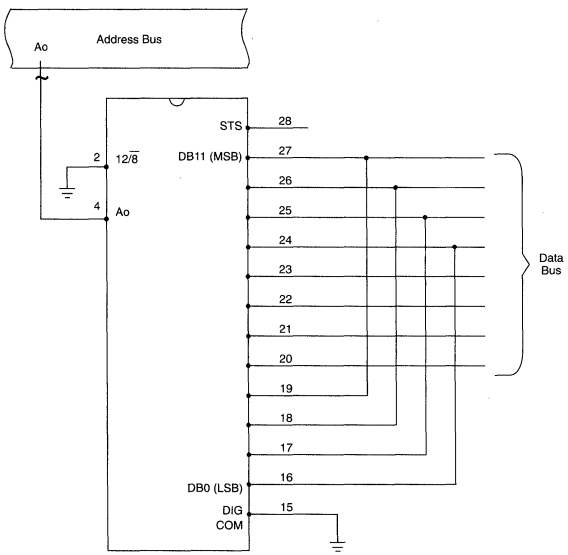


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Table I - Truth Table for the HADC574Z Control Inputs

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	Ao	Operation
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12 bit conversion
↑	0	0	X	1	Initiate 8 bit conversion
1	↓	0	X	0	Initiate 12 bit conversion
1	↓	0	X	1	Initiate 8 bit conversion
1	0	↓	X	0	Initiate 12 bit conversion
1	0	↓	X	1	Initiate 8 bit conversion
1	0	1	1	X	Enable 12 bit Output
1	0	1	0	0	Enable 8 MSB's Only
1	0	1	0	1	Enable 4 LSB's Plus 4 Trailing Zeroes

CONVERSION LENGTH

A conversion start transition latches the state of Ao as shown in figure 13 and table I. The latched state determines if the conversion stops with 8-bit (Ao high) or continues for 12-bits (Ao low). If all 12-bits are read following an 8-bit conversion, the three LSB's will be a logic 0 and DB3 will be a logic 1. Ao is latched because it is also involved in enabling the output buffers as will be explained later. No other control inputs are latched.

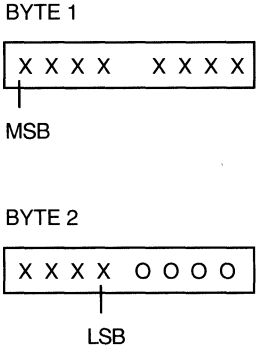
CONVERSION START

A conversion may be initiated by a logic transition on any of the three inputs: CE, $\overline{CS}$, R/$\overline{C}$, as shown in table I. The last of the three to reach the correct state starts the conversions, so one, two or all three may be dynamically controlled. The nominal delay from each is the same and all three may change state simultaneously. In order to assure that a particular input controls the start of conversion, the other two should be set up at least 50 ns earlier. Refer to the convert mode timing specifications. The Convert Start timing diagram is illustrated in figure 1.

The output signal STS is the status flag and goes high only when a conversion is in progress. While STS is high, the output buffers remain in a high impedance state so that data can not be read. Also, when STS is high, an additional Start Convert will not reset the converter or reinitiate a conversion. Note, if Ao changes state after a conversion begins, an additional Start Convert command will latch the new start of Ao and possibly cause a wrong cycle length for that conversion (8 versus 12-bits).

READING THE OUTPUT DATA

The output data buffers remain in a high impedance state until the following four conditions are met: R/$\overline{C}$ is high, STS is low, CE is high, and $\overline{CS}$ is low. The data lines become active in response to the four conditions and output data according to the conditions of 12/$\overline{8}$ and Ao. The timing diagram for this process is shown in figure 2. When 12/$\overline{8}$ is high, all 12 data outputs become active simultaneously and the Ao input is ignored. This is for easy interface to a 12 or 16-bit data bus. The 12/$\overline{8}$ input is usually tied high or low, although it is TTL/CMOS compatible. When 12/$\overline{8}$ is low, the output is separated into two 8-bit bytes as shown below:



This configuration makes it easy to connect to an 8-bit data bus as shown in figure 13. The Ao control can be connected to the least significant bit of the address bus in order to store the output data into two consecutive memory locations. When Ao is pulled low, the 8 MSBs are enabled only. When Ao is high, the 4 MSBs are disabled, bits 4 through 7 are forced to a zero and the four LSBs are enabled. The two byte format is left justified data as shown above and can be considered to have a decimal point or binary to the left of byte 1.

Ao may be toggled without damage to the converter at any time. Break-before-make action is guaranteed between the two data bytes. This assures that the outputs which are strapped together in figure 13 will never be enabled at the same time.

In figure 2, it can be seen that a read operation usually begins after the conversion is completed and STS is low. If earlier access is needed, the read can begin no later than the addition of time t_{DD} and t_{HS} before STS goes low.

Figure 14 - Control Logic

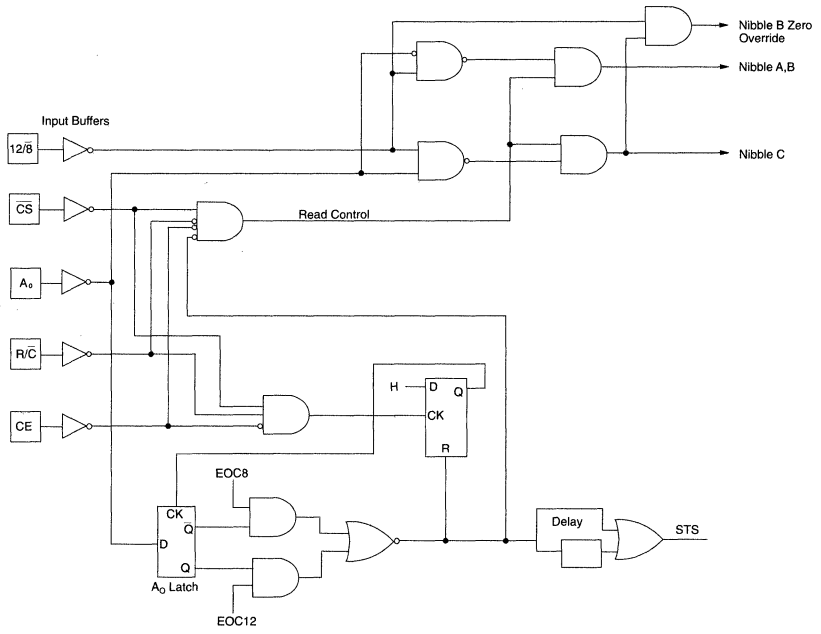
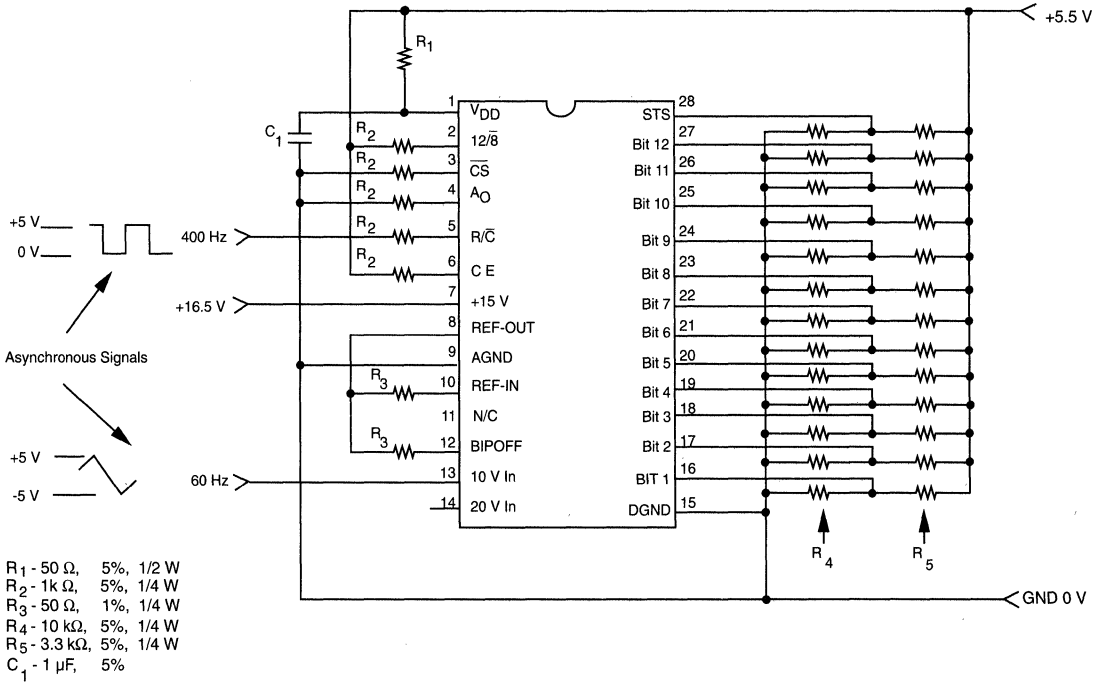


Figure 15 - Burn-In Schematic



R_1 - 50 Ω, 5%, 1/2 W
R_2 - 1k Ω, 5%, 1/4 W
R_3 - 50 Ω, 1%, 1/4 W
R_4 - 10 kΩ, 5%, 1/4 W
R_5 - 3.3 kΩ, 5%, 1/4 W
C_1 - 1 µF, 5%

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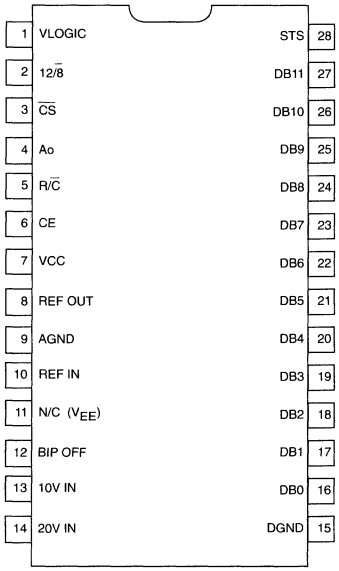
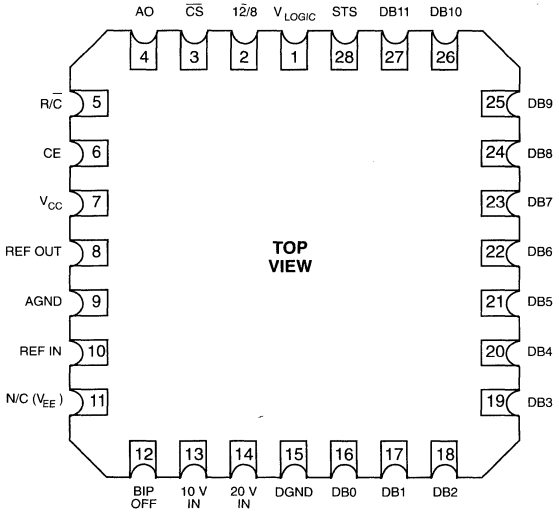
PIN ASSIGNMENTS

TOP VIEW



28 LEAD DIP



28 Lead LCC

PIN FUNCTIONS

NAME	FUNCTION
V_{LOGIC}	Logic Supply Voltage, Nominally +5 V
12/$\overline{8}$	Data Mode Selection
$\overline{CS}$	Chip Selection
Ao	Byte Address/Short Cycle
R/$\overline{C}$	Read/Convert
CE	Chip Enable
V_{CC}	Analog Positive Supply Voltage, Nominally +15 V
REF OUT	Reference Output, Nominally +10 V
AGND*	Analog Ground
REF IN	Reference Input
N/C (V_{EE})	This pin is not connected to the device.
BIP OFF	Bipolar Offset
10 V IN	10 Volt Analog Input
20 V IN	20 Volt Analog Input
DGND	Digital Ground
DB0 - DB11	Digital Data Output DB11 - MSB DB0 - LSB
STS	Status

* The lids on the sidebrazed and LCC packages are internally connected to AGND.

LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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SIGNAL PROCESSING TECHNOLOGIES

HADC674Z

FAST, COMPLETE 12-BIT µP COMPATIBLE A/D CONVERTER WITH SAMPLE/HOLD

3

FEATURES

- Improved Pin-To-Pin Compatible Monolithic Version of the HI674A
- Complete 12-Bit A/D Converter with Sample/Hold, Reference and Clock
- Low Power Dissipation (150 mW Max)
- 12-Bit Linearity (Over Temp)
- 15 µs Max Conversion Time
- No Negative Supply Required
- Full Bipolar and Unipolar Input Range

APPLICATIONS

- Military/Industrial Data Acquisition Systems
- 8 or 12-Bit µP Input Functions
- Process Control Systems
- Test and Scientific Instruments
- Personal Computer Interface

GENERAL DESCRIPTION

The HADC674Z is a complete, 12-bit successive approximation A/D converter. The device is integrated on a *single die* to make it the first monolithic CMOS version of the industry standard device, HI674A. Included on chip are an internal reference, clock, and a sample-and-hold. The S/H is an additional feature not available on similar devices.

The HADC674Z features 15 µs (max) conversion time of 10 or 20 volt input signals. Also, a three-state output buffer is added for direct interface to an 8, 12, or 16-bit µP bus.

The HADC674Z is manufactured on a Bipolar Enhanced CMOS process (BEMOS) which combines CMOS logic and fast bipolar npn transistors to yield high performance digital and analog functions on one chip.

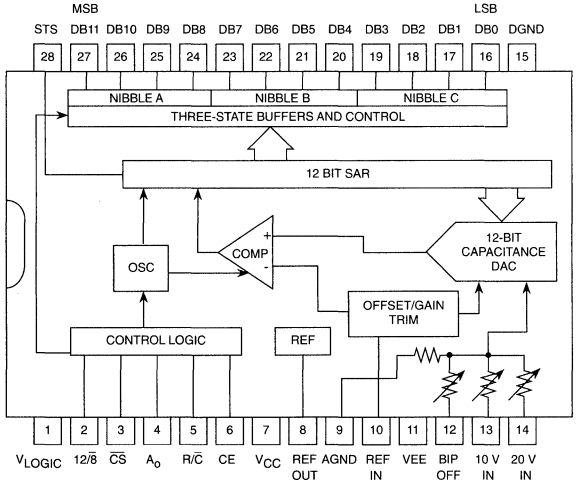
The BEMOS process and monolithic construction reduces power consumption and ground noise and keeps parasitics to a minimum. In addition, the thin film option on this process allows active adjustment of DAC and comparator offsets, linearity errors, and gain errors.

The HADC674Z has standard bipolar and unipolar input ranges of 10 V and 20 V that are controlled by a bipolar offset pin and laser trimmed for specified linearity, gain and offset accuracy.

Power requirements are +5 V and +12 V to +15 V with a maximum dissipation of 150 mW at the specified voltages. Power consumption is about five times lower than that of currently available devices, and a negative power supply is not needed.

A standard military drawing is published under DESC number 5962-91690.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING (Beyond which damage may occur) [1] 25 °C

Supply Voltages

Positive Supply Voltage (V_{CC} to DGND) ..... 0 to +16.5 V
Logic Supply Voltage (V_{LOGIC} to DGND) ..... 0 to +7 V
Analog to Digital Ground (AGND to DGND) . -0.5 to +1 V

Input Voltages

Control Input Voltages (to DGND)
(CE, CS, Ao, 12/8, R/C) ..... -0.5 to V_{LOGIC} +0.5 V
Analog Input Voltage (to AGND)
(REF IN, BIP OFF, 10 Vin) ..... ±16.5 V
20 V Vin Input Voltage (to AGND) ..... ±24 V

Output

Reference Output Voltage ..... Indefinite short to GND
Momentary short to V_{CC}

Temperature

Operating Temperature, ambient ..... -55 to +125 °C
junction ..... +175 °C
Lead Temperature, (soldering 10 seconds)..... +300 °C
Storage Temperature ..... -65 to +150 °C
Power Dissipation..... 1000 mW
Thermal Resistance (θ_{jA}) ..... 48 °C/W

Note: Operation at any Absolute Maximum Rating is not implied. See Operating Conditions for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

T_A=T_{MIN} to T_{MAX}, V_{CC}=+15 V or +12 V, V_{LOGIC}=+5 V, unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEST LEVEL	HADC674ZC MIN	HADC674ZC TYP	HADC674ZC MAX	HADC674ZB MIN	HADC674ZB TYP	HADC674ZB MAX	HADC674ZA MIN	HADC674ZA TYP	HADC674ZA MAX	UNITS
DC ELECTRICAL CHARACTERISTICS												
Resolution		VI			12			12			12	Bits
Linearity Error[1]	T_A=0 to 70 °C	VI			±1			±1/2			±1/2	LSB
	T_A = -25 to +85 °C	I			±1			±1/2			±1/2	LSB
	T_A = -55 to +125 °C	I			±1			±1			±1	LSB
Differential Linearity	No Missing Codes	VI	11			12			12			Bits
Unipolar Offset; 10 V, 20 V	+25 °C Adjustable to Zero	VI		±0.1	±2		±0.1	±2		±0.1	±2	LSB
Bipolar Offset1; ±5 V, ±10 V	+25 °C Adjustable to Zero	VI			±10			±4			±4	LSB
Full Scale Calibration Error[2] All Input Ranges	+25 °C Adjustable to Zero	VI			0.3			0.3			0.3	% of FS
	No Adjustment at +25°											
	T_A = 0 to 70 °C	V		0.5			0.4			0.35		%of FS
	T_A = -25 to +85 °C	V		0.7			0.5			0.4		%of FS
	T_A = -55 to +125 °C	V		0.8			0.6			0.4		%of FS
	With Adjustment at +25 °C											
	T_A = 0 to 70 °C	V		0.22			0.12			0.05		%of FS
	T_A = -25 to +85 °C	V		0.4			0.2			0.1		%of FS
	T_A = -55 to +125 °C	V		0.5			0.25			0.12		%of FS
Temperature Coefficients[3]	Using Internal Reference											
Unipolar Offset	T_A = 0 to 70 °C	IV		±0.2	±2		±0.1	±1		±0.1	±1	LSB
					(10)			(5)			(5)	(ppm/°C)
	T_A = -25 to +85 °C	IV			±2			±1			±1	LSB
					(5)			(2.5)			(2.5)	(ppm/°C)
	T_A = -55 to +125 °C	IV			±2			±1			±1	LSB
					(5)			(2.5)			(2.5)	(ppm/°C)
Bipolar Offset	T_A = 0 to 70 °C	IV		±0.2	±2		±0.1	±1		±0.1	±1	LSB
					(10)			(5)			(5)	(ppm/°C)
	T_A = -25 to +85 °C	IV			±2			±1			±1	LSB
					(5)			(2.5)			(2.5)	(ppm/°C)

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ELECTRICAL SPECIFICATIONS

$T_A = T_{MIN}$ to T_{MAX}, V_{CC} = +15 V or +12 V, V_{LOGIC} = +5 V, unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEST LEVEL	HADC674ZC MIN	HADC674ZC TYP	HADC674ZC MAX	HADC674ZB MIN	HADC674ZB TYP	HADC674ZB MAX	HADC674ZA MIN	HADC674ZA TYP	HADC674ZA MAX	UNITS
DIGITAL CHARACTERISTICS												
Logic Inputs (CE, $\overline{CS}$, R/$\overline{C}$, Ao, 12/$\overline{8}$)												
Logic "0"		VI	-0.5		+0.8	-0.5		+0.8	-0.5		+0.8	Volts
Logic "1"		VI	2.0		5.5	2.0		5.5	2.0		5.5	Volts
Current	0 to 5.5 V Input	VI		±.01	+1		±.01	+1		±.01	+1	µA
Capacitance		V		5			5			5		pF
Logic Outputs (DB11-DB0, STS)												
Logic "0"	(I_{Sink} = 1.6 mA)	VI			+0.4			+0.4			+0.4	Volts
Logic "1"	(I_{SOURCE} = 500 µA)	VI	+2.4			+2.4			+2.4			Volts
Leakage	(High Z State, DB11-DB0 Only)	VI	-5	±0.1	+5	-5	±0.1	+5	-5	±0.1	+5	µA
Capacitance		V		5			5			5		pF

Note 1: For military temperature range, the device linearity is guaranteed to be 1/2 LSB at 25 °C.
Note 2: Fixed 50 Ω resistor from REF OUT to REF IN and REF OUT to BIP OFF.
Note 3: Full Tempco testing is performed on all Grade A and MIL-STD-883 devices.
Note 4: Available for external loads; external load should not change during conversion. When supplying an external load and operating on a +12.0 V supply, a buffer amplifier must be provided for the reference output.

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ELECTRICAL SPECIFICATIONS

$T_A = T_{MIN}$ to T_{MAX}, V_{CC} = +15 V or +12 V, V_{LOGIC} = +5 V, unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEST LEVEL	HADC674ZC MIN	HADC674ZC TYP	HADC674ZC MAX	HADC674ZB MIN	HADC674ZB TYP	HADC674ZB MAX	HADC674ZA MIN	HADC674ZA TYP	HADC674ZA MAX	UNITS
DC ELECTRICAL CHARACTERISTICS												
Bipolar Offset (Cont.)	T_A = -55 to +125 °C	IV			±4 (10)			±2 (5)			±1 (2.5)	LSB (ppm/°C)
Full Scale Calibration	T_A = 0 to 70 °C	IV			±9 (45)			±5 (25)			±2 (10)	LSB (ppm/°C)
	T_A = -25 to +85 °C	IV			±12 (50)			±7 (25)			±3 (12)	LSB (ppm/°C)
	T_A = -55 to +125 °C	IV			±20 (50)			±10 (25)			±5 (12.5)	LSB (ppm/°C)
Power Supply Rejection	Max change in full scale calibration											
+13.5 V<V_{CC}<+16.5 V or +11.4 V<V_{CC}<+12.6 V		VI		±0.5	±2		±0.5	±1		±0.5	±1	LSB
+4.5 V<V_{LOGIC}<+5.5 V		VI		±0.1	±0.5		±0.1	±0.5		±0.1	±0.5	LSB
Analog Input Ranges												
Bipolar		VI	-5 -10		+5 +10	-5 -10		+5 +10	-5 -10		+5 +10	Volts Volts
Unipolar		VI	0 0		+10 +20	0 0		+10 +20	0 0		+10 +20	Volts Volts
Input Impedance 10 Volt Span 20 Volt Span		VI	 3.75 15	 5 20	 6.25 25	 3.75 15	 5 20	 6.25 25	 3.75 15	 5 20	 6.25 25	 kΩ kΩ
Power Supplies Operating Voltage Range												
V_{LOGIC}		VI	+4.5		+5.5	+4.5		+5.5	+4.5		+5.5	Volts
V_{CC}		VI	+11.4		+16.5	+11.4		+16.5	+11.4		+16.5	Volts
V_{EE}	Not required for circuit operation											
Operating Current												
I_{LOGIC}		VI		0.5	1		0.5	1		0.5	1	mA
I_{CC}		VI		7	9		7	9		7	9	mA
I_{EE}	Not required for circuit operation											
Power Dissipation +15 V, +5 V		VI		110	150		110	150		110	150	mW
Internal Reference Voltage Output Current[4]		VI VI	9.97	10	10.03 2	9.97	10	10.03 2	9.97	10	10.03 2	Volts mA

ELECTRICAL SPECIFICATIONS

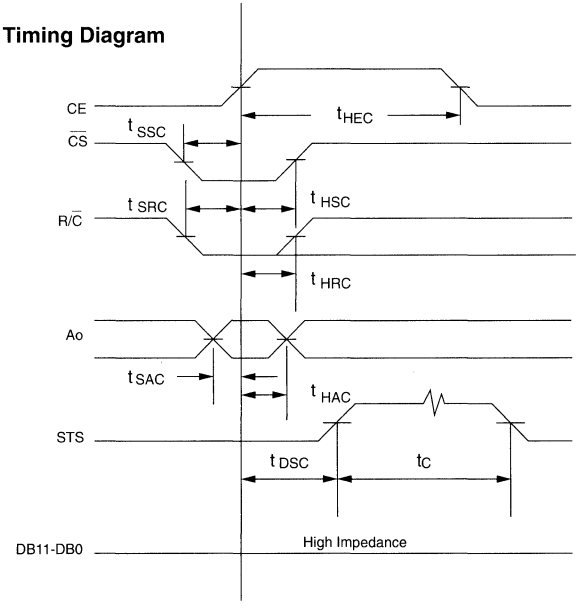
CONVERT MODE TIMING CHARACTERISTICS

T_A = +25 °C, V_{CC} = +15.0 V or +12 V, V_{LOGIC} = +5 V, unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEST LEVEL	HADC674ZC MIN	HADC674ZC TYP	HADC674ZC MAX	HADC674ZB MIN	HADC674ZB TYP	HADC674ZB MAX	HADC674ZA MIN	HADC674ZA TYP	HADC674ZA MAX	UNITS
AC ELECTRICAL CHARACTERISTICS[5]												
t_{DSC} STS Delay from CE		I			200			200			200	ns
t_{HEC} CE Pulse Width		I	50			50			50			ns
t_{SSC} $\overline{CS}$ to CE Setup		I	50			50			50			ns
t_{HSC} $\overline{CS}$ Low during CE High		I	50			50			50			ns
t_{SRC} R/$\overline{C}$ to CE Setup		I	50			50			50			ns
t_{HRC} R/$\overline{C}$ Low During CE High		I	50			50			50			ns
t_{SAC} Ao to CE Setup		I	0			0			0			ns
t_{HAC} Ao Valid During CE High		I	50			50			50			ns
t_C Conversion Time												
12-Bit Cycle	T_{MIN} to T_{MAX}	I	9	13	15	9	13	15	9	13	15	µs
8-Bit Cycle	T_{MIN} to T_{MAX}	I	6	8	10	6	8	10	6	8	10	µs

Note 5: Time is measured from 50% level of digital transitions. Parameters are tested with a 100 pF and 3 kΩ load for high impedance to drive and tested with 10 pF and 3 kΩ load for drive to high impedance.

Figure 1 - Convert Mode Timing Diagram



ELECTRICAL SPECIFICATIONS

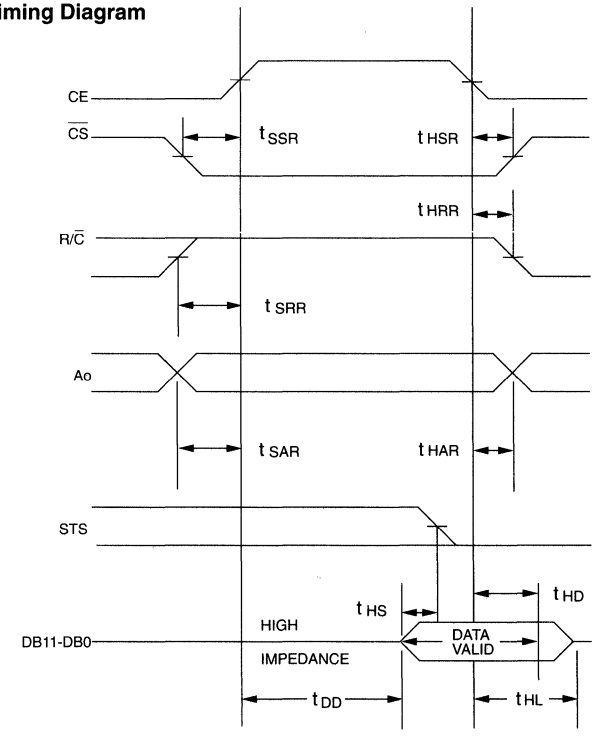
READ MODE TIMING CHARACTERISTICS

T_A = 25 °C, V_{CC} = +15.0 V or +12 V, V_{LOGIC} = +5 V, unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEST LEVEL	HADC674ZC MIN	HADC674ZC TYP	HADC674ZC MAX	HADC674ZB MIN	HADC674ZB TYP	HADC674ZB MAX	HADC674ZA MIN	HADC674ZA TYP	HADC674ZA MAX	UNITS
AC ELECTRICAL CHARACTERISTICS[6]												
t_{DD} Access Time from CE		I			150			150			150	ns
t_{HD} Data Valid After CE Low		I	25			25			25			ns
t_{HL} Output Float Delay		I			150			150			150	ns
t_{SSR} $\overline{CS}$ to CE Setup		I	50	0		50	0		50	0		ns
t_{SRR} R/$\overline{C}$ to CE Setup		I	0	0		0	0		0	0		ns
t_{SAR} Ao to CE Setup		I	50			50			50			ns
t_{HSR} $\overline{CS}$ Valid After CE Low		I	0	0		0	0		0	0		ns
t_{HRR} R/$\overline{C}$ High After CE Low		I	50			50			50			ns
t_{HS} STS Delay After Data Valid		I	100		600	100		600	100		600	ns
t_{HAR} Ao Valid after CE Low		I	50			50			50			ns

Note 6: Time is measured from 50% level of digital transitions. Parameters are tested with a 100 pF and 3 kΩ load for high impedance to drive and tested with 10 pF and 3 kΩ load for drive to high impedance.

Figure 2 - Read Mode Timing Diagram



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ELECTRICAL SPECIFICATIONS

STAND-ALONE MODE TIMING CHARACTERISTICS

T_A = 25 °C, V_{CC} = +15.0 V or +12 V, V_{LOGIC} = +5 V, unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEST LEVEL	HADC674ZC MIN	HADC674ZC TYP	HADC674ZC MAX	HADC674ZB MIN	HADC674ZB TYP	HADC674ZB MAX	HADC674ZA MIN	HADC674ZA TYP	HADC674ZA MAX	UNITS
AC ELECTRICAL CHARACTERISTICS[6]												
t_{HRL} Low R/$\overline{C}$ Pulse Width		I	50			50			50			ns
t_{DS} STS Delay from R/$\overline{C}$		I			200			200			200	ns
t_{HDR} Data Valid After R/$\overline{C}$ Low		I	25			25			25			ns
t_{HS} STS Delay After Data Valid		I	100		600	100		600	100		600	ns
t_{HRH} High R/$\overline{C}$ Pulse Width		I	150			150			150			ns
t_{DDR} Data Access Time		I			150			150			150	ns
SAMPLE-AND-HOLD												
Acquisition Time		IV	1.2	1.7	2.0	1.2	1.7	2.0	1.2	1.7	2.0	µs
Aperture Uncertainty Time		V		8			8			8		ns,RMS

Figure 3 - Low Pulse for R/$\overline{C}$ - Outputs Enabled After Conversion

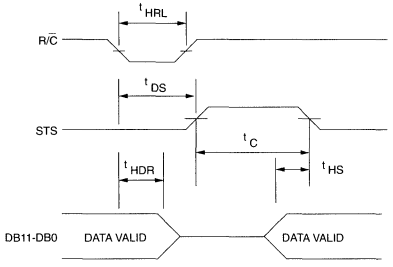
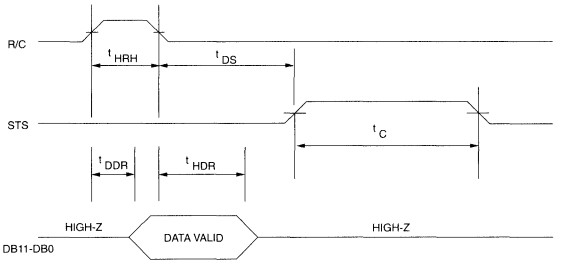


Figure 4 - High Pulse for R/$\overline{C}$ - Outputs Enabled While R/$\overline{C}$ is High, Otherwise High Impedance



TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests; therefore, $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

DEFINITION OF SPECIFICATIONS

INTEGRAL LINEARITY ERROR

Linearity error refers to the deviation of each individual code from a line drawn from zero through full scale with all offset errors nulled out. (See figures 5 and 6.) The point used as zero occurs 1/2 LSB (1.22 mV for a 10 volt span) before the first code transition (all zeros to only the LSB on). Full scale is defined as a level 1 and 1/2 LSB beyond the last code transition (to all ones). The deviation of a code from the true straight line is measured from the middle of each particular code.

The HADC674ZAC and BC grades are guaranteed for maximum nonlinearity of ±1/2 LSB. For these grades, this means that an analog value that falls exactly in the center of a given code width will result in the correct digital output code. Values nearer the upper or lower transition of the code width may produce the next upper or lower digital output code. The HADC674ZAM, BM, CC and CM grades are guaranteed to ±1 LSB maximum error. For these grades, an analog value that falls within a given code width will result in either the correct code for the region or either adjacent one. The linearity is not user-adjustable.

DIFFERENTIAL LINEARITY ERROR (NO MISSING CODES)

A specification that guarantees no missing codes requires that every code combination appear in a monotonically increasing sequence as the analog input level is increased. Thus every code must have a finite width. For the HADC674Z type AC, BC, AM and BM grades that guarantee no missing codes to 12-bit resolution, all 4096 codes must be present over the entire operating temperature ranges. The HADC674Z CC and CM grades guarantee no missing codes to 11-bit resolution over temperature; this means that all code combinations of the upper 11-bits must be present. In practice, very few of the 12-bit codes are missing.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is a measure of how much the actual quantization step width varies from the ideal step width of 1 LSB. Figure 6 shows a differential nonlinearity of 2 LSB - the actual step width is 3 LSB. The HADC674Z's specification gives the worst case differential nonlinearity in the A/D transfer function under specified dynamic operating conditions. Small, localized differential nonlinearities may be insignificant when digitizing full scale signals. However, if a low level input signal happens to fall on the part of the A/D transfer function with the differential nonlinearity error, the effect will be significant.

MISSING CODES

Missing codes represent a special kind of differential nonlinearity. The quantization step width for a missing code is 0 LSB which results in a differential nonlinearity of -1 LSB. Figure 6 points out two missed codes in the transfer function.

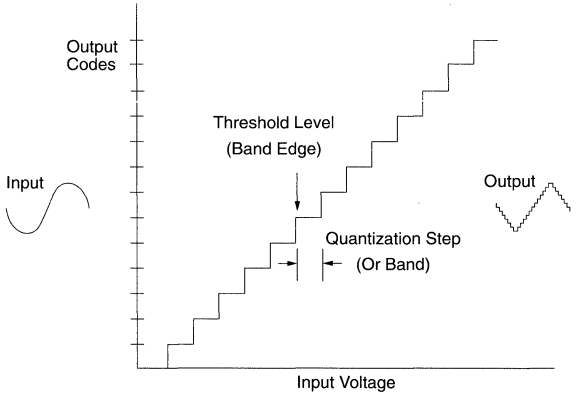
QUANTIZATION UNCERTAINTY

Analog-to-digital converters exhibit an inherent quantization uncertainty of ±1/2 LSB. This uncertainty is a fundamental characteristic of the quantization process and cannot be reduced for a converter of a given resolution.

QUANTIZATION ERROR

Quantization error is the fundamental, irreducible error associated with the perfect quantizing of a continuous (analog) signal into a finite number of digital bits (A/D transfer function). A 12-bit A/D converter can represent an input voltage with a best case uncertainty of 1 part in 2^{12} (1 part in 4096). In real A/Ds under dynamic operating conditions, the quantization bands (bit change step vs input amplitude) for certain codes can be significantly larger (or smaller) than the ideal. The ideal width of each quantization step (or band) is $Q=FSR/2^N$ where FSR=full scale range and N=12. Nonideal quantization bands represent differential non linearity errors. (See figures 5, 6 and 7.)

Figure 5 - Static Input Conditions



RESOLUTION - ACTUAL vs AVAILABLE

The available resolution of an N-bit converter is 2^N. This means it is theoretically possible to generate 2^N unique output codes.

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Figure 6 - Dynamic Conditions

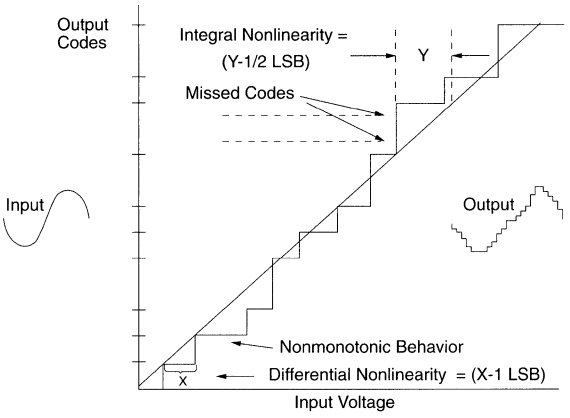
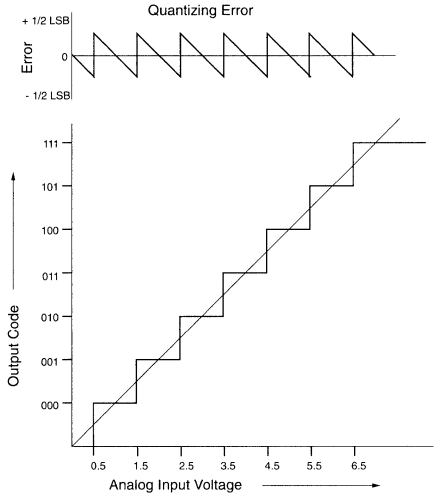


Figure 7 - Quantizing Error



THROUGHPUT

Maximum throughput is the greatest number of conversions per second at which an ADC will deliver its full rate performance. This is equivalent to the inverse of the sum of the multiplex time (if applicable), the S/H settling time and the conversion time.

GAIN

Gain is the slope of the transfer curve. Gain is generally user adjustable to compensate for long term drift.

ACQUISITION TIME/APERTURE DELAY TIME

In the HADC674Z, this is the time delay between the R/$\overline{C}$ falling edge and the actual start of the HOLD mode in a sample-and-hold function.

APERTURE JITTER

This is a specification indicating how much the aperture delay time varies between samples.

SUCCESSIVE APPROXIMATION ADC

The successive approximation converter uses an architecture with inherently high throughput rates that converts high frequency signals with great accuracy. A sample-and-hold type circuit can be used on the input to freeze these signals during conversion.

An N-bit successive approximation converter performs a sequence of tests comparing the input voltage to a successively narrower voltage range. The first range is half full scale, the next is quarter full scale, etc., until it reaches the Nth test which narrows it to a range of $1/2^N$ of full scale. The conversion time is fixed by the clock frequency and is thus independent of the input voltage.

UNIPOLAR OFFSET

The first transition should occur at a level 1/2 LSB above analog common. Unipolar offset is defined as the deviation of the actual transition from that point. This offset can be adjusted as discussed on the following pages. The unipolar offset temperature coefficient specifies the maximum change of the transition point over temperature, with and without external adjustment.

BIPOLAR OFFSET

In the bipolar mode, the major carry transition (0111 1111 1111 to 1000 0000 0000) should occur for an analog value 1/2 LSB below analog common. The bipolar offset error and temperature coefficient specify the initial deviation and maximum change in the error over temperature.

CONVERSION TIME

This is the time required to complete a conversion over the specified operating range. Conversion time can be expressed as time/bit for a converter with selectable resolution or as time/conversion when the number of bits is constant. The HADC674Z is specified as time/conversion for all 12 bits. Conversion time should not be confused with maximum allowable analog input frequency which is discussed later.

FULL SCALE CALIBRATION ERROR

The last transition (from 1111 1111 1110 to 1111 1111 1111 1111) should occur for an analog value 1 and 1/2 LSB below the nominal full scale (9.9963 volts for 10.000 volts full scale). The full scale calibration error is the deviation of the actual level at the last transition from the ideal level. This error, which typically is 0.05 to 0.1% of full scale, can be trimmed out as show in figures 11 and 12. The full scale calibration error over temperature is given with and without the initial error trimmed out. The temperature coefficients for each grade indicate the maximum change in the full scale gain from the initial value using the internal 10 volt reference.

TEMPERATURE COEFFICIENTS

The temperature coefficients for full scale calibration, unipolar offset, and bipolar offset specify the maximum change from the initial (25 °C) value to the value at Tmin or Tmax.

POWER SUPPLY REJECTION

The standard specifications for the HADC674Z assume +5.00 and +15.00 or +12.00 volt supplies. The only effect of power supply error on the performance of the device will be a small change in the full scale calibration. This will result in a linear change in all lower order codes. The specifications show the maximum change in calibration from the initial value with the supplies at the various limits.

CODE WIDTH

The fundamental unit for A/D converter specifications is the code width. This is defined as the range of analog input values for which a given digital output code will occur. The nominal value of a code width is equivalent to one least significant bit (LSB) of the full scale range or 2.44 mV out of 10 volts for a 12-bit ADC.

LEFT-JUSTIFIED DATA

The data format used in the HADC674Z is left-justified. This means that the data represents the analog input as fraction of full scale, ranging from 0 to 4095/4096. This implies a binary point to the left of the MSB.

MONOTONICITY

This characteristic describes an aspect of the code to code progression from minimum to maximum input. A device is said to be monotonic if the output code continuously increases as the input signal increases, and if the output code continuously decreases as the input signal decreases. Figure 6 demonstrates nonmonotonic behavior.

CIRCUIT OPERATION

The HADC674Z is a complete 12-bit analog-to-digital converter that consists of a single chip version of the industry standard 674. This single chip contains a precision 12-bit capacitor digital-to-analog converter (CDAC) with voltage reference, comparator, successive approximation register (SAR), sample-and-hold, clock, output buffers and control circuitry to make possible to use the HADC674Z with few external components.

When the control section of the HADC674Z initiates a conversion command, the clock is enabled and the successive-approximation register is reset to all zeros. Once the conversion cycle begins, it cannot be stopped or restarted and data is not available from the output buffers.

The SAR, timed by the clock, sequences through the conversion cycle and returns an end-of-convert flag to the control section of the ADC. The clock is then disabled by the control section, the output status goes low, and the control section is enabled to allow the data to be read by external command.

The internal HADC674Z 12-bit CDAC is sequenced by the SAR starting from the MSB to the LSB at the beginning of the conversion cycle to provide an output voltage from the CDAC that is equal to the input signal voltage (which is divided by the input voltage divider network). The comparator determines whether the addition of each successively-weighted bit voltage causes the CDAC output voltage summation to greater or less than the input voltage; if the sum is less, the bit is left on; if more, the bit is turned off. After testing all the bits, the SAR contains a 12-bit binary code which accurately represents the input signal to within ±1/2 LSB.

The internal reference provides the voltage reference to the CDAC with excellent stability over temperature and time. The reference is trimmed to 10.00 volts ±1% and can supply up to 2 mA to an external load in addition to that required to drive the reference input resistor (1 mA) and offset resistor (1 mA) when operating with ±15 V supplies. If the HADC674Z is used with ±12 V supplies, or if external current must be supplied over the full temperature range, and external buffer amplifier is recommended. Any external load on the HADC674Z reference must remain constant during conversion.

The sample-and-hold feature is a bonus of the CDAC architecture. Therefore the majority of the S/H specifications are included within the A/D specifications.

Although the sample-and-hold circuit is not implemented in the classical sense, the sampling nature of the capacitive DAC makes the HADC674Z appear to have a built in sample-and-hold. This sample-and-hold action substantially increases the signal bandwidth of the HADC674Z over that of similar competing devices.

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Note that even though the user may use an external sample-and-hold for very high frequency inputs, the internal sample-and-hold still provides a very useful isolation function. Once the internal sample is taken by the CDAC capacitance, the input of the HADC674Z is disconnected from the user's sample-and-hold. This prevents transients occurring during conversion from being inflicted upon the attached sample-and-hold buffer. All other 674 circuits will cause a transient load current on the sample-and-hold which will upset the buffer output and may add error to the conversion itself.

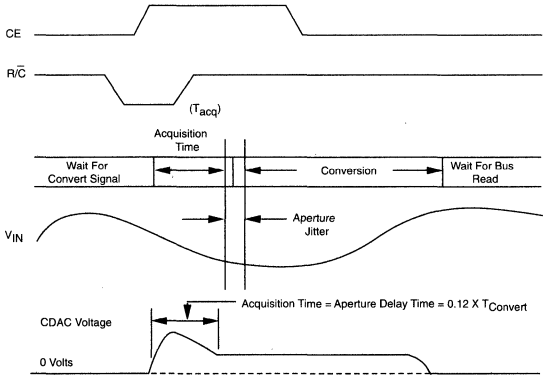
Furthermore, the isolation of the input after the acquisition time in the HADC674Z allows the user an opportunity to release the hold on an external sample-and-hold and start it tracking the next sample. This will increase system throughput with the user's existing components.

SAMPLE-AND-HOLD FUNCTION

When using an external S/H, the HADC674Z acts as any other 674 device because the internal S/H is transparent. The sample/hold function in the HADC674Z is inherent to the capacitor DAC structure, and its timing characteristics are determined by the internally generated clock. However, for limited frequency ranges, the internal S/H may eliminate the need for an external S/H. This function will be explained in the next two sections.

The operation of the S/H function is internal to the HADC674Z and is controlled through the normal R/$\overline{C}$ control line. (Refer to figure 8.) When the R/$\overline{C}$ line makes a negative transition, the HADC674Z starts the timing of the sampling and conversion. The first two clock cycles are allocated to signal acquisition of the input by the CDAC. (This time is defined as T_{acq}). Following these two cycles, the input sample is taken and held. The A/D conversion follows this cycle with the duration controlled by the internal clock cycle.

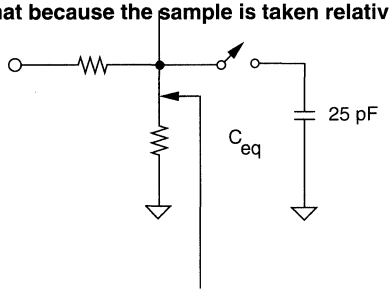
Figure 8 - Sample-and-hold Function



During T_{acq}, the equivalent circuit of the HADC674Z input is as shown in figure 9. (The time constant of the input is independent of which input level is used.) This CDAC capacitance must be charged up to the input voltage during T_{acq}. Since the CDAC time constant is 100 nsecs, there is more than enough time for settling the input to 12-bits of accuracy during T_{acq}. The excess time left during T_{acq} allows the user's buffer amp to settle after being switched to the CDAC load.

Figure 9 - Equivalent HADC674Z Input Circuit

Note that because the sample is taken relative to the



R_{eq} = 4 kΩ at any range

$\tau = R_{eq} C_{eq}$ = 100 nsec

R/$\overline{C}$ transition, T_{acq} is also the traditional "aperture delay" of this internal sample-and-hold.

Since T_{acq} is measured in clock cycles, its duration will vary with the internal clock frequency. This results in T_{acq} =1.7 µsec between units and over temperature.

Offset, gain and linearity errors of the S/H circuit, as well as the effects of its droop rate are included in the overall specifications for the HADC674Z.

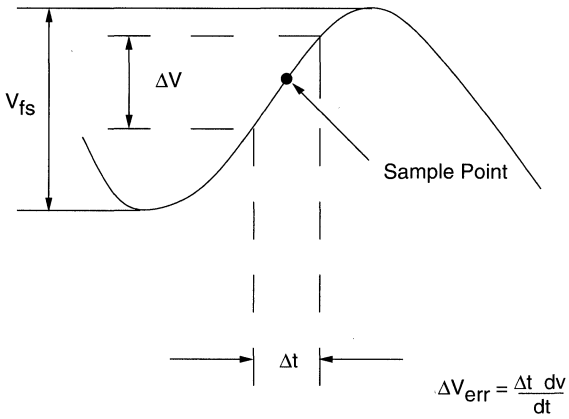
APERTURE UNCERTAINTY

Often the limiting factor in the application of the sample-and-hold is the uncertainty in the time that the actual sample is taken, i.e., the aperture jitter or T_{AJ}. The HADC674Z has a nominal aperture jitter of 8 nsec between samples. With this jitter, it is possible to accurately sample a wide range of input signals.

The aperture jitter causes an amplitude uncertainty for any input where the voltage is changing. The approximate voltage error due to aperture jitter depends on the slew rate of the signal at the sample point. (See figure 10.) The magnitude of this change for a sine wave can be calculated:

$V_{err} \leq V_{fs}/2^{N+1}$ (where V_{err} is the allowable error voltage and V_{fs} is the full scale voltage)

Figure 10 - Aperture Uncertainty



From figure 10:

$SR=\Delta V/\Delta t=2\ \pi fVp$

Let $\Delta V = V_{err} = V_{fs}(2 - (N+1))$, $Vp = Vin/2$ and $\Delta t = t_{AJ}$ (The time during which unwanted voltage change occurs)

The above conditions then yield:

$V_{fs}/2^{(N+1)} \geq \pi f V_{in}\ t_{AJ}$ or $f_{MAX} \leq V_{fs}/(\pi Vin\ t_{AJ})2^{(N+1)}$

For the HADC674Z, t_{AJ}=8 nsec, therefore $f_{max} \leq 5$ kHz.

For higher frequency signal inputs, an external sample-and-hold is recommended.

TYPICAL INTERFACE CIRCUIT

The HADC674Z is a complete A/D converter that is fully operational when powered up and issued a Start Convert Signal. Only a few external components are necessary as shown in figure 11 and 12. The two typical interface circuits are for operating the HADC674Z in either an unipolar or bipolar input mode. Information on these connections and on conditions concerning board layout to achieve the best operation are discussed below.

For each application of this device, strict attention must be given to power supply decoupling, board layout (to reduce pickup between analog and digital sections), and grounding. Digital timing, calibration and the analog signal source must be considered for correct operation.

To achieve specified accuracy, a double-sided printed circuit board with a copper ground plane on the component side is recommended. Keep analog signal traces away from digital lines. It is best to lay the PC board out such that there is an analog section and a digital section with a single point ground connection between the two through an RF bead located as closely to the device as possible. If possible, run analog signals between ground traces and cross digital lines at right angles only.

POWER SUPPLIES

The supply voltages for the HADC674Z must be kept as quiet as possible from noise pickup and also regulated from transients or drops. Because the part has 12-bit accuracy, voltage spikes on the supply lines can cause several LSB deviations on the output. Switching power supply noise can be a problem. Careful filtering and shielding should be employed to prevent the noise from being picked up by the converter.

Capacitor bypass pairs are needed from each supply pin to its respective ground to filter noise and counter the problems caused by the variations in supply current. A 10 µF tantalum and a 0.1 µF ceramic type in parallel between V_{LOGIC} (pin 1) and digital common (pin 15), and V_{CC} (pin 7) and analog common (pin 9) are sufficient. V_{EE} is generated internally so pin 11 may be grounded or connected to a negative supply if the HADC674Z is being used to upgrade an already existing design.

GROUNDING CONSIDERATIONS

Any ground path from the analog and digital ground should be as low resistance as possible to accommodate the ground currents present with this device.

The analog ground current is approximately 6 mADC while the digital ground is 3 mADC. The analog and digital common pins should be tied together as closely to the package as possible to guarantee best performance. The code dependent currents flow through the V_{LOGIC} and V_{CC} terminals and not through the analog and digital common pins.

The HADC674Z may be operated by a µP or in the stand-alone mode. The part has four standard input ranges: 0 V to +10 V, 0 V to +20 V, ±5 V and ±10 V. The maximum errors that are listed in the specifications for gain and offset may be adjusted externally to zero as explained in the next two sections.

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CALIBRATION AND CONNECTION PROCEDURES

UNIPOLAR

The calibration procedure consists of adjusting the converter's most negative output to its ideal value for offset adjustment, and then adjusting the most positive output to its ideal value for gain adjustment.

Starting with offset adjustment and referring to figure 11, the midpoint of the first LSB increment should be positioned at the origin to get an output code of all 0s. To do this, an input of +1/2 LSB or +1.22 mV for the 10 V range and +2.44 mV for the 20 V range should be applied to the HADC674Z. Adjust the offset potentiometer R1 for code transition flickers between 0000 0000 0000 and 0000 0000 0001.

The gain adjustment should be done at positive full scale. The ideal input corresponding to the last code change is applied. This is 1 and 1/2 LSB below the nominal full scale which is +9.9963 V for the 10 V range and +19.9927 V for the 20 V range. Adjust the gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111. If calibration is not necessary for the intended application, replace R2 with a 50 Ω, 1% metal film resistor and remove the network from pin 12. Connect pin 12 to pin 9. Connect the analog input to pin 13 for the 0 V to 10 V range or to pin 14 for the 0 V to 20 V range.

BIPOLAR

The gain and offset errors listed in the specification may be adjusted to zero using the potentiometers R1 and R2. (See figure 12.) If adjustment is not needed, either or both pots may be replaced by a 50 Ω, 1% metal film resistor.

To calibrate, connect the analog input signal to pin 13 for a ±5 V range or to pin 14 for a ±10 V range. First apply a DC input voltage 1/2 LSB above negative full scale which is -4.9988 V for the ±5 V range or -9.9976 V for the ±10 V range. Adjust the offset potentiometer R1 for flicker between output codes 0000 0000 0000 and 0000 0000 0001. Next, apply a DC input voltage 1 and 1/2 LSB below positive full scale which is +4.9963 V for the ±5 V range or +9.9927 V for the ±10 V range. Adjust the gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111.

ALTERNATIVE

In some applications, a full scale of 10.24 V (for an LSB of 2.5 mV) or 20.48 V (for an LSB of 5.0 mV) is more convenient. In the Unipolar mode of operation, replace R2 with a 200 Ω potentiometer and add 150 Ω in series with pin 13 for 10.24 V input range or 500 Ω in series with pin 14 for 20.48 V input range. In bipolar mode of operation, replace R1 with a 500 Ω potentiometer (in addition to the previous changes). The calibration will remain similar to the standard calibration procedure.

Figure 11 - Unipolar Input Connections

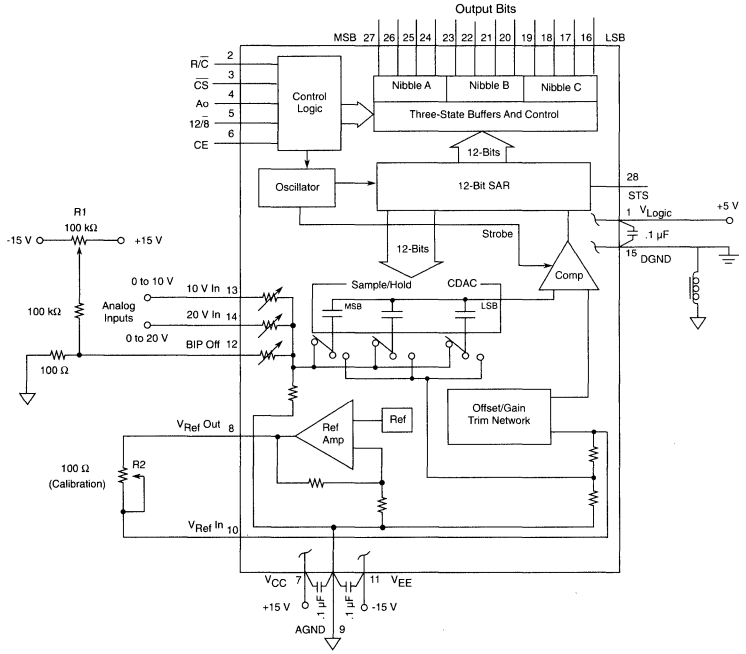
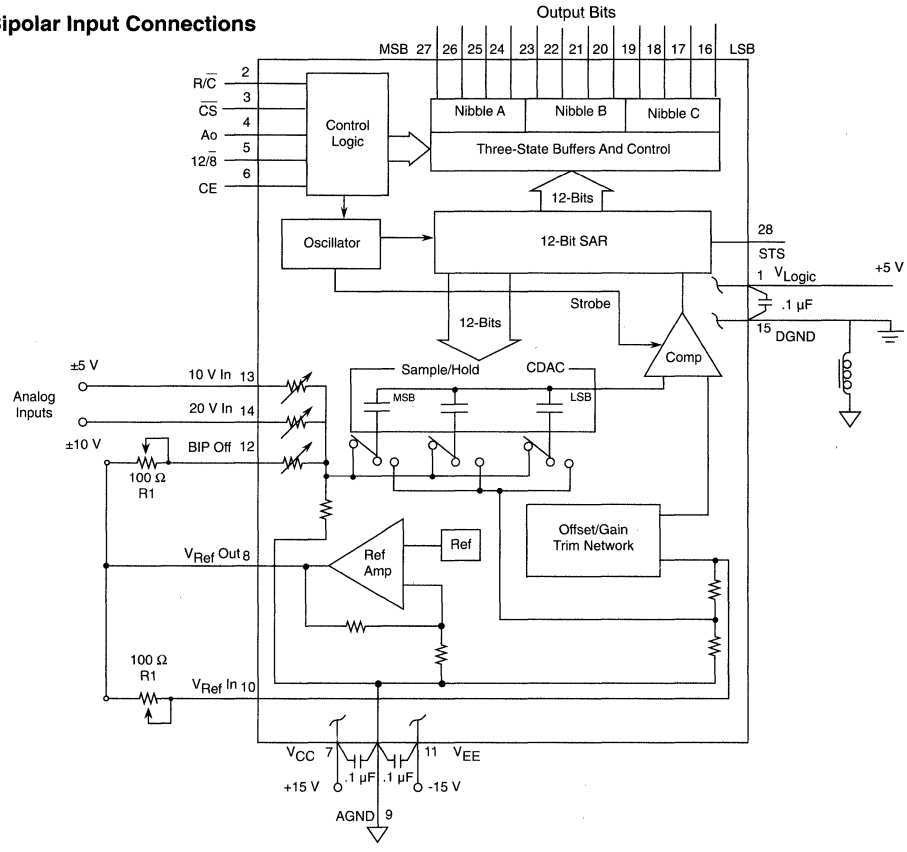


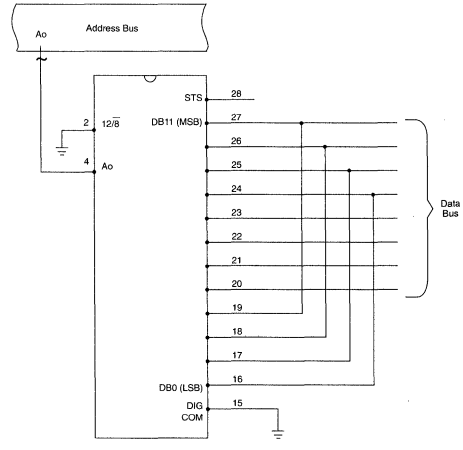
Figure 12 - Bipolar Input Connections



CONTROLLING THE HADC674Z

The HADC674Z can be operated by most microprocessor systems due to the control input pins and on-chip logic. It may also be operated in the stand-alone mode and enabled by the R/$\overline{C}$ input pin. Full µP control consists of selecting an 8 or 12-bit conversion cycle, initiating the conversion, and reading the output data when ready. The output read has the options of choosing either 12-bits at once or 8 bits followed by 4 bits in a left-justified format. All five control inputs are TTL/CMOS compatible and include 12/$\overline{8}$, $\overline{CS}$, Ao, R/$\overline{C}$ and CE. The use of these inputs in controlling the converter's operations is shown in table I, and the internal control logic is shown in a simplified schematic in figure 14.

Figure 13 - Interfacing the HADC674Z to an 8-bit Data Bus



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STAND-ALONE OPERATION

The simplest interface is a control line connected to R/$\overline{C}$. The output controls must be tied to known states as follows: CE and 12/$\overline{8}$ are wired high, Ao and $\overline{CS}$ are wired low. The output data arrives in words of 12-bits each. The limits on R/$\overline{C}$ duty cycle are shown in figures 3 and 4. It may have a duty cycle within and including the extremes shown in the specifications. In general, data may be read when R/$\overline{C}$ is high unless STS is also high, indicating a conversion is in progress.

Table I - Truth Table for the HADC674Z Control Inputs

CONVERSION LENGTH

A conversion start transition latches the state of Ao as shown

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	Ao	Operation
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12 bit conversion
↑	0	0	X	1	Initiate 8 bit conversion
1	↓	0	X	0	Initiate 12 bit conversion
1	↓	0	X	1	Initiate 8 bit conversion
1	0	↓	X	0	Initiate 12 bit conversion
1	0	↓	X	1	Initiate 8 bit conversion
1	0	1	1	X	Enable 12 bit Output
1	0	1	0	0	Enable 8 MSB's Only
1	0	1	0	1	Enable 4 LSB's Plus 4 Trailing Zeroes

in figure 13 and table I. The latched state determines if the conversion stops with 8-bit (Ao high) or continues for 12-bits (Ao low). If all 12-bits are read following an 8-bit conversion, the three LSB's will be a logic "0" and DB3 will be a logic 1. Ao is latched because it is also involved in enabling the output buffers as will be explained later. No other control inputs are latched.

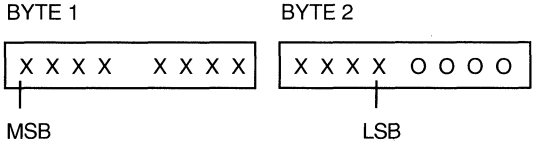
CONVERSION START

A conversion may be initiated by a logic transition on any of the three inputs: CE, $\overline{CS}$, R/$\overline{C}$, as shown in table I. The last of the three to reach the correct state starts the conversions, so one, two or all three may be dynamically controlled. The nominal delay from each is the same and all three may change state simultaneously. In order to assure that a particular input controls the start of conversion, the other two should be set up at least 50 ns earlier. Refer to the convert mode timing specifications. The Convert Start timing diagram is illustrated in figure 1.

The output signal STS is the status flag and goes high only when a conversion is in progress. While STS is high, the output buffers remain in a high impedance state so that data can not be read. Also, when STS is high, an additional Start Convert will not reset the converter or reinitiate a conversion. Note, if Ao changes state after a conversion begins, an additional Start Convert command will latch the new start of Ao and possibly cause a wrong cycle length for that conversion (8 versus 12-bits).

READING THE OUTPUT DATA

The output data buffers remain in a high impedance state until the following four conditions are met: R/$\overline{C}$ is high, STS is low, CE is high, and $\overline{CS}$ is low. The data lines become active in response to the four conditions and output data according to the conditions of 12/$\overline{8}$ and Ao. The timing diagram for this process is shown in figure 2. When 12/$\overline{8}$ is high, all 12 data outputs become active simultaneously and the Ao input is ignored. This results in east interface to a 12 or 16-bit data bus. The 12/$\overline{8}$ input is usually tied high or low, although it is TTL/CMOS compatible. When 12/$\overline{8}$ is low, the output is separated into two 8-bit bytes as shown below:



This configuration makes it easy to connect to an 8-bit data bus as shown in figure 13. The Ao control can be connected to the least significant bit of the address bus in order to store the output data into two consecutive memory locations. When Ao is pulled low, the 8 MSBs are enabled only. When Ao is high, the 4 MSBs are disabled, bits 4 through 7 are forced to a zero and the four LSBs are enabled. The two byte format is left justified data as shown above and can be considered to have a decimal point or binary to the left of byte 1.

Ao may be toggled without damage to the converter at any time. Break-before-make action is guaranteed between the two data bytes. This assures that the outputs which are strapped together in figure 13 will never be enabled at the same time.

In figure 2, it can be seen that a read operation usually begins after the conversion is completed and STS is low. If earlier access is needed, the read can begin no later than the addition of time t_{DD} and t_{HS} before STS goes low.

Figure 14 - Control Logic

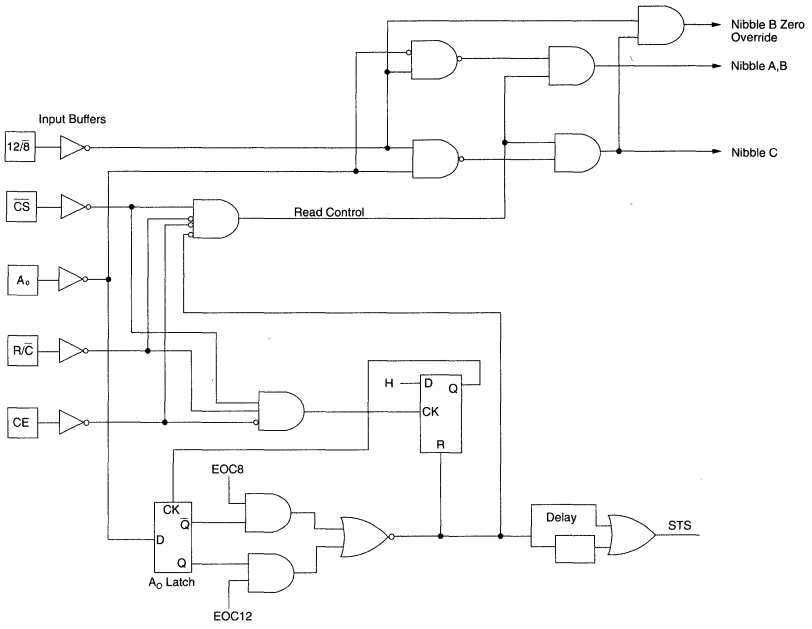
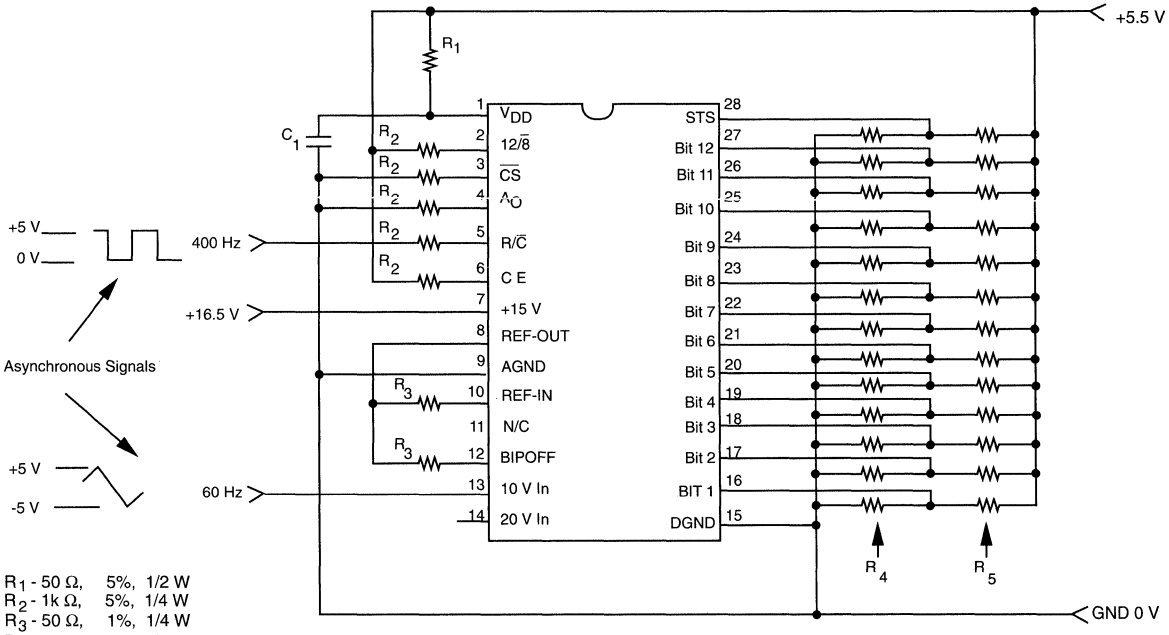


Figure 15 - Burn-In Schematic



R_1 - 50 Ω, 5%, 1/2 W
R_2 - 1k Ω, 5%, 1/4 W
R_3 - 50 Ω, 1%, 1/4 W
R_4 - 10 kΩ, 5%, 1/4 W
R_5 - 3.3 kΩ, 5%, 1/4 W
C_1 - 1 µF, 5%

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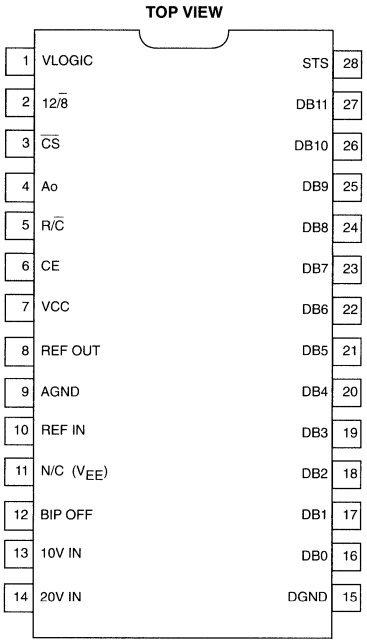
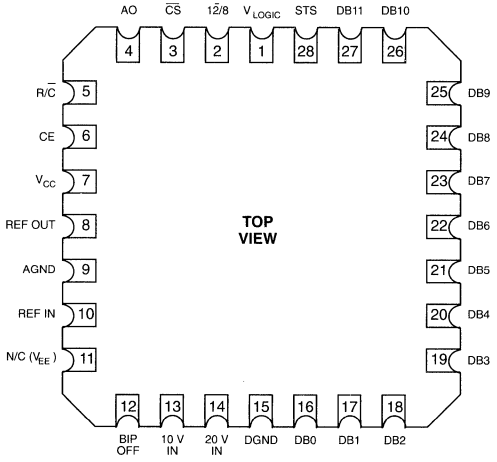
PIN Assignment HADC674Z



28 LEAD DIP



28 Lead LCC

PIN Functions HADC674Z

NAME	FUNCTION
V_{LOGIC}	Logic Supply Voltage, Nominally +5 V
12/$\overline{8}$	Data Mode Selection
$\overline{CS}$	Chip Selection
Ao	Byte Address/Short Cycle
R/$\overline{C}$	Read/Convert
CE	Chip Enable
V_{CC}	Analog Positive Supply Voltage, Nominally +15 V
REF OUT	Reference Output, Nominally +10 V
AGND*	Analog Ground
REF IN	Reference Input
N/C (V_{EE})	This pin is not connected to the device.
BIP OFF	Bipolar Offset
10 V IN	10 Volt Analog Input
20 V IN	20 Volt Analog Input
DGND	Digital Ground
DB0 - DB11	Digital Data Output DB11 - MSB DB0 - LSB
STS	Status

* The lids on the sidebrazed and LCC packages are internally connected to AGND.

LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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SIGNAL PROCESSING TECHNOLOGIES

SPT774

FAST, COMPLETE 12-BIT µP COMPATIBLE A/D CONVERTER WITH SAMPLE/HOLD

FEATURES

- Improved Pin-To-Pin Compatible Monolithic Version of the HI774
- Complete 12-Bit A/D Converter with Sample/Hold, Reference and Clock
- Low Power Dissipation (150 mW Max)
- 12-Bit Linearity (Over Temp)
- 8 µs Max Conversion Time Including S/H Acquisition
- No Negative Supply Required
- Full Bipolar and Unipolar Input Range

APPLICATIONS

- Military/Industrial Data Acquisition Systems
- 8 or 12-Bit µP Input Functions
- Process Control Systems
- Test and Scientific Instruments
- Personal Computer Interface

3

GENERAL DESCRIPTION

The SPT774 is a complete, 12-bit successive approximation A/D converter. Included on the chip are an internal reference, clock, and a sample-and-hold. The S/H allows full Nyquist sampling of input signals.

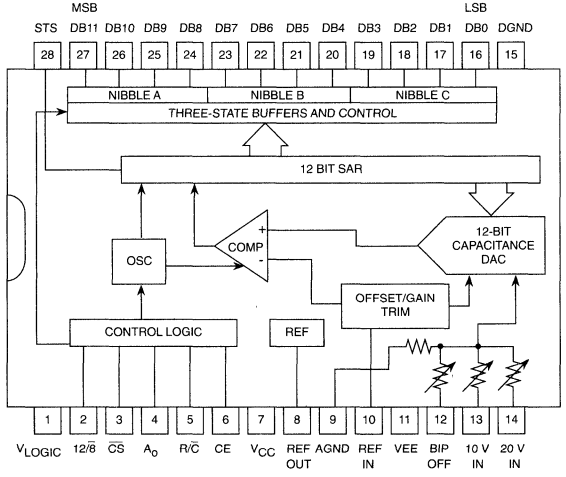
The SPT774 features 8 µs (max) conversion time of 10 or 20 V input signals. Also, a three-state output buffer is added for direct interface to an 8, 12, or 16-bit µP bus.

The BEMOS process and monolithic construction reduces power consumption and ground noise and keeps parasitics to a minimum. In addition, the thin film available on this process allows active adjustment of DAC and comparator offsets, linearity errors, and gain errors.

The SPT774 has standard bipolar and unipolar input ranges of 10 V and 20 V that are controlled by a bipolar offset pin and laser trimmed for specified linearity, gain and offset accuracy.

Power requirements are +5 V and +12 V to +15 V with a maximum dissipation of 150 mW at the specified voltages. Power consumption is about five times lower than that of currently available devices, and a negative power supply is not needed.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING (Beyond which damage may occur) [1] 25 °C

Supply Voltages

Positive Supply Voltage (V_{CC} to DGND) ..... 0 to +16.5 V
Logic Supply Voltage (V_{LOGIC} to DGND) ..... 0 to +7 V
Analog to Digital Ground (AGND to DGND) . -0.5 to +1 V

Input Voltages

Control Input Voltages (to DGND)
(CE, CS, Ao, 12/8, R/C) ..... -0.5 to V_{LOGIC} +0.5 V
Analog Input Voltage (to AGND)
(REF IN, BIP OFF, 10 Vin) ..... ±16.5 V
20 V Vin Input Voltage (to AGND) ..... ±24 V

Output

Reference Output Voltage ..... Indefinite short to GND
Momentary short to V_{CC}

Temperature

Operating Temperature, ambient ..... -55 to +125 °C
junction ..... +175 °C
Lead Temperature, (soldering 10 seconds) ..... +300 °C
Storage Temperature ..... -65 to +150 °C
Power Dissipation ..... 1000 mW
Thermal Resistance (θ_{jA}) ..... 48 °C/W

Note: Operation at any Absolute Maximum Rating is not implied. See Operating Conditions for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

T_A=T_{MIN} to T_{MAX}, V_{CC}=+15 V or +12 V, V_{LOGIC}=+5 V, unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEST LEVEL	SPT774C MIN	SPT774C TYP	SPT774C MAX	SPT774B MIN	SPT774B TYP	SPT774B MAX	SPT774A MIN	SPT774A TYP	SPT774A MAX	UNITS
DC ELECTRICAL CHARACTERISTICS												
Resolution		VI			12			12			12	BITS
Linearity Error[1]	T_A=0 to 70 °C	VI			±1			±1/2			±1/2	LSB
T_A = -25 to +85 °C	I			±1			±1/2			±1/2	LSB	
T_A = -55 to +125 °C	I			±1			±1			±1	LSB	
Differential Linearity	No Missing Codes	VI	11			12			12			BITS
Unipolar Offset; 10 V, 20 V	+25 °C Adjustable to Zero	VI		±0.1	±2		±0.1	±2		±0.1	±2	LSB
Bipolar Offset1; ±5 V,±10 V	+25 °C Adjustable to Zero	VI			±10			±4			±4	LSB
Full Scale Calibration Error[2] All Input Ranges	+25 °C Adjustable to Zero	VI			0.3			0.3			0.3	% of FS
	No Adjustment at +25°											
	T_A = 0 to 70 °C	V		0.5			0.4			0.35		%of FS
T_A = -25 to +85 °C	V		0.7			0.5			0.4		%of FS	
T_A = -55 to +125 °C	V		0.8			0.6			0.4		%of FS	
With Adjustment at +25 °C												
T_A = 0 to 70 °C	V		0.22			0.12			0.05		%of FS	
T_A = -25 to +85 °C	V		0.4			0.2			0.1		%of FS	
T_A = -55 to +125 °C	V		0.5			0.25			0.12		%of FS	
Temperature Coefficients[3]	Using Internal Reference											
Unipolar Offset	T_A = 0 to 70 °C	IV		±0.2	±2		±0.1	±1		±0.1	±1	LSB
					(10)			(5)			(5)	(ppm/°C)
	T_A = -25 to +85 °C	IV			±2			±1			±1	LSB
					(5)			(2.5)			(2.5)	(ppm/°C)
T_A = -55 to +125 °C	IV			±2			±1			±1	LSB	
					(5)			(2.5)			(2.5)	(ppm/°C)
Bipolar Offset	T_A = 0 to 70 °C	IV		±0.2	±2		±0.1	±1		±0.1	±1	LSB
					(10)			(5)			(5)	(ppm/°C)
	T_A = -25 to +85 °C	IV			±2			±1			±1	LSB
					(5)			(2.5)			(2.5)	(ppm/°C)

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ELECTRICAL SPECIFICATIONS

$T_A = T_{MIN}$ to T_{MAX}, V_{CC} = +15 V or +12 V, V_{LOGIC} = +5 V, unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEST LEVEL	SPT774C MIN	SPT774C TYP	SPT774C MAX	SPT774B MIN	SPT774B TYP	SPT774B MAX	SPT774A MIN	SPT774A TYP	SPT774A MAX	UNITS
DC ELECTRICAL CHARACTERISTICS												
Bipolar Offset (Cont.)	T_A = -55 to +125 °C	IV			±4			±2			±1	LSB
					(10)			(5)			(2.5)	(ppm/°C)
Full Scale Calibration	T_A = 0 to 70 °C	IV			±9			±5			±2	LSB
					(45)			(25)			(10)	(ppm/°C)
	T_A = -25 to +85 °C	IV			±12			±7			±3	LSB
					(50)			(25)			(12)	(ppm/°C)
	T_A = -55 to +125 °C	IV			±20			±10			±5	LSB
					(50)			(25)			(12.5)	(ppm/°C)
Power Supply Rejection	Max change in full scale calibration											
+13.5 V<V_{CC}<+16.5 V or +11.4 V<V_{CC}<+12.6 V		VI		±0.5	±2		±0.5	±1		±0.5	±1	LSB
+4.5 V<V_{LOGIC}<+5.5 V		VI		±0.1	±0.5		±0.1	±0.5		±0.1	±0.5	LSB
Analog Input Ranges												
Bipolar		VI	-5		+5	-5		+5	-5		+5	Volts
			-10		+10	-10		+10	-10		+10	Volts
Unipolar		VI	0		+10	0		+10	0		+10	Volts
			0		+20	0		+20	0		+20	Volts
Input Impedance												
10 Volt Span		VI	3.75	5	6.25	3.75	5	6.25	3.75	5	6.25	kΩ
20 Volt Span			15	20	25	15	20	25	15	20	25	kΩ
Power Supplies Operating Voltage Range												
V_{LOGIC}		VI	+4.5		+5.5	+4.5		+5.5	+4.5		+5.5	Volts
V_{CC}		VI	+11.4		+16.5	+11.4		+16.5	+11.4		+16.5	Volts
V_{EE}	Not Required for circuit operation.											
Operating Current												
I_{LOGIC}		VI		0.5	1		0.5	1		0.5	1	mA
I_{CC}		VI		7	9		7	9		7	9	mA
I_{EE}	Not required for circuit operation.											
Power Dissipation												
+15 V, +5 V		VI		110	150		110	150		110	150	mW
Internal Reference Voltage		VI	9.97	10	10.03	9.97	10	10.03	9.97	10	10.03	Volts
Output Current[4]		VI			2			2			2	mA

ELECTRICAL SPECIFICATIONS

$T_A = T_{MIN}$ to T_{MAX}, V_{CC} = +15 V or +12 V, V_{LOGIC} = +5 V, unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEST LEVEL	SPT774C MIN	SPT774C TYP	SPT774C MAX	SPT774B MIN	SPT774B TYP	SPT774B MAX	SPT774A MIN	SPT774A TYP	SPT774A MAX	UNITS
DIGITAL CHARACTERISTICS												
Logic Inputs (CE, $\overline{CS}$, R/$\overline{C}$, Ao, 12/$\overline{8}$)												
Logic "0"		VI	-0.5		+0.8	-0.5		+0.8	-0.5		+0.8	Volts
Logic "1"		VI	2.0		5.5	2.0		5.5	2.0		5.5	Volts
Current	0 to 5.5 V Input	VI		±.01	+1		±.01	+1		±.01	+1	µA
Capacitance		V		5			5			5		pF
Logic Outputs (DB11-DB0, STS)												
Logic "0"	(I_{Sink} = 1.6 mA)	VI			+0.4			+0.4			+0.4	Volts
Logic "1"	(I_{SOURCE} = 500 µA)	VI	+2.4			+2.4			+2.4			Volts
Leakage	(High Z State, DB11-DB0 Only)	VI	-5	±0.1	+5	-5	±0.1	+5	-5	±0.1	+5	µA
Capacitance		V		5			5			5		pF

Note 1: For military temperature range, the device linearity is guaranteed to be 1/2 LSB at 25 °C.
Note 2: Fixed 50 Ω resistor from REF OUT to REF IN and REF OUT to BIP OFF.
Note 3: Full Tempco testing is performed on all Grade A and MIL-STD-883 devices.
Note 4: Available for external loads; external load should not change during conversion. When supplying an external load and operating on a +12.0 V supply, a buffer amplifier must be provided for the reference output.

4755 Forge Road, Co. Springs, CO 80907
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ELECTRICAL SPECIFICATIONS

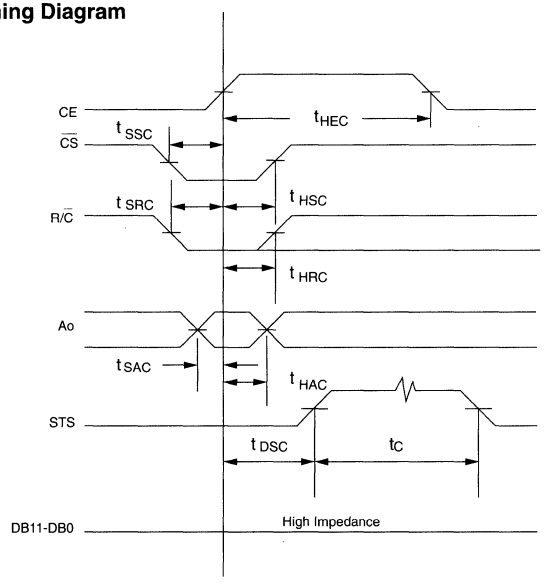
CONVERT MODE TIMING CHARACTERISTICS

T_A = +25 °C, V_{CC} = +15.0 V or +12 V, V_{LOGIC} = +5 V, unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEST LEVEL	SPT774C MIN	SPT774C TYP	SPT774C MAX	SPT774B MIN	SPT774B TYP	SPT774B MAX	SPT774A MIN	SPT774A TYP	SPT774A MAX	UNITS
AC ELECTRICAL CHARACTERISTICS[5]												
t_{DSC} STS Delay from CE		I			200			200			200	ns
t_{HEC} CE Pulse Width		I	50			50			50			ns
t_{SSC} $\overline{CS}$ to CE Setup		I	50			50			50			ns
t_{HSC} $\overline{CS}$ Low during CE High		I	50			50			50			ns
t_{SRC} R/$\overline{C}$ to CE Setup		I	50			50			50			ns
t_{HRC} R/$\overline{C}$ Low During CE High		I	50			50			50			ns
t_{SAC} Ao to CE Setup		I	0			0			0			ns
t_{HAC} Ao Valid During CE High		I	50			50			50			ns
t_C Conversion Time												
12-Bit Cycle	T_{MIN} to T_{MAX}	I	7.0	7.5	8.0	7.0	7.5	8.0	7.0	7.5	8.0	µs
8-Bit Cycle	T_{MIN} to T_{MAX}	I	4.85	5.25	5.65	4.85	5.25	5.65	4.85	5.25	5.65	µs

Note 5: Time is measured from 50% level of digital transitions. Parameters are tested with a 100 pF and 3 kΩ load for high impedance to drive and tested with 10 pF and 3 kΩ load for drive to high impedance.

Figure 1 - Convert Mode Timing Diagram



ELECTRICAL SPECIFICATIONS

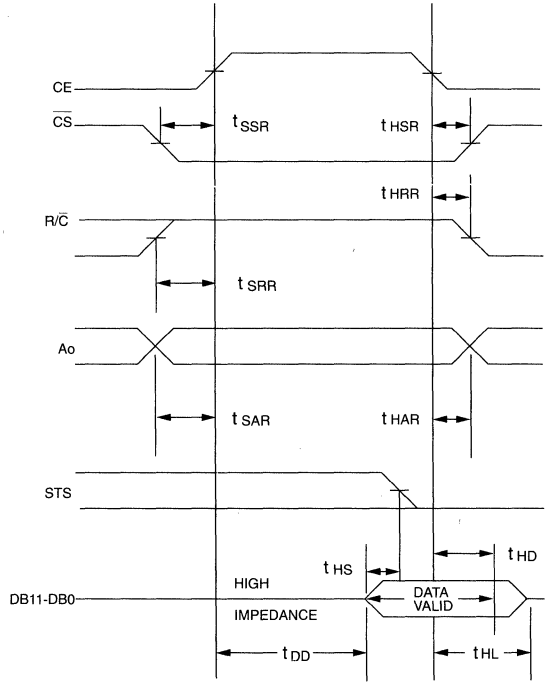
READ MODE TIMING CHARACTERISTICS

T_A = 25 °C, V_{CC} = +15.0 V or +12 V, V_{LOGIC} = +5 V, unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEST LEVEL	SPT774C MIN	SPT774C TYP	SPT774C MAX	SPT774B MIN	SPT774B TYP	SPT774B MAX	SPT774A MIN	SPT774A TYP	SPT774A MAX	UNITS
AC ELECTRICAL CHARACTERISTICS[6]												
t_{DD} Access Time from CE		I			150			150			150	ns
t_{HD} Data Valid After CE Low		I	25			25			25			ns
t_{HL} Output Float Delay		I			150			150			150	ns
t_{SSR} $\overline{CS}$ to CE Setup		I	50	0		50	0		50	0		ns
t_{SRR} R/$\overline{C}$ to CE Setup		I	0	0		0	0		0	0		ns
t_{SAR} Ao to CE Setup		I	50			50			50			ns
t_{HSR} $\overline{CS}$ Valid After CE Low		I	0	0		0	0		0	0		ns
t_{HRR} R/$\overline{C}$ High After CE Low		I	50			50			50			ns
t_{HS} STS Delay After Data Valid		I	90		300	90		300	90		300	ns
t_{HAR} Ao Valid after CE Low		I	50			50			50			ns

Note 6: Time is measured from 50% level of digital transitions. Parameters are tested with a 100 pF and 3 kΩ load for high impedance to drive and tested with 10 pF and 3 kΩ load for drive to high impedance.

Figure 2 - Read Mode Timing Diagram



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ELECTRICAL SPECIFICATIONS

STAND-ALONE MODE TIMING CHARACTERISTICS

T_A = 25 °C, V_{CC} = +15.0 V or +12 V, V_{LOGIC} = +5 V, unless otherwise specified.

PARAMETER	TEST CONDITIONS	TEST LEVEL	SPT774C MIN	SPT774C TYP	SPT774C MAX	SPT774B MIN	SPT774B TYP	SPT774B MAX	SPT774A MIN	SPT774A TYP	SPT774A MAX	UNITS
AC ELECTRICAL CHARACTERISTICS[6]												
t_{HRL} Low R/$\overline{C}$ Pulse Width		I	50			50			50			ns
t_{DS} STS Delay from R/$\overline{C}$		I			200			200			200	ns
t_{HDR} Data Valid After R/$\overline{C}$ Low		I	25			25			25			ns
t_{HS} STS Delay After Data Valid		I	90		300	90		300	90		300	ns
t_{HRH} High R/$\overline{C}$ Pulse Width		I	150			150			150			ns
t_{DDR} Data Access Time		I			150			150			150	ns
SAMPLE-AND-HOLD												
Acquisition Time		IV	1.35	1.45	1.55	1.35	1.45	1.55	1.35	1.45	1.55	µs
Aperture Uncertainty Time		V		1			1			1		ns,RMS

Figure 3 - Low Pulse for R/$\overline{C}$ - Outputs Enabled After Conversion

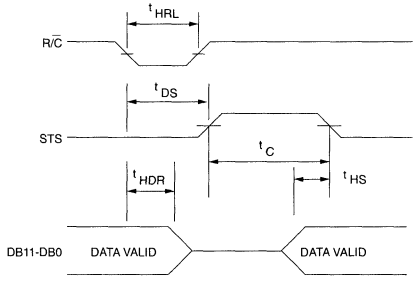
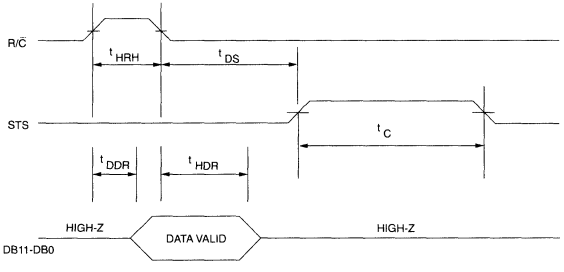


Figure 4 - High Pulse for R/$\overline{C}$ - Outputs Enabled While R/$\overline{C}$ is High, Otherwise High Impedance



TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests; therefore, $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

DEFINITION OF SPECIFICATIONS

INTEGRAL LINEARITY ERROR

Linearity error refers to the deviation of each individual code from a line drawn from "zero" through "full scale" with all offset errors nulled out. (See figures 5 and 6.) The point used as "zero" occurs 1/2 LSB (1.22 mV for a 10 volt span) before the first code transition (all zeros to only the LSB "on"). "Full scale" is defined as a level 1 and 1/2 LSB beyond the last code transition (to all ones). The deviation of a code from the true straight line is measured from the middle of each particular code.

The SPT774AC and BC grades are guaranteed for maximum nonlinearity of ±1/2 LSB. For these grades, this means that an analog value that falls exactly in the center of a given code width will result in the correct digital output code. Values nearer the upper or lower transition of the code width may produce the next upper or lower digital output code. The SPT774AM, BM, CC and CM grades are guaranteed to ±1 LSB maximum error. For these grades, an analog value that falls within a given code width will result in either the correct code for the region or either adjacent one. The linearity is not user-adjustable.

DIFFERENTIAL LINEARITY ERROR (NO MISSING CODES)

A specification that guarantees no missing codes requires that every code combination appear in a monotonically increasing sequence as the analog input level is increased. Thus every code must have a finite width. For the SPT774 type AC, BC, AM and BM grades, that guarantee no missing codes to 12-bit resolution, all 4096 codes must be present over the entire operating temperature ranges. The SPT774 CC and CM grades guarantee no missing codes to 11-bit resolution over temperature; this means that all code combinations of the upper 11-bits must be present. In practice, very few of the 12-bit codes are missing.

DIFFERENTIAL NONLINEARITY

Differential nonlinearity is a measure of how much the actual quantization step width varies from the ideal step width of 1 LSB. Figure 6 shows a differential nonlinearity of 2 LSB - the actual step width is 3 LSB. The SPT774's specification gives the worst case differential nonlinearity in the A/D transfer function under specified dynamic operating conditions. Small, localized differential nonlinearities may be insignificant when digitizing full scale signals. However, if a low level input signal happens to fall on the part of the A/D transfer function with the differential nonlinearity error, the effect will be significant.

MISSING CODES

Missing codes represent a special kind of differential nonlinearity. The quantization step width for a missing code is 0 LSB which results in a differential nonlinearity of -1 LSB. Figure 6 points out two missed codes in the transfer function.

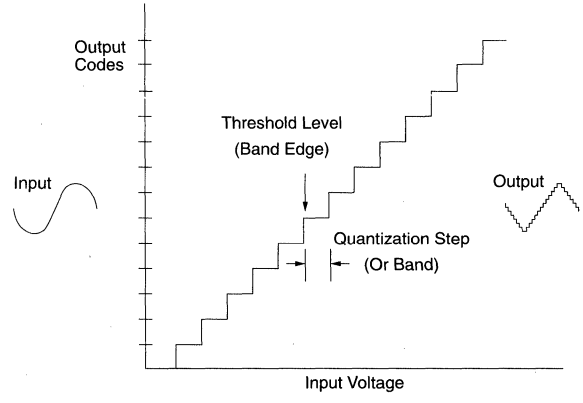
QUANTIZATION UNCERTAINTY

Analog-to-digital converters exhibit an inherent quantization uncertainty of ±1/2 LSB. This uncertainty is a fundamental characteristic of the quantization process and cannot be reduced for a converter of a given resolution.

QUANTIZATION ERROR

Quantization error is the fundamental, irreducible error associated with the perfect quantizing of a continuous (analog) signal into a finite number of digital bits (A/D transfer function). A 12-bit A/D converter can represent an input voltage with a best case uncertainty of 1 part in 2^{12} (1 part in 4096). In real A/Ds under dynamic operating conditions, the quantization bands (bit change step vs input amplitude) for certain codes can be significantly larger (or smaller) than the ideal. The ideal width of each quantization step (or band) is $Q=FSR/2^N$ where FSR=full scale range and N=12. Nonideal quantization bands represent differential non linearity errors. (See figures 5, 6 and 7.)

Figure 5 - Static Input Conditions



RESOLUTION - ACTUAL vs AVAILABLE

The available resolution of an N-bit converter is 2^N. This means it is theoretically possible to generate 2^N unique output codes.

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Figure 6 - Dynamic Conditions

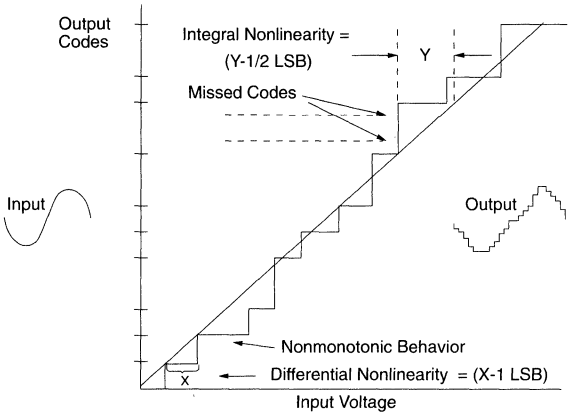
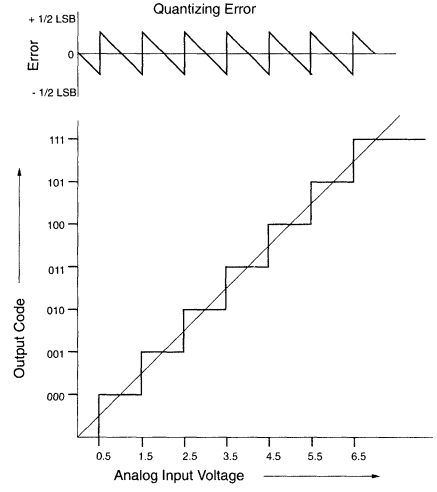


Figure 7 - Quantizing Error



THROUGHPUT

Maximum throughput is the greatest number of conversions per second at which an ADC will deliver its full rate performance. This is equivalent to the inverse of the sum of the multiplex time (if applicable), the S/H settling time and the conversion time.

GAIN

Gain is the slope of the transfer curve. Gain is generally user adjustable to compensate for long term drift.

ACQUISITION TIME/APERTURE DELAY TIME

In the SPT774, this is the time delay between the R/$\overline{C}$ falling edge and the actual start of the HOLD mode in a sample-and-hold function.

APERTURE JITTER

This is a specification indicating how much the aperture delay time varies between samples.

SUCCESSIVE APPROXIMATION ADC

The successive approximation converter uses an architecture with inherently high throughput rates that converts high frequency signals with great accuracy. A sample-and-hold type circuit can be used on the input to freeze these signals during conversion.

An N-bit successive approximation converter performs a sequence of tests comparing the input voltage to a successively narrower voltage range. The first range is half full scale, the next is quarter full scale, etc., until it reaches the Nth test which narrows it to a range of $1/2^N$ of full scale. The conversion time is fixed by the clock frequency and is thus independent of the input voltage.

UNIPOLAR OFFSET

The first transition should occur at a level 1/2 LSB above analog common. Unipolar offset is defined as the deviation of the actual transition from that point. This offset can be adjusted as discussed on the following pages. The unipolar offset temperature coefficient specifies the maximum change of the transition point over temperature, with and without external adjustment.

BIPOLAR OFFSET

In the bipolar mode, the major carry transition (0111 1111 1111 to 1000 0000 0000) should occur for an analog value 1/2 LSB below analog common. The bipolar offset error and temperature coefficient specify the initial deviation and maximum change in the error over temperature.

CONVERSION TIME

This is the time required to complete a conversion over the specified operating range. Conversion time can be expressed as time/bit for a converter with selectable resolution or as time/conversion when the number of bits is constant. The SPT774 is specified as time/conversion for all 12-bits. Conversion time should not be confused with maximum allowable analog input frequency which is discussed later.

FULL SCALE CALIBRATION ERROR

The last transition (from 1111 1111 1110 to 1111 1111 1111 1111) should occur for an analog value 1 and 1/2 LSB below the nominal full scale (9.9963 volts for 10.000 volts full scale). The full scale calibration error is the deviation of the actual level at the last transition from the ideal level. This error, which typically is 0.05 to 0.1% of full scale, can be trimmed out as show in figures 11 and 12. The full scale calibration error over temperature is given with and without the initial error trimmed out. The temperature coefficients for each grade indicate the maximum change in the full scale gain from the initial value using the internal 10 volt reference.

TEMPERATURE COEFFICIENTS

The temperature coefficients for full scale calibration, unipolar offset, and bipolar offset specify the maximum change from the initial (25 °C) value to the value at Tmin or Tmax.

POWER SUPPLY REJECTION

The standard specifications for the SPT774 assume +5.00 and +15.00 or +12.00 volt supplies. The only effect of power supply error on the performance of the device will be a small change in the full scale calibration. This will result in a linear change in all lower order codes. The specifications show the maximum change in calibration from the initial value with the supplies at the various limits.

CODE WIDTH

The fundamental unit for A/D converter specifications is the code width. This is defined as the range of analog input values for which a given digital output code will occur. The nominal value of a code width is equivalent to one least significant bit (LSB) of the full scale range or 2.44 mV out of 10 volts for a 12-bit ADC.

LEFT-JUSTIFIED DATA

The data format used in the SPT774 is left-justified. This means that the data represents the analog input as fraction of full scale, ranging from 0 to 4095/4096. This implies a binary point to the left of the MSB.

MONOTONICITY

This characteristic describes an aspect of the code to code progression from minimum to maximum input. A device is said to be monotonic if the output code continuously increases as the input signal increases, and if the output code continuously decreases as the input signal decreases. Figure 6 demonstrates nonmonotonic behavior.

CIRCUIT OPERATION

The SPT774 is a complete 12-bit analog-to-digital converter that consists of a single chip version of the industry standard 774. This single chip contains a precision 12-bit capacitor digital-to-analog converter (CDAC) with voltage reference, comparator, successive approximation register (SAR), sample-and-hold, clock, output buffers and control circuitry to make possible to use the SPT774 with few external components.

When the control section of the SPT774 initiates a conversion command, the clock is enabled and the successive-approximation register is reset to all zeros. Once the conversion cycle begins, it cannot be stopped or restarted and data is not available from the output buffers.

The SAR, timed by the clock, sequences through the conversion cycle and returns an end-of-convert flag to the control section of the ADC. The clock is then disabled by the control section, the output status goes low, and the control section is enabled to allow the data to be read by external command.

The internal SPT774 12-bit CDAC is sequenced by the SAR starting from the MSB to the LSB at the beginning of the conversion cycle to provide an output voltage from the CDAC that is equal to the input signal voltage (which is divided by the input voltage divider network). The comparator determines whether the addition of each successively-weighted bit voltage causes the CDAC output voltage summation to greater or less than the input voltage; if the sum is less, the bit is left on; if more, the bit is turned off. After testing all the bits, the SAR contains a 12-bit binary code which accurately represents the input signal to within ±1/2 LSB.

The internal reference provides the voltage reference to the CDAC with excellent stability over temperature and time. The reference is trimmed to 10.00 volts ±1% and can supply up to 2 mA to an external load in addition to that required to drive the reference input resistor (1 mA) and offset resistor (1 mA) when operating with ±15 V supplies. If the SPT774 is used with ±12 V supplies, or if external current must be supplied over the full temperature range, and external buffer amplifier is recommended. Any external load on the SPT774 reference must remain constant during conversion.

The sample-and-hold feature is a bonus of the CDAC architecture. Therefore the majority of the S/H specifications are included within the A/D specifications.

Although the sample-and-hold circuit is not implemented in the classical sense, the sampling nature of the capacitive DAC makes the SPT774 appear to have a built in sample-and-hold. This sample-and-hold action substantially increases the signal bandwidth of the SPT774 over that of similar competing devices.

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Note that even though the user may use an external sample-and-hold for very high frequency inputs, the internal sample-and-hold still provides a very useful isolation function. Once the internal sample is taken by the CDAC capacitance, the input of the SPT774 is disconnected from the user's sample-and-hold. This prevents transients occurring during conversion from being inflicted upon the attached sample-and-hold buffer. All other 774 circuits will cause a transient load current on the sample-and-hold which will upset the buffer output and may add error to the conversion itself.

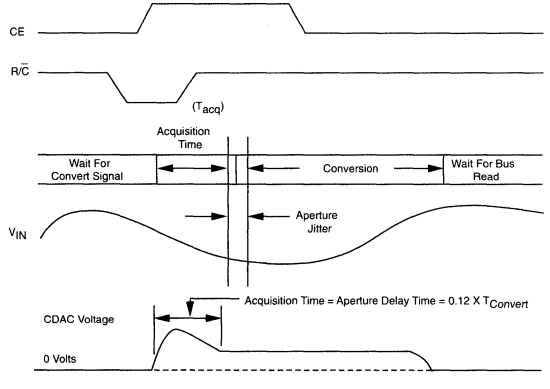
Furthermore, the isolation of the input after the acquisition time in the SPT774 allows the user an opportunity to release the hold on an external sample-and-hold and start it tracking the next sample. This will increase system throughput with the user's existing components.

SAMPLE-AND-HOLD FUNCTION

When using an external S/H, the SPT774 acts as any other 774 device because the internal S/H is transparent. The sample/hold function in the SPT774 is inherent to the capacitor DAC structure, and its timing characteristics are determined by the internally generated clock. However, for limited frequency ranges, the internal S/H may eliminate the need for an external S/H. This function will be explained in the next two sections.

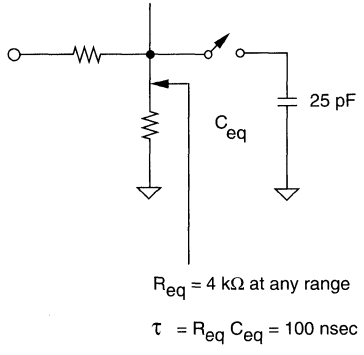
The operation of the S/H function is internal to the SPT774 and is controlled through the normal R/$\overline{C}$ control line. (Refer to figure 8.) When the R/$\overline{C}$ line makes a negative transition, the SPT774 starts the timing of the sampling and conversion. The first two clock cycles are allocated to signal acquisition of the input by the CDAC. (This time is defined as T_{acq}.) Following these two cycles, the input sample is taken and held. The A/D conversion follows this cycle with the duration controlled by the internal clock cycle.

Figure 8 - Sample-and-Hold Function



During T_{acq}, the equivalent circuit of the SPT774 input is as shown in figure 9. (The time constant of the input is independent of which input level is used.) This CDAC capacitance must be charged up to the input voltage during T_{acq}. Since the CDAC time constant is 100 nsecs, there is more than enough time for settling the input to 12-bits of accuracy during T_{acq}. The excess time left during T_{acq} allows the user's buffer amp to settle after being switched to the CDAC load.

Figure 9 - Equivalent SPT774 Input Circuit



Note that because the sample is taken relative to the R/$\overline{C}$ transition, T_{acq} is also the traditional "aperture delay" of this internal sample-and-hold.

Since T_{acq} is measured in clock cycles, its duration will vary with the internal clock frequency. This results in T_{acq} = 1.45 µsec between units and over temperature.

Offset, gain and linearity errors of the S/H circuit as well as the effects of its droop rate are included in the overall specifications for the SPT774.

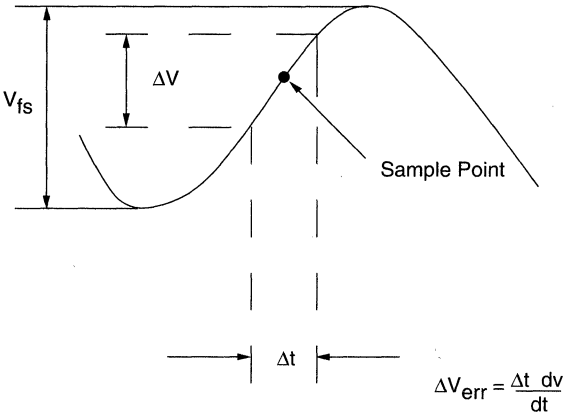
APERTURE UNCERTAINTY

Often the limiting factor in the application of the sample-and-hold is the uncertainty in the time that the actual sample is taken, i.e., the "aperture jitter" or T_{AJ}. The SPT774 has a nominal aperture jitter of 8 nsec between samples. With this jitter, it is possible to accurately sample a wide range of input signals.

The aperture jitter causes an amplitude uncertainty for any input where the voltage is changing. The approximate voltage error due to aperture jitter depends on the slew rate of the signal at the sample point. (See figure 10.) The magnitude of this change for a sine wave can be calculated:

$V_{err} \leq V_{fs}/2^{N+1}$ (where V_{err} is the allowable error voltage and V_{fs} is the full scale voltage)

Figure 10 - Aperture Uncertainty



From figure 10:

$SR=\Delta V/\Delta t=2\ \pi fVp$

Let $\Delta V = V_{err} = V_{fs}(2 - (N+1))$, $Vp = Vin/2$ and $\Delta t = t_{AJ}$ (The time during which unwanted voltage change occurs)

The above conditions then yield:

$V_{fs}/2^{(N+1)} \geq \pi f V_{in}\ t_{AJ}$ or $f_{MAX} \leq V_{fs}/(\pi Vin\ t_{AJ})2^{(N+1)}$

For the SPT774, t_{AJ}=1 nsec, therefore $f_{max} \leq$40 kHz.

For higher frequency signal inputs, an external sample-and-hold is recommended.

TYPICAL INTERFACE CIRCUIT

The SPT774 is a complete A/D converter that is fully operational when powered up and issued a Start Convert Signal. Only a few external components are necessary as shown in figures 11 and 12. The two typical interface circuits are for operating the SPT774 in either an unipolar or bipolar input mode. Information on these connections and on conditions concerning board layout to achieve the best operation are discussed below.

For each application of this device, strict attention must be given to power supply decoupling, board layout (to reduce pickup between analog and digital sections), and grounding. Digital timing, calibration and the analog signal source must be considered for correct operation.

To achieve specified accuracy, a double-sided printed circuit board with a copper ground plane on the component side is recommended. Keep analog signal traces away from digital lines. It is best to lay the PC board out such that there is an analog section and a digital section with a single point ground connection between the two through an RF bead located as closely to the device as possible. If possible, run analog signals between ground traces and cross digital lines at right angles only.

POWER SUPPLIES

The supply voltages for the SPT774 must be kept as quiet as possible from noise pickup and also regulated from transients or drops. Because the part has 12-bit accuracy, voltage spikes on the supply lines can cause several LSB deviations on the output. Switching power supply noise can be a problem. Careful filtering and shielding should be employed to prevent the noise from being picked up by the converter.

Capacitor bypass pairs are needed from each supply pin to its respective ground to filter noise and counter the problems caused by the variations in supply current. A 10 µF tantalum and a 0.1 µF ceramic type in parallel between V_{LOGIC} (pin 1) and digital common (pin 15), and V_{CC} (pin 7) and analog common (pin 9) are sufficient. V_{EE} is generated internally so pin 11 may be grounded or connected to a negative supply if the SPT774 is being used to upgrade an already existing design.

GROUNDING CONSIDERATIONS

Any ground path from the analog and digital ground should be as low resistance as possible to accommodate the ground currents present with this device.

The analog ground current is approximately 6 mADC while the digital ground is 3 mADC. The analog and digital common pins should be tied together as closely to the package as possible to guarantee best performance. The code dependent currents flow through the V_{LOGIC} and V_{CC} terminals and not through the analog and digital common pins.

The SPT774 may be operated by a µP or in the stand-alone mode. The part has four standard input ranges: 0 V to +10 V, 0 V to +20 V, ±5 V and ±10 V. The maximum errors that are listed in the specifications for gain and offset may be adjusted externally to zero as explained in the next two sections.

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CALIBRATION AND CONNECTION PROCEDURES

UNIPOLAR

The calibration procedure consists of adjusting the converter's most negative output to its ideal value for offset adjustment, and then adjusting the most positive output to its ideal value for gain adjustment.

Starting with offset adjustment and referring to figure 11, the midpoint of the first LSB increment should be positioned at the origin to get an output code of all 0s. To do this, an input of +1/2 LSB or +1.22 mV for the 10 V range and +2.44 mV for the 20 V range should be applied to the SPT774. Adjust the offset potentiometer R1 for code transition flickers between 0000 0000 0000 and 0000 0000 0001.

The gain adjustment should be done at positive full scale. The ideal input corresponding to the last code change is applied. This is 1 and 1/2 LSB below the nominal full scale which is +9.9963 V for the 10 V range and +19.9927 V for the 20 V range. Adjust the gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111. If calibration is not necessary for the intended application, replace R2 with a 50 Ω, 1% metal film resistor and remove the network from pin 12. Connect pin 12 to pin 9. Connect the analog input to pin 13 for the 0 V to 10 V range or to pin 14 for the 0 V to 20 V range.

BIPOLAR

The gain and offset errors listed in the specification may be adjusted to zero using the potentiometers R1 and R2. (See figure 12.) If adjustment is not needed, either or both pots may be replaced by a 50 Ω, 1% metal film resistor.

To calibrate, connect the analog input signal to pin 13 for a ±5 V range or to pin 14 for a ±10 V range. First apply a DC input voltage 1/2 LSB above negative full scale which is -4.9988 V for the ±5 V range or -9.9976 V for the ±10 V range. Adjust the offset potentiometer R1 for flicker between output codes 0000 0000 0000 and 0000 0000 0001. Next, apply a DC input voltage 1 and 1/2 LSB below positive full scale which is +4.9963 V for the ±5 V range or +9.9927 V for the ±10 V range. Adjust the gain potentiometer R2 for flicker between codes 1111 1111 1110 and 1111 1111 1111.

ALTERNATIVE

In some applications, a full scale of 10.24 V (for an LSB of 2.5 mV) or 20.48 V (for an LSB of 5.0 mV) is more convenient. In the Unipolar mode of operation, replace R2 with a 200 Ω potentiometer and add 150 Ω in series with pin 13 for 10.24 V input range or 500 Ω in series with pin 14 for 20.48 V input range. In bipolar mode of operation, replace R1 with a 500 Ω potentiometer (in addition to the previous changes). The calibration will remain similar to the standard calibration procedure.

Figure 11 - Unipolar Input Connections

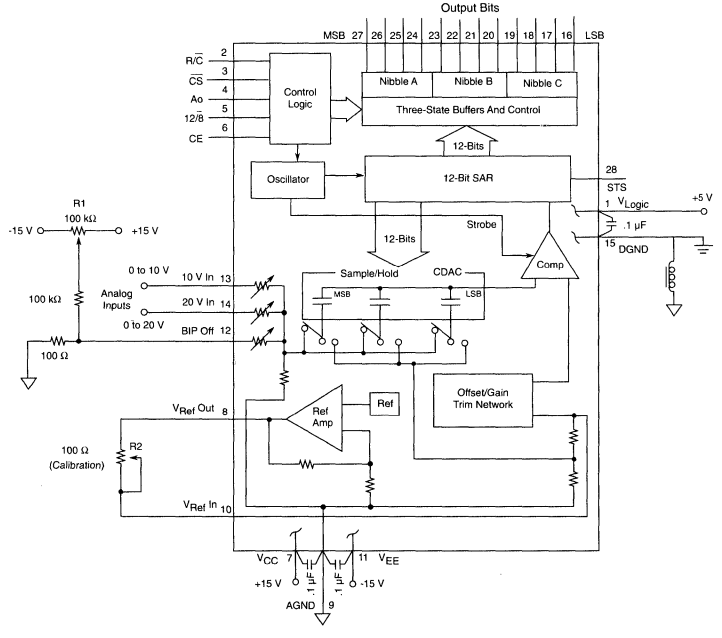
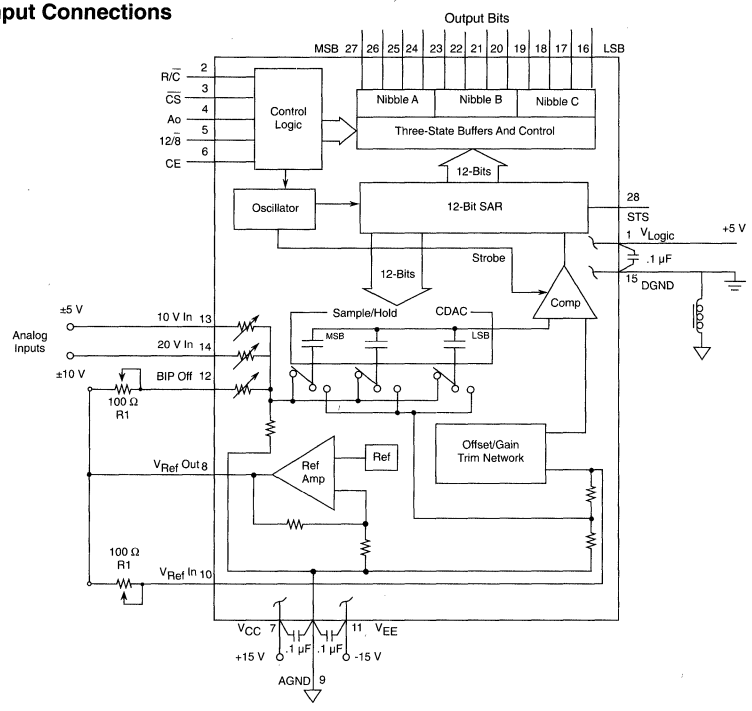


Figure 12 - Bipolar Input Connections



CONTROLLING THE SPT774

The SPT774 can be operated by most microprocessor systems due to the control input pins and on-chip logic. It may also be operated in the "stand-alone" mode and enabled by the R/$\overline{C}$ input pin. Full µP control consists of selecting an 8 or 12-bit conversion cycle initiating the conversion and reading the output data when ready. The output read has the options of choosing either 12-bits at once or 8 bits followed by 4 bits in a left-justified format. All five control inputs are TTL/CMOS compatible and include 12/$\overline{8}$, $\overline{CS}$, Ao, R/$\overline{C}$ and CE. The use of these inputs in controlling the converter's operations is shown in table I, and the internal control logic is shown in a simplified schematic in figure 14.

STAND-ALONE OPERATION

The simplest interface is a control line connected to R/$\overline{C}$. The output controls must be tied to known states as follows: CE and 12/$\overline{8}$ are wired high, Ao and $\overline{CS}$ are wired low. The output data arrives in words of 12-bits each. The limits on R/$\overline{C}$ duty cycle are shown in figures 3 and 4. It may have a duty cycle within and including the extremes shown in the specifications. In general, data may be read when R/$\overline{C}$ is high unless STS is also high, indicating a conversion is in progress.

Figure 13 - Interfacing the SPT774 to an 8-bit Data Bus

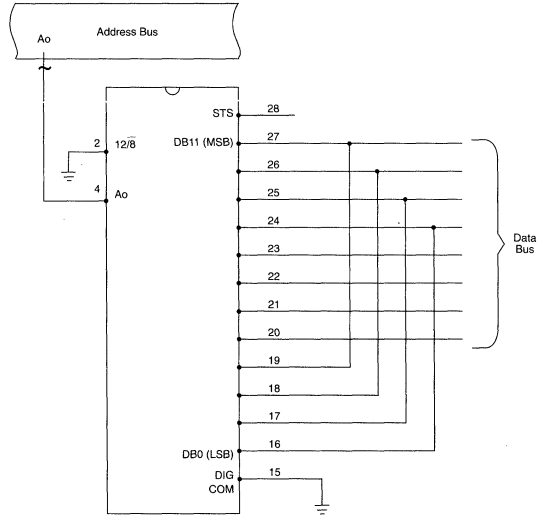


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Table I - Truth Table for the SPT774 Control Inputs

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	Ao	Operation
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12 bit conversion
↑	0	0	X	1	Initiate 8 bit conversion
1	↓	0	X	0	Initiate 12 bit conversion
1	↓	0	X	1	Initiate 8 bit conversion
1	0	↓	X	0	Initiate 12 bit conversion
1	0	↓	X	1	Initiate 8 bit conversion
1	0	1	1	X	Enable 12 bit Output
1	0	1	0	0	Enable 8 MSB's Only
1	0	1	0	1	Enable 4 LSB's Plus 4 Trailing Zeroes

CONVERSION LENGTH

A conversion start transition latches the state of Ao as shown in figure 13 and table I. The latched state determines if the conversion stops with 8-bit (Ao high) or continues for 12-bits (Ao low). If all 12-bits are read following an 8-bit conversion, the three LSB's will be a logic 0 and DB3 will be a logic 1. Ao is latched because it is also involved in enabling the output buffers as will be explained later. No other control inputs are latched.

CONVERSION START

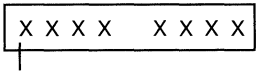
A conversion may be initiated by a logic transition on any of the three inputs: CE, $\overline{CS}$, R/$\overline{C}$, as shown in table I. The last of the three to reach the correct state starts the conversions, so one, two or all three may be dynamically controlled. The nominal delay from each is the same and all three may change state simultaneously. In order to assure that a particular input controls the start of conversion, the other two should be set up at least 50 ns earlier. Refer to the convert mode timing specifications. The Convert Start timing diagram is illustrated in figure 1.

The output signal STS is the status flag and goes high only when a conversion is in progress. While STS is high, the output buffers remain in a high impedance state so that data can not be read. Also, when STS is high, an additional Start Convert will not reset the converter or reinitiate a conversion. Note, if Ao changes state after a conversion begins, an additional Start Convert command will latch the new start of Ao and possibly cause a wrong cycle length for that conversion (8 versus 12-bits).

READING THE OUTPUT DATA

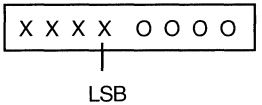
The output data buffers remain in a high impedance state until the following four conditions are met: R/$\overline{C}$ is high, STS is low, CE is high, and $\overline{CS}$ is low. The data lines become active in response to the four conditions and output data according to the conditions of 12/$\overline{8}$ and Ao. The timing diagram for this process is shown in figure 2. When 12/$\overline{8}$ is high, all 12 data outputs become active simultaneously and the Ao input is ignored. This results in easy interface to a 12 or 16-bit data bus. The 12/$\overline{8}$ input is usually tied high or low, although it is TTL/CMOS compatible. When 12/$\overline{8}$ is low, the output is separated into two 8-bit bytes as shown below:

BYTE 1



MSB

BYTE 2



LSB

This configuration makes it easy to connect to an 8-bit data bus as shown in figure 13. The Ao control can be connected to the least significant bit of the address bus in order to store the output data into two consecutive memory locations. When Ao is pulled low, the 8 MSBs are enabled only. When Ao is high, the 4 MSBs are disabled, bits 4 through 7 are forced to a zero and the four LSBs are enabled. The two byte format is "left justified data" as shown above and can be considered to have a decimal point or binary to the left of byte 1.

Ao may be toggled without damage to the converter at any time. Break-before-make action is guaranteed between the two data bytes. This assures that the outputs which are strapped together in figure 13 will never be enabled at the same time.

In figure 2, it can be seen that a read operation usually begins after the conversion is completed and STS is low. If earlier access is needed, the read can begin no later than the addition of time t_{DD} and t_{HS} before STS goes low.

Figure 14 - Control Logic

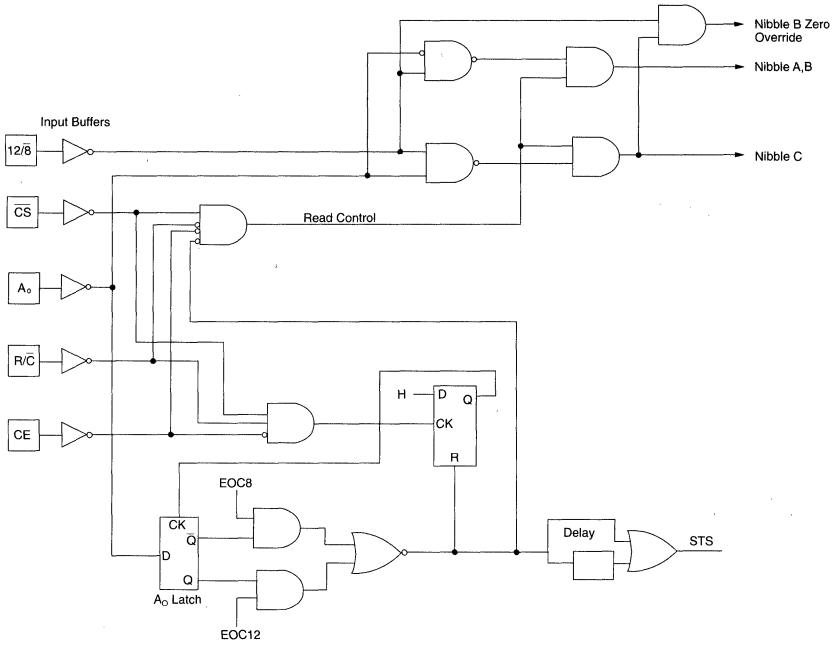
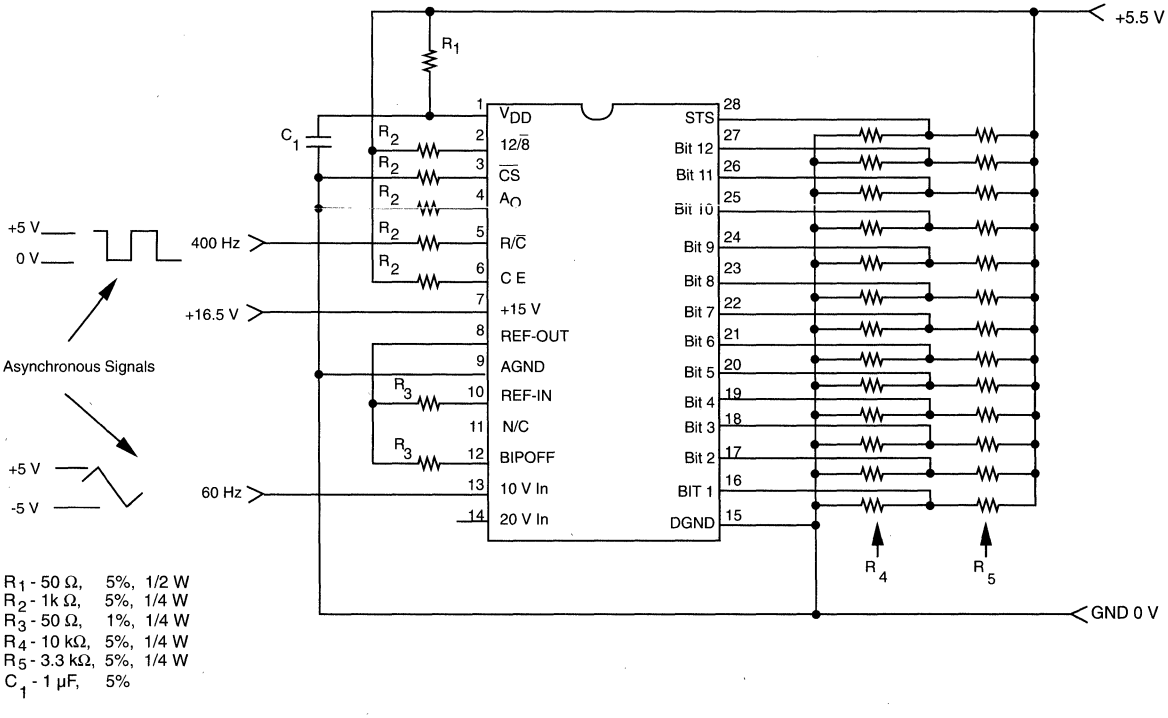


Figure 15 - Burn-In Schematic



R_1 - 50 Ω, 5%, 1/2 W
R_2 - 1k Ω, 5%, 1/4 W
R_3 - 50 Ω, 1%, 1/4 W
R_4 - 10 kΩ, 5%, 1/4 W
R_5 - 3.3 kΩ, 5%, 1/4 W
C_1 - 1 µF, 5%

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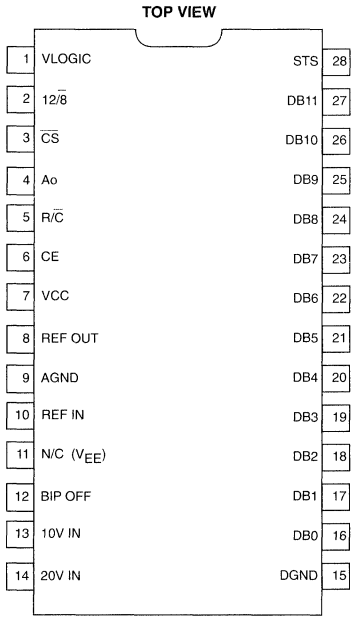
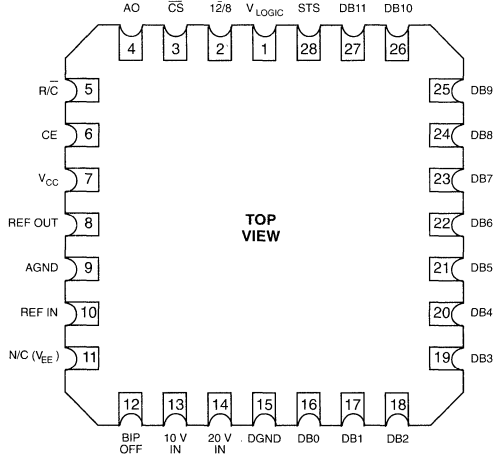
PIN ASSIGNMENT SPT774



28-LEAD DIP



28-LEAD LCC

PIN FUNCTIONS SPT774

NAME	FUNCTION
V_{LOGIC}	Logic Supply Voltage, Nominally +5 V
12/$\overline{8}$	Data Mode Selection
$\overline{CS}$	Chip Selection
Ao	Byte Address/Short Cycle
R/$\overline{C}$	Read/Convert
CE	Chip Enable
V_{CC}	Analog Positive Supply Voltage, Nominally +15 V
REF OUT	Reference Output, Nominally +10 V
AGND*	Analog Ground
REF IN	Reference Input
N/C (V_{EE})	This pin is not connected to the device.
BIP OFF	Bipolar Offset
10 V IN	10 Volt Analog Input
20 V IN	20 Volt Analog Input
DGND	Digital Ground
DB0 - DB11	Digital Data Output DB11 - MSB DB0 - LSB
STS	Status

* The lids on the sidebrazed and LCC packages are internally connected to AGND.

LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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SIGNAL PROCESSING TECHNOLOGIES

SPT7610

6-BIT, 1 GSPS FLASH A/D CONVERTER

ADVANCED INFORMATION

3

FEATURES

- 1:2 Demuxed ECL Compatible Outputs
- 1.0 GSPS Conversion Rate
- Wide Input Bandwidth - 1.4 GHz
- Low Input Capacitance - 8 pF
- Metastable Errors Reduced to 1 LSB
- Monolithic Construction

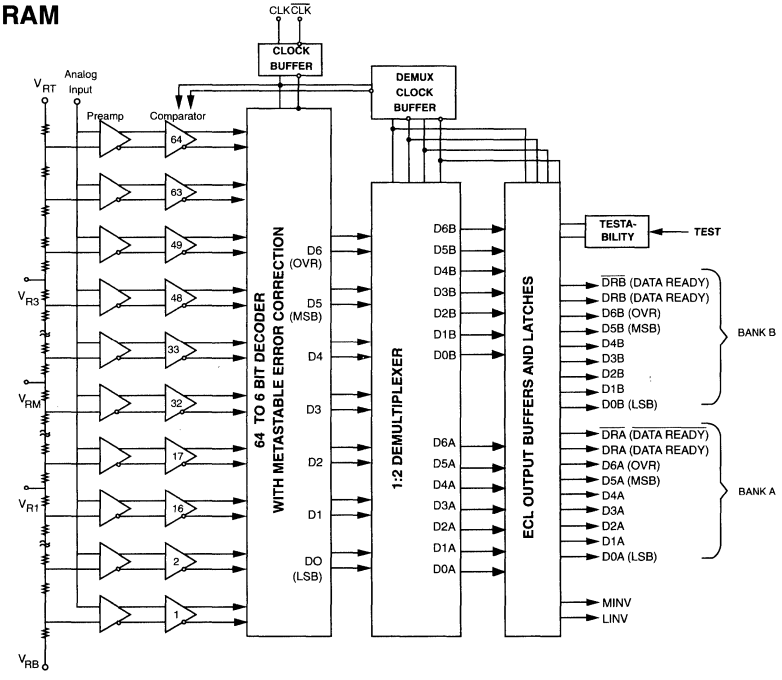
APPLICATIONS

- Digital Oscilloscopes
- Transient Capture
- Radar, EW, ECM
- Direct RF Down-Conversion

GENERAL DESCRIPTION

The SPT7610 is a full parallel (flash) analog-to-digital converter capable of digitizing full scale (0 to -1 V) inputs into six-bit digital words at an update rate of 1 GSPS. The ECL-compatible outputs are demultiplexed into two separate output banks, each with differential data ready outputs to ease the task of data capture. The SPT7610's wide input bandwidth and low capacitance eliminate the need for external track-and-hold amplifiers for most applications. A proprietary decoding scheme reduces metastable errors to the 1 LSB level. The SPT7610 operates from a single -5.2 V supply, with a nominal power dissipation of 3.0 W. The SPT7610 is available in a 44L cerquad surface-mount package in the industrial temperature range. Contact the factory for military and /883 availability.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages
Negative Supply Voltage (V_{EE} TO GND) ..... -7.0 to +0.5 V
Ground Voltage Differential ..... -0.5 to +0.5 V

Input Voltage
Analog Input Voltage ..... +0.5 V to V_{EE}
Reference Input Voltage ..... +0.5 V to V_{EE}
Digital Input Voltage ..... +0.5 V to V_{EE}
Reference Current V_{RT} to V_{RB} ..... +20 mA

Output
Digital Output Current ..... 0 to -25 mA

Temperature
Operating Temperature, ambient ..... -25 to +85 °C
Lead Temperature, (soldering 10 seconds) ..... +300 °C
Storage Temperature ..... -65 to +150 °C

Notes: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

TARGET ELECTRICAL SPECIFICATIONS

$T_A = T_{MIN}$ to T_{MAX}, V_{EE}=-5.2 V ±5%, V_{RB}=-1.00 V, V_{RM}=-0.5 V, V_{RT}=0.00 V, f_{clk}=100 kHz, Duty Cycle=50%, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7610 MIN	SPT7610 TYP	SPT7610 MAX	UNITS
DC ELECTRICAL CHARACTERISTICS						
Integral Linearity		I	-0.5		+0.5	LSB
Differential Linearity		I	-0.5		+0.5	LSB
No missing codes guaranteed		I	6			Bit
Offset Error V_{RT}		I	-30		+30	mV
Offset Error V_{RB}		I	-30		+30	mV
Input Voltage Range		I	-1		0.0	Volts
Input Capacitance	Over Full Input Range	IV		8		pF
Input Resistance		IV		60		kΩ
Input Current		I		300		µA
Clock Synchronous Input Currents		V		2		µA
Supply Current[1]	At +25 °C, V_{EE} = -5.2 V	I		465	700	mA
Power Dissipation[1]	At +25 °C, V_{EE} = -5.2 V	I		2.75	3.65	W
Ladder Resistance		I		80		Ω
Reference Bandwidth		V		100		MHz
Digital Output High Voltage	R_1 = 50 Ω to -2V	I	-1.2	-0.9		Volts
Digital Output Low Voltage	R_1 = 50 Ω to -2V	I		-1.8	-1.5	Volts
Digital Input High Voltage (CLK, NCLK)		I	-1.1		-0.7	Volts
Input Low Voltage (CLK, NCLK)		I	-2.0		-1.5	Volts
Input Swing (CLK, NCLK)		IV	100	700		mV

1 Supply current and power dissipation will be tested over full temperature range, but maximum specifications may change at temperature extremes.

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TARGET ELECTRICAL SPECIFICATIONS

T_A = +25 °C ambient, V_{EE}=-5.2 V ±5%, V_{RB}=-1.00 V, V_{RM}=-0.5 V, V_{RT}=0.00 V, f_{clk}=1000 MSPS, Duty Cycle=50%, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7610 MIN	SPT7610 TYP	SPT7610 MAX	UNITS
AC ELECTRICAL CHARACTERISTICS						
Maximum Sample Rate		I	1000	1200		MSPS
Clock Low Width, TPW0		I	0.5	0.4		ns
Clock High Width, TPW1		I	0.5	0.4		ns
DATA to DATA READY Delay		IV		TBD		ns
Clock to Data Delay		IV		TBD		ns
Data Skew	Between Output Data	IV		250		ps
Small Signal Bandwidth		V		1.4		GHz
Aperture Jitter		V		2		ps
Acquisition Time		V		250		ps
Input Slew Rate		V		5		V/ns
Total Dynamic Error[1]	F_{IN}=250 MHz at +25 °C F_{IN}=400 MHz at +25 °C	I I	31 27	34 32		dB dB
Signal to Noise Ratio[1]	F_{IN}=250 MHz at +25 °C F_{IN}=400 MHz at +25 °C	I I	TBD TBD	36 33		dB dB
Total Harmonic Distortion[1]	F_{IN}=250 MHz at +25 °C F_{IN}=400 MHz at +25 °C	I I	TBD TBD	36 33		dBc dBc

1 These parameters will be tested over full temperature range, but performance minimums are TBD at temperature extremes. However, total dynamic error in test conditions f_{IN} = 250 MHz, f_{CLK} = 650 MHz over full temperature is guaranteed at 30 dB minimum.

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests; therefore, $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

SUBCIRCUIT SCHEMATICS

Figure 1A - Input Circuit

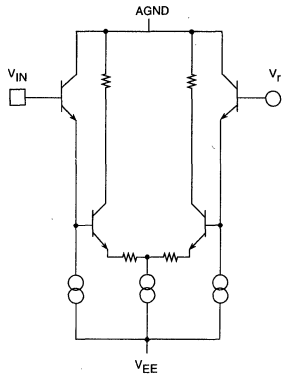

Figure 1B - Output Circuit

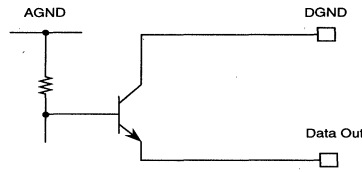

Figure 1C - Clock Input

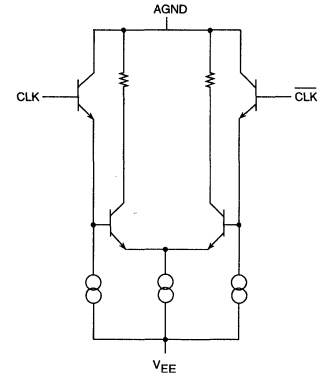

Table 1 - Truth Table

STEP	IDEAL INPUT[1] VOLTAGE (V)	D6A(OVR) D6B(OVR)	BINARY		TWOs COMPLEMENT	
			TRUE	INVERTED	TRUE	INVERTED
			$MSB_{INV}(V_{EE})$[2] $LSB_{INV}(V_{EE})$[2]	$MSB_{INV}(GND)$ $LSB_{INV}(GND)$	$MSB_{INV}(GND)$ $LSB_{INV}(V_{EE})$[2]	$MSB_{INV}(V_{EE})$[2] $LSB_{INV}(GND)$
00	-1.000	0	000 000	111 111	100 000	011 111
01	-0.984	0	000 001	111 110	100 001	011 110
---	---	0	---	---	---	---
---	---	0	---	---	---	---
---	---	0	---	---	---	---
31	-0.516	0	011 111	100 000	111 111	000 000
32	-0.500	0	100 000	011 111	000 000	111 111
33	-0.484	0	100 001	011 110	000 001	111 110
---	---	0	---	---	---	---
---	---	0	---	---	---	---
---	---	0	---	---	---	---
62	-0.031	0	111 110	000 001	011 110	100 001
63	-0.016	0	111 111	000 000	011 111	100 000
>63	-0.000	1	111 111	000 000	011 111	100 000

1 Ideal input voltage does not include gain, offset and linearity voltage errors.
2 V_{EE} or floating.

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Figure 5 - A/D Converter Testability

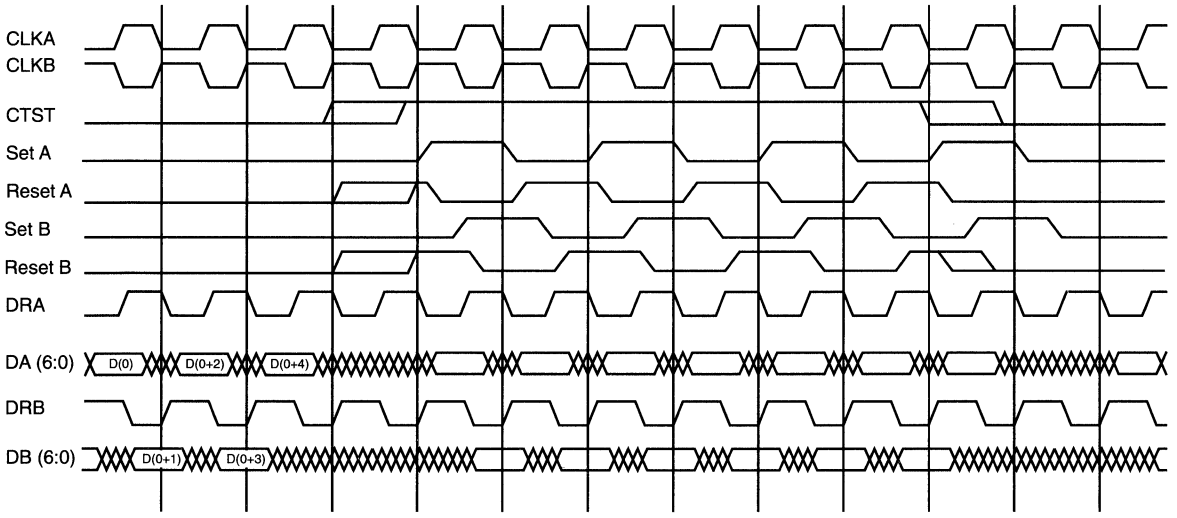

Figure 6 - Timing Diagram

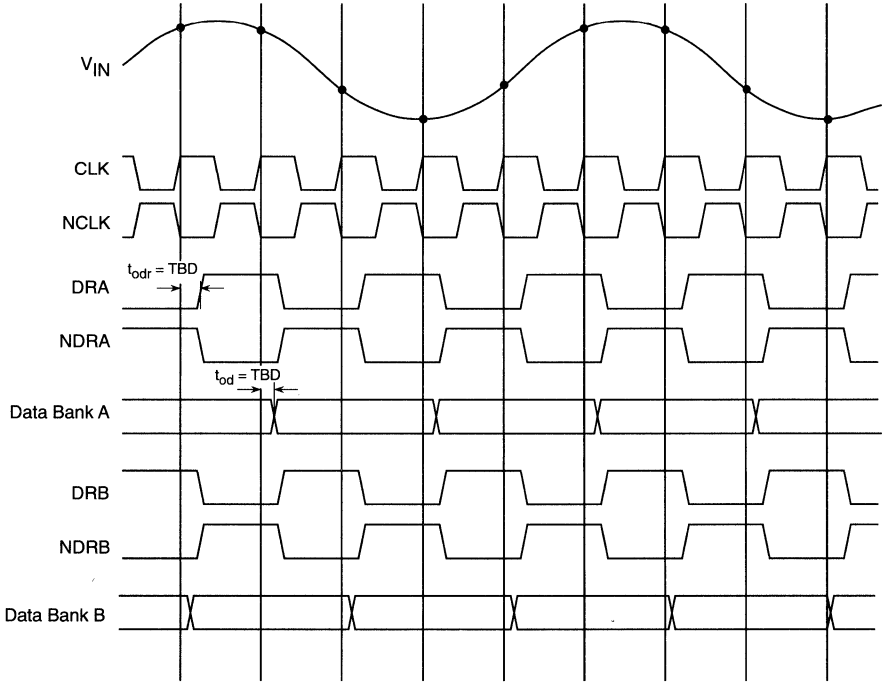

Table 2 - Testability Truth Table

	D6A	D5A	D4A	D3A	D2A	D1A	DØA
nth DRA	1	0	1	0	1	0	1
(n+1)th DRA	0	1	0	1	0	1	0

	D6B	D5B	D4B	D3B	D2B	D1B	DØB
nth DRB	1	0	1	0	1	0	1
(n+1)th DRB	0	1	0	1	0	1	0

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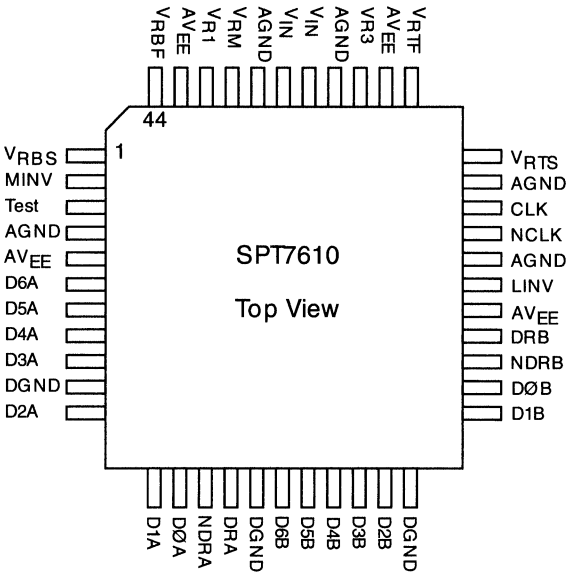
PIN ASSIGNMENT SPT7610



PIN FUNCTIONS

NAME	FUNCTION
V_{EE}	Negative Supply Nominally -5.2 V
AGND	Analog Ground
V_{RTF}	Reference Voltage Force Top, Nominally 0 V
V_{RTS}	Reference Voltage Sense Top
V_{RM}	Reference Voltage Middle, Nominally -0.5 V
V_{RBF}	Reference Voltage Force Bottom, Nominally -1.0 V
V_{RBS}	Reference Voltage Sense Bottom
V_{IN}	Analog Input Voltage, Can Be Either Voltage or Sense
DGND	Digital Ground
D0~D5A	Data Output Bank A
D0~D5B	Data Output Bank B
DRA	Data Ready Bank A
NDRA	Not Data Ready Bank A
DRB	Data Ready Bank B
NDRB	Not Data Ready Bank B
D6A	Overrange Output Bank A
D6B	Overrange Output Bank B
CLK	Clock Input
NCLK	$\overline{\text{Clock}}$ Input
MINV	MSB Control Pin
LINV	LSB Control Pin
TEST	Test Control Pin
V_{R1}	Reference Voltage 1/4 Nominally -0.75 V
V_{R3}	Reference Voltage 3/4, Nominally -0.25 V

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SIGNAL PROCESSING TECHNOLOGIES

SPT1175

8-BIT, 20 AND 30 MSPS CMOS A/D CONVERTER

FEATURES

- 30 MSPS Maximum Conversion Rate
- Internal Sample-and-Hold Function
- 90 mW Power Dissipation at 20 MSPS
- Internal Voltage Reference
- Single +5.0 V Power Supply
- Three-State TTL-Outputs
- CMOS Compatible Clock

APPLICATIONS

- Video Digitizing
- Image Scanners
- Personal Computer Video
- Medical Ultrasound
- Multimedia
- Digital Television

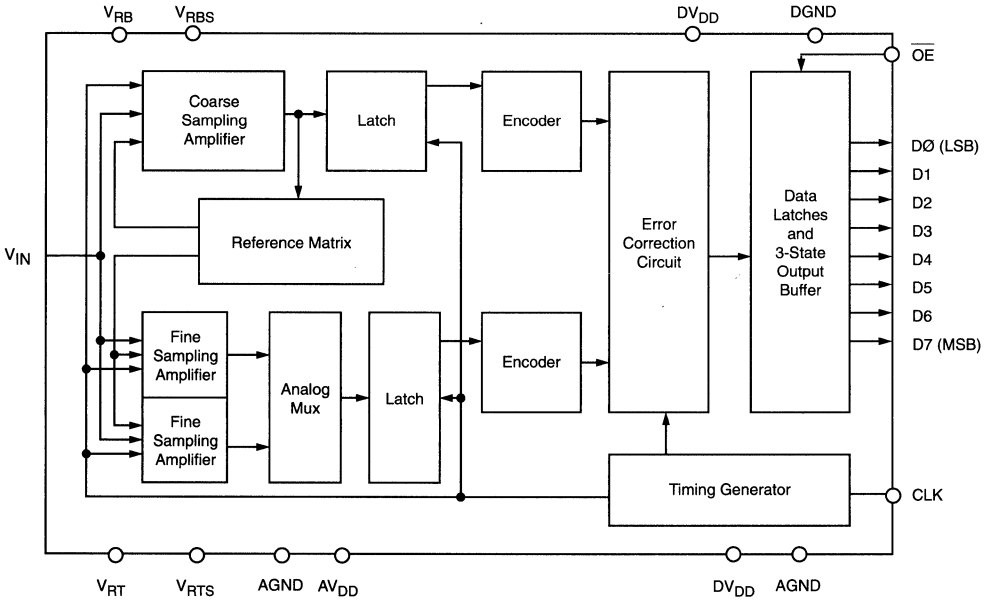
GENERAL DESCRIPTION

The SPT1175 is a CMOS two-step A/D converter capable of digitizing full scale analog input signals into 8-bit digital words at sample rates of 20 and 30 MSPS.

For most applications, no external sample-and-hold or video driving amplifiers are required due to the device's narrow aperture time, wide bandwidth, and low input capacitance.

The SPT1175 operates from a single +5.0 V power supply and has an internal voltage reference which eliminates the need for external reference circuitry. All digital inputs are CMOS compatible and the tri-state outputs are TTL-compatible. The SPT1175 is ideal for most video and image processing applications that require low power dissipation and low cost. The SPT1175 is available in 24-lead plastic SOIC, plastic DIP, ceramic DIP, PLCC and die form.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages
V_{DD} ..... -0.5 to +7.0 V

Input Voltages
Analog Input ..... AGND to V_{DD}
Reference Input Voltage ..... AGND to V_{DD}
ESD Susceptibility[2] ..... ±1,500 V

Temperature
Operating Temperature ..... -20 to +70 °C
Junction Temperature ..... 175 °C
Lead Temperature, (soldering 10 seconds) ..... 300 °C
Storage Temperature ..... -55 to +125 °C

Notes: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.
2. 100 pF discharged through a 1.5 kΩ resistor (human body model).

ELECTRICAL SPECIFICATIONS

T_A= +25 °C, AV_{DD}=DV_{DD}=+5.0 V, AGND=DGND=0.0 V, V_{RB}=+0.6 V and V_{RT}=+2.6 V, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
Resolution			8			Bits
DC Accuracy (+25 °C)						
Integral Nonlinearity		I		±0.8	±1.2	LSB
Differential Nonlinearity		I		±0.6	±1.0	LSB
No Missing Codes		I		Guaranteed		
Analog Input						
Input Voltage Range		I	V_{RB}		V_{RT}	V
Input Bias Current		I			±5.0	µA
Input Resistance		VI	100	200		kΩ
Input Capacitance		V		15		pF
Input Bandwidth		V	12			MHz
Reference Input						
Reference Ladder Resistance		I	200	300	400	Ω
Reference Current		I	5.0	6.7	10.0	mA
Reference Input Voltage	V_{RB}	IV	0	0.6	-	V
	V_{RT}	IV	-	2.6	2.8	V
Internal Bias	V_{RB}	I	0.55	0.60	0.65	V
	V_{RT}-V_{RB}	I	1.9	2.0	2.1	V
	Short V_{RT} and V_{RTS}					
	Short V_{RB} and V_{RBS}					
Offset Voltage Error						
Top		I	-18	-25	-68	mV
Bottom		I	0	10	40	mV
Timing Characteristics						
Maximum Conversion Rate	1 MHz Input Sine Wave	I	30	40		MSPS
Output Data Delay (td)		IV		18	30	ns
Output Data Delay (Tdish, Tdisl)	(High 'Z')	IV			100	ns
Data Valid Time (Teneh, Tenel)	Tri-state circuit	IV			100	ns
Sampling Time Offset		IV		5	10	ns

NOTE: It is strongly recommended that all of the supply pins (AV_{DD}, DV_{DD}) be powered from the same source.

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ELECTRICAL SPECIFICATIONS

T_A=+25 °C, AV_{DD}=DV_{DD}=+5.0 V, AGND=DGND=0.0 V, V_{RB}=+0.6 V and V_{RT}=+2.6 V, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
Dynamic Performance						
Signal-To-Noise Ratio	fs= 20 MSPS					
$f$in=1.0 MHz		I	44	46		dB
$f$in=3.58 MHz		I	43	45		dB
$f$in=10 MHz		I		44		dB
Spurious Free						
Dynamic Range	fs= 20 MSPS					
$f$in=1.0 MHz		I	44	47		dB
$f$in=3.58 MHz		I	41	44		dB
$f$in=10 MHz		I	30	33		dB
Signal-To-Noise Ratio	fs= 30 MSPS					
$f$in=1.0 MHz		I	42	44		dB
$f$in=3.58 MHz		I	41	43		dB
$f$in=10 MHz		I	40	42		dB
Spurious Free						
Dynamic Range	fs= 30 MSPS					
$f$in=1.0 MHz		I	42	45		dB
$f$in=3.58 MHz		I	35	38		dB
$f$in=10 MHz		I	30	33		dB
Differential Phase	NTSC 20 IRE Mod Ramp	I		0.7		Degrees
Differential Gain	fs= 14.3 MSPS	I		1.0		%
Digital Inputs						
Input Current, Logic High	V_{DD} = 5.25 V, V_{IH} = V_{DD}	I			1.0	µA
Input Current, Logic Low	V_{DD} = 5.25 V, V_{IL} = DGND	I			1.0	µA
Pulse Width High (CLK)		IV	15			ns
Pulse Width Low (CLK)		IV	15			ns
Voltage, Logic High		I	4.0			V
Voltage, Logic Low		I			1.0	V
Digital Outputs						
Output Current, High	V_{DD} = 4.75 V	I	-1.1			mA
Output Current, Low	V_{DD} = 4.75 V	I	3.5			mA
Output Current, High 'Z'	V_{DD} = 5.25 V, $\overline{OE}$= V_{DD}	I			16	µA
Voltage High		I	4.0			V
Voltage Low		I			0.4	V
Power Supply Requirements						
AV_{DD} (Analog Supply Voltage)		IV	+4.75	+5.0	+5.25	V
DV_{DD} (Digital Supply Voltage)		IV	+4.75	+5.0	+5.25	V
Supply Voltage Difference	(AV_{DD} -DV_{DD})	IV	-0.1	0.0	0.1	V
Supply Current	fs=20 MSPS	I		18	27	mA
Power Dissipation		I		90	135	mW

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests; therefore, T_J = T_C = T_A.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

Table 1 - Output Coding

INDEX	ANALOG INPUT (V)	DIGITAL OUTPUT	
0	0.6078125	00000000	
1	0.6078125 ~ 0.6156260	00000001	V_{RB}=0.6 V
2	0.6156250 ~ 0.6234375	00000010	V_{RT}=2.6 V
....	....	....	
123	1.5921875 ~ 1.6000000	01111111	1 LSB=7.8125 mV
124	1.6000000 ~ 1.6078125	10000000	
125	1.6078125 ~ 1.6156250	10000001	
....	....	....	
254	2.5843750 ~2.5921875	11111110	
255	2.5921875 ~	11111111	

Figure 1A: Timing Diagram

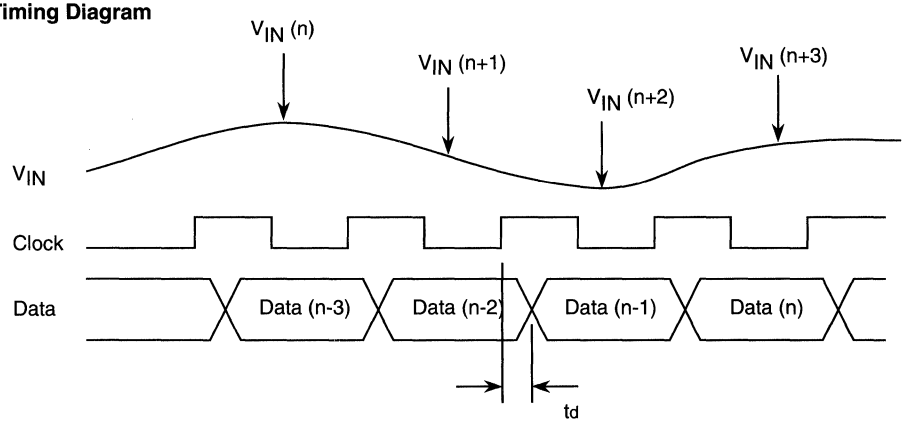
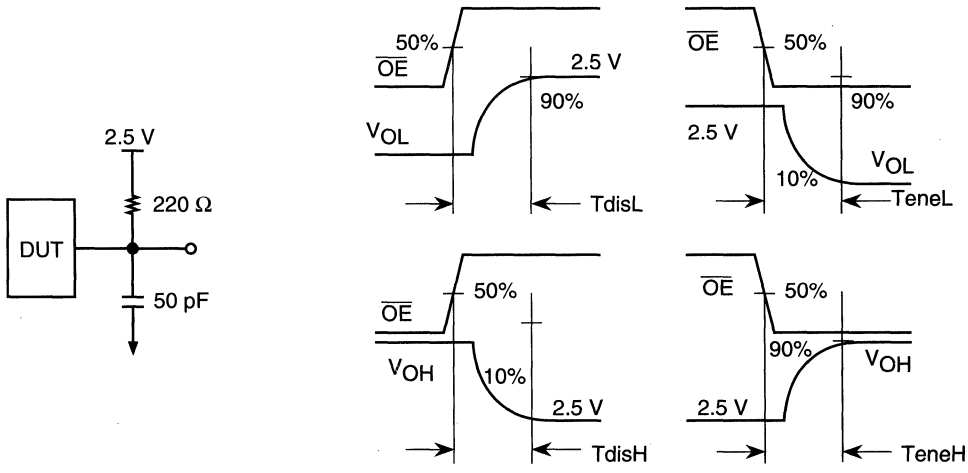


Figure 1B: Tri-State Output Timing Diagram



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TYPICAL INTERFACE CIRCUIT

The SPT1175 is an 8-bit analog-to-digital converter which uses a two-step, ping-pong architecture to perform conversions up to 30 MSPS. Figure 2 shows the typical interface requirements when using the SPT1175 in normal operation. The following sections describe the function and operation of the device.

POWER SUPPLIES AND GROUNDING

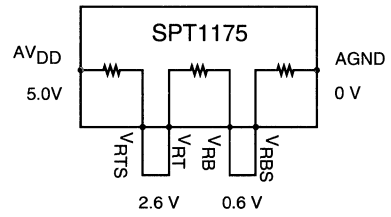
The SPT1175 operates from a single +5 V power supply. AV_{DD} and DV_{DD} must be supplied from the same source (analog +5 V) to prevent a latch-up condition due to power supply sequencing. Each power supply pin should be bypassed as closely as possible to the device. For optimal performance, both the AGND and DGND should be connected to the system's analog ground plane.

ANALOG INPUT AND VOLTAGE REFERENCE

The SPT1175 input voltage range is $V_{RT}>V_{IN}>V_{RB}$. Two reference voltages (V_{RT} and V_{RB}) are required for device operation. These voltages may be generated externally or the SPT1175's internal reference may be used.

Inside the SPT1175, reference resistors are placed between AV_{DD} and V_{RTS} and between AGND and V_{RBS} so that V_{RTS} and V_{RBS} generate the 2.6 V and 0.6 V references respectively. (See figure 3.) In order to utilize the internal self-bias reference voltage, V_{RTS} is to be shorted with V_{RT} and the V_{RBS} pin is to be shorted to the V_{RB} pin. The self-bias internal reference is not as stable over temperature and supply variations as externally generated reference voltages but will perform well in many commercial video applications.

Figure 3 - Reference Circuit Diagram



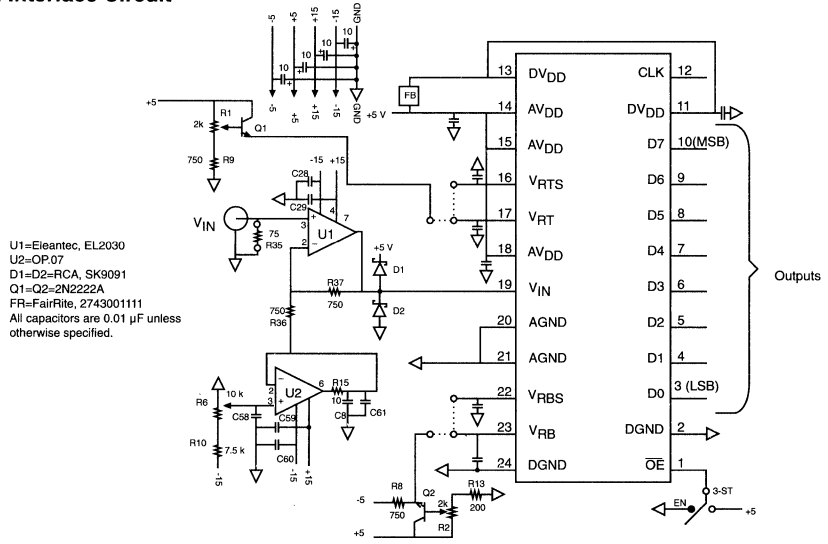
DIGITAL INPUTS AND OUTPUTS

The analog input is sampled and tracked on the first 'H' cycle of the external clock and is held from the falling edge of CLK. The output remains valid (output hold time), and the new data becomes valid (output delay time) after the rising edge of CLK, delayed by 2.5 clock cycles. The clock input and output enable input must be driven at CMOS-compatible levels.

EVALUATION BOARD

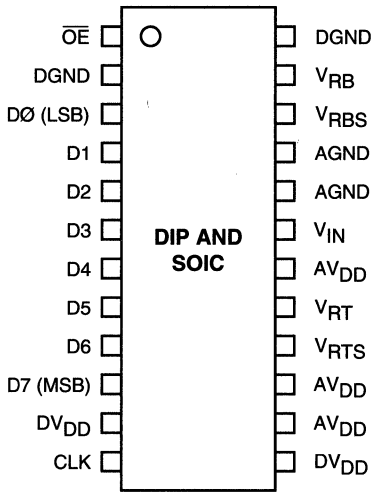
The EB1175 evaluation board is available to aid designers in demonstrating the full performance of the SPT1175. This board includes a reference circuit, clock driver circuit, output data latches, and an on-board reconstruction DAC. An application note describing the operation of the board is available. Contact the factory for price and delivery.

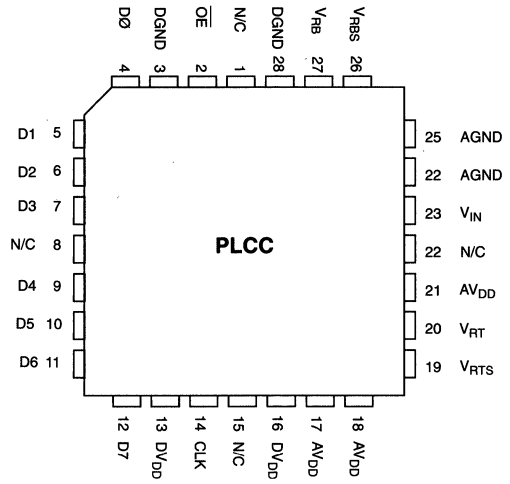
Figure 2 - Typical Interface Circuit



NOTE: AV_{DD} and DV_{DD} must be supplied from the same source (Analog +5 V) to prevent a latch-up condition due to power supply sequencing.

PIN ASSIGNMENTS





PIN FUNCTIONS

$\overline{OE}$	Tri-State Output Enable Tri-State When $\overline{OE}$ = DV_{DD}, Enable When $\overline{OE}$ = DGND
DGND	Digital Ground
D0	Digital Output Data (LSB)
D1-6	Digital Output Data
D7	Digital Output Data (MSB)
DV_{DD}	Digital Supply
CLK	CMOS Digital Clock Input

AV_{DD}	Analog Supply
V_{RTS}	Internal Self-Biased Reference Top Shorted with V_{RT} pin (17). Generates 2.6 V.
V_{RT}	Reference Resistor Top Side
V_{IN}	Analog Input
AGND	Analog Ground
V_{RBS}	Internal Self-Biased Reference Bottom Shorted with V_{RB} pin (23). Generates 0.6 V.
V_{RB}	Reference Resistor Bottom Side

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SIGNAL PROCESSING TECHNOLOGIES

SPT7710

8-BIT, 150 MSPS FLASH A/D CONVERTER

FEATURES

- Metastable Errors Reduced to 1 LSB
- Low Input Capacitance: 10 pF
- Wide Input Bandwidth: 210 MHz
- 150 MSPS Conversion Rate
- Typical Power Dissipation: 2.2 Watts

APPLICATIONS

- Digital Oscilloscopes
- Transient Capture
- Radar, EW, ECM
- Direct RF Down-Conversion
- Medical Electronics: Ultrasound, CAT Instrumentation

3

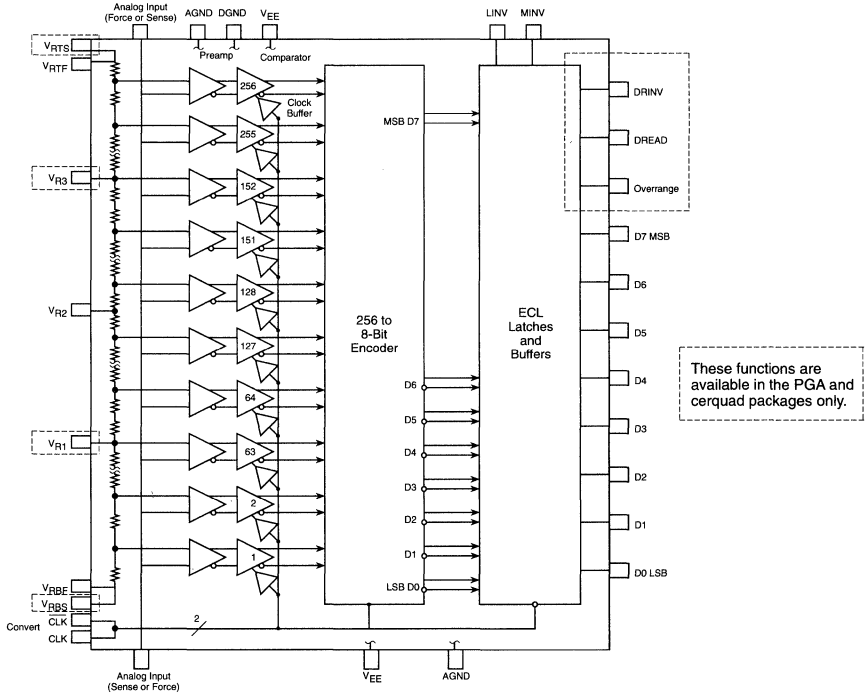
GENERAL DESCRIPTION

The SPT7710 is a monolithic flash A/D converter capable of digitizing a two volt analog input signal into 8-bit digital words at a 150 MSPS (typ) update rate.

For most applications, no external sample-and-hold is required for accurate conversion due to the device's narrow aperture time, wide bandwidth, and low input capacitance. A single standard -5.2 volt power supply is required for operation of the SPT7710, with nominal power dissipation of 2.2 W. A proprietary decoding scheme reduces metastable errors to the 1 LSB level.

The part is packaged in a 42L ceramic sidebrazed DIP which is pin compatible with the CX20116 and CXA1396D. A surface-mount 44L cerquad and a 46L PGA package are also available which allow access to additional reference ladder taps, an overrange bit, and a data ready output. The SPT7710 is available in industrial and military temperature ranges and in /883 compliant versions.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages
- Negative Supply Voltage (V_{EE} TO GND) ..... -7.0 to +0.5 V
- Ground Voltage Differential ..... -0.5 to +0.5 V

Input Voltage
- Analog Input Voltage ..... V_{EE} to +0.5 V
- Reference Input Voltage ..... V_{EE} to +0.5 V
- Digital Input Voltage ..... V_{EE} to +0.5 V
- Reference Current V_{RTF} to V_{RBF} ..... 25 mA

Output
- Digital Output Current ..... 0 to -30 mA

Temperature
- Operating Temperature ..... -25°C ambient to +85 °C ambient
- junction ..... +150 °C
- Lead Temperature, (soldering 10 seconds). ..... +300 °C
- Storage Temperature ..... -65 to +150 °C

Notes: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

T_A= T_{MIN} to T_{MAX}, V_{EE}=-5.2 V, R_{Source}=50 Ω, V_{RBF}=-2.00 V, V_{R2}=-1.00 V, V_{RTF}=0.00 V, f_{clk}=150 MHz, Duty Cycle=50%, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7710A MIN	SPT7710A TYP	SPT7710A MAX	SPT7710B MIN	SPT7710B TYP	SPT7710B MAX	UNITS
DC Accuracy									
Integral Linearity	f_{CLK} = 100 kHz	VI	-0.75	±0.60	+0.75	-0.95	±0.80	+0.95	LSB
Differential Linearity	f_{CLK} = 100 kHz	VI	-0.75		+0.75	-0.95		+0.95	LSB
No missing codes			Guaranteed			Guaranteed			
Analog Input									
Offset Error V_{RT}		IV	-30		+30	-30		+30	mV
Offset Error V_{RB}		IV	-30		+30	-30		+30	mV
Input Voltage Range		VI	-2.0		0.0	-2.0		0.0	Volts
Input Capacitance	Over full input range	V		10			10		pF
Input Resistance		V		15			15		kΩ
Input Current		VI		250	500		250	500	µA
Input Slew Rate		V		1,000			1,000		V/µs
Large Signal Bandwidth	V_{IN}=F.S.	V		210			210		MHz
Small Signal Bandwidth	V_{IN}=500 mV P-P	V		335			335		MHz
Reference Input									
Ladder Resistance		VI	100	200	300	100	200	300	Ω
Reference Bandwidth		V		10			10		MHz
Timing Characteristics									
Maximum Sample Rate		VI	125	150		125	150		MSPS
Clock to Data Delay		V		2.4			2.4		ns
Output Delay TEMPCO		V		2			2		ps/°C
CLK-to-Data Ready Delay (t_d)		V		2.0			2.0		ns
Aperture Jitter		V		5			5		ps
Acquisition Time		V		1.5			1.5		ns
Dynamic Performance									
Signal-to-Noise Ratio	F_{IN} = 3.58 MHz	VI	46	48		45	47		dB
	F_{IN} = 50 MHz	VI	42	46		40	44		dB
Total Harmonic Distortion	F_{IN} = 3.58 MHz	VI	-48	-52		-46	-50		dB
	F_{IN} = 50 MHz	VI	-40	-44		-39	-43		dB
Signal-to-Noise and Distortion	F_{IN} = 3.58 MHz	VI	45	48		43	46		dB
(SINAD)	F_{IN} = 50 MHz	VI	39	42		37	40		dB

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ELECTRICAL SPECIFICATIONS

$T_A = T_{MIN}$ to T_{MAX}, V_{EE}=-5.2 V, R_{Source}=50 Ω, V_{RBF}=-2.00 V, V_{R2}=-1.00 V, V_{RTF}=0.00 V, f_{clk}=150 MHz, Duty Cycle=50%, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7710A MIN	SPT7710A TYP	SPT7710A MAX	SPT7710B MIN	SPT7710B TYP	SPT7710B MAX	UNITS
Digital Inputs									
Digital Input High Voltage (MINV, LINV)		VI	-1.1		-0.7	-1.1		-0.7	Volts
Digital Input Low Voltage (MINV, LINV)		VI	-2.0		-1.5	-2.0		-1.5	Volts
Clock Synchronous Input Currents		V		40			40		µA
Clock Low Width, T_{PWL}		VI	4	3		4	3		ns
Clock High Width, T_{PWH}		VI	4	3		4	3		ns
Digital Outputs									
Digital Output High Voltage	50 Ω to -2 V	VI	-1.1			-1.1			Volts
Digital Output Low Voltage	50 Ω to -2 V	VI			-1.5			-1.5	Volts
Power Supply Requirements									
Supply Current	+25 °C	I		425	550		425	550	mA
Power Dissipation	+25 °C	I		2.2	2.9		2.2	2.9	W

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

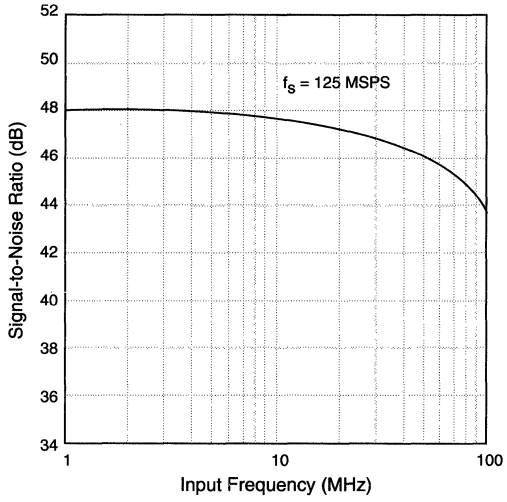
All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests; therefore, $T_J = T_C = T_A$.

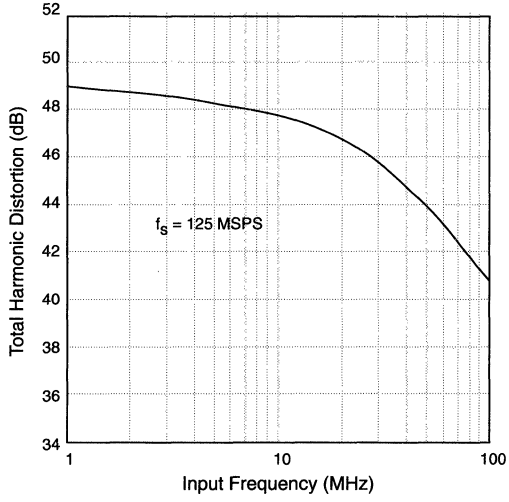
TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

TYPICAL PERFORMANCE CHARACTERISTICS

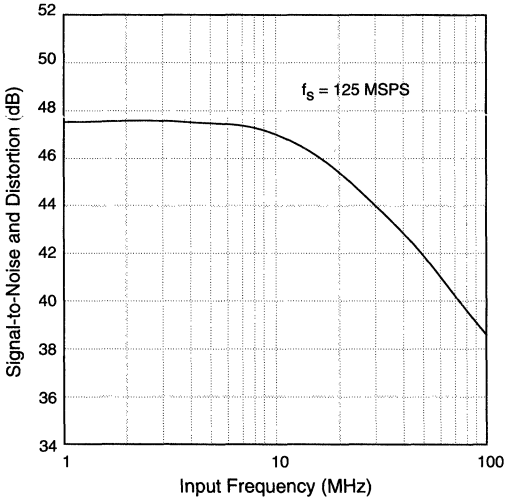
SNR vs Input Frequency



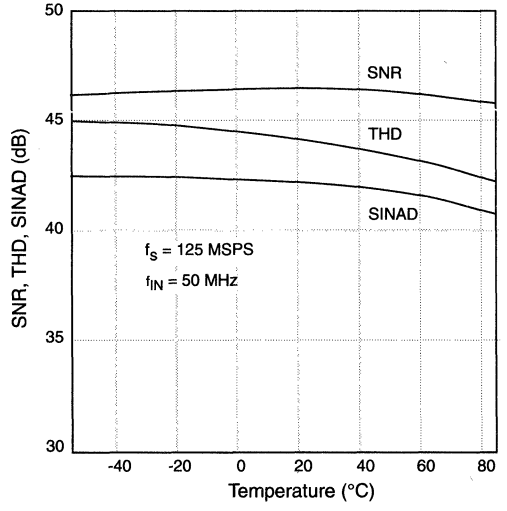
THD vs Input Frequency



SINAD vs Input Frequency



SNR, THD, SINAD vs Temperature



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GENERAL DESCRIPTION

The SPT7710 is a fast monolithic 8-bit parallel flash A/D converter. The nominal conversion rate is 150 MSPS and the analog bandwidth is in excess of 200 MHz. A major advance over previous flash converters is the inclusion of 256 input preamplifiers between the reference ladder and input comparators. (See block diagram.) This not only reduces clock transient kickback to the input and reference ladder due to a low AC beta but also reduces the effect of the dynamic state of the input signal on the latching characteristics of the input comparators. The preamplifiers act as buffers and stabilize the input capacitance so that it remains constant for varying input voltages and frequencies and, therefore, makes the part easier to drive than previous flash converters. The SPT7710 incorporates a proprietary decoding scheme that reduces metastable errors (sparkle codes or *flyers*) to a maximum of 1 LSB.

The SPT7710 has true differential analog and digital data paths from the preamplifiers to the output buffers (Current Mode Logic) for reducing potential missing codes while rejecting common mode noise.

Signature errors are also reduced by careful layout of the analog circuitry. Every comparator also has a clock buffer to reduce differential delays and to improve signal-to-noise ratio. The output drive capability of the device can provide full ECL swings into 50 Ω loads.

TYPICAL INTERFACE CIRCUIT

The typical interface circuit is shown in figure 1. The SPT7710 is relatively easy to apply depending on the accuracy needed in the intended application. Wire-wrap may be employed with careful point-to-point ground connections if desired, but to achieve the best operation, a double sided PC board with a ground plane on the component side separated into digital and analog sections will give the best performance. The converter is bonded-out to place the digital pins on the left side of the package and the analog pins on the right side. Additionally, an RF bead connection through a single point from the analog to digital ground planes will reduce ground noise pickup.

The circuit in figure 2 (PGA and cerquad packages only) is intended to show the most elaborate method of achieving the least error by correcting for integral nonlinearity, input induced distortion, and power supply/ground noise. This is achieved by the use of external reference ladder tap connections, an input buffer and supply decoupling. The function of each pin and external connections to other components is as follows:

Figure 1 - SPT7710 Typical Interface Circuit 1

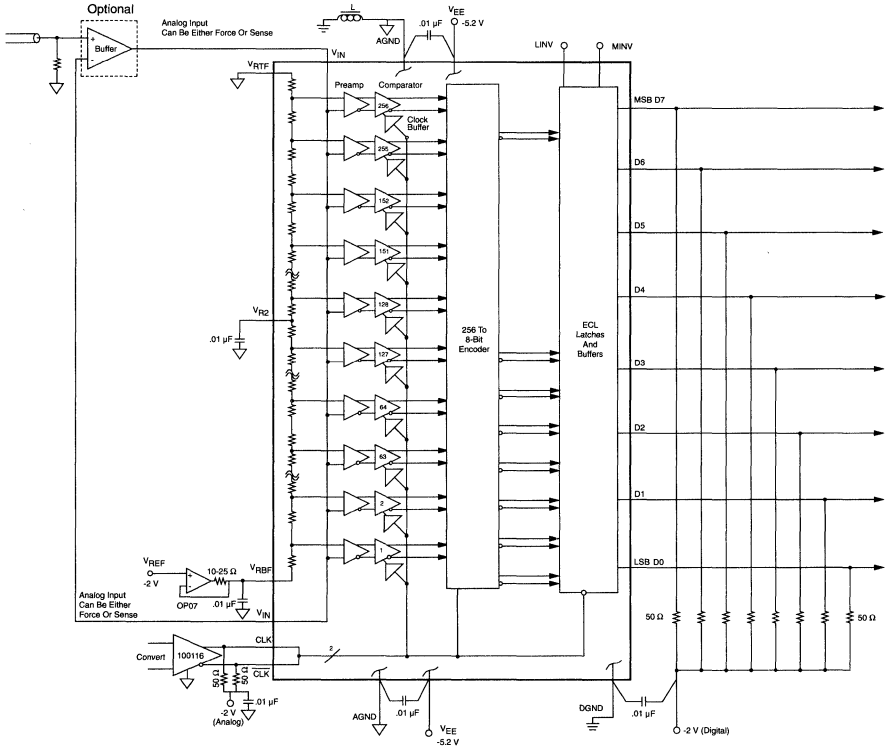
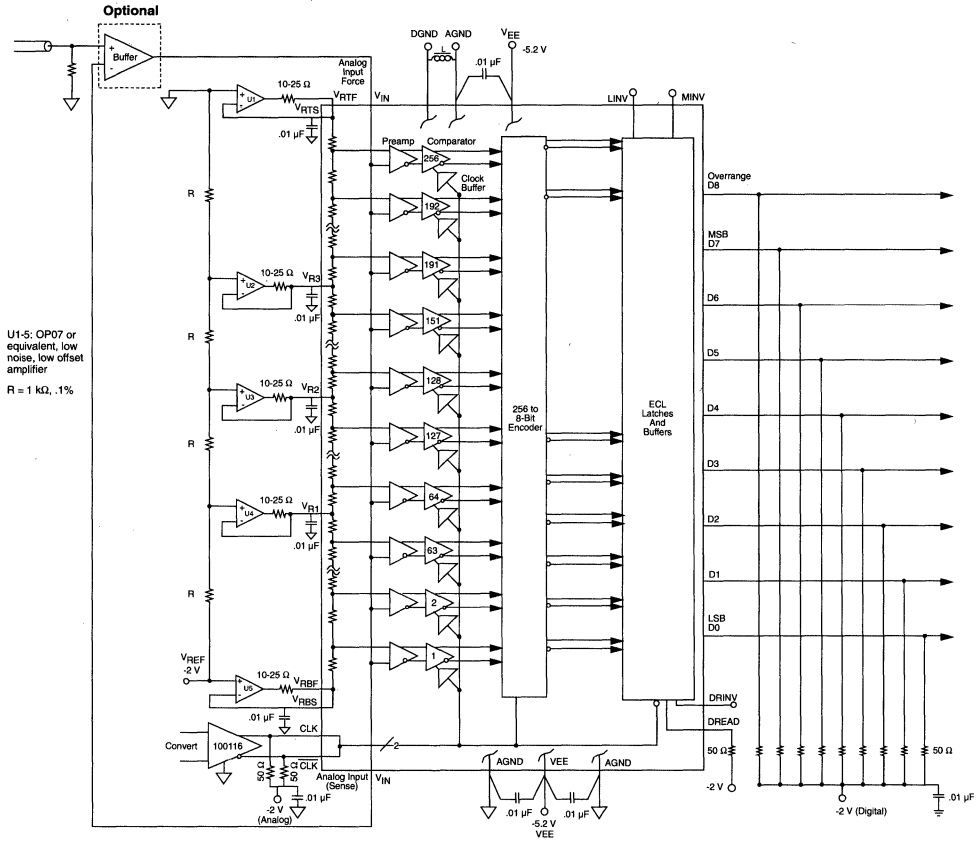


Figure 2 - SPT7710 Typical Interface Circuit 2 (PGA and Cerquad Packages Only)



V_{EE}, AGND, DGND

V_{EE} is the supply pin with AGND as ground for the device. The power supply pins should be bypassed as close to the device as possible with at least a .01 µF ceramic capacitor. A 1 µF tantalum should also be used for low frequency suppression. DGND is the ground for the ECL outputs and is to be referenced to the output pulldown voltage and appropriately bypassed as shown in figure 1.

V_{IN} (ANALOG INPUT)

There are two analog input pins that are tied to the same point internally. Either one may be used as an analog input *sense* and the other for input *force*. This is convenient for testing the source signal to see if there is sufficient drive capability. The pins can also be tied together and driven by the same source. The SPT7710 is superior to similar devices due to a preamplifier stage before the comparators. This makes the device easier to drive because it has constant capacitance and induces less slew rate distortion. An optional input buffer may be used.

CLK, $\overline{CLK}$ (CLOCK INPUTS)

The clock inputs are designed to be driven differentially with ECL levels. The clock may be driven single-ended since $\overline{CLK}$ is internally biased to -1.3 V. (See clock input circuit.) $\overline{CLK}$ may be left open but a .01 µF bypass capacitor from $\overline{CLK}$ to AGND is recommended. NOTE: System performance may be degraded due to increased clock noise or jitter.

MINV, LINV (OUTPUT LOGIC CONTROL)

These are ECL-compatible digital controls for changing the output code from straight binary to two's complement, etc. For more information, see table I. Both MINV and LINV are in the logic low (0) state when they are left open. The high state can be obtained by tying to AGND through a diode or 3.9 kΩ resistor.

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Table I - Output Coding

MINV LINV	0 0	0 1	1 0	1 1
0V	111...11	100...00	011...11	000...00
.	111...10	100...01	011...10	000...01
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
V_{IN} .	100...00	111...11	000...00	011...11
.	011...11	000...00	111...11	100...00
.	.	.	.	.
.	.	.	.	.
.	.	.	.	.
.	000...01	011...10	100...01	111...10
-2V	000...00	011...11	100...00	111...11

1: V_{IH}, V_{OH} 0: V_{IL}, V_{OL}

D0 TO D7 (DIGITAL OUTPUTS)

The digital outputs can drive ECL levels into 50 Ω when pulled down to -2 V. When pulled down to -5.2 V, the outputs can drive 150 Ω to 1 kΩ loads.

V_{RBF}, V_{R2}, V_{RTF} (REFERENCE INPUTS)

There are two reference inputs and one external reference voltage tap. These are -2 V (V_{RBF}), mid-tap (V_{R2}) and AGND (V_{RTF}). The reference pins can be driven as shown in figure 1. V_{R2} should be bypassed to AGND for further noise suppression.

V_{RBF}, V_{RBS}, V_{R1}, V_{R2}, V_{R3}, V_{RTF}, V_{RTS} REFERENCE INPUTS *(PGA AND CERQUAD PACKAGES ONLY)*

These are five external reference voltage taps from -2 V (V_{RBF}) to AGND (V_{RTF}) which can be used to control integral linearity over temperature. The taps can be driven by op amps as shown in figure 2. These voltage level inputs can be bypassed to AGND for further noise suppression if so desired. V_{RB} and V_{RT} have force and sense pins for monitoring the top and bottom voltage references.

N/C

All *Not Connected* pins should be tied to DGND on the left side of the package and to AGND on the right side of the package.

DREAD - DATA READY, DRINV - DATA READY INVERSE *(PGA AND CERQUAD PACKAGES ONLY)*

The data ready pin is a flag that goes high or low at the output when data is valid or ready to be received. It is essentially a delay line that accounts for the time necessary for information to be clocked through the SPT7710's decoders and latches. This function is useful for interfacing with high speed memory. Using the data ready output to latch the output data ensures minimum setup and hold times. DRINV is a data ready inverse control pin (see Timing Diagram).

D8 - OVERRANGE *(PGA AND CERQUAD PACKAGES ONLY)*

This is an overrange function. When the SPT7710 is in an overrange condition, D8 goes high and all data outputs go high as well. This makes it possible to include the SPT7710 into higher resolution systems.

OPERATION

The SPT7710 has 256 preamp/comparator pairs which are each supplied with the voltage from V_{RTF} to V_{RBF} divided equally by the resistive ladder as shown in the block diagram. This voltage is applied to the positive input of each preamplifier/comparator pair. An analog input voltage applied at V_{IN} is connected to the negative inputs of each preamplifier/comparator pair. The comparators are then clocked through each comparator's individual clock buffer. When CLK pn is in the low state, the master or input stage of the comparators compares the analog input voltage to the respective reference voltage. When CLK changes from low to high, the comparators are latched to the state prior to the clock transition and output logic codes in sequence from the top comparators, closest to V_{RTF} (0 V), down to the point where the magnitude of the input signal changes sign (thermometer code). The output of each comparator is then registered into four 64-to-6 bit decoders when CLK is changed from high to low. At the output of the decoders is a set of four 7-bit latches which are enabled (*track*) when CLK changes from high to low. From here, the outputs of the latches are coded into 6 LSBs from 4 columns and 4 columns are coded into 2 MSBs. Next are the MINV and LINV controls for output inversions which consist of a set of eight XOR gates. Finally, 8 ECL output latches and buffers are used to drive the external loads. The conversion takes one clock cycle from the input to the data outputs.

Figure 3 - Timing Diagram

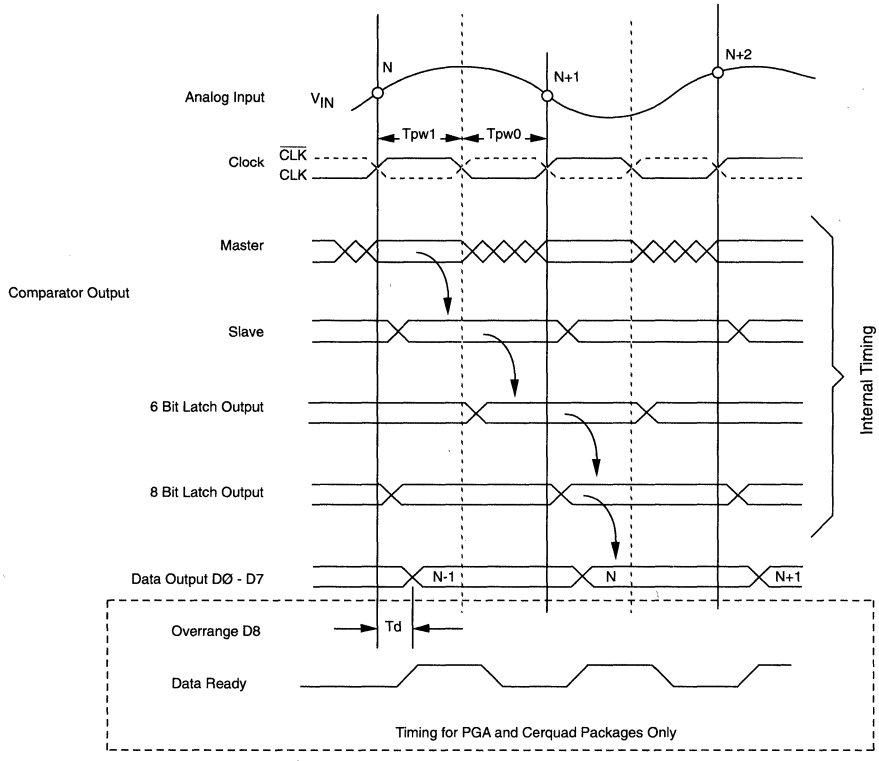
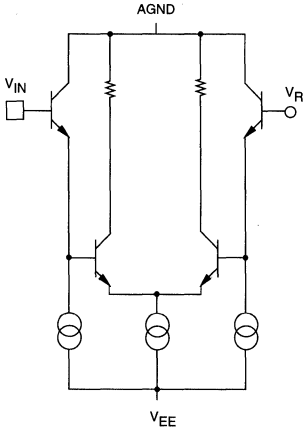
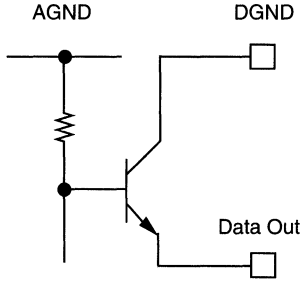


Figure 4 - Subcircuit Schematics

Input Circuit



Output Circuit



MINV, LINV Input Circuit

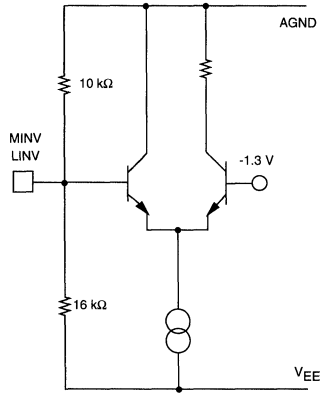


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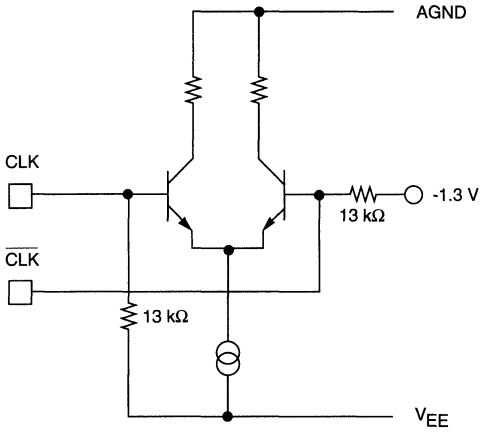
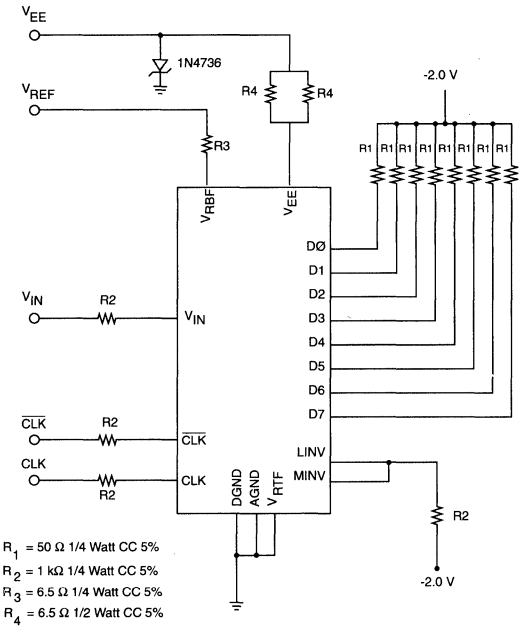
Figure 5 - Clock Input



EVALUATION BOARDS

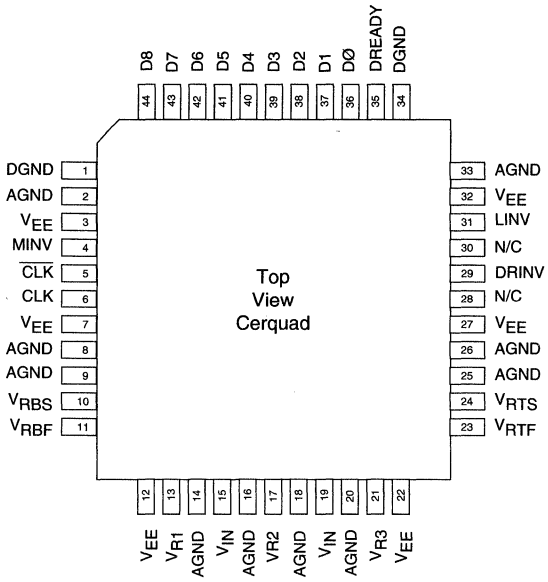
The EB7710 evaluation board is available to aid designers in demonstrating the full performance of the SPT7710. This board includes a voltage reference circuit, clock driver circuit, output data latches and an on-board reconstruction of the digital data. An application note describing the operation of this board as well as application tips is also available. Contact the factory for price and delivery.

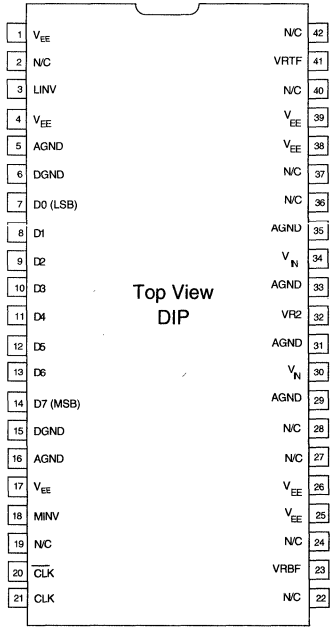
Figure 6 - Burn-In Circuit (42L DIP Package Only)



R_1 = 50 Ω 1/4 Watt CC 5%
R_2 = 1 kΩ 1/4 Watt CC 5%
R_3 = 6.5 Ω 1/4 Watt CC 5%
R_4 = 6.5 Ω 1/2 Watt CC 5%
V_{REF} = -2.00 Volts
V_{EE} = -6.6 Volts

PIN ASSIGNMENTS SPT7710



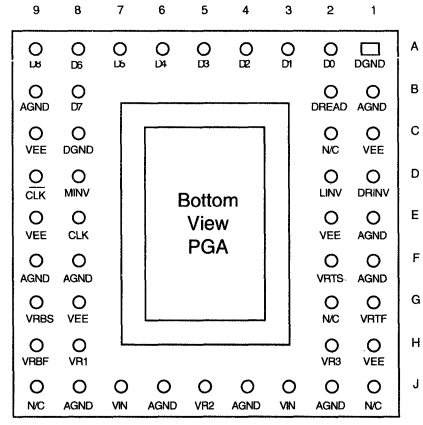


PIN FUNCTIONS

NAME	FUNCTION
LINV	D0 through D6 Output Inversion Control Pin
V_{EE}	Negative Analog Supply Nominally -5.2 V
DGND	Digital Ground
D0	Digital Data Output (LSB)
D1-D6	Digital Data Output
D7	Digital Data Output (MSB)
MINV	D7 Output Inversion Control Pin
$\overline{CLK}$	Inverse ECL Clock Input Pin
CLK	ECL Clock Input Pin
AGND	Analog Ground
V_{IN}	Analog Input; Can be Connected to the
	Input Signal or Used as a Sense
V_{R2}	Reference Voltage Tap 2 (-1.0 V typ)
V_{RTF}	Reference Voltage Top
V_{RBF}	Reference Voltage Bottom

The following pins are on PGA and cerquad packages only.

DRINV	Data Ready Inverse
DREAD	Data Ready Output
Overrange	Overrange Output D8
V_{R1}	Reference Voltage Tap 1 (-1.5 V typ)
V_{R3}	Reference Voltage Tap 3 (-0.5 V typ)
V_{RTS}	Reference Voltage Top, Sense
V_{RBS}	Reference Voltage Bottom, Sense



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LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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SIGNAL PROCESSING TECHNOLOGIES

SPT7725

8-BIT, 300 MSPS FLASH A/D CONVERTER

3

FEATURES

- Metastable Errors Reduced to 1 LSB
- Low Input Capacitance: 10 pF
- Wide Input Bandwidth: 210 MHz
- 300 MSPS Conversion Rate
- Typical Power Dissipation: 2.2 Watts

APPLICATIONS

- Digital Oscilloscopes
- Transient Capture
- Radar, EW, ECM
- Direct RF Down-Conversion
- Medical Electronics: Ultrasound, CAT Instrumentation

GENERAL DESCRIPTION

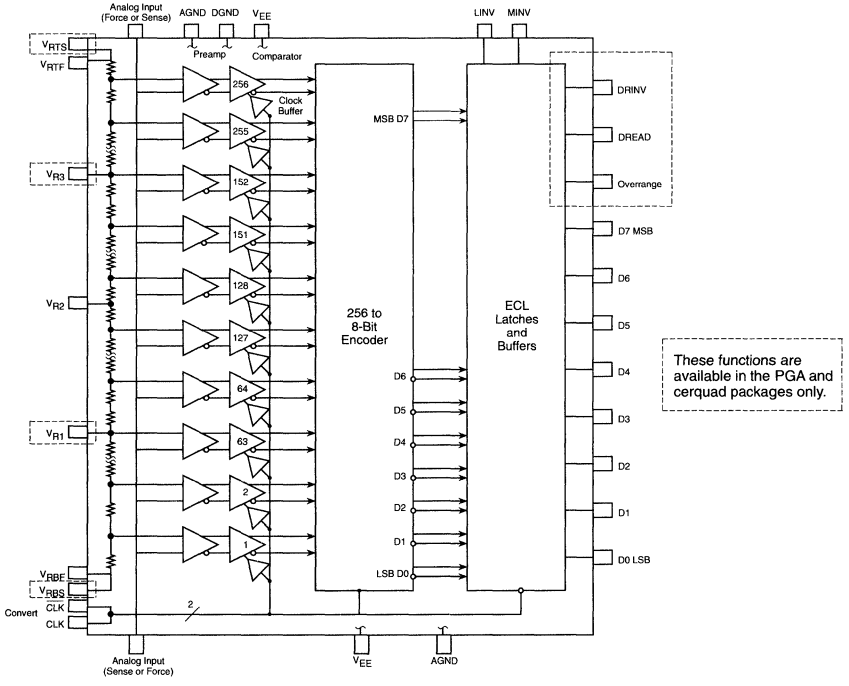
The SPT7725 is a monolithic flash A/D converter capable of digitizing a two volt analog input signal into 8-bit digital words at a 300 MSPS (typ) update rate.

For most applications, no external sample-and-hold is required for accurate conversion due to the device's narrow aperture time, wide bandwidth, and low input capacitance. A single standard -5.2 volt power supply is required for operation of the SPT7725, with nominal power dissipation of 2.2 W.

A proprietary decoding scheme reduces metastable errors to the 1 LSB level.

The part is packaged in a 42L ceramic sidebrazed DIP which is pin compatible with the SPT7710. A 44L surface-mount cerquad package and a 46L PGA package are also available which allow access to additional reference ladder taps, an overrange bit, and a data ready output. They are also pin-compatible with the SPT7710. The SPT7725 is available in industrial and military temperature ranges and in /883 compliant versions.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages
- Negative Supply Voltage (V_{EE} TO GND) ..... -7.0 to +0.5 V
- Ground Voltage Differential ..... -0.5 to +0.5 V

Input Voltage
- Analog Input Voltage ..... V_{EE} to +0.5 V
- Reference Input Voltage ..... V_{EE} to +0.5 V
- Digital Input Voltage ..... V_{EE} to +0.5 V
- Reference Current V_{RTF} to V_{RBF} ..... 25 mA

Output
- Digital Output Current ..... 0 to -30 mA

Temperature
- Operating Temperature ..... -25°C ambient to +85 °C ambient
- junction ..... +150 °C
- Lead Temperature, (soldering 10 seconds). ..... +300 °C
- Storage Temperature ..... -65 to +150 °C

Notes: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

$T_A=T_{MIN}$ to T_{MAX}, V_{EE}=-5.2 V, R_{Source}=50 Ω, V_{RBF}=-2.00 V, V_{R2}=-1.00 V, V_{RTF}=0.00 V, f_{clk}=250 MHz, Duty Cycle=50%, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7725A MIN	SPT7725A TYP	SPT7725A MAX	SPT775B MIN	SPT775B TYP	SPT775B MAX	UNITS
DC Accuracy									
Integral Linearity		VI	-0.75	±0.60	+0.75	-0.95	±0.80	+0.95	LSB
Differential Linearity		VI	-0.75		+0.75	-0.95		+0.95	LSB
No missing codes			Guaranteed			Guaranteed			
Analog Input									
Offset Error V_{RT}		IV	-30		+30	-30		+30	mV
Offset Error V_{RB}		IV	-30		+30	-30		+30	mV
Input Voltage Range		VI	-2.0		0.0	-2.0		0.0	Volts
Input Capacitance	Over full input range	V		10			10		pF
Input Resistance		V		15			15		kΩ
Input Current		VI		250	500		250	500	µA
Input Slew Rate		V		1,000			1,000		V/µs
Large Signal Bandwidth	V_{IN}=F.S.	V		210			210		MHz
Small Signal Bandwidth	V_{IN}=500 mV P-P	V		335			335		MHz
Reference Input									
Ladder Resistance		VI	100	200	300	100	200	300	Ω
Reference Bandwidth		V		10			10		MHz
Timing Characteristics									
Maximum Sample Rate		VI	250	300		250	300		MSPS
Clock to Data Delay		V		2.4			2.4		ns
Output Delay TEMPCO		V		2.0			2.0		ps/°C
CLK-to-Data Ready Delay (t_d)		V		2.0			2.0		ns
Aperture Jitter		V		5.0			5.0		ps
Acquisition Time		V		1.5			1.5		ns
Dynamic Performance									
Signal-to-Noise Ratio	F_{IN} = 3.58 MHz	VI	45	47		44	46		dB
	F_{IN} = 100 MHz	VI	39	42		38	41		dB
Total Harmonic Distortion	F_{IN} = 3.58 MHz	VI	-48	-52		-46	-50		dB
	F_{IN} = 100 MHz	VI	-40	-43		-39	-42		dB
Signal-to-Noise and Distortion	F_{IN} = 3.58 MHz	VI	44	46		42	44		dB
(SINAD)	F_{IN} = 100 MHz	VI	37	39		35	37		dB

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ELECTRICAL SPECIFICATIONS

$T_A=T_{MIN}$ to T_{MAX}, V_{EE}=-5.2 V, R_{Source}=50 Ω, V_{RBF}=-2.00 V, V_{R2}=-1.00 V, V_{RTF}=0.00 V, f_{clk}=250 MHz, Duty Cycle=50%, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7725A MIN	SPT7725A TYP	SPT7725A MAX	SPT775B MIN	SPT775B TYP	SPT775B MAX	UNITS
Digital Inputs									
Digital Input High Voltage (MINV, LINV)		VI	-1.1		-0.7	-1.1		-0.7	Volts
Digital Input Low Voltage (MINV, LINV)		VI	-2.0		-1.5	-2.0		-1.5	Volts
Clock Synchronous Input Currents		V		40			40		µA
Clock Low Width, T_{PWL}		VI	2	1.8		2	1.8		ns
Clock High Width, T_{PWH}		VI	2	1.8		2	1.8		ns
Digital Output									
Digital Output High Voltage	50 Ω to -2 V	VI	-1.1			-1.1			Volts
Digital Output Low Voltage	50 Ω to -2 V	VI			-1.5			-1.5	Volts
Power Supply Requirements									
Supply Current	T = +25 °C	I		425	550		425	550	mA
Power Dissipation	T = +25 °C	I		2.2	2.9		2.2	2.9	W

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

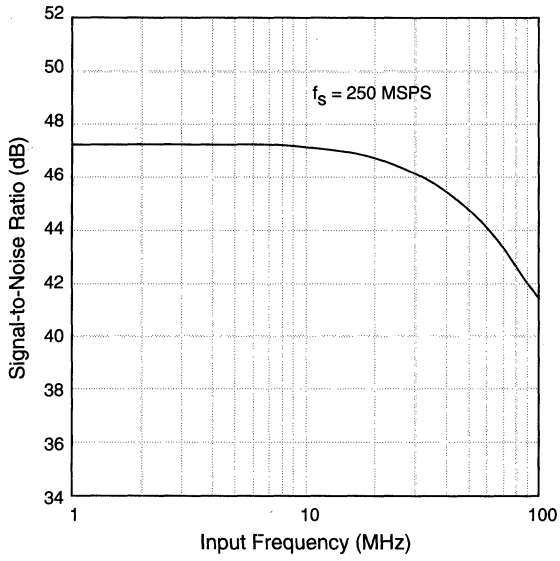
All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests; therefore, $T_J = T_C = T_A$.

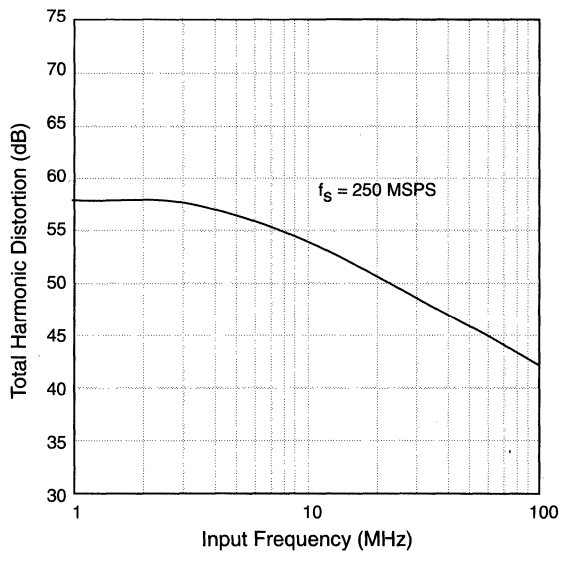
TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

TYPICAL PERFORMANCE CHARACTERISTICS

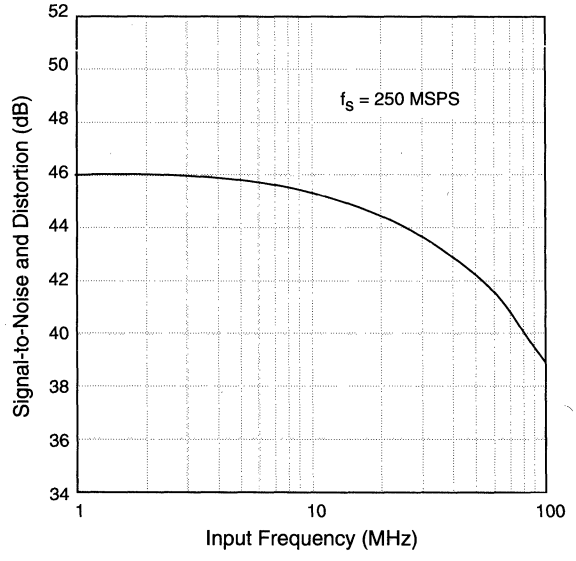
SNR vs Input Frequency



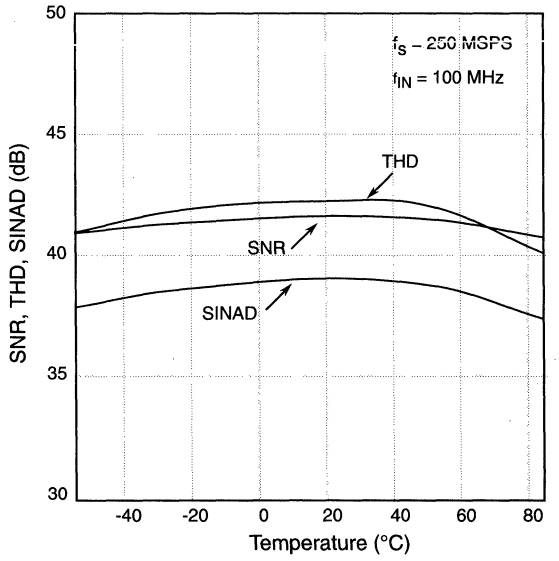
THD vs Input Frequency



SINAD vs Input Frequency



SNR, THD, SINAD vs Temperature



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GENERAL DESCRIPTION

The SPT7725 is a fast monolithic 8-bit parallel flash A/D converter. The nominal conversion rate is 300 MSPS and the analog bandwidth is in excess of 200 MHz. A major advance over previous flash converters is the inclusion of 256 input preamplifiers between the reference ladder and input comparators. (See block diagram.) This not only reduces clock transient kickback to the input and reference ladder due to a low AC beta but also reduces the effect of the dynamic state of the input signal on the latching characteristics of the input comparators. The preamplifiers act as buffers and stabilize the input capacitance so that it remains constant for varying input voltages and frequencies and therefore makes the part easier to drive than previous flash converters. The SPT7725 incorporates a proprietary decoding scheme that reduces metastable errors (sparkle codes or *flyers*) to a maximum of 1 LSB.

The SPT7725 has true differential analog and digital data paths from the preamplifiers to the output buffers (Current Mode Logic) for reducing potential missing codes while rejecting common mode noise.

Signature errors are also reduced by careful layout of the analog circuitry. Every comparator also has a clock buffer to reduce differential delays and to improve signal-to-noise ratio. The output drive capability of the device can provide full ECL swings into 50 Ω loads.

TYPICAL INTERFACE CIRCUIT

The typical interface circuit is shown in figure 1. The SPT7725 is relatively easy to apply depending on the accuracy needed in the intended application. Wire-wrap may be employed with careful point-to-point ground connections if desired, but to achieve the best operation, a double sided PC board with a ground plane on the component side separated into digital and analog sections will give the best performance. The converter is bonded-out to place the digital pins on the left side of the package and the analog pins on the right side. Additionally, an RF bead connection through a single point from the analog to digital ground planes will reduce ground noise pickup.

The circuit in figure 2 (PGA and cerquad packages only) is intended to show the most elaborate method of achieving the least error by correcting for integral nonlinearity, input induced distortion, and power supply/ground noise. This is achieved by the use of external reference ladder tap connections, an input buffer and supply decoupling. The function of each pin and external connections to other components is as follows:

Figure 1 - SPT7725 Typical Interface Circuit 1

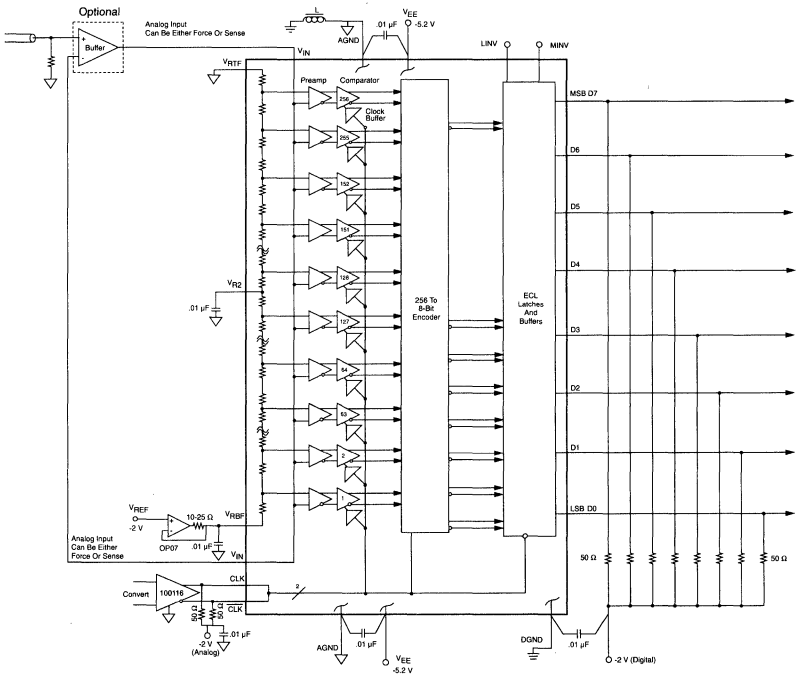
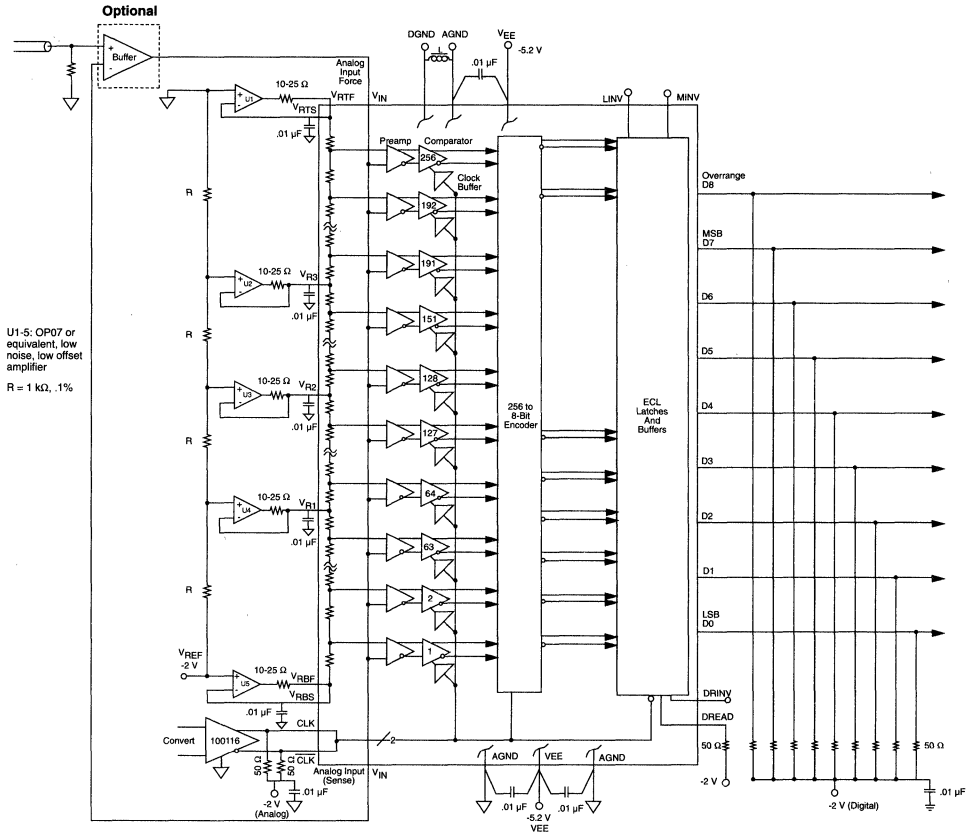


Figure 2 - SPT7725 Typical Interface Circuit 2 (PGA and Cerquad Packages Only)



V_{EE}, AGND, DGND

V_{EE} is the supply pin with AGND as ground for the device. The power supply pins should be bypassed as close to the device as possible with at least a .01 µF ceramic capacitor. A 1 µF tantalum should also be used for low frequency suppression. DGND is the ground for the ECL outputs and is to be referenced to the output pulldown voltage and appropriately bypassed as shown in figure 1.

V_{IN} (ANALOG INPUT)

There are two analog input pins that are tied to the same point internally. Either one may be used as an analog input *sense* and the other for input *force*. This is convenient for testing the source signal to see if there is sufficient drive capability. The pins can also be tied together and driven by the same source. The SPT7725 is superior to similar devices due to a preamplifier stage before the comparators. This makes the device easier to drive because it has constant capacitance and induces less slew rate distortion. An optional input buffer may be used.

CLK, $\overline{CLK}$ (CLOCK INPUTS)

The clock inputs are designed to be driven differentially with ECL levels. The clock may be driven single-ended since $\overline{CLK}$ is internally biased to -1.3 V. (See clock input circuit.) $\overline{CLK}$ may be left open but a .01 µF bypass capacitor from $\overline{CLK}$ to AGND is recommended. NOTE: System performance may be degraded due to increased clock noise or jitter.

MINV, LINV (OUTPUT LOGIC CONTROL)

These are ECL-compatible digital controls for changing the output code from straight binary to two's complement, etc. For more information, see table I. Both MINV and LINV are in the logic low (0) state when they are left open. The high state can be obtained by tying to AGND through a diode or 3.9 kΩ resistor.

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Table I - Output Coding

	MINV	0	0	1	1
	LINV	0	1	0	1
	0V	111...11	100...00	011...11	000...00
	.	111...10	100...01	011...10	000...01
	.	.	.	.	.
	.	.	.	.	.
	.	.	.	.	.
V_{IN}	.	100...00	111...11	000...00	011...11
	.	011...11	000...00	111...11	100...00
	.	.	.	.	.
	.	.	.	.	.
	.	.	.	.	.
	.	000...01	011...10	100...01	111...10
	-2V	000...00	011...11	100...00	111...11
		1: V_{IH}, V_{OH}		0: V_{IL}, V_{OL}	

D0 TO D7 (DIGITAL OUTPUTS)

The digital outputs can drive ECL levels into 50 Ω when pulled down to -2 V. When pulled down to -5.2 V, the outputs can drive 150 Ω to 1 kΩ loads.

V_{RBF}, V_{R2}, V_{RTF} (REFERENCE INPUTS)

There are two reference inputs and one external reference voltage tap. These are -2 V (V_{RBF}), mid-tap (V_{R2}) and AGND (V_{RTF}). The reference pins can be driven as shown in figure 1. V_{R2} should be bypassed to AGND for further noise suppression.

V_{RBF}, V_{RBS}, V_{R1}, V_{R2}, V_{R3}, V_{RTF}, V_{RTS} REFERENCE INPUTS *(PGA AND CERQUAD PACKAGES ONLY)*

These are five external reference voltage taps from -2 V (V_{RBF}) to AGND (V_{RTF}) which can be used to control integral linearity over temperature. The taps can be driven by op amps as shown in figure 2. These voltage level inputs can be bypassed to AGND for further noise suppression if so desired. V_{RB} and V_{RT} have "force" and "sense" pins for monitoring the top and bottom voltage references.

N/C

All *Not Connected* pins should be tied to DGND on the left side of the package and to AGND on the right side of the package.

DREAD - DATA READY, DRINV - DATA READY INVERSE *(PGA AND CERQUAD PACKAGES ONLY)*

The data ready pin is a flag that goes high or low at the output when data is valid or ready to be received. It is essentially a delay line that accounts for the time necessary for information to be clocked through the SPT7725's decoders and latches. This function is useful for interfacing with high speed memory. Using the data ready output to latch the output data ensures minimum setup and hold times. DRINV is a data ready inverse control pin (see Timing Diagram).

D8 - OVERRANGE *(PGA AND CERQUAD PACKAGES ONLY)*

This is an overrange function. When the SPT7725 is in an overrange condition, D8 goes high and all data outputs go high as well. This makes it possible to include the SPT7725 into higher resolution systems.

OPERATION

The SPT7725 has 256 preamp/comparator pairs which are each supplied with the voltage from V_{RTF} to V_{RBF} divided equally by the resistive ladder as shown in the block diagram. This voltage is applied to the positive input of each preamplifier/comparator pair. An analog input voltage applied at V_{IN} is connected to the negative inputs of each preamplifier/comparator pair. The comparators are then clocked through each comparator's individual clock buffer. When CLK is in the low state, the master or input stage of the comparators compares the analog input voltage to the respective reference voltage. When CLK changes from low to high, the comparators are latched to the state prior to the clock transition and output logic codes in sequence from the top comparators, closest to V_{RTF} (0 V), down to the point where the magnitude of the input signal changes sign (thermometer code). The output of each comparator is then registered into four 64-to-6 bit decoders when CLK is changes from high to low. At the output of the decoders is a set of four 7-bit latches which are enabled (*track*) when CLK changes from high to low. From here, the outputs of the latches are coded into 6 LSBs from 4 columns and 4 columns are coded into 2 MSBs. Next are the MINV and LINV controls for output inversions which consist of a set of eight XOR gates. Finally, 8 ECL output latches and buffers are used to drive the external loads. The conversion takes one clock cycle from the input to the data outputs.

Figure 3 - Timing Diagram

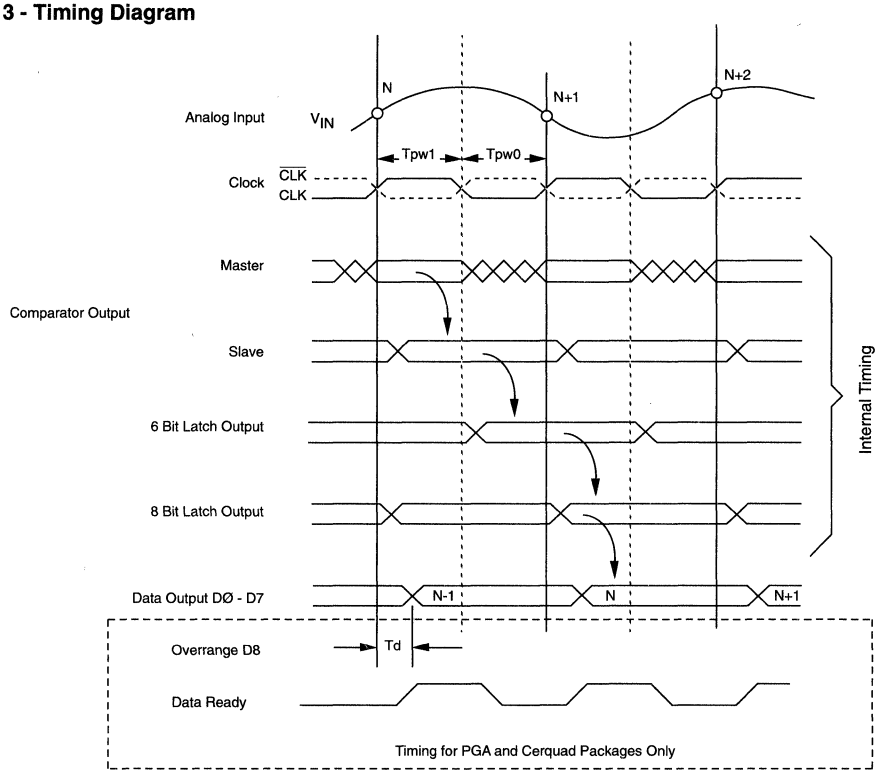
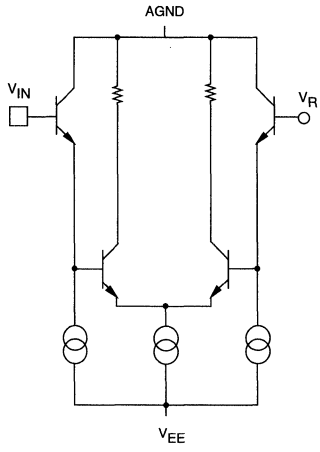
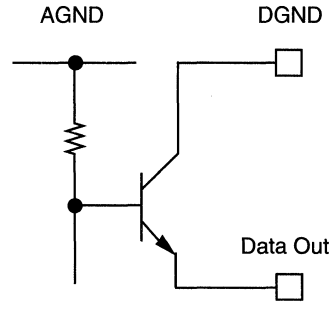


Figure 4 - Subcircuit Schematics

Input Circuit



Output Circuit



MINV, LINV Input Circuit

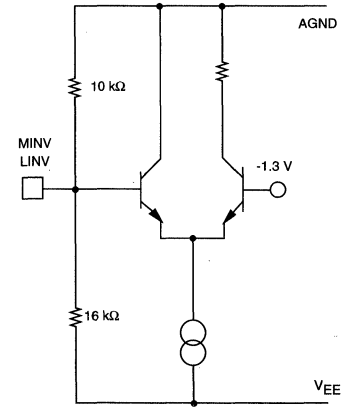


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Figure 5 - Clock Input

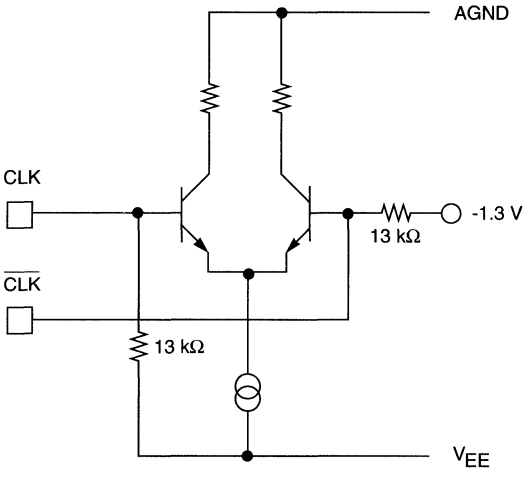
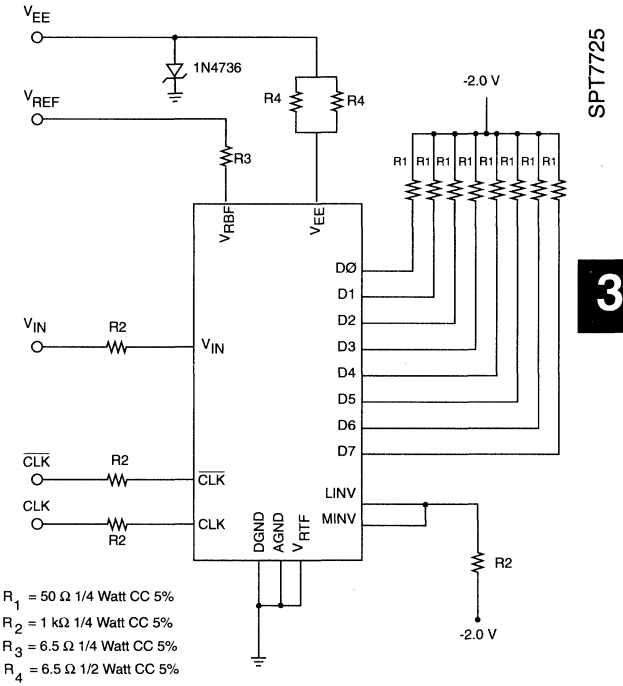


Figure 6 - Burn-In Circuit (42L DIP Package Only)

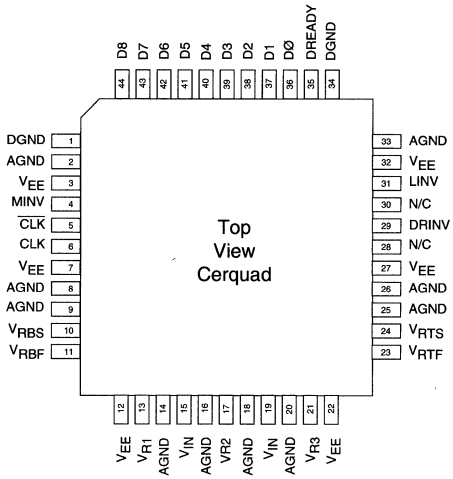


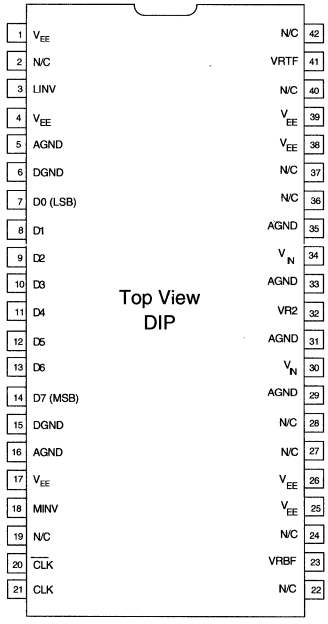
R_1 = 50 Ω 1/4 Watt CC 5%
R_2 = 1 kΩ 1/4 Watt CC 5%
R_3 = 6.5 Ω 1/4 Watt CC 5%
R_4 = 6.5 Ω 1/2 Watt CC 5%
V_{REF} = -2.00 Volts
V_{EE} = -6.6 Volts

EVALUATION BOARDS

The EB7725 evaluation board is available to aid designers in demonstrating the full performance of the SPT7725. This board includes a voltage reference circuit, clock driver circuit, output data latches and an on-board reconstruction of the digital data. An application note describing the operation of this board as well as application tips is also available. Contact the factory for price and delivery.

PIN ASSIGNMENTS SPT7725



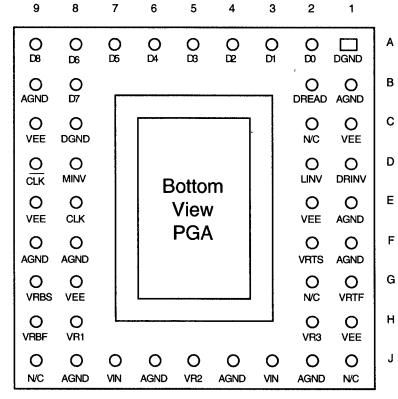


PIN FUNCTIONS

NAME	FUNCTION
LINV	D0 through D6 Output Inversion Control Pin
V_{EE}	Negative Analog Supply Nominally -5.2 V
DGND	Digital Ground
D0	Digital Data Output (LSB)
D1-D6	Digital Data Output
D7	Digital Data Output (MSB)
MINV	D7 Output Inversion Control Pin
$\overline{CLK}$	Inverse ECL Clock Input Pin
CLK	ECL Clock Input Pin
AGND	Analog Ground
V_{IN}	Analog Input; Can be Connected to the
	Input Signal or Used as a Sense
V_{R2}	Reference Voltage Tap 2 (-1.0 V typ)
V_{RTF}	Reference Voltage Top
V_{RBF}	Reference Voltage Bottom

The following pins are on PGA and cerquad packages only.

DRINV	Data Ready Inverse
DREAD	Data Ready Output
Overrange	Overrange Output D8
V_{R1}	Reference Voltage Tap 1 (-1.5 V typ)
V_{R3}	Reference Voltage Tap 3 (-0.5 V typ)
V_{RTS}	Reference Voltage Top, Sense
V_{RBS}	Reference Voltage Bottom, Sense



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LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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SIGNAL PROCESSING TECHNOLOGIES

SPT7750

8-BIT, 500 MSPS FLASH A/D CONVERTER

FEATURES

- 1:2 Demuxed ECL Compatible Outputs
- Wide Input Bandwidth - 900 MHz
- Low Input Capacitance - 15 pF (MQUAD)
- Metastable Errors Reduced to 1 LSB
- Monolithic for Low Cost
- Gray Code Output

APPLICATIONS

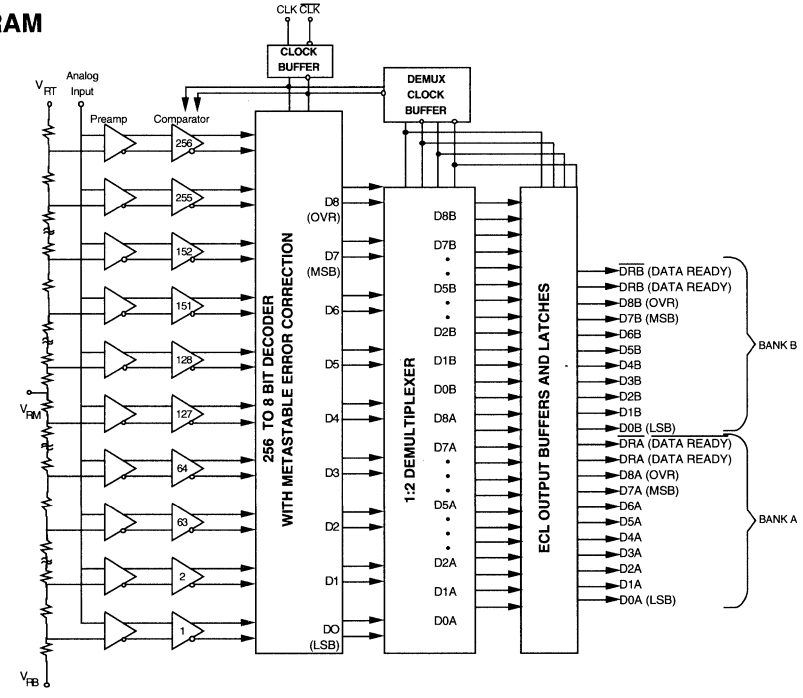
- Digital Oscilloscopes
- Transient Capture
- Radar, EW, ECM
- Direct RF Down-Conversion

GENERAL DESCRIPTION

The SPT7750 is a full parallel (flash) analog-to-digital converter capable of digitizing full scale (0 to -2 V) inputs into eight-bit digital words at an update rate of 500 MSPS. The ECL-compatible outputs are demultiplexed into two separate output banks, each with differential data ready outputs to ease the task of data capture. The SPT7750's wide input bandwidth and low capacitance eliminate the need for external track-and-hold amplifiers for most applications. A proprietary decoding scheme reduces metastable errors to the 1 LSB level. The SPT7750 operates from a single -5.2 V supply, with a nominal power dissipation of 5.5 W.

The SPT7750 is available in a 68L PGA and an 80L surface-mount MQUAD package over the industrial temperature range of -25 to + 85 °C. Contact the factory for availability of die and /883 versions.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages
- Negative Supply Voltage (V_{EE} TO GND) ..... -7.0 to +0.5 V
- Ground Voltage Differential ..... -0.5 to +0.5 V

Input Voltage
- Analog Input Voltage ..... +0.5 V to V_{EE}
- Reference Input Voltage ..... +0.5 V to V_{EE}
- Digital Input Voltage ..... +0.5 V to V_{EE}
- Reference Current V_{RT} to V_{RB} ..... 35 mA

Output
- Digital Output Current ..... 0 to -28 mA

Temperature
- Operating Temperature, ambient ..... -25 to +85 °C
- case ..... +125 °C
- junction ..... +150 °C
- Lead Temperature, (soldering 10 seconds). ..... +300 °C
- Storage Temperature ..... -65 to +150 °C

Notes: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

$T_J = T_C = T_A = +25$ °C , V_{EE}=-5.2 V, V_{RB}=-2.00 V, V_{RM}=-1.0 V, V_{RT}=0.00 V, f_{clk}=500 MHz, Duty Cycle=50%, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7750A MIN	SPT7750A TYP	SPT7750A MAX	SPT7750B MIN	SPT7750B TYP	SPT7750B MAX	UNITS
Resolution				8			8		Bits
DC Accuracy (+25 °C)									
Integral Nonlinearity	f_{CLK} = 100 kHz	I	-1.0		+1.0	-1.5		+1.5	LSB
Differential Nonlinearity	f_{CLK} = 100 kHz	I	-0.85		+0.95	-0.95		+1.5	LSB
No Missing Codes				Guaranteed			Guaranteed		
Analog Input									
Input Voltage Range		I	V_{RB}		V_{RT}	V_{RB}		V_{RT}	V
Input Bias Current	V_{IN}=0 V	I		.75	2.0		.75	2.0	mA
Input Resistance		V		15			15		kΩ
Input Capacitance		V							
MQuad	Over Full Input Range	V		15			15		pF
PGA	Over Full Input Range	V		30			30		pF
Input Bandwidth									
Small Signal		V		900			900		MHz
Large Signal		V		500			500		MHz
Offset Error V_{RT}		IV	-30		+30	-30		+30	mV
Offset Error V_{RB}		IV	-30		+30	-30		+30	mV
Input Slew Rate		V		5			5		V/ns
Reference Input									
Ladder Resistance		I	60	80		60	80		Ω
Reference Bandwidth		V		30			30		MHz
Timing Characteristics									
Maximum Sample Rate		I	500			500			MHz
Aperture Jitter		V		2			2		ps
Acquisition Time		V		250			250		ps
CLK to DATA READY Delay		IV	0.9	1.4	1.9	0.9	1.4	1.9	ns
Clock to Data Delay		IV	1.25	1.75	2.25	1.25	1.75	2.25	ns
Dynamic Performance									
Signal-To-Noise Ratio (without Harmonics)									
f_{In} = 50 MHz		I	47			45			dB
f_{In} = 250 MHz		I	44			42			dB
Total Harmonic Distortion									
f_{In} = 50 MHz		I	-46			-44			dBc
f_{In} = 250 MHz		I	-38			-36			dBc

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ELECTRICAL SPECIFICATIONS

$T_J = T_C = T_A = +25$ °C , V_{EE}=-5.2 V, V_{RB}=-2.00 V, V_{RM}=-1.0 V, V_{RT}=0.00 V, f_{clk}=500 MHz, Duty Cycle=50%, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7750A MIN	SPT7750A TYP	SPT7750A MAX	SPT7750B MIN	SPT7750B TYP	SPT7750B MAX	UNITS
Dynamic Performance									
Signal-to-Noise and Distortion									
f_{in} = 50 MHz		I	43			41			dB
f_{in} = 250 MHz		I	37			35			dB
Spurious Free Dynamic Range									
f_{in} = 50 MHz		I	49			44			dB
f_{in} = 250 MHz		I	41			36			dB
Digital Inputs									
Input High Voltage									
(CLK, NCLK)		I	-1.1	-0.7		-1.1	-0.7		V
Input Low Voltage									
(CLK, NCLK)		I		-1.8	-1.5		-1.8	-1.5	V
Clock Pulse Width High (t_{PWH})		I	1.0	0.67		1.0	0.67		ns
Clock Pulse Width Low (t_{PWL})		I	1.0	0.67		1.0	0.67		ns
Clock Synchronous									
Input Currents		V		2		2			µA
Digital Outputs									
Logic "1" Voltage		I	-1.1	-0.9		-1.1	-0.9		V
Logic "0" Voltage		I		-1.8	-1.5		-1.8	-1.5	V
Power Supply Requirements									
Voltage V_{EE}		IV	-4.95	-5.2	-5.45	-4.95	-5.2	-5.45	V
Current I_{EE}		I		1.05	1.2		1.05	1.2	A
Power Dissipation		I		5.5	6.25		5.5	6.25	W

Typical Thermal Impedances: θ_{JC} (PGA) = 5°c/w; θ_{JC} (MQUAD) = 4°c/w

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests; therefore, $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

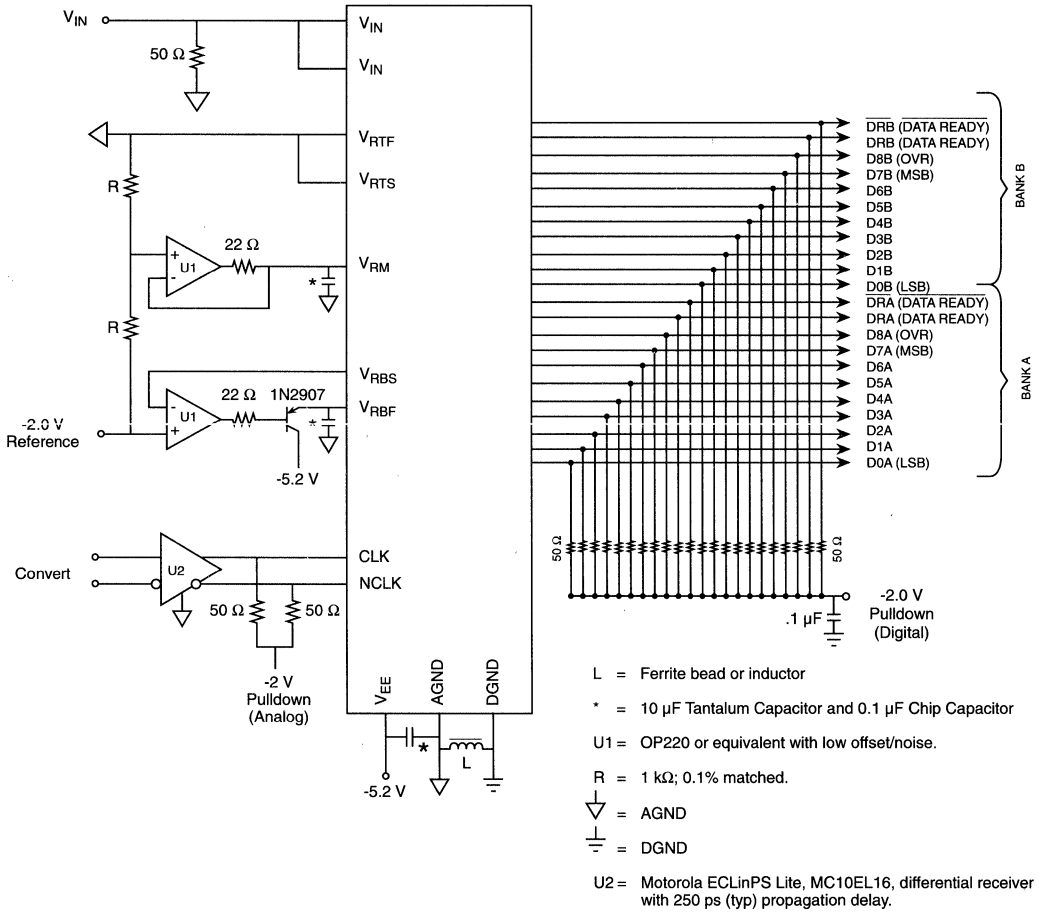
GENERAL DESCRIPTION

The SPT7750 is one of the fastest monolithic 8-bit parallel flash A/D converters available today. The nominal conversion rate is 500 MSPS and the analog bandwidth is in excess of 900 MHz. A major advance over previous flash converters is the inclusion of 256 input preamplifiers between the reference ladder and input comparators (see block diagram). This not only reduces clock transient kickback to the input and reference ladder due to a low AC beta but also reduces the effect of the dynamic state of the input signal on the latching characteristics of the input comparators. The preamplifiers act as buffers and stabilize the input capacitance so that it remains constant over different input voltage and frequency ranges and therefore makes the part easier to drive than previous flash converters. The preamplifiers also add a gain of two to the input signal so that each comparator has a wider overdrive or threshold range to "trip" into or out of the active state. This gain reduces metastable states that can cause errors at the output.

The SPT7750 has true differential analog and digital data paths from the preamplifiers to the output buffers (Current Mode Logic) for reducing potential missing codes while rejecting common mode noise.

Signature errors are also reduced by careful layout of the analog circuitry. The output drive capability of the device can provide full ECL swings into 50 Ω loads.

Figure 1 - SPT7750 Typical Interface Circuit



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TYPICAL INTERFACE CIRCUIT

The circuit in figure 1 is intended to show the most elaborate method of achieving the least error by correcting for integral linearity, input induced distortion and power supply/ground noise. This is achieved by the use of external reference ladder tap connections, input buffer and supply decoupling. Please contact the factory for the SPT7750 evaluation board applications note that contains more details on interfacing the SPT7750. The function of each pin and external connections to other components is as follows:

V_{EE}, AGND, DGND

V_{EE} is the supply pin with AGND as ground for the device. The power supply pins should be bypassed as close to the device as possible with at least a .01 µF ceramic capacitor. A 1 µF tantalum can also be used for low frequency suppression. DGND is the ground for the ECL outputs and is to be referenced to the output pulldown voltage and appropriately bypassed as shown in figure 5.

V_{IN} (ANALOG INPUT)

There are two analog input pins that are tied to the same point internally. Either one may be used as an analog input sense and the other for input force. This is convenient for testing the source signal to see if there is sufficient drive capability. The pins can also be tied together and driven by the same source. The SPT7750 is superior to similar devices due to a preamplifier stage before the comparators. This makes the device easier to drive because it has constant capacitance and induces less slew rate distortion.

CLK, $\overline{CLK}$ (CLOCK INPUTS)

The clock inputs are designed to be driven differentially with ECL levels. The duty cycle of the clock should be kept at 50% to avoid causing larger second harmonics. If this is not important to the intended application, then duty cycles other than 50% may be used.

D0 TO D8, DR, NDR, (A AND B)

The digital outputs can drive 50 Ω to ECL levels when pulled down to -2 V. When pulled down to -5.2 V, the outputs can drive 130 Ω to 1 kΩ loads. All digital outputs are grey code with the coding as shown in table 1.

V_{RBF}, V_{RBS}, V_{RTF}, V_{RTS}, V_{RM} (REFERENCE INPUTS)

There are two reference inputs and one external reference voltage tap. These are -2 V (V_{RB} force and sense), mid-tap (V_{RM}) and AGND (V_{RT} force and sense). The reference pins and tap can be driven by op amps as shown in figure 1 or V_{RM} may be bypassed for limited temperature operation. These voltage inputs can be bypassed to AGND for further noise suppression if so desired.

Table I - Output Coding

V_{IN}	D8	D7.....DO
0 V	1	10000000
		10000001
		10000011
		•
		•
		•
		10100001
-0.5 V	0	10100000
		11100000
		•
		•
		•
		11000001
-1.0 V	0	11000000
		01000000
		•
		•
		•
		01100001
-1.5 V	0	01100000
		00100000
		•
		•
		•
		00000011
		00000001
-2.0 V	0	00000000

THERMAL MANAGEMENT

The typical thermal impedances have been measured for each package type:

ΘCA (PGA) = 13 °C/W in still air with no heat sink
ΘCA (MQUAD) = 17 °C/W in still air with no heat sink

We highly recommend that a heat sink be used for this device with adequate air flow to ensure rated performance of the device. We have found that a Thermalloy 17846 heat sink with a minimum air flow of 1 meter/second (200 linear feet per minute) provides adequate thermal performance under laboratory tests. Application specific conditions should be taken into account to ensure that the device is properly heat sinked.

OPERATION

The SPT7750 has 256 preamp/comparator pairs which are each supplied with the voltage from V_{RT} to V_{RB} divided equally by the resistive ladder as shown in the block diagram. This voltage is applied to the positive input of each preamplifier/comparator pair. An analog input voltage applied at V_{IN} is connected to the negative inputs of each preamplifier/comparator pair. The comparators are then clocked through each one's individual clock buffer. When the CLK pin is in the low state, the master or input stage of the comparators compare the analog input voltage to the respective reference voltage. When the CLK pin changes from low to high the comparators are latched to the state prior to the clock transition and output logic codes in sequence from the top comparators, closest to V_{RT} (0 V), down to the point where the magnitude of the input signal changes sign (thermometer code). The output of each comparator is then registered into four 64-to-6 bit decoders when the CLK is changed from high to low. At the output of the decoders is a set of four 7-bit latches which are enabled ("track") when the clock changes from high to low. From here, the output of the latches are coded into 6 LSBs from 4 columns and 4 columns are coded into 2 MSBs. Finally, 8 ECL output latches and buffers are used to drive the external loads. The conversion takes one clock cycle from the input to the data outputs.

Figure 2 - Timing Diagram

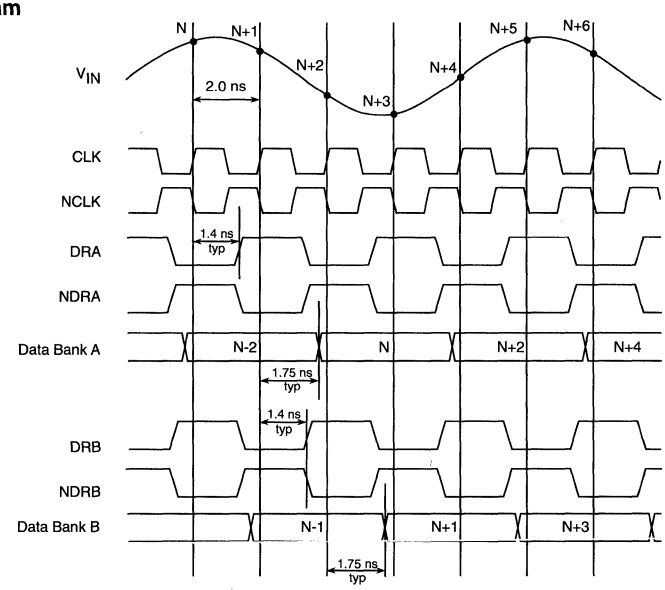
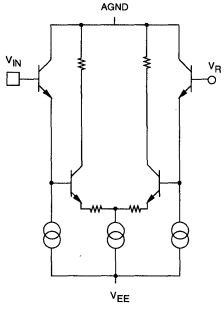
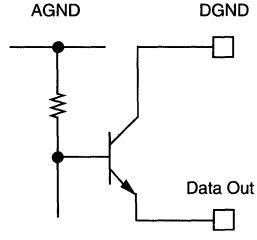


Figure 3 - Subcircuit Schematics

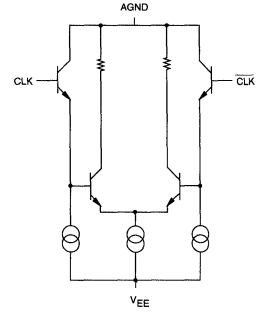
INPUT CIRCUIT



OUTPUT CIRCUIT



CLOCK INPUT



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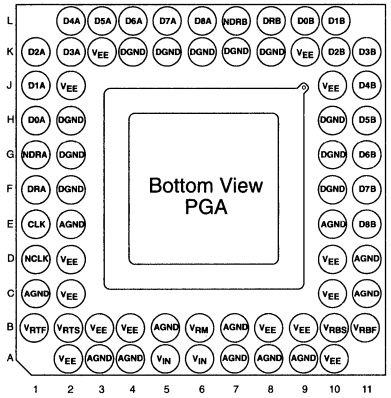
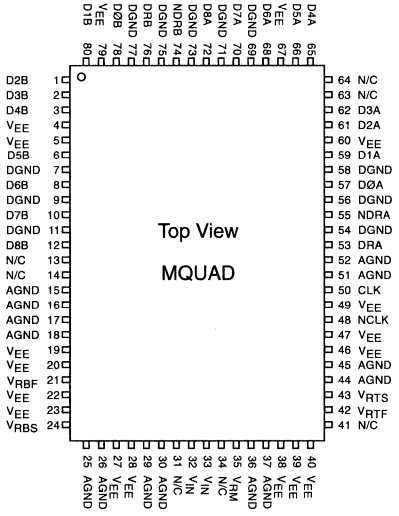
PIN ASSIGNMENT SPT7750





PIN FUNCTIONS SPT7750

V_{EE}	Negative Supply Nominally -5.2 V
AGND	Analog Ground
V_{RTF}	Reference Voltage Force Top,
	Nominally 0 V
V_{RTS}	Reference Voltage Sense Top
V_{RM}	Reference Voltage Middle, Nominally -1 V
V_{RBF}	Reference Voltage Force Bottom,
	Nominally -2 V
V_{RBS}	Reference Voltage Sense Bottom
V_{IN}	Analog Input Voltage, Can Be Either
	Voltage or Sense
DGND	Digital Ground
D0_D7A	Data Output Bank A
D0_D7B	Data Output Bank B
DRA	Data Ready Bank A
NDRA	Not Data Ready Bank A
DRB	Data Ready Bank B
NDRB	Not Data Ready Bank B
D8A	Overrange Output Bank A
D8B	Overrange Output Bank B
CLK	Clock Input
NCLK	Clock Input

3

LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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SIGNAL PROCESSING TECHNOLOGIES

SPT7755

8-BIT, 750 MSPS FLASH A/D CONVERTER

FEATURES

- 1:2 Demuxed ECL Compatible Outputs
- Wide Input Bandwidth - 900 MHz
- Low Input Capacitance - 15 pF (MQUAD)
- Metastable Errors Reduced to 1 LSB
- Monolithic for Low Cost
- Gray Code Output

APPLICATIONS

- Digital Oscilloscopes
- Transient Capture
- Radar, EW, ECM
- Direct RF Down-Conversion

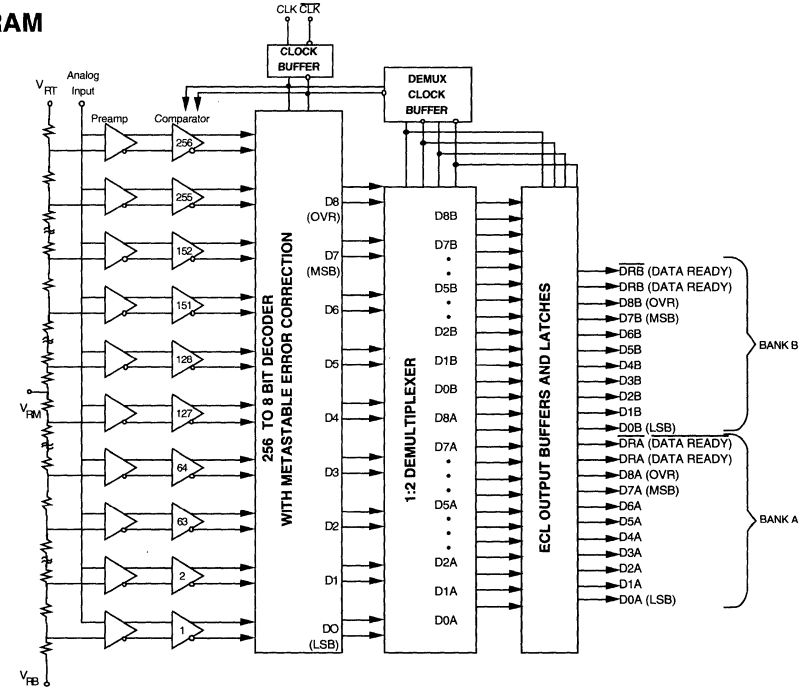
3

GENERAL DESCRIPTION

The SPT7755 is a full parallel (flash) analog-to-digital converter capable of digitizing full scale (0 to -2 V) inputs into eight-bit digital words at an update rate of 750 MSPS. The ECL-compatible outputs are demultiplexed into two separate output banks, each with differential data ready outputs to ease the task of data capture. The SPT7755's wide input bandwidth and low capacitance eliminate the need for external track-and-hold amplifiers for most applications. A proprietary decoding scheme reduces metastable errors to the 1 LSB level. The SPT7755 operates from a single -5.2 V supply, with a nominal power dissipation of 5.5 W.

The SPT7755 is available in a 68L PGA and an 80L surface-mount MQUAD package over the industrial temperature range of -25 to + 85 °C. Contact the factory for availability of die and /883 versions.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages
Negative Supply Voltage (V_{EE} TO GND) ..... -7.0 to +0.5 V
Ground Voltage Differential ..... -0.5 to +0.5 V

Input Voltage
Analog Input Voltage ..... +0.5 V to V_{EE}
Reference Input Voltage ..... +0.5 V to V_{EE}
Digital Input Voltage ..... +0.5 V to V_{EE}
Reference Current V_{RT} to V_{RB} ..... 35 mA

Output
Digital Output Current ..... 0 to -28 mA

Temperature
Operating Temperature, ambient ..... -25 to +85 °C
case ..... +125 °C
junction ..... +150 °C
Lead Temperature, (soldering 10 seconds). ..... +300 °C
Storage Temperature ..... -65 to +150 °C

Notes: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

$T_J = T_C = T_A = +25$ °C , V_{EE}=-5.2 V, V_{RB}=-2.00 V, V_{RM}=-1.0 V, V_{RT}=0.00 V, f_{clk}=750 MHz, Duty Cycle=50%, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7755A MIN	SPT7755A TYP	SPT7755A MAX	SPT7755B MIN	SPT7755B TYP	SPT7755B MAX	UNITS
Resolution				8			8		Bits
DC Accuracy (+25 °C)									
Integral Nonlinearity	f_{CLK} = 100 kHz	I	-1.0		+1.0	-1.5		+1.5	LSB
Differential Nonlinearity	f_{CLK} = 100 kHz	I	-0.85		+0.95	-0.95		+1.5	LSB
No Missing Codes				Guaranteed			Guaranteed		
Analog Input									
Input Voltage Range		I	V_{RB}		V_{RT}	V_{RB}		V_{RT}	V
Input Bias Current	V_{IN}=0 V	I		.75	2.0		.75	2.0	mA
Input Resistance		V		15			15		kΩ
Input Capacitance		V							
MQuad	Over Full Input Range	V		15			15		pF
PGA	Over Full Input Range	V		30			30		pF
Input Bandwidth									
Small Signal		V		900			900		MHz
Large Signal		V		500			500		MHz
Offset Error V_{RT}		IV	-30		+30	-30		+30	mV
Offset Error V_{RB}		IV	-30		+30	-30		+30	mV
Input Slew Rate		V		5			5		V/ns
Reference Input									
Ladder Resistance		I	60	80		60	80		Ω
Reference Bandwidth		V		30			30		MHz
Timing Characteristics									
Maximum Sample Rate		I	750			750			MHz
Aperture Jitter		V		2			2		ps
Acquisition Time		V		250			250		ps
CLK to DATA READY Delay		IV	0.9	1.4	1.9	0.9	1.4	1.9	ns
Clock to Data Delay		IV	1.25	1.75	2.25	1.25	1.75	2.25	ns
Dynamic Performance									
Signal-To-Noise Ratio (without Harmonics)									
f_{In} = 50 MHz		I	46			44			dB
f_{In} = 250 MHz		I	44			42			dB
Total Harmonic Distortion									
f_{In} = 50 MHz		I	-45			-43			dBc
f_{In} = 250 MHz		I	-37			-35			dBc

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Dynamic Performance									
Signal-to-Noise and Distortion									
f_{In} = 50 MHz		I	43			41			dB
f_{In} = 250 MHz		I	36			34			dB
Spurious Free Dynamic Range									
f_{In} = 50 MHz		I	48			44			dB
f_{In} = 250 MHz		I	40			36			dB
Digital Inputs									
Input High Voltage									
(CLK, NCLK)		I	-1.1	-0.7		-1.1	-0.7		V
Input Low Voltage									
(CLK, NCLK)		I		-1.8	-1.5		-1.8	-1.5	V
Clock Pulse Width High (t_{PWH})		I	0.67	0.5		0.67	0.5		ns
Clock Pulse Width Low (t_{PWL})		I	0.67	0.5		0.67	0.5		ns
Clock Synchronous									
Input Currents		V		2		2			µA
Digital Outputs									
Logic "1" Voltage		I	-1.1	-0.9		-1.1	-0.9		V
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Power Supply Requirements									
Voltage V_{EE}		IV	-4.95	-5.2	-5.45	-4.95	-5.2	-5.45	V
Current I_{EE}		I		1.05	1.2		1.05	1.2	A
Power Dissipation		I		5.5	6.25		5.5	6.25	W

Typical Thermal Impedances: θ_{JC} (PGA) = 5°c/w; θ_{JC} (MQUAD) = 4°c/w

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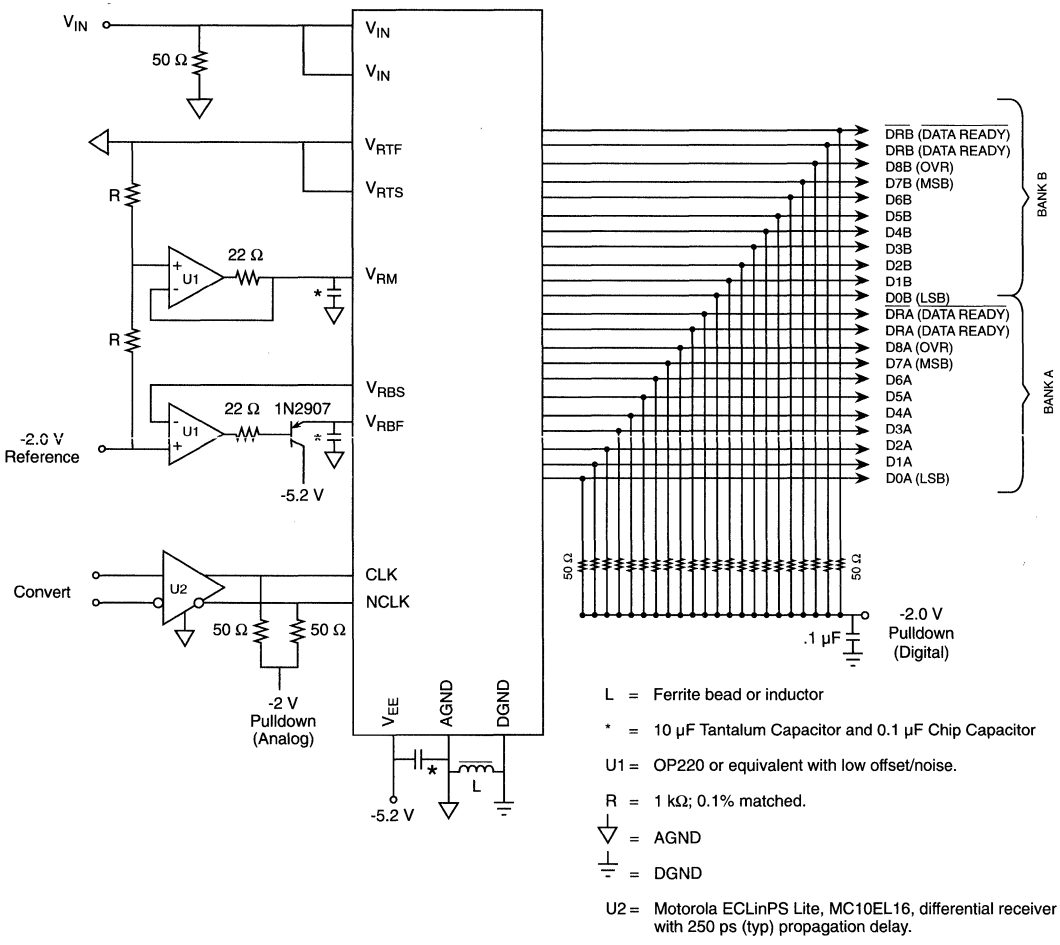

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		10000011
		•
		•
		•
		10100001
-0.5 V	0	10100000
		11100000
		•
		•
		•
		11000001
-1.0 V	0	11000000
		01000000
		•
		•
		•
		01100001
-1.5 V	0	01100000
		00100000
		•
		•
		•
		00000011
		00000001
-2.0 V	0	00000000

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The SPT7755 has 256 preamp/comparator pairs which are each supplied with the voltage from V_{RT} to V_{RB} divided equally by the resistive ladder as shown in the block diagram. This voltage is applied to the positive input of each preamplifier/comparator pair. An analog input voltage applied at V_{IN} is connected to the negative inputs of each preamplifier/comparator pair. The comparators are then clocked through each one's individual clock buffer. When the CLK pin is in the low state, the master or input stage of the comparators compare the analog input voltage to the respective reference voltage. When the CLK pin changes from low to high the comparators are latched to the state prior to the clock transition and output logic codes in sequence from the top comparators, closest to V_{RT} (0 V), down to the point where the magnitude of the input signal changes sign (thermometer code). The output of each comparator is then registered into four 64-to-6 bit decoders when the CLK is changed from high to low. At the output of the decoders is a set of four 7-bit latches which are enabled ("track") when the clock changes from high to low. From here, the output of the latches are coded into 6 LSBs from 4 columns and 4 columns are coded into 2 MSBs. Finally, 8 ECL output latches and buffers are used to drive the external loads. The conversion takes one clock cycle from the input to the data outputs.

Figure 2 - Timing Diagram

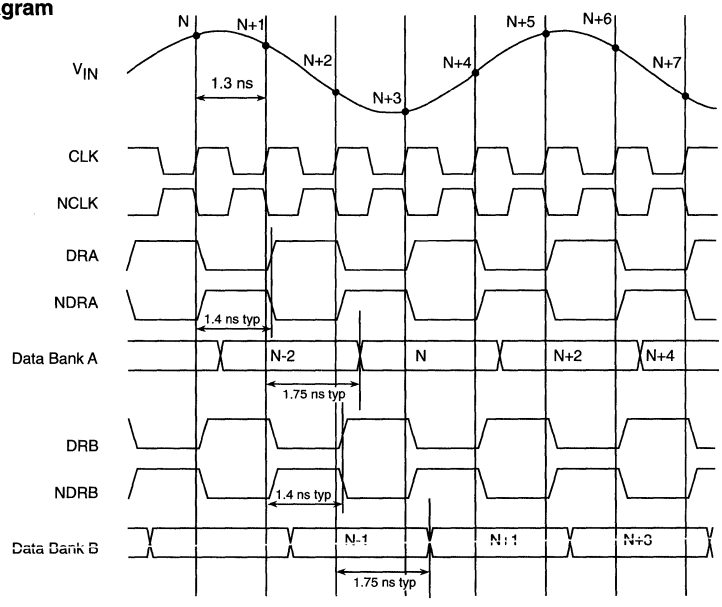
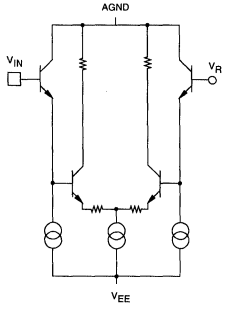
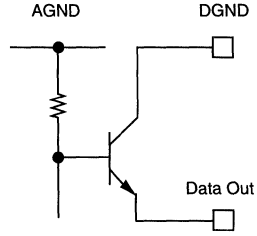


Figure 3 - Subcircuit Schematics

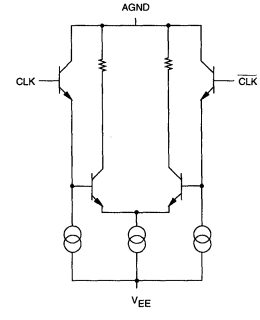
INPUT CIRCUIT



OUTPUT CIRCUIT



CLOCK INPUT



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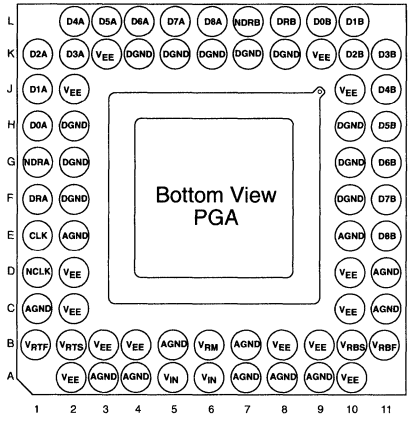
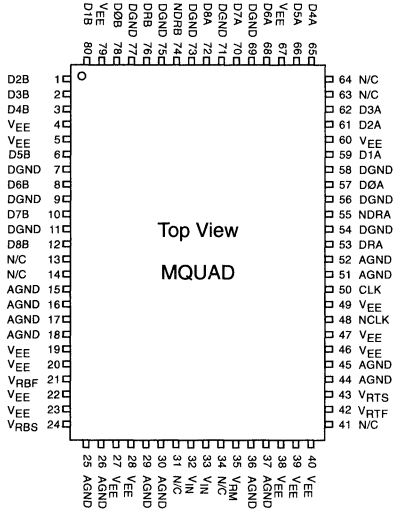
PIN ASSIGNMENT SPT7755





PIN FUNCTIONS SPT7755

V_{EE}	Negative Supply Nominally -5.2 V
AGND	Analog Ground
V_{RTF}	Reference Voltage Force Top, Nominally 0 V
V_{RTS}	Reference Voltage Sense Top
V_{RM}	Reference Voltage Middle, Nominally -1 V
V_{RBF}	Reference Voltage Force Bottom, Nominally -2 V
V_{RBS}	Reference Voltage Sense Bottom
V_{IN}	Analog Input Voltage, Can Be Either Voltage or Sense
DGND	Digital Ground
D0_D7A	Data Output Bank A
D0_D7B	Data Output Bank B
DRA	Data Ready Bank A
NDRA	Not Data Ready Bank A
DRB	Data Ready Bank B
NDRB	Not Data Ready Bank B
D8A	Overrange Output Bank A
D8B	Overrange Output Bank B
CLK	Clock Input
NCLK	Clock Input

LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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SIGNAL PROCESSING TECHNOLOGIES

SPT7760

8-BIT, 1000 MSPS FLASH A/D CONVERTER

FEATURES

- 1:2 Demuxed ECL Compatible Outputs
- Wide Input Bandwidth - 900 MHz
- Low Input Capacitance - 15 pF (MQUAD)
- Metastable Errors Reduced to 1 LSB
- Monolithic for Low Cost
- Gray Code Output

APPLICATIONS

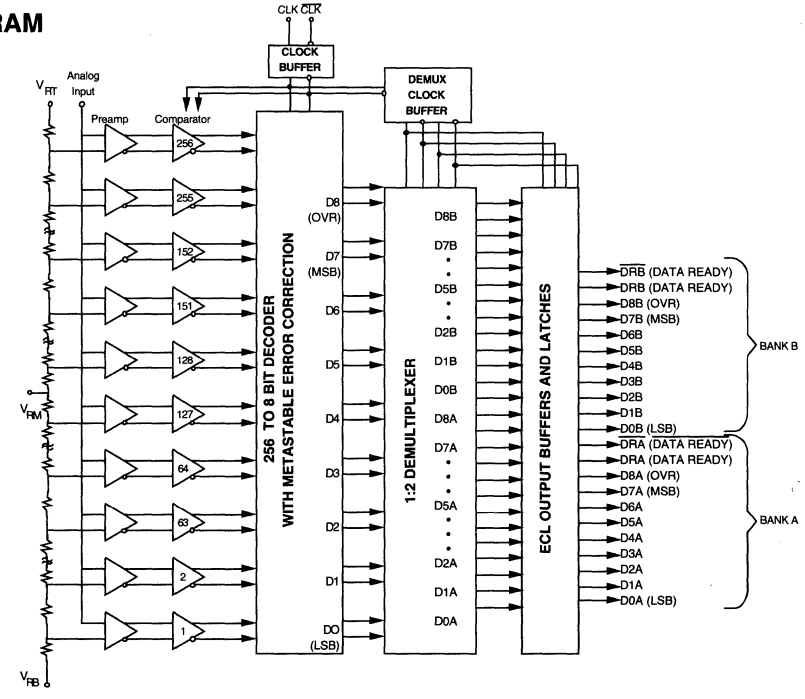
- Digital Oscilloscopes
- Transient Capture
- Radar, EW, ECM
- Direct RF Down-Conversion

GENERAL DESCRIPTION

The SPT7760 is a full parallel (flash) analog-to-digital converter capable of digitizing full scale (0 to -2 V) inputs into eight-bit digital words at an update rate of 1000 MSPS. The ECL-compatible outputs are demultiplexed into two separate output banks, each with differential data ready outputs to ease the task of data capture. The SPT7760's wide input bandwidth and low capacitance eliminate the need for external track-and-hold amplifiers for most applications. A proprietary decoding scheme reduces metastable errors to the 1 LSB level. The SPT7760 operates from a single -5.2 V supply, with a nominal power dissipation of 5.5 W.

The SPT7760 is available in a 68L PGA and an 80L surface-mount MQUAD package over the industrial temperature range of -25 to + 85 °C. Contact the factory for availability of die and /883 versions.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages
- Negative Supply Voltage (V_{EE} TO GND) ..... -7.0 to +0.5 V
- Ground Voltage Differential ..... -0.5 to +0.5 V

Input Voltage
- Analog Input Voltage ..... +0.5 V to V_{EE}
- Reference Input Voltage ..... +0.5 V to V_{EE}
- Digital Input Voltage ..... +0.5 V to V_{EE}
- Reference Current V_{RT} to V_{RB} ..... 35 mA

Output
- Digital Output Current ..... 0 to -28 mA

Temperature
- Operating Temperature, ambient ..... -25 to +85 °C
- case ..... +125 °C
- junction ..... +150 °C
- Lead Temperature, (soldering 10 seconds). ..... +300 °C
- Storage Temperature ..... -65 to +150 °C

Notes: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

$T_J = T_C = T_A$ = +25 °C , V_{EE}=-5.2 V, V_{RB}=-2.00 V, V_{RM}=-1.0 V, V_{RT}=0.00 V, f_{clk}=1000 MHz, Duty Cycle=50%, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7760A MIN	SPT7760A TYP	SPT7760A MAX	SPT7760B MIN	SPT7760B TYP	SPT7760B MAX	UNITS
Resolution				8			8		Bits
DC Accuracy (+25 °C)									
Integral Nonlinearity	f_{CLK} = 100 kHz	I	-1.0		+1.0	-1.5		+1.5	LSB
Differential Nonlinearity	f_{CLK} = 100 kHz	I	-0.85		+0.95	-0.95		+1.5	LSB
No Missing Codes				Guaranteed			Guaranteed		
Analog Input									
Input Voltage Range		I	V_{RB}		V_{RT}	V_{RB}		V_{RT}	V
Input Bias Current	V_{IN}=0 V	I		.75	2.0		.75	2.0	mA
Input Resistance		V		15			15		kΩ
Input Capacitance		V							
MQuad	Over Full Input Range	V		15			15		pF
PGA	Over Full Input Range	V		30			30		pF
Input Bandwidth									
Small Signal		V		900			900		MHz
Large Signal		V		500			500		MHz
Offset Error V_{RT}		I	-30		+30	-30		+30	mV
Offset Error V_{RB}		I	-30		+30	-30		+30	mV
Input Slew Rate		V		5			5		V/ns
Reference Input									
Ladder Resistance		I	60	80		60	80		Ω
Reference Bandwidth		V		30			30		MHz
Timing Characteristics									
Maximum Sample Rate		I	1,000			1,000			MHz
Aperture Jitter		V		2			2		ps
Acquisition Time		V		250			250		ps
CLK to DATA READY Delay		IV	0.9	1.4	1.9	0.9	1.4	1.9	ns
Clock to Data Delay		IV	1.25	1.75	2.25	1.25	1.75	2.25	ns
Dynamic Performance									
Signal-To-Noise Ratio (without Harmonics)									
f_{In} = 50 MHz		I	45			43			dB
f_{In} = 250 MHz		I	43			41			dB
Total Harmonic Distortion									
f_{In} = 50 MHz		I	-44			-42			dBc
f_{In} = 250 MHz		I	-36			-34			dBc

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ELECTRICAL SPECIFICATIONS

$T_J = T_C = T_A$ = +25 °C , V_{EE}=-5.2 V, V_{RB}=-2.00 V, V_{RM}=-1.0 V, V_{RT}=0.00 V, f_{clk}=1000 MHz, Duty Cycle=50%, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7760A MIN	SPT7760A TYP	SPT7760A MAX	SPT7760B MIN	SPT7760B TYP	SPT7760B MAX	UNITS
Dynamic Performance									
Signal-to-Noise and Distortion									
f_{in} = 50 MHz		I	42			40			dB
f_{in} = 250 MHz		I	35			33			dB
Spurious Free Dynamic Range									
f_{in} = 50 MHz		I	47			43			dB
f_{in} = 250 MHz		I	39			35			dB
Digital Inputs									
Input High Voltage									
(CLK, NCLK)		I	-1.1	-0.7		-1.1	-0.7		V
Input Low Voltage									
(CLK, NCLK)		I		-1.8	-1.5		-1.8	-1.5	V
Clock Pulse Width High (t_{PWH})		I	0.5	0.4		0.5	0.4		ns
Clock Pulse Width Low (t_{PWL})		I	0.5	0.4		0.5	0.4		ns
Clock Synchronous									
Input Currents		V		2		2			µA
Digital Outputs									
Logic "1" Voltage		I	-1.1	-0.9		-1.1	-0.9		V
Logic "0" Voltage		I		-1.8	-1.5		-1.8	-1.5	V
Rise Time	20% to 80%	V		TBD			TBD		ps
Fall Time	20% to 80%	V		TBD			TBD		ps
Power Supply Requirements									
Voltage V_{EE}		IV	-4.95	-5.2	-5.45	-4.95	-5.2	-5.45	V
Current I_{EE}		I		1.05	1.2		1.05	1.2	A
Power Dissipation		I		5.5	6.25		5.5	6.25	W

Typical Thermal Impedances: θ_{JC} (PGA) = 5°c/w; θ_{JC} (MQUAD) = 4°c/w

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests; therefore, $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

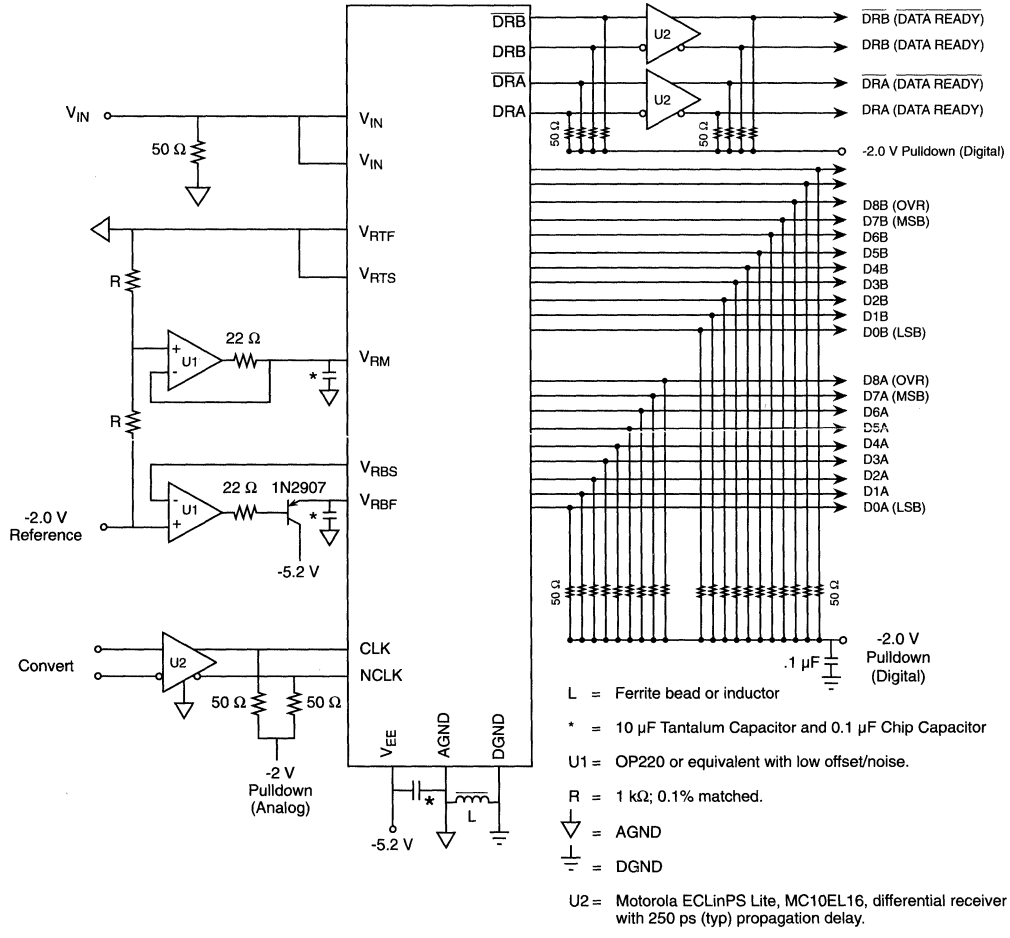
GENERAL DESCRIPTION

The SPT7760 is the fastest monolithic 8-bit parallel flash A/D converter available today. The nominal conversion rate is 1,000 MSPS and the analog bandwidth is in excess of 900 MHz. A major advance over previous flash converters is the inclusion of 256 input preamplifiers between the reference ladder and input comparators (see block diagram). This not only reduces clock transient kickback to the input and reference ladder due to a low AC beta but also reduces the effect of the dynamic state of the input signal on the latching characteristics of the input comparators. The preamplifiers act as buffers and stabilize the input capacitance so that it remains constant over different input voltage and frequency ranges and therefore makes the part easier to drive than previous flash converters. The preamplifiers also add a gain of two to the input signal so that each comparator has a wider overdrive or threshold range to "trip" into or out of the active state. This gain reduces metastable states that can cause errors at the output.

The SPT7760 has true differential analog and digital data paths from the preamplifiers to the output buffers (Current Mode Logic) for reducing potential missing codes while rejecting common mode noise.

Signature errors are also reduced by careful layout of the analog circuitry. The output drive capability of the device can provide full ECL swings into 50 Ω loads.

Figure 1 - SPT7760 Typical Interface Circuit



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TYPICAL INTERFACE CIRCUIT

The circuit in figure 1 is intended to show the most elaborate method of achieving the least error by correcting for integral linearity, input induced distortion and power supply/ground noise. This is achieved by the use of external reference ladder tap connections, input buffer and supply decoupling. Please contact the factory for the SPT7760 evaluation board applications note that contains more details on interfacing the SPT7760. The function of each pin and external connections to other components is as follows:

V_{EE}, AGND, DGND

V_{EE} is the supply pin with AGND as ground for the device. The power supply pins should be bypassed as close to the device as possible with at least a .01 µF ceramic capacitor. A 1 µF tantalum can also be used for low frequency suppression. DGND is the ground for the ECL outputs and is to be referenced to the output pulldown voltage and appropriately bypassed as shown in figure 5.

V_{IN} (ANALOG INPUT)

There are two analog input pins that are tied to the same point internally. Either one may be used as an analog input sense and the other for input force. This is convenient for testing the source signal to see if there is sufficient drive capability. The pins can also be tied together and driven by the same source. The SPT7760 is superior to similar devices due to a preamplifier stage before the comparators. This makes the device easier to drive because it has constant capacitance and induces less slew rate distortion.

CLK, $\overline{CLK}$ (CLOCK INPUTS)

The clock inputs are designed to be driven differentially with ECL levels. The duty cycle of the clock should be kept at 50% to avoid causing larger second harmonics. If this is not important to the intended application, then duty cycles other than 50% may be used.

D0 TO D8, DR, NDR (A AND B)

The digital outputs can drive 50 Ω to ECL levels when pulled down to -2 V. When pulled down to -5.2 V, the outputs can drive 130 Ω to 1 kΩ loads. All digital outputs are grey code with the coding as shown in table 1. SPT recommends using differential receivers on the outputs of the data ready lines to ensure the proper output rise and fall times.

V_{RBF}, V_{RBS}, V_{RTF}, V_{RTS}, V_{RM} (REFERENCE INPUTS)

There are two reference inputs and one external reference voltage tap. These are -2 V (V_{RB} force and sense), mid-tap (V_{RM}) and AGND (V_{RT} force and sense). The reference pins and tap can be driven by op amps as shown in figure 1 or V_{RM} may be bypassed for limited temperature operation. These voltage inputs can be bypassed to AGND for further noise suppression if so desired.

Table I - Output Coding

V_{IN}	D8	D7.....DO
0 V	1	10000000
		10000001
		10000011
		•
		•
		•
		10100001
-0.5 V	0	10100000
		11100000
		•
		•
		•
		11000001
-1.0 V	0	11000000
		01000000
		•
		•
		•
		01100001
-1.5 V	0	01100000
		00100000
		•
		•
		•
		00000011
		00000001
-2.0 V	0	00000000

THERMAL MANAGEMENT

The typical thermal impedances have been measured for each package type:

ΘCA (PGA) = 13 °C/W in still air with no heat sink
ΘCA (MQUAD) = 17 °C/W in still air with no heat sink

We highly recommend that a heat sink be used for this device with adequate air flow to ensure rated performance of the device. We have found that a Thermalloy 17846 heat sink with a minimum air flow of 1 meter/second (200 linear feet per minute) provides adequate thermal performance under laboratory tests. Application specific conditions should be taken into account to ensure that the device is properly heat sinked.

OPERATION

The SPT7760 has 256 preamp/comparator pairs which are each supplied with the voltage from V_{RT} to V_{RB} divided equally by the resistive ladder as shown in the block diagram. This voltage is applied to the positive input of each preamplifier/comparator pair. An analog input voltage applied at V_{IN} is connected to the negative inputs of each preamplifier/comparator pair. The comparators are then clocked through each one's individual clock buffer. When the CLK pin is in the low state, the master or input stage of the comparators compare the analog input voltage to the respective reference voltage. When the CLK pin changes from low to high the comparators are latched to the state prior to the clock transition and output logic codes in sequence from the top comparators, closest to V_{RT} (0 V), down to the point where the magnitude of the input signal changes sign (thermometer code). The output of each comparator is then registered into four 64-to-6 bit decoders when the CLK is changed from high to low. At the output of the decoders is a set of four 7-bit latches which are enabled ("track") when the clock changes from high to low. From here, the output of the latches are coded into 6 LSBs from 4 columns and 4 columns are coded into 2 MSBs. Finally, 8 ECL output latches and buffers are used to drive the external loads. The conversion takes one clock cycle from the input to the data outputs.

Figure 2 - Timing Diagram

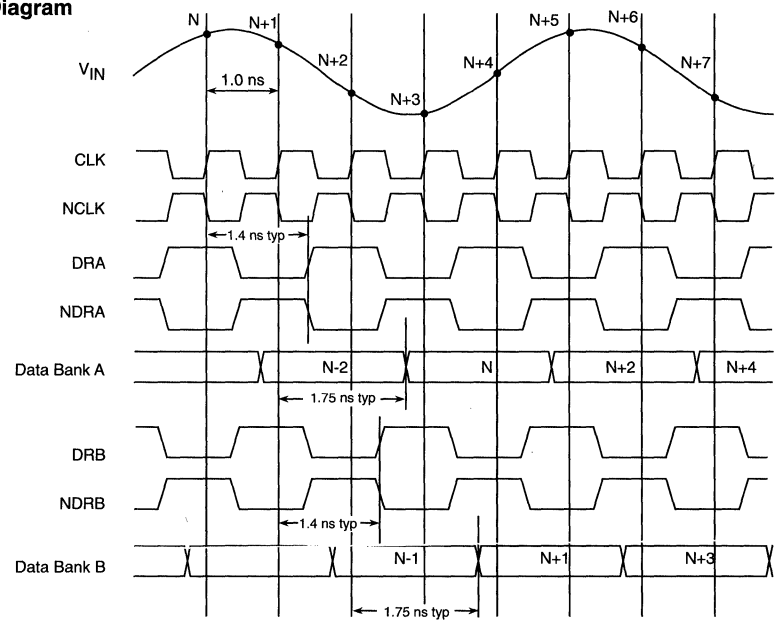
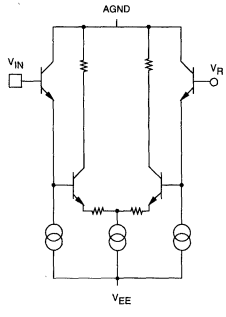
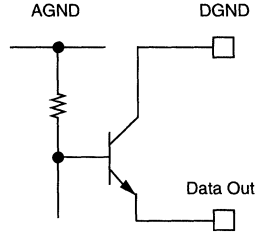


Figure 3 - Subcircuit Schematics

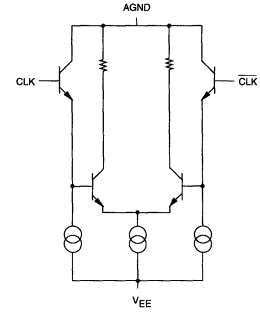
INPUT CIRCUIT



OUTPUT CIRCUIT



CLOCK INPUT



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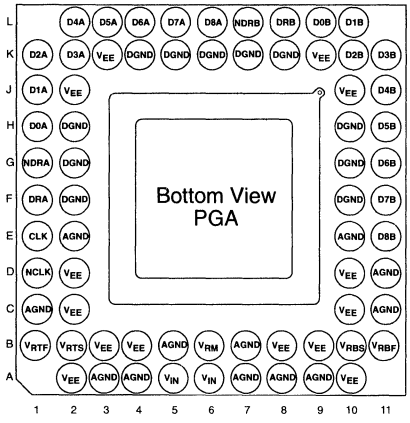
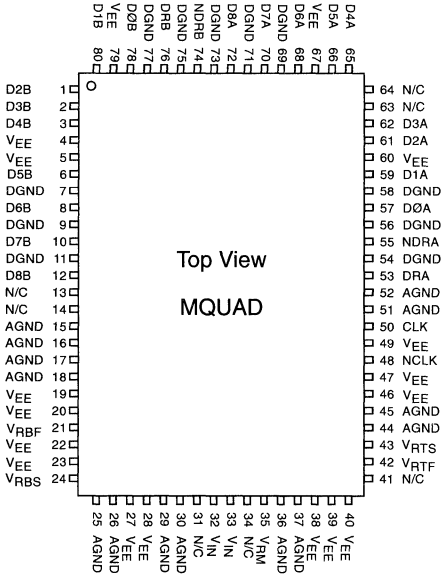
PIN ASSIGNMENTS





PIN FUNCTIONS

NAME	FUNCTION
V_{EE}	Negative Supply Nominally -5.2 V
AGND	Analog Ground
V_{RTF}	Reference Voltage Force Top, Nominally 0 V
V_{RTS}	Reference Voltage Sense Top
V_{RM}	Reference Voltage Middle, Nominally -1 V
V_{RBF}	Reference Voltage Force Bottom, Nominally -2 V
V_{RBS}	Reference Voltage Sense Bottom
V_{IN}	Analog Input Voltage, Can Be Either Voltage or Sense
DGND	Digital Ground
D0_D7A	Data Output Bank A
D0_D7B	Data Output Bank B
DRA	Data Ready Bank A
NDRA	Not Data Ready Bank A
DRB	Data Ready Bank B
NDRB	Not Data Ready Bank B
D8A	Overrange Output Bank A
D8B	Overrange Output Bank B
CLK	Clock Input
NCLK	Clock Input

LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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SIGNAL PROCESSING TECHNOLOGIES

SPT7810

10-BIT, 20 MSPS, ECL OUTPUT A/D CONVERTER

FEATURES

- Monolithic 20 MSPS Converter
- On-Chip Track/Hold
- Bipolar ±2.0 V Analog Input
- 60 dB SNR @ 1 MHz Input
- Low Power (1.3 W Typical)
- 5 pF input Capacitance
- ECL Outputs

APPLICATIONS

- Medical Imaging
- Professional Video
- Radar Receivers
- Instrumentation
- Electronic Warfare
- Digital Communications

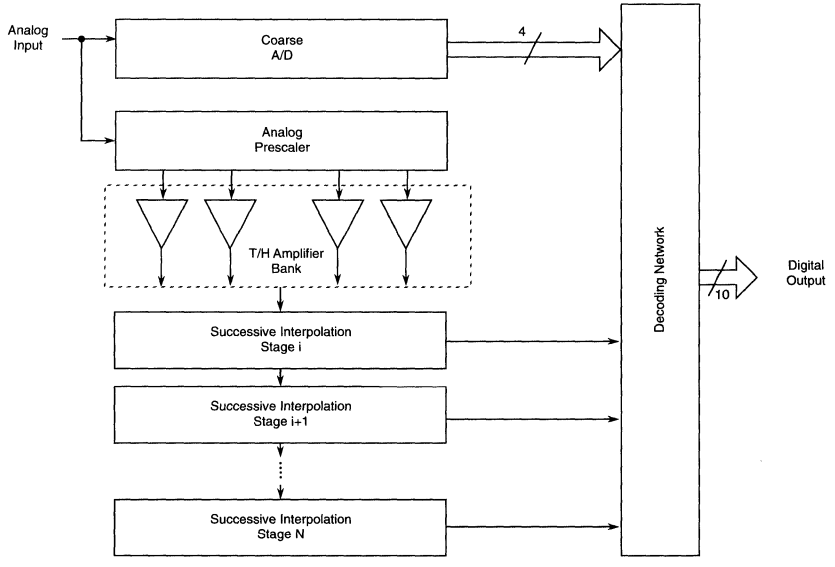
GENERAL DESCRIPTION

The SPT7810 A/D converter is a 10-bit monolithic converter capable of word rates of a minimum of 20 MSPS. On board track/hold function assures excellent dynamic performance without the need for external components. Drive requirement problems are minimized with an input capacitance of only 5 pF.

Inputs and outputs are ECL to provide a higher level of noise immunity in high speed system applications. An overrange output signal is provided to indicate overflow conditions. Output data format is straight binary. Power dissipation is very low at only 1.3 watts with power supply voltages of +5.0 and -5.2 volts. The SPT7810 also provides a wide input voltage swing of ±2.0 volts.

The SPT7810 is available in a small 28-lead ceramic side-brazed DIP, PDIP, and die form. Commercial and industrial temperature ranges are currently offered. Contact the factory for availability of military temperature range and /883 processed units.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages
- V_{CC} ..... +6 V
- V_{EE} ..... -6 V

Input Voltages
- Analog Input ..... $V_{FB} \leq V_{IN} \leq V_{FT}$
- V_{FT}, V_{FB} ..... +3.0 V, -3.0 V
- Reference Ladder Current ..... 12 mA

Output
- Digital Outputs ..... +30 to -30 mA

Temperature
- Operating Temperature ..... -25 to +85 °C
- Junction Temperature (1) ..... 175 °C
- Lead Temperature, (soldering 10 seconds) ..... 300 °C
- Storage Temperature ..... -65 to +150 °C

Note: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

$T_A=T_{min}$ - T_{max}, V_{CC}=+5.0 V, V_{EE}=-5.2 V, V_{IN}=±2.0 V, V_{SB}=-2.0 V, V_{ST}=+2.0 V, f_{clock}=20 MHz, 50% clock duty cycle, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7810A MIN	SPT7810A TYP	SPT7810A MAX	SPT7810B MIN	SPT7810B TYP	SPT7810B MAX	UNITS
Resolution			10			10			Bits
DC Accuracy (+25 °C)	± Full Scale								
Integral Nonlinearity	250 kHz Sample Rate	I		±1.0			±1.5		LSB
Differential Nonlinearity		I		±0.5			±0.75		LSB
No Missing Codes				Guaranteed			Guaranteed		
Analog Input									
Input Voltage Range		VI		±2.0			±2.0		V
Input Bias Current	V_{IN}=0 V	VI		30	60		30	60	µA
Input Resistance		VI	100	300		100	300		kΩ
Input Capacitance		V		5			5		pF
Input Bandwidth	3 dB Small Signal	V		120			120		MHz
+FS Error		V		±2.0			±2.0		LSB
-FS Error		V		±2.0			±2.0		LSB
Reference Input									
Reference Ladder Resistance		VI	500	800		500	800		Ω
Reference Ladder Tempco		V		0.8			0.8		Ω/°C
Timing Characteristics									
Maximum Conversion Rate		VI	20			20			MHz
Overvoltage Recovery Time		V		20			20		ns
Pipeline Delay (Latency)		VI			1			1	Clock Cycle
Output Delay	T_A=+25 °C	V		5			5		ns
Aperture Delay Time	T_A=+25 °C	V		1			1		ns
Aperture Jitter Time	T_A=+25 °C	V		5			5		ps-RMS
Dynamic Performance									
Effective Number of Bits									
	fin=1 MHz				9.2		8.7		Bits
	fin=3.58 MHz				8.8		8.3		Bits
	fin=10.3 MHz				7.5		7.0		Bits

[1]Typical thermal impedances: 28L sidebrazed DIP. θ_{ja} = 50 °C/W,
28L plastic DIP θ_{ja} = 50 °C/W.

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ELECTRICAL SPECIFICATIONS

$T_A=T_{min}$ - T_{max}, V_{CC}=+5.0 V, V_{EE}=-5.2 V, V_{IN}=±2.0 V, V_{SB}=-2.0 V, V_{ST}=+2.0 V, f_{clock}=20 MHz, 50% clock duty cycle, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7810A MIN	SPT7810A TYP	SPT7810A MAX	SPT7810B MIN	SPT7810B TYP	SPT7810B MAX	UNITS
Dynamic Performance									
Signal-To-Noise Ratio (without Harmonics)									
fin=1 MHz	+25 °C	I	57	60		54	57		dB
	$T_A=T_{min}$ - T_{max}	IV	55	58		52	55		dB
fin=3.58 MHz	+25 °C	I	56	58		53	55		dB
	$T_A=T_{min}$ - T_{max}	IV	54	56		51	53		dB
fin=10.3 MHz	+25 °C	I	50	53		47	49		dB
	$T_A=T_{min}$ - T_{max}	IV	47	50		44	46		dB
Harmonic Distortion									
fin=1 MHz	+25 °C	I	57	60		54	57		dB
	$T_A=T_{min}$ - T_{max}	IV	54	57		51	54		dB
fin=3.58 MHz	+25 °C	I	56	58		53	55		dB
	$T_A=T_{min}$ - T_{max}	IV	53	55		50	52		dB
fin=10.3 MHz	+25 °C	I	46	48		43	45		dB
	$T_A=T_{min}$ - T_{max}	IV	45	47		42	44		dB
Signal-to-Noise and Distortion									
fin=1 MHz	+25 °C	I	55	57		52	54		dB
	$T_A=T_{min}$ - T_{max}	IV	52			49			dB
fin=3.58 MHz	+25 °C	I	54	55		51	52		dB
	$T_A=T_{min}$ - T_{max}	IV	51			48			dB
fin=10.3 MHz	+25 °C	I	44	47		41	44		dB
	$T_A=T_{min}$ - T_{max}	IV	43			40			dB
Spurious Free Dynamic Range	+25 °C, fin = 1 MHz	V		67			67		dB
Differential Phase	+25 °C, fin=3.58 & 4.35 MHz	V		0.2			0.2		Degree
Differential Gain	+25 °C, fin=3.58 & 4.35 MHz	V		0.5			0.7		%
Digital Inputs									
Logic "1" Voltage		V	-1.1			-1.1			V
Logic "0" Voltage		V			-1.5			-1.5	V
Maximum Input Current Low		VI	-500	±200	+750	-500	±200	+750	µA
Maximum Input Current High		VI	-500	±300	+750	-500	+300	+750	µA
Pulse Width Low (CLK)		IV	20			20			ns
Pulse Width High (CLK)		IV	20		300	20		300	ns
Digital Outputs									
Logic "1" Voltage	50 Ω to -2 V	VI	-1.1	-0.8		-1.1	-0.8		V
Logic "0" Voltage	50 Ω to -2 V	VI		-1.8	-1.5		-1.8	-1.5	V
Power Supply Requirements									
Voltages V_{CC}		IV	+4.75	-5.0	+5.25	+4.75	+5.0	+5.25	V
$-V_{EE}$		IV	-4.95	-5.2	-5.45	-4.95	-5.2	-5.45	V
Currents I_{CC}		VI		140	170		140	190	mA
$-I_{EE}$		VI		115	140		115	160	mA
Power Dissipation	Outputs Open	VI		1.3	1.6		1.3	1.8	W
Power Supply Rejection Ratio	(5 V ±0.25 V, -5.2 V ±2.0 V)	V		1.0			1.0		LSB

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests; therefore, $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

Figure 1A: Timing Diagram

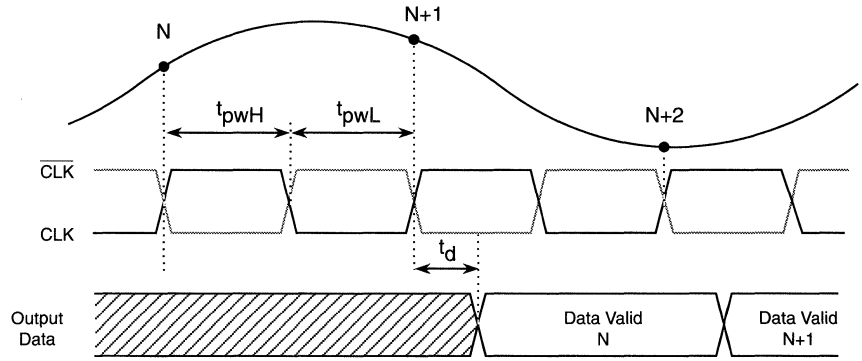

Figure 1B: Single Event Clock

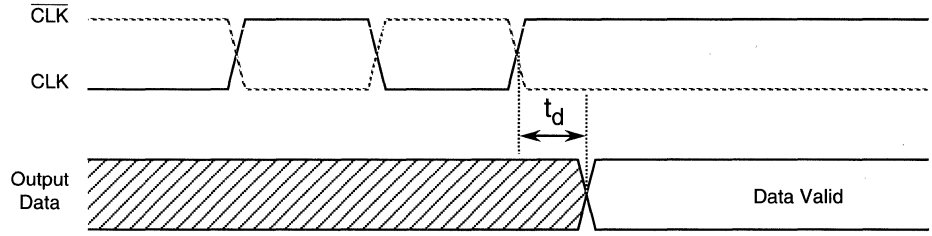

Table 1 - Timing Parameters

PARAMETERS	DESCRIPTION	MIN	TYP	MAX	UNITS
t_d	CLK to Data Valid Prop Delay	-	5		ns
t_{pwH}	CLK High Pulse Width	20	-	300	ns
t_{pwL}	CLK Low Pulse Width	20	-	-	ns

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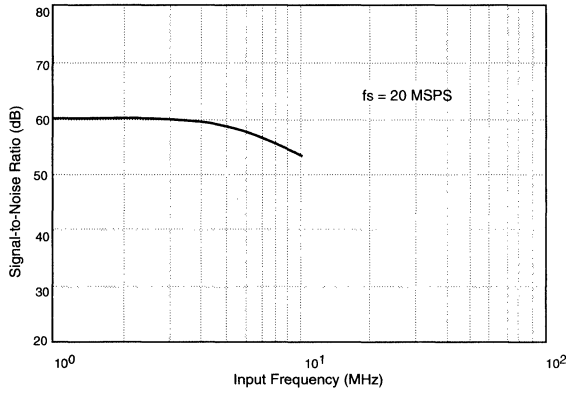
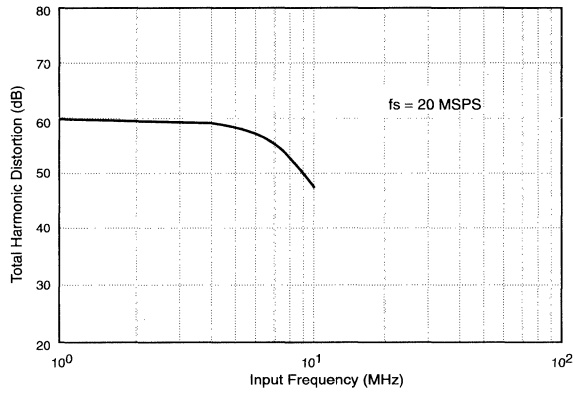
TYPICAL PERFORMANCE CHARACTERISTICS

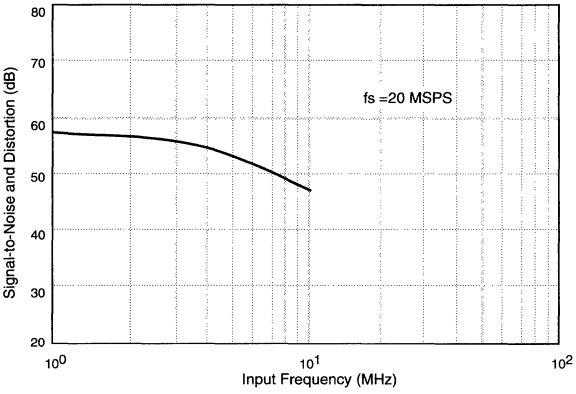
SNR vs Input Frequency



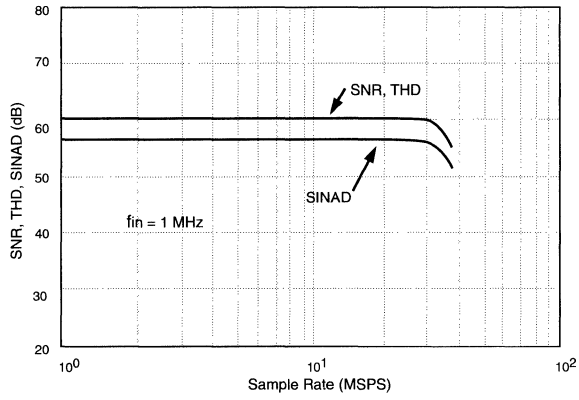
THD vs Input Frequency



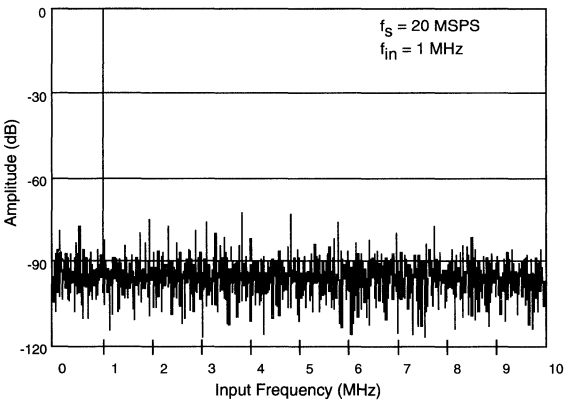
SINAD vs Input Frequency



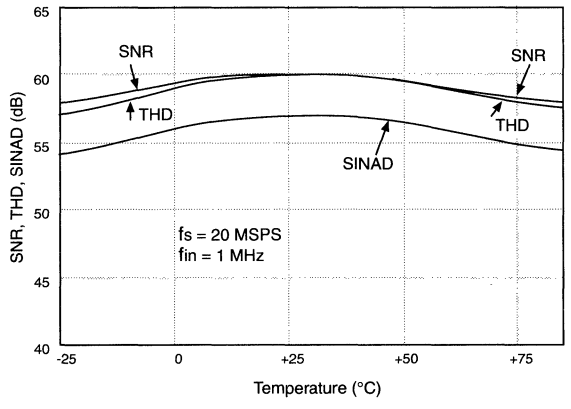
SNR, THD, SINAD vs Sample Rate



Spectral Response



SNR, THD, SINAD vs Temperature



TYPICAL INTERFACE CIRCUIT

The SPT7810 requires few external components to achieve the stated operation and performance. Figure 2 shows the typical interface requirements when using the SPT7810 in normal circuit operation.

The following section provides a description of the pin functions and outlines critical performance criteria to consider for achieving the optimal device performance.

POWER SUPPLIES AND GROUNDING

The SPT7810 requires the use of two supply voltages, V_{EE} and V_{CC}. Both supplies should be treated as analog supply sources. This means the V_{EE} and V_{CC} ground returns of the device should both be connected to the analog ground plane. All other -5.2 V requirements of the external digital logic circuit should be connected to the digital ground plane. Each power supply pin should be bypassed as closely as possible to the device with .01 µF and 10 µF capacitors as shown in figure 2.

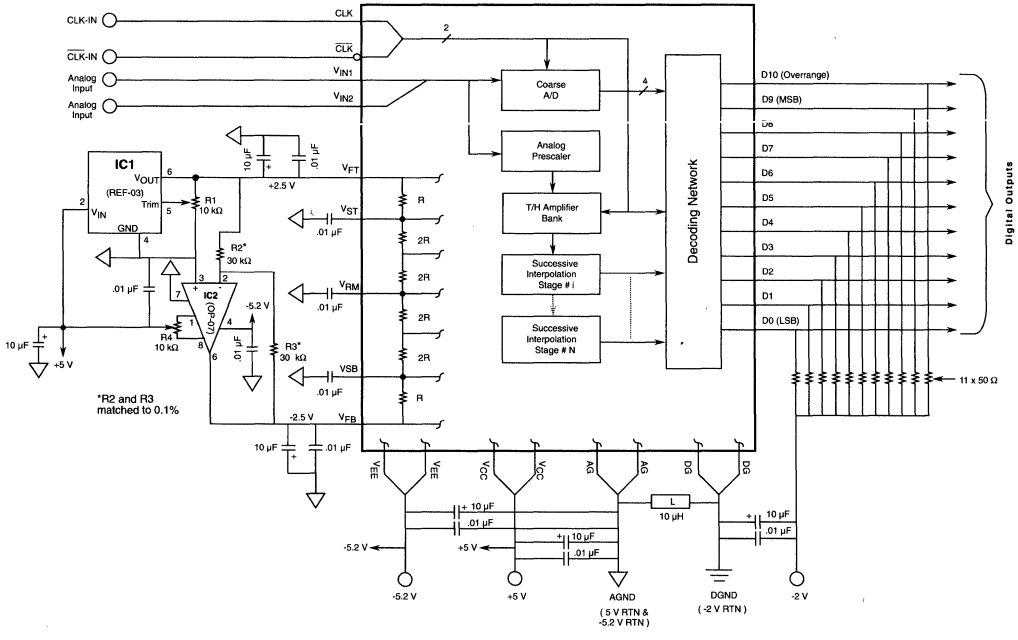
The two grounds available on the SPT7810 are AGND and DGND. DGND is used only for ECL outputs and is to be referenced to the output pulldown voltage. These grounds are not tied together internal to the device. The use of ground planes is recommended to achieve the best performance of the SPT7810. The AGND and the DGND ground planes should be separated from each other and only connected together at the device through an inductance. Doing this will minimize the ground noise pickup.

VOLTAGE REFERENCE

The SPT7810 requires the use of two voltage references: V_{FT} and V_{FB}. V_{FT} is the force for the top of the voltage reference ladder (+2.5 V typ), V_{FB} (-2.5 V typ) is the force for the bottom of the voltage reference ladder. Both voltages are applied across an internal reference ladder resistance of 800 ohms. In addition, there are 3 reference ladder taps (V_{ST},V_{RM} and V_{SB}). V_{ST} is the sense for the top of the reference ladder (+2.0 V), V_{RM} is the midpoint of the ladder (0.0 V typ) and V_{SB} is the sense for the bottom of the reference ladder (-2.0 V). The voltages seen at V_{ST} and V_{SB} are the true full scale input voltages of the device when V_{FT} and V_{FB} are driven to the recommended voltages (+2.5 V and -2.5 V typical respectively). These points should be used to monitor the actual full scale input voltage of the device and should not be driven to the expected ideal values as is commonly done with standard flash converters. When not being used, a decoupling capacitor of .01 uF connected to AGND from each tap is recommended to minimize high frequency noise injection.

An example of a reference driver circuit recommended is shown in figure 2. IC1 is REF-03, the +2.5 V reference with a

Figure 2 - Typical Interface Circuit



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tolerance of 0.6% or ± 0.015 V. The potentiometer R1 is 10 kΩ and supports a minimum adjustable range of up to 150 mV. IC2 is recommended to be an OP-07 or equivalent device. R2 and R3 must be matched to within 0.1% with good TC tracking to maintain a 0.3 LSB matching between V_{FT} and V_{FB}. If 0.1% matching is not met, then potentiometer R4 can be used to adjust the V_{FB} voltage to the desired level. R1 and R4 should be adjusted such that V_{ST} and V_{SB} are exactly +2.0 V and -2.0V respectively.

The analog input range will scale proportionally with respect to the reference voltage if a different input range is required. The maximum scaling factor for device operation is ± 20% of the recommended reference voltages of V_{FT} and V_{FB}. However, because the device is laser trimmed to optimize performance with ± 2.5 V references, the accuracy of the device will degrade if operated beyond a ± 2% range.

The following errors are defined:
+FS error = top of ladder offset voltage = Δ(+FS -V_{ST}+1 LSB)
-FS error = bottom of ladder offset voltage = Δ(-FS -V_{SB} -1 LSB)

where the +FS (full scale) input voltage is defined as the output transition between 1-10 and 1-11 and the -FS input voltage is defined as the output transition between 0-00 and 0-01.

ANALOG INPUT

V_{IN1} and V_{IN2} are the analog inputs. Both inputs are tied to the same point internally. Either one may be used as an analog input "sense" and the other for an input "force." The inputs can also be tied together and driven from the same source. The full scale input range will be 80% of the reference voltage or ±2 volts with V_{FB}=-2.5 V and V_{FT}=+2.5 V.

The drive requirements for the analog inputs are minimal when compared to conventional Flash converters due the SPT7810's extremely low input capacitance of only 5 pF and very high input resistance of 300 kΩ. For example, for an input signal of ± 2 V p-p with an input frequency of 10 MHz, the peak output current required for the driving circuit is only 628 μA.

CLOCK INPUT

The clock inputs (CLK, $\overline{CLK}$) are designed to be driven differentially with ECL levels. The clock may be driven single ended since $\overline{CLK}$ is internally biased to -1.3 V $\overline{CLK}$. may be left open, but a .01 μF bypass capacitor to AGND is recommended. As with all high speed circuits, proper terminations are required to avoid signal reflections and possible ringing that can cause the device to trigger at an unwanted time.

The CLK pulse width (tpwH) must be kept between 10 ns and 300 ns to ensure proper operation of the internal track-and-hold amplifier. (See timing diagram.) When operating the SPT7810 at sampling rates above 3 MSPS, it is recommended that the clock input duty cycle be kept at 50% to optimize performance. The analog input signal is latched on the rising edge of the CLK.

DIGITAL OUTPUTS

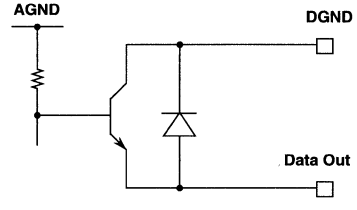
The format of the output data (D0-D9) is straight binary. These outputs are ECL with the output circuit shown in figure 4. The outputs are latched on the rising edge of CLK with a propagation delay of 4 ns. There is a one clock cycle latency between CLK and the valid output data (see timing diagram). These digital outputs can drive 50 ohms to ECL levels when pulled down to -2 V. The total specified power dissipation of the device does not include the power used by these loads. The additional power used by these loads can vary between 10 and 300 mW typically (including the overrange load) depending on the output codes. If lower power levels are desired, the output loads can be reduced, but careful consideration to the capacitive loads in relation to the operating frequency must be considered.

Table 2 - Output Data Information

ANALOG INPUT	OVERRANGE D10	OUTPUT CODE D9-D0
>+2.0 V + 1/2 LSB	1	11 1111 1111
+2.0 V -1 LSB	0	11 1111 111Ø
0.0 V	0	ØØ ØØØØ ØØØØ
-2.0 V +1 LSB	0	00 0000 0000
<2.0 V	0	00 0000 0000

(Ø indicates the flickering bit between logic 0 and 1).

Figure 3 - Output Circuit



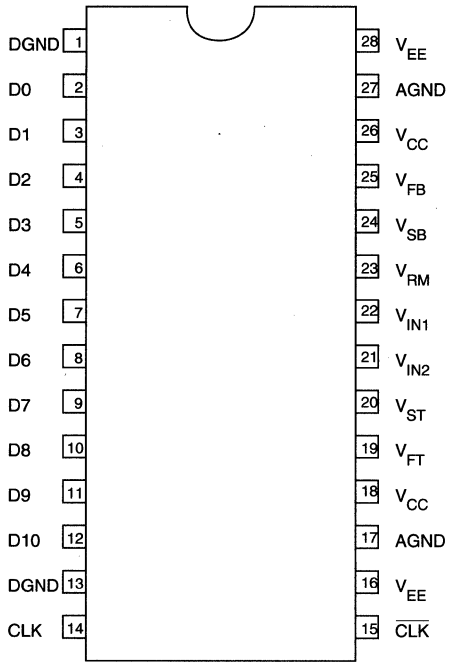
OVERRANGE OUTPUT

The OVERRANGE OUTPUT (D10) is an indication that the analog input signal has exceeded the positive full scale input voltage by 1 LSB. When this condition occurs, D10 will switch to logic 1. All other data outputs (D0 to D9) will remain at logic 1 as long as D10 remains at logic 1. This feature makes it possible to include the SPT7810 into higher resolution systems.

EVALUATION BOARD

The EB7810 evaluation board is available to aid designers in demonstrating the full performance of the SPT7810. This board includes a reference circuit, clock driver circuit, output data latches and an on-board reconstruction of the digital data. An application note describing the operation of this board as well as information on the testing of the SPT7810 is also available. Contact the factory for price and availability.

PIN ASSIGNMENT



PIN FUNCTIONS

NAME	FUNCTION
DGND	Digital Ground
D0-D9	ECL Outputs (D0=LSB)
D10	ECL Output Overrange
CLK	Clock Input
$\overline{\text{CLK}}$	Inverted Clock Input
V_{EE}	-5.2 V Supply
AGND	Analog Ground
V_{CC}	+5.0 V supply
V_{IN1}, V_{IN2}	Inputs (tied together at the die)
V_{FT}	Force for Top of Reference Ladder
V_{ST}	Sense for Top of Reference Ladder
V_{FB}	Force for Bottom of Reference Ladder
V_{SB}	Sense for Bottom of Reference Ladder
V_{RM}	Middle of Reference Ladder

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LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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SIGNAL PROCESSING TECHNOLOGIES

SPT7814

10-BIT, 40 MSPS, ECL OUTPUT A/D CONVERTER

FEATURES

- Monolithic 40 MSPS Converter
- On-Chip Track/Hold
- Bipolar ±2.0 V Analog Input
- 57 dB SNR @ 3.58 MHz Input
- 50 dB SNR @ 10.3 MHz Input
- Low Power (1.3 W Typical)
- 5 pF Input Capacitance
- ECL Outputs

APPLICATIONS

- Medical Imaging
- Professional Video
- Radar Receivers
- Instrumentation
- Electronic Warfare
- Digital Communications

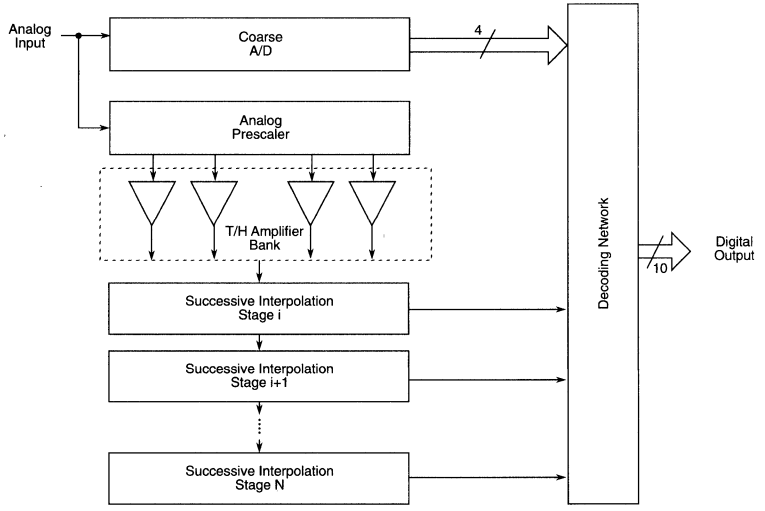
GENERAL DESCRIPTION

The SPT7814 A/D converter is a 10-bit monolithic converter capable of word rates of a minimum of 40 MSPS. On board track/hold function assures excellent dynamic performance without the need for external components. Drive requirement problems are minimized with an input capacitance of only 5 pF.

Inputs and outputs are ECL to provide a higher level of noise immunity in high speed system applications. An overrange output signal is provided to indicate overflow conditions. Output data format is straight binary. Power dissipation is very low at only 1.3 watts with power supply voltages of +5.0 and -5.2 volts. The SPT7814 also provides a wide input voltage swing of ±2.0 volts.

The SPT7814 is available in a small 28-lead ceramic side-brazed DIP, PDIP, and die form. Commercial and industrial temperature ranges are currently offered. Contact the factory for availability of military temperature ranges and /833 processed units.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages
- V_{CC} ..... +6 V
- V_{EE} ..... -6 V

Input Voltages
- Analog Input ..... $V_{FB} \leq V_{IN} \leq V_{FT}$
- V_{FT}, V_{FB} ..... +3.0 V, -3.0 V
- Reference Ladder Current ..... 12 mA

Output
- Digital Outputs ..... +30 to -30 mA

Temperature
- Operating Temperature ..... -25 to +85 °C
- Junction Temperature (1) ..... 175 °C
- Lead Temperature, (soldering 10 seconds) ..... 300 °C
- Storage Temperature ..... -65 to +150 °C

Note: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

$T_A=T_{min}$ - T_{max}, V_{CC}=+5.0 V, V_{EE}=-5.2 V, V_{IN}=±2.0 V, V_{SB}=-2.0 V, V_{ST}=+2.0 V, f_{clock}=40 MHz, 50% clock duty cycle, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7814A MIN	SPT7814A TYP	SPT7814A MAX	SPT7814B MIN	SPT7814B TYP	SPT7814B MAX	UNITS
Resolution			10			10			Bits
DC Accuracy (+25 °C)	± Full Scale								
Integral Nonlinearity	250 kHz Sample Rate	I		±1.0			±1.5		LSB
Differential Nonlinearity		I		±0.5			±0.75		LSB
No Missing Codes				Guaranteed			Guaranteed		
Analog Input									
Input Voltage Range		VI		±2.0			±2.0		
Input Bias Current	V_{IN}=0 V	VI		30	60		30	60	µA
Input Resistance		VI	100	300		100	300		kΩ
Input Capacitance		V		5			5		pF
Input Bandwidth	3 dB Small Signal	V		120			120		MHz
+FS Error		V		±2.0			±2.0		LSB
-FS Error		V		±2.0			±2.0		LSB
Reference Input									
Reference Ladder Resistance		VI	500	800		500	800		Ω
Reference Ladder Tempco		V		0.8			0.8		Ω/°C
Timing Characteristics									
Maximum Conversion Rate		VI	40			40			MHz
Overvoltage Recovery Time		V		20			20		ns
Pipeline Delay (Latency)		VI			1			1	Clock Cycle
Output Delay	T_A=+25 °C	V		5			5		ns
Aperture Delay Time	T_A=+25 °C	V		1			1		ns
Aperture Jitter Time	T_A=+25 °C	V		5			5		ps-RMS
Dynamic Performance									
Effective Number of Bits									
fin=1 MHz				8.7			8.2		Bits
fin=3.58 MHz				8.7			8.2		Bits
fin=10.3 MHz				7.3			6.9		Bits

1 Typical thermal impedances: 28L sidebrazed DIP: θ_{ja} = 50 °C/W,
28L plastic DIP: θ_{ja} = 50 °C/W.

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ELECTRICAL SPECIFICATIONS

$T_A=T_{min}$ - T_{max}, V_{CC}=+5.0 V, V_{EE}=-5.2 V, V_{IN}=±2.0 V, V_{SB}=-2.0 V, V_{ST}=+2.0 V, f_{clock}=40 MHz, 50% clock duty cycle, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7814A MIN	SPT7814A TYP	SPT7814A MAX	SPT7814B MIN	SPT7814B TYP	SPT7814B MAX	UNITS
Dynamic Performance									
Signal-To-Noise Ratio (without Harmonics)									
fin=1 MHz	+25 °C	I	55	57		52	54		dB
	$T_A=T_{min}$ - T_{max}	IV	53	55		50	52		dB
fin=3.58 MHz	+25 °C	I	55	57		52	54		dB
	$T_A=T_{min}$ - T_{max}	IV	53	55		50	52		dB
fin=10.3 MHz	+25 °C	I	48	50		46	48		dB
	$T_A=T_{min}$ - T_{max}	IV	45	47		43	45		dB
Harmonic Distortion									
fin=1 MHz	+25 °C	I	54	56		52	54		dB
	$T_A=T_{min}$ - T_{max}	IV	51	53		49	51		dB
fin=3.58 MHz	+25 °C	I	54	56		52	54		dB
	$T_A=T_{min}$ - T_{max}	IV	51	53		49	51		dB
fin=10.3 MHz	+25 °C	I	46	48		43	45		dB
	$T_A=T_{min}$ - T_{max}	IV	45	47		41	43		dB
Signal-to-Noise and Distortion									
fin=1 MHz	+25 °C	I	52	54		49	51		dB
	$T_A=T_{min}$ - T_{max}	IV	49			46			dB
fin=3.58 MHz	+25 °C	I	52	54		49	51		dB
	$T_A=T_{min}$ - T_{max}	IV	49			46			dB
fin=10.3 MHz	+25 °C	I	44	46		41	43		dB
	$T_A=T_{min}$ - T_{max}	IV	43			40			dB
Spurious Free Dynamic Range	+25 °C, fin=1 MHz	V		67			67		dB
Differential Phase	+25 °C, fin=3.58 & 4.35 MHz	V		0.2			0.2		Degree
Differential Gain	+25 °C, fin=3.58 & 4.35 MHz	V		0.5			0.7		%
Digital Inputs									
Logic "1" Voltage		V	-1.1			-1.1			V
Logic "0" Voltage		V			-1.5			-1.5	V
Maximum Input Current Low		VI	-500	±200	+750	-500	±200	+750	µA
Maximum Input Current High		VI	-500	±300	+750	-500	+300	+750	µA
Pulse Width Low (CLK)		IV	10			10			ns
Pulse Width High (CLK)		IV	10		300	10		300	ns
Digital Outputs									
Logic "1" Voltage	50 Ω to -2 V	VI	-1.1	-0.8		-1.1	-0.8		V
Logic "0" Voltage	50 Ω to -2 V	VI		-1.8	-1.5		-1.8	-1.5	V
Power Supply Requirements									
Voltages V_{CC}		IV	+4.75	-5.0	+5.25	+4.75	+5.0	+5.25	V
$-V_{EE}$		IV	-4.95	-5.2	-5.45	-4.95	-5.2	-5.45	V
Currents I_{CC}		VI		140	170		140	190	mA
$-I_{EE}$		VI		115	140		115	160	mA
Power Dissipation	Outputs Open	VI		1.3	1.6		1.3	1.8	W
Power Supply Rejection Ratio	(5 V ±0.25 V, -5.2 V ±2.0 V)	V		1.0			1.0		LSB

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests; therefore, $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

Figure 1A: Timing Diagram

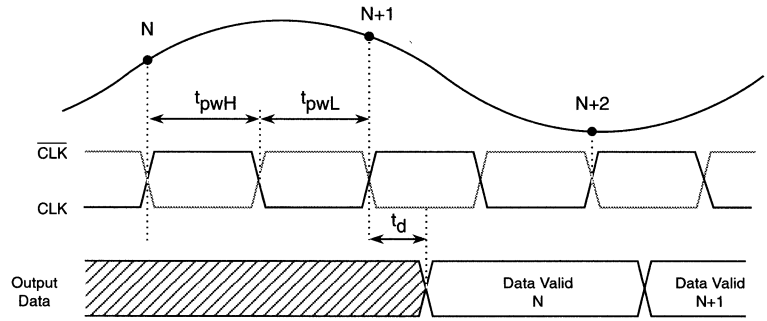

Figure 1B: Single Event Clock

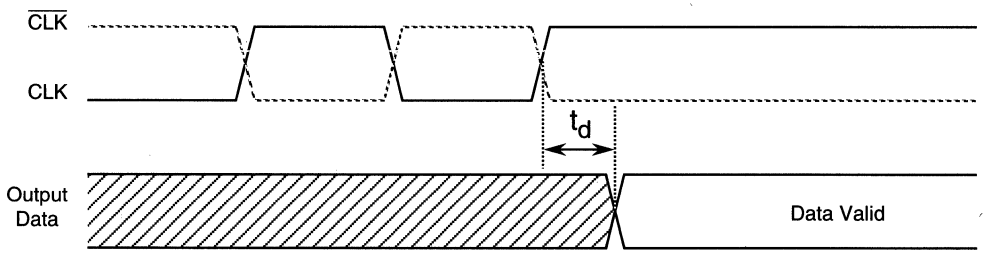

Table 1 - Timing Parameters

PARAMETERS	DESCRIPTION	MIN	TYP	MAX	UNITS
t_d	CLK to Data Valid Prop Delay	-	5		ns
t_{pwH}	CLK High Pulse Width	10	-	300	ns
t_{pwL}	CLK Low Pulse Width	10	-	-	ns

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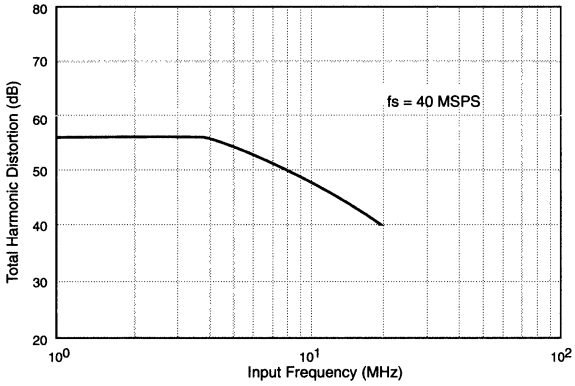
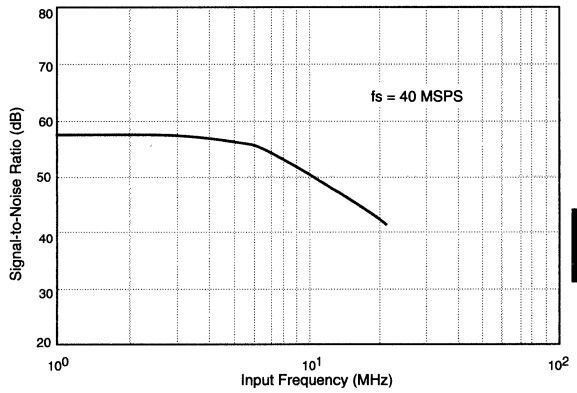
TYPICAL PERFORMANCE CHARACTERISTICS

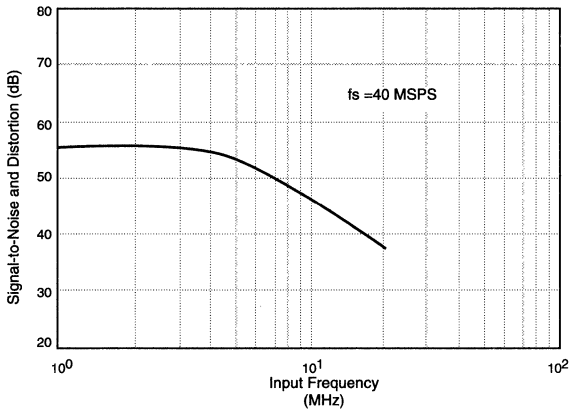
THD vs Input Frequency



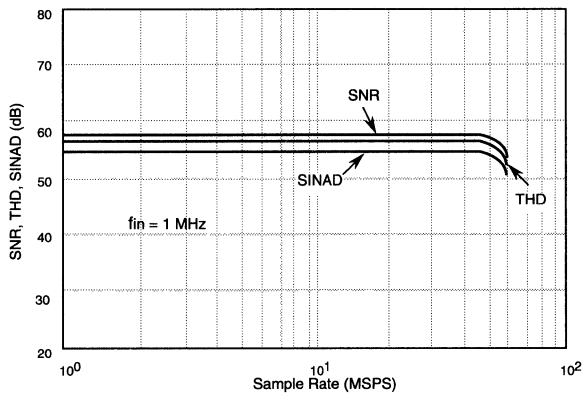
SNR vs Input Frequency



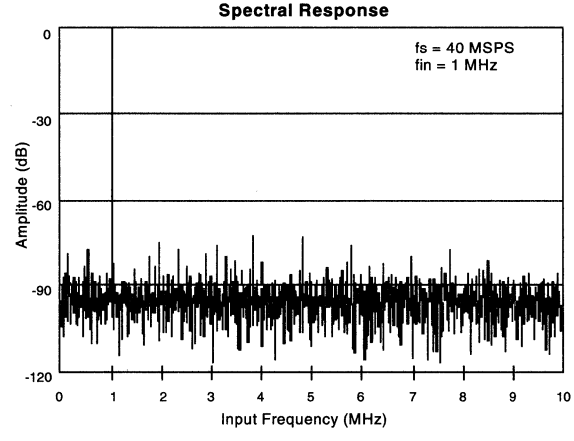
SINAD vs Input Frequency



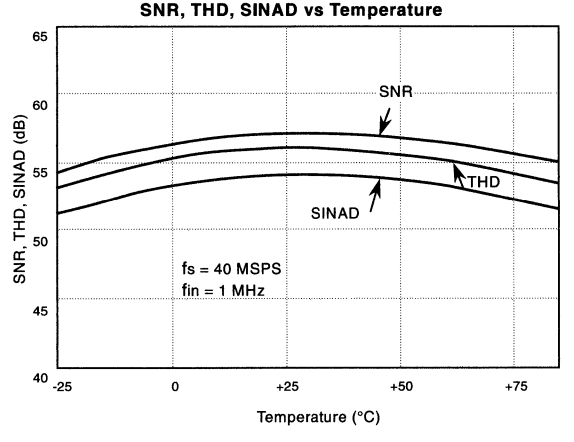
SNR, THD, SINAD vs Sample Rate



Spectral Response



SNR, THD, SINAD vs Temperature



TYPICAL INTERFACE CIRCUIT

The SPT7814 requires few external components to achieve the stated operation and performance. Figure 2 shows the typical interface requirements when using the SPT7814 in normal circuit operation.

The following section provides a description of the pin functions and outlines critical performance criteria to consider for achieving the optimal device performance.

POWER SUPPLIES AND GROUNDING

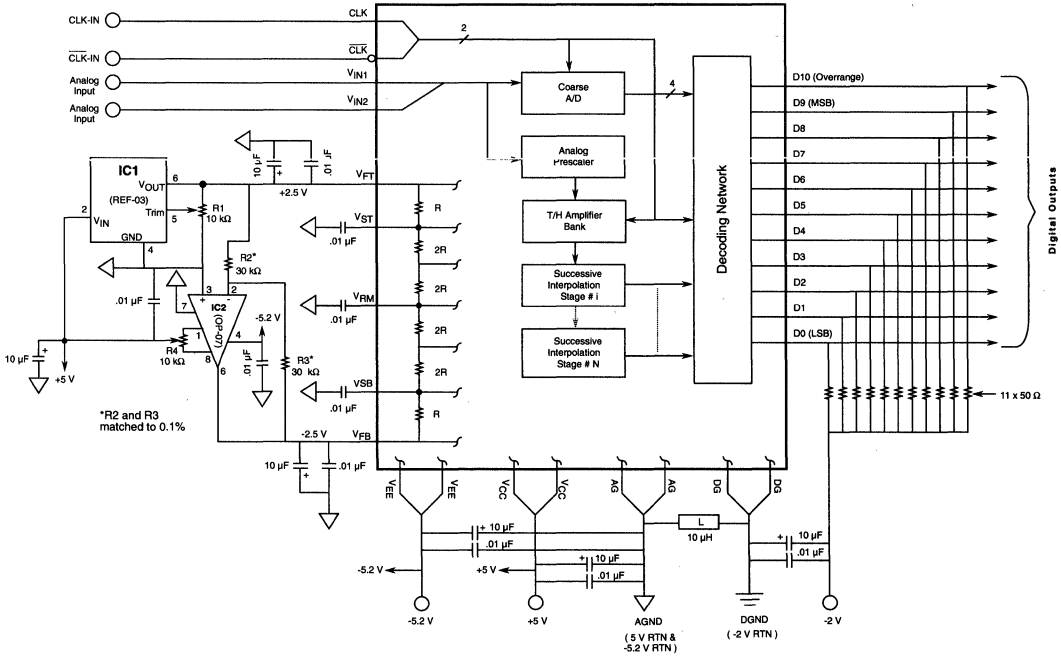
The SPT7814 requires the use of two supply voltages, V_{EE} and V_{CC}. Both supplies should be treated as analog supply sources. This means the V_{EE} and V_{CC} ground returns of the device should both be connected to the analog ground plane. All other -5.2 V requirements of the external digital logic circuit should be connected to the digital ground plane. Each power supply pin should be bypassed as closely as possible to the device with .01 µF and 10 µF capacitors as shown in figure 2.

The two grounds available on the SPT7814 are AGND and DGND. DGND is used only for ECL outputs and is to be referenced to the output pulldown voltage. These grounds are not tied together internal to the device. The use of ground planes is recommended to achieve the best performance of the SPT7814. The AGND and the DGND ground planes should be separated from each other and only connected together at the device through an inductance. Doing this will minimize the ground noise pickup.

VOLTAGE REFERENCE

The SPT7814 requires the use of two voltage references: V_{FT} and V_{FB}. V_{FT} is the force for the top of the voltage reference ladder (+2.5 V typ), V_{FB} (-2.5 V typ) is the force for the bottom of the voltage reference ladder. Both voltages are applied across an internal reference ladder resistance of 800 ohms. In addition, there are 3 reference ladder taps (V_{ST},V_{RM} and V_{SB}). V_{ST} is the sense for the top of the reference ladder (+2.0 V), V_{RM} is the midpoint of the ladder (0.0 V typ) and V_{SB} is the sense for the bottom of the reference ladder (-2.0 V). The voltages seen at V_{ST} and V_{SB} are the true full scale input voltages of the device when V_{FT} and V_{FB} are driven to the recommended voltages (+2.5 V and -2.5 V typical respectively). These points should be used to monitor the actual full scale input voltage of the device and should not be driven to the expected ideal values as is commonly done with standard flash converters. When not being used, a decoupling capacitor of .01 uF connected to AGND from each tap is recommended to minimize high frequency noise injection.

Figure 2 - Typical Interface Circuit



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An example of a reference driver circuit recommended is shown in figure 2. IC1 is REF-03, the +2.5 V reference with a tolerance of 0.6% or ± 0.015 V. The potentiometer R1 is 10 kΩ and supports a minimum adjustable range of up to 150 mV. IC2 is recommended to be an OP-07 or equivalent device. R2 and R3 must be matched to within 0.1% with good TC tracking to maintain a 0.3 LSB matching between V_{FT} and V_{FB}. If 0.1% matching is not met, then potentiometer R4 can be used to adjust the V_{FB} voltage to the desired level. R1 and R4 should be adjusted such that V_{ST} and V_{SB} are exactly +2.0 V and -2.0 V respectively.

The analog input range will scale proportionally with respect to the reference voltage if a different input range is required. The maximum scaling factor for device operation is ± 20% of the recommended reference voltages of V_{FT} and V_{FB}. However, because the device is laser trimmed to optimize performance with ± 2.5 V references, the accuracy of the device will degrade if operated beyond a ± 2% range.

The following errors are defined:
+FS error = top of ladder offset voltage = Δ(+FS -V_{ST}+1 LSB)
-FS error=bottom of ladder offset voltage=Δ(-FS -V_{SB} -1 LSB)
where the +FS (full scale) input voltage is defined as the output transition between 1-10 and 1-11 and the -FS input voltage is defined as the output transition between 0-00 and 0-01.

ANALOG INPUT

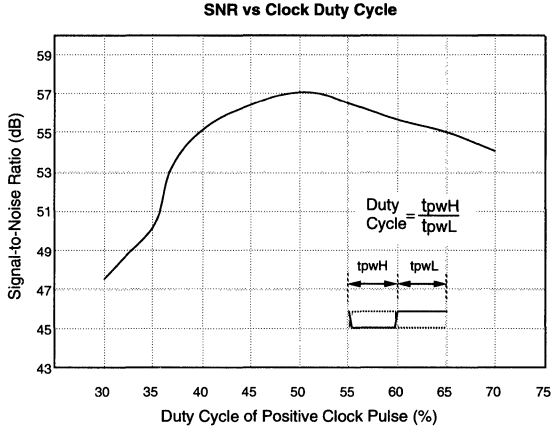
V_{IN1} and V_{IN2} are the analog inputs. Both inputs are tied to the same point internally. Either one may be used as an analog input "sense" and the other for an input "force." The inputs can also be tied together and driven from the same source. The full scale input range will be 80% of the reference voltage or ±2 volts with V_{FB}=-2.5 V and V_{FT}=+2.5 V.

The drive requirements for the analog inputs are minimal when compared to conventional Flash converters due the SPT7814's extremely low input capacitance of only 5 pF and very high input resistance of 300 kΩ. For example, for an input signal of ± 2 V p-p with an input frequency of 10 MHz, the peak output current required for the driving circuit is only 628 μA.

CLOCK INPUT

The clock inputs (CLK,$\overline{CLK}$) are designed to be driven differentially with ECL levels. The clock may be driven single ended since $\overline{CLK}$ is internally biased to -1.3 V$\overline{CLK}$. may be left open, but a .01 μF bypass capacitor to AGND is recommended. As with all high speed circuits, proper terminations are required to avoid signal reflections and possible ringing that can cause the device to trigger at an unwanted time.

The CLK pulse width (tpwH) must be kept between 10 ns and 300 ns to ensure proper operation of the internal track-and-hold amplifier. (See timing diagram.) When operating the SPT7814 at sampling rates above 3 MSPS, it is recommended that the clock input duty cycle be kept at 50% to optimize performance. (See graph.) The analog input signal is latched on the rising edge of the CLK.



DIGITAL OUTPUTS

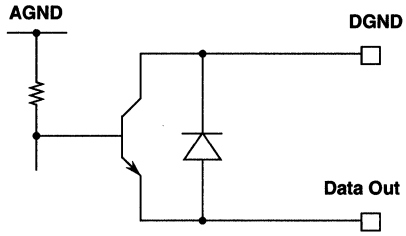
The format of the output data (D0-D9) is straight binary. These outputs are ECL with the output circuit shown in figure 4. The outputs are latched on the rising edge of CLK with a propagation delay of 4 ns. There is a one clock cycle latency between CLK and the valid output data (see timing diagram). These digital outputs can drive 50 ohms to ECL levels when pulled down to -2 V. The total specified power dissipation of the device does not include the power used by these loads. The additional power used by these loads can vary between 10 and 300 mW typically (including the overrange load) depending on the output codes. If lower power levels are desired, the output loads can be reduced, but careful consideration to the capacitive loads in relation to the operating frequency must be considered.

Table 2 - Output Data Information

ANALOG INPUT	OVERRANGE D1O	OUTPUT CODE D9-DO
>+2.0 V + 1/2 LSB	1	11 1111 1111
+2.0 V -1 LSB	O	11 1111 111Ø
0.0 V	O	ØØ ØØØØ ØØØØ
-2.0 V +1 LSB	O	OO OOOO OOOØ
<-2.0 V	O	OO OOOO OOOO

(Ø indicates the flickering bit between logic 0 and 1).

Figure 3 - Output Circuit



OVERRANGE OUTPUT

The OVERRANGE OUTPUT (D10) is an indication that the analog input signal has exceeded the positive full scale input voltage by 1 LSB. When this condition occurs, D10 will switch to logic 1. All other data outputs (D0 to D9) will remain at logic 1 as long as D10 remains at logic 1. This feature makes it possible to include the SPT7814 into higher resolution systems.

EVALUATION BOARD

The EB7814 evaluation board is available to aid designers in demonstrating the full performance of the SPT7814. This board includes a reference circuit, clock driver circuit, output data latches and an on-board reconstruction of the digital data. An application note describing the operation of this board as well as information on the testing of the SPT7814 is also available. Contact the factory for price and availability.

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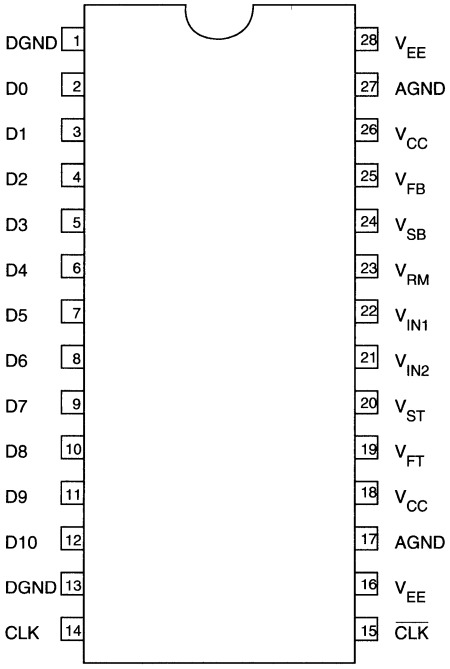
PIN ASSIGNMENT



PIN FUNCTIONS

NAME	FUNCTION
DGND	Digital Ground
D0-D9	ECL Outputs (D0=LSB)
D10	ECL Output Overrange
CLK	Clock Input
$\overline{CLK}$	Inverted Clock Input
V_{EE}	-5.2 V Supply
AGND	Analog Ground
V_{CC}	+5.0 V supply
V_{IN1}, V_{IN2}	Inputs (tied together at the die)
V_{FT}	Force for Top of Reference Ladder
V_{ST}	Sense for Top of Reference Ladder
V_{FB}	Force for Bottom of Reference Ladder
V_{SB}	Sense for Bottom of Reference Ladder
V_{RM}	Middle of Reference Ladder

LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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SPT7820

10-BIT, 20 MSPS, TTL OUTPUT, A/D CONVERTER

SIGNAL PROCESSING TECHNOLOGIES

FEATURES

- Monolithic 20 MSPS Converter
- On-Chip Track/Hold
- Bipolar ±2.0 V Analog Input
- 60 dB SNR @ 1 MHz Input
- Low Power (1.0 W Typical)
- 5 pF Input Capacitance
- TTL Outputs

APPLICATIONS

- Medical Imaging
- Professional Video
- Radar Receivers
- Instrumentation
- Electronic Warfare
- Digital Communications

3

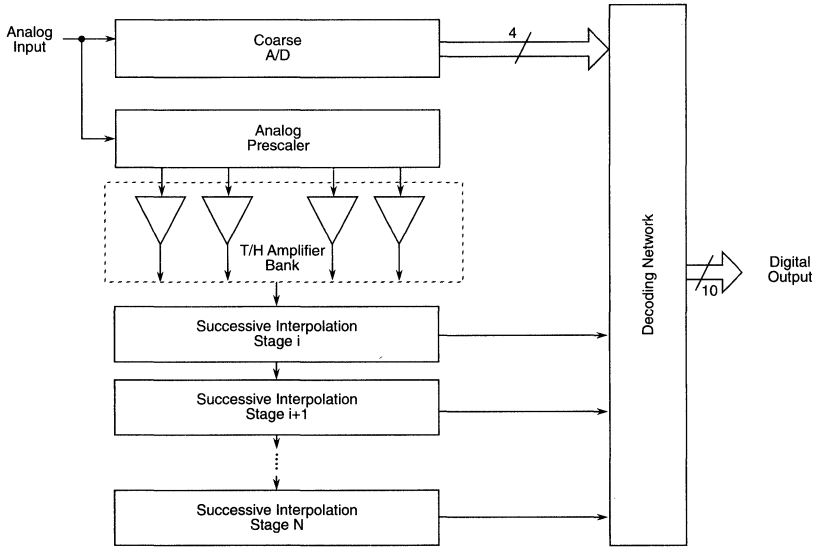
GENERAL DESCRIPTION

The SPT7820 A/D converter is a 10-bit monolithic converter capable of word rates of a minimum of 20 MSPS. On board track/hold function assures excellent dynamic performance without the need for external components. Drive requirement problems are minimized with an input capacitance of only 5 pF.

Inputs and outputs are TTL compatible to interface with TTL logic systems. An overrange output signal is provided to indicate overflow conditions. Output data format is straight binary. Power dissipation is very low at only 1.0 watt with power supply voltages of +5.0 and -5.2 volts. The SPT7820 also provides a wide input voltage swing of ±2.0 volts.

The SPT7820 is available in a 28-lead ceramic sidebrazed DIP, PDIP, LCC, and SOIC packages in commercial, industrial and military temperature ranges. The SPT7820 is available in an /883 version in 28L DIP, and it is available in die form.

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages
- V_{CC} ..... +6 V
- V_{EE} ..... -6 V

Input Voltages
- Analog Input ..... $V_{FB} \leq V_{IN} \leq V_{FT}$
- V_{FT}, V_{FB} ..... +3.0 V, -3.0 V
- Reference Ladder Current ..... 12 mA
- CLK Input ..... V_{CC}

Output
- Digital Outputs ..... +30 to -30 mA

Temperature
- Operating Temperature ..... -55 to +125 °C
- Junction Temperature[1] ..... 175 °C
- Lead Temperature, (soldering 10 seconds) ..... 300 °C
- Storage Temperature ..... -65 to +150 °C

Note: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

$T_A=T_{min}$ - T_{max}, V_{CC}=+5.0 V, V_{EE}=-5.2 V, DV_{CC}=+5.0 V, V_{IN}=±2.0 V, V_{SB}=-2.0 V, V_{ST}=+2.0 V, f_{clock}=20 MHz, 50% clock duty cycle, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7820A MIN	SPT7820A TYP	SPT7820A MAX	SPT7820B MIN	SPT7820B TYP	SPT7820B MAX	UNITS
Resolution			10			10			Bits
DC Accuracy (+25 °C)	+/- Full Scale								
Integral Nonlinearity	250 kHz Sample Rate	I		±1.0			±1.5		LSB
Differential Nonlinearity		I		±0.5			±0.75		LSB
No Missing Codes				Guaranteed			Guaranteed		
Analog Input									
Input Voltage Range		VI		±2.0			±2.0		V
Input Bias Current	V_{IN}=0 V	VI		30	60		30	60	µA
Input Bias Current	T_A=-55 to +125 °C	VI			75			75	µA
Input Resistance		VI	100	300		100	300		kΩ
Input Resistance	-55 to +125 °C	VI	75	300		75	300		kΩ
Input Capacitance		V		5			5		pF
Input Bandwidth	3 dB Small Signal	V		120			120		MHz
+FS Error		V		±2.0			±2.0		LSB
-FS Error		V		±2.0			±2.0		LSB
Reference Input									
Reference Ladder Resistance		VI	500	800		500	800		Ω
Reference Ladder Tempco		V		0.8			0.8		Ω/°C
Timing Characteristics									
Maximum Conversion Rate		VI	20			20			MHz
Overvoltage Recovery Time		V		20			20		ns
Pipeline Delay (Latency)		VI			1			1	Clock Cycle
Output Delay	T_A=+25 °C	V		14	18		14	18	ns
Aperture Delay Time	T_A=+25 °C	V		1			1		ns
Aperture Jitter Time	T_A=+25 °C	V		5			5		ps-RMS
Acquisition Time	T_A=+25 °C	V		20			20		ns
Dynamic Performance									
Effective Number of Bits									
fin=1 MHz				9.2			8.7		Bits
fin=3.58 MHz				8.8			8.3		Bits
fin=10.0 MHz				7.5			7.0		Bits

1 Typical thermal impedances (unsoldered, in free air): 28L sidebrazed DIP: θ_{ja} = 50 °C/W, 28L LCC: θ_{ja} = 99 °C/W, 28L plastic DIP: θ_{ja} = 50 °C/W, 28L SOIC: θ_{ja} = 100 °C/W.

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ELECTRICAL SPECIFICATIONS

$T_A=T_{min}$ - T_{max}, V_{CC}=+5.0 V, V_{EE}=-5.2 V, DV_{CC}=+5.0 V, V_{IN}=±2.0 V, V_{SB}=-2.0 V, V_{ST}=+2.0 V, f_{clock}=20 MHz, 50% clock duty cycle, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7820A MIN	SPT7820A TYP	SPT7820A MAX	SPT7820B MIN	SPT7820B TYP	SPT7820B MAX	UNITS
Dynamic Performance									
Signal-To-Noise Ratio (without Harmonics)									
fin=1 MHz	+25 °C	I	57	60		54	57		dB
	(0-70, -25 to +85 °C)	IV	55	58		52	55		dB
	-55 to +125 °C*	I	52	55		49	52		dB
fin=3.58 MHz	+25 °C	I	56	58		53	55		dB
	(0-70, -25 to +85 °C)	IV	54	56		51	53		dB
	-55 to +125 °C*	I	52	54		49	51		dB
fin=10.0 MHz	+25 °C	I	50	53		47	49		dB
	(0-70, -25 to +85 °C)	IV	47	50		44	46		dB
	-55 to +125 °C*	I	43	46		40	42		dB
Harmonic Distortion									
fin=1 MHz	+25 °C	I	57	60		54	57		dB
	(0-70, -25 to +85 °C)	IV	54	57		51	54		dB
	-55 to +125 °C*	I	50	53		47	50		dB
fin=3.58 MHz	+25 °C	I	56	58		53	55		dB
	(0-70, -25 to +85 °C)	IV	53	55		50	52		dB
	-55 to +125 °C*	I	50	52		47	49		dB
fin=10.0 MHz	+25 °C	I	46	48		43	45		dB
	(0-70, -25 to +85 °C)	IV	45	47		42	44		dB
	-55 to +125 °C*	I	45	47		42	44		dB
Signal-to-Noise and Distortion									
fin=1 MHz	+25 °C	I	55	57		52	54		dB
	(0-70, -25 to +85 °C)	IV	52			49			dB
	-55 to +125 °C*	I	48			45			dB
fin=3.58 MHz	+25 °C	I	54	55		51	52		dB
	(0-70, -25 to +85 °C)	IV	51			48			dB
	-55 to +125 °C*	I	48			45			dB
fin=10.0 MHz	+25 °C	I	44	47		41	44		dB
	(0-70, -25 to +85 °C)	IV	43			40			dB
	-55 to +125 °C*	I	41			38			dB
Spurious Free Dynamic Range	+25 °C, fin = 1 MHz	V		67			67		dB
Differential Phase	+25 °C, fin = 3.58 & 4.35 MHz	V		0.2			0.2		Degree
Differential Gain	+25 °C, fin = 3.58 & 4.35 MHz	V		0.5			0.7		%
Digital Inputs									
Logic "1" Voltage		V	2.4		4.5	2.4		4.0	V
Logic "0" Voltage		V			0.8			0.8	V
Maximum Input Current Low	+25 °C	IV	0	+5	+20	0	+5	+20	µA
Maximum Input Current High	+25 °C	IV	0	+5	+20	0	+5	+20	µA
Pulse Width Low (CLK)		IV	20			20			ns
Pulse Width High (CLK)		IV	20		300	20		300	ns
Digital Outputs									
Logic "1" Voltage		IV	2.4			2.4			V
Logic "0" Voltage		IV			0.6			0.6	V
Power Supply Requirements									
Voltages V_{CC}		IV	4.75		5.25	4.75		5.25	V
DV_{CC}		IV	4.75	5.0	5.25	4.75	5.0	5.25	V
$-V_{EE}$		IV	-4.95	-5.2	-5.45	-4.95	-5.2	-5.45	V
Currents I_{CC}		VI		118	145		118	145	mA
DI_{CC}		VI		40	55		40	55	mA
$-I_{EE}$		VI		40	57		40	57	mA
Power Dissipation		VI		1.0	1.3		1.0	1.3	W
Power Supply Rejection	(5 V ±0.25 V, -5.2 ±0.25 V)	V		1.0			1.0		LSB

*Temperature tested MIL and /883 only.

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests; therefore, $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

Figure 1A: Timing Diagram

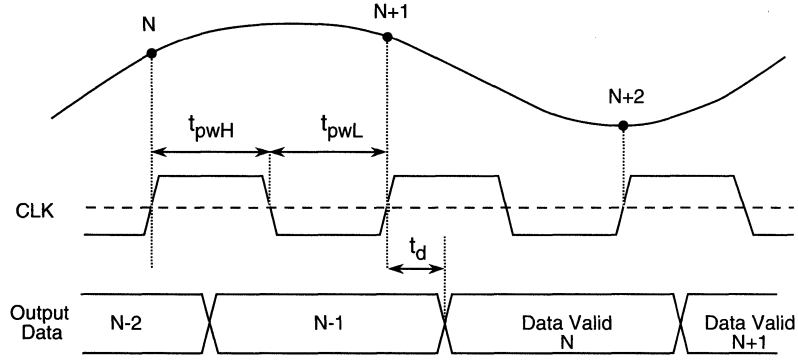

Figure 1B: Single Event Clock

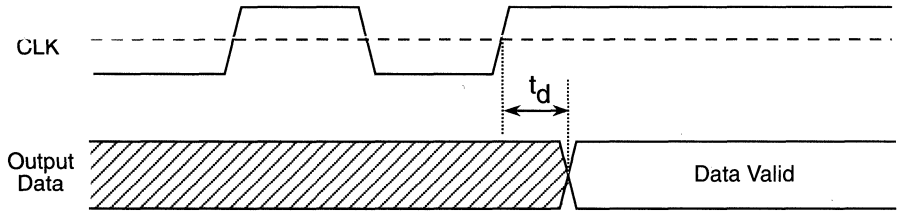

Table 1 - Timing Parameters

PARAMETERS	DESCRIPTION	MIN	TYP	MAX	UNITS
t_d	CLK to Data Valid Prop Delay	-	14	18	ns
t_{pwH}	CLK High Pulse Width	20	-	300	ns
t_{pwL}	CLK Low Pulse Width	20	-	-	ns

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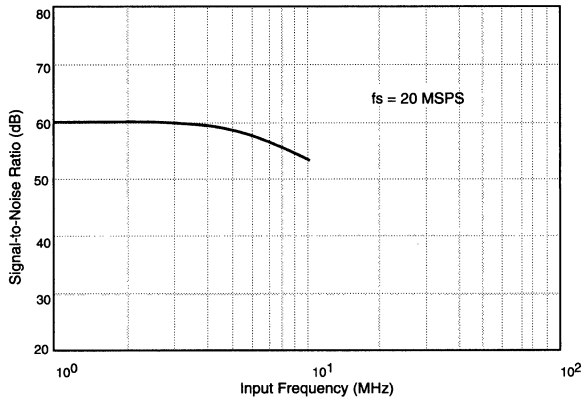
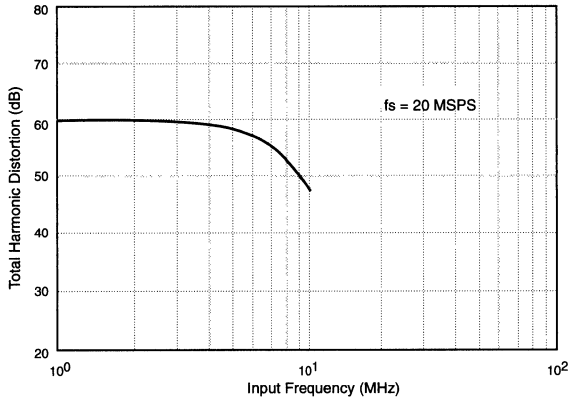
TYPICAL PERFORMANCE CHARACTERISTICS

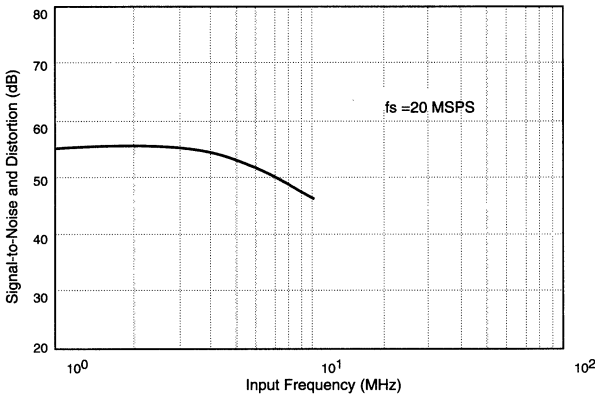
SNR vs Input Frequency



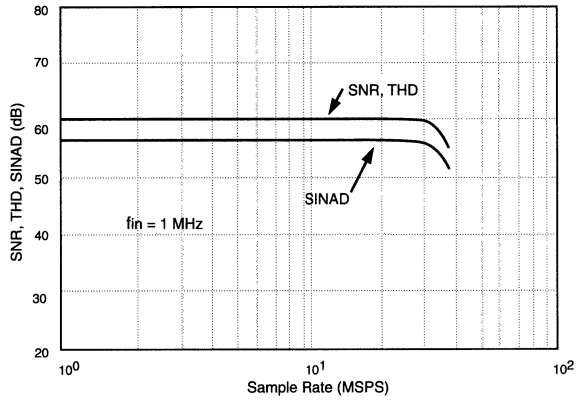
THD vs Input Frequency



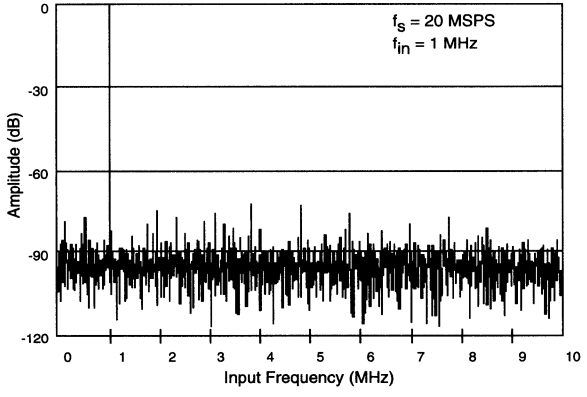
SINAD vs Input Frequency



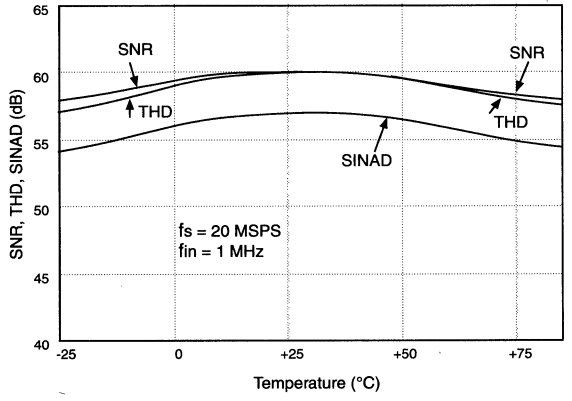
SNR, THD, SINAD vs Sample Rate



Spectral Response



SNR, THD, SINAD vs Temperature



TYPICAL INTERFACE CIRCUIT

The SPT7820 requires few external components to achieve the stated operation and performance. Figure 2 shows the typical interface requirements when using the SPT7820 in normal circuit operation. The following section provides a description of the pin functions and outlines critical performance criteria to consider for achieving the optimal device performance.

POWER SUPPLIES AND GROUNDING

The SPT7820 requires -5.2 V and +5 V analog supply voltages. The +5 V supply is common to analog V_{CC} and digital DV_{CC}. A ferrite bead in series with each supply line is intended to reduce the transient noise injected into the analog V_{CC}. These beads should be connected as closely as possible to the device. The connection between the beads and the SPT7820 should not be shared with any other device. Each power supply pin should be bypassed as closely as possible to the device. Use 0.1 µF for V_{EE} and V_{CC}, and 0.01 µF for DV_{CC} (chip caps are preferred).

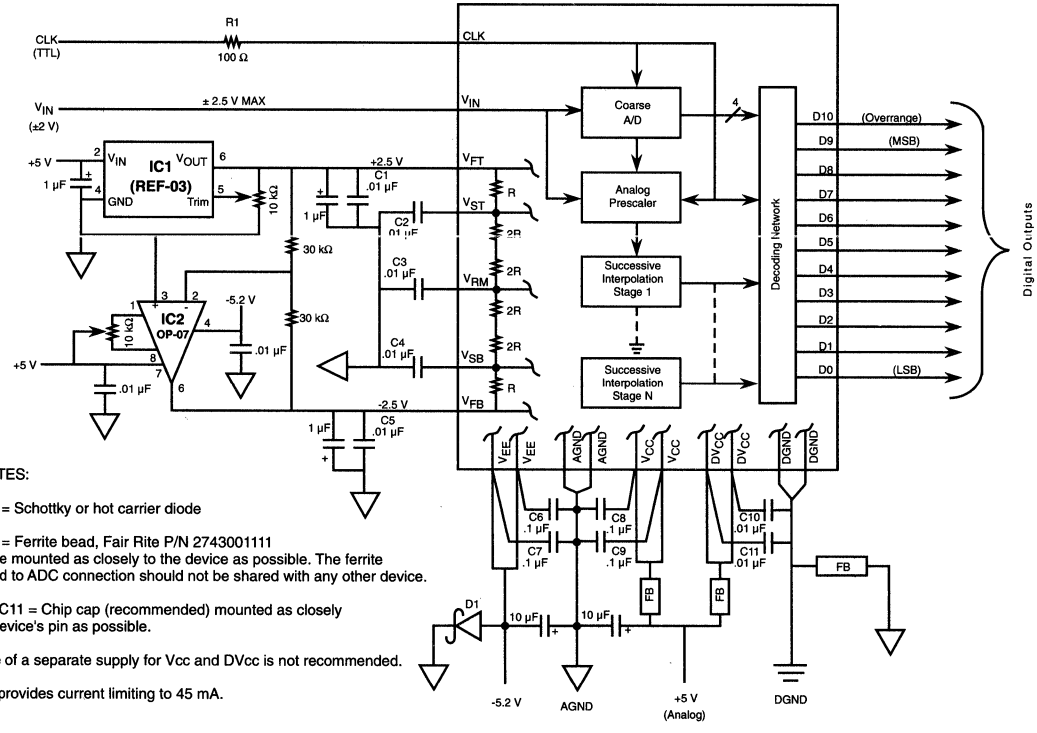
AGND and DGND are the two grounds available on the SPT7820. These two internal grounds are isolated on the device. The use of ground planes is recommended to achieve optimum device performance. DGND is needed for the DV_{CC} return path (40 mA typical) and for the return path for all digital output logic interfaces. AGND and DGND should be separated from each other and connected together only at the device through a ferrite bead.

A Schottky or hot carrier diode connected between AGND and V_{EE} is required. The use of separate power supplies between V_{CC} and DV_{CC} is not recommended due to potential power supply sequencing latch-up conditions. Using the recommended interface circuit shown in figure 2 will provide optimum device performance for the SPT7820.

VOLTAGE REFERENCE

The SPT7820 requires the use of two voltage references: V_{FT} and V_{FB}. V_{FT} is the force for the top of the voltage reference ladder (+2.5 V typ), V_{FB} (-2.5 V typ) is the force for the bottom of the voltage reference ladder. Both voltages are applied across an internal reference ladder resistance of 800 Ω. The +2.5 V voltage source for reference V_{FT} must be current limited to 20 mA maximum if a different driving circuit is used in place of the recommended reference circuit shown in figures 2 and 3. In addition, there are three reference

Figure 2 - Typical Interface Circuit



NOTES:

1) D1 = Schottky or hot carrier diode
2) FB = Ferrite bead, Fair Rite P/N 2743001111 to be mounted as closely to the device as possible. The ferrite bead to ADC connection should not be shared with any other device.
3) C1-C11 = Chip cap (recommended) mounted as closely to device's pin as possible.
4) Use of a separate supply for Vcc and DVcc is not recommended.
5) R1 provides current limiting to 45 mA.

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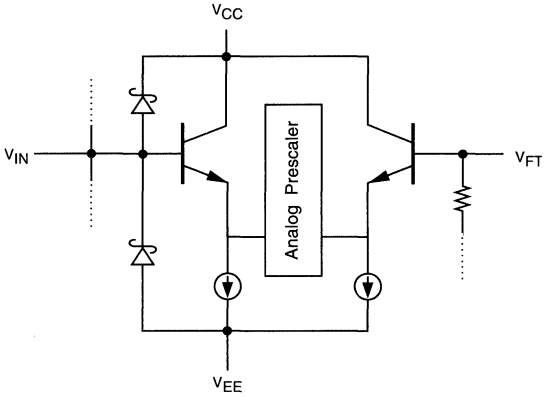
ladder taps (V_{ST}, V_{RM} and V_{SB}). V_{ST} is the sense for the top of the reference ladder (+2.0 V), V_{RM} is the midpoint of the ladder (0.0 V typ) and V_{SB} is the sense for the bottom of the reference ladder (-2.0 V). The voltages seen at V_{ST} and V_{SB} are the true full scale input voltages of the device when V_{FT} and V_{FB} are driven to the recommended voltages (+2.5 V and -2.5 V typical respectively). These points should be used to monitor the actual full scale input voltage of the device and should not be driven to the expected ideal values as is commonly done with standard flash converters. When not being used, a decoupling capacitor of .01 µF (chip cap preferred) connected to AGND from each tap is recommended to minimize high frequency noise injection.

Figure 3 - Analog Equivalent Input Circuit



An example of a reference driver circuit recommended is shown in figure 2. IC1 is REF-03, the +2.5 V reference with a tolerance of 0.6% or +/- 0.015 V. The potentiometer R1 is 10 kΩ and supports a minimum adjustable range of up to 150 mV. IC2 is recommended to be an OP-07 or equivalent device. R2 and R3 must be matched to within 0.1% with good TC tracking to maintain a 0.3 LSB matching between V_{FT} and V_{FB}. If 0.1% matching is not met, then potentiometer R4 can be used to adjust the V_{FB} voltage to the desired level. V_{FT} and V_{FB} should be adjusted such that V_{ST} and V_{SB} are exactly +2.0 V and -2.0 V respectively.

The analog input range will scale proportionally with respect to the reference voltage if a different input range is required. The maximum scaling factor for device operation is ± 20% of the recommended reference voltages of V_{FT} and V_{FB}. However, because the device is laser trimmed to optimize performance with ± 2.5 V references, the accuracy of the device will degrade if operated beyond a ± 2% range.

The following errors are defined:
+FS error = top of ladder offset voltage = Δ(+FS -V_{ST}+1 LSB)
-FS error = bottom of ladder offset voltage = Δ(-FS -V_{SB}-1 LSB)
where the +FS (full scale) input voltage is defined as the output transition between 1-10 and 1-11 and the -FS input voltage is defined as the output transition between 0-00 and 0-01.

ANALOG INPUT

V_{IN} is the analog input. The full scale input range will be 80% of the reference voltage or ±2 volts with V_{FB}=-2.5 V and V_{FT}=+2.5 V.

The drive requirements for the analog inputs are minimal when compared to conventional Flash converters due to the SPT7820's extremely low input capacitance of only 5 pF and very high input resistance of 300 kΩ. For example, for an input signal of ±2 V p-p with an input frequency of 10 MHz, the peak output current required for the driving circuit is only 628 µA.

CLOCK INPUT

The SPT7820 is driven from a single-ended TTL input (CLK). The CLK pulse width (tpwH) must be kept between 20 ns and 300 ns to ensure proper operation of the internal track-and-hold amplifier. (See timing diagram.) When operating the SPT7820 at sampling rates above 3 MSPS, it is recommended that the clock input duty cycle be kept at 50% but performance will not be degraded if kept within the range of 40-60%. The analog input signal is latched on the rising edge of the CLK.

The clock input must be driven from fast TTL logic (V_{IH} ≤4.5 V, T_{RISE} <6 ns). In the event the clock is driven from a high current source, use a 100 Ω resistor in series to current limit to approximately 45 mA.

DIGITAL OUTPUTS

The format of the output data (D0-D9) is straight binary. (See table 2.) The outputs are latched on the rising edge of CLK with a propagation delay of 14 ns (typ). There is a one clock cycle latency between CLK and the valid output data. (See timing diagram.)

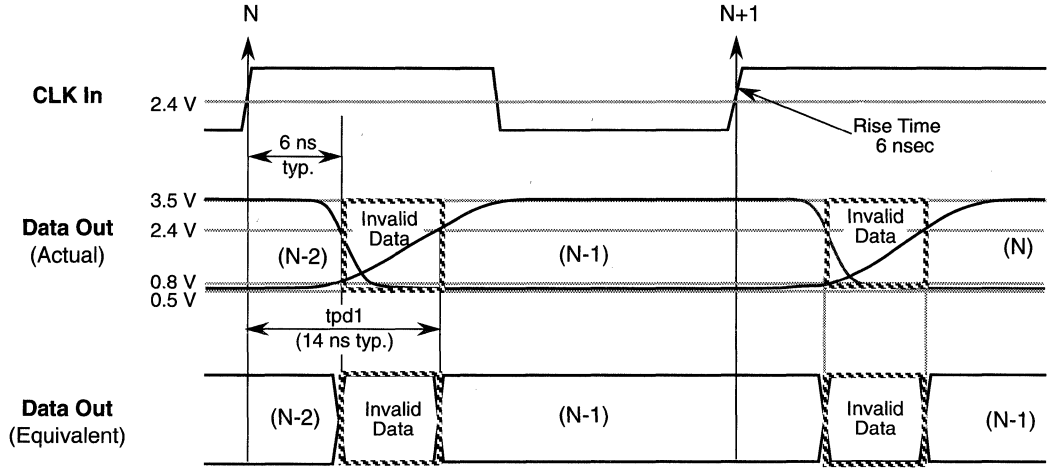
Table 2 - Output Data Information

ANALOG INPUT	OVERRANGE D1O	OUTPUT CODE D9-DO
>+2.0 V + 1/2 LSB	1	11 1111 1111
+2.0 V -1 LSB	O	11 1111 111Ø
0.0 V	O	ØØ ØØØØ ØØØØ
-2.0 V +1 LSB	O	OO OOOO OOOØ
<2.0 V	O	OO OOOO OOOO

(Ø indicates the flickering bit between logic 0 and 1).

The rise times and fall times of the digital outputs are not symmetrical. The propagation delay of the rise time is typically 14 ns and the fall time is typically 6 ns. (See figure 4.) The nonsymmetrical rise and fall times create approximately 8 ns of invalid data.

Figure 4 - Digital Output Characteristics



OVERRANGE OUTPUT

The OVERRANGE OUTPUT (D10) is an indication that the analog input signal has exceeded the positive full scale input voltage by 1 LSB. When this condition occurs, D10 will switch to logic 1. All other data outputs (D0 to D9) will remain at logic 1 as long as D10 remains at logic 1. This feature makes it possible to include the SPT7820 into higher resolution systems.

EVALUATION BOARD

The EB7820 evaluation board is available to aid designers in demonstrating the full performance of the SPT7820. This board includes a reference circuit, clock driver circuit, output data latches and an on-board reconstruction of the digital data. An application note describing the operation of this board as well as information on the testing of the SPT7820 is also available. Contact the factory for price and availability.

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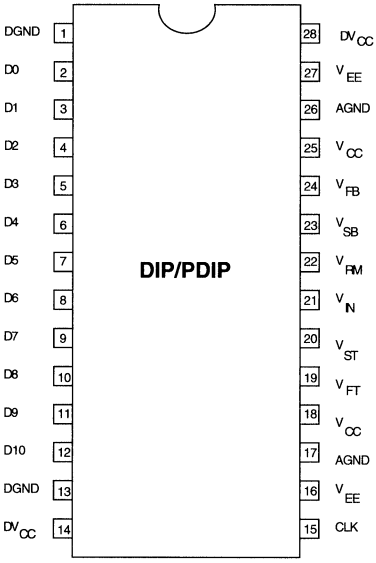
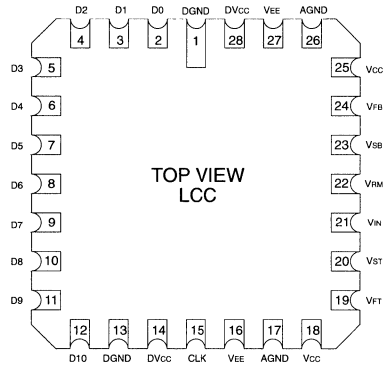
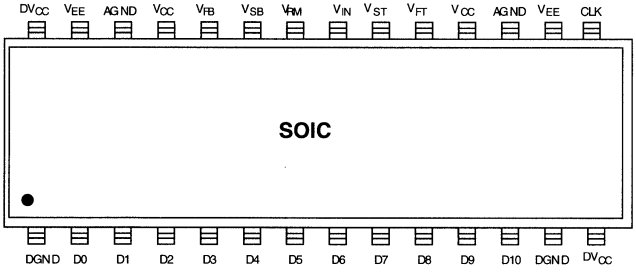
PIN ASSIGNMENTS







PIN FUNCTIONS

NAME	FUNCTION
DGND	Digital Ground
D0-D9	TTL Outputs (D0=LSB)
D10	TTL Output Overrange
CLK	Clock
V_{EE}	-5.2 V Supply (Analog)
AGND	Analog Ground
V_{CC}	+5.0 V supply (Analog)

NAME	FUNCTION
V_{IN}	Analog Input
DV_{CC}	Digital +5.0 V Supply
V_{RM}	Middle of Voltage Reference Ladder
V_{FT}	Force for Top of Reference Ladder
V_{ST}	Sense for Top of Reference Ladder
V_{FB}	Force for Bottom of Reference Ladder
V_{SB}	Sense for Bottom of Reference Ladder

LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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SIGNAL PROCESSING TECHNOLOGIES

SPT7824

10-BIT, 40 MSPS, TTL OUTPUT A/D CONVERTER

FEATURES

- Monolithic 40 MSPS Converter
- On-Chip Track/Hold
- Bipolar ±2.0 V Analog Input
- 57 dB SNR @ 3.58 MHz Input
- Low Power (1.0 W Typical)
- 5 pF Input Capacitance
- TTL Outputs

APPLICATIONS

- Medical Imaging
- Professional Video
- Radar Receivers
- Instrumentation
- Electronic Warfare
- Digital Communications

3

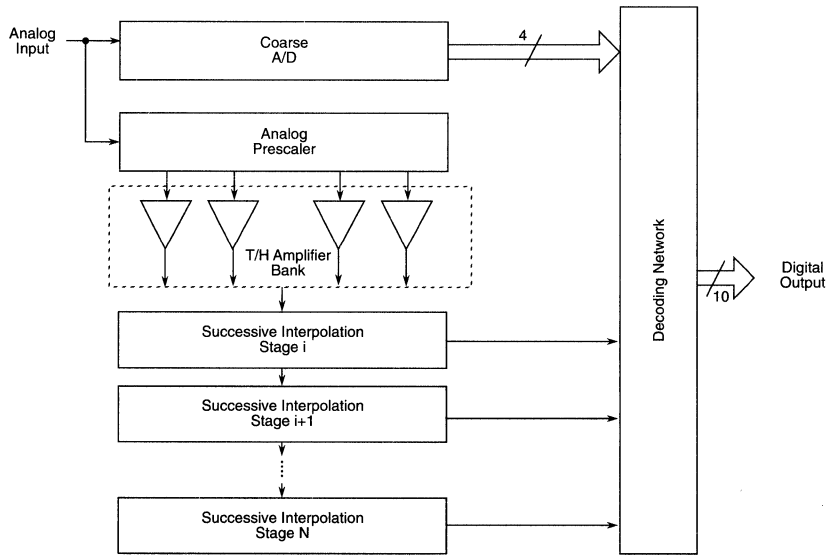
GENERAL DESCRIPTION

The SPT7824 A/D converter is a 10-bit monolithic converter capable of word rates a minimum of 40 MSPS. On board track/hold function assures excellent dynamic performance without the need for external components. Drive requirement problems are minimized with an input capacitance of only 5 pF.

Inputs and outputs are TTL compatible to interface with TTL logic systems. An overrange output signal is provided to indicate overflow conditions. Output data format is straight binary. Power dissipation is very low at only 1.0 watt with power supply voltages of +5.0 and -5.2 volts. The SPT7824 also provides a wide input voltage swing of ±2.0 volts.

The SPT7824 is available in a 28-lead ceramic sidebrazed DIP, PDIP, LCC, and SOIC packages in commercial, industrial and military temperature ranges. The SPT7824 is available in an /883 version in 28L DIP, and it is available in die form.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages
- V_{CC} ..... +6 V
- V_{EE} ..... -6 V

Input Voltages
- Analog Input ..... $V_{FB} \leq V_{IN} \leq V_{FT}$
- V_{FT}, V_{FB} ..... +3.0 V, -3.0 V
- Reference Ladder Current ..... 12 mA
- CLK Input ..... V_{CC}

Output
- Digital Outputs ..... +30 to -30 mA

Temperature
- Operating Temperature ..... -55 to +125 °C
- Junction Temperature[1] ..... 175 °C
- Lead Temperature, (soldering 10 seconds) ..... 300 °C
- Storage Temperature ..... -65 to +150 °C

Note: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

$T_A=T_{min}$ - T_{max}, V_{CC}=+5.0 V, V_{EE}=-5.2 V, DV_{CC}=+5.0 V, V_{IN}=±2.0 V, V_{SB}=-2.0 V, V_{ST}=+2.0 V, f_{clock}=40 MHz, 50% clock duty cycle, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7824A MIN	SPT7824A TYP	SPT7824A MAX	SPT7824B MIN	SPT7824B TYP	SPT7824B MAX	UNITS
Resolution			10			10			Bits
DC Accuracy (+25 °C)	+/- Full Scale								
Integral Nonlinearity	250 kHz Sample Rate	I		±1.0			±1.5		LSB
Differential Nonlinearity		I		±0.5			±0.75		LSB
No Missing Codes				Guaranteed			Guaranteed		
Analog Input									
Input Voltage Range		VI		±2.0			±2.0		V
Input Bias Current	V_{IN}=0 V	VI		30	60	30		60	µA
Input Bias Current	T_A=-55 to +125 °C	VI			75			75	µA
Input Resistance		VI	100	300		100	300		kΩ
Input Resistance	-55 to +125 °C	VI	75	300		75	300		kΩ
Input Capacitance		V		5			5		pF
Input Bandwidth	3 dB Small Signal	V		120			120		MHz
+FS Error		V		±2.0			±2.0		LSB
-FS Error		V		±2.0			±2.0		LSB
Reference Input									
Reference Ladder Resistance		VI	500	800		500	800		Ω
Reference Ladder Tempco		V		0.8			0.8		Ω/°C
Timing Characteristics									
Maximum Conversion Rate		VI	40			40			MHz
Overvoltage Recovery Time		V		20			20		ns
Pipeline Delay (Latency)		VI		1				1	Clock Cycle
Output Delay	T_A=+25 °C	V		14	18	14		18	ns
Aperture Delay Time	T_A=+25 °C	V		1			1		ns
Aperture Jitter Time	T_A=+25 °C	V		5			5		ps-RMS
Acquisition Time	T_A=+25 °C	V		12			12		ns
Dynamic Performance									
Effective Number of Bits									
	fin=1 MHz				8.7			8.2	Bits
	fin=3.58 MHz				8.7			8.2	Bits
	fin=10.0 MHz				7.3			6.9	Bits

1 Typical thermal impedances (unsoldered, in free air): 28L sidebrazed DIP: θ_{ja} = 50 °C/W, 28L LCC: θ_{ja} = 99 °C/W, 28L plastic DIP: θ_{ja} = 50°C/W, 28L SOIC.

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ELECTRICAL SPECIFICATIONS

T_A=T_{MIN}-T_{MAX}, V_{CC}=+5.0 V, V_{EE}=-5.2 V, DV_{CC}=+5.0 V, V_{IN}=±2.0 V, V_{SB}=-2.0 V, V_{ST}=+2.0 V, f_{clock}=40 MHz, 50% clock duty cycle unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7824A MIN	SPT7824A TYP	SPT7824A MAX	SPT7824B MIN	SPT7824B TYP	SPT7824B MAX	UNITS
Dynamic Performance									
Signal-To-Noise Ratio (without Harmonics)									
fin=1 MHz	+25 °C	I	55	57		52	54		dB
	(0 to 70, -25 to +85 °C)	IV	53	55		50	52		dB
	-55 to +125 °C*	I	49	51		46	48		dB
fin=3.58 MHz	+25 °C	I	55	57		52	54		dB
	(0 to 70, -25 to +85 °C)	IV	53	55		50	52		dB
	-55 to +125 °C*	I	49	51		46	48		dB
fin=10.0 MHz	+25 °C	I	48	50		46	48		dB
	(0 to 70, -25 to +85 °C)	IV	45	47		43	45		dB
	-55 to +125 °C*	I	41	43		39	41		dB
Harmonic Distortion									
fin=1 MHz	+25 °C	I	54	56		52	54		dB
	(0 to 70, -25 to +85 °C)	IV	51	53		49	51		dB
	-55 to +125 °C*	I	50	52		48	50		dB
fin=3.58 MHz	+25 °C	I	54	56		52	54		dB
	(0 to 70, -25 to +85 °C)	IV	51	53		49	51		dB
	-55 to +125 °C*	I	50	52		48	50		dB
fin=10.0 MHz	+25 °C	I	46	48		43	45		dB
	(0 to 70, -25 to +85 °C)	IV	45	47		41	44		dB
	-55 to +125 °C*	I	44	46		40	42		dB
Signal-to-Noise and Distortion									
fin=1 MHz	+25 °C	I	52	54		49	51		dB
	(0 to 70, -25 to +85 °C)	IV	49			46			dB
	-55 to +125 °C*	I	48			45			dB
fin=3.58 MHz	+25 °C	I	52	54		49	51		dB
	(0 to 70, -25 to +85 °C)	IV	49			46			dB
	-55 to +125 °C*	I	48			45			dB
fin=10.0 MHz	+25 °C	I	44	46		41	43		dB
	(0 to 70, -25 to +85 °C)	IV	43			40			dB
	-55 to +125 °C*	I	40			37			dB
Spurious Free Dynamic Range	+25 °C, fin = 1 MHz	V		67			67		dB
Differential Phase	+25 °C	V		0.2			0.2		Degree
Differential Gain	+25 °C, fin = 3.58 & 4.35 MHz	V		0.5			0.7		%
Digital Inputs									
Logic "1" Voltage		V	2.4		4.5	2.4		4.0	V
Logic "0" Voltage		V			0.8			0.8	V
Maximum Input Current Low	+25 °C	IV	0	+5	+20	0	+5	+20	µA
Maximum Input Current High	+25 °C	IV	0	+5	+20	0	+5	+20	µA
Pulse Width Low (CLK)		IV	10			10			ns
Pulse Width High (CLK)		IV	10		300	10		300	ns
Digital Outputs									
Logic "1" Voltage		IV	2.4			2.4			V
Logic "0" Voltage		IV			0.6			0.6	V
Power Supply Requirements									
Voltages V_{CC}		IV	4.75		5.25	4.75		5.25	V
DV_{CC}		IV	4.75	5.0	5.25	4.75	5.0	5.25	V
$-V_{EE}$		IV	-4.95	-5.2	-5.45	-4.95	-5.2	-5.45	V
Currents I_{CC}		VI		118	145		118	145	mA
DI_{CC}		VI		40	55		40	55	mA
$-I_{EE}$		VI		40	57		40	57	mA
Power Dissipation		VI		1.0	1.3		1.0	1.3	W
Power Supply Rejection	(5 V ±0.25 V, -5.2 V ±0.25 V)	V		1.0			1.0		LSB

*Temperature tested MIL and /883 only.

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests; therefore, $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

Figure 1A - Timing Diagram

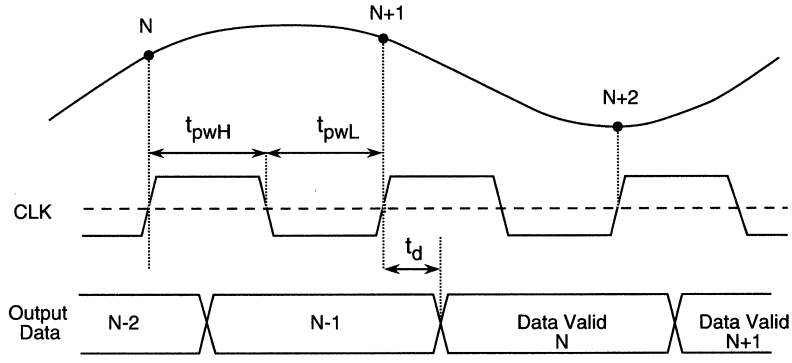

Figure 1B - Single Event Clock

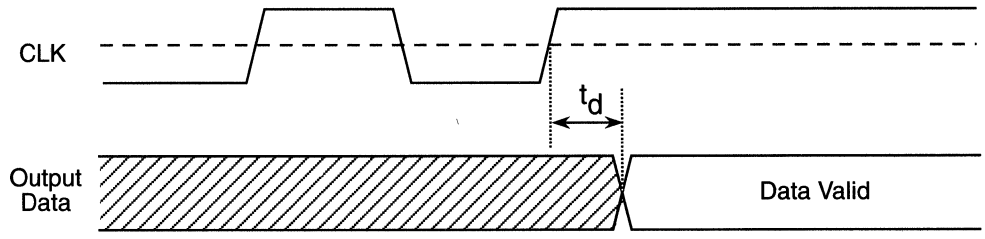

Table 1 - Timing Parameters

PARAMETERS	DESCRIPTION	MIN	TYP	MAX	UNITS
t_d	CLK to Data Valid Prop Delay	-	14	18	ns
t_{pwH}	CLK High Pulse Width	10	-	300	ns
t_{pwL}	CLK Low Pulse Width	10	-	-	ns

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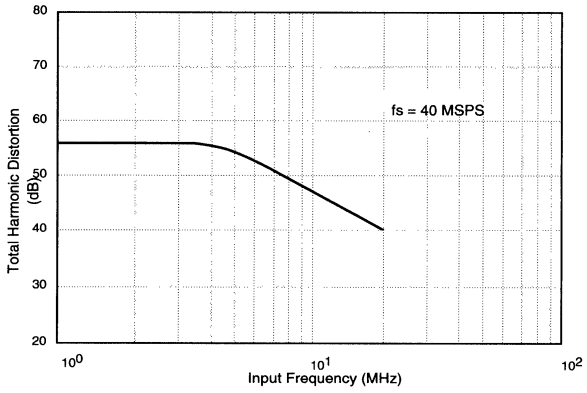
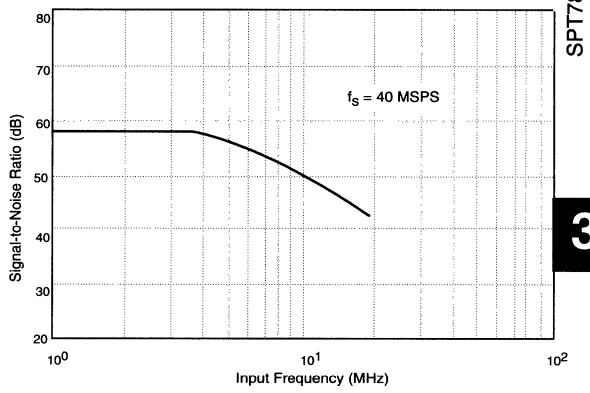
TYPICAL PERFORMANCE CHARACTERISTICS

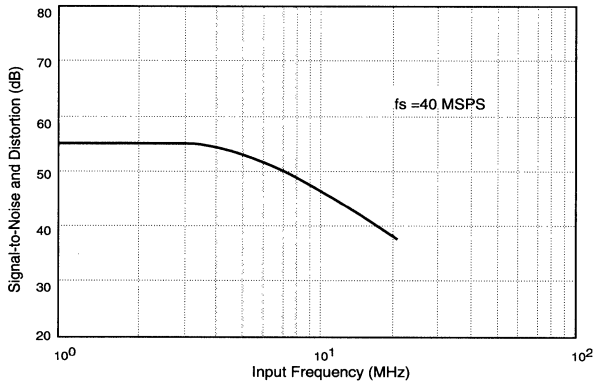
THD vs Input Frequency



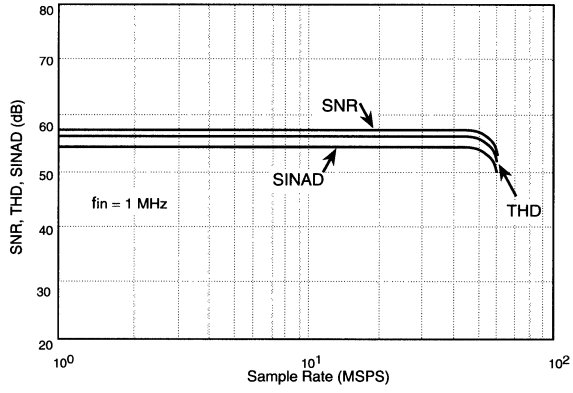
SNR vs Input Frequency



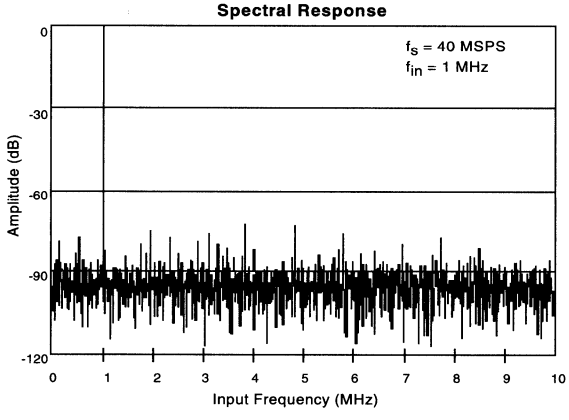
SINAD vs Input Frequency



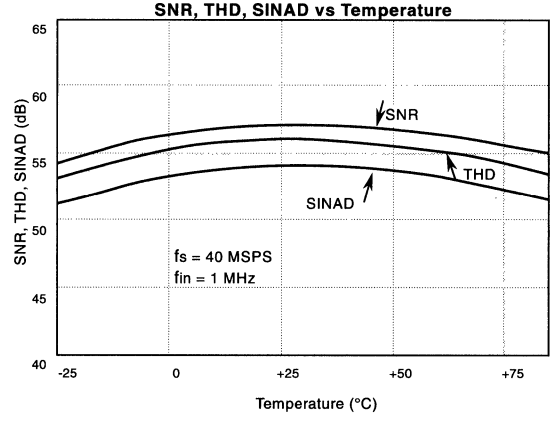
SNR, THD, SINAD vs Sample Rate



Spectral Response



SNR, THD, SINAD vs Temperature



TYPICAL INTERFACE CIRCUIT

The SPT7824 requires few external components to achieve the stated operation and performance. Figure 2 shows the typical interface requirements when using the SPT7824 in normal circuit operation. The following section provides a description of the pin functions and outlines critical performance criteria to consider for achieving the optimal device performance.

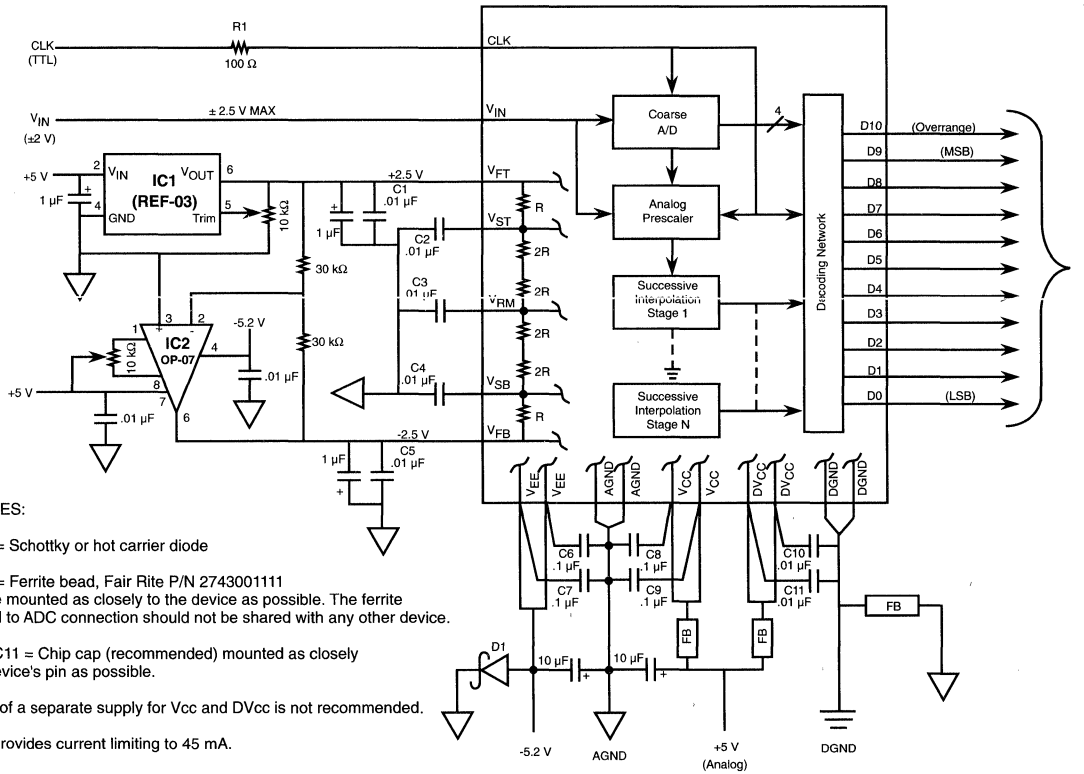
POWER SUPPLIES AND GROUNDING

The SPT7824 requires -5.2 V and +5 V analog supply voltages. The +5 V supply is common to analog V_{CC} and digital DV_{CC}. A ferrite bead in series with each supply line is intended to reduce the transient noise injected into the analog V_{CC}. These beads should be connected as closely as possible to the device. The connection between the beads and the SPT7824 should not be shared with any other device. Each power supply pin should be bypassed as closely as possible to the device. Use 0.1 µF for V_{EE} and V_{CC}, and 0.01 µF for DV_{CC} (chip caps are preferred).

AGND and DGND are the two grounds available on the SPT7824. These two internal grounds are isolated on the device. The use of ground planes is recommended to achieve optimum device performance. DGND is needed for the DV_{CC} return path (40 mA typical) and for the return path for all digital output logic interfaces. AGND and DGND should be separated from each other and connected together only at the device through a ferrite bead.

A Schottky or hot carrier diode connected between AGND and V_{EE} is required. The use of separate power supplies between V_{CC} and DV_{CC} is not recommended due to potential power supply sequencing latch-up conditions. Using the recommended interface circuit shown in figure 2 will provide optimum device performance for the SPT7824.

Figure 2 - Typical Interface Circuit



NOTES:

1) D1 = Schottky or hot carrier diode

2) FB = Ferrite bead, Fair Rite P/N 2743001111 to be mounted as closely to the device as possible. The ferrite bead to ADC connection should not be shared with any other device.

3) C1-C11 = Chip cap (recommended) mounted as closely to device's pin as possible.

4) Use of a separate supply for Vcc and DVcc is not recommended.

5) R1 provides current limiting to 45 mA.

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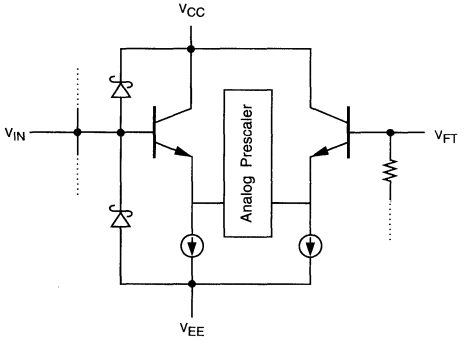
VOLTAGE REFERENCE

The SPT7824 requires the use of two voltage references: V_{FT} and V_{FB}. V_{FT} is the force for the top of the voltage reference ladder (+2.5 V typ), V_{FB} (-2.5 V typ) is the force for the bottom of the voltage reference ladder. Both voltages are applied across an internal reference ladder resistance of 800 ohms. The +2.5 V voltage source for reference V_{FT} must be current limited to 20 mA maximum if a different driving circuit is used in place of the recommended reference circuit shown in figures 2 and 3. In addition, there are three reference ladder taps (V_{ST}, V_{RM} and V_{SB}). V_{ST} is the sense for the top of the reference ladder (+2.0 V), V_{RM} is the midpoint of the ladder (0.0 V typ) and V_{SB} is the sense for the bottom of the reference ladder (-2.0 V). The voltages seen at V_{ST} and V_{SB} are the true full scale input voltages of the device when V_{FT} and V_{FB} are driven to the recommended voltages (+2.5 V and -2.5 V typical respectively). These points should be used to monitor the actual full scale input voltage of the device and should not be driven to the expected ideal values as is commonly done with standard flash converters. When not being used, a decoupling capacitor of .01 uF (chip carrier preferred) connected to AGND from each tap is recommended to minimize high frequency noise injection.

Figure 3 - Analog Equivalent Input Circuit



An example of a reference driver circuit recommended is shown in figure 2. IC1 is REF-03, the +2.5 V reference with a tolerance of 0.6% or +/- 0.015 V. The potentiometer R1 is 10 kΩ and supports a minimum adjustable range of up to 150 mV. IC2 is recommended to be an OP-07 or equivalent device. R2 and R3 must be matched to within 0.1% with good TC tracking to maintain a 0.3 LSB matching between V_{FT} and V_{FB}. If 0.1% matching is not met, then potentiometer R4 can be used to adjust the V_{FB} voltage to the desired level. V_{FT} and V_{FB} should be adjusted such that V_{ST} and V_{SB} are exactly +2.0 V and -2.0 V respectively.

The analog input range will scale proportionally with respect to the reference voltage if a different input range is required. The maximum scaling factor for device operation is ± 20% of the recommended reference voltages of V_{FT} and V_{FB}. However, because the device is laser trimmed to optimize performance with ± 2.5 V references, the accuracy of the device will degrade if operated beyond a ± 2% range.

The following errors are defined:
+FS error = top of ladder offset voltage = Δ(+FS -V_{ST}+1 LSB)
-FS error = bottom of ladder offset voltage = Δ(-FS-V_{SB}-1LSB)
where the +FS (full scale) input voltage is defined as the output transition between 1-10 and 1-11 and the -FS input voltage is defined as the output transition between 0-00 and 0-01.

ANALOG INPUT

V_{IN} is the analog input. The full scale input range will be 80% of the reference voltage or ±2 V with V_{FB}=-2.5 V and V_{FT}=+2.5 V.

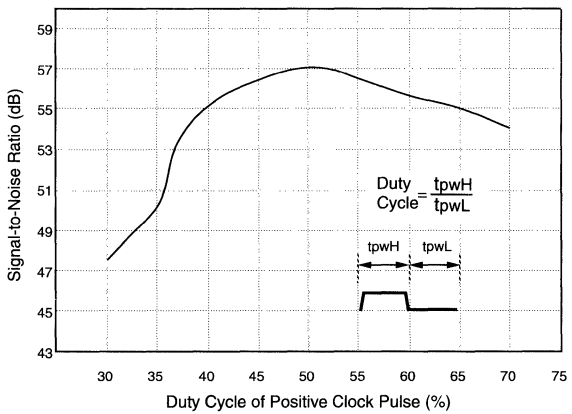
The drive requirements for the analog inputs are minimal when compared to conventional Flash converters due to the SPT7824's extremely low input capacitance of only 5 pF and very high input resistance of 300 kΩ. For example, for an input signal of ± 2 V p-p with an input frequency of 10 MHz, the peak output current required for the driving circuit is only 628 μA.

CLOCK INPUT

The SPT7824 is driven from a single-ended TTL input (CLK). The CLK pulse width (tpwH) must be kept between 10 ns and 300 ns to ensure proper operation of the internal track-and-hold amplifier. (See timing diagram.) When operating the SPT7824 at sampling rates above 3 MSPS, it is recommended that the clock input duty cycle be kept at 50% to optimize performance. (See figure 4.) The analog input signal is latched on the rising edge of the CLK.

The clock input must be driven from fast TTL logic (V_{IH}≤4.5 V, T_{RISE} <6 ns). In the event the clock is driven from a high current source, use a 100 Ω resistor in series to current limit to approximately 45 mA.

Figure 4 - SNR vs Clock Duty Cycle



DIGITAL OUTPUTS

The format of the output data (D0-D9) is straight binary. (See table 2.) The outputs are latched on the rising edge of CLK with a propagation delay of 14 ns (typ). There is a one clock cycle latency between CLK and the valid output data. (See timing diagram.)

Table 2 - Output Data Information

ANALOG INPUT	OVERRANGE D1O	OUTPUT CODE D9-DO
>+2.0 V + 1/2 LSB	1	11 1111 1111
+2.0 V -1 LSB	O	11 1111 111Ø
0.0 V	O	ØØ ØØØØ ØØØØ
-2.0 V +1 LSB	O	OO OOOO OOOØ
<2.0 V	O	OO OOOO OOOO

(Ø indicates the flickering bit between logic 0 and 1).

The rise times and fall times of the digital outputs are not symmetrical. The propagation delay of the rise time is typically 14 ns and the fall time is typically 6 ns. (See figure 5.) The nonsymmetrical rise and fall times create approximately 8 ns of invalid data.

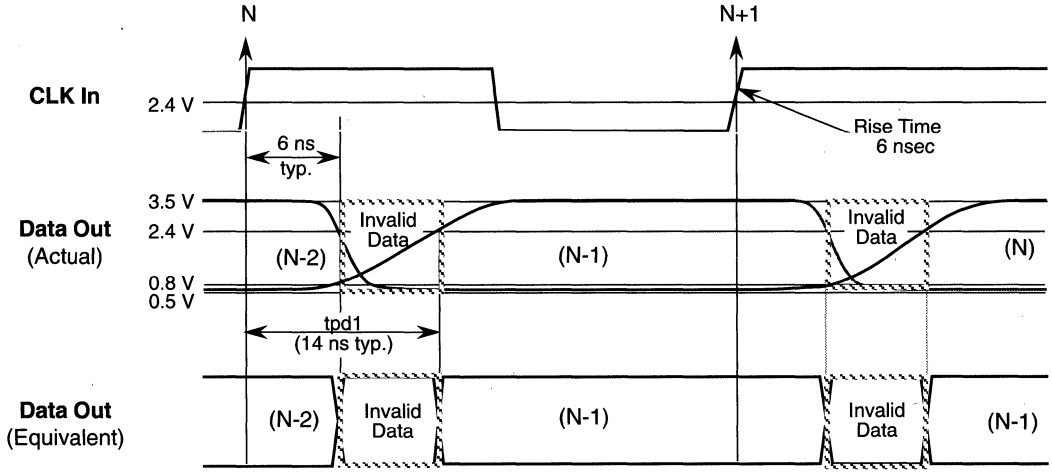
OVERRANGE OUTPUT

The OVERRANGE OUTPUT (D10) is an indication that the analog input signal has exceeded the positive full scale input voltage by 1 LSB. When this condition occurs, D10 will switch to logic 1. All other data outputs (D0 to D9) will remain at logic 1 as long as D10 remains at logic 1. This feature makes it possible to include the SPT7824 into higher resolution systems.

EVALUATION BOARD

The EB7824 Evaluation Board is available to aid designers in demonstrating the full performance of the SPT7824. This board includes a reference circuit, clock driver circuit, output data latches and an on-board reconstruction of the digital data. An application note describing the operation of this board as well as information on the testing of the SPT7824 is also available. Contact the factory for price and availability.

Figure 5 - Digital Output Characteristics



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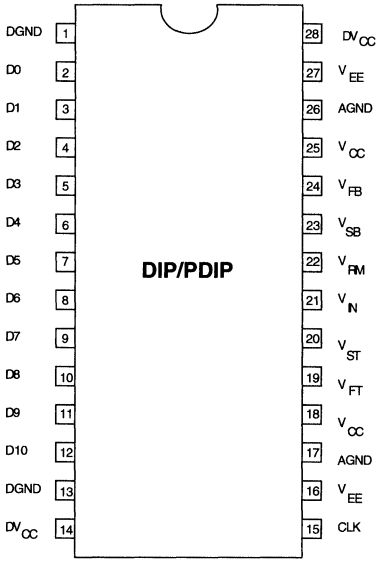
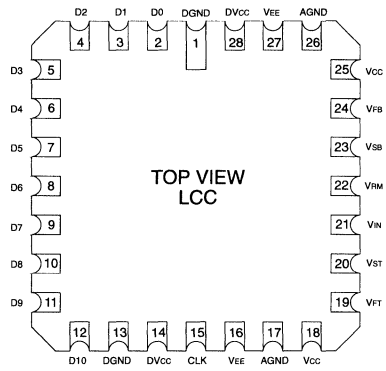
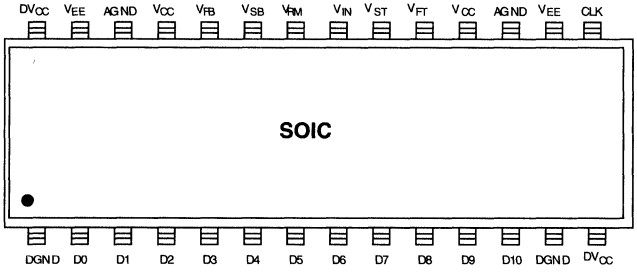
PIN ASSIGNMENTS







PIN FUNCTIONS

NAME	FUNCTION
DGND	Digital Ground
D0-D9	TTL Outputs (D0=LSB)
D10	TTL Output Overrange
CLK	Clock
V_{EE}	-5.2 V Supply (Analog)
AGND	Analog Ground
V_{CC}	+5.0 V supply (Analog)

NAME	FUNCTION
V_{IN}	Analog Input
DV_{CC}	Digital +5.0 V Supply
V_{RM}	Middle of Voltage Reference Ladder
V_{FT}	Force for Top of Reference Ladder
V_{ST}	Sense for Top of Reference Ladder
V_{FB}	Force for Bottom of Reference Ladder
V_{SB}	Sense for Bottom of Reference Ladder

LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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SPT7830

10-BIT, 2.5 MSPS, SERIAL OUTPUT A/D CONVERTER

ADVANCED INFORMATION

FEATURES

- 10-Bit, 100 kHz to 2.5 MSPS Analog-to-Digital Converter
- Monolithic CMOS
- Serial Output
- Internal Sample-and-Hold
- Analog Input Range: 0 to 2 V Nominal; 3 V Max
- Power Dissipation (including reference ladder)
  - 56 mW at +5 V
  - 37 mW at +3.3 V
- Single Power Supply: +3.3 V to +5 V Range

APPLICATIONS

- Handheld and Desktop Scanners
- DSP Interface Applications
- Automotive Applications
- Remote Sensing

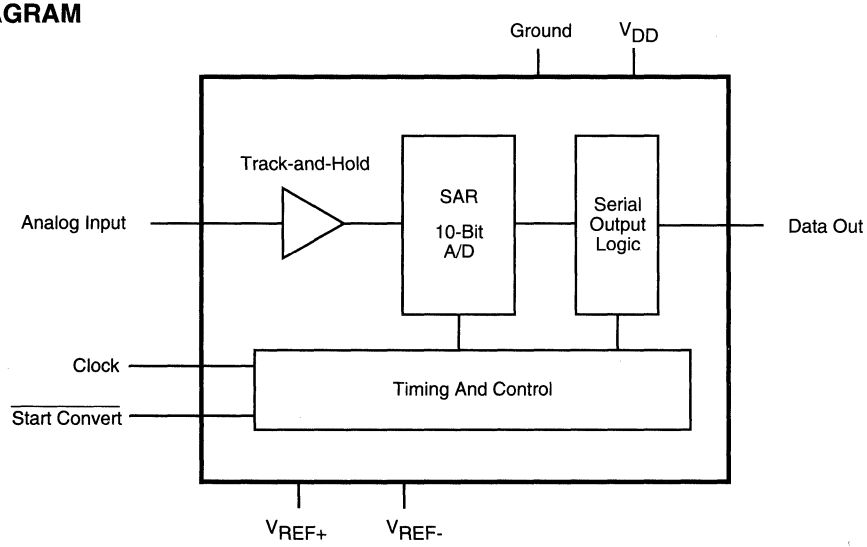
3

GENERAL DESCRIPTION

The SPT 10-bit, 2.5 MSPS serial analog-to-digital converter delivers excellent high speed conversion performance, with low cost and low power. The serial port protocol is compatible with the serial peripheral interface (SPI) or MICROWIRE™ industry standard, high-speed synchronous MPU interfaces. The large input bandwidth and fast transient response time allows for CCD applications operating up to 2.5 MSPS.

The device can operate with either +3.3 V or +5 V single supplies, with low power dissipations of 37 mW and 56 mW, respectively. The small package size makes this part excellent for hand-held applications where board real-estate is a premium. The SPT7830 is available in the commercial temperature range in an 8L SOIC package and die.

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATING (Beyond which damage may occur)[1]

Supply Voltages
- V_{DD} ..... +6 V

Input Voltages
- Analog Input ..... -0.5 to +6 V
- V_{REF+} ..... 0 to V_{DD}
- V_{REF-} ..... 0 to V_{REF+}
- Clock and $\overline{SC}$ ..... V_{DD}

Output
- Data Out ..... 10 mA

Temperature
- Operating, ambient ..... 0 to 70 °C
- junction ..... + 175 °C
- Lead, Soldering (10 seconds) ..... + 300 °C
- Storage ..... -65 to + 150 °C

Note: 1. Operation at any Absolute Maximum Ratings is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

T_A = +25 °C, V_{DD} = +3.3 V to +5.0 V, V_{IN} = 0 to 2 V, f_{CLK} = 35 MHz, f_S = 2.5 MSPS, V_{REF+} = 2.0 V, V_{REF-} = 0.0 V, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS						
DC Performance						
Resolution				10		Bits
Differential Linearity		I		±0.5		LSB
Integral Linearity		I		±1.0		LSB
No Missing Codes		I		Guaranteed		
Analog Input						
Input Voltage Range		IV	V_{REF-}	2.0	V_{REF+}	V
Input Bias Current		IV		TBD		mA
Input Resistance		I		250		kΩ
Input Capacitance		IV		5		pF
Input Bandwidth (Small Signal)		IV		TBD		MHz
Offset				±2.0		LSB
Gain Error				±2.0		LSB
Reference Input						
Resistance			250	300	350	Ω
Voltage Range						
V_{REF-}			0		V_{REF+}	V
V_{REF+}					3.0	V
Reference Settling Time					90	ns
Timing Characteristics						
Maximum Conversion Rate		I	2.5			MSPS
Minimum Conversion Rate		IV	0.1			MSPS
Maximum External Clock Rate		I	35			MHz
Minimum External Clock Rate		IV	1.4			MHz
$\overline{\text{Start Convert}}$ Min Pulse Width (t_{SC})		I	1			Clock Cycles
Aperture Delay Time		IV		5		ns
Aperture Jitter Time		IV		5		ps

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ELECTRICAL SPECIFICATIONS

T_A = +25 °C, V_{DD} = +3.3 V to +5.0 V, V_{IN} = 0 to 2 V, f_{CLK} = 35 MHz, f_S = 2.5 MSPS, V_{REF+} = 2.0 V, V_{REF-} = 0.0 V, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
Dynamic Performance						
Effective Number of Bits						
f_{IN} = 500 kHz		III		TBD		Bits
f_{IN} = 1 MHz		III		8.8		Bits
Signal-to-Noise Ratio						
f_{IN} = 500 kHz		III		TBD		dB
f_{IN} = 1 MHz		III		57		dB
Harmonic Distortion						
f_{IN} = 500 kHz		III		TBD		dB
f_{IN} = 1 MHz		III		60		dB
Power Supply Requirements						
+V_{DD} Supply Current	V_{DD} = 3.3 V	IV		9	11	mA
	V_{DD} = 5.0 V	I		13	15	mA
Power Dissipation	V_{DD} = 3.3 V	IV		31	35	mW
With V_{REF} Included	V_{DD} = 5.0 V	I		65	75	mW
Power Supply Rejection Ratio		IV		TBD		mV/V

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests; therefore, $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

GENERAL DESCRIPTION AND OPERATION

The SPT7830 is a 10-bit analog-to-digital converter that uses a successive approximation architecture to perform data conversion. Each conversion cycle is 14 clocks in length. When the Not Start Convert ($\overline{SC}$) line is held low, conversion begins on the next rising edge of the input clock. The $\overline{SC}$ line must be held low for a minimum of one clock cycle. When the conversion cycle begins, the data output pin is forced low until valid data output begins.

The first two clock cycles are used to perform internal offset calibrations and tracking of the analog input. The analog input is then sampled using and internal track-and-hold amplifier on the rising edge of the third clock cycle. On clock cycles 4 through 14, a 10-bit successive approximation conversion is performed, and the data is output starting with the MSB.

Serial data output begins with output of the MSB. See the Data Output Set Up and Hold Timing section for details. Each bit of the data conversion is sequentially determined and placed on the data output pin at the clock rate. This process continues until the LSB has been determined and output. At this point, if the $\overline{SC}$ line is high, the data output pin will be forced into a high impedance state, and the converter will go into an idle state waiting for the $\overline{SC}$ line to go low. This is referred to as Single Shot Mode. See Modes of Operation for details.

If the $\overline{SC}$ is either held low through the entire 14 clock conversion cycle (free run mode) or is brought synchronous with the trailing edge of the fourteenth clock cycle (synchronous mode), the data output pin goes low and stays low until valid data output begins. Because the chip has either remained selected in the free run mode or has been immediately selected again in the synchronous mode, the next conversion cycle begins immediately after the fourteenth clock cycle of the previous conversion. See Modes of Operation for details.

TYPICAL INTERFACE CIRCUIT

Figure 4 shows the typical interface circuit for the SPT7830.

CLOCK INPUT

The SPT7830 requires a 50% duty cycle clock running at 14 times the required sample rate. The clock may be stopped and started without degradation of operation (single shot type of operation), however, the clock should remain running during a conversion cycle.

POWER SUPPLY AND REFERENCE REQUIREMENTS

The SPT7830 requires only a single supply and operates from 3.3 V to 5.0 V. The reference ladder bottom may be grounded or range from -x V to V_{REF+}. The V_{REF+} pin may range up to V_{DD}.

The recommended V_{REF+} voltage for 3.3 V operation is V_{REF+} = 2.0 V. The recommended V_{REF+} voltage for 5.0 V operation is V_{REF+} = 3.0 V.

DATA OUTPUT SET UP AND HOLD TIMING

Figure 5 shows the set up and hold timing for the serial data output of the MSB. The MSB data output is valid on the rising edge of the fifth clock cycle. Each of following output bits is valid on the rising edge of each subsequent clock cycle. The times indicated are for 35 MHz clock operation (2.5 MSPS conversion rate).

DATA OUTPUT CODING

The coding of the output is straight binary. (See table 1.)

Table 1 - Data Output Coding

ANALOG INPUT	OUTPUT CODE D9 - DO
+F.S. ± 1/2 LSB	11 1111 111Ø
+1/2 F.S.	ØX XXXX XXXX
+1/2 LSB	OO OOOO OOOØ
V_{REF-}	OO OOOO OOOO

Ø indicates the flickering bit between logic O and 1.

X indicates the flickering bit between logic 1 and O.

ANALOG INPUT AND REFERENCE SETTLING TRACK AND HOLD TIMING

Figure 6 shows the timing relationship between the input clock and $\overline{SC}$ versus the analog input tracking and reference settling. The analog input is tracked from the fourteenth clock cycle of the previous conversion to the third clock cycle of the current conversion. On the rising edge of the third clock cycle, the analog input is held by the internal sample-and-hold. After this sample, the analog input may vary without affecting data conversion.

The reference ladder inputs (V_{REF+} and V_{REF-}) may be changed starting on the fourteenth clock cycle of the previous conversion and must be settled by the rising edge of the third clock cycle of the current conversion. The times shown in figure 6 are for 35 MHz clock operation (2.5 MSPS conversion rate).

MODES OF OPERATION

The SPT7830 has three modes of operation.The mode of operation is based strictly on how the $\overline{SC}$ is used.

SINGLE SHOT MODE

When $\overline{SC}$ goes low, conversion starts on the next rising edge of the clock (defined as the first conversion clock). $\overline{SC}$ must be held low for a minimum of one clock period. The MSB of data is valid on the rising edge of the fifth conversion clock.

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The conversion is complete after 14 clock cycles. At the fifteenth clock cycle, if $\overline{SC}$ is high (not selected), the data output goes to a high impedance state, and no more conversions will take place until the next $\overline{SC}$ low event. (See the single shot mode timing diagram in figure 1.)

SYNCHRONIZED MODE

When $\overline{SC}$ goes low, conversion will start on the next rising edge of the clock (defined as the first conversion clock). $\overline{SC}$ must be held low for a minimum of one clock period. The MSB bit of data is valid on the rising edge of the fifth conversion clock.

The first conversion is complete after 14 clock cycles. At any time after the falling edge of the fourteenth clock cycle, $\overline{SC}$ may go low again to initiate the next conversion. When the $\overline{SC}$ goes low, the conversion starts on the rising edge of the next clock. (See the synchronized mode timing diagram in figure 2.)

The data output remains low between conversion cycles if $\overline{SC}$ is asserted with the falling edge of the fourteenth clock cycle. If the assertion occurs after more than 14 clock cycles, the data output will go to a high impedance state between conversions.

FREE RUN MODE

When $\overline{SC}$ goes low, conversion starts on the next rising edge of the clock (defined as the first conversion clock). The MSB data is valid on the rising edge of the fifth conversion clock.

As long as $\overline{SC}$ is held low, the device operates in the free run mode. New conversions start after every fourteenth cycle with valid data available on the rising edge of the fifth clock within each new conversion cycle.

The data output remains low between conversion cycles. See the free run mode timing diagram in figure 3.

Figure 1 - Single Shot Mode Timing Diagram

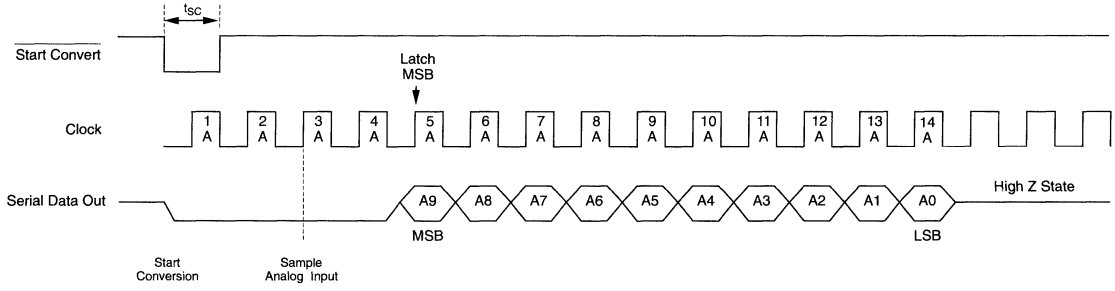


Figure 2 - Synchronous Mode Timing Diagram

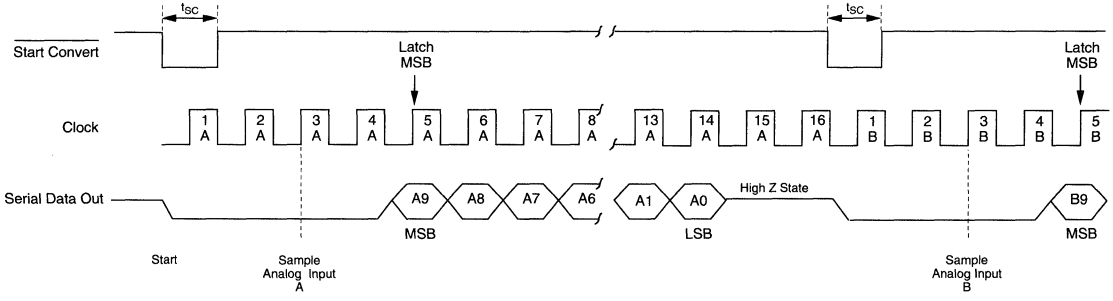


Figure 3 - Free Run Mode Timing Diagram

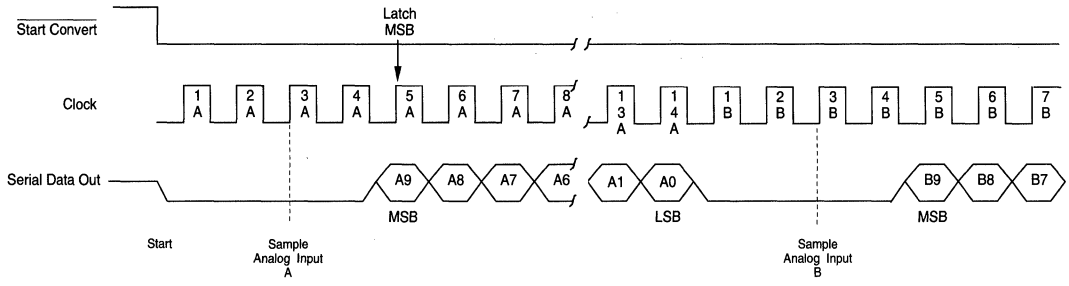


Figure 4 - Typical Interface Circuit

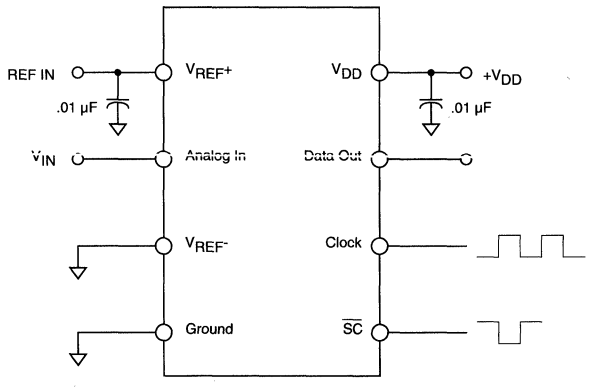
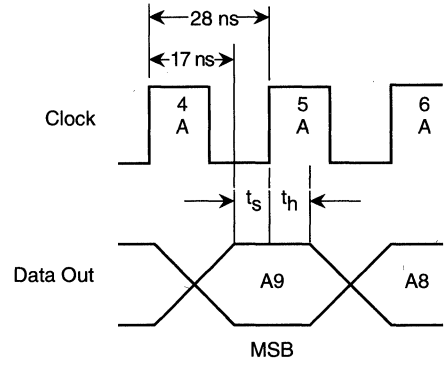


Figure 5 - Data Set-Up and Hold Times for 35 MHz Clock



t_s = 11 ns t_h = 16 ns

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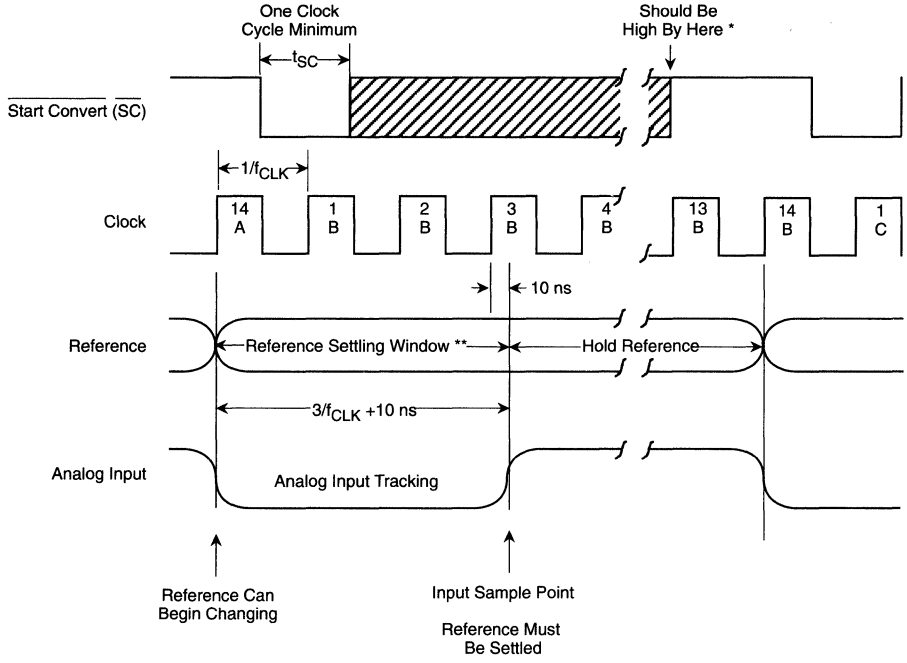
Figure 6 - Analog Input Track-and-Hold Timing and Reference Settling-and-Hold Timing

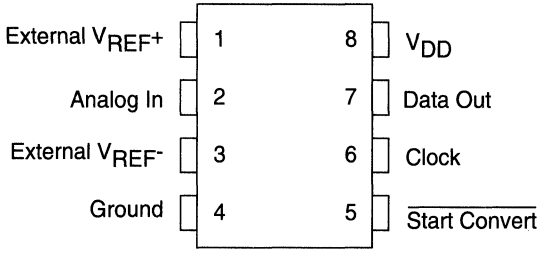


14 Cycles per Conversion Example

* Should be high by the rising edge of clock 13 to ensure that internal logic will be ready for the next start convert when operating in synchronous mode.

** The reference settling window can be extended by adding extra clocks per conversion cycle. The example shown is the minimum number of clocks required (14) per conversion cycle.

PIN ASSIGNMENTS



PIN FUNCTIONS

NAME	FUNCTION
Analog In	Analog signal input
Start Convert	Start Convert. A high-to-low transition on this input begins conversion cycle and enables serial data output
Clock	Clock that drives A/D conversion cycle and the synchronous serial data output
Data Out	Serial Data. Tri-state serial data output for the A/D result driven by the CLOCK input
External V_{REF+}	External voltage reference for top of reference ladder
External V_{REF-}	External voltage reference for bottom of reference ladder
V_{DD}	Analog & Digital +3.3 V to +5 V Power Supply Input
GND	Analog & Digital Ground

LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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SIGNAL PROCESSING TECHNOLOGIES

SPT7835

10-BIT, 5 MSPS, 75 mW A/D CONVERTER

3

FEATURES

- Monolithic 5 MSPS Converter
- 75 mW Power Dissipation
- On-Chip Track-and-Hold
- +Single 5 V Power Supply
- TTL/CMOS Outputs
- 5 pF Input Capacitance
- Low Cost
- Tri-State Output Buffers
- High ESD Protection: 3,500 V Minimum

APPLICATIONS

- All High-Speed Applications Where Low Power Dissipation is Required
- Video Imaging
- Medical Imaging
- IR Imaging
- Scanners
- Digital Communications

GENERAL DESCRIPTION

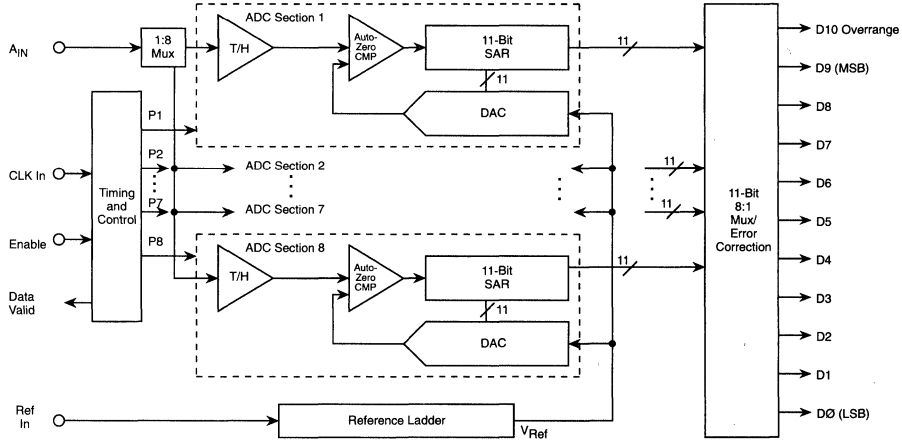
The SPT7835 is a 10-bit monolithic, low cost, ultra-low power analog-to-digital converter capable of minimum word rates of 5 MSPS. The on-chip track-and-hold function assures very good dynamic performance without the need for external components. The input drive requirements are minimized due to the SPT7835's low input capacitance of only 5 pF.

Power dissipation is extremely low at only 75 mW typical at 5 MSPS with a power supply of +5.0 V. The SPT7835 is pin-compatible with the entire family of SPT 10-bit, CMOS converters (SPT7835/40/50/55/60) which simplifies upgrades.

The SPT7835 has incorporated proprietary circuit design (*) and CMOS processing technologies to achieve its advanced performance. Inputs and outputs are TTL/CMOS-compatible to interface with TTL/CMOS-logic systems. Output data format is straight binary.

The SPT7835 is available in 28-lead 300 mil cerdip and PDIP, 28-lead SOIC and 32-lead small (7 mm square) TQFP packages over the temperature range of 0 to 70 °C. Die are also available. For extended temperature ranges and /883 processing requirements, consult the factory.

BLOCK DIAGRAM



*** Patent pending.**

ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages

AV_{DD} ..... +6 V
DV_{DD} ..... +6 V

Input Voltages

Analog Input ..... -0.5 V to AV_{DD} +0.5 V
V_{REF} ..... 0 to AV_{DD}
CLK Input ..... V_{DD}
AV_{DD} - DV_{DD} ..... ±100 mV
AGND - DGND ..... ±100 mV

Output

Digital Outputs ..... 10 mA

Temperature

Operating Temperature ..... 0 to 70 °C
Junction Temperature ..... 175 °C
Lead Temperature, (soldering 10 seconds) ..... 300 °C
Storage Temperature ..... -65 to +150 °C

Note: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

T_A=25 °C, AV_{DD} = DV_{DD} = +5.0 V, V_{IN} = 0 to 4 V, f_{CLK} = 10 MHz, f_S = 5 MSPS, V_{RHS} = 4.0 V, V_{RLS} = 0.0 V, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
Resolution			10			Bits
DC Accuracy						
Integral Nonlinearity		I		±1.0		LSB
Differential Nonlinearity		I		±0.5		LSB
No Missing Codes		I		Guaranteed		
Analog Input						
Input Voltage Range		I	V_{RLS}		V_{RHS}	V
Input Resistance		I	250			kΩ
Input Capacitance		V		5.0		pF
Input Bandwidth	(Small Signal)	V		100		MHz
Offset		V		±2.0		LSB
Gain Error		V		±2.0		LSB
Reference Input						
Resistance		I	400	500	600	Ω
Bandwidth		V	100	150		MHz
Voltage Range						
V_{RLS}		IV	0	-	2.0	V
V_{RHS}		IV	3.0	-	AV_{DD}	V
V_{RHS} - V_{RLS}		V	1.0	4.0	5.0	V
$\Delta(V_{RHF} - V_{RHS})$		V		90		mV
$\Delta(V_{RLS} - V_{RLF})$		V		75		mV
Reference Settling Time						
V_{RHS}		V		15		Clock Cycles
V_{RLS}		V		20		Clock Cycles
Conversion Characteristics						
Maximum Conversion Rate		I	5			MHz
Minimum Conversion Rate		IV	2			MHz
Pipeline Delay (Latency)		IV			12	Clock Cycles
Aperture Delay Time		V		5		ns
Aperture Jitter Time		V		10		ps
Dynamic Performance						
Effective Number of Bits						
f_{IN}=500 kHz		I		9.2		Bits
f_{IN}=1 MHz		I		9.2		Bits

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ELECTRICAL SPECIFICATIONS

T_A=25 °C, AV_{DD} = DV_{DD} = +5.0 V, V_{IN} = 0 to 4 V, f_{CLK} = 10 MHz, f_S = 5 MSPS, V_{RHS} = 4.0 V, V_{RLS} = 0.0 V, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
Dynamic Performance						
Signal-to-Noise Ratio (without Harmonics)						
f_{IN}=500 kHz		I	54	59		dB
f_{IN}=1 MHz		I	54	59		dB
Harmonic Distortion						
f_{IN}=500 kHz		I	59	63		dB
f_{IN}=1 MHz		I	59	63		dB
Signal-to-Noise and Distortion (SINAD)						
f_{IN}=500 kHz		I	52	57		dB
f_{IN}=1 MHz		I	52	57		dB
Spurious Free Dynamic Range		V		63		dB
Differential Phase		V		TBD		Degree
Differential Gain		V		TBD		%
Intermodulation Distortion		V		TBD		dB
Digital Inputs						
Logic "1" Voltage		I	2.0			V
Logic "0" Voltage		I			0.8	V
Maximum Input Current Low		I	-10		+10	µA
Maximum Input Current High		I	-10		+10	µA
Input Capacitance		V		5		pF
Digital Outputs						
Logic "1" Voltage	(I_{OH}=0.5 mA)	I	3.5			V
Logic "0" Voltage	(I_{OL}=1.6 mA)	I			0.4	V
t_{RISE}	15 pF load	V		10		ns
t_{FALL}	15 pF load	V		10		ns
Output Enable to Data Output Delay	20 pF load, T_A = +25 °C	V		10		ns
	50 pF load over temp.	V		22		ns
Power Supply Requirements						
Voltages	DV_{DD}	I	4.75	5.0	5.25	V
	AV_{DD}	I	4.75	5.0	5.25	V
Currents	AI_{DD}	I		9	12	mA
	DI_{DD}	I		6	10	mA
Power Dissipation	f_{IN}=1 MHz	I		75	110	mW

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions: All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests; therefore, $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

Figure 1A: Timing Diagram 1

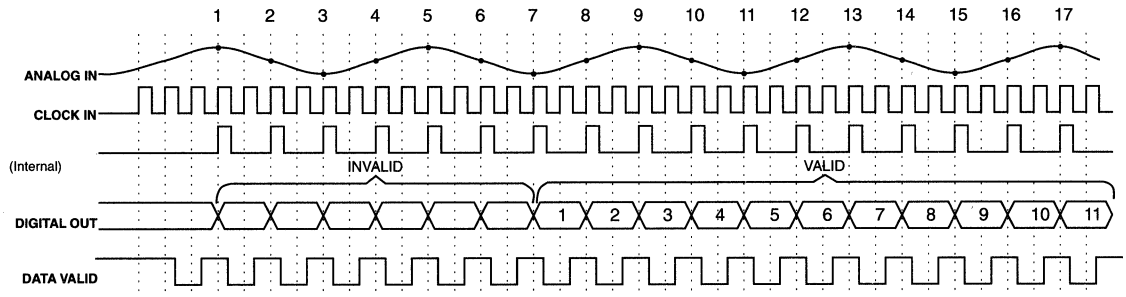

Figure 1B: Timing Diagram 2

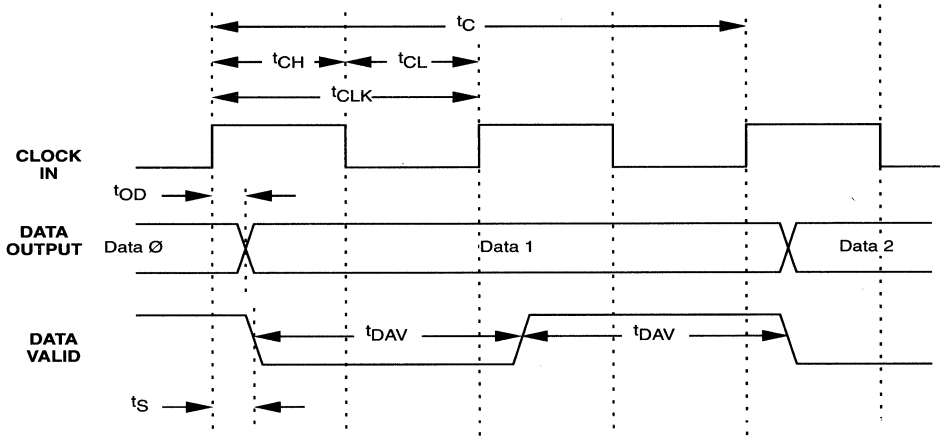

Table 1 - Timing Parameters

DESCRIPTION	PARAMETERS	MIN	TYP	MAX	UNITS
Conversion Time	t_c	2*t_{CLK}			ns
Clock Period	t_{CLK}	100			ns
Clock High Duty Cycle	t_{CH}	40	50	60	%
Clock Low Duty Cycle	t_{CL}	40	50	60	%
Output Delay	t_{OD}	15	20	25	ns
DAV Pulse Width	t_{DAV}		t_{CLK}		ns
Clock to DAV	t_S	16	21	26	ns

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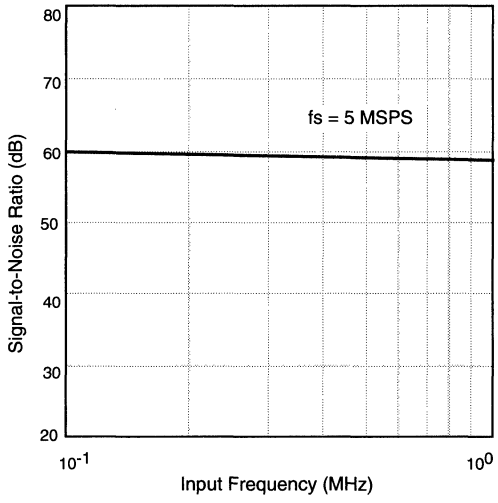
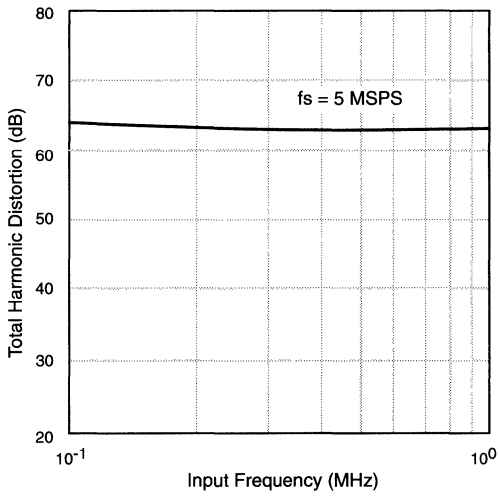
TYPICAL PERFORMANCE CHARACTERISTICS

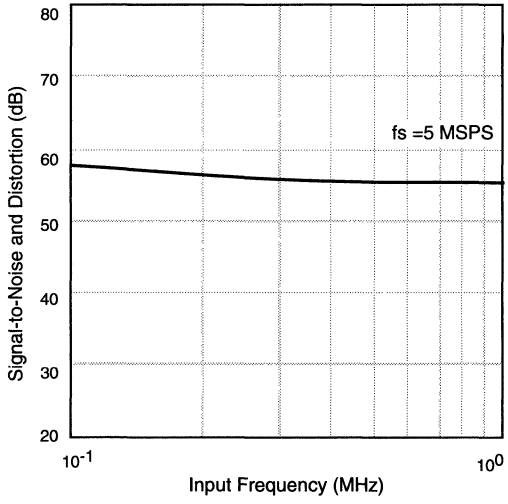
SNR vs Input Frequency



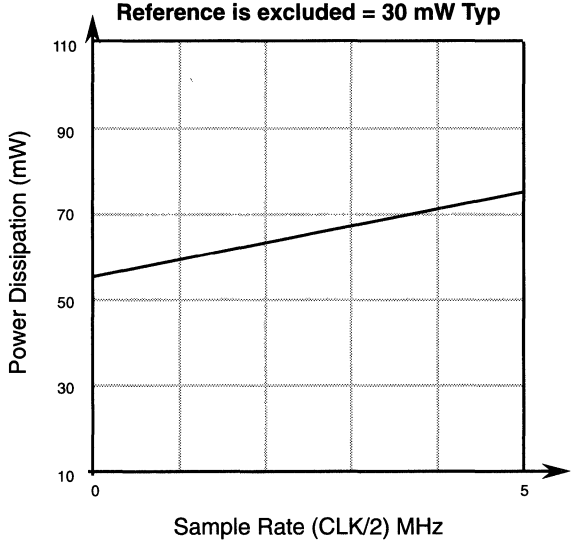
THD vs Input Frequency



SINAD vs Input Frequency



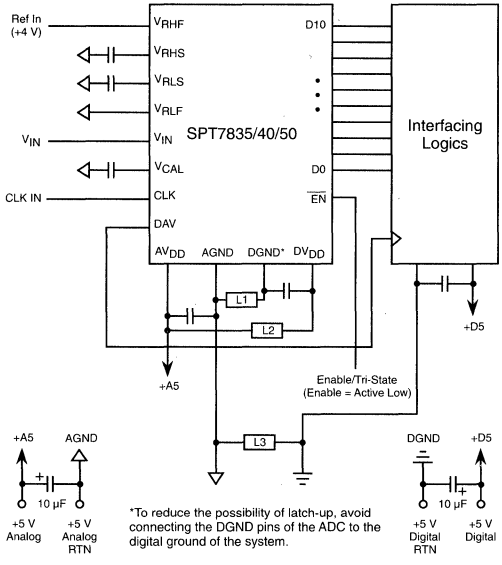
Total Power Dissipation Vs. Sample Rate
Reference is excluded = 30 mW Typ



TYPICAL INTERFACE CIRCUIT

Figure 1 shows the typical interface requirements when using the SPT7835 in normal circuit operation. To reduce the possibility of latch-up, avoid connecting the DGND pins of the ADC to the digital ground of the system. The following sections provide descriptions of the major functions and outline critical performance criteria to consider for achieving the optimal device performance.

Figure 1 - Typical Interface Circuit



NOTES: 1) L3 is to be located as closely to the device as possible.
2) There should be no additional connections to the right of L1 and L2.
3) All capacitors are 0.1 µF surface-mount unless otherwise specified.
4) L1, L2 and L3 are 10 µH inductors or ferrite beads.

POWER SUPPLIES AND GROUNDING

SPT suggests that both the digital and the analog supply voltages on the SPT7835 be derived from a single analog supply as shown in figure 1. A separate digital supply should be used for all interface circuitry. SPT suggests using this power supply configuration to prevent a possible latch-up condition on power up.

OPERATING DESCRIPTION

The general architecture for the CMOS ADC is shown in the block diagram. The design contains eight identical successive approximation ADC sections, all operating in parallel, a 16-phase clock generator, an 11-bit 8:1 digital output multiplexer, correction logic, and a voltage reference generator which provides common reference levels for each ADC section.

The high sample rate is achieved by using multiple SAR ADC sections in parallel, each of which samples the input signal in sequence. Each ADC uses 16 clock cycles to complete a conversion. The clock cycles are allocated as follows:

Clock	Operation
1	Reference zero sampling
2	Auto-zero comparison
3	Auto-calibrate comparison
4	Input sample
5-15	11-bit SAR conversion
16	Data transfer

The 16 phase clock, which is derived from the input clock, synchronizes these events. The timing signals for adjacent ADC sections are shifted by two clock cycles so that the analog input is sampled on every other cycle of the input clock by exactly one ADC section. After 16 clock periods, the timing cycle repeats. The sample rate for the configuration is one-half of the clock rate, e.g., for a 10 MHz clock rate, the input sample rate is 5 MHz. The latency from analog input sample to the corresponding digital output is 12 clock cycles.

- Since only eight comparators are used, a huge power savings is realized.
- The auto-zero operation is done using a closed loop system that uses multiple samples of the comparators response to a reference zero.
- The auto-calibrate operation, which calibrates the gain of the MSB reference and the LSB reference, is also done with a closed loop system. Multiple samples of the gain error are integrated to produce a calibration voltage for each ADC section.
- Capacitive displacement currents, which can induce sampling error, are minimized since only one comparator samples the input during a clock cycle.
- The total input capacitance is very low since sections of the converter which are not sampling the signal are isolated from the input by transmission gates.

VOLTAGE REFERENCE

The SPT7835 requires the use of a single external voltage reference for driving the high side of the reference ladder. It must be within the range of 3 V to 5 V. The lower side of the ladder is typically tied to AGND (0.0 V), but can be run up to 2.0 V with a second reference. The analog input voltage range will track the total voltage difference measured between the ladder sense lines, V_{RHS} and V_{RLS}.

Force and sense taps are provided to ensure accurate and stable setting of the upper and lower ladder sense line voltages across part-to-part and temperature variations. By using the configuration shown in figure 2, offset and gain errors of less than ±2 LSB can be obtained.

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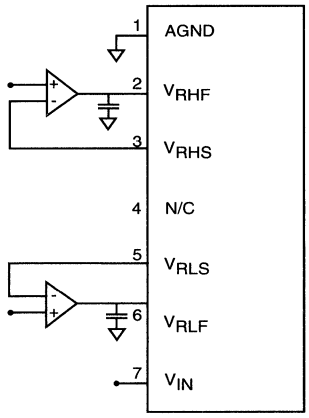
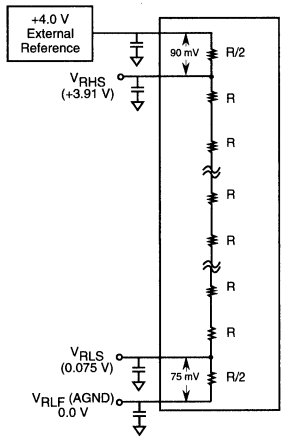
Figure 2 - Ladder Force/Sense Circuit



All capacitors are 0.01 µF

Figure 3 - Reference Ladder



R=30 Ω (typ)
All capacitors are 0.01 µF

In cases where wider variations in offset and gain can be tolerated, V_{Ref} can be tied directly to V_{RHF} and AGND can be tied directly to V_{RLF} as shown in figure 3. Decouple force and sense lines to AGND with a .01 µF capacitor (chip cap preferred) to minimize high-frequency noise injection. If this simplified configuration is used, the following considerations should be taken into account:

The reference ladder circuit shown in figure 3 is a simplified representation of the actual reference ladder with force and sense taps shown. Due to the actual internal structure of the ladder, the voltage drop from V_{RHF} to V_{RHS} is not equivalent to the voltage drop from V_{RLF} to V_{RLS}.

Typically, the top side voltage drop for V_{RHF} to V_{RHS} will equal:

$V_{RHF} - V_{RHS}$ = 2.25 % of ($V_{RHF} - V_{RLF}$) (typical),

and the bottom side voltage drop for V_{RLS} to V_{RLF} will equal:

$V_{RLS} - V_{RLF}$ = 1.9 % of ($V_{RHF} - V_{RLF}$) (typical).

Figure 3 shows an example of expected voltage drops for a specific case. Vref of 4.0 V is applied to V_{RHF} and V_{RLF} is tied to AGND. A 90 mV drop is seen at V_{RHS} (= 3.91 V) and a 75 mV increase is seen at V_{RLS} (= 0.075 V).

ANALOG INPUT

V_{IN} is the analog input. The input voltage range is from V_{RLS} to V_{RHS} (typically 4.0 V) and will scale proportionally with respect to the voltage reference. (See voltage reference section.)

The drive requirements for the analog inputs are very minimal when compared to most other converters due to the SPT7835's extremely low input capacitance of only 5 pF and very high input resistance of 250 kΩ.

The analog input should be protected through a series resistor and diode clamping circuit as shown in figure 4.

CALIBRATION

The SPT7835 uses an auto calibration scheme to ensure 10-bit accuracy over time and temperature. Gain and offset errors are continually adjusted to 10-bit accuracy during device operation. This process is completely transparent to the user.

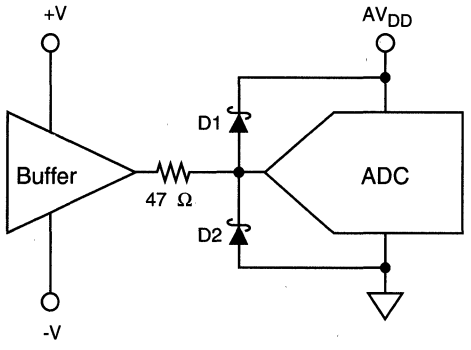
Upon power-up, the SPT7835 begins its calibration algorithm. In order to achieve the calibration accuracy required, the offset and gain adjustment step size is a fraction of a 10-bit LSB. Since the calibration algorithm is an oversampling process, a minimum of 10k clock cycles are required. This results in a minimum calibration time upon power-up of 1 msec for a 5 MHz sample rate. Once calibrated, the SPT7835 remains calibrated over time and temperature.

Since the calibration cycles are initiated on the rising edge of the clock, the clock must be continuously applied for the SPT7835 to remain in calibration.

INPUT PROTECTION

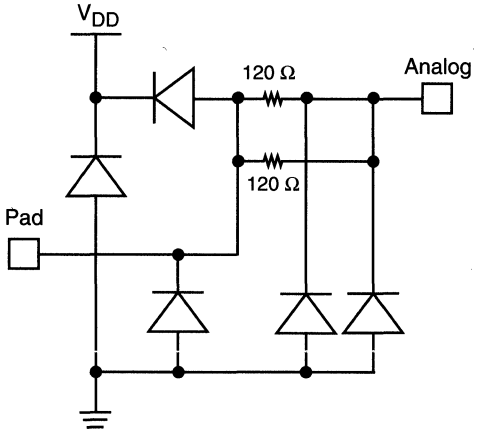
All I/O pads are protected with an on-chip protection circuit shown in figure 5. This circuit provides ESD robustness to 3.5 kV and prevents latch-up under severe discharge conditions without degrading analog transition times.

Figure 4 - Recommended Input Protection Circuit



D1 = D2 = Hewlett Packard HP5712 or equivalent

Figure 5 - On-Chip Protection Circuit



POWER SUPPLY SEQUENCING CONSIDERATIONS

All logic inputs should be held low until power to the device has settled to the specific tolerances. Avoid power decoupling networks with large time constants which could delay V_{DD} power to the device.

CLOCK INPUT

The SPT7835 is driven from a single-ended TTL-input clock. Because the pipelined architecture operates on the rising edge of the clock input, the device can operate over a wide range of input clock duty cycles without degrading the dynamic performance. **The device's sample rate is 1/2 of the input clock frequency. (See timing diagram.)**

DIGITAL OUTPUTS

The format of the output data (D0-D9) is straight binary. (See table 2.) The outputs are latched on the rising edge of CLK. These outputs can be switched into a tri-state mode by bringing $\overline{EN}$ high.

Table 2 - Output Data Information

ANALOG INPUT	OVERRANGE D10	OUTPUT CODE D9-D0
+F.S. + 1/2 LSB	1	11 1111 1111
+F.S. -1/2 LSB	0	11 1111 111Ø
+1/2 F.S.	0	ØØ ØØØØ ØØØØ
+1/2 LSB	0	OO OOOO OOOØ
0.0 V	0	OO OOOO OOOO

(Ø indicates the flickering bit between logic 0 and 1).

OVERRANGE OUTPUT

The OVERRANGE OUTPUT (D10) is an indication that the analog input signal has exceeded the positive full scale input voltage by 1 LSB. When this condition occurs, D10 will switch to logic 1. All other data outputs (D0 to D9) will remain at logic 1 as long as D10 remains at logic 1. This feature makes it possible to include the SPT7835 into higher resolution systems.

EVALUATION BOARD

The EB7835 Evaluation Board is available to aid designers in demonstrating the full performance of the SPT7835. This board includes a reference circuit, clock driver circuit, output data latches and an on-board reconstruction of the digital data. An application note describing the operation of this board as well as information on the testing of the SPT7835 is also available. Contact the factory for price and availability.

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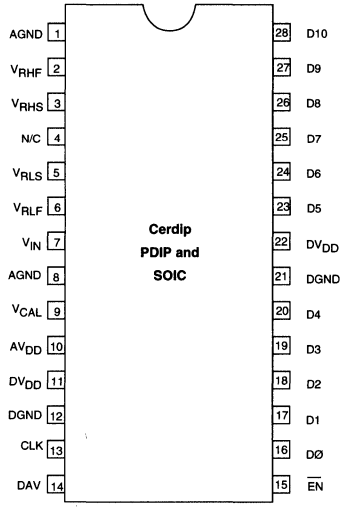
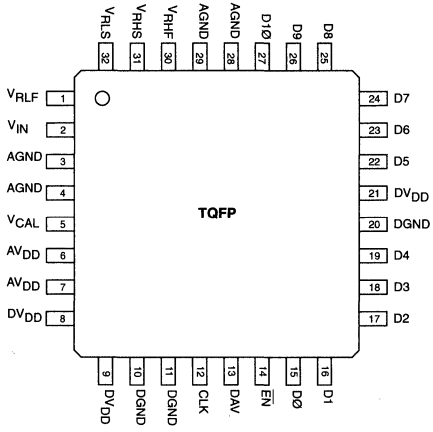
PIN ASSIGNMENTS





PIN FUNCTIONS

NAME	FUNCTION
AGND	Analog Ground
V_{RHF}	Reference High Force
V_{RHS}	Reference High Sense
V_{RLS}	Reference Low Sense
V_{RLF}	Reference Low Force
V_{CAL}	Calibration Reference
V_{IN}	Analog Input
AV_{DD}	Analog V_{DD}
DV_{DD}	Digital V_{DD}
DGND	Digital Ground
CLK	Input Clock f_{CLK} =fs (TTL)
$\overline{EN}$	Output Enable
D0-9	Tri-State Data Output, (DØ=LSB)
D10	Tri-State Output Overrange
DAV	Data Valid Output

LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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SIGNAL PROCESSING TECHNOLOGIES

SPT7840

10-BIT, 10 MSPS, 100 mW A/D CONVERTER

3

FEATURES

- Monolithic 10 MSPS Converter
- 100 mW Power Dissipation
- On-Chip Track-and-Hold
- Single +5 V Power Supply
- TTL/CMOS Outputs
- 5 pF Input Capacitance
- Low Cost
- Tri-State Output Buffers
- High ESD Protection: 3,500 V Minimum

APPLICATIONS

- All High-Speed Applications Where Low Power Dissipation is Required
- Video Imaging
- Medical Imaging
- IR Imaging
- Scanners
- Digital Communications

GENERAL DESCRIPTION

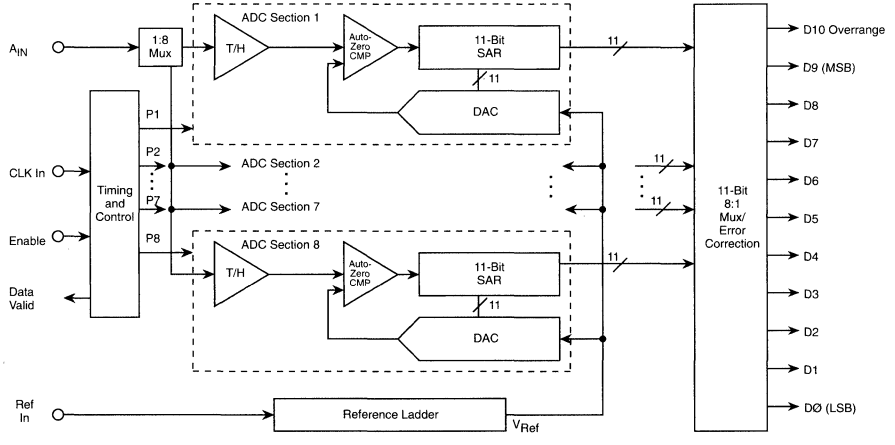
The SPT7840 is a 10-bit monolithic, low cost, ultra-low power analog-to-digital converter capable of minimum word rates of 10 MSPS. The on-chip track-and-hold function assures very good dynamic performance without the need for external components. The input drive requirements are minimized due to the SPT7840's low input capacitance of only 5 pF.

Power dissipation is extremely low at only 100 mW typical (120 mW maximum) at 10 MSPS with a power supply of +5.0 V. The SPT7840 is pin-compatible with the entire family of SPT 10-bit, CMOS converters (SPT7835/40/50/55/60) which simplifies upgrades.

The SPT7840 has incorporated proprietary circuit design (*) and CMOS processing technologies to achieve its advanced performance. Inputs and outputs are TTL/CMOS-compatible to interface with TTL/CMOS-logic systems. Output data format is straight binary.

The SPT7840 is available in 28-lead 300 mil cerdip and PDIP, 28-lead SOIC and 32-lead small (7 mm square) TQFP packages over the temperature range of 0 to 70 °C. Die are also available. For extended temperature ranges and /883 processing requirements, consult the factory.

BLOCK DIAGRAM



*** Patent pending.**

ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages

AV_{DD} ..... +6 V
DV_{DD} ..... +6 V

Input Voltages

Analog Input ..... -0.5 V to AV_{DD} +0.5 V
V_{Ref} ..... 0 to AV_{DD}
CLK Input ..... V_{DD}
AV_{DD} - DV_{DD} ..... ±100 mV
AGND - DGND ..... ±100 mV

Output

Digital Outputs ..... 10 mA

Temperature

Operating Temperature ..... 0 to 70 °C
Junction Temperature ..... 175 °C
Lead Temperature, (soldering 10 seconds) ..... 300 °C
Storage Temperature ..... -65 to +150 °C

Note: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

T_A=25 °C, AV_{DD} = DV_{DD} = +5.0 V, V_{IN} = 0 to 4 V, f_{CLK}=20 MHz, f_S = 10 MSPS, V_{RHS} = 4.0 V, V_{RLS} = 0.0 V, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
Resolution			10			Bits
DC Accuracy						
Integral Nonlinearity		I		±1.0		LSB
Differential Nonlinearity		I		±0.5		LSB
No Missing Codes		I		Guaranteed		
Analog Input						
Input Voltage Range		I	V_{RLS}		V_{RHS}	V
Input Resistance		I	250			kΩ
Input Capacitance		V		5.0		pF
Input Bandwidth	(Small Signal)	V		100		MHz
Offset		V		±2.0		LSB
Gain Error		V		±2.0		LSB
Reference Input						
Resistance		I	400	500	600	Ω
Bandwidth		V	100	150		MHz
Voltage Range						
V_{RLS}		IV	0	-	2.0	V
V_{RHS}		IV	3.0	-	AV_{DD}	V
V_{RHS} - V_{RLS}		V	1.0	4.0	5.0	V
$\Delta(V_{RHF} - V_{RHS})$		V		90		mV
$\Delta(V_{RLS} - V_{RLF})$		V		75		mV
Reference Settling Time						
V_{RHS}		V		15		Clock Cycles
V_{RLS}		V		20		Clock Cycles
Conversion Characteristics						
Maximum Conversion Rate		I	10			MHz
Minimum Conversion Rate		IV	2			MHz
Pipeline Delay (Latency)		IV			12	Clock Cycles
Aperture Delay Time		V		5		ns
Aperture Jitter Time		V		10		ps
Dynamic Performance						
Effective Number of Bits						
f_{IN}=1 MHz		I		9.1		Bits
f_{IN}=3.58 MHz		I		9.0		Bits
f_{IN}=5 MHz		I		9.0		Bits

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ELECTRICAL SPECIFICATIONS

T_A=25 °C, AV_{DD} = DV_{DD} = +5.0 V, V_{IN} = 0 to 4 V, f_{CLK}=20 MHz, f_S = 10 MSPS, V_{RHS} = 4.0 V, V_{RLS} = 0.0 V, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
Dynamic Performance						
Signal-to-Noise Ratio (without Harmonics)						
f_{IN}=1 MHz		I	53	58		dB
f_{IN}=3.58 MHz		I	52	57		dB
f_{IN}=5 MHz		I	52	57		dB
Harmonic Distortion						
f_{IN}=1 MHz		I	59	63		dB
f_{IN}=3.58 MHz		I	56	60		dB
f_{IN}=5 MHz		I	56	59		dB
Signal-to-Noise and Distortion (SINAD)						
f_{IN}=1 MHz		I	52	57		dB
f_{IN}=3.58 MHz		I	51	56		dB
f_{IN}=5 MHz		I	51	56		dB
Spurious Free Dynamic Range		V		63		dB
Differential Phase		V		TBD		Degree
Differential Gain		V		TBD		%
Intermodulation Distortion		V		TBD		dB
Digital Inputs						
Logic "1" Voltage		I	2.0			V
Logic "0" Voltage		I			0.8	V
Maximum Input Current Low		I	-10		+10	µA
Maximum Input Current High		I	-10		+10	µA
Input Capacitance		V		5		pF
Digital Outputs						
Logic "1" Voltage	(I_{OH}=0.5 mA)	I	3.5			V
Logic "0" Voltage	(I_{OL}=1.6 mA)	I			0.4	V
t_{RISE}	15 pF load	V		10		ns
t_{FALL}	15 pF load	V		10		ns
Output Enable to Data Output Delay	20 pF load, T_A = +25 °C	V		10		ns
	50 pF load over temp.	V		22		ns
Power Supply Requirements						
Voltages	DV_{DD}	I	4.75	5.0	5.25	V
	AV_{DD}	I	4.75	5.0	5.25	V
Currents	AI_{DD}	I		9	12	mA
	DI_{DD}	I		11	12	mA
Power Dissipation	f_{IN}=1 MHz	I		100	120	mW

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions: All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests; therefore, $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

Figure 1A: Timing Diagram 1

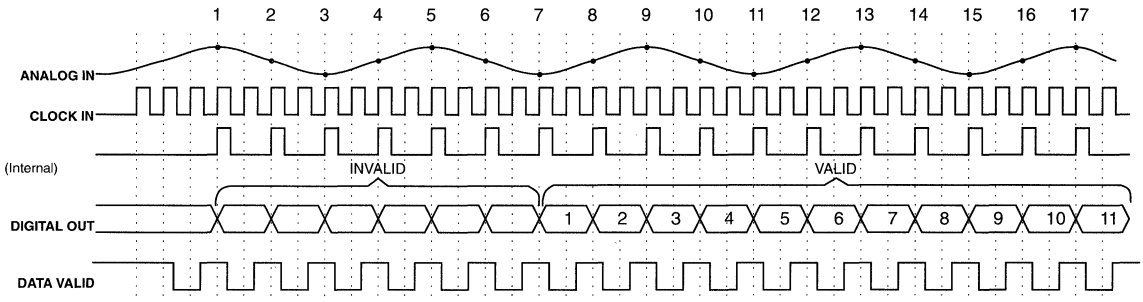

Figure 1B: Timing Diagram 2

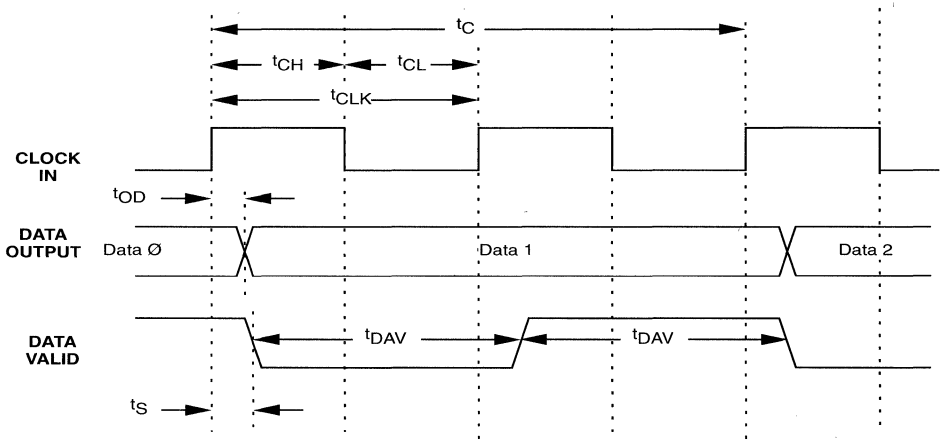

Table 1 - Timing Parameters

DESCRIPTION	PARAMETERS	MIN	TYP	MAX	UNITS
Conversion Time	t_c	2*t_{CLK}			ns
Clock Period	t_{CLK}	50			ns
Clock High Duty Cycle	t_{CH}	40	50	60	%
Clock Low Duty Cycle	t_{CL}	40	50	60	%
Output Delay	t_{OD}	15	20	25	ns
DAV Pulse Width	t_{DAV}		t_{CLK}		ns
Clock to DAV	t_S	16	21	26	ns

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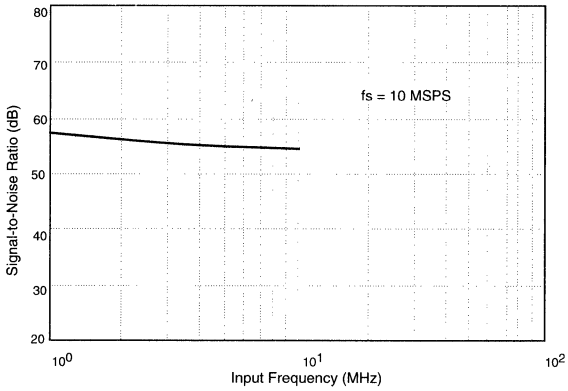
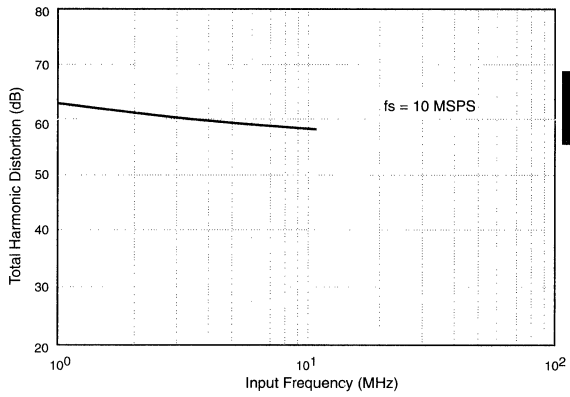
TYPICAL PERFORMANCE CHARACTERISTICS

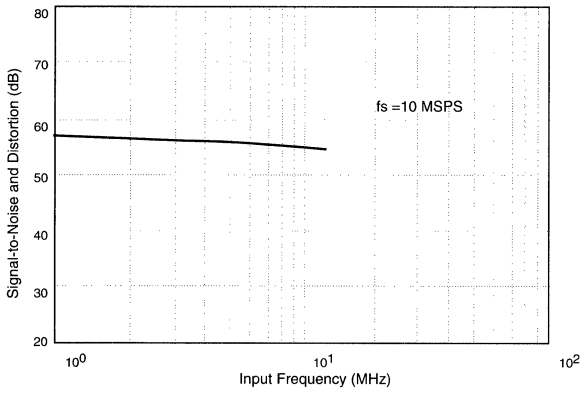
SNR vs Input Frequency



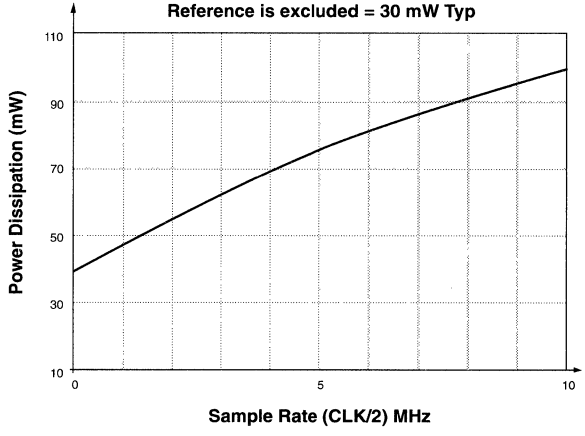
THD vs Input Frequency



SINAD vs Input Frequency



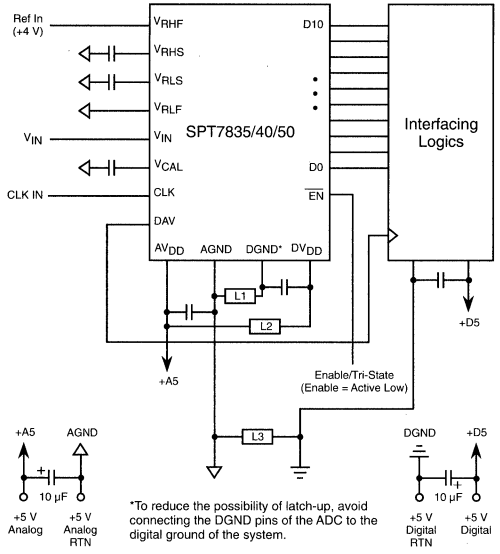
Total Power Dissipation vs Sample Rate
Reference is excluded = 30 mW Typ



TYPICAL INTERFACE CIRCUIT

Figure 1 shows the typical interface requirements when using the SPT7840 in normal circuit operation. To reduce the possibility of latch-up, avoid connecting the DGND pins of the ADC to the digital ground of the system. The following sections provide descriptions of the major functions and outline critical performance criteria to consider for achieving the optimal device performance.

Figure 1 - Typical Interface Circuit



NOTES: 1) L3 is to be located as closely to the device as possible.
2) There should be no additional connections to the right of L1 and L2.
3) All capacitors are 0.1 µF surface-mount unless otherwise specified.
4) L1, L2 and L3 are 10 µH inductors or ferrite beads.

POWER SUPPLIES AND GROUNDING

SPT suggests that both the digital and the analog supply voltages on the SPT7840 be derived from a single analog supply as shown in figure 1. A separate digital supply should be used for all interface circuitry. SPT suggests using this power supply configuration to prevent a possible latch-up condition on power up.

OPERATING DESCRIPTION

The general architecture for the CMOS ADC is shown in the block diagram. The design contains eight identical successive approximation ADC sections, all operating in parallel, a 16-phase clock generator, an 11-bit 8:1 digital output multiplexer, correction logic, and a voltage reference generator which provides common reference levels for each ADC section.

The high sample rate is achieved by using multiple SAR ADC sections in parallel, each of which samples the input signal in sequence. Each ADC uses 16 clock cycles to complete a conversion. The clock cycles are allocated as follows:

Clock	Operation
1	Reference zero sampling
2	Auto-zero comparison
3	Auto-calibrate comparison
4	Input sample
5-15	11-bit SAR conversion
16	Data transfer

The 16 phase clock, which is derived from the input clock, synchronizes these events. The timing signals for adjacent ADC sections are shifted by two clock cycles so that the analog input is sampled on every other cycle of the input clock by exactly one ADC section. After 16 clock periods, the timing cycle repeats. The sample rate for the configuration is one-half of the clock rate, e.g., for a 20 MHz clock rate, the input sample rate is 10 MHz. The latency from analog input sample to the corresponding digital output is 12 clock cycles.

- Since only eight comparators are used, a huge power savings is realized.
- The auto-zero operation is done using a closed loop system that uses multiple samples of the comparators response to a reference zero.
- The auto-calibrate operation, which calibrates the gain of the MSB reference and the LSB reference, is also done with a closed loop system. Multiple samples of the gain error are integrated to produce a calibration voltage for each ADC section.
- Capacitive displacement currents, which can induce sampling error, are minimized since only one comparator samples the input during a clock cycle.
- The total input capacitance is very low since sections of the converter which are not sampling the signal are isolated from the input by transmission gates.

VOLTAGE REFERENCE

The SPT7840 requires the use of a single external voltage reference for driving the high side of the reference ladder. It must be within the range of 3 V to 5 V. The lower side of the ladder is typically tied to AGND (0.0 V), but can be run up to 2.0 V with a second reference. The analog input voltage range will track the total voltage difference measured between the ladder sense lines, V_{RHS} and V_{RLS}.

Force and sense taps are provided to ensure accurate and stable setting of the upper and lower ladder sense line voltages across part-to-part and temperature variations. By using the configuration shown in figure 2, offset and gain errors of less than ±2 LSB can be obtained.

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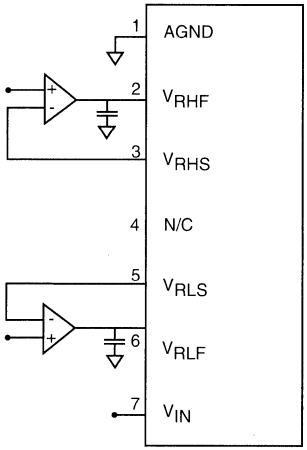
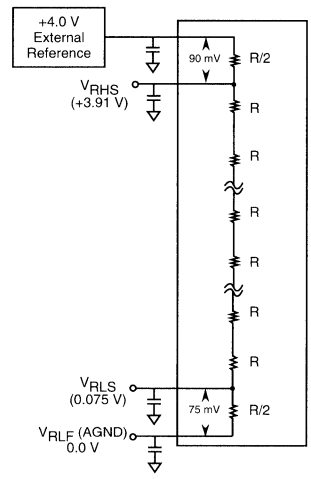
Figure 2 - Ladder Force/Sense Circuit



All capacitors are 0.01 µF

Figure 3 - Reference Ladder



In cases where wider variations in offset and gain can be tolerated, V_{Ref} can be tied directly to V_{RHF} and AGND can be tied directly to V_{RLF} as shown in figure 3. Decouple force and sense lines to AGND with a .01 µF capacitor (chip cap preferred) to minimize high-frequency noise injection. If this simplified configuration is used, the following considerations should be taken into account:

The reference ladder circuit shown in figure 3 is a simplified representation of the actual reference ladder with force and sense taps shown. Due to the actual internal structure of the ladder, the voltage drop from V_{RHF} to V_{RHS} is not equivalent to the voltage drop from V_{RLF} to V_{RLS}.

Typically, the top side voltage drop for V_{RHF} to V_{RHS} will equal:

$V_{RHF} - V_{RHS} = 2.25\%$ of $(V_{RHF} - V_{RLF})$ (typical),

and the bottom side voltage drop for V_{RLS} to V_{RLF} will equal:

$V_{RLS} - V_{RLF} = 1.9\%$ of $(V_{RHF} - V_{RLF})$ (typical).

Figure 3 shows an example of expected voltage drops for a specific case. VRef of 4.0 V is applied to V_{RHF} and V_{RLF} is tied to AGND. A 90 mV drop is seen at V_{RHS} (= 3.91 V) and a 75 mV increase is seen at V_{RLS} (= 0.075 V).

ANALOG INPUT

V_{IN} is the analog input. The input voltage range is from V_{RLS} to V_{RHS} (typically 4.0 V) and will scale proportionally with respect to the voltage reference. (See voltage reference section.)

The drive requirements for the analog inputs are very minimal when compared to most other converters due to the SPT7840's extremely low input capacitance of only 5 pF and very high input resistance of 250 kΩ.

The analog input should be protected through a series resistor and diode clamping circuit as shown in figure 4.

CALIBRATION

The SPT7840 uses an auto calibration scheme to ensure 10-bit accuracy over time and temperature. Gain and offset errors are continually adjusted to 10-bit accuracy during device operation. This process is completely transparent to the user.

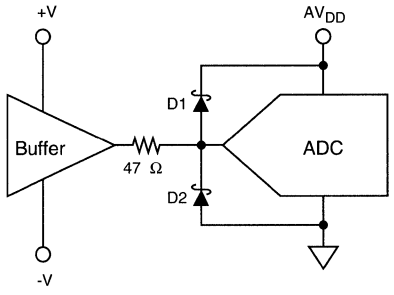
Upon power-up, the SPT7840 begins its calibration algorithm. In order to achieve the calibration accuracy required, the offset and gain adjustment step size is a fraction of a 10-bit LSB. Since the calibration algorithm is an oversampling process, a minimum of 10k clock cycles are required. This results in a minimum calibration time upon power-up of 500 µsec (for a 10 MHz sample rate). Once calibrated, the SPT7840 remains calibrated over time and temperature.

Since the calibration cycles are initiated on the rising edge of the clock, the clock must be continuously applied for the SPT7840 to remain in calibration.

INPUT PROTECTION

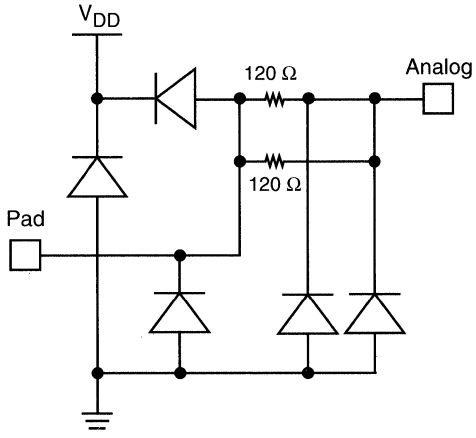
All I/O pads are protected with an on-chip protection circuit shown in figure 5. This circuit provides ESD robustness to 3.5 kV and prevents latch-up under severe discharge conditions without degrading analog transition times.

Figure 4 - Recommended Input Protection Circuit



D1 = D2 = Hewlett Packard HP5712 or equivalent

Figure 5 - On-Chip Protection Circuit



POWER SUPPLY SEQUENCING CONSIDERATIONS

All logic inputs should be held low until power to the device has settled to the specific tolerances. Avoid power decoupling networks with large time constants which could delay V_{DD} power to the device.

CLOCK INPUT

The SPT7840 is driven from a single-ended TTL-input clock. Because the pipelined architecture operates on the rising edge of the clock input, the device can operate over a wide range of input clock duty cycles without degrading the dynamic performance. *The device's sample rate is 1/2 of the input clock frequency. (See timing diagram.)*

DIGITAL OUTPUTS

The format of the output data (D0-D9) is straight binary. (See table 2.) The outputs are latched on the rising edge of CLK. These outputs can be switched into a tri-state mode by bringing $\overline{EN}$ high.

Table 2 - Output Data Information

ANALOG INPUT	OVERRANGE D10	OUTPUT CODE D9-D0
+F.S. + 1/2 LSB	1	11 1111 1111
+F.S. -1/2 LSB	0	11 1111 111Ø
+1/2 F.S.	0	ØØ ØØØØ ØØØØ
+1/2 LSB	0	OO OOOO OOOØ
0.0 V	0	OO OOOO OOOO

(Ø indicates the flickering bit between logic 0 and 1).

OVERRANGE OUTPUT

The OVERRANGE OUTPUT (D10) is an indication that the analog input signal has exceeded the positive full scale input voltage by 1 LSB. When this condition occurs, D10 will switch to logic 1. All other data outputs (D0 to D9) will remain at logic 1 as long as D10 remains at logic 1. This feature makes it possible to include the SPT7840 into higher resolution systems.

EVALUATION BOARD

The EB7840 Evaluation Board is available to aid designers in demonstrating the full performance of the SPT7840. This board includes a reference circuit, clock driver circuit, output data latches and an on-board reconstruction of the digital data. An application note describing the operation of this board as well as information on the testing of the SPT7840 is also available. Contact the factory for price and availability.

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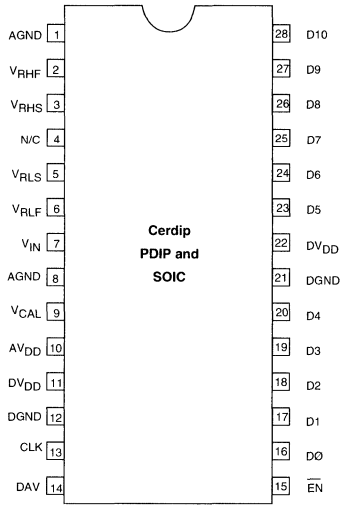
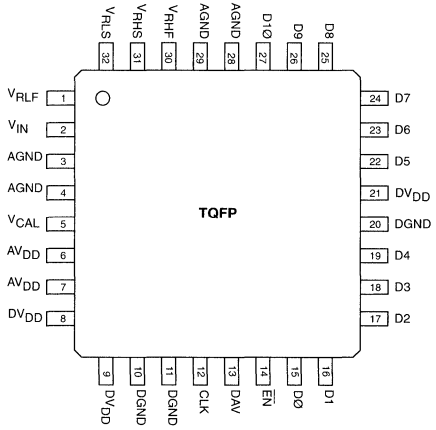
PIN ASSIGNMENTS





PIN FUNCTIONS

NAME	FUNCTION
AGND	Analog Ground
V_{RHF}	Reference High Force
V_{RHS}	Reference High Sense
V_{RLS}	Reference Low Sense
V_{RLF}	Reference Low Force
V_{CAL}	Calibration Reference
V_{IN}	Analog Input
AV_{DD}	Analog V_{DD}
DV_{DD}	Digital V_{DD}
DGND	Digital Ground
CLK	Input Clock f_{CLK} =fs (TTL)
$\overline{EN}$	Output Enable
D0-9	Tri-State Data Output, (DØ=LSB)
D10	Tri-State Output Overrange
DAV	Data Valid Output

LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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SIGNAL PROCESSING TECHNOLOGIES

SPT7850

10-BIT, 20 MSPS, 140 mW A/D CONVERTER

FEATURES

- Monolithic 20 MSPS Converter
- 140 mW Power Dissipation
- On-Chip Track-and-Hold
- Single +5 V Power Supply
- TTL/CMOS Outputs
- 5 pF Input Capacitance
- Low Cost
- Tri-State Output Buffers
- High ESD Protection: 3,500 V Minimum

APPLICATIONS

- All High-Speed Applications Where Low Power Dissipation is Required
- Video Imaging
- Medical Imaging
- IR Imaging
- Scanners
- Digital Communications

GENERAL DESCRIPTION

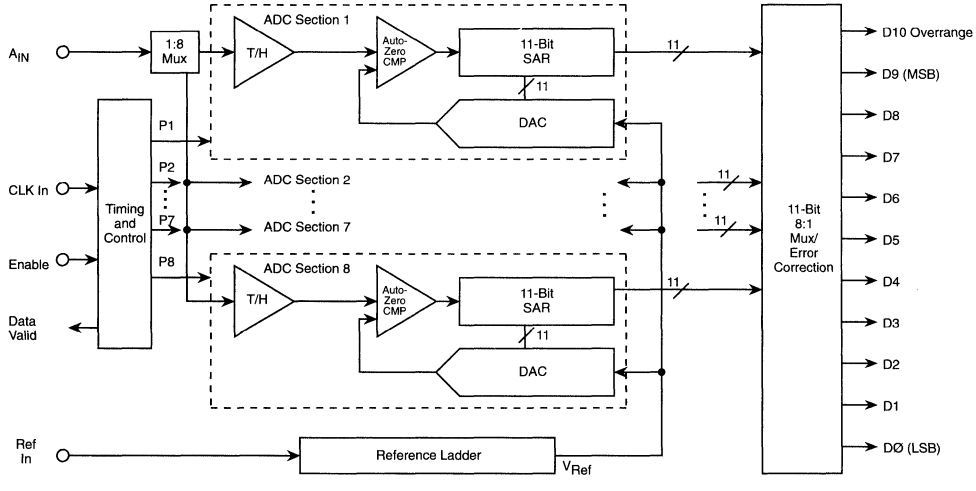
The SPT7850 is a 10-bit monolithic, low cost, ultra-low power analog-to-digital converter capable of minimum word rates of 20 MSPS. The on-chip track-and-hold function assures very good dynamic performance without the need for external components. The input drive requirements are minimized due to the SPT7850's low input capacitance of only 5 pF.

Power dissipation is extremely low at only 140 mW typical (165 mW maximum) at 20 MSPS with a power supply of +5.0 V. The SPT7850 is pin-compatible with the entire family of SPT 10-bit, CMOS converters (SPT7835/40/50/55/60) which simplifies upgrades.

The SPT7850 has incorporated proprietary circuit design (*) and CMOS processing technologies to achieve its advanced performance. Inputs and outputs are TTL/CMOS-compatible to interface with TTL/CMOS-logic systems. Output data format is straight binary.

The SPT7850 is available in 28-lead 300 mil cerdip and PDIP, 28-lead SOIC and 32-lead small (7 mm square) TQFP packages over the temperature range of 0 to 70 °C. For extended temperature ranges and /883 processing requirements, consult the factory.

BLOCK DIAGRAM



*** Patent pending.**

ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages
- AV_{DD} ..... +6 V
- DV_{DD} ..... +6 V

Input Voltages
- Analog Input ..... -0.5 V to AV_{DD} +0.5 V
- V_{REF} ..... 0 to AV_{DD}
- CLK Input ..... V_{DD}
- AV_{DD} - DV_{DD} ..... ±100 mV
- AGND - DGND ..... ±100 mV

Output
- Digital Outputs ..... 10 mA

Temperature
- Operating Temperature ..... 0 to 70 °C
- Junction Temperature ..... 175 °C
- Lead Temperature, (soldering 10 seconds) ..... 300 °C
- Storage Temperature ..... -65 to +150 °C

Note: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

T_A=25 °C, AV_{DD} = DV_{DD} = +5.0 V, V_{IN}=0 to 4 V, f_S=20 MSPS, f_{CLK}=40 MHz, V_{RHS}= 4.0 V, V_{RLS}=0.0 V, unless otherwise specified.

TEST PARAMETERS	TEST CONDITIONS	LEVEL	MIN	TYP	MAX	UNITS
Resolution			10			Bits
DC Accuracy						
Integral Nonlinearity		I		±1.0		LSB
Differential Nonlinearity		I		±0.5		LSB
No Missing Codes		I		Guaranteed		
Analog Input						
Input Voltage Range		I	V_{RLS}		V_{RHS}	V
Input Resistance		I	250			kΩ
Input Capacitance		V		5.0		pF
Input Bandwidth	(Small Signal)	V		100		MHz
Offset		V		±2.0		LSB
Gain Error		V		±2.0		LSB
Reference Input						
Resistance		I	400	500	600	Ω
Bandwidth		V	100	150		MHz
Voltage Range						
V_{RLS}		IV	0	-	2.0	V
V_{RHS}		IV	3.0	-	AV_{DD}	V
V_{RHS} - V_{RLS}		V	1.0	4.0	5.0	V
$\Delta(V_{RHF} - V_{RHS})$		V		90		mV
$\Delta(V_{RLS} - V_{RLF})$		V		75		mV
Reference Settling Time						
V_{RHS}		V		15		Clock Cycles
V_{RLS}		V		20		Clock Cycles
Conversion Characteristics						
Maximum Conversion Rate		I	20			MHz
Minimum Conversion Rate		IV	2			MHz
Pipeline Delay (Latency)		IV			12	Clock Cycles
Aperture Delay Time		V		5		ns
Aperture Jitter Time		V		30		ps
Dynamic Performance						
Effective Number of Bits						
f_{IN}=1 MHz		I		8.8		Bits
f_{IN}=3.58 MHz		I		8.8		Bits
f_{IN}=5 MHz		I		8.7		Bits
f_{IN}=10.3 MHz		I		8.5		Bits

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ELECTRICAL SPECIFICATIONS

T_A=25 °C, AV_{DD} = DV_{DD} = +5.0 V, V_{IN}=0 to 4 V, f_S=20 MSPS, f_{CLK}=40 MHz, V_{RHS}= 4.0 V, V_{RLS}=0.0 V, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
Dynamic Performance						
Signal-to-Noise Ratio (without Harmonics)						
f_{IN}=1 MHz		I	53	56		dB
f_{IN}=3.58 MHz		I	53	56		dB
f_{IN}=5 MHz		I	52	55		dB
f_{IN}=10.3 MHz		I	52	55		dB
Harmonic Distortion						
f_{IN}=1 MHz		I	57	60		dB
f_{IN}=3.58 MHz		I	56	59		dB
f_{IN}=5 MHz		I	56	59		dB
f_{IN}=10.3 MHz		I	53	56		dB
Signal-to-Noise and Distortion (SINAD)						
f_{IN}=1 MHz		I	52	55		dB
f_{IN}=3.58 MHz		I	52	55		dB
f_{IN}=5 MHz		I	51	54		dB
f_{IN}=10.3 MHz		I	50	53		dB
Spurious Free Dynamic Range	f_{IN} = 1 MHz	V		63		dB
Differential Phase		V		TBD		Degree
Differential Gain		V		TBD		%
Intermodulation Distortion				TBD		dB
Digital Inputs						
Logic "1" Voltage		I	2.0			V
Logic "0" Voltage		I			0.8	V
Maximum Input Current Low		I	-10		+10	µA
Maximum Input Current High		I	-10		+10	µA
Input Capacitance		V		5		pF
Digital Outputs						
Logic "1" Voltage	(I_{OH}=0.5 mA)	I	3.5			V
Logic "0" Voltage	(I_{OS}=1.6 mA)	I			0.4	V
t_{RISE}/t_{FALL}	15 pF load	V		10		ns
Output Enable to Data Output Delay	20 pF load, T_A = +25 °C	V		10		ns
	50 pF load over temp.	V		22		ns
Power Supply Requirements						
Voltages DV_{DD}		I	4.75	5.0	5.25	V
AV_{DD}		I	4.75	5.0	5.25	V
Currents AI_{DD}		I		10	12	mA
DI_{DD}		I		18	21	mA
Power Dissipation		I		140	165	mW

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions: All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests; therefore, $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

Figure 1A: Timing Diagram 1

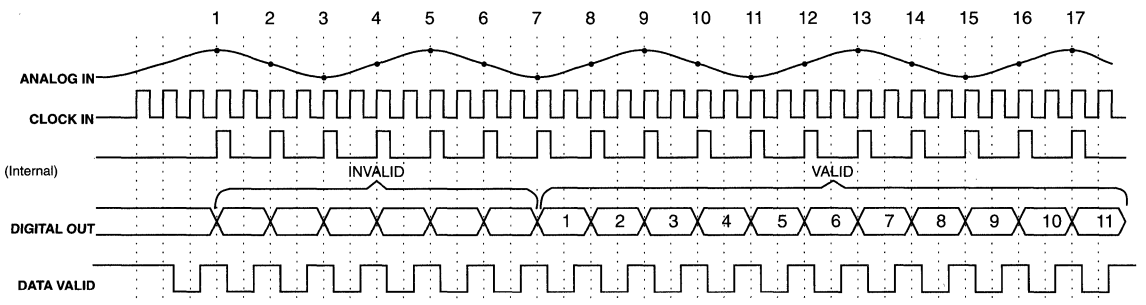

Figure 1B: Timing Diagram 2

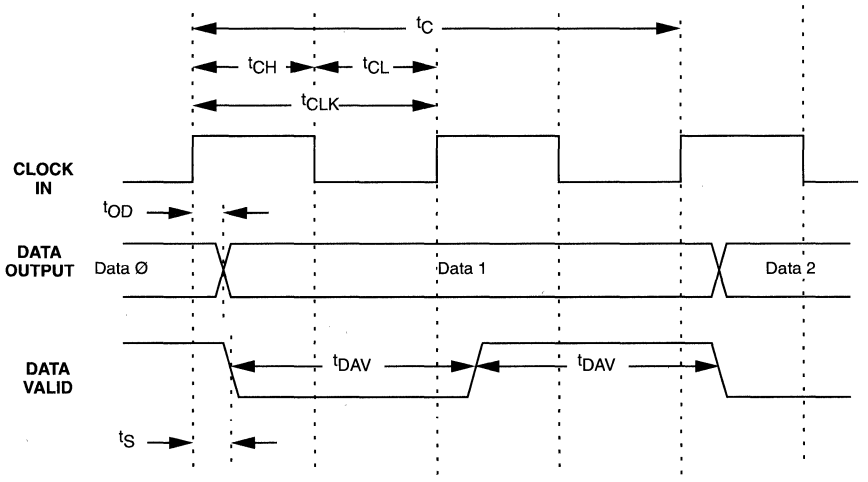

Table 1 - Timing Parameters

DESCRIPTION	PARAMETERS	MIN	TYP	MAX	UNITS
Conversion Time	t_c	$2*t_{CLK}$			ns
Clock Period	t_{CLK}	25			ns
Clock High Duty Cycle	t_{CH}	40	50	60	%
Clock Low Duty Cycle	t_{CL}	40	50	60	%
Output Delay (15 pF Load)	t_{OD}	15	20	25	ns
DAV Pulse Width	t_{DAV}		t_{CLK}		ns
Clock to DAV	t_S	16	21	26	ns

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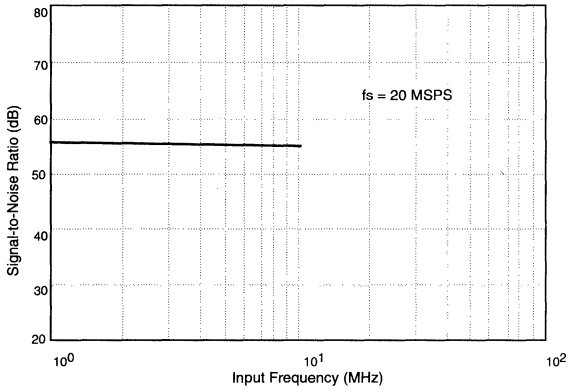
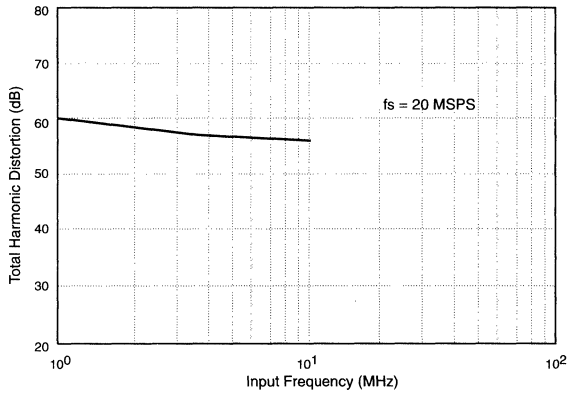
TYPICAL PERFORMANCE CHARACTERISTICS

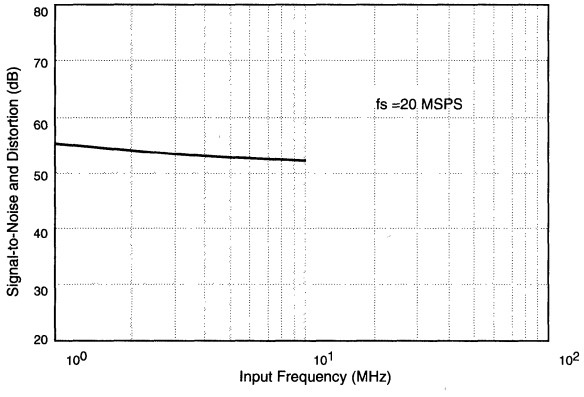
SNR vs Input Frequency



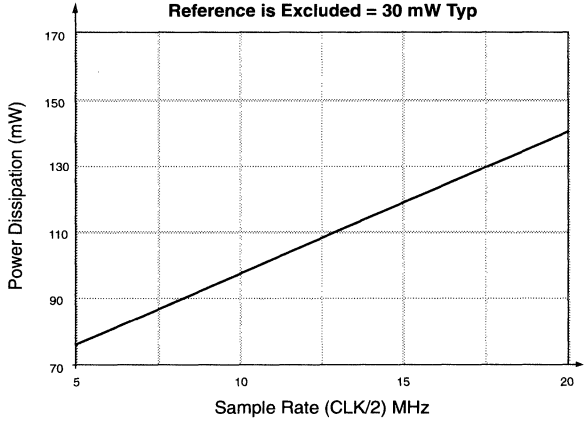
THD vs Input Frequency



SINAD vs Input Frequency



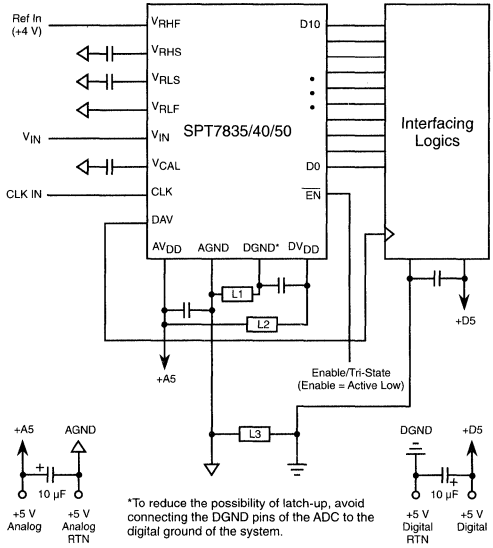
Total Power Dissipation Vs. Sample Rate
Reference is Excluded = 30 mW Typ



TYPICAL INTERFACE CIRCUIT

Figure 1 shows the typical interface requirements when using the SPT7850 in normal circuit operation. To reduce the possibility of latch-up, avoid connecting the DGND pins of the ADC to the digital ground of the system. The following sections provide descriptions of the major functions and outline critical performance criteria to consider for achieving the optimal device performance.

Figure 1 - Typical Interface Circuit



NOTES: 1) L3 is to be located as closely to the device as possible.
2) There should be no additional connections to the right of L1 and L2.
3) All capacitors are 0.1 µF surface-mount unless otherwise specified.
4) L1, L2 and L3 are 10 µH inductors or ferrite beads.

POWER SUPPLIES AND GROUNDING

SPT suggests that both the digital and the analog supply voltages on the SPT7850 be derived from a single analog supply as shown in figure 1. A separate digital supply must be used for all interface circuitry. SPT suggests using this power supply configuration to prevent a possible latch-up condition on power up.

OPERATING DESCRIPTION

The general architecture for the CMOS ADC is shown in the block diagram. The design contains eight identical successive approximation ADC sections, all operating in parallel, a 16-phase clock generator, an 11-bit 8:1 digital output multiplexer, correction logic, and a voltage reference generator which provides common reference levels for each ADC section.

The high sample rate is achieved by using multiple SAR ADC sections in parallel, each of which samples the input signal in sequence. Each ADC uses 16 clock cycles to complete a conversion. The clock cycles are allocated as follows:

Clock	Operation
1	Reference zero sampling
2	Auto-zero comparison
3	Auto-calibrate comparison
4	Input sample
5-15	11-bit SAR conversion
16	Data transfer

The 16 phase clock, which is derived from the input clock, synchronizes these events. The timing signals for adjacent ADC sections are shifted by two clock cycles so that the analog input is sampled on every other cycle of the input clock by exactly one ADC section. After 16 clock periods, the timing cycle repeats. The sample rate for the configuration is one-half of the clock rate, e.g., for a 40 MHz clock rate, the input sample rate is 20 MHz. The latency from analog input sample to the corresponding digital output is 12 clock cycles.

- Since only eight comparators are used, a huge power savings is realized.
- The auto-zero operation is done using a closed loop system that uses multiple samples of the comparators response to a reference zero.
- The auto-calibrate operation, which calibrates the gain of the MSB reference and the LSB reference, is also done with a closed loop system. Multiple samples of the gain error are integrated to produce a calibration voltage for each ADC section.
- Capacitive displacement currents, which can induce sampling error, are minimized since only one comparator samples the input during a clock cycle.
- The total input capacitance is very low since sections of the converter which are not sampling the signal are isolated from the input by transmission gates.

VOLTAGE REFERENCE

The SPT7850 requires the use of a single external voltage reference for driving the high side of the reference ladder. It must be within the range of 3 V to 5 V. The lower side of the ladder is typically tied to AGND (0.0 V), but can be run up to 2.0 V with a second reference. The analog input voltage range will track the total voltage difference measured between the ladder sense lines, V_{RHS} and V_{RLS}.

Force and sense taps are provided to ensure accurate and stable setting of the upper and lower ladder sense line voltages across part-to-part and temperature variations. By using the configuration shown in figure 2, offset and gain errors of less than ±2 LSB can be obtained.

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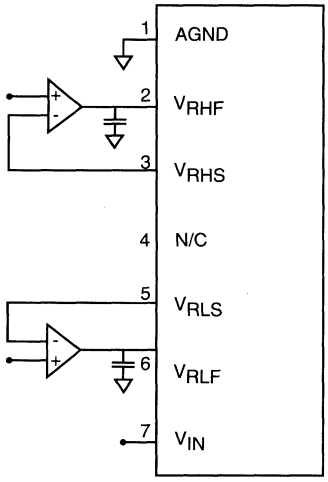
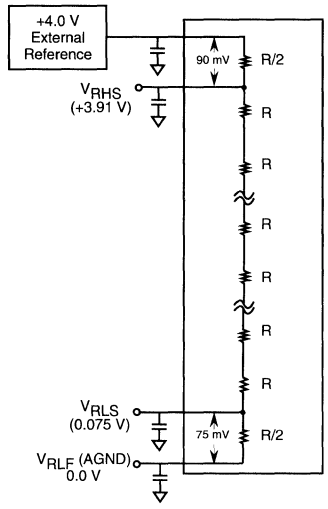
Figure 2 - Ladder Force/Sense Circuit



All capacitors are 0.01 µF

Figure 3 - Simplified Reference Ladder Drive Circuit Without Force/Sense Circuit



R=30 Ω (typ)
All capacitors are 0.01 µF

In cases where wider variations in offset and gain can be tolerated, V_{Ref} can be tied directly to V_{RHF} and AGND can be tied directly to V_{RLF} as shown in figure 3. Decouple force and sense lines to AGND with a .01 µF capacitor (chip cap preferred) to minimize high-frequency noise injection. If this simplified configuration is used, the following considerations should be taken into account:

The reference ladder circuit shown in figure 3 is a simplified representation of the actual reference ladder with force and sense taps shown. Due to the actual internal structure of the ladder, the voltage drop from V_{RHF} to V_{RHS} is not equivalent to the voltage drop from V_{RLF} to V_{RLS}.

Typically, the top side voltage drop for V_{RHF} to V_{RHS} will equal:

$V_{RHF} - V_{RHS}$ = 2.25 % of ($V_{RHF} - V_{RLF}$) (typical),

and the bottom side voltage drop for V_{RLS} to V_{RLF} will equal:

$V_{RLS} - V_{RLF}$ = 1.9 % of ($V_{RHF} - V_{RLF}$) (typical).

Figure 3 shows an example of expected voltage drops for a specific case. Vref of 4.0 V is applied to V_{RHF} and V_{RLF} is tied to AGND. A 90 mV drop is seen at V_{RHS} (= 3.91 V) and a 75 mV increase is seen at V_{RLS} (= 0.075 V).

ANALOG INPUT

V_{IN} is the analog input. The input voltage range is from V_{RLS} to V_{RHS} (typically 4.0 V) and will scale proportionally with respect to the voltage reference. (See voltage reference section.)

The drive requirements for the analog inputs are very minimal when compared to most other converters due to the SPT7850's extremely low input capacitance of only 5 pF and very high input resistance of 250 kΩ.

The analog input should be protected through a series resistor and diode clamping circuit as shown in figure 4.

CALIBRATION

The SPT7850 uses an auto calibration scheme to ensure 10-bit accuracy over time and temperature. Gain and offset errors are continually adjusted to 10-bit accuracy during device operation. This process is completely transparent to the user.

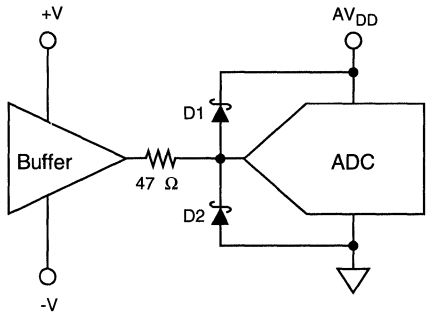
Upon power-up, the SPT7850 begins its calibration algorithm. In order to achieve the calibration accuracy required, the offset and gain adjustment step size is a fraction of a 10-bit LSB. Since the calibration algorithm is an oversampling process, a minimum of 10k clock cycles are required. This results in a minimum calibration time upon power-up of 250 µsec (for a 20 MHz sample rate). Once calibrated, the SPT7850 remains calibrated over time and temperature.

Since the calibration cycles are initiated on the rising edge of the clock, the clock must be continuously applied for the SPT7850 to remain in calibration.

INPUT PROTECTION

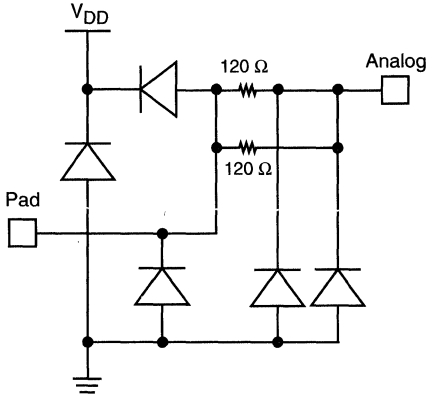
All I/O pads are protected with an on-chip protection circuit shown in figure 5. This circuit provides ESD robustness to 3.5 kV and prevents latch-up under severe discharge conditions without degrading analog transition times.

Figure 4 - Recommended Input Protection Circuit



D1 = D2 = Hewlett Packard HP5712 or equivalent

Figure 5 - On-Chip Protection Circuit



POWER SUPPLY SEQUENCING CONSIDERATIONS

All logic inputs should be held low until power to the device has settled to the specific tolerances. Avoid power decoupling networks with large time constants which could delay V_{DD} power to the device.

CLOCK INPUT

The SPT7850 is driven from a single-ended TTL-input clock. Because the pipelined architecture operates on the rising edge of the clock input, the device can operate over a wide range of input clock duty cycles without degrading the dynamic performance. **The device's sample rate is 1/2 of the input clock frequency. (See timing diagram.)**

DIGITAL OUTPUTS

The format of the output data (D0-D9) is straight binary. (See table 2.) The outputs are latched on the rising edge of CLK. These outputs can be switched into a tri-state mode by bringing $\overline{EN}$ high.

Table 2 - Output Data Information

ANALOG INPUT	OVERRANGE D10	OUTPUT CODE D9-D0
+F.S. + 1/2 LSB	1	11 1111 1111
+F.S. -1/2 LSB	0	11 1111 111Ø
+1/2 F.S.	0	ØØ ØØØØ ØØØØ
+1/2 LSB	0	OO OOOO OOOØ
0.0 V	0	OO OOOO OOOO

(Ø indicates the flickering bit between logic 0 and 1).

OVERRANGE OUTPUT

The OVERRANGE OUTPUT (D10) is an indication that the analog input signal has exceeded the positive full scale input voltage by 1 LSB. When this condition occurs, D10 will switch to logic 1. All other data outputs (D0 to D9) will remain at logic 1 as long as D10 remains at logic 1. This feature makes it possible to include the SPT7850 into higher resolution systems.

EVALUATION BOARD

The EB7850 Evaluation Board is available to aid designers in demonstrating the full performance of the SPT7850. This board includes a reference circuit, clock driver circuit, output data latches and an on-board reconstruction of the digital data. An application note describing the operation of this board as well as information on the testing of the SPT7850 is also available. Contact the factory for price and availability.

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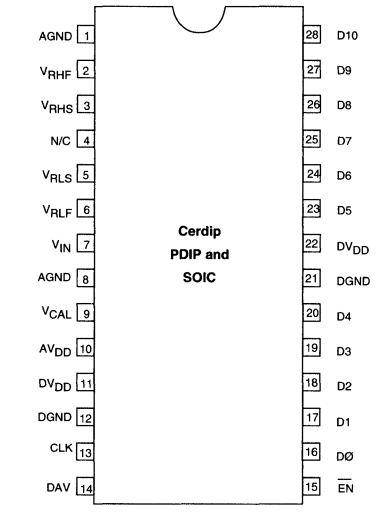
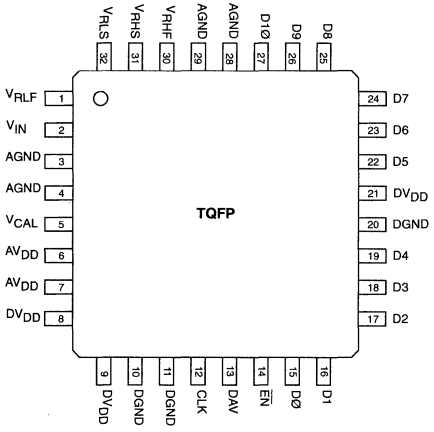
PIN ASSIGNMENTS





PIN FUNCTIONS

NAME	FUNCTION
AGND	Analog Ground
V_{RHF}	Reference High Force
V_{RHS}	Reference High Sense
V_{RLS}	Reference Low Sense
V_{RLF}	Reference Low Force
V_{CAL}	Calibration Reference
V_{IN}	Analog Input
AV_{DD}	Analog V_{DD}
DV_{DD}	Digital V_{DD}
DGND	Digital Ground
CLK	Input Clock f_{CLK} =fs (TTL)
EN	Output Enable
D0-9	Tri-State Data Output, (DØ=LSB)
D10	Tri-State Output Overrange
DAV	Data Valid Output

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SIGNAL PROCESSING TECHNOLOGIES

SPT7852

DUAL 10-BIT, 20 MSPS, 165 mW A/D CONVERTER

ADVANCED INFORMATION

FEATURES

- Dual 10-Bit/20 MSPS Analog-to-Digital Converter
- Monolithic CMOS
- Internal Track-and-Hold
- Low Power Dissipation: 165 mW
- 4 Vp-p Analog Input Range for Each ADC
- Single +5 Volt Power Supply
  With option for 3.3 V Digital Outputs
- Tri-Stable, TTL-Compatible Outputs
- Overrange Bit
- Selectable Twos Complement or Straight Binary Output

APPLICATIONS

- Composite Video Digitizers
- S-Video Digitizers
- Video Set-Top Boxes
- Telecommunications
- QAM Demodulation
- Ethernet Over Cable

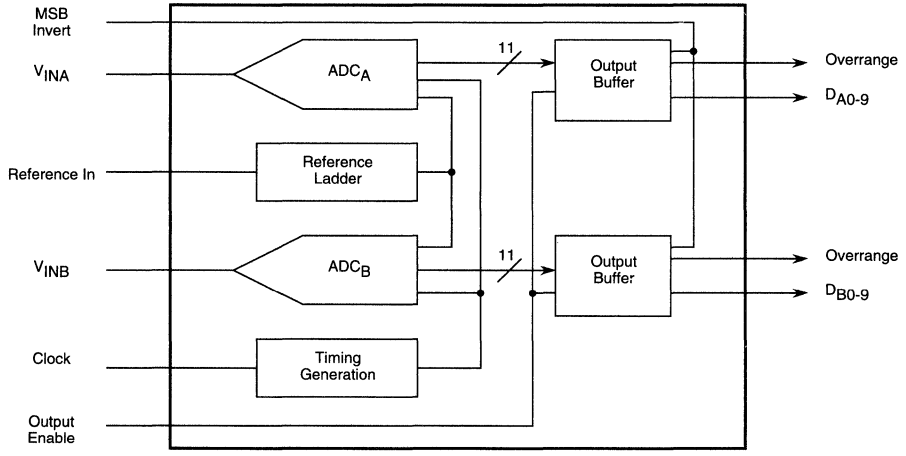
GENERAL DESCRIPTION

The SPT7852 has two 10-Bit CMOS analog-to-digital converters that can sample data at speeds up to 20 MSPS. It has excellent low noise performance with a very low typical power dissipation of only 165 mW - that's the total power for *both* converters. The SPT7852 uses a dual configuration of the proprietary circuit design found in our 10-bit CMOS single converter family, to achieve its high performance in a CMOS process.

The SPT7852 is specifically designed for video decoding applications and is ideal for S-video decoding and decoding of multiple composite video sources. It also has excellent application in the area of coherent I/Q demodulation in such applications as QAM demodulation and TV set-top box converters.

Inputs and outputs are TTL/CMOS -compatible to interface with TTL/CMOS-logic systems. Output data format is selectable for either straight binary or two's complement. The SPT7852 is available in a 44L TQFP package in the commercial temperature range (0 to 70°C).

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages
- AV_{DD} ..... +6 V
- DV_{DD} ..... +6 V

Input Voltages
- Analog Input ..... -0.5 V to AV_{DD} +0.5 V
- V_{REF} ..... 0 to AV_{DD}
- CLK Input ..... V_{DD}
- AV_{DD} - DV_{DD} ..... ±100 mV
- AGND - DGND ..... ±100 mV

Output
- Digital Outputs ..... 10 mA

Temperature
- Operating Temperature ..... 0 to 70 °C
- Junction Temperature ..... 175 °C
- Lead Temperature, (soldering 10 seconds) ..... 300 °C
- Storage Temperature ..... -65 to +150 °C

Note: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS FOR EACH CHANNEL

T_A=25 °C, AV_{DD} = DV_{DD} = +5.0 V, V_{IN}=0 to 4 V, f_S=20 MSPS, f_{CLK}=40 MHz, V_{RHS}= 4.0 V, V_{RLS}=0.0 V, unless otherwise specified.

TEST PARAMETERS	TEST CONDITIONS	LEVEL	MIN	TYP	MAX	UNITS
Resolution			10			Bits
DC Accuracy						
Integral Nonlinearity		I		±1.0		LSB
Differential Nonlinearity		I		±0.5		LSB
No Missing Codes		I		Guaranteed		
Analog Input						
Input Voltage Range		I	V_{RLS}		V_{RHS}	V
Input Resistance		I	250			kΩ
Input Capacitance		V		5.0		pF
Input Bandwidth	(Small Signal)	V		100		MHz
Offset		V		±2.0		LSB
Gain Error		V		±2.0		LSB
Reference Input						
Resistance		I	400	500	600	Ω
Bandwidth		V	100	150		MHz
Voltage Range						
V_{RLS}		IV	0	-	2.0	V
V_{RHS}		IV	3.0	-	AV_{DD}	V
V_{RHS} - V_{RLS}		V	1.0	4.0	5.0	V
$\Delta(V_{RHF} - V_{RHS})$		V		90		mV
$\Delta(V_{RLS} - V_{RLF})$		V		75		mV
Reference Settling Time						
V_{RHS}		V		15		Clock Cycles
V_{RLS}		V		20		Clock Cycles
Conversion Characteristics						
Maximum Conversion Rate		I	20			MHz
Minimum Conversion Rate		IV	2			MHz
Pipeline Delay (Latency)		IV			12	Clock Cycles
Aperture Delay Time		V		5		ns
Aperture Jitter Time		V		15		ps
Dynamic Performance						
Effective Number of Bits						
f_{IN}=1 MHz		I		8.8		Bits
f_{IN}=3.58 MHz		I		8.8		Bits
f_{IN}=5 MHz		I		8.7		Bits
f_{IN}=10.3 MHz		I		8.5		Bits

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ELECTRICAL SPECIFICATIONS

T_A=25 °C, AV_{DD} = DV_{DD} = +5.0 V, V_{IN}=0 to 4 V, f_S=20 MSPS, f_{CLK}=40 MHz, V_{RHS}= 4.0 V, V_{RLS}=0.0 V, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
Dynamic Performance						
Signal-to-Noise Ratio (without Harmonics)						
f_{IN}=1 MHz		I		56		dB
f_{IN}=5 MHz		I		55		dB
f_{IN}=10.3 MHz		I		55		dB
Harmonic Distortion						
f_{IN}=1 MHz		I		60		dB
f_{IN}=5 MHz		I		59		dB
f_{IN}=10.3 MHz		I		56		dB
Signal-to-Noise and Distortion (SINAD)						
f_{IN}=1 MHz		I		55		dB
f_{IN}=5 MHz		I		54		dB
f_{IN}=10.3 MHz		I		53		dB
Spurious Free Dynamic Range	f_{IN} = 1 MHz	V		63		dB
Differential Phase		V		0.3		Degree
Differential Gain		V		0.5		%
Intermodulation Distortion				TBD		dB
Digital Inputs						
Logic "1" Voltage		I	2.0			V
Logic "0" Voltage		I			0.8	V
Maximum Input Current Low		I	-10		+10	µA
Maximum Input Current High		I	-10		+10	µA
Input Capacitance		V		5		pF
Digital Outputs						
Logic "1" Voltage	(I_{OH}=0.5 mA)	I	3.5			V
Logic "0" Voltage	(I_{OS}=1.6 mA)	I			0.4	V
t_{RISE}/t_{FALL}	15 pF load	V		10		ns
Output Enable to Data Output Delay	20 pF load, T_A = +25 °C	V		10		ns
	50 pF load over temp.	V		22		ns
Power Supply Requirements	Total for both converter					
Voltages DV_{DD}	channels	I	4.75	5.0	5.25	V
AV_{DD}		I	4.75	5.0	5.25	V
Currents AI_{DD}		I		12		mA
DI_{DD}		I		21		mA
Power Dissipation		I		165		mW

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions: All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests; therefore, $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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SIGNAL PROCESSING TECHNOLOGIES

SPT7855

10-BIT, 25 MSPS, 135 mW A/D CONVERTER

FEATURES

- Monolithic 25 MSPS Converter
- 135 mW Power Dissipation
- On-Chip Track-and-Hold
- Single +5 V Power Supply
- TTL/CMOS Outputs
- 5 pF Input Capacitance
- Low Cost
- Tri-State Output Buffers
- High ESD Protection: 3,500 V Minimum

APPLICATIONS

- All High-Speed Applications Where Low Power Dissipation is Required
- Video Imaging
- Medical Imaging
- IR Imaging
- Digital Communications

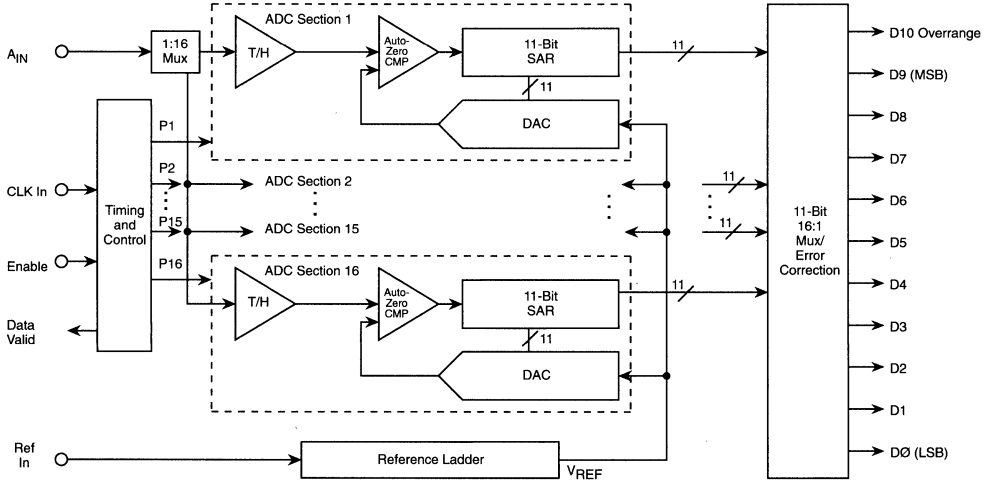
GENERAL DESCRIPTION

The SPT7855 is a 10-bit monolithic, low cost, ultra-low power analog-to-digital converter capable of minimum word rates of 25 MSPS. The on-chip track-and-hold function assures very good dynamic performance without the need for external components. The input drive requirements are minimized due to the SPT7855's low input capacitance of only 5 pF.

Power dissipation is extremely low at only 135 mW typical at 25 MSPS with a power supply of +5.0 V. The SPT7855 is pin-compatible with the entire family of SPT 10-bit, CMOS converters (SPT7835/40/50/55/60) which simplifies upgrades. The SPT7855 has incorporated proprietary circuit design (*) and CMOS processing technologies to achieve its advanced performance. Inputs and outputs are TTL/CMOS-compatible to interface with TTL/CMOS-logic systems. Output data format is straight binary.

The SPT7855 is available in 28-lead 300 mil cerdip and PDIP, 28-lead SOIC and 32-lead small (7 mm square) TQFP packages over the temperature range of 0 to 70 °C. For extended temperature ranges and /883 processing requirements, consult the factory.

BLOCK DIAGRAM



***PATENT PENDING**

ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages
- AV_{DD} ..... +6 V
- DV_{DD} ..... +6 V

Input Voltages
- Analog Input ..... -0.5 V to AV_{DD} +0.5 V
- V_{REF} ..... 0 to AV_{DD}
- CLK Input ..... V_{DD}
- AV_{DD} - DV_{DD} ..... ±100 mV
- AGND - DGND ..... ±100 mV

Output
- Digital Outputs ..... 10 mA

Temperature
- Operating Temperature ..... 0 to 70 °C
- Junction Temperature ..... 175 °C
- Lead Temperature, (soldering 10 seconds) ..... 300 °C
- Storage Temperature ..... -65 to +150 °C

Note: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

T_A=25 °C, AV_{DD} = DV_{DD} = +5.0 V, V_{IN} = 0 to 4 V, f_{CLK} = 25 MSPS, V_{RHS} = 4.0 V, V_{RLS} = 0.0 V, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
Resolution			10			Bits
DC Accuracy						
Integral Nonlinearity		I		±1.0		LSB
Differential Nonlinearity		I		±0.5		LSB
No Missing Codes		I		Guaranteed		
Analog Input						
Input Voltage Range		I	V_{RLS}		V_{RHS}	V
Input Resistance		I	250			kΩ
Input Capacitance		V		5.0		pF
Input Bandwidth	(Small Signal)	V		100		MHz
Offset		V		±2.0		LSB
Gain Error		V		±2.0		LSB
Reference Input						
Resistance		I	400	500	600	Ω
Bandwidth		V	100	150		MHz
Voltage Range						
V_{RLS}		IV	0	-	2.0	V
V_{RHS}		IV	3.0	-	AV_{DD}	V
V_{RHS} - V_{RLS}		V	1.0	4.0	5.0	V
$\Delta(V_{RHF} - V_{RHS})$		V		90		mV
$\Delta(V_{RLS} - V_{RLF})$		V		75		mV
Reference Settling Time						
V_{RHS}		V		15		Clock Cycles
V_{RLS}		V		20		Clock Cycles
Conversion Characteristics						
Maximum Conversion Rate		I	25			MHz
Minimum Conversion Rate		IV	2			MHz
Pipeline Delay (Latency)		IV			12	Clock Cycles
Aperture Delay Time		V		8		ns
Aperture Jitter Time		V			15	ps(p-p)
Dynamic Performance	T_A=25 °C					
Effective Number of Bits						
fin=3.58 MHz		I		8.5		Bits
fin=10.3 MHz		I		8.3		Bits

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ELECTRICAL SPECIFICATIONS

T_A=25 °C, AV_{DD} = DV_{DD} = +5.0 V, V_{IN} = 0 to 4 V, f_{CLK} = 25 MSPS, V_{RHS} = 4.0 V, V_{RLS} = 0.0 V, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
Dynamic Performance						
Signal-to-Noise Ratio (without Harmonics)						
fin=3.58 MHz		I	56.0	58		dB
fin=10.3 MHz		I	54.0	56		dB
Harmonic Distortion	(9 Distortion bins from					
f_{IN}=3.58 MHz	1024 pt FFT)	I	55.5	59		dB
f_{IN}=10.3 MHz		I	51.5	54		dB
Signal-to-Noise and Distortion (SINAD)						
fin=3.58 MHz		I	53.0	55		dB
fin=10.3 MHz		I	50.5	52		dB
Spurious Free Dynamic Range	f_{IN}=1 MHz	V		63		dB
Differential Phase				TBD		Degree
Differential Gain				TBD		%
Intermodulation Distortion	f_A=1.0 MHz f_B=1.05 MHz			TBD		dB
Inputs						
Logic "1" Voltage		I	2.0			V
Logic "0" Voltage		I			0.8	V
Maximum Input Current Low		I	-10		+10	µA
Maximum Input Current High		I	-10		+10	µA
Input Capacitance		I		+5		pF
Digital Outputs						
Logic "1" Voltage	I_{OH} = 0.5 mA	I	3.5			V
Logic "0" Voltage	I_{OL} = 1.6 mA	I			0.4	V
t_{RISE}	15 pF load	V		10		ns
t_{FALL}	15 pF load	V		10		ns
Output Enable to Data Output Delay	20 pF load, T_A = +25 °C	V		10		ns
	50 pF load over temp.	V		22		ns
Power Supply Requirements						
Voltages	DV_{DD}	I	4.75	5.0	5.25	V
	AV_{DD}	I	4.75	5.0	5.25	V
Currents	AI_{DD}	I		16	20	mA
	DI_{DD}	I		11	15	mA
Power Dissipation		I		135	175	mW

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions: All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests; therefore, $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

Figure 1A: Timing Diagram 1

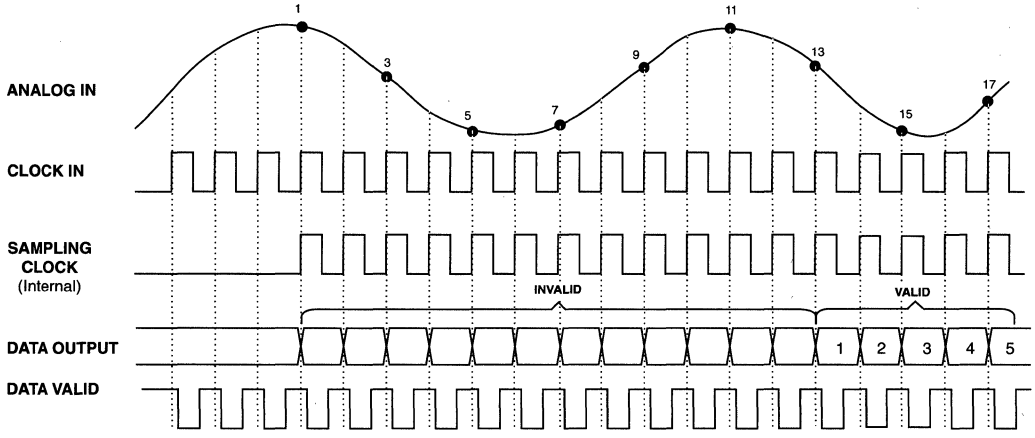

Figure 1B: Timing Diagram 2

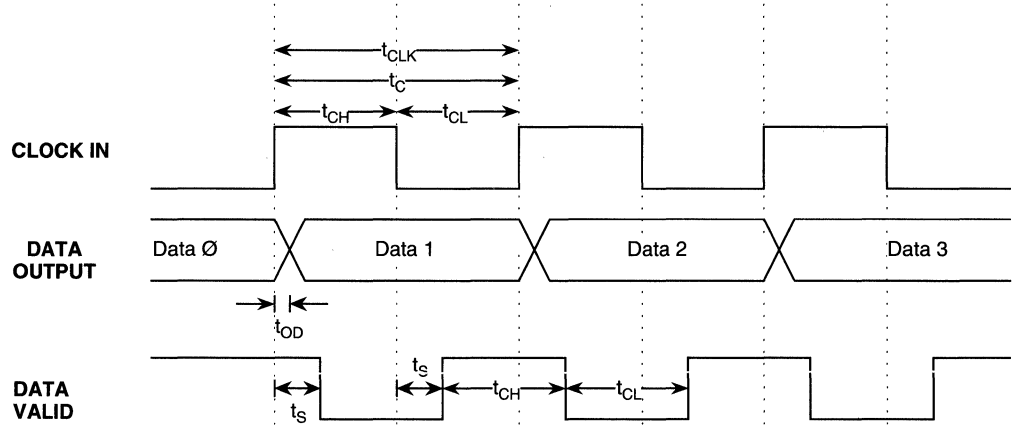

Table 1 - Timing Parameters

DESCRIPTION	PARAMETERS	MIN	TYP	MAX	UNITS
Conversion Time	t_C	t_{CLK}			ns
Clock Period	t_{CLK}	40			ns
Clock High Duty Cycle	t_{CH}	40	50	60	%
Clock Low Duty Cycle	t_{CL}	40	50	60	%
Clock to Output Delay (15 pF Load)	t_{OD}		17		ns
Clock to DAV	t_S		10		ns

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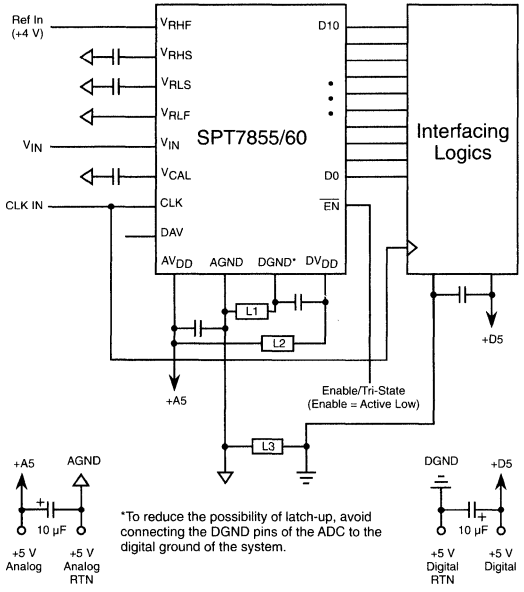
TYPICAL INTERFACE CIRCUIT

Figure 1 shows the typical interface requirements when using the SPT7855 in normal circuit operation. To reduce the possibility of latch-up, avoid connecting the DGND pins of the ADC to the digital ground of the system. The following sections provide descriptions of the major functions and outline critical performance criteria to consider for achieving the optimal device performance.

Figure 1 - Typical Interface Circuit



NOTES: 1) L3 is to be located as closely to the device as possible.
2) There should be no additional connections to the right of L1 and L2.
3) All capacitors are 0.1 µF surface-mount unless otherwise specified.
4) L1, L2 and L3 are 10 µH inductors or ferrite beads.

POWER SUPPLIES AND GROUNDING

SPT suggests that both the digital and the analog supply voltages on the SPT7855 be derived from a single analog supply as shown in figure 1. A separate digital supply should be used for all interface circuitry. SPT suggests using this power supply configuration to prevent a possible latch-up condition on power up.

OPERATING DESCRIPTION

The general architecture for the CMOS ADC is shown in the block diagram. The design contains 16 identical successive approximation ADC sections, all operating in parallel, a 16-phase clock generator, an 11-bit 16:1 digital output multiplexer, correction logic, and a voltage reference generator which provides common reference levels for each ADC section.

The high sample rate is achieved by using multiple SAR ADC sections in parallel, each of which samples the input signal in sequence. Each ADC uses 16 clock cycles to complete a conversion. The clock cycles are allocated as follows:

Clock	Operation
1	Reference zero sampling
2	Auto-zero comparison
3	Auto-calibrate comparison
4	Input sample
5-15	11-bit SAR conversion
16	Data transfer

The 16 phase clock, which is derived from the input clock, synchronizes these events. The timing signals for adjacent ADC sections are shifted by one clock cycle so that the analog input is sampled on every cycle of the input clock by exactly one ADC section. After 16 clock periods, the timing cycle repeats. The latency from analog input sample to the corresponding digital output is 12 clock cycles.

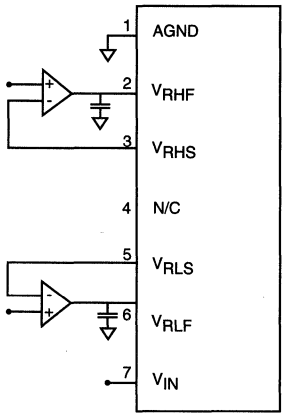
- Since only 16 comparators are used, a huge power savings is realized.
- The auto-zero operation is done using a closed loop system that uses multiple samples of the comparators response to a reference zero.
- The auto-calibrate operation, which calibrates the gain of the MSB reference and the LSB reference, is also done with a closed loop system. Multiple samples of the gain error are integrated to produce a calibration voltage for each ADC section.
- Capacitive displacement currents, which can induce sampling error, are minimized since only one comparator samples the input during a clock cycle.
- The total input capacitance is very low since sections of the converter which are not sampling the signal are isolated from the input by transmission gates.

VOLTAGE REFERENCE

The SPT7855 requires the use of a single external voltage reference for driving the high side of the reference ladder. It must be within the range of 3 V to 5 V. The lower side of the ladder is typically tied to AGND (0.0 V), but can be run up to 2.0 V with a second reference. The analog input voltage range will track the total voltage difference measured between the ladder sense lines, V_{RHS} and V_{RLS}.

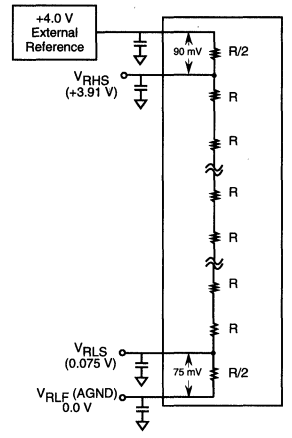
Force and sense taps are provided to ensure accurate and stable setting of the upper and lower ladder sense line voltages across part-to-part and temperature variations. By using the configuration shown in figure 2, offset and gain errors of less than ±2 LSB can be obtained.

Figure 2 - Ladder Force/Sense Circuit



All capacitors are 0.01 µF

Figure 3 - Reference Ladder



R=30 Ω (typ)
All capacitors are 0.01 µF

In cases where wider variations in offset and gain can be tolerated, V_{Ref} can be tied directly to V_{RHF} and AGND can be tied directly to V_{RLF} as shown in figure 3. Decouple force and sense lines to AGND with a .01 µF capacitor (chip cap preferred) to minimize high-frequency noise injection. If this simplified configuration is used, the following considerations should be taken into account:

The reference ladder circuit shown in figure 3 is a simplified representation of the actual reference ladder with force and sense taps shown. Due to the actual internal structure of the ladder, the voltage drop from V_{RHF} to V_{RHS} is not equivalent to the voltage drop from V_{RLF} to V_{RLS}.

Typically, the top side voltage drop for V_{RHF} to V_{RHS} will equal:

$V_{RHF} - V_{RHS}$ = 2.25 % of ($V_{RHF} - V_{RLF}$) (typical),

and the bottom side voltage drop for V_{RLS} to V_{RLF} will equal:

$V_{RLS} - V_{RLF}$ = 1.9 % of ($V_{RHF} - V_{RLF}$) (typical).

Figure 3 shows an example of expected voltage drops for a specific case. Vref of 4.0 V is applied to V_{RHF} and V_{RLF} is tied to AGND. A 90 mV drop is seen at V_{RHS} (= 3.91 V) and a 75 mV increase is seen at V_{RLS} (= 0.075 V).

ANALOG INPUT

V_{IN} is the analog input. The input voltage range is from V_{RLS} to V_{RHS} (typically 4.0 V) and will scale proportionally with respect to the voltage reference. (See voltage reference section.)

The drive requirements for the analog inputs are very minimal when compared to most other converters due to the SPT7855's extremely low input capacitance of only 5 pF and very high input resistance of 250 kΩ.

The analog input should be protected through a series resistor and diode clamping circuit as shown in figure 4.

CALIBRATION

The SPT7855 uses an auto calibration scheme to ensure 10-bit accuracy over time and temperature. Gain and offset errors are continually adjusted to 10-bit accuracy during device operation. This process is completely transparent to the user.

Upon power-up, the SPT7855 begins its calibration algorithm. In order to achieve the calibration accuracy required, the offset and gain adjustment step size is a fraction of a 10-bit LSB. Since the calibration algorithm is an oversampling process, a minimum of 10,000 clock cycles are required. This results in a minimum calibration time upon power-up of 400 µsec (for a 25 MHz clock). Once calibrated, the SPT7855 remains calibrated over time and temperature.

Since the calibration cycles are initiated on the rising edge of the clock, the clock must be continuously applied for the SPT7855 to remain in calibration.

INPUT PROTECTION

All I/O pads are protected with an on-chip protection circuit shown in figure 5. This circuit provides ESD robustness to 3.5 kV and prevents latch-up under severe discharge conditions without degrading analog transition times.

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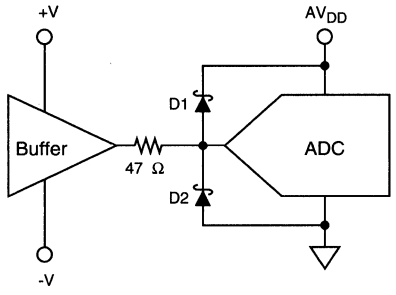
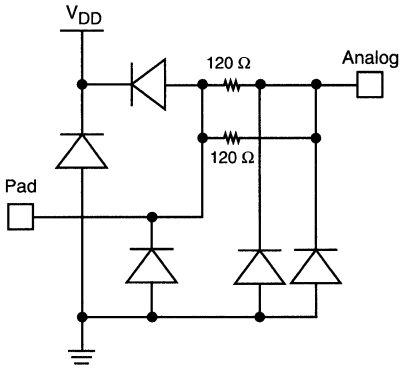
Figure 4 - Recommended Input Protection Circuit



D1 = D2 = Hewlett Packard HP5712 or equivalent

Figure 5 - On-Chip Protection Circuit



POWER SUPPLY SEQUENCING CONSIDERATIONS

All logic inputs should be held low until power to the device has settled to the specific tolerances. Avoid power decoupling networks with large time constants which could delay V_{DD} power to the device.

CLOCK INPUT

The SPT7855 is driven from a single-ended TTL-input clock. Because the pipelined architecture operates on the rising edge of the clock input, the device can operate over a wide range of input clock duty cycles without degrading the dynamic performance.

DIGITAL OUTPUTS

The format of the output data (D0-D9) is straight binary. (See table 2.) The outputs are latched on the rising edge of CLK. These outputs can be switched into a tri-state mode by bringing $\overline{EN}$ high.

Table 2 - Output Data Information

ANALOG INPUT	OVERRANGE D10	OUTPUT CODE D9-D0
+F.S. + 1/2 LSB	1	11 1111 1111
+F.S. -1/2 LSB	O	11 1111 111Ø
+1/2 F.S.	O	ØØ ØØØØ ØØØØ
+1/2 LSB	O	OO OOOO OOOØ
0.0 V	O	OO OOOO OOOO

(Ø indicates the flickering bit between logic 0 and 1.)

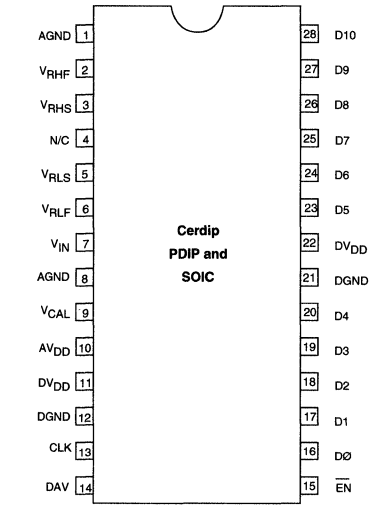
OVERRANGE OUTPUT

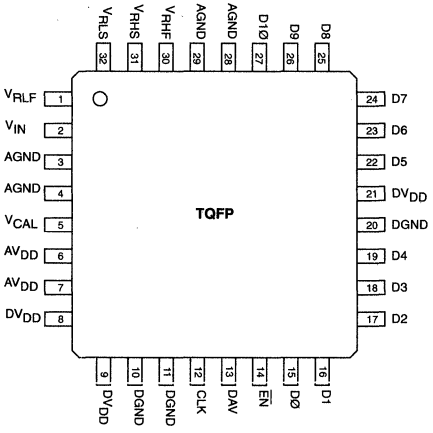
The OVERRANGE OUTPUT (D10) is an indication that the analog input signal has exceeded the positive full scale input voltage by 1 LSB. When this condition occurs, D10 will switch to logic 1. All other data outputs (D0 to D9) will remain at logic 1 as long as D10 remains at logic 1. This feature makes it possible to include the SPT7855 into higher resolution systems.

EVALUATION BOARD

The EB7855 evaluation board is available to aid designers in demonstrating the full performance of the SPT7855. This board includes a reference circuit, clock driver circuit, output data latches and an on-board reconstruction of the digital data. An application note describing the operation of this board as well as information on the testing of the SPT7855 is also available. Contact the factory for price and availability.

PIN ASSIGNMENTS





PIN FUNCTIONS

NAME	FUNCTION
AGND	Analog Ground
V_{RHF}	Reference High Force
V_{RHS}	Reference High Sense
V_{RLS}	Reference Low Sense
V_{RLF}	Reference Low Force
V_{CAL}	Calibration Reference
V_{IN}	Analog Input
AV_{DD}	Analog V_{DD}
DV_{DD}	Digital V_{DD}
DGND	Digital Ground
CLK	Input Clock f_{CLK} =fs (TTL)
$\overline{EN}$	Output Enable
D0-9	Tri-State Data Output, (DØ=LSB)
D10	Tri-State Output Overrange
DAV	Data Valid Output

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LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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SIGNAL PROCESSING TECHNOLOGIES

SPT7860

10-BIT, 40 MSPS,175 mW A/D CONVERTER

3

FEATURES

- Monolithic 40 MSPS Converter
- 175 mW Power Dissipation
- On-Chip Track-and-Hold
- Single +5 V Power Supply
- TTL/CMOS Outputs
- 5 pF Input Capacitance
- Low Cost
- Tri-State Output Buffers
- High ESD Protection: 3,500 V Minimum

APPLICATIONS

- All High-Speed Applications Where Low Power Dissipation is Required
- Video Imaging
- Medical Imaging
- Radar Receivers
- IR Imaging
- Digital Communications

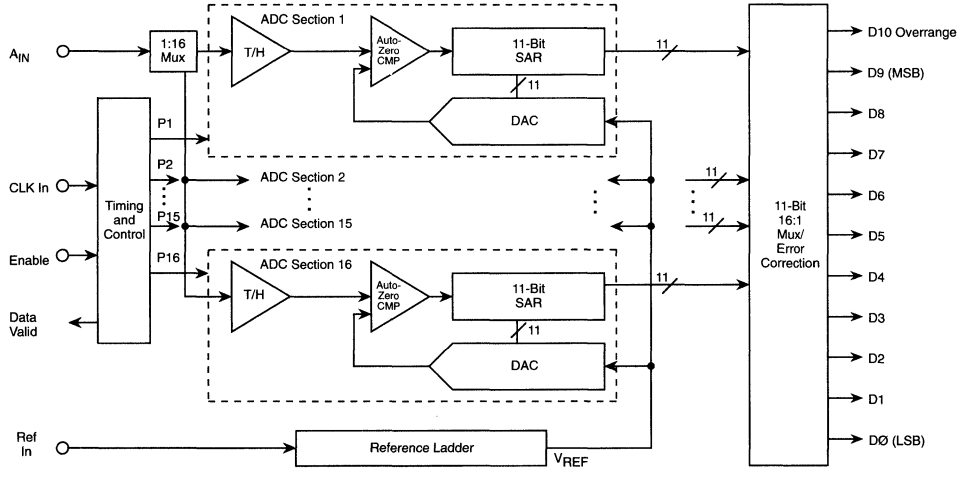
GENERAL DESCRIPTION

The SPT7860 is a 10-bit monolithic, low cost, ultra-low power analog-to-digital converter capable of minimum word rates of 40 MSPS. The on-chip track-and-hold function assures very good dynamic performance without the need for external components. The input drive requirements are minimized due to the SPT7860's low input capacitance of only 5 pF.

Power dissipation is extremely low at only 175 mW typical at 40 MSPS with a power supply of +5.0 V. The SPT7860 is pin-compatible with the entire family of SPT 10-bit, CMOS converters (SPT7835/40/50/55/60) which simplifies upgrades. The SPT7860 has incorporated proprietary circuit design (*) and CMOS processing technologies to achieve its advanced performance. Inputs and outputs are TTL/CMOS compatible to interface with TTL/CMOS logic systems. Output data format is straight binary.

The SPT7860 is available in 28-lead 300 mil cerdip and PDIP, 28-lead SOIC and 32-lead small (7 mm square) TQFP packages over the temperature range of 0 to 70 °C. For extended temperature ranges and /883 processing requirements, consult the factory.

BLOCK DIAGRAM



***PATENT PENDING**

ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages

AV_{DD} ..... +6 V
DV_{DD} ..... +6 V

Input Voltages

Analog Input ..... -0.5 V to AV_{DD} +0.5 V
V_{REF} ..... 0 to AV_{DD}
CLK Input ..... V_{DD}
AV_{DD} - DV_{DD} ..... ±100 mV
AGND - DGND ..... ±100 mV

Output

Digital Outputs ..... 10 mA

Temperature

Operating Temperature ..... 0 to 70 °C
Junction Temperature ..... 175 °C
Lead Temperature, (soldering 10 seconds) ..... 300 °C
Storage Temperature ..... -65 to +150 °C

Note: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

T_A=25 °C, AV_{DD} = DV_{DD} = +5.0 V, V_{IN} = 0 to 4 V, f_S = 40 MSPS, V_{RHS} = 4.0 V, V_{RLS} = 0.0 V, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
Resolution			10			Bits
DC Accuracy						
Integral Nonlinearity		I		±1.0		LSB
Differential Nonlinearity		I		±0.5		LSB
No Missing Codes		I		Guaranteed		
Analog Input						
Input Voltage Range		I	V_{RLS}		V_{RHS}	V
Input Resistance		I	250			kΩ
Input Capacitance		V		5.0		pF
Input Bandwidth	(Small Signal)	V	250			MHz
Offset		V		±2.0		LSB
Gain Error		V		±2.0		LSB
Reference Input						
Resistance		I	400	500	600	Ω
Bandwidth		V	100	150		MHz
Voltage Range						
V_{RLS}		IV	0	-	2.0	V
V_{RHS}		IV	3.0	-	AV_{DD}	V
V_{RHS} - V_{RLS}		V	1.0	4.0	5.0	V
Δ(V_{RHF} - V_{RHS})		V		90		mV
Δ(V_{RLS} - V_{RLF})		V		75		mV
Reference Settling Time						
V_{RHS}		V		15		Clock Cycles
V_{RLS}		V		20		Clock Cycles
Conversion Characteristics						
Maximum Conversion Rate		I	40			MHz
Minimum Conversion Rate		IV	2			MHz
Pipeline Delay (Latency)		IV			12	Clock Cycles
Aperture Delay Time		V		4.0		ns
Aperture Jitter Time		V		30		ps(p-p)
Dynamic Performance	T_A = +25 °C					
Effective Number of Bits						
fin=3.58 MHz		I		8.5		Bits
fin=10.3 MHz		I		8.3		Bits

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ELECTRICAL SPECIFICATIONS

T_A=25 °C, AV_{DD} = DV_{DD} = +5.0 V, V_{IN} = 0 to 4 V, f_S = 40 MSPS, V_{RHS} = 4.0 V, V_{RLS} = 0.0 V, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
Dynamic Performance	T_A = +25 °C					
Signal-to-Noise Ratio (without Harmonics)						
fin=3.58 MHz		I	52	54		dB
fin=10.3 MHz		I	51	52		dB
Harmonic Distortion	(9 Distortion bins from					
f_{IN}=3.58 MHz	1024 pt FFT)	I	55	61		dB
f_{IN}=10.3 MHz		I	52	53		dB
Signal-to-Noise and Distortion (SINAD)						
fin=3.58 MHz		I	51	54		dB
fin=10.3 MHz		I	49	52		dB
Spurious Free Dynamic Range	f_{IN}=1.0 MHz	V		63		dB
Differential Phase		V		TBD		Degree
Differential Gain				TBD		%
Intermodulation Distortion				TBD		dB
Inputs						
Logic "1" Voltage		I	2.0			V
Logic "0" Voltage		I			0.8	V
Maximum Input Current Low		I	-10		+10	µA
Maximum Input Current High		I	-10		+10	µA
Input Capacitance		V		+5		pF
Digital Outputs						
Logic "1" Voltage	I_{OH} = 0.5 mA	I	3.5			V
Logic "0" Voltage	I_{OL} = 1.6 mA	I			0.4	V
t_{RISE}	15 pF load	V		10		ns
t_{FALL}	15 pF load	V		10		ns
Output Enable to Data Output Delay	20 pF load, T_A = +25 °C	V		10		ns
	50 pF load over temp.	V		22		ns
Power Supply Requirements						
Voltages	DV_{DD}	IV	4.75	5.0	5.25	V
	AV_{DD}	IV	4.75	5.0	5.25	V
Currents	AI_{DD}	I		17	22	mA
	DI_{DD}	I		18	23	mA
Power Dissipation		I		175	225	mW

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests; therefore, $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

Figure 1A: Timing Diagram 1

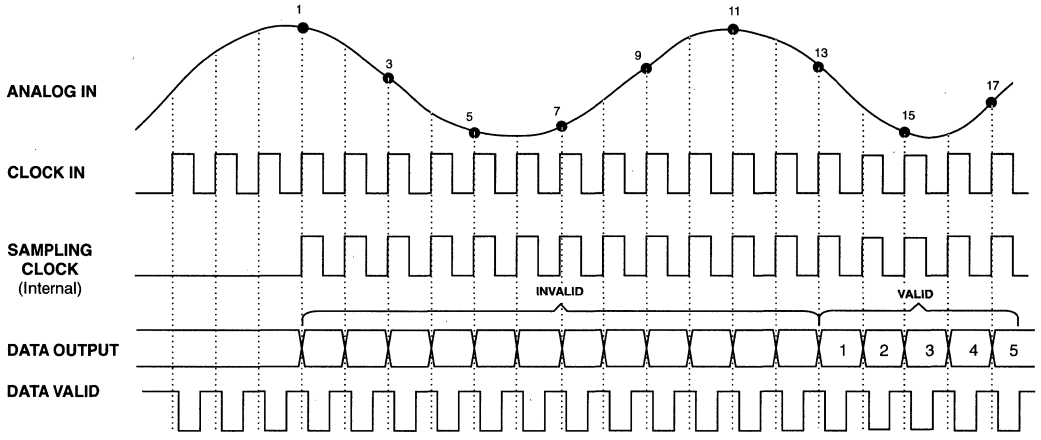

Figure 1B: Timing Diagram 2

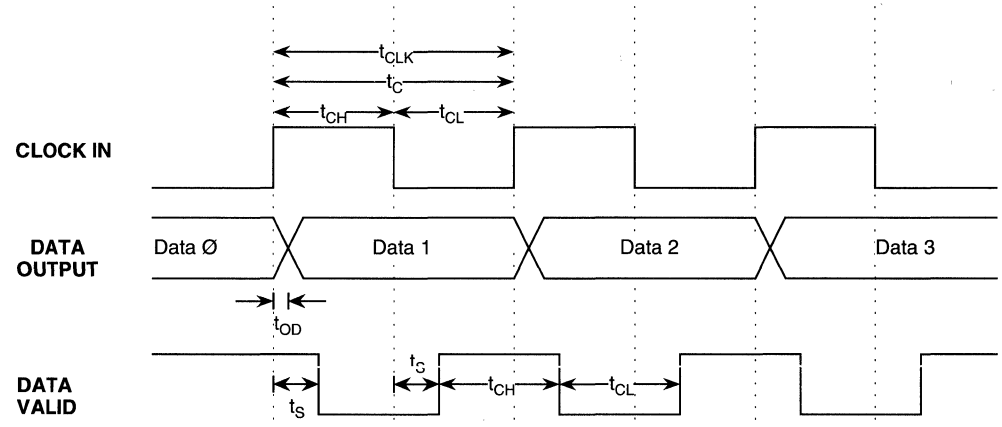

Table 1 - Timing Parameters

DESCRIPTION	PARAMETERS	MIN	TYP	MAX	UNITS
Conversion Time	t_C	t_{CLK}			ns
Clock Period	t_{CLK}	25			ns
Clock High Duty Cycle	t_{CH}	40	50	60	%
Clock Low Duty Cycle	t_{CL}	40	50	60	%
Clock to Output Delay (15 pF Load)	t_{OD}		17		ns
Clock to DAV	t_S		10		ns

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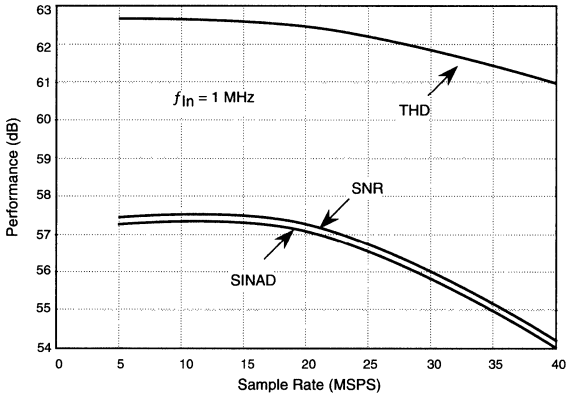
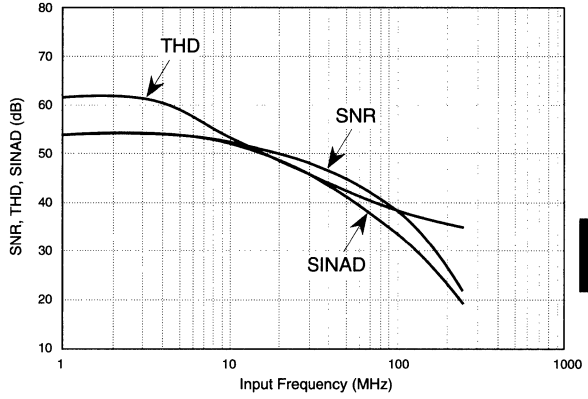
TYPICAL PERFORMANCE CHARACTERISTICS

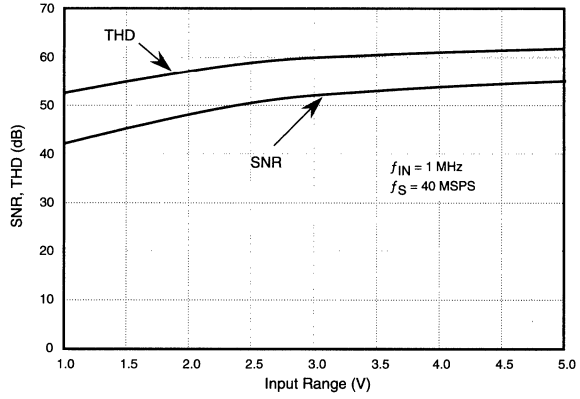
Performance vs Sample Rate



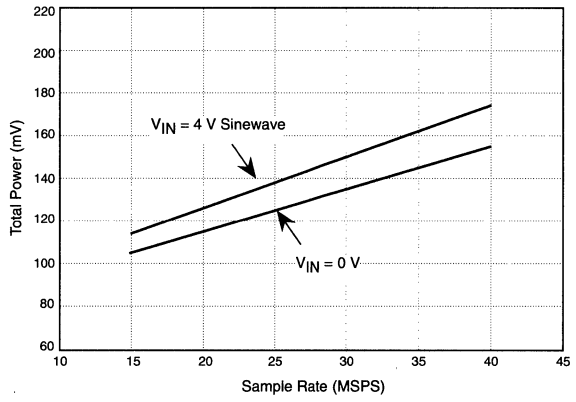
SNR, THD and SINAD vs Input Frequency



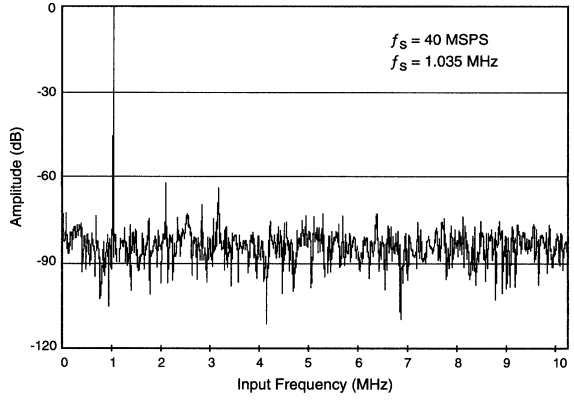
SNR and THD vs Input Range



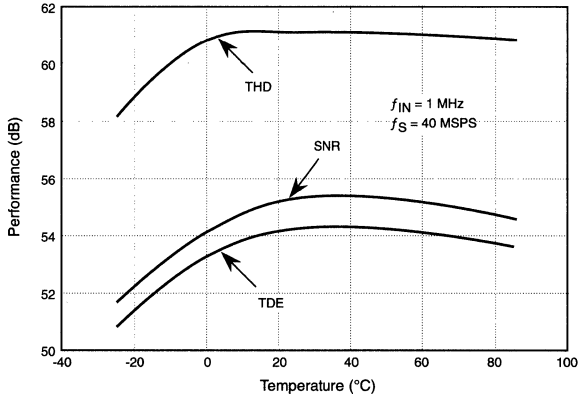
Power Dissipation vs Sample Rate



Spectral Response



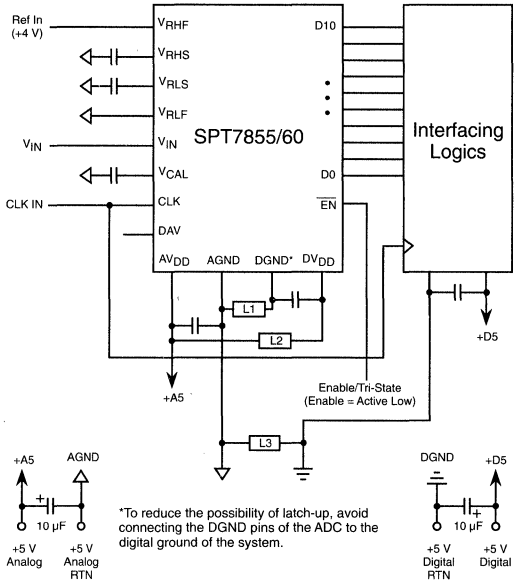
Performance vs Temperature



TYPICAL INTERFACE CIRCUIT

Figure 1 shows the typical interface requirements when using the SPT7860 in normal circuit operation. To reduce the possibility of latch-up, avoid connecting the DGND pins of the ADC to the digital ground of the system. The following sections provide descriptions of the major functions and outline critical performance criteria to consider for achieving the optimal device performance.

Figure 1 - Typical Interface Circuit



NOTES: 1) L3 is to be located as closely to the device as possible.
2) There should be no additional connections to the right of L1 and L2.
3) All capacitors are 0.1 µF surface-mount unless otherwise specified.
4) L1, L2 and L3 are 10 µH inductors or ferrite beads.

POWER SUPPLIES AND GROUNDING

SPT suggests that both the digital and the analog supply voltages on the SPT7860 be derived from a single analog supply as shown in figure 1. A separate digital supply should be used for all interface circuitry. SPT suggests using this power supply configuration to prevent a possible latch-up condition on power up.

OPERATING DESCRIPTION

The general architecture for the CMOS ADC is shown in the block diagram. The design contains 16 identical successive approximation ADC sections, all operating in parallel, a 16-phase clock generator, an 11-bit 16:1 digital output multiplexer, correction logic, and a voltage reference generator which provides common reference levels for each ADC section.

The high sample rate is achieved by using multiple SAR ADC sections in parallel, each of which samples the input signal in sequence. Each ADC uses 16 clock cycles to complete a conversion. The clock cycles are allocated as follows:

Clock	Operation
1	Reference zero sampling
2	Auto-zero comparison
3	Auto-calibrate comparison
4	Input sample
5-15	11-bit SAR conversion
16	Data transfer

The 16 phase clock, which is derived from the input clock, synchronizes these events. The timing signals for adjacent ADC sections are shifted by one clock cycle so that the analog input is sampled on every cycle of the input clock by exactly one ADC section. After 16 clock periods, the timing cycle repeats. The latency from analog input sample to the corresponding digital output is 12 clock cycles.

- Since only 16 comparators are used, a huge power savings is realized.
- The auto-zero operation is done using a closed loop system that uses multiple samples of the comparators response to a reference zero.
- The auto-calibrate operation, which calibrates the gain of the MSB reference and the LSB reference, is also done with a closed loop system. Multiple samples of the gain error are integrated to produce a calibration voltage for each ADC section.
- Capacitive displacement currents, which can induce sampling error, are minimized since only one comparator samples the input during a clock cycle.
- The total input capacitance is very low since sections of the converter which are not sampling the signal are isolated from the input by transmission gates.

VOLTAGE REFERENCE

The SPT7860 requires the use of a single external voltage reference for driving the high side of the reference ladder. It must be within the range of 3 V to 5 V. The lower side of the ladder is typically tied to AGND (0.0 V), but can be run up to 2.0 V with a second reference. The analog input voltage range will track the total voltage difference measured between the ladder sense lines, V_{RHS} and V_{RLS}.

Force and sense taps are provided to ensure accurate and stable setting of the upper and lower ladder sense line voltages across part-to-part and temperature variations. By using the configuration shown in figure 2, offset and gain errors of less than ±2 LSB can be obtained.

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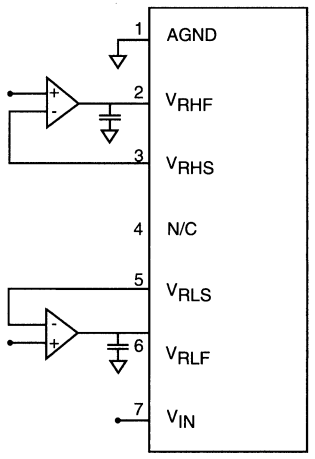
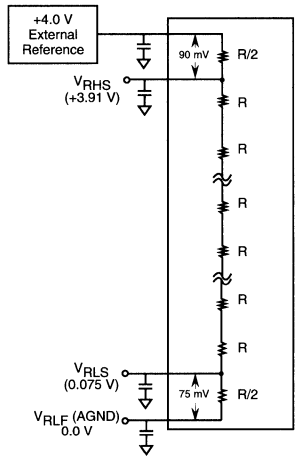
Figure 2 - Ladder Force/Sense Circuit



All capacitors are 0.01 µF

Figure 3 - Simplified Reference Ladder Drive Circuit Without Force/Sense Circuit



R=30 Ω (typ)
All capacitors are 0.01 µF

In cases where wider variations in offset and gain can be tolerated, V_{Ref} can be tied directly to V_{RHF} and AGND can be tied directly to V_{RLF} as shown in figure 3. Decouple force and sense lines to AGND with a .01 µF capacitor (chip cap preferred) to minimize high-frequency noise injection. If this simplified configuration is used, the following considerations should be taken into account:

The reference ladder circuit shown in figure 3 is a simplified representation of the actual reference ladder with force and sense taps shown. Due to the actual internal structure of the ladder, the voltage drop from V_{RHF} to V_{RHS} is not equivalent to the voltage drop from V_{RLF} to V_{RLS}.

Typically, the top side voltage drop for V_{RHF} to V_{RHS} will equal:

$V_{RHF} - V_{RHS}$ = 2.25 % of ($V_{RHF} - V_{RLF}$) (typical),

and the bottom side voltage drop for V_{RLS} to V_{RLF} will equal:

$V_{RLS} - V_{RLF}$ = 1.9 % of ($V_{RHF} - V_{RLF}$) (typical).

Figure 3 shows an example of expected voltage drops for a specific case. Vref of 4.0 V is applied to V_{RHF} and V_{RLF} is tied to AGND. A 90 mV drop is seen at V_{RHS} (= 3.91 V) and a 75 mV increase is seen at V_{RLS} (= 0.075 V).

ANALOG INPUT

V_{IN} is the analog input. The input voltage range is from V_{RLS} to V_{RHS} (typically 4.0 V) and will scale proportionally with respect to the voltage reference. (See voltage reference section.)

The drive requirements for the analog inputs are very minimal when compared to most other converters due to the SPT7860's extremely low input capacitance of only 5 pF and very high input resistance in excess of 250 kΩ.

The analog input should be protected through a series resistor and diode clamping circuit as shown in figure 4.

CALIBRATION

The SPT7860 uses an auto calibration scheme to ensure 10-bit accuracy over time and temperature. Gain and offset errors are continually adjusted to 10-bit accuracy during device operation. This process is completely transparent to the user.

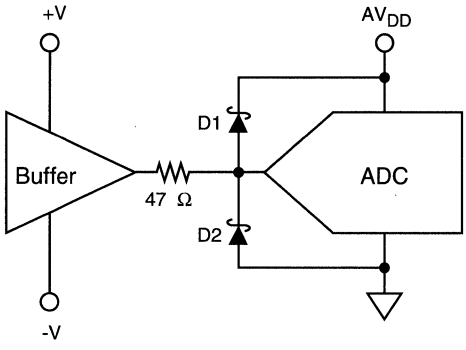
Upon power-up, the SPT7860 begins its calibration algorithm. In order to achieve the calibration accuracy required, the offset and gain adjustment step size is a fraction of a 10-bit LSB. Since the calibration algorithm is an oversampling process, a minimum of 10,000 clock cycles are required. This results in a minimum calibration time upon power-up of 250 µsec (for a 40 MHz clock). Once calibrated, the SPT7860 remains calibrated over time and temperature.

Since the calibration cycles are initiated on the rising edge of the clock, the clock must be continuously applied for the SPT7860 to remain in calibration.

INPUT PROTECTION

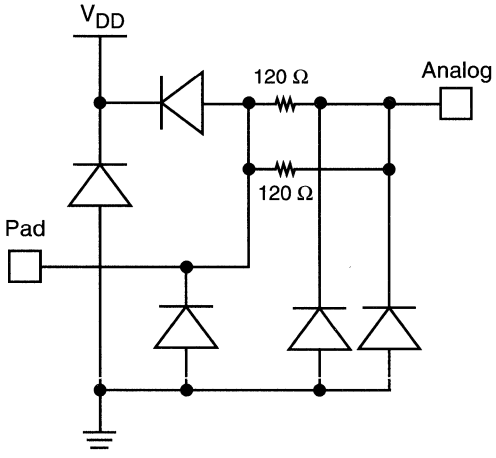
All I/O pads are protected with an on-chip protection circuit shown in figure 5. This circuit provides ESD robustness to 3.5 kV and prevents latch-up under severe discharge conditions without degrading analog transition times.

Figure 4 - Recommended Input Protection Circuit



D1 = D2 = Hewlett Packard HP5712 or equivalent

Figure 5 - On-Chip Protection Circuit



CLOCK INPUT

The SPT7860 is driven from a single-ended TTL-input clock. Because the pipelined architecture operates on the rising edge of the clock input, the device can operate over a wide range of input clock duty cycles without degrading the dynamic performance.

DIGITAL OUTPUTS

The format of the output data (D0-D9) is straight binary. (See table 2.) The outputs are latched on the rising edge of CLK. These outputs can be switched into a tri-state mode by bringing $\overline{EN}$ high.

Table 2 - Output Data Information

ANALOG INPUT	OVERRANGE D10	OUTPUT CODE D9-D0
+F.S. + 1/2 LSB	1	11 1111 1111
+F.S. -1/2 LSB	O	11 1111 111Ø
+1/2 F.S.	O	ØØ ØØØØ ØØØØ
+1/2 LSB	O	OO OOOO OOOØ
0.0 V	O	OO OOOO OOOO

(Ø indicates the flickering bit between logic 0 and 1).

OVERRANGE OUTPUT

The OVERRANGE OUTPUT (D10) is an indication that the analog input signal has exceeded the positive full scale input voltage by 1 LSB. When this condition occurs, D10 will switch to logic 1. All other data outputs (D0 to D9) will remain at logic 1 as long as D10 remains at logic 1. This feature makes it possible to include the SPT7860 into higher resolution systems.

EVALUATION BOARD

The EB7860 evaluation board is available to aid designers in demonstrating the full performance of the SPT7860. This board includes a reference circuit, clock driver circuit, output data latches and an on-board reconstruction of the digital data. An application note describing the operation of this board as well as information on the testing of the SPT7860 is also available. Contact the factory for price and availability.

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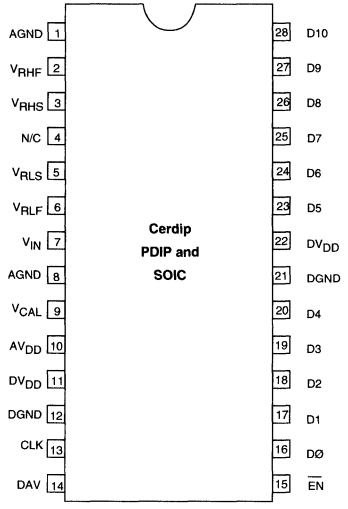
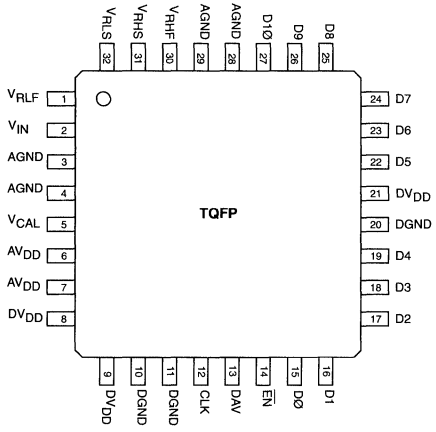
PIN ASSIGNMENTS





PIN FUNCTIONS

NAME	FUNCTION
AGND	Analog Ground
V_{RHF}	Reference High Force
V_{RHS}	Reference High Sense
V_{RLS}	Reference Low Sense
V_{RLF}	Reference Low Force
V_{CAL}	Calibration Reference
V_{IN}	Analog Input
AV_{DD}	Analog V_{DD}
DV_{DD}	Digital V_{DD}
DGND	Digital Ground
CLK	Input Clock f_{CLK} =fs (TTL)
$\overline{EN}$	Output Enable
D0-9	Tri-State Data Output, (DØ=LSB)
D10	Tri-State Output Overrange
DAV	Data Valid Output

LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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SIGNAL PROCESSING TECHNOLOGIES

SPT7861

10-BIT, 40 MSPS,160 mW A/D CONVERTER

ADVANCED INFORMATION

3

FEATURES

- Monolithic 40 MSPS Converter
- 160 mW Power Dissipation
- On-Chip Track-and-Hold
- Single +5 V Power Supply
- TTL/CMOS Outputs
- 5 pF Input Capacitance
- Low Cost
- Tri-State Output Buffers
- High ESD Protection: 3,500 V Minimum

APPLICATIONS

- All High-Speed Applications Where Low Power Dissipation is Required
- Video Imaging
- Medical Imaging
- Radar Receivers
- IR Imaging
- Digital Communications

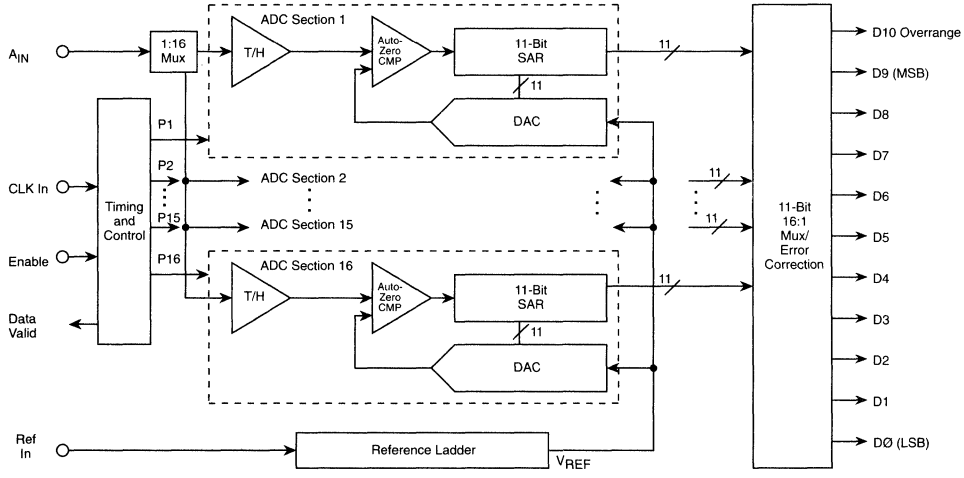
GENERAL DESCRIPTION

The SPT7861 is a 10-bit monolithic, low cost, ultra-low power analog-to-digital converter capable of minimum word rates of 40 MSPS. This is a pin-compatible improved version of the SPT7860. The on-chip track-and-hold function assures very good dynamic performance without the need for external components. The input drive requirements are minimized due to the SPT7861's low input capacitance of only 5 pF.

Power dissipation is extremely low at only 160 mW typical at 40 MSPS with a power supply of +5.0 V. The SPT7861 is pin-compatible with the entire family of SPT 10-bit, CMOS converters (SPT7835/40/50/55/60) which simplifies upgrades. The SPT7861 has incorporated proprietary circuit design (*) and CMOS processing technologies to achieve its advanced performance. Inputs and outputs are TTL/CMOS compatible to interface with TTL/CMOS logic systems. Output data format is straight binary.

The SPT7861 is available in 28-lead 300 mil PDIP, 28-lead SOIC and 32-lead small (7 mm square) TQFP packages over the temperature range of 0 to +70 °C. For extended temperature ranges, consult the factory.

BLOCK DIAGRAM



*PATENT PENDING

ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages

AV_{DD} ..... +6 V
DV_{DD} ..... +6 V

Input Voltages

Analog Input ..... -0.5 V to AV_{DD} +0.5 V
V_{REF} ..... 0 to AV_{DD}
CLK Input ..... V_{DD}
AV_{DD} - DV_{DD} ..... ±100 mV
AGND - DGND ..... ±100 mV

Output

Digital Outputs ..... 10 mA

Temperature

Operating Temperature ..... 0 to 70 °C
Junction Temperature ..... 175 °C
Lead Temperature, (soldering 10 seconds) ..... 300 °C
Storage Temperature ..... -65 to +150 °C

Note: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

T_A=25 °C, AV_{DD} = DV_{DD} = +5.0 V, V_{IN} = 0 to 4 V, f_S = 40 MSPS, V_{RHS} = 4.0 V, V_{RLS} = 0.0 V, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
Resolution			10			Bits
DC Accuracy						
Integral Nonlinearity		I		±1.0		LSB
Differential Nonlinearity		I		±0.5		LSB
No Missing Codes		I		Guaranteed		
Analog Input						
Input Voltage Range		I	V_{RLS}		V_{RHS}	V
Input Resistance		I	250			kΩ
Input Capacitance		V		5.0		pF
Input Bandwidth	(Small Signal)	V	250			MHz
Offset		V		±2.0		LSB
Gain Error		V		±2.0		LSB
Reference Input						
Resistance		I	500	600	700	Ω
Bandwidth		V	100	150		MHz
Voltage Range						
V_{RLS}		IV	0	-	2.0	V
V_{RHS}		IV	3.0	-	AV_{DD}	V
V_{RHS} - V_{RLS}		V	1.0	4.0	5.0	V
$\Delta(V_{RHF} - V_{RHS})$		V		90		mV
$\Delta(V_{RLS} - V_{RLF})$		V		75		mV
Reference Settling Time						
V_{RHS}		V		15		Clock Cycles
V_{RLS}		V		20		Clock Cycles
Conversion Characteristics						
Maximum Conversion Rate		I	40			MHz
Minimum Conversion Rate		IV	2			MHz
Pipeline Delay (Latency)		IV			12	Clock Cycles
Aperture Delay Time		V		4.0		ns
Aperture Jitter Time		V		15		ps(p-p)
Dynamic Performance	T_A = +25 °C					
Effective Number of Bits						
fin=3.58 MHz		I		9.2		Bits
fin=10.3 MHz		I		9.0		Bits

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ELECTRICAL SPECIFICATIONS

T_A=25 °C, AV_{DD} = DV_{DD} = +5.0 V, V_{IN} = 0 to 4 V, f_S = 40 MSPS, V_{RHS} = 4.0 V, V_{RLS} = 0.0 V, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
Dynamic Performance	T_A = +25 °C					
Signal-to-Noise Ratio (without Harmonics)						
fin=3.58 MHz		I		58		dB
fin=10.3 MHz		I		57		dB
Harmonic Distortion	(9 Distortion bins from					
f_{IN}=3.58 MHz	1024 pt FFT)	I		62		dB
f_{IN}=10.3 MHz		I		58		dB
Signal-to-Noise and Distortion (SINAD)						
fin=3.58 MHz		I		57		dB
fin=10.3 MHz		I		56		dB
Spurious Free Dynamic Range	f_{IN}=1.0 MHz	V		64		dB
Differential Phase		V		TBD		Degree
Differential Gain				TBD		%
Intermodulation Distortion				TBD		dB
Inputs						
Logic "1" Voltage		I	2.0			V
Logic "0" Voltage		I			0.8	V
Maximum Input Current Low		I	-10		+10	µA
Maximum Input Current High		I	-10		+10	µA
Input Capacitance		V		+5		pF
Digital Outputs						
Logic "1" Voltage	I_{OH} = 0.5 mA	I	3.5			V
Logic "0" Voltage	I_{OL} = 1.6 mA	I			0.4	V
t_{RISE}	15 pF load	V		10		ns
t_{FALL}	15 pF load	V		10		ns
Output Enable to Data Output Delay	20 pF load, T_A = +25 °C	V		10		ns
	50 pF load over temp.	V		22		ns
Power Supply Requirements						
Voltages	DV_{DD}	IV	4.75	5.0	5.25	V
	AV_{DD}	IV	4.75	5.0	5.25	V
Currents	AI_{DD}	I		14	19	mA
	DI_{DD}	I		18	23	mA
Power Dissipation		I		160	210	mW

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests; therefore, $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

Figure 1A: Timing Diagram 1

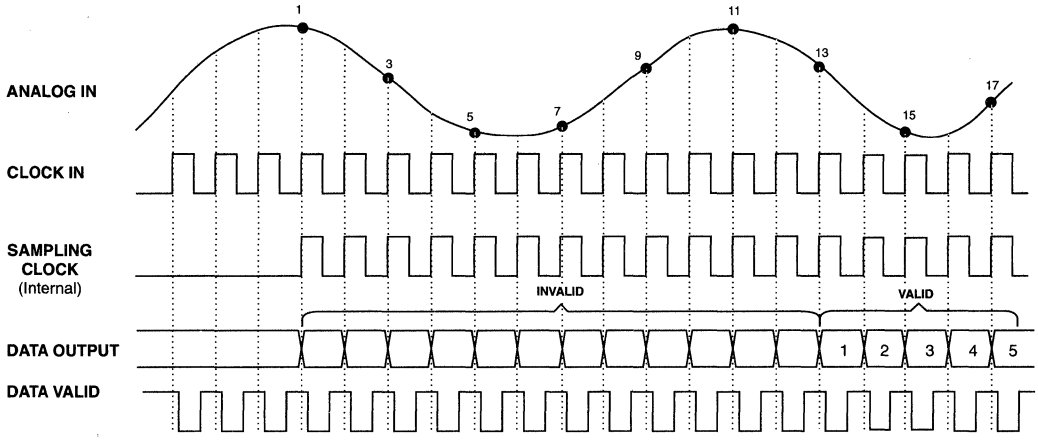

Figure 1B: Timing Diagram 2

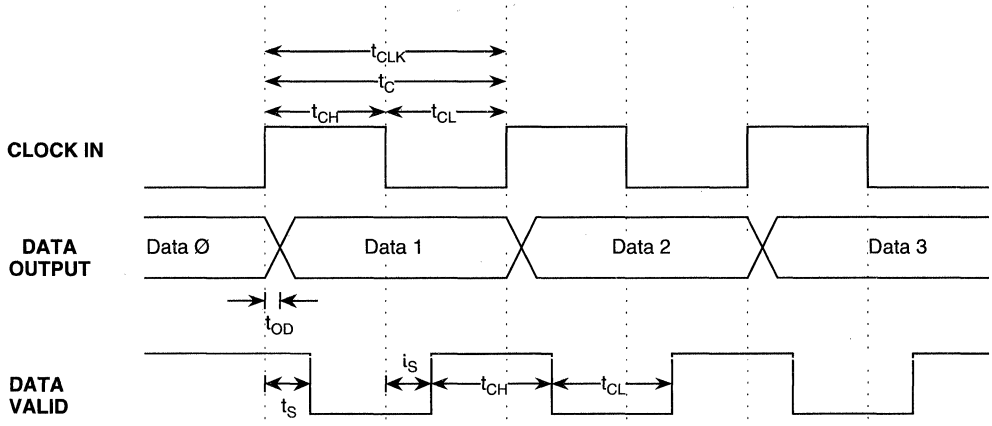

Table 1 - Timing Parameters

DESCRIPTION	PARAMETERS	MIN	TYP	MAX	UNITS
Conversion Time	t_C	t_{CLK}			ns
Clock Period	t_{CLK}	25			ns
Clock High Duty Cycle	t_{CH}	40	50	60	%
Clock Low Duty Cycle	t_{CL}	40	50	60	%
Clock to Output Delay (15 pF Load)	t_{OD}		17		ns
Clock to DAV	t_S		10		ns

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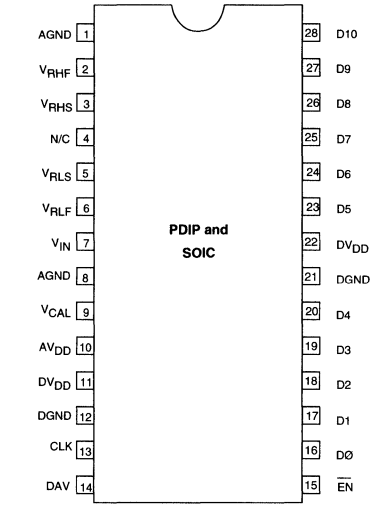
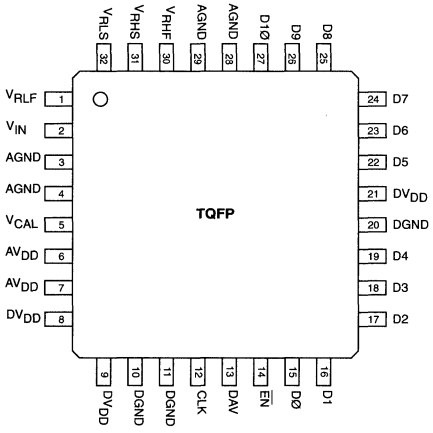
PIN ASSIGNMENTS





PIN FUNCTIONS

NAME	FUNCTION
AGND	Analog Ground
V_{RHF}	Reference High Force
V_{RHS}	Reference High Sense
V_{RLS}	Reference Low Sense
V_{RLF}	Reference Low Force
V_{CAL}	Calibration Reference
V_{IN}	Analog Input
AV_{DD}	Analog V_{DD}
DV_{DD}	Digital V_{DD}
DGND	Digital Ground
CLK	Input Clock f_{CLK} =fs (TTL)
$\overline{EN}$	Output Enable
D0-9	Tri-State Data Output, (DØ=LSB)
D10	Tri-State Output Overrange
DAV	Data Valid Output

LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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SIGNAL PROCESSING TECHNOLOGIES

SPT7870

10-BIT, 100 MSPS ECL A/D CONVERTER

ADVANCED INFORMATION

3

FEATURES

- 10-Bit, 100 MSPS Analog-to-Digital Converter
- Monolithic Bipolar
- -1.0 V to +1.0 V Analog Input Range
- Internal Sample-and-Hold
- Internal Voltage Reference
- Power Dissipation of 1.4 Watts
- Single Ended ECL Outputs
- MIL-STD-883 Compliant Versions

APPLICATIONS

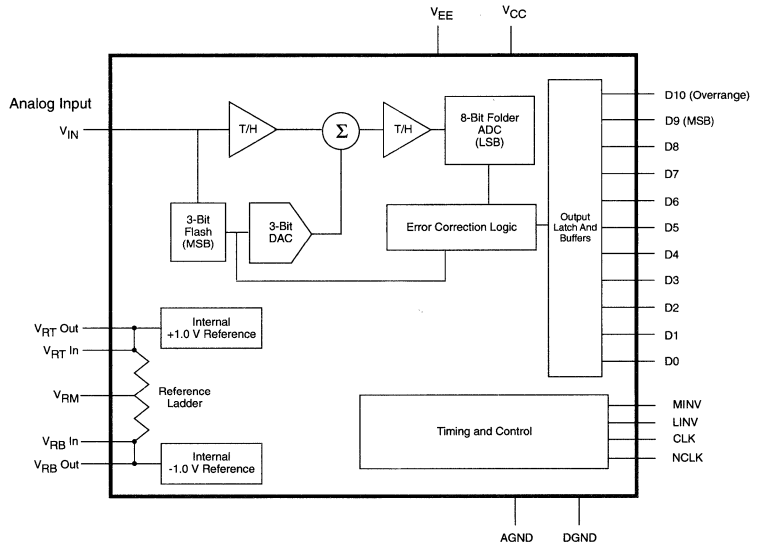
- Professional Video
- HDTV
- Communications
- Imaging
- Digital Oscilloscopes

GENERAL DESCRIPTION

The SPT 10-Bit, 100 MSPS analog-to-digital converter, with its two stage sub-ranging flash/folder architecture, delivers very high performance at a fraction of the power of other flash type converters in this performance class. Power dissipation, including the internal voltage reference is only 1.4 W typical. The device supports high speed ECL outputs.

The resolution and performance of this device makes it well suited for professional video and HDTV applications. The on-board track-and-hold provides for excellent AC performance enabling this device to be a converter of choice for RF communications and digital sampling oscilloscopes. The SPT7870 is available in 32L sidebrazed and 44L cerquad packages in the industrial temperature range. Contact the factory for availability of military and /883 versions.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING (Beyond which damage may occur)[1]

Supply Voltages
- V_{CC} ..... +6 V
- V_{EE} ..... -6 V

Input Voltages
- Analog Input ..... $V_{EE} \leq V_{IN} \leq V_{CC}$
- V_{RT}, V_{RB} ..... +1.5 V, -1.5 V
- Reference Ladder Current ..... 12 mA

Output
- Digital Outputs ..... +30 to -30 mA

Temperature
- Operating Temperature ..... -25 to + 85 °C
- Junction Temperature ..... + 175 °C
- Lead, Soldering (10 seconds) ..... + 300 °C
- Storage ..... -60 to + 150 °C

Note: 1. Operation at any Absolute Maximum Ratings is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

$T_A=T_{min}$ - T_{max}, V_{CC}=+5.0 V, V_{EE}=-5.2 V, V_{IN}=±1.0 V, V_{RB}=-1.0 V, V_{RT}=+1.0 V, f_{clock}=100 MHz, 50% clock duty cycle, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
DC Performance						
Resolution				10		Bits
Differential Linearity				±0.75		LSB
Integral Linearity	+25 °C			±1.0	±2.0	LSB
Full Temp.				±2.5		LSB
No Missing Codes				Guaranteed		
Analog Input						
Input Voltage Range				±1.0		V
Input Bias Current				100		µA
Input Resistance	+25 °C			300		kΩ
	Full Temperature			100		kΩ
Input Capacitance	+25 °C			5	10	pF
Input Bandwidth	+25 °C (Small Signal)		175	200		MHz
±FS Error				15	70	LSB
Voltage Reference						
Ref. Ladder Resistance			600	800	1000	Ω
Ref. Ladder Temp. Coefficient				0.1		Ω/°C
Full Scale Drift with Temperature				±0.1		mV/°C
Timing Characteristics						
Conversion Rate			100	110		MSPS
Pipeline Delay (Latency)				1		Clock
Transient Response				10		ns
Overvoltage Recovery Time				10		ns
Output Delay (t_d)				3		ns
Aperture Delay Time				1		ns
Aperture Jitter Time				5		ps (rms)
Dynamic Performance						
Effective Number of Bits	Full Temperature					
f_{in} = 3.58 MHz				9.0		Bits
f_{in} = 25.0 MHz				8.7		Bits
f_{in} = 50.0 MHz				8.0		Bits

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ELECTRICAL SPECIFICATIONS

$T_A=T_{min}$ - T_{max}, V_{CC}=+5.0 V, V_{EE}=-5.2 V, V_{IN}=±1.0 V, V_{RB}=-1.0 V, V_{RT}=+1.0 V, f_{clock}=100 MHz, 50% clock duty cycle, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
Dynamic Performance						
Signal-To-Noise Ratio	Full Temperature					
f_{in} = 3.58 MHz				56		dB
f_{in} = 25.0 MHz				56		dB
f_{in} = 50.0 MHz				53		dB
Harmonic Distortion (Full Temp.)						
f_{in} = 3.58 MHz				65		dB
f_{in} = 25.0 MHz				58		dB
f_{in} = 50.0 MHz				53		dB
Spurious Free Dynamic Range						
f_{in} = 3.58 MHz				65		dB
f_{in} = 25.0 MHz				58		dB
f_{in} = 50.0 MHz				53		dB
Two-Tone Intermodulation						
Dist. Rejection	+25 °C		70			dB
Differential Phase	+25 °C			0.5		Degree
Differential Gain	+25 °C			1		%
Power Supply Requirements						
+V_S Supply Voltage			4.75	5.0	5.25	V
- V_S Supply Voltage			-4.90	-5.2	-5.50	V
+V_S Supply Current				150		mA
- V_S Supply Current				140		mA
Power Dissipation with						
Internal Voltage Reference				1.4	1.7	W
Power Supply Rejection Ratio				6	10	mV/V
Clock Inputs[1]						
Difference ICLK-NCLKI			0.5		2.0	V
Common Mode .5 (CLK+NCLK)			-1.5		+1.5	V
Input Current			-1		+1	mA
Pulse Width Low (CLK)			4.5			ns
Pulse Width High (CLK)			4.5		300	ns
Digital Outputs						
Logic 1 Voltage	50 Ω to -2 V		-1.1	-0.9		V
Logic 0 Voltage	50 Ω to -2 V			-1.7	-1.5	V

[1]Clock accepts both ECL and TTL input levels. ECL may be driven single ended or differential.

TEST LEVEL CODES

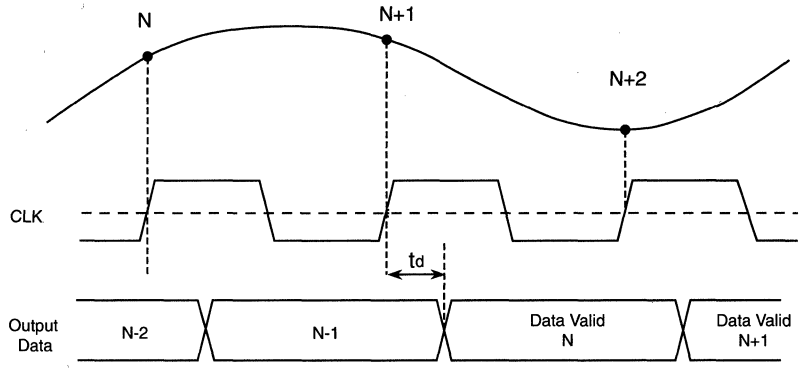
All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests; therefore, $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

Figure 1 - Timing Diagram



THEORY OF OPERATION

The SPT7870 is uses a two stage subranging architecture incorporating a 3-bit flash MSB conversion stage followed by an 8-bit interpolating folder conversion stage. Digital error correction logic combines the results of both stages to produce a 10-bit data conversion digital output.

The analog signal is input directly to the 3-bit flash converter which performs a 3-bit conversion and in turn drives an internal DAC used to set the second stage voltage reference level. The 3-bit result from the flash conversion is input to the digital error correction logic and used in calculation of the upper most significant bits of the data output.

The analog input is also input directly to an internal track-and-hold amplifier. The signal is held and amplified for use in the second stage conversion. The output of the this track-and-hold is input into a summing junction that takes the difference between the track-and-hold amplifier and the 3-bit DAC output. The residual is captured by a second track-and-hold which holds and amplifies this residual voltage.

The residual held by the track-and-hold amplifier is input to an 8-bit interpolating folder stage for data conversion. The 8-bit converted data from the folder stage is input into the digital error correction logic and used in calculation of the lower significant bits.

The error correction logic incorporates a proprietary scheme for compensation of any internal offset and gain errors that might exist to determine the 10-bit conversion result. The resultant 10-bit data conversion is internally latched and presented on the data output pins via buffered output drivers.

CLOCK INPUTS

The clock inputs are designed to be driven differentially with ECL levels. For optimal noise performance, the clock input slew rate should be a minimum of 2 ns. Because of this, the use of *fast* logic is recommended. The clock input duty cycle should be 50% where possible. The analog input signal is latched on the rising edge of the CLK.

The clock may be driven single-ended since the NOT CLK pin is internally biased to -1.3 V. NOT CLK may be left open but a .01 µF bypass capacitor from NOT CLK to AGND is recommended. NOTE: System performance may be degraded due to increased clock noise or jitter.

VOLTAGE REFERENCE

The SPT7870 incorporates an on-board voltage reference. The top and bottom reference voltages are each internally tied to their respective top and bottom of the internal reference ladder. The pins for the voltage references and the ladder, including the center of the ladder are brought out to pins on the device. These pins are for decoupling purposes only. A .01 µF capacitor should be used on each pin and tied to AGND.

The internal voltage reference and the internal error correction logic eliminate the need for driving externally the voltage reference ladder. In fact, *the voltage reference ladder should not be driven* with and external voltage reference source as the internal error correction circuitry already compensates for the internal voltage and no improvement will result.

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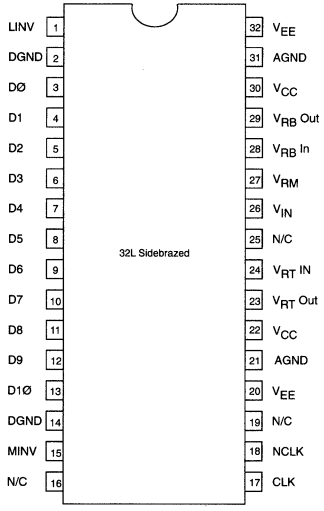
DIGITAL OUTPUTS

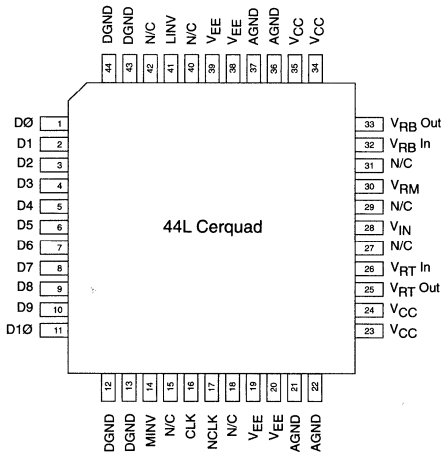
The format of the output data (DO - D9) is straight binary. (See table 1.) The outputs are latched on the rising edge of the CLK with a propagation delay of 3 ns (typ). There is a one clock cycle latency between CLK and valid data output data. (See the timing diagram.)

Table 1 - Data Output Coding

ANALOG INPUT	OVERRANGE D10	OUTPUT CODE D9 - D0
>+1.0 V + 1/2 LSB	1	11 1111 1111
+1.0 V - 1 LSB	O	11 1111 111Ø
0.0 V	O	ØØ ØØØØ ØØØØ
-1.0 V + 1 LSB	O	OO OOOO OOOØ
<-1.0 V	O	OO OOOO OOOO

PIN ASSIGNMENTS





PIN FUNCTIONS

V_{IN}	Analog Input
D_0-D_9	Digital Output Data
D_{10}	Overflow
CLK	Clock
NCLK	Inverted Clock
LINV	Least Significant Bits (D_0 - D_8 Inverted)
MINV	Most Significant Bit (D_9 Inverted)
V_{RT} In	Top of Reference Ladder
V_{RT} Out	Internal Top Ref Out
V_{RB} In	Bottom of Reference Ladder
V_{RB} Out	Internal Bottom Ref Out
V_{CC}	+5 V Analog Supply
V_{RM}	Reference Ladder Center Tap
V_{EE}	-5.2 V Supply
N/C	Not Connected
AGND	Analog Ground
DGND	Digital Ground

LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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SIGNAL PROCESSING TECHNOLOGIES

SPT7871

10-BIT, 100 MSPS TTL A/D CONVERTER

ADVANCED INFORMATION

3

FEATURES

- 10-Bit, 100 MSPS Analog-to-Digital Converter
- Monolithic Bipolar
- -1.0 V to +1.0 V Analog Input Range
- Internal Sample-and-Hold
- Internal Voltage Reference
- Power Dissipation of 1.3 Watts
- Single Ended TTL Outputs
- MIL-STD-883 Compliant Versions

APPLICATIONS

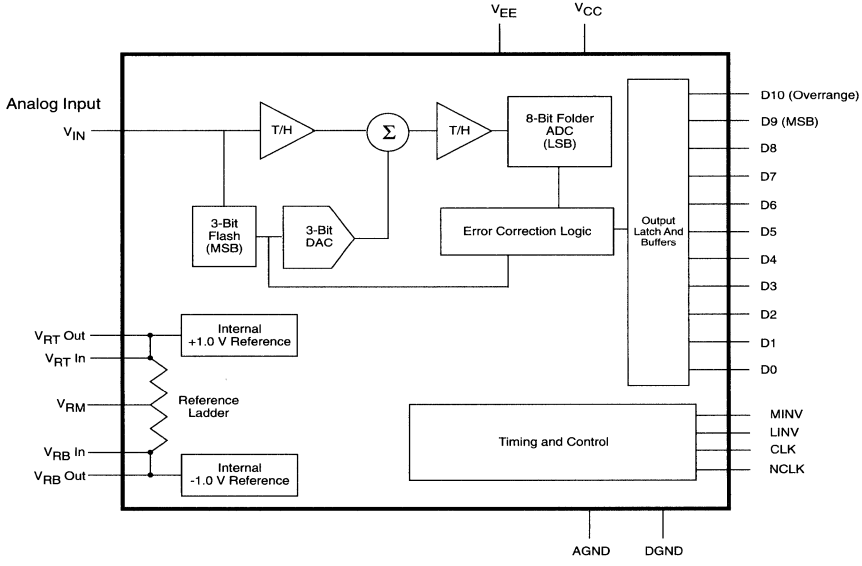
- Professional Video
- HDTV
- Communications
- Imaging
- Digital Oscilloscopes

GENERAL DESCRIPTION

The SPT 10-bit, 100 MSPS analog-to-digital converter, with its two stage sub-ranging flash/folder architecture, delivers very high performance at a fraction of the power of other flash type converters in this performance class. Power dissipation, including the internal voltage reference is only 1.3 W typical. The device supports high speed TTL outputs.

The resolution and performance of this device makes it well suited for professional video and HDTV applications. The on-board track-and-hold provides for excellent AC performance enabling this device to be a converter of choice for RF communications and digital sampling oscilloscopes. The SPT7871 is available in 32L sidebrazed and 44L cerquad packages in the industrial temperature range. Contact the factory for availability of military and /883 versions.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING (Beyond which damage may occur)[1]

Supply Voltages
- AV_{CC} ..... +6 V
- DV_{CC} ..... +6 V
- V_{EE} ..... -6 V

Input Voltages
- Analog Input ..... $V_{EE} \leq V_{IN} \leq V_{CC}$
- V_{RT}, V_{RB} ..... +1.5 V, -1.5 V
- Reference Ladder Current ..... 12 mA

Output
- Digital Outputs ..... +30 to -30 mA

Temperature
- Operating Temperature ..... -25 to + 85 °C
- Junction Temperature ..... + 175 °C
- Lead, Soldering (10 seconds) ..... + 300 °C
- Storage ..... -60 to + 150 °C

Note: 1. Operation at any Absolute Maximum Ratings is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

$T_A=T_{min}$ - T_{max}, V_{CC}=+5.0 V, V_{EE}=-5.2 V, V_{IN}=±1.0 V, V_{RB}=-1.0 V, V_{RT}=+1.0 V, f_{clock}=100 MHz, 50% clock duty cycle, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
DC Performance						
Resolution				10		Bits
Differential Linearity				±0.75		LSB
Integral Linearity	+25 °C			±1.0	±2.0	LSB
Full Temp.				±2.5		LSB
No Missing Codes				Guaranteed		
Analog Input						
Input Voltage Range				±1.0		V
Input Bias Current				100		µA
Input Resistance	+25 °C			300		kΩ
	Full Temperature			100		kΩ
Input Capacitance	+25 °C			5	10	pF
Input Bandwidth	+25 °C (Small Signal)		175	200		MHz
±FS Error				15	70	LSB
Voltage Reference						
Ref. Ladder Resistance			600	800	1000	Ω
Ref. Ladder Temp. Coefficient				0.1		Ω/°C
Full Scale Drift with Temperature				±0.1		mV/°C
Timing Characteristics						
Conversion Rate			100	110		MSPS
Pipeline Delay (Latency)				1		Clock
Transient Response				10		ns
Overvoltage Recovery Time				10		ns
Output Delay (t_d)				3		ns
Aperture Delay Time				1		ns
Aperture Jitter Time				5		ps (rms)
Dynamic Performance						
Effective Number of Bits	Full Temperature					
f_{in} = 3.58 MHz				9.0		Bits
f_{in} = 25.0 MHz				8.7		Bits
f_{in} = 50.0 MHz				8.0		Bits

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ELECTRICAL SPECIFICATIONS

$T_A=T_{min}$ - T_{max}, V_{CC}=+5.0 V, V_{EE}=-5.2 V, V_{IN}=±1.0 V, V_{RB}=-1.0 V, V_{RT}=+1.0 V, f_{clock}=100 MHz, 50% clock duty cycle, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
Dynamic Performance						
Signal-To-Noise Ratio	Full Temperature					
f_{in} = 3.58 MHz				56		dB
f_{in} = 25.0 MHz				56		dB
f_{in} = 50.0 MHz				53		dB
Harmonic Distortion (Full Temp.)						
f_{in} = 3.58 MHz				65		dB
f_{in} = 25.0 MHz				58		dB
f_{in} = 50.0 MHz				53		dB
Spurious Free Dynamic Range						
f_{in} = 3.58 MHz				65		dB
f_{in} = 25.0 MHz				58		dB
f_{in} = 50.0 MHz				53		dB
Two-Tone Intermodulation	f_{in} = 3.58 MHz					
Dist. Rejection	+25 °C		70			dB
Differential Phase	+25 °C			0.5		Degree
Differential Gain	+25 °C			1		%
Power Supply Requirements						
+V_S Supply Voltage			4.75	5.0	5.25	V
- V_S Supply Voltage			-4.9	-5.2	-5.5	V
+V_S Supply Current				200		mA
- V_S Supply Current				60		mA
Power Dissipation with						
Internal Voltage Reference				1.3	1.6	W
Power Supply Rejection Ratio				6	10	mV/V
Clock Inputs[1]						
Difference ICLK-NCLKI			0.5		2.0	V
Common Mode .5 (CLK+NCLK)			-1.5		+1.5	V
Input Current			-1		+1	mA
Pulse Width Low (CLK)			4.5			ns
Pulse Width High (CLK)			4.5		300	ns
Digital Outputs						
Logic 1 Voltage	10 TTL Loads		2.4	2.8		V
Logic 0 Voltage	10 TTL Loads			0.5	0.6	V

[1]Clock accepts both ECL and TTL input levels. ECL may be driven single ended or differential.

TEST LEVEL CODES

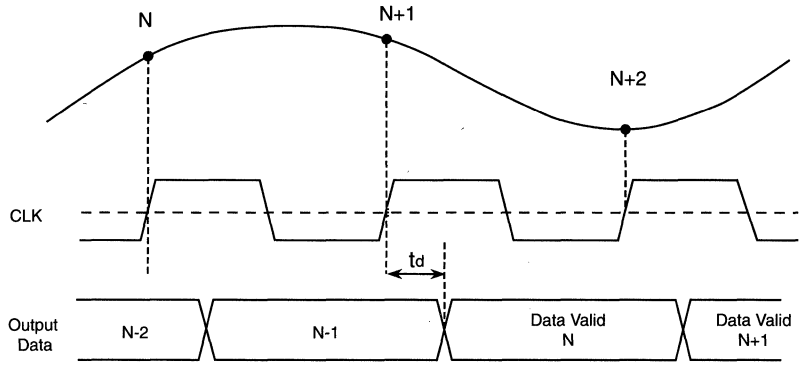
All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests; therefore, $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

Figure 1 - Timing Diagram



THEORY OF OPERATION

The SPT7871 is uses a two stage subranging architecture incorporating a 3-bit flash MSB conversion stage followed by an 8-bit interpolating folder conversion stage. Digital error correction logic combines the results of both stages to produce a 10-bit data conversion digital output.

The analog signal is input directly to the 3-bit flash converter which performs a 3-bit conversion and in turn drives an internal DAC used to set the second stage voltage reference level. The 3-bit result from the flash conversion is input to the digital error correction logic and used in calculation of the upper most significant bits of the data output.

The analog input is also input directly to an internal track-and-hold amplifier. The signal is held and amplified for use in the second stage conversion. The output of the this track-and-hold is input into a summing junction that takes the difference between the track-and-hold amplifier and the 3-bit DAC output. The residual is captured by a second track-and-hold which holds and amplifies this residual voltage.

The residual held by the track-and-hold amplifier is input to an 8-bit interpolating folder stage for data conversion. The 8-bit converted data from the folder stage is input into the digital error correction logic and used in calculation of the lower significant bits.

The error correction logic incorporates a proprietary scheme for compensation of any internal offset and gain errors that might exist to determine the 10-bit conversion result. The resultant 10-bit data conversion is internally latched and presented on the data output pins via buffered output drivers.

CLOCK INPUTS

The clock inputs are designed to be driven differentially with ECL levels. For optimal noise performance, the clock input slew rate should be a minimum of 2 ns. Because of this, the use of *fast* logic is recommended. The clock input duty cycle should be 50% where possible. The analog input signal is latched on the rising edge of the CLK.

The clock may be driven single-ended since the NOT CLK pin is internally biased to -1.3 V. NOT CLK may be left open but a .01 µF bypass capacitor from NOT CLK to AGND is recommended. NOTE: System performance may be degraded due to increased clock noise or jitter.

VOLTAGE REFERENCE

The SPT7871 incorporates an on-board voltage reference. The top and bottom reference voltages are each internally tied to their respective top and bottom of the internal reference ladder. The pins for the voltage references and the ladder, including the center of the ladder are brought out to pins on the device. These pins are for decoupling purposes only. A .01 µF capacitor should be used on each pin and tied to AGND.

The internal voltage reference and the internal error correction logic eliminate the need for driving externally the voltage reference ladder. In fact, the *voltage reference ladder should not be driven* with and external voltage reference source as the internal error correction circuitry already compensates for the internal voltage and no improvement will result.

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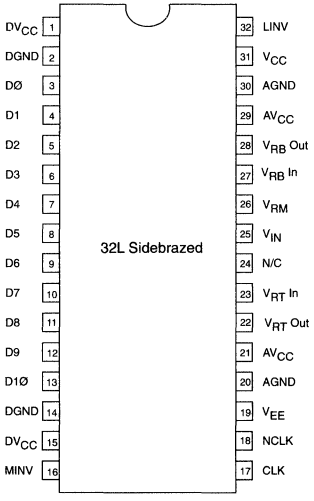
DIGITAL OUTPUTS

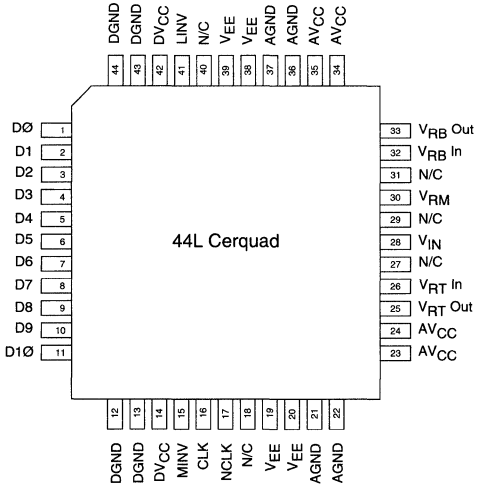
The format of the output data (DO - D9) is straight binary. (See table 1.) The outputs are latched on the rising edge of the CLK with a propagation delay of 3 ns (typ). There is a one clock cycle latency between CLK and valid data output data. (See the timing diagram.)

Table 1 - Data Output Coding

ANALOG INPUT	OVERRANGE D10	OUTPUT CODE D9 - D0
>+1.0 V + 1/2 LSB	1	11 1111 1111
+1.0 V - 1 LSB	O	11 1111 111Ø
0.0 V	O	ØØ ØØØØ ØØØØ
-1.0 V + 1 LSB	O	OO OOOO OOOØ
<-1.0 V	O	OO OOOO OOOO

PIN ASSIGNMENTS





PIN FUNCTIONS

V_{IN}	Analog Input
D_0-D_9	Digital Output Data
D_{10}	Overflow
CLK	Clock
NCLK	Inverted Clock
LINV	Least Significant Bits (D_0 - D_8 Inverted)
MINV	Most Significant Bit (D_9 Inverted)
V_{RT} In	Top of Reference Ladder
V_{RT} Out	Internal Top Ref Out
V_{RB} In	Bottom of Reference Ladder
V_{RB} Out	Internal Bottom Ref Out
AV_{CC}	+5 V Analog Supply
DV_{CC}	+5 V Digital Supply
V_{RM}	Reference Ladder Center Tap
V_{EE}	-5.2 V Supply
N/C	Not Connected
AGND	Analog Ground
DGND	Digital Ground

LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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SIGNAL PROCESSING TECHNOLOGIES

SPT7910

12-BIT, 10 MSPS, ECL, A/D CONVERTER

FEATURES

- Monolithic
- 12-Bit 10 MSPS Converter
- 67 dB SNR @ 500 kHz Input
- On-Chip Track/Hold
- Bipolar ±2.0 V Analog Input
- Low Power (1.4 W Typical)
- 5 pF Input Capacitance
- ECL Outputs

APPLICATIONS

- Radar Receivers
- Professional Video
- Instrumentation
- Medical Imaging
- Electronic Warfare
- Digital Communications
- Digital Spectrum Analyzers
- Electro-Optics

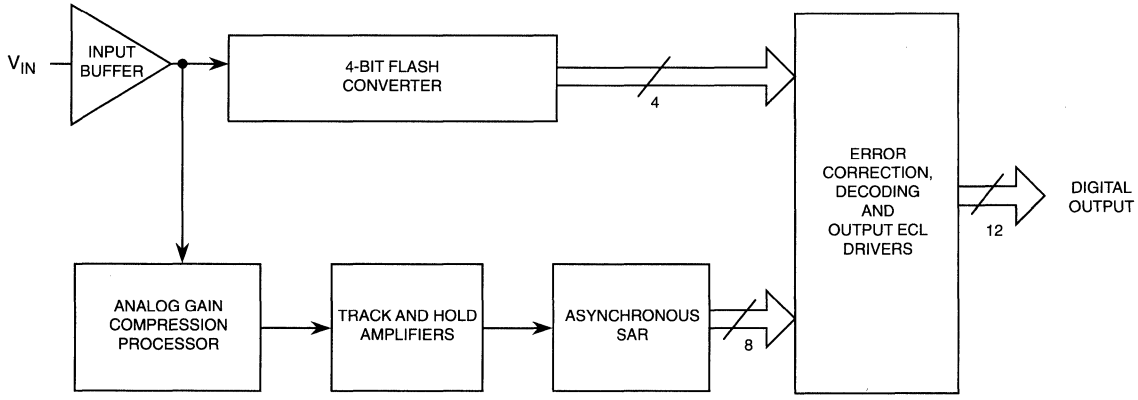
GENERAL DESCRIPTION

The SPT7910 A/D converter is industry's first 12-bit monolithic A-to-D converter capable of sample rates greater than 10 MSPS. On board input buffer and track/hold function assures excellent dynamic performance without the need for external components. Drive requirement problems are minimized with an input capacitance of only 5 pF.

Inputs and outputs are ECL to provide a higher level of noise immunity in high speed system applications. An overrange output signal is provided to indicate overflow conditions. Output data format is straight binary. Power dissipation is very low at only 1.4 watts with power supply voltages of +5.0 and -5.2 volts. The SPT7910 also provides a wide input voltage range of ±2.0 volts.

The SPT7910 is available in a small 32-lead ceramic side-brazed DIP package and in die form. A commercial temperature range of 0 to +70 °C is currently offered. A surface mount package, military temperature, and /883 processed units will be available in the near future.

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages
- V_{CC} ..... +6 V
- V_{EE} ..... -6 V

Input Voltages
- Analog Input ..... $V_{FB} \leq V_{IN} \leq V_{FT}$
- V_{FT}, V_{FB} ..... +3.0 V, -3.0 V
- Reference Ladder Current ..... 12 mA

Output
- Digital Outputs ..... 0 to -30 mA

Temperature
- Operating Temperature ..... 0 to 70 °C
- Junction Temperature ..... 175 °C
- Lead Temperature, (soldering 10 seconds) ..... 300 °C
- Storage Temperature ..... -65 to +150 °C

Note: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

$T_A=T_{MIN}$ to T_{MAX}, V_{CC}=+5.0 V, V_{EE}=-5.2 V, DV_{CC}=+5.0 V, V_{IN}=±2.0 V, V_{SB}=-2.0 V, V_{ST}=+2.0 V, f_{clock}=10 MHz, 50% clock duty cycle, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7910 MIN	SPT7910 TYP	SPT7910 MAX	UNITS
Resolution			12			Bits
DC Accuracy (+25 °C)						
Integral Nonlinearity	± Full Scale	I		±2.0		LSB
Differential Nonlinearity	250 kHz Sample Rate	I		±0.8		LSB
No Missing Codes		I		Guaranteed		
Analog Input						
Input Voltage Range		VI		±2.0		V
Input Bias Current		VI		30	60	µA
Input Resistance	V_{IN}=0 V	VI	100	300		kΩ
Input Capacitance		V		5		pF
Input Bandwidth	3 dB Small Signal	V		120		MHz
+FS Error		V		±5.0		LSB
-FS Error		V		±5.0		LSB
Reference Input						
Reference Ladder Resistance		VI	500	800		Ω
Reference Ladder Tempco		V		0.8		Ω/°C
Timing Characteristics						
Maximum Conversion Rate		VI	10			MHz
Overvoltage Recovery Time		V		20		ns
Pipeline Delay (Latency)		VI			1	Clock Cycle
Output Delay		V		5		ns
Aperture Delay Time		V		1		ns
Aperture Jitter Time		V		5		ps-RMS
Dynamic Performance						
Effective Number of Bits						
fin=500 kHz				10.2		Bits
fin=1.0 MHz				10.0		Bits
fin=3.58 MHz				9.5		Bits

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ELECTRICAL SPECIFICATIONS

$T_A=T_{MIN}$ to T_{MAX}, V_{CC}=+5.0 V, V_{EE}=-5.2 V, DV_{CC}=+5.0 V, V_{IN}=±2.0 V, V_{SB}=-2.0 V, V_{ST}=+2.0 V, f_{clock}=10 MHz, 50% clock duty cycle, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7910 MIN	SPT7910 TYP	SPT7910 MAX	UNITS
Dynamic Performance						
Signal-To-Noise Ratio (without Harmonics)						
fin=500 kHz	+25 °C	I	64	67		dB
	T_{MIN} to T_{MAX}	IV	58	61		dB
fin=1 MHz	+25 °C	I	64	66		dB
	T_{MIN} to T_{MAX}	IV	58	60		dB
fin=3.58 MHz	+25 °C	I	62	64		dB
	T_{MIN} to T_{MAX}	IV	58	60		dB
Harmonic Distortion[2]						
fin=500 kHz	+25 °C	I	63	66		dB
	T_{MIN} to T_{MAX}	IV	59	62		dB
fin=1.0 MHz	+25 °C	I	63	65		dB
	T_{MIN} to T_{MAX}	IV	59	61		dB
fin=3.58 MHz	+25 °C	I	59	61		dB
	T_{MIN} to T_{MAX}	IV	57	59		dB
Signal-to-Noise and Distortion						
fin=500 kHz	+25 °C	I	60	63		dB
	T_{MIN} to T_{MAX}	IV	55	58		dB
fin=1.0 MHz	+25 °C	I	60	62		dB
	T_{MIN} to T_{MAX}	IV	55	57		dB
fin=3.58 MHz	+25 °C	I	57	59		dB
	T_{MIN} to T_{MAX}	IV	54	56		dB
Spurious Free Dynamic Range[3]	+25 °C	V		74		dB
Differential Phase[4]	+25 °C	V		0.2		Degree
Differential Gain[4]	+25 °C	V		0.7		%
Digital Inputs						
Logic "1" Voltage		V	-1.1			V
Logic "0" Voltage		V			-1.5	V
Maximum Input Current Low		VI	-500	±200	+750	µA
Maximum Input Current High		VI	-500	±300	+750	µA
Pulse Width Low (CLK)		IV	30			ns
Pulse Width High (CLK)		IV	30		300	ns
Digital Outputs						
Logic "1" Voltage	50 Ω to -2 V	VI	-1.1	-0.8		V
Logic "0" Voltage	50 Ω to -2 V	VI		-1.8	-1.5	V
Power Supply Requirements						
Voltages V_{CC}		IV	+4.75		+5.25	V
$-V_{EE}$		IV	-4.95		-5.45	V
Currents I_{CC}		VI		150	190	mA
$-I_{EE}$		VI		125	160	mA
Power Dissipation	Outputs Open	VI		1.4	1.8	W
Power Supply Rejection Ratio	(5 V±0.25 V, -5.2 V ±0.25 V)	V		1.0		LSB

[1] Typical thermal impedances (unsoldered, in free air): 32L sidebrazed DIP. θ_{ja} = 50 °C/W.
[2] 64 distortion BINS from 4096 pt FFT.
[3] fin = 1 MHz.
[4] fin = 3.58 and 4.35 MHz.

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests; therefore, $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

Figure 1A: Timing Diagram

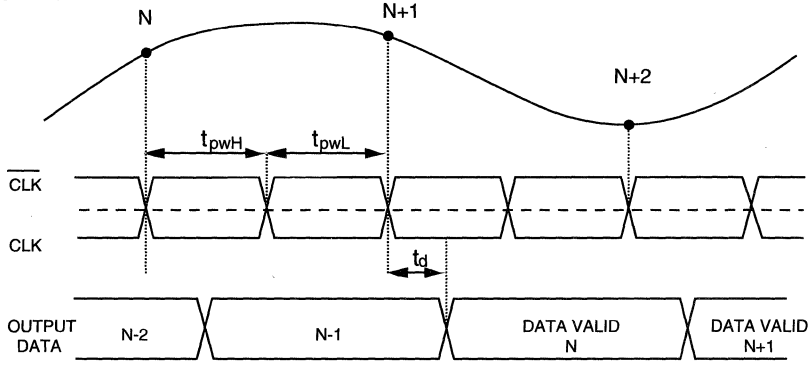

Figure 1B: Single Event Clock

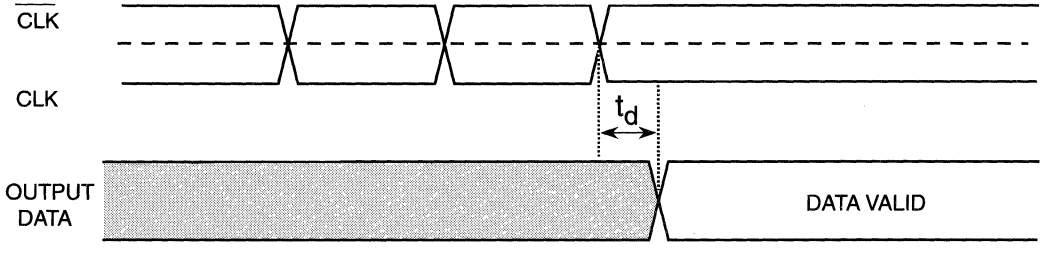

Table 1 - Timing Parameters

PARAMETERS	DESCRIPTION	MIN	TYP	MAX	UNITS
t_d	CLK to Data Valid Prop Delay	-	5		ns
t_{pwH}	CLK High Pulse Width	30	-	300	ns
t_{pwL}	CLK Low Pulse Width	30	-	-	ns

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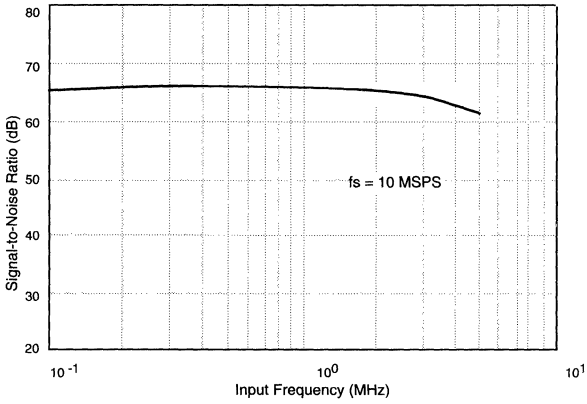
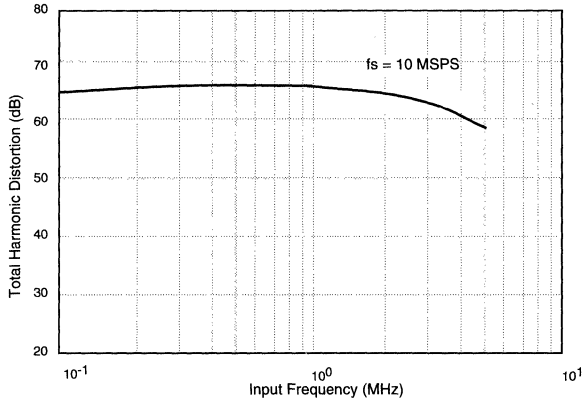
TYPICAL PERFORMANCE CHARACTERISTICS

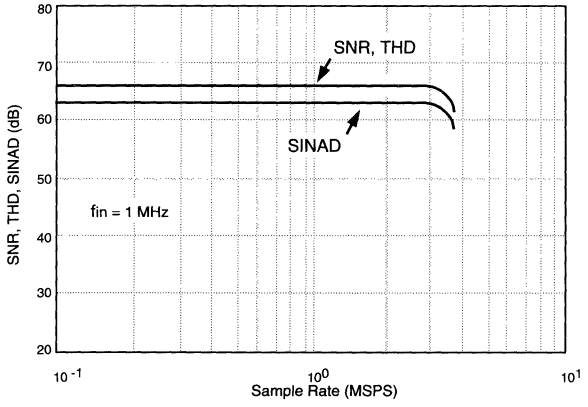
SNR vs Input Frequency



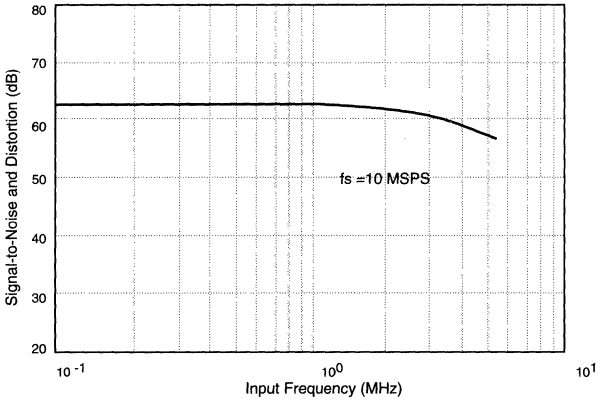
THD vs Input Frequency



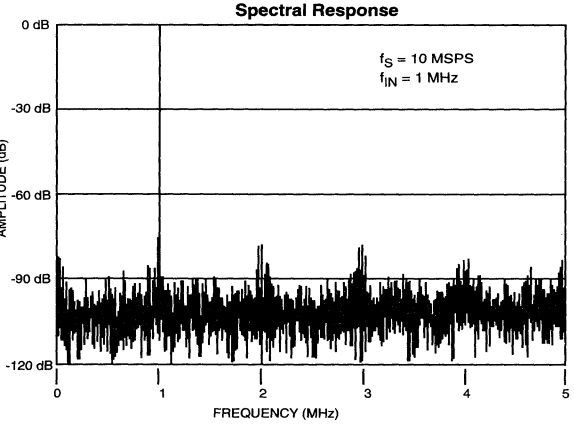
SNR, THD, SINAD vs Sample Rate



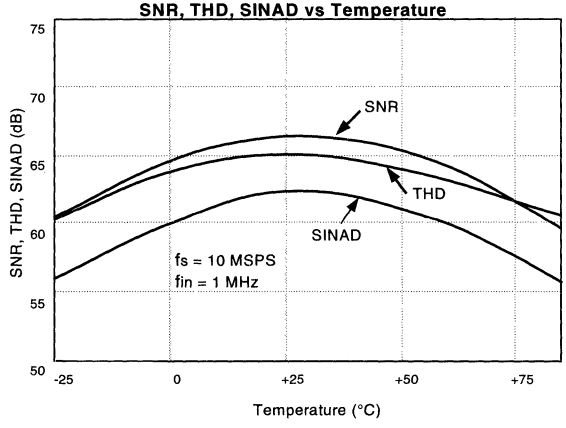
SINAD vs Input Frequency



Spectral Response



SNR, THD, SINAD vs Temperature



TYPICAL INTERFACE CIRCUIT

The SPT7910 requires few external components to achieve the stated operation and performance. Figure 2 shows the typical interface requirements when using the SPT7910 in normal circuit operation. The following section provides a description of the pin functions and outlines critical performance criteria to consider for achieving the optimal device performance.

POWER SUPPLIES AND GROUNDING

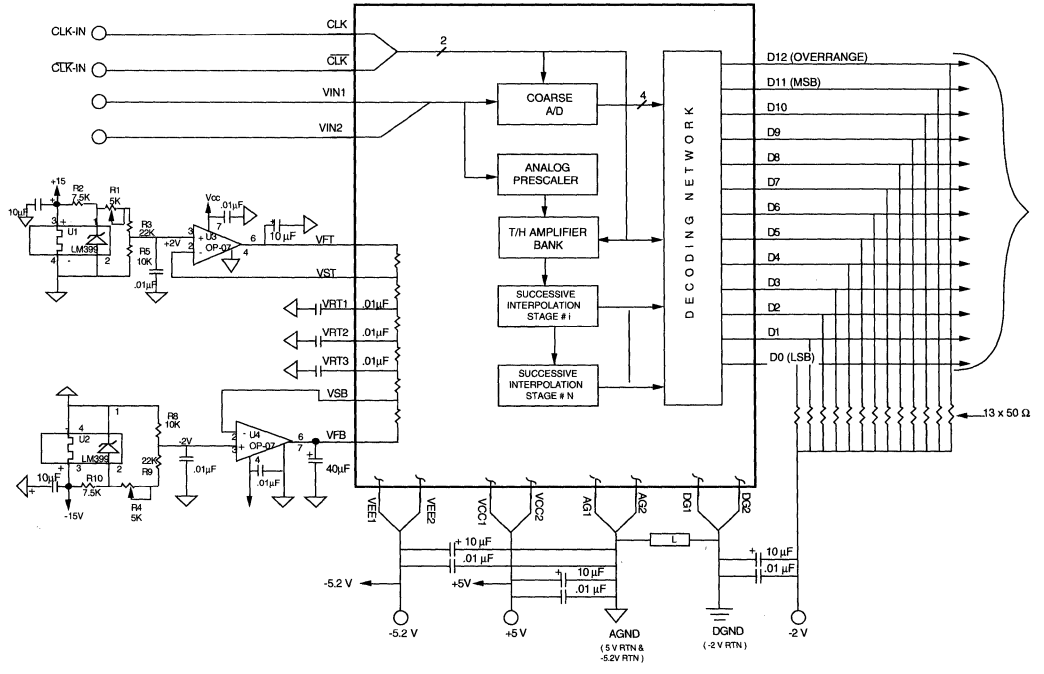
The SPT7910 requires the use of two supply voltages, V_{EE} and V_{CC}. Both supplies should be treated as analog supply sources. This means the V_{EE} and V_{CC} ground returns of the device should both be connected to the analog ground plane. All other -5.2 V requirements of the external digital logic circuit should be connected to the digital ground plane. Each power supply pin should be bypassed as closely as possible to the device with .01 µF and 10 µF capacitors as shown in figure 2.

The two grounds available on the SPT7910 are AGND and DGND. DGND is used only for ECL outputs and is to be referenced to the output pulldown voltage. These grounds are not tied together internal to the device. The use of ground planes is recommended to achieve the best performance of the SPT7910. The AGND and the DGND ground planes should be separated from each other and only connected together at the device through an inductance or ferrite bead. Doing this will minimize the ground noise pickup.

VOLTAGE REFERENCE

The SPT7910 requires the use of two voltage references: V_{FT} and V_{FB}. V_{FT} is the force for the top of the voltage reference ladder (+2.5 V typ), V_{FB} (-2.5 V typ) is the force for the bottom of the voltage reference ladder. Both voltages are applied across an internal reference ladder resistance of 800 ohms. In addition, there are five reference ladder taps (V_{ST},V_{RT1}, V_{RT2}, V_{RT3}, and V_{SB}). V_{ST} is the sense for the top of the reference ladder (+2.0 V), V_{RT2} is the midpoint of the ladder (0.0 V typ) and V_{SB} is the sense for the bottom of the reference ladder (-2.0 V). V_{RT1} and V_{RT3} are quarter point ladder taps (+1.0 and -1.0 V typical, respectively). The voltages seen at V_{ST} and V_{SB} are the true full scale input voltages of the device when V_{FT} and V_{FB} are driven to the recommended voltages (+2.5 V and -2.5 V typical respectively). V_{ST} and V_{SB} should be used to monitor the actual full scale input voltage of the device. V_{RT1}, V_{RT2} and V_{RT3} should not be driven to the expected ideal values as is commonly done with standard flash converters. When not being used, a decoupling capacitor of .01 uF connected to AGND from each tap is recommended to minimize high frequency noise injection.

Figure 2 - Typical Interface Circuit



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The analog input range will scale proportionally with respect to the reference voltage if a different input range is required. The maximum scaling factor for device operation is ± 20% of the recommended reference voltages of V_{FT} and V_{FB}. However, because the device is laser trimmed to optimize performance with V_{SB} and V_{ST} equal to -2.0 V and +2.0 V respectively, the accuracy of the device will degrade if operated beyond a ± 2% range.

The following errors are defined:

+FS error = top of ladder offset voltage = Δ(+FS -V_{ST})
-FS error = bottom of ladder offset voltage = Δ(-FS -V_{SB})

Where the +FS (full scale) input voltage is defined as the input approximately 1 LSB above the output transition of 1—10 and 1—11 and the -FS input voltage is defined as the input approximately 1 LSB below the output transition of 0—00 and 0—01.

An example of a typical reference driver circuit is shown in figure 2. This circuit is to be used to minimize the +FS and -FS errors over temperature. U1 and U2 are LM339s with an output voltage of +2 V and -2 V respectively. U3 and U4 are recommended to be OP-07s or equivalent. The input offset of these devices is 150 uV maximum. This circuit uses a true force and sense when driving the reference ladder of the SPT7910. U3 sources the current through V_{FT} (V_{ST} is a sense) while U4 is sinking current through V_{FB} (V_{SB} is a sense). To calibrate the reference, adjust R1 for V_{ST}=+2.0 V (V_{FT} will be typically +2.5 V) and adjust R4 for V_{SB}=-2.0 V (V_{FB} will be typically -2.5 V). This circuit is preferred because it allows the user to know exactly what the full scale input voltage is.

ANALOG INPUT

V_{IN1} and V_{IN2} are the analog inputs. Both inputs are tied to the same point internally. Either one may be used as an analog input "sense" and the other for an input "force." The inputs can also be tied together and driven from the same source. The full scale input range will be 80% of the reference voltage or ±2 volts with V_{FB}=-2.5 V and V_{FT}=+2.5 V.

The drive requirements for the analog inputs are minimal when compared to conventional Flash converters due the SPT7910's extremely low input capacitance of only 5 pF and very high input impedance of 300 kΩ. For example, for an input signal of ± 2 V p-p with an input frequency of 10 MHz, the peak output current required for the driving circuit is only 628 µA.

CLOCK INPUT

The clock inputs (CLK, $\overline{CLK}$) are designed to be driven differentially with ECL levels. Differential clock driving is highly recommended to minimize the effects of clock jitter. The clock may be driven single ended since $\overline{CLK}$ is internally biased to -1.3 V $\overline{CLK}$. may be left open, but a .01 µF bypass capacitor to AGND is recommended. As with all high speed circuits, proper terminations are required to avoid signal reflections and possible ringing that can cause the device to trigger at an unwanted time.

The clock input duty cycle should be 50% where possible, but performance will not be degraded if kept within the range of 40-60%. However, in any case the clock pulse width (tpwH) must be kept at 300 ns maximum to ensure proper operation of the internal track and hold amplifier (see timing diagram). The analog input signal is latched on the rising edge of the CLK.

DIGITAL OUTPUTS

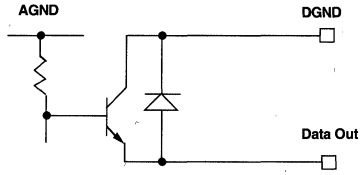
The format of the output data (D0-D11) is straight binary. (See table 2.) These outputs are ECL 10K and 10KH compatible with the output circuit shown in figure 3. The outputs are latched on the rising edge of CLK with a propagation delay of 5 ns. There is a one clock cycle latency between CLK and the valid output data (see timing diagram). These digital outputs can drive 50 ohms to ECL levels when pulled down to -2 V. Output loading pulled down to -5.2 V is not recommended. The total specified power dissipation of the device does not include the power used by these loads. The additional power used by these loads can vary between 10 and 300 mW typically (including the overrange load) depending on the output codes. If lower power levels are desired, the output loads can be reduced, but careful consideration to the resistive and capacitive loads in relation to the operating frequency must be considered.

Table 2 - Output Data Information

ANALOG INPUT	OVERRANGE D12	OUTPUT CODE D11-DO
>+2.0 V + 1/2 LSB	1	1111 1111 1111
+2.0 V -1 LSB	O	1111 1111 111Ø
0.0 V	O	ØØØØ ØØØØ ØØØØ
-2.0 V +1 LSB	O	OOOO OOOO OOOØ
<2.0 V	O	OOOO OOOO OOOO

(Ø indicates the flickering bit between logic 0 and 1).

Figure 3 - Output Circuit



OVERRANGE OUTPUT

The OVERRANGE OUTPUT (D12) is an indication that the analog input signal has exceeded the full scale input voltage by 1 LSB. When this condition occurs, the output will switch to logic 1. All other data outputs are unaffected by this operation. This feature makes it possible to include the SPT7910 into higher resolution systems.

EVALUATION BOARD

The EB7910 Evaluation Board is available to aid designers in demonstrating the full performance of the SPT7910. This board includes a reference circuit, clock driver circuit, output data latches and an on-board reconstruction of the digital data. An application note (AN7910) describing the operation of this board as well as information on the testing of the SPT7910 is also available. Contact the factory for price and availability.

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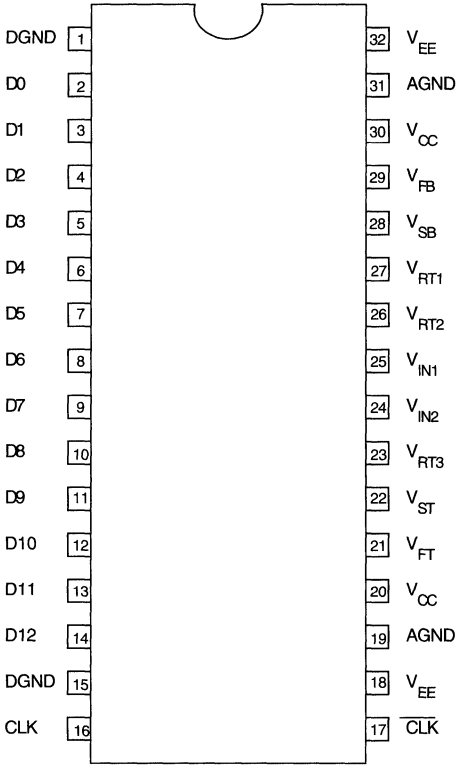
PIN ASSIGNMENTS



PIN FUNCTIONS

NAME	FUNCTION
DGND	Digital Ground
AGND	Analog Ground
D0-D11	ECL Outputs (D0=LSB)
D12	ECL Output Overrange
CLK	Clock
$\overline{CLK}$	Inverted Clock
V_{EE}	-5.2 V Supply
V_{CC}	+5.0 V supply
V_{RT1},V_{RT2},V_{RT3}	Voltage Reference Taps
V_{IN1}, V_{IN2}	Inputs (tied together at the die)
V_{FT}	Force for Top of Reference Ladder
V_{ST}	Sense for Top of Reference Ladder
V_{FB}	Force for Bottom of Reference Ladder
V_{SB}	Sense for Bottom of Reference Ladder

LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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SIGNAL PROCESSING TECHNOLOGIES

SPT7912

12-BIT, 30 MSPS, ECL, A/D CONVERTER

FEATURES

- Monolithic
- 12-Bit 30 MSPS Converter
- 65 dB SNR @ 1 MHz Input
- On-Chip Track/Hold
- Bipolar ±2.0 V Analog Input
- Low Power (1.4 W Typical)
- 5 pF Input Capacitance
- ECL Outputs

APPLICATIONS

- Radar Receivers
- Professional Video
- Instrumentation
- Medical Imaging
- Electronic Warfare
- Digital Communications
- Digital Spectrum Analyzers
- Electro-Optics

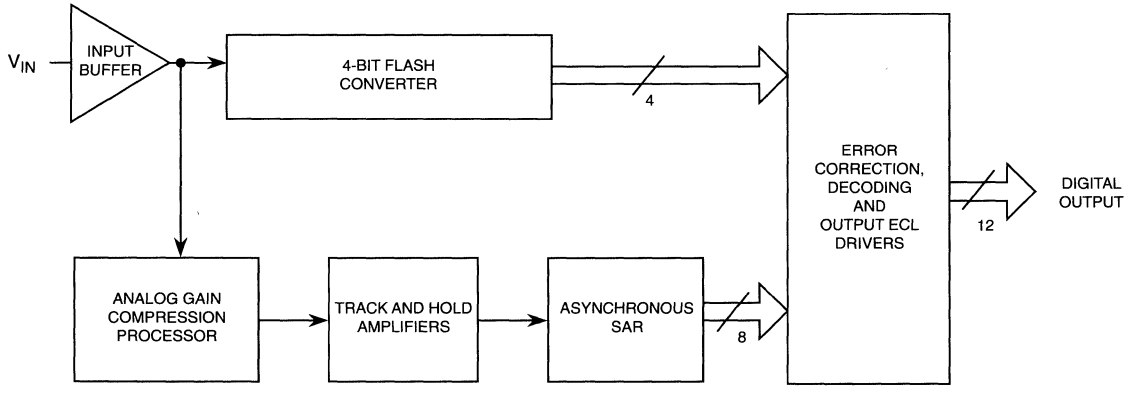
GENERAL DESCRIPTION

The SPT7912 A/D converter is industry's first 12-bit monolithic A-to-D converter capable of sample rates greater than 30 MSPS. On board input buffer and track/hold function assures excellent dynamic performance without the need for external components. Drive requirement problems are minimized with an input capacitance of only 5 pF.

Inputs and outputs are ECL to provide a higher level of noise immunity in high speed system applications. An overrange output signal is provided to indicate overflow conditions. Output data format is straight binary. Power dissipation is very low at only 1.4 watts with power supply voltages of +5.0 and -5.2 volts. The SPT7912 also provides a wide input voltage range of ±2.0 volts.

The SPT7912 is available in a small 32-lead ceramic side-brazed DIP package and in die form. A commercial temperature range of 0 to +70 °C is currently offered. Contact the factory for availability of surface mount packages, military temperature, and /883 processed units.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages
- V_{CC} ..... +6 V
- V_{EE} ..... -6 V

Input Voltages
- Analog Input ..... $V_{FB} \leq V_{IN} \leq V_{FT}$
- V_{FT}, V_{FB} ..... +3.0 V, -3.0 V
- Reference Ladder Current ..... 12 mA

Output
- Digital Outputs ..... 0 to -30 mA

Temperature
- Operating Temperature ..... 0 to 70 °C
- Junction Temperature ..... 175 °C
- Lead Temperature, (soldering 10 seconds) ..... 300 °C
- Storage Temperature ..... -65 to +150 °C

Note: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

$T_A=T_{MIN}$ to T_{MAX}, V_{CC}=+5.0 V, V_{EE}=-5.2 V, DV_{CC}=+5.0 V, V_{IN}=±2.0 V, V_{SB}=-2.0 V, V_{ST}=+2.0 V, f_{clock}=30 MHz, 50% clock duty cycle, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7912 MIN	SPT7912 TYP	SPT7912 MAX	UNITS
Resolution			12			Bits
DC Accuracy (+25 °C)						
Integral Nonlinearity	± Full Scale	I		±2.0		LSB
Differential Nonlinearity	250 kHz Sample Rate	I		±0.8		LSB
No Missing Codes		I		Guaranteed		
Analog Input						
Input Voltage Range		VI		±2.0		V
Input Bias Current		VI		30	60	µA
Input Resistance	V_{IN}=0 V	VI	100	300		kΩ
Input Capacitance		V		5		pF
Input Bandwidth	3 dB Small Signal	V		120		MHz
+FS Error		V		±5.0		LSB
-FS Error		V		±5.0		LSB
Reference Input						
Reference Ladder Resistance		VI	500	800		Ω
Reference Ladder Tempco		V		0.8		Ω/°C
Timing Characteristics						
Maximum Conversion Rate		VI	30	40		MHz
Overvoltage Recovery Time		V		20		ns
Pipeline Delay (Latency)		VI			1	Clock Cycle
Output Delay		V		5		ns
Aperture Delay Time		V		1		ns
Aperture Jitter Time		V		5		ps-RMS
Dynamic Performance						
Effective Number of Bits						
fin=500 kHz				10.0		Bits
fin=1.0 MHz				9.8		Bits
fin=3.58 MHz				9.5		Bits

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ELECTRICAL SPECIFICATIONS

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PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7912 MIN	SPT7912 TYP	SPT7912 MAX	UNITS
Dynamic Performance						
Signal-To-Noise Ratio (without Harmonics)						
fin=500 kHz	+25 °C	I	63	66		dB
	T_{MIN} to T_{MAX}	IV	58	61		dB
fin=1 MHz	+25 °C	I	63	65		dB
	T_{MIN} to T_{MAX}	IV	58	60		dB
fin=3.58 MHz	+25 °C	I	62	64		dB
	T_{MIN} to T_{MAX}	IV	58	60		dB
Harmonic Distortion[2]						
fin=500 kHz	+25 °C	I	63	65		dB
	T_{MIN} to T_{MAX}	IV	59	61		dB
fin=1.0 MHz	+25 °C	I	62	64		dB
	T_{MIN} to T_{MAX}	IV	58	60		dB
fin=3.58 MHz	+25 °C	I	59	61		dB
	T_{MIN} to T_{MAX}	IV	57	59		dB
Signal-to-Noise and Distortion						
fin=500 kHz	+25 °C	I	60	62		dB
	T_{MIN} to T_{MAX}	IV	55	58		dB
fin=1.0 MHz	+25 °C	I	59	61		dB
	T_{MIN} to T_{MAX}	IV	55	57		dB
fin=3.58 MHz	+25 °C	I	57	59		dB
	T_{MIN} to T_{MAX}	IV	54	56		dB
Spurious Free Dynamic Range[3]	+25 °C	V		74		dB
Differential Phase[4]	+25 °C	V		0.2		Degree
Differential Gain[4]	+25 °C	V		0.7		%
Digital Inputs						
Logic "1" Voltage		V	-1.1			V
Logic "0" Voltage		V			-1.5	V
Maximum Input Current Low		VI	-500	±200	+750	µA
Maximum Input Current High		VI	-500	±300	+750	µA
Pulse Width Low (CLK)		IV	15			ns
Pulse Width High (CLK)		IV	15		300	ns
Digital Outputs						
Logic "1" Voltage	50 Ω to -2 V	VI	-1.1	-0.8		V
Logic "0" Voltage	50 Ω to -2 V	VI		-1.8	-1.55	V
Power Supply Requirements						
Voltages V_{CC}		IV	+4.75		+5.25	V
$-V_{EE}$		IV	-4.95		-5.45	V
Currents I_{CC}		VI		150	190	mA
$-I_{EE}$		VI		125	160	mA
Power Dissipation	Outputs Open	VI		1.4	1.8	W
Power Supply Rejection Ratio	(5 V±0.25 V, -5.2 V ±0.25 V)	V		1.0		LSB

[1] Typical thermal impedances (unsoldered, in free air): 32L sidebrazed DIP. θ_{ja} = 50 °C/W.
[2] 64 distortion BINS from 4096 pt FFT.
[3] fin = 1 MHz.
[4] fin = 3.58 and 4.35 MHz.

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests; therefore, $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

Figure 1A: Timing Diagram

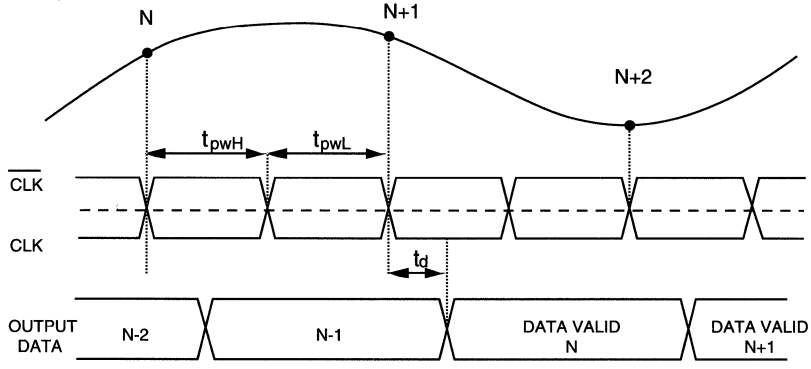

Figure 1B: Single Event Clock

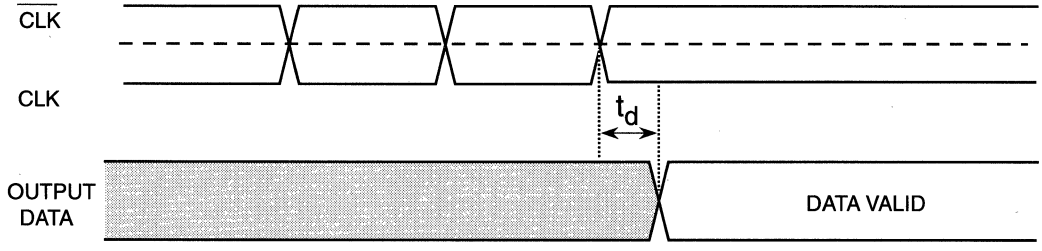

Table 1 - Timing Parameters

DESCRIPTION	PARAMETERS	MIN	TYP	MAX	UNITS
CLK to Data Valid Prop Delay	t_d	-	5		ns
CLK High Pulse Width	t_{pwH}	15	-	300	ns
CLK Low Pulse Width	t_{pwL}	15	-	-	ns

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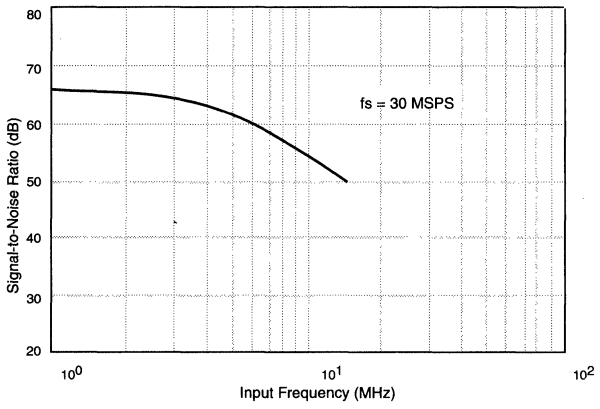
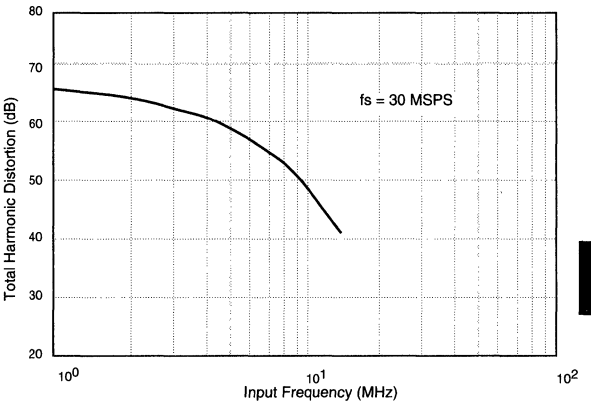
TYPICAL PERFORMANCE CHARACTERISTICS

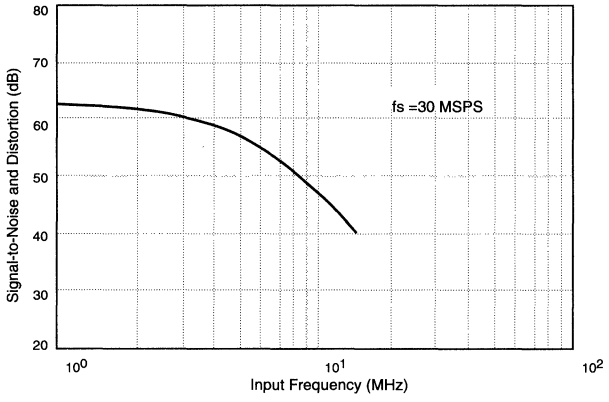
SNR vs Input Frequency



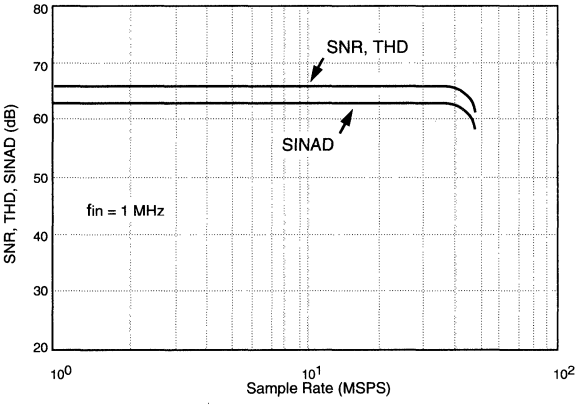
THD vs Input Frequency



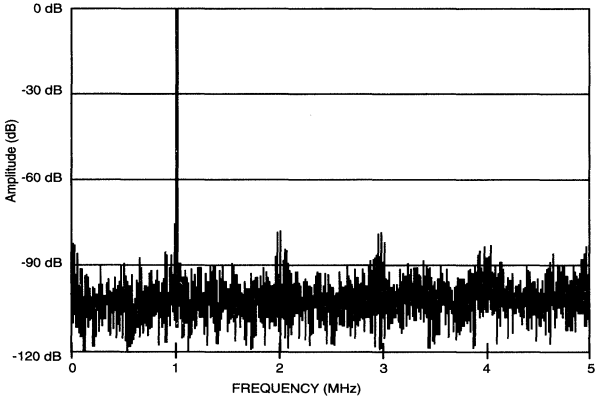
SINAD vs Input Frequency



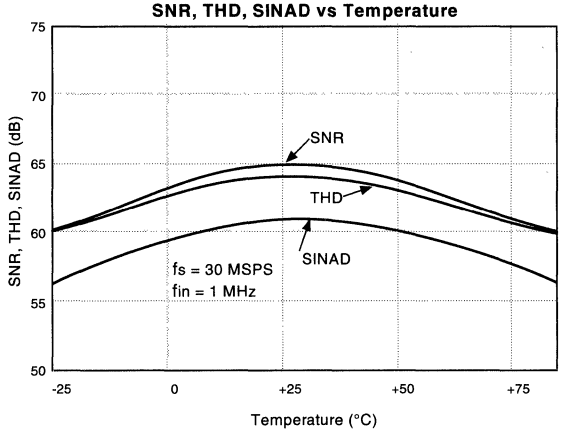
SNR, THD, SINAD vs Sample Rate



Spectral Response



SNR, THD, SINAD vs Temperature



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POWER SUPPLIES AND GROUNDING

The SPT7912 requires the use of two supply voltages, V_{EE} and V_{CC}. Both supplies should be treated as analog supply sources. This means the V_{EE} and V_{CC} ground returns of the device should both be connected to the analog ground plane. All other -5.2 V requirements of the external digital logic circuit should be connected to the digital ground plane. Each power supply pin should be bypassed as closely as possible to the device with .01 µF and 10 µF capacitors as shown in figure 2.

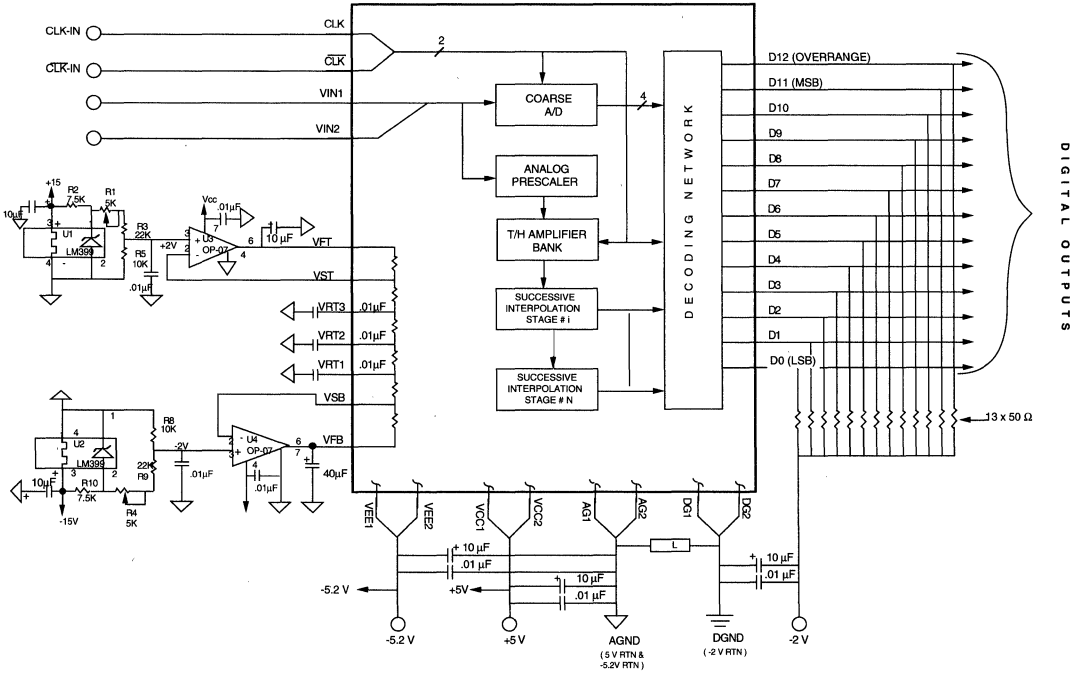
The two grounds available on the SPT7912 are AGND and DGND. DGND is used only for ECL outputs and is to be referenced to the output pulldown voltage. These grounds are not tied together internal to the device. The use of ground planes is recommended to achieve the best performance of the SPT7912. The AGND and the DGND ground planes should be separated from each other and only connected together at the device through an inductance or ferrite bead. Doing this will minimize the ground noise pickup.

VOLTAGE REFERENCE

The SPT7912 requires the use of two voltage references: V_{FT} and V_{FB}. V_{FT} is the force for the top of the voltage reference ladder (+2.5 V typ), V_{FB} (-2.5 V typ) is the force for the bottom of the voltage reference ladder. Both voltages are applied across an internal reference ladder resistance of 800 ohms. In addition, there are five reference ladder taps (V_{ST},V_{RT1}, V_{RT2}, V_{RT3}, and V_{SB}). V_{ST} is the sense for the top of the reference ladder (+2.0 V), V_{RT2} is the midpoint of the ladder (0.0 V typ) and V_{SB} is the sense for the bottom of the reference ladder (-2.0 V). V_{RT1} and V_{RT3} are quarter point ladder taps (+1.0 and -1.0 V typical, respectively). The voltages seen at V_{ST} and V_{SB} are the true full scale input voltages of the device when V_{FT} and V_{FB} are driven to the recommended voltages (+2.5 V and -2.5 V typical respectively). V_{ST} and V_{SB} should be used to monitor the actual full scale input voltage of the device. V_{RT1}, V_{RT2} and V_{RT3} should not be driven to the expected ideal values as is commonly done with standard flash converters. When not being used, a decoupling capacitor of .01 uF connected to AGND from each tap is recommended to minimize high frequency noise injection.

The analog input range will scale proportionally with respect to the reference voltage if a different input range is required.

Figure 2 - Typical Interface Circuit



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The maximum scaling factor for device operation is ± 20% of the recommended reference voltages of V_{FT} and V_{FB}. However, because the device is laser trimmed to optimize performance with V_{SB} and V_{ST} equal to -2.0 V and +2.0 V respectively, the accuracy of the device will degrade if operated beyond a ± 2% range.

The following errors are defined:

+FS error = top of ladder offset voltage = Δ(+FS -V_{ST})
-FS error = bottom of ladder offset voltage = Δ(-FS -V_{SB})

Where the +FS (full scale) input voltage is defined as the input approximately 1 LSB above the output transition of 1—10 and 1—11 and the -FS input voltage is defined as the input approximately 1 LSB below the output transition of 0—00 and 0—01.

An example of a typical reference driver circuit is shown in figure 2. This circuit is to be used to minimize the +FS and -FS errors over temperature. U1 and U2 are LM339s with an output voltage of +2 V and -2 V respectively. U3 and U4 are recommended to be OP-07s or equivalent. The input offset of these devices is 150 uV maximum. This circuit uses a true force and sense when driving the reference ladder of the SPT7912. U3 sources the current through V_{FT} (V_{ST} is a sense) while U4 is sinking current through V_{FB} (V_{SB} is a sense). To calibrate the reference, adjust R1 for V_{ST}=+2.0 V (V_{FT} will be typically +2.5 V) and adjust R4 for V_{SB}=-2.0 V (V_{FB} will be typically -2.5 V). This circuit is preferred because it allows the user to know exactly what the full scale input voltage is.

ANALOG INPUT

V_{IN1} and V_{IN2} are the analog inputs. Both inputs are tied to the same point internally. Either one may be used as an analog input "sense" and the other for an input "force." The inputs can also be tied together and driven from the same source. The full scale input range will be 80% of the reference voltage or ±2 volts with V_{FB}=-2.5 V and V_{FT}=+2.5 V.

The drive requirements for the analog inputs are minimal when compared to conventional Flash converters due the SPT7912's extremely low input capacitance of only 5 pF and very high input impedance of 300 kΩ. For example, for an input signal of ± 2 V p-p with an input frequency of 10 MHz, the peak output current required for the driving circuit is only 628 μA.

CLOCK INPUT

The clock inputs (CLK, $\overline{CLK}$) are designed to be driven differentially with ECL levels. Differential clock driving is highly recommended to minimize the effects of clock jitter. The clock may be driven single ended since $\overline{CLK}$ is internally biased to -1.3 V $\overline{CLK}$. may be left open, but a .01 μF bypass capacitor to AGND is recommended. As with all high speed circuits, proper terminations are required to avoid signal reflections and possible ringing that can cause the device to trigger at an unwanted time.

The clock input duty cycle should be 50% where possible, but performance will not be degraded if kept within the range of 40-60%. However, in any case the clock pulse width (tpwH) must be kept at 300 ns maximum to ensure proper operation of the internal track and hold amplifier (see timing diagram). The analog input signal is latched on the rising edge of the CLK.

DIGITAL OUTPUTS

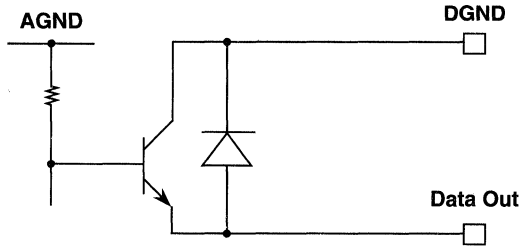
The format of the output data (D0-D11) is straight binary. (See table 2.) These outputs are ECL 10K and 10KH compatible with the output circuit shown in figure 3. The outputs are latched on the rising edge of CLK with a propagation delay of 5 ns. There is a one clock cycle latency between CLK and the valid output data (see timing diagram). These digital outputs can drive 50 ohms to ECL levels when pulled down to -2 V. Output loading pulled down to -5.2 V is not recommended. The total specified power dissipation of the device does not include the power used by these loads. The additional power used by these loads can vary between 10 and 300 mW typically (including the overrange load) depending on the output codes. If lower power levels are desired, the output loads can be reduced, but careful consideration to the resistive and capacitive loads in relation to the operating frequency must be considered.

Table 2 - Output Data Information

ANALOG INPUT	OVERRANGE D12	OUTPUT CODE D11-DO
>+2.0 V + 1/2 LSB	1	1111 1111 1111
+2.0 V -1 LSB	O	1111 1111 111Ø
0.0 V	O	ØØØØ ØØØØ ØØØØ
-2.0 V +1 LSB	O	OOOO OOOO OOOØ
<2.0 V	O	OOOO OOOO OOOO

(Ø indicates the flickering bit between logic 0 and 1).

Figure 3 - Output Circuit



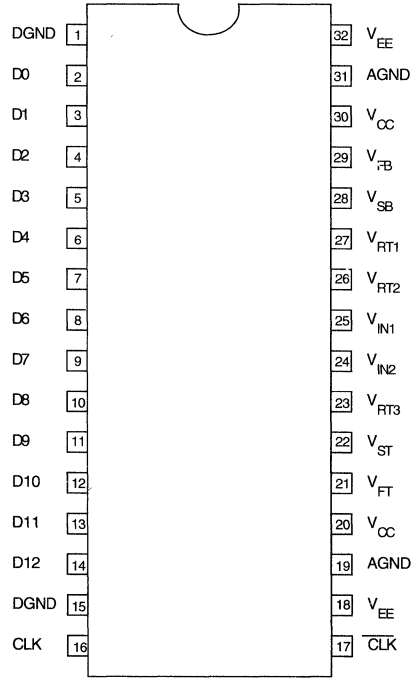
OVERRANGE OUTPUT

The OVERRANGE OUTPUT (D12) is an indication that the analog input signal has exceeded the full scale input voltage by 1 LSB. When this condition occurs, the output will switch to logic 1. All other data outputs are unaffected by this operation. This feature makes it possible to include the SPT7912 into higher resolution systems.

EVALUATION BOARD

The EB7912 Evaluation Board is available to aid designers in demonstrating the full performance of the SPT7912. This board includes a reference circuit, clock driver circuit, output data latches and an on-board reconstruction of the digital data. An application note (AN7912) describing the operation of this board as well as information on the testing of the SPT7912 is also available. Contact the factory for price and availability.

PIN ASSIGNMENT



PIN FUNCTIONS

NAME	FUNCTION
DGND	Digital Ground
AGND	Analog Ground
D0-D11	ECL Outputs (D0=LSB)
D12	ECL Output Overrange
CLK	Clock
$\overline{CLK}$	Inverted Clock
V_{EE}	-5.2 V Supply
V_{CC}	+5.0 V supply
V_{RT1}, V_{RT2}, V_{RT3}	Voltage Reference Taps
V_{IN1}, V_{IN2}	Inputs (tied together at the die)
V_{FT}	Force for Top of Reference Ladder
V_{ST}	Sense for Top of Reference Ladder
V_{FB}	Force for Bottom of Reference Ladder
V_{SB}	Sense for Bottom of Reference Ladder

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SPT

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LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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SPT
SIGNAL PROCESSING TECHNOLOGIES

SPT7920

12-BIT, 10 MSPS, TTL, A/D CONVERTER

3

FEATURES

- Monolithic
- 12-Bit 10 MSPS Converter
- 66 dB SNR @ 1 MHz Input
- On-Chip Track/Hold
- Bipolar ±2.0 V Analog Input
- Low Power (1.1 W Typical)
- 5 pF Input Capacitance
- TTL Outputs

APPLICATIONS

- Radar Receivers
- Professional Video
- Instrumentation
- Medical Imaging
- Electronic Warfare
- Digital Communications
- Digital Spectrum Analyzers
- Electro-Optics

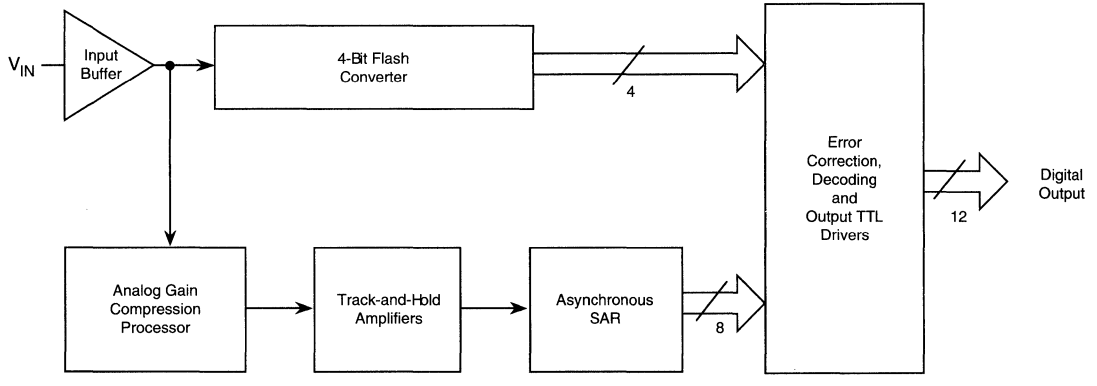
GENERAL DESCRIPTION

The SPT7920 A/D converter is the industry's first 12-bit monolithic A-to-D converter capable of sample rates greater than 10 MSPS. On board input buffer and track/hold function assures excellent dynamic performance without the need for external components. Drive requirement problems are minimized with an input capacitance of only 5 pF.

Logic inputs and outputs are TTL. An overrange output signal is provided to indicate overflow conditions. Output data format is straight binary. Power dissipation is very low at only 1.1 watts with power supply voltages of +5.0 and -5.2 volts. The SPT7920 also provides a wide input voltage range of ±2.0 volts.

The SPT7920 is available in a small 32-lead ceramic sidebrazed DIP package and a 44-lead surface-mount cerquad package. A commercial temperature range of 0 to +70 °C is currently offered. Consult the factory for military temperature availability.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages

V_{CC} ..... +6 V
V_{EE} ..... -6 V

Input Voltages

Analog Input ..... $V_{FB} \leq V_{IN} \leq V_{FT}$
V_{FT}, V_{FB} ..... +3.0 V, -3.0 V
Reference Ladder Current ..... 12 mA
CLK IN ..... V_{CC}

Output

Digital Outputs ..... 0 to -30 mA

Temperature

Operating Temperature ..... 0 to 70 °C
Junction Temperature ..... 175 °C
Lead Temperature, (soldering 10 seconds) ..... 300 °C
Storage Temperature ..... -65 to +150 °C

Note: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

$T_A=T_{MIN}$ to T_{MAX}, V_{CC}=+5.0 V, V_{EE}=-5.2 V, DV_{CC}=+5.0 V, V_{IN}=±2.0 V, V_{SB}=-2.0 V, V_{ST}=+2.0 V, f_{clock}=10 MHz, 50% clock duty cycle, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7920 MIN	SPT7920 TYP	SPT7920 MAX	UNITS
Resolution			12			Bits
DC Accuracy (+25 °C)						
Integral Nonlinearity	± Full Scale	IV		±2.0		LSB
Differential Nonlinearity	250 kHz Sample Rate	IV		±0.8		LSB
No Missing Codes		I		Guaranteed		
Analog Input						
Input Voltage Range		VI		±2.0		V
Input Bias Current	+25 °C	I		30	60	µA
Input Resistance	V_{IN}=0 V, +25 °C	I	100	300		kΩ
Input Capacitance		V		5		pF
Input Bandwidth	3 dB Small Signal	V		120		MHz
+FS Error		V		±5.0		LSB
-FS Error		V		±5.0		LSB
Reference Input						
Reference Ladder Resistance		VI	500	800		Ω
Reference Ladder Tempco		V		0.8		Ω/°C
Timing Characteristics						
Maximum Conversion Rate		VI	10			MHz
Overvoltage Recovery Time		V		20		ns
Pipeline Delay (Latency)		VI			1	Clock Cycle
Output Delay	T_A=+25 °C	V		14	18	ns
Aperture Delay Time	T_A=+25 °C	V		1		ns
Aperture Jitter Time	T_A=+25 °C	V		5		ps-RMS
Dynamic Performance						
Effective Number of Bits						
fin=500 kHz				10.2		Bits
fin=1.0 MHz				10.0		Bits
fin=3.58 MHz				9.5		Bits
Signal-To-Noise Ratio (without Harmonics)						
fin=500 kHz	+25 °C	I	64	67		dB
	T_{MIN} to T_{MAX}	IV	58	61		dB
fin=1 MHz	+25 °C	I	64	66		dB
	T_{MIN} to T_{MAX}	IV	58	60		dB
fin=3.58 MHz	+25 °C	I	62	64		dB
	T_{MIN} to T_{MAX}	IV	58	60		dB

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ELECTRICAL SPECIFICATIONS

T_A=T_{MIN} to T_{MAX}, V_{CC}=+5.0 V, V_{EE}=-5.2 V, DV_{CC}=+5.0 V, V_{IN}=±2.0 V, V_{SB}=-2.0 V, V_{ST}=+2.0 V, f_{clock}=10 MHz, 50% clock duty cycle, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7920 MIN	SPT7920 TYP	SPT7920 MAX	UNITS
Dynamic Performance						
Harmonic Distortion						
fin=500 kHz	+25 °C	I	63	66		dB
	T_{MIN} to T_{MAX}	IV	59	62		dB
fin=1.0 MHz	+25 °C	I	63	65		dB
	T_{MIN} to T_{MAX}	IV	59	61		dB
fin=3.58 MHz	+25 °C	I	59	61		dB
	T_{MIN} to T_{MAX}	IV	57	59		dB
Signal-to-Noise and Distortion						
fin=500 kHz	+25 °C	I	60	63		dB
	T_{MIN} to T_{MAX}	IV	55	58		dB
fin=1.0 MHz	+25 °C	I	60	62		dB
	T_{MIN} to T_{MAX}	IV	55	57		dB
fin=3.58 MHz	+25 °C	I	57	59		dB
	T_{MIN} to T_{MAX}	IV	54	56		dB
Spurious Free Dynamic Range[2]	+25 °C	V		74		dB
Differential Phase[3]	+25 °C	V		0.2		Degree
Differential Gain[3]	+25 °C	V		0.7		%
Digital Inputs						
Logic "1" Voltage		V	2.4		4.0	V
Logic "0" Voltage		V			0.8	V
Maximum Input Current Low	+25 °C	I	0	+5	+20	µA
Maximum Input Current High	+25 °C	I	0	+5	+20	µA
Pulse Width Low (CLK)		IV	30			ns
Pulse Width High (CLK)		IV	30		300	ns
Digital Outputs						
Logic "1" Voltage	+25 °C	I	2.4			V
Logic "0" Voltage	+25 °C	I			0.6	V
Power Supply Requirements						
Voltages V_{CC}		IV	4.75	5.0	5.25	V
DV_{CC}		IV	4.75	5.0	5.25	V
$-V_{EE}$		IV	-4.95	-5.2	-5.45	V
Currents I_{CC}	+25 °C	I		135	150	mA
DI_{CC}		IV		40	55	mA
$-I_{EE}$	+25 °C	I		45	70	mA
Power Dissipation		VI		1.1	1.3	W
Power Supply Rejection	(5 V ±0.25 V, -5.2 ±0.25 V)	V		1.0		LSB

1 Typical thermal impedances (unsoldered, in free air):
32L sidebrazed DIP:
θ_{ja} = 50 °C/W
44L cerquad:
θ_{ja} = 78 °C/W
θ_{ja} at 1 M/s airflow = 58 °C/W
θ_{jc} = 3.3 °C/W

2 fin = 1 MHz.

3 fin = 3.58 and 4.35 MHz.

Figure 1A: Timing Diagram

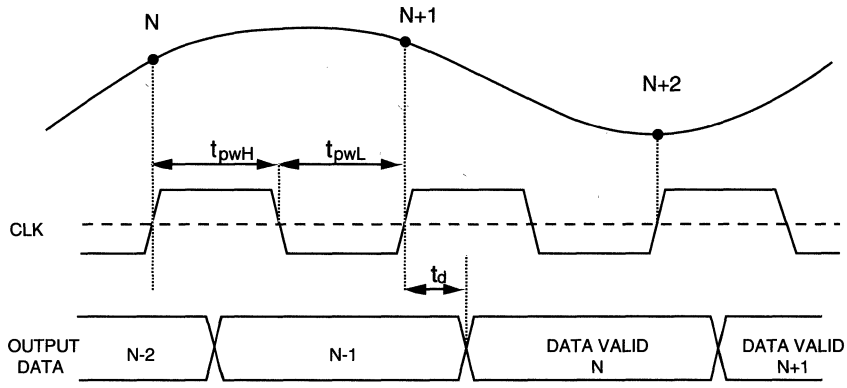

Figure 1B: Single Event Clock

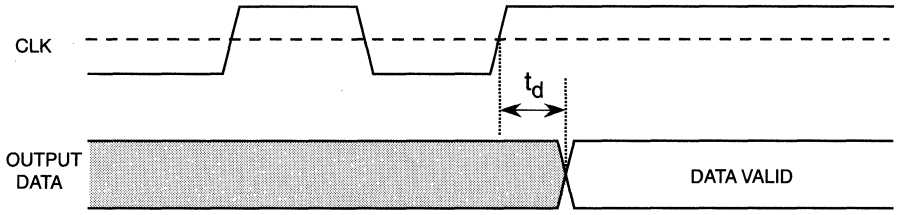

Table 1 - Timing Parameters

PARAMETERS	DESCRIPTION	MIN	TYP	MAX	UNITS
t_d	CLK to Data Valid Prop Delay	-	14	18	ns
t_{pwH}	CLK High Pulse Width	30	-	300	ns
t_{pwL}	CLK Low Pulse Width	30	-	-	ns

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests; therefore, $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

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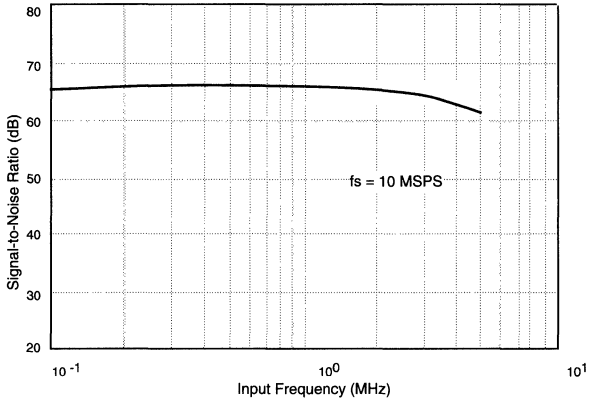
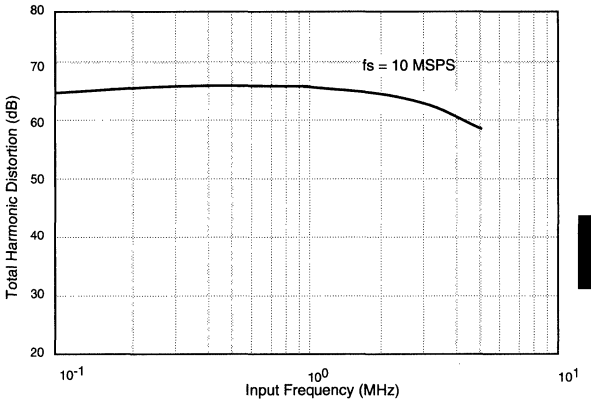
PERFORMANCE CHARACTERISTICS

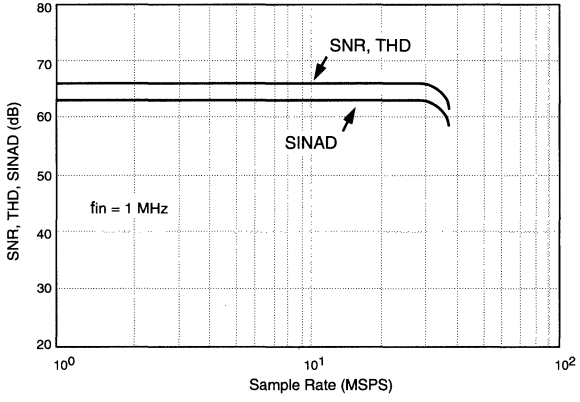
SNR vs Input Frequency



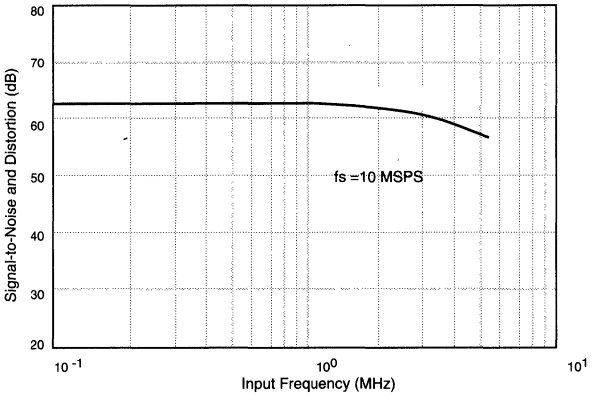
THD vs Input Frequency



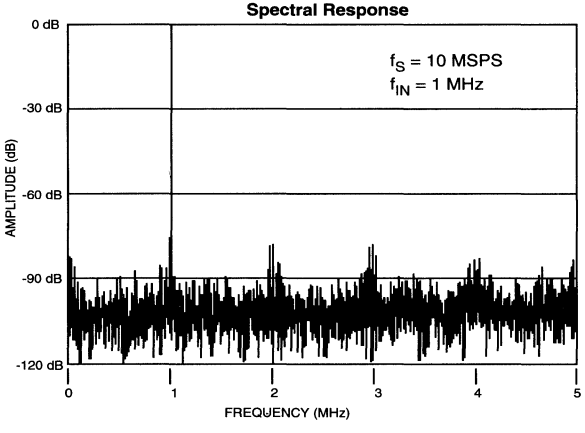
SNR, THD, SINAD vs Sample Rate



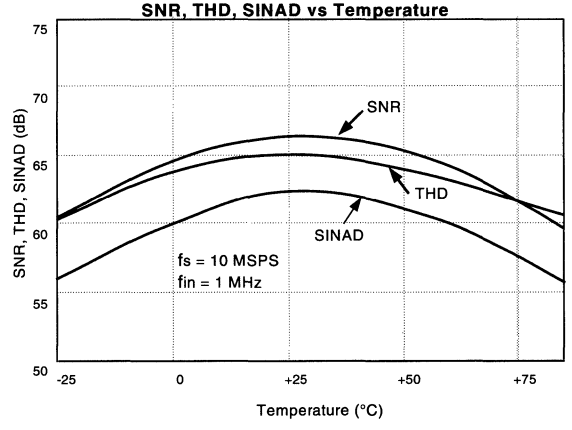
SINAD vs Input Frequency



SPT7920
Spectral Response



SNR, THD, SINAD vs Temperature



TYPICAL INTERFACE CIRCUIT

The SPT7920 requires few external components to achieve the stated operation and performance. Figure 2 shows the typical interface requirements when using the SPT7920 in normal circuit operation. The following section provides a description of the pin functions and outlines critical performance criteria to consider for achieving the optimal device performance.

POWER SUPPLIES AND GROUNDING

The SPT7920 requires -5.2 V and +5 V analog supply voltages. The +5 V supply is common to analog V_{CC} and digital DV_{CC}. A ferrite bead in series with each supply line is intended to reduce the transient noise injected into the analog V_{CC}. These beads should be connected as closely as possible to the device. The connection between the beads and the SPT7920 should not be shared with any other device. Each power supply pin should be bypassed as closely as possible to the device. Use 0.1 µF for V_{EE} and V_{CC}, and 0.01 µF for DV_{CC} (chip caps are preferred).

AGND and DGND are the two grounds available on the SPT7920. These two internal grounds are isolated on the device. The use of ground planes is recommended to achieve optimum device performance. DGND is needed for the DV_{CC} return path (40 mA typical) and for the return path for all digital output logic interfaces. AGND and DGND should be separated from each other and connected together only at the device through a ferrite bead.

A Schottky or hot carrier diode connected between AGND and V_{EE} is required. The use of separate power supplies between V_{CC} and DV_{CC} is not recommended due to potential power supply sequencing latch-up conditions. Using the recommended interface circuit shown in figure 2 will provide optimum device performance for the SPT7920.

VOLTAGE REFERENCE

The SPT7920 requires the use of two voltage references: V_{FT} and V_{FB}. V_{FT} is the force for the top of the voltage reference ladder (+2.5 V typ), V_{FB} (-2.5 V typ) is the force for the bottom of the voltage reference ladder. Both voltages are applied across an internal reference ladder resistance of 800 ohms. The +2.5 V voltage source for reference V_{FT} must be current limited to 20 mA maximum if a different driving circuit is used in place of the recommended reference circuit shown in figures 2 and 3. In addition, there are five reference ladder taps (V_{ST}, V_{RT1}, V_{RT2}, V_{RT3}, and V_{SB}). V_{ST} is the sense for the top of the reference ladder (+2.0 V), V_{RT2} is the midpoint of the ladder (0.0 V typ) and V_{SB} is the sense for the bottom of the reference ladder (-2.0 V). V_{RT1} and V_{RT3} are quarter point ladder taps (+1.0 and -1.0 V typical, respectively). The voltages seen at V_{ST} and V_{SB} are the true full scale input voltages of the device when V_{FT} and V_{FB} are driven to the recommended voltages (+2.5 V and -2.5 V typical respectively). V_{ST} and V_{SB} should be used to monitor the actual full scale input voltage of the device. V_{RT1}, V_{RT2} and V_{RT3} should not be driven to the expected ideal values as is commonly done with standard flash converters. When not being used, a decoupling capacitor of .01 µF connected to AGND from each tap is recommended to minimize high frequency noise injection.

Figure 2 - Typical Interface Circuit

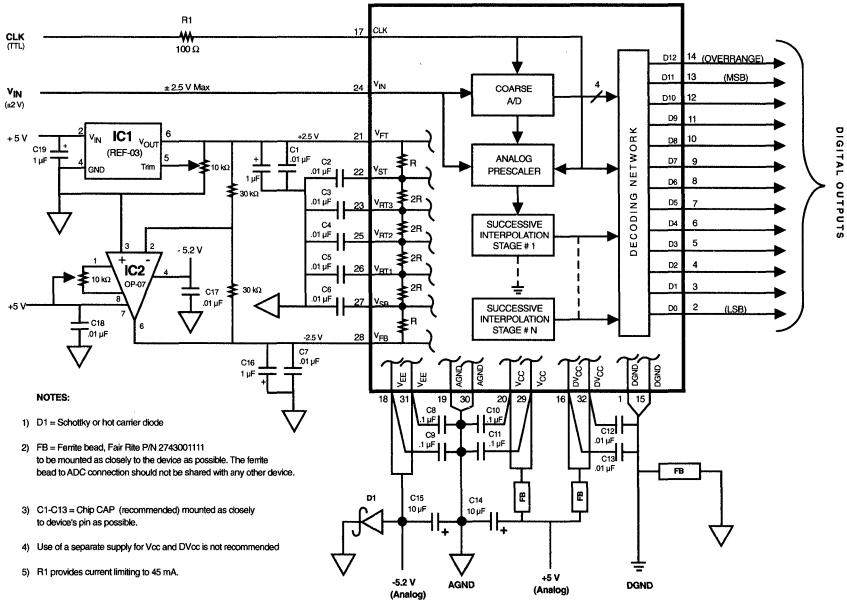


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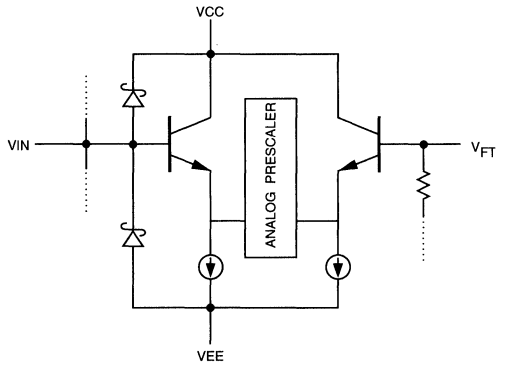
Figure 3 - Analog Equivalent Input Circuit



The analog input range will scale proportionally with respect to the reference voltage if a different input range is required. The maximum scaling factor for device operation is ± 20% of the recommended reference voltages of V_{FT} and V_{FB}. However, because the device is laser trimmed to optimize performance with ± 2.5 V references, the accuracy of the device will degrade if operated beyond a ± 2% range.

An example of a recommended reference driver circuit is shown in figure 2. IC1 is REF-03, the +2.5 V reference with a tolerance of 0.6% or +/- 0.015 V. The potentiometer R1 is 10 kΩ and supports a minimum adjustable range of up to 150 mV. IC2 is recommended to be an OP-07 or equivalent device. R2 and R3 must be matched to within 0.1% with good TC tracking to maintain a 0.3 LSB matching between V_{FT} and V_{FB}. If 0.1% matching is not met, then potentiometer R4 can be used to adjust the V_{FB} voltage to the desired level. R1 and R4 should be adjusted such that V_{ST} and V_{SB} are exactly +2.0 V and -2.0 V respectively.

The following errors are defined:
+FS error = top of ladder offset voltage = Δ(+FS -V_{ST})
-FS error = bottom of ladder offset voltage = Δ(-FS -V_{SB})

Where the +FS (full scale) input voltage is defined as the output 1 LSB above the transition of 1—10 and 1—11 and the -FS input voltage is defined as the output 1 LSB below the transition of 0—00 and 0—01.

ANALOG INPUT

V_{IN} is the analog input. The full scale input range will be 80% of the reference voltage or ±2 volts with V_{FB}=-2.5 V and V_{FT}=+2.5 V.

The drive requirements for the analog inputs are minimal when compared to conventional Flash converters due to the SPT7920's extremely low input capacitance of only 5 pF and very high input impedance of 300 kΩ. For example, for an input signal of ± 2 V p-p with an input frequency of 10 MHz, the peak output current required for the driving circuit is only 628 µA.

CLOCK INPUT

The SPT7920 is driven from a single-ended TTL input (CLK). For optimal noise performance, the clock input slew rate should be a minimum of 6 ns. Because of this, the use of *fast* logic is recommended. The clock input duty cycle should be 50% where possible, but performance will not be degraded if kept within the range of 40-60%. However, in any case the clock pulse width (tpwH) must be kept at 300 ns maximum to ensure proper operation of the internal track and hold amplifier (see timing diagram). The analog input signal is latched on the rising edge of the CLK.

The clock input must be driven from fast TTL logic ($V_{IH} \leq 4.5$ V, T_{RISE} <6 ns). In the event the clock is driven from a high current source, use a 100 Ω resistor in series to current limit to approximately 45 mA.

DIGITAL OUTPUTS

The format of the output data (D0-D11) is straight binary. (See table 2.) The outputs are latched on the rising edge of CLK with a propagation delay of 14 ns (typ). There is a one clock cycle latency between CLK and the valid output data. (See timing diagram.)

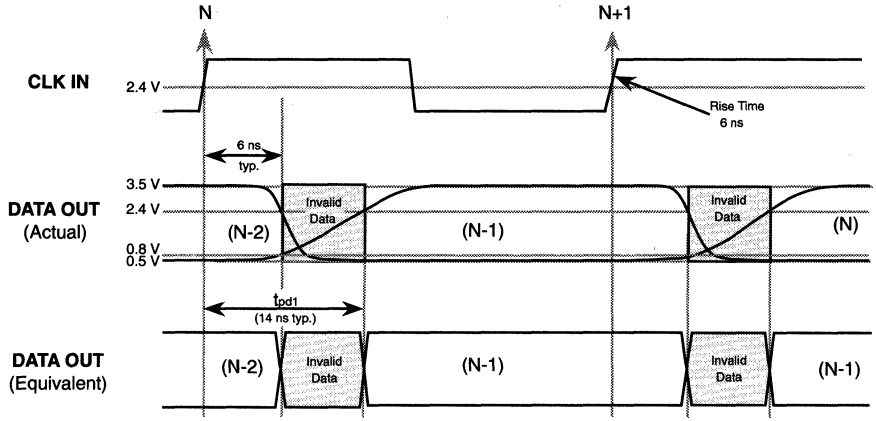
Table 2 - Output Data Information

ANALOG INPUT	OVERRANGE D12	OUTPUT CODE D11-DO
>+2.0 V + 1/2 LSB	1	1111 1111 1111
+2.0 V -1 LSB	O	1111 1111 111Ø
0.0 V	O	ØØØØ ØØØØ ØØØØ
-2.0 V +1 LSB	O	OOOO OOOO OOOØ
<2.0 V	O	OOOO OOOO OOOO

(Ø indicates the flickering bit between logic 0 and 1).

The rise times and fall times of the digital outputs are not symmetrical. The propagation delay of the rise time is typically 14 ns and the fall time is typically 6 ns. (See figure 4.) The nonsymmetrical rise and fall times create approximately 8 ns of invalid data.

Figure 4 - Digital Output Characteristics



OVERRANGE OUTPUT

The OVERRANGE OUTPUT (D12) is an indication that the analog input signal has exceeded the full scale input voltage by 1 LSB. When this condition occurs, the outputs will switch to logic 1s. All other data outputs are unaffected by this operation. This feature makes it possible to include the SPT7920 into higher resolution systems.

EVALUATION BOARD

The EB7920 evaluation board is available to aid designers in demonstrating the full performance of the SPT7920. This board includes a reference circuit, clock driver circuit, output data latches and an on-board reconstruction of the digital data. An application note (AN7920) describing the operation of this board as well as information on the testing of the SPT7920 is also available. Contact the factory for price and availability.

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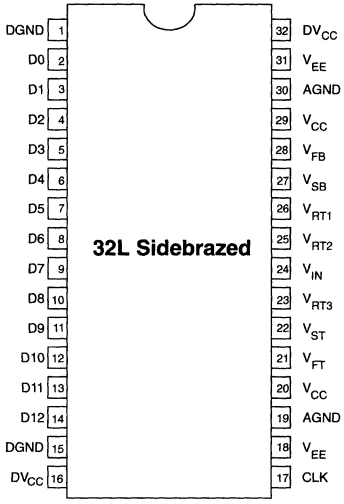
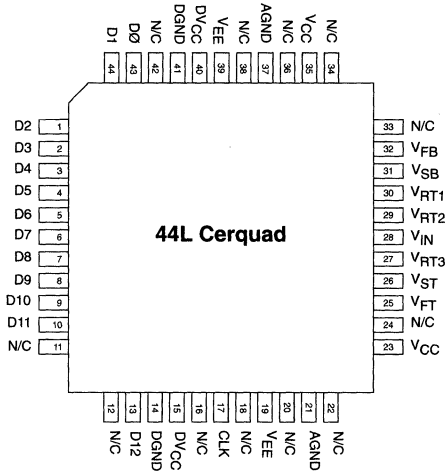
PIN ASSIGNMENTS





PIN FUNCTIONS

NAME	FUNCTION
DGND	Digital Ground
AGND	Analog Ground
D0-D11	TTL Outputs (D0=LSB)
D12	TTL Output Overrange
CLK	Clock Input
V_{EE}	-5.2 V Supply
V_{CC}	+5.0 V supply
V_{RT1}-V_{RT3}	Voltage Reference Taps
V_{IN}	Analog Input
DV_{CC}	Digital +5.0 V Supply (TTL Outputs)
V_{FT}	Force for Top of Reference Ladder
V_{ST}	Sense for Top of Reference Ladder
V_{FB}	Force for Bottom of Reference Ladder
V_{SB}	Sense for Bottom of Reference Ladder

LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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SIGNAL PROCESSING TECHNOLOGIES

SPT7921

12-BIT, 20 MSPS, TTL, A/D CONVERTER

3

FEATURES

- Monolithic
- 12-Bit 20 MSPS Converter
- 66 dB SNR @ 1 MHz Input
- On-Chip Track/Hold
- Bipolar ±2.0 V Analog Input
- Low Power (1.1 W Typical)
- 5 pF input Capacitance
- TTL Outputs

APPLICATIONS

- Radar Receivers
- Professional Video
- Instrumentation
- Medical Imaging
- Electronic Warfare
- Digital Communications
- Digital Spectrum Analyzers
- Electro-optics

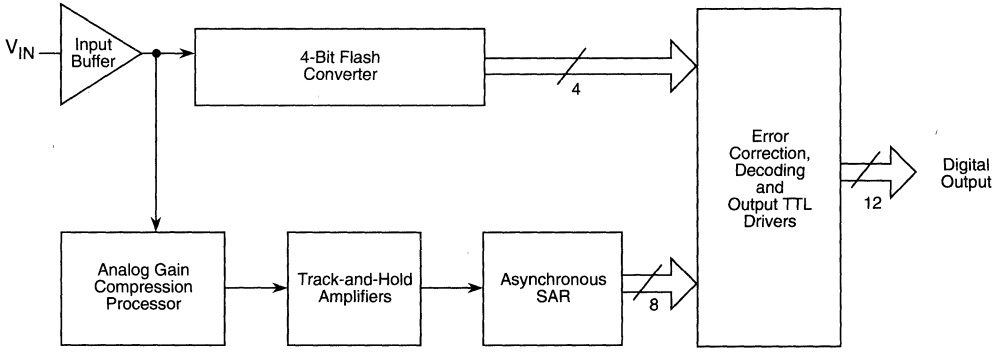
GENERAL DESCRIPTION

The SPT7921 A/D converter is the industry's first 12-bit monolithic A-to-D converter capable of sample rates greater than 20 MSPS. On board input buffer and track/hold function assures excellent dynamic performance without the need for external components. Drive requirement problems are minimized with an input capacitance of only 5 pF.

Logic inputs and outputs are TTL. An overrange output signal is provided to indicate overflow conditions. Output data format is straight binary. Power dissipation is very low at only 1.1 watts with power supply voltages of +5.0 and -5.2 volts. The SPT7921 also provides a wide input voltage range of ±2.0 volts.

The SPT7921 is available in a small 32-lead ceramic side-brazed DIP package and a 44-lead cerquad package for surface-mount applications. A commercial temperature range of 0 to +70 °C is currently offered. Consult the factory for military temperature availability.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages

V_{CC} ..... +6 V
V_{EE} ..... -6 V

Input Voltages

Analog Input ..... $V_{FB} \leq V_{IN} \leq V_{FT}$
V_{FT}, V_{FB} ..... +3.0 V, -3.0 V
Reference Ladder Current ..... 12 mA
CLK IN ..... V_{CC}

Output

Digital Outputs ..... 0 to -30 mA

Temperature

Operating Temperature ..... 0 to 70 °C
Junction Temperature ..... 175 °C
Lead Temperature, (soldering 10 seconds) ..... 300 °C
Storage Temperature ..... -65 to +150 °C

Note: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

$T_A=T_{MIN}$ to T_{MAX}, V_{CC}=+5.0 V, V_{EE}=-5.2 V, DV_{CC}=+5.0 V, V_{IN}=±2.0 V, V_{SB}=-2.0 V, V_{ST}=+2.0 V, f_{clock}=20 MHz, 50% clock duty cycle, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7921 MIN	SPT7921 TYP	SPT7921 MAX	UNITS
Resolution			12			Bits
DC Accuracy (+25 °C)						
Integral Nonlinearity	± Full Scale	IV		±2.0		LSB
Differential Nonlinearity	250 kHz Sample Rate	IV		±0.8		LSB
No Missing Codes		I		Guaranteed		
Analog Input						
Input Voltage Range		VI		±2.0		V
Input Bias Current	+25 °C	I		30	60	µA
Input Resistance	V_{IN}=0 V, +25 °C	I	100	300		kΩ
Input Capacitance		V		5		pF
Input Bandwidth	3 dB Small Signal	V		120		MHz
+FS Error		V		±5.0		LSB
-FS Error		V		±5.0		LSB
Reference Input						
Reference Ladder Resistance		VI	500	800		Ω
Reference Ladder Tempco		V		0.8		Ω/°C
Timing Characteristics						
Maximum Conversion Rate		VI	20			MHz
Overvoltage Recovery Time		V		20		ns
Pipeline Delay (Latency)		VI			1	Clock Cycle
Output Delay	T_A=+25 °C	V		14	18	ns
Aperture Delay Time	T_A=+25 °C	V		1		ns
Aperture Jitter Time	T_A=+25 °C	V		5		ps-RMS
Dynamic Performance						
Effective Number of Bits						
fin=500 kHz				10.2		Bits
fin=1.0 MHz				10.0		Bits
fin=3.58 MHz				9.5		Bits
Signal-To-Noise Ratio (without Harmonics)						
fin=500 kHz	+25 °C	I	64	67		dB
	T_{MIN} to T_{MAX}	IV	58	61		dB
fin=1 MHz	+25 °C	I	64	66		dB
	T_{MIN} to T_{MAX}	IV	58	60		dB
fin=3.58 MHz	+25 °C	I	62	64		dB
	T_{MIN} to T_{MAX}	IV	58	60		dB

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ELECTRICAL SPECIFICATIONS

T_A=T_{MIN} to T_{MAX}, V_{CC}=+5.0 V, V_{EE}=-5.2 V, DV_{CC}=+5.0 V, V_{IN}=±2.0 V, V_{SB}=-2.0 V, V_{ST}=+2.0 V, f_{clock}=20 MHz, 50% clock duty cycle, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7921 MIN	SPT7921 TYP	SPT7921 MAX	UNITS
Dynamic Performance						
Harmonic Distortion						
fin=500 kHz	+25 °C	I	63	66		dB
	T_{MIN} to T_{MAX}	IV	59	62		dB
fin=1.0 MHz	+25 °C	I	63	65		dB
	T_{MIN} to T_{MAX}	IV	59	61		dB
fin=3.58 MHz	+25 °C	I	59	61		dB
	T_{MIN} to T_{MAX}	IV	57	59		dB
Signal-to-Noise and Distortion						
fin=500 kHz	+25 °C	I	60	63		dB
	T_{MIN} to T_{MAX}	IV	55	58		dB
fin=1.0 MHz	+25 °C	I	60	62		dB
	T_{MIN} to T_{MAX}	IV	55	57		dB
fin=3.58 MHz	+25 °C	I	57	59		dB
	T_{MIN} to T_{MAX}	IV	54	56		dB
Spurious Free Dynamic Range[2]	+25 °C	V		74		dB
Differential Phase[3]	+25 °C	V		0.2		Degree
Differential Gain[3]	+25 °C	V		0.7		%
Digital Inputs						
Logic "1" Voltage		V	2.4		4.0	V
Logic "0" Voltage		V			0.8	V
Maximum Input Current Low	+25 °C	I	0	+5	+20	µA
Maximum Input Current High	+25 °C	I	0	+5	+20	µA
Pulse Width Low (CLK)		IV	20			ns
Pulse Width High (CLK)		IV	20		300	ns
Digital Outputs						
Logic "1" Voltage	+25 °C	I	2.4			V
Logic "0" Voltage	+25 °C	I			0.6	V
Power Supply Requirements						
Voltages V_{CC}		IV	4.75	5.0	5.25	V
DV_{CC}		IV	4.75	5.0	5.25	V
$-V_{EE}$		IV	-4.95	-5.2	-5.45	V
Currents I_{CC}	+25 °C	I		135	150	mA
DI_{CC}		IV		40	55	mA
$-I_{EE}$	+25 °C	I		45	70	mA
Power Dissipation		VI		1.1	1.3	W
Power Supply Rejection	(5 V ±0.25 V, -5.2 ±0.25 V)	V		1.0		LSB

[1] Typical thermal impedances (unsoldered, in free air):
32L sidebrazed DIP:
θ_{ja} = 50 °C/W
44L cerquad:
θ_{ja} = 78 °C/W
θ_{ja} at 1 M/s airflow = 58 °C/W
θ_{jc} = 3.3 °C/W

[2] fin = 1 MHz.

[3] fin = 3.58 and 4.35 MHz.

Figure 1A: Timing Diagram

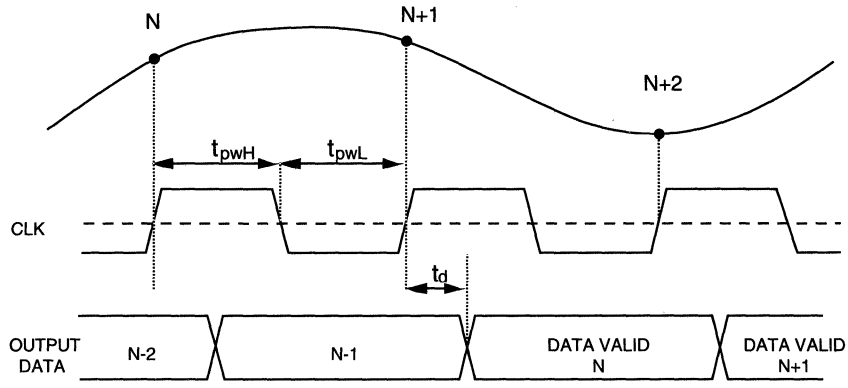

Figure 1B: Single Event Clock

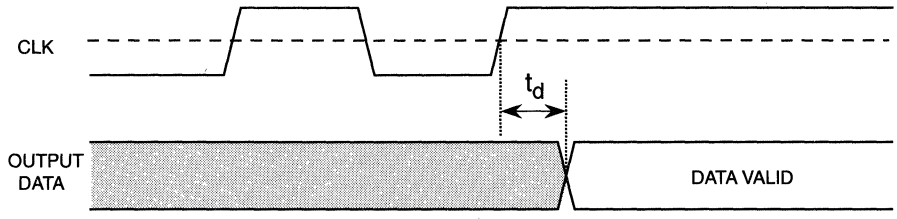

Table 1 - Timing Parameters

PARAMETERS	DESCRIPTION	MIN	TYP	MAX	UNITS
t_d	CLK to Data Valid Prop Delay	-	14	18	ns
t_{pwH}	CLK High Pulse Width	20	-	300	ns
t_{pwL}	CLK Low Pulse Width	20	-	-	ns

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests; therefore, $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

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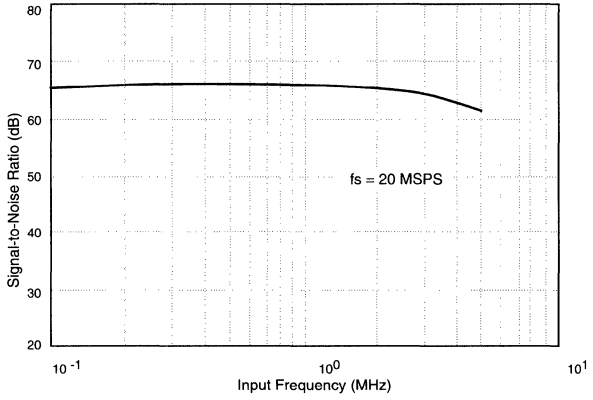
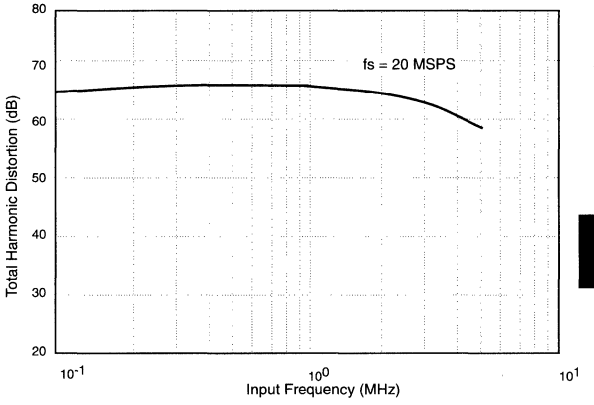
PERFORMANCE CHARACTERISTICS

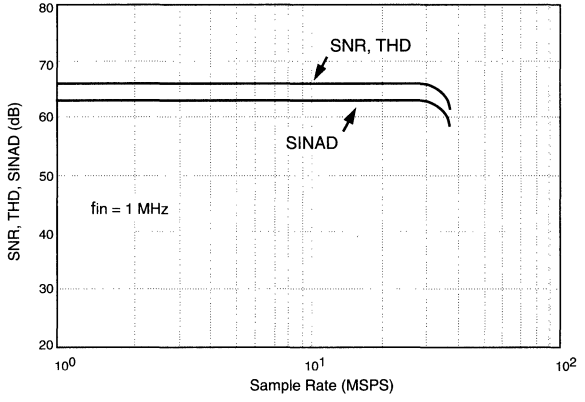
SNR vs Input Frequency



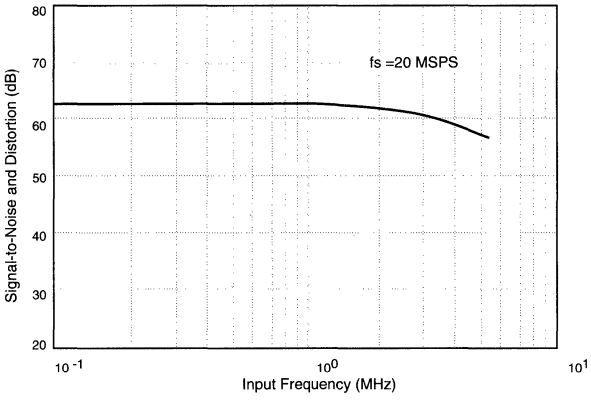
THD vs Input Frequency



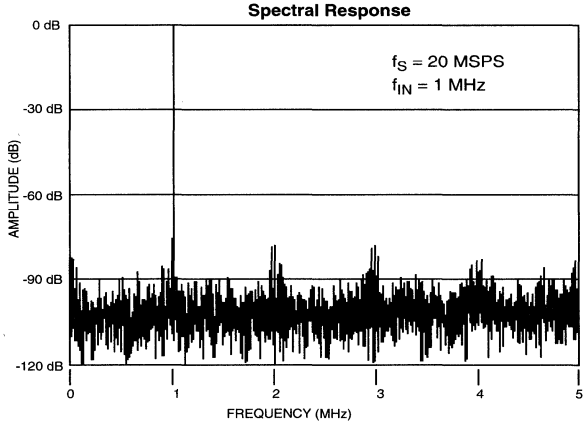
SNR, THD, SINAD vs Sample Rate



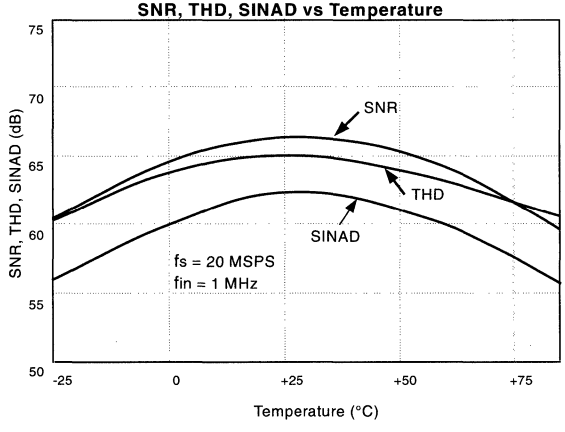
SINAD vs Input Frequency



SPT7921
Spectral Response



SNR, THD, SINAD vs Temperature



TYPICAL INTERFACE CIRCUIT

The SPT7921 requires few external components to achieve the stated operation and performance. Figure 2 shows the typical interface requirements when using the SPT7921 in normal circuit operation. The following section provides a description of the pin functions and outlines critical performance criteria to consider for achieving the optimal device performance.

POWER SUPPLIES AND GROUNDING

The SPT7921 requires -5.2 V and +5 V analog supply voltages. The +5 V supply is common to analog V_{CC} and digital DV_{CC}. A ferrite bead in series with each supply line is intended to reduce the transient noise injected into the analog V_{CC}. These beads should be connected as closely as possible to the device. The connection between the beads and the SPT7921 should not be shared with any other device. Each power supply pin should be bypassed as closely as possible to the device. Use 0.1 µF for V_{EE} and V_{CC}, and 0.01 µF for DV_{CC} (chip caps are preferred).

AGND and DGND are the two grounds available on the SPT7921. These two internal grounds are isolated on the device. The use of ground planes is recommended to achieve optimum device performance. DGND is needed for the DV_{CC} return path (40 mA typical) and for the return path for all digital output logic interfaces. AGND and DGND should be separated from each other and connected together only at the device through a ferrite bead.

A Schottky or hot carrier diode connected between AGND and V_{EE} is required. The use of separate power supplies between V_{CC} and DV_{CC} is not recommended due to potential power supply sequencing latch-up conditions. Using the recommended interface circuit shown in figure 2 will provide optimum device performance for the SPT7921.

VOLTAGE REFERENCE

The SPT7921 requires the use of two voltage references: V_{FT} and V_{FB}. V_{FT} is the force for the top of the voltage reference ladder (+2.5 V typ), V_{FB} (-2.5 V typ) is the force for the bottom of the voltage reference ladder. Both voltages are applied across an internal reference ladder resistance of 800 ohms. The +2.5 V voltage source for reference V_{FT} must be current limited to 20 mA maximum if a different driving circuit is used in place of the recommended reference circuit shown in figures 2 and 3. In addition, there are five reference ladder taps (VST, VRT1, V_{RT2}, V_{RT3}, and V_{SB}). V_{ST} is the sense for the top of the reference ladder (+2.0 V), V_{RT2} is the midpoint of the ladder (0.0 V typ) and V_{SB} is the sense for the bottom of the reference ladder (-2.0 V). V_{RT1} and V_{RT3} are quarter point ladder taps (+1.0 and -1.0 V typical, respectively). The voltages seen at V_{ST} and V_{SB} are the true full scale input voltages of the device when V_{FT} and V_{FB} are driven to the recommended voltages (+2.5 V and -2.5 V typical respectively). V_{ST} and V_{SB} should be used to monitor the actual full scale input voltage of the device. V_{RT1}, V_{RT2} and V_{RT3} should not be driven to the expected ideal values as is commonly done with standard flash converters. When not being used, a decoupling capacitor of .01 µF connected to AGND from each tap is recommended to minimize high frequency noise injection.

Figure 2 - Typical Interface Circuit

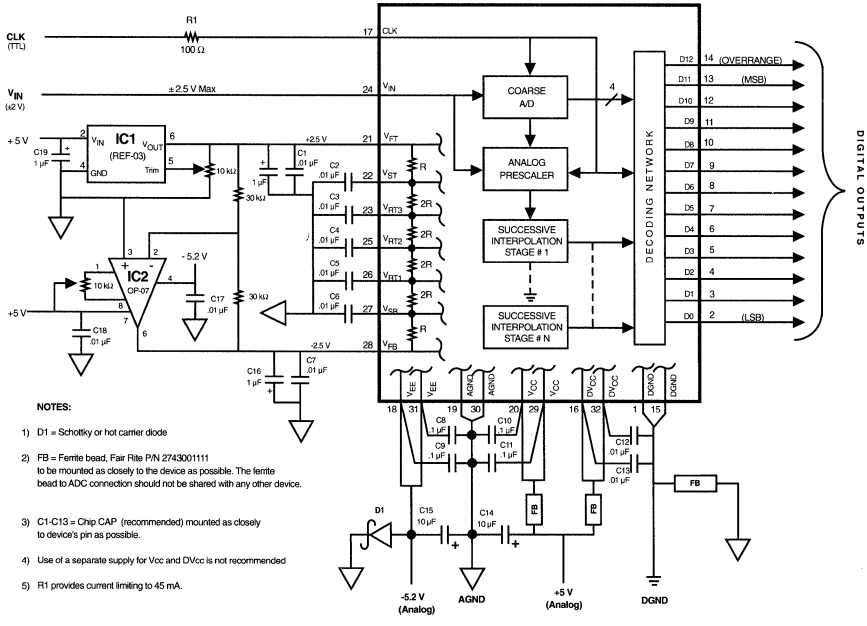


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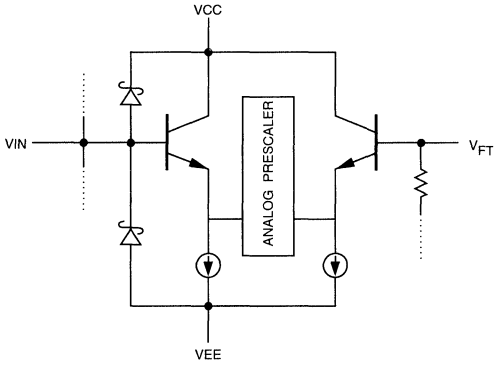
Figure 3 - Analog Equivalent Input Circuit



The analog input range will scale proportionally with respect to the reference voltage if a different input range is required. The maximum scaling factor for device operation is ± 20% of the recommended reference voltages of V_{FT} and V_{FB}. However, because the device is laser trimmed to optimize performance with ± 2.5 V references, the accuracy of the device will degrade if operated beyond a ± 2% range.

An example of a recommended reference driver circuit is shown in figure 2. IC1 is REF-03, the +2.5 V reference with a tolerance of 0.6% or +/- 0.015 V. The potentiometer R1 is 10 kΩ and supports a minimum adjustable range of up to 150 mV. IC2 is recommended to be an OP-07 or equivalent device. R2 and R3 must be matched to within 0.1% with good TC tracking to maintain a 0.3 LSB matching between V_{FT} and V_{FB}. If 0.1% matching is not met, then potentiometer R4 can be used to adjust the V_{FB} voltage to the desired level. R1 and R4 should be adjusted such that V_{ST} and V_{SB} are exactly +2.0 V and -2.0 V respectively.

The following errors are defined:
+FS error = top of ladder offset voltage = Δ(+FS -V_{ST})
-FS error = bottom of ladder offset voltage = Δ(-FS -V_{SB})

Where the +FS (full scale) input voltage is defined as the output 1 LSB above the transition of 1—10 and 1—11 and the -FS input voltage is defined as the output 1 LSB below the transition of 0—00 and 0—01.

ANALOG INPUT

V_{IN} is the analog input. The full scale input range will be 80% of the reference voltage or ±2 volts with V_{FB}=-2.5 V and V_{FT}=+2.5 V.

The drive requirements for the analog inputs are minimal when compared to conventional Flash converters due to the SPT7921's extremely low input capacitance of only 5 pF and very high input impedance of 300 kΩ. For example, for an input signal of ± 2 V p-p with an input frequency of 10 MHz, the peak output current required for the driving circuit is only 628 μA.

CLOCK INPUT

The SPT7921 is driven from a single-ended TTL input (CLK). For optimal noise performance, the clock input slew rate should be a minimum of 6 ns. Because of this, the use of *fast* logic is recommended. The clock input duty cycle should be 50% where possible, but performance will not be degraded if kept within the range of 40-60%. However, in any case the clock pulse width (tpwH) must be kept at 300 ns maximum to ensure proper operation of the internal track and hold amplifier (see timing diagram). The analog input signal is latched on the rising edge of the CLK.

The clock input must be driven from fast TTL logic (V_{IH} ≤4.5 V, T_{RISE} <6 ns). In the event the clock is driven from a high current source, use a 100 Ω resistor in series to current limit to approximately 45 mA.

DIGITAL OUTPUTS

The format of the output data (D0-D11) is straight binary. (See table 2.) The outputs are latched on the rising edge of CLK with a propagation delay of 14 ns (typ). There is a one clock cycle latency between CLK and the valid output data. (See timing diagram.)

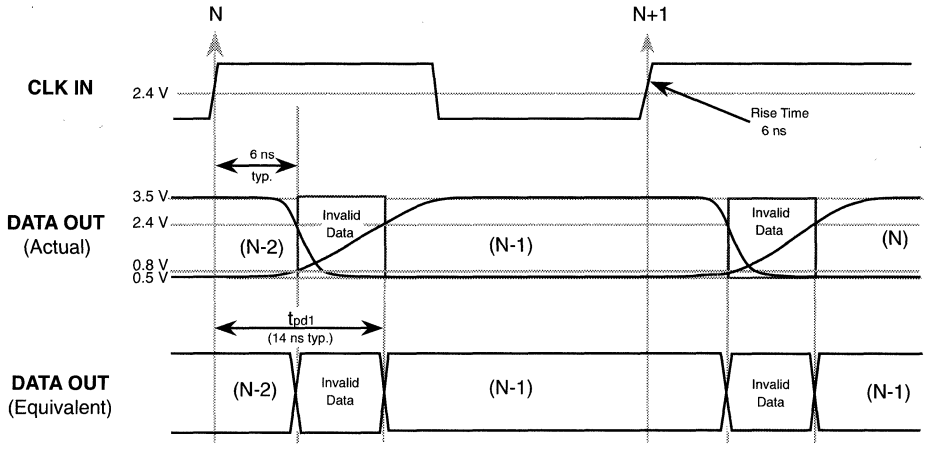
Table 2 - Output Data Information

ANALOG INPUT	OVERRANGE D12	OUTPUT CODE D11-DO
>+2.0 V + 1/2 LSB	1	1111 1111 1111
+2.0 V -1 LSB	O	1111 1111 111Ø
0.0 V	O	ØØØØ ØØØØ ØØØØ
-2.0 V +1 LSB	O	OOOO OOOO OOOØ
<2.0 V	O	OOOO OOOO OOOO

(Ø indicates the flickering bit between logic 0 and 1).

The rise times and fall times of the digital outputs are not symmetrical. The propagation delay of the rise time is typically 14 ns and the fall time is typically 6 ns. (See figure 4.) The nonsymmetrical rise and fall times create approximately 8 ns of invalid data.

Figure 4 - Digital Output Characteristics



OVERRANGE OUTPUT

The overrange output (D12) is an indication that the analog input signal has exceeded the full scale input voltage by 1 LSB. When this condition occurs, the outputs will switch to logic 1s. All other data outputs are unaffected by this operation. This feature makes it possible to include the SPT7921 into higher resolution systems.

EVALUATION BOARD

The EB7921 evaluation board is available to aid designers in demonstrating the full performance of the SPT7921. This board includes a reference circuit, clock driver circuit, output data latches and an on-board reconstruction of the digital data. An application note (AN7921) describing the operation of this board as well as information on the testing of the SPT7921 is also available. Contact the factory for price and availability.

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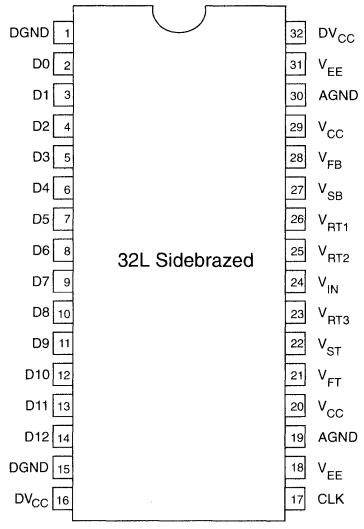
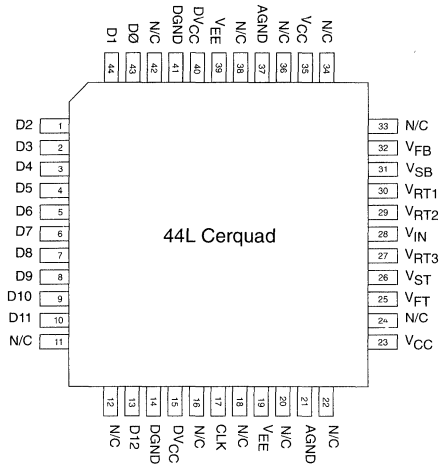
PIN ASSIGNMENTS





PIN FUNCTIONS

NAME	FUNCTION
DGND	Digital Ground
AGND	Analog Ground
D0-D11	TTL Outputs (D0=LSB)
D12	TTL Output Overrange
CLK	Clock Input
V_{EE}	-5.2 V Supply
V_{CC}	+5.0 V supply
V_{RT1}-V_{RT3}	Voltage Reference Taps
V_{IN}	Analog Input
DV_{CC}	Digital +5.0 V Supply (TTL Outputs)
V_{FT}	Force for Top of Reference Ladder
V_{ST}	Sense for Top of Reference Ladder
V_{FB}	Force for Bottom of Reference Ladder
V_{SB}	Sense for Bottom of Reference Ladder

LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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SIGNAL PROCESSING TECHNOLOGIES

SPT7922

12-BIT, 30 MSPS, TTL, A/D CONVERTER

FEATURES

- Monolithic
- 12-Bit 30 MSPS Converter
- 64 dB SNR @ 3.58 MHz Input
- On-Chip Track/Hold
- Bipolar ±2.0 V Analog Input
- Low Power (1.1 W Typical)
- 5 pF Input Capacitance
- TTL Outputs

APPLICATIONS

- Radar Receivers
- Professional Video
- Instrumentation
- Medical Imaging
- Electronic Warfare
- Digital Communications
- Digital Spectrum Analyzers
- Electro-Optics

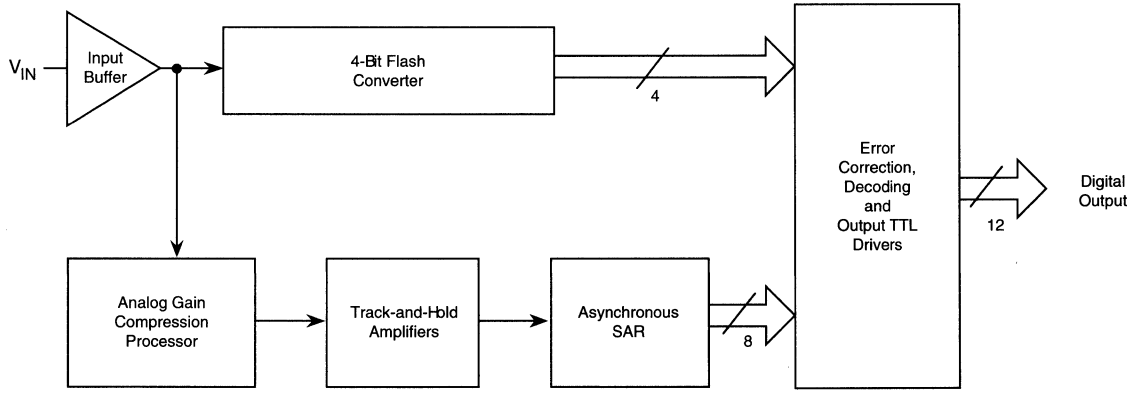
GENERAL DESCRIPTION

The SPT7922 A/D converter is the industry's first 12-bit monolithic A-to-D converter capable of sample rates of greater than 30 MSPS. On board input buffer and track/hold function assures excellent dynamic performance without the need for external components. Drive requirement problems are minimized with an input capacitance of only 5 pF.

Logic inputs and outputs are TTL. An overrange output signal is provided to indicate overflow conditions. Output data format is straight binary. Power dissipation is very low at only 1.1 watts with power supply voltages of +5.0 and -5.2 volts. The SPT7922 also provides a wide input voltage range of ±2.0 volts.

The SPT7922 is available in a small 32-lead ceramic sidebrazed DIP and a 44-lead cerquad package for surface-mount applications. A commercial temperature range of 0 to +70 °C is currently offered. Consult the factory for military temperature availability.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages
- V_{CC} ..... +6 V
- V_{EE} ..... -6 V

Input Voltages
- Analog Input ..... $V_{FB} \leq V_{IN} \leq V_{FT}$
- V_{FT}, V_{FB} ..... +3.0 V, -3.0 V
- Reference Ladder Current ..... 12 m
- CLK IN ..... V_{CC}

Output
- Digital Outputs ..... 0 to -30 mA

Temperature
- Operating Temperature ..... 0 to +70 °C
- Junction Temperature ..... 175 °C
- Lead Temperature, (soldering 10 seconds) ..... 300 °C
- Storage Temperature ..... -65 to +150 °C

Note: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

$T_A=T_{MIN}$ to T_{MAX}, V_{CC}=+5.0 V, V_{EE}=-5.2 V, DV_{CC}=+5.0 V, V_{IN}=±2.0 V, V_{SB}=-2.0 V, V_{ST}=+2.0 V, f_{clock}=30 MHz, 50% clock duty cycle, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7922 MIN	SPT7922 TYP	SPT7922 MAX	UNITS
Resolution			12			Bits
DC Accuracy (+25 °C)						
Integral Nonlinearity	± Full Scale	IV		±2.0		LSB
Differential Nonlinearity	250 kHz Sample Rate	IV		±0.8		LSB
No Missing Codes		I		Guaranteed		
Analog Input						
Input Voltage Range		VI		±2.0		V
Input Bias Current	+25 °C	I		30	60	µA
Input Resistance	V_{IN}=0 V, +25 °C	I	100	300		kΩ
Input Capacitance		V		5		pF
Input Bandwidth	3 dB Small Signal	V		120		MHz
+FS Error		V		±5.0		LSB
-FS Error		V		±5.0		LSB
Reference Input						
Reference Ladder Resistance		VI	500	800		Ω
Reference Ladder Tempco		V		0.8		Ω/°C
Timing Characteristics						
Maximum Conversion Rate		VI	30	40		MHz
Overvoltage Recovery Time		V		20		ns
Pipeline Delay (Latency)		VI			1	Clock Cycle
Output Delay	T_A=+25 °C	V		14	18	ns
Aperture Delay Time	T_A=+25 °C	V		1		ns
Aperture Jitter Time	T_A=+25 °C	V		5		ps-RMS
Dynamic Performance						
Effective Number of Bits						
fin=500 kHz				10.0		Bits
fin=1 MHz				9.8		Bits
fin=3.58 MHz				9.5		Bits
Signal-To-Noise Ratio (without Harmonics)						
fin=500 kHz	+25 °C	I	63	66		dB
	T_{MIN} to T_{MAX}	IV	58	61		dB
fin=1 MHz	+25 °C	I	63	65		dB
	T_{MIN} to T_{MAX}	IV	58	60		dB
fin=3.58 MHz	+25 °C	I	62	64		dB
	T_{MIN} to T_{MAX}	IV	58	60		dB

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ELECTRICAL SPECIFICATIONS

T_A=T_{MIN} to T_{MAX}, V_{CC}=+5.0 V, V_{EE}=-5.2 V, DV_{CC}=+5.0 V, V_{IN}=±2.0 V, V_{SB}=-2.0 V, V_{ST}=+2.0 V, f_{clock}=30 MHz, 50% clock duty cycle, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT7922 MIN	SPT7922 TYP	SPT7922 MAX	UNITS
Dynamic Performance						
Harmonic Distortion						
fin=500 kHz	+25 °C	I	63	65		dB
	T_{MIN} to T_{MAX}	IV	59	61		dB
fin=1.0 MHz	+25 °C	I	62	64		dB
	T_{MIN} to T_{MAX}	IV	58	60		dB
fin=3.58 MHz	+25 °C	I	59	61		dB
	T_{MIN} to T_{MAX}	IV	57	59		dB
Signal-to-Noise and Distortion (SINAD)						
fin=500 kHz	+25 °C	I	60	62		dB
	T_{MIN} to T_{MAX}	IV	55	57		dB
fin=1.0 MHz	+25 °C	I	59	61		dB
	T_{MIN} to T_{MAX}	IV	55	57		dB
fin=3.58 MHz	+25 °C	I	57	59		dB
	T_{MIN} to T_{MAX}	IV	54	56		dB
Spurious Free Dynamic Range[2]	+25 °C	V		74		dB
Differential Phase[3]	+25 °C	V		0.2		Degree
Differential Gain[3]	+25 °C	V		0.7		%
Digital Inputs						
Logic "1" Voltage		V	2.4		4.0	V
Logic "0" Voltage		V			0.8	V
Maximum Input Current Low	+25 °C	I	0	+5	+20	µA
Maximum Input Current High	+25 °C	I	0	+5	+20	µA
Pulse Width Low (CLK)		IV	15			ns
Pulse Width High (CLK)		IV	15		300	ns
Digital Outputs						
Logic "1" Voltage	+25 °C	I	2.4			V
Logic "0" Voltage	+25 °C	I			0.6	V
Power Supply Requirements						
Voltages V_{CC}		IV	4.75	5.0	5.25	V
DV_{CC}		IV	4.75	5.0	5.25	V
$-V_{EE}$		IV	-4.95	-5.2	-5.45	V
Currents I_{CC}	+25 °C	I		135	150	mA
DI_{CC}		IV		40	55	mA
$-I_{EE}$	+25 °C	I		45	70	mA
Power Dissipation		VI		1.1	1.3	W
Power Supply Rejection	(5 V ±0.25 V, -5.2 ±0.25 V)	V		1.0		LSB

1 Typical thermal impedances (unsoldered, in free air):
32L sidebrazed DIP:
θ_{ja} = 50 °C/W
44L cerquad:
θ_{ja} = 78 °C/W
θ_{ja} at 1 M/s airflow = 58 °C/W
θ_{jc} = 3.3 °C/W

2 fin = 1 MHz.

3 fin = 3.58 and 4.35 MHz.

Figure 1A: Timing Diagram

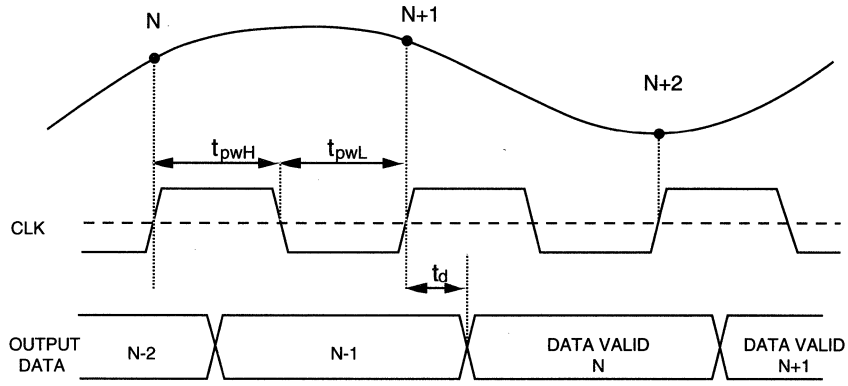

Figure 1B: Single Event Clock

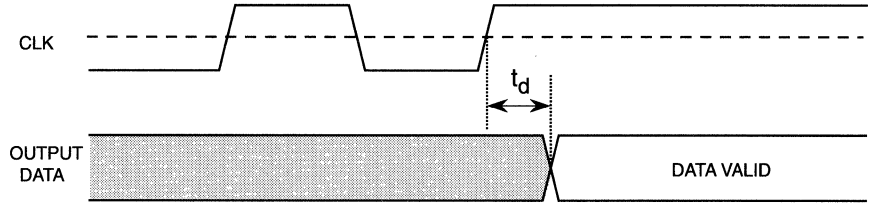

Table 1 - Timing Parameters

PARAMETERS	DESCRIPTION	MIN	TYP	MAX	UNITS
t_d	CLK to Data Valid Prop Delay	-	14	18	ns
t_{pwH}	CLK High Pulse Width	15	-	300	ns
t_{pwL}	CLK Low Pulse Width	15	-	-	ns

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests; therefore, $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

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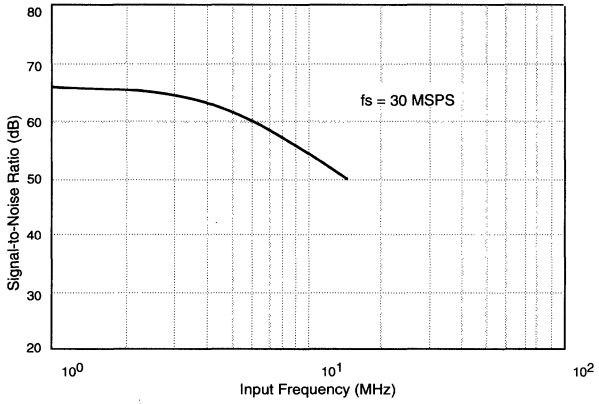
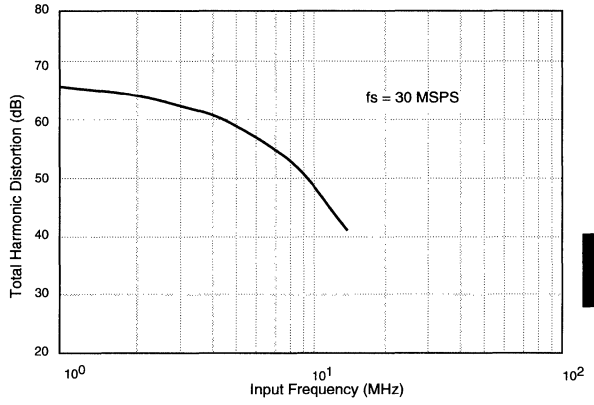
PERFORMANCE CHARACTERISTICS

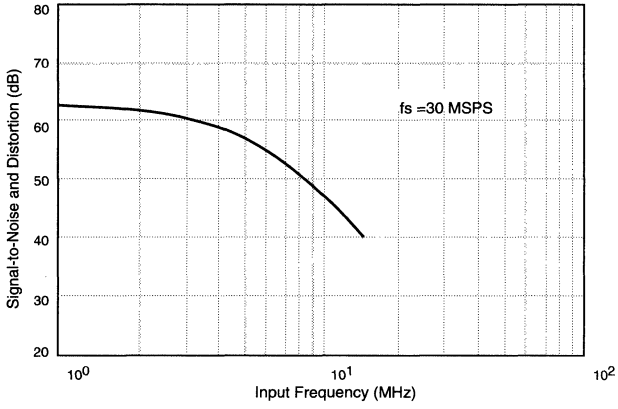
SNR vs Input Frequency



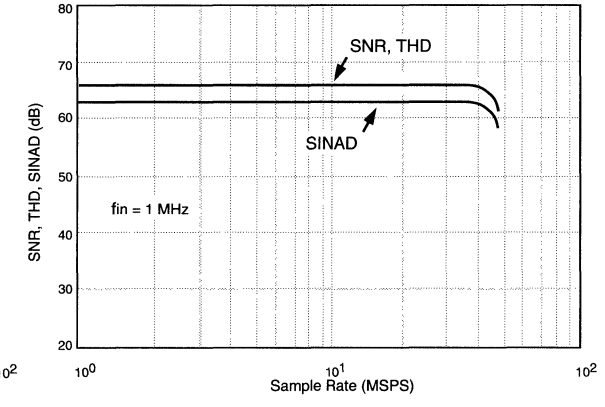
THD vs Input Frequency



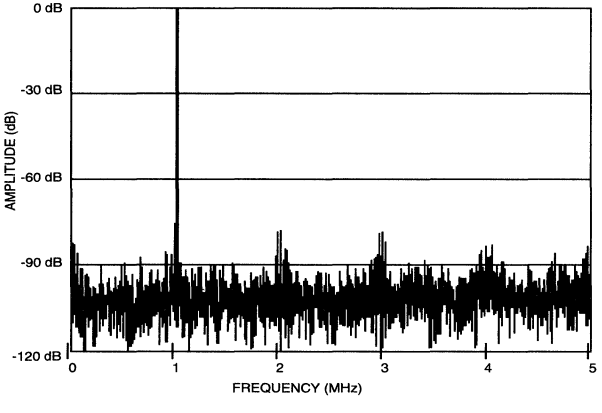
SINAD vs Input Frequency



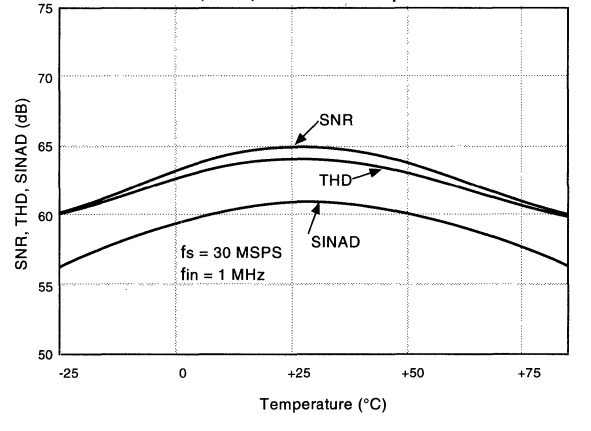
SNR, THD, SINAD vs Sample Rate



SPT7922
Spectral Response



SNR, THD, SINAD vs Temperature



TYPICAL INTERFACE CIRCUIT

The SPT7922 requires few external components to achieve the stated operation and performance. Figure 2 shows the typical interface requirements when using the SPT7922 in normal circuit operation. The following section provides a description of the pin functions and outlines critical performance criteria to consider for achieving the optimal device performance.

POWER SUPPLIES AND GROUNDING

The SPT7922 requires -5.2 V and +5 V analog supply voltages. The +5 V supply is common to analog V_{CC} and digital DV_{CC}. A ferrite bead in series with each supply line is intended to reduce the transient noise injected into the analog V_{CC}. These beads should be connected as closely as possible to the device. The connection between the beads and the SPT7922 should not be shared with any other device. Each power supply pin should be bypassed as closely as possible to the device. Use 0.1 µF for V_{EE} and V_{CC}, and 0.01 µF for DV_{CC} (chip caps are preferred).

AGND and DGND are the two grounds available on the SPT7922. These two internal grounds are isolated on the device. The use of ground planes is recommended to achieve optimum device performance. DGND is needed for the DV_{CC} return path (40 mA typical) and for the return path for all digital output logic interfaces. AGND and DGND should be separated from each other and connected together only at the device through a ferrite bead.

A Schottky or hot carrier diode connected between AGND and V_{EE} is required. The use of separate power supplies between V_{CC} and DV_{CC} is not recommended due to potential power supply sequencing latch-up conditions. Using the recommended interface circuit shown in figure 2 will provide optimum device performance for the SPT7922.

VOLTAGE REFERENCE

The SPT7922 requires the use of two voltage references: V_{FT} and V_{FB}. V_{FT} is the force for the top of the voltage reference ladder (+2.5 V typ), V_{FB} (-2.5 V typ) is the force for the bottom of the voltage reference ladder. Both voltages are applied across an internal reference ladder resistance of 800 ohms. The +2.5 V voltage source for reference V_{FT} must be current limited to 20 mA maximum if a different driving circuit is used in place of the recommended reference circuit shown in figures 2 and 3. In addition, there are five reference ladder taps (V_{ST}, V_{RT1}, V_{RT2}, V_{RT3}, and V_{SB}). V_{ST} is the sense for the top of the reference ladder (+2.0 V), V_{RT2} is the midpoint of the ladder (0.0 V typ) and V_{SB} is the sense for the bottom of the reference ladder (-2.0 V). V_{RT1} and V_{RT3} are quarter point ladder taps (+1.0 and -1.0 V typical, respectively). The voltages seen at V_{ST} and V_{SB} are the true full scale input voltages of the device when V_{FT} and V_{FB} are driven to the recommended voltages (+2.5 V and -2.5 V typical respectively). V_{ST} and V_{SB} should be used to monitor the actual full scale input voltage of the device. V_{RT1}, V_{RT2} and V_{RT3} should not be driven to the expected ideal values as is commonly done with standard flash converters. When not being used, a decoupling capacitor of .01 µF connected to AGND from each tap is recommended to minimize high frequency noise injection.

Figure 2 - Typical Interface Circuit

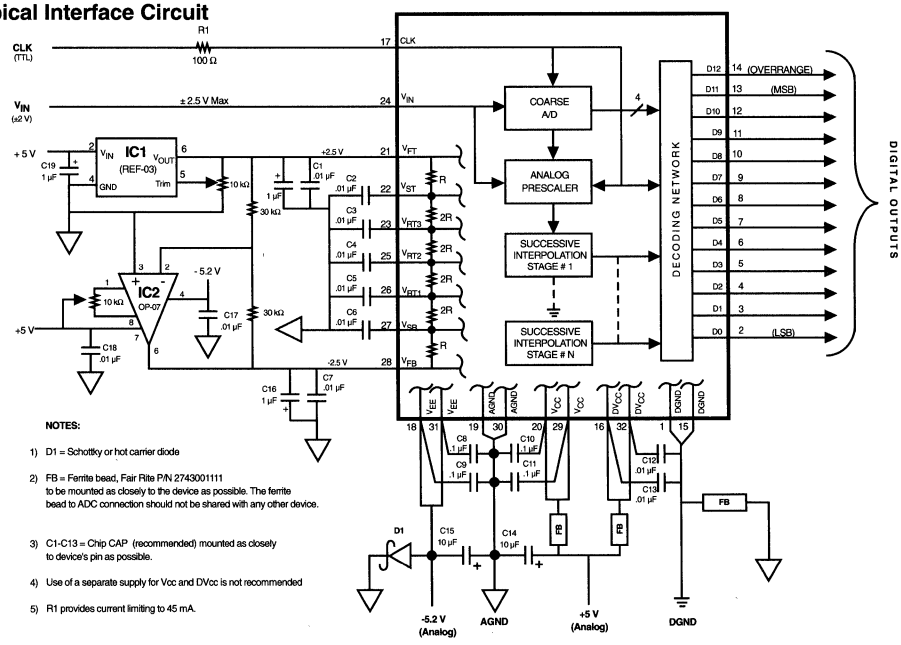


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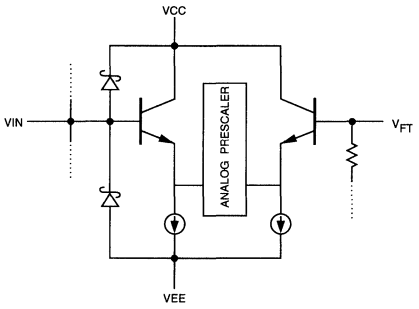
Figure 3 - Analog Equivalent Input Circuit



The analog input range will scale proportionally with respect to the reference voltage if a different input range is required. The maximum scaling factor for device operation is ± 20% of the recommended reference voltages of V_{FT} and V_{FB}. However, because the device is laser trimmed to optimize performance with ± 2.5 V references, the accuracy of the device will degrade if operated beyond a ± 2% range.

An example of a recommended reference driver circuit is shown in figure 2. IC1 is REF-03, the +2.5 V reference with a tolerance of 0.6% or +/- 0.015 V. The potentiometer R1 is 10 kΩ and supports a minimum adjustable range of up to 150 mV. IC2 is recommended to be an OP-07 or equivalent device. R2 and R3 must be matched to within 0.1% with good TC tracking to maintain a 0.3 LSB matching between V_{FT} and V_{FB}. If 0.1% matching is not met, then potentiometer R4 can be used to adjust the V_{FB} voltage to the desired level. R1 and R4 should be adjusted such that V_{ST} and V_{SB} are exactly +2.0 V and -2.0 V respectively.

The following errors are defined:

+FS error = top of ladder offset voltage = Δ(+FS -V_{ST})
-FS error = bottom of ladder offset voltage = Δ(-FS -V_{SB})

Where the +FS (full scale) input voltage is defined as the output 1 LSB above the transition of 1—10 and 1—11 and the -FS input voltage is defined as the output 1 LSB below the transition of 0—00 and 0—01.

ANALOG INPUT

V_{IN} is the analog input. The full scale input range will be 80% of the reference voltage or ±2 volts with V_{FB}=-2.5 V and V_{FT}=+2.5 V.

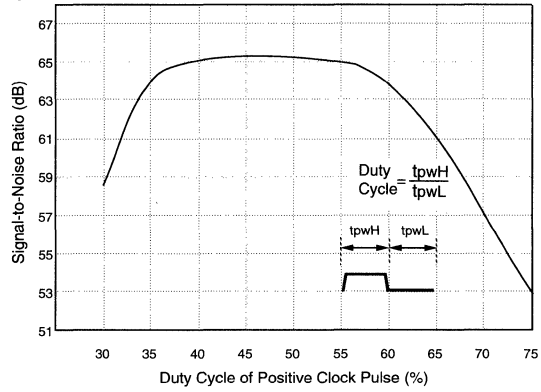
The drive requirements for the analog inputs are minimal when compared to conventional Flash converters due to the SPT7922's extremely low input capacitance of only 5 pF and very high input impedance of 300 kΩ. For example, for an input signal of ± 2 V p-p with an input frequency of 10 MHz, the peak output current required for the driving circuit is only 628 µA.

CLOCK INPUT

The SPT7922 is driven from a single-ended TTL input (CLK). The CLK pulse width (tpwH) must be kept between 15 ns and 300 ns to ensure proper operation of the internal track-and-hold amplifier. (See timing diagram.) When operating the SPT7922 at sampling rates above 3 MSPS, it is recommended that the clock input duty cycle be kept at 50% to optimize performance. (See figure 4.) The analog input signal is latched on the rising edge of the CLK.

The clock input must be driven from fast TTL logic (V_{IH} ≤4.5 V, T_{RISE} <6 ns). In the event the clock is driven from a high current source, use a 100 Ω resistor in series to current limit to approximately 45 mA.

Figure 4 - SNR vs Clock Duty Cycle



DIGITAL OUTPUTS

The format of the output data (D0-D11) is straight binary. (See table 2.) The outputs are latched on the rising edge of CLK with a propagation delay of 14 ns (typ). There is a one clock cycle latency between CLK and the valid output data. (See timing diagram.)

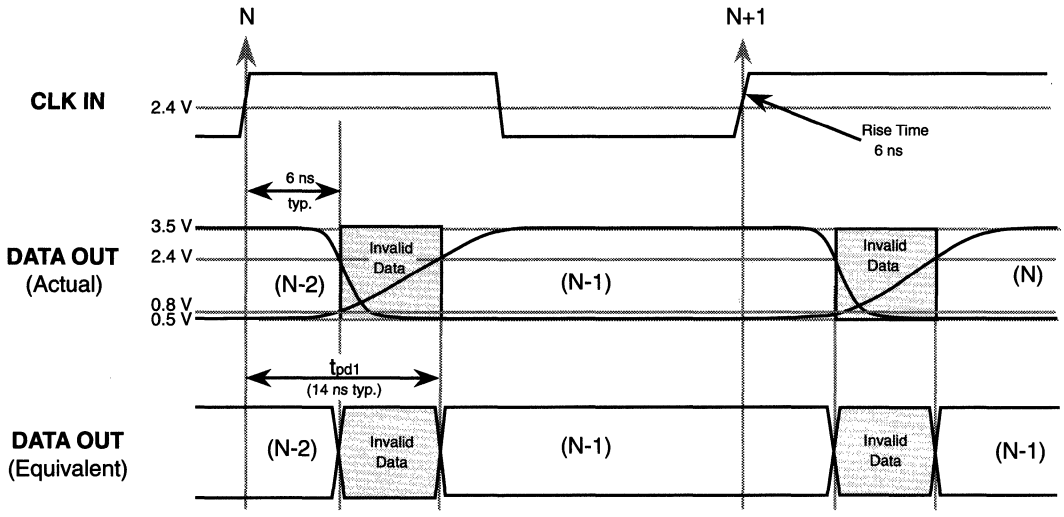
Table 2 - Output Data Information

ANALOG INPUT	OVERRANGE D12	OUTPUT CODE D11-DO
>+2.0 V + 1/2 LSB	1	1111 1111 1111
+2.0 V -1 LSB	O	1111 1111 111Ø
0.0 V	O	ØØØØ ØØØØ ØØØØ
-2.0 V +1 LSB	O	OOOO OOOO OOOØ
<2.0 V	O	OOOO OOOO OOOO

(Ø indicates the flickering bit between logic 0 and 1).

The rise times and fall times of the digital outputs are not symmetrical. The propagation delay of the rise time is typically 14 ns and the fall time is typically 6 ns. (See figure 5.) The nonsymmetrical rise and fall times create approximately 8 ns of invalid data.

Figure 5 - Digital Output Characteristics



OVERRANGE OUTPUT

The overrange output (D12) is an indication that the analog input signal has exceeded the full scale input voltage by 1 LSB. When this condition occurs, the outputs will switch to logic 1s. All other data outputs are unaffected by this operation. This feature makes it possible to include the SPT7922 into higher resolution systems.

EVALUATION BOARD

The EB7922 evaluation board is available to aid designers in demonstrating the full performance of the SPT7922. This board includes a reference circuit, clock driver circuit, output data latches and an on-board reconstruction of the digital data. An application note (AN7922) describing the operation of this board as well as information on the testing of the SPT7922 is also available. Contact the factory for price and availability.

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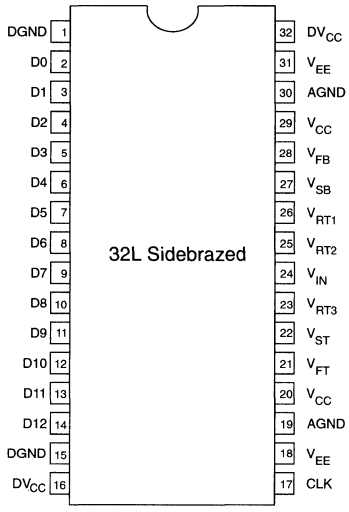
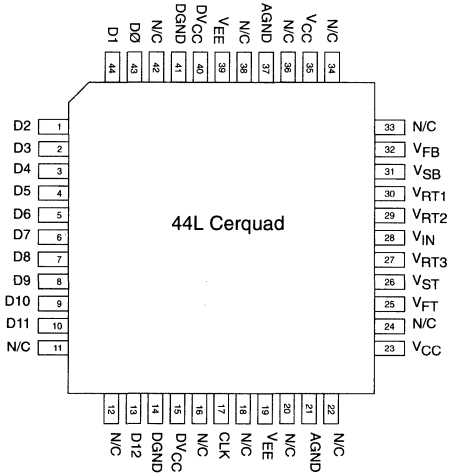
PIN ASSIGNMENTS





PIN FUNCTIONS

NAME	FUNCTION
DGND	Digital Ground
AGND	Analog Ground
D0-D11	TTL Outputs (D0=LSB)
D12	TTL Output Overrange
CLK	Clock Input
V_{EE}	-5.2 V Supply
V_{CC}	+5.0 V supply
V_{RT1}-V_{RT3}	Voltage Reference Taps
V_{IN}	Analog Input
DV_{CC}	Digital +5.0 V Supply (TTL Outputs)
V_{FT}	Force for Top of Reference Ladder
V_{ST}	Sense for Top of Reference Ladder
V_{FB}	Force for Bottom of Reference Ladder
V_{SB}	Sense for Bottom of Reference Ladder

LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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SIGNAL PROCESSING TECHNOLOGIES

SPT7930

12-BIT, 5 MSPS, 450 mW A/D CONVERTER

ADVANCED INFORMATION

3

FEATURES

- 12-Bit/5 MSPS Analog-to-Digital Converter
- Monolithic CMOS
- Internal Track-and-Hold
- Internal Voltage Reference
- Low Power Dissipation: 450 mW
- 2 Vp-p Differential/Single-ended Analog Input Range
- Single +5 Volt Power Supply with option for 3.3 V Digital Outputs
- Tri-Stable, TTL-Compatible Outputs

APPLICATIONS

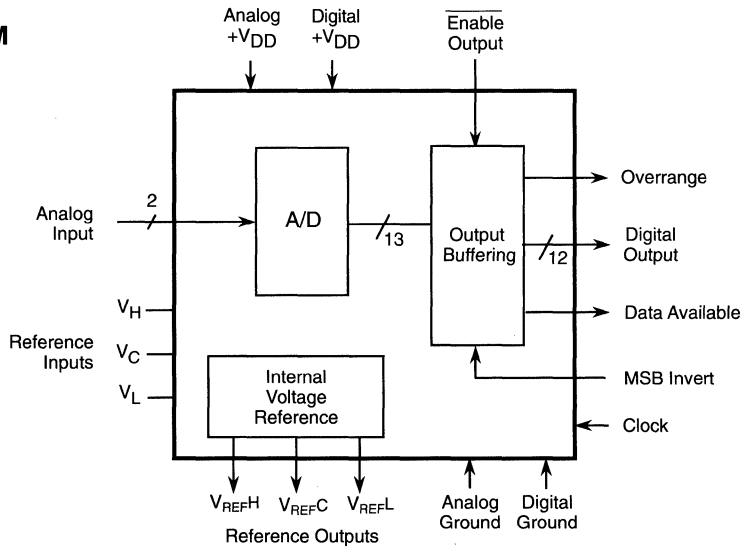
- CCD Imaging Sensors
- Document and Film Scanners
- Medical Imaging
- Electro-Optics
- Transient Signal Analysis

GENERAL DESCRIPTION

The SPT7930 12-bit, 5 MSPS analog-to-digital converter is a multi-stage pipelined converter architecture built in a monolithic CMOS process. It delivers excellent low noise performance with a typical power dissipation of only 450 mW. It is ideal for CCD image sensing and scanning applications. The internal track-and-hold, internal voltage reference and the single +5 V supply voltage make interfacing this device a very simple task.

The SPT7930 has a differential analog input that can be configured to run in a single-ended mode with minimal effort. It is available in 28L DIP and SOIC packages and in a 44L cerquad package for the commercial temperature range. Contact the factory for availability of military and /883 versions.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages

AV_{DD} ..... +6 V
DV_{DD} ..... +6 V

Input Voltages

Analog Input ..... -0.5 V to AV_{DD} +0.5 V
V_{Ref} ..... 0 to AV_{DD}
CLK Input ..... V_{DD}
AV_{DD} - DV_{DD} ..... ±100 mV
AGND - DGND ..... ±100 mV

Output

Digital Outputs ..... 10 mA

Temperature

Operating Temperature ..... 0 to 70 °C
Junction Temperature ..... 175 °C
Lead Temperature, (soldering 10 seconds) ..... 300 °C
Storage Temperature ..... -65 to +150 °C

Note: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

T_A=25 °C, AV_{DD} = DV_{DD} = +5.0 V, V_{IN} = 1.25 to 3.25 V, f_S = 5 MSPS, V_{RHS} = 4.0 V, V_{RLS} = 0.0 V, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
DC Performance						
Resolution				12		Bits
Differential Linearity				±0.5		LSB
Integral Linearity				±1.0		LSB
No Missing Codes				Guaranteed		
Analog Input						
Input Voltage Range	DC Offset of +2.25 V			2		V p-p
Input Resistance				250		kΩ
	Full Temp.			TBD		kΩ
Input Capacitance				10		pF
Input Bandwidth	Full Power			TBD		MHz
Offset				TBD		LSB
Gain Error				10	20	LSB
Timing Characteristics						
Conversion Rate				5		MSPS
Pipeline Delay (Latency)				6		Clk Cycles
Transient Response (0.01% Settling)				18		ns
Over Voltage Recovery Time				TBD		ns
Aperture Delay Time				1		ns
Aperture Jitter Time				4		ps RMS
Dynamic Performance						
Effective Number of Bit						
f_{IN} = 1.0 MHz				11		Bits
f_{IN} = 2.0 MHz				11		Bits
Signal-To-Noise Ratio						
f_{IN}= 1.0 MHz				69		dB
f_{IN} = 2.0 MHz				68		dB

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ELECTRICAL SPECIFICATIONS

T_A=25 °C, AV_{DD} = DV_{DD} = +5.0 V, V_{IN} = 1.25 to 3.25 V, f_S = 5 MSPS, V_{RHS} = 4.0 V, V_{RLS} = 0.0 V, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
Dynamic Performance						
Harmonic Distortion						
f_{IN} = 1.0 MHz				68		dBc
f_{IN} = 2.0 MHz				67		dBc
Spurious Free Dynamic Range				TBD		dB
Two-Tone Intermodulation Distortion Rejection				TBD		dBc
Power Supply Requirements						
$+V_S$ Supply Voltage			4.75	5.0	5.25	V
$+V_S$ Supply Current				90	100	mA
Power Dissipation				450	500	mW

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions: All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests; therefore, $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

NOTES

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NOTES

LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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Section 4 Digital-to-Analog Converters

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SIGNAL PROCESSING TECHNOLOGIES

SPT5100

8-BIT, 20 MWPS DUAL CHANNEL VIDEO DAC

PRELIMINARY INFORMATION

FEATURES

- 8-Bit Dual Channel Video Digital-to-Analog Converter
- 20 MWPS Operation
- Low Power: 70 mW
- Operating Temperature Range: 0 to +70 °C
- 5 V Monolithic CMOS
- 32-pin QFP Package (7 mm by 7 mm, 0.8 mm pitch)

APPLICATIONS

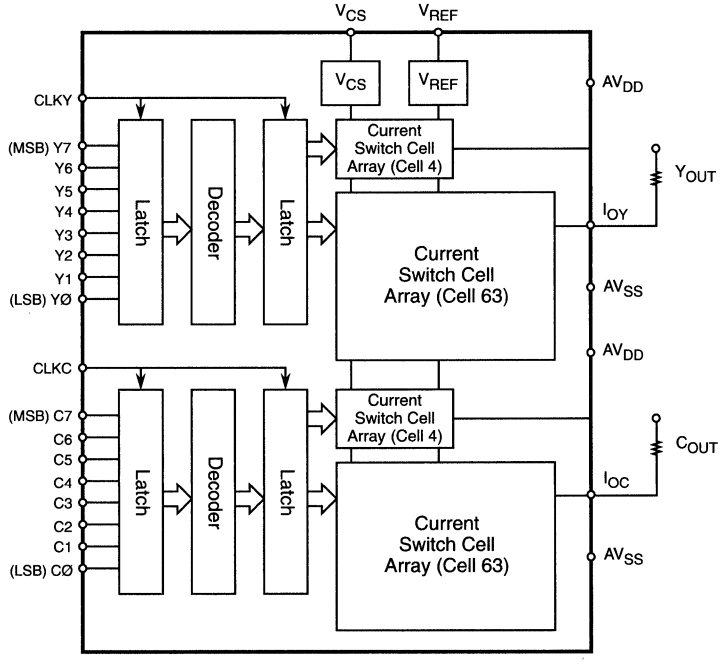
- High-Speed Digital-to-Analog Conversion
- Y/ C, S-Video Processing
- Desktop Video Processing
- Digtial TV
- Satellite TV Decoders
- Digital VCRs

4

GENERAL DESCRIPTION

The SPT5100 is a 8-bit, 20 MWPS, dual channel video digital-to-analog converter specifically designed for video processing applications including digital TV decoders and digital VCRs. A single external resistor controls the full-scale output current. The differential linearity errors of the DACs are guaranteed to be a maximum of ±0.5 LSB over the full temperature range. The device is available in a 32-pin QFP package in a commercial temperature range.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING (Beyond which damage may occur)[1]

Supply Voltages
AV_{DD} (measured to GND) ..... -0.3 to 7.0 V

Input Voltage
Clock and Data ..... GND to AV_{DD}

Output Current
I_{OUT} ..... 0 to 8 mA

Temperature
Operating, ambient ..... 0 to +70 °C
Storage ..... -55 to + 125 °C

Note: 1. Operation at any Absolute Maximum Ratings is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

f_{CLK} = 20 MHz, AV_{DD} = 5.0 V, Output Pull-Up Load = 240 Ω, T_A = 25 °C

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS						
DC Performance						
Resolution				8.0		Bits
Differential Linearity	$T_A = T_{MIN}$ to T_{MAX}	I		±0.25	±0.5	LSB
Integral Linearity		I		±0.5	±1.0	LSB
Analog Outputs						
Output Full Scale Voltage		I	0.85	1.0	1.15	V
Compliance Voltage		I	0.5	1.0	1.2	V
Dynamic Performance						
Conversion Rate		I	20			MWPS
Propagation Delay		V		12		ns
Crosstalk		V		-47		dB
Digital Inputs and Timing						
Input Current, Logic High	V_{IH} = 5 V	I			5	µA
Logic Low	V_{IL} = 0 V	I	-5			µA
Set-Up Time, Data and Controls (t_S)		I	5			ns
Hold Time, Data and Controls (t_h)		I	10			ns
Clock Pulse Width (Low) (t_{PW0})		I	25			ns
Clock Pulse Width (High) (t_{PW1})		I	25			ns
Power Supply Requirements						
Supply Voltage		I	4.75		5.25	V
Supply Current		V		14		mA
Power Dissipation		V		70		mW

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests; therefore, $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

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INTERFACE CONSIDERATIONS

Figure 2 shows a typical interface circuit of the SPT5100 in normal circuit operation.

SUPPLY AND GROUND CONSIDERATIONS

SPT suggests that all power supply pins (AV_{DD}) be tied together and decoupled using a 0.1 µF ceramic capacitor in parallel with a 10 µF tantalum capacitor. These decoupling capacitors should be tied between the power supply line and ground.

INTRNAL REFERENCE VOLTAGE (V_{REF})

Voltage reference is internally generated. Connect a 0.1 µF bypass capacitor with the shortest possible lead length between V_{REF} and AV_{SS}.

FULL-SCALE ADJUST CONTROL (V_{CS})

Connect a 0.1 µF bypass capacitor with the shortest possible lead length between V_{CS} and AV_{SS}. A resistor connected between this pin and AV_{CC} controls the magnitude of the full-scale video signal.

The output full-scale voltage of the SPT5110 can be kept constant and stable by keeping the value of V_{CS} to ground constant. The full-scale voltage changes from 0.5 V to 1.5 V according to V_{CS} changing from approximately 1.0 to 1.4 V.

CURRENT OUTPUTS

The Y channel and C channel current outputs should have a load resistor connected to AV_{DD}. The resistors are typically 240 Ω and should be kept in the 150 Ω to 250 Ω range.

LATCH-UP CONSIDERATIONS

In order to prevent a possible latch-up condition, SPT suggests that a 100 Ω resistor be placed in series with each clock input pin.

Table 1 - Binary Code Table
1 LSB = 3.91 mV

Step	Digital Input A7 (MSB)	A6	A5	A4	A3	A2	A1	A0 (LSB)	Analog Out (V)
0	0	0	0	0	0	0	0	0	4.0000
1	0	0	0	0	0	0	0	1	4.0039
2	0	0	0	0	0	0	1	0	4.0078
3	0	0	0	0	0	0	1	1	4.0117
.				.					.
.				.					.
.				.					.
254	1	1	1	1	1	1	1	0	4.9922
255	1	1	1	1	1	1	1	1	4.9961

Figure 1 - Typical Interface Circuit

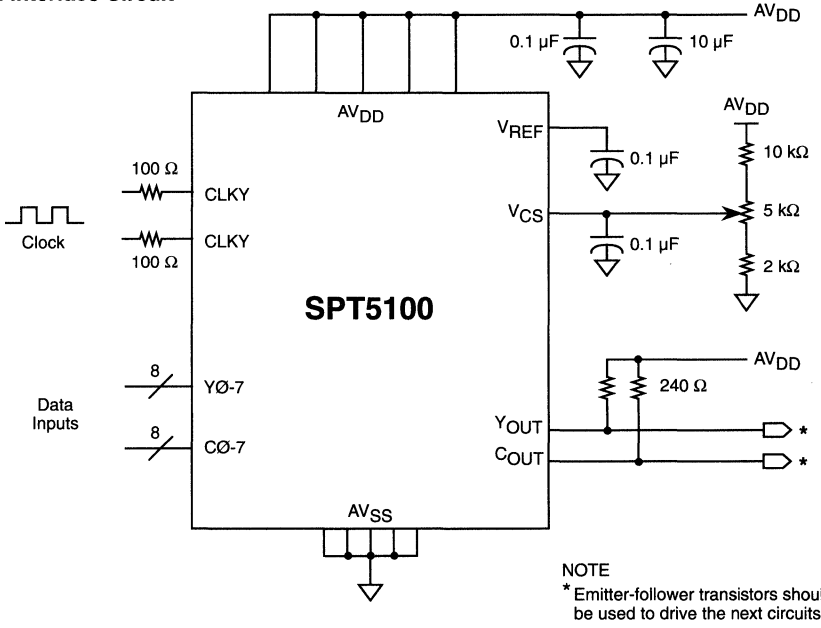


Figure 2 - Typical Performance Characteristics

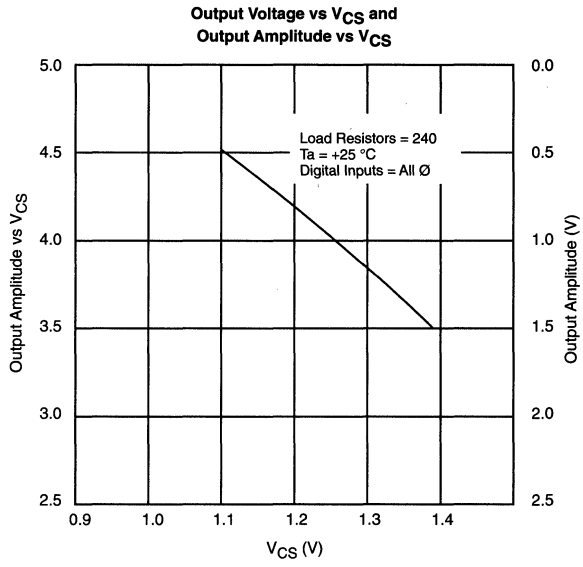
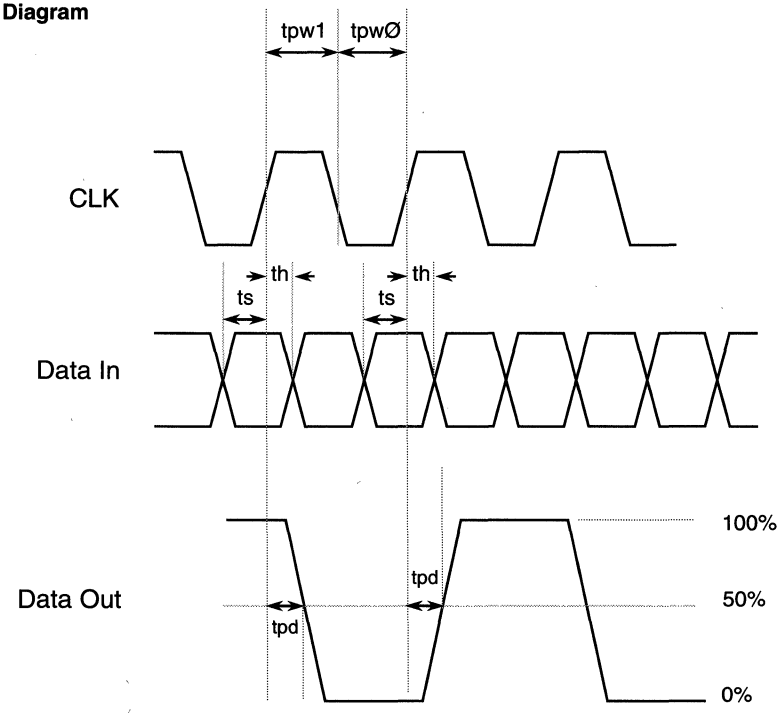


Figure 3 - Timing Diagram



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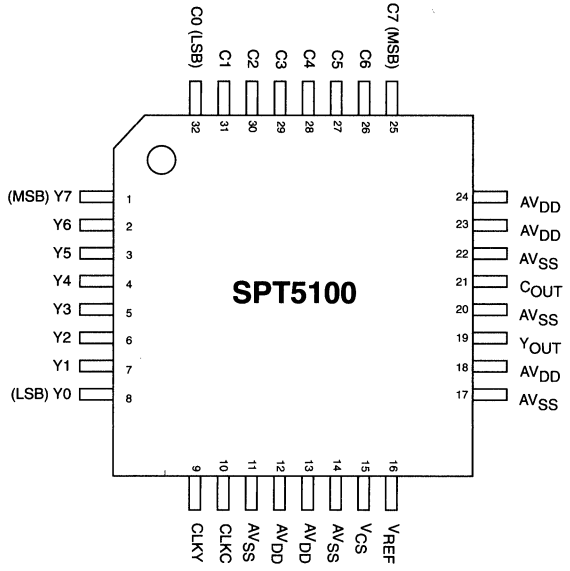
PIN ASSIGNMENTS



PIN FUNCTIONS

NAME	FUNCTION
C_{OUT}	C Channel Analog Current Output
Y_{OUT}	Y Channel Analog Current Output
C7 - C0	C Channel Data Inputs
Y7 - Y0	Y Channel Data Inputs
CLKY	Y Channel Clock Input
CLKC	C Channel Clock Input
V_{REF}	Voltage Reference (A 0.1 µF ceramic capacitor should be used)
V_{CS}	Full-Scale Adjust Control Voltage 1 to 1.4 V
AV_{SS}	Ground
AV_{DD}	Power Supply Voltage

LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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SIGNAL PROCESSING TECHNOLOGIES

SPT5110

8-BIT, 30 MWPS TRIPLE VIDEO DAC

PRELIMINARY INFORMATION

FEATURES

- 8-Bit Triple Video Digital-to-Analog Converter
- 30 MWPS Operation (typ)
- Low Power: 135 mW
- Operating Temperature Range: 0 to +70 °C
- 5 V Monolithic CMOS
- 48-pinVQFP Package

APPLICATIONS

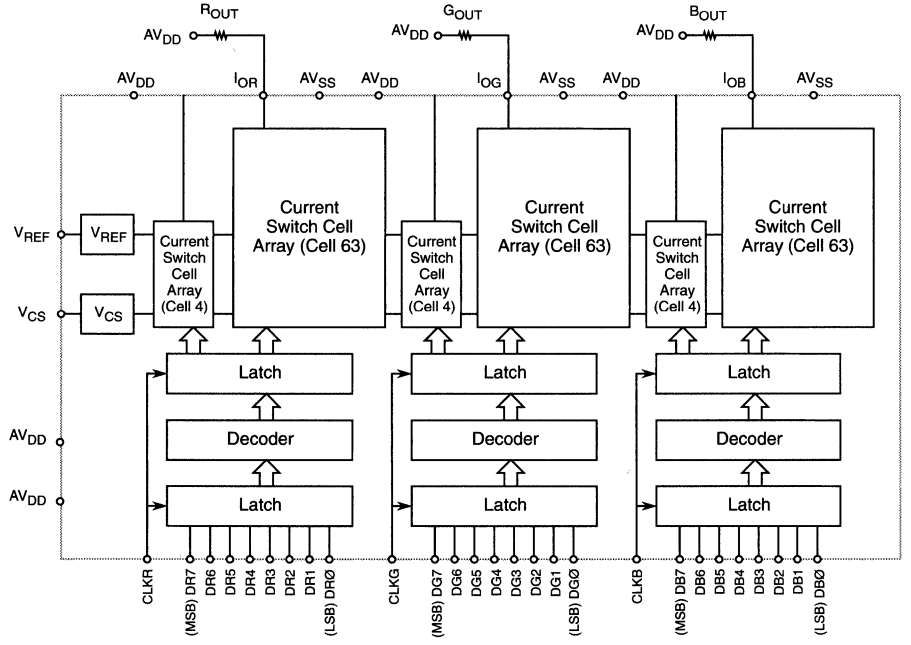
- High-speed Digital-to-Analog Conversion
- High Performance, High Resolution Color Graphics
- Desktop Video Processing
- Digital Television

4

GENERAL DESCRIPTION

The SPT5110 is a 8-bit, 30 MWPS triple video digital-to-analog converter specifically designed for high performance, high resolution color graphics monitor and video processing applications. A single external resistor controls the full-scale output current. The differential linearity errors of the DACs are guaranteed to be a maximum of ±0.5 LSB over the full temperature range. The device is available in a 48-pin VQFP package in a temperature range from 0 °C to +70 °C.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING (Beyond which damage may occur)[1]

Supply Voltages
AV_{DD} (measured to GND) ..... -0.3 to 7.0 V

Input Voltage
Clock and Data ..... GND to AV_{DD}

Output Current
I_{OUT} ..... 0 to 7 mA

Temperature
Operating, ambient ..... 0 to +70 °C
Storage ..... -55 to + 125 °C

Note: 1. Operation at any Absolute Maximum Ratings is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

f_{CLK} = 20 MHz, AV_{DD} = 5.0 V, Output Pull-Up Load = 240 Ω, T_A = 25 °C

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS						
DC Performance						
Resolution				8.0		Bits
Differential Linearity		I		±0.25	±0.3	LSB
Differential Linearity	$T_A = T_{MIN}$ to T_{MAX}	I			±0.5	LSB
Integral Linearity		I		±0.5	±1.0	LSB
Analog Outputs						
Output Full Scale Voltage		I	1.23	1.4	1.57	V
Compliance Voltage		I	0.5		1.4	V
Dynamic Performance						
Conversion Rate		I	27	30		MWPS
Propagation Delay		V		12		ns
Crosstalk		V		-47		dB
Digital Inputs and Timing						
Input Current, Logic High	V_{IH} = 5 V	I			5	µA
Logic Low	V_{IL} = 0 V	I	-5			µA
Set-Up Time, Data and Controls (t_S)		I	5			ns
Hold Time, Data and Controls (t_h)		I	10			ns
Clock Pulse Width (Low) (t_{PW0})		I	18.5			ns
Clock Pulse Width (High) (t_{PW1})		I	18.5			ns
Power Supply Requirements						
Supply Voltage		I	4.75		5.25	V
Supply Current		V		27		mA
Power Dissipation		V		135		mW

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests; therefore, $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

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INTERFACE CONSIDERATIONS

Figure 2 shows a typical interface circuit of the SPT5110 in normal circuit operation.

SUPPLY AND GROUND CONSIDERATIONS

SPT suggests that all power supply pins (AV_{DD}) be tied together and decoupled using a 0.1 µF ceramic capacitor in parallel with a 10 µF tantalum capacitor. These decoupling capacitors should be tied between the power supply line and ground.

INTERNAL REFERENCE VOLTAGE (V_{REF})

Voltage reference is internally generated. Connect a 0.1 µF bypass capacitor with the shortest possible lead length between V_{REF} and AV_{SS}.

FULL-SCALE ADJUST CONTROL (V_{CS})

Connect a 0.1 µF bypass capacitor with the shortest possible lead length between V_{CS} and AV_{SS}. A resistor connected between this pin and AV_{CC} controls the magnitude of the full-scale video signal.

The output full-scale voltage of the SPT5110 can be kept constant and stable by keeping the value of V_{CS} to ground constant. The full-scale voltage changes from 0.5 V to 1.5 V according to V_{CS} changing from approximately 1.0 to 1.4 V.

CURRENT OUTPUTS

Each red, green and blue current output should have a load resistor connected to AV_{DD}. The resistors are typically 240 Ω and should be kept in the 150 Ω to 250 Ω range.

Table 1 - Binary Code Table
1 LSB = 5.49 mV

Step	Digital Input A7 (MSB)	A6	A5	A4	A3	A2	A1	A0 (LSB)	Analog Out (V)
0	0	0	0	0	0	0	0	0	3.6000
1	0	0	0	0	0	0	0	1	3.6055
2	0	0	0	0	0	0	1	0	3.6110
3	0	0	0	0	0	0	1	1	3.6165
.				.					.
.				.					.
.				.					.
254	1	1	1	1	1	1	1	0	4.9890
255	1	1	1	1	1	1	1	1	4.9945

Figure 1 - Typical Interface Circuit

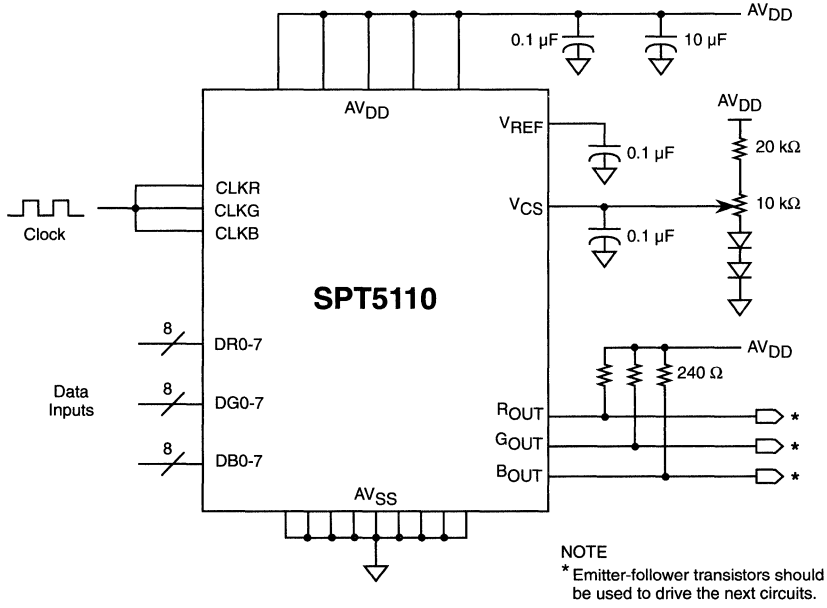


Figure 2 - Typical Performance Characteristics

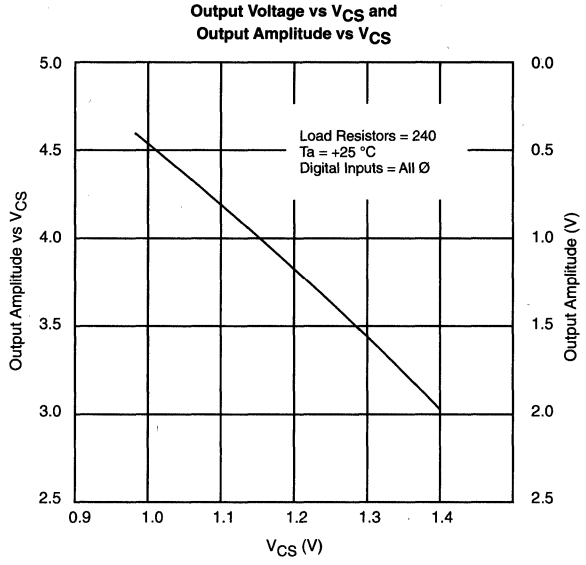
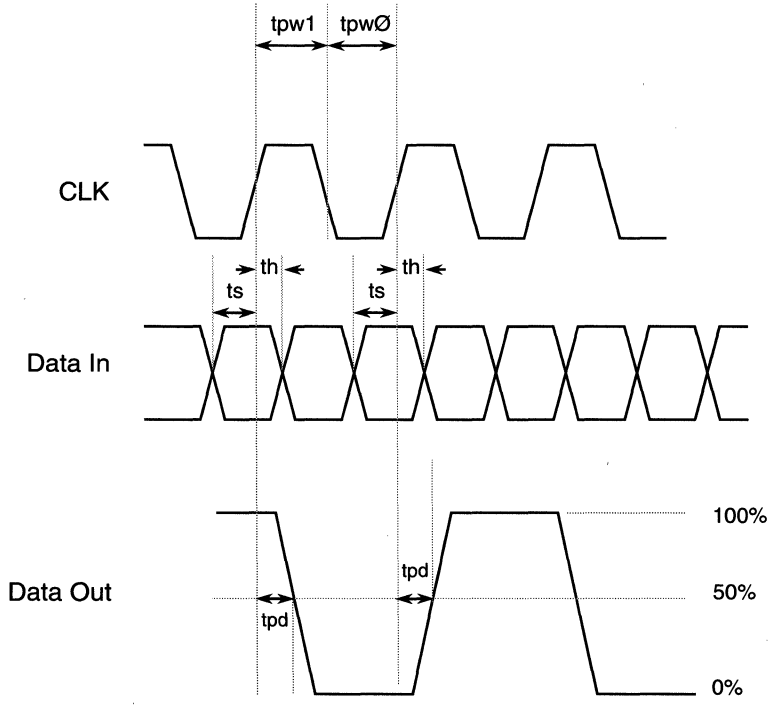


Figure 3 - Timing Diagram



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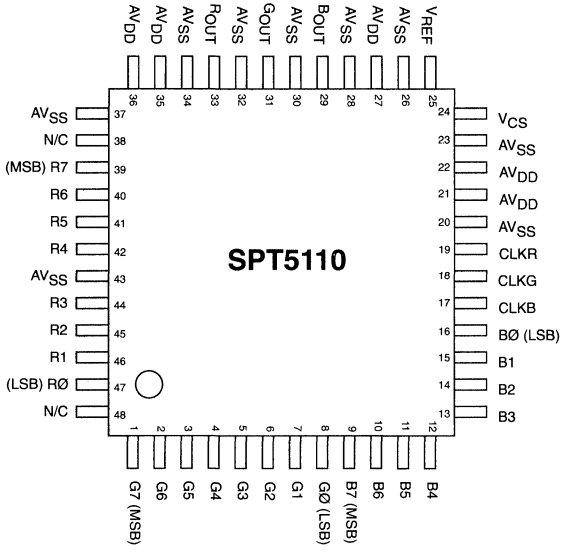
PIN ASSIGNMENTS



PIN FUNCTIONS

NAME	FUNCTION
R_{OUT}	Red Analog Current Output
G_{OUT}	Green Analog Current Output
B_{OUT}	Blue Analog Current Output
R7 - R0	Red Data Inputs
G7 - G0	Green Data Inputs
B7 - B0	Blue Data Inputs
CLKR	Red Clock Input
CLKG	Green Clock Input
CLKB	Blue Clock Input
V_{REF}	Voltage Reference (A 0.1 µF ceramic capacitor should be used.)
V_{CS}	Full-Scale Adjust Control Voltage 1 to 1.4 V.
AV_{SS}	Ground
AV_{DD}	Analog Power
N/C	No Connection

LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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SIGNAL PROCESSING TECHNOLOGIES

SPT1018

8-BIT, HIGH SPEED D/A CONVERTER

FEATURES

- 275 MWPS Conversion Rate - Version A
- 165 MWPS Conversion Rate - Version B
- Compatible with TDC1018 and HDAC10180 with Improved Performance
- RS-343-A Compatible
- Complete Video Controls: Sync, Blank, Bright and Reference White (Force High)
- 10KH, 100K ECL Compatible
- Single Power Supply
- Registered Data and Video Controls
- Differential Current Outputs
- ESD Protected Data and Control Inputs

APPLICATIONS

- High Resolution Color or Monochrome Raster Graphics Displays
- Medical Electronics: CAT, PET, MR Imaging Displays
- CAD/CAE Workstations
- Solids Modeling
- General Purpose High-Speed D/A Conversion
- Digital Synthesizers
- Automated Test Equipment
- Digital Transmitters/Modulators

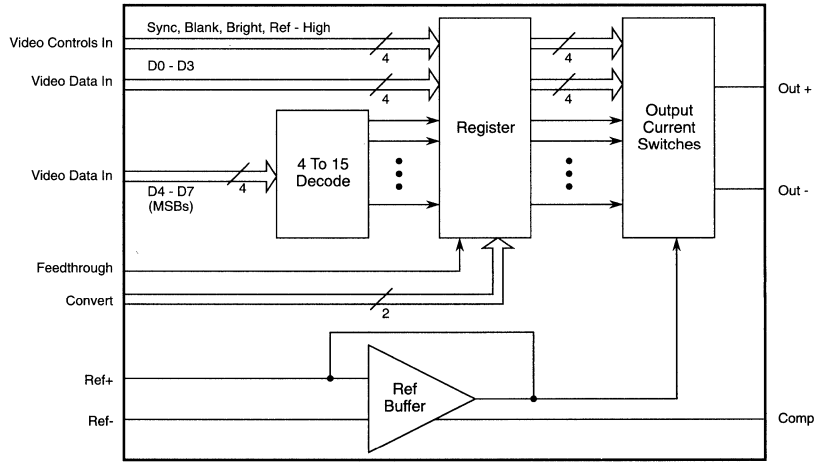
4

GENERAL DESCRIPTION

The SPT1018 is a monolithic 8-bit digital-to-analog converter capable of accepting video data at a 165 or 275 MWPS rate. Complete with video controls (Sync, Blank, Reference White [Force High], Bright), the SPT1018 directly drives doubly-terminated 50 or 75 ohm loads to standard composite video levels. The standard set-up level is 7.5 IRE. The SPT1018 is pin-compatible with the HDAC10180 and the TDC1018, with improved performance. The SPT1018 contains data and control input registers, video control logic, reference buffer, and current switches.

The SPT1018 is available in a 24-lead PDIP package in the industrial temperature range of -25 to +85 °C. Contact the factory for military temperature and /883 versions.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING (Beyond which damage may occur)[1]

Supply Voltages
- V_{EED} (measured to V_{CCD}) ..... -7.0 to 0.5 V
- V_{EEA} (measured to V_{CCA}) ..... -7.0 to 0.5 V
- V_{CCA} (measured to V_{CCD}) ..... -0.5 to 0.5 V

Input Voltages
- CONV, Data, and Controls ..... V_{EED} to 0.5 V (measured to V_{CCD})

Input Voltages
- Ref+ (measured to V_{CCA}) ..... V_{EEA} to 0.5 V
- Ref- (measured to V_{CCA}) ..... V_{EEA} to 0.5 V

Temperature
- Operating, ambient ..... -25 to + 85 °C
- junction ..... + 175 °C
- Lead, Soldering (10 seconds) ..... + 300 °C
- Storage ..... -60 to + 150 °C

Note: 1. Operation at any Absolute Maximum Ratings is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

V_{CCD} = V_{CCA} =ground, V_{EEA} = V_{EED} = -5.2 V ±0.3 V, T_A =T_{MIN} to T_{MAX}, C_C = 0 pF, I_{Set} = 1.105 mA

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS						
Integral Linearity Error	1.0 mA<I_{Set}<1.3 mA	VI	-.37 -.95		+.37 +.95	% Full Scale LSB
Differential Linearity Error	1.0 mA<I_{Set}<1.3 mA	VI	-0.2 -0.5		+0.2 +0.5	% Full Scale LSB
Gain Error		VI	-6.5		+6.5	% Full Scale
Gain Error Tempco		V		150		PPM/°C
Input Capacitance, REF +, REF -		V		5		pF
Compliance Voltage, + Output		VI	-1.2		1.5	V
Compliance Voltage, - Output		VI	-1.2		1.5	V
Equivalent Output Resistance		VI	20			kΩ
Output Capacitance		V		12		pF
Maximum Current, + Output		IV	45			mA
Maximum Current, - Output		IV	45			mA
Output Offset Current		VI		0.05	0.5	LSB
Input Voltage, Logic HIGH		VI	-1.0			V
Input Voltage, Logic LOW		VI			-1.5	V
Convert Voltage, Common Mode Range		IV	-0.5		-2.5	V
Convert Voltage, Differential		IV	0.4		1.2	V
Input Current, Logic LOW, Data and Controls		VI		35	120	µA
Input Current, Logic HIGH, Data and Controls		VI		40	120	µA
Input Current, Convert		VI		2	60	µA

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ELECTRICAL SPECIFICATIONS

V_{CCD} = V_{CCA} =ground, V_{EEA} = V_{EED} = -5.2 V ±0.3 V, T_A =T_{MIN} to T_{MAX}, C_C = 0 pF, I_{Set} = 1.105 mA

PARAMETERS	TEST CONDITIONS	LEVEL	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS						
Input Capacitance, Data and Controls		V		3.0		pF
Power Supply Sensitivity		VI	-120	20	+120	µA/V
Supply Current		VI		155	220	mA
DYNAMIC CHARACTERISTICS (R_L = 37.5 ohms, C_L = 5 pF, T_A = 25 °C, I_{Set} = 1.105 mA)						
Maximum Conversion Rate	B Grade	III	165			MWPS
	A Grade	III	275			MWPS
Rise Time	10% to 90% G.S.	III			1.6	ns
	$T_A = T_{MIN}$ to T_{MAX}	IV			2.0	ns
Rise Time	10% to 90% G.S. R_L = 25 ohms	V		1.0		ns
Current Settling Time, Clocked Mode	To 0.2% G.S.	V		7.0		ns
Current Settling Time, Clocked Mode	To 0.8% G.S.	V		5.5		ns
Current Settling Time, Clocked Mode t_{SI}	To 0.2% G.S. R_L = 25 Ω	V		4.5		ns
Clock to Output Delay, Clocked Mode		III		2.2	4.0	ns
t_{DSC}	$T_A = T_{MIN}$ to T_{MAX}	IV			4.5	ns
Data to Output Delay, Transparent Mode t_{DST}		III		3.2	6.0	ns
	$T_A = T_{MIN}$ to T_{MAX}	IV			6.0	ns
Convert Pulse Width, (LOW or HIGH)	B Grade	III	3.0			ns
t_{PWL}, t_{PWH}	A Grade	III	1.8			ns
Glitch Energy	Area = 1/2 VT	V		4		pV-s
Reference Bandwidth, -3 dB		V		1.0		MHz
Set-up Time, Data and Controls		III	1.0			ns
t_S	$T_A = T_{MIN}$ to T_{MAX}	IV	1.0			ns
Hold Time, Data and Controls		III	0.5			ns
t_H	$T_A = T_{MIN}$ to T_{MAX}	IV	0.5			ns
Slew Rate	20% to 80% G.S.	III	390			V/µS
	$T_A = T_{MIN}$ to T_{MAX}	IV	325			V/µS
Clock Feedthrough		III			-48	dB
	$T_A = T_{MIN}$ to T_{MAX}	IV			-48	dB

TEST LEVEL CODES

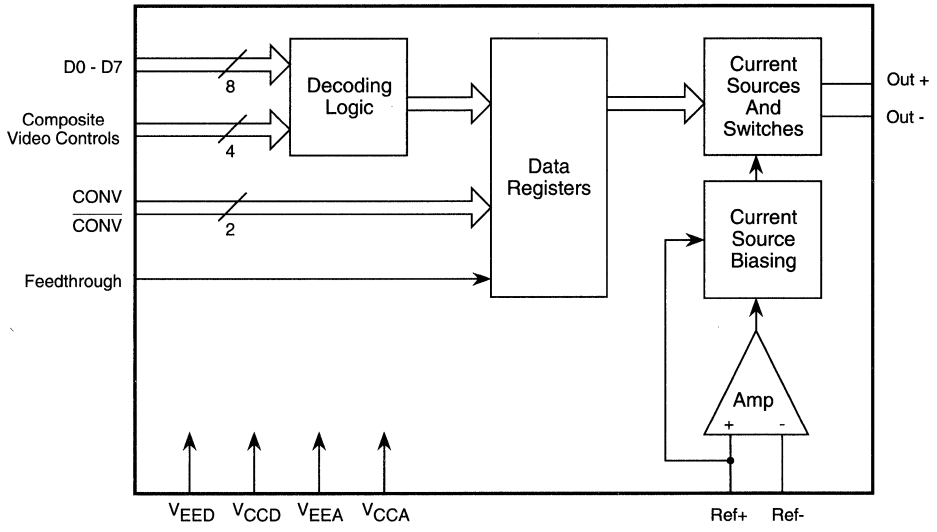
All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests; therefore, $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

Figure 1 - Functional Diagram



APPLICATION INFORMATION

The SPT1018 is a high speed video digital-to-analog converter capable of conversion rates of up to 275 MWPS. This makes the device suitable for driving 1500 X 1800 pixel displays at 70 to 90 Hz update rates.

The SPT1018 is separated into different conversion rate categories as shown in table I.

The SPT1018 has 10 KH and 100K ECL logic level compatible video controls and data inputs. The complementary analog output currents produced by the devices are proportional to the product of the digital control and data inputs in conjunction with the analog reference current. The SPT1018 is segmented so that the four MSBs of the input data are separated into a parallel thermometer code. From here, fifteen identical current sinks are driven to fabricate sixteen coarse output levels. The remaining four LSBs drive four binary weighted current switches.

The MSB currents are then summed with the LSBs, which provide a one-sixteenth of full scale contribution, to provide the 256 distinct analog output levels.

The video control inputs drive weighted current sinks that are added to the output current to produce composite video output levels. These controls, Sync, Blank, Reference White (Force High), and Bright are needed in video applications.

Another feature that similar video D/A converters do not have is the Feedthrough Control. This pin allows registered or unregistered operation of the video control and data inputs. In the registered mode, the composite functions are latched to the pixel data to prevent screen-edge distortions generally found on unregistered video DACs.

Table I - The SPT1018 Family and Speed Designations

PART NUMBER	UPDATE	COMMENTS
SPT1018A	275 MWPS	Suitable for 1200 X 1500 to 1500 X 1800 displays at 60 to 90 Hz update rate.
SPT1018B	165 MWPS	Suitable for 1024 X 1280 to 1200 X 1500 displays at 60 to 90 Hz update rate.

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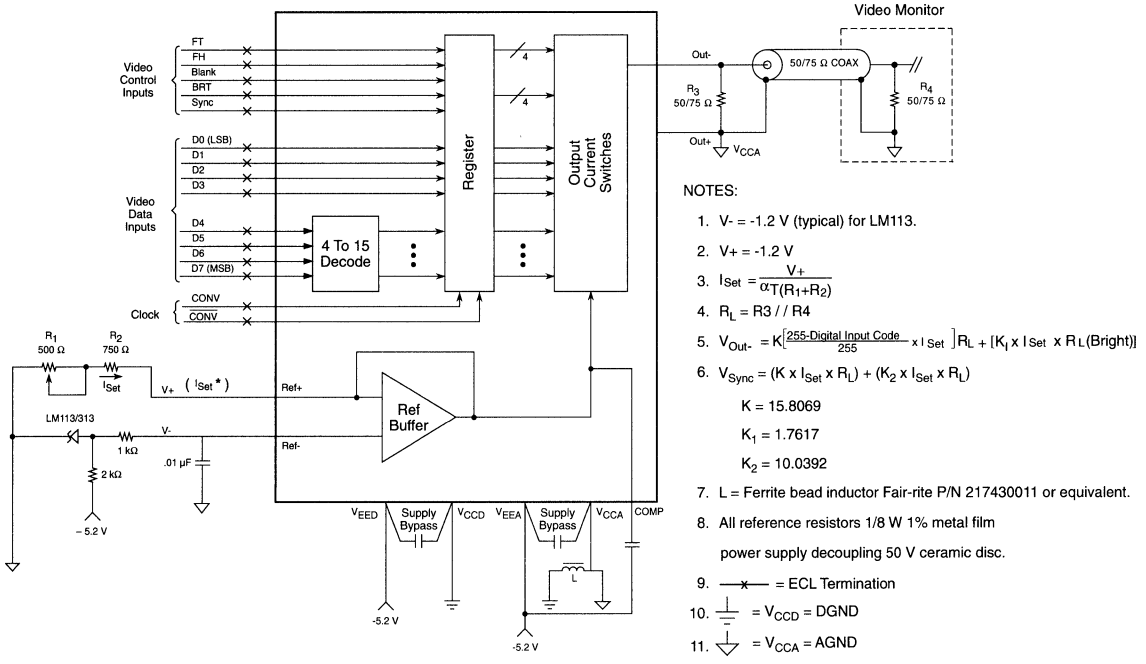
Figure 2 - Typical Interface Circuit



NOTES:

1. V- = -1.2 V (typical) for LM113.
2. V+ = -1.2 V
3. $I_{Set} = \frac{V+}{\alpha T(R_1+R_2)}$
4. R_L = R3 / / R4
5. $V_{Out-} = K\left[\frac{255\text{-Digital Input Code}}{255} \times I_{Set}\right] R_L + [K_1 \times I_{Set} \times R_L(\text{Bright})]$
6. $V_{Sync} = (K \times I_{Set} \times R_L) + (K_2 \times I_{Set} \times R_L)$

   K = 15.8069

   K_1 = 1.7617

   K_2 = 10.0392
7. L = Ferrite bead inductor Fair-rite P/N 217430011 or equivalent.
8. All reference resistors 1/8 W 1% metal film

   power supply decoupling 50 V ceramic disc.
9. —x— = ECL Termination
10. ⏚ = V_{CCD} = DGND
11. ⏚ = V_{CCA} = AGND
12. See figure 8 for detail on Ref Buffer.

TYPICAL INTERFACE CIRCUIT

GENERAL

A typical interface circuit using the SPT1018 in a color raster application is shown in figure 2. The SPT1018 requires few external components and is extremely easy to use. The very high operating speeds of the SPT1018 require good circuit layout, decoupling of supplies, and proper design of transmission lines. The following considerations should be noted to achieve best performance.

INPUT CONSIDERATIONS

Video input data and controls may be directly connected to the SPT1018. Note that all ECL inputs are terminated as closely to the device as possible to reduce ringing, crosstalk and reflections. A convenient and commonly used microstrip impedance is about 130 ohms, which is easily terminated using a 330 ohm resistor to V_{EE} and a 220 ohm resistor to Ground. This arrangement gives a Thevenin equivalent termination of 130 ohms to -2 volts without the need for a -2 volt supply. Standard SIP (Single Inline Package) 220/330 resistor networks are available for this purpose.

It is recommended that stripline or microstrip techniques be used for all ECL interface. Printed circuit wiring of known impedance over a solid ground plane is recommended. The ground plane should be constructed such that analog and digital ground currents are isolated as much as possible. The SPT1018 provides separate digital and analog ground connections to simplify ground layout.

OUTPUT CONSIDERATIONS

The analog outputs are designed to directly drive a dual 50 or 75 ohm load transmission system as shown. The source impedances of the SPT1018 outputs are high impedance current sinks. The load impedance (R_L) must be 25 or 37.5 ohms to attain standard RS-343-A video levels. Any deviation from this impedance will affect the resulting video output levels proportionally. As with the data interface, it is important that the analog transmission lines have matched impedance throughout, including connectors and transitions between printed wiring and coaxial cable. The combination of matched source termination resistor R_S and load terminator R_L minimizes reflections of both forward and reverse traveling waves in the analog transmission system. The return path for analog output current is V_{CCA} which is connected to the source termination resistor R_S.

POWER CONSIDERATIONS

The SPT1018 operates from a single standard -5.2 volt supply. Proper bypassing of the supplies will augment the SPT1018's inherent supply noise rejection characteristics. As shown in figure 2, a large tantalum capacitor in parallel with smaller ceramic capacitors is recommended for best performance. The small-valued capacitors should be connected as closely to the device package as possible, whereas the tantalum capacitor may be placed up to a few inches away.

The SPT1018 operates with separate analog (V_{EEA}) and digital (V_{EED}) power supplies to establish high noise immunity. Both supplies should eventually be connected to the same power source, but they should be individually decoupled as mentioned previously. The digital supply has a separate ground return which is V_{CCD}. The analog ground return is V_{CCA}. All power and ground pins must be connected in any application. If a +5 V power source is required, the ground pins V_{CCD} and V_{CCA} become the positive supply pins while V_{EED} and V_{EEA} become the ground returns. The relative polarities of the other voltages on inputs and outputs must be maintained.

REFERENCE CONSIDERATIONS

The SPT1018 has two reference inputs: Ref+ and Ref-. These pins are connected to the inverting and noninverting inputs of an internal amplifier that serves as a reference buffer amplifier.

The output of the buffer amplifier is the reference for the current sinks. The amplifier feedback loop is connected around one of the current sinks to achieve better accuracy. (See figure 8.)

Since the analog output currents are proportional to the digital input data and the reference current (I_{Set}), the full-scale output may be adjusted by varying the reference current. I_{Set} is controlled through the Ref+ input on the SPT1018. A method and equations to set I_{Set} is shown in figure 2. The SPT1018 uses an external negative voltage reference. The external reference must be stable to achieve a satisfactory output and the Ref- pin should be driven through a resistor to minimize offsets caused by bias current. The value for I_{Set} can be varied with the 500 ohm trimmer to change the full scale output. A double 50 ohm load (25 ohm) can be driven if I_{Set} is increased 50% more than I_{Set} for doubly terminated 75 ohm video applications.

COMPENSATION

The SPT1018 provides an external compensation input (COMP) for the reference buffer amplifier. In order to use this pin correctly, a capacitor should be connected between COMP and V_{EEA} as shown in figure 2. Keep the lead lengths as short as possible. If the reference is to be kept as a constant, use a large capacitor (.01 µF). The value of the capacitor determines the bandwidth of the amplifier. If modulation of the reference is required, smaller values of capacitance can be used to achieve up to a 1 MHz bandwidth.

DATA INPUTS AND VIDEO CONTROLS

The SPT1018 has standard single-ended data inputs. The inputs are registered to produce the lowest differential data propagation delay (skew) to minimize glitching. There are also four video control inputs to generate composite video outputs. These are Sync, Blank, Bright and Reference White or Force High. Also provided is the Feedthrough control as

Figure 3 - Timing Diagram

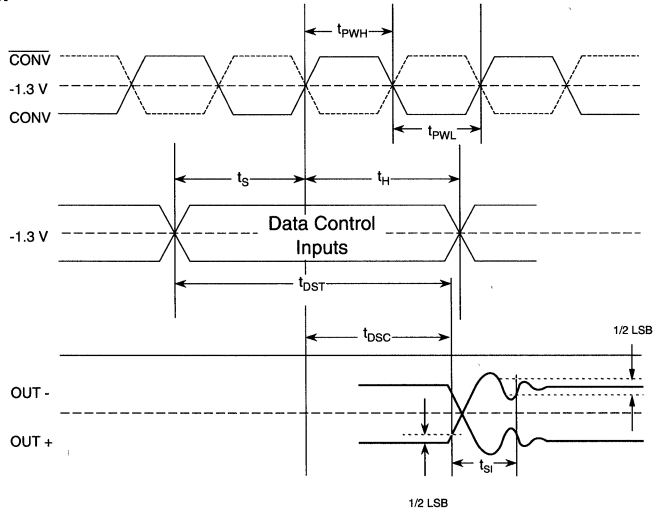


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Table II - Video Control Operation (Output values for set-up = 10 IRE and 75 ohm standard load)

Sync	Blank	Ref White	Bright	Data Input	Out - (mA)	Out - (V)	Out - (IRE)	Description
1	X	X	X	X	28.57	-1.071	-40	Sync Level
0	1	X	X	X	20.83	-0.781	0	Blank Level
0	0	1	1	X	0.00	0.000	110	Enhanced High Level
0	0	1	0	X	1.95	-0.073	100	Normal High Level
0	0	0	0	000...	19.40	-0.728	7.5	Normal Low Level
0	0	0	0	111...	1.95	-0.073	100	Normal High Level
0	0	0	1	000...	17.44	-0.654	17.5	Enhanced Low Level
0	0	0	1	111...	0.00	0.000	110	Enhanced High Level

mentioned earlier. The controls and data inputs are all 10 KH and 100K ECL compatible. In addition, all have internal pulldown resistors to leave them at a logic low so the pins are inactive when not used. This is useful if the devices are applied as standard DACs without the need for video controls or if less than eight bits are used.

The SPT1018 is usually configured in the synchronous mode. In this mode, the controls and data are synchronized to prevent pixel dropout. This reduces screen-edge distortions and provides the lowest output noise while maintaining the highest conversion rate. By leaving the Feedthrough (FT) control open (low), each rising edge of the convert (CONV) clock latches decoded data and control values into a D-type internal register. The registered data is then converted into the appropriate analog output by the switched current sinks. When FT is tied high, the control inputs and data are not registered. The analog output asynchronously tracks the input data and video controls. Feedthrough itself is asynchronous and usually used as a DC control.

The controls and data have to be present at the input pins for a set-up time of t_S before, and a hold time of t_h after, the rising edge of the clock (CONV) in order to be synchronously registered. The set-up and hold times are not important in the asynchronous mode. The minimum pulse widths high (t_{PWH}) and low (t_{PWL}) as well as settling time become the limiting factors. (See figure 3.)

The video controls produce the output levels needed for horizontal blanking, frame synchronization, etc., to be compatible with video system standards as described in RS-343-A. Table II shows the video control effects on the analog output. Internal logic governs Blank, Sync, and Force High so that they override the data inputs as needed in video applications. Sync overrides both the data and other controls to produce full negative video output (figure 9).

Reference White video level output is provided by Force High, which drives the internal digital data to full scale output or 100 IRE units. Bright gives an additional 10% of full scale value to the output level. This function can be used in graphic displays for highlighting menus, cursors or warning messages. Again, if the devices are used in non-video applications, the video controls can be left open.

CONVERT CLOCK

For best performance, the clock should be ECL driven, differentially, by utilizing CONV and $\overline{\text{CONV}}$ (figure 4). By driving the clock this way, clock noise and power supply/output intermodulation will be minimized. The rising edge of the clock synchronizes the data and control inputs to the SPT1018. Since the actual switching threshold of $\overline{\text{CONV}}$ is determined by CONV, the clock can be driven single-ended by connecting a bias voltage to $\overline{\text{CONV}}$. The switching threshold of CONV is set by this bias voltage.

ANALOG OUTPUTS

The SPT1018 has two analog outputs that are high impedance, complementary current sinks. The outputs vary in proportion to the input data, controls and reference current values so that the full scale output can be changed by setting I_{Set} as mentioned earlier.

In video applications, the outputs can drive a doubly terminated 50 or 75 ohm load to standard video levels. In the standard configuration of figure 5, the output voltage is the product of the output current and load impedance and is between 0 and -1.07 V. The Out- output (figure 9) will provide a video output waveform with the Sync pulse bottom at the -1.07 V level. The Out+ is inverted with Sync up.

Figure 4 - CONVert, $\overline{\text{CONV}}$ert Switching Levels

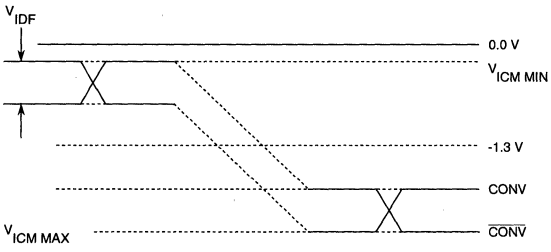


Figure 5A - Standard Load

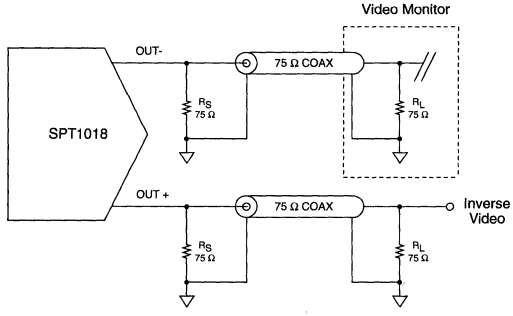
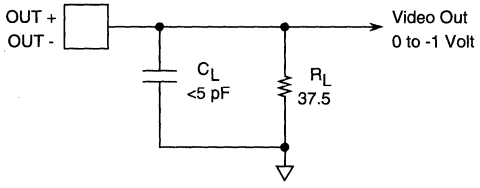


Figure 5B - Test Load



TYPICAL RGB GRAPHICS SYSTEM

In an RGB graphics system, the color displayed is determined by the combined intensities of the red, green and blue (RGB) D/A converter outputs. A change in gain or offset in any of the RGB outputs will affect the apparent hue displayed on the CRT screen.

Thus, it is very important that the outputs of the D/A converters track each other over a wide range of operating conditions. Since the D/A output is proportional to the product of the reference and digital input code, a common reference should be used to drive all three D/As in an RGB system to minimize RGB DAC-to-DAC mismatch and improve TC tracking.

The SPT1019 contains an internal precision bandgap reference which completely eliminates the need for an external reference. The reference can supply up to 50 µA to an external load, such as two other DAC reference inputs. (See the SPT1019 data sheet).

The circuits shown in figure 6 illustrate how a single SPT1019 may be used as a master reference in a system with multiple DACs (such as RGB). The other DACs are simply slaved from the SPT1019's reference output. The SPT1018s shown are especially well-suited to be slaved to a SPT1019 for a better TC tracking from DAC-to-DAC, since they are essentially SPT1019s without the reference. The SPT1018 is pin-compatible with the TDC1018, that does not have an internal reference. Although either the TDC1018 or the SPT1018 may be slaved from an SPT1019, the higher performance SPT1018 and the above mentioned DAC-to-DAC TC tracking is the best choice for new designs.

No external reference is required for operation of the SPT1019, as this function is provided internally. The internal reference is a bandgap type and is suitable for operation over extended temperature ranges. The SPT1018 must use an external reference.

Figure 6 - Typical RGB Graphics System

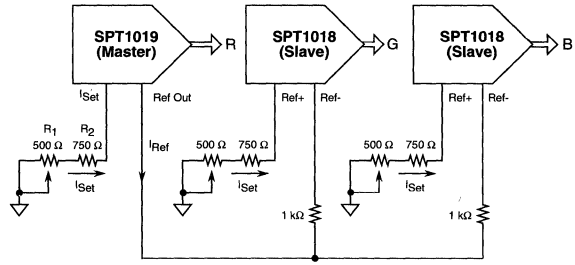
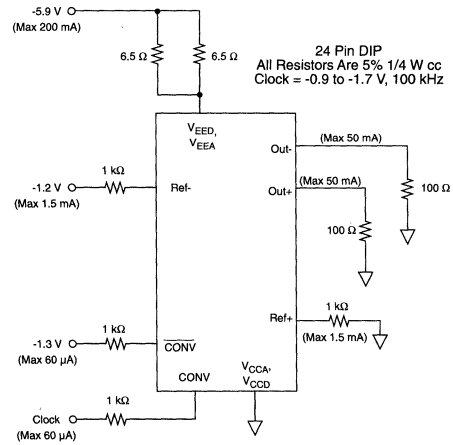


Figure 7 - Burn-In Circuit



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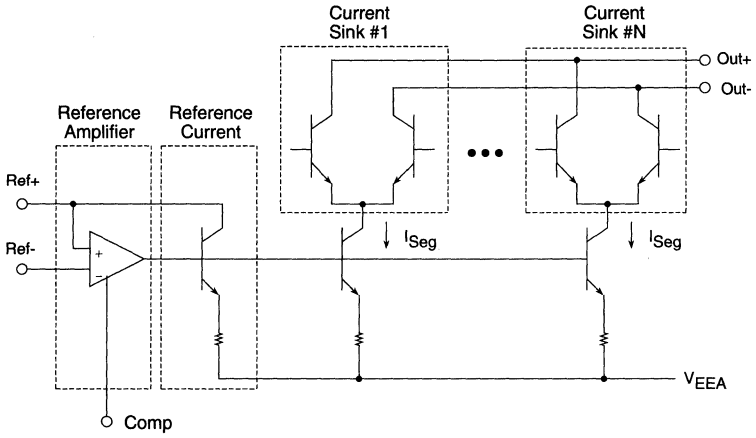


Figure 9 - Video Output Waveform for Standard Load

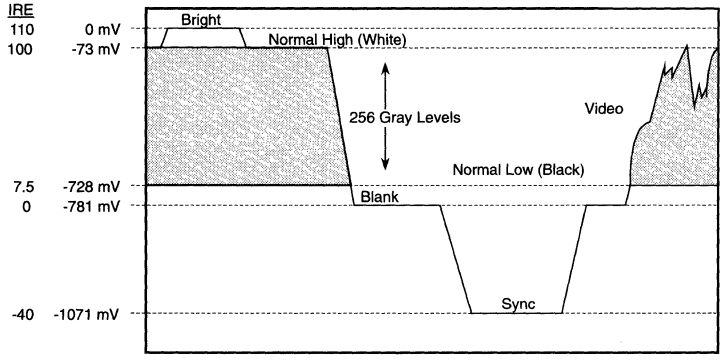
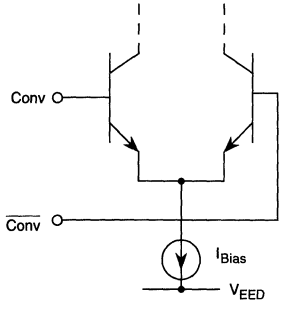
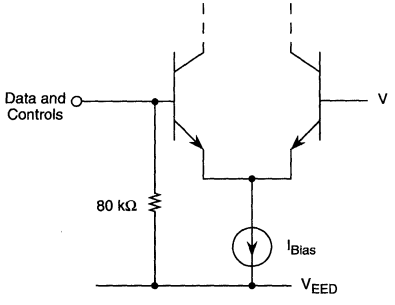
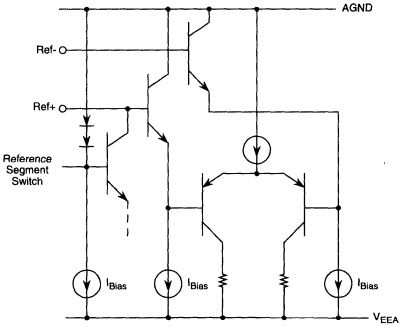


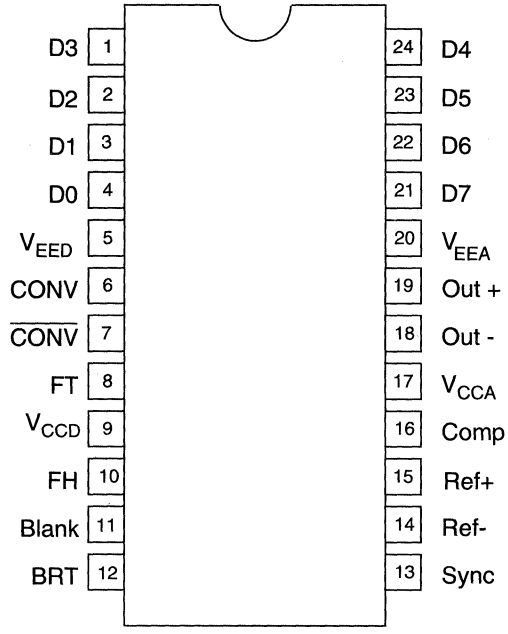
Figure 10 - Equivalent Input Circuits - Data, Clock, Controls and Reference







PIN ASSIGNMENTS



PIN FUNCTIONS

NAME	FUNCTION
D3	Data Bit 3
D2	Data Bit 2
D1	Data Bit 1
D0	Data Bit 0 (LSB)
V_{EED}	Digital Negative Supply
CONV	Convert Clock Input
$\overline{CONV}$	Convert Clock Input Complement
FT	Register Feedthrough Control
V_{CCD}	Digital Positive Supply
FH	Data Force High Control
Blank	Video Blank Input
BRT	Video Bright Input
Sync	Video Sync Input
Ref-	Reference Current - Input
Ref+	Reference Current + Input
COMP	Compensation Input
V_{CCA}	Analog Positive Supply
Out-	Output Current Negative
Out+	Output Current Positive
V_{EEA}	Analog Negative Supply
D7	Data Bit 7 (MSB)
D6	Data Bit 6
D5	Data Bit 5
D4	Data Bit 4

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LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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PH: (719) 528-2300; Fax: (719) 528-2370 SPT

SIGNAL PROCESSING TECHNOLOGIES

SPT1019

8-BIT, HIGH SPEED D/A CONVERTER

FEATURES

- 275 MWPS Conversion Rate - Version A
- 165 MWPS Conversion Rate - Version B
- Compatible with the HDAC10181 with Improved Performance
- RS-343-A Compatible
- Complete Video Controls: Sync, Blank, Bright and Reference White (Force High)
- 10KH, 100K ECL Compatible
- Single Power Supply
- Registered Data and Video Controls
- Differential Current Outputs
- Stable On-Chip Bandgap Reference
- ESD Protected Data and Control Inputs

APPLICATIONS

- High Resolution Color or Monochrome Raster Graphics Displays
- Medical Electronics: CAT, PET, MR Imaging Displays
- CAD/CAE Workstations
- Solids Modeling
- General Purpose High-Speed D/A Conversion
- Digital Synthesizers
- Automated Test Equipment
- Digital Transmitters/Modulators

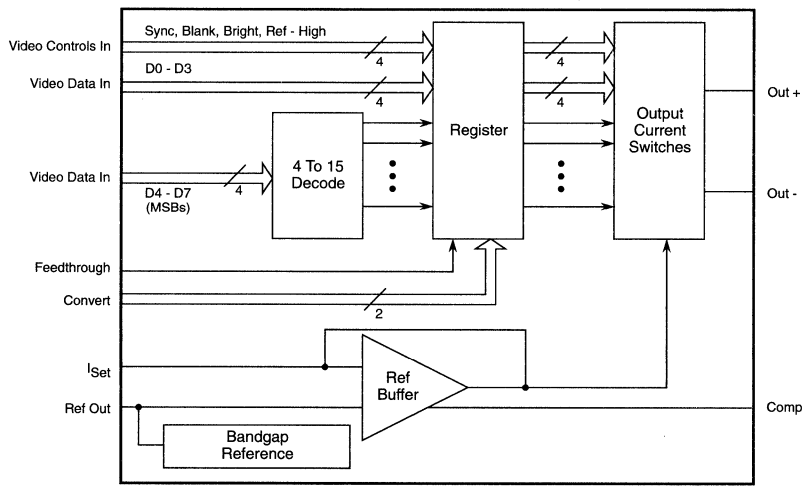
4

GENERAL DESCRIPTION

The SPT1019 is a monolithic 8-bit digital-to-analog converter capable of accepting video data at a 165 or 275 MWPS rate. Complete with video controls (Sync, Blank, Reference White [Force High], Bright), the SPT1019 directly drives doubly-terminated 50 or 75 ohm loads to standard composite video levels. The standard setup level is 7.5 IRE. The SPT1019 is pin-compatible with the HDAC10181 with improved performance. The SPT1019 contains data and control input registers, video control logic, reference buffer, and current switches.

The SPT1019 is available in a 24-lead PDIP package in the industrial temperature range of -25 to +85 °C. Contact the factory for military temperature and /883 versions.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING (Beyond which damage may occur)[1]

Supply Voltages

V_{EED} (measured to V_{CCD}) ..... -7.0 to 0.5 V
V_{EEA} (measured to V_{CCA}) ..... -7.0 to 0.5 V
V_{CCA} (measured to V_{CCD}) ..... -0.5 to 0.5 V

Input Voltages

CONV, Data, and Controls ..... V_{EED} to 0.5 V
(measured to V_{CCD})

Input Voltages

Ref+ (measured to V_{CCA}) ..... V_{EEA} to 0.5 V
Ref- (measured to V_{CCA}) ..... V_{EEA} to 0.5 V

Temperature

Operating, ambient ..... -25 to + 85 °C
junction ..... + 175 °C
Lead, Soldering (10 seconds) ..... + 300 °C
Storage ..... -60 to + 150 °C

Note: 1. Operation at any Absolute Maximum Ratings is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

V_{CCD} = V_{CCA} =ground, V_{EEA} = V_{EED} = -5.2 V ±0.3 V, T_A =T_{MIN} to T_{MAX}, C_C = 0 pF, I_{Set} = 1.105 mA

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTISTICS						
Integral Linearity Error	1.0 mA<I_{Set}<1.3 mA	VI	-.37 -.95		+.37 +.95	% Full Scale LSB
Differential Linearity Error	1.0 mA<I_{Set}<1.3 mA	VI	-0.2 -0.5		+0.2 +0.5	% Full Scale LSB
Gain Error		VI	-19		+19	% Full Scale
Gain Error Tempco		V		150		PPM/°C
Input Capacitance, Ref Out, I_{Set}		V		5		pF
Compliance Voltage, + Output		VI	-1.2		1.5	V
Compliance Voltage, - Output		VI	-1.2		1.5	V
Equivalent Output Resistance		VI	20			kΩ
Output Capacitance		V		12		pF
Maximum Current, + Output		IV	45			mA
Maximum Current, - Output		IV	45			mA
Output Offset Current		VI		0.05	0.5	LSB
Input Voltage, Logic HIGH		VI	-1.0			V
Input Voltage, Logic LOW		VI			-1.5	V
Convert Voltage, Common Mode Range		IV	-0.5		-2.5	V
Convert Voltage, Differential		IV	0.4		1.2	V
Input Current, Logic LOW, Data and Controls		VI		35	120	µA
Input Current, Logic HIGH, Data and Controls		VI		40	120	µA
Input Current, Convert		VI		2	60	µA
Bandgap Tempco		V		100		PPM/°C

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ELECTRICAL SPECIFICATIONS

V_{CCD} = V_{CCA} =ground, V_{EEA} = V_{EED} = -5.2 V ±0.3 V, T_A =T_{MIN} to T_{MAX}, C_C = 0 pF, I_{Set} = 1.105 mA

PARAMETERS	TEST CONDITIONS	LEVEL	MIN	TYP	MAX	UNITS
Reference Voltage Measured to V_{CCA}		VI	1.3	-1.2	1.0	V
Input Capacitance, Data and Controls		V		3.0		pF
Power Supply Sensitivity		VI	-120	20	+120	µA/V
Supply Current		VI		155	220	mA
DYNAMIC CHARACTERISTICS (R_L = 37.5 ohms, C_L = 5 pF, T_A = 25 °C, I_{Set} = 1.105 mA)						
Maximum Conversion Rate	B Grade	III	165			MWPS
	A Grade	III	275			MWPS
Rise Time	10% to 90% G.S.	III			1.6	ns
	T_A = T_{MIN} to T_{MAX}	IV			2.0	ns
Rise Time	10% to 90% G.S. R_L = 25 ohms	V		1.0		ns
Current Settling Time, Clocked Mode	To 0.2% G.S.	V		7.0		ns
Current Settling Time, Clocked Mode	To 0.8% G.S.	V		5.5		ns
Current Settling Time, Clocked Mode t_{SI}	To 0.2% G.S. R_L = 25 Ω	V		4.5		ns
Clock to Output Delay, Clocked Mode		III		2.2	4.0	ns
t_{DSC}	T_A = T_{MIN} to T_{MAX}	IV			4.5	ns
Data to Output Delay, Transparent Mode t_{DST}		III		3.2	6.0	ns
		IV			6.0	ns
Convert Pulse Width, (LOW or HIGH)	B Grade	III	3.0			ns
t_{PWL}, t_{PWH}	A Grade	III	1.8			ns
Glitch Energy	Area = 1/2 VT	V		4		pV-s
Reference Bandwidth, -3 dB		V		1.0		MHz
Setup Time, Data and Controls		III	1.0			ns
t_S	T_A = T_{MIN} to T_{MAX}	IV	1.0			ns
Hold Time, Data and Controls		III	0.5			ns
t_H	T_A = T_{MIN} to T_{MAX}	IV	0.5			ns
Slew Rate	20% to 80% G.S.	III	390			V/µS
	T_A = T_{MIN} to T_{MAX}	IV	325			V/µS
Clock Feedthrough		III			-48	dB
	T_A = T_{MIN} to T_{MAX}	IV			-48	dB

TEST LEVEL CODES

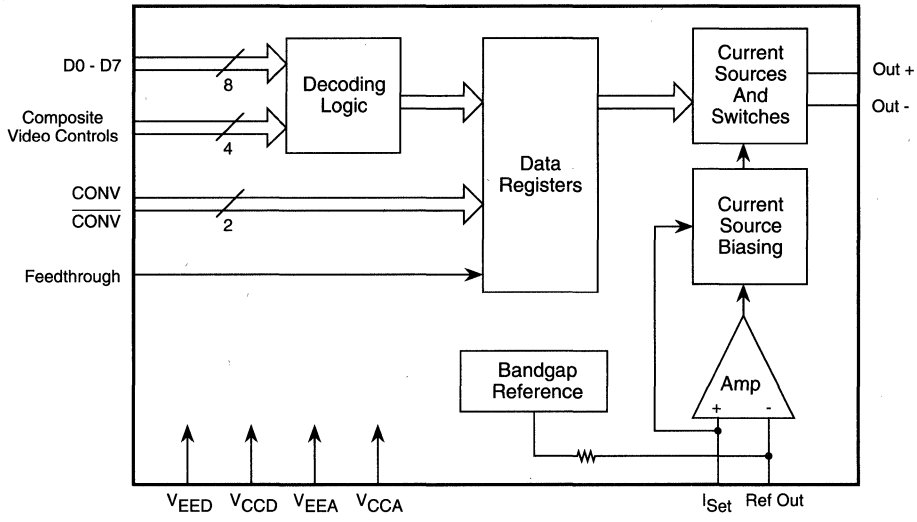
All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests; therefore, T_J = T_C = T_A.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

Figure 1 - Functional Diagram



APPLICATION INFORMATION

The SPT1019 is a high speed video digital-to-analog converter capable of conversion rates of up to 275 MWPS. This makes the device suitable for driving 1500 X 1800 pixel displays at 70 to 90 Hz update rates.

The SPT1019 is separated into different conversion rate categories as shown in table I.

The SPT1019 has 10 KH and 100K ECL logic level compatible video controls and data inputs. The complementary analog output currents produced by the devices are proportional to the product of the digital control and data inputs in conjunction with the analog reference current. The SPT1019 is segmented so that the four MSBs of the input data are separated into a parallel thermometer code. From here, fifteen identical current sinks are driven to fabricate sixteen coarse output levels. The remaining four LSBs drive four binary weighted current switches.

The MSB currents are then summed with the LSBs, which provide a one-sixteenth of full scale contribution, to provide the 256 distinct analog output levels.

The video control inputs drive weighted current sinks that are added to the output current to produce composite video output levels. These controls, Sync, Blank, Reference White (Force High), and Bright are needed in video applications.

Another feature that similar video D/A converters do not have is the Feedthrough Control. This pin allows registered or unregistered operation of the video control and data inputs. In the registered mode, the composite functions are latched to the pixel data to prevent screen-edge distortions generally found on unregistered video DACs.

Table I - The SPT1019 Family and Speed Designations

PART NUMBER	UPDATE	COMMENTS
SPT1019A	275 MWPS	Suitable for 1200 X 1500 to 1500 X 1800 displays at 60 to 90 Hz update rate.
SPT1019B	165 MWPS	Suitable for 1024 X 1280 to 1200 X 1500 displays at 60 to 90 Hz update rate.

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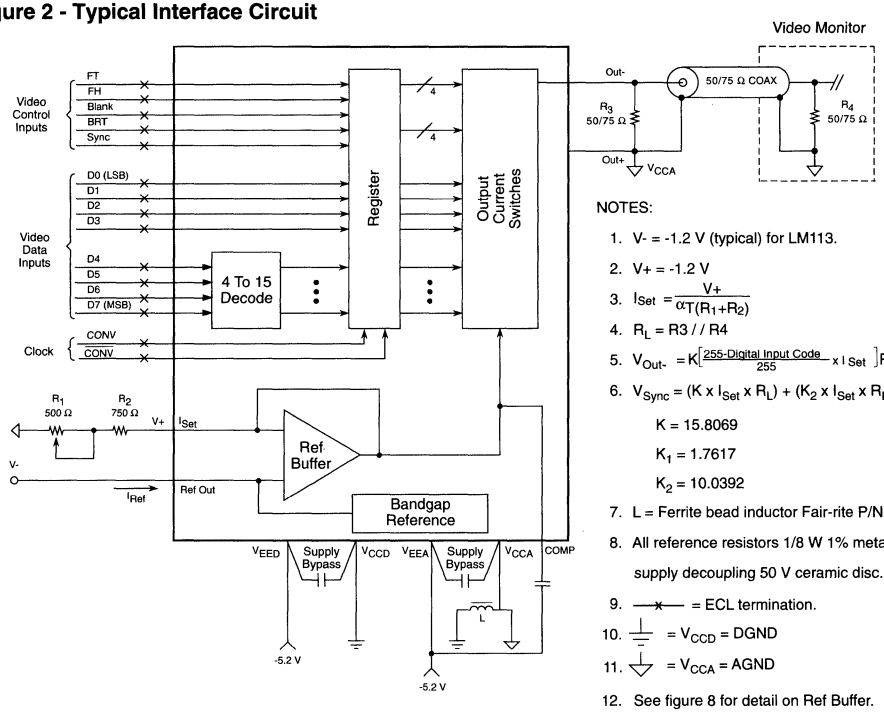
Figure 2 - Typical Interface Circuit



NOTES:

1. V- = -1.2 V (typical) for LM113.
2. V+ = -1.2 V
3. $I_{Set} = \frac{V+}{\alpha T(R_1+R_2)}$
4. R_L = R3 / / R4
5. $V_{Out-} = K\left[\frac{255\text{-Digital Input Code}}{255} \times I_{Set}\right] R_L + [K_1 \times I_{Set} \times R_{L(Bright)}]$
6. $V_{Sync} = (K \times I_{Set} \times R_L) + (K_2 \times I_{Set} \times R_L)$

   K = 15.8069

   K_1 = 1.7617

   K_2 = 10.0392
7. L = Ferrite bead inductor Fair-rite P/N 217430011 or equivalent.
8. All reference resistors 1/8 W 1% metal film power.

   supply decoupling 50 V ceramic disc.
9. —x— = ECL termination.
10. ⏚ = V_{CCD} = DGND
11. ⏚ = V_{CCA} = AGND
12. See figure 8 for detail on Ref Buffer.
13. Ref Out on the SPT1019 can be used to drive up to two SPT1018 reference inputs.

TYPICAL INTERFACE CIRCUIT

GENERAL

A typical interface circuit using the SPT1019 in a color raster application is shown in figure 2. The SPT1019 requires few external components and is extremely easy to use. The very high operating speeds of the SPT1019 require good circuit layout, decoupling of supplies, and proper design of transmission lines. The following considerations should be noted to achieve best performance.

INPUT CONSIDERATIONS

Video input data and controls may be directly connected to the SPT1019. Note that all ECL inputs are terminated as closely to the device as possible to reduce ringing, crosstalk and reflections. A convenient and commonly used microstrip impedance is about 130 ohms, which is easily terminated using a 330 ohm resistor to V_{EE} and a 220 ohm resistor to Ground. This arrangement gives a Thevenin equivalent termination of 130 ohms to -2 volts without the need for a -2 volt supply. Standard SIP (Single Inline Package) 220/330 resistor networks are available for this purpose.

It is recommended that stripline or microstrip techniques be used for all ECL interface. Printed circuit wiring of known impedance over a solid ground plane is recommended. The ground plane should be constructed such that analog and digital ground currents are isolated as much as possible. The SPT1019 provides separate digital and analog ground connections to simplify ground layout.

OUTPUT CONSIDERATIONS

The analog outputs are designed to directly drive a dual 50 or 75 ohm load transmission system as shown. The source impedances of the SPT1019 outputs are high impedance current sinks. The load impedance (R_L) must be 25 or 37.5 ohms to attain standard RS-343-A video levels. Any deviation from this impedance will affect the resulting video output levels proportionally. As with the data interface, it is important that the analog transmission lines have matched impedance throughout, including connectors and transitions between printed wiring and coaxial cable. The combination of matched source termination resistor R_S and load terminator R_L minimizes reflections of both forward and reverse traveling waves in the analog transmission system. The return path for analog output current is V_{CCA} which is connected to the source termination resistor R_S.

POWER CONSIDERATIONS

The SPT1019 operates from a single standard -5.2 volt supply. Proper bypassing of the supplies will augment the SPT1019's inherent supply noise rejection characteristics. As shown in figure 2, a large tantalum capacitor in parallel with smaller ceramic capacitors is recommended for best performance. The small-valued capacitors should be connected as closely to the device package as possible, whereas the tantalum capacitor may be placed up to a few inches away.

The SPT1019 operates with separate analog (V_{EEA}) and digital (V_{EED}) power supplies to establish high noise immunity. Both supplies should eventually be connected to the same power source, but they should be individually decoupled as mentioned previously. The digital supply has a separate ground return which is V_{CCD}. The analog ground return is V_{CCA}. All power and ground pins must be connected in any application. If a +5 V power source is required, the ground pins V_{CCD} and V_{CCA} become the positive supply pins while V_{EED} and V_{EEA} become the ground returns. The relative polarities of the other voltages on inputs and outputs must be maintained.

REFERENCE CONSIDERATIONS

The SPT1019 has one reference input (I_{Set}) and one reference output (Ref Out). These pins are connected to the inverting and noninverting inputs of an internal amplifier that serves as a reference buffer amplifier. The SPT1019 has a bandgap reference connected internally to the inverting input of the buffer amplifier and Ref Out.

The output of the buffer amplifier is the reference for the current sinks. The amplifier feedback loop is connected around one of the current sinks to achieve better accuracy. (See Figure 8.)

Since the analog output currents are proportional to the digital input data and the reference current (I_{Set}), the full-scale output may be adjusted by varying the reference current. I_{SET} is controlled through the I_{Set} input on the SPT1019. A method and equations to set I_{Set} is shown in Figure 2. The SPT1019 uses its own reference voltage for setting up I_{Set} as shown in Figure 2. The value for I_{Set} can be varied with the 500 Ohm trimmer to change the full scale output. A double 50 Ohm load (25 Ohm) can be driven if I_{Set} is increased 50% more than I_{Set} for doubly terminated 75 Ohm video applications.

COMPENSATION

The SPT1019 provides an external compensation input (COMP) for the reference buffer amplifier. In order to use this pin correctly, a capacitor should be connected between COMP and V_{EEA} as shown in figure 2. Keep the lead lengths as short as possible. If the reference is to be kept as a constant, use a large capacitor (.01 µF). The value of the capacitor determines the bandwidth of the amplifier. If modulation of the reference is required, smaller values of capacitance can be used to achieve up to a 1 MHz bandwidth.

Figure 3 - Timing Diagram

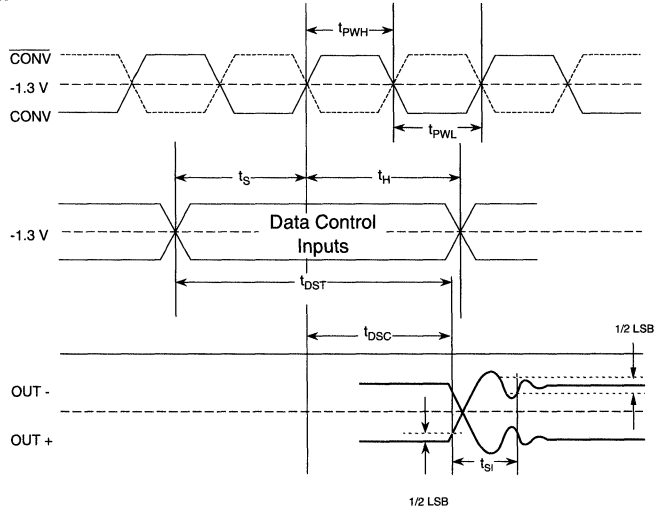


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Table II - Video Control Operation (Output values for setup = 10 IRE and 75 ohm standard load)

Sync	Blank	Ref White	Bright	Data Input	Out - (mA)	Out - (V)	Out - (IRE)	Description
1	X	X	X	X	28.57	-1.071	-40	Sync Level
0	1	X	X	X	20.83	-0.781	0	Blank Level
0	0	1	1	X	0.00	0.000	110	Enhanced High Level
0	0	1	0	X	1.95	-0.073	100	Normal High Level
0	0	0	0	000...	19.40	-0.728	7.5	Normal Low Level
0	0	0	0	111...	1.95	-0.073	100	Normal High Level
0	0	0	1	000...	17.44	-0.654	17.5	Enhanced Low Level
0	0	0	1	111...	0.00	0.000	110	Enhanced High Level

DATA INPUTS AND VIDEO CONTROLS

The SPT1019 has standard single-ended data inputs. The inputs are registered to produce the lowest differential data propagation delay (skew) to minimize glitching. There are also four video control inputs to generate composite video outputs. These are Sync, Blank, Bright and Reference White or Force High. Also provided is the Feedthrough control as mentioned earlier. The controls and data inputs are all 10 KH and 100K ECL compatible. In addition, all have internal pulldown resistors to leave them at a logic low so the pins are inactive when not used. This is useful if the devices are applied as standard DACs without the need for video controls or if less than eight bits are used.

The SPT1019 is usually configured in the synchronous mode. In this mode, the controls and data are synchronized to prevent pixel dropout. This reduces screen-edge distortions and provides the lowest output noise while maintaining the highest conversion rate. By leaving the Feedthrough (FT) control open (low), each rising edge of the convert (CONV) clock latches decoded data and control values into a D-type internal register. The registered data is then converted into the appropriate analog output by the switched current sinks. When FT is tied high, the control inputs and data are not registered. The analog output asynchronously tracks the input data and video controls. Feedthrough itself is asynchronous and usually used as a DC control.

The controls and data have to be present at the input pins for a setup time of t_s before, and a hold time of t_h after, the rising edge of the clock (CONV) in order to be synchronously registered. The setup and hold times are not important in the asynchronous mode. The minimum pulse widths high (t_{PWH}) and low (t_{PWL}) as well as settling time become the limiting factors. (See figure 3.)

The video controls produce the output levels needed for horizontal blanking, frame synchronization, etc., to be compatible with video system standards as described in RS-343-A. Table II shows the video control effects on the analog output. Internal logic governs Blank, Sync, and Force High so that they override the data inputs as needed in video applications. Sync overrides both the data and other controls to produce full negative video output (figure 9).

Reference White video level output is provided by Force High, which drives the internal digital data to full scale output or 100 IRE units. Bright gives an additional 10% of full scale value to the output level. This function can be used in graphic displays for highlighting menus, cursors or warning messages. Again, if the devices are used in non-video applications, the video controls can be left open.

CONVERT CLOCK

For best performance, the clock should be ECL driven, differentially, by utilizing CONV and $\overline{\text{CONV}}$ (figure 4). By driving the clock this way, clock noise and power supply/output intermodulation will be minimized. The rising edge of the clock synchronizes the data and control inputs to the SPT1019. Since the actual switching threshold of $\overline{\text{CONV}}$ is determined by CONV, the clock can be driven single-ended by connecting a bias voltage to $\overline{\text{CONV}}$. The switching threshold of CONV is set by this bias voltage.

ANALOG OUTPUTS

The SPT1019 has two analog outputs that are high impedance, complementary current sinks. The outputs vary in proportion to the input data, controls and reference current values so that the full scale output can be changed by setting I_{Set} as mentioned earlier.

In video applications, the outputs can drive a doubly terminated 50 or 75 ohm load to standard video levels. In the standard configuration of figure 5, the output voltage is the product of the output current and load impedance and is between 0 and -1.07 V. The Out- output (figure 9) will provide a video output waveform with the Sync pulse bottom at the -1.07 V level. The Out+ is inverted with Sync up.

Figure 4 - CONVert, $\overline{\text{CONV}}$ert Switching Levels

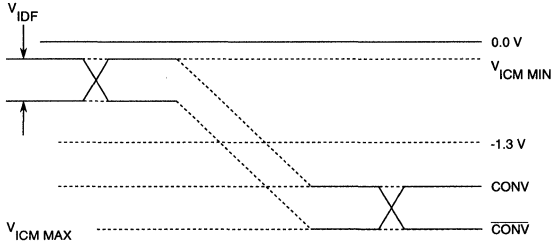


Figure 5A - Standard Load

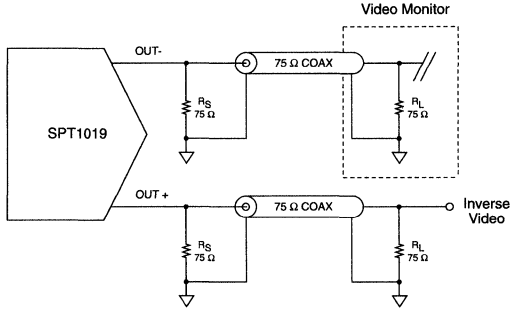
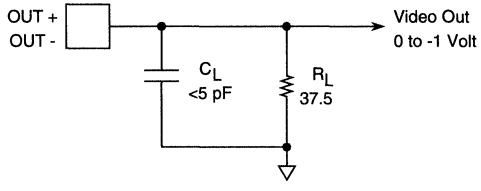


Figure 5B - Test Load



TYPICAL RGB GRAPHICS SYSTEM

In an RGB graphics system, the color displayed is determined by the combined intensities of the red, green and blue (RGB) D/A converter outputs. A change in gain or offset in any of the RGB outputs will affect the apparent hue displayed on the CRT screen.

Thus, it is very important that the outputs of the D/A converters track each other over a wide range of operating conditions. Since the D/A output is proportional to the product of the reference and digital input code, a common reference should be used to drive all three D/As in an RGB system to minimize RGB DAC-to-DAC mismatch and improve TC tracking.

The SPT1019 contains an internal precision bandgap reference which completely eliminates the need for an external reference. The reference can supply up to 50 μA to an external load, such as two other DAC reference inputs.

The circuits shown in figure 6 illustrate how a single SPT1019 may be used as a master reference in a system with multiple DACs (such as RGB). The other DACs are simply slaved from the SPT1019's reference output. The SPT1018s shown are especially well-suited to be slaved to a SPT1019 for a better TC tracking from DAC-to-DAC, since they are essentially SPT1019s without the reference. The SPT1018 is pin-compatible with the TDC1018, that does not have an internal reference. Although either the TDC1018 or the SPT1018 may be slaved from an SPT1019, the higher performance SPT1018 and the above mentioned DAC-to-DAC TC tracking is the best choice for new designs.

No external reference is required for operation of the SPT1019, as this function is provided internally. The internal reference is a bandgap type and is suitable for operation over extended temperature ranges. The SPT1018 must use an external reference.

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Figure 6 - Typical RGB Graphics System

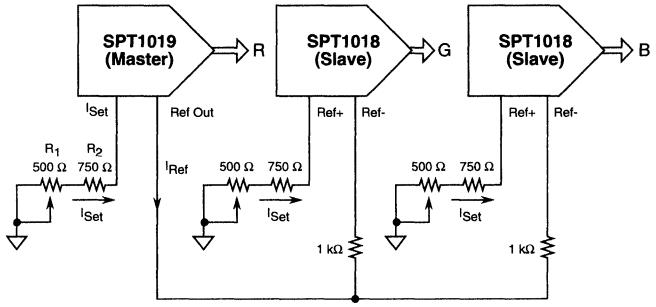


Figure 7 - Burn-In Circuit

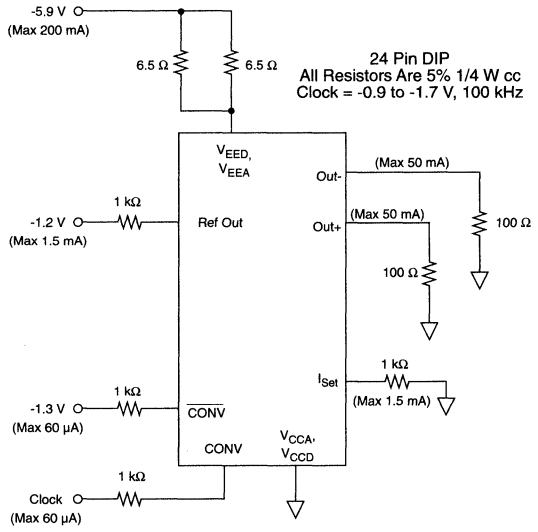


Figure 8 - DAC Output Circuit

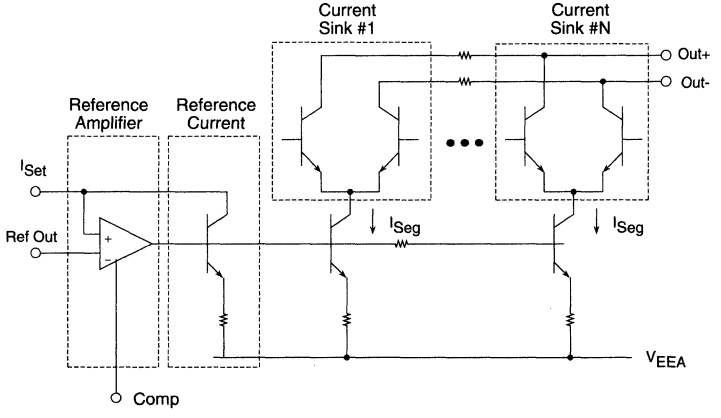


Figure 9 - Video Output Waveform for Standard Load

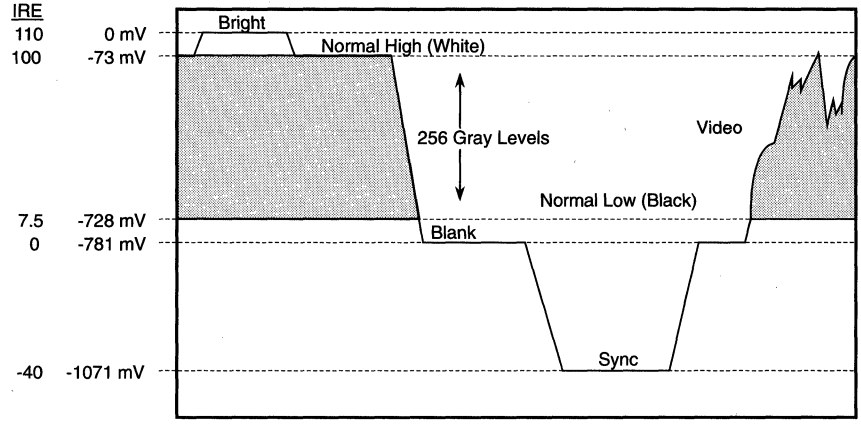
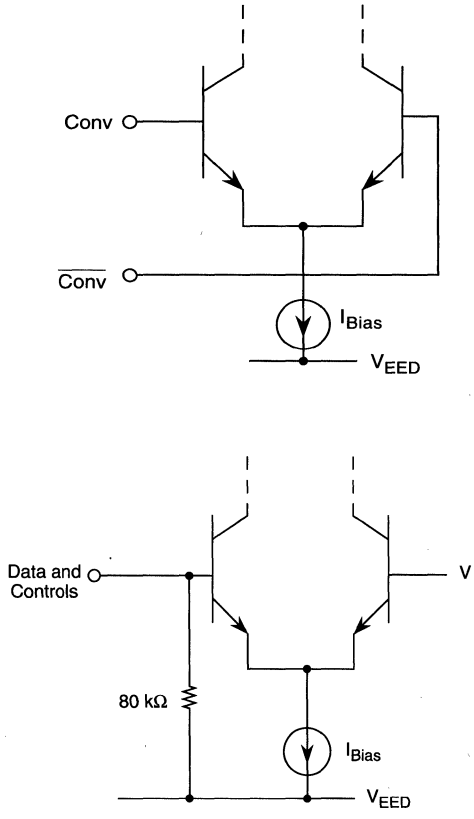
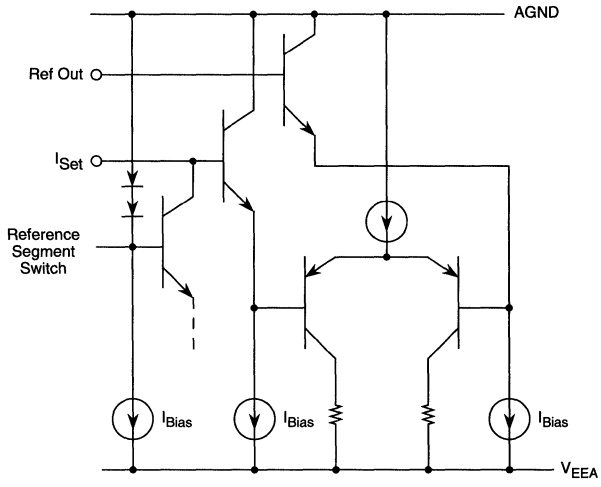


Figure 10- Equivalent Input Circuit - Data, Clock, Controls and Reference





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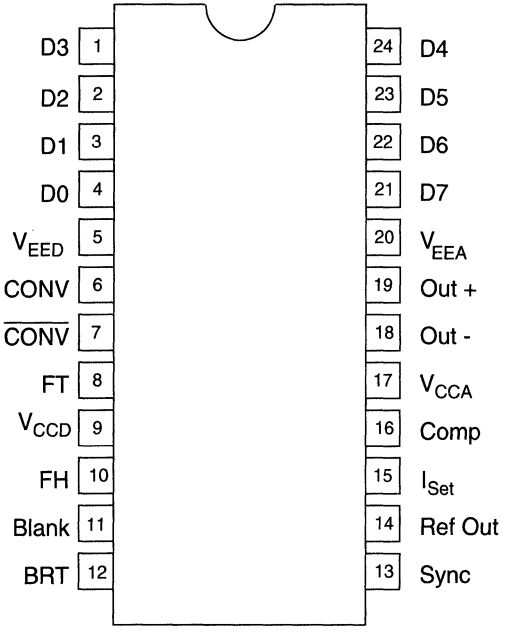
PIN ASSIGNMENTS



PIN FUNCTIONS

NAME	FUNCTION
D3	Data Bit 3
D2	Data Bit 2
D1	Data Bit 1
D0	Data Bit 0 (LSB)
V_{EED}	Digital Negative Supply
CONV	Convert Clock Input
$\overline{CONV}$	Convert Clock Input Complement
FT	Register Feedthrough Control
V_{CCD}	Digital Positive Supply
FH	Data Force High Control
Blank	Video Blank Input
BRT	Video Bright Input
Sync	Video Sync Input
Ref Out	Reference Output
I_{Set}	Reference Current + Input
COMP	Compensation Input
V_{CCA}	Analog Positive Supply
Out-	Output Current Negative
Out+	Output Current Positive
V_{EEA}	Analog Negative Supply
D7	Data Bit 7 (MSB)
D6	Data Bit 6
D5	Data Bit 5
D4	Data Bit 4

LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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SPT5140

8-BIT, ULTRAHIGH SPEED D/A CONVERTER

SIGNAL PROCESSING TECHNOLOGIES

FEATURES

- 400 MWPS Nominal Conversion Rate
- RS-343-A Compatible
- Complete Video Controls: Sync, Blank, Bright and Reference White (Force High)
- 10 KH, 100K ECL Compatible
- Single Power Supply
- Registered Data and Video Controls
- Differential Current Outputs
- Stable On-Chip Bandgap Reference
- 50 and 75 Ohm Output Drive
- ESD Protected Data and Control Inputs

APPLICATIONS

- Raster Graphics
- High Resolution Color or Monochrome Displays to 2k x 2k Pixels
- Medical Electronics: CAT, PET, MR Imaging Displays
- CAD/CAE Workstations
- Solids Modeling
- General Purpose High-Speed D/A Conversion
- Digital Synthesizers
- Automated Test Equipment
- Digital Transmitters/Modulators

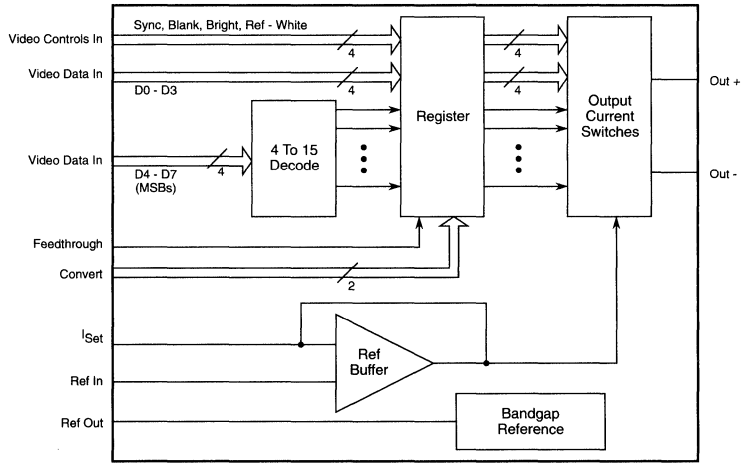
4

GENERAL DESCRIPTION

The SPT5140 is a monolithic 8-bit digital-to-analog converter capable of accepting video data at 400 MWPS. Complete with video controls (Sync, Blank, Reference White [Force High], Bright), the SPT5140 directly drives doubly-terminated 50 or 75 ohm loads to standard composite video levels. Standard set-up level is 7.5 IRE. The SPT5140 includes an internal precision bandgap reference which can drive two other SPT5140s in an RGB graphics system.

The SPT5140 is available in a 24-lead PDIP package in the industrial temperature range of -25 to +85 °C. Contact the factory for military temperature and /883 versions.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING (Beyond which the useful life will be impaired)[1]

Supply Voltages

V_{EED} (measured to V_{CCD}) ..... -7.0 to 0.5 V
V_{EEA} (measured to V_{CCA}) ..... -7.0 to 0.5 V
V_{CCA} (measured to V_{CCD}) ..... -0.5 to 0.5 V

Input Voltages

CONV, Data, and Controls ..... V_{EED} to 0.5 V
(measured to V_{CCD})

Ref+ (measured to V_{CCA}) ..... V_{EEA} to 0.5 V
Ref– (measured to V_{CCA}) ..... V_{EEA} to 0.5 V

Temperature

Operating, ambient ..... -25 to + 85 °C
junction ..... + 175 °C
Lead, Soldering (10 seconds) ..... + 300 °C
Storage ..... -60 to + 150 °C

Note: 1. Operation at any Absolute Maximum Ratings is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

V_{CCD}=V_{CCA} = ground, V_{EEA} = V_{EED} = -5.2 V ±0.3 V, T_A = T_{MIN} to T_{MAX}, C_C = 0 pF, I_{Set} = 1.105 mA

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS						
Integral Linearity Error	1.0 mA<I_{Set}<1.3 mA	VI	-.37 -.95		+.37 +.95	% Full Scale LSB
Differential Linearity Error	1.0 mA<I_{Set}<1.3 mA	VI	-0.2 -0.5		+0.2 +0.5	% Full Scale LSB
Gain Error		VI	-6.5		+6.5	% Full Scale
Gain Error Tempco		V		150		PPM/°C
Bandgap Tempco		V		100		PPM/°C
Input Capacitance, I_{Set}, Ref Out		V		5		pF
Compliance Voltage, + Output		VI	-1.2		1.5	V
Compliance Voltage, - Output		VI	-1.2		1.5	V
Equivalent Output Resistance		VI	20			kΩ
Output Capacitance		V		9		pF
Maximum Current, + Output		IV	45			mA
Maximum Current, - Output		IV	45			mA
Output Offset Current		VI		0.05	0.5	LSB
Input Voltage, Logic High		VI	-1.0			V
Input Voltage, Logic Low		VI			-1.5	V
Convert Voltage, Common Mode Range		IV	-0.5		-2.5	V
Convert Voltage, Differential		IV	0.4		1.2	V
Input Current, Logic Low, Data and Controls		VI		35	120	µA
Input Current, Logic High, Data and Controls		VI		40	120	µA
Input Current, Convert		VI		2	60	µA

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ELECTRICAL SPECIFICATIONS

V_{CCD}=V_{CCA} = ground, V_{EEA} = V_{EED} = -5.2 V ±0.3 V, T_A = T_{MIN} to T_{MAX}, C_C = 0 pF, I_{Set} = 1.105 mA

PARAMETERS	TEST CONDITIONS	LEVEL	MIN	TYP	MAX	UNITS
Reference Voltage Measured to V_{CCA}		VI	-1.3	-1.2	-1.0	V
Reference Output Current		VI	-50			µA
Input Capacitance, Data and Controls		V		3		pF
Power Supply Sensitivity		VI	-120	+20	+120	µA/V
Supply Current		VI		155	220	mA
DYNAMIC CHARACTERISTICS (R_L = 37.5 ohms, C_L = 5 pF, T_A=+25 °C, I_{Set}=1.105 mA)						
Maximum Conversion Rate		IV	385	400		MWPS
Rise Time	10% to 90% G.S.	IV			900	ps
Rise Time	10% to 90% G.S. R_L = 25 ohms	IV			600	ps
Current Settling Time, Clocked Mode t_{SI}	To 0.2% G.S.	V		4		ns
Current Settling Time, Clocked Mode t_{SI}	To 0.2% G.S. R_L = 25 Ω	V		3		ns
Clock to Output Delay, Clocked Mode t_{DSC}	T_A = T_{MIN} to T_{MAX}	III IV		2.2	4 4.5	ns ns
Data to Output Delay, Transparent Mode t_{DST}	T_A = T_{MIN} to T_{MAX}	III IV		3.2	6 6	ns ns
Glitch Energy	Area = 1/2 VT	V		4		pV-s
Convert Pulse Width t_{PWH}, t_{PWL}		III	1.3			ns
Reference Bandwidth, -3 dB		V		1.25		MHz
Set-up Time, Data and Controls t_S		III	1.0			ns
Hold Time, Data and Controls t_H		III	0.5			ns
Slew Rate	20% to 80% G.S.	V		700		V/µS
Clock Feedthrough		III			-48	dB

TEST LEVEL CODES

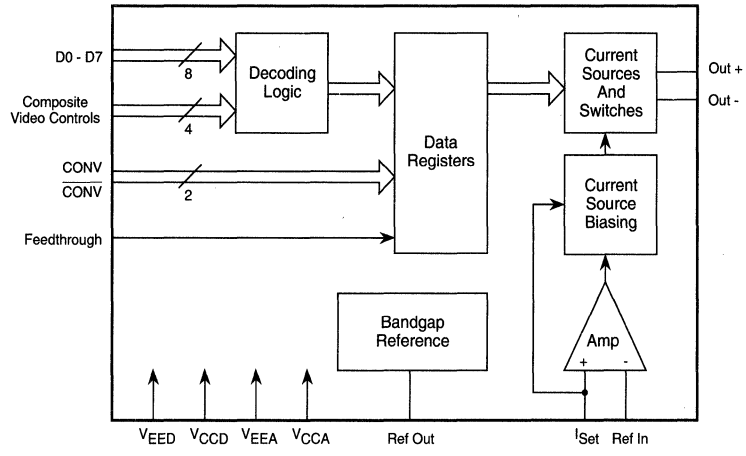
All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests; therefore, T_J = T_C = T_A.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

Figure 1 - Functional Diagram



APPLICATION INFORMATION

The SPT5140 is a high speed video digital-to-analog converter capable of up to 400 MWPS conversion rates. This makes the devices suitable for driving 2048 X 2048 pixel displays at update rates of 60 to 90 Hz.

In addition, the SPT5140 includes an internal bandgap reference which may be used to drive two other SPT5140s if desired.

The SPT5140 has 10KH and 100K ECL logic level compatible video control and data inputs. The complementary analog output currents produced by the devices are proportional to the product of the digital control and data inputs in conjunction with the analog reference current. The SPT5140 is segmented so that the four MSBs of the input data are separated into a parallel "thermometer" code. From here, fifteen current sinks, which are identical, are driven to fabricate sixteen coarse output levels. The remaining four LSBs drive four binary weighted current switches.

MSB currents are then summed with the LSBs that provide a one-sixteenth of full scale contribution to provide the 256 distinct analog output levels.

The video control inputs drive weighted current sinks which are added to the output current to produce composite video output levels. These controls, Sync, Blank, Reference White (Force High), and Bright are needed in video applications.

Another feature that similar video D/A converters do not have is the Feedthrough Control. This pin allows registered or unregistered operation of the video control and data inputs. In the registered mode, the composite functions are latched to the pixel data to prevent screen-edge distortions generally found on unregistered video DACs.

TYPICAL INTERFACE CIRCUIT

GENERAL

A typical interface circuit using the SPT5140 in a color raster application is shown in figure 2. The SPT5140 requires few external components and is extremely easy to use. The very high operating speeds of the SPT5140 require good circuit layout, decoupling of supplies, and proper design of transmission lines. The following considerations should be noted to achieve best performance.

INPUT CONSIDERATIONS

Video input data and controls may be directly connected to the SPT5140. Note that all ECL inputs are terminated as closely to the device as possible to reduce ringing, crosstalk and reflections. A convenient and commonly used microstrip impedance is about 130 ohms, which is easily terminated using a 330 ohm resistor to V_{EE} and a 220 ohm resistor to ground. This arrangement gives a Thevenin equivalent termination of 130 ohms to -2 volts without the need for a -2 volt supply. Standard SIP (Single Inline Package) 220/330 resistor networks are available for this purpose.

It is recommended that stripline or microstrip techniques be used for all ECL interface. Printed circuit wiring of known impedance over a solid ground plane is recommended. The ground plane should be constructed such that analog and digital ground currents are isolated as much as possible. The SPT5140 provides separate digital and analog ground connections to simplify ground layout.

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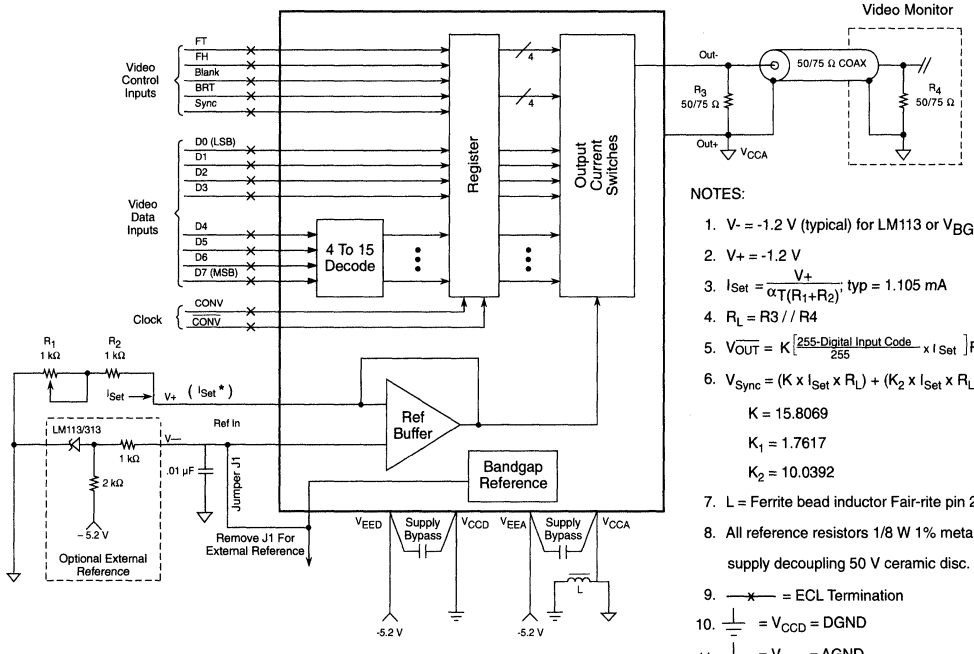
Figure 2 - Typical Interface Circuit



*An external reference can be used or the reference from Ref Out can drive three SPT5140s.

NOTES:

1. V- = -1.2 V (typical) for LM113 or V_{BG}.
2. V+ = -1.2 V
3. $I_{Set} = \frac{V+}{\alpha T(R_1+R_2)}$; typ = 1.105 mA
4. R_L = R3 / / R4
5. $V_{\overline{OUT}} = K\left[\frac{255\text{-Digital Input Code}}{255} \times I_{Set}\right] R_L + [K_1 \times I_{Set} \times R_{L(Bright)}]$
6. $V_{Sync} = (K \times I_{Set} \times R_L) + (K_2 \times I_{Set} \times R_L)$

   K = 15.8069

   K_1 = 1.7617

   K_2 = 10.0392
7. L = Ferrite bead inductor Fair-rite pin 217430011 or equivalent.
8. All reference resistors 1/8 W 1% metal film power supply decoupling 50 V ceramic disc.
9. —x— = ECL Termination
10. ⏚ = V_{CCD} = DGND
11. ⏚ = V_{CCA} = AGND
12. See figure 8 for detail on Ref Buffer.

OUTPUT CONSIDERATIONS

The analog outputs are designed to directly drive a doubly terminated 50 or 75 ohm load transmission system as shown. The source impedances of the SPT5140 outputs are high impedance current sinks. The load impedance (R_L) must be 25 or 37.5 ohms to attain standard RS-343-A video levels. Any deviation from this impedance will affect the resulting video output levels proportionally. As with the data interface, it is important that the analog transmission lines have matched impedance throughout, including connectors and transitions between printed wiring and coaxial cable. The combination of matched source termination resistor R_S and load terminator R_L minimizes reflections of both forward and reverse traveling waves in the analog transmission system. The return path for analog output current is V_{CCA} which is connected to the source termination resistor R_S.

POWER CONSIDERATIONS

The SPT5140 operates from a single standard -5.2 volt supply. Proper bypassing of the supplies will augment the SPT5140 inherent supply noise rejection characteristics. As shown in figure 2, a large tantalum capacitor in parallel with smaller ceramic capacitors is recommended for best performance. The small-valued capacitors should be connected as close to the device package as possible, whereas the tantalum capacitor may be placed up to a few inches away.

The SPT5140 operates with separate analog (V_{EEA}) and digital (V_{EED}) power supplies to establish high noise immunity. Both supplies should eventually be connected to the same power source, but they should be individually decoupled as mentioned previously. The digital supply has a separate ground return which is V_{CCD}. The analog ground return is V_{CCA}. All power and ground pins must be connected in any application. If a +5 V power source is required, the ground pins V_{CCD} and V_{CCA} become the positive supply pins while V_{EED} and V_{EEA} become the ground returns. The relative polarities of the other voltages on inputs and outputs must be maintained.

REFERENCE CONSIDERATIONS

The SPT5140 has two reference inputs (Ref In and I_{Set}) and one reference output (Ref Out). The input pins are connected to the inverting and noninverting inputs of an internal amplifier that serves as a reference buffer.

The output of the buffer amplifier is the reference for the current sinks. The amplifier feedback loop is connected around one of the current sinks to achieve better accuracy. (See figure 8.)

Since the analog output currents are proportional to the digital input data and the reference current (I_{Set}), the full-scale output may be adjusted by varying the reference current. I_{Set} is controlled through the (I_{Set}) input on the SPT5140. A method and equations to set I_{Set} are shown in figure 2. The SPT5140 can use an external negative voltage reference. The external reference must be stable to achieve a satisfactory output and the Ref Inshould be driven through a resistor to minimize offsets caused by bias current. The value for I_{Set} can be varied with the 500 to 1 kΩ trimmer to change the full scale output. A double 50 ohm load (25 ohm) can be driven if I_{Set} is increased by 50% above for doubly-terminated 75 ohm video applications.

DATA INPUTS AND VIDEO CONTROLS

The SPT5140 has standard single-ended data inputs. The inputs are registered to produce the lowest differential data propagation delay (skew) to minimize glitching. There are also four video control inputs to generate composite video outputs. These are Sync, Blank, Bright and Reference White or Force High. Also provided is the Feedthrough control as mentioned earlier. The controls and data inputs are all 10 KH and 100K ECL compatible. In addition, all have internal pulldown resistors to leave them at a logic low so the pins are inactive when not used. This is useful if the devices are applied as standard DACs without the need for video controls or if less than eight bits are used.

The SPT5140 is usually configured in the synchronous mode. In this mode, the controls and data are synchronized to prevent pixel dropout. This reduces screen-edge distortions and provides the lowest output noise while maintaining the highest conversion rate. By leaving the Feedthrough (FT) control open (low), each rising edge of the convert (CONV) clock latches decoded data and control values into a D-type internal register. The registered data is then converted into the appropriate analog output by the switched current sinks. When FT is tied high, the control inputs and data are not registered. The analog output asynchronously tracks the input data and video controls. Feedthrough itself is asynchronous and usually used as a DC control.

The controls and data have to be present at the input pins for a set-up time of t_S before, and a hold time of t_H after, the rising edge of the clock (CONV) in order to be synchronously registered. The set-up and hold times are not important in the asynchronous mode. The minimum pulse widths high (t_{PWH}) and low (t_{PWL}) as well as settling time become the limiting factors. (See figure 3.)

Figure 3 - Timing Diagram

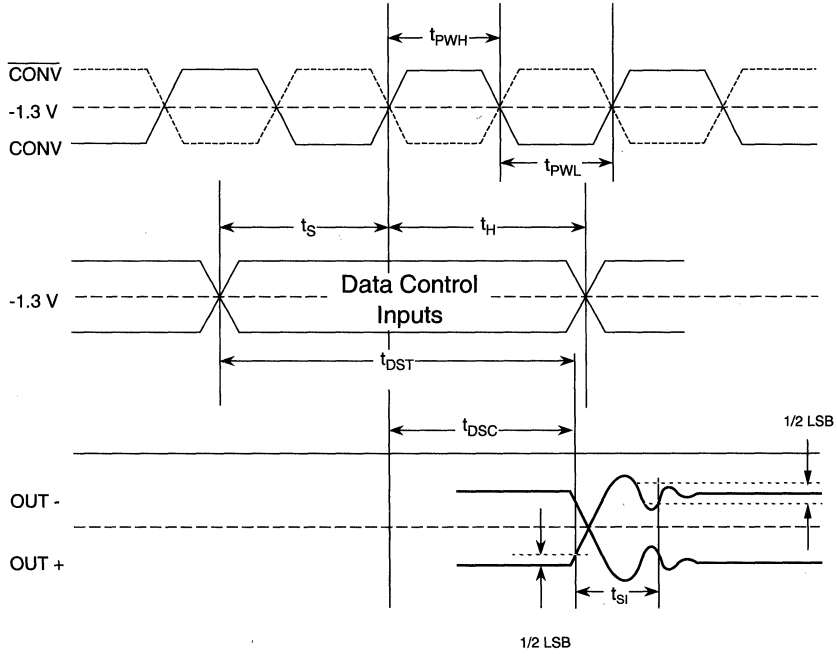


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Table I - Video Control Operation (Output values for setup = 10 IRE and 75 ohm standard load)

Sync	Blank	Ref White	Bright	Data Input	Out - (mA)	Out - (V)	Out - (IRE)	Description
1	X	X	X	X	28.57	-1.071	-40	Sync Level
0	1	X	X	X	20.83	-0.781	0	Blank Level
0	0	1	1	X	0.00	0.000	110	Enhanced High Level
0	0	1	0	X	1.95	-0.073	100	Normal High Level
0	0	0	0	000..	19.40	-0.728	7.5	Normal Low Level
0	0	0	0	111..	1.95	-0.073	100	Normal High Level
0	0	0	1	000..	17.44	-0.654	17.5	Enhanced Low Level
0	0	0	1	111..	0.00	0.000	110	Enhanced High Level

The video controls produce the output levels needed for horizontal blanking, frame synchronization, etc., to be compatible with video system standards as described in RS-343-A. Table I shows the video control effects on the analog output. Internal logic governs Blank, Sync and Force High so that they override the data inputs as needed in video applications. Sync overrides both the data and other controls to produce full negative video output (figure 9).

Reference White video level output is provided by Force High, which drives the internal digital data to full scale output or 100 IRE units. Bright gives an additional 10% of full scale value to the output level. This function can be used in graphic displays for highlighting menus, cursors or warning messages. Again, if the devices are used in non-video applications, the video controls can be left open.

CONVERT CLOCK

For best performance, the clock should be ECL driven, differentially, by utilizing CONV and $\overline{\text{CONV}}$ (figure 4). By driving the clock this way, clock noise and power supply/output intermodulation will be minimized. The rising edge of the clock synchronizes the data and control inputs to the SPT5140. Since the actual switching threshold of CONV is determined by $\overline{\text{CONV}}$, the clock can be driven single-ended by connecting a bias voltage to $\overline{\text{CONV}}$. The switching threshold of CONV is set by this bias voltage.

ANALOG OUTPUTS

The SPT5140 has two analog outputs that are high impedance, complementary current sinks. The outputs vary in proportion to the input data, controls and reference current values so that the full scales output can be changed by setting I_{Set} as mentioned earlier.

In video applications, the outputs can drive a doubly terminated 50 or 75 ohm load to standard video levels. In the standard configuration of figure 5, the output voltage is the product of the output current and load impedance and is between 0 and -1.07 V. The Out- output (figure 9) will provide a video output waveform with the Sync pulse bottom at the -1.07 V level. The Out+ is inverted with Sync up.

Figure 4 - CONVert, $\overline{\text{CONV}}$ ert Switching Levels

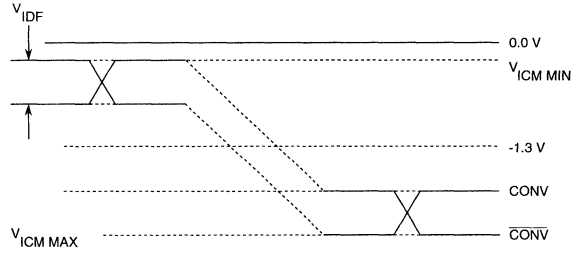


Figure 5A - Standard Load

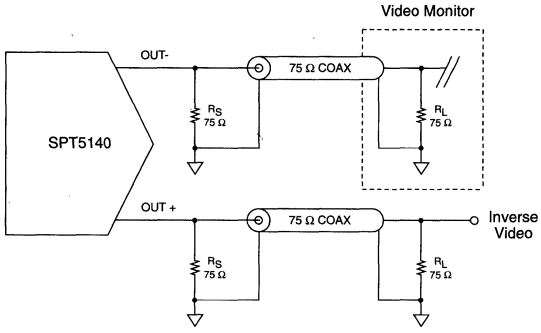
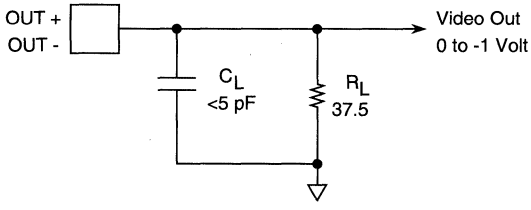


Figure 5B - Test Load



TYPICAL RGB GRAPHICS SYSTEM

In an RGB graphics system, the color displayed is determined by the combined intensities of the red, green and blue (RGB) D/A converter outputs. A change in gain or offset in any of the RGB outputs will affect the apparent hue displayed on the CRT screen.

Thus, it is very important that the outputs of the D/A converters track each other over a wide range of operating conditions. Since the D/A output is proportional to the product of the reference and digital input code, a common reference should be used to drive all three D/As in an RGB system to minimize RGB DAC-to-DAC mismatch and improve TC tracking.

The SPT5140 contains an internal precision bandgap reference which completely eliminates the need for an external reference. The reference can supply up to 50 µA to an external load, such as two other DAC reference inputs.

The circuits shown in figure 6 illustrate how a single SPT5140 may be used as a master reference in a system with multiple DACs (such as RGB). The other DACs are simply slaved from the SPT5140's reference output.

Figure 6 - Typical RGB Graphics System

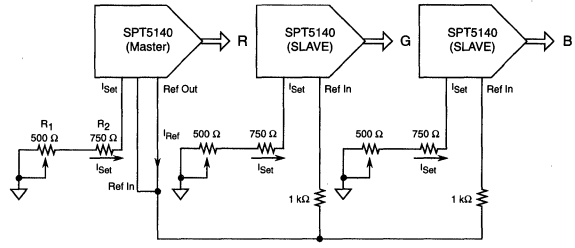


Figure 7 - Burn-In Circuit

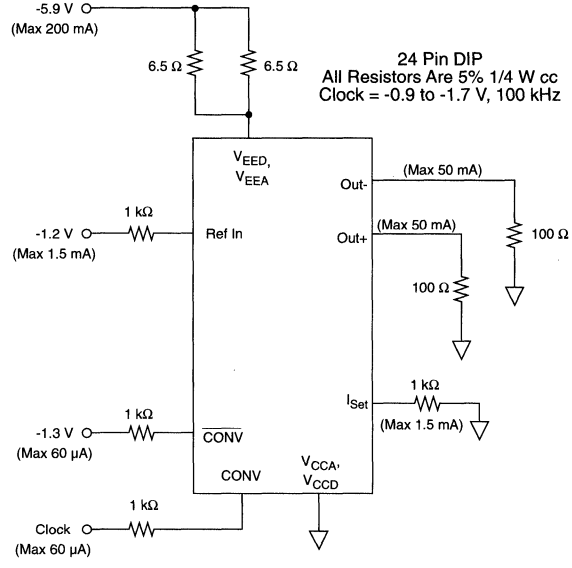


Figure 8 - DAC Output Circuit

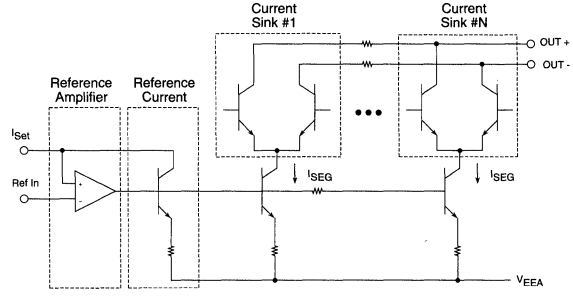


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Figure 9 - Video Output Waveform for Standard Load

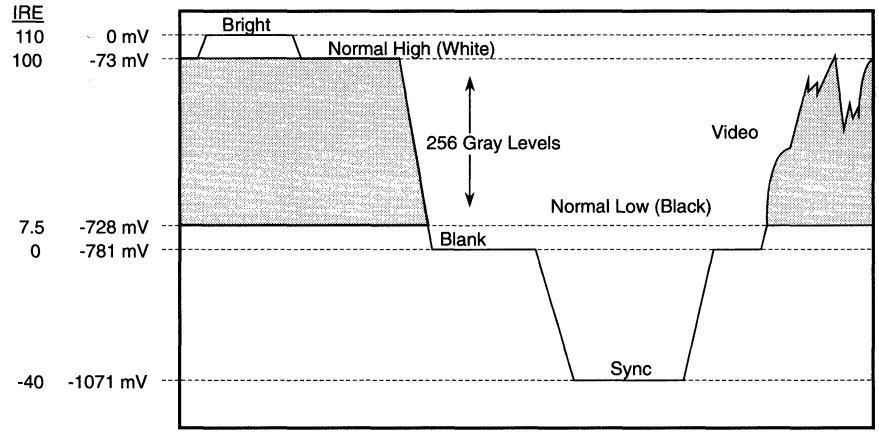
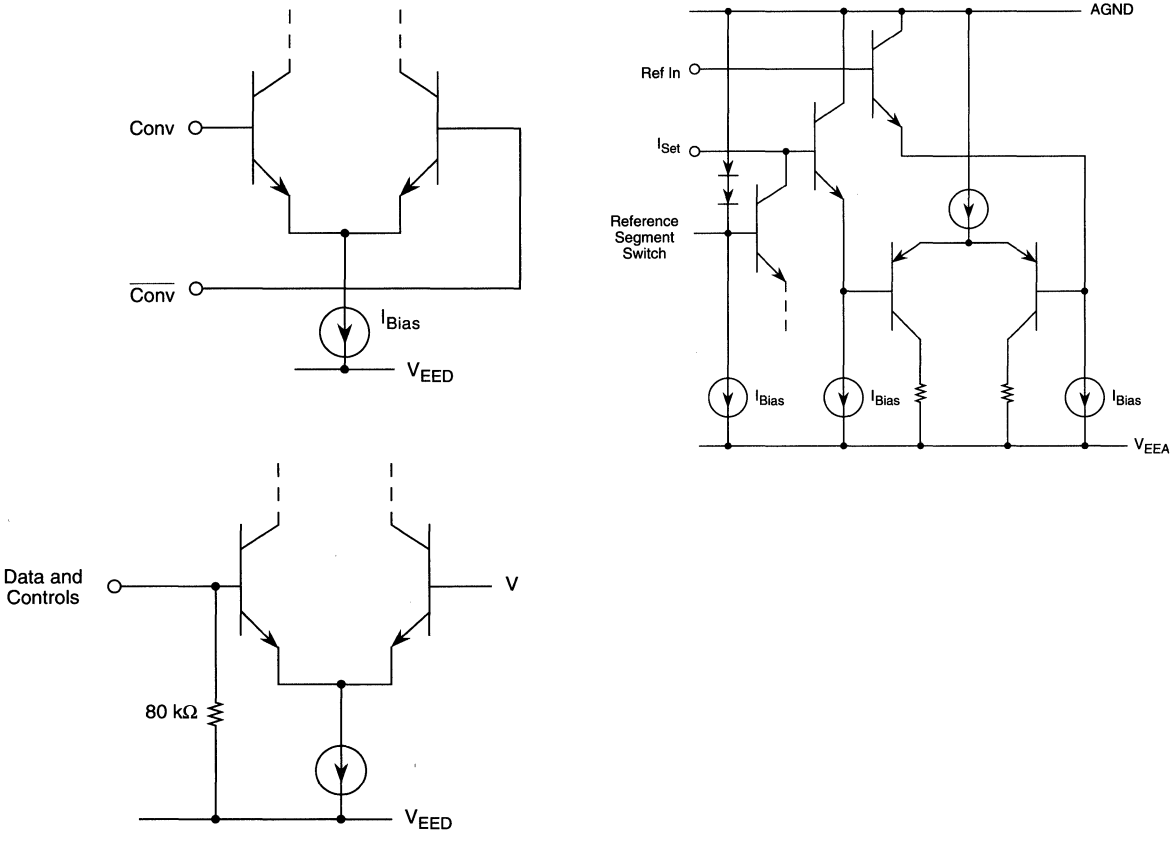
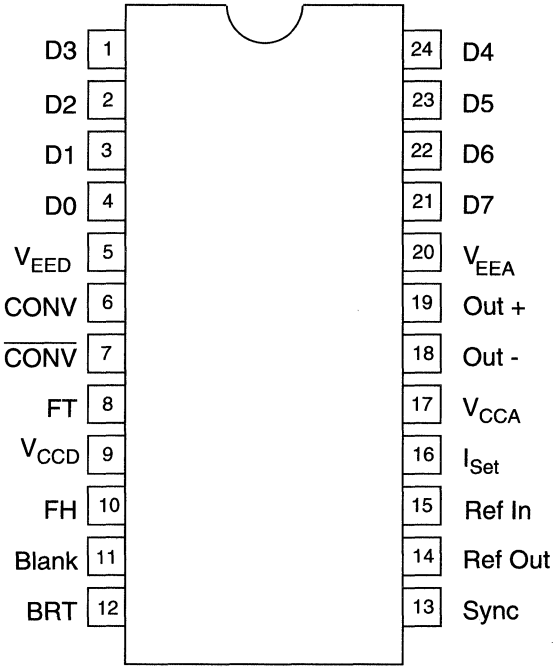


Figure 10 - Equivalent Input Circuits - Data, Clock, Controls and Reference



PIN ASSIGNMENTS



PIN FUNCTIONS

NAME	FUNCTION
$\overline{D3}$	Data Bit 3
$\overline{D2}$	Data Bit 2
$\overline{D1}$	Data Bit 1
$\overline{D0}$	Data Bit 0 (LSB)
V_{EED}	Digital Negative Supply
$\overline{CONV}$	Convert Clock Input
$\overline{\overline{CONV}}$	Convert Clock Input Complement
$\overline{FT}$	Register Feedthrough Control
V_{CCD}	Digital Positive Supply
$\overline{FH}$	Data Force High Control
$\overline{Blank}$	Video Blank Input
$\overline{BRT}$	Video Bright Input
$\overline{Sync}$	Video Sycn Input
$\overline{Ref\ Out}$	Reference Output
$\overline{Ref\ In}$	Reference Input
I_{Set}	Reference Current
V_{CCA}	Analog Positive Supply
$\overline{Out\ -}$	Output Current Negative
$\overline{Out\ +}$	Output Current Positive
V_{EEA}	Analog Negative Supply
$\overline{D7}$	Data Bit 7 (MSB)
$\overline{D6}$	Data Bit 6
$\overline{D5}$	Data Bit 5
$\overline{D4}$	Data Bit 4

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LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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SIGNAL PROCESSING TECHNOLOGIES

SPT5220

10-BIT, 80 MWPS VIDEO DAC

FEATURES

- 80 MHz Pipelined Operation
- +5 V CMOS Monolithic Construction
- ±0.4 LSB Differential Linearity Error
- ±0.6 LSB Integral Linearity Error
- TTL-Compatible Inputs
- RS-343A/RS-170 Compatible Outputs
- Binary or Two's Complement Input Data Format
- Low Power Dissipation of 260 mW
- Internal/External Voltage Reference

APPLICATIONS

- High Resolution Color Graphics
- Medical Electronics: CAT, PET, MR Imaging Displays
- CAD/CAE Workstations
- General Purpose High-Speed D/A Conversion
- Direct Digital Synthesis (DDS)
- Digital Radio Transmitters/Modulators
- High Definition Television (HDTV)

4

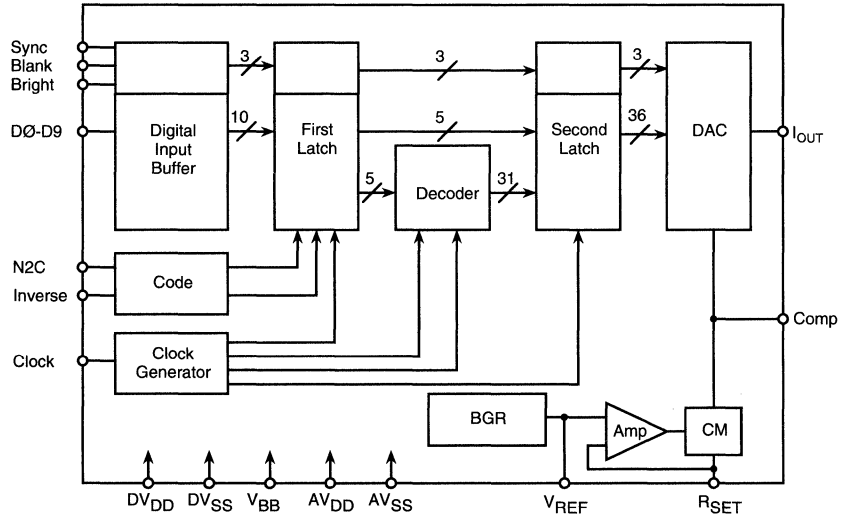
GENERAL DESCRIPTION

The SPT5220 is a monolithic 10-bit, 80 MWPS CMOS D/A converter for high-resolution color graphics and video system applications. The device operates from a single +5 V power supply and all digital inputs are TTL/CMOS compatible.

The SPT5220 generates RS343A-compatible video outputs (capable of driving a doubly-terminated 75 Ω load) and RS170-compatible video outputs (capable of driving a singly-terminated 75 Ω load) without the need for external buffers. The data latches minimize the data time skew and reduce the glitches that can adversely affect many applications.

The device is available in a 28-lead plastic DIP package with performance guaranteed over a commercial temperature range.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1,2,3]

Supply Voltages

AV_{DD} ..... -0.5 to +7.0 V
DV_{DD} ..... -0.5 to +7.0 V

Input Voltages

Any Digital Pin ..... DV_{SS}-3.0 V to DV_{DD}+3.0 V

ESD Susceptibility ..... ±2,000 V

Temperature

Operating Temperature Range (Ambient) ..... 0 to +70 °C
Storage Temperature ..... -55 to +150 °C

Notes: 1. Operation at any absolute maximum rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.
2. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is not implied.
3. Applied voltage must be current limited to the specified range.

ELECTRICAL SPECIFICATIONS[4]

T_A=T_{MIN} to T_{MAX}, AV_{DD}=DV_{DD}=V_{BB}=+5.0 V, AV_{SS}=DV_{SS}=0.0 V, V_{REF}=1.235 V, R_{SET}=165 Ω, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT5220 MIN	SPT5220 TYP	SPT5220 MAX	UNITS
DC CHARACTERISTICS						
Resolution			10			Bits
Differential Linearity Error		VI		±0.4	±1.0	LSB
Integral Linearity Error		VI		±0.6	±1.0	LSB
Gray Scale Error		VI			±5.0	% Gray
Monotonicity		VI		Guaranteed		
Digital Input High Current	V_{IN}=2.4 V	VI			1.0	µA
Digital Input Low Current	V_{IN}=0.4 V	VI	-1.0			µA
Digitial Input Capacitance	f_{IN}=1 MHz	IV		20	40	pF
Analog Outputs						
Gray Scale Current		VI			22	mA
Output Current						
	Bright to White	VI	1.0	1.90	3.0	mA
	White to Black	VI	18.1	19.05	20.0	mA
	Black to Blank	VI	0.5	1.43	2.5	mA
	Blank to Sync	VI	6.5	7.62	8.5	mA
	Sync Level	VI	0	5	50	µA
	LSB Size	V		18.62		µA
Output Compliance		VI	-1.0		+1.5	V
Output Impedence		V		11		kΩ
Output Capacitance	f_{IN}=1 MHz	IV		14	30	pF
Internal Reference Voltage		VI	1.16	1.235	1.36	V
Power Supply Rejection Ratio	f_{IN}=1 kHz, comp=0.1 µF	V		-30		dB
Operating Supply Voltage		VI	4.75	5.00	5.25	V
Digital Input Voltage	High	VI	2.0		V_{DD}+0.3	V
	Low	VI	V_{SS}-0.3		0.8	V
Effective Output Load		V		37.5		Ω
Data Input Setup Time		IV	2.0			ns
Data Input Hold Time		IV	2.0			ns
Clock Cycle Time		IV	12.5			ns
Clock Pulse Width High		IV	5			ns
Clock Pulse Width Low		IV	5			ns

Note: 4. To avoid power latch-up, drive all supply pins (AV_{DD}, DV_{DD}, and V_{BB}) from the same source.

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ELECTRICAL SPECIFICATIONS

$T_A=T_{MIN}$ to T_{MAX}, $AV_{DD}=DV_{DD}=V_{BB}$=+5.0 V, $AV_{SS}=DV_{SS}$=0.0 V, V_{REF}=1.235 V, R_{SET}=165 Ω, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT5220 MIN	SPT5220 TYP	SPT5220 MAX	UNITS
AC CHARACTERISTICS						
Clock Rate			80			MHz
Analog Output Delay		V		7		ns
Analog Output Rise Time		V		4		ns
Analog Output Fall Time		V		4		ns
Analog Output Settling Time[5]						
to ±1 LSB		IV		100	150	ns
to ±2 LSB		IV		70	100	ns
Clock and Data Feedthrough[5]		V		-34		dB
Glitch Impulse[5]		IV		30		pv-sec
Differential Gain Error		V		0.8		%
Differential Phase Error		V		0.9		Degree
Pipeline Delay		VI			2	Clock Cycles
V_{DD} Supply Current[6]		VI		50	70	mA

Note: 5. Clock and data feedthrough are functions of the amount of overshoot and undershoot on the digital inputs. For this test, the digital inputs have a 1 kΩ resistor to ground driven by 74HC logic. Settling time does not include clock and data feedthrough. Glitch impulse includes clock and data feedthrough.

6. At f_{MAX}, IDD (typ) at $AV_{DD}=DV_{DD}$=5.25 V, CLK=0 V to 3 V (80 MHz), NC2=High, Data (DØ-D9)=0 V to 3 V (40 MHz), Inverse=Sync=Blank=Bright=Low.

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests; therefore, $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

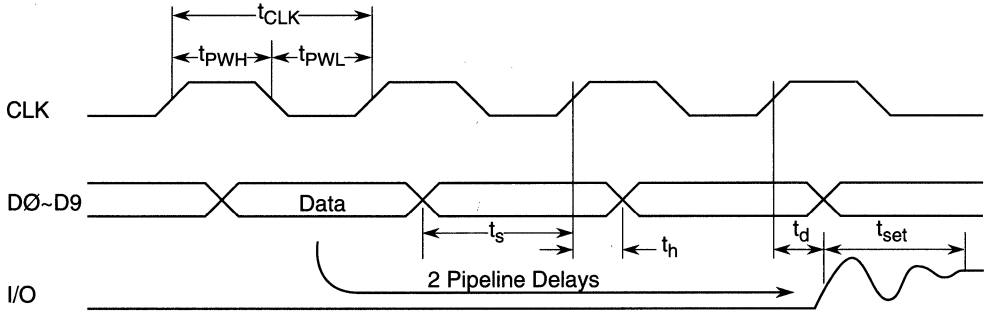
CIRCUIT DESCRIPTION AND OPERATION

The SPT5220 contains a 10-bit DAC, input buffers and latches, internally or externally generated voltage reference and complete video controls. The following describes the main operation of the device and outlines several considerations that should be noted to achieve the best performance.

CLOCK INPUT

CLK is the device clock input and is typically the pixel clock rate of the system. It is TTL compatible. The digital data D0-D9 and all video controls (SYNC, BLANK, BRIGHT) are all latched on the rising edge of CLK. See figure 1.

Figure 1: Timing Waveform[7,8,9]



Note:
7. Output delay (t_d) is measured from the 50% point of the rising edge of CLK to the full scale transition.
8. Settling time (t_{set}) is measured from the 50% point of full scale transition to the output remaining within ±1, ±2 LSB.
9. Output rise/fall time (t_r, t_f) is measured between the 10% and 90% points of full scale transition.

DIGITAL INPUTS AND VIDEO CONTROLS

All ten bits of data (D0-D9, D0 is the LSB) are latched into the device on the rising edge of each clock cycle. There are also three video control inputs to generate composite video outputs. They are SYNC, BLANK and BRIGHT. A logic "1" on the SYNC input generates the sync level. A logic "1" on the BLANK input generates the pedestal level. BRIGHT is the bright signal input. These inputs are pipelined to maintain synchronization with the digital input data. These video controls produce the output levels needed to be compatible with video system standards. Table 1 shows the video control effects on the analog output.

Table 1 - Video Output Truth Table[10]

DESCRIPTION	I_{OUT} (mA)	SYNC	BLANK	BRIGHT	DATA (D9-D0)
White + Bright	30.00	0	0	1	3FFH
White	28.10	0	0	0	3FFH
Data + Bright	Data + 10.95	0	0	1	Data
Data	Data + 9.05	0	0	0	Data
Black	9.05	0	0	0	000H

Note: 10. Double-terminated load of 75 Ω. VREF=1.235 V R_{SET}=165 Ω.

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There are two different input data formats available: binary and two's complement. In addition, these formats can be either normal or inverted. The video control truth table for these options are given in table 2.

Table 2 - Video Control Truth Table[11]

N2C	INVERSE	DATA (D9-D0)	OUTPUT (I/O)	DESCRIPTION
1	0	0000000000 1111111111	Black Level White Level	Binary
1	1	0000000000 1111111111	White Level Black Level	Inverse Binary
0	0	1000000000 0111111111	Black Level White Level	Two's Complement
0	1	1000000000 0111111111	White Level Black Level	Inverse Two's Complement

Note: 11. Doubly-terminated load of 75 Ω, Sync=Blank=Bright=Low

REFERENCE

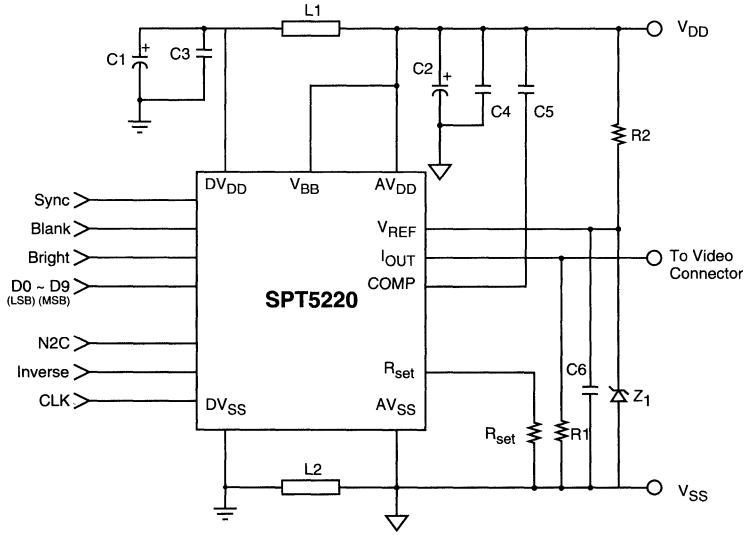
The SPT5220 can be used with either an internal or external voltage reference. The typical interface circuits are shown in figures 2 and 3. When using an external reference (figure 2), the input voltage supplied must be 1.235 volt (typ). When using the internal reference (figure 3), the V_{REF} pin should not drive any external circuitry except for the decoupling capacitor. A bypass capacitor of 0.1 µF with the shortest possible lead lengths should be connected between V_{REF} and V_{SS}. With either configuration, the COMP pin (compensation capacitor) should be connected to V_{DD} through the bypass capacitor. The COMP capacitor should be kept as close as possible to the device to keep the lead lengths to an absolute minimum.

Rset is the full scale adjust control. A resistor (Rset) connected between this pin and ground controls the magnitude of the full-scale video signal. The value for Rset is determined by the relationship:

$$Rset=3.754 \times 1000 \times V_{REF}/Iout.$$

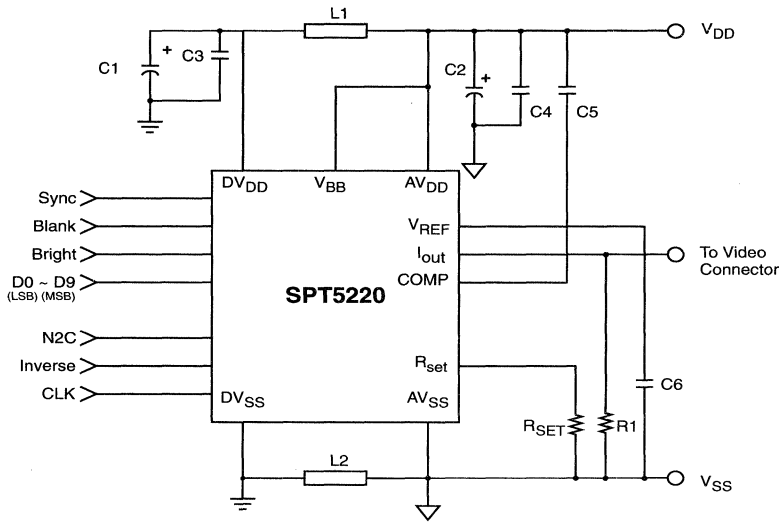
The electrical specifications are given with an Rset value of 165 ohms.

Figure 2 - Typical Interface Circuit (External Reference)



Component	Description
C1, C2	10 µF Capacitor
C3 - C6	0.1 µF Ceramic Capacitor
L1, L2	Ferrite Bead
R1	75 Ω 1% Metal Film Resistor
R2	1 kΩ 5% Resistor
R_{SET}	165 Ω 1% Film Resistor (180 Ω//2 kΩ)
Z_1	1.235 V Voltage Reference (ICL8069CCSQ2)

Figure 3 - Typical Interface Circuit (Internal Reference)



Component	Description
C1, C2	10 µF Capacitor
C3 - C6	0.1 µF Ceramic Capacitor
L1, L2	Ferrite Bead
R1	75 Ω 1% Metal Film Resistor
R_{SET}	165 Ω 1% Film Resistor (180 Ω//2 kΩ)

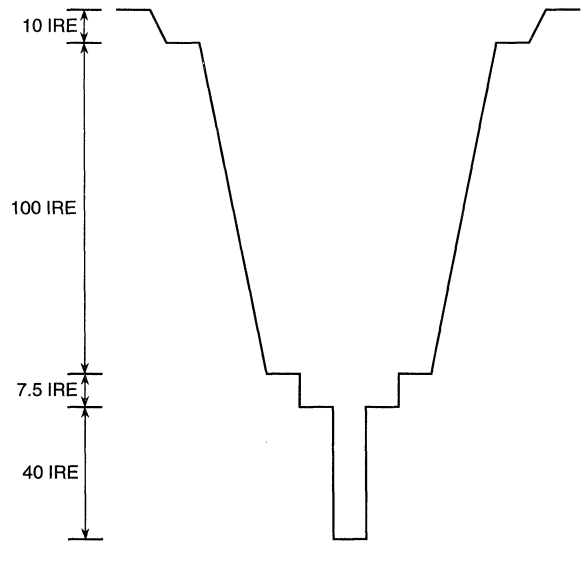
NOTE: AV_{DD}, DV_{DD} and V_{RB} must be supplied from the same source (Analog +5 V) to prevent a latch-up condition due to power supply sequencing.

ANALOG OUTPUT

The SPT5220 generates RS-343A compatible video outputs capable of directly driving a doubly-terminated 75 ohm load, and RS-170 compatible video outputs capable of directly driving a singly-terminated 75 ohm load without the need for external buffers. Figure 4 shows the video waveforms associated with the output driving the doubly-terminated 75 ohm load.

Figure 4 - Composite Video Output Wave Form[12]

LEVEL	mA	V
Bright	30.00	1.125
White	28.10	1.054
Black	9.05	0.340
Blank	7.62	0.286
Sync	0.00	0.00



Note: 12. Doubly-terminated load of 75 Ω, V_{REF}=1.235 V, R_{SET}=165 Ω. RS-343 levels and tolerances are assumed on all levels.

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PC BOARD CONSIDERATIONS

LAYOUT CONSIDERATIONS

To minimize noise on the power lines and ground lines, shield and decouple the digital inputs. Keep the trace length between groups of V_{DD} (AV_{DD}, DV_{DD}) and V_{SS} (AV_{SS}, DV_{SS}) as short as possible to minimize inductive ringing.

SUPPLY AND GROUND CONSIDERATIONS

Use a 0.1 µF ceramic capacitor in parallel with a 10 µF tantalum capacitor for decoupling between the power line and the ground line. The digital power plane (DV_{DD}) and the analog power plane (AV_{DD}) are connected through a ferrite bead. The digital ground plane (DV_{SS}) and the analog ground plane (AV_{SS}) are also connected through a ferrite bead. (See figures 3 and 4). Locate these ferrite beads within three inches of the SPT5220.

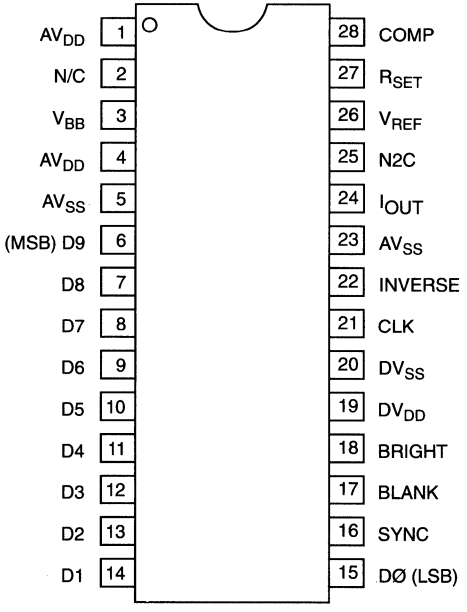
DIGITAL SIGNAL INTERCONNECT

The PCB line between the TTL driver (that drives the SPT5220) and the input to the SPT5220 will have a low impedance source and be terminated with a high impedance. It behaves like a low impedance transmission line so signal transitions will be reflected from the high impedance input of the SPT5220. To reduce ringing caused by transmission line mismatch, shorten the line length or terminate the line. Both serial and parallel termination methods will work, but serial is preferred. Serial termination is achieved by installing a resistor of approximately 50 Ω between the TTL driver output and the SPT5220 digital input.

ANALOG SIGNAL INTERCONNECT

To minimize noise pickup and reflections due to impedance mismatch, locate the SPT5220 as closely as possible to the output connector. The line between the DAC output and the monitor input should be regarded as a transmission line since it can cause problems in transmission line mismatch. Use the double-termination method to avoid these problems. By using the double terminated method, the transmission lines are matched, providing an ideal, nonreflective system.

PIN ASSIGNMENTS



PIN FUNCTIONS

NAME	FUNCTION
AV_{DD}	Analog Power
N/C	No Connection
V_{BB}	Substrate Power (Connected to AV_{DD})
AV_{DD}	Analog Power
AV_{SS}	Analog Ground
D9 - D0	Digital Inputs (D9=MSB, D0=LSB)
SYNC	Sync Signal Input (Logic 1 Generates Level)
BLANK	Blank Signal Input (Logic 1 Generates Level)
BRIGHT	Bright Signal Input
DV_{DD}	Digital Power
DV_{SS}	Digital Ground
CLK	Clock Input (TTL-Compatible)
INVERSE	Inverse Signal Input
AV_{SS}	Analog Ground
I_{out}	Analog Current Output
N2C	Two's Complement Signal Input (Active Low)
V_{REF}	Voltage Reference (Externally Driven)
R_{set}	Full-Scale Adjust Control
COMP	Compensation Capacitor

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SPT5230

10-BIT, 50 MWPS TRIPLE VIDEO DAC

ADVANCED INFORMATION

FEATURES

- 10-Bit Triple Video Digital-to-Analog Converter
- 50 MWPS Operation (typ)
- Low Power: 280 mW
- Operating Temperature Range: 0 to +70 °C
- 5 V Monolithic CMOS
- 52-pin SQFP Package (10 mm x 10 mm, 0.65 mm pitch)

APPLICATIONS

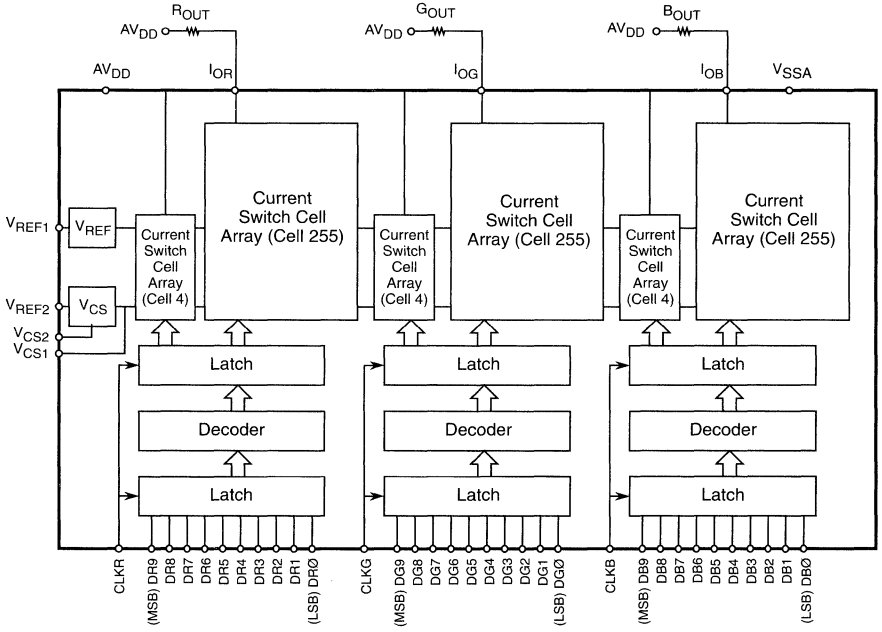
- High-Speed Digital-to-Analog Conversion
- High Performance, High Resolution Color Graphics
- Desktop Video Processing
- Digital TV

4

GENERAL DESCRIPTION

The SPT5230 is a 10-bit, 50 MWPS triple video digital-to-analog converter specifically designed for high performance, high resolution color graphics monitor applications and video processing applications. A single external resistor controls the full-scale output current. The differential linearity errors of the DACs are guaranteed to be a maximum of ±0.5 LSB over the full temperature range. The device is available in a 52-pin SQFP package.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING (Beyond which damage may occur)[1]

Supply Voltages
AV_{DD} (measured to GND) ..... -0.3 to 7.0 V

Input Voltage
Clock and Data ..... GND to AV_{DD}

Output Current
I_{OUT} ..... 0 to 30 mA

Temperature
Operating, ambient ..... 0 to +70 °C
Storage ..... -55 to + 125 °C

Note: 1. Operation at any Absolute Maximum Ratings is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

f_{CLK} = 36 MHz, AV_{DD} = 5.0 V, Output Pull-Up Load = 75 Ω, T_A = 25 °C

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS						
DC Performance						
Resolution				10.0		Bits
Differential Linearity	$T_A = T_{MIN}$ to T_{MAX}	I			±1.0	LSB
Integral Linearity		I			±2.0	LSB
Analog Outputs						
Output Full Scale Voltage		I	0.85	1.0	1.15	V
Compliance Voltage		I	0.5	1.0	1.25	V
Dynamic Performance						
Conversion Rate		I	36	50		MWPS
Propagation Delay		V		10		ns
Crosstalk		V		-49		dB
Digital Inputs and Timing						
Input Current, Logic High	V_{IH} = 5 V	I			5	µA
Logic Low	V_{IL} = 0 V	I	-5			µA
Set-Up Time, Data and Controls (t_S)		I	5			ns
Hold Time, Data and Controls (t_h)		I	5			ns
Clock Pulse Width (Low) (t_{PW0})		I	14.0			ns
Clock Pulse Width (High) (t_{PW1})		I	14.0			ns
Power Supply Requirements						
Supply Voltage		I	4.75		5.25	V
Supply Current		V		56		mA
Power Dissipation		V		280		mW

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests; therefore, $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

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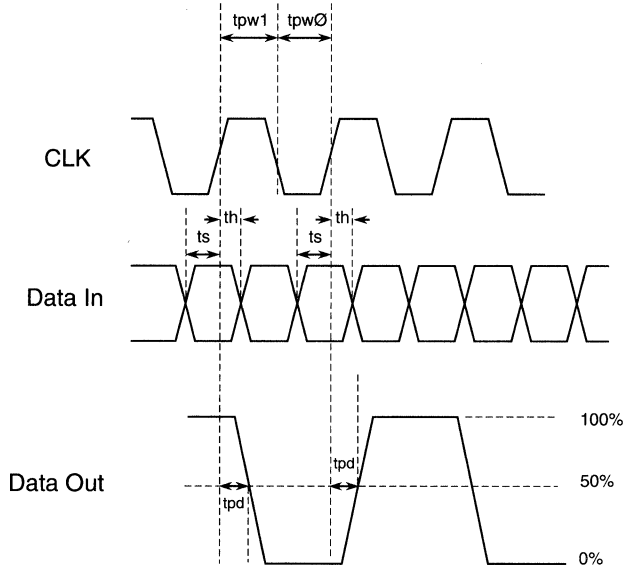
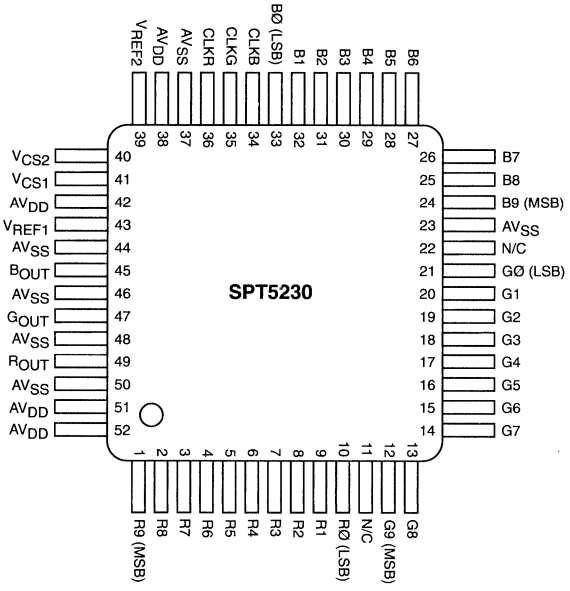
Figure 1 - Timing Diagram



PIN ASSIGNMENTS



PIN FUNCTIONS

NAME	FUNCTION
R_{OUT}	Red Analog Current Output
G_{OUT}	Green Analog Current Output
B_{OUT}	Blue Analog Current Output
R0 - R9	Red Data Inputs
G0 - G9	Green Data Inputs
B0 - B9	Blue Data Inputs
CLKR	Red Clock Input
CLKG	Green Clock Input
CLKB	Blue Clock Input
V_{REF1}	Voltage Reference Decoupling (A 0.1 µF ceramic capacitor should be used.)
V_{REF2}	Voltage Reference Input (A 0.1 µF ceramic capacitor should be used.)
V_{CS1}	Control Voltage Decoupling (A 0.1 µF ceramic capacitor should be used.)
V_{CS2}	Full-Scale Adjust Control Voltage (A 0.1 µF ceramic capacitor should be used.)
AV_{SS}	Analog Ground
AV_{DD}	Analog Power Supply
N/C	No Connection

LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

4755 Forge Road, Co. Springs, CO 80907
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SIGNAL PROCESSING TECHNOLOGIES

SPT9712

12-BIT, 100 MWPS ECL D/A CONVERTER

ADVANCED INFORMATION

FEATURES

- 12-Bit, 100 MWPS Digital to Analog Converter
- ECL Compatibility
- Low Power: 600 mW
- 1/2 LSB DNL
- 40 MHz Multiplying Bandwidth
- Industrial Temperature Range
- Superior Performance over AD9712
  - Improved Settling Time of 8 ns
  - Improved Glitch Energy 5 pV-s

APPLICATIONS

- Fast Frequency Hopping Spread Spectrum Radios
- Direct Sequence Spread Spectrum Radios
- Microwave and Satellite Modems
- Test & Measurement Instrumentation
- Military Applications

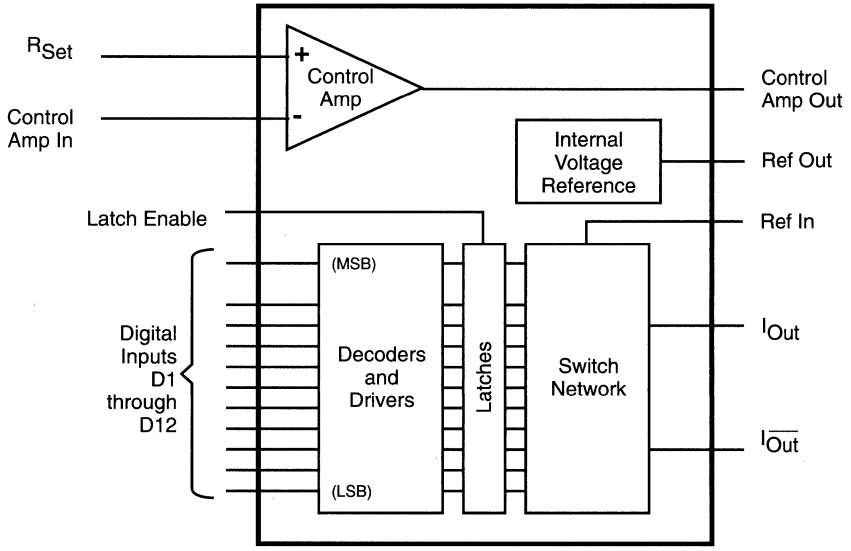
4

GENERAL DESCRIPTION

The SPT9712 is a 12-bit, 100 MWPS digital-to-analog converter designed for direct digital synthesis, high resolution imaging and arbitrary waveform generation applications. This device is pin-for-pin compatible with the AD9712 with significantly improved performance. The SPT9712 is an ECL-compatible device. It features a fast settling time of 8 ns and low glitch impulse energy of 5 pV-s, which results in excellent spurious free dynamic range characteristics.

The SPT9712 is available in 28-lead plastic DIPs and 28-lead PLCCs. Contact the factory for military and /883 package options.

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATING (Beyond which damage may occur)[1]

Supply Voltages
- Negative Supply Voltage (V_{EE}) ..... -7 V
- A/D Ground Voltage Differential ..... 0.5 V

Input Voltages
- Digital Input Voltage (D1-D12, Latch Enable) ..... 0 V to V_{EE}
- Control Amp Input Voltage Range ..... 0 V to -4 V
- Reference Input Voltage Range (V_{REF}) .... -3.7 V to V_{EE}

Output Currents
- Internal Reference Output Current ..... 500 µA
- Control Amplifier Output Current ..... ±2.5 mA

Temperature
- Operating Temperature ..... -25 to + 85 °C
- Junction Temperature ..... + 150 °C
- Lead, Soldering (10 seconds) ..... + 300 °C
- Storage ..... -65 to + 150 °C

Note: 1. Operation at any Absolute Maximum Ratings is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

$T_A=T_{min}$ - T_{max}, V_{EE}=-5.2 V, f_{clock}=100 MHz, 50% clock duty cycle, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
DC Performance						
Resolution				12		Bits
Differential Linearity				±0.5	±0.75	LSB
Differential Linearity	Max at Full Temp.				±1.5	LSB
Integral Linearity	Best Fit			±0.75	±1.0	LSB
Integral Linearity	Max at Full Temp.				±1.75	LSB
Output Capacitance				10		pF
Gain Error	+25 °C			1.0	5.0	% F.S.
Gain Error Tempco				150		PPM/°C
Zero-Scale Offset Error	+ 25 °C			0.5	2.5	µA
Offset Drift Coefficient				0.01		µA/°C
Compliance Voltage			-1.2		+2.0	V
Equivalent Output Resistance				1.0		kΩ
Input Voltage, Logic			-4.0		0.0	V
Dynamic Performance						
Conversion Rate	(Settling to 0.1%)		100			MWPS
Current Settling Time[1] t_{ST}				8		ns
Delay Time t_D				1		ns
Glitch Energy				5		pV-s
Full Scale Output Current				20.48		mA
Spurious-Free Dynamic Range	+ 25 °C					
1.23 MHz; 10 MWPS	2 MHz Span		70			dBc
5.055 MHz; 20 MWPS	2 MHz Span		72			dBc
10.1 MHz; 50 MWPS	2 MHz Span		68			dBc
16 MHz; 40 MWPS	10 MHz Span		68			dBc
Rise Time / Fall Time	R_L = 50 Ω			2		ns
Power Supply Requirements						
Negative Supply Current (-5.2 V)	+25 °C			115		mA
Nominal Power Dissipation				600		mW
Power Supply Rejection Ratio				30	100	µA/V

[1]Measured as voltage settling at mid-scale transition to ±0.024%; R_L = 50 Ω.

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ELECTRICAL SPECIFICATIONS

$T_A=T_{min}$ - T_{max}, V_{EE}=-5.2 V, f_{clock}=100 MHz, 50% clock duty cycle, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
Voltage Input and Control						
Reference Input Impedance	+25 °C			3		kΩ
Ref. Multiplying Bandwidth	+25 °C			40		MHz
Internal Reference Voltage	+25 °C		-1.15	-1.20	-1.25	V
Internal Reference Voltage Drift	Full			50		ppm/°C
Amplifier Input Impedance				50		kΩ
Amplifier Input Bandwidth				1		MHz
Digital Inputs						
Logic 1 Voltage	Full Temp.		-1.0	-0.8		V
Logic 0 Voltage	Full Temp.			-1.7	-1.5	V
Logic 1 Current	Full Temp.				20	µA
Logic 0 Current	Full Temp.				10	µA
Input Capacitance	+25 °C			3		pF
Input Setup Time - t_S	+25 °C		0.5	-0.3		ns
Input Setup Time - t_S	Full Temp.		0.8			ns
Input Hold Time - t_H	+25 °C		1.8	1.2		ns
Input Hold Time - t_H	Full Temp.		2.0			ns
Latch Pulse Width - t_{PWL}, t_{PWH}	+25 °C			4.0		ns

TEST LEVEL CODES

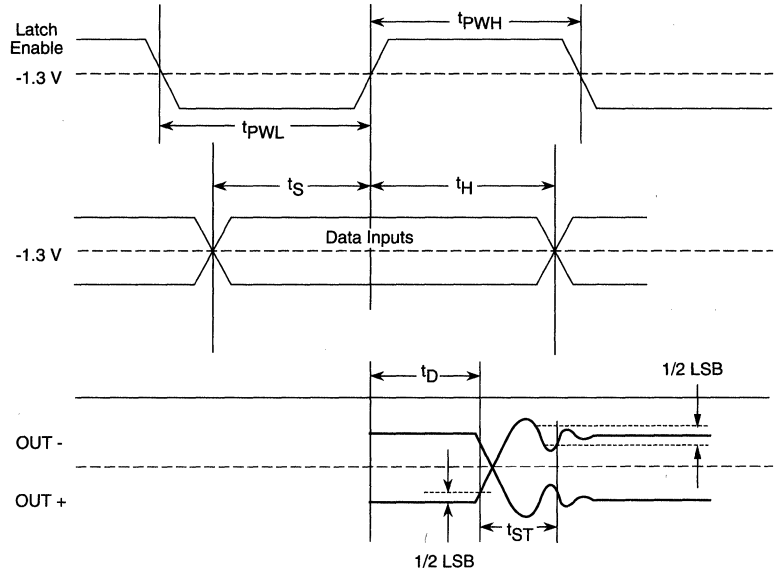
All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests; therefore, $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

Figure 1 - Timing Diagram



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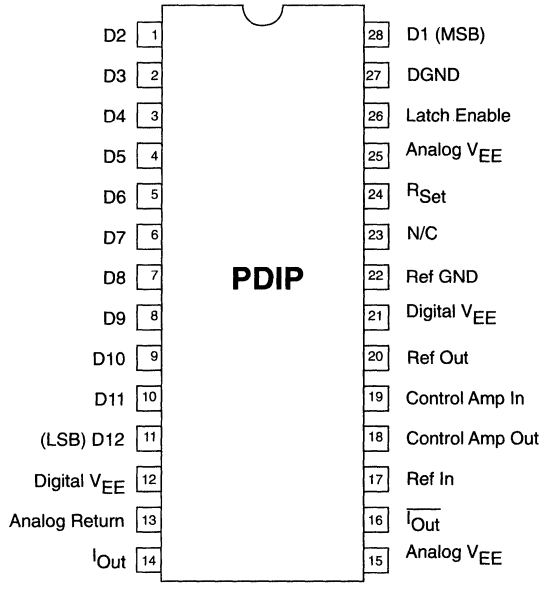
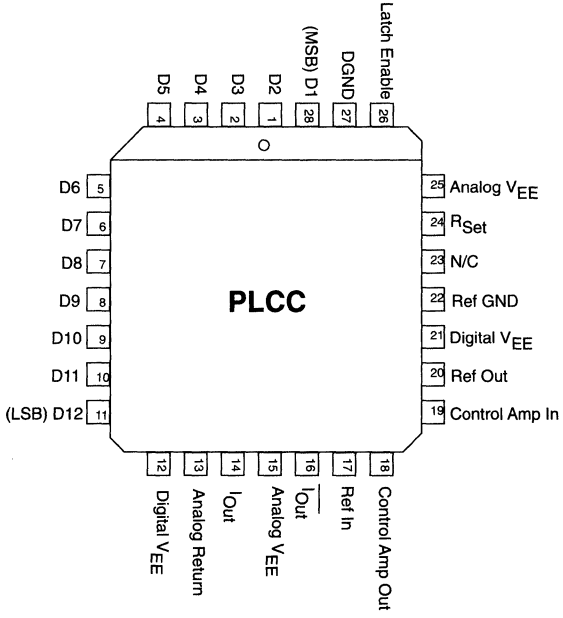
PIN ASSIGNMENTS



PIN FUNCTIONS

Out+	Analog Current Output
Out-	Complementary Analog Current Output
D_1-D_{12}	Digital Input Bits (D_{12} is the LSB)
Latch Enable	Latch Control Line
Ref In	Voltage Reference Input
Ref Out	Internal Voltage Reference Output Normally Connected to Control Amp In
Ref GND	Ground Return For Internal Voltage Reference and Amplifier
Control Amp In	Normally Connected to Ref Out If Not Connected to External Reference
Control Amp Out	Output of Internal Control Amplifier Normally Connected to Ref In
R_{Set}[1]	Connection for External Resistance Reference When Using Internal Amplifier. Nominally 7.5 kΩ
Analog Return	Analog Return Ground
Analog V_{EE}	Analog Negative Supply (-5.2 V)
Digital V_{EE}	Digital Negative Supply (-5.2 V)
DGND	Digital Ground Return
N/C	Not Connected

[1]Full-Scale Current Out=128(V_{Ref}/R_{Set})



LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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SIGNAL PROCESSING TECHNOLOGIES

SPT9713

12-BIT, 100 MWPS TTL D/A CONVERTER

ADVANCED INFORMATION

FEATURES

- 12-Bit, 100 MWPS Digital to Analog Converter
- TTL Compatibility
- Low Power: 640 mW
- 1/2 LSB DNL
- 40 MHz Multiplying Bandwidth
- Industrial Temperature Range
- Superior Performance over AD9713
  - Improved Settling Time of 8 ns
  - Improved Glitch Energy 5 pV-s

APPLICATIONS

- Fast Frequency Hopping Spread Spectrum Radios
- Direct Sequence Spread Spectrum Radios
- Microwave and Satellite Modems
- Test & Measurement Instrumentation
- Military Applications

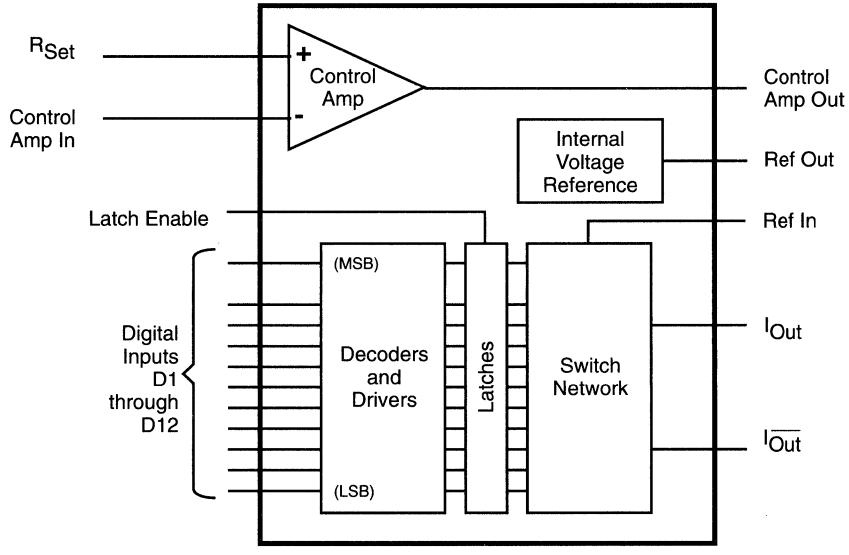
4

GENERAL DESCRIPTION

The SPT9713 is a 12-bit, 100 MWPS digital-to-analog converter designed for direct digital synthesis, high resolution imaging and arbitrary waveform generation applications. This device is pin-for-pin compatible with the AD9713 with significantly improved performance. The SPT9713 is a TTL-compatible device. It features a fast settling time of 8 ns and low glitch impulse energy of 5 pV-s, which results in excellent spurious free dynamic range characteristics.

The SPT9713 is available in 28-lead plastic DIPs and 28-lead PLCCs. Contact the factory for military and /883 package options.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING (Beyond which damage may occur)[1]

Supply Voltages
- Positive Supply Voltage ..... +7 V
- Negative Supply Voltage (V_{EE}) ..... -7 V
- A/D Ground Voltage Differential ..... 0.5 V

Input Voltages
- Digital Input Voltage (D1-D12, Latch Enable) ... 0 V to V_{CC}
- Control Amp Input Voltage Range ..... 0 V to -4 V
- Reference Input Voltage Range (V_{REF}) .... -3.7 V to V_{EE}

Output Currents
- Internal Reference Output Current ..... 500 µA
- Control Amplifier Output Current ..... ±2.5 mA

Temperature
- Operating Temperature ..... -25 to + 85 °C
- Junction Temperature ..... + 150 °C
- Lead, Soldering (10 seconds) ..... + 300 °C
- Storage ..... -65 to + 150 °C

Note: 1. Operation at any Absolute Maximum Ratings is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

$T_A=T_{min}$ - T_{max}, V_{CC}=+5.0 V, V_{EE}=-5.2 V, f_{clock}=100 MHz, 50% clock duty cycle, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
DC Performance						
Resolution				12		Bits
Differential Linearity				±0.5	±0.75	LSB
Differential Linearity	Max at Full Temp.				±1.5	LSB
Integral Linearity	Best Fit			±0.75	±1.0	LSB
Integral Linearity	Max at Full Temp.				±1.75	LSB
Output Capacitance				10		pF
Gain Error	+25 °C			1.0	5.0	% F.S.
Gain Error Tempco				150		PPM/°C
Zero-Scale Offset Error	+25 °C			0.5	2.5	µA
Offset Drift Coefficient				0.01		µA/°C
Compliance Voltage			-1.2		+2.0	V
Equivalent Output Resistance				1.0		kΩ
Input Voltage, Logic			0		V_{CC}	V
Dynamic Performance						
Conversion Rate	(Settling to 0.1%)		100			MWPS
Current Settling Time t_{ST}[1]				8		ns
Delay Time t_D				2		ns
Glitch Energy				5		pV-s
Full Scale Output Current				20.48		mA
Spurious-Free Dynamic Range	+ 25 °C					
1.23 MHz; 10 MWPS	2 MHz Span		70			dBc
5.055 MHz; 20 MWPS	2 MHz Span		72			dBc
10.1 MHz; 50 MWPS	2 MHz Span		68			dBc
16 MHz; 40 MWPS	10 MHz Span		68			dBc
Rise Time / Fall Time	R_L = 50 Ω			2		ns
Power Supply Requirements						
Positive Supply Current (+5.0 V)				8		mA
Negative Supply Current (-5.2 V)	+25 °C			115		mA
Nominal Power Dissipation				640		mW
Power Supply Rejection Ratio				30	100	µA/V

[1]Measured as voltage settling at mid-scale transition to ±0.024%; R_L = 50 Ω.

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ELECTRICAL SPECIFICATIONS

$T_A=T_{min}$ - T_{max}, V_{CC}=+5.0 V, V_{EE}=-5.2 V, f_{clock}=100 MHz, 50% clock duty cycle, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
Voltage Input and Control						
Reference Input Impedance	+25 °C			3		kΩ
Ref. Multiplying Bandwidth	+25 °C			40		MHz
Internal Reference Voltage	+25 °C		-1.15	-1.20	-1.25	V
Internal Reference Voltage Drift	Full			50		ppm/°C
Amplifier Input Impedance				50		kΩ
Amplifier Input Bandwidth				1		MHz
Digital Inputs						
Logic 1 Voltage	Full Temp.		2.0			V
Logic 0 Voltage	Full Temp.				0.8	V
Logic 1 Current	Full Temp.				20	µA
Logic 0 Current	Full Temp.				600	µA
Input Capacitance	+25 °C			3		pF
Input Setup Time - t_S	+25 °C		0.5	-0.3		ns
Input Setup Time - t_S	Full Temp.		0.8			ns
Input Hold Time - t_H	+25 °C		1.8	1.2		ns
Input Hold Time - t_H	Full Temp.		2.0			ns
Latch Pulse Width - t_{PWL}, t_{PWH}	+25 °C			4.0		ns

TEST LEVEL CODES

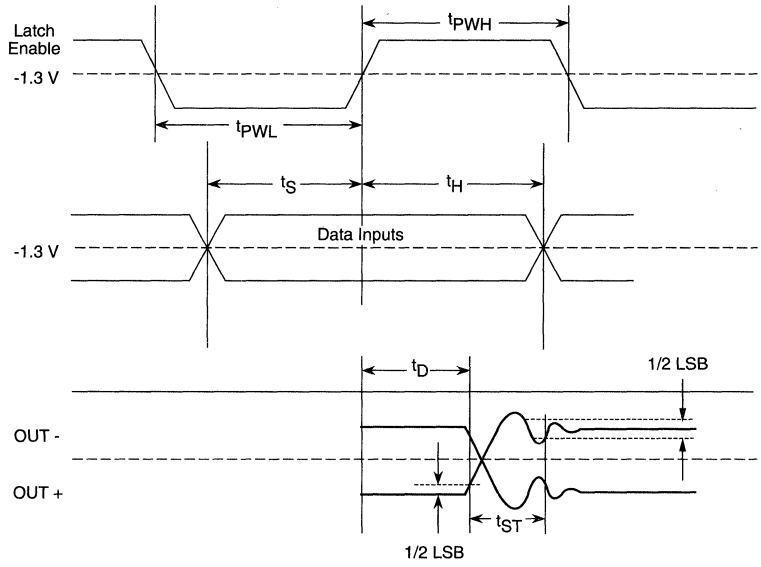
All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests; therefore, $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

Figure 1 - Timing Diagram



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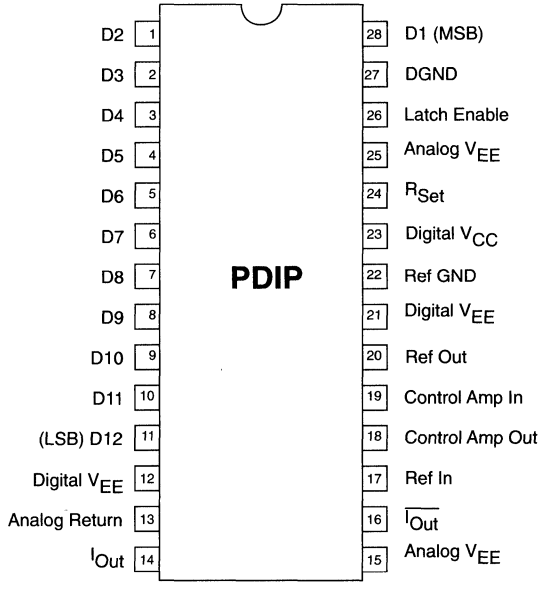
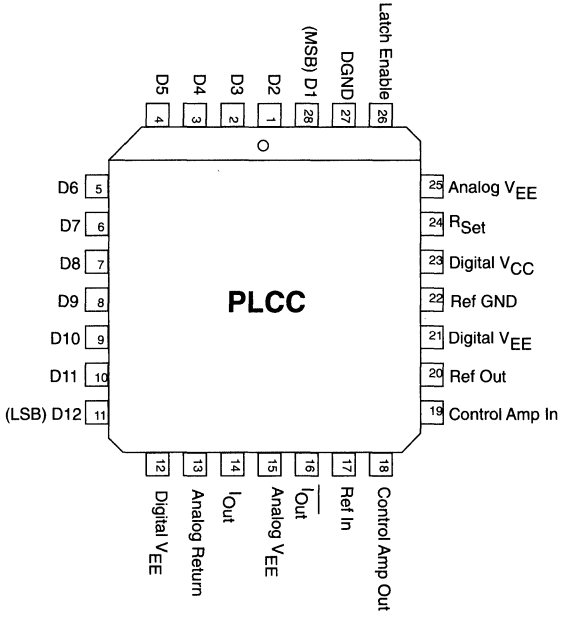
PIN ASSIGNMENTS





PIN FUNCTIONS

Out+	Analog Current Output
Out-	Complementary Analog Current Output
D_1-D_{12}	Digital Input Bits (D_{12} is the LSB)
Latch Enable	Latch Control Line
Ref In	Voltage Reference Input
Ref Out	Internal Voltage Reference Output Normally Connected to Control Amp In
Ref GND	Ground Return For Internal Voltage Reference and Amplifier
Control Amp In	Normally Connected to Ref Out If Not Connected to External Reference
Control Amp Out	Output of Internal Control Amplifier Normally Connected to Ref In
R_{Set}[1]	Connection for External Resistance Reference When Using Internal Amplifier. Nominally 7.5 kΩ
Analog Return	Analog Return Ground
Analog V_{EE}	Analog Negative Supply (-5.2 V)
Digital V_{EE}	Digital Negative Supply (-5.2 V)
Digital V_{CC}	Digital Positive Supply (+5.0 V)
DGND	Digital Ground Return
N/C	Not Connected

[1]Full-Scale Current Out=128 (V_{Ref}/R_{Set})

LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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SIGNAL PROCESSING TECHNOLOGIES

SPT5216

16-BIT ULTRAHIGH SPEED DAC

ADVANCED INFORMATION

FEATURES

- Fast Settling Time - 150 nsec
- Excellent Linearity T. C. 1.5 ppm/°C
- On-Chip Band-Gap Voltage Reference
- On-Chip Application Resistors for Gain Selection
- TTL Compatible Inputs

APPLICATIONS

- High Speed Analog-to-Digital Converters
- Automatic Test Equipment
- Digital Attenuators
- Digital Communication Equipment
- Waveform Generators

4

GENERAL DESCRIPTION

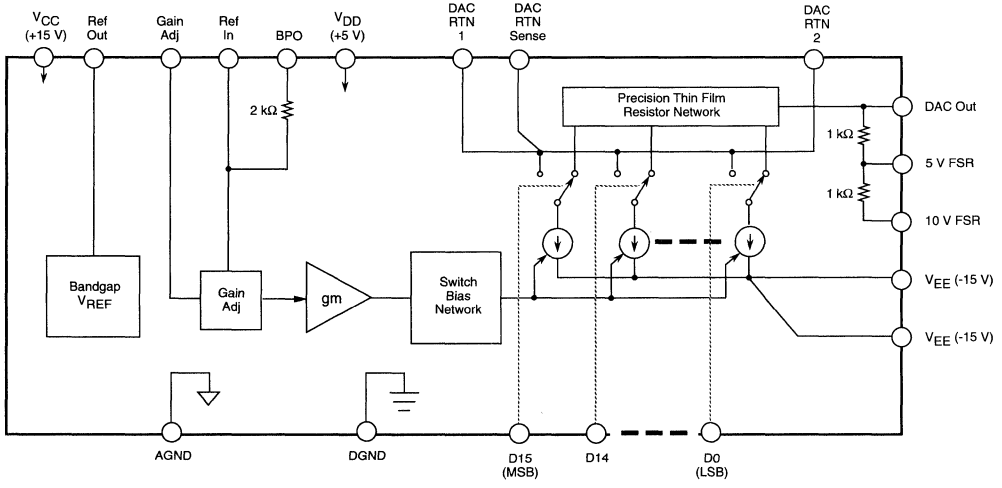
The SPT5216 is a monolithic, high-performance, 16-bit digital-to-analog converter with unmatched speed and accuracy. With its 150 nanosecond settling time, it is the highest speed 16-bit DAC in the industry. Unique features include the band-gap voltage reference and precision application resistors which greatly simplify device application. Unlike other high speed DACs, the SPT5216 can be used in either a current-output or voltage-output mode.

The internal application resistors support output range selections of 0 to +10, 0 to +5, -5 to +5, and -2.5 to +2.5 volts. These internal resistors, used in conjunction with an external op amp, provide current-to-voltage conversion. Because of the high compliance voltage of the DAC output (± 2.5 volts), the SPT5216 can also provide a direct voltage drive into a high impedance load without an external op amp.

The SPT5216 operates with ±15 volt analog supplies, a separate +5 V digital supply and separate analog and digital grounds to provide maximum noise immunity. All logic input levels are TTL and 5 volt CMOS compatible. Laser-trimmed thin film technology ensures accuracy over time and environmental changes.

The device is offered in a 32L DIP package and a 44L cerquad surface-mount package over the commercial temperature range of 0 to 70 °C.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING (Beyond which damage may occur) 25 °C (1)

Supply Voltages

V_{CC} to AGND ..... +18 V
V_{EE} to AGND ..... -18 V
V_{DD} to DGND ..... +6 V
AGND to DGND Differential ..... +0.5 V

Input Voltages

All Digital Inputs to DGND ..... -0.3 V to (V_{DD} +0.3 V)
REF IN to AGND ..... 0 to +10 V

Temperature

Temperature, Ambient ..... 0 to 70 °C
case ..... -60 to +140 °C
junction ..... +150 °C
Lead Temperature (soldering 10 seconds) ..... +300 °C
Storage Temperature ..... -65 to +100 °C

Note: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

T_A = 0 to +70 °C, V_{CC} = 15 V, V_{DD} = 5 V, V_{EE} = -15 V, unless otherwise specified. Minimum air flow is 50 LFPM.

PARAMETER	TEST CONDITIONS	TEST LEVEL	SPT5216B MIN	SPT5216B TYP	SPT5216B MAX	SPT5216C MIN	SPT5216C TYP	SPT5216C MAX	UNIT
ACCURACY SPECIFICATIONS									
Integral Linearity Error	T_A=25 °C	I		±.0015	±.003		±.0015	±.003	%FSR
Integral Linearity Error	T_A=0 to 70 °C	I		±.0045	±.006		±.006	±.012	%FSR
Integral Linearity Drift	Drift	IV		±1.5			±2.0		PPM/°C
Differential Linearity Error	T_A=25 °C	I		±.003	±.006		±.003	±.006	%FSR
Differential Linearity Error	T_A=0 to 70 °C	I		±.009	±.012		±.012	±.024	%FSR
Differential Linearity Drift	Drift	IV		±2.5			±4.0		PPM/°C
Gain Error	T_A=25 °C	I		±.03	±.15		±.03	±.15	%FSR
Gain Error		I		±.08	±.25		±.08	±.25	%FSR
Gain Error Drift		IV		±20			±20		PPM/°C
Unipolar Offset Error	T_A=25°C	I		±.02	±.1		±.02	±.1	%FSR
Unipolar Offset Error		I		±.02	±.3		±.02	±.3	%FSR
Bipolar Offset Error	T_A=25°C	I		±2.5	±10		±2.5	±10	mV
Bipolar Offset Error		I		±5	±15		±5	±15	mV
DAC OUTPUT SPECIFICATIONS									
I_{OUT}		V		5			5		mA
R_{OUT}		V		1			1		kΩ
C_{OUT}	See Figure 1	V		12			12		pF
Output Compliance[2]		V		±2.5			±2.5		V
Output Noise	BW = 1 MHz	V		40			40		µV RMS

Note 1: Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.
Note 2: Accuracy is not guaranteed beyond this limit.

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ELECTRICAL SPECIFICATIONS

T_A = 0 to +70 °C, V_{CC} = 15 V, V_{DD} = 5 V, V_{EE} = -15 V, unless otherwise specified. Minimum air flow is 50 LFPM.

PARAMETER	TEST CONDITIONS	TEST LEVEL	SPT5216B MIN	SPT5216B TYP	SPT5216B MAX	SPT5216C MIN	SPT5216C TYP	SPT5216C MAX	UNIT
DYNAMIC SPECIFICATIONS									
Settling Time	to .0015%	V		150			150		ns
LOGIC SPECIFICATIONS									
V_{IH} 2		I	3.75			3.75			V
V_{IL} 2		I			1.5			1.5	V
I_{IH}		I		2	20		2	20	µA
I_{IL}		I		1	10		1	10	µA
REFERENCE									
Reference Output Voltage	T_A=25 °C	I	4.99	5	5.01	4.99	5	5.01	V
Reference Output Voltage		I	4.98	5	5.02	4.98	5	5.02	V
Max. Reference Output Load3	Total Current	V		8			8		mA
Output Noise4	BW = 1 MHz	V		40			40		µV RMS
POWER SUPPLIES									
V_{CC} Supply		I	14.25	15.00	15.75	14.25	15.00	15.75	V
V_{EE} Supply		I	-14.25	-15.00	-15.75	-14.25	-15.00	-15.75	V
V_{DD} Supply		I	4.75	5.00	5.25	4.75	5.00	5.25	V
V_{CC} Supply Current		I		4	6		4	6	mA
V_{EE} Supply Current		I		20	35		20	35	mA
V_{DD} Supply Current		I		6	9		6	9	mA
Power Dissipation		I		450	660		450	660	mW
PSRR, V_{CC}	+15 V±5%	V		.001			.001		%G/%PS
PSRR, V_{EE}	-15 V±5%	V		.01			.01		%G/%PS
PSRR, V_{DD}	+5 V±5%	V		.001			.001		%G/%PS

Note 3: Reference Load: REF IN = 1 mA BPO = 2.5 mA
Note 4: Reference decoupled as shown in figure 6.

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests; therefore, $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

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GENERAL CIRCUIT DESCRIPTION

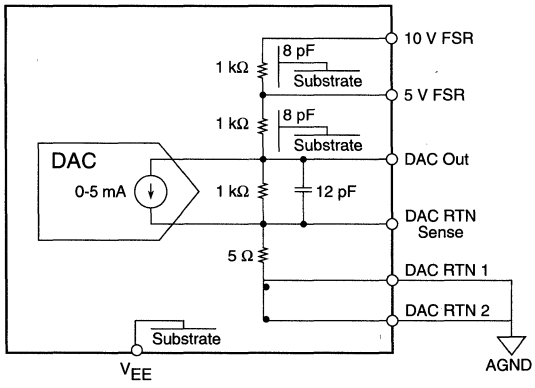
The SPT5216 uses a unique design approach to set a new standard in monolithic DAC performance. It delivers exceptional 16-bit accuracy and stability over temperature and, at the same time, exhibits an extremely fast 150 ns settling time. On chip support functions include a stable band-gap voltage reference and application resistors for output scaling. Inclusion of these functions reduces the external analog component requirements and further increases accuracy. Digital circuitry on the chip is kept to a minimum (limited to the digital inputs), thus minimizing internal noise generation and providing interface flexibility.

DAC CIRCUITRY

The SPT5216 uses current source segmentation for the most significant bits and an R-2R ladder for the least significant bits. The ladder, which consists of a resistor network, successively divides the (remaining) reference current to produce a binary weighted current division. In other words, in moving down the ladder, each 2R resistor leg has half the current flow of the previous leg. Each 2R resistor leg is connected to a current source that is trimmed during manufacturing to provide the 16-bit accuracy. Bipolar switches within each leg are controlled by the respective data bits (pins D0 through D15). When the controlling data bit is low, the 2R resistor leg current is steered to pin DAC OUT. When the data bit is high, the leg current is steered to the DAC RTN pins (DAC RTN 1, and DAC RTN 2), which are externally connected to analog ground.

Figure 1 illustrates the equivalent output circuit of the SPT5216 showing on-chip application resistors and parasitic capacitances.

Figure 1 - Equivalent SPT5216 Output Circuit



APPLICATION INFORMATION

ACTIVE CURRENT-TO-VOLTAGE CONVERSION

In many DAC applications the output current needs to be converted into a usable voltage signal. The most common current-to-voltage configuration for the SPT5216 output is shown in figure 2. Here, an external op amp in conjunction with the internal feedback resistor(s) are used for current-to-voltage (I-to-V) conversion. The op amp provides both a buffered V_{OUT} and maintains DAC OUT at a virtual ground. This way, V_{OUT} can provide up to a 10 volt output swing (using internal feedback resistors) and the output compliance specification (±2.5 volts maximum) is met.

V_{OUT} swing is determined by the feedback resistance. For a 5 volt V_{OUT} swing, the op amp's output is connected to pin 5 V FSR (Full Scale Range) which provides an internal 1 kΩ feedback resistance. A 10 volt V_{OUT} swing is derived by connecting the op amp output to pin 10 V FSR. This feedback connection option is illustrated by the dotted line in figure 2. Properly trimmed (as discussed later), the connections of figure 2 as indicated, would result in the ideal output values as listed in table I.

Figure 2 - Connection of External OP AMP for Active Current-to-Voltage Conversion

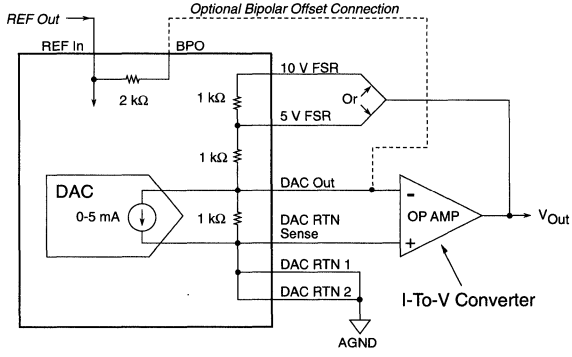


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Table I - Normalized Voltage Values for Programmable Output Ranges (Using Figure 6)

INPUT CODE	OUTPUT VOLTAGE RANGES			
	UNIPOLAR		BIPOLAR	
	5 VOLT	10 VOLT	5 VOLT	10 VOLT
1111 1111 1111 1111	0.00 V	0.00 V	- 2.50 V	- 5.00 V
1111 1111 1111 1110	+ 76.3 µV	+ 152.6 µV	- 2.499924 V	- 4.999846 V
0111 1111 1111 1111	+ 2.500 V	+ 5.00 V	0.00 V	0.00 V
0000 0000 0000 0000	+4.999924 V	+ 9.999846 V	+2.499924 V	+ 4.999846 V

To configure the bipolar output range as indicated in table I, connect the BPO pin to DAC OUT. This connection option is illustrated in figure 2; this offsets the output range by half of the full scale range so that a half-scale digital input value results in a output current value of zero.

The pin connections for the active I-to-V ranges supported by the internal application resistors are summarized in table II.

OPERATIONAL AMPLIFIER SELECTION

Selection of the external op amp involves understanding the final system performance requirements in terms of both speed and accuracy. To maintain the 16-bit accuracy provided by DAC OUT at V_{OUT} shown in figure 2, the op amp open loop gain (Avol) must be 96 dB minimum. Any gain lower than this will contribute an error in the I-to-V conversion circuit. To maintain the 150 ns settling time capability provided by DAC OUT at V_{OUT}, the op amp must have a minimum gain bandwidth of 50 MHz and settling time of less than 100 ns to 0.0015% of full scale.

Table II - Device Pin Connection Summary for Output Range Programming (Active I-to-V Conversion Only)

DEVICE PINS	OUTPUT VOLTAGE RANGES			
	UNIPOLAR		BIPOLAR	
	5 Volt	10 Volt	5 Volt	10 Volt
BPO	Not Connected	Not Connected	Connected To DAC Out	Connected To DAC Out
5 V FSR	Connected To Op Amp Output	Not Connected	Connected To Op Amp Output	Not Connected
10 V FSR	Not Connected	Connected To Op Amp Output	Not Connected	Connected To Op Amp Output

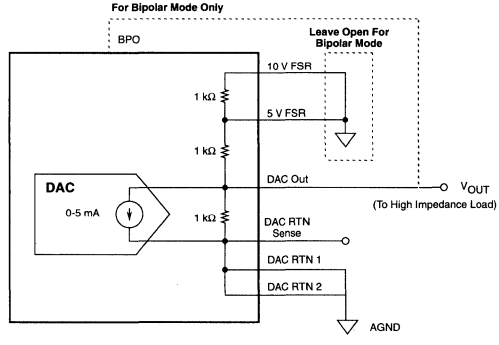
PASSIVE CURRENT-TO-VOLTAGE CONVERSION

Because of the SPT5216's high voltage compliance, a voltage output can be derived directly at DAC OUT in a method suitable for some applications. By driving a load resistor directly with the current from DAC OUT, a voltage drop results producing V_{OUT}. An example of this implementation is shown in figure 3, where an internal feedback resistor is used as the load 10 V FSR is grounded to optimize settling time. By utilizing all internal resistors, this circuit offers optimized stability and matching.

Output current from the DAC ranges between 0 and 5 mA, which corresponds to an input code of all 1s and all 0s, respectively. For unipolar mode, the net 500 Ω load of figure 3 results in a -2.5 to 0 volt output range. For bipolar mode, the output voltage range is from +1.67 V to -1.67 V (typical). Both output ranges are within the specified output compliance limits. An external load resistor could also be used with this circuit, however, there are difficulties with this arrangement: thermal tracking is not optimum, and the gain adjustment required to overcome the absolute internal resistance and DAC output current errors is beyond the correction range provided by the trim circuit. This is described later.

Note that the input resistance of the circuit driven by V_{OUT} will be placed in parallel with the load resistor. This limits the application of figure 3 to high impedance loads. Also note that if a buffer (or other active circuit) is used at V_{OUT} in figure 3, that circuit's CMRR must be at least 100 dB to maintain the DAC's accuracy. This is an advantage of the active current-to-voltage configuration shown in figure 2, where the input of the op amp is always at virtual ground.

Figure 3 - Connection of Internal Load Resistors for Passive Unipolar/Bipolar Current-to-Voltage Conversion

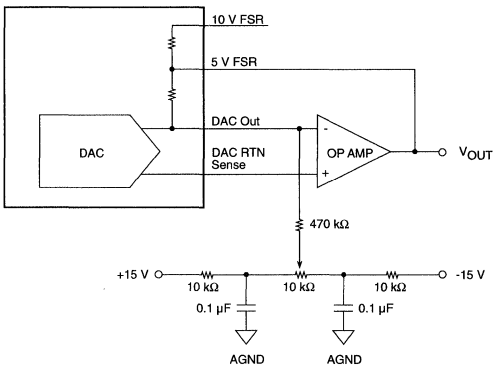


OUTPUT OFFSET COMPENSATION

Although the zero offset error of the SPT5216 is within ±0.1% of the full scale range, some applications require better accuracy. The offset trim network of figure 4 shown connected to DAC OUT allows offset adjustment in excess of ±0.2%. This trim network can be used for the active I-to-V conversion network of figure 2 or the passive circuit of figure 3. When using an external op amp as in figure 2, optimum offset stability may be achieved by using the nulling network recommended by the op amp's manufacturer.

Although accuracy of the offset network components is not important, temperature tracking of the resistor and potentiometer values will affect offset trim stability. The resistors and potentiometer should have a low temperature coefficient and the potentiometer should be a high quality, multi-turn component to ensure minute adjustability and stability over time and temperature. The 0.1 µF capacitors shown (typically ceramic) are used to decouple power supply noise from the DAC output circuit.

Figure 4 - Offset Compensation



LOGIC INTERFACE

Because of the low logic input current specification, most TTL families will adequately drive the SPT5216, even though minimum V_{IH} is specified at 3.75 volts, a figure relatively high by TTL standards. Nonadherence to the V_{IH} specification can result in a less than specified DAC accuracy. High-speed CMOS logic (HC) or High-speed CMOS logic with TTL compatible inputs (HCT) are directly compatible with the SPT5216 logic inputs.

GAIN ADJUSTMENT

With the gain error of the SPT5216 pre-trimmed to within ±0.15% of full scale accuracy, many applications require external gain adjustments. Configuration of the external gain adjustment network is shown is figure 5. The adjustment potentiometer is connected between two low noise voltage sources, REF OUT and AGND, as shown. The two bypass capacitors shown further help to eliminate noise. Because of the voltage source asymmetry in relationship to the potentiometer wiper, the adjustment range is an asymmetric -0.6% to +1%. This adjustment range does sufficiently compensate for the error of the device, and the network will work for any type of output configuration. The adjustment range can be made larger and symmetrical by using a circuit similar to the offset compensation network as shown in figure 4, but with the consequence of introducing power supply noise (and power supply variations) into the vital voltage reference circuit.

The selection criteria for the gain adjustment network components is similar to those described for the offset compensation network. Accuracy is not as important as temperature stability.

Figure 5 - Gain Trim Network Suitable for All Output Configurations

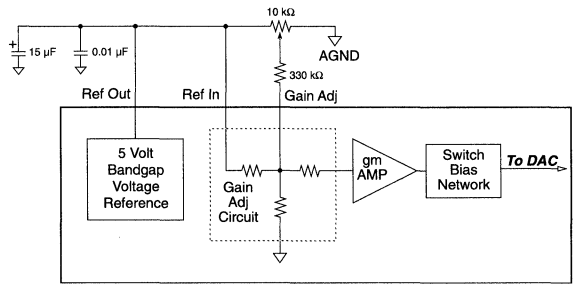


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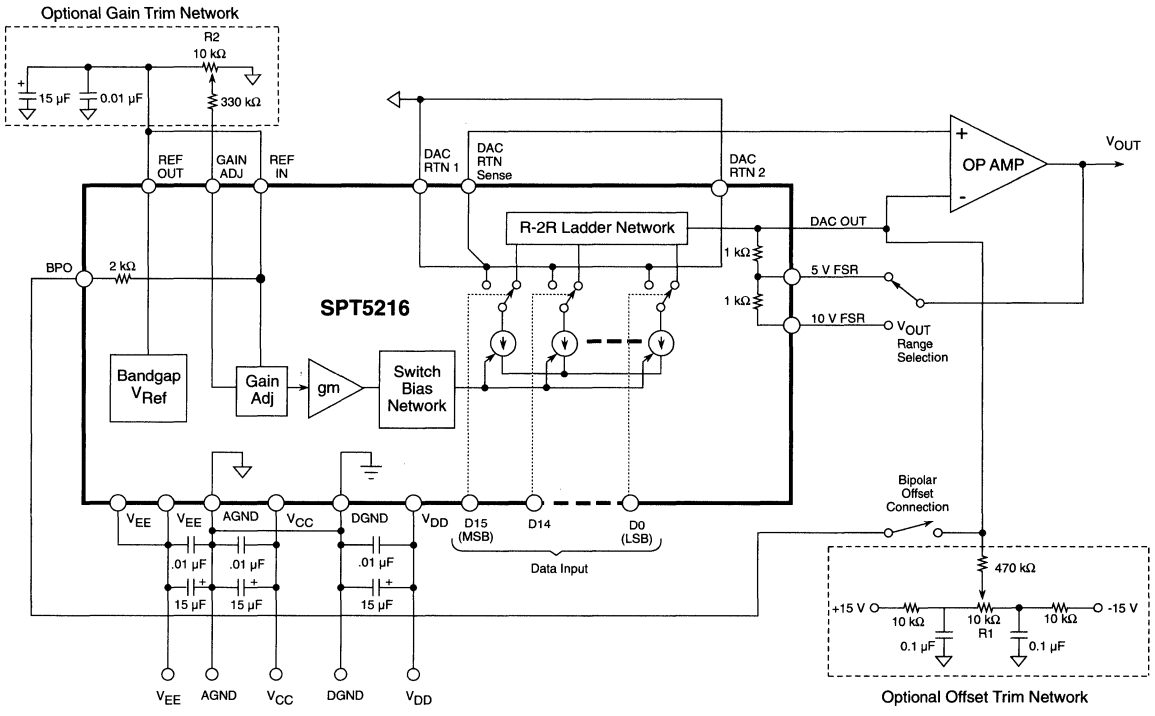
Figure 6 - Typical SPT5216 Application Circuit



OFFSET AND GAIN CALIBRATION PROCEDURE

This calibration procedure is only applied to the I-to-V applications as shown in figure 6.

The calibration consists of adjusting the V_{OUT} most negative voltage to its ideal value for the offset adjustment and adjusting the most positive V_{OUT} to its ideal value for gain adjustment. The offset and gain errors listed in the specifications for both unipolar and bipolar operation may be adjusted to zero using R1 and R2 (see figure 6) respectively. All components in the optional offset trim network and optional gain trim network shown in figure 6 should have a low temperature coefficient. The potentiometers (R1 and R2) should be multi-turn components to ensure minute adjustability.

If the adjustment is not needed, remove the optional offset trim network from the circuit.

Unipolar

The first step is offset adjustment. Set the input code to 1111 1111 1111 1111 and adjust R1 until V_{OUT} reads zero volts for either 5 V FSR operation or 10 V FSR operation.

Next is the gain adjustment. Set the input code to 0000 0000 0000 0000 and adjust R2 until V_{OUT} reads +4.999924 volts for 5 V FSR operation or +9.999846 volts for 10 V FSR operation.

Bipolar

For the Bipolar mode of operation, start the calibration by adjusting the offset. Set the input code to 1111 1111 1111 1111 and adjust R1 until V_{OUT} reads -2.50000 volts for 5 V FSR or -5.00000 volts for 10 V FSR operation. The gain error calibration is done by setting the input code to 0000 0000 0000 0000 and adjusting R2 until V_{OUT} reads +2.499924 V for 5 V FSR operation or +4.999848 volts for 10 V FSR operation.

CIRCUIT LAYOUT CONSIDERATIONS

In any analog system design, care must be taken in the circuit layout process. The design of a high-speed, 16-bit analog system offers an exceptional challenge. The integrity of the system's power supply and grounding is critical and, as with any precision analog component, good decoupling is needed directly at the device. Analog signal traces must be routed in a manner to minimize coupling from potential noise sources. With a 5 volt full-scale output voltage range, a mere 38 μVp-p noise level is equivalent to 1/2 LSB. Low amplitude noise such as this is virtually impossible to eliminate without totally shielding the analog circuit portion.

The power supply must be a well-regulated, noise-free analog voltage source. As with any analog device, the PSRR performance of the SPT5216 degrades with higher frequency components. Logic noise in the supply or ground line contains high frequency components, so separate supplies and ground returns are recommended for the analog and logic portions of the system. Radiated noise from digital signal traces and power supply traces must also be avoided. Completely shield the analog circuit portion from digital circuitry and digital power supplies and ground. A separate analog ground plane near the device should be used to shield the digital data lines going into the device; this plane should have a trace that completely surrounds the digital inputs, if possible. If an analog ground plane is used with the device for shielding, keep the space between the digital ground plane and analog ground plane wide to prevent capacitive coupling. The best analog ground plane is one with the least resistance, i.e., the minimum total "squares" of surface area, regardless of size. All device grounding should be to the analog ground plane, except for the GND RTN pins which should be tied to the plane at one connection point only.

Figure 6 shows the implementation of decoupling devices (0.01 μF and 15 μF in parallel) at pin REF OUT. These devices should be connected to the analog ground and their incorporation will minimize the overall D/A conversion noise.

Since virtually all the interfacing to the SPT5216 is analog in nature (the logic inputs are actually analog current switches), DGND and AGND should be tied together at the device and treated as an analog ground. This analog ground and the system's digital ground should be inter-tied only at a single point which has a low impedance path back to the system's power supplies. This will prevent modulation of the analog ground by digital power supply currents as well as digital noise injection.

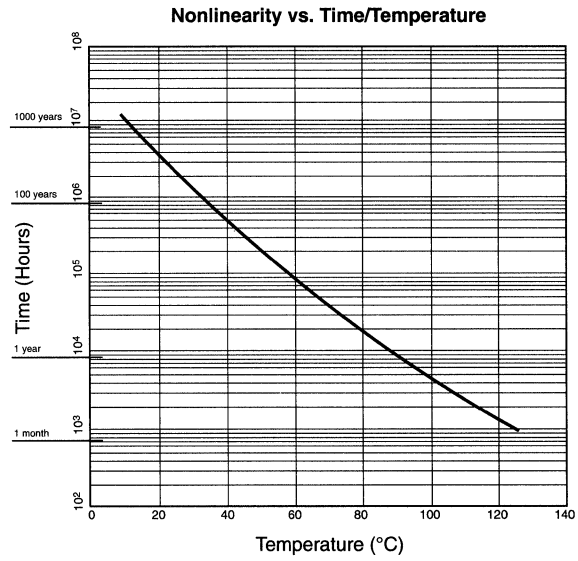
The external components should be connected to the SPT5216 with minimum length leads to help prevent noise coupling. The inputs of the external op amp are especially sensitive, so they should have short traces and be well shielded.

To the circuit driven by the SPT5216, a voltage drop in the common analog ground will appear as a voltage offset. To avoid this, the SPT5216 includes a DAC SENSE pin which can be used for remote ground potential sensing.

LONG-TERM STABILITY VERSUS TEMPERATURE

As with all high speed, high resolution digital-to-analog converters, the initial accuracy of the device will degrade with both time and temperature. The graph shown in figure 7 can be used to determine the expected change in linearity performance over time when the device is operated at various ambient temperatures. This graph shows how long it will take for the SPT5216 linearity to change by 8 ppm (or 1/2 LSB) at any operating temperature. The curve shown is valid for both integral nonlinearity (ILE) and differential nonlinearity (DLE) changes.

Figure 7 - Linearity Performance over Time



Expected time required to produce an 8 ppm (1/2 LSB) linearity (ILE or DLE) shift as a function of temperature.

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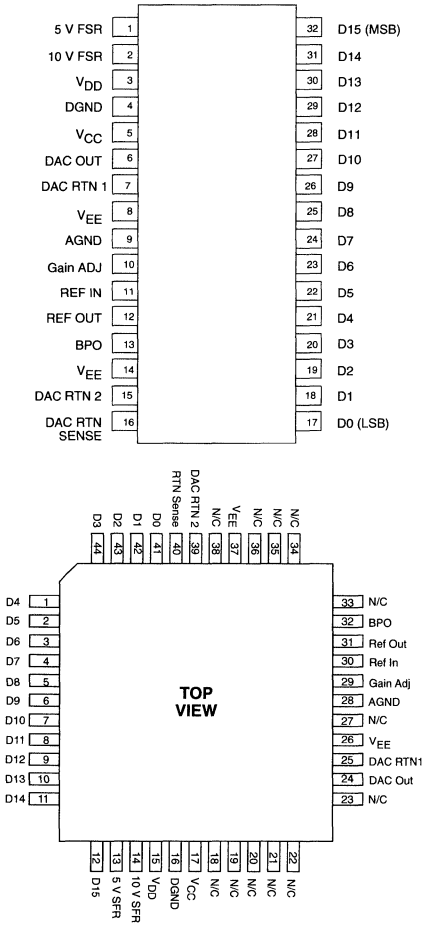
PIN ASSIGNMENTS



PIN FUNCTIONS

NAME	FUNCTION
5 V FSR	Output range scaling application resistor
10 V FSR	Output range scaling application resistor
V_{DD}	+5 volt power supply connection
DGND	Digital ground connection
V_{CC}	+15 volt power supply connection
DAC OUT	Analog current output of DAC
DAC RTN 1	DAC ground current return path
V_{EE}	-15 volt power supply connection
AGND	Analog ground connection
Gain ADJ	Input reference trim adjustment
REF IN	Input for internal or external reference
REF OUT	Output of internal reference
BPO	Output offsetting application resistor
V_{EE}	-15 volt power supply connection
DAC RTN 2	DAC ground current return path
DAC RTN Sense	DAC ground current sense connection
D0	Input data bit 0 (LSB)
D1-14	Input data bit 1-14
D15	Input data bit 15 (MSB)

LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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Section 5 Comparators

5

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SIGNAL PROCESSING TECHNOLOGIES

HCMP96850

SINGLE ULTRA FAST VOLTAGE COMPARATOR

FEATURES

- Propagation Delay of 2.4 ns (typ)
- Propagation Delay Skew <300 ps
- Low Offset ±3 mV
- Latch Control

APPLICATIONS

- High Speed Instrumentation, ATE
- High Speed Timing
- Window Comparators
- Line Receivers
- A/D Conversion
- Threshold Detection

GENERAL DESCRIPTION

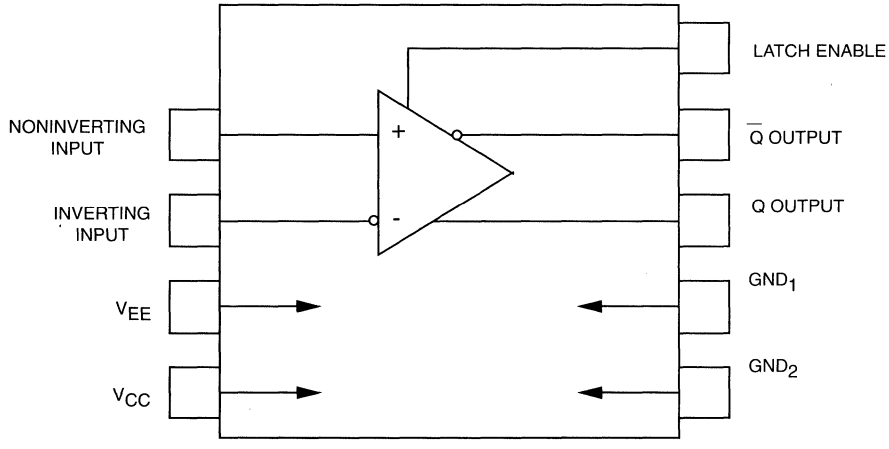
The HCMP96850 is a single, very high speed monolithic comparator. It is pin-compatible with and has improved performance over the AD9685 and the AM6685. The HCMP96850 is designed for use in Automatic Test Equipment (ATE), high speed instrumentation, and other high speed comparator applications.

Improvements over other sources include reduced power consumption, reduced propagation delays, and higher input impedance.

The HCMP96850 is available in a 16 lead cerdip and in die form.

5

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages
- Positive Supply Voltage (V_{CC} to GND) ..... -0.5 to +6.0 V
- Negative Supply Voltage (V_{EE} to GND) ... -6.0 to +0.5 V
- Ground Voltage Differential ..... -0.5 to +0.5 V

Input Voltages
- Input Voltage ..... -4.0 to +4.0 V
- Differential Input Voltage ..... -5.0 to +5.0 V
- Input Voltage, Latch Controls ..... V_{EE} to 0.5 V

Output
- Output Current ..... 30 mA

Temperature
- Operating Temperature, ambient ..... -25 to +85 °C
- junction ..... +150 °C
- Lead Temperature, (soldering 60 seconds) ..... +300 °C
- Storage Temperature ..... -65 to +150 °C

Note: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

T_A = +25 °C, V_{CC} = +5.0 V ±.25 V, V_{EE} = -5.2 V ±.3 V, R_L = 50 Ohms, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS						
Input Offset Voltage	R_S = 0 Ohms	IV	-3		+3	mV
Input Offset Voltage (V_{os})	R_S = 0 Ohms, $T_{MIN} < T_A < T_{MAX}$	IV	-3.5		+3.5	mV
(V_{os}) Tempco		V		4		µV/°C
Input Bias Current		I		4	±20	µA
Input Bias Current	$T_{MIN} < T_A < T_{MAX}$	IV		7		µA
Input Offset Current		I	-1.0		+1.0	µA
Input Offset Current	$T_{MIN} < T_A < T_{MAX}$	IV	-1.5		+1.5	µA
Positive Supply Current		I		3.3	5	mA
Negative Supply Current		I		13.5	18	mA
Common Mode Range		I	-2.5		+2.5	V
Open Loop Gain		V		4000		V/V
Input Resistance		V		60		kΩ
Input Capacitance		V		3		pF
Input Capacitance	(LCC Package)	V		1		pF
Power Supply Sensitivity	V_{CC} and V_{EE}	V		70		dB
Common Mode Rejection Ratio		V		80		dB
Power Dissipation	I_{OUTPUT} = 0 mA	IV		90	120	mW

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ELECTRICAL SPECIFICATIONS

T_A = +25 °C, V_{CC} = +5.0 V ±.25 V, V_{EE} = -5.2 V ±.3 V, R_L = 50 Ohms, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS	
OUTPUT LOGIC LEVELS (ECL 10 KH Compatible)							
Output High	50 Ohms to -2 V	I	-.98			-.81	V
Output Low	50 Ohms to -2 V	I	-1.95			-1.63	V
AC ELECTRICAL CHARACTERISTICS[1]							
Propagation Delay	10 mV O.D.	III			2.4	3.0	ns
Latch Set-up Time		IV			0.6	1	ns
Latch to Output Delay	50 mV O.D.	IV				3	ns
Latch Pulse Width		V			2		ns
Latch Hold Time		IV				0.5	ns
Rise Time	20% to 80%	V			1.76		ns
Fall Time	20% to 80%	V			1.76		ns

Note 1: 100 mV input step

5

TEST LEVEL CODES

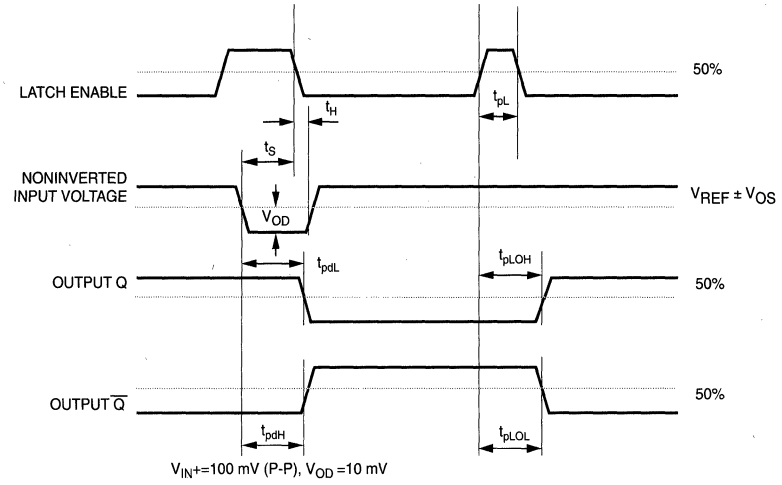
All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests; therefore, $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

Figure 1 - Timing Diagram



The set-up and hold times are a measure of the time required for an input signal to propagate through the first stage of the comparator to reach the latching circuitry. Input signal changes occurring before t_S will be detected and held; those occurring after t_H will not be detected. Changes between t_S and t_H may or may not be detected.

SWITCHING TERMS (Refer to figure 1)

t_{pdH} INPUT TO OUTPUT HIGH DELAY - The propagation delay measured from the time the input signal crosses the input reference voltage (± the input offset voltage) to the 50% point of an output LOW to HIGH transition.

t_{pdL} INPUT TO OUTPUT LOW DELAY - The propagation delay measured from the time the input signal crosses the input reference voltage (± the input offset voltage) to the 50% point of an output HIGH to LOW transition.

t_{pLOH} LATCH ENABLE TO OUTPUT HIGH DELAY - The propagation delay measured from the 50% point of the Latch Enable signal LOW to HIGH transition to 50% point of an output LOW to HIGH transition.

V_{OD} VOLTAGE OVERDRIVE - The difference between the input and reference input voltages.

t_{pLOL} LATCH ENABLE TO OUTPUT LOW DELAY - The propagation delay measured from the 50% point of the Latch Enable signal LOW to HIGH transition to the 50% point of an output HIGH to LOW transition.

t_H MINIMUM HOLD TIME - The minimum time after the negative transition of the Latch Enable signal that the input signal must remain unchanged in order to be acquired and held at the outputs.

t_{pL} MINIMUM LATCH ENABLE PULSE WIDTH - The minimum time that the Latch Enable signal must be HIGH in order to acquire an input signal change.

t_S MINIMUM SET-UP TIME - The minimum time before the negative transition of the Latch Enable signal that an input signal change must be present in order to be acquired and held at the outputs.

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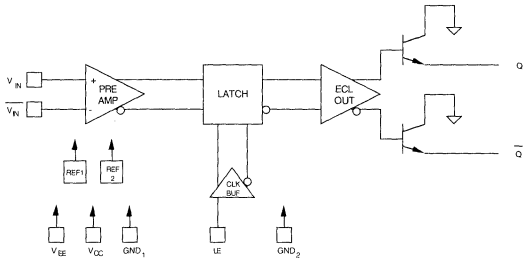
Figure 2 - Internal Function Diagram



GENERAL INFORMATION

The HCMP96850 is an ultra high speed single voltage comparator. It offers tight absolute characteristics which guarantee matching from package to package. The device has differential analog inputs and complementary logic outputs compatible with ECL systems. The output stage is adequate for driving terminated 50 Ohm transmission lines.

The HCMP96850 has one latch enable control and can be driven by standard ECL logic. It also has two separate ground pins, one for the output to accommodate large ground currents without affecting the rest of the circuit, while the other is for the small signal intermediate stages. The input stage is referenced to V_{CC} and V_{EE}.

This comparator offers the following improvements over existing devices:

- Short propagation delays
- Low offset voltage and temperature coefficient
- Low power
- Minimal thermal tails
- Does not oscillate

All of these features combined produce high performance products with timing stability and repeatability for large system precision.

TYPICAL INTERFACE CIRCUIT

A typical interface circuit using the comparator is shown in figure 3. Although it needs few external components and is easy to apply, there are several considerations that should be noted to achieve optimal performance. The very high operating speeds of the comparator require careful layout, decoupling of supplies, and proper design of transmission lines.

Since the HCMP96850 comparator is a very high frequency and high gain device, certain layout rules must be followed to avoid spurious oscillations. The comparator should be soldered to the board with component lead lengths kept as short as possible. A ground plane should be used, while the input impedance to the part is kept as low as possible, to decrease parasitic feedback. If the output board traces are longer than approximately one-half inch, microstripline techniques must be employed to prevent ringing on the output waveform. Also, the microstriplines must be terminated at the far end of the characteristic impedance of the line to prevent reflections. The HCMP96850 is capable of driving 50 Ohm terminated lines. The termination can be directly tied to -2.0 V or a Thevenin equivalent terminated to the negative supply if a -2.0 V supply is not available. Both supply voltage pins should be decoupled with high frequency capacitors as close to the device as possible.

All pins designated N/C should be soldered to ground for additional noise immunity and interelectrode shielding. All ground pins should be connected to the same ground plane.

The timing diagram for the comparator is shown in figure 1. The latch enable (LE) pulse is shown at the top. If LE is high in the HCMP96850, the comparator tracks the input difference voltage. When LE is driven low, the comparator outputs are latched into their existing logic states.

The leading edge of the input signal (which consists of 10 mV overdrive) changes the comparator output after a time of t_{pdL} or t_{pdH} (Q or $\overline{Q}$). The input signal must be maintained for a time t_S (set-up time) before the latch enable falling edge and held for time t_H after the falling edge for the comparator to accept data. After t_H, the output ignores the input status until the latch is strobed again. A minimum latch pulse width of t_{pL} is needed for strobe operation, and the output transitions occur after a time of t_{pLOH} or t_{pLOL}.

Unused outputs must be terminated with 50 Ohms to ground while unused latch enable pins should be connected directly to ground.

Figure 3 - Typical Interface Circuit

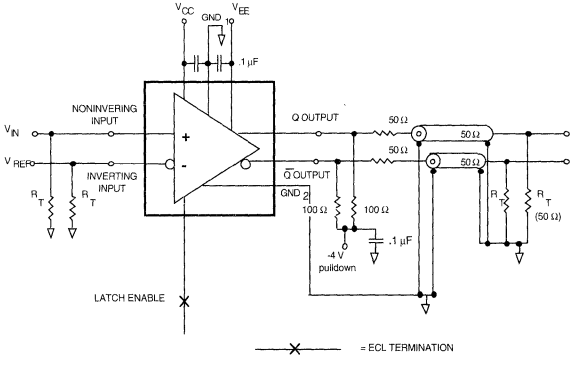


Figure 4 - Equivalent Input Circuit

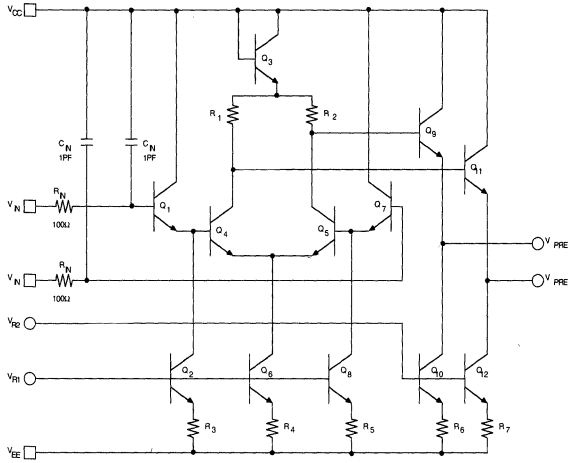


Figure 5 - Output Circuit

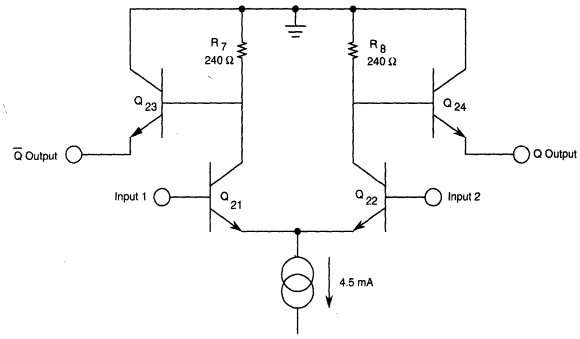


Figure 6 - Test Load

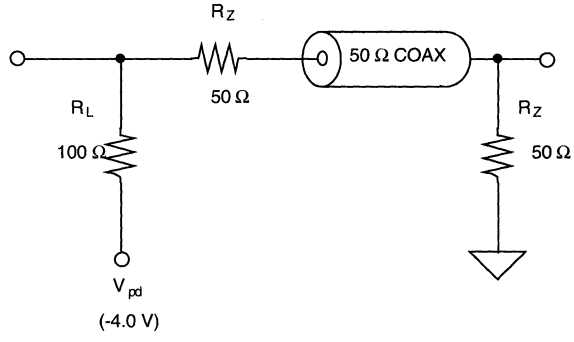
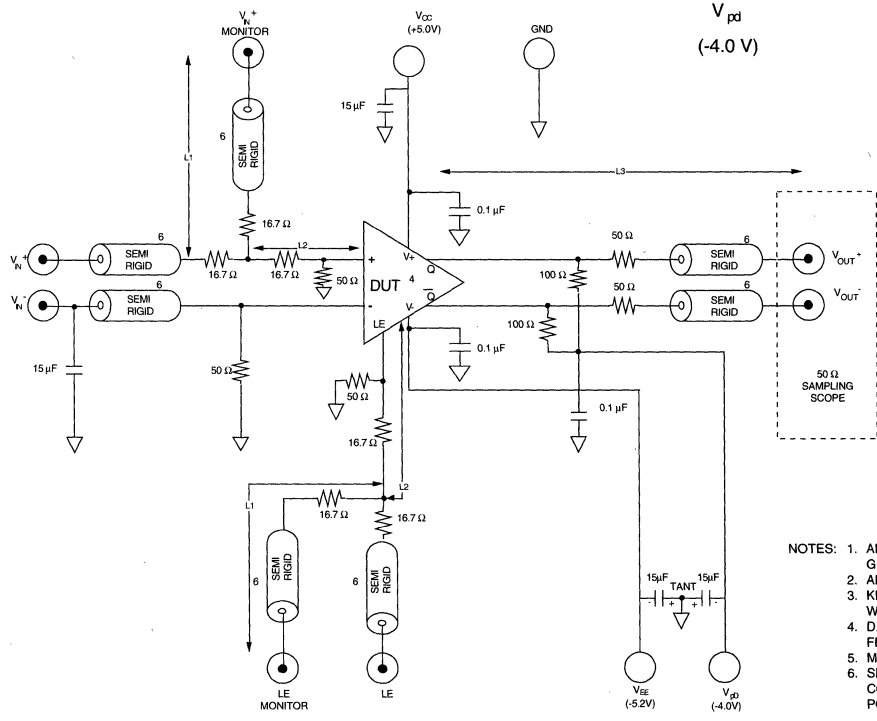


Figure 7 - AC Test Fixture



NOTES:
1. ALL BNC & SEMIRIGID COAX SHIELD ARE GROUNDED.
2. ALL RESISTORS 1% (10 Ω = 49.9 Ω).
3. KEEP ALL LEADS AS SHORT AS POSSIBLE WITH ELECTRICAL LENGTHS L1 = L2 + L3.
4. D.U.T. PLUGS INTO A 16 PIN HIGH FREQUENCY PIN SOCKET.
5. MONITOR INPUT IMPEDANCE 50 Ω TO GND.
6. SEMIRIGID COAX SHIELD SHOULD BE CONNECTED AS CLOSE TO THE DEVICE AS POSSIBLE.

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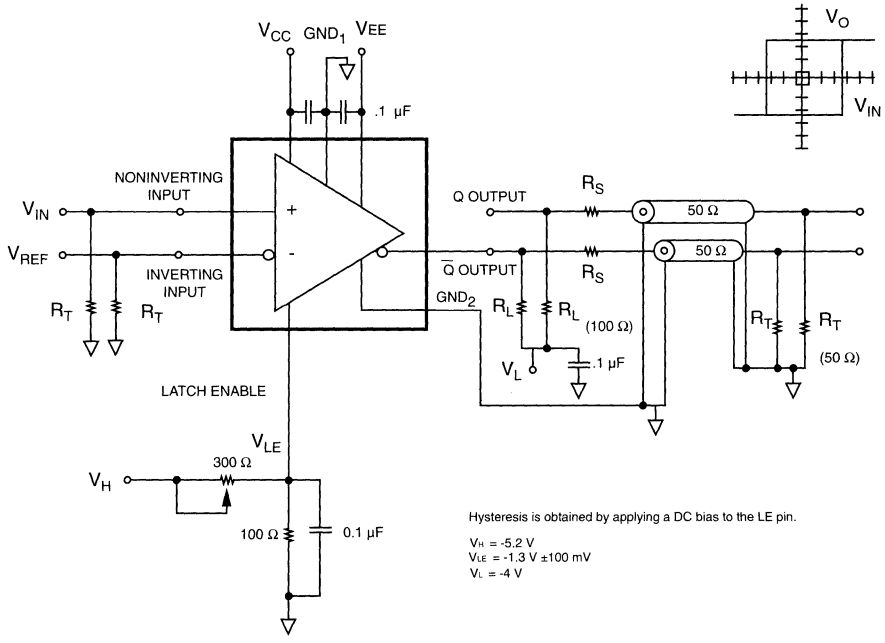
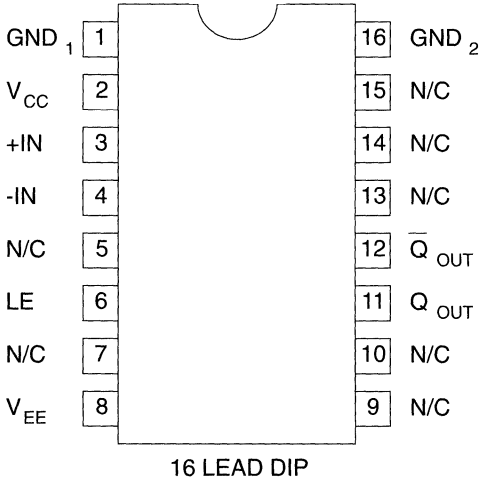
Figure 8 - HCMP96850 with Hysteresis



PIN ASSIGNMENTS



16 LEAD DIP

PIN FUNCTIONS

NAME	FUNCTION
GND_1	Circuit Ground
V_{CC}	Positive Supply Voltage
+IN	Noninverting Input
-IN	Inverting Input
N/C	No Connection
LE	Latch Enable
V_{EE}	Negative Supply Voltage
Q_{OUT}	Output
$\overline{Q}_{OUT}$	Inverted Output
GND_2	Output Ground

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LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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SIGNAL PROCESSING TECHNOLOGIES

SPT9687

DUAL ULTRA FAST VOLTAGE COMPARATOR

FEATURES

- Propagation Delay <2.3 ns
- Propagation Delay Skew <300 ps
- 300 MHz Minimum Tracking Bandwidth
- Low Offset ±3 mV
- Low Feedthrough and Crosstalk
- Differential Latch Control

APPLICATIONS

- High Speed Instrumentation, ATE
- High Speed Timing
- Window Comparators
- Line Receivers
- A/D Conversion
- Threshold Detection

GENERAL DESCRIPTION

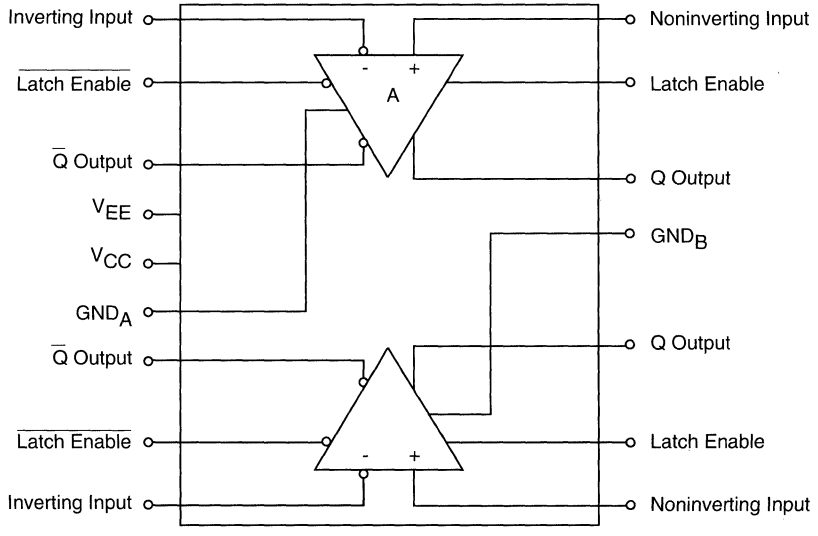
The SPT9687 is a dual, very high speed monolithic comparator. It is pin compatible with, and has improved performance over AMD's AM6687 and Analog Device's AD9687. The SPT9687 is designed for use in Automatic Test Equipment (ATE), high speed instrumentation, and other high speed comparator applications.

Improvements over other sources include reduced power consumption, reduced propagation delays, and higher input impedance.

The SPT9687 is available in an industrial temperature range in a 16-lead cerdip, 16-lead PDIP, 20-contact leadless chip carrier (LCC), 20-lead PLCC, 16-lead sidebrazed, and die form.

5

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages
- Positive Supply (V_{CC} to GND) ..... -0.5 to +6.0 V
- Negative Supply (V_{EE} to GND) ..... -6.0 to +0.5 V
- Ground Voltage Differential ..... -0.5 to +0.5 V

Input Voltages
- Input Voltage ..... -4.0 to +4.0 V
- Differential Input Voltage ..... -5.0 to +5.0 V
- Input Voltage, Latch Controls ..... V_{EE} to 0.5 V

Output
- Output Current ..... 30 mA

Temperature
- Operating Temperature, ambient ..... -25 to +85 °C
- junction ..... +150 °C
- Lead Temperature, (soldering 60 seconds) ..... +300 °C
- Storage Temperature ..... -65 to +150 °C

Note: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

T_A = +25 °C, V_{CC} = +5.0 V, V_{EE} = -5.20 V, R_L = 50 Ohm, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS						
Input Offset Voltage	R_S = 0 Ohms	III	-3	±.5	+3	mV
Input Offset Voltage	R_S = 0 Ohms, $T_{MIN} < T_A < T_{MAX}$	IV	-3.5		+3.5	mV
Offset Voltage Tempco		V		4		µV/°C
Input Bias Current		I		6	±20	µA
Input Bias Current	$T_{MIN} < T_A < T_{MAX}$	IV		7	±38	µA
Input Offset Current		I	-1.0		+1.0	µA
Input Offset Current	$T_{MIN} < T_A < T_{MAX}$	IV	-1.5		+1.5	µA
Common Mode Range		I	-2.5		+2.5	V
Open Loop Gain		V		4000		V/V
Input Resistance		V		60		kΩ
Input Capacitance		V		3		pF
Input Capacitance	(LCC Package)	V		1		pF
Power Supply Sensitivity	V_{CC} and V_{EE}	IV	50	100		dB
Common Mode Rejection Ratio		IV	50	85		dB
Positive Supply Current		I		7	11	mA
Negative Supply Current		I		27	37	mA
Positive Supply Voltage		I	4.75	5.0	5.25	V
Negative Supply Voltage		I	-4.95	-5.2	-5.45	V
Power Dissipation	I_{OUTPUT} = 0 mA	I		185	250	mW
OUTPUT LOGIC LEVELS (ECL 10 KH Compatible)						
Output High	50 Ohms to -2 V	I	-.98		-.81	V
Output Low	50 Ohms to -2 V	I	-1.95		-1.63	V

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ELECTRICAL SPECIFICATIONS

T_A = +25 °C, V_{CC} = +5.0 V, V_{EE} = -5.20 V, R_L = 50 Ohm, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
AC ELECTRICAL CHARACTERISTICS[1]						
Propagation Delay	10 mV OD	III		2.0	2.3	ns
Latch Set-up Time		IV		0.6	1	ns
Latch to Output Delay	50 mV OD	IV			3	ns
Latch Pulse Width		V		2		ns
Latch Hold Time		IV			0.5	ns
Rise Time	20% to 80%	V		1.2		ns
Fall Time	20% to 80%	V		1.2		ns
Min Clock Rate		V		300		MHz

Note 1. 100 mV input step.

5

TEST LEVEL CODES

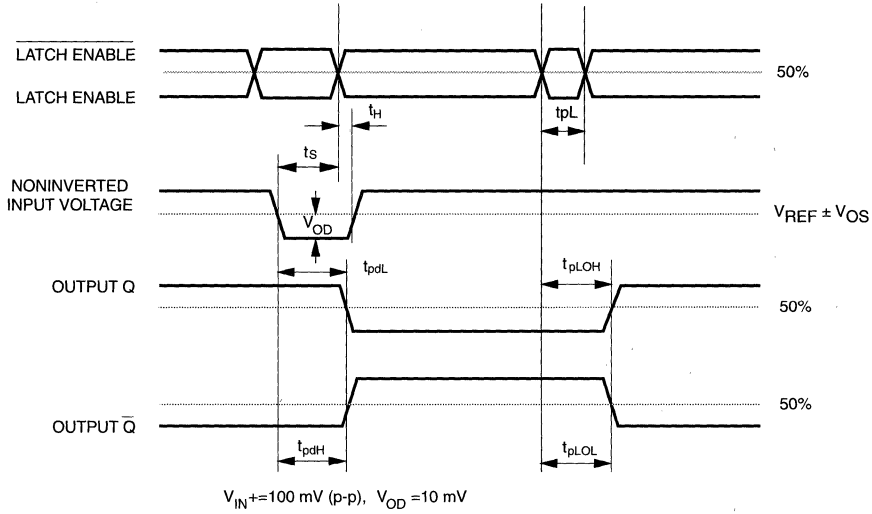
All electrical characteristics are subject to the following conditions:

All parameters having Min./Max. specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests, therefore $T_j = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A = 25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.

Figure 1 - Timing Diagram



V_{IN}+=100 mV (p-p), V_{OD} =10 mV

The set-up and hold times are a measure of the time required for an input signal to propagate through the first stage of the comparator to reach the latching circuitry. Input signals occurring before t_S will be detected and held; those occurring after t_H will not be detected. Changes between t_S and t_H may not be detected.

SWITCHING TERMS (Refer to figure 1)

t_{pdH} INPUT TO OUTPUT HIGH DELAY - The propagation delay measured from the time the input signal crosses the reference voltage (± the input offset voltage) to the 50% point of an output LOW to HIGH transition.

t_{pdL} INPUT TO OUTPUT LOW DELAY - The propagation delay measured from the time the input signal crosses the reference voltage (± the input offset voltage) to the 50% point of an output HIGH to LOW transition.

t_{pLOH} LATCH ENABLE TO OUTPUT HIGH DELAY - The propagation delay measured from the 50% point of the Latch Enable signal LOWto HIGH transition to 50% point of an output LOW to HIGH transition.

V_{OD} VOLTAGE OVERDRIVE - The difference between the input and the reference voltages.

t_{pLOL} LATCH ENABLE TO OUTPUT LOW DELAY - The propagation delay measured from the 50% point of the Latch Enable signal LOW to HIGH transition to the 50% point of an output HIGH to LOW transition.

t_H MINIMUM HOLD TIME - The minimum time after the negative transition of the Latch Enable signal that the input signal must remain unchanged in order to be acquired and held at the outputs.

t_{pL} MINIMUM LATCH ENABLE PULSE WIDTH - The minimum time that the Latch Enable signal must be HIGH in order to acquire an input signal change.

t_S MINIMUM SET-UP TIME - The minimum time before the negative transition of the Latch Enable signal that an input signal change must be present in order to be acquired and held at the outputs.

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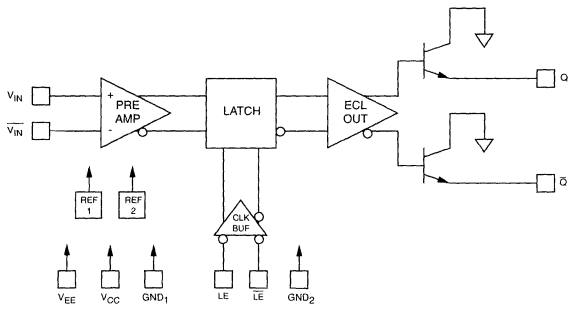
Figure 2 - Internal Functional Diagram



GENERAL INFORMATION

The SPT9687 is an ultra high speed dual voltage comparator. It offers tight absolute characteristics. The device has differential analog inputs and complementary logic outputs compatible with ECL systems. The output stage is adequate for driving terminated 50 ohm transmission lines.

The SPT9687 has a complementary latch enable control for each comparator. Both can be driven by standard ECL logic.

The dual comparator shares the same V_{CC} and V_{EE} connections but have separate grounds for each comparator to achieve high crosstalk rejection.

This comparator offers the following improvements over existing devices:

- Shorter propagation delays
- Lower offset voltage and temperature coefficient
- Lower overall system power
- Better rejection between comparator channels
- Minimal thermal tails
- Does not oscillate

All of these features combined produce high performance products with timing stability and repeatability for large system precision.

TYPICAL INTERFACE CIRCUIT

The typical interface circuit using the comparator is shown in figure 3. Although it needs few external components and is easy to apply, there are several conditions that should be met to achieve optimal performance. The very high operating speeds of the comparator require careful layout, decoupling of supplies, and proper design of transmission lines.

Since the SPT9687 comparator is a very high frequency and high gain device, certain layout rules must be followed to avoid spurious oscillations. The comparator should be soldered to the board with component lead lengths kept as short as possible. A ground plane should be used, and the input impedance to the part should be kept as low as possible to decrease parasitic feedback. If the output board traces are longer than approximately one-half inch, microstripline techniques must be employed to prevent ringing on the output waveform. Also, the microstriplines must be terminated at the far end with the characteristic impedance of the line to prevent reflections. The SPT9687 is capable of driving 50 ohm terminated lines. The termination can be directly tied to -2.0 V or a Thevenin equivalent terminated to the negative supply if a -2.0 V supply is not available. Both supply voltage pins should be decoupled with high frequency capacitors as close to the device as possible.

All pins designated "N/C" should be soldered to ground for additional noise immunity and interelectrode shielding. All ground pins should be connected to the same ground plane.

The timing diagram for the comparator is shown in figure 1. The latch enable (LE) pulse is shown at the top. If LE is high and $\overline{LE}$ low in the SPT9687, the comparator tracks the input difference voltage. When LE is driven low and $\overline{LE}$ high, the comparator outputs are latched into their existing logic states. Please note that the Latch Enable and Latch Enable notations are not consistent with the industry standard; these names have always been opposite to the pins' functional descriptions. Please see the timing diagram in figure 1 for absolute clarification.

The leading edge of the input signal (which consists of 10 mV overdrive) changes the comparator output after a time of t_{pdL} or t_{pdH} (Q or $\overline{Q}$). The input signal must be maintained for a time t_S (set-up time) before the latch enable falling edge and LE rising edge and held for time t_H after the falling edge for the comparator to accept data. After t_H, the output ignores the input status until the latch is strobed again. A minimum latch pulse width of t_{pL} is needed for strobe operation, and the output transitions occur after a time of t_{pLOH} or t_{pLOL}.

Unused outputs must be terminated with 50 ohms to ground while unused latch enable pins should be connected to the appropriate supplies: ground or V_{EE}.

Figure 3 - Typical Interface Circuit

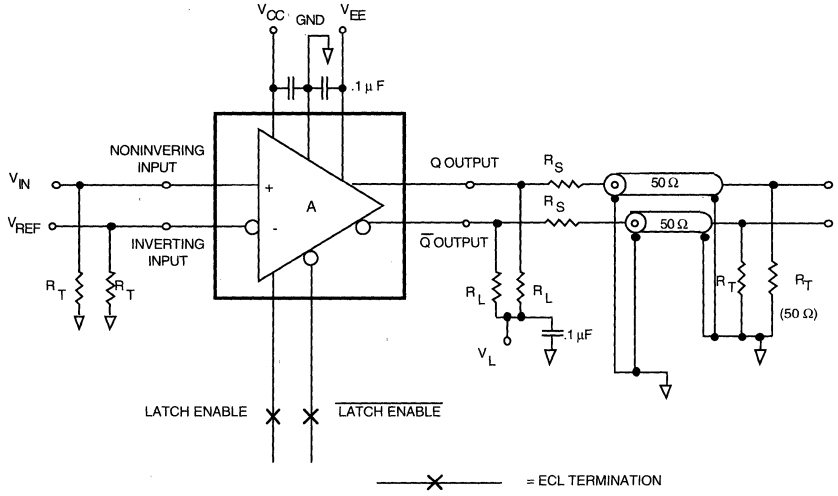


Figure 4 - Equivalent Input Circuit

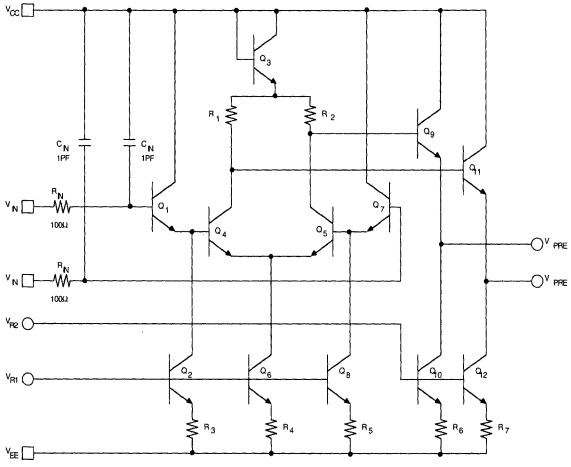


Figure 5 - Output Circuit

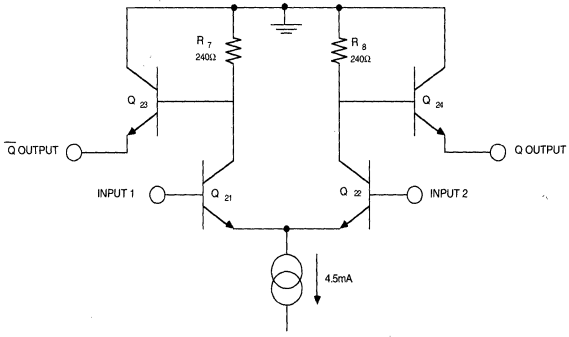


Figure 6 - Test Load

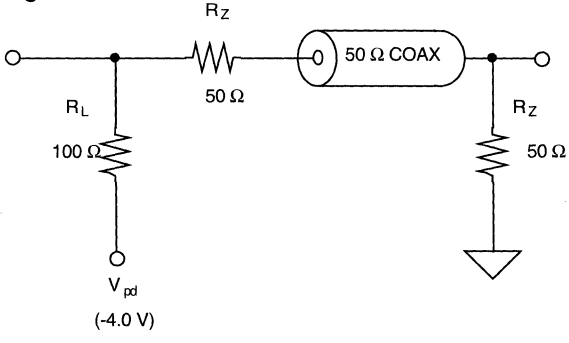


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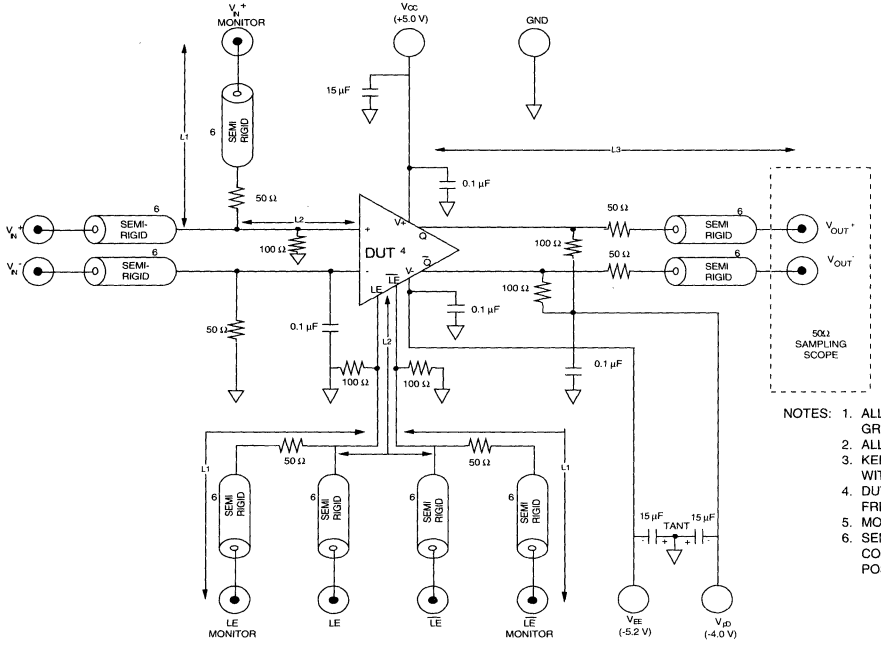
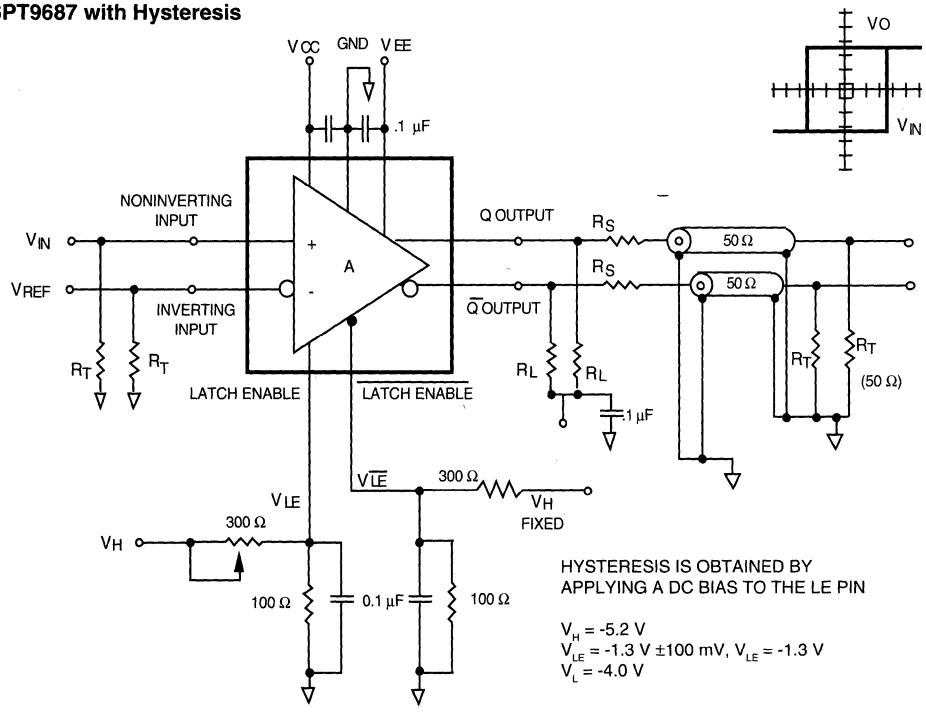
Figure 7 - AC Test Fixture



NOTES:
1. ALL BNC & SEMI RIGID COAX SHIELD ARE GROUNDED.
2. ALL RESISTORS 1% (50 Ω = 49.9 Ω).
3. KEEP ALL LEADS AS SHORT AS POSSIBLE WITH ELECTRICAL LENGTHS L1 = L2 + L3.
4. DUT PLUGS INTO A 16 PIN HIGH FREQUENCY PIN SOCKET.
5. MONITOR INPUT IMPEDANCE 50 Ω TO GND.
6. SEMI RIGID COAX SHIELD SHOULD BE CONNECTED AS CLOSE TO THE DEVICE AS POSSIBLE.

Figure 8 - SPT9687 with Hysteresis

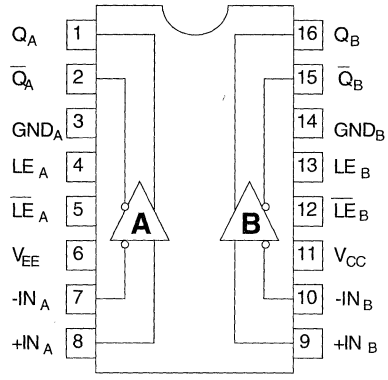


HYSTERESIS IS OBTAINED BY APPLYING A DC BIAS TO THE LE PIN

V_H = -5.2 V
V_{LE} = -1.3 V ±100 mV, V_{LE} = -1.3 V
V_L = -4.0 V

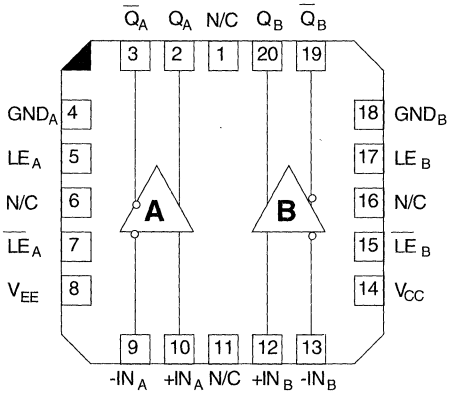
PIN ASSIGNMENTS

TOP VIEW



16 LEAD DIP

TOP VIEW



20 CONTACT CERAMIC LCC/PLCC

PIN FUNCTIONS

NAME	FUNCTION
Q_A	Output A
$\overline{Q}_A$	Inverted Output A
GND_A	Ground A
LE_A	Latch Enable A
$\overline{LE}_A$	Inverted Latch Enable A
V_{EE}	Negative Supply Voltage
$-IN_A$	Inverting Input A
$+IN_A$	Non-Inverting Input A
$+IN_B$	Non-Inverting Input B
$-IN_B$	Inverting Input B
V_{CC}	Positive Supply Voltage
LE_B	Latch Enabled B
$\overline{LE}_B$	Inverted Latch Enable B
GND_B	Ground B
Q_B	Output B
$\overline{Q}_B$	Inverted Output B

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LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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SIGNAL PROCESSING TECHNOLOGIES

SPT9689

DUAL ULTRA-FAST VOLTAGE COMPARATOR

FEATURES

- 650 ps Propagation Delay
- 100 ps Propagation Delay Variation
- 900 MHz Tracking Bandwidth
- 70 dB CMRR
- Low Feedthrough and Crosstalk
- Differential Latch Control
- ECL Compatible

APPLICATIONS

- Automated Test Equipment
- High Speed Instrumentation
- Window Comparators
- High Speed Timing
- Line Receivers
- High Speed Triggers
- Threshold Detection
- Peak Detection

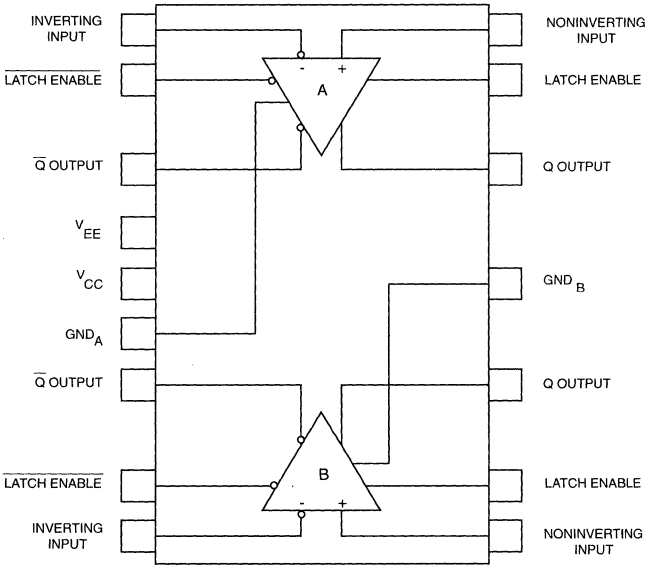
GENERAL DESCRIPTION

The SPT9689 is a *Sub*-nanosecond monolithic dual comparator. The propagation delay variation is less than 100 ps from 5 mV to 50 mV input overdrive voltage. The input slew rate is 10 V/ns. The device utilizes a high precision differential input stage with a common-mode range of -2.5 V to +4.0 V.

ECL compatible complimentary digital outputs are capable of driving 50 Ω terminated transmission lines and providing 30 mA output drive. The SPT9689 is pin-compatible with the HCMP96870. It is available in the industrial temperature range in 20-lead LCC and PLCC packages, a 16-lead ceramic sidebrazed DIP, and die form.

5

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25 °C

Supply Voltages
- Positive Supply Voltage (V_{CC} to GND) ..... -0.5 to +6.0 V
- Negative Supply Voltage (V_{EE} to GND) ... -6.0 to +0.5 V
- Ground Voltage Differential ..... -0.5 to +0.5 V

Input Voltages
- Input Common Mode Voltage ..... -4.0 to +5.0 V
- Differential Input Voltage ..... -3.0 to +3.0 V
- Input Voltage, Latch Controls ..... V_{EE} to 0.5 V

Output
- Output Current ..... 30 mA

Temperature
- Operating Temperature, ambient ..... -55 to +125 °C
- junction ..... +150 °C
- Lead Temperature, (soldering 60 seconds) ..... +300 °C
- Storage Temperature ..... -65 to +150 °C

Note: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications.

ELECTRICAL SPECIFICATIONS

T_A = +25 °C V_{CC} = +5.0 V ±.25 V, V_{EE} =-5.20 V, RL = 50 Ohm to -2 V, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	SPT9689A MIN	SPT9689A TYP	SPT9689A MAX	SPT9689B MIN	SPT9689B TYP	SPT9689B MAX	UNITS
DC CHARACTERISTICS									
Input Offset Voltage	$V_{IN,CM}$=0	I	-10	±3.0	10	-25	±12	25	mV
Input Offset Voltage	$V_{IN,CM}$=0 T_{MIN} <T_A<T_{MAX}	IV	-15	±4.5	15	-30	±15	30	mV
Offset Voltage Tempco		V		10			40		µV/°C
Input Bias Current		I		±8	±20		±8	±20	µA
Input Bias Current	T_{MIN} <T_A<T_{MAX}	IV		±12	±30		±12	±30	µA
Input Offset Current		I		±1.0	±3.0		±2.0	±5.0	µA
Input Offset Current	T_{MIN} <T_A<T_{MAX}	IV		±2.0	±5.0		±4.0	±7.0	µA
Positive Supply Current	Dual	I		18	30		18	35	mA
Negative Supply Current	Dual	I		40	55		40	60	mA
Common Mode Range		I	-2.5		+4.0	-2.5		+4.0	V
Open Loop Gain		V		66			66		dB
Differential Input Resistance		V		500			500		kΩ
Input Capacitance	Cerdip Package	V		2.0			2.0		pF
Input Capacitance	LCC Package	V		0.6			0.6		pF
Power Supply Sensitivity		V		70			70		dB
Common Mode Rejection Ratio	Vcmv=-2.5 to +4.0	V		70			70		dB
Power Dissipation	Dual, Without Load	I		350	425		350	475	mW
Power Dissipation	Dual, With Load	I		400	550		400	550	mW
Output High Level	ECL 50 Ohms to -2 V	I	-1.00		-.81	-1.00		-.81	V
Output Low Level	ECL 50 Ohms to -2 V	I	-1.95		-1.54	-1.95		-1.54	V
AC CHARACTERISTICS									
Propagation Delay	20 mV O.D.	III		650	850		750	950	ps
Latch Set-up Time		V		450	600		450	600	ps
Latch to Output Delay	50 mV O.D.	V		350	500		350	500	ps
Latch Pulse Width		V		500			500		ps
Latch Hold Time		V		30			30		ps
Rise Time	20% to 80%	V		180			180		ps
Fall Time	20% to 80%	V		80			80		ps
Slew Rate		V		10			10		V/ns
Bandwidth	-3 dB	V		900			900		MHz

CAUTION: ESD SENSITIVE DEVICE

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TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests; therefore, $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

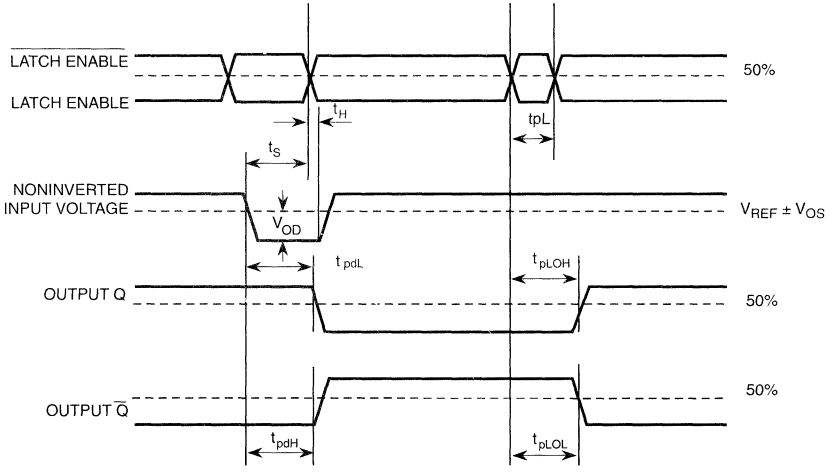
TIMING INFORMATION

The timing diagram for the comparator is shown in figure 1. The latch enable (LE) pulse is shown at the top. If LE is high and $\overline{LE}$ low in the SPT9689, the comparator tracks the input difference voltage. When LE is driven low and $\overline{LE}$ high, the comparator outputs are latched into their existing logic states.

The leading edge of the input signal (which consists of 10 mV overdrive) changes the comparator output after a time of t_{pdL} or t_{pdH} (Q or $\overline{Q}$). The input signal must be maintained for a time t_S (set-up time) before the latch enable falling edge and $\overline{LE}$ rising edge and held for time t_H after the falling edge for the comparator to accept data. After t_H, the output ignores the input status until the latch is strobed again. A minimum latch pulse width of t_{pL} is needed for strobe operation, and the output transitions occur after a time of t_{pLOH} or t_{pLOL}.

Unused outputs must be terminated with 50 ohms to ground while unused latch enable pins should be connected directly to ground.

Figure 1 - Timing Diagram



V_{IN}+=100 mV (p-p), V_{OD} =10 mV

The set-up and hold times are a measure of the time required for an input signal to propagate through the first stage of the comparator to reach the latching circuitry. Input signals occurring before t_S will be detected and held; those occurring after t_H will not be detected. Changes between t_S and t_H may not be detected.

SWITCHING TERMS (Refer to figure 1)

t_{pdH} INPUT TO OUTPUT HIGH DELAY - The propagation delay measured from the time the input signal crosses the reference (± the input offset voltage) to the 50% point of an output LOW to HIGH transition

t_{pdL} INPUT TO OUTPUT LOW DELAY - The propagation delay measured from the time the input signal crosses the reference (± the input offset voltage) to the 50% point of an output HIGH to LOW transition

t_{pLOH} LATCH ENABLE TO OUTPUT HIGH DELAY - The propagation delay measured from the 50% point of the Latch Enable signal LOW to HIGH transition to 50% point of an output LOW to HIGH transition

V_{OD} VOLTAGE OVERDRIVE - The difference between the input and reference input voltages.

t_{pLOL} LATCH ENABLE TO OUTPUT LOW DELAY - The propagation delay measured from the 50% point of the Latch Enable signal LOW to HIGH transition to the 50% point of an output HIGH to LOW transition

t_H MINIMUM HOLD TIME - The minimum time after the negative transition of the Latch Enable signal that the input signal must remain unchanged in order to be acquired and held at the outputs

t_{pL} MINIMUM LATCH ENABLE PULSE WIDTH - The minimum time that the Latch Enable signal must be HIGH in order to acquire an input signal change

t_S MINIMUM SET-UP TIME - The minimum time before the negative transition of the Latch Enable signal that an input signal change must be present in order to be acquired and held at the outputs

GENERAL INFORMATION

The SPT9689 is an ultra high speed dual voltage comparator. It offers tight absolute characteristics. The device has differential analog inputs and complementary logic outputs compatible with ECL systems. The output stage is adequate for driving terminated 50 ohm transmission lines.

The SPT9689 has a complementary latch enable control for each comparator. Both can be driven by standard ECL logic.

The negative common mode voltage is -2.5 V. The positive common mode voltage is +4.0 V.

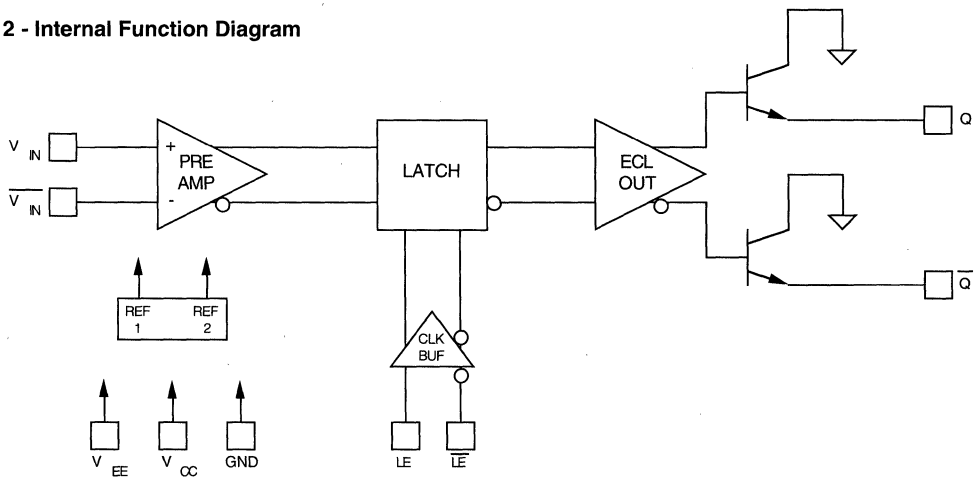
The dual comparators share the same V_{CC} and V_{EE} connections but have separate grounds for each comparator to achieve high crosstalk rejection.

This comparator offers the following improvements over existing devices:

- Proprietary design techniques such as precision clamping of the gain stages result in well behaved and stable output transient response
- Ultra-fast propagation delay time of 650 ps
- Very low propagation delay skew of less than 100 ps in response to input overdrive of +5 to +50 mV
- Excellent input and output rejection between comparator channels
- Hysteresis can be programmed by using LE and $\overline{LE}$ pins to stabilize the output
- Low offset voltage, temp. coefficient and thermal tails

All of these combined features produce high performance products with timing stability and repeatability for large system precision.

Figure 2 - Internal Function Diagram



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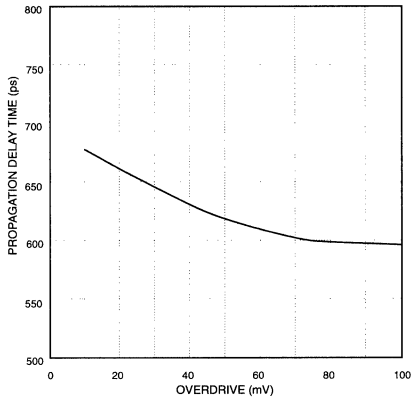
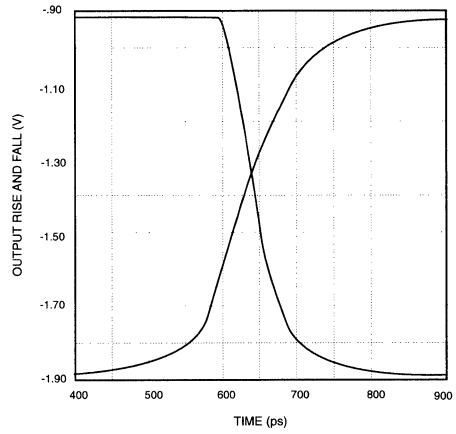
TYPICAL PERFORMANCE CHARACTERISTICS

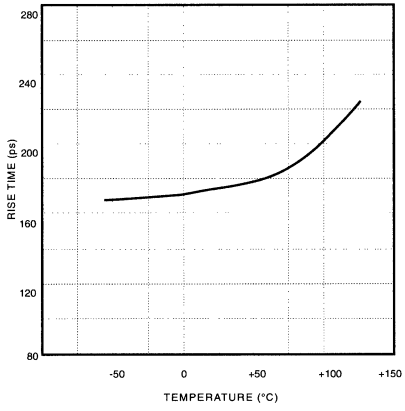
PROPAGATION DELAY VS OVERDRIVE VOLTAGE



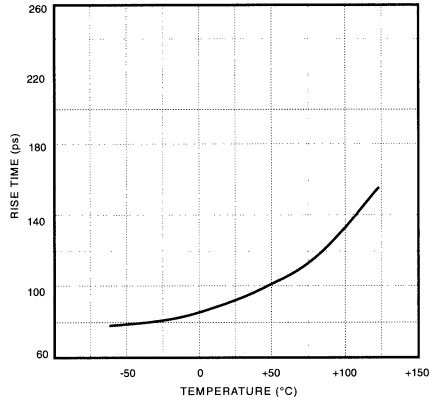
RISE AND FALL OF OUTPUTS VS TIME CROSSOVER



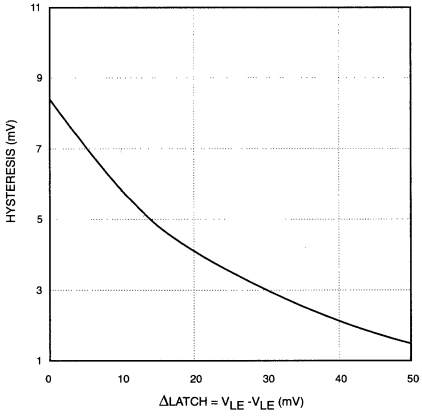
RISE TIME VS TEMPERATURE



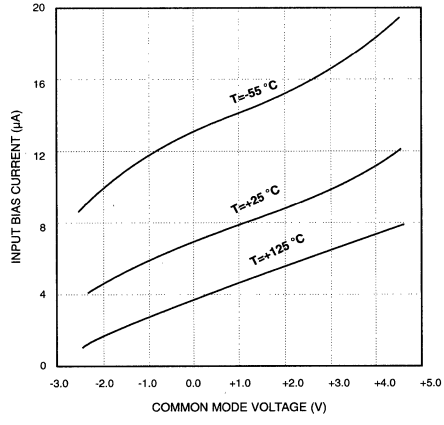
FALL TIME VS TEMPERATURE



HYSTERESIS VS ΔLATCH



INPUT BIAS CURRENT VS COMMON MODE VOLTAGE



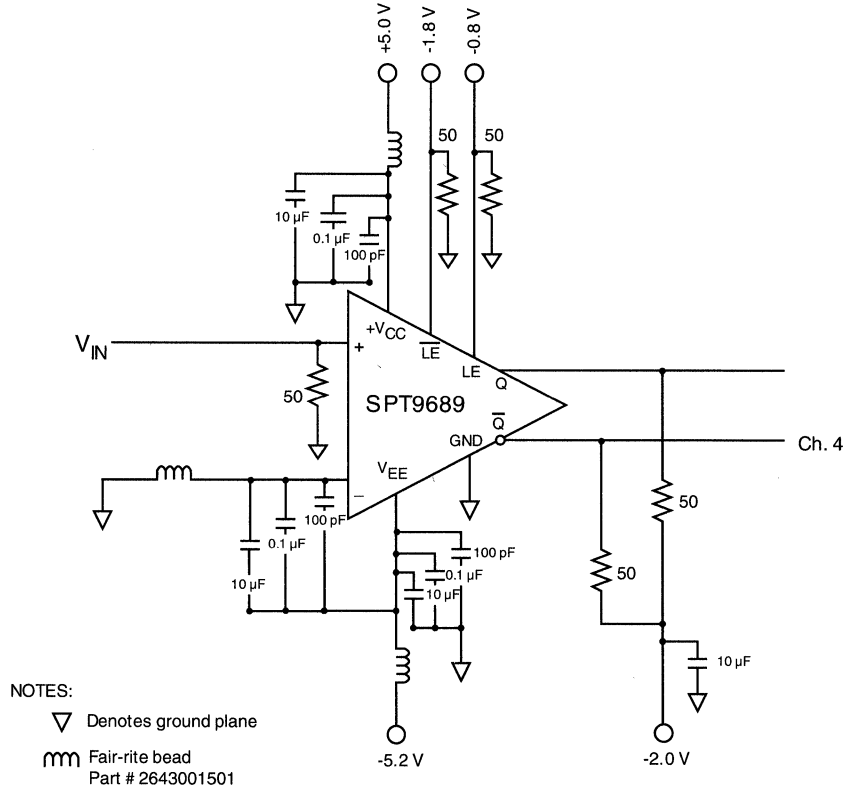
TYPICAL INTERFACE CIRCUIT

The typical interface circuit using the comparator is shown in figure 3. Although it needs few external components and is easy to apply, there are several conditions that should be noted to achieve optimal performance. The very high operating speeds of the comparator require careful layout, decoupling of supplies, and proper design of transmission lines.

Since the SPT9689 comparator is a very high frequency and high gain device, certain layout rules must be followed to avoid oscillations. The comparator should be soldered to the board with component lead lengths kept as short as possible. A ground plane should be used, while the input impedance to the part is kept as low as possible, to decrease parasitic feedback. If the output board traces are longer than approximately half an inch, microstripline techniques must be employed to prevent ringing on the output waveform. Also, the microstriplines must be terminated at the far end with the characteristic impedance of the line to prevent reflections. The SPT9689 is capable of driving 50 ohm terminated lines. The termination can be directly tied to -2.0 V or a Thevenin equivalent terminated to the negative supply if a -2.0 V supply is not available. Both supply voltage pins should be decoupled with high frequency capacitors as close to the device as possible.

All pins designated N/C should be soldered to ground for additional noise immunity and interelectrode shielding. All ground pins should be connected to the same ground plane.

Figure 3 - SPT9689 Typical Interface Circuit



All resistors are chip type 1%
0.1 µF and 100 pF capacitors are chip type mounted as close to pins as possible
10 µF tant capacitors have lead lengths < 0.25" long

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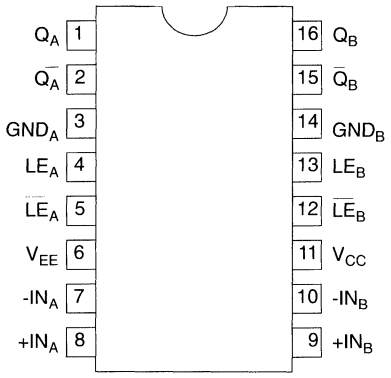
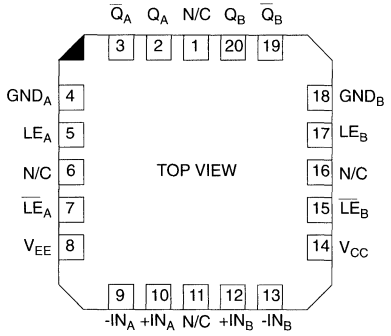
PIN ASSIGNMENTS



16 LEAD DIP



20 CONTACT CERAMIC LCC/PLCC

PIN FUNCTIONS

NAME	FUNCTION
Q_A	Output A
$\overline{Q}_A$	Inverted Output A
GND_A	Ground A
LE_A	Latch Enable A
$\overline{LE}_A$	Inverted Latch Enable A
V_{EE}	Negative Supply Voltage
$-IN_A$	Inverting Input A
$+IN_A$	Noninverting Input A
$+IN_B$	Noninverting Input B
$-IN_B$	Inverting Input B
V_{CC}	Positive Supply Voltage
LE_B	Latch Enabled B
$\overline{LE}_B$	Inverted Latch Enable B
GND_B	Ground B
Q_B	Output B
$\overline{Q}_B$	Inverted Output B

LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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SIGNAL PROCESSING TECHNOLOGIES

SPT9691

WIDE INPUT VOLTAGE, JFET COMPARATOR

FEATURES

- Common Mode Range -4.0 to +8.0 V
- Low Input Bias Current <100 pA
- Propagation Delay 2.5 ns (max)
- 300 MHz Minimum Tracking Bandwidth
- Low Offset ±25 mV
- Low Feedthrough and Crosstalk
- Differential Latch Control

APPLICATIONS

- Automated Test Equipment
- High Speed Instrumentation
- Window Comparators
- High Speed Timing
- Line Receivers
- High Speed Triggers
- Threshold Detection
- Peak Detection

GENERAL DESCRIPTION

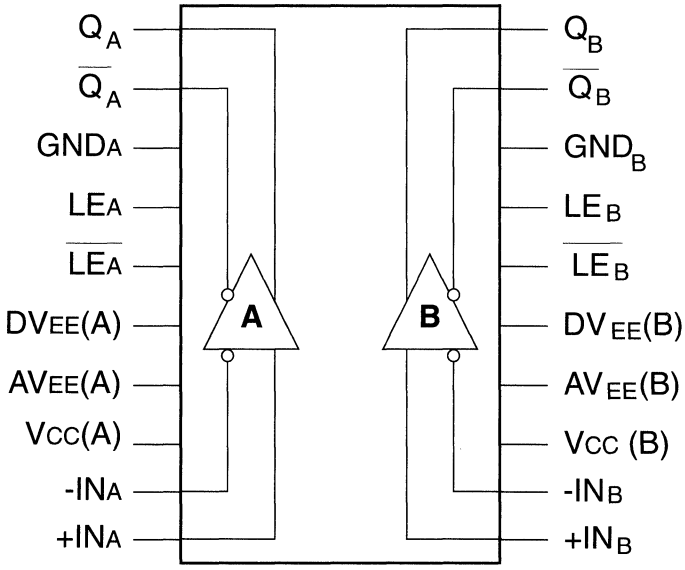
The SPT9691 is a high speed, wide common mode voltage, JFET input, dual comparator. It is designed for applications that measure critical timing parameters in which wide common mode input voltages of -4.0 to +8.0 V are required. Propagation delays are constant for overdrives greater than 200 mV.

JFET inputs reduce the input bias currents to the nanoamp level, eliminating the need for input drivers and buffers in most applications. The device has differential analog inputs and complementary logic outputs compatible with ECL systems. Each comparator has a complementary latch enable control that can be driven by standard ECL logic.

The SPT9691 is available in the commercial temperature range in 20-lead LCC (leadless chip carrier), PLCC, side-brazed ceramic dip and plastic DIP packages as well as in die form.

5

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25°C

Supply Voltages (Measured to GND)

Positive Supply Voltage (AV_{CC}) ..... -0.5 to +11.0 V
Negative Supply Voltage (AV_{EE}) ..... -11.0 to +0.5 V
Negative Supply Voltage (DV_{EE}) ..... -6.0 to +0.5 V

Input Voltages

Input Common Mode Voltage ..... DV_{EE}-1 to +AV_{CC}+1
Differential Input Voltage ..... -12.0 to +12.0 V
Input Voltage, Latch Controls ..... DV_{EE} to 0.5 V
V_{IN} to AV_{CC} Differential Voltage ..... -16 to +1.0 V
V_{IN} to AV_{EE} Differential Voltage ..... +4 to +21.0 V

Output

Output Current ..... 30 mA

Temperature

Operating Temperature, ambient ..... 0 to +70 °C
junction ..... +150 °C
Lead Temperature, (soldering 60 seconds) ..... +300 °C
Storage Temperature ..... -65 to +150 °C

Note: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications. Application of multiple maximum rating conditions at the same time may damage the device.

ELECTRICAL SPECIFICATIONS

T_A = +25 °C, V_{CC} = +10 V, AV_{EE}=-10.0 V, DV_{EE}=-5.2 V, RL = 50 Ohm to -2V, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
DC ELECTRICAL CHARACTERISTICS						
Input Offset Voltage	$V_{IN,CM}$=0	I	-25	0.0	+25	mV
	$T_{MIN} < T_A < T_{MAX}$	IV	-25	0.0	+25	mV
Offset Voltage Tempco		V		50		µV/°C
Input Bias Current		I		±0.1	±10	nA
Input Bias Current	$T_{MIN} < T_A < T_{MAX}$	IV		±2.0	±100	nA
Input Offset Current		V		±1.0		nA
Input Offset Current	$T_{MIN} < T_A < T_{MAX}$	V		±10		nA
Positive Supply Current (Dual)	Vcc=10 V	I		25	33	mA
Negative Supply Current (Dual)	V_{AEE}=-10.0 V	I		15	20	mA
Negative Supply Current (Dual)	V_{DEE}=-5.2 V	I		55	70	mA
Common Mode Range		I	-4.0		+8.0	V
Differential Voltage Range		I			±10	V
Open Loop Gain		V		60		dB
Differential Input Resistance		V		2		GΩ
Input Capacitance	Sidebrazed Package	V		2.9		pF
	LCC Package			1.0		pF
	PLCC Package			1.0		pF
	PDIP			2.9		pF
Power Supply Sensitivity		V		60		dB
Common Mode Rejection Ratio		I	50	60		dB
	$T_{MIN} < T_A < T_{MAX}$	IV	45	55		dB
Power Dissipation	Dual	I		700	800	mW
Output High Level	ECL 50 Ohms to -2V	I	-.98		-.70	V
Output Low Level	ECL 50 Ohms to -2V	I	-1.95		-1.65	V

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ELECTRICAL SPECIFICATIONS

T_A = +25 °C, V_{CC} = +10 V, AV_{EE}=-10.0 V, DV_{EE}=-5.2 V, RL = 50 Ohm to -2V, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
AC ELECTRICAL CHARACTERISTICS						
Propagation Delay[1]	150 mV O.D.	III	1.5	2.0	2.5	ns
Propagation Delay TEMPCO		V		2		ps/ °C
Propagation Delay Skew (A vs B)		V		100		ps
Propagation Delay Dispersion[2]	150 mV Overdrive Min.	V		200		ps
Latch Set-up Time		V		1.7		ns
Latch to Output Delay	150 mV O.D.	V		0.8		ns
Latch Pulse Width		V		2		ns
Latch Hold Time		V		-1.9		ns
Rise Time	20% to 80%	V		0.4		ns
Fall Time	20% to 80%	V		0.4		ns
Slew Rate		V		3		V/ns
Bandwidth	-3 dB	V		300		MHz

NOTES:

[1]Valid for both high-to-low and low-to-high transitions

[2]Dispersion is the change in propagation delay due to changes in slew rate, overdrive, and common mode level.

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests; therefore, $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

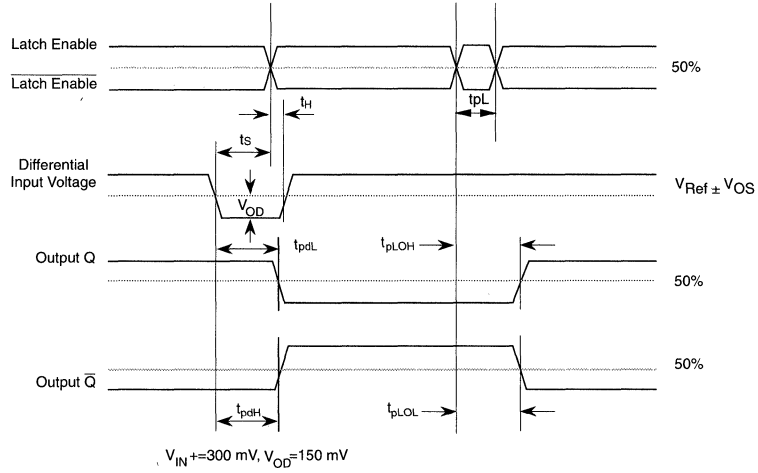
TIMING INFORMATION

The timing diagram for the comparator is shown in figure 1. If LE is high and $\overline{LE}$ low in the SPT9691, the comparator tracks the input difference voltage. When LE is driven low and $\overline{LE}$ high, the comparator outputs are latched into their existing logic states.

The leading edge of the input signal (which consists of the overdrive voltage) changes the comparator output after a time of t_{pdL} or t_{pdH} (Q or $\overline{Q}$). The input signal must be maintained for a time t_s (set-up time) before the LE falling edge and $\overline{LE}$ rising edge and held for time t_H after the falling edge for the comparator to accept data. After t_H, the output ignores the input status until the latch is strobed again. A minimum latch pulse width of t_{pL} is needed for strobe operation, and the output transitions occur after a time of t_{pLOH} or t_{pLOL}.

Unused outputs must be terminated with 50 ohms to ground while unused $\overline{LE}$ pins should be connected directly to ground.

Figure 1 - Timing Diagram



The set-up and hold times are a measure of the time required for an input signal to propagate through the first stage of the comparator to reach the latching circuitry. Input signals occurring before t_s will be detected and held; those occurring after t_H will not be detected. Changes between t_S and t_H may not be detected.

SWITCHING TERMS (Refer to figure 1)

t_{pdH} INPUT TO OUTPUT HIGH DELAY - The propagation delay measured from the time the input signal crosses the reference voltage (± the input offset voltage) to the 50% point of an output LOW to HIGH transition.

t_{pdL} INPUT TO OUTPUT LOW DELAY - The propagation delay measured from the time the input signal crosses the reference voltage (± the input offset voltage) to the 50% point of an output HIGH to LOW transition.

t_{pLOH} LATCH ENABLE TO OUTPUT HIGH DELAY - The propagation delay measured from the 50% point of the Latch Enable signal LOW to HIGH transition to 50% point of an output LOW to HIGH transition.

t_{pLOL} LATCH ENABLE TO OUTPUT LOW DELAY - The propagation delay measured from the 50% point of the Latch Enable signal LOW to HIGH transition to the 50% point of an output HIGH to LOW transition.

t_H MINIMUM HOLD TIME - The minimum time after the negative transition of the Latch Enable signal that the input signal must remain unchanged in order to be acquired and held at the outputs.

t_{pL} MINIMUM LATCH ENABLE PULSE WIDTH - The minimum time that the Latch Enable signal must be HIGH in order to acquire an input signal change.

t_S MINIMUM SET-UP TIME - The minimum time before the negative transition of the Latch Enable signal that an input signal change must be present in order to be acquired and held at the outputs.

V_{OD} VOLTAGE OVERDRIVE - The difference between the input and reference input voltages.

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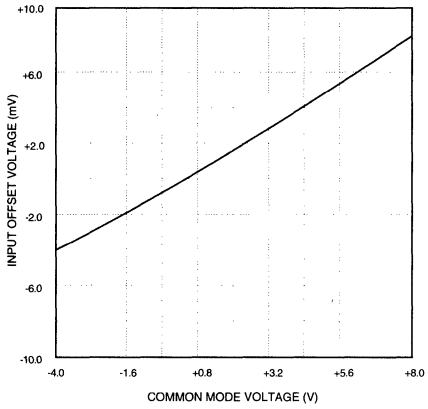
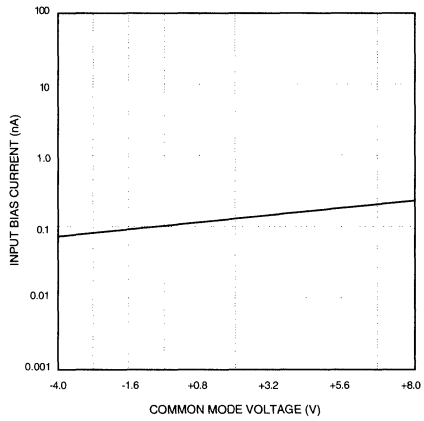
TYPICAL PERFORMANCE CURVES

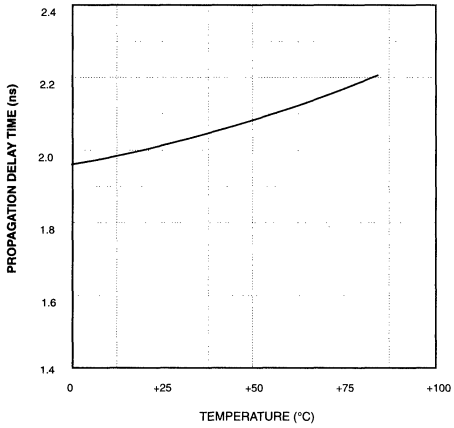
INPUT OFFSET VOLTAGE VS COMMON MODE VOLTAGE (T=+25 °C)



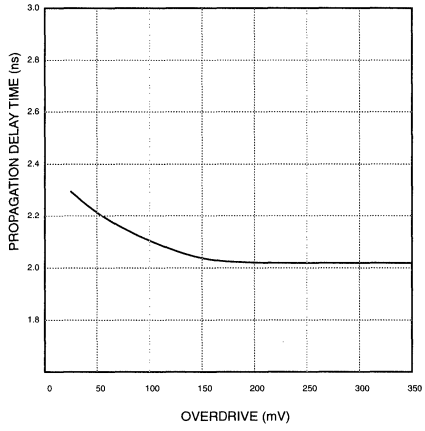
INPUT BIAS CURRENT VS COMMON MODE VOLTAGE (+25 °C)



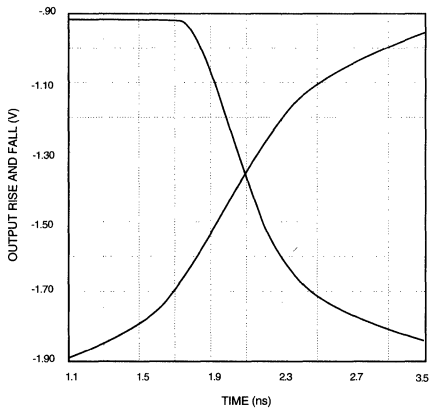
PROPOGATION DELAY TIME VS TEMPERATURE (V_{OD}=150 mV)



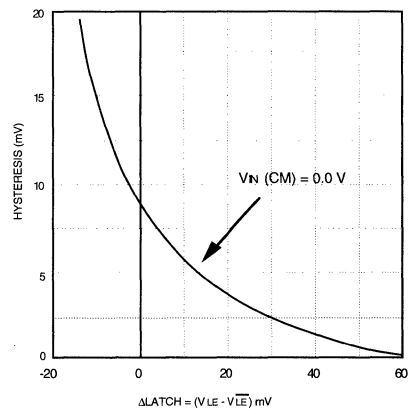
PROPAGATION DELAY TIME VS OVERDRIVE (mV)



RISE AND FALL OF OUTPUTS VS TIME CROSSOVER



HYSTERESIS VS ΔLATCH



GENERAL INFORMATION

The SPT9691 is an ultra high speed dual voltage comparator. It offers tight absolute characteristics. The device has differential analog inputs and complementary logic outputs compatible with ECL systems. The output stage is adequate for driving terminated 50 ohm transmission lines.

The SPT9691 has a complementary latch enable control for each comparator. Both can be driven by standard ECL logic.

A common mode voltage range of -4 V to +8 V is achieved by a proprietary JFET input design which requires a separate negative power supply (AV_{EE}).

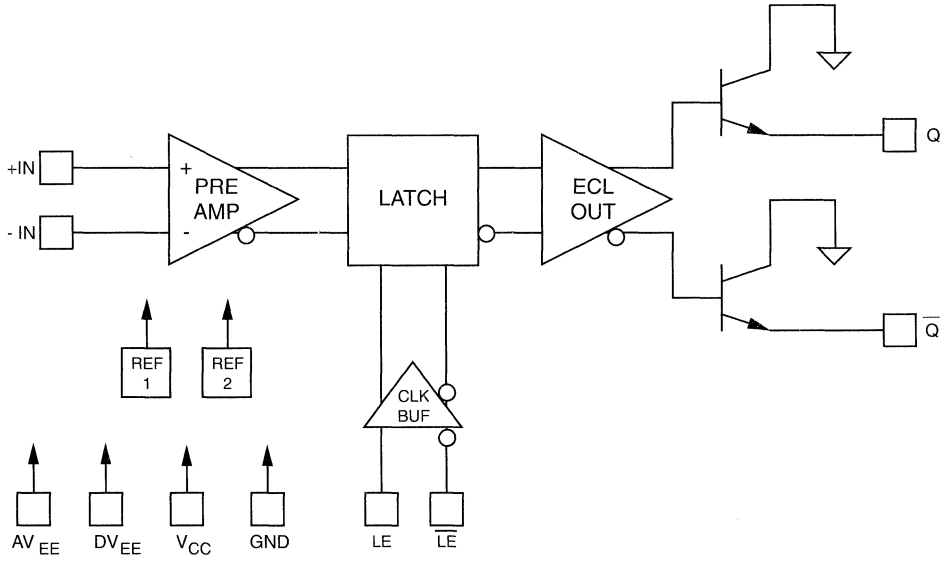
The dual comparators have separate V_{CC}, AV_{EE}, DV_{EE}, and grounds for each comparator to achieve high crosstalk rejection. Single channel operation can be accomplished by floating all pins (including the ground and supply pins) of the unused comparator. Power dissipation during single mode operation will be reduced to 1/2 of the dual mode operation.

This comparator offers the following improvements over existing devices:

- Ultra low input bias current and input current offset
- Common mode voltage of -4 to +8 V
- Short propagation delays
- Excellent input and output rejection between comparator channels
- Improved input protection reliability due to JFET input stage design

All of these combined features produce high performance products with timing stability and repeatability for large system precision.

Figure 2 - Internal Function Diagram



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TYPICAL INTERFACE CIRCUIT

The typical interface circuit using the comparator is shown in figure 3. Although it needs few external components and is easy to apply, there are several conditions that should be noted to achieve optimal performance. The very high operating speeds of the comparator require careful layout, decoupling of supplies, and proper design of transmission lines.

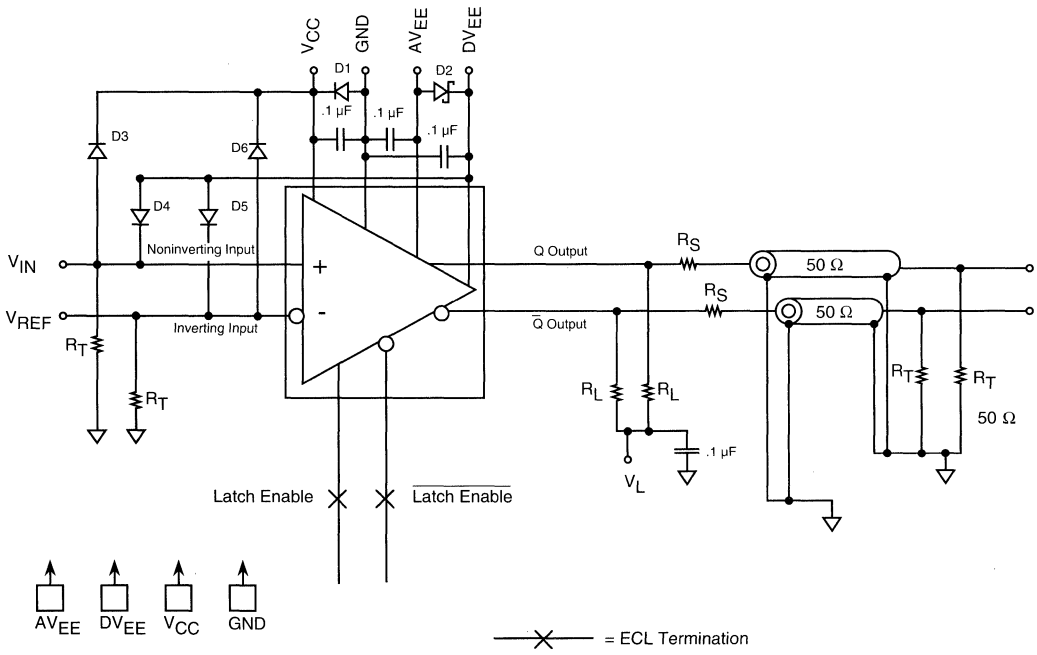
Since the SPT9691 comparator is a very high frequency and high gain device, certain layout rules must be followed to avoid oscillations. The comparator should be soldered to the board with component lead lengths kept as short as possible. A ground plane should be used, while the input impedance to the part is kept as low as possible, to decrease parasitic feedback. If the output board traces are longer than approximately half an inch, microstripline techniques must be employed to prevent ringing on the output waveform. Also, the microstriplines must be terminated at the far end with the characteristic impedance of the line to prevent reflections. The SPT9691 is capable of driving 50 ohm terminated lines. The termination can be directly tied to -2.0 V or a Thevenin equivalent terminated to the negative supply if a -2.0 V supply is not available. All supply voltage pins should be decoupled with high frequency capacitors as close to the device as possible.

Diode D1 connected between V_{CC} and GND is recommended to prevent possible damage to the device in case the V_{CC} supply is disconnected. The diode should be a 1N914 or equivalent. If V_{CC} is disconnected with this diode in place, there will be approximately a 6 mA current draw from both AV_{EE} and DV_{EE}. Diode D2 connected between AV_{EE} and DV_{EE} is necessary to avoid power supply sequence latch-up. This diode keeps AV_{EE} (also the substrate) less than a silicon diode drop away from the most negative circuit potential if DV_{EE} is powered up first. This diode should be a 1N5817 (Schottky) or equivalent.

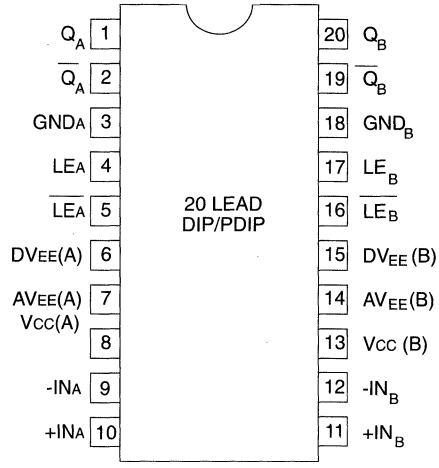
Note: At no time should both inputs be allowed to float with power applied to the device. At least one of the inputs should be tied to a voltage within the common mode range (-4.0 to +8.0 V) to prevent possible damage to the device. To prevent possible latch-up during initial power up, the input voltages should not exceed ±1 V. Additional protection diodes D3-D6 should be used on the inputs if there is the possibility of exceeding the absolute maximum ratings of the inputs with respect to AV_{CC} and DV_{EE} (1N914 or equivalent). NOTE: For ease of implementation, all diodes (D1 - D6) can be 1N5817 (Schottky) or equivalent.

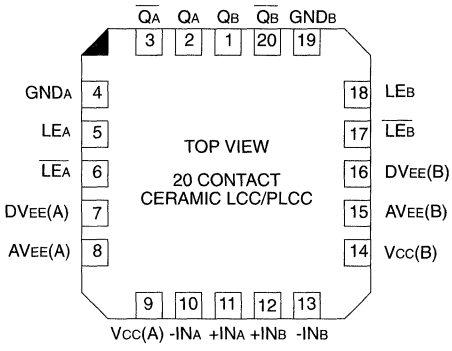
All ground pins should be connected to the same ground plane to further improve noise immunity and shielding.

Figure 3 - SPT9691 Typical Interface Circuit



PIN ASSIGNMENTS





PIN FUNCTIONS

NAME	FUNCTION
Q_A	Output A
$\overline{Q}_A$	Inverted Output A
GND_A	Ground A
$\overline{LE}_A$	Inverted Latch Enable A
LE_A	Latch Enable A
V_{CC}(A)	Positive Supply Voltage (+10 V)
AV_{EE}(A)	Negative Supply Voltage (-10 V)
DV_{EE}(A)	Negative Supply Voltage (-5.2 V)
V_{CC}(B)	Positive Supply Voltage (+10 V)
AV_{EE}(B)	Negative Supply Voltage (-10 V)
DV_{EE}(B)	Negative Supply Voltage (-5.2 V)
$-IN_A$	Inverting Input A
$+IN_A$	Noninverting Input A
$+IN_B$	Noninverting Input B
$-IN_B$	Inverting Input B
$\overline{LE}_B$	Inverted Latch Enabled B
LE_B	Latch Enable B
GND_B	Ground B
$\overline{Q}_B$	Inverted Output B
Q_B	Output B

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SPT9693

WIDE INPUT VOLTAGE, JFET COMPARATOR

FEATURES

- Common Mode Range -3.0 to +8.0 V
- Low Input Bias Current <100 pA
- Propagation Delay 1.5 ns (max)
- Low Offset ±25 mV
- Low Feedthrough and Crosstalk
- Differential Latch Control

APPLICATIONS

- Automated Test Equipment
- High Speed Instrumentation
- Window Comparators
- High Speed Timing
- Line Receivers
- High Speed Triggers
- Threshold Detection
- Peak Detection

GENERAL DESCRIPTION

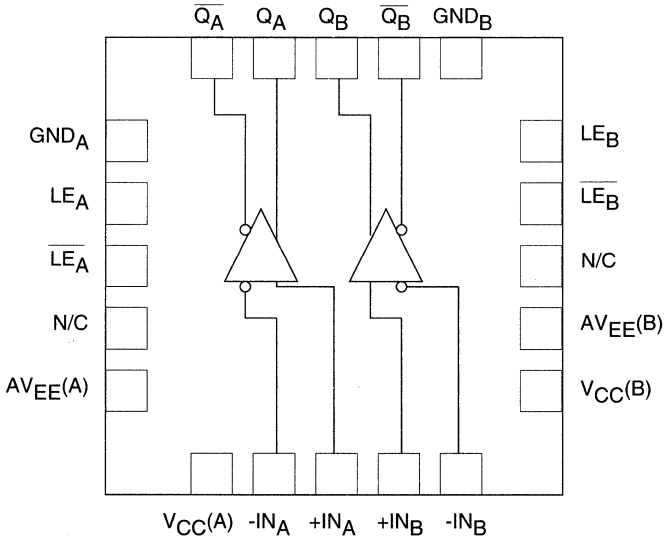
The SPT9693 is a high speed, wide common mode voltage, JFET input, dual comparator. It is designed for applications that measure critical timing parameters in which wide common mode input voltages of -3.0 to +8.0 V are required. Propagation delays are constant for overdrives greater than 50 mV.

JFET inputs reduce the input bias currents to the nanoamp level, eliminating the need for input drivers and buffers in most applications. The device has differential analog inputs and complementary logic outputs compatible with ECL systems. Each comparator has a complementary latch enable control that can be driven by standard ECL logic.

The SPT9693 is available in the commercial temperature range in 20-lead LCC (leadless chip carrier), PLCC, and sidebrazed ceramic dip packages as well as in die form.

5

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25°C

Supply Voltages (Measured to GND)

Positive Supply Voltage (AV_{CC}) ..... -0.5 to +11.0 V
Negative Supply Voltage (AV_{EE}) ..... -11.0 to +0.5 V

Input Voltages

Input Common Mode Voltage ..... -6 to $+AV_{CC}+1$
Differential Input Voltage ..... -12.0 to +12.0 V
Input Voltage, Latch Controls ..... -6 to 0.5 V
V_{IN} to AV_{CC} Differential Voltage ..... -16 to +1.0 V
V_{IN} to AV_{EE} Differential Voltage ..... +4 to +21.0 V

Output

Output Current ..... 30 mA

Temperature

Operating Temperature, ambient ..... 0 to +70 °C
junction..... +150 °C
Lead Temperature, (soldering 60 seconds) ..... +300 °C
Storage Temperature ..... -65 to +150 °C

Note: 1. Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications. Application of multiple maximum rating conditions at the same time may damage the device.

ELECTRICAL SPECIFICATIONS

T_A = +25 °C, V_{CC} = +10 V, AV_{EE}=-10.0 V, RL = 50 Ohm to -2V, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS						
Input Offset Voltage	V_{IN} (Common Mode) = 0	I	-25	0.0	+25	mV
	$T_{MIN} < T_A < T_{MAX}$	IV	-25	0.0	+25	mV
Offset Voltage Tempco		V		50		µV/°C
Input Bias Current	$T_{MIN} < T_A < T_{MAX}$ V_{IN} (Common Mode) = -3 to +7 V	I		±10	±100	nA
Input Bias Current	$T_{MIN} < T_A < T_{MAX}$ V_{IN} (Common Mode) = +7 to +8 V	I		±50	±150	nA
Input Offset Current		V		±1.0		nA
Input Offset Current	$T_{MIN} < T_A < T_{MAX}$	V		±10		nA
Positive Supply Current (Dual)	Vcc=10 V	I		3	6	mA
Negative Supply Current (Dual)	AV_{EE}=-10.0 V	I		40	55	mA
Common Mode Range		I	-3.0		+8.0	V
Differential Voltage Range		I			±10	V
Open Loop Gain		V		52		dB
Differential Input Resistance		V		2		GΩ
Input Capacitance	LCC Package			1.0		pF
	PLCC Package			1.0		pF
	Sidebrazed DIP			2.9		pF
Power Supply Sensitivity		V		60		dB

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ELECTRICAL SPECIFICATIONS

T_A = +25 °C, V_{CC} = +10 V, AV_{EE}=-10.0 V, RL = 50 Ohm to -2V, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
Common Mode Rejection Ratio		I	50	60		dB
	$T_{MIN} < T_A < T_{MAX}$	IV	45	55		dB
Power Dissipation	Dual	I		430	610	mW
Output High Level	ECL 50 Ohms to -2V	I	-.98		-.70	V
Output Low Level	ECL 50 Ohms to -2V	I	-1.95		-1.65	V
AC ELECTRICAL PARAMETERS						
Propagation Delay[1]	50 mV O.D. Slew 10V/ns	III	.75	1.25	1.50	ns
Propagation Delay TEMPCO		V		2		ps/ °C
Propagation Delay Skew (A vs B)		V		100		ps
Delay Dispersion from Input Direction		V		50		ps
Delay Dispersion from Input Common Mode		V		60		ps
Latch Set-up Time		V		500		ps
Latch to Output Delay	50 mV O.D.	V		500		ps
Latch Pulse Width		V		500		ps
Latch Hold Time		V		0		ps
Rise Time	20% to 80%	V		0.45		ns
Fall Time	20% to 80%	V		0.45		ns
Slew Rate		V		5		V/ns

NOTES:

[1]Valid for both high-to-low and low-to-high transitions

TEST LEVEL CODES

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I	100% production tested at the specified temperature.
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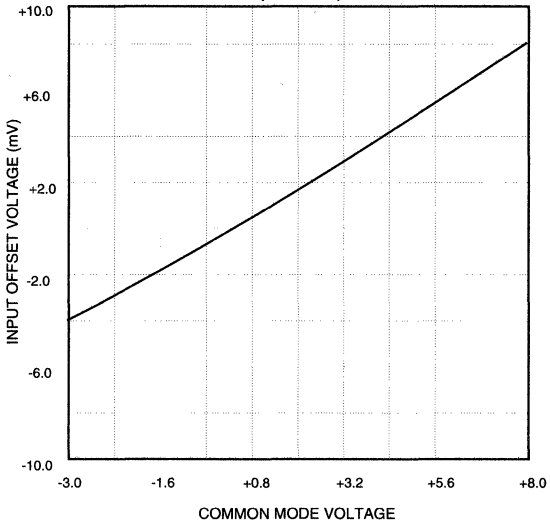
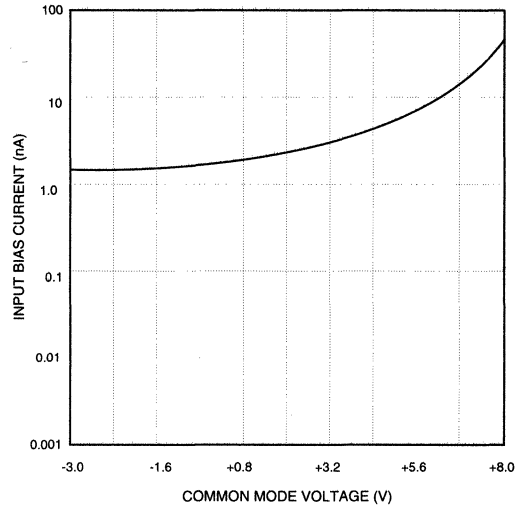
TYPICAL PERFORMANCE CURVES

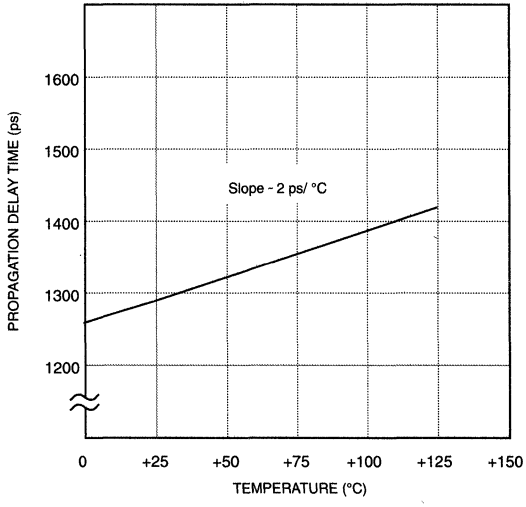
INPUT OFFSET VOLTAGE VS COMMON MODE VOLTAGE (T=+25 °C)



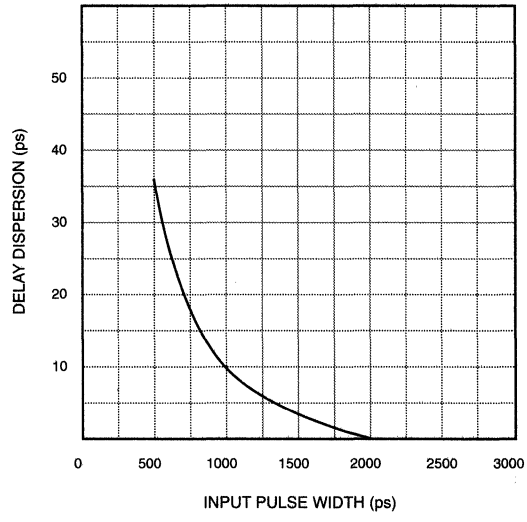
INPUT BIAS CURRENT VS COMMON MODE VOLTAGE (+25 °C)



PROPAGATION DELAY TIME vs TEMPERATURE



DELAY DISPERSION vs INPUT PULSE WIDTH



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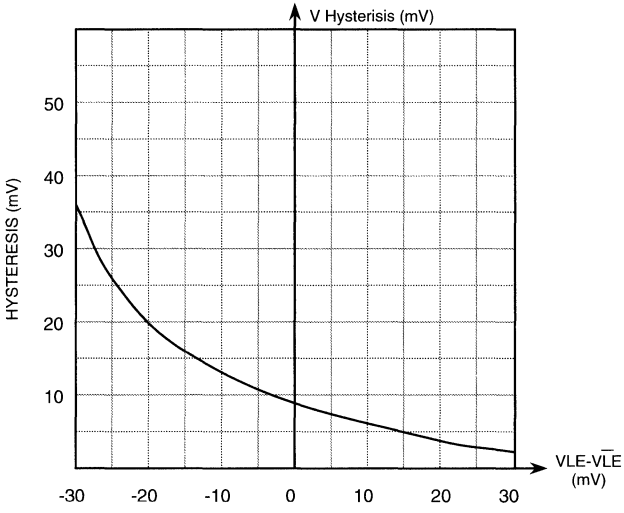
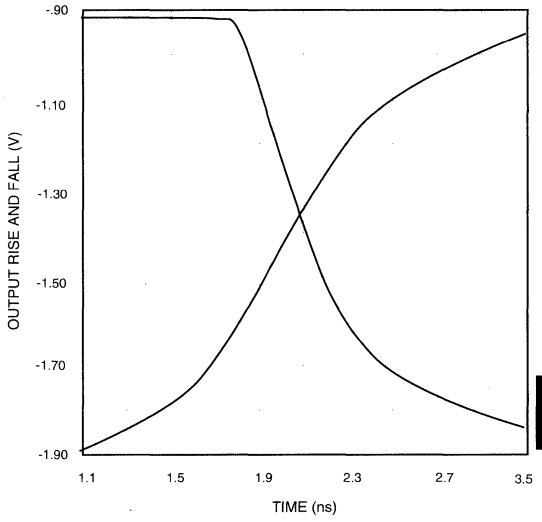
TYPICAL PERFORMANCE CURVES

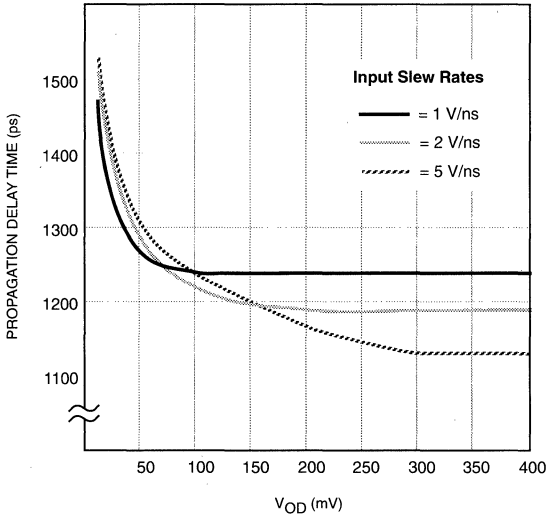
HYSTERESIS vs ΔLATCH VOLTAGE



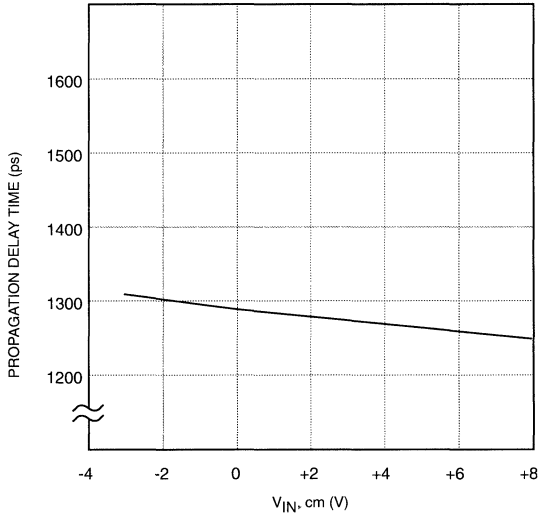
RISE AND FALL OF OUTPUTS vs TIME CROSSOVER



PROPAGATION DELAY vs INPUT OVERDRIVE VOLTAGE



PROPAGATION DELAY vs COMMON MODE INPUT VOLTAGE



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- Short propagation delays
- Excellent input and output rejection between comparator channels
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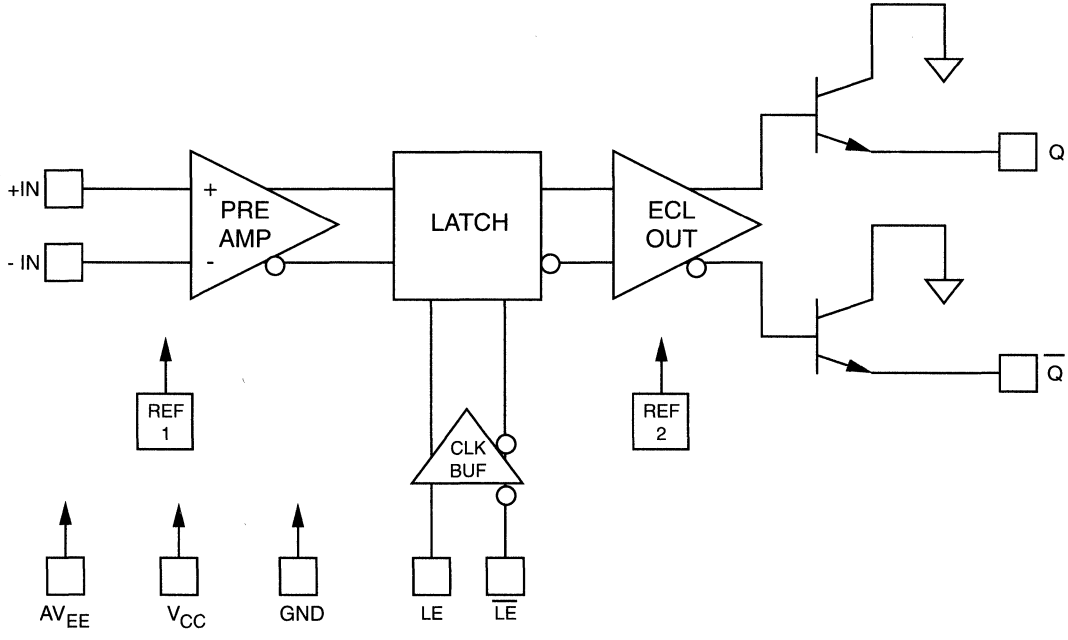
Figure 1 - Internal Function Diagram



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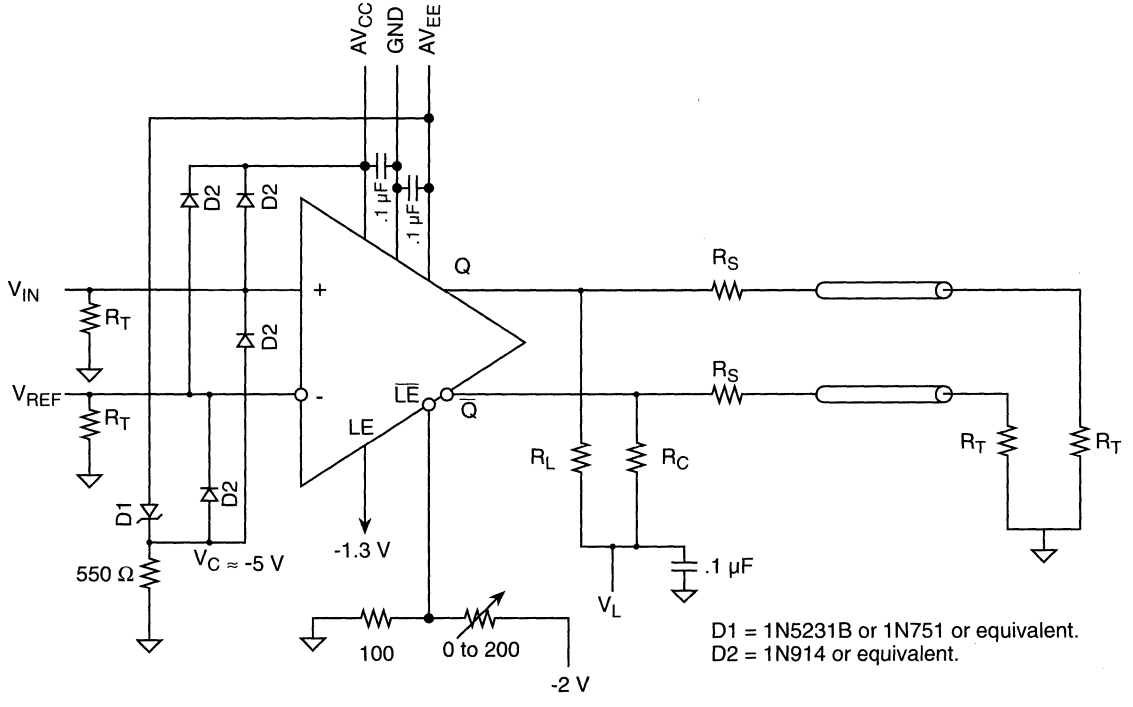
TYPICAL INTERFACE CIRCUIT

The typical interface circuit using the comparator is shown in figure 2. Although it needs few external components and is easy to apply, there are several conditions that should be noted to achieve optimal performance. The very high operating speeds of the comparator require careful layout, decoupling of supplies, and proper design of transmission lines.

Since the SPT9693 comparator is a very high frequency and high gain device, certain layout rules must be followed to avoid oscillations. The comparator should be soldered to the board with component lead lengths kept as short as possible. A ground plane should be used, while the input impedance to the part is kept as low as possible, to decrease parasitic feedback. If the output board traces are longer than approximately half an inch, microstripline techniques must be employed to prevent ringing on the output waveform. Also, the microstriplines must be terminated at the far end with the characteristic impedance of the line to prevent reflections. The SPT9693 is capable of driving 50 ohm terminated lines. The termination can be directly tied to -2.0 V or a Thevenin equivalent terminated to the negative supply if a -2.0 V supply is not available. All supply voltage pins should be decoupled with high frequency capacitors as close to the device as possible.

All ground pins should be connected to the same ground plane to further improve noise immunity and shielding.

Figure 2 - SPT9693 Typical Interface Circuit



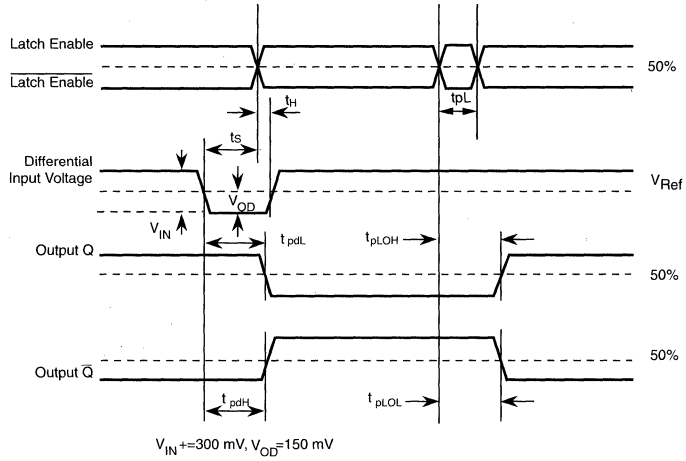
TIMING INFORMATION

The timing diagram for the comparator is shown in figure 3. If LE is high and $\overline{LE}$ low in the SPT9693, the comparator tracks the input difference voltage. When LE is driven low and $\overline{LE}$ high, the comparator outputs are latched into their existing logic states.

The leading edge of the input signal (which consists of the overdrive voltage) changes the comparator output after a time of t_{pdL} or t_{pdH} (Q or $\overline{Q}$). The input signal must be maintained for a time t_S (set-up time) before the LE falling edge and $\overline{LE}$ rising edge and held for time t_H after the falling edge for the comparator to accept data. After t_H , the output ignores the input status until the latch is strobed again. A minimum latch pulse width of t_{pL} is needed for strobe operation, and the output transitions occur after a time of t_{pLOH} or t_{pLOL}.

Unused outputs must be terminated with 50 ohms to ground while unused $\overline{LE}$ pins should be connected directly to ground.

Figure 3 - Timing Diagram



The set-up and hold times are a measure of the time required for an input signal to propagate through the first stage of the comparator to reach the latching circuitry. Input signals occurring before t_s will be detected and held; those occurring after t_H will not be detected. Changes between t_s and t_H may not be detected.

SWITCHING TERMS (Refer to figure 3)

t_{pdH} INPUT TO OUTPUT HIGH DELAY - The propagation delay measured from the time the input signal reaches the input overdrive voltage to the 50% point of an output LOW to HIGH transition.

t_{pdL} INPUT TO OUTPUT LOW DELAY - The propagation delay measured from the time the input signal reaches the input overdrive voltage to the 50% point of an output HIGH to LOW transition.

t_{pLOH} LATCH ENABLE TO OUTPUT HIGH DELAY - The propagation delay measured from the 50% point of the Latch Enable signal LOW to HIGH transition to 50% point of an output LOW to HIGH transition.

t_{pLOL} LATCH ENABLE TO OUTPUT LOW DELAY - The propagation delay measured from the 50% point of the Latch Enable signal LOW to HIGH transition to the 50% point of an output HIGH to LOW transition.

t_H MINIMUM HOLD TIME - The minimum time after the negative transition of the Latch Enable signal that the input signal must remain unchanged in order to be acquired and held at the outputs.

t_{pL} MINIMUM LATCH ENABLE PULSE WIDTH - The minimum time that the Latch Enable signal must be HIGH in order to acquire an input signal change.

t_S MINIMUM SET-UP TIME - The minimum time before the negative transition of the Latch Enable signal that an input signal change must be present in order to be acquired and held at the outputs.

V_{OD} VOLTAGE OVERDRIVE - The difference between the input and reference input voltages.

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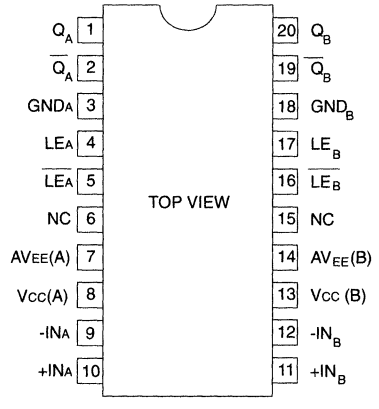
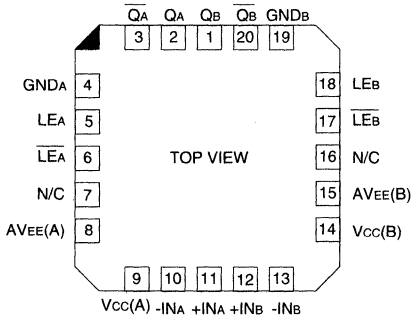
PIN ASSIGNMENTS



20 LEAD DIP



20 CONTACT CERAMIC LCC/PLCC

PIN FUNCTIONS

NAME	FUNCTION
Q_A	Output A
$\overline{Q}_A$	Inverted Output A
GND_A	Ground A
$\overline{LE}_A$	Inverted Latch Enable A
LE_A	Latch Enable A
V_{CC}(A)	Positive Supply Voltage (+10 V)
AV_{EE}(A)	Negative Supply Voltage (-10 V)
V_{CC}(B)	Positive Supply Voltage (+10 V)
AV_{EE}(B)	Negative Supply Voltage (-10 V)
$-IN_A$	Inverting Input A
$+IN_A$	Noninverting Input A
$+IN_B$	Noninverting Input B
$-IN_B$	Inverting Input B
$\overline{LE}_B$	Inverted Latch Enabled B
LE_B	Latch Enable B
GND_B	Ground B
$\overline{Q}_B$	Inverted Output B
Q_B	Output B
N/C	Not Connected

5

LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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SIGNAL PROCESSING TECHNOLOGIES

SPT9500

HIGH-SPEED PIN DRIVER

ADVANCED INFORMATION

FEATURES

- 300 MHz Driver Operation
- Driver Inhibit Function
- 100 ps Edge Matching
- Guaranteed Industry Specifications
  - 50 Ω Output Impedance
  - 3 V/ns Slew Rate
  - Variable Output Voltages for ECL, TTL, and CMOS

APPLICATIONS

- Automated Test Equipment
  - Semiconductor Test Systems
  - Board Test Systems
- Instrumentation and Characterization Equipment

GENERAL DESCRIPTION

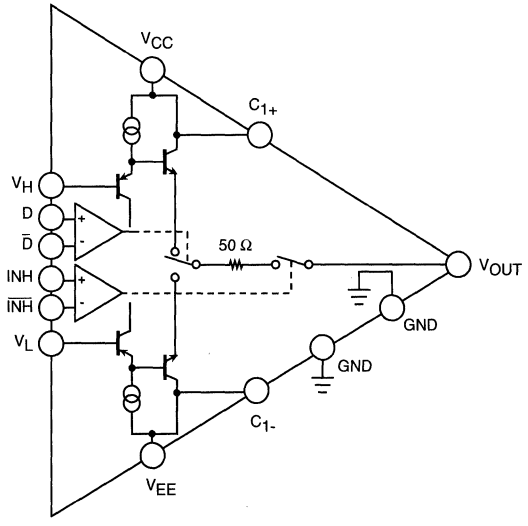
The SPT9500 is a complete, high-speed pin driver designed for use in digital or mixed signal test systems. It features unity gain programmable output levels of -3 V to +10 V with output swing capability of less than 200 mV to 8 V. The SPT9500 is designed to stimulate ECL, TTL and CMOS logic families. The 300 MHz data rate capacity and matched output impedance allow for real-time stimulation of these digital logic families. To test I/O devices, the pin driver can be switched into a high impedance state (inhibit mode) electrically removing the driver from the path through the inhibit mode feature. The pin driver leakage current in inhibit mode is typically 100 µA, and output capacitance is 5 pF (typ).

The SPT9500 transition from Hi/Lo or to inhibit is controlled through the data and inhibit inputs. The input circuitry is implemented using high-speed differential inputs with a common mode range of 5 volts. This allows for direct interface to the precision of differential ECL timing or the simplicity of stimulating the pin driver from a single ended TTL or CMOS logic source. The analog logic Hi/Lo inputs are equally easy to interface. The SPT9500 typically requires 50 µA of reference bias current.

The SPT9500 is available in a 28-lead PLCC package over the commercial temperature range of 0 to +70 °C.

6

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Beyond which damage may occur)[1] 25°C

Power Supply Voltage

V_{CC} to Gnd ..... +13 V
V_{EE} to Gnd ..... -7 V
Difference from V_{CC} to V_{EE} ..... +19 V

Inputs

Difference from D to $\overline{D}$ ..... TBD
Difference from INH to $\overline{INH}$ ..... TBD
D, $\overline{D}$, INH, $\overline{INH}$ ..... TBD
V_H to V_L ..... -1 V, +11 V
V_H, V_L ..... V_{CC} - 16 V, V_{EE} + 15 V

Driver Output

Voltage ..... V_{CC} - 16 V, V_{EE} + 15 V
Short Circuit to GND ..... Indefinite

Temperature Ranges

Operating ..... 0 to +70 °C
Storage Temperature ..... -65 to +125 °C
Lead Temperature, (soldering 20 seconds) ..... +300 °C

Note 1: Operation at any Absolute Maximum Rating is not implied. See Electrical Specifications for proper nominal applied conditions in typical applications. Application of multiple maximum rating conditions at the same time may damage the device.

ELECTRICAL SPECIFICATIONS

T_A = +25 °C, V_{CC} = +12 V, V_{EE}=-6.0 V, Output Load = 2 pF, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS						
Differential Input Characteristics						
D to $\overline{D}$, INH to $\overline{INH}$						
Input Voltage, Any Input		I	TBD	ECL	TBD	V
Diffential Input Range		I	0.4	ECL	3.0	V
Bias Current		I	TBD	+50	TBD	µA
Reference Inputs						
V_{HIGH} Range (V_H)		I	-3.0		+8.0	V
V_{LOW} Range (V_L)		I	-3.0		+8.0	V
Bias Currents		I	TBD	±50	TBD	µA
Output Characteristics						
Logic High Range		I	-3.0		+8.0	V
Logic Low Range		I	-3.0		+8.0	V
Amplitude (V_H - V_L)		I	0.1		+10.0	V
Accuracy						
Initial Offset		I	TBD	50	TBD	mV
Gain Error		I	TBD	-1.0	TBD	% of V_{SET}
Current Drive						
Static		I	-35		+35	mA
Dynamic		IV	-100		+100	mA
Current Limit		V		40		mA
Output Resistance		I	48	50	52	Ω
Leakage Current in Inhibit Mode						
-3 V to +10 V		I	-1		+1	µA
AC CHARACTERISTICS						
Dynamic Performance						
Driver Mode						
Delay Time		III	TBD	1.2	TBD	ns
Prop Delay TC		V		2		ps/°C
Delay Time Matching Edge to Edge		V	0	70	TBD	ps
Rise and Fall Times						
1 V Swing	20 to 80%	III		1.0		ns
3 V Swing	20 to 80%	III		1.2	1.0	ns
5 V Swing	20 to 80%	III		2.0		ns

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ELECTRICAL SPECIFICATIONS

T_A = +25 °C, V_{CC} = +12 V, V_{EE}=-5.2 V, Output Load = 2 pF, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
AC CHARACTERISTICS						
Dynamic Performance						
Toggle Rate	ECL Output	IV	300			MHz
Minimum Pulse Width, V_{OUT} = 3 V		IV		1.5	TBD	ns
Overshoot, Undershoot, Preshoot		IV	-(3% V_O)-50		+(3% V_O)+50	mV
Settling Time		IV		TBD		ns
Delay Time versus PW		V		70	TBD	ps
Input Mode Delay Time R_L = 50 Ω						
Drive-to-Inhibit		III		2		ns
Inhibit-to-Drive		III		2		ns
Output Capacitance		IV		5		pF
Power Supplies						
V_{CC} to V_{EE} Range		I		18.0	18.2	V
Supply Range						
Positive Supply		I		+12.0		V
Negative Supply		I		-6.0		V
Current						
Positive Supply		I		TBD	TBD	mA
Negative Supply		I		TBD	TBD	mA
Power Dissipation		I		1.2		W

TEST LEVEL CODES

All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests; therefore, $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

PIN ASSIGNMENTS

TBD

PIN FUNCTIONS

NAME	FUNCTION
GND	Circuit Ground
V_{OUT}	Driver Output
C_{I+}	Positive Decouple
C_{I-}	Negative Decouple
V_L	Voltage Logic Low
V_H	Voltage Logic High
$\overline{D}$	Driver Input
D	Driver Input
$\overline{INH}$	Inhibit Input
V_{EE}	Negative Supply
V_{CC}	Positive Supply

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SIGNAL PROCESSING TECHNOLOGIES

SPT9101

125 MSPS SAMPLING AMPLIFIER

ADVANCED INFORMATION

FEATURES

- Second Source of AD9101
- 350 MHz Sampling Bandwidth
- 125 MHz Sampling Rate
- Excellent Hold Mode Distortion
  - -75 dB at 50 MSPS (25 MHz V_{IN})
  - -66 dB at 100 MSPS (50 MHz V_{IN})
- 7 ns Acquisition Time to 0.1%
- <1 ps Aperture Jitter
- 66 dB Feedthrough Rejection at 50 MHz
- Low Spectral Noise Density

APPLICATIONS

- Test Instrumentation Equipment
- RF Demodulation Systems
- High Performance CCD Capture
- Digital Sampling Oscilloscopes
- Commercial and Military Radar
- High Speed DAC Deglitching

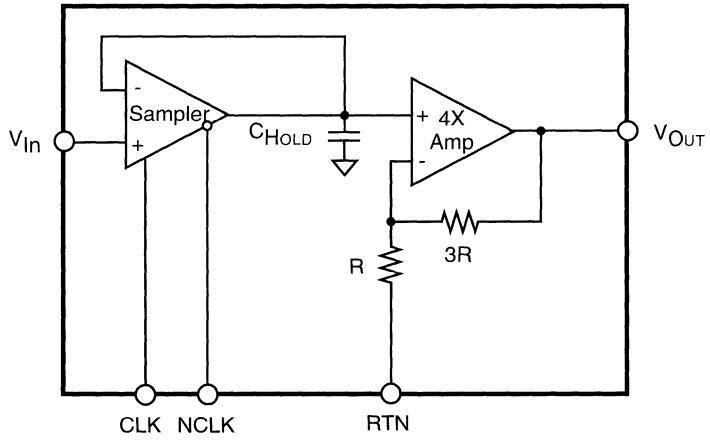
GENERAL DESCRIPTION

The SPT9101 is a high speed track-and-hold amplifier designed for a wide range of use. The SPT 9101 is capable of sampling at speeds up to 125 MSPS with resolutions ranging from 8 to 12 bits. Trim programmable internal hold and compensation capacitors provide for optimized input bandwidth and slew rate versus noise performance.

The performance of this device makes it an excellent front end driver for a wide range of ADCs on the market today. Significant improvements in dynamic performance can be achieved by using this device ahead of virtually all ADCs that do not have an internal track-and-hold.

The SPT9101 is offered in a 20L SOIC package and a 20L LCC package in the industrial temperature range. Contact the factory for military and /833 package options.

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATING (Beyond which damage may occur)[1]

Supply Voltages
- Supply Voltage ($+V_S$) ..... -0.5 V to +6 V
- Supply Voltage ($-V_S$) ..... -6 V to +0.5 V
- A/D Ground Voltage Differential ..... 0.5 V

Input Voltages
- Analog Input Voltage ..... ±5 V
- CLK, NCLK Input ..... -5 V to +0.5 V

Output Currents
- Continuous Output Current ..... 70 mA

Temperature
- Operating Temperature ..... -25 to + 85 °C
- Junction Temperature ..... + 150 °C
- Lead, Soldering (10 seconds) ..... + 220 °C
- Storage ..... -65 to + 150 °C

Note 1: Operation at any Absolute Maximum Ratings is not implied. See Electrical Specifications for proper nominal applied conditions in typical application.

ELECTRICAL SPECIFICATIONS

$T_A=T_{MIN}$ - T_{MAX}, V_{CC}=+5.0 V, V_{EE}=-5.2 V, V_{IN}=±1.0 V, V_{RB}=-1.0 V, V_{RT}=+1.0 V, f_{clock}=100 MHz, 50% clock duty cycle, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
DC Performance						
Gain ΔV_{IN} = 0.5 V	+25 °C		3.93	4.0	4.07	V/V
	Full Temp.		3.9		4.1	V/V
Offset ΔV_{IN} = 0 V	+25 °C			±3	±10	mV
	Full Temp.				±15	mV
Output Resistance	+25 °C			0.4		Ω
Output Drive Capacity	Full Temp.		±60	±70		mA
PSRR ΔV_S = 0.5 V p-p	+25 °C		37	43		dB
Pedestal Sensitivity to Pos. Supply				4		mV/V
ΔV_S = 0.5 V p-p	Full Temp.					
Pedestal Sensitivity to Neg. Supply				8		mV/V
ΔV_S = 0.5 V p-p	Full Temp.					
Analog Input/Output						
Output Voltage Range	Full Temp.		±2.4	±2.7		V
Input Bias Current	+25 °C			-50		µA
Input Capacitance	+25 °C			2		pF
Input Resistance	+25 °C to T_{MAX}		30	125		kΩ
	T_{MIN}		25			kΩ
Clock Inputs						
Input Bias Current	+25 °C			25		µA
Input Low Voltage			-1.8		-1.5	V
ΔV_S = 0.5 V p-p	Full Temp.					
Input High Voltage			-1.0		-0.8	V
ΔV_S = 0.5 V p-p	Full Temp.					
Track Mode Dynamics						
Bandwidth (-3 dB) Vout = 1.0 V p-p	Full Temp.		160	250		MHz
Slew Rate 4 V Output Step	Full Temp.		1300	1800		V/µs
Overdrive Recovery Time[1]	To 0.1%			55		ns
Integrated Output Noise	BW = 5 to 200 MHz			270		µV
Input RMS Spectral Noise	10 MHz			4.3		$nV/\sqrt{Hz}$

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ELECTRICAL SPECIFICATIONS

$T_A=T_{min}$ - T_{max}, V_{CC}=+5.0 V, V_{EE}=-5.2 V, V_{IN}=±1.0 V, V_{RB}=-1.0 V, V_{RT}=+1.0 V, f_{clock}=100 MHz, 50% clock duty cycle, unless otherwise specified.

PARAMETERS	TEST CONDITIONS	TEST LEVEL	MIN	TYP	MAX	UNITS
Hold Mode Dynamics						
Worst Harmonic	23 MHz, 50 MSPS			-75		dBFS
V_{Out} = 2 V p-p	+25 °C					
Worst Harmonic	48 MHz, 100 MSPS			-66	-60	dBFS
V_{Out} = 2 V p-p	+25 °C					
Worst Harmonic	48 MHz, 100 MSPS				-57	dBFS
V_{Out} = 2 V p-p	Full Temp.					
Worst Harmonic	48 MHz, 125 MSPS			-60		dBFS
V_{Out} = 2 V p-p	+25 °C					
Sampling Bandwidth[2]	-3 dB, +25 °C			350		MHz
V_{IN} = 0.5 V p-p						
Hold Noise[3] (RMS)	+25 °C			450 x t_H		mV/s
	Full Temp.					
Droop Rate (RMS)	+25 °C			±20		mV/µs
At 50 MHz and 4 V p-p	Full Temp.					
Feedthrough Rejection (50 MHz)				-66		dB
Vout = 2 V p-p	Full Temp.					
Track-and-Hold Switching						
Aperture Delay	+25 °C			-250		ps
Aperture Jitter	+25 °C			<1		ps rms
Pedestal Offset	+25 °C			±10		mV
Transient Amplitude	V_{IN} = 0 V			16		mV
Full Temp.						
Settling Time to 3 mV	Full Temp.			4		ns
Glitch Product[4]	+25 °C			40		pV-s
V_{IN} = 0 V						
Hold-to-Track Switching						
Acquisition Time to 0.1%	+25 °C			7		ns
2 V Output Step						
Acquisition Time to 0.01%	+25 °C			11	14	ns
2 V Output Step	Full Temp.				16	ns
Power Supply						
+V_S Current	Full Temp.			52	70	mA
-V_S Current	Full Temp.			58	72	mA
Power Dissipation	Full Temp.			550	710	mW

[1]Time to recover within rated error band from 160% overdrive.
[2]Sampling bandwidth is defined as the -3 dB frequency response of the input sampler to the hold capacitor when operating in the sampling mode. It is greater than tracking bandwidth because it does not include the bandwidth of the output amplifier.
[3]Hold mode noise is proportional to the length of time a signal is held. For example, if the hold time (t_H) is 20 ns, the accumulated noise is typically 3 µV (150 mV/s x 20 ns). This value must be combined with the track mode noise to obtain total noise.
[4]Total energy of worst case track-to-hold or hold-to-track glitch.

TEST LEVEL CODES

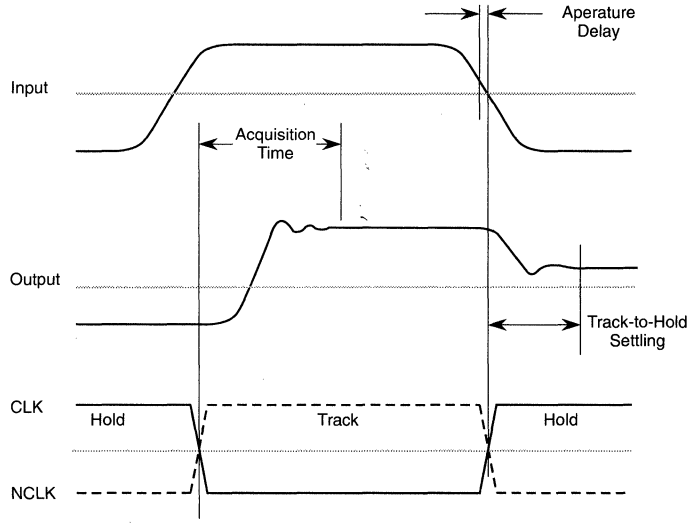
All electrical characteristics are subject to the following conditions:

All parameters having min/max specifications are guaranteed. The Test Level column indicates the specific device testing actually performed during production and Quality Assurance inspection. Any blank section in the data column indicates that the specification is not tested at the specified condition.

Unless otherwise noted, all tests are pulsed tests; therefore, $T_J = T_C = T_A$.

TEST LEVEL	TEST PROCEDURE
I	100% production tested at the specified temperature.
II	100% production tested at T_A=25 °C, and sample tested at the specified temperatures.
III	QA sample tested only at the specified temperatures.
IV	Parameter is guaranteed (but not tested) by design and characterization data.
V	Parameter is a typical value for information purposes only.
VI	100% production tested at T_A = 25 °C. Parameter is guaranteed over specified temperature range.

Figure 1 - Timing Diagram



TIMING SPECIFICATION DEFINITIONS

ACQUISITION TIME

This is the time it takes the SPT9101 to acquire the analog signal when it makes a transition from hold mode to track mode. It is measured from the 50% input clock transition point to the point when the signal is within a specified error band at the hold capacitor.

TRACK-TO-HOLD SETTLING TIME

The time required for the output to settle to within 4 mV of its final value.

APERTURE DELAY

The aperture delay time is the interval between the leading edge transition of the clock input and the instant when the input signal was equal to the held value. It is the difference in time between the digital hold switch delay and the analog signal propagation time. Because the analog propagation time is longer than the digital delay in the SPT9101, the aperture delay is a negative value.

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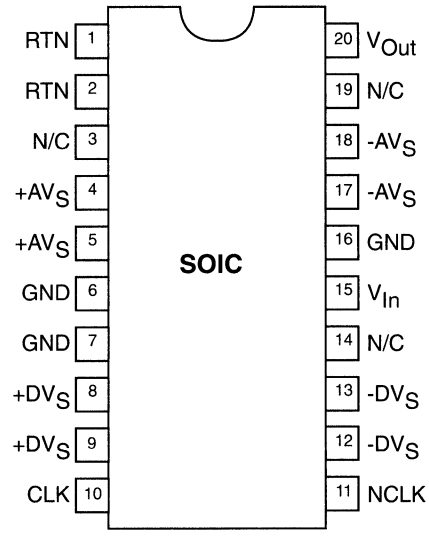
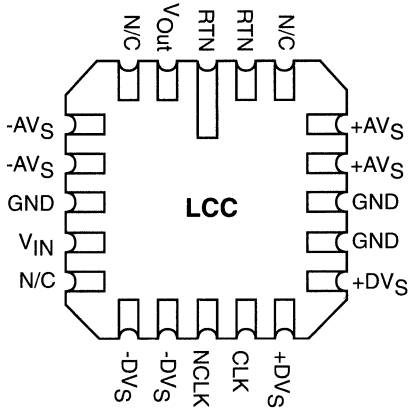
PIN ASSIGNMENTS





PIN FUNCTIONS

RTN	Gain Set Resister Return
$+AV_S$	+5 V Power Supply (Analog)
GND	Hold Capacitor Ground
$+DV_S$	+5 V Power Supply (Digital)
CLK	True ECL T/H Clock
NCLK	Complement ECL T/H Clock
$-DV_S$	-5.2 V Power Supply (Digital)
N/C	No Connection
V_{IN}	Analog Signal Input
	GND Ground (Signal Return)
$-AV_S$	-5.2 V Power Supply (Analog)
V_{OUT}	Analog Signal Output

7

LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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Section 8 Evaluation Boards

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SIGNAL PROCESSING TECHNOLOGIES

EB104
EVALUATION BOARD

FEATURES

- Provides Operating Environment for HADC574Z, HADC674Z, or SPT774 Devices
- Fully Demonstrates Device Function and Resolution
- Eliminates Noisy Breadboard Evaluation Circuitry
- Buffered A/D and D/A Conversion Data Buses
- Includes Sample/Hold-Amp and Output Op Amp ICs
- Unipolar or Bipolar Operation

APPLICATIONS

- Evaluation/Comparison of HADC574, HADC674Z and SPT774 Converters
- System Development
- Data Acquisition Systems
- Bus Structured Instumentation
- Process Control Systems

GENERAL DESCRIPTION

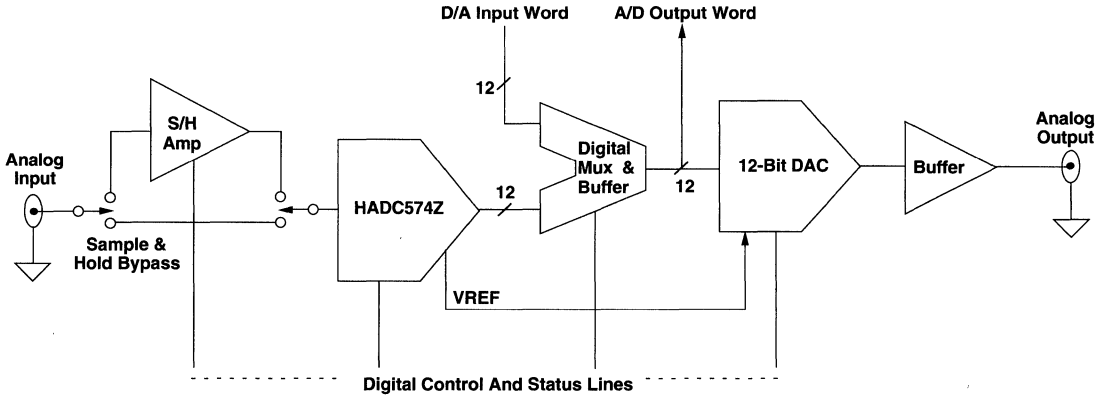
The EB104 evaluation board fully demonstrates the capabilities of the HADC574/674Z and SPT774 12-bit analog-to-digital converters. All of the basic power supply connections, control lines, and external components are included. Unlike most laboratory breadboarding, the ground-planed PC board provides the necessary low-noise environment essential for 12-bit resolution. The board makes full use of connectors to allow easy hookup and operation.

Other support provided on the EB104 includes an input sample/hold amplifier, output operational amplifiers and potentiometers for offset and gain adjustments. Customization and function selections are performed by jumper pins.

The EB104 is supplied with an HADC574ZBCJ device. It will support all 574/674/774 type devices.

8

BLOCK DIAGRAM



SIGNAL PROCESSING TECHNOLOGIES

EB1175
EVALUATION BOARD

FEATURES

- 30 MSPS Conversion Rate
- On-Board Reference Circuit
- Analog Input Buffer
- Clock Input/Clock Divider Circuit
- On-Board Reconstruction DAC

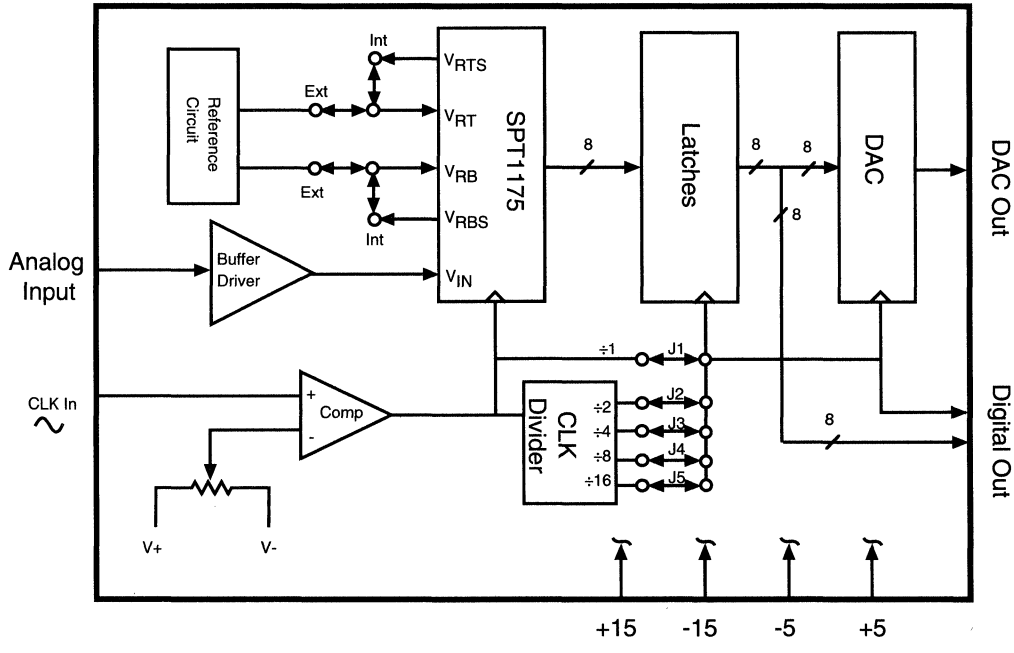
APPLICATIONS

- Evaluation of the SPT1175, 8-bit 30 MSPS ADC
- Engineering System Prototype Aide
- Incoming Inspection Tool
- AC and DC Accuracy Testing
- Guide for System Layout

GENERAL DESCRIPTION

The EB1175 is intended to be used as a tool for evaluation and characterization of the SPT1175, monolithic 8-bit 30 MSPS ADC. This application note is a supplement to the data sheet, including more detailed technical information of the interfacing circuits required. The evaluation board is designed to cover a wide variety of applications, but can also be greatly simplified to suit a specific application. Contact the SPT Applications Engineering department if assistance is needed.

BLOCK DIAGRAM



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SIGNAL PROCESSING TECHNOLOGIES

EB5220
EVALUATION BOARD

FEATURES

- Up to 80 MWPS Conversion Rate
- Manual Format and Video Controls Available
- Internal Feference Provided

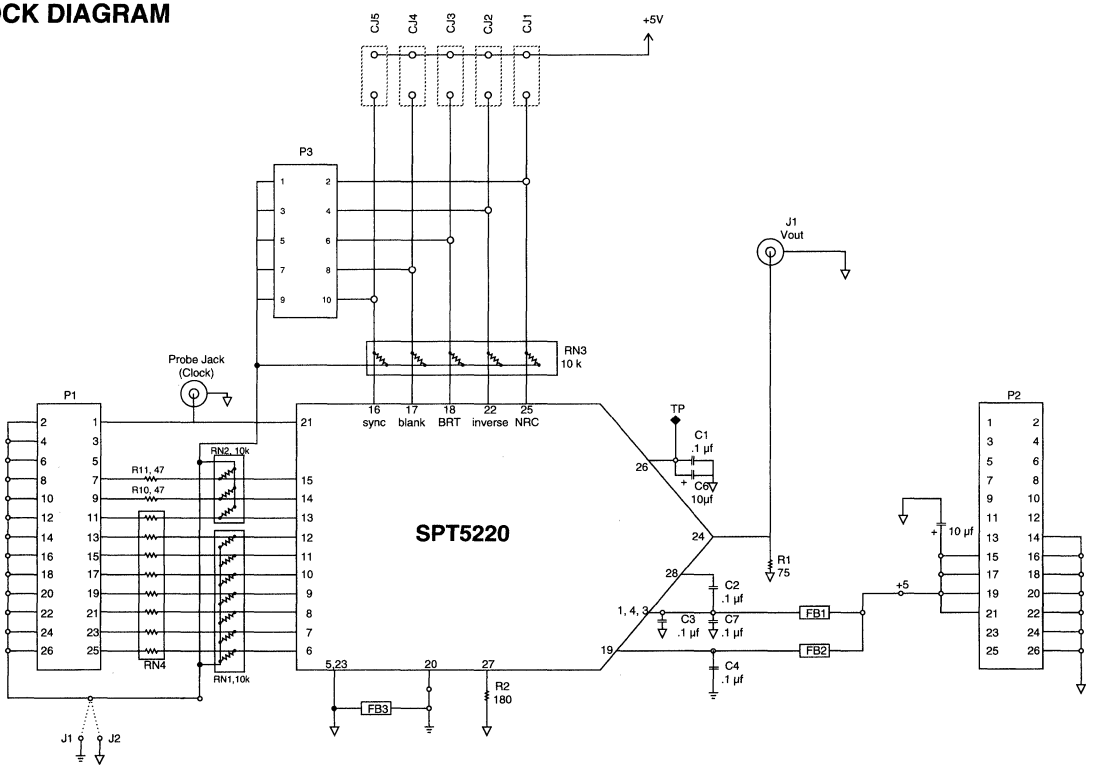
APPLICATIONS

- Evaluation of SPT5220
- Engineering Prototype Aid
- Incoming Inspection Tool
- Guide for System Layout

GENERAL DESCRIPTION

The EB5220 evaluation board is intended to be used as a tool for device characterization and to demonstrate the performance of the SPT5220. The SPT5220 is a monolithic 10-bit, 80 MWPS CMOS DAC for high-resolution color graphics and video system applications. It generates RS-343A and RS-170 video outputs capable of driving a singly-terminated 75 Ω load without the need for external buffers. A 10-bit word is applied to P1, video controls are applied to P3 and power is applied to P2. The analog output can then be observed at J1.

BLOCK DIAGRAM



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SIGNAL PROCESSING TECHNOLOGIES

EB7610
EVALUATION BOARD
ADVANCE INFORMATION

FEATURES

- 1 GSPS Conversion Rate
- On-Board Reference Driver
- Differential Clock Driver
- On-Board Reconstruction DAC
- Full Speed Digital Output Through High Speed Connector
- Decimated Digital Data Output Through 37 D-Connector
- Selectable Decimation Divide by 16/32/64/128
- Programmable Clock Delay Line

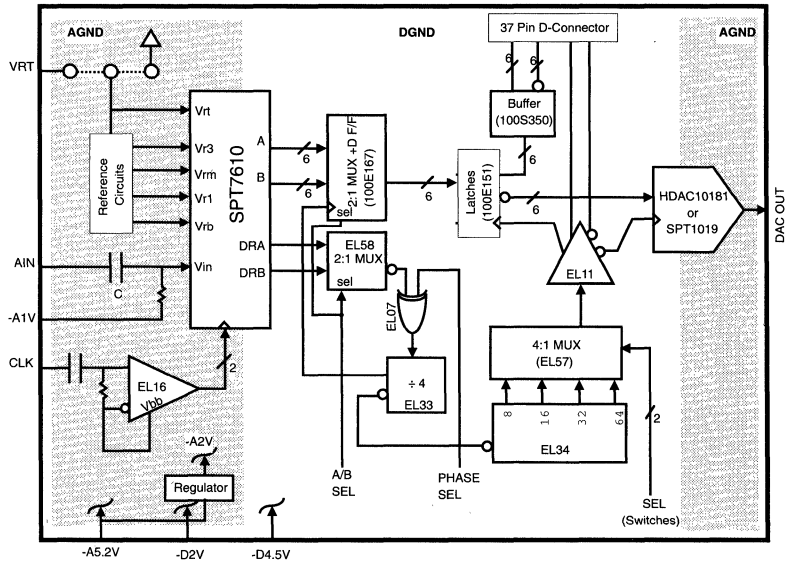
APPLICATIONS

- Evaluation of SPT7610
- Engineering System Prototype
- Guide for Design of SPT7610 Interface Circuitry
- Guide for Design of SPT7610 PCB Layout

GENERAL DESCRIPTION

The EB7610 is intended to be used as a tool for evaluation and characterization of the SPT7610, 6-bit 1 GSPS ADC. At such a high sampling rate, a printed circuit board is essential for proper evaluation. This application note is a supplement to the data sheet, including more detailed technical information of the interfacing circuits required. The evaluation board is designed to cover a wide variety of applications, but can also be greatly simplified to suit a specific application. Contact the SPT Applications Engineering department if assistance is needed.

BLOCK DIAGRAM



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SPT
SIGNAL PROCESSING TECHNOLOGIES

EB7710/25
EVALUATION BOARD

FEATURES

- 150/300 MHz Conversion Rate
- On Board Reference Circuit
- AC or DC Coupled Input
- Clock Input/Clock Divider Circuit
- On Board Reconstruction DAC

APPLICATIONS

- Evaluation of the SPT7710/25
- Engineering System Prototype Aid
- Incoming Inspection Tool
- AC and DC Accuracy Testing
- Guide for System Layout

GENERAL DESCRIPTION

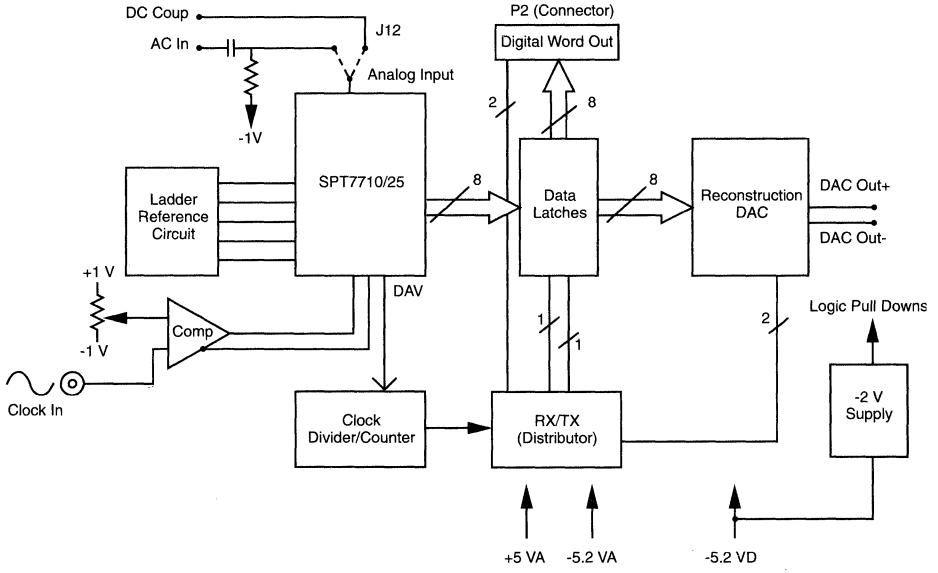
The EB7710/25 is a tool for the evaluation and characterization of the SPT7710 (150 MHz) or SPT7725 (300 MHz) ADCs in the PGA package. This application note is an addendum to the product data sheets and provides a more detailed description of the device and the interfacing circuits.

The evaluation board is designed to cover a wide variety of applications. It can also be simplified to suit a specific application. Contact the SPT applications engineering department for assistance.

The dimensions of the EB7710/25 are 5.25 by 7.43 inches. Electrically it consists of several sections, each of which is explained in the application note.

- Power connections
- Reference circuit
- Analog input circuit
- SPT7710/25 A/D converter
- Clock driver/divider circuit
- Digital output latches

BLOCK DIAGRAM



8

SIGNAL PROCESSING TECHNOLOGIES

EB7750/55/60
EVALUATION BOARD

FEATURES

- 1 GSPS Conversion Rate
- On-Board Reconstruction DAC
- On-Board Reference Circuit
- Full Speed Digital Output Through a High Speed Connector
- Decimated Digital Data Output
- Selectable Decimation Divide by 16/32/64/128 Options
- On-Board Gray-to-Binary Conversion
- Available in Two Versions: Fully & Partially Loaded

APPLICATIONS

- Evaluation of SPT7750, SPT7755, or SPT7760 8-bit ADCs
- Engineering System Prototype Aid
- Guide for Design of SPT7750/55/60 Interface Circuitry
- Guide for Design of SPT7750/55/60 PCB Layout

GENERAL DESCRIPTION

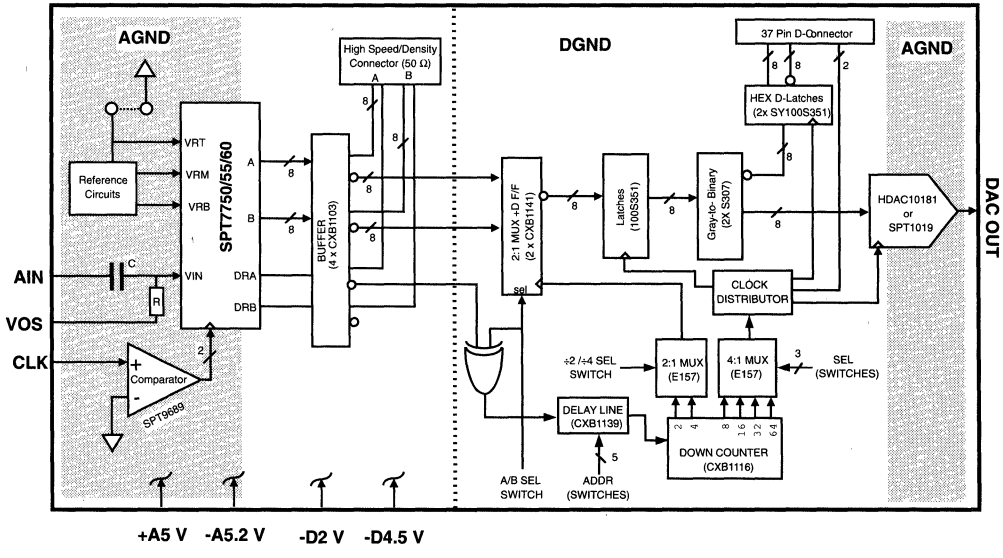
The EB7750/55/60-1 evaluation board is intended to be used as a tool for device characterization and demonstration of the performance of the SPT7750, SPT7755 and SPT7760 A/D converters. The parts have guaranteed minimum sample rates as follows: 500 MSPS for the SPT7750, 750 MSPS for the SPT7755, and 1 GSPS for the SPT7760. At these high conversion speeds a printed circuit board is a must. Hand-crafted bread boards simply will not work effectively at these speeds.

SPECIAL REQUIREMENTS

The SPT7750/55/60 devices require adequate heat sinking and air flow for optimum performance.

The EB7750/55-1 comes with the SPT7750AIK, SPT7755AIK or SPT7760AIK in an 80-lead MQUAD surface mount package directly soldered to the board for optimum performance. The EB7750/55/60-1 is capable of operating at clock rates up to 1 GSPS (clock rates higher than 1 GSPS are possible but not guaranteed). The block diagram overview of the board is shown in the block diagram. Note that adequate air flow and a heat sink are necessary for optimum performance of the ADC.

BLOCK DIAGRAM



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SIGNAL PROCESSING TECHNOLOGIES

EB7810/14
EVALUATION BOARD

FEATURES

- 20 and 40 MSPS Conversion Rates
- On-Board Reconstruction DAC
- Data Output and Strobe Signal - ECL
- Data Output and Strobe Signal - TTL
- User Selectable Capture Clock
- On Board Reference Drivers
- On Board Power Supplies to SPT7810/14

APPLICATIONS

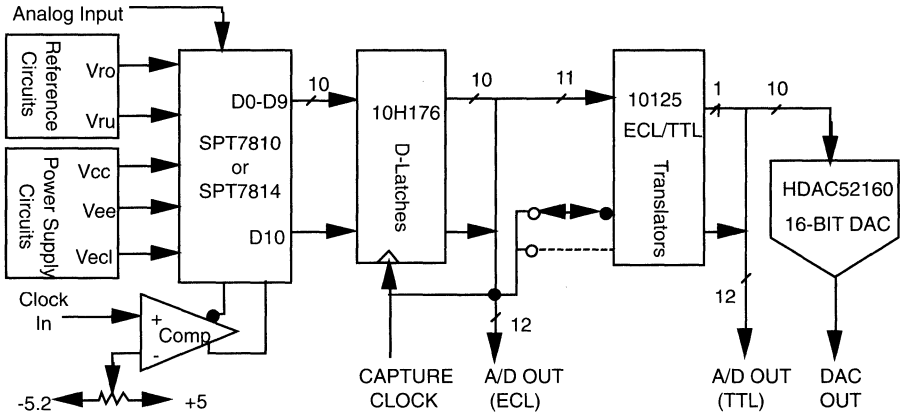
- Evaluation of SPT7810 and SPT7814
- Engineering System Prototype Aid
- Differential Clock Driver
- Incoming Inspection Tool
- Differential Linearity Error (DLE) Testing
- Integral Linearity Error (ILE) Testing
- AC Accuracy Testing: SNR, THD
- Power Supply Sensitivity Testing
- Guide for the System Layout

GENERAL DESCRIPTION

The EB7810/14 Evaluation Board is intended to demonstrate the performance of the SPT7810 and SPT7814, monolithic high speed analog-to-digital converters (ADC). Both the SPT7810 and SPT7814 have an analog input range of ±2 V.

The SPT7810 is capable of digitizing an analog input signal up to 10 MHz into 10-bit words at a minimum of 20 MSPS update rate, while the SPT7814 is capable of digitizing an analog input signal up to 20 MHz into 10-bit words at a minimum of 40 MSPS update rate. They are pin compatible.

BLOCK DIAGRAM



The EB7810/14 consists of seven separate sections:

- Reference circuits
- Power Supply circuits
- SPT7810 or SPT7814, 10-bit ADC
- Clock driver circuit
- Output ECL data latches available through 26-pin female ribbon connector
- ECL-to-TTL output translators available through 26-pin female ribbon connector

SIGNAL PROCESSING TECHNOLOGIES

EB7820/24
EVALUATION BOARD

FEATURES

- 20 and 40 MSPS Conversion Rate
- On-Board Clock Drivers
- Data Output and Strobe Signal
- User Selectable Capture Clock
- On-Board Reference Drivers
- Dimension : ≈ 4.0" X 7.5"

APPLICATIONS

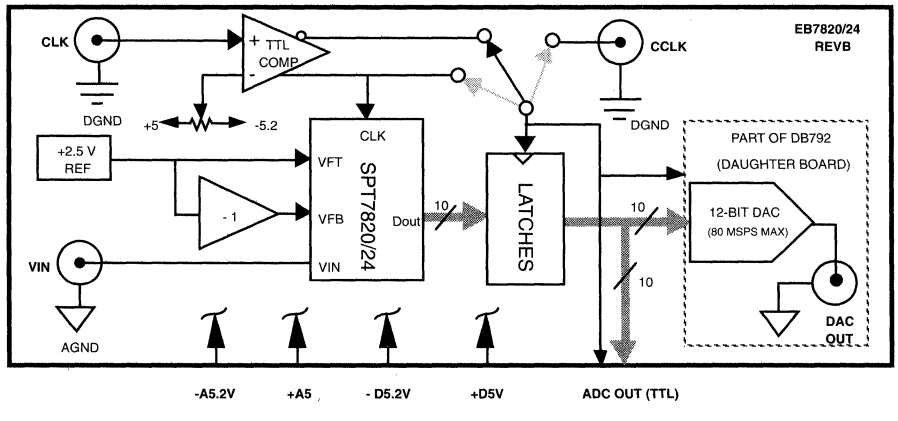
- Evaluation of SPT7820 and SPT7824
- Engineering System Prototype Aid
- Incoming Inspection Tool
- Differential Linearity Error (DLE) Testing
- Integral Linearity Error (ILE) Testing
- AC Accuracy Testing: SNR, THD
- Guide for System Layout

GENERAL DESCRIPTION

The EB7820/24 evaluation board demonstrates the performance of the SPT7820 and SPT7824, monolithic high speed analog-to-digital converters (ADCs). This document can used as an application note and as supplemental information to the existing data sheets (SPT7820 or SPT7824). Both the SPT7820 and SPT7824 have analog input ranges of ±2 V.

The SPT7820 is capable of digitizing an analog input signal into 10-bit words at a minimum update rate of 20 MSPS, while the SPT7824 is capable of digitizing an analog input signal into 10-bit words at a minimum update rate of 40 MSPS. Both devices are pin-compatible. All input/output logic is TTL-compatible.

BLOCK DIAGRAM



The EB7820/24 (≈ 4" X 7.5") consists of five separate sections:

- Reference circuits
- Clock circuits
- SPT7820 or SPT7824, 10-bit ADC (not included with the board)
- Output latches available through 26-pin female ribbon connector
- The DB792 DAC reconstruction board is a separate daughter board (≈ 2.5" X 3.0") that directly interfaces with the EB7820/24

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SIGNAL PROCESSING TECHNOLOGIES

EB7830
EVALUATION BOARD

FEATURES

- 100 kSPS to 2.5 MSPS Conversion Rate
- On-Board Reference Driver
- Clock Driver
- Analog Input Driver/Level Shift
- On-Board Serial to Parallel Converter
- 3 V Logic Digital Output Connector
- 5 V Logic Digital Output Connector
- 3 V to 5 V Logic Operation
- Clock Generation for Self Start

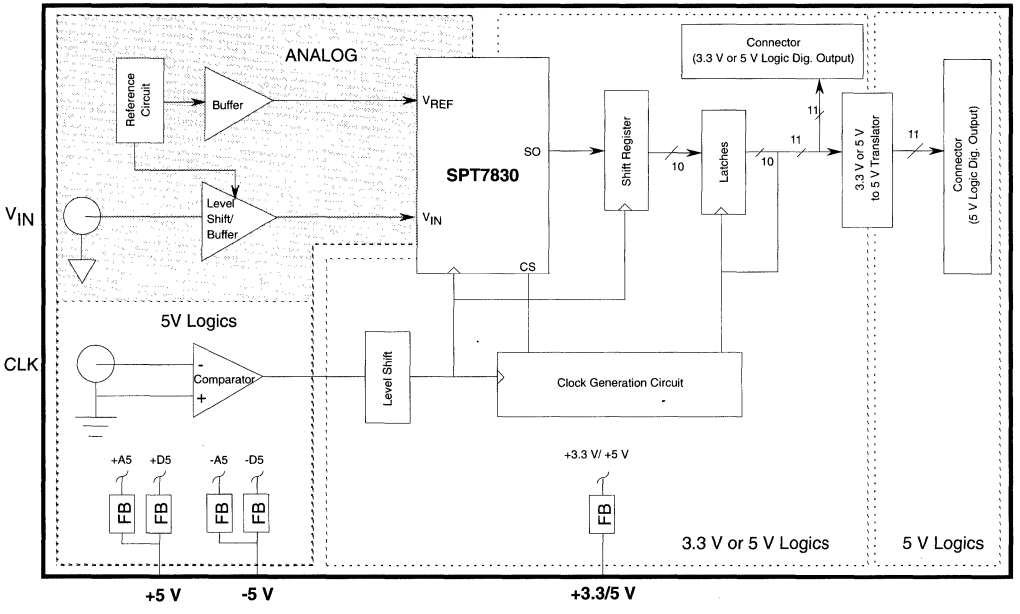
APPLICATIONS

- Evaluation of SPT7830
- Engineering System Prototype Aid
- Incoming Inspection Tool
- Guide for Design of SPT7830 Interface Circuitry
- Guide for Design of SPT7850 PCB Layout

GENERAL DESCRIPTION

The EB7830 is intended to be used as a tool for evaluation and characterization of the SPT7830, serial 10-bit 2.5 MSPS ADC. This application note is a supplement to the data sheet, including more detailed technical information of the interfacing circuits required. The evaluation board is designed to cover a wide variety of applications, but can also be greatly simplified to suit a specific application. Contact the SPT Applications Engineering department if assistance is needed.

BLOCK DIAGRAM



8

SIGNAL PROCESSING TECHNOLOGIES

EB7835/40/50
EVALUATION BOARD

FEATURES

- 5, 10 and 20 MSPS Conversion Rates
- Data Output Latch
- On-Board Reference Circuits
- Analog Input Buffer
- Regulated Power Supplies

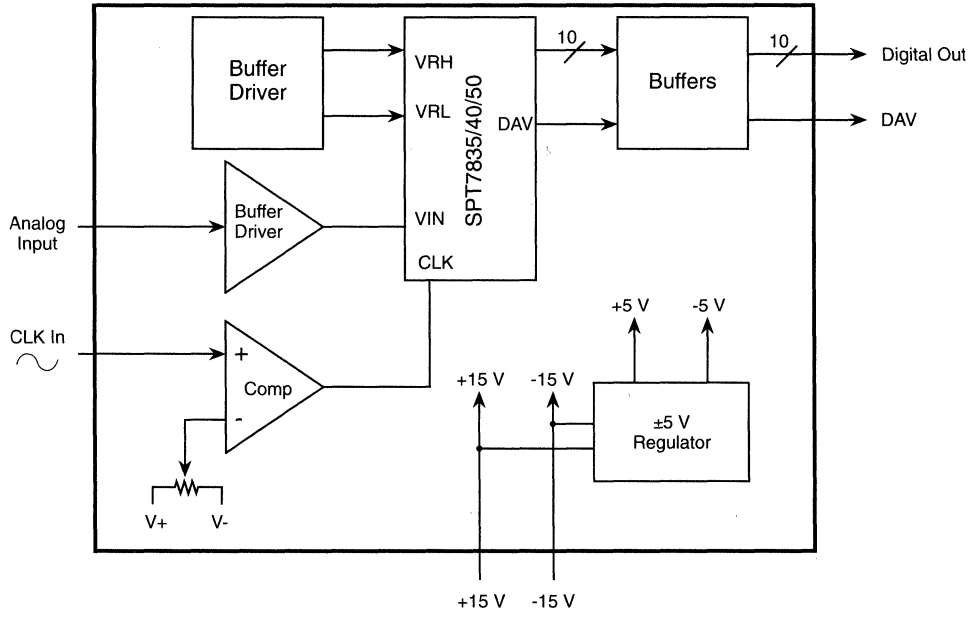
APPLICATIONS

- Evaluation of SPT7835/40/50 10-bit ADCs
- Engineering System Prototype Aid
- Incoming Inspection Tool
- Guide for System Layout

GENERAL DESCRIPTION

The EB7835/40/50 evaluation board is intended to be used as a tool for device characterization and to demonstrate the performance of the SPT7835/40/50 family of A/D converters. With an appropriate external clock frequency adjustment, the board can be used with each member of the family. This evaluation board can also be used with SPT7855 and SPT7860. Refer to EB7855/60.

BLOCK DIAGRAM



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SIGNAL PROCESSING TECHNOLOGIES

EB7855/60
EVALUATION BOARD

FEATURES

- 25 and 40 MSPS Conversion Rates
- Data Output Latch
- On-Board Reference Circuits
- Analog Input Buffer
- Regulated Power Supplies

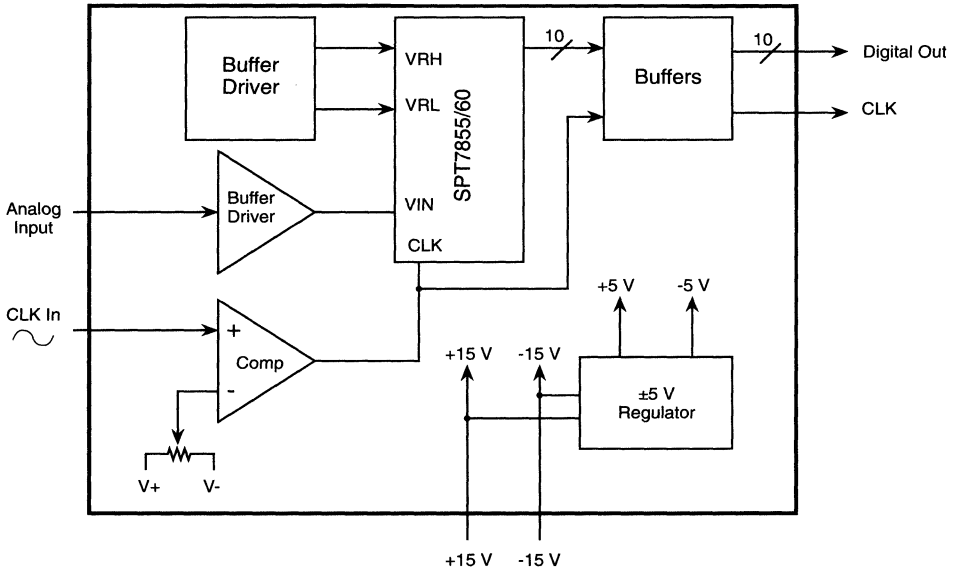
APPLICATIONS

- Evaluation of SPT7855/60 10-bit ADCs
- Engineering System Prototype Aid
- Incoming Inspection Tool
- Guide for System Layout

GENERAL DESCRIPTION

The EB7855/60 evaluation board is intended to be used as a tool for device characterization and to demonstrate the performance of the SPT7855/60 family of A/D converters. With an appropriate external clock frequency adjustment, the board can be used with each member of the family. This evaluation board can also be used with SPT7835, SPT7840 and SPT7850. Refer to EB7835/40/50.

BLOCK DIAGRAM



8

SIGNAL PROCESSING TECHNOLOGIES

EB7870
EVALUATION BOARD

FEATURES

- 100 MSPS Conversion Rate
- Differential Clock Driver
- Digital Output Connector

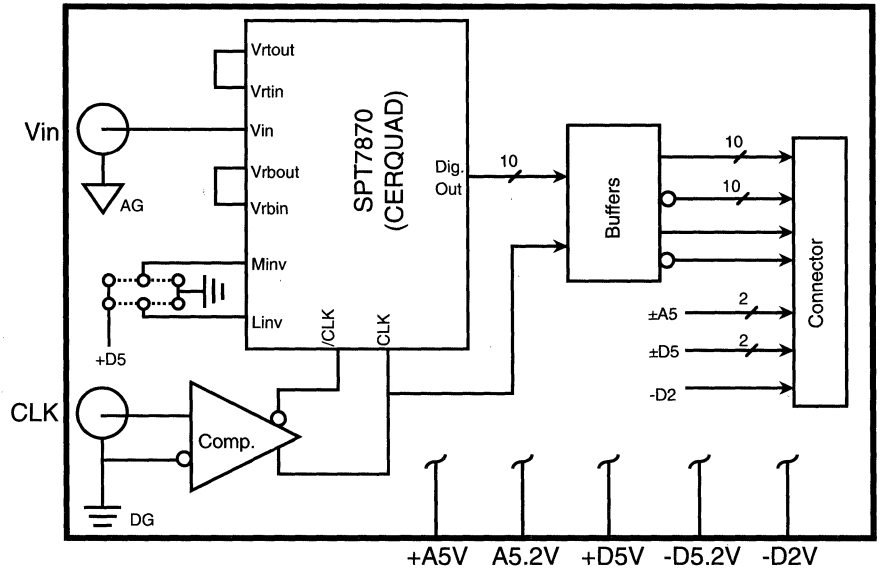
APPLICATIONS

- Evaluation of SPT7870
- Engineering System Prototype Aid
- Guide to Design of SPT7870 Interface Circuit
- Guide for Design of SPT7870 PCB Layout

GENERAL DESCRIPTION

The EB7870 is intended to be used as a tool for evaluation and characterization of the SPT7870, 10-bit 100 MSPS ADC. This application note is a supplement to the data sheet, including more detailed technical information of the interfacing circuits required. The evaluation board is designed to cover a wide variety of applications, but can also be greatly simplified to suit a specific application. Contact the SPT Applications Engineering department if assistance is needed.

BLOCK DIAGRAM



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SIGNAL PROCESSING TECHNOLOGIES

EB7871
EVALUATION BOARD

FEATURES

- 100 MSPS Conversion Rate
- Differential Clock Driver
- Digital Output Connector

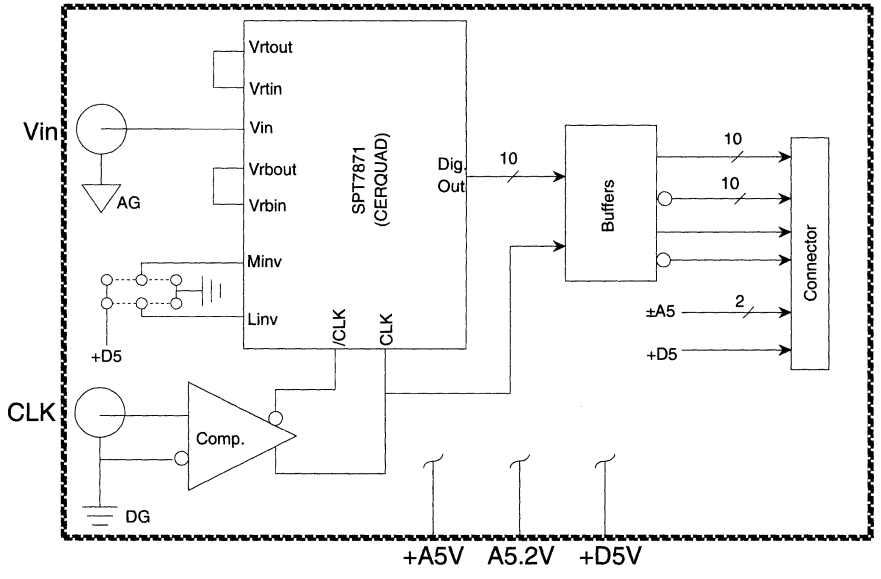
APPLICATIONS

- Evaluation of SPT7871
- Engineering System Prototype Aid
- Guide to Design of SPT7870 Interface Circuit
- Guide for Design of SPT7870 PCB Layout

GENERAL DESCRIPTION

The EB7871 is intended to be used as a tool for evaluation and characterization of the SPT7871, 10-bit 100 MSPS ADC. This application note is a supplement to the data sheet, including more detailed technical information of the interfacing circuits required. The evaluation board is designed to cover a wide variety of applications, but can also be greatly simplified to suit a specific application. Contact the SPT Applications Engineering department if assistance is needed.

BLOCK DIAGRAM



8

SIGNAL PROCESSING TECHNOLOGIES

EB7910/12
EVALUATION BOARD

FEATURES

- 30 MSPS Conversion Rate
- On-Board Reconstruction DAC
- Differential Clock Driver
- Data Output and Strobe Signal - ECL
- Data Output and Strobe Signal - TTL
- User Selectable Capture Clock
- On Board Reference Drivers
- On Board Power Supplies for SPT7910/12

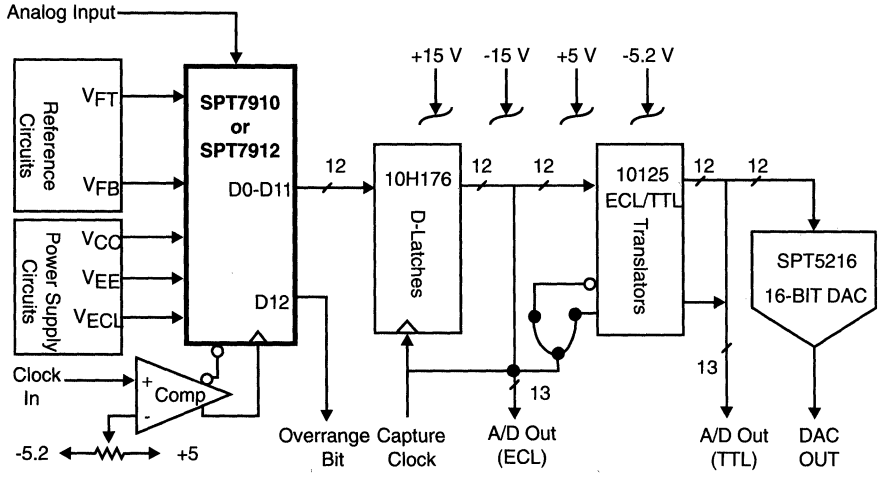
APPLICATIONS

- Evaluation of SPT7910 and SPT7912
- Engineering System Prototype Aid
- Incoming Inspection Tool
- Differential Linearity Error (DLE) Testing
- Integral Linearity Error (ILE) Testing
- AC Accuracy Testing: SNR, THD
- Power Supply Sensitivity Testing
- Guide for System Layout

GENERAL DESCRIPTION

The EB7910/12 evaluation board is intended to demonstrate the performance of the SPT7910 and SPT7912, monolithic high speed analog-to-digital converters (ADC). Both the SPT7910 and SPT7912 have an analog input range of ±2 V. The SPT7910 is capable of digitizing an analog input signal up to 5 MHz into 12-bit words at a minimum update rate of 10 MSPS, while the SPT7912 is capable of digitizing an analog input signal up to 10 MHz into 12-bit words at a minimum update rate of 30 MSPS.

BLOCK DIAGRAM



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SIGNAL PROCESSING TECHNOLOGIES

EB7920/22
EVALUATION BOARD

FEATURES

- Up to 30 MSPS Conversion Rate
- On-Board Clock Drivers
- Data Output and Strobe Signal
- User Selectable Capture Clock
- On-Board Reference Drivers
- Dimension: ≈ 4.0" X 7.5"

APPLICATIONS

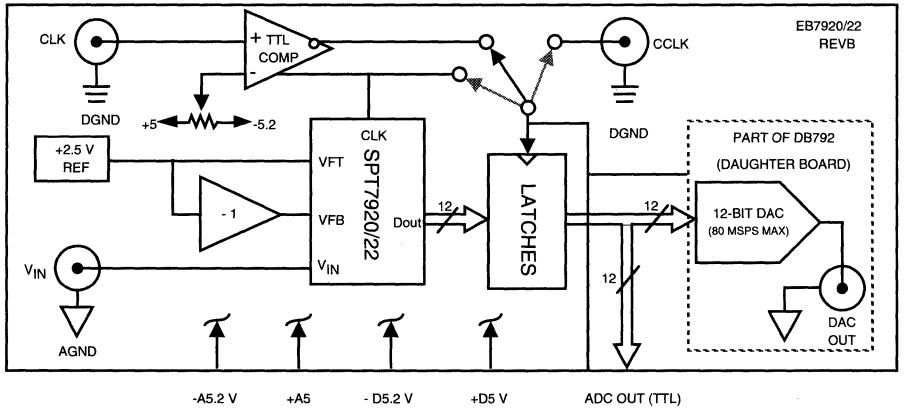
- Evaluation of SPT7920 and SPT7922
- Engineering System Prototype Aid
- Incoming Inspection Tool
- Differential Linearity Error (DLE) Testing
- Integral Linearity Error (ILE) Testing
- AC Accuracy Testing: SNR, THD
- Guide for System Layout

GENERAL DESCRIPTION

The EB7920/22 evaluation board demonstrates the performance of the SPT7920 and SPT7922, monolithic high speed analog-to-digital converters (ADCs). This document can also be used as an application note or as supplemental information to the existing data sheet (SPT7920 or SPT7922).

Both the SPT7920 and SPT7922 have analog input ranges of ±2 V. The SPT7920 is capable of digitizing an analog input signal into 12-bit words at a minimum update rate of 10 MSPS, while the SPT7922 is capable of digitizing an analog input signal into 12-bit words at an update rate of a minimum of 30 MSPS. Both devices are pin-compatible. The input/output logic is TTL-compatible.

BLOCK DIAGRAM



The EB7920/22 (≈ 4" X 7.5") consists of five separate sections:
- Reference circuits
- Clock circuits
- SPT7920 or SPT7922, 12-bit ADC
- Output latches available through 26-pin female ribbon connector
- DAC reconstruction board, DB792, is a separate daughter board (≈2.5" X 3.0") which directly interfaces with the EB7920/22

SIGNAL PROCESSING TECHNOLOGIES

EB9101

EVALUATION BOARD

ADVANCE INFORMATION

FEATURES

- 125 MHz Sampling Rate
- Differential Clock Driver

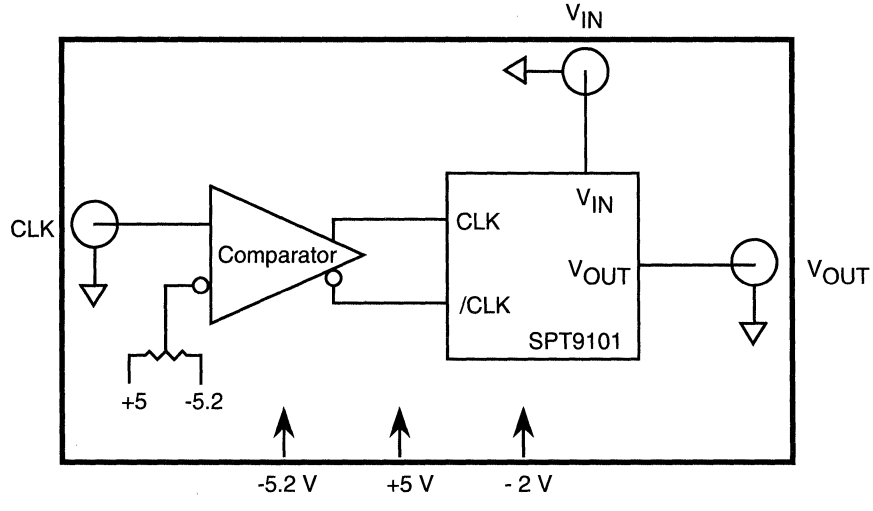
APPLICATIONS

- Evaluation of SPT9101
- Engineering System Prototype Aid
- Guide to Design of SPT9101 Interface Circuit
- Guide for Design of SPT9101 PCB Layout

GENERAL DESCRIPTION

The EB9101 is intended to be used as a tool for evaluation and characterization of the SPT9101, track-and-hold amplifier. This application note is a supplement to the data sheet, including more detailed technical information of the interfacing circuits required. The evaluation board is designed to cover a wide variety of applications, but can also be greatly simplified to suit a specific application. Contact the SPT Applications Engineering department if assistance is needed.

BLOCK DIAGRAM



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SIGNAL PROCESSING TECHNOLOGIES

EB9712
EVALUATION BOARD
ADVANCE INFORMATION

FEATURES

- 100 MWPS Conversion Rate
- ECL Digital Input Connector
- On-Board Latches

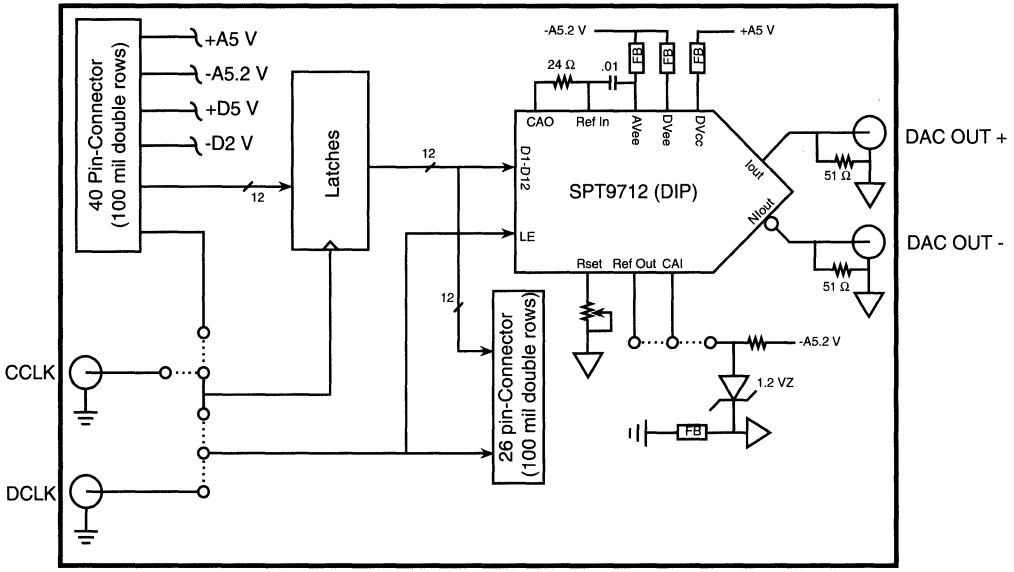
APPLICATIONS

- Evaluation of SPT9712
- Engineering System Prototype Aid
- Guide to Design of SPT9712 Interface Circuitry
- Guide for Design of SPT9712 PCB Layout
- Reconstruction DAC for other SPT, ADC Devices-ECL

GENERAL DESCRIPTION

The EB9712 is intended to be used as a tool for evaluation and characterization of the SPT9712, 12-bit 100 MWPS DAC. This application note is a supplement to the data sheet, including more detailed technical information of the interfacing circuits required. The evaluation board is designed to cover a wide variety of applications, but can also be greatly simplified to suit a specific application. Contact the SPT Applications Engineering department if assistance is needed.

BLOCK DIAGRAM



8

SIGNAL PROCESSING TECHNOLOGIES

EB9713
EVALUATION BOARD
ADVANCE INFORMATION

FEATURES

- 100 MWPS Update Rate
- TTL Digital Input Connector
- On-Board Latches

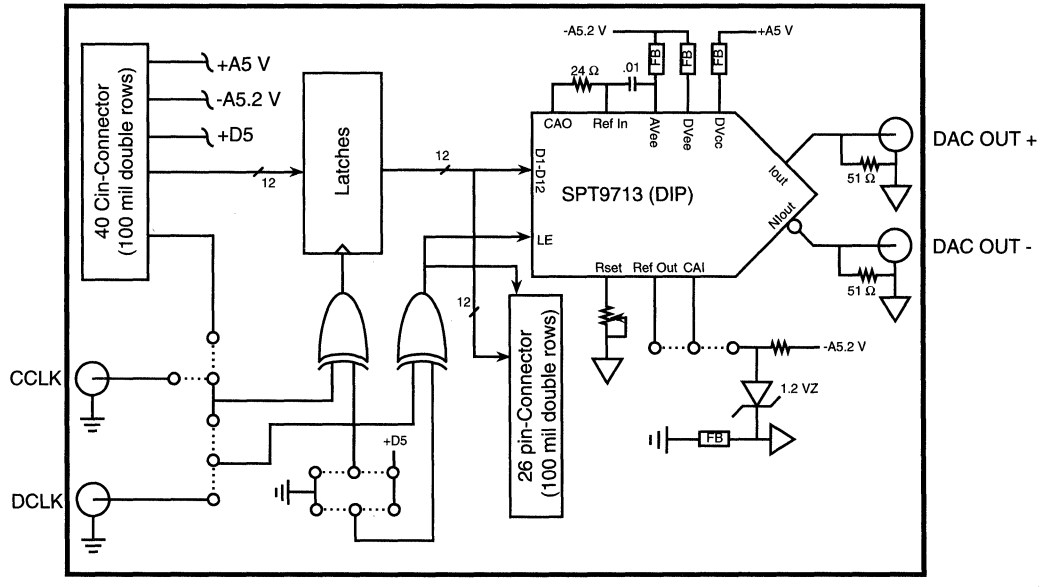
APPLICATIONS

- Evaluation of SPT9713
- Engineering System Prototype Aid
- Guide to Design of SPT9713 Interface Circuitry
- Guide for Design of SPT9713 PCB Layout
- Reconstruction DAC for other SPT, ADC Devices-TTL

GENERAL DESCRIPTION

The EB9713 is intended to be used as a tool for evaluation and characterization of the SPT9713, 12-bit 100 MWPS DAC. This application note is a supplement to the data sheet, including more detailed technical information of the interfacing circuits required. The evaluation board is designed to cover a wide variety of applications, but can also be greatly simplified to suit a specific application. Contact the SPT Applications Engineering department if assistance is needed.

BLOCK DIAGRAM



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LEADERSHIP IN DATA CONVERSION AND SIGNAL PROCESSING

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SPT
SIGNAL PROCESSING TECHNOLOGIES

APPLICATION NOTES & BRIEFS

CONTACT SPT FOR COMPLETE COPIES OF THE FOLLOWING APPLICATION NOTES.

AN1175
EB1175 EVALUATION BOARD

The EB1175 evaluation board is used to demonstrate the performance of the SPT1175, 8-bit, 30 MSPS A/D converter. Features include 30 MSPS conversion rate, on-board reference driver circuits, and a reconstruction DAC. Detailed discussions on grounding, references, timing, and product characterization are included. The board is shipped calibrated and tested. The ADC device is not included with the board.

AN5220
EB5220 EVALUATION BOARD

The EB5220 evaluation board is used to demonstrate the performance of the SPT5220, 10-bit 80 MWPS video D/A converter. Features include on-board reference circuit, digital input connector, on-board pull-up resistors, manual format and video controls and conversion rates up to 80 MSPS. It includes discussions of power supplies, grounding, video controls, timing. It also includes discussions on design of PC board layout.

AN7610
EB7610 EVALUATION BOARD

The EB7610 evaluation board is used to demonstrate the performance of the SPT7610, 6-bit 1 GSPS A/D converter. Features include on-board reference driver, differential clock input, selectable data output decimation for divide by 16/32/64/128, programmable clock delay line, on-board reconstruction DAC and conversion sampling rates up to 1 GSPS. It includes detailed discussions of power supplies, grounding, voltage references, clock driver, timing and product characterization. Board calibration and dynamic testing are explained in detail. It also includes discussions on design of PC board layout.

AN7710/25
EB7710/25 EVALUATION BOARD

The EB7710/25 evaluation board is used to demonstrate the performance of the SPT7710 and SPT7725, 8-bit 150 and 300 MSPS A/D converters. Features include 150 and 300 MSPS conversion rates, on-board reference driver circuits, and a reconstruction DAC. Detailed discussions on timing and product characterization are included. The board is shipped calibrated and tested. The ADC device is not included with the board.

AN7750/55/60
EB7750/55/60 EVALUATION BOARD

The EB7750/55/60 evaluation board is used to demonstrate the performance of the SPT7750, SPT7755, and SPT7760 8-bit A/D converters. Features include 500, 750, and 1,000 MSPS conversion rates, on-board reference driver circuits, timing circuits and two latches to capture each of the demuxed outputs. Discussions on timing and product characterization are included along with high performance PC board design and layout guidelines.

AN7810/24
EB7810/24 EVALUATION BOARD

The EB7810/24 evaluation board is used to demonstrate the performance of the SPT7810 and the SPT7814. Features include reference inputs, clock driver circuit, on-board reconstruction DAC, data output and strobe signals for ECL and TTL, user-selectable capture clock, and conversion rates up to 40 MSPS. It includes detailed discussions of power supplies, grounding, voltage references, clock driver, output data latches, timing, DAC reconstruction, selection of signal generators, and product characterization. Board calibration, accuracy testing and dynamic testing are explained in detail. The board can be used for system prototypes, incoming inspection, testing of IL and DL, AC accuracy testing, and power supply sensitivity testing. The board is calibrated and tested before shipment. The ADC device is not included with the board.

AN7820/24
EB7820/24 EVALUATION BOARD

The EB7820/24 evaluation board is used to demonstrate the performance of the SPT7820 and the SPT7824. Features include reference inputs, clock driver circuit, on-board reconstruction DAC, data output and strobe signals for ECL and TTL, user-selectable capture clock, and conversion rates up to 40 MSPS. It includes detailed discussions of power supplies, grounding, voltage references, clock driver, output data latches, timing, DAC reconstruction, selection of signal generators, and product characterization. Board calibration, accuracy testing and dynamic testing are explained in detail. The board can be used for system prototypes, incoming inspection, testing of IL and DL, AC accuracy testing, and power supply sensitivity testing. The board is calibrated and tested before shipment. The ADC device is not included with the board.

AN7830
EB7830 EVALUATION BOARD

The EB7830 evaluation board is used to demonstrate the performance of the SPT7830, 10-bit 2.5 MSPS Serial A/D converter. Features include on-board reference driver, clock driver, analog input driver/level shifter, serial to parallel converter, 3 V and 5V logic digital output and conversion sampling rates up to 2.5 MSPS. It includes detailed discussions of power supplies, grounding, voltage references, clock driver, timing and product characterization. It also includes discussions on design of PC board layout.

AN7835/40/50/55/60
EB7835/40/50/55/60 EVALUATION BOARD

The EB7835/40/50/55/60 evaluation board is used to demonstrate the performance of the SPT7835, SPT7840, SPT7850, SPT7855 and SPT7860, 10-bit ADCs. Features include 5, 10, 20, 25, and 40 MSPS conversion rates, on-board reference driver circuits, and a reconstruction DAC. Detailed discussions on grounding, references, timing, and product characterization are included. The board is shipped calibrated and tested. The ADC device is not included with the board.

AN7870
EB7870 EVALUATION BOARD

The EB7870 evaluation board is used to demonstrate the performance of the SPT7870, 10-bit 100 MSPS A/D converter. Features include on-board reference driver, differential clock input, on-board output buffers and conversion sampling rates up to 100 MSPS. It includes detailed discussions of power supplies, grounding, voltage references, clock driver, timing and product characterization. Board calibration and dynamic testing are explained in detail. It also includes discussions on design of PC board layout.

AN7910/12
EB7910/12 EVALUATION BOARD

The EB7910/12 evaluation board is used to demonstrate the performance of the SPT7910 and the SPT7912. Features include on-board reference drivers, on-board reconstruction DAC, data output and strobe signals for ECL and TTL, user selectable capture clock, and conversion rates up to 30 MSPS. It includes detailed discussions of power supplies, grounding, voltage references, clock driver, output data latches, timing, DAC reconstruction, selection of signal generators, and product characterization. Board calibration, accuracy testing and dynamic testing are explained in detail. The board can be used for system prototypes, incoming inspection, testing of IL and DL, AC accuracy testing, power supply sensitivity testing and as a guide for system layout. The board is calibrated and tested before shipment. The ADC device is not included with the board.

AN7920/22
EB7920/22 EVALUATION BOARD

The EB7920/22 evaluation board is used to demonstrate the performance of the SPT7920 and the SPT7922. Features include on-board reference drivers, on-board reconstruction DAC, data output and strobe signals for ECL and TTL, user selectable capture clock, and conversion rates up to 30 MSPS. It includes detailed discussions of power supplies, grounding, voltage references, clock driver, output data latches, timing, DAC reconstruction, selection of signal generators, and product characterization. Board calibration, accuracy testing and dynamic testing are explained in detail. The board can be used for system prototypes, incoming inspection, testing of IL and DL, AC accuracy testing, power supply sensitivity testing and as a guide for system layout. The board is calibrated and tested before shipment. The ADC device is not included with the board.

AN9101
EB9101 EVALUATION BOARD

The EB9101 evaluation board is used to demonstrate the performance of the SPT9101, 125 MSPS sampling amplifier. Features include on-board differential clock input driver and conversion sampling rates up to 125 MSPS. It includes detailed discussions of power supplies, grounding, clock driver, timing and product characterization. It also includes discussions on design of PC board layout.

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AN9712
EB9712 EVALUATION BOARD

The EB9712 evaluation board is used to demonstrate the performance of the SPT9712, 12-bit 100 MWPS D/A converter (ECL input). Features include on-board reference circuit, ECL digital input connector, on-board latches and conversion rates up to 100 MSPS. It includes detailed discussions of power supplies, grounding, timing and product characterization. It also includes discussions on design of PC board layout.

AN9713
EB9713 EVALUATION BOARD

The EB9713 evaluation board is used to demonstrate the performance of the SPT9713, 12-bit 100 MWPS D/A converter (TTL input). Features include on-board reference circuit, TTL digital input connector, on-board latches and conversion rates up to 100 MSPS. It includes detailed discussions of power supplies, grounding, timing and product characterization. It also includes discussions on design of PC board layout.

AN104
VIDEO DACS AND RASTER GRAPHICS

AN104 explains high-speed DACs and how they are used in CRT designs and raster graphics systems. This application note describes video DAC performance parameters including speed, rise time, glitch energy, resolution, logic compatibility, and analog output drive. A block diagram and associated graphs are included to clearly illustrate raster scan graphics systems.

AN106
EB104 EVALUATION BOARD

The EB104 is used to demonstrate performance of the HADC574Z/674Z, and SPT774 12-bit ADC products. The low noise environment provided by the board makes 12-bit resolution easier to achieve compared to most lab breadboarding. Features include buffered A/D and D/A conversion data buses, S/H amp and output op-amp ICs, and unipolar or bipolar operation. It is shipped fully assembled and tested.

AN108
THERMAL CONSIDERATIONS FOR HIGH-PERFORMANCE DEVICES

AN108 is a general overview of the integrated circuit package and its interface to the outside world. Information on system thermodynamics, calculating the operating die temperature, package thermal resistance, and heat sinking is included. Thermal resistances of concern to system designers are also discussed.

AB100
USING ECL DACS WITH TTL LOGIC

This application brief describes why most high-speed DACs are designed to perform in ECL systems due to the speed and low noise characteristics of this logic group. It gives specific information on methods for using SPT's ECL DACs in TTL systems. Solutions for overcoming incompatibility between -5.2 V and +5 V systems are included.

AB102
CHARGE SCALING DATA CONVERTERS

Current scaling versus charge scaling data conversion techniques are discussed in this application note. SPT's BiCMOS process used to manufacture the HADC574Z, HADC674Z, and SPT774 uses this technique to lower power consumption and provide an inherent S/H function. A simple explanation of how this is performed is included.

AB103
HADC574Z/674Z AND SPT774 ANALOG INPUT STRUCTURE

This application brief describes the BiCMOS process and design architecture of the input circuits of the HADC574Z/674Z and the SPT774 and how the architecture reduces the need for specific signal source characteristics and signal buffering. Included is a brief discussion of conversion events and DC dynamic input characteristics of the device and how the input structure improves the overall performance of the ADC.

AB104
TESTING THE HADC574Z/674Z AND THE SPT774 ON THE LTS2020

This application brief provides technical information on the LTS2020 test system commonly used as an incoming inspection tool. Hardware and software modifications to achieve accurate test results for the HADC574Z/674Z and SPT774 are explained.

AB105
GLITCH ENERGY IN HIGH-SPEED D/A CONVERTERS

This brief provides a brief explanation of how glitch energy affects some applications, how to overcome these problems, and why SPT's devices have superior glitch performance. Included is specific information on SPT's DAC designs and information on defining glitch energy.

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SPT
SIGNAL PROCESSING TECHNOLOGIES

QUALITY ASSURANCE

INTRODUCTION

Signal Processing Technologies, Inc. (SPT), is a manufacturer of high performance integrated circuits. As detailed by the manufacturing flow charts in the subsequent pages, the products of SPT are developed and tested through precise and defined processes.

SPT is registered through the British Standards Institution (BSI) for the assessment and audit process of its quality management system to the requirements of ISO9000 series of standards. *The assessment process was performed and SPT received its certification to ISO9001 as of February 1995.* The ISO9001 certification is a model for quality assurance at a system level for design/development, production, installation and servicing.

MANUFACTURING AND TEST PROCESSES

After manufacturing of the wafers, they are processed through the inspection and wafer probe functions. Upon completion of the assembly process, the packaged product undergoes a complete electrical test evaluation and marking. Once the production phase of electrical testing has been completed, the products are processed through Quality Conformance Inspection (QCI).

Military products (Hi-Rel and Class B) are initially processed through a complete qualification process of MIL-I-38535 utilizing MIL-STD-883, Method 5004 and 5005, Groups A, B, C, and D. A product qualification report is developed for each device type for internal reference and customer use. Once the initial Class B product qualification is complete, the product is released to production. At this point, periodic Quality Conformance Inspections (QCI) are performed on each production lot utilizing the requirements of MIL-STD-883, Method 5005. (Refer to Military Product Flow section for the differences between Hi-Rel and Class B products.)

The Quality Assurance department performs periodic audits of all SPT subcontracted vendors. To verify internal compliance, SPT also performs periodic audits of its own internal processes. Through these evaluations, SPT controls and assures the quality of products manufactured for its customers.

Through the Class B qualification process, SPT has received qualification for specific products on the Defense Electronics Supply Center (DESC) Standardized Military Drawings (SMD) list. Specific products have been qualified to guidelines established by MIL-STD-883, Method 5004 and 5005. In the future, SPT plans to add additional products to this list as they become available.

Customers are notified prior to implementation of any major change of product or product assurance program that may affect performance, quality, reliability, or interchangeability in accordance with MIL-I-38535, DESC and all applicable Class B requirements.

SPT was audited by DESC to verify compliance of its self-certification program for its SMD/MIL-STD-883 products. All DESC audit corrective action items, completed by SPT, have been reviewed and accepted by DESC. Through the completion of this audit process, SPT is considered to be compliant to the requirements of SMD and MIL-STD-883 guidelines by DESC.

QUALITY OBJECTIVE, POLICY, AND CONTROL SYSTEM

CORPORATE OBJECTIVE

SPT's commitment to quality is implicit in its corporate objective which is:

> "To provide products of the highest quality and greatest possible value to its customers, thereby gaining and maintaining their respect and loyalty."

QUALITY PHILOSOPHY

SPT defines quality as a set of product or process attributes that provide a value to customers that meet or exceed their expectations.

Three fundamental beliefs form the basis for SPT's quality philosophy, the strategic management and operation of a quality system:

1. Quality is paramount - All departments within SPT must keep quality of product as their number one objective.
2. Quality is dynamic - Customers define quality. Where customers expectations change, SPT must respond quickly with innovative products and services.
3. Quality is pervasive - Quality applies to every aspect of a business relationship, not just product development and manufacturing. Moreover, quality is the responsibility of all individuals, not just select teams.

QUALITY OBJECTIVE

SPT's overall quality objective is to institutionalize Total Quality Control (TQC) throughout the company, thereby ensuring customer satisfaction. TQC is a management philosophy and operating methodology that results in continuous innovation in meeting customer needs. Attention to this objective contributes to increased profitability through the reduction of avoidable costs while meeting or exceeding customer expectations.

QUALITY POLICY

The SPT organization quality policy is to effectively implement a quality system that achieves the quality objective mentioned above. As the Management Representative of the Quality System, the Quality Assurance manager establishes the Quality System, and ensures that the established requirements are implemented and maintained. Proper procedures are established for internal and external quality audits to ensure the fulfillment of this system. The results of the audit are reported to the top management at SPT, and corrective/prevention actions are taken by appropriate departments. The Quality Assurance manager sets annual goals for quality improvement. The activities with respect to the quality improvement goals are deployed into all management aspects in the quality system. The Quality Assurance manager takes responsibility for in-process quality control and outgoing quality of products and reports quality trends to the relevant departments.

TOTAL QUALITY CONTROL SYSTEM (TQCS)

The quality system at SPT is composed of various levels of documentation including quality policy, information on the many processes utilized, and key work instructions necessary to complete assigned tasks. The aggregate combination of quality documentation, policy, responsibilities, processes, work instructions, technical manuals, and procedures form our documented Total Quality Control Systems (TQCS). Adherence to this documented quality system is the means by which SPT strives to meet its quality objective. SPT places emphasis on five aspects of quality management:

1. Customer focus - essential to understand our customers needs and levels of satisfaction.
2. Planning - a vital element of our business that must clearly define the strategies, direction and goals for the organization to be successful.
3. Process Management - recognizing that products are delivered through processes. The quality of these processes are monitored, improved and managed to ensure that customer needs and expectations are met.
4. Process Improvement - emphasizing continuous innovation and improvement of products and processes to meet changing customer needs.
5. Total Participation - recognizing that the commitment and direction for quality improvement is achieved through the involvement of employees and management sharing ideas, successes and contribution.

TOTAL QUALITY MANAGEMENT SYSTEM (TQMS)

TQMS is defined as total management understanding, involvement, and support for the implementation of a sound and practical quality system applicable to SPT's day-to-day operations.

Practically, this system is practiced through comprehensive management training sessions held by the Quality Assurance/Reliability Engineering department and/or by commercial agencies found suitable for this purpose. The internal training conducted by the Quality Assurance/Reliability Engineering department covers:

- SPT Quality Assurance Manual - its purpose and its implications throughout SPT's operations.
- SPT General Quality Specifications (GQS) - contents and specified responsibilities for each group or department.
- SPT work instructions which procedurally define the day-to-day operations for applicable operators.
- SPT forms and technical documents pertinent to the equipment in use.

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RESPONSIBILITIES OF THE QUALITY ASSURANCE DEPARTMENT

PURPOSE

The purpose of the Quality Assurance department and program is to assist in maintaining a high level of quality products manufactured by SPT. This quality can only be created and controlled at the point of manufacture. Inspection alone will never accomplish this task. This goal is achieved through efforts involving all phases of the company: management, engineering, technical staff, administrators, operators, and support staff. The Quality Assurance program prescribes the steps to be followed to maintain this quality and the means of Quality Conformance Inspection and record keeping to monitor performance and prevention plans.

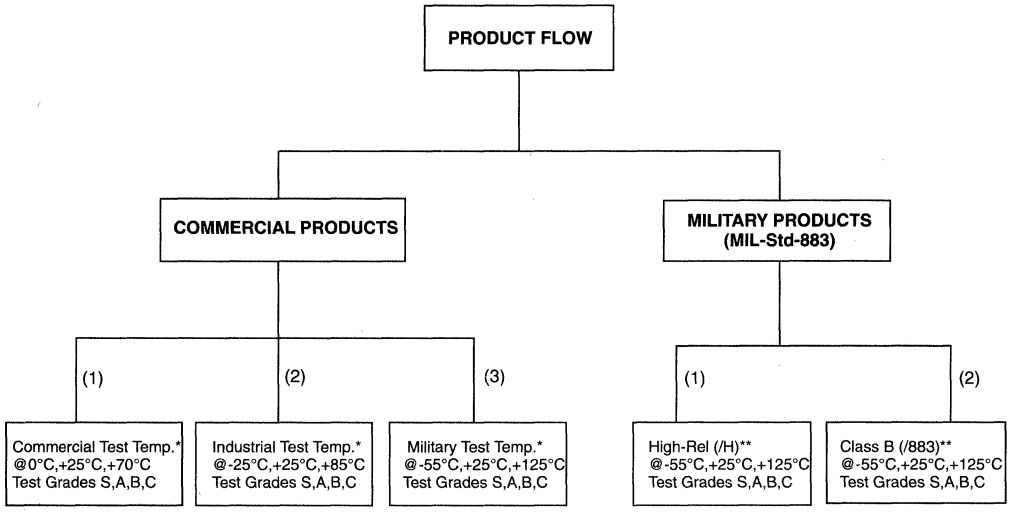
SCOPE OF RESPONSIBILITY

The Quality Assurance/Reliability Engineering department's responsibility is to assure the quality of product produced by manufacturing or engineering which will ultimately be delivered to customers, extending throughout procurement, manufacturing, packaging, testing, and shipping processes. Therefore, the Quality Assurance/Reliability Engineering department is SPT's customer representative for assuring and guaranteeing quality and long-term reliability of SPT products shipped to customers.

QUALITY ASSURANCE PROGRAM

This program is designed to manufacture quality products. In doing so, the program complies with the following specifications: MIL-I-45208, MIL-Q-9858, MIL-STD-45662, MIL-STD-883, and MIL-I-38535. An up-to-date copy of each specification is maintained in the SPT Document Control department, managed by the Quality Assurance department. Other related reference documents are also maintained within this department. Additionally, SPT operations are in compliance with General Quality Specification for Manufacturing Configuration that defines the General Quality Specifications by which SPT governs itself with regard to compliance to customer technical specifications.

PRODUCT FLOW DESCRIPTION



* The only difference between Commercial, Industrial, and Military is the Test temperature, although all three are considered commercial products.

** Differences between:	/H	and /883
1) Mil-I-38535 Certified wafer FAB required.	No	Yes
2) Lot traceability required	Yes	Yes
3) PDA Calculation required	Yes	Yes
4) Off-shore assembly permitted	Yes	Yes
5) Method 5004, Class B screening procedures	Yes	Yes
6) Method 5005, Class B initial product Qual. group A, B, C, & D required	Yes(1)	Yes
7) QCI Visual & Group A on every inspection lot required	Yes	Yes
8) QCI group B per Mil-Std-883	No	Yes
9) QCI group C per Mil-Std-883	No	Yes
10) QCI group D per Mil-Std-883	No	Yes
11) Certificate of Compliance w/every lot shipment required	Yes	Yes

(1) This process is required for /H but product may be shipped to customers prior to completeion of qualification process.

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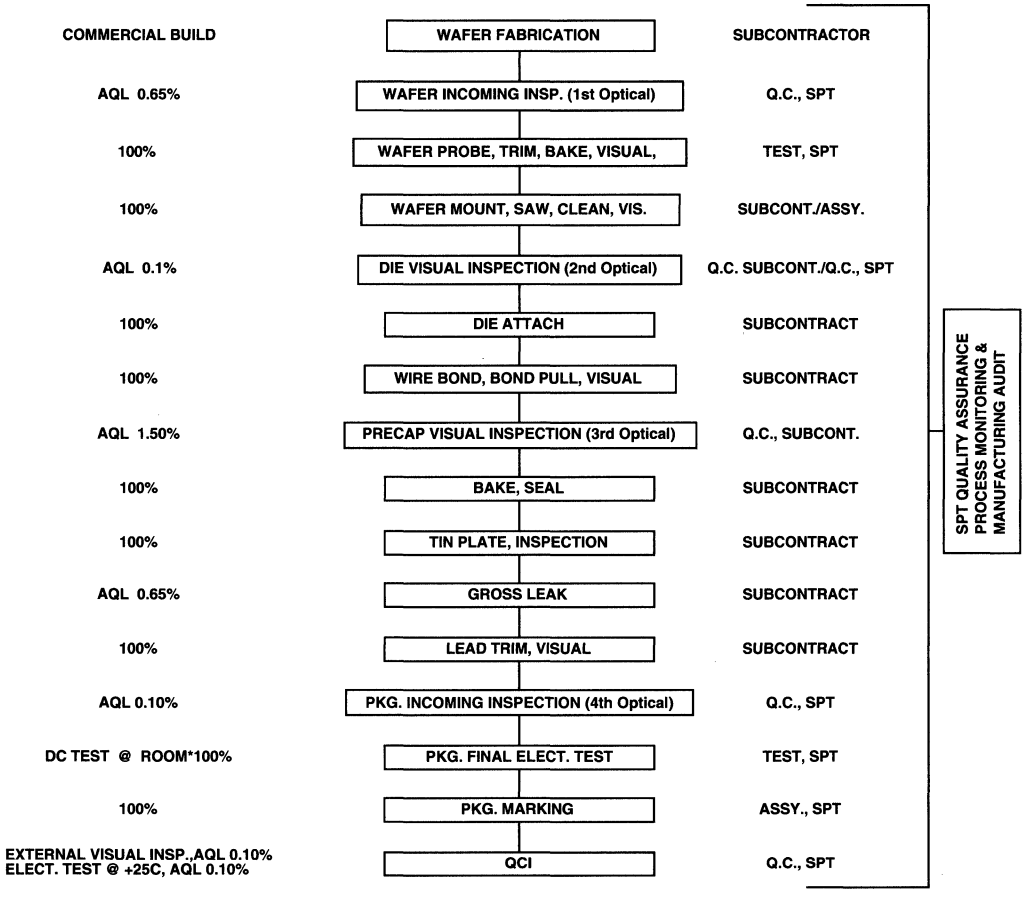
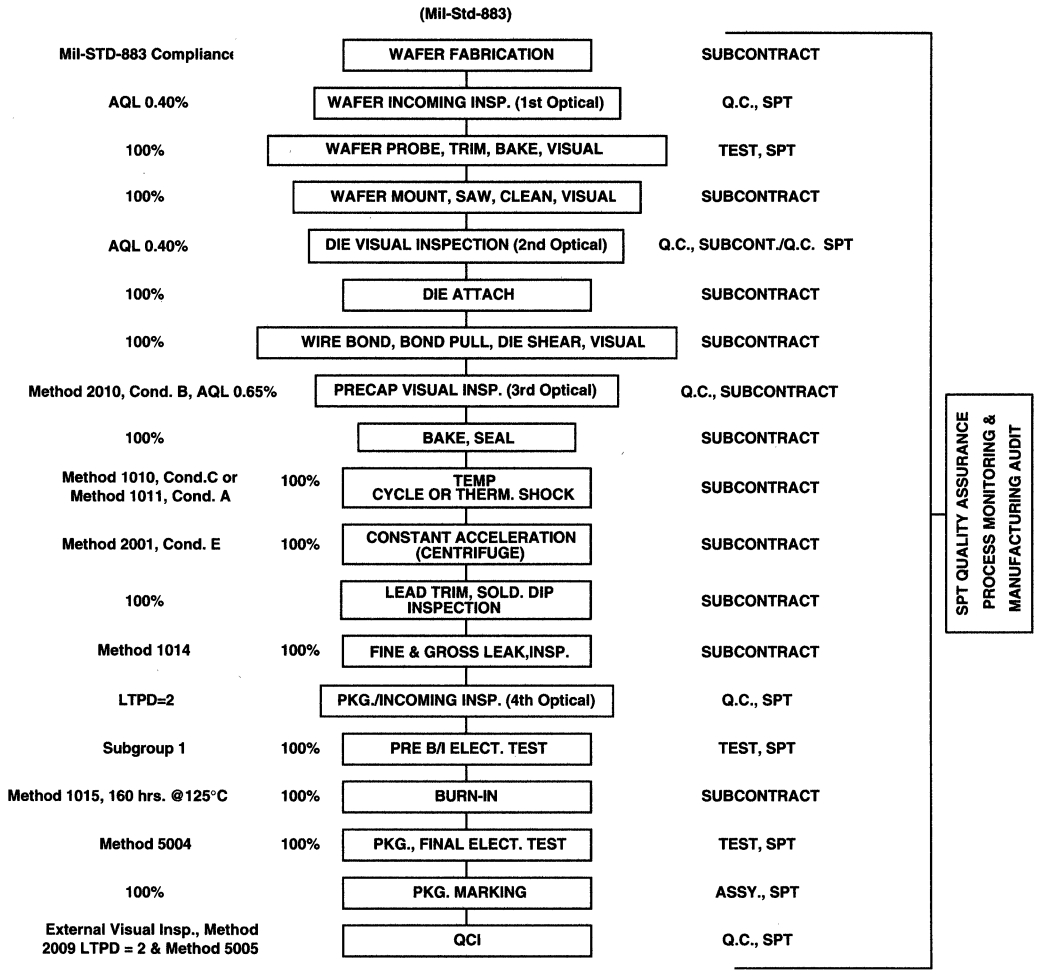
COMMERCIAL PRODUCT FLOW (1)



(1) INCLUDES COMMERCIAL, INDUSTRIAL & MILITARY TEST TEMPERATURE. THIS STANDARD FLOW IS SUBJECT TO CHANGE DUE TO PRODUCT SPECIFIC FLOW.

* HOT AND/OR COLD TEST TEMPERATURES AND AC TEST ARE PERFORMED ONLY WHEN REQUIRED.

MILITARY PRODUCT FLOW (1)



(1) INCLUDES HIGH-REL (/H) AND CLASS "B" (/883) PRODUCTS.

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Package Outlines

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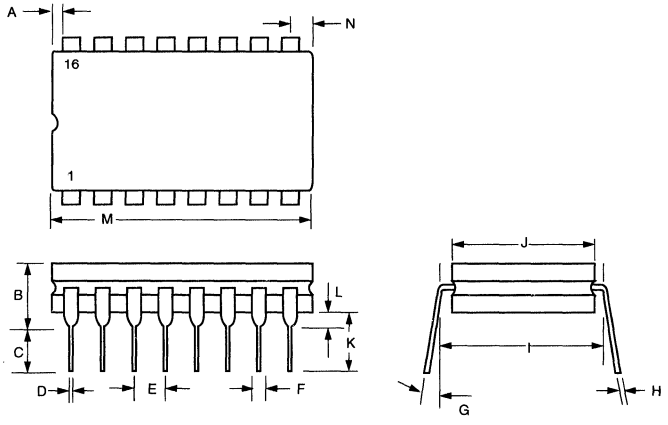
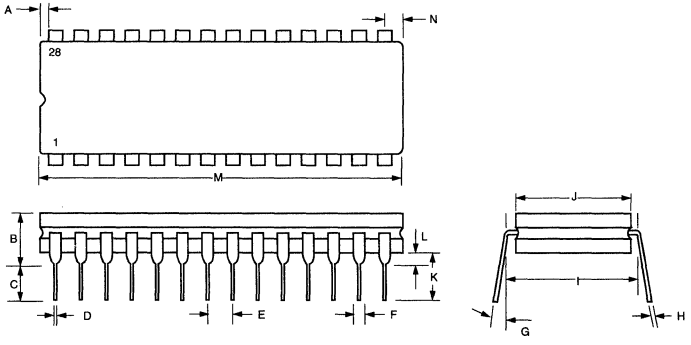
16-LEAD CERDIP (C/D)



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.005		0.13	
B		0.200		5.08
C	0.125	0.150	3.18	3.81
D	0.015	0.023	0.38	0.58
E	0.090	0.110	2.29	2.79
F	0.030	0.065	0.76	1.65
G	0°	15°	0°	15°
H	0.008	0.015	0.20	0.38
I	0.290	0.320	7.37	8.13
J	0.250	0.310	6.35	7.87
K	0.140	0.200	3.56	5.08
L	0.015	0.050	0.38	1.27
M	0.745	0.785	18.92	19.94
N	0.015	0.050	0.38	1.27

28-LEAD CERDIP (C/D)



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.005		0.13	
B	0.205	0.235	5.21	5.97
C	0.120	0.200	3.05	5.08
D	0.016	0.020	0.41	0.51
E	0.090	0.110	2.29	2.79
F	0.045	0.065	1.14	1.65
G	0°	15°	0°	15°
H	0.009	0.011	0.23	0.28
I	0.590	0.610	14.99	15.49
J	0.500	0.550	12.70	13.97
K	0.160	0.260	4.06	6.60
L	0.040	0.060	1.02	1.52
M	1.430	1.490	36.32	37.85
N	0.060	0.100	1.52	2.54

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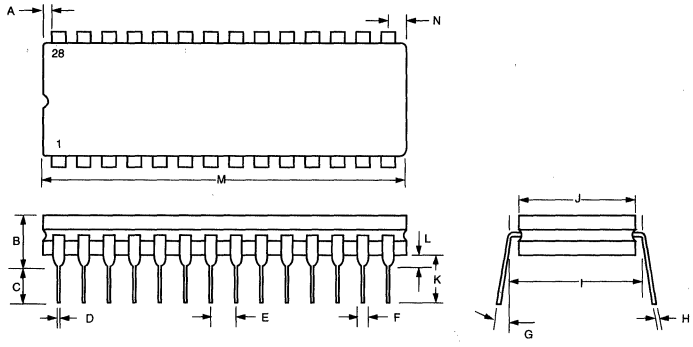
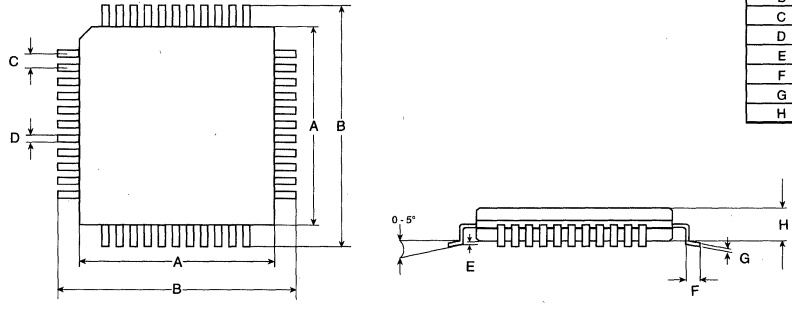
28-LEAD SKINNY (300 MIL) CERDIP (C/D)



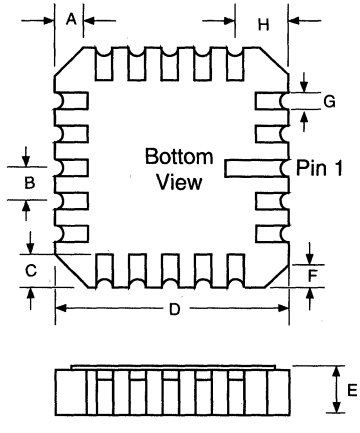
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.005		0.13	
B		0.200		5.08
C	0.125	0.200	3.18	5.08
D		0.018		0.46
E		0.100		2.54
F		0.056		1.42
G	0°	15°	0°	15°
H		0.010		0.25
I	0.311	0.317	7.90	8.05
J	0.285	0.291	7.24	7.39
K	0.150		3.81	
L	0.015	0.060	0.38	1.52
M	1.440	1.460	36.58	37.08
N		0.098		2.49

44-LEAD CERQUAD (C/Q)



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.546 Typ	0.000	14.00 Typ	
B	0.679	0.694	17.40	17.80
C	0.038	0.040	0.98	1.02
D	0.016 Typ	0.000	0.40 Typ	
E	0.008 Typ	0.000	0.20 Typ	
F	0.027	0.051	0.70	1.30
G	0.006 Typ	0.000	0.15 Typ	
H	0.115	0.140	2.96	3.58

20-CONTACT LEADLESS CHIP CARRIER (LCC)



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A		.040 typ		1.02
B		.050 typ		1.27
C	0.045	0.055	1.14	1.40
D	0.345	0.360	8.76	9.14
E	0.054	0.066	1.37	1.68
F		.020 typ		0.51
G	0.022	0.028	0.56	0.71
H		0.075		1.91

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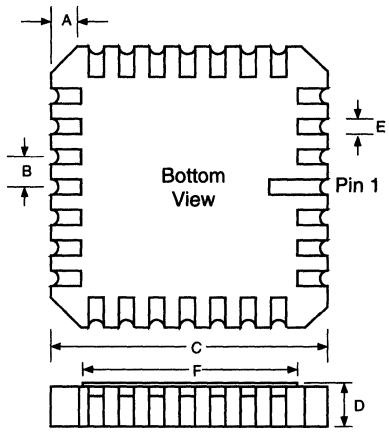
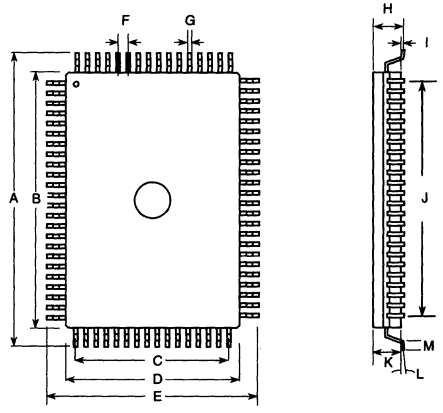
28-CONTACT LEADLESS CHIP CARRIER (LCC)



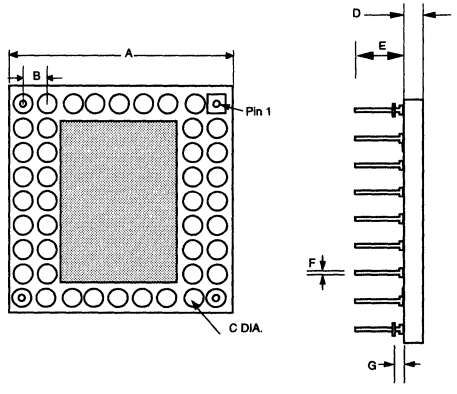
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A		.040 x 45°		
B		0.050		1.27
C	0.442	0.458	11.23	11.63
D	0.060	0.070	1.52	1.78
E	0.022	0.028	0.56	0.71
F	0.396	0.412	10.06	10.46

80-LEAD MQUAD



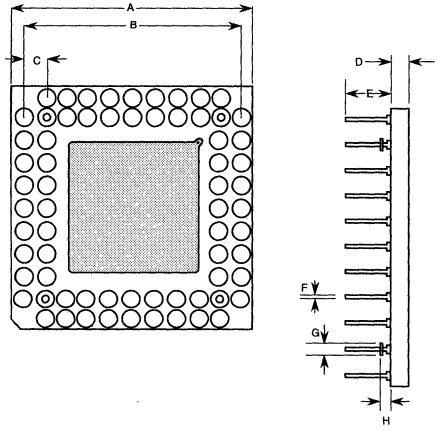
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.937	0.945	23.80	24.00
B	0.777	0.785	19.72	19.93
C	0.472 TYP		12.0 TYP	
D	0.541	0.549	13.73	13.94
E	0.701	0.709	17.80	18.00
F	0.032 TYP		0.80 TYP	
G	0.014 TYP		0.36 TYP	
H	0.114	0.122	2.90	3.10
I	.006 TYP		0.15 TYP	
J	0.724 TYP		18.4 TYP	
K	0.099	0.109	2.51	2.77
L	7°		7°	
M	0.026	0.036	0.66	0.91

46-PIN GRID ARRAY (PGA)



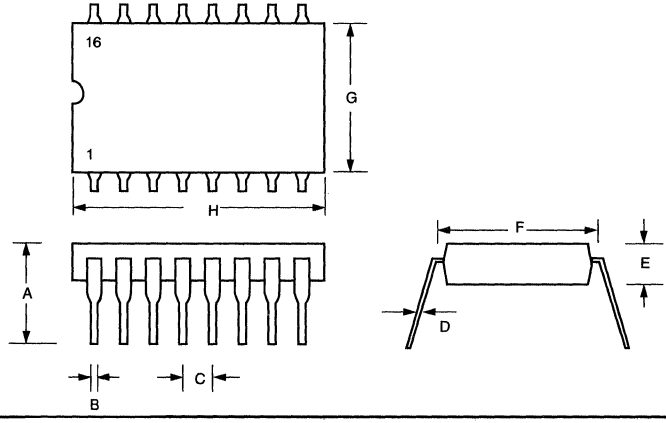
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.890	0.910	22.61	23.11
B		0.100 typ		2.54 typ
C	.045 dia	.055 dia	1.14	1.40
D	0.084	0.096	2.13	2.44
E	0.169	0.193	4.29	4.90
F	.020 dia	.030 dia	0.51	0.76
G		.050 typ		1.27 typ

68-PIN GRID ARRAY (PGA)



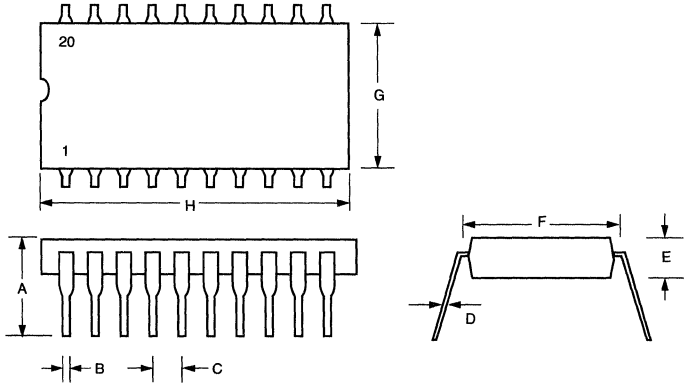
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.089	1.111	27.66	28.22
B	1.090	1.110	27.69	28.19
C		.100 typ		2.54
D	0.067	0.083	1.70	2.11
E	0.150	0.170	3.81	4.32
F	.016 dia	0.02 dia	0.41	0.51
G		.050 dia		1.27
H		0.050		1.27

16-LEAD PLASTIC DIP (PDIP)



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A		0.300		7.62
B	0.014	0.026	0.36	0.66
C		.100 typ		2.54
D		.010 typ		0.25
E	1.150	1.950	29.21	49.53
F	0.290	0.330	7.37	8.38
G	0.246	0.254	6.25	6.45
H	0.740	0.760	18.80	19.30

20-LEAD PLASTIC DIP (PDIP)



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A		0.300		7.62
B	0.014	0.026	0.36	0.66
C		.100 typ		2.54
D		.010 typ		0.25
E		1.20 typ		30.48
F	0.290	0.330	7.37	8.38
G	0.246	0.254	6.25	6.45
H	1.010	1.030	25.65	26.16

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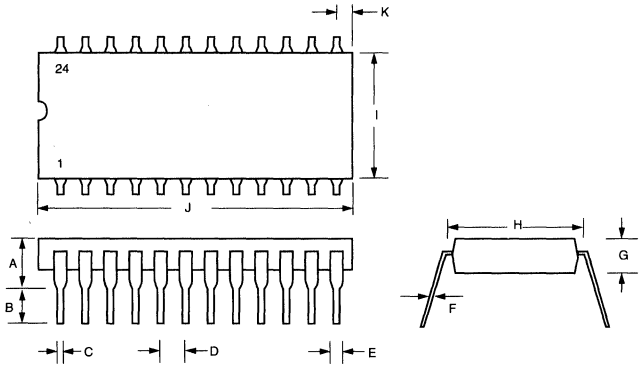
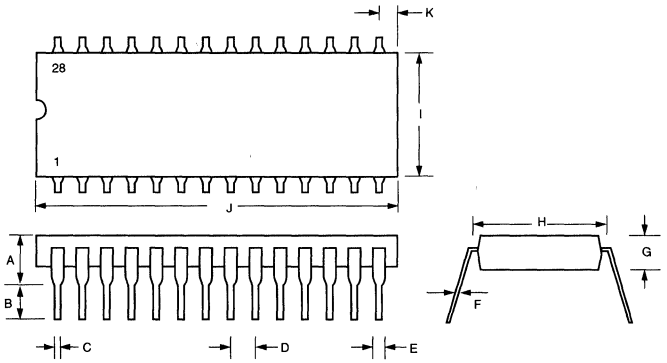
24-LEAD PLASTIC DIP (PDIP)



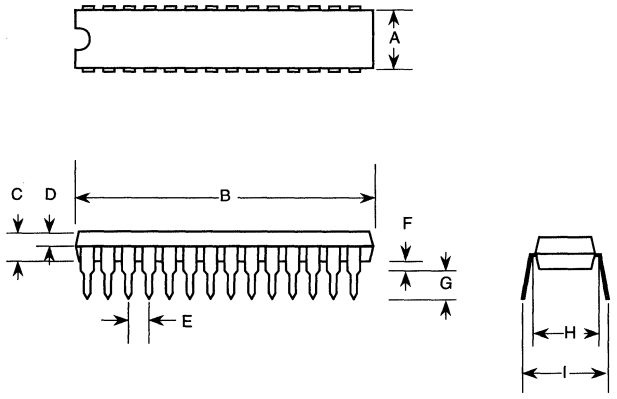
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A		0.190		4.83
B	0.125	0.135	3.18	3.43
C	0.015	0.022	0.38	0.56
D	0.100 typ		25.4 typ	
E	0.055	0.065	1.40	1.65
F	0.008	0.012	0.20	0.30
G	0.150 typ		3.81 typ	
H	0.600	0.625	15.24	15.88
I	0.530	0.550	13.46	13.97
J	1.245	1.255	31.62	31.88
K	0.070	0.080	1.78	2.03

28-LEAD PLASTIC DIP (PDIP)



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A		0.200		5.08
B	0.120	0.135	3.05	3.43
C		0.020		0.51
D		0.100		2.54
E		0.067		1.70
F		0.013		0.33
G	0.170	0.180	4.32	4.57
H		0.622		15.80
I		0.555		14.10
J		1.460		37.08
K		0.085		2.16

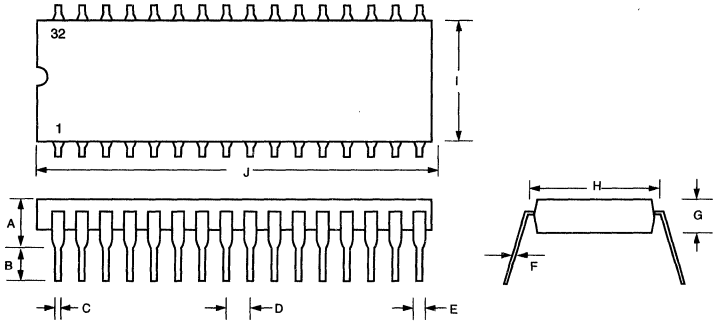
28-LEAD SKINNY (300 MIL) PLASTIC DIP (PDIP)



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.288 typ		7.3 typ	
B	1.386 typ		35.2 typ	
C	0.130 typ		3.3 typ	
D	0.060 typ		1.5 typ	
E	0.100 typ		2.5 typ	
F	0.020 typ		0.5 typ	
G	0.130 typ		3.3 typ	
H	0.310 typ		7.9 typ	
I	0.345 typ		8.8 typ	

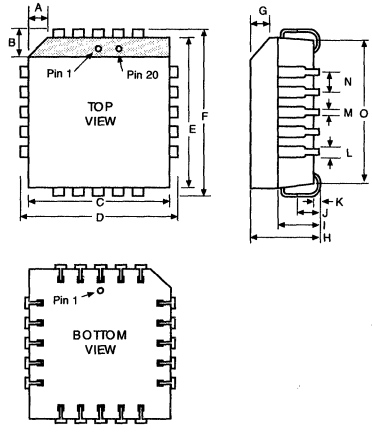
11

32-LEAD PLASTIC DIP (PDIP)



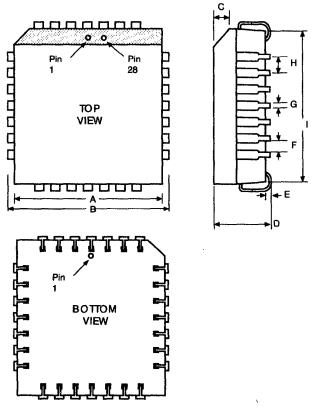
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A		0.200		5.08
B	0.128	0.131	3.25	3.33
C	0.017	0.018	0.43	0.46
D		.100 typ		2.54
E	0.059	0.060	1.50	1.52
F	0.008	0.010	0.20	0.25
G	0.149	0.150	3.78	3.81
H		.600 typ		15.24
I	0.527	0.543	13.39	13.79
J	1.640	1.660	41.66	42.16

20-LEAD PLASTIC LEADED CHIP CARRIER (PLCC)



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A		.045 typ		1.14
B				
C	0.350	0.356	8.89	9.04
D	0.385	0.395	9.78	10.03
E	0.350	0.356	8.89	9.04
F	0.385	0.395	9.78	10.03
G	0.042	0.056	1.07	1.42
H	0.165	0.180	4.19	4.57
I	0.085	0.110	2.16	2.79
J	0.025	0.040	0.64	1.02
K	0.015	0.025	0.38	0.64
L	0.026	0.032	0.66	0.81
M	0.013	0.021	0.33	0.53
N		0.050		1.27
O	0.290	0.330	7.37	8.38

28-LEAD PLASTIC LEADED CHIP CARRIER (PLCC)



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.450	0.456	11.43	11.58
B	0.485	0.495	12.32	12.57
C	45°		45°	
D	0.165	0.175	4.19	4.45
E		0.010		0.25
F	0.022 typ		.56 typ	0.00
G	0.18 typ		4.57 typ	0.00
H	0.05 typ		1.27 typ	0.00
I	0.039	0.430	0.99	10.92

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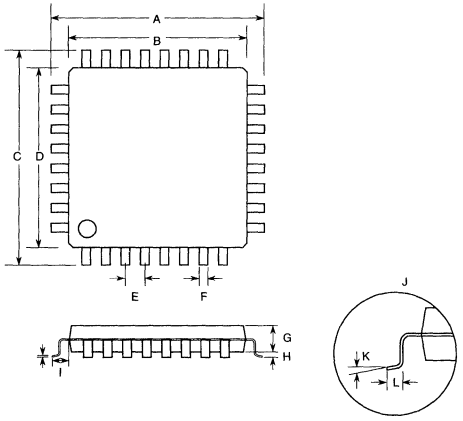
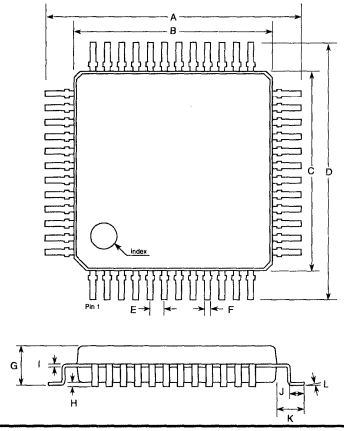
32-LEAD QUAD FLAT PACK (QFP)



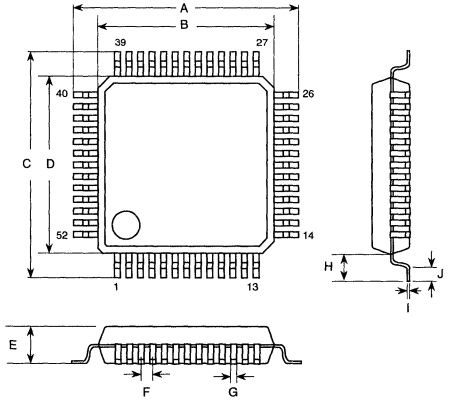
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.339	0.363	8.70	9.30
B	0.261	0.285	6.70	7.30
C	0.339	0.363	8.70	9.30
D	0.261	0.285	6.70	7.30
E	0.023	0.039	0.60	1.00
F	0.012	0.020	0.30	0.50
G	0.056	0.057	1.44	1.46
H	0.002	0.006	0.05	0.15
I	0.039 typ		1.00 typ	
J	0.004	0.008	0.09	0.20
K	0°	7°	0°	7°
L	0.016 typ		0.4 typ	

48-LEAD QUAD FLAT PACK (QFP)



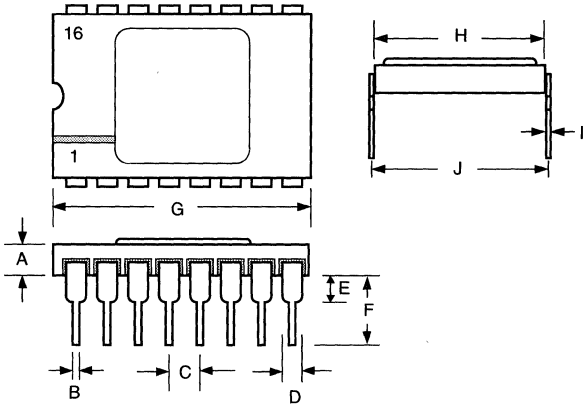
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.343	0.359	8.79	9.21
B	0.269	0.277	6.89	7.11
C	0.269	0.277	6.89	7.11
D	0.343	0.359	8.79	9.21
E	0.016	0.023	0.41	0.59
F	0.004	0.012	0.09	0.31
G	0.052	0.067	1.34	1.71
H	0.000	0.006		0.16
I	0.003	0.007	0.074	0.176
J	0.011	0.028	0.29	0.71
K	0.039 typ		1.0 typ	
L	0°	10°	0°	10°

52-LEAD QUAD FLAT PACK (QFP)



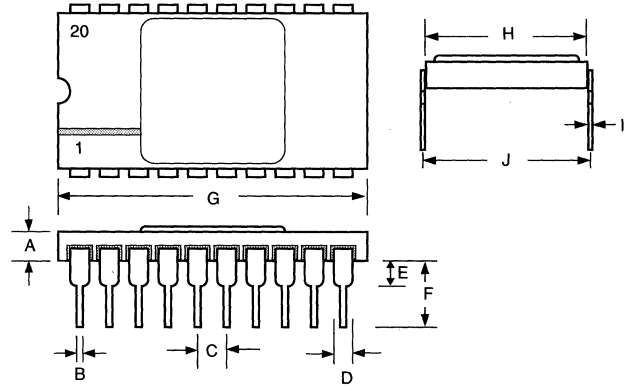
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.507	0.523	13.0	13.4
B	0.386	0.394	9.9	10.1
C	0.507	0.523	13.0	13.4
D	0.386	0.394	9.9	10.1
E	0.080	0.088	2.05	2.25
F	0.025 typ		0.65 typ	
G	0.008	0.016	0.2	0.4
H	0.062 typ		1.6 typ	
I	0.004	0.008	0.1	0.2
J	0.023	0.039	0.6	1.0

16-LEAD SIDEBRAZED (S/B)



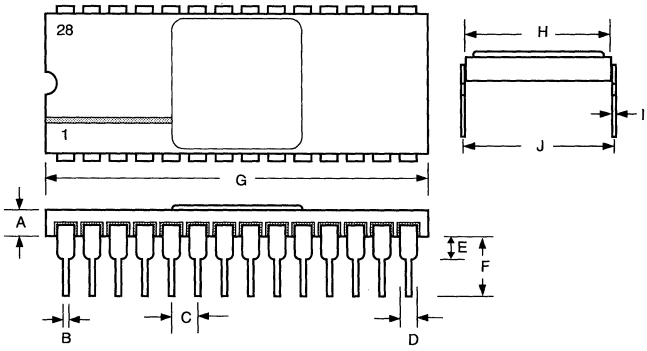
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.070	0.090	1.78	2.29
B	0.015	0.021	0.38	0.53
C	0.100 typ		2.54 typ	
D	0.049	0.059	1.24	1.50
E	—	—	—	—
F	—	—	—	—
G	0.792	0.808	20.12	20.52
H	0.287	0.303	7.29	7.70
I	0.009	0.012	0.23	0.30
J	0.290	0.310	7.37	7.87

20-LEAD SIDEBRAZED (S/B)



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.075	0.095	1.91	2.41
B	0.014	0.023	0.36	0.58
C	0.090	0.110	2.29	2.79
D	0.030	0.070	0.76	1.78
E	0.015	0.060	0.38	1.52
F	0.150		3.81	
G		1.060		26.92
H	0.220	0.310	5.59	7.87
I	0.008	0.015	0.20	0.38
J	0.290	0.320	7.37	8.13

28-LEAD SIDEBRAZED (S/B)



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.077	0.093	1.96	2.36
B	0.016	0.020	0.41	0.51
C	0.095	0.105	2.41	2.67
D		.050 typ		1.27 typ
E	0.040	0.060	1.02	1.52
F	0.215	0.235	5.46	5.97
G	1.388	1.412	35.26	35.86
H	0.585	0.605	14.86	15.37
I	0.009	0.012	0.23	0.30
J	0.600	0.620	15.24	15.75

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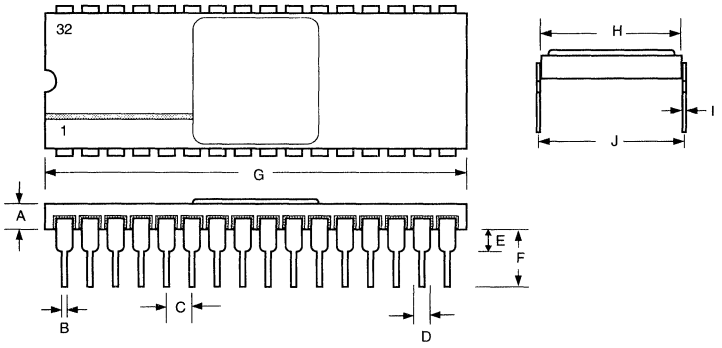
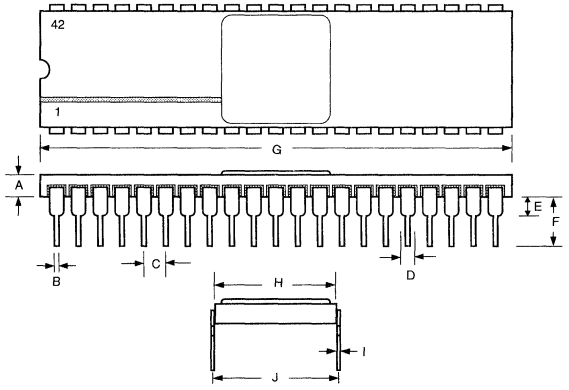
32-LEAD SIDEBRAZED (S/B)



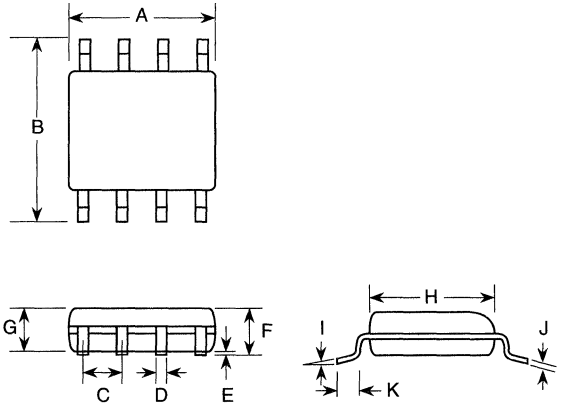
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.081	0.099	2.06	2.51
B	0.016	0.020	0.41	0.51
C	0.095	0.105	2.41	2.67
D		.050 typ		1.27
E	0.040		1.02	
F	0.175	0.225	4.45	5.72
G	1.580	1.620	40.13	41.15
H	0.585	0.605	14.86	15.37
I	0.009	0.012	0.23	0.30
J	0.600	0.620	15.24	15.75

42-LEAD SIDEBRAZED (S/B)



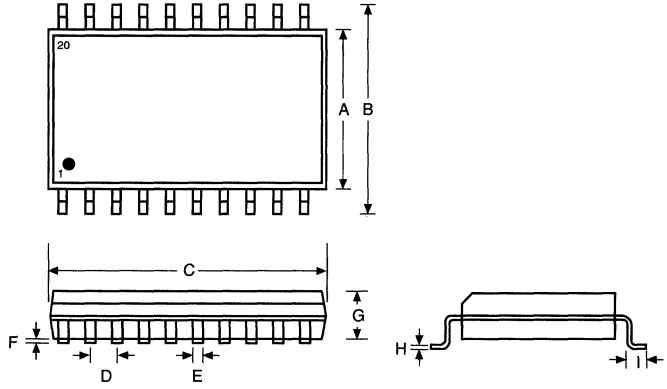
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.081	0.099	2.06	2.51
B	0.016	0.020	0.41	0.51
C	0.095	0.105	2.41	2.67
D		.050 typ		1.27
E		.050 typ		1.27
F		0.275		6.99
G	2.080	2.120	52.83	53.85
H	0.585	0.605	14.86	15.37
I	0.008	0.015	0.20	0.38
J	0.600	0.620	15.24	15.75

8-LEAD SMALL OUTLINE INTEGRATED CIRCUIT (SOIC)



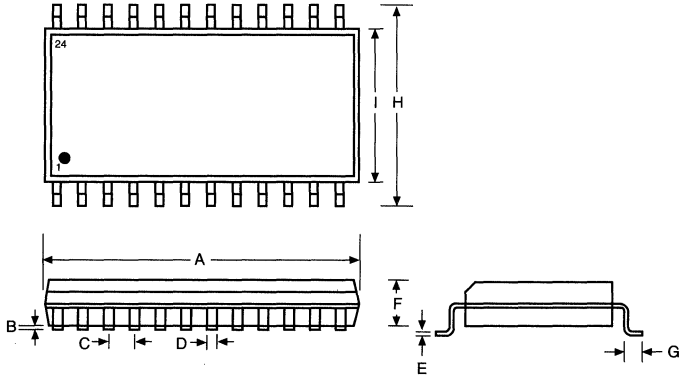
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.187	0.194	4.80	4.98
B	0.228	0.242	5.84	6.20
C	0.050 typ		1.27 typ	
D	0.014	0.019	0.35	0.49
E	0.005	0.010	0.13	0.25
F	0.060	0.067	1.55	1.73
G	0.055	0.060	1.40	1.55
H	0.149	0.156	3.81	3.99
I	0°	8°	0°	8°
J	0.007	0.010	0.19	0.25
K	0.016	0.035	0.41	0.89

20-LEAD SMALL OUTLINE INTEGRATED CIRCUIT (SOIC)



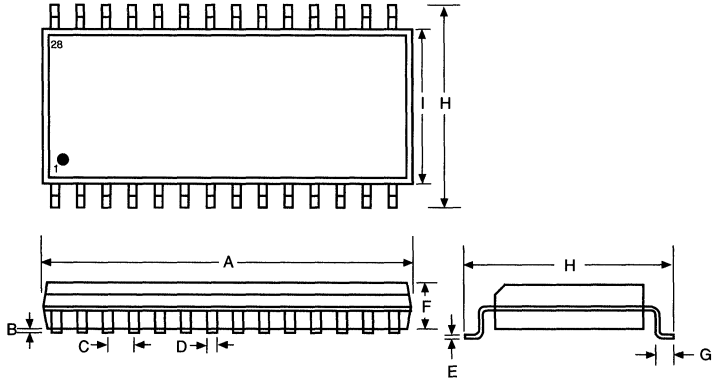
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.291	0.299	7.40	7.60
B	0.394	0.419	10.00	10.65
C	0.496	0.512	12.60	13.00
D	0.050 typ		1.27 typ	
E	0.014	0.019	0.35	0.49
F	0.004	0.012	0.10	0.30
G	0.093	0.104	2.35	2.65
H	0.009	0.013	0.23	0.32
I	0.016	0.050	0.40	1.27

24-LEAD SMALL OUTLINE INTEGRATED CIRCUIT (SOIC)



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.581	0.601	14.90	15.40
B				
C	.050 typ		1.27 typ	
D	0.014	0.021	0.35	0.55
E	0.006	0.012	0.15	0.30
F	0.066	0.088	1.70	2.25
G	0.012	0.027	0.30	0.70
H	0.293	0.324	7.50	8.30
I	0.203	0.218	5.20	5.60

28-LEAD SMALL OUTLINE INTEGRATED CIRCUIT (SOIC)



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.696	0.712	17.68	18.08
B	0.004	0.012	0.10	0.30
C		.050 typ	0.00	1.27
D	0.014	0.019	0.36	0.48
E	0.009	0.012	0.23	0.30
F	0.080	0.100	2.03	2.54
G	0.016	0.050	0.41	1.27
H	0.394	0.419	10.01	10.64
I	0.291	0.299	7.39	7.59

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