STANDARD
MICROSYSTEMS
CORPORATION

LAN83C183

PRELIMINARY

10/100 Mbps TX/FX/10BT
Fast Ethernet Physical Layer Device (PHY)

FEATURES

- Single Chip 100BASE-TX/FX/10BASE-T Fast Ethernet Physical Layer Solution
- Dual Speed - 10/100 Mbps
- Half And Full Duplex Support
- MII Interface to Ethernet Controller
- MI Interface for Configuration and Status
- Optional Repeater Interface
- AutoNegotiation: 10/100, Full/Half Duplex
- Meets All Applicable IEEE 802.3 Standards
- On Chip Wave Shaping - No External Filters Required
- Adaptive Equalizer
- Baseline Wander Correction
- Interface to External 100BASE-T4 PHY
- LED Outputs
  - Link
  - Activity
  - Collision
  - Full Duplex
  - 10/100
  - User Programmable
- Many User Features and Options
- Few External Components
- 3.3V Supply with 5V Tolerant I/O
- Pin Compatible with SEEQ TQ80223 10/100 Fast Ethernet PHY
- 64 Pin TQFP Package (1.0 mm Body Thickness)

GENERAL DESCRIPTION

The SMSC LAN83C183 is a highly integrated analog interface IC for twisted pair Ethernet applications. The LAN83C183 can be configured for either 100 Mbps (100BASE-TX or 100 BASE-FX) or 10 Mbps (10BASE-T) Ethernet operation. The 100BASE-FX is packaged in a 64 Pin TQFP package.

The LAN83C183 consists of a 4B5B/Manchester encoder/decoder, scrambler/descrambler, transmitter with wave shaping and output driver, twisted pair receiver with on chip equalizer and baseline wander correction, clock and data recovery, AutoNegotiation, controller interface (MII), and serial port (MI).

The addition of internal output waveshaping circuitry and on-chip filters eliminates the need for external filters normally required in 100BASE-TX and 10BASE-T applications.

The LAN83C183 can automatically configure itself for 100 or 10 Mbps and Full or Half Duplex operation with the on-chip AutoNegotiation algorithm.

The eleven 16-bit registers of the LAN83C183 can be accessed through the Management Interface (MI) serial port. These registers contain configuration inputs, status outputs, and device capabilities.

The LAN83C183 is ideal as a media interface for 100BASE-TX/10BASE-T adapter cards, PC Cards, motherboards, mobile applications, repeaters, switching hubs, and external PHY's.

The LAN83C183 operates from a single 3.3V supply. All inputs and outputs are 5V tolerant and will directly interface to other 5V devices.

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PIN CONFIGURATION

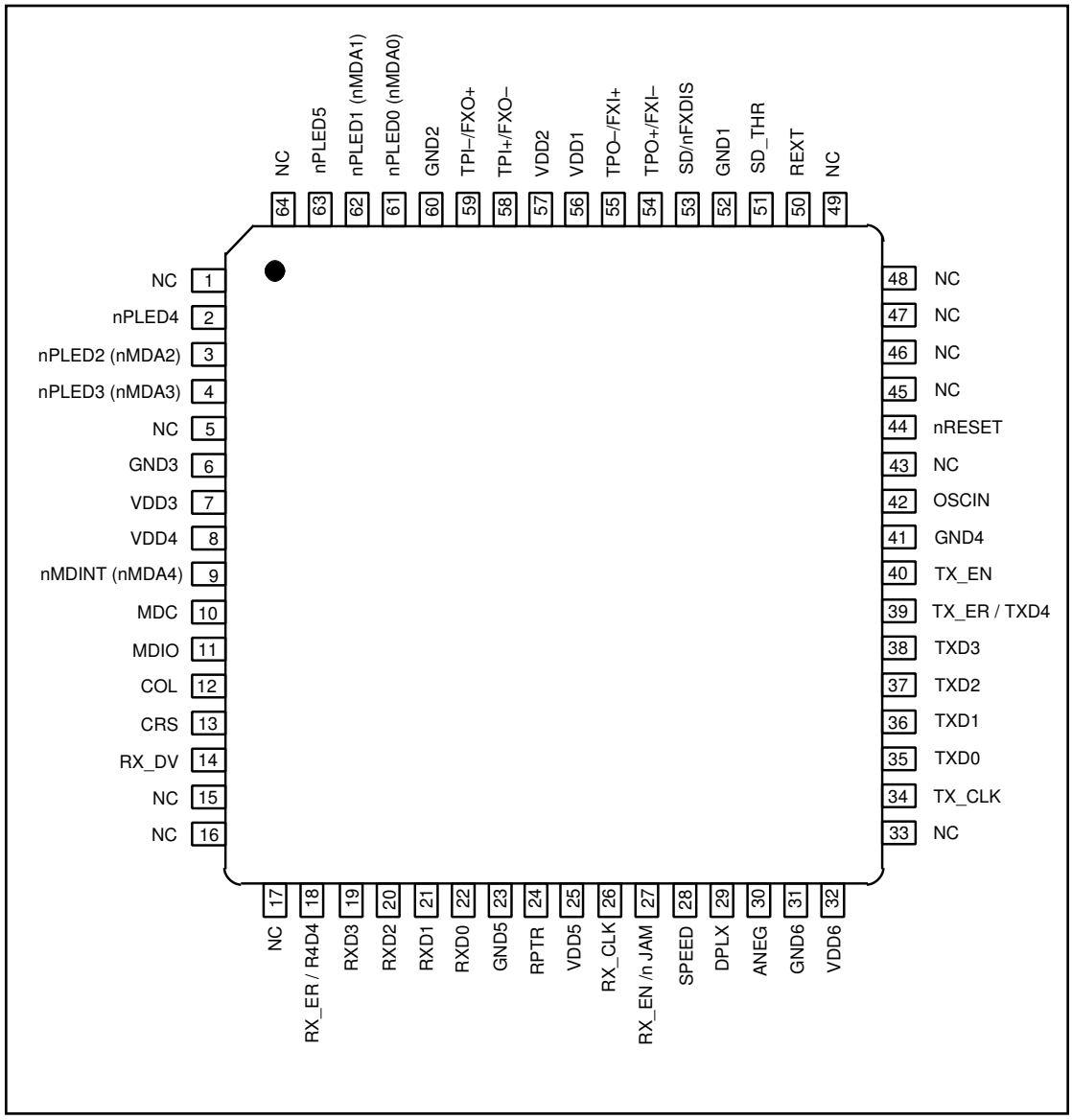


Table 1 - Pin Description

PIN #	PIN NAME	I/O	DESCRIPTION
32 25 8 7 57 56	VDD6 VDD5 VDD4 VDD3 VDD2 VDD1	—	**Positive Supply.** 3.3V ± 5% Volts
31 23 41 6 60 52	GND6 GND5 GND4 GND3 GND2 GND1	—	**Ground.** 0 Volts
54	TPO+/ FXI–	O/I	**Twisted Pair Transmit Output, Positive.** **FX Receive Input, Negative.**
55	TPO -/ FXI+	O/I	**Twisted Pair Transmit Output, Negative.** **FX Receive Input, Positive.**
58	TPI+/ FXO–	I/O	**Twisted Pair Receive Input, Positive.** **FX Transmit Output, Negative.**
59	TPI -/ FXO+	I/O	**Twisted Pair Receive Input, Negative.** **FX Transmit Output, Positive.**
53	SD/ nFXDIS	I	**FX Signal Detect Input/FX Interface Disable.** When this pin is not tied to GND, the FX interface is enabled and this pin becomes a signal detect ECL input. The trip point for this ECL input is determined by the voltage on SD_THR. When this pin is tied to GND, the FX interface is disabled (i.e. TP interface is enabled).
51	SD_THR	I	**Signal Detect Input Threshold Level Set.** The voltage on this pin determines the ECL threshold level (i.e. trip point) for the SD input pin so that the device can directly interface to both 3.3v and 5v fiber optic transceivers. Typically, this pin is either tied to GND (for 3.3v) or to an external voltage divider (for 5v).
50	REXT	—	**Transmit Current Set.** An external resistor connected between this pin and GND will set the output current for the TP and FX transmit outputs.
42	OSCIN	I	**Clock Oscillator Input.** There must be either a 25 Mhz crystal between this pin and GND or a 25 Mhz clock applied to this pin. TX_CLK output is generated from this input.
34	TX_CLK	O	**Transmit Clock Output.** This controller interface output provides a clock to an external controller. Transmit data from the controller on TXD, TX_EN, and TX_ER is clocked in on rising edges of TX_CLK and OSCIN.

Table 1 - Pin Description (continued)

PIN #	PIN NAME	I/O	DESCRIPTION
40	TX_EN	I	**Transmit Enable Input.** This controller interface input has to be asserted active high to indicate that data on TXD and TX_ER is valid, and it is clocked in on rising edges of TX_CLK and OSCIN.
38 37 36 35	TXD3 TXD2 TXD1 TXD0	I	**Transmit Data Input.** These controller interface inputs contain input nibble data to be transmitted on the TP outputs, and they are clocked in on rising edges of TX_CLK and OSCIN when TX_EN is asserted.
39	TX_ER / TXD4	I	**Transmit Error Input.** This controller interface input causes a special pattern to be transmitted on the twisted pair outputs in place of normal data, and it is clocked in on rising edges of TX_CLK when TX_EN is asserted. If the device is placed in the Bypass 4B5B Encoder mode, this pin is reconfigured to be the fifth TXD transmit data input, TXD4.
26	RX_CLK	O	**Receive Clock Output.** This controller interface output provides a clock to an external controller. Receive data on RXD, RX_DV, and RX_ER is clocked out on falling edges of RX_CLK.
13	CRS	O	**Carrier Sense Output.** This controller interface output is asserted active high when valid data is detected on the receive twisted pair inputs, and it is clocked out on falling edges of RX_CLK.
14	RX_DV	O	**Receive Data Valid Output.** This controller interface output is asserted active high when valid decoded data is present on the RXD outputs, and it is clocked out on falling edges of RX_CLK.
19 20 21 22	RXD3 RXD2 RXD1 RXD0	O	**Receive Data Output.** These controller interface outputs contain receive nibble data from the TP input, and they are clocked out on falling edges of RX_CLK.
18	RX_ER/ RXD4	O	**Receive Error Output.** This controller interface output is asserted active high when a coding or other specified errors are detected on the receive twisted pair inputs and it is clocked out on falling edges of RX_CLK. If the device is placed in the Bypass 4B5B Decoder mode, this pin is reconfigured to be the fifth RXD receive data output, RXD4.
12	COL	O	**Collision Output.** This controller interface output is asserted active high when a collision between transmit and receive data is detected.
10	MDC	I	**Management Interface (MI) Clock Input.** This MI clock shifts serial data into and out of MDIO on rising edges.
11	MDIO	I/O	**Management Interface (MI) Data Input/Output.** This bidirectional pin contains serial MI data that is clocked in and out on rising edges of the MDC clock.

Table 1 - Pin Description (continued)

PIN #	PIN NAME	I/O	DESCRIPTION
9	nMDINT (nMDA4)	I/O O.D. Pullup	**Management Interface Interrupt Output/Management Interface Address Input.** This pin is an interrupt output and is asserted active low whenever there is a change in certain MI serial port register bits, and deasserted after all changed bits have been read out. During powerup or reset, this pin is high impedance and the value on this pin is latched in as the physical device address nMDA4 for the MI serial port
4	nPLED3 (nMDA3)	I/O O.D. Pullup	**Programmable LED Output/Management Interface Address Input.** The default function of this pin is to be a 100 Mbps Link Detect output. This pin can also be programmed through the MI serial port to indicate other events or be user controlled. This pin can drive an LED from VDD. When programmed as 100 Mbps Link Detect Output (default): 1= No Detect 0 = 100 Mbps Link Detected During powerup or reset, this pin is high impedance and the value on this pin is latched inas the physical device address nMDA3 for the MI serial port.
3	nPLED2 (nMDA2)	I/O O.D. Pullup	**Programmable LED Output/Management Interface Address Input.** The default function of this pin is to be an Activity Detect output. This pin can also be programmed through the MI serial port to indicte other events or be user controlled. This pin can drive an LED from VDD. When programmed as an Activity Detect Output (default): 1 = No Activity 0 = Transmit Or Receive Packet Occurred, Hold Low for 100 mS During powerup or reset, this pin is high impedance and the value on this pin is latched in as the physical device address nMDA2 for the MI serial port.
62	nPLED1 (nMDA1)	I/O Pullup	**Programmable LED Output/Management Interface Address Input.** The default function of this pin is to be a Full Duplex Detect output. This pin can also be programmed through the MI serial port to indicate other events or be user controlled. This pin can drive an LED from both VDD and GND. When programmed as Full Duplex Detect Output (default). 1 = Half Duplex 0 = Full Duplex During powerup or reset, this pin is high impedance and the value on this pin is latched in as the physical address device address nMDA1 for the MI serial port.

Table 1 - Pin Description (continued)

PIN #	PIN NAME	I/O	DESCRIPTION
61	nPLED0 (nMDA0)	I/O Pullup	**Programmable LED Output/Management Interface Address Input.** The default function of this pin is to be a 10 Mbps Link Detect output. This pin can also be programmed through the MI serial port to indicate other events or be user controlled. This pin can drive an LED from both VDD and GND. When programmed as 10 Mbps Link Detect Output (default): 1 = No Detect 0 = 10 Mbps Link Detected During powerup or reset, this pin is high impedance and the value on this pin is latched in as the address nMDA0 for the MI serial port.
27	RX_EN/ nJAM	I	**Receive Enable Input** 1 = All Outputs Enabled 0 = Receive Controller Outputs are High Impedance (RX_CLK, RXD[3:0], RX_DV, RX_ER, COL). **Automatic Jam Input** 1 = Normal 0 = Jam Packet Transmitted when Receive Activity Detected
63	nPLED5	O O.D. Pullup	**Receive LED Output.** The function of this pin is to be a Receive Activity Detect output and this pin can drive an LED from VDD. 1 = No Receive Activity 0 = Receive Packet Occurred, Hold Low for 100 mS
2	nPLED4	O O.D. Pullup	**Transmit LED Output.** The function of this pin is to be a Transmit Activity Detect output and this pin can drive an LED from VDD. 1 = No Transmit Activity 0 = Transmit Packet Occurred, Hold Low for 100 mS
24	RPTR	I Pull-down	**Repeater Mode Enable Input.** 1 = Repeater Mode Enabled 0 = Normal Operation
28	SPEED	I Pullup	**Speed Select Input.** This input pin selects 10/100 Mbps operation when pin ANEG = 0. When ANEG = 1, this pin is ignored and 10/100 Mbps operation is determined by register Bit 0.13 or outcome of AutoNegotiation. 1 = 100 Mbps 0 = 10 Mbps

Programmable LED Output/Management Interface Address Input. The defau

Table 1 - Pin Description (continued)

PIN #	PIN NAME	I/O	DESCRIPTION
29	nDPLX	I Pullup	**Full/Half Duplex Select Input.** This input pin selects Half/Full Duplex operation when pin ANEG = 0. When ANEG = 1, this pin is ignored and Half/Full Duplex operation is determined by register Bit 0.8 or outcome of AutoNegotiation. 1 = Full Duplex 0 = Half Duplex
30	ANEG	I Pullup	**AutoNegotiation Enable Input.** 1 = AutoNegotiation On; AutoNegotiation Enable, 10/100 and Half/Full Duplex determined by register Bits 0.12, 0.13, and 0.8 or outcome of AutoNegotiation. 0 = AutoNegotiation Off; 10/100 and Half/Full Duplex determined by SPEED and nDPLX Pins.
44	nRESET	I Pullup	**RESET Input** 1 = Normal Operation 0 = Device Reset
1 5 15 16 17 33 43 45 46 47 48 49 64	NC		**No Connect.**

BLOCK DIAGRAM

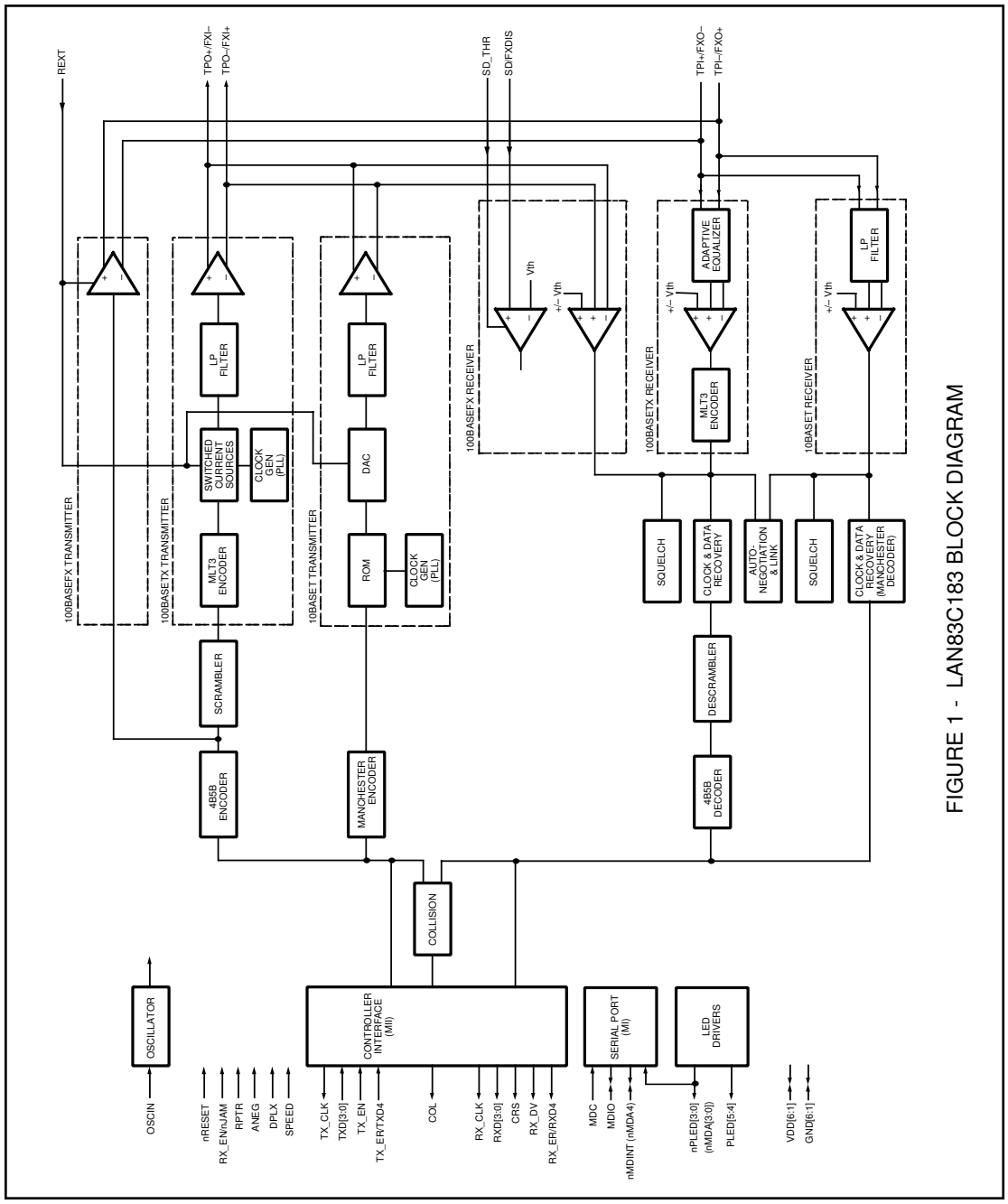


FIGURE 1 - LAN83C183 BLOCK DIAGRAM

FUNCTIONAL DESCRIPTION

GENERAL

The LAN83C183 is a complete 100/10 Mbps Ethernet Media Interface IC. The LAN83C183 has nine main sections: controller interface, encoder, decoder, scrambler, descrambler, clock and data recovery, twisted pair transmitter, twisted pair receiver, and MI serial port. A block diagram is shown in Figure 1.

The LAN83C183 can operate as a 100BASE-TX/FX device (hereafter referred to as 100 Mbps mode) or as a 10BASE-T device (hereafter referred to as 10 Mbps mode). The difference between the 100 Mbps mode and the 10 Mbps mode is data rate, signalling protocol, and allowed wiring. The 100 Mbps TX mode uses two pairs of category 5 or better UTP or STP twisted pair cable with 4B5B encoded, scrambled, and MLT-3 coded 62.5 MHz ternary data to achieve a thruput of 100 Mbps. The 100 Mbps FX mode uses two fiber cables with 4B5B encoded, 125 MHz binary data to achieve a thruput of 100 Mbps. The 10 Mbps mode uses two pairs of category 3 or better UTP or STP twisted pair cable with Manchester encoded, 10 MHz binary data to achieve a 10 Mbps thruput. The data symbol format on the twisted pair cable for the 100 and 10 Mbps modes are defined in IEEE 802.3 specifications and shown in Figure 2.

On the transmit side for 100 Mbps TX operation, data is received on the controller interface from an

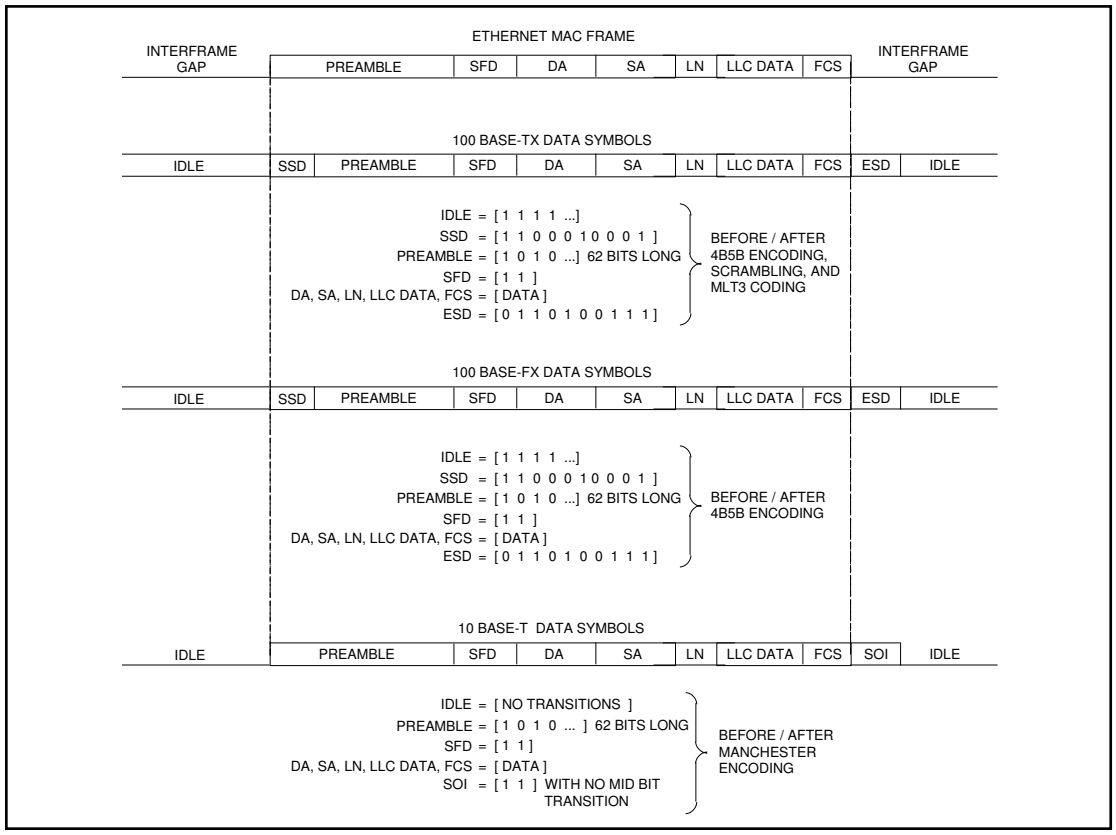
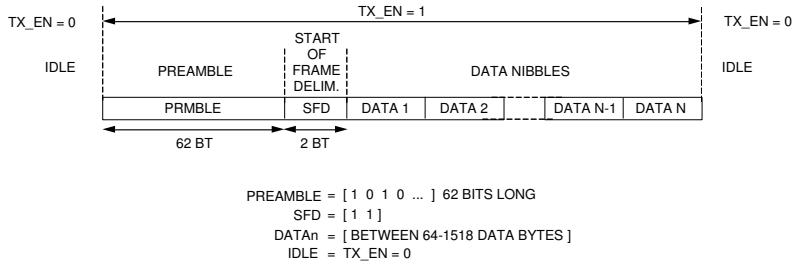
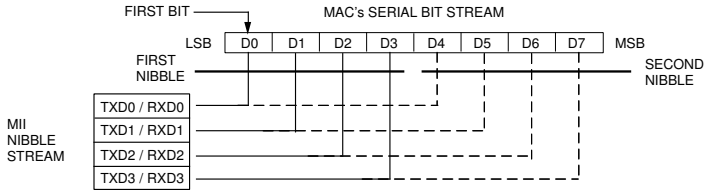


FIGURE 2 - TX/FX/10BT FRAME FORMAT



PREAMBLE = [1 0 1 0 ...] 62 BITS LONG
SFD = [1 1]
DATAn = [BETWEEN 64-1518 DATA BYTES]
IDLE = TX_EN = 0

a.) MII Frame Format



b.) MII Nibble Order

Signals	Bit Value																			
TXDO	X	X	1[1]	1	1	1	1	1	1	1	1	1	1	1	1	1	1[2]	1	D0[3]	D4[4]
TXD1	X	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	D1	D5
TXD2	X	X	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	D2	D6
TXD3	X	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	D3	D7
TX_EN	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

1. 1st preamble nibble transmitted.
2. 1st sfd nibble transmittted.
3. 1st data nibble transmitted.
4. D0 thru D7 are the first 8 bits of the data field.

c.) Transmit Preamble and SFD bits

Signals	Bit Value																			
RXDO	X	1[1]	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1[2]	1	D0[3]	D4[4]
RXD1	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	D1	D5
RXD2	X	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	D2	D6
RXD3	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	D3	D7
RX_DV	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

1. 1st preamble nibble received. Depending on mode, device may eliminate either all or some of the preamble nibbles, up to 1st SFD nibble.
2. 1st sfd nibble received.
3. 1st data nibble received.
4. D0 thru D7 are the first 8 bits of the data field.

d.) Receive Preamble and SFD Bits

FIGURE 3 - MII FRAME FORMAT

external Ethernet controller per the format shown in Figure 3. The data is then sent to the 4B5B encoder for formatting. The encoded data is then sent to the scrambler. The scrambled and encoded data is then sent to the TP transmitter. The TP transmitter converts the encoded and scrambled data into MLT-3 ternary format, preshapes the output, and drives the twisted pair cable.

On the receive side for 100 Mbps TX operation, the twisted pair receiver receives incoming encoded and scrambled MLT-3 data from the twisted pair cable, remove any high frequency noise, equalizes the input signal to compensate for the effects of the cable, qualifies the data with a squelch algorithm, and converts the data from MLT-3 coded twisted pair levels to internal digital levels. The output of the twisted pair receiver then goes to a clock and data recovery block which recovers a clock from the incoming data, uses the clock to latch in valid data into the device, and converts the data back to NRZ format. The NRZ data is then unscrambled and decoded by the 4B5B decoder and descrambler, respectively, and outputted to an external Ethernet controller by the controller interface.

100 Mbps FX operation is similar to 100 Mbps TX operation except (1) the transmit output/receive input is not scrambled or MLT3 encoded, (2) the transmit data is output to a FX transmitter instead of the TP waveshaper/transmitter, (3) the receive data is input to the FX ECL level detector instead of the equalizer and associated TP circuitry, and (4) the FX Interface has a signal detect input.

10 Mbps operation is similar to the 100 Mbps TX operation except, (1) there is no scrambler/descrambler, (2) the encoder/decoder is Manchester instead of 4B5B, (3) the data rate is 10 Mbps instead of 100 Mbps, and (4) the twisted pair symbol data is two level Manchester instead of ternary MLT-3.

The Management Interface, (hereafter referred to as the MI serial port), is a two pin bidirectional link through which configuration inputs can be set and status outputs can be read.

Each block plus the operating modes are described in more detail in the following sections. Since the LAN83C183 can operate either as a 100BASE-TX/FX or a 10BASE-T device, each of the following sections describes the performance of the respective section in both the 100 and 10 Mbps modes.

CONTROLLER INTERFACE

General

The LAN83C183 has two interfaces to an external controller: Media Independent Interface (referred to as the MII) and Five Bit interface (referred to as the FBI).

MII - 100 Mbps

The MII is a nibble wide packet data interface defined in IEEE 802.3 and shown in Figure 3. The LAN83C183 meets all the MII requirements outlined in IEEE 802.3. The LAN83C183 can directly connect, without any external logic, to any Ethernet controllers or other devices which also complies with the IEEE 802.3 MII specifications. The MII frame format is shown in Figure 3.

The MII consists of eighteen signals: four transmit data bits (TXD[3:0]), transmit clock (TX_CLK), transmit enable (TX_EN), transmit error (TX_ER), four receive data bits (RXD[3:0]), receive clock (RX_CLK), carrier sense (CRS), receive data valid (RX_DV), receive data error (RX_ER), and collision (COL). The transmit and receive clocks operate at 25 MHz in 100 Mbps mode.

On the transmit side, the TX_CLK output runs continuously at 25 Mhz. When no data is to be transmitted, TX_EN has to be deasserted. While TX_EN is deasserted, TX_ER and TXD[3:0] are ignored and no data is clocked into the device. When TX_EN is asserted on the rising edge of TX_CLK, data on TXD[3:0] is clocked into the device on rising edges of the TX_CLK output clock. TXD[3:0] input data is nibble wide packet data whose format needs to be the same as specified in IEEE 802.3 and shown in Figure 3. When all data on TXD[3:0] has been latched into the device, TX_EN has to be deasserted on the rising edge of TX_CLK.

TX_ER is also clocked in on rising edges of the TX_CLK clock. TX_ER is a transmit error signal which, when asserted, will substitute an error nibble in place of the normal data nibble that was clocked in on TXD[3:0]. The error nibble is defined to be the /H/ symbol which is defined in IEEE 802.3 and shown in Table 2.

Since OSCIN input clock generates the TX_CLK output clock, TXD[3:0], TX_EN, and TX_ER are also clocked in on rising edges of OSCIN.

On the receive side, as long as a valid data packet is not detected, CRS and RX_DV are deasserted and RXD[3:0] is held low. When the start of packet is detected , CRS and RX_DV are asserted on falling edge of RX_CLK. The assertion of RX_DV indicates that valid data is clocked out on RXD[3:0] on falling edges of the RX_CLK clock. The RXD[3:0] data has the same frame structure as the TXD[3:0] data and is specified in IEEE 802.3 and shown in Figure 3. When the end of packet is detected, CRS and RX_DV are deasserted, and RXD[3:0] is held low. CRS and RX_DV also stay deasserted if the device is in the Link Fail State.

RX_ER is a receive error output which is asserted when certain errors are detected on a data nibble. RX_ER is asserted on the falling edge of RX_CLK for the duration of that RX_CLK clock cycle during which the nibble containing the error is being outputted on RXD[3:0].

The collision output, COL, is asserted whenever the collision condition is detected.

MII - 10 Mbps

10 Mbps operation is identical to the 100 Mbps operation except, (1) TX_CLK and RX_CLK clock frequency is reduced to 2.5 MHZ, (2) TX_ER is ignored, (3) RX_ER is disabled and always held low, and (4) receive operation is modified as follows: On the receive side, when the squelch circuit determines that invalid data is present on the TP inputs, the receiver is idle. During idle, RX_CLK follows TX_CLK, RXD[3:0] is held low, and CRS and RX_DV are deasserted. When a start of packet is detected on the TP receive inputs, CRS is asserted and the clock recovery process starts on the incoming TP input data. After the receive clock has been recovered from the data, the RX_CLK is switched over to the recovered clock and the data valid signal RX_DV is asserted on a falling edge of RX_CLK. Once RX_DV is asserted, valid data is clocked out on RXD[3:0] on falling edges of the RX_CLK clock. The RXD[3:0] data has the same packet structure as the TXD[3:0] data and is formatted on RXD[3:0] as specified in IEEE 802.3 and shown in Figure 3. When the end of packet is detected, CRS and RX_DV are deasserted. CRS and RX_DV also stay deasserted as long as the device is in the Link Fail State.

FBI - 100 Mbps

The Five Bit Interface (also referred to as the FBI) is a five bit wide interface that is produced when the 4B5B encoder/decoder is bypassed. The FBI is primarily used for repeaters or Ethernet controllers which have integrated encoder/decoders.

The FBI is identical to the MII except, (1) the FBI data path is five bits wide, not nibble wide like the MII, (2) TX_ER pin is reconfigured to be the fifth transmit data bit, TXD4, and (3) RX_ER pin is reconfigured to be the fifth receive data bit RXD4, (4) CRS is asserted as long as the device is in the Link Pass State, (5) COL is not valid, (6) RX_DV is not valid, and (7) TX_EN is ignored.

FBI - 10 Mbps

The FBI is not available in 10 Mbps mode.

Selection Of MII Or FBI

The FBI is automatically enabled when the 4B5B encoder/decoder is bypassed. Bypassing the encoder/decoder passes the 5B symbols between the receiver/transmitter directly to the FBI without any alteration or substitutions noted in the Encoder and Decoder sections. The 4B5B encoder/decoder can be bypassed by setting the bypass encoder bit in the MI serial port Configuration 1 register.

When the FBI is enabled, it may also be desirable to bypass the scrambler/descrambler and disable the internal CRS loopback function. The scrambler/

descrambler can be bypassed by setting the bypass scrambler bit in the MI serial port Configuration 1 register. The internal CRS loopback can be disabled by setting the TX_EN to CRS loopback disable bit in the MI serial port Configuration 1 register.

MII Disable

The MII and FBI inputs and outputs can be disabled by setting the MII disable bit in the MI serial port Control register. When the MII is disabled, the MII/FBI inputs are ignored, the MII/FBI outputs are placed in high impedance state, and the TP output is high impedance.

If the MI address lines, nMDA[4:0], are pulled high during reset or powerup, the LAN83C183 powers up and resets with the MII and FBI disabled. Otherwise, the LAN83C183 powers up and resets with the MII and FBI enabled.

Receive Output High Impedance Control

The RX_EN/nJAM pin can be configured to be RX_EN, a high impedance control for the receive controller output signals, by setting the R/J Configuration select bit in the MI serial port Configuration 2 register. When this pin is configured to be RX_EN and is deasserted active low, the following outputs will be placed in the high impedance state: RX_CLK, RXD[3:0], RX_DV, RX_ER, and COL.

TX_EN to CRS Loopback Disable

The internal TX_EN to CRS loopback can be disabled by appropriately setting the TXEN to CRS loopback disable bit in the MI serial port Configuration 1 register.

ENCODER

4B5B Encoder - 100 Mbps

100BASE-TX requires that the data be 4B5B encoded. 4B5B coding converts the 4-Bit data nibbles into 5-Bit date code words. The mapping of the 4B nibbles to the 5B code words is specified in IEEE 802.3 and shown in Table 2. The 4B5B encoder on the LAN83C183 takes 4B nibbles from the controller interface, converts them into 5B words according to Table 2, and sends the 5B words to the scrambler. The 4B5B encoder also substitutes the first 8 bits of the preamble with the SSD delimiters (a.k.a. /J/K/ symbols) and adds an ESD delimiter (a.k.a /T/R/ symbols) to the end of every packet, as defined in IEEE 802.3 and shown in Figure 2. The 4B5B encoder also fills the period between packets, called the idle period, with the a continuous stream of idle symbols, as shown in Figure 2.

Manchester Encoder - 10 Mbps

The Manchester encoding process combines clock and NRZ data such that the first half of the data bit contains the complement of the data, and the second half of the data bit contains the true data, as specified in IEEE 802.3. This guarantees that a transition always occurs in the middle of the bit cell. The Manchester encoder on the LAN83C183 converts the 10 Mbps NRZ data from the controller interface into a Manchester Encoded data stream for the TP transmitter and adds a start of idle pulse (SOI) at the end of the packet as specified in IEEE 802.3 and shown in Figure 2. The Manchester encoding process is only done on actual packet data, and the idle period between packets is not Manchester encoded and filled with link pulses.

Encoder Bypass

The 4B5B encoder can be bypassed by setting the bypass encoder/decoder bit in the MI serial port Configuration 1 register. When this bit is set to bypass the encoder/decoder, 5B code words are passed directly from the controller interface to the scrambler without any of the alterations described in the 4B5B Encoder section. Setting this bit automatically places the device in the FBI mode as described in the Controller Interface section.

DECODER

4B5B Decoder - 100 Mbps

Since the TP input data is 4B5B encoded on the transmit side, it must also be decoded by the 4B5B decoder on the receive side. The mapping of the 5B nibbles to the 4B code words is specified in IEEE 802.3 and shown in Table 2. The 4B45 decoder on

the LAN83C183 takes the 5B code words from the descrambler, converts them into 4B nibbles per Table 2, and sends the 4B nibbles to the controller interface. The 4B5B decoder also strips off the SSD delimiter (a.k.a. /J/K/ symbols) and replaces them with two 4B Data 5 nibbles (a.k.a /5/ symbol), and strips off the ESD delimiter (a.k.a /T/R/ symbols) and replaces it with two 4B Data 0 nibbles (a.k.a /I/ symbol), per IEEE 802.3 specifications and shown in Figure 2.

The 4B5B decoder detects SSD, ESD and, codeword errors in the incoming data stream as specified in IEEE 802.3. These errors are indicated by asserting RX_ER output while the errors are being transmitted across RXD[3:0], and they are also indicated in the serial port by setting SSD, ESD, and codeword error bits in the MI serial port Status Output register.

Manchester Decoder - 10 Mbps

In Manchester coded data, the first half of the data bit contains the complement of the data, and the second half of the data bit contains the true data. The Manchester decoder in the LAN83C183 converts the Manchester encoded data stream from the TP receiver into NRZ data for the controller interface by decoding the data and stripping off the SOI pulse. Since the clock and data recovery block has already separated the clock and data from the TP receiver, the Manchester decoding process to NRZ data is inherently performed by that block.

Decoder Bypass

The 4B5B decoder can be bypassed by setting the bypass encoder/decoder bit in the MI serial port Configuration 1 register. When this bit is set to bypass the encoder/decoder, (1) 5B code words are passed directly to the controller interface from the descrambler without any of the alterations described in the 4B5B Decoder section, and (2) CRS is continuously asserted whenever the device is in the Link Pass state. Setting this bit automatically places the device in the FBI mode as described in the Controller Interface section.

Table 2 - 4B/5B Symbol Mapping

SYMBOL NAME	DESCRIPTION	5B CODE	4B CODE
0	Data 0	11110	0000
1	Data 1	01001	0001
2	Data 2	10100	0010
3	Data 3	10101	0011
4	Data 4	01010	0100
5	Data 5	01011	0101
6	Data 6	01110	0110
7	Data 7	01111	0111
8	Data 8	10010	1000
9	Data 9	10011	1001
A	Data A	10110	1010
B	Data B	10111	1011
C	Data C	11010	1100
D	Data D	11011	1101
E	Data E	11100	1110
F	Data F	11101	1111
I	Idle	11111	0000
J	SSD #1	11000	0101
K	SSD #2	10001	0101
T	ESD #1	01101	0000
R	ESD #2	00111	0000
H	Halt	00100	Undefined
---	Invalid codes	All others*	0000*

* These 5B codes are not used. For decoder, these 5B codes are decoded to 4B 0000. For encoder, 4B 0000 is encoded to 5B 11110, as shown in symbol Data 0.

CLOCK AND DATA RECOVERY

Clock Recovery - 100 Mbps

Clock recovery is done with a PLL. If there is no valid data present on the TP inputs, the PLL is locked to the 25 MHz TX_CLK. When valid data is detected on the TP inputs with the squelch circuit and when the adaptive equalizer has settled, the PLL input is switched to the incoming data on the TP input. The PLL then recovers a clock by locking onto the transitions of the incoming signal from the twisted pair wire. The recovered clock frequency is a 25 MHz nibble clock, and that clock is outputted on the controller interface signal RX_CLK.

Data Recovery - 100 Mbps

Data recovery is performed by latching in data from the TP receiver with the recovered clock extracted by the PLL. The data is then converted from a single bit stream into nibble wide data word according to the format shown in Figure 3.

Clock Recovery - 10 Mbps

The clock recovery process for 10 Mbps mode is identical to the 100 Mbps mode except, (1) the recovered clock frequency is 2.5 MHz nibble clock, (2) the PLL is switched from TX_CLK to the TP input when the squelch indicates valid data, (3) The PLL takes up to 12 transitions (bit times) to lock onto the preamble, so some of the preamble data symbols are lost, but the clock recovery block recovers enough preamble symbols to pass at least 6 nibbles of preamble to the receive controller interface as shown in Figure 3.

Data Recovery - 10 Mbps

The data recovery process for 10 Mbps mode is identical to the 100 Mbps mode. As mentioned in the Manchester Decoder section, the data recovery process inherently performs decoding of Manchester encoded data from the TP inputs.

SCRAMBLER

100 Mbps

100BASE-TX requires scrambling to reduce the radiated emissions on the twisted pair. The LAN83C183 scrambler takes the encoded data from the 4B5B encoder, scrambles it per the IEEE 802.3 specifications, and sends it to the TP transmitter.

10 Mpbs

A scrambler is not used in 10 Mbps mode.

Scrambler Bypass

The scrambler can be bypassed by setting the bypass scrambler/descrambler bit in the MI serial port Configuration 1 register. When this bit is set, the 5B data bypasses the scrambler and goes directly from the 4B5B encoder to the twisted pair transmitter.

DESCRAMBLER

100 Mbps

The LAN83C183 descrambler takes the scrambled data from the data recovery block, descrambles it per the IEEE 802.3 specifications, aligns the data on the correct 5B word boundaries, and sends it to the 4B5B decoder.

The algorithm for synchronization of the descrambler is the same as the algorithm outlined in the IEEE 802.3 specification. Once the descrambler is synchronized, it will maintain synchronization as long as enough descrambled idle pattern 1's are detected within a given interval. To stay in synchronization, the descrambler needs to detect at least 25 consecutive descrambled idle pattern 1's in a 1 mS interval. If 25 consecutive descrambled idle pattern 1's are not detected within the 1 mS interval, the descrambler goes out of synchronization and restarts the synchronization process.

If the descrambler is in the unsynchronized state, the descrambler loss of synchronization detect bit is set in the MI serial port Status Output register to indicate this condition. Once this bit is set, it will stay set until the descrambler achieves synchronization.

10 Mpbs

A descrambler is not used in 10 Mbps mode.

Descrambler Bypass

The descrambler can be bypassed by setting the bypass scrambler/descrambler bit in the MI serial port Configuration 1 register. When this bit is set, the data bypasses the descrambler and goes directly from the TP receiver to the 4B5B decoder.

TWISTED PAIR TRANSMITTER

Transmitter - 100 Mbps

The TX transmitter consists of a MLT-3 encoder, waveform generator and line driver.

The MLT-3 encoder converts the NRZ data from the scrambler into a three level MLT-3 code required by IEEE 802.3. MLT-3 coding uses three levels and converts 1's to transitions between the three levels, and converts 0's to no transitions or changes in level.

The purpose of the waveform generator is to shape the transmit output pulse. The waveform generator takes the MLT-3 three level encoded waveform and uses an array of switched current sources to control the rise/fall time and level of the signal at the output. The output of the switched current sources then goes through a low pass filter in order to "smooth" the current output and remove any high frequency components. In this way, the waveform generator preshapes the output waveform transmitted onto the twisted pair cable to meet the pulse template requirements outlined in IEEE 802.3. The waveform generator eliminates the need for any external filters on the TP transmit output.

The line driver converts the shaped and smoothed waveform to a current output that can drive 100 meters of category 5 unshielded twisted pair cable or 150 Ohm shielded twisted pair cable.

Transmitter - 10 Mbps

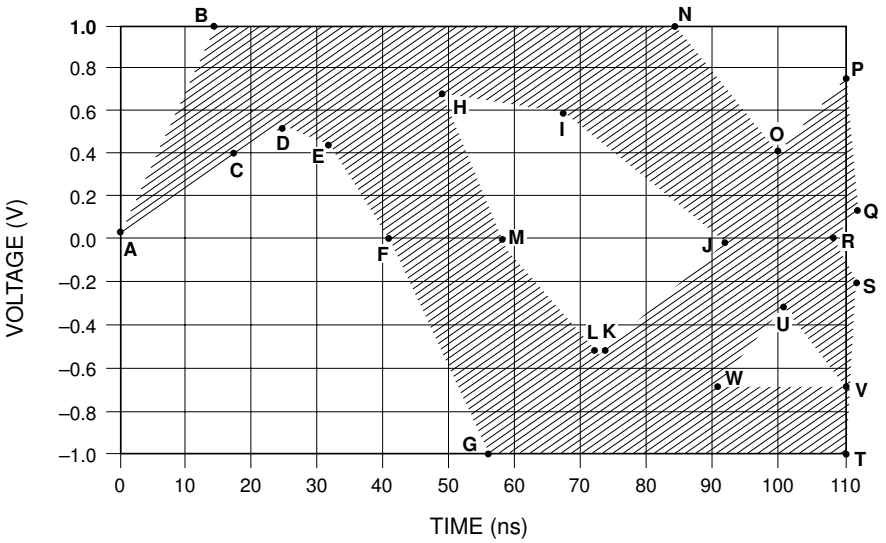
The transmitter operation in 10 Mbps mode is much different than the 100 Mbps transmitter. Even so, the transmitter still consists of a waveform generator and line driver.

The purpose of the waveform generator is to shape the output transmit pulse. The waveform generator consists of a ROM, DAC, clock generator, and filter. The DAC generates a stair-stepped representation of the desired output waveform. The stairstepped DAC output then goes through a low pass filter in order to "smooth" the DAC output and remove any high frequency components. The DAC values are determined from the ROM outputs; the ROM contents are chosen to shape the pulse to the desired template and are clocked into the DAC at high speed by the clock generator. In this way, the waveform generator preshapes the output waveform to be transmitted onto the twisted pair cable to meet the pulse template requirements outlined in IEEE 802.3 Clause 14 and also shown in Figure 4. The waveshaper replaces and eliminates external filters on the TP transmit output.

The line driver converts the shaped and smoothed waveform to a current output that can drive 100 meters of category 3/4/5 100 Ohm unshielded twisted pair cable or 150 Ohm shielded twisted pair cable tied directly to the TP output pins without any external filters. During the idle period, no output signal is transmitted on the TP outputs (except link pulse).

Transmit Level Adjust

The transmit output current level is derived from an internal reference voltage and the external resistor on REXT pin. The transmit level can be adjusted with either (1) the external resistor on the REXT pin,



Reference	Time (ns) Internal MAU	Voltage (V)
A	0	0
B	15	1.0
C	15	0.4
D	25	0.55
E	32	0.45
F	39	0
G	57	-1.0
H	48	0.7
I	67	0.6
J	89	0
K	74	-0.55
L	73	-0.55
M	61	0
N	85	1.0
O	100	0.4
P	110	0.75
Q	111	0.15
R	111	0
S	111	-0.15
T	110	-1.0
U	100	-0.3
V	110	-0.7
W	90	-0.7

FIGURE 4 - TP OUTPUT VOLTAGE TEMPLATE-10 MBPS

or (2) the four transmit level adjust bits in the MI serial port Configuration 1 register as shown in Table 3. The adjustment range is approximately -14% to +16% in 2% steps.

Table 3 - Transmit Level Adjust

TLVL[3:0]	GAIN
0000	1.16
0001	1.14
0010	1.12
0011	1.10
0100	1.08
0101	1.06
0110	1.04
0111	1.02
1000	1.00
1001	0.98
1010	0.96
1011	0.94
1100	0.92
1101	0.90
1110	0.88
1111	0.86

Transmit Rise And Fall Time Adjust

The transmit output rise and fall time can be adjusted with the two transmit rise/fall time adjust bits in the MI serial port Configuration 1. The adjustment range is -0.25 nS to +0.5 nS in 0.25 nS steps.

STP (150 Ohm) Cable Mode

The transmitter can be configured to drive 150 Ohm shielded twisted pair cable. The STP mode can be selected by appropriately setting the cable type select bit in the MI serial port Configuration 1 register. When STP mode is enabled, the output current is automatically adjusted to comply with IEEE 802.3 levels.

Transmit Activity Indication

Transmit activity can be programmed to appear on some of the nPLED[5:0] pins by appropriately setting the programmable LED output select bits in the MI serial port LED Configuration 2 register as described in Table 5. When one or more of the nPLED[5:0] pins is programmed to be an activity or transmit activity detect output, that pin is asserted low for 100 mS every time a transmit packet occurs. The nPLED[5:0] output is open drain with pullup resistor and can drive an LED from VDD or can drive another digital input.

Transmit Disable

The TP transmitter can be disabled by setting the transmit disable bit in the MI serial port Configuration 1 register. When the transmit disable bit is set, the TP transmitter is forced into the idle state, no data is transmitted, no link pulses are transmitted, and internal loopback is disabled.

Transmit Powerdown

The TP transmitter can be powered down by setting the transmit powerdown bit in the MI serial port Configuration 1 register. When the transmit powerdown bit is set, the TP transmitter is powered down, the TP transmit outputs are high impedance, and the rest of the LAN83C183 operates normally.

TWISTED PAIR RECEIVER

Receiver - 100 Mbps

The TX receiver detects input signals from the twisted pair input and convert it to a digital data bit stream ready for clock and data recovery. The receiver can reliably detect data from a 100BASE-TX compliant transmitter that has been passed through 0-100 meters of 100 Ohm category 5 UTP or 150 Ohm STP.

The TX receiver consists of an adaptive equalizer, baseline wander correction circuit, comparators, and MLT-3 decoder. The TP inputs first go to an

adaptive equalizer. The adaptive equalizer compensates for the low pass characteristic of the cable, and it has the ability to adapt and compensate for 0-100 meters of category 5,100 Ohm UTP or 150 Ohm STP twisted pair cable. The baseline wander correction circuit restores the DC component of the input waveform that was removed by external transformers. The comparators convert the equalized signal back to digital levels and are used to qualify the data with the squelch circuit. The MLT-3 decoder takes the three level MLT-3 digital data from the comparators and converts it to back to normal digital data to be used for clock and data recovery.

Receiver - 10 Mbps

The 10 Mbps receiver is able to detect input signals from the twisted pair cable that are within the template shown in Figure 5. The inputs are biased by internal resistors. The TP inputs pass through a low pass filter designed to eliminate any high frequency noise on the input. The output of the receive filter goes to two different types of comparators, squelch and zero crossing. The squelch comparator determines whether the signal is valid, and the zero crossing comparator is used to sense the actual data transitions once the signal is determined to be valid. The output of the squelch comparator goes to the squelch circuit and is also used for link pulse detection, SOI detection, and reverse polarity detection; the output of the zero crossing comparator is used for clock and data recovery in the Manchester decoder.

TP Squelch - 100 Mbps

The squelch block determines if the TP input contains valid data. The 100 Mbps TP squelch is one of the criteria used to determine link intergrity. The squelch comparators compare the TP inputs against fixed positive and negative thresholds, called squelch levels. The output from the squelch comparator goes to a digital squelch circuit which determines if the receive input data on that channel is valid. If the data is invalid, the receiver is in the squelched state. If the input voltage exceeds the squelch levels at least 4 times with alternating polarity within a 10 µS interval, the data is considered to be valid by the squelch circuit and the receiver now enters into the unquelch state. In the unsquelch state, the receive threshold level is reduced by approximately 30% for noise immunity reasons and is called the unsquelch level. When the receiver is in the unsquelch state, then the input signal is deemed to be valid. The device stays in the unsquelch state until loss of data is detected. Loss of data is detected if no alternating polarity unsquelch transitions are detected during any 10 µS interval. When the loss of data is detected, the receive squelch is turned on again.

TP Squelch, 10 Mbps

The TP squelch algorithm for 10 Mbps mode is identical to the 100 Mbps mode except, (1) the 10 Mbps TP squelch algorithm is not used for link integrity but to sense the beginning of a packet, (2) the receiver goes into the unsquelch state if the input voltage exceeds the squelch levels for three bit times with alternating polarity within a 50-250 nS interval, (3) the receiver goes into the squelch state when idle is detected, (4) unsquelch detection has

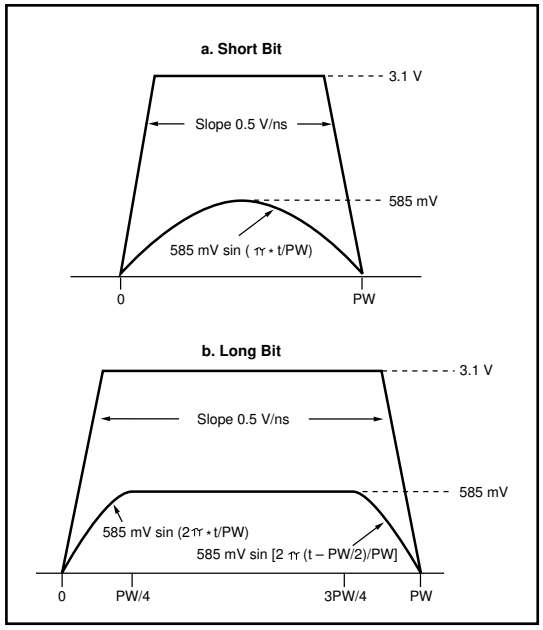


FIGURE 5 -
TP INPUT VOLTAGE TEMPLATE-10MBPS

no affect on link integrity, link pulses are used for that in 10 Mbps mode, (5) start of packet is determined when the receiver goes into the unsquelch state and CRS is asserted, and (6) the receiver meets the squelch requirements defined in IEEE 802.3 Clause 14.

Equalizer Disable

The adaptive equalizer can be disabled by setting the equalizer disable bit in the MI serial port Configuration 1 register. When disabled, the equalizer is forced into the response it would normally have if zero cable length was detected.

Receive Level Adjust

The receiver squelch and unsquelch levels can be lowered by 4.5 dB by setting the receive level adjust bit in the MI serial port Configuration 1 register. By setting this bit, the device may be able to support longer cable lengths.

Receive Activity Indication

Receive activity can be programmed to appear on some of the nPLED[5:0] pins by appropriately setting the programmable LED output select bits in the MI serial port LED Configuration 2 register as shown in Table 5. When one or more of the nPLED[5:0] pins is programmed to be an receive activity or activity detect output, that pin is asserted low for 100 mS every time a receive packet occurs. The nPLED[5:0] outputs are open drain with pullup resistor and can drive an LED from VDD or can drive another digital input.

FX TRANSMITTER & RECEIVER

General

The FX transmitter and receiver implement the 100BaseFX function defined in IEEE 802.3. 100BaseFX is intended for transmission and reception of data over fiber and is specified to operate at 100 Mbps. Thus, the FX transmitter and receiver in the device only operate when the device is placed in 100 Mbps mode.

Transmitter

The FX transmitter converts data from the 4B5B encoder into binary NRZI data and outputs the data onto the FXO+/- pins. The output driver is a differential current source that will drive a 100 ohm load to ECL levels. The FXO+/- pins can directly drive an external fiber optic transceiver. The FX transmitter meets all the requirements defined in IEEE 802.3.

The FX transmit output current level is derived from an internal reference voltage and the external resistor on REXT pin. The FX transmit level can be adjusted with this resistor or it can also be adjusted with the two FX transmit level adjust bits in the MI serial port Mask register as shown in Table 4.

TABLE 4 - FX TRANSMIT LEVEL ADJUST

FXLVL[1:0]	GAIN
11	1.30
10	1.15
01	0.85
00	1.00

Receiver

The FX receiver (1) converts the differential ECL inputs on the FXI+/- pins to a digital bit stream, (2) validates the data on FXI+/- with the SD/nFXDIS input pin, and (3) enable/disables the FX interface with the SD/nFXDIS pin. The FX receiver meets all requirements defined in IEEE 802.3.

The input to the FXI+/- pins can be directly driven from a fiber optic transceiver and first goes to a comparator. The comparator compares the input waveform against the internal ECL threshold levels to produce a low jitter serial bit stream with internal logic levels. The data from the comparator output is then passed to the clock and data recovery block, provided that the signal detect input, SD/nFXDIS, is asserted. The signal detect function is described in the next section.

Signal Detect

The FX receiver has a signal detect input pin, SD/nFXDIS, which indicates whether the incoming data on FXI+/- is valid or not. The SD/nFXDIS can be driven directly from an external fiber optic transceiver and meets all requirements defined in the IEEE 802.3 specifications.

The SD/nFXDIS input goes directly to a comparator. The comparator compares the input waveform against the internal ECL threshold level to produce a digital signal with internal logic levels. The output of the signal detect comparator then goes to the link integrity and squelch blocks. If the signal detect input is asserted, the device is placed in the Link Pass state and the input data on FXI+/- is determined to be valid. If the signal detect input is deasserted, the device is placed in the Link Fail state and the input data on FXI+/- is determined to be invalid.

The SD_THR pin adjusts the ECL trip point of the SD/nFXDIS input. When the SD_THR pin is tied to a voltage between GND and GND+0.45V, the trip point of the SD/nFXDIS ECL input buffer is internally set to VDD-1.3V. When SD_THR pin is set to a voltage greater than GND+0.85v, the trip point of the SD/nFXDIS ECL input buffer is set to the voltage that is applied to the SD_THR pin. The trip level for the SD/nFXDIS input buffer must be set to VDD-1.3V. Having external control of the SD/nFXDIS buffer trip level with the SD_THR pin allows this trip level to be referenced to an external supply which facilitates connection to an external fiber optic transceiver. If the device is to be connected to a 3.3V external fiber optic transceiver, then SD_THR should be tied to GND. If the device is to be connected to a 5V external fiber optic transceiver, then SD_THR needs to be tied to VDD-1.3V, and this can be done so with an external resistor divider. Refer to the Applications section for more details on connections to external fiber optic transceivers.

FX Disable

The FX interface will be disabled if the SD/nFXDIS pin is tied to GND. Otherwise, the FX interface is enabled. Disabling the FX interface automatically enables the TP interface, and vice versa.

COLLISION

100 Mbps

Collision occurs whenever transmit and receive occur simultaneously while the device is in Half Duplex.

Collision is sensed whenever there is simultaneous transmission (packet transmission on TPO±) and reception (non idle symbols detected on TP input). When collision is detected, the COL output is asserted, TP data continues to be transmitted on twisted pair outputs, TP data continues to be received on twisted pair inputs, and internal CRS loopback is disabled. Once collision starts, CRS is asserted and stays asserted until the receive and transmit packets that caused the collision are terminated.

The collision function is disabled if the device is in the Full Duplex mode, is in the Link Fail state, or if the device is in the diagnostic loopback mode.

10 Mbps

Collision in 10 Mbps mode is identical to the 100 Mbps mode except, (1) reception is determined by the 10 Mbps squelch criteria, (2) RXD[3:0] outputs are forced to all 0's, (3) collision is asserted when the SQE test is performed, (4) collision is asserted when the jabber condition has been detected.

Collision Test

The controller interface collision signal, COL, can be tested by setting the collision test register bit in the MI serial port Control register. When this bit is set, TX_EN is looped back onto COL and the TP outputs are disabled.

Collision Indication

Collision can be programmed to appear on the nPLED2 pin by appropriately setting the programmable LED output select bits in the MI serial port

Configuration 2 register, as shown in Table 5. When the nPLED2 pin is programmed to be a collision detect output, this pin is asserted low for 100 mS every time a collision occurs. The nPLED2 output is open drain with pullup resistor and can drive an LED from VDd or can drive another digital input.

START OF PACKET

100 Mbps

Start of packet for 100 Mbps mode is indicated by a unique Start of Stream Delimiter (referred to as SSD). The SSD pattern consists of the two /J/K/ 5B symbols inserted at the beginning of the packet in place of the first two preamble symbols, as defined in IEEE 802.3 Clause 24 and shown in Figure 2.

The transmit SSD is generated by the 4B5B encoder and the /J/K/ symbols are inserted by the 4B4B encoder at the beginning of the transmit data packet in place of the first two 5B symbols of the preamble, as shown in Figure 2.

The receive pattern is detected by the 4B5B decoder by examining groups of 10 consecutive code bits (two 5B words) from the descrambler. Between packets, the receiver will be detecting the idle pattern, which is 5B /I/ symbols. While in the idle state, CRS and RX_DV are deasserted.

If the receiver is in the idle state and 10 consecutive code bits from the receiver consist of the /J/K/ symbols, the start of packet is detected, data reception is begun, CRS and RX_DV are asserted, and /5/5/ symbols are substituted in place of the /J/K/ symbols.

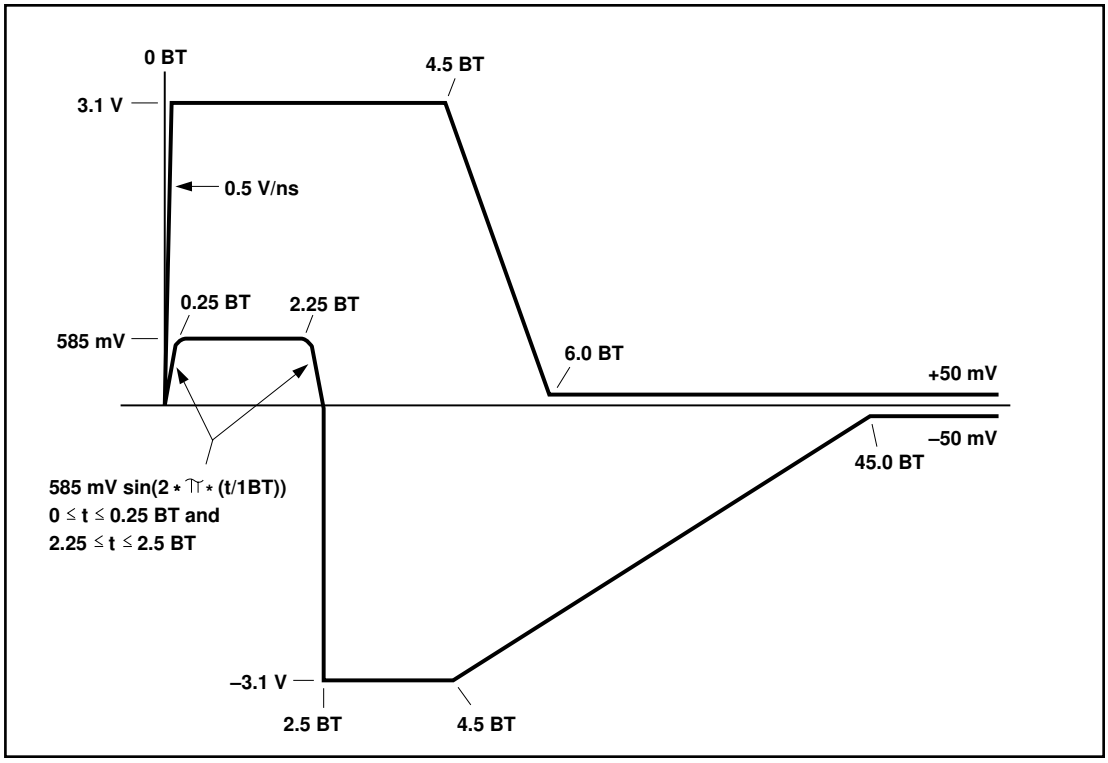


FIGURE 6 - SOI OUTPUT VOLTAGE TEMPLATE - 10 MBPS

If the receiver is in the idle state and 10 consecutive code bits from the receiver consist of a pattern that is neither /I/I/ nor /J/K/ symbols but contains at least 2 non contiguous 0's, then activity is detected but the start of packet is considered to be faulty and a False Carrier Indication (also referred to as bad SSD) is signalled to the controller interface. When False Carrier is detected, then CRS is asserted, RX_DV remains deasserted, RXD[3:0]=1110 while RX_ER is asserted, and the bad SSD bit is set in the MI serial port Status Output register. Once a False Carrier Event is detected, the idle pattern (two /I/I/ symbols) must be detected before any new SSD's can be sensed.

If the receiver is in the idle state and 10 consecutive code bits from the receiver consist of a pattern that is neither /I/I/ nor /J/K/ symbols but does not contain at least 2 non- contiguous 0's, the data is ignored and the receiver stays in the idle state.

10 Mbps

Since the idle period in 10 Mbps mode is defined to be the period when no data is present on the TP inputs, then the start of packet for 10 Mbps mode is detected when valid data is detected by the TP squelch circuit. When start of packet is detected, CRS is asserted as described in the Controller Interface section. Refer to the TP squelch section for 10 Mbps mode for the algorithm for valid data detection.

END OF PACKET

100 Mbps

End of packet for 100 Mbps mode is indicated by a the End of Stream Delimiter (referred to as ESD). The ESD pattern consists of the two /T/R/ 4B5B symbols inserted after the end of the packet, as defined in IEEE 802.3 Clause 24 and shown in Figure 2.

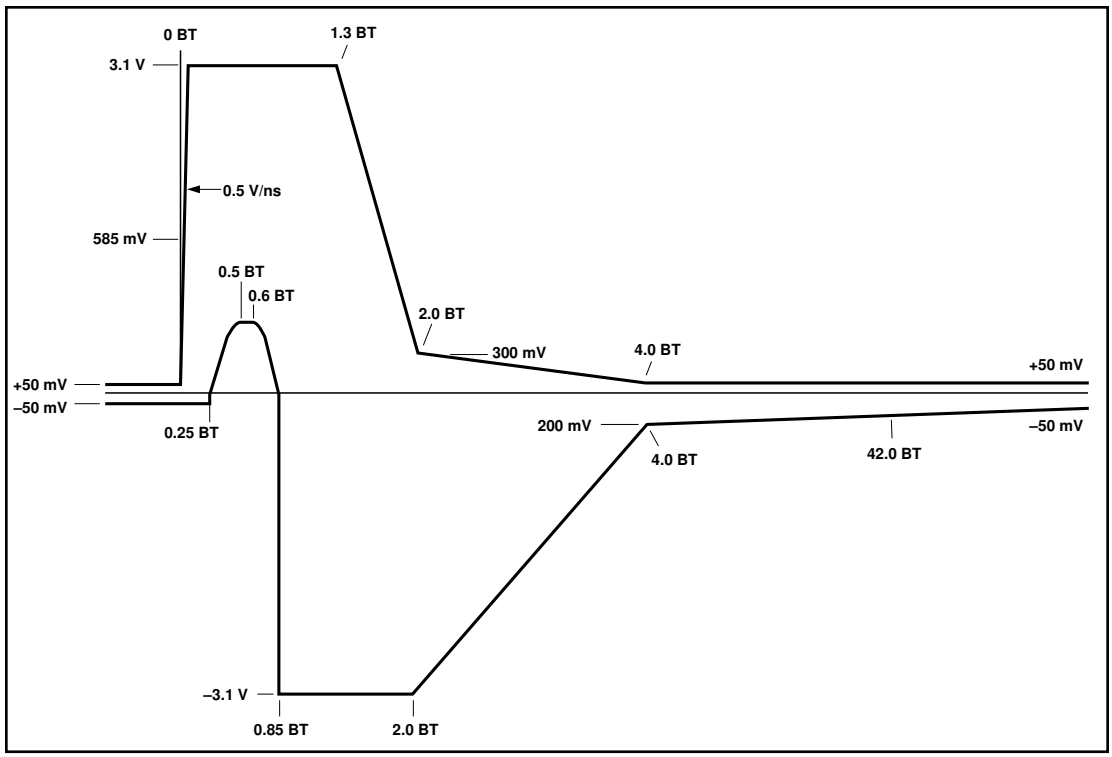


FIGURE 7 - LINK PULSE OUTPUT VOLTAGE TEMPLATE _ NLP, FLP

The transmit ESD is generated by the 4B5B encoder and the /T/R/ symbols are inserted by the 4B5B encoder after the end of the transmit data packet, as shown in Figure 2.

The receive ESD pattern is detected by the 4B5B decoder by examining groups of 10 consecutive code bits (two 5B words) from the descrambler during valid packet reception to determine if there is an ESD.

If the 10 consecutive code bits from the receiver during valid packet reception consist of the /T/R/ symbols, the end of packet is detected, data reception is terminated, CRS and RX_DV are asserted, and /I/I/ symbols are substituted in place of the /T/R/ symbols.

If 10 consecutive code bits from the receiver during valid packet reception do not consist of /T/R/ symbols but consist of /I/I/ symbols instead, then the packet is considered to have been terminated prematurely and abnormally. When this premature end of packet condition is detected, RX_ER is asserted for the nibble associated with the first /I/ symbol detected and then CRS and RX_DV are deasserted. Premature end of packet condition is also indicated by setting the bad ESD bit in the MI serial port Status Output register.

10 Mbps

The end of packet for 10 Mbps mode is indicated with the SOI (Start of Idle) pulse. The SOI pulse is a positive pulse containing a Manchester code violation inserted at the end of every packet .

The transmit SOI pulse is generated by the TP transmitter and inserted at the end of the data packet after TX_EN is deasserted. The transmitted SOI output pulse at the TP output is shaped by the transmit waveshaper to meet the pulse template requirements specified in IEEE 802.3 Clause 14 and shown in Figure 6.

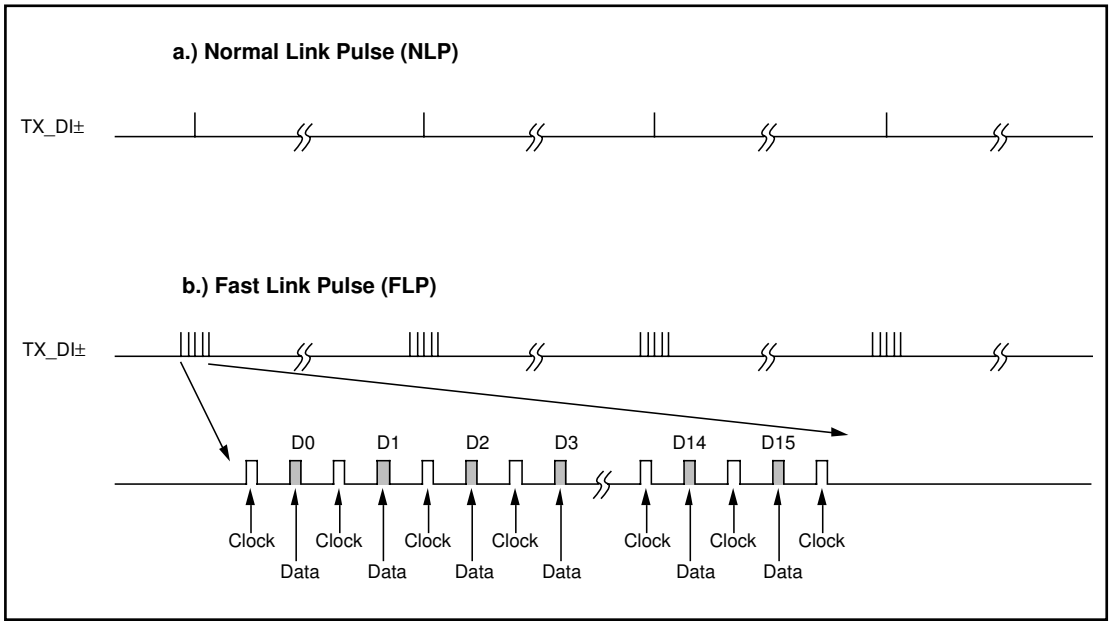


FIGURE 8 - NLP VS. FLP LINK PULSE

The receive SOI pulse is detected by the TP receiver by sensing missing data transitions. Once the SOI pulse is detected, data reception is ended and CRS and RX_DV are deasserted.

LINK INTEGRITY & AUTONEGOTIATION

General

The LAN83C183 can be configured to implement either the standard link integrity algorithms or the AutoNegotiation algorithm.

The standard link integrity algorithms are used solely to establish an active link to and from a remote device. There are different standard link integrity algorithms for 10 and 100 Mbps modes. The AutoNegotiation algorithm is used for two purposes: (1) To automatically configure the device for either 10/100 Mbps and Half/Full Duplex modes, and (2) to establish an active link to and from a remote device. The standard link integrity and AutoNegotiation algorithms are described below.

AutoNegotiation is only specified for 100BASE-TX and 10BASE-T operation and should be disabled when the device is placed in 100BASE-FX mode.

10BASE-T Link Integrity Algorithm - 10Mbps

The LAN83C183 uses the same 10BASE-T link integrity algorithm that is defined in IEEE 802.3 Clause 14. This algorithm uses normal link pulses, referred to as NLP's and transmitted during idle periods, to determine if a device has successfully established a link with a remote device (called Link Pass state). The transmit link pulse meets the template defined in IEEE 802.3 Clause 14 and shown in Figure 7. Refer to IEEE 802.3 Clause 14 for more details if needed.

100BASE-TX Link Integrity Algorithm -100Mbps

Since 100BASE-TX is defined to have an active idle signal, then there is no need to have separate link pulses like those defined for 10BASE-T. The LAN83C183 uses the squelch criteria and descrambler synchronization algorithm on the input data to determine if the device has successfully established a link with a remote device (called Link Pass state). Refer to IEEE 802.3 for both of these algorithms for more details.

AutoNegotiation Algorithm

As stated previously, the AutoNegotiation algorithm is used for two purposes: (1) To automatically configure the device for either 10/100 Mbps and Half/Full Duplex modes, and (2) to establish an active link to and from a remote device. The AutoNegotiation algorithm is the same algorithm that is defined in IEEE 802.3 Clause 28. AutoNegotiation uses a burst of link pulses, called fast link pulses and referred to as FLP's, to pass up to 16 bits of signaling data back and forth between the LAN83C183 and a remote device. The transmit FLP pulses meet the templated specified in IEEE 802.3 and shown in Figure 7. A timing diagram contrasting NLP's and FLP's is shown in Figure 8.

The AutoNegotiation algorithm is initiated by any of the following events: (1) Powerup, (2) device reset, (3) AutoNegotiation reset, (4) AutoNegotiation enabled, or (5) a device enters the Link Fail State. Once a negotiation has been initiated, the LAN83C183 first determines if the remote device has AutoNegotiation capability. If the remote device is not AutoNegotiation capable and is just transmitting either a 10BASE-T or 100BASE-TX signal, the LAN83C183 will sense that and place itself in the correct mode. If the LAN83C183 detects FLP's from the remote device, then the remote device is determined to have AutoNegotiation capability and the device then uses the contents of the MI serial port AutoNegotiation Advertisement register and FLP's to advertise its capabilities to a remote device. The remote device does the same, and the capabilities read back from the remote device are stored in the MI serial port AutoNegotiation Remote End Capability register. The LAN83C183 negotiation algorithm then matches it's capabilities to the remote device's capabilities and determines what mode the device should be configured to according to the priority resolution algorithm defined in IEEE 802.3 Clause 28. Once the negotiation process is completed, the LAN83C183 then configures itself for either 10 or

100 Mbps mode and either Full or Half Duplex modes (depending on the outcome of the negotiation process), and it switches to either the 100BASE-TX or 10BASE-T link integrity algorithms (depending on which mode was enabled by AutoNegotiation). Refer to IEEE 802.3 Clause 28 for more details.

AutoNegotiation Outcome Indication

The outcome or result of the AutoNegotiation process is stored in the speed detect and duplex detect bits in the MI serial port Status Output register.

AutoNegotiation Status

The status of the AutoNegotiation process can be monitored by reading the AutoNegotiation acknowledgement bit in the MI serial port Status register. The MI serial port Status register contains a single AutoNegotiation acknowledgement bit which indicates when an AutoNegotiation has been initiated and successfully completed.

AutoNegotiation Enable

The AutoNegotiation algorithm can be enabled (or restarted) by setting the AutoNegotiation enable bit in the MI serial port Control register or by asserting the ANEG pin. When the AutoNegotiation algorithm is enabled, the device halts all transmissions including link pulses for 1200-1500 mS, enters the Link Fail State, and restarts the negotiation process. When the AutoNegotiation algorithm is disabled, the selection of 100 Mbps or 10 Mbps modes is determined by the speed select bit in the MI serial port Control register, and the selection of Half or Full Duplex is determined by the duplex select bit in the MI serial port Control register.

AutoNegotiation Reset

The AutoNegotiation algorithm can be initiated at any time by setting the AutoNegotiation reset bit in the MI serial port Control register.

Link Indication

Receive link detect activity can be monitored through the link detect bit in the MI serial port Status and Status Output registers or it can also be programmed to appear on the nPLED3 or nPLED0 pin by appropriately setting the programmable LED output select bits in the MI serial port Configuration 2 register as shown in Table 5. When either the nPLED3 or nPLED0 pins are programmed to be a link detect output, these pins are asserted low whenever the device is in the Link Pass State. The nPLED3 output is open drain with pullup resistor and can drive an LED from VDD; The nPLED0 output has both pullup and pulldown driver transistors in addition to a weak pullup resistor, so it can drive an LED from either VDD or GND. Both nPLED3 and nPLED0 can also drive another digital input. Refer to the LED Driver Section (3.23) for a description on how to program the nPLED[3:0] pins and their defaults.

Link Disable

The link integrity function can be disabled by setting the link disable bit in the MI serial port Configuration 1 register. When the link integrity function is disabled, the device is forced into the Link Pass state, configures itself for Half/Full Duplex based on the value of the duplex bit in the MI serial port Control register, configures itself for 100/10 Mbps operation based on the values of the speed bit in the MI serial port Control register, and continues to transmit NLP's or TX idle patterns, depending on whether the device is in 10 or 100 Mbps mode.

JABBER

100 Mbps

Jabber function is disabled in the 100 Mbps mode.

10 Mbps

Jabber condition occurs when the transmit packet exceeds a predetermined length. When jabber is detected, the TP transmit outputs are forced to the idle state, collision is asserted, and register bits in the MI serial port Status and Status Output registers are set.

Jabber Disable

The jabber function can be disabled by setting the jabber disable bit in the MI serial port Configuration 2 register.

RECEIVE POLARITY CORRECTION

100 Mbps

No polarity detection or correction is needed in 100 Mbps mode.

10 Mbps

The polarity of the signal on the TP receive input is continuously monitored. If either 3 consecutive link pulses or one SOI pulse indicates incorrect polarity on the TP receive input, the polarity is internally determined to be incorrect, and a reverse polarity bit is set in the MI serial port Status Output register.

The LAN83C183 will automatically correct for the reverse polarity condition provided that the autopolarity feature is not disabled.

Autopolarity Disable

The autopolarity feature can be disabled by setting the autopolarity disable bit in the MI serial port Configuration 2 register.

FULL DUPLEX MODE

100 Mbps

Full Duplex mode allows transmission and reception to occur simultaneously. When Full Duplex mode is enabled, collision is disabled and internal TX_EN to CRS loopback is disabled.

The device can be either forced into Half or Full Duplex mode, or the device can detect either Half or Full Duplex capability from a remote device and automatically place itself in the correct mode.

The device can be forced into the Full or Half Duplex modes by either setting the duplex bit in the MI serial port Control register or by asserting the nDPLX pin assuming AutoNegotiation is not enabled.

The device can automatically configure itself for Full or Half Duplex modes by using the AutoNegotiation algorithm to advertise and detect Full and Half Duplex capabilities to and from a remote terminal. All of this is described in detail in the Link Integrity and AutoNegotiation section.

10 Mbps

Full Duplex in 10 Mbps mode is identical to the 100 Mbps mode.

Full Duplex Indication

Full Duplex detection can be monitored through the duplex bit in the MI serial port Status Output register, or it can also be programmed to appear on the nPLED1 pin by appropriately setting the programmable LED output select bits in the MI serial port Configuration 2 register as described in Table 5. When the nPLED1 pin is programmed to be a Full Duplex detect output, this pin is asserted low when the device is configured for Full Duplex operation. The nPLED1 output has both pullup and pulldown driver transistors and a weak pullup resistor, so it can drive an LED from either VDD or GND and can also drive a digital input.

100/10 MBPS SELECTION

General

The device can be forced into either the 100 or 10 Mbps mode, or the device also can detect 100 or 10 Mbps capability from a remote device and automatically place itself in the correct mode.

The device can be forced into either the 100 or 10 Mbps mode by setting the speed select bit in the MI serial port Control register or by appropriately asserting the SPEED pin assuming AutoNegotiation is not enabled.

The device can automatically configure itself for 100 or 10 Mbps mode by using the AutoNegotiation algorithm to advertise and detect 100 and 10 Mbps capabilities to and from a remote terminal. All of this is described in detail in the Link Integrity & AutoNegotiation section.

10/100 Mbps Indication

The device speed (100/10 Mbps) can be determined through the speed bit in the MI serial port Status Output register, or it can also be programmed to appear on the nPLED0 pin by setting the programmable LED output select bits in the MI serial port Configuration 2 register. When the nPLED0 pin is programmed to be speed detect output, this pin is asserted low when the device is configured for 100 Mbps operation. The nPLED0 output has both pullup and pulldown driver transistors and a weak pullup resistor, so it can drive an LED from either VDD or GND and can also drive a digital input.

LOOPBACK

Internal CRS Loopback

TX_EN is internally looped back onto CRS during every transmit packet. This internal CRS loopback is disabled during collision, in Full Duplex mode, in Link Fail State, and when the transmit disable bit is set in the MI serial port Configuration 1 register. In 10 Mbps mode, internal CRS loopback is also disabled when jabber is detected.

The internal CRS loopback can be disabled by setting the TX_EN to CRS loopback disable bit in the MI serial port Configuration 1 register. When this bit is set, TX_EN is no longer looped back to CRS.

Diagnostic Loopback

A diagnostic loopback mode can also be selected by setting the loopback bit in the MI serial port Control register. When diagnostic loopback is enabled, TXD[3:0] data is looped back onto RXD[3:0], TX_EN is looped back onto CRS, RX_DV operates normally, the TP receive and transmit paths are disabled, the transmit link pulses are halted, and the Half/Full Duplex modes do not change. Diagnostic loopback mode can not be enabled when the FBI interface is selected.

AUTOMATIC JAM

100 Mbps

The LAN83C183 has an automatic JAM feature which will cause the device to automatically transmit a JAM packet if receive activity is detected. If automatic JAM is enabled, then the following JAM packet will be transmitted on TPO± when the JAM pin is asserted active low and receive activity is detected on TP inputs (expressed in 5B code words):

/J/K/5/5/5/5/5/5/5/5/5/5/5/5/D/H/H/H/H/H/H/H/T/R/

This automatic nJAM feature is enabled when the RX_EN/nJAM pin is programmed to be a nJAM input. RX_EN/nJAM can be configured to be a nJAM input by appropriately setting the R/J configuration bit in the MI serial port Configuration 2 register.

10 Mbps

The JAM feature for 10 Mbps mode is identical to 100 Mbps mode except: (1) the JAM packet transmitted on TPO± is composed of standard 62 bit preamble (alternating 1,0) followed by SFD (11) followed by 32 bits of alternating 1,0 pattern.

RESET

The device is reset when either (1) VDD is applied to the device, (2) the reset bit is set in the MI serial port Control register, or (3) the nRESET pin is asserted active low. When reset is initiated by (1) or (2), an internal power-on reset pulse is generated which resets all internal circuits, forces the MI serial port bits to their default values, and latches in new values for the MI address. After the power-on reset pulse has finished, the reset bit in the MI serial port Control register is cleared and the device is ready for normal operation. When reset is initiated by (3), the same procedure occurs except the device stays in the reset state as long as the nRESET pin is held low. The nRESET pin has an internal pullup to VDD. The device is guaranteed to be ready for normal operation 50 mS after the reset was initiated.

POWERDOWN

The LAN83C183 can be powered down by setting the powerdown bit in the MI serial port Control register. In powerdown mode, the TP outputs are in

high impedance state, all functions are disabled except the MI serial port, and the power consumption is reduced to a minimum. The device is guaranteed to be ready for normal operation 500 mS after powerdown is deasserted.

OSCILLATOR

The LAN83C183 requires a 25 Mhz reference frequency for internal signal generation. This 25 Mhz reference frequency is generated by either connecting an external 25 MHz crystal between OSCIN and GND or by applying an external 25Mhz clock to OSCIN.

LED DRIVERS

The nPLED[5:2] outputs are open drain with a pullup resistor and can drive LED's tied to VDD. The nPLED[1:0] outputs have both pullup and pulldown driver transistors with a pullup resistor, so nPLED[1:0] can drive LED's tied to either VDD or GND.

The nPLED[5:0] outputs can be programmed through the MI serial port to do 4 different functions: (1) Normal Function (2) On, (3) Off, and (4) Blink. nPLED[5:0] can be programmed with the LED output select bits and the LED Normal Function select bits in the MI serial port Configuration 2 register.

When nPLED[5:0] are programmed for their Normal Functions, these outputs indicate specific events. There are four sets of specific events that these outputs can indicate, and they are described in Tables 5 and 6. The selection of which set of events that these outputs indicate is determined by appropriately setting the LED Normal Function select bits in the MI serial port Configuration 2 register. The default Normal Functions for nPLED[5:0] are Transmit Activity, Receive Activity, Link 100, Activity, Full Duplex, and Link 10, respectively.

When nPLED[3:0] is programmed to be On, the LED output driver go low, thus turning on the LED under user control.

When nPLED[3:0] is programmed to be Off, the LED output driver will turn off, thus turning off the LED under user control. When nPLED[3:0] is programmed to Blink, the LED output driver will continuously blink at a rate of 100 mS on, 100 mS off.

Table 5 - LED Normal Function Definition

BITS 17.7-6	nPLED5	nPLED4	nPLED3	nPLED2	nPLED1	nPLED0
11	RCV ACT	XMT ACT	LINK	COL	FDX	10/100
10	RCV ACT	XMT ACT	LINK	ACT	FDX	10/100
01	RCV ACT	XMT ACT	LINK + ACT	COL	FDX	10/100
00	RCV ACT	XMT ACT	LINK 100	ACT	FDX	LINK10

Device powers up with default set to 00.

Table 6 - LED Event Definition

SYMBOL	DEFINITION
XMT ACT	Transmit Activity Occurred, Stretch Pulse to 100 mS
RCV ACT	Receive Activity Occurred, Stretch Pulse to 100 mS
ACT	Activity Occurred, Stretch Pulse to 100 mS
COL	Collision Occurred, Stretch Pulse to 100 mS
LINK100	100 Mb Link Detected
LINK10	10 Mb Link Detected
LINK	100 or 10 Mb Link Detected
LINK+ACT	100 or 10 Mb Link Detected or Activity Occurred, Stretch Pulse To 100 mS (Link Detect Causes LED to be On, Activity Causes LED to Blink)
FDX	Full Duplex Mode Enabled
10/100	10 Mb Mode Enabled (High), or 100 Mb Mode Enabled (Low)

REPEATER MODE

The LAN83C183 has one predefined repeater mode which can be enabled by asserting the RPTR pin. When this repeater mode is enabled with the RPTR pin, the device operation is altered as follows: (1) TX_EN to CRS loopback is disabled, (2) AutoNegotiation is disabled, (3) 100 Mbps operation is enabled, and (4) Half Duplex operation is enabled. Note that the repeater mode enabled by the RPTR pin is only one of many possible repeater modes available on the device; other repeater modes are available by setting the appropriate register bits to enable or disable the desired functions for a given repeater mode type. See the Repeater Applications Section (5.10.2) for more details on other possible repeater modes.

MI SERIAL PORT

Signal Description

The MI serial port has eight pins, MDC, MDIO, nMDINT, and nMDA[4:0]. MDC is the serial shift clock input. MDIO is a bidirectional data I/O pin. nMDINT is an interrupt output. nMDA[4:0] are address pins for the MI serial port.

nMDA[4:0] inputs share the same pins as the nMDINT and nPLED[3:0] outputs, respectively. At powerup or reset, the nPLED[3:0] and nMDINT output drivers are tristated for an interval called the power-on reset time. During the power-on reset interval, the value on these pins is latched into the device, inverted, and used as the MI serial port physical device addresses.

Timing

A timing diagram for a MI serial port frame is shown in Figure 9. The MI serial port is idle when at least 32 continuous 1's are detected on MDIO and remains idle as long as continuous 1's are detected. During idle, MDIO is in the high impedance state. When the MI serial port is in the idle state, a 01 pattern on the MDIO pin initiates a serial shift cycle. Data on MDIO is then shifted in on the next 14 rising edges of MDC (MDIO is high impedance). If the register access mode is not enabled, on the next 16 rising edges of MDC, data is either shifted in or out on MDIO, depending on whether a write or read cycle was selected with the bits READ and WRITE. After the 32 MDC cycles have been completed, one complete register has been read/written, the serial shift process is halted, data is latched into the device, and MDIO goes into high impedance state. Another serial shift cycle cannot be initiated until the idle condition (at least 32 continuous 1's) is detected.

Multiple Register Access

Multiple registers can be accessed on a single MI serial port access cycle with the multiple register access feature. The multiple register access feature can be enabled by setting the multiple register access enable bit in the MI serial port Configuration 2 register. When multiple register access is enabled, multiple registers can be accessed on a single MI serial port access cycle by setting the register address to 11111 during the first 16 MDC clock cycles. There is no actual register residing in register address location 11111, so when the register address is then set to 11111, all eleven registers are accessed on the 176 rising edges of MDC that occur after the first 16 MDC clock cycles of the MI serial port access cycle. The registers are accessed in numerical order from 0 to 20. After all 192 MDC clocks have been completed, all the registers have been read/written, and the serial shift process is halted, data is latched into the device, and MDIO goes into high impedance state. Another serial shift cycle cannot be initiated until the idle condition (at least 32 continuous 1's) is detected.

Bit Types

Since the serial port is bidirectional, there are many types of bits. Write bits (W) are inputs during a write cycle and are high impedance during a read cycle. Read bits (R) are outputs during a read cycle and high impedance during a write cycle. Read/Write bits (R/W) are actually write bits which can be read out during a read cycle. R/WSC bits are R/W bits that are self clearing after a set period of time or after a specific event has completed. R/LL bits are read bits that latch themselves when they go low, and they stay latched low until read. After they are read, they are reset high. R/LH bits are the same as R/LL

bits except that they latch high. R/LT are read bits that latch themselves whenever they make a transition or change value, and they stay latched until they are read. After R/LT bits are read, they are updated to their current value. R/LT bits can also be programmed to assert the interrupt function as described in the Interrupt section. The bit type definitions are summarized in Table 7.

Table 7 - MI Register Bit Type Definition

SYM.	NAME	DEFINITION	
		WRITE CYCLE	READ CYCLE
W	Write	Input	No Operation, Hi Z
R	Read	No Operation, Hi Z	Output
R/W	Read/ Write	Input	Ouput
R/ WSC	Read/ Write Self Clearing	Input	Ouput Clears Itself After Operation Completed
R/LL	Read/ Latching Low	No Operation, Hi Z	Output When Bit Goes Low, Bit Latched. When Bit Is Read, Bit Updated.
R/LH	Read/ Latching High	No Operation, Hi Z	Output When Bit Goes High, Bit Latched. When Bit Is Read, Bit Updated.
R/LT	Read/ Latching on Transition	No Operation, Hi Z	Output When Bit Transitions, Bit Latched And Interrupt Set When Bit Is Read, Interrupt Cleared And Bit Updated.

Frame Structure

The structure of the serial port frame is shown in Table 8 and a timing diagram of a frame is shown in Figure 9. Each serial port access cycle consists of 32 bits (or 192 bits if multiple register access is enabled and REGAD[4:0]=11111), exclusive of idle. The first 16 bits of the serial port cycle are always write bits and are used for addressing. The last 16/ 176 bits are from one/all of the 11 data registers.

The first 2 bits in Table 8 and Figure 9 are start bits and need to be written as a 01 for the serial port cycle to continue. The next 2 bits are a read and write bit which determine if the accessed data register bits will be read or write. The next 5 bits are device addresses and they must match the inverted values latched in from pins nMDA[4:0] during the power-on reset time for the serial port access to continue. The next 5 bits are register address select bits which select one of the five data registers for access. The next 1 bit is a turnaround bit which is not an actual register bit but extra time to switch MDIO from write to read if necessary, as shown in Figure 2. The final 16 bits of the MI serial port cycle (or 176 bits if multiple register access is enabled and REGAD[4:0]=11111) come from the specific data register designated by the register address bits REGAD[4:0].

Register Structure

The LAN83C183 has eleven internal 16 bit registers. Ten registers are available for setting configuration inputs and reading status outputs, and one register is reserved for factory use. A map of the registers is shown in Table 9. The ten accessible registers consist of six registers that are defined by IEEE 802.3 specifications (Registers 0-5) and four registers that are unique to the LAN83C183 (Registers 16-19).

The structure and bit definition of the Control register is shown in Table 10. This register stores various configuration inputs and its bit definition complies with the IEEE 802.3 specifications.

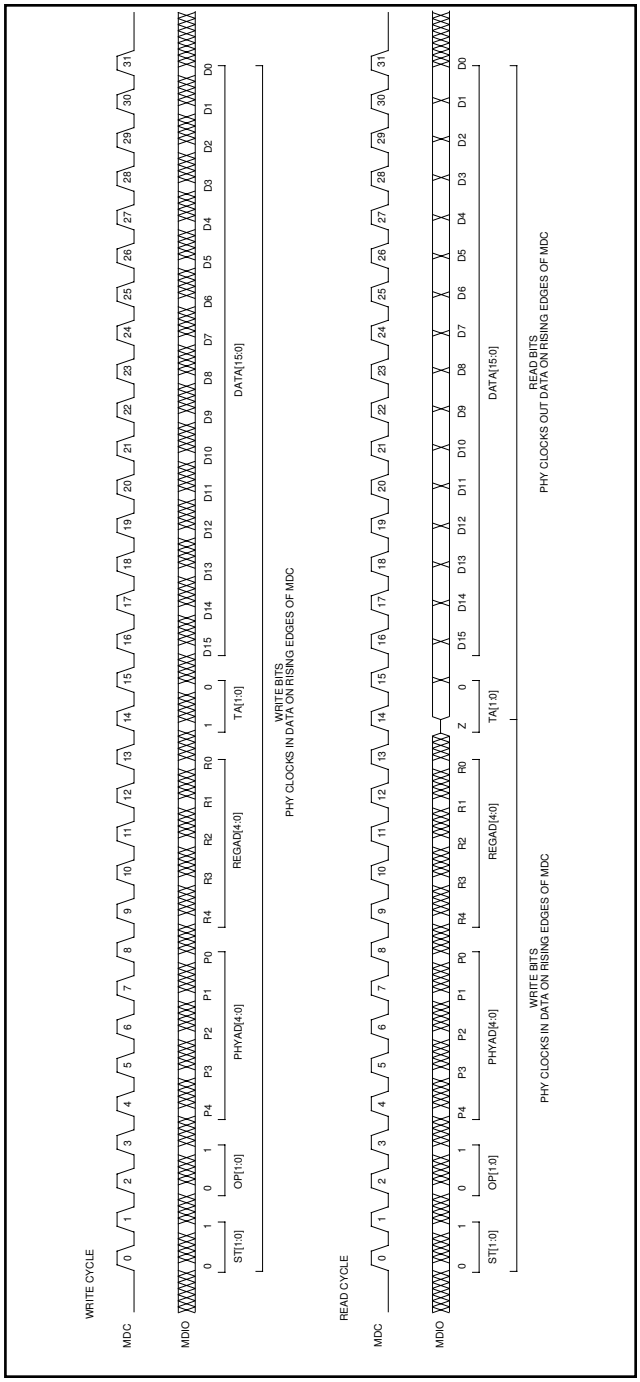


FIGURE 9 - MII SERIAL PORT FRAME TIMING DIAGRAM

The structure and bit definition of the Status register is shown in Table 11. This register contains device capabilities and status output information. and its bit definition complies with the IEEE 802.3 specifications.

The structure and bit definition of the PHY ID #1 and #2 registers is shown in Tables 12 and 13, respectively. These registers contain an identification code unique to the LAN83C183 and their bit definition complies with the IEEE 802.3 specifications.

The structure and bit definition of the AutoNegotiation Advertisement and AutoNegotiation Remote End Capability registers is shown in Tables 14 and 15, respectively. These registers are used by the AutoNegotiation algorithm and their bit definition complies with the IEEE 802.3 specifications.

The structure and bit definition of the Configuration 1 and Configuration 2 registers is shown in Table 16 and 17, respectively. These registers store various configuration inputs.

The structure and bit definition of the Status Output register is shown in Table 18. This register contains output status information.

The structure and bit definition of the Mask register is shown in Table 19. This register allows each R/LT bit in the Status Output register to be masked out or removed as a bit that will set interrupt.

Register 20 is reserved for factory use. All bit values must be set to the defaults for normal operation.

Interrupt

The LAN83C183 has hardware and software interrupt capability. The interrupt is triggered by certain output status bits (also referred to as interrupt bits) in the serial port. As indicated previously, R/LT bits are read bits that latch on transition. R/LT bits are also interrupt bits if they are not masked out with the Mask register bits. Interrupt bits automatically latch themselves into their register locations and assert the interrupt indication when they change state. Interrupt bits stay latched until they are read. When interrupt bits are read, the interrupt indication is deasserted and the interrupt bits that caused the interrupt to happen are updated to their current value. Each interrupt bit can be individually masked and subsequently be removed as an interrupt bit by setting the appropriate mask register bits in the Mask register.

Interrupt indication is done in three ways: (1) nMDINT pin, (2) INT bit in the MI serial port Status Output register, and (3) interrupt pulse on MDIO. The nMDINT pin is an active low interrupt output indication. The INT bit is an active high interrupt register bit that resides in the Status Output register. The interrupt pulse on MDIO also indicates interrupt and is available when the interrupt pulse select bit is set in the MI serial port Configuration 2 register. When this bit is set, an interrupt is signalled by an low going pulse on MDIO when MDC is high and the serial port is in the idle state, as shown in the timing diagram in Figure 10. Once MDIO is forced low to indicate the interrupt condition, MDIO stays low until MDC returns low. Once MDC returns low, then MDIO goes back to high impedance state. If the interrupt occurs while the serial port is being accessed, then the MDIO interrupt pulse is delayed until one clock bit after the serial port access cycle is ended as shown in Figure 10.

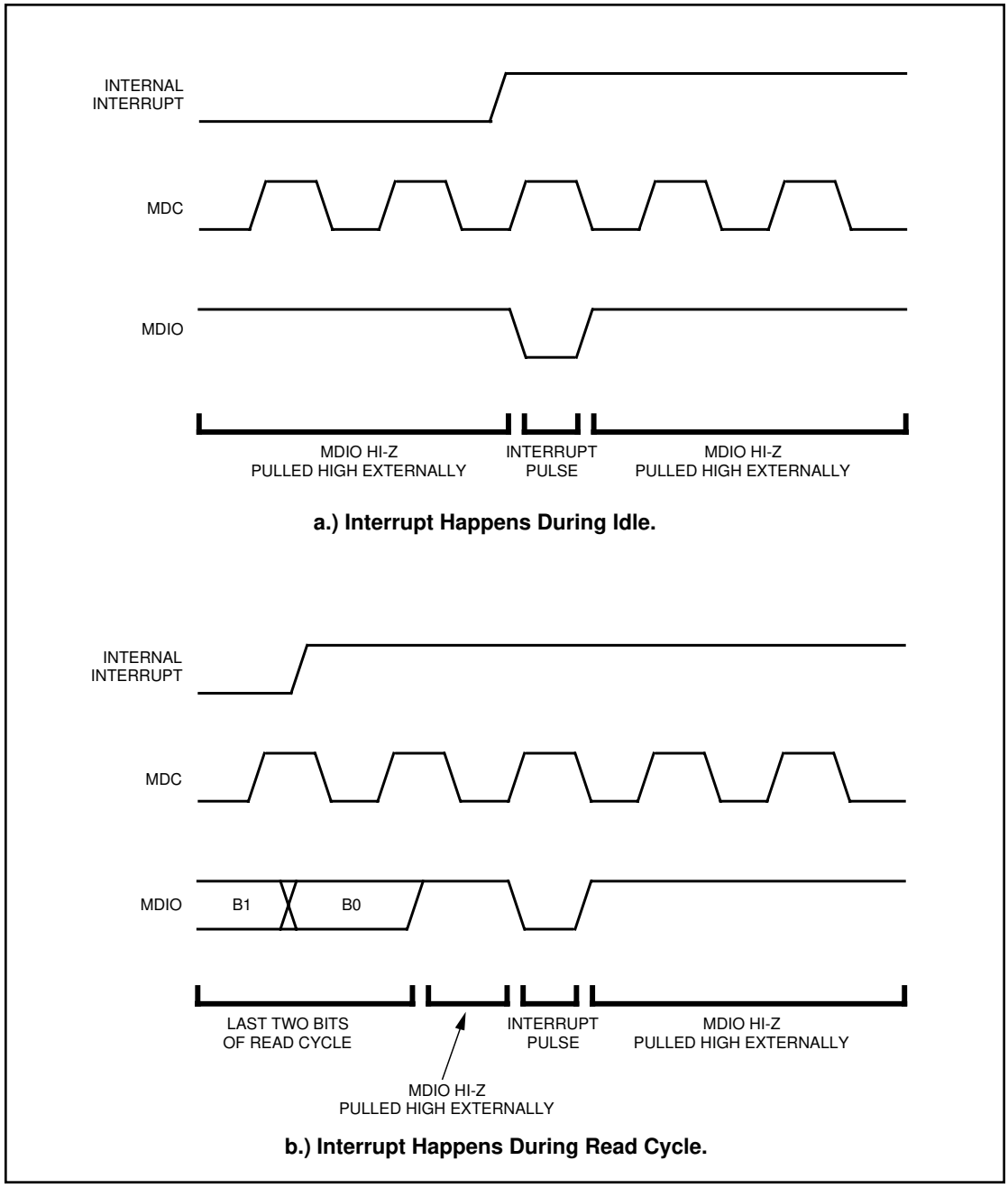
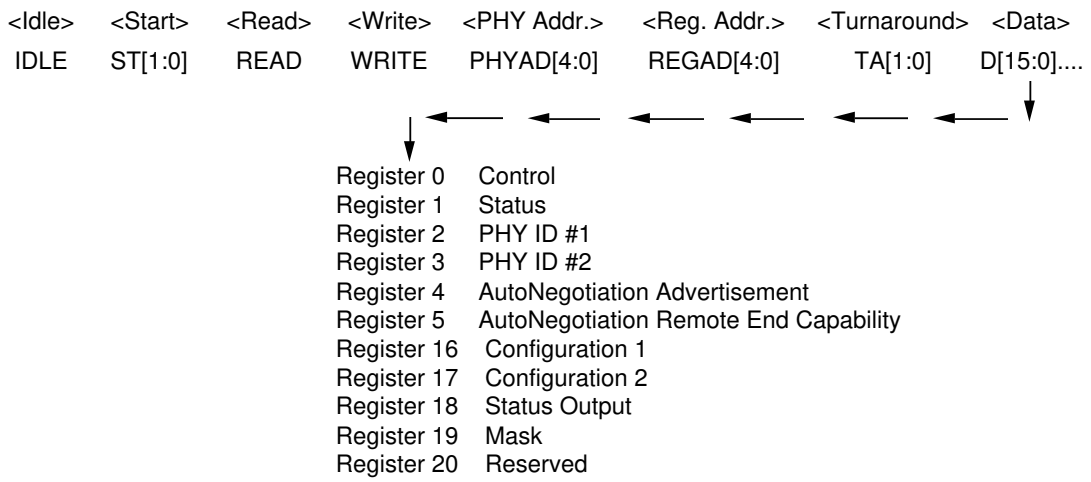


FIGURE 10 - MDIO INTERRUPT PULSE

Table 8 - MI Serial Port Frame Structure



SYMBOL	NAME	DEFINITION	R/W
IDLE	Idle Pattern	These bits are an idle pattern. Device will not initiate an MI cycle until it detects at least 32 1's.	W
ST1 ST0	Start Bits	When ST[1:0]=01, a MI Serial Port access cycle starts.	W
READ	Read Select	1 = Read Cycle	W
WRITE	Write Select	1 = Write Cycle	W
PHYAD[4:0]	Physical Device Address	When PHYAD[4:0]=nMDA[4:0] pins inverted, the MI Serial Port is selected for operation.	W
REGAD4[4:0]	Register Address	If REGAD[4:0]=00000-11110, these bits determine the specific register from which D[15:0] is read/written. If multiple register access is enabled and REGAD[4:0]=11111, all registers are read/written in a single cycle.	W
TA1 TA0	Turnaround Time	These bits provide some turnaround time for MDIO When READ=1, TA[1:0]=Z0 When WRITE=1, TA[1:0]=ZZ	R/W
D[15:0]....	Data	These 16 bits contain data to/from one of the eleven registers selected by register address bits REGAD[4:0].	Any

IDLE is shifted in first

TABLE 9 - MII SERIAL PORT REGISTER MAP

	x.15	x.14	x.13	x.12	x.11	x.10	x.9	x.8	x.7	x.6	x.5	x.4	x.3	x.2	x.1	x.0
0 Control	RST	LPBK	SPEED	ANEG_EN	PDN	MII_DIS	ANEG_RST	DPLX	COLTST	0	0	0	0	0	0	0
	R/WSC	R/W	R/W	R/W	R/W	R/W	R/WSC	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	0	0	1	1	0	1 or 0	0	0	0	0	0	0	0	0	0	0
1 Status	CAP_T4	CAP_TXF	CAP_TXH	CAP_TF	CAP_TH	0	0	0	0	0	ANEG_ACK	REM_FLT	CAP_ANEG	LINK	JAB	EXREG
	R	R	R	R	R	R	R	R	R	R	R	R/LH	R	R/LL	R/LH	R
	0	1	1	1	1	0	0	0	0	0	0	0	1	0	0	1
2 PHY ID #1	OUI3	OUI4	OUI5	OUI6	OUI7	OUI8	OUI9	OUI10	OUI11	OUI12	OUI13	OUI14	OUI15	OUI16	OUI17	OUI18
	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0
3 PHY ID #2	OUI19	OUI20	OUI21	OUI22	OUI23	OUI24	PART5	PART4	PART3	PART2	PART1	PART0	REV3	REV2	REV1	REV0
	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
	1	1	1	1	1	0	0	0	0	0	1	1	0	0	0	0
4 AutoNegot. Advertisement	NP	ACK	RF	0	0	0	T4	TX_FDX	TX_HDX	10_FDX	10_HDX	0	0	0	0	CSMA
	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0	1
5 AutoNegot. Remote Capability	NP	ACK	RF	0	0	0	T4	TX_FDX	TX_HDX	10_FDX	10_HDX	0	0	0	0	CSMA
	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
16 Configuration 1	LNK_DIS	XMT_DIS	XMT_PDN	TXEN_CRS	BYP_ENC	BYP_SCR	0	EQLZR	CABLE	RLVL0	TLVL3	TLVL2	TLVL1	TLVL0	TRF1	TRF0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0
17 Configuration 2	PLED3_1	PLED3_0	PLED2_1	PLED2_0	PLED1_1	PLED1_0	PLED0_1	PLED0_0	LED_DEF1	LED_DEF0	APOL_DIS	JAB_DIS	MREG	INT_MDIO	P26_CFG	0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
18 Status Output	INT	LNK_FAIL	LOSS_SYNC	CWRD	SSD	ESD	RPOL	JAB	SPD_DET	DPLX_DET	ANEG_ST1	ANEG_ST2	0	0	0	0
	R	R/LT	R/LT	R/LT	R/LT	R/LT	R/LT	R/LT	R/LT	R/LT	R/LT	R/LT	R	R	R	R
	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0
19 Mask	MASK_ INT	MASK_ LNK_FAIL	MASK_ LOSS_SYNC	MASK_ CWRD	MASK_ SSD	MASK_ ESD	MASK_ RPOL	MASK_ JAB	MASK_ SPD_DET	MASK_ DPLX_DET	MASK_ ANEG_ST1	MASK_ ANEG_ST2	1	1	1	1
		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
		1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
20 Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 10 - MI Register 0 (Control) Structure And Bit Definition

0.15	0.14	0.13	0.12	0.11	0.10	0.9	0.8
RST	LPBK	SPEED	ANEG_EN	PDN	MII_DIS	ANEG_RST	nDPLX
R/WSC	R/W	R/W	R/W	R/W	R/W	R/WSC	R/W
0.7	0.6	0.5	0.4	0.3	0.2	0.1	0.0
COLTST	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

BIT	SYMBOL	NAME	DEFINITION	R/W	DEF.
0.15	RST	Reset	1 = Reset, Bit Self Clearing After Reset Completed 0 = Normal	R/W SC	0
0.14	LPBK	Loopback Enable	1 = Loopback Mode Enabled 0 = Normal	R/W	0
0.13	SPEED	Speed Select	1 = 100 Mbps Selected (100BaseTX) 0 = 10 Mbps Selected (10BASE-T) NOTE: This Bit can be Overriden with SPEED Pin	R/W	1
0.12	ANEG_EN	AutoNegotiation Enable	1 = AutoNegotiation Enabled 0 = Normal NOTE: This Bit can be Overriden with ANEG Pin	R/W	1
0.11	PDN	Powerdown Enable	1 = Powerdown 0 = Normal	R/W	0
0.10	MII_DIS	MII Interface Disable	1 = MII Interface Disabled 0 = Normal	R/W	1[1]
0.9	ANEG_RST	AutoNegotiation Reset	1 = Restart AutoNegotiation Process, Bit Self Clearing After Reset Completed 0 = Normal	R/W SC	0
0.8	nDPLX	Duplex Mode Select	1 = Full Duplex 0 = Half Duplex NOTE: This Bit can be Overriden with nDPLX Pin	R/W	0
0.7	COLTST	Collision Test Enable	1 = Collision Test Enabled 0 = Normal	R/W	0
0.6 thru 0.0	Reserved	Reserved	Reserved	R/W	0

x.15 Bit Is Shifted First

Note 1: If nMDA[4:0] not = 11111, then the MII_DIS default value is changed to 0

Table 11 - MI Register 1 (Status) Structure And Bit Definition

1.15	1.14	1.13	1.12	1.11	1.10	1.9	1.8
CAP_T4	CAP_TXF	CAP_TXH	CAP_TF	CAP_TH	0	0	0
R	R	R	R	R	R	R	R

1.7	1.6	1.5	1.4	1.3	1.2	1.1	1.0
0	CAP_SUPR	ANEG_ACK	REM_FLT	CAP_ANEG	LINK	JAB	EXREG
R	R	R	R/LH	R	R/LL	R/LH	R

BIT	SYMBOL	NAME	DEFINITION	R/W	DEF.
1.15	CAP_T4	100BASE-T4 Capable	0 = Not Capable of 100BASE-T4 Operation	R	0
1.14	CAP_TXF	100BASE-TX Full Duplex Capable	1 = Capable Of 100BASE-TX Full Duplex	R	1
1.13	CAP_TXH	100BASE-TX Half Duplex Capable	1 = Capable Of 100BASE-TX Half Duplex	R	1
1.12	CAP_TF	10BASE-T Full Duplex Capable	1 = Capable Of 10BASE-T Full Duplex	R	1
1.11	CAP_TH	10BASE-T Half Duplex Capable	1 = Capable Of 10BASE-T Half Duplex	R	1
1.10 thru 1.7	Reserved	Reserved	Reserved	R	0
1.6	CAP_SUPR	MI Preamble Suppression Capable	0 = Not Capable of Accepting MI Frames with MI Preamble Suppressed	R	0
1.5	ANEG_ACK	AutoNegotiation Acknowledgment	1 = AutoNegotiation Acknowledgement Process Complete 0 = Normal	R	0
1.4	REM_FLT	Remote Fault Detect	1 = Remote Fault Detected. This bit is set when Either Interrupt Detect Bit 18.15 or AutoNegotiation Remote Fault Bit 5.13 is set. 0 = No Remote Fault	R/LH	0
1.3	CAP_ANEG	AutoNegotiation Capable	1 = Capable of AutoNegotiation Operation	R	1
1.2	LINK	Link Status	1 = Link Detected (Same As Bit 18.14 Inverted) 0 = Link Not Detected	R/LL	0
1.1	JAB	Jabber Detect	1 = Jabber Detected (Same As Bit 18.8) 0 = Normal	R/LH	0
1.0	EXREG	Extended Register Capable	1 = Extended Registers Exist	R	1

x.15 Bit Is Shifted First

Table 12 - MI Register 2 (PHY ID #1) Structure And Bit Definition

2.15	2.14	2.13	2.12	2.11	2.10	2.9	2.8
OUI3	OUI4	OUI5	OUI6	OUI7	OUI8	OUI9	OUI10
R	R	R	R	R	R	R	R
2.7	2.6	2.5	2.4	2.3	2.2	2.1	2.0
OUI11	OUI12	OUI13	OUI14	OUI15	OUI16	OUI17	OUI18
R	R	R	R	R	R	R	R

BIT	SYMBOL	NAME	DEFINITION	R/W	DEF.
2.15	OUI3	Company ID,	OUI = 00-A0-7D	R	0
2.14	OUI4	Bits 3-18			0
2.13	OUI5				0
2.12	OUI6				0
2.11	OUI7				0
2.10	OUI8				0
2.9	OUI9				0
2.8	OUI10				0
2.7	OUI11				0
2.6	OUI12				0
2.5	OUI13				0
2.4	OUI14				1
2.3	OUI15				0
2.2	OUI16				1
2.1	OUI17				1
2.0	OUI18				0

x.15 Bit Is Shifted First

Table 13 - MI Register 3 (PHY ID #2) Structure And Bit Definition

3.15	3.14	3.13	3.12	3.11	3.10	3.9	3.8
OUI19	OUI20	OUI21	OUI22	OUI23	OUI24	PART5	PART4
R	R	R	R	R	R	R	R
3.7	3.6	3.5	3.4	3.3	3.2	3.1	3.0
PART3	PART2	PART1	PART0	REV3	REV2	REV1	REV0
R	R	R	R	R	R	R	R

BIT	SYMBOL	NAME	DEFINITION	R/W	DEF.
3.15	OUI19	Company ID, Bits 19-24	OUI = 00-A0-7D	R	1
3.14	OUI20				1
3.13	OUI21				1
3.12	OUI22				1
3.11	OUI23				1
3.10	OUI24				0
3.9	PART5	Manufacturer's Part Number	03_H	R	0
3.8	PART4				0
3.7	PART3				0
3.6	PART2				1
3.5	PART1				0
3.4	PART0				0
3.3	REV3	Manufacturer's Revision Number		R	–
3.2	REV2				–
3.1	REV1				–
3.0	REV0				–

x.15 Bit Is Shifted First Table

Table 14 - MI Register 4 (AutoNegotiation Advertisement) Structure

4.15	4.14	4.13	4.12	4.11	4.10	4.9	4.8
NP	ACK	RF	0	0	0	T4	TX_FDX
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W

4.7	4.6	4.5	4.4	4.3	4.2	4.1	4.0
TX_HDX	10_FDX	10_HDX	0	0	0	0	CSMA
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

BIT	SYMBOL	NAME	DEFINITION	R/W	DEF.
4.15	NP	Next Page Enable	1 = Next Page Exists [1] 0 = No Next Page	R/W	0
4.14	ACK	Acknowledge	1 = Received AutoNegotiation Word Recognized 0 = Not Recognized	R	0
4.13	RF	Remote Fault Enable	1 = AutoNegotiation Remote Fault Detected 0 = No Remote Fault	R/W	0
4.12 4.11 4.10	Reserved	Reserved	Reserved	R/W	0 0 0
4.9	T4	100BASE-T4 Capable	1 = Capable Of 100BASE-T4 0 = Not Capable	R/W	0
4.8	TX_FDX	100BASE-TX Full Duplex Capable	1 = Capable of 100BASE-TX Full Duplex 0 = Not Capable	R/W	1
4.7	TX_HDX	100BASE-TX Half Duplex Capable	1 = Capable Of 100BASE-TX Half Duplex 0 = Not Capable	R/W	1
4.6	10_FDX	10BASE-T Full Duplex Capable	1 = Capable Of 10BASE-T Full Duplex 0 = Not Capable	R/W	1
4.5	10_HDX	10BASE-T Half Duplex Capable	1 = Capable Of 10BASE-T Half Duplex 0 = Not Capable	R/W	1
4.4 thru 4.1	Reserved	Reserved	Reserved	R/W	0 0 0 0
4.0	CSMA	CSMA 802.3 Capable	1 = Capable of 802.3 CSMA Operation 0 = Not Capable	R/W	1

x.15 Bit Is Shifted First

Note 1. Next Page currently not supported.

Table 15 - MI Register 5 (AutoNegotiation Remote End Capability) Structure

5.15	5.14	5.13	5.12	5.11	5.10	5.9	5.8
NP	ACK	RF	0	0	0	T4	TX_FDX
R	R	R	R	R	R	R	R
5.7	5.6	5.5	5.4	5.3	5.2	5.1	5.0
TX_HDX	10_FDX	10_HDX	0	0	0	0	CSMA
R	R	R	R	R	R	R	R

BIT	SYMBOL	NAME	DEFINITION	R/W	DEF.
5.15	NP	Next Page Enable	1 = Next Page Exists 0 = No Next Page	R	0
5.14	ACK	Acknowledge	1 = Received AutoNegotiation Word Recognized 0 = Not Recognized	R	0
5.13	RF	Remote Fault Enable	1 = AutoNegotiation Remote Fault Detected 0 = No Remote Fault	R	0
5.12 5.11 5.10	Reserved	Reserved	Reserved	R	0 0 0
5.9	T4	100BASE-T4 Capable	1 = Capable Of 100BASE-T4 0 = Not Capable	R	0
5.8	TX_FDX	100BASE-TX Full Duplex Capable	1 = Capable of 100BASE-TX Full Duplex 0 = Not Capable	R	0
5.7	TX_HDX	100BASE-TX Half Duplex Capable	1 = Capable Of 100BASE-TX Half Duplex 0 = Not Capable	R	0
5.6	10_FDX	10BASE-T Full Duplex Capable	1 = Capable Of 10BASE-T Full Duplex 0 = Not Capable	R	0
5.5	10_HDX	10BASE-T Half Duplex Capable	1 = Capable Of 10BASE-T Half Duplex 0 = Not Capable	R	0
5.4 thru 5.1	Reserved	Reserved	Reserved	R	0 0 0 0
5.0	CSMA	CSMA 802.3 Capable	1 = Capable of 802.3 CSMA Operation 0 = Not Capable	R	0

x.15 Bit Is Shifted First

Table 16 - MI Register 16 (Configuration 1) Structure And Bit Definition

16.15	16.14	16.13	16.12	16.11	16.10	16.9	16.8
LNK_DIS	XMT_DIS	XMT_PDN	TXEN_CRS	BYP_ENC	BYP_SCR	UNSCR_DIS	EQLZR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

16.7	16.6	16.5	16.4	16.3	16.2	16.1	16.0
CABLE	RLVL0	TLVL3	TLVL2	TLVL1	TLVL0	TRF1	TRF0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

BIT	SYMBOL	NAME	DEFINITION	R/W	DEF.
16.15	LNK_DIS	Link Disable	1 = Receive Link Detect Function Disabled (Force Link Pass) 0 = Normal	R/W	0
16.14	XMT_DIS	TP Transmit Disable	1 = TP Transmitter Disabled 0 = Normal	R/W	0
16.13	XMT_PDN	TP Transmit Powerdown	1 = TP Transmitter Powered Down 0 = Normal	R/W	0
16.12	TXEN_CRS	TXEN to CRS Loopback Disable	1 = TX_EN to CRS Loopback Disabled 0 = Enabled	R/W	0
16.11	BYP_ENC	Bypass Encoder/Decoder Select	1 = Bypass 4B5B Encoder/Decoder 0 = No Bypass	R/W	0
16.10	BYP_SCR	Bypass Scrambler/Descr-ambler Select	1 = Bypass Scrambler/Descrambler 0 = No Bypass	R/W	0
16.9	UNSCR_DIS	Unscrambled Idle Reception Disable	1 = Disable AutoNegotiation with devices that transmit unscrambled idle on powerup and various instances 0 = Enables AutoNegotiation with devices that transmit unscramblled idle on powerup and various instances	R/W	0
16.8	EQLZR	Receive Equalizer Select	1 = Receive Equalizer Disabled, Set To 0 Length 0 = Receive Equalizer On (For 100Mb Mode Only)	R/W	0
16.7	CABLE	Cable Type Select	1 = STP (150 Ohm) 0 = UTP (100 Ohm)	R/W	0
16.6	RLVL0	Receive Input Level Adjust	1 = Receive Squelch Levels Reduced By 4.5 dB 0 = Normal	R/W	0
16.5 16.4 16.3 16.2	TLVL3 TLVL2 TLVL1 TLVL0	Transmit Output Level Adjust	See Table 3	R/W	1 0 0 0
16.1 16.0	TRF1 TRF0	Transmitter Rise/Fall Time Adjust	11 = -0.25 nS 10 = +0.0 nS 01 = +0.25 nS 00 = +0.50 nS	R/W	1 0

x.15 Bit Is Shifted First

Table 17 - MI Register 17 (Configuration 2) Structure And Bit Definition

17.15	17.14	17.13	17.12	17.11	17.10	17.9	17.8
nPLED3_1	nPLED3_0	nPLED2_1	nPLED2_0	nPLED1_1	nPLED1_0	nPLED0_1	nPLED0_0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

17.7	17.6	17.5	17.4	17.3	17.2	17.1	17.0
LED_DEF1	LED_DEF0	APOL_DIS	JAB_DIS	MREG	INT_MDIO	R/J_CFG	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

BIT	SYMBOL	NAME	DEFINITION	R/W	DEF.
17.15 17.14	nPLED3_1 nPLED3_0	Programmable LED Output Select, Pin nPLED3	11 = Normal (nPLED3 Is Determined By Bits 17.7-17.6 And Table 5. Default is LINK100) 10 = LED Blink (nPLED3 Is Toggling 100 mS Low, 100 mS High) 01 = LED On (nPLED3 Is Low) 00 = LED Off (nPLED3 Is High)	R/W	11
17.13 17.12	nPLED2_1 nPLED2_0	Programmable LED Output Select, Pin nPLED2	11 = Normal (nPLED2 Is Determined By Bits 17.7-17.6 And Table 5. Default is Activity) 10 = LED Blink (nPLED2 Is Toggling 100 mS Low, 100 mS High) 01 = LED On (nPLED2 Is Low) 00 = LED Off (nPLED2 Is High)	R/W	11
17.11 17.10	nPLED1_1 nPLED1_0	Programmable LED Output Select, Pin nPLED1	11 = Normal (nPLED1 Is Determined By Bits 17.7-17.6 And Table 5. Default is Full Duplex) 10 = LED Blink (nPLED1 Is Toggling 100 mS Low, 100 mS High) 01 = LED On (nPLED1 Is Low) 00 = LED Off (nPLED1 Is High)	R/W	11
17.9 17.8	nPLED0_1 nPLED0_0	Programmable LED Output Select, Pin nPLED0	11 = Normal (nPLED0 Is Determined By Bits 17.7-17.6 And Table 5. Default is LINK10) 10 = LED Blink (nPLED0 Is Toggling 100 mS Low, 100 mS High) 01 = LED On (nPLED0 Is Low) 00 = LED Off (nPLED0 Is High)	R/W	11
17.7 17.6	LED_DEF1 LED_DEF0	LED Normal Function Select	See Table 5 R/W	0	
17.5	APOL_DIS	Auto Polarity Disable	1 = Auto Polarity Correction Function Disabled 0 = Normal	R/W	0
17.4	JAB_DIS	Jabber Disable Select	1 = Jabber Disabled 0 = Enabled	R/W	0
17.3	MREG	Multiple Register Access Enable	1 = Multiple Register Access Enabled 0 = No Multiple Register Access	R/W	0
17.2	INT_MDIO	Interrupt Scheme Select	1 = Interrupt Signaled With MDIO Pulse During Idle 0 = Interrupt Not Signalled On MDIO	R/W	0
17.1	R/J_CFG	R/J Configuration Select	1 = RX_EN/nJAM Pin Is Configured To Be nJAM 0 = RX_EN/nJAM Pin Is Configured To Be RX_EN	R/W	0
17.0			Reserved, Must be 0 for Proper Operation	R/W	0

Table 18 - MI Register 18 (Status Output) Structure And Bit Definition

18.15	18.14	18.13	18.12	18.11	18.10	18.9	18.8
INT	LNK_FAIL	LOSS_SYNC	CWRD	SSD	ESD	RPOL	JAB
R	R/LT	R/LT	R/LT	R/LT	R/LT	R/LT	R/LT

18.7	18.6	18.5	18.4	18.3	18.2	18.1	18.0
SPD_DET	nDPLX_DET	0	0	0	0	0	0
R/LT	R/LT	R	R	R	R	R	R

BIT	SYMBOL	NAME	DEFINITION	R/W	DEF.
18.15	INT	Interrupt Detect	1 = Interrupt Bit(s) Have Changed Since Last Read Operation. 0 = No Change	R	0
18.14	LNK_FAIL	Link Fail Detect	1 = Link Not Detected 0 = Normal	R/LT	0
18.13	LOSS_SYNC	Descrambler Loss of Synchronization Detect	1 = Descrambler Has Lost Synchronization 0 = Normal	R/LT	0
18.12	CWRD	Codeword Error	1 = Invalid 4B5B Code Detected On Receive Data 0 = Normal	R/LT	0
18.11	SSD	Start Of Stream Error	1 = No Start Of Stream Delimiter Detected on Receive Data 0 = Normal	R/LT	0
18.10	ESD	End Of Stream Error	1 = No End Of Stream Delimiter Detected on Receive Data 0 = Normal	R/LT	0
18.9	RPOL	Reverse Polarity Detect	1 = Reverse Polarity Detected 0 = Normal	R/LT	0
18.8	JAB	Jabber Detect	1 = Jabber Detected 0 = Normal	R/LT	0
18.7	SPD_DET	100/10 Speed Detect	1 = Device in 100 Mbps Mode (100BASE-TX) 0 = Device in 10 Mbps Mode (10BASE-T)	R/LT	1
18.6	nDPLX_DET	Duplex Detect	1 = Device In Full Duplex 0 = Device In Half Duplex	R/LT	0
18.5 18.4	Reserved	Reserved	Reserved for Factory Use	R/LT	0 0
18.3 18.2 18.1 18.0	Reserved	Reserved	Reserved	R	0 0 0 0

x.15 Bit Is Shifted First

Table 19 - MI Register 19 (Mask) Structure And Bit Definition

19.15	19.14	19.13	19.12	19.11	19.10	19.9	19.8
MASK_ INT	MASK_ LNK_FAIL	MASK_ LOSS_SYNC	MASK_ CWRD	MASK_ SSD	MASK_ ESD	MASK_ RPOL	MASK_ JAB
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

19.7	19.6	19.5	19.4	19.3	19.2	19.1	19.0
MASK_ SPD_DET	MASK_ nDPLX_DET	MASK_ ANEG_STS1	MASK_ ANEG_STS0	FXLVL1	FXLVL0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R	R

BIT	SYMBOL	NAME	DEFINITION	R/W	DEF.
19.15	MASK_ INT	Interrupt Mask - Interrupt Detect	1 = Mask Interrupt For INT In Register 18 0 = No Mask	R/W	1
19.14	MASK_ LNK_FAIL	Interrupt Mask - Link Fail Detect	1 = Mask Interrupt For LNK_FAIL In Register 18 0 = No Mask	R/W	1
19.13	MASK_ LOSS_SYNC	Interrupt Mask - Descrambler Loss of Synchronization Detect	1 = Mask Interrupt For LOSS_SYNC In Register 18 0 = No Mask	R/W	1
19.12	MASK_ CWRD	Interrupt Mask - Codeword Error	1 = Mask Interrupt For CWRD In Register 18 0 = No Mask	R/W	1
19.11	MASK_ SSD	Interrupt Mask - Start Of Stream Error	1 = Mask Interrupt For SSD In Register 18 0 = No Mask	R/W	1
19.10	MASK_ ESD	Interrupt Mask -End Of Stream Error	1 = Mask Interrupt For ESD In Register 18 0 = No Mask	R/W	1
19.9	MASK_ RPOL	Interrupt Mask - Reverse Polarity Detect	1 = Mask Interrupt For RPOL In Register 18 0 = No Mask	R/W	1
19.8	MASK_ JAB	Interrupt Mask - Jabber Detect	1 = Mask Interrupt For JAB In Register 18 0 = No Mask	R/W	1
19.7	MASK_ SPD_DET	Interrupt Mask - 100/10 Speed Detect	1 = Mask Interrupt For SPD_DET In Register 18 0 = No Mask	R/W	1
19.6	MASK_ nDPLX_DET	Interrupt Mask - Duplex Detect	1 = Mask Interrupt For nDPLX_DET In Register 18 0 = No Mask	R/W	1
19.5 19.4	FXLVL1 FXLVL0	FX Transmit Level Adjust	11 = 1.30 10 = 1.15 01 = 0.85 00 = 1.00	R/W	0 0
19.3 19.2 19.1 19.0	Reserved	Reserved	Reserved, Must be 0 for Proper Operation	R	0 0 0 0

x.15 Bit Is Shifted First

Table 20 - MI Register 20 (Reserved) Structure And Bit Definition

20.15	20.14	20.13	20.12	20.11	20.10	20.9	20.8
0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

20.7	20.6	20.5	20.4	20.3	20.2	20.1	20.0
0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

BIT	SYMBOL	NAME	DEFINITION	R/W	DEF.
20.15	Reserved	Reserved	Reserved for Factory Use. Must Be Written to 0 for Normal Operation	R/W	0
20.14					0
20.13					0
20.12					0
20.11					0
20.10					0
20.9					0
20.8					0
20.7					0
20.6					0
20.5					0
20.4					0
20.3					0
20.2					0
20.1					0
20.0					0

x.15 Bit Is Shifted First

Specifications

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are limits beyond which may cause permanent damage to the device or affect device reliability. All voltages are specified with respect to GND, unless otherwise specified.

VDD Supply Voltage	-0.3V to +4.0V
All Inputs and Outputs	-0.3V to 5.5V
Package Power Dissipation	2.0 Watt@70°C
Storage Temperature	-65 to +150°C
Temperature Under Bias	-10 to +80°C
Lead Temperature (Soldering, 10 Sec)	260°C
Body Temperature (Soldering, 30 Sec)	220°C

DC ELECTRICAL CHARACTERISTICS

Unless otherwise noted, all test conditions are as follows:

1. T_A= 0 to +70°C
2. V_{DD} = 3.3V +/-5%
3. 25 MHz +/- 0.01%
4. REXT = 10K +/- 1%, no load

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
VIL	Input Low Voltage			0.8	Volt	All except OSCIN, nMDA[4:0], SD/nFXDIS, SD_THR
				VDD-1.0	Volt	nMDA[4:0]
				1.5	Volt	OSCIN
				0.45	Volt	SD/nFXDIS (for FX disable), SD_THR (for 3.3V/5V select)
VIH	Input High Voltage	2		5.5	Volt	All except OSCIN, nMDA[4:0], SD/nFXDIS, SD_THR
		VDD -0.5			Volt	nMDA[4:0]
		3.5			Volt	OSCIN
		0.85			Volt	SD/nFXDIS (for FX disable), SD_THR (for 3.3V/5V select)
IIL	Input Low Current			-1	uA	VIN=GND. All Except OSCIN, nMDA[4:0], nRESET
		-4		-25	uA	VIN=GND. nMDA[4:0]
		-12		-120	uA	VIN=GND. nRESET
				-150	uA	VIN=GND. OSCIN
IIH	Input High Current			1	uA	VIN=VDD. All Except OSCIN, RPTR
		12		120	uA	VIN=VDD. RPTR
				150	uA	VIN=VDD. OSCIN
VOL	Output Low Voltage			0.4	Volt	IOL=-4 mA. All Except nPLED[5:0]
				1	Volt	IOL=-10 mA. nPLED[5:0]
VOH	Output High Voltage	VDD-1.0			Volt	IOH=4 mA. All Except nPLED[5:0], nMDINT
		2.4			Volt	IOH=4 uA. nPLED[5:2], nMDINT
		VDD-1.0			Volt	IOH=10mA. nPLED[1:0]
CIN	Input Capacitance		5		pF	
IDD	VDD Supply Current			120	mA	Transmitting, 100 Mbps
				140	mA	Transmitting, 10 Mbps
IGND	GND Supply Current			190	mA	Transmitting, 100 Mbps, Note 1
				220	mA	Transmitting, 10 Mbps, Note 1
IPDN	Powerdown Supply Current			200	uA	Powerdown, Either IDD or IGND

Note 1: IGND includes current flowing into GND from the external resistors and transformer on TPO/FXO aS shown in Figure 11.

TWISTED PAIR CHARACTERISTICS, TRANSMIT

Unless otherwise noted, all test conditions are as follows:

1. T_A= 0 to +70°C
2. V_{DD} = 3.3V +/-5%
3. 25 MHz +/- 0.01%
4. REXT = 10K +/- 1%, no load
5. TPO± loading shown in Figure 11 or equivalent.

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
T_{OV}	TP Differential Output Voltage	0.950	1.000	1.050	V pk	100 Mbps, UTP Mode, 100 Ohm Load
		1.165	1.225	1.285	V pk	100 Mbps, STP Mode, 150 Ohm Load
		2.2	2.5	2.8	V pk	10 Mbps, UTP Mode, 100 Ohm Load
		2.694	3.062	3.429	V pk	10 Mbps, STP Mode, 150 Ohm Load
T_{OVS}	TP Differential Output Voltage Symmetry	98		102	%	100 Mbps, Ratio of Positive And Negative Amplitude Peaks on TPO±
T_{ORF}	TP Differential Output Rise And Fall Time	3.0		5.0	nS	100 Mbps TRFADJ [1:0] = 10
T_{ORFS}	TP Differential Output Rise And Fall Time Symmetry			+/- 0.5	nS	100 Mbps, Difference Between Rise And Fall Times on TPO±
T_{ODC}	TP Differential Output Duty Cycle Distortion			+/- 0.25	nS	100 Mbps, Output Data= 0101... NRZ Pattern Unscrambled, Measure At 50% Points
T_{OJ}	TP Differential Output Jitter			+/- 1.4	nS	100 Mbps, Output Data =scrambled /H/
T_{OO}	TP Differential Output Overshoot			5.0	%	100 Mbps
T_{OVT}	TP Differential Output Voltage Template	See Figure 4				10 Mbps
T_{SOI}	TP Differential Output SOI Voltage Template	See Figure 6				10 Mbps

TWISTED PAIR CHARACTERISTICS, TRANSMIT (continued)

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
T_{LPT}	TP Differential Output Link Pulse Voltage Template	See Figure 7				10 Mbps, NLP and FLP
T_{OIV}	TP Differential Output Idle Voltage			+/- 50	mV	10 Mbps. Measured on SecondarySide of Xfmr in Figure 11.
T_{OIA}	TP Output Current	38	40	42	mA pk	100 Mbps, UTP with TLVL[3:0]=1000
		31.06	32.66	34.26	mA pk	100 Mbps, STP with TLVL[3:0]=1000
		88	100	112	mA pk	10 Mbps, UTP with TLVL[3:0]=1000
		71.86	81.64	91.44	mA pk	10 Mbps, STP with TLVL[3:0]=1000
T_{OIR}	TP Output Current Adjustment Range	0.80		1.2		V_{DD}= 3.3V, Adjustable with REXT, relative to T_{OIA} with REXT=10K
		0.86		1.16		V_{DD}= 3.3V, Adjustable with TLVL[3:0] See Section 5.4 Relative to Value at TLVL [3:0]=1000
T_{ORA}	TP Output Current TLVL Step Accuracy			+/-50	%	Relative to Ideal Values in Table 3. Table 3 Values Relative to Output with TLVL[3:0]=1000.
T_{OR}	TP Output Resistance		10K		Ohm	
T_{OC}	TP Output Capacitance		15		pF	

TWISTED PAIR CHARACTERISTICS, RECEIVE

Unless otherwise noted, all test conditions are as follows:

1. T_A= 0 to +70°C
2. V_{CC} = 3.3V +/-5%
3. 25 MHz +/- 0.01%
4. REXT = 10K +/- 1%, no load
5. 62.5/10 Mhz Square Wave on TP inputs in 100/10 Mbps

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
R_{ST}	TP Input Squelch Threshold	166		500	mV pk	100 Mbps, RLVL=0
		310		540	mV pk	10 Mbps, RLVL=0
		60		200	mV pk	100 Mbps, RLVL=1
		186		324	mV pk	10 Mbps, RLVL=1
R_{UT}	TP Input Unsquelch Threshold	100		300	mV pk	100 Mbps, RLVL=0
		186		324	mV pk	10 Mbps, RLVL=0
		20		90	mV pk	100 Mbps, RLVL=1
		112		194	mV pk	10 Mbps, RLVL=1
R_{OCV}	TP Input Open Circuit Voltage		V_{DD} – 2.4 ± 0.2		Volt	Voltage on Either TPI+ or TPI– with Respect to GND.
R_{CMR}	TP Input Common Mode Voltage Range		R_{OCV} ± 0.25		Volt	Voltage on TPI± with Respect to GND.
R_{DR}	TP Input Differential Voltage Range			V_{DD}	Volt	
R_{IR}	TP Input Resistance	5K			Ohm	
R_{IC}	TP Input Capacitance		10		pF	

FX CHARACTERISTICS, TRANSMIT

Unless otherwise noted, all test conditions are as follows:

1. T_A= 0 to +70° C
2. VDD=3.3V +/-5%
3. 25 MHz +/- 0.01%
4. REXT=10K +/- 1%, no load
5. FXO± Loading as Shown in Figure 14 or Equivalent

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
FOVH	FXO+/- Output Voltage, High	VDD -1.020		VDD -0.880	V	Single Ended, Measure FXO+/- relative to GND
FOVL	FXO+/- Output Voltage, Low	VDD -1.810		VDD -1.620	V	Single Ended, Measure FXO+/- relative to GND
FOIA	FXO+/- Output Current	12		20	mA pk	
FOIR	FXO+/- Output Current Adjustment Range	0.85		1.15		VDD=3.3V, Adjustable With REXT, Relative to FOIA WithREXT=10K
		0.85		1.30		VDD=3.3V, Adjustable With FLVL[1:0], Relative To Value At FLVL[1:0]=10
FORA	FXO+/- Output Current TLVL Step Accuracy			+/-50	%	Relative To Ideal Values In Table 4
FORF	FXO+/- Differential Output Rise And Fall Time			1.3	nS	
FORFS	FXO+/- Differential Output Rise And Fall Time Symmetry			+/- 0.5	nS	Difference Between Rise And Fall Times on FXO+
FODC	FXO+/- Differential Output Duty Cycle Distortion			+/- 0.25	nS	Output Data=0101... Pattern Measure At 50% Points
FOJ	FXO+/- Differential Output Jitter			+/- 1.3	nS	Output Data=/H/
FOR	FXO+/- Output Resistance		10K		Ohm	
FOC	FXO+/- Output Capacitance		10		pF	

FX CHARACTERISTICS, RECEIVE

Unless otherwise noted, all test conditions are as follows:

1. T_A= 0 to +70° C
2. VDD=3.3V +/-5%
3. 25 MHz +/- 0.01%
4. REXT=10K +/- 1%, no load
5. 125 MHZ Square Wave on FXI+/- and SD Inputs

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
FDIV	FXI+/- Differential Input Voltage	0.150			V pk	
FCMR	FXI+/- Input Common Mode Voltage Range	1.35		VDD-0.80	V	Voltage on Either FXI+ or FXI- with Respect to GND
FSDIH	SD/nFXDIS Input High Voltage	V_{SD_THR} - 50mV			V	This spec applies when device interfaces to 5V external fiber optic transceivers. V_{SD_THR} is the voltage applied to the SD_THR pin and is spec'ed by FSDTHR
		VCC-1.165			V	This spec applies when device interfaces to 3.3V external fiber optic transceivers. SD_THR is tied to GND.
FSDIL	SD/nFXDIS Input Low Voltage			V_{SD_THR} + 50mV	V	This spec applies when device interfaces to 5V external fiber optic transceivers. V_{SD_THR} is the voltage applied to the SD_THR pin and is spec'ed by FSDTHR
				VCC-1.475		This spec appies when device interfaces to 3.3V external fiber optic transceivers. SD_THR is tied to GND.
FSDTHR	SD_THR Input Voltage	VCC -1.3V -10%	VCC -1.3V	VCC -1.3V + 10%	V	This spec applies when device interfaces to 5V external fiber optic transceivers. When interfacing to 3.3V fiber transceivers, SD_THR is tied to GND.
FIR	FXI+/-, SD/nFXDIS Input Resistance	5K			ohm	
FIC	FXI+/-, SD/nFXDIS Input Capacitance		10		pF	

AC TEST TIMING CONDITIONS

Unless otherwise noted, all test conditions are as follows:

1. T_A= 0 to +70°C
2. V_{DD} = 3.3V +/-5%
3. 25 MHz +/- 0.01%
4. REXT = 10K +/- 1%, no load
5. Input conditions:
   - All Inputs: tr,tf<=10nS, 20-80%
6. Output Loading
   - TPO±: Same as Figure 11 or equivalent, 10pF
   - Open Drain Outputs: 1K Pullup, 50pF
   - All Other Digital Outputs: 25pF
7. Measurement Points:
   - TPO±, TPI±: 0.0 V During Data, ±0.3V at start/end of packet
   - All other inputs and outputs: 1.4 Volts

25 Mhz INPUT / OUTPUT CLOCK TIMING CHARACTERISTICS

Refer to Figure 18 for Timing Diagram.

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
t_1	OSCIN Period	39.996	40	40.004	nS	Clock Applied to OSCIN
t_2	OSCIN High Time	16			nS	Clock Applied to OSCIN
t_3	OSCIN Low Time	16			nS	Clock Applied to OSCIN
t_4	OSCIN to TX_CLK Delay			10	nS	100 Mbps
				20	nS	10 Mbps

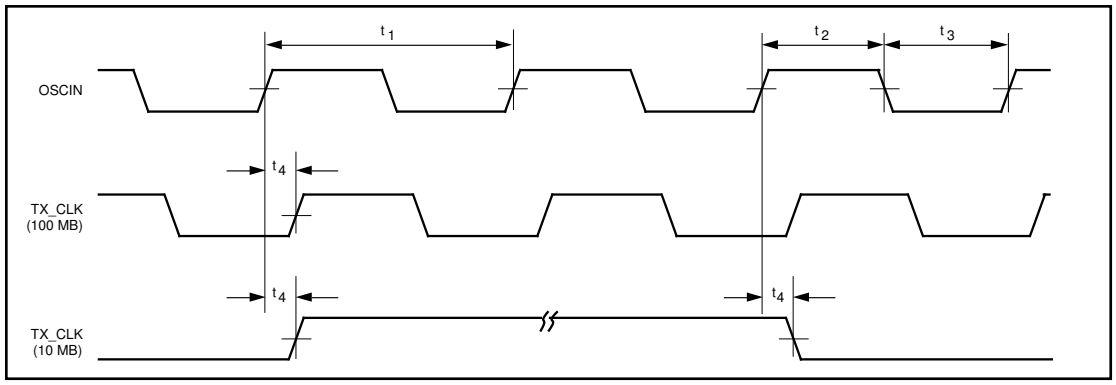


FIGURE 18 - 25 MHZ OUTPUT TIMING

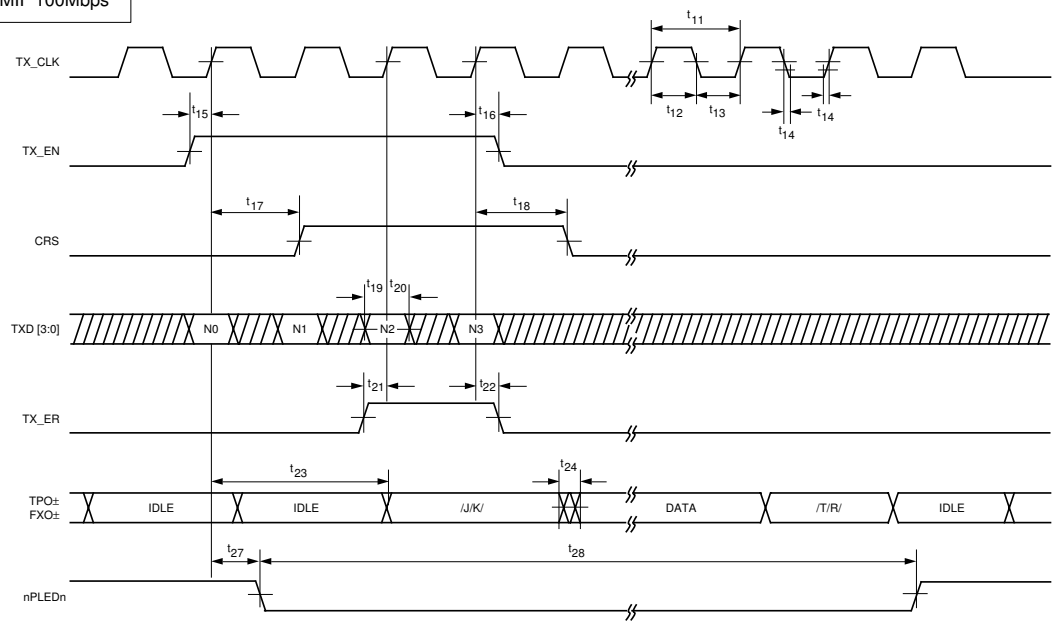
TRANSMIT TIMING CHARACTERISTICS

Refer to Figure 19-20 for Timing Diagram

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
t_{11}	TX_CLK Period	39.996	40	40.004	nS	100 Mbps
		399.96	400	400.04	nS	10 Mbps
t_{12}	TX_CLK Low Time	16	20	24	nS	100 Mbps
		160	200	240	nS	10 Mbps
t_{13}	TX_CLK High Time	16	20	24	nS	100 Mbps
		160	200	240	nS	10 Mbps
t_{14}	TX_CLK Rise/Fall Time			10	nS	
t_{15}	TX_EN Setup Time	15			nS	Note 1
t_{16}	TX_EN Hold Time	0			nS	
t_{17}	CRS During Transmit Assert Time			40	nS	100 Mbps
				400	nS	10 Mbps
t_{18}	CRS During Transmit Deassert Time			160	nS	100 Mbps
				900	nS	10 Mbps
t_{19}	TXD Setup Time	15			nS	Note 1
t_{20}	TXD Hold Time	0			nS	
t_{21}	TX_ER Setup Time	15			nS	Note 1
t_{22}	TX_ER Hold Time	0			nS	
t_{23}	Transmit Propagation Delay	60		140	nS	100 Mbps, MII
				140	nS	100 Mbps, FBI
				600	nS	10 Mbps
t_{24}	Transmit Output Jitter			±0.7	nS pk-pk	100 Mbps
				±5.5	nS pk-pk	10 Mbps
t_{25}	Transmit SOI Pulse Width To 0.3V	250			nS	10 Mbps
t_{26}	Transmit SOI Pulse Width to 40 mV			4500	nS	10 Mbps
t_{27}	nPLEDn Delay Time			25	mS	nPLEDn Programmed For Activity
t_{28}	nPLEDn Pulse Width	80		105	mS	nPLEDn Programmed For Activity

Note 1: Setup time measured with 5 pF loading on TXC. Additional leading will create delay on TXC rise time which will require increased setup times accordingly.

MII 100Mbps



FBI 100Mbps

Same as MII 100Mbps Except:

1. TX_ER Converted to TXD4
2. RX_ER Converted to RXD4

FIGURE 19 - TRANSMIT TIMING - 100 Mbps

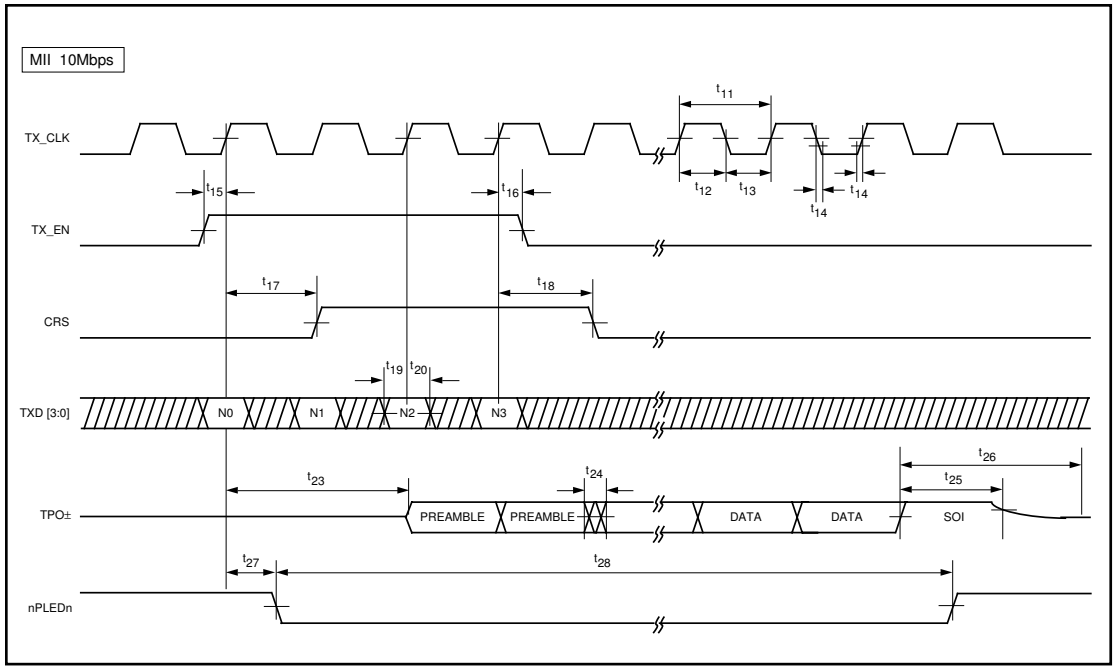


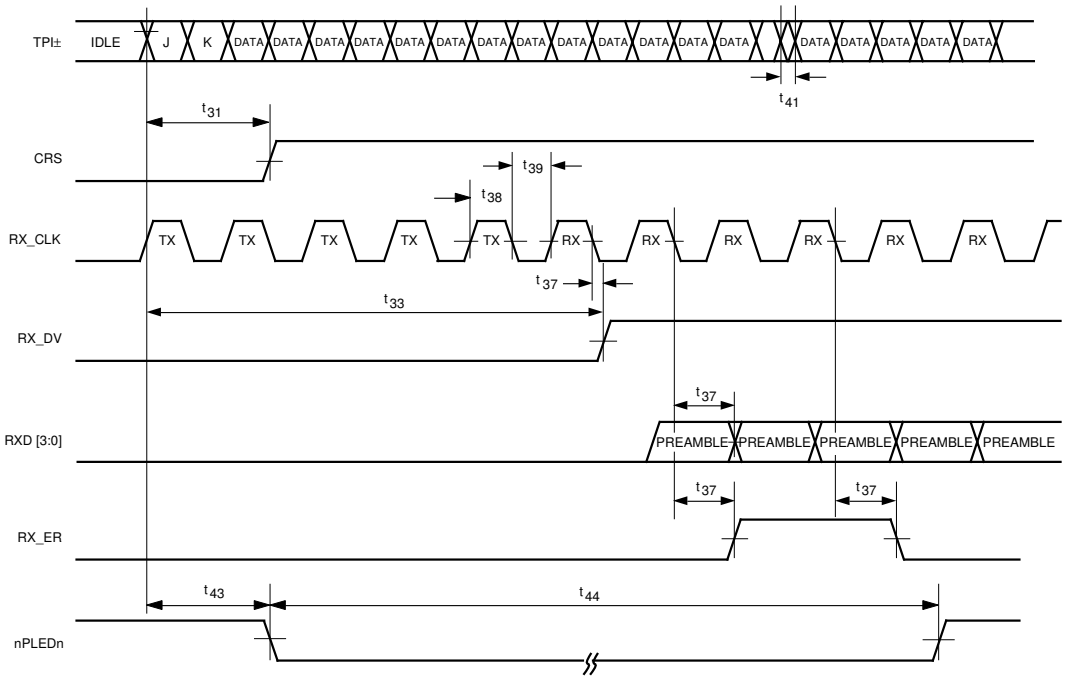
FIGURE 20 - TRANSMIT TIMING - 10 Mbps

RECEIVE TIMING CHARACTERISTICS

Refer to Figures 21-25 for Timing Diagrams

SYM	PARAMETER	LIMIT MIN	LIMIT TYP	LIMIT MAX	UNIT	CONDITIONS
t_{31}	Start Of Packet To CRS Assert Delay			200	nS	100 Mbps, MII
				200	nS	100 Mbps, FBI
				700	nS	10 Mbps
t_{32}	End Of Packet To CRS Deassert Delay	130		240	nS	100 Mbps, MII
				240	nS	100 Mbps, FBI
				600	nS	10 Mbps. Relative To Start Of SOI Pulse
t_{33}	Start Of Packet To RX_DV Assert Delay			240	nS	100 Mbps
				3600	nS	10 Mbps
t_{34}	End Of Packet To RX_DV Deassert Delay			280	nS	100 Mbps
				1000	nS	10 Mbps. Relative To Start Of SOI Pulse
t_{37}	RX_CLK To RX_DV, RXD, RX_ER Delay	-8		8	nS	100 Mbps
		-80		80	nS	10 Mbps
t_{38}	RX_CLK High Time	18	20	22	nS	100 Mbps
		180	200	600	nS	10 Mbps
t_{39}	RX_CLK Low Time	18	20	22	nS	100 Mbps
		180	200	600	nS	10 Mbps
t_{40}	SOI Pulse Minimum Width Required for Idle Detection	125		200	nS	10 Mbps Measure TPI± from last zero cross to 0.3V point.
t_{41}	Receive Input Jitter			±3.0	nS pk - pk	100 Mbps
				±13.5	nS pk -pk	10 Mbps
t_{43}	nPLEDn Delay Time			25	mS	nPLEDn Programmed for Activity
t_{44}	nPLEDn Pulse Width	80		105	mS	nPLEDn Programmed for Activity
t_{45}	RX_CLK, RXD, CRC, RX_DV, RX_ER Output Rise and Fall Times			10	nS	
t_{46}	RX_EN Deassert to Rcv MII Output HI-Z Delay			40	nS	
t_{47}	RX_EN Assert to Rcv MII Output Active Delay			40	nS	

MII 100 Mbps



FBI 100 Mbps

Same as MII 100 Mbps except:
1. RX_ER Converted to RXD4
2. TX_ER Converted to TXD4

FIGURE 21 - RECEIVE TIMING, START OF PACKET - 100 Mbps

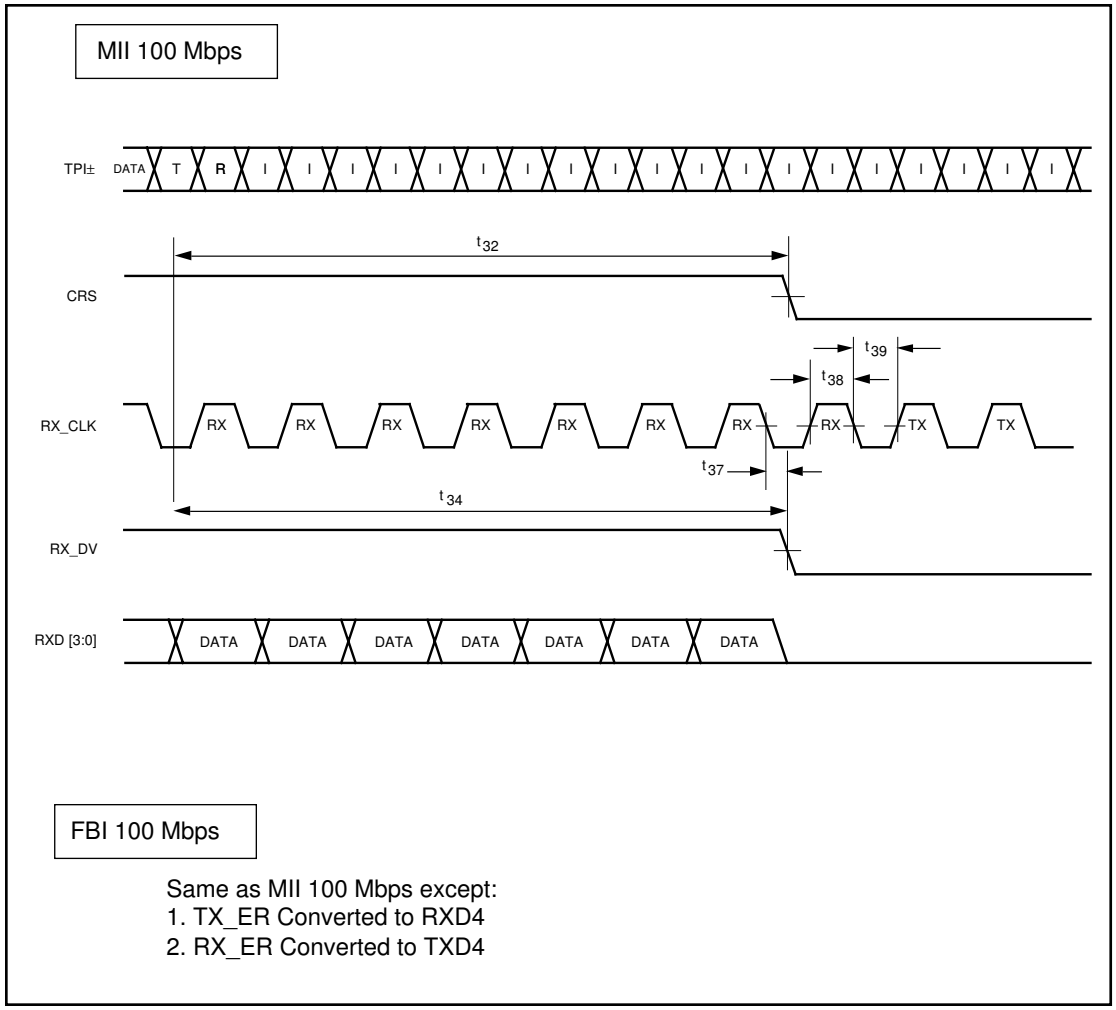


FIGURE 22 - RECEIVE TIMING, END OF PACKET - 100 Mbps

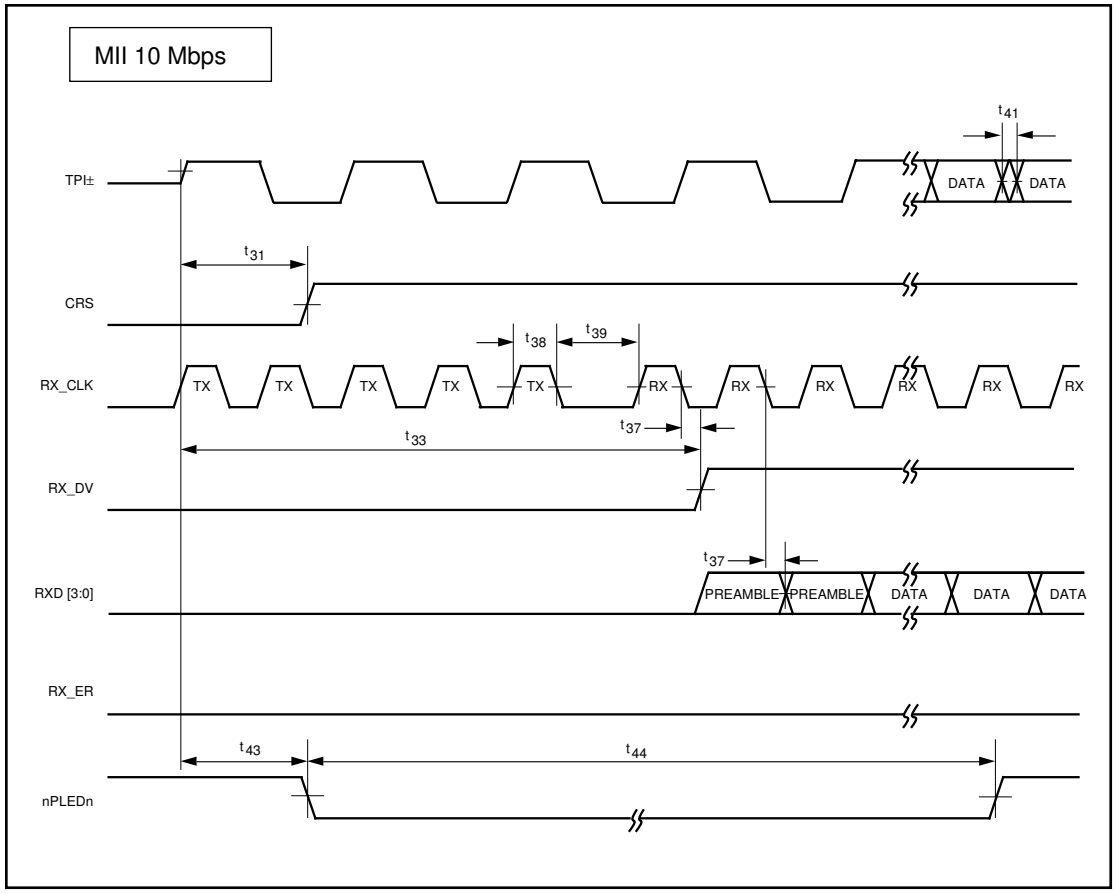


FIGURE 23 - RECEIVE TIMING, START OF PACKET - 10 Mbps

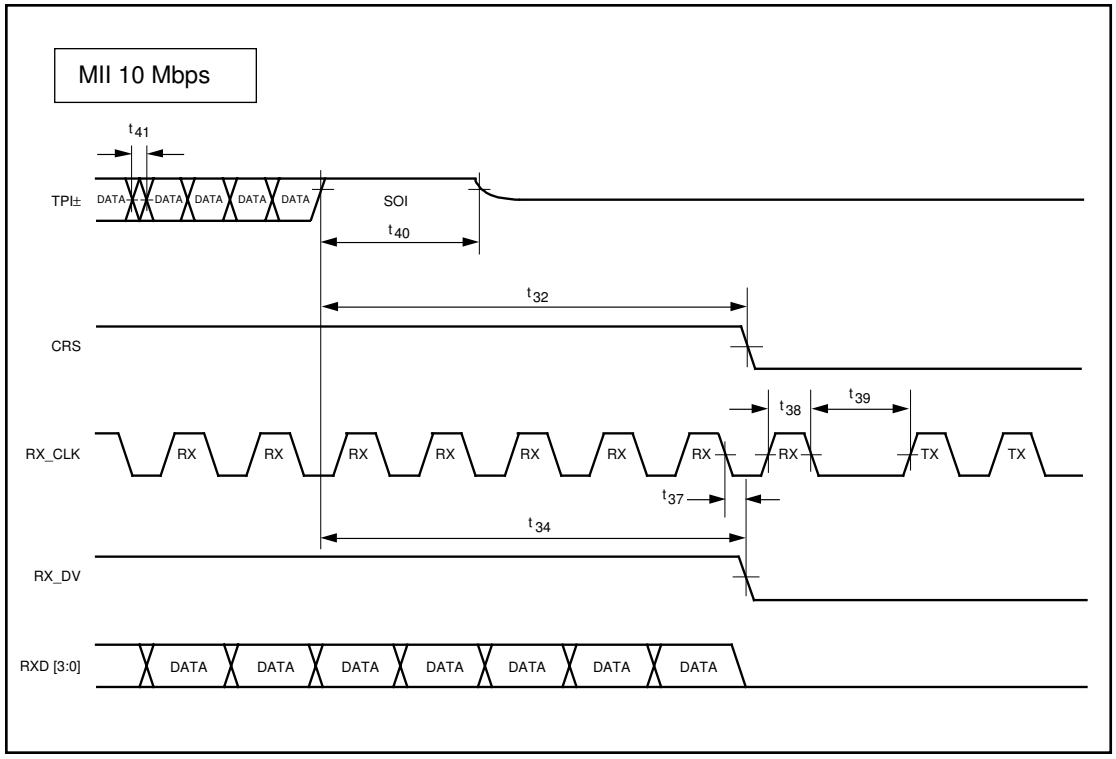


FIGURE 24 - RECEIVE TIMING, END OF PACKET - 10 Mbps

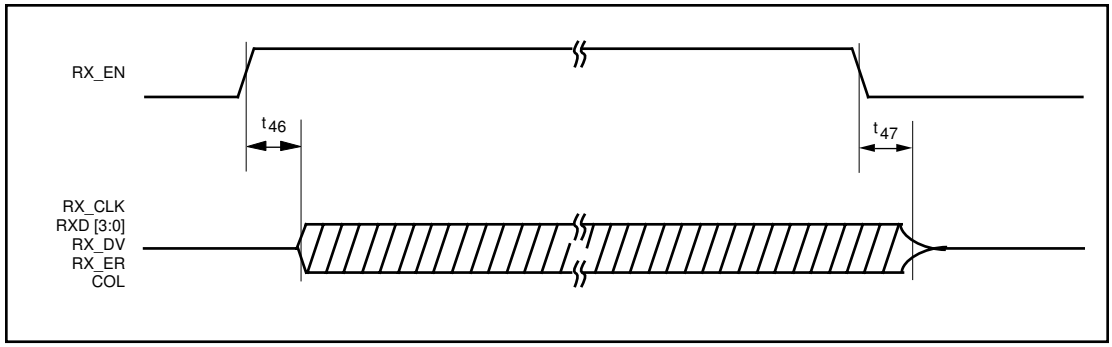


FIGURE 25 - RX_EN TIMING

COLLISION AND JAM TIMING CHARACTERISTICS

Refer to Figures 26-29 for Timing Diagrams

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
t_{51}	Rcv Packet Start to			200	nS	100 Mbps
	COL Assert Time			700	nS	10 Mbps
t_{52}	Rcv Packet Stop to	130		240	nS	100 Mbps
	COL Deassert Time			300	nS	10 Mbps
t_{53}	Xmt Packet Start to			200	nS	100 Mbps
	COL Assert Time			700	nS	10 Mbps
t_{54}	Xmt Packet Stop to			240	nS	100 Mbps
	COL Deassert Time			300	nS	10 Mbps.
t_{55}	nPLEDn Delay Time			25	mS	nPLEDn Programmed for Collision
t_{56}	nPLEDn Pulse Time	80		105	mS	nPLEDn Programmed for Collision
t_{57}	Collision Test Assert Time			5120	nS	
t_{58}	Collision Test Deassert Time			40	nS	
t_{59}	CRS Assert to Transmit			300	nS	100 Mbps
	JAM Packet Start During JAM			800	nS	10 Mbps
t_{60}	COL Rise and Fall Time			10	nS	

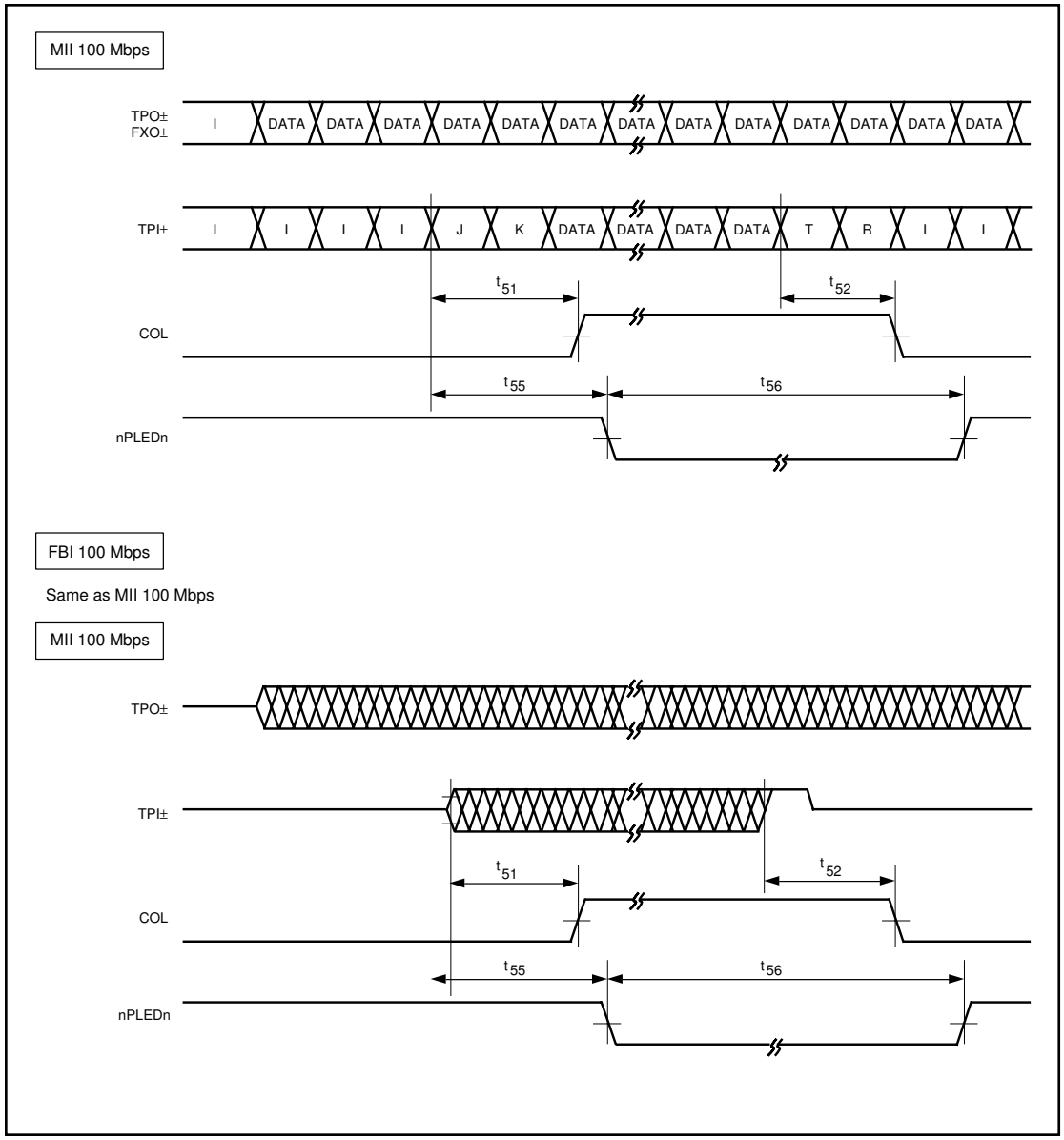


FIGURE 26 - COLLISION TIMING, RECEIVE

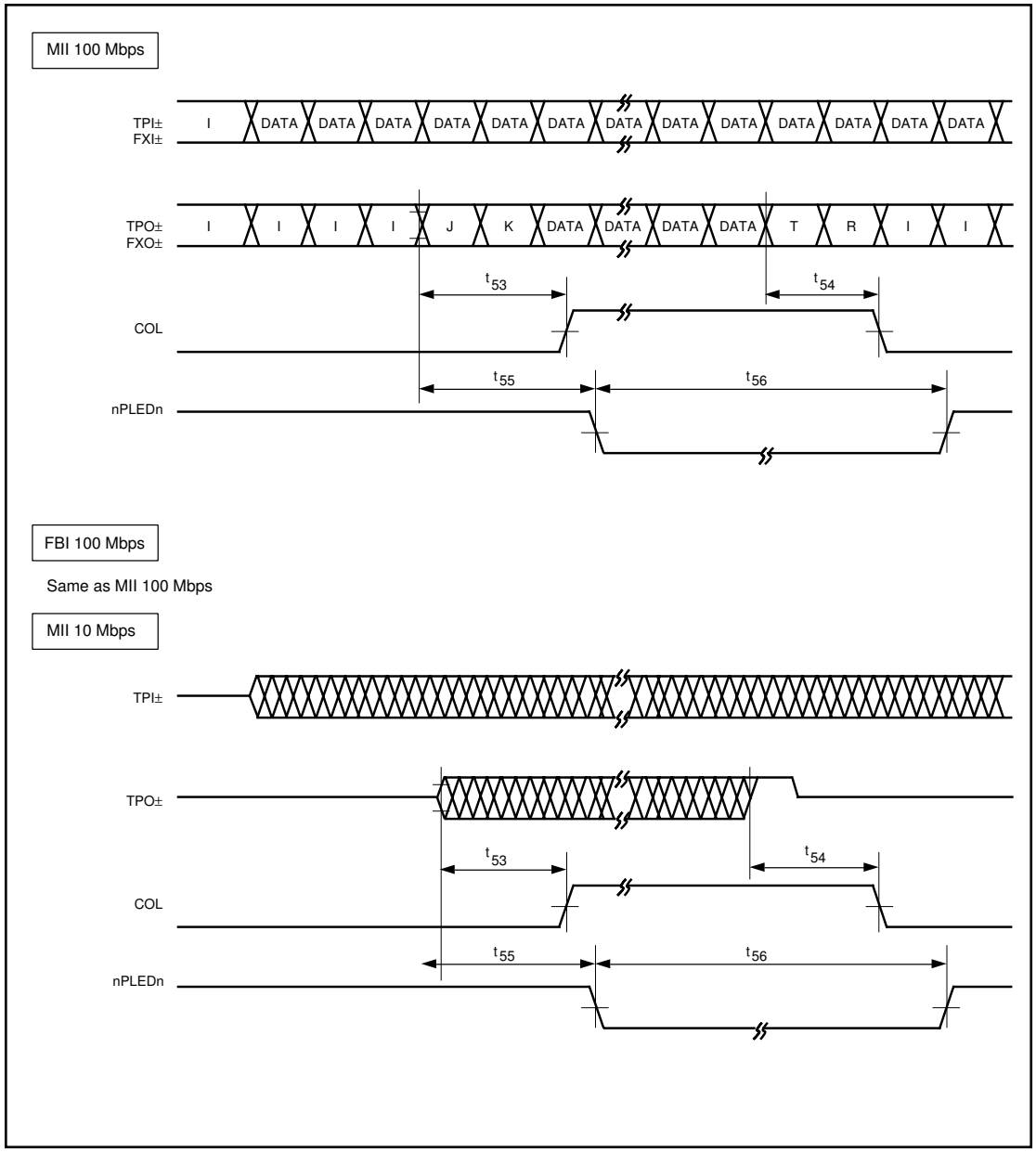


FIGURE 27 - COLLISION TIMING, TRANSMIT

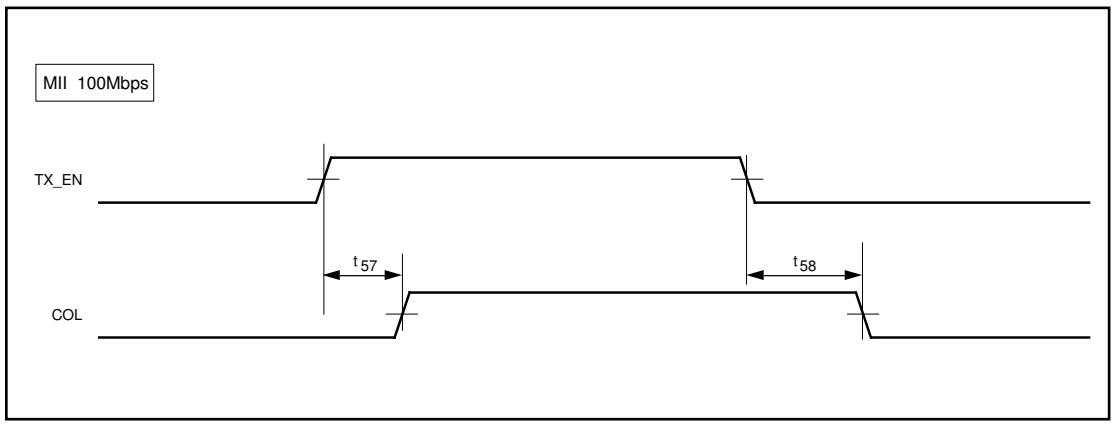


FIGURE 28 - COLLISION TEST TIMING

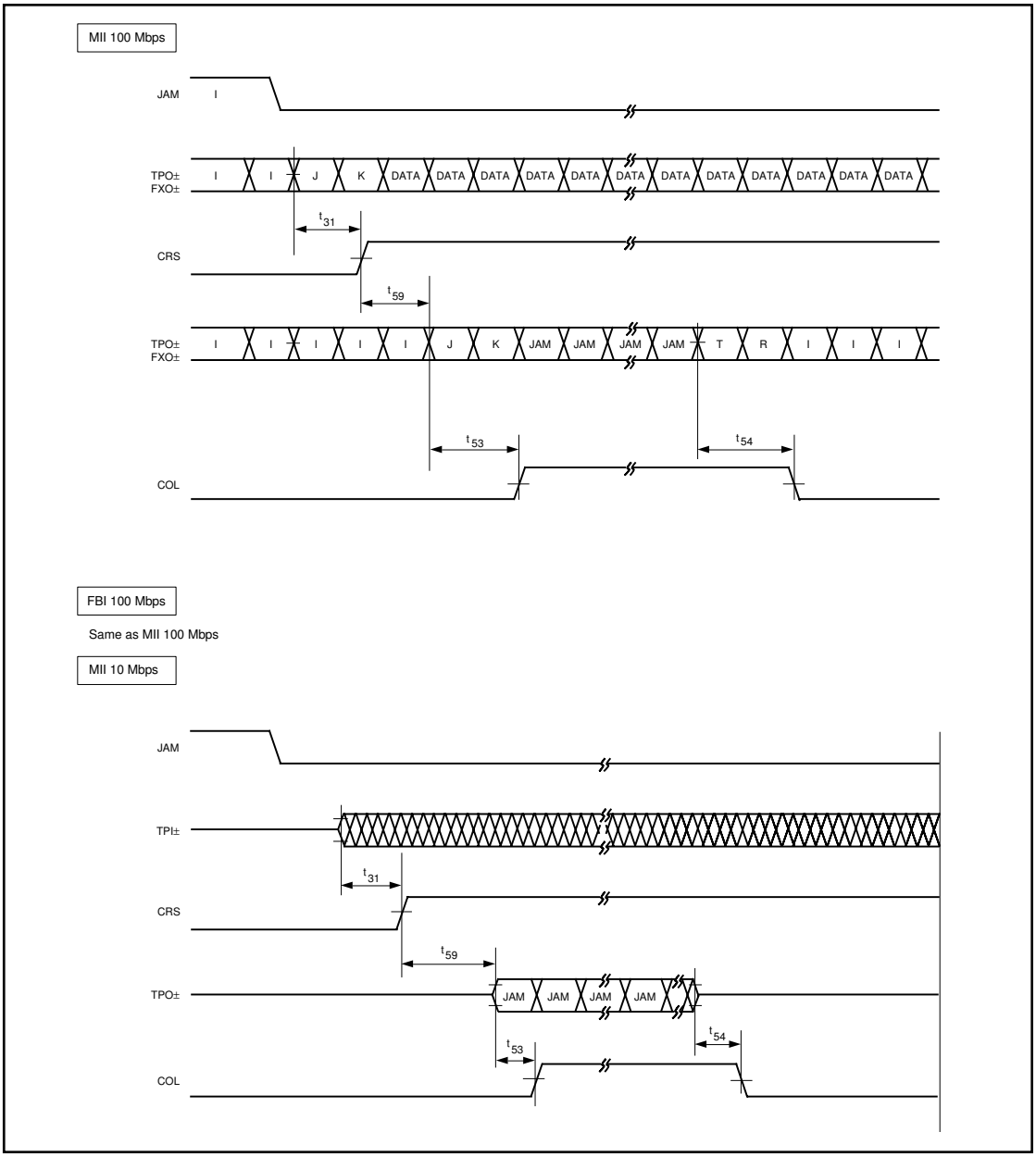


FIGURE 29 - JAM TIMING

LINK PULSE TIMING CHARACTERISTICS

Refer to Figures 30-31 for Timing Diagrams

SYM	PARAMETER	LIMIT			UNIT	CONDITION
		MIN	TYP	MAX		
t_{61}	NLP Transmit Link Pulse Width	See Figure 7			ns	
t_{62}	NLP Transmit Link Pulse Period	8		24	mS	
t_{63}	NLP Receive Link Pulse Width Required For Detection	50			nS	
t_{64}	NLP Receive Link Pulse Minimum Period Required For Detection	6		7	mS	link_test_min
t_{65}	NLP Receive Link Pulse Maximum Period Required For Detection	50		150	mS	link_test_max
t_{66}	NLP Receive Link Pulses Required To Exit Link Fail State	3	3	3	Link Pulses	lc_max
t_{67}	FLP Transmit Link Pulse Width	100		150	nS	
t_{68}	FLP Transmit Clock Pulse To Data Pulse Period	55.5	62.5	69.5	µS	interval_timer
t_{69}	FLP Transmit Clock Pulse To Clock Pulse Period	111	125	139	µS	
t_{70}	FLP Transmit Link Pulse Burst Period	8		22	mS	transmit_link_burst_timer
t_{71}	FLP Receive Link Pulse Width Required For Detection	50			nS	
t_{72}	FLP Receive Link Pulse Minimum Period Required For Clock Pulse Detection	5		25	µS	flp_test_min_timer
t_{73}	FLP Receive Link Pulse Maximum Period Required For Clock Pulse Detection	165		185	µS	flp_test_max_timer

LINK PULSE TIMING CHARACTERISTICS continued

SYM	PARAMETER	LIMIT			UNIT	CONDITION
		MIN	TYP	MAX		
t_{74}	FLP Receive Link Pulse Minimum Period Required For Data Pulse Detection	15		47	µS	data_detect_min_timer
t_{75}	FLP Receive Link Pulse Maximum Period Required For Data Pulse Detection	78		100	µS	data_detect_max_timer
t_{76}	FLP Receive Link Pulses Required To Detect Valid FLP Burst	17		17	Link Pulses	
t_{77}	FLP Receive Link Pulse Burst Minimum Period Required For Detection	5		7	mS	nlp_test_min_timer
t_{78}	FLP Receive Link Pulse Burst Maximum Period Required For Detection	50		150	mS	nlp_test_max_timer
t_{79}	FLP Receive Link Pulses Bursts Required To Detect AutoNegotiation Capability	3	3	3	Link Pulse	
t_{80}	FLP Receive Acknowledge Fail Period	1200		1500	mS	
t_{81}	FLP Transmit Renegotiate Link Fail Period	1200		1500	mS	break_link_timer
t_{82}	NLP Receive Link Pulse Maximum Period Required For Detection After FLP Negotation Has Completed	750		1000	mS	link_fail_inhibit_timer

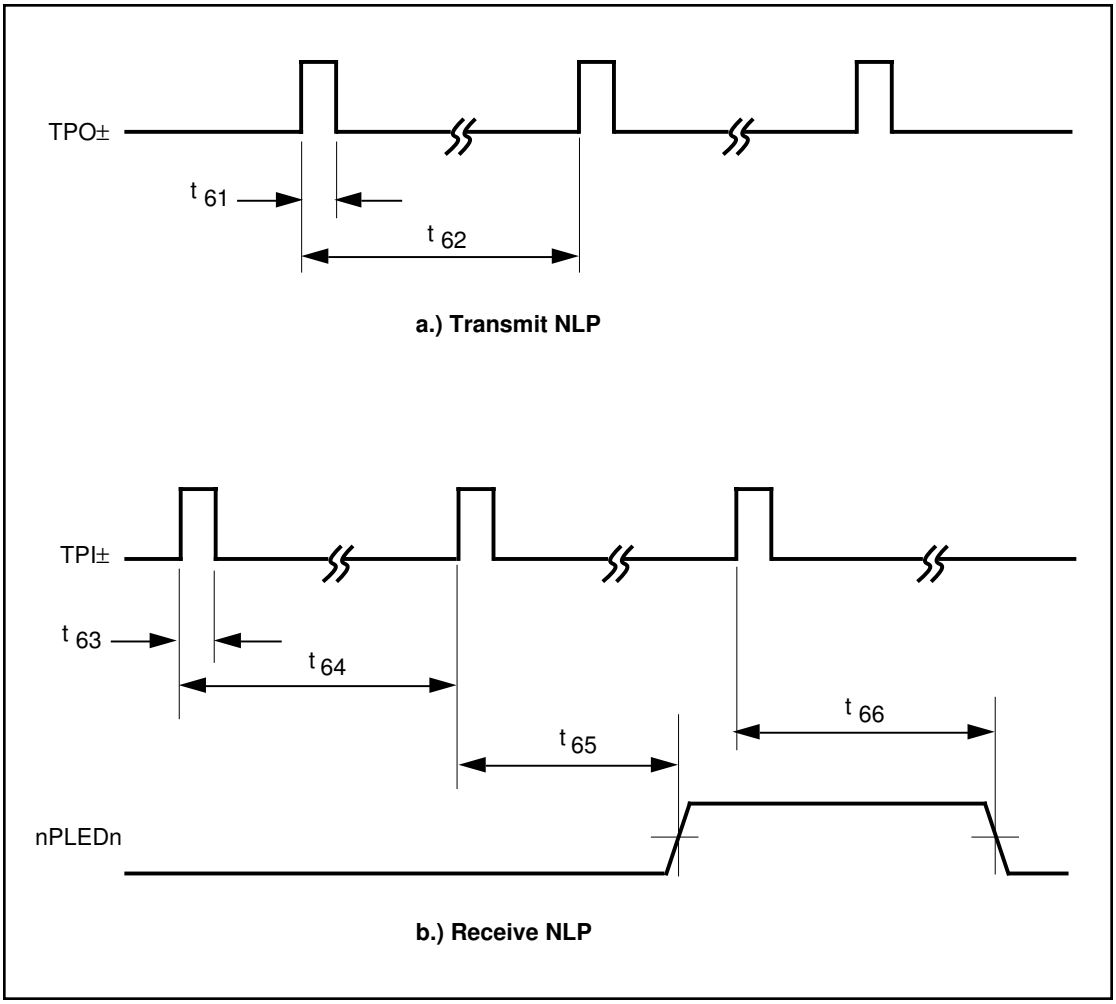
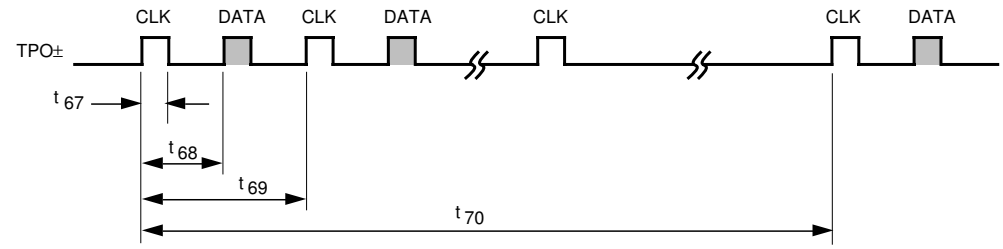
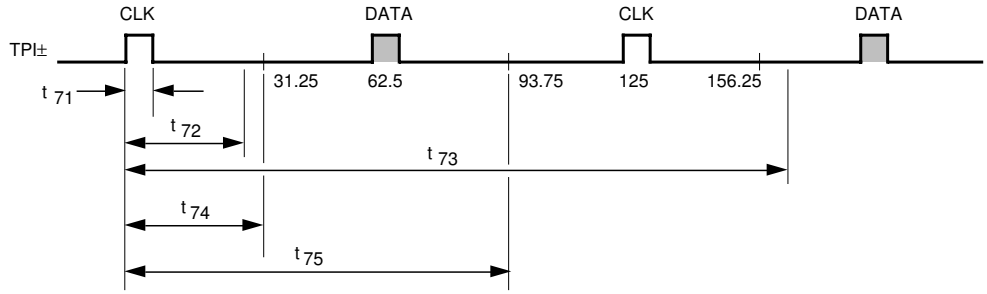


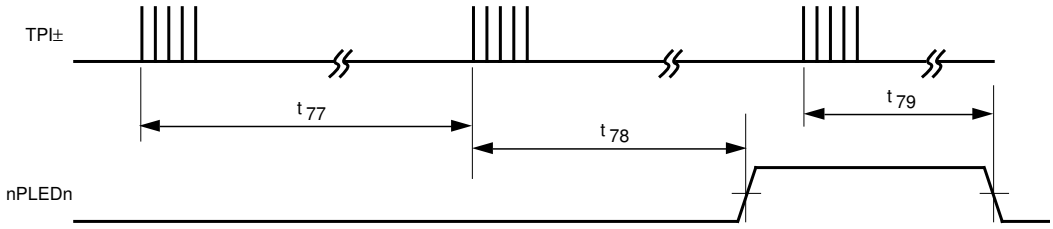
FIGURE 30 - NLP LINK PULSE TIMING



a.) Transmit FLP and Transmit FLP Burst



b.) Receive FLP



c.) Receive FLP Burst

FIGURE 31 - FLP LINK PULSE TIMING

JABBER TIMING CHARACTERISTICS

Refer to Figure 32 for Timing Diagram

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
t_{91}	Jabber Activation Delay Time	50		100	mS	10 Mbps
t_{92}	Jabber Deactivation Delay Time	250		750	mS	10 Mbps

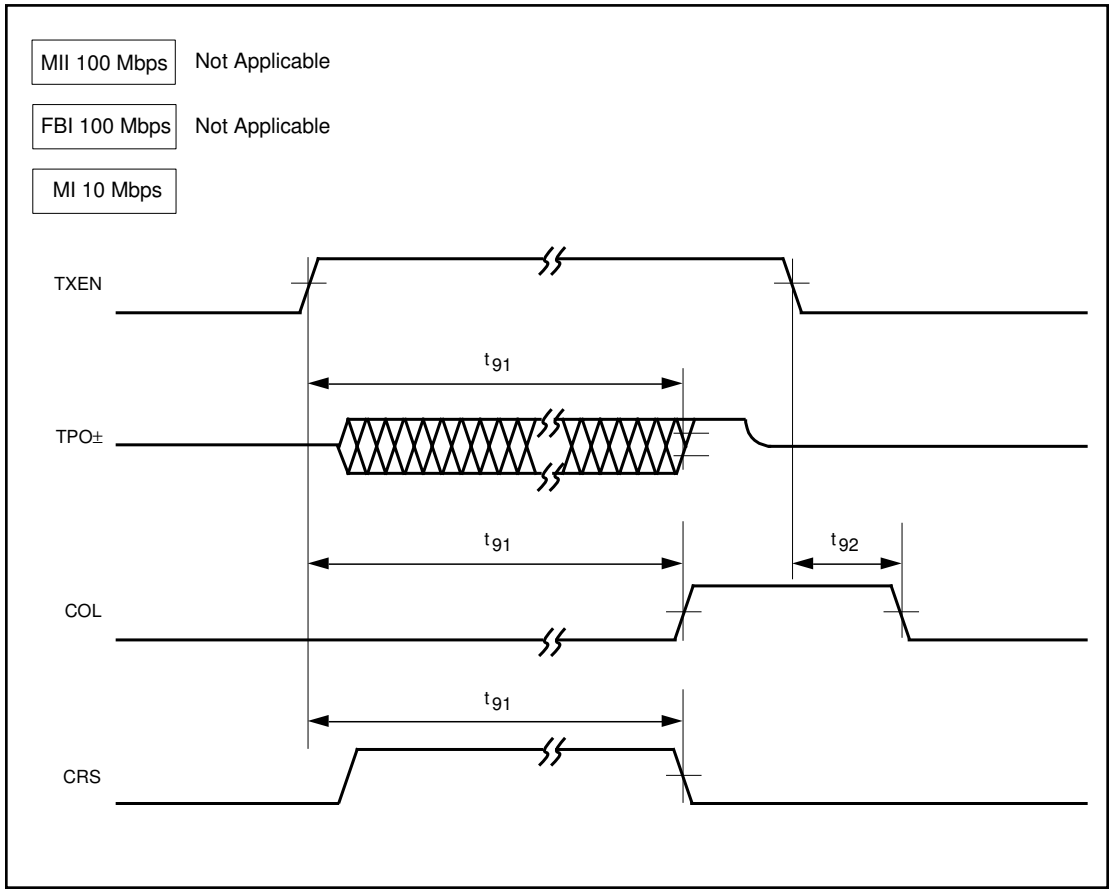


FIGURE 32 - JABBER TIMING

LED DRIVER TIMING CHARACTERISTICS

Refer to Figure 33 for Timing Diagram

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
t_{96}	nPLED[5:0] On Time	80		105	mS	nPLED[5:0] Programmed to Blink
t_{97}	nPLED[5:0] Off Time	80		105	mS	nPLED[5:0] Programmed to Blink

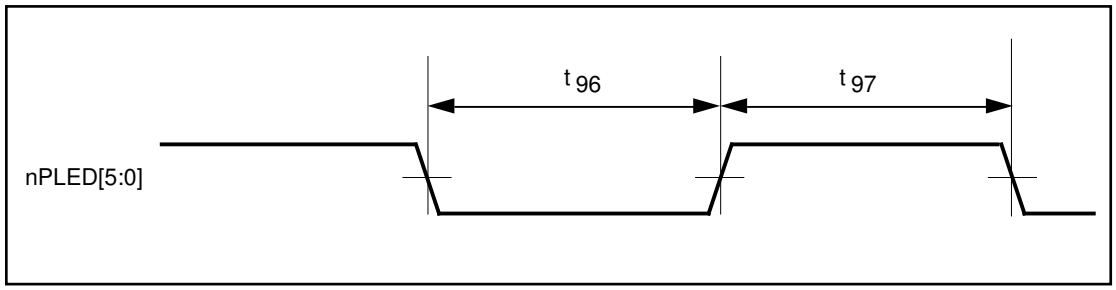


FIGURE 33 - LED DRIVER TIMING

MI SERIAL PORT TIMING CHARACTERISTICS

Refer to Figures 34-35 for Timing Diagrams

SYM	PARAMETER	LIMIT			UNIT	CONDITIONS
		MIN	TYP	MAX		
t_{101}	MDC High Time	20			nS	
t_{102}	MDC Low Time	20			nS	
t_{103}	MDIO Setup Time	10			nS	Write Bits
t_{104}	MDIO Hold Time	10			nS	Write Bits
t_{105}	MDC To MDIO Delay			20	nS	Read Bits
t_{106}	MDIO Hi-Z To Active Delay			20	nS	Write-Read Bit Transition
t_{107}	MDIO Active To HI-Z Delay			20	nS	Read-Write Bit Transition
t_{108}	Frame Delimiter (Idle)	32			Clocks	# of Consecutive MDC Clocks With MDIO=1
t_{109}	End Of Frame To nMDINT Transition			100	nS	
t_{110}	MDC To MDIO Interrupt Pulse Assert Delay			100	nS	
t_{111}	MDC To MDIO Interrupt Pulse Deassert Delay			100	nS	

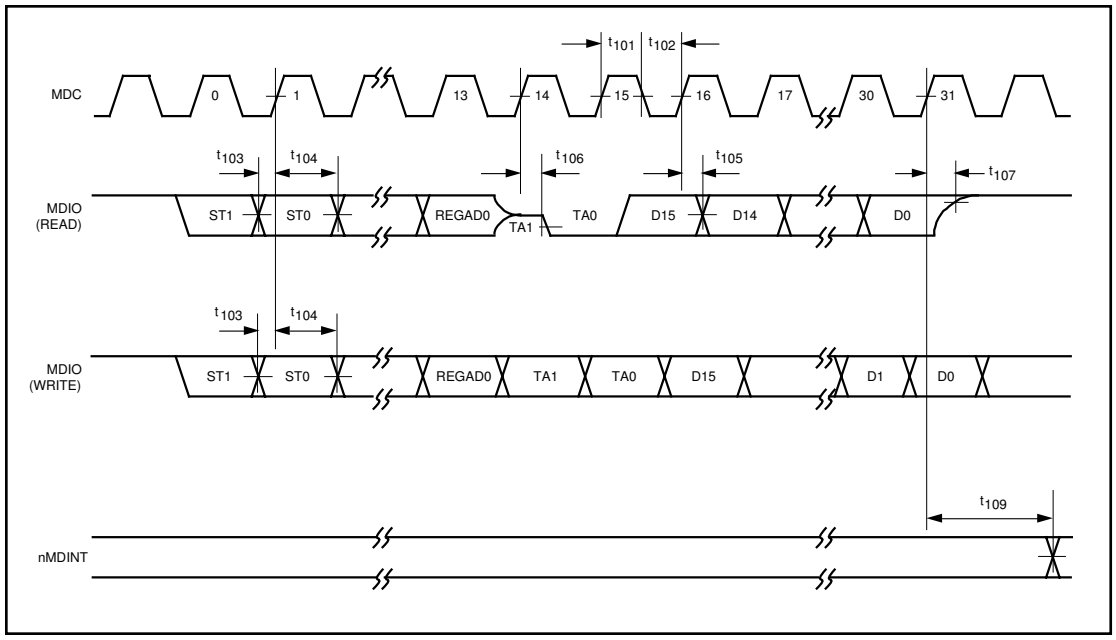


FIGURE 34 - MI SERIAL PORT TIMING

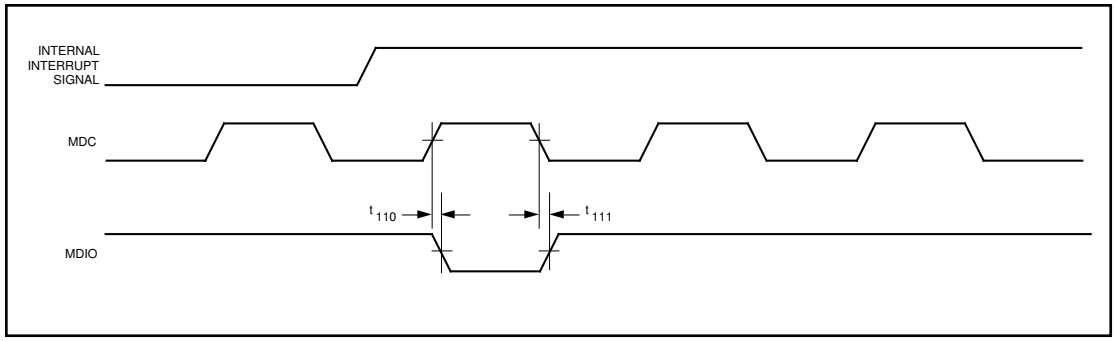
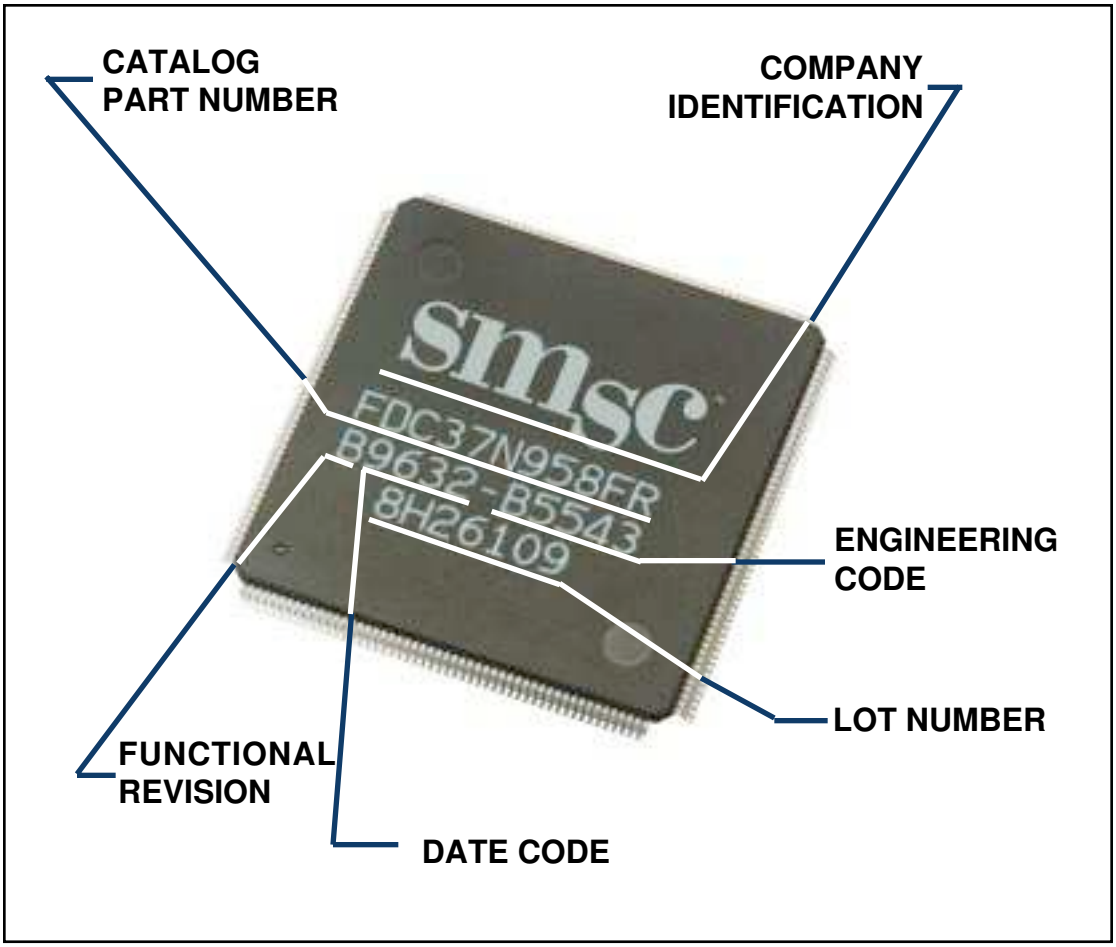


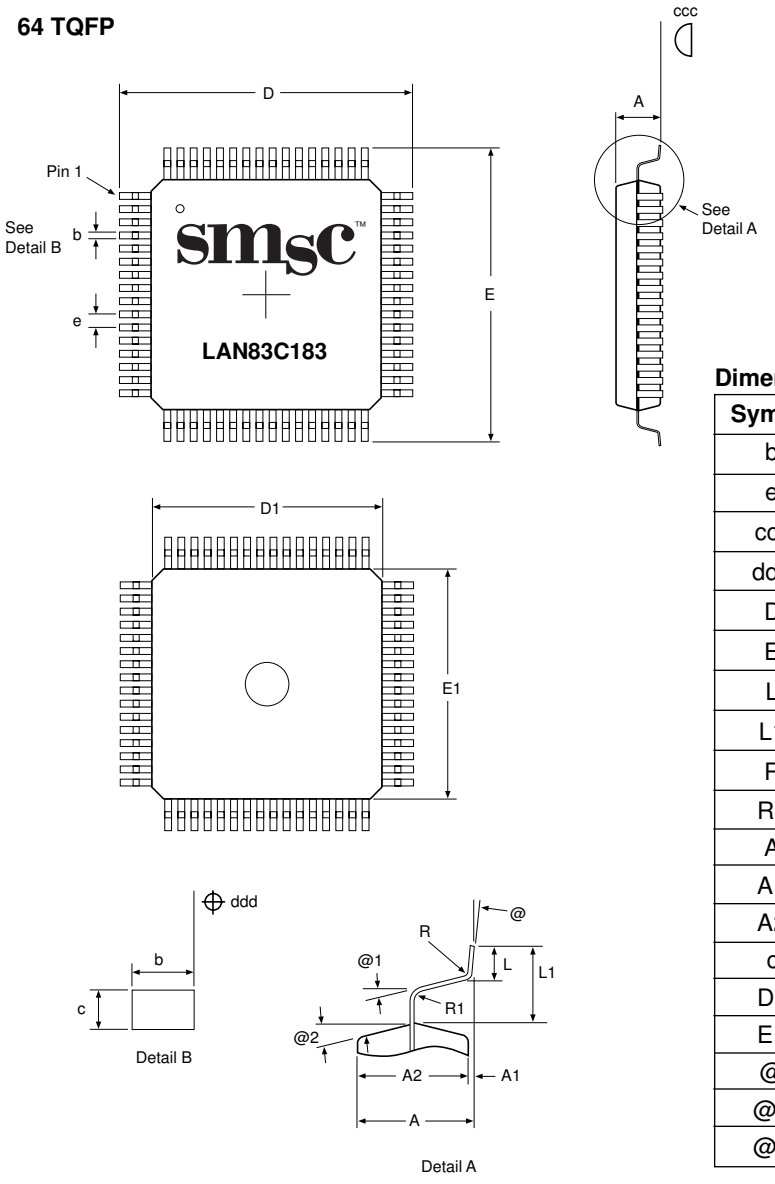
Figure 35 - MDIO Interrupt Pulse Timing

PART MARKING INFORMATION



Surface Mount Packages

64 TQFP



Dimension Table

Symbol	Dimensions
b	0.17 - 0.27
e	0.50 Basic
ccc	Max. 0.08
ddd	Max. 0.08
D	11.85 - 12.15
E	11.85 - 12.15
L	0.45 - 0.75
L1	1.0 Ref
R	0.08 - 0.20
R1	Min. 0.08
A	Max. 1.20
A1	0.05 - 0.15
A2	0.892 - 1.108
c	0.09 - 0.20
D1	9.90 - 10.10
E1	9.90 - 10.10
@	0° - 7°
@1	Min. 0°
@2	12°

Notes

1. **All dimensions are in millimeters.**
2. **Dimensions do not include mold flash. Maximum allowable flash is 0.25.**
3. **All leads are coplanar to a tolerance of 0.08 (ccc). Bent leads to a tolerance of 0.08 (ddd).**

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LAN83C183 Rev. 11/17/98