STANDARD MICROSYSTEMS CORPORATION
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FDC37C651
FDC37C652

SUPER I/O FLOPPY DISK CONTROLLERS

FEATURES

- Super I/O Floppy Disk Controller
  - Licensed CMOS 765B Floppy Disk Controller
  - Advanced Digital Data Separator
  - Two 16450 Compatible UARTs
  - One Bidirectional Parallel Port
  - ChiProtect™ Circuitry on Parallel Port
  - Sophisticated Power Control Circuitry (PCC) Including Multiple Powerdown Modes for Reduced Power Consumption
  - IDE Interface
  - Game Port Select Logic (FDC37C652 Only)
  - Supports Four Floppy Drives Directly
  - 24 mA AT Bus Drivers
  - Low Power CMOS 1.2μ Design
- Licensed CMOS 765B Floppy Disk Controller Core
  - 100% IBM® Compatibility
  - Detects All Overrun and Underrun Conditions
  - 48 mA Drivers and Schmitt Trigger Inputs
  - DMA Enable Logic
  - Data Rate and Drive Control Registers
  - Uses SMC®'s Proven SuperCell™ Technology
- Enhanced Digital Data Separator
  - Low Cost Implementation - 24 MHz Crystal
    - No Filter Components Required
    - Ease of Test and Use, Lower System Cost, and Reduced Board Area
  - 500 Kb/s, 300 Kb/s and 250 Kb/s Data Rates
  - Supports Floppy Disk Drives and Tape Drives
  - Programmable Precompensation Modes
  - Uses SMC's Proven SuperCell Technology
- Serial Ports
  - INS8250-B and NS16450 Compatible UARTs
  - Programmable Baud Rate Generator
  - Modem Control Circuitry
  - Uses SMC's Proven SuperCell Technology
- Parallel Port
  - IBM PC/XT®, PC/AT® and PS/2™ Compatible Bidirectional Parallel Port (FDC37C651 only)
  - Incorporates ChiProtect Circuitry for Protection Against Damage Due to Printer Power-On
  - 24 mA Output Drivers
  - Uses SMC's Proven SuperCell Technology
- IDE Interface
  - On-Chip Decode and Select Logic Compatible with IBM PC/XT and PC/AT Embedded Hard Disk Drives
  - Uses SMC's Proven SuperCell Technology
- 100 Pin QFP Package

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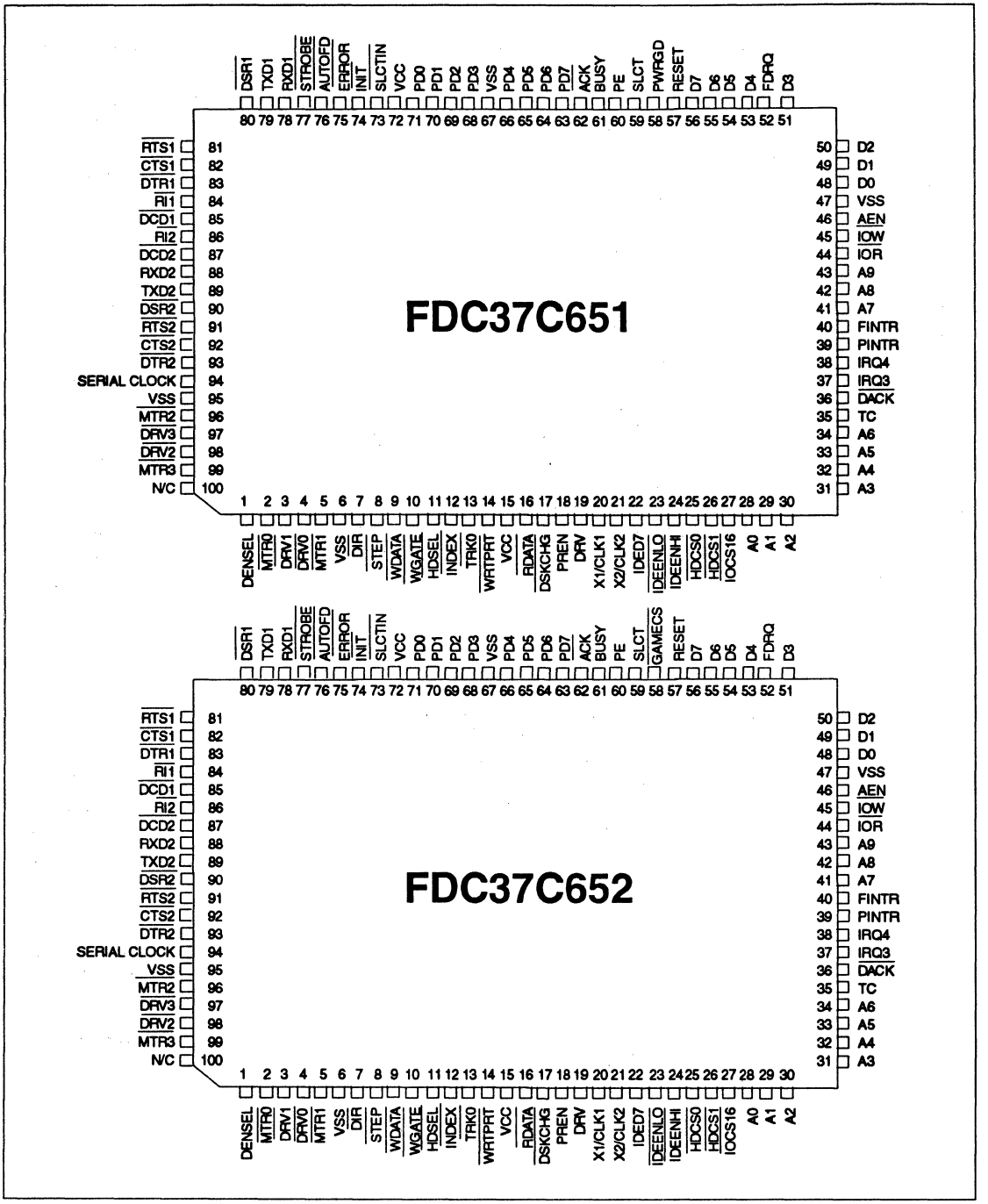
SUPPORT TOOLS

Please contact your salesperson for further information from Standard Microsystems Corporation regarding available System Schematics, Test Software, Support Software and Application Notes.

PIN CONFIGURATION



GENERAL DESCRIPTION

The SMC FDC37C651 and FDC37C652 Super I/O Floppy Disk Controller ICs utilize SMC's proven SuperCell technology for increased product reliability and functionality. The FDC37C651 is optimized for motherboard applications while the FDC37C652 is oriented towards controller card applications.

The FDC37C651 and FDC37C652 incorporate SMC's true CMOS 765B floppy disk controller, advanced digital data separator, two 16540 compatible UARTs, one bidirectional parallel port with ChiProtect circuitry, IDE interface, on-chip 24 mA AT bus drivers, game port chip select (FDC37C652 only), and four floppy direct drive support. The true CMOS 765B core provides 100% compatibility with IBM PC/XT and PC/AT architectures in addition to providing data overflow and underflow protection. The SMC advanced digital data separator incorporates SMC's patented data separator technology allowing for ease of testing and use.

Both on-chip UARTs are compatible with the INS8250-B and NS16450. The parallel port, as well as the IDE interface and game port select logic, are compatible with IBM PC/XT and PC/AT architectures. The FDC37C651 and FDC37C652 incorporate sophisticated power control circuitry (PCC). The PCC supports multiple low power down modes.

The FDC37C651 Floppy Disk Controller incorporates Software Configurable Logic (SCL) for ease of use. Use of the SCL feature allows programmable system configuration of key functions such as the FDC, parallel port, game port and UARTs. The parallel port ChiProtect prevents damage caused by the printer being powered when the FDC37C651 or FDC37C652 is unpowered.

The FDC37C651 and FDC37C652 do not require any external filter components and are, therefore, easy to use and offer lower system cost and reduced board area.

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
		HOST PROCESSOR INTERFACE		
48-51 53-56	Data Bus 0-7	D0-D7	I/O24	The data bus connection used by the host microprocessor to transmit data to and from the FDC37C651. These pins are in a high-impedance state when not in the output mode.
44	$\overline{\text{I/O Read}}$	$\overline{\text{IOR}}$	I	This active low signal is issued by the host microprocessor to indicate a read operation.
45	$\overline{\text{I/O Write}}$	$\overline{\text{IOW}}$	I	This active low signal is issued by the host microprocessor to indicate a write operation.

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
46	Address Enable	AEN	I	Active high Address Enable indicates DMA operations on the host data bus. Used internally to qualify appropriate address decodes.
28-34 41-43	I/O Address	A0-A9	I	These host address bits determine the I/O address to be accessed during $\overline{IOR}$ and $\overline{IOW}$ cycles. These bits are latched internally by the leading edge of $\overline{IOR}$ and $\overline{IOW}$.
52	FDC DMA Request	FDRQ	O24	This active high output is the DMA request for byte transfers of data to the host. This signal is cleared when the host responds with the $\overline{DACK}$ signal going low.
36	$\overline{DMA\ Acknowledge}$	$\overline{DACK}$	I	An active low input acknowledging the request for a DMA transfer of data. This input enables the DMA read or write internally.
35	Terminal Count	TC	I	This active high signal indicates to the FDC37C651 that data transfer is complete.
38	Serial Port Interrupt Request Primary Serial Port Interrupt	IRQ4 PSPIRQ	O24	FDC37C651 (Motherboard application): IRQ4 is the interrupt from the Primary Serial Port (PSP) or Secondary Serial Port (SSP) when the PSP or SSP have their address programmed as COM1 or COM3 (as defined in the Configuration Registers). The appropriate interrupt from the Serial Port is enabled/disabled via the Interrupt Enable Register (IER). The interrupt is reset inactive after interrupt service. It is disabled through IER or hardware reset. FDC37C652 (Adapter application): PSPIRQ is a source of PSP interrupt. Externally, it should be connected to either IRQ3 or IRQ4 on PC/AT via jumpers.

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
37	Serial Port Interrupt Request Register	IRQ3	O24	FDC37C651 (Motherboard application): IRQ3 is the interrupt from the Primary Serial Port (PSP) or secondary Serial Port (SSP) when the PSP or SSP have their address programmed as COM2 or COM4 (as defined in the Configuration Registers). The appropriate interrupt from the Serial Port is enabled/disabled via the Interrupt Enable Register (IER). The interrupt is reset inactive after interrupt service. It is disabled through IER or hardware reset. FDC37C652 (Adapter application): SSPIRQ is a source of SSP interrupt. Externally, it should be connected to either IRQ3 or IRQ4 on PC/AT via jumpers.
	Secondary Serial Port Interrupt	SSPIRQ		
40	Floppy Controller Interrupt Request	FINTR	O24	This interrupt from the Floppy Disk Controller is enabled/disabled via bit 3 of the Drive Control Register.
39	Parallel Port Interrupt Request	PINTR	O24	This interrupt from the Parallel Port is enabled/disabled via bit 4 of the Parallel Port Control Register. If enabled, the interrupt is generated by the $\overline{ACK}$ signal input.
57	Reset	RST	IS	This active high signal resets the FDC37C651 and must be valid for 500 ns minimum. The effect on the internal registers is described in the appropriate section. The configuration registers are not affected by this reset. In the FDC37C652, the falling edge of reset latches the jumper configuration. The jumper select lines must be valid 50 ns prior to this edge.
		FLOPPY DISK INTERFACE		
16	$\overline{\text{Read Disk Data}}$	$\overline{\text{RDATA}}$	IS	Raw serial bit stream from the disk drive. Each falling edge represents a flux transition of the encoded data.

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
10	Write Gate	WGATE	OD48	This active low high current driver allows current to flow through the write head. It becomes active just prior to writing to the diskette.
9	Write Data	WDATA	OD48	This active low high current driver provides the encoded data to the disk drive. Each falling edge causes a flux transition on the media.
11	Head Select	HDSEL	OD48	This high current output selects the floppy disk side for reading or writing. A logic "1" on this pin means side 0 will be accessed, while a logic "0" means side 1 will be accessed.
7	Direction Control	DIR	OD48	This high current output determines the direction of the head movement. A logic "1" on this pin means outward motion, while a logic "0" means inward motion.
8	Step Pulse	STEP	OD48	This active low high current driver issues a low pulse for each track-to-track movement of the head.
17	Disk Change	DSKCHG	IS	This input senses that the drive door is open or that the diskette has possibly been changed since the last drive selection. This input is inverted and read via bit 7 of I/O address 3F7H.
4,3, 98,97	Drive Select 0,1,2,3	DRV0,1,2,3	OD48	These active low open drain outputs select drives 0-3. Four drives can be supported directly.
2,5, 96,99	Motor On 0,1,2,3	MTR0,1,2,3	OD48	These active low open drain outputs select motor drives 0-3. Four drives are supported directly. These motor enable bits are controlled by software via the Digital Output Register (DOR).

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
1	Density Select	DENSEL	OD48	Depending on the DRV input, this open drain output signal can function in two modes: 1. When DRV is low (dual speed spindle), this output selects either 300 RPM or 360 RPM. This output is low when 250/300 Kb/s is selected and high when 500 or 1000 Kb/s is selected. 2. When DRV is high (single speed spindle), the output goes high when 500 Kb/s is selected (high density media).
14	$\overline{\text{Write Protected}}$	$\overline{\text{WRTPRT}}$	IS	This active low Schmitt Trigger input senses from the disk drive that a disk is write protected. Any write command is ignored.
13	$\overline{\text{Track 00}}$	$\overline{\text{TR0}}$	IS	This active low Schmitt Trigger input senses from the disk drive that the head is positioned over the outermost track.
12	$\overline{\text{Index}}$	$\overline{\text{INDEX}}$	IS	This active low Schmitt Trigger input senses from the disk drive that the head is positioned over the beginning of a track, as marked by an index hole.
18	Precompensation Enable	PREN	I	This input selects precompensation mode: Low = Normal; High = Alternate. Precompensation values (shown in Floppy section) depend on the selected data rate and precompensate mode.
19	Drive Type	DRV	I	This input is used to indicate the drive type being used. A logic "0" on this input indicates a two speed spindle motor.
SERIAL PORT INTERFACE				
78,88	Receive Data	RXD1, RXD2	I	Receiver serial data input.

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
79	Transmit Data	TXD1 PCF0	O4	Transmitter serial data output from Primary Serial Port. Parallel Port Configuration Control 0 in FDC37C652 (Adapter application). During Reset active this input is read and latched to define the address of the Parallel Port.
81	$\overline{\text{Request to Send}}$ Parallel Port Configuration Control	$\overline{\text{RTS1}}$ PCF1	O4 I	Active low Request to Send output for Primary Serial Port. Handshake output signal notifies modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hardware reset will reset the $\overline{\text{RTS}}$ signal to inactive mode (high). Forced inactive during loop mode operation. Parallel Port Configuration Control in FDC37C652 (Adapter application). During reset active this input is read and latched to define the address of the Parallel Port.
91	$\overline{\text{Request to Send}}$ Secondary Serial Port Configuration Control	$\overline{\text{RTS2}}$ S2CF0	O4 I	Active low Request to Send output for Secondary Serial Port. Handshake output signal notifies modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of Modem Control Register (MCR). The hardware reset will reset the $\overline{\text{RTS}}$ signal to inactive mode (high). Forced inactive during loop mode operation. Secondary Serial Port Configuration Control 0 in FDC37C652 (Adapter application). During Reset active this input is read and latched to define the address of the Secondary Serial Port.

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
83	Data Terminal Ready	DTR1	O4	Active low Data Terminal Ready output for primary serial port. Handshake output signal notifies modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR). The hardware reset will reset the DTR signal to inactive mode (high). Forced inactive during loop mode operation.
	IDE Configuration Control	IDECF	I	IDE configuration control in FDC37C652 (Adapter application). During Reset active this input is read and latched to enable/disable the IDE.
93	Data Terminal Ready	DTR2	O4	Active low Data Terminal Ready output for secondary serial port. Handshake output signal notifies modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR), The hardware reset will reset the DTR signal to inactive mode (high). Forced inactive during loop mode operation.
	Secondary Serial Port Configuration Control 1	S2CF1	I	Secondary Serial Port Configuration Control 1 in FDC37C652 (Adapter application). During Reset active this input is read and latched to define the address of the Secondary Serial Port.
89	Transmit Data 2	TXD2	O4	Transmitter Serial Data output from Secondary Serial Port.
		TDCCF	I	In FDC37C652 (Adapter application), this input is read and latched during Reset to enable/disable the Floppy Disk Controller.

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
82,92	$\overline{\text{Clear to Send}}$	$\overline{\text{CTS1}}$, $\overline{\text{CTS2}}$	I	Active low Clear to Send inputs for primary and secondary serial ports. Handshake signal which notifies the UART that the modem is ready to receive data. The CPU can monitor the status of $\overline{\text{CTS}}$ signal by reading bit 4 of Modem Status Register (MSR). A $\overline{\text{CTS}}$ signal state change from low to high after the last MSR read will set MSR bit 0 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when $\overline{\text{CTS}}$ changes state. The $\overline{\text{CTS}}$ signal has no effect on the transmitter. Note: Bit 4 of MSR is the complement of $\overline{\text{CTS}}$.
80,90	$\overline{\text{Data Set Ready}}$	$\overline{\text{DSR1}}$, $\overline{\text{DSR2}}$	I	Active low Data Set Ready inputs for primary and secondary serial ports. Handshake signal which notifies the UART that the modem is ready to establish the communication link. The CPU can monitor the status of $\overline{\text{DSR}}$ signal by reading bit 5 of Modem Status Register (MSR). A $\overline{\text{DSR}}$ signal state change from low to high after the last MSR read will set MSR bit 1 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when $\overline{\text{DSR}}$ changes state. Note: Bit 5 of MSR is the complement of $\overline{\text{DSR}}$.
85,87	$\overline{\text{Data Carrier Detect}}$	$\overline{\text{DCD1}}$, $\overline{\text{DCD2}}$	I	Active low Data Set Ready inputs for primary and secondary serial ports. Handshake signal which notifies the UART that carrier signal is detected by the modem. The CPU can monitor the status of $\overline{\text{DCD}}$ signal by reading bit 7 of Modem Status Register (MSR). A $\overline{\text{DCD}}$ signal state change from low to high after the last MSR read will set MSR bit 3 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when $\overline{\text{DCD}}$ changes state. Note: Bit 7 of MSR is the complement of $\overline{\text{DCD}}$.

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
84,86	$\overline{\text{Ring Indicator}}$	$\overline{\text{RI1}}$, $\overline{\text{RI2}}$	I	Active low Ring Indicator input for primary and secondary serial ports. Handshake signal which notifies the UART that the telephone ring signal is detected by the modem. The CPU can monitor the status of $\overline{\text{RI}}$ signal by reading bit 6 of Modem Status Register (MSR). A $\overline{\text{RI}}$ signal state change from low to high after the last MSR read will set MSR bit 2 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when $\overline{\text{RI}}$ changes state. Note: Bit 6 of MSR is the complement of $\overline{\text{RI}}$.
94	Serial Clock	SERIAL CLOCK	O4	The 1.8462 MHz clock generated by dividing the 24 MHz crystal frequency by 13 is output as the serial clock.
		PARALLEL PORT INTERFACE		
73	$\overline{\text{Printer Select Input}}$	$\overline{\text{SLCTIN}}$	OD24	This active low output selects the printer. This is the complement of bit 3 of the Printer Control Register.
74	$\overline{\text{Initiate Output}}$	$\overline{\text{INIT}}$	OD24	This output is bit 2 of the printer control register. This is used to initiate the printer when low.
76	$\overline{\text{Autofeed Output}}$	$\overline{\text{AUTOFD}}$	OD24	This output goes low to cause the printer to automatically feed one line after each line is printed. The $\overline{\text{AUTOFD}}$ output is the complement of bit 1 of the Printer Control Register.
77	$\overline{\text{Strobe Output}}$	$\overline{\text{STROBE}}$	OD24	An active low pulse on this output is used to strobe the printer data into the printer. The $\overline{\text{STROBE}}$ output is the complement of bit 0 of the Printer Control Register.
61	Busy	BUSY	I	This is a status output from the printer, a high indicating that the printer is not ready to receive new data. Bit 7 of the Printer Status Register is the complement of the BUSY input.

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
62	$\overline{\text{Acknowledge}}$	$\overline{\text{ACK}}$	I	A low active output from the printer indicating that it has received the data and is ready to accept new data. Bit 6 of the Printer Status Register reads the $\overline{\text{ACK}}$ input.
60	Paper End	PE	I	Another status output from the printer, a high indicating that the printer is out of paper. Bit 5 of the Printer Status Register reads the PE input.
59	Printer Selected Status	SLCT	I	This high active output from the printer indicates that it has power on. Bit 4 of the Printer Status Register reads the SLCT input.
75	$\overline{\text{Error}}$	$\overline{\text{ERR}}$	I	A low on this input from the printer indicates that there is a error condition at the printer. Bit 3 of the Printer Status register reads the $\overline{\text{ERR}}$ input.
71-68 66-63	Port Data	PD0-PD7	I/O24	The bi-directional parallel data bus is used to transfer information between CPU and peripherals. These signals have high current drive and are capable of sinking 24 mA 0.5V.
		IDE		
23	$\overline{\text{IDE Low Byte Enable}}$	$\overline{\text{IDEENLO}}$ SICF1	O4	This active low signal is used in both the XT and AT mode. In the AT mode, this pin is active when the IDE is enabled and the I/O address is accessing 1F0H-1F7H and 3F6H-3F7H. In the XT mode, this signal is active for accessing 320H-323H, 8 bit programmed I/O or DMA. Primary Serial Configuration 1 in FDC37C652 (Adapter application). Read and latched during Reset active to select the address of the Secondary Serial Port.

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
24	$\overline{\text{IDE High Byte Enable}}$	$\overline{\text{IDEENHI}}$ SICF0	O4	This signal is active low only in the AT mode, and IO16CSB is also active. The I/O addresses for which this pin reacts are 1F0H-1F7H. This pin is not used in XT mode. Primary Serial Configuration 0 in FDC37C652 (Adapter application). Read and latched during Reset active to define the address of the Secondary Serial Port.
25	$\overline{\text{Hard Disk Chip Select}}$	$\overline{\text{HDCS0}}$	O24	This is the Primary Hard Disk Chip select corresponding to addresses 1F0H-1F7H in the AT mode and addresses 320H-323H in the XT mode.
26	$\overline{\text{Hard Disk Chip Select}}$	$\overline{\text{HDCS1}}$	O24	This is the Secondary Hard Disk Chip select corresponding to addresses 3F5H-3F7H in the AT and XT modes.
27	$\overline{\text{I/O 16 Bit Indicator}}$	$\overline{\text{IOCS16}}$ $\overline{\text{HDACK}}$	I	This input indicates, in AT mode only, when 16 bit transfers are to take place. This signal is generated by the hard disk interface. Logic "0" = 16 bit mode; logic "1" = 8 bit mode. In the XT mode, this is the Hard Disk Controller DMA Acknowledge, low active.
22	IDE Data Bit 7	IDED7	I/O24	IDE data bit 7 in the AT mode. IDED7 transfers data at I/O addresses 1F0H-1F7H (R/W), 3F6 (R/W), 3F7(W). IDED7 should be connected to IDE data bit 7. The FDC37C651 functions as a buffer transferring data bit 7 between the IDE device and the host. During I/O read of 3F7H, IDED7 is the FDC disk change bit. In the XT mode, IDE7 is not used.

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	BUFFER TYPE	DESCRIPTION
		MISCELLANEOUS		
58	Power Good	PWRGD	I	In motherboard mode (FDC37C651), this input indicates that the power (V_{CC}) is valid. For device operation, PWRGD must be active. When PWRGD is inactive, all inputs to the FDC37C651 are disconnected and put in a low power mode, all outputs are put into high impedance. The contents of all registers are preserved as long as V_{CC} has a valid value. The driver current drain in this mode drops to ISTBY - standby current. This input has a weak pullup resistor to V_{CC}. In FDC37C652 (Adapter application), this is the Game Port Chip Select output - active low. It will go active when the I/O address is 201H.
	Game Port Chip Select	$\overline{\text{GAMECS}}$		
20	CLOCK 1	X1/CLK1	ICLK	The external connection for a series resonant 24 MHz crystal. A CMOS compatible oscillator is required if crystal is not used.
21	CLOCK 2	X2/CLK2	OCLK	24MHz crystal. If an external clock is used, this pin should not be connected. This pin should not be used to drive any other drivers.
15,72	Power	V_{CC}		+ 5 Volt supply pin.
6,47, 67,95	Ground	GND		Ground pin.

BUFFER TYPE DESCRIPTIONS

BUFFER TYPE	DESCRIPTION
I/O24	Input/output pin. Output 24 mA sink @ 0.4V; source 12 mA @ 2.4V
O24	Output driver with HiZ capability. Sinks 24 mA @ 0.4V; source 12 mA @ 2.4V.
OD48	Open drain outputs, sink 48 mA @ 0.4V.
O4	Output with 4 mA sink @ 0.4V; source 2.0 mA @ 2.4V.
OD24	Output sinks 24 mA @ 0.4V; sources 50μA @ 2.4V.
OCLK	Output to external crystal
ICLK	Input to Crystal Oscillator Circuit (CMOS levels)
I	Input TTL compatible.
IS	Input with Schmitt Trigger.

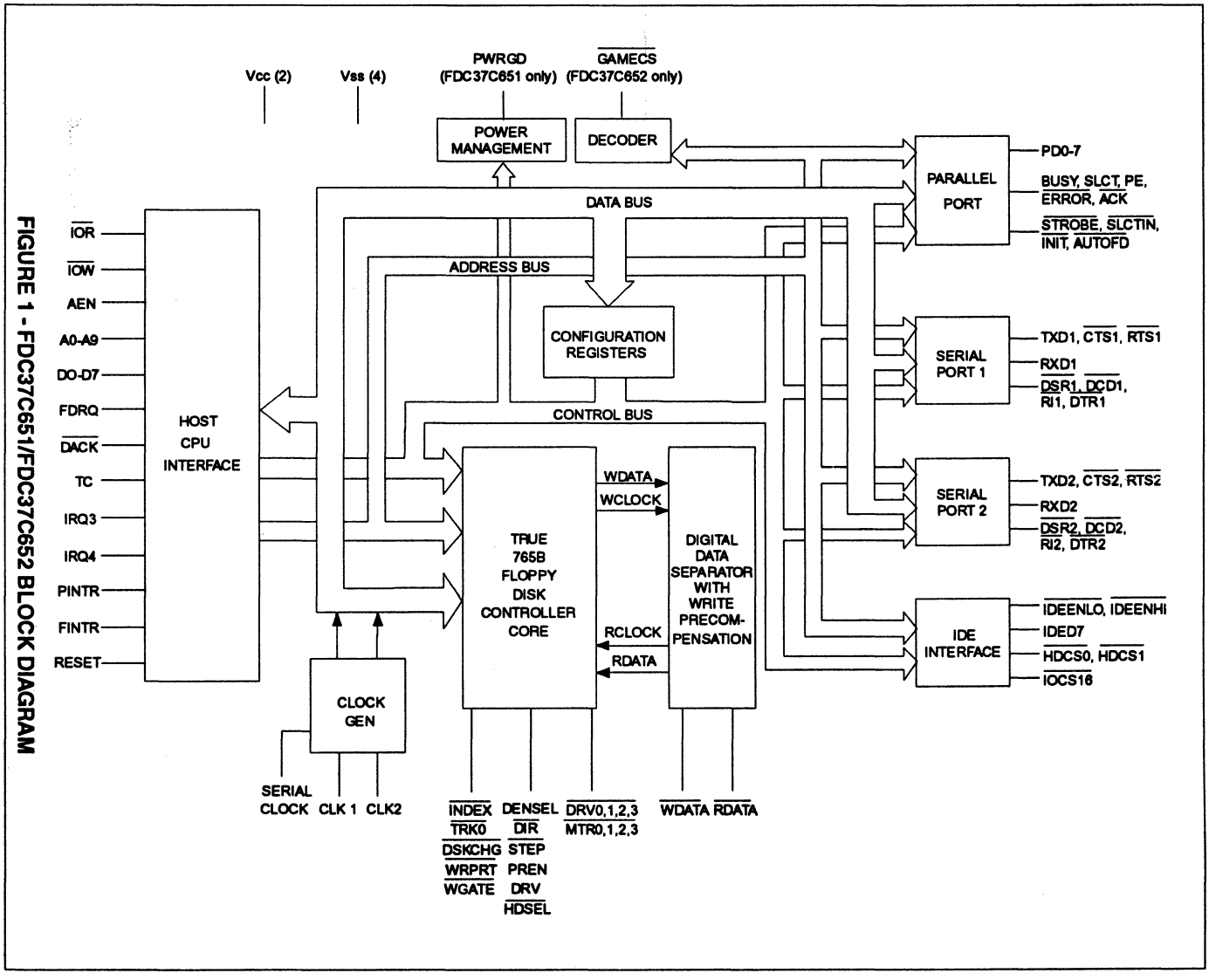


FIGURE 1 - FDC37C651/FDC37C652 BLOCK DIAGRAM

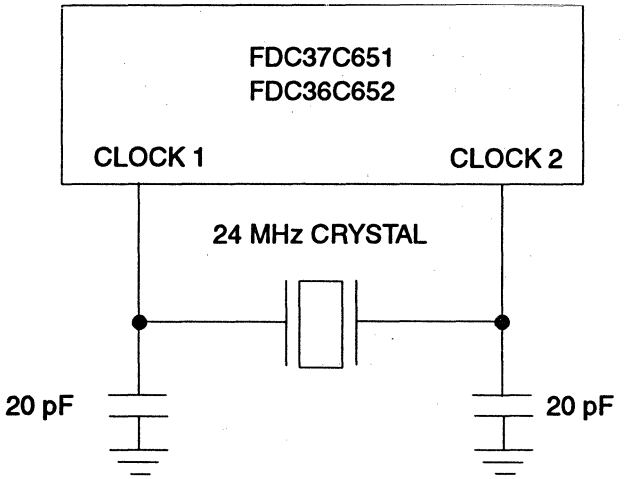
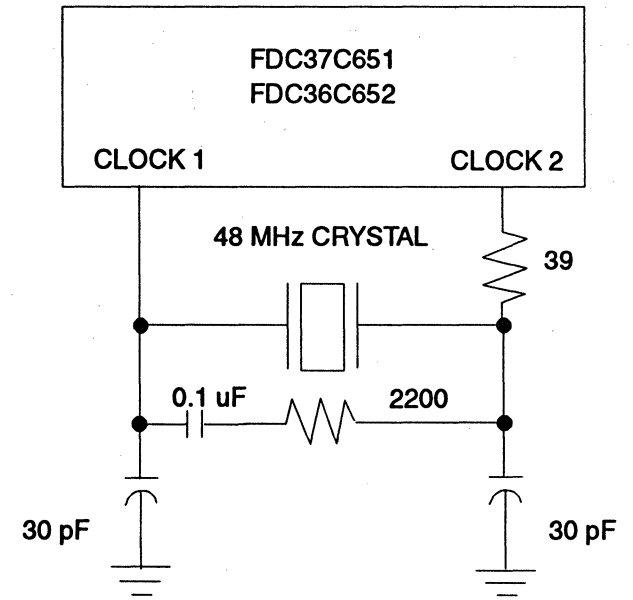


FIGURE 2 - SUGGESTED 24 MHz OSCILLATOR CIRCUIT



NOTE: If stand-by current is not important, the 0.1 uF capacitor can be removed.

FIGURE 3 - SUGGESTED 48 MHz OSCILLATOR CIRCUIT

FUNCTIONAL DESCRIPTION

REGISTERS

The address map, shown below in Table 1, shows the addresses of the different blocks of the Super I/O immediately after power up. The base addresses of the serial and parallel ports can be moved via the configuration registers. Some addresses are used to access more than one register.

Table 1 - FDC Block Addresses

ADDRESS	BLOCK NAME	NOTES
3F0, 3F1	Configuration	
3F2, 3F4, 3F5, 3F7	Floppy Disk	
3F8-3FF	Serial Port Com 1	Address at power up; Note 1
2F8-2FF	Serial Port Com 2	Address at power up; Note 1
278-27A	Parallel Port	Address at power up; Note 1
1F0-1F7, 3F6, 3F7	IDE	AT Mode; Note 2

Note 1: These addresses can be changed in the configuration setup.
Note 2: Addresses 320H-323H and 3F5-3F7H for XT Mode. Selectable in configuration setup.

HOST PROCESSOR INTERFACE

The host processor communicates with the FDC37C651/652 through a series of read/write registers. The port addresses for these registers are shown in Table 1. Register access is accomplished through programmed I/O or DMA transfers. All registers are 8 bits wide except the IDE data register at port 1F0H which is 16 bits wide. All host interface output buffers are capable of sinking a minimum of 24 mA.

FLOPPY DISK CONTROLLER

The Floppy Disk Controller (FDC) provides the interface between a host microprocessor and the floppy disk drives. The FDC integrates the functions of the Formatter/Controller, Digital Data Separator, Write Precompensation and Data Rate Selection logic for an IBM XT/AT compatible FDC. The true CMOS 765B core guarantees 100% IBM PC XT/AT compatibility in addition to providing data overflow and underflow protection.

FLOPPY DISK CONTROLLER INTERNAL REGISTERS

The FDC37C651 and FDC37C652 contain eight internal registers which facilitate the interfacing between the host microprocessor and the disk drive. The eight registers consist of the Data Rate Selection Register, the Main Status Register, Status Registers 0-3, the Data Register, and the Digital Output Register. Table 2 shows the addresses required to access the registers. Registers other than the ones shown are not supported.

Table 2 - Register Access Addresses

ADDRESS	TYPE	REGISTER NAME
3F2	Write only	Digital Output Register
3F4	Read only	Main Status Register
3F5	Read/Write	Data, Status 0-3 Registers
3F7	Write only	Data Rate Selection Register
3F7	Read only	Digital Input Register

Digital Output Register (3F2H - Write Only)

The Digital Output Register provides for selection of the disk drive, control of the disk drive spindle motors, and DMA enable and reset functions. The bits of this register are:

Table 3 - Digital Output Register

BIT NO.	BIT NAME	SYMBOL
Bit 7	Motor Enable 3	MOEN3
Bit 6	Motor Enable 2	MOEN2
Bit 5	Motor Enable 1	MOEN1
Bit 4	Motor Enable 0	MOEN0
Bit 3	DMA and IRQ Enable	DMAEN
Bit 2	Reset FDC	$\overline{\text{RFDC}}$
Bit 1	Drive Select 1	DSEL1
Bit 0	Drive Select 0	DSEL0

The high active Motor Enable 3 to 0 of this register are inverted to drive the $\overline{\text{MTR3-0}}$ outputs. (More than one $\overline{\text{MTRx}}$ output can be active at a time). The decoding used to generate the Drive Select outputs $\overline{\text{DRV0-3}}$ is shown below:

Table 4 - Drive Select Decoding

DIGITAL OUTPUT REGISTER						$\overline{\text{DRV}}$ OUTPUTS			
BIT 7	BIT 6	BIT 5	BIT 4	BIT 1	BIT 0	$\overline{\text{DRV}}$ #0	$\overline{\text{DRV}}$ #1	$\overline{\text{DRV}}$ #2	$\overline{\text{DRV}}$ #3
X	X	X	1	0	0	0	1	1	1
X	X	1	X	0	1	1	0	1	1
X	1	X	X	1	0	1	1	0	1
1	X	X	X	1	1	1	1	1	0

Reset FDC

RESET FDC resets the Floppy Disk Controller only. To initiate a software reset, the user must load the Digital Output Register with bit 2 (RESET FDC) as a logic one. The reset must be removed by the user, writing this bit to a logic zero. RESET FDC will reset the FDC as did the RST, but will not affect the current data rate selection.

DMA and IRQ Enable

This bit qualifies the DMA and IRQ outputs and the $\overline{\text{DACK}}$ input. When this bit is high, DMA, IRQ and $\overline{\text{DACK}}$ are enabled. When low, DMA and IRQ are tri-stated and $\overline{\text{DACK}}$ is not recognized by the chip.

Main Status Register (3F4H - Read Only)

The Main Status Register is an 8-bit register that contains the status information of the FDC, and may be accessed at any time. Only the Main Status Register may be accessed to facilitate the transfer of data between the microprocessor and the FDC. That is, Status Registers 0-3 may be read only after the completion of a command and provide no assistance in the transfer of data between the microprocessor and the FDC. Each time the Main Status Register is accessed, the microprocessor should wait 12 μs if 500 kbits/sec MFM is selected as the data rate and 24 μs if 250 kbits/sec MFM is selected. Refer to Table 5 for the contents of the Main Status Register.

Table 5 - Main Status Register Read (3F4, Read Only)

BIT NO.	BIT NAME	SYMBOL	DESCRIPTION
0	FDD 0 Busy	D0B	A high level on this bit indicates that drive 0 is in the Seek Mode and that the FDC will not accept READ or WRITE commands.
1	FDD 1 Busy	D1B	A high level on this bit indicates that drive 1 is in the Seek Mode and that the FDC will not accept READ or WRITE commands.
2	FDD 2 Busy	D2B	A high level on this bit indicates that drive 2 is in the Seek Mode and that the FDC will not accept READ or WRITE commands.
3	FDD 3 Busy	D3B	A high level on this bit indicates that drive 3 is in the Seek Mode and that the FDC will not accept READ or WRITE commands.
4	FDC Busy	CB	A high level on this bit indicates that a READ or WRITE command is in progress and that the FDC will not accept any other command.
5	Execution Mode	EXM	A high level on this bit indicates that the FDC is in the Execution Phase in Non-DMA Mode. When this bit goes low, the Execution Phase has ended and the Results Phase has begun. This bit operates only in the Non-DMA Mode.
6	Data	DIO	A high level on this bit indicates that the direction of data transfer is from the Data Register to the microprocessor. A low level on this bit indicates that the direction of data transfer is from the microprocessor to the Data Register.
7	Request	RQM	A high level on this bit indicates that the Data Register is ready to send or receive data to or from the microprocessor. Both the DIO and the RQM bits should be used to perform the "ready" and "direction" handshaking functions to the host.

Data Rate Selection Register (3F7H - Write Only)

The Data Rate Selection Register provides support logic that latches the two LSBs of the data bus when port 3F7H is written to. These bits are used to select the desired data rate which, in turn, controls the internal clock generation. When the data rate is switched, the clock is de-glitched to allow for continuous operation. Refer to Table 6 for manipulation of the Data Rate Selection Register.

Table 6 - Data Rate and Precompensation Programming Values

D0[2]	D1[2]	DRVTYP PIN	DATA RATE MFM (Kb/s)	NORMAL PRECOMP[1] (ns)	ALTERNATE PRECOMP[1] (ns)	DENSEL PIN LEVEL	CONTROLLER CLOCKS	
							TO FDC (MCLK)	TO DDS
0	0	X	500	187	125	High	8 MHz	16 MHz
0	1	0	250	187	125	Low	4 MHz	8 MHz
0	1	1	300	208	208	Low	4.8 MHz	9.6 MHz
1	0	0	250	187	125	Low	4 MHz	8 MHz
1	0	1	250	187	125	Low	4 MHz	8 MHz
1	1	0	1000[3]	93.5	62.5	High	16 MHz	32 MHz
1	1	1	1000	93.5	62.5	Low		

1. Normal values when PUMP/PREN pin set low; alternate values when PUMP/PREN set high.
2. D0 and D1 are Data Rate Control Bits.
3. For 1000 Kb/s, a 48 MHz crystal is required to be used. With the use of a 48 MHz crystal, Configuration Register 3 bit 2, CLKEQ48, must be set high to a logic "1". This allows all clock dividers for all data rates to adjust for this double frequency crystal.

Digital Input Register (3F7H - Read Only)

When this register is accessed, DB7 is driven with the inverted value of the $\overline{DCHG}$ input. Bits DB6-DB0 remain in high impedance.

Data Register (3F5H - Read/Write)

The Data Register is an 8-bit register which can be read by or written to by the host CPU. During Command phase, the command code and associated parameters are written to this register. During execution phase, data is read from or written to this register. In result phase, the status of the operation is read from the data register.

Status Registers 0-3 (3F5H - Read Only)

Status Registers 0-3 are each 8 bit registers that contain status information on the FDC and are available only in the Result Phase and may be read only after completing a command. The command that has been executed determines which of the Status Registers will be read. Refer to Tables 7-10 for the contents of Status Registers 0-3.

Table 7 - Status Register 0

BIT NO.	BIT NAME	SYMBOL	DESCRIPTION
0	Unit Select 0	US0	This flag is used to indicate a Drive Unit Number at interrupt.
1	Unit Select 1	US1	This flag is used to indicate a Drive Unit Number at interrupt.
2	Head Select	HS	This flag is used to indicate the state of the head at interrupt.
3	Not Ready	NR	This bit will always be a logic "0", since Drive Ready is always presumed to be true.
4	Equipment Check	EC	A high level on this bit indicates that the Track 0 signal has failed to occur after 77 step pulses (Recalibrate Command).
5	Seek End	SE	A high level on this bit indicates that the FDC has completed the seek command.
6,7	Interrupt Code	IC	The four combinations of these bits indicate four different situations: 7 6 0 0 Normal Termination of command was completed and properly executed. 0 1 Abnormal Termination (AT) of command. Execution of command was started but not successfully completed. 1 0 Invalid Command (IC) issue. Command which was issued was never started. 1 1 Abnormal Termination (AT) of command. During execution of command, the ready signal from drive changed state.

Table 8 - Status Register 1

BIT NO.	BIT NAME	SYMBOL	DESCRIPTION
0	Missing Address Mark	MA	A high level on his bit indicates that the FDC cannot detect the Data Address Mark or the Deleted Data Address Mark. In this case, the MD bit of Status Register 2 is also set to a logic "1".
1	Not Writable	NW	A high level on this bit indicates that, during execution of the WRITE DATA, WRITE DELETED DATA or FORMAT A TRACK Command, the FDC has detected a $\overline{WP}$ signal from the drive, indicating that the diskette is write protected.
2	No Data	ND	A high level on this bit indicates one of three conditions. Either 1) during the execution of the READ DATA, READ DELETED DATA, WRITE DATA, or WRITE DELETED DATA Command, the FDC cannot find the sector specified in the Internal Data Register, or 2) during the execution of the READ ID Command, the FDC cannot read the ID field without an error, or 3) during the execution of the READ A CYLINDER Command, the starting sector cannot be found.
3	(not used)		This bit is not used and is always at a logic "0".
4	Overrun)	OR	A high level on this bit indicates that the FDC has not been serviced by the microprocessor during data transfers within a certain time interval.
5	Data Error	DE	A high level on this bit indicates that the FDC has detected a Cyclic Redundancy Check Error in either the ID field or the data field.
6	(not used)		This bit is not used and is always at a logic "0".
7	End of Cylinder	EN	A high level on this bit indicates that the FDC has tried to access a sector beyond the final sector of a cylinder.

Table 9 - Status Register 2

BIT NO.	BIT NAME	SYMBOL	DESCRIPTION
0	Missing Address Mark in Data Field	MD	A high level on this bit indicates that the FDC, upon reading data from the drive, cannot find a Data Address Mark, or Deleted Data Address Mark.
1	Bad Cylinder	BC	A high level on this bit indicates that the contents of the cylinder on the medium is different from that stored in the Internal Data Register and the contents of the cylinder is FFH. This bit is related to the ND (No Data) bit of Status Register 1.
2	Scan Not Satisfied	SN	A high level on this bit indicates that, during the execution of a SCAN Command, the FDC cannot find a sector on the cylinder which meets the specified condition.
3	Scan Equal Hit	SH	A high level on this bit indicates that, during the execution of a SCAN command, the condition of "equal" has been satisfied.
4	Wrong Cylinder	WC	A high level on this bit indicates that the contents of the cylinder on the medium is different from that stored in the Internal Data Register. This bit is related to the ND (No Data) bit of Status Register 1.
5	Data Error	DE	A high level on this bit indicates that the FDC has detected a Cyclic Redundancy Check Error in the data field.
6	Control Mark	CM	A high level on this bit indicates that, during the execution of the READ DATA or SCAN Command, the FDC has encountered a sector which contains a Deleted Data Address Mark.
7	(not used)		This bit is not used and is always at a logic "0".

Table 10 - Status Register 3

BIT NO.	BIT NAME	SYMBOL	DESCRIPTION
0	Unit Select 0	US0	This bit is used to indicate the status of the Unit Select 0 signal to the drive.
1	Unit Select 1	US1	This bit is used to indicate the status of the Unit Select 1 signal to the drive.
2	Head Address	HD	This bit is used to indicate the status of the Side Select signal to the drive.
3			This bit is always a logic 1.
4	Track 0	T0	This bit is used to indicate the status of the Track 0 signal to the drive.
5	Ready	RY	This bit is always at a logic "1".
6	$\overline{\text{Write Protected}}$	$\overline{\text{WP}}$	This bit is used to indicate the status of the $\overline{\text{WRITE PROTECTED}}$ signal from the drive.
7	Fault	FT	This bit is always a logic "0".

Digital Data Separator

The Data Separator portion of the Floppy Disk Controller is based on the Standard Microsystems FDC92C39. It performs the complete data separation function of separating the data and clock pulses from the FM and MFM encoded data. In addition, it contains the Automatic Write Precompensation Logic necessary when writing to the inner and outer tracks of the drive. The encoded Write Data signal is synchronized to the input clock and is clocked through an internal shift register. The taps out of this shift register enable precompensation of the signal if selected.

Polling Routine

Following a reset, the FDC automatically begins polling the drives. The drives are polled every 1.024 ms. For mini-floppies, the polling rate is 2.048 ms. If DMAEN is not valid by 1 ms after reset becomes inactive, then IRQ may already be set and pending when enabled onto the bus.

FDC Power Down Mode (FDC37C651 Only)

The FDC may be placed into the power down mode through the use of the configuration registers. In the power down mode, the FDC core is halted, and the 48 mA drivers to the diskette are inactive. Power down mode is exited by writing to the Configuration Register.

COMMAND SEQUENCE

The FDC is capable of performing 18 different commands. Each command is initiated by a multi-byte transfer from the processor, and the result after execution of the command may also be a multi-byte transfer back to the processor. Because of this multi-byte interchange of information between the FDC and the processor, it is convenient to consider each command as consisting of three phases:

Command Phase: The FDC receives all information required to perform a particular operation from the processor.

Execution Phase: The FDC performs the operation it was instructed to do.

Result Phase: After completion of the operation, status and other housekeeping information is made available to the processor.

Table 11 - Description of Command Symbols

SYMBOL	NAME	DESCRIPTION
A_0	Address Line 0	A_0 controls selection of the Main Status Register (A_0 = 0) or the Data Register (A_0 = 1).
C	Cylinder Number	C stands for the current/selected Cylinder (track) number 0 through 255 of the medium.
D	Data	D stands for the data pattern which is going to be written into a sector.
D_7 - D_0	Data Bus	8-bit Data bus; D_7 is the most significant bit, and D_0 is the least significant bit.
DTL	Data Length	When N is defined as 00, DTL stands for the data length which users are going to read out or write into the sector.
EOT	End of Track	EOT is the final Sector number on a Cylinder. During Read or Write operation the FDC will stop data transfer after a sector number equal to EOT.
GPL	Gap Length	GPL stands for the length of Gap 3. During Read/Write commands, this value determines the number of bytes that VCO's will stay low after two CRC bytes. During Format command GPL determines the size of Gap 3.
H	Head Address	H stands for head number 0 or 1, as specified in the ID field.
HD	Head	HD stands for a selected head number 0 or 1 and controls the polarity of pin 27. (H = HD in all command words).
HLT	Head Load Time	HLT stands for the head load time in the FDC (2 to 254 ms in 2 ms increments).

Table 11 - Description of Command Symbols

SYMBOL	NAME	DESCRIPTION
HUT	Head Unload Time	HUT stands for the head unload time after a read or write operation has occurred (16 to 240 ms in 16 ms increments).
MF	FM or MFM Mode	If MF is low, FM mode is selected, and if it is high, MFM mode is selected.
MT	Multi-Track	If MT is high, a multi-track operation is to be performed. If MT = 1 after finishing Read/Write operation on side 0, the FDC will automatically start searching for sector 1 on side 1.
N	Number	N stands for the number of data bytes written in a sector.
NCN	New Cylinder Number	NCN stands for a new Cylinder number, which is going to be reached as a result of the Seek operation. Desired position of head.
ND	Non-DMA Mode	ND stands for operation in the Non-DMA Mode.
PCN	Present Cylinder Number	PCN stands for the Cylinder number at the completion of SENSE INTERRUPT STATUS Command. Position of Head at present time.
R	Record	R is the Sector number which will be read or written.
R/W	Read/Write	R/W is the Read (R) or Write (W) signal.
SC	Sector	SC indicates the number of Sectors per Cylinder.
SK	Skip	SK stands for Skip Deleted Data Address Mark.
SRT	Step Rate Time	SRT is the Stepping Rate for the FDC. The stepping rate applies to all drives. The stepping rate is programmable from 1 to 16 ms in 1 ms increments. F_H = 1 ms, E_H = 2 ms, etc.
ST0 ST1 ST2 ST3	Status 0 Status 1 Status 2 Status 3	ST0-ST3 stand for one of four registers which store the status information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the main status register (selected by A_0 = 0). ST0-ST3 may be read only after a command has been executed and contain information relevant to that particular command.
STP		During a Scan operation, if STP = 1, the data in contiguous sectors is compared byte by byte with data sent from the processor (or DMA); if STP = 2, then alternate sectors are read and compared.
US0, US1	Unit Select	US stands for a selected drive (0 or 1).

INSTRUCTION SET

Table 12 lists the required parameters and the results associated with each command that the FDC is capable of performing. Refer to Table 11 for explanations of the various symbols used.

Table 12 - Instruction Set [1] [2] [3]

READ DATA										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	MT	MF	SK	0	0	1	1	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	——— C ———								Sector ID information prior to Command execution. The 4 bytes are compared against header on Floppy Disk.
	W	——— H ———								
	W	——— R ———								
	W	——— N ———								
	W	——— EOT ———								
	W	——— GPL ———								
	W	——— DTL ———								
Execution										Data transfer between the FDD and main system.
Result	R	——— ST0 ———								Status information after Command execution.
	R	——— ST1 ———								
	R	——— ST2 ———								
	R	——— C ———								Sector ID information after Command execution.
	R	——— H ———								
	R	——— R ———								
	R	——— N ———								

[1] Symbols used in this table are described in the beginning of this section

[2] A_0 should equal binary 1 for all operations.

[3] X = Don't care, usually made to equal binary 0.

READ DELETED DATA										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	MT	MF	SK	0	1	1	0	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution. The 4 bytes are compared against header on Floppy Disk.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and main system.
Result	R	ST0								Status information after Command execution.
	R	ST1								
	R	ST2								
	R	C								Sector ID information after Command execution.
	R	H								
	R	R								
	R	N								

WRITE DATA										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	MT	MF	0	0	0	1	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution. The 4 bytes are compared against header on Floppy Disk.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the main system and FDD.
Result	R	ST0								Status information after Command execution.
	R	ST1								
	R	ST2								
	R	C								Sector ID information after Command execution.
	R	H								
	R	R								
	R	N								

WRITE DELETED DATA									
		DATA BUS							
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	MT	MF	0	0	1	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution. The 4 bytes are compared against header on Floppy Disk.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the main system and FDD.
Result	R	ST0								Status information after Command execution.
	R	ST1								
	R	ST2								
	R	C								Sector ID information after Command execution.
	R	H								
	R	R								
	R	N								

READ A TRACK									
		DATA BUS							
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	0	MF	SK	0	0	0	1	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data transfer between the FDD and main system. FDC reads all data fields from index hole to EOT.
Result	R	ST0								Status information after Command execution.
	R	ST1								
	R	ST2								
	R	C								Sector ID information after Command execution.
	R	H								
	R	R								
	R	N								

READ ID									
		DATA BUS							
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	0	MF	0	0	1	0	1	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
Execution										The first correct ID information on the Cylinder is stored in Data Register
Result	R	ST0								Status information after Command execution.
	R	ST1								
	R	ST2								
	R	C								Sector ID information read during Execution Phase from Floppy Disk
	R	H								
	R	R								
	R	N								

FORMAT A TRACK										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	0	MF	0	0	1	1	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	N								Bytes/Sector
	W	SC								Sectors/Track
	W	GPL								Gap 3
	W	D								Filler Byte
Execution										FDC formats an entire track
Result	R	ST0								Status information after Command execution.
	R	ST1								
	R	ST2								
	R	(UNDEFINED)								In this case, the ID information has no meaning
	R	(UNDEFINED)								
	R	(UNDEFINED)								
	R	(UNDEFINED)								

SCAN EQUAL									
		DATA BUS							
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	MT	MF	SK	1	0	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	STP								
Execution										Data compared between the FDD and main system.
Result	R	ST0								Status information after Command execution.
	R	ST1								
	R	ST2								
	R	C								Sector ID information after Command execution.
	R	H								
	R	R								
	R	N								

SCAN LOW OR EQUAL										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	MT	MF	SK	1	1	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	STP								
Execution										Data compared between the FDD and main system.
Result	R	ST0								Status information after Command execution.
	R	ST1								
	R	ST2								
	R	C								Sector ID information after Command execution.
	R	H								
	R	R								
	R	N								

SCAN HIGH OR EQUAL										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	MT	MF	SK	1	1	1	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution.
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	STP								
Execution										Data compared between the FDD and main system.
Result	R	ST0								Status information after Command execution.
	R	ST1								
	R	ST2								
	R	C								Sector ID information after Command execution.
	R	H								
	R	R								
	R	N								

RECALIBRATE										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	0	0	0	0	0	1	1	1	Command Codes
	W	X	X	X	X	X	0	US1	US0	
Execution										Head retracted to Track 0.

SENSE INTERRUPT STATUS										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	0	0	0	0	1	0	0	0	Command Codes
	W									
Result	W	STO								FDC status information at the end of seek-operation.
	W	PCN								

SPECIFY									
		DATA BUS							
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	0	0	0	0	0	0	1	1	Command Codes
	W	SRT				HUT				
	W	HLT							ND	

SENSE DRIVE STATUS									
		DATA BUS							
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	0	0	0	0	0	1	0	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
Result	W	ST3								Status information about FDD

SEEK									
		DATA BUS							
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	0	0	0	0	1	1	1	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
Execution	W	NCN								Head positioned over proper cylinder on diskette

INVALID CODES									
		DATA BUS							
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	——— Invalid Codes ———								Invalid Command Codes (NoOp - FDC goes into Standby State)
Result	R	——— ST0 ———								ST0 = 80_H

SOFTWARE RESET									
		DATA BUS							
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	0	0	1	1	0	1	1	0	Command Codes
Execution										Same as hardware reset

RETURN VERSION									
		DATA BUS							
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
COMMAND	W	X	X	X	1	0	0	0	0	Command Codes
Result	R	1	0	0	*1	0	0	0	0	*Indicates B-type product

Read Data

A set of nine (9) byte words are required to place the FDC into the Read Data Mode. After the Read Data command has been issued, the FDC loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the Specify Command), and begins reading ID Address Marks and ID fields. When the current sector number ("R") stored in the ID Register (IDR) compares with the sector number read off the diskette, then the FDC outputs data (from the data field) byte-by-byte to the main system via the data bus.

After completion of the read operation from the current sector, the Sector Number is incremented by one, and the data from the next sector is read and output on the data bus. This continuous read function is called a "Multi-Sector Read Operation". The Read Data Command may be terminated by the receipt of a Terminal count signal. TC should be issued at the same time that the $\overline{\text{DACK}}$ for the last byte of data is sent. Upon receipt of this signal, the FDC stops outputting data to the processor, but will continue to read data from the current sector, check CRC (Cyclic Redundancy Count) bytes, and then, at the end of the sector, terminate the Read Data Command.

The amount of data which can be handled with a single command to the FDC depends upon MT (Multi-Track), MF (MFM/FM), and N (Number of Bytes/Sector). Table 13 shows the Transfer Capacity.

Table 13 - Transfer Capacity

Multi-Track MT	MFM/FM MF	Bytes/Sector N	Maximum Transfer Capacity (Bytes/Sector) X (Number of Sectors)	Final Sector Read from Diskette
0	0	00	(128) x (26) = 3,328	26 at Side 0
0	1	01	(256) x (26) = 6,656	or 26 at Side 1
1	0	00	(128) x (52) = 6,656	26 at Side 1
1	1	01	(256) x (52) = 13,312	
0	0	01	(256) x (15) = 3,840	15 at Side 0
0	1	02	(512) x (15) = 7,680	or 15 at Side 1
1	0	01	(256) x (30) = 7,680	15 at Side 1
1	1	02	(512) x (30) = 15,360	
0	0	02	(512) x (8) = 4,096	8 at Side 0
0	1	03	(1024) x (8) = 8,192	or 8 at Side 1
1	0	02	(512) x (16) = 8,192	8 at Side 1
1	1	03	(1024) x (16) = 16,384	

The "multi-track" function (MT) allows the FDC to read data from both sides of the diskette. For a particular cylinder, data will be transferred starting at Sector L, Side 0 and completing at Sector L, Side 1 (Sector L is the last sector on the side). Please note that this function pertains to only one cylinder (the same track) on each side of the diskette.

When N = 0, the DTL defines the data length which the FDC must treat as a sector. If DTL is smaller than the actual data length in a Sector, the data beyond DTL in the Sector is not sent to the Data Bus. The FDC reads (internally) the complete Sector performing the CRC check, and depending upon the manner of command termination, may perform a Multi-Sector Read Operation. When N is non-zero, then DTL has no meaning and should be set to FF Hexadecimal.

At the completion of the Read Data command, the head is not unloaded until after the Head Unload Time Interval (specified in the Specify Command) has elapsed. If the processor issues another command before the head unloads, then the head settling time may be saved between subsequent reads. This time out is particularly valuable when a diskette is copied from one drive to another.

If the FDC detects the Index Hole twice without finding the right sector, (indicated in "R"), then the FDC sets the ND (No Data) flag in Status Register 1 to a 1 (high), and terminates the Read Data Command. Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.

After reading the ID and Data Fields in each sector, the FDC checks the CRC bytes. If a read error is detected (incorrect CRC in ID field), the FDC sets he DC (Data Error) flag in Status Register 1 to a 1 (high), and if a CRC error occurs in the Data Field the FDC also sets the DD (Data Error in Data field) flag in Status Register 2 to a 1 (high), and terminates the Read Data Command. Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.

If the FDC reads a Deleted Data Address Mark from the diskette, and the SK bit (bit D5 in the first Command Word is not set (SK = 0) then the FDC sets he CM (Control Mark) flag in Status Register 2 to a 1 (high), and terminates the Read Data Command, after reading all the data in the Sector. If SK = 1, the FDC skips the sector with the Deleted Data Address Mark and reads the next sector. The CRC bits in the deleted data field are not checked when SK = 1.

During disk data transfers between the FDC and the processor, via the data bus, the FDC must be serviced by the processor every 27 μs in the FM Mode, and every 13 μs in the MFM Mode, or the FDC sets the OR (Over Run) flag in Status Register 1 to a 1 (high), and terminates the Read Data Command.

If the processor terminates a read (or write) operation in the FDC, then the ID information in the Result Phase is dependent upon the state of the MT bit and EOT byte. Table 14 shows the value for C, H, R, and N, when the processor terminates the Command.

Table 14 - ID Information in Processor - Terminated Command

MT	HD	Final Sector Transferred to Processor	ID Information at Result Phase			
			C	H	R	N
0	0	Less than EOT	NC	NC	R + 1	NC
	0	Equal to EOT	C + 1	NC	R = 01	NC
	1	Less than EOT	NC	NC	R + 1	NC
	1	Equal to EOT	C + 1	NC	R = 01	NC
1	0	Less than EOT	NC	NC	R + 1	NC
	0	Equal to EOT	NC	LSB	R = 01	NC
	1	Less than EOT	NC	NC	R + 1	NC
	1	Equal to EOT	C + 1	LSB	R = 01	NC

NOTES: 1. NC (No Change): The same value as the one at the beginning of command execution.
2. LSB (Least Significant Bit): The least significant bit of H is complemented.

Write Data

A set of nine (9) bytes are required to set the FDC into the Write Data mode. After the Write Data command has been issued, the FDC loads the head (if it is in the unloaded state), waits the specified Head Settling Time (defined in the specify command), and begins reading ID Fields. When all four bytes loaded during the Command (C, H, R, N) match the four bytes of the ID field from the diskette, the FDC takes data from the processor byte-by-byte via the data bus, and outputs it to the drive.

After writing data into the current sector, the Sector Number stored in "R" is incremented by one, and the next data field is written. The FDC continues this "Multi-Sector Write Operation" until the issuance of a Terminal Count signal. If a Terminal Count signal is sent to the FDC, it continues writing into the current sector to complete the data field. If the Terminal Count signal is received while a data field is being written, then the remainder of the data field is filled with 00 (zeros).

The FDC reads the ID field of each sector and checks the CRC bytes. If the FDC detects a read error (incorrect CRC) in one of the ID Fields, it sets the DE (Data Error) flag of Status Register 1 to a 1 (high), and terminates the Write Data Command. Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.

The Write Command operates in much the same manner as the Read Command. The following items are the same, and one should refer to the Read Data Command for details:

- Transfer Capacity
- EN (End of Cylinder) Flag
- ND (No Data) Flag
- Head Unload Time Interval
- ID Information when the processor terminates command
- Definition of DTL when N = 0 and when N ≠ 0

In the Write Data mode, data transfers between the processor and FDC, via the Data Bus, must occur every 27 μs in the FM mode, and every

13 μs in the MFM mode. If the time interval between data transfers is longer than this, the FDC sets the OR (Over Run) flag in Status Register 1 to a 1 (high), and terminates the Write Data Command. Status register 0 also has bit 7 and 6 set to 0 and 1 respectively.

Write Deleted Data

This command is the same as the Write Data Command except a Deleted Data Address Mark is written at the beginning of the Data Field instead of the normal Data Address Mark.

Read Deleted Data

This command is the same as the Read Data Command except that when the FDC detects a Data Address Mark at the beginning of a Data Field and SK = 0 (low), it will read all the data in the sector and set the CM flag in Status Register 2 to a 1 (high), and then terminate the command. If SK = 1, the FDC skips the sector with the Data Address Mark and reads the next sector.

Read a Track

This command is similar to the READ DATA Command except that this is a continuous READ operation where the entire data field from each of the sectors are read. Immediately after encountering the INDEX HOLE, the FDC starts reading all data fields on the track, as continuous blocks of data. If the FDC finds an error in the ID or DATA CRC check bytes, it continues to read data from the track. The FDC compares the ID information read from each sector with the value stored in the IDR, and sets the ND flag of Status Register 1 to a 1 (high) if there is no comparison. Multi-track or skip operations are not allowed with this command.

This command terminates when the number of sectors read is equal to EOT. If the FDC does not find an ID Address Mark on the diskette after it encounters the INDEX HOLE for the second time, it sets the MA (missing address mark) flag in Status register 1 to a 1 (high), and terminates the command. Status Register 0 has bits 7 and 6 set to 0 and 1 respectively.

Read ID

The READ ID Command is used to give the present position of the recording head. The FDC stores the values from the first ID field it is able to read. If no proper ID Address Mark is found on the diskette before the INDEX HOLE is encountered for the second time, the MA (Missing Address Mark) flag in Status Register 1 is set to a "1" (high), and if no data is found then the ND (No Data) flag is also set in Status Register 1 to a "1" (high). The command is then terminated with Bits 7 and 6 in Status Register 0 set to "0" and "1" respectively. During this command there is no data transfer between FDC and the CPU except during the result phase.

Format a Track

The Format Command allows an entire track to be formatted. After the INDEX HOLE is detected, Data is written on the Diskette. Gaps, Address Marks, ID Fields and Data Fields, all per the IBM System 34 (Double Density) or System 3740 (Single Density) Format are recorded. The particular format which will be written is controlled by the values programmed into N (number of bytes/sector), SC (sectors/cylinder), GPL (Gap Length), and D (Data Pattern) which are supplied by the processor during the Command Phase. The Data Field is filled with the Byte of data stored in D. The ID Field for each sector is supplied by the processor; four data requests per sector are made by the FDC for C (Cylinder Number), H (Head Number), R (Sector Number) and N (Number of Bytes/Sector). This allows the diskette to be formatted with nonsequential sector numbers, if desired.

The processor must send new values for C, H, R, and N to the FDC for each sector on the track. If the FDC is set for DMA mode, it will issue 4 DMA requests per sector. If it is set for interrupt mode, it will issue four interrupts per sector and the processor must supply C, H, R and N load for each sector. The contents of the R register are incremented by one after each sector is formatted. The R register therefore contains a value of R when it is read during the Result Phase. This incrementing and formatting continues for the whole track until the FDC encounters the INDEX HOLE for the second time, whereupon it terminates the command.

If a FAULT signal is received from the drive at the end of a write operation, then the FDC sets the EC flag of Status Register 0 to a 1 (high), and terminates the command after setting bits 7 and 6 of Status Register 0 to 0 and 1 respectively. Also, the loss of a READY signal at the beginning of a command execution phase causes bits 7 and 6 of Status Register 0 to be set to 0 and 1 respectively.

Table 15 shows the relationship between N, SC, GPL for various sector sizes. (See Table 18 for recommended IBM PC and PC/AT compatible programming parameters.)

Table 15

FORMAT	SECTOR SIZE	N	SC	GPL[1]	GPL[2][3]
8" Standard Floppy					
FM Mode	128 Bytes/Sector	00	1A	07	1B
	256	01	0F	0E	2A
	512	02	08	1B	3A
	1024	03	04	47	8A
	2048	04	02	C8	FF
	4096	05	01	C8	FF
MFM Mode [4]	256	01	1A	0E	36
	512	02	0F	1B	54
	1024	03	08	35	74
	2048	04	04	99	FF
	4096	05	02	C8	FF
	8192	06	01	C8	FF
5¼" Minifloppy					
FM Mode	128 Bytes/Sector	00	12	07	09
	128	00	10	10	19
	256	01	08	18	30
	512	02	04	46	87
	1024	03	02	C8	FF
	2048	04	01	C8	FF

FORMAT	SECTOR SIZE	N	SC	GPL[1]	GPL[2][3]
MFM Mode [4]	256	01	12	0A	0C
	256	01	10	20	32
	512	02	09	2A	50
	1024	03	04	80	F0
	2048	04	02	C8	FF
	4096	05	01	C8	FF
3½" Sony Micro Floppydisk•					
FM Mode	128 Bytes/Sector	0	0F	07	1B
	256	1	09	0E	2A
	512	2	05	1B	3A
MFM Mode	256	1	0F	0E	36
	512	2	09	1B	54
	1024	3	05	35	74

NOTES: (1) Suggested values of GPL in Read or Write commands to avoid splice point between data field and ID field of contiguous sections.
(2) Suggested values of GPL in format command.
(3) All values except sector size and hexadecimal.
(4) In MFM mode FDC cannot perform a Read/Write/Format operation with 128 bytes/sector. (N = 00)

Scan Commands

The SCAN Commands allow data which is being read from the diskette to be compared against data which is being supplied from the main system. The FDC compares the data on a byte-by-byte basis, and looks for a sector of data which meets the conditions of:

$$D_{FDD} = D_{PROCESSOR}, D_{FDD} \leq D_{PROCESSOR}, \text{ or}$$

$$D_{FDD} \geq D_{PROCESSOR}$$

The hexadecimal byte of FF either from memory or from the drive can be used as a mask byte because it always meets the condition of the compare. Ones complement arithmetic is used for comparison (FF = largest number, 00 = smallest number). After a whole sector of data is compared, if the conditions are not met, the sector number is incremental (R + STP → R), and the scan operation is continued. The scan operation continues until one of the following conditions occur:

1. The conditions for scan are met (equal, low, or high), or,
2. The last sector on the track is reached (EOT), or
3. The terminal count signal is received.

If the conditions for scan are met, then the FDC sets the SH (Scan Hit) flag of Status Register 2 to a "1" (high), and terminates the Scan Command. If the conditions for scan are not met between the starting sector (as specified by R) and the last sector on the cylinder (EOT), then the FDC sets the SN (Scan Not Satisfied)

flag of Status Register 2 to a 1 (high), and terminates the Scan Command. The receipt of a TERMINAL COUNT signal from the Processor or DMA Controller during the scan operation will cause the FDC to complete the comparison of the particular byte which is in process, and then to terminate the command. Table 16 shows the status of bits SH and SN under various conditions of SCAN.

Table 16

COMMAND	STATUS REGISTER 2		COMMENTS
	BIT 2 (SN)	BIT 3 (SH)	
Scan Equal	0	1	$D_{FDD} = D_{PROCESSOR}$
	1	0	$D_{FDD} \neq D_{PROCESSOR}$
Scan Low or Equal	0	1	$D_{FDD} = D_{PROCESSOR}$
	0	0	$D_{FDD} < D_{PROCESSOR}$
	1	0	$D_{FDD} > D_{PROCESSOR}$
Scan High or Equal	0	1	$D_{FDD} = D_{PROCESSOR}$
	0	0	$D_{FDD} > D_{PROCESSOR}$
	1	0	$D_{FDD} < D_{PROCESSOR}$

If the FDC encounters a Deleted Data Address Mark on one of the sectors (and SK = 0), then it regards the sector as the last sector on the cylinder, sets the CM (Control Mark) flag of Status Register 2 to a 1 (high) and terminates the command. If SK = 1, the FDC skips the sector with the Deleted Address Mark, and reads the next sector. In the second case (SK = 1), the FDC sets the CM (Control Mark) flag of Status Register 2 to a 1 (high) in order to show that a Deleted Sector had been encountered.

When either the STP (contiguous sectors = 01, or alternate sectors = 02) sectors are read, or the MT (Multi-Track) is programmed, it is necessary to remember that the last sector on the track must be read. For example, if STP = 02, MT = 0, the sectors are numbered sequentially 1 through 26, and we start the Scan Command at sector 21, the following will happen: Sectors 21, 23 and 25 will be read, then the next sector (26) will be skipped, and the Index Hole will be encountered before the EOT value of 26 can be read. This will result in an abnormal termination of the command. If the EOT has been set at 25 or the scanning started at sector 20, then the Scan Command would be completed in a normal manner.

During the Scan Command, data is supplied by either the processor or DMA Controller for comparison against the data read from the diskette. In order to avoid having the OR (Over Run) flag set in Status Register 1, it is necessary to have the data available in less than 27 μs (FM Mode) or 13 μs (MFM Mode). If an Overrun occurs the FDC ends the command with bits 7 and 6 of Status Register 0 set to 0 and 1, respectively.

Seek

The read/write head within the drive is moved from cylinder to cylinder under control of the Seek Command. FDC has four independent Present Cylinder Registers for each drive. They are clear only after the Recalibrate command.

The FDC compares the PCN (Present Cylinder Number), which is the current head position, with the NCN (New Cylinder Number), and if there is a difference performs the following operation:

PCN < NCN: Direction signal to drive set to a 1 (high),and Step Pulses are issued (Step In).

PCN > NCN: Direction signal to drive set to a 0 (low), and Step Pulses are issued (Step Out).

The rate at which Step Pulses are issued is controlled by the SRT (Stepping Rate Time) in the SPECIFY Command. After each Step Pulse is issued, NCN is compared against PCN; when NCN = PCN, the SE (Seek End) flag in Status Register 0 is set to a 1 (high), and the command is terminated. At this point the FDC interrupt goes high. Bits DB0 - DB3 in the Main Status Register are set during the seek operation and are cleared by the Sense Interrupt Status Command.

During the Command Phase of the Seek operation, the FDC is in the FDC BUSY state, but during the Execution Phase it is in the NON-BUSY state. While the FDC is in the NON BUSY state, another seek Command may be issued, and in this manner parallel Seek Operations may be performed on up to 4 Drives at once. No other command can be issued for as long as the FDC is in process of sending Step Pulses to any drive.

If a drive is in a NOT READY state at the beginning of the command execution phase or during the seek operation, then the NR (NOT READY) flag is set in Status Register 0 to a 1 (high), and the command is terminated after bits 7 and 6 of Status Register 0 are set to 0 and 1 respectively.

If the time to write 3 bytes of seek command exceeds 150 μs, the timing between the first two Step Pulses may be shorter than set in the Specify command by as much as 1 ms.

Recalibrate

The function of this command is to retract the read/write head within the drive to the Track 0 position. The FDC clears the contents of the PCN counter, and checks the status of the Track 0 signal from the drive. As long as the Track 0 signal is low, the Direction signal remains 0 (low) and Step Pulses are issued. When the Track 0 signal goes high, the SE (SEEK END) flag in Status Register 0 is set to a 1 (high) and the command is terminated. If the Track 0 signal is still low after 77 Step Pulses have been issued, the FDC sets the SE (SEEK END) and EC (EQUIPMENT CHECK) flags of Status Register 0 to both 1's (highs), and terminates the command after bits 7 and 6 of Status Register 0 are set to 0 and 1 respectively.

For IBM compatibility, two RECALIBRATE Commands must be issued for disks with more than 77 tracks.

The ability to overlap RECALIBRATE Commands to multiple drives and the loss of the READY signal, as described in the Seek Command, also applies to the RECALIBRATE Command.

Sense Interrupt Status

An Interrupt signal will be generated by the FDC for one of the following reasons:

1. Upon entering the Result Phase of:
   a. Read Data Command
   b. Read a Track Command
   c. Read ID Command
   d. Read Deleted Data Command

e. Write Data Command
f. Format a Cylinder Command
g. Write Deleted Data Command
h. Scan Commands

2. Ready Line of drive changes state
3. End of Seek or Recalibrate Command
4. During Execution Phase in the NON-DMA Mode

Interrupts caused by reasons 1 and 4 above occur during normal command operations and are easily discernible by the processor. During an execution phase in the NON-DMA Mode, DB5 in the Main Status Register is high. Upon entering the Result Phase this bit is cleared. Reasons 1 and 4 do not require a Sense Interrupt Status command. The interrupt is cleared by reading or writing data to the FDC.

Interrupts caused by reasons 2 and 3 above may be uniquely identified with the aid of the Sense Interrupt status Command. This command when issued resets the interrupt signal and via bits 5, 6, and 7 of Status Register, 0 identifies the cause of the interrupt. See Table 17.

Neither the Seek or Recalibrate Command have a Result Phase. Therefore, it is mandatory to use the Sense Interrupt Status Command after these commands to effectively terminate them and to provide verification of the head position (PCN).

Issuing the Sense Interrupt Status Command without an interrupt pending is treated as an invalid command.

Table 17

SEEK END BIT 5	INTERRUPT CODE		CAUSE
	BIT 6	BIT 7	
0	1	1	Ready Line changed state, either polarity
1	0	0	Normal Termination of Seek or Recalibrate Command
1	1	0	Abnormal Termination of Seek or Recalibrate Command

Specify

The Specify Command sets the initial values for each of the three internal timers. The HUT (Head Unload Time) defines the time from the end of the Execution Phase of one of the Read/Write Commands to the head unload state. This timer is programmable from 16 to 240 ms in increments of 16 ms (01 = 16 ms, 02 = 32 ms, ... 0F = 240 ms). The SRT (Step Rate Time) defines the time interval between adjacent step pulses. This timer is programmable from 1 to 16 ms in increments of 1 ms (F = 1 ms, E = 2 ms, D = 3 ms, etc.).

The HLT (Head Load Time) defines the time between the Head Load signal going high and the Read/Write operation starting. This timer is programmable from 2 to 254 ms in increments of 2 ms (01 = 2 ms, 02 = 4 ms, 03 = 6 ms,... 7F = 254 ms).

The time intervals mentioned above are a direct function of the clock (CLK1 or XTAL1). Times indicated above are for a 16 MHz clock; if the clock is reduced to 8 MHz then the time intervals are increased by a factor of two. If the clock is increased to 32 MHz then all time intervals are decreased by a factor of two.

The choice of DMA or non-DMA operation is made by the ND (NON-DMA) bit. When this bit is high (ND = 1), the non-DMA mode is selected, and when ND = 0, the DMA mode is selected.

Sense Drive Status

This command may be used by the processor whenever it wishes to obtain the status of the drives. Status Register 3 contains the Drive Status information stored internally in the FDC registers.

Invalid

If an invalid command is sent to the FDC (a command not defined above), then the FDC will terminate the command after bits 7 and 6 of Status Register 0 are set to 1 and 0 respectively. No interrupt is generated by the FDC during this condition. Bit 6 and bit 7 (DIO and RQM) in the Main Status Register are both high ("1") indicating to the processor that the FDC is in the Result Phase and the contents of Status Register 0 (STO) must be read. When the processor reads Status Register 0, it will find an 80 hex indicating an invalid command was received.

A Sense Interrupt Status Command must be sent after a Seek or Recalibrate Interrupt, otherwise the FDC will consider the next command to be an Invalid Command.

In some applications the user may wish to use this command as a No-Op command, to place the FDC in a standby or no operation state.

Software Reset

The Software Reset Command places the FDC into reset, but does not affect the Digital Output Register or the Data Rate Selection Register. Reset is exited by the first FDC register access (usually a read of the Main Status Register - 3F4H). A ready change interrupt is generated after exiting reset.

Return Version

The Return Version Command identifies the type of FDC core in use. A value of 90 hex is returned as the result byte, indicating a B-type FDC core. No interrupts are generated.

FLOPPY DISK FORMAT FIELDS

SYSTEM 34 (DOUBLE DENSITY) FORMAT

GAP4a	SYNC	IAM		GAP1	SYNC	IDAM		C	H	S	N	C	GAP2	SYNC	DATA		DATA	C	GAP3	GAP 4b
80x	12x			50x	12x			Y	D	E	O	R	22x	12x	AM			R		
4E	00	3x C2	FC	4E	00	3x A1	FE	L		C		C	4E	00	3x A1	FB F8		C		

SYSTEM 3740 (SINGLE DENSITY) FORMAT

GAP4a	SYNC	IAM	GAP1	SYNC	IDAM	C	H	S	N	C	GAP2	SYNC	DATA	DATA	C	GAP3	GAP 4b
40x	6x		26x	6x		Y	D	E	O	R	11x	6x	AM		R		
FF	00	FC	FF	00	FE	L		C		C	FF	00	FB or F8		C		

Table 18 - Programming Values for Floppy Disk Controllers (IBM PC and PC/AT Compatible Systems)

PARAMETER	HEX VALUES TO BE PROGRAMMED			
	1.44 MB 3.5"	720 KB 3.5"	1.2 MB 5.25"	360 KB 5.25"
Bytes/Sector {N}	02	02	02	02
Sectors/Track {SC}	12	09	0F	09
Gap Length (1) {GPL1}	1B	2A	1B	2A
Gap Length (2),(3){GPL2,3}	6C	50	54	50
Head Settle Time (ms)	15	15	15	15
Motor Start Up (1/8 sec)	08	08	08	08
Cylinders	80	80	80	40
Tracks	160	160	160	80
Tracks/Inch	135	135	96	48
Heads	02	02	02	02
RPM	300	300	360	300
Transfer (KB/s)	500	250	500	250

SERIAL PORT (UART)

The FDC37C651 and FDC37C652 incorporate two full function UARTs. They are compatible with the NS16450 and the 16450 ACE registers. The UARTS perform serial-to-parallel conversion on received characters and parallel-to-serial conversion on transmit characters. The data rates are independently programmable from 115.2K baud down to 50 baud. The character options are programmable for 1 start; 1, 1.5 or 2 stop bits; even, odd, sticky or no parity; and prioritized interrupts. The UARTS each contain programmable baud rate generator that is capable of dividing the input clock or crystal by a number from 1 to 65535. Refer to the FDC37C651 Configuration Registers and FDC37C652 Hardware Configuration description for information on disabling, power down and changing the base address of the UARTS. The interrupt from a UART is enabled by programming OUT2 of that UART to a logic "1". OUT2 being a logic "0" disables that UART's interrupt.

REGISTER DESCRIPTION

Addressing of the accessible registers of the Serial Port is shown below. The base addresses of the serial ports are defined by the configuration registers (see Configuration section). The Serial Port registers are located at sequentially increasing addresses above these base addresses. The FDC37C651 contains two serial ports, each of which contain a register set as described below.

Table 19 - Addressing the Serial Port

DLAB*	A2	A1	A0	REGISTER NAME
0	0	0	0	Receive Buffer (read)
0	0	0	0	Transmit Buffer (write)
0	0	0	1	Interrupt Enable (read/write)
X	0	1	0	Interrupt Identification (read/write)
X	0	1	1	Line Control (read/write)
X	0	0	0	Modem Control (read/write)
X	1	0	1	Line Status (read/write)
X	1	1	0	Modem Status (read/write)
X	1	1	1	Scratchpad (read/write)
1	1	0	0	Divisor LSB (read/write)
1	0	0	1	Divisor MSB (read/write

*NOTE: DLAB is Bit 7 of the Line Control Register

The following section describes the operation of the registers.

RECEIVE BUFFER REGISTER (RB)
Address Offset = 0H, DLAB = 0, READ ONLY

This register holds the received incoming data byte. Bit 0 is the least significant bit, which is transmitted and received first. Received data is double buffered; this uses an additional shift register to receive the serial data stream and convert it to a parallel 8 bit word which is transferred to the Receive Buffer register. The shift register is not accessible.

TRANSMIT BUFFER REGISTER (TB)
Address Offset = 0H, DLAB = 0, WRITE ONLY

This register contains the data byte to be transmitted. The transmit buffer is double buffered, utilizing an additional shift register (not accessible) to convert the 8 bit data word to a serial format. This shift register is loaded from the Transmit Buffer when the transmission of the previous byte is complete.

INTERRUPT ENABLE REGISTER (IER)
Address Offset = 1H, DLAB = 0, READ/WRITE

The lower four bits of this register control the enables of the four interrupt sources of the Serial Port interrupt. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of this register. Similarly, setting the appropriate bits of this register to a high, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and disables any Serial Port interrupt out of the FDC37C651. All other system functions operate in their normal manner, including the Line Status and MODEM Status Registers. The contents of the Interrupt Enable Register are described below.

Bit 0
This bit enables the Received Data Available Interrupt when set to logic "1".

Bit 1
This bit enables the Transmitter Holding Register Empty Interrupt when set to logic "1".

Bit 2
This bit enables the Received Line Status Interrupt when set to logic "1". The error sources causing the interrupt are Overrun, Parity, Framing and Break. The Line Status Register must be read to determine the source.

Bit 3
This bit enables the MODEM Status Interrupt when set to logic "1". This is caused when one of the Modem Status Register bits changes state.

Bits 4 through 7
These bits are always logic "0".

INTERRUPT IDENTIFICATION REGISTER (IIR)
Address Offset = 2H, DLAB = X, READ/WRITE

By accessing this register, the host CPU can determine the highest priority interrupt and its source. Four levels of priority interrupt exist. They are in descending order of priority:

1. Receiver Line Status (highest priority)
2. Received Data Ready
3. Transmitter Holding Register Empty
4. MODEM Status (lowest priority)

Information indicating that a prioritized interrupt is pending and the source of that interrupt is stored in the Interrupt Identification Register (refer to Interrupt Control Table). When the CPU accesses the IIR, the Serial Port freezes all interrupts and indicates the highest priority pending interrupt to the CPU. During this CPU access, even if the Serial Port records new interrupts, the current indication does not change until access is completed. The contents of the IIR are described below.

Bit 0
This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic "0", an interrupt is pending and the contents of the IIR may be used as a pointer to the appropriate internal service routine. When bit 0 is a logic "1", no interrupt is pending.

Bits 1 and 2
These two bits of the IIR are used to identify the highest priority interrupt pending as indicated by the Interrupt Control Table.

Bits 3 through 7
These bits of the IIR are always logic "0".

Table 20 - Interrupt Control Table

INTERRUPT IDENTIFICATION REGISTER			INTERRUPT SET AND RESET FUNCTIONS			
BIT 2	BIT 1	BIT 0	PRIORITY LEVEL	INTERRUPT TYPE	INTERRUPT SOURCE	INTERRUPT RESET CONTROL
0	0	1	-	None	None	-
1	1	0	Highest	Receiver Line Status	Overrun Error, Parity Error, Framing Error or Break Interrupt	Reading the Line Status Register
1	0	0	Second	Received Data Available	Receiver Data Available	Read Receiver Buffer
0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if Source of Interrupt) or Writing the Transmitter Holding Register
0	0	0	Fourth	MODEM Status	Clear to Send or Data Set Ready or Ring Indicator or Data Carrier Detect	Reading the MODEM Status Register

Table 21 - Register Summary for an Individual UART Channel

REGISTER ADDRESS*	REGISTER NAME	REGISTER SYMBOL	BIT 0	BIT 1
ADDR = 0 DLAB = 0	Receive Buffer Register (Read Only)	RBR	Data Bit 0 (Note 1)	Data Bit 1
ADDR = 0 DLAB = 0	Transmitter Holding Register (Write Only)	THR	Data Bit 0	Data Bit 1
ADDR = 1 DLAB = 0	Interrupt Enable Register	IER	Enable Received Data Available Interrupt (ERDAI)	Enable Transmitter Holding Register Empty Interrupt (ETHREI)
ADDR = 2	Interrupt Ident. Register (Read Only)	IIR	"0" if Interrupt Pending	Interrupt ID Bit
ADDR = 2	Test Control Register (Write Only)	TCR	Reserved	Reserved
ADDR = 3	Line Control Register	LCR	Word Length Select Bit 0 (WLS0)	Word Length Select Bit 1 (WLS1)
ADDR = 4	MODEM Control Register	MCR	Data Terminal Ready (DTR)	Request to Send (RTS)
ADDR = 5	Line Status Register	LSR	Data Ready (DR)	Overrun Error (OE)
ADDR = 6	MODEM Status Register	MSR	Delta Clear to Send (DCTS)	Delta Data Set Ready (DDSR)
ADDR = 7	Scratch Register (Note 4)	SCR	Bit 0	Bit 1
ADDR = 0 DLAB = 1	Divisor Latch (LS)	DDL	Bit 0	Bit 1
ADDR = 1 DLAB = 1	Divisor Latch (MS)	DLM	Bit 8	Bit 9

Table 21 - Register Summary for an Individual UART Channel (continued)

BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
Data Bit 2	Data Bit 3	Data Bit 4	Data Bit 5	Data Bit 6	Data Bit 7
Data Bit 2	Data Bit 3	Data Bit 4	Data Bit 5	Data Bit 6	Data Bit 7
Enable Receiver Line Status Interrupt (ELSI)	Enable MODEM Status Interrupt (EMSI)	0	0	0	0
Interrupt ID Bit	0	0	0	0	0
Reserved	Reserved	$\overline{\text{BAUDOUT}}$ Select	Reserved	Reserved	Reserved
Number of Stop Bits (STB)	Parity Enable (PEN)	Even Parity Select (EPS)	Stick Parity	Set Break	Divisor Latch Access Bit (DLAB)
Out 1 (Note 3)	IRQ ENable (Note 3)	Loop	0	0	0
Parity Error (PE)	Framing Error (FE)	Break Interrupt (BI)	Transmitter Holding Register (THRE)	Transmitter Empty (TEMT) (Note 2)	0
Trailing Edge Ring Indicator (TERI)	Delta Data Carrier Detect (DDCD)	Clear to Send (CTS)	Data Set Ready (DSR)	Ring Indicator (RI)	Data Carrier Detect (DCD)
Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Bit 10	Bit 11	Bit 12	Bit 13	Bit 14	Bit 15

*DLAB is Bit 7 of the Line Control Register (ADDR = 3).

Note 1: Bit 0 is the least significant bit. It is the first bit serially transmitted or received.
Note 2: When operating in the XT mode, this bit will be set any time that the transmitter shift register is empty.
Note 3: This bit no longer has a pin associated with it.
Note 4: When operating in the XT mode, this register is not available.

LINE CONTROL REGISTER (LCR)
Address Offset = 3H, DLAB = X, READ/WRITE

This register contains the format information of the serial line. The bit definitions are:

Bits 0 and 1
These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 is as follows:

BIT 1	BIT 0	WORD LENGTH
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

The Start, Stop and Parity bits are not included in the word length.

Bit 2
This bit specifies the number of stop bits in each transmitted or received serial character. The following table summarizes the information.

BIT 2	WORD LENGTH	NUMBER OF STOP BITS
0	--	1
1	5 bits	1.5
1	6 bits	2
1	7 bits	2
1	8 bits	2

Note: The receiver will ignore all stop bits beyond the first, regardless of the number used in transmitting.

Bit 3
Parity Enable bit. When bit 3 is a logic "1", a parity bit is generated (transmit data) or checked (receive data) between the last data word bit and the first stop bit of the serial data. (The parity bit is used to generate an even or odd number of 1s when the data word bits and the parity bit are summed).

Bit 4
Even Parity Select bit. When bit 3 is a logic "1" and bit 4 is a logic "0", an odd number of logic "1"'s is transmitted or checked in the data word bits and the parity bit. When bit 3 is a logic "1" and bit 4 is a logic "1" an even number of bits is transmitted and checked.

Bit 5
Stick Parity bit. When bit 3 is a logic "1" and bit 5 is a logic "1", the parity bit is transmitted and then detected by the receiver in the opposite state indicated by bit 4.

Bit 6
Set Break Control bit. When bit 6 is a logic "1", the transmit data output (TXD) is forced to the Spacing or logic "0" state and remains there (until reset by a low level bit 6) regardless of other transmitter activity. This feature enables the Serial Port to alert a terminal in a communications system.

Bit 7
Divisor Latch Access bit (DLAB). It must be set high (logic "1") to access the Divisor Latches of the Baud Rate Generator during read or write operations. It must be set low (logic "0") to access the Receiver Buffer Register, the Transmitter Holding Register, or the Interrupt Enable Register.

MODEM CONTROL REGISTER (MCR)
Address Offset = 4H, DLAB = X, READ/WRITE

This 8 bit register controls the interface with the MODEM or data set (or device emulating a MODEM). The contents of the MODEM control register are described below.

Bit 0
This bit controls the Data Terminal Ready ($\overline{DTR}$) output. When bit 0 is set to a logic "1", the

$\overline{DTR}$ output is forced to a logic "0". When bit 0 is a logic "0", the $\overline{DTR}$ output is forced to a logic "1".

Bit 1
This bit controls the Request To Send ($\overline{RTS}$) output. Bit 1 affects the $\overline{RTS}$ output in a manner identical to that described above for bit 0.

Bit 2
This bit controls the Output 1 (OUT1) bit. This bit does not have an output pin and can only be read or written by the CPU.

Bit 3
Output 2 (OUT2). This bit is used to enable an UART interrupt. When OUT2 is a logic "0", the serial port interrupt output is forced to a high impedance state - disabled. When OUT2 is a logic "1", the serial port interrupt outputs are enabled.

Bit 4
This bit provides the loopback feature for diagnostic testing of the Serial Port. When bit 4 is set to logic "1", the following occur:

1. The TXD is set to the Marking State (logic "1").
2. The receiver Serial Input (SIN) is disconnected.
3. The output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input.
4. All MODEM Control inputs ($\overline{CTS}$, $\overline{DSR}$, $\overline{RI}$ and $\overline{DCD}$) are disconnected.
5. The four MODEM Control outputs ($\overline{DTR}$, $\overline{RTS}$, and OUT2) are internally connected to the four MODEM Control inputs.
6. The Modem Control output pins are forced inactive high.
7. Data that is transmitted is immediately received.

This feature allows the processor to verify the transmit and receive data paths of the Serial Port. In the diagnostic mode, the receiver and the transmitter interrupts are fully operational. The MODEM Control Interrupts are also operational but the interrupts' sources are now the lower four bits of the MODEM Control Register instead of the MODEM Control inputs. The interrupts are still controlled by the Interrupt Enable Register.

Bits 5 through 7
These bits are permanently set to logic zero.

LINE STATUS REGISTER (LSR)
Address Offset = 5H, DLAB = X, READ/WRITE

Bit 0
Data Ready (DR). It is set to a logic "1" whenever a complete incoming character has been received and transferred into the Receiver Buffer Register. Bit 0 will be reset to a logic "0" by the read of the data in the Receiver Buffer Register.

Bit 1
Overrun Error (OE). Bit 1 indicates that data in the Receiver Buffer Register was not read before the next character was transferred into the register, thereby destroying the previous character. The OE indicator is reset whenever the Line Status Register is read.

Bit 2
Parity Error (PE). Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even parity select bit. The PE is set to a logic "1" upon detection of a parity error and is reset to a logic "0" whenever the Line Status Register is read.

Bit 3
Framing Error (FE). Bit 3 indicates that the received character did not have a valid stop bit. Bit 3 is set to a logic "1" whenever the stop bit following the last data bit or parity bit is detected as a zero bit (Spacing level). The FE is reset to a logic "0" whenever the Line Status

Register is read. The Serial Port will try to resynchronize after a framing error. To do this, it assumes that the framing error was due to the next start bit, so it samples this 'start' bit twice and then takes in the 'data'.

Bit 4
Break Interrupt (BI). Bit 4 is set to a logic "1" whenever the received data input is held in the Spacing state (logic "0") for longer than a full word transmission time (that is, the total time of the start bit + data bits + parity bits + stop bits). The BI is reset after the CPU reads the contents of the Line Status Register. Restarting after a break is received, requires the serial data (SIN) to be logic "1" for at least 1/2 bit time.

Note: Bits 1 through 4 are the error conditions that produce a Receiver Line Status Interrupt whenever any of the corresponding conditions are detected and the interrupt is enabled.

Bit 5
Transmitter Holding Register Empty (THRE). Bit 5 indicates that the Serial Port is ready to accept a new character for transmission. In addition, this bit causes the Serial Port to issue an interrupt when the Transmitter Holding Register interrupt enable is set high. The THRE bit is set to a logic "1" when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic "0" whenever the CPU loads the Transmitter Holding Register. Bit 5 is a read only bit.

Bit 6
Transmitter Empty (TEMT). Bit 6 is set to a logic "1" whenever the Transmitter Holding Register (THR) and Transmitter Shift Register (TSR) are both empty. It is reset to logic "0" whenever either the THR or TSR contains a data character. Bit 6 is a read only bit.

Bit 7
This bit is permanently set to logic "0".

MODEM STATUS REGISTER (MSR)
Address Offset = 6H, DLAB = X, READ/WRITE

This 8 bit register provides the current state of the control lines from the MODEM (or peripheral device). In addition to this current state information, four bits of the MODEM Status Register (MSR) provide change information. These bits are set to logic one whenever a control input from the MODEM changes state. They are reset to logic "0" whenever the MODEM Status Register is read.

Bit 0
Delta Clear To Send (DCTS). Bit 0 indicates that the $\overline{CTS}$ input to the chip has changed state since the last time the MSR was read.

Bit 1
Delta Data Set Ready (DDSR). Bit 1 indicates that the $\overline{DSR}$ input has changed state since the last time the MSR was read.

Bit 2
Trailing Edge of Ring Indicator (TERI). Bit 2 indicates that the $\overline{RI}$ input has changed from logic "0" to logic "1".

Bit 3
Delta Data Carrier Detect (DDCD). Bit 3 indicates that the $\overline{DCD}$ input to the chip has changed state.
NOTE: Whenever bit 0, 1, 2, or 3 is set to a logic "1", a MODEM Status Interrupt is generated.

Bit 4
This bit is the complement of the Clear To Send ($\overline{CTS}$) input. If bit 4 of the MCR is set to logic "1", this bit is equivalent to $\overline{RTS}$ in the MCR.

Bit 5
This bit is the complement of the Data Set Ready ($\overline{DTR}$) input. If bit 4 of the MCR is set to logic "1", this bit is equivalent to $\overline{DSR}$ in the MCR.

Bit 6
This bit is the complement of the Ring Indicator ($\overline{RI}$) input. If bit 4 of the MCR is set to logic "1", this bit is equivalent to OUT1 in the MCR.

Bit 7
This bit is the complement of the Data Carrier Detect ($\overline{DCD}$) input. If bit 4 of the MCR is set to logic "1", this bit is equivalent to OUT2 in the MCR.

SCRATCHPAD REGISTER (SCR)
Address Offset = 7H, DLAB = X, READ/WRITE

This 8 bit read/write register has no effect on the operation of the Serial Port. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.

PROGRAMMABLE BAUD RATE GENERATOR (AND DIVISOR LATCHES DLH, DLL)

The Serial Port contains a programmable Baud Rate Generator that is capable of taking any clock input (DC to 3 MHz) and dividing it by any divisor from 1 to 65535. This output frequency of the Baud Rate Generator is 16x the Baud rate. Two 8 bit latches store the divisor in 16 bit binary format. These Divisor Latches must be loaded during initialization in order to insure desired operation of the Baud Rate Generator. Upon loading either of the Divisor Latches, a 16 bit Baud counter is immediately loaded. This prevents long counts on initial load. If a 0 is loaded into the BRG registers the output divides the clock by the number 3. If a 1 is loaded the output is the inverse of the input oscillator. If a two is loaded the output is a divide by 2 signal with a 50% duty cycle. If a 3 or greater is loaded the output is low for 2 bits and high for the remainder of the count. The input clock to the BRG is the 24 MHz crystal divided by 13, giving a 1.8462 MHz clock.

The table below shows the baud rates possible with a 1.8462 MHz crystal.

Effect Of The Reset on Register File

The Reset Function Table below details the effect of the Reset input on each of the registers of the Serial Port.

Table 22 - Baud Rates Using 1.8462 MHz Clock (24 MHz/13)

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16X CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL*
50	2304	0.001
75	1536	-
110	1047	-
134.5	857	0.004
150	768	-
300	384	-
600	192	-
1200	96	-
1800	64	-
2000	58	0.005
2400	48	-
3600	32	-
4800	24	-
7200	16	-
9600	12	-
19200	6	-
38400	3	0.030
56000	2	2.86

*Note: The percentage error for all baud rates, except where indicated otherwise, is 0.002%.

Table 23 - Reset Function Table

REGISTER/SIGNAL	RESET CONTROL	RESET STATE
Interrupt Enable Register	RESET	All bits low
Interrupt Identification Reg.	RESET	Bit 0 is high; Bits 1, 2 low
Line Control Reg.	RESET	All bits low
MODEM Control Reg.	RESET	All bits low
Line Status Reg.	RESET	All bits low except 5, 6 high
MODEM Status Reg.	RESET	Bits 0 - 3 low; Bits 4 - 7 input
SOUT	RESET	High
INTRPT (RCVR errs)	RESET/Read LSR	Low
INTRPT (RCVR Data Ready)	RESET/Read RBR	Low
INTRPT (THRE)	RESET/ReadIIR/Write THR	Low
OUT2B	RESET	High
RTSB	RESET	High
DTRB	RESET	High
OUT1B	RESET	High

PARALLEL PORT

The FDC37C651 and FDC37C652 incorporate one IBM XT/AT compatible parallel port. The FDC37C651 supports the optional PS/2 type bi-directional parallel port mode. Refer to the FDC37C651 Configuration Registers and FDC37C652 Hardware Configuration description for information on disabling, power down and changing the base address of the parallel port.

The FDC37C651 and FDC37C652 incorporate protection circuitry which prevents possible damage to the parallel port due to printer power-up.

The functionality of the Parallel Port is achieved through the use of three addressable ports, with their associated registers and control gating. These ports are:

DATA PORT
CONTROL PORT
STATUS PORT

The control and data port are read write by the CPU, while the status port is read only. The address map of the Parallel Port is shown below:

DATA PORT	BASE ADDRESS + 00H
STATUS PORT	BASE ADDRESS + 01H
CONTROL PORT	BASE ADDRESS + 02H

The bit map of these registers is:

	D0	D1	D2	D3	D4	D5	D6	D7
DATA PORT	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7
STATUS PORT	0	0	0	$\overline{ERR}$	SLCT	PE	$\overline{ACK}$	$\overline{BUSY}$
CONTROL PORT	STROBE	AUTOFD	$\overline{INIT}$	SLC	IRQE	PCD	0	0

DATA PORT (Offset = 00H)

The Data Port is located at an offset of '00H' from the base address. The data register is cleared at initialization by RESET. During a WRITE operation, the Data Register latches the controls of the data bus rising edge of the $\overline{IOW}$ input. The contents of this register are buffered (non inverting) and output onto the PD0 - PD7 ports. During a READ operation, PD0 - PD7 ports are read and output to the host CPU.

STATUS PORT (Offset = 01H)

The Status Port is located at an offset of '01H' from the base address. BITS 0 - 2 are not implemented as register bits, during a read of the Printer Status Register these bits are a low level. The bits of the Status Port are defined as follows:

BIT 3 $\overline{ERR}$ - $\overline{ERROR}$
The level on the $\overline{ERROR}$ input is read by the CPU as bit 3 of the Printer Status Register. A logic 0 means an error has been detected; a logic 1 means no error has been detected.

BIT 4 SLCT - PRINTER SELECTED STATUS
The level on the SLCT input is read by the CPU as bit 4 of the Printer Status Register. A logic 1 means the printer is on line; a logic 0 means it is not selected.

BIT 5 PE - PAPER END
The level on the PE input is read by the CPU as bit 5 of the Printer Status Register. A logic 1 indicates a paper end; a logic 0 indicates the presence of paper.

BIT 6 $\overline{\text{ACK}}$ - $\overline{\text{ACKNOWLEDGE}}$
The level on the $\overline{\text{ACK}}$ input is read by the CPU as bit 6 of the Printer Status Register. A logic 0 means that the printer has received a character and can now accept another. A logic 1 means that it is still processing the last character or has not received the data.

BIT 7 $\overline{\text{BUSY}}$ - $\overline{\text{BUSY}}$
The complement of the level on the BUSY input is read by the CPU as bit 7 of the Printer Status Register. A logic 0 in this bit means that the printer is busy and cannot accept a new character. A logic 1 means that it is ready to accept the next character.

CONTROL PORT (Offset = 02H)

The Control Port is located at an offset of '02H' from the base address. The Control Register is initialized by the RESET input, bits 0 to 4 only being affected; bits 5, 6 and 7 are hard wired low.

BIT 0 STROBE - STROBE
This bit is inverted and output onto the $\overline{\text{STROBE}}$ output.

BIT 1 AUTOFD - AUTOFEED
This bit is inverted and output onto the $\overline{\text{AUTOFD}}$ output. A logic 1 causes the printer to generate a line feed after each line is printed. A logic 0 means no autofeed.

BIT 2 $\overline{\text{INIT}}$ - $\overline{\text{INITIATE OUTPUT}}$
This bit is output onto the $\overline{\text{INIT}}$ output without inversion.

BIT 3 SLCTIN - PRINTER SELECT INPUT
This bit is inverted and output onto the $\overline{\text{SLCTIN}}$ output. A logic 1 on this bit selects the printer; a logic 0 means the printer is not selected.

BIT 4 IRQE - INTERRUPT REQUEST ENABLE
The interrupt request enable bit when set to a high level may be used to enable interrupt requests from the Parallel Port to the CPU. An interrupt request is generated on the IRQ port by a positive going $\overline{\text{ACK}}$ input. When the IRQE bit is programmed low the IRQ is disabled.

BIT 5 PCD - PARALLEL CONTROL DIRECTION
Parallel Control Direction is valid in extended mode only (CR#1<6> = 1). In printer mode, the direction is always out regardless of the state of this bit. In extended mode, a logic 0 means that the printer port is in output mode (write); a logic 1 means that the printer port is in input mode (read). Bits 6 and 7 during a read are a low level, and cannot be written.

INTEGRATED DRIVE ELECTRONICS INTERFACE

The IDE interface enables hard disks with embedded controllers (AT and XT) to be interfaced to the host processor. The following definitions are for reference only. These registers are not implemented in the FDC37C651 and FDC37C652. Access to these registers are controlled by the FDC37C651 and FDC37C652. For more information, refer to the IDE pin descriptions.

HOST FILE REGISTERS

The HOST FILE REGISTERS are accessed by the AT Host, rather than the Local Processor. There are two groups of registers, the AT Task File, and the Miscellaneous AT Registers.

ADDRESS 1F0H-1F7H

The address space from 1F0H to 1F7H contains the Task File Registers. These registers communicate data, command, and status information with the AT host, and are addressed when $\overline{\text{HDCS0}}$ is low.

ADDRESS 376H/3F6H; 377H/3F7H

These AT registers may be used by the BIOS for drive control. They are accessed by the AT interface when $\overline{\text{HDSC0}}$ is active.

Figure 4 shows the AT Host Register Map of the FDC37C651 and FDC37C652.

FIGURE 4 - HOST PROCESSOR REGISTER ADDRESS MAP

000H | 007H	TASK FILE REGISTERS
376H/3F6H | 377H/3F7H	MISC AT REGISTERS

TASK FILE REGISTERS

Task File Registers may be accessed by the host AT when pin $\overline{\text{HDCS0}}$ is active (low). The Data Register (1F0H) is 16 bits wide; the remaining task file registers are 8 bits wide. The task file registers are ATA and EATA compatible.

DATA (READ/WRITE) - 1F0H

The DATA REGISTER provides a 16 bit data path to the IDE disk drive. Programmed I/O data transfers between the host and the disk are through this register. In addition, the sector table is transferred through the data register during format commands.

ERROR (READ) - 1F1H

This read-only register contains the status from the last command executed by the drive when the error bit (Register 1F8H, bit D0) is set. If the drive has just been powered up, or has just completed internal diagnostic testing, this register should contain a status code.

BIT D7: BAD BLOCK DETECT

D7 = 1: A bad block mark was detected by the controller in the requested sector's ID field.

BIT D6: UNCORRECTABLE DATA ERROR

D6 = 1: An ECC or CRC error has been encountered in the data.

BIT D4: ID NOT FOUND

D4 = 1: A sync error (correct cylinder, head, sector number, or sector size parameter could not be found) or CRC error has been encountered in any command phase other than the data phase.

BIT D2: ABORTED COMMAND

D2 = 1: The requested command has been aborted due to a drive status error. This indicates that either the command was invalid, or the drive specified in the HEAD/DRIVE register did not have Drive Ready Asserted.

BIT D1: TRACK ZERO NOT FOUND

D1 = 1: After receiving a Restore Command, the drive has generated Seek Complete, but not Track 0.

BIT D0: DATA ADDRESS MARK NOT FOUND

D0 = 1: The controller is reporting a Sync error (missing address mark) in the data phase of a command.

WRITE PRECOMP CYLINDER/FEATURES (WRITE) - 1F1H

This register is written by the host AT. This register is typically used to define the cylinder number where the write precompensation is to be asserted.

SECTOR COUNT (READ/WRITE) - 1F2H

This register is read and written by the host AT. This register is used to store the number of sectors that are to be transferred across the host bus for the subsequent command.

SECTOR NUMBER (READ/WRITE) - 1F3H

This register is read and written by the host AT. This register is used to store the sector number for any disk data access for the subsequent command. During a multiple sector command, this register is used to specify the first sector in the transfer.

CYLINDER LOW (READ/WRITE) - 1F4H

This register is read and written by the host AT. This register is used to store the 8 least significant bits of the desired cylinder number.

CYLINDER HIGH (READ/WRITE) - 1F5H

This register is read and written by the host AT. This register is used to store the 8 most significant bits of the desired cylinder number.

HEAD, DRIVE (READ/WRITE) - 1F6H

This register is read and written by the host AT.

COMMAND (WRITE) - 1F7H

COMMAND REGISTER 1F7H is a write-only register for the AT host. When the COMMAND REGISTER is written, the IDE drive will execute the specified command.

The commands are as follows:

COMMAND	D7	D6	D5	D4	D3	D2	D1	D0
RESTORE (RECALIBRATE)	0	0	0	1	r	r	r	r
SEEK	0	1	1	1	r	r	r	r
READ SECTOR	0	0	1	0	D	0	L	T
WRITE SECTOR	0	0	1	1	D	0	L	T
FORMAT TRACK	0	1	0	1	D	0	0	0
READ VERIFY	0	1	0	0	D	0	0	T
DIAGNOSE	1	0	0	1	0	0	0	0
SET PARAMETERS	1	0	0	1	0	0	0	1

Bit definitions:

r: specifies the step rate to be used for the command.
D: If set, 16 bit DMA is to be used for the data transfer. (Optional for high performance)
L: If set, the ECC will be transferred following the data.
T: if set, retries are inhibited for the command.

AT_STATUS (READ) - 1F7H

This register is read by the host AT. Status is provided by the IDE drive. A read of this register clears the host interrupt signal.

BIT D7: BUSY

BUSY is set by any of the following conditions:

1. Hard reset.
2. Soft reset. A soft reset is initiated by the host processor setting and resetting the RESET bit of the FIXED DISK REGISTER (Bit D2, 3F6/376H).
3. During execution of a command.

BUSY is made inactive, but not cleared, while DRQ (bit D3 of this register) is active.

BIT D6: DRIVE READY

Bit D6 indicates the Ready status of the drive.

BIT D5: WRITE FAULT

Bit D5 indicates the write fault status of the drive.

BIT D4: SEEK COMPLETE

Bit D4 indicates the seek status of the drive.

BIT D3: DATA REQUEST

When set, Bit D3 indicates that the drive is ready for transfer of a word or byte of data between the host and the disk drive.

BIT D2: CORRECTED DATA

When set, Bit D2 indicates that a correctable data error has been encountered and the data has been corrected.

BIT D1: INDEX

Bit D1 is the latched status of the Index pulse. This bit is cleared by reading the AT_STATUS register.

BIT D0: ERROR

When set, Bit D0 indicates that the previous command ended in an error.

MISCELLANEOUS AT REGISTERS

The miscellaneous AT registers provide the AT interface with drive control and status. They are typically used by the BIOS for drive control. These registers are read or written by the AT interface when $\overline{\text{HDCS1}}$ is active (low).

FIXED DISK (WRITE) - 3F6/376

BITS D7-D4: RESERVED

BIT D3: HEAD SELECT 3 ENABLE

HS3EN is set by the Host AT to specify that the $\overline{\text{HS3}}$ signal of the ST-506 drive interface is used to access heads 8 through 15 when the HD SEL 3 bit of the DRIVE/HEAD Register (06H, bit D3). When this bit is low, the $\overline{\text{HS3}}$ signal is used to enable the reduce write current function of the drive.

BIT D2: ADAPTER RESET (RST)

The AT Host may issue a software reset by setting this bit.

BIT D1: DISABLE INTERRUPT REQUEST

The AT Host setting this bit will disable the IRQ output.

BIT D0: RESERVED

ALTERNATE STATUS (READ) - 3F6/376

The ALTERNATE STATUS REGISTER contains the same information as provided in the STATUS REGISTER 1F7H with the difference that a read of this register does not clear the interrupt to the host processor.

For information on the bit definitions, please refer to STATUS REGISTER 1F7H (READ).

DIGITAL INPUT REGISTER (READ) - 3F7/377

This register contains information from the HEAD/DRIVE register and the drive write gate.

BIT D7: NOT USED

BIT D6: $\overline{\text{WGATE}}$

BIT D6 indicates the status of the $\overline{\text{WRITE GATE}}$ output from the disk drive.

BITS D5-D2: $\overline{\text{HEAD SELECT3-0}}$

BITS D5-D2 indicate the contents of the head select bits in the HEAD/DRIVE register. (Bits D3-D0 of register 1F6H.

BIT D1: $\overline{\text{DRIVE SELECT 1}}$

BIT D1 is active low when bit D4 of the HEAD/DRIVE register (1F6H) is set.

BIT D0: $\overline{\text{DRIVE SELECT 0}}$

BIT D0 is active low when bit D3 of the HEAD/DRIVE register (1F6H) is set.

AT HOST ADDRESSABLE REGISTERS
(For Reference Only)

TASK FILE REGISTERS

ADDR	R/W	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	NAME
000H	R/W	DATA REGISTER (REDIRECTED TO FIFO)																DATA REG

ADDR	R/W	D7	D6	D5	D4	D3	D2	D1	D0	NAME
001H	R	BB	CRC	-	ID	-	AC	TK	DM	ERROR FLAGS
001H	W	CYLINDER NUMBER + 4								WRITE PRECOMP CYLINDER
002H	R/W	NUMBER OF SECTORS								SECTOR COUNT
003H	R/W	SECTOR NUMBER								SECTOR NUMBER
004H	R/W	CYLINDER NUMBER (LSB'S)								CYLINDER LOW
005H	R/W	CYLINDER NUMBER (MSB'S)								CYLINDER HIGH
006H	R/W	-	-	DRIVE		HEAD				HEAD, DRIVE
007H	R	BSY	RDY	WF	SC	DRQ	CD	INDEX	ERR	STATUS
007H	W	COMMAND								COMMAND

MISCELLANEOUS AT REGISTERS

ADDR	R/W	D7	D6	D5	D4	D3	D2	D1	D0	NAME
3F6H/ 376H	R	BSY	RDY	WF	SC	DRQ	CD	INDEX	ERR	STATUS
3F6H/ 376H	W	RESERVED				HS3EN	ADPTR RESET	DISABLE IRQ	RE-SERVED	FIXED DISK
3F7H/ 377H	R	-	$\overline{WG}$	$\overline{HS3}$	$\overline{HS2}$	$\overline{HS1}$	$\overline{HS0}$	$\overline{DS1}$	$\overline{DS0}$	DIGITAL INPUT
3F7H/ 377H	W	-	-	-	-	-	-	-	-	RESERVED

CONFIGURATION

The configuration of the FDC37C651 within the user system is selected through software selectable configuration registers. The different configurations of the FDC37C652 can only be selected through jumper options.

FDC37C651 CONFIGURATION REGISTERS

The configuration registers are used to select programmable options of the FDC. After power up, the FDC is in the default mode. The default modes are identified in the Configuration Mode Register Description. To program the configuration registers, the following sequence must be followed:

1. Enter Configuration Mode.
2. Configure FDC Registers.
3. Exit configuration Mode.

Enter Configuration Mode

To enter the configuration mode, two writes in succession to port 3F0H with 55H data are required. If a write to another address or port occurs between these two writes, the chip does not enter the configuration mode. It is strongly recommended that interrupts be disabled for the duration of these two writes.

Configure FDC37C651

The FDC37C651 contains four configuration registers, CR0-CR3. These registers are accessed by first writing the number (0-3) of the desired register to port 3F0H and then writing or reading the configuration register through port 3F1H.

Exit Configuration Mode

The configuration mode is exited by writing an AAH to port 3F0H.

Programming Example

The following is an example of a configuration program in Intel 8086 assembly language. For this example, the FDC37C651 is being reset to the default condition after power up.

```
;-----------------------------.
; ENTER CONFIGURATION MODE    |
;-----------------------------'
MOV   DX,3F0H
MOV   AX,055H
CLI                 ; disable interrupts
OUT   DX,AL
OUT   DX,AL
STI                 ; enable interrupts
;-----------------------------.
; CONFIGURE REGISTERS CR0-CR3 |
;-----------------------------'
MOV   DX,3F0H
MOV   AL,00H
OUT   DX,AL ; Point to CR0
MOV   DX,3F1H
MOV   AL,3FH
OUT   DX,AL ; Update CR0
;
MOV   DX,3F0H       ;
MOV   AL,01H
OUT   DX,AL ; Point to CR1
MOV   DX,3F1H
MOV   AL,9FH
OUT   DX,AL ; Update CR1
;
MOV   DX,3F0H       ;
MOV   AL,02H
OUT   DX,AL ; Point to CR2
MOV   DX,3F1H
MOV   AL,0DCH
OUT   DX,AL ; Update CR2
;
MOV   DX,3F0H       ;
MOV   AL,03H
OUT   DX,AL ; Point to CR3
MOV   DX,3F1H
MOV   AL,00H
OUT   DX,AL ; Update CR3
;
;-----------------------------.
; EXIT CONFIGURATION MODE     |
;-----------------------------'
MOV   DX,3F0H
MOV   AX,0AAH
OUT   DX,AL
```

FDC37C651 Configuration Register Description

The configuration registers consist of five registers, the Configuration Select Register and Configuration Registers 0-3. The configuration select register is written to by writing to port 3F0H. The Configuration Registers 0-3 are accessed by reading or writing to port 3F1H.

Configuration Select Register (CSR)

This register can only be accessed when the FDC is in the CONFIGURATION MODE. This register, located at port 3F0H, must initialized upon entering the CONFIGURATION MODE before the configuration registers (CR0-CR3) can be accessed and is used to select which of the Configuration Registers are to be accessed at port 3F1H.

Configuration Registers 0-3

These registers are set to their default values at power up and are not affected by RESET. They are accessed at port 3F1H. CR0 is used to set the options for the oscillator, Baud Rate Generator and the FDC and IDE blocks. CR1 is used for allowing reading of the configuration registers and selecting options on the serial ports, IRQ signal and the parallel port. CR2 is used to set the options for the primary and secondary serial ports. CR3 is used to select the 48 MHz crystal option and setting the test modes of the chip.

CR0

This register can only be accessed when the FDC is in the CONFIGURATION MODE and after the CSR has been initialized to 00H. The default value of this register after power up is 3FH.

Table 23 - CR0

BIT NO.	BIT NAME	DESCRIPTION
0	IDE ENABLE	A high level on this bit, enables the IDE (Default). A low level on this bit disables the IDE.
1	IDE AT/XT	A high level on this bit sets the IDE to AT type (Default). A low level on this bit sets the IDE to XT type.
2	RESR	(This bit is Reserved - set to '0').
3	FDC POWER	A high level on this bit, supplies power to the FDC (Default). A low level on this bit puts the FDC in low power mode.
4	FDC ENABLE	A high level on this bit, enables the FDC (Default). A low level on this bit disables the FDC.
5,6	OSC	6 5 0 0 Osc ON, BR Generator (BRG) Clock Enabled. 0 1 Osc is On, BRG Clock is ON when PWRGD is active. When PWRGD is inactive, Osc is off and BRG Clock is Disabled (Default). 1 0 (same as 0 1 case) 1 1 Osc OFF, BR Generator Clock Disabled
7	VALID	A high level on this software controlled bit indicates that a valid configuration cycle has occurred. The control software must take care to set this bit at the appropriate times. Set to zero after power up.

CR1

This register can only be accessed when the FDC is in the CONFIGURATION MODE and after the CSR has been initialized to 01H. The default value of this register after power up is 9FH.

Table 24 - CR1

BIT NO.	BIT NAME	DESCRIPTION
0,1	Parallel Port Address	These bits are used to select the Parallel Port Address. 1 0 Parallel Port Address 0 0 Disabled 0 1 3BCH 1 0 378H 1 1 278H (Default)
2	Parallel Port Power	A high level on this bit, supplies power to the Parallel Port (Default). A low level on this bit puts the Parallel Port in low power mode.
3	Parallel Port Mode	Parallel Port Mode. A high level on this bit, sets the Parallel Port for Printer Mode (Default). A low level on this bit sets the Parallel Port for EXTENDED PARALLEL PORT MODE (Bi-directional).
4	IRQ Polarity	A high level on this bit, programs IRQ for active high, inactive low (Default). A low level on this bit programs IRQ for active low, inactive hi-Z.
5,6	COM3,4	Select the COM3 and COM4 address. 6 5 COM3 COM4 0 0 338H 238H (Default) 0 1 3E8H 2E8H 1 0 2E8H 2E0H 1 1 220H 228H
7	Enable CRx	A high level on this bit, enables the reading of CR0-CR3 (Default). A low level on this bit disables the reading of CR0-CR3.

CR2

This register can only be accessed when the FDC is in the CONFIGURATION MODE and after the CSR has been initialized to 02H. The default value of this register after power up is DCH.

Table 25 - CR2

BIT NO.	BIT NAME	DESCRIPTION
0,1	UART 1 Address Select	These bits select the Primary Serial Port Address. 1 0 COM Port ADDRESS 0 0 COM1 3F8H (Default) 0 1 COM2 2F8H 1 0 COM3 (Refer to CR1, bits 5,6) 1 1 COM4 (Refer to CR1, bits 5,6)
2	UART 1 Enable	A high level on this bit, enables the Primary Serial Port (Default). A low level on this bit disables the Primary Serial Port.
3	UART 1 Power down	A high level on this bit, allows normal operation of the Primary Serial Port (Default). A low level on this bit places the Primary Serial Port into Power Down Mode.
4,5	UART 2 Address Select	These bits select the Primary Serial Port Address. 1 0 COM Port ADDRESS 0 0 COM1 3F8H 0 1 COM2 2F8H (Default) 1 0 COM3 (Refer to CR1, bits 5,6) 1 1 COM4 (Refer to CR1, bits 5,6)
6	UART 2 Enable	A high level on this bit enables the Secondary Serial Port (Default). A low level on this bit disables the Secondary Serial Port.
7	UART 2 Power down	A high level on this bit, allows normal operation of the Secondary Serial Port (Default). A low level on this bit places the Secondary Serial Port into Power Down Mode.

CR3

This register can only be accessed when the FDC is in the CONFIGURATION MODE and after the CSR has been initialized to 03H. The default value of this register after power up is 00H.

Table 26 - CR3

BIT NO.	BIT NAME	DESCRIPTION
0	Reserved	Reserved - Program to zero (Default).
1	Reserved	Reserved for factory test of Data Separator - Program to zero (Default).
2	CLKEQ48	A high level on this bit indicates a 48 MHz crystal is used. This allows access to the 1 Mbps data rate. A low level on this bit indicates a 24 MHz crystal is used (Default).
3	Reserved	Reserved for factory test of Floppy Disk Controller - Program to zero (Default).
4,5	Reserved	Reserved for factory test of Floppy Disk Controller and Data Separator - Program to zero (Default).
6	Reserved	Reserved for factory test of Primary Serial Port - Program to zero (Default).
7	Reserved	Reserved for factory test of Secondary Serial Port - Program to zero (Default).

FDC37C652 Hardware Configuration

The FDC37C652 hardware configuration can select or deselect the arallel, serial, FDC and IDE circuits and set the parallel port and serial port addresses.

PCF1	PCF0	PARALLEL PORT ADDRESS
0	0	Disabled
0	1	3BCH
1	0	378H
1	1	278H

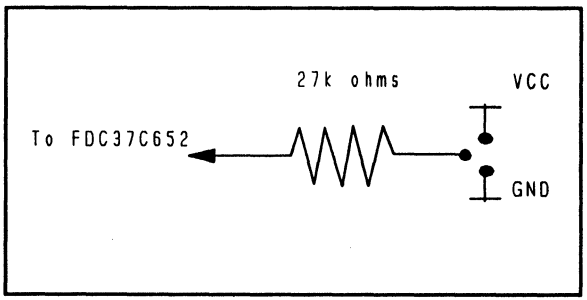
S1CF1	S1CF0	PRIMARY SERIAL PORT ADDRESS
0	0	Disabled
0	1	COM3 338H
1	0	COM2 2F8H
1	1	COM1 3F8H

S2CF1	S2CF0	SECONDARY SERIAL PORT ADDRESS
0	0	Disabled
0	1	COM4 238H
1	0	COM1 3F8H
1	1	COM2 2F8H

IDECF	IDE CONTROL
0	Disabled
1	Enabled

FDCCF	FDC CONTROL
0	Disabled
1	Enabled

In the FDC37C652, the pins used to configure the part should be connected as per the diagram below. This shows how a jumper can be used to set a high (VCC) or a low (GND) into the port for configuration at the end of the reset pulse.



OPERATIONAL DESCRIPTION

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range . . . . . 0°C to +70°C
Storage Temperature Range . . . . . -55° to +150°C
Lead Temperature Range (soldering, 10 seconds) . . . . . +325°C
Positive Voltage on any pin, with respect to Ground . . . . . V_{CC}+0.3V
Negative Voltage on any pin, with respect to Ground . . . . . -0.3V
Maximum V_{CC} . . . . . +7V

*Stresses above those listed above could cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied.

Note: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

DC ELECTRICAL CHARACTERISTICS (T_A = 0°C - 70°C, V_{CC} = +5.0 V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
I Type Input Buffer						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0			V	
IS Type Input Buffer						
Low Input Level	V_{ILIS}	0.8			V	Schmitt Trigger
High Input Level	V_{IHIS}			2.2	V	Schmitt Trigger
Schmitt Trigger Hysteresis	V_{HYS}		250		mV	
I_{CLK} Input Buffer						
Low Input Level	V_{ILCK}	0.4			V	
High Input Level	V_{IHCK}			3.0	V	

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
Input Leakage (All I and IS buffers except PWRGD)						
Low Input Leakage	I_{IL}	-10		+10	μA	V_{IN} = 0
High Input Leakage	I_{IH}	-10		+10	μA	V_{IN} = V_{CC}
Input Current PWRGD	I_{OH}		75	150	μA	V_{IN} = 0

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
I/O24 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 24 mA
High Output Level	V_{OH}	2.4			V	V_{OH} = -12 mA
Output Leakage	I_{OL}	-10		+10	μA	V_{IN} = 0 to V_{CC} (Note 1)
O24 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 24 mA
High Output Level	V_{OH}	2.4			V	V_{OH} = -12 mA
Output Leakage	I_{OL}	-10		+10	μA	V_{IN} = 0 to V_{CC} (Note 1)
OD48 Type Buffer						
Low Output Level	V_{OL}			0.4	V	V_{OL} = 48 mA
Output Leakage	I_{OH}	-10		+10	μA	V_{OH} = 0 to V_{CC} (Note 2)

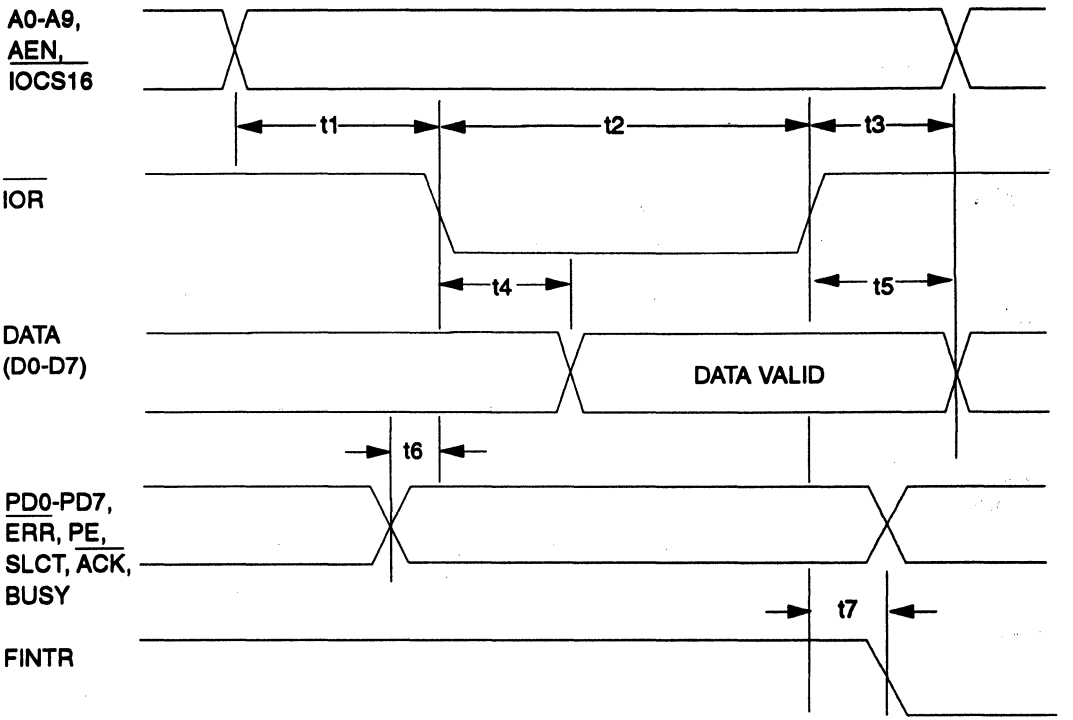
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
O4 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 4 mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -1 mA
Output Leakage	I_{OL}	-10		+10	μA	V_{IN} = 0 to V_{CC} (Note 1)
OD24 Type Buffer						
Low Output Level	V_{OL}			0.4	V	V_{OL} = 24 mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -50 μA
Output Leakage	I_{OL}	-10		+10	μA	V_{IN} = 0 to V_{CC} (Note 1)
Suppy Current Active	I_{CC}			40	mA	All outputs open.
Supply Current Standby	I_{CSBY}		300	500	μA	Note 3

Note 1: All output leakages are measured with the current pins in high impedance as defined by the PWRGD pin (FDC37C651 only).
Note 2: Output leakage is measured with the low driving output off, either for a high level output or a high impedance state defined by PWRGD (FDC37C651 only).
Note 3: Defined by the device configuration with the PWRGD input low.

CAPACITANCE T_A = 25°C; fc = 1MHz; V_{CC} = 5V

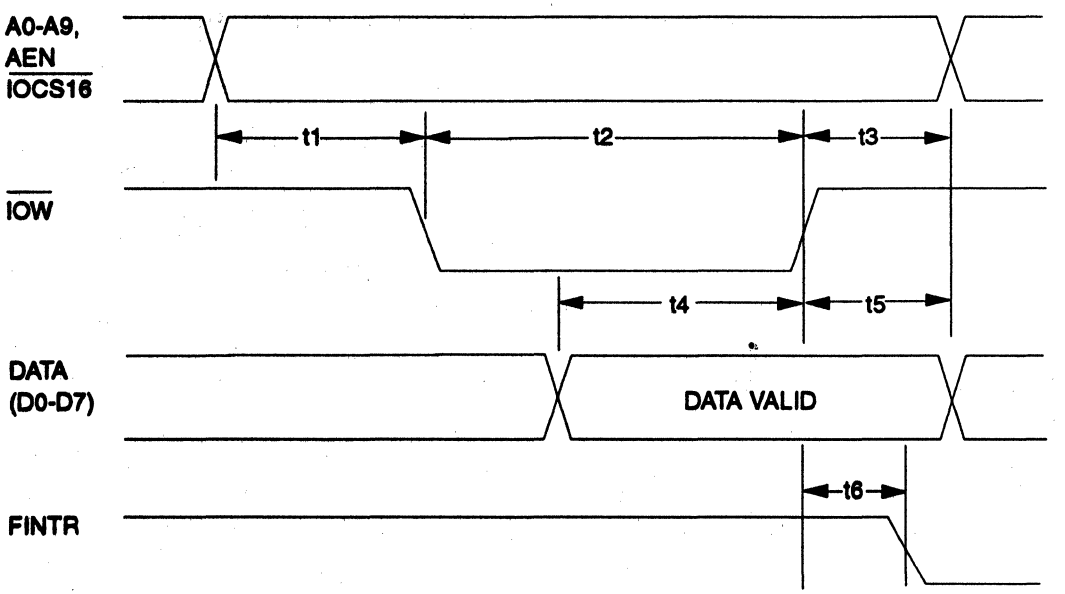
PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITION
		MIN	TYP	MAX		
Clock Input Capacitance	C_{IN}			20	pF	All pins except pin under test tied to AC ground
Input Capacitance	C_{IN}			10	pF	
Output Capacitance	C_{OUT}			20	pF	

TIMING DIAGRAMS



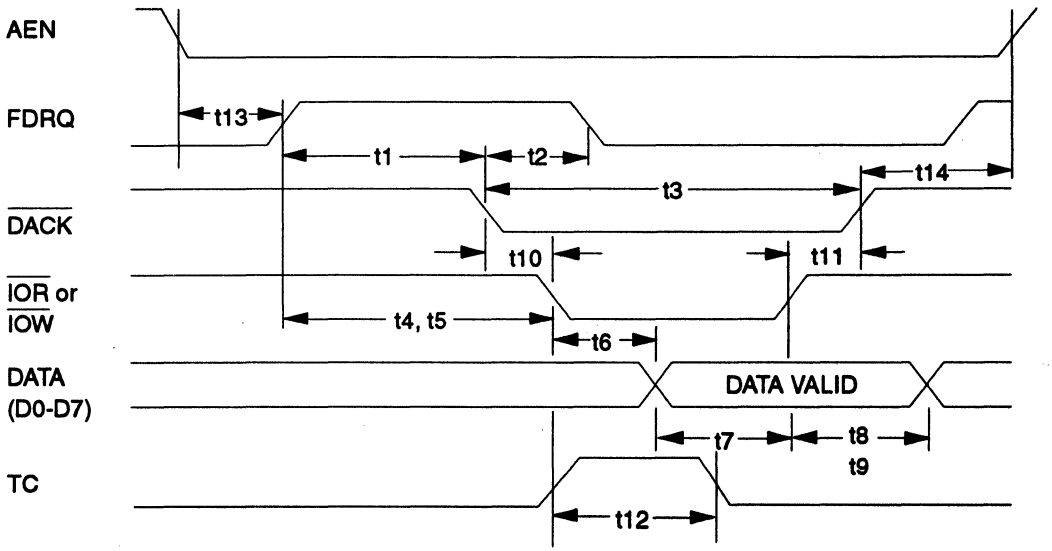
	Parameter	min	typ	max	units
t1	A0-A9, AEN, IOCS16 Set Up to IOR Low	40			ns
t2	IOR Width	150			ns
t3	A0-A9, AEN, IOCS16 Hold from IOR High	10			ns
t4	Data Access Time from IOR Low			100	ns
t5	Data to Float Delay from IOR High	10		60	ns
t6	Port Setup		20		ns
t7	Read Strobe to Clear FINTR		40	55	ns

FIGURE 5 - MICROPROCESSOR READ TIMING



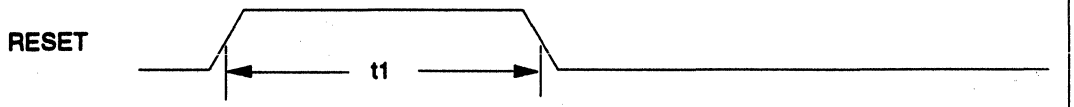
	Parameter	min	typ	max	units
t1	A0-A9, AEN, IOCS16 Set Up to IOW Low	40			ns
t2	IOW Width	150			ns
t3	A0-A9, AEN, IOCS16 Hold from IOW High	10			ns
t4	Data Set Up Time to IOW High	40			ns
t5	Data Hold Time from IOW High	10			ns
t6	Write Strobe to Clear FINTR		40	55	ns

FIGURE 6 - MICROPROCESSOR WRITE TIMING



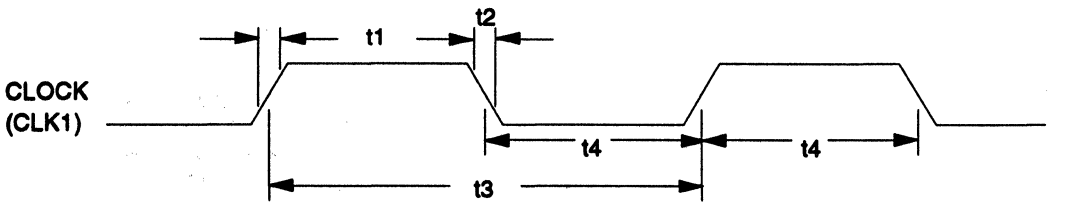
	Parameter	min	typ	max	units
t1	DACK Delay Time from FDRQ High	0			ns
t2	FDRQ Reset Delay from DACK Low			140	ns
t3	DACK Width	150			ns
t4	IOR Delay from FDRQ High	0			ns
t5	IOW Delay from FDRQ High	0			ns
t6	Data Access Time from IOR Low			100	ns
t7	Data Set Up Time to IOW High	40			ns
t8	Data to Float Delay from IOR High	10		60	ns
t9	Data Hold Time from IOW High	10			ns
t10	DACK Set Up to IOW/IOR Low	5			ns
t11	DACK Hold After IOW/IOR High	10			ns
t12	TC Pulse Width	60			ns
t13	AEN Set Up to IOR/IOW	40			ns
t14	AEN Hold from DACK	10			ns

FIGURE 7 - DMA TIMING



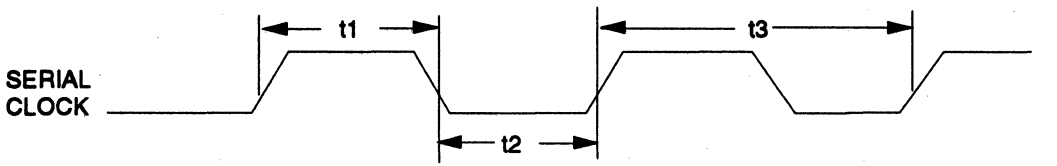
	Parameter	min	typ	max	units
t1	RESET Width	500			ns

FIGURE 8 - RESET TIMING



	Parameter	min	typ	max	units
t1	Clock Rise Time (VIN = 0.4 to 3.0)			5	ns
t2	Clock Fall Time (VIN = 3.0 to 0.4)			5	ns
t3	Clock Period	40	41.67		ns
t4	Clock Active (High or Low)	14			ns

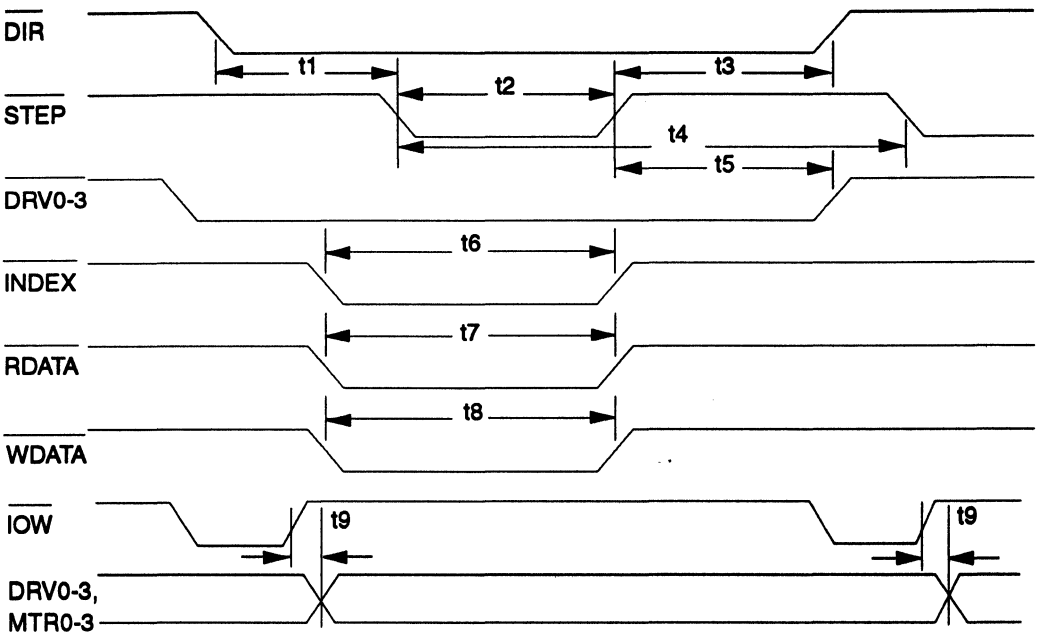
FIGURE 9 - CLOCK TIMING



	Parameter	min	typ	max	units
t1	Serial Clock High Pulse Width	250			ns
t2	Serial Clock Low Pulse Width	250			ns
t3	Serial Clock Period		541.67		ns

Note: t3 = 13 x period CLK1 (t3 Figure 9).

FIGURE 10 - SERIAL CLOCK TIMING

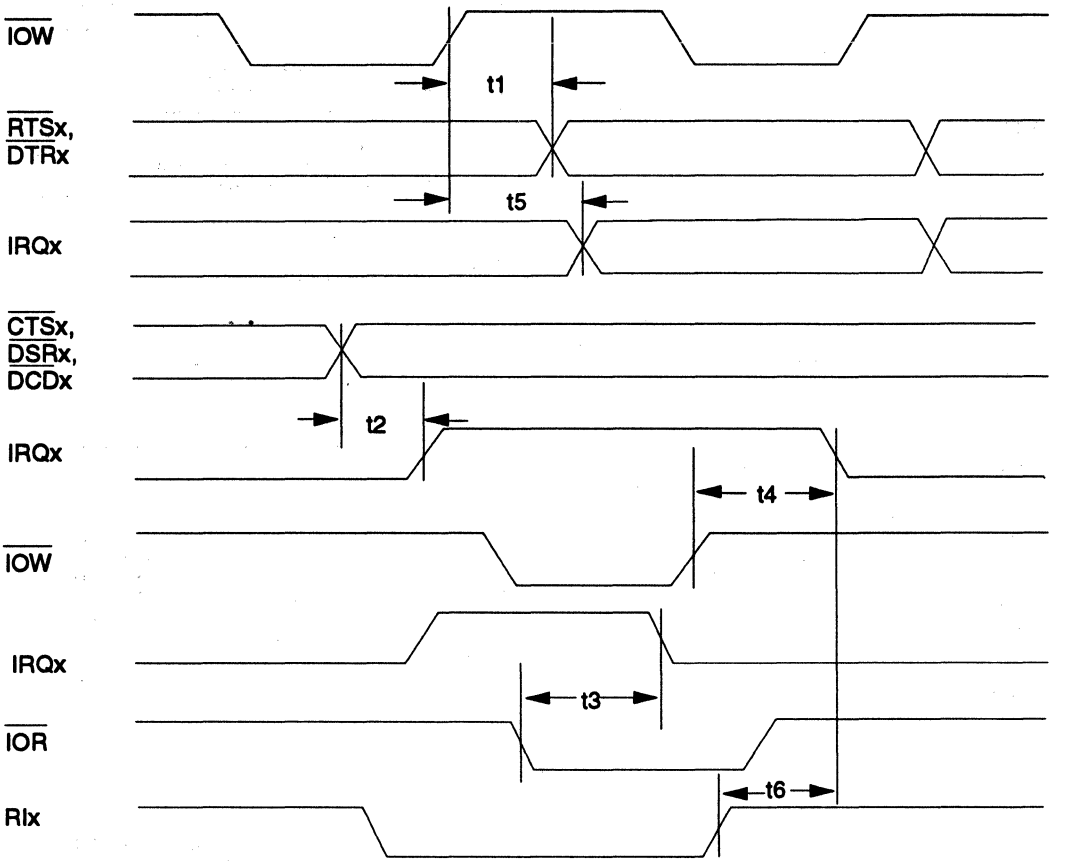


(AT Mode timing only)

	Parameter	min	typ	max	units
t1	DIR Set Up to STEP Low		4		X*
t2	STEP Active Time Low		24		X*
t3	DIR Hold Time After STEP		96		X*
t4	STEP Cycle Time		132		X*
t5	DRV0-3 Hold Time from STEP Low		20		X*
t6	INDEX Pulse Width		2		X*
t7	RDATA Active Time Low		40		ns
t8	WDATA Write Data Width Low		.5		Y*
t9	DRV0-3, MTR0-3 from End of IOW		25		ns

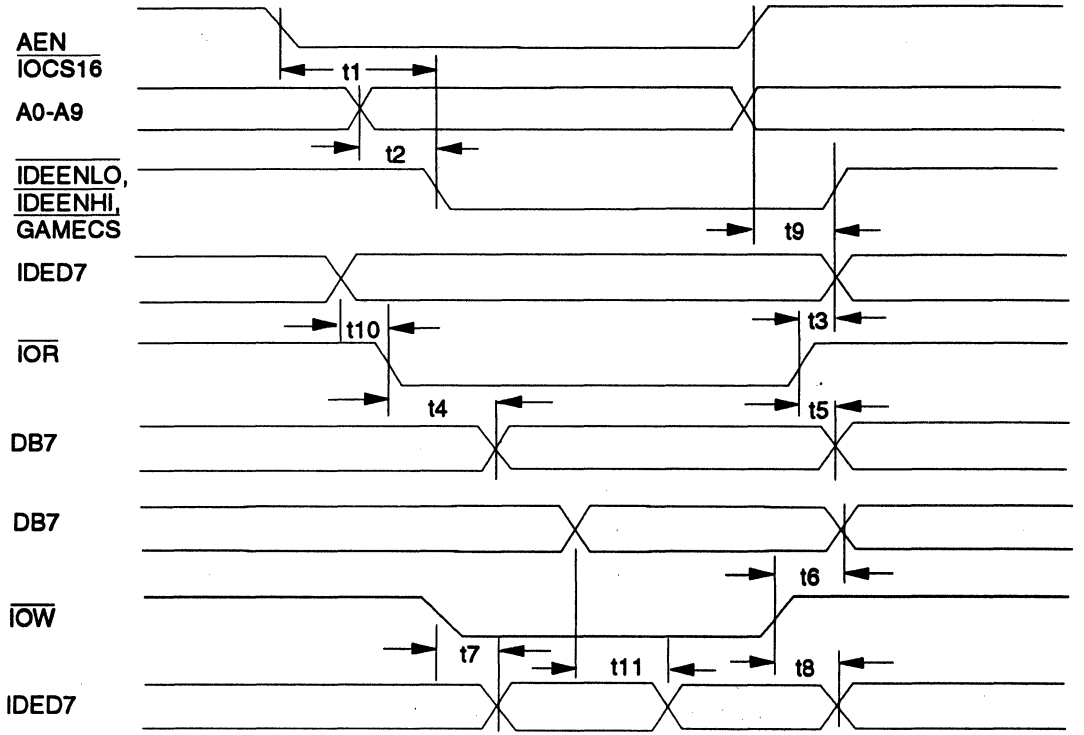
*X specifies one MCLK period and Y specifies one WCLK period.
MCLK = Controller Clock to FDC (See Table 6).
WCLK = 2 x Data Rate (See Table 6).

FIGURE 11 - DISK DRIVE TIMING



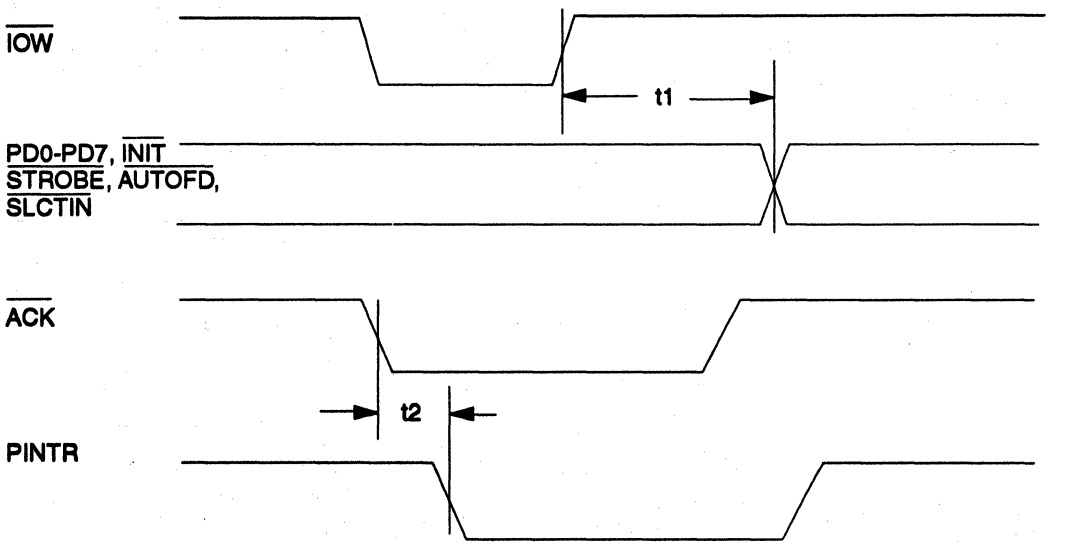
	Parameter	min	typ	max	units
t1	RTSx, DTRx Delay from IOW			200	ns
t2	IRQx Active Delay from CTSx, DSRx, DCDx			100	ns
t3	IRQx Inactive Delay from IOR (Leading Edge)			120	ns
t4	IRQx Inactive Delay from IOW (Trailing Edge)			125	ns
t5	IRQx Inactive Delay from IOW	10		100	ns
t6	IRQx Active Delay from RIx			100	ns

FIGURE 12 - SERIAL PORT TIMING



	Parameter	min	typ	max	units
t1	IDEENLO, IDEENHI, GAMECS Delay from AEN, IOCS16			40	ns
t2	IDEENLO, IDEENHI, GAMECS Delay from A0-A9			40	ns
t3	IDED7 Hold Time after IOR	10			ns
t4	DB7 Delay from IOR			60	ns
t5	DB7 Hold Time from IOR	10		60	ns
t6	DB7 Hold Time from IOW	10			ns
t7	IDED7 Delay from Data Bus IOW Active			50	ns
t8	IDED7 Inactive Delay from IOW	10		50	ns
t9	IDEENLO Delay from IDEENHI, IOCS16, AEN			40	ns
t10	IDED7 Set Up Time before IOR	40			ns
t11	IDED7 Delay from DB7, IDED7 in Output Mode			25	

FIGURE 13 - IDE INTERFACE TIMING



	Parameter	min	typ	max	units
t1	PD0-7, INIT, STROBE, AUTOFD Delay from IOW			100	ns
t2	PINTR Delay from ACK			60	ns

FIGURE 14 - PARALLEL PORT TIMING

STANDARD MICROSYSTEMS CORPORATION
COMPONENT PRODUCTS DIVISION