TEXAS INSTRUMENTS

Designing With The TI486SXL2-G

Converting Existing 486-Based Microprocessor Designs

Application Report

1995

PC Systems Products

Designing With the TI486SXL2-G

Converting Existing 486-Based Microprocessor Designs

Applications Engineering
PC Systems Products
Semiconductor Group

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1 Introduction

The purpose of this document is to assist the system designer in converting existing 5-V TI486 designs to the TI486SXL(C)-G device. The TI486SXL(C)-G is a 3.3-V device (3.6 V for the TI486SXL2-G66) with 5-V-tolerant I/Os.

The following topics are contained in this document:

- Converting 5-V designs that use the 100-pin QFP TI486SLC/E and the TI486SXLC2 to accommodate the 100-pin QFP TI486SXLC2-G
- Converting 5-V designs that use the 132-pin CPGA TI486DLC/E to accommodate the 144-pin QFP TI486SXL2-G
- Converting 5-V designs that use the 144-pin QFP or the 168-pin CPGA TI486SXL2 to accommodate the 144-pin QFP or the 168-pin CPGA TI486SXL2-G
- Converting 5-V designs that use the 486SX and 486DX to accommodate the 168-pin CPGA TI486SXL2-G

The TI486 provides the lowest cost 486 solution as well as the fastest 3.3-V (3.6 V for the TI486SXL2-G66) 486SX2-class microprocessor on the market today. In addition to providing the performance required for today's PCs, the TI486 microprocessors offer a low-cost system bus interface (chipset and coprocessor). By using the TI486 microprocessor, system designers are given the flexibility to support a wide range of CPUs on the same motherboard while providing their customer base the option of selecting the price/performance point that best meets their needs. A summary of the features and benefits is provided in Table 1. Table 2 shows the primary bus handling and on-chip cache capabilities.

Table 1. Features and Benefits

Feature	Benefit(s)
Fastest 3.3-V 486SX2 available	Ideal entry-level price/performance point
60% power savings over 5-V CPU	Longer battery life, smaller power supply, and no heatsinks or fans at frequencies up to 50 MHz
Low-end alternative to DX2/4 designs	Wider product offerings, CPU/product flexibility
SMM/SMI, power management, static core, suspend mode	Enhanced power savings
Coprocessor interface	CPU plus coprocessor: Low-cost DX2 positioning
168-CPGA, 144-QFP, and 100-QFP packaging	Flexibility, low cost

Table 2. Bus, Cache, and Byte Handling Capabilities

Description	TI486SXLC2-G50 (100-pin QFP)	TI486SXL2-G50 and TI486SXL2-G66 (144-pin QFP and 168-pin CPGA)
Data bus	16-bits wide (D15–D0)	32-bits wide (D31–D0)
Address bus	A23–A1	A31–A2
On-chip cache	8K-byte, 2-way set associative	8K-byte, 2-way set associative
Byte enables	2 byte enables used (BHE#, BLE#)	4 byte enables used (BE3#–BE0#)

2 Converting 100-Pin QFP TI486SLC/E and TI486SXLC2 5-V Designs

The TI486SXLC2-G microprocessor is ideal for low-cost, 16-bit solutions. This microprocessor achieves a 60% CPU power savings over 5-V designs and features a 32-bit internal/16-bit external bus, on-chip 8K-byte cache, and clock-doubled performance. The microprocessor has 5-V-tolerant I/Os that eliminate the need for translation buffers when used in a mixed voltage system. This section details the modifications necessary to support a variety of TI486 microprocessors in the same design, specifically the TI486SLC/E, the TI486SXLC2, and the TI486SXLC2-G.

2.1 Design Considerations

The following design-related issues should be considered when converting 5-V designs to mixed-voltage designs with 5-V-tolerant I/Os:

- For 66-MHz designs, the recommended operating voltage range is 3.6 ± 0.1 V, and the maximum case temperature is 65°C. To operate within this case temperature limit, a heat sink fin is included with all 66-MHz devices.
- To ensure that reliability specifications are achieved, output and I/O loading must not exceed 100 pF and I/O and bus contention must be prevented.
- A voltage regulator is required to supply 3.3 V (3.6 V for the TI486SXLC2-G66) to the V_{CC} terminals and 5 V to the V_{CC5} terminal.
- The 3.3-V V_{CC} can be no more than 1 V greater than V_{CC5} during power up. In a pure 3.3-V only system (3.6 V for the TI486SXLC2-G66), V_{CC5} should be connected to the V_{CC} supply (3.3 or 3.6 V).
- Connect (short) all V_{CC} terminals to the 3.3-V (3.6 V for the TI486SXLC2-G66) output of the voltage regulator.
- Connect the V_{CC5} terminal (terminal 45) to the 5-V input of the voltage regulator.
- Leave electrically open (unconnected) all NC terminals.

2.2 Hardware Modifications

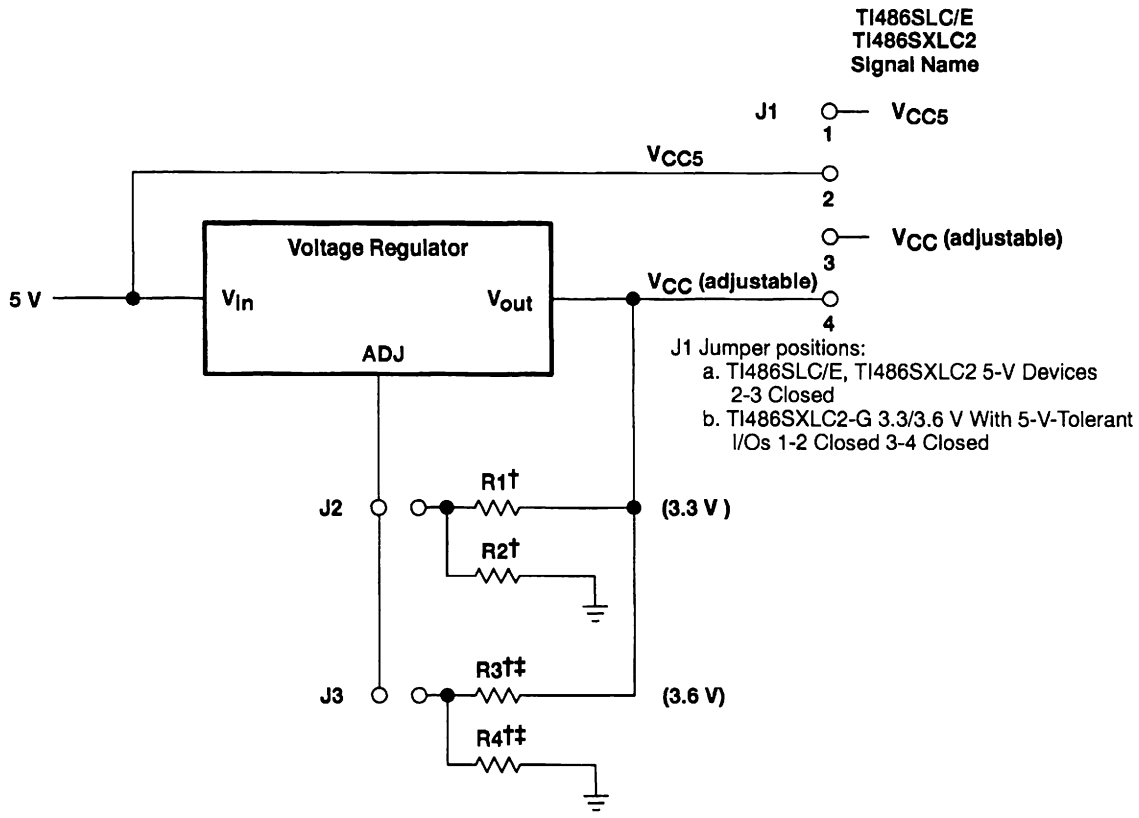
The modifications for address bit A20 masking (A20M) and general cache invalidation described in Appendix C, *Design Considerations and Cache Flush* of the *TI486SXLC and TI486SXL Microprocessors Reference Guide* (SRZU006D), should be implemented.

2.3 BIOS Modifications

The BIOS modifications required for supporting the TI486 products, outlined in Appendix B, *BIOS Modifications Guide* of the *TI486SXLC and TI486SXL Microprocessors Reference Guide* (SRZU006D), should be implemented. In addition, if system management mode (SMM) is being implemented, Appendix A, *SMM Programmer's Guide* of the *TI486SXLC and TI486SXL Microprocessors Reference Guide* should be consulted.

2.4 Jumpers

Figure 1 shows an example of the recommended voltage regulation implementation.



†Consult voltage regulator specifications for resistor values. By using higher resistor values (> 100 kΩ) power loss through the unused resistor pairs will be reduced.

‡In order to achieve the 0.1 V tolerance at 66MHz (3.6 ± 0.1 V), use 1% precision resistors for voltage adjustment.

Figure 1. V_{CC} Options for 100-Pin QFP

2.5 Voltage Regulator

A list of recommended voltage regulators is included in Listing 1 on page 13. This is a partial list and is not meant to be all inclusive.

2.6 Signal/Pin Differences

The signal/pin differences between the three processors occur on pin number 45. Table 3 shows the correct termination for each processor.

Table 3. 100-Pin Signal/Pin Differences

Pin Number	SLC/E	SXLC	SXLC2-G
45	NC	NC	V_{CC5}

2.7 Chipset Support

A list of chipset vendors providing solutions that support the the TI486SXLC2-G interface has been compiled from information received from the specified chipset vendors (see Listing 2 on page 14 and Listing 3 on page 16). This is a partial list and is not meant to be all inclusive.

3 Converting 132-Pin CPGA TI486DLC/E 5-V Designs

The TI486SXL2-G achieves a 60% CPU power savings over 5-V designs and features a full 32-bit bus, on-chip 8K-byte cache, and clock-doubled performance. The microprocessor has 5-V-tolerant I/Os that eliminate the need for translation buffers when used in a mixed voltage system. This section details the modifications necessary to convert an existing 5-V TI486DLC/E (132-pin CPGA) design to the 144-pin TI486SXL2-G (3.3/3.6-V with 5-V-tolerant I/Os).

3.1 Design Considerations

The following design-related issues should be considered when converting 5-V designs to mixed-voltage designs with 5-V-tolerant I/Os:

- For 66-MHz designs, the recommended operating voltage range is 3.6 ± 0.1 V, and the maximum case temperature is 65°C. To operate within this case temperature limit, a heat sink fin is included with all 66-MHz devices.
- To insure that reliability specifications are achieved, output and I/O loading must not exceed 100 pF and I/O and bus contention must be prevented.
- A voltage regulator is required to supply 3.3 V (3.6 V for the TI486SXL2-G66) to the V_{CC} terminals and 5 V to the V_{CC5} terminal.
- The 3.3-V V_{CC} can be no more than 1 V greater than V_{CC5} during power up. In a pure 3.3-V only system (3.6 V for the TI486SXL2-G66), V_{CC5} should be connected to the V_{CC} supply (3.3 or 3.6 V).
- Connect (short) all V_{CC} terminals to the 3.3-V (3.6 V for the TI486SXL2-G66) output of the voltage regulator.
- Connect the V_{CC5} terminal (terminal 47) to the 5-V input of the voltage regulator.
- Connect (short) both W/R# terminals (36 and 37) together and connect to the W/R# signal source.
- Leave electrically open (unconnected) all NC terminals.

3.2 Hardware Modifications

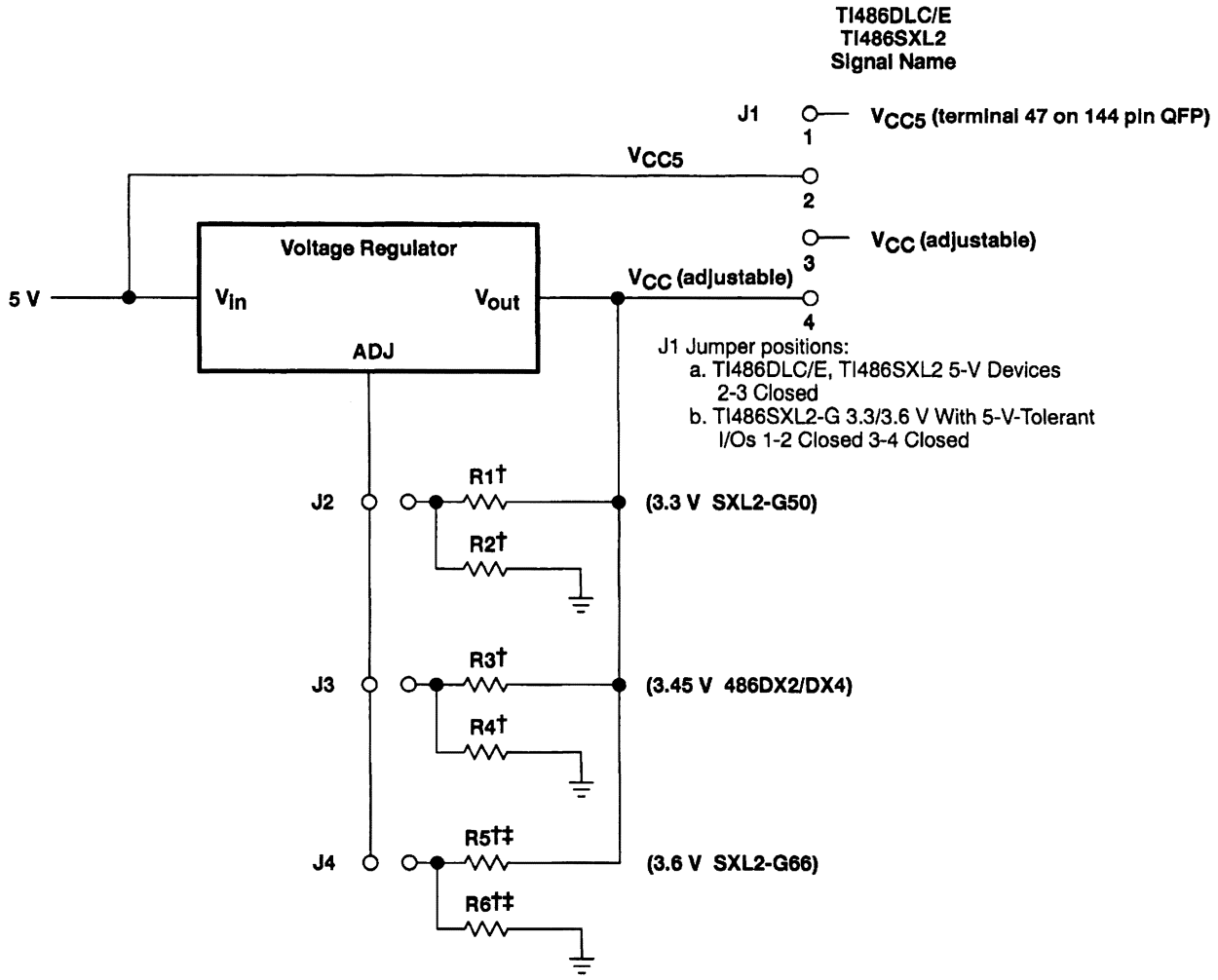
The modifications for address bit A20 masking (A20M) and general cache invalidation described in Appendix C, *Design Considerations and Cache Flush*, of the *TI486SXLC and TI486SXL Microprocessors Reference Guide* (SRZU006D), should be implemented.

3.3 BIOS Modifications

The BIOS modifications required for supporting the TI486 products that are outlined in Appendix B, *BIOS Modifications Guide*, of the *TI486SXLC and TI486SXL Microprocessors Reference Guide* (SRZU006D), should be implemented. In addition, if system management mode (SMM) is being implemented, Appendix A, *SMM Programmer's Guide* of the *TI486SXLC and TI486SXL Microprocessors Reference Guide* should be consulted.

3.4 Jumpers

Figure 2 shows an example of the recommended voltage regulation implementation.



†Consult voltage regulator specifications for resistor values. By using higher resistor values (> 100 kΩ) power loss through the unused resistor pairs will be reduced.

‡In order to achieve the 0.1 V tolerance at 66MHz (3.6 ± 0.1 V), use 1% precision resistors for voltage adjustment.

Figure 2. V_{CC} Sources for 144-Pin QFP

3.5 Voltage Regulator

A list of recommended voltage regulators is included in Listing 1 on page 13. This is a partial list and is not meant to be all inclusive.

3.6 Chipset Support

A list of chipset vendors providing solutions that support the TI486SXL2-G interface has been compiled from information received from the specified chipset vendors (see Listing 2 on page 14 and Listing 3 on page 16). This is a partial list and is not meant to be all inclusive.

4 Converting 144-Pin QFP or 168-Pin CPGA 5-V Designs

The TI486SXL2-G microprocessor achieves a 60% CPU power savings over 5-V designs and features a full 32-bit bus, on-chip 8K-byte cache, and clock-doubled performance. The microprocessor has 5-V-tolerant I/Os that eliminate the need for translation buffers when used in a mixed voltage system. This section details the modifications necessary to convert an existing 5-V TI486SXL2 (144-pin QFP or 168-pin CPGA) design to the 144-pin QFP or 168-pin CPGA TI486SXL2-G.

4.1 Design Considerations

The following design-related issues should be considered when converting 5-V designs to mixed-voltage designs with 5-V-tolerant I/Os:

- For 66-MHz designs, the recommended operating voltage range is 3.6 ± 0.1 V, and the maximum case temperature is 65°C. To operate within this case temperature limit, a heat sink fin is included with all 66-MHz devices.
- To insure that reliability specifications are achieved, output and I/O loading must not exceed 100 pF and I/O and bus contention must be prevented.
- A voltage regulator is required to supply 3.3 V (3.6 V for the TI486SXL2-G66) to the V_{CC} terminals and 5 V to the V_{CC5} terminal.
- The 3.3-V V_{CC} can be no more than 1 V greater than V_{CC5} during power up. In a pure 3.3-V only system (3.6 V for the TI486SXL2-G66), V_{CC5} should be connected to the V_{CC} supply (3.3 or 3.6 V).
- Connect (short) all V_{CC} terminals to the 3.3-V (3.6 V for the TI486SXL2-G66) output of the voltage regulator.
- Connect the V_{CC5} terminal (see Figure 3) to the 5-V input of the voltage regulator.
- Connect (short) both W/R# terminals (36 and 37) on the 144-pin QFP together and connect to the W/R# signal source.
- Leave electrically open (unconnected) all NC terminals.

4.2 Hardware Modifications

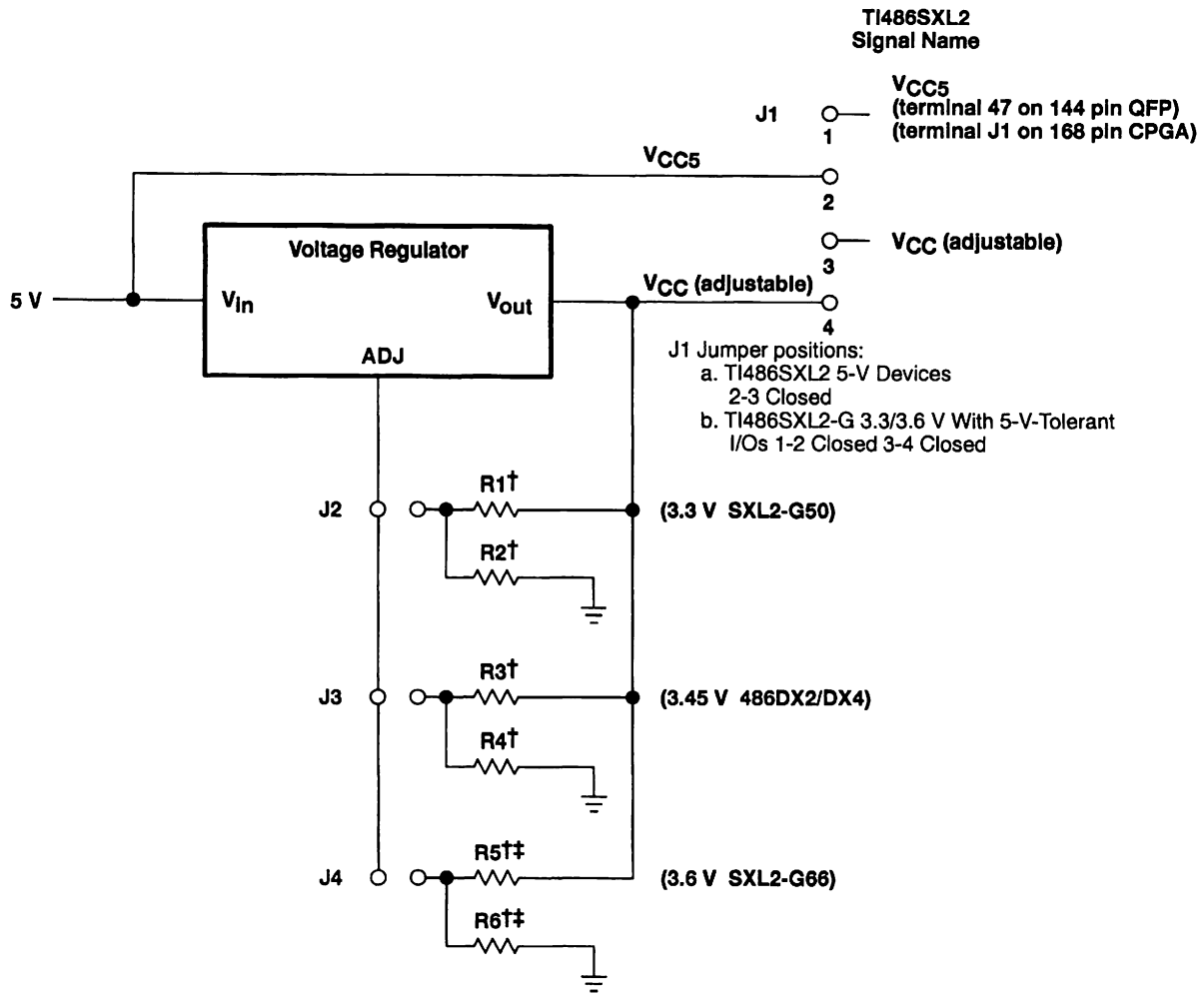
The modifications for address bit A20 masking (A20M) and general cache invalidation described in Appendix C, *Design Considerations and Cache Flush*, of the *TI486SXLC and TI486SXL Microprocessors Reference Guide* (SRZU006D) should be implemented.

4.3 BIOS Modifications

The BIOS modifications required for supporting the TI486 products that are outlined in Appendix B, *BIOS Modifications Guide*, of the *TI486SXLC and TI486SXL Microprocessors Reference Guide* (SRZU006D) should be implemented. In addition, if system management mode (SMM) is being implemented, Appendix A, *SMM Programmer's Guide*, of the *TI486SXLC and TI486SXL Microprocessors Reference Guide* should be consulted.

4.4 Jumpers

Figure 3 shows an example of the recommended voltage regulation implementation.



†Consult voltage regulator specifications for resistor values. By using higher resistor values (> 100 kΩ) power loss through the unused resistor pairs will be reduced.

‡In order to achieve the 0.1 V tolerance at 66MHz (3.6 ± 0.1 V), use 1% precision resistors for voltage adjustment.

Figure 3. V_{CC} Sources for 144-Pin QFP and 168-Pin CPGA

4.5 Voltage Regulator

A list of recommended voltage regulators is included in Listing 1 on page 13. This is a partial list and is not meant to be all inclusive.

4.6 Signal/Pin Differences

Signal/pin differences between the processors occur on the pins listed in Table 4 and Table 5. These tables show the correct termination for each processor.

Table 4. 144-Pin Signal/Pin Differences

Pin Number	144-Pin DLC/E (5 V)	144-Pin SXL2 (5 V)	144-Pin SXL2-G (3.3-V With 5-V-Tolerant I/Os or 3.6-V With 5-V-Tolerant I/Os at 66 MHz)
47	NC	NC	V_{CC5}
66	NC	MEMW#	MEMW#

Table 5. 168-Pin Signal/Pin Differences

Pin Number	168-Pin SXL2 (5 V)	168-Pin SXL2-G (3.3-V With 5-V-Tolerant I/Os or 3.6-V With 5-V-Tolerant I/Os at 66 MHz)
J1	V_{CC}	V_{CC5}

4.7 Chipset Support

A list of chipset vendors providing solutions that support the TI486 interface has been compiled from information received from the specified chipset vendors (see Listing 2 on page 14 and Listing 3 on page 16). This is a partial list and is not meant to be all inclusive.

5 Converting 168-Pin 486SX or 486DX 5-V Designs

The TI486SXL2-G microprocessor is packaged in the 168-pin CPGA to offer a more cost-efficient solution to the 486SX and 486DX. In order to simplify this design, the system logic must support both the 386 and 486 bus interfaces. The TI486SXL2-G achieves a 60% CPU power savings over 5-V designs and features a full 32-bit bus, on-chip 8K-byte cache, and clock-doubled performance. The microprocessor has 5-V-tolerant I/Os that eliminate the need for translation buffers when used in a mixed voltage system. This section details the modifications required to support the TI486SXL2-G, the 486SX, and the 486DX in the same design.

5.1 Design Considerations

The following design-related issues should be considered:

- The board design requires the use of system logic that supports both the 386 and 486 bus interfaces. Since board modifications for the TI486SXL2-G support are system logic dependent, the implementation details are left to the board designer. The final responsibility for verifying designs incorporating any version of a TI486 microprocessor rests with the customer originating the motherboard design.
- For 66-MHz designs, the recommended operating voltage range is 3.6 ± 0.1 V, and the maximum case temperature is 65°C. To operate within this case temperature limit, a heat sink fin is included with all 66-MHz devices.
- To insure that reliability specifications are achieved, output and I/O loading must not exceed 100 pF and I/O and bus contention must be prevented.
- A voltage regulator is required to supply 3.3 V (3.6 V for the TI486SXL2-G66) to the V_{CC} terminals and 5 V to the V_{CC5} terminal.
- The 3.3-V V_{CC} can be no more than 1 V greater than V_{CC5} during power up. In a pure 3.3-V only system (3.6 V for the TI486SXL2-G66), V_{CC5} should be connected to the V_{CC} supply (3.3 or 3.6 V).
- Connect (short) all V_{CC} terminals to the 3.3-V (3.6 V for the TI486SXL2-G66) output of the voltage regulator.
- Connect the V_{CC5} terminal (terminal J1) to the 5-V input of the voltage regulator.
- Leave electrically open (unconnected) all NC terminals.

5.2 Hardware Modifications

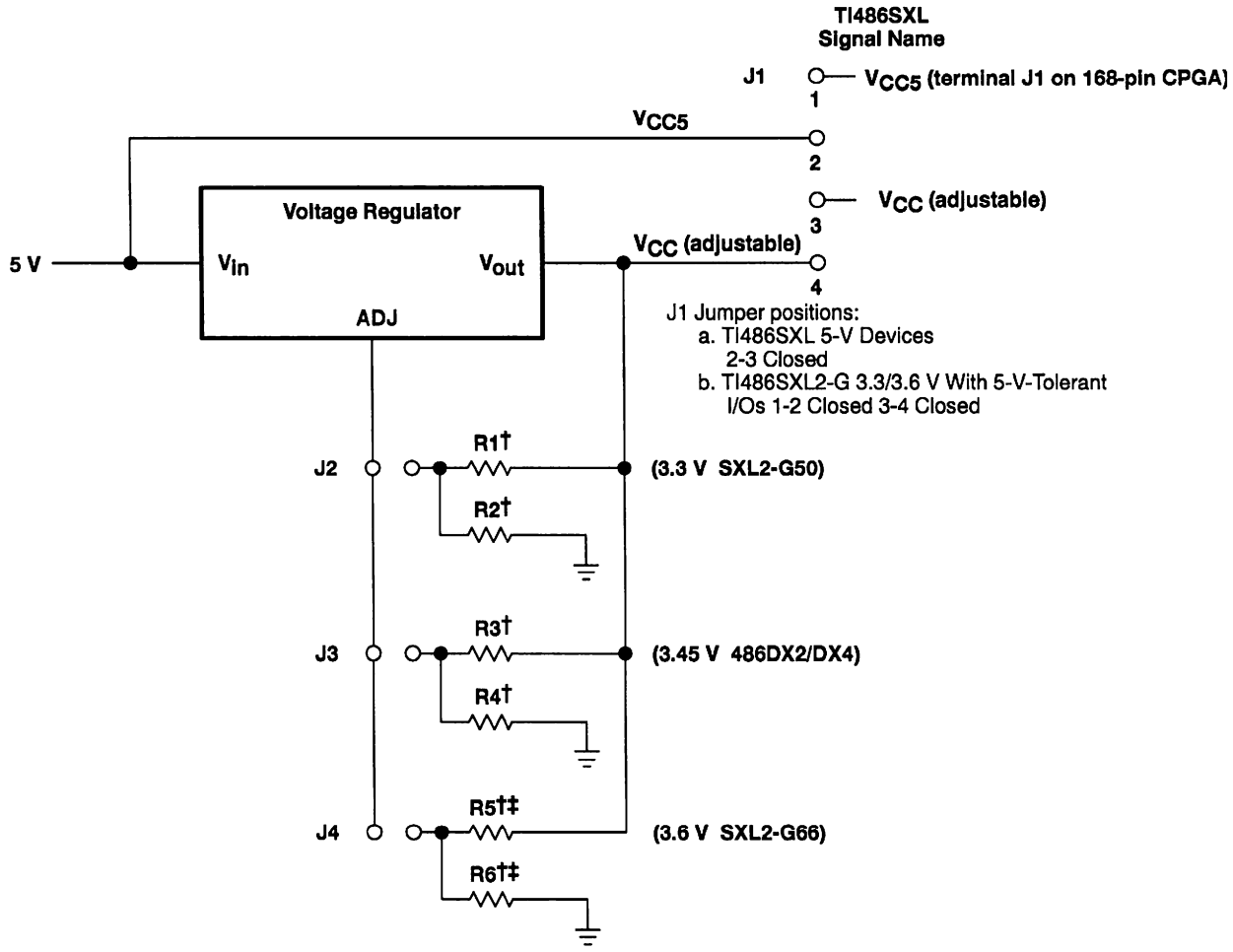
The modifications for address bit A20 masking (A20M) and general cache invalidation described in Appendix C, *Design Considerations and Cache Flush*, of the *TI486SXLC and TI486SXL Microprocessors Reference Guide* (SRZU006D) should be implemented. In addition, the modifications necessary to implement the 168-pin TI486SXL2-G in an existing 486SX/DX motherboard design are outlined in Appendix D, *OEM Modifications for 168-Pin CPGA*, of the *TI486SXLC and TI486SXL Microprocessors Reference Guide* (SRZU006D).

5.3 BIOS Modifications

The BIOS modifications required for supporting the TI486 products that are outlined in Appendix B, *BIOS Modifications Guide*, of the *TI486SXLC and TI486SXL Microprocessors Reference Guide* (SRZU006D) should be implemented. In addition, if system management mode (SMM) is being implemented, Appendix A, *SMM Programmer's Guide*, of the *TI486SXLC and TI486SXL Microprocessors Reference Guide* should be consulted.

5.4 Jumpers

Figure 4 shows an example of the recommended voltage regulation implementation.



†Consult voltage regulator specifications for resistor values. By using higher resistor values (> 100 kΩ) power loss through the unused resistor pairs will be reduced.

‡In order to achieve the 0.1 V tolerance at 66MHz (3.6 ± 0.1 V), use 1% precision resistors for voltage adjustment.

Figure 4. VCC Sources for the 168-Pin CPGA

5.5 Voltage Regulator

A list of recommended voltage regulators is included in Listing 1 on page 13. This is a partial list and is not meant to be all inclusive.

5.6 Signal/Pin Differences

Signal/pin differences between the three processors occur on the pins listed in Table 6. The table shows the correct termination for each processor.

Table 6. 168-Pin SX/DX Signal/Pin Differences

Pin Number	168-Pin TI486SXL2-G	486SX	486DX
A3	NC	NC	TCK
A5	NC	DP3	DP3
A12	ERROR#	NC	NC
A13	NA#	NC	NC
A14	NC	NC	TDI
A17	NC	AHOLD	AHOLD
B10	SMI#	NC	NC
B12	SUSPA#	NC	NC
B13	SMADS#	NC	NC
B14	NC	NC	TMS
B15	NC	NC	NMI
B16	MEMW#	NC	TDO
B17	NC	EADS#	EADS#
C3	CLK2	CLK	CLK
C11	FLT#	NC	NC
C12	NC	NC	NC
C13	SUSP#	NC	NC
C14	NC	NC	FERR#
D16	NC	BS8#	BS8#
D17	NC	BOFF#	BOFF#
F1	NC	DP1	DP1
H3	NC	DP2	DP2
H15	NC	BRDY#	BRDY#
J1	V_{CC5}	V_{CC}	V_{CC}
J17	NC	PCD	PCD
L15	NC	PWT	PWT
N3	NC	DP0	DP0
Q15	NC	BREQ	BREQ
Q16	NC	PLOCK#	PLOCK#
Q17	NC	PCHK#	PCHK#
R16	NC	BLAST#	BLAST#
R17	PEREQ	NC	NC
S4	BUSY#	NC	NC

5.7 Chipset Support

A list of chipset vendors providing solutions that support both the 386 and 486 interfaces has been compiled from information received from the specified chipset vendors (see Listing 2 on page 14 and Listing 3 on page 16). This is a partial list and is not meant to be all inclusive.

Listing 1. Voltage Regulator Support for TI486SXL(C)2-G†

Vendor	Regulator	Supply Current	Voltage Input	Voltage Output	Technology	Usage
AT&T	—	5A	5 V	3.3 V or Adj.	Switching	TI486SXL2-G50 up to DX4-100
Linear Tech.	LT1086	1.5A	5 V	3.3 V ± 2% or Adj.	Linear	TI486SXL2-G50 up to DX4-100
Linear Tech.	LT1085	3A	5 V	3.3 V ± 2% or Adj.	Linear	TI486SXL2-G50 up to DX4-100
Linear Tech.	LT1084	5A	5 V	3.3 V ± 2% or Adj.	Linear	TI486SXL2-G50 up to DX4-100
Linear Tech.	LT1083	7.5A	5 V	3.3 V ± 2% or Adj.	Linear	TI486SXL2-G50 up to DX4-100
Maxim	MAX471	3A	5 V	3.3 V or Adj.	Switching	TI486SXL2-G50 up to DX4-100
Maxim	MAX474	2.5A	5 V	3.3 V or Adj.	Switching	TI486SXL2-G50 up to DX4-100
National	LP2952	3A	5 V	3.3 V or Adj.	Linear	TI486SXL2-G50 up to DX4-100
Semtech	E5Z3	1A	5 V	3.3 V ± 2% or Adj.	Switching	TI486SXL2-G50 up to DX4-100
Semtech	LT1086	1.5A	5 V	3.3 V ± 2% or Adj.	Linear	TI486SXL2-G50 up to DX4-100
Semtech	LT1085	3A	5 V	3.3 V ± 2% or Adj.	Linear	TI486SXL2-G50 up to DX4-100
Semtech	LT1084	5A	5 V	3.3 V ± 2% or Adj.	Linear	TI486SXL2-G50 up to DX4-100
Semtech	LT1083	7.5A	5 V	3.3 V ± 2% or Adj.	Linear	TI486SXL2-G50 up to DX4-100
TI	TL5001	750mA	5 V	3.3 V ± 5% or Adj.	Switching	TI486SXL2-G50

† This voltage regulator information was received from the specified vendors. The responsibility for verifying designs incorporating the TI486 rests with the customer originating the design.

Listing 2. 486SXL/SXLC and 486DLC/SLC Notebook Chipset Support Summary†

Vendor (Part Name)	Part Number	PMU Chip	No. of Chips Without PMU	Package	CPU Support	Maximum Bus Freq./Voltage	SMI	Local Bus	L2 Cache	Production
Acc Micro	2036, 2036LV	2026	3	208 + RTC + Combo	486SXLC, SLC	25 MHz/3.3 V	No	NA	No	Yes
Acc Micro	2046, 2046LV 2046nt/ntLV 2046st/stLV	2026 2026 2026	3	208 + RTC + Combo	486SXL, DLC, 486SX/DX	33 MHz/3.3 V 40 MHz/5 V	No	VL‡	WT/DM – 2046 WB/DM – nt WB/DM – st	Yes
Acc Micro	2168, 2168LV 2168dt/dtLV 2168gt/gtLV	NA 2026 2026	3	208 + RTC + Combo	486SXL, DLC, 486SX/DX	33 MHz/3.3 V 40 MHz/5 V	Yes	VL	WT/DM – 2168 WB/DM – dt WB/DM – gt	Yes
Acc Micro	2086	Built-in	2	256 + RTC	486SXL, DLC, 486SX/DX	33 MHz/3.3 V 40 MHz/5 V	Yes	NA	WB	Yes
Acc Micro	2066	Built-in	1	208 + RTC + Combo	486SXL, DLC	33 MHz/	Yes	VL	WB/DM	Yes
ACER	M1709	Built-in			486SXL, DLC	33 MHz/5 V, 33 MHz/3.3 V	Yes	VL	No	Sampling
ETEQ (CUB™)	ET8000	Built-in	3	208 + 84 (#206) + Combo	486SXL, DLC, 486SX/DX	50 MHz/5 V	Yes	VL	WB/DM	Yes
Headland	HT25	Built-in	3	208 + RTC + Combo	486SXLC, SLC	25 MHz/5 V	Yes	NA	No	Yes
OAK (OakNote™)	OTI040	Built-in	3	160 + 144 + Combo	486SXLC, SLC	25 MHz/3.3 V 33 MHz/5 V	No	NA	No	Yes
OAK (OakNote)	OTI060	NA	3	160+84 (#206)	486SXL, DLC, 486SX/DX	50 MHz/5 V	No	NA	Yes	Yes
OPTI (SCNB™)	82C463MV/ 82C465MV	Built-in	3	208 + RTC + Combo	486SXL, DLC, 486SX/DX	33 MHz/3.3 V, 33 MHz/5 V	Yes	NA	No	Yes
PicoPower (Evergreen™)	PT86C168	Built-in	3	208 + 84 (#206) + Combo	486SXL, DLC, 486SX/DX	33 MHz/3.3 V 33 MHz/5 V	No	VL	No	Yes
PicoPower (Evergreen HV™)	PT86C268	Built-in	3	208 + 84 (#206) + Combo	486SXL, DLC, 486SX/DX	33 MHz/3.3 V 33 MHz/5 V	Yes	VL	No	Yes

† This chipset information was received from the specified vendors. The responsibility for verifying designs incorporating the TI486 rests with the customer originating the design.
‡ nt and st only

Listing 2. 486SXL/SXLC and 486DLC/SLC Notebook Chipset Support Summary† (Continued)

Vendor (Part Name)	Part Number	PMU Chip	No. of Chips Without PMU	Package	CPU Support	Maximum Bus Freq./Voltage	SMI	Local Bus	L2 Cache	Production
PicoPower (Pine™)	PT86C368	Built-in	3	208 + 84 (#206) + Combo	486SXL, DLC, 486SX/DX	33 MHz/3.3 V 33 MHz/5 V	Yes	VL	No	Yes
Picopower (Redwood™)		Built-in	2	160 *2 + Combo	486SXL, DLC	40 MHz/3.3 V 40 MHz/5 V	Yes	VL	WB/DM	Yes
Picopower (Cedar™)		Built-in	2	208 *1+ 84*1 + Combo	486SXLC, SLC, 486SXL,SXLC	33 MHz/3.3 V 33 MHz/5 V	Yes	VL	No	Sampling
Samsung	82C388	–	2	208	486SXLC, SLC	33 MHz/5 V	No	VL	WT/DM	Yes
TIDALWAVE	8100A	Built-in	2 (Integrated PCMCIA & CGA/ LCD)	240 + RTC	486SXLC, SLC	33 MHz/5 V, 25 MHz/3 V	Yes	NA	No	Yes
UMC	UM8486	Built-in	3	208 + 100 + Combo	486SXL, DLC	33 MHz/5 V, 33 MHz/3 V	Yes	VL	WB/DM	Yes
WD	7855/7855LV	Built-in	3	160 + 84 + 84	486SXLC, SLC	25 MHz/3.3 V 33 MHz/5 V	Yes	NA	No	Yes
WD (Magnum™)	8110/8110LV	Built-in	4	208 + 144 + 84 + 84	486SXL,SXLC 486SLC/DLC, 486SX/DX	25 MHz/3.3 V 40 MHz/5 V	Yes	VL	No	Yes

† This chipset information was received from the specified vendors. The responsibility for verifying designs incorporating the TI486 rests with the customer originating the design.

Listing 3. 486SXL/SXLC and 486DLC/SLC Desktop Chipset Support Summary†

Vendor (Part Name)	Part Number	PMU Chip	No. of Chips Without PMU	Package	CPU Support	Maximum Bus Freq/Voltage	SMI	Local Bus	L2 Cache	Production
Acc Micro	2046, 2046LV 2046nt/ntLV 2046st/stLV	2026 2026 2026	3	208 + RTC + Combo	486SXL, DLC, 486SX/DX	33 MHz/3.3 V 40 MHz/5 V	No	VL	WT/DM – 2046 WB/DM – nt WB/DM – st	Yes
Acc Micro	2168, 2168LV 2168dt/dtLV 2168gt/gtLV	NA 2026 2026	3	208 + RTC + Combo	486SXL, DLC, 486SX/DX	40 MHz/5 V- SXL	Yes	VL	WT/DM – 2168 WB/DM – dt WB/DM – gt	Yes
Acc Micro	2178	Built-in	2	208 + RTC	486SXL, DLC, 486SX/DX	40 MHz	Yes	No	WB	Yes
Acc Micro	2066	Built-in	1	208 + RTC	486SXL, DLC	33 MHz	Yes	VL	WB/DM	Yes
ACER	1217B	NA	1	208	486SXLC, SLC	40 MHz	No	No	NA	Yes
ACER	1419/1241	NA	4	208 +100 + RTC+Combo	486SXL, DLC, 486SX./DX	40 MHz/5 V	No	VL	WB/DM	Yes
ACER	1429G/1431	Built-in	4	208 +100 + RTC+Combo	486SXL, DLC, 486SX/DX, P24T	40 MHz/5 V	Yes	VL/ PCI	WB/DM	Yes
ACER	1439G	Built-in			486SXL	40 MHz/5 V	Yes	VL/ PCI	WB/DM	Yes
EFAR	EC798	NA	2	208 + 84 + Combo	486SXL, 486DLC	40 MHz/5 V	No	VL	WB/DM	Yes
EFAR	EC802G	Built-in	2	208 + 84 + Combo	486SXL,SXLC 486DLC.SLC	40 MHz/5 V	Yes	VL	WB/DM	Yes
ETEQ (CUB)	ET8000	Built-in	3	208 +84 + Combo	486SXL, DLC, 486SX/DX	40 MHz/5 V	Yes	VL	WB/DM	Yes
ETEQ (PANDA™)	82C390SX	ET5000	3	184 + 84 (#206) + Combo	486SXLC, SLC	33 MHz/5 V	No	VL	WT/DM	Yes
ETEQ (BUFFALO™)	ET9000	ET5000	3	184 + 84 (#206) + Combo	486SXL, DLC, 486SX/DX	40 MHz/5 V	No	VL	WB/DM	Yes
ETEQ (MUSTANG™)	ET9600	ET5000	3	160 + 84(#206) + Combo	486SXL, DLC, 486SX/DX	40 MHz/5 V	No	VL	WB/DM	Yes
ETEQ (FIREFOX™)	ET9800	ET5000	3	160 + 84 (#206) + Combo	486SXLC, SLC	40 MHz/5 V	No	VL	WB/DM	Yes
FTD	823480	Built-in	4	160 + 160 + RTC + Combo	486SXL, 486DLC	40 MHz/5 V	No	VL	WB/WT	Yes

† This chipset information was received from the specified vendors. The responsibility for verifying designs incorporating the TI486 rests with the customer originating the design.

Listing 3. 486SXL/SXLC and 486DLC/SLC Desktop Chipset Support Summary† (Continued)

Vendor (Part Name)	Part Number	PMU Chip	No. of Chips Without PMU	Package	CPU Support	Maximum Bus Freq./Voltage	SMI	Local Bus	L2 Cache	Production
Forex	521B	Built-in	2		486SXL, DLC 486SX, DX	40 MHz/5 V	Yes	PCI	WB/DM	Yes
Macronix	MX83C305/306				486SXL, DLC	40 MHz/5 V		No	WB/DM	Yes
OPTI (WBSLC™)	82C295	NA			486SXLC, SLC	33 MHz/5 V	No	No	WB/DM	Yes
OPTI (LCWB™)	82C495SX/XLC	NA	4	160 + 100 + 84 (#206) + Combo	486SXL, DLC, 486SX/DX	40 MHz/5 V	No	No	WB/DM	Yes
OPTI (DXSC™)	82C499	NA	3	208 + RTC + Combo	486SXL, DLC, 486SX/DX	40 MHz/5 V	No	No	WB/DM	Yes
PCCHIP	18/16				486SXL, DLC	40 MHz/5 V		VL		Yes
PCCHIP	13/11				486SXL, DLC	40 MHz/5 V		No		Yes
Picopower (Redwood)	PT668/618	Built-in	2	160 *2	486SXL, DLC	40 MHz/3.3 V 40 MHz/5 V	Yes	VL	WB/DM	Yes
SAMSUNG	KS82C388				486SXL, DLC	40 MHz/5 V		No		
SARC	RC2016A5				486SXL, DLC	40 MHz/5 V				
SIS	85C460	NA	3	208 + RTC + Combo	486SXL, DLC, 486SX/DX	40 MHz/5 V	No	No	WB/DM	Yes
SIS	85C461	NA	3	208 + RTC + Combo	486SXL, DLC, 486SX/DX	40 MHz/5 V	No	VL	WB/DM	Yes
SIS	85C471	Built-in						VL	WB/DM	Yes
SYMPHONY (HAYDN™)	C460	NA	5	160 +160 + 100 + RTC + Combo	486SXL, SXLC 486DLC/SLC 486SX/DX	40 MHz/5 V	No	VL	WB/DM	Yes
UMC	481/482	NA	3	160 *2 + RTC	486SXL, DLC	40 MHz/5 V	No	No	WT	Yes
UMC	498	NA	2	208 + 84	486SXL, DLC	40 MHz/5 V	Yes	VL	WB/DM	Yes
UMC	491/493/495	NA	4	208 + 100 +100 + Combo	486SXL, DLC, 486SX/DX	40 MHz/5 V	No	VL	WB/DM	Yes
UNI CHIP	U6000	Built-in	2	160 + #206 + Combo	486SXL, DLC	40 MHz/5 V	Yes	PCI/ VL	WB/DM	1Q/95
UNI CHIP	4900G	Built-in	2	208 + 84 + Combo	486SXL, DLC	40 MHz/5 V	Yes	VL	WB/DM	Yes
VIA	82C470				486SXL, DLC	40 MHz/5 V		No	WB/DM	Yes
VIA	82C486A				486SXL, DLC	40 MHz/5 V		VL	WB/DM	Yes
VIA	82C496G	Built-in			486SXL, DLC	40 MHz/5 V		VL/ PCI	WB/DM	Yes

† This chipset information was received from the specified vendors. The responsibility for verifying designs incorporating the TI486 rests with the customer originating the design.

6 Microprocessors Offered

Table 7 lists the family of TI486SXL(C) microprocessors currently offered. The table also provides the minimum, nominal, and maximum recommended supply voltages, including the V_{CC5} terminal supply voltage range. Also shown are CLK2 input frequency requirements, maximum case temperature, and package availability.

Table 7. TI486SXL(C) Supply Voltage, Input Frequency, Case Temperature, and Package

Device Part Number	Supply Voltage, V_{CC} (V) (V_{CC5}†) (V)			CLK2 Input Frequency (MHz)	Maximum Case Temperature (°C)	Package
	Min	Nom	Max			
TX486SXLC-V25-PJF	3	3.3	3.6	50	85	100-pin TEP§ QFP
TX486SXLC-040-PJF	4.75	5	5.25	80‡	100	
TX486SXLC2-G50-WN	3 (3)	3.3	3.7 (5.25)	50	85	100-pin ceramic QFP
TI486SXLC2-G66-WN¶	3.5 (3.5)	3.6	3.7 (5.25)	66	65	
TX486SXL-040S-GA	4.75	5	5.25	80‡	85	132-pin CPGA
TX486SXL2-050S-GA	4.75	5	5.25	50	85	
TX486SXL-040-PCE	4.75	5	5.25	80‡	100	144-pin TEP QFP
TX486SXL2-G50-HBN	3 (3)	3.3	3.7 (5.25)	50	85	144-pin ceramic QFP
TX486SXL2-G66-HBN¶	3.5 (3.5)	3.6	3.7 (5.25)	66	65	
TX486SXL2-G50-GA	3 (3)	3.3	3.7 (5.25)	50	85	168-pin CPGA
TX486SXL2-G66-GA	3.5 (3.5)	3.6	3.7 (5.25)	66	65	
TX486SXL-040-GA	4.75	5	5.25	80‡	85	
TX486SXL2-050-GA	4.75	5	5.25	25	85	

† V_{CC5} applies to the -G50 and -G66 devices in the 100-pin, 144-pin, and 168-pin packages. The minimum and maximum range for V_{CC5} is shown in parenthesis beneath the V_{CC} minimum and maximum, respectively.

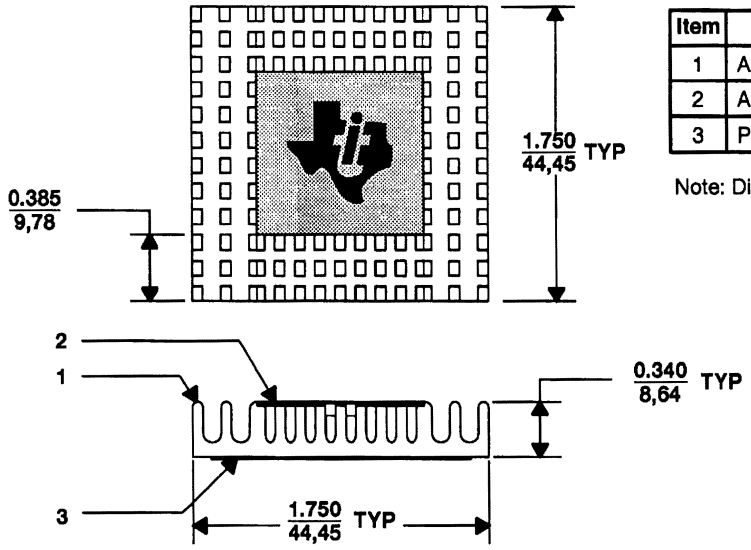
‡ These microprocessors can be operated as nonclock-doubled 40 MHz (CLK2 = 80 MHz) or clock-doubled 20/40 MHz (CLK2 = 40 MHz).

§ Thermally enhanced package

¶ These microprocessors are not released to a production status.

A heat sink fin, illustrated in Figure 5, is attached to each TI486SXL(C)-G66 microprocessor that is supplied in the 168-pin PGA. The heat sink fin is required to meet operation within the recommended case temperature range.

Figure 5. Heat Sink Fin for the 168-Pin CPGA



Item	Material
1	Aluminum Alloy
2	Aluminum Alloy
3	Pressure Sensitive Adhesive

Note: Dimensions are in $\frac{\text{in.}}{\text{mm}}$.

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