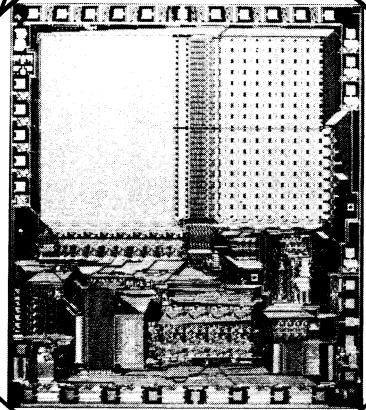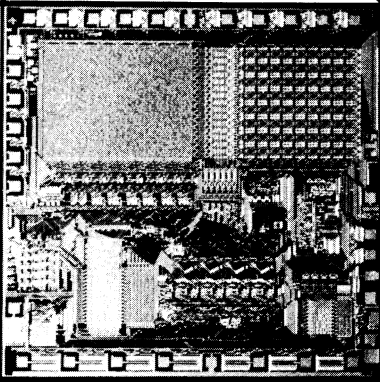The Engineering Staff of
TEXAS INSTRUMENTS INCORPORATED
Semiconductor Group

TMS 1000 Series
Data Manual

MOS/LSI One-Chip
Microcomputers

FEBRUARY 1976

TEXAS INSTRUMENTS
INCORPORATED

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1. THE ONE-CHIP MICROCOMPUTERS FROM TEXAS INSTRUMENTS

1.1 DESCRIPTION

The TMS 1000 series is a family of P-channel MOS four-bit microcomputers with a ROM, a RAM, and an arithmetic logic unit on a single semiconductor chip. The TMS 1000 family is unique in the field of microprocessors because this device is a single-chip binary computer. A customer's specification determines the software that is reproduced during wafer processing by a single-level mask technique that defines a fixed ROM pattern. As summarized in Table 1, the TMS 1000 and TMS 1200 are the basic 1024-instruction ROM microcomputers. The TMS 1070 and TMS 1270 interface directly to high-voltage displays and use instructions identical to the TMS 1000/1200 devices. To increase the software capacity in one chip, the TMS 1100 and TMS 1300 provide twice the ROM and RAM size of the TMS 1000/1200.

The design support for the entire series includes software assembler and simulator, hardware simulator with debug control, and system evaluator devices for prototype fabrication.

TABLE 1
4-BIT MICROCOMPUTER FEATURES

	TMS 1000	TMS 1200	TMS 1070	TMS 1270	TMS 1100	TMS 1300
Package Pin Count	28 Pins	40 Pins	28 Pins	40 Pins	28 Pins	40 Pins
Instruction Read Only Memory	1024 X 8 Bits (8,192 Bits)		1024 X 8 Bits (8,192 Bits)		*2048 X 8 Bits (16,384 Bits)*	
Data Random Access Memory	64 X 4 Bits (256 Bits)		64 X 4 Bits (256 Bits)		*128 X 4 Bits (512 Bits)*	
"R" Individually Addressed Output Latches	11	13	11	13	11	*16*
"O" Parallel Latched Data Outputs	8 Bits		8 Bits	*10 Bits	8 Bits	
Maximum-Rated Voltage (O, R, and K)	20 V		*35 V*		20 V	
Working Registers	2-4 Bits Each		2-4 Bits Each		2-4 Bits Each	
Instruction Set	See Table 2, Page 9		See Table 2, Page 9		See Table 3, Page 15	
Programmable Instruction Decoder	Yes		Yes		Yes	
On-Chip Oscillator	Yes		Yes		Yes	
Power Supply/Typical Dissipation	15 V/90 mW		15 V/90 mW		15 V/105 mW	
Time-Share Assembler Support	Yes		Yes		Yes	
Time-Share Simulator Support	Yes		Yes		Yes	
Hardware Evaluator and Debugging Unit	HE-2		HE-2		HE-2	
System Evaluator Device with External Instruction Memory	SE-1 (TMS 1099 JL)		SE-1 (TMS 1099 JL)		SE-2 (TMS 1098 JL)	

*The HE-2 does not have a decoder for the extra O outputs.

1.2 DESIGN SUPPORT

Through a staff of experienced application programmers, Texas Instruments will, upon request, assist customers in evaluating applications, in training designers to program the TMS 1000 series, and in simulating programs. TI will also contract to write programs to customer's specifications.

TI developed assemblers and simulators for aiding software designs. These assembler and simulator programs are available on nationwide time-sharing systems and at TI computer facilities.

A TMS 1000 series program (see flowchart, Figure 1) is written in assembly language using standard mnemonics. The assembler converts the source code (assembly language program) into machine code, which is transferred to a software simulation program. Also, the assembler produces a machine code object deck. The object deck is used to produce a tape for hardware simulation or a tape for generating prototype tooling.

The TMS 1000 series programs are checked by software and hardware simulation. The software simulation offers the advantages of printed outputs for instruction traces or periodic outputs. The hardware simulation offers the designer the advantages of real-time simulation and testing asynchronous inputs.

After the algorithms have been checked and approved by the customer, the final object code and machine option statements are supplied to TI. A gate mask is generated and slices produced. After assembly and testing, the prototypes are shipped to the customer for approval. Upon receiving final approval, the part is released for volume production at the required rate as one unique version of the TMS 1000 family.
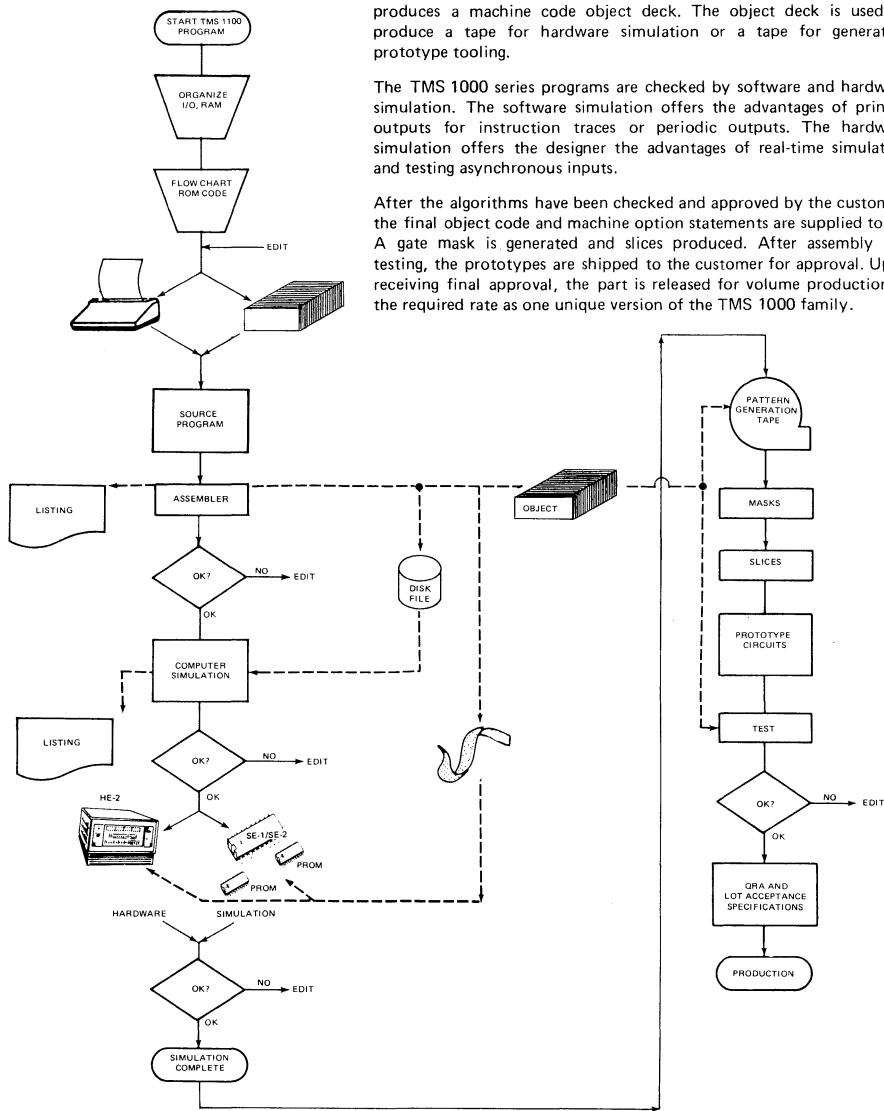
FIGURE 1 — TMS 1000 SERIES ALGORITHM DEVELOPMENT

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1.3 APPLICATIONS

One major advantage of the TMS 1000 series is flexibility. The TMS 1000 series is effective in applications such as printer controllers, data terminals, remote sensing systems, cash registers, appliance controls, and automotive applications. A data terminal is a useful example. In Figure 2, a sample interconnect diagram shows how the R outputs control a universal asynchronous receiver/transmitter (UART), display scan, and keyboard scan. The ROM controls data output to the appropriate display digit or to the transmitter section of the UART. A routine in the ROM program controls selection of incoming data through the K-input ports. Two dedicated R outputs (load and ready reset) control the UART's transmit and receive modes. The remaining R outputs both scan the display and select inputs. The SN74157 TTL devices multiplex eight bits of the incoming data word, four bits of UART status, and the four key input lines. Through the TMS 1000 series' versatility, a wide range of systems realize reduced costs, fewer parts, and high reliability.
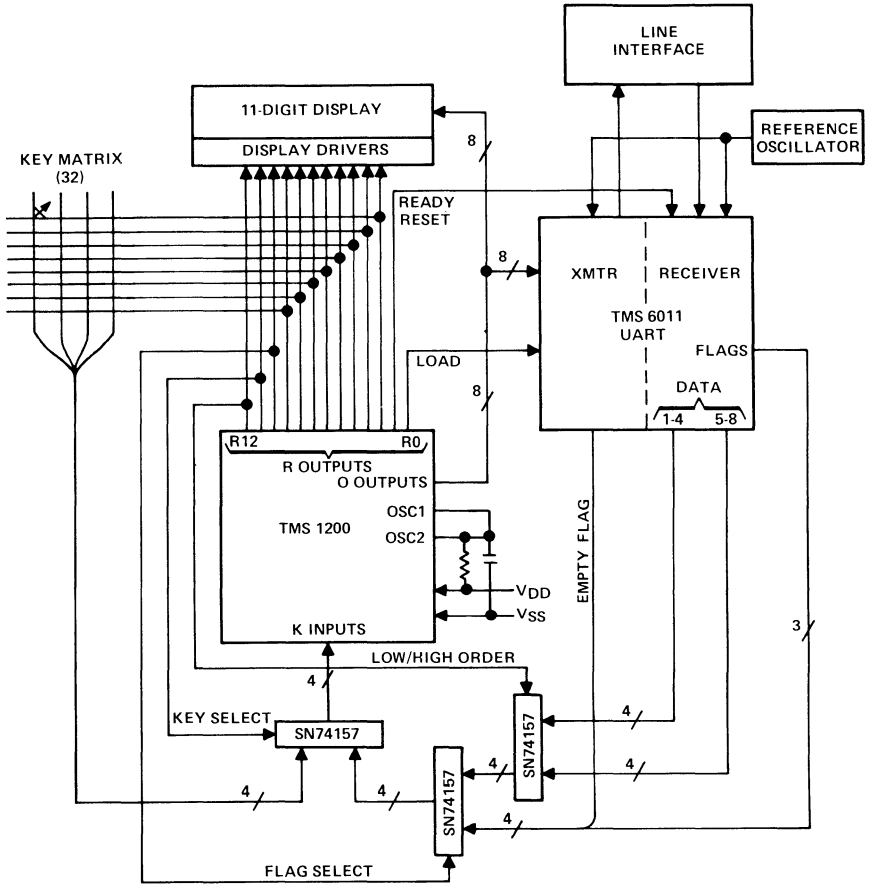
NOTE: Discrete components for level shifting and other functions are not shown.

FIGURE 2 — BLOCK DIAGRAM OF TYPICAL APPLICATION—TERMINAL CONTROLLER

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2. TMS 1000/1200 AND TMS 1070/1270 MICROCOMPUTERS

2.1 INTRODUCTION

The TMS 1000/1200 and TMS 1070/1270 are identical except for maximum voltage ratings for the K inputs and the O and R outputs, and the TMS 1270 has a total of ten O outputs. See Section 5 for a TMS 1070/1270 description.

The microcomputer's ROM program controls data input, storage, processing, and output. Data processing takes place in the arithmetic logic unit. K input data goes into the ALU, as shown in Figure 3, and is stored in the four-bit accumulator. The accumulator output accesses the output latches, the RAM storage cells, and the adder input. Data storage in the 256-bit RAM is organized into 64 words, four bits per word. The four-bit words are conveniently grouped into four 16-word files addressed by a two-bit register. A four-bit register addresses one of the 16 words in a file by ROM control.

The O outputs and the R outputs are the output channels. The eight parallel O outputs are decoded from five data latches. The O outputs serve many applications because the decoder is a programmable logic array (PLA) that is modified by changing the gate-level mask tooling. Each of the thirteen R outputs of the TMS 1200 and the eleven R outputs on the TMS 1000 has an individual storage element that can be set or reset by program control. The R outputs send status or enable signals to external devices. The R outputs strobe the O outputs to displays, to other TMS 1000 series chips, or to TTL and other interface circuits. The same R outputs multiplex data into the K inputs whenever necessary.

There are 43 basic instructions that handle I/O, constant data from the ROM, bit control, internal data transfer, arithmetic processing, branching, looping, and subroutines. The eight-bit instruction word performs 256 unique operations for maximum efficiency. Section 2.9 defines the standard instruction set, which is optimized for most programs. Microprogramming for special applications is possible, and the operations of the instruction set can be modified by the same mask-tooling step that programs the ROM and the O output PLA.
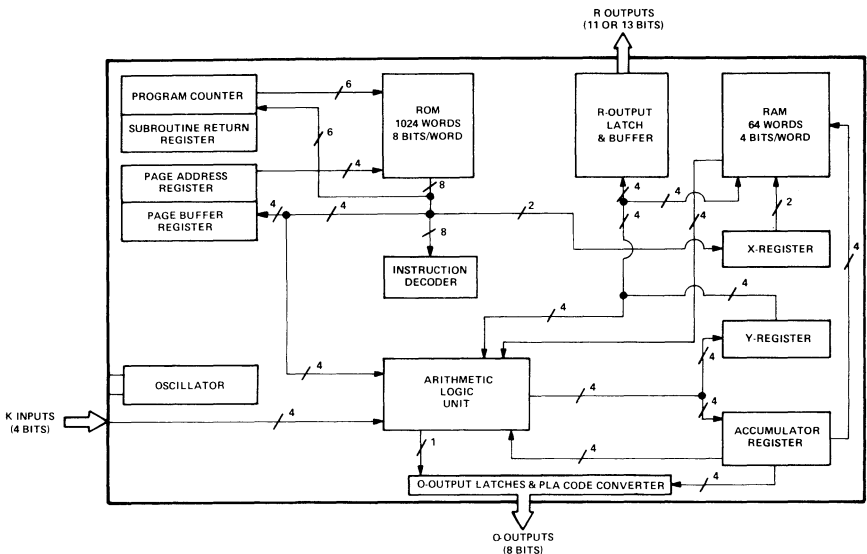
FIGURE 3 — TMS 1000/1200 LOGIC BLOCKS

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2.2 ROM OPERATION

The sequence of the 1024 eight-bit ROM instructions determines the device operation. There are 16 pages of instructions with 64 instructions on each page. After power-up the program execution starts at a fixed instruction address. Then a shift-register program counter sequentially addresses each ROM instruction on a page. A conditional branch or call subroutine instruction may alter the six-bit program-counter address to transfer software control. One level of subroutine return address is stored in the subroutine return register. The page address register (four bits) holds the current address for one of the 16 ROM pages. To change pages, a constant from the ROM loads into the page buffer register (four bits), and upon a successful branch or call, the page buffer loads into the page address register. The page buffer register also holds the return page address in the call subroutine mode.

2.3 RAM OPERATION

There are 256 addressable bits of RAM storage available. The RAM is comprised of four files, each file containing 16 four-bit words. The RAM is addressed by the Y register and the X register. The Y register selects one of the 16 words in a file and is completely controllable by the arithmetic unit. The TMS 1000 series has instructions that: Compare Y to a constant, set Y to a constant, increment or decrement Y, and/or perform data transfer to or from Y. Two bits in the X register select one of the four 16-word files. The X register is set to a constant or is complemented. A four-bit data word goes to the RAM location addressed by X and Y from the accumulator or from the constants in the ROM. The RAM output words go to the arithmetic unit and can be operated on and loaded into Y or the accumulator in one instruction interval. Any selected bit in the RAM can be set, reset, or tested.

2.4 ARITHMETIC LOGIC UNIT OPERATION

Arithmetic and logic operations are performed by the four-bit adder and associated logic. The arithmetic unit performs logical comparison, arithmetic comparison, add, and subtract functions. The arithmetic unit and interconnects are shown in Figure 4. The operations are performed on two sets of inputs, P and N. The two four-bit parallel inputs may be added together or logically compared. The accumulator has an inverted output to the N selector for subtraction by two's complement arithmetic. The other N inputs are from the true output of the accumulator, the RAM, constants, and the K inputs. The P inputs come from the Y register, the RAM, the constants, and the K inputs.

Addition and subtraction results are stored in either the Y register or the accumulator. An arithmetic function may cause a carry output to the status logic. Logical comparison may generate an output to status. If the comparison functions are used, only the status bit affects the program control, and neither the Y register's nor the accumulator register's contents are affected. If the status feedback is a logic one, which is the normal state, then the conditional branch or call is executed successfully. If an instruction calls for a carry output to status and the carry does not occur,
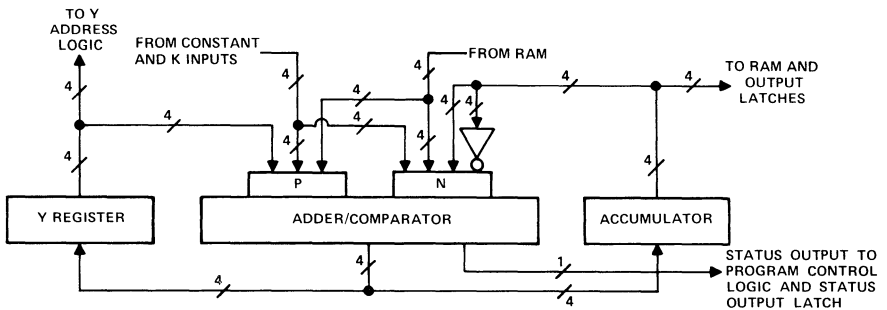
FIGURE 4 — ALU AND ASSOCIATED DATA PATHS

then status will go to a zero state for one instruction cycle. Likewise, if an instruction calls for the logical-comparison function and the bits compared are all equal, then status will go to a zero state for one instruction cycle. If status is a logic zero, then branches and calls are not performed successfully.

2.5 INPUT

There are four data inputs to the TMS 1000-series circuit, K1, K2, K4, and K8. Each time an input word is requested, the data path from the K inputs is enabled to the adder. The inputs are either tested for a high level ($\approx V_{SS}$), or the input data are stored in the accumulator for further use. The R outputs usually multiplex inputs such as keys and other data. Other input interfaces are possible. An external device that sends data out to the K-input bus at a fixed rate may be used with the TMS 1000 series when an initiating "handshake" signal is given from an R output. Data from the K inputs is stored periodically in synchronization with the predetermined data rate of the external device. Thus, multiple four-bit words can be requested and stored with only one R output supplying the control signal.

2.6 OUTPUT

There are two output channels with multiple purposes, the R outputs and the O outputs. Thirteen latches store the R output data. The eight parallel O outputs come from a five-bit-to-eight-bit code converter, which is the O-output PLA. The R outputs are individually addressed by the Y register. Each addressed bit can be set or reset.

The R outputs are normally used to multiplex inputs and strobe O output data to displays, external memories, and other devices. Also, one R output can strobe other R outputs that represent variable data, because every R output may be set or reset individually. For example, the Y register addresses each latch in turn; the variable data R outputs are set or reset; and finally, the data strobe R latch is set.

The eight O outputs usually send out display or binary data that are encoded from the O output latches. The O latches contain five bits. Four bits load from the accumulator in parallel. The fifth bit comes from the status latch, which is selectively loaded from the adder output (see Figure 4). The load output command sends the status latch and accumulator information into the five output latches. The five bits are available in true or complementary form to 20 programmable-input NAND gates in the O output PLA. Each NAND gate can simultaneously select any combination of O0 through O7 as an output. The user defines this PLA's decoding to suit an optimum output configuration. As an illustration, the O output PLA can encode any 16 characters of eight-segment display information and additionally can transfer out a four-bit word of binary data.

2.7 THE INSTRUCTION PROGRAMMABLE LOGIC ARRAY

The programmable instruction decode is defined by the instruction PLA. Thirty programmable-input NAND gates decode the eight bits of instruction word. Each NAND gate output selects a combination of 16 microinstructions. The 16 microinstructions control the arithmetic unit, status logic, status latch, and write inputs to the RAM.

As an example, the "add eight to the accumulator, results to accumulator" instruction can be modified to perform a "add eight to the Y register, result to Y" instruction. Modifications that take away an instruction that is not used very often are desirable if the modified instructions save ROM words by increasing the efficiency of the instruction repertoire. A programmer's reference manual is available to explain PLA programming and the TMS 1000-series operation in detail.

2.8 TIMING RELATIONSHIPS

Six oscillator pulses constitute one instruction cycle. All instructions are executed in one instruction cycle. The actual machine cycle period is determined by either a fixed external resistor and capacitor connected to the OSC1 and OSC2 pins (refer to Section 4), or an external clock input frequency.

2.9 SOFTWARE SUMMARY

Table 2 defines the TMS 1000/1200 and TMS 1070/1270 standard instruction set with a description, mnemonic, and status effect. The mnemonics were defined for easy reference to the functional description. Eighteen mnemonics use an identifier to indicate the condition that satisfies the status requirement for a successful branch or call if the instruction is followed immediately by a branch or call command. "C" means that if the instruction generates a carry (status = one), then a following branch or call is executed. If a branch instruction does not follow or if there is no carry (status = zero), then the program counter proceeds to the next address without changing the normal counting sequence. "N" means that if no borrow (equal to a carry in two's complement arithmetic) is generated, an ensuing branch or call is taken. "Z" indicates that if the two's complement of zero in the accumulator (instruction CPAIZ) is attempted with a branch or call following, then the branch or call is taken. "1", "LE", "NE", and "NEZ" are used to indicate conditions for branch and call for seven test instructions. The test instructions do not modify data at all; tests are used solely in conjunction with subsequent branches or calls.

If an instruction that does not affect status is placed between an instruction that does affect status and a branch or call instruction, then the branch or call is always successful. This is true because status always returns to its normal state (status = one) after one instruction cycle, and branches and calls are taken if status equals one.

TABLE 2

TMS 1000/1200 AND TMS 1070/1270 STANDARD INSTRUCTION SET

FUNCTION	MNEMONIC	STATUS EFFECTS C	N	DESCRIPTION
Register to	TAY			Transfer accumulator to Y register.
Register	TYA			Transfer Y register to accumulator.
	CLA			Clear accumulator.
Transfer	TAM			Transfer accumulator to memory.
Register to	TAMIY			Transfer accumulator to memory and increment Y register.
Memory	TAMZA			Transfer accumulator to memory and zero accumulator.
Memory to	TMY			Transfer memory to Y register.
Register	TMA			Transfer memory to accumulator.
	XMA			Exchange memory and accumulator.
Arithmetic	AMAAC	Y		Add memory to accumulator, results to accumulator. If carry, one to status.
	SAMAN	Y		Subtract accumulator from memory, results to accumulator. If no borrow, one to status.
	IMAC	Y		Increment memory and load into accumulator. If carry, one to status.
	DMAN	Y		Decrement memory and load into accumulator. If no borrow, one to status.
	IA			Increment accumulator, no status effect.
	IYC	Y		Increment Y register. If carry, one to status.
	DAN	Y		Decrement accumulator. If no borrow, one to status.
	DYN	Y		Decrement Y register. If no borrow, one to status.
	A8AAC	Y		Add 8 to accumulator, results to accumulator. If carry, one to status.
	A10AAC	Y		Add 10 to accumulator, results to accumulator. If carry, one to status.
	A6AAC	Y		Add 6 to accumulator, results to accumulator. If carry, one to status.
	CPAIZ	Y		Complement accumulator and increment. If then zero, one to status.
Arithmetic	ALEM	Y		If accumulator less than or equal to memory, one to status.
Compare	ALEC	Y		If accumulator less than or equal to a constant, one to status.
Logical	MNEZ		Y	If memory not equal to zero, one to status.
Compare	YNEA		Y	If Y register not equal to accumulator, one to status and status latch.
	YNEC		Y	If Y register not equal to a constant, one to status.

— CONTINUED —

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TABLE 2

TMS 1000/1200 AND TMS 1070/1270 STANDARD INSTRUCTION SET (Continued)

FUNCTION	MNEMONIC	STATUS EFFECTS		DESCRIPTION
		C	N	
Bits in	SBIT			Set memory bit.
Memory	RBIT			Reset memory bit.
	TBIT1		Y	Test memory bit. If equal to one, one to status.
Constants	TCY			Transfer constant to Y register.
	TCMIY			Transfer constant to memory and increment Y.
Input	KNEZ		Y	If K inputs not equal to zero, one to status.
	TKA			Transfer K inputs to accumulator.
Output	SETR			Set R output addressed by Y.
	RSTR			Reset R output addressed by Y.
	TDO			Transfer data from accumulator and status latch to O outputs.
	CLO			Clear O-output register.
RAM 'X'	LDX			Load 'X' with a constant.
Addressing	COMX			Complement 'X'.
ROM	BR			Branch on status = one.
Addressing	CALL			Call subroutine on status = one.
	RETN			Return from subroutine.
	LDP			Load page buffer with constant.

NOTES: C-Y (Yes) means that if there is a carry out of the MSB, status output goes to the one state. If no carry is generated, status output goes to the zero state.

N-Y (Yes) means that if the bits compared are not equal, status output goes to the one state. If the bits are equal, status output goes to the zero state.

A zero in status remains through the next instruction cycle only. If the next instruction is a branch or call and status is a zero, then the branch or call is not executed successfully.

2.10 SAMPLE PROGRAM

The following example shows register addition of up to fifteen BCD digits. The add routine (flow charted in Figure 5) can use the entire RAM, which is divided into two pairs of registers. The definition of registers, for the purpose of illustration, is expanded to include the concept of a variable-length word that is a subset of a 16-digit file. Addition proceeds from the least-significant digit (LSD) to the most-significant digit (MSD), and carry ripples through the accumulator. The decrement-Y instruction is used to index the numbers in a register. The initial Y value sets the address for the LSD's of two numbers to be added. Thus, if Y equals eight at the start, the LSD is defined to be stored in $M(X,8)$, $[M(X, Y) \equiv$ contents of RAM word location X equals 0, 1, 2, or 3, and Y equals 0 to 15]. If Y is eight initially, $M(X,7)$ is the next-most-significant digit.

RAM DATA MAP BEFORE EXECUTING SAMPLE ROUTINE

FILE ADDRESS	REGISTER	Y-REGISTER ADDRESS															
		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
X = 00	D	OV 0	MSD 9	8	7	6	5	4	3	LSD 2							
X = 01	E	OV 0	MSD 1	2	3	4	5	6	7	8	9	0	1	2	3	4	LSD 5
X = 10	F	OV 0	MSD 5	4	3	2	1	0	9	8	7	6	5	4	3	2	LSD 1
X = 11	G	OV 0	MSD 8	7	6	5	4	3	2	LSD 1							

OV ≡ overflow, MSD ≡ most-significant digit, and LSD ≡ least-significant digit

In the preceding RAM register assignment map, registers D and G are nine digits long, and registers E and F are 16 digits long. The sample routine calls the D plus G → D subroutine and the E plus F → E subroutine. After executing the two subroutines, the RAM contents are the following:

RAM DATA MAP AFTER EXECUTING SAMPLE ROUTINE

FILE ADDRESS	REGISTER	OV	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
			MSD								LSD							
X = 00	D	1	8	6	4	1	9	7	5	3	░	░	░	░	░	░	░
			MSD															LSD
X = 01	E	0	6	6	6	6	6	7	7	7	6	6	6	6	6	6	6	6
			MSD															LSD
X = 10	F	0	5	4	3	2	1	0	9	8	7	6	5	4	3	2		1
			MSD								LSD							
X = 11	G	0	8	7	6	5	4	3	2	1	░	░	░	░	░	░	░

NOTE: Shaded areas indicate locations in the RAM that are unaffected by executing the example routine.

LABEL	OPCODE	OPERAND	COMMENT
	TCY	8	Transfer 8 → Y
	CALL	ADGD	Add: D + G → D
	TCY	15	Transfer 15 → Y
	CALL	AEFE	Add: E + F → E
ADGG	LDX	3	3 → X; Set up for D + G → G.
	BR	BCDADD	Branch to BCD add.
AEFF	LDX	2	2 → X; Set up for E + F → F.
	BR	BCDADD	Branch to BCD add.
AEFE	LDX	1	1 → X; Set up for E + F → E.
	BR	BCDADD	Branch to BCD add.
ADGD	LDX	0	0 → X; Add D + G → D.
BCDADD	CLA		Clear accumulator (A).
LOOP	COMX		$\bar{X}$ → X.
	AMAAC		M(X,Y) + A → A; A contains possible carry if in loop.
	COMX		$\bar{X}$ → X.
	AMAAC		Add digits: M(X, Y) + [M($\bar{X}$,Y) + Carry] → A.
	BR	GT9	Branch if sum >15.
	ALEC	9	If A ⩽ 9, one to status.
	BR	LT10	Branch if sum < 10.
GT9	A6AAC		Sum > 9, A + 6 → A; BCD Correction.
	TAMZA		Transfer corrected sum to memory, 0 → A.
	IA		1 → A; to propagate carry
DECY	DYN		Y − 1 → Y; index next digit.
	BR	LOOP	If no borrow, continue.
	RETN		If borrow, return to instruction after call.
LT10	TAMZA		Sum < 9, A → M(X,Y); 0 →A; No carry propagated.
	BR	DECY	

Labels at left:
MAIN PROGRAM PRESETS Y, AND CALL SUBROUTINES
MULTIPLE ENTRY POINTS FOR SUBROUTINES
BASE SUBROUTINE CONTAINS LOOPING AND BCD CORRECTION

D + G→G

ADGG
3→X

E + F→F

AEFF
2→X

E + F→E

AEFE
1→X

D + G→D

ADGD
0→X

BCDADD
0→A

LOOP
X̄→X

M + A→A

X̄→X

M + A→A

SUM > 15

SUM ≤ 15

A ≤ 9

SUM ≤ 9

SUM > 9

GT9
A + 6→A

A→M

0→A

A + 1→A

DECY
Y − 1→Y

NO BORROW

BORROW

RETURN

LT10
A→M

0→A
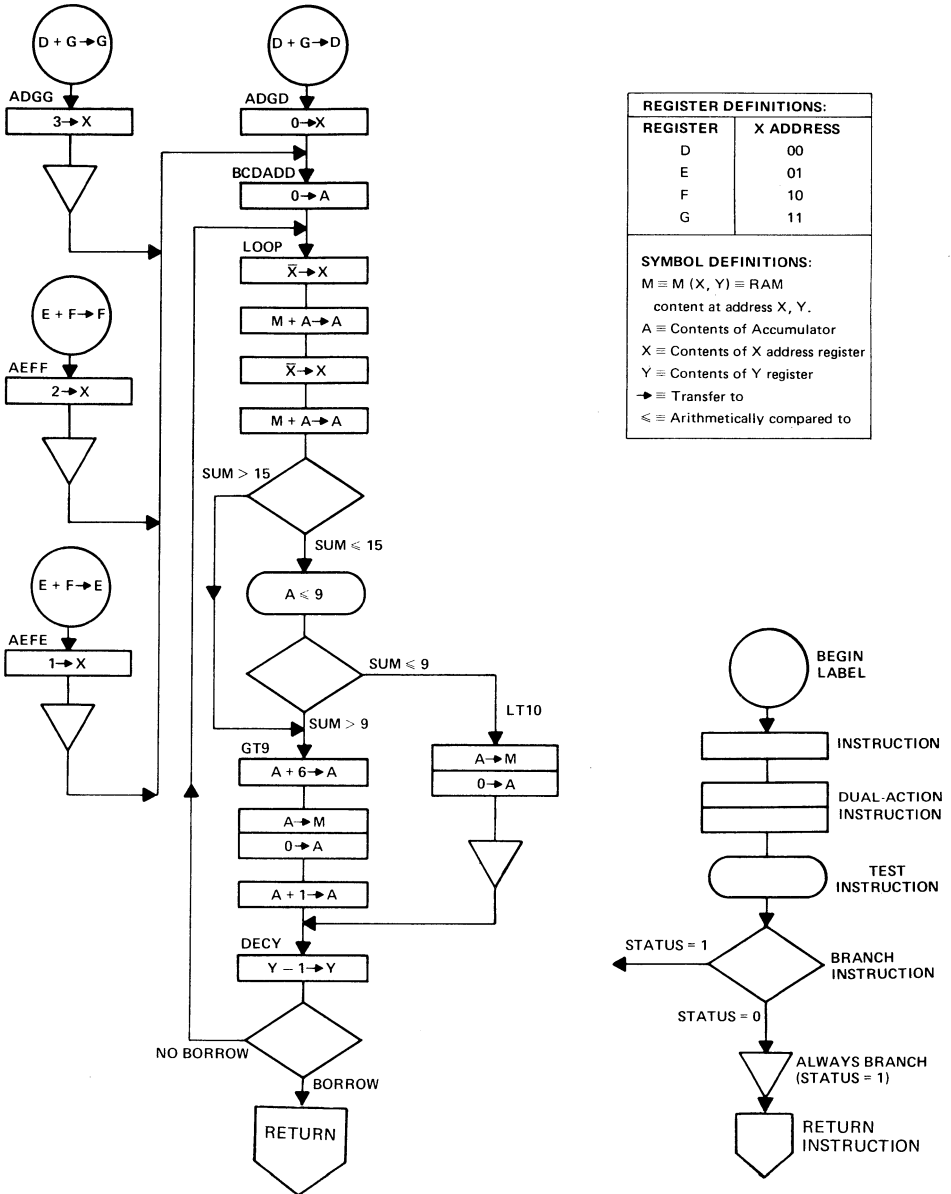
REGISTER DEFINITIONS:

REGISTER	X ADDRESS
D	00
E	01
F	10
G	11

SYMBOL DEFINITIONS:

M ≡ M (X, Y) ≡ RAM
content at address X, Y.
A ≡ Contents of Accumulator
X ≡ Contents of X address register
Y ≡ Contents of Y register
→ ≡ Transfer to
≤ ≡ Arithmetically compared to

BEGIN
LABEL

INSTRUCTION

DUAL-ACTION
INSTRUCTION

TEST
INSTRUCTION

STATUS = 1

BRANCH
INSTRUCTION

STATUS = 0

ALWAYS BRANCH
(STATUS = 1)

RETURN
INSTRUCTION
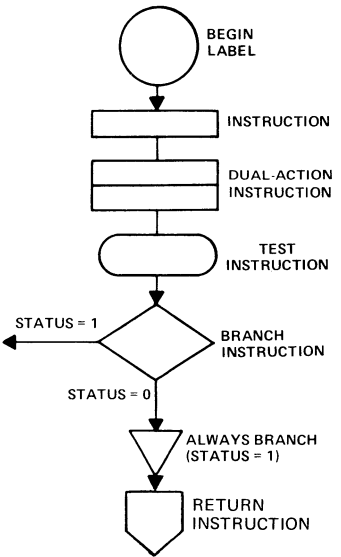
FIGURE 5 — MACHINE INSTRUCTION FLOWCHART–BCD-ADDITION SUBROUTINE

Note that there are four entry points to the base subroutine (ADGG, ADGD, AEFF, AEFE). The main program can call two of the other possible subroutines that store the addition results differently. These subroutines have applications in floating-point arithmetic, multiplication, division, and subtraction routines.

2.11 POWER-ON

The TMS 1000 series has a built-in power-on latch, which resets the program counter upon the proper application of power (with INIT input open or tied to V_{DD}). After power-up the chip resets and begins execution at a fixed ROM address. The system reset depends on the ROM program after the starting address. For power supplies with slow rise times or noisy conditions, the following network connected to the INIT pin may be necessary. To assist initialization of the TMS 1000 series devices, a capacitor maintains a high-level voltage on the INIT input after the power supply settles. The diode connecting V_{DD} to INIT is used to fully discharge C_{ext} and allow a proper reset when fast power-on-off-on cycles are expected.
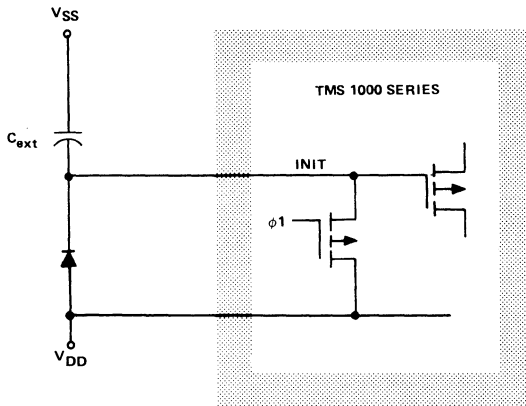
$C_{ext}(\mu F) = 0.06$ Power Supply Rise Time (ms)

1

3. TMS 1100 AND TMS 1300 MICROCOMPUTERS

3.1 INTRODUCTION

Texas Instruments increased the four-bit microprocessor capability with an expanded one-chip microcomputer containing all of the TMS 1000 features plus twice the ROM and RAM capacity. (See Figure 6.) Two versions of the expanded memory device are available:

TMS 1100

- Pin-for-pin interchangeable with the TMS 1000
- 16,384-bit ROM, 2048 eight-bit instruction words
- 512-bit RAM, 128 four-bit data words
- 11 individually latched R outputs, 28-pin package

TMS 1300

- 16,384-bit ROM
- 512-bit RAM
- 16 individually latched R outputs, 40-pin package

Many industrial, consumer, and business applications can be implemented with a microcomputer having the capabilities of two TMS 1000 devices. With considerably lower system cost, the TMS 1100/1300 single-device microcomputers enable a number of applications that previously required two TMS 1000's or external read/write memory. In the 40-pin version, the TMS 1300, the maximum number of R outputs is increased to 16. Displays 16 characters long as well as a 64-position keyboard or switch matrix (16 X 4) are scanned directly by the TMS 1300.

The TMS 1100/1300 operation is identical to that of the TMS 1000/†200 except where noted otherwise in the following paragraphs.

FIGURE 6 — TMS 1100/1300 LOGIC BLOCKS

3.2 ROM OPERATION

The TMS 1100/1300 instruction ROM contains two chapters of 16 pages each. A page contains 64 eight-bit words. The chapter logic consists of three control bits, chapter address, chapter buffer, and chapter subroutine. The chapter buffer bit is controlled by a complement chapter buffer instruction 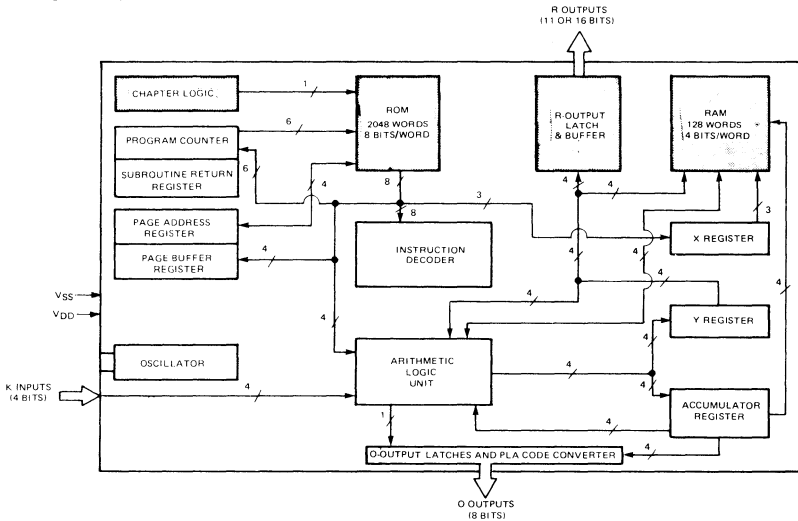(see COMC in Table 3). The chapter buffer bit transfers into the current chapter address if a branch or call executes successfully. If a call is successful, the return chapter is saved in a chapter subroutine latch. Since the buffer bit is changeable without affecting the chapter subroutine-return address, up to 128 words that are contained on two pages of alternate chapters are available in a single subroutine. The program counter and page addressing operation is identical to the TMS 1000/1200 explained in 2-2.

TABLE 3
TMS 1100/1300 STANDARD INSTRUCTION SET

FUNCTION	MNEMONIC	STATUS EFFECT C	N	DESCRIPTION
Register-to-	TAY			Transfer accumulator to Y register
Register	TYA			Transfer Y register to accumulator
Transfer	CLA			Clear accumulator
Register to	TAM			Transfer accumulator to memory
Memory	TAMIYC	Y		Transfer accumulator to memory and increment Y register. If carry, one to status.
	TAMDYN	Y		Transfer accumulator to memory and decrement Y register. If no borrow, one to status.
	TAMZA			Transfer accumulator to memory and zero accumulator
Memory to	TMY			Transfer memory to Y register
Register	TMA			Transfer memory to accumulator
	XMA			Exchange memory and accumulator
Arithmetic	AMAAC	Y		Add memory to accumulator, results to accumulator. If carry, one to status.
	SAMAN	Y		Subtract accumulator from memory, results to accumulator. If no borrow, one to status.
	IMAC	Y		Increment memory and load into accumulator. If carry, one to status.
	DMAN	Y		Decrement memory and load into accumulator. If no borrow, one to status.
	IAC	Y		Increment accumulator. If carry, one to status.
	DAN	Y		Decrement accumulator. If no borrow, one to status.
	A2AAC	Y		Add 2 to accumulator. Results to accumulator. If carry, one to status.
	A3AAC	Y		Add 3 to accumulator. Results to accumulator. If carry, one to status.
	A4AAC	Y		Add 4 to accumulator. Results to accumulator. If carry, one to status.
	A5AAC	Y		Add 5 to accumulator. Results to accumulator. If carry, one to status.
	A6AAC	Y		Add 6 to accumulator. Results to accumulator. If carry, one to status.
	A7AAC	Y		Add 7 to accumulator. Results to accumulator. If carry, one to status.
	A8AAC	Y		Add 8 to accumulator. Results to accumulator. If carry, one to status.
	A9AAC	Y		Add 9 to accumulator. Results to accumulator. If carry, one to status.
	A10AAC	Y		Add 10 to accumulator. Results to accumulator. If carry, one to status.
	A11AAC	Y		Add 11 to accumulator. Results to accumulator. If carry, one to status.
	A12AAC	Y		Add 12 to accumulator. Results to accumulator. If carry, one to status.
	A13AAC	Y		Add 13 to accumulator. Results to accumulator. If carry, one to status.
	A14AAC	Y		Add 14 to accumulator. Results to accumulator. If carry, one to status.
	IYC	Y		Increment Y register. If carry, one to status.
	DYN	Y		Decrement Y register. If no borrow, one to status.
	CPAIZ	Y		Complement accumulator and increment. If then zero, one to status.

— CONTINUED —

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TABLE 3
TMS 1100/1300 STANDARD INSTRUCTION SET (Continued)

| FUNCTION | MNEMONIC | STATUS EFFECT | | DESCRIPTION |
		C	N	
Arithmetic Compare	ALEM	Y		If accumulator less than or equal to memory, one to status.
Logical Compare	MNEA		Y	If memory is not equal to accumulator, one to status.
	MNEZ		Y	If memory not equal to zero, one to status.
	YNEA		Y	If Y register not equal to accumulator, one to status and status latch.
	YNEC		Y	If Y register not equal to a constant, one to status.
Bits in Memory	SBIT			Set memory bit
	RBIT			Reset memory bit
	TBIT1		Y	Test memory bit. If equal to one, one to status.
Constants	TCY			Transfer constant to Y register
	TCMIY			Transfer constant to memory and increment Y
Input	KNEZ		Y	If K inputs not equal to zero, one to status.
	TKA			Transfer K inputs to accumulator
Output	SETR			Set R output addressed by Y
	RSTR			Reset R output addressed by Y
	TDO			Transfer data from accumulator and status latch to O-outputs
RAM X Addressing	LDX			Load X with file address
	COMX			Complement the MSB of X
ROM Addressing	BR			Branch on status = one
	CALL			Call subroutine on status = one
	RETN			Return from subroutine
	LDP			Load page buffer with constant
	COMC			Complement chapter

NOTES: C-Y (Yes) means that if there is a carry out of the MSB, status output goes to the one state. If no carry is generated, status output goes to the zero state.

N-Y (Yes) means that if the bits compared are not equal, status output goes to the one state. If the bits are equal status output goes to the zero state.

A zero in status remains through the next instruction cycle only. If the next instruction is a branch or call and status is a zero, then the branch or call is not executed successfully.

3.3 RAM OPERATION

The TMS 1100/1300 devices contain a 512-bit RAM for data storage. The matrix consists of eight files, each file containing 16 four-bit words. Similar to the TMS 1000/1200, the X and Y registers address the RAM. The Y register selects one of the 16 words in a file and the X register (three bits long) selects one of eight possible files. When using the set or reset R instructions, the X register must be less than four.

3.4 OUTPUT

The TMS 1100 is pin-for-pin interchangeable with the TMS 1000 and contains eleven R outputs and eight O outputs.

The R-output capability in the TMS 1300 is increased to 16 output latches. These extra latches perform control functions directly that would have required external decoding logic in the TMS 1100 device. These additional R outputs can be set to any combination. For example, Figure 2 shows an O-output data bus going into the transmitter section of the UART. If the O-output PLA is programmed to send out four bits of binary data (when directed to do so by the status latch), then three additional R outputs connected to the UART transmitter input provides the user with full seven-bit ASCII output capability.

4. TMS 1000/1200 AND TMS 1100/1300 ELECTRICAL AND MECHANICAL SPECIFICATIONS

4.1 ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)*

Voltage applied to any device terminal (see Note 1) . . . . −20 V
Supply voltage, V_{DD} . . . . −20 V to 0.3 V
Data input voltage . . . . −20 V to 0.3 V
Clock input voltage . . . . −20 V to 0.3 V
Average output current (see Note 2): O outputs . . . . −24 mA
　　　　　　　　　　　　　　　　　 R outputs . . . . −14 mA
Peak output current: O outputs . . . . −48 mA
　　　　　　　　　 R outputs . . . . −28 mA
Continuous power dissipation: TMS 1000/1100 NL . . . . 400 mW
　　　　　　　　　　　　　　TMS 1200/1300 NL . . . . 600 mW
Operating free-air temperature range . . . . 0°C to 70°C
Storage temperature range . . . . −55°C to 150°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

4.2 RECOMMENDED OPERATING CONDITIONS

PARAMETER		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD} (see Note 3)		−14	−15	−17.5	V
High-level input voltage, V_{IH} (see Note 4)	K	−1.3	−1	0.3	V
	INIT or Clock	−1.3	−1	0.3	
Low-level input voltage, V_{IL} (see Note 4)	K	V_{DD}		−4	V
	INIT or Clock	V_{DD}	−15	−8	
Clock cycle time, $t_{c(\phi)}$		2.5	3	10	μs
Instruction cycle time, t_c		15	·	60	μs
Pulse width, clock high, $t_{w(\phi H)}$		1			μs
Pulse width, clock low, $t_{w(\phi L)}$		1			μs
Sum of rise time and pulse width, clock high, $t_r + t_{w(\phi H)}$		1.25			μs
Sum of fall time and pulse width, clock low, $t_f + t_{w(\phi L)}$		1.25			μs
Oscillator frequency, f_{osc}		100		400	kHz
Operating free-air temperature, T_A		0		70	°C

NOTES: 1. Unless otherwise noted, all voltages are with respect to V_{SS}.
　　　　2. These average values apply for any 100-ms period.
　　　　3. Ripple must not exceed 0.2 volts peak-to-peak in the operating frequency range.
　　　　4. The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this specification for logic voltage levels only.
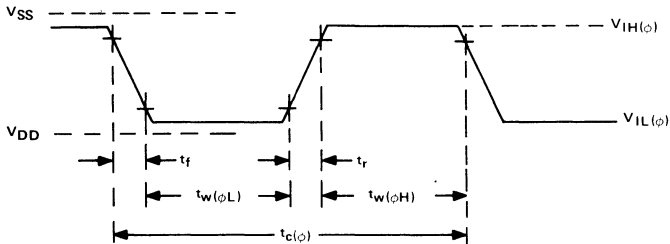
NOTE: Timing points are 90% (high) and 10% (low).

FIGURE 7 — EXTERNALLY DRIVEN CLOCK INPUT WAVEFORM

4.3 ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)

PARAMETER			TEST CONDITIONS		MIN	TYP[†]	MAX	UNIT
I_I	Input current, K inputs		$V_I = 0$ V		50	300	500	μA
V_{OH}	High-level output voltage	O outputs	$I_O = -10$ mA			$-1.1^\ddagger$	$-0.6^\ddagger$	V
	(see Note 1)	R outputs	$I_O = -2$ mA			-0.75	-0.4	
I_{OL}	Low-level output current		$V_{OL} = V_{DD}$				-100	μA
$I_{DD(av)}$	Average supply current from V_{DD} TMS 1000/1200 (see Note 2)		All outputs open			-6	-10	mA
$I_{DD(av)}$	Average supply current from V_{DD} TMS1100/1300 (see Note 2)		All outputs open			-7	-11	mA
$P_{(AV)}$	Average power dissipation TMS 1000/1200 (see Note 2		All outputs open			90	175	mW
$P_{(AV)}$	Average power dissipation TMS1100/1300 (see Note 2)		All outputs open			105	193	mW
f_{osc}	Internal oscillator frequency		$R_{ext} = 50$ kΩ,	$C_{ext} = 47$ pF	250	300	350	kHz
C_i	Small-signal input capacitance, K inputs		$V_I = 0$,	$f = 1$ kHz		10		pF
$C_{i(\phi)}$	Input capacitance, clock input		$V_I = 0$,	$f = 100$ kHz		25		pF

[†] All typical values are at $V_{DD} = -15$ V, $T_A = 25°$C.

[‡] Parts with V_{OH} of -2 V minimum, -1.3 V typical, are available if requested.

NOTES: 1. The algebraic convention where the most-positive (least-negative) limit is designa'.d as maximum is used in this specification for logic voltage levels only.

2. Values are given for the open-drain O and R output configurations. Pull-down resistors are optionally available on all outputs and increase I_{DD} (see Section 4.4).

4.4 SCHEMATICS OF INPUTS AND OUTPUTS

TYPICAL OF ALL K INPUTS
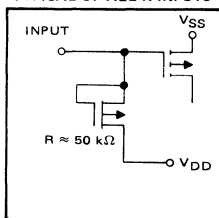
TYPICAL OF ALL O AND R OPEN-DRAIN OUTPUTS
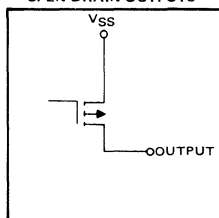
TYPICAL OF ALL O AND R OUTPUTS WITH OPTIONAL PULL-DOWN RESISTORS
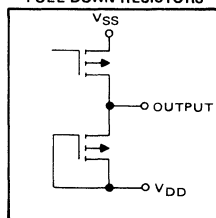
The O outputs have nominally 60 Ω on-state impedance; however, upon request a 130-Ω buffer can be mask programmed (see note [‡] section 4.3).

The value of the pull-down resistors is mask alterable and provides the following nominal short-circuit output currents (outputs shorted to V_{SS}):

O outputs: 100, 200, 300, 500, or 900 μA

R outputs: 100, 150, or 200 μA.

4.5 INTERNAL OR EXTERNAL CLOCK

If the internal oscillator is used, the OSC1 and OSC2 terminals are shorted together and tied to an external resistor to V_{DD} and a capacitor to V_{SS}. If an external clock is desired, the clock source may be connected to OSC1 and OSC2 shorted to V_{SS}.

CONNECTION FOR INTERNAL OSCILLATOR
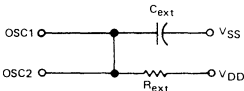
TYPICAL INTERNAL OSCILLATOR FREQUENCY
vs
EXTERNAL RESISTANCE
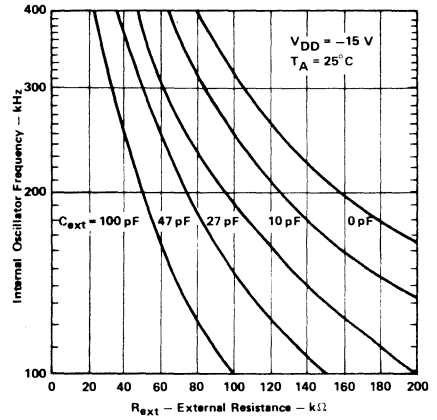
4.6 TYPICAL BUFFER CHARACTERISTICS

O OUTPUTS

HIGH-LEVEL OUTPUT CURRENT
vs
HIGH-LEVEL OUTPUT VOLTAGE
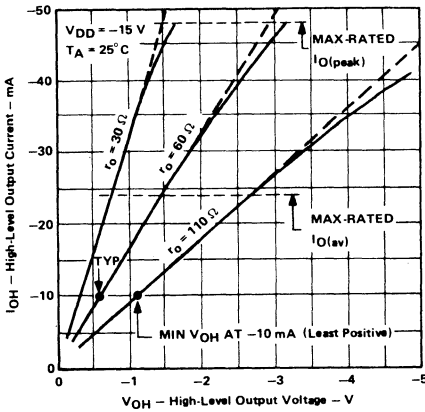
R OUTPUTS

HIGH-LEVEL OUTPUT CURRENT
vs
HIGH-LEVEL OUTPUT VOLTAGE

1
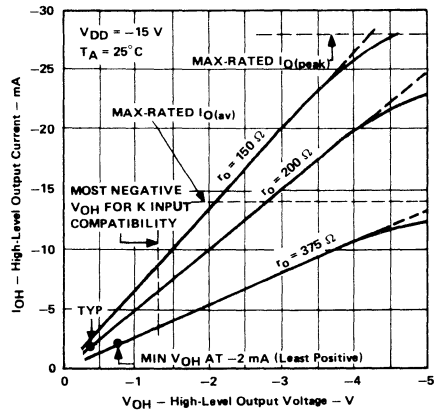
4.7 OUTPUT, INPUT, AND INSTRUCTION TIMING

EXECUTE SETR OR RSTR OR TDO INSTRUCTION | NEXT INSTRUCTION

OSC

APPROXIMATE INTERNAL OSCILLATOR WAVEFORM

φ1

φ2

φ5

φ3

INSTRUCTION

See Note 1

SETR
φ2
H
L

See Note 2

RSTR
H
L

See Note 2 | See Note 1

TDO
φ3
H
L

FETCH CYCLE – INSTRUCTION N | EXECUTE CYCLE – INSTRUCTION N
EXECUTE CYCLE – INSTRUCTION N-1 | FETCH CYCLE – INSTRUCTION N+1

φ1

φ5

φ2

ROM
ADDRESS ── FETCH ── INST DECODE ── INSTRUCTION EXECUTE ──

UPDATE PC | READ RAM | WRITE RAM

RAM ADDRESS | ALU INPUT | REGISTER STORE

EXECUTE BR/CALL

K INPUT VALID

TIME ──→

NOTES: 1. Initial rise time is load dependent. The high-level output voltage, V_{OH}, is characterized following the indicated clock period. (See Section 4.6).
2. Rise and fall times are load dependent.

4.8 INTERFACE BETWEEN LOW-POWER SCHOTTKY AND TMS 1000

4.8.1 Push-Pull to MOS Input, $V_{SS} = V_{CC}$

Low-power Schottky series logic interfaces, as shown below, to the TMS 1000 series low-voltage devices and has the advantage of reduced power supply requirements. The level-shifting components are minimal if the V_{CC} supply is common to the V_{SS} supply.

To obtain a sufficient high-level input voltage, V_{IH}, a pull-up resistor R1 is tied from V_{SS} to the K input. With the upper transistor in the TTL push-pull output on and reverse biased by R1, the typical resistor value is calculated:

$$R1 = \frac{V_{IH}}{V_{DD}} \cdot (R2 + R1) \qquad\qquad R2 \gg R1$$

$$R1 \approx \frac{V_{IH}}{V_{DD}} \cdot R2$$

For example if a -0.5-volt noise margin is desired, the recommended V_{IH} is -1.3 volts plus 0.5 volts, which equals -0.8 volts. Since V_{DD} is -17.5 volts maximum, R1 is:

$$R1 = \frac{-0.8\ V}{-17.5\ V} \cdot 50\ k\Omega = 2.28\ k\Omega$$

To use $\pm10\%$ resistors, R1 should be at most 2.0 kΩ. This procedure for calculating a pull-up resistor applies to standard TTL and open-collector interface as well.

If the lower transistor in the TTL push-pull output is on, the output current is 2 to 3 milliamperes and the low-level output voltage is typically 0.2 volts. Thus the low-level input voltage, V_{IL}, for the K inputs is obtained with 0.3-volt noise margin (at V_{CC} minimum of 4.5 volts). For high-noise environments, an open-collector interface device is shown in paragraph 4.11.
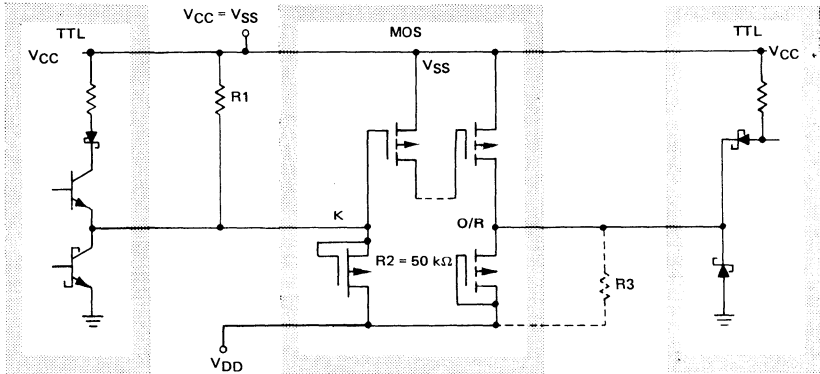
POWER SUPPLIES	VOLTAGE	
MOS TTL	COMBINATIONS	
$V_{SS} = V_{CC}$	5 V	0 V
GND	0 V	−5 V
V_{DD}	−10 V	−15 V

NOTE: TI cannot assume responsibility for any circuits shown or represent that they are free from patent infringement.

4.8.2 MOS to Low-Power Schottky, $V_{SS} = V_{CC}$

Due to the low current ($-400\ \mu A$) required to bring a Schottky TTL input low, a single 22-kilohm pull-down resistor (R3) or the 900-microampere pull-down option (O outputs only) provides the necessary low-level input current. The high-level input voltage with the V_{CC} supply at 4.5 volts has 1-volt noise margin.

If a fan-out to more than one TTL circuit is used, the pull-down resistor value is divided by the fan-out number. In the increased fan-out situation, an O output requires an external resistor to assist the 900-microampere pull-down option.

4.9 INTERFACE BETWEEN STANDARD TTL AND TMS 1000

4.9.1 Push-Pull to MOS Input, $V_{SS} = V_{CC}$

Standard TTL logic interfaces as shown with the TMS 1000-series low-voltage devices. The input pull-up resistor R1 is calculated by the same procedure as found in paragraph 4.8.1. The lower push-pull device is stronger in standard TTL compared to Schottky versions. Thus a lower low-level input voltage, V_{IL}, is expected to provide a 0.1-volt increase in noise margin.
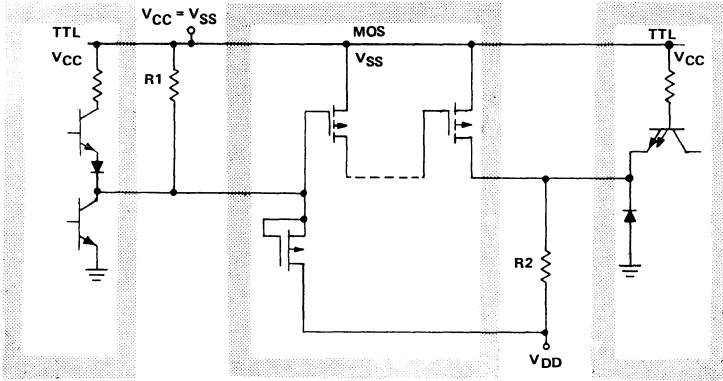
POWER SUPPLIES		VOLTAGE	
MOS	TTL	COMBINATIONS	
$V_{SS} = V_{CC}$		5 V	0 V
	GND	0 V	−5 V
V_{DD}		−10 V	−15 V

4.9.2 MOS to Standard TTL, $V_{SS} = V_{CC}$

Since standard TTL requires −1.6 milliampere of low-level input current, a pull-down resistor R2 is used for both O and R outputs. With either of the outputs connected to a standard TTL input, a 6.2-kilohm resistor tied to V_{DD} provides slightly more low-level input current. To calculate the pull-down resistor's value, it is assumed that there is negligible current through the open-drain MOS output and that the short-circuit pull-down options are not programmed:

$$R2 \approx \frac{-10\ V}{-1.6\ mA \cdot Fan\text{-}Out\ Number}$$

4.10 INTERFACE BETWEEN OPEN-COLLECTOR TTL AND MOS

4.10.1 SN7406, SN7407 Open-Collector to MOS Input, V_{DD} = TTL Ground

The SN7406 and SN7407 provide superior noise margins for converting TTL logic levels to MOS inputs. A single pull-up resistor R1 is calculated by the same procedure as found in 4.8.1. The major difference in noise margin occurs with the output low and results from the open-collector being about 1 volt above TTL ground. Thus, the low-level noise margin is approximately 9 volts. More high-level noise margin is obtained by lowering the value of R1 at the cost of increased power dissipation.
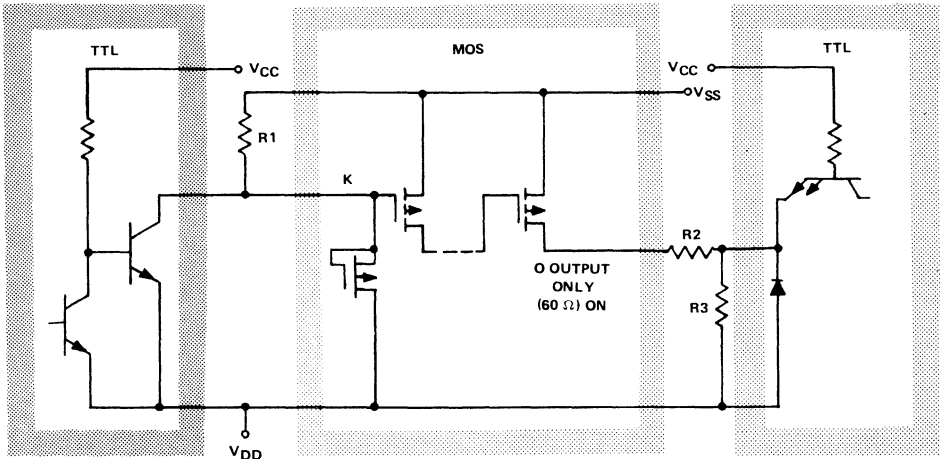
POWER SUPPLIES		VOLTAGE	
MOS	TTL	COMBINATIONS	
V_{SS}		15 V	10 V
	V_{CC}	5 V	0 V
V_{DD} =	GND	0 V	−5 V

4.10.2 Interface Between MOS and Standard TTL, V_{DD} = TTL Ground

When the TTL ground and V_{DD} supplies are common, two resistors, R2 and R3, are required for level-shifting. This interface circuit applies to Schottky TTL also when V_{DD} = GND; only the values of R2 and R3 are changed.

To supply −1.6 milliamperes of low-level input current at 0.4 V above ground requires a clamping resistor R3.

$$R3 = \frac{0.4 \text{ V}}{1.6 \text{ mA}} = 250 \ \Omega$$

The series limiting resistor R2 is calculated to provide a high-level input voltage between 2.7 volts and 5 volts above TTL ground. For the O outputs ($r_{o(on)}$ = 60 Ω typically), R2 is between 1 kilohm and 500 ohms. The maximum current rating for the O output is not to be exceeded, and the fan-out is one TTL input maximum.

Note that when the low-level input current is reduced to 400 microamperes for low-power Schottky TTL, the same resistor network provides a fan-out of four using the O outputs. For an R output to Schottky input with V_{DD} = TTL ground, a fan-out of two is obtainable when R2 $\approx$ 1 kilohm and R3 $\approx$ 500 ohms.

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TYPICAL SCANNED LED INTERFACE
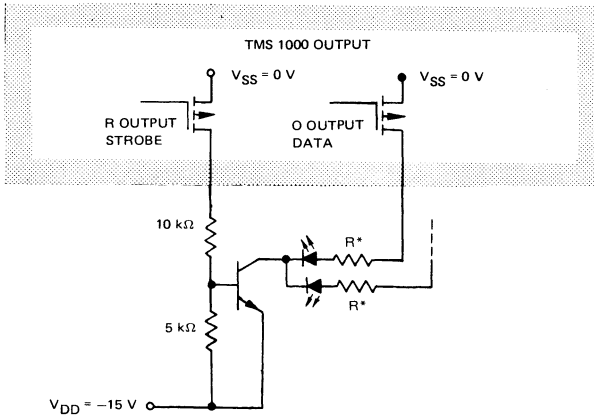
*R value depends on duty cycle and brightness.

†The maximum number of LED's depends on the current required by each and the driver used.

SN75492 is recommended for the R-output interface for up to six display characters. The SN75491 quad driver is recommended for O-output interface to LED's requiring high current.

4.12 TERMINAL ASSIGNMENTS

TMS 1000/TMS 1100

R8	1	28	R7
R9	2	27	R6
R10	3	26	R5
VDD	4	25	R4
K1	5	24	R3
K2	6	23	R2
K4	7	22	R1
K8	8	21	R0
INIT	9	20	VSS
O7	10	19	OSC2
O6	11	18	OSC1
O5	12	17	O0
O4	13	16	O1
O3	14	15	O2

TMS 1200

R8	1	40	R7
R9	2	39	R6
R10	3	38	R5
R11	4	37	R4
R12	5	36	R3
VDD	6	35	NC
K1	7	34	NC
K2	8	33	NC
K4	9	32	NC
K8	10	31	R2
INIT	11	30	R1
O7	12	29	R0
NC	13	28	VSS
NC	14	27	OSC2
NC	15	26	OSC1
O6	16	25	O0
O5	17	24	O1
O4	18	23	O2
O3	19	22	NC
NC	20	21	NC

TMS 1300

R11	1	40	R10
R12	2	39	R9
R13	3	38	R8
R14	4	37	R7
R15	5	36	R6
VDD	6	35	NC
K1	7	34	R5
K2	8	33	R4
K4	9	32	R3
K8	10	31	R2
INIT	11	30	R1
O7	12	29	R0
NC	13	28	VSS
NC	14	27	OSC2
NC	15	26	OSC1
O6	16	25	O0
O5	17	24	O1
O4	18	23	O2
O3	19	22	NC
NC	20	21	NC

NC — NO INTERNAL CONNECTION

5. TMS 1070 AND TMS 1270 MICROCOMPUTERS

5.1 INTRODUCTION

The TMS 1000 series flexibility is augmented by two versions of high-voltage (35-volt) microcomputers, the TMS 1070 and the TMS 1270. The standard instruction set and operation is identical to that of the TMS 1000/1200. Architecturally, the devices are identical to the TMS 1000/1200 except that two additional O-output OR-matrix terms were added to provide a total of ten O outputs in the TMS 1270, a 40-pin package unit. The TMS 1070/1270 provides direct interface to low-voltage flourescent displays. The TMS 1070/1270 interfaces with all circuits requiring up to 35-volt levels.

The accompanying diagram, Figure 8, shows an interface to a 30-volt fluorescent display.
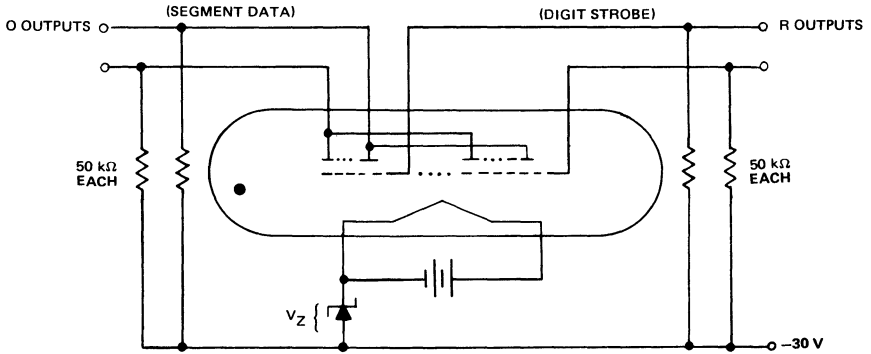
FIGURE 8 – STROBED FLUORESCENT DISPLAY INTERCONNECT

5.2 DESIGN SUPPORT

The TMS 1070/1270 simulation is provided by several time-sharing services. The assembler and simulator programs are accessed by specifying the appropriate device option in the assembler TITLE command.

Functional hardware simulation is accomplished by an SE-1 or an HE-2. To emulate more than eight O outputs in the TMS 1270 with an HE-2 requires an external decoder. Level-shifting buffers allow functional evaluation in the high-voltage prototyping systems.

2!

5.3 ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)*

Voltage applied to any device terminal (see Note 1)	−20 V
Supply voltage, V_{DD}	−20 V to 0.3 V
Data input and output voltage with V_{DD} applied (see Note 2)	−35 V to 0.3 V
Clock input and INIT input voltage	−20 V to 0.3 V
Average output current (see Note 3): O outputs	−2.5 mA
R outputs	−12 mA
Peak output current: O outputs	−5 mA
R outputs	−24 mA
Continuous power dissipation: TMS 1070 NL	400 mW
TMS 1270 NL	600 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−55°C to 150°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.4 RECOMMENDED OPERATING CONDITIONS

PARAMETER		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD} (see Note 4)		−14	−15	−17.5	V
High-level input voltage, V_{IH} (see Note 5)	K	−6		0.3	V
	INIT or Clock	−1.3	−1	0.3	
Low-level input voltage, V_{IL} (see Note 5)	K (See Note 2)	−35		−8	V
	INIT or Clock	V_{DD}	−15	−8	
Clock cycle time, $t_{c(\phi)}$		2.5	3	10	µs
Instruction cycle time, t_c		15		60	µs
Pulse width, clock high, $t_{w(\phi H)}$		1			µs
Pulse width, clock low, $t_{w(\phi L)}$		1			µs
Sum of rise time and pulse width, clock high, $t_r + t_{w(\phi H)}$		1.25			µs
Sum of fall time and pulse width, clock low, $t_f + t_{w(\phi L)}$		1.25			µs
Oscillator frequency, f_{osc}		100		400	kHz
Operating free-air temperature, T_A		0		70	°C

NOTES: 1. Unless otherwise noted, all voltages are with respect to V_{SS}.
   2. V_{DD} must be within the recommended operating conditions specified in 5.4.
   3. These average values apply for any 100-ms period.
   4. Ripple must not exceed 0.2 volts peak-to-peak in the operating frequency range.
   5. The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this specification for logic voltage levels only.

5.5 ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)

	PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
I_I	Input current, K inputs		$V_I = 0$ V		40	100	300	μA
V_{OH}	High-level output voltage (see Note 1)	O outputs	$I_O = -1$ mA.		−1	−0.5		V
		R outputs	$I_O = -10$ mA		−4.5	−2.25		
I_{OL}	Low-level output current		$V_{OL} = V_{DD}$				−100	μA
$I_{DD(av)}$	Average supply current from V_{DD}		All outputs open			−6	−10	mA
$P_{(AV)}$	Average power dissipation		All outputs open			90	175	mW
f_{osc}	Internal oscillator frequency		$R_{ext} = 50$ kΩ,	$C_{ext} = 47$ pF	250	300	350	kHz
C_i	Small-signal input capacitance, K inputs		$V_I = 0$ V,	f = 1 kHz		10		pF
$C_{i(\phi)}$	Input capacitance, clock input		$V_I = 0$ V,	f = 100 kHz		25		pF

†All typical values are at $V_{DD} = -15$ V, $T_A = 25°$C.

NOTE 1: The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this specification for logic voltage levels only.
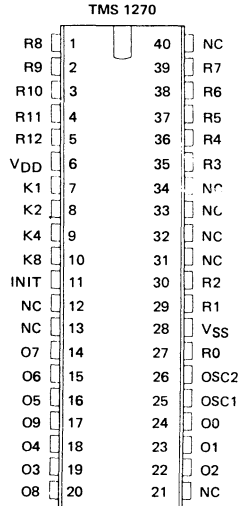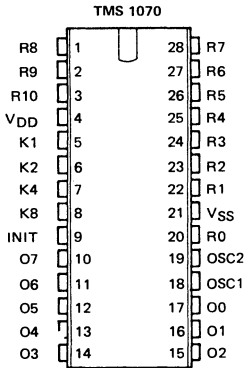
5.6 TERMINAL ASSIGNMENTS

TMS 1070

R8	1		28	R7
R9	2		27	R6
R10	3		26	R5
V_{DD}	4		25	R4
K1	5		24	R3
K2	6		23	R2
K4	7		22	R1
K8	8		21	V_{SS}
INIT	9		20	R0
O7	10		19	OSC2
O6	11		18	OSC1
O5	12		17	O0
O4	13		16	O1
O3	14		15	O2

TMS 1270

R8	1		40	NC
R9	2		39	R7
R10	3		38	R6
R11	4		37	R5
R12	5		36	R4
V_{DD}	6		35	R3
K1	7		34	NC
K2	8		33	NC
K4	9		32	NC
K8	10		31	NC
INIT	11		30	R2
NC	12		29	R1
NC	13		28	V_{SS}
O7	14		27	R0
O6	15		26	OSC2
O5	16		25	OSC1
O9	17		24	O0
O4	18		23	O1
O3	19		22	O2
O8	20		21	NC

NC – NO INTERNAL CONNECTION

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6. MICROCOMPUTER SYSTEM EVALUATORS, SE-1 AND SE-2

6.1 INTRODUCTION

The SE-1 and SE-2 are functionally identical to the TMS 1000/1200 and TMS 1100/1300, respectively, when combined with external instruction memory. The system evaluators are ideally suited for prototype fabrication and field testing. The TMS 1000/1200 and TMS 1100/1300 standard instruction sets are used in the SE-1 and SE-2, respectively. Each unit sends out an instruction address to a PROM (or to other memory device), which feeds an eight-bit instruction word back into the system evaluator for execution. Table 4 summarizes the functions of both system evaluators. Costly errors in mask programming the TMS 1000 series can be eliminated by testing algorithms thoroughly before submitting the final code to Texas Instruments for manufacturing.

TABLE 4
SYSTEM EVALUATORS SE-1 AND SE-2

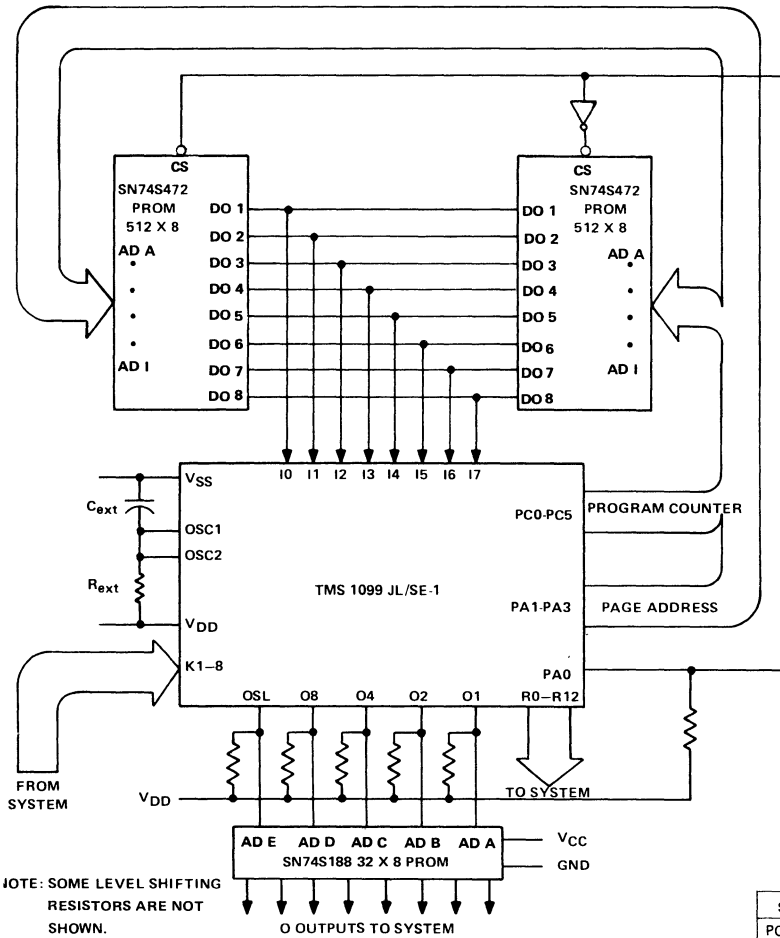|	SE-1	SE-2
TMS number	TMS 1099 JL	TMS 1098 JL
Simulates microcomputers (instruction set)	TMS 1000/1200 TMS 1070/1270	TMS 1100/1300
Maximum ROM addresses	1024 words X 8 bits/word	2048 words X 8 bits/word
O outputs	5	5
Maximum R outputs	13	16
Single power supply (15 V)	Yes	Yes
Internal or external oscillator	Yes	Yes

6.2 OPERATION

When the system evaluators are combined with external instruction memory, their operation is identical to their respective TMS 1000 series devices described in the *"TMS 1000 Series Programmer's Reference Manual"* (CM 122-1). A dedicated parallel-instruction address selects the instruction word that transfers into the system evaluator through a dedicated eight-bit-parallel input. Therefore, the user does not need external timing or multiplexing circuits.

To store the program, Texas Instruments provide a variety of memory products. The TTL PROM's, SN74S470, 'S471, 'S472, and 'S473, and TTL RAM's, SN74S209 and 'S309, store the instruction codes for program execution by the system evaluator. These TTL RAM's, as well as the MOS static RAM's such as the TMS 4033, are convenient when a teletype or paper-tape interface is available for entering an assembled program.

The system evaluators O-output Programmable Logic Array (PLA) transfers the five-bit O-register contents directly to the five O outputs, O1, O2, O4, O8, and OSL. Various devices are available that can emulate the O-output PLA coding. If seven-segment displays are used, an SN7448, SN7449, or equivalent, is ideal. For nonstandard codes, an SN74188 PROM (organized as 32 X 8) provides the code conversion (two required for users with TMS 1270 applications having ten O outputs).

If the system evaluators are used to emulate the TMS 1000 series devices, the user must remember that the O-output PLA has a maximum of 20 product terms. Refer to the O-output PLA description in the *TMS 1000 Series Programmer's Reference Manual* for details.

Figure 9 and 10 show typical configurations with the system evaluators in prototyping systems.

CS
SN74S472
PROM
512 X 8
AD A
•
•
•
AD I

DO 1
DO 2
DO 3
DO 4
DO 5
DO 6
DO 7
DO 8

CS
DO 1
DO 2
DO 3
DO 4
DO 5
DO 6
DO 7
DO 8

SN74S472
PROM
512 X 8
AD A
•
•
•
AD I

V_{SS}

C_{ext}

OSC1
OSC2

R_{ext}

V_{DD}

K1—8

I0 I1 I2 I3 I4 I5 I6 I7

TMS 1099 JL/SE-1

PC0-PC5 **PROGRAM COUNTER**

PA1-PA3 **PAGE ADDRESS**

PA0

OSL   O8   O4   O2   O1   R0—R12

FROM SYSTEM V_{DD}

TO SYSTEM

AD E   AD D   AD C   AD B   AD A
SN74S188 32 X 8 PROM

V_{CC}
GND

NOTE: SOME LEVEL SHIFTING RESISTORS ARE NOT SHOWN.

O OUTPUTS TO SYSTEM

POWER SUPPLIES MOS TTL	VOLTAGE COMBINATIONS	
$V_{SS} = V_{CC}$	5 V	0 V
GND	0 V	5 V
V_{DD}	−10 V	−15 V

INTERFACE

SE-1	PROM
PC5	AD A
PC4	AD B
PC3	AD C
PC2	AD D
PC1	AD E
PC0	AD F
PA3	AD G
PA2	AD H
PA1	AD I
PA0/$\overline{PA0}$	$\overline{CS}$

FIGURE 9 — BLOCK DIAGRAM OF TYPICAL APPLICATION — PROTOTYPING SYSTEM WITH SE-1

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INTERFACE

SE-1	PROM
PC5	AD A
PC4	AD B
PC3	AD C
PC2	AD D
PC1	AD E
PC0	AD F
PA3	AD G
PA2	AD H
PA1	AD I
PA0	SN74156
CA	SN74156

SN74S472 PROM (×4 blocks, one labeled 512 X 8)

DO1, DO2, DO3, DO4, DO5, DO6, DO7, DO8

AD A ... AD I, CS

1/2 OF 2- TO 4-LINE DECODER
SN74156
CHAPTER ADDRESS

TMS 1099 JL/SE-2

VSS, OSC1, OSC2, VDD, K1–K8
Cext, Rext

I0 I1 I2 I3 I4 I5 I6 I7

PC0–PC5 PROGRAM COUNTER
PA1–PA3 PAGE ADDRESS
PA0
CA

OSL O8 O4 O2 O1 R0–R15

FROM SYSTEM   VDD
TO SYSTEM

NOTE: SOME LEVEL SHIFTING RESISTORS ARE NOT SHOWN.

AD E AD D AD C AD B AD A   VCC
GND

O OUTPUTS TO SYSTEM

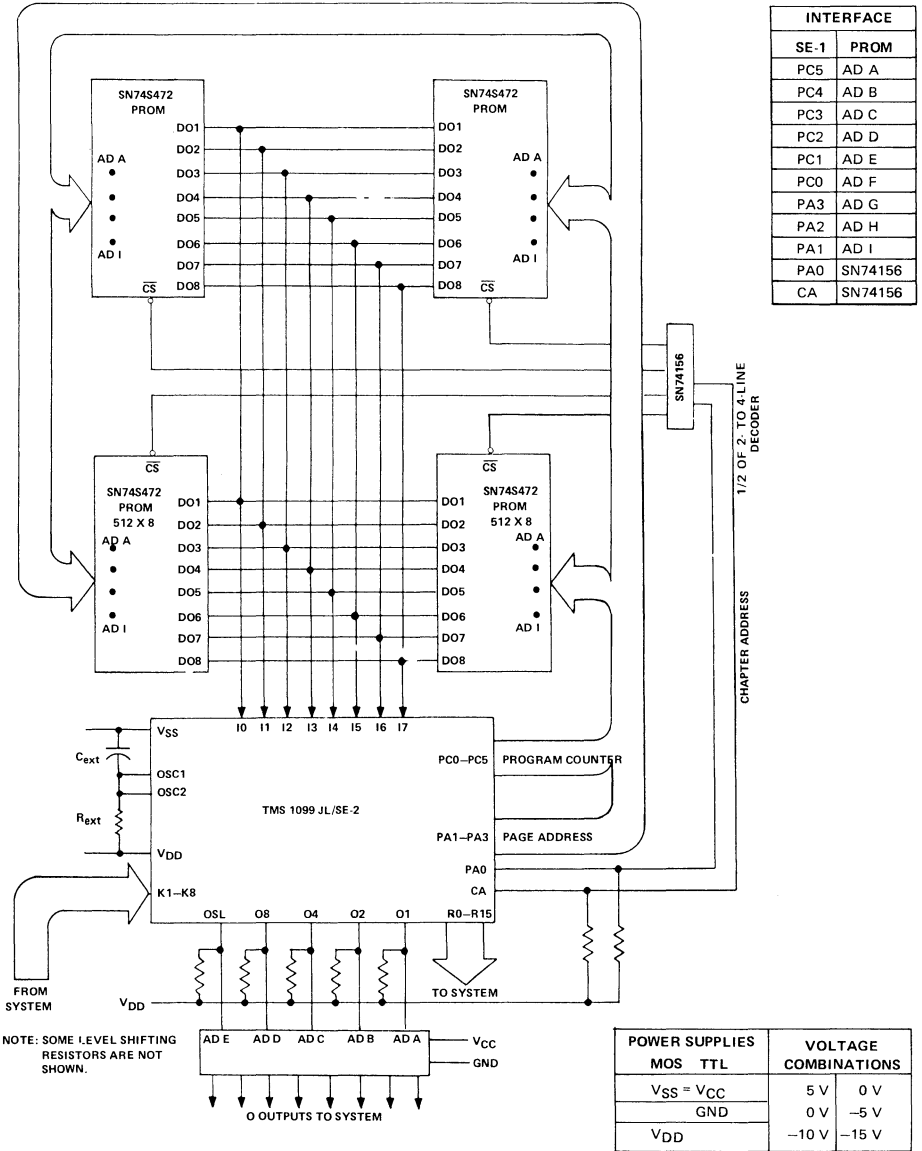| POWER SUPPLIES		VOLTAGE COMBINATIONS	
MOS	TTL		
VSS = VCC		5 V	0 V
GND		0 V	−5 V
VDD		−10 V	−15 V

FIGURE 10 — BLOCK DIAGRAM OF TYPICAL APPLICATION — PROTOTYPING SYSTEM WITH SE-2

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6.3 ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)*

Voltage applied to any device terminal (see Note 1) . . . . −20 V
Supply voltage, V_{DD} . . . . −20 V to 0.3 V
Data input voltage . . . . −20 V to 0.3 V
Clock input voltage . . . . −20 V to 0.3 V
Average output current (see Note 2)
   O, R, PC, PA, CA . . . . −14 mA
Peak output current
   O, R, PC, PA, CA . . . . −28 mA
Operating free-air temperature range . . . . 0°C to 70°C
Storage temperature range . . . . −55°C to 150°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.4 RECOMMENDED OPERATING CONDITIONS

PARAMETER		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD} (see Note 3)		−14	−15	−17.5	V
High-level input voltage, V_{IH} (see Note 4)	K	−1.3	−1	0.3	V
	INIT or Clock	−1.3	−1	0.3	
Low-level input voltage, V_{IL} (see Note 4)	K	V_{DD}		−4	V
	INIT or Clock	V_{DD}	−15	−8	
Clock cycle time, $t_{c(\phi)}$		2.5	3	10	μs
Instruction cycle time, t_c		15		60	μs
Pulse width, clock high, $t_{w(\phi H)}$		1			μs
Pulse width, clock low, $t_{w(\phi L)}$		1			μs
Sum of rise time and pulse width, clock high, $t_r + t_{w(\phi H)}$		1.25			μs
Sum of fall time and pulse width, clock low, $t_f + t_{w(\phi L)}$		1.25			μs
Oscillator frequency, f_{osc}		100		400	kHz
Operating free-air temperature, T_A		0		70	°C

6.5 ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I_I	Input current	$V_I = V_{SS}$	50	300	500	μA
V_{OH}	High-level output	O, PC, PA, and CA	$I_O = -2$ mA	−1	−0.5		V
	voltage (see Note 3)	R		−0.75	−0.4		
I_{OL}	Low-level output current	$V_{OL} = V_{DD}$			−100	μA
$I_{DD(av)}$	Average supply current from V_{DD}	All outputs open		−7	−11	mA
$P_{(AV)}$	Average power dissipation	All outputs open		105	193	mW
f_{osc}	Internal oscillator frequency	$R_{ext} = 50$ kΩ, $C_{ext} = 47$ pF	250	300	350	kHz
C_i	Input capacitance	$V_I = 0$ V, f = 1 kHz		10		pF
$C_{i(\phi)}$	Input capacitance, clock input	$V_I = 0$ V, f = 100 kHz		25		pF

NOTES: 1. Throughout this data sheet supply voltage values are with respect to V_{SS}, unless otherwise noted.
2. Average current is specified over any 100-ms period.
3. Ripple must not exceed 0.3 volts peak-to-peak in the operating frequency range.
4. The algebraic convention where the most-positive (least-negative) limit is designated as maximum is used in this specification for logic voltage levels only.
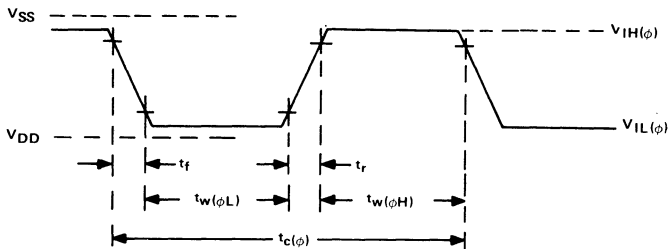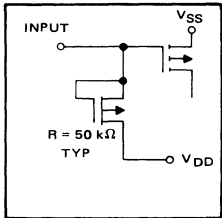
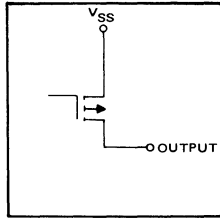NOTE: Timing points are 90% (high) and 10% (low).

FIGURE 11 — EXTERNALLY DRIVEN CLOCK INPUT WAVEFORM

6.6 SCHEMATICS OF INPUTS AND OUTPUTS

**TYPICAL OF ALL K AND I INPUTS**

TYPICAL OF ALL O, R, PC, AND PA OPEN-DRAIN OUTPUTS


6.7 INTERNAL OR EXTERNAL CLOCK

If the internal oscillator is used, OSC1 and OSC2 terminals are shorted together and tied to an external resistor to V_{DD} and a capacitor to V_{SS}. If an external clock is desired, the clock source may be connected to OSC1 and OSC2 shorted to V_{SS}.

CONNECTION FOR INTERNAL OSCILLATOR
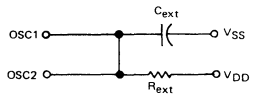
TYPICAL INTERNAL OSCILLATOR FREQUENCY
vs
EXTERNAL RESISTANCE
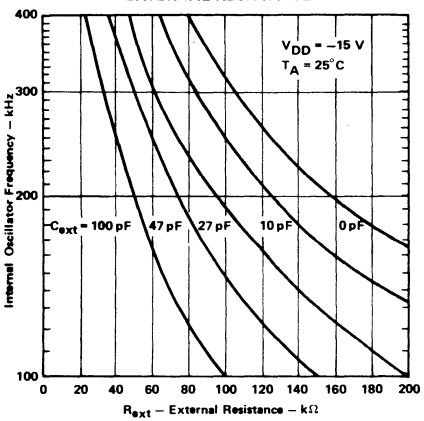
6.8 TERMINAL ASSIGNMENTS

PIN NO.	FUNCTION	PIN NO.	FUNCTION	PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	NC	17	PC4	33	NC	49	NC
2	NC	18	PC3	34	R11*	50	PA0
3	O4	19	PC2	35	R12*	51	NC
4	NC	20	PC1	36	R13*	52	I0
5	O2	21	NC	37	R14*	53	NC
6	NC	22	R3	38	R15*	54	I1
7	O1	23	R4	39	NC	55	NC
8	NC	24	R5	40	V_{DD}	56	I2
9	OSC1	25	NC	41	PA2	57	OSL
10	OSC2	26	NC	42	PA3	58	I3
11	V_{SS}	27	R6	43	K1	59	I4
12	R0	28	R7	44	K2	60	I5
13	R1	29	R8	45	K4	61	I6
14	R2	30	R9	46	K8	62	I7
15	CA, SE-2 (NC, SE-1)	31	R10	47	PA1	63	O8
16	PC5	32	PC0	48	INIT	64	NC

*The user determines which R outputs are appropriate for a specified device emulation. Note the device descriptions.
NC — NO INTERNAL CONNECTION

6.9 TERMINAL FUNCTION DESCRIPTION

1. PC0 → PC5 are the ROM program-counter outputs with PC0 being the most-significant bit and PC5 being the least-significant bit. The addresses change in a non-sequential binary manner.

2. PA0 → PA3 are the ROM page-address outputs with PA0 being the most-significant bit.

3. CA is the ROM chapter address output for the SE-2.

4. I0 → I7 are the external-memory-instruction inputs with I0 being the most-significant bit.

5. O1, O2, O4, O8, and OSL are the data outputs latched in the O register, with O1 being the least-significant bit and OSL being the output of the status latch.

6. K1, K2, K4, and K8 are the data input lines with K1 being the least-significant bit of those inputs.

7. R0 → R15 are the R-output register outputs.

8. V_{DD} is the power-supply input.

9. V_{SS} is the ground pin.

10. OSC1† is the oscillator input if driven by an external clock. OSC1 and OSC2 are shorted together to operate with the internal oscillator. The frequency is controlled by an external RC circuit.

11. OSC2 is the oscillator output.

12. INIT is used for power-on initialization or hardware reset (see the *Programmer's Reference Manual* for more information).

†If an external clock is used, OSC2 is tied to V_{SS}.

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7. HE-2 HARDWARE EVALUATOR

7.1 INTRODUCTION

The HE-2 is a register-level emulator and debugging unit for TMS 1000 series microcomputers. The software simulation provided by time-sharing processing combined with the HE-2 having such features as single-step, repetitive step, breakpoint, RAM inspection, and manual load for instructions make significant improvements in design-cycle time possible. The unit is especially valuable when programs that control mechanical devices or several peripherals must be verified in real time. If problems are encountered in the laboratory, there is no need for immediate reassembly of the code since algorithm changes can be entered manually into the instruction RAM's. RAM's are used for the instruction memory, instruction decoder, and the output decoder. Thus, each programmable portion of the TMS 1000 series devices is modified by a paper-tape input, rather than programming a PROM every time a design change occurs.

Since every day saved in new-product development can represent thousands of dollars, the hardware evaluator will usually pay for itself many times over in the first project.

The HE-2 emulates all microcomputers in the TMS 1000 series. By removing a small PC board, the HE-2 can emulate the TMS 1000, TMS 1200, TMS 1070, or the TMS 1270. Replacing the PC board enables emulation of the TMS 1100 and TMS 1300.

7.2 CONTROLS AND FRONT PANEL

All of the internal status bits, register and RAM contents, and instruction codes are displayed on the front panel. Address and instruction bit switches control the memory inspection and manual entry mode. In the halt mode or with breakpoint, a display select switch allows RAM inspection at any point in the program execution. The step enable allows the designer to cycle through single instructions or through multiple instructions at a 2-Hz to 3-Hz rate.

A complete operation guide is available upon request for review. A manual is shipped with each system purchased.
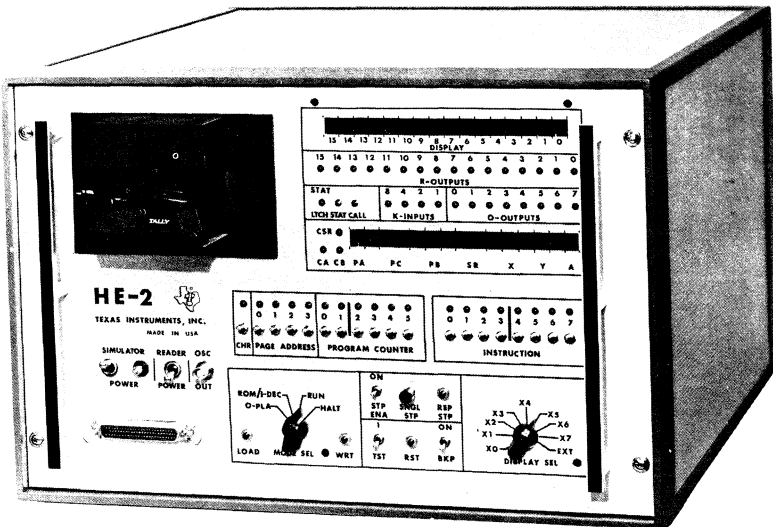
7.3 ELECTRICAL AND MECHANICAL FEATURES

Implementation: MOS and BiPolar

Space Requirements: 19 1/2'' wide X 13'' high X 25 1/4'' deep

Paper Tape Reader: Front panel mounted (50 characters per second)

Power Requirements: 120 V ac, 2 amperes, 50 to 60 Hz

Cooling: Self contained, rear of chassis

Connector: Amphenol #57-20500 female

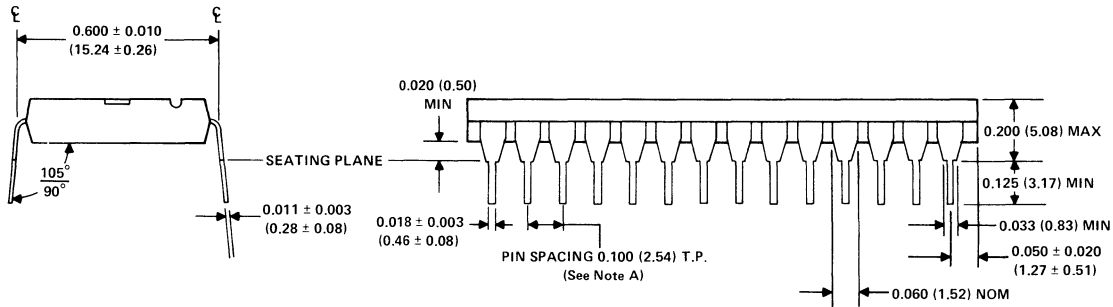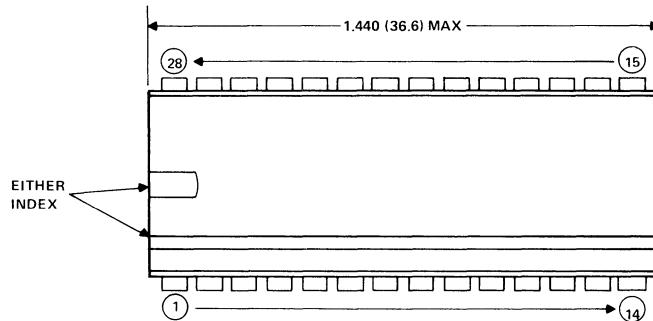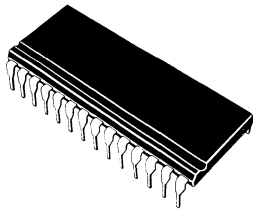Self-Contained Oscillator: 100 kHz to 400 kHz, adjustable.

7.4 CONNECTOR PIN ASSIGNMENTS

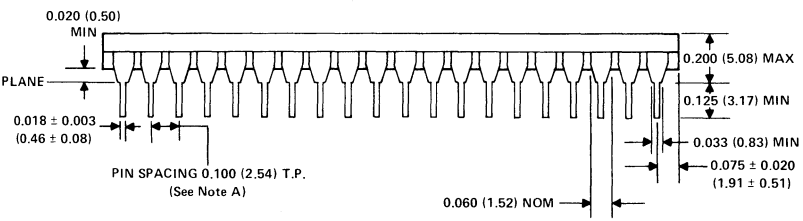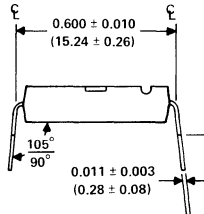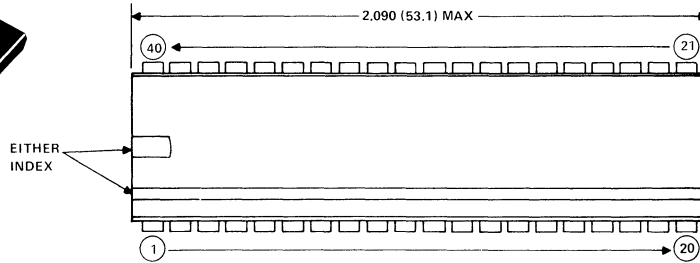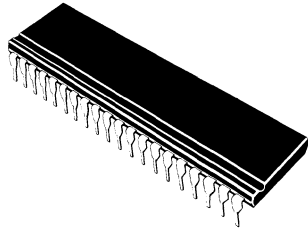| PIN NO.	FUNCTION	PIN NO.	FUNCTION
1	R0	26	K2
2	R1	27	K4
3	R2	28	K8
4	R3	29	INIT
5	R4	30	NC
6	R5	31	NC
7	R6	32	NC
8	R7	33	NC
9	R8	34	NC
10	R9	35	NC
11	R10	36	NC
12	R11	37	NC
13	R12	38	NC
14	R13	39	NC
15	R14	40	NC
17	R15	41	NC
17	O0	42	NC
18	O1	43	NC
19	O2	44	GND
20	O3	45	GND
21	O4	46	GND
22	O5	47	NC
23	O6	48	+5 V
24	O7	49	+5 V } 1A maximum
25	K1	50	+5 V

NOTE: The R and O outputs have standard push-pull TTL outputs. Each K input uses an emitter-follower input buffer with a five-volt power supply.
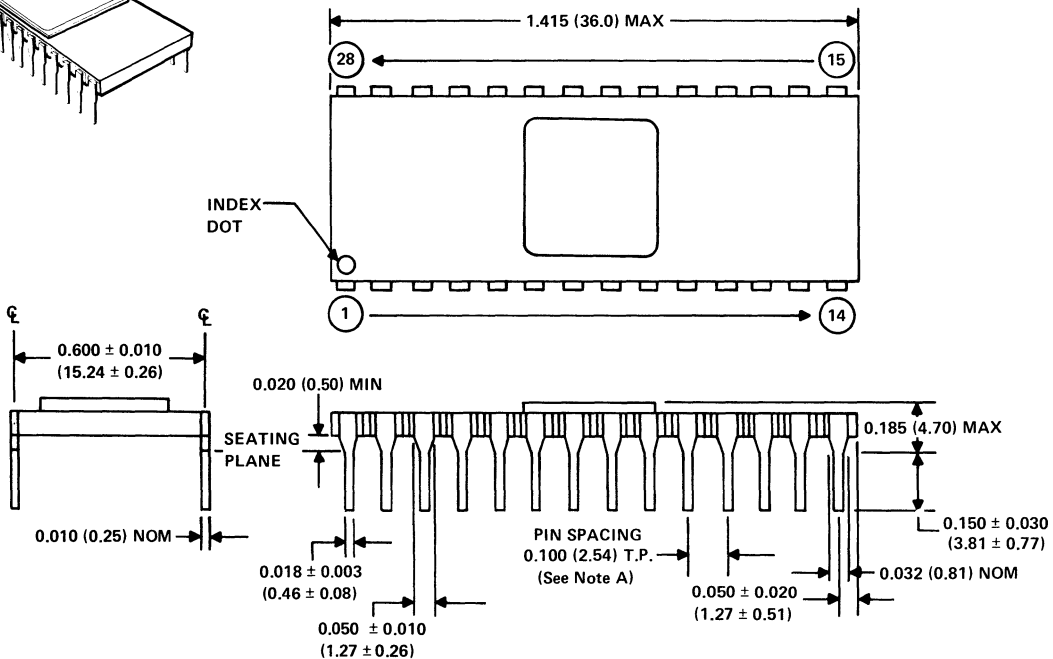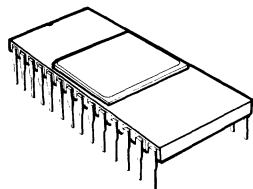
1.440 (36.6) MAX

28   15

EITHER INDEX

1   14

0.600 ± 0.010
(15.24 ± 0.26)

0.020 (0.50) MIN

0.200 (5.08) MAX

SEATING PLANE

0.125 (3.17) MIN

105°
90°

0.011 ± 0.003
(0.28 ± 0.08)

0.018 ± 0.003
(0.46 ± 0.08)

0.033 (0.83) MIN

0.050 ± 0.020
(1.27 ± 0.51)

PIN SPACING 0.100 (2.54) T.P.
(See Note A)

0.060 (1.52) NOM

NOTES: a. Each pin centerline is located within 0.010 inch (0.26 millimeters) of its true longitudinal position.
           b. All linear dimensions are shown in inches (and parenthetically in millimeters for reference only). Inch dimensions govern.

2.090 (53.1) MAX

40

21

1

20

EITHER
INDEX

0.600 ± 0.010
(15.24 ± 0.26)

0.020 (0.50)
MIN

0.200 (5.08) MAX

0.125 (3.17) MIN

— SEATING PLANE —

105°
90°

0.033 (0.83) MIN

0.011 ± 0.003
(0.28 ± 0.08)

0.018 ± 0.003
(0.46 ± 0.08)

0.075 ± 0.020
(1.91 ± 0.51)

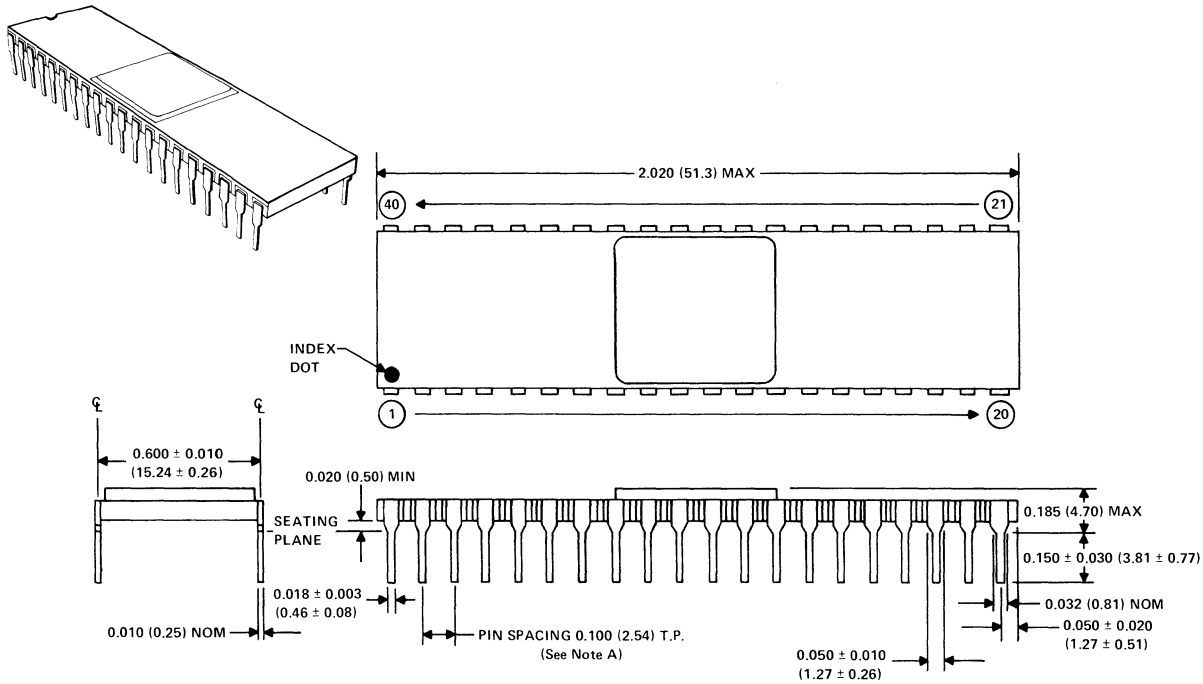PIN SPACING 0.100 (2.54) T.P.
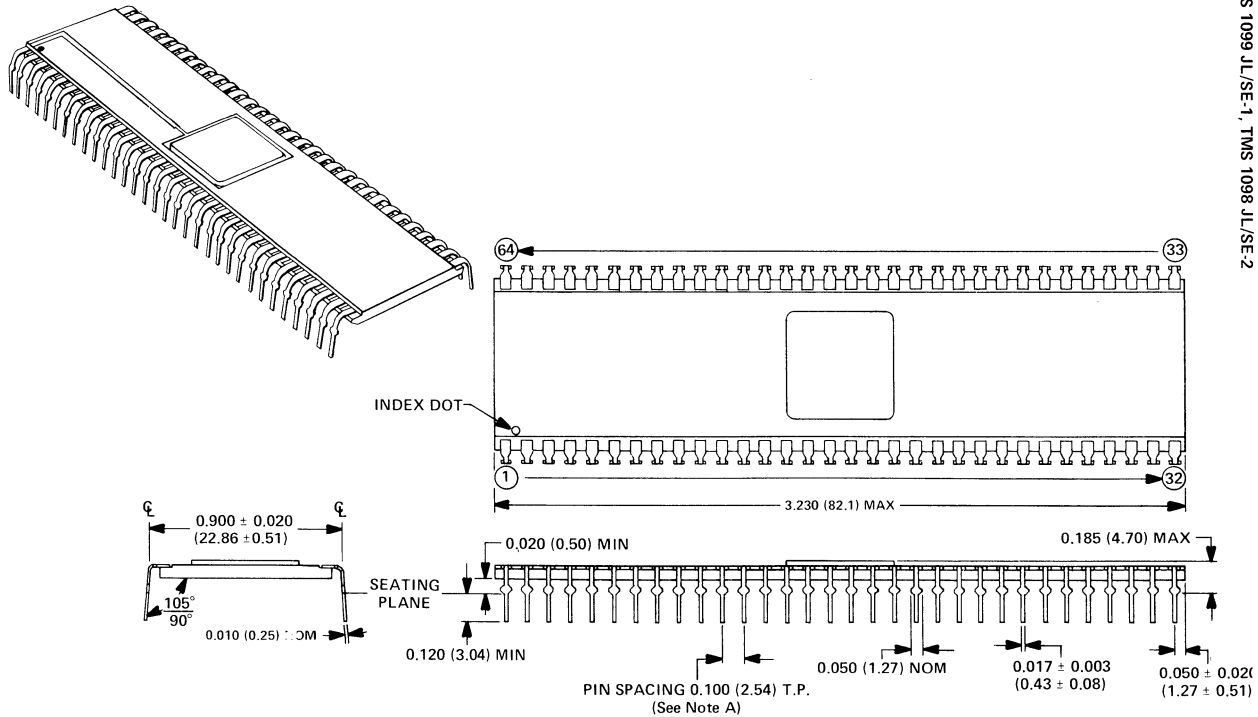(See Note A)

0.060 (1.52) NOM

NOTES: a. Each pin centerline is located within 0.010 inch (0.26 millimeters) of its true longitudinal position.
         b. All linear dimensions are shown in inches (and parenthetically in millimeters for reference only). Inch dimensions govern.

1.415 (36.0) MAX

28

15

INDEX DOT

1

14

C̗L   C̗L

0.600 ± 0.010
(15.24 ± 0.26)

0.020 (0.50) MIN

SEATING PLANE

0.010 (0.25) NOM

0.018 ± 0.003
(0.46 ± 0.08)

0.050 ± 0.010
(1.27 ± 0.26)

PIN SPACING
0.100 (2.54) T.P.
(See Note A)

0.050 ± 0.020
(1.27 ± 0.51)

0.185 (4.70) MAX

0.150 ± 0.030
(3.81 ± 0.77)

0.032 (0.81) NOM

NOTES: a. Each pin centerline is located within 0.010 inch (0.26 millimeters) of its true longitudinal position.
              b. All linear dimensions are shown in inches (and parenthetically in millimeters for reference only). Inch dimensions govern.

2.020 (51.3) MAX

40

21

INDEX DOT

1

20

0.600 ± 0.010
(15.24 ± 0.26)

0.020 (0.50) MIN

SEATING PLANE

0.185 (4.70) MAX

0.150 ± 0.030 (3.81 ± 0.77)

0.018 ± 0.003
(0.46 ± 0.08)

0.032 (0.81) NOM

0.010 (0.25) NOM

0.050 ± 0.020
(1.27 ± 0.51)

PIN SPACING 0.100 (2.54) T.P.
(See Note A)

0.050 ± 0.010
(1.27 ± 0.26)

NOTES: a. Each pin centerline is located within 0.010 inch (0.26 millimeters) of its true longitudinal position.
b. All linear dimensions are shown in inches (and parenthetically in millimeters for reference only). Inch dimensions govern.

64   33

INDEX DOT

1   32

3.230 (82.1) MAX

0.900 ± 0.020
(22.86 ±0.51)

105°
90°

0.010 (0.25) NOM

SEATING
PLANE

0.020 (0.50) MIN

0.185 (4.70) MAX

0.120 (3.04) MIN

PIN SPACING 0.100 (2.54) T.P.
(See Note A)

0.050 (1.27) NOM

0.017 ± 0.003
(0.43 ± 0.08)

0.050 ± 0.020
(1.27 ± 0.51)

NOTES: a. Each pin centerline is located within 0.010 inch (0.26 millimeters) of its true longitudinal position.
          b. All linear dimensions are shown in inches (and parenthetically in millimeters for reference only). Inch dimensions govern.