TEXAS INSTRUMENTS

1000

TMS 2100, TMS 2170, TMS 2300, TMS 2370
4-Bit Microcomputers

μC™ MICROCOMPUTER SERIES™

Preliminary Data Manual

1.

2.

3.

4.

5.

APP

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1. INTRODUCTION

1.1 DESCRIPTION

The TMS 2100/2300 and TMS 2170/2370 microcomputers are new enhanced members of the TMS 1000 family. Through greater on-chip integration of system functions, the TMS 2100 series provides more efficient and cost-effective solutions to a variety of controller applications (see Table 1).

TABLE 1 – TMS 2100 MICROCOMPUTER SERIES FEATURES†

FEATURES	TMS 2100	TMS 2300	TMS 2170	TMS 2370
Maximum-Rated Voltage (O, R, K, J, INT, and ECI)	–15 V	–15 V	–35 V	–35 V
Package Pin Count	28 Pins	40 Pins	28 Pins	40 Pins
"R" Individually Addressed Output Latches	7	15	6	14
K, J and R Inputs	8	12	8	12
Analog Inputs	1	2	1	2
Event Counter	No	Yes	No	Yes
Interval Timer	Yes			
Instruction Read Only Memory	2048 X 8 Bits (16,384 Bits)			
Data Random Access Memory	128 X 4 Bits (512 Bits)			
"O" Parallel Latched Data Outputs	8			
Working Registers	3 (4 Bits each)			
Instruction Set	Enhanced TMS 1100 Instruction Set			
Programmable O Output Decoder	Yes (32 AND terms)			
On-Chip Oscillator	Yes			
Power Supply/Typical Dissipation	–9 V/90 mW			
Development System	AMPL1000 2100			
System Evaluator Device with External Instruction Memory	SE-2100 (TMS 1096 JLL)			
Subroutine Levels	4 Levels			
8-Bit A/D Converter	Yes			
Hardware Interrupt (1 level) or Zero Cross Detector	Yes (Mask Option)			
Frequency Divider to K8	Yes (Optional ÷ Pass, 1/2, 1/10 and 1/20)			

1.2 DESIGN SUPPORT

TI provides design support for the entire TMS 1000 family

- System evaluators with an external EPROM‡
- AMPL development systems for program development
- Field application specialists nationwide for local assistance
- Regional Technology Centers

A staff of experienced application programmers is available at Texas Instruments to assist customers in evaluating applications, in training designers to program the TMS 1000 series, and in simulating programs. TI will also contract to write programs to customer's specifications. (See Figure 1.)

†See Appendix A for TMS 2400 Series

‡See Appendix B for evaluator data.

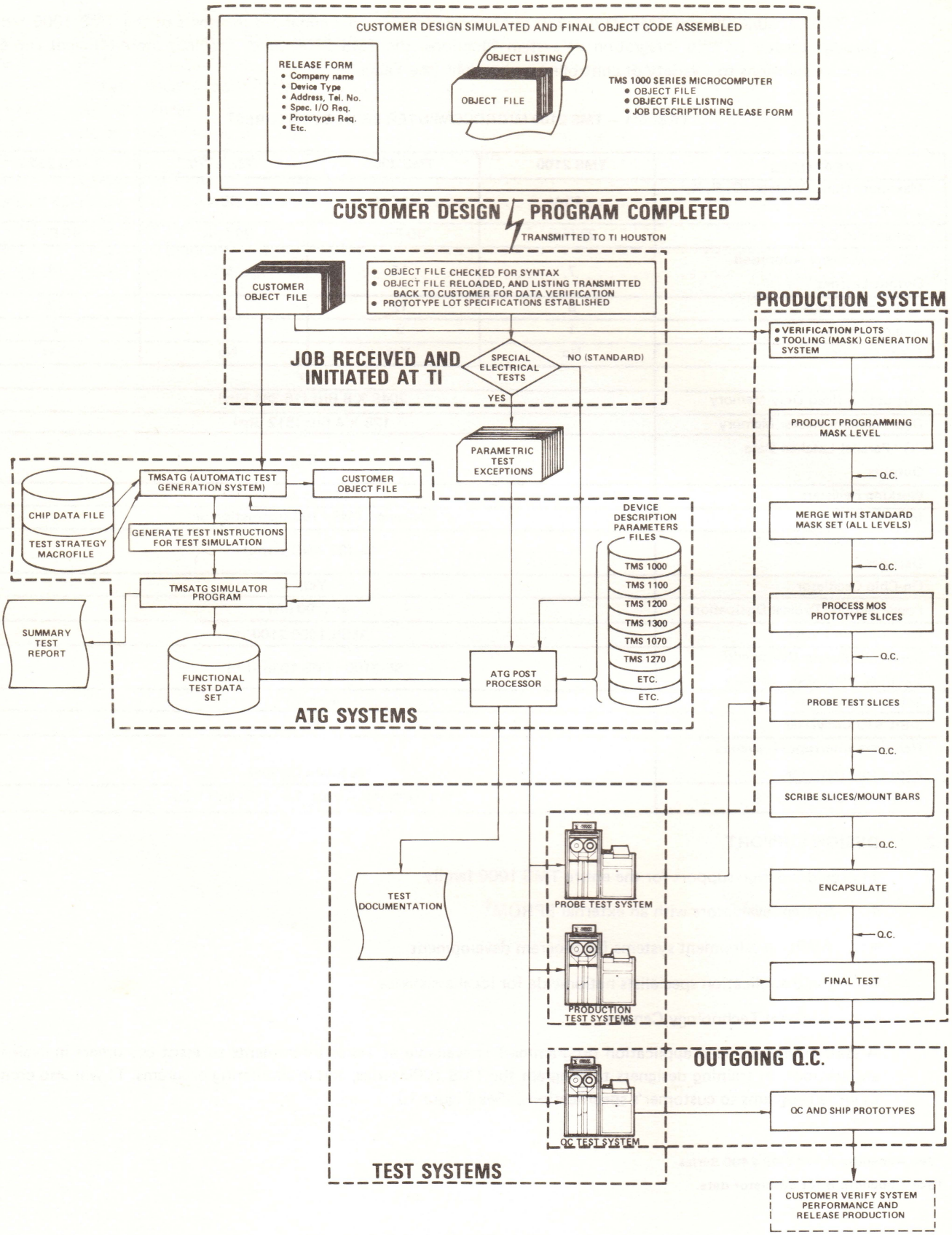


FIGURE 1 – MICROCOMPUTER DESIGN RELEASE TO PRODUCTION

2. DEVICE HARDWARE OPERATION

2.1 OVERVIEW

The microcomputer ROM program controls data input, storage, processing, and output. Data processing takes place in the arithmetic logic unit (ALU). K and J-inputs are sent to the ALU, as shown in Figure 2, and are stored in the four-bit accumulator. The accumulator output accesses the O-output latches, the RAM storage cells, Accumulator 2, the X register, and the adder input. Data storage in the 512-bit RAM is organized into 128 words, four bits per word. The four-bit words are conveniently grouped into eight 16-word files addressed by a three-bit register. A four-bit Y register addresses one of the 16 words in a file.

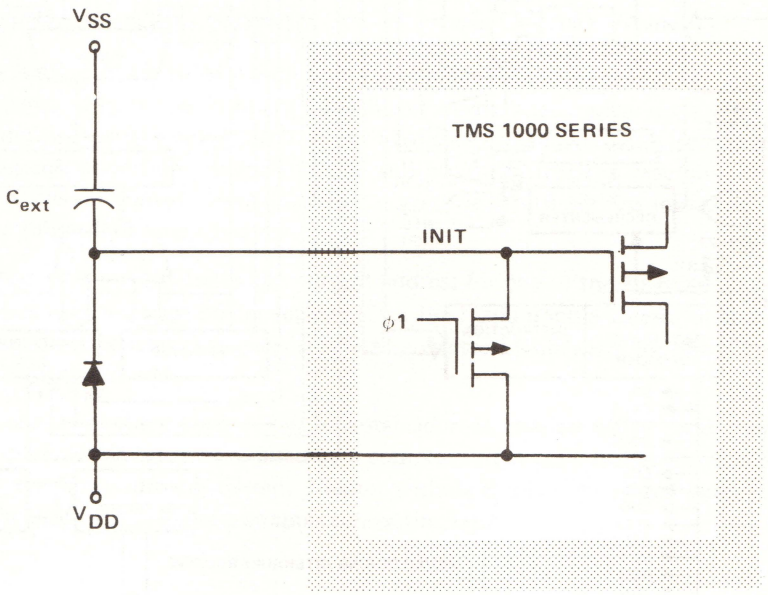
The O-outputs and the R-outputs are the output channels. The eight parallel O-outputs are decoded from five data latches. The O-output decoder is a programmable logic array (PLA) that is modified by changing the gate level mask tooling. Each of the R-outputs has a storage element that can be individually set or reset by program control. The R-outputs send status or enable signals to external devices. The R-outputs strobe the O-outputs to displays†, to other TMS 1000 family devices, or to other interface circuitry. The same R-outputs may be used to multiplex data into the K or J-inputs whenever necessary.

2.2 TIMING RELATIONSHIPS

Six oscillator pulses constitute one instruction cycle. All instructions are executed in one instruction cycle. The actual machine cycle period is determined by either a fixed external resistor and capacitor connected to the OSC1 and OSC2 pins (refer to Section 2.4), or an external clock input frequency.

2.3 POWER-ON

The TMS 1000 family has a built-in power-on latch (see below), which resets the program counter upon the proper application of power (with INIT input open or tied to V_{DD}). After power-up the chip resets and begins execution at a fixed ROM address. The system reset depends on the ROM program after the starting address. For power supplies with slow rise times or noisy conditions, the following network connected to the INIT pin may be necessary. To assist initialization of the TMS 1000 family devices, a capacitor maintains a high-level voltage on the INIT input after the power supply settles. The diode connecting V_{DD} to INIT is used to fully discharge C_{ext} and allow a proper reset when fast power-on-off-on cycles are expected.



$C_{ext}(\mu F)$ = 0.06 Power Supply Rise Time (ms)

† R0-R3 may also be used as a four-bit parallel input/output port.

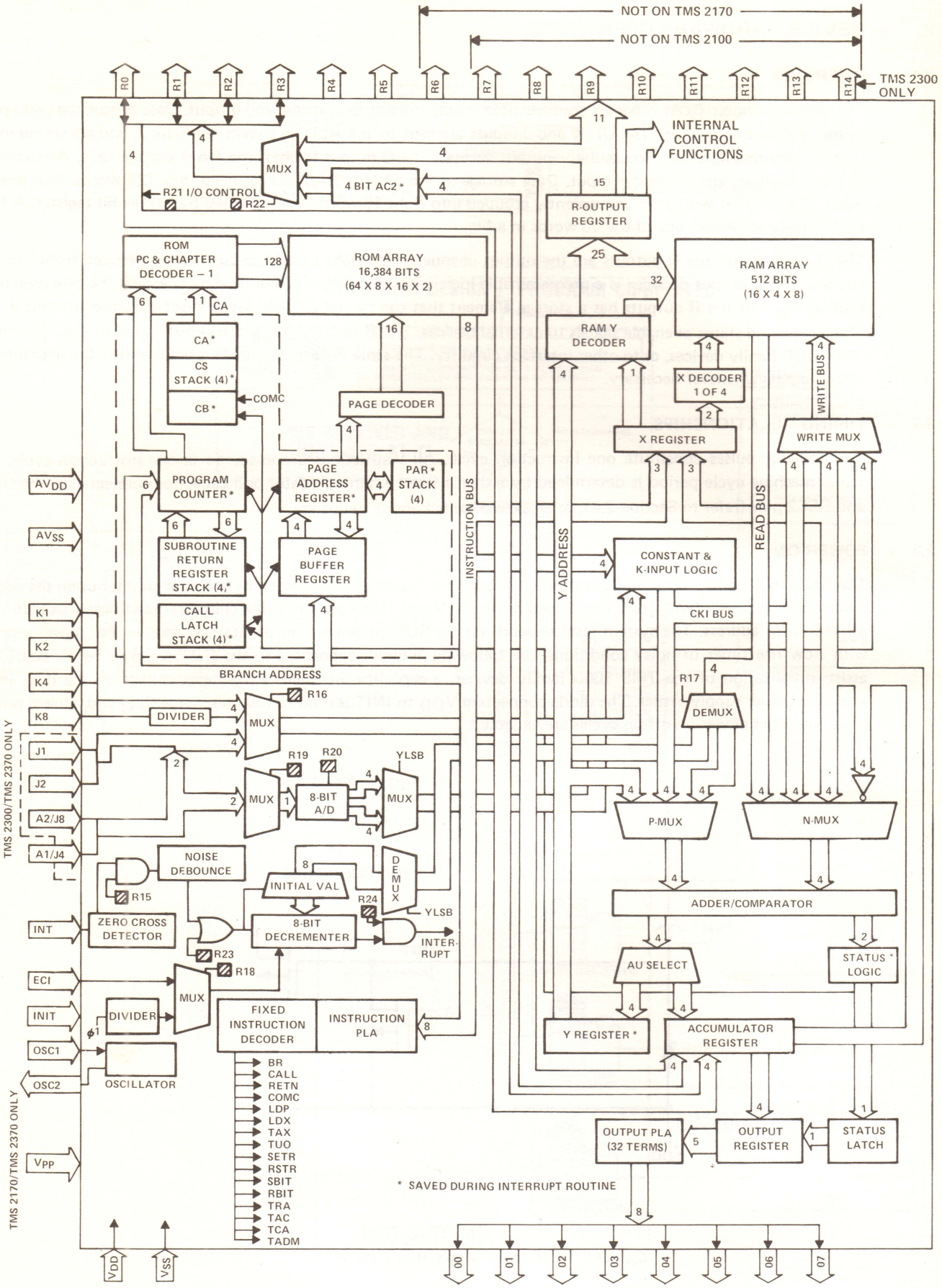
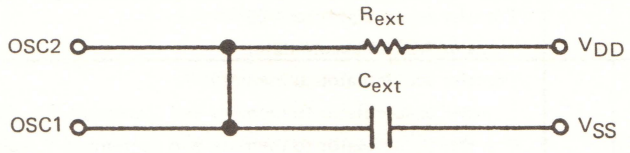


FIGURE 2 – TMS 2100 TENTATIVE BLOCK DIAGRAM

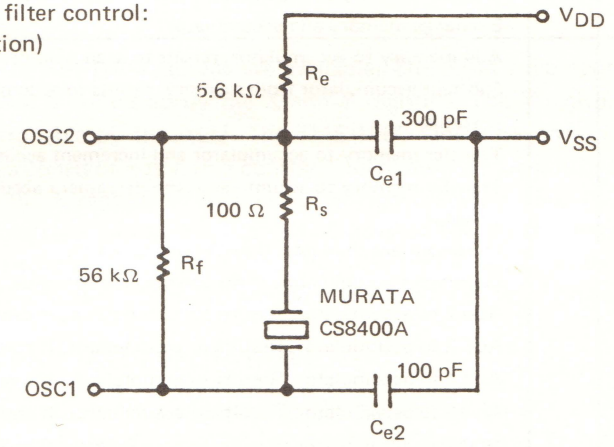
2.4 ON-CHIP OSCILLATOR

The internal oscillator for the TMS 2100/TMS 2300 is similar to the TMS 1100/TMS 1300 oscillator, except that it has been designed to be driven not only with an RC filter, but also with a ceramic filter or an external clock. The following diagrams show the appropriate connections for each method of oscillator control:

(1) R-C filter control:



(2) Ceramic or crystal filter control: (typical configuration)



If an external clock is desired, the clock source may be connected to OSC1, and OSC2 shorted to V_{SS}.

2.5 ROM ORGANIZATION/CHAPTER CONTROL

The sequence of the 2048 eight-bit ROM instructions determines the device operation. The instruction ROM contains two chapters of 16 pages each. A page contains 64 eight-bit words. After power-up, the program execution starts at a fixed instruction address, CH:O;PA:F;PC:OO. A shift-register program counter sequentially addresses each ROM instruction on a page. A conditional branch or call subroutine instruction may alter the six-bit program counter address to transfer software control. Four levels of subroutine return address including one for interrupt, if used, may be stored in the subroutine return register.

The page address register (four bit) holds the current address for one of the 16 ROM pages. To change pages, a constant from ROM loads into the page buffer register (four bits), and upon a successful branch or call, the page buffer loads into the page address register. The page subroutine register, which is a four-level stack, holds the return page address in the call subroutine mode.

The chapter logic consists of three control bits, chapter address, chapter buffer, and chapter subroutine with four level stack. The chapter buffer bit is controlled by a complement chapter buffer instruction (see COMC in Table 2). The chapter buffer transfers into the current chapter address if a branch or call executes successfully. If a call is successful, the return chapter is saved in a chapter subroutine latch.

TABLE 2 – TMS 2100 STANDARD INSTRUCTION SET

FUNCTION	MNEMONIC	STATUS EFFECT		DESCRIPTION
		C	N	
Register-to-Register Transfer	TAY			Transfer accumulator to Y register
	TYA			Transfer Y register to accumulator
	CLA			Clear accumulator
	TAC			Transfer accumulator to AC2
	TCA			Transfer AC2 to accumulator
Register-to-Memory	TAM			Transfer accumulator to memory
	TAMIYC	Y		Transfer accumulator to memory and increment Y register. If carry, one to status.
	TAMDYN	Y		Transfer accumulator to memory and decrement Y register. If no borrow, one to status.
	TADM			Transfer A/D register to memory.
Memory-to-Register	TMY			Transfer memory to Y register
	TMA			Transfer memory to accumulator (R17 = 0), to initial value Reg. (R17 = 1).
	XMA			Exchange memory and accumulator
Arithmetic	AMAAC	Y		Add memory to accumulator, results to accumulator. If carry, one to status.
	SAMAN	Y		Subtract accumulator from memory, results to accumulator. If no borrow, one to status.
	IMAC	Y		Transfer memory to accumulator and increment accumulator. If carry, one to status.
	DMAN	Y		Transfer memory to accumulator and decrement accumulator. If no borrow, one to status.
	IAC	Y		Increment accumulator. If carry, one to status.
	DAN	Y		Decrement accumulator. If no borrow, one to status.
	A2AAC	Y		Add 2 to accumulator. Results to accumulator. If carry, one to status.
	A3AAC	Y		Add 3 to accumulator. Results to accumulator. If carry, one to status.
	A4AAC	Y		Add 4 to accumulator. Results to accumulator. If carry, one to status.
	A5AAC	Y		Add 5 to accumulator. Results to accumulator. If carry, one to status.
	A6AAC	Y		Add 6 to accumulator. Results to accumulator. If carry, one to status.
	A7AAC	Y		Add 7 to accumulator. Results to accumulator. If carry, one to status.
	A8AAC	Y		Add 8 to accumulator. Results to accumulator. If carry, one to status.
	A9AAC	Y		Add 9 to accumulator. Results to accumulator. If carry, one to status.
	A10AAC	Y		Add 10 to accumulator. Results to accumulator. If carry, one to status.
	A11AAC	Y		Add 11 to accumulator. Results to accumulator. If carry, one to status.
	A12AAC	Y		Add 12 to accumulator. Results to accumulator. If carry, one to status.
	IYC	Y		Increment Y register. If carry, one to status.
	DYN	Y		Decrement Y register. If no borrow, one to status.
	CPAIZ	Y		Complement accumulator and increment. If then zero, one to status.
Arithmetic Compare	ALEM	Y		If accumulator less than or equal to memory, one to status.
Logical Compare	MNEA		Y	If memory is not equal to accumulator, one to status.
	MNEZ		Y	If memory not equal to zero, one to status.
	YNEA		Y	If Y register not equal to accumulator, one to status and status latch.
	YNEC		Y	If Y register not equal to a constant, one to status.
Bits in Memory	SBIT			Set memory bit
	RBIT			Reset memory bit
	TBIT1		Y	Test memory bit. If equal to one, one to status.
Constants	TCY			Transfer constant to Y register
	TCMIY			Transfer constant to memory, then increment Y
Input	TKA			Transfer K or J inputs to accumulator
	TRA			Transfer R inputs to accumulator

TABLE 2 – TMS 2100 STANDARD INSTRUCTION SET (Concluded)

FUNCTION	MNEMONIC	STATUS EFFECT		DESCRIPTION
		C	N	
Output	SETR			Set R output addressed by Y
	RSTR			Reset R output addressed by Y
	TDO			Transfer data from accumulator and status latch to O outputs
RAM X Addressing	LDX			Load X with file address
	TAX			Transfer accumulator (A1, A2, A4) to X register.
ROM Addressing	BR			Branch on status = one
	CALL			Call subroutine on status = one
	RETN			Return from subroutine (No-op if not in subroutine)
	LDP			Load page buffer with constant
	COMC			Complement Chapter Buffer

2.6 RAM OPERATION

Up to 512 addressable bits of RAM storage are available. The RAM is composed of eight files, each containing 16 four-bit words. The RAM is addressed by the X and Y registers. The Y register selects one of the 16 words in a file and is completely controllable by the ALU. The TMS 1000 family has instructions within the standard instruction set that compare Y to a constant, set Y to a constant, increment or decrement Y, and/or perform data transfer to or from Y. Three bits in the X register select one of the eight 16-word files. The X register is set to a constant or is loaded from the accumulator. A four-bit data word goes to the RAM location addressed by X and Y from the accumulator or from the constants in the ROM. The RAM output words go to the ALU and can be operated on and loaded into Y or the accumulator in one instruction interval. Any selected bit in the RAM can be set, reset, or tested.

2.7 ARITHMETIC LOGIC UNIT (ALU) OPERATION

Arithmetic and logic operations are performed by the four-bit adder and associated logic. The ALU performs logic comparison, arithmetic comparison, and add and subtract functions. The ALU and interconnects are shown in Figure 3. The operations are performed on two sets of inputs, P and N. The two four-bit parallel inputs may be added together or logically compared. The accumulator has an inverted output to the N-selector for subtraction by two's complement arithmetic. The other N-inputs are from the true output of the accumulator, the RAM, the ROM instruction constants, and the K-inputs. The P-inputs come from the Y register, the RAM, the constants, and the K-inputs.

Addition and subtraction results are stored in either the Y register or the accumulator. An arithmetic function may cause a carry output to the status logic. Logical comparison may generate an output to status. If the comparison functions are used, only the status bit affects the program control, and neither the Y register nor the accumulator register contents are affected. If the status feedback is a logic one, which is the normal state, then the conditional branch or call is executed successfully. If an instruction calls for a carry output to status and the carry does not occur, then status will go to a zero state for one instruction cycle. Likewise, if an instruction calls for the logical-comparison function and the bits compared are equal, then status will go to a zero state for one instruction cycle. If status is a logic zero, then branches and calls immediately following the status-affecting instruction are not performed.

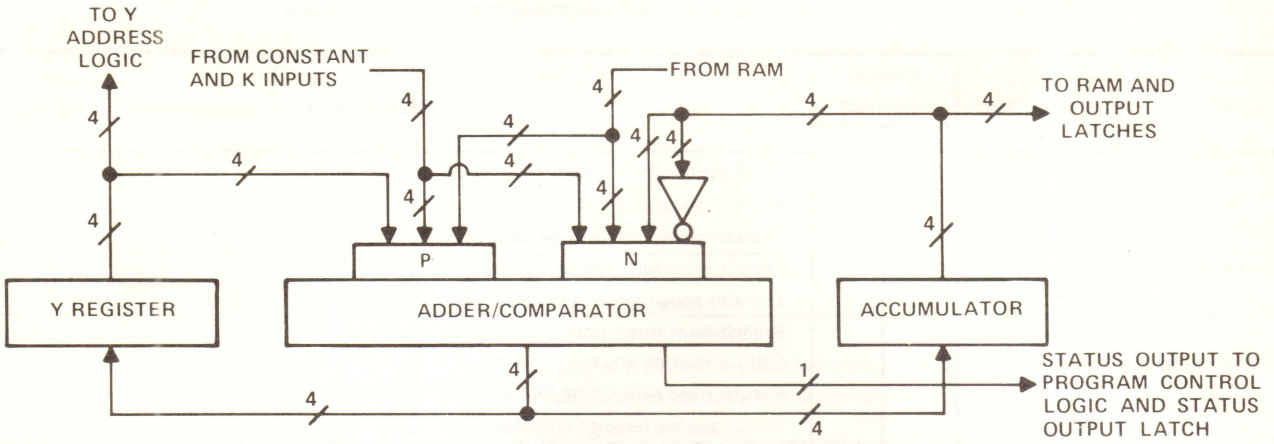


FIGURE 3 – ARITHMETIC LOGIC UNIT (ALU)

2.8 DIGITAL INPUT

2.8.1 TMS 2100/TMS 2170 Digital Inputs

There are eight data inputs to the TMS 2100/TMS 2170 circuit: K1, K2, K4 and K8 and R0, R1, R2, R3. Each time an input word is requested, the data path from the K-inputs is enabled to the adder, and the data is stored in the accumulator for future use. The R-outputs usually multiplex inputs such as keys and other data onto the K-input lines. Data can be stored periodically in synchronization with the predetermined rate of an external device. Thus, multiple four-bit words can be requested and stored with only one R-output supplying the control signal.

The input function of R0, R1, R2, R3 is explained in Section 2.13.

2.8.2 TMS 2300/TMS 2370 Digital Inputs

The TMS 2300/TMS 2370 have 12 data inputs: K1, K2, K4, K8 and J1, J2, J4, J8 and R0, R1, R2, R3. The K and J ports are multiplexed internally into a four-bit input bus with selection being under program control of R16.

2.9 K8 FREQUENCY DIVIDER

A frequency divider has been incorporated into the K8 input. Any one of four options (K8 pass, divided by 2, 10 or 20) can be defined during device manufacture. The divider count is reset when the INIT signal goes to a high level.

2.10 ANALOG INPUT

To provide interface to analog signals the TMS 2100/TMS 2170 has analog input A1, which is monitored by the on-board analog to digital converter (see Figure 4). The TMS 2300/TMS 2370 have two analog inputs, A1 and A2, that share device pins with inputs J4 and J8. Selection of A1 or A2 is under ROM program control of R19.

FIGURE 4 — K/J AND ANALOG INPUT PORTS

2.11 DATA OUTPUT

The TMS 2100 series devices have two types of output channels, the R-outputs and the O-outputs, each of which have multiple purposes. The R-outputs are addressed by the Y-register, and each output can be individually set or reset. The eight parallel O-outputs come from a five-bit-to-eight-bit code converter, the O-output PLA.

2.11.1 R-Data Output

There are seven R-outputs for the TMS 2100, six for the TMS 2170, 15 for the TMS 2300 and 14 for the TMS 2370. The R-outputs are addressed by the Y-register and decoded by the RAM Y-decoder.

2.11.2 O-Data Output

The internally latched eight parallel O-outputs may be used for a wide variety of applications: driving displays, driving speakers, communicating with external memories or processors, and a host of other functions. The user defines a 5-bit-to-8-bit converter called the O-output PLA, which specifies the state of the O-lines for a given input. The four bits of the accumulator and the output of the status latch provide for 32 unique eight-bit patterns.

2.12 INTERNAL CONTROL FUNCTIONS

The MSB of the X register is used to enable addressing of the internal control functions R16 through R24 (see Table 3).

TABLE 3 – CONTROL FUNCTIONS

FUNCTION	DEFINITION	HIGH	LOW
R15	External interrupt	Enable	Disable
R16	K/J select	J-input	K-input
R17	Initial value load	Down load	Disable
R18	Ext/Int counter clock control	External	Internal
R19	A1/A2 select	A2 input	A1 input
R20	A/D enable	Enable	Disable
R21	R0-R3 I/O control	Input	Output
R22	ACC2/R0-R3 output select	ACC2	R0-R3
R23	Decrementer load enable	Down load	Disable
R24	Interrupt disable	Enable	Disable

2.13 ANALOG TO DIGITAL CONVERTER (SEE FIGURE 5)

The analog-to-digital converter is a complete hardware successive approximation converter that can be set to continuously convert the input signal A1 or A2, with the digital result being monitored via software control. Conversion time for eight-bit resolution is 200 microseconds.

The following specifications apply to the A/D converter:

1) 2 analog inputs (1 only on 2100/2170)
2) Input range: $AV_{SS} \sim AV_{DD}$
3) Successive approximation: 200 μs sample time
4) 8-bit resolution (with 7-bit accuracy)

R19	OPERATION
0	A1 input to A/D converter
1	A2 input to A/D converter

Reference voltage is provided from AV_{SS}, AV_{DD} input pins. A/D converter function can be implemented as follows:

1) SET/RESET R19 to select input port
2) *SET R20 to start analog input conversion
3) SET RAM address (can be preset)
4) SET YLSB 1 to select upper half of A/D reg.
5) *RESET R20
6) Execute TADM to store converted results to RAM
7) Increment or decrement Y to select the lower half of A/D and address next RAM location.
8) Execute TADM

* At least 8 instruction cycles should be performed between (2) ~ (5).

NOTES: 1. A/D converter will continue to convert next signal unless R20 is RESET.
2. No output operation TDO, SETR, RSTR, etc.) is recommended during (2) ~ (5).

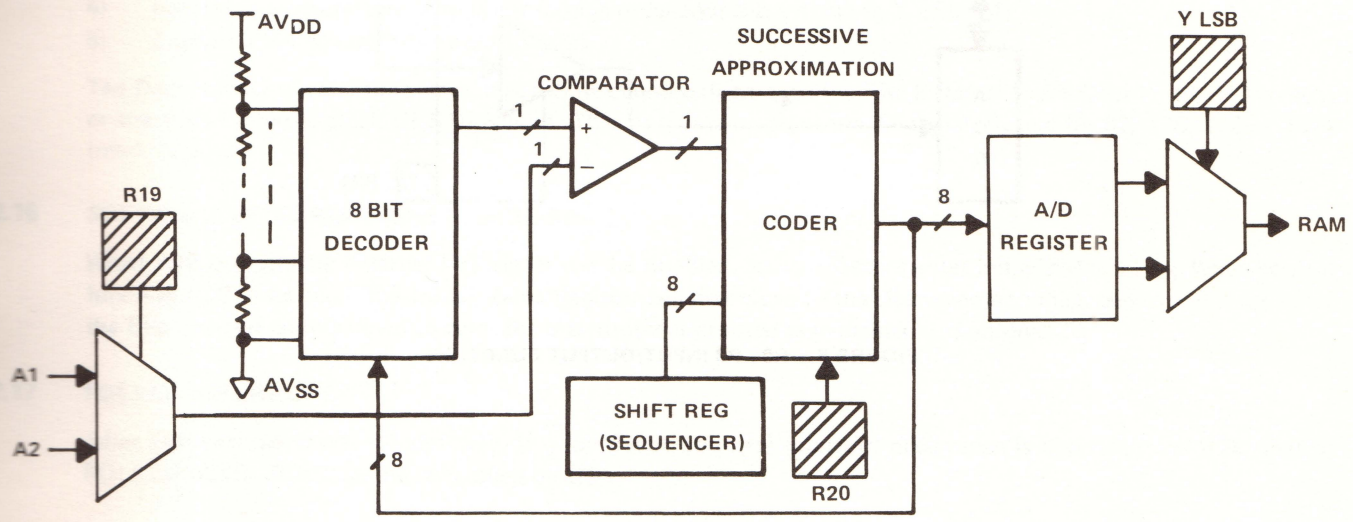


FIGURE 5 – A/D CONVERTER

2.14 INPUT/OUTPUT PORT

Four R-output lines R0, R1, R2, R3 can function as a four-bit bidirectional input/output port for data transfers, such as to or from an external data memory. The operation of this port is regulated by control functions R21 and R22 as shown in Figure 6. If R21 is set, then R0-R3 is an input port, and execution of the TRA instruction transfers data to the accumulator. If R21 is reset, then R0-R3 is an output port with data coming from AC2 (R22 = 1) or the R-output latches (R22 = 0).

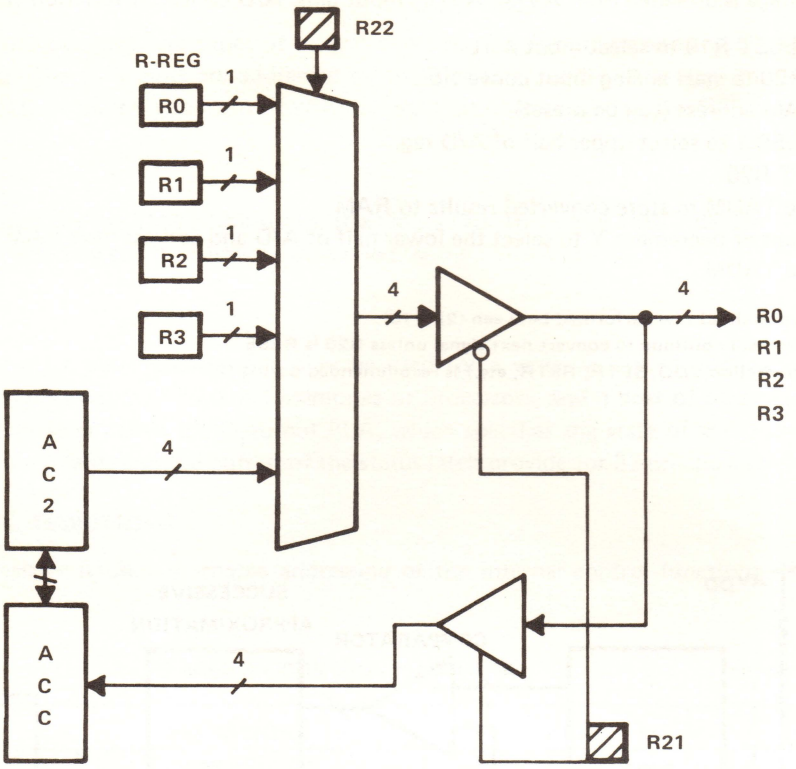


FIGURE 6 – R0 - R3 INPUT/OUTPUT FUNCTION

CONTROL FUNCTION

R21	R22	OPERATION
0	0	R0 ~ R3 from R-output Reg. is selected to output from R0 ~ R3
0	1	AC-2 register is selected to output from R0 ~ R3
1	don't care	Select R0 ~ R3 functions as a 4-bit input to accumulator

INSTRUCTION

TRA	Transfer R0 ~ R3 into accumulator
TAC	Transfer accumulator into AC2
TCA	Transfer AC2 into accumulator

2.15 HARDWARE INTERRUPT (SEE FIGURES 7 AND 8)

The control function R15 must be high to enable an external interrupt. When the INT signal goes from low (V_{DD}) to high (V_{SS}), and this pulse is wider than the specified noise debounce (mask option), then the Initial Value Register is downloaded to the Decrementer, which starts counting. After the Decrementer counts down to zero, the following conditions must be satisfied before an interrupt routine will be executed:

1) Control function R24 must be high.
2) The prior interrupt routine must be complete.
3) The present instruction is not CALL, BR or RETN.

Until all three conditions are met, normal program execution will continue. When they are satisfied, the program will jump to CA = 0, PA = 0, PC = 00 and begin the interrupt routine. This routine is terminated by a RETN instruction.

To load the eight-bit Initial Value Register from RAM requires the following sequence:

1) Set control function R17 high.
2) Point to RAM location where low order four-bits are stored (Y even).
3) Execute TMA to load low order four-bits.
4) Increment or decrement Y to point to high order four-bits (Y odd so Y LSB = 1).
5) Execute TMA to load high order four-bits.

The Decrementer is a real-time clock that can be counted down by either the External Event Counter (if R18 is high) or the scaled internal clock (if R18 is low). This clock comes from the $\phi 1$ signal divided by 32, 128, 256 or 1024 (mask option).

2.16 SOFTWARE INTERRUPT (SEE FIGURE 9)

When R15 is reset, the external INT signal will be disabled, and the Decrementer initialized to FF_{16}. When control function R23 is set high, the Initial Value Register will download to the Decrementer, which begins counting. After the Decrementer counts down to zero, the interrupt will proceed as explained in Section 2.15.

2.17 POLLED INTERRUPT

After Decrementer count reaches zero, (e.g. by Event Counter) interrupt occurrence is dependent on R24, that is, POLLED INTERRUPT can be controlled by R24.

NOTES:
1. After power up, all R-outputs are reset to LOW.
2. While Decrementer is counting, download by next hardware interrupt is forbidden by hardware.
3. It is not recommended to use hardware and software interrupts simultaneously.
4. Since no multilevel interrupt is allowed, it is recommended to disable external interrupt by RESET R15 at the beginning of interrupt routine.

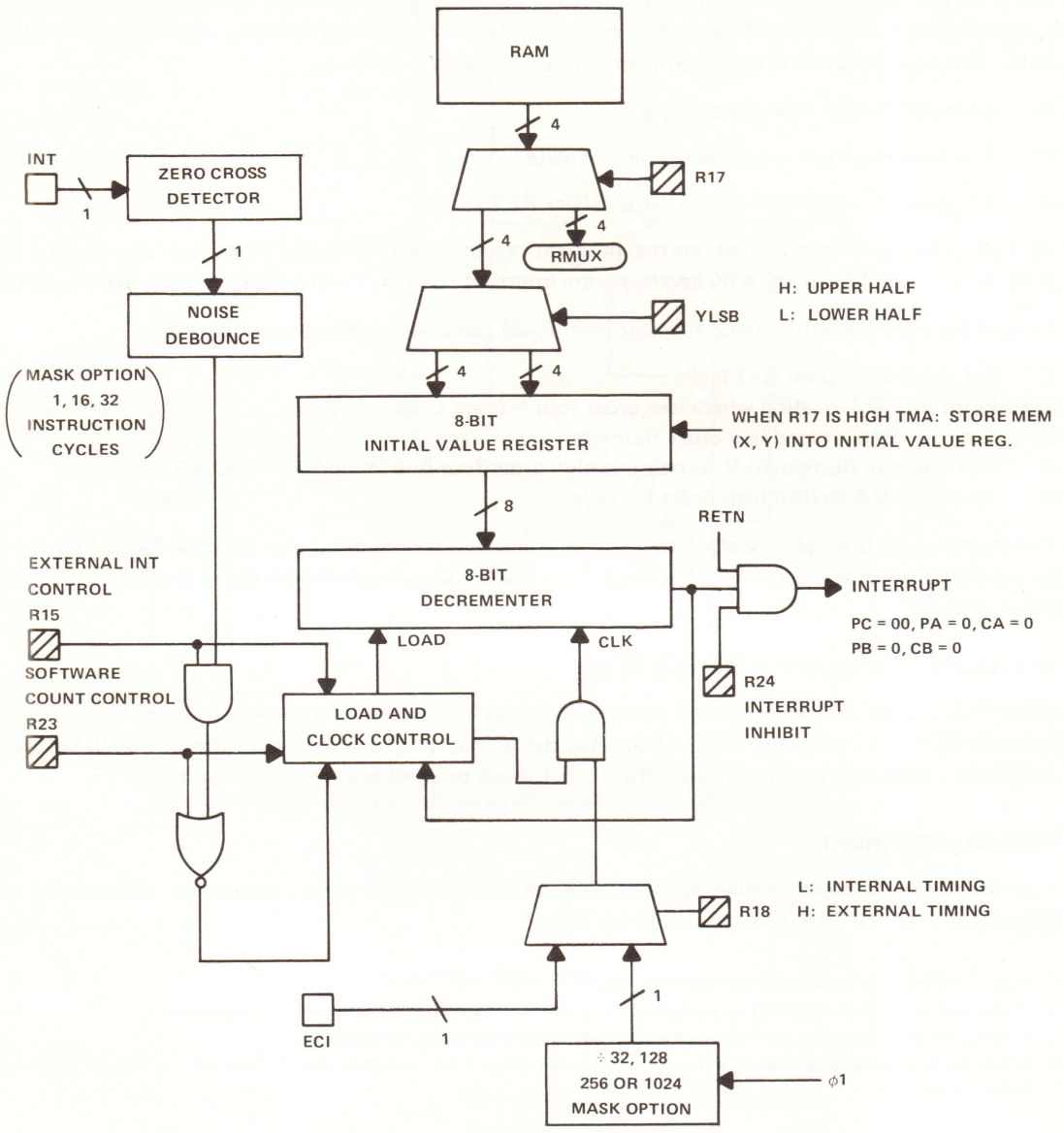
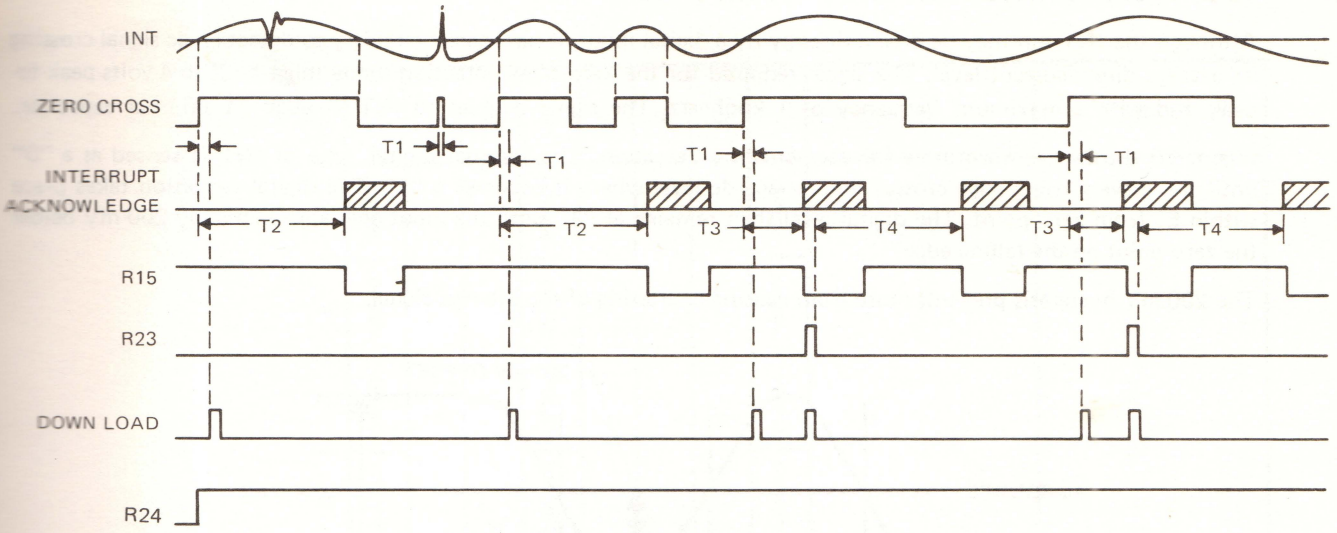


FIGURE 7 – INTERRUPT INTERVAL TIMER AND EVENT COUNTER FUNCTIONS

INTERRUPT SEQUENCE

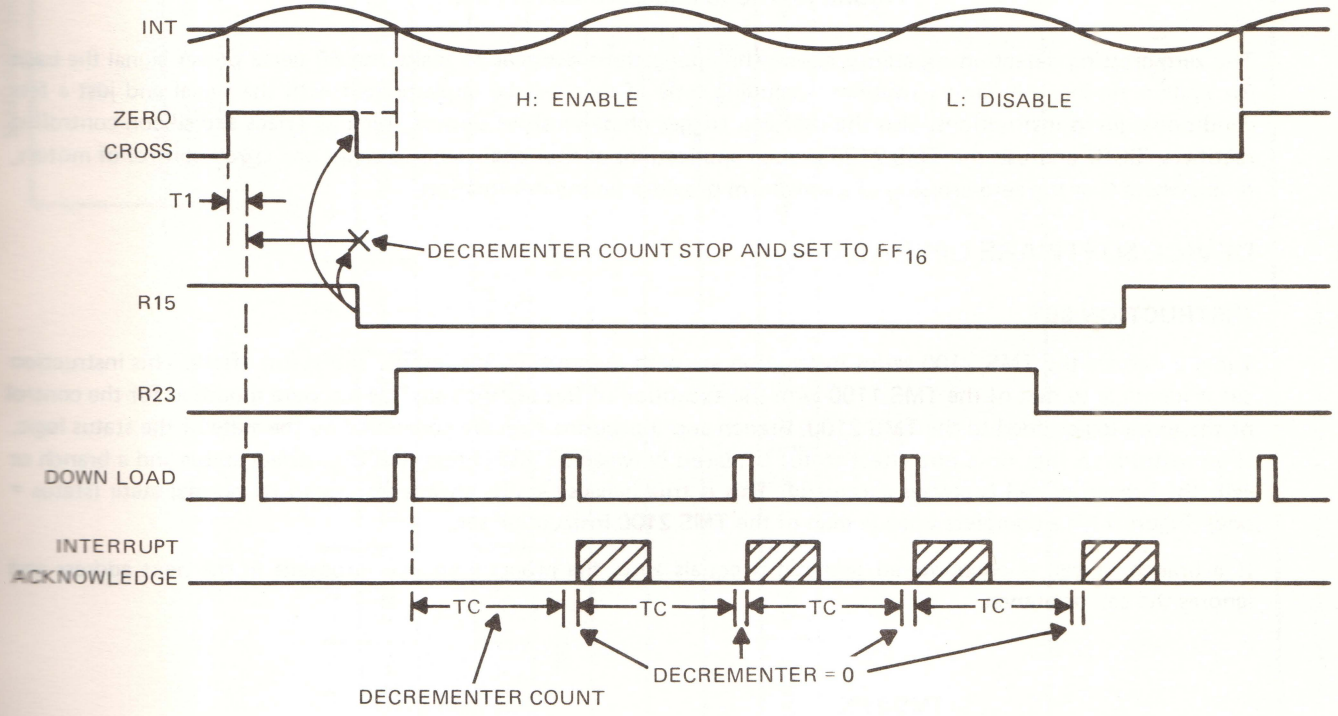
1. Interrupt acknowledge
2. Save X, Y, ACC, AC2, SF, SL, PC, PA, CA,
   PB, CB, CL, OREG into individual stack registers
3. Interrupt routine
4. RETN
5. Pop up stack registers



NOTE:

: Interrupt routine execution.
T1: Noise debounce.
T2, T3, T4: Decrementer circuit. T4 should not be within interrupt routine.

FIGURE 8 – EXAMPLE OF EXTERNAL HARDWARE INTERRUPT



NOTE: Interrupt will occur periodically if R23 is kept high.

FIGURE 9 – EXAMPLE OF SOFTWARE INTERRUPT

2.18 ZERO CROSS DETECTOR (INT INPUT – MASK OPTION)

Although the INT pin may be driven directly by a digital input, it has special circuitry to detect an ac signal crossing its average direct-current level. The signal required for the zero-cross detection mode must be 2 to 4 volts peak-to-peak and with a maximum frequency of 1 kilohertz. The signal couples to INT through an external capacitor.

Figure 10 shows the waveforms for zero-crossing detection. The internal digital state of INT is sensed as a "0" until the wave's rising edge crosses the average dc level where it becomes a "1". The digital transition takes place within 5° from zero point. The digital level then remains at "1" until the input goes approximately 200 mV below the zero point on the falling edge.

The 200 mV hysteresis prevents noise from causing chattering of the internal signal.

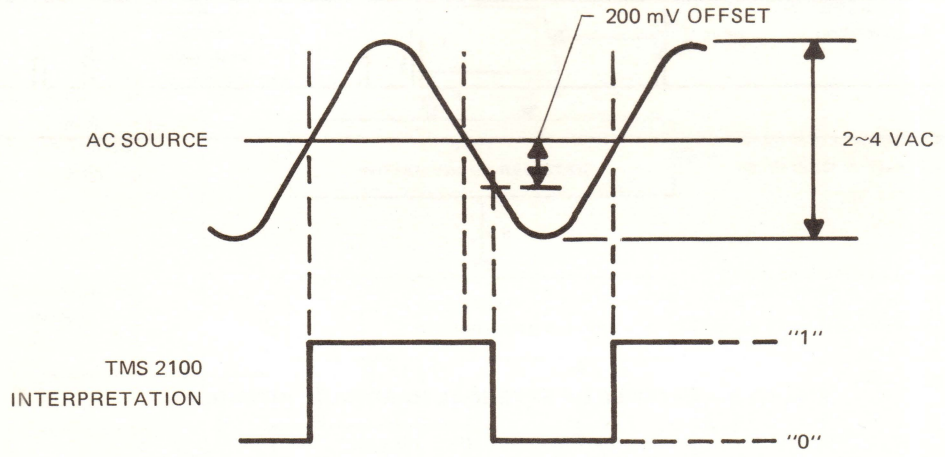


FIGURE 10 – ZERO-CROSSING WAVEFORM

The zero-crossing detection capability allows the applications designer to make the 60 hertz power signal the basis for system timing. All timing routines, including time of day, can be implemented with the signal and just a few conditional jump instructions; also the user can trigger phase-sensitive devices, such as Triacs and silicon-controlled rectifiers (SCR) and use the TMS 2100 in such applications as shaftangle measurement and speed control of motors, or anywhere that the zero-crossing of a waveform provides timing information.

3. DEVICE SOFTWARE OPERATION

3.1 INSTRUCTION SET

Table 2 defines the TMS 2100 series instruction set with description, mnemonic and status effect. This instruction set is identical to that of the TMS 1100 with the exception of five instructions* which were modified for the control of the extra logic added to the TMS 2100. Branch and subroutine calls are controlled by the state of the status logic. If an instruction that does not affect status is placed between an instruction that does affect status and a branch or call, the branch or call is always successful. This is true because status always returns to its normal state (status = one). Figure 11 is a complete upcode map of the TMS 2100 instruction set.

If a branch or call is encountered and status equals zero, the program counter proceeds to the next address and ignores the call or branch.

* TMS 2100		TMS 1100
TAX	←	COMX
TRA	←	A14AAC
TAC	←	TAMZA
TCA	←	A13AAC
TADM	←	KNEZ

MACHINE INSTRUCTION CODE

A				Z			
I(0)	I(1)	I(2)	I(3)	I(4)	I(5)	I(6)	I(7)

MSB LSB

A \ Z	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	*OPERAND
0	MNEA	ALEM	YNEA	XMA	DYN	IYC	AMAAC	DMAN	TKA	TAX	TDO	COMC	RSTR	SETR	TADM	RETN	
1	LDP																C
2	TAY	TMA	TMY	TYA	TAM-DYN	TAM-IYC	TAC	TAM	LDX								F
3	SBIT				RBIT				TBIT1				SAMAN	CPAIZ	IMAC	MNEZ	B
4	TCY																C
5	YNEC																C
6	TCMIY																C
7	IAC	A9AAC	A5AAC	TCA	A3AAC	A11AAC	A7AAC	DAN	A2AAC	A10AAC	A6AAC	TRA	A4AAC	A12AAC	A8AAC	CLA	
8	BR																W
9																	
A																	
B																	
C	CALL																W
D																	
E																	
F																	

* C = constant; B = bit address; W = memory address; F = file address.

FIGURE 11 — TMS 2100 STANDARD INSTRUCTION MAP

3.2 SUBROUTINE CALLS

The TMS 2100 series devices have a four-level subroutine stack. Long branches can be executed during any level of subroutine. Subroutines can be of any length and long branches may be executed at any time. Figure 12 is a flow diagram of subroutine calls. The total of four calls includes one level of interrupt. Only one level of subroutine is allowed during an interrupt. If the interrupt routine uses a subroutine, then only two levels of subroutine are allowed in the main program.

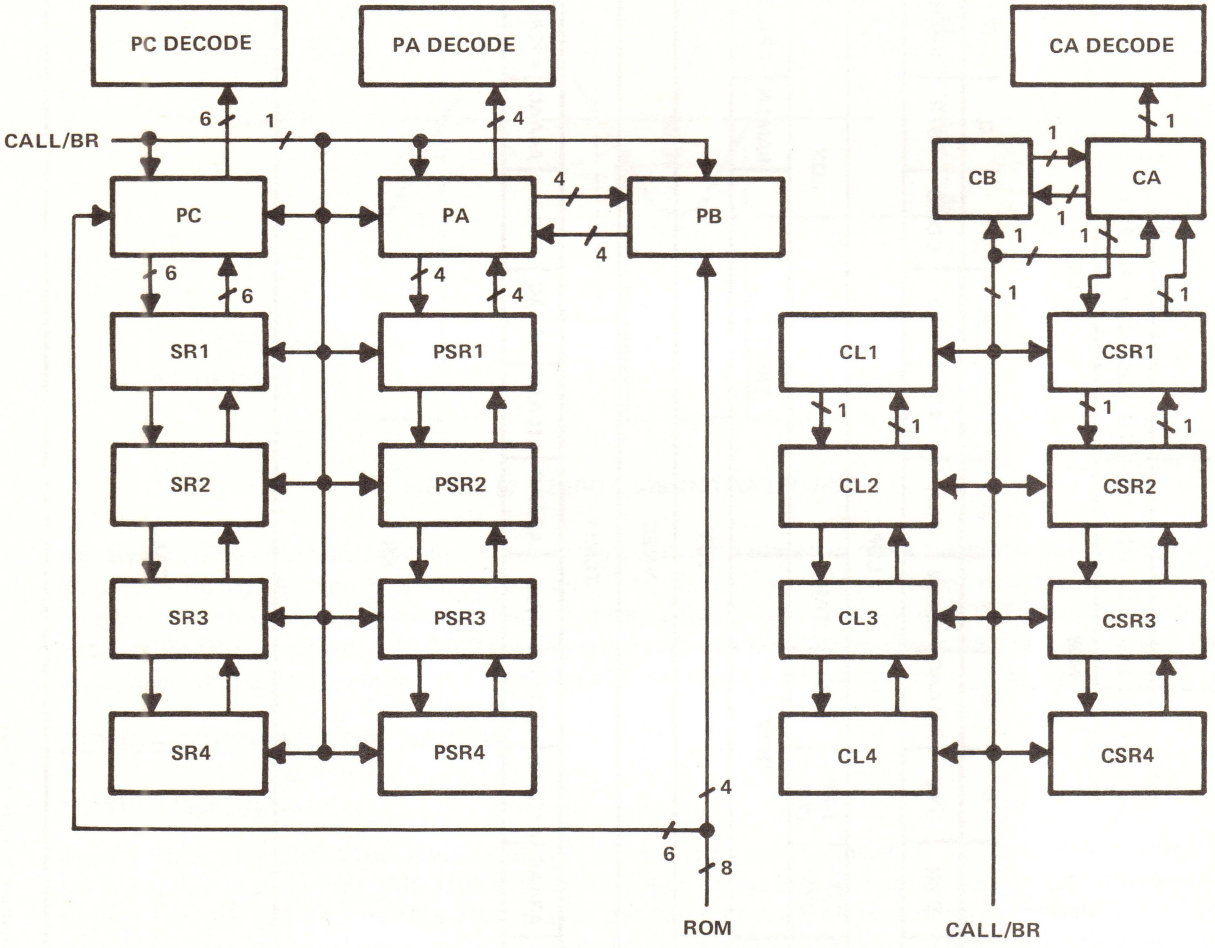


FIGURE 12 – FLOW DIAGRAM OF SUBROUTINE CALLS

3.3 ACTION OF BR INSTRUCTION

a) S (STATUS) = 1

PB → PA I(W) → PC CB → CA

b) S = 0

PC + 1 → PC 1 → S

3.4 ACTION OF CALL INSTRUCTION

a) S = 1, IL = 0

SR3 → SR4
SR2 → SR3
SR1 → SR2
PC + 1 → SR1
I(W) → PC

PSR3 → PSR4
PSR2 → PSR3
PSR1 → PSR2
PA → PSR1
PB → PA

CL3 → CL4
CL2 → CL3
CL1 → CL2
1 → CL1

CSR3 → CSR4
CSR2 → CSR3
CSR1 → CSR2
CA → CSR1
CB → CA

b) S = 1, IL = 1, ICL = 0 (INT. CALL)

Same as a) Except 1 → ICL

c) S = 0

PC + 1 → PC
1 → S

PA → PB

CA → CB

NOTES: 1. Only a one-level CALL will be allowed in INTERRUPT routine.
2. A total 4 levels of CALLS including one level of INT, will be allowed.

3.5 ACTION OF RETN INSTRUCTION

a) CL = 1, IL = 0, ICL = 0

SR1 → PC
SR2 → SR1
SR3 → SR2
SR4 → SR3

PSR1 → PA, PB
PSR2 → PSR1
PSR3 → PSR2
PSR4 → PSR3

CL2 → CL1
CL3 → CL2
CL4 → CL3
0 → CL4
1 → S

CSR1 → CA, CB
CSR2 → CSR1
CSR3 → CSR2
CSR4 → CSR3

b) CL1 = 1, IL = 1, ICL = 1

Same as a) Except 0 → ICL

c) CL1 = 0 (Dummy RETN)

PC + 1 → PC 1 → S

d) CL1 = 1, IL = 1, ICL = 0 (Interrupt RETN)

SR1 → PC
SR2 → SR1
SR3 → SR2
SR4 → SR3

PSR1 → PA
PSR2 → PSR1
PSR3 → PSR2
PSR4 → PSR3
PB STACK → PB

CL2 → CL1
CL3 → CL2
CL4 → CL3
0 → CL4

CSR1 → CA
CSR2 → CSR1
CSR3 → CSR2
CSR4 → CSR3
CB STACK → CB

XREG STACK → XREG
YREG STACK → YREG
ACC STACK → ACC
AC2 STACK → AC2
SF STACK → SF
SL STACK → SL
OREG STACK → OREG

0 → IL

4. ELECTRICAL SPECIFICATIONS

4.1 TMS 2100/2300

4.1.1 ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)*

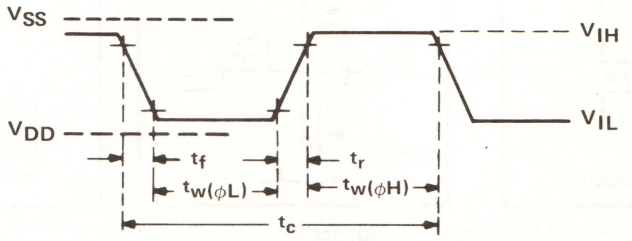
Voltage applied to any device terminal (see Note 1)	−15 V
Supply voltage range, V_{DD}, AV_{DD}	−15 V to 0.3 V
Input voltage range: Data, clock	−15 V to 0.3 V
Input voltage range: Analog A1, A2	−15 V to 2 V
Average output current (see Note 2): O-Outputs	−24 mA
R-Outputs	−14 mA
Peak output current: O-Outputs	−48 mA
R-Outputs	−28 mA
Continuous power dissipation: TMS 2100	400 mW
TMS 2300	600 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−55°C to 150°C

* Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

4.1.2 RECOMMENDED OPERATING CONDITIONS

PARAMETER		MIN	NOM	MAX	UNIT
Logic supply voltage, V_{DD} (see Note 3)		−8.5	−9	−10.5	V
Analog supply voltage	AV_{DD} (see Note 4)	−5		0.6 V_{DD}	V
	AV_{SS} with respect to V_{SS}		0		
Analog input voltage range	A1, A2	AV_{SS}		AV_{DD}	V
High-level input voltage, V_{IH} (see Note 5)	K,J,R,ECI or INT (TTL)	−2.4		0.3	V
	INIT or Clock	−0.6		0.3	
Low-level input voltage, V_{IL} (see Note 5)	K,J,R,ECI or INT (TTL)	V_{DD}		−4	V
	INIT or Clock	V_{DD}		−6	
INT (zero-cross) peak-to-peak input voltage				2	V
INT (zero-cross) input current				20	μA
Clock cycle time, $t_{c(\phi)}$		2		3.3	μs
Instruction cycle timer, t_c		12		20	μs
Pulse width, clock high, $t_{w(\phi H)}$		0.81			μs
Pulse width, clock low, $t_{w(\phi L)}$		0.81			μs
Sum of rise time and pulse width, clock high, $t_r + t_{w(\phi H)}$		0.91			μs
Sum of fall time and pulse width, clock low, $t_f + t_{w(\phi L)}$		0.91			μs
Oscillator frequency, f_{osc}		300		500	kHz
Operating free-air temperature, T_A		0		70	°C

NOTES:
1. Unless otherwise noted, all logic-associated voltages are with respect to V_{SS} and all analog-associated voltages are with respect to AV_{SS}.
2. These average values apply for any 100 ms period.
3. Ripple must not exceed 0.2 volts peak-to-peak in the operating frequency range.
4. Device accuracy is dependent on stability of the analog supply voltage. Ripple must not exceed 5 mV peak-to-peak.
5. The algebraic convention where the more negative (less positive) limit is designated as minimum is used in this specification for logic voltage levels only.



NOTE: Timing points are 90% (high) and 10% (low).

4.1.3 ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED) TMS 2100/2300

PARAMETER				TEST CONDITIONS	MIN	NOM†	MAX	UNIT
I_I	Input current	K, J1, J2, INT (TTL) ECI		V_I = 0 V	70	180	400	μA
		J4/A1 J8/A2 INT (zero cross), R		V_I = 0 V/V_{DD}			2	
V_{OH}	High-level output voltage (see Note 1)	O-Outputs		I_O = −10 mA	−1.1	−0.6		V
		R-Outputs		I_O = −2 mA	−0.75	−0.4		
I_{OL}	Low-level output current, K, J, INT			V_{OL} = V_{DD}			−10	μA
I_{OSS}	Pull down short-circuit current	O-Outputs	No pull down	V_O = V_{SS}, V_{DD} = −9 V		0		μA
			100 μA pull down		100			
			300 μA pull down		300			
			900 μA pull down		900			
		R-Outputs	No pull down			0		
			100 μA pull down		100			
			300 μA pull down		300			
V_{OL}	Low-level output voltage		No pull down	I_O = 50 μA, V_{DD} = −9 V		V_{DD}	−8	V
			With pull down					
$I_{DD(AV)}$	Average supply current from V_{DD} (see Note 2)			All outputs open		−10	−15	mA
$P_{(AV)}$	Average power dissipation (see Note 2)			All outputs open		90	158	mW
f_{osc}	Internal oscillator frequency			R_{ext} = 47 kΩ, C_{ext} = 47 pF	450	500	550	kHz
C_i	Small-signal input capacitance, K inputs, J inputs			V_I = 0, f = 1 kHz		10		pF
$C_{i(\phi)}$	Input capacitance, clock input			V_I = 0, f = 100 kHz		25		pF

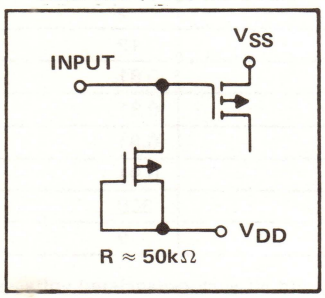
† All typical values are at V_{DD} = −9 V, T_A = 25°C.

NOTES: 1. The algebraic convention where the more positive (less negative) limit is designated as maximum is used in the specification for logic voltage levels only.

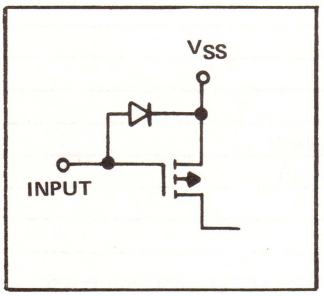
2. Values are given for the open-drain O and R output configurations. Pull-down resistors are optionally available on all outputs and increase I_{DD} (see schematic).

4.1.4 SCHEMATICS OF INPUTS AND OUTPUTS

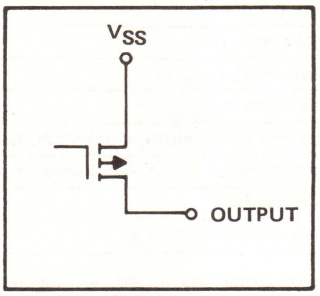
TYPICAL OF K, J1, J2, ECI AND INT (TTL) INPUTS



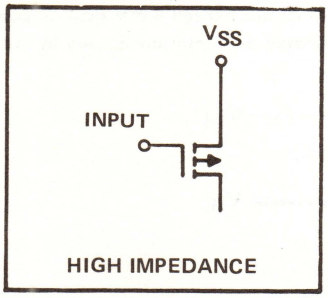
TYPICAL OF INT (ZERO-CROSS)



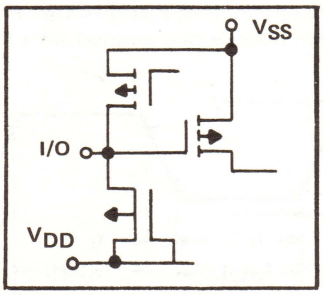
TYPICAL OF ALL O AND R OPEN DRAIN OUTPUTS



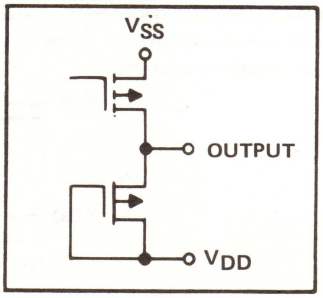
TYPICAL OF A1/J4, A2/J8



TYPICAL OF R0-R3



TYPICAL OF ALL O AND R OUTPUTS WITH OPTIONAL PULL DOWN RESISTORS



The O-outputs have nominally 60-Ω on-state impedance.
The R-outputs have nominally 200-Ω on-state impedance.

4.2 TMS 2170/2370

4.2.1 ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)*

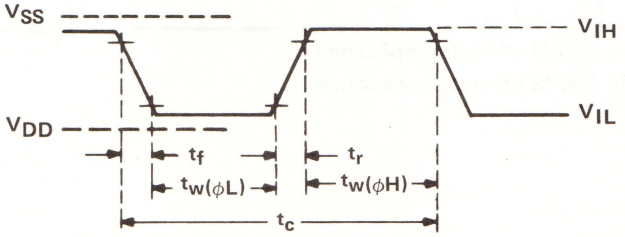
Applied output voltage range (see Note 1) . . . . . −35 V
Applied input voltage range . . . . . −35 V
Supply voltage range, V_{CC} . . . . . −15 V to 0.3 V
Input voltage range: INIT, clock . . . . . −15 V to 0.3 V
Input voltage range: Analog A1, A2 . . . . . −15 V to 2 V
Average output current (see Note 2): O-Outputs . . . . . −2.5 mA
R-Outputs . . . . . −12 mA
Peak output current: O-Outputs . . . . . −5 mA
R-Outputs . . . . . −24 mA
Continuous power dissipation: TMS 2170 . . . . . 400 mW
TMS 2370 . . . . . 600 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −55°C to 150°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

4.2.2 RECOMMENDED OPERATING CONDITIONS

PARAMETER		MIN	NOM	MAX	UNIT
Applied output and input voltage range		0	−26	−30	V
Supply voltage, V_{PP}		0	−26	−30	V
Logic supply voltage V_{DD} (see Note 3)		−8.5	−9	−10.5	V
Analog supply voltage (see Note 5)	AV_{DD} (see Note 4)	−5		0.6 V_{DD}	V
	AV_{SS} with respect to V_{SS}		0		
Analog input voltage range, A1, A2		AV_{SS}		AV_{DD}	V
High-level input voltage, V_{IH} (see Note 5)	K, J, INT (TTL), R, ECI	−2.4		0.3	V
	INIT or Clock	−1		0.3	
Low-level input voltage, V_{IL} (see Note 5)	K, J, INT (TTL), R, ECI	−30		−4	V
	INIT or Clock	V_{DD}		−6	
INT (zero-cross) peak-to-peak input voltage				2	V
INT (zero-cross) input current				20	μA
Clock cycle time, $t_{c(\phi)}$		2		3.3	μs
Instruction cycle timer, t_c		12		20	μs
Pulse width, clock high, $t_{w(\phi H)}$		0.81			μs
Pulse width, clock low, $t_{w(\phi L)}$		0.81			μs
Sum of rise time and pulse width, clock high, $t_r + t_{w(\phi H)}$		0.91			μs
Sum of fall time and pulse width, clock low, $t_f + t_{w(\phi L)}$		0.91			μs
Oscillator frequency, f_{osc}		300		500	kHz
Operating free-air temperature, T_A		0		70	°C

NOTES: 1. Unless otherwise noted, all logic-associated voltages are with respect to V_{SS} and all analog-associated voltages are with respect to AV_{SS}.
2. These average values apply for any 100 ms period.
3. Ripple must not exceed 0.2 volts peak-to-peak in the operating frequency range.
4. Device accuracy is dependent on stability of the analog supply voltage. Ripple must not exceed 5 mV peak-to-peak.
5. The algebraic convention where the more negative (less positive) limit is designated as minimum is used in this specification for logic voltage levels only.



NOTE: Timing points are 90% (high) and 10% (low).

4.2.3 ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED) TMS 2170/TMS 2370

PARAMETER				TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I_I	Input current	K, J1, J2, INT (TTL), ECI		V_I = 0 V	70	180	400	μA
		J4/A2, J8/A2, R		V_I = 0 V/V_{DD}			2	
V_{OH}	High-level output voltage (see Note 1)	O-Output		I_O = –1.8 mA	–1.7			V
		R-Output		I_O = –4.5 mA	–1.7			
I_{OL}	Output current	O-Output		V_O = –30 V			–20	μA
		R-Output		V_O = –30 V			–20	
I_{OSS}	Pull down short-circuit current	O-Output	No pull down	V_O = V_{SS}, V_{DD} = –9		0		μA
			100 μA pull down		100			
			300 μA pull down		300			
			900 μA pull down		900			
		R-Output	No pull down			0		
			100 μA pull down		100			
			300 μA pull down		300			
V_{OL}	Low level output voltage		No pull down	I_O = 50 μA, V_{DD} = –9 V, V_{PP} = –30 V				V
			With pull down			V_{PP}	–25	
$I_{DD(AV)}$	Average supply current from (see Note 2)			All (outputs/inputs) open		10	15	mA
$P_{(AV)}$	Average power dissipation (see Note 2)			All (outputs/inputs) open		90	158	mW
f_{osc}	Internal oscillator frequency			R_{ext} = 47 kΩ, C_{ext} = 47 pF	40	50	550	kHz
C_i	Small-signal input capacitance, K-inputs			V_I = 0 V, f = 1 kHz		10		pF
$C_{i(\phi)}$	Input capacitance, clock input			V_I = 0 V, f = 100 kHz		25		pF

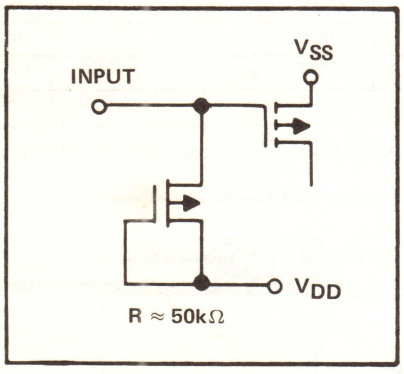
† All typical values are at V_{DD} = –9 V, T_A = 25°C (low power version).

NOTES: 1. The algebraic convention where the more positive (less negative) limit is designated as maximum is used in this specification for logic voltage levels only.

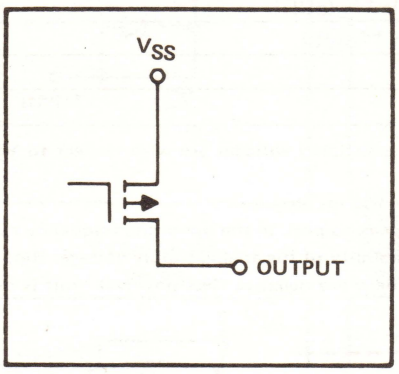
2. Values are given for the open-drain O and R output configurations. Pull-down devices are optionally available on all outputs per increase I_{DD} (see schematics).

4.2.4 SCHEMATICS OF INPUTS AND OUTPUTS

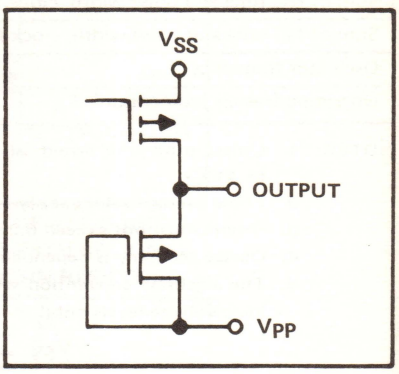
TYPICAL OF ALL K INPUTS K, J1, J2, ECI, INT (TTL)



TYPICAL OF ALL O AND R OPEN DRAIN OUTPUTS



TYPICAL OF ALL O AND R OUTPUTS WITH OPTIONAL PULL DOWN RESISTORS



The O-outputs have nominally 750-Ω on-state impedance.
The R-outputs have nominally 300-Ω on-state impedance.

ANGE

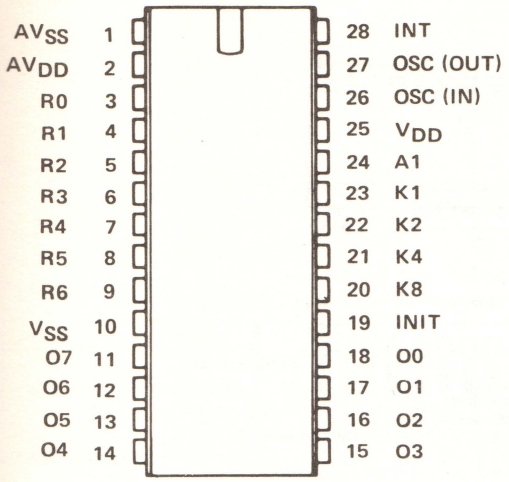
UNIT
μA
V
μA
μA
V
mA
mW
kHz
pF
pF

ion for

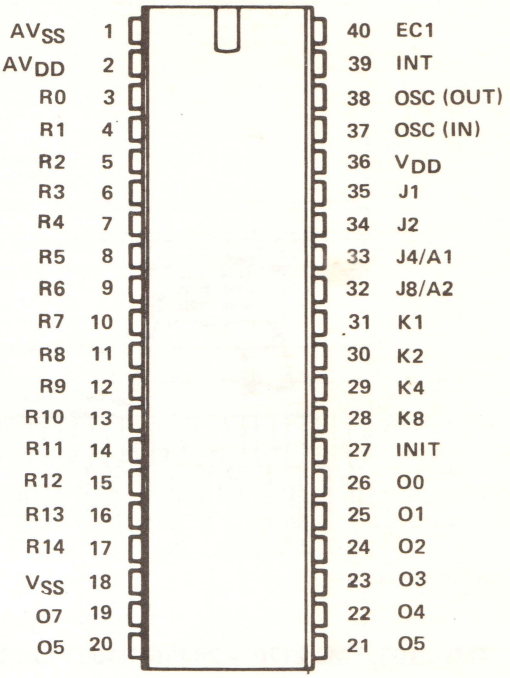
uts per

4.3 TERMINAL ASSIGNMENTS

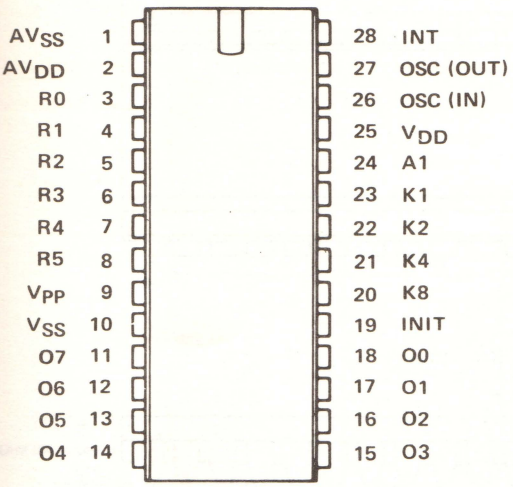
TMS 2100
28-PIN N400



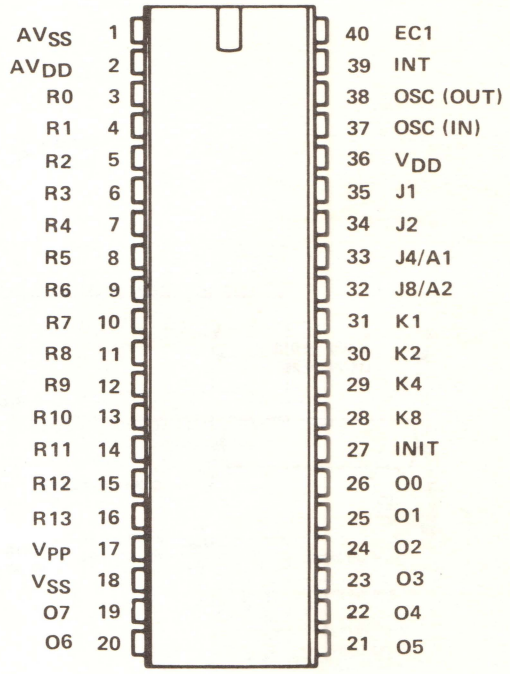
TMS 2300
40-PIN N600



TMS 2170
28-PIN N400

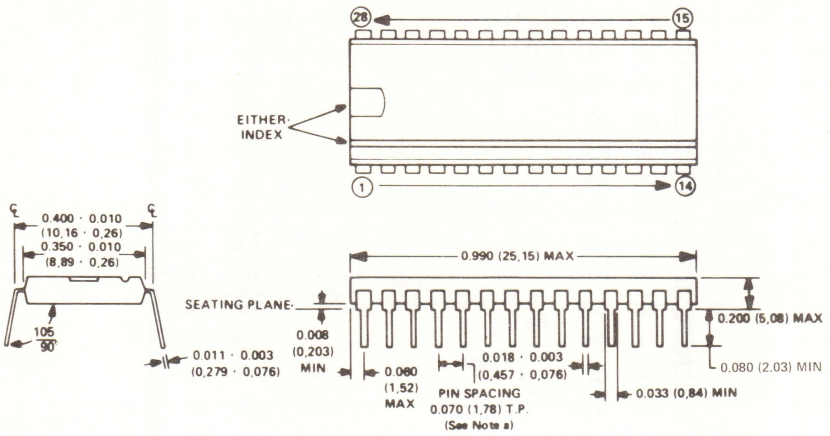


TMS 2370
40-PIN N600

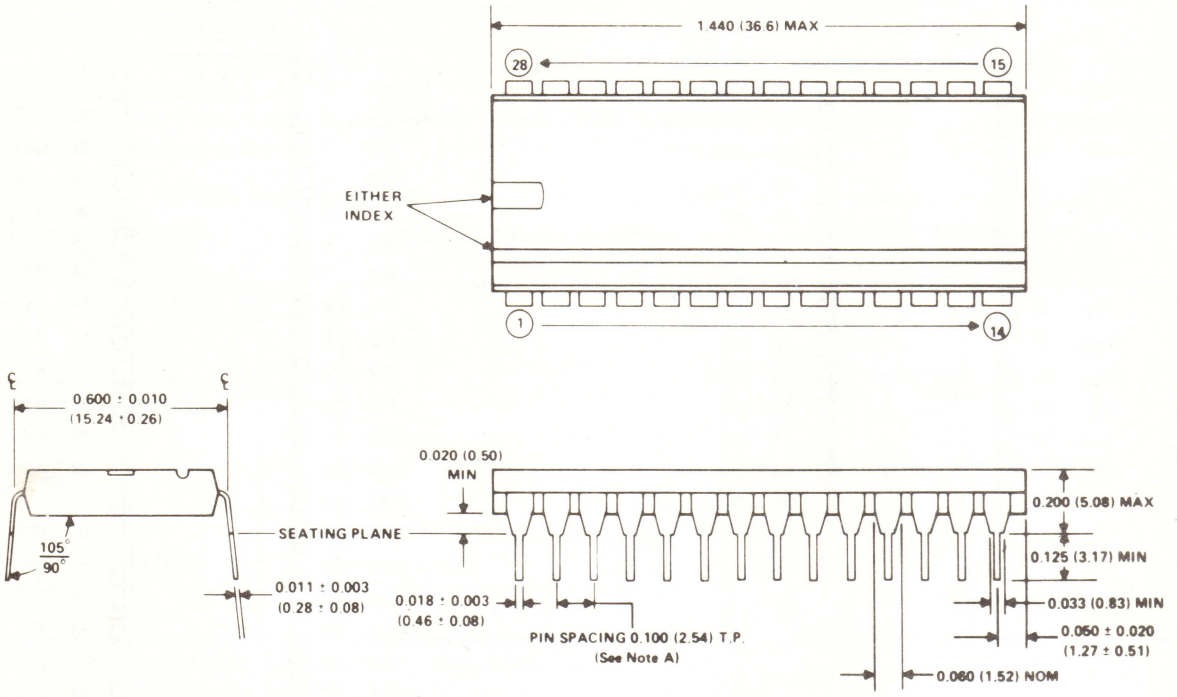


5. MECHANICAL DATA

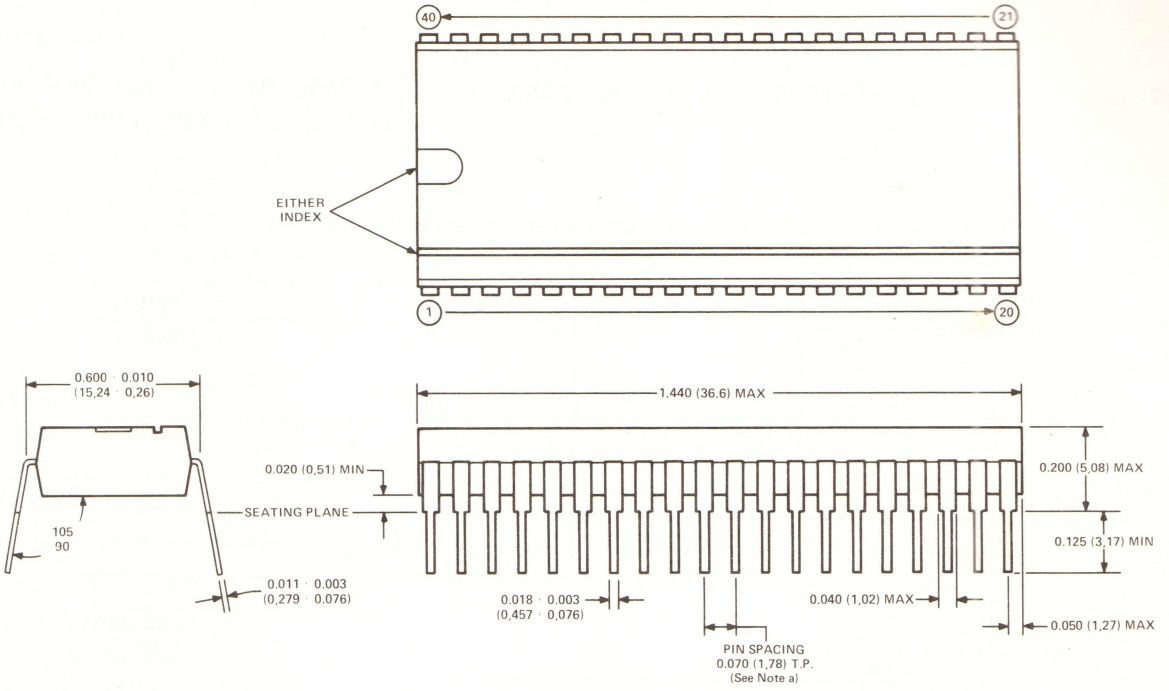
5.1 TMS 2100, TMS 2170 – 28-PIN N400 PLASTIC PACKAGE – PIN SPACING 0.070



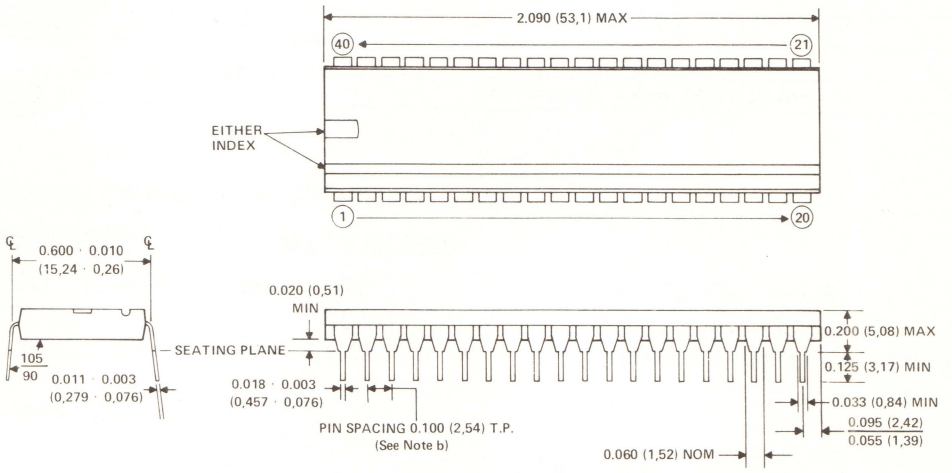
5.2 TMS 2100, TMS 2170 – 28-PIN N400 PLASTIC PACKAGE – PIN SPACING 0.100



5.3 TMS 2300, TMS 2370 – 40-PIN N600 PLASTIC PACKAGE – PIN SPACING 0.070



5.4 TMS 2300, TMS 2370 – 40-PIN N600 PLASTIC PACKAGE – PIN SPACING 0.100



NOTES: a. All linear dimensions are in inches and parenthetically in millimeters. Inch dimensions govern.
b. Each pin centerline is located within 0.010 (0,26) of its true longitudinal position.

APPENDIX A

TMS 2400 SERIES FEATURES

DESCRIPTION

The TMS2400/2600 and TMS2470/2670 microcomputers are extensions of the TMS2100 series. The key features are summarized in Table 1 below.

TABLE 1 – TMS 2400 MICROCOMPUTER SERIES FEATURES

FEATURES	TMS 2400	TMS 2600	TMS 2470	TMS 2670
Maximum-Rated Voltage (O, R, K, J, INT, and ECI)	–15 V	–15 V	–35 V	–35 V
Package Pin Count	28 Pins	40 Pins	28 Pins	40 Pins
"R" Individually Addressed Output Latches	7	15	6	14
K, J and R Inputs	8	12	8	12
Analog Inputs	1	4	1	4
Event Counter	No	Yes	No	Yes
Interval Timer	Yes			
Instruction Read Only Memory	4096 X 8 Bits (32,768 bits)			
Data Random Access Memory	256 X 4 Bits (1024 bits)			
"O" Parallel Latched Data Outputs	8			
Working Registers	3 (4 Bits each)			
Instruction Set	Enhanced TMS 1100 Instruction Set (See Note)			
Programmable O Output Decoder	Yes (32 AND terms)			
On-Chip Oscillator	Yes			
Power Supply/Typical Dissipation	–9 V/90 mW			
Development System				
System Evaluator Device with External Instruction Memory	SE-2400 (TMS 1094 JLL)			
Subroutine Levels	4 Levels			
8-Bit A/D Converter	Yes			
Hardware Interrupt (1 level)	Yes			
Zero Cross Detector	Yes (Mask Option)			
Frequency Divider to K8	Yes (Optional – Pass, 1/2, 1/10 and 1/20)			

NOTE the following instruction set differences

TMS2100/2300		TMS2400/2600	
COMC	→	TPC	Transfer PB → CB
A11AAC	→	COMX	Complement MSB of X
A12AAC	→	TXA	Transfer X-register to accumulator

Analog Input Selection

A-Input	R25	R19
A1	L	L
A2	L	H
A4	H	L
A8	H	H

APPENDIX B

EVALUATOR BOARD

GENERAL

The SEB 2100 System Evaluation Board is described in Table B-1. This board utilizes the SE 2100 and a TMS 2716 or 2516 to emulate the TMS 2100 series microcomputers.

The System Evaluator (SE 2100), together with the stored program in EPROM, the O-output PROM, oscillator elements, input and output interface and the on-board voltage regulation make up the System Evaluation Board. The following sections will present each of the board components in greater detail.

Table B-1. System Evaluation Board, SEB 2100

CHARACTERISTICS				
System Evaluator	SE 2100			
Microcomputer Simulated	TMS 2100	TMS 2300	TMS 2170	TMS 2370
Read Only Memory	2048 x 8 bits/word			
EPROM Utilized	TMS 2516 or TMS 2716			
Random Access Memory	128 x 4 bits/word			
Maximum R Lines of Corresponding Device	7	15	6	14
O-Output Lines	8	8	8	8
O-Output PROM	74S288			

SE 2100 SYSTEM EVALUATOR

The SE 2100 System Evaluator contains the on-chip random access memory, utilizes the standard instruction set, and with external memory is functionally identical to the TMS 2100 series.

The SE 2100 used on the System Evaluation Board utilizes a dedicated parallel instruction address port to select an instruction word from the external program memory, a TMS 2516 or TMS 2716. The instruction word is then transferred into the system evaluator through an 8-bit parallel input port, I0 through 17. An SN74S288 PROM provides O-output code conversion of the five O-outputs from the SE 2100. The four K inputs, four J inputs, and the 15 R outputs of the System Evaluator are functionally identical to the respective TMS 2100 series inputs and outputs.

Table B-2 presents the SE 2100 pin assignments and describes the function of each pin.

Table B-2. SE 2100 Pin Assignments and Pin Functions

SIGNATURE	PIN	I/O	DESCRIPTION
R0	4	I/O	R0 through R3 are bidirectional.
R1	5	I/O	
R2	6	I/O	
R3	7	I/O	
R4	8	OUT	R4 through R14 are the outputs of the R-register.
R5	9	OUT	
R6	10	OUT	
R7	11	OUT	
R8	12	OUT	
R9	13	OUT	
R10	14	OUT	
R11	15	OUT	
R12	16	OUT	
R13	17	OUT	
R14	18	OUT	
K1	45	IN	These are the data input lines, with K1 and J1 being the least significant bit.
K2	44	IN	
K4	43	IN	
K8	42	IN	
J1	49	IN	
J2	48	IN	
J4/A1	47	IN	A1 and A2 are analog inputs.
J8/A2	46	IN	
O1	51	OUT	These are the data outputs of the O-register, with O1 being the least significant bit and OSL being the output of the status latch.
O2	52	OUT	
O4	53	OUT	
O8	54	OUT	
OSL	50	OUT	
V_{DD}	55		Power supply input.
V_{SS}	1		Power supply input.
AV_{DD}	3	IN	Analog negative voltage reference.
AV_{SS}	2	IN	Analog positive voltage reference.
INIT	41	IN	INIT is used for initialization, during power-on or for hardware reset.
OSCIN	56	IN	OSCIN and OSCOUT are shorted together to operate the internal oscillator. See section 2.3.
OSCOUT	57	IN	
PA1	38	OUT	PA1 through PA8 are the ROM page address outputs, with PA8 being the most significant bit.
PA2	37	OUT	
PA4	36	OUT	
PA8	35	OUT	
PC0	32	OUT	PC0 through PC5 are the ROM program counter outputs, with PC0 being the most significant bit.
PC1	31	OUT	
PC2	30	OUT	
PC3	29	OUT	
PC4	28	OUT	
PC5	27	OUT	

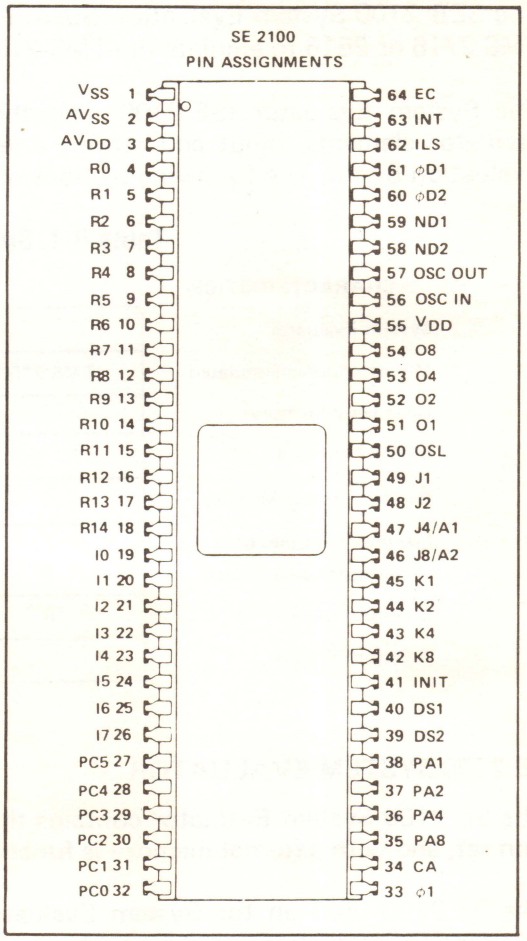


Table B-2. SE 2100 Pin Assignments and Pin Functions (Continued)

SIGNATURE	PIN	I/O	DESCRIPTION
CA	34	OUT	CA is the ROM chapter address output.
I0	19	IN	I0 through I7 are the external memory instruction inputs, with I0 being the most significant bit.
I1	20	IN	
I2	21	IN	
I3	22	IN	
I4	23	IN	
I5	24	IN	
I6	25	IN	
I7	26	IN	
DS1	40		DS1 and DS2 select the frequency divider options (pass, 1/2, 1/10, 1/20).
DS2	39		
ND1	59		ND1 and ND2 select the noise debounce options (1, 16, 32 instruction cycles).
ND2	58		
ϕD1	61		ϕD1 and ϕD2 select the decrementer clock divider options (1/32, 1/128, 1/256, 1/1024).
ϕD2	60		
ILS	62		Input level interface option (zero cross or TTL).
INT	63		Interrupt.
EC	64		Event counter.

TEXAS INSTRUMENTS
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