The Engineering Staff of
TEXAS INSTRUMENTS INCORPORATED
Semiconductor Group

The Line Driver and Line Receiver Data Book

for

Design Engineers

1981

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INCORPORATED

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IMPORTANT NOTICES

Texas Instruments reserves the right to make changes at any time in order to improve design and to supply the best product possible.

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Information contained herein supersedes all previously published data on Line Driver and Line Receiver Interface Circuits including data books CC-415, *The Line Driver and Line Receiver Data Book 1977* (LCC4290), and portions of *The Interface Circuits Data Book*, first edition (LCC4330).

TABLE OF CONTENTS

ALPHANUMERIC INDEX

*Future product, to be announced

INTERCHANGEABILITY GUIDE
(MANUFACTURERS ARRANGED ALPHABETICALLY)

Direct replacements were based on similarity of electrical and mechanical characteristics as shown in currently published data. Interchangeability in particular applications is not guaranteed. Before using a device as a substitute, the user should compare the specifications of the substitute device with the specifications of the original.

Texas Instruments makes no warranty as to the information furnished and buyer assumes all risk in the use thereof. No liability is assumed for damages resulting from the use of the information contained in this list.

ADVANCED MICRO DEVICES

EXAMPLE OF NOMENCLATURE

AM	1489A	N
Prefix	Device Type	Package Type
		N = Plastic DIP (second source designation for TI Plastic DIP)
		P = Plastic DIP
		J = Ceramic DIP (second source designation for TI Ceramic DIP)
		D = Ceramic DIP

AMD	TI DIRECT REPLACEMENT	TI CLOSEST REPLACEMENT
AM1488	SN75188	
AM1489	SN75189	
AM1489A	SN75189A	
AM26LS31C	AM26LS31C	
AM26LS32C	AM26LS32AC	
AM26LS33C	AM26LS33AC	
AM26S10C	AM26S10C	
AM26S10M	AM26S10M	
AM26S11C	AM26S11C	
AM26S11M	AM26S11M	
AM55107B	SN55107B	
AM55108B	SN55108B	
AM55109	SN55109A	
AM55110	SN55110A	
AM75107B	SN75107B	
AM75108B	SN75108B	
AM75109	SN75109A	
AM75110	SN75110A	
AM75207	SN75207	
AM75208	SN75208	
AM7820A	SN55182	
AM7830	SN55183	
AM7831	DS7831	
AM7832	DS7832	
AM8T26A	N8T26A	
AM8820A	SN75182	
AM8830	SN75183	
AM8831	DS8831	
AM8832	DS8832	
AM9614C	SN75114	
AM9614M	SN55114	
AM9615C	SN75115	
AM9615M	SN55115	

FAIRCHILD

EXAMPLE OF NOMENCLATURE

9636A	D	C
Device Type	Package Type D = Ceramic DIP P = Plastic DIP R = Ceramic Mini DIP T = Plastic Mini DIP F = Flat Package	Temperature Range C = Commercial 0°C to 70°C or 75°C M = Military −55°C to 125°C

FAIRCHILD	TI DIRECT REPLACEMENT	TI CLOSEST REPLACEMENT
μA1488C	SN75188	
μA1489C	SN75189	
μA1489AC	SN75189A	
μA8T13M	SN55121	
μA8T13C	SN75121	
μA8T14M	SN55122	
μA8T14C	SN75122	
μA8T23C	SN75123	
μA8T24C	SN75124	
55107AM	SN55107A	
55107BM	SN55107B	
55108AM	SN55108A	
55108BM	SN55108B	
55109M	SN55109A	
55110M	SN55110A	
55121M	SN55121	
55122M	SN55122	
55450AM	SN55450B	
55450BM	SN55450B	
55451AM	SN55451B	
55451BM	SN55451B	
75107AC	SN75107A	
75107BC	SN75107B	
75108AC	SN75108A	
75108BC	SN75108B	
75109C	SN75109A	
75110C	SN75110A	
75112C	SN75112	
75121C	SN75121	
75122C	SN75122	
75123C	SN75123	
75124C	SN75124	

FAIRCHILD	TI DIRECT REPLACEMENT	TI CLOSEST REPLACEMENT
75150C	SN75150	
75154C	SN75154	
75207C	SN75207	
75208C	SN75208	
75450AC	SN75450B	
75450BC	SN75450B	
75451AC	SN75451B	
75451BC	SN75451B	
9614M	SN55114	
9614C	SN75114	
9615M	SN55115	
9615C	SN75115	
9616C		SN75188 SN75150
9617C		SN75152 SN75154 SN75189 SN75189A
9626C	N8T26A	
9627C		SN75152
9634C		SN75159
9636AC	uA9636AC	
9636AM	uA9636AM	
9637AC	uA9637AC	
9637AM	uA9637AM	
9638C	uA9638C	
9638M	uA9638M	
9640C	AM26S10C	
9640M	AM26S10M	
9641C	AM26S11C	
9641M	AM26S11M	
9644C		SN75361A

ITT

EXAMPLE OF NOMENCLATURE

ITT	75107A	–5	D
Prefix	Device Type	Temperature Range –1 = –55°C to 125°C –5 = 0°C to 70°C	Package D = Ceramic DIP N = Plastic DIP

ITT	TI DIRECT REPLACEMENT	TI CLOSEST REPLACEMENT
ITT1488	SN75188	
ITT1489	SN75189	
ITT1489A	SN75189A	
ITT55107A	SN55107A	
ITT55107B	SN55107B	
ITT55108A	SN55108A	
ITT55108B	SN55108B	
ITT55109	SN55109A	
ITT55110	SN55110A	
ITT55138	SN55138	
ITT55450	SN55450B	
ITT55451	SN55451B	
ITT75107A	SN75107A	
ITT75107B	SN75107B	
ITT75108A	SN75108A	
ITT75108B	SN75108B	
ITT75109	SN75109A	
ITT75110	SN75110A	
ITT75138	SN75138	
ITT75207	SN75207	
ITT75208	SN75208	
ITT75450	SN75450B	
ITT75451	SN75451B	
ITT9614	SN75114	
ITT9615	SN75115	

MOTOROLA

EXAMPLE OF NOMENCLATURE

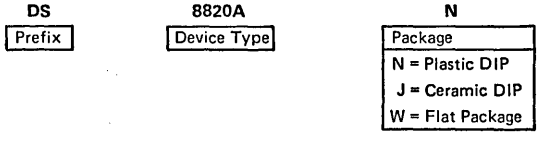
MC	1489A	P
Prefix	Device Type	Package P = Plastic DIP L = Ceramic DIP F = Flat Package

MOTOROLA	TI DIRECT REPLACEMENT	TI CLOSEST REPLACEMENT
MC1488	SN75188	
MC1489	SN75189	
MC1489A	SN75189A	
MC26S10	AM26S10C	
MC26S11	AM26S11C	
MC3443		SN75138
MC3446	MC3446	
MC3447		SN75160A SN75161A SN75162A
MC3453		SN75110A
MC3481	SN75126	
MC3485	SN75130	
MC3486	MC3486	
MC3487	MC3487	
MC55107	SN55107A	
MC55108	SN55108A	
MC75107	SN75107A	
MC75108	SN75108A	
MC75109	SN75109A	
MC75110	SN75110A	

MOTOROLA	TI DIRECT REPLACEMENT	TI CLOSEST REPLACEMENT
MC75125	SN75125	
MC75127	SN75127	
MC75128	SN75128	
MC75129	SN75129	
MC75140	SN75140	
MC75450	SN75450B	
MC75451	SN75451B	
MC8T13	SN75121	
MC8T14	SN75122	
MC8T23	SN75123	
MC8T24	SN75124	
MC8T26A	N8T26A	

NATIONAL

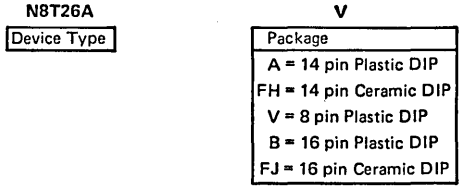
EXAMPLE OF NOMENCLATURE



NATIONAL	TI DIRECT REPLACEMENT	TI CLOSEST REPLACEMENT
DS1488	SN75188	
DS1489	SN75189	
DS1489A	SN75189A	
DS26LS31	AM26LS31C	
DS26LS32	AM26LS32AC	
DS26S10C	AM26S10C	
DS26S10M	AM26S10M	
DS26S11C	AM26S11C	
DS26S11M	AM26S11M	
DS3486	MC3486	
DS3487	MC3487	
DS55107	SN55107B	
DS55108	SN55108B	
DS55109	SN55109A	
DS55110	SN55110A	
DS55113	SN55113	
DS55114	SN55114	
DS55115	SN55115	
DS55121	SN55121	
DS55122	SN55122	
DS55450	SN55450B	
DS55451	SN55451B	
DS75107	SN75107B	
DS75108	SN75108B	
DS75109	SN75109A	
DS75110	SN75110A	
DS75113	SN75113	
DS75114	SN75114	
DS75115	SN75115	
DS75121	SN75121	
DS75122	SN75122	
DS75123	SN75123	
DS75124	SN75124	
DS75150	SN75150	
DS75154	SN75154	
DS75207	SN75207B	
DS75208	SN75208B	
DS75361	SN75361A	
DS75450	SN75450B	
DS75451	SN75451B	
DS78LS20		SN55182
DS7820	SN55182	
DS7820A	SN55182	
DS7830	SN55183	
DS7831	DS7831	
DS7832	DS7832	
DS8T26A	N8T26A	
DS88LS20		SN75182
DS8820	SN75182	
DS8820A	SN75182	
DS8830	SN75183	
DS8831	DS8831	
DS8832	DS8832	

SIGNETICS

EXAMPLE OF NOMENCLATURE



SIGNETICS	TI DIRECT REPLACEMENT	TI CLOSEST REPLACEMENT
DM7820	SN55182	
DM7830	SN55183	
DM8820	SN75182	
DM8830	SN75183	
MC1488	SN75188	
MC1489	SN75189	
MC1489A	SN75189A	
N8T13	SN75121	
N8T14	SN75122	
N8T15		SN75150
N8T16		SN75152
N8T23	SN75123	
N8T24	SN75124	

SIGNETICS	TI DIRECT REPLACEMENT	TI CLOSEST REPLACEMENT
N8T26	N8T26	
N8T26A	N8T26A	
S8T13	SN55121	
S8T14	SN55122	
55450B	SN55450B	
55451B	SN55451B	
75S107		SN75107A
75S108		SN75108A
75S207		SN75207
75S208		SN75208
75361A	SN75361A	
75450B	SN75450B	
75451B	SN75451B	

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TEXAS INSTRUMENTS
INCORPORATED

APPLICATION	OUTPUT	DRIVERS PER PACKAGE	TYPE NUMBERS	PAGE NUMBER
EIA Standard RS-422A	Differential	2	SN55158, SN75158	180
			SN75159	184
			uA9638C	276
		4	AM26LS31C	29
			MC3487	57
			SN55151, SN75151	157
			SN55153, SN75153	157
			SN75172	205
			SN75174	215
EIA Committee TR30.1 Draft PN1360 (April 1980)	Differential	4	SN75172	205
			SN75174	215
EIA Standard RS-423A	Single-Ended	2	SN75156†	176
			uA9636AC	269
		4	SN75186†	252
			SN75187†	253
EIA Standard RS-232C	Single-Ended	2	SN75150	153
			SN75156†	176
			uA9636AC	269
		4	SN75186	255
IBM 360/370	Single-Ended	2	SN75123	119
			SN75126†	129
			SN75130†	134
General Purpose	Single-Ended	2	SN55121, SN75121	113
			SN75361A‡	‡
			SN55450B, SN75450B	§
			SN55451B, SN75451B	§
		4	DS7831, DS8831	43
			DS7832, DS8831	43
	Differential	2	DS7831, DS8831	43
			DS7832, DS8831	43
			SN55109A, SN75109A	79
			SN55110A, SN75110A	79
			SN55113, SN75113	87
			SN55114, SN75114	87
			SN55183, SN75183	241
			SN55450B, SN75450B	§
			SN75112	79

†Future Products.
‡For data sheet see *The Interface Circuits Data Book for Design Engineers.*
§For data sheet, see *The Peripheral Driver Data Book for Design Engineers.*

LINE RECEIVER SELECTION GUIDE

APPLICATION	INPUT	RECEIVERS PER PACKAGE	TYPE NUMBERS	PAGE NUMBER
EIA Standard RS-422A	Differential	2	SN75157	177
			uA9637AC	273
		4	AM26LS32AC	33
			AM26LS33AC	33
			MC3486	53
			SN75173	210
			SN75175	220
EIA Committee TR30.1 Draft PN1360 (April 1980)	Differential	4	SN75173	210
			SN75175	220
EIA Standard RS-423A	Single-Ended	2	SN75157	177
			uA9637AC	273
		4	AM26LS32AC	33
			AM26LS33AC	33
			MC3486	53
			SN75173	210
			SN75175	220
EIA Standard RS-232C	Single-Ended	2	SN75152	164
		4	SN75154	171
			SN75189	259
			SN75189A	259
IBM 360/370	Single-Ended	3	SN75124	119
		7	SN75125	125
			SN75127	125
		8	SN75128	130
			SN75129	130
General Purpose	Single-Ended	2	SN55122, SN75122	113
			SN55140, SN75140	145
			SN55141, SN75141	145
			SN55142A, SN75142A	145
			SN55143A, SN75143A	145
	Differential	2	SN55107A, SN75107A	67
			SN55107B, SN75107B	67
			SN55108A, SN75108A	67
			SN55108B, SN75108B	67
			SN55115, SN75115	87
			SN55182, SN75182	241
			SN75207	263
			SN75207B	263
			SN75208	263
			SN75208B	263

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APPLICATION	BUS I/O	TRANSCEIVERS PER PACKAGE	TYPE NUMBERS	PAGE NUMBER
EIA Standard RS-422A	Differential	1	SN75176	225
			SN75177	233
			SN75178	233
EIA Committee TR30.1 Draft PN1360 (April 1980)	Differential	1	SN75176	225
			SN75177	233
			SN75178	233
IEEE Standard 488 GPIB	Single-Ended	4	MC3446	49
		8	SN75160A	189
			SN75161A	195
			SN75162A	195
General Purpose	Single-Ended	4	AM26S10M, AM26S10C	39
			AM26S11M, AM26S11C	39
			N8T26	61
			N8T26A	61
			SN75136	135
			SN55138, SN75138	139
		8	SN75163A	202
	Differential	1	SN55116, SN75116	105
			SN55117, SN75117	105
			SN55118, SN75118	105
			SN55119, SN75119	105

†Future products.

Interfacing to IEEE Standard 488 GPIB

Because of the large number of manufacturers building programmable instruments that must be easily and economically interfaced, there is an overwhelming need for industry-wide standardization. For this reason the General-Purpose Interface Bus (GPIB) defined by IEEE Standard 488 has received wide acceptance in a short time with, at present, an estimated 500 commercially available instruments utilizing the GPIB. IEEE Std 488 has standardized the interface system used to interconnect programmable and non-programmable instruments, computers, and peripherals necessary to build an instrumentation system. This allows a user to purchase instruments from many different manufacturers and then connect them together using off-the-shelf cable. The GPIB uses a 16-line bidirectional bus that carries data at rates of up to 1 megabytes/second on eight lines, and hand-shaking and bus-management signals on the others. Up to 15 instruments can be tied together with a maximum line length of 20 meters. A typical interface arrangement is shown in Figure 1.

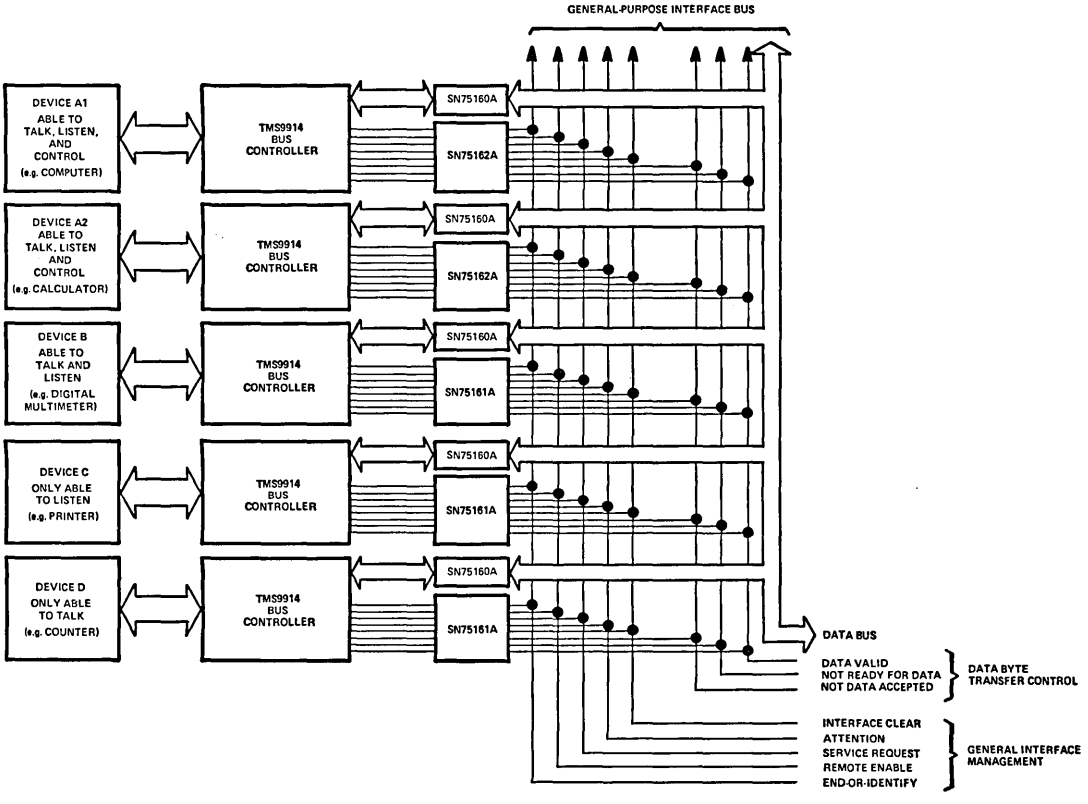

FIGURE 1–TYPICAL INTERFACE ARRANGEMENT

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The TI SN75160 family of bus transceivers is designed to provide the interface between the GPIB (bus) and the bus controller. These transceivers may be used with the TMS 9914 bus controller or any of the other commercially available bus controllers. They provide the simplest method of interfacing because each part is tailored to either the 8-line data bus or the 8-line control bus and they require no extra logic or complicated board layout. All the transceivers in the SN75160 family have several features in common. Each driver output has a built-in termination network required by IEEE Std 488 designed so that, when power is removed from the transceiver, the output presents a high-impedance to the bus. Also, each receiver has a minimum of 400 millivolts hysteresis for additional noise margin. With the SN75160 family it takes only two 20-pin DIP packages to get on the GPIB.

The SN75160A is designed to implement the 8-line data bus and is pin-for-pin compatible with the original SN75160 series but with lower power and faster speeds as illustrated in Figure 2. The direction of data flow is controlled by the Talk Enable (TE) input. All eight channels are simultaneously in the receive mode when TE is low, and data is received from the bus and transferred to the bus controller. When TE is in the high state, all eight channels go to the transmit mode, and data will be transmitted onto the bus. Each driver features a totem-pole output which can actively drive the bus high or low to give the fastest data rates possible. The SN75160A has a Pull-up Enable (PE) input which, when taken low, disables the upper stage of all eight driver outputs to turn them into open-collector-type outputs. The open-collector-output mode does not allow data rates as fast as is possible with the totem-pole, but it does allow more than one instrument to be transmitting on the bus at the same time. This feature is used in parallel polling where up to eight instruments may be polled simultaneously, each responding on a single line of the eight-line data bus, thus greatly speeding up the polling process. They may then be switched back to the totem-pole mode for regular data transmission.

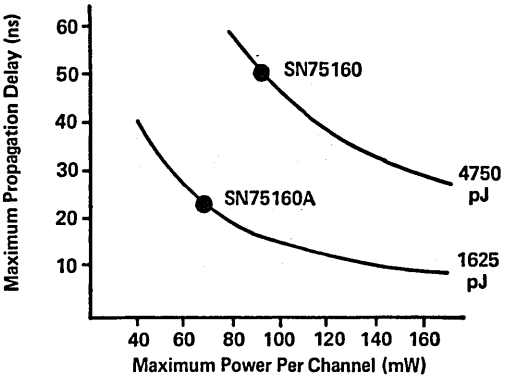

FIGURE 2

The SN75161A is used to implement the eight-line control bus. It includes with the Talk-Enable (TE) and Direction-Control (DC) inputs the necessary logic to enable each channel in the correct direction for the exchange of bus-management and hand-shaking signals. Three of the channels, (NDAC, NRFD, and SRQ) have open-collector driver outputs as required by the IEEE Std 488. These lines are always used in a Wired-OR configuration. The other five channels have totem-pole outputs.

The SN75162A offers an alternate method of implementing the eight-line control bus. It is identical to the SN75161A except that the direction of the REN and IFC channels is controlled by a separate input called the System Controller (SC). With this additional flexibility, control of the entire bus system may be transferred from one instrument to another in multiple-controller systems. Because of this extra input the SN75162A is packaged in a 22-pin DIP.

EIA Standards

There are two basic methods for electronic communication between components of a data processing system: single-ended transmission, which uses only one signal line, and differential transmission, which uses two signal lines. Single-ended transmission is used only for short distances and slower data rates since, as line length increases, it is difficult to distinguish between a valid data signal and invalid signals, such as ground shifts and noise, introduced by the environment. Differential data transmission overcomes these problems. Unwanted signals appear as common-mode levels and are rejected by the differential line receiver.

The Electronic Industries Association (EIA) has developed several specifications to standardize the interface system in data communications. Table 1 shows the key aspects of each of these specifications.

RS-232 was introduced in 1962 and has been widely used throughout the industry. It was developed for single-ended transmission over short distances at slow data rates. Today's higher-performance systems, demanding data transmission at faster rates over longer distances, are rapidly making RS-232 inadequate. The newer standard for single-ended systems, RS-423, extends the maximum data rate to 100 kilobits per second (up to 300 feet) and the maximum distance to 4000 feet (up to 1 kb/s). It also provides wave shaping dependent on data rate and wire length to control reflections and radiated emission or cross-talk. Another improvement of RS-423 is the requirement for high-impedance outputs when component power is off to avoid loading the transmission line.

For data rates over 100 kb/s and for long distances, differential transmission should be used to nullify effects of ground shifts and noise signals, which appear as common-mode voltages on the bus. EIA Standard RS-422 defines a differential interface that allows data rates up to 10 Mb/s (up to 40 feet) and line lengths up to 4000 feet (up to 100 kb/s). Line drivers designed to meet this standard are capable of transmitting a 2-V-minimum differential signal on a twisted-pair line terminated in 100 Ω. The receivers are capable of detecting ±200-mV differential signals in the presence of common-mode levels from –7 V to 7 V.

TABLE 1

SPECIFICATION		RS-232C	RS-423A	RS-422A	EIA Committee TR30.1 Draft Standard PN1360
Mode of operation		Single-ended	Single-ended	Differential	Differential
Number of drivers and receivers allowed on one line		1 Driver, 1 Receiver	1 Driver, 10 Receivers	1 Driver, 10 Receivers	32 Drivers, 32 Receivers
Maximum cable length		50 feet	4000 feet	4000 feet	4000 feet
Maximum data rate		20 kb/s	100 kb/s	10 Mb/s	10 mb/s
Maximum voltage applied to driver output		±25 V	±6 V	–0.25 V to 6 V	–7 V to 12 V
Driver output signal	Loaded	±5 V	±3.6 V	±2 V	±1.5 V
	Unloaded	±15 V	±6 V	±5 V	±5 V
Driver load		3 kΩ to 7 kΩ	450 Ω min	100 Ω	54 Ω
Maximum driver output current (High-impedance state)	Power on	—	—	—	±100 μA
	Power off	V_{max}/300 Ω	±100 μA	±100 μA	±100 μA
Output slew rate		30 V/μs max	Controls provided	—	—
Receiver input voltage range		±15 V	±12 V	–7 V to 7 V	–7 V to 12 V
Receiver input sensitivity		±3 V	±200 mV	±200 mV	±200 mV
Receiver input resistance		3 kΩ to 7 kΩ	4 kΩ min	4 kΩ min	12 kΩ min

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The main limitations of RS-422 occur in systems where output drivers of several components or subassemblies are connected to the same bus line. Ideally, only one driver on a line should be active (high or low) at a time, and all the others should be in a high-impedance state that prevents loading the line even when subassembly power is off. RS-422 does not require that drivers be in a high-impedance state except when the power supply is off, and then only for common-mode bus voltages from −0.25 volts to 6 volts. In systems where large positive and negative common-mode signals can appear on the bus, it is necessary that driver outputs maintain a high impedance over a wide range of common-mode voltage when disabled with power on or when power is off.

Another limitation of RS-422 occurs when more than one driver is enabled. The outputs may be in contention (trying to drive the bus to opposite logic states) or there may be a large difference in common-mode voltages. In either case, relatively large currents can cause excessive power dissipation and possible damage.

EIA Committee TR30.1 is, at the time of this publication, drafting a new standard (Project Number 1360) patterned after RS-422 (See Figure 1) but specified for multipoint interface. It is intended to allow for as many as 32 driver-receiver pairs on a data bus otherwise very similar to that of RS-422. Key features of the new standard are:

- Up to 32 Components Interfaced to One Bus
- Extended Common-Mode Voltage Range with Power On or Off
- Contention Protection for Drivers
- Receiver Sensitivity of ±200 millivolts
- Receiver Input Impedance Increased to 12 kΩ Min

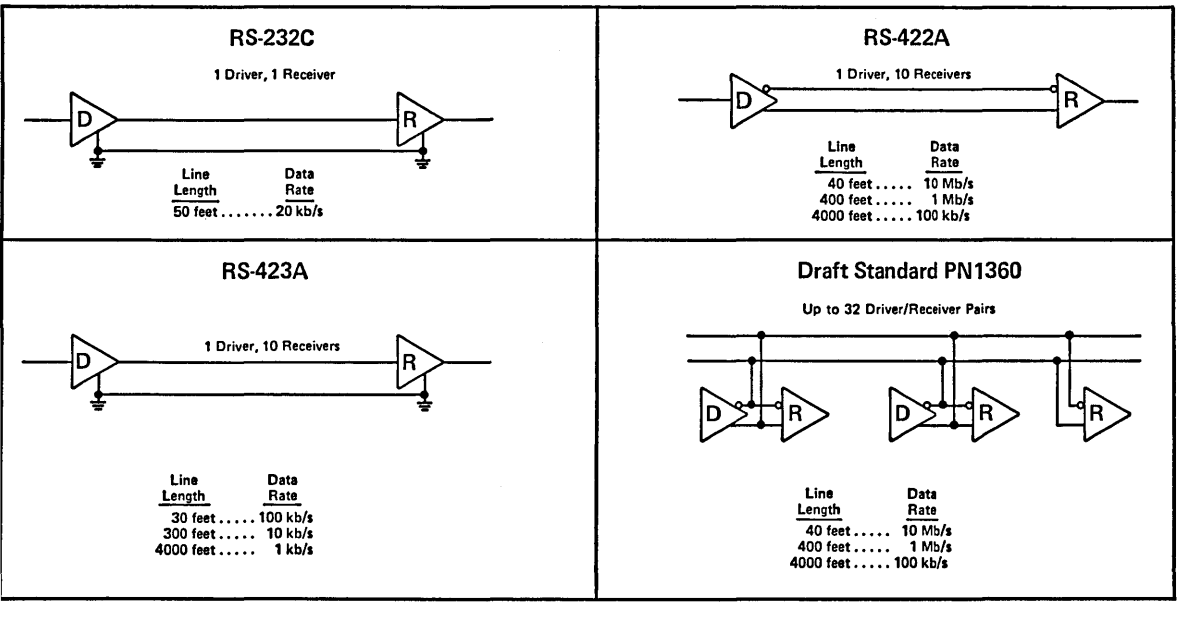

FIGURE 1

The new SN75172 and SN75174 drivers, and SN75173 and SN75175 receivers are available now for systems designed around either RS-422 or present PN1360 requirements. The drivers operate from a single 5-V supply and maintain high output impedance with power on or off. This improved design was achieved without appreciable sacrifice in speed, since they have maximum delay times of 50 ns and rise and fall times of 80 ns, and the data rate can be as high as 4 Mb/s. Also featured is the low maximum power requirement of 79 mW per enabled channel and 53 mW per disabled channel. These drivers provide contention protection through positive- and negative-current limiting and thermal shutdown. Each output is limited to −250 mA sink current and to 500 mA source current over the maximum output voltage range of −7 V to 12 V, and a thermal sensing circuit will cause these devices to go into a disabled state whenever the internal temperature exceeds approximately 150°C.

The SN75173 and SN75175 quadruple receivers are similar to existing RS-422 receivers but have higher input impedance and extended common-mode range without any sacrifice in sensitivity or speed. They feature ±200 mV sensitivity over a common-mode input range of ±12 V, 12 kΩ input impedance, and 35 ns propagation delay. Each receiver has 50 mV input hysteresis for increased noise margin.

Other new devices include the SN75176 transceiver, the equivalent of one SN75172 driver and one SN75173 receiver interconnected (see Figure 2) in a single 8-pin package. The SN75177 and SN75178 transceivers are designed for use as repeaters to extend the maximum cable distance. The enable controls on all these devices are complementary to allow bidirectional data communication.

Figure 1 illustrates how several of these new devices might be combined in a typical bus system. The SN75177 and SN75178 are connected to form a bidirectional repeater to extend the cable length. Other devices interface with terminals or MODEMs and drive peripherals. The twisted-pair line should normally be terminated at each end of the main wire lengths in 120-Ω resistors.

Texas Instruments manufactures a wide variety of integrated circuits designed to meet the requirements of EIA Standards RS-232C, RS-422A, RS-423A, and draft standard PN1360. This variety offers flexibility, choice, and compatibility that will provide cost-effective solutions to many interfacing problems.

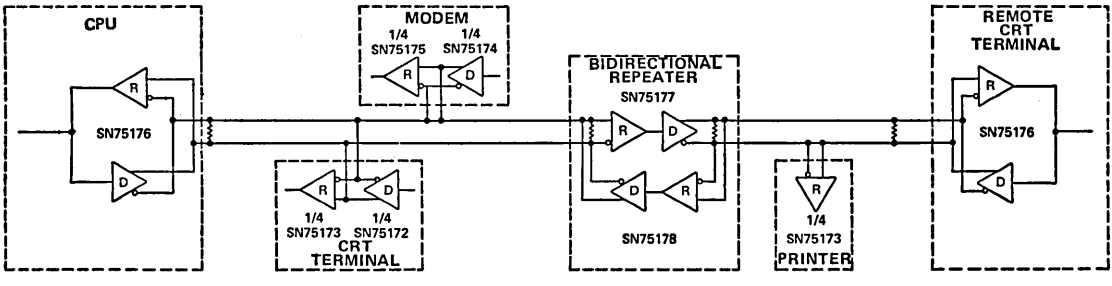

FIGURE 2

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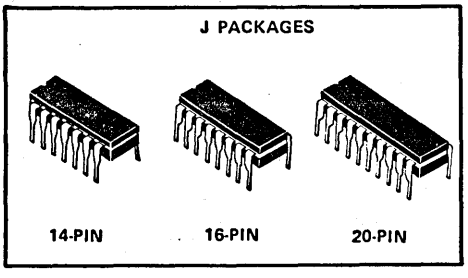
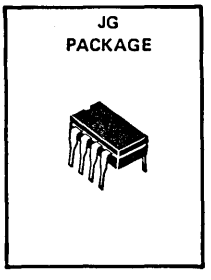
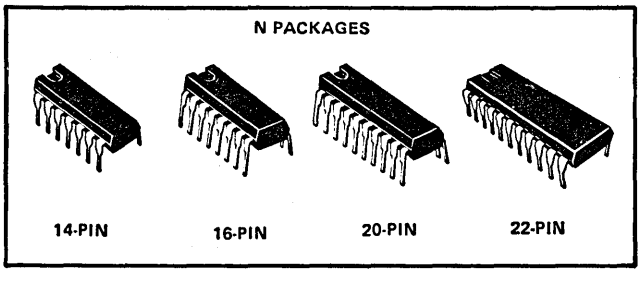
THERMAL RESISTANCE

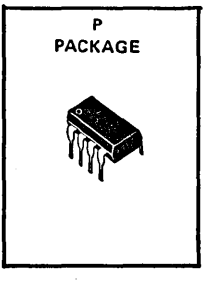
PACKAGE	PINS	JUNCTION-TO-CASE THERMAL RESISTANCE $R_{\theta JC}$ (°C/W)	JUNCTION-TO-AMBIENT THERMAL RESISTANCE $R_{\theta JA}$ (°C/W)
J ceramic dual-in-line (glass-mounted chips)	14 thru 20	60	122
J ceramic dual-in-line† (alloy-mounted chips)	14 thru 20	29†	91†
JG ceramic dual-in-line (glass-mounted chips)	8	58	151
JG ceramic dual-in-line† (alloy-mounted chips)	8	26†	119†
N plastic dual-in-line	14 thru 20	44	108
	22	39	94
P plastic dual-in-line	8	45	125

†In addition to those products so designated on their data sheets, all devices having a type number prefix of "SNC" or "SNM," or a suffix of "/883" have alloy-mounted chips.





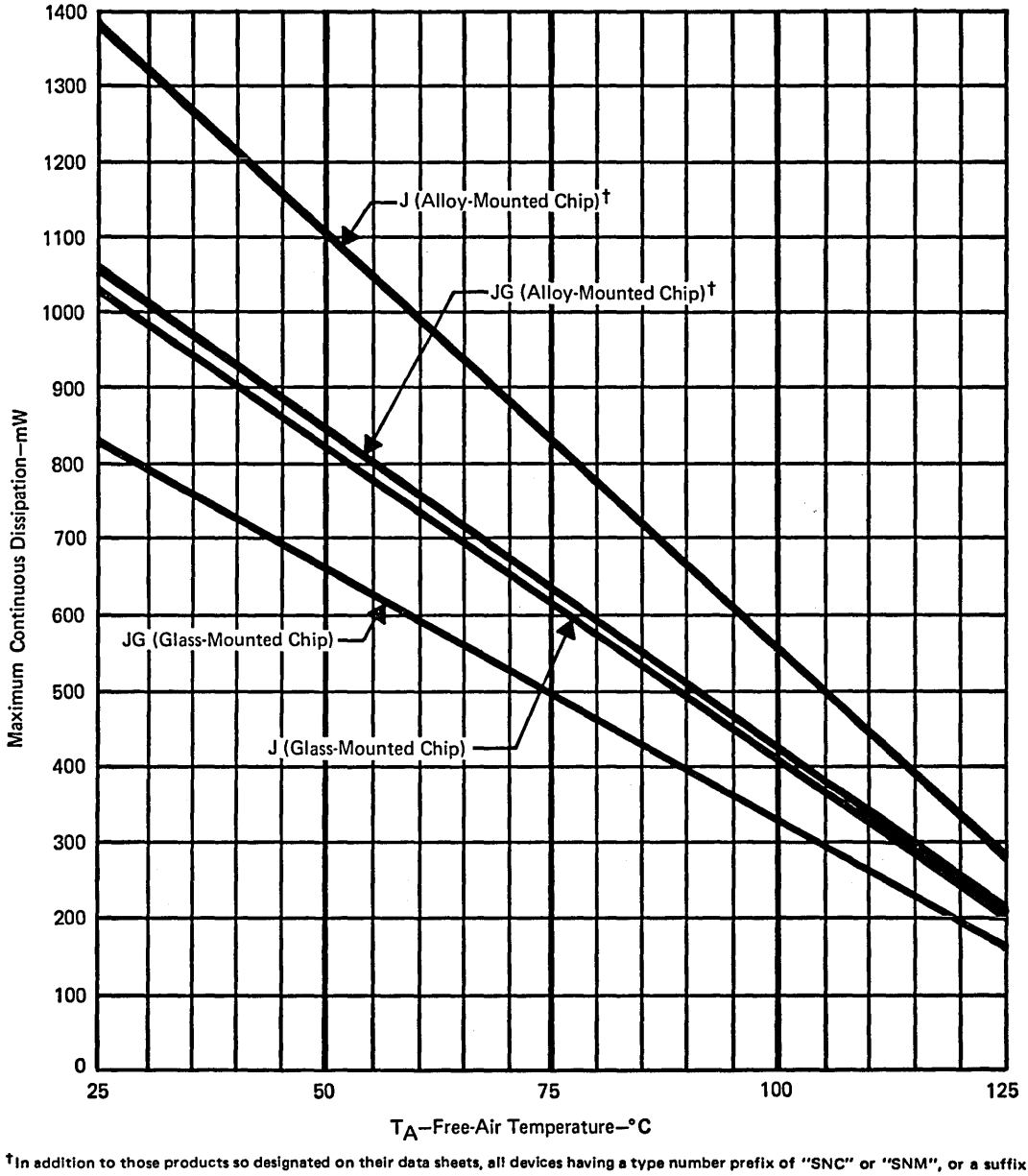




CERAMIC DUAL-IN-LINE PACKAGES

These curves are for use with the continuous dissipation ratings specified on the individual data sheets. Those ratings apply up to the temperature at which the rated level intersects the appropriate derating curve or the maximum operating free-air temperature.

DISSIPATION DERATING CURVE



†In addition to those products so designated on their data sheets, all devices having a type number prefix of "SNC" or "SNM", or a suffix of "/883" have alloy-mounted chips.

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PLASTIC DUAL-IN-LINE PACKAGES

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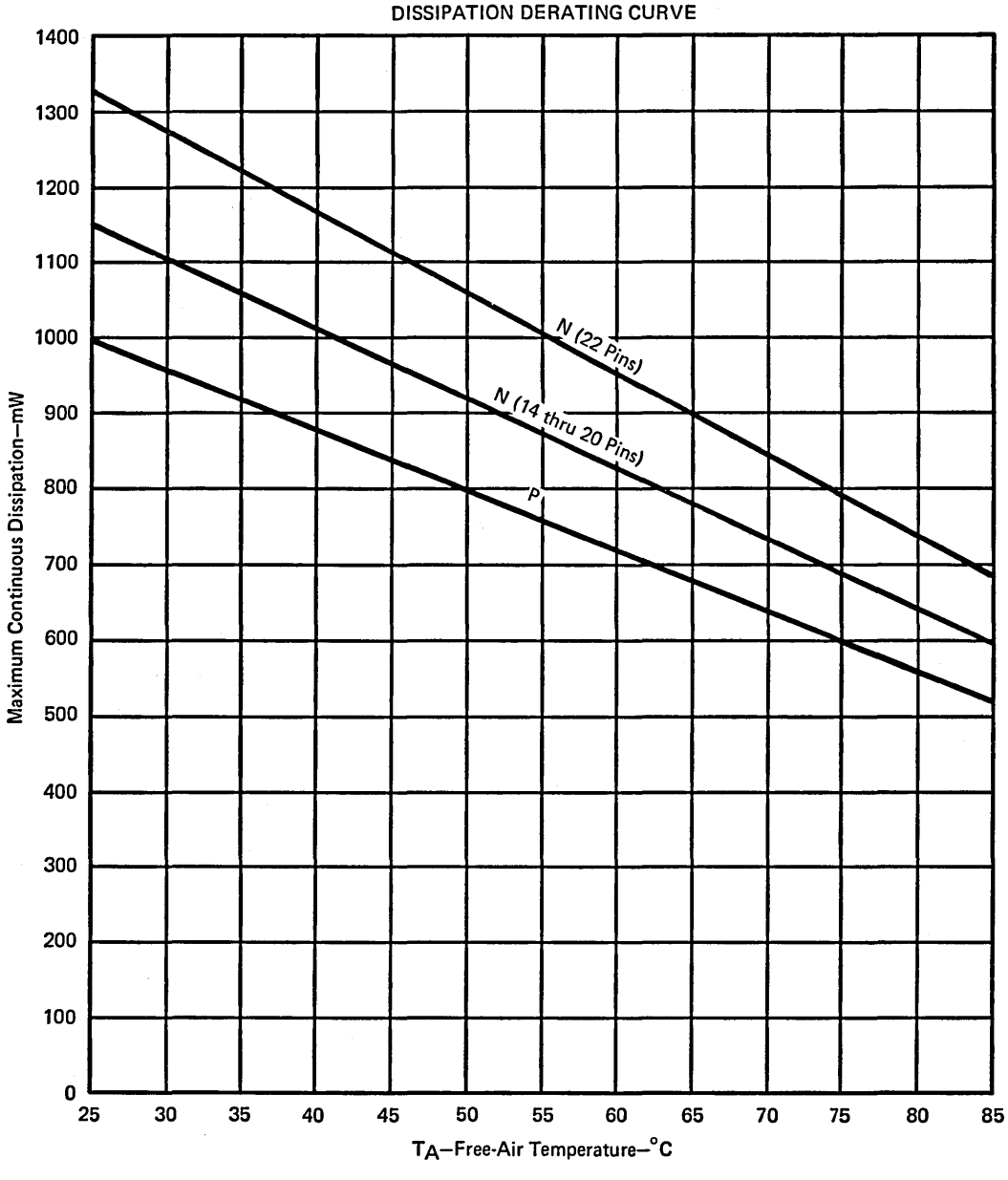

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WASHINGTON: Redmond, United Components (206) 885 1985; Seattle, Almac/Stroum Electronics (206) 763-2300, Kierulff Electronics (206) 575-4420; Tukwila, Arrow Electronics (206) 575-0907.

WISCONSIN: Oak Creek, Arrow Electronics (414) 764-6600; Hall-Mark/Milwaukee (414) 761-3000; Waukesha, Kierulff Electronics (414) 784-8160.

CANADA: Calgary, Cam Gard Supply (403) 287-0520; Future Electronics (403) 259-6408; Downsview, CESCO Electronics (416) 661-0220; Edmonton, Cam Gard Supply (403) 426-1805; Halifax, Cam Gard Supply (902) 454-8581; Kamloops, Cam Gard Supply (604) 372-3338; Moncton, Cam Gard Supply (506) 855-2200; Montreal, CESCO Electronics (514) 735-5511; Future Electronics (514) 731-7441; Ottawa, CESCO Electronics (613) 729-5118; Future Electronics (613) 820-8313; Quebec City, CESCO Electronics (418) 687-4231; Regina, Cam Gard Supply (306) 525-1317; Saskatoon, Cam Gard Supply (306) 652-6424; Toronto, Future Electronics (416) 663-5563; Vancouver, Cam Gard Supply (604) 291-1441; Future Electronics (604) 438-5545; Winnipeg, Cam Gard Supply (204) 786-8481. W

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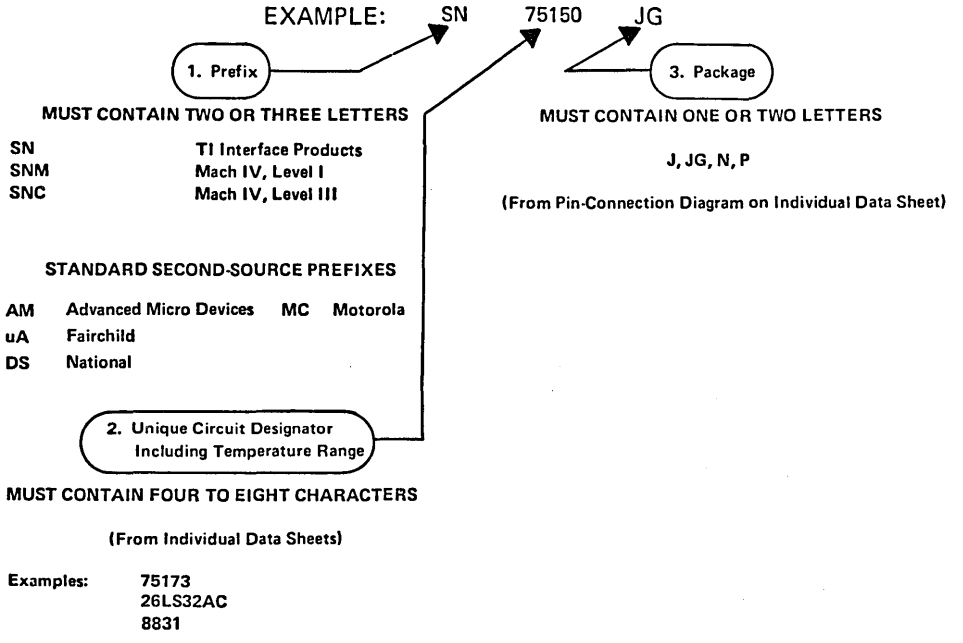
ORDERING INSTRUCTIONS

Electrical characteristics presented in this data book apply for the circuit type(s) listed in the page heading, unless otherwise noted, regardless of package. The availability of a circuit function in a particular package is indicated by an alphabetical reference above the pin-connection diagram(s). These alphabetical references refer to mechanical outline drawings shown in this section.

Factory orders for circuits described in this data book should include a three-part type number as explained in the following example.



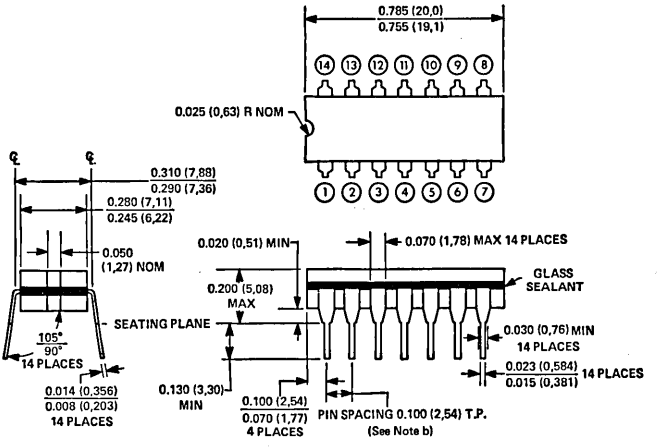
Circuits are shipped in one of the carriers shown below. Unless a specific method of shipment is specified by the customer (with possible additional costs), circuits will be shipped in the most practical carrier.

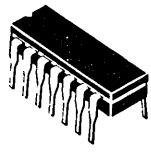
—Slide Magazines
—A-Channel Plastic Tubing
—Sectioned Cardboard Box
—Individual Plastic Box

J ceramic dual-in-line packages

These hermetically sealed dual-in-line packages consist of a ceramic base, ceramic cap, and a 14-, 16-, or 20-lead frame. Hermetic sealing is accomplished with glass. The packages are intended for insertion in mounting-hole rows on 0.300 (7,62) centers (see Note a). Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads require no additional cleaning or processing when used in soldered assembly.

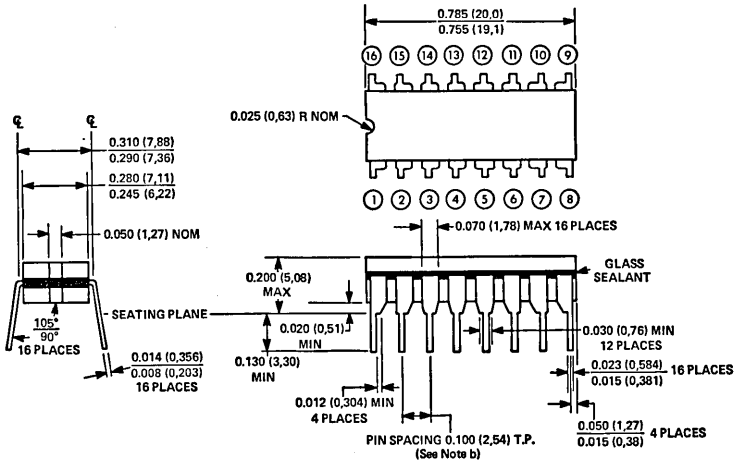
14-PIN J CERAMIC

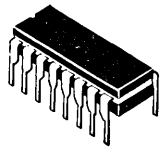




Falls within JEDEC TO-116 and MO-001AA Dimensions

16-PIN J CERAMIC





NOTES: a. All dimensions are in inches and parenthetically in millimeters. Inch dimensions govern.
b. Each pin centerline is located within 0.010 (0,26) of its true longitudinal position.

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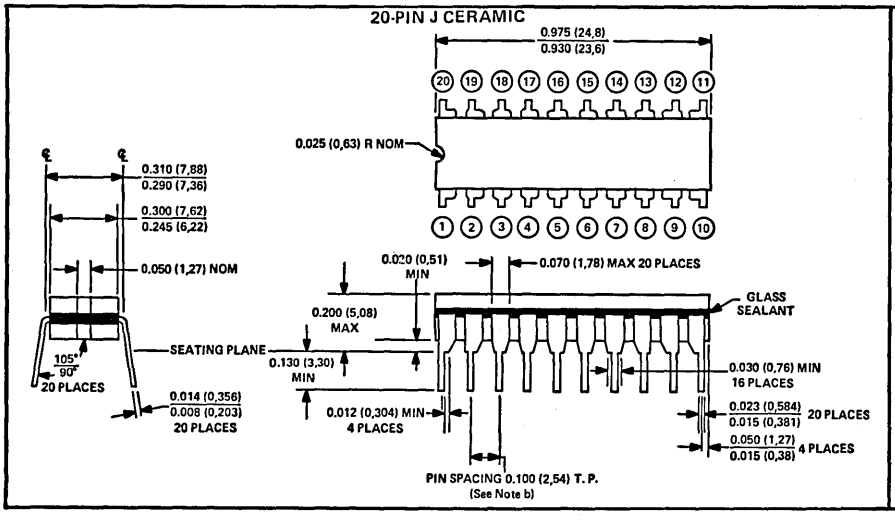
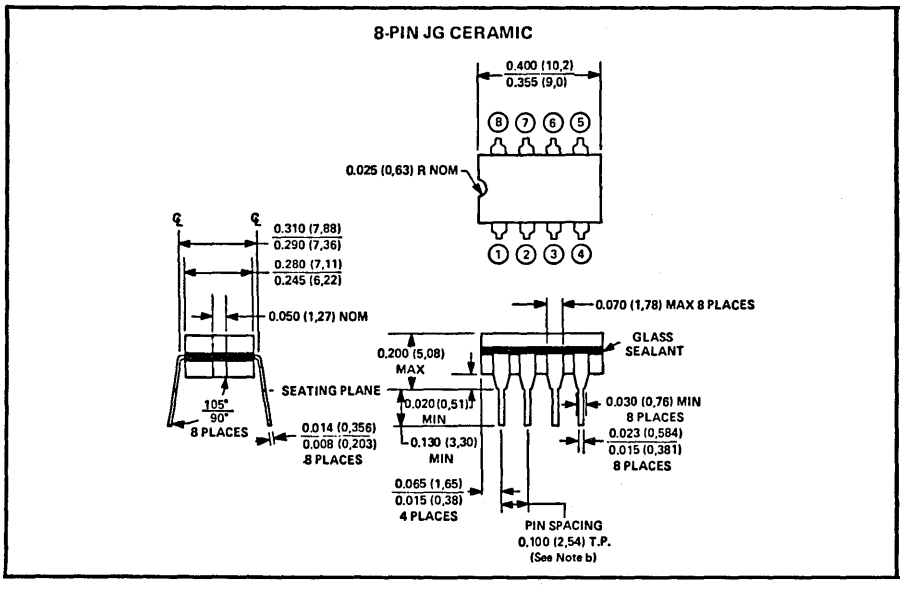
J ceramic dual-in-line packages (continued)



JG ceramic dual-in-line package

This hermetically sealed dual-in-line package consists of a ceramic base, ceramic cap, and 8-lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 0.300 (7,62) centers (see Note a). Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Tin-plated ("bright-dipped") leads require no additional cleaning or processing when used in soldered assembly.

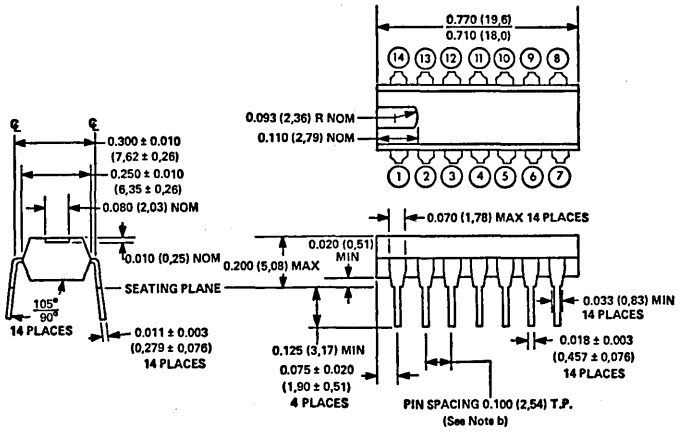


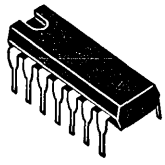
NOTES: a. All dimensions are in inches and parenthetically in millimeters. Inch dimensions govern.
b. Each pin centerline is located within 0.010 (0,26) of its true longitudinal position.

N plastic dual-in-line packages

These dual-in-line packages consist of a circuit mounted on a 14-, 16-, 20-, or 22-lead frame and encapsulated within an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics remain stable when operated in high-humidity conditions. The packages are intended for insertion in mounting-hole rows on 0.300 (7,62) centers (see Note a). Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

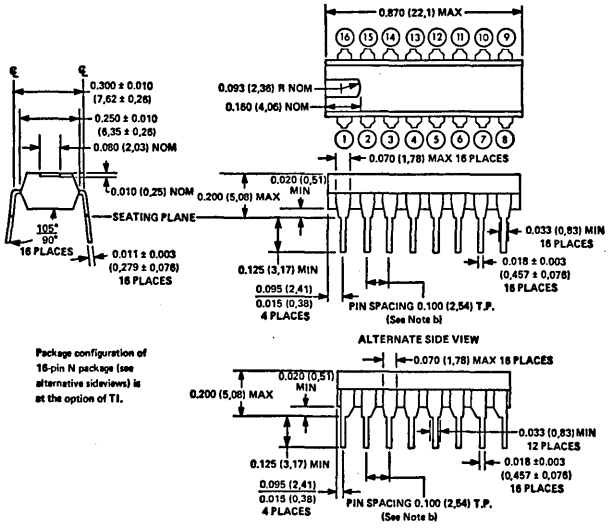
14-PIN N PLASTIC



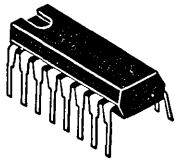


Falls Within JEDEC TO-116 and MO-001AA Dimensions

16-PIN N PLASTIC



Package configuration of 16-pin N package (see alternative sideviews) is at the option of TI.



NOTES: a. All dimensions are in inches and parenthetically in millimeters. Inch dimensions govern.

b. Each pin centerline is located within 0.010 (0,26) of its true longitudinal position.

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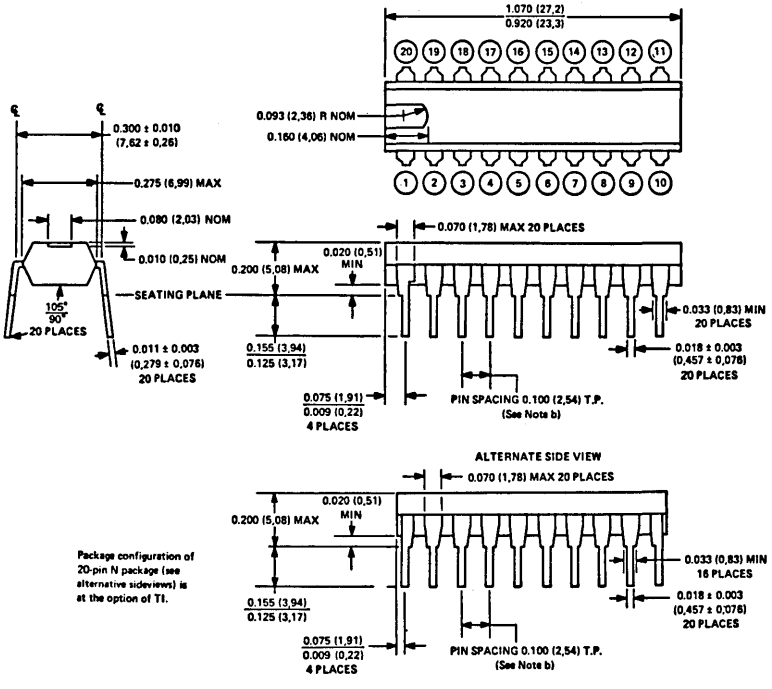
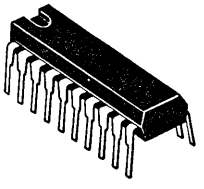
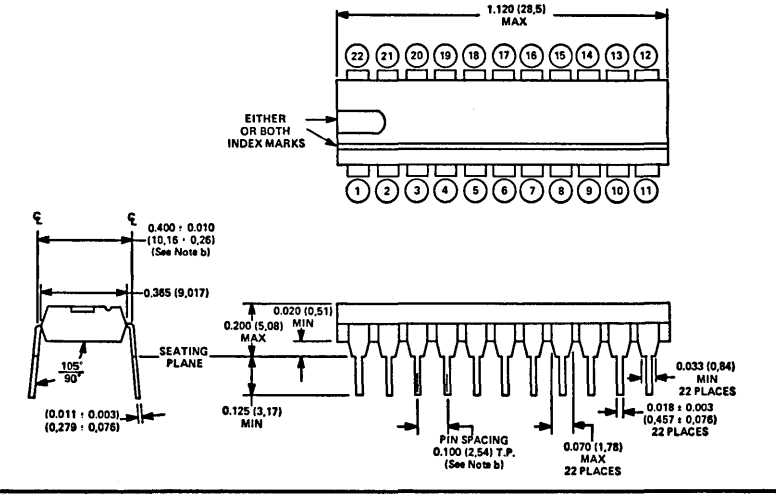
N dual-in-line plastic packages (continued)

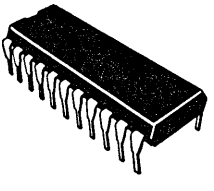
20-PIN N PLASTIC





22-PIN N PLASTIC

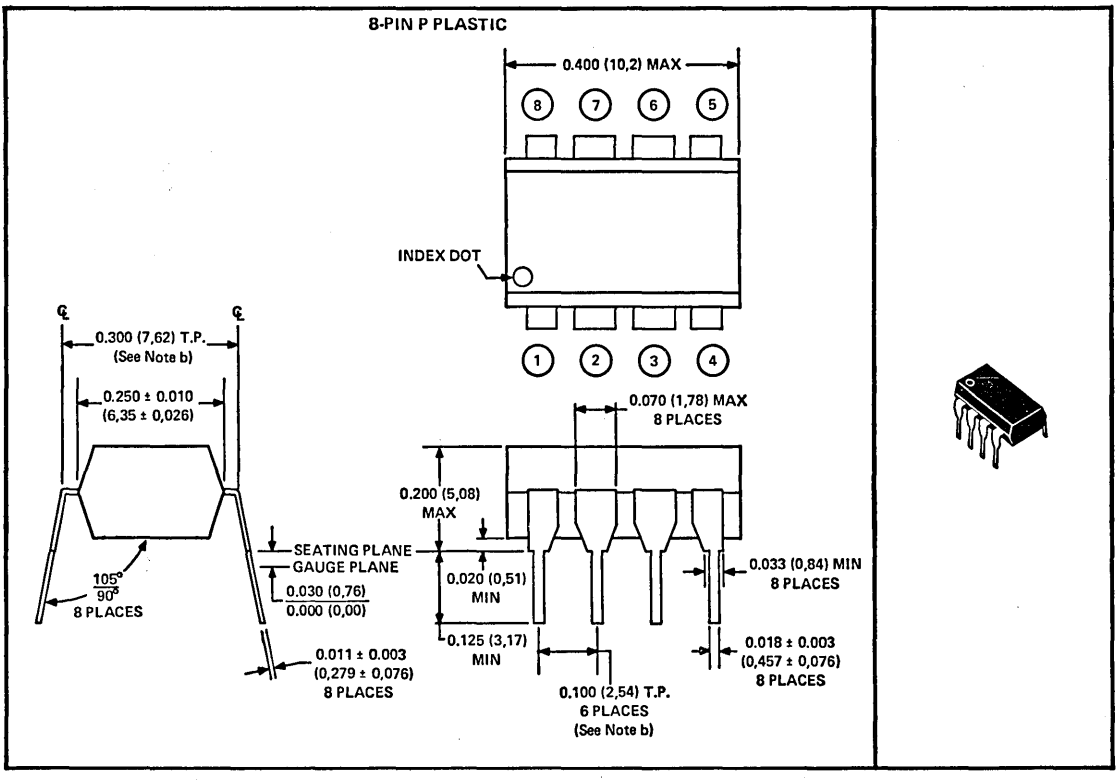




NOTES: a. All dimensions are in inches and parenthetically in millimeters. Inch dimensions govern.
b. Each pin centerline is located within 0.010 (0,26) of its true longitudinal position.

P dual-in-line plastic package

This dual-in-line package consists of a circuit mounted on an 8-lead frame and encapsulated in an electrically nonconductive plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics remain stable when operated under high-humidity conditions. This package is intended for insertion in mounting hole rows on 0.300 (7,62) centers (see Note a). Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Silver-plated leads require no additional cleaning or processing when used in soldered assembly.



NOTES: a. All dimensions are in inches and parenthetically in millimeters. Inch dimensions govern.
b. Each pin centerline is within 0.005 (0,127) radius of true position at the gauge plane with maximum material condition and unit installed.

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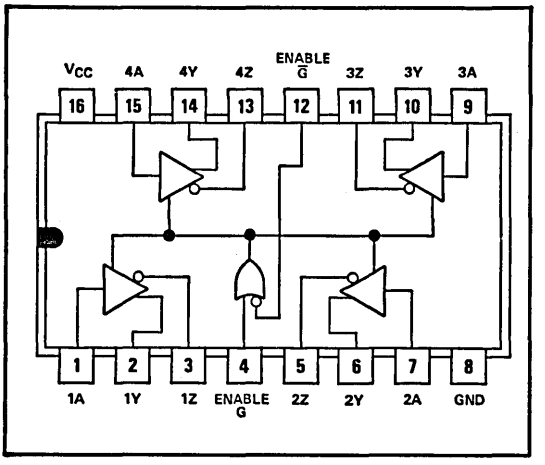
TYPES AM26LS31M, AM26LS31C
QUADRUPLE DIFFERENTIAL LINE DRIVERS

BULLETIN NO. DL-S 12671, JANUARY 1979 – REVISED SEPTEMBER 1980

- Meets EIA Standard RS-422A
- Operates from a Single 5-V Supply
- TTL-, DTL-Compatible
- Complementary Outputs
- High Output Impedance in Power-Off Conditions
- Complementary Output Enable Inputs

AM26LS31M . . . J
AM26LS31C . . . J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



description

The AM26LS31M and AM26LS31C are quadruple complementary-output line drivers designed to meet the requirements of EIA Standard RS-422 and Federal Standard 1020. The three-state outputs have high-current capability for driving balanced lines such as twisted-pair or parallel-wire transmission lines, and they provide a high-impedance state in the power-off condition. The enable function is common to all four drivers and offers a choice of active-high or active-low inputs. Low-power Schottky circuitry reduces power consumption without sacrificing speed.

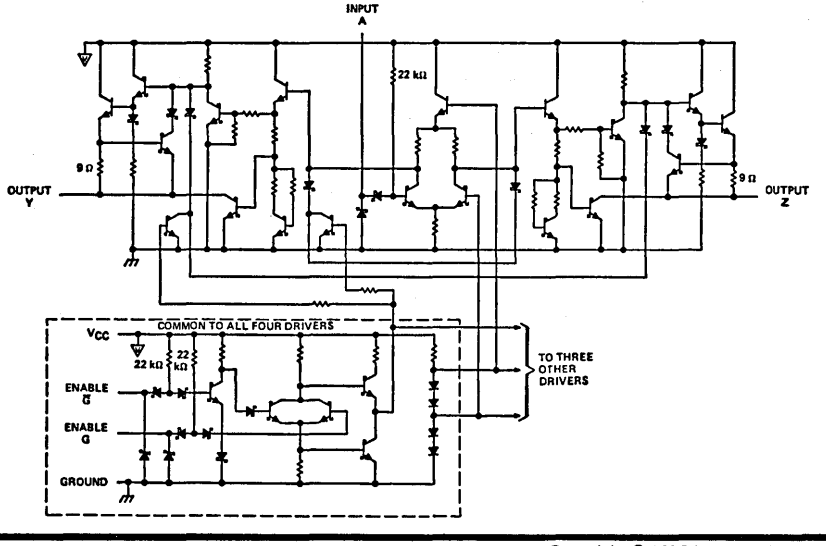
The AM26LS31M is characterized for operation over the full military temperature range of −55°C to 125°C, the AM26LS31C is characterized for operation from 0°C to 70°C.

FUNCTION TABLE (EACH DRIVER)

INPUT	ENABLES		OUTPUTS	
A	G	$\overline{G}$	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

H = high level
L = low level
X = irrelevant
Z = high impedance (off)

schematic (each driver)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 7 V
Output off-state voltage . . . . . 5.5 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 1 W
Operating free-air temperature range: AM26LS31M . . . . . −55°C to 125°C
AM26LS31C . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch (1,6 mm) from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1/16 inch (1,6 mm) from case for 10 seconds: N package . . . . . 260°C

NOTES: 1. All voltage values, except differential output voltage V_{OD}, are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, refer to the Dissipation Derating Table. In the J package, AM26LS31M chips are alloy-mounted; AM26LS31C chips are glass-mounted.

DISSIPATION DERATING TABLE

PACKAGE	POWER RATING	DERATING FACTOR	ABOVE T_A
J (Alloy-Mounted Chip)	1000 mW	11.0 mW/°C	59°C
J (Glass-Mounted Chip)	1000 mW	8.2 mW/°C	28°C
N	1000 mW	9.2 mW/°C	41°C

recommended operating conditions

	AM26LS31M			AM26LS31C			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−20			−20	mA
Low-level output current, I_{OL}			20			20	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN,	I_{OH} = −20 mA	2.5			V
V_{OL}	Low-level output voltage	V_{CC} = MIN,	I_{OL} = 20 mA			0.5	V
I_{OZ}	Off-state (high-impedance-state) output current	V_{CC} = MAX	V_O = 0.5 V			−20	μA
			V_O = 2.5 V			20	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 7 V			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			−0.36	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−30		−150	mA
I_{CC}	Supply current (both drivers)	V_{CC} = MAX,	All outputs disabled		32	80	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V and T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

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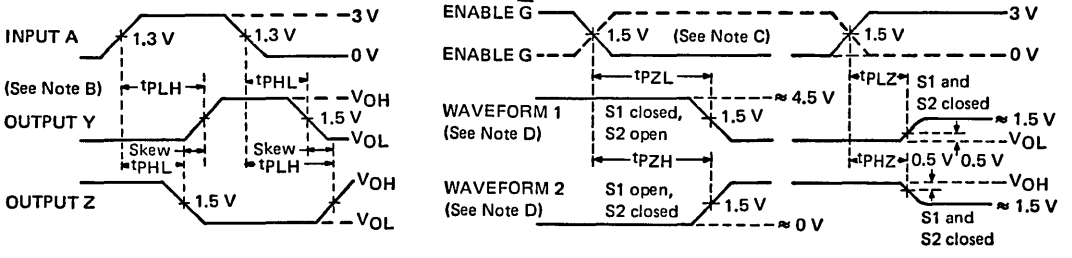
switching characteristics, V_{CC} = 5 V, T_A = 25°C

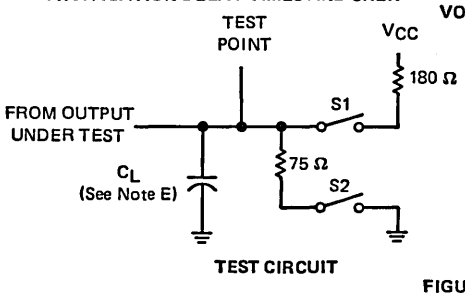
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 30 pF, See Figure 1, S1 and S2 open		14	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output			14	20	ns
	Output-to-output skew			1	6	ns
t_{PZH}	Output enable time to high level	C_L = 30 pF, R_L = 75 Ω, See Figure 1		25	40	ns
t_{PZL}	Output enable time to low level	C_L = 30 pF, R_L = 180 Ω, See Figure 1		37	45	ns
t_{PHZ}	Output disable time from high level	C_L = 10 pF, See Figure 1, S1 and S2 closed		21	30	ns
t_{PLZ}	Output disable time from low level			23	35	ns

PARAMETER MEASUREMENT INFORMATION



PROPAGATION DELAY TIMES AND SKEW

ENABLE AND DISABLE TIMES



TEST CIRCUIT

VOLTAGE WAVEFORMS

NOTES: A. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_{out} ≈ 50 Ω, t_r ≤ 15 ns, and t_f ≤ 6 ns.

B. When measuring propagation delay times and skew, switches S1 and S2 are open.

C. Each enable is tested separately.

D. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

E. C_L includes probe and jig capacitance.

FIGURE 1–SWITCHING TIMES

TYPICAL CHARACTERISTICS†

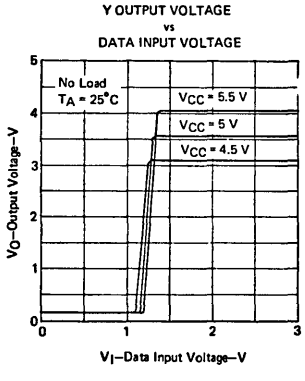


FIGURE 2

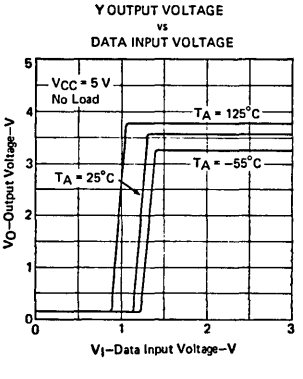


FIGURE 3

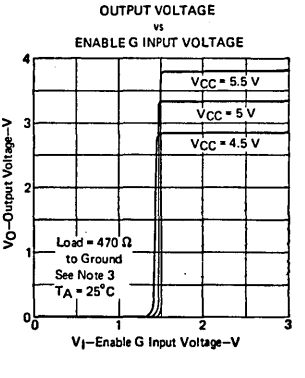


FIGURE 4

NOTE 3: The A input is connected to V_{CC} during the testing of the Y outputs and to ground during testing of the Z outputs.

†Data for temperatures below 0°C and above 70°C are applicable to AM26LS31M circuits only.

TYPICAL CHARACTERISTICS†

OUTPUT VOLTAGE vs ENABLE G INPUT VOLTAGE

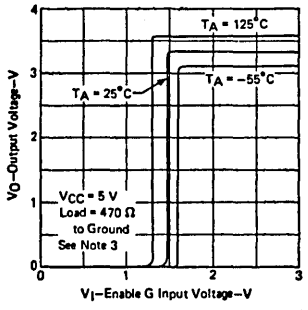


FIGURE 5

OUTPUT VOLTAGE vs ENABLE G INPUT VOLTAGE

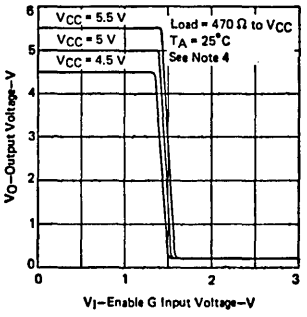


FIGURE 6

OUTPUT VOLTAGE vs ENABLE G INPUT VOLTAGE

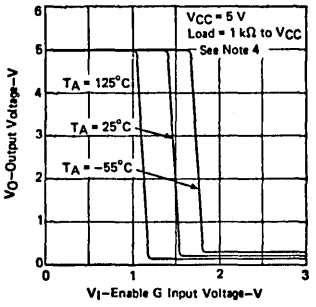


FIGURE 7

HIGH-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

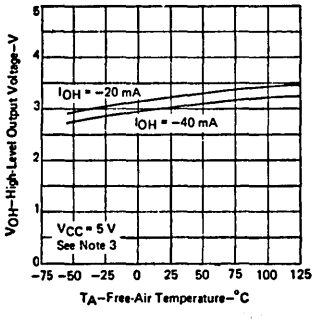


FIGURE 8

HIGH-LEVEL OUTPUT VOLTAGE vs OUTPUT CURRENT

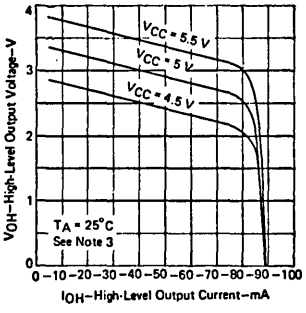


FIGURE 9

LOW-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

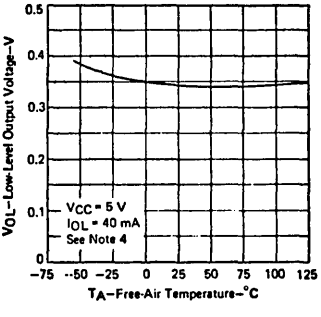


FIGURE 10

LOW-LEVEL OUTPUT VOLTAGE vs OUTPUT CURRENT

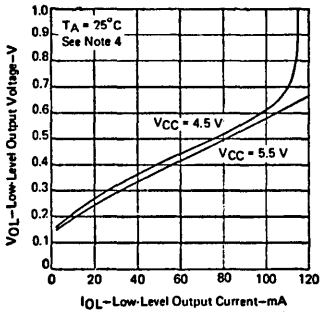


FIGURE 11

SUPPLY CURRENT vs SUPPLY VOLTAGE

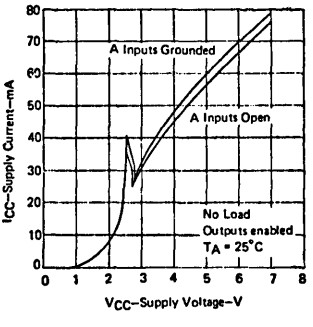


FIGURE 12

SUPPLY CURRENT vs SUPPLY VOLTAGE

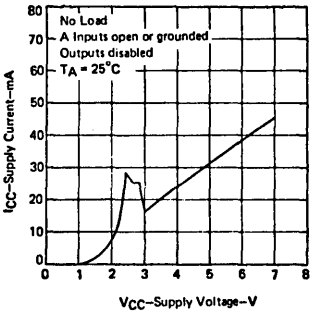


FIGURE 13

NOTES: 3. The A input is connected to V_{CC} during the testing of the Y outputs and to ground during testing of the Z outputs.
4. The A input is connected to ground during the testing of the Y outputs and to V_{CC} during the testing of the Z outputs.

†Data for temperature below 0°C and above 70°C are applicable to AM26LS31M circuits only.

TEXAS INSTRUMENTS
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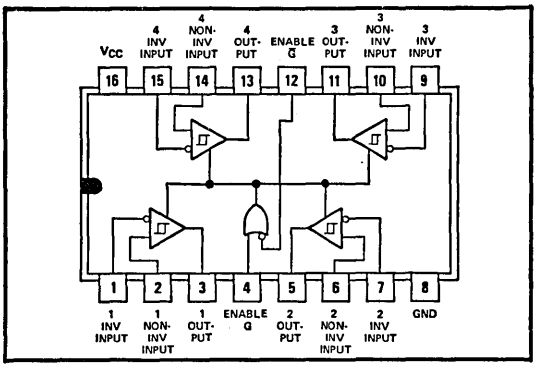
TYPES AM26LS32AC, AM26LS33AC
QUADRUPLE DIFFERENTIAL LINE RECEIVERS

BULLETIN NO. DL-S 12655, OCTOBER 1980

- AM26LS32AC Meets EIA Standards RS-422A and RS-423A
- AM26LS32AC has ±7-V Common-Mode Range with ±200-mV Sensitivity
- AM26LS33AC has ±15-V Common-Mode Range with ±500 mV Sensitivity
- Input Hysteresis . . . 50 mV Typical
- Operates From a Single 5-V Supply
- Low-Power Schottky Circuitry
- 3-State Outputs
- Complementary Output Enable Inputs
- Input Impedance . . . 12 kΩ Min
- Designed to be Interchangeable with Advanced Micro Devices AM26LS32C and AM26LS33C

J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



FUNCTION TABLE (EACH RECEIVER)

DIFFERENTIAL INPUT	ENABLES G	ENABLES $\overline{G}$	OUTPUT
$V_{ID} \geq V_{TH}$	H	X	H
	X	L	H
$V_{TL} < V_{ID} < V_{TH}$	H	X	?
	X	L	?
$V_{ID} \leq V_{TL}$	H	X	L
	X	L	L
X	L	H	Z

H = high level, L = low level, X = irrelevant
Z = high impedance (off), ? = indeterminate

description

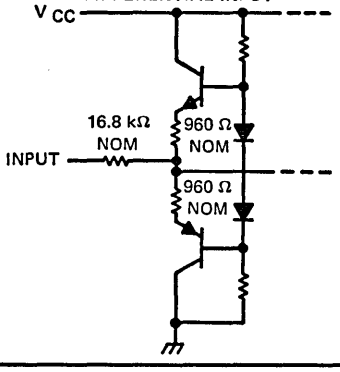
The AM26LS32AC and AM26LS33AC are quadruple line receivers for balanced and unbalanced digital data transmission. The enable function is common to all four receivers and offers a choice of active-high or active-low input. Three-state outputs permit connection directly to a bus-organized system. Fail-safe design ensures that if the inputs are open, the outputs will always be high.

Compared to the AM26LS32C and the AM26LS33C, the AM26LS32AC and AM26LS33AC incorporate an additional stage of amplification to improve sensitivity. The input impedance has been increased resulting in less loading of the bus line. The additional stage has increased propagation delay; however, this will not affect interchangeability in most applications.

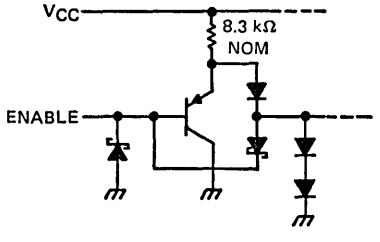
The AM26LS32AC and the AM26LS33AC are characterized for operation from 0°C to 70°C.

schematics of inputs and outputs

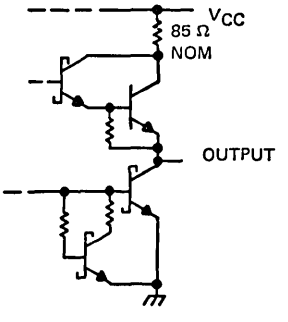
EQUIVALENT OF EACH DIFFERENTIAL INPUT



EQUIVALENT OF EACH ENABLE INPUT



TYPICAL OF ALL OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage, any differential input . . . . . ±25 V
Differential input voltage (see Note 2) . . . . . ±25 V
Enable input voltage . . . . . 7 V
Low-level output current . . . . . 50 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3) . . . . . 1 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch (1,6 mm) from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1/16 inch (1,6 mm) from case for 10 seconds: N package . . . . . 260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Differential voltage values are at the noninverting terminal with respect to the inverting terminal.
3. For operation above 25°C free-air temperature, refer to Dissipation Derating Table. In the J package the chips are glass-mounted.

DISSIPATION DERATING TABLE

PACKAGE	POWER RATING	DERATING FACTOR	ABOVE T_A
J (Glass-Mounted Chip)	1000 mW	8.2 mW/°C	28°C
N	1000 mW	9.2 mW/°C	41°C

recommended operating conditions

	AM26LS32AC			AM26LS33AC			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.75	5	5.25	4.75	5	5.25	V
Common-mode input voltage, V_{IC}			±7			±15	V
High-level output current, I_{OH}			−440			−440	μA
Low-level output current, I_{OL}			8			8	mA
Operating free-air temperature, T_A	0		70	0		70	°C

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electrical characteristics over recommended ranges of V_{CC}, V_{IC}, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{TH}	Differential input high-threshold voltage	V_{OH} = 2.7 V,	I_{OH} = −440 μA	AM26LS32AC			0.2	V
				AM26LS33AC			0.5	
V_{TL}	Differential input low-threshold voltage	V_{OL} = 0.45 V,	I_{OL} = 8 mA	AM26LS32AC	−0.2‡			V
				AM26LS33AC	−0.5‡			
$V_{T+} - V_{T-}$	Hysteresis§					50		mV
V_{IH}	High-level enable input voltage				2			V
V_{IL}	Low-level enable input voltage						0.8	V
V_{IK}	Enable input clamp voltage	V_{CC} = 4.75 V,	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC} = 4.75 V, $V_{I(\overline{G})}$ = 0.8 V,	V_{ID} = 1 V, I_{OH} = −440 μA		2.7	3.5		V
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V, $V_{I(\overline{G})}$ = 0.8 V	V_{ID} = −1 V,	I_{OL} = 4 mA			0.4	V
				I_{OL} = 8 mA			0.45	
I_{OZ}	Off-state (high-impedance-state) output current	V_{CC} = 5.25 V,		V_O = 2.4 V			20	μA
				V_O = 0.4 V			−20	
I_I	Line input current	V_I = 15 V,	Other input at −10 V to 15 V				1.2	mA
		V_I = −15 V,	Other input at −15 V to 10 V				−1.7	
$I_{I(EN)}$	Enable input current	V_I = 5.5 V					100	μA
I_{IH}	High-level enable current	V_I = 2.7 V					20	μA
I_{IL}	Low-level enable current	V_I = 0.4 V					−0.36	mA
r_i	Input resistance	V_{IC} = −15 V to 15 V,	One input to AC ground		12	15		kΩ
I_{OS}	Short-circuit output current¶	V_{CC} = 5.25 V,			−15		−85	mA
I_{CC}	Supply current	V_{CC} = 5.25 V, All outputs disabled	Data inputs at 0 V,			52	70	mA

†All typical values are at V_{CC} = 5 V, T_A = 25° C, and V_{IC} = 0.

‡The algebraic convention, where the less-positive (more-negative) limit is designated as minimum, is used in this data sheet for threshold levels only.

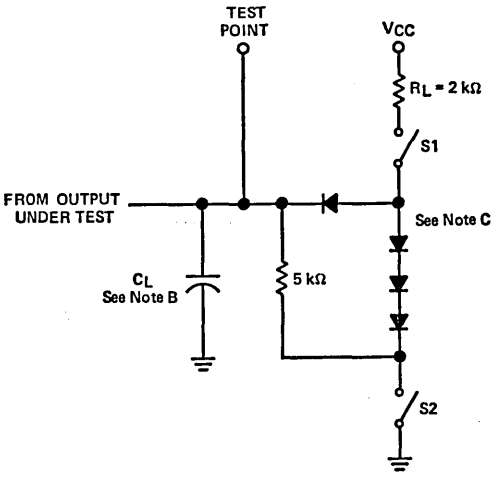
§Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}. See Figures 10 and 11.

¶Not more than one output should be shorted at a time.

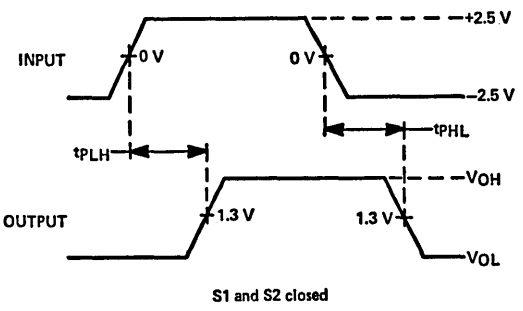
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF,	See Figure 1		20	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output				22	35	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF,	See Figure 1		17	22	ns
t_{PZL}	Output enable time to low level				20	25	ns
t_{PHZ}	Output disable time from high level	C_L = 5 pF,	See Figure 1		21	30	ns
t_{PLZ}	Output disable time from low level				30	40	ns

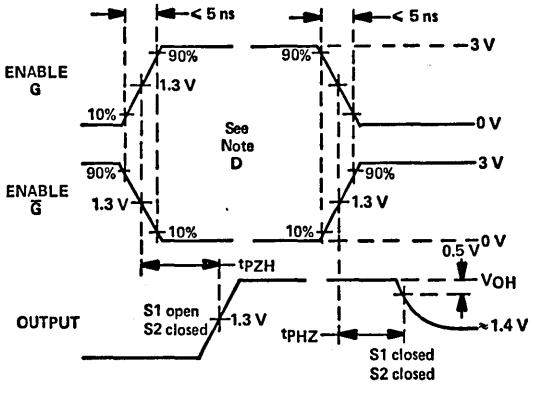
PARAMETER MEASUREMENT INFORMATION



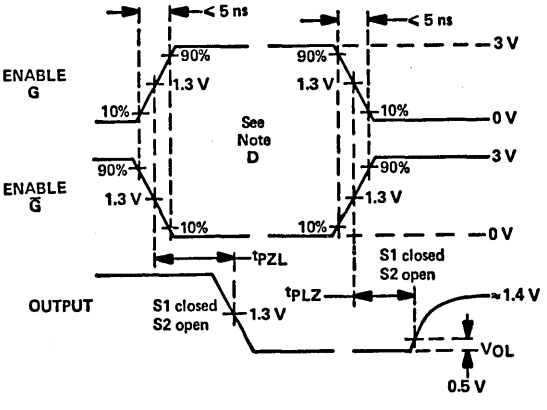
TEST CIRCUIT



VOLTAGE WAVEFORMS FOR t_{PLH}, t_{PHL}



VOLTAGE WAVEFORMS FOR t_{PHZ}, t_{PZH}



VOLTAGE WAVEFORMS FOR t_{PLZ}, t_{PZL}

NOTES: A. The pulse generator has the following characteristics: Z_{out} = 50 Ω, PRR = 1 MHz, t_w = 0.5 μs.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or equivalent.
D. Enable G is tested with $\overline{G}$ high; $\overline{G}$ is tested with G low.

FIGURE 1

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TYPICAL CHARACTERISTICS

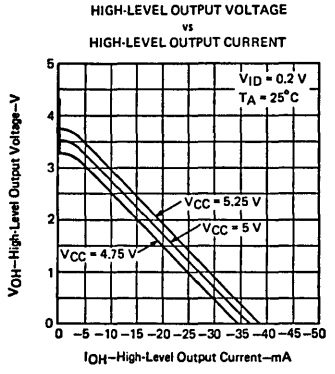


FIGURE 2

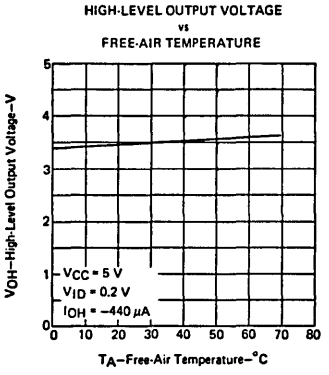


FIGURE 3

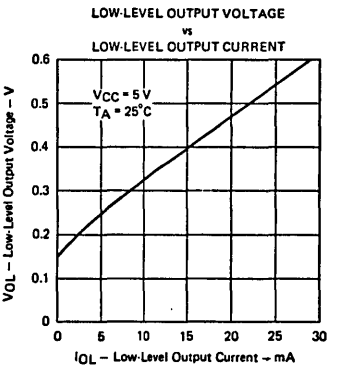


FIGURE 4

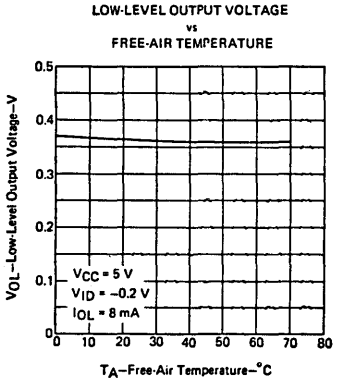


FIGURE 5

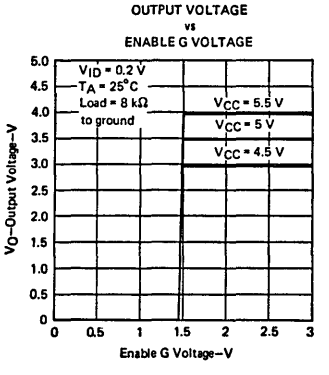


FIGURE 6

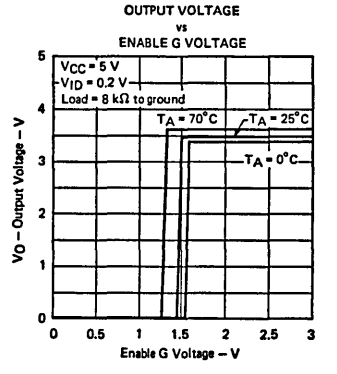


FIGURE 7

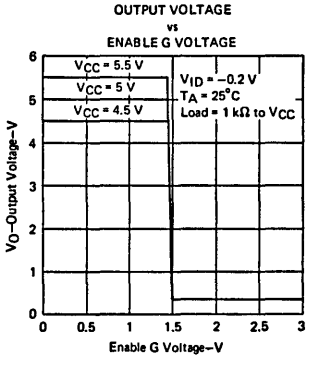


FIGURE 8

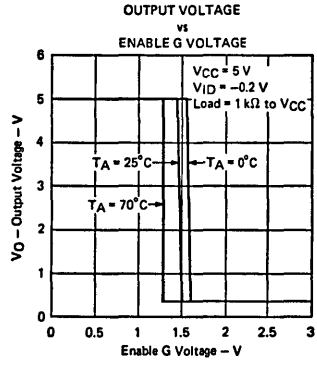


FIGURE 9

TYPICAL CHARACTERISTICS

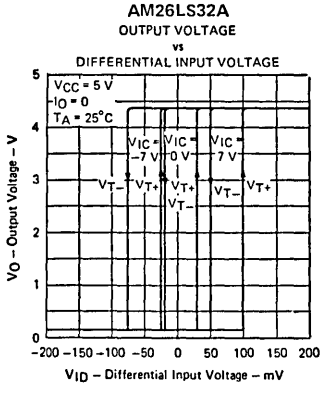


FIGURE 10

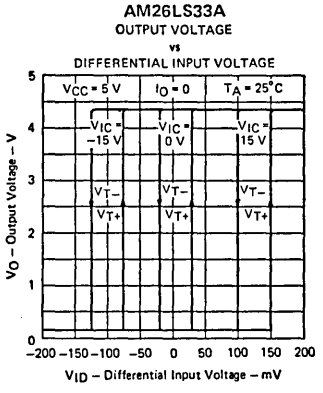


FIGURE 11

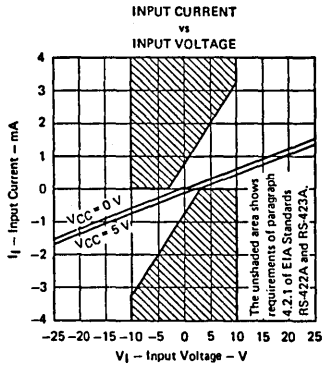
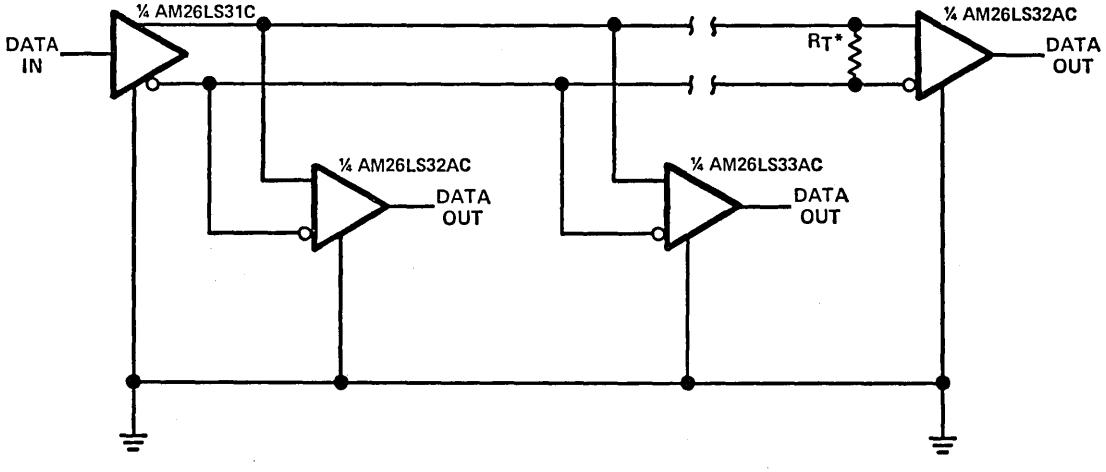


FIGURE 12

TYPICAL APPLICATION



*R_T equals the characteristic impedance of the line.

FIGURE 13 – CIRCUIT WITH MULTIPLE RECEIVERS

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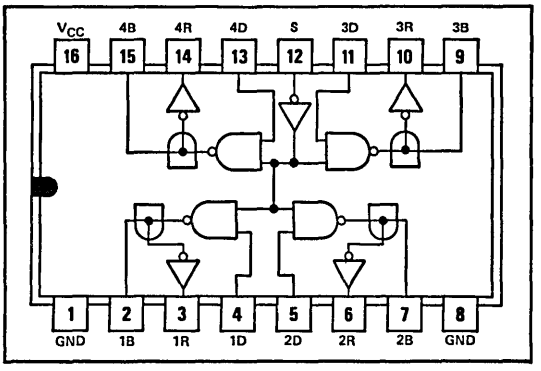
TYPES AM26S10M, AM26S10C, AM26S11M, AM26S11C
QUADRUPLE BUS TRANSCEIVERS

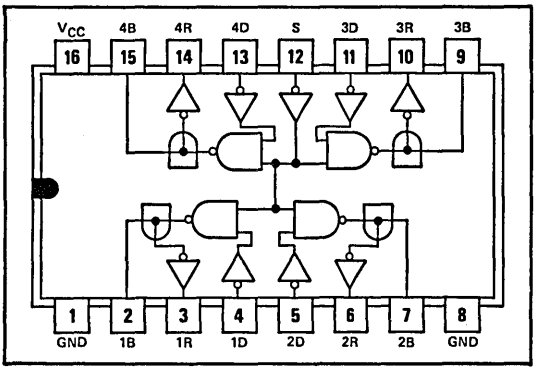
BULLETIN NO. DL-S 12498, JANUARY 1977 – REVISED SEPTEMBER 1980

- Schottky Circuitry† for High Speed, Typical Propagation Delay Time . . . 12 ns
- Drivers Feature Open-Collector Outputs for Party-Line (Data bus) Operation
- Driver Outputs Can Sink 100 mA at 0.8 V Maximum
- P-N-P Inputs for Minimal Input Loading
- Designed to be Interchangeable with Advanced Micro Devices AM26S10 and AM26S11

AM26S10
J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



AM26S11
J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

The AM26S10 and AM26S11 are quadruple bus transceivers utilizing Schottky-diode-clamped transistors for high speed. The drivers feature open-collector outputs capable of sinking 100 mA at 0.8 V maximum. The driver and strobe inputs use p-n-p transistors to reduce the input loading.

The driver of the AM26S10 is inverting; the driver of the AM26S11 is noninverting. Each device has two ground connections, for improved ground current-handling capability. For proper operation, the ground pins should be tied together.

The AM26S10M and AM26S11M are characterized for operation over the full military temperature range of −55°C to 125°C. The AM26S10C and AM26S11C are characterized for operation over the temperature range of 0°C to 70°C.

AM26S10
FUNCTION TABLE
(TRANSMITTING)

INPUTS		OUTPUTS	
S	D	B	R
L	H	L	H
L	L	H	L

AM26S11
FUNCTION TABLE
(TRANSMITTING)

INPUTS		OUTPUTS	
S	D	B	R
L	H	H	L
L	L	L	H

AM26S10 AND AM26S11
FUNCTION TABLE
(RECEIVING)

INPUTS			OUTPUT
S	B	D	R
H	H	X	L
H	L	X	H

H = high level, L = low level, X = irrelevant

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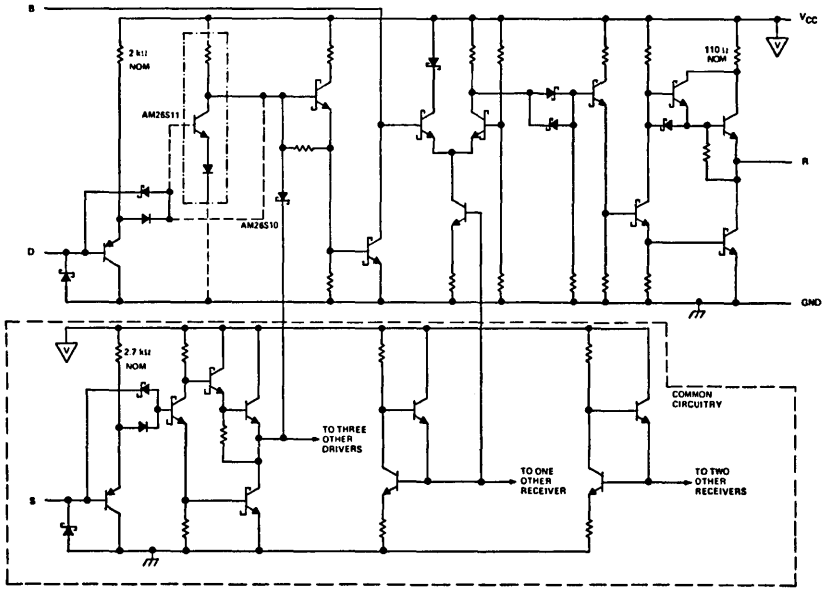
†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U. S. Patent Number 3,463,975.

schematic (each transceiver)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	−0.5 V to 7 V
Driver or strobe input voltage	−0.5 V to 5.5 V
Bus voltage, driver output off: AM26S10M, AM26S11M	−0.5 V to 5.5 V
AM26S10C, AM26S11C	−0.5 V to 5.25 V
Driver or strobe input current	−30 mA to 5 mA
Driver output current	200 mA
Receiver output current	30 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2)	800 mW
Operating free-air temperature range: AM26S10M, AM26S11M	−55°C to 125°C
AM26S11C, AM26S11C	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N package	260°C

NOTES: 1. Voltage values are with respect to network ground terminals connected together.

2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information Section, which starts on page 21. In the J package, AM26S10M and AM26S11M chips are alloy-mounted; AM26S10C and AM26S11C chips are glass-mounted.

recommended operating conditions

		AM26S10M AM26S11M			AM26S10C AM26S11C			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Receiver high-level output current, I_{OH}				−1			−1	mA
Low-level output current, I_{OL}	Driver			100			100	mA
	Receiver			20			20	
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

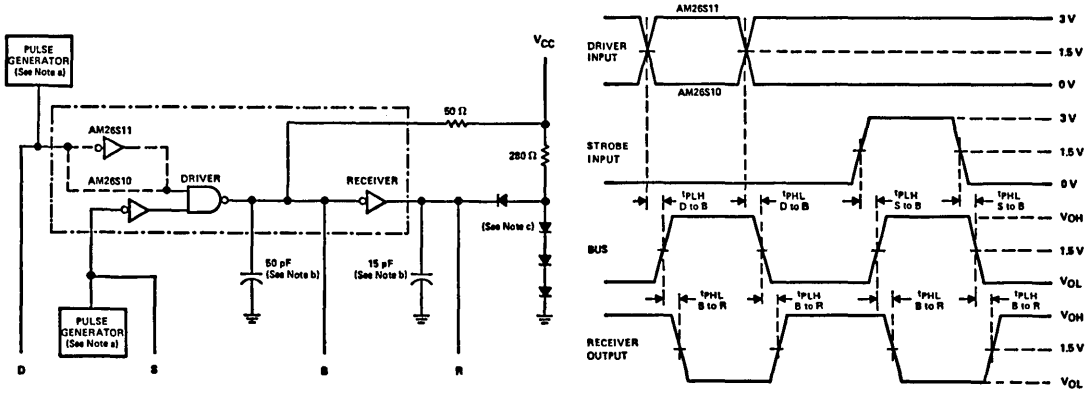
PARAMETER			TEST CONDITIONS†			AM26S10M AM26S11M MIN	AM26S10M AM26S11M TYP‡	AM26S10M AM26S11M MAX	AM26S10C AM26S11C MIN	AM26S10C AM26S11C TYP‡	AM26S10C AM26S11C MAX	UNIT
V_{IH}	High-level input voltage	D or S				2			2			V
		B				2.4			2.25			
V_{IL}	Low-level input voltage	D or S						0.8			0.8	V
		B						1.6			1.75	
V_{IK}	Input clamp voltage	D or S	V_{CC} = MIN, I_I = −18 mA					−1.2			−1.2	V
V_{OH}	High-level output voltage	R	V_{CC} = MIN, V_{IH} = 2 V, I_{OH} = −1 mA		V_{IL} = V_{IL} max,	2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	R	V_{CC} = MIN, V_{IH} = V_{IH} min, V_{IL} = 0.8 V		I_{OL} = 20 mA			0.5			0.5	V
		B			I_{OL} = 40 mA		0.33	0.5		0.33	0.5	
					I_{OL} = 70 mA		0.42	0.7		0.42	0.7	
					I_{OL} = 100 mA		0.51	0.8		0.51	0.8	
$I_{O(off)}$	Off-state output current	B	V_{IH} = 2 V, V_{IL} = 0.8 V	V_{CC} = MAX,	V_O = 0.8 V			−50			−50	μA
				V_{CC} = MAX,	V_O = 4.5 V			200			100	
				V_{CC} = 0,	V_O = 4.5 V			100			100	
I_{IH}	High-level input current	D	V_{CC} = MAX, V_I = 2.7 V					30			30	μA
		S						20			20	
I_I	Input current at maximum input voltage	D or S	V_{CC} = MAX, V_I = 5.5 V					100			100	μA
I_{IL}	Low-level input current	D	V_{CC} = MAX, V_I = 0.4 V					−0.54			−0.54	mA
		S						−0.36			−0.36	
I_{OS}	Short-circuit output current§	R	V_{CC} = MAX			−20		−55	−18		−60	mA
I_{CC}	Supply current	AM26S10	V_{CC} = MAX, Strobe at 0 V, All driver outputs low		No load,		45	70		45	70	mA
		AM26S11						80			80	

†For conditions shown as MIN or MAX, use the appropriate value shown under recommended operating conditions.
‡All typical values are at T_A = 25°C and V_{CC} = 5 V.
§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		FROM	TO	TEST CONDITIONS	AM26S10 MIN	AM26S10 TYP	AM26S10 MAX	AM26S11 MIN	AM26S11 TYP	AM26S11 MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	D	B	See Figure 1		10	15		12	19	ns
t_{PHL}	Propagation delay time, high-to-low-level output					10	15		12	19	
t_{PLH}	Propagation delay time, low-to-high-level output	S	B			14	18		15	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output					13	18		14	20	
t_{PLH}	Propagation delay time, low-to-high-level output	B	R			10	15		10	15	ns
t_{PHL}	Propagation delay time, high-to-low-level output					10	15		10	15	
t_{TLH}	Transition time, low-to-high-level output		B		4	10		4	10		ns
t_{THL}	Transition time, high-to-low-level output				2	4		2	4		

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

NOTES: a. The pulse generators have the following characteristics: Z_{out} = 50 Ω, t_r = 10 ± 5 ns.
b. Includes probe and jig capacitance.
c. All diodes are 1N916 or equivalent.

FIGURE 1

TYPICAL APPLICATION

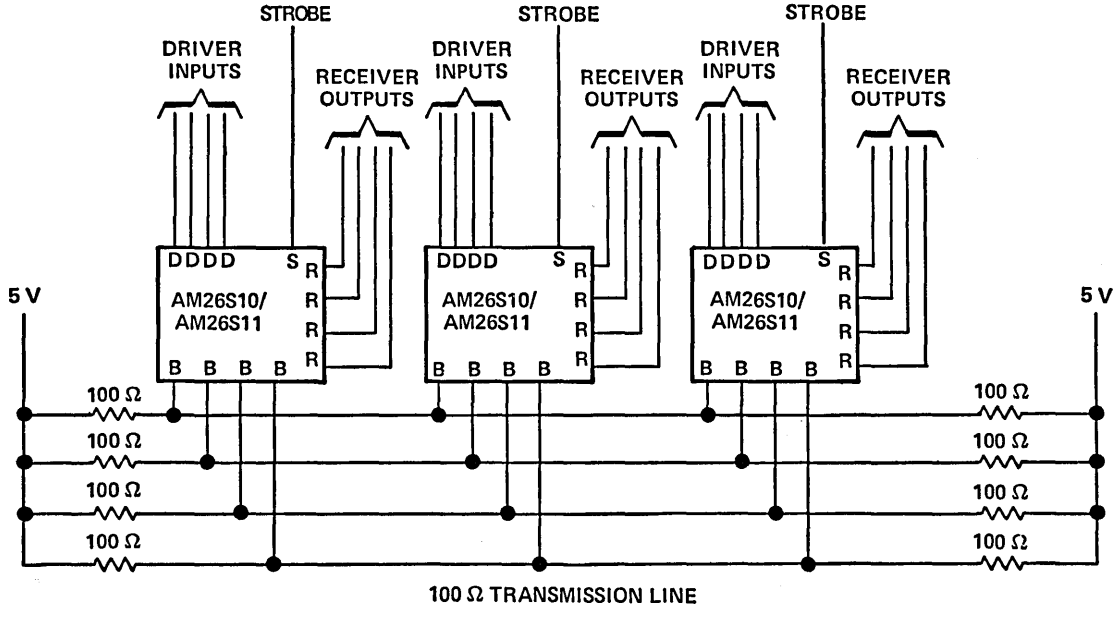


FIGURE 2–PARTY-LINE SYSTEM

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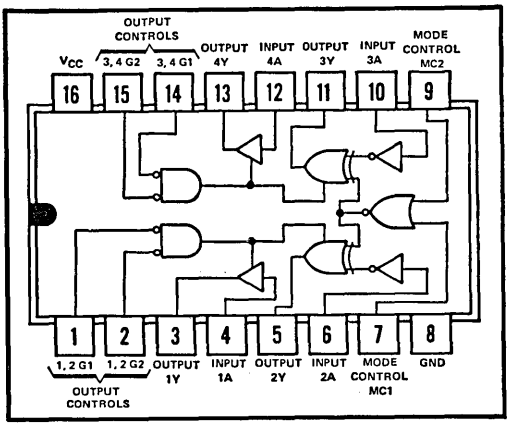
TYPES DS7831, DS7832, DS8831, DS8832
LINE DRIVERS WITH 3-STATE OUTPUTS

BULLETIN NO. DL-S 12496, JANUARY 1977

- TTL Compatible
- Propagation Delay Time . . . 15 ns Typ
- Very Low Output Impedance with High Drive Capability
- 40-mA Sink and Source Capability
- Gating Control to Allow Either Single-Ended or Differential Operation
- Three-State Outputs for Party-Line (Data-Bus) Operation

DS7831, DS7832.....J PACKAGE
DS8831, DS8832.....J OR N PACKAGE
(TOP VIEW)



description

The DS7831, DS7832, DS8831, and DS8832 can be used as either guadruple single-ended line drivers or as dual differential line drivers. This multi-mode operation and simple logic control make these devices especially useful for party-line or bus-organized systems. The DS7831 and DS8831 have output clamp diodes to V_{CC}; the DS7832 and DS8832 do not.

For one of these circuits to operate as four independent single-ended line drivers, both mode-control pins must be low. In this mode, no signal inversion takes place between inputs and outputs. To operate as a dual differential line driver, at least one of the mode control inputs must be high. Inputs 1A and 2A should be connected together as should 3A and 4A. Then signals applied to the inputs will appear noninverted at 1Y and 4Y and inverted at 2Y and 3Y, provided the output control pins are low.

While enabled, these outputs provide good drive capability for capacitive loads, and fast transitions from both low-to-high levels and high-to-low levels.

Taking either of the associated output controls high disables the outputs. When disabled, these three-state outputs neither load nor drive a line and hundreds of these devices may be connected to a common bus line. Only one output should be enabled at a time.

The DS7831 and DS7832 are characterized for operation over the full military temperature range of −55°C to 125°C. The DS8831 and DS8832 are characterized for operation from 0°C to 70°C.

FUNCTION TABLE

OUTPUT CONTROLS		MODE CONTROLS		DATA INPUT	OUTPUT	DATA INPUT	OUTPUT
G1	G2	MC1	MC2	1A/4A	1Y/4Y	2A/3A	2Y/3Y
L	L	L	L	H	H	H	H
L	L	L	L	L	L	L	L
L	L	X	H	H	H	H	L
L	L	H	X	L	L	L	H
H	X	X	X	X	Z	X	Z
X	H	X	X	X	Z	X	Z

H = high level, L = low level, X = irrelevant, Z = high impedance (off)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2): J package . . . . . 1025 mW
N package . . . . . 1150 mW
Operating free-air temperature range: DS78' . . . . . −55°C to 125°C
DS88' . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1/16 inch from case for 10 seconds: N package . . . . . 260°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 21. In the J package, DS7831 and DS7832 chips are alloy-mounted; DS8831 and DS8832 chips are glass-mounted.

recommended operating conditions

	DS78'			DS88'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Output voltage, V_O			5.5			5.5	V
High-level output current, I_{OH}			−40			−40	mA
Low-level output current, I_{OL}			40			40	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA				−1	−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V	I_{OH} = −2 mA	DS7831,DS7832	2.4	3.1		V
			I_{OH} = −5.2 mA	DS8831,DS8832	2.4	3.0		
			I_{OH} = −40 mA		1.8	2.5		
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V		I_{OL} = 32 mA		0.26	0.4	V
				I_{OL} = 40 mA		0.3	0.5	
V_{OK}	Output clamp voltage	V_{CC} = 5 V, T_A = 25°C	I_O = −12 mA				−1.5	V
			I_O = 12 mA	DS7831,DS8831			V_{CC} + 1.5	
I_{OZ}	Off-state (high-impedance-state) output current	V_{CC} = MAX, T_A = 25°C		V_O = 2.4 V			40	μA
				V_O = 0.4 V			−40	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V					1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V					40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−1	−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX, V_O = 0,		T_A = MAX	−40	−70	−120	mA
I_{CC}	Supply current	V_{CC} = MAX				50	90	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at T_A = 25°C and V_{CC} = 5 V.
§ Only one output should be shorted at a time.

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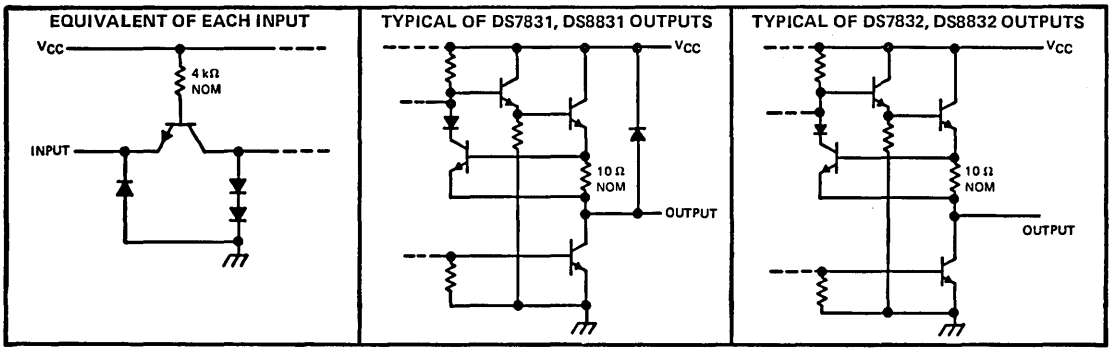
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM	TO	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	2A or 3A	2Y or 3Y (noninverting)	Mode controls low, See Figure 11		10	25	ns
t_{PHL}					12	25	
t_{PLH}	2A or 3A	2Y or 3Y (inverting)	Mode controls high, See Figure 11		12	25	ns
t_{PHL}					15	25	
t_{PLH}	1A or 4A	1Y or 4Y	See Figure 11		9	25	ns
t_{PHL}					11	25	
t_{PZH}	G1 or G2	Any Y	C_L = 50 pF, See Figure 13		12	22	ns
t_{PZL}					14	27	
t_{PHZ}	G1 or G2	Any Y	C_L = 5 pF, See Figure 13		6	12	ns
t_{PLZ}					15	22	

¶ t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output
t_{PZH} ≡ Output enable time to high level
t_{PZL} ≡ Output enable time to low level
t_{PHZ} ≡ Output disable time from high level
t_{PLZ} ≡ Output disable time from low level

schematics of inputs and outputs



TYPICAL CHARACTERISTICS

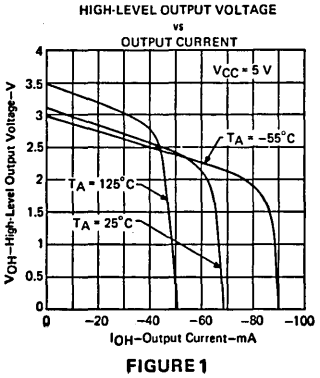


FIGURE 1

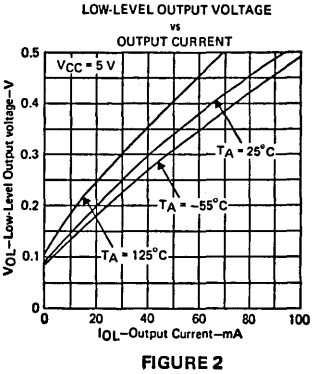


FIGURE 2

TYPICAL CHARACTERISTICS†

OFF-STATE OUTPUT CURRENT vs OUTPUT VOLTAGE

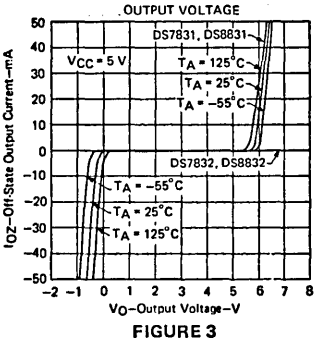


FIGURE 3

SUPPLY CURRENT vs FREQUENCY

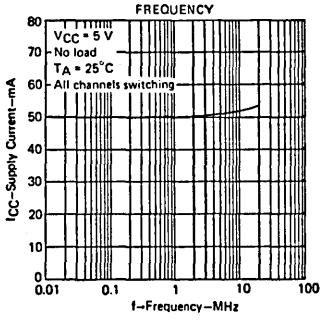


FIGURE 4

PROPAGATION DELAY TIMES vs FREE-AIR TEMPERATURE (DRIVERS 2 AND 3 ONLY, NONINVERTING)

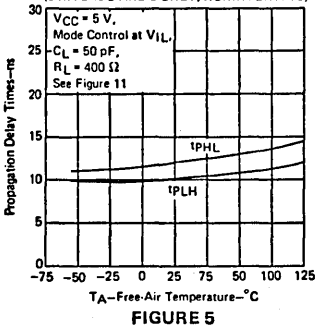


FIGURE 5

PROPAGATION DELAY TIMES vs FREE-AIR TEMPERATURE (DRIVERS 2 AND 3 ONLY, INVERTING)

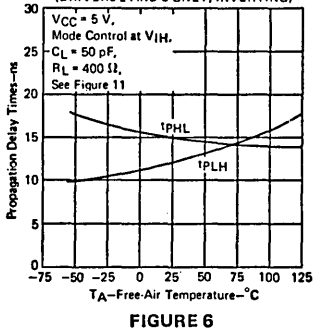


FIGURE 6

PROPAGATION DELAY TIMES vs FREE-AIR TEMPERATURE (DRIVERS 1 AND 4 ONLY)

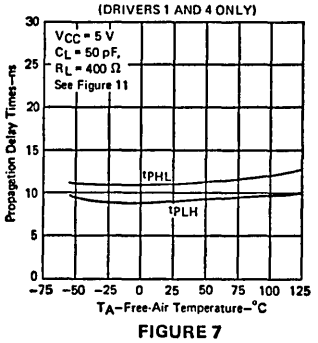


FIGURE 7

PROPAGATION DELAY vs LOAD CAPACITANCE (AVERAGE FOR ALL DRIVERS)

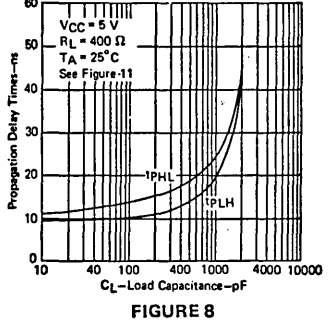


FIGURE 8

PROPAGATION DELAY IN DIFFERENTIAL MODE vs FREE-AIR TEMPERATURE

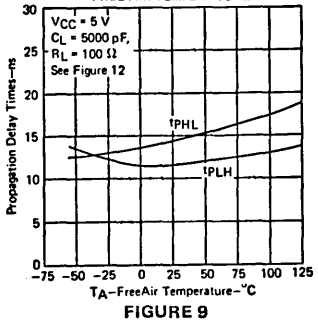


FIGURE 9

DRIVER OUTPUT ENABLE AND DISABLE TIMES vs FREE-AIR TEMPERATURE

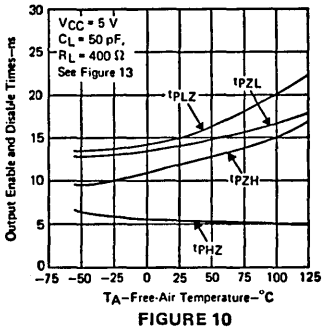


FIGURE 10

† Data for free-air temperature below 0°C and above 70°C are applicable to DS7831 and DS7832 circuits only.

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PARAMETER MEASUREMENT INFORMATION

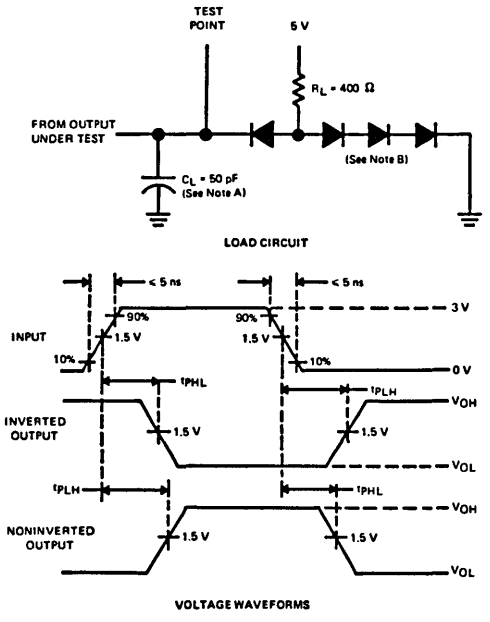


FIGURE 11– t_{PLH} and t_{PHL}, SINGLE-ENDED MODE

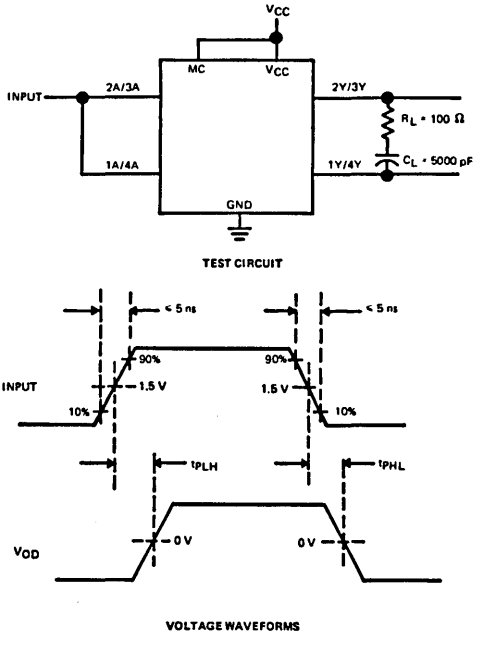
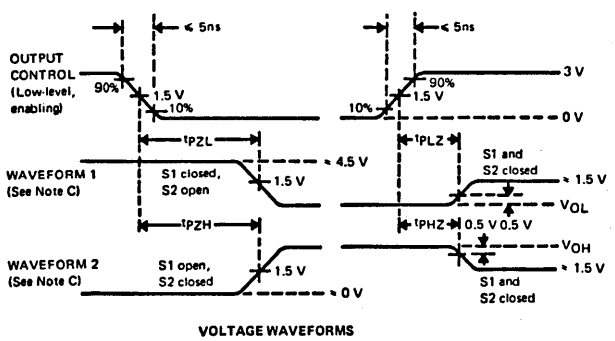


FIGURE 12–t_{PLH} and t_{PHL}, DIFFERENTIAL MODE



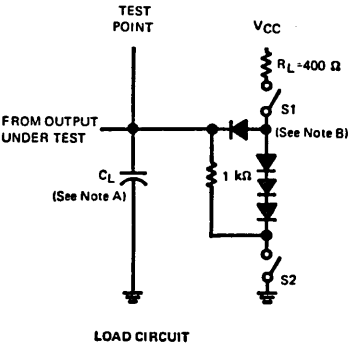


FIGURE 13–ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and job capacitance.
B. All diodes are 1N916 or 1N3064.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

TYPICAL APPLICATION DATA

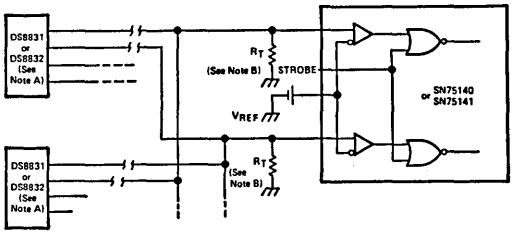


FIGURE 14–PARTY-LINE OPERATION UTILIZING THE SINGLE-ENDED CAPABILITY OF THE DEVICE

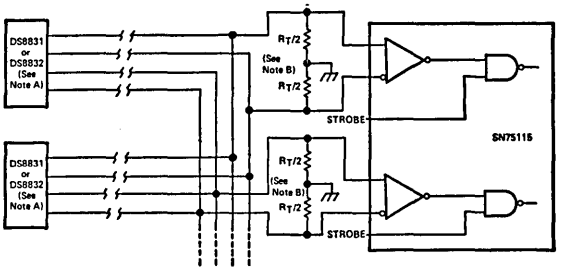


FIGURE 15–PARTY-LINE OPERATION UTILIZING THE DIFFERENTIAL CAPABILITY OF THE DEVICE

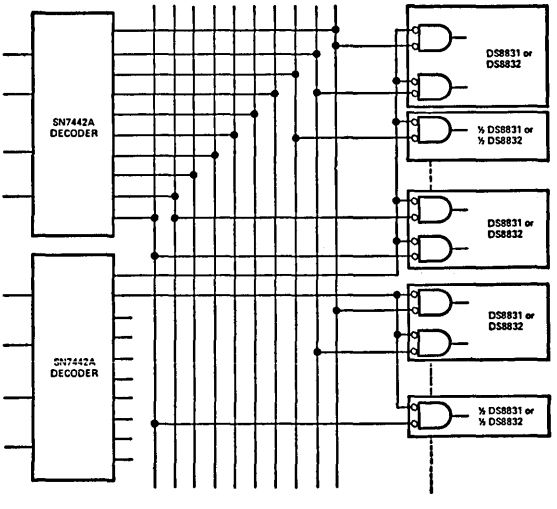


FIGURE 16–USING TWO 4-LINE-TO-10-LINE DECODERS TO CONTROL 100 DRIVER OUTPUTS

NOTES: A. One device may be driving onto the bus lines, and all other devices should be in the high-impedance state.
B. The value of R_T should be approximately equal to the characteristic impedance of the transmission line.

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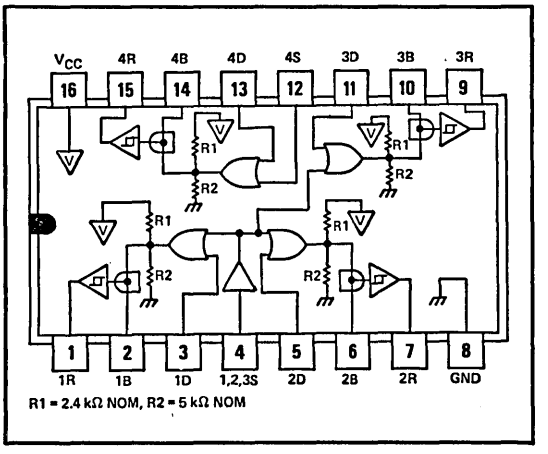
TYPE MC3446
QUADRUPLE BUS TRANSCEIVER

BULLETIN NO. DL-S 12492, JANUARY 1977 – REVISED AUGUST 1977

- Driver Inputs Compatible with TTL and MOS Circuitry
- Driver Outputs Stay Off During Power Up and Power Down
- Drivers Feature Open-Collector Outputs for Party-Line Operation
- Designed for Interchangeability with Motorola MC3446
- Meets IEEE Standard 488-1975

J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

These circuits are quadruple, single-ended line transceivers designed for bidirectional flow of data and instructions. The bus terminal characteristic complies with paragraph 3.5.3 of IEEE Standard 488 (see Figure 3). Each driver output is tied to the junction of an internal voltage divider that sets the no-load output voltage and provides bus termination. The driver outputs are guaranteed to be "off" during power up and power down if either input is high. The receivers feature 950 millivolts typical hysteresis for noise immunity.

The MC3446 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE
(TRANSMITTING)

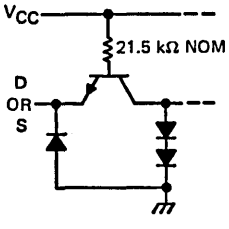
INPUTS		OUTPUT	
S	D	B	R
L	H	H	H
L	L	L	L

FUNCTION TABLE
(RECEIVING)

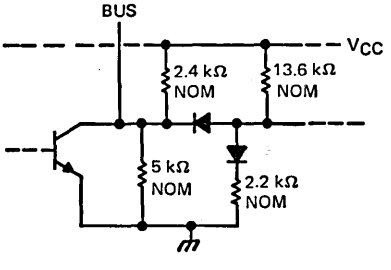
INPUTS			OUTPUT
S	B	D	R
H	H	X	H
H	L	X	L

schematics of inputs and outputs

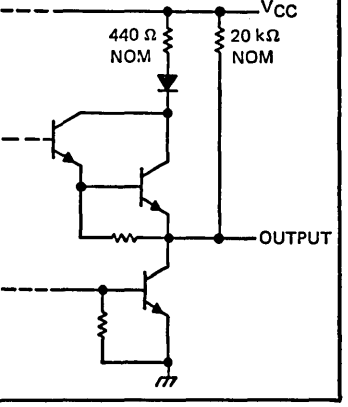
EQUIVALENT OF EACH DRIVER AND STROBE INPUT



EQUIVALENT OF DRIVER OUTPUTS/RECEIVER INPUTS



RECEIVER OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Driver output current . . . . . 150 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 830 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J Package . . . . . 300°C
Lead temperature 1/16 inch from case for 10 seconds: N Package . . . . . 260°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 18. In the J package, MC3446 chips are glass-mounted.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level output current, I_{OH}	Receiver			−0.4	mA
Low-level output current, I_{OL}	Driver			48	mA
	Receiver			8	
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended ranges of V_{CC} and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage	D or S		2			V
V_{IL}	Low-level input voltage	D or S				0.8	V
V_{IK}	Input clamp voltage	D or S	I_I = −12 mA			−1.5	V
V_{T+}	Positive-going input threshold voltage	B		1.5	1.8	2	V
V_{T-}	Negative-going input threshold voltage	B		0.6	0.85	1.1	V
$V_{T+} - V_{T-}$	Input hysteresis	B		400	950		mV
V_{OH}	High-level output voltage	B	V_{IH} = 2.4 V, I_{OH} = 0	2.5	3.3	3.7	V
		R	V_{IH} = 2 V, I_{OH} = −400 μA	2.4			
V_{OL}	Low-level output voltage	B	V_{IL} = 0.8 V, I_{OL} = 48 mA			0.4	V
		R	V_{IL} = 0.8 V, I_{OL} = 8 mA			0.4	
$I_{O(bus)}$	Bus current	B	V_{IH} = 2.4 V, V_O = 5.5 V			2.5	mA
			V_{IH} = 2.4 V, V_O = 5 V	0.7			
			V_{IH} = 2.4 V, V_O = 0.4 V	−1.3		−3.2	
V_{OK}	Output clamp voltage	B	I_O = −12 mA			−1.5	V
I_I	Input current at maximum input voltage	D or S	V_I = 5.5 V			1	mA
I_{IH}	High-level input current	D or S	V_{IH} = 2.4 V		5	20	μA
I_{IL}	Low-level input current	D or S	V_{CC} = 5 V, V_{IL} = 0.4 V, T_A = 25°C		0.2	0.36	mA
I_{OS}	Short-circuit output current	R	V_{IH} = 2 V	4		14	mA
I_{CCH}	Supply current, all outputs high		No load		10	19	mA
I_{CCL}	Supply current, all outputs low		No load		32	39	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

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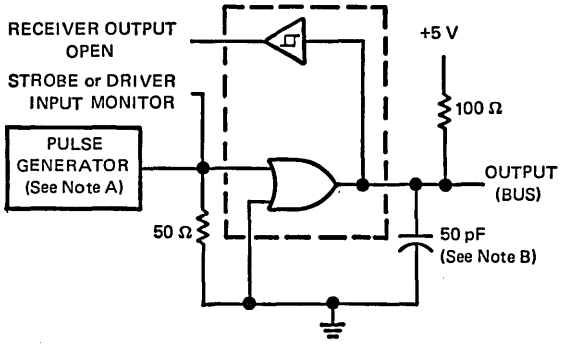
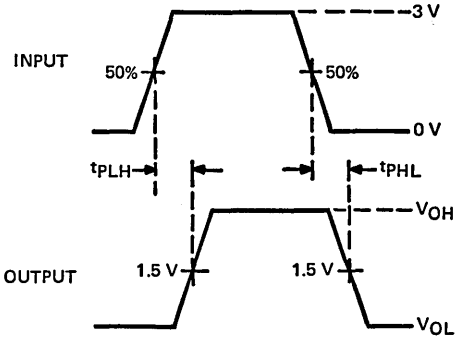
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		FROM	TO	TEST CONDITIONS	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	D	B	See Figure 1		40	ns
t_{PHL}	Propagation delay time, high-to-low-level output					50	
t_{PLH}	Propagation delay time, low-to-high-level output	S	B			50	ns
t_{PHL}	Propagation delay time, high-to-low-level output					50	
t_{PLH}	Propagation delay time, low-to-high-level output	B	R	See Figure 2		50	ns
t_{PHL}	Propagation delay time, high-to-low-level output					40	

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

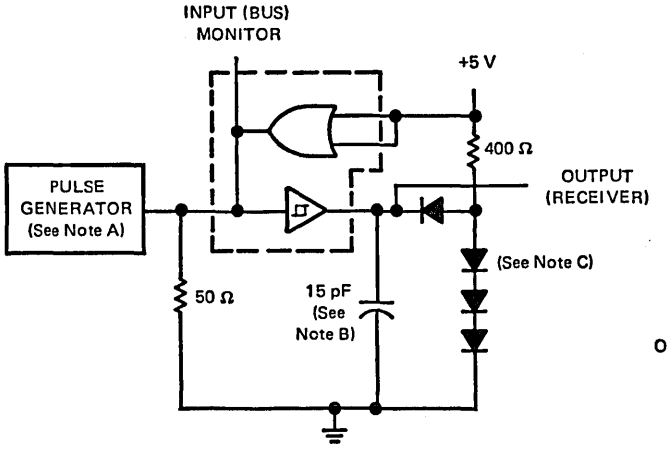


VOLTAGE WAVEFORMS

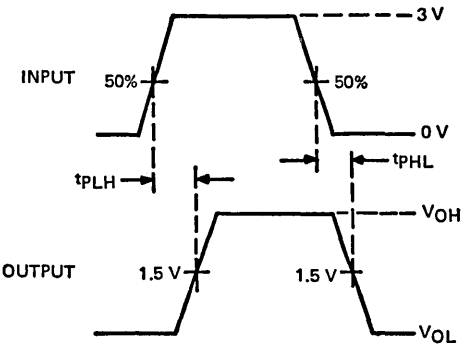
NOTES: A. The input pulse is supplied by a generator having the following characteristics: t_w = 100 ns, PRR = 1 MHz, $t_r \leq 10$ ns, $t_f \leq 10$ ns, $Z_{out} \approx 50\ \Omega$.
B. This value includes probe and jig capacitance.

FIGURE 1

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: t_w = 100 ns, PRR = 1 MHz, t_r < 10 ns, t_f < 10 ns, $Z_{out} \approx 50\ \Omega$.
B. This value includes probe and jig capacitance.
C. All diodes are 1N916 or 1N3064.

FIGURE 2

TYPICAL CHARACTERISTICS

DRIVER OUTPUT CHARACTERISTICS†

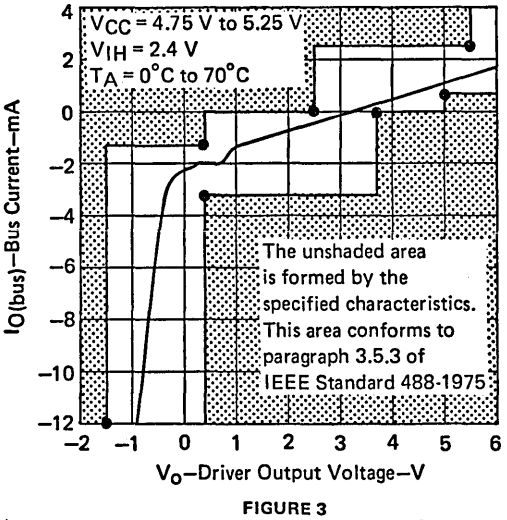


FIGURE 3

†Conditions for typical curve are V_{CC} = 5 V, T_A = 25°C.

RECEIVER TRANSFER CHARACTERISTICS

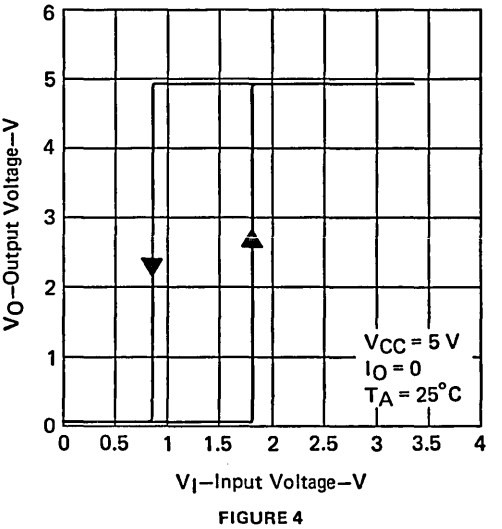


FIGURE 4

TEXAS INSTRUMENTS
INCORPORATED
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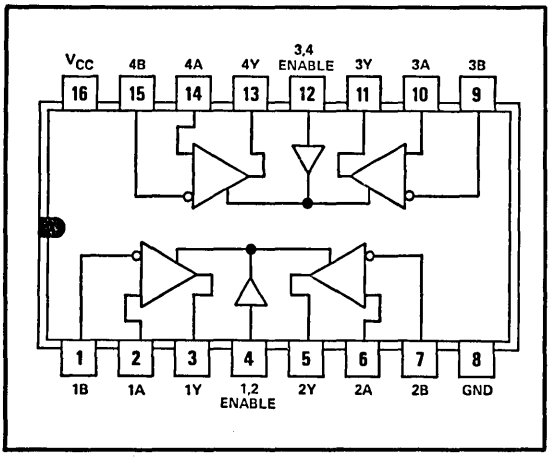
TYPE MC3486
QUADRUPLE LINE RECEIVER WITH 3-STATE OUTPUT

BULLETIN NO. DL-S 12748, JUNE 1980

- Meets EIA Standards RS-422A and RS-423A and Federal Standards 1020 and 1030
- Three-State, TTL-Compatible Outputs
- Fast Transition Times
- Operates From Single 5-Volt Supply
- Designed to be Interchangeable with Motorola MC3486

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



description

The MC3486 is a monolithic quadruple differential line receiver designed to meet the specifications of EIA Standards RS-422A and RS-423A and Federal Standards 1020 and 1030. The MC3486 offers four independent differential-input line receivers that have TTL-compatible outputs. The outputs utilize three-state circuitry to provide a high-impedance state at any output when the appropriate output enable is at a low logic level.

The MC3486 is designed for optimum performance when used with the MC3487 quadruple differential line driver. It is supplied in a 16-pin dual-in-line package and operates from a single 5-volt supply.

The MC3486 is characterized for operation from 0°C to 70°C.

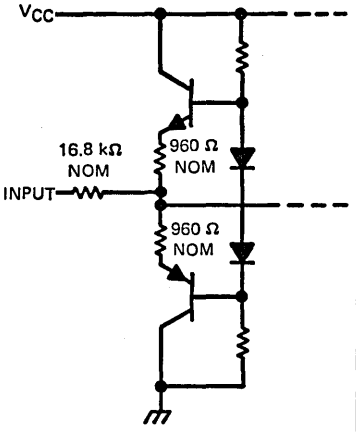
FUNCTION TABLE (EACH RECEIVER)

DIFFERENTIAL INPUTS A–B	ENABLE	OUTPUT Y
$V_{ID} \geq 0.2$ V	H	H
-0.2 V $< V_{ID} < 0.2$ V	H	?
$V_{ID} \leq -0.2$ V	H	L
Irrelevant	L	Z

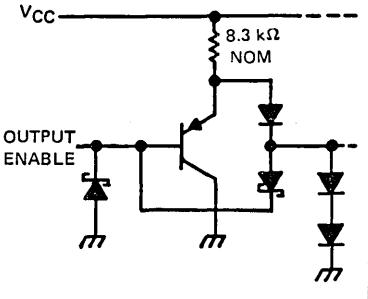
H = high level, L = low level, Z = high-impedance (off),
? = indeterminate

schematics of inputs and outputs

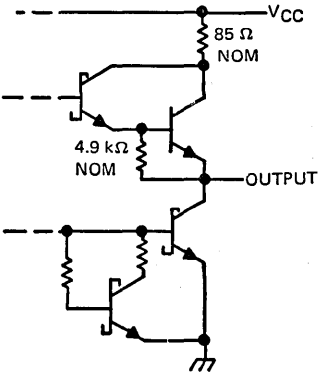
EQUIVALENT OF EACH INPUT EXCEPT OUTPUT ENABLE



EQUIVALENT OF OUTPUT ENABLE



TYPICAL OF ALL OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 8 V
Input voltage, A or B inputs . . . . . ±15 V
Differential input voltage (see Note 2) . . . . . ±25 V
Enable input voltage . . . . . 8 V
Low-level output current . . . . . 50 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3): J Package . . . . . 1025 mW
N Package . . . . . 1150 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch (1,6 mm) from case for 60 seconds: J Package . . . . . 300°C
Lead temperature 1/16 inch (1,6 mm) from case for 10 seconds: N Package . . . . . 260°C

NOTES: 1. All voltage values, except differential-input voltage, are with respect to network ground terminal.
2. Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.
3. For operation above 25°C free-air temperature, derate the J package at the rate of 8.2 mW/°C and the N package at the rate of 9.2 mW/°C.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Common-mode input voltage, V_{IC}			±7	V
Differential input voltage, V_{ID}			±6	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	MAX	UNIT
V_{TH}	Differential-input high-threshold voltage	V_O = 2.7 V, I_O = −0.4 mA				0.2	V
V_{TL}	Differential-input low-threshold voltage	V_O = 0.5 V, I_O = 8 mA			−0.2†		V
V_{IH}	High-level enable input voltage				2		V
V_{IL}	Low-level enable input voltage					0.8	V
V_{IK}	Enable-input clamp voltage	I_I = −10 mA				−1.5	V
V_{OH}	High-level output voltage	V_{ID}* = 0.4 V, I_O = −0.4 mA, See Note 4 and Figure 1			2.7		V
V_{OL}	Low-level output voltage	V_{ID}* = −0.4 V, I_O = 8 mA, See Note 4 and Figure 1				0.5	V
I_{OZ}	High-impedance-state output current	V_{IL} = 0.8 V, V_{ID} = −3 V,		V_O = 2.7 V		40	μA
		V_{IL} = 0.8 V, V_{ID} = 3 V,		V_O = 0.5 V		−40	
I_{IB}	Differential-input bias current	V_{CC} = 0 V or 5.25 V, Other inputs at 0 V		V_I = −10 V		−3.25	mA
				V_I = −3 V		−1.5	
				V_I = 3 V		1.5	
				V_I = 10 V		3.25	
I_{IH}	High-level enable input current	V_I = 5.25 V				100	μA
		V_I = 2.7 V				20	
I_{IL}	Low-level enable input current	V_I = 0.5 V				−100	μA
I_{OS}	Short-circuit output current	V_{ID} = 3 V, V_O = 0 V,		See Note 5	−15	−100	mA
I_{CC}	Supply current	V_{IL} = 0 V				85	mA

†The algebraic convention, where the least-positive (most-negative) limit is designated as minimum, is used in this data sheet for threshold voltages only.

NOTES: 4. Refer to EIA Standards RS-422A and RS-423A for exact conditions.
5. Only one output at a time should be shorted.

TEXAS INSTRUMENTS
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switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 15 pF, see Figure 2		28	35	ns
t_{PLH}	Propagation delay time, low-to-high-level output			27	30	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF, see Figure 3		13	30	ns
t_{PZL}	Output enable time to low level			20	30	ns
t_{PHZ}	Output disable time from high level			26	35	ns
t_{PLZ}	Output disable time from low level			27	35	ns

PARAMETER MEASUREMENT INFORMATION

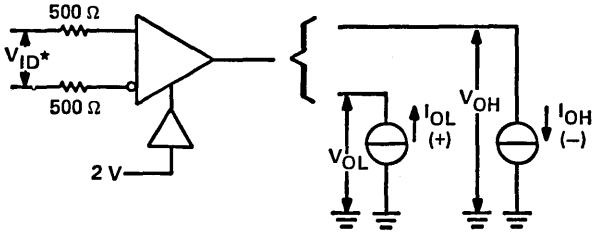
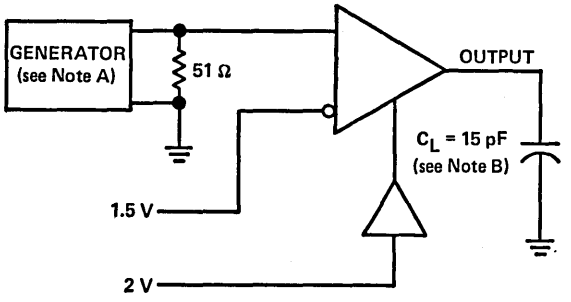
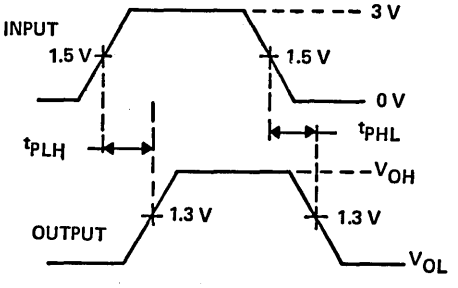


FIGURE 1–V_{OH}, V_{OL}



TEST CIRCUIT

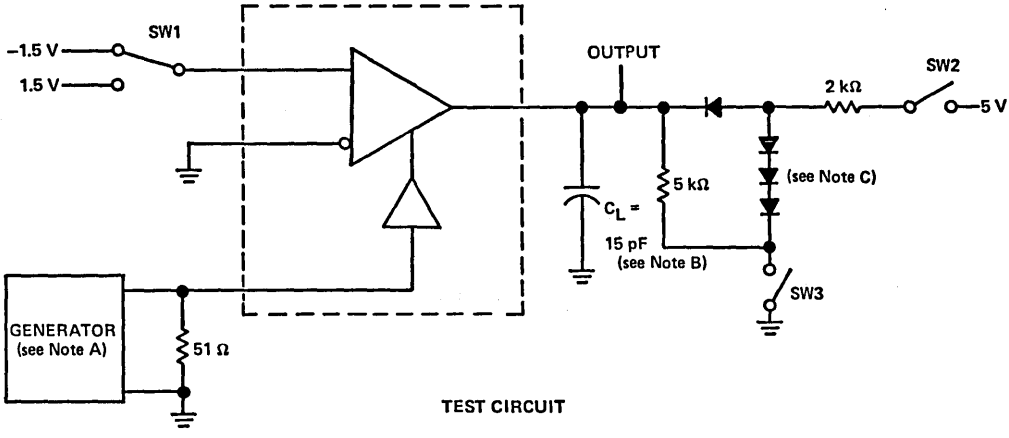


VOLTAGE WAVEFORMS

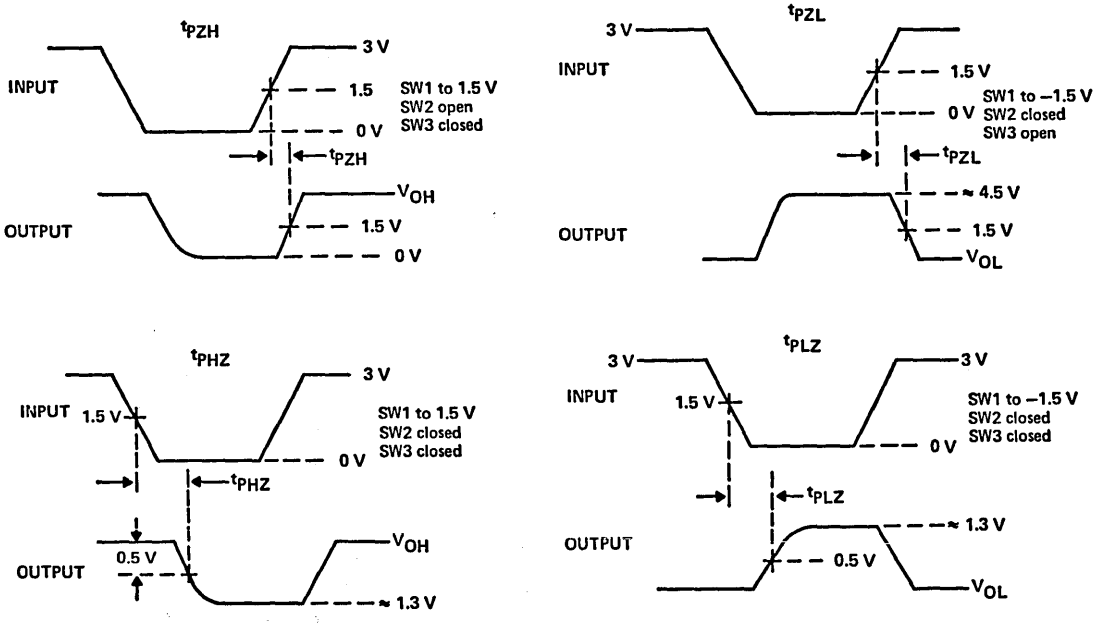
NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r = t_f$ = 6 ns.
B. C_L includes probe and stray capacitance.

FIGURE 2–PROPAGATION DELAY TIMES

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 3–ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle ≈ 50%, $t_r = t_f = 6$ ns.
B. C_L includes probe and stray capacitance
C. All diodes are 1N916 or equivalent.

TEXAS INSTRUMENTS
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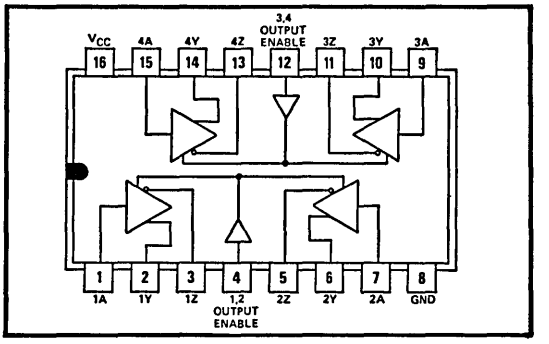
TYPE MC3487
QUADRUPLE DIFFERENTIAL LINE DRIVER WITH 3-STATE OUTPUTS

BULLETIN NO. DL-S 12749, MAY 1980

- Meets EIA Standard RS-422A and Federal Standard 1020
- Three-State, TTL-Compatible Outputs
- Fast Transition Times
- High-Impedance Inputs
- Single 5-Volt Supply
- Power-Up and Power-Down Protection
- Designed To Be Interchangeable with Motorola MC3487

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



description

The MC3487 offers four independent differential line drivers designed to meet the specifications of EIA Standard RS-422A and Federal Standard 1020. Each driver has a TTL-compatible input buffered to reduce current and minimize loading.

The driver outputs utilize 3-state circuitry to provide high-impedance states at any pair of differential outputs when the appropriate output enable is at a logic low level. Internal circuitry is provided to ensure a high-impedance state at the differential outputs during power-up and power-down transition times, provided the output enable is low. The outputs are capable of source or sink currents of 48 milliamperes.

FUNCTION TABLE (EACH DRIVER)

INPUT	OUTPUT ENABLE	OUTPUTS	
		Y	Z
H	H	H	L
L	H	L	H
X	L	High-Impedance	High-Impedance

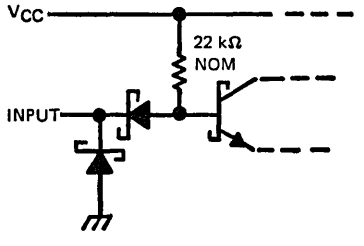
H = TTL high level X = irrelevant
L = TTL low level

The MC3487 is designed for optimum performance when used with the MC3486 quadruple line receiver. It is supplied in a 16-pin dual-in-line package and operates from a single 5-volt supply.

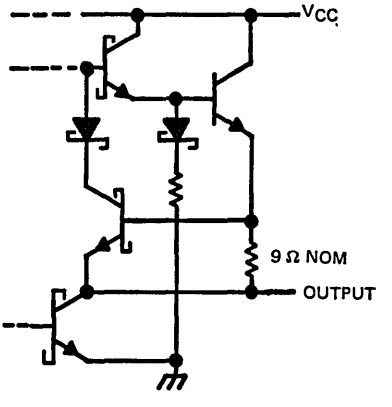
The MC3487 is characterized for operation from 0°C to 70°C.

schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



TYPICAL OF ALL OUTPUTS



TYPE MC3487
QUADRUPLE DIFFERENTIAL LINE DRIVER WITH 3-STATE OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 8 V
Input voltage . . . . . 5.5 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2):
J package . . . . . 1025 mW
N package . . . . . 1150 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch (1,6 mm) from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1/16 inch (1,6 mm) from case for 10 seconds: N package . . . . . 260°C

NOTES: 1. All voltage values, except differential output voltage V_{OD}, are with respect to the network ground terminal.
2. For operation above 25°C free-air temperature, derate the J package at the rate of 8.2 mW/°C and the N package at the rate of 9.2 mW/°C.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	MAX	UNIT
V_{IH}	High-level input voltage				2		V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{IL} = 0.8 V,	V_{IH} = 2 V	I_{OH} = −20 mA	2.5		V
				I_{OH} = −48 mA	2		
V_{OL}	Low-level output voltage	V_{IL} = 0.8 V,	V_{IH} = 2 V,	I_{OL} = 48 mA		0.5	V
$\lvert V_{OD}\rvert$	Differential output voltage	R_L = 100 Ω,	See Figure 1		2		V
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of differential output voltage†	R_L = 100 Ω,	See Figure 1			±0.4	V
V_{OC}	Common-mode output voltage‡	R_L = 100 Ω,	See Figure 1			3	V
$\Delta\lvert V_{OC}\rvert$	Change in magnitude of common-mode output voltage†	R_L = 100 Ω,	See Figure 1			± 0.4	V
I_O	Output current with power off	V_{CC} = 0 V	V_O = 6 V			100	μA
			V_O = −0.25 V			−100	
I_{OZ}	High-impedance-state output current	Output enables at 0.8 V	V_O = 2.7 V			100	μA
			V_O = 0.5 V			−100	
I_I	Input current at maximum input voltage	V_I = 5.5 V				100	μA
I_{IH}	High-level input current	V_I = 2.7 V				50	μA
I_{IL}	Low-level input current	V_I = 0.5 V				−400	μA
I_{OS}	Short-circuit output current§	V_I = 2 V			−40	−140	mA
I_{CC}	Supply current (all drivers)	Inputs grounded,	No load			105	mA
		Output enables at 2 V				85	

†$\Delta\lvert V_{OD}\rvert$ and $\Delta\lvert V_{OC}\rvert$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
‡In EIA Standard RS-422A, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.
§Only one output at a time should be shorted and duration of the short-circuit should not exceed one second.

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switching characteristics, V_{CC} = 5 V, T_A = 25°C

	PARAMETER	TEST CONDITION	MIN	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF, See Figure 2		20	ns
t_{PHL}	Propagation delay time, high-to-low-level output			20	ns
	Skew			6	ns
t_{TD}	Differential-output transition time	C_L = 15 pF, See Figure 3		20	ns
t_{PZH}	Output enable time to high level	C_L = 50 pF, See Figure 4		30	ns
t_{PZL}	Output enable time to low level			30	ns
t_{PHZ}	Output disable time from high level			25	ns
t_{PLZ}	Output disable time from low level			25	ns

PARAMETER MEASUREMENT INFORMATION

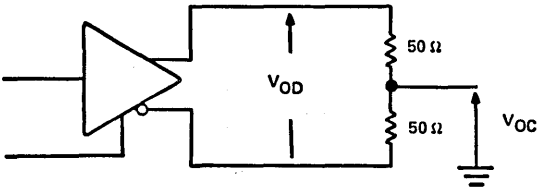
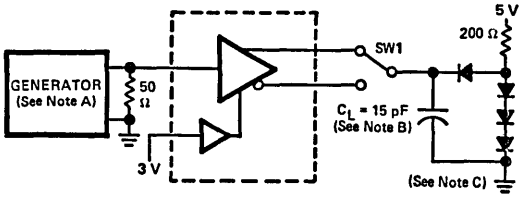
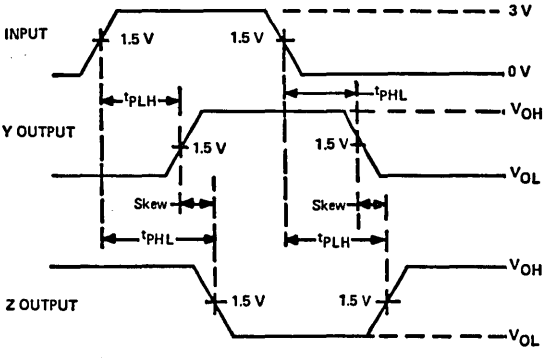


FIGURE 1–DIFFERENTIAL AND COMMON-MODE OUTPUT VOLTAGES



TEST CIRCUIT

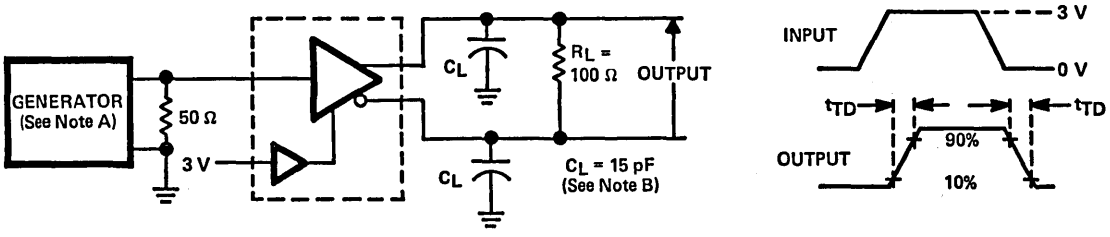


VOLTAGE WAVEFORM

NOTES: A. The input pulse is supplied by a generator having the following characteristics: $t_r \leq 5$ ns, $t_f \leq 5$ ns, PRR = 1 MHz, duty cycle = 50%, Z_o = 50 Ω.
B. C_L includes probe and stray capacitance.
C. All diodes are IN916 or IN3064.

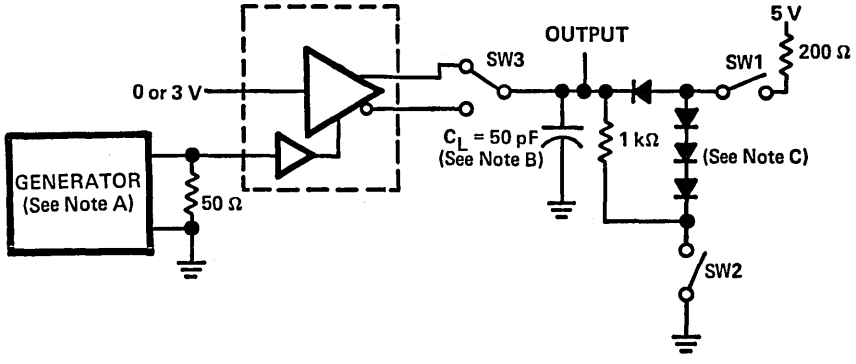
FIGURE 2–PROPAGATION DELAY TIMES

PARAMETER MEASUREMENT INFORMATION

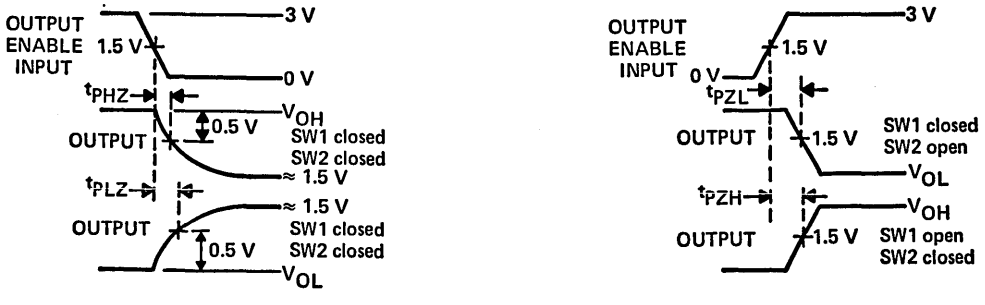


TEST CIRCUIT VOLTAGE WAVEFORMS

FIGURE 3–DIFFERENTIAL-OUTPUT TRANSITION TIMES



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 4–DRIVER ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: $t_r \leq 5$ ns, $t_f \leq 5$ ns, PRR = 1 MHz, duty cycle = 50%, Z_o = 50 Ω.
B. C_L includes probe and stray capacitance.
C. All diodes are IN916 or IN3064.

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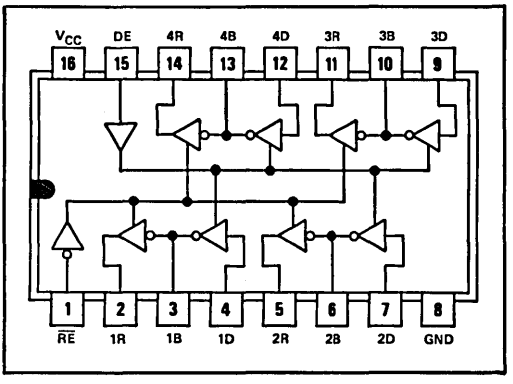
TYPES N8T26, N8T26A QUADRUPLE BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

BULLETIN NO. DL-S 12617, MAY 1978 – REVISED JULY 1980

- P-N-P Inputs for Minimal Input Loading (200 μA Maximum)
- High-Speed Schottky Circuitry†
- 3-State Outputs for Driver and Receiver
- Party-Line (Data-Bus) Operation
- Single 5-V Supply
- N8T26A Driver has 48-mA Current Sink Capability
- Designed to be Interchangeable with Signetics N8T26 and N8T26A, also Called 8T26 and 8T26A

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)

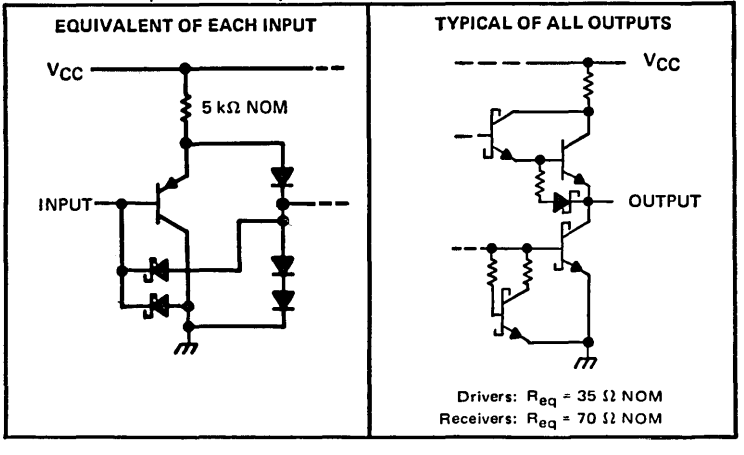


description

The N8T26 and N8T26A are quadruple transceivers utilizing Schottky-diode-clamped transistors. Both the driver and receiver have three-state outputs. With p-n-p inputs, the input loading is reduced to a maximum input current of 200 microamperes. These devices are capable of high switching rates into high-capacitance loads and are suitable for driving long bus lines.

The N8T26 and N8T26A are characterized for operation from 0°C to 70°C.

schematics of inputs and outputs



FUNCTION TABLE (DRIVER)

INPUT		OUTPUT
D	DE	B
L	H	H
H	H	L
X	L	Z

FUNCTION TABLE (RECEIVER)

INPUT		OUTPUT
B	$\overline{RE}$	R
L	L	H
H	L	L
X	H	Z

H = high level, L = low level,
X = irrelevant, Z = high impedance

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2): J package . . . . . 1025 mW
N package . . . . . 1150 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . –65°C to 150°C
Lead temperature 1/16 inch (1,6 mm) from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1/16 inch (1,6 mm) from case for 10 seconds: N package . . . . . 260°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, derate the J package at the rate of 8.2 mW/°C and the N package at the rate of 9.2 mW/°C.

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†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U.S. Patent Number 3,463,975.

N8T26 recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level output current, I_{OH}	Driver, B			−10	mA
	Receiver, R			−2	
Low-level output current, I_{OL}	Driver, B			40	mA
	Receiver, R			16	
Operating free-air temperature, T_A		0		70	°C

N8T26 electrical characteristics over recommended operating free-air temperature and supply voltage ranges (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage	B, D, DE, $\overline{RE}$		2			V
V_{IL}	Low-level input voltage	B, D, DE, $\overline{RE}$				0.85	V
V_{IK}	Input clamp voltage	B, D, DE, $\overline{RE}$	I_I = −5 mA			−1	V
V_{OH}	High-level output voltage	B	V_{IH} = 2 V, V_{IL} = 0.85 V, I_{OH} = −10 mA	2.6	3.1		V
		R	V_{IL} = 0.85 V I_{OH} = −2 mA	2.6	3.1		
V_{OL}	Low-level output voltage	B	V_{IH} = 2 V, I_{OL} = 40 mA			0.5	V
		R	V_{IH} = 2 V, V_{IL} = 0.85 V, I_{OL} = 16 mA			0.5	
I_{OZ}	Off-state (high-impedance state) output current	B, R	DE at 0.85 V $\overline{RE}$ at 2 V, V_O = 2.6 V			100	μA
		R	$\overline{RE}$ at 2 V, V_O = 0.5 V			−100	
I_{IH}	High-level input current	D, DE, $\overline{RE}$	V_I = 5.25 V			25	μA
I_{IL}	Low-level input current	B, D, DE, $\overline{RE}$	V_I = 0.4 V			−200	μA
I_{OS}	Short-circuit output current§	B	V_{CC} = 5.25 V	−50		−150	mA
		R		−30		−75	
I_{CC}	Supply current		V_{CC} = 5.25 V, No load			87	mA

N8T26 switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		FROM	TO	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	B	R	C_L = 30 pF, See Figure 1		8	18	ns
t_{PHL}	Propagation delay time, high-to-low-level output					7	10	
t_{PLH}	Propagation delay time, low-to-high-level output	D	B	C_L = 300 pF, See Figure 2		14	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output					12	20	
t_{PLZ}	Output disable time from low level	$\overline{RE}$	R	C_L = 30 pF, See Figure 3		9	17	ns
t_{PZL}	Output enable time to low level					15	30	
t_{PLZ}	Output disable time from low level	DE	B	C_L = 300 pF, See Figure 4		20	43	ns
t_{PZL}	Output enable time to low level					20	38	

†All typical values are at T_A = 25°C and V_{CC} = 5 V.
§Only one output should be shorted at a time, and duration of the short circuit should not exceed one second.

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N8T26A recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level output current, I_{OH}	Driver, B			−10	mA
	Receiver, R			−2	
Low-level output current, I_{OL}	Driver, B			48	mA
	Receiver, R			20	
Operating free-air temperature, T_A		0		70	°C

N8T26A electrical characteristics over recommended operating free-air temperature and supply voltage ranges (unless otherwise noted)

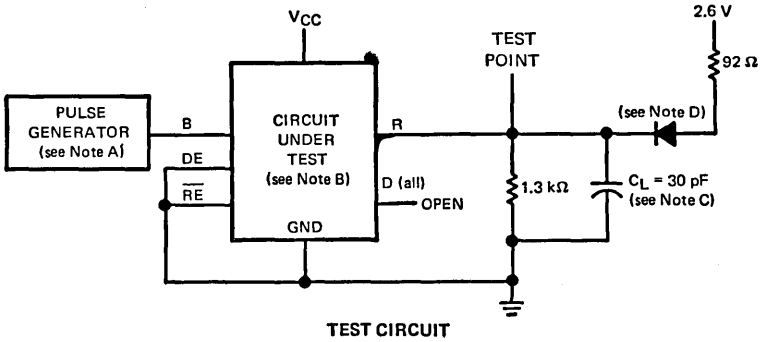
PARAMETER			TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage	B, D, DE, $\overline{RE}$				2			V
V_{IL}	Low-level input voltage	B, D, DE, $\overline{RE}$						0.85	V
V_{IK}	Input clamp voltage	B, D, DE, $\overline{RE}$	I_I = −12 mA					−1	V
V_{OH}	High-level output voltage	B	V_{IH} = 2 V,	V_{IL} = 0.85 V,	I_{OH} = −10 mA	2.6	3.1		V
		R	V_{IL} = 0.85 V	I_{OH} = −2 mA		2.6	3.1		
			V_{IL} = 0.85 V	I_{OH} = −100 μA		3.5			
V_{OL}	Low-level output voltage	B	V_{IH} = 2 V,	I_{OL} = 48 mA				0.5	V
		R	V_{IH} = 2 V,	V_{IL} = 0.85 V,	I_{OL} = 20 mA			0.5	
I_{OZ}	Off-state (high-impedance state) output current	B, R	DE at 0.85 V	$\overline{RE}$ at 2 V,	V_O = 2.6 V			100	μA
		B, R	DE at 0.85 V,	$\overline{RE}$ at 2 V,	V_O = 0.5 V			−100	
I_{IH}	High-level input current	D, DE, $\overline{RE}$	V_I = 5.25 V					25	μA
I_{IL}	Low-level input current	B, D, DE, $\overline{RE}$	V_I = 0.4 V					−200	μA
		D	V_I = 0.4 V,	DE at 0.85 V				−25	
I_{OS}	Short-circuit output current§	B	V_{CC} = 5.25 V			−50		−150	mA
		R				−30		−75	
I_{CC}	Supply current		V_{CC} = 5.25 V,	No load				87	mA

N8T26A switching characteristics, V_{CC} = 5 V, T_A = 25°C

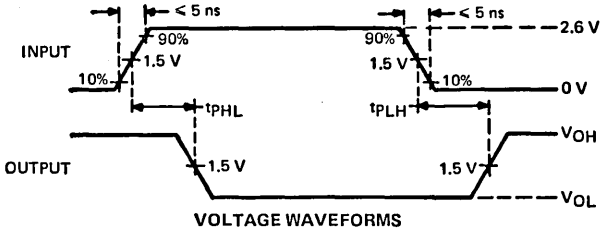
PARAMETER		FROM	TO	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	B	R	C_L = 30 pF, See Figure 1		8	14	ns
t_{PHL}	Propagation delay time, high-to-low-level output					7	14	
t_{PLH}	Propagation delay time, low-to-high-level output	D	B	C_L = 300 pF, See Figure 2		12	14	ns
t_{PHL}	Propagation delay time, high-to-low-level output					10	14	
t_{PLZ}	Output disable time from low level	$\overline{RE}$	R	C_L = 30 pF, See Figure 3		7	15	ns
t_{PZL}	Output enable time to low level					12	20	
t_{PLZ}	Output disable time from low level	DE	B	C_L = 300 pF, See Figure 4		14	20	ns
t_{PZL}	Output enable time to low level					17	25	

†All typical values are at T_A = 25°C and V_{CC} = 5 V.
§Only one output should be shorted at a time, and duration of the short circuit should not exceed one second.

PARAMETER MEASUREMENT INFORMATION

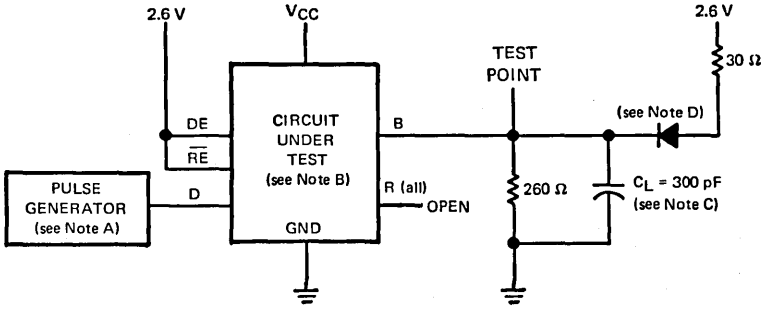


TEST CIRCUIT

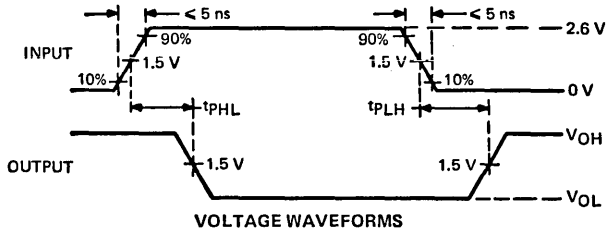


VOLTAGE WAVEFORMS

FIGURE 1–PROPAGATION DELAY TIMES FROM BUS TO RECEIVER OUTPUT



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 2–PROPAGATION DELAY TIMES FROM DRIVER INPUT TO BUS

NOTES: A. The pulse generator in Figures 1 and 2 has the following characteristics: PRR = 10 MHz, duty cycle = 50%, $Z_{out} \approx 50\ \Omega$.
B. All inputs and outputs not shown are open.
C. C_L includes probe and jig capacitance.
D. All diodes are 1N916 or 1N3064.

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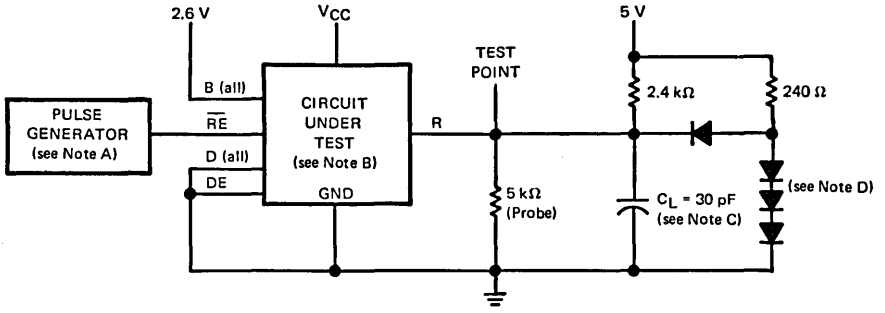
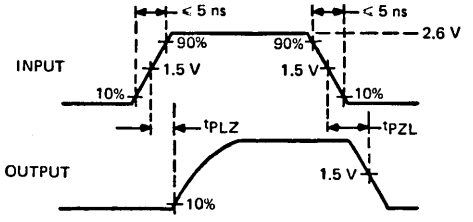
PARAMETER MEASUREMENT INFORMATION

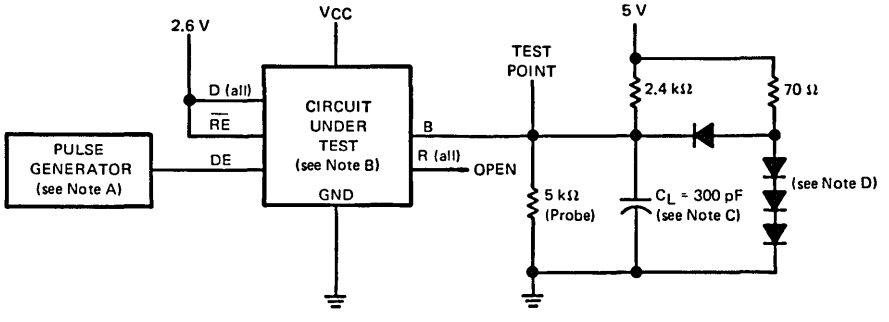


TEST CIRCUIT

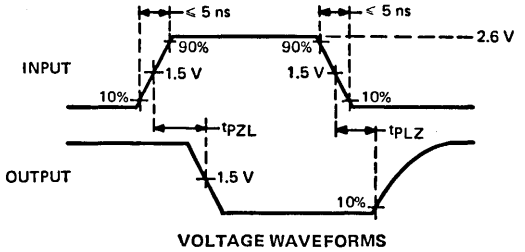


VOLTAGE WAVEFORMS

FIGURE 3–RECEIVER ENABLE AND DISABLE TIMES



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 4–DRIVER ENABLE AND DISABLE TIMES

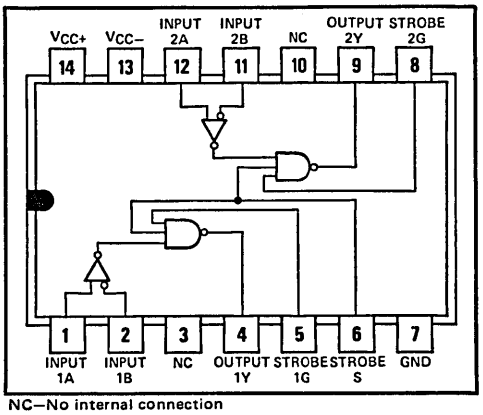
NOTES: A. The pulse generator in Figures 3 and 4 has the following characteristics: PRR = 5 MHz, duty cycle = 50%, $Z_{out} \approx 50\ \Omega$.
B. All inputs and outputs not shown are open.
C. C_L includes probe and jig capacitance.
D. All diodes are 1N916 or 1N3064.

TYPES SN55107A, SN55107B, SN55108A, SN55108B, SN75107A, SN75107B, SN75108A, SN75108B DUAL LINE RECEIVERS

BULLETIN NO. DL-S 12493, JANUARY 1977

- High Speed
- Standard Supply Voltages
- Dual Channels
- High Common-Mode Rejection Ratio
- High Input Impedance
- High Input Sensitivity
- Differential Input Common-Mode Range of ±3 V
- Differential Input Common-Mode Range of More than ±15 V Using External Attenuator
- Strobe Inputs For Receiver Selection
- Gate Inputs For Logic Versatility
- TTL or DTL Drive Capability
- High D-C Noise Margin
- '107A and '107B Have Totem-Pole Outputs
- '108A and '108B Have Open-Collector Outputs
- "B" Versions Have Diode-Protected Input Stage For Power-Off Condition

SN55107A, SN55107B, SN55108A, SN55108B . . . J DUAL-IN-LINE PACKAGE
SN75107A, SN75107B, SN75108A, SN75108B . . . J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



NC—No internal connection

FUNCTION TABLE

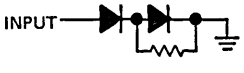
DIFFERENTIAL INPUTS A – B	STROBES G	STROBES S	OUTPUT Y
$V_{ID} \geq 25$ mV	X	X	H
-25 mV $< V_{ID} < 25$ mV	X	L	H
	L	X	H
	H	H	Indeterminate
$V_{ID} \leq -25$ mV	X	L	H
	L	X	H
	H	H	L

H = high level, L = low level, X = irrelevant

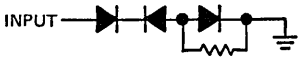
description

These circuits are TTL/DTL compatible high-speed line receivers. Each is a monolithic dual circuit featuring two independent channels. They are designed for general use as well as such specific applications as data comparators and balanced, unbalanced, and party-line transmission systems. These devices are unilaterally interchangeable with and replace SN55107, SN55108, SN75107, and SN75108, but offer diode-clamped strobe inputs to simplify circuit design.

The essential difference between the "A" and "B" versions can be seen in the schematics. Input-protection diodes are in series with the collectors of the differential-input transistors of the "B" versions. These diodes are useful in certain "party-line" systems that may have multiple V_{CC+} power supplies and may be operated with some of the V_{CC+} supplies turned off. In such a system, if a supply is turned off and allowed to go to ground, the equivalent input circuit connected to that supply would be as follows:



"A" VERSION



"B" VERSION

This would be a problem in specific systems that might possibly have the transmission lines biased to some potential greater than 1.4 volts.

The SN55107A, SN55107B, SN55108A, and SN55108B, are characterized for operation over the full military temperature range of −55°C to 125°C. The SN75107A, SN75107B, SN75108A, and SN75108B are characterized for operation from 0°C to 70°C.

design characteristics

The '107A, '107B, '108A, and '108B line receivers are TTL-compatible dual circuits intended for use in high-speed data-transmission systems. They are designed to detect low-level differential signals in the presence of common-mode noise and variations of temperature and supplies. Dc specifications reflect worst-case conditions of temperature, supply voltages, and input voltages.

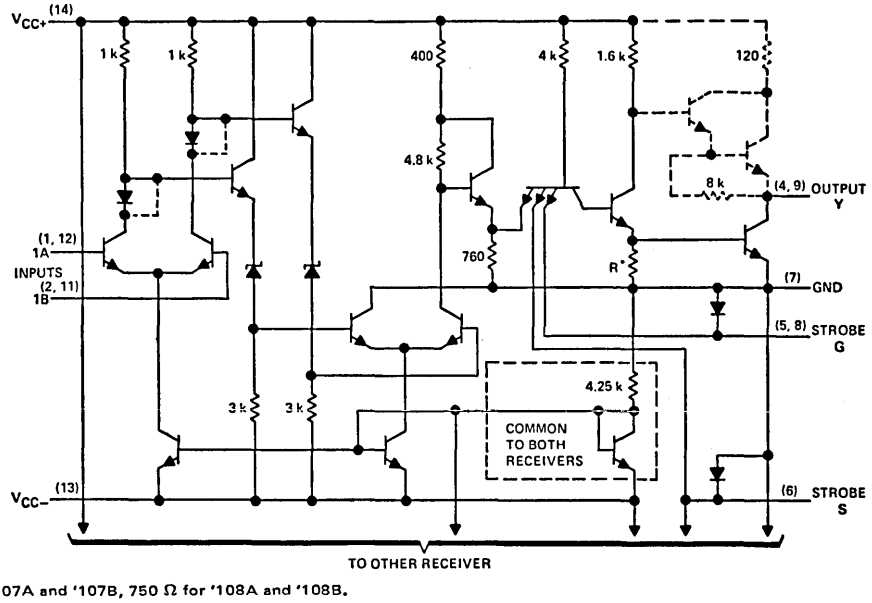
These receivers feature independent channels with common voltage supply and ground terminals. The '107A and '107B feature TTL-compatible active pull-up (totem-pole) outputs. The '108A and '108B are also TTL-compatible, but feature an open-collector output configuration that permits the wired-AND logic connection with similar outputs (such as the SN5401/SN7401 TTL gate or other '108A/'108B line receivers). This permits a level of logic to be implemented without extra delay. All other features of the line receivers are identical.

The input common-mode voltage range is ±3 volts. This is adequate for application in most systems. In systems with requirements for greater common-mode voltage range, input attenuators may be used to decrease the noise to an acceptable level at the receiver-input terminals.

The receivers feature individual strobe inputs for each channel and a strobe input common to both channels for logic versatility. The strobe inputs are tested to guarantee 400 millivolts of dc noise margin when interfaced with Series 54/74 TTL.

The circuits feature high input impedance and low input currents, which induce very little loading on the transmission line. This makes these devices especially useful in party-line systems. The excellent input sensitivity is particularly important when data is to be detected at the end of a long transmission line and the amplitude of the data has deteriorated due to cable losses. These line receivers are designed to detect input signals of 25 millivolts (or greater) amplitude and convert the polarity of the signal into appropriate TTL-compatible output logic levels. For applications that require a greater sensitivity (±10 mV), the SN75207, SN75207B, SN75208, and SN75208B are recommended.

schematic (each receiver)



*R = 1 kΩ for '107A and '107B, 750 Ω for '108A and '108B.

NOTES: A. Resistor values shown are nominal and in ohms.

B. Components shown with dashed lines in the output circuitry are applicable to the '107A and 107B only. Diodes in series with the collectors of the differential input transistors are short-circuited on '107A and '108A.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC+} (see Note 1) . . . . . 7 V
Supply voltage V_{CC-} . . . . . −7 V
Differential input voltage (see Note 2) . . . . . ±6 V
Common-mode input voltage (see Note 3) . . . . . ±5 V
Strobe input voltage . . . . . 5.5 V
Continuous total dissipation at (or below) 70°C free-air temperature (see Note 4) . . . . . 600 mW
Operating free-air temperature range, Series 55 . . . . . −55°C to 125°C
Series 75 . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

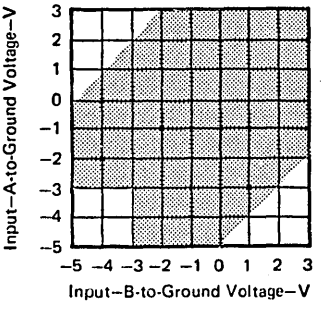
recommended operating conditions (see note 5)

	SN55107A, SN55107B SN55108A, SN55108B			SN75107A, SN75107B SN75108A, SN75108B			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC+}	4.5	5	5.5	4.75	5	5.25	V
Supply voltage V_{CC-}	−4.5	−5	−5.5	−4.75	−5	−5.25	V
Low-level output current, I_{OL}			−16			−16	mA
Differential input voltage, V_{ID} (see Note 6)	−5†		5	−5†		5	V
Common-mode input voltage, V_{IC} (see Notes 6 and 7)	−3†		3	−3†		3	V
Input voltage range, any differential input to ground (see Note 6)	−5†		3	−5†		3	V
Operating free-air temperature, T_A	−55		125	0		70	°C

†The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

NOTES:
1. All voltage values, except differential voltages, are with respect to network ground terminal.
2. Differential voltage values are at the noninverting (A) terminal with respect to the inverting (B) terminal.
3. Common-mode input voltage is the average of the voltages at the A and B inputs.
4. For operation of SN55107A, SN55107B, SN55108A, or SN55108B above 70°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 21. In the J package, these Series 55 chips are alloy-mounted; Series 75 chips are glass-mounted.
5. When using only one channel of the line receiver, the strobe G of the unused channel should be grounded and at least one of the differential inputs of the unused receiver should be terminated at some voltage between −3 V and 3 V.
6. The recommended combinations of input voltages fall within the shaded area of the figure at the right.
7. The common-mode voltage may be as low as −4 V provided that the more positive of the two inputs is not more negative than −3 V.

RECOMMENDED COMBINATIONS OF INPUT VOLTAGES



definition of input logic levels†

		MIN	MAX	UNIT
V_{IDH}	High-level input voltage between differential inputs	0.025	5	V
V_{IDL}	Low-level input voltage between differential inputs	−5	−0.025	V
$V_{IH(S)}$	High-level input voltage at strobe inputs	2	5.5	V
$V_{IL(S)}$	Low-level input voltage at strobe inputs	0	0.8	V

†The algebraic convention where the more positive (less negative) limit is designated as maximum is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS‡		'107A, '107B MIN	'107A, '107B TYP§	'107A, '107B MAX	'108A, '108B MIN	'108A, '108B TYP§	'108A, '108B MAX	UNIT
I_{IH}	High-level input current	A	$V_{CC\pm}$ = MAX	V_{ID} = 5 V		30	75		30	75	μA
		B		V_{ID} = −5 V		30	75		30	75	
I_{IL}	Low-level input current	A	$V_{CC\pm}$ = MAX	V_{ID} = −5 V			−10			−10	μA
		B		V_{ID} = 5 V			−10			−10	
I_{IH}	High-level input current into 1G or 2G		$V_{CC\pm}$ = MAX, $V_{IH(S)}$ = 2.4 V				40			40	μA
			$V_{CC\pm}$ = MAX, $V_{IH(S)}$ = MAX V_{CC+}				1			1	mA
I_{IL}	Low-level input current into 1G or 2G		$V_{CC\pm}$ = MAX, $V_{IL(S)}$ = 0.4 V				−1.6			−1.6	mA
I_{IH}	High-level input current into S		$V_{CC\pm}$ = MAX, $V_{IH(S)}$ = 2.4 V				80			80	μA
			$V_{CC\pm}$ = MAX, $V_{IH(S)}$ = MAX V_{CC+}				2			2	mA
I_{IL}	Low-level input current into S		$V_{CC\pm}$ = MAX, $V_{IL(S)}$ = 0.4 V				−3.2			−3.2	mA
V_{OH}	High-level output voltage		$V_{CC\pm}$ = MIN, $V_{IL(S)}$ = 0.8 V, I_{OH} = −400 μA,	V_{IDH} = 25 mV, V_{IC} = −3 V to 3 V	2.4						V
V_{OL}	Low-level output voltage		$V_{CC\pm}$ = MIN, $V_{IH(S)}$ = 2 V, I_{OL} = 16 mA,	V_{IDL} = −25 mV, V_{IC} = −3 V to 3 V			0.4			0.4	V
I_{OH}	High-level output current		$V_{CC\pm}$ = MIN, V_{OH} = MAX V_{CC+}							250	μA
I_{OS}	Short-circuit output current¶		$V_{CC\pm}$ = MAX		−18		−70				mA
I_{CCH+}	Supply current from V_{CC+}, outputs high		$V_{CC\pm}$ = MAX, T_A = 25°C			18	30		18	30	mA
I_{CCH-}	Supply current from V_{CC-}, outputs high		$V_{CC\pm}$ = MAX, T_A = 25°C			−8.4	−15		−8.4	−15	mA

‡For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

§All typical values are at V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C.
¶Not more than one output should be shorted at a time.

switching characteristics, $V_{CC\pm}$ = ±5 V, T_A = 25°C, see figure 1

PARAMETER		TEST CONDITIONS	'107A, '107B MIN	'107A, '107B TYP	'107A, '107B MAX	'108A, '108B MIN	'108A, '108B TYP	'108A, '108B MAX	UNIT
$t_{PLH(D)}$	Propagation delay time, low-to-high-level output, from differential inputs A and B	R_L = 390 Ω, C_L = 50 pF		17	25				ns
		R_L = 390 Ω, C_L = 15 pF					19	25	
$t_{PHL(D)}$	Propagation delay time, high-to-low-level output, from differential inputs A and B	R_L = 390 Ω, C_L = 50 pF		17	25				ns
		R_L = 390 Ω, C_L = 15 pF					19	25	
$t_{PLH(S)}$	Propagation delay time, low-to-high-level output, from strobe input G or S	R_L = 390 Ω, C_L = 50 pF		10	15				ns
		R_L = 390 Ω, C_L = 15 pF					13	20	
$t_{PHL(S)}$	Propagation delay time, high-to-low-level output, from strobe input G or S	R_L = 390 Ω, C_L = 50 pF		8	15				ns
		R_L = 390 Ω, C_L = 15 pF					13	20	

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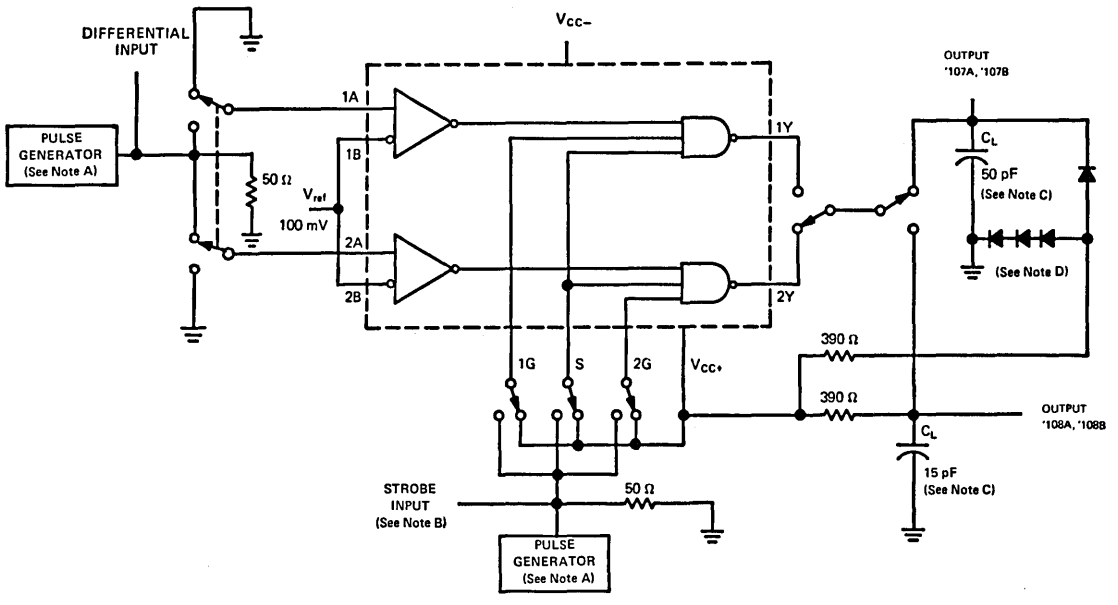
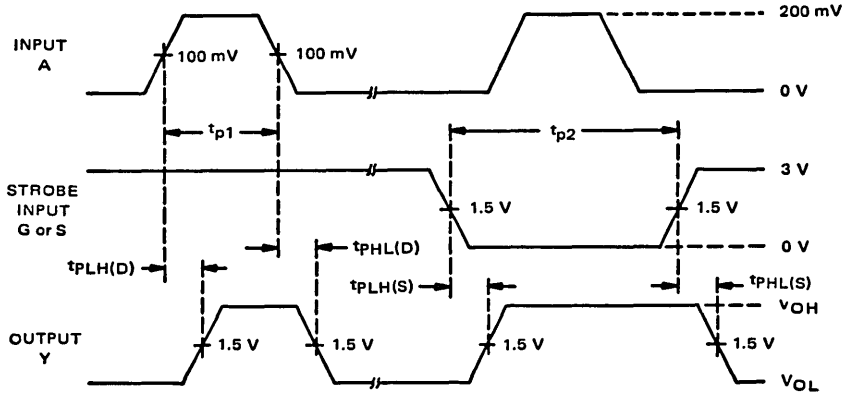
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: Z_{out} = 50 Ω, $t_r = t_f = 10 \pm 5$ ns, t_{p1} = 500 ns, PRR = 1 MHz, t_{p2} = 1 μs, PRR = 500 kHz.

B. Strobe input pulse is applied to Strobe 1G when inputs 1A-1B are being tested, to Strobe S when inputs 1A-1B or 2A-2B are being tested, and to Strobe 2G when inputs 2A-2B are being tested.

C. C_L includes probe and jig capacitance.

D. All diodes are 1N916.

FIGURE 1–PROPAGATION DELAY TIMES

TYPICAL CHARACTERISTICS†

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

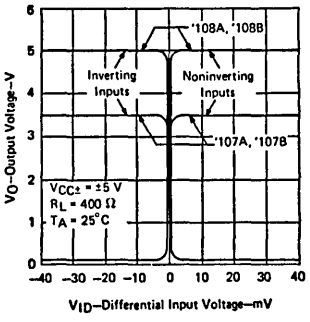


FIGURE 2

HIGH-LEVEL INPUT CURRENT
INTO 1A or 2A
vs
FREE-AIR TEMPERATURE

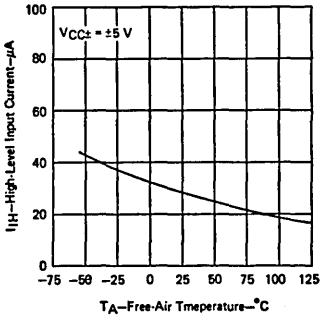


FIGURE 3

SUPPLY CURRENT, OUTPUTS HIGH
vs
FREE-AIR TEMPERATURE

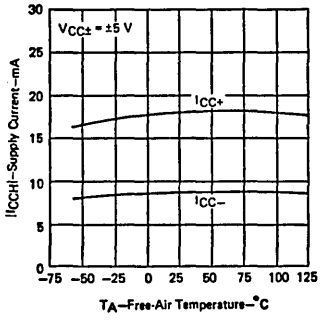


FIGURE 4

'107A, '107B
PROPAGATION DELAY TIME
(DIFFERENTIAL INPUTS)
vs
FREE-AIR TEMPERATURE

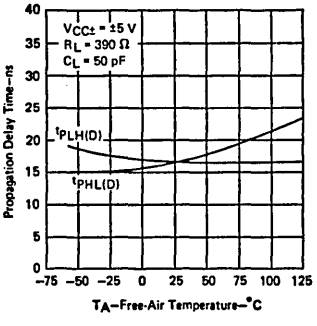


FIGURE 5

'108A, '108B
PROPAGATION DELAY TIME
LOW-TO-HIGH LEVEL
(DIFFERENTIAL INPUTS)
vs
FREE-AIR TEMPERATURE

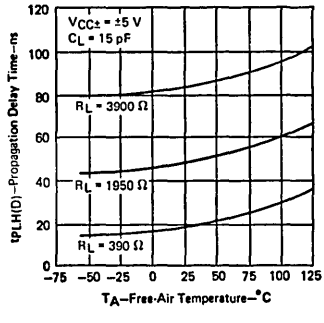


FIGURE 6

'108A, '108B
PROPAGATION DELAY TIME
HIGH-TO-LOW LEVEL
(DIFFERENTIAL INPUTS)
vs
FREE-AIR TEMPERATURE

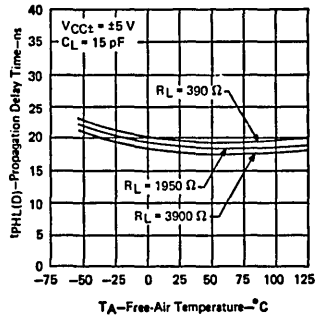


FIGURE 7

'107A, '107B
PROPAGATION DELAY TIME
(STROBE INPUTS)
vs
FREE-AIR TEMPERATURE

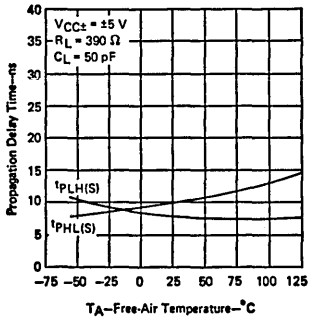


FIGURE 8

'108A, '108B
PROPAGATION DELAY TIME
(STROBE INPUTS)
vs
FREE-AIR TEMPERATURE

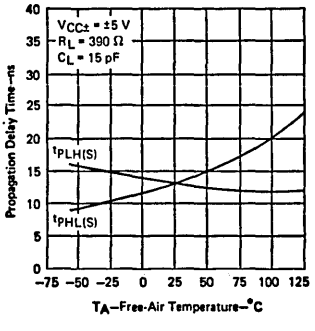


FIGURE 9

†Data for temperatures below 0°C and above 70°C are applicable for Series 55 devices only.

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TYPICAL APPLICATION DATA

basic balanced-line transmission system

The '107A, '107B, '108A, and '108B dual line circuits are designed specifically for use in high-speed data transmission systems that utilize balanced, terminated transmission lines such as twisted-pair lines. The system operates in the balanced mode, so noise induced on one line is also induced on the other. The noise appears common-mode at the receiver input terminals where it is rejected. The ground connection between the line driver and receiver is not part of the signal circuit so that system performance is not affected by circulating ground currents.

The unique driver-output circuit allows terminated transmission lines to be driven at normal line impedances. High-speed system operation is ensured since line reflections are virtually eliminated when terminated lines are used. Crosstalk is minimized by low signal amplitudes and low line impedances.

The typical data delay in a system is approximately (30 + 1.3 L) nanoseconds, where L is the distance in feet separating the driver and receiver. This delay includes one gate delay in both the driver and receiver.

Data is impressed on the balanced-line system by unbalancing the line voltages with the driver output current. The driven line is selected by appropriate driver-input logic levels. The voltage difference is approximately:

$$V_{DIFF} \approx 1/2\, I_{O(on)} \cdot R_T.$$

High series line resistance will cause degradation of the signal. The receivers, however, will detect signals as low as 25 mV (or less). For normal line resistances, data may be recovered from lines of several thousand feet in length.

Line-termination resistors (R_T) are required only at the extreme ends of the line. For short lines, termination resistors at the receiver only may prove adequate. The signal amplitude will then be approximately:

$$V_{DIFF} \approx I_{O(on)} \cdot R_T.$$

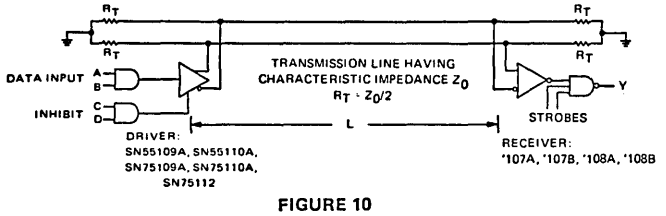

FIGURE 10

data-bus or party-line system

The strobe feature of the receivers and the inhibit feature of the drivers allow these dual line circuits to be used in data-bus or party-line systems. In these applications, several drivers and receivers may share a common transmission line. An enabled driver transmits data to all enabled receivers on the line while other drivers and receivers are disabled. Data is thus time-multiplexed on the transmission line. The device specifications allow widely varying thermal and electrical environments at the various driver and receiver locations. The data-bus system offers maximum performance at minimum cost.

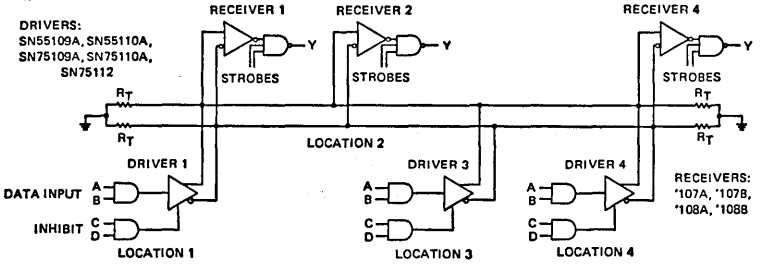

FIGURE 11

TYPICAL APPLICATION DATA

unbalanced or single-line systems

These dual line circuits may also be used in unbalanced or single-line systems. Although these systems do not offer the same performance as balanced systems for long lines, they are adequate for very short lines where environmental noise is not severe.

The receiver threshold level is established by applying a d-c reference voltage to one receiver input terminal. The signal from the transmission line is applied to the remaining input. The reference voltage should be optimized so that signal swing is symmetrical about it for maximum noise margin. The reference voltage should be in the range of −3 volts to +3 volts. It can be provided by a voltage supply or by a voltage divider from an available supply voltage.

A single-ended output from a driver may be used in single-line systems. Coaxial or shielded line is preferred for minimum noise and crosstalk problems. For large signal swings, the high output current (typically 27 mA) of the SN75112 is recommended. Drivers may be paralleled for higher current. When using only one channel of the line drivers, the other channel should be inhibited and/or have its outputs grounded.

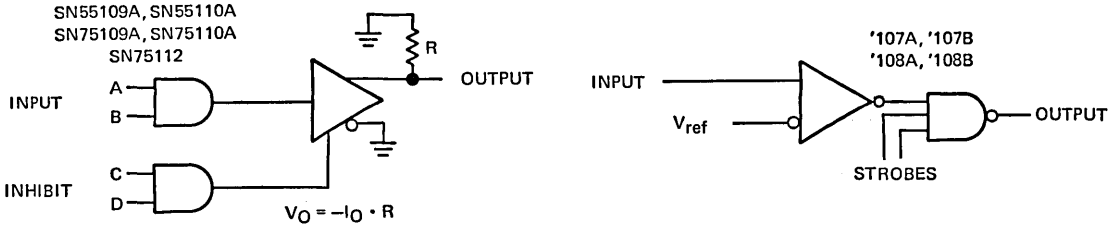

FIGURE 12

'108A, '108B dot-AND output connections

The '108A, '108B line receivers feature an open-collector-output circuit that can be connected in the dot-AND logic configuration with other similar open-collector outputs. This allows a level of logic to be implemented without additional logic delay.

For rules for such dot-AND connections, refer to the SN5401/SN7401 data sheet.

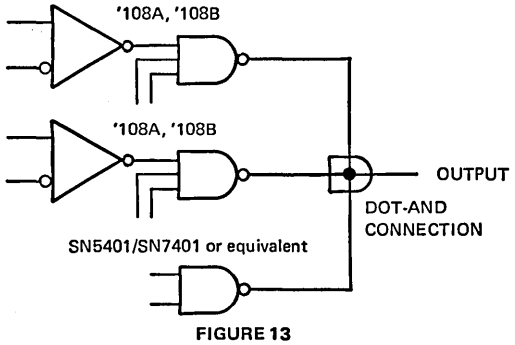

FIGURE 13

increasing common-mode input voltage range of receiver

The common-mode voltage range or CMVR is defined as the range of voltage applied simultaneously to both input terminals that if exceeded does not allow normal operation of the receiver.

The recommended operating CMVR is ±3 volts, making it useful in all but the noisiest environments. In extremely noisy environments, common-mode voltage can easily reach ±10 V to ±15 V if some precautions are not taken to reduce ground and power supply noise, as well as crosstalk problems. When the receiver must operate in such conditions, input attenuators should be used to decrease the system common-mode noise to a tolerable level at the receiver inputs. Differential noise is also reduced by the same ratio.

These attenuators have been intentionally omitted from the receiver input terminals so the designer may select resistors that will be compatible with his particular application or environment. Furthermore, the use of attenuators adversely affects the input sensitivity, the propagation delay time, the power dissipation, and in some cases (depending on the selected resistor values) the input impedance, therefore reducing the versatility of the receiver.

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TYPICAL APPLICATION DATA

increasing common-mode input voltage range of receiver, continued

The ability of the receiver to operate with approximately ±15 volts common-mode voltage at the inputs has been checked using the circuit shown in Figure 14. The resistors R1 and R2 provide a voltage divider network. Dividers with three different values presenting a 5-to-1 attenuation were used so as to operate the differential inputs at approximately ±3 volts common-mode voltage. Careful matching of the two attenuators is needed so as to balance the overdrive at the input stage. The resistors used are shown in Table A.

TABLE A

Attenuator 1: R1 = 2 kΩ, R2 = 0.5 kΩ
Attenuator 2: R1 = 6 kΩ, R2 = 1.5 kΩ
Attenuator 3: R1 = 12 kΩ, R2 = 3 kΩ

Table B shows some of the typical switching results obtained under such conditions.

TABLE B – TYPICAL PROPAGATION DELAYS FOR RECEIVER WITH ATTENUATOR TEST CIRCUIT SHOWN IN FIGURE 14

DEVICE	PARAMETERS	INPUT ATTENUATOR	TYPICAL (ns)
'107A, '107B	t_{PLH}	1	20
		2	32
		3	42
	t_{PHL}	1	22
		2	31
		3	33
'108A, '108B	t_{PLH}	1	36
		2	47
		3	57
	t_{PHL}	1	29
		2	38
		3	41

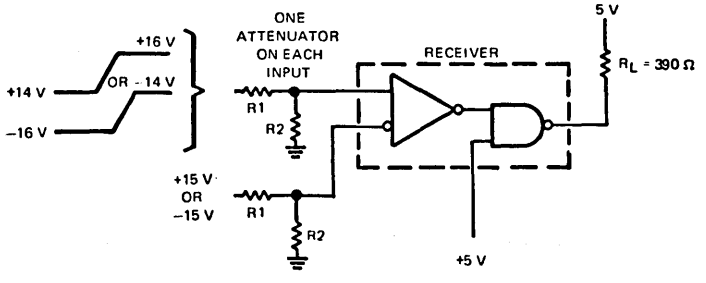

FIGURE 14–COMMON-MODE CIRCUIT FOR TESTING INPUT ATTENUATORS, WITH RESULTS SHOWN IN TABLE B

Two methods of terminating a transmission line to reduce reflections are:

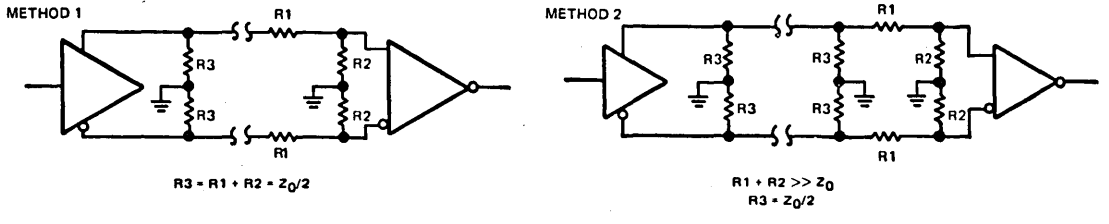

FIGURE 15

The first method uses the resistors as the attenuation network and line termination. The second method uses two additional resistors for the line terminations.

TYPICAL APPLICATION DATA

increasing common-mode input voltage range of receiver, continued

For party-line operation, method 2 should be used as follows:

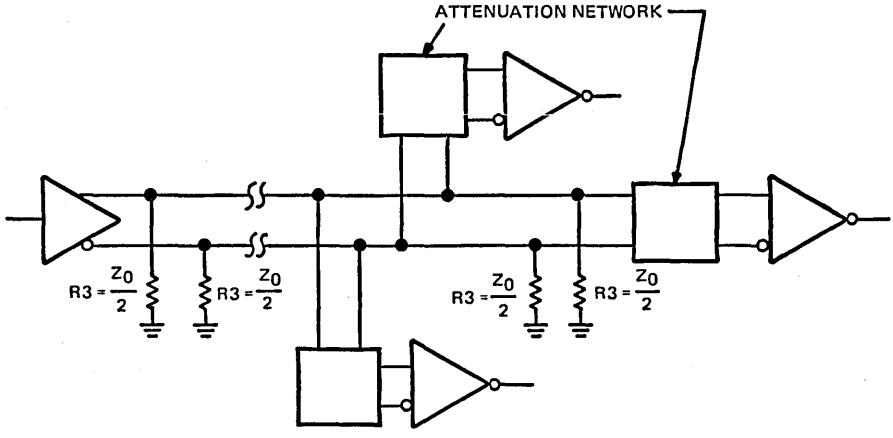

FIGURE 16

To minimize the loading, the values of R1 and R2 should be fairly large. Examples of possible values are shown in Table A.

furnace control using the SN75108A

The furnace control circuit in Figure 17 is an example of the possible use of the SN55107A Series in areas other than what would normally be considered electronic systems. Basically the operation of this control is as follows. When the room temperature is below the desired level, the resistance of the room temperature sensor is high and channel 1 noninverting input is below (less positive than) the reference level set on the input differential amplifier. This situation causes a low output, operating the "heat on" relay and turning on the heat. The channel 2 noninverting input is below the reference level when the bonnet temperature of the furnace reaches the desired level. This causes a low output, thus operating the blower relay. Normally the furnace is shut down when the room temperature reaches the desired level and the channel 1 output goes high, turning the heat off. The blower remains on as long as the bonnet temperature is high, even after the "heat on" relay is off. There is also a safety switch in the bonnet that shuts the furnace down if the temperature there exceeds desired limitations. The types of temperature-sensing devices and bias-resistor values used are determined by the particular operating conditions encountered.

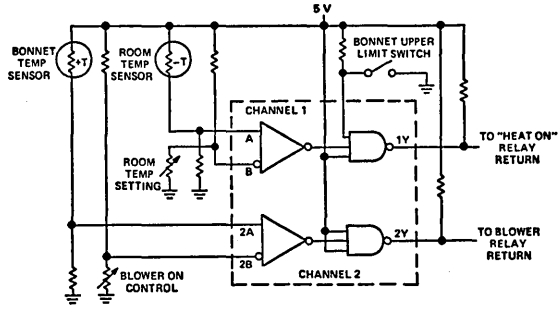

FIGURE 17—FURNACE CONTROL USING SN75108A

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TYPICAL APPLICATION DATA

repeaters for long lines

In some cases, the driven line may be so long that the noise level on the line reaches the common-mode limits or the attenuation becomes too large and results in poor reception. In such a case, a simple application of a receiver and a driver as repeaters (shown in Figure 18a) restores the signal level and allows an adequate signal level at the receiving end. If multichannel operation is desired, then proper gating for each channel must be sent through the repeater station using another repeater set as in Figure 18b.

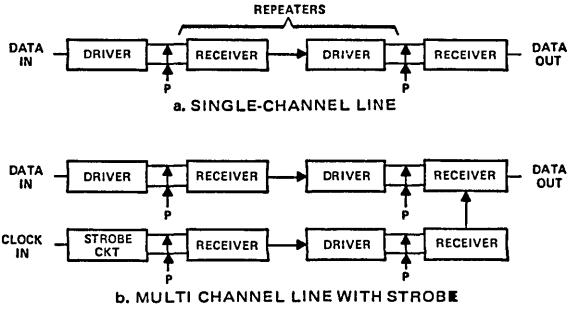


FIGURE 18–RECEIVER-DRIVER REPEATERS

receiver as dual differential comparator

There are many applications for differential comparators, such as voltage comparison, threshold detection, controlled Schmitt triggering, and pulse width control.

As a differential comparator, a '107A or '108A may be connected so as to compare the noninverting input terminal with the inverting input as shown in Figure 19. Thus the output will be high or low resulting from the A input being greater or less than the reference. The strobe inputs allow additional control over the circuit so that either output or both may be inhibited.

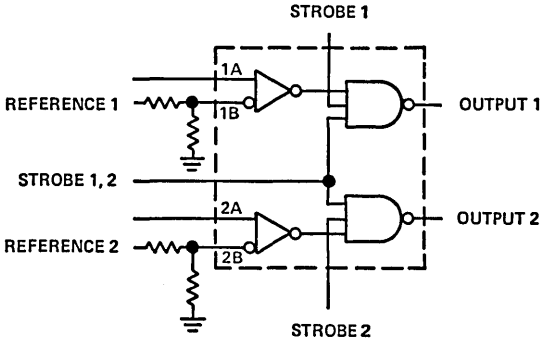
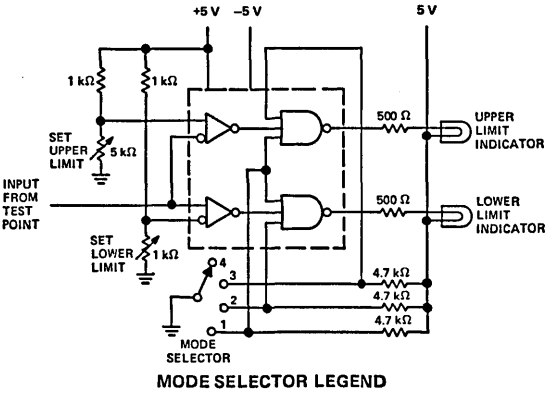


FIGURE 19–SN55107A SERIES RECEIVER AS A DUAL DIFFERENTIAL COMPARATOR

window detector

The window detector circuit in Figure 20 has a large number of applications in test equipment and in determining upper limits, lower limits, or both at the same time – such as detecting whether a voltage or signal has exceeded its limits or "window". Illumination of the upper-limit (lower-limit) indicator shows that the input voltage is above (below) the selected upper (lower) limit. A mode selector is provided for selecting the desired test. For window detecting, the "upper and lower limits" test position is used.



MODE SELECTOR LEGEND

POSITION	CONDITION
1	OFF
2	TEST FOR UPPER LIMIT
3	TEST FOR LOWER LIMIT
4	TEST FOR UPPER AND LOWER LIMITS

FIGURE 20–WINDOW DETECTOR USING SN75108A

TYPICAL APPLICATION DATA

temperature controller with zero-voltage switching

The circuit in Figure 21 switches an electric resistive heater on or off by providing negative-going pulses to the gate of a triac during the time interval when the line voltage is passing through zero. The pulse generator is the 2N5447 and four diodes. This portion of the circuit provides negative-going pulses during the short time (approximately 100 μs) when the line voltage is near zero. These pulses are fed to the inverting input of one channel of the '108A. If the room temperature is below the desired level, the resistance of the thermistor is high and the noninverting input of channel 2 is above the reference level determined by the thermostat setting. This provides a high-level output from channel 2. This output is AND'ed with the positive-going pulses from the output of channel 1, which are reinverted in the 2N5449.

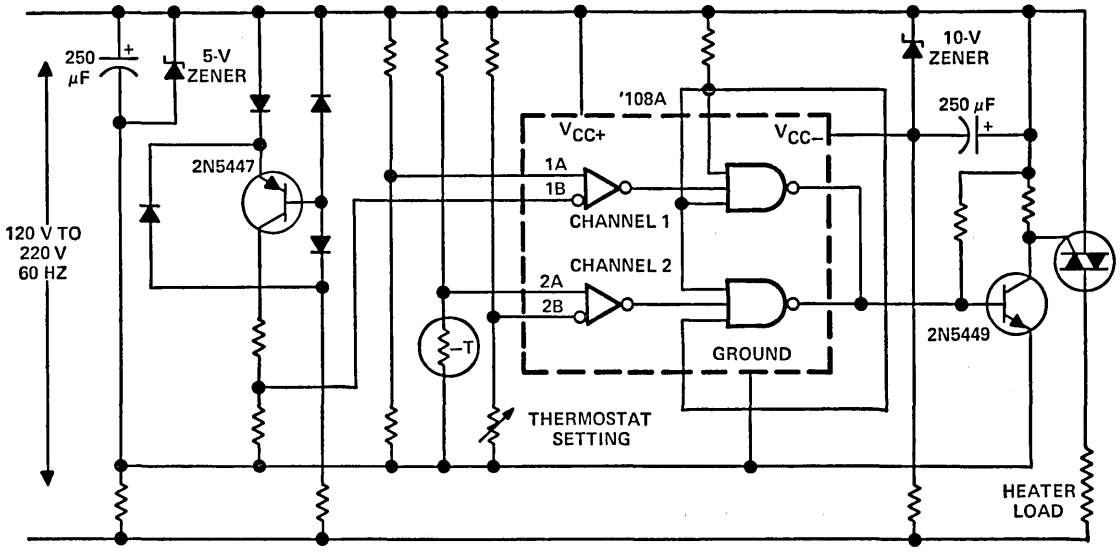


FIGURE 21–ZERO-VOLTAGE SWITCHING TEMPERATURE CONTROLLER

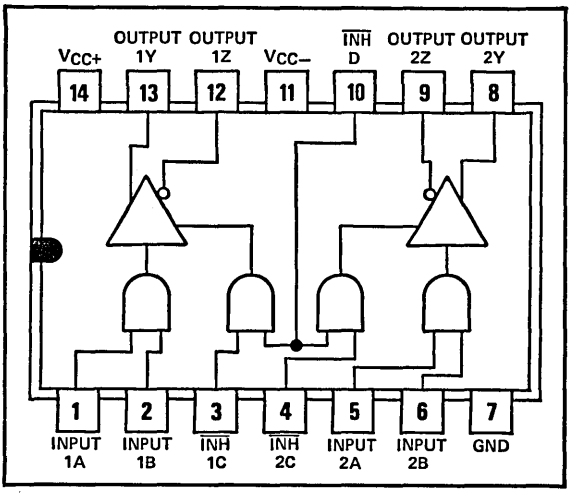
TYPES SN55109A, SN55110A, SN75109A, SN75110A, SN75112 DUAL LINE DRIVERS

BULLETIN NO. DL-S 12334, DECEMBER 1975—REVISED JANUARY 1977

- Improved Stability over Supply Voltage and Temperature Ranges
- Constant-Current Output
- High Speed
- Standard Supply Voltages
- High Output Impedance
- High Common-Mode Output Voltage Range (−3 V to 10 V)
- TTL Input Compatibility
- Inhibitor Available for Driver Selection

−55°C to 125°C J Package	0°C to 70°C J or N Package	OUTPUT FUNCTION
SN55109A	SN75109A	6-mA Current Switch
SN55110A	SN75110A	12-mA Current Switch
	SN75112	27-mA Current Switch

SN55109A, SN55110A . . . J DUAL-IN-LINE PACKAGE
SN75109A, SN75110A, SN75112 . . . J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

The SN55109A, SN55110A, SN75109A, SN75110A, and SN75112 have improved output current regulation with supply voltage and temperature variations. In addition the higher current of the SN75112 (27 mA) allows data to be transmitted over longer lines. These drivers offer optimum performance when used with the SN55107A, SN55108A, SN75107A, and SN75108A line receivers.

FUNCTION TABLE

LOGIC INPUTS		INHIBITOR INPUTS		OUTPUTS	
A	B	C	D	Y	Z
X	X	L	X	OFF	OFF
X	X	X	L	OFF	OFF
L	X	H	H	ON	OFF
X	L	H	H	ON	OFF
H	H	H	H	OFF	ON

H = high level, L = low level, X = irrelevant

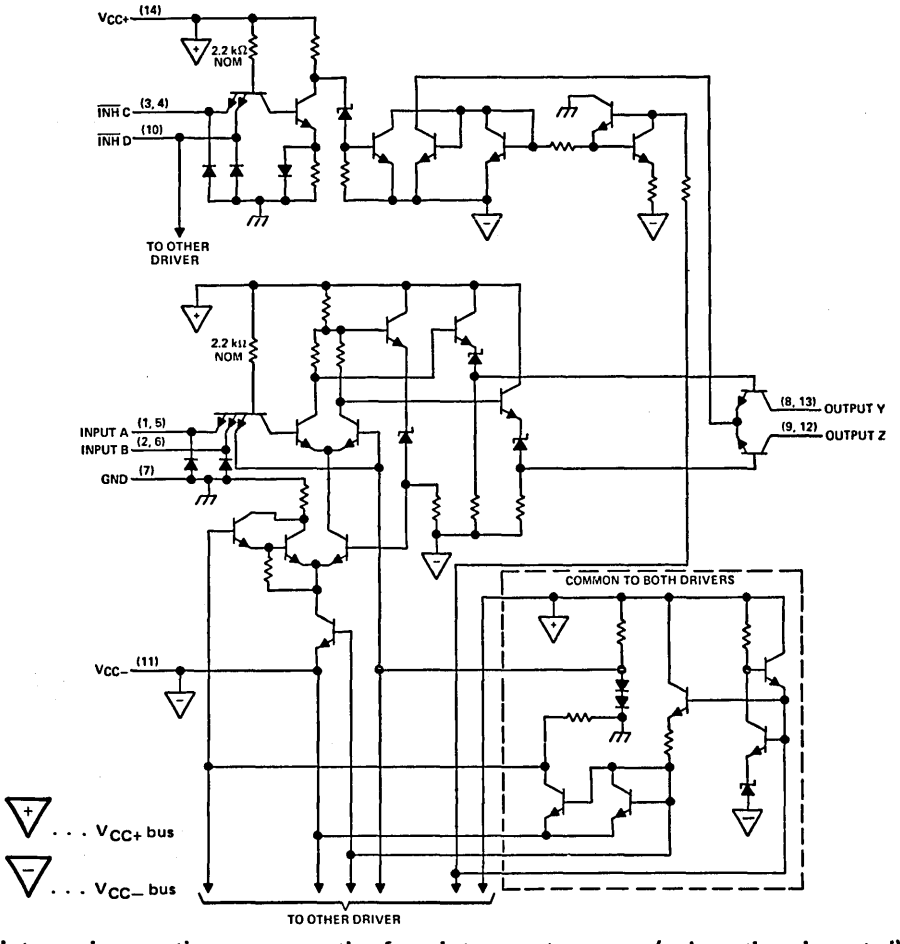
These drivers feature independent channels with common voltage supply and ground terminals. The significant difference between the three drivers is in the output current specification. The driver circuits feature a constant output current that is switched to either of two output terminals by the appropriate logic levels at the input terminals. The output current can be switched off (inhibited) by low logic levels on the inhibit inputs. The output current is nominally 6 milliamperes for the '109A, 12 milliamperes for the '110A, and 27 milliamperes for the SN75112.

The inhibit feature is provided so the circuits can be used in party-line or data-bus applications. A strobe or inhibitor, common to both drivers, is included for increased driver-logic versatility. The output current in the inhibited mode, $I_{O(off)}$, is specified so that minimum line loading is induced when the driver is used in a party-line system with other drivers. The output impedance of the driver in the inhibited mode is very high—the output impedance of a transistor biased to cutoff.

The driver outputs have a common-mode voltage range of −3 volts to 10 volts, allowing common-mode voltage on the line without affecting driver performance.

All inputs are diode clamped and are designed to satisfy TTL-system requirements. The inputs are tested at 2.0 volts for high-logic-level input conditions and 0.8 volt for low-logic-level input conditions. These tests guarantee 400 millivolts of noise margin when interfaced with Series 54/74 TTL.

schematic (each driver)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC+} (see Note 1)	7 V
Supply voltage, V_{CC-}	−7 V
Input voltage (any input)	5.5 V
Output voltage (any output)	−5 V to 12 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2): J package	1025 mW
N package	1150 mW
Operating free-air temperature, Series 55	−55°C to 125°C
Series 75	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch fromcase for 60 seconds: J package	300°C
Lead temperature 1/16 inch fromcase for 10 seconds: N package	260°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 21. In the J package, SN55109A and SN55110A chips are alloy-mounted; SN75109A, SN75110A, and SN75112 chips are glass-mounted.

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recommended operating conditions (see note 3)

	SN55109A, SN55110A			SN75109A, SN75110A, SN75112			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC+}	4.5	5	5.5	4.75	5	5.25	V
Supply voltage V_{CC-}	−4.5	−5	−5.5	−4.75	−5	−5.25	V
Positive common-mode output voltage	0		10	0		10	V
Negative common-mode output voltage	0		−3	0		−3	V
Operating free-air temperature, T_A	−55		125	0		70	°C

NOTE 3: When using only one channel of the line drivers, the other channel should be inhibited and/or its outputs grounded.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†	SN55109A, SN75109A			SN55110A, SN75110A			SN75112			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8			0.8	V
V_{IK}	Input clamp voltage		$V_{CC\pm}$ = MIN, I_I = −12 mA		−0.9	−1.5		−0.9	−1.5		−0.9	−1.5	V
$I_{O(on)}$	On-state output current		$V_{CC\pm}$ = MAX, V_O = 10 V		6	7		12	15		27	36	mA
			$V_{CC\pm}$ = MIN, V_O = −3 V	3.5	6		6.5	12		18	27		
$I_{O(off)}$	Off-state output current		$V_{CC\pm}$ = MIN, V_O = 10 V			100			100			100	μA
I_I	Input current at maximum input voltage	A, B, or C inputs	$V_{CC\pm}$ = MAX, V_I = 5.5 V			1			1			1	mA
		D input				2			2			2	
I_{IH}	High-level input current	A, B, or C inputs	$V_{CC\pm}$ = MAX, V_I = 2.4 V			40			40			40	μA
		D input				80			80			80	
I_{IL}	Low-level input current	A, B, or C inputs	$V_{CC\pm}$ = MAX, V_I = 0.4 V			−3			−3			−3	mA
		D input				−6			−6			−6	
$I_{CC+(on)}$	Supply current from V_{CC+} with driver enabled		$V_{CC\pm}$ = MAX, A and B inputs at 0.4 V, C and D inputs at 2 V		18	30		23	35		25	40	mA
$I_{CC-(on)}$	Supply current from V_{CC-} with driver enabled				−18	−30		−34	−50		−65	−100	
$I_{CC+(off)}$	Supply current from V_{CC+} with driver inhibited		$V_{CC\pm}$ = MAX, A, B, C, and D inputs at 0.4 V		18			21			30		mA
$I_{CC-(off)}$	Supply current from V_{CC-} with driver inhibited				−10			−17			−32		

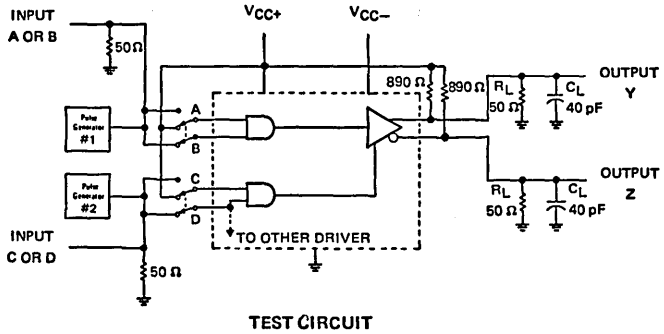
†For conditions shown as MIN or MAX, use appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C.

switching characteristics, V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C

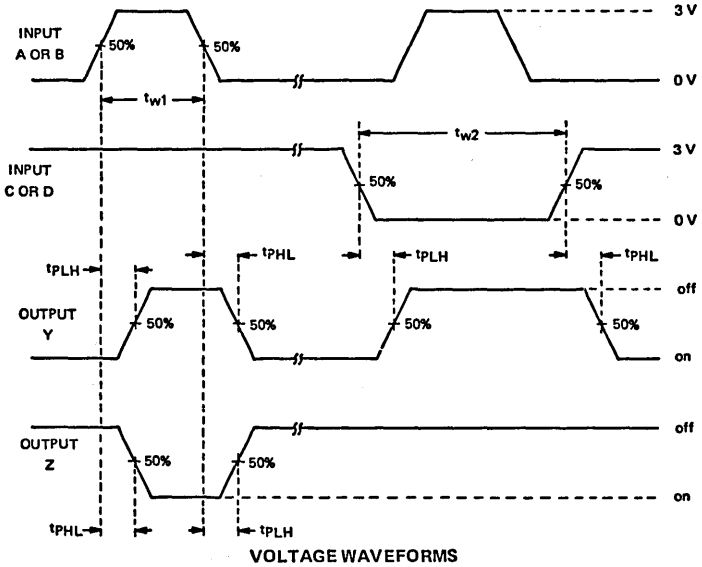
PARAMETER§	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	A or B	Y or Z	C_L = 40 pF, R_L = 50 Ω, See Figure 1		9	15	ns
t_{PHL}					9	15	ns
t_{PLH}	C or D	Y or Z			16	25	ns
t_{PHL}					13	25	ns

§t_{PLH} ≡ Propagation delay time, low-to-high-level output.
t_{PHL} ≡ Propagation delay time, high-to-low-level output.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: Z_{out} = 50 Ω, $t_r = t_f$ = 10 ± 5 ns, t_{w1} = 500 ns, PRR = 1 MHz, t_{w2} = 1 μs, PRR = 500 kHz.
B. C_L includes probe and jig capacitance.
C. For simplicity, only one channel and the inhibitor connections are shown.

FIGURE 1–PROPAGATION DELAY TIMES

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TYPICAL CHARACTERISTICS

ON-STATE OUTPUT CURRENT vs NEGATIVE SUPPLY VOLTAGE

SN55109A, SN75109A

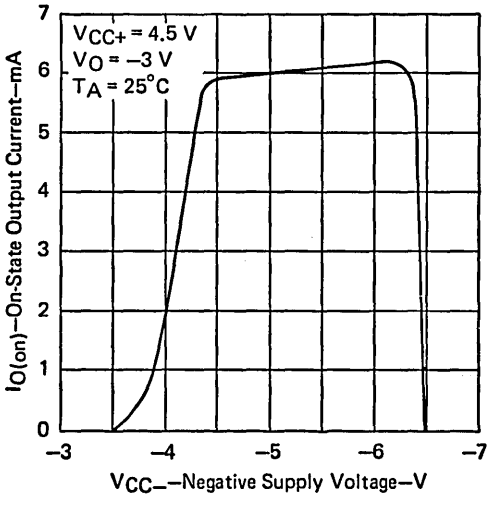

FIGURE 2

SN55110A, SN75110A

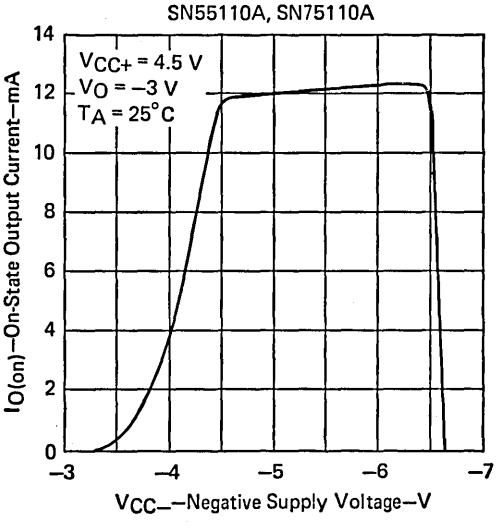

FIGURE 3

SN75112

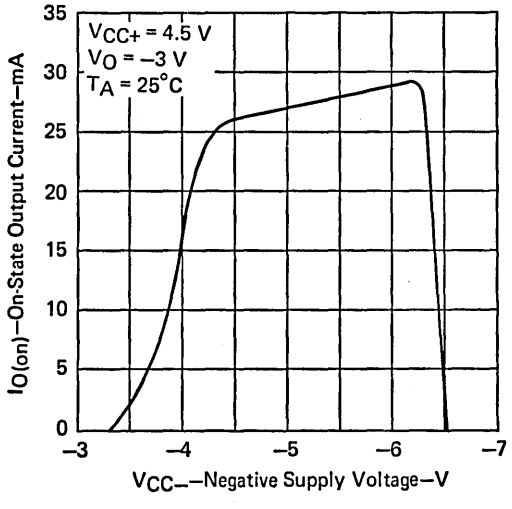

FIGURE 4

TYPICAL APPLICATION INFORMATION

basic balanced-line transmission system

The '109A, '110A, and SN75112 dual line drivers are designed specifically for use in high-speed data transmission systems that utilize balanced, terminated transmission lines such as twisted-pair lines. The system operates in the balanced mode, so that noise induced on one line is also induced on the other. The noise appears common-mode at the receiver input terminals, where it is rejected. The ground connection between the line driver and receiver is not part of the signal circuit so that system performance is not affected by circulating ground currents.

The unique driver-output circuit allows terminated transmission lines to be driven at normal line impedances. High-speed system operation is ensured since line reflections are virtually eliminated when terminated lines are used. Crosstalk is minimized by low signal amplitudes and low line impedances.

The typical data delay in a system is approximately (30 + 1.3L) nanoseconds, where L is the distance in feet separating the driver and receiver. This delay includes one gate delay in both the driver and receiver.

Data is impressed on the balanced-line system by unbalancing the line voltages with the driver output current. The driven line is selected by appropriate driver-input logic levels. The voltage difference is approximately: $V_{DIFF} \approx 1/2\, I_{O(on)} \cdot R_T$

High series line resistance will cause degradation of the signal. However, line receivers such as the SN55107A, SN55108A, SN75107A, and SN75108A will detect signal as low as 25 mV (or less). For normal line resistances, data may be recovered from lines of several thousand feet in length.

Line-termination resistors (R_T) are required only at the extreme ends of the line. For short lines, termination resistors at the receiver only may prove adequate. The signal amplitude will then be approximately: $V_{DIFF} \approx I_{O(on)} \cdot R_T$

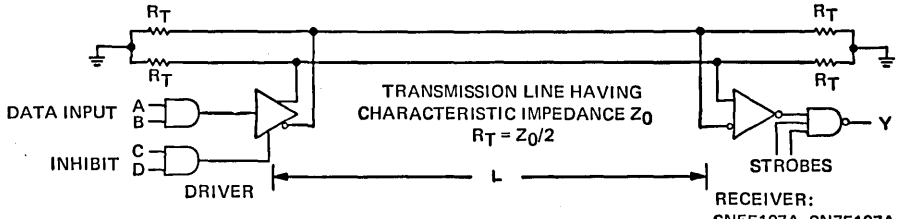

FIGURE 5

data-bus or party-line system

The strobe feature of the '109A, '110A, and SN75112 line drivers allow these circuits to be used in data-bus or party-line systems. In these applications, several drivers and receivers may share a common transmission line. An enabled driver transmits data to all enabled receivers on the line while other drivers are disabled. This series of drivers has been designed to allow widely varying thermal and electrical environments at the various terminal locations. The data-bus system offers maximum performance at minimum cost.

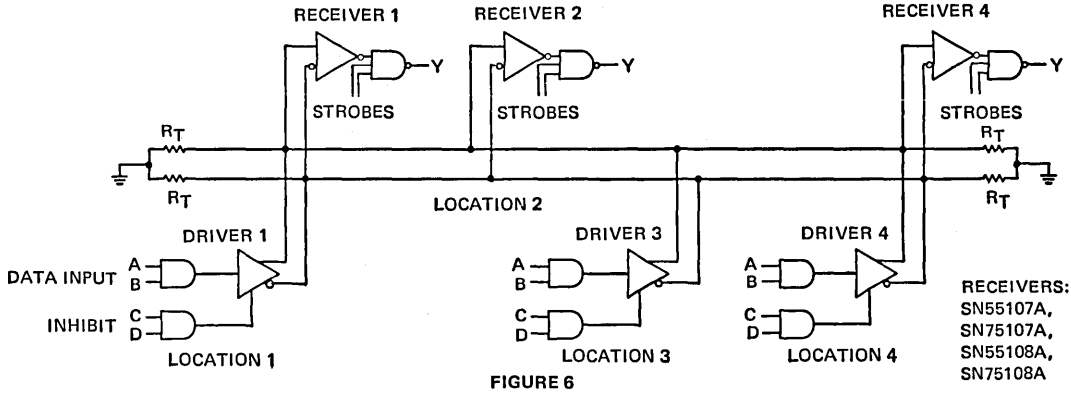

FIGURE 6

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TYPICAL APPLICATION DATA

special pulse-control circuit

Figure 7 shows a circuit that may be used as a pulse generator output or in many other testing applications.

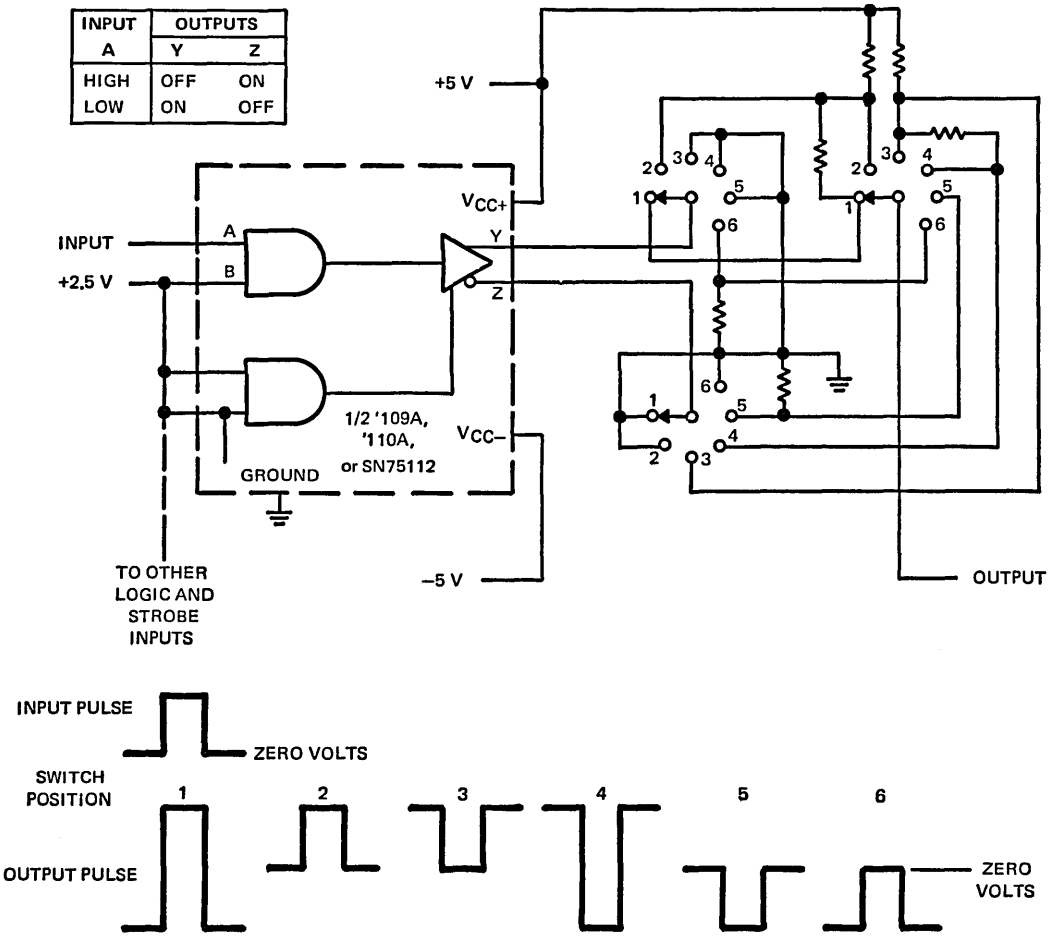


FIGURE 7–PULSE CONTROL CIRCUIT

TYPES SN55113, SN55114, SN55115, SN75113, SN75114, SN75115
DUAL DIFFERENTIAL DRIVERS AND RECEIVERS

BULLETIN NO. DL-S 11910, SEPTEMBER 1973—REVISED SEPTEMBER 1980

LINE CIRCUITS
featuring

- Each Circuit Offers Choice of Open-Collector or Active Pull-Up (Totem-Pole) Outputs
- Single 5-V Supply
- Differential Line Operation
- Dual Channels
- TTL/DTL Compatibility

additional features of SN55113 and SN75113 line drivers with three-state outputs

- High-Impedance Output State for Party-Line Applications
- Short-Circuit Protection
- High-Current Outputs
- Single-Ended or Differential AND/NAND Outputs
- Common and Individual Output Controls
- Clamp Diodes at Inputs
- Easily Adaptable to SN55114 and SN75114 Applications

additional features of SN55114 and SN75114 line drivers

- Designed to be Interchangeable with Fairchild 9614 Line Drivers
- Short-Circuit Protection of Outputs
- High-Current Outputs
- Clamp Diodes at Inputs and Outputs to Terminate Line Transients
- Single-Ended or Differential AND/NAND Outputs
- Triple Inputs

additional features of
SN55115 and SN75115 line receivers

- Designed to be interchangeable with Fairchild 9615 Line Receivers
- ±15 V Common-Mode Input Voltage Range
- Optional-Use Built-In 130-Ω Line-Terminating Resistor
- Individual Frequency Response Controls
- Individual Channel Strobes

CONTENTS

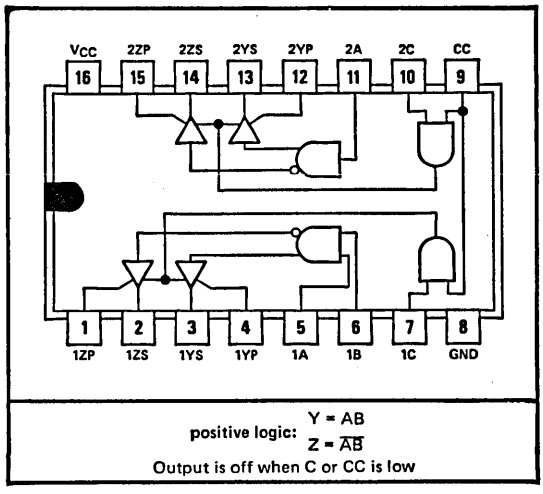
TYPES SN55113, SN75113
DUAL DIFFERENTIAL LINE DRIVERS WITH 3-STATE OUTPUTS

description

The SN55113 and SN75113 dual differential line drivers with three-state outputs are designed to provide all the features of the SN55114 and SN75114 line drivers with the added feature of driver output controls. There are individual controls for each output pair, as well as a common control for both output pairs. When an output control is low, the associated output is in a high-impedance state and the output can neither drive nor load the bus. This permits many devices to be connected together on the same transmission line for party-line applications.

The output stages are similar to TTL totem-pole outputs, but with the sink outputs, YS and ZS, and the corresponding active pull-up terminals, YP and ZP, available on adjacent package pins.

J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: $Y = AB$, $Z = \overline{AB}$

Output is off when C or CC is low

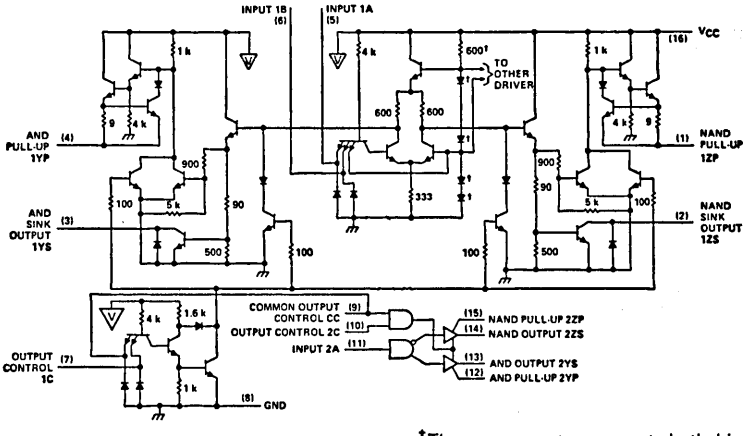
FUNCTION TABLE

INPUTS				OUTPUTS	
OUTPUT CONTROL		DATA		AND	NAND
C	CC	A	B†	Y	Z
L	X	X	X	Z	Z
X	L	X	X	Z	Z
H	H	L	X	L	H
H	H	X	L	L	H
H	H	H	H	H	L

H = high level, L = low level, X = irrelevant, Z = high impedance (off)

†B input and 4th line of function table applicable only to driver number 1.

schematic



▽ . . . V_{CC} bus

Resistor values shown are nominal and in ohms.

†These components common to both drivers.

absolute maximum ratings over operating free-air temperature (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Off-state voltage applied to open-collector outputs	12 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2)	1 W
Operating free-air temperature range: SN55113	−55°C to 125°C
SN75113	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N package	260°C

NOTES: 1. All voltage values are with respect to network ground terminal.

2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 21. In the J package, SN55113 chips are alloy-mounted; SN75113 chips are glass-mounted.

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recommended operating conditions

	SN55113			SN75113			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−40			−40	mA
Low-level output current, I_{OL}			40			40	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

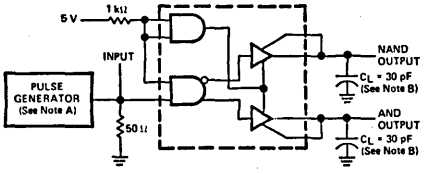
PARAMETER			TEST CONDITIONS†			SN55113			SN75113			UNIT
						MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage					2			2			V
V_{IL}	Low-level input voltage							0.8			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −12 mA			−0.9	−1.5		−0.9	−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V	V_{IH} = 2 V,	I_{OH} = −10 mA	2.4	3.4		2.4	3.4		V
					I_{OH} = −40 mA	2	3.0		2	3.0		
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = 40 mA			0.23	0.4		0.23	0.4	V
V_{OK}	Output clamp voltage		V_{CC} = MAX,	I_O = −40 mA			−1.1	−1.5		−1.1	−1.5	V
$I_{O(off)}$	Off-state open-collector output current		V_{CC} = MAX	V_{OH} = 12 V	T_A = 25°C		1	10				μA
					T_A = 125°C			200				
				V_{OH} = 5.25 V	T_A = 25°C					1	10	
					T_A = 70°C						20	
I_{OZ}	Off-state (high-impedance-state) output current		V_{CC} = MAX, Output controls at 0.8 V	T_A = 25°C,	V_O = 0 to V_{CC}			±10			±10	μA
				T_A = MAX	V_O = 0			−150			−20	
					V_O = 0.4 V			±80			±20	
					V_O = 2.4 V			±80			±20	
					V_O = V_{CC}			80			20	
I_I	Input current at maximum input voltage	A, B, C	V_{CC} = MAX,	V_I = 5.5 V				1			1	mA
		CC						2			2	
I_{IH}	High-level input current	A, B, C	V_{CC} = MAX,	V_I = 2.4 V				40			40	μA
		CC						80			80	
I_{IL}	Low-level input current	A, B, C	V_{CC} = MAX,	V_I = 0.4 V				−1.6			−1.6	mA
		CC						−3.2			−3.2	
I_{OS}	Short-circuit output current§		V_{CC} = MAX,	V_O = 0,	T_A = 25°C	−40	−90	−120	−40	−90	−120	mA
I_{CC}	Supply current (both drivers)		All inputs at 0 V, No load, T_A = 25°C		V_{CC} = MAX		47	65		47	65	mA
					V_{CC} = 7 V		65	85		65	85	

†All parameters with the exception of off-state open-collector output current are measured with the active pull-up connected to the sink output.
‡All typical values are at T_A = 25°C and V_{CC} = 5 V, with the exception of I_{CC} at 7 V.
§Only one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

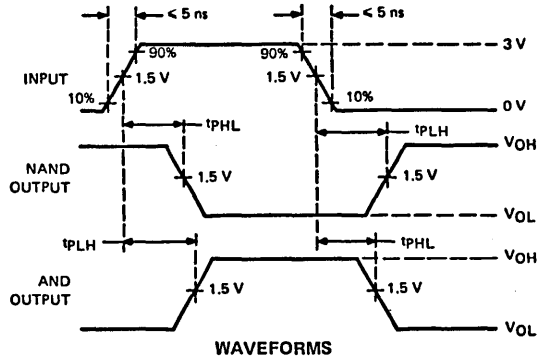
switching characteristics, V_{CC} = 5 V, C_L = 30 pF, T_A = 25°C

PARAMETER		TEST CONDITIONS	SN55113			SN75113			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 1		13	20		13	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output			12	20		12	30	ns
t_{PZH}	Output enable time to high level	R_L = 180 Ω, See Figure 2		7	15		7	20	ns
t_{PZL}	Output enable time to low level	R_L = 250 Ω, See Figure 3		14	30		14	40	ns
t_{PHZ}	Output disable time from high level	R_L = 180 Ω, See Figure 2		10	20		10	30	ns
t_{PLZ}	Output disable time from low level	R_L = 250 Ω, See Figure 3		17	35		17	35	ns

PARAMETER MEASUREMENT INFORMATION

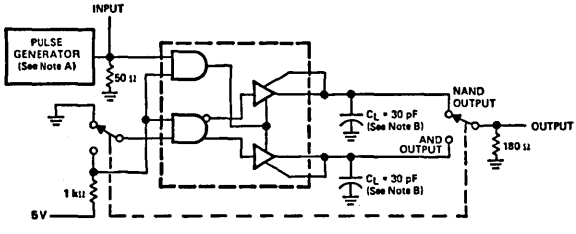


TEST CIRCUIT

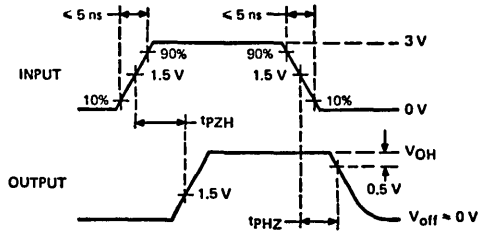


WAVEFORMS

FIGURE 1–t_{PLH} and t_{PHL}

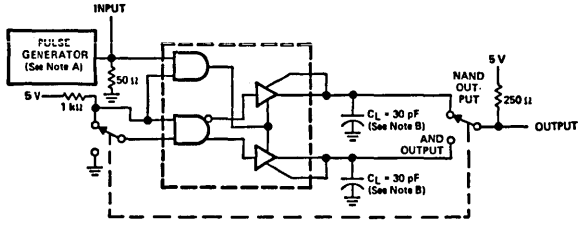


TEST CIRCUIT

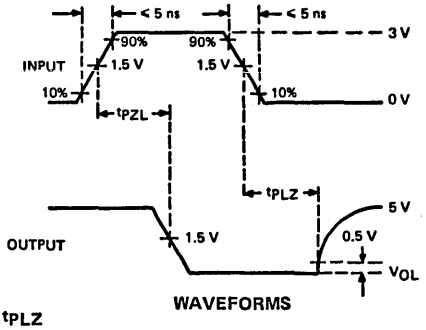


WAVEFORMS

FIGURE 2–t_{PZH} and t_{PHZ}



TEST CIRCUIT



WAVEFORMS

FIGURE 3–t_{PZL} and t_{PLZ}

NOTES: A. The pulse generator has the following characteristics: Z_{out} = 50 Ω, PRR = 500 kHz, t_w = 100 ns.
B. C_L includes probe and jig capacitance.

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TYPICAL CHARACTERISTICS†

OUTPUT VOLTAGE vs DATA INPUT VOLTAGE

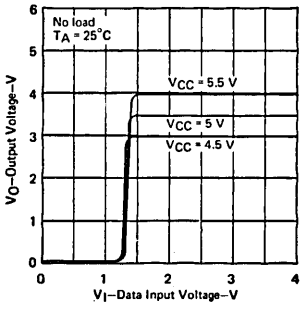

FIGURE 4

OUTPUT VOLTAGE vs DATA INPUT VOLTAGE

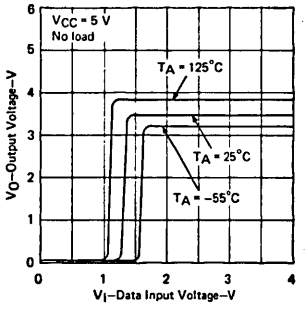

FIGURE 5

OUTPUT VOLTAGE vs OUTPUT CONTROL VOLTAGE

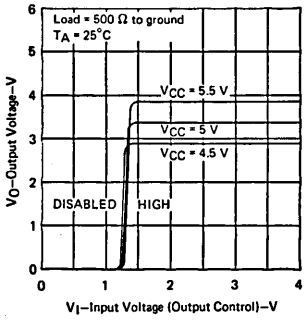

FIGURE 6

OUTPUT VOLTAGE vs OUTPUT CONTROL VOLTAGE

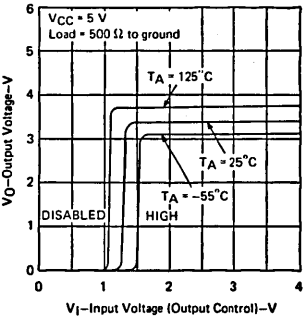

FIGURE 7

OUTPUT VOLTAGE vs OUTPUT CONTROL VOLTAGE

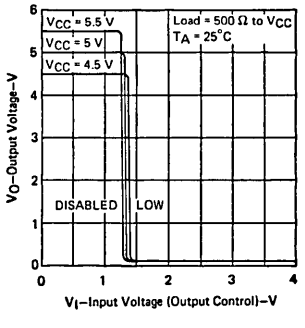

FIGURE 8

OUTPUT VOLTAGE vs OUTPUT CONTROL VOLTAGE

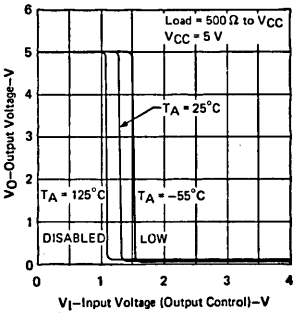

FIGURE 9

†Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75 V and above 5.25 V are applicable to SN55113 circuits only. These parameters were measured with the active pull-up connected to the sink output.

TYPICAL CHARACTERISTICS†

OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

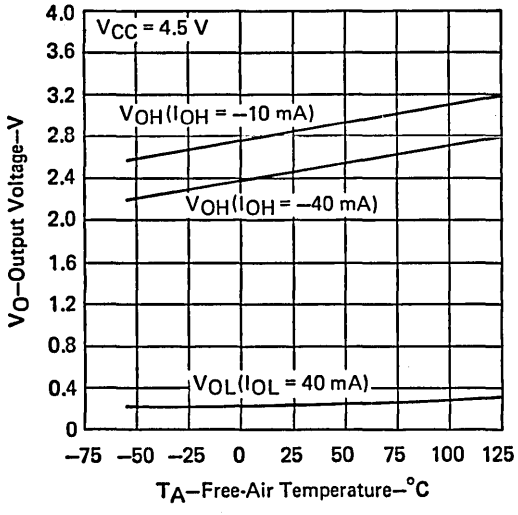

FIGURE 10

HIGH-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

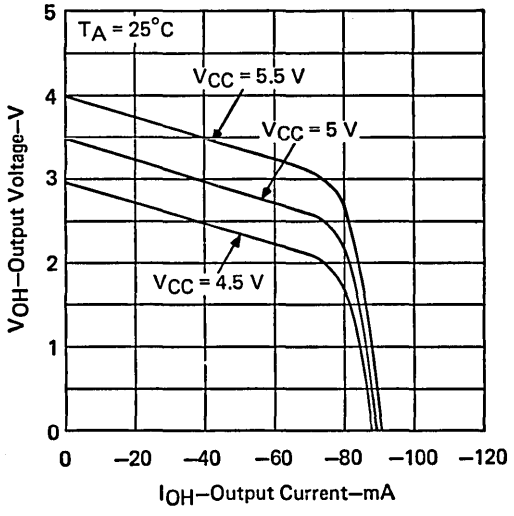

FIGURE 11

LOW-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

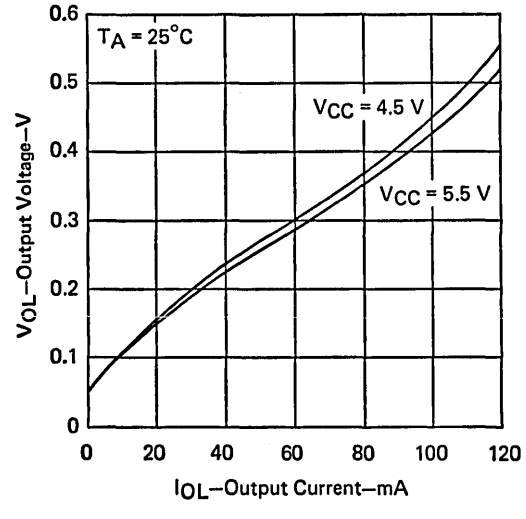

FIGURE 12

SUPPLY CURRENT
(BOTH DRIVERS)
vs
SUPPLY VOLTAGE

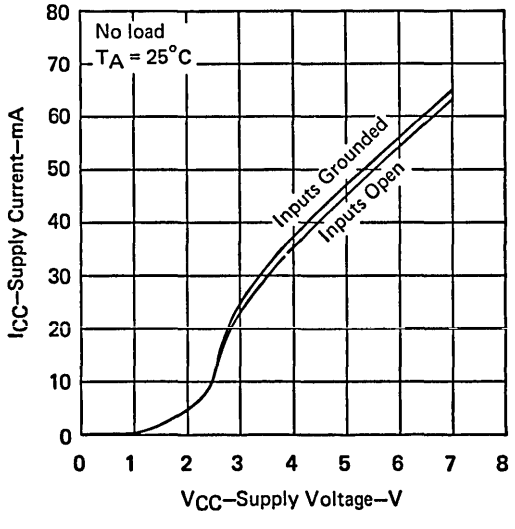

FIGURE 13

†Data for temperature below 0°C and above 70°C and for supply voltages below 4.75 V and above 5.25 V are applicable to SN55113 circuits only. These parameters were measured with the active pull-up connected to the sink output.

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TYPICAL CHARACTERISTICS†

SUPPLY CURRENT
(BOTH DRIVERS)
vs
FREE-AIR TEMPERATURE

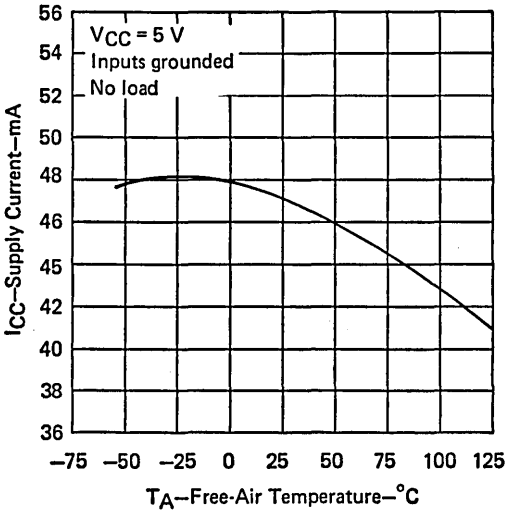


FIGURE 14

SUPPLY CURRENT
(BOTH DRIVERS)
vs
FREQUENCY

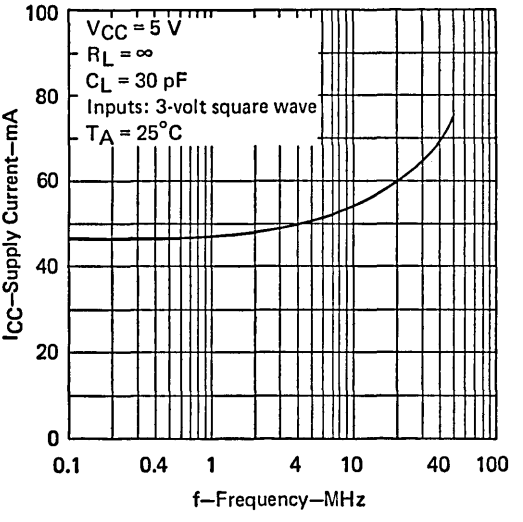


FIGURE 15

PROPAGATION DELAY TIMES
FROM DATA INPUTS
vs
FREE-AIR TEMPERATURE

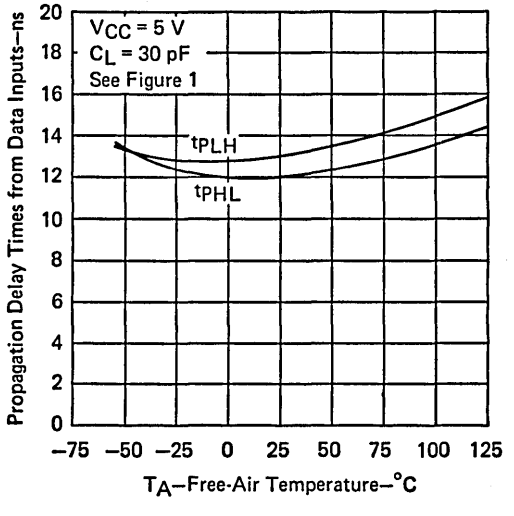


FIGURE 16

OUTPUT ENABLE and DISABLE TIMES
vs
FREE-AIR TEMPERATURE

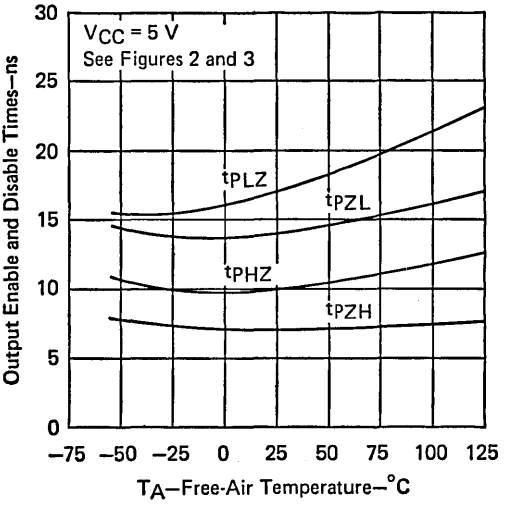


FIGURE 17

†Data for temperature below 0°C and above 70°C and for supply voltages below 4.75 V and above 5.25 V are applicable to SN55113 circuits only. These parameters were measured with the active pull-up connected to the sink output.

TYPES SN55114, SN75114
DUAL DIFFERENTIAL LINE DRIVERS

description

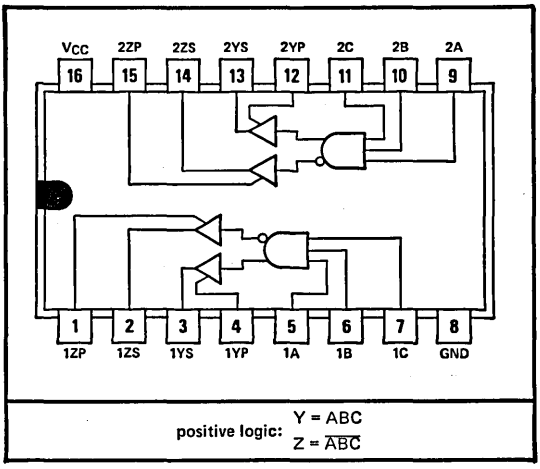
The SN55114 and SN75114 dual differential line drivers are designed to provide differential output signals with high current capability for driving balanced lines, such as twisted-pair at normal line impedances, without high power dissipation. The output stages are similar to TTL totem-pole outputs, but with the sink outputs, YS and ZS, and the corresponding active pull-up terminals, YP and ZP, available on adjacent package pins. Since the output stages provide TTL compatible output levels, these devices may also be used as TTL expanders or phase splitters.

FUNCTION TABLE

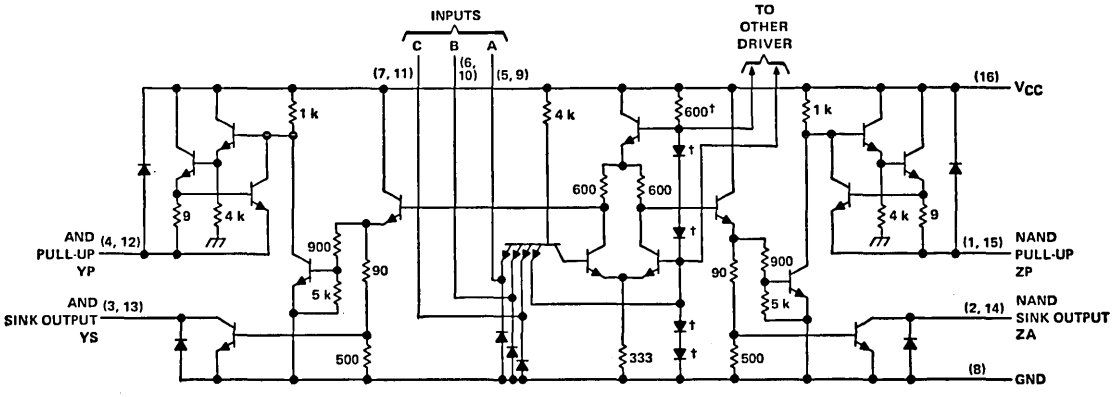
INPUTS			OUTPUTS	
A	B	C	Y	Z
H	H	H	H	L
ALL OTHER INPUT COMBINATIONS			L	H

H = high level, L = low level

J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



schematic (each driver)



†These components common to both drivers.
Resistor values shown are nominal and in ohms.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Off-state voltage applied to open-collector outputs	12 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2)	1 W
Operating free-air temperature range: SN55114	−55°C to 125°C
SN75114	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N package	260°C

NOTES: 1. All voltage values are with respect to network ground terminal.

2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 21. In the J package, SN55114 chips are alloy-mounted; SN75114 chips are glass-mounted.

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recommended operating conditions

	SN55114			SN75114			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−40			−40	mA
Low-level output current, I_{OL}			40			40	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

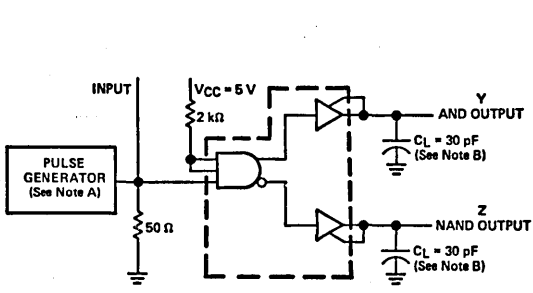
PARAMETER		TEST CONDITIONS†			SN55114			SN75114			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −12 mA			−0.9	−1.5		−0.9	−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V,	I_{OH} = −10 mA	2.4	3.4		2.4	3.4		V
				I_{OH} = −40 mA	2	3.0		2	3.0		
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = 40 mA			0.2	0.4		0.2	0.45	V
V_{OK}	Output clamp voltage	V_{CC} = 5 V,	I_O = 40 mA,	T_A = 25°C		6.1	6.5		6.1	6.5	V
		V_{CC} = MAX,	I_O = −40 mA,	T_A = 25°C		−1.1	−1.5		−1.1	−1.5	
$I_{O(off)}$	Off-state open-collector output current	V_{CC} = MAX	V_{OH} = 12 V	T_A = 25°C		1	100				μA
				T_A = 125°C			200				
			V_{OH} = 5.25 V	T_A = 25°C					1	100	
				T_A = 70°C						200	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4 V				40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			−1.1	−1.6		−1.1	−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX,	V_O = 0,	T_A = 25°C	−40	−90	−120	−40	−90	−120	mA
I_{CC}	Supply current (both drivers)	All inputs at 0 V, No load, T_A = 25°C		V_{CC} = MAX		37	50		37	50	mA
				V_{CC} = 7 V		47	65		47	70	

†All parameters, with the exception of off-state open-collector output current, are measured with the active pull-up connected to the sink output.
‡All typical values are at T_A = 25°C and V_{CC} = 5 V, with the exception of I_{CC} at 7 V.
§Only one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

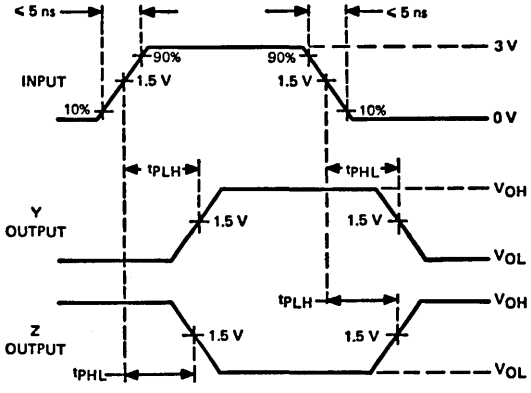
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	SN55114			SN75114			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 30 pF, See Figure 18		15	20		15	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output			11	20		11	30	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: Z_{out} = 50 Ω, t_w = 100 ns, PRR = 500 kHz.
B. C_L includes probe and jig capacitance.

FIGURE 18–PROPAGATION DELAY TIMES

TYPICAL CHARACTERISTICS†

OUTPUT VOLTAGE vs DATA INPUT VOLTAGE

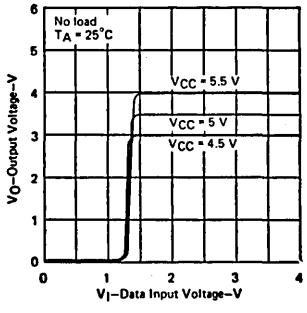


FIGURE 19

OUTPUT VOLTAGE vs DATA INPUT VOLTAGE

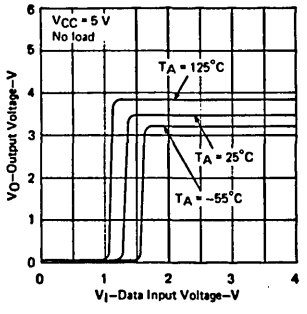


FIGURE 20

HIGH-LEVEL OUTPUT VOLTAGE vs OUTPUT CURRENT

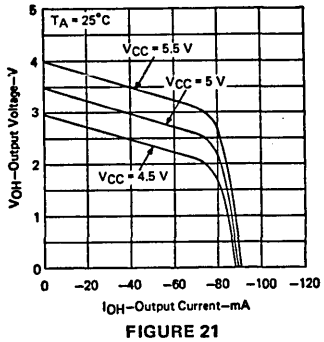


FIGURE 21

LOW-LEVEL OUTPUT VOLTAGE vs OUTPUT CURRENT

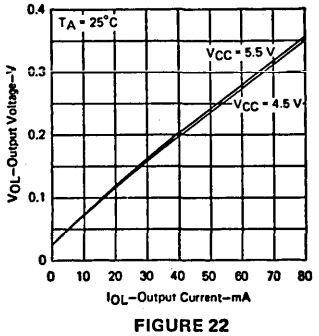


FIGURE 22

†Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75 V and above 5.25 V are applicable to SN55114 circuits only. These parameters were measured with the active pull-up connected to the sink output.

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TYPICAL CHARACTERISTICS†

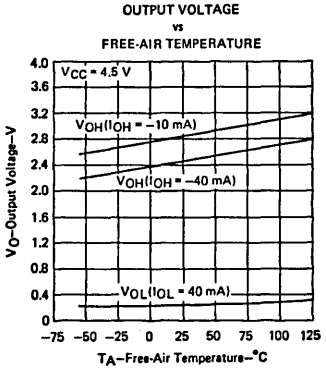


FIGURE 23

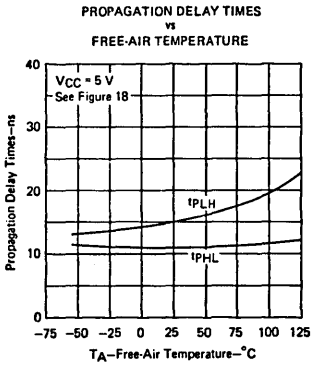


FIGURE 24

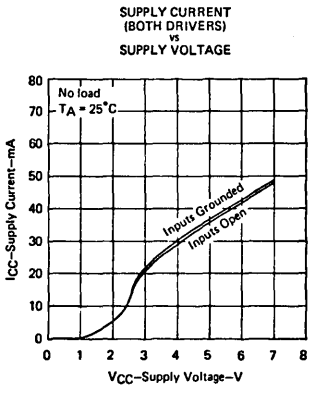


FIGURE 25

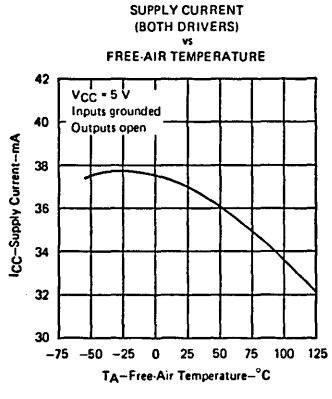


FIGURE 26

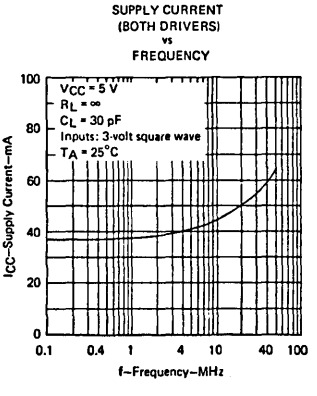


FIGURE 27

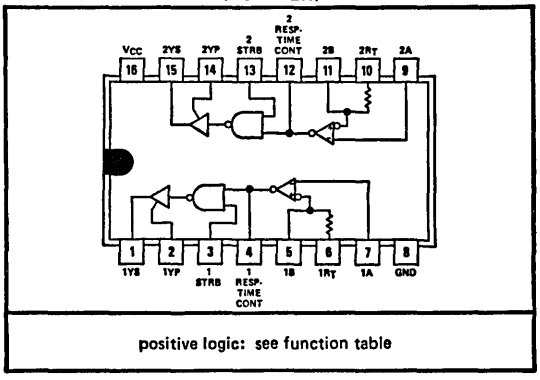
† Data for temperatures below 0°C and above 70°C are applicable to SN55114 circuits only. These parameters were measured with the active pull-up connected to the sink output.

TYPES SN55115, SN75115
DUAL DIFFERENTIAL LINE RECEIVERS

description

The SN55115 and SN75115 dual differential line receivers are designed to sense small differential signals in the presence of large common-mode noise. These devices give TTL-compatible output signals as a function of the polarity of the differential input voltage. The open-collector output configuration permits the wire-AND connection with similar outputs (such as SN5401/SN7401 TTL gates or other SN55115/SN75115 line receivers). This permits a level of logic to be implemented without extra delay. The output stages are similar to TTL totem-pole outputs, but with the sink outputs, 1YS and 2YS, and the corresponding active pull-up terminals, 1YP and 2YP, available on adjacent package pins. The frequency response of each channel may be easily controlled by a single external capacitor to provide immunity to differential noise spikes. A strobe input is provided for each channel. With the strobe in the low level, the receiver is disabled and the outputs are forced to a high level.

J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



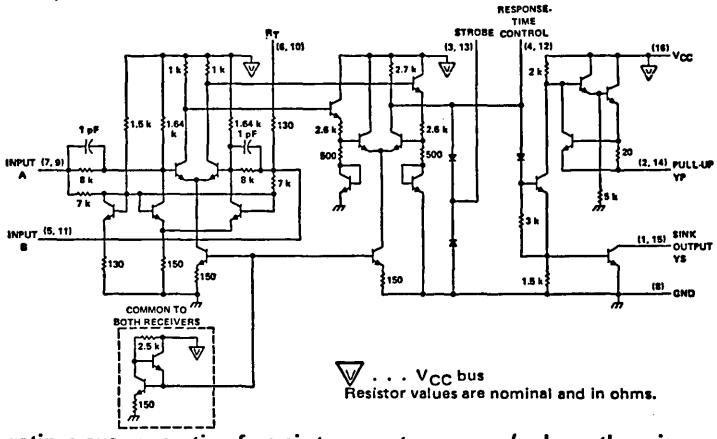
positive logic: see function table

FUNCTION TABLE

STROBE	DIFF INPUT	OUTPUT
L	X	H
H	L	H
H	H	L

H = $V_I \geq V_{IH}$ min or V_{ID} more positive than V_{TH} max
L = $V_I \leq V_{IL}$ max or V_{ID} more negative than V_{TL} max
X = irrelevant

schematic (each receiver)



▽ . . . V_{CC} bus
Resistor values are nominal and in ohms.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage at A, B, and R_T inputs	±25 V
Input voltage at strobe input	5.5 V
Off-state voltage applied to open-collector outputs	14 V
Continuous total dissipation at (or below 25°C free-air temperature (see Note 2)	1 W
Operating free-air temperature range: SN55115	−55°C to 125°C
SN75115	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N package	260°C

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 21. In the J package, SN55115 chips are alloy-mounted; SN75115 chips are glass-mounted.

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recommended operating conditions

	SN55115			SN75115			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−5			−5	mA
Low-level output current, I_{OL}			15			15	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

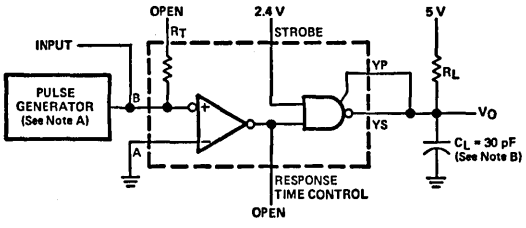
PARAMETER		TEST CONDITIONS†		SN55115			SN75115			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{TH}§	Differential input high-threshold voltage	V_O = 0.4 V, I_{OL} = 15 mA, V_{IC} = 0				500			500	mV
V_{TL}§	Differential input low-threshold voltage	V_O = 2.4 V, I_{OH} = −5 mA, V_{IC} = 0		−500¶			−500¶			mV
V_{ICR}	Common-mode input voltage range	V_{ID} = ±1 V		+15 to −15	+24 to −19		+15 to −15	+24 to −19		V
$V_{IH(strobe)}$	High-level strobe input voltage			2.4			2.4			V
$V_{IL(strobe)}$	Low-level strobe input voltage					0.4			0.4	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{ID} = −0.5 V, I_{OH} = −5 mA	T_A = MIN	2.2			2.4			V
			T_A = 25°C	2.4	3.4		2.4	3.4		
			T_A = MAX	2.4			2.4			
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{ID} = 0.5 V, I_{OL} = 15 mA			0.22	0.4		0.22	0.45	V
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V, Other Input at 5.5 V	T_A = MIN			−0.9			−0.9	mA
			T_A = 25°C		−0.5	−0.7		−0.5	−0.7	
			T_A = MAX			−0.7			−0.7	
I_{SH}	High-level strobe current	V_{CC} = MIN, V_{ID} = −0.5 V, V_{strobe} = 4.5 V	T_A = 25°C			2			5	μA
			T_A = MAX			5			10	
I_{SL}	Low-level strobe current	V_{CC} = MAX, V_{ID} = 0.5 V, V_{strobe} = 0.4 V	T_A = 25°C		−1.15	−2.4		−1.15	−2.4	mA
I_4, I_{12}	Response-time-control current (Pin 4 or Pin 12)	V_{CC} = MAX, V_{ID} = 0.5 V, V_{RC} = 0	T_A = 25°C	−1.2	−3.4		−1.2	−3.4		mA
$I_{O(off)}$	Off-state open-collector output current	V_{CC} = MIN, V_{OH} = 12 V, V_{ID} = −4.5 V	T_A = 25°C			100				μA
			T_A = MAX			200				
		V_{CC} = MIN, V_{OH} = 5.25 V, V_{ID} = −4.75 V	T_A = 25°C						100	
			T_A = MAX						200	
R_T	Line-terminating resistance	V_{CC} = 5 V	T_A = 25°C	77	130	167	74	130	179	Ω
I_{OS}	Short-circuit output current◆	V_{CC} = MAX, V_O = 0, V_{ID} = −0.5 V	T_A = 25°C	−15	−40	−80	−14	−40	−100	mA
I_{CC}	Supply current (both receivers)	V_{CC} = MAX, V_{ID} = 0.5 V, V_{IC} = 0	T_A = 25°C		32	50		32	50	mA

†Unless otherwise noted V_{strobe} = 2.4 V. All parameters with the exception of off-state open-collector output current are measured with the active pull-up connected to the sink output.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C, and V_{IC} = 0.
§Differential voltages are at the B input terminal with respect to the A input terminal.
¶The algebraic convention, where the less-positive (more-negative) limit is designated as minimum, is used in this data sheet for threshold voltages only.
◆Only one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

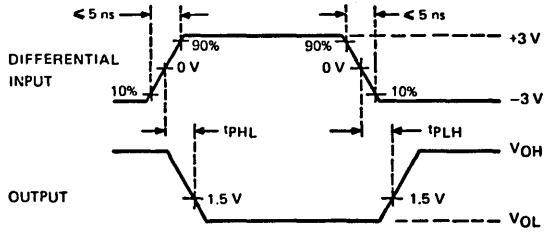
switching characteristics, V_{CC} = 5 V, C_L = 30 pF, T_A = 25°C

PARAMETER	TEST CONDITIONS	SN55115			SN75115			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH} Propagation delay time, low-to-high-level output	R_L = 3.9 kΩ, See Figure 28		18	50		18	75	ns
t_{PHL} Propagation delay time, high-to-low-level output	R_L = 390 Ω, See Figure 28		20	50		20	75	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: Z_{out} = 50 Ω, PRR = 500 kHz, t_w = 100 ns.
B. C_L includes probe and jig capacitance.

FIGURE 28–PROPAGATION DELAY TIMES

TYPICAL CHARACTERISTICS†

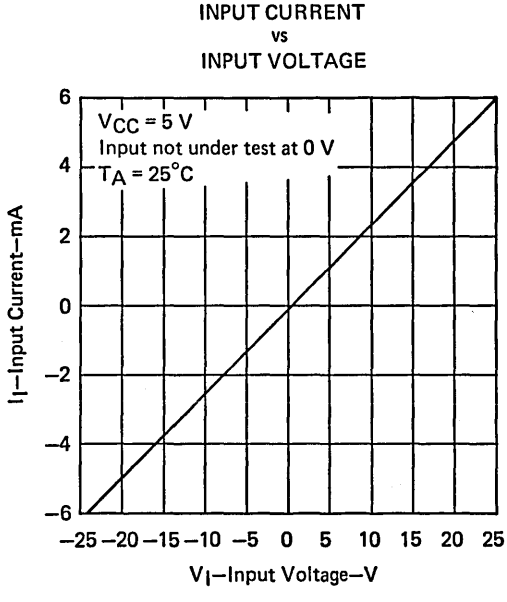


FIGURE 29

†Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75 V and above 5.25 V are applicable to SN55115 circuits only.

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TYPICAL CHARACTERISTICS†

OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

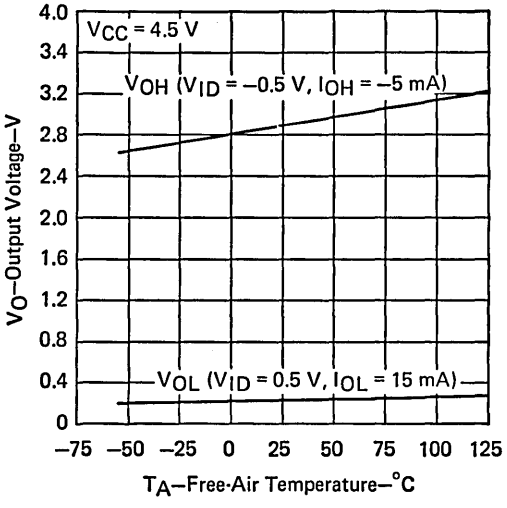

FIGURE 30

OUTPUT VOLTAGE
vs
COMMON-MODE INPUT VOLTAGE

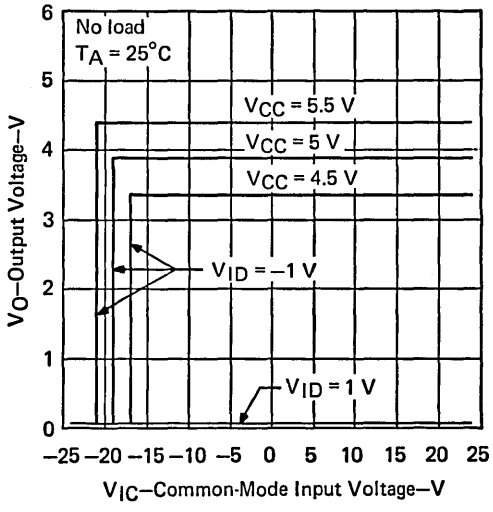

FIGURE 31

HIGH-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

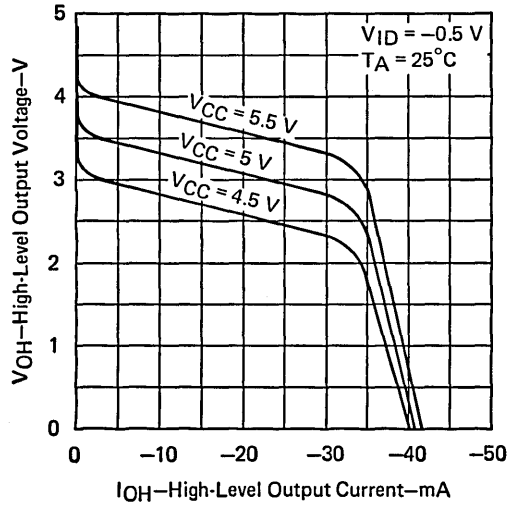

FIGURE 32

LOW-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

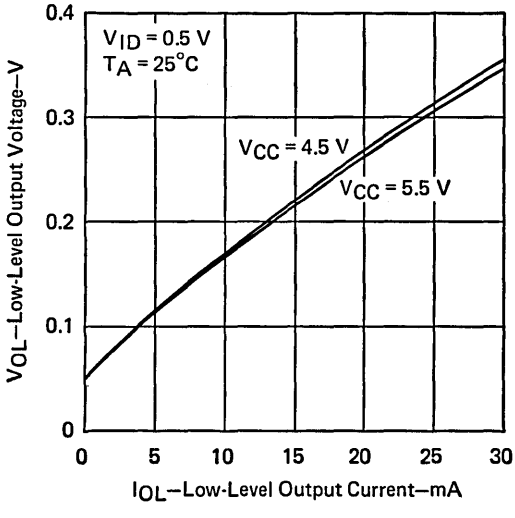

FIGURE 33

†Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75 V and above 5.25 V are applicable to SN55115 circuits only. These parameters were measured with the active pull-up connected to the sink output.

TYPICAL CHARACTERISTICS†

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

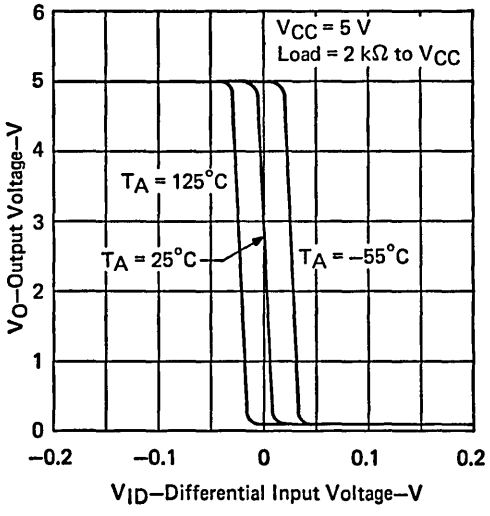

FIGURE 34

OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

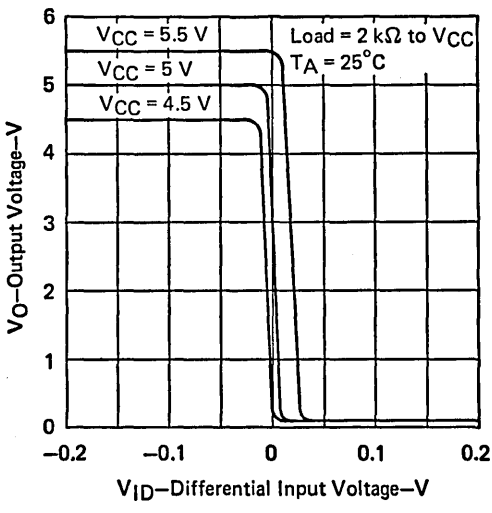

FIGURE 35

OUTPUT VOLTAGE
vs
STROBE INPUT VOLTAGE

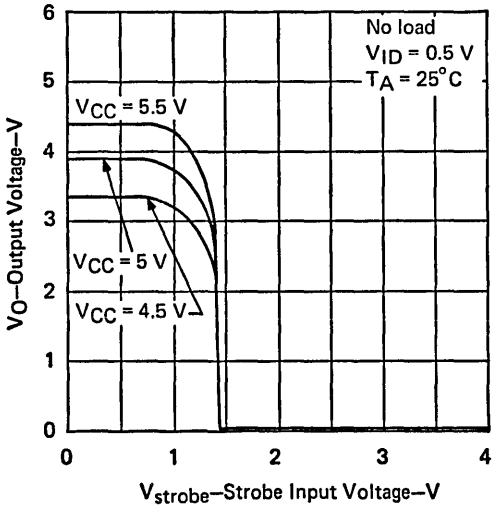

FIGURE 36

OUTPUT VOLTAGE
vs
STROBE INPUT VOLTAGE

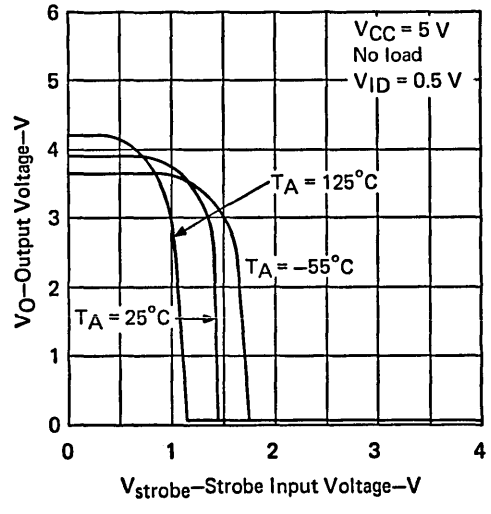

FIGURE 37

†Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75 V and above 5.25 V are applicable to SN55115 circuits only. These parameters were measured with the active pull-up connected to the sink output.

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TYPICAL CHARACTERISTICS†

SUPPLY CURRENT
(BOTH RECEIVERS)
vs
SUPPLY VOLTAGE

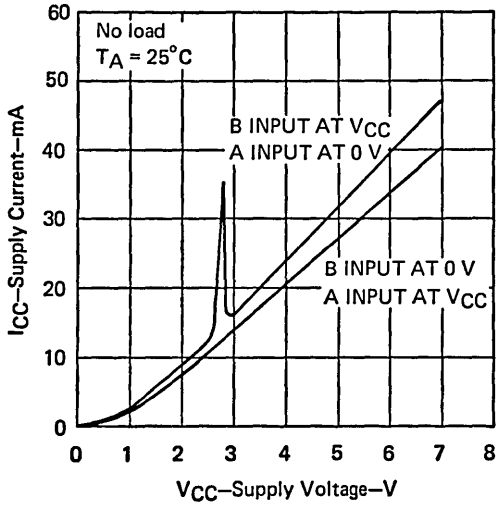


FIGURE 38

SUPPLY CURRENT
(BOTH RECEIVERS)
vs
FREE-AIR TEMPERATURE

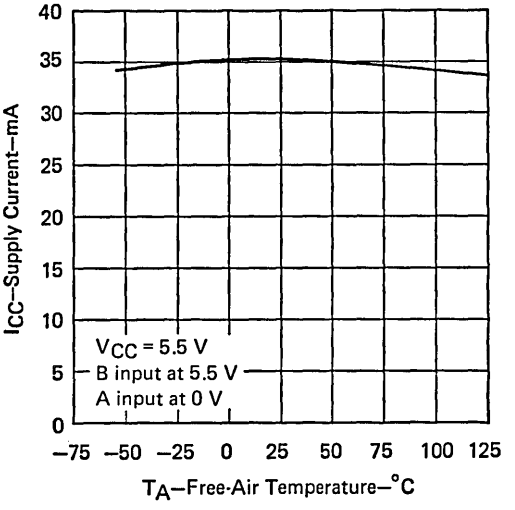


FIGURE 39

PROPAGATION DELAY TIMES
vs
FREE-AIR TEMPERATURE

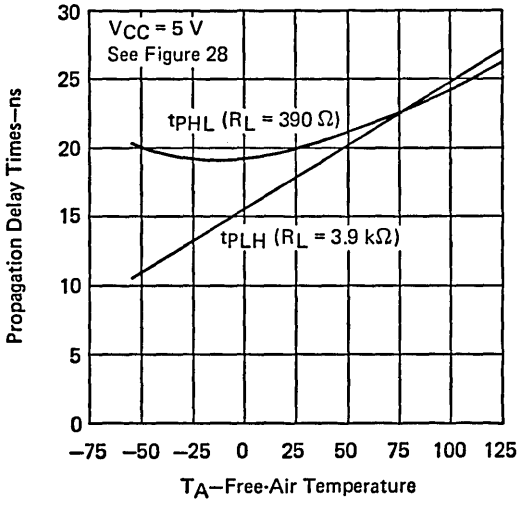


FIGURE 40

MAXIMUM OPERATING FREQUENCY
vs
RESPONSE-TIME-CONTROL CAPACITANCE

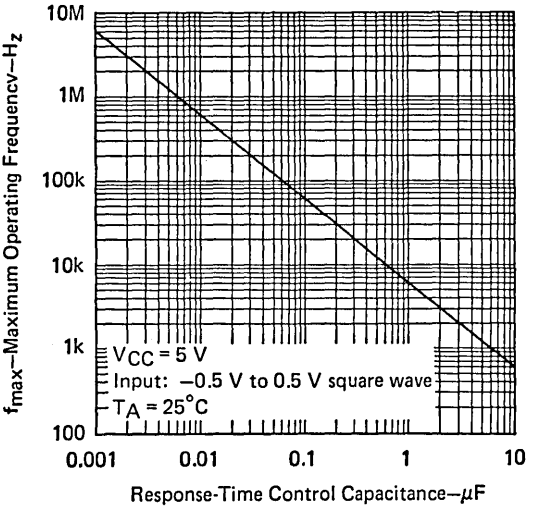
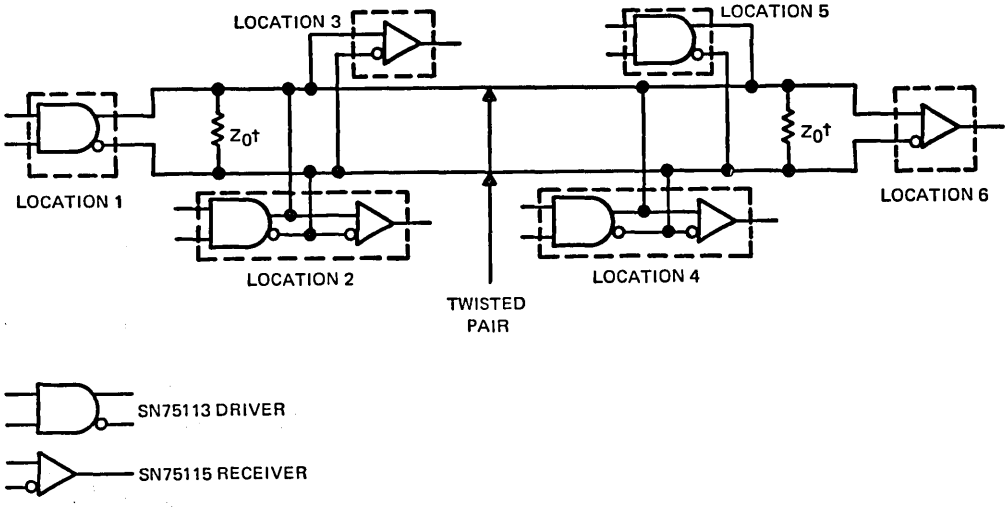


FIGURE 41

†Data for temperatures below 0°C and above 70°C and for supply voltages below 4.75 V and above 5.25 V are applicable to SN55115 circuits only. These parameters were measured with the active pull-up connected to the sink output.

TYPICAL APPLICATION DATA



†A capacitor may be connected in series with Z_0 to reduce power dissipation.

FIGURE 42–BASIC PARTY-LINE OR DATA-BUS DIFFERENTIAL DATA TRANSMISSION

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TYPES SN55116 THRU SN55119, SN75116 THRU SN75119 DIFFERENTIAL LINE TRANSCEIVERS

BULLETIN NO. DL-S 12376, MAY 1976 – REVISED SEPTEMBER 1980

features common to all types

- Single 5-V Supply
- 3-State Driver Output Circuitry
- TTL-Compatible Driver Inputs
- TTL-Compatible Receiver Output
- Differential Line Operation
- Receiver Output Strobe ('116, '117) or Enable ('118, '119)
- Designed for Party-Line (Data-Bus) Applications
- Choice of Ceramic or Plastic Packages

additional features of the SN55116/SN55116

- Independent Driver and Receiver
- Choice of Open-Collector or Totem-Pole Outputs on Both Driver and Receiver
- Dual Data Inputs on Driver
- Optional Line-Termination Resistor in Receiver
- ±15-V Receiver Common-Mode Capability
- Receiver Frequency Response Control

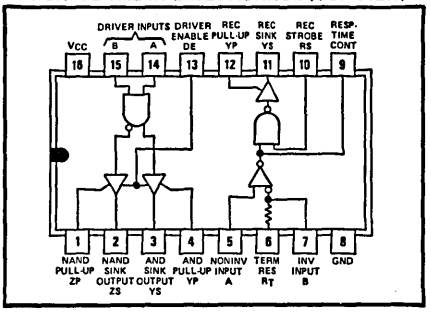
additional features of the SN55117/SN75117

- Driver Output Internally Connected to Receiver Input

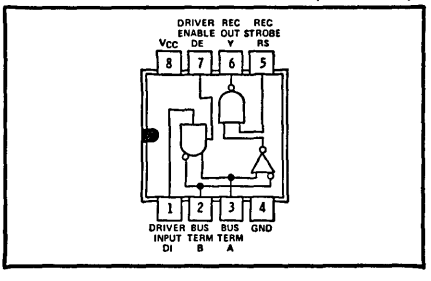
The SN55118/SN75118 is an SN55116/SN75116 with 3-State Receiver Output Circuitry

The SN55119/SN75119 is an SN55117/SN75117 with 3-State Receiver Output Circuitry

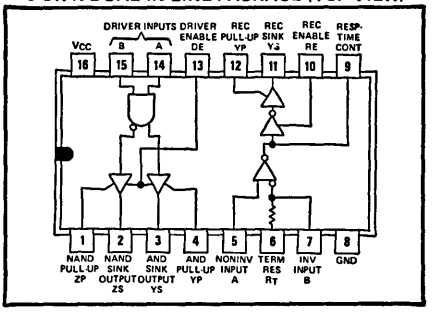
SN55116, SN75116
J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)



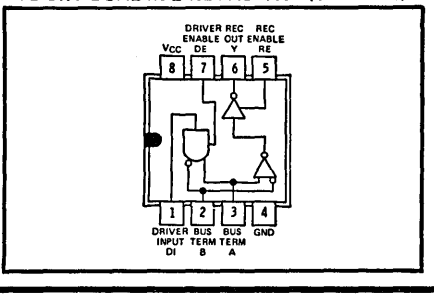
SN55117, SN75117
JG OR P DUAL-IN-LINE PACKAGE (TOP VIEW)



SN55118, SN75118
J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)



SN55119, SN75119
JG OR P DUAL-IN-LINE PACKAGE (TOP VIEW)



description

These integrated circuits are designed for use in interfacing between TTL-type digital systems and differential data transmission lines. They are especially useful for party-line (data-bus) applications. Each of these circuit types combine in one package a three-state differential line driver and a differential-input line receiver, both of which operate from a single 5-volt power supply. The driver inputs and receiver outputs are TTL compatible. The driver employed is similar to the SN55113/SN75113 three-state line driver, and the receiver is similar to the SN55115/SN75115 line receiver.

description (continued)

The '116 and '118 circuits offer all the features of the SN55113/SN75113 driver and the SN55115/SN75115 receiver. The driver performs the dual input AND and NAND functions when enabled, or presents a high impedance to the load when in the disabled state. The driver output stages are similar to the TTL totem-pole outputs, but have the current-sink portion separated from the current-sourcing portion and both are brought out to adjacent package pins. This feature allows the user the option of using the driver in the open-collector output configuration, or, by connecting the adjacent source and sink pins together, of using the driver in the normal totem-pole output configuration.

The receiver portion of the '116 and '118 features a differential-input circuit having a common-mode voltage range of ±15 volts. An internal 130-ohm resistor is also provided, which may optionally be used for terminating the transmission line. A frequency response control pin allows the user to reduce the speed of the receiver or to improve differential noise immunity. The receiver of the '116 also has an output strobe and a split totem-pole output. The receiver of the '118 has an output-enable for the three-state split totem-pole output. The receiver section of either circuit is independent of the driver section except for the V_{CC} and ground pins.

The '117 and '119 circuits provide the basic driver and receiver functions of the '116 and '118, but use a package that is only half as large. The '117 and '119 are intended primarily for party-line or bus-organized systems as the driver outputs are internally connected to the receiver inputs. The driver has a single data input and a single enable input, and the '117 receiver has an output strobe while the '119 receiver has a three-state-output enable. These devices do not, however, provide output connection options, line termination resistors, or receiver frequency response controls.

The SN55116, SN55117, SN55118, and SN55119 are characterized for operation over the full military temperature range of −55°C to 125°C; the SN75116, SN75117, SN75118, and SN75119 are characterized for operation from 0°C to 70°C.

'116, '118
FUNCTION TABLE
OF DRIVER

INPUTS			OUTPUTS	
DE	A	B	Y	Z
L	X	X	Z	Z
H	L	X	L	H
H	X	L	L	H
H	H	H	H	L

'116, '118
FUNCTION TABLE OF RECEIVER

STROBE OR ENABLE	DIFF INPUT	OUTPUT Y	
		'116	'118
L	X	H	Z
H	L	H	H
H	H	L	L

'117, '119
FUNCTION TABLE
OF DRIVER

INPUTS		OUTPUTS	
DI	DE	A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

'117, '119
FUNCTION TABLE OF RECEIVER

INPUTS			OUTPUT Y	
A	B	RS/RE	'117	'119
H	L	H	H	H
L	H	H	L	L
X	X	L	H	Z

H = high level ($V_I \geq V_{IH}$ min or V_{ID} more positive than V_{TH} max)
L = low level ($V_I \leq V_{IL}$ max or V_{ID} more negative than V_{TL} max)
X = irrelevant
Z = high impedance (off)
? = indeterminate

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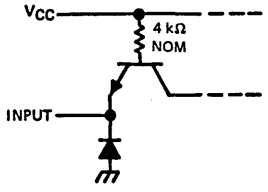
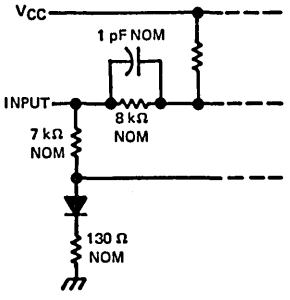
schematics of inputs and outputs

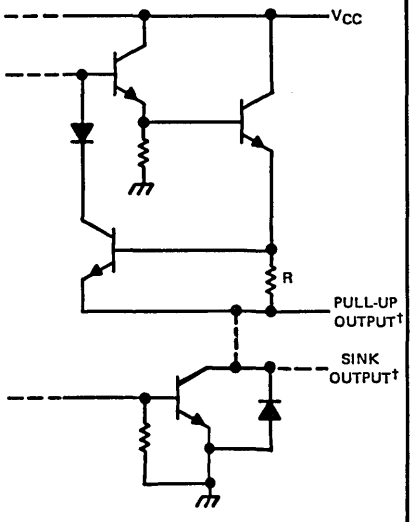
EQUIVALENT OF EACH DRIVER INPUT



EQUIVALENT OF EACH RECEIVER INPUT



TYPICAL OF ALL OUTPUTS



Driver output R = 9 Ω NOM
Receiver output R = 20 Ω NOM
†On '117 and '119, common outputs replace the separate pull-up and sink outputs.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage at data, enable, and strobe inputs	5.5 V
Input voltage at receiver and termination inputs: '116 and '118	±25 V
Input voltage at receiver inputs: '117 and '119	0 to 6 V
Off-state voltage applied to open-collector outputs: '116 and '118	12 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2)	1 W
Operating free-air temperature range: SN55'	−55°C to 125°C
SN75'	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J or JG package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N or P package	260°C

NOTES: 1. Voltage values are with respect to network ground terminal unless otherwise specified.
2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 21. In the J package, SN55116 through SN55119 chips are alloy-mounted; SN75116 through SN75119 chips are glass-mounted.

recommended operating conditions

			SN55'			SN75'			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}			4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}	Drivers				−40			−40	mA
	Receivers				−5			−5	
Low-level output current, I_{OL}	Drivers				40			40	mA
	Receivers				15			15	
Receiver common-mode input voltage, V_{IC}		'116			±15			±15	V
		'117	0		6	0		6	
Operating free-air temperature, T_A			−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

driver section

PARAMETER		TEST CONDITIONS†			'116, '118 MIN	'116, '118 TYP‡	'116, '118 MAX	'117, '119 MIN	'117, '119 TYP‡	'117, '119 MAX	UNIT
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA				−0.9	−1.5		−0.9	−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V	I_{OH} = −10 mA		2.4	3.4		2.4	3.4		V
			I_{OH} = −40 mA		2	3.0		2	3.0		
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 40 mA					0.4			0.4	V
V_{OK}	Output clamp voltage	V_{CC} = MAX, I_O = −40 mA,	DE at 0.8 V				−1.5			−1.5	V
$I_{O(off)}$	Off-state open-collector output current	V_{CC} = MAX, V_O = 12 V	T_A = 25°C			1	10				μA
			T_A = MAX	SN55'			200				
				SN75'			20				
I_{OZ}	Off-state (high-impedance-state) output current	V_{CC} = MAX, V_O = 0 to V_{CC}, T_A = 25°C	DE at 0.8 V,				±10				μA
		V_{CC} = MAX, DE at 0.8 V, T_A = MAX	V_O = 0	SN55'			−150				
			V_O = 0.4 V to V_{CC}	SN55'			±80				
			V_O = 0 to V_{CC}	SN75'			±20				
I_I	Input current at maximum input voltage	Driver or enable input	V_{CC} = MAX, V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.4 V				40			40	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.4 V				−1.6			−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX, V_O = 0,	T_A = 25°C		−40		−120	−40		−120	mA
I_{CC}	Supply current (driver and receiver combined)	V_{CC} = MAX				42	60		42	60	mA

†All parameters with the exception of off-state open-collector output current are measured with the active pull-up connected to the sink output. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at T_A = 25°C and V_{CC} = 5 V.
§Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, C_L = 30 pF, T_A = 25°C

driver section

PARAMETER		TEST CONDITIONS	SN55' MIN	SN55' TYP	SN55' MAX	SN75' MIN	SN75' TYP	SN75' MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 13		14	20		14	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output			12	20		12	30	
t_{PZH}	Output enable time to high level	R_L = 180 Ω, See Figure 14		8	15		8	20	ns
t_{PZL}	Output enable time to low level	R_L = 250 Ω, See Figure 15		17	30		17	40	ns
t_{PHZ}	Output disable time from high level	R_L = 180 Ω, See Figure 14		16	20		16	30	ns
t_{PLZ}	Output disable time from low level	R_L = 250 Ω, See Figure 15		20	35		20	35	ns

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

receiver section

PARAMETER			TEST CONDITIONS†			'116, '118 MIN	'116, '118 TYP‡	'116, '118 MAX	'117, '119 MIN	'117, '119 TYP‡	'117, '119 MAX	UNIT
V_{TH}◆	Differential input high-threshold voltage¶		V_O = 0.4 V, I_{OL} = 15 mA		V_{IC} = 0			0.5			0.5	V
					V_{IC} = MAX			1			1	
V_{TL}◆	Differential input low-threshold voltage¶		V_O = 2.4 V, I_{OH} = −5 mA		V_{IC} = 0	−0.5#			−0.5#			V
					V_{IC} = MAX	−1#			−1#			
V_{ICR}	Common-mode input voltage range¶		V_{CC} = 5 V, V_{ID} = −1 V or 1 V			+15 to −15			+6 to 0			V
V_{IH}	High-level strobe or enable input voltage					2			2			V
V_{IL}	Low-level strobe or enable input voltage							0.8			0.8	V
V_{OH}	High-level output voltage¶		V_{CC} = MIN, I_{OH} = −5 mA	V_{ID} = −0.5 V,	V_{IC} = 0	2.4			2.4			V
				V_{ID} = −1 V,	V_{IC} = MAX	2.4			2.4			
V_{OL}	Low-level output voltage¶		V_{CC} = MIN, I_{OL} = 15 mA	V_{ID} = 0.5 V,	V_{IC} = 0			0.4			0.4	V
				V_{ID} = 1 V,	V_{IC} = MAX			0.4			0.4	
$I_{I(rec)}$	Receiver input current¶		V_{CC} = MAX	V_I = 0 V,	Other input at 0 V	−0.5	−0.9		−0.5	−1		mA
				V_I = 0.4 V,	Other input at 2.4 V	−0.4	−0.7		−0.4	−0.8		
				V_I = 2.4 V	Other input at 0.4 V	0.1	0.3		0.1	0.4		
I_I	Input current at maximum input voltage	Strobe	V_{CC} = MIN, V_{strobe} = 4.5 V	V_{ID} = −0.5 V,	'116, '117			5			5	μA
		Enable	V_{CC} = MAX,	V_I = 5.5 V	'118, '119			1			1	mA
I_{IH}	High-level input current	Enable	V_{CC} = MAX,	V_I = 2.4 V	'118, '119			40			40	μA
I_{IL}	Low-level input current	Strobe	V_{CC} = MAX, V_{strobe} = 0.4 V	V_{ID} = 0.5 V,	'116, '117			−2.4			−2.4	mA
		Enable	V_{CC} = MAX,	V_I = 0.4 V	'118, '119			−1.6			−1.6	
$I_{(RC)}$	Response-time-control current (Pin 9)		V_{CC} = MAX, RC at 0 V	V_{ID} = 0.5 V,	T_A = 25°C	−1.2						mA
$I_{O(off)}$	Off-state open-collector output current		V_{CC} = MAX, V_O = 12 V, V_{ID} = −1 V	T_A = 25°C			1	10				μA
				T_A = MAX	SN55'			200				
					SN75'			20				
I_{OZ}	Off-state (high-impedance state) output current		V_{CC} = MAX, V_O = 0 to V_{CC}, RE at 0.4 V	T_A = 25°C	'118, '119			±10			±10	μA
				T_A = MAX	SN55118			±40				
					SN55119						±40	
					SN75118			±20				
					SN75119						±20	
R_T	Line-terminating resistance		V_{CC} = 5 V		T_A = 25°C	77		167				Ω
I_{OS}	Short-circuit output current§		V_{CC} = MAX, V_{ID} = −0.5 V	V_O = 0,	T_A = 25°C	−15		−80	−15		−80	mA
I_{CC}	Supply current (driver and receiver combined)		V_{CC} = MAX, V_{IC} = 0	V_{ID} = 0.5 V	T_A = 25°C		42	60		42	60	mA

†Unless otherwise noted V_{strobe} = 2.4 V. All parameters with the exception of off-state open-collector output current are measured with the active pull-up connected to the sink output. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C, and V_{IC} = 0.

◆Differential voltages are at the B input terminal with respect to the A input terminal.

¶Measurement of these characteristics on the '117 and '119 requires the driver to be disabled with the driver enable at 0.8 V.

#The algebraic convention, where the less-positive (more-negative) limit is designated as minimum, is used in this data sheet for threshold voltages only.

§Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, C_L = 30 pF, T_A = 25°C

receiver section

PARAMETER			TEST CONDITIONS	SN55' MIN	SN55' TYP	SN55' MAX	SN75' MIN	SN75' TYP	SN75' MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output		R_L = 400 Ω, See Figure 16		20	50		20	75	ns
t_{PHL}	Propagation delay time, high-to-low-level output				17	50		17	75	ns
t_{PZH}	Output enable time to high level	'118	R_L = 480 Ω, See Figure 14		9	15		9	20	ns
t_{PZL}	Output enable time to low level	and	R_L = 250 Ω, See Figure 15		16	25		16	35	ns
t_{PHZ}	Output disable time from high level	'119	R_L = 480 Ω, See Figure 14		12	20		12	30	ns
t_{PLZ}	Output disable time from low level	only	R_L = 250 Ω, See Figure 15		17	25		17	35	ns

TYPICAL CHARACTERISTICS

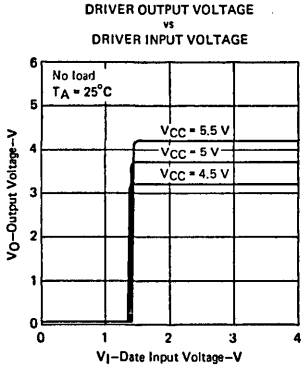

FIGURE 1

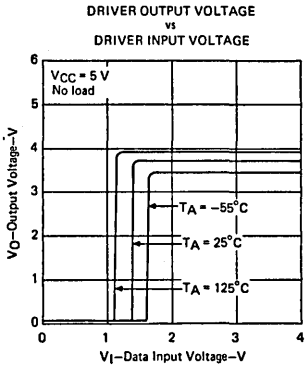

FIGURE 2

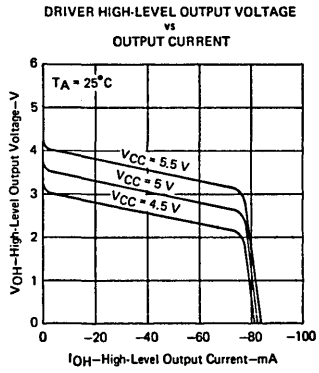

FIGURE 3

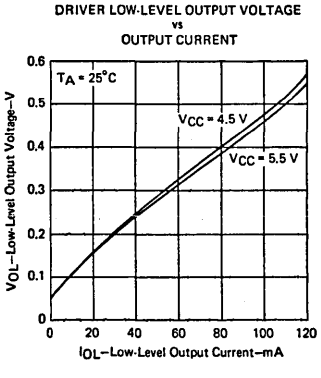

FIGURE 4

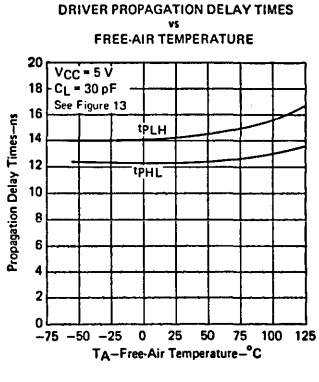

FIGURE 5

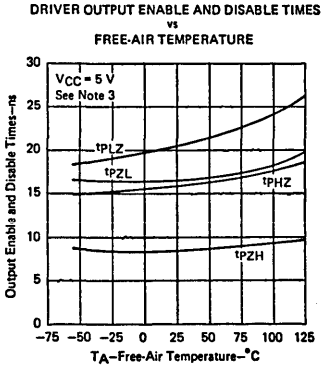

FIGURE 6

NOTE 3: For t_{PZH} and t_{PHZ}: R_L = 180 Ω, see Figure 14. For t_{PZL} and t_{PLZ}: R_L = 250 Ω, see Figure 15.

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TYPICAL CHARACTERISTICS

RECEIVER OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

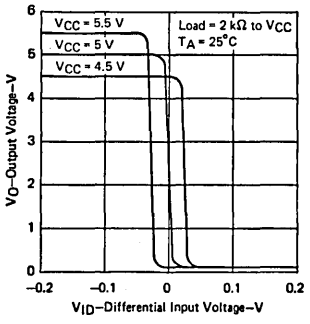


FIGURE 7

RECEIVER OUTPUT VOLTAGE
vs
DIFFERENTIAL INPUT VOLTAGE

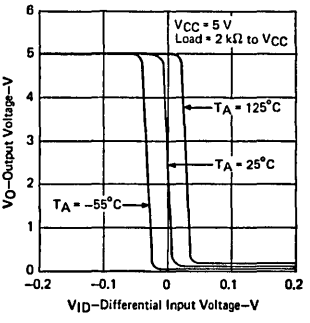


FIGURE 8

RECEIVER PROPAGATION DELAY TIMES
vs
FREE-AIR TEMPERATURE

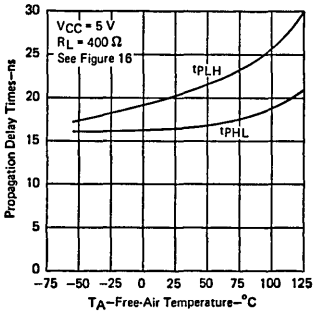


FIGURE 9

RECEIVER OUTPUT ENABLE AND DISABLE TIMES
vs
FREE-AIR TEMPERATURE

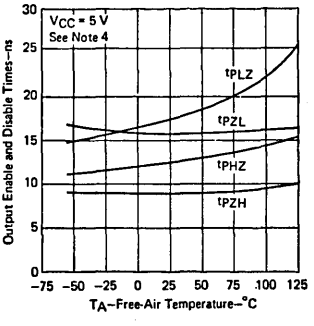


FIGURE 10

SUPPLY CURRENT (DRIVER AND RECEIVER)
vs
SUPPLY VOLTAGE

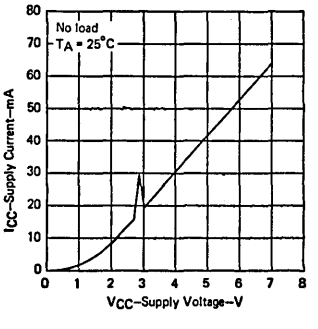


FIGURE 11

SUPPLY CURRENT (DRIVER & RECEIVER)
vs
FREE-AIR TEMPERATURE

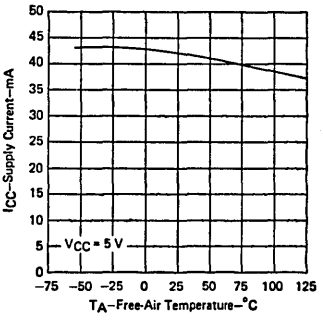
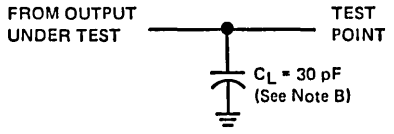


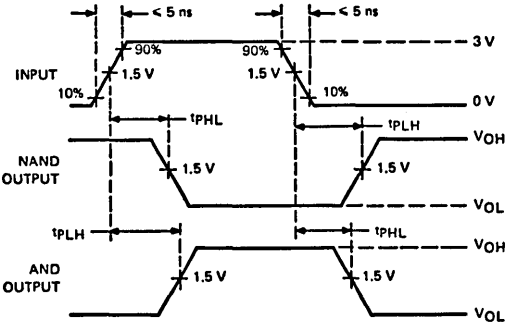
FIGURE 12

NOTE 4: For t_{PZH} and t_{PHZ}: R_L = 480 Ω, see Figure 14. For t_{PZL} and t_{PLZ}: R_L = 250 Ω, see Figure 15.

PARAMETER MEASUREMENT INFORMATION

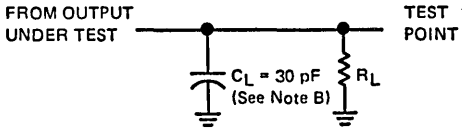


LOAD CIRCUIT

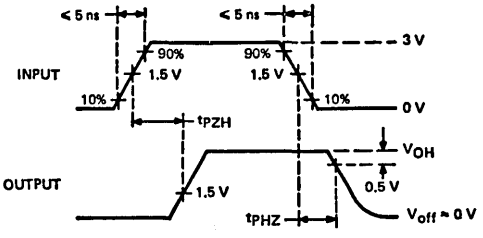


VOLTAGE WAVEFORMS

FIGURE 13–t_{PLH} and t_{PHL} (DRIVERS ONLY)

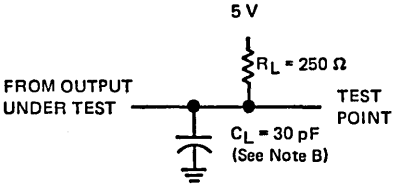


LOAD CIRCUIT

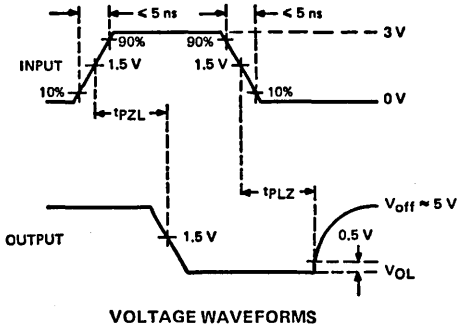


VOLTAGE WAVEFORMS

FIGURE 14–t_{PZH} and t_{PHZ}

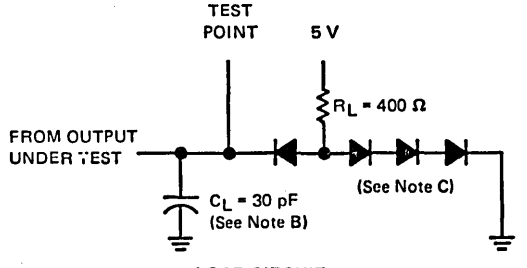


LOAD CIRCUIT

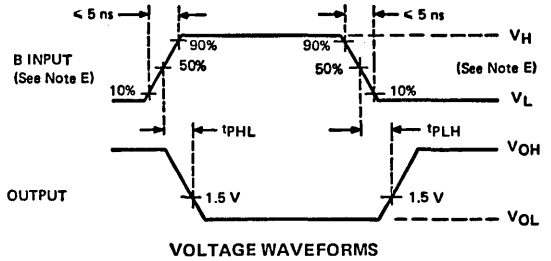


VOLTAGE WAVEFORMS

FIGURE 15–t_{PZL} and t_{PLZ}



LOAD CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 16–t_{PLH} and t_{PHL} (RECEIVERS ONLY)

NOTES: A. Input pulses are supplied by generators having the following characteristics: Z_{out} = 50 Ω, PRR = 500 kHz, t_w = 100 ns.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or equivalent.
D. When testing the '116 and '118 receiver sections, the response-time control and the termination resistor pins are left open.
E. For '116 and '118, V_H = 3 V, V_L = −3 V, the A input is at 0 V.
For '117 and '119, V_H = 3 V, V_L = 0 V, the A input is at 1.5 V.

TEXAS INSTRUMENTS
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TYPES SN55121, SN55122, SN75121, SN75122
DUAL LINE DRIVERS AND TRIPLE LINE RECEIVERS

BULLETIN NO. DL-S 12049, SEPTEMBER 1973 – REVISED APRIL 1974

LINE CIRCUITS

- Designed for Digital Data Transmission over Coaxial Cable, Strip Line, or Twisted Pair
- Designed for Operation with 50-Ω to 500-Ω Transmission Lines
- TTL Compatible with Single 5-V Supply

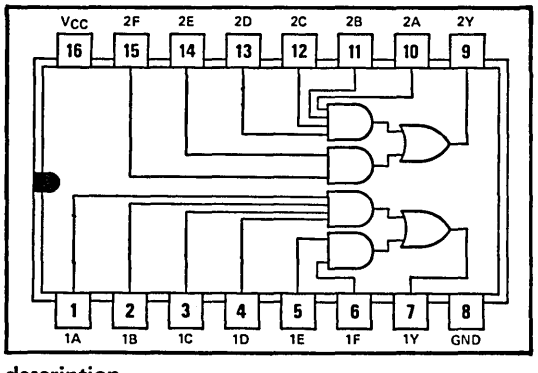
additional features of SN55121, SN75121 line drivers

- Plug-In Replacement for Signetics 8T13
- 2.4-V Output at I_{OH} = –75 mA
- Uncommitted Emitter-Follower Output Structure for Party-Line Operation
- Short-Circuit Protection
- AND-OR Logic Configuration
- High Speed . . .Maximum Propagation Delay Time = 20 ns

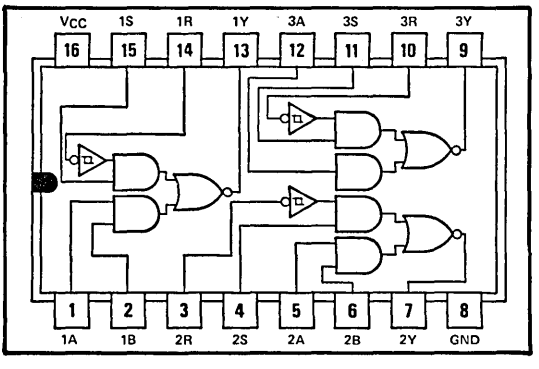
additional features of SN55122, SN75122 line receivers

- Plug-In Replacement for Signetics 8T14
- Built-In Input Threshold Hysteresis
- High Speed . . . Typical Propagation Delay Time = 20 ns
- Independent Channel Strobes
- Input Gating Increases Application Flexibility
- Fanout to 10 Series 54/74 Standard Loads

SN55121, SN75121
J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



SN55122, SN75122
J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



description

The SN55121, SN75121 dual line drivers and the SN55122, SN75122 triple line receivers are designed for digital data transmission over lines having impedances from 50 to 500 ohms. They are also compatible with standard TTL logic and supply voltage levels.

The low-impedance emitter-follower outputs of the SN55121, SN75121 will drive terminated lines such as coaxial cable or twisted pair. Having the outputs uncommitted allows wired-OR logic to be performed in party-line applications. Output short-circuit protection is provided by an internal clamping network which turns on when the output voltage drops below approximately 1.5 volts. All of the inputs are in conventional TTL configuration and the gating can be used during power-up and power-down sequences to ensure that no noise is introduced to the line.

The SN55122, SN75122 have receiver inputs with built-in hysteresis to provide increased noise margin for single-ended systems. The high impedance of this input presents a minimum load to the driver and allows termination of the transmission line in its characteristic impedance to minimize line reflection. An open line will affect the receiver input as would a low-level input voltage and the receiver input can withstand a level of –0.15 volt with power on or off. The other inputs are in TTL configuration. The S input must be high to enable the receiver input. Two of the line receivers have A and B inputs which, if both are high, will hold the output low. The third receiver has only an A input which, if high, will hold the output low.

SN55121, SN75121 FUNCTION TABLE

INPUTS						OUTPUT
A	B	C	D	E	F	Y
H	H	H	H	X	X	H
X	X	X	X	H	H	H
All other input combinations						L

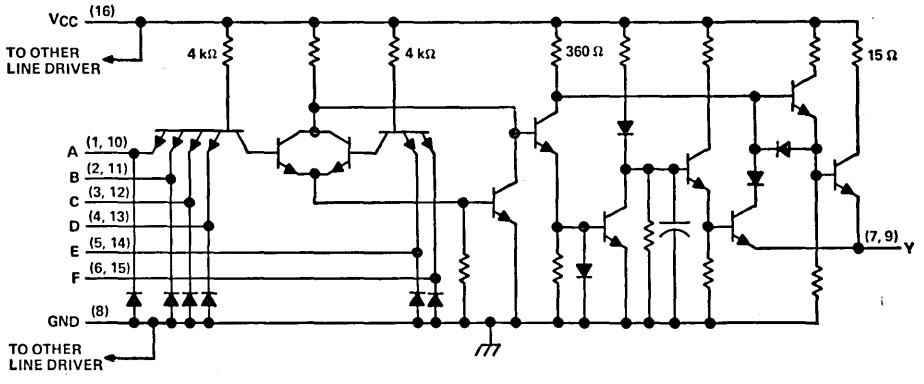
H = high level
L = low level
X = irrelevant

SN55122, SN75122 FUNCTION TABLE

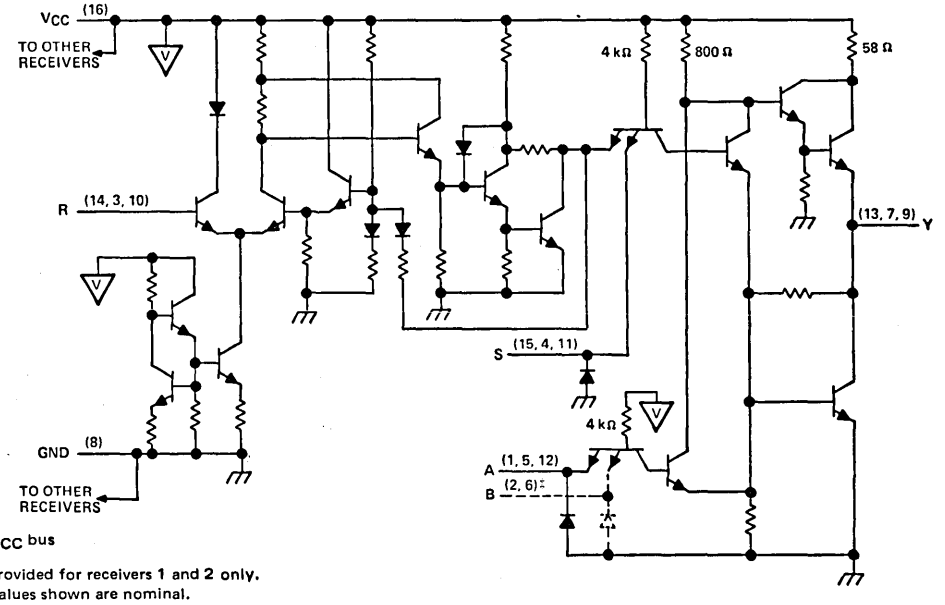
INPUTS				OUTPUT
A	B†	R	S	Y
H	H	X	X	L
X	X	L	H	L
L	X	H	X	H
L	X	X	L	H
X	L	H	X	H
X	L	X	L	H

†B input and last two lines of the function table are applicable to receivers 1 and 2 only.

SN55121, SN75121 schematic (each driver)



SN55122, SN75122 schematic (each receiver)



▽ . . . VCC bus

‡B input is provided for receivers 1 and 2 only.
Resistor values shown are nominal.

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SN55121, SN75121 absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 6 V
Input voltage . . . . . 6 V
Output voltage . . . . . 6 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 1 W
Operating free-air temperature range: SN55121 . . . . . −55°C to 125°C
SN75121 . . . . . 0°C to 75°C
Lead temperature 1/16 inch from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1/16 inch from case for 10 seconds: N package . . . . . 260°C

SN55121, SN75121 recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level output current, I_{OH}			−75	mA
Operating free-air temperature, T_A: SN55121	−55		125	°C
SN75121	0		75	°C

SN55121, SN75121 electrical characteristics over recommended operating free-air temperature range, V_{CC} = 4.75 V to 5.25 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	MAX	UNIT
V_{IH}	High-level input voltage				2		V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	V_{CC} = 5 V,	I_I = −12 mA			−1.5	V
$V_{(BR)I}$	Input breakdown voltage	V_{CC} = 5 V,	I_I = 10 mA		5.5		V
V_{OH}	High-level output voltage	V_{IH} = 2 V,	I_{OH} = −75 mA,	See Note 3	2.4		V
I_{OH}	High-level output current	V_{CC} = 5 V, T_A = 25°C,	V_{IH} = 4.5 V, See Note 3	V_{OH} = 2 V,	−100	−250	mA
I_{OL}	Low-level output current	V_{IL} = 0.8 V,	V_{OL} = 0.4 V,	See Note 3		−800	μA
$I_{O(off)}$	Off-state output current	V_{CC} = 3 V,	V_O = 3 V			500	μA
I_{IH}	High-level input current	V_I = 4.5 V				40	μA
I_{IL}	Low-level input current	V_I = 0.4 V			−0.1	−1.6	mA
I_{OS}	Short-circuit output current‡	V_{CC} = 5 V,	T_A = 25°C			−30	mA
I_{CCH}	Supply current, outputs high	V_{CC} = 5.25 V,	All inputs at 2 V,	Outputs open		28	mA
I_{CCL}	Supply current, outputs low	V_{CC} = 5.25 V,	All inputs at 0.8 V,	Outputs open		60	mA

‡Not more than one output should be shorted at a time.

SN55121, SN75121 switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 37 Ω, C_L = 15 pF, See Figure 1		11	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output			8	20	
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 37 Ω, C_L = 1000 pF, See Figure 1		22	50	ns
t_{PHL}	Propagation delay time, high-to-low-level output			20	50	

NOTES: 1. Voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, refer to the Dissipation Derating Curves in the Thermal Information section, which starts on page 21. In the J package, SN55121 chips are alloy-mounted; SN75121 chips are glass-mounted.
3 The output voltage and current limits are guaranteed for any appropriate combination of high and low inputs specified by the function table for the desired output.

SN55122, SN75122 absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	6 V
Input voltage: R input	6 V
A, B, or S input	5.5 V
Output voltage	6 V
Output current	±100 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 6)	1 W
Operating free-air temperature range: SN55122	−55°C to 125°C
SN75122	0°C to 75°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N package	260°C

SN55122, SN75122 recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level output current, I_{OH}			−500	μA
Low-level output current, I_{OL}			16	mA
Operating free-air temperature, T_A: SN55122	−55		125	°C
SN75122	0		75	°C

SN55122, SN75122 electrical characteristics over recommended operating free-air temperature range, V_{CC} = 4.75 V to 5.25 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage	A,B,R, or S		2			V
V_{IL}	Low-level input voltage	A,B,R, or S				0.8	V
$V_{T+}-V_{T-}$	Hysteresis†	R	V_{CC} = 5 V, T_A = 25°C	0.3	0.6		V
V_{IK}	Input clamp voltage	A,B, or S	V_{CC} = 5 V, I_I = −12 mA			−1.5	V
$V_{(BR)I}$	Input breakdown voltage	A,B, or S	V_{CC} = 5 V, I_I = 10 mA	5.5			V
V_{OH}	High-level output voltage		V_{IH} = 0 V, V_{IL} = 0.8 V, I_{OH} = −500 μA, See Note 3	2.6			V
			$V_{I(A)}$ = 0 V, $V_{I(B)}$ = 0 V, $V_{I(S)}$ = 2 V, $V_{I(R)}$ = 1.45 V (See Note 4), I_{OH} = −500 μA	2.6			
V_{OL}	Low-level output voltage		V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA, See Note 3			0.4	V
			$V_{I(A)}$ = 0 V, $V_{I(B)}$ = 0 V, $V_{I(S)}$ = 2 V, $V_{I(R)}$ = 1.45 V (See Note 5), I_{OL} = 16 mA			0.4	
I_{IH}	High-level input current	A,B, or S	V_I = 4.5 V			40	μA
		R	V_I = 3.8 V			170	
I_{IL}	Low-level input current	A,B, or S	V_I = 0.4 V	−0.1		−1.6	mA
I_{OS}	Short-circuit output current‡		V_{CC} = 5 V, T_A = 25°C	−50		−100	mA
I_{CC}	Supply current		V_{CC} = 5.25 V			72	mA

†Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}. See Figure 4.

‡Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

NOTES: 1. Voltage values are with respect to network ground terminal.

3. The output voltage limits are guaranteed for any appropriate combination of high and low inputs specified by the function table for the desired output.
4. Receiver input was at a high level immediately before being reduced to 1.45 V.
5. Receiver input was at a low level immediately before being raised to 1.45 V.
6. For operation above 25°C free-air temperature, refer to the Dissipation Derating Curves in the Thermal Information section, which starts on page 21. In the J package, SN55122 chips are alloy-mounted; SN75122 chips are glass-mounted.

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SN55122, SN75122 switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output from R input	See Figure 2		20	30	ns
t_{PHL} Propagation delay time, high-to-low-level output from R input			20	30	

PARAMETER MEASUREMENT INFORMATION

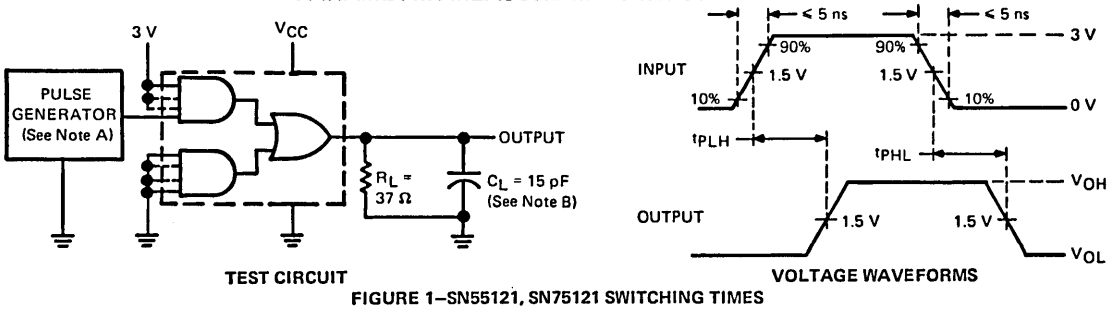


FIGURE 1–SN55121, SN75121 SWITCHING TIMES

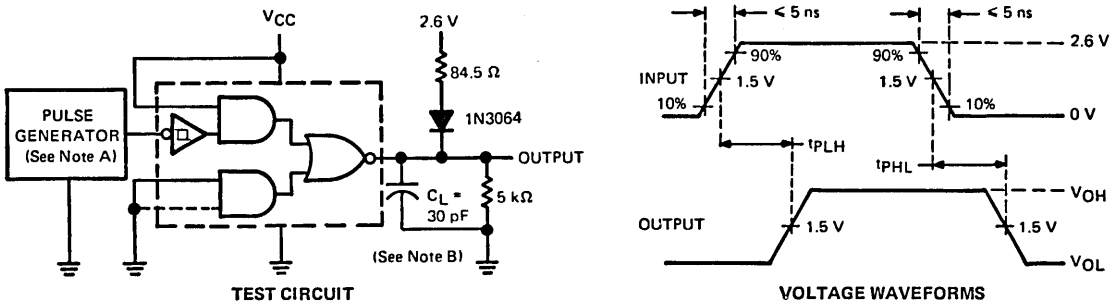


FIGURE 2–SN55122, SN75122 SWITCHING TIMES

NOTES: A. The pulse generators have the following characteristics: $Z_{out} \approx 50\ \Omega$, t_w = 200 ns, duty cycle = 50%.
B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

SN55121, SN75121

OUTPUT CURRENT vs OUTPUT VOLTAGE

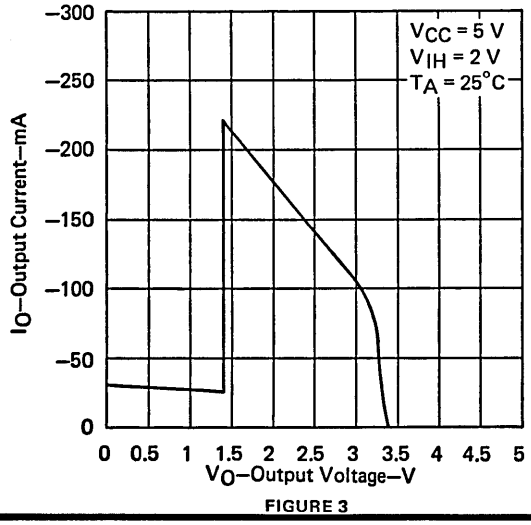


FIGURE 3

SN55122, SN75122

OUTPUT VOLTAGE vs INPUT VOLTAGE

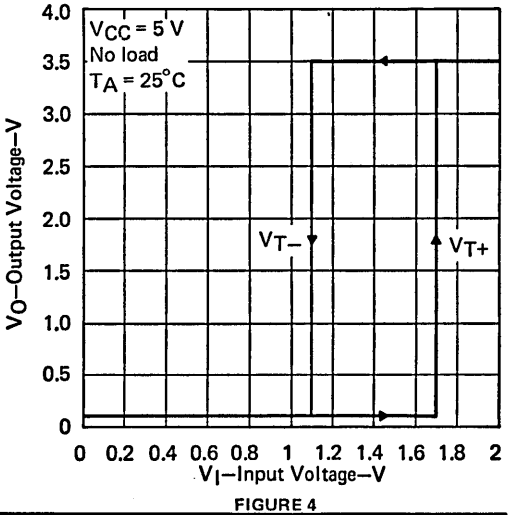


FIGURE 4

TYPICAL APPLICATION DATA

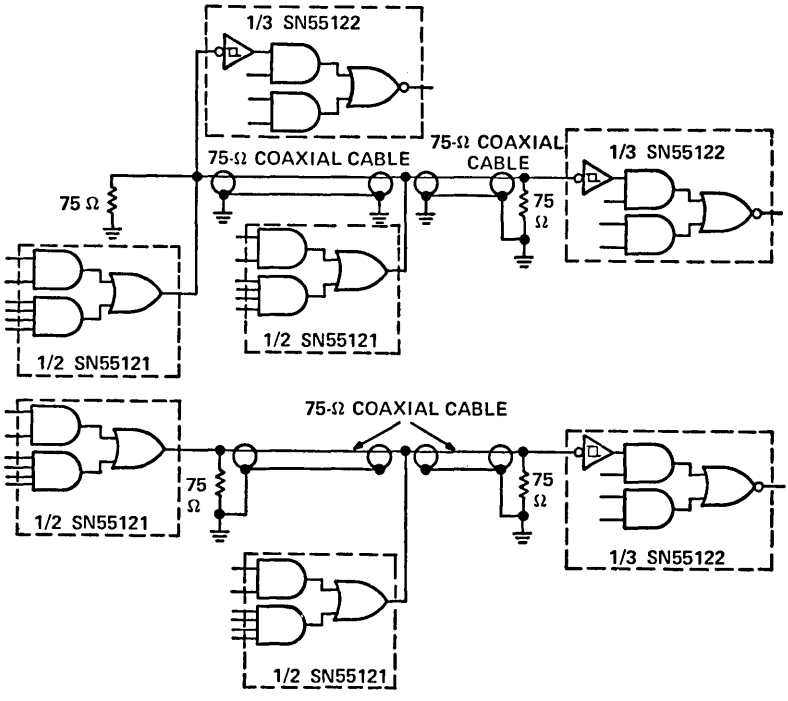
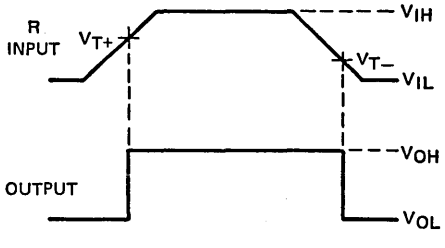


FIGURE 5–SINGLE-ENDED PARTY LINE CIRCUITS



The high gain and built-in hysteresis of the SN55122 and SN75122 line receivers enable them to be used as Schmitt triggers in squaring up pulses.

FIGURE 6–PULSE SQUARING

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TYPES SN75123, SN75124

DUAL LINE DRIVER AND TRIPLE LINE RECEIVER

BULLETIN NO. DL-S 12043, SEPTEMBER 1973—REVISED APRIL 1974

LINE CIRCUITS

- Meet IBM System 360 Input/Output Interface Specifications
- Operate from Single 5-V Supply
- TTL Compatible

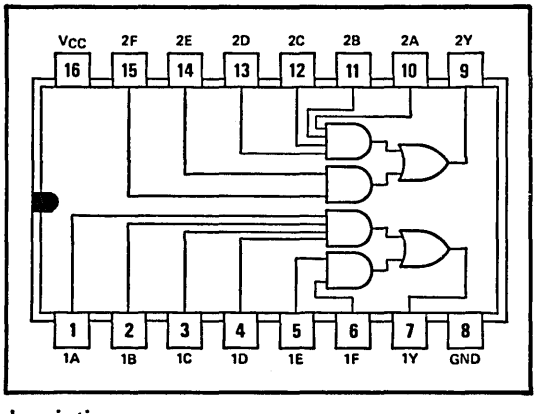
additional features of SN75123 line driver

- Plug-In Replacement for Signetics 8T23
- 3.11-V Output at I_{OH} = −59.3 mA
- Uncommitted Emitter-Follower Output Structure for Party-Line Operation
- Short-Circuit Protection
- AND-OR Logic Configuration

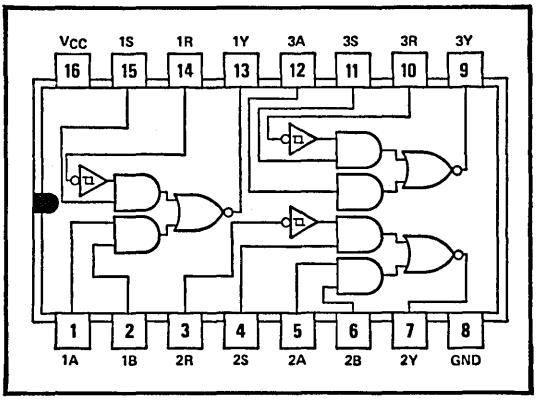
additional features of SN75124 line receiver

- Plug-In Replacement for Signetics 8T24
- Built-In Input Threshold Hysteresis
- High Speed . . . Typical Propagation Delay Time = 20 ns
- Independent Channel Strobes
- Input Gating Increases Application Flexibility

SN75123
J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



SN75124
J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



description

The SN75123 dual line driver and the SN75124 triple line receiver are both specifically designed to meet the input/output interface specifications for IBM System 360. They are also compatible with standard TTL logic and supply voltage levels.

The low-impedance emitter-follower outputs of the SN75123 will drive terminated lines such as coaxial cable or twisted pair. Having the outputs uncommitted allows wired-OR logic to be performed in party-line applications. Output short-circuit protection is provided by an internal clamping network which turns on when the output voltage drops below approximately 1.5 volts. All of the inputs are in conventional TTL configuration and the gating can be used during power-up and power-down sequences to ensure that no noise is introduced to the line.

The SN75124 has receiver inputs with built-in hysteresis to provide increased noise margin for single-ended systems. An open line will affect the receiver input as would a low-level input voltage and the receiver input can withstand a level of −0.15 volt with power on or off. The other inputs are in TTL configuration. The S input must be high to enable the receiver input. Two of the line receivers have A and B inputs which, if both are high, will hold the output low. The third receiver has only an A input which, if high, will hold the output low.

SN75123 FUNCTION TABLE

INPUTS						OUTPUT
A	B	C	D	E	F	Y
H	H	H	H	X	X	H
X	X	X	X	H	H	H
All other input combinations						L

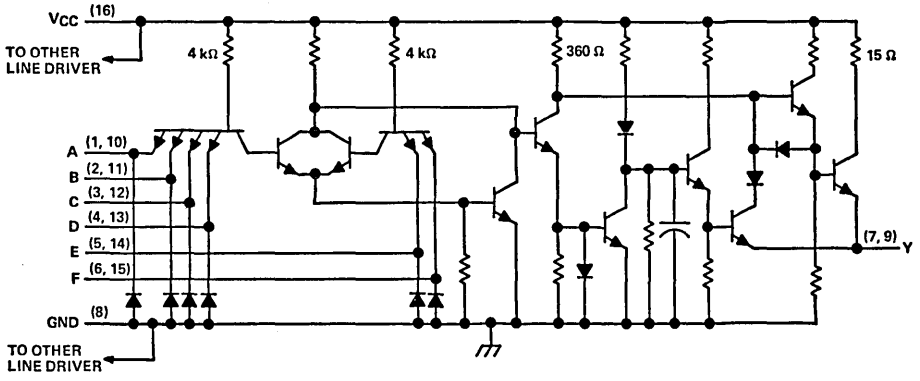
H = high level
L = low level
X = irrelevant

SN75124 FUNCTION TABLE

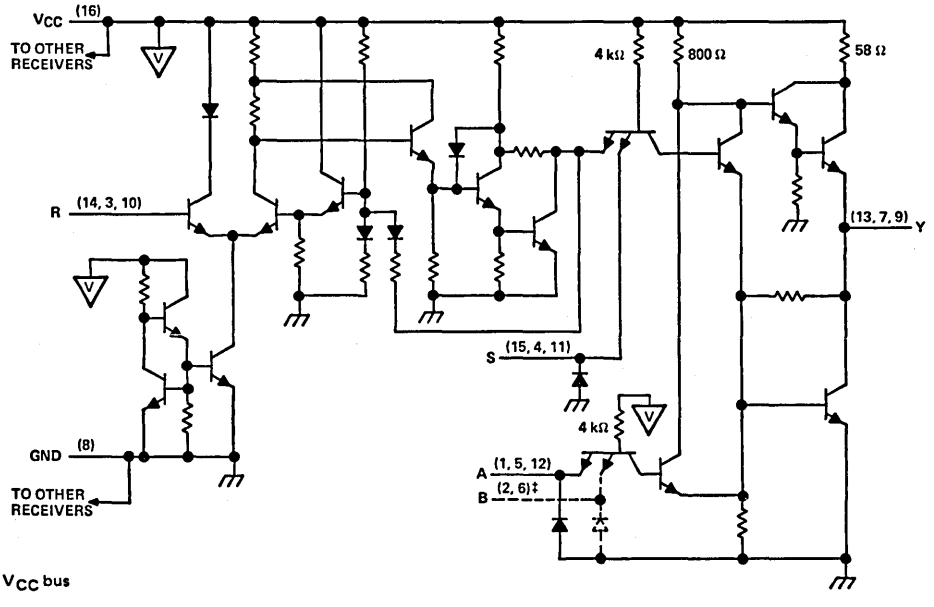
INPUTS				OUTPUT
A	B†	R	S	Y
H	H	X	X	L
X	X	L	H	L
L	X	H	X	H
L	X	X	L	H
X	L	H	X	H
X	L	X	L	H

†B input and last two lines of the function table are applicable to receivers 1 and 2 only.

SN75123 schematic (each driver)



SN75124 schematic (each receiver)



▽ . . . V_{CC} bus

‡B input is provided on receivers 1 and 2 only
Resistor values shown are nominal

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SN75123 absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Output voltage	7 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2)	1 W
Operating free-air temperature range	0°C to 75°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N package	260°C

SN75123 recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level output current, I_{OH}			−100	mA
Operating free-air temperature, T_A	0		75	°C

SN75123 electrical characteristics, V_{CC} = 4.75 V to 5.25 V, T_A = 0°C to 75°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage	V_{CC} = 5 V,	I_I = −12 mA				−1.5	V
$V_{(BR)I}$	Input breakdown voltage	V_{CC} = 5 V,	I_I = 10 mA		5.5			V
V_{OH}	High-level output voltage	V_{CC} = 5 V,	V_{IH} = 2 V,	T_A = 25°C	3.11			V
		I_{OH} = −59.3 mA,	See Note 3	T_A = 0°C to 75°C	2.9			
I_{OH}	High-level output current	V_{CC} = 5 V, T_A = 25°C,	V_{IH} = 4.5 V, See Note 3	V_{OH} = 2 V,	−100		−250	mA
V_{OL}	Low-level output voltage	V_{IL} = 0.8 V,	I_{OL} = −240 μA, See Note 3				0.15	V
$I_{O(off)}$	Off-state output current	V_{CC} = 0,	V_O = 3 V				40	μA
I_{IH}	High-level input current	V_I = 4.5 V					40	μA
I_{IL}	Low-level input current	V_I = 0.4 V			−0.1		−1.6	mA
I_{OS}	Short-circuit output current ‡	V_{CC} = 5 V,	T_A = 25°C				−30	mA
I_{CCH}	Supply current, outputs high	V_{CC} = 5.25 V, Outputs open	All inputs at 2 V,				28	mA
I_{CCL}	Supply current, outputs low	V_{CC} = 5.25 V, Outputs open	All inputs at 0.8 V,				60	mA

‡ Not more than one output should be shorted at a time.

SN75123 switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 50 Ω, C_L = 15 pF, See Figure 1		12	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output			12	20	
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 50 Ω, C_L = 100 pF, See Figure 1		20	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output			15	25	

NOTES: 1. Voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, refer to the Dissipation Derating Curves in the Thermal Information section, which starts on page 21. In the J package, SN75123 chips are glass-mounted.
3. The output voltage and current limits are guaranteed for any appropriate combination of high and low inputs specified by the function table for the desired output.

SN75124 absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage: R input with V_{CC} applied	7 V
R input with V_{CC} not applied	6 V
A, B, or S input	5.5 V
Output voltage	7 V
Output current	±100 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 4)	1 W
Operating free-air temperature range	0°C to 75°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N package	260°C

SN75124 recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level output current, I_{OH}			−800	μA
Low-level output current, I_{OL}			16	mA
Operating free-air temperature, T_A	0		75	°C

SN75124 electrical characteristics, V_{CC} = 4.75 V to 5.25 V, T_A = 0°C to 75°C (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage	A,B, or S		2			V
		R		1.7			
V_{IL}	Low-level input voltage	A,B, or S				0.8	V
		R				0.7	
$V_{T+}-V_{T-}$	Hysteresis†	R	V_{CC} = 5 V, T_A = 25°C	0.2	0.4		V
V_{IK}	Input clamp voltage	A,B, or S	V_{CC} = 5 V, I_I = −12 mA			−1.5	V
$V_{(BR)I}$	Input breakdown voltage	A,B, or S	V_{CC} = 5 V, I_I = 10 mA	5.5			V
V_{OH}	High-level output voltage		V_{IH} = V_{IH} min, V_{IL} = V_{IL}max, I_{OH} = −800 μA, See Note 3	2.6			V
V_{OL}	Low-level output voltage		V_{IH} = V_{IH} min, V_{IL} = V_{IL}max, I_{OL} = 16 mA, See Note 3			0.4	V
I_I	Input current at maximum input voltage	R	V_I = 7 V			5	mA
			V_I = 6 V, V_{CC} = 0			5	
I_{IH}	High-level input current	A,B, or S	V_I = 4.5 V			40	μA
		R	V_I = 3.11 V			170	
I_{IL}	Low-level input current	A,B, or S	V_I = 0.4 V	−0.1		−1.6	mA
I_{OS}	Short-circuit output current‡		V_{CC} = 5 V, T_A = 25°C	−50		−100	mA
I_{CC}	Supply current		V_{CC} = 5.25 V			72	mA

†Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}. See Figure 4.
‡Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

SN75124 switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output from R input	See Figure 2		20	30	ns
t_{PHL} Propagation delay time, high-to-low-level output from R input			20	30	

NOTES: 1. Voltage values are with respect to network ground terminal.
3. The output voltage and current limits are guaranteed for any appropriate combination of high and low inputs specified by the function table for the desired output.
4. For operation above 25°C free-air temperature, refer to the Dissipation Derating Curves in the Thermal Information section, which starts on page 21. In the J package, SN75124 chips are glass-mounted

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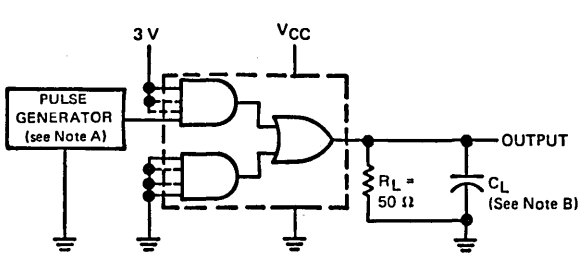
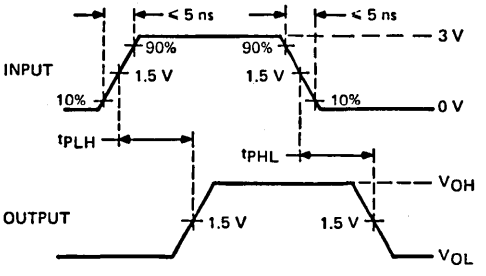
PARAMETER MEASUREMENT INFORMATION

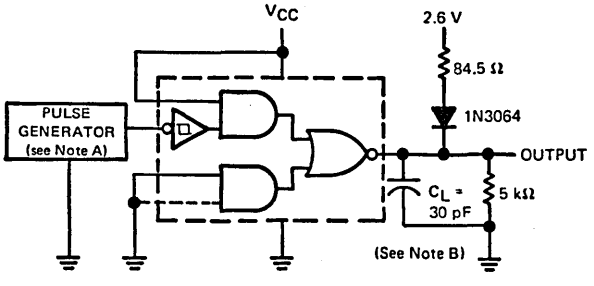


TEST CIRCUIT

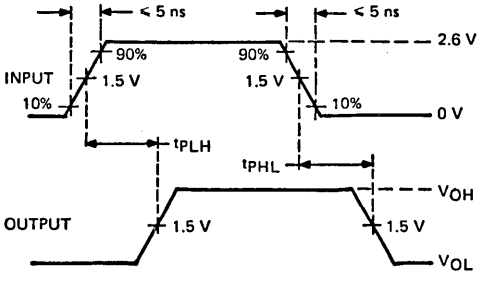


VOLTAGE WAVEFORMS

FIGURE 1–SN75123 SWITCHING TIMES



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 2–SN75124 SWITCHING TIMES

NOTES: A. The pulse generator has the following characteristics: $Z_{out} \approx 50\ \Omega$; $t_w = 200$ ns, duty cycle = 50%.
B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

SN75123
OUTPUT CURRENT
vs
OUTPUT VOLTAGE

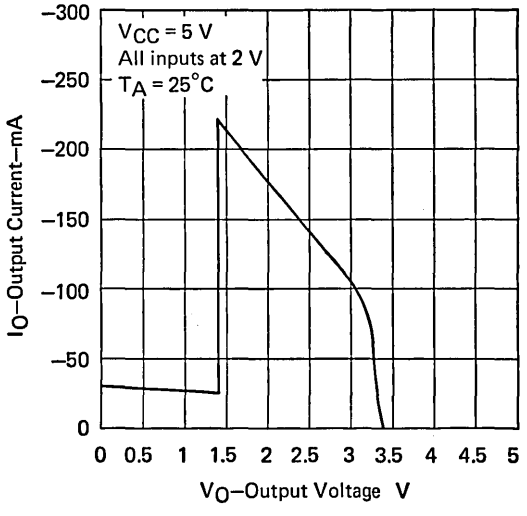


FIGURE 3

SN75124
OUTPUT VOLTAGE
vs
RECEIVER INPUT VOLTAGE

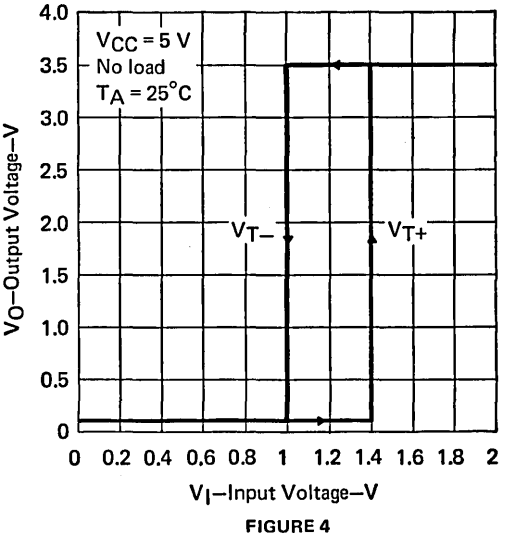


FIGURE 4

TYPICAL APPLICATION DATA

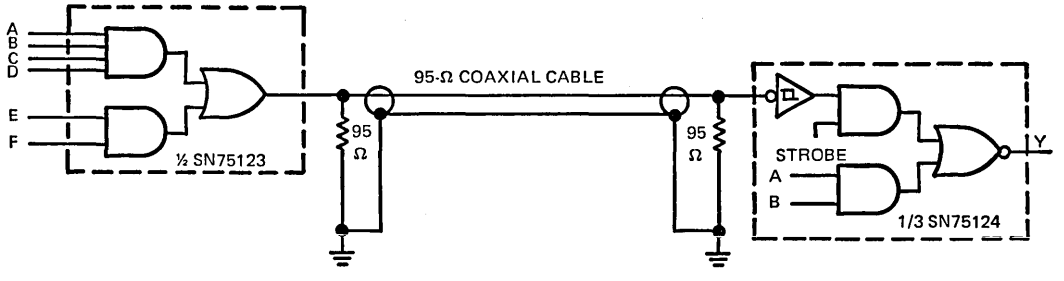


FIGURE 5–UNBALANCED LINE COMMUNICATION USING '123 AND '124

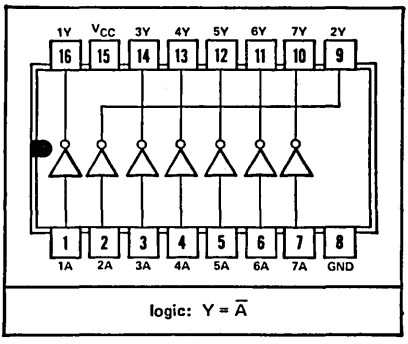
TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

TYPES SN75125, SN75127
SEVEN-CHANNEL LINE RECEIVERS

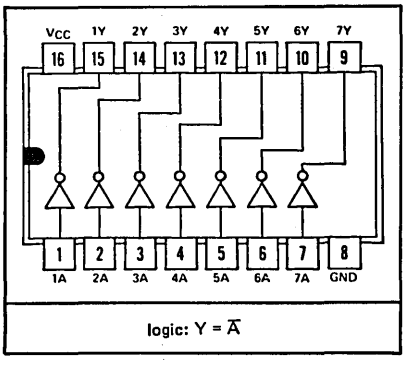
BULLETIN NO. DL-S 12457, JANUARY 1977 – REVISED SEPTEMBER 1980

- Meets IBM 360/370 I/O Specification
- Input Resistance . . . 7 kΩ to 20 kΩ
- Output Compatible with DTL or TTL
- Schottky-Clamped Transistors†
- Operates from Single 5-V Supply
- High Speed . . . Low Propagation Delay
- Ratio Specification for Propagation Delay Time, Low-to-High/High-to-Low
- Seven Channels in one 16-Pin Package
- Standard V_{CC} and Ground Positioning on SN75127

SN75125
J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



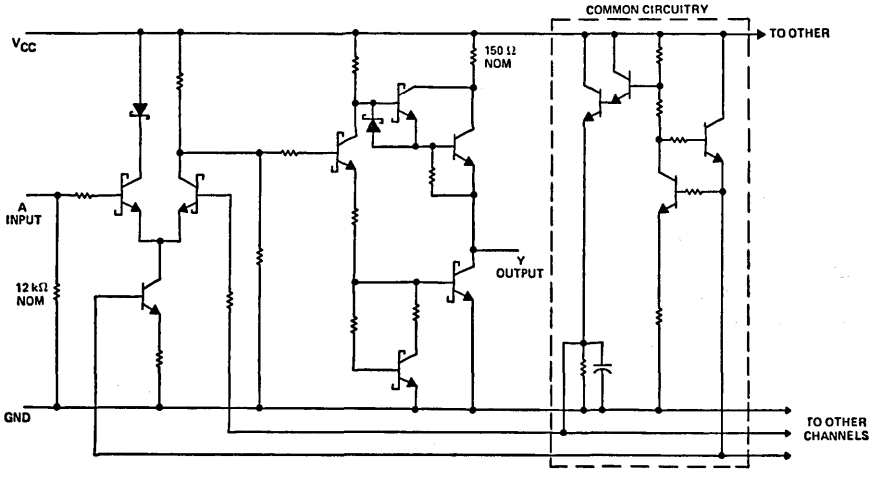
SN75127
J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

The SN75125 and SN75127 are monolithic seven-channel line receivers designed to satisfy the requirements of the IBM System 360/370 input/output interface specifications. Special low-power design and Schottky clamped transistors allow for low supply-current requirements while maintaining fast switching speeds and high-current TTL outputs. The SN75125 and SN75127 are characterized for operation from 0°C to 70°C.

schematic (each receiver)



†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U. S. Patent Number 3,463,975.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage range: SN75125 . . . . . −0.15 V to 7 V
SN75127 . . . . . −2 V to 7 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 800 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1/16 inch from case for 10 seconds: N package . . . . . 260°C

NOTES: 1. All voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information Section, which starts on page 21. In the J package, SN75125 and SN7512' chips are glass-mounted.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	V
High-level output current, I_{OH}			−0.4	mA
Low-level output current, I_{OL}			16	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage		1.7			V
V_{IL}	Low-level input voltage				0.7	V
V_{OH}	High-level output voltage	V_{CC} = 4.5 V, V_{IL} = 0.7 V, I_{OH} = −0.4 mA	2.4	3.1		V
V_{OL}	Low-level output voltage	V_{CC} = 4.5 V, V_{IH} = 1.7 V, I_{OL} = 16 mA		0.4	0.5	V
I_{IH}	High-level input current	V_{CC} = 5.5 V, V_I = 3.11 V		0.3	0.42	mA
I_{IL}	Low-level input current	V_{CC} = 5.5 V, V_I = 0.15 V			30	μA
I_{OS}	Short-circuit output current‡	V_{CC} = 5.5 V, V_O = 0	−18		−60	mA
r_I	Input resistance	V_{CC} = 4.5 V, 0 V, or open, ΔV_I = 0.15 V to 4.15 V	7		20	kΩ
I_{CC}	Supply current	V_{CC} = 5.5 V, I_{OH} = −0.4 mA, All inputs at 0.7 V		15	25	mA
		V_{CC} = 5.5 V, I_{OL} = 16 mA, All inputs at 4 V		28	47	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 400 Ω, C_L = 50 pF, See Figure 1	7	14	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output		10	18	30	ns
$\frac{t_{PLH}}{t_{PHL}}$	Ratio of propagation delay times		0.5	0.8	1.3	ns
t_{TLH}	Transition time, low-to-high-level output		1	7	12	ns
t_{THL}	Transition time, high-to-low-level output		1	3	12	ns

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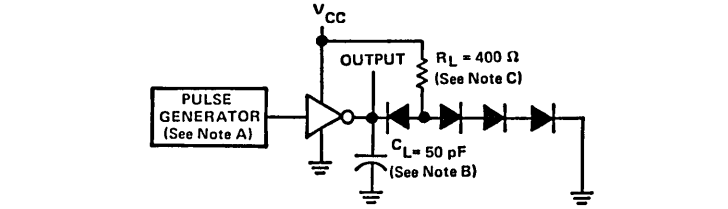
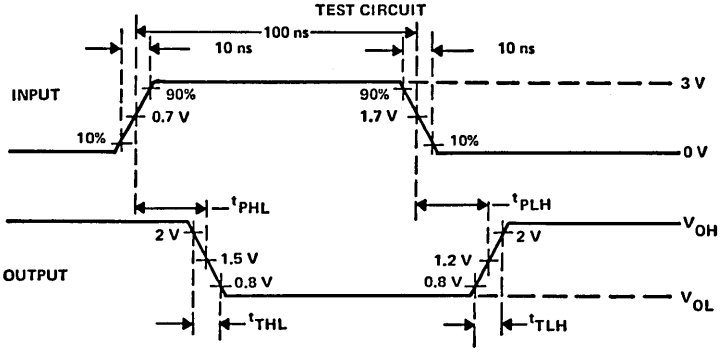
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 1

NOTES: A. The pulse generator has the following characteristics: $Z_{out} \approx 50\ \Omega$, PRR = 5 MHz.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or equivalent.

TYPICAL CHARACTERISTICS

VOLTAGE TRANSFER CHARACTERISTICS

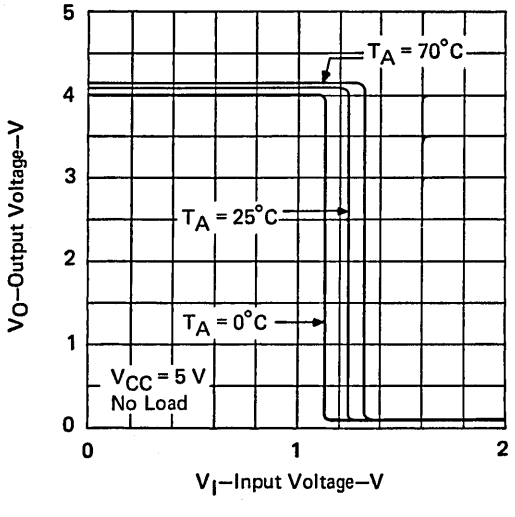


FIGURE 2

VOLTAGE TRANSFER CHARACTERISTICS

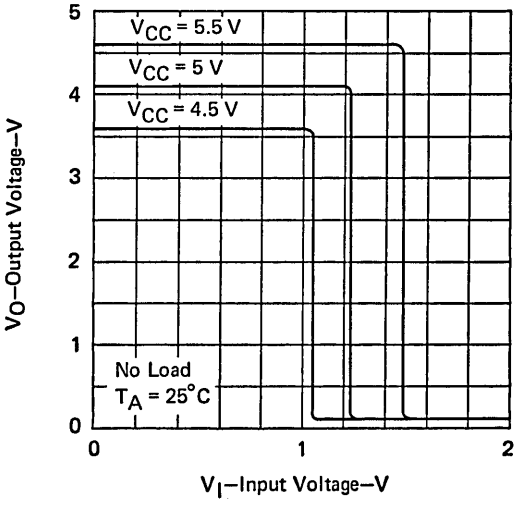


FIGURE 3

TYPICAL CHARACTERISTICS

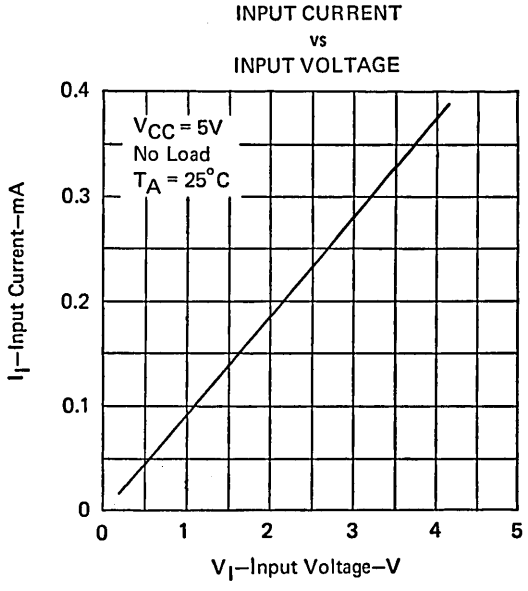


FIGURE 4

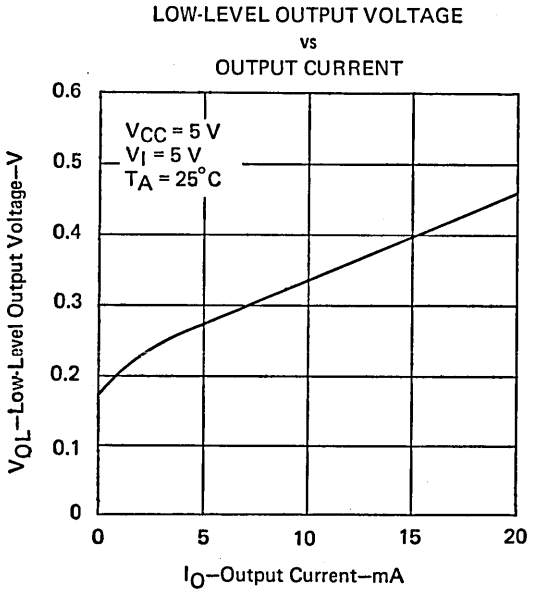


FIGURE 5

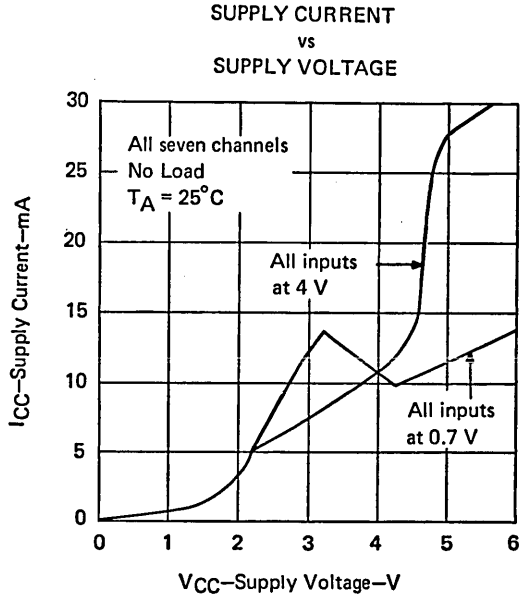


FIGURE 6

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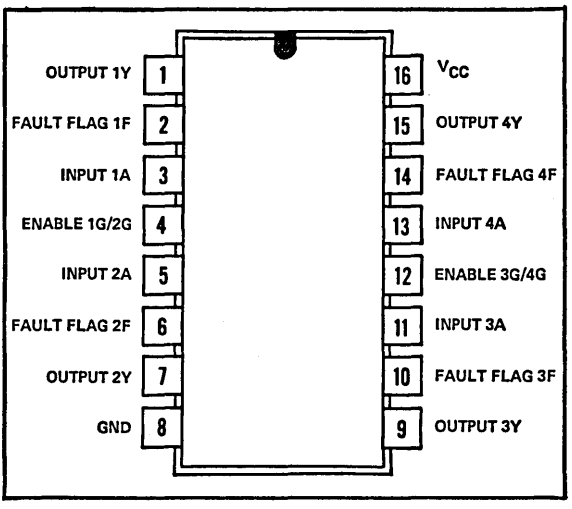
TYPE SN75126
QUADRUPLE LINE DRIVER

OCTOBER 1980

- Meets IBM 360/370 I/O Interface Specification GA22-6974-3 (Also See SN75130)
- Output Voltage of 3.11 V Min at I_{OH} = −60 mA
- Overload Protection with Foldback Current Limiting
- High-Speed, Low-Power Schottky Circuitry
- Functionally Interchangeable with MC 3481

J OR N PACKAGE
(TOP VIEW)

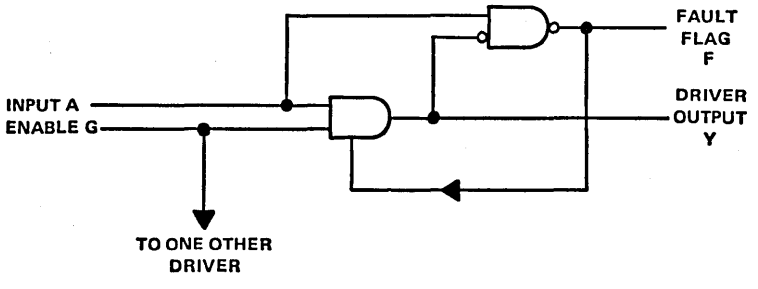


description

The SN75126 quadruple line driver is designed to meet the IBM 360/370 I/O specifications GA22-6974-3. The output voltage is 3.11 volts minimum (at I_{OH} = −60 milliamperes) over the recommended ranges of supply voltage (4.5 volts to 5.5 volts) and temperature (0°C to 70°C). This device is compatible with standard TTL logic and supply voltages. Fabrication techniques employ low-power-Schottky technology to achieve fast switching and low power dissipation. The data bus will not be disturbed during power up and power down. Fault flag circuitry is designed to sense a line short on any Y output line, output a logic low level, and reduce the output current to a safe level.

The SN75126 is designed for use with the SN75125 or SN75127 seven-channel receivers, or the SN75128 or SN75129 eight-channel receivers.

functional block diagram (one of four drivers, positive logic)

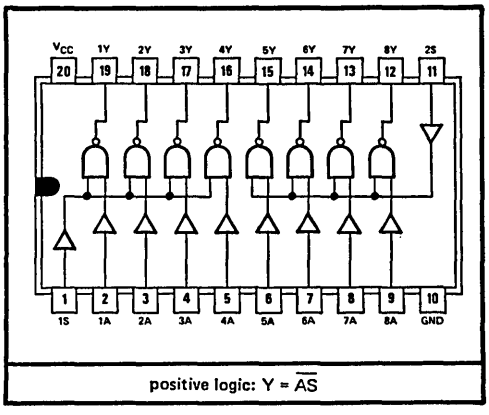


TYPES SN75128, SN75129
EIGHT-CHANNEL LINE RECEIVERS

BULLETIN NO. DL-S 12569, JANUARY 1977 – REVISED SEPTEMBER 1980

- Meets IBM 360/370 I/O Specification
- Input Resistance . . . . . 7 kΩ to 20 kΩ
- Output Compatible with DTL or TTL
- Schottky-Clamped Transistors†
- Operates from a Single 5-Volt Supply
- High-Speed . . . Low Propagation Delay
- Ratio Specification . . . t_{PLH}/t_{PHL}
- Common Strobe for Each Group of Four Receivers
- SN75128 Strobe . . . Active-High
  SN75129 Strobe . . . Active-Low

SN75128
J OR N DUAL IN-LINE PACKAGE
(TOP VIEW)

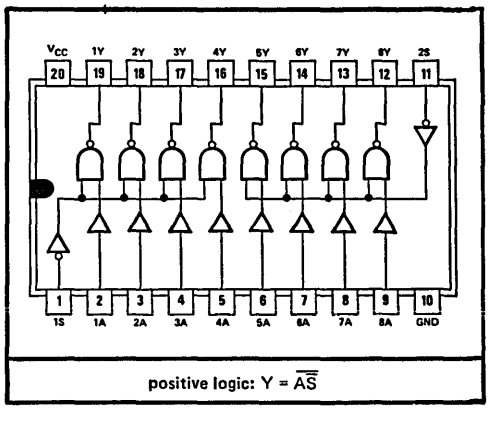


positive logic: $Y = \overline{AS}$

description

The SN75128 and SN75129 are eight-channel line receivers designed to satisfy the requirements of the input-output interface specification for IBM 360/370. Both devices feature common strobes for each group of four receivers. The SN75128 has an active-high strobe; the SN75129 has an active-low strobe. Special low-power design and Schottky-diode-clamped transistors† allow low supply-current requirements while maintaining fast switching speeds and high-current TTL outputs. The SN75128 and SN75129 are characterized for operation from 0°C to 70°C.

SN75129
J OR N DUAL IN-LINE PACKAGE
(TOP VIEW)



positive logic: $Y = \overline{AS}$

† Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments, U.S. Patent Number 3,463,975.

TEXAS INSTRUMENTS
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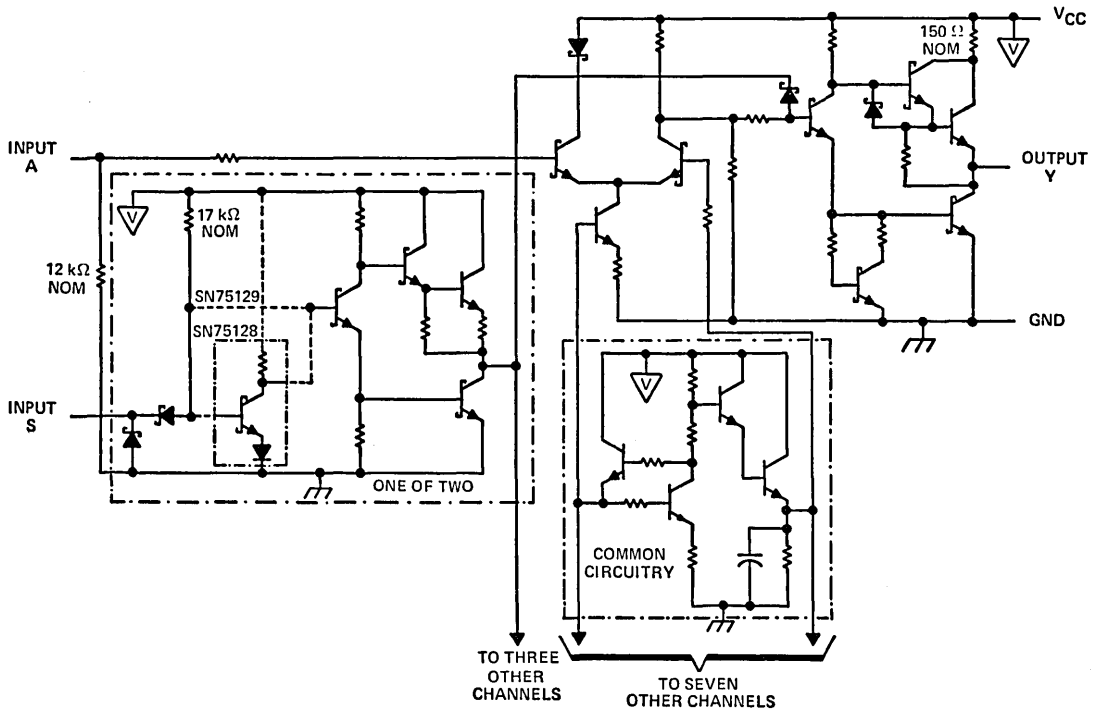
schematic (each receiver)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
A input voltage range	−0.15 V to 7 V
Strobe input voltage	7 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2)	800 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N package	260°C

NOTES: 1. All voltage values are with respect to network ground terminal.

2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 18. In the J package, SN75128 and SN75129 chips are glass-mounted.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	V
High-level output current, I_{OH}			−0.4	mA
Low-level output current, I_{OL}			16	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

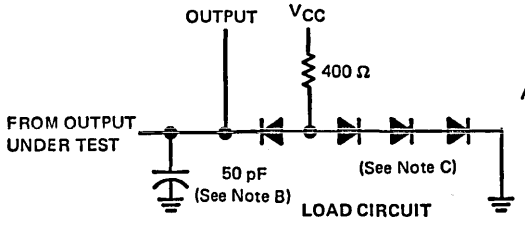
PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage	A		1.7			V
		S		2			
V_{IL}	Low-level input voltage	A				0.7	V
		S				0.7	
V_{OH}	High-level output voltage		V_{CC} = 4.5 V, V_{IL} = 0.7 V, I_{OH} = −0.4 mA	2.4	3.1		V
V_{OL}	Low-level output voltage		V_{CC} = 4.5 V, V_{IH} = 1.7 V, I_{OL} = 16 mA		0.4	0.5	V
V_{IK}	Input clamp voltage	S	V_{CC} = 4.5 V, I_I = −18 mA			−1.5	V
I_{IH}	High-level input current	A	V_{CC} = 5.5 V, V_I = 3.11 V		0.3	0.42	mA
		S	V_{CC} = 5.5 V, V_I = 2.7 V			20	μA
I_{IL}	Low-level input current	A	V_{CC} = 5.5 V, V_I = 0.15 V			30	μA
		S	V_{CC} = 5.5 V, V_I = 0.4 V			−0.4	mA
I_{OS}	Short-circuit output current‡		V_{CC} = 5.5 V, V_O = 0	−18		−60	mA
r_I	Input resistance		V_{CC} = 4.5 V, 0 V, or open; ΔV_I = 0.15 V to 4.15 V	7		20	kΩ
I_{CC}	Supply current	SN75128	V_{CC} = 5.5 V, Strobe at 2.4 V, All A inputs at 0.7 V		19	31	mA
		SN75129	V_{CC} = 5.5 V, Strobe at 0.4 V, All A inputs at 0.7 V		19	31	
		SN75128	V_{CC} = 5.5 V, Strobe at 2.4 V, All A inputs at 4 V		32	53	
		SN75129	V_{CC} = 5.5 V, Strobe at 0.4 V, All A inputs at 4 V		32	53	

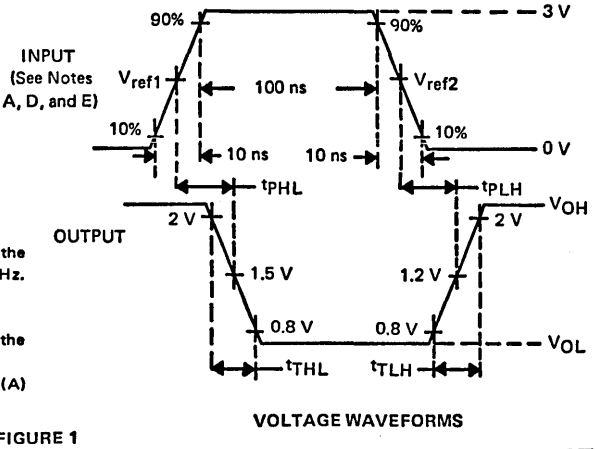
†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		FROM	TEST CONDITIONS	SN75128			SN75129			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	A	R_L = 400 Ω, C_L = 50 pF, See Figure 1	7	14	25	7	14	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output			10	18	30	10	18	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output	S			26	40		20	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output				22	35		16	30	ns
$\frac{t_{PLH}}{t_{PHL}}$	Ratio of propagation delay times	A		0.5	0.8	1.3	0.5	0.8	1.3	
t_{TLH}	Transition time, low-to-high-level output			1	7	12	1	7	12	ns
t_{THL}	Transition time, high-to-low-level output			1	3	12	1	3	12	ns

PARAMETER MEASUREMENT INFORMATION





VOLTAGE WAVEFORMS

NOTES: A. Input pulses are supplied by a generator having the following characteristics: Z_o = 50 Ω, PRR = 5 MHz.
B. Includes probe and jig capacitance.
C. All diodes are 1N3064 or equivalent.
D. The strobe inputs of SN75129 are in-phase with the output.
E. V_{ref1} = 0.7 V and V_{ref2} = 1.7 V for testing data (A) inputs, V_{ref1} = V_{ref2} = 1.3 V for strobe inputs.

FIGURE 1

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TYPICAL CHARACTERISTICS

VOLTAGE TRANSFER CHARACTERISTICS

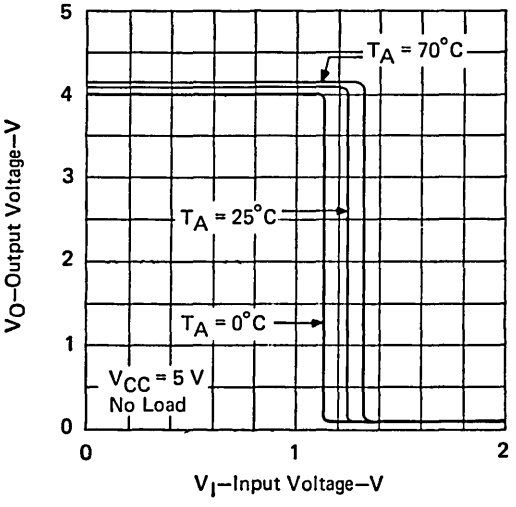


FIGURE 2

VOLTAGE TRANSFER CHARACTERISTICS
FROM A INPUTS

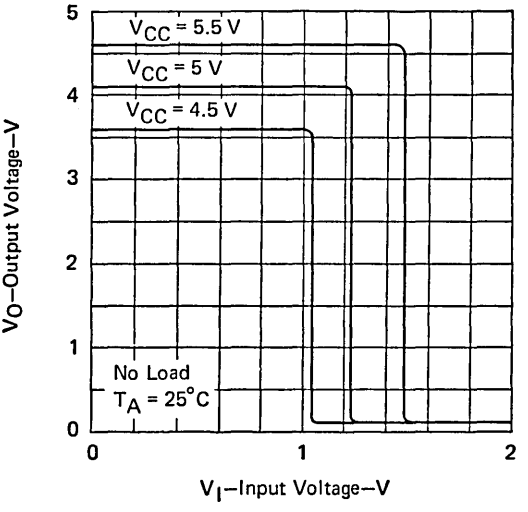


FIGURE 3

INPUT CURRENT
vs
INPUT VOLTAGE

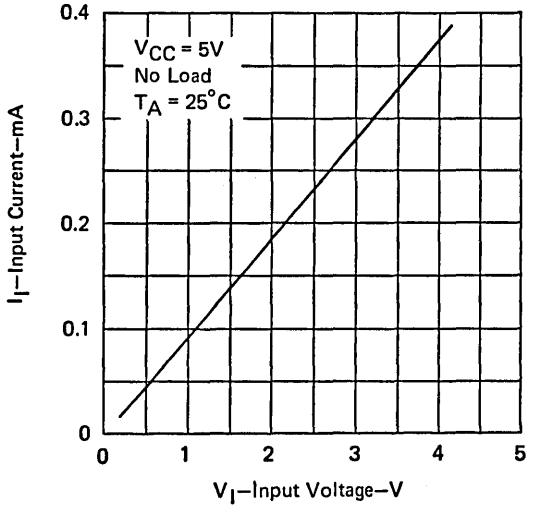


FIGURE 4

LOW-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

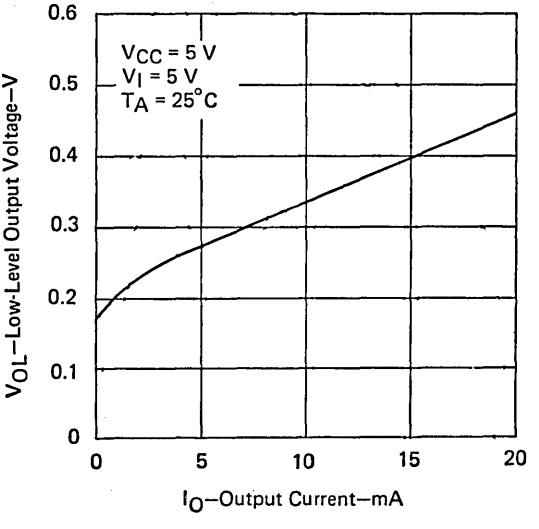


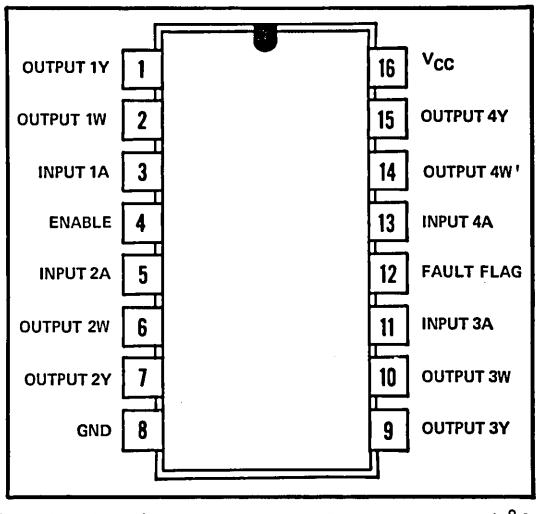
FIGURE 5

TYPE SN75130
QUADRUPLE LINE DRIVER

OCTOBER 1980

- Meets IBM 360/370 I/O Interface Specification GA22-6974-3 (Also See SN75126)
- Output Voltage of 3.11 V Min at I_{OH} = −60 mA
- Overload Protection with Foldback Current Limiting
- Common Enable and Common Fault Flag
- High-Speed, Low-Power Schottky Circuitry
- Functionally Interchangeable with MC 3485

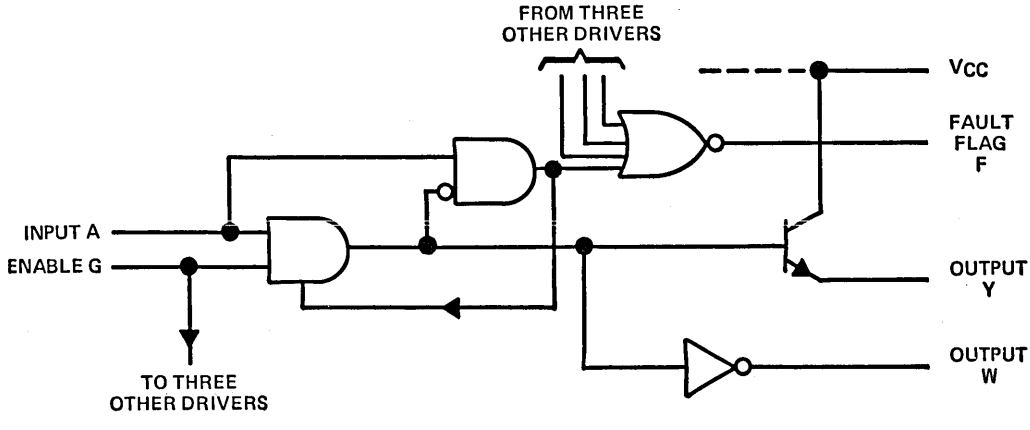
J OR N PACKAGE
(TOP VIEW)



description

The SN75130 quadruple line driver is designed to meet the IBM 360/370 I/O Specifications GA22-6974-3. The output voltage is 3.11 volts minimum (at I_{OH} = −60 milliamperes) over the recommended ranges of supply voltage (4.5 volts to 5.5 volts) and temperature (0°C to 70°C). This device is compatible with standard TTL logic and supply voltages. Fabrication techniques employ low-power Schottky technology to achieve fast switching and low power dissipation. The data bus will not be disturbed during power up and power down. Fault-flag circuitry is designed to sense a short on any of the Y output lines, output a logic low level, and reduce the output current on the shorted line to a safe level.

functional block diagram (one of four drivers, positive logic)



PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

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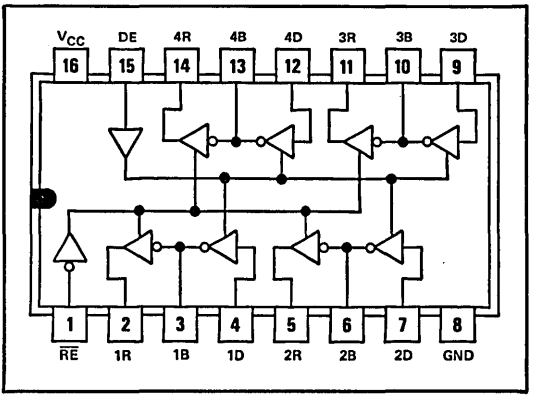
TYPE SN75136
QUADRUPLE BUS TRANSCEIVER WITH 3-STATE OUTPUTS

BULLETIN NO. DL-S 12485, JANUARY 1977

- P-N-P Inputs for Minimal Input Loading (200 μA Maximum)
- High-Speed Schottky Circuitry†
- 3-State Outputs for Driver and Receiver
- Party-Line (Data-Bus) Operation
- Single 5-V Supply
- 40-mA Current Sink Capability (Driver)
- Designed to be Functionally Interchangeable with Signetics N8T26

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



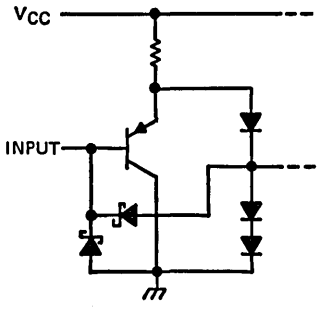
description

The SN75136 is a quadruple transceiver utilizing Schottky-diode-clamped transistors. Both the driver and receiver have three-state outputs. With p-n-p inputs, the input loading is minimized to a maximum input current of 200 μA.

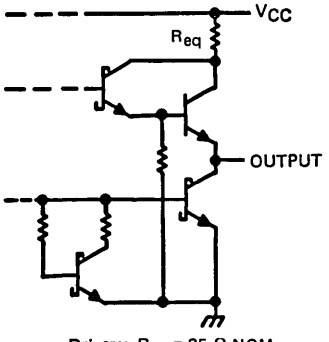
The SN75136 is characterized for operation from 0°C to 70°C.

schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



TYPICAL OF ALL OUTPUTS



Drivers: R_{eq} = 35 Ω NOM
Receivers: R_{eq} = 70 Ω NOM

FUNCTION TABLE (DRIVER)

INPUTS		OUTPUT
D	DE	B
L	H	H
H	H	L
X	L	Z

FUNCTION TABLE (RECEIVER)

INPUTS		OUTPUT
B	$\overline{RE}$	R
L	L	H
H	L	L
X	H	Z

H = high level, L = low level,
X = irrelevant, Z = high impedance

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2): N package . . . . . 1150 mW
J package . . . . . 1025 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1/16 inch from case for 10 seconds: N package . . . . . 260°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information Section, which starts on page 21. In the J package, SN75136 chips are glass-mounted.

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†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U.S. Patent Number 3,463,975.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level output current, I_{OH}	Driver			−10	mA
	Receiver			−2	
Low-level output current, I_{OL}	Driver			40	mA
	Receiver			16	
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended operating free-air temperature and supply voltage ranges (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage	B, D, DE, $\overline{RE}$		2			V
V_{IL}	Low-level input voltage	B, D, DE, $\overline{RE}$				0.85	V
V_{IK}	Input clamp voltage	B, D, DE, $\overline{RE}$	I_I = −5 mA			−1	V
V_{OH}	High-level output voltage	B	V_{IH} = 2 V, V_{IL} = 0.85 V, I_{OH} = −10 mA	2.6	3.1		V
		R	V_{IL} = 0.85 V, I_{OH} = −2 mA	2.6	3.1		
V_{OL}	Low-level output voltage	B	V_{IH} = 2 V, I_{OL} = 40 mA			0.5	V
		R	V_{IH} = 2 V, V_{IL} = 0.85 V, I_{OL} = 16 mA			0.5	
I_{OZ}	Off-state (high-impedance state) output current	B, R	DE at 0.85 V, $\overline{RE}$ at 2 V, V_O = 2.6 V			100	μA
		R	$\overline{RE}$ at 2 V, V_O = 0.5 V			−100	
I_{IH}	High-level input current	D, DE, $\overline{RE}$	V_I = 5.25 V			25	μA
I_{IL}	Low-level input current	B, D, DE, $\overline{RE}$	V_I = 0.4 V			−200	μA
I_{OS}	Short-circuit output current§	B	V_{CC} = 5.25 V	−50		−150	mA
		R		−30		−75	
I_{CC}	Supply current		V_{CC} = 5.25 V, No load			87	mA

†All typical values are at T_A = 25°C and V_{CC} = 5 V.
§Only one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		FROM	TO	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	B	R	C_L = 30 pF, See Figure 1		8	18	ns
t_{PHL}	Propagation delay time, high-to-low-level output					7	14	
t_{PLH}	Propagation delay time, low-to-high-level output	D	B	C_L = 300 pF, See Figure 2		11	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output					16	24	
t_{PLZ}	Output disable time from low level	$\overline{RE}$	R	C_L = 30 pF, See Figure 3		16	24	ns
t_{PZL}	Output enable time to low level					15	30	
t_{PLZ}	Output disable time from low level	DE	B	C_L = 300 pF, See Figure 4		9	24	ns
t_{PZL}	Output enable time to low level					31	38	

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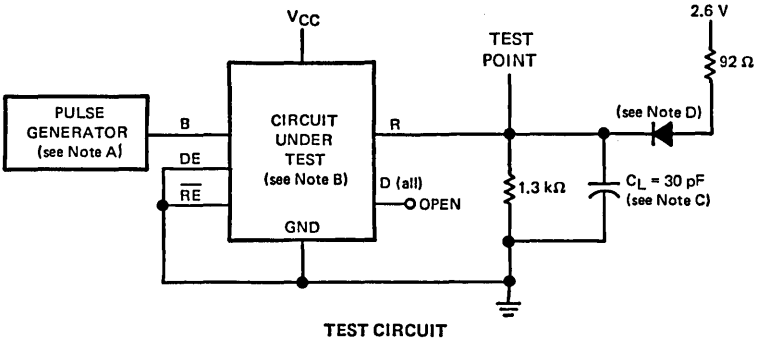
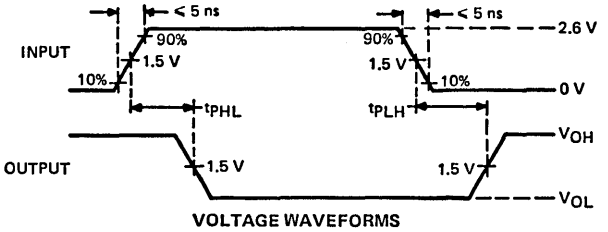
PARAMETER MEASUREMENT INFORMATION

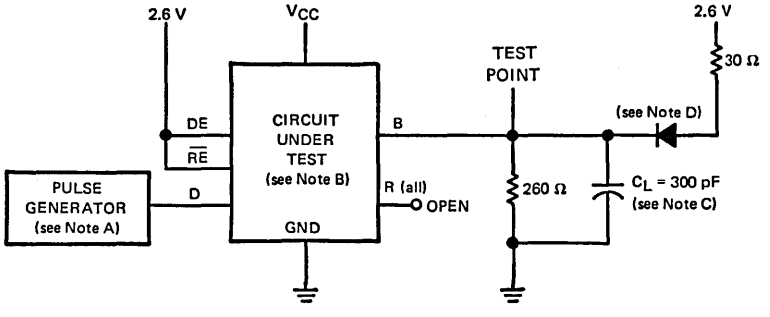


TEST CIRCUIT

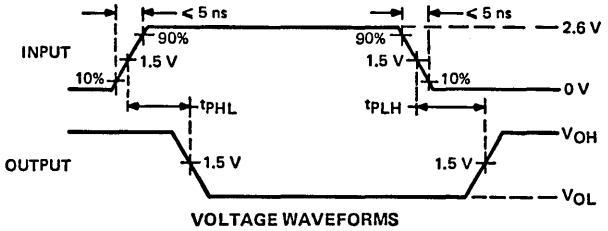


VOLTAGE WAVEFORMS

FIGURE 1–PROPAGATION DELAY TIMES FROM BUS TO RECEIVER OUTPUT



TEST CIRCUIT

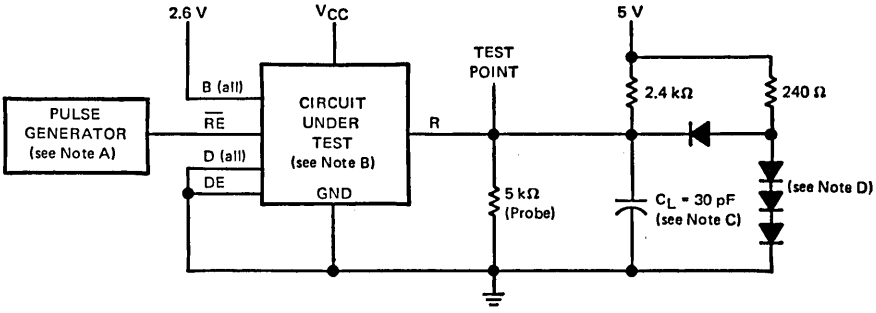


VOLTAGE WAVEFORMS

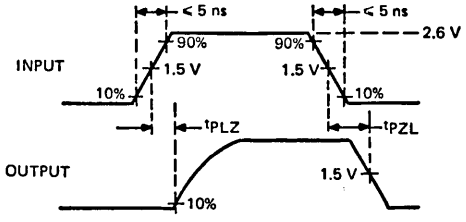
FIGURE 2–PROPAGATION DELAY TIMES FROM DRIVER INPUT TO BUS

NOTES: A. The pulse generator in Figures 1 and 2 has the following characteristics: PRR = 10 MHz, duty cycle = 50%, $Z_{out} \approx 50\ \Omega$.
B. All inputs and outputs not shown are open.
C. C_L includes probe and jig capacitance.
D. All diodes are 1N916 or 1N3064.

PARAMETER MEASUREMENT INFORMATION

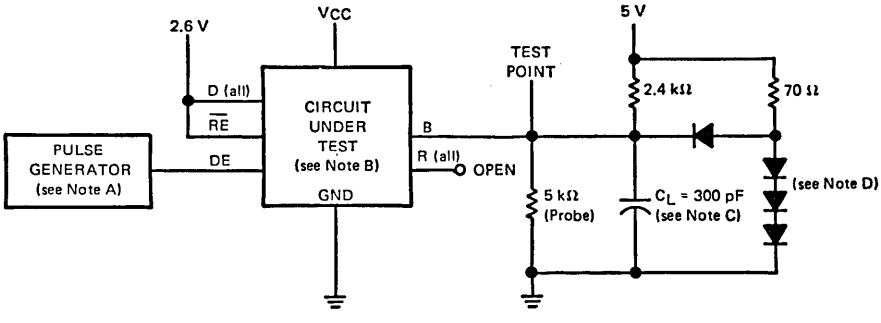


TEST CIRCUIT

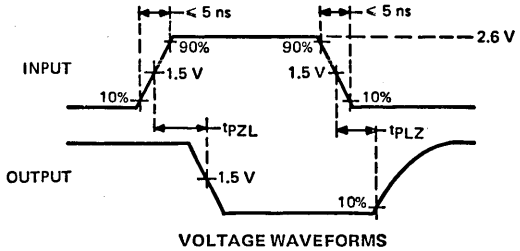


VOLTAGE WAVEFORMS

FIGURE 3–RECEIVER ENABLE AND DISABLE TIMES



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 4–DRIVER ENABLE AND DISABLE TIMES

NOTES: A. The pulse generator in Figures 3 and 4 has the following characteristics: PRR = 5 MHz, duty cycle = 50%, $Z_{out} \approx 50\ \Omega$.
B. All inputs and outputs not shown are open.
C. C_L includes probe and jig capacitance.
D. All diodes are 1N916 or 1N3064.

TEXAS INSTRUMENTS
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TYPES SN55138, SN75138
QUADRUPLE BUS TRANSCEIVERS

BULLETIN NO. DL-S 12046, SEPTEMBER 1973 – REVISED JANUARY 1977

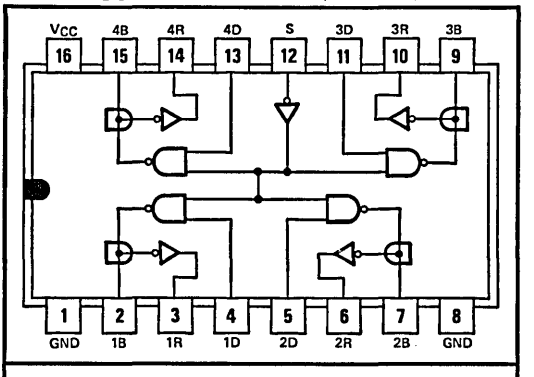
- Single 5-V Supply
- High-Input-Impedance, High-Threshold Receivers
- Common Driver Strobe
- TTL/DTL Compatible Driver and Strobe Inputs with Clamp Diodes
- High-Speed Operation
- 100-mA Open-Collector Driver Outputs
- Four Independent Channels
- TTL Compatible Receiver Output
- Available in Plastic or Ceramic 16-Pin Dual-In-Line Packages

description

The SN55138 and SN75138 quad bus transceivers are designed for two-way data communication over single-ended transmission lines. Each of the four identical channels consists of a driver with TTL inputs and a receiver with a TTL output. The driver output is of the open-collector type, and is designed to handle loads of up to 100 milliamperes (50 ohms to 5 volts). The receiver input is internally connected to the driver output, and has a high impedance to minimize loading of the transmission line. Because of the high driver-output current and the high receiver-input impedance, a very large number (typically hundreds) of transceivers may be connected to a single data bus.

The receiver design also features a threshold of 2.3 volts (typical), providing a wider noise margin than would be possible with a receiver having the usual TTL threshold. A strobe turns off all drivers (high impedance) but does not affect receiver operation. These circuits are designed for operation from a single five-volt supply and include a provision to minimize loading of the data bus when the power-supply voltage is zero. The SN55138 is characterized for operation over the full military temperature range of –55°C to 125°C; the SN75138 is characterized for operation from 0°C to 70°C.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



Positive logic: $B = \overline{DS}$, $R = \overline{B}$
Each bus terminal, B, is a driver output and a receiver input.

FUNCTION TABLE (TRANSMITTING)

INPUTS		OUTPUTS	
S	D	B	R
L	H	L	H
L	L	H	L

FUNCTION TABLE (RECEIVING)

INPUTS			OUTPUT
S	B	D	R
H	H	X	L
H	L	X	H

H = high level, L = low level, X = irrelevant

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

		SN55138	SN75138	UNIT
Supply voltage, V_{CC} (see Note 1)		7	7	V
Input voltage		5.5	5.5	V
Driver off-state output voltage		7	7	V
Low-level output current into the driver output		150	150	mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2)	J package	1375	1025	mW
	N package		1150	
Operating free-air temperature range		–55 to 125	0 to 70	°C
Storage temperature range		–65 to 150	–65 to 150	°C
Lead temperature 1/16 inch from case for 60 seconds: J package		300	300	°C
Lead temperature 1/16 inch from case for 10 seconds: N package			260	°C

NOTES: 1. Voltage values are with respect to both ground terminals connected together.
2. For operation above 25°C free-air temperature, refer to the Dissipation Derating Curves in the Thermal Information section, which starts on page 21. In the J package, SN55138 chips are alloy-mounted; SN75138 chips are glass-mounted.

recommended operating conditions

		SN55138			SN75138			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Low-level output current, I_{OL}	Driver output			100			100	mA
	Receiver output			16			16	
High-level output current, I_{OH}	Receiver output			−400			−400	μA
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN55138			SN75138			UNIT
					MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage	Driver or strobe			2			2			V
		Receiver			3.2			2.9			
V_{IL}	Low-level input voltage	Driver or strobe					0.8			0.8	V
		Receiver					1.5			1.8	
V_{IK}	Input clamp voltage	Driver or strobe	V_{CC} = MIN,	I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	Receiver	V_{CC} = MIN, $V_{IL(R)} = V_{IL}$ max,	$V_{IH(S)}$ = 2 V, I_{OH} = −400 μA	2.4	3.5		2.4	3.5		V
V_{OL}	Low-level output voltage	Driver	V_{CC} = MIN, $V_{IL(S)}$ = 0.8 V,	$V_{IH(D)}$ = 2 V, I_{OL} = 100 mA			0.45			0.45	V
		Receiver	V_{CC} = MIN, $V_{IH(S)}$ = 2 V,	$V_{IH(R)} = V_{IH}$ min, I_{OL} = 16 mA			0.4			0.4	
I_I	Input current at maximum input voltage	Driver or strobe	V_{CC} = MAX,	$V_I = V_{CC}$			1			1	mA
I_{IH}	High-level input current	Driver or strobe	V_{CC} = MAX,	V_I = 2.4 V			40			40	μA
		Receiver	V_{CC} = 5 V, $V_{I(S)}$ = 2 V	$V_{I(R)}$ = 4.5 V,		25	300		25	300	
I_{IL}	Low-level input current	Driver or strobe	V_{CC} = MAX,	V_I = 0.4 V		−1	−1.6		−1	−1.6	mA
		Receiver	V_{CC} = MAX, $V_{I(S)}$ = 2 V	$V_{I(R)}$ = 0.45 V,			−50			−50	μA
	Input current with power off	Receiver	V_{CC} = 0,	V_I = 4.5 V		1.1	1.5		1.1	1.5	mA
I_{OS}	Short-circuit output current§	Receiver	V_{CC} = MAX		−20		−55	−18		−55	mA
I_{CC}	Supply current	All driver outputs low	V_{CC} = MAX, $V_{I(S)}$ = 0.8 V	$V_{I(D)}$ = 2 V,		50	65		50	65	mA
		All driver outputs high	V_{CC} = MAX, $V_{I(S)}$ = 2 V, Receiver outputs open	$V_{I(R)}$ = 3.5 V,		42	55		42	55	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions. Parenthetical letters D, R, and S used with V_I refer to the driver input, receiver input, and strobe input, respectively.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

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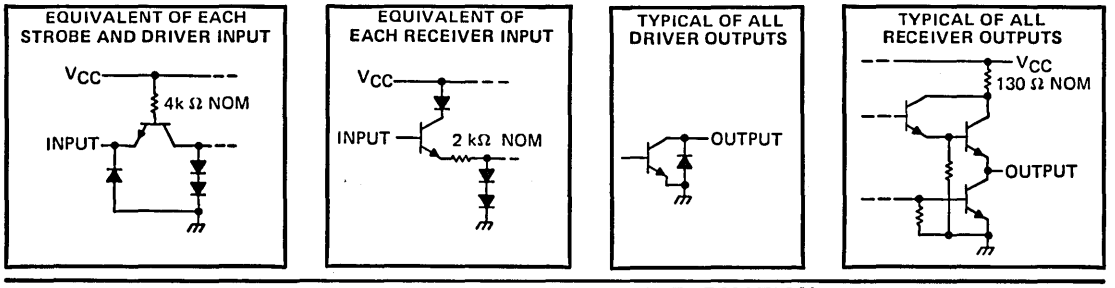
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Driver	Driver	C_L = 50 pF, R_L = 50 Ω, See Figure 1		15	24	ns
t_{PHL}					14	24	
t_{PLH}	Strobe	Driver			18	28	ns
t_{PHL}					22	32	
t_{PLH}	Receiver	Receiver	C_L = 15 pF, R_L = 400 Ω, See Figure 2		7	15	ns
t_{PHL}					8	15	

¶ t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output

schematics of inputs and outputs



PARAMETER MEASUREMENT INFORMATION

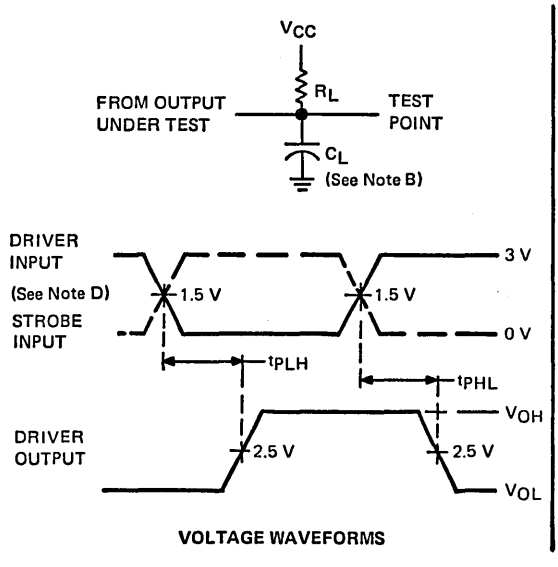


FIGURE 1–PROPAGATION DELAY TIMES FROM DATA AND STROBE INPUTS

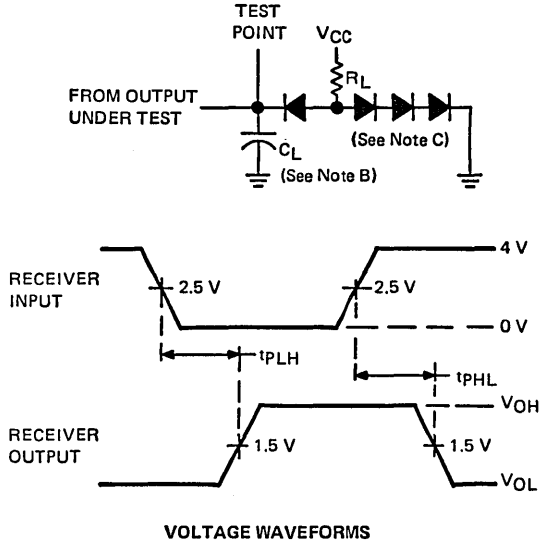
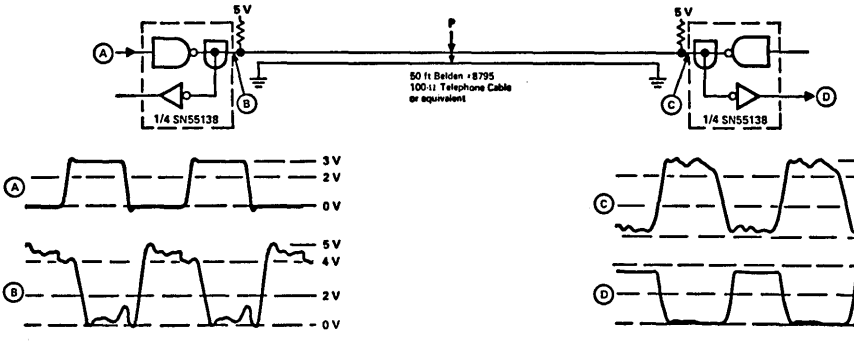


FIGURE 2–PROPAGATION DELAY TIMES FROM RECEIVER INPUT

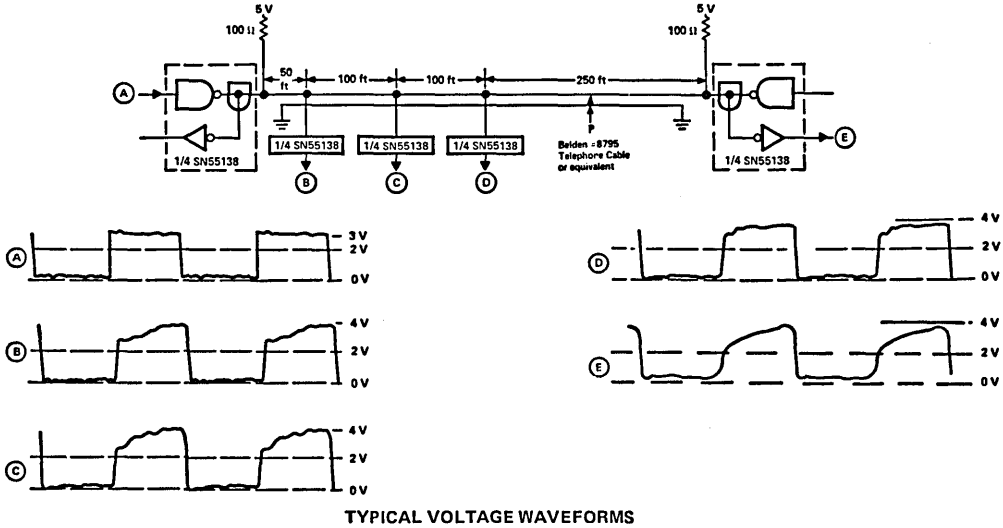
NOTES: A. Input pulses are supplied by generators having the following characteristics: t_w = 100 ns, PRR = 1 MHz, t_r ≤10ns, t_f ≤10 ns, Z_{out} ≈ 50 Ω.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916 or 1N3064.
D. When testing driver input (solid line) strobe must be low; when testing strobe input (dashed line) driver input must be high.

TYPICAL APPLICATION DATA



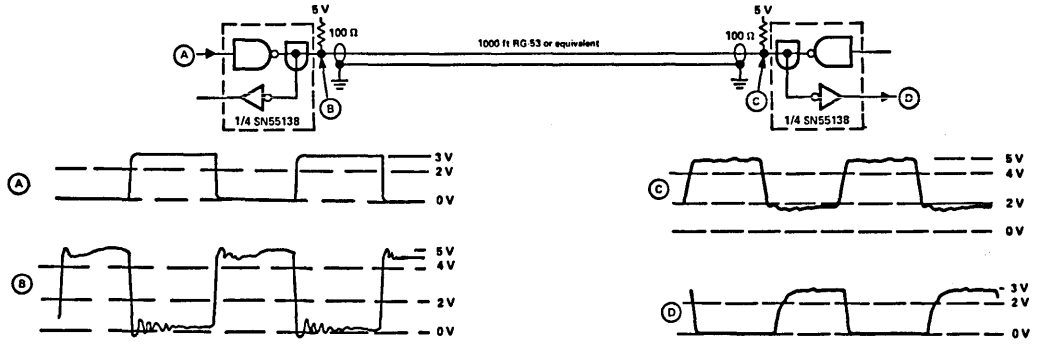
TYPICAL VOLTAGE WAVEFORMS

FIGURE 3–POINT-TO-POINT COMMUNICATION OVER 50 FEET OF TWISTED PAIR AT 5 MHz



TYPICAL VOLTAGE WAVEFORMS

FIGURE 4–PARTY-LINE COMMUNICATION ON 500 FEET OF TWISTED PAIR AT 1 MHz



TYPICAL VOLTAGE WAVEFORMS

FIGURE 5–POINT-TO-POINT COMMUNICATION OVER 1000 FEET OF COAX AT 1 MHz

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TYPICAL CHARACTERISTICS†

DRIVER TRANSFER CHARACTERISTICS

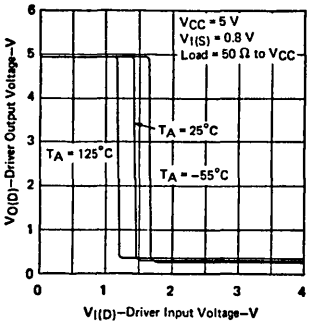

FIGURE 6

DRIVER TRANSFER CHARACTERISTICS

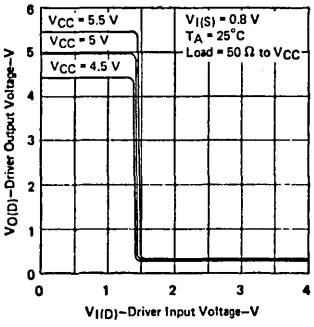

FIGURE 7

STROBE-TO-DRIVER-OUTPUT TRANSFER CHARACTERISTICS

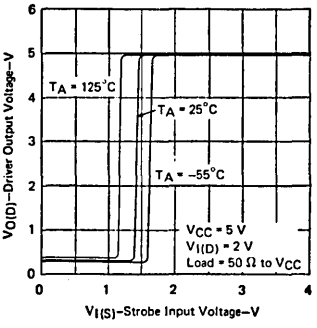

FIGURE 8

STROBE-TO-DRIVER OUTPUT TRANSFER CHARACTERISTICS

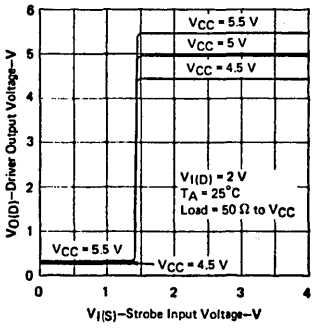

FIGURE 9

RECEIVER TRANSFER CHARACTERISTICS

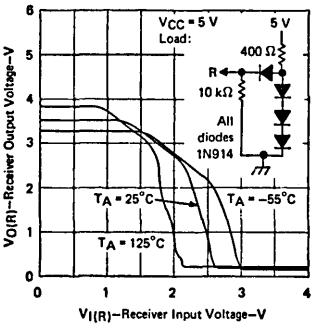

FIGURE 10

RECEIVER TRANSFER CHARACTERISTICS

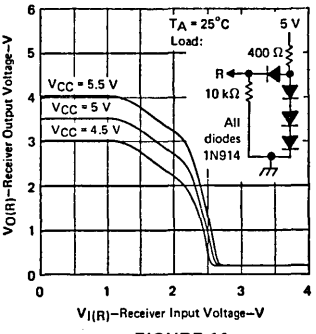

FIGURE 11

HIGH-LEVEL OUTPUT VOLTAGE vs OUTPUT CURRENT (RECEIVER)

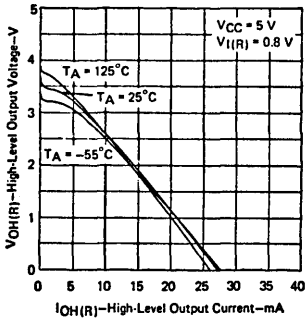

FIGURE 12

HIGH-LEVEL OUTPUT VOLTAGE vs OUTPUT CURRENT (RECEIVER)

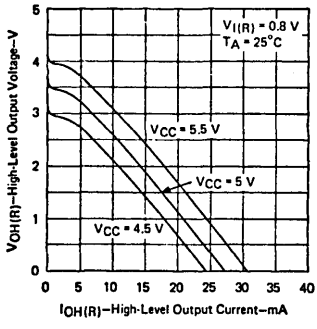

FIGURE 13

LOW-LEVEL OUTPUT VOLTAGE vs OUTPUT CURRENT (RECEIVER)

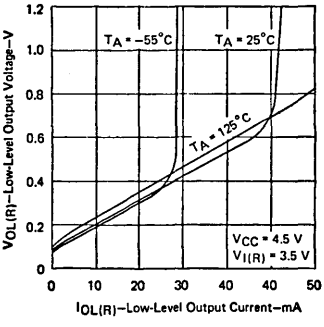

FIGURE 14

†Data for temperatures below 0°C and above 70°C is applicable to SN55138 circuits only.

TYPICAL CHARACTERISTICS†

LOW-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT (DRIVER OUTPUT)

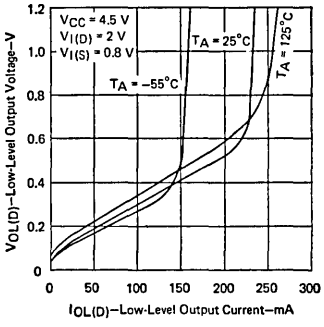

FIGURE 15

RECEIVER INPUT CURRENT
vs
RECEIVER INPUT VOLTAGE

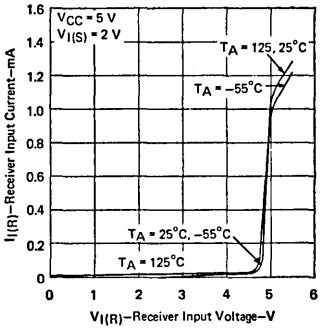

FIGURE 16

RECEIVER INPUT CURRENT
vs
RECEIVER INPUT VOLTAGE

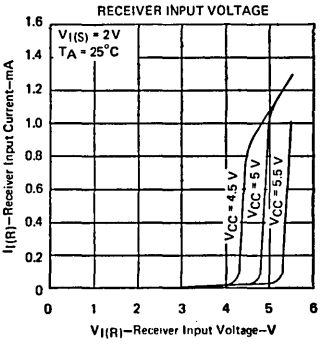

FIGURE 17

SUPPLY CURRENT
vs
SUPPLY VOLTAGE
(ALL DRIVER OUTPUTS LOW)

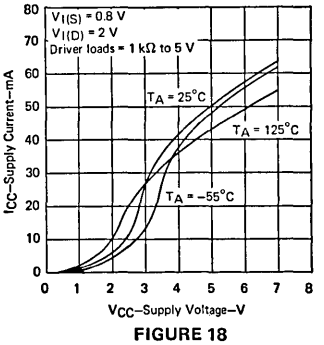

FIGURE 18

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

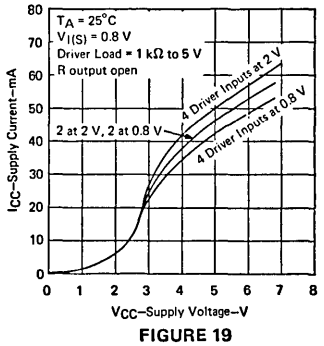

FIGURE 19

PROPAGATION DELAY TIMES
vs
FREE-AIR TEMPERATURE

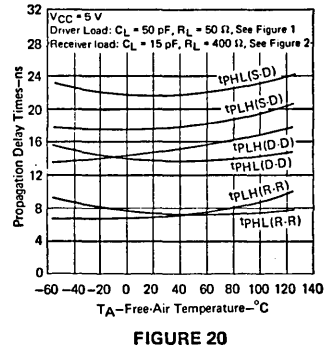

FIGURE 20

PROPAGATION DELAY TIMES
vs
SUPPLY VOLTAGE

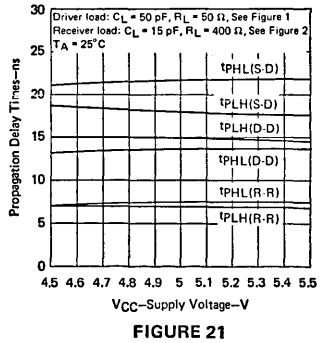

FIGURE 21

DRIVER PROPAGATION DELAY TIMES
vs
LOAD CAPACITANCE

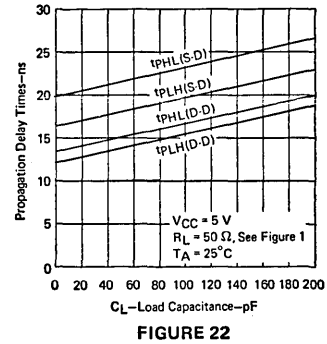

FIGURE 22

RECEIVER PROPAGATION DELAY TIMES
vs
LOAD CAPACITANCE

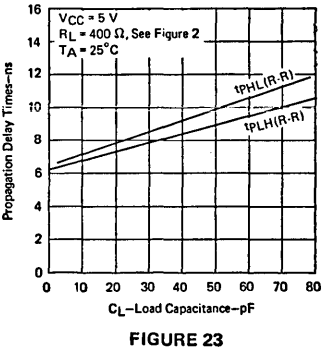

FIGURE 23

†Data for temperatures below 0°C and above 70°C is applicable to SN55138 circuits only.

TEXAS INSTRUMENTS
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TYPES SN55140, SN55141, SN55142A, SN55143A, SN75140, SN75141, SN75142A, SN75143A DUAL LINE RECEIVERS

BULLETIN NO. DL-S 12456, JANUARY 1977–REVISED JULY 1979

features common to all eight types

- Single 5-V Supply
- ±100 mV Sensitivity
- For Application As:
  Single-Ended Line Receiver
  Gated Oscillator
  Level Comparator
- Adjustable Reference Voltage
- TTL Outputs
- TTL-Compatible Strobe
- Designed for Party-Line (Data-Bus) Applications

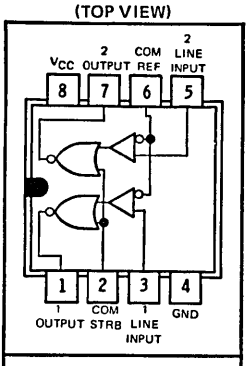
features of '140 and '141

- Common Reference Pin
- Common Strobe
- '141 Has Diode-Protected Input Stage for Power-Off Condition

features of '142A and '143A

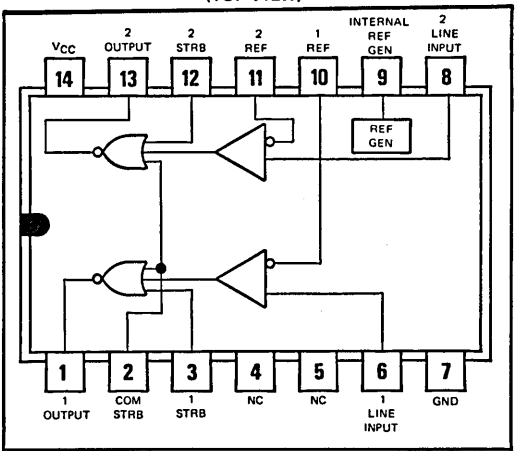
- Individual Reference Pins
- Common and Individual Strobes
- Internal 2.5-Volt Reference Available
- '143A Has Diode-Protected Input Stage for Power-Off Condition

SN55140, SN55141 . . .
JG DUAL-IN-LINE PACKAGE
SN75140, SN75141 . . .
JG OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic:
see function table

SN55142A, SN55143A . . . J DUAL-IN-LINE PACKAGE
SN75142A, SN75143A . . . J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: see function table

NC—No internal connection

Pin 2, if unused, must be grounded when replacing '142 or '143 with '142A or '143A devices.

description

Each of these devices consists of a dual single-ended line receiver with TTL-compatible strobes and outputs. The reference voltage (switching threshold) is applied externally and can be adjusted from 1.5 volts to 3.5 volts, making it possible to optimize noise immunity for a given system design. A 2.5-volt internal reference is available for use on the '142A and '143A. Due to their low input current (less than 100 microamperes), they are ideally suited for party-line (bus-organized) systems.

The '140 has a common reference voltage pin and a common strobe. The '141 is the same as the '140 except that the input stage is diode protected. Each receiver of the '142A has an individual reference voltage pin and an individual strobe. The '143A is the same as the '142A except that the input stage is diode protected. The internal reference voltage of the '142A and '143A can be externally adjusted with a single resistor from 1.5 volts to 3.5 volts.

'140, '141 FUNCTION TABLE
(EACH RECEIVER)

LINE INPUT	STROBE	OUTPUT
$\leq V_{ref} - 100$ mV	L	H
$\geq V_{ref} + 100$ mV	X	L
X	H	L

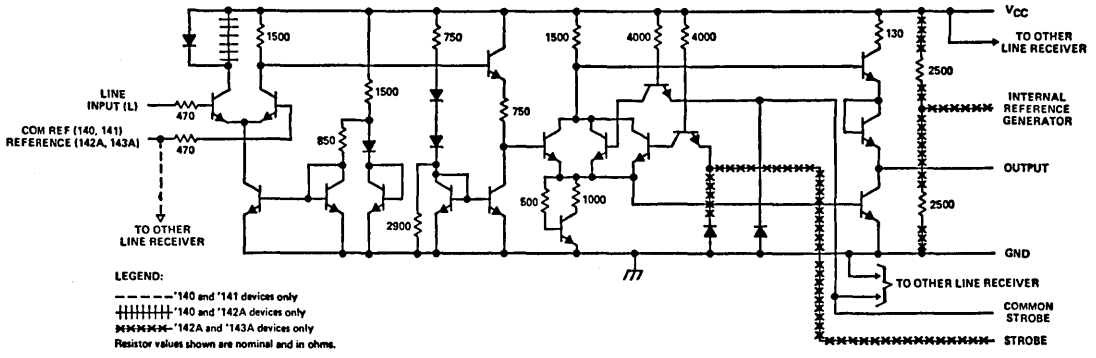
H = high level, L = low level, X = irrelevant

'142A, '143A FUNCTION TABLE
(EACH RECEIVER)

LINE INPUT	INDIVIDUAL STROBE	COMMON STROBE	OUTPUT
$\leq V_{REF} - 100$ mV	L	L	H
$\geq V_{REF} + 100$ mV	X	X	L
X	H	X	L
X	X	H	L

H = high level, L = low level, X = irrelevant

schematic (each receiver)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Reference input voltage, V_{ref} . . . . . 5.5 V
Line input voltage with respect to ground . . . . . −2 V to 5.5 V
Line input voltage with respect to V_{ref} . . . . . ±5 V
Strobe input voltage . . . . . 5.5 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 600 mW
Operating free-air temperature range: SN55′ Circuits . . . . . −55°C to 125°C
SN75′ Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J or JG package . . . . . 300°C
Lead temperature 1/16 inch from case for 10 seconds: N or P package . . . . . 260°C

NOTES: 1. Unless otherwise specified, voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, see the Dissipation Derating Table. In the J and JG package, these chips are glass mounted.

DISSIPATION DERATING TABLE

PACKAGE	POWER RATING	DERATING FACTOR	ABOVE T_A
J	600 mW	8.2 mW/°C	77°C
JG	600 mW	6.6 mW/°C	59°C
N	600 mW	9.2 mW/°C	85°C
P	600 mW	8.0 mW/°C	75°C

recommended operating conditions

		SN55′ CIRCUITS			SN75′ CIRCUITS			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.5	5	5.5	V
Reference input voltage, V_{ref}		1.5		3.5	1.5		3.5	V
Input voltage, V_I	Line	0		$V_{CC}-1$	0		$V_{CC}-1$	V
	Strobe	0		5.5	0		5.5	
Operating free-air temperature, T_A		−55		125	0		70	°C

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electrical characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 10%, V_{ref} = 1.5 V to 3.5 V (unless otherwise noted)

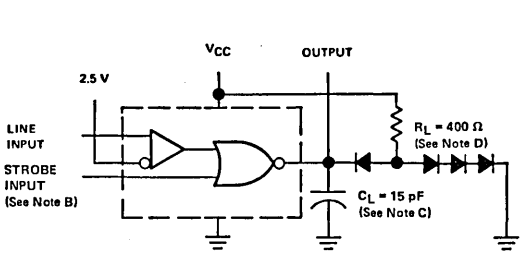
PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$V_{IH(L)}$	High-level line input voltage			V_{ref} + 100			mV
$V_{IL(L)}$	Low-level line input voltage					V_{ref} – 100	mV
$V_{IH(S)}$	High-level strobe input voltage			2			V
$V_{IL(S)}$	Low-level strobe input voltage					0.8	V
V_{OH}	High-level output voltage		$V_{IL(L)}$ = V_{ref} – 100 mV, $V_{IL(S)}$ = 0.8 V, I_{OH} = –400 μA	2.4			V
V_{OL}	Low-level output voltage		$V_{IH(L)}$ = V_{ref} + 100 mV, $V_{IL(S)}$ = 0.8 V, I_{OL} = 16 mA			0.4	V
			$V_{IL(L)}$ = V_{ref} – 100 mV, $V_{IH(S)}$ = 2 V, I_{OL} = 16 mA			0.4	
$V_{IK(S)}$	Strobe input clamp voltage		$I_{I(S)}$ = –12 mA			–1.5	V
$I_{I(S)}$	Strobe input current at maximum input voltage	Strobe	$V_{I(S)}$ = 5.5 V			1	mA
		Com strb				2	
I_{IH}	High-level input current	Strobe	$V_{I(S)}$ = 2.4 V			40	μA
		Com strb				80	
		Line input	$V_{I(L)}$ = 3.5 V, V_{ref} = 1.5 V		35	100	
		Reference	$V_{I(L)}$ = 0 V, V_{ref} = 3.5 V		35	100	
		Com ref			70	200	
I_{IL}	Low-level input current	Strobe	$V_{I(S)}$ = 0.4 V			–1.6	mA
		Com strb				–3.2	
		Line input	$V_{I(L)}$ = 0 V, V_{ref} = 1.5 V			–10	μA
		Reference	$V_{I(L)}$ = 1.5 V, V_{ref} = 0 V			–10	
		Com ref				–20	
V_{gen}	Internal reference generator voltage	'142A, '143A	V_{CC} = 5 V, I_{gen} = 0	2.3	2.5	2.7	V
			V_{CC} = 5 V, I_{gen} = –70 μA		2.4		
I_{OS}	Short-circuit output current‡		V_{CC} = 5.5 V	–15		–55	mA
I_{CCH}	Supply current, output high		$V_{I(S)}$ = 0 V, $V_{I(L)}$ = V_{ref} – 100 mV		18	30	mA
I_{CCL}	Supply current, output low		$V_{I(S)}$ = 0 V, $V_{I(L)}$ = V_{ref} + 100 mV		20	35	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡Only one output should be shorted at a time.

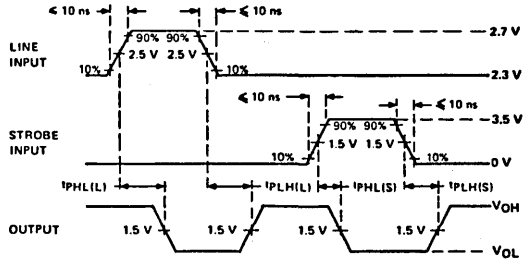
switching characteristics, V_{CC} = 5 V, V_{ref} = 2.5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH(L)}$	Propagation delay time, low-to-high-level output from line input	C_L = 15 pF, R_L = 400 Ω, See Figure 1		22	35	ns
$t_{PHL(L)}$	Propagation delay time, high-to-low-level output from line input			22	30	
$t_{PLH(S)}$	Propagation delay time, low-to-high-level output from strobe input			12	22	ns
$t_{PHL(S)}$	Propagation delay time, high-to-low-level output from strobe input			8	15	

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 1

NOTES: A. Input pulses are supplied by generators having the following characteristics: PRR = 1 MHz, duty cycle ≤ 50%, Z_{out} ≈ 50 Ω.
B. Unused strobe(s) is (are) to be grounded.
C. C_L includes probe and jig capacitance.
D. All diodes are 1N3064.

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
LINE INPUT VOLTAGE

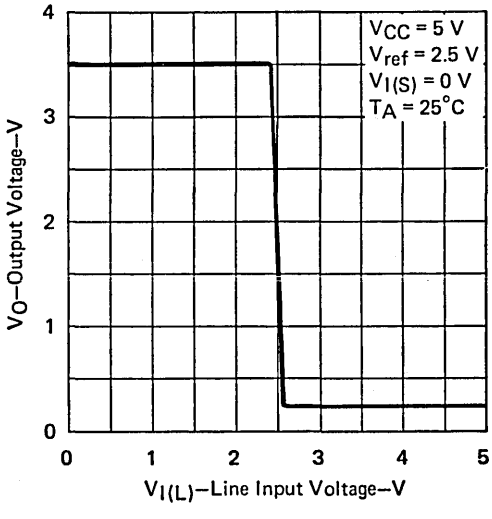


FIGURE 2

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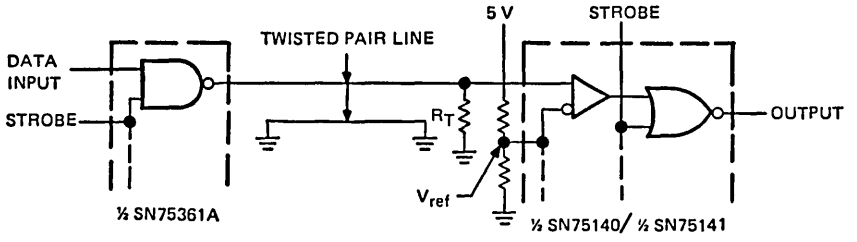
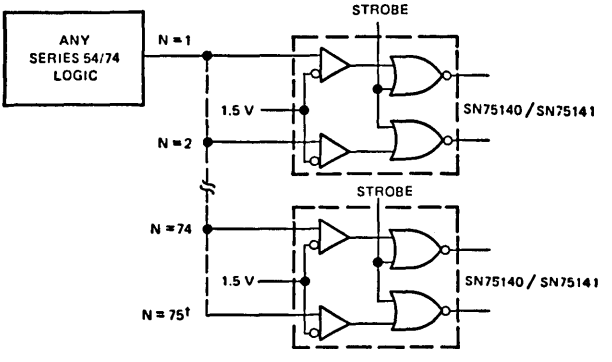
TYPICAL APPLICATION DATA

line receiver

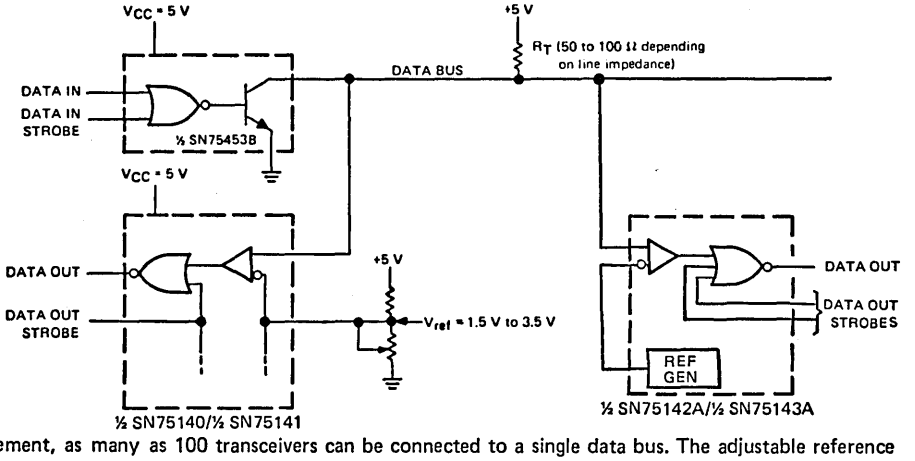


high fan-out from standard TTL gate



†Although most Series 54/74 circuits have a guaranteed 2.4-V output at 400 μA, they are typically capable of maintaining a 2.4-V output level under a load of 7.5 mA.

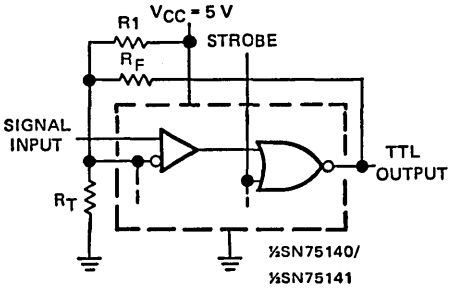
dual bus transceiver



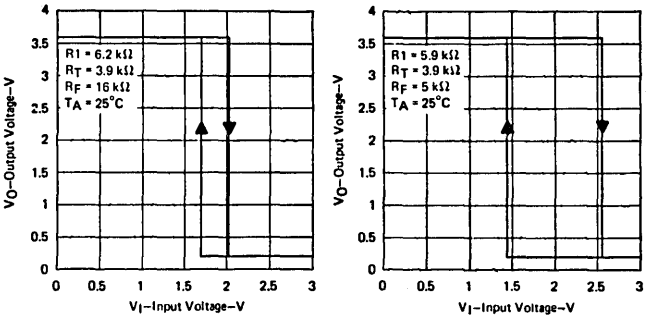
Using this arrangement, as many as 100 transceivers can be connected to a single data bus. The adjustable reference voltage feature allows the noise margin to be optimized for a given system. The complete dual bus transceiver (SN75453B driver and SN75140 receiver) can be assembled in approximately the same space required by a single 16-pin package, and only one power supply is required (+5 V). Data In and Data Out terminals are TTL compatible.

TYPICAL APPLICATION DATA

schmitt trigger

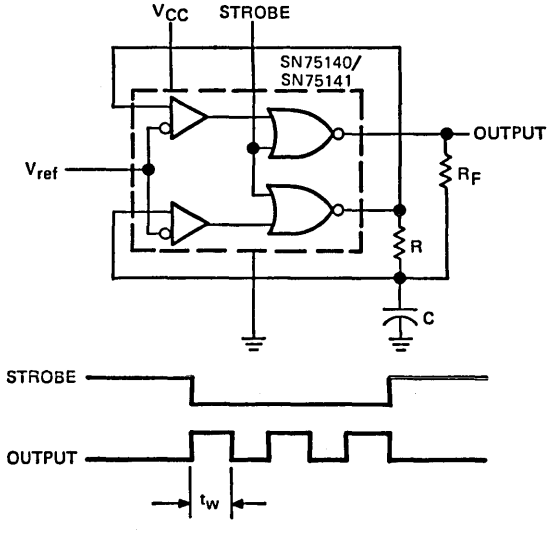


EXAMPLES OF TRANSFER CHARACTERISTICS

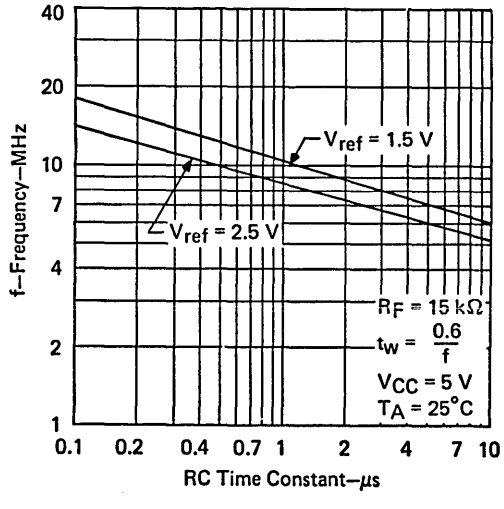


Slowly changing input levels from data lines, optical detectors, and other types of transducers may be converted to standard TTL signals with this Schmitt trigger circuit. R1, R_F, and R_T may be adjusted for the desired hysteresis and trigger levels.

gated oscillator



OSCILLATOR FREQUENCY
vs
RC TIME CONSTANT



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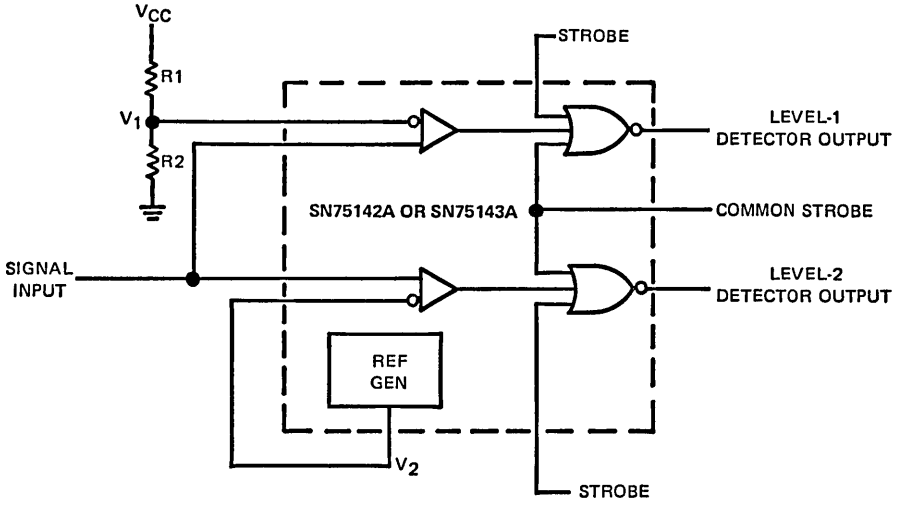
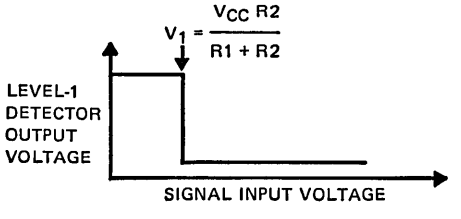
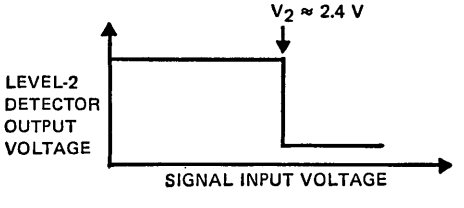
TYPICAL APPLICATION DATA

level detector



VOLTAGE TRANSFER CHARACTERISTICS WITH STROBES LOW



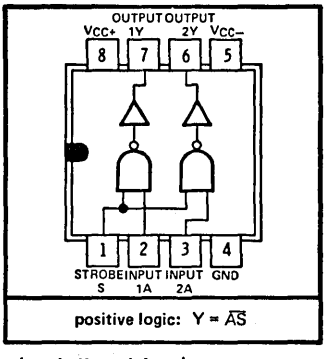


TYPE SN75150
DUAL LINE DRIVER

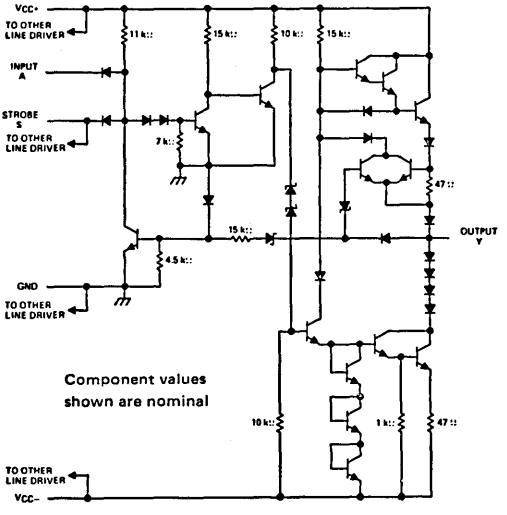
BULLETIN NO. DL-S 11428, JANUARY 1971 – REVISED JANUARY 1977

- Satisfies Requirements of EIA Standard RS-232-C
- Withstands Sustained Output Short-Circuit to any Low-Impedance Voltage between –25 V and 25 V
- 2 μs Max Transition Time through the +3 V to –3 V Transition Region under Full 2500-pF Load
- Inputs Compatible with Most TTL and DTL Families
- Common Strobe Input
- Inverting Output
- Slew Rate can be Controlled with an External Capacitor at the Output
- Standard Supply Voltages . . . ±12 V

JG OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)



schematic (each line driver)



description

The SN75150 is a monolithic dual line driver designed to satisfy the requirements of the standard interface between data terminal equipment and data communication equipment as defined by EIA Standard RS-232-C. A rate of 20,000 bits per second can be transmitted with a full 2500-pF load. Other applications are in data-transmission systems using relatively short single lines, in level translators, and for driving MOS devices. The logic input is compatible with most TTL and DTL families. Operation is from +12-volt and –12-volt power supplies. The SN75150 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC+} (see Note 1)	.15 V
Supply voltage V_{CC-}	–15 V
Input voltage	.15 V
Applied output voltage	±25 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2): JG package	925 mW
P package	1000 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	–65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: JG package	300°C
Lead temperature 1/16 inch from case for 10 seconds: P package	260°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 21. In the JG package, SN75150 chips are glass-mounted.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage V_{CC+}	10.8	12	13.2	V
Supply voltage V_{CC-}	−10.8	−12	−13.2	V
Input voltage, V_I	0		5.5	V
Applied output voltage, V_O			±15	V
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP†	MAX (SEE NOTE 3)	UNIT
V_{IH}	High-level input voltage	1			2			V
V_{IL}	Low-level input voltage	2					0.8	V
V_{OH}	High-level output voltage	2	V_{CC+} = 10.8 V, V_{CC-} = −13.2 V, V_{IL} = 0.8 V, R_L = 3 kΩ to 7 kΩ		5	8		V
V_{OL}	Low-level output voltage (See note 3)	1	V_{CC+} = 10.8 V, V_{CC-} = −10.8 V, V_{IH} = 2 V, R_L = 3 kΩ to 7 kΩ			−8	−5	V
I_{IH}	High-level input current	3	V_{CC+} = 13.2 V, V_{CC-} = −13.2 V, V_I = 2.4 V	Data input		1	10	μA
				Strobe input		2	20	
I_{IL}	Low-level input current	3	V_{CC+} = 13.2 V, V_{CC-} = −13.2 V, V_I = 0.4 V	Data input		−1	−1.6	mA
				Strobe input		−2	−3.2	
I_{OS}	Short-circuit output current‡	4	V_{CC+} = 13.2 V, V_{CC-} = −13.2 V	V_O = 25 V		2	8	mA
				V_O = −25 V		−3	−8	
				V_O = 0 V, V_I = 3 V	10	15	30	
				V_O = 0 V, V_I = 0 V	−10	−15	−30	
I_{CCH+}	Supply current from V_{CC+}, high-level output	5	V_{CC+} = 13.2 V, V_{CC-} = −13.2 V, V_I = 0 V, R_L = 3 kΩ, T_A = 25°C			10	22	mA
I_{CCH-}	Supply current from V_{CC-}, high-level output					−1	−10	mA
I_{CCL+}	Supply current from V_{CC+}, low-level output	5	V_{CC+} = 13.2 V, V_{CC-} = −13.2 V, V_I = 3 V, R_L = 3 kΩ, T_A = 25°C			8	17	mA
I_{CCL-}	Supply current from V_{CC-}, low-level output					−9	−20	mA

NOTE 3: The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for logic levels only, e.g., when −5 V is the maximum, the typical value is a more negative voltage.

†All typical values are at V_{CC+} = 12 V, V_{CC-} = −12 V, T_A = 25°C.

‡Not more than one output should be shorted at a time.

switching characteristics, V_{CC+} = 12 V, V_{CC-} = −12 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{TLH}	Transition time, low-to-high-level output	6	C_L = 2500 pF, R_L = 3 kΩ to 7 kΩ	0.2	1.4	2	μs
t_{THL}	Transition time, high-to-low-level output			0.2	1.5	2	μs
t_{TLH}	Transition time, low-to-high-level output	6	C_L = 15 pF, R_L = 7 kΩ		40		ns
t_{THL}	Transition time, high-to-low-level output				20		ns
t_{PLH}	Propagation delay time, low-to-high-level output	6	C_L = 15 pF, R_L = 7 kΩ		60		ns
t_{PHL}	Propagation delay time, high-to-low-level output				45		ns

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PARAMETER MEASUREMENT INFORMATION

d-c test circuits‡

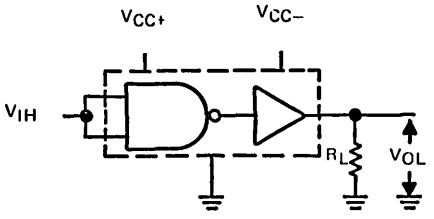
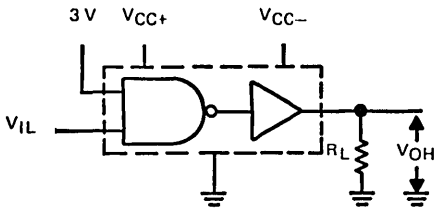
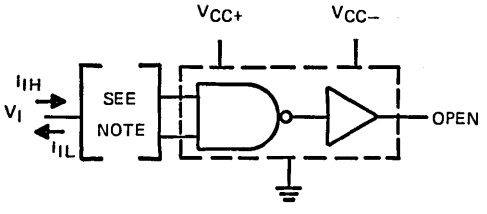


FIGURE 1–V_{IH}, V_{OL}



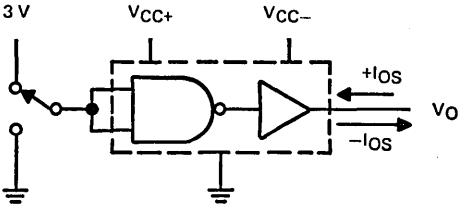
Each input is tested separately.

FIGURE 2–V_{IL}, V_{OH}



NOTE: When testing I_{IH}, the other input is at 3 V; when testing I_{IL}, the other input is open.

FIGURE 3–I_{IH}, I_{IL}



I_{OS} is tested for both input conditions at each of the specified output conditions.

FIGURE 4–I_{OS}

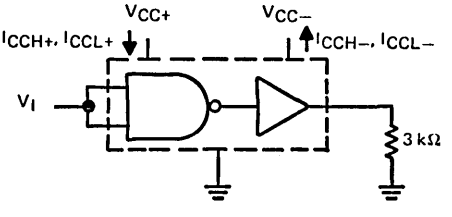
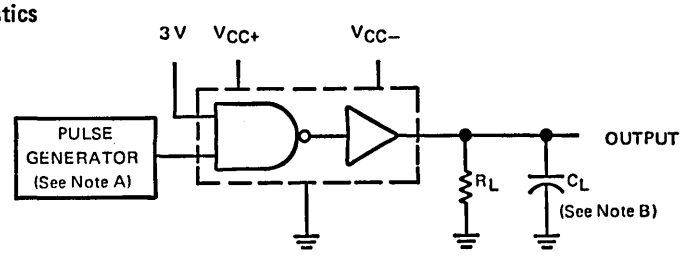


FIGURE 5–I_{CCH+}, I_{CCH-}, I_{CCL+}, I_{CCL-}

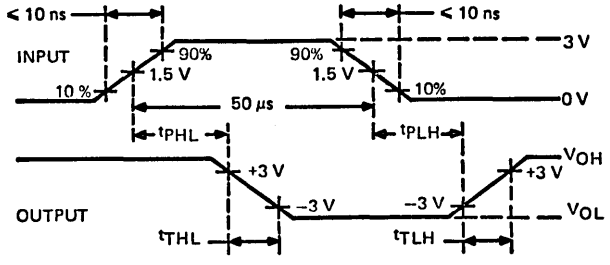
‡Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: duty cycle ≤ 50%, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

FIGURE 6–SWITCHING CHARACTERISTICS

TYPICAL CHARACTERISTICS

OUTPUT CURRENT
vs
APPLIED OUTPUT VOLTAGE

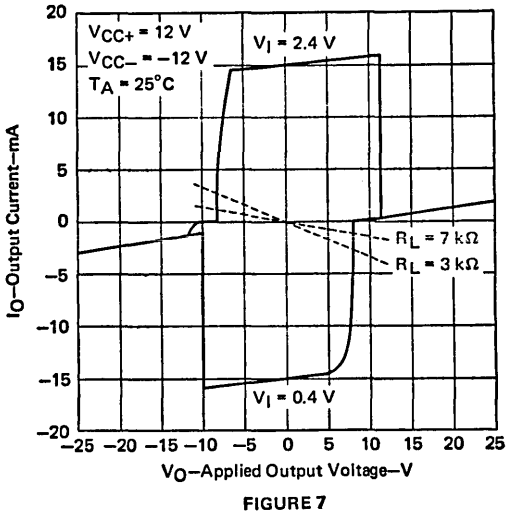


FIGURE 7

TYPICAL APPLICATION DATA

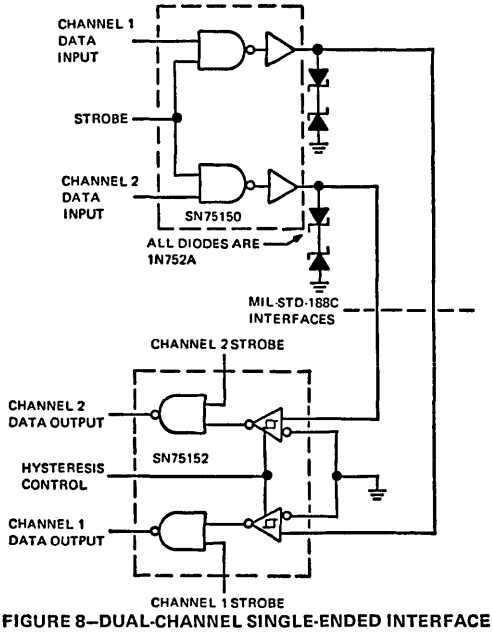


FIGURE 8–DUAL-CHANNEL SINGLE-ENDED INTERFACE CIRCUIT MEETING MIL-STD-188C, PARAGRAPH 7.2.

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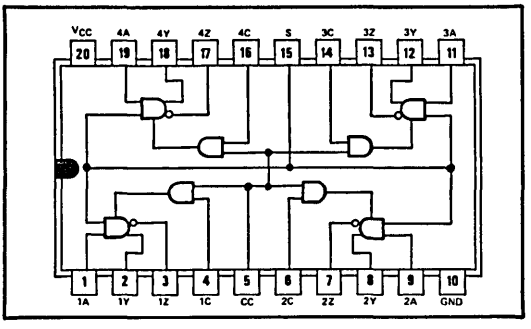
TYPES SN55151, SN55153, SN75151, SN75153
QUAD DIFFERENTIAL LINE DRIVERS WITH 3-STATE OUTPUTS

BULLETIN NO. DL-S 12629, DECEMBER 1978

- Meets EIA Standard RS-422A
- High-Impedance Output State for Party-Line Operation
- High Output Impedance in Power-Off Condition
- Low Input Current to Minimize Loading
- Single 5-V Supply
- 40-mA Sink- and Source-Current Capability
- High-Speed Schottky Circuitry
- Low Power Requirements

SN55151 . . . . J
SN75151 . . . . J OR N
DUAL-IN-LINE PACKAGE
(TOP VIEW)



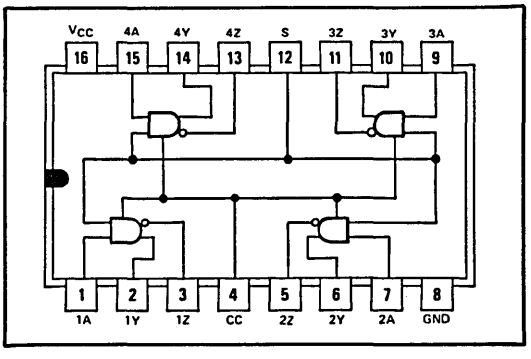
description

These line drivers are designed to provide differential signals with high current capability on balanced lines. These circuits provide strobe and enable inputs to control all four drivers, and the '151 provides an additional enable input for each driver. The output circuits have active pull-up and pull-down and are capable of sinking or sourcing 40 milliamperes.

The '151 and '153 meet all requirements of RS-422A and Federal Standard 1020.

The SN55151 and SN55153 are characterized over the full military temperature range of −55°C to 125°C. The SN75151 and SN75153 are characterized for operation from 0°C to 70°C.

SN55153 . . . . J
SN75153 . . . . J OR N
DUAL-IN-LINE PACKAGE
(TOP VIEW)

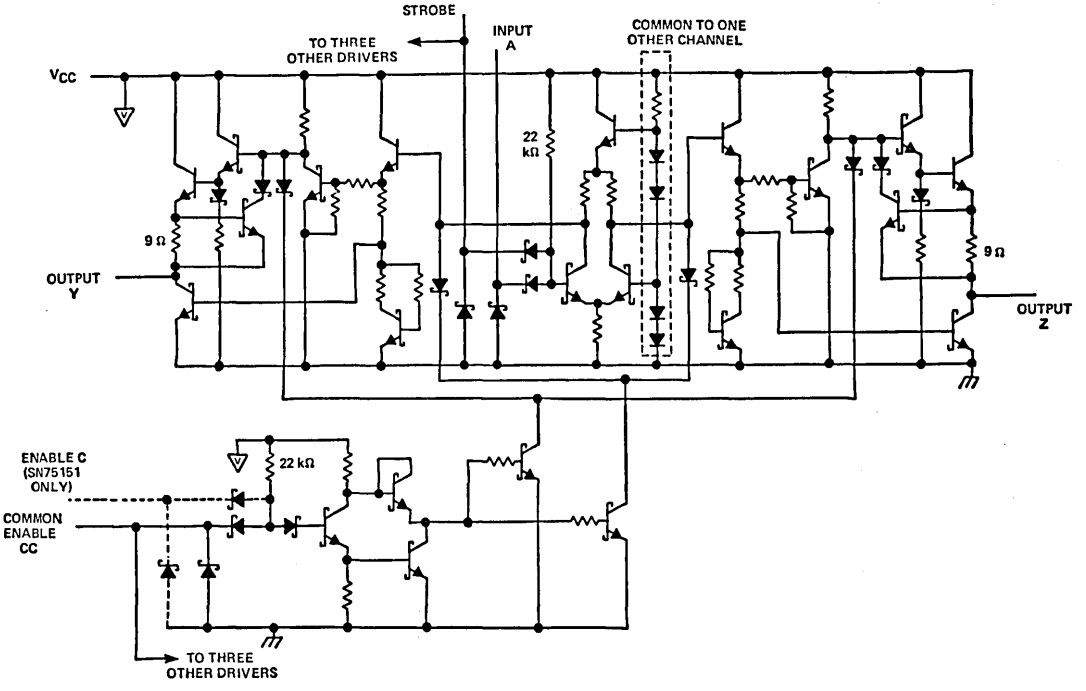


SN55151, SN75151
FUNCTION TABLE

INPUTS				OUTPUTS	
ENABLE CC	ENABLE C	STROBE	DATA A	Y	Z
L	X	X	X	Z	Z
X	L	X	X	Z	Z
H	H	L	X	L	H
H	H	X	L	L	H
H	H	H	H	H	L

SN55153, SN75153
FUNCTION TABLE

INPUTS			OUTPUTS	
ENABLE CC	STROBE	DATA A	Y	Z
L	X	X	Z	Z
H	L	X	L	H
H	X	L	L	H
H	H	H	H	L



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2)	1 W
Operating free-air temperature range: SN55151, SN55153	−55°C to 125°C
SN75151, SN75153	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch (1, 6 mm) from case for 60 seconds: J package	300°C
Lead temperature 1/16 inch (1, 6 mm) from case for 10 seconds: N package	260°C

NOTES: 1. All voltage values, except differential output voltage V_{OD}, are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, refer to the Dissipation Derating Table. In the J package, SN55151 and SN55153 chips are alloy-mounted; SN75151 and SN75153 chips are glass-mounted.

DISSIPATION DERATING TABLE

PACKAGE	POWER RATING	DERATING FACTOR	ABOVE T_A
J (Alloy-mounted)	1000 mW	11 mW/°C	59°C
J (Glass-mounted)	1000 mW	8.2 mW/°C	28°C
N	1000 mW	9.2 mW/°C	41°C

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recommended operating conditions

	SN55'			SN75'			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Common-mode output voltage	−0.25		6	−0.25		6	V
High-level output current, I_{OH}			−40			−40	mA
Low-level output current, I_{OL}			40			40	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN55'			SN75'			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA	CC, S			−2			−2	V
			All others		−0.9	−1.5		−0.9	−1.5	
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = 2 V	I_{OH} = −20 mA	2.4			2.5			V
			I_{OH} = −40 mA	2			2.4			
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V,	V_{IL} = MAX, I_{OL} = 40 mA			0.5			0.5	V
$\lvert V_{OD1} \rvert$	Differential output voltage	V_{CC} = MAX,	I_O = 0		3.4	$2V_{OD2}$		3.4	$2V_{OD2}$	V
$\lvert V_{OD2} \rvert$	Differential output voltage	V_{CC} = MIN	R_L = 100 Ω, See Figure 1	2	2.8		2	2.8		V
$\Delta\lvert V_{OD} \rvert$	Change in magnitude of differential output voltage§	V_{CC} = MIN			±0.01	±0.4		±0.01	±0.4	V
V_{OC}	Common-mode output voltage¶	V_{CC} = MAX			1.9	3		1.8	3	V
		V_{CC} = MIN			1.5	3		1.6	3	
$\Delta\lvert V_{OC} \rvert$	Change in magnitude of common-mode output voltage§	V_{CC} = MIN or MAX			±0.02	±0.4		±0.02	±0.4	V
I_{OZ}	Off-state (high-impedance-state) output current	V_{CC} = MAX, Enable at 0.8 V	V_O = 0.5 V			−150			−20	μA
			V_O = 2.5 V			80			20	
			V_O = V_{CC}			150			20	
I_O	Output current with power off	V_{CC} = 0	V_O = 6 V		0.1	100		0.1	100	μA
			V_O = −0.25 V		−0.1	−100		−0.1	−100	
			V_O = −0.25 V to 6 V			±100			±100	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V	C ('151), A			20			20	μA
			CC, S			80			80	
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V	C ('151), A			−0.36			−0.36	mA
			CC, S			−1.6			−1.6	
I_{OS}	Short-circuit output current#	V_{CC} = MAX		−50	−90	−150	−50	−90	−150	mA
I_{CC}	Supply current (both drivers)	V_{CC} = MAX, No load	outputs disabled		30	60		30	60	mA
			outputs enabled		60	80		60	80	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at T_A = 25°C and V_{CC} = 5 V except for V_{OC}, for which V_{CC} is as stated under test conditions.
§$\Delta\lvert V_{OD} \rvert$ and $\Delta\lvert V_{OC} \rvert$ are the changes in magnitudes of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
¶In EIA Standard RS-422A, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.
#Only one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 30 pF, R_L = 100 Ω, See Figure 2, Termination A		15	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output			15	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 30 pF See Figure 2, Termination B		13	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output			13	25	ns
t_{TLH}	Transition time, low-to-high-level output	C_L = 30 pF, R_L = 100 Ω, See Figure 2, Termination A		12	20	ns
t_{THL}	Transition time, high-to-low-level output			12	20	ns
t_{PZH}	Output enable time to high level	C_L = 30 pF, R_L = 60 Ω, See Figure 3		18	35	ns
t_{PZL}	Output enable time to low level	C_L = 30 pF, R_L = 111 Ω, See Figure 4		20	35	ns
t_{PHZ}	Output disable time from high level	C_L = 30 pF, R_L = 60 Ω, See Figure 3		19	30	ns
t_{PLZ}	Output disable time from low level	C_L = 30 pF, R_L = 111 Ω, See Figure 4		13	30	ns
	Overshoot factor	R_L = 100 Ω, See Figure 2, Termination C			10	%

PARAMETER MEASUREMENT INFORMATION

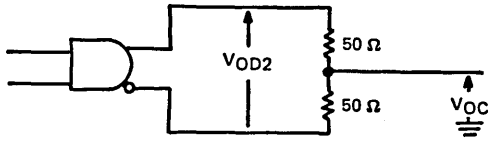
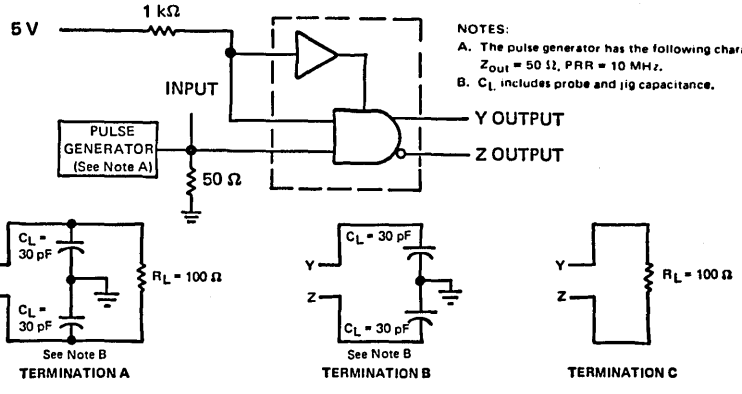


FIGURE 1–DIFFERENTIAL AND COMMON-MODE OUTPUT VOLTAGES



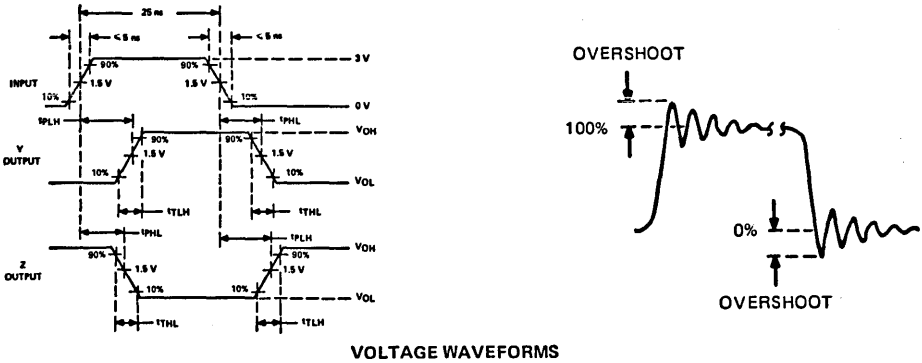


FIGURE 2–t_{PLH}, t_{PHL}, t_{TLH}, t_{THL}, AND OVERSHOOT FACTOR

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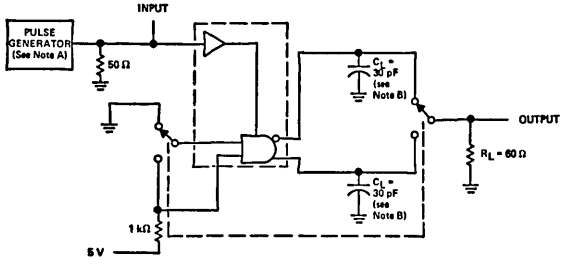
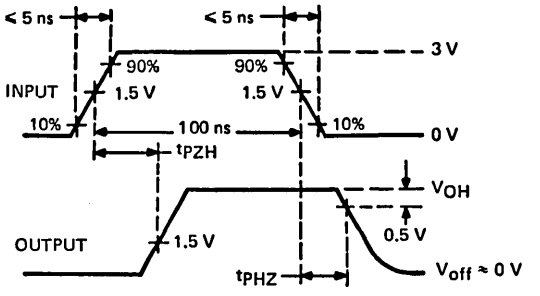
PARAMETER MEASUREMENT INFORMATION

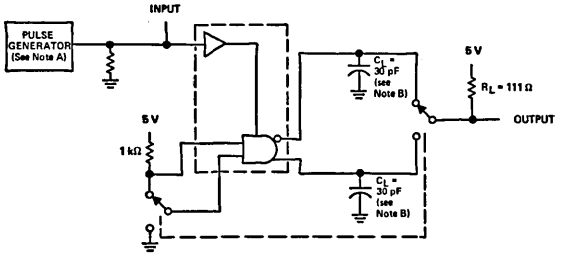


TEST CIRCUIT

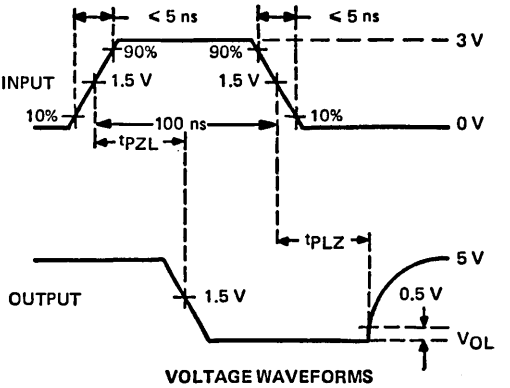


VOLTAGE WAVEFORMS

FIGURE 3–t_{PZH} AND t_{PHZ}



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 4–t_{PZL} AND t_{PLZ}

NOTES: A. The pulse generators have the following characteristics: Z_{out} = 50 Ω, PRR = 500 kHz
B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

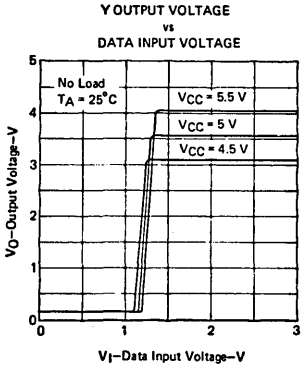


FIGURE 5

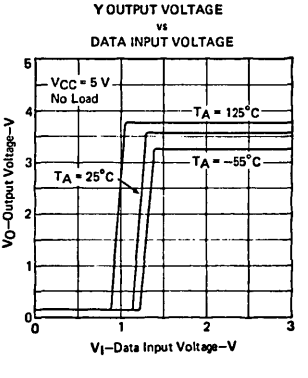


FIGURE 6

TYPICAL CHARACTERISTICS†

OUTPUT VOLTAGE
vs
ENABLE INPUT VOLTAGE

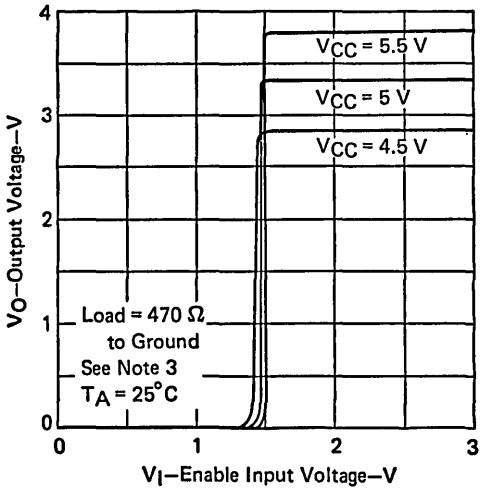


FIGURE 7

OUTPUT VOLTAGE
vs
ENABLE INPUT VOLTAGE

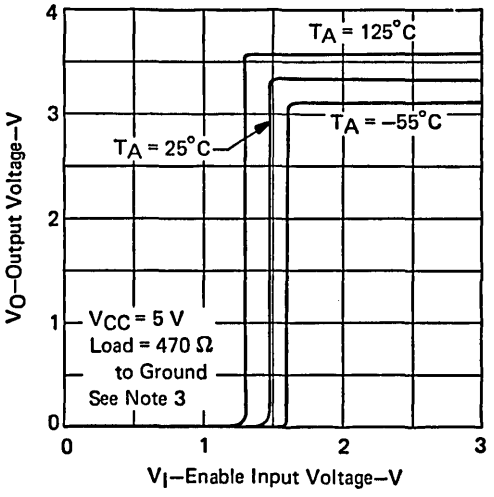


FIGURE 8

OUTPUT VOLTAGE
vs
ENABLE INPUT VOLTAGE

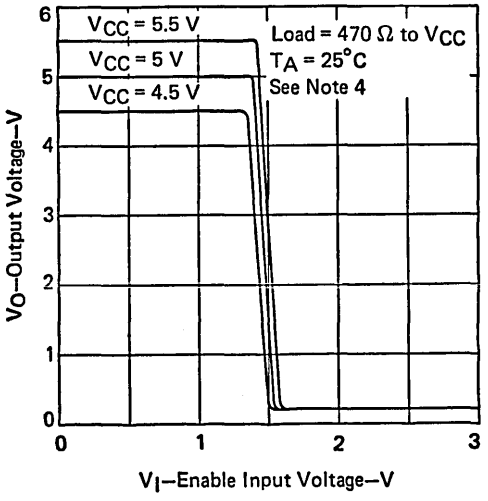


FIGURE 9

OUTPUT VOLTAGE
vs
ENABLE INPUT VOLTAGE

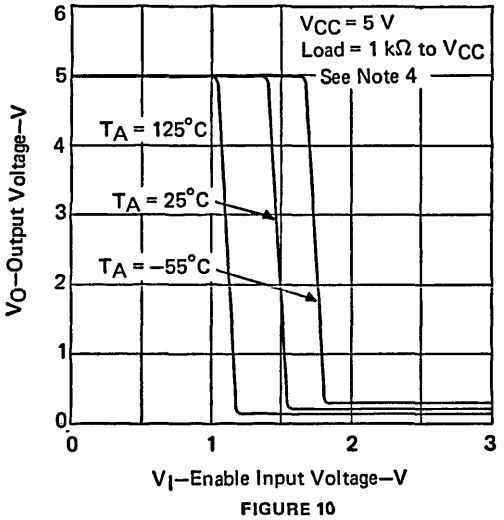


FIGURE 10

NOTES: 3. The A input is connected to V_{CC} during the testing of the Y outputs and to ground during testing of the Z outputs.
4. The A input is connected to ground during the testing of the Y outputs and to V_{CC} during the testing of the Z inputs.

†Data for temperatures below 0°C and above 70°C are applicable to SN55151 and SN55153 circuits only.

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TYPICAL CHARACTERISTICS†

HIGH-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

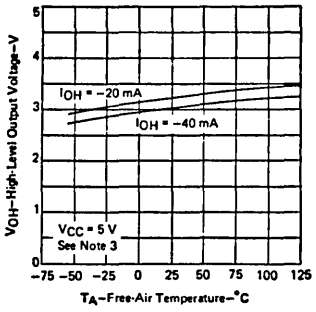


FIGURE 11

HIGH-LEVEL OUTPUT VOLTAGE vs OUTPUT CURRENT

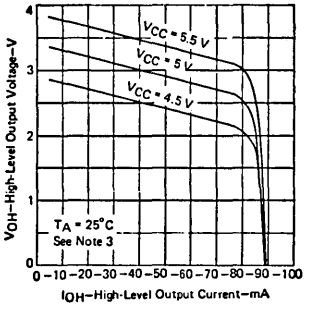


FIGURE 12

LOW-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

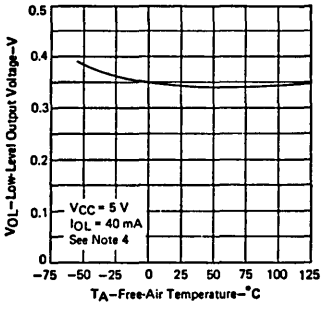


FIGURE 13

LOW-LEVEL OUTPUT VOLTAGE vs OUTPUT CURRENT

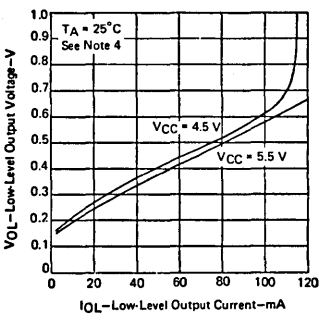


FIGURE 14

SUPPLY CURRENT vs SUPPLY VOLTAGE

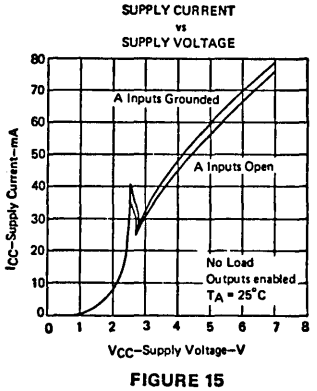


FIGURE 15

SUPPLY CURRENT vs SUPPLY VOLTAGE

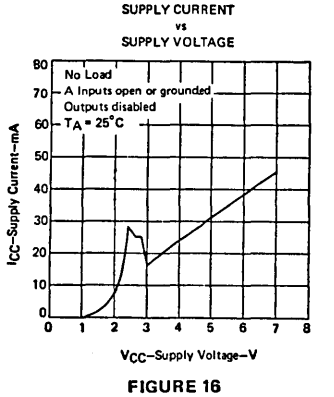


FIGURE 16

NOTES: 3. The A input is connected to V_{CC} during the testing of the Y outputs and to ground during testing of the Z outputs.

4. The A input is connected to ground during the testing of the Y outputs and to V_{CC} during the testing of the Z outputs.

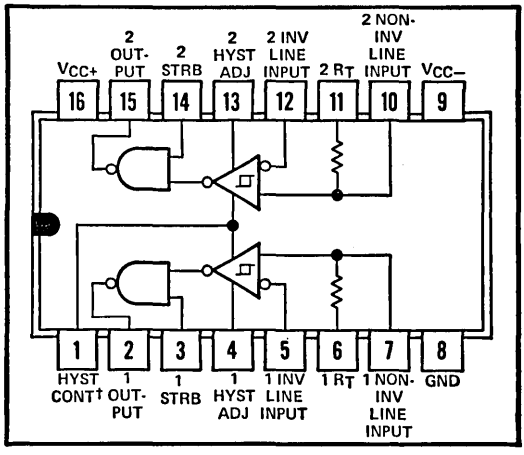
†Data for temperature below 0°C and above 70°C are applicable to SN55151 and SN55153 circuits only.

TYPE SN75152
DUAL LINE RECEIVER

BULLETIN NO. DL-S 11755, AUGUST 1972

- Meets Specifications of EIA RS-232-C or MIL-STD-188C†
- Dual Differential Receiver with Independent Strobes
- Common-Mode Input Voltage Range . . . ±25 V
- Differential Input Capability with One Input Grounded . . . ±25 V
- Continuously Adjustable Hysteresis with External Resistors
- Standard Supply Voltages . . . +12 V and −12 V
- Input Hysteresis (Double Thresholds) Remain Approximately Fixed for Power Supply and/or Temperature Variations

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



†To meet the specifications of EIA Standard RS-232-C, connect Hysteresis Control (Pin 1) to V_{CC-} (Pin 9). Also, connect pin 6 to pin 5 and pin 11 to pin 12. To meet the specifications of MIL-STD-188, leave Hysteresis Control (pin 1) and termination resistors (pin 6 and 11) open.

description

The SN75152 is a dual differential line receiver designed to meet the requirements of EIA standard RS-232-C or MIL-STD-188 interfaces. A single control (pin 1) sets the input hysteresis for the required operation. An added feature is the capability of adjusting the hysteresis to any voltage between ± 0.3 volt typical and ± 5 volts typical by means of the hysteresis adjust terminals (pin 4 and 13) making the SN75152 useful for a wide variety of line receiver and Schmitt trigger applications. The large common-mode input voltage range and differential input voltage (± 25 volts) give the circuit added versatility. The SN75152 is designed for operation from standard ± 12-volt supplies with ± 10% variation. Each receiver has an output strobe that is TTL compatible.

FUNCTION TABLE
(EACH RECEIVER)

LINE INPUT	STROBE	OUTPUT
H	H	H
L	H	L
X	L	H

Definition of logic levels:

For the strobe: H (high) is any voltage between V_{IH} min and V_{CC}.
L (low) is any voltage between ground and V_{IL} max.

For the line input: H (high) is any differential input voltage (V_{ID})‡ more positive than V_{T-}, once the level of V_{T+} has been reached.
L (low) is any differential input voltage (V_{ID})‡ more negative than V_{T+}, once the level of V_{T-} has been reached.
X (irrelevant) is any input voltage permitted by maximum ratings.

‡Differential input voltages (V_T and V_{ID}) are at the noninverting input terminal with respect to the inverting input terminal.

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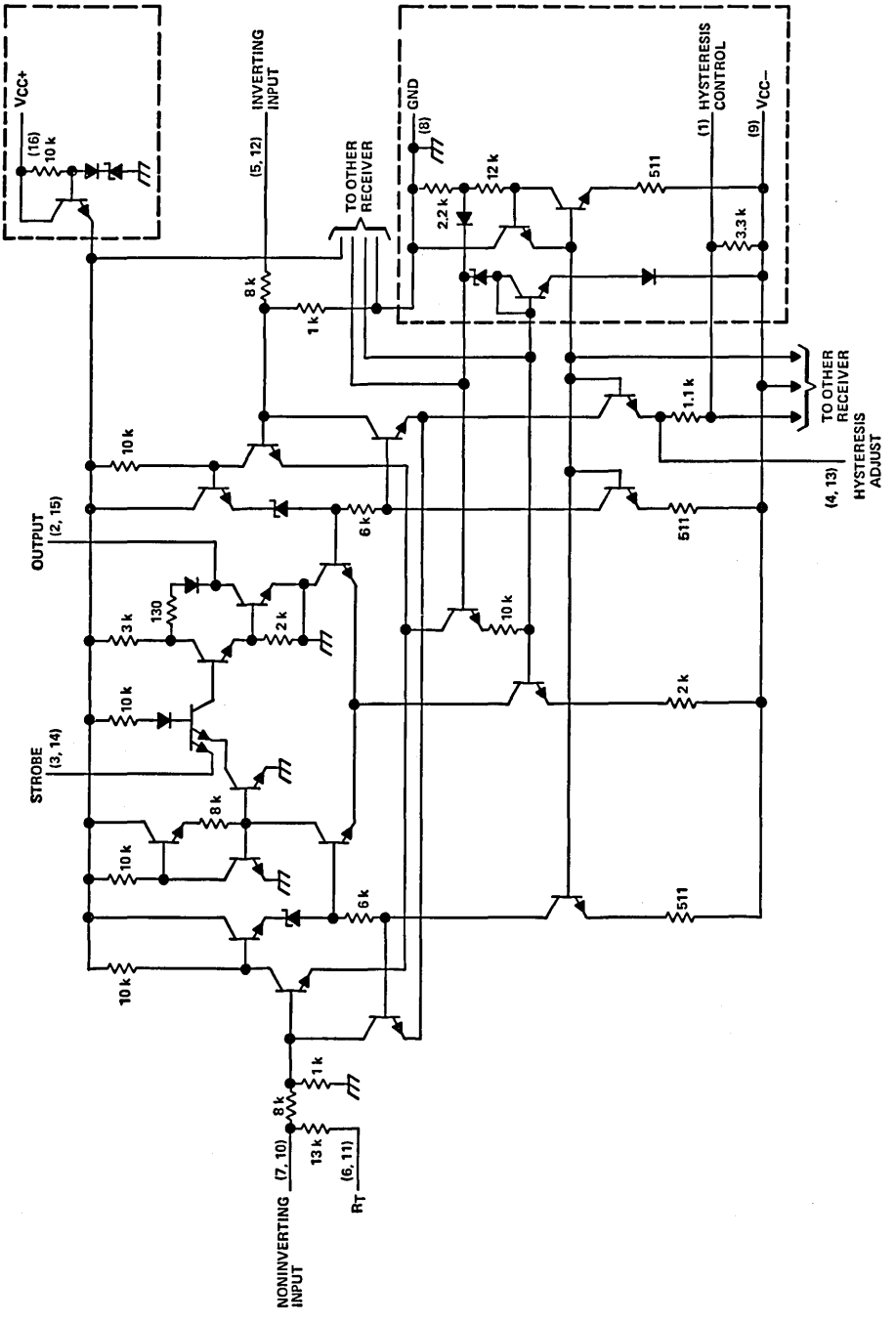
schematic (each receiver)



Portions of circuit within dashed lines are common to both receivers.
Resistor values shown are nominal and in ohms.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC+} (see Note 1)	15 V
Supply voltage V_{CC-} (see Note 1)	−15 V
Voltage at any line input with respect to other line input, ground, or R_T terminal	±25 V
R_T terminal voltage (see Note 1)	±25 V
Strobe input voltage (see Note 1)	5.5 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N package	260°C

NOTE 1: These voltage values are with respect to network ground terminal.

electrical characteristics over operating free-air temperature range, V_{CC+} = 12 V ± 10%, V_{CC-} = −12 V ± 10% (unless otherwise noted)

PARAMETER			TEST FIGURE	TEST CONDITIONS‡	MIN	TYP§	MAX (SEE NOTE 2)	UNIT
V_{T+}	Positive-going threshold voltage	See Figure 8 and Note 2	1	MIL-STD-188 Conditions	0.1	0.3	0.5	V
V_{T-}	Negative-going threshold voltage				−0.5	−0.3	−0.1	
V_{T+}	Positive-going threshold voltage		2	EIA RS-232-C Conditions	1.5	2.2	3	V
V_{T-}	Negative-going threshold voltage				−3	−2.2	−1.5	
V_{IH}	High-level input voltage at strobe		1		2			V
V_{IL}	Low-level input voltage at strobe		1				0.8	V
V_{OH}	High-level output voltage		1 and 2	V_{ID} = V_{T+} max, $V_{I(strobe)}$ = 2 V, I_{OH} = −500 μA	3	4.1	6	V
			1 and 2	V_{ID} = V_{T-} min, $V_{I(strobe)}$ = 0.8 V, I_{OH} = −500 μA	3	4.1	6	
V_{OL}	Low level output voltage		1 and 2	V_{ID} = V_{T-} min, $V_{I(strobe)}$ = 2 V, I_{OL} = 6.4 mA	0	0.15	0.4	V
I_I	Input current into strobe at maximum strobe voltage		3	$V_{I(strobe)}$ = 5.5 V		0.1	1	mA
I_{IH}	High-level strobe current		3	$V_{I(strobe)}$ = 2.4 V		30	80	μA
I_{IL}	Low-level strobe current		3	$V_{I(strobe)}$ = 0.4 V		−0.5	−1.5	mA
r_I	Input resistance	MIL-STD-188	4	$\|V_{ID}\|$ = 0 V to 25 V, R_T open	6	9		kΩ
		EIA RS-232-C	4	$\|V_{ID}\|$ = 3 V to 25 V, R_T connected to inverting line input	3	5	7	
$V_{I(open)}$	Open-circuit input voltage		5			+1	±2	V
I_{OS}	Short-circuit output current		6	V_{ID} = 3 V		−1.9	−4	mA
I_{CC+}	Supply current from V_{CC+}		1	V_{ID} = −3 V, $V_{I(strobe)}$ = 2.4 V		10	16	mA
I_{CC-}	Supply current from V_{CC-}		1	V_{ID} = −3 V, $V_{I(strobe)}$ = 2.4 V		−7	−13	mA

‡Differential input voltages (V_T and V_{ID}) are at the noninverting line input terminal with respect to the inverting line input terminal.

§Typical values are at V_{CC+} = 12 V, V_{CC-} = −12 V, T_A = 25°C.

NOTE 2: The algebraic convention, where the less-positive (more-negative) limit is designated as minimum, is used in this data sheet for threshold levels only, e.g., when −0.1 V is the maximum, the minimum limit is a more-negative voltage.

switching characteristics, V_{CC+} = 12 V, V_{CC-} = −12 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	7	C_L = 15 pF		40		ns
t_{PHL}	Propagation delay time, high-to-low-level output				60		ns

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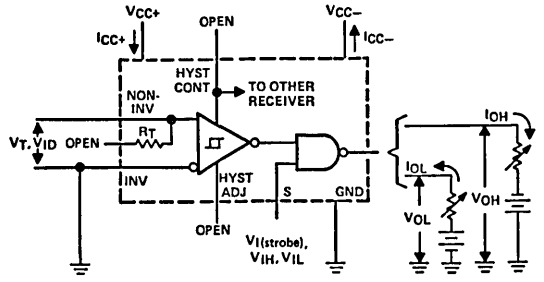
PARAMETER MEASUREMENT INFORMATION



NOTE: Output is open for testing I_{CC+} and I_{CC-}

FIGURE 1–MIL-STD-188 CONDITION

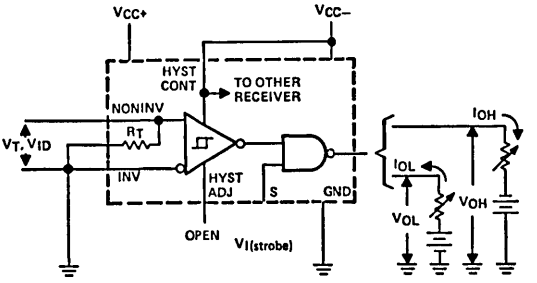


FIGURE 2–EIA RS-232-C CONDITION

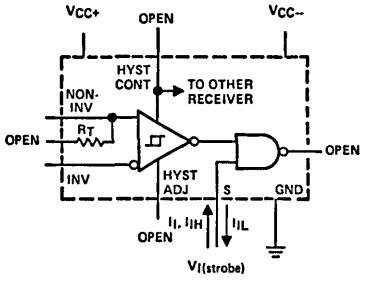


FIGURE 3

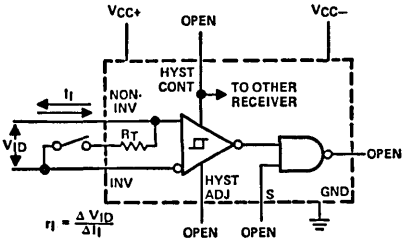


FIGURE 4

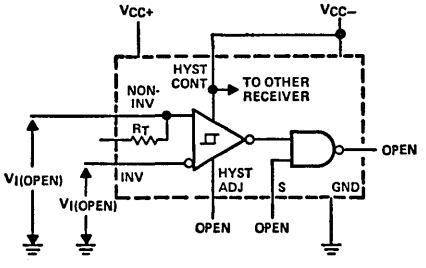


FIGURE 5

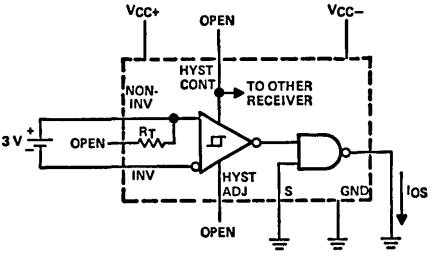
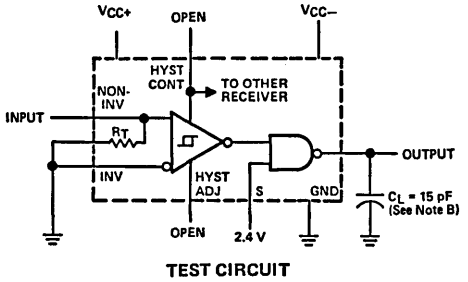
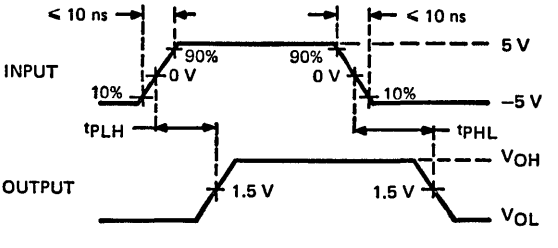


FIGURE 6



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: t_w = 500 ns, PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.

FIGURE 7–PROPAGATION DELAY TIMES

TYPICAL CHARACTERISTICS

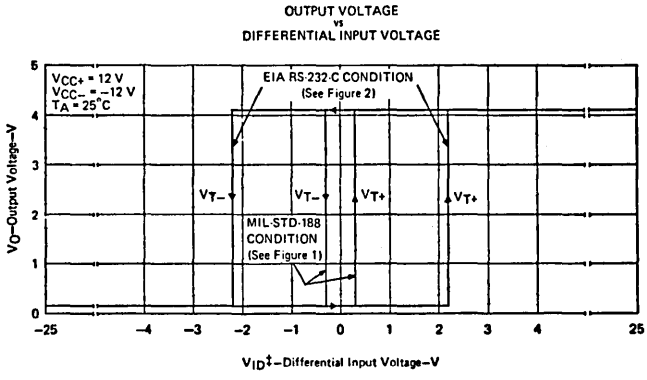


FIGURE 8

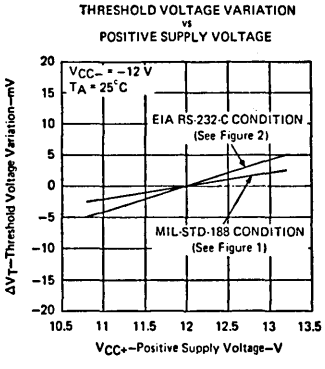


FIGURE 9

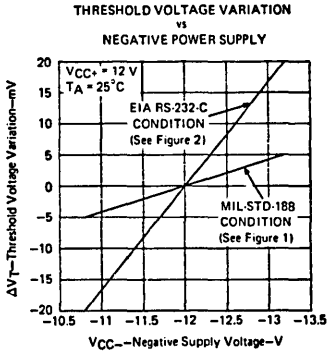


FIGURE 10

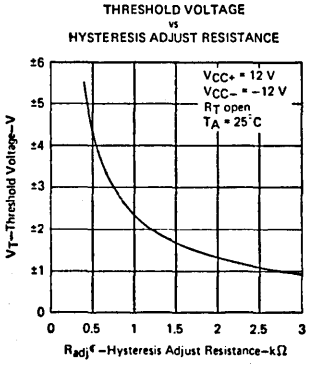


FIGURE 11

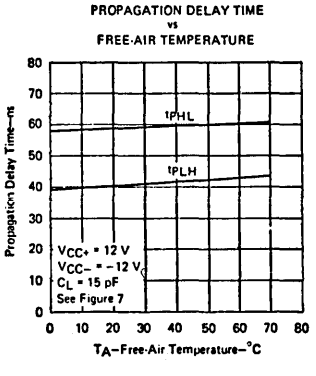


FIGURE 12

‡Differential input voltages (V_T and V_{ID}) are at the noninverting input terminal with respect to the inverting input terminal.
¶R_{adj} is connected between Hysteresis Adjust terminal and V_{CC-}.

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TYPICAL APPLICATIONS

Some typical applications of the SN75152 are as follows:

- MIL-STD-188 Interface Receiver
- EIA RS-232-C Interface Receiver
- Single-Ended Line Receiver
- Differential Line Receiver
- High-Noise-Immunity Line Receiver
- Schmitt Trigger
- High-Voltage-Logic-to-TTL Translator
- MOS to TTL Converter
- Pulse Generator
- Threshold detector
- Pulse Shaper

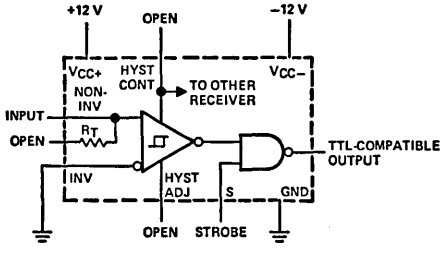
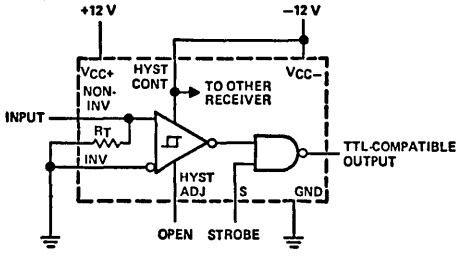
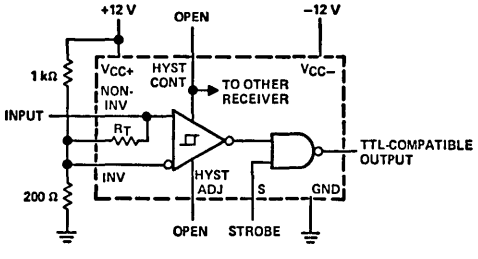


FIGURE 13—MIL-STD-188 SINGLE-ENDED LINE RECEIVER



NORMAL OPERATION



FAIL-SAFE OPERATION

FIGURE 14—EIA RS-232-C SINGLE-ENDED RECEIVER

TYPICAL APPLICATIONS

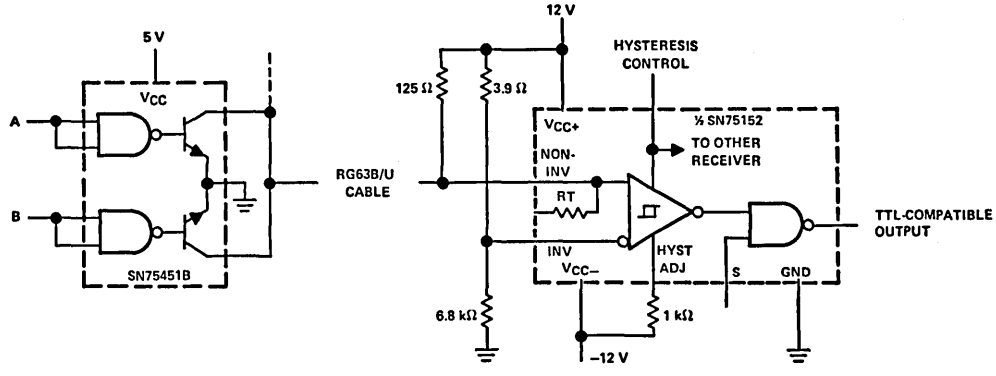
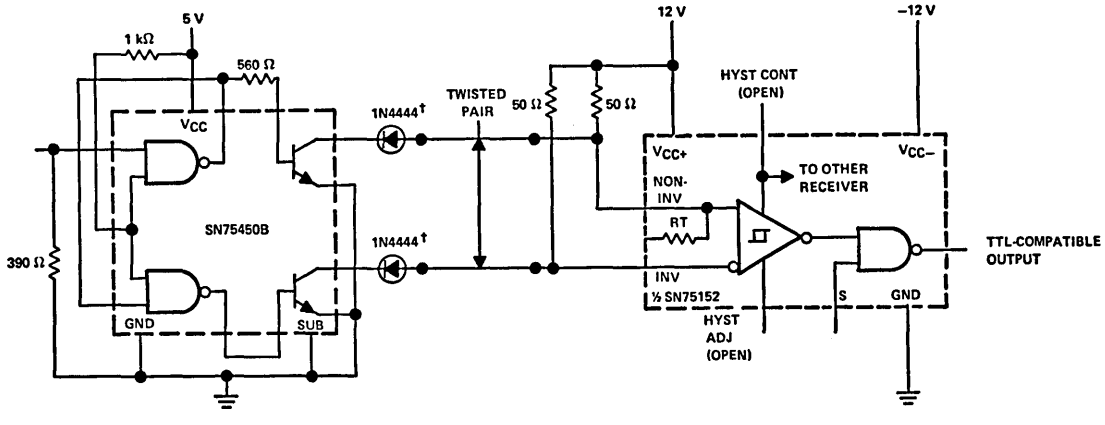


FIGURE 15–SINGLE-ENDED TRANSMITTER WITH DRIVER "OR" CAPABILITY AND RECEIVER WITH ADJUSTABLE NOISE IMMUNITY



Frequency to 0.5 MHz
Common-Mode Voltage . . . –12 V to +10 V

†The 1N4444 diodes are required only for negative common-mode protection at the driver outputs.

FIGURE 16–BALANCED LINE OPERATION WITH HIGH COMMON-MODE-VOLTAGE CAPABILITY

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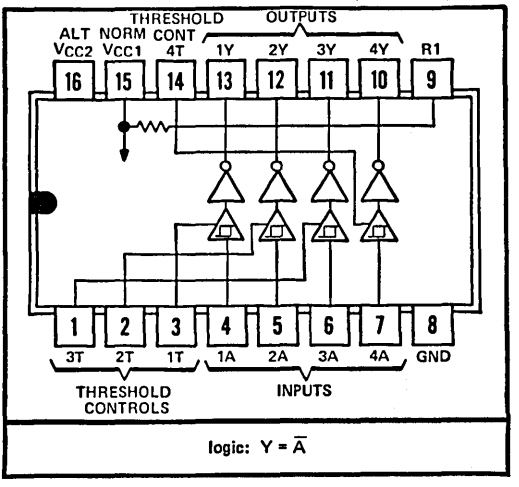
TYPE SN75154
QUADRUPLE LINE RECEIVER

BULLETIN NO. DL-S 11389, NOVEMBER 1970 – REVISED JANUARY 1977

- Satisfies Requirements of EIA Standard RS-232-C
- Input Resistance . . . 3 kΩ to 7 kΩ over Full RS-232-C Voltage Range
- Input Threshold Adjustable to Meet "Fail-Safe" Requirements Without Using External Components
- Built-In Hysteresis for Increased Noise Immunity
- Inverting Output Compatible with DTL or TTL
- Output with Active Pull-Up for Symmetrical Switching Speeds
- Standard Supply Voltages . . . 5 V or 12 V

J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)



description

The SN75154 is a monolithic quadruple line receiver designed to satisfy the requirements of the standard interface between data terminal equipment and data communication equipment as defined by EIA Standard RS-232C. Other applications are for relatively short, single-line, point-to-point data transmission and for level translators. Operation is normally from a single five-volt supply; however, a built-in option allows operation from a 12-volt supply without the use of additional components. The output is compatible with most TTL and DTL circuits when either supply voltage is used.

In normal operation, the threshold-control terminals are connected to the V_{CC1} terminal, pin 15, even if power is being supplied via the alternate V_{CC2} terminal, pin 16. This provides a wide hysteresis loop which is the difference between the positive-going and negative-going threshold voltages. See typical characteristics. In this mode of operation, if the input voltage goes to zero, the output voltage will remain at the low or high level as determined by the previous input.

For fail-safe operation, the threshold-control terminals are open. This reduces the hysteresis loop by causing the negative-going threshold voltage to be above zero. The positive-going threshold voltage remains above zero as it is unaffected by the disposition of the threshold terminals. In the fail-safe mode, if the input voltage goes to zero or an open-circuit condition, the output will go to the high level regardless of the previous input condition.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Normal supply voltage (pin 15), V_{CC1} (see Note 1)	7 V
Alternate supply voltage (pin 16), V_{CC2}	14 V
Input voltage	±25 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2): J package	1025 mW
N package	1150 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N package	260°C

NOTES: 1. Voltage values are with respect to the network ground terminal.
2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information Section, which starts on page 21. In the J package, SN75154 chips are glass-mounted.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Normal supply voltage (pin 15), V_{CC1}	4.5	5	5.5	V
Alternate supply voltage (pin 16), V_{CC2}	10.8	12	13.2	V
Input voltage			±15	V
Normalized fan-out from each output, N			10	
Operating free-air temperature, T_A	0		70	°C

REVISED JANUARY 1977

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST FIGURE	TEST CONDITIONS	MIN	TYP‡	MAX (SEE NOTE 3)	UNIT
V_{IH}	High-level input voltage		1		3			V
V_{IL}	Low-level input voltage		1				−3	V
V_{T+}	Positive-going threshold voltage	Normal operation	1		0.8	2.2	3	V
		Fail-safe operation			0.8	2.2	3	
V_{T-}	Negative-going threshold voltage	Normal operation	1		−3	−1.1	0	V
		Fail-safe operation			0.8	1.4	3	
$V_{T+}-V_{T-}$	Hysteresis	Normal operation	1		0.8	3.3	6	V
		Fail-safe operation			0	0.8	2.2	
V_{OH}	High-level output voltage		1	I_{OH} = −400 μA	2.4	3.5		V
V_{OL}	Low-level output voltage		1	I_{OL} = 16 mA		0.23	0.4	V
r_I	Input resistance		2	ΔV_I = −25 V to −14 V	3	5	7	kΩ
				ΔV_I = −14 V to −3 V	3	5	7	
				ΔV_I = −3 V to 3 V	3	6	8	
				ΔV_I = 3 V to 14 V	3	5	7	
				ΔV_I = 14 V to 25 V	3	5	7	
$V_{I(open)}$	Open-circuit input voltage		3	I_I = 0	0	0.2	2	V
I_{OS}	Short-circuit output current†		4	V_{CC1} = 5.5 V, V_I = −5 V	−10	−20	−40	mA
I_{CC1}	Supply current from V_{CC1}		5	V_{CC1} = 5.5 V, T_A = 25°C		20	35	mA
I_{CC2}	Supply current from V_{CC2}			V_{CC2} = 13.2 V, T_A = 25°C		23	40	

†Not more than one output should be shorted at a time.

‡ All typical values are at V_{CC1} = 5 V, T_A = 25°C.

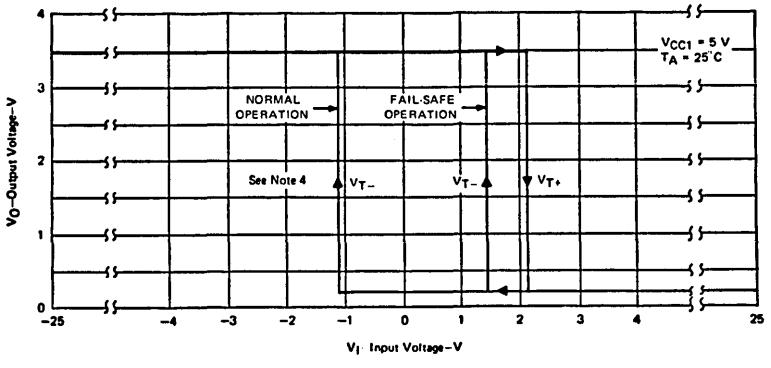
NOTE 3: The algebraic convention, where the less-positive (more-negative) limit is designated as minimum, is used in this data sheet for logic and threshold levels only, e.g., when 0 V is the maximum, the minimum limit is a more negative voltage.

switching characteristics, V_{CC1} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	6	C_L = 50 pF, R_L = 390 Ω		22		ns
t_{PHL}	Propagation delay time, high-to-low-level output				20		ns
t_{TLH}	Transition time, low-to-high-level output				9		ns
t_{THL}	Transition time, high-to-low-level output				6		ns

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE vs INPUT VOLTAGE



NOTE 4: For normal operation, the threshold controls are connected to V_{CC1}, pin 15. For fail-safe operation, the threshold controls are open.

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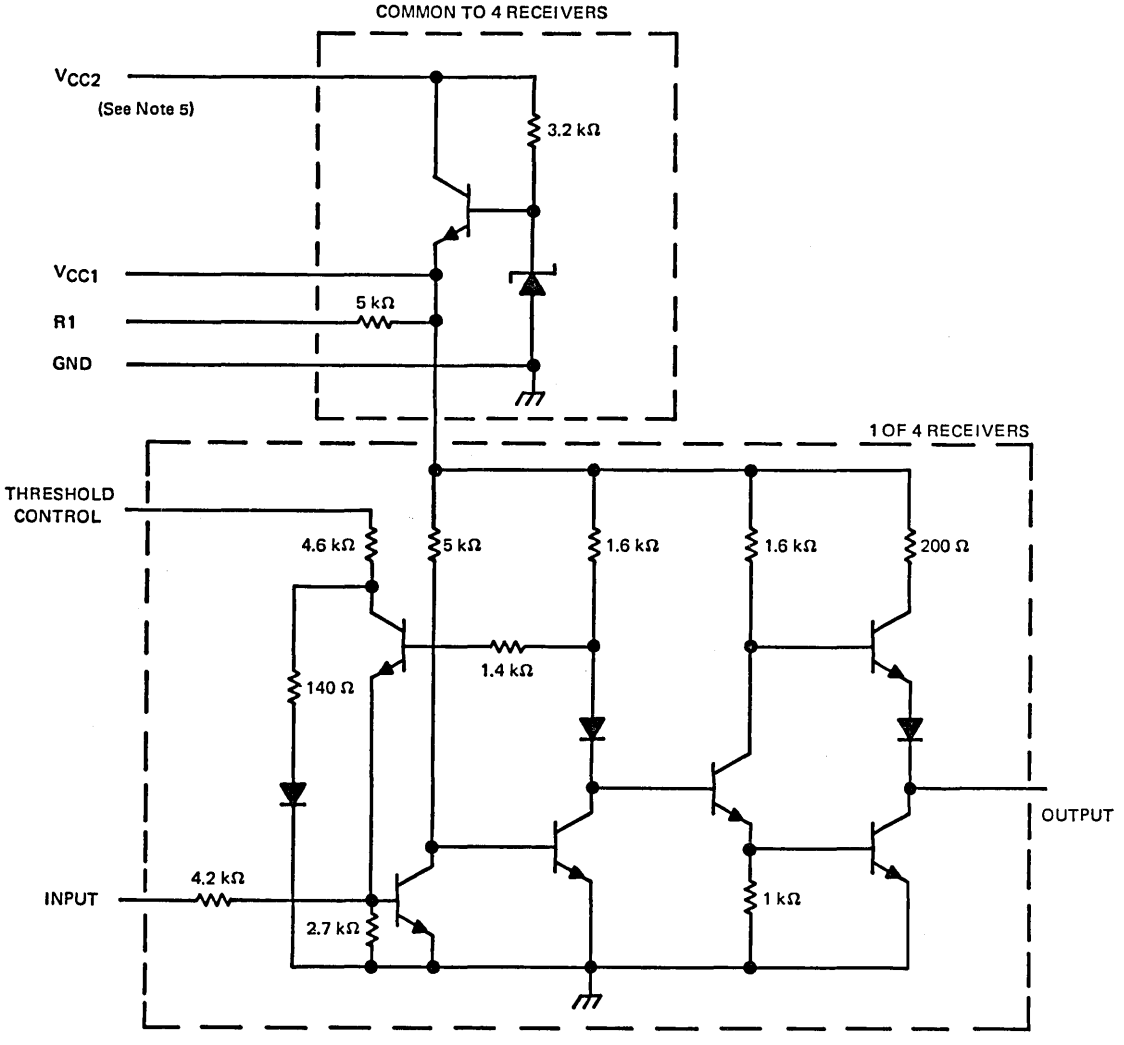
schematic



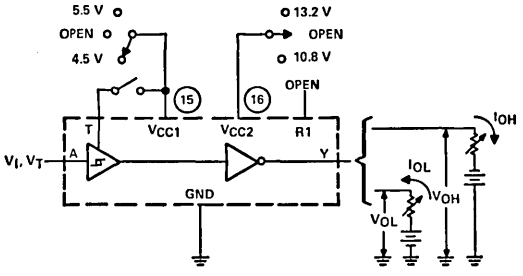
Component values shown are nominal

⏚ . . . Substrate

NOTE 5: When using V_{CC1} (pin 15), V_{CC2} (pin 16) may be left open or shorted to V_{CC1}. When using V_{CC2}, V_{CC1} must be left open or connected to the threshold control pins.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits†

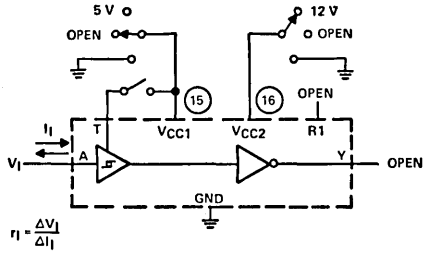


NOTES: A. Momentarily apply −5 V, then 0.8 V.
B. Momentarily apply 5 V, then ground.

TEST TABLE

TEST	MEASURE	A	T	Y	V_{CC1} (PIN 15)	V_{CC2} (PIN 16)
Open-circuit input (fail safe)	V_{OH}	Open	Open	I_{OH}	4.5 V	Open
	V_{OH}	Open	Open	I_{OH}	Open	10.8 V
V_{T+} min, V_{T-} min (fail safe)	V_{OH}	0.8 V	Open	I_{OH}	5.5 V	Open
	V_{OH}	0.8 V	Open	I_{OH}	Open	13.2 V
V_{T+} min (normal)	V_{OH}	Note A	Pin 15	I_{OH}	5.5 V and T	Open
	V_{OH}	Note A	Pin 15	I_{OH}	T	13.2 V
V_{IL} max, V_{T-} min (normal)	V_{OH}	−3 V	Pin 15	I_{OH}	5.5 V and T	Open
	V_{OH}	−3 V	Pin 15	I_{OH}	T	13.2 V
V_{IH} min, V_{T+} max, V_{T-} max (fail safe)	V_{OL}	3 V	Open	I_{OL}	4.5 V	Open
	V_{OL}	3 V	Open	I_{OL}	Open	10.8 V
V_{IH} min, V_{T+} max (normal)	V_{OL}	3 V	Pin 15	I_{OL}	4.5 V and T	Open
	V_{OL}	3 V	Pin 15	I_{OL}	T	10.8 V
V_{T-} max (normal)	V_{OL}	Note B	Pin 15	I_{OL}	5.5 V and T	Open
	V_{OL}	Note B	Pin 15	I_{OL}	T	13.2 V

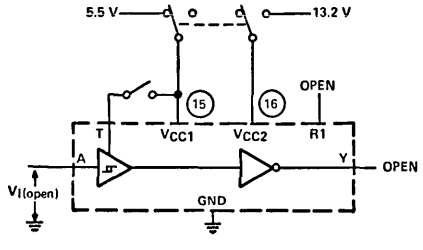
FIGURE 1 – V_{IH}, V_{IL}, V_{T+}, V_{T-}, V_{OH}, V_{OL}



TEST TABLE

T	V_{CC1} (PIN 15)	V_{CC2} (PIN 16)
Open	5 V	Open
Open	GND	Open
Open	Open	Open
Pin 15	T and 5 V	Open
GND	GND	Open
Open	Open	12 V
Open	Open	GND
Pin 15	T	12 V
Pin 15	T	GND
Pin 15	T	Open

FIGURE 2–r_I



TEST TABLE

T	V_{CC1} (PIN 15)	V_{CC2} (PIN 16)
Open	5.5 V	Open
Pin 15	5.5 V	Open
Open	Open	13.2 V
Pin 15	T	13.2 V

FIGURE 3–$V_{I(open)}$

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

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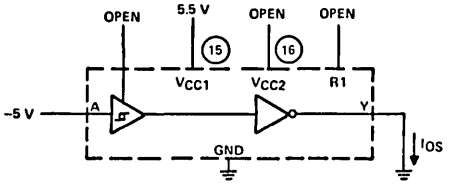
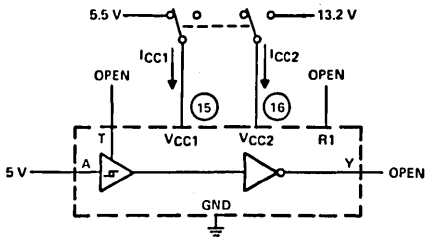
PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



Each output is tested separately.

FIGURE 4–I_{OS}

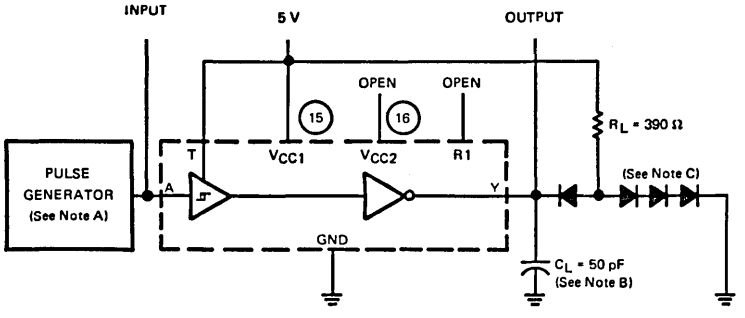


All four line receivers are tested simultaneously.

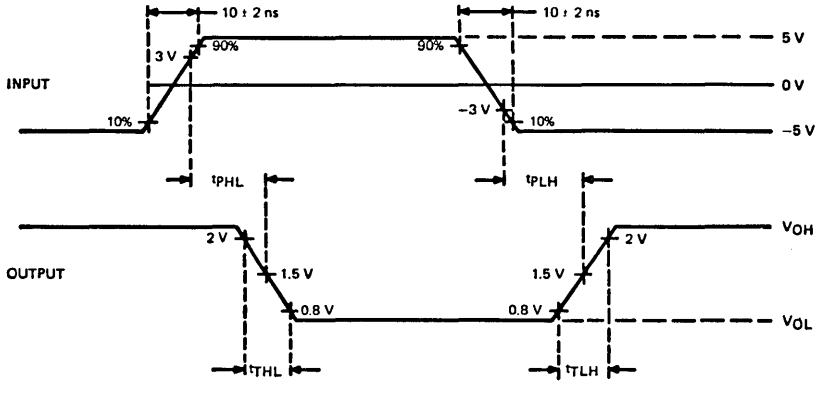
FIGURE 5–I_{CC}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: Z_{out} = 50 Ω, t_w = 200 ns, duty cycle ≤ 20%.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.

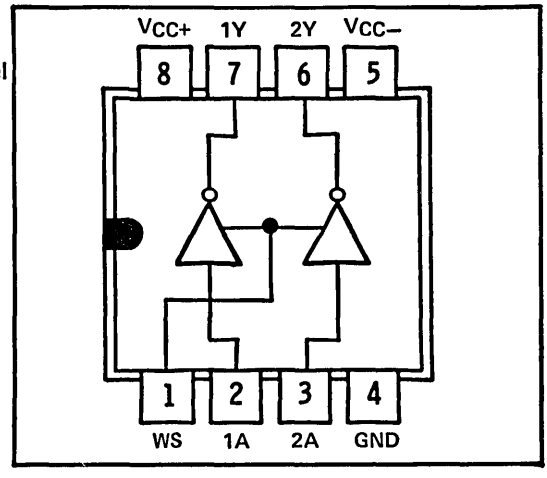
FIGURE 6–SWITCHING TIMES

TYPE SN75156
DUAL LINE DRIVER

OCTOBER 1980

- Meets EIA Standards RS-232C and RS-423A
- Wide Supply Voltage Range . . . ±7.5 V To ±15 V
- Low Supply Current . . . 4.5 mA Max per Channel
- Wave Shaping with External Resistor
- Inputs Compatible with TTL and CMOS
- Outputs at High Impedance when Power Is Off
- Positive- and Negative-Current Limiting
- Designed for Interchangeability with uA9636A
- Quad Version is SN75186

JG OR P PACKAGE
(TOP VIEW)



description

The SN75156 is a single-ended line driver designed to meet the requirements of EIA Standards RS-232C and RS-423A, CCITT Recommendations V.10, V.28, and X.26, and Federal Standard FIPS 1030. This device maintains regulated high and low output levels of 5.5 volts and –5.5 volts, respectively, over a wide range of power supply voltages. The output transition time for both drivers can be adjusted from 1 microsecond to 100 microseconds by means of an external resistor at the wave shaping (WS) pin. A high output impedance is maintained without the use of an external blocking diode.

PRODUCT PREVIEW

This document contains information on a product under development. Texas Instruments reserves the right to change or discontinue this product without notice.

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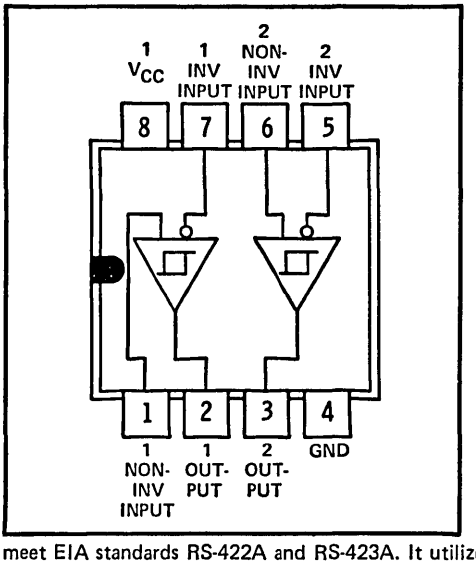
TYPE SN75157
DUAL DIFFERENTIAL LINE RECEIVER

BULLETIN NO. DL-S 12783, SEPTEMBER 1980

- Meets EIA Standards RS-422A and RS-423A
- Meets Federal Standards 1020 and 1030
- Operates from Single 5-V Power Supply
- Wide Common-Mode Voltage Range
- High Input Impedance
- TTL-Compatible Outputs
- High-Speed Schottky Circuitry
- 8-Pin Dual-In-Line Package
- Similar to uA9637AC But With Standard V_{CC} and Ground Pin Position

JG OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)



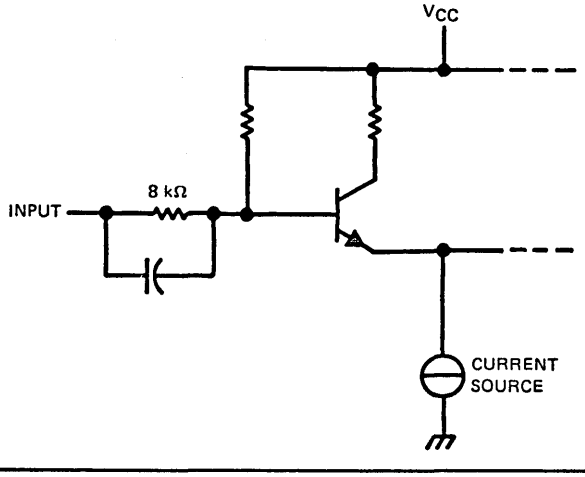
description

The SN75157 is a dual differential line receiver designed to meet EIA standards RS-422A and RS-423A. It utilizes Schottky† circuitry and has TTL-compatible outputs. The inputs are compatible with either a single-ended or a differential-line system. This device operates from a single 5-volt power supply and is supplied in an 8-pin dual-in-line package.

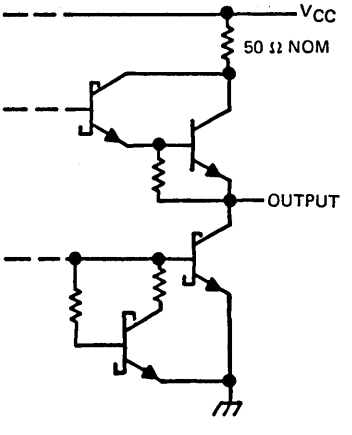
The SN75157 is characterized for operation from 0°C to 70°C.

schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



TYPICAL OF ALL OUTPUTS



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†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U.S. Patent Number 3,463,975.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC} (see Note 1) ..... −0.5 V to 7 V
Input voltage ..... ±15 V
Differential input voltage (see Note 2) ..... ±15 V
Output voltage (see Note 1) ..... −0.5 V to 5.5 V
Low-level output current ..... 50 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3):
JG package ..... 825 mA
P package ..... 1000 mA
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1/16 inch (1,6 mm) from case for 60 seconds: JG package ..... 300°C
Lead temperature 1/16 inch (1,6 mm) from case for 10 seconds: P package ..... 260°C

NOTES:
1. All voltage values, except differential-input voltage, are with respect to the network ground terminal.
2. Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.
3. For operation above 25°C free-air temperature, derate the JG package to 528 mW at 70°C at the rate of 6.6 mW/°C and the P package to 640 mW at 70°C at the rate of 8.0 mW. In the JG package, SN75157 chips are glass-mounted.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Common-mode input voltage, V_{IC}			±7	V
Operating free-air temperature, T_A	0	25	70	°C

electrical characteristics over recommended ranges of supply voltage, common-mode input voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
					See Note 4		
V_T	Threshold voltage (V_{T+} and V_{T-})			−0.2		0.2	V
		See Note 5		−0.4		0.4	
$V_{T+} - V_{T-}$	Hysteresis				70		mV
V_{OH}	High-level output voltage	V_{ID} = 0.2 V,	I_O = −1 mA	2.5	3.5		V
V_{OL}	Low-level output voltage	V_{ID} = −0.2 V,	I_O = 20 mA		0.35	0.5	V
I_I	Input current	V_{CC} = 0 to 5.5 V,	V_I = 10 V		1.1	3.25	mA
		See Note 6	V_I = −10 V		−1.6	−3.25	
I_{OS}	Short-circuit input current‡	V_O = 0,	V_{ID} = 0.2 V	−40	−75	−100	mA
I_{CC}	Supply current	V_{ID} = −0.5 V,	No load		35	50	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡Only one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTES:
4. The algebraic convention, where the less-positive (more-negative) limit is designated as minimum, is used in this data sheet for threshold levels only.
5. The expanded threshold parameter is tested with a 500-Ω resistor in series with each input.
6. The input not under test is grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 30 pF, See Figure 1		15	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output			13	25	ns

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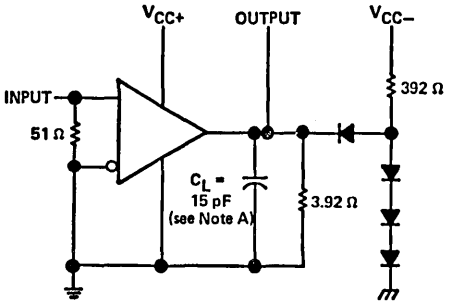
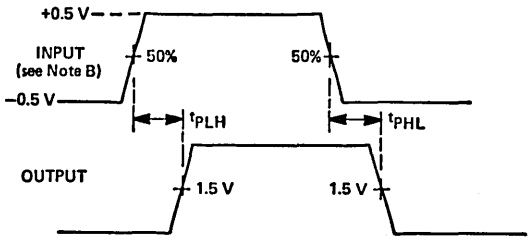
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORM

NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: t_r < 5 ns, t_f = 5 ns, PRR = 5 MHz, duty cycle = 10%.

FIGURE 1–TRANSITION TIMES

TYPICAL CHARACTERISTICS

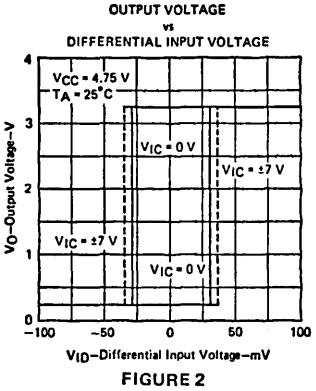


FIGURE 2

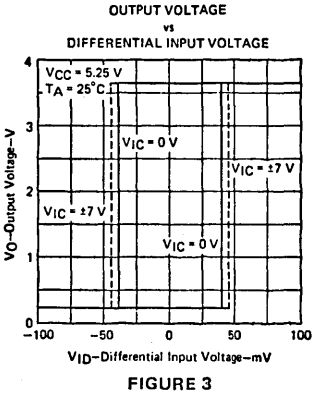


FIGURE 3

TYPICAL APPLICATION DATA

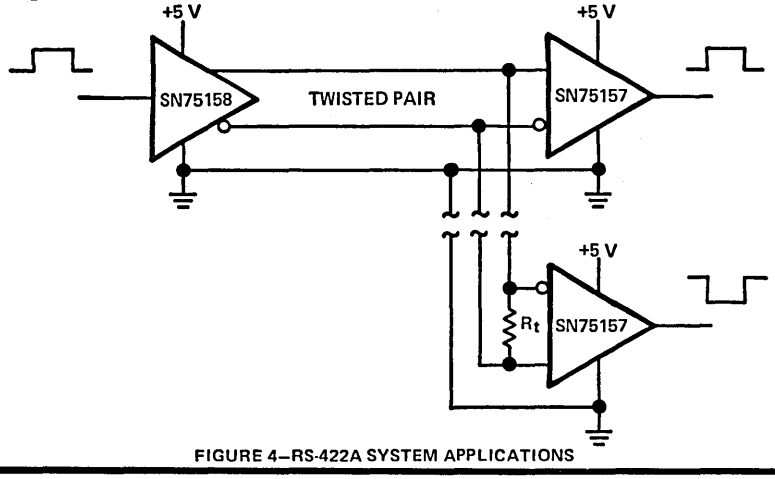


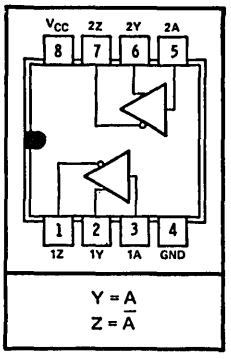
FIGURE 4–RS-422A SYSTEM APPLICATIONS

TYPES SN55158, SN75158 DUAL DIFFERENTIAL LINE DRIVERS

BULLETIN NO. DL-S 12497, JANUARY 1977

- Meets EIA Standard RS-422
- Single 5-V Supply
- Balanced-Line Operation
- TTL-, DTL-Compatible
- High Output Impedance in Power-Off Condition
- High-Current Active-Pull-Up Outputs
- Short-Circuit Protection
- Dual Channels
- Input Clamp Diodes

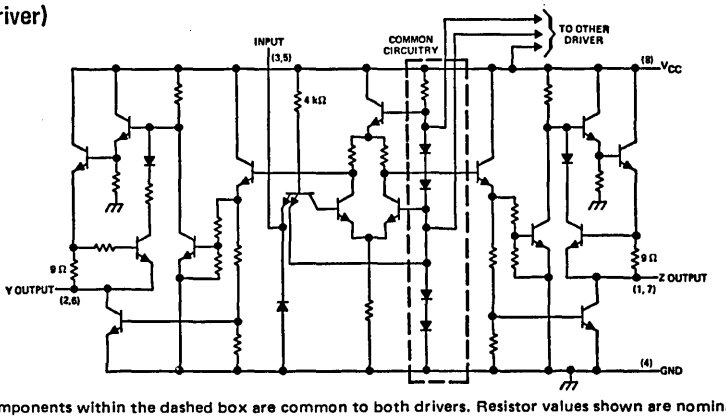
SN55158 . . . JG DUAL-IN-LINE PACKAGE
SN75158 . . . JG OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

The SN55158 and SN75158 are dual complementary-output line drivers designed to satisfy the requirements set by the EIA RS-422 standard interface specifications. The inputs are standard TTL. The outputs provide complementary signals with high-current capability for driving balanced lines, such as twisted-pair, at normal line impedance without high power dissipation. The output stages are TTL totem-pole outputs providing a high-impedance state in the power-off condition.

schematic (each driver)



Components within the dashed box are common to both drivers. Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2)	1 W
Operating free-air temperature range: SN55158	−55°C to 125°C
SN75158	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: JG package	300°C
Lead temperature 1/16 inch from case for 10 seconds: P package	260°C

NOTES: 1. All voltage values except, differential output voltage V_{OD}, are with respect to network ground terminal. V_{OD} is at the Y output with respect to the Z output.

2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 21. In the JG package, SN55158 chips are alloy-mounted; SN75158 chips are glass-mounted.

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recommended operating conditions

	SN55158			SN75158			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−40			−40	mA
Low-level output current, I_{OL}			40			40	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN55158			SN75158			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −12 mA		−0.9	−1.5		−0.9	−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V,	V_{IL} = 0.8 V, I_{OH} = −40 mA	2	3.0		2.4	3.0		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V,	V_{IL} = 0.8 V, I_{OL} = 40 mA		0.2	0.4		0.2	0.4	V
$\lvert V_{OD1}\rvert$	Differential output voltage	V_{CC} = MAX,	I_O = 0		3.5	$2V_{OD2}$		3.5	$2V_{OD2}$	V
$\lvert V_{OD2}\rvert$	Differential output voltage	V_{CC} = MIN	R_L = 100 Ω, See Figure 1	2	3.0		2	3.0		V
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of differential output voltage §	V_{CC} = MIN			±0.02	±0.4		±0.02	±0.4	V
V_{OC}	Common-mode output voltage ¶	V_{CC} = MAX			1.9	3		1.8	3	V
		V_{CC} = MIN			1.4	3		1.5	3	
$\Delta\lvert V_{OC}\rvert$	Change in magnitude of common-mode output voltage §	V_{CC} = MIN or MAX			±0.01	±0.4		±0.01	±0.4	V
I_O	Output current with power off	V_{CC} = 0	V_O = 6 V		0.1	100		0.1	100	µA
			V_O = −0.25 V		−0.1	−100		−0.1	−100	
			V_O = −0.25 V to 6 V			±100			±100	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4 V			40			40	µA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V		−1	−1.6		−1	−1.6	mA
I_{OS}	Short-circuit output current #	V_{CC} = MAX		−40	−90	−150	−40	−90	−150	mA
I_{CC}	Supply current (both drivers)	V_{CC} = MAX, No load,	Inputs grounded, T_A = 25°C		37	50		37	50	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V and T_A = 25°C except for V_{OC}, for which V_{CC} is as stated under test conditions.
§$\Delta\lvert V_{OD}\rvert$ and $\Delta\lvert V_{OC}\rvert$ are the changes in magnitudes of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
¶In EIA Standard RS-422, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.
#Only one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	SN55158			SN75158			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 2, Termination A		16	25		16	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output			10	20		10	20	ns
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 2, Termination B		13	20		13	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output			9	15		9	15	ns
t_{TLH}	Transition time, low-to-high-level output	See Figure 2, Termination A		4	20		4	20	ns
t_{THL}	Transition time, high-to-low-level output			4	20		4	20	ns
	Overshoot factor	See Figure 2, Termination C			10			10	%

PARAMETER MEASUREMENT INFORMATION

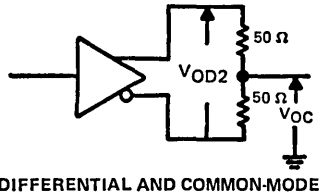
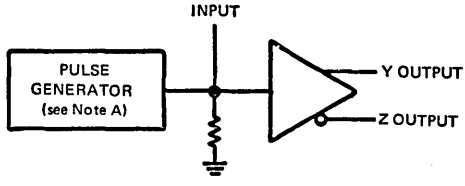
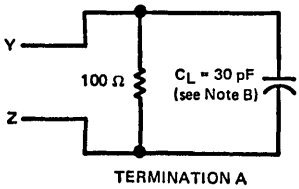
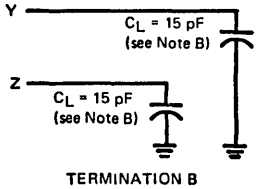


FIGURE 1–DIFFERENTIAL AND COMMON-MODE OUTPUT VOLTAGES

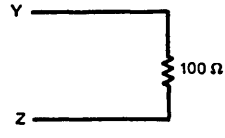




TERMINATION A

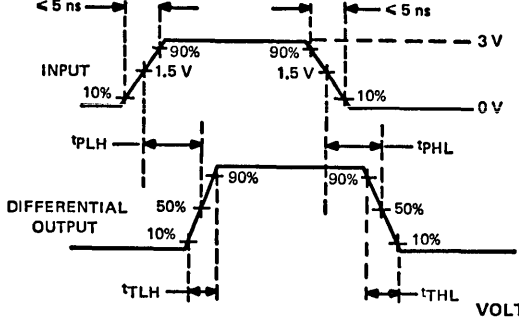


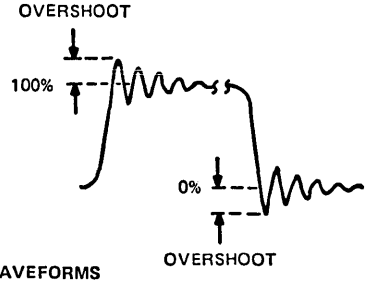
TERMINATION B



TERMINATION C

TEST CIRCUIT





VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: Z_{out} = 50 Ω, t_w = 25 ns, PRR = 10 MHz.
B. C_L includes probe and jig capacitance.

FIGURE 2–SWITCHING TIMES

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TYPICAL CHARACTERISTICS†

OUTPUT VOLTAGE vs DATA INPUT VOLTAGE

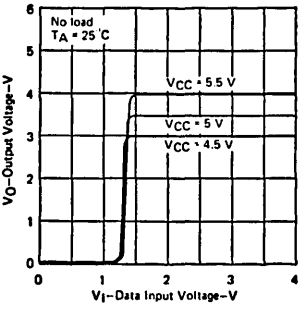


FIGURE 3

OUTPUT VOLTAGE vs DATA INPUT VOLTAGE

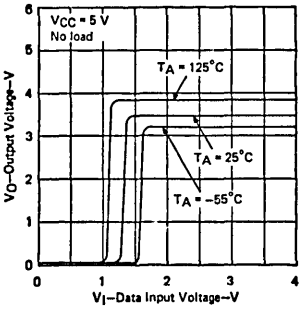


FIGURE 4

HIGH-LEVEL OUTPUT VOLTAGE vs OUTPUT CURRENT

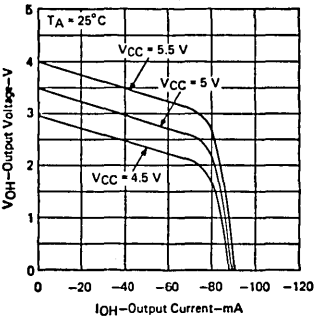


FIGURE 5

LOW-LEVEL OUTPUT VOLTAGE vs OUTPUT CURRENT

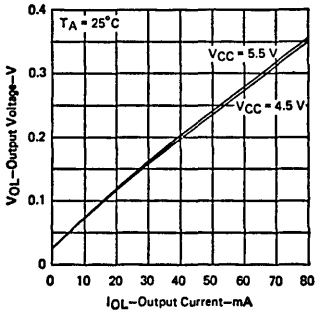


FIGURE 6

OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

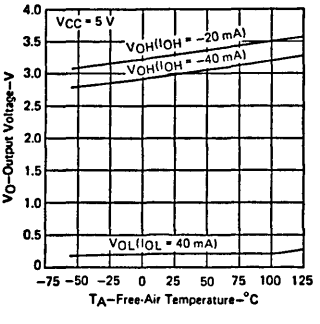


FIGURE 7

PROPAGATION DELAY TIMES vs FREE-AIR TEMPERATURE

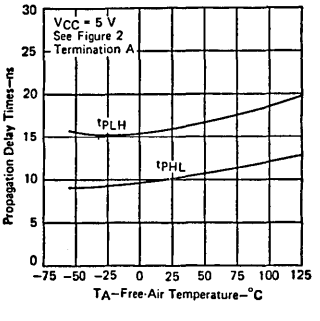


FIGURE 8

SUPPLY CURRENT (BOTH DRIVERS) vs SUPPLY VOLTAGE

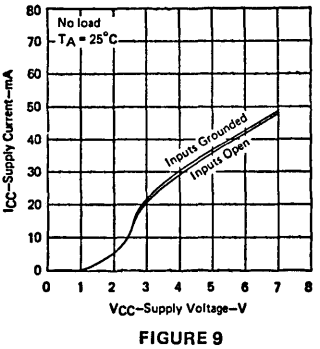


FIGURE 9

SUPPLY CURRENT (BOTH DRIVERS) vs FREE-AIR TEMPERATURE

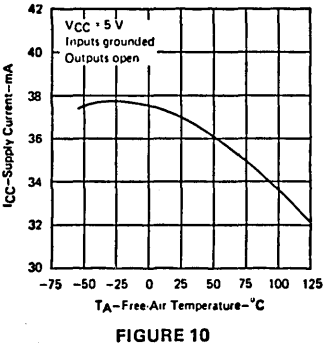


FIGURE 10

SUPPLY CURRENT (BOTH DRIVERS) vs FREQUENCY

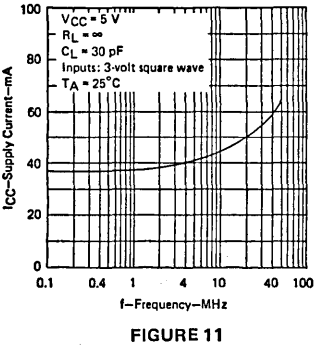


FIGURE 11

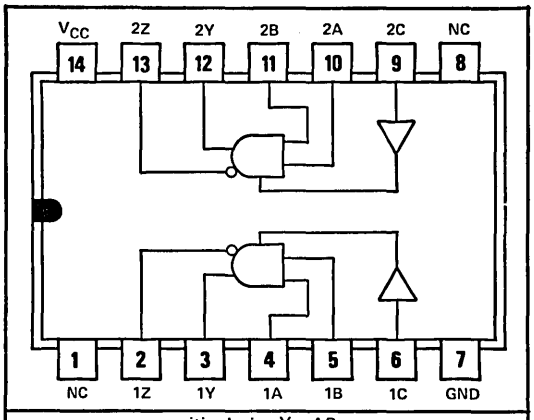
†Data for temperatures below 0°C and above 70°C are applicable to SN55158 circuits only.

TYPE SN75159
DUAL DIFFERENTIAL LINE DRIVER WITH 3-STATE OUTPUTS

BULLETIN NO. DL-S 12501, JANUARY 1977

- Meets EIA Standard RS-422
- Single 5-V Supply
- Balanced Line Operation
- TTL and DTL Compatible
- High-Impedance Output State for Party-Line Applications
- High-Current Active-Pull-Up Outputs
- Short-Circuit Protection
- Dual Channels
- Clamp Diodes at Inputs

J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



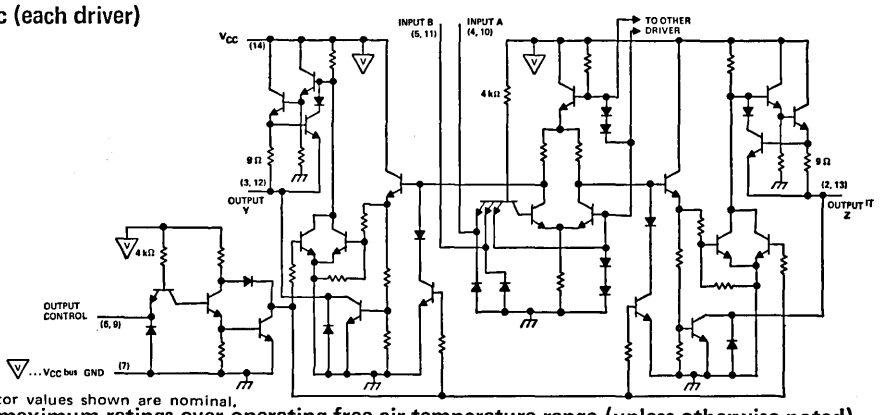
positive logic: $Y = AB$
$Z = \overline{AB}$
Outputs are off when C is low

NC—No internal connection

description

The SN75159 dual differential line driver with three-state outputs is designed to provide all the features of the SN75158 line driver with the added feature of driver output controls. There is an individual control for each driver. When the output control is low, the associated outputs are in a high-impedance state and the outputs can neither drive nor load the bus. This permits many devices to be connected together on the same transmission line for party-line applications.

schematic (each driver)



Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Off-state voltage applied to open-collector outputs	12 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2): J package	1025 mW
N package	1150 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N package	260°C

NOTES: 1. All voltage values, except differential output voltage V_{OD}, are with respect to network ground terminal. V_{OD} is at the Y output with respect to the Z output.

2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 21. In the J package, SN75159 chips are glass-mounted.

TEXAS INSTRUMENTS
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recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level output current, I_{OH}			−40	mA
Low-level output current, I_{OL}			40	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −12 mA			−0.9	−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V,	V_{IL} = 0.8 V, I_{OH} = −40 mA		2.4	3.0		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V,	V_{IL} = 0.8 V, I_{OL} = 40 mA			0.25	0.4	V
V_{OK}	Output clamp voltage	V_{CC} = MAX,	I_O = −40 mA			−1.1	−1.5	V
$\lvert V_{OD1}\rvert$	Differential output voltage	V_{CC} = MAX,	I_O = 0			3.5	$2V_{OD2}$	V
$\lvert V_{OD2}\rvert$	Differential output voltage	V_{CC} = MIN	R_L = 100 Ω,	See Figure 1	2	3.0		V
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of differential output voltage §	V_{CC} = MIN				±0.02	±0.4	V
V_{OC}	Common-mode output voltage ¶	V_{CC} = MAX				1.8	3	V
		V_{CC} = MIN				1.5	3	
$\Delta\lvert V_{OC}\rvert$	Change in magnitude of common-mode output voltage §	V_{CC} = MIN or MAX				±0.01	±0.4	V
I_O	Output current with power off	V_{CC} = 0	V_O = 6 V			0.1	100	μA
			V_O = −0.25 V			−0.1	−100	
			V_O = −0.25 V to 6 V				±100	
I_{OZ}	Off-state (high-impedance-state) output current	V_{CC} = MAX, Output controls at 0.8 V	T_A = 25°C,	V_O = 0 to V_{CC}			±10	μA
			T_A = 70°C	V_O = 0			−20	
				V_O = 0.4 V			±20	
				V_O = 2.4 V			±20	
				V_O = V_{CC}			20	
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4 V				40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			−1	−1.6	mA
I_{OS}	Short-circuit output current #	V_{CC} = MAX			−40	−90	−150	mA
I_{CC}	Supply current (both drivers)	V_{CC} = MAX, T_A = 25°C	Inputs grounded,	No load,		47	65	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V and T_A = 25°C except for V_{OC}, for which V_{CC} is as stated under test conditions.
§$\Delta\lvert V_{OD}\rvert$ and $\Delta\lvert V_{OC}\rvert$ are the changes in magnitudes of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
¶In EIA Standard RS-422, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.
#Only one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 30 pF,	R_L = 100 Ω,	See Figure 2,		16	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output	Termination A				11	20	ns
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF,	See Figure 2,	Termination B		13	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output					9	15	ns
t_{TLH}	Transition time, low-to-high-level output	C_L = 30 pF,	R_L = 100 Ω,	See Figure 2,		4	20	ns
t_{THL}	Transition time, high-to-low-level output	Termination A				4	20	ns
t_{PZH}	Output enable time to high level	C_L = 30 pF,	R_L = 180 Ω,	See Figure 3		7	20	ns
t_{PZL}	Output enable time to low level	C_L = 30 pF,	R_L = 250 Ω,	See Figure 4		14	40	ns
t_{PHZ}	Output disable time from high level	C_L = 30 pF,	R_L = 180 Ω,	See Figure 3		10	30	ns
t_{PLZ}	Output disable time from low level	C_L = 30 pF,	R_L = 250 Ω,	See Figure 4		17	35	ns
	Overshoot factor	R_L = 100 Ω,	See Figure 2,	Termination C			10	%

PARAMETER MEASUREMENT INFORMATION

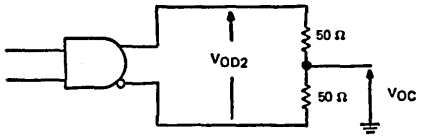
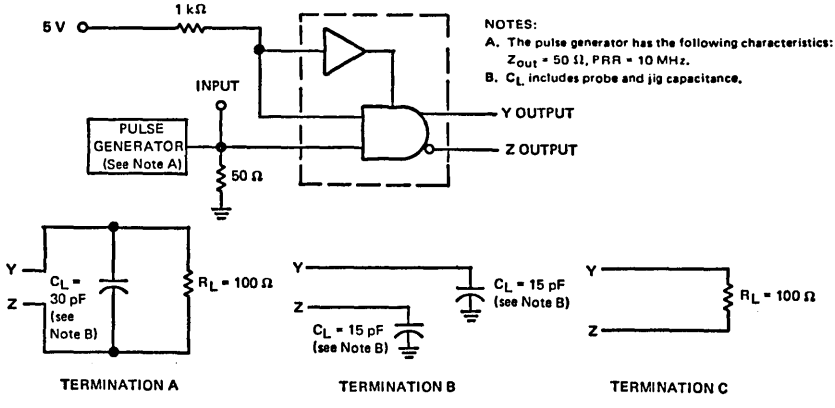
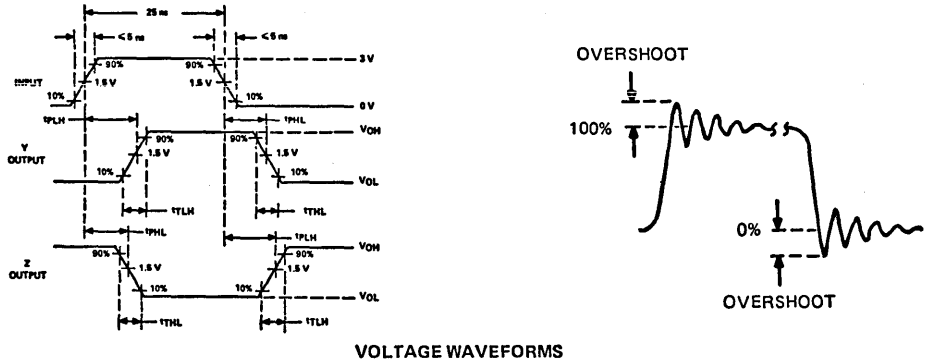


FIGURE 1–DIFFERENTIAL AND COMMON-MODE OUTPUT VOLTAGES



TEST CIRCUITS



VOLTAGE WAVEFORMS

FIGURE 2–t_{PLH}, t_{PHL}, t_{TLH}, t_{THL}, AND OVERSHOOT FACTOR

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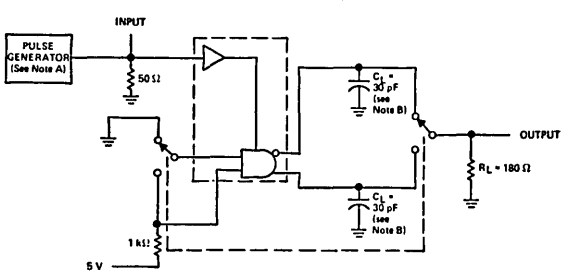
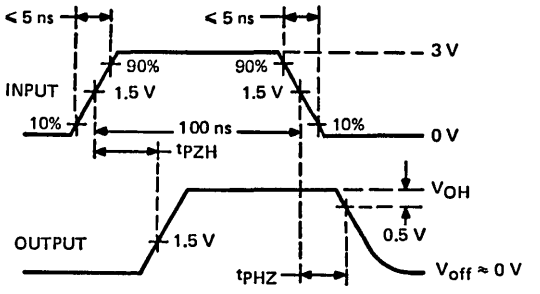
PARAMETER MEASUREMENT INFORMATION

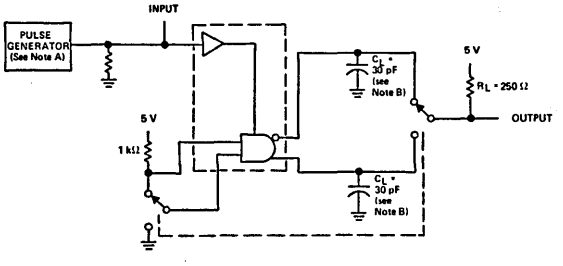


TEST CIRCUIT

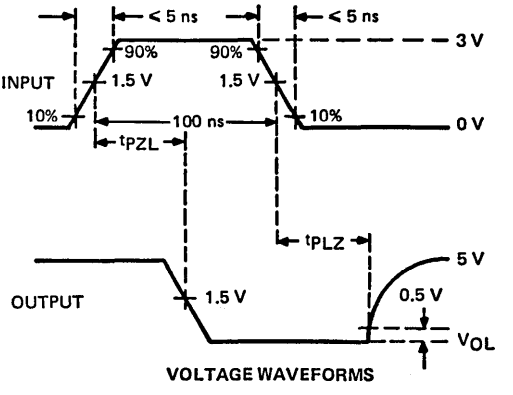


VOLTAGE WAVEFORMS

FIGURE 3–t_{PZH} AND t_{PHZ}



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 4–t_{PZL} AND t_{PLZ}

NOTES: A. The pulse generators have the following characteristics: Z_{out} = 50 Ω, PRR = 500 kHz
B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

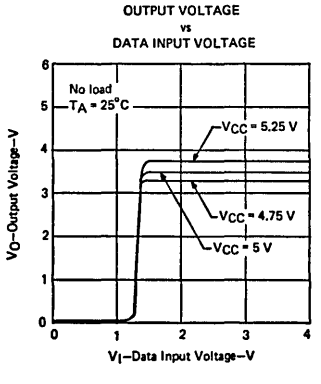


FIGURE 5

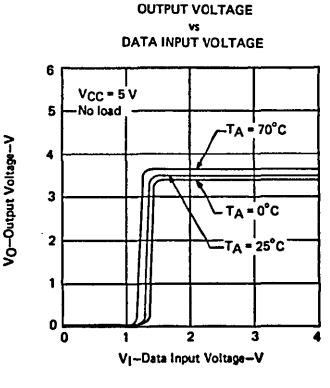


FIGURE 6

TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

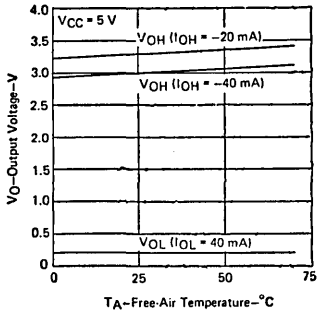


FIGURE 7

HIGH-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

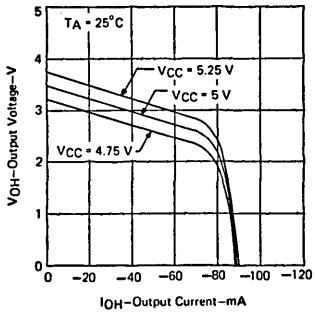


FIGURE 8

LOW-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

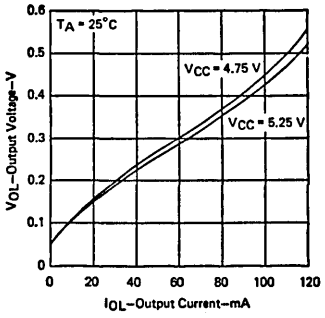


FIGURE 9

SUPPLY CURRENT
(BOTH DRIVERS)
vs
SUPPLY VOLTAGE

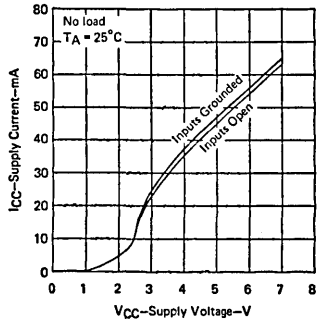


FIGURE 10

SUPPLY CURRENT
(BOTH DRIVERS)
vs
FREE-AIR TEMPERATURE

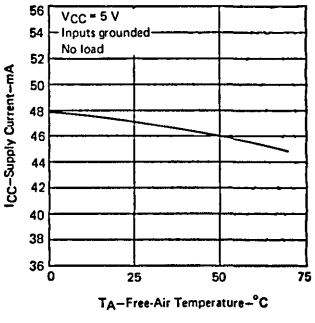


FIGURE 11

SUPPLY CURRENT
(BOTH DRIVERS)
vs
FREQUENCY

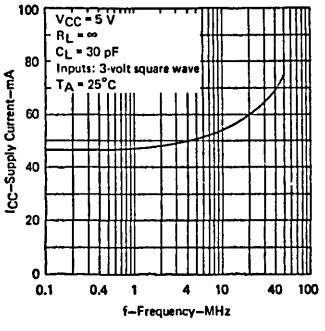


FIGURE 12

PROPAGATION DELAY TIMES
FROM DATA INPUTS
vs
FREE-AIR TEMPERATURE

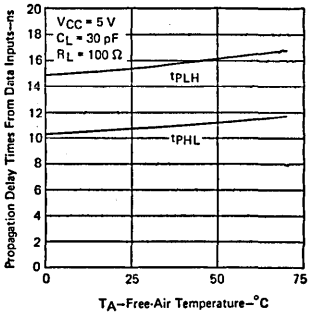


FIGURE 13

OUTPUT ENABLE and DISABLE TIMES
vs
FREE-AIR TEMPERATURE

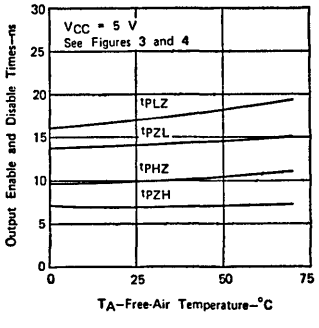


FIGURE 14

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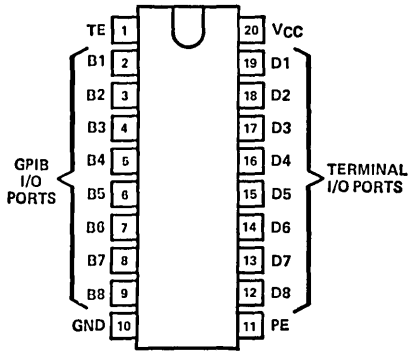
TYPE SN75160A OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVER

BULLETIN NO. DL-S 12786, OCTOBER 1980

MEETS IEEE STANDARD 488-1978 (GPIB)

- 8-Channel Bidirectional Transceiver
- High-Speed, Low-Power Schottky Circuitry†
- Low Power Dissipation . . . 66 mW Max per Channel
- Fast Propagation Times . . . 22 ns Max
- High-Impedance P-N-P Inputs
- Receiver Hysteresis . . . 650 mV Typ
- Open-Collector Driver Output Option
- No Loading of Bus When Device is Powered Down (V_{CC} = 0 V)

J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)

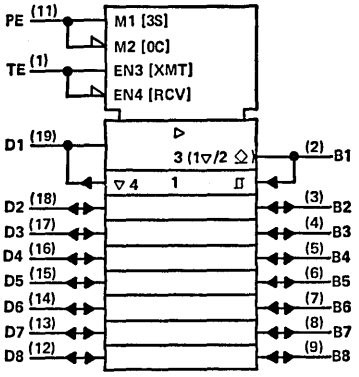


description

The SN75160A 8-channel general-purpose interface bus transceiver is a monolithic, high-speed, low-power Schottky device designed for two-way data communications over single-ended transmission lines. It is designed to meet the requirements of IEEE Standard 488-1978. The transceiver features driver outputs that can be operated in either the open-collector or three-state mode. If Talk Enable (TE) is high, these ports have the characteristics of open-collector outputs when Pull-up Enable (PE) is low, and of three-state outputs when PE is high. Taking TE low places these ports in the high-impedance state. The driver outputs are designed to handle loads up to 48 milliamperes of sink current.

An active-turn-off feature has been incorporated into the bus-terminating resistors so that the device exhibits a high-impedance to the bus when V_{CC} = 0 volts. When combined with the SN75161A or SN75162A management bus transceivers, the pair provides the complete 16-wire interface for the IEEE 488 bus.

logic symbol‡



‡This symbol is in accordance with IEEE Std 91/ANSI Y32.14 and current discussions in IEC and IEEE.

FUNCTION TABLES

DRIVERS

INPUTS			OUTPUT
D	TE	PE	B
H	H	H	H
L	H	X	L
H	X	L	Z*
X	L	X	Z*

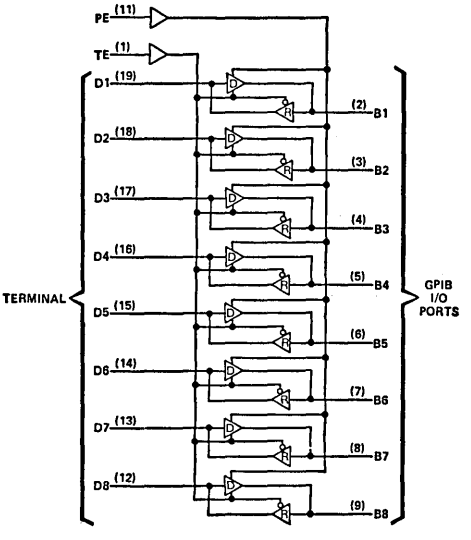
RECEIVERS

INPUTS			OUTPUTS
B	TE	PE	D
L	L	X	L
H	L	X	H
X	H	X	Z

H = high level, L = low level, X = irrelevant, Z = High-impedance state.

*This is the high-impedance state of a normal 3-state output modified by the internal resistors to V_{CC} and ground.

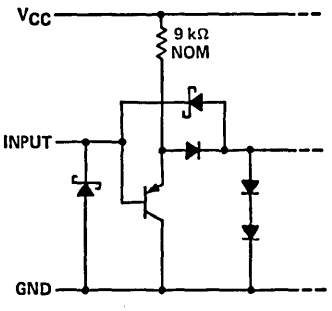
functional block diagram (positive logic)



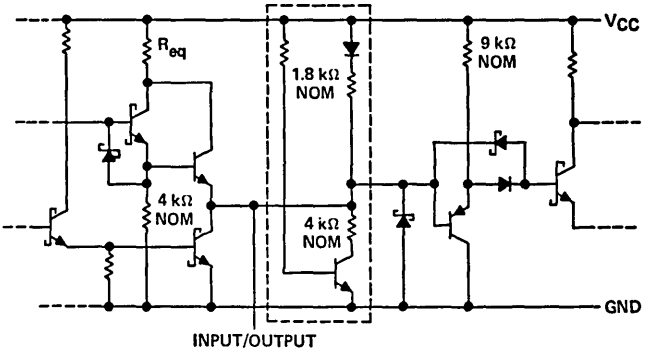
†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U.S. Patent Number 3,463,975.

schematics of inputs and outputs

EQUIVALENT OF ALL CONTROL INPUTS



EQUIVALENT OF ALL INPUT/OUTPUT PORTS



Driver output R_{eq} = 30 Ω NOM
Receiver output R_{eq} = 110 Ω NOM
Circuit inside dashed lines is on the driver outputs only.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Low-level driver output current	100 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2): J package	1375 mW
N package	1150 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 (1,6 mm) from case for 10 seconds	260°C

NOTES: 1. All voltage values are with respect to network ground terminal.

2. For operation above 25°C free-air temperature, derate the J package to 880 mW at 70°C at the rate of 11 mW/°C and derate the N package to 736 mW at 70°C at the rate of 9.2 mW/°C. In the J package, SN75160A chips are alloy-mounted.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level output current, I_{OH}	Bus ports with pull-ups active			−5.2	mA
	Terminal ports			−800	μA
Low-level output current, I_{OL}	Bus ports			48	mA
	Terminal ports			16	
Operating free-air temperature, T_A		0		70	°C

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electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

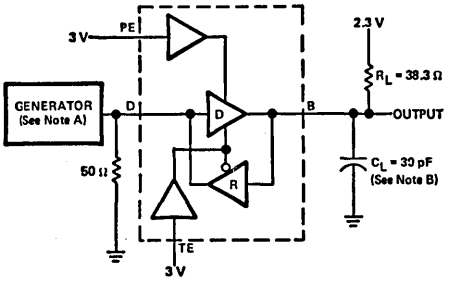
PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage		I_I = −18 mA			−0.8	−1.5	V
$V_{T+} - V_{T-}$	Hysteresis‡	Bus			0.4	0.65		V
V_{OH}	High level output voltage	Terminal	I_{OH} = −800 μA,	TE at 0.8 V	2.7	3.5		V
		Bus	I_{OH} = −5.2 mA,	PE and TE at 2 V	2.5	3.3		
V_{OL}	Low-level output voltage	Terminal	I_{OL} = 16 mA,	TE at 0.8 V		0.3	0.5	V
		Bus	I_{OL} = 48 mA,	TE at 2 V		0.4	0.5	
I_I	Input current at maximum input voltage	Terminal	V_I = 5.5 V			0.2	100	μA
I_{IH}	High-level input current	Terminal	V_I = 2.7 V			0.1	20	μA
I_{IL}	Low-level input current	Terminal	V_I = 0.5 V			−10	−100	μA
$V_{I/O(bus)}$	Voltage at bus port		Driver disabled	$I_{I(bus)}$ = 0	2.5	3.0	3.7	V
				$I_{I(bus)}$ = −12 mA			−1.5	
$I_{I/O(bus)}$	Current into bus port	Power on	Driver disabled	$V_{I(bus)}$ = −1.5 V to 0.4 V	−1.3			mA
				$V_{I(bus)}$ = 0.4 V to 2.5 V	0		−3.2	
				$V_{I(bus)}$ = 2.5 V to 3.7 V			+2.5 −3.2	
				$V_{I(bus)}$ = 3.7 V to 5 V	0		2.5	
				$V_{I(bus)}$ = 5 V to 5.5 V	0.7		2.5	
		Power off	V_{CC} = 0,	$V_{I(bus)}$ = 0 V to 2.5 V			−40	μA
I_{OS}	Short-circuit output current	Terminal			−15	−35	−75	mA
		Bus			−25	−50	−125	
I_{CC}	Supply current		No load	Receivers low and enabled		60	80	mA
				Drivers low and enabled		75	100	
$C_{i/o(bus)}$	Bus-port capacitance		V_{CC} = 5 V or 0 V,	$V_{I/O}$ = 0 to 2 V, f = 1 MHz		30		pF

†All typical values are at V_{CC} = 5, T_A = 25°C.
‡Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}. See Figure 8.

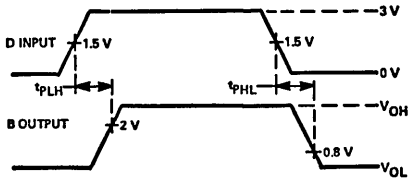
switching characteristics, V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C (unless otherwise noted)

PARAMETER		FROM	TO	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	Terminal	Bus	C_L = 30 pF, R_L = 38.3 Ω to 2.3 V, See Figure 1		14	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output					14	20	
t_{PLH}	Propagation delay time, low-to-high-level output	Bus	Terminal	C_L = 30 pF, R_L = 240 Ω to 5 V, See Figure 2		12	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output					16	22	
t_{PZH}	Output enable time to high level	TE	Bus	R_L = 480 Ω to 0 V, See Figure 3		25	35	ns
t_{PHZ}	Output disable time from high level					13	22	
t_{PZL}	Output enable time to low level			R_L = 38.3 Ω to 2.3 V, See Figure 3		22	35	
t_{PLZ}	Output disable time from low level					22	32	
t_{PZH}	Output enable time to high level	TE	Terminal	R_L = 3 kΩ to 0 V, See Figure 4		20	30	ns
t_{PHZ}	Output disable time from high level					12	20	
t_{PZL}	Output enable time to low level			R_L = 280 Ω to 5 V, See Figure 4		23	32	
t_{PLZ}	Output disable time from low level					19	30	
t_{en}	Output pull-up enable time	PE	Bus	R_L = 480 Ω to 0 V, See Figure 5		15	22	ns
t_{dis}	Output pull-up disable time					13	20	

PARAMETER MEASUREMENT INFORMATION

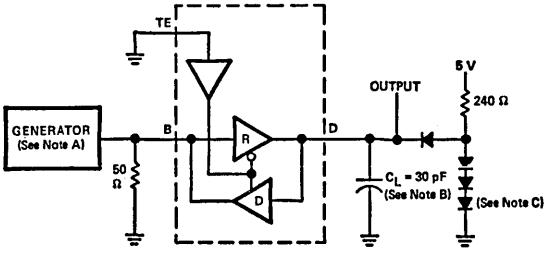


TEST CIRCUIT

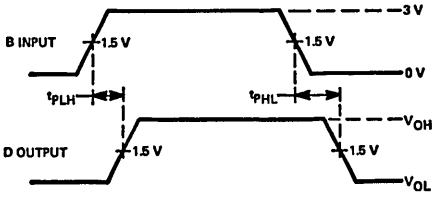


VOLTAGE WAVEFORMS

FIGURE 1–TERMINAL-TO-BUS PROPAGATION DELAY TIMES

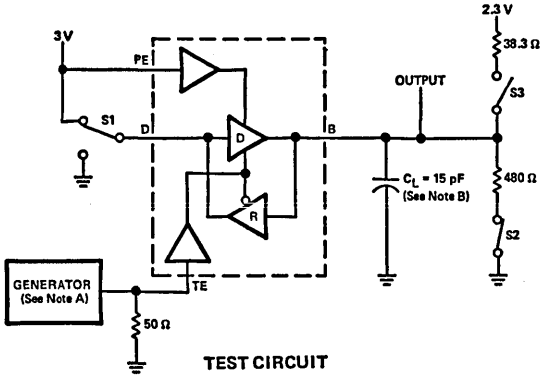


TEST CIRCUIT

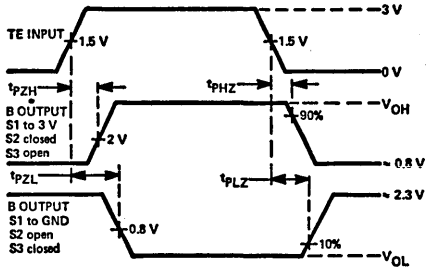


VOLTAGE WAVEFORMS

FIGURE 2–BUS-TO-TERMINAL PROPAGATION DELAY TIMES



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 3–TE-TO-BUS ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_{out} = 50\ \Omega$.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916 or equivalent.

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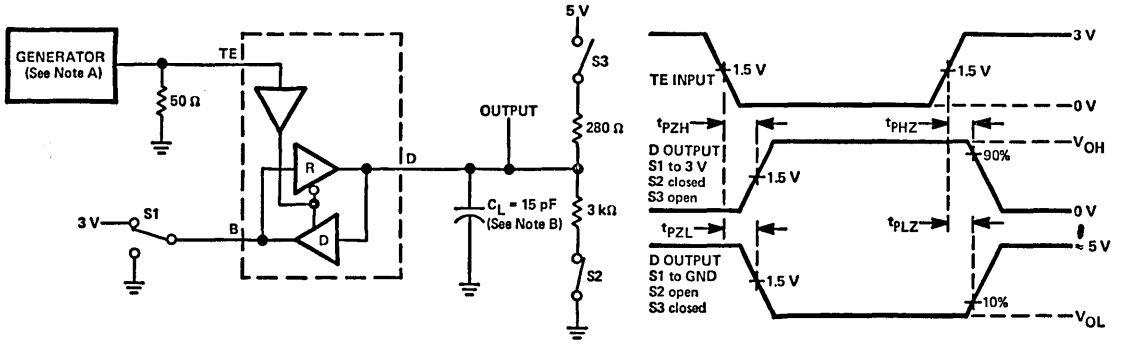
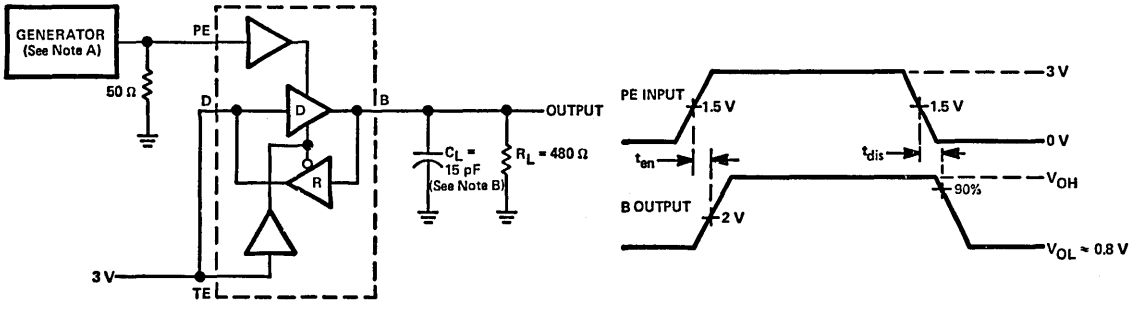
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

FIGURE 4—TE-TO-TERMINAL ENABLE AND DISABLE TIMES



TEST CIRCUIT VOLTAGE WAVEFORMS

FIGURE 5—PE-TO-BUS PULL-UP ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_{out} = 50\ \Omega$.

B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

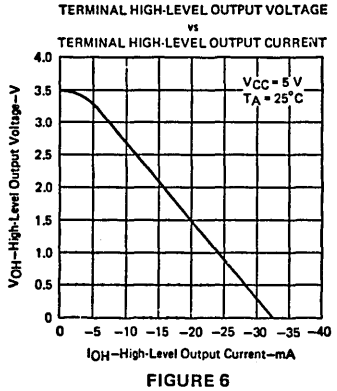


FIGURE 6

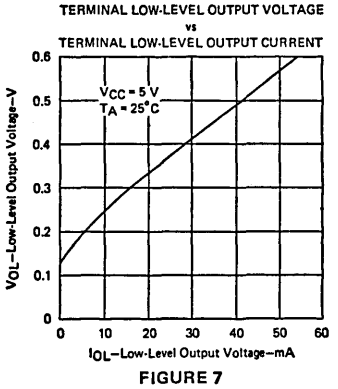


FIGURE 7

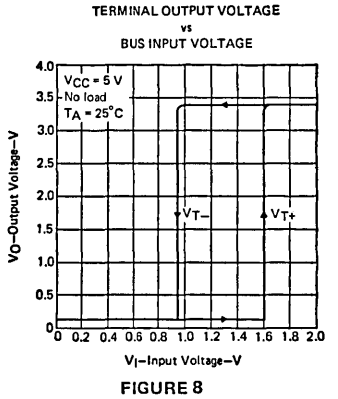


FIGURE 8

TYPICAL CHARACTERISTICS

BUS HIGH-LEVEL OUTPUT VOLTAGE
vs
BUS HIGH-LEVEL OUTPUT CURRENT

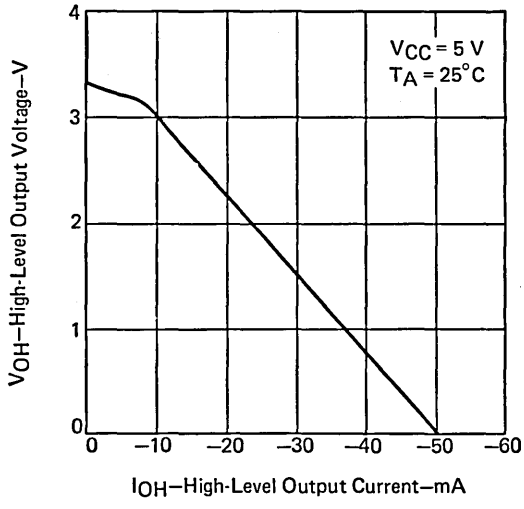


FIGURE 9

BUS LOW-LEVEL OUTPUT VOLTAGE
vs
BUS LOW-LEVEL OUTPUT CURRENT

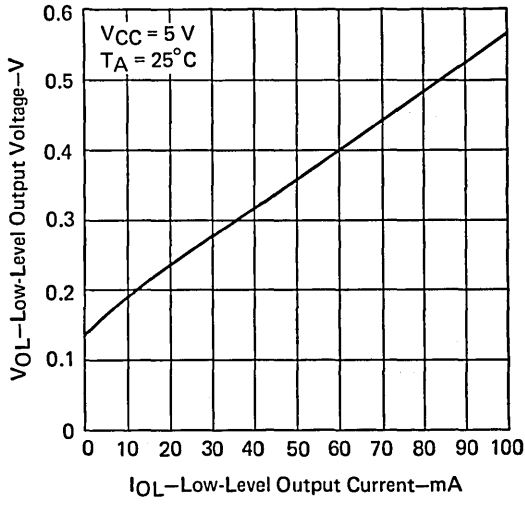


FIGURE 10

BUS OUTPUT VOLTAGE
vs
TERMINAL INPUT VOLTAGE

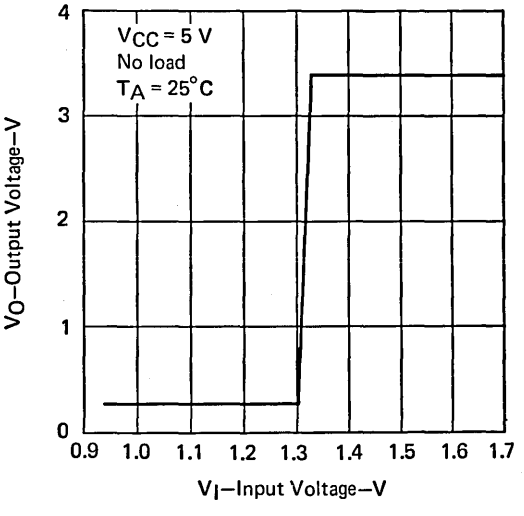


FIGURE 11

BUS CURRENT
vs
BUS VOLTAGE

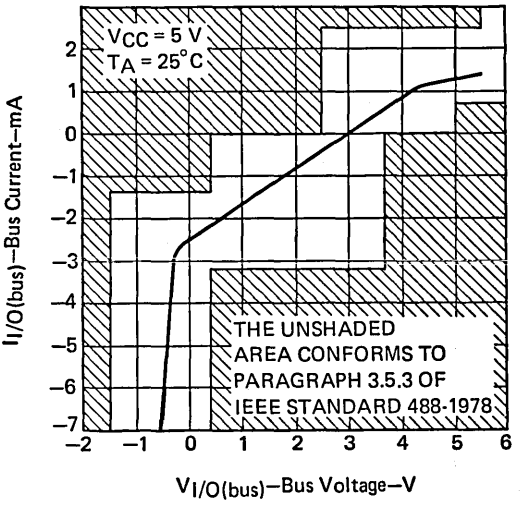


FIGURE 12

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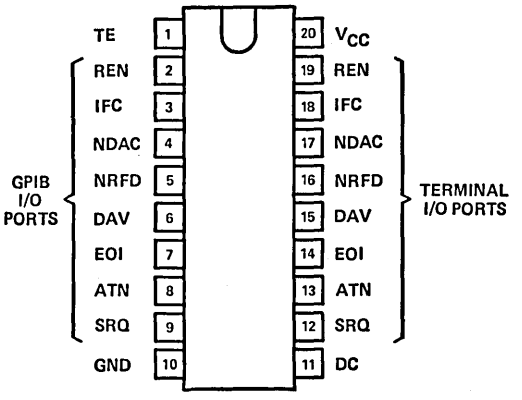
TYPES SN75161A, SN75162A OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVERS

BULLETIN NO. DL-S 12787, OCTOBER 1980

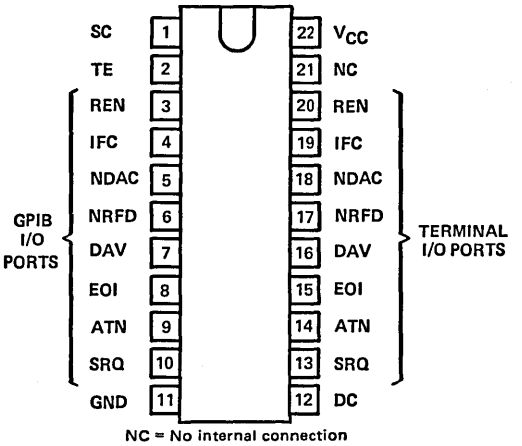
MEETS IEEE STANDARD 488-1978 (GPIB)

- 8-Channel Bidirectional Transceiver
- Designed to Implement Control Bus Interface
- SN75161A Designed for Single Controller
- SN75162A Designed for Multi-Controllers
- High-Speed, Low-Power Schottky Circuitry†
- Low Power Dissipation . . . 65 mW Max Per Channel
- Fast Propagation Times . . . 22 ns Max
- High-Impedance P-N-P Inputs
- Receiver Hysteresis . . . 650 mV Typ
- Bus-Terminating Resistors Provided on Driver Outputs
- No Loading of Bus when Device is Powered Down (V_{CC} = 0 V)

SN75161A . . . J or N
DUAL-IN-LINE PACKAGE
(TOP VIEW)



SN75162A . . . J OR N
DUAL-IN-LINE PACKAGE
(TOP VIEW)



NC = No internal connection

description

The SN75161A and SN75162A eight-channel general-purpose interface bus transceivers are monolithic, high-speed, low-power Schottky devices designed to meet the requirements of IEEE Standard 488-1978. Each transceiver is designed to provide the bus-management and data-transfer signals between operating units of a single- or multiple-controller instrumentation system. When combined with the SN75160A octal bus transceiver, the SN75161A or SN75162A provides the complete 16-wire interface for the IEEE 488 bus.

The SN75161A and SN75162A each features eight driver-receiver pairs connected in a front-to-back configureation to form input/output (I/O) ports at both the bus and terminal sides. The direction of data through these driver-receiver pairs is determined by the DC, TE, and SC (on SN75162A) enable signals. The SC input on the SN75162A allows the REN and IFC transceivers to be controlled independently.

The driver outputs (GPIB I/O ports) feature active bus-terminating resistor circuits designed to provide a high-impedance to the bus when V_{CC} = 0 volts. The drivers are designed to handle loads up to 48 milliamperes of sink current. Each receiver features p-n-p transistor inputs for high-input impedance and a guaranteed hysteresis of 400 millivolts for increased noise immunity. All receivers have 3-state outputs to present a high-impedance to the terminal when disabled.

The SN75161A is manufactured in a 20-pin dual-in-line package. The SN75162A is manufactured in a 22-pin 400-mil (10,2-mm) dual-in-line package. The SN75161A and SN75162A are characterized for operation from 0°C to 70°C.

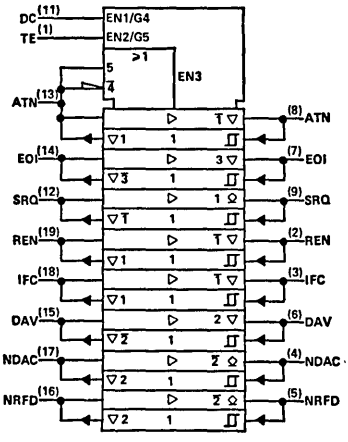
TABLE OF ABBREVIATIONS

NAME	IDENTITY	CLASS
DC	Direction Control	Control
TE	Talk Enable	
SC	System Control (SN75162 only)	
ATN	Attention	Bus Management
SRQ	Service Request	
REN	Remote Enable	
IFC	Interface Clear	
EOI	End or Edentify	
DAV	Data Valid	Data Transfer
NDAC	Not Data Accepted	
NRFD	Not Ready for Data	

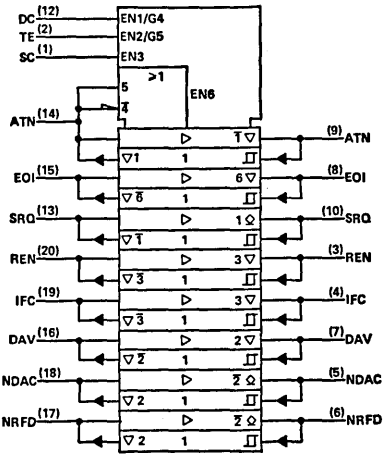
†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U.S. Patent Number 3,463,975.

logic symbols†

SN75161A



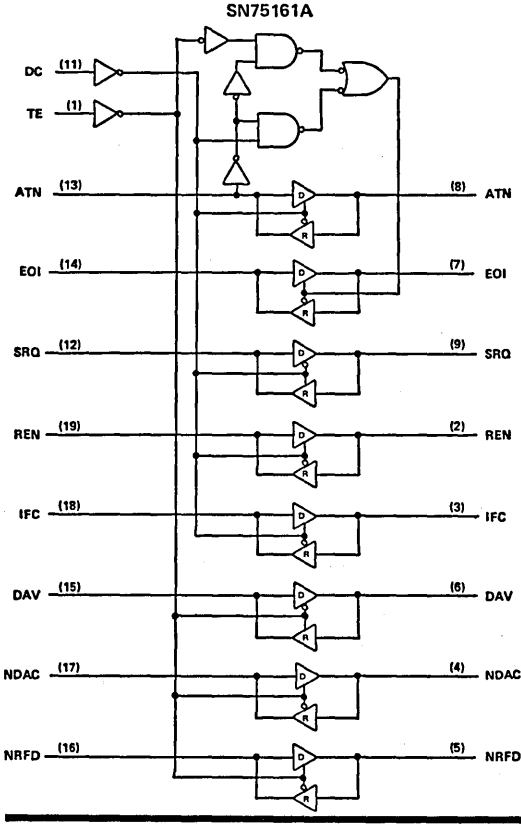
SN75162A



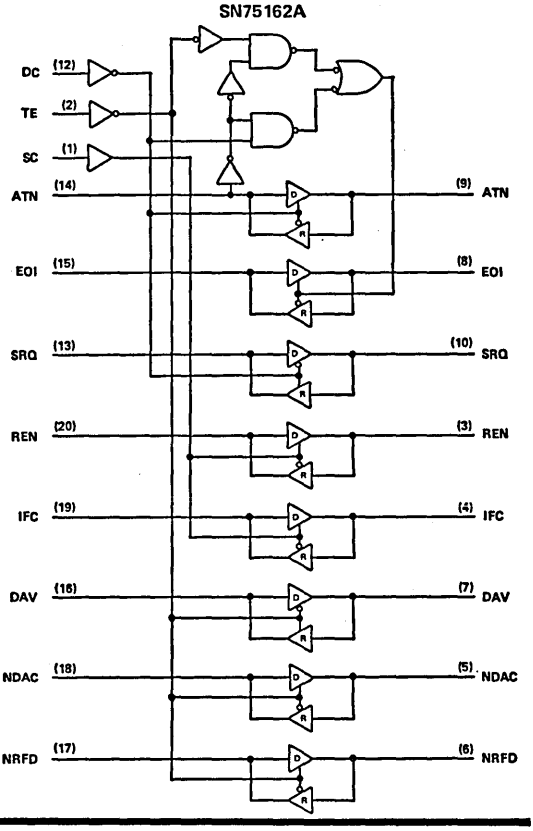
▽ designates 3-state output, ◇ designates open-collector outputs.
† These symbols are in accordance with IEEE Std 91/ANSI Y32.14 and current discussions in IEC and IEEE.

functional block diagrams (positive logic)

SN75161A



SN75162A



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SN75161A

RECEIVE/TRANSMIT FUNCTION TABLE

CONTROLS			BUS-MANAGEMENT CHANNELS					DATA-TRANSFER CHANNELS		
DC	TE	ATN†	ATN†	SRQ	REN	IFC	EOI	DAV	NDAC	NRFD
			(Controlled by DC)					(Controlled by TE)		
H	H	H	R	T	R	R	T	T	R	R
H	H	L					R			
L	L	H	T	R	T	T	R	R	T	T
L	L	L					T			
H	L	X	R	T	R	R	R	R	T	T
L	H	X	T	R	T	T	T	T	R	R

SN75162A

RECEIVE/TRANSMIT FUNCTION TABLE

CONTROLS				BUS-MANAGEMENT CHANNELS					DATA-TRANSFER CHANNELS		
SC	DC	TE	ATN†	ATN†	SRQ	REN	IFC	EOI	DAV	NDAC	NRFD
				(Controlled by DC)		(Controlled by SC)			(Controlled by TE)		
	H	H	H	R	T			T	T	R	R
	H	H	L					R			
	L	L	H	T	R			R	R	T	T
	L	L	L					T			
	H	L	X	R	T			R	R	T	T
	L	H	X	T	R			T	T	R	R
H						T	T				
L						R	R				

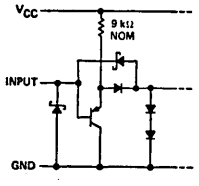
H = high level, L = Low level, R = receive, T = transmit, X = irrelevant

Direction of data transmission is from the terminal side to the bus side, and the direction of data receiving is from the bus side to the terminal side. Data transfer is noninverting in both directions.

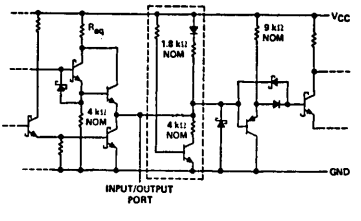
†ATN is a normal transceiver channel that functions additionally as an internal direction control or talk enable for EOI whenever the DC and TE inputs are in the same state. When DC and TE are in opposite states, the ATN channel functions as an independent transceiver only.

schematics of inputs and outputs

EQUIVALENT OF ALL CONTROL INPUTS

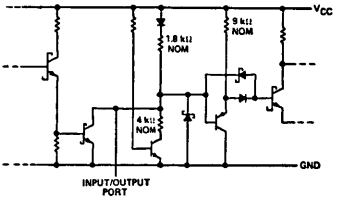


TYPICAL OF ALL I/O PORTS EXCEPT SRQ, NDAC, and NRFD GPIB I/O PORTS



Driver output R_{eq} = 30 Ω NOM
Receiver output R_{eq} = 110 Ω NOM
Circuit inside dashed lines is on GPIB I/O ports only.

TYPICAL OF SRQ, NDAC, and NRFD GPIB I/O PORT



absolute maximum ratings over operating free-air temperature range (unless othewise noted)

Supply voltage, V_{CC} (See Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Low-level driver output current . . . . . 100 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2): J Package . . . . . 1375 mW
N Package . . . . . 1150 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch (1,6 mm) from case for 10 seconds . . . . . 260°C

NOTES: 1. All voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, derate the J package to 880 mW at 70°C at the rate of 11 mW/°C and derate the N package to 736 mW at 70°C at the rate of 9.2 mW/°C. In the J package, SN75161A and SN75162A chips are alloy-mounted.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level output current, I_{OH}	Bus ports with 3-state outputs			−5.2	mA
	Terminal ports			−800	μA
Low-level output current, I_{OL}	Bus ports			48	mA
	Terminal ports			16	
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage		I_I = −18 mA			−0.8	−1.5	V
$V_{T+} - V_{T-}$	Hysteresis	Bus			0.4	0.65		V
V_{OH}	High-level output voltage	Terminal	I_{OH} = −800 μA		2.7	3.5		V
		Bus	I_{OH} = −5.2 mA		2.5	3.3		
V_{OL}	Low-level output voltage	Terminal	I_{OL} = 16 mA			0.3	0.5	V
		Bus	I_{OL} = 48 mA			0.35	0.5	
I_I	Input current at maximum input voltage	Terminal	V_I = 5.5 V			0.2	100	μA
I_{IH}	High-level input current	Terminal and control inputs	V_I = 2.7 V			0.1	20	μA
I_{IL}	Low-level input current		V_I = 0.5 V			−10	−100	μA
$V_{(I/O(bus)}$	Voltage at bus port		Driver disabled	$I_{I(bus)}$ = 0	2.5	3.0	3.7	V
				$I_{I(bus)}$ = −12 mA			−1.5	
$I_{I/O(bus)}$	Current into bus port	Power on	Driver disabled	$V_{I(bus)}$ = −1.5 V to 0.4 V	−1.3			mA
				$V_{I(bus)}$ = 0.4 to 2.5 V	0		−3.2	
				V(I(bus) = 2.5 V to 3.7 V			+2.5 −3.2	
				$V_{I(bus)}$ = 3.7 V to 5 V	0		2.5	
				$V_{I(bus)}$ = 5 V to 5.5 V	0.7		2.5	
		Power off	V_{CC} = 0,	$V_{I(bus)}$ = 0 V to 2.5 V			−40	μA
I_{OS}	Short-circuit output current	Terminal			−15	−35	−75	mA
		Bus			−25	−50	−125	
I_{CC}	Supply current		No load, TE, DC, and SC low				100	mA
$C_{i/o(bus)}$	Bus-port capacitance		V_{CC} = 5 V or 0 V, $V_{I/O}$ = 0 to 2 V, f = 1 MHz			30		pF

†All typical values are at V_{CC} = 5 V, T_A = 25°C

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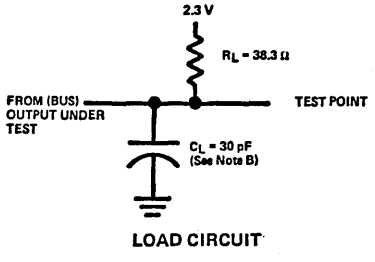
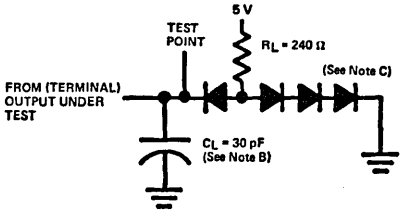
switching characteristics, V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C (unless otherwise noted)

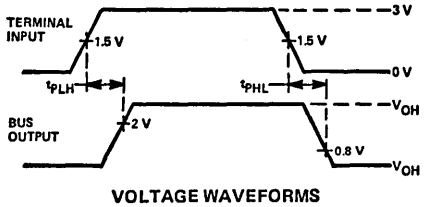
PARAMETER		FROM	TO	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	Terminal	Bus	C_L = 30 pF, R_L = 38.3 Ω to 2.3 V, See Figure 1		14	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output					14	20	
t_{PLH}	Propagation delay time, low-to-high-level output	Bus	Terminal	C_L = 30 pF, R_L = 240 Ω to 5 V, See Figure 2		12	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output					16	22	
t_{PZH}	Output enable time to high level	TE, DC, or SC	BUS (ATTN, EOI, REN, IFC, and DAV)	R_L = 480 Ω to 0 V, See Figure 3			60	ns
t_{PHZ}	Output disable time from high level						45	
t_{PZL}	Output enable time to low level			R_L = 38.3 Ω to 2.3 V, See Figure 3			60	
t_{PLZ}	Output disable time from low level						55	
t_{PZH}	Output enable time to high level	TE, DC, or SC	Terminal	R_L = 3 kΩ to 0 V, See Figure 4			55	ns
t_{PHZ}	Output disable time from high level						50	
t_{PZL}	Output enable time to low level			R_L = 280 Ω to 5 V, See Figure 4			45	
t_{PLZ}	Output disable time from low level						55	

PARAMETER MEASUREMENT INFORMATION



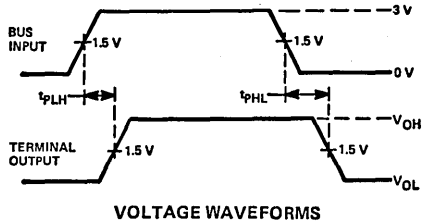
LOAD CIRCUIT





VOLTAGE WAVEFORMS

FIGURE 1 – TERMINAL-TO-BUS PROPAGATION DELAY TIMES

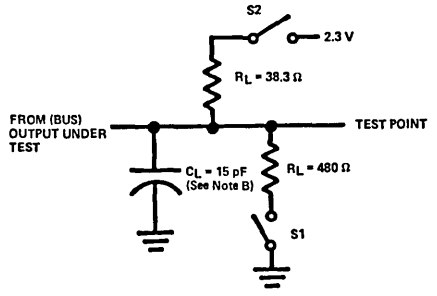


VOLTAGE WAVEFORMS

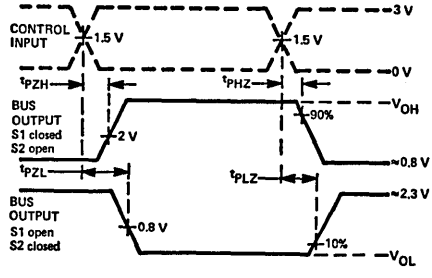
FIGURE 2 – BUS-TO-TERMINAL PROPAGATION DELAY TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916 or equivalent.

PARAMETER MEASUREMENT INFORMATION

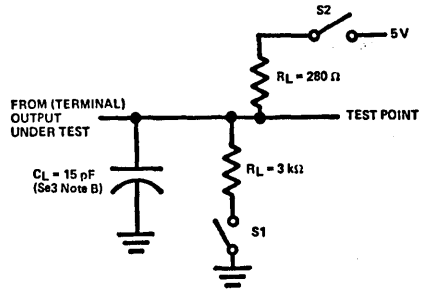


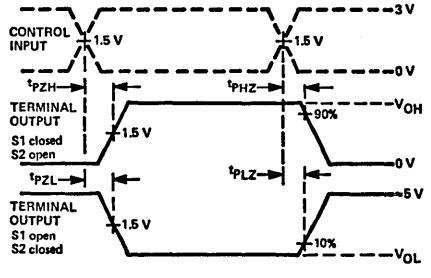
LOAD CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 3 – BUS ENABLE AND DISABLE TIMES





VOLTAGE WAVEFORMS

FIGURE 4 – TERMINAL ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r \leq 6$ ns, $t_f \leq 6$ ns, Z_{out} = 50 Ω.

B. C_L includes probe and jig capacitance.

TYPICAL CHARACTERISTICS

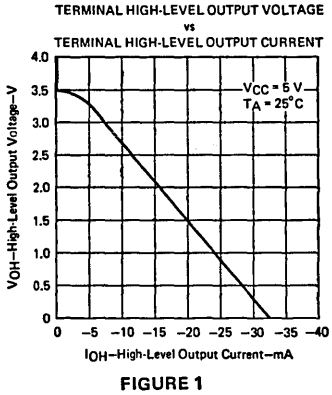


FIGURE 1

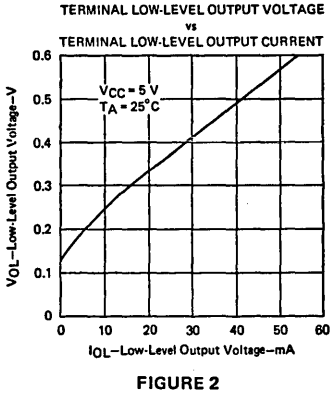


FIGURE 2

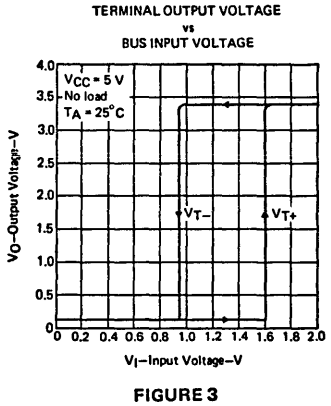


FIGURE 3

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TYPICAL CHARACTERISTICS

BUS HIGH-LEVEL OUTPUT VOLTAGE
vs
BUS HIGH-LEVEL OUTPUT CURRENT

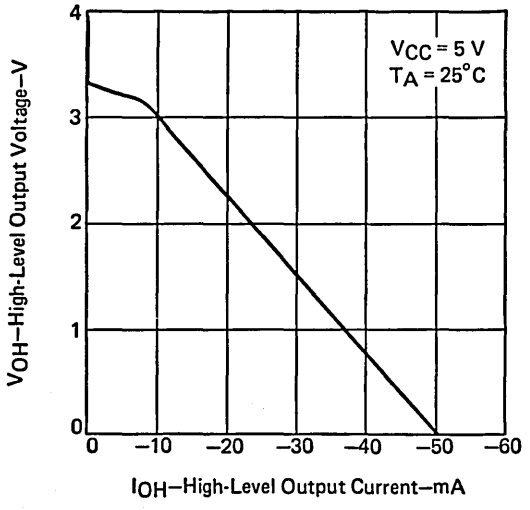


FIGURE 4

BUS LOW-LEVEL OUTPUT VOLTAGE
vs
BUS LOW-LEVEL OUTPUT CURRENT

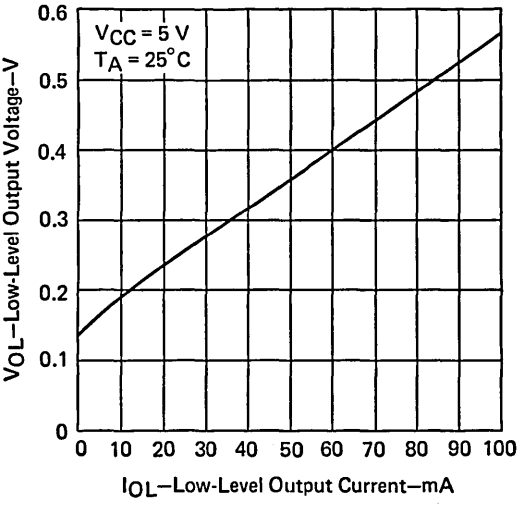


FIGURE 5

BUS OUTPUT VOLTAGE
vs
TERMINAL INPUT VOLTAGE

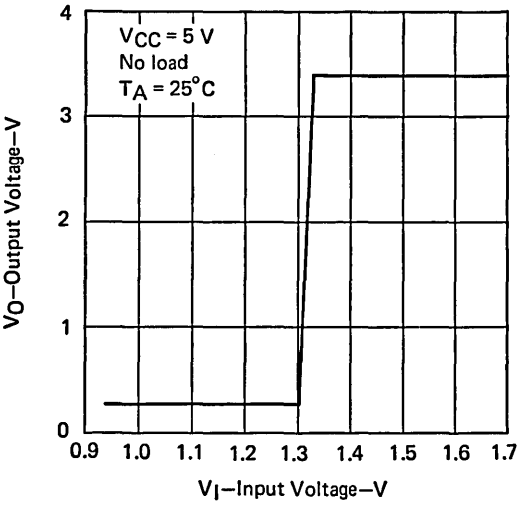


FIGURE 6

BUS CURRENT
vs
BUS VOLTAGE

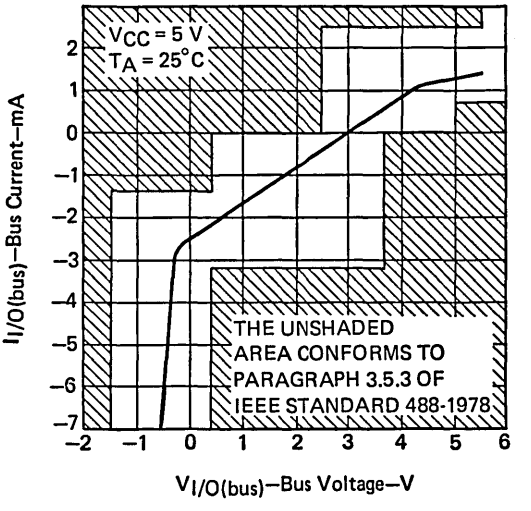


FIGURE 7

TYPE SN75163A OCTAL GENERAL-PURPOSE INTERFACE BUS TRANSCEIVER

BULLETIN NO. DL-S 12778, OCTOBER 1980

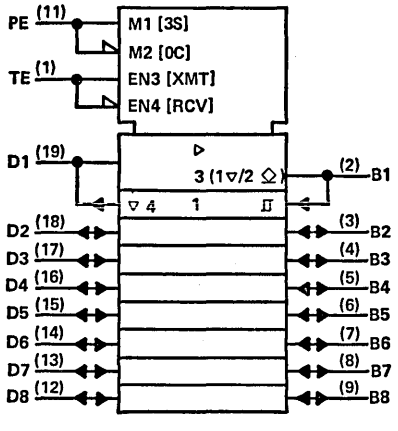
- 8-Channel Bidirectional Transceivers
- High-Speed Low-Power Schottky Circuitry†
- Low Power Dissipation . . . 60 mW Max per Channel
- High-Impedance P-N-P Inputs
- Receiver Hysteresis . . . 650 mV Typ
- Open-Collector Driver Output Option
- No Loading of Bus When Device is Powered Down (V_{CC} = 0 V)

description

The SN75163A octal general-purpose interface bus transceiver is a monolithic, high-speed, low-power Schottky device. It is designed for two-way data communications over single-ended transmission lines. The transceiver features driver outputs that can be operated in either the open-collector or three-state modes. If Talk Enable is high, these outputs have the characteristics of open-collector outputs when Pull-up Enable (PE) is low and of three-state outputs when PE is high. Taking TE low places the outputs in the high-impedance state. The driver outputs are designed to handle loads up to 48 milliamperes of sink current. Each receiver features p-n-p transistor inputs for high input impedance and 400 millivolts of guaranteed hysteresis for increased noise immunity.

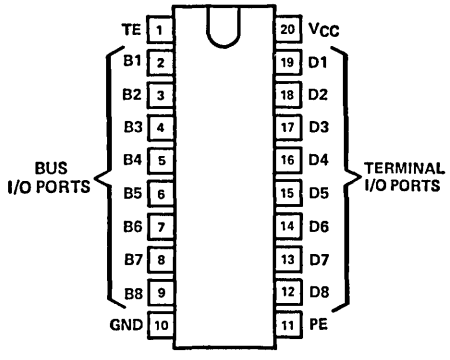
The SN75163 is characterized for operation from 0°C to 70°C.

logic symbol‡



‡This symbol is in accordance with IEEE Std 91/ANSI Y32.14 and current discussions in IEC and IEEE.

J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



FUNCTION TABLES

DRIVERS

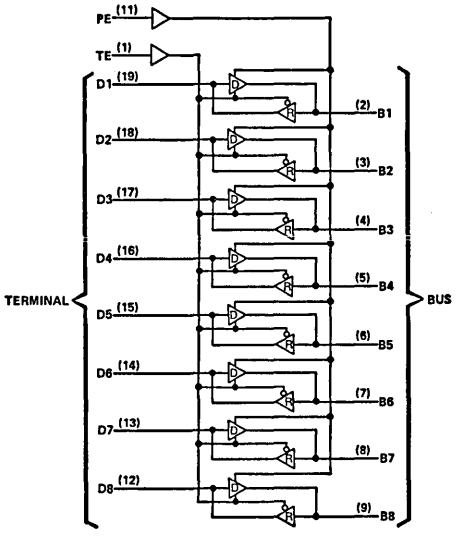
INPUTS			OUTPUT
D	TE	PE	B
H	H	H	H
L	H	H	L
H	X	L	Z
L	H	L	L
X	L	X	Z

RECEIVERS

INPUTS			OUTPUTS
B	TE	PE	D
L	L	X	L
H	L	X	H
X	H	X	Z

H = high level, L = low level, X = irrelevant, Z = High-impedance state.

functional block diagram (positive logic)



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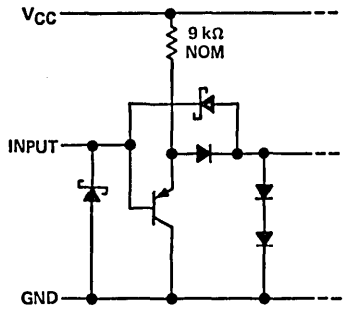
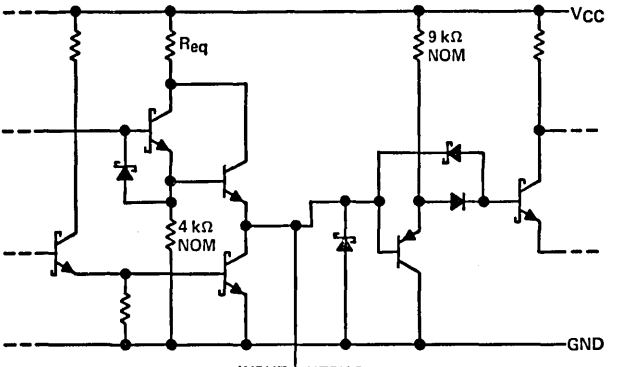
schematics of inputs and outputs

EQUIVALENT OF ALL CONTROL INPUTS



EQUIVALENT OF ALL INPUT/OUTPUT PORTS



Driver output R_{eq} = 30 Ω NOM
Receiver output R_{eq} = 110 Ω NOM

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Low-level driver output current . . . . . 100 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2): J package . . . . . 1375 mW
N package . . . . . 1150 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 (1,6 mm) from case for 10 seconds . . . . . 260°C

NOTES: 1. All voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, derate the J package to 880 mW at 70°C at the rate of 11 mW/°C and derate the N package to 736 mW at 70°C at the rate of 9.2 mW/°C. In the J package, SN75163A chips are alloy-mounted.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level output current, I_{OH}	Bus ports with pull-ups active			−10	mA
	Terminal ports			−800	μA
Low-level output current, I_{OL}	Bus ports			48	mA
	Terminal ports			16	
Operating free-air temperature, T_A		0		70	°C

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage		I_I = −18 mA			−0.8	−1.5	V
$V_{T+} - V_{T-}$	Hysteresis‡	Bus			0.4	0.65		V
V_{OH}	High level output voltage	Terminal	I_{OH} = −800 μA,	TE at 0.8 V	2.7	3.5		V
		Bus	I_{OH} = −10 mA,	PE and TE at 2 V	2.5	3.3		
V_{OL}	Low-level output voltage	Terminal	I_{OL} = 16 mA,	TE at 0.8 V		0.3	0.5	V
		Bus	I_{OL} = 48 mA,	PE and TE at 2 V		0.4	0.5	
I_{OH}	High-level output current (open-collector mode)	Bus	V_O = 5.5 V, PE at 0.8 V, D and TE at 2 V				100	μA
I_{OZ}	Off-state output current (3-state mode)	Bus	PE at 2 V, TE at 0.8 V	V_O = 2.7 V			20	μA
				V_O = 0.4 V			−20	
I_I	Input current at maximum input voltage	Terminal	V_I = 5.5 V			0.2	100	μA
I_{IH}	High-level input current	Terminal	V_I = 2.7 V			0.1	20	μA
I_{IL}	Low-level input current	Terminal	V_I = 0.5 V			−10	−100	μA
I_{OS}	Short-circuit output current	Terminal			−15	−35	−75	mA
		Bus			−25	−50	−125	
I_{CC}	Supply current		No load	Receivers low and enabled			70	mA
				Drivers low and enabled			90	
$C_{i/o(bus)}$	Bus-port capacitance		V_{CC} = 5 V or 0 V, $V_{I/O}$ = 0 to 2 V, f = 1 MHz			30		pF

†All typical values are at V_{CC} = 5, T_A = 25°C.
‡Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}.

switching characteristics, V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C (unless otherwise noted)

PARAMETER		FROM	TO	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	Terminal	Bus	C_L = 30 pF, R_L = 38.3 Ω to 2.3 V		14	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output					14	20	
t_{PLH}	Propagation delay time, low-to-high-level output	Bus	Terminal	C_L = 30 pF, R_L = 240 Ω to 5 V		12	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output					16	22	
t_{PZH}	Output enable time to high level	TE	Bus	R_L = 480 Ω to 0 V		25	35	ns
t_{PHZ}	Output disable time from high level					13	22	
t_{PZL}	Output enable time to low level			R_L = 38.3 Ω to 2.3 V		22	35	
t_{PLZ}	Output disable time from low level					22	32	
t_{PZH}	Output enable time to high level	TE	Terminal	R_L = 3 kΩ to 0 V		20	30	ns
t_{PHZ}	Output disable time from high level					12	20	
t_{PZL}	Output enable time to low level			R_L = 280 Ω to 5 V		23	32	
t_{PLZ}	Output disable time from low level					19	30	
t_{en}	Output pull-up enable time	PE	Terminal	R_L = 480 Ω to 0 V		15	22	ns
t_{dis}	Output pull-up disable time					13	20	

For test circuits and voltage waveforms, see SN75160A, pages 192 and 193.

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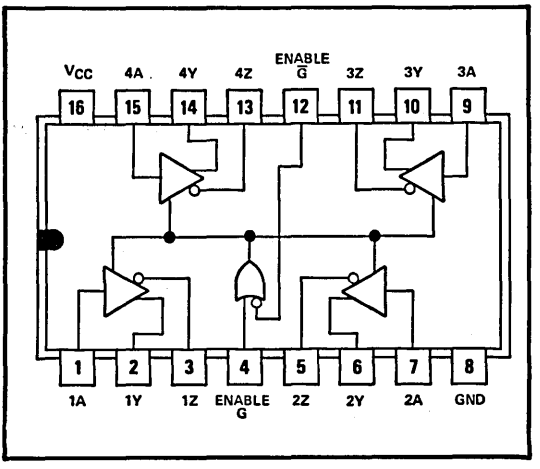
TYPE SN75172
QUADRUPLE DIFFERENTIAL LINE DRIVER

BULLETIN NO. DL-S 12769, OCTOBER 1980

- Meets EIA Standard RS-422A and CCITT Recommendations V.11 and X.27
- Meets EIA Subcommittee TR30.1 Draft Standard PN1360 (as of April 1980)
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- 3-State Outputs
- Common-Mode Output Voltage Range . . . −7 V to 12 V
- Active-High and Active-Low Enables
- Thermal Shutdown Protection
- Positive and Negative Current Limiting
- Operates from Single 5-Volt Supply
- Low Power Requirements
- Functionally Interchangeable With AM26LS31

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



description

The SN75172 is a monolithic quadruple differential line driver with three-state outputs. It is designed to meet the requirements of EIA Standard RS-422A and CCITT Recommendations V.11 and X.27. The device is optimized for balanced multipoint bus transmission at rates up to 4 megabits per second. Each driver features wide positive and negative common-mode output voltage ranges making it suitable for party-line applications in noisy environments.

FUNCTION TABLE (EACH DRIVER)

INPUT	ENABLES		OUTPUTS	
A	G	$\overline{G}$	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

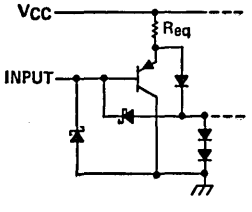
H = high level
L = low level
X = irrelevant
Z = high impedance (off)

The SN75172 provides positive- and negative-current limiting and thermal shutdown for protection from line fault conditions on the transmission-bus line. Shutdown occurs at a junction temperature of approximately 150°C. This device offers optimum performance when used with the SN75173 or SN75175 quadruple differential line receivers.

The SN75172 is characterized for operation from 0°C to 70°C.

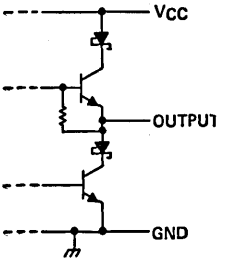
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



Data inputs: R_{eq} = 3 kΩ NOM
Enable inputs: R_{eq} = 8 kΩ NOM

TYPICAL OF ALL OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2): J package . . . . . 1375 mW
N package . . . . . 1150 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch (1,6 mm) from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1/16 inch (1,6 mm) from case for 10 seconds: N package . . . . . 260°C

NOTES: 1. All voltage values are with respect to the network ground terminal.
2. For operation above 25°C free-air temperature, derate the J package to 880 mW at 70°C at the rate of 11 mW/°C and the N package to 736 mW at 70°C at the rate of 9.2 mW/°C. In the J package, SN75172 chips are alloy-mounted.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Common-mode output voltage, V_{OC}	−7†		12	V
High-level output current, I_{OH}			−60	mA
Low-level output current, I_{OL}			60	mA
Operating free-air temperature, T_A	0		70	°C

†The algebraic convention, where the less-positive (more-negative) limit is designated minimum, is used in this data sheet with common-mode output voltage only.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless other noted)

PARAMETER		TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{IH} = 2 V, I_{OH} = −33 mA	V_{IL} = 0.8 V,		3.7		V
V_{OL}	Low-level output voltage	V_{IH} = 2 V, I_{OL} = 33 mA	V_{IL} = 0.8 V,		1.1		V
$\lvert V_{OD1}\rvert$	Differential output voltage	I_O = 0				$2V_{OD2}$	V
$\lvert V_{OD2}\rvert$	Differential output voltage	R_L = 100 Ω,	See Figure 1	2			V
		R_L = 60 Ω,	See Figure 1	1.5			
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of differential output voltage§	R_L = 60 Ω or 100 Ω, See Figure 1				±0.2	V
V_{OC}	Common-mode output voltage¶					3	V
$\Delta\lvert V_{OC}\rvert$	Change in magnitude of common-mode output voltage§					±0.2	V
I_O	Output current with power off	V_{CC} = 0,	V_O = −7 V to 12			±100	μA
I_{OZ}	High-impedance-state output current	V_O = −7 V to 12 V				±100	μA
I_{IH}	High-level input current	V_I = 2.7 V				20	μA
I_{IL}	Low-level input current	V_I = 0.5 V				−360	μA
I_{OS}	Short-circuit output current	V_O = −7 V				−180	mA
		V_O = V_{CC}				180	
		V_O = 12 V				500	
I_{CC}	Supply current (all drivers)	No load	Outputs enabled		38	60	mA
			Outputs disabled		18	40	

‡All typical values are at V_{CC} = 5 V and T_A = 25°C.
§$\Delta\lvert V_{OD}\rvert$ and $\Delta\lvert V_{OC}\rvert$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
¶In EIA Standard RS-422A, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.

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switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DD}	Differential-output delay time	R_L = 60 Ω, See Figure 2		35	50	ns
t_{TD}	Differential-output transition time			50	75	ns
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 27 Ω, See Figure 3		16	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output			44	65	ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω, See Figure 4		60	80	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω, See Figure 5		30	45	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω, See Figure 4		51	75	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω, See Figure 5		18	30	ns

PARAMETER MEASUREMENT INFORMATION

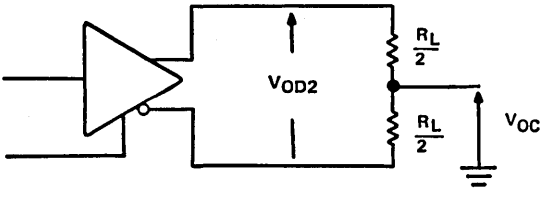
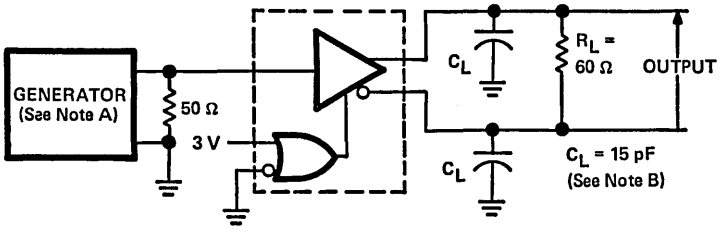
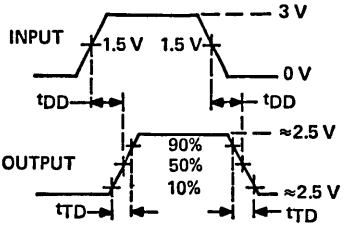


FIGURE 1–DIFFERENTIAL AND COMMON-MODE OUTPUT VOLTAGES



TEST CIRCUIT

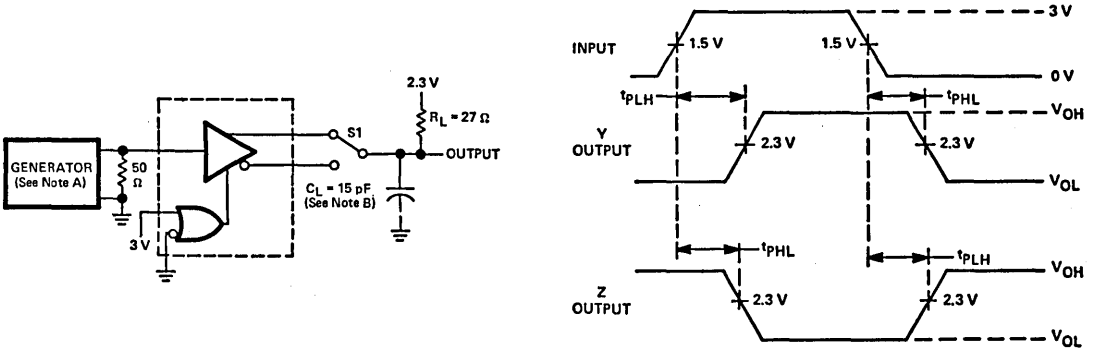


VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: $t_r \leq 5$ ns, $t_f \leq 5$ ns, PRR = 1 MHz, duty cycle = 50%, Z_o = 50 Ω.
B. C_L includes probe and stray capacitance.
C. All diodes are IN916 or IN3064.

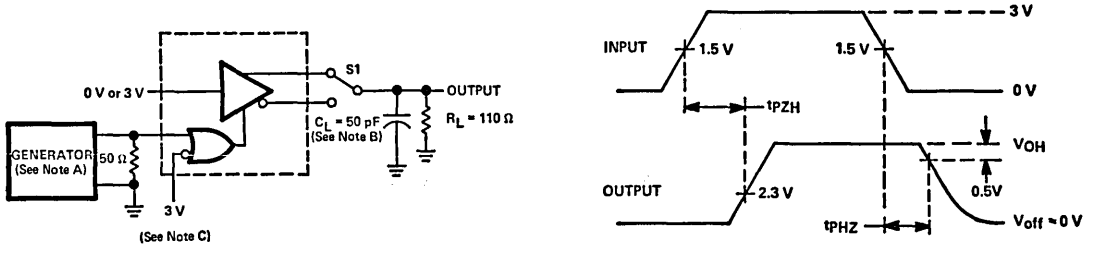
FIGURE 2–DIFFERENTIAL-OUTPUT DELAY AND TRANSITION TIMES

PARAMETER MEASUREMENT INFORMATION



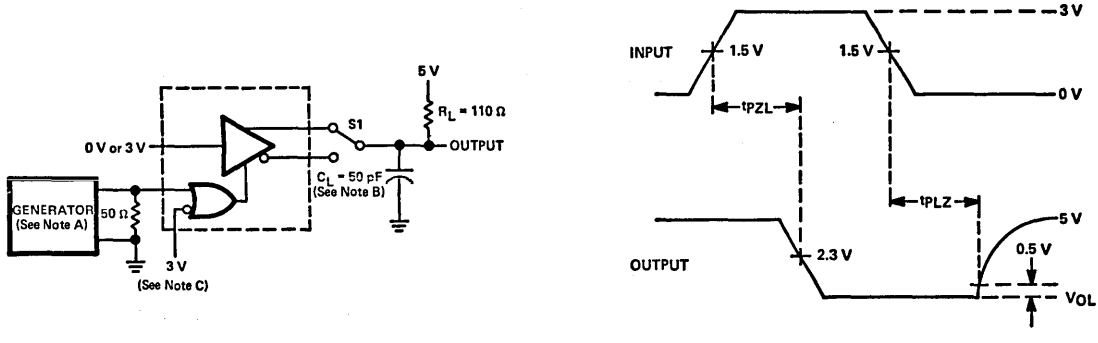
TEST CIRCUIT VOLTAGE WAVEFORMS

FIGURE 3–PROPAGATION DELAY TIMES



TEST CIRCUIT VOLTAGE WAVEFORMS

FIGURE 4–t_{PZH} AND t_{PHZ}



TEST CIRCUIT VOLTAGE WAVEFORMS

FIGURE 5–t_{PZL} AND t_{PLZ}

NOTES: A. The input pulse is supplied by a generator having the following characteristics: $t_f \leq 5$ ns, $t_f \leq 5$ ns, PRR = 1 MHz, duty cycle = 50%, Z_{out} = 50 Ω.

B. C_L include probe and jig capacitance.

C. To test the active-low enable $\overline{G}$, ground G and apply an inverted waveform to $\overline{G}$.

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TYPICAL CHARACTERISTICS

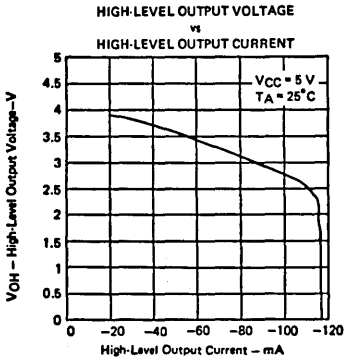


FIGURE 6

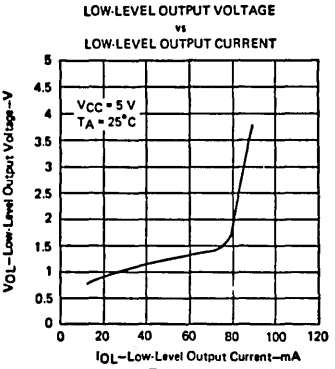


FIGURE 7

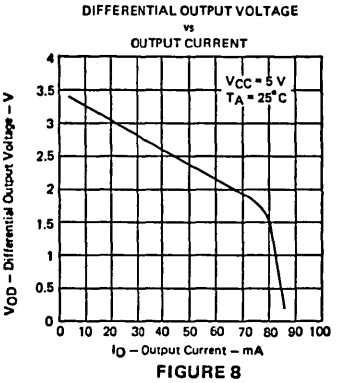


FIGURE 8

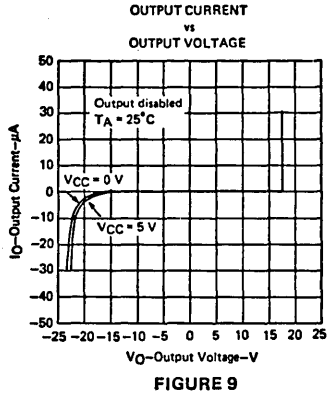


FIGURE 9

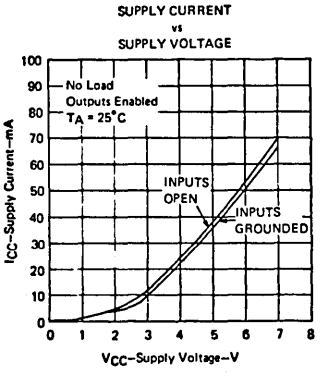


FIGURE 10

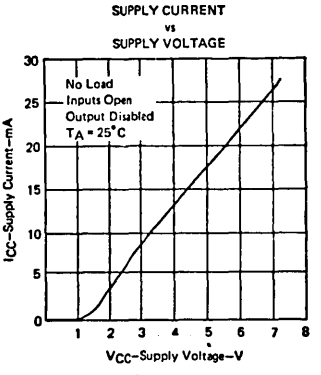
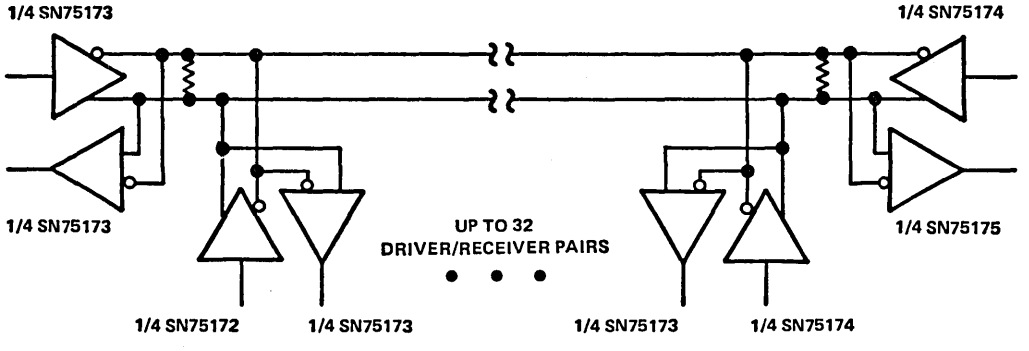


FIGURE 11

TYPICAL APPLICATION



NOTE: The line length should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

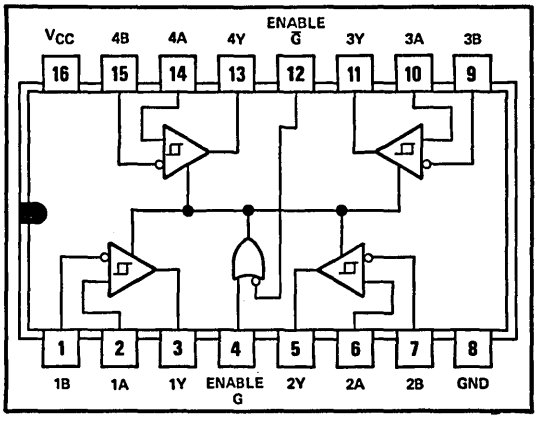
FIGURE 12

TYPE SN75173
QUADRUPLE DIFFERENTIAL LINE RECEIVER

BULLETIN NO. DL-S 12770, OCTOBER 1980

- Meets EIA Standards RS-422A and RS-423A
- Meets CCITT Recommendations V.10, V.11 X.26, and X.27
- Meets EIA Subcommittee TR30.1 Draft Standard PN1360 (as of April 1980)
- Designed for Multipoint Bus Transmission on Long Bus Lines in Noisy Environments
- 3-State Outputs
- Common-Mode Input Voltage Range . . . −12 V to 12 V
- Input Sensitivity . . . ±200 mV
- Input Hysteresis . . . 50 mV Typ
- High Input Impedance . . . 12 kΩ Min
- Operates from Single 5-Volt Supply
- Low Power Requirements
- Plug-In Replacement for AM26LS32

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



FUNCTION TABLE (EACH RECEIVER)

DIFFERENTIAL INPUTS A − B	ENABLES G	ENABLES $\overline{G}$	OUTPUT Y
$V_{ID} > 0.2$ V	H	X	H
	X	L	H
−0.2 V < V_{ID} < 0.2 V	H	X	?
	X	L	?
$V_{ID} < -0.2$ V	H	X	L
	X	L	L
X	L	H	Z

H = high level
L = low level
X = irrelevant
? = indeterminate
Z = high-impedance (off)

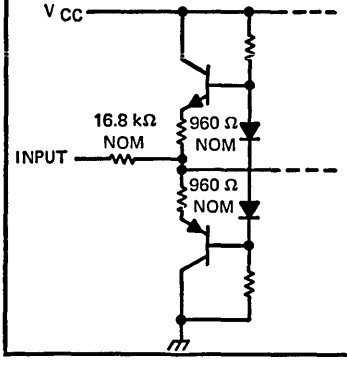
description

The SN75173 is a monolithic quadruple differential line receiver with three state outputs. It is designed to meet the requirements of EIA Standards RS-422A and RS-423A and several CCITT recommendations. The device is optimized for balanced multipoint bus transmission at rates up to 10 megabits per second. Each receiver features an active-high enable and an active-low enable common to all four receivers. It also features high input impedance, input hysteresis for increased noise immunity, and input sensitivity of ±200 millivolts over a common-mode input voltage range of −12 volts to 12 volts. The SN75173 is designed for optimum performance when used with the SN75172 or SN75174 quadruple differential line drivers.

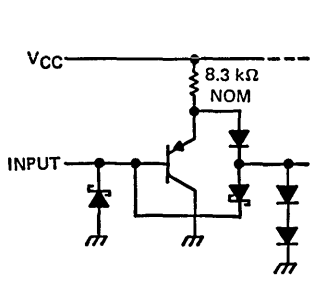
The SN75173 is characterized for operation from 0°C to 70°C.

schematics of inputs and outputs

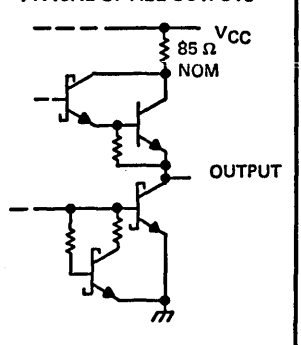
EQUIVALENT OF A OR B INPUT



EQUIVALENT OF G OR $\overline{G}$ INPUT



TYPICAL OF ALL OUTPUTS



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage, A or B inputs . . . . . ±25 V
Differential input voltage (see Note 2) . . . . . ±25 V
Enable input voltage . . . . . 7 V
Low-level output current . . . . . 50 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3): J Package . . . . . 1025 mW
N Package . . . . . 1150 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch (1,6 mm) from case for 60 seconds: J Package . . . . . 300°C
Lead temperature 1/16 inch (1,6 mm) from case for 10 seconds: N Package . . . . . 260°C

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
2. Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.
3. For operation above 25°C free-air temperature, derate the J package to 656 mW at 70°C at the rate of 8.2 mW/°C and the N package to 736 mW at 70°C at the rate of 9.2 mW/°C. In the J package, SN75173 chips are glass-mounted.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Common-mode input voltage, V_{IC}			±12	V
Differential input voltage, V_{ID}			±12	V
High-level output current, I_{OH}			−400	μA
Low-level output current, I_{OL}			16	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

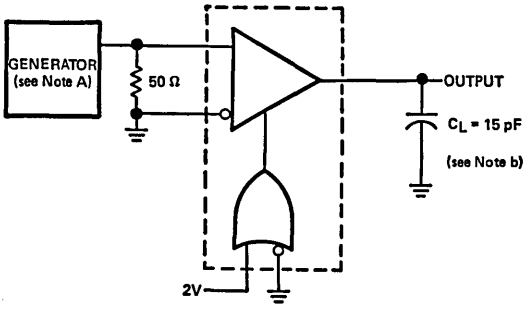
	PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{TH}	Differential-input high-threshold voltage	V_O = 2.7 V,	I_O = −0.4 mA			0.2	V
V_{TL}	Differential-input low-threshold voltage	V_O = 0.5 V,	I_O = 16 mA	−0.2‡			V
$V_{T+} - V_{T-}$	Hysteresis§				50		mV
V_{IH}	High-level enable input voltage			2			V
V_{IL}	Low-level enable input voltage					0.8	V
V_{IK}	Enable-input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV,	I_{OH} = −400 μA	2.7			V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV,	I_{OL} = 8 mA			0.45	V
			I_{OL} = 16 mA			0.5	
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V				±20	μA
I_I	Line input current	Other input at 0 V, See Note 4	V_I = 12 V			1	mA
			V_I = −7 V			−0.8	
I_{IH}	High-level enable-input current	V_{IH} = 2.7 V				20	μA
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V				−100	μA
r_i	Input resistance			12			kΩ
I_{OS}	Short-circuit output current¶			−15		−85	mA
I_{CC}	Supply current	Outputs disabled				70	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C
‡The algebraic convention, where the less-positive (more-negative) limit is designated minimum, is used in this data sheet for threshold voltage levels only.
§Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}. See Figure 4.
¶Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.
NOTE 4: Refer to EIA Standard RS-422A and RS-423A for exact conditions.

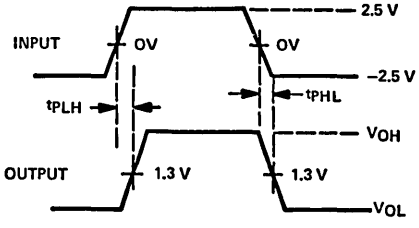
switching characteristics, V_{CC} = 5 V, T_A = 25°C

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = −2.5 V to 2.5 V,	C_L = 15 pF,		20	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output	See Figure 1			22	35	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF,	See Figure 2		17	22	ns
t_{PZL}	Output enable time to low level	C_L = 15 pF,	See Figure 3		20	25	ns
t_{PHZ}	Output disable time from high level	C_L = 5 pF,	See Figure 2		21	30	ns
t_{PLZ}	Output disable time from low level	C_L = 5 pF,	See Figure 3		30	40	ns

PARAMETER MEASUREMENT INFORMATION

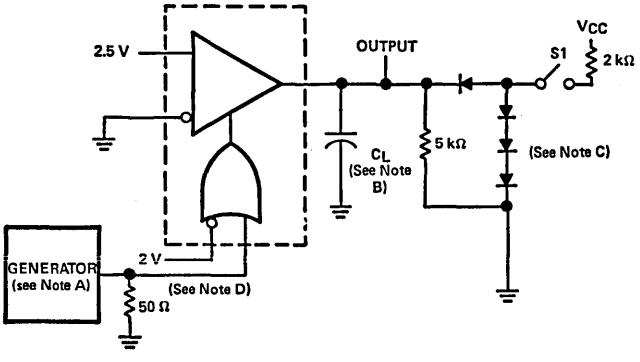


TEST CIRCUIT

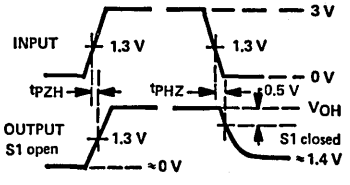


VOLTAGE WAVEFORMS

FIGURE 1 – t_{PLH}, t_{PHL}



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 2 – t_{PHZ}, t_{PZH}

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r = t_f$ = 6 ns, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.
C. All diodes are in 916 or equivalent.
D. To test the active low enable $\overline{G}$, ground G and apply an inverted input waveform to $\overline{G}$.

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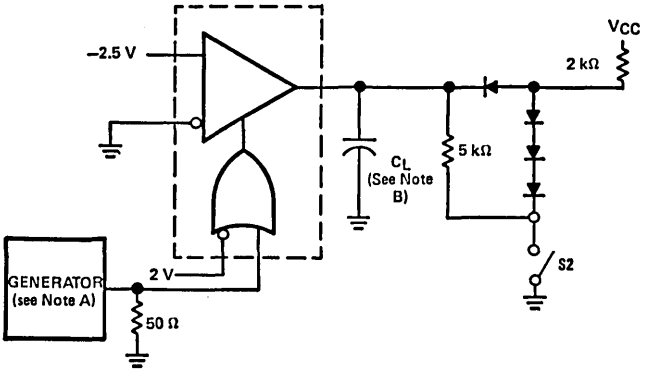
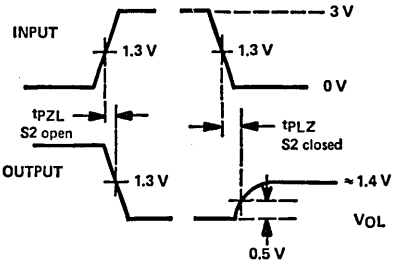
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle, = 50%, $t_r = t_f = 6$ ns, $Z_{out} = 50\ \Omega$.
B. C_L includes probe and jig capacitance.
C. All diodes are in 916 or equivalent.
D. To test the active low enable $\overline{G}$, ground G and apply an inverted input waveform to $\overline{G}$.

FIGURE 3 – t_{PZL}, t_{PLZ}

TYPICAL CHARACTERISTICS

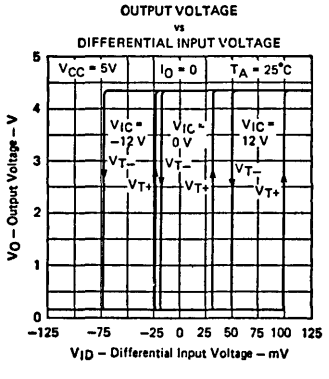


FIGURE 4

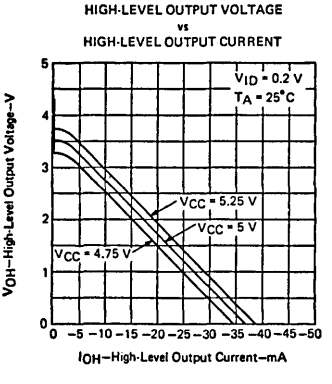


FIGURE 5

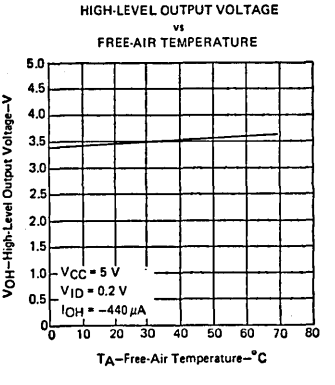


FIGURE 6

TYPICAL CHARACTERISTICS

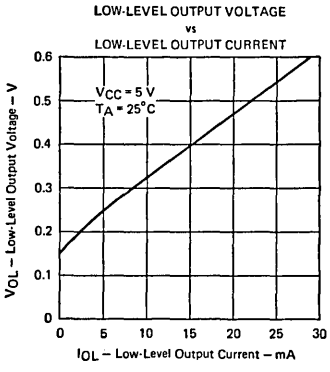


FIGURE 7

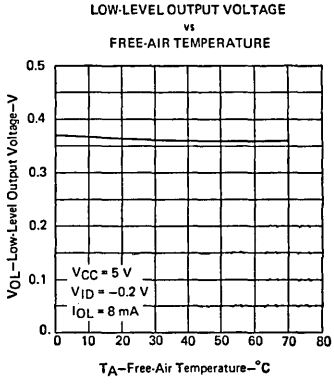


FIGURE 8

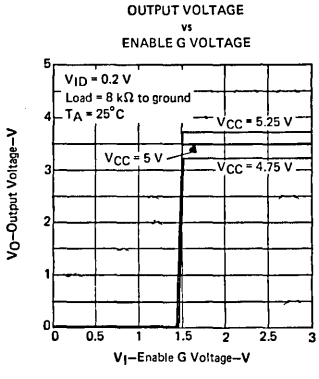


FIGURE 9

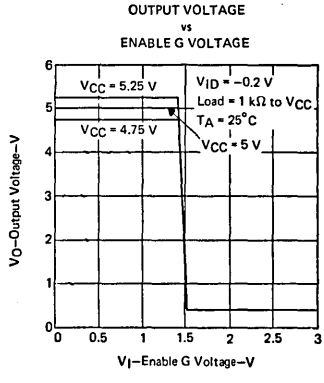
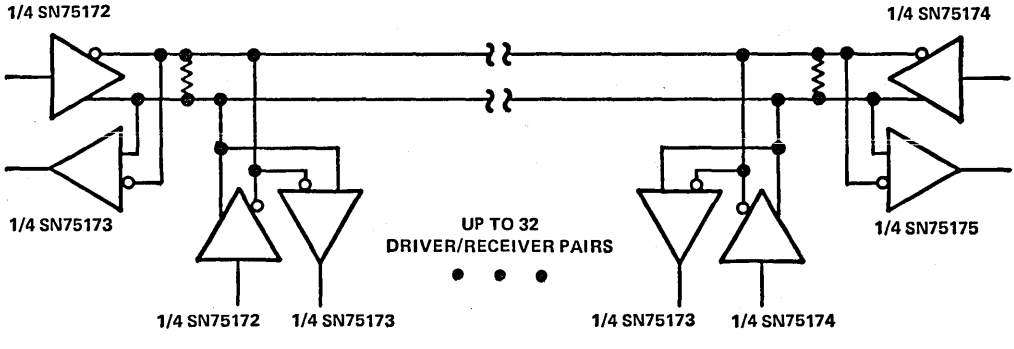


FIGURE 10

TYPICAL APPLICATION



NOTE: The line should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

FIGURE 11

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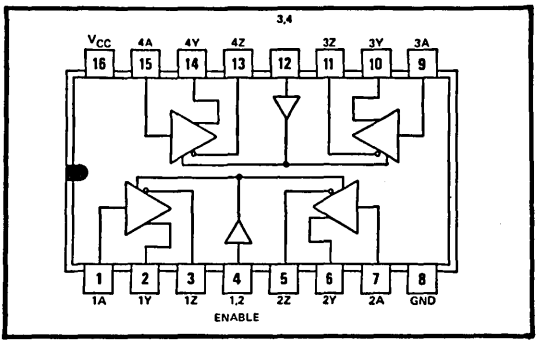
TYPE SN75174
QUADRUPLE DIFFERENTIAL LINE DRIVER

BULLETIN NO. DL-S 12771, OCTOBER 1980

- Meets EIA Standard RS-422A and CCITT Recommendations V.11 and X.27
- Meets EIA Subcommittee TR30.1 Draft Standard PN1360 (as of April 1980)
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- 3-State Outputs
- Common-Mode Output Voltage Range ... −7 V to 12 V
- Active-High Enables
- Thermal Shutdown Protection
- Positive and Negative Current Limiting
- Operates from Single 5-Volt Supply
- Low Power Requirements
- Functionally Interchangeable with MC3487

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



FUNCTION TABLE (EACH DRIVER)

INPUT	ENABLE	OUTPUTS	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

H = TTL high level, L = TTL low level, X = irrelevant, Z = high impedance (off)

description

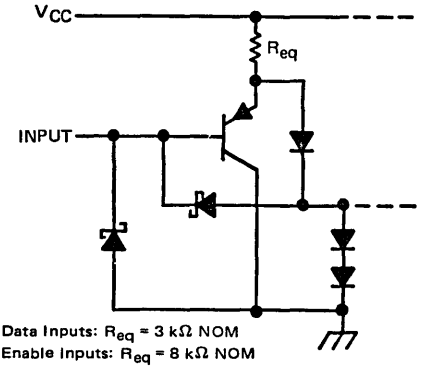
The SN75174 is a monolithic guadruple differential line driver with three-state outputs. It is designed to meet the requirements of EIA Standard RS-422A and CCITT Recommendations V.11 and X.27. The device is optimized for balanced multipoint bus transmission at rates up to 4 megabits per second. Each driver features wide positive and negative common-mode output voltage ranges making it suitable for party-line applications in noisy environments.

The SN75174 provides positive- and negative-current limiting and thermal shutdown for protection from line fault conditions on the transmission bus line. Shutdown occurs at a junction temperature of approximately 150°C. This device offers optimum performance when used with the SN75173 or SN75175 quadruple differential line receivers.

The SN75174 is characterized for operation from 0°C to 70°C.

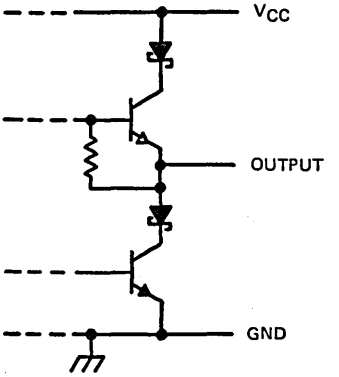
schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



Data Inputs: R_{eq} = 3 kΩ NOM
Enable Inputs: R_{eq} = 8 kΩ NOM

TYPICAL OF ALL OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2): J package . . . . . 1375 mW
N package . . . . . 1150 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch (1,6 mm) from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1/16 inch (1,6 mm) from case for 10 seconds: N package . . . . . 260°C

NOTES: 1. All voltage values are with respect to the network ground terminal.
2. For operation above 25°C free-air temperature, derate the J package to 880 mW at 70°C at the rate of 11 mW/°C and the N package to 736 mW at 70°C at the rate of 9.2 mW/°C. In the J package, SN75174 chips are alloy-mounted.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Common-mode output voltage, V_{OC}	−7†		12	V
High-level output current, I_{OH}			−60	mA
Low-level output current, I_{OL}			60	mA
Operating free-air temperature, T_A	0		70	°C

†The algebraic convention, where the less-positive (more-negative) limit is designated minimum, is used in this data sheet with common-mode output voltage only.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless other noted)

PARAMETER		TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{IH} = 2 V, I_{OH} = −33 mA	V_{IL} = 0.8 V,		3.7		V
V_{OL}	Low-level output voltage	V_{IH} = 2 V, I_{OL} = 33 mA	V_{IL} = 0.8 V,		1.1		V
$\lvert V_{OD1}\rvert$	Differential output voltage	I_O = 0				$2V_{OD2}$	V
$\lvert V_{OD2}\rvert$	Differential output voltage	R_L = 100 Ω,	See Figure 1	2			V
		R_L = 60 Ω,	See Figure 1	1.5			
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of differential output voltage§	R_L = 60 Ω or 100 Ω, See Figure 1				±0.2	V
V_{OC}	Common-mode output voltage¶					3	V
$\Delta\lvert V_{OC}\rvert$	Change in magnitude of common-mode output voltage§					±0.2	V
I_O	Output current with power off	V_{CC} = 0,	V_O = −7 V to 12			±100	μA
I_{OZ}	High-impedance-state output current	V_O = −7 V to 12 V				±100	μA
I_{IH}	High-level input current	V_I = 2.7 V				20	μA
I_{IL}	Low-level input current	V_I = 0.5 V				−360	μA
I_{OS}	Short-circuit output current	V_O = −7 V				−180	mA
		V_O = V_{CC}				180	
		V_O = 12 V				500	
I_{CC}	Supply current (all drivers)	No load	Outputs enabled		38	60	mA
			Outputs disabled		18	40	

‡All typical values are at V_{CC} = 5 V and T_A = 25°C.
§$\Delta\lvert V_{OD}\rvert$ and $\Delta\lvert V_{OC}\rvert$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
¶In EIA Standard RS-422A, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.

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switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{DD}	Differential-output delay time	R_L = 60 Ω,	See Figure 2		35	50	ns
t_{TD}	Differential-output transition time				50	75	ns
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 27 Ω,	See Figure 3		16	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output				44	65	ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω,	See Figure 4		60	80	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω,	See Figure 5		30	45	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω,	See Figure 4		51	75	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω,	See Figure 5		18	30	ns

PARAMETER MEASUREMENT INFORMATION

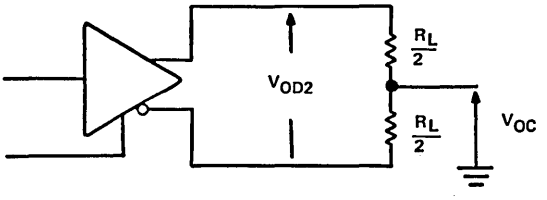
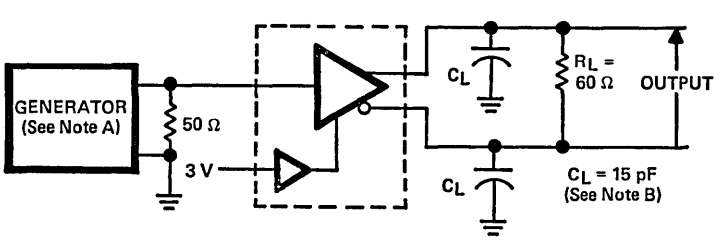
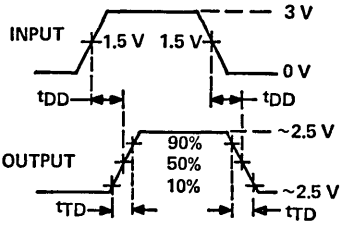


FIGURE 1–DIFFERENTIAL AND COMMON-MODE OUTPUT VOLTAGES



TEST CIRCUIT

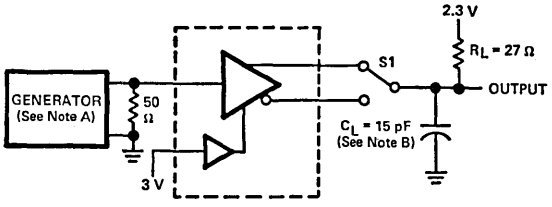


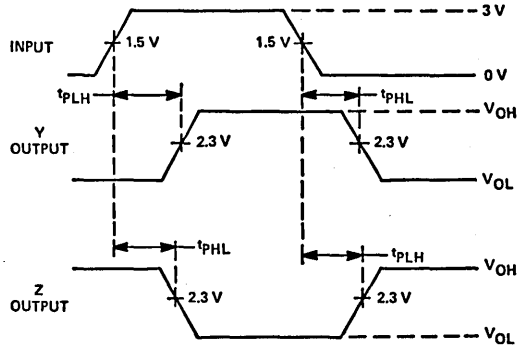
VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: $t_r \leq 5$ ns, $t_f \leq 5$ ns, PRR = 1 MHz, duty cycle = 50%, Z_o = 50 Ω.
B. C_L includes probe and stray capacitance.
C. All diodes are 1N916 or 1N3064.

FIGURE 2–DIFFERENTIAL-OUTPUT DELAY AND TRANSITION TIMES

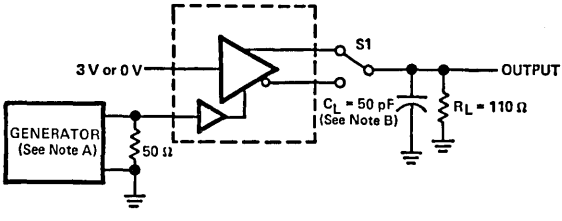
PARAMETER MEASUREMENT INFORMATION

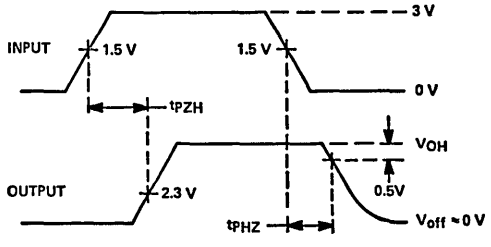




TEST CIRCUIT VOLTAGE WAVEFORMS

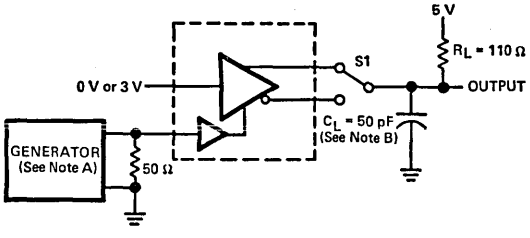
FIGURE 3–PROPAGATION DELAY TIMES

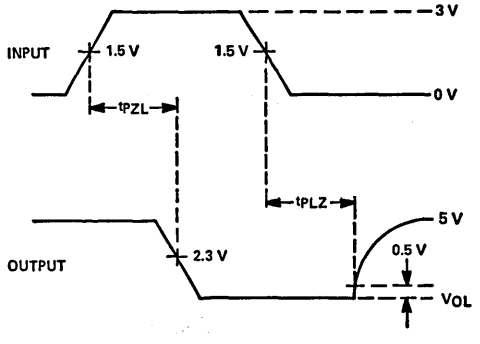




TEST CIRCUIT VOLTAGE WAVEFORMS

FIGURE 4–t_{PZH} AND t_{PHZ}





TEST CIRCUIT VOLTAGE WAVEFORMS

FIGURE 5–t_{PZL} AND t_{PLZ}

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r \leq 5$ ns, $t_f \leq 5$ ns, $Z_o = 50\ \Omega$.

B. C_L includes probe and stray capacitance.

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TYPICAL CHARACTERISTICS

HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

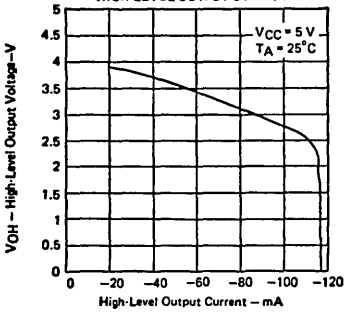


FIGURE 6

LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

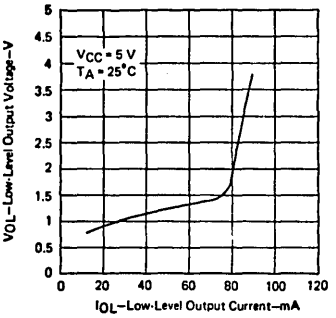


FIGURE 7

DIFFERENTIAL OUTPUT VOLTAGE vs OUTPUT CURRENT

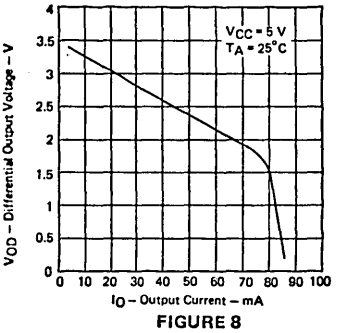


FIGURE 8

OUTPUT CURRENT vs OUTPUT VOLTAGE

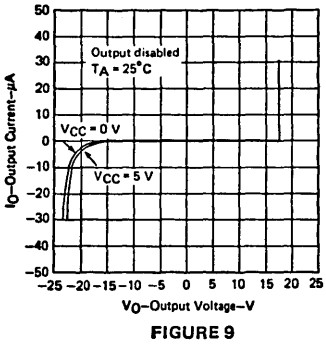


FIGURE 9

SUPPLY CURRENT vs SUPPLY VOLTAGE

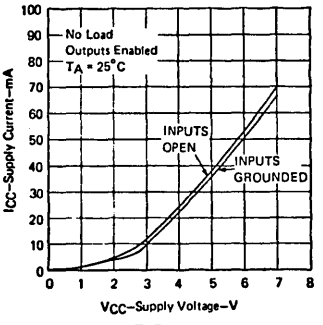


FIGURE 10

SUPPLY CURRENT vs SUPPLY VOLTAGE

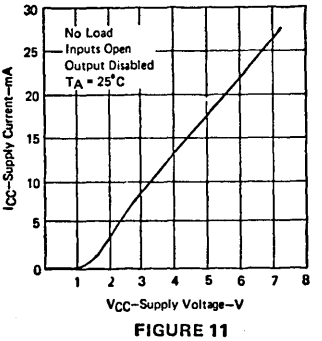
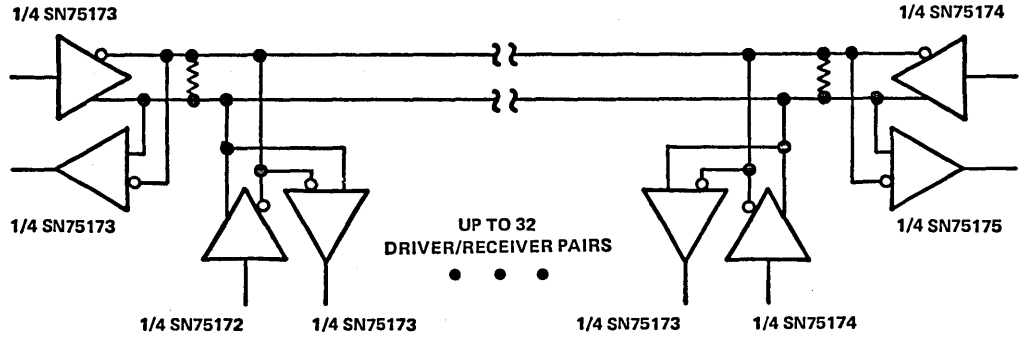


FIGURE 11

TYPICAL APPLICATION



NOTE: The line length should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

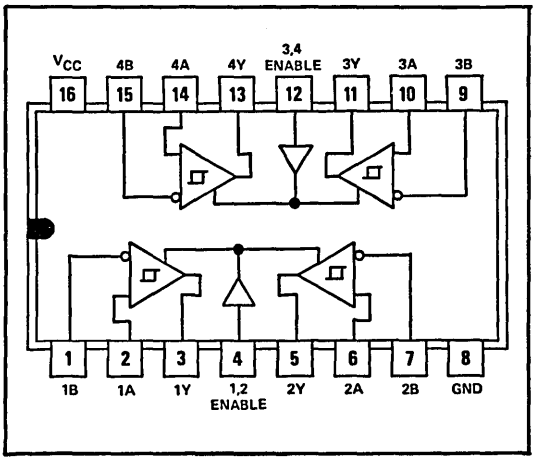
FIGURE 12

TYPE SN75175
QUADRUPLE DIFFERENTIAL LINE RECEIVER

BULLETIN NO. DL-S 12772, OCTOBER 1980

- Meets EIA Standards RS-422A and RS-423A
- Meets CCITT Recommendations V.10, V.11, X.26, and X.27
- Meets EIA Subcommittee TR30.1 Draft Standard PN1360 (as of April 1980)
- Designed for Multipoint Bus Transmission on Long Bus Lines in Noisy Environments
- 3-State Outputs
- Common-Mode Input Voltage Range . . . −12 V to 12 V
- Input Sensitivity . . . ±200 mV
- Input Hysteresis . . . 50 mV Typ
- High Input Impedance . . . 12 kΩ Min
- Operates from Single 5-Volt Supply
- Low Power Requirements
- Plug-In Replacement for MC3486

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



description

The SN75175 is a monolithic quadrupled differential line receiver with three-state outputs. It is designed to meet the requirements of EIA Standards RS-422A and RS-423A and several CCITT recommendations. The device is optimized for balanced multipoint bus transmission at rates up to 10 megabits per second. Each receiver features two active-high enables, each common to two receivers. It also features high input impedance, input hysteresis for increased noise immunity, and input sensitivity of ±200 millivolts over a common-mode input voltage range of −12 volts to 12 volts. The SN75175 is designed for optimum performance when used with the SN75172 or SN75174 quadruple differential line drivers.

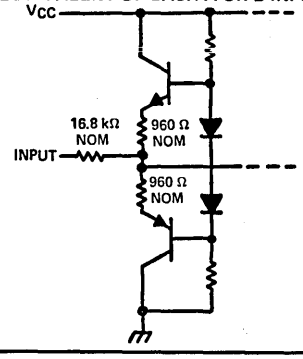
FUNCTION TABLE (EACH RECEIVER)

DIFFERENTIAL INPUTS A − B	ENABLE	OUTPUT Y
$V_{ID} \geq 0.2$ V	H	H
$-0.2\text{ V} < V_{ID} < 0.2$ V	H	?
$V_{ID} \leq -0.2$ V	H	L
X	L	Z

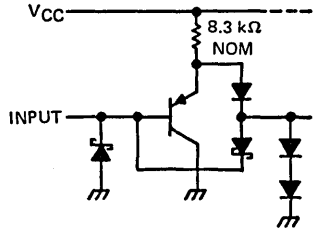
H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

schematics of inputs and outputs

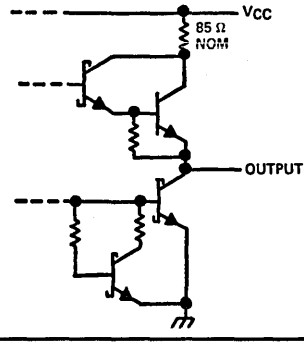
EQUIVALENT OF EACH A OR B INPUT



EQUIVALENT OF EACH ENABLE INPUT



TYPICAL OF ALL OUTPUTS



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage, A or B inputs	±25 V
Differential input voltage (see Note 2)	±25 V
Enable input voltage	7 V
Low-level output current	50 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3): J Package	1025 mW
N Package	1150 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch (1,6 mm) from case for 60 seconds: J Package	300°C
Lead temperature 1/16 inch (1,6 mm) from case for 10 seconds: N Package	260°C

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
2. Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.
3. For operation above 25°C free-air temperature, derate the J package to 656 mW at 70°C at a rate of 8.2 mW/°C and the N package to 736 mW at 70°C at a rate of 9.2 mW/°C. In the J package, SN75175 chips are glass-mounted.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Common-mode input voltage, V_{IC}			±12	V
Differential input voltage, V_{ID}			±12	V
High-level output current, I_{OH}			−400	μA
Low-level output current, I_{OL}			16	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{TH}	Differential-input high-threshold voltage	V_O = 2.7 V, I_O = −0.4 mA				0.2	V
V_{TL}	Differential-input low-threshold voltage	V_O = 0.5 V, I_O = 16 mA		−0.2‡			V
$V_{T+} - V_{T-}$	Hysteresis§				50		mV
V_{IH}	High-level enable input voltage			2			V
V_{IL}	Low-level enable input voltage					0.8	V
V_{IK}	Enable-input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV, I_{OH} = −400 μA, See Figure 1		2.7			V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV, See Figure 1	I_{OL} = 8 mA			0.45	V
			I_{OL} = 16 mA			0.5	
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V				±20	μA
I_I	Line input current	Other input at 0 V, See Note 4	V_I = 12 V			1	mA
			V_I = −7 V			−0.8	
I_{IH}	High-level enable-input current	V_{IH} = 2.7 V				20	μA
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V				−100	μA
r_i	Input resistance			12			kΩ
I_{OS}	Short-circuit output current¶			−15		−85	mA
I_{CC}	Supply current	Outputs disabled				70	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C
‡The algebraic convention, where the less-positive (more-negative) limit is designated as minimum, is used in this data sheet for threshold voltage levels only.
§Hysteresis is the difference between the positive-going input threshold voltage, V_{T+} and the negative-going input threshold voltage, V_{T-}. See Figure 4.
¶Not more than one output should be shorted at a time and the duration of the short-circuit should not exceed one second.
NOTE 4: Refer to EIA standards RS-422A and RS-423A for exact conditions.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF,	See Figure 2		22	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output				25	35	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF,	See Figure 3		13	30	ns
t_{PZL}	Output enable time to low level				19	30	ns
t_{PHZ}	Output disable time from high level	C_L = 5 pF,	See Figure 3		26	35	ns
t_{PLZ}	Output disable time from low level				25	35	ns

PARAMETER MEASUREMENT INFORMATION

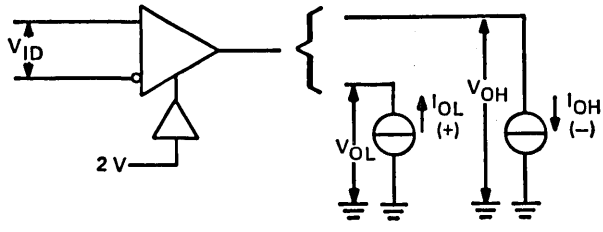
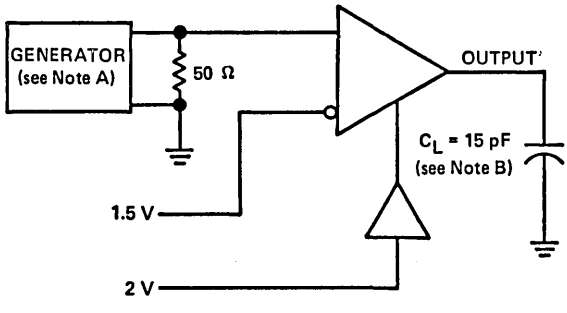
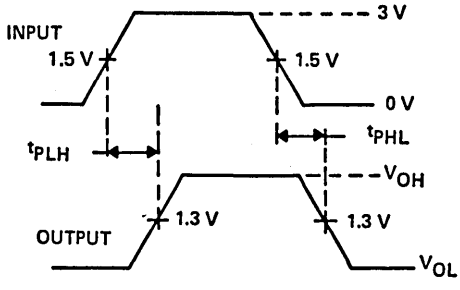


FIGURE 1–V_{OH}, V_{OL}



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 2–PROPAGATION DELAY TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r = t_f$ = 6 ns, Z_{out} = 50 Ω.
B. C_L includes probe and stray capacitance.

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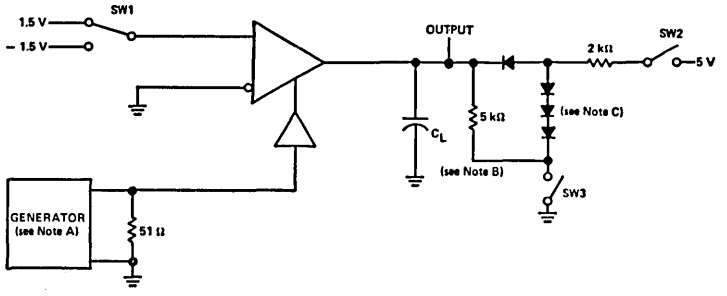
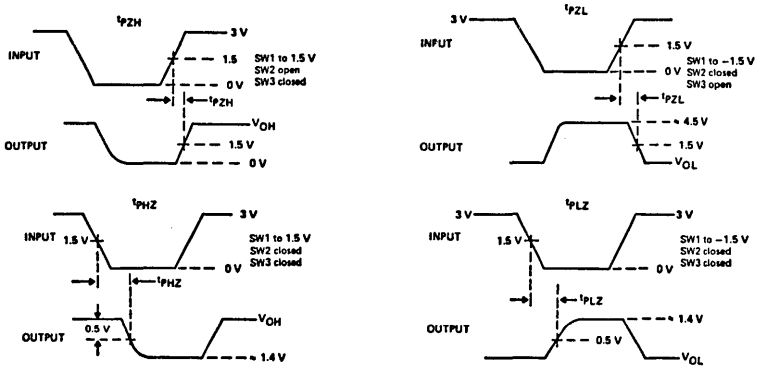
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 3–ENABLE AND DISABLE TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle = 50%, $t_r = t_f = 6$ ns, $Z_{out} = 50\ \Omega$.
B. C_L includes probe and stray capacitance
C. All diodes are 1N916 or equivalent.

TYPICAL CHARACTERISTICS

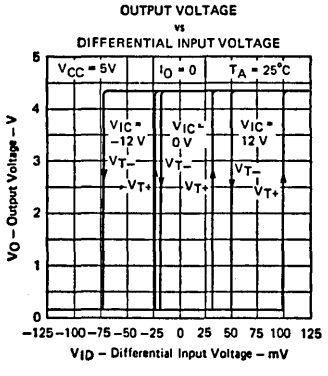


FIGURE 4

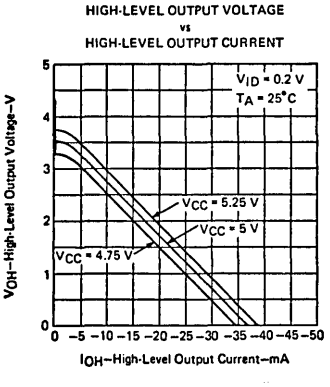


FIGURE 5

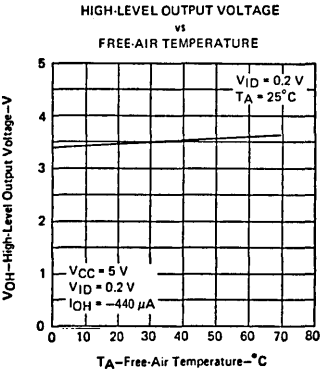


FIGURE 6

TYPICAL CHARACTERISTICS

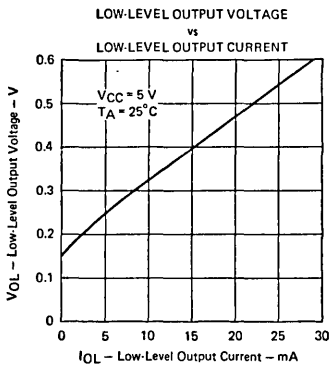


FIGURE 7

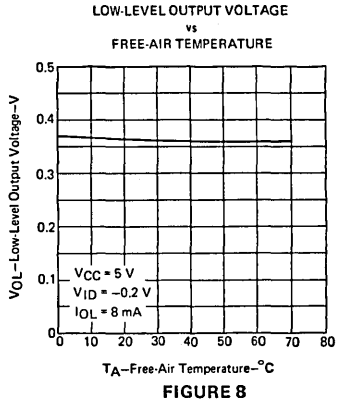


FIGURE 8

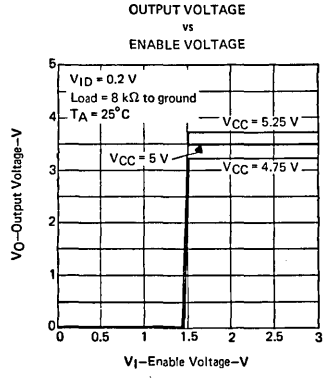


FIGURE 9

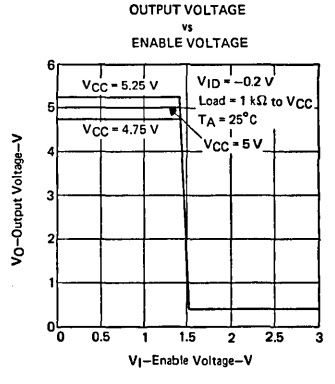


FIGURE 10

TYPICAL APPLICATION

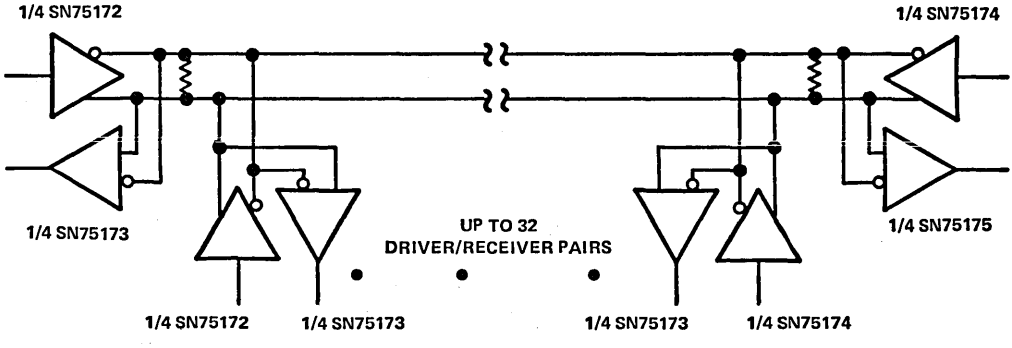


FIGURE 11

NOTE: The line should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

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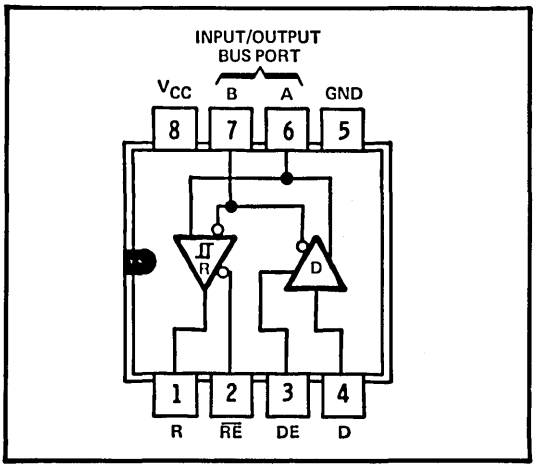
TYPE SN75176 DIFFERENTIAL BUS TRANSCEIVER

BULLETIN NO. DL-S 12790, OCTOBER 1980

- Bidirectional Transceiver
- Meets EIA Standard RS-422A and CCITT Recommendations V.11 and X.27
- Meets EIA Subcommittee TR30.1 Draft Standard PN1360 (as of April 1980)
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- 3-State Driver and Receiver Outputs
- Individual Driver and Receiver Enables
- Wide Positive and Negative Input/Output Bus Voltage Ranges
- Driver Output Capability . . . ± 60 mA Max
- Thermal Shutdown Protection
- Driver Positive and Negative Current Limiting
- Receiver Input Impedance . . . 12 kΩ Min
- Receiver Input Sensitivity . . . ±200 mV
- Receiver Input Hysteresis . . . 50 mV Typ
- Operates from Single 5-Volt Supply
- Low Power Requirements

JG OR P
DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

The SN75176 differential bus transceiver is a monolithic integrated circuit designed for bidirectional data communication on multipoint bus transmission lines. It is designed for balanced transmission lines and meets EIA Standard RS-422A, the EIA Subcommittee TR30.1 Draft Standard PN1360, and CCITT Recommendations V.11 and X.27.

FUNCTION TABLE (DRIVER)

INPUT	ENABLE	OUTPUTS	
D	DE	A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

FUNCTION TABLE (RECEIVER)

DIFFERENTIAL INPUTS	ENABLE	OUTPUT
A − B	$\overline{RE}$	R
$V_{ID} \geq 0.2$ V	L	H
$-0.2\text{ V} < V_{ID} < 0.2$ V	L	?
$V_{ID} \leq -0.2$ V	L	L
X	H	Z

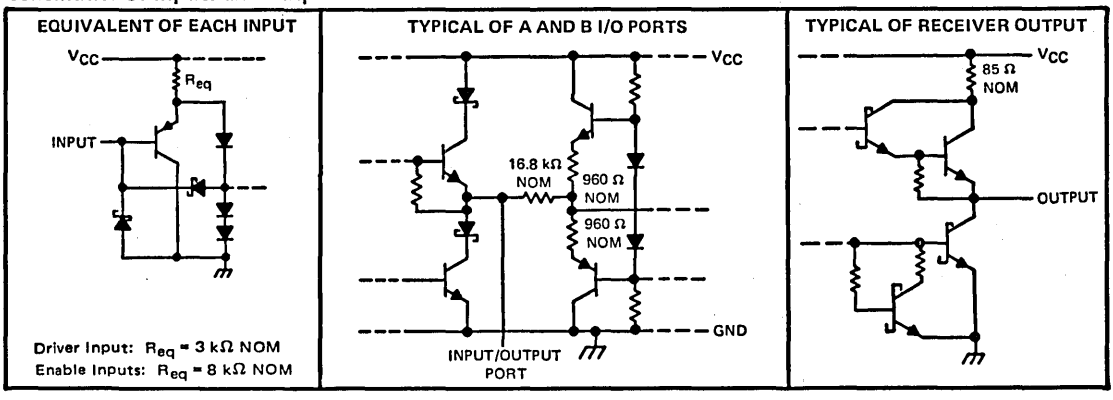
H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

The SN75176 combines a three-state differential line driver and a differential-input line receiver both of which operate from a single 5-volt power supply. The driver and receiver have an active enable that can be externally connected to function as a direction control. The driver differential-outputs and the receiver differential-inputs are internally connected to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus whenever the driver is disabled or V_{CC} = 0 volts. These ports feature wide positive and negative common-mode voltage ranges making the device suitable for party-line applications.

The driver is designed to handle loads up to 60 milliamperes of sink or source current. The driver features positive- and negative-current limiting and thermal shutdown for protection from line fault conditions. Thermal shutdown is designed to occur at a junction temperature of approximately 150°C. The receiver features a minimum input impedance of 12 kΩ, an input sensitivity of ±200 millivolts, and a typical input hysteresis of 50 millivolts.

The SN75176 can be used in transmission line applications employing the SN75172 and SN75174 quadruple differential line drivers and the SN75173 and SN75175 quadruple differential line receivers.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Voltage at any bus terminal . . . . . −10 V to 15 V
Enable input voltage . . . . . 5.5 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2): JG Package . . . . . 825 mW
P Package . . . . . 1000 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch (1,6 mm) from case for 60 seconds: JG Package . . . . . 300°C
Lead temperature 1/16 inch (1,6 mm) from case for 10 seconds: P Package . . . . . 260°C

NOTES: 1. All voltage values, except differential input/output bus voltage, are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, derate the JG package to 528 mW at 70°C at the rate of 6.6 mW/°C and the P package to 640 mW at 70°C at the rate of 8.0 mW/°C. In the JG package, SN75176 chips are glass-mounted.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Voltage at any bus terminal (separately or common-mode), V_I or V_{IC}		−7†		12	V
Differential input voltage, V_{ID} (see Note 3)				±12	V
High-level output current, I_{OH}	Driver			−60	mA
	Receiver			−400	μA
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			16	
Operating free-air temperature, T_A		0		70	°C

†The algebraic convention, where the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

NOTE 3: Differential-input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.

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DRIVER SECTION

driver electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	I_I = −18 mA				−1.5	V
V_{OH}	High-level output voltage	V_{IH} = 2 V, I_{OH} = −33 mA	V_{IL} = 0.8 V,		3.7		V
V_{OL}	Low-level output voltage	V_{IH} = 2 V, I_{OL} = 33 mA	V_{IL} = 0.8 V,		1.1		V
$\lvert V_{OD1}\rvert$	Differential output voltage	I_O = 0				$2V_{OD2}$	V
$\lvert V_{OD2}\rvert$	Differential output voltage	R_L = 100 Ω,	See Figure 9	2	2.7		V
		R_L = 54 Ω,	See Figure 9	1.5	2.4		
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of differential output voltage‡	R_L = 54 Ω or 100 Ω,	See Figure 9			±0.2	V
V_{OC}	Common-mode output voltage§					3	V
$\Delta\lvert V_{OC}\rvert$	Change in magnitude of common-mode output voltage‡					±0.2	V
I_O	Output current	Output disabled, See Note 4	V_O = 12 V			1	mA
			V_O = −7 V			−0.8	
I_{IH}	High-level input current	V_I = 2.4 V				20	μA
I_{IL}	Low-level input current	V_I = 0.4 V				−360	μA
I_{OS}	Short-circuit output current	V_O = −7 V				−180	mA
		V_O = V_{CC}				180	
		V_O = 12 V				500	
I_{CC}	Supply current (total package)	No load	Outputs enabled			35	mA
			Outputs disabled			30	

†All typical values are at V_{CC} = 5 V and T_A = 25°C.
‡$\Delta\lvert V_{OD}\rvert$ and $\Delta\lvert V_{OC}\rvert$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
§In EIA Standard RS-422A, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.
NOTE 4: This applies for both power on and power off. Refer to EIA Standard RS-422A for exact conditions.

driver switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{DD}	Differential-output delay time	R_L = 60 Ω,	See Figure 11		35	50	ns
t_{TD}	Differential-output transition time				50	75	ns
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 27 Ω,	See Figure 12		16	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output				44	65	ns
t_{PZH}	Output enable time to high level	R_L = 110 Ω,	See Figure 13		60	80	ns
t_{PZL}	Output enable time to low level	R_L = 110 Ω,	See Figure 14		30	45	ns
t_{PHZ}	Output disable time from high level	R_L = 110 Ω,	See Figure 13		51	75	ns
t_{PLZ}	Output disable time from low level	R_L = 110 Ω,	See Figure 14		18	30	ns

RECEIVER SECTION

receiver electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{TH}	Differential-input high-threshold voltage	V_O = 2.7 V,	I_O = −0.4 mA				0.2	V
V_{TL}	Differential-input low-threshold voltage	V_O = 0.5 V,	I_O = 8 mA		−0.2¶			V
$V_{T+} - V_{T-}$	Hysteresis§					50		mV
V_{IH}	High-level enable input voltage				2			V
V_{IL}	Low-level enable input voltage						0.8	V
V_{IK}	Enable-input clamp voltage	I_I = −18 mA					−1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV,	I_{OH} = −400 μA, See Figure 10		2.7			V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV, See Figure 10		I_{OL} = 8 mA			0.45	V
				I_{OL} = 16 mA			0.5	
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V					±20	μA
I_I	Line input current	Other input = 0 V, See Note 4		V_I = 12 V			1	mA
				V_I = −7 V			−0.8	
I_{IH}	High-level enable-input current	V_{IH} = 2.7 V					20	μA
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V					−100	μA
r_i	Input resistance				12			kΩ
I_{OS}	Short-circuit output current				−15		−85	mA
I_{CC}	Supply current (total package)	No load		Outputs enabled			35	mA
				Outputs disabled			30	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

¶The algebraic convention, where the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

§Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}. See Figure 4.

NOTE 4: This applies for both power on and power off. Refer to EIA Standard RS-422A for exact conditions.

receiver switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = −2.5 V to 2.5 V,			26	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 15 pF,	See Figure 15		27	35	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF,	See Figure 16		13	30	ns
t_{PZL}	Output enable time to low level				19	30	ns
t_{PHZ}	Output disable time from high level	C_L = 5 pF,	See Figure 16		26	35	ns
t_{PLZ}	Output disable time from low level				27	35	ns

TYPICAL CHARACTERISTICS

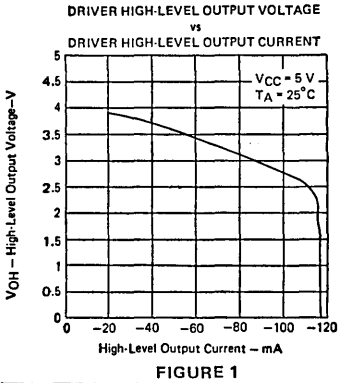

FIGURE 1

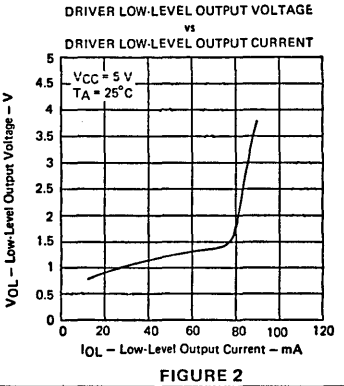

FIGURE 2

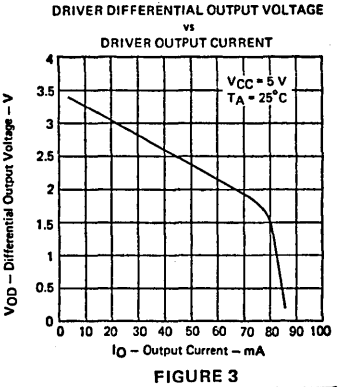

FIGURE 3

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TYPICAL CHARACTERISTICS

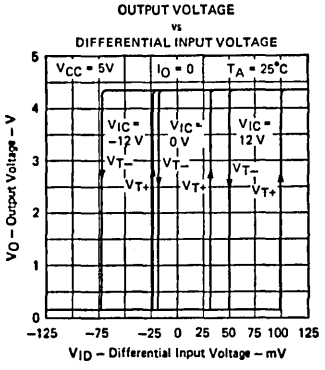


FIGURE 4

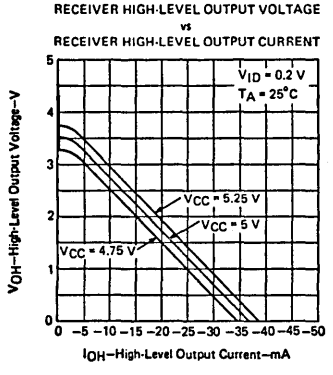


FIGURE 5

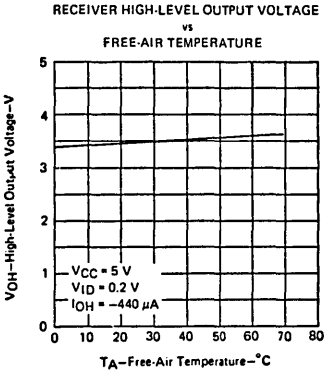


FIGURE 6

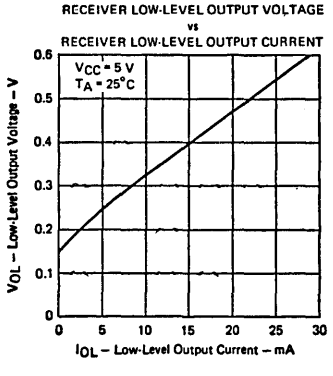


FIGURE 7

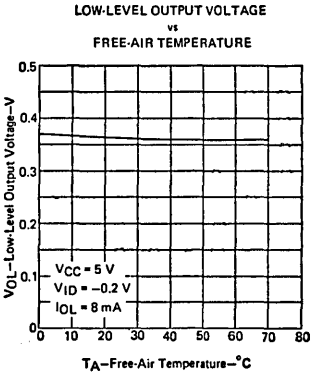


FIGURE 8

PARAMETER MEASUREMENT INFORMATION

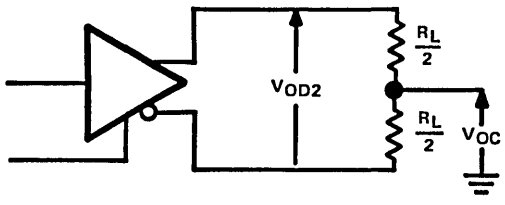


FIGURE 9–DRIVER V_{OD} AND V_{OC}

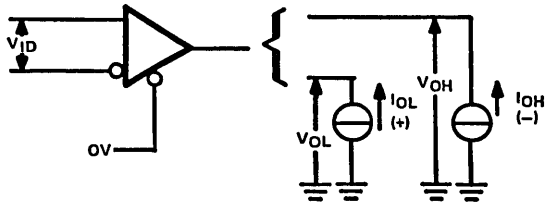
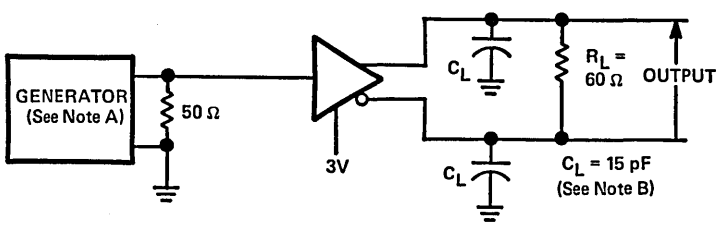
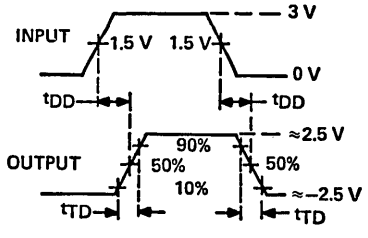


FIGURE 10–RECEIVER V_{OH} AND V_{OL}

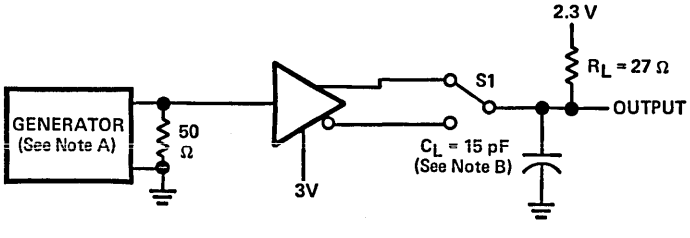


TEST CIRCUIT

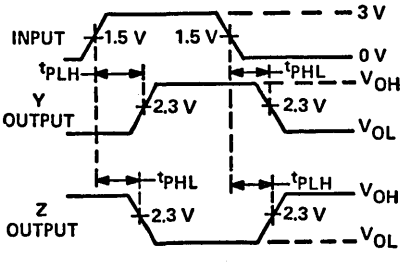


VOLTAGE WAVEFORMS

FIGURE 11–DRIVER DIFFERENTIAL-OUTPUT DELAY AND TRANSITION TIMES



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 12–DRIVER PROPAGATION TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_{out} = 50\ \Omega$.
B. C_L includes probe and jig capacitance.

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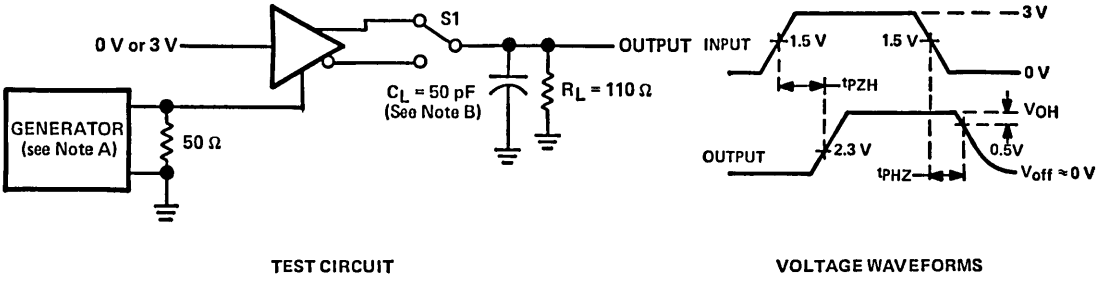
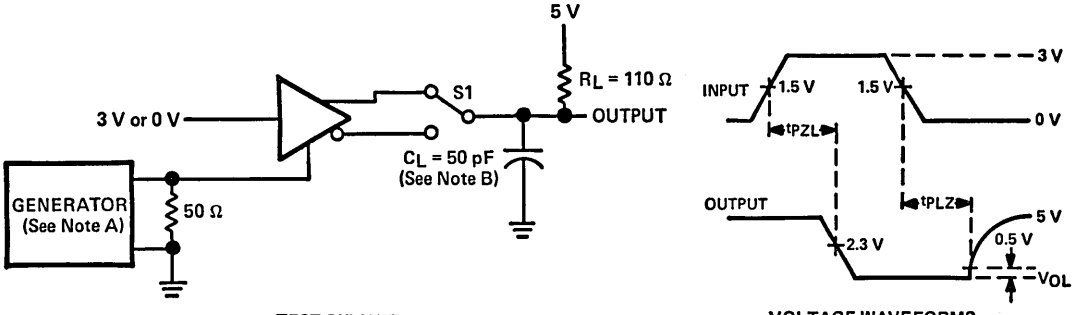
PARAMETER MEASUREMENT INFORMATION



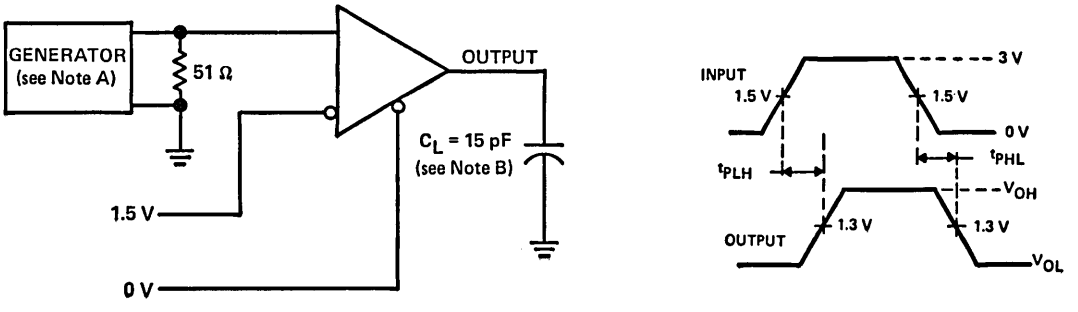
TEST CIRCUIT VOLTAGE WAVEFORMS

FIGURE 13–DRIVER ENABLE AND DISABLE TIMES



TEST CIRCUIT VOLTAGE WAVEFORMS

FIGURE 14–DRIVER ENABLE AND DISABLE TIMES

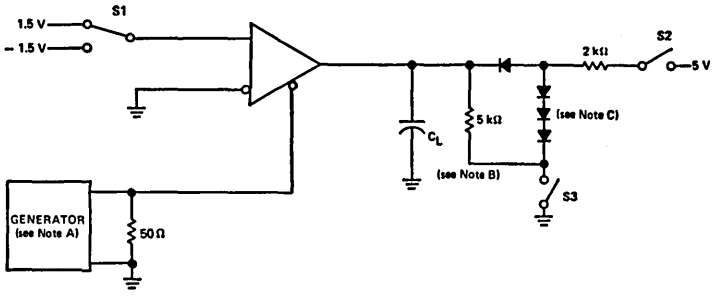


TEST CIRCUIT VOLTAGE WAVEFORMS

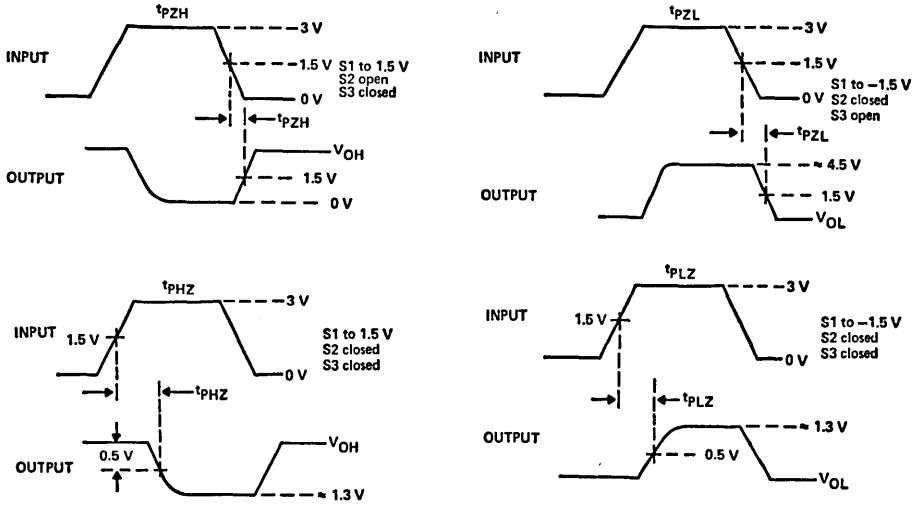
FIGURE 15–RECEIVER PROPAGATION DELAY TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_{out} = 50\ \Omega$.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

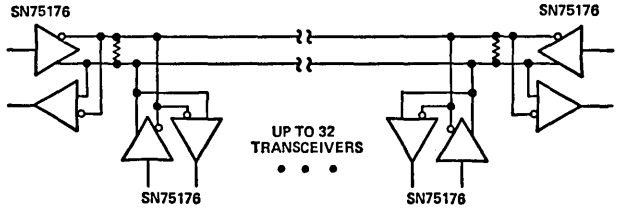


VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle ≈ 50%, $t_r = t_f = 6$ ns.
B. C_L includes probe and stray capacitance.
C. All diodes are 1N916 or equivalent.

FIGURE 16–RECEIVER ENABLE AND DISABLE TIMES

TYPICAL APPLICATION



NOTE: The line length should be terminated at both ends in its characteristic impedance. Stubs lengths off the mainline should be kept as short as possible.

FIGURE 17

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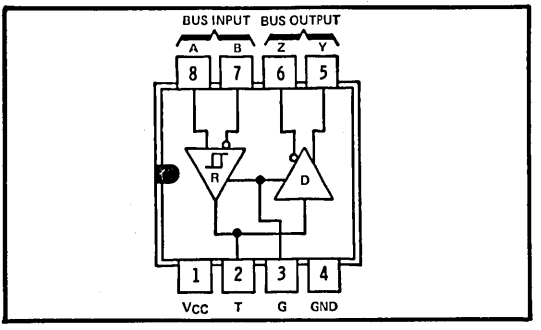
TYPES SN75177, SN75178 DIFFERENTIAL BUS REPEATERS

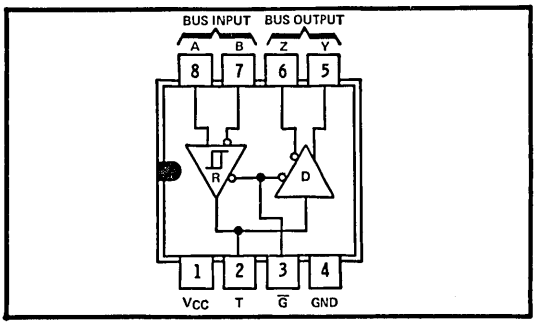
BULLETIN NO. DL-S 12793, OCTOBER 1980

- Meets EIA Standard RS-422A and CCITT Recommendations V.11 and X.27
- Meets EIA Subcommittee TR30.1 Draft Standard PN1360 (as of April 1980)
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- 3-State Outputs
- Bus Voltage Range . . . –7 V to 12 V
- Positive and Negative Current Limiting
- Driver Output Capability . . . 60 mA Max
- Driver Thermal Shutdown Protection
- Receiver Input Impedance . . . 12 kΩ Min
- Receiver Input Sensitivity . . . ±200 mV
- Receiver Input Hysteresis . . . 50 mV Typ
- Operates from Single 5-Volt Supply
- Low Power Requirements

SN75177 . . . JG or P
DUAL-IN-LINE PACKAGE
(TOP VIEW)



SN75178 . . . JG or P
DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

The SN75177 and SN75178 differential bus repeaters are monolithic integrated devices each designed for one-way data communication on multipoint bus transmission lines. These devices are designed for balanced transmission bus line applications and meet EIA Standard RS-422A, EIA Subcommittee TR30.1 draft Standard PN1360, and CCITT Recommendations V.11 and X.27. Each device is designed to improve the performance of the data communication over long bus lines. The SN75177 and SN75178 are identical except for the enable inputs, which are complementary, that is, on the SN75177 it is active-high and on the SN75178 it is active-low. These complementary enables allow the devices to be used in pairs for bidirectional communication.

The SN75177 and SN75178 feature positive- and negative-current limiting and three-state outputs for the receiver and driver. The receiver features high input impedance, input hysteresis for increased noise immunity, and input sensitivity of ±200 millivolts over a common-mode input voltage range of –12 volts to 12 volts. The driver features thermal shutdown for protection from line fault conditions. Thermal shutdown is designed to occur at a junction temperature of approximately 150° C. The driver is designed to drive current loads up to 60 milliamperes maximum.

SN75177 FUNCTION TABLE

DIFFERENTIAL INPUTS	ENABLE	OUTPUTS		
A–B	G	T	Y	Z
$V_{ID} \geq 0.2$ V	H	H	H	L
$-0.2\text{ V} < V_{ID} < 0.2$ V	H	?	?	?
$V_{ID} \leq 0.2$ V	H	L	L	H
X	L	Z	Z	Z

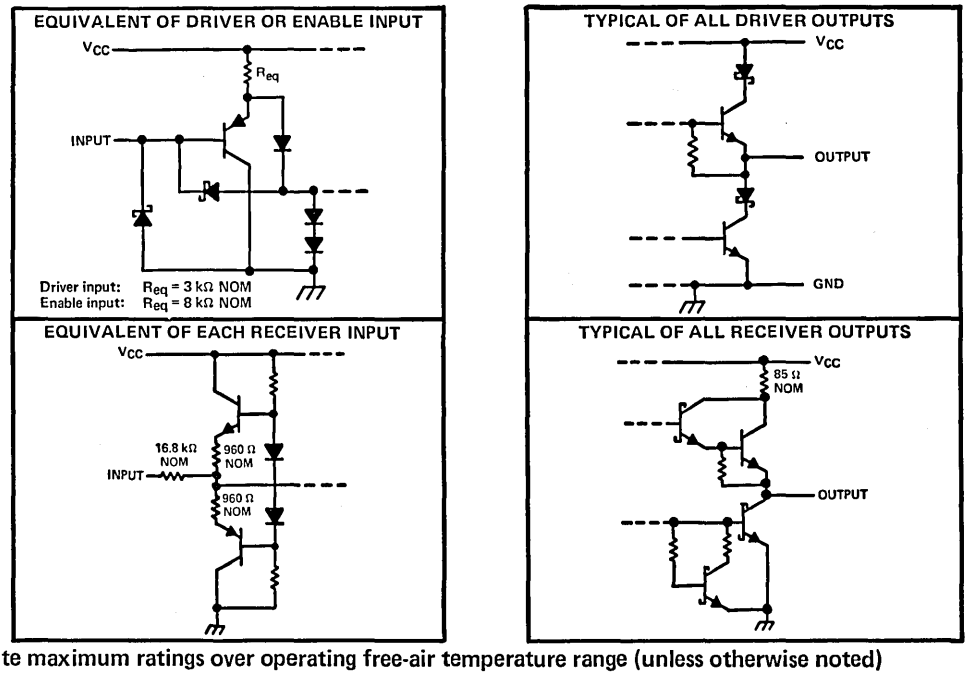
SN75178 FUNCTION TABLE

DIFFERENTIAL INPUTS	ENABLE	OUTPUTS		
A–B	$\overline{G}$	T	Y	Z
$V_{ID} \geq 0.2$ V	L	H	H	L
$-0.2\text{ V} < V_{ID} < 0.2$ V	L	?	?	?
$V_{ID} \leq 0.2$ V	L	L	L	H
X	H	Z	Z	Z

H = high level, L = low level, ? = indeterminate,
X = irrelevant, Z = high impedance (off)

The SN75177 and SN75178 are designed for optimum performance when used on transmission buses employing the SN75172 and SN75174 differential line drivers, SN75173 and SN75175 differential line receivers, or SN75176 differential bus transceiver.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Voltage at any bus terminal . . . . . −10 V to 15 V
Differential input voltage (see Note 2) . . . . . ±25 V
Enable input voltage . . . . . 5.5 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3): JG Package . . . . . 830 mW
P Package . . . . . 1000 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch (1,6 mm) from case for 60 seconds: JG Package . . . . . 300°C
Lead temperature 1/16 inch (1,6 mm) from case for 10 seconds: P Package . . . . . 260°C

NOTES: 1. All voltage values, except differential input voltage, are with respect to network ground terminal.
2. Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.
3. For operation above 25° C free-air temperature, derate the JG package to 528 mW at 70° C at the rate of 6.6 mW/° C and the P package to 640 mW at 70° C at the rate of 8.0 mW/°C. In the JG package, SN75177 and SN75178 chips are glass-mounted.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Common-mode input voltage, V_{IC}		−7†		12	V
Differential input voltage, V_{ID}				±12	V
High-level output current, I_{OH}	Driver			−60	mA
	Receiver			−400	μA
Low-level output current, I_{OL}	Driver			60	mA
	Receiver			16	
Operating free-air temperature, T_A		0		70	°C

†The algebraic convention, where the less-positive (more-negative) limit is designated minimum, is used in his data sheet for common-mode input voltage and threshold voltage.

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DRIVER SECTION

driver electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	$I_I = -18$ mA				−1.5	V
V_{OH}	High-level output voltage	$V_{IH} = 2$ V, $I_{OH} = -33$ mA	$V_{IL} = 0.8$ V,		3.7		V
V_{OL}	Low-level output voltage	$V_{IH} = 2$ V, $I_{OL} = 33$ mA	$V_{IL} = 0.8$ V,		1.1		V
$\lvert V_{OD1} \rvert$	Differential output voltage	$I_O = 0$				$2V_{OD2}$	V
$\lvert V_{OD2} \rvert$	Differential output voltage	$R_L = 100\ \Omega$,	See Figure 9	2	2.7		V
		$R_L = 54\ \Omega$,	See Figure 9	1.5	2.4		
$\Delta\lvert V_{OD} \rvert$	Change in magnitude of differential output voltage‡	$R_L = 54\ \Omega$ or $100\ \Omega$,	See Figure 9			±0.2	V
V_{OC}	Common-mode output voltage§					3	V
$\Delta\lvert V_{OC} \rvert$	Change in magnitude of common-mode output voltage‡					±0.2	V
I_O	Output current with power off	$V_{CC} = 0$,	$V_O = -7$ V to 12			±100	μA
I_{OZ}	High-impedance-state output current	$V_O = -7$ V to 12 V				±100	μA
I_{IH}	High-level input current	$V_I = 2.4$ V				20	μA
I_{IL}	Low-level input current	$V_I = 0.4$ V				−360	μA
I_{OS}	Short-circuit output current	$V_O = -7$ V				−180	mA
		$V_O = V_{CC}$				180	
		$V_O = 12$ V				500	
I_{CC}	Supply current (total package)	No load	Outputs enabled			35	mA
			Outputs disabled			30	

†All typical values are at $V_{CC} = 5$ V and $T_A = 25°C$.
‡$\Delta\lvert V_{OD} \rvert$ and $\Delta\lvert V_{OC} \rvert$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
§In EIA Standard RS-422A, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.

driver switching characteristics, $V_{CC} = 5$ V, $T_A = 25°C$

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{DD}	Differential-output delay time	$R_L = 60\ \Omega$,	See Figure 11		35	50	ns
t_{TD}	Differential-output transition time				50	75	ns
t_{PLH}	Propagation delay time, low-to-high-level output	$R_L = 27\ \Omega$,	See Figure 12		16	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output				44	65	ns
t_{PZH}	Output enable time to high level	$R_L = 110\ \Omega$,	See Figure 13		60	80	ns
t_{PZL}	Output enable time to low level	$R_L = 110\ \Omega$,	See Figure 14		30	45	ns
t_{PHZ}	Output disable time from high level	$R_L = 110\ \Omega$,	See Figure 13		51	75	ns
t_{PLZ}	Output disable time from low level	$R_L = 110\ \Omega$,	See Figure 14		18	30	ns

RECEIVER SECTION

receiver electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{TH}	Differential-input high-threshold voltage	V_O = 2.7 V,	I_O = −0.4 mA				0.2	V
V_{TL}	Differential-input low-threshold voltage	V_O = 0.5 V,	I_O = 8 mA		−0.2¶			V
$V_{T+} - V_{T-}$	Hysteresis§					50		mV
V_{IH}	High-level enable input voltage				2			V
V_{IL}	Low-level enable input voltage						0.8	V
V_{IK}	Enable-input clamp voltage	I_I = −18 mA					−1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV,	I_{OH} = −400 μA, See Figure 10		2.7			V
V_{OL}	Low-level output voltage	V_{ID} = −200 mV, See Figure 10		I_{OL} = 8 mA			0.45	V
				I_{OL} = 16 mA			0.5	
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V					20	μA
							−360	
I_I	Line input current	Other input at 0 V, See Note 4		V_I = 12 V			1	mA
				V_I = −7 V			−0.8	
I_{IH}	High-level enable-input current	V_{IH} = 2.7 V					20	μA
I_{IL}	Low-level enable-input current	V_{IL} = 0.4 V					−100	μA
r_i	Input resistance				12			kΩ
I_{OS}	Short-circuit output current				−15		−85	mA
I_{CC}	Supply current (total package)	No load		Outputs enabled			35	mA
				Outputs disabled			30	

†All typical values are at V_{CC} = 5 V, T_A = 25°C.

¶The algebraic convention, where the less-positive (more-negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

§Hysteresis is the difference between the positive-going input threshold voltage, V_{T+}, and the negative-going input threshold voltage, V_{T-}. See Figure 4.

NOTE 4: Refer to EIA standard RS-422A for exact conditions

receiver switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = −2.5 V to 2.5 V,			26	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 15 pF,	See Figure 15		27	35	ns
t_{PZH}	Output enable time to high level	C_L = 15 pF,	See Figure 16		13	30	ns
t_{PZL}	Output enable time to low level				19	30	ns
t_{PHZ}	Output disable time from high level	C_L = 5 pF,	See Figure 16		26	35	ns
t_{PLZ}	Output disable time from low level				27	35	ns

TYPICAL CHARACTERISTICS

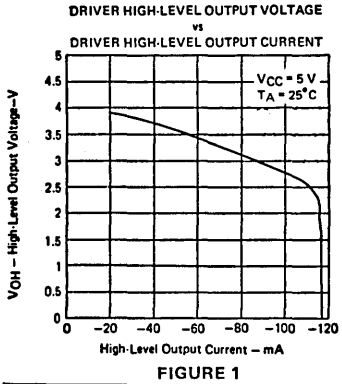

FIGURE 1

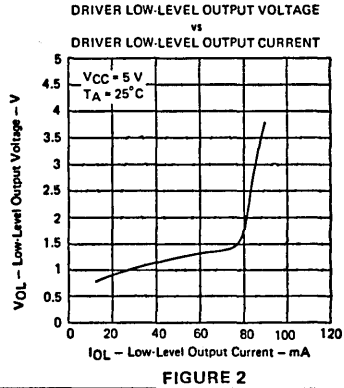

FIGURE 2

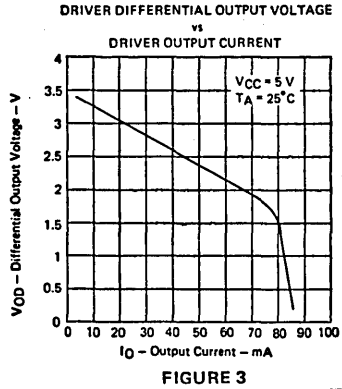

FIGURE 3

TEXAS INSTRUMENTS
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TYPICAL CHARACTERISTICS

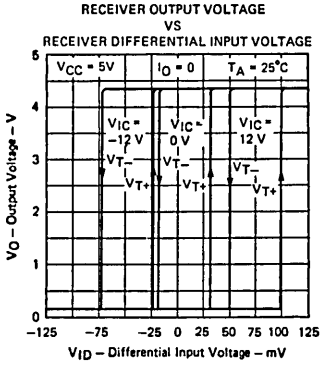


FIGURE 4

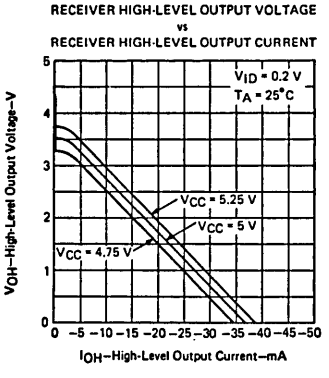


FIGURE 5

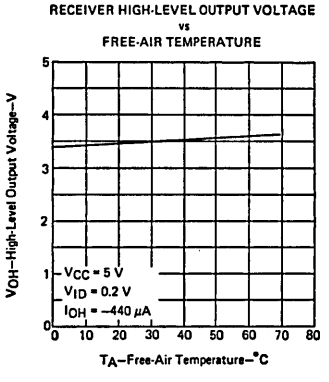


FIGURE 6

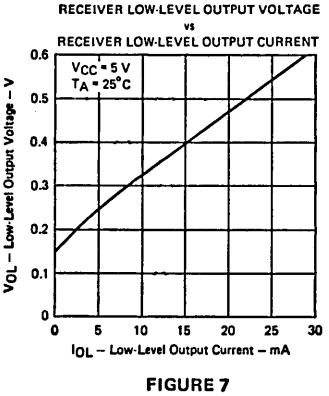


FIGURE 7

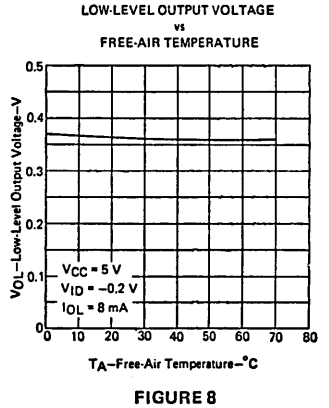


FIGURE 8

PARAMETER MEASUREMENT INFORMATION

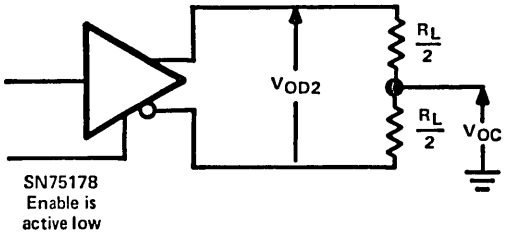


FIGURE 9–DRIVER V_{OD} AND V_{OC}

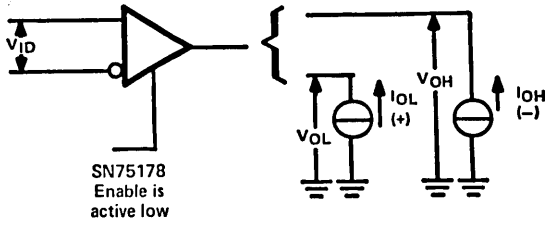
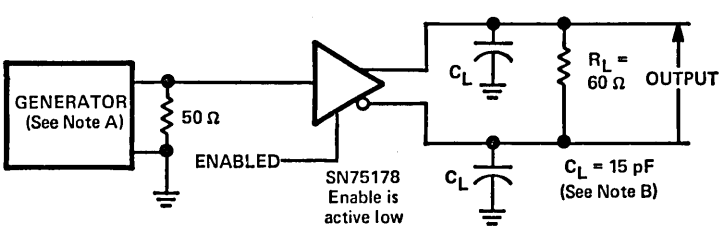
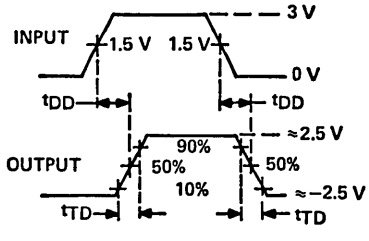


FIGURE 10–RECEIVER V_{OH} AND V_{OL}

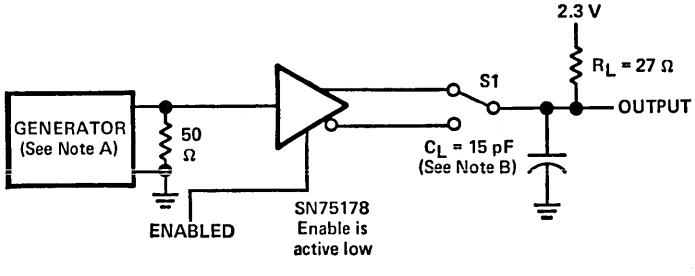


TEST CIRCUIT

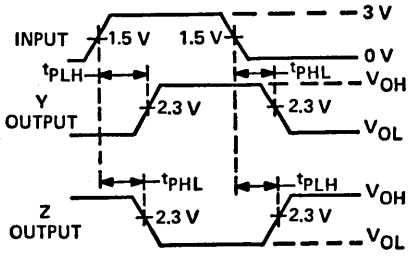


VOLTAGE WAVEFORMS

FIGURE 11–DRIVER DIFFERENTIAL-OUTPUT DELAY AND TRANSITION TIMES



TEST CIRCUIT



VOLTAGE WAVEFORMS

FIGURE 12–DRIVER PROPAGATION TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_{out} = 50\ \Omega$.
B. C_L includes probe and jig capacitance.

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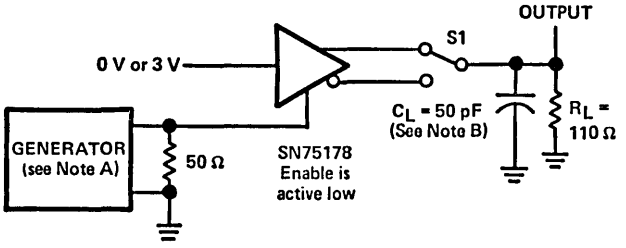
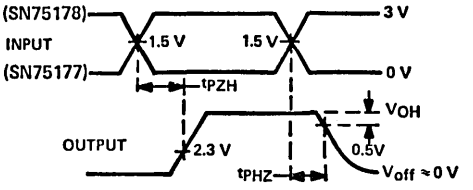
PARAMETER MEASUREMENT INFORMATION

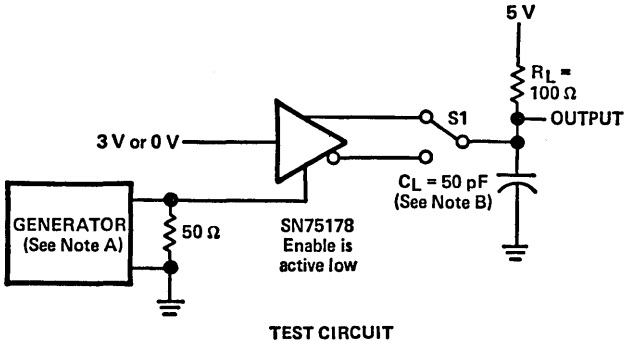


TEST CIRCUIT

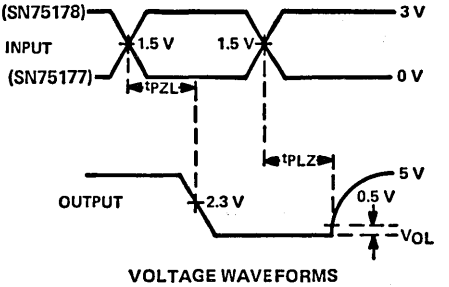


VOLTAGE WAVEFORMS

FIGURE 13–DRIVER ENABLE AND DISABLE TIMES (t_{PZH}, t_{PHZ})

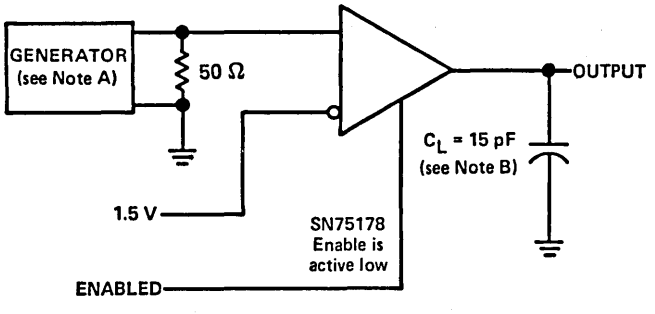


TEST CIRCUIT

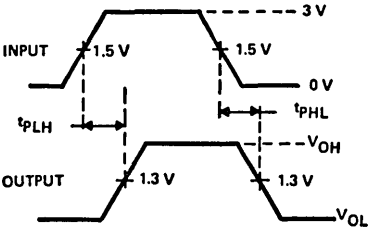


VOLTAGE WAVEFORMS

FIGURE 14–DRIVER ENABLE AND DISABLE TIMES (t_{PZL}, t_{PLZ})



TEST CIRCUIT

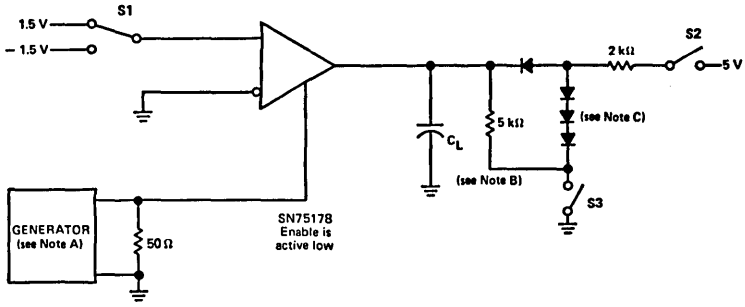


VOLTAGE WAVEFORMS

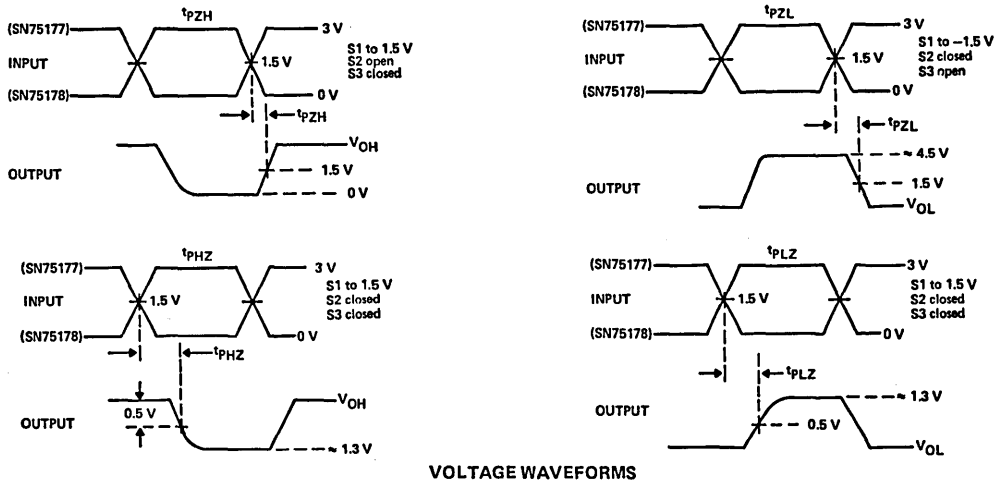
FIGURE 15–RECEIVER PROPAGATION DELAY TIMES

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_{out} = 50\ \Omega$.
B. C_L includes probe and jig capacitance.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT

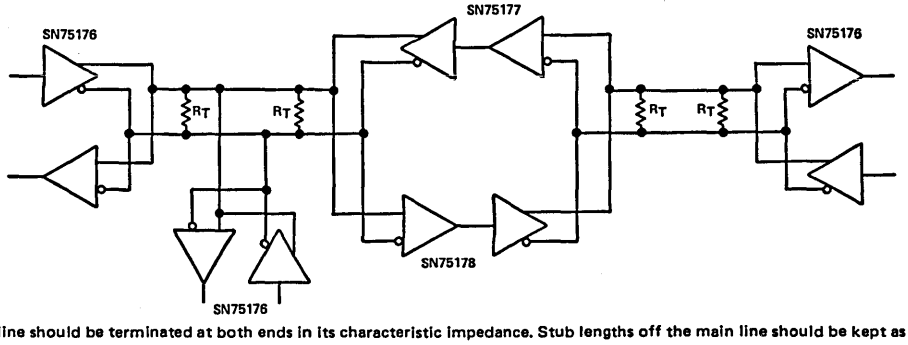


VOLTAGE WAVEFORMS

NOTES: A. The input pulse is supplied by a generator having the following characteristics: PRR = 1 MHz, duty cycle ≈ 50%, $t_r = t_f = 6$ ns.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916 or equivalent.

FIGURE 17–RECEIVER ENABLE AND DISABLE TIMES

TYPICAL APPLICATION



NOTE: The line should be terminated at both ends in its characteristic impedance. Stub lengths off the main line should be kept as short as possible.

FIGURE 18

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TYPES SN55182, SN75182, SN55183, SN75183
DUAL DIFFERENTIAL RECEIVERS AND DRIVERS

BULLETIN NO. DL-S 11767, OCTOBER 1972—REVISED JANUARY 1977

LINE CIRCUITS
featuring

- Single 5-V Supply
- Differential Line Operation
- Dual Channels
- TTL/DTL Compatibility

additional features of SN55182 and SN75182 line receivers

- Designed to be Interchangeable with National Semiconductor DS7820A and DS8820A
- ±15 V Common-Mode Input Voltage Range
- ±15 V Differential Input Voltage Range
- Individual Channel Strobes
- Built-In Optional Line-Termination Resistor
- Individual Frequency Response Controls

additional features of SN55183 and SN75183 line drivers

- Designed to be Interchangeable with National Semiconductor DS7830 and DS8830
- Short-circuit Protection of Outputs
- Output Clamp Diodes to Terminate Line Transients
- High-Current Outputs
- Quad Inputs
- Single-Ended or Differential AND/NAND Outputs

description

The SN55182 and SN75182 dual differential line receivers are designed to sense small differential signals in the presence of large common-mode noise. These devices give TTL compatible output signals as a function of the polarity of the differential input voltage. The frequency response of each channel may be easily controlled by a single external capacitor to provide immunity to differential noise spikes. The output goes to a high level when the inputs are open-circuited. A strobe input is provided which, when in the low level, disables the receiver and forces the output to a high level.

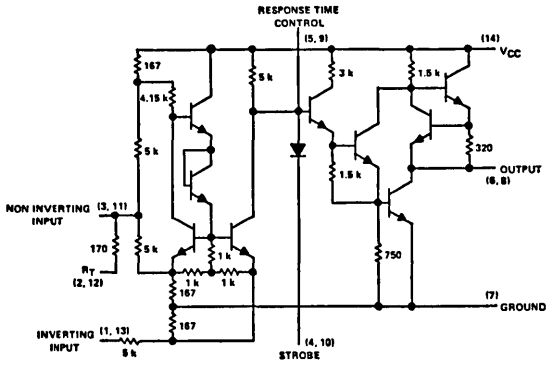
The SN55183 and SN75183 dual differential line drivers are designed to provide differential output signals with high-current capability for driving balanced lines, such as twisted-pair, at normal line impedances without high power dissipation. These devices may be used as TTL expander/phase splitters as the output stages are similar to TTL totem-pole outputs.

Both the driver and receiver are of monolithic single-chip construction, and both halves of the dual circuits use common power supply and ground terminals.

The SN55182 and SN55183 are characterized for operation over the full military temperature range of −55°C to 125°C and the SN75182 and SN75183 are characterized for operation from 0°C to 70°C. Both devices are available in either the ceramic (J) or plastic (N) dual-in-line package.

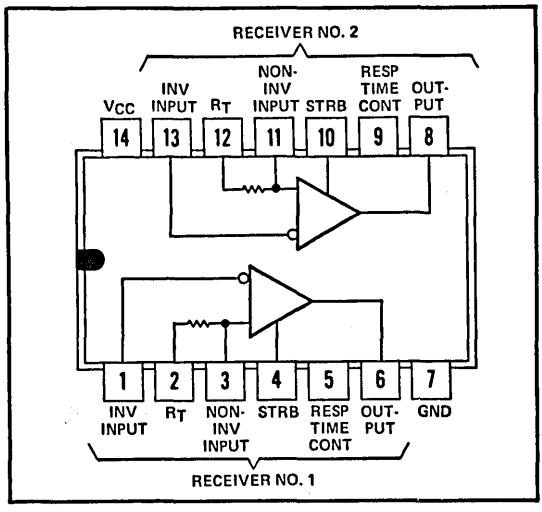
CONTENTS

schematic (each receiver)



Resistor values shown are nominal and in ohms.

J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



logic

FUNCTION TABLE

STROBE	DIFF INPUT	OUTPUT
L	X	H
H	H	H
H	L	L

H = $V_I \geq V_{IH}$ min or V_{ID} more positive than V_{TH} max
L = $V_I \leq V_{IL}$ max or V_{ID} more negative than V_{TL} max
X = irrelevant

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	8 V
Common-mode input voltage	±20 V
Differential input voltage (see Note 2)	±20 V
Strobe input voltage	8 V
Output sink current	50 mA
Continuous total dissipation at (or below) 70°C free-air temperature (see Note 3)	600 mW
Operating free-air temperature range: SN55182	−55°C to 125°C
SN75182	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N package	260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to the network ground terminal.
2. Differential voltage values are at the noninverting terminal with respect to the inverting terminal.
3. For operation of SN55182 above 70°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 21. In the J package, these chips are glass-mounted.

recommended operating conditions

	SN55182			SN75182			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.5	5	5.5	V
Common-mode input voltage, V_{IC}			±15			±15	
High-level output current, I_{OH}			−400			−400	μA
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

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electrical characteristics over recommended ranges of V_{CC}, V_{IC}, and operating free-air temperature (unless otherwise noted)

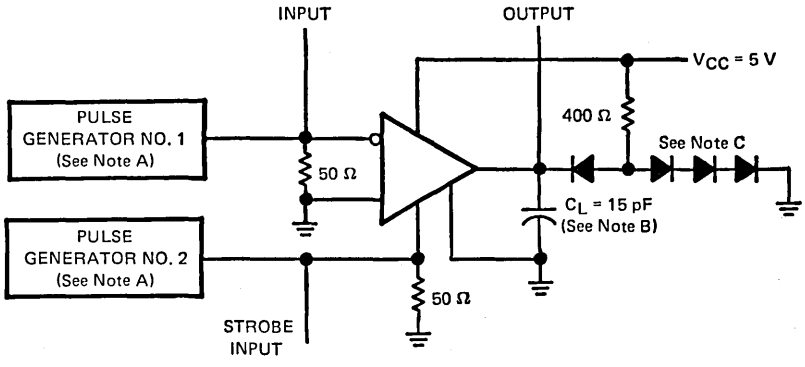
PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{TH}	Differential input high-threshold voltage		V_O = 2.5 V, I_{OH} = −400 μA	V_{IC} = −3 V to 3 V			0.5	V
				V_{IC} = −15 V to 15 V			1	
V_{TL}	Differential input low-threshold voltage		V_O = 0.4 V, I_{OL} = 16 mA,	V_{IC} = −3 V to 3 V			−0.5	V
				V_{IC} = −15 V to 15 V			−1	
$V_{IH(strobe)}$	High-level strobe input voltage				2.1		5.5	V
$V_{IL(strobe)}$	Low-level strobe input voltage				0		0.9	V
V_{OH}	High-level output voltage		V_{ID} = 1 V, I_{OH} = −400 μA	V_{strobe} = 2.1 V,	2.5	4.2	5.5	V
			V_{ID} = −1 V, I_{OH} = −400 μA	V_{strobe} = 0.4 V,	2.5	4.2	5.5	
V_{OL}	Low-level output voltage		V_{ID} = −1 V, I_{OL} = 16 mA	V_{strobe} = 2.1 V,		0.25	0.4	V
I_I	Input current	Inverting input	V_{IC} = 15 V			3	4.2	mA
			V_{IC} = 0 V			0	0.5	
			V_{IC} = −15 V			−3	−4.2	
		Noninverting input	V_{IC} = 15 V			5	7	mA
			V_{IC} = 0 V			−1	−1.4	
			V_{IC} = −15 V			−7	−9.8	
I_{SH}	High-level strobe current		V_{strobe} = 5.5 V				5	μA
I_{SL}	Low-level strobe current		V_{strobe} = 0			−1	−1.4	mA
r_i	Input resistance	Inverting input			3.6	5		kΩ
		Noninverting input			1.8	2.5		kΩ
R_T	Line terminating resistance		T_A = 25°C		120	170	250	Ω
I_{OS}	Short-circuit output current		V_{CC} = 5.5 V,	V_O = 0	−2.8	−4.5	−6.7	mA
I_{CC}	Supply current (average per receiver)		V_{IC} = 15 V,	V_{ID} = −1 V		4.2	6	mA
			V_{IC} = 0,	V_{ID} = −0.5 V		6.8	10.2	
			V_{IC} = −15 V,	V_{ID} = −1 V		9.4	14	

†Unless otherwise noted, $V_{strobe} \geq 2.1$ V or open.
‡All typical values are at V_{CC} = 5 V, V_{IC} = 0, and T_A = 25°C.

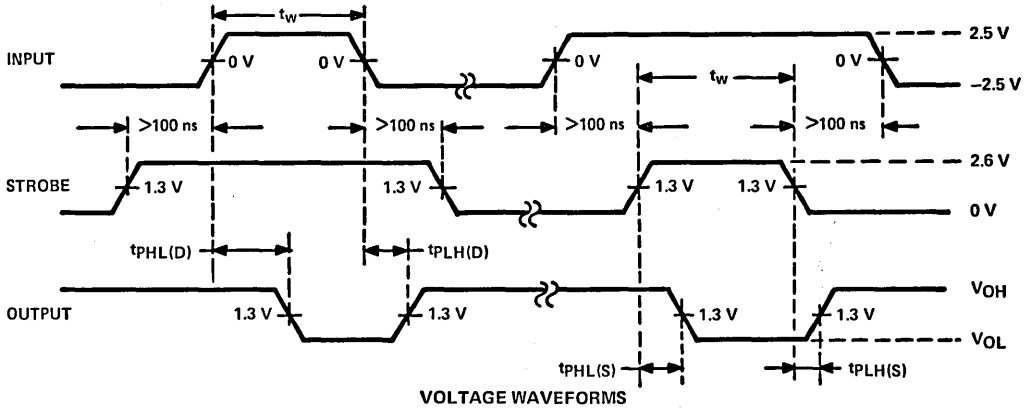
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PLH(D)}$	Propagation delay time, low-to-high-level output from differential input	R_L = 400 Ω, C_L = 15 pF, See Figure 1		18	40	ns
$t_{PHL(D)}$	Propagation delay time, high-to-low-level output from differential input			31	45	ns
$t_{PLH(S)}$	Propagation delay time, low-to-high-level output from strobe input			9	30	ns
$t_{PHL(S)}$	Propagation delay time, high-to-low-level output from strobe input			15	25	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: Z_O = 50 Ω, t_r = 10 ns, t_f = 10 ns, t_w = 0.5 ± 0.1 μs, PRR = 1 MHz.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064 or equivalent.

FIGURE 1–PROPAGATION DELAY TIMES

TYPICAL CHARACTERISTICS

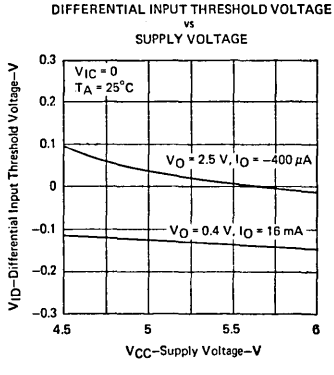


FIGURE 2

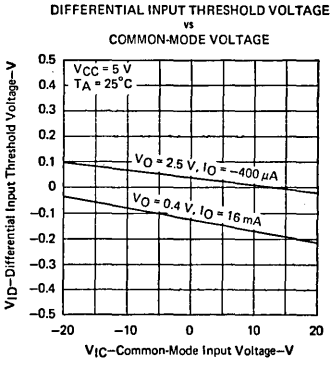


FIGURE 3

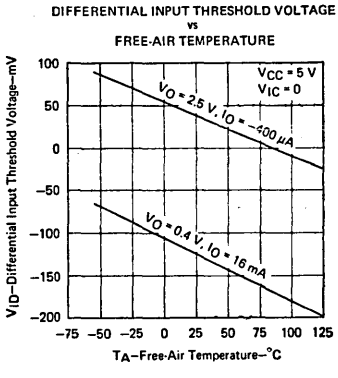


FIGURE 4

TEXAS INSTRUMENTS
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TYPICAL CHARACTERISTICS

OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

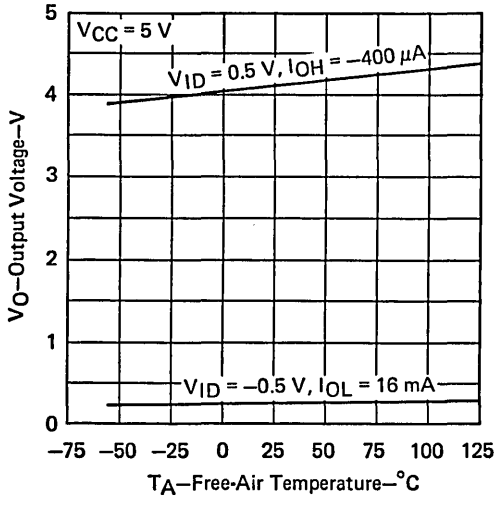


FIGURE 5

VOLTAGE TRANSFER CHARACTERISTICS

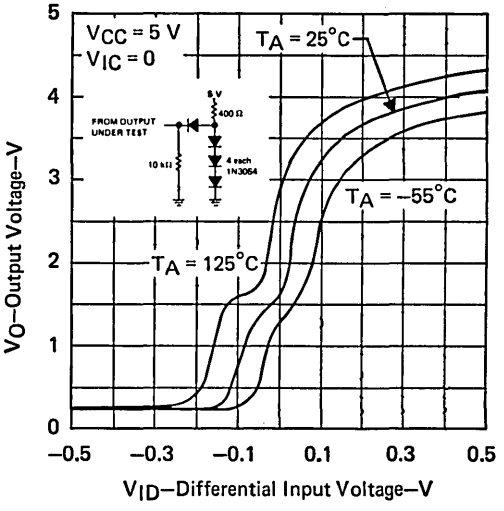


FIGURE 6

INPUT CURRENT
vs
INPUT VOLTAGE

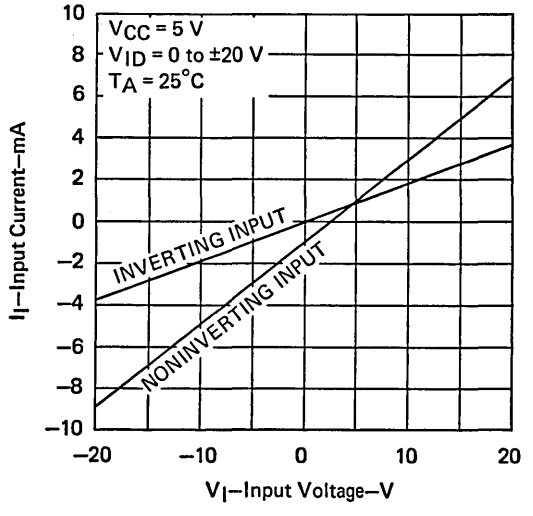


FIGURE 7

TERMINATING RESISTANCE
vs
FREE-AIR TEMPERATURE

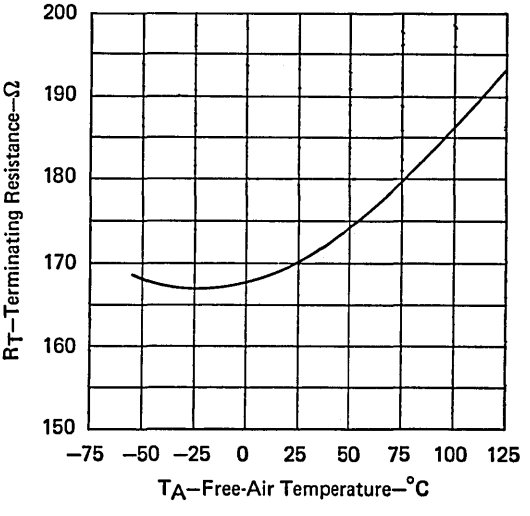


FIGURE 8

TYPICAL CHARACTERISTICS

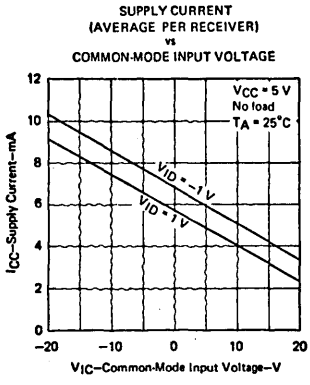


FIGURE 9

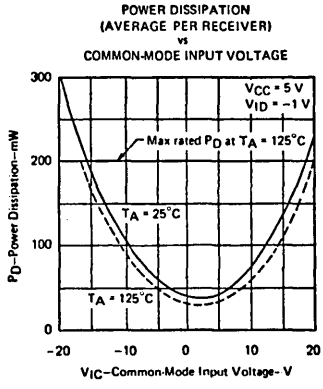


FIGURE 10

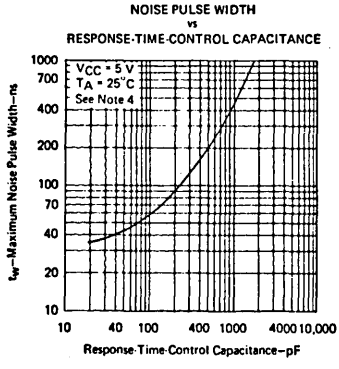
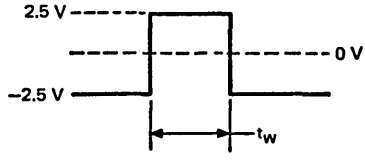


FIGURE 11



INPUT PULSE FOR FIGURE 11

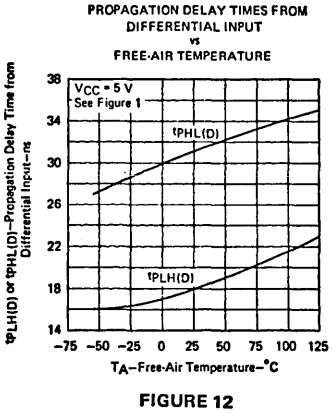


FIGURE 12

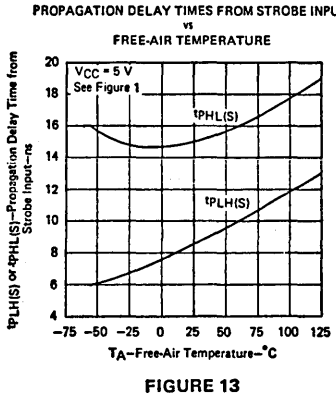


FIGURE 13

NOTE 4: Figure 11 shows the maximum width of the illustrated pulse that can be applied differentially without the output changing from the low to high level.

TEXAS INSTRUMENTS
INCORPORATED
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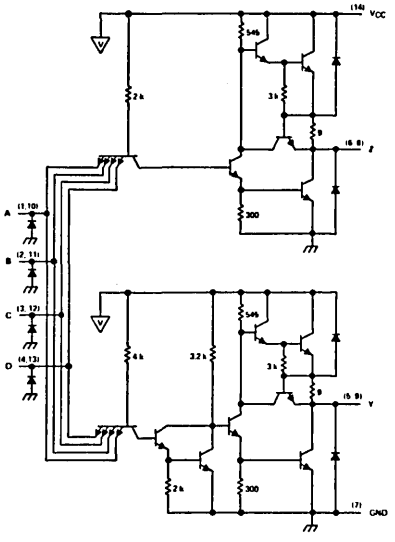
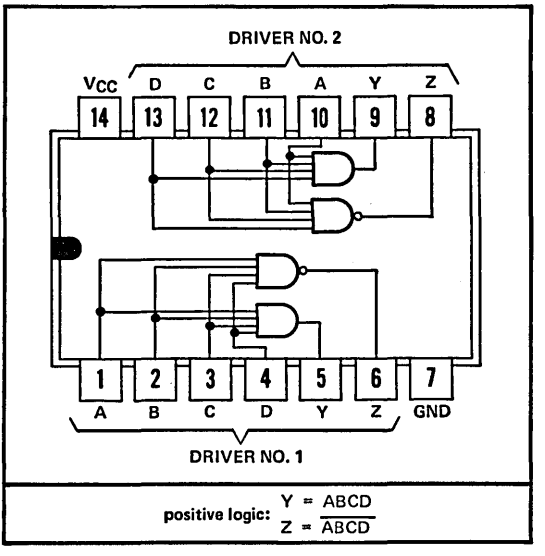
schematic (each driver)



Resistor values shown are nominal and in ohms.
▽. . . V_{CC} bus

J OR N DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: $Y = ABCD$, $Z = \overline{ABCD}$

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Duration of output short-circuit (see Note 2)	1 s
Continuous total power dissipation at (or below) 70°C free-air temperature (see Note 3)	600 mW
Operating free-air temperature range, SN55183	−55°C to 125°C
SN75183	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch from case for 60 seconds: J package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N package	260°C

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground terminal.
2. Not more than one output should be shorted to ground at a time.
3. For operation of SN55183 above 70°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 21. In the J package, these chips are glass-mounted.

recommended operating conditions

	SN55183			SN75183			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−40			−40	mA
Low-level output current, I_{OL}			40			40	mA
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended ranges of V_{CC} and operating free-air temperature (unless otherwise noted)

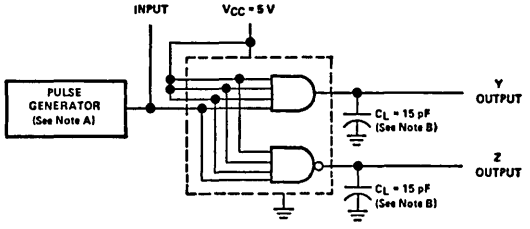
PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{OH}	High-level output voltage	Y (AND) OUTPUT	V_{IH} = 2 V, I_{OH} = −0.8 mA	2.4			V
			V_{IH} = 2 V, I_{OH} = −40 mA	1.8	3.3		
V_{OL}	Low-level output voltage		V_{IL} = 0.8 V, I_{OL} = 32 mA		0.2		V
			V_{IL} = 0.8 V, I_{OL} = 40 mA		0.22	0.4	
V_{OH}	High-level output voltage	Z (NAND) OUTPUT	V_{IL} = 0.8 V, I_{OH} = −0.8 mA	2.4			V
			V_{IL} = 0.8 V, I_{OH} = −40 mA	1.8	3.3		
V_{OL}	Low-level output voltage		V_{IH} = 2 V, I_{OL} = 32 mA		0.2		V
			V_{IH} = 2 V, I_{OL} = 40 mA		0.22	0.4	
I_{IH}	High-level input current		V_{IH} = 2.4 V			120	μA
I_I	Input current at maximum input voltage		V_{IH} = 5.5 V			2	mA
I_{IL}	Low-level input current		V_{IL} = 0.4 V			−4.8	mA
I_{OS}	Short-circuit output current§		V_{CC} = 5 V, T_A = 125°C	−40	−100	−120	mA
I_{CC}	Supply current (average per driver)		V_{CC} = 5 V, All inputs at 5 V, No load		10	18	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted to ground at a time, and duration of the short-circuit should not exceed one second.

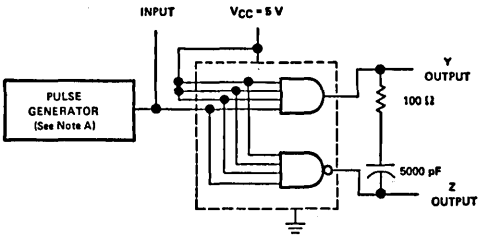
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level Y output	AND gates	C_L = 15 pF, See Figure 14(a)		8	12	ns
t_{PHL}	Propagation delay time, high-to-low-level Y output				12	18	ns
t_{PLH}	Propagation delay time, low-to-high-level Z output	NAND gates			6	12	ns
t_{PHL}	Propagation delay time, high-to-low-level Z output				6	8	ns
t_{PLH}	Propagation delay time, low-to-high-level differential output	Y output with respect to Z output	Z_L = 100 Ω in series with 5000 pF, See Figure 14(b)		9	16	ns
t_{PHL}	Propagation delay time high-to-low-level differential output				8	16	ns

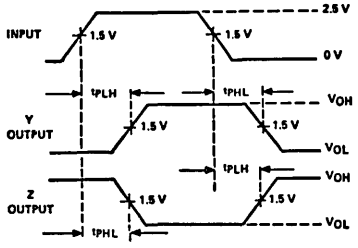
PARAMETER MEASUREMENT INFORMATION



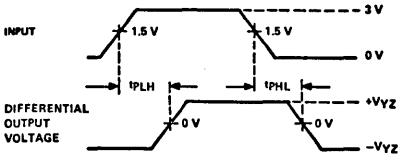
TEST CIRCUIT



TEST CIRCUIT



VOLTAGE WAVEFORMS
(a)—OUTPUTS Y AND Z



VOLTAGE WAVEFORMS
(b)—DIFFERENTIAL OUTPUT

NOTES: A. The pulse generator has the following characteristics: Z_O = 50 Ω, t_r = 10 ns, t_f = 10 ns, t_w = 0.5 μs, PRR = 1 MHz.
B. C_L includes probe and jig capacitance.
C. Waveforms are monitored on an oscilloscope with R_{in} > 1 MΩ.

FIGURE 14—PROPAGATION DELAY TIMES

TYPICAL CHARACTERISTICS

THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE

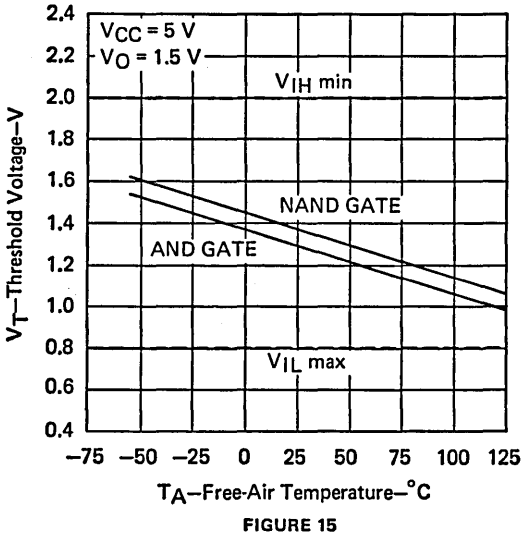


FIGURE 15

HIGH-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

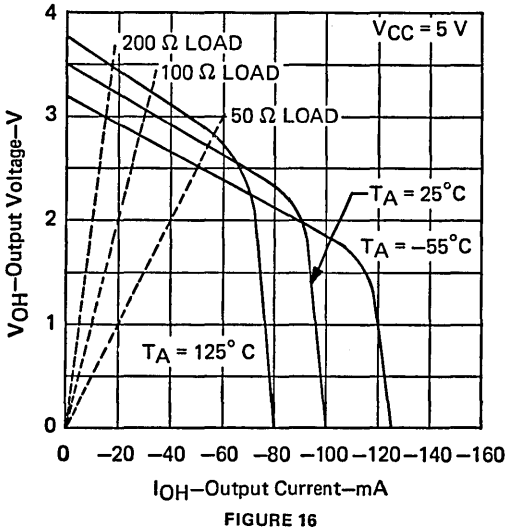


FIGURE 16

TYPICAL CHARACTERISTICS

DIFFERENTIAL OUTPUT VOLTAGE
vs
DIFFERENTIAL OUTPUT CURRENT

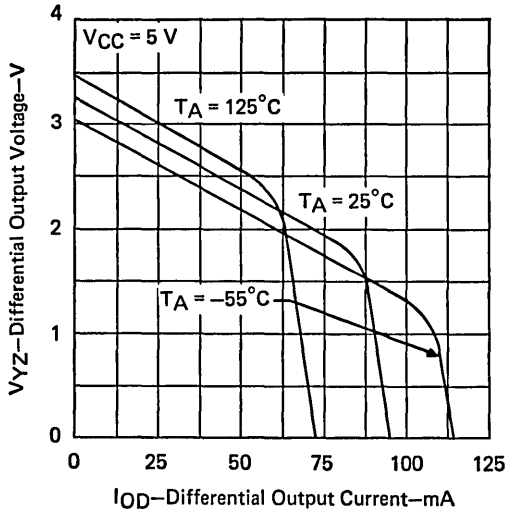


FIGURE 17

LOW-LEVEL OUTPUT VOLTAGE
vs
OUTPUT CURRENT

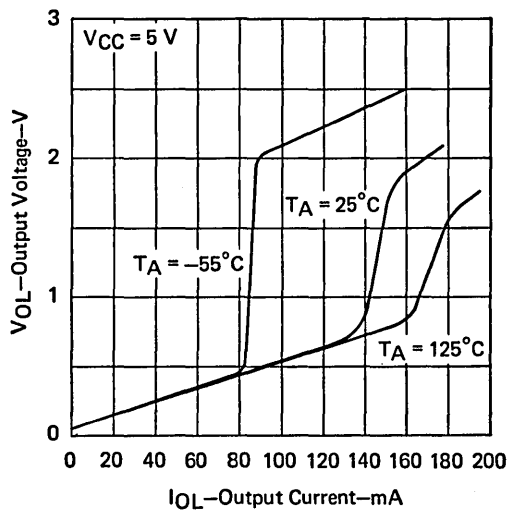


FIGURE 18

PROPAGATION DELAY TIME OF
DIFFERENTIAL OUTPUT
vs
FREE-AIR TEMPERATURE

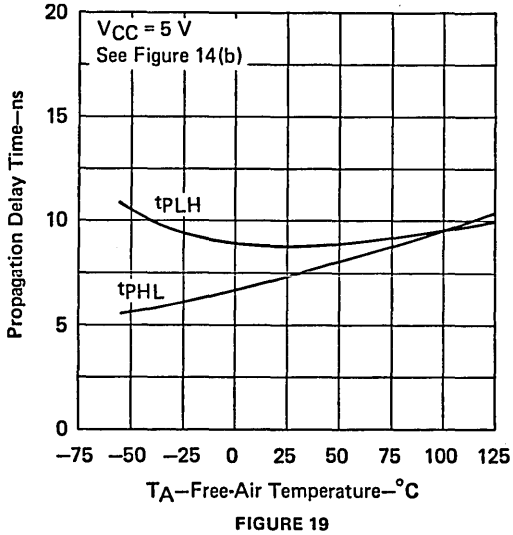


FIGURE 19

TOTAL POWER DISSIPATION
(BOTH DRIVERS)
vs
FREQUENCY

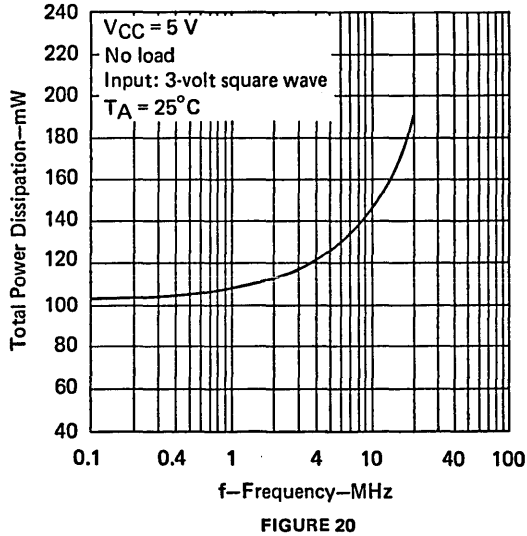


FIGURE 20

TEXAS INSTRUMENTS
INCORPORATED
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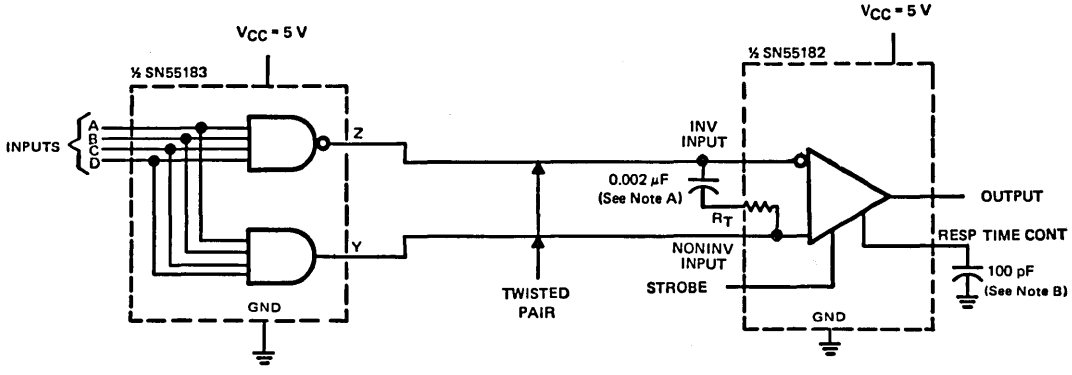
TYPICAL APPLICATION DATA



NOTES: A. When the inputs are open-circuited, the output will be high. A capacitor may be used for dc isolation of the line-terminating resistor. At the frequency of operation, the impedance of the capacitor should be relatively small.

Example: let $f = 5$ MHz
$C = 0.002\ \mu F$

$$Z_C = \frac{1}{2\pi fC} = \frac{1}{2\pi\,(5 \times 10^{6})\,(0.002 \times 10^{-6})}$$

$$Z_C \approx 16\ \Omega$$

B. Use of a capacitor to control response time is optional.

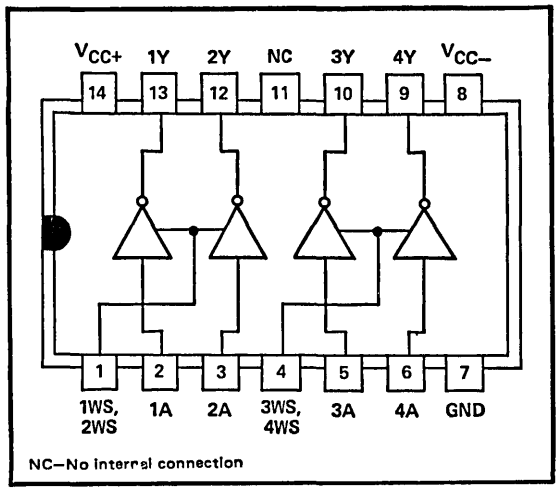
FIGURE 21—TRANSMISSION OF DIGITAL DATA OVER TWISTED-PAIR LINE

TYPE SN75186
QUADRUPLE LINE DRIVER

OCTOBER 1980

- Meets EIA Standards RS-232C and RS-423A
- Wide Supply Voltage Range . . . ±7.5 V to ±15 V
- Low Supply Current . . . 4.5 mA Max per Channel
- Wave Shaping with External Resistors
- Inputs Compatible with TTL and CMOS
- Outputs at High Impedance when Power Is Off
- Positive- and Negative-Current Limiting
- SN75156 is Dual Version in 8-Pin Package

J OR N PACKAGE
(TOP VIEW)



description

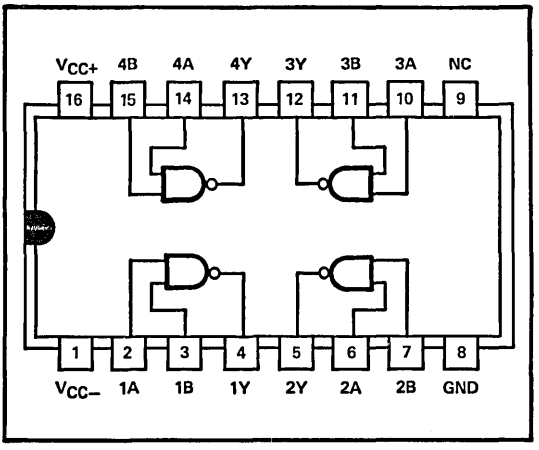
The SN75186 consists of two pairs of single-ended line drivers designed to meet the requirements of EIA Standards RS-232C and RS-423A, CCITT Recommendations V.10, V.28, and X.26, and Federal Standard FIPS 1030. This device maintains regulated high and low output levels of 5.5 volts and –5.5 volts, respectively, over a wide range of power supply voltages. A high output impedance is maintained without the use of an external blocking diode. The output transition time of each pair of drivers can be adjusted from 1 microsecond to 100 microseconds by means of an external resistor at the waveshaping (WS) pin.

TYPE SN75187
QUADRUPLE LINE DRIVER

OCTOBER 1980

- Meets EIA Standard RS-423A
- Operates From ±5-V Supplies
- Minimum Unloaded Output Voltage Of ±4 V
- High-Impedance Output over ±6-V Common-Mode Range with Power Off (No external diode required)
- Low Power Dissipation . . . 60 mW Max per Channel
- Positive- and Negative-Current Limiting for Slew Rate Control

J OR N PACKAGE



description

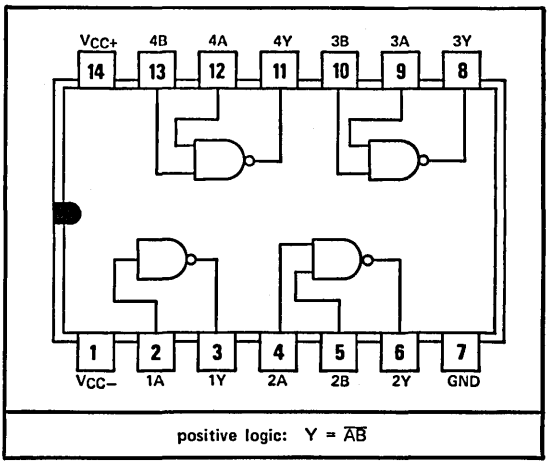
The SN75187 is a single-ended line driver designed to meet the requirements of EIA Standard RS-423A. The unloaded output voltage is at least 4 volts and –4 volts for high and low levels, respectively, over the recommended ranges of supply voltage (±4.5 volts to ±5.5 volts) and temperature (0°C to 70°C). The fully loaded output voltages are greater than ±3.6 volts for the same conditions. The outputs maintain the high-impedance state when both power supplies are off over the common-mode input voltage range of –6 volts to 6 volts. Limiting is provided for both positive and negative currents to limit slew rates.

TYPE SN75188
QUADRUPLE LINE DRIVER

BULLETIN NO. DL-S 11874, SEPTEMBER 1973—REVISED JANUARY 1977

- Meets Specifications of EIA RS-232C
- Designed to be Interchangeable with Motorola MC1488
- Current-Limited Output . . . 10 mA Typical
- Power-Off Output Impedance . . . 300 Ω Min
- Slew Rate Control by Load Capacitor
- Flexible Supply Voltage Range
- Input Compatible with Most TTL and DTL Circuits

J OR N
DUAL-IN-LINE PACKAGE
(TOP VIEW)



positive logic: $Y = \overline{AB}$

description

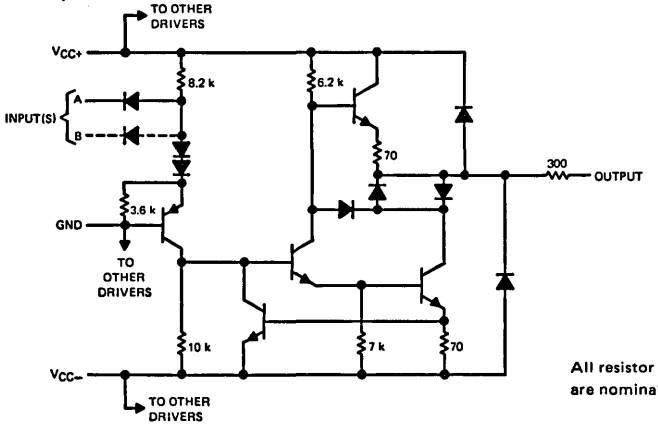
The SN75188 is a monolithic quadruple line driver designed to interface data terminal equipment with data communications equipment in conformance with the specifications of EIA Standard RS-232C with a diode in series with each supply-voltage terminal as shown under typical applications. The device is characterized for operation from 0°C to 75°C.

FUNCTION TABLE

A	B	Y
H	H	L
L	X	H
X	L	H

H = high level, L = low level,
X = irrelevant

schematic (each driver)



All resistor values shown are nominal and in ohms.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC+} at (or below) 25°C free-air temperature (see Notes 1 and 2) . . . . . 15 V
Supply voltage V_{CC-} at (or below) 25°C free-air temperature (see Notes 1 and 2) . . . . . −15 V
Input voltage range . . . . . −15 V to 7 V
Output voltage range . . . . . −15 V to 15 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 1 W
Operating free-air temperature range . . . . . 0°C to 75°C
Storage temperature range . . . . . −65°C to 175°C
Lead temperature 1/16 inch from case for 60 seconds: J package . . . . . 300°C
Lead temperature 1/16 inch from case for 10 seconds: N package . . . . . 260°C

NOTES: 1. All voltage values are with respect to the network ground terminal.
2. For operation above 25°C free-air temperature, refer to the Maximum Supply Voltage Curve, Figure 6, and the Dissipation Derating Curves in the Thermal Information Section, which begins on page 21. In the J package, SN75188 chips are glass-mounted.

TYPE SN75188
QUADRUPLE LINE DRIVER

REVISED JANUARY 1977

electrical characteristics over operating free-air temperature range, V_{CC+} = 9 V, V_{CC-} = −9 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX (SEE NOTE 4)	UNIT
V_{IH}	High-level input voltage			1.9			V
V_{IL}	Low-level input voltage					0.8	V
V_{OH}	High-level output voltage	V_{IL} = 0.8 V, R_L = 3 kΩ	V_{CC+} = 9 V, V_{CC-} = −9 V	6	7		V
			V_{CC+} = 13.2 V, V_{CC-} = −13.2 V	9	10.5		
V_{OL}	Low-level output voltage	V_{IH} = 1.9 V, R_L = 3 kΩ	V_{CC+} = 9 V, V_{CC-} = −9 V		−7	−6	V
			V_{CC+} = 13.2 V, V_{CC-} = −13.2 V		−10.5	−9	
I_{IH}	High-level input current	V_I = 5 V				10	μA
I_{IL}	Low-level input current	V_I = 0			−1	−1.6	mA
$I_{OS(H)}$	Short-circuit output current at high level ♦	V_I = 0.8 V,	V_O = 0	−6	−10	−12	mA
$I_{OS(L)}$	Short-circuit output current at low level ♦	V_I = 1.9 V,	V_O = 0	6	10	12	mA
r_o	Output resistance, power off	V_{CC+} = 0, V_{CC-} = 0, V_O = −2 V to 2 V		300			Ω
I_{CC+}	Supply current from V_{CC+}	V_{CC+} = 9 V, No load	All inputs at 1.9 V		15	20	mA
			All inputs at 0.8 V		4.5	6	
		V_{CC+} = 12 V, No load	All inputs at 1.9 V		19	25	
			All inputs at 0.8 V		5.5	7	
		V_{CC+} = 15 V, No load, T_A = 25°C	All inputs at 1.9 V			34	
			All inputs at 0.8 V			12	
I_{CC-}	Supply current from V_{CC-}	V_{CC-} = −9 V, No load	All inputs at 1.9 V		−13	−17	mA
			All inputs at 0.8 V			−0.015	
		V_{CC-} = −12 V, No load	All inputs at 1.9 V		−18	−23	
			All inputs at 0.8 V			−0.015	
		V_{CC-} = −15 V, No load, T_A = 25°C	All inputs at 1.9 V			−34	
			All inputs at 0.8 V			−2.5	
P_D	Total power dissipation	V_{CC+} = 9 V, No load	V_{CC-} = −9 V,			333	mW
		V_{CC+} = 12 V, No load	V_{CC-} = −12 V,			576	

†All typical values are at T_A = 25°C.

♦Not more than one output should be shorted at a time.

NOTE 4: The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for logic voltage levels only, e.g., if −6 V is a maximum, the typical value is a more negative voltage.

switching characteristics, V_{CC+} = 9 V, V_{CC-} = −9 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	R_L = 3 kΩ, C_L = 15 pF, See Figure 1		220	350	ns
t_{PHL}	Propagation delay time, high-to-low-level output			100	175	ns
t_{TLH}	Transition time, low-to-high-level output‡			55	100	ns
t_{THL}	Transition time, high-to-low-level output‡			45	75	ns
t_{TLH}	Transition time, low-to-high-level output§	R_L = 3 kΩ to 7 kΩ, C_L = 2500 pF, See Figure 1		2.5		μs
t_{THL}	Transition time, high-to-low-level output§			3.0		μs

‡Measured between 10% and 90% points of output waveform.

§Measured between +3 V and −3 V points on the output waveform (EIA RS-232C conditions)

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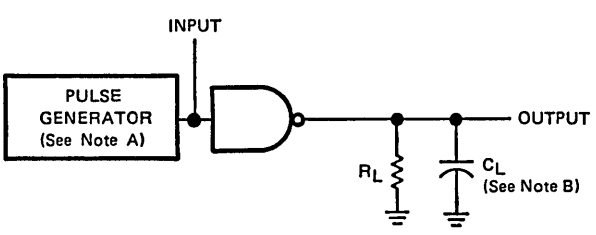
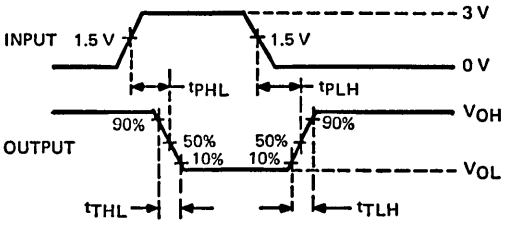
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTE: A. The pulse generator has the following characteristics: t_w = 0.5 μs, PRR = 1 MHz, Z_O = 50 Ω.
B. C_L includes probe and jig capacitance.

FIGURE 1—PROPAGATION AND TRANSITION TIMES

TYPICAL CHARACTERISTICS

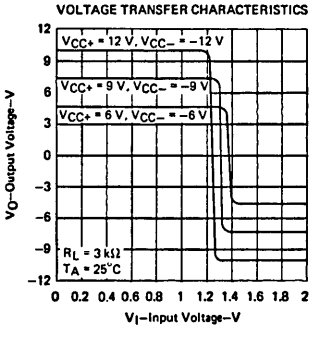


FIGURE 2

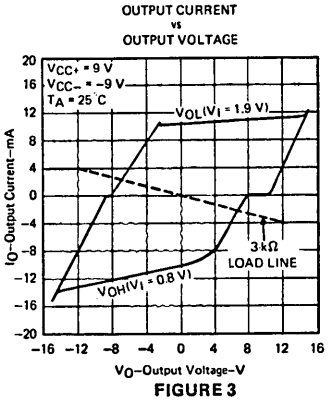


FIGURE 3

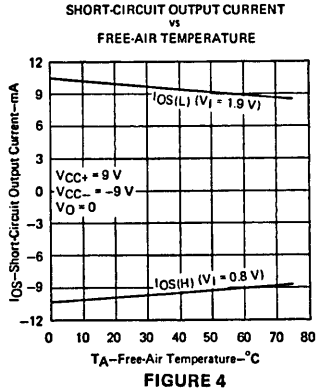


FIGURE 4

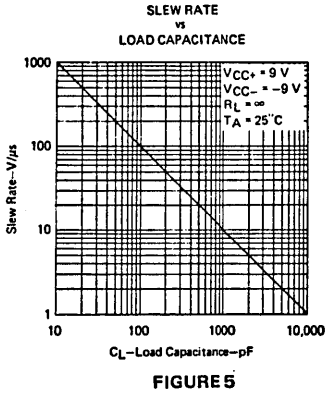


FIGURE 5

THERMAL INFORMATION

MAXIMUM SUPPLY VOLTAGE
vs
FREE-AIR TEMPERATURE

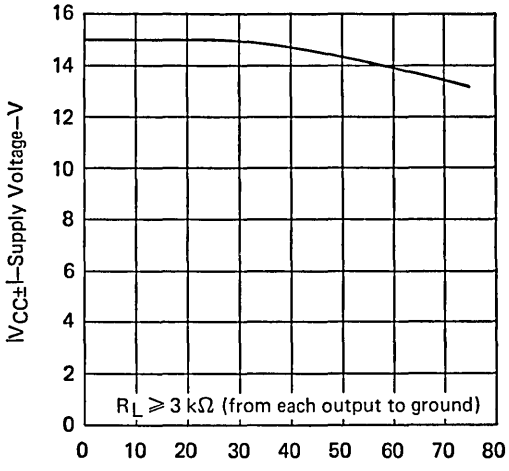


FIGURE 6

TYPICAL APPLICATION DATA

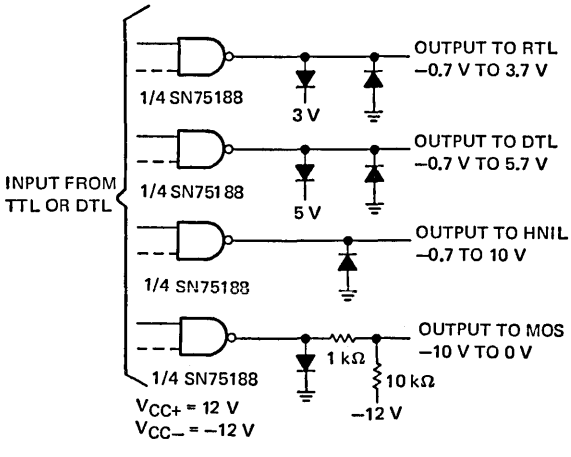


FIGURE 7–LOGIC TRANSLATOR APPLICATIONS

Diodes placed in series with the V_{CC+} and V_{CC-} leads will protect the SN75188 in the fault condition where the device outputs are shorted to ±15 V and the power supplies are at low voltage and provide low-impedance paths to ground.

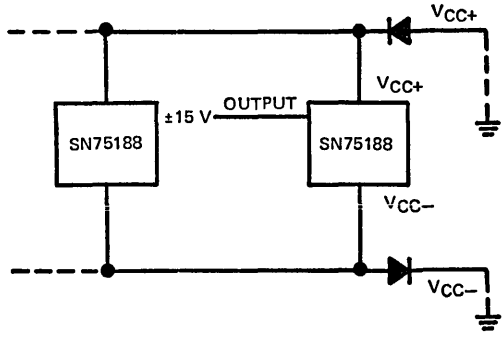


FIGURE 8–POWER SUPPLY PROTECTION TO MEET POWER-OFF FAULT CONDITIONS OF EIA STANDARD RS-232C

TEXAS INSTRUMENTS
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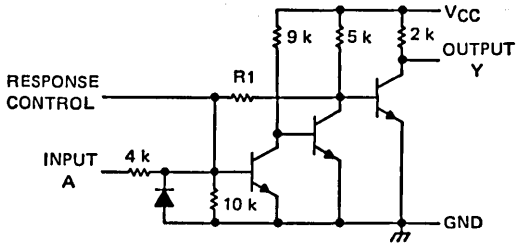
TYPES SN75189, SN75189A
QUADRUPLE LINE RECEIVERS

BULLETIN NO. DL-S 12035, SEPTEMBER 1973 – REVISED SEPTEMBER 1980

- Input Resistance . . . 3 kΩ to 7 kΩ
- Input Signal Range . . . ±30 V
- Fully Interchangeable with Mototola MC1489, MC1489A
- Operates From Single 5-V Supply
- Built-in Input Hysteresis (Double Thresholds)
- Response Control Provides:
  Input Threshold Shifting
  Input Noise Filtering
- Satisfies Requirements of EIA RS-232-C

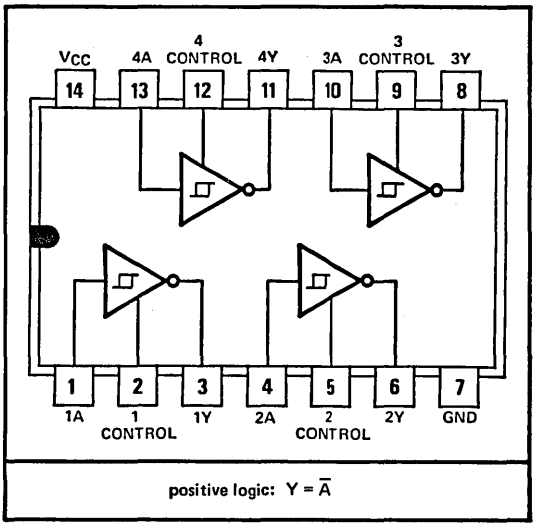
schematic (each receiver)



	SN75189	SN75189A
R1	10 k	2 k

Resistor values shown are nominal and in ohms.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{A}$

description

The SN75189 and SN75189A are monolithic quadruple line receivers designed to satisfy the requirements of the standard interface between data terminal equipment and data communication equipment as defined by EIA Standard RS-232C. A separate response control terminal is provided for each receiver. A resistor or a resistor and bias voltage source can be connected between this terminal and ground to shift the input threshold voltage levels. An external capacitor can be connected between this terminal and ground to provide input noise filtering.

absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	10 V
Input voltage	±30 V
Output current	20 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2)	1 W
Operating free-air temperature range	0°C to 75°C
Storage temperature range	−65°C to 175°C
Lead temperature 1/16 inch from case for 60 seconds: J package	300°C
Lead temperature 1/16 inch from case for 10 seconds: N package	260°C

NOTES: 1. Voltage values are with respect to the network ground terminal.
2. For operation above 25°C free-air temperature, refer to Dissipation Derating Curves in the Thermal Information section, which starts on page 21. In the J package, SN75189 and SN75189A chips are glass-mounted.

electrical characteristics over operating free-air temperature range, V_{CC} = 5V ± 1%, (unless otherwise noted)

PARAMETER	TEST FIGURE	TEST CONDITIONS†		SN75189 MIN	SN75189 TYP‡	SN75189 MAX	SN75189A MIN	SN75189A TYP‡	SN75189A MAX	UNIT
V_{T+} Positive-going threshold voltage	1		T_A = 25°C	1		1.5	1.75	1.9	2.25	V
				0.9		1.6	1.55		2.25	
V_{T-} Negative-going threshold voltage	1		T_A = 25°C	0.75		1.25	0.75	0.97	1.25	V
				0.65		1.25	0.65		1.25	
V_{OH} High-level output voltage	1	V_I = 0.75 V,	I_{OH} = −0.5 mA	2.6	4	5	2.6	4	5	V
		Input open,	I_{OH} = −0.5 mA	2.6	4	5	2.6	4	5	
V_{OL} Low-level output voltage	1	V_I = 3 V,	I_{OL} = 10 mA		0.2	0.45		0.2	0.45	V
I_{IH} High-level input current	2	V_I = 25 V		3.6		8.3	3.6		8.3	mA
		V_I = 3 V		0.43			0.43			
I_{IL} Low-level input current	2	V_I = −25 V		−3.6		−8.3	−3.6		−8.3	mA
		V_I = −3 V		−0.43			−0.43			
I_{OS} Short-circuit output current	3				−3			−3		mA
I_{CC} Supply current	2	V_I = 5 V,	Outputs open		20	26		20	26	mA

†All characteristics are measured with the response control terminal open.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output	4	C_L = 15 pF, R_L = 3.9 kΩ		25	85	ns
t_{PHL} Propagation delay time, high-to-low-level output		C_L = 15 pF, R_L = 390 Ω		25	50	
t_{TLH} Transition time, low-to-high-level output		C_L = 15 pF, R_L = 3.9 kΩ		120	175	ns
t_{THL} Transition time, high-to-low-level output		C_L = 15 pF, R_L = 390 Ω		10	20	

PARAMETER MEASUREMENT INFORMATION§

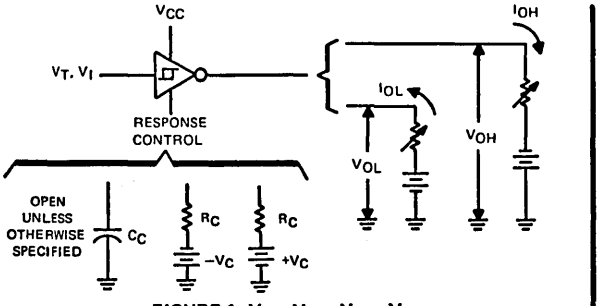
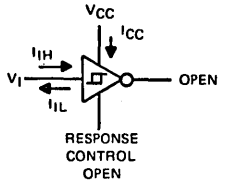


FIGURE 1–V_{T+}, V_{T-}, V_{OH}, V_{OL}



I_{CC} is tested for all four receivers simultaneously

FIGURE 2–I_{IH}, I_{IL}, I_{CC}

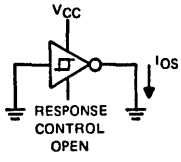
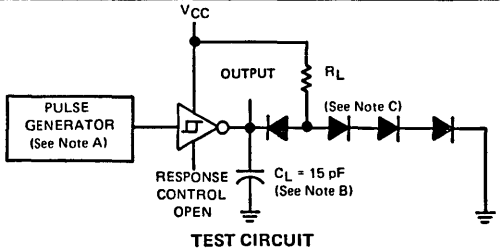
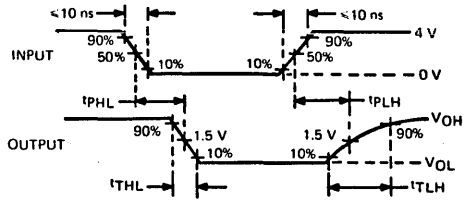


FIGURE 3–I_{OS}



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: $Z_{out} \approx 50\ \Omega$, t_w = 500 ns.
B. C_L includes probe and jig capacitance. C. All diodes are 1N3064 or equivalent.

FIGURE 4–SWITCHING TIMES

§Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

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TYPICAL CHARACTERISTICS

SN75189
OUTPUT VOLTAGE vs INPUT VOLTAGE

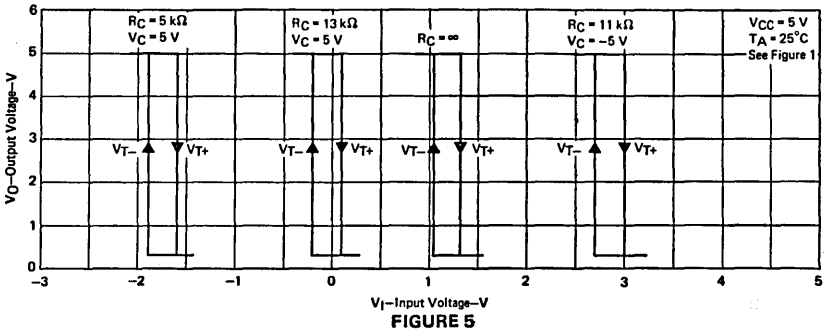

FIGURE 5

SN75189A
OUTPUT VOLTAGE vs INPUT VOLTAGE

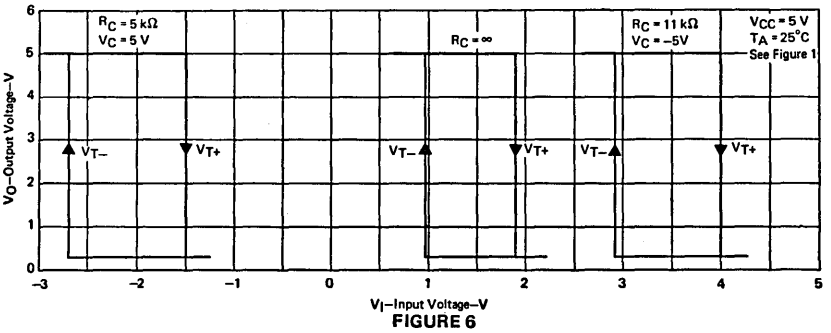

FIGURE 6

INPUT THRESHOLD VOLTAGE
vs
FREE-AIR TEMPERATURE

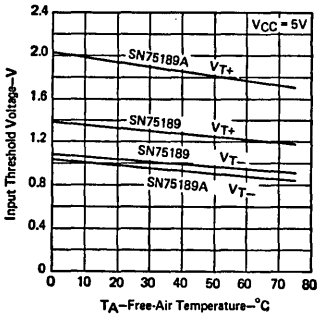

FIGURE 7

INPUT THRESHOLD VOLTAGE
vs
SUPPLY VOLTAGE

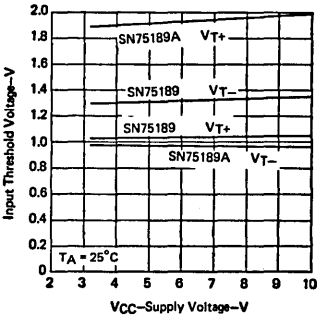

FIGURE 8

TYPICAL CHARACTERISTICS

SN75189
NOISE REJECTION

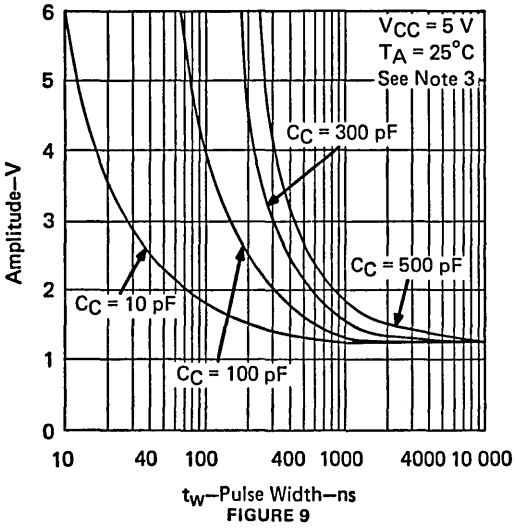

FIGURE 9

SN75189A
NOISE REJECTION

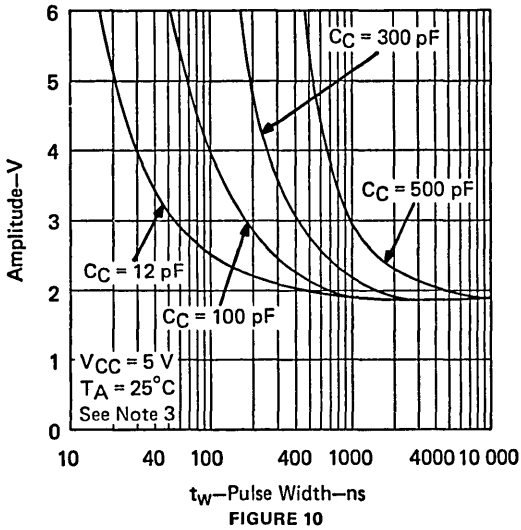

FIGURE 10

INPUT CURRENT
vs
INPUT VOLTAGE

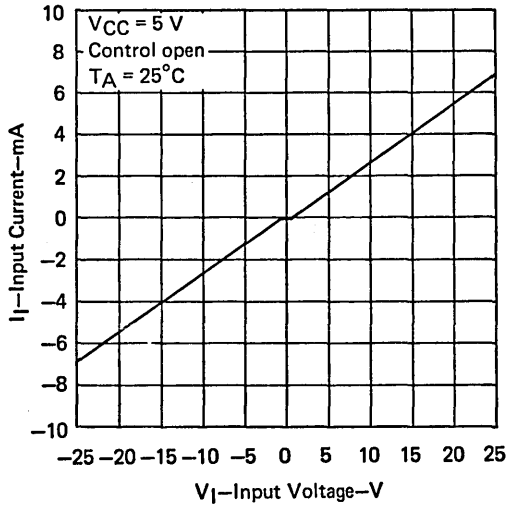

FIGURE 11

NOTE 3: This figure shows the maximum amplitude of a positive-going pulse that, starting from zero volts, will not cause a change of the output level.

TEXAS INSTRUMENTS
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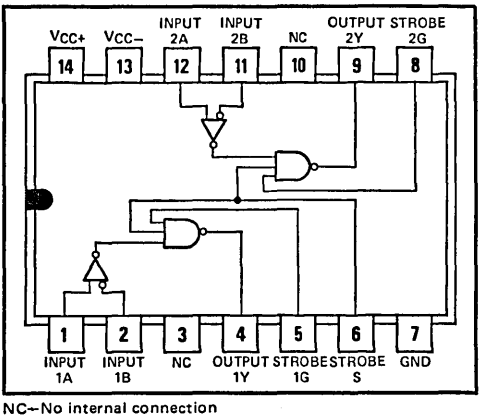
TYPES SN75207, SN75207B, SN75208, SN75208B DUAL SENSE AMPLIFIERS FOR MOS MEMORIES OR DUAL HIGH-SENSITIVITY LINE RECEIVERS

BULLETIN NO. DL-S 11793, JULY 1973–REVISED JANUARY 1977

- Plug-in Replacement for SN75107A, SN75107B, SN75108A, SN75108B with Improved Characteristics
- ±10 mV Guaranteed Input Sensitivity
- TTL Compatible
- Standard Supply Voltages . . . ±5 V
- Differential Input Common-Mode Voltage Range of ±3 V
- Strobe Inputs for Channel Selection
- '207 and '207B Have Totem-Pole Outputs
- '208 and '208B Have Open-Collector Outputs
- "B" Versions Have Diode-Protected Input Stage for Power-Off Condition
- Sense Amplifier for MOS Memories
- Dual Comparator
- High-Sensitivity Line Receiver

J OR N
DUAL-IN-LINE PACKAGE
(TOP VIEW)



NC–No internal connection

description

The SN75207, SN75207B, SN75208, and SN75208B are pin-for-pin replacements for the SN75107A, SN75107B, SN75108A, and SN75108B, respectively. The improved input sensitivity makes them more suitable for MOS memory sense amplifiers and can result in faster memory cycles. Improved sensitivity also makes them more useful in line receiver applications by allowing use of longer transmission line lengths. The '207 and '207B each features a TTL-compatible active-pull-up output. The '208 and '208B each features an open-collector output that permits wired-AND logic connections with similar output configurations. These devices are designed for operation from 0°C to 70°C and are available in the ceramic dual-in-line (J) package or in the plastic dual-in-line (N) package.

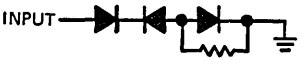
FUNCTION TABLE

DIFFERENTIAL INPUTS A-B	STROBES G	STROBES S	OUTPUT Y
$V_{ID} \geq 10$ mV	X	X	H
-10 mV $< V_{ID} <$ 10 mV	X	L	H
	L	X	H
	H	H	Indeterminate
$V_{ID} \leq -10$ mV	X	L	H
	L	X	H
	H	H	L

H = high level, L = low level, X = irrelevant

The essential difference between the unsuffixed and "B" versions can be seen in the schematics. Input-protection diodes are in series with the collectors of the differential-input transistors of the "B" versions. These diodes are useful in certain "party-line" systems that may have multiple V_{CC+} power supplies and may be operated with some of the V_{CC+} supplies turned off. In such a system, if a supply is turned off and allowed to go to ground, the equivalent input circuit connected to that supply would be as follows:

UNSUFFIXED VERSION



"B" VERSION

This would be a problem in specific systems that might possibly have the transmission lines biased to some potential greater than 1.4 volts.

design characteristics

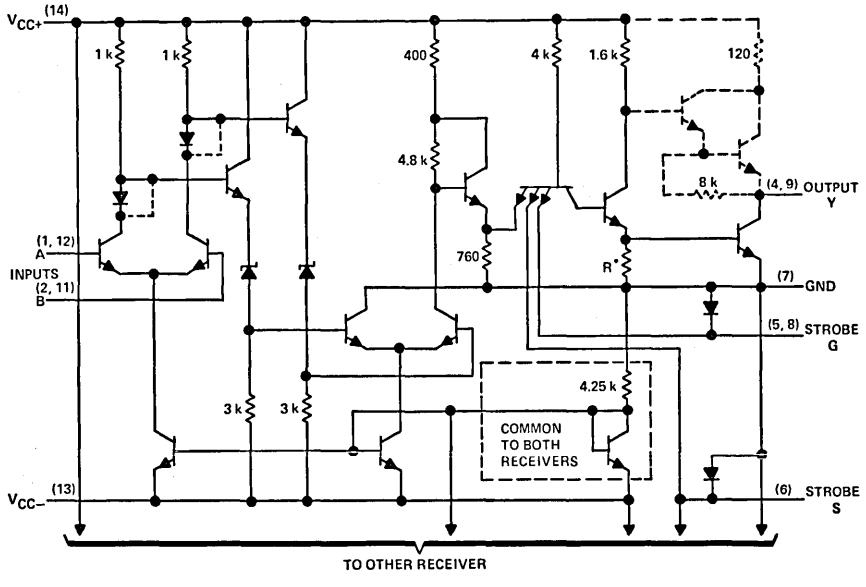
The '207, '207B, '208, and '208B line receivers/sense amplifiers are TTL-compatible dual circuits intended for use in high-speed data-transmission systems or MOS memory systems. They are designed to detect low-level differential signals in the presence of common-mode noise and variations of temperature and supplies. Dc specifications reflect worst-case conditions of temperature, supply voltages, and input voltages.

The input common-mode voltage range is ±3 volts. This is adequate for application in most systems. In systems with requirements for greater common-mode voltage range, input attenuators may be used to decrease the noise to an acceptable level at the receiver-input terminals.

The circuits feature individual strobe inputs for each channel and a strobe input common to both channels for logic versatility. The strobe inputs are tested to guarantee 400 millivolts of dc noise margin when interfaced with Series 54/74 TTL.

The circuits feature high input impedance and low input currents, which induce very little loading on the transmission line. This makes these devices especially useful in party-line systems. The excellent input sensitivity (3 millivolts typical) is particularly important when data is to be detected at the end of a long transmission line and the amplitude of the data has deteriorated due to cable losses. The circuits are designed to detect input signals of 10 millivolts (or greater) amplitude and convert the polarity of the signal into appropriate TTL-compatible output logic levels.

schematic (each receiver)



*R = 1 kΩ for '207 and '207B, 750 Ω for '208 and '208B.

NOTES: A. Resistor values shown are nominal and in ohms.

B. Components shown with dashed lines in the output circuitry are applicable to the '207 and '207B only. Diodes in series with the collectors of the differential input transistors are short-circuited on '207 and '208.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC+} (see Note 1)	7 V
Supply voltage V_{CC-}	−7 V
Differential input voltage (see Note 2)	±6 V
Common-mode input voltage (see Note 3)	±5 V
Strobe input voltage	5.5 V
Continuous total dissipation	600 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C

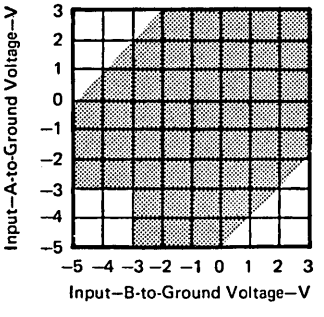
recommended operating conditions (see note 4)

	MIN	NOM	MAX	UNIT
Supply voltage V_{CC+}	4.75	5	5.25	V
Supply voltage V_{CC-}	−4.75	−5	−5.25	V
Low-level output current, I_{OL}			−16	mA
Differential input voltage, V_{ID} (see Note 5)	−5†		5	V
Common-mode input voltage, V_{IC} (see Notes 5 and 6)	−3†		3	V
Input voltage range, any differential input to ground (see Note 5)	−5†		3	V
Operating free-air temperature, T_A	0		70	°C

†The algebraic convention, where the less positive (more negative) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

NOTES:
1. All voltage values, except differential voltages, are with respect to network ground terminal.
2. Differential voltage values are at the noninverting (A) terminal with respect to the inverting (B) terminal.
3. Common-mode input voltage is the average of the voltages at the A and B inputs.
4. When using only one channel of the line receiver, the strobe G of the unused channel should be grounded and at least one of the differential inputs of the unused receiver should be terminated at some voltage between −3 V and 3 V.
5. The recommended combinations of input voltages fall within the shaded area of the figure at the right.
6. The common-mode voltage may be as low as −4 V provided that the more positive of the two inputs is not more negative than −3 V.

RECOMMENDED COMBINATIONS OF INPUT VOLTAGES



definition of input logic levels†

		MIN	MAX	UNIT
V_{IDH}	High-level input voltage between differential inputs	0.01	5	V
V_{IDL}	Low-level input voltage between differential inputs	−5	−0.01	V
$V_{IH(S)}$	High-level input voltage at strobe inputs	2	5.5	V
$V_{IL(S)}$	Low-level input voltage at strobe inputs	0	0.8	V

†The algebraic convention, where the more positive (less negative) limit is designated maximum, is used in this data sheet with logic input voltage levels only.

electrical characteristics over recommended free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS‡		'207, '207B MIN	'207, '207B TYP§	'207, '207B MAX	'208, '208B MIN	'208, '208B TYP§	'208, '208B MAX	UNIT
I_{IH}	High-level input current	A	$V_{CC\pm}$ = MAX	V_{ID} = 5 V		30	75		30	75	μA
		B		V_{ID} = −5 V		30	75		30	75	
I_{IL}	Low-level input current	A	$V_{CC\pm}$ = MAX	V_{ID} = −5 V			−10			−10	μA
		B		V_{ID} = 5 V			−10			−10	
I_{IH}	High-level input current into 1G or 2G		$V_{CC\pm}$ = MAX, $V_{IH(S)}$ = 2.4 V				40			40	μA
			$V_{CC\pm}$ = MAX, $V_{IH(S)}$ = MAX V_{CC+}				1			1	mA
I_{IL}	Low-level input current into 1G or 2G		$V_{CC\pm}$ = MAX, $V_{IL(S)}$ = 0.4 V				−1.6			−1.6	mA
I_{IH}	High-level input current into S		$V_{CC\pm}$ = MAX, $V_{IH(S)}$ = 2.4 V				80			80	μA
			$V_{CC\pm}$ = MAX, $V_{IH(S)}$ = MAX V_{CC+}				2			2	mA
I_{IL}	Low-level input current into S		$V_{CC\pm}$ = MAX, $V_{IL(S)}$ = 0.4 V				−3.2			−3.2	mA
V_{OH}	High-level output voltage		$V_{CC\pm}$ = MIN, $V_{IL(S)}$ = 0.8 V, V_{IDH} = 10 mV, I_{OH} = −400 μA, V_{IC} = −3 V to 3 V		2.4						V
V_{OL}	Low-level output voltage		$V_{CC\pm}$ = MIN, $V_{IH(S)}$ = 2 V, V_{IDL} = −10 mV, I_{OL} = 16 mA, V_{IC} = −3 V to 3 V				0.4			0.4	V
I_{OH}	High-level output current		$V_{CC\pm}$ = MIN, V_{OH} = MAX V_{CC+}							250	μA
I_{OS}	Short-circuit output current¶		$V_{CC\pm}$ = MAX		−18		−70				mA
I_{CCH+}	Supply current from V_{CC+}, outputs high		$V_{CC\pm}$ = MAX, T_A = 25°C			18	30		18	30	mA
I_{CCH-}	Supply current from V_{CC-}, outputs high		$V_{CC\pm}$ = MAX, T_A = 25°C			−8.4	−15		−8.4	−15	mA

‡For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§All typical values are at V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C.
¶Not more than one output should be shorted at a time.

switching characteristics, V_{CC+} = 5 V, V_{CC-} = −5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	'207, '207B MIN	'207, '207B TYP	'207, '207B MAX	'208, '208B MIN	'208, '208B TYP	'208, '208B MAX	UNIT
$t_{PLH(D)}$	Propagation delay time, low-to-high-level output, from differential inputs A and B	R_L = 470 Ω, C_L = 15 pF, See Figure 1			35			35	ns
$t_{PHL(D)}$	Propagation delay time, high-to-low-level output, from differential inputs A and B				20			20	ns
$t_{PLH(S)}$	Propagation delay time, low-to-high-level output, from strobe input G or S				17			17	ns
$t_{PHL(S)}$	Propagation delay time, high-to-low-level output, from strobe input G or S				17			17	ns

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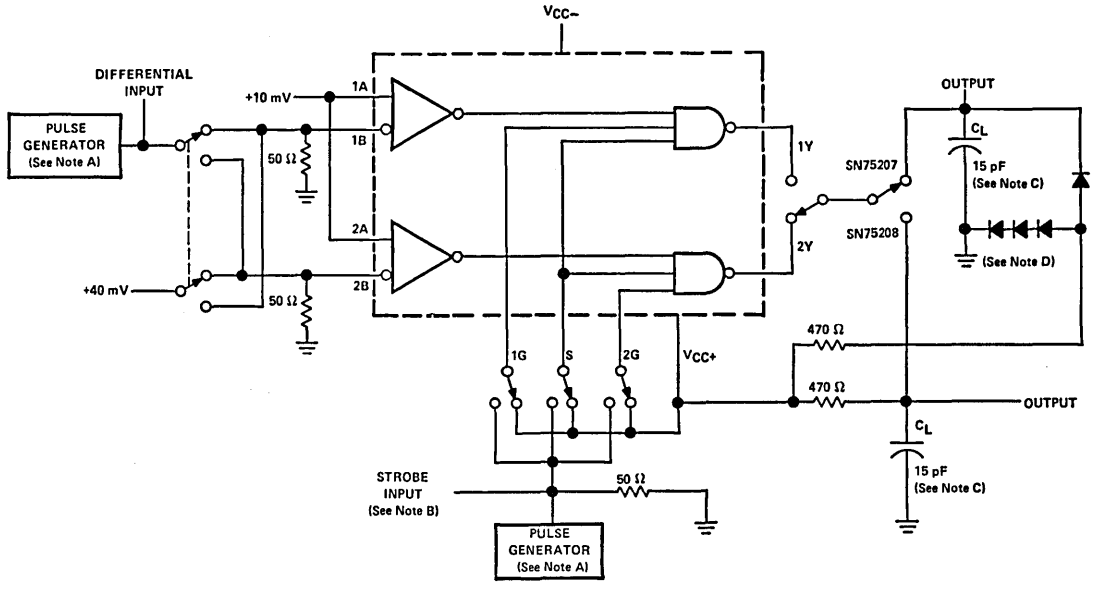
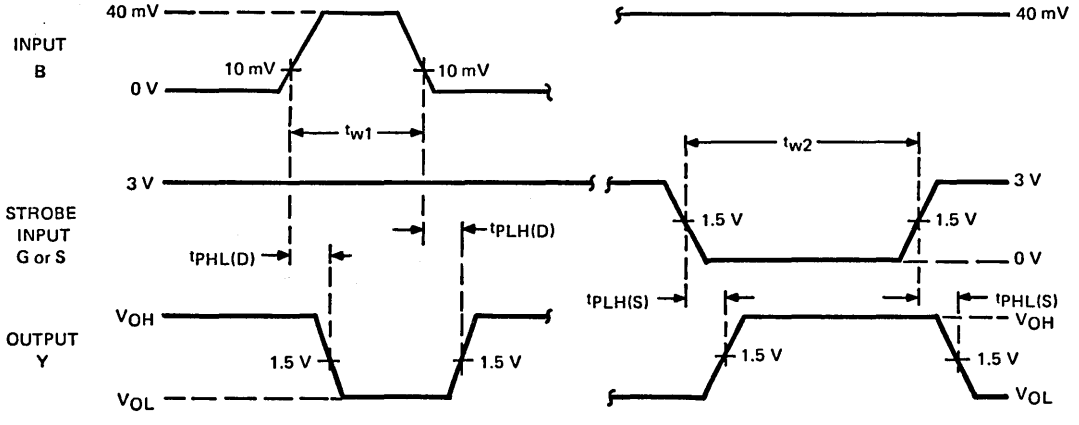
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: Z_{out} = 50 Ω, $t_r \leq 5$ ns, $t_f \leq 5$ ns, t_{w1} = 500 ns with PRR = 1 MHz, t_{w2} = 1 μs with PRR = 500 kHz.
B. Strobe input pulse is applied to Strobe 1G when inputs 1A-1B are being tested, to Strobe S when inputs 1A-1B or 2A-2B are being tested, and to Strobe 2G when inputs 2A-2B are being tested.
C. C_L includes probe and jig capacitance.
D. All diodes are 1N916.

FIGURE 1–PROPAGATION DELAY TIMES

TYPICAL APPLICATION DATA

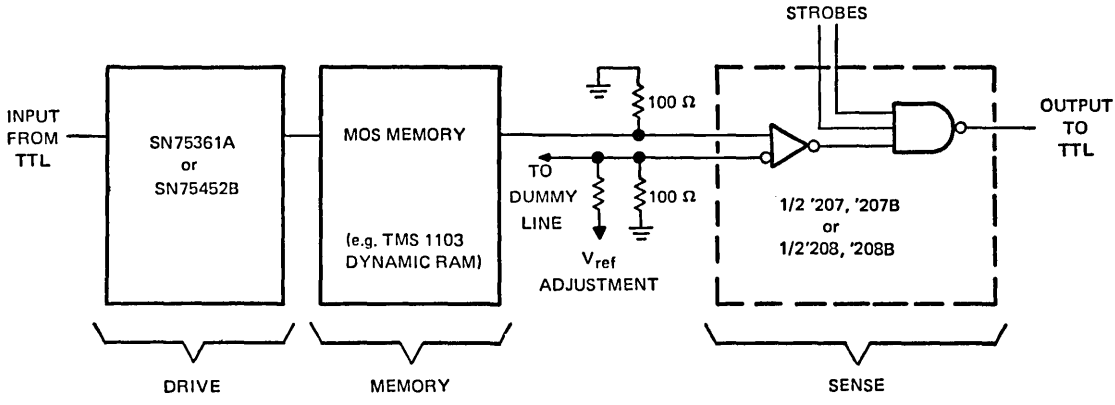
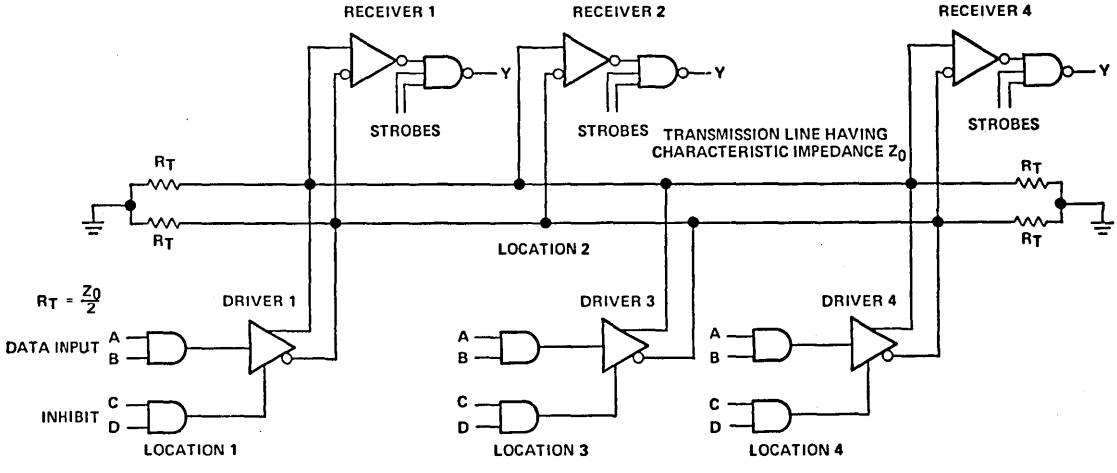


FIGURE 2–MOS MEMORY SENSE AMPLIFIER



Receivers are '207, '207B, '208, or '208B; drivers are SN55109A, SN75109A, SN55110A, SN75110A, or SN75112.

FIGURE 3–DATA-BUS OR PARTY-LINE SYSTEM

PRECAUTIONS: When only one receiver in a package is being used, at least one of the differential inputs of the unused receiver should be terminated at some voltage between −3 volts and +3 volts, preferably at ground. Failure to do so will cause improper operation of the unit being used because of common bias circuitry for the current sources of the two receivers. Strobe G of the unused channel should be grounded.

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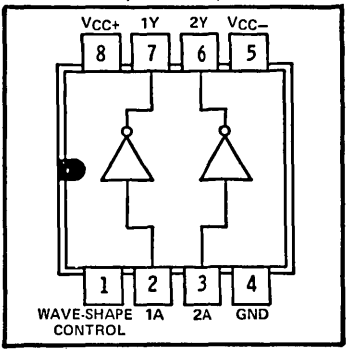
TYPE uA9636AC
DUAL LINE DRIVERS WITH ADJUSTABLE SLEW RATE

BULLETIN NO. DL-S 12774, OCTOBER 1980

- Meets EIA Standards RS-423, RS-232C, and Federal Standard 1030
- Slew Rate Control
- Output Short-Circuit-Current Limiting
- Wide Supply Voltage Range
- 8-Pin Dual-In-Line Package
- Designed to be Interchangeable With Fairchild 9636A

JG OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)



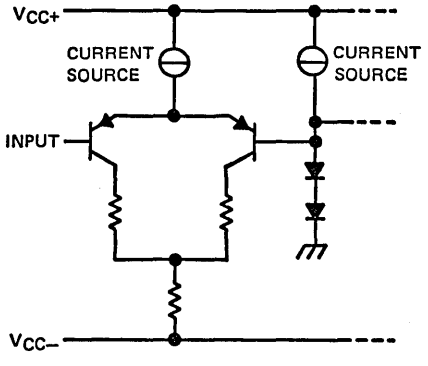
description

The uA9636AC is a dual single-ended line driver designed to meet EIA Standards RS-423, RS-232C, and Federal Standard 1030. The slew rates of both amplifiers are controlled by a single external resistor, R_{WS}, connected between the wave-shape-control terminal and ground. Output current limiting is provided. Inputs are compatible with TTL and CMOS and are diode-protected against negative transients. This device operates from ±12 volts and is supplied in an 8-pin dual-in-line package.

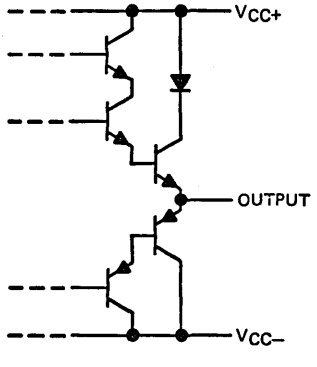
The uA9636AC is characterized for operation from 0°C to 70°C.

schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



TYPICAL OF ALL OUTPUTS



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Positive supply voltage range, V_{CC+} (see Note 1) . . . . . V_{CC-} to 15 V
Negative supply voltage range, V_{CC-} . . . . . 0.5 V to −15 V
Output voltage . . . . . ±15 V
Output current . . . . . ±150 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2): JG package . . . . . 825 mW
P package . . . . . 1000 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch (1,6 mm) from case for 60 seconds: JG package . . . . . 300°C
Lead temperature 1/16 inch (1,6 mm) from case for 10 seconds: P package . . . . . 260°C

NOTES: 1. All voltage values are with respect to the network ground terminal.
2. For operation above 25°C free-air temperature, derate at the rate of 6.6 mW/°C for the JG package and 8.0 mW/°C for the P package.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Positive supply voltage, V_{CC+}	10.8	12	13.2	V
Negative supply voltage, V_{CC-}	−10.8	−12	−13.2	V
Operating free-air temperature, T_A	0		70	°C
Wave-shaping resistor, R_{WS}	10		1000	kΩ

electrical characteristics over recommended range of free-air temperature, supply voltage, and wave-shaping resistance (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP† (See Note 3)	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	I_I = −15 mA			−1.1	−1.5	V
V_{OH}	High-level output voltage	V_I = 0.8 V	R_L = ∞	5	5.6	6	V
			R_L = 3 kΩ to ground	5	5.6	6	
			R_L = 450 Ω to ground	4	5.4	6	
V_{OL}	Low-level output voltage	V_I = 2 V	R_L = ∞	−6	−5.7	−5	V
			R_L = 3 kΩ to ground	−6	−5.6	−5	
			R_L = 450 Ω to ground	−6	−5.4	−4	
I_{IH}	High-level input current	V_I = 2.4 V				10	μA
		V_I = 5.5 V				100	
I_{IL}	Low-level input current	V_I = 0.4 V			−20	−80	μA
I_O	Output current (power off)	$V_{CC\pm}$ = 0,	V_O = ±6 V			±100	μA
I_{OS}	Short-circuit output current‡	V_I = 2 V		15	25	150	mA
		V_I = 0 V		−15	−40	−150	
r_o	output resistance	R_L = 450 Ω			25	50	Ω
I_{CC+}	Positive supply current	V_{CC} = ±12 V, R_{WS} = 100 kΩ,	V_I = 0 V, Output open		13	18	mA
I_{CC-}	Negative supply current	V_{CC} = ±12 V, R_{WS} = 100 kΩ,	V_I = 0 V, Output open		−13	−18	mA

†All typical values are at V_{CC} ± 12 V, T_A = 25°C.
‡Not more than one output should be shorted to ground at a time, and duration of the short-circuit should not exceed one-second.
NOTE 3: The algebraic convention, where the less-positive (more-negative) limit is designated as minimum, is used in this data sheet for logic voltage levels, e.g., when −5 V is the maximum, the minimum is a more-negative voltage.

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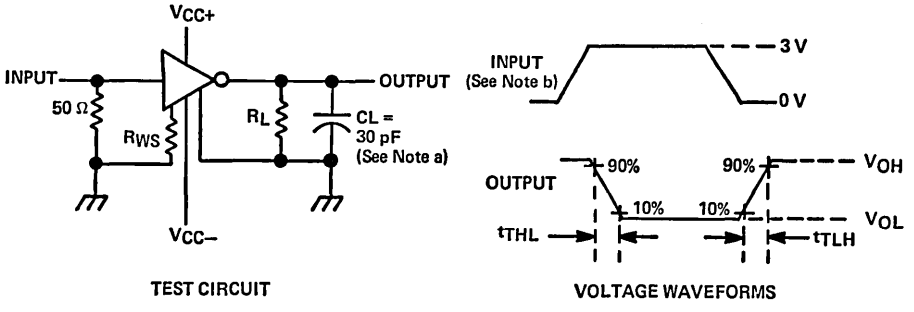
switching characteristics, $V_{CC\pm}$ = 12 V, T_A = 25°C, see figure 1

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{TLH}	Transition time, low-to-high-level output	R_L = 450 Ω, C_L = 30 pF	R_{WS} = 10 kΩ	0.8	1.1	1.4	µs
			R_{WS} = 100 kΩ	8	11	14	
			R_{WS} = 500 kΩ	40	55	70	
			R_{WS} = 1 MΩ	80	110	140	
t_{THL}	Transition time, high-to-low-level output	R_L = 450 Ω, C_L = 30 pF	R_{WS} = 10 kΩ	0.8	1.1	1.4	µs
			R_{WS} = 100 kΩ	8	11	14	
			R_{WS} = 500 kΩ	40	55	70	
			R_{WS} = 1 MΩ	80	110	140	

PARAMETER MEASUREMENT INFORMATION



NOTES: a. C_L includes probe and jig capacitance.
b. The input pulse is supplied by a generator having the following characteristics: $t_r \leq 10$ ns, $t_f = 10$ ns, $Z_{out} = 50\ \Omega$, PRR = 1 kHz, duty cycle = 10%.

FIGURE 1 – TRANSITION TIMES

TYPICAL APPLICATION DATA

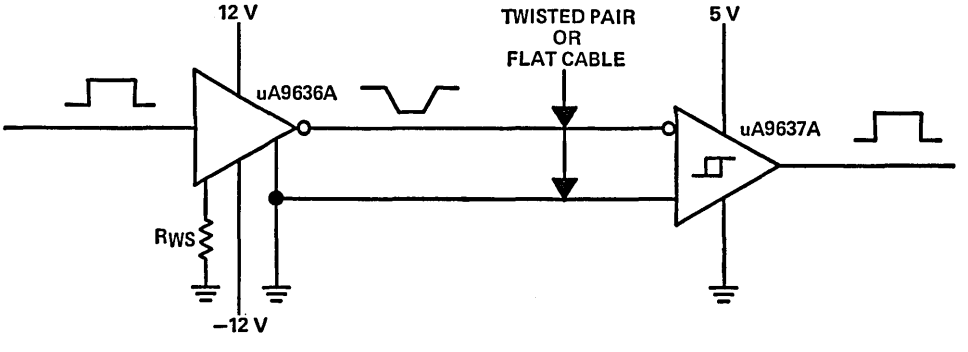


FIGURE 2 – RS-423 SYSTEM APPLICATION

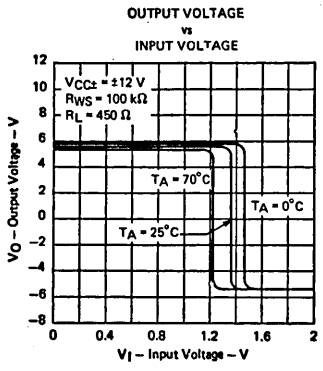


FIGURE 3

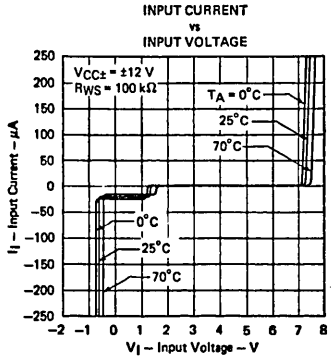


FIGURE 4

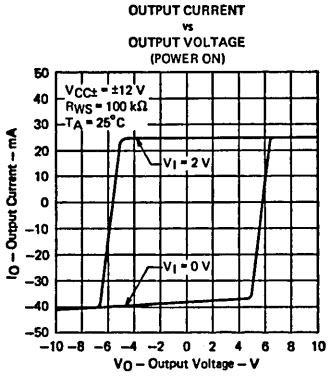


FIGURE 5

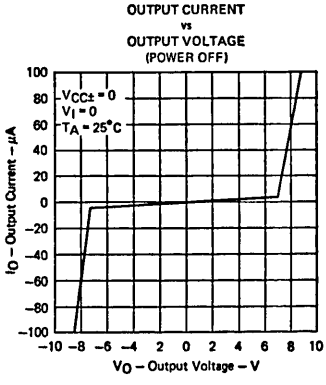


FIGURE 6

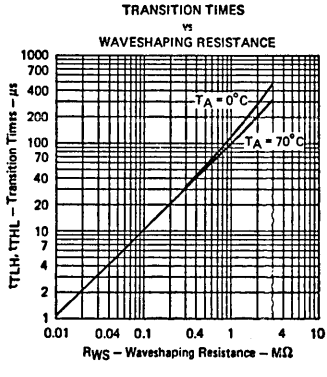


FIGURE 7

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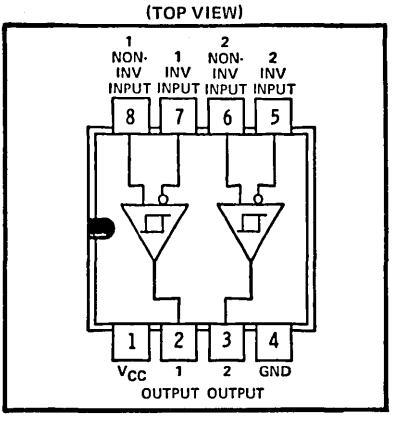
TYPE uA9637AC
DUAL DIFFERENTIAL LINE RECEIVER

BULLETIN NO. DL-S 12775, SEPTEMBER 1980

- Meets EIA Standards RS-422A and RS-423A
- Meets Federal Standards 1020 and 1030
- Operates from Single 5-V Power Supply
- Wide Common-Mode Input Voltage Range
- High Input Impedance
- TTL-Compatible Outputs
- High-Speed Schottky Circuitry
- 8-Pin Dual-In-Line Package

JG OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)



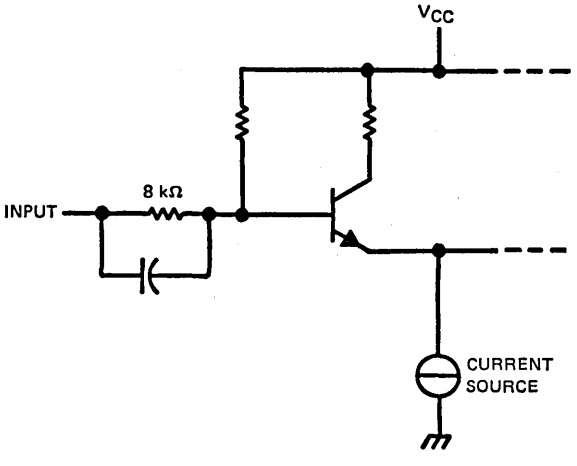
description

The uA9637AC is a dual differential line receiver designed to meet EIA standards RS-422A and RS-423A. It utilizes Schottky† circuitry and has TTL-compatible outputs. The inputs are compatible with either a single-ended or a differential-line system. This device operates from a single 5-volt power supply and is supplied in an 8-pin dual-in-line package.

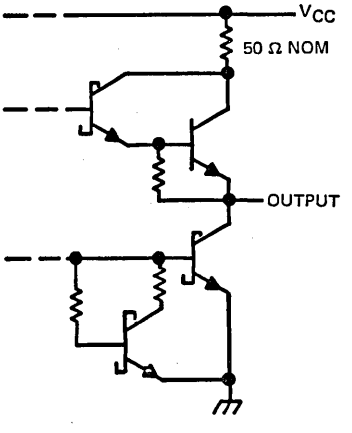
The uA9637AC is characterized for operation from 0°C to 70°C.

schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



TYPICAL OF ALL OUTPUTS



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†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U.S. Patent Number 3,463,975.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC} (see Note 1) . . . . . −0.5 V to 7 V
Input voltage . . . . . ±15 V
Differential input voltage (see Note 2) . . . . . ±15 V
Output voltage (see Note 1) . . . . . −0.5 V to 5.5 V
Low-level output current . . . . . 50 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 3):
JG package . . . . . 825 mA
P package . . . . . 1000 mA
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch (1,6 mm) from case for 60 seconds: JG package . . . . . 300°C
Lead temperature 1/16 inch (1,6 mm) from case for 10 seconds: P package . . . . . 260°C

NOTES: 1. All voltage values, except differential-input voltage, are with respect to the network ground terminal.
2. Differential-input voltage is measured at the noninverting input with respect to the corresponding inverting input.
3. For operation above 25°C free-air temperature, derate the JG package to 528 mW at 70°C at the rate of 6.6 mW/°C and the P package to 640 mW at 70°C at the rate of 8.0 mW. In the JG package, uA9637AC chips are glass-mounted.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Common-mode input voltage, V_{IC}			±7	V
Operating free-air temperature, T_A	0	25	70	°C

electrical characteristics over recommended ranges of supply voltage, common-mode input voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
					See Note 4		
V_T	Threshold voltage (V_{T+} and V_{T-})			−0.2		0.2	V
		See Note 5		−0.4		0.4	
$V_{T+} - V_{T-}$	Hysteresis				70		mV
V_{OH}	High-level output voltage	V_{ID} = 0.2 V,	I_O = −1 mA	2.5	3.5		V
V_{OL}	Low-level output voltage	V_{ID} = −0.2 V,	I_O = 20 mA		0.35	0.5	V
I_I	Input current	V_{CC} = 0 to 5.5 V,	V_I = 10 V		1.1	3.25	mA
		See Note 6	V_I = −10 V		−1.6	−3.25	
I_{OS}	Short-circuit input current‡	V_O = 0,	V_{ID} = 0.2 V	−40	−75	−100	mA
I_{CC}	Supply current	V_{ID} = −0.5 V,	No load		35	50	mA

†All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡Only one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTES: 4. The algebraic convention, where the less-positive (more-negative) limit is designated as minimum, is used in this data sheet for threshold levels only.
5. The expanded threshold parameter is tested with a 500-Ω resistor in series with each input.
6. The input not under test is grounded.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 30 pF, See Figure 1		15	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output			13	25	ns

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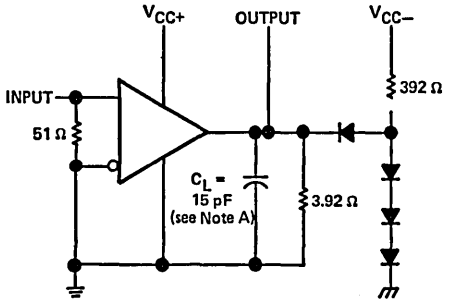
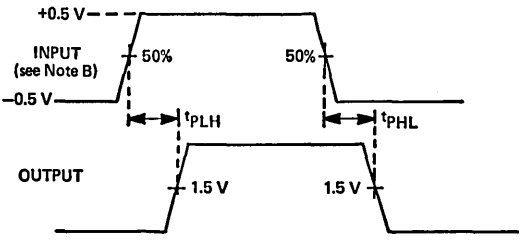
PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORM

NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: $t_r \leq 5$ ns, $t_f = 5$ ns, PRR = 5 MHz, duty cycle = 10%.

FIGURE 1—TRANSITION TIMES

TYPICAL CHARACTERISTICS

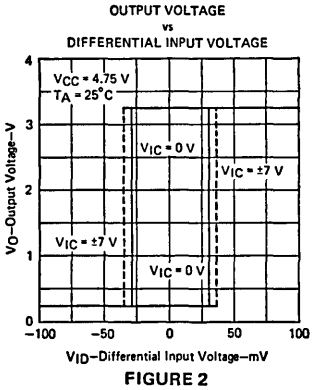


FIGURE 2

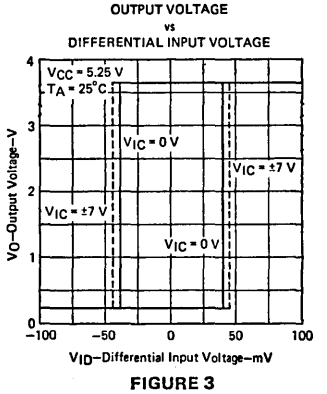


FIGURE 3

TYPICAL APPLICATION DATA

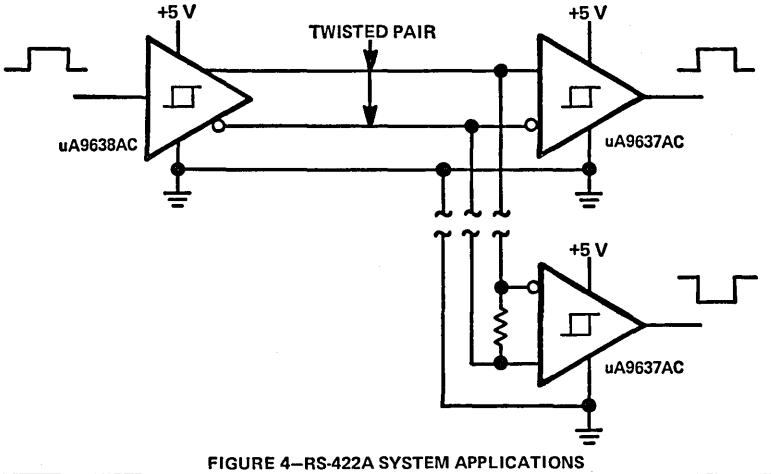


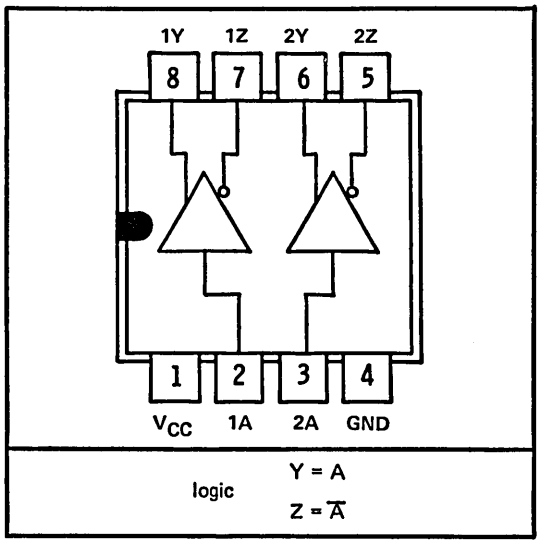
FIGURE 4—RS-422A SYSTEM APPLICATIONS

TYPE uA9638C
DUAL HIGH-SPEED DIFFERENTIAL LINE DRIVER

BULLETIN NO. DL-S 12780, OCTOBER 1980

- Meets EIA Standard RS-422A
- Operates From a Single 5-V Supply
- TTL and CMOS Input Compatibility
- Output Short-Circuit Protection
- Schottky Circuitry
- Designed to be Interchangeable with Fairchild 9638

JG OR P DUAL-IN-LINE PACKAGE
(TOP VIEW)



logic $Y = A$, $Z = \overline{A}$

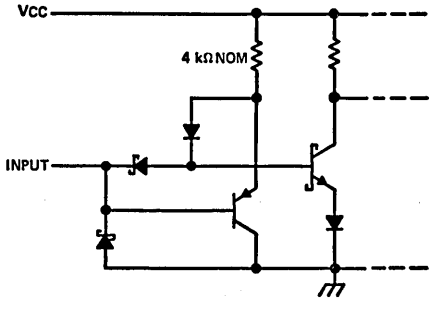
description

The uA9638C is a dual high-speed differential line driver designed to meet EIA Standard RS-422A. The inputs are TTL- and CMOS-compatible and have input clamp diodes. Schottky-diode-clamped transistors† are used to minimize propagation delay time. This device operates from a single 5-volt power supply and is supplied in an 8-pin dual-in-line package.

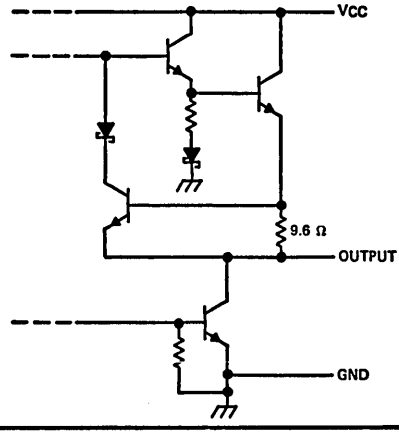
The uA9638C is characterized for operation from 0°C to 70°C.

schematics of inputs and outputs

EQUIVALENT OF EACH INPUT



TYPICAL OF ALL OUTPUTS



absolute maximum rating over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC} (see Note 1)	−0.5 V to 7 V
Input voltage range	−0.5 V to 7 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2):	800 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch (1,6 mm) from case for 30 seconds: JG package	300°C
Lead temperature 1/16 inch (1,6 mm) from case for 10 seconds: P package	260°C

NOTES: 1. Voltage values except differential output voltages are with respect to the network ground terminal.
2. For operation above 25°C free-air temperature, refer to Dissipation Derating Table.

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†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U.S. Patent Number 3,463,975.

DISSIPATION DERATING TABLE

PACKAGE	POWER RATING	DERATING FACTOR	ABOVE T_A
JG (Glass-Mounted Chip)	800 mW	6.6 mW/°C	29°C
P	800 mW	8.0 mW/°C	50°C

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level output current, I_{OH}			−50	mA
Low-level output current, I_{OL}			50	mA
Operating free-air temperature, T_A	0		70	°C

electrical characteristics over operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS†			MIN	TYP†	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_{IK}	Input clamp voltage	V_{CC} = 4.75 V,	I_I = −18 mA			−1	−1.2	V
V_{OH}	High level output voltage	V_{CC} = 4.75 V, V_{IL} = 0.8 V	V_{IH} = 2 V,	I_{OH} = −10 mA	2.5	3.5		V
				I_{OH} = −40 mA	2			
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V, I_{OL} = 40 mA	V_{IH} = 2 V,	V_{IL} = 0.8 V,			0.5	V
$\lvert V_{OD1}\rvert$	Differential output voltage	V_{CC} = 5.25 V,	I_O = 0				$2V_{OD2}$	V
$\lvert V_{OD2}\rvert$	Differential output voltage	V_{CC} = 4.75 V to 5.25 V, R_L = 100 Ω, See Figure 1			2			V
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of‡ differential output voltage						±0.4	V
V_{OC}	Common-mode output voltage§						3	V
$\Delta\lvert V_{OC}\rvert$	Change in magnitude of‡ common-mode output voltage						±0.4	V
I_O	Output current with power off	V_{CC} = 0,		V_O = 6 V		0.1	100	μA
				V_O = −0.25 V		−0.1	−100	
				V_O = −0.25 V to 6 V			±100	
I_I	Input current	V_{CC} = 5.25 V,	V_I = 5.5 V				50	μA
I_{IH}	High-level input current	V_{CC} = 5.25 V,	V_I = 2.7 V				25	μA
I_{IL}	Low-level input current	V_{CC} = 5.25 V,	V_I = 0.5 V				−200	μA
I_{OS}	Short-circuit output current¶	V_{CC} = 5.25 V,			−50		−150	mA
I_{CC}	Supply current (all drivers)	V_{CC} = 5.25 V,	No load,	All inputs at 0 V		45	65	mA

†All typical values are at V_{CC} = 5 V and T_A = 25°C.
‡$\Delta\lvert V_{OD}\rvert$ and $\Delta\lvert V_{OC}\rvert$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
§In EIA Standard RS-422A, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.
¶Only one output at a time should be shorted and duration of the short-circuit should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
t_{DD}	Differential-output delay time	C_L = 15 pF, R_L = 100 Ω, See Figure 2		10	15	ns
t_{TD}	Differential-output transition time			10	15	ns
	Skew			1		ns

PARAMETER MEASUREMENT INFORMATION

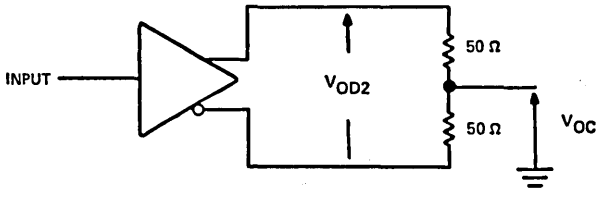
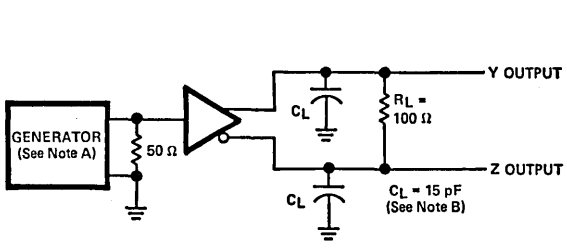
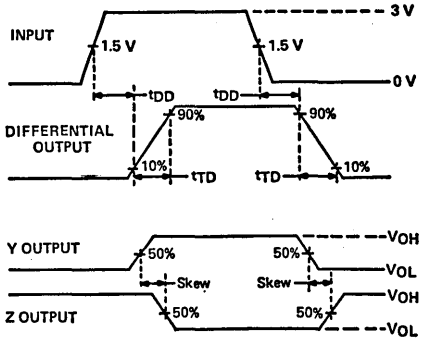


FIGURE 1– DIFFERENTIAL AND COMMON-MODE OUTPUT VOLTAGES



TEST CIRCUIT



VOLTAGE WAVEFORM

NOTES: a. The input pulse generator has the following characteristics: Z_{OUT} = 50 Ω, PRR = 500 kHz, t_w = 100 ns, t_r = ≤ 5 ns.
b. C_L includes probe and jig capacitance.

FIGURE 2 – SWITCHING TIMES

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introduction

The systems designer is constantly faced with the problem of interfacing subsystems and of transmitting data over a distance, whether it is a few inches on a circuit board or many feet to another unit in the system. The quality of the signal reproduced in the receiving unit is dependent on:

A. Transmission line characteristics
   1. Length and attenuation
   2. Geometry (single wire, coaxial, parallel wires, twisted pair, shielded or unshielded, etc.)
      a. Characteristic impedance and line termination
      b. Distributed capacitance and inductance

B. General layout and noise environment

C. Receiver characteristics
   1. Input impedance
   2. Sensitivity, hysteresis, and input threshold
   3. Frequency response (switching time)

D. Driver characteristics
   1. Output impedance
   2. Output peak current capability
   3. Frequency response

E. Bit rate and pulse duration $\left(\text{bit rate} = \frac{2}{\text{period}}\right)$

The impact of many of these factors is discussed on the following pages and in several data sheets. Other applications where line circuit characteristics can be used to advantage are also discussed. For convenient access to all the application information in this data book, a topical index is provided on the next page.

additional circuit design information

Bulletin CA-130, *Line Drivers and Receivers: SN55107 Series*, and Bulletin CA-146, *Data Transmission with SN55107 Series*, are available from Texas Instruments upon request.

The Texas Instruments videotape course "Linear and Interface Integrated Circuits" is available for a nominal fee.

INDEX TO APPLICATION TOPICS

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line terminations

The voltage across an impedance terminating a transmission line is a function of the real and imaginary components of the impedance, the characteristic impedance of the line, and the incident power. When the impedance is a pure resistance (see Note 1) and the transmission line is ideal, then:

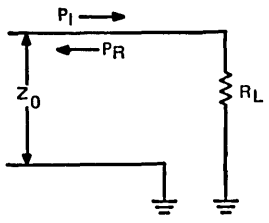


FIGURE 1

$$P_R = P_I \left(\frac{R_L - Z_0}{R_L + Z_0} \right)^2 \quad (1)$$

$$P_L = P_I - P_R = P_I \left[1 - \left(\frac{R_L - Z_0}{R_L + Z_0} \right)^2 \right] \quad (2)$$

$$V_L = \sqrt{P_L R_L} = \sqrt{I_L^2 R_L^2} \quad (3)$$

where

P_I = incident power
P_R = reflected power
R_L = load resistance
P_L = power delivered to R_L
Z_0 = line characteristic impedance

When $R_L = Z_0$, the numerators of the fractional terms in Equations 1 and 2 become zero and the reflected power is zero. With reflections reduced to zero, one source of signal distortion and noise is eliminated. Equation 3 shows the relationship between P_L, R_L, V_L, and I_L.

In line circuit design R_L is a lumped value representing the combination of a termination resistor and the input resistance of a line receiver.

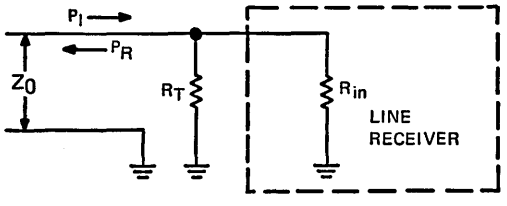


FIGURE 2

$$V_L = \sqrt{P_L \frac{R_{in} \times R_T}{R_{in} + R_T}} \quad (4)$$

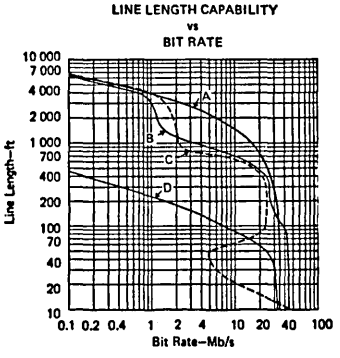
When $R_{in} \gg R_T$, the incoming signal power and noise power are shunted to ground by R_T, decreasing the effective power to the input of the receiver.

NOTE 1: The assumption that the terminating impedance is a pure resistance simplifies this discussion. In practice, the reactive components of impedance can usually be neglected.

line terminations (continued)

Figure 3 illustrates how much the line length versus bit rate boundary for acceptable TTL signals was affected by variation of the termination resistor values. Case A clearly provides the best capability for high bit rates and long transmission lines, while Cases B and C show irregularities primarily due to reflected signals.

	R1	R2
Case A	100 Ω	100 Ω
Case B	∞	100 Ω
Case C	∞	122 Ω
Case D	∞	205 Ω



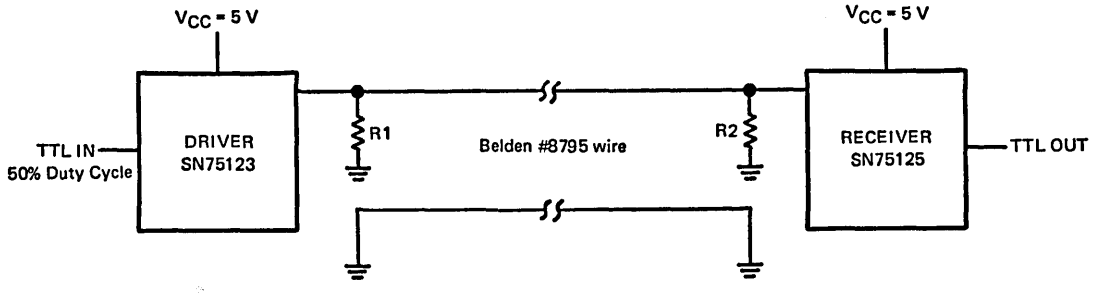
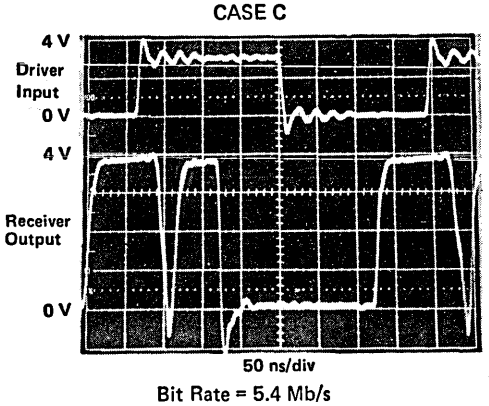


FIGURE 3

The voltage waveform for Case C at a line length of 50 feet shows a large negative transient in the receiver output due to a reflection. At 10 feet, the bit rate capability (see Figure 3) has increased to 45 Mb/s compared to 47 Mb/s for Case B.



Bit Rate = 5.4 Mb/s
Line Length = 50 feet
VOLTAGE WAVEFORM

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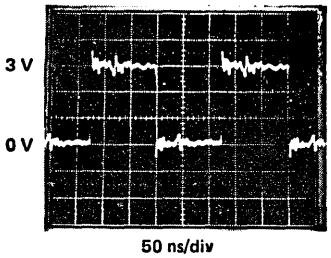
line terminations (continued)

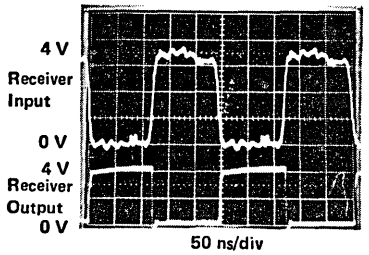
The waveforms below offer an interesting comparison of the driver input signal to the resulting signals that appear at the receiver input and at the receiver output. The circuit of Figure 3 with 100 feet of line and a bit rate of 2 Mb/s was used. Note that the pulse duration for Case D receiver output is much shorter than the apparent duration of the input pulse. Case C, with somewhat less distortion, produces input and output pulse widths of about the same value.

VOLTAGE WAVEFORMS

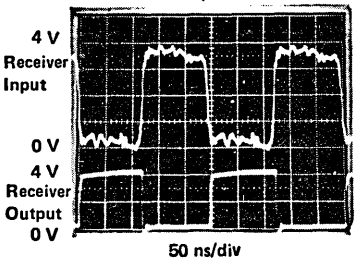
INPUT TO DRIVER



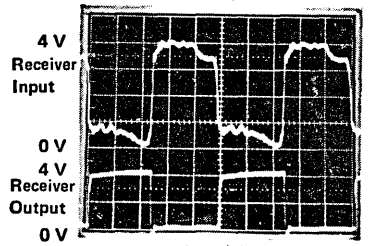
CASE A



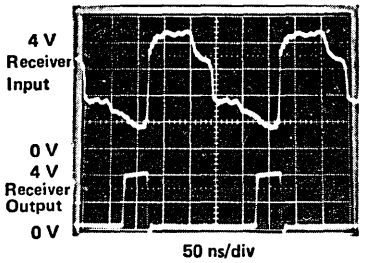
CASE B



CASE C



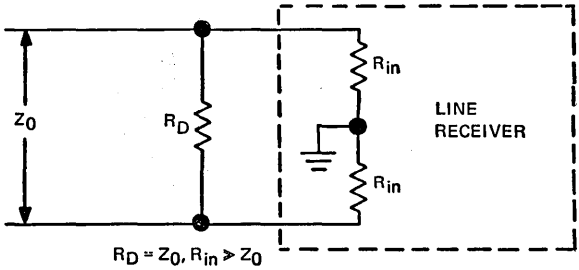
CASE D

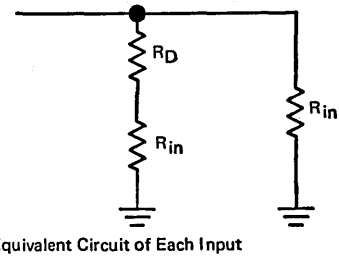


noise

The environment of any transmission line will produce noise from many sources. That noise will be transmitted to the input of the line receiver and can cause severe signal distortion. The familiar differential-line technique has provided a means of reducing the effect of common-mode noise on low-level signals in linear, digital, and rf transmission for some time, and is thoroughly discussed in the literature. One method of reducing the common-mode noise on balanced lines will be presented in this topic.

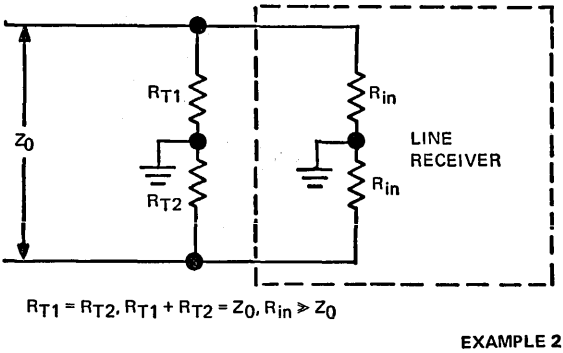
The noise power present on a line terminated in a resistance will act in the same manner as the signal power in Equations 1 through 4 under Line Terminations. Specifically, the noise will be shunted to ground and will not provide power to the receiver input if the line is terminated in a low-value resistor to ground. Examples 1 and 2 below show two typical means of terminating differential lines at the receiver.

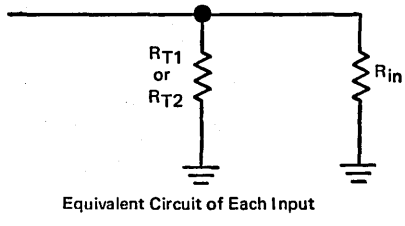




EXAMPLE 1

Since the shunting resistance, $R_D + R_{in}$, is high, most of the noise on each conductor will appear at the receiver input.





EXAMPLE 2

Most of the noise power on each conductor of the balanced line will be shunted to ground by R_{T1} or R_{T2} because of their low value compared to R_{in}.

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noise (continued)

Figure 1 below illustrates the effectiveness of the differential-line technique in rejecting noise from an external source.

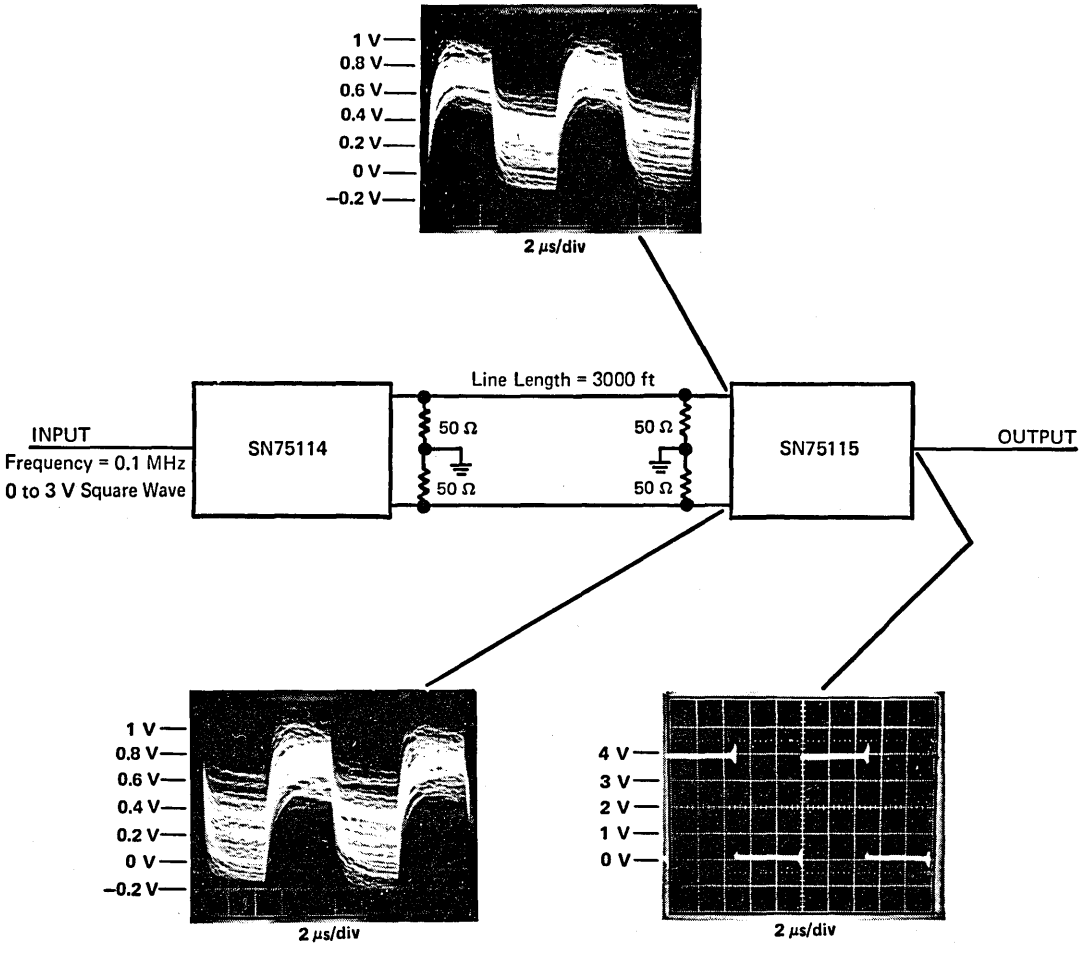


FIGURE 1

line length capability vs bit rate

The data presented in this section is intended to assist the designer who must choose a combination of line driver and receiver to meet line length and bit rate requirements. It does not represent the complete set of available options, but offers a means of comparison for many device types in typical applications. Each graph is associated with a specific line termination scheme, and all measurements utilized Belden #8795 wire as transmission line (see Note 1).

The duty cycle value refers to the time at TTL high level divided by the period length.

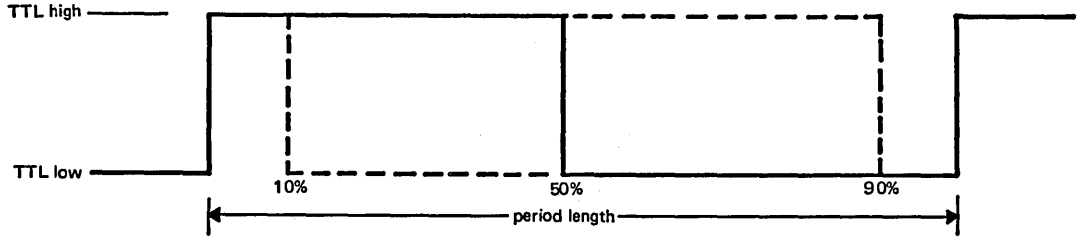


FIGURE 1– PERIOD AND DUTY CYCLE

Duty cycle and bit rate values will yield the high-level pulse duration by means of the formula:

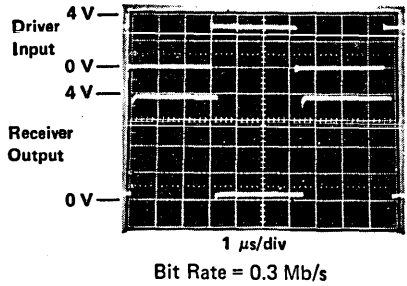
$$\text{Pulse duration} = \text{period} \times \text{duty cycle} = \frac{2}{\text{bit rate}} \times \text{duty cycle}$$

The data on the following pages was obtained in each case by monitoring the output of the receiver. Acceptable waveforms exhibited:

1. TTL low level less than 0.4 V
2. TTL high level greater than 2.4 V
3. No oscillations

Figures 2 and 3 show examples of acceptable and unacceptable voltage waveforms with regard to oscillations of the SN75112 driver and SN75207 receiver.

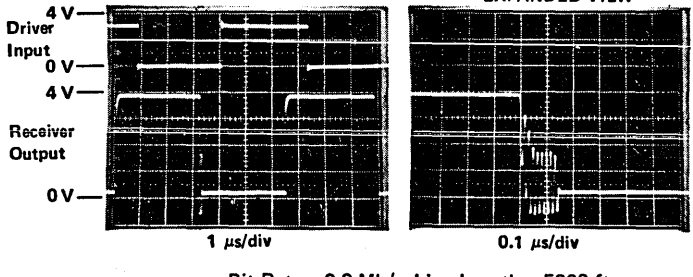
ACCEPTABLE VOLTAGE WAVEFORM



Bit Rate = 0.3 Mb/s
Line Length = 2000 ft

FIGURE 2

UNACCEPTABLE VOLTAGE WAVEFORMS



Bit Rate = 0.3 Mb/s, Line Length = 5000 ft

FIGURE 3

NOTE 1: Belden #8795 twisted-pair wire is 22 AWG and exhibits the following characteristics: $Z_O \approx 100\ \Omega$, C ≈ 15 pF/ft, propagation delay ≈ 1.3 ns/ft.

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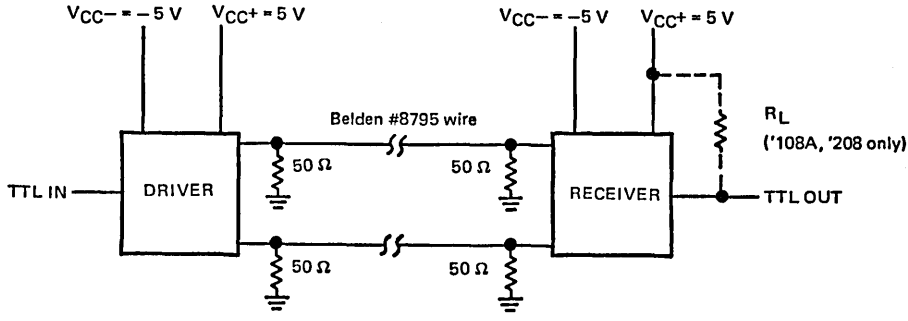
LINE LENGTH CAPABILITY vs BIT RATE

INDEX TO DATA

DRIVER APPLICATIONS	
TYPE	FIGURE NUMBERS
SN75109A	4, 7
SN75110A	5, 8
SN75112	6, 9
SN75113	10, 13
SN75114	10, 13
SN75116	42
SN75117	43
SN75121	31
SN75123	32, 33
SN75138	34
SN75150	37, 38
SN75158	41
SN75183	11, 14
SN75188	35, 36, 39, 40
SN75450B	44
SN75451B	16, 17, 18, 19, 20
SN75361A	21, 22, 23, 24, 25
DS8831	12, 15, 26, 27, 28, 29, 30
DS8832	12, 15, 26, 27, 28, 29, 30

RECEIVER APPLICATIONS	
TYPE	FIGURE NUMBERS
SN75107A	4, 5, 6
SN75108A	7, 8, 9
SN75115	13, 14, 15, 16, 21
SN75116	42
SN75117	43
SN75122	17, 22, 26, 31
SN75124	27, 32
SN75125	28, 33
SN75127	28, 33
SN75138	34
SN75140	18, 23, 29
SN75152	19, 24, 30, 38, 44
SN75154	37
SN75182	10, 11, 12, 20, 25
SN75189	35, 39
SN75189A	36, 40
SN75207	4, 5, 6
SN75208	7, 8, 9, 41

LINE LENGTH CAPABILITY vs BIT RATE



MEASUREMENT INFORMATION FOR FIGURES 4 THRU 9

DRIVER SN75109A
RECEIVER SN75107A, SN75207

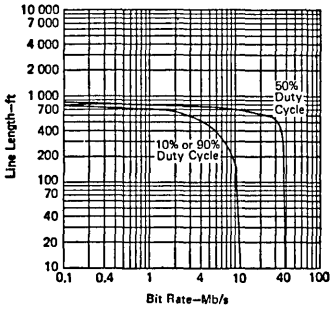


FIGURE 4

DRIVER SN75110A
RECEIVER SN75107A, SN75207

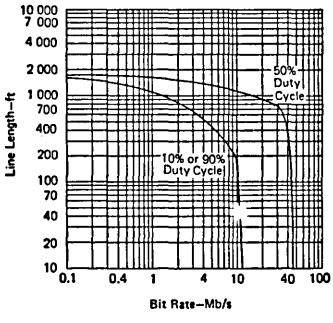


FIGURE 5

DRIVER SN75112
RECEIVER SN75107A, SN75207

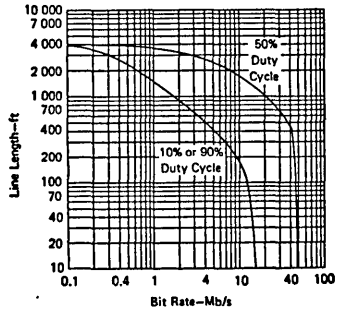


FIGURE 6

DRIVER SN75109A
RECEIVER SN75108A, SN75208

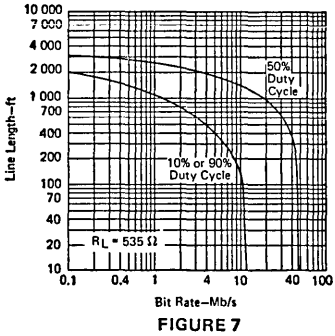


FIGURE 7

DRIVER SN75110A
RECEIVER SN75108A, SN75208

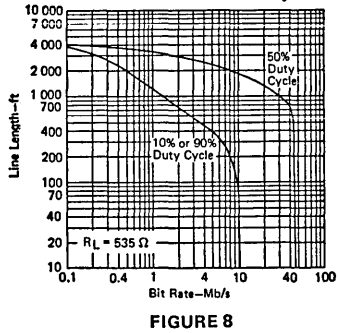


FIGURE 8

DRIVER SN75112
RECEIVER SN75108A, SN75208

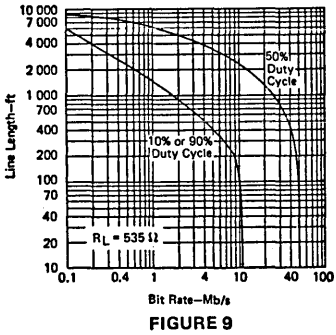
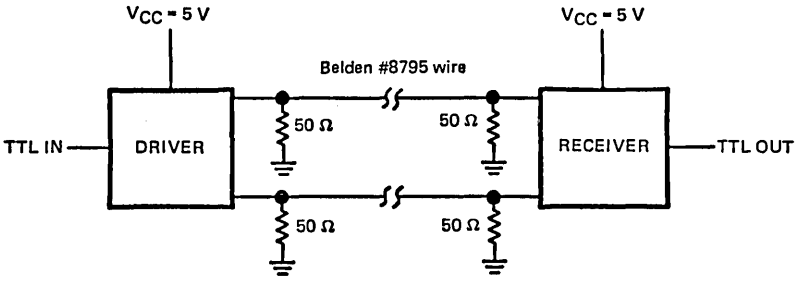


FIGURE 9

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

LINE LENGTH CAPABILITY vs BIT RATE



MEASUREMENT INFORMATION FOR FIGURES 10 THRU 15

DRIVER . .SN75113, SN75114
RECEIVER SN75182

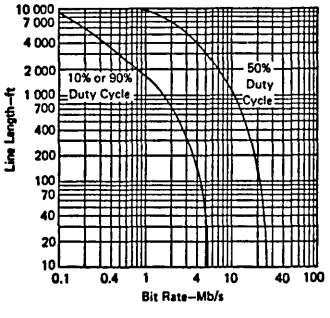


FIGURE 10

DRIVER SN75183
RECEIVER SN75182

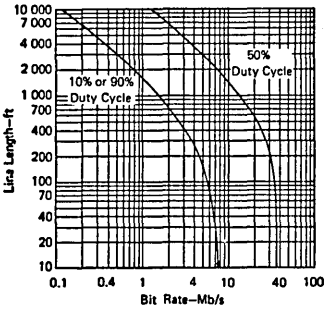


FIGURE 11

DRIVER . . .DS8831, DS8832
RECEIVER SN75182

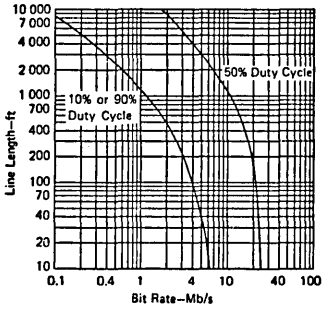


FIGURE 12

DRIVER . .SN75113, SN75114
RECEIVER SN75115

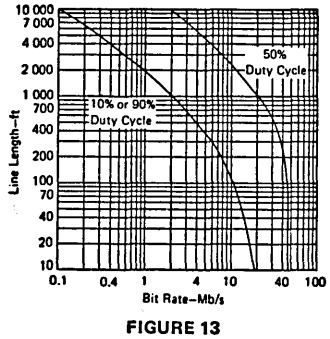


FIGURE 13

DRIVER SN75183
RECEIVER SN75115

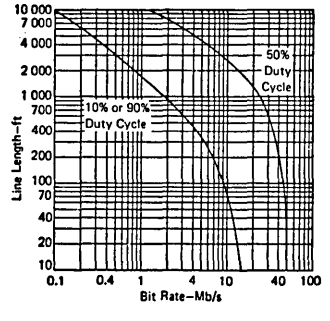


FIGURE 14

DRIVER . . .DS8831, DS8832
RECEIVER SN75115

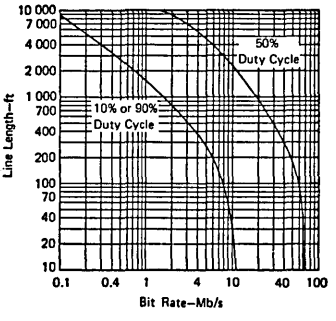
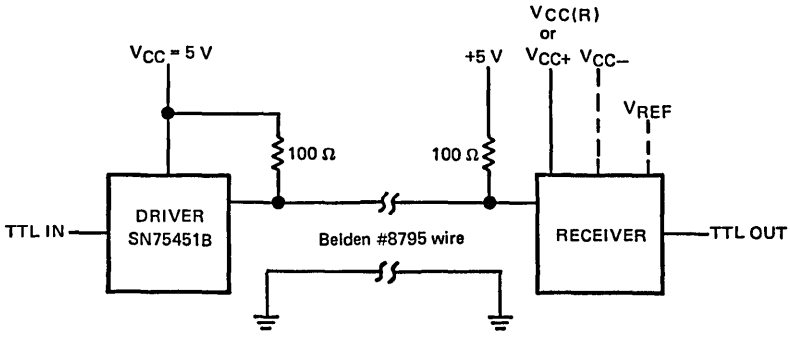


FIGURE 15

LINE LENGTH CAPABILITY vs BIT RATE



MEASUREMENT INFORMATION FOR FIGURES 16 THRU 20

RECEIVER SN75115

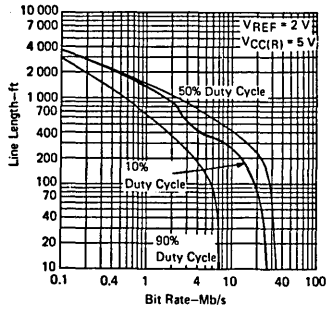


FIGURE 16

RECEIVER SN75122

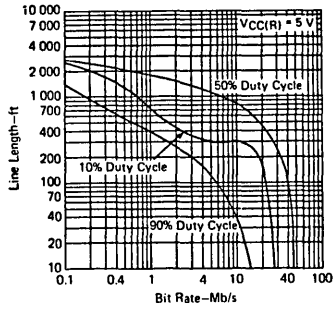


FIGURE 17

RECEIVER SN75140

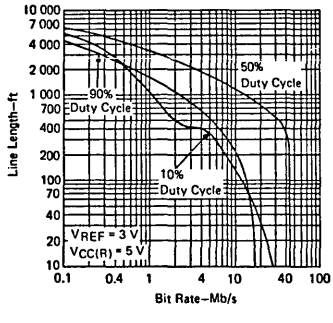


FIGURE 18

RECEIVER SN75152

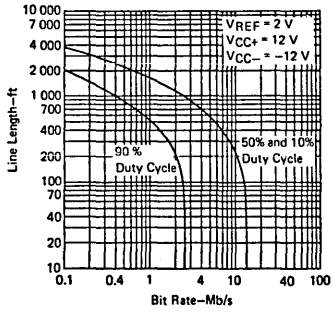


FIGURE 19

RECEIVER SN75182

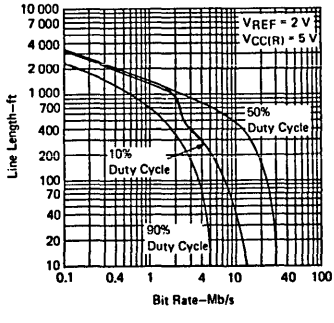


FIGURE 20

TEXAS INSTRUMENTS
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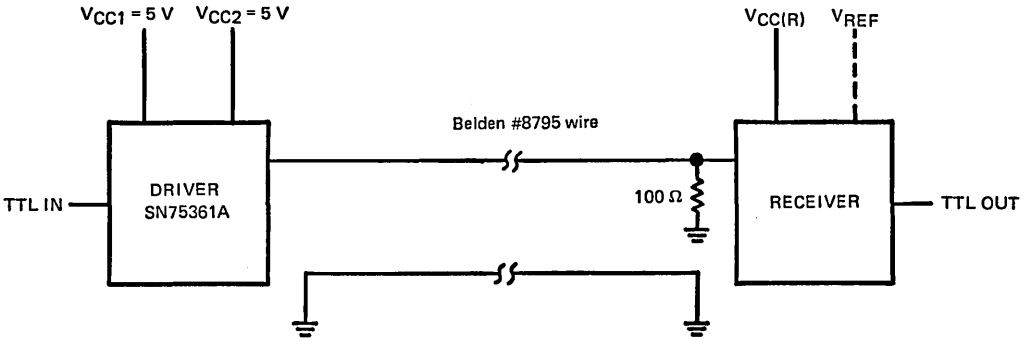
LINE LENGTH CAPABILITY vs BIT RATE



MEASUREMENT INFORMATION FOR FIGURES 21 THRU 25

RECEIVER SN75115

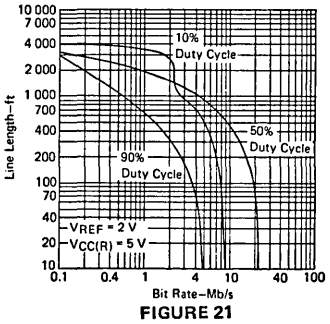


FIGURE 21

RECEIVER SN75122

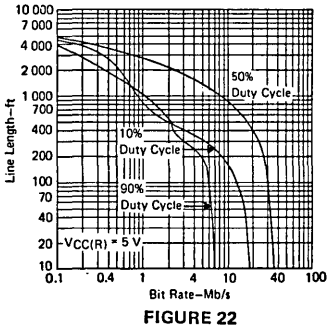


FIGURE 22

RECEIVER SN75140

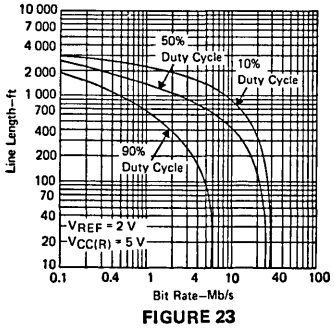


FIGURE 23

RECEIVER SN75152

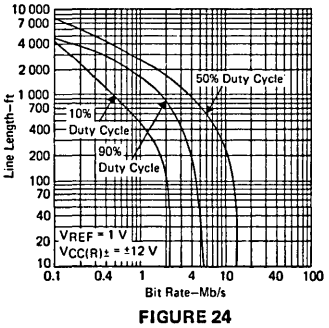


FIGURE 24

RECEIVER SN75182

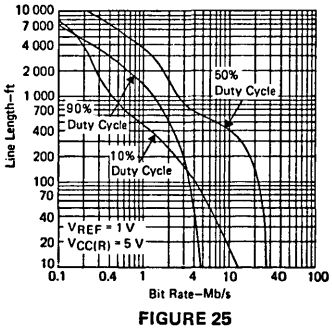
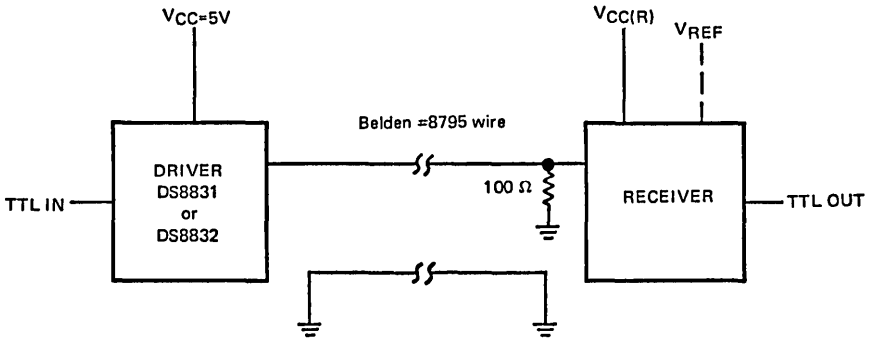


FIGURE 25

LINE LENGTH CAPABILITY vs BIT RATE



MEASUREMENT INFORMATION FOR FIGURES 26 THRU 30

RECEIVER . . . SN75122

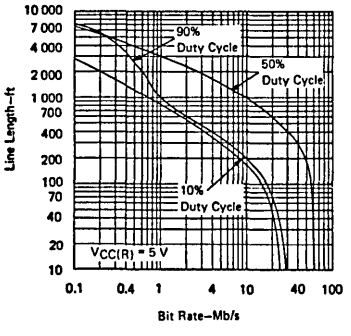


FIGURE 26

RECEIVER SN75124

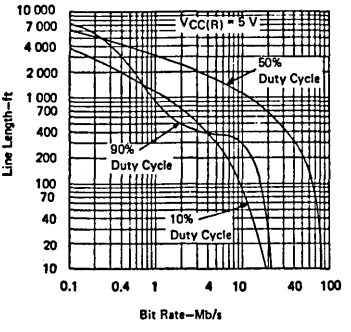


FIGURE 27

RECEIVER SN75125, SN75127

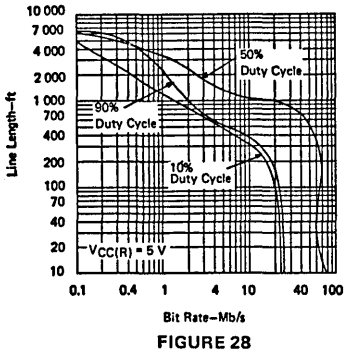


FIGURE 28

RECEIVER SN75140

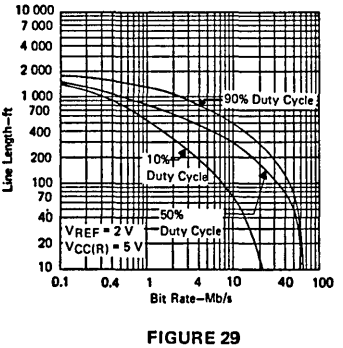


FIGURE 29

RECEIVER SN75152

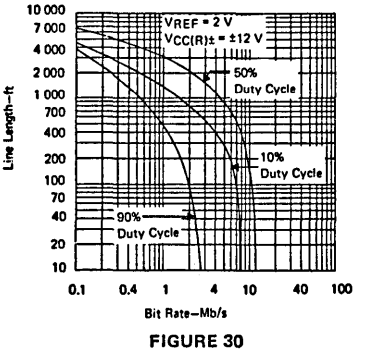


FIGURE 30

TEXAS INSTRUMENTS
INCORPORATED
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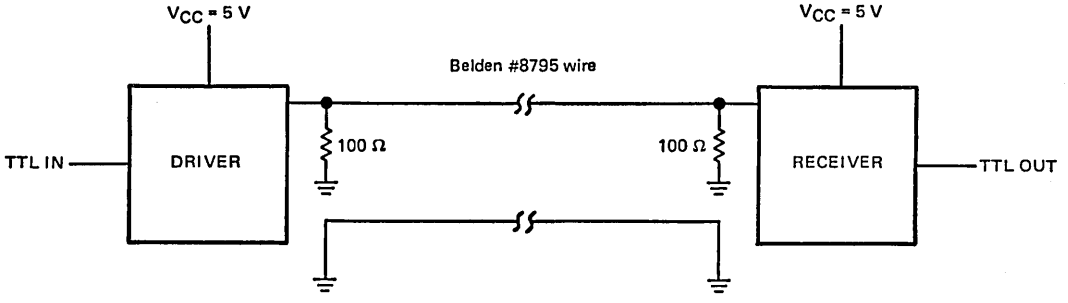
LINE LENGTH CAPABILITY vs BIT RATE



MEASUREMENT INFORMATION FOR FIGURES 31 THRU 33

DRIVER SN75121
RECEIVER SN75122

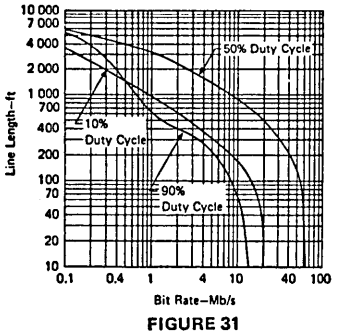


FIGURE 31

DRIVER SN75123
RECEIVER SN75124

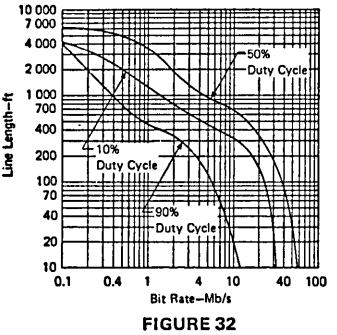


FIGURE 32

DRIVER SN75123
RECEIVER SN75125, SN75127

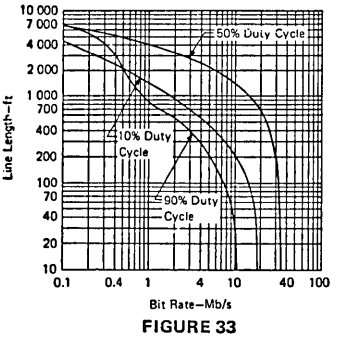
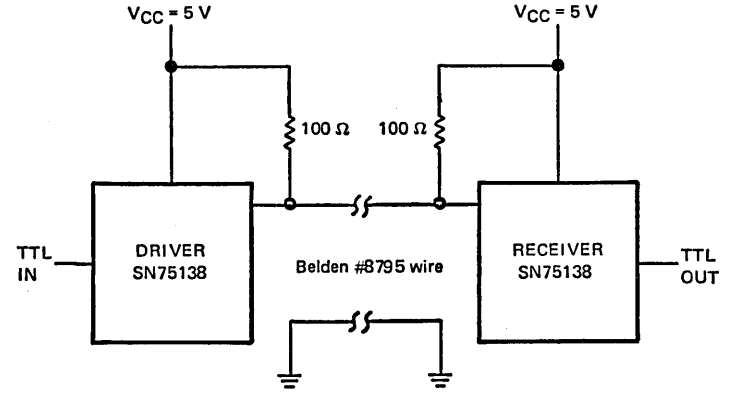


FIGURE 33



MEASUREMENT INFORMATION FOR FIGURE 34

DRIVER SN75138
RECEIVER SN75138

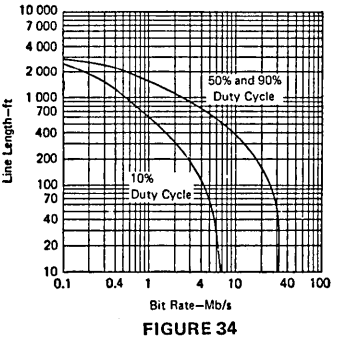
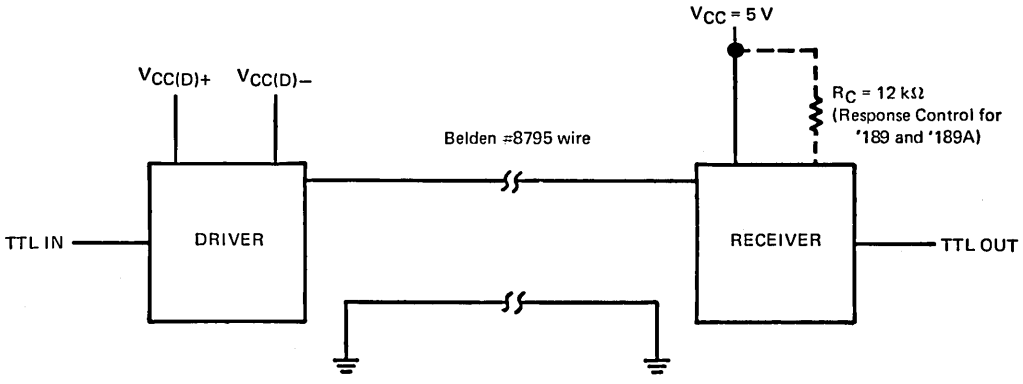


FIGURE 34

LINE LENGTH CAPABILITY vs BIT RATE



MEASUREMENT INFORMATION FOR FIGURES 35 thru 37

DRIVER SN75188
RECEIVER SN75189

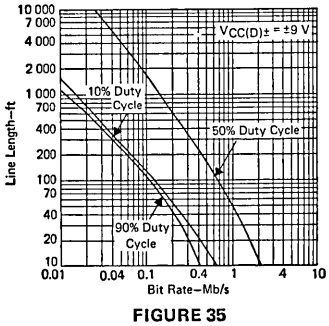


FIGURE 35

DRIVER SN75188
RECEIVER SN75189A

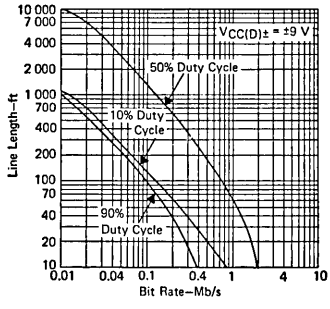


FIGURE 36

DRIVER SN75150
RECEIVER SN75154

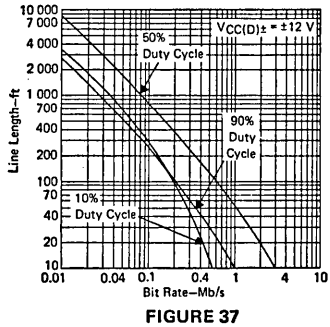
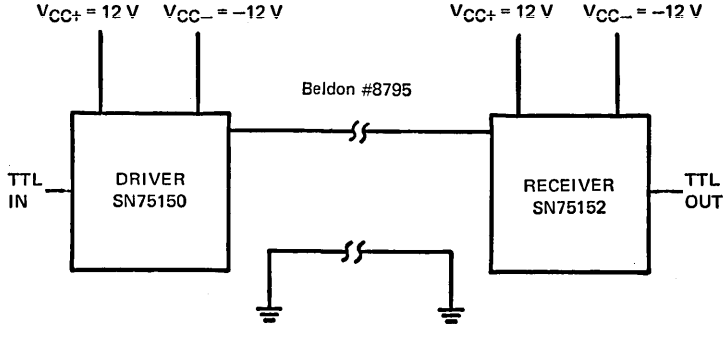


FIGURE 37



DRIVER SN75150
RECEIVER SN75152

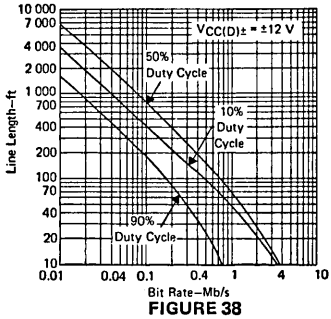


FIGURE 38

MEASUREMENT INFORMATION FOR FIGURE 38

TEXAS INSTRUMENTS
INCORPORATED
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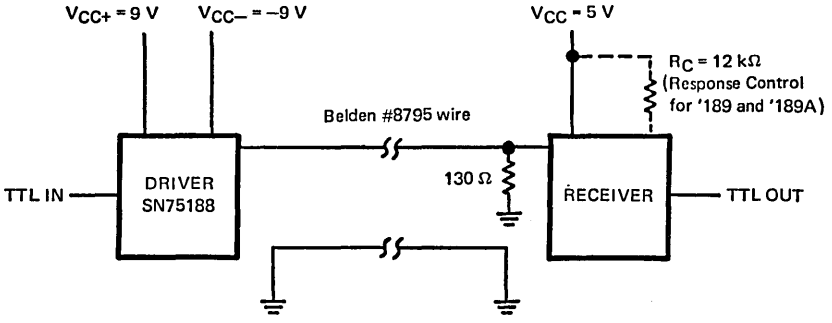
LINE LENGTH CAPABILITY vs BIT RATE



MEASUREMENT INFORMATION FOR FIGURES 39 AND 40

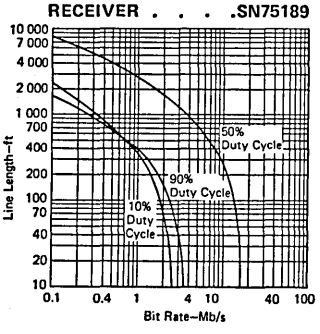


FIGURE 39

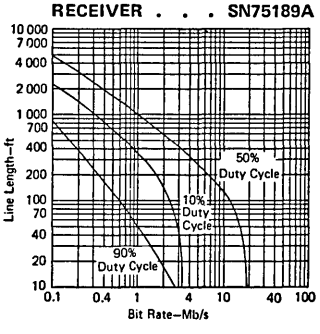
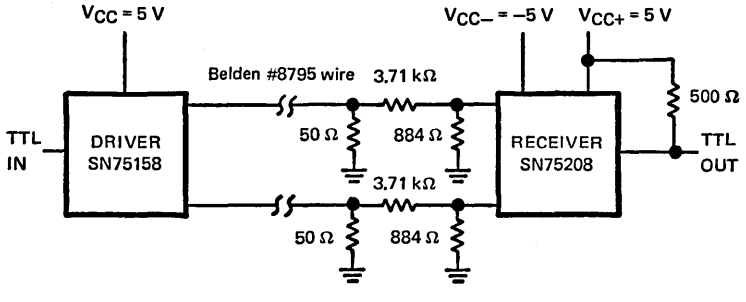


FIGURE 40



MEASUREMENT INFORMATION FOR FIGURE 41

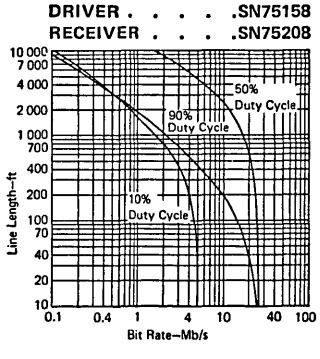
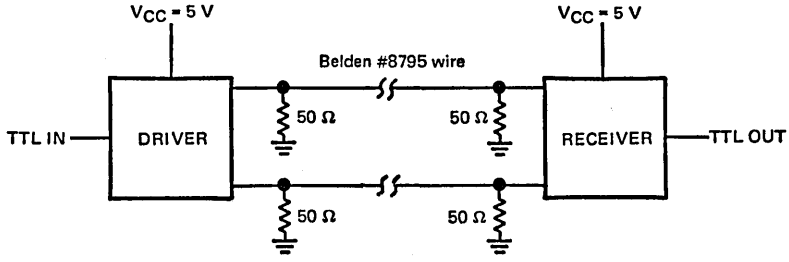


FIGURE 41

LINE LENGTH CAPABILITY vs BIT RATE



MEASUREMENT INFORMATION FOR FIGURES 42 AND 43

DRIVER SN75116
RECEIVER SN75116

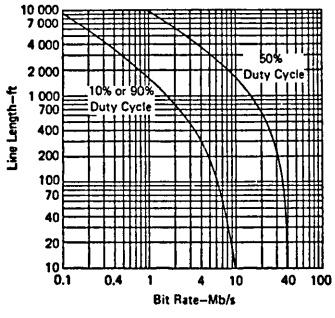


FIGURE 42

DRIVER SN75117
RECEIVER SN75117

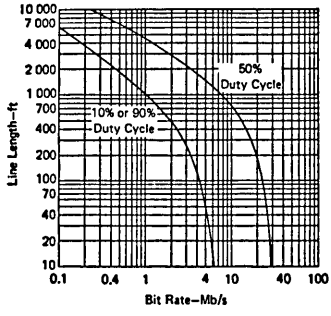
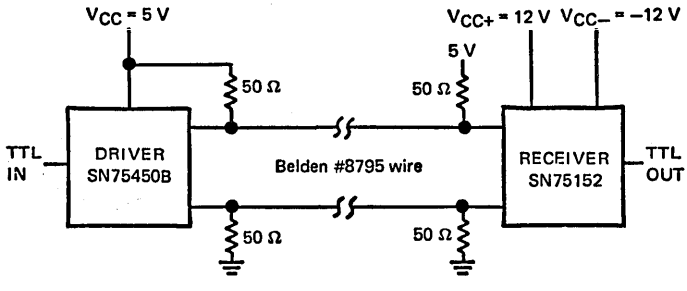


FIGURE 43



MEASUREMENT INFORMATION FOR FIGURE 44

DRIVER SN75450B
RECEIVER SN75152

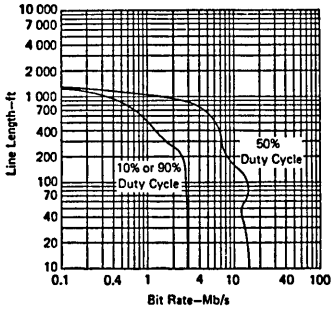


FIGURE 44

TEXAS INSTRUMENTS
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